Phase Change Memory: Fundamentals and Measurement Techniques

Alexander Pronin, Lead Applications Engineer
Keithley Instruments, Inc.

PHASE CHANGE MEMORY (variously abbreviated as PCM, PRAM, or PCRAM) is an emerging non-volatile computer memory technology. It may someday replace flash memory because it is not only much faster and scaleable to smaller dimensions than flash memory, but it's also more resilient, offering up to 100 million write cycles. This article will address the underlying technology of phase change memory devices and the latest techniques for testing them.

What is PCM and how does it work?

A PCM cell is a tiny chunk of a chalcogenide alloy that can be switched rapidly from an ordered crystalline phase (with low resistance) to a disordered, amorphous phase (with much higher resistance) through the focused application of heat in the form of an electrical pulse. These same materials are also widely used in the active layers of re-writable optical media such as CDs and DVDs. The switch from the crystalline to the amorphous phase and back is triggered by melting and quick cooling (or a slightly slower process known as re-crystallization). One of the most promising PCM materials is GST (germanium, antimony, and tellurium), which has a melting temperature in the range of 500º–600ºC.

The differing levels of resistivity of the crystalline and amorphous phases of these alloys are what allow them to store binary data. The high resistance amorphous state is used to represent a binary 0; the low resistance crystalline state represents a 1. The newest PCM designs and materials can achieve multiple distinct levels [1], for example, 16 crystalline states, not just two, each with different electrical properties. This allows a single cell to represent multiple bits, and to increase memory density substantially, which is currently done in flash memory.

The amorphous state vs. the crystalline state

A brief overview of the differences between the amorphous and crystalline states may help clarify how PCM devices work.

In the amorphous phase, the GST material has short-range atomic order and low free electron density, which results in higher resistivity. This is sometimes referred to as the RESET phase, because it is usually formed after a RESET operation, in which the temperature of the DUT is raised slightly above the melting point, then the GST is suddenly quenched to cool it. The rate of cooling is critical for the formation of the amorphous layer. The typical resistance of the amorphous layer can exceed one mega-ohm.

In the crystalline phase, the GST material has long-range atomic order and high free electronic density, which results in lower resistivity. This is also known as the SET phase because it is formed after a SET operation, in which the temperature of the material is raised above the

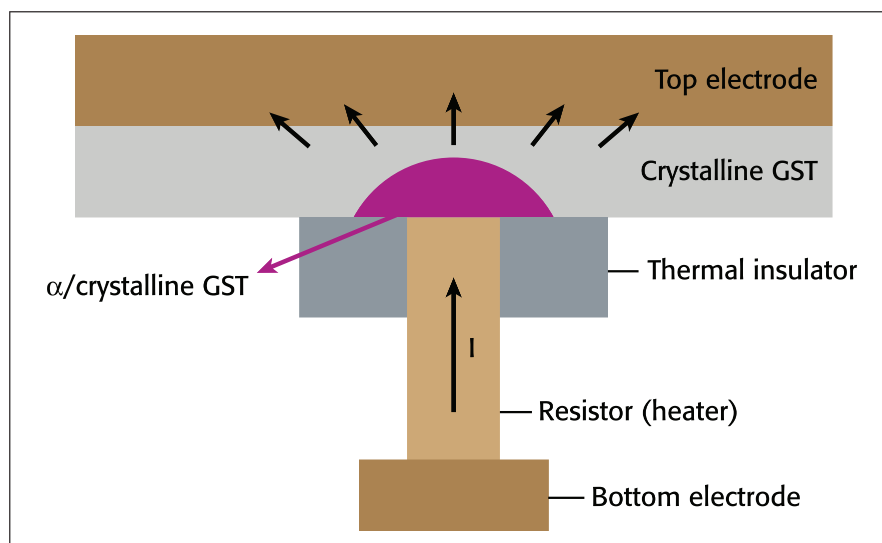

Figure 1. Typical PCM device structure.

re-crystallization temperature but below the melting point, then cooled slightly slower to allow crystalline grains to form throughout the layer. The typical resistance of the crystalline phase ranges from 1 to 10 kilo-ohms. The crystalline phase is a low energy state; therefore, when heat is applied to material in the amorphous phase and the temperature approaches the crystallization temperature, it tends to change spontaneously to the crystalline phase.

The structure of a PCM device

The schematic diagram in ***Figure 1*** illustrates the structure of a typical GST PCM device. The resistor is attached to the underside of the GST layer. Heating/melting affects only a small area around the tip of the resistor. Erase/RESET pulses set high resistance or logical 0 and form an area of an amorphous layer on the device. Erase/RESET pulses are higher, narrower, and steeper than Write/SET pulses. A SET pulse, which sets a logical 1, re-crystallizes the amorphous layer back to the crystalline state.

Pulse requirements for characterizing PCM devices

The voltage and current values of the RESET and SET pulses used should be carefully selected to produce melting and re-crystallization. RESET pulses should raise the temperature just above the melting point and then allow the material to cool rapidly to the amorphous phase. SET pulses should raise the temperature just above the re-crystallization temperature but below the melting point, and allow a longer time to cool it; therefore, the pulse width and fall time for a SET pulse should be longer than for a RESET pulse.

Pulse widths of one microsecond or shorter are usually sufficient. A pulse of this duration will produce enough energy either to melt PCM material or to re-crystallize it. Pulse voltages need to be as high as 6V, and it's desirable for them to be higher, to reach melting temperatures. Current values range from 0.3–3mA.

Fall time for a RESET pulse is a critical parameter [2]. The state of the PCM technology determines the required minimum for a fall time. Currently, it is a common requirement to have 30–50 nanoseconds. Newer materials will push that requirement to shorter fall times. If the pulse fall time is longer than that required time, the material may not effectively quench into an amorphous phase.

Critical parameters for characterizing PCM materials

The ability to develop new PCM materials and refine device designs will depend largely on manufacturers' ability to characterize several parameters:

- **Re-crystallization rate** – Current re-crystallization rates are now as short as several tens of nanoseconds, but they may soon drop to as little as a few nanoseconds. That will make reducing the time needed to make a measurement increasingly crucial.
- **Data retention** – As discussed previously, the SET phase is a lower energy state, and PCM materials tend to re-crystallize spontaneously. The rate of crystallization is temperature dependent. Therefore, data retention can be defined as a maximum temperature at which data, the RESET state, will remain unchanged and stable for a specified time period (typically 10 years).
- **Cycling endurance** – This is a measurement of how many times a memory cell can be successfully programmed to the 0 and 1 states. The newer multi-state memory cells with additional distinct states mentioned previously allow packing more memory into a single cell, which modifies cycling endurance test procedures.
- **Drift** – This is simply a measure of the drift of the cell's resistance over time, typically performed at various temperatures.
- **Read Disturb** – This is an evaluation of how the "read" procedure impacts the stored state. The measurement pulse must be less than 0.5V. Higher voltages will lead to Read Disturb problems.
- **Resistance-current (RI) curves** – The RI curve (***Figure 2***) is one of the most common parameters collected during PCM characterization. A pulse sequence (***Figure 3***) is sent through a DUT. The first one, a RESET pulse, sets the resistance of the DUT to the high value. It is followed by a DC-read or MEASURE pulse that's usually 0.5V or lower in order to avoid affecting the state of the DUT. This is followed by a SET pulse and another MEASURE pulse. The entire sequence is repeated multiple times, with the amplitude of the SET pulse slowly increased to the value of the RESET pulse. In the RI curve in ***Figure 2***, note the plotted values of the measured resistances after the SET or RESET pulse. These values are plotted against current in the SET pulse. RESET values slightly exceed 1MΩ; SET resistance values range from one mega-ohm to several kilo-ohms, depending on the value of the SET current.

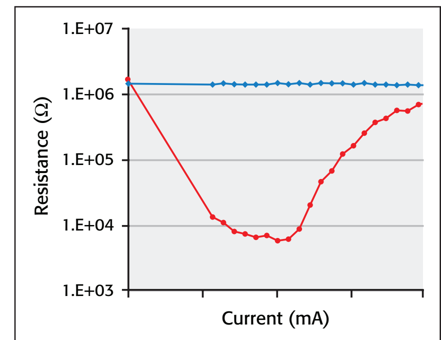

Figure 2. RI curve in red.

- **I-V (current-voltage) curves** – Here, the voltage sent through a DUT previously RESET to its highly resistive state is swept from low to high (***Figure 4***). The dynamic switch from a high- to a low-resistive state in the presence of a load resistor produces a characteristic RI curve with a snapback, an area of negative resistance. Snapback itself is not a feature of PCMs or of PCM testing but rather a side effect of the R-load technique that has long been used to obtain both RI and I-V curves.

In the standard R-Load measurement technique (illustrated in ***Figure 5***), a resistor is connected in series with the DUT, allowing current to be measured across the DUT by measuring the voltage across the load resistor. Active, high impedance probes and

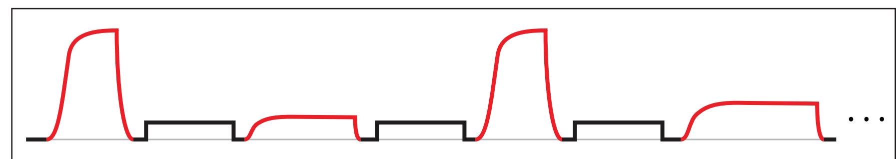

Figure 3. Pulse sequence for creating an RI curve. The tall red curves are RESET pulses. The shorter red pulses are SET pulses. The short rectangular black pulses are the resistance (R) measurements.

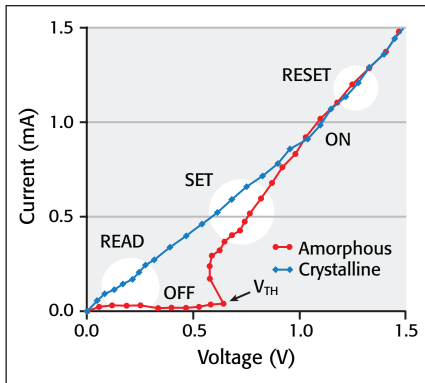

Figure 4. Example of I-V current voltage sweep [3].

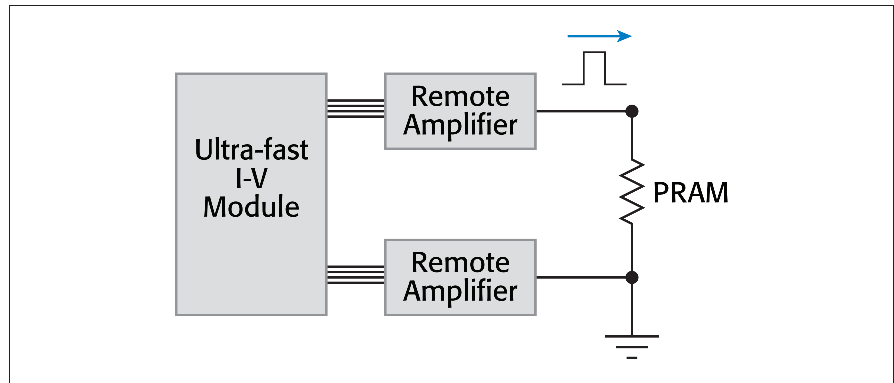

Figure 6. Current-limiting technique employed with Model 4225-PMU.

an oscilloscope are used to record the voltage across the load resistor. Current across the DUT will be equal to the applied voltage ($V_{APPLIED}$) minus the voltage across the device (V_{DEV}), divided by the load resistance. The values of the load resistor usually range from one to three kilo-ohms. This technique involves a tradeoff: if the load resistance is too high, RC effects and the voltage division between the R-Load and the DUT limits this technique's performance; however, if the resistor value is too small, it impacts the current resolution.

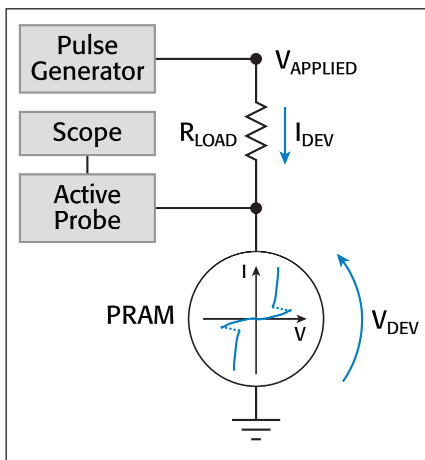

Figure 5. Standard R-Load technique.

Recently, a new current-limiting technique has been developed that eliminates the need for the load resistor. Tight control over the level of current sourced allows for more accurate characterization of low currents in the RI curve. This new technique (***Figure 6***), which allows taking both I-V and RI curves in a single pulse sweep, employs a high-speed pulse source and measure instrument, the dual-channel Model 4225-PMU Ultra-Fast I-V Module. This new module can source voltage and simultaneously measure both voltage and current responses with high accuracy, with rise and fall times as short as 20ns.

The elimination of the load resistor also eliminates the snapback side effect. The Model 4225-PMU and the Model 4225-RPM Remote Amplifier/Switches that extend its sensitivity (***Figure 7***) are designed to integrate with the Model 4200-SCS Semiconductor Characterization System, which not only provides the other measurement functions necessary to characterize a PCM device but offers the ability to automate the entire testing process.

Figure 7. Model 4225-PMU Ultra-Fast I-V Module and two Model 4225-RPM Remote Amplifier/Switches, available for the Keithley Model 4200-SCS characterization system.

Summary

As industry looks for more reliable memory devices, the ability to characterize these new devices quickly and accurately during development becomes increasingly important. New tools and techniques now being developed will be critical to this pursuit. For further details on these new techniques, view the archived online webinar on this topic: http://www.keithley.com/events/semconfs/webseminars. KEITHLEY

References

[1] T. Nirschl, J. B. Phipp, et al. (2007, Dec. 10-12). Write strategies for 2- and 4-bit multi-level phase-change memory. Presented at IEDM 2007. IEEE International. [Online]. Available: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4418973

[2] D.-S. Suh, K. H. P. Kim, et al (2006, Dec. 11-13). Critical quenching speed determining phase of Ge2Sb2Te5 in phase-change memory. Presented at IEDM '06. IEEE International. [Online]. Available: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4154328

[3] A. Pirovano, A. L. Lacaita, et al, "Low-field amorphous state resistance and threshold voltage drift in chalcogenide materials," IEEE Trans. Electron Devices, vol. 51, no. 5, May 2004.

About the Author

Alex Pronin is a lead applications engineer with Keithley Instruments, Inc. in Cleveland, Ohio. He holds an M.S. in Physics from the Moscow Institute of Physics and Technology and a Ph.D. in Material Science from Dartmouth.

Specifications are subject to change without notice.
All Keithley trademarks and trade names are the property of Keithley Instruments, Inc.
All other trademarks and trade names are the property of their respective companies.

KEITHLEY

A GREATER MEASURE OF CONFIDENCE

KEITHLEY INSTRUMENTS, INC. ■ 28775 AURORA ROAD ■ CLEVELAND, OHIO 44139-1891 ■ 440-248-0400 ■ Fax: 440-248-6168 ■ 1-888-KEITHLEY ■ www.keithley.com

BELGIUM
Sint-Pieters-Leeuw
Ph: 02-3630040
Fax: 02-3630064
info@keithley.nl
www.keithley.nl

CHINA
Beijing
Ph: 8610-82255010
Fax: 8610-82255018
china@keithley.com
www.keithley.com.cn

FRANCE
Saint-Aubin
Ph: 01-64532020
Fax: 01-60117726
info@keithley.fr
www.keithley.fr

GERMANY
Germering
Ph: 089-84930740
Fax: 089-84930734
info@keithley.de
www.keithley.de

INDIA
Bangalore
Ph: 080-26771071, -72, -73
Fax: 080-26771076
support_india@keithley.com
www.keithley.com

ITALY
Peschiera Borromeo (Mi)
Ph: 02-5538421
Fax: 02-55384228
info@keithley.it
www.keithley.it

JAPAN
Tokyo
Ph: 81-3-5733-7555
Fax: 81-3-5733-7556
info.jp@keithley.com
www.keithley.jp

KOREA
Seoul
Ph: 82-2-574-7778
Fax: 82-2-574-7838
keithley@keithley.co.kr
www.keithley.co.kr

MALAYSIA
Penang
Ph: 60-4-643-9679
Fax: 60-4-643-3794
koh_william@keithley.com
www.keithley.com

NETHERLANDS
Gorinchem
Ph: 0183-635333
Fax: 0183-630821
info@keithley.nl
www.keithley.nl

SINGAPORE
Singapore
Ph: 65-6747-9077
Fax: 65-6747-2991
koh_william@keithley.com
www.keithley.com

SWITZERLAND
Zürich
Ph: 044-8219444
Fax: 044-8203081
info@keithley.ch
www.keithley.ch

TAIWAN
Hsinchu
Ph: 886-3-572-9077
Fax: 886-3-572-9031
info_tw@keithley.com
www.keithley.com.tw

UNITED KINGDOM
Theale
Ph: 0118-9297500
Fax: 0118-9297519
info@keithley.co.uk
www.keithley.co.uk

© Copyright 2010 Keithley Instruments, Inc.

Printed in the U.S.A. No. 3079 03.28.10