KEITHLEY
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Number 3047

Methods to Achieve Higher Currents from I-V Measurement Equipment

The most flexible test equipment for sourcing and measuring current (I) and voltage (V) are source-measure units (SMUs) such as Keithley's Series 2600B System SourceMeter® instruments. The Series 2600B also includes three new benchtop models that offer best-in-class value and performance. These specialized instruments are high performance I-V source-measure instruments that are designed for use either as bench-top I-V characterization tools or as building block components of multi-channel I-V test systems. Each Series 2600B SourceMeter instrument combines a precision power supply, a true current source, a DMM, an arbitrary waveform generator with measurement, an electronic load, and a trigger controller – all in one instrument. In short, they can source I or V, and then measure V or I, simultaneously. They also support both polarities of I and V (sinking and sourcing power), referred to as "four quadrant operation."

By design, there is a limit to the maximum current or voltage that a single SMU can source and measure. This paper will present methods to achieve current levels during test sequencing that are higher than the published DC (direct current) specifications of a single SMU. Two techniques will be explored:

1. Pulse sweeps
2. Combining multiple SMU channels together

These techniques can be used to source and measure currents up to 40A for high-power applications such as:

- Solar cells and other photovoltaics
- Power management devices such as power MOSFETs and IGBTs
- High brightness light emitting diodes
- RF power transistors

Pulse sweeps

There is a limit to the DC maximum current or voltage that a single SMU can source and measure. This limit is a function of the inherent equipment design and is typically dependent on design parameters such as the maximum output of the power supply internal to the SMU itself, the safe operating area (SOA) of the discrete components used in the SMU, the spacing of the metal lines on the SMU's internal printed circuit board, etc. Some of these design parameters are constrained by maximum current limits, some by maximum voltage limits, and some by maximum power limits (I×V). A typical expression of the DC I-V limits of a four quadrant SMU is shown in ***Figure 1***. It shows a maximum DC current of 3A (point A in the figure) and a maximum voltage of 40V (point B). The maximum power the SMU can output is 40W, which is achieved at point B (1A×40V). At point A the power is lower at 18W. The difference can be explained, for example, that the maximum at point B is constrained by the maximum allowed power output of the on-board power supply, whereas at point A the limit is based on the maximum current (not power) that a key component can handle.

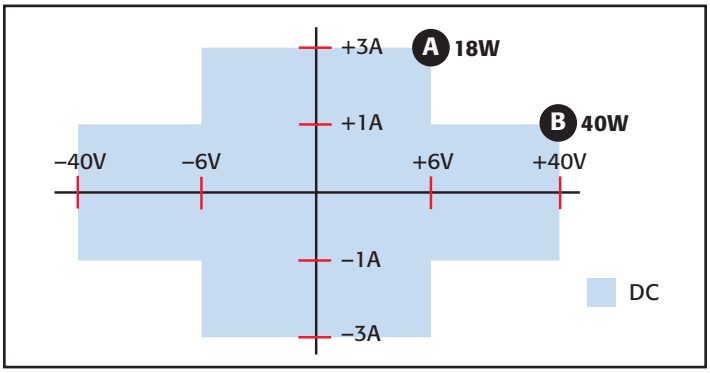


Figure 1

Figure 1 shows the DC (or continuous wave, CW) I-V limits, or performance envelope. Now consider if the SMU could produce a time-varying waveform such as a pulse. If the pulse waveform had 40V amplitude, 1ms pulse width, and a 50% duty cycle, then the effective CW power averaged over several seconds is 20W, not 40W. Depending on its design, it may be possible for that SMU to source higher current in pulse mode than in DC mode – the instantaneous maximum peak power in pulse mode is higher than DC peak power, but the CW power dissipation during pulse mode is less on average than in DC mode.

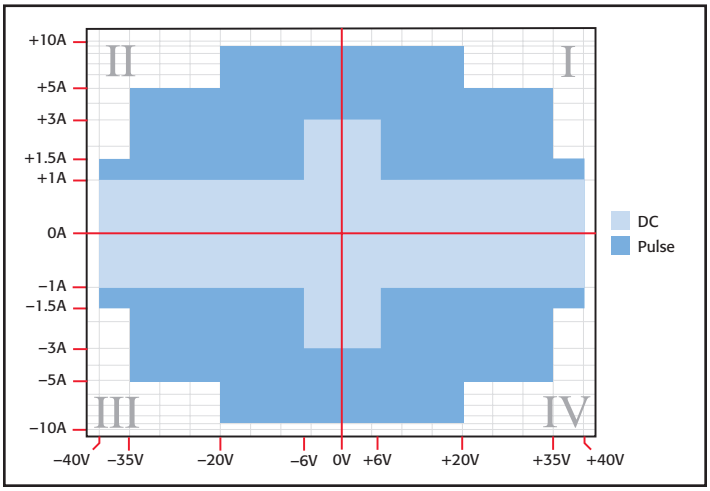


Figure 2

As an example, the pulsed I-V envelope is shown in ***Figure 2*** for the same SMU model shown in ***Figure 1***. There are constraints on the allowed pulse width and duty cycle, but by pulsing the instantaneous power can be as high as 200W (10A×20V). Although the instantaneous power may be high, the CW power based on allowed pulse width and duty cycle is below the DC power limit of 40W.

The higher instantaneous power when pulsing can be applied to achieve higher power I-V sweeps. Consider a standard scenario where a voltage bias is applied to a DUT (Device Under Test). The voltage values are swept over time, from low voltage to high voltage. Intermittently, the current is measured (schematic shown in ***Figure 3***). This generates I-V pairs that, when plotted, give a typical I-V sweep such as that shown in ***Figure 4*** for a P-N junction diode (1N5400 component). P-N diodes are encountered when measuring a solar cell or other photovoltaic (PV) device, or high-brightness light emitting diodes (HB-LEDs). In this sweep, voltage increments of 0.02V were used during the sweep. As shown in ***Figure 2***, when the applied voltage is less than 6V, that particular SMU's maximum allowed DC current is 3A, as demonstrated in ***Figure 4***.

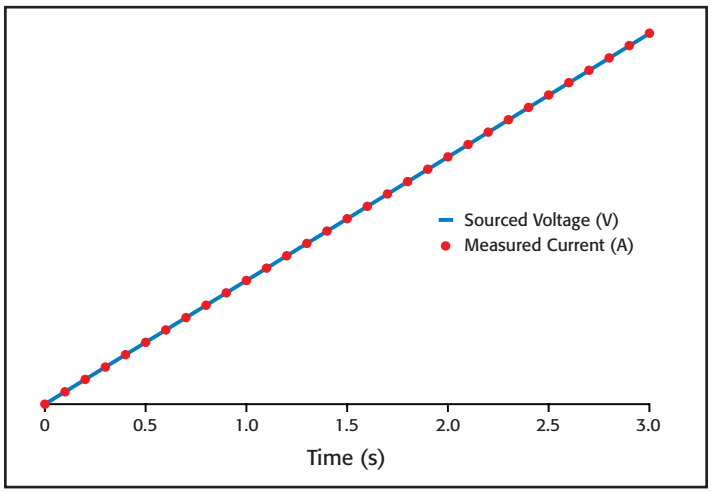


Figure 3

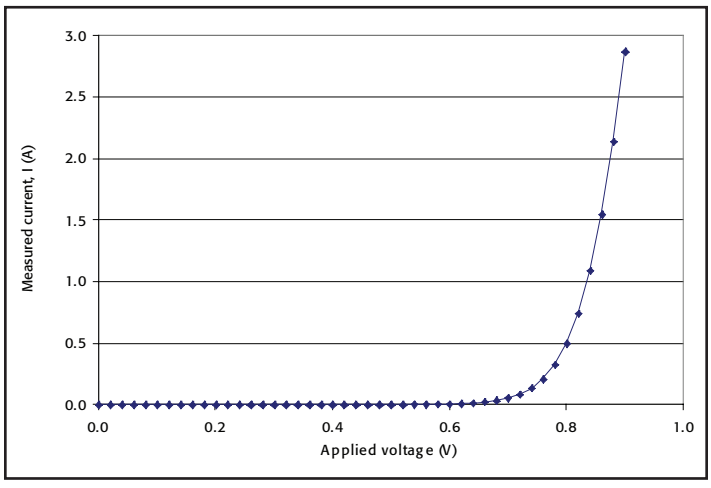


Figure 4

The schematic for a pulsed voltage sweep is shown in ***Figure 5***, which is equivalent to the DC sweep shown in ***Figure 3***. When current is not being measured, the sourced voltage values simply return to zero to keep the averaged CW power within the allowed limits. As seen in ***Figure 5***, the V bias values at which the I values are measured and the I sampling rates are identical to those in the DC sweep shown in ***Figure 3***. Performing pulse sweeps in this manner allows identical I-V values as DC to be achieved in the lower power regions (***Figure 6***), while allowing I-V curves in the higher power region up to 10A to be achieved ***(Figure 7***).

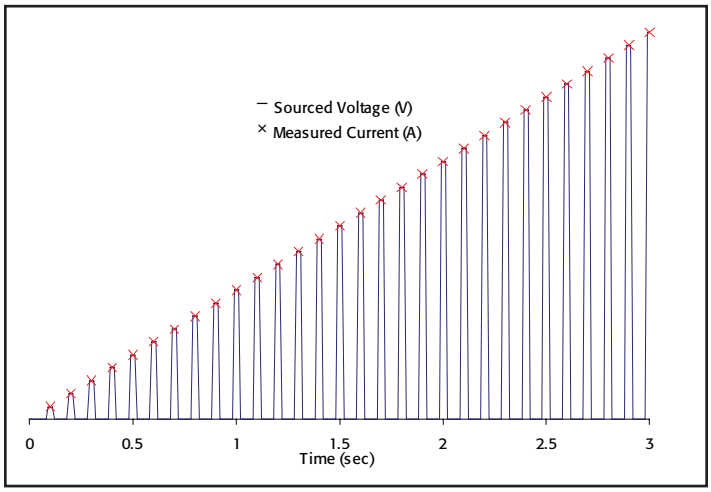


Figure 5

In ***Figure 6***, the DC and pulse sweep I-V curves are so closely overlaid that it is difficult to visually discern the differences between the curves. Therefore to quantify the excellent correlation, the relative percent difference between the curves is also calculated and shown in ***Figure 6***. At the higher current values of most interest, ±2% correlation is achieved between the DC and pulse sweeps (using the DC sweep values as the reference). With excellent correlation established at the lower current levels, we then use pulse sweeps to extend the I-V curves to 3× higher currents of 10A maximum than could be achieved with DC sweeps. This is shown in ***Figure 7***.

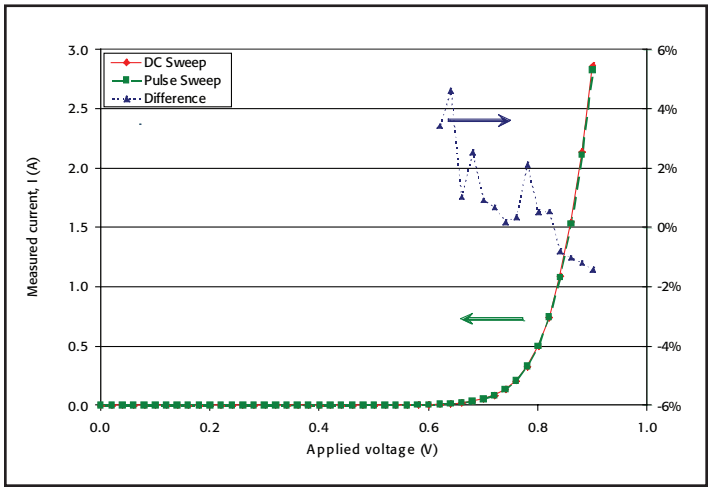


Figure 6

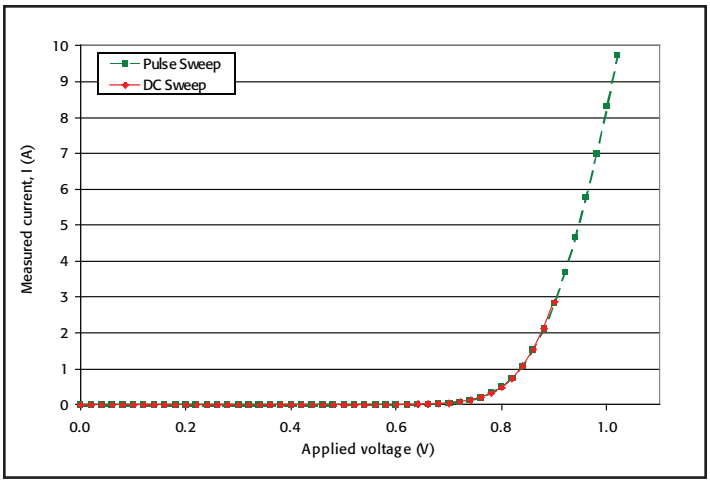


Figure 7

For many DUT types, a pulsed sweep can be substituted for a DC sweep to achieve higher power I-V sweeps with little impact on results. DUT types for which pulsed sweeps may not adequately correlate to DC sweeps are those DUTs potentially impacted by displacement current (second term in Maxwell's equation for current, $J_{tot} = J + \partial D/\partial t$). Large displacement currents can be generated at the sharp edges of the voltage pulse, and DUTs such as capacitors can have their electrical properties changed by large displacement currents.

However, there are many high power devices where pulsed I-V testing ***must*** be performed to get optimal results. The reason is that during high power CW testing, the semiconductor material itself starts to dissipate the applied power via thermal heating. As the material in the device heats up, the conduction current decreases as the carriers have more collisions with the vibrating lattice (phonon scattering). Therefore, the measured current is erroneously too low, due to so-called self-heating effects (http://www.keithley.com/data?asset=50742) caused by Joule heating. Because devices such as these are typically run in pulsed mode, intermittently, or AC and not run continuously on, the erroneously-low DC-measured currents are not an accurate characterization of their performance. In this case, pulsed testing must be used, and pulse width and duty cycle are explicitly stated in the device's published datasheet (see for example the inset in Figure 2 at http://www.fairchildsemi.com/ds/1N%2F1N5400.pdf). Example devices that require pulse testing are high-power RF power amplifiers and even low-power nanoscale devices.

The primary tradeoffs when migrating from a DC sweep to a pulse sweep are as follows:

- The pulse width must be wide enough to allow time for the device transients, cabling and other interfacing circuitry to settle so a stable, repeatable measurement can be made.
- The pulse width cannot be so wide so as to violate the test instruments' maximum pulse width and duty cycle limits, which would exceed the allowed power duty cycle of the instrument.

Combining multiple SMU channels to achieve higher DC current

The most commonly-used method of combining SMU channels to achieve higher DC currents is to put the current sources in parallel across the DUT, as shown in ***Figure 8***.

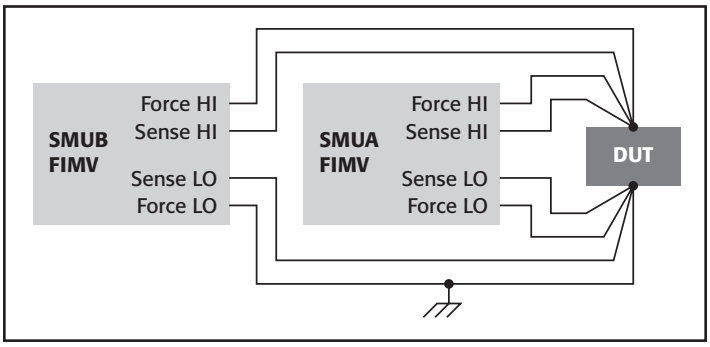


Figure 8

This test setup takes advantage of the well-known electrical principal that two current sources connected to the same circuit node in parallel will have their currents added together (Kirchhoff's current law). In ***Figure 8***, both SMUs are sourcing current and measuring voltage. The HI terminals refer to the high impedance terminals of the SMU and the LO terminals are the low impedance terminals. The "FORCE" terminals are the ones forcing current, and the SENSE lines are used for the four-wire voltage measurements. four-wire configuration is a mandatory requirement when high values of current are involved and is discussed later in this document. All of the LO terminal (FORCE and SENSE) of both SMUs are tied to earth ground.

Characteristics of this particular configuration are:

- Source Current:
  $I_{DUT} = I_{SMU\ A} + I_{SMU\ B}$
- Load Voltage:
  $V_{DUT} = V_{SMU\ A} = V_{SMU\ B}$
- Maximum Source Current:
  $I_{MAX} = I_{MAX\ SMU\ A} + I_{MAX\ SMU\ B}$
- Maximum Voltage: Limited to the smaller of the two SMUs maximum voltage capabilities. This is a result of very small variations between units of the maximum voltage that can be output when sourcing current. V_{MAX} = Smaller of $V_{MAX\ CMPL\ SMU\ A}$ and $V_{MAX\ CMPL\ SMU\ B}$.

Other notes:

- Set SMU A and SMU B output currents to the same polarities to obtain maximum output.
  - – While not absolutely required, the source polarity is generally the same for the two SMUs in this configuration.
- When possible, have one SMU in a fixed source configuration at a time and the other SMU performing the sweep. This is preferable to having both sweeping simulataneously. If both SMUs are sweeping, their output impedances are naturally changing, for example, as the meter autoranges. In

addition, the DUT's output impedance may also be changing significantly, for example, from high resistance off state to low resistance on state. With so many of the impedance elements in the circuit changing, this could increase overall circuit settling time at each bias point. Although this is a transient effect that damps out, nonetheless, fixing one SMU's source and sweeping the other usually results in more stable and faster-settling transient measurements, therefore higher test throughput.

- One ramification of having one SMU's current fixed and the others sweeping current is that for current levels well below I_{MAX}, one SMU will be sourcing or sinking much more current than the other. The current levels are not balanced between the two SMUs, but this does not cause any accuracy or precision issues when done with high quality SMUs. There is no particular reason to try to keep the SMUs at approximately the same current throughout the sweep.
- Therefore, to sweep from 0A to I_{MAX}, set both SMUs to source 0A and then sweep SMU B from 0A to $+I_{MAX\ SMU\ B}$. Next sweep SMU A from 0A to $+I_{MAX\ SMU\ A}$. Similar approaches can be used to sweep from I_{MAX} to 0A, or 0A to $-I_{MAX}$, or $-I_{MAX}$ to 0A.
- To sweep from $-I_{MAX}$ to $+I_{MAX}$, first set SMU A to $-I_{MAX\ SMU\ A}$ and SMU B to $-I_{MAX\ SMU\ B}$. Sweep SMU B from $-I_{MAX\ SMU\ B}$ to $+I_{MAX\ SMU\ B}$ and then sweep SMU A from $-I_{MAX\ SMU\ A}$ to $+I_{MAX\ SMU\ A}$. Again, there is no particular reason to try to keep the SMUs at approximately the same current. A similar approach can be used to sweep from $+I_{MAX}$ to $-I_{MAX}$.

- Both SMUs are sourcing current, but only let one SMU limit the maximum output voltage via the compliance setting. For example, set the I-source voltage compliance of SMU B greater than the compliance of SMU A, i.e. $V_{LIMIT\ SMU\ B} > V_{LIMIT\ SMU\ A}$.
  - If the DUT is an active source, the compliance setting of SMU A must be greater than the maximum voltage the DUT can source, to avoid putting the circuit and SMUs into an unknown state. For example, if the DUT is a 9V battery but SMU A's compliance is set to 5V, the results will be unpredictable and unstable.
  - Set the voltage readback measurement range of SMU B equal to its compliance range. There is no special requirement for SMU A's measurement range, but be aware of range compliance if the measurement range is less than compliance range and the instrument allows differences between real compliance and range compliance (such as Keithley Model 24xx and 6430).

Now we apply this technique of combining SMUs in parallel using the SMU models whose DC I-V power envelope are shown in ***Figure 2***. The same P-N diode DUT is used whose results are shown in ***Figure 4*** for a single SMU. By combining two SMUs in parallel, we expect to be able to double the maximum DC current measured from 3A to 6A.

This is confirmed by the results shown in ***Figure 9***. Up to 3A, the single-SMU and dual-SMU results are so closely correlated that is difficult to visually discern any differences between the results. As before, the relative percent difference between the results is calculated and plotted in the figure and, in most cases, shows ±1% correlation is achieved between the single-SMU and dual-SMU sweeps (using the single-SMU sweep values as the reference). With excellent correlation established at the lower current levels, we then use dual-SMU sweeps to extend the I-V curves to 2× higher currents of 6A maximum than could be achieved with single-SMU sweeps.

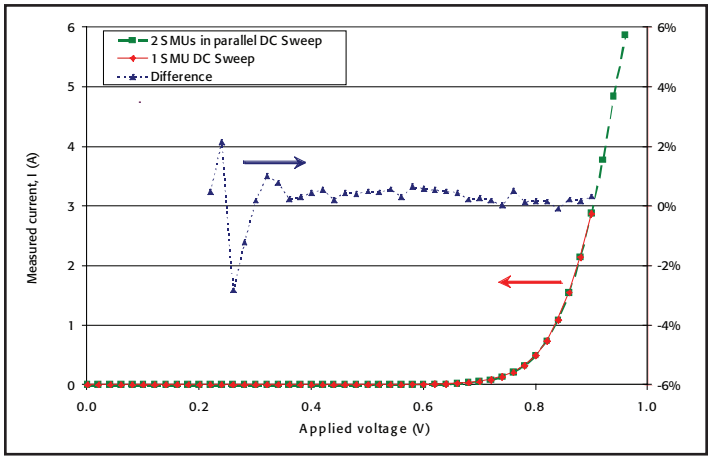


Figure 9

Pulse sweeps while combining multiple SMU channels

In this section we combine power-enhancement techniques of the Pulse Sweep method with the method of combining multiple SMU channels in parallel. Furthermore, we increase the number of SMU channels from two to four by using two dual channel SMUs such as the Keithley Model 2602B. As seen in ***Figure 2***, this SMU can achieve a maximum 10A pulse for DUT bias less than 20V. Therefore the maximum current now achievable is 40A (4×10A), which is more than 13× higher than the 3A that can be achieved by using a single SMU with DC sweeps.

Not surprisingly, great care must be taken when implementing this testing method. First, there is a personnel safety aspect: When dealing with hazardous voltages, it is critical to insulate or install barriers to prevent user contact with live circuits. Failure to exercise these precautions could result in electric shock or death.

There is also an aspect related to avoiding damage to the measurement equipment or the DUT. The multiple pulses must be tightly synchronized in time (on the nsec scale) so that one piece of equipment is not applying power and damaging units that are not turned on yet. Most SMUs on the market simply do not have the capability to synchronize on sufficiently short time scales and therefore are not suitable for implementing this type of test methodology; however, the Keithley Series 2600B SMUs have been intrinsically designed to do this. There are

other important considerations when using more than two SMUs together, which will be discussed in the next section.

To set a baseline before combining SMUs, we perform a 10A pulse using a single SMU and observe the results on an oscilloscope. A high power precision resistor (0.01Ω, ±025%, KRL R-3274) was used as the test DUT and a pulse width of 300μs was programmed. We expect the oscilloscope to show a nearly square waveform of amplitude 0.1V (10A × 0.01Ω) and 300μs width, and, in fact, those are the results we see in ***Figure 10***. As also shown in ***Figure 10***, combining four SMUs in parallel to pulse 40A across the same DUT results in the expected 0.4V magnitude with excellent synchronization (low jitter) between the channels.

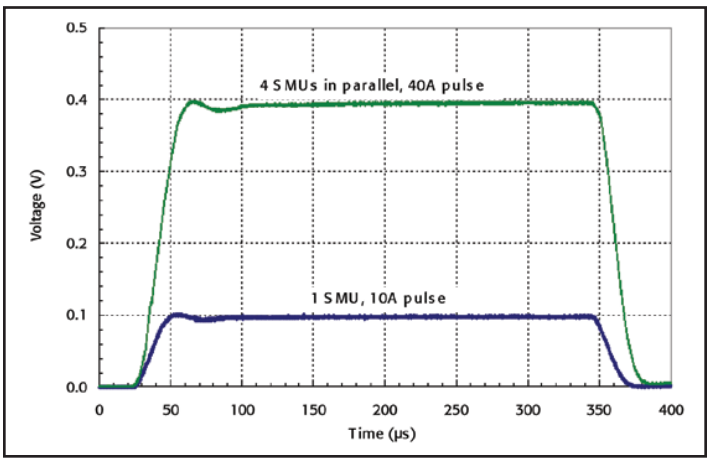


Figure 10

Using the pulse waveform shown in ***Figure 10*** (40A amplitude, 300μs width, generating 0.4V across a 0.01Ω ±0.25% resistor), repeatability testing was done to verify pulse consistency. This is a particularly stringent test that simultaneously checks both the high I sourcing performance along with low V measurement performance. The results are shown in ***Figure 11***, with a 3σ standard deviation of 0.045% observed across 25 repetitions done in quick succession.

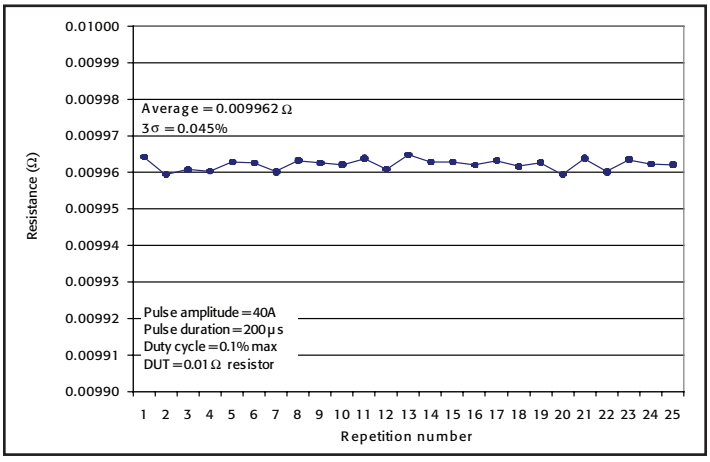


Figure 11

With the pulse performance verified, we program a pulse sweep combining four SMUs and repeat the I-V curve on the P-N diode test DUT. The results are shown in ***Figure 12***. We see excellent correlation with the 1-SMU DC sweeps up to 3A, and with the 1-SMU pulse sweep up to 10A. Then, we extend the achievable I-V curve up to 40A.

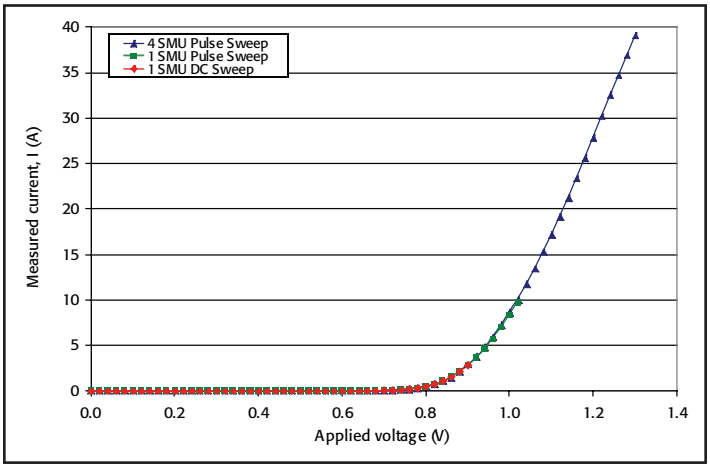


Figure 12

With the results of this technique (combining four SMU channels and pulsing to achieve 40A) verified on two-terminal devices (resistor and diode), the technique is next applied to a three-terminal device, a high-power MOSFET (IRFP240, datasheet available at www.datasheetcatalog.org/datasheet/fairchild/IRFP240.pdf). Such devices have high operating drain current $I_{D(ON)}$ (>20A at V_{DS}>20V, V_{GS}>10V), and low drain-source on resistance $r_{DS(ON)}$ (<0.2Ω at V_{GS}=10V, I_D=10A). Typical electrical parameters that are measured on such a device include:

- I_D–V_{DS} curves for a variety of V_{GS} values
- $r_{DS(ON)}$–I_D curves for different V_{GS} values
- Threshold voltage (gate to source), $V_{GS(TH)}$
- Drain-to-source breakdown voltage, BV_{DSS}
- Continuous source-to-drain current and voltage, I_{SD} and V_{SD}

For the three-terminal measurements, four SMUs are connected in parallel across the drain-source nodes to enable 40A pulsed currents; a fifth SMU is connected across the gate-source nodes to provide the gate bias.

The I_D–V_{DS} curves for a variety of V_{GS} values are shown in ***Figure 13***. The measurements and curves are the expected results, with the effects of minor device self-heating observed at around V_{DS}=10V for the V_{GS}=7V and V_{GS}=8V curves. Self-heating is expected for the pulse width of 1000μs that was used. Note that nearly 800W peak power (20V × 40A) is achieved with this tests setup.

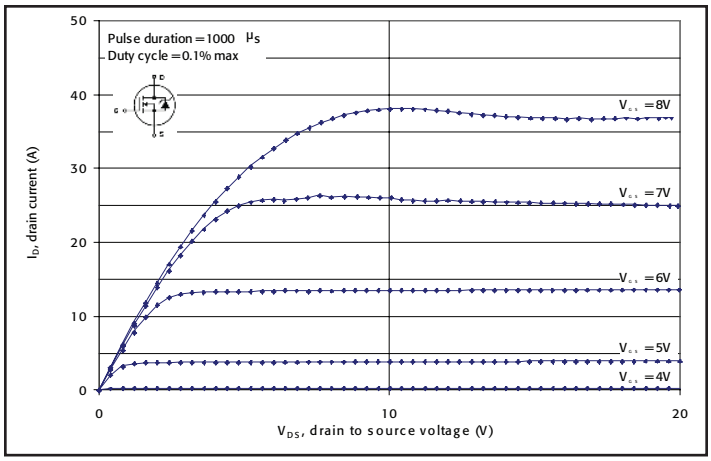


Figure 13

The $r_{DS(ON)}$–I_D curve was measured for V_{GS}=10V up to the maximum measurable drain current of I_D=40A. The results are shown in ***Figure 14***, and, for comparison purposes, the data from the device's published datasheet (Figure 8 in www.datasheetcatalog.org/datasheet/fairchild/IRFP240.pdf) are also shown. The correlation is excellent when using this multiple-SMU technique combined with pulse sweeping. With the standard, single-SMU DC sweep, the curve would have ended at 3A, which is not sufficient to properly characterize the device.

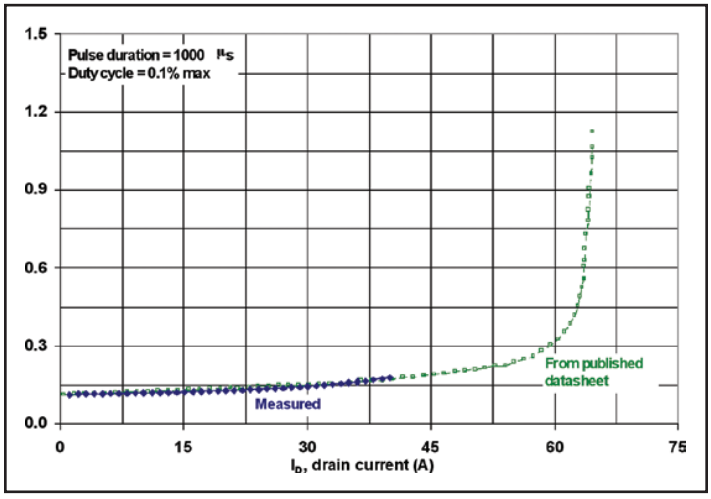


Figure 14

Finally, the I_{SD}–V_{SD} curves for V_{GS}=0V are shown in ***Figure 15***. These are compared to the results from the device's published datasheet (Figure 13 in www.datasheetcatalog.org/datasheet/fairchild/IRFP240.pdf), and, again, correlation is very good.

With a modern smart SMU like the Keithley Series 2600B, which has its own microprocessor, onboard memory, and math and logic programming functions via an embedded open-source scripting language, it is easy to run the SMU via a graphical user-interface for benchtop applications, or have the scripts resident on the SMU with no need for a control PC for high-speed parallel test production applications. Also, because the Keithley Series

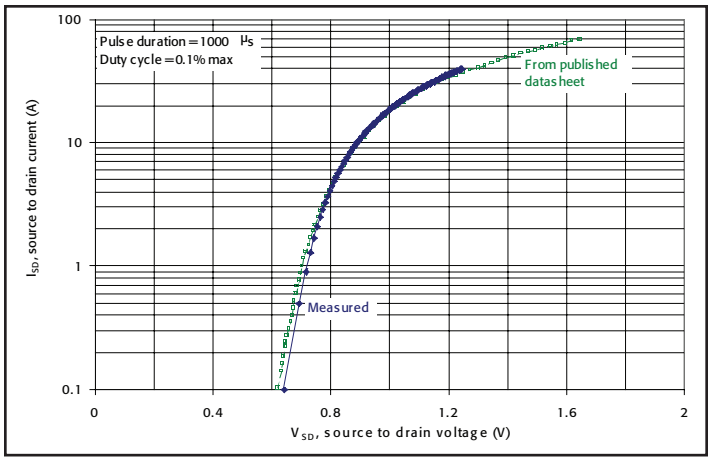


Figure 15

2600B SMUs are mainframeless, the exact number of channels can be expanded to the desired number without having to incur the additional cost or power limitations of a mainframe.

Important test implementation details

This section describes key implementation details that significantly improve the accuracy and precision of the results obtained using this multi-SMU pulsed sweep approach.

Source readback

Consider the case when a test applies a voltage to a DUT and measures a current. Because an SMU has both source and measure functions built into the same unit, it can also read back the actual value of the applied voltage using its measurement circuitry. This is a source-measure-measure sequence not just source-measure: Source voltage, measure (readback) applied voltage, measure resulting current across the device. A typical reason why the programmed value for the source voltage is not the same as the voltage applied to the DUT is that the DUT is sinking a large current, which slightly loads the voltage source. In that case, the actual measured voltage values that are read back are typically slightly lower than the values that were programmed. A comparison was done for the P-N diode DUT used previously, and the results are shown in ***Figure 16***. At the maximum point of the I-V (current about 40A), the programmed voltage is 1.3000V and the actual measured sourced value is 1.2917V, a small 0.64% error, which may or may not be impactful depending on the actual application. The error manifests itself primarily as a small offset on the voltage axis (left-right shift on the X-axis in ***Figure 16***) with little impact to the measured current values (little shift on the Y-axis).

Four-wire measurements

Four-wire (Kelvin) measurements must be used when doing high current testing. A four-wire measurement bypasses the voltage drop in the test leads by bringing two very high impedance voltage sense leads out to the DUT. With very little current flowing into the SENSE leads, the voltage seen by the SENSE

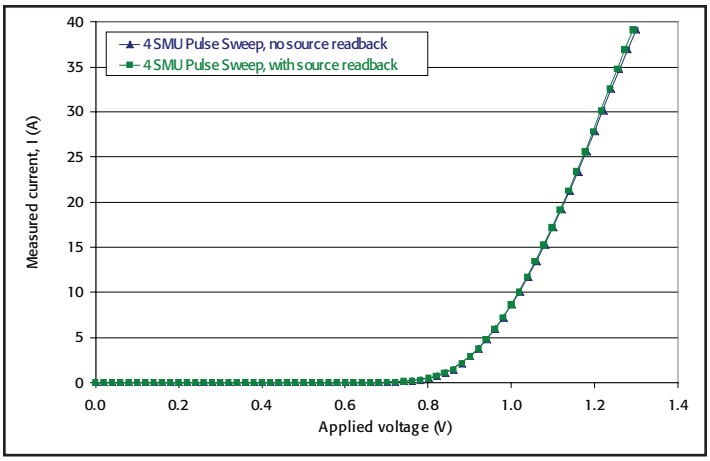


Figure 16

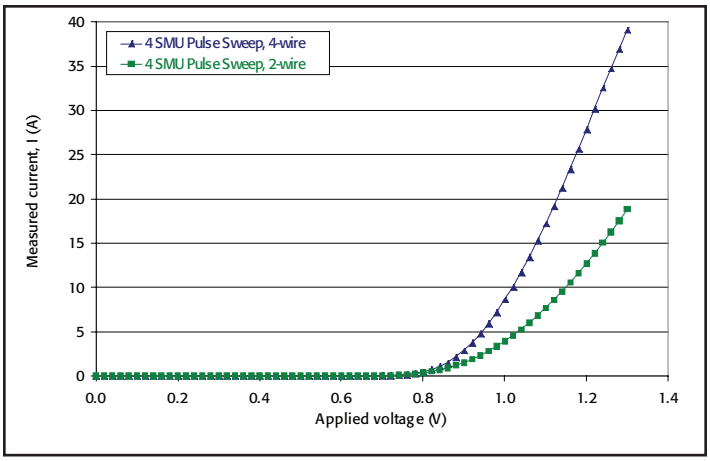


Figure 17

terminals is the virtually same as the voltage developed across the unknown resistance.

This is very important when high currents are being tested. At 40A levels, even a small resistance such as 10mΩ in the test cable can generate a voltage drop of 0.4V. So if the SMU is forcing 1V at 40A current and the cable resistance is 10mΩ and there are two test leads, the DUT might only receive a voltage of 0.2V, with 0.8V dropped across the test cables. A more detailed discussion of four-wire measurements can be found at http://www.keithley.com/data?asset=10636.

Unlike source readback, which primarily impacted just the source values, implementing four-wire measurements will result in significantly more accuracy on both the sourced and measured values. That is because most good-quality modern SMUs have an analog feedback control loop; in other words, if it is programmed to source, say, 1V, but the measured value at the DUT using four-wire is only 0.2V, then the SMU will increase the current it sources to compensate for the loads and voltage drops in the circuit, until the four-wire voltage value reaches the programmed source value (within the loop exit limits). The DUT's bias will be closer to the desired value; hence, the measured value will be more accurate. Therefore, by enabling four-wire measurement capability, both the sourced values and the measured values will be more accurate (impacts both axes in an I-V curve).

The results of two-wire versus the more accurate four-wire results are shown in ***Figure 17*** for the P-N diode used previously. As seen in that figure, due to the voltage drops in the test leads, in two-wire mode the DUT sees only a small fraction of the intended applied voltage, and, therefore, the forward current is lower. At 1.3V bias in 2-wire mode (bearing in mind that the DUT will get less voltage around 1.1V due to uncompensated voltage drops from the resistance in the test leads), the measured current is less than 20A, half of the real value (40A) when four-wire mode is used. This is a significant error, justifying the benefit of four-wire full Kelvin (not quasi-Kelvin) testing.

Of course, to achieve best results, every effort must be made to place the test leads for the four-wire Kelvin connection as close to the DUT as is possible.

Maximum of one voltage source at each DUT node

It is common in many test sequences to perform voltage sweeps (force voltage) and measure current (FVMI). In the case of more than one SMU connected in parallel to a single terminal of the device, the obvious implementation would be to have all of the SMUs in V-source mode and measure I. However, three factors must be considered:

- SMUs when sourcing voltage are in a very low-impedance state.
- DUTs can have impedances higher than an SMU that's in V-source mode. The DUT's impedance can be static or dynamic, changing during the test sequence.
- Even when all SMUs in parallel are programmed to output the same voltage, small variations between SMUs related to the instruments' voltage source accuracy means that one of the SMU channels will be at a slightly lower voltage (mV order of magnitude) than the others.

So, if three SMUs are connected in parallel to one terminal of a DUT, and each SMU is forcing voltage and outputting near-maximum currents, and the DUT is in a high impedance state, then all current will go to the SMU which is sourcing the slightly lower voltage. This will most likely damage that SMU. Therefore, when connecting SMUs in parallel to a single terminal of a DUT, only one SMU should be sourcing V, as shown, for example, in ***Figure 18*** for the multiple SMUs connected to the drain of the MOSFET whose results were shown in ***Figures 13–15***.

Even if the configuration in ***Figure 18*** is used, extreme care must be taken so that throughout the sweep only one SMU is in FVMI mode and that none of the SMUs in FIMV mode automatically or inadvertently change to FVMI mode. An SMU can change from FIMV to FVMI mode, for example, when an SMU in FIMV mode reaches its programmed voltage level for source compliance. When an SMU is sourcing current to a programmed level in FIMV mode and the DUT sinks current, the SMU will automatically increase its output voltage via an analog feedback loop so as to maintain the programmed output current. The maximum voltage it will use is set by the user via a source compliance voltage level. When an SMU is in FIMV mode and source voltage compliance is reached, the SMU switches modes

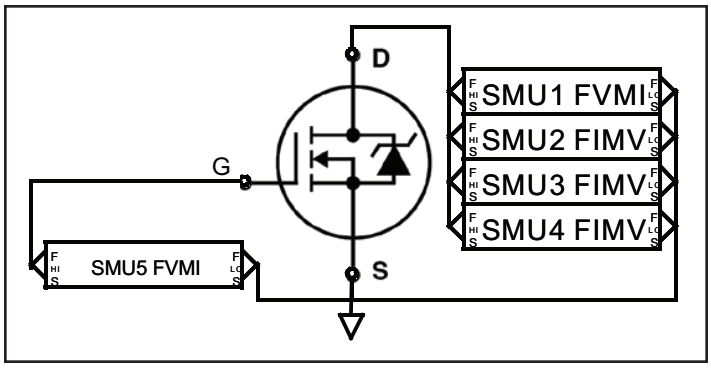


Figure 18

and becomes a low-impedance voltage source and is at risk to being damaged. To prevent that from happening:

- Voltage compliance levels should be set appropriately (typically as high as possible)
- Control code can be written to monitor results during the sweep and take corrective action to avoid compliance as the instrument approaches compliance levels.

One practical implementation of a maximum of 1V-source at each DUT node is to have no SMUs in V-source, all in I-source. The sweep then would be entirely I-bias (not V-bias). While this is easiest to implement, this method suffers from the fact that I-V data will not be equally spaced on the voltage axis; they will be equally spaced on the current axis. This might complicate or confuse some standard analysis algorithms. A demonstration of this is shown in ***Figure 19***, where all SMUs are FIMV and none are V-source. These results should be compared to ***Figure 13***, where one SMU is in V-source mode and, therefore, the data points are equally spaced in voltage.

The method shown in ***Figure 18*** works on the basis that one SMU controls the output voltage while the rest of the SMUs supplement the current. To do this, one SMU is configured as a V source while the rest are configured as current sources for the entire sweep. The SMUs supplying current are supplying it at the level measured by all SMUs at the previous bias point.

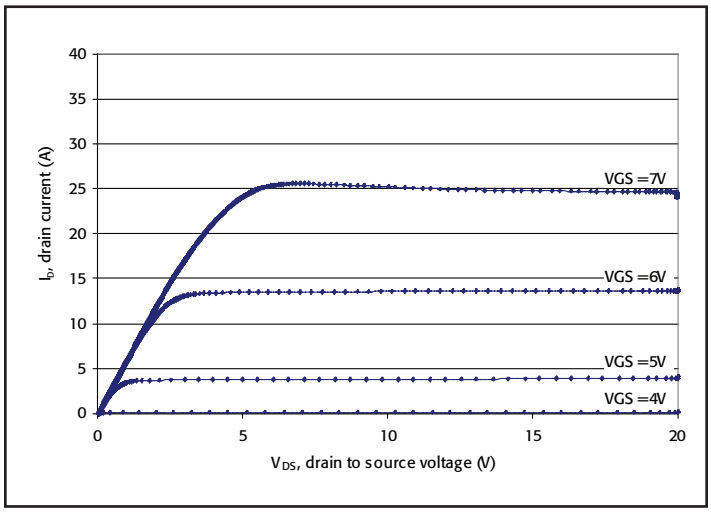


Figure 19

So in the case of four SMUs for the results shown in ***Figures 12–17***:

- Put SMU1 in V-source mode; SMU2, SMU3, SMU4 in I-source mode
- Determine V_{step}
- Initially SMU1 sources 0V (or a voltage level that will result in a DUT current that is less than the maximum current that SMU1 can handle on its own). SMU2–4 source 0A.
- Sweep loop:
  - All 4 SMUs measure I.
  - Calculate Itotal = $I_{SMU1} + I_{SMU2} + I_{SMU3} + I_{SMU4}$
  - $I_{bias} = I_{total}/3$
  - Set SMU1 to source voltage at the level of the previous voltage plus V_{step}
  - Set SMU2, SMU3, SMU4 to source current each at a level of I_{bias}
  - Repeat loop until exit condition is reached

Mitigating excessive energy dissipation due to device breakdown

When two SMUs of the same capability are connected in parallel to a single node in the circuit, one SMU is always capable of sinking all of the current being output by the other SMU. This scenario can occur, for example, when a DUT breaks down, becomes an open (near-infinite impedance), and is no longer a continuity path where current can flow. There is a short time during which 1 SMU has to sink all the current from the other.

However, when there are more than 2 SMUs connected in parallel at a single circuit node, 1 SMU cannot sink all of the current coming from the other SMUs. The SMU(s) that will be forced to sink current if the DUT breaks down are the SMUs at the lowest voltage or lowest impedance, most likely the ones sourcing voltage. In order to protect the signal input of the SMU forcing voltage, a diode such as the 1N5820 can be used. This limits the amount of current that can go into the SMU. A diode is preferable, because a fuse is too slow, and a resistor will cause too large of a voltage drop a across it. A diode has a much faster response than a fuse, and the diode has a much smaller maximum voltage drop across it (typically around 1V) than a resistor.

Adding diode protection to the test setup previously shown in ***Figure 18*** results in the circuit schematic shown in ***Figure 20***. Although SMU5 is also in FVMI mode, it does not require input protection because its Force-HI connection is connected to the high-impedance gate node. Also, in the test setup shown in ***Figure 20***, extra test code has been implemented to ensure that SMUs 2–4 will not reach compliance during the test sequence, to ensure they don't switch to FVMI mode. If this extra test code is not used, hardware protection should be added to the inputs of SMUs 2–4 in case any of them reach source voltage compliance.

To demonstrate little impact on results of adding diode protection to SMU1, we repeat the $r_{DS(ON)}$–I_D curve measured on

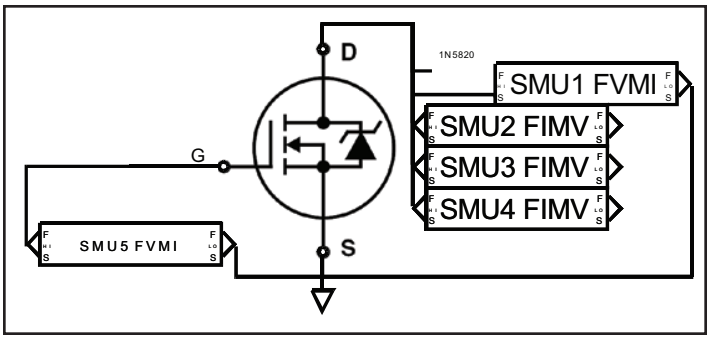


Figure 20

the IRFP240 part for V_{GS}=10V up to the maximum measurable drain current of I_D=40A (results previously shown in ***Figure 14***), both with and without diode protection. The results are shown in ***Figure 21***. The results overlay so well they are almost indistinguishable, and, upon calculating the relative percent difference between the two curves and plotting, in most cases, shows ±1% correlation is achieved between the no-diode and diode cases. This confirms that diode protection can and should be used.

It is also important to ground the LO terminals of both SourceMeter units, as shown in ***Figures 8***, ***18***, and ***19***. If the DUT becomes grounded and the steps above are not followed carefully, the SMUs could be damaged.

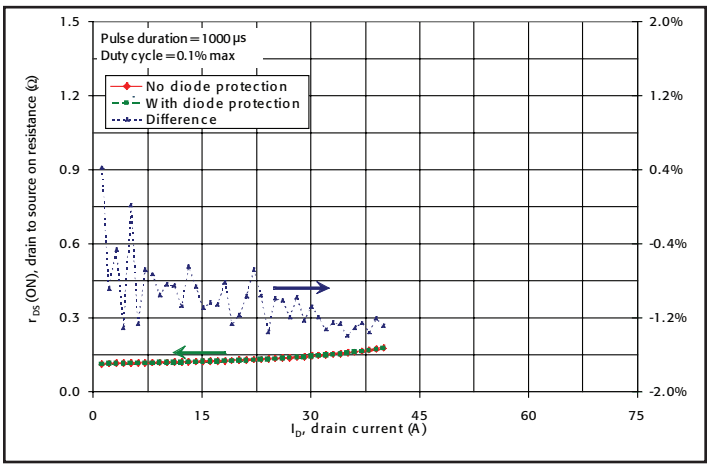


Figure 21

Cabling and test fixture considerations

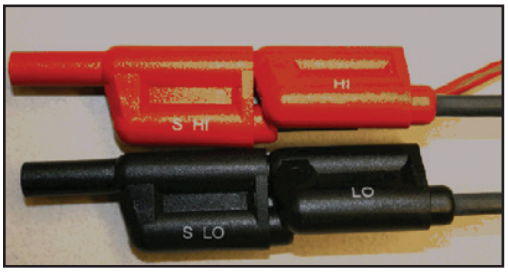
In general, test cabling and test connections must all be designed to minimize resistance (R), capacitance (C), and inductance (L), between the DUT and SMU.

To minimize resistance, use thick gauge wire (14 gauge is acceptable, 12 gauge is better) wherever possible, and definitely within the test fixture itself. Cable resistance can range from 30-300 mΩ/meter and higher, so obviously choose cabling at the lower end of that range. Keep cable lengths a short as possible and in no case longer than one meter.

Cables used in this document were Keithley Model 2600B-BAN: 1m (3.3 ft) banana test leads/adapter cable, which provide safety banana connections to Hi, Sense Hi, Lo, Sense Lo, and guard. The test leads were connected to the DUTs using alligator clips with boots (barrels accept standard banana plugs), such as those in Keithley Model 5804 Test Lead Set.

It is generally thought that guarding can minimize the effects of cable charging, but this is typically more of a concern for high voltage testing and not for high current testing. Guarding was not used in the results shown in this paper.

Four-wire Kelvin connections must be as close to the DUT as possible (every mm matters). So if using banana test leads and "piggybacking" the jacks, the Sense leads should be in front of the Force leads, as shown in the photo below. Putting the Sense leads behind the Force leads will degrade the results. While "piggybacking" is acceptable for the SMUs forcing current, the SMU forcing voltage must have its sense leads separated and right at the DUT (for example using alligator clips) in order to have proper 4-wire operation. Also, it should be noted that the voltage readback should be done with the SMU forcing voltage, because the current SMU's voltage readings will all vary quite a bit due to the connections, and will be different then what is actually at the DUT.



The jacks used on the test fixture should be high quality. In particular, some red jacks use high amounts of ferrous (Fe, iron) content to produce the red coloring, and these jacks can have unacceptably high levels of leakage due to conduction. The resistance between the plugs to the case should be as high as possible and in all cases $>10^{10}\Omega$.

Many published test setups recommend to add a resistor between the SMU and the device's gate in the case of test a FET or IGBT. For example in ***Figure 20***, a 10kΩ resistor would be added between SMU5 and the gate node. This resistor can stabilize measurements, and, because the gate does not draw much current, the resistor does not cause a significant voltage drop.

If voltages in excess of 40V will be used during the test sequence, the test fixture and SMUs must have the proper interlock installed and be operational according to normal safety procedures.

Summary

Methods were shown how to increase from 3A to 40A the maximum current level that can be measured:

1. Pulse sweeps
2. Combining multiple SMU channels in parallel to achieve higher current

Example results using these techniques were given for commercially-available devices, and the results show excellent correlation with the published datasheets.

In addition, important test implementation factors were discussed in detail, including source readback, four-wire measurements, single V-source at each DUT node, and mitigating excessive energy dissipation due to device breakdown.

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