DAS-Scan Register-Level Programming

USER'S GUIDE

DAS-Scan Register-Level Programming User's Guide

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Preface

This guide describes the register-level functions of the DAS-Scan system and is offered as a supplement to the *DAS-Scan User's Guide*.

The *DAS-Scan Register-Level Programming User's Guide* is intended for users whose applications require operational control through the registers of the SCAN-AD-HR board. To use the information in this manual, you must be familiar with data acquisition principles and with the functions of the DAS-Scan system. You must also be familiar with the configuration and installation requirements for the boards, and you must be experienced at programming register-level functions.

Note: The information in this guide is not intended for use with any of the software packages currently available for DAS-Scan system. If you want information on a particular software package, refer to the manual for that package.

This guide is organized as follows:

- Chapter 1 describes the functions for each I/O address of the DAS-Scan system.
- Chapter 2 outlines example procedures for programming the DAS-Scan system.
- Appendix A summarizes functions of the bits at each I/O address.

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I/O Addresses

The DAS-Scan system uses 16 addresses in the computer I/O space. The addresses start at the base address and extend as shown in the I/O map of Table 1-1.

Table 1-1. I/O Address Map

Location	Function	Type
Base Address +0h[1]	A/D FIFO[2] QRAM data A/D conversion	Read Read/Write Write
Base Address +2h	Data Select register	Read/Write
Base Address +3h	Board Identification register	Read
Base Address +4h	Control Register A	Read/Write
Base Address +5h	Control Register B	Read/Write
Base Address +6h	Control Register C	Read/Write
Base Address +7h	Status register	Read/Write
Base Address +8h	Burst Length register	Read/Write
Base Address +9h	Burst Mode Conversion Rate register	Read/Write
Base Address +Ah	QRAM Address Start register	Read/Write
Base Address +Bh	N/A	- - -
Base Address +Ch	Counter 0 register	Read/Write
Base Address +Dh	Counter 1 register	Read/Write

Table 1-1. I/O Address Map (cont.)

Location	Function	Type
Base Address +Eh	Counter 2 register	Read/Write
Base Address +Fh	Counter Control register	Write

Notes
[1] Access to the data sources at Base Address +0h requires indirect addressing.
[2] FIFO stands for *first in, first out*.

Note: All register bits of fixed value, except the identification value in the upper nibble of the Board Identification register (Base Address +3h), are reserved for internal use and subject to change without notification; do not change or use these bits.

The following sections describe the I/O map in more detail.

Base Address +0h

The register at Base Address +0h can perform any of the following functions:

- Read data from the A/D FIFO
- Read/write data from/to the QRAM
- Write data to initiate an A/D Conversion

Access to the register at Base Address +0h requires indirect addressing, using the Data Select register. Refer to “Base Address +2h” on page 1-5 for more information.

The functions of the register at Base Address +0h are described in the following subsections.

A/D FIFO Data (Read)

The 16-bit A/D FIFO data is read-only and uses 16-bit data transfers on the computer bus. Data is right-justified and in twos complement format for bipolar mode and positive magnitude for unipolar mode.

Data words in the SCAN-AD-HR board are 16-bits long. In bipolar or unipolar mode, bit assignments for A/D FIFO data in the SCAN-AD-HR board are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Note: The Data Select register (Base Address +2h) must be set to 00h prior to reading the A/D FIFO data.

QRAM Data (Read/Write)

The channel-gain QRAM is read/write when used in conjunction with the QRAM Address Start register (Base Address +Ah). The QRAM uses 16-bit data transfers on the computer bus. Bit assignments for QRAM data are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GN2	GN1	GN0	X	MUX11	MUX10	MUX9	MUX8	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0

The bit names are defined and used as follows:

- **Bits 15** to **13:** GN2 to GN0 - These bits set the gain code of the instrumentation amplifier on the SCAN-BRD assembly. Table 1-2 lists the gain codes and corresponding gain settings.

Table 1-2. Gain-Code-Select Bits GN1 and GN0

Gain Code			Gain Value
GN2	GN1	GN0	SCAN-AD-HR Board
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	50
1	0	1	100
1	1	0	200
1	1	1	400

- **Bit 12**: X- The X indicates that a value for bit 12 does not matter.
- **Bits 11** to **0:** MUX11 to MUX0 - These bits set the address of a SCAN-BRD assembly and the multiplexer input channel. MUX11 to MUX6 set the board address of a SCAN-BRD assembly, while MUX5 to MUX0 set the address of the multiplexer input channel on that SCAN-BRD assembly.

To program the QRAM refer to “Programming the QRAM Data Register” on page 2-1.

A/D Conversion (Write)

A write to Base Address +0h starts an A/D conversion only if the following conditions exist:

- The software pacer clock is selected (by S1 and S0 of Control Register C at Base Address +6h).
- Conversions are enabled (by CVEN of the Status register at Base Address +7h).
- A/D conversion is selected by the Data Select register, at Base Address +2h (the value of the Data Select Register must be 00h).

Note: Any data written to Base Address +0h during an A/D conversion is not used.

Base Address +2h

The register at Base Address +2h is the Data Select register and is read/write. This register selects the data source to connect with the computer's data bus. Possible data sources are the A/D Converter and the channel-gain QRAM. This register is set to 00h during power-up reset.

Bit assignments of the Data Select register are as follows:

7	6	5	4	3	2	1	0
0	0	0	0	0	DSL2	DSL1	DSL0

The bit names are defined and used as follows:

- **Bits 7** to **3** - These bits should be set to a fixed value of 0.
- **Bits 2** to **0:** DSL2 to DSL0 - These bits select a data source to connect to the computer bus, according to the values shown in Table 1-3.

Table 1-3. Data-Source-Select Bits DSL2 and DSL0

DSL2	DSL1	DSL0	Data Source
0	0	0	A/D Converter
0	0	1	QRAM
0	1	0	Not used
0	1	1	Not used
1	0	0	Not used
1	0	1	Not used

Table 1-3. Data-Source-Select Bits DSL2 and DSL0 (cont.)

DSL2	DSL1	DSL0	Data Source
1	1	0	Not used
1	1	1	Not used

Base Address +3h

The register at Base Address +3h is the Board Identification register and is read-only. The value of the upper nibble of the Board Identification register is fixed at 1h, while the value of the lower nibble is X (value does not matter). Bit assignments for this register are as follows:

7	6	5	4	3	2	1	0
0	0	0	1	X	X	X	X

Base Address +4h

The register at Base Address +4h is Control Register A and is read/write. This register controls the trigger/gate, counter 1/counter 2, and FIFO Enable functions. This register is set to 00h during power-up reset. Bit assignments for Control Register A are as follows:

7	6	5	4	3	2	1	0
ATEN	TGPL	TGSL	TGEN	CGSL	CGEN	0	FFEN

Bit names for Control Register A are defined as follows:

- **Bit 7:** ATEN - This bit indicates whether the about-trigger mode is enabled/disabled and is using Counter 0 programmed for Interrupt On Terminal Count (82C54 Mode 0) as a post-trigger counter. Conversions can be started by software (TGEN = 0) or by a hardware external trigger (TGEN = 1). After a hardware trigger (TGIN) is

detected (or second hardware trigger in the case TGEN = 1), Counter 0 begins to count down until it reaches zero (Counter 0 Terminal Count). Counter 0 reaches zero N conversions later, where N is the value loaded into counter 0 (zero < N). When counter 0 reaches zero, A/D conversions stop and an interrupt is issued.

ATEN functions are as follows:

– ATEN = 0 disables about-triggering

– ATEN = 1 enables about-triggering

Note: Counter 0 must be programmed for 82C54 Mode 0 if about-trigger mode is to function.

See also “Base Address +7h” on page 1-13 for information on the Counter 0 Terminal Count (C0TC) bit.

- **Bit 6:** TGPL - This bit selects the polarity of the external trigger/gate input for connector J5 signal TGIN and determines the polarity that will initiate the triggering or gating of A/D conversions or initiate a trigger to start the about-trigger counter, counter 0. TGPL functions are as follows:

  – TGPL = 0 selects negative edge/level for external trigger/gate

  – TGPL = 1 selects positive edge/level for external trigger/gate

- **Bit 5**: TGSL - This bit selects external trigger/gate selects connector J5 signal TGIN as either a trigger input or a gate input, as follows:

  – TGSL = 0 selects external trigger (edge)

  – TGSL = 1 selects external gate (level)

  In about-trigger mode, set TGSL to 0 (trigger selected).

- **Bit 4:** TGEN - This bit enables/disables connector J5 signal TGIN as a trigger or gate source for A/D conversions. TGEN does not enable/disable TGIN as a trigger or gate for about-trigger mode. TGEN functions are as follows:

  – TGEN = 0 disables external trigger/gate

  – TGEN = 1 enables external trigger/gate

Note: When TGEN = 1, jumper J6 must be set for TGIN.

When about-trigger mode is enabled (ATEN = 1) and hardware triggers are enabled (TGEN = 1), the first hardware trigger starts conversions, and the second hardware trigger begins counting down conversions (counter 0) to ultimately stop conversions.

- **Bit 3:** CGSL - This bit selects either control bit CGEN or connector J5 signal TGIN as the Counter 1/Counter 2 gate source (see “Base Address +Ch, +Dh, +Eh, and +Fh” on page 1-20 for more information on Counter 1/Counter 2). CGSL functions are as follows:
  - CGSL = 0 selects control bit CGEN as the Counter 1/Counter 2 gate source
  - CGSL = 1 selects the trigger/gate signal on connector J5 as the Counter 1/Counter 2 gate source

Note: When CGSL = 1, jumper J6 must be set for TGIN.

- **Bit 2:** CGEN - This bit functions only if bit CGSL = 0; CGEN functions are as follows:
  - CGEN = 0 disables the Counter 1/Counter 2 gate
  - CGEN = 1 enables the Counter 1/Counter 2 gate
- **Bit 1** - This bit should have a fixed value of 0.
- **Bit 0:** FFEN - This bit enables/disables the FIFO's read and write address pointers. The FIFO should be reset before A/D conversions are enabled to ensure proper FIFO operation. FFEN functions are as follows:
  - FFEN = 0 disables FIFO (FIFO reset)
  - FFEN = 1 enables FIFO

Table 1-4 shows trigger modes using an internal A/D pacer clock (82C54 counter 1/counter 2).

Table 1-4. Trigger Modes Using an Internal A/D Pacer Clock

Function	ATEN	TGSL	TGEN	CGSL	CGEN	T/G Source
Internal Gate	0	X[1]	0	0	G[2]	CGEN
External Gate	0	1	1	1	X	TGIN
External Post Trigger	0	0	1	1	X	TGIN
Ext. Pre/About Trigger[3]	1	0	0	0	1	TGIN
Ext. Pre/About Trigger[4]	1	0	1	0	1	TGIN

Notes
[1] X indicates that value does not matter.
[2] G = Internal gate.
[3] With TGEN = 0, the first external trigger begins the countdown of Counter 0 for pre- and about-trigger acquisitions.
[4] With TGEN = 1, the first trigger starts A/D conversions, and the second trigger begins the countdown of Counter 0 for pre- and about-trigger mode.

Table 1-5 shows trigger modes using an external A/D clock signal on connector J5 (when using an external A/D clock signal on connector J5, jumper J6 must be set for XCLK).

Table 1-5. Trigger Modes Using an External Pacer Clock

Function	ATEN	TGSL	TGEN	CGSL	CGEN	T/G Source
Internal Gate	0	X[1]	0	0	A[2]	CVEN

Notes
[1] X indicates that value does not matter.
[2] A = Available.

Note: During about-trigger and pre-trigger acquisitions, the Convert Enable bit (CVEN) is automatically reset to 0 when Counter 0 reaches Terminal Count.

Base Address +5h

The register at Base Address +5h is Control Register B and is read/write. Control Register B sets the enabling/disabling and the levels of interrupts and DMA. This register is set to 00h during power-up reset, thereby disabling DMA and interrupts. Bit assignments for this register are as follows:

7	6	5	4	3	2	1	0
CIEN	FIMD	IL2	IL1	IL0	DL2	DL1	DL0

The bit names are defined as follows:

- **Bit 7:** CIEN - This bit enables/disables interrupt on Counter 1/Counter 2 Terminal Count, as follows:
  - CIEN = 0 disables the interrupt on Counter 1/Counter 2
  - CIEN = 1 enables the interrupt on Counter 1/Counter 2
- **Bit 6:** FIMD - This bit enables the FIFO Interrupt Mode, as follows:
  - FIMD = 0 enables interrupt on FIFO Not Empty only if interrupts are enabled
  - FIMD = 1 enables interrupt on FIFO Half Full only if interrupts are enabled

  FIFO Not Empty or Half Full interrupts are disabled when DMA is enabled.
- **Bits 5 to 3:** IL2 to IL0 - These bits select and enable the desired interrupt level for processing interrupts.

  If interrupts are enabled and DMA is disabled, an interrupt is generated according to the status of the FIFO Interrupt mode (FIMD) bit. If interrupts are enabled and DMA is enabled, an interrupt is generated when the computer's DMA controller issues a terminal count (T/C) to signify completion of the DMA transfer.

IL2 to IL0 function as shown in Table 1-6.

Table 1-6. Interrupt Level Select Bits IL2 to IL0

IL2	IL1	IL0	Interrupt Level
0	0	0	Interrupts not enabled
0	0	1	Level 3
0	1	0	Level 5
0	1	1	Level 7
1	0	0	Interrupts not enabled
1	0	1	Level 10
1	1	0	Level 11
1	1	1	Level 15

- **Bits 2 to 0:** DL2 to DL0 - These bits enable/disable DMA operation. A DMA request is issued when the FIFO is not empty.

  DL2 to DL0 function as shown in Table 1-7.

Table 1-7. DMA Level Select Bits DL2 to DL0

DL2	DL1	DL0	Function
0	0	0	Disable DMA
0	0	1	Select DMA level 5
0	1	0	Select DMA level 6
0	1	1	Select DMA level 7
1	0	0	disable DMA
1	0	1	Select DMA levels 5 and 6
1	1	0	Select DMA levels 6 and 7
1	1	1	Select DMA levels 7 and 5

As Table 1-7 shows, the SCAN-AD-HR board supports single or dual DMA. In dual DMA mode, the first level used for data transfer is the first level indicated in the sequences shown under *Function* in Table 1-7. For example, when bits DL0 = 1, DL1 = 0, and DL2 = 1, they select dual DMA operation at levels 5 and 6. From Table 1-7, level 5 is the first DMA level used for data transfer; level 6 follows.

Base Address +6h

The register at Base Address +6h is Control Register C and is read/write. This register controls the following board-level functions: selection of unipolar/bipolar input mode, selection of differential input mode, selection of the ADC pacer clock source, and enabling/disabling of the burst mode. Control Register C is set to 00h during power-up reset.

Bit assignments for Control Register C are as follows:

7	6	5	4	3	2	1	0
U/B	0	X	UQEN	0	BMDE	S1	S0

The bit names for Control Register C are defined as follows:

- **Bit 7:** U/B - The Unipolar/Bipolar select bit functions as follows:
  - U/B = 0 sets the analog input for bipolar mode
  - U/B = 1 sets the analog input for unipolar mode
- **Bit 6** - Bit 6 should be fixed at a value of 0.
- **Bit 5:** X - The X indicates that the value for this bit does not matter.
- **Bit 4:** UQEN - *This bit* a enables upper QRAM address bits QA6 and QA7 (see “Base Address +Ah” on page 1-19) for addressing up to 256 locations in QRAM. Bit 4 must be set to 1 for the SCAN-AD-HR board. **Bit 3:** fixed - set this bit to 0.
- **Bit 2:** BMDE - This bit enables or disables burst mode as follows:
  - BMDE = 0 disables burst mode
  - BMDE = 1 enables burst mode

- **Bits 1 and 0:** S1 and S0 - These bits select the pacer-clock source for A/D conversions as shown in Table 1-8.

Table 1-8. Pacer Clock Select Bits S1 and S0

S1	S0	Function
0	0	Software convert only
0	1	Internal pacer clock source 82C54 (counter 1/counter 2 falling edge)
1	0	External pacer clock source (rising edge) XCLK
1	1	External pacer clock source (falling edge) XCLK

Note: When using an external clock source from connector J5, set jumper J6 for XCLK.

Base Address +7h

The register at Base Address +7h is the Status register and is read/write. The Status register is set to a value of 00h during power-up reset. Bit assignments are as follows:

7	6	5	4	3	2	1	0
CVEN	FNE	FHF	OVF	C0TC	C2TC	DMATC	INT

You can read all bits of the Status register by issuing an I/O read at Base Address +7h. You can also clear, set, and mask many of the Status register bits by manipulating them as shown in Table 1-9.

Table 1-9. Status Register Bit Manipulation Operations

Bit No.	Flag	Bit Manipulation Operation
0	INT - Event-driven interrupt	Read, Clear[1], Mask[2]
1	DMATC - DMA Terminal Count	Read, Clear, Mask
2	C2TC - Counter 2 Terminal Count	Read, Clear, Mask
3	C0TC - Counter 0 Terminal Count	Read, Clear, Mask
4	OVF - Conversion overflow	Read, Clear, Mask
5	FHF - FIFO Half Empty	Read
6	FNE - FIFO Not Empty	Read
7	CVEN - Convert Enable/Disable A/D Conversions	Read, Clear, Mask, Set[3]

Notes
[1] *Clear* indicates that writing a 0 to this location clears the bit.
[2] *Mask* indicates that writing a 1 to this location protects the value of the bit against an overwrite. The exception is CVEN, which is masked against an overwrite by bit 6 of the Status register.
[3] *Set* indicates that writing a 1 to this location sets the bit to a 1.

The bit names are defined as follows:

- **Bit 7:** CVEN - This bit enables disables A/D conversions. When this bit is low, no conversions take place. When this bit is high, conversion take place depending on the states of triggers, gates, and pacer clocks.

  Note: Hardware automatically resets CVEN in the event of a FIFO overflow condition or when, during an about-trigger acquisition, a Counter 0 Terminal Count occurs.

  CVEN can be written to only if bit 6 of this register is 0. You use bit 6 to mask CVEN from being over-written when you wish to clear other bits in this register. Writing a 0 to bit 6 does not reset bit 6 to 0.

CVEN functions as follows:

– CVEN = 0 disables conversions

– CVEN = 1 enables conversions

Note: CVEN is automatically reset by hardware in the event of a FIFO overflow condition or when, during about-trigger acquisitions, a Counter 0 Terminal Count occurs.

- **Bit 6:** FNE - This bit indicates whether the FIFO contains data and can not be reset by writing to the status register.

  FNE functions are as follows:

  – FNE = 0 if the FIFO is empty

  – FNE = 1 if the FIFO is not empty

Note: When FIMD (bit 6) of Control Register B is 0 and interrupts are enabled (and DMA disabled), a FIFO Not Empty event causes an interrupt and sets INT (bit 0) of the Status register to 1.

- **Bit 5:** FHF - This bit indicates whether the FIFO is half full (512 words) or not half full; FHF can not be reset by writing to the Status register. This interrupt is useful in conjunction with the Intel INSW instruction to move large blocks of data. FHF functions as follows:

  – FHF = 0 if the FIFO is not half full

  – FHF = 1 if the FIFO is half full

Note: When FIMD (bit 6) of Control Register B is 1 and interrupts are enabled (and DMA Disabled), the FIFO Half Full event causes an interrupt and sets INT (bit 0) of the Status register to 1.

- **Bit 4:** OVF - This bit indicates that the FIFO contains the maximum amount of data it can hold (1024 words) and is about to overflow. To prevent data loss, this condition always terminates A/D conversions (CVEN = 0). If interrupts are enabled, FIFO Overflow always causes

an interrupt and sets the INT bit of the Status register to 1. OVF can be cleared by writing a 0 to Status register bit 4.

OVF functions as follows:

– OVF = 0 if data has not overflowed in FIFO

– OVF = 1 if data has overflowed in FIFO

Note: This status bit is enabled only when the FIFO is enabled (FFEN = 1).

OVF can be masked from being cleared by setting bit 4 to 1 when you write to the Status register.

- **Bit 3:** C0TC - This bit indicates whether Counter 0 has reached its Terminal Count and is to be used in conjunction with about-trigger mode. Counter 0 must be programmed for 82C54 Mode 0 and ATEN (bit 7) of Control Register A set to 1 for about-trigger mode to operate. If interrupts are enabled, this event causes an interrupt and sets the INT bit of this register to 1. C0TC can be cleared by writing a 0 to Status register bit 3.

  C0TC functions are as follows:

  – C0TC = 0: a Counter 0 Terminal Count has not occurred

  – C0TC = 1: a Counter 0 Terminal Count has occurred

  Note: C0TC is enabled only when about-triggering is enabled (ATEN = 1).

  C0TC can be masked from being cleared by setting bit 3 to a 1 when you write to the Status register.

- **Bit 2:** C2TC - This bit indicates whether Counter 2 of the cascaded Counters 1 and 2 has reached its Terminal Count. Bit 2 detects a low-going Terminal Count pulse (82C54 mode 2) when CIEN (bit 7) of Control Register B is set to a 1. If interrupts are enabled, this event will cause an interrupt and set the INT bit of this register to 1. C2TC can be cleared by writing a 0 to Status register bit 2.

C2TC functions are as follows:

– C2TC = 0: a counter 1/counter 2 Terminal Count has not occurred

– C2TC = 1: a counter 1/counter 2 Terminal Count has occurred

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Note: C2TC is enabled only if an interrupt is enabled on Counters 1 and 2 (CIEN = 1).

You can mask C2TC from being cleared by setting bit 2 to 1 when you write to the Status register.

- **Bit 1:** DMATC - When DMA is enabled, DMATC indicates that a DMA Terminal Count has been reached. If interrupts are also enabled, this event causes an interrupt and sets the INT bit of this register. DMATC can be cleared by writing a 0 to Status register bit 1.

  DMATC functions are as follows:

  – DMATC = 0 if a DMA terminal count has not occurred

  – DMATC = 1 if a DMA terminal count has occurred

  Note: DMATC is enabled only if DMA is enabled.

  DMATC can be masked from being cleared by setting bit 1 to 1 when you write to the Status register.

- **Bit 0:** INT - The events that can cause an interrupt flag to be set to be set are as follows:

  – DMA Terminal Count

  – Counter 1/Counter 2 Terminal Count

  – Counter 0 Terminal Count

  – FIFO Overflow

  – FIFO Half Full

  – FIFO Not Empty

  Interrupts must be enabled for this bit to function. INT can be cleared by writing a 0 to Status register bit 0.

INT functions are as follows:

– INT = 0 indicates that no interrupt has occurred

– INT = 1 indicates that an interrupt has occurred

Note: You can mask INT from being cleared by setting bit 0 to 1 when you write to the Status register.

Base Address +8h

The register at Base Address +8h is the Burst Length register and is read/write. This register controls the operation of the Burst Length counter when in burst mode. The Burst Length register is set to 00h during power-up reset.

Bit assignments of the Burst Length register are as follows:

7	6	5	4	3	2	1	0
BLV7	BLV6	BLV5	BLV4	BLV3	BLV2	BLV1	BLV0

Bits 7 to 0: BLV7 to BLV0 - These bits represent the *Burst Length Value*. These bits determine the number of conversions to perform for each pacer clock tick during a burst mode acquisition. These bits have no function if burst mode is not enabled. Burst Length Values have the following characteristics: Burst Length = BLV + 1; BLV < 256

Base Address +9h

The register at Base Address +9h is the Burst Mode Conversion Rate register and is an 8-bit read/write register. This register's lower six bits program the burst mode conversion rate (A/D conversion rate) during burst mode acquisition. This register is set to 00h during power-up reset.

Bit assignments of the Burst Mode Conversion Rate register are as follows:

7	6	5	4	3	2	1	0
X	X	BRV5	BRV4	BRV3	BRV2	BRV1	BRV0

The bit names are defined as follows:

- **Bits 7 and 6**: X - The X indicates that the value of this bit does not matter.
- **Bits 5 to 0:** BRV5 to BRV0 - These bits determine the rate of conversions during a burst mode acquisition. The bits have no function if burst mode is not enabled. The Burst Rate Value has the following characteristics: Burst Rate = 1 MHz / (BRV + 1); BRV > 1

Base Address +Ah

The register at Base Address +Ah is the QRAM Address Start register and is read/write. This register determines the starting address of the channel-gain QRAM for A/D multiplexing. This register, when used in conjunction with the QRAM Data location (Base Address 0h, write), sets the address for loading the QRAM.

Note: The QRAM Address counter is a down counter. Thus, the QRAM is loaded with the first channel-gain data at Address N-1, the next at N-2, and so on down to Address 00h (where N is the scan length).

When a data word has been loaded into the QRAM, the QRAM address automatically decrements. Thus, a QRAM address need not be loaded prior to every QRAM data write. An address write need only occur at the beginning and end of loading the entire scan data into the QRAM.

After all of the channel-gain data is loaded into the QRAM, the QRAM address must be set to the *starting* address by writing the starting address to the QRAM Address Start register.

Bit assignments of the QRAM Address Start register are as follows:

7	6	5	4	3	2	1	0
QAS7	QAS6	QAS5	QAS4	QAS3	QAS2	QAS1	QAS0

Bits 7 to 0: QAS7 to QAS0 - These bits determine the starting address of the channel-gain QRAM for A/D multiplexing.

About 500 ns after the ADC starts a conversion, while the sample/hold is holding the previous channel, the QRAM address decrements for the next conversion. At the end of a conversion scan, the cycle repeats, starting with the QRAM start address. On writing to the QRAM Address Start register, the QRAM Address counter always automatically initializes to the QRAM start address. To perform conversions on a single channel, set the QRAM start address to 00h and load the QRAM with the appropriate channel number and gain data. The QRAM Address register is set to 00h during power-up reset.

Base Address +Ch, +Dh, +Eh, and +Fh

The registers from Base Address +Ch to +Fh correspond to the four registers of the 82C54 Programmable Counter/Timer. Refer to the Intel 82C54 data sheet for a full description of features (you can obtain the data sheet from Intel by telephoning 800/548-4725).

On the SCAN-AD-HR board, counter 0 of the 82C54 is dedicated to serving as an A/D conversion counter for the about-trigger mode. In the about-trigger mode, **counter 0 MUST be programmed in 82C54 Mode 0.**

Counters 1 and 2 of the 82C54 are used as the onboard A/D pacer clock or as a programmable interrupt generator. These counters are cascaded as Counter 1 then Counter 2, with the Counter 2 output as the source of A/D pacing or programmed interrupts. **These counters must be programmed in 82C54 Mode 2.** The read/write capabilities of Counter/Timer registers are shown in Table 1-10.

Table 1-10. Read/Write Capabilities of Counter/Timer Registers

Base Address	Register	Mode
+Ch	Counter 0	Read/Write
+Dh	Counter 1	Read/Write
+Eh	Counter 2	Read/Write
+Fh	82C54 control	Write only

Note: Counter 0 is programmed with the number of post-trigger samples for about-trigger mode (0 < # of post-trigger samples < 65,536).
Counter 1 Rate = 5 MHz ÷ N; where 1 < N < 65,536.
Counter 2 Rate = counter 1 Rate ÷ M; where 1 < M < 65,536.
Pacer clock period = 200 ns ∞ N ∞ M.
Counters 1 and 2 must be disabled when written to.

2

Programming Example

This chapter provides basic steps for programming an A/D conversion with the SCAN-AD-HR board.

In the following example, program the SCAN-AD-HR board for bipolar mode, software conversions, and internal trigger. You are sampling the data input channels of four SCAN-BRD assemblies in ascending order (board addresses of 00h to 03h), using a gain of 2 for for the SCAN-BRD assemblies. To perform the A/D conversion, program the QRAM Data register first, then program the board setup. The following sections describe these procedures.

Programming the QRAM Data Register

Perform the following procedure to program the QRAM Data register:

1. Set the Data Select register to point to the QRAM by writing the value 01h to Base Address +2h.
2. Initialize the QRAM starting address to the number of SCAN-BRD assemblies minus one by writing the value 03h to Base Address Ah.
3. Load the QRAM Data register (Base Address +0h) with hexadecimal values representing the following information:
   - GN2 to GN0 = 001
   - Board address (MUX11 to MUX6) for each SCAN-BRD assembly.
   - Input channel address (MUX5 to MUX0) for each input channel of each SCAN-BRD assembly

3a. Begin with the SCAN-BRD assembly at board address 00h as follows:

- For input channel 0, write 2000h to Base Address +0h.
- For input channel 1, write 2001h to Base Address +0h.

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- For input channel 63, write 203Fh to Base Address +0h.

3b. Continue with the SCAN-BRD assembly at board address 01h as follows:

- For input channel 0, write 2040h to Base Address +0h.
- For input channel 1, write 2041h to Base Address +0h.

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- For input channel 63, write 207Fh to Base Address +0h.

3c. Continue with the SCAN-BRD assembly at board address 02h as follows:

- For input channel 0, write 2080h to Base Address +0h.
- For input channel 1, write 2081h to Base Address +0h.

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- For input channel 63, write 20BFh to Base Address +0h.

3d. Complete the programming of the QRAM Data register with entries for the SCAN-BRD assembly at board address 03h as follows:

- For input channel 0, write 20C0h to Base Address +0h.
- For input channel 1, write 20C1h to Base Address +0h.

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- For input channel 63, write 20FFh to Base Address +0h.

4. Re-initialize the QRAM to its starting address by writing the value 03h to Base Address Ah.

Programming the Board Setup

Program the board for its A/D modes, input configuration, trigger modes, and other operations as follows:

1. Set the A/D operating modes (bipolar and software conversions) by writing the value 00h to Base Address +6h (Control Register C).
2. Enable the A/D FIFO by writing the value 01h to Base Address +4h (Control Register A).
3. Set the Data Select register to point to the A/D FIFO by writing the value 00h to Base Address +2h.
4. Enable A/D conversions by writing the value 80h to Base Address +7h (Status register).
5. Initiate an A/D conversion by writing any word value to Base Address +0h.
6. Poll for the condition of *A/D FIFO Not Empty* by continuously reading Base Address +7h (Status register) for the condition of bit 6 = 1.
7. Read the A/D FIFO by reading a word of ADC data from Base Address +0h.
8. Repeat steps 5, 6, and 7 until inputs from all four SCAN-BRD assemblies are converted.
9. Disable A/D conversions by writing the value 00h to Base Address +7h (Status register).
10. Disable the A/D FIFO by writing the value 00h to Base Address +4h (Control Register A).

A

Summary of I/O Address Bits

Table A-1 and Table A-2 show the bit assignments for the registers. Table A-3 summarizes the functions of all bits at the I/O addresses.

Table A-1. Bit Assignments for 16-Bit Registers

Bit #	15/7	14/6	13/5	12/4	11/3	10/2	9/1	8/0
Base Address +0h Read/Write for QRAM Data	G2/ MUX7	GN1/ MUX6	GN0/ MUX5	X/ MUX4	MUX11/ MUX3	MUX10/ MUX2	MUX9/ MUX1	MUX8/ MUX0
Base Address +0h Read Only for A/D Data (Bipolar or Unipolar)	D15/D7	D14/D6	D13/D5	D12/D4	D11/D3	D10/D2	D9/D1	D8/D0

Table A-2. Bit Assignments for 8-Bit Registers

Bit #	7	6	5	4	3	2	1	0
Base Address +2h Read/Write: Data Select Bits	0	0	0	0	0	DSL2	DSL1	DSL0
Base Address +3h Read Only for Board Identification register	0	0	0	1	X	X	X	X
Base Address +4h Read/Write: Control Register A Bits	ATEN	TGPL	TGSL	TGEN	CGSL	CGEN	0	FFEN
Base Address +5h Read/Write: Control Register B Bits	CIEN	FIMD	IL2	IL1	IL0	DL2	DL1	DL0
Base Address +6h Read/Write: Control Register C Bits	U/B	0	0	UQEN	0	BMDE	S1	S0

Table A-2. Bit Assignments for 8-Bit Registers (cont.)

Bit #	7	6	5	4	3	2	1	0
Base Address +7h Read/Write: Status Bits	CVEN	FNE	FHF	OVF	C0TC	C2TC	DMATC	INT
Base Address +8h Read/Write: Burst Length Bits	BLV7	BLV6	BLV5	BLV4	BLV3	BLV2	BLV1	BLV0
Base Address +9h Read/Write: Burst Mode Conversion Rate Bits	X	X	BRV5	BRV4	BRV3	BRV2	BRV1	BRV0
Base Address +Ah Read/Write: QRAM Address Start Bits	QAS7	QAS6	QAS5	QAS4	QAS3	QAS2	QAS1	QAS0

Table A-3. Summary of I/O Address Bits

Bit Name	Description	Page Reference
ATEN	Enable/disable bit for about-trigger mode	page 1-6
BLV0 to BLV7	Determine the number of conversions during each burst mode scan	page 1-18
BMDE	Enables/disables burst mode	page 1-12
BRV0 to BRV5	Determine the burst mode conversion rate	page 1-19
C0TC	Indicates whether a Counter 0 Terminal Count has occurred	page 1-16
C2TC	Indicates whether a Counter 1/Counter 2 Terminal Count has occurred	page 1-16
CGEN	Enables/disables the Counter 1/Counter 2 gate	page 1-8
CGSL	Selects either bit CGEN or I/O connector signal TGIN as the Counter 1/Counter 2 gate source	page 1-8
CIEN	Enables/disables the interrupt on Counter 1/Counter 2 terminal count	page 1-10
CVEN	Enables/disables A/D conversions	page 1-14
D0 to D15	Data bits for A/D FIFO data	page 1-3
DL0 to DL2	Enables/disables DMA operation and sets DMA level	page 1-11
DMATC	Indicates whether a DMA Terminal Count has occurred	page 1-17
DSL0 to DSL2	Selects the data source to connect to the computer bus	page 1-5

Table A-3. Summary of I/O Address Bits (cont.)

Bit Name	Description	Page Reference
FFEN	Enables/disables the FIFO read/write address pointers	page 1-8
FHF	Indicates whether or not the FIFO is half full	page 1-15
FIMD	Enables interrupt on FIFO Not Empty or FIFO Half Full - only when interrupts are enabled	page 1-10
FNE	Indicates whether the FIFO is not empty	page 1-15
GN0 to GN2	Selects the gain code	page 1-3
IL0 to IL2	Selects and enables the interrupt level	page 1-10
INT	Indicates whether an interrupt has occurred	page 1-17
MUX0 to MUX11	Address bits for multiplexer; MUX6 to MUX11 select the SCAN-BRD assembly, while MUX0 to MUX 5 select the multiplexer input channel.	page 1-4
OVF	Indicates whether data has overflowed in the FIFO	page 1-15
QAS0 to QAS7	Determines starting address of the channel-gain QRAM	page 1-19
S0 and S1	Selects the pacer clock source for A/D conversions	page 1-13
TGEN	Enables/disables connector J5 signal TGIN as a trigger or gate source for A/D conversions	page 1-7
TGPL	Sets the polarity for initiating a trigger/gate of A/D conversions or a trigger to start the about-trigger counter	page 1-7
TGSL	Selects connector J5 signal TGIN as either an external trigger or an external gate	page 1-7
U/B	Selects unipolar or bipolar input mode	page 1-12
UQEN	Enables QRAM address bits QA6 and QA7 for addressing up to 256 locations in QRAM	page 1-12