Taken from DAS-8, DAS-8/PGA(G2), DAS-8/AO, & DAS-8/LT USER GUIDE Revision F, April 1993

Chapter 3 PROGRAMMING Section 3.2 only

I/O Address Map of DAS-8/PGA(G2)/AO/LT

First let's look at the DAS-8/PGA(G2)/AO/LT I/O address map:

ADDRESS	READ	WRITE
Base Address	+ 0	A/D Lo byte Start 8 bit A/D conversion
	+ 1	A/D Hi byte Start 12 bit A/D conversion
	+ 2	STATUS register CONTROL register
	+ 3*	Status & Gain Gain Control Register
	+ 4	Read Counter 0 Load Counter 0
	+ 5	Read Counter 1 Load Counter 1
	+ 6	Read Counter 2 Load Counter 2
	+ 7	- Counter control
	+ 8**	Simul. Update DAC 0 Lo Byte
	+ 9**	Simul. Update DAC 0 Hi Byte
	+10**	Simul. Update DAC 1 Lo Byte
	+11**	Simul. Update DAC 1 Hi Byte

* DAS-8/PGA(G2) only.
**DAS-8/AO

Since the A/D provides 12 bits of data, it requires two bytes to handle each word of data. Data is held as Low Byte first, then High Byte. This sequence is a convenience for Assembly Language programmers, since the 8088 processor in the IBM PC accesses data in this order. Now that we know register location, let's examine the data format of each register and illustrate data transfer using INP's and OUT's.

Initiating A/D Conversion

An A/D conversion is initiated by writing to Location BASE ADDRESS+0 or BASE ADDRESS+1. If you write to BASE ADDRESS+1, a full 12-bit A/D conversion is performed. Writing to BASE ADDRESS+0 initiates a short cycle (8-bit) conversion. A 12-bit conversion takes no more than 35 microseconds (max) to complete, while a short cycle 8-bit conversion takes less time (25 microseconds, max). These times are dependent upon the type and manufacturer of AD574 ADC used in your DAS-8/PGA(G2)/AO/LT and may be less, but will not exceed the durations specified.

A/D conversion example code (BASICA):

```
12 bits     xxx10 OUT BASADR% + 1, 0
8 bits      xxx10 OUT BASADR%, 0
```

Data written to these locations is irrelevant and is lost; the decoded Address Write Pulse is, in fact, what triggers the A/D.

A/D Data Format

At the end of a conversion cycle, data from the A/D may be read from Locations BASE ADDRESS+0 and BASE ADDRESS+1. Data follows the usual Intel Low Byte/High Byte sequence. BASE ADDRESS+1 contains the most significant 8 bits from the conversion:

```
Bits  D7    D6    D5    D4    D3    D2    D1    D0
Base Addr+1 B1    B2    B3    B4    B5    B6    B7    B8
      (MSB)
```

The remaining four LSBs (followed by 4 zeroes) are read from BASE ADDRESS+0:

```
Bits  D7    D6    D5    D4    D3    D2    D1    D0
Base Addr+0 B9    B10   B11   B12   0     0     0     0
                        (LSB)
```

A/D data bits B1-B12 correspond to an offset binary code, as follows:

```
      BINARY      HEX   ANALOG INPUT VOLTAGE
0000  0000  0000  000   -5.0000 V (-Full scale)
0000  0000  0001  001   -4.9976 V
.     .     .     .     .
0100  0000  0000  400   -2.5000 V (-1/2 scale)
.     .     .     .     .
1000  0000  0000  800   ±0 V (zero)
1000  0000  0001  801   +0.0024 V
.     .     .     .     .
1100  0000  0000  C00   +2.5000 V (+1/2 scale)
.     .     .     .     .
1111  1111  1111  FFF   +4.9976 V (+Full scale)
```

A sequence of BASIC INP instructions to read data would be:

```
xxx10 XL%=INP(BASADR%)  'read low byte
xxx20 XH%=INP(BASADR% + 1)    'read high byte
xxx30 X% = XH%x16 + XL%/16    'combine bytes, X% = data
```

From here you may convert the binary data to volts or other engineering units:

```
xxx40 V = X% x (10/4096)      '(output) x (span/resolution)
xxx50  V = V - 5  'subtract zero offset, -5.0000 V
                                        (Bipolar Only)
```

Attenuation and amplification normalization may also be accomplished *`:

```
xxx60 V = V * G
```

* Note: DAS-8/PGA(G2) and DAS-8/AO gain selection is via software.

DAS-8/PGA(G2)/AO/LT Status Register (Read Only)

This status register is a read only register providing DAS-8/PGA(G2)/AO/LT operational information. It is mapped as follows:

Bits	D7	D6	D5	D4	D3	D2	D1	D0
Base Addr+2	EOC	IP3	IP2	IP1	IRQ	MA2	MA1	MA0

The Base Address bits have the following significance:

EOC: End of Conversion. If EOC is high (Logic 1), the A/D is busy performing a conversion. Data should not be read in this condition as it will be invalid. Wait for EOC to return to logic 0 signifying valid data available.
IP3-IP1: These bits correspond to the three digital input port lines IP3, IP2 and IP1. They may be used for any digital data input.

IRQ: After generation of an interrupt, IRQ is set to Logic High (1). It is reset to Logic Low (0) by a Write to the Control Register. This provides a means of acknowledging or "handshaking" DAS-8/PGA(G2)/AO/LT interrupts.
MA2-MA0: Correspond to current multiplexer channel:

MA2	MA1	MA0	CHANNEL
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

DAS-8/PGA(G2)/AO/LT Control Register (Write Only)

The control register sets the multiplexer (channel) address, enables and disables interrupts, provides output data to the 4 general purpose digital outputs OP1-OP4, and resets the IRQ status bit. The control register is a write only register located at BASE ADDRESS + 2 (same location as status register). The data format of the control register is as follows:

Bits	D7	D6	D5	D4	D3	D2	D1	D0
Base Addr+2	OP4	OP3	OP2	OP1	INTE	MA2	MA1	MA0

The Base Address bits have the following significance:

OP4-OP1: These bits correspond to the four general-purpose digital-output lines OP1 - OP4. These accommodate external control functions such as driving an input sub-multiplexer to increase the number of analog input channels. A 16-channel multiplexer on each of DAS-8/PGA(G2)/AO/LT's input channels can expand the system to 128 channels.
INTE: When INTE = 1 (logic high), DAS-8/PGA(G2) generated interrupts are enabled onto one of the selected IBM PC Interrupt Levels 2-7. Interrupts are disabled if INTE = 0 (logic low). Interrupts from INT.IN Input (Pin 24) are passed through to the selected level and are positive-edge triggered. It is the programmer's responsibility to set up an interrupt handling routine interrupt vectors, and to initialize the (IBM PC) 8259 interrupt controller. Writing to the Control Register clear the IRQ bit of the Status Register.

MA2-MA0: These bits select the current analog multiplexer channel:

MA2	MA1	MA0	CHANNEL
0	0	0	0
0	0	1	1
0	1	0	2
0	1	0	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Multiplexer channel address can be determined by reading the status register.

One further note concerning the control register. During power up, the IBM PC RESET line is asserted clearing the DAS-8/PGA(G2)/AO/LT control register. This disables DAS-8/PGA(G2)/AO/LT interrupts, sets digital outputs OP1-4 to zero, sets the multiplexer channel address to zero, and sets the input range to ±5 VDC.

DAS-8/PGA(G2) & DAS-8/AO Gain Control Register (Read/Write)

The Gain Control Register is used to read and set the Programmable Gain Amplifier for the DAS-8/PGA(G2) and DAS-8/AO. The Gain Control Register is, therefore a Read/Write register and is located at Base Address +3. The data format is as follows:

Bits	D7	D6	D5	D4	D3	D2	D1	D0
Base Addr+3 (WRITE)	---	---	---	---	R3	R2	R1	R0
Base Addr+3 (READ)*	---	MA2	MA1	MA0	R3	R2	R1	R0

R3 - R0 select the input range (gain), as follows:

R3	R2	R1	R0	PGA & AO RANGE	PGA-G2 RANGE
0	0	0	0	±5V (Bipolar)	±5V (Bipolar)
1	0	0	0	±10V (Bipolar)	±10V (Bipolar)
1	0	0	1	+10V (Unipolar)	+10V (Unipolar)
1	0	1	0	±0.5V (Bipolar)	±2.5V (Bipolar)
1	0	1	1	+1V (Unipolar)	0-5V (Unipolar)
1	1	0	0	±0.05V (Bipolar)	±1.25V (Bipolar)
1	1	0	1	+0.1V (Unipolar)	0-2.5 V (Unipolar)
1	1	1	0	±0.01V (Bipolar)	±0.625V (Bipolar)
1	1	1	1	+0.02V (Unipolar)	0-1.25V (Unipolar)

* NOTE: When the DAS-8/PGA(G2) or DAS-8/AO Gain Control Register is read, additional information is provided concerning it's operation. See Section 3.2.5 concerning the MA2-MA0 bit significance.

The Counter/Timer Registers

An 8254 programmable interval timer is used on DAS-8/PGA(G2)/AO/LT. This is a versatile device consisting of three individually programmable 16-bit down-counters with a variety of operating modes. A full description of 8254 capability is contained in Chapter 5 (Counter/Timer Operation). Additional technical information concerning this device may be obtained from the "Intel Component Data Catalog" or equivalent manufacturer's data sheet.

From a programming standpoint, addressing the Counter/Timer functions is straightforward. The Counter Registers are Read/Write and located as follows:

BASE ADDRESS + 4 Counter 0
BASE ADDRESS + 5 Counter 1
BASE ADDRESS + 6 Counter 2

Before reading or writing the counter registers, you must write the counter/timer control register to define the operating mode of each counter and the type of data transfer you intend to perform.

The Write Only Counter Control Register is at BASE ADDRESS + 7, as follows:

Bits	D7	D6	D5	D4	D3	D2	D1	D0
Base Addr+7	SC1	SC0	RL1	RL0	M2	M1	M0	BCD

SC1-0: These are the "counter select" bits. They are mapped as shown:

SC1	SC0	Counter Selected
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Invalid

RL1-0: These are the "Read & Load" bits controlling data transfer to the selected counter. They are mapped as shown:

RL1	RL0	Data Transfer Operation
0	0	Counter latching operation
0	1	Read/load high byte
1	0	Read/load low byte
1	1	Read/load low then high byte (Word transfer)

See Chapter 5 (Counter/Timer) for a full description of the data transfer modes.

M2-0: M2 - M0 are Counter Operation Control bits:

M2`	M1`	M0`	Counter Operation MODE
0	0	0	0 - Change on terminal count
0	0	1	1 - Programmable one-shot
0	1	0	2 - Rate generator
0	1	1	3 - Square wave generator
1	0	0	4 - Software triggered strobe
1	0	1	5 - Hardware triggered strobe

See Chapter 4 (Counter/Timer) for a full description of these operating modes.

BCD: This bit controls whether the selected counter will count in binary (2, 4, 8, etc.) or binary-coded-decimal format.

BCD	Counting Code	
0	16 bit binary	(65,535 max.count)
1	4 decade BCD	(9,999 max. count)

Data Format For DAS-8/AO DACs

Refer to the table in Section 3.2. Data is written in true binary and is right-justified, as follows:

Lo Byte

D7	D6	D5	D4	D3	D2	D1	D0
B5	B6	B7	B8	B9	B10	B11	B12
							(LSB)

Hi Byte

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	B1	B2	B3	B4
				(MSB)			

MSB = Most Significant Bit
LSB = Least Significant Bit
X = Value irrelevant.

For Unipolar (0 to +Full-Scale) ranges, coding is true binary, as follows:

```
0000 0000 0000  Zero
1000 0000 0000  1/2 Scale
1111 1111 1111  +Full Scale (minus one bit)
```

For Bipolar (-FS to +FS) ranges, coding is offset binary, as follows:

```
0000 0000 0000  -FS
1000 0000 0000  Zero
1111 1111 1111  +FS (minus one bit)
```

If the SIM/NORM slide switch on the DAS-8/AO is at SIM, a Read to Base Address +8, +9, +10, or +11 updates both DACs simultaneously.

If the SIM/NORM switch is at NORM, only one DAC is updated when the Hi Byte is Written to it.