KEITHLEY

KPCMCIA-12AIAOH

Type II PCMCIA Card

User's Manual

A GREATER MEASURE OF CONFIDENCE

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Type II PCMCIA Card
User's Manual

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Manual Print History

The print history shown below lists the printing dates of all Revisions and Addenda created for this manual. The Revision Level letter increases alphabetically as the manual undergoes subsequent updates. Addenda, which are released between Revisions, contain important change information that the user should incorporate immediately into the manual. Addenda are numbered sequentially. When a new Revision is created, all Addenda associated with the previous Revision of the manual are incorporated into the new Revision of the manual. Each new Revision includes a revised copy of this print history page.

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Safety Precautions

The following safety precautions should be observed before using this product and any associated instrumentation. Although some instruments and accessories would normally be used with non-hazardous voltages, there are situations where hazardous conditions may be present.

This product is intended for use by qualified personnel who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. Read and follow all installation, operation, and maintenance information carefully before using the product. Refer to the manual for complete product specifications.

If the product is used in a manner not specified, the protection provided by the product may be impaired.

The types of product users are:

Responsible body is the individual or group responsible for the use and maintenance of equipment, for ensuring that the equipment is operated within its specifications and operating limits, and for ensuring that operators are adequately trained.

Operators use the product for its intended function. They must be trained in electrical safety procedures and proper use of the instrument. They must be protected from electric shock and contact with hazardous live circuits.

Maintenance personnel perform routine procedures on the product to keep it operating properly, for example, setting the line voltage or replacing consumable materials. Maintenance procedures are described in the manual. The procedures explicitly state if the operator may perform them. Otherwise, they should be performed only by service personnel.

Service personnel are trained to work on live circuits, and perform safe installations and repairs of products. Only properly trained service personnel may perform installation and service procedures.

Keithley products are designed for use with electrical signals that are rated Installation Category I and Installation Category II, as described in the International Electrotechnical Commission (IEC) Standard IEC 60664. Most measurement, control, and data I/O signals are Installation Category I and must not be directly connected to mains voltage or to voltage sources with high transient over-voltages. Installation Category II connections require protection for high transient over-voltages often associated with local AC mains connections. Assume all measurement, control, and data I/O connections are for connection to Category I sources unless otherwise marked or described in the Manual.

Exercise extreme caution when a shock hazard is present. Lethal voltage may be present on cable connector jacks or test fixtures. The American National Standards Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30V RMS, 42.4V peak, or 60VDC are present. **A good safety practice is to expect that hazardous voltage is present in any unknown circuit before measuring.**

Operators of this product must be protected from electric shock at all times. The responsible body must ensure that operators are prevented access and/or insulated from every connection point. In some cases, connections must be exposed to potential human contact. Product operators in these circumstances must be trained to protect themselves from the risk of electric shock. If the circuit is capable of operating at or above 1000 volts, **no conductive part of the circuit may be exposed.**

Do not connect switching cards directly to unlimited power circuits. They are intended to be used with impedance limited sources. NEVER connect switching cards directly to AC mains. When connecting sources to switching cards, install protective devices to limit fault current and voltage to the card.

Before operating an instrument, make sure the line cord is connected to a properly grounded power receptacle. Inspect the connecting cables, test leads, and jumpers for possible wear, cracks, or breaks before each use.

When installing equipment where access to the main power cord is restricted, such as rack mounting, a separate main input power disconnect device must be provided, in close proximity to the equipment and within easy reach of the operator.

For maximum safety, do not touch the product, test cables, or any other instruments while power is applied to the circuit under test. ALWAYS remove power from the entire test system and discharge any capacitors before: connecting or disconnecting cables or jumpers, installing or removing switching cards, or making internal changes, such as installing or removing jumpers.

Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always make measurements with dry hands while standing on a dry, insulated surface capable of withstanding the voltage being measured.

The instrument and accessories must be used in accordance with its specifications and operating instructions or the safety of the equipment may be impaired.

Do not exceed the maximum signal levels of the instruments and accessories, as defined in the specifications and operating information, and as shown on the instrument or test fixture panels, or switching card.

When fuses are used in a product, replace with same type and rating for continued protection against fire hazard.

Chassis connections must only be used as shield connections for measuring circuits, NOT as safety earth ground connections.

If you are using a test fixture, keep the lid closed while power is applied to the device under test. Safe operation requires the use of a lid interlock.

If  or  is present, connect it to safety earth ground using the wire recommended in the user documentation.

The  symbol on an instrument indicates that the user should refer to the operating instructions located in the manual.

The  symbol on an instrument shows that it can source or measure 1000 volts or more, including the combined effect of normal and common mode voltages. Use standard safety precautions to avoid personal contact with these voltages.

The **WARNING** heading in a manual explains dangers that might result in personal injury or death. Always read the associated information very carefully before performing the indicated procedure.

The **CAUTION** heading in a manual explains hazards that could damage the instrument. Such damage may invalidate the warranty.

Instrumentation and accessories shall not be connected to humans.

Before performing any maintenance, disconnect the line cord and all test cables.

To maintain protection from electric shock and fire, replacement components in mains circuits, including the power transformer, test leads, and input jacks, must be purchased from Keithley Instruments. Standard fuses, with applicable national safety approvals, may be used if the rating and type are the same. Other components that are not safety related may be purchased from other suppliers as long as they are equivalent to the original component. (Note that selected parts should be purchased only through Keithley Instruments to maintain accuracy and functionality of the product.) If you are unsure about the applicability of a replacement component, call a Keithley Instruments office for information.

To clean an instrument, use a damp cloth or mild, water based cleaner. Clean the exterior of the instrument only. Do not apply cleaner directly to the instrument or allow liquids to enter or spill on the instrument. Products that consist of a circuit board with no case or chassis (e.g., data acquisition board for installation into a computer) should never require cleaning if handled according to instructions. If the board becomes contaminated and operation is affected, the board should be returned to the factory for proper cleaning/servicing.

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B PCMCIA Interface

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1
Introduction

Getting started

The KPCMCIA-12AIAOH PC card is a PCMCIA type II data acquisition system with four differential or eight single-ended analog input channels. The number of input channels can be expanded to 128 with input expansion cards. Each channel has a bipolar input range from ±0.01V (gain = 1000), ±0.1V (gain =100), ±1V (gain =10), and ±10V (gain = 1) with programmable gains of 1, 10, 100, and 1000. The KPCMCIA-12AIAOH PC card supports sampling rates up to 100 kHz at either 12-bit or 16-bit resolution.

Equipped with a data FIFO of 2048 samples, the KPCMCIA-12AIAOH PC card can achieve full speed data acquisition under Windows 95/98 and Windows NT. It also has a scan FIFO of the same size that supports full-speed, random-order channel scanning and gain selection for all the input channels (up to 128 channels when using the input expansion cards).

The KPCMCIA-12AIAOH PC card has a 24-bit pacer clock and a programmable divided-by-2, by-10, or by-100 pre-scaler. The pacer clock can also be used with an external clock source. With the 10MHz internal clock source, the pacer clock can generate accurate sampling rates from 0.006Hz to 100kHz.

The KPCMCIA-12AIAOH PC cards are also equipped with two independent 12-bit D/A output channels with a bipolar output range from -5 to +5V. The D/A channels can be updated directly when writing to the corresponding D/A port (direct mode) or simultaneously when a synchronization signal (timer overflow, gate control goes low to high, or pacer clock fires) comes.

The analog trigger and pre-trigger are two new features added to the KPCMCIA-12AIAOH PC cards. One of the D/A channels (channel 1) can be used to set up the analog trigger level anywhere in the full input range of the A/D converter (±10V). The pre-trigger mode, when enabled, keeps the most recently received data samples in the data FIFO before the actual trigger comes so these samples can be recorded together with those after the trigger.

The 16-bit timer/counter with auto-reload and read-out latch provides independent timing for the D/A channels. It can also be used as an independent timer/counter for other purposes. The timer/counter operates with internal or external clock sources and with internal or external gate control. Its latched read-out guarantees the integrity whenever the timer/counter's content is referenced.

The KPCMCIA-12AIAOH PC card also has four digital input and four digital output channels, all are TTL compatible, which may be used for controlling or monitoring in addition to analog data acquisition.

The DriverLINX software drivers provided support various programming languages including Visual C/C++, Visual Basic and Delphi. A Dynamic Link Library (DLL) is provided for all types of programming languages under Microsoft Windows and Visual Basic Controls (VBX). The KPCMCIA-12AIAOH PC card also has turn-key software support for TestPoint with optional software support for LabView.

The KPCMCIA-12AIAOH PC card is packaged with a cable terminating in a 37-pin D-type female connector. Refer to Section 6 for a description of the connector pin assignments. For applications requiring discrete wire hook-ups, an optional screw terminal adapter is also available to convert the D-37 connector into 37 discrete screw terminal blocks.

Features

The KPCMCIA-12AIAOH PC card offers the following features:

- 12- or 16-bit A/D resolution.
- Four differential or eight single-ended analog input channels, expandable to 128 channels.
- Bipolar input range up to ±10V.
- Truly programmable gains of 1, 10, 100, and 1000.
- Programmable scan list with up to 2048 channels and gain entries. Selectable scan speed (10, 20, or 40µs).
- Data FIFO of 2048 samples.
- 24-bit pacer clock with variable pre-scalers to generate sampling rates from 0.006Hz to 100kHz (0 to 100kHz with external clock source).*
- Software, TTL, or analog trigger with programmable threshold. Pre-trigger capability up to the size of the data FIFO.
- Two 12-bit D/A channels with direct or synchronized update.
- Additional 16-bit timer/counter with auto-reload, read-out latch, overflow latch, internal/external gate control, and internal/external clock source.
- Digital input/output channels.
- Software drivers for Windows 95/98 and Windows NT, and TestPoint. An optional driver is available for LABView.

*NOTE *In "Paced" mode, the same input pin is shared between external clock and external trigger, hence only one function can be used (not both simultaneously).*

Technical support

Before returning any equipment for repair, call Keithley Instruments, Inc., for technical support at:

1-888-KEITHLEY
Monday - Friday, 8:00 a.m. - 5:00 p.m., Eastern Time

An applications engineer will help you diagnose and resolve your problem over the telephone.

If a telephone resolution is not possible, the applications engineer will issue you a Return Material Authorization (RMA) number and ask you to return the equipment. Include the RMA number with any documentation regarding the equipment.

When returning equipment for repair, include the following information:

- Your name, address, and telephone number.
- The invoice or order number and date of equipment purchase.
- A description of the problem or its symptoms.
- The RMA number on the **outside** of the package.

Repackage the equipment using the original anti-static wrapping, if possible, and handle it with ground protection. Ship the equipment to:

ATTN: RMA #_____
Repair Department
Keithley Instruments, Inc.
28775 Aurora Road
Cleveland, OH 44139

Telephone 1-888-KEITHLEY
FAX (440) 248-6168

NOTES *If you are submitting your equipment for repair under warranty, you must include the invoice number and date of purchase.*

To enable Keithley Instruments, Inc., to respond as quickly as possible, you must include the RMA number on the outside of the package.

2
Installation

Hardware setup

To install a KPCMCIA-12AIAOH PC card, insert the adapter into any type II PCMCIA socket. All other configuration options are determined by the DriverLINX software and operating system, as discussed in your DriverLINX documentation.

Software setup

Refer to your DriverLINX documentation for a detailed description of the software installation procedure.

3
Theory of Operation

Introduction

The KPCMCIA-12AIAOH PC card consists of four differential or eight single-ended analog input channels, each having a bipolar input range of ±0.01V (gain = 1000), ±0.1V (gain = 100), ±1V (gain = 10), or ±10V (gain = 1) with programmable gains of 1, 10, 100, and 1000). The A/D converter, either 12-bit or 16-bit, can be operated at its top speed of 100,000 samples per second (10µs per sample).

The A/D converter uses left-justified 2's complement coding. For the 16-bit version, its output ranges from -32768 to 32767 as usual. However, the 12-bit version has its 12-bit result occupying the most significant 12 bits and pads its least significant four bits with zeroes to make a 16-bit output word for each converted input sample.

The KPCMCIA-12AIAOH PC card can be operated as an I/O device, occupying 16 consecutive bytes in the I/O address space. It can also be configured to operate via memory mapped I/O. It fully complies with the PCMCIA standard 2.1 as a type II card. The card does not have any jumpers or DIP switches; all of its configurable features are programmable.

Functionally, the KPCMCIA-12AIAOH PC card consists of the following components:

- DC/DC power supply
- Analog input multiplexer
- Programmable gain control
- A/D converter
- Data FIFO
- Scan list
- Trigger control
- Pacer clock
- Interrupt and status
- Digital I/O
- D/A circuit
- 16-bit timer/counter circuit
- Associated control circuits

DC/DC power supply

The KPCMCIA-12AIAOH PC card uses a standard 5V power supply for its digital circuit. The ±15V power supplies are used for the analog front end, and the analog +5V power supply is used for the A/D converter. All are generated by a DC/DC converter off of the +5 digital input power supply from the PCMCIA connector. The DC/DC converter takes 140mA, two-thirds of the 210mA total load current, from the input power supply.

According to the new PCMCIA specification, any card that takes more than 100mA must not be blindly turned on when the card is inserted; the card must be intentionally accessed.The KPCMCIA-12AIAOH PC card will support the new specification by providing a unique power-down mode control. When the card is first plugged in, powered up, or reset, the DC/DC converter shuts off so only the digital portion is up and running, taking only 70mA from the input +5 power supply. Full-powered mode can then be activated by software.

Analog input multiplexer

The differential or single-ended configuration is selected via software.The expansion cards can only be used on single-ended channels. The single-ended/differential selection should be the same for all the internal channels (e.g., all four channels as differential, or all eight channels as single-ended). Having some channels configured as single-ended and others as differential, possible as it is, may cause confusion and unexpected signal errors.

In a differential configuration, there are, at most, four channels. However, if you specify channels 4 to 7 in a differential configuration, the inputs to ground for system offset measurement will short. The readings taken under such a circumstance can be used for offset correction.

The input multiplexers have built-in protection against overvoltage when the board is both powered on and powered down. The protection mechanism isolates the input from the rest of the board as long as the input voltage is within the protection range of ±30V.

Programmable gain control

The KPCMCIA-12AIAOH PC card has an internal gain of 1, 10, 100, and 1000. The gain can be changed "on the fly" from channel to channel when scanning through the channels. There is a programmable gain instrumentation amplifier with gains of 1, 10, 100, and 1000. The internal gain selection is specified in the scan list entry via software.

The settling time of the analog front end meets the speed requirement. However, if the amplifier is saturated, it may need a longer time to recover, which may cause distortion in the input signal to the A/D converter. Amplifier saturation should be avoided (use low gains, attenuate the input signal, etc.).

Scan list

One entry to the scan list contains a 16-bit word, or two 8-bit bytes. It specifies the internal channel selection and gain selection (in the high byte, or MSB), the external channel and gain selection (in the low byte, or LSB), and other control and configuration settings.

The external selections are used for channels on the expansion cards, while internal selections are used for channels on the KPCMCIA-12AIAOH PC card.

The expansion cards are not included as part of the KPCMCIA-12AIAOH data acquisition system. However, they can be purchased separately from Keithley.

The number of entries in the scan list ranges from 1 to 2048. No dependencies are implied among the entries of the scan list. You may choose any valid gain combinations for any channel, internal or external. The channels can be scanned in any order as required, repeated or not, with the same or different gain for each entry.

The differential/single-ended control bit (at bit 14, MSB) should be the same for all the entries in the scan list, which is most likely the case for normal operations. Single-ended configurations should be selected if one or more expansion cards are connected to the KPCMCIA-12AIAOH PC card.

The synchronous sample hold bit (or SSH at bit 6, LSB) is reserved for the expansion cards.

Trigger circuit

The KPCMCIA-12AIAOH PC card can be triggered by the software (i.e., an internal trigger), an external TTL input,* the analog input passing through the preset threshold, or the pacer clock. For the TTL or analog trigger, an active trigger edge can be selected for either the low-to-high transition or the high-to-low transition.

In one-shot trigger mode, one trigger, either internal or external, starts one scan of all the channels specified in the scan list. The pacer clock does not have any effect in this mode. Multiple scans can be set up by issuing (or receiving) multiple triggers.

In continuous trigger mode (without pre-trigger), a software, TTL, or analog trigger starts a series of scans in which the first is initiated immediately upon receiving the trigger and the rest occur each time the pacer clock fires. The process continues until the software issues an A/D stop command.

If the internal trigger (or the software trigger) is selected, a trig/arm command from software serves as a trigger as soon as it is received by the PC card. For the external trigger sources (TTL or analog), the same command is taken as an arm command, which arms the PC card so the first proper trigger edge since the reception of the arm command serves as the trigger. Any trigger edges before the first one will be ignored. Unexpected edge transitions during the configuration of the trigger source and edge will not be taken as triggers as long as the PC card is not armed.The pre-trigger option can be selected in continuous mode (not allowed in one-shot mode) with external trigger sources (TTL or analog but not with internal trigger). If the option is selected, the arm command will actually start the pacer clock so the input channels specified in the scan list are scanned each time the pacer clock fires and the scan results are placed in the data FIFO. However, once the almost-full threshold (programmed as an integer multiple of the scan list length) of the data FIFO is reached, the least recent scan is automatically discarded and the most recent one is placed in the data FIFO. This filling and discarding continues until the external trigger (TTL or analog) activates. At that point, no more discarding will be performed, and the normal data acquisition process starts with half FIFO full of data samples right before the trigger. A/D event bits are not set until the trigger activates, guaranteeing that no interrupts can be sent before the trigger eventually activates.

**NOTE* *In "Paced" mode, the same input pin is shared between external clock and external trigger, hence only one function can be used (not both simultaneously).*

A/D converter and data FIFO

The KPCMCIA-12AIAOH PC card always assumes a bipolar input range of ±10V if the gain is one. The output data format will always be in 2's complement (and left justified for 12-bit versions). The data acquisition time of the A/D converter is 2µs, while its conversion time is no more than 8µs. The A/D converter output is fed into the data FIFO providing data buffering of 2048 samples.

The hardware design guarantees that the A/D converter, once triggered, will perform a conversion for every analog input channel specified in the scan list at the selected scan speed and feed the results into the data FIFO. In between scans, the PC card waits until another trigger activates (one-shot mode) or the pacer clock fires (continuous mode).

The data FIFO has two programmable thresholds: one for almost full and the other for almost empty. The KPCMCIA-12AIAOH PC card only uses the almost-full threshold and ignores the other. Upon power up or reset, the almost-full threshold is defaulted to 7 bytes to full (3.5 samples).

When the FIFO is full, no more samples can be written into the FIFO. At the end of each scan, the KPCMCIA-12AIAOH PC card sets a data-lost flag if the data FIFO is already full.

Interrupt and status

The KPCMCIA-12AIAOH PC card has three interrupt sources: the end-of-scan (EOS) interrupt, the FIFO threshold interrupt, and the timer interrupt. These interrupts are used as follows:

- When the EOS interrupt is enabled, an interrupt is sent to the host at the end of each scan of the channel list. If only one channel is in the scan list, the EOS interrupt is reduced to an EOC (end-of-conversion) interrupt.
- The FIFO threshold interrupt, when enabled, is sent to the host when an almost-full flag is set by the card. The host can then use the string input instruction to move a block of samples from the FIFO.
- When the timer interrupt is enabled, an interrupt is sent to the host each time the timer overflows.

Digital I/O

The KPCMCIA-12AIAOH PC card has one digital input port (base + 3, read only) of four bits (bits 0 to 3) and one digital output port (base + 3, write only) of four output bits (bits 0 to 3). The output port is latched, but the input port is not.

Four input lines are connected to the digital input port; each represents one bit in the port. When reading the digital input port, the current status of the digital input lines are returned to the host.

All four input lines are shared with other functions. Bit 0 is shared as the external trigger and external paced clock input. Bit 2 is shared as the external clock burst input. Bits 1 and 3 are taken over as the external gain selection lines if one or more expansion cards are connected and an expansion bit is set by software. However, the current status of the digital input lines is always returned when the host reads the digital input port, whether the lines are shared or not.

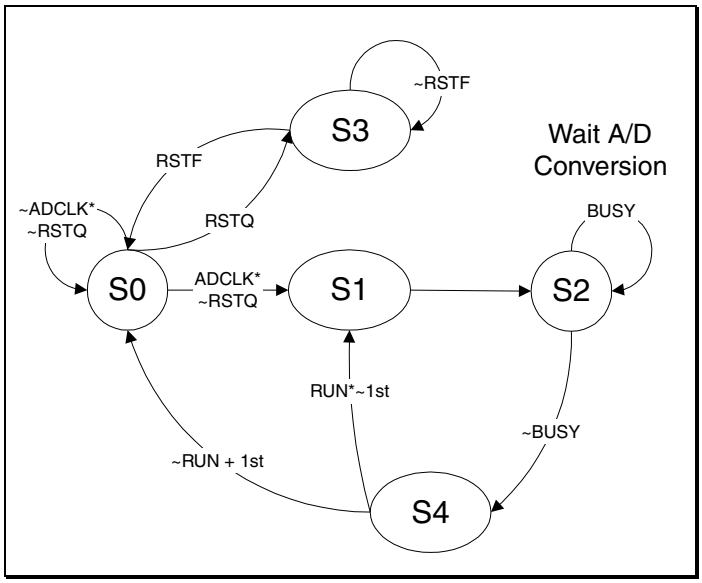
The four digital output lines are taken over as the external channel selection lines if an expansion bit is set by software. In this case, the digital output lines are driven by the external channel selection bits of the current scan list entry. Otherwise, they are connected to the latched bits 0 through 3 of the digital output port.

A/D state machine

The KPCMCIA-12AIAOH PC card has an internal state machine (see Figure 3-1) that controls A/D operation.

The state machine defaults to state S0 after power up or reset. The normal state flow is first S0 to S3, initiated by a scan list (queue) flush command (RSTQ). Then, the queue is programmed.The state machine then moves from S3 back to S0. The S3 to S0 step is initiated by issuing a flush-data FIFO command (RSTF)—which sets up the gain and channel selections for the first channel in the scan list—and then waiting for a trigger to start the scan. When the trigger (ADCLK) activates, the state machine moves from S0 to S1, and the A/D conversion starts once it is moved to S1. The state machine waits at S2 until the conversion is done. At this time, it moves to S4, where the A/D conversion result is written into the data FIFO. The scan rate is determined by the time the state machine moves from S1 to S4, which can be set to 10µs, 20µs, or 40µs. If there are more channels to scan in the list, the state machine will skip to S1 for another conversion loop. Otherwise it will return to S0 and wait for another trigger (or a sampling pulse from the pacer clock if it is in the continuous trigger mode). At any time during data acquisition, an A/D stop command will clear RUN to zero and eventually stop the data acquisition by moving the state machine back to S0.

Figure 3-1
State transition diagram of A/D conversion process



The sequence of the first trip of S0-S3-S0, as previously described, is important. Software issues two commands to the PC card: the flush scan list command (RSTQ) and then the flush data FIFO command (RSTF). In between, the scan list is programmed. Once the flush data FIFO command is issued, the PC card prepares the first channel in the scan list, and then goes back to state S0 waiting for the first trigger.This guarantees that the scan list and the data FIFO are flushed properly for the expected data acquisition.

D/A circuit

The KPCMCIA-12AIAOH PC card is equipped with two D/A channels. The 12-bit serial D/A converter (AD7249 from analog device) supports synchronous update. It is configured to have a bipolar output range from -5 to +5V. The 12-bit output data format is always in 2's complement (right justified) with the upper four bits indicating the output channel number (binary 0000 for channel 0 and 0001 for channel 1). The D/A data port occupies two bytes (write only) in the I/O space.

The serial link from the D/A port to the D/A converter contains a 16-bit buffer register and a 16-bit shift register. A data word written into the D/A port is written into the buffer register, loaded into the shift register, and sent to the input register of the corresponding D/A channel (inside the D/A converter AD7249).

Inside the D/A converter, each channel also has a 16-bit shift register, a 12-bit input register, and a 12-bit output register. The data loaded into the output register determines the analog output of the D/A channel.

The KPCMCIA-12AIAOH PC card has four D/A operation modes (modes 0 to 3). Mode 0 is the direct update mode. The corresponding D/A channel output register updates immediately after the data word is written into the D/A port (if byte I/O is used, after the high byte is written). There is no synchronization between the two channels in this mode.

Modes 1, 2, and 3 are all using synchronized update, in which the two D/A channels are updated at the same time (synchronously) for certain events. In mode 1, the event is the timer overflow. In mode 2, it is the external gate control (going from low to high). In mode 3, the event comes from the pacer clock.

In the synchronous update modes, the data word written to each D/A channel is buffered in its input register (inside the AD7249) first and then loaded into the output register (and therefore the D/A output gets updated) when the corresponding event (depending on the mode) is received.

Synchronous update modes can be used to generate waveforms with accurate phase requirements, such as orthogonal, sinusoidal waveforms (sine and cosine).

Timer counter

In addition to the 24-bit pacer clock, the KPCMCIA-12AIAOH PC card is equipped with an independent 16-bit timer/counter. The timer/counter has an internal clock source of 1MHz and an external clock input (for counting or as an external clock source, shared with the pacer clock external input).

The timer circuit contains a 16-bit reload register, a 16-bit up-counter, and a 16-bit read-latch register. The reload register holds the initial value for the counter. The counter is also loaded with the same value each time it overflows. The read-latch register latches the current count of the counter each time it receives a latch command. The integrity of the latched count is guaranteed by the logic design.

The 16-bit reload register is accessed when writing into the port, while the read-latch register is accessed when reading the port. The up-counter cannot be accessed directly.

Either the 1MHz internal clock source or the external clock source (or the counter pulse input) is software selectable. Because of the I/O pin confinement, the timer external clock input is shared with pacer clock external input (also shared as the digital input bit 2).

There are four timer/counter modes: 0, 1, 2, and 3. In mode 0, the counter stops and reloads with the initial value by the rising edge of the selected clock source. In mode 1, the counter pauses counting but does not reload (as it does in mode 0). Mode 2 is the counting mode in which the counter counts up the rising edge of the selected clock source. In mode 3, the counter is controlled by the external gate (shared with D/A) signal. The counting proceeds when the signal is high and pauses when the signal is low.

Three I/O pins are associated with the timer: the external clock source input (shared with the pacer clock), external gate control (shared with D/A), and the timer overflow pulse output (TTL), which goes high when the timer reaches its final count (hexadecimal FFFF).

The reload register can be set up for both counting and timing operations. The value written into the reload register, denoted as X for the sake of the discussion, determines the divisor or modulus for timing and counting. Since the final count before reloading is always 65535 (hexadecimal FFFF) for the up-counter, the reload (initial) value determines from where the counting will start. Therefore, 65536 - X will be the divisor for timing operations or the modulus for counting operations. For example, a divided-by-2 timer (or modulus 2 counter) can be configured by setting X equal to 65534, while X = 0 implies the divisor is 65536 (or the modulus is 65536).

Avoid X = 65535 (hexadecimal FFFF) because the timer will be stuck at the final count and the hardware will not reject or indicate such a setting.

Changing the reload register "on the fly" is allowed, but the setting will not take effect until the up-counter reaches its final count (65535 or hexadecimal FFFF). The next clock rising edge will load the counter with the new setting.

The timer interrupt is enabled and disabled by software. When enabled, an interrupt is sent each time the up-counter overflows (passes through its final count).

4
I/O Connections

Introduction

The KPCMCIA-12AIAOH PC card is fitted in with a 32-pin, 0.8mm shielded connector with the pin assignment shown in Table 4-1.

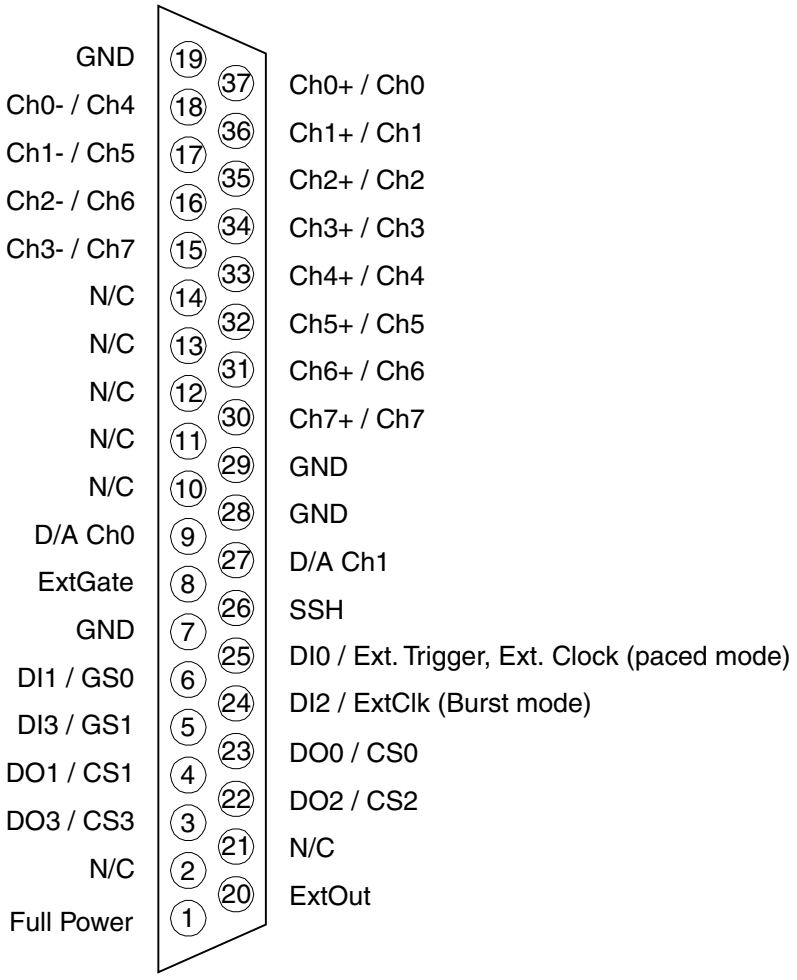
Cable assembly

Table 4-1
KPCMCIA-12AIAOH PC card cable mapping

PC Card 32 pin connector	D-37 pin connector	Name		Description
32	37	Channel 0 (+)	Channel 0	A/D input, differential/single-ended
31	18,33	Channel 0 (-)	Channel 4	A/D input, differential/single-ended
30	36	Channel 1 (+)	Channel 1	A/D input, differential/single-ended
29	17,32	Channel 1 (-)	Channel 5	A/D input, differential/single-ended
28	35	Channel 2 (+)	Channel 2	A/D input, differential/single-ended
27	16,31	Channel 2 (-)	Channel 6	A/D input, differential/single-ended
26	34	Channel 3 (+)	Channel 3	A/D input, differential/single-ended
25	15,30	Channel 3 (-)	Channel 7	A/D input, differential/single-ended
24	19	GND		Signal ground (analog input)
23	9	DA0		D/A channel 0 output
22	27	DA1		D/A channel 1 output
20	7	GND		Power supply ground return
19	24	ExtClk (shared with A/D)		Timer/Counter external clock input
18	8	ExtGate		Timer/Counter external gate control
17	11	ExtOut		Timer/Counter overflow pulse output
16	7	GND		Power supply ground return
15	1	FullPower (org. D/A 0 ref. in)		1/0 : Full power/Power down
14	26	SSH (org. D/A 1 ref. in)		Synchronous sample hold
13	25	Digital in bit 0 (shared)		External trigger (same as in DAS-16)
12	6	Digital in bit 1 (normal mode)		External gain, LSB (expansion mode)
11	24	Digital in bit 2 (shared)		External clock (org. DAS-16 Ctr 0 Gate)
10	5	Digital in bit 3 (normal mode)		External gain, MSB (expansion mode)
9	23	Digital out bit 0 (normal mode)		External channel bit 0 (expansion mode)
8	4	Digital out bit 1 (normal mode)		External channel bit 1 (expansion mode)
7	22	Digital out bit 2 (normal mode)		External channel bit 2 (expansion mode)
6	3	Digital out bit 3 (normal mode)		External channel bit 3 (expansion mode)
5	28	GND		Signal ground (D/A output)
4	28	GND		Signal ground (D/A output)
3	29	GND		Signal ground (digital)
2	29	GND		Signal ground (digital)
1	N/C	Reserved		

Note that the cable assembly for the KPCMCIA-12AIAOH PC card (KCAB-AIAO) in Figure 4-1 looks very similar to the one for the KPCMCIA-12AI/16AI and KPCMCIA-12AIH PC cards (KCAB-AI). Do not mistake one for the other; severe damage to the PC cards may occur. The cable assembly for the KPCMCIA-12AIAOH PC cards have the name KCAB-AIAO on its 37-pin D-shell connector. If the cable is not identified as such, do not use it with the KPCMCIA-12AIAOH PC cards.

Figure 4-1
KPCMCIA-12AIAOH PC card D-37 output connector, KCAB-AIAO



5
Optional Accessories

The following optional accessories are available from Keithley:

- STP-37
- STA-U
- EXP-1600

A
Specifications

A/D converter	**12-bit version**	**16-bit version**
Acquisition + Conversion	2µs + 8µs	2µs + 8µs
Monotonicity	No missing codes	No missing codes
Integral linearity error	±1 LSB	±3 LSB
Differential linearity error	±1 LSB	+3/-2 LSB
Full-scale error	±0.5%	±0.5%
Aperture delay	40ns	40ns

Analog input	
Number of input channels	Four differential/eight single-ended; expandable to 128
Input range	±10, ±1, ±0.1, and ±0.01V
Programmable gain	1, 10, 100,1000
Maximum overvoltage	±30V
Input impedance	100MΩ (DC)

A/D miscellaneous specifications	
Data FIFO depth	2048 samples
Scan list length	2048 entries
Scan speed	10µs, 20µs, 40µs
Trigger source	Internal (software)/external (TTL, analog)
Trigger mode	Continuous/one-shot
Pre-trigger option	Programmable, up to the data FIFO depth
TTL trigger	0.8V (low) / 2.2V (high), rising/falling edges
Analog trigger	Threshold set in full A/D input range (±10V) Rising/falling directions, 10mV hysteresis
Sampling rate	0.006Hz to 100kHz (with internal clock source)
External clock rate*	DC - 5MHz

**NOTE* *In "Paced" mode, the same input pin is shared between external clock and external trigger, hence only one function can be used (not both simultaneously).*

D/A converter	
Resolution	12-bit
Relative accuracy	±1 LSB
Bipolar zero error	±7 LSB max
Differential nonlinearity	±1 LSB max
Full scale error	±7 LSB max

Analog output	
Number of output channels	2 (single-ended only)
Output settling time	10µs
Output range	±5V (bipolar only)
Output current	±2mA
DC output impedance	0.5Ω (typical)

Timer/counter	
Word length	16-bit, with auto reload and read latch
Clock source	Internal (1MHz) / External (DC - 5MHz)
External clock input	TTL, pulse width > 100ns, frequency < 5MHz
Overflow output	TTL
Divisor/modulus range	2 - 65535

Digital I/O	
Digital input channels	4 (no latch)
Digital output channels	4 (latched)
Maximum source current	0.5mA
Maximum sinking current	2.5mA
Minimum logic 1 level	2.4V
Maximum logic 0 level	0.8V

General specifications

Power consumption	210mA (full power), 70mA (power down)
Operating temperature	0° to 50°C
Storage temperature	0° to 70°C
Humidity	0 to 95%, non-condensing
Size (cable not included)	Standard PCMCIA type II
Weight	1.5 oz (for reference only)

Specifications subject to change without notice.

B

PCMCIA Interface

NOTE *A typical user of this manual does not need to read the material in this section. If you write a custom program, write it to work through DriverLINX, using the many interface and support features of DriverLINX. Register-level programming of the card is not recommended. This section is provided only for an advanced programmer who must write a specialized driver.*

Introduction

Information in this section is provided for those who need low-level PCMCIA interface details of the KPCMCIA-12AIAOH PC card. The client driver or the enabler that comes with the PC card is sufficient for most applications.

The KPCMCIA-12AIAOH PC card performs data acquisition for all host computers equipped with a version 2.1 compliant PCMCIA interface. The PC card, which is the name given to all PCMCIA interface cards, has a form factor of type II (5mm thick).

Due to the PCMCIA interface, the PC card is highly flexible with respect to addressing and interrupt level use. It can be configured either as a memory only interface or as an I/O interface and can be powered up or down with the help of the PCMCIA card and socket services software. The KPCMCIA-12AIAOH PC card provides a single interrupt that is routable to any system interrupt via the PCMCIA socket controller.

Two sets of registers are on the KPCMCIA-12AIAOH PC card: the configuration registers and program registers.

The configuration registers are those defined in the PCMCIA 2.1 specification. The PCMCIA configuration registers are located in the PC card's configuration space at offset 8000H. Configuration space also contains the Card Information Structure (CIS). This memory is located at offset 0000H in the configuration space. The CIS memory contains information about the PC card as defined by the PCMCIA 2.1 specification. The configuration and power-up/down control of the PC card should be carried out through the standard card and socket services software even though they can be achieved with an enabler.

Program registers are the registers that fall under program control and belong to the KPCMCIA-12AIAOH PC card. The I/O location of these registers are controlled by the PCMCIA socket configuration and by the contents of the PCMCIA configuration registers. See the descriptions in Appendix C for more information.

Two PCMCIA configuration registers are supported by the KPCMCIA-12AIAOH PC card: the configuration option register and the card configuration and status register. Refer to Table B-1.

Table B-1
PCMCIA configuration registers

Offset	Access	Description
0x8000	R/W	Configuration option register
0x8002	R/W	Card configuration and status register

Configuration and option register (COR)

Refer to Table B-2. Bits 6 and 7 of the configuration option register are defined by the PCMCIA standard as the SRESET and the LevlREQ Bits. A 1 written into the SRESET bit puts the card into a reset state, while a 0 moves it out of the reset state. When the card is in a reset state, it behaves as if a hardware reset is received from the host. The LevlREQ bit controls the type of interrupt signal generated by the PC card. Setting the configuration index bits to 0 makes the PC card a memory-only card (accessed only by memory read/write operations), while setting it to 1 enables the card to be a standard I/O card.

Table B-2
COR bit definitions

Bit	Name	Description
7	SRESET	1 = Put the card into a reset state 0 = Get out of a reset state
6	LevlReq	1 = Level mode interrupt 0 = Edge mode interrupt
5-0	Index bits	000000 = Memory mode 000001 = I/O mode

Card configuration and status register (CCSR)

Refer to Table B-3. The KPCMCIA-12AIAOH PC card uses two bits in this register. When bit 1 is set to 1, it indicates a pending interrupt. The bit will remain as 1 until the software clears the interrupt source. Bit 2 is used for power-down control. A 1 set to this bit puts the card into power-down mode, while a 0 brings it back to full-powered mode. The rest of the bits are not used.

Table B-3
CCSR bit definitions

Bit	Name	Description
7-3	Not used	Reserved, all 0 when writing and reading
2	PwrDwn	1 = Power-down mode 0 = Full-powered mode
1	Intr	1 = Interrupt pending 0 = No interrupt pending
0	Reserved	Reserved as 0

C
I/O Registers

NOTE *A typical user of this manual does not need to read the material in this section. If you write a custom program, write it to work through DriverLINX, using the many interface and support features of DriverLINX. Register-level programming of the card is not recommended. This section is provided only for an advanced programmer who must write a specialized driver.*

Introduction

The KPCMCIA-12AIAOH PC card uses eight consecutive I/O locations within the system I/O address space. The base address of the adapter is determined by the client driver or enabler. The eight I/O locations used by the PC card are summarized in Table C-1.

The D/A port and timer port registers can be accessed as 16-bit I/O registers. They can also be accessed with 8-bit I/O instructions. The remaining registers are 8-bit wide. Each entry in Table C-1 is discussed in detail in the following paragraphs.

Table C-1
KPCMCIA-12AIAOH PC card register map

Address lines (A3A2A1A0)	I/O address	Port access	Register description
0000	base + 0	Read/Write	Data FIFO
0001	base + 1	Write Only	Scan list queue
0010	base + 2	Write Read	Control register Status register
0011	base + 3	Write Read	Digital output register Digital input register
0100	base + 4	Write Only	Pacer clock, low byte
0101	base + 5	Write Only	Pacer clock, middle byte
0110	base + 6	Write Only	Pacer clock, high byte
0111	base + 7	Write Only	Command register
1000-1001	base + 8,9	Write Only	D/A port
1010-1011	base + 10,11	Write Read	Timer port (reload) Timer port (read latch)
1100-1110	base + 12,13,14		Reserved
1111	base + 15	Write Read	Auxiliary control reg. Auxiliary status reg.

Data FIFO register (base + 0)

The data FIFO register can be considered the access port to the data FIFO, which can hold up to 2048 data words of the A/D conversion result. The port is also used to program the data FIFO thresholds.

Two consecutive bytes should be read from (written into) the port each time it is accessed. Table C-2 illustrates the bit allocation.

NOTE *Although the data FIFO register is 8-bit wide, accessing the register as a 16-bit word guarantees the integrity. The low byte (LSB, or the least significant byte) should always be accessed first, followed by the high byte (MSB, or the most significant byte).*

Table C-2
Data FIFO register bit allocation

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LSB	D7	D6	D5	D4	D3	D2	D1	D0
MSB	D15	D14	D13	D12	D11	D10	D9	D8

Data FIFO operation modes

Depending on the mode of operation, the 16-bit word read from or written into the register has different meanings, as described in Table C-3.

Table C-3
Data FIFO operation mode

Mode	Selection bit	A/D	Access	Operation
0	0, threshold	Idle	Read Write	Verify data FIFO threshold Program data FIFO threshold
1	1, data FIFO	Idle	Read Write	Read data FIFO Write data FIFO (diagnosis)
2	0, threshold	Run	Read Write	Verify data FIFO threshold Not allowed
3	1, data FIFO	Run	Read Write	Read data FIFO Not allowed

The selection bit in Table C-3 is also called the program/access control bit as defined in the command register (base + 7). Refer to "Command Register (base + 7, write only)" for details on setting the bit and issuing commands to change the status of the A/D conversion (from scan to idle or vice versa).

Mode 0 is the FIFO program mode in which the two consecutive words (four bytes) written into the register address will set the almost-full and almost-empty thresholds (in bytes). The first word specifies the almost-empty threshold (not used; can be set to anything), while the second word determines the almost-full threshold. The threshold should be set to a value from 1 to FIFO size minus 1 (default is 7 when reset or powered up). Refer to Table C-4.

Table C-4
Data FIFO threshold setting

Threshold	Default	Threshold range	Suggested value
Almost Empty	7	Irrelevant	Irrelevant
Almost Full	7	1..4095 bytes*	2048 bytes*

* 2 bytes per sample/data word

Mode 1 is the FIFO test mode in which the data bytes can be written into the data FIFO and read back from it. The FIFO flags (FIFO empty, almost-full, and full flags) will change according to the data bytes available in the data FIFO and the configured threshold.

Mode 2 should be avoided. The data bytes cannot be written into the FIFO under this mode, while the bytes read from the FIFO will be the same as in mode 0.

Mode 3 is the data transfer mode. Data bytes will be written into the FIFO by the A/D converter, while the data byte read from the address is the first available byte in the data FIFO if it is not empty. Otherwise, the most recent byte written into the FIFO will be returned. The data FIFO register is read-only under this mode. You cannot write data bytes into the data FIFO through I/O instructions.

Mode setting

The FIFO operation mode setting is always initiated by the data FIFO flush command with the access/program bit set to 0 (bit 0 at base + 7) before the data acquisition is started. See "Command Register (base + 7, write only)." This will bring it to mode 0 (threshold setting mode). After the threshold is programmed or verified, set the bit to 1 so the consequent read/write operations to the FIFO will be taken as data access operations.

The A/D circuit is in idle mode before starting into the run mode by a trigger command (or an arm command with pre-trigger). For one-shot operation, the A/D circuit will be set to run mode after it receives the trigger signal. It will not return to the idle mode until the specified scan list is completed or an A/D stop command is received. See "Command register (base + 7, write only)." For continuous trigger operation, the A/D circuit will stay in run mode after being triggered (or armed with the pre-trigger option) until an A/D stop command is received.

FIFO flags

When reading the register under mode 1 or 3, the first available data byte from the data FIFO will be returned if it is not empty. Otherwise, the returned byte is not defined. The FIFO empty flag will be set immediately after the last byte is read from the FIFO, while the FIFO full flag will be cleared after reading the data FIFO register provided no more data bytes are written into the FIFO by the A/D converter under mode 1 or 3. The same happens to the FIFO almost full flag, if the data bytes available in the FIFO are less than the almost full threshold. Refer to Table C-5.

Table C-5
Data FIFO flag status

Data bytes in FIFO	Empty	Almost full	Full
0	True	False	False
1 to (Threshold - 1)	False	False	False
Threshold to (FIFO size - 1)	False	True	False
FIFO size (4096 bytes*)	False	True	True

*Note: Threshold is the almost-full threshold, and FIFO size is measured in bytes, 4096 (2048 samples/data words).

Scan list queue register (base + 1, write only)

The scan list queue register can be considered the access port to the scan list queue, which can hold up to 2048 entries (each has two bytes), each specifying an analog input channel and its associated gain as well as other settings. The bit definition of an entry to the scan list queue is explained in Table C-6.

NOTE *Although the scan list queue register is 8-bit wide, it is required that the register be accessed as a 16-bit word to guarantee its integrity. The low byte (LSB, or the least significant byte) should always be accessed first followed by the high byte (MSB, or the most significant byte).*

Table C-6
Scan list queue entry bit definitions

Bit	Byte	Definition	Explanation
15	MSB	Reserved	As 0
14	MSB	Analog input mode	1/0 : differential/single-ended
13-12	MSB	Internal gain selection	00/01/10/11 : 1/10/100/1000
11	MSB	Not in use	Don't care
10-8	MSB	Internal channel selection	000..111 : channel 0..7
7	LSB	Starting channel mark	Set to 1 for the first entry in the list. Set to 0 for all the rest entries.
6	LSB	Reserved	For expansion cards (as SSH)
5-4	LSB	External gain selection	00/01/10/11 : 1/2/4/8 (or 1/10/100/1000)
3-0	LSB	External channel selection	0000..1111 : channel 0..15

Scan list queue programming

The scan list queue has to be programmed when the A/D circuit is idle. Each queue entry contains two bytes as previously described. The integrity of the entry has to be guaranteed. The scan list queue is write only.

The scan list queue should be flushed before writing any entries into it. Refer to "Command register (base + 7, write only)" for information about the scan list queue flush command.

The first entry of the queue should have bit 7 (LSB) set to 1 as the first channel mark. All other entries, if any, should normally have the bit set to 0.

The synchronous sample hold bit (LSB) is not used by the PC card. It is reserved for the expansion cards that supports simultaneous sample-hold.

Example 1

Refer to Table C-7. The following entries to the queue specify a scan list of three single-ended internal channels: 0, 12, and 7. Channel 0 has a gain of 10, and channels 12 and 7 have a gain of 100.

Table C-7
Scan list queue programming example 1

Entry	Binary	Hex	Explanation
1	0001 0000 1000 0000	0180	Select channel 0, gain 10, first entry
2	0010 1100 0000 0000	2C00	Select channel 12, gain 100
3	0010 0111 0000 0000	2700	Select channel 7, gain 100

Example 2

Refer to Table C-8. The following entries to the queue specify a scan list of four differential internal channels: 2, 1, 6, and 7. Each channel has a gain of 1.

Table C-8
Scan list queue programming example 2

Entry	Binary	Hex	Explanation
1	0100 0010 1000 0000	4280	Select channel 2, gain 1, first entry
2	0100 0001 0000 0000	4100	Select channel 1, gain 1
3	0100 0110 0000 0000	4600	Select channel 6, gain 1
4	0100 0111 0000 0000	4700	Select channel 7, gain 1

Channel configuration

Bits 4 and 5 (LSB) in a queue entry specify the gain on the external expansion card for the external channel selected by bits 3 through 0 of the same byte. Each expansion card has up to 16 channels (0, 1, 2, ... 15). Each channel may have up to four gain options: 1, 2, 4, or 8 if it is a low gain expansion card. 1, 10, 100, or 1000 if it is a high gain expansion card.

If there is no expansion card for the specified internal channel, the external channel and gain selection in the LSB will be ignored. However, the first channel mark on bit 7 should always be set properly.

The internal channel is selected by bits 8 through 11 (MSB), while the internal gain for the selected channel is specified by bits 12 and 13 (MSB). The internal gain can only be 1, 10, 100, or 1000.

Bit 14 (MSB) determines whether the input is differential (1) or single-ended (0). There are 16 singled-ended channels but only eight differential channels. This bit should always be set to 0 if the selected internal channel is connected to an expansion card because the output from the expansion cards is always single-ended.

Bit 15 (MSB) is not used by the KPCMCIA-12AIAOH PC card. It should be set to 0.

Analog input offset correction

The input to the A/D converter will be shorted to ground if bit 14 (MSB) is set to 1 while the internal channel selection of bits 8 through 10 specifies internal channels 4 through 7. (Bit 11 is not used and therefore should be considered as "don't care.") This can be used for analog input offset correction.

Control register (base + 2, write only)

The control register specifies the pacer clock source and pre-scaler, the expansion mode, A/D interrupt enable control, and part of the A/D trigger control. The bits are explained in Table C-9.

Table C-9
Control register bit definitions

Bit	Function	Explanation
7-6	Pacer clock source and pre-scaler	00 : External clock 01 : Internal, 5MHz 10 : Internal, 1MHz 11 : Internal, 100kHz
5	Expansion mode	0/1 : disable/enable
4	EOS interrupt	0/1 : disable/enable
3	FIFO interrupt	0/1 : disable/enable
2	Trigger mode	0/1 : one-shot/continuous
1	Trigger source	0/1 : internal/external
0	Trigger edge	0/1 : rising/falling

Clock source

The external clock source, if selected, must not exceed 5MHz with a minimum pulse width greater than 100ns. The external clock frequency can be as low as DC, and there is no limit on the maximum pulse width.

Expansion mode

Bit 5 has to be set to 1 if there is one (or more) expansion card(s) connected to the KPCMCIA-12AIAOH PC card. This setting also indicates that all digital output lines (bits 0 to 3) will be used for external channel selection and two of the four digital input lines (bits 1 and 3) will be used for external gain selection.

A/D interrupt enable

Bits 3 and 4 are used for the A/D interrupt enable control. The EOS (end-of-scan) interrupt is enabled (disabled) by setting bit 4 to 1 (0). Setting bit 3 to 1 (0) enables (disables) the data FIFO interrupt when the A/D data FIFO becomes almost full. (Data available in the FIFO reaches the almost-full threshold.) Since the EOS and FIFO threshold events are latched into the status register, temporarily disabling the interrupt and then enabling it will not lose an interrupt as long as no events are repeated during the time the interrupt is disabled.

Trigger mode

Bit 2 determines the trigger mode. It is set to 0 for the one-shot mode in which each trigger signal, internal or external, starts one scan of input analog channels specified by the scan list. Bit 2 should be set to 1 for the continuous trigger mode in which the trigger signal, internal or external, starts the first scan of the input analog channels specified by the scan list.The pacer clock then initiates the subsequent scans each time it fires until the stop A/D command is received.

Trigger source

Bit 1 specifies the trigger source. It is set to 1 for external trigger (either TTL or analog trigger depending on the setting of bit 7 in the auxiliary control register at base + 15) and 0 for internal trigger (software trigger). When it is set to internal trigger, the trigger edge selection can be ignored. The external trigger signal shares the same pin on the interface connector with the digital input bit 0.

To use the external trigger, TTL or analog, bit 1 in the control register must be set to 1. The setting of bit 7 in the auxiliary control register determines whether it is TTL (bit 7 is 0) or analog (bit 7 is 1). If the internal trigger was selected by setting bit 1 to 0 in the control register, setting bit 7 in the auxiliary control register would be irrelevant.

Trigger edge

Bit 0 selects the external trigger edge. The falling edge of the external trigger signal is chosen as the trigger edge if the bit is set to 1. Otherwise, the rising edge is selected. The edge selection will be ignored if the internal trigger source is specified.

For the analog trigger, the falling edge corresponds to a selected analog channel input signal falling through the configured trigger threshold (from above it to below it), while the rising edge means the opposite.

Analog trigger threshold

The analog trigger threshold can be set only by the output of D/A channel 1 with an equivalent range from -10 to +10V (full A/D converter input range). The threshold level is set against the A/D converter input (after the programmable gain amplifier)—not the one at the input connector (before the PGA). The following formula can be used to convert the code value C (-2048 to 2047) written into D/A channel 1 to the trigger level set against the analog input voltage U for the selected A/D input channel (measured at the input connector of the PC card):

$$U = (C/2048) \times (10/G)$$

where U is in volts and G is the (internal) gain of the selected analog input channel. In case an expansion card is involved, the threshold can be further calculated by converting the U obtained above with the transfer function of the expansion card.

A fixed hysteresis of about 10mV in the analog comparator circuit is used to generate the analog trigger. The accuracy of the analog trigger level is typically 1% of the A/D input range (±10V), or within ±0.1V.

The selected analog input channel will always be the one specified as the first entry of the scan list queue (first channel mark set to 1). However, this is not the case with the pre-trigger option.

Take care when using the analog trigger with the pre-trigger option. After receiving the arm command, the A/D converter is already scanning the analog input channels specified in the scan list. The analog comparator generates the analog trigger any time its input passes through the threshold. For example, if one of the input channels specified in the scan list is below the threshold while another is above it, the trigger will be generated because the input to the analog comparator will definitely pass through the threshold in either direction during the channel scanning. The following conditions must both be met to use the analog trigger with pre-trigger option selected:

- All the input channels specified in the scan list must be either all below or all above the analog trigger threshold before the trigger event comes.
- When the trigger event comes, either one of the input channels passes across the threshold in the right direction or one of the input channel passes the threshold (not necessarily in the right direction) and at least one channel stays on the original side.

Status register (base + 2, read only)

The status register is read only. It shares the same offset as the control register. It reports data FIFO flag status, A/D interrupt status, and A/D conversion status. The status register bits are explained in Table C-10.

Table C-10
Status register bit definitions

Bit	Status	Explanation
7	In-scan status	0/1 : yes / no
6	A/D running status	0/1 : no / yes
5	Data lost event	0/1 : no / yes
4	End of scan event	0/1 : no / yes
3	FIFO threshold event	0/1 : no / yes
2	Data FIFO full	0/1 : false / true
1	Data FIFO almost full	0/1 : false / true
0	Data FIFO empty	0/1 : false / true

Bit 7 is actually the inverse of the in-scan flag. It is 0 when the PC card is in the process of scanning the input channels specified by the scan list and 1 when it is finished.

Bit 6 is the A/D running flag. A 1 here indicates that the A/D is busy doing the data acquisition, while a 0 means it is (idle). If the pre-trigger is selected, this bit will be set as soon as the arm command is received. However, this bit will only be set after a trigger has been received if the pre-trigger is not selected.

Bits 3, 4, and 5 are the event latches. When an event is detected, the corresponding bit will be set to 1 until the status register is read, which clears all the event bits to 0. Bit 5 is used for data lost event, bit 4 for EOS (end-of-scan), and bit 3 for the FIFO threshold event. When the corresponding interrupt is enabled, a 1 in bit 3 (or bit 4) will also cause an interrupt. Bits 0, 1, and 2 are the data FIFO flags.

Each time the status register is read, the latched events (bits 3, 4 and 5) will clear. This setup may also cause the loss of events. (The read action might overwrite the event setting and lose the corresponding event). This is very critical in a tight "check-and-wait" loop where the status register is read and checked for the expected events to occur. The intensive reading in the tight loop greatly increases the possibility of losing the events.

The clear-after-read nature of the status register is what causes the conflicts. To keep the compatibility with the DAQP series PC cards, this configuration is not changed in the KPCMCIA-12AIAOH PC card. However, the newly added auxiliary status register has two bits allocated for these events. Since the auxiliary status register does not have this clear-after-read nature, the conflicts may be avoided by referencing the auxiliary status register instead.

Digital output register (base + 3, write only)

The four digital output lines share the same pins on the interface connector with the four external channel selection bits. When using the expansion cards, bit 5 of the control register (base + 2) should be set to 1, so the external channel selection bits from the scan FIFO drive the four lines. The values in bits 0 to 3 latched during the last write operation drive the four lines if bit 5 of the control register is set to 0 (default after reset). In other words, the digital output bits are only valid when KPCMCIA-12AIAOH PC card is not in expansion mode. These bits are ignored otherwise. For digital output register bit definitions, refer to Table C-11.

Table C-11
Digital output register bit definitions

Bits	Normal mode	Expansion mode
0-3	Digital output bits 0 to 3	Ignored, the four output lines will be driven by the external channel selection bits in the scan list FIFO.
4-7	Reserved as all 0	Ignored.

Digital input register (base + 3, read only)

As mentioned before, two of the digital input lines are shared with external trigger (bit 0) and external clock (bit 2). The other two lines are also used for external gain control in the expansion mode. If bit 2 of the control register is set to 1, refer to "Control register (base + 2, write only)." The digital input lines are not latched. Table C-12 shows what will be returned when reading this port.

Although the digital input lines are also used as external trigger, external clock, and the external gain selection, the current status of these lines is always returned when reading the port. However, the line status has nothing to do with the digital output register whose contents cannot be read back directly even though they share the same port offset with the digital input register.

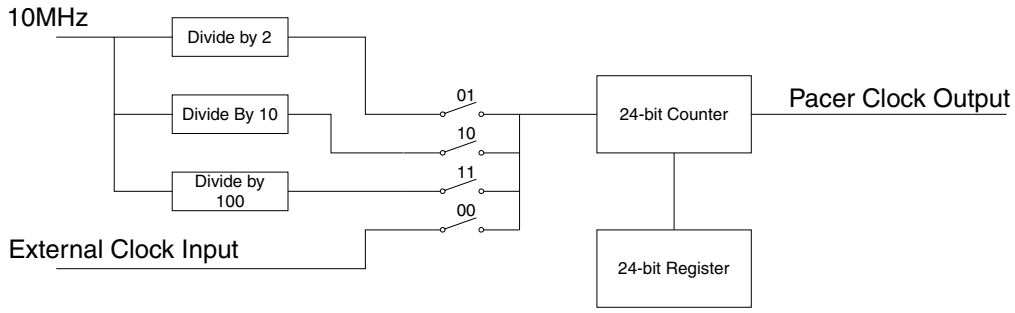
Table C-12
Digital input register bit definitions

Bits	Normal mode	Expansion mode
0	Digital input bit 0, also serve as external trigger	The same as in normal mode
1	Digital input bit 1	External gain select, low bit
2	Digital input bit 2, also serve as external clock	The same as in normal mode
3	Digital input bit 3	External gain select, high bit
4-7	All 0	All 0

Pacer clock (base + 4, + 5, + 6; write only)

The pacer clock is actually a 24-bit, auto-reload frequency divider. It contains a 24-bit divisor register, a 24-bit counter, an internal clock pre-scaler, and a clock source multiplexer as shown in Figure C-1.

Figure C-1
Pacer clock block diagram



The clock source selection is specified by bit 6 and 7 in the control register. Refer to "Control register (base + 2, write only)." The 24-bit register occupies three ports in which the low byte is located at base + 3, the middle byte at base + 4, and the high byte at base + 5. All three registers are write only. The pacer clock will not generate any clock pulse output until the A/D circuit is running (after receiving the arm command under pre-trigger or after being triggered if pre-trigger is not selected), and the trigger mode is not one-shot. In continuous mode, the trigger serves as the first clock output pulse and loads the counter from the register. The counter counts down the input clock pulse until it reaches zero. An output clock pulse is then generated, and the counter is reloaded. The pacer clock generation continues until the KPCMCIA-12AIAOH PC card receives the stop command, represented by writing a 1 at bit 4 of the command register. Refer to "Command register (base + 7, write only)."

The clock rate generated can be determined by (Source Frequency) / (Divisor Count + 1). For example, if the clock source is 100kHz (internal clock, control register bit 7,6 = 11) and the divisor count is 49, then the pacer clock output frequency will be 2kHz. If an external clock source (control register bit 7,6 = 00) of 120kHz is applied and the divisor count is 39, the pacer clock will then be set at 3kHz.

Command register (base + 7, write only)

The command register is used to send control commands to the KPCMCIA-12AIAOH PC card including arm/trigger (or start A/D), scan list queue and data FIFO flush, stop A/D, and timer/counter latch commands. It also sets the data program/access mode for the data FIFO. The command bits (bits 3 to 7) are actually monostable or self-clearing after the specified command function is completed. They do not need to be cleared. Even though it is possible, sending multiple commands in one I/O instruction is not recommended.

The data FIFO program/access bit and the scan speed selection bits are latched each time they are written. Therefore, take care to avoid changing these bits accidentally when sending the commands to the KPCMCIA-12AIAOH PC card. Refer to Table C-13 for the command register bit definitions.

Table C-13
Command register bit definitions

Bit	Function	Explanation
7	Trigger/arm command	1 = send trigger/arm, 0 = no action
6	Flush data FIFO command	1 = flush, 0 = no action
5	Flush scan list command	1 = flush, 0 = no action
4	Stop A/D command	1 = stop, 0 = no action
3	Latch timer/counter command	1 = latch, 0 = no action
2-1	Scan rate selection	00 = 100, 01 = 50, 10 = 25 (kHz)
0	Data FIFO program/access	1 = data access, 0 = program threshold

Trigger/arm command

If the trigger source is internal (software trigger), writing a 1 at bit 7 sends a trigger to the PC card and starts the A/D conversion process. If the trigger source is external (TTL or analog), writing a 1 to bit 7 serves as an ARM command, which tells the PC card to look for the specified external trigger edge from the moment the ARM command is received. With the pre-trigger option, the arm command actually starts the A/D conversion. This command should never be issued together with the stop A/D command. The data acquisition is initiated after this command is received. Only the stop A/D command can terminate the acquisition.

Flush data FIFO command

The data FIFO should be flushed before the data acquisition can be initiated by the trigger/arm command but after the scan list has been set up. The flush command may also be followed by FIFO threshold programming. After the FIFO is flushed, the FIFO empty flag is set to 1 and the almost full and full flag reset to 0. The flush FIFO command always sets the FIFO thresholds to the default setting (7 bytes to full) at power up or reset.

NOTE *Any time the data FIFO is flushed, the default threshold setting is restored (7 bytes to full) by the hardware. The data FIFO threshold should always be programmed after the flushing if the required threshold is different from the default one.*

Flush scan list queue command

The scan list queue needs to be flushed before it can be programmed. This command should be issued before the flush data FIFO command. The queue may have up to 2048 word entries, each containing two bytes. It is your responsibility to guarantee the integrity of the entries. Refer to "Scan list queue register (base + 1, write only)" for more information about the scan list queue.

Stop A/D command

Once the data acquisition is started by the trigger/arm command, it can only be stopped by receiving this command. As mentioned before, the two commands are exclusive. The stop A/D command should be issued as soon as the required data points are collected to prevent data FIFO overflow, which is the only flag to indicate data lost during the data acquisition process. Without the stop command, the A/D may still be running and filling data into the data FIFO whether it is filled or not. When the data FIFO is full, it will ignore the data samples coming from the A/D converter.

Latch timer/counter command

This command latches the current value of the timer/counter into the 16-bit read latch register. It works if the timer/counter is running (on the fly) or not. The latched value will not change until a new latch command is issued.

Data FIFO program/access control

The A/D data FIFO has two programmable thresholds, almost empty and almost full, and two associated flags. The almost-empty threshold is not used, nor is the almost-empty flag. By default, the thresholds are set to 7 bytes (7 to full and 7 to empty) when reset, powered up, or any time the FIFO is flushed. It can be programmed to any value in between 1 and FIFO size - 1 (in bytes) according to the application. For example, it can be set to the length of the scan list, half to full or quarter to full, etc.

To program the FIFO threshold, make sure the A/D has been stopped. Set this bit to 0 by writing an all 0 byte to the auxiliary control register. Then send a flush A/D FIFO command with the same bit setting by writing a byte of 40H (hex 40) to the same register. This setting will put the FIFO into program mode. When accessing the data FIFO at base + 1 the following read/write operation will be directed to the threshold registers instead. The four byte threshold setting should be written into the data FIFO by performing four consecutive write operations. Optionally, the threshold setting can be read back for verification by performing four consecutive read operations. The four-byte threshold setting has the format shown in Table C-14.

Table C-14
Data FIFO threshold setting

Byte no.	Definition	Valid range
0	Low byte of the almost-empty threshold	0..255
1	High byte of the almost-empty threshold	0..15
2	Low byte of the almost-full threshold	0..255
3	High byte of the almost-full threshold	0..15

After the thresholds are programmed, set the access control bit to 1 by writing a command byte whose bit 0 is set to 1 into the auxiliary control register. This setting will make the following read/write operation access the data bytes in the FIFO instead of its thresholds. It is recommended that the access control bit be set to 1 when sending other commands (flush scan list, stop A/D, or trig/arm) to the KPCMCIA-12AIAOH PC card by writing them into the auxiliary control register after programming the thresholds. A useful tip for safe operation is to set the bit to 0 only when flushing and programming the FIFO thresholds.

Although the almost-empty threshold is never used, it has to be programmed because the four configuration bytes must be accessed as a single entity.

Scan rate selection

Depending on the input mode and the gain selection, the analog front end may have different settling times. To keep the best performance, the KPCMCIA-12AIAOH PC card allows you to choose three different scanning rates by setting bit 2 and bit 3 while the start A/D command is issued. The default scanning rate is 100kHz (bits 3 and 2 set to 00). Setting the bits to 01, selects the 50kHz rate. Setting the bits to 10 selects 25kHz. Setting the bits to 11 is the same as 01.

It is recommended that the scan rate setting be issued together with the trigger/arm command, and not changed during data acquisition. For example, writing 81H to the auxiliary control register will start the data acquisition with the scan rate set to 100kHz (use 83H for 50kHz and 85H for 25kHz).

D/A data port (base + 8, base + 9)

The D/A data port can be accessed either as a 16-bit word at base + 8 or as two consecutive bytes at base + 8 (low byte) and base + 9 (high byte). The port is write only. For simplicity, the 16-bit word is assumed in the following discussion.

Bits 12 to 15 select the D/A channel in which bits 13, 14, and 15 must all be set to 0, and bit 12 is either set at 0 to select D/A channel 0 or 1 to select D/A channel 1. Refer to Table C-15 for bit definitions.

Table C-15
D/A data port bit definitions

Bits	Definition	Explanation
15-13	Reserved	as all 0
12	D/A channel selection	0 for channel 0, 1 for channel 1
11-0	D/A output code value	-2048..2047 in 2's complement

D/A channel output

Bits 0 to 11 specify the D/A channel data, which is always in 2's complement format. The bipolar D/A channel output ranges from -5 to +5V with corresponding code values from -2048 to 2047. The actual D/A output voltage U (in volts) can be determined from the output code value C from the following formula:

U = C*5 / 2048

Only the output of D/A channel 1 is used to set the analog trigger threshold. Refer to "Analog trigger threshold" for more information.

D/A port interface

The data link between the D/A data port and the D/A converter is a serial link. A 16-bit buffer register and a 16-bit shift register are in the port interface. On the other side of the link, an input register and an output register are in each D/A channel of the D/A converter. The actual analog output voltage is determined by the code value loaded into the output register as described in the previous paragraph.

The data word written into the D/A port is first latched into the 16-bit buffer register. It is then loaded into the 16-bit shift register and shifted into the D/A channel's input register across the serial link. Bit 5 in the auxiliary status register is set to 1 to show that the buffer is occupied as soon as the buffer register is written. It remains 1 until its content is loaded into the shift register. By then, the bit is cleared to indicate that the buffer is empty.

Since the serial link needs 16 of the 2MHz clock cycles to complete one 16-bit data word, it takes about 8µs for each data word transfer. The buffer register is only loaded into the shift register when the latter has finished shifting. You must check this bit and make sure the buffer register is empty before writing into it. Otherwise, the original data in the buffer register may become corrupted. The interface hardware will neither prevent it from happening nor report it as an error.

D/A update modes

Depending on the D/A update mode, the data word shifted into the D/A channel may either be passed immediately into the output register (direct update mode) or loaded into the output register upon receiving the synchronous event (synchronous update modes).

Bits 1 and 0 of the auxiliary control register (base + 15, write) defines the D/A update modes as summarized in Table C-16.

Table C-16
D/A update modes

Bit 1,0	Mode	Update
00	0	Direct update immediately after the data word is written
01	1	Each time when the timer overflows
10	2	Each time when the gate control goes from low to high
11	3	Each time the A/D pacer clock fires

In mode 0, the D/A converter's output register is updated as soon as the data word shifts into its shift register, bypassing its input register, after the D/A port buffer register is written. There is no synchronization between the two D/A channels in this mode. Each are operated independently.

In modes 1, 2, and 3 (the synchronous modes), the data word written into the port buffer register is loaded into the D/A channel's input register before it can be written into its output register. Upon receiving a synchronous event, the output registers in both D/A channels are updated at the same time.

In mode 1, the synchronous event is the timer overflow. The synchronous event in mode 2 is the gate control going from low to high. In mode 3, the event is the pacer clock.

Timer/counter port (base + 10, base + 11)

The timer/counter port can be accessed either as a 16-bit word at base + 8 or two consecutive bytes at base + 8 (low byte) and base + 9 (high byte). The port contains a 16-bit reload register, a 16-bit up-counter, a 16-bit read latch register, and the associated control logic.

The reload register is write only. It holds the initial value (or the reload value) for the up-counter. Each time the counter overflows, the next clock rising edge reloads the counter with this value. The same value is also loaded into the counter as its initial value in mode 0. (See the discussion below.)

The read latch register is read only. It holds the current count of the up-counter when a latch command is received. The content of this register will not change until the next latch command comes. Refer to "Latch timer/counter command" to send the read latch command.

The up-counter cannot be accessed directly. It reloads on the next rising edge of the selected clock from the reload register either when it reaches its final count of 65535 (hexadecimal FFFF) or when the timer/counter is in mode 0.

Timer/counter operation modes

Bits 3 and 4 in the auxiliary control register (base + 15, write) determine the timer modes as summarized in Table C-17.

Table C-17
Timer/counter mode

Bit 4,3	Mode	Timer/counter operation
00	0	Stop and reload the up-counter from the reload register
01	1	Pause
10	2	Start/Continue
11	3	Operation controlled by the gate input: Gate = Low: Pause, Gate = High: Start/Continue

Mode 0 is used to reload the up-counter. Note that the reloading only takes place when the next rising edge of the selected clock source comes. For the internal clock source, it takes at least 1µs. When the timer/counter is used to count external pulses, select mode 0 and the internal clock source to guarantee the initial reloading by the internal clock and then switch the source to external. Refer to "Timer/counter clock source" for information on setting the internal clock.

Mode 1 is designed to temporarily pause the up-counter. The up-counter is frozen in this mode.

Mode 2 is also named the "go" mode. The up-counter either starts or continues counting up on the rising edge of the selected clock source. If the up-counter reaches its final count, it reloads on the next clock rising edge.

In mode 3, the up-counter operation is controlled by the external gate signal [pin 18 on the PC card 33-pin connector (pin 8 on the D-37)]. The counter "goes" when the signal is high (logic 1) and stops when the signal is low (logic 0).

Timer/counter clock source

Bit 2 of the auxiliary control register (base + 15, write) selects the timer/counter clock source. It is either the internal 1MHz clock (bit 2 is 0) or the external clock (bit 2 is 1). Because of the pin confinement, the timer/counter external clock input is shared with the A/D external clock input, which is also the digital input bit 2.

The external clock has a minimum pulse width of more than 100ns and a maximum frequency of no more than 5MHz, the same as specified in "Clock source."

Reading the contents of the timer/counter

The content of the up-counter can be read "on the fly" by sending the read latch command. Refer to "Latch timer/counter command" for more information. Upon receiving the command, the current content of the up-counter latches into the read latch register. The timer/counter control logic guarantees the integrity of the latched value. The read latch operation is independent of the timer/counter modes. It works in all four modes.

The latched value in the read latch register does not change until next read latch command is received.

Timer divisor or counter modulus

As described in Section 3, the up-counter always counts up from its initial value (determined by the reload register) to its final count (always 65535 or hexadecimal FFFF). Suppose D is the divisor (also called modulus for counter) of the timer and X is the value written into the reload register. The relation between the two is:

D = 65536 - X

The up-counter will now count up from X to 65535. Avoid D=1 or X=65535 because the up-counter will be stuck with this value.

Timer/counter overflow

When the timer/counter reaches its final count of 65535, the next rising edge of the selected clock source reloads the up-counter from the reload register and sets the timer/counter overflow event latch to 1 (bit 4 of the auxiliary status register, read). This will cause an interrupt if the timer/counter interrupt is enabled (bit 5 of the auxiliary control register set to 1).

The overflow event latch can be cleared only by writing a 0 into bit 5 of the auxiliary control register (originally 1 or 0). Reading the auxiliary status register does not clear the timer/counter overflow event latch.

Generally speaking, the timer/counter output will be 1 for one clock cycle time as the timer/counter overflows (after the cycle when it reaches the final value of 65535). If the timer/counter is paused or stuck at its final count, the output pin will then be high as long as the final count holds.

The timer/counter is totally independent of the pacer clock, which is dedicated to generating a sample rate in continuous trigger mode for the A/D converter. It can be used for the D/A converter to synchronize its channel output updating, as described in "D/A update models."

Auxiliary control register (base + 15, write only)

This register configures the operation of A/D, D/A, and the timer counter. It is 8-bit wide and write only.

Refer to Table C-18. Bit 7 selects between TTL and analog trigger source. Bit 6 sets the pre-trigger option. Refer to Section 3 and "Analog trigger threshold" in this section for further information.

Bit 5 is for the timer/counter interrupt control. Bits 3 and 4 determine the timer/counter operation modes, while bit 2 selects its clock source. Refer to Section 3 and "Timer/counter port (base +10, base +11)" in this section for more information.

Bits 1 and 0 specify the D/A update modes. Refer to Section 3 and "D/A update modes" in this section for more information.

Table C-18
Auxiliary control register bit definitions

Bit	Function	Explanation
7	External trigger source	0 selects TTL trigger 1 selects analog trigger
6	Pre-trigger option	1 = with pre-trigger, 0 = without
5	Timer/counter interrupt Clear overflow event latch	1 = Enabled, 0 = Disabled by writing 0 into this bit
4,3	Timer/counter mode	00 = Reload 01 = Pause 10 = Go 11 = Go/Pause by external gate signal
2	Timer/counter clock source	1 = External, 0 = Internal (1MHz)
1,0	D/A update mode	00 = Direct update 01 = When timer/counter overflows 10 = When ext. gate goes low to high 11 = When pacer clock fires

Auxiliary status register (base + 15, read only)

Bits 0 to 3 and bit 7 in this register are organized for bits in the status register (base + 2) and can be referenced without the associated side effect of "clear after read" on the latched events. Backward compatibility is kept by preserving the "clear after read" side effect for the status register in KPCMCIA-12AIAOH PC cards.

Refer to Table C-19. Bits 0 and bit 1 are the data FIFO flags exactly as in the status register. Bit 2 in this register is the data lost event latch, as is bit 5 in the status register. These three bits are defined exactly the same as in the status register.

Bit 3 in this register is the logic OR of the two event latches in the status register; i.e., the EOS event latch and the data FIFO event latch. This bit is 1 if either EOS or FIFO event is latched. It is 0 if both EOS and FIFO events are cleared (by power up, reset, or reading the status register).

Table C-19
Auxiliary status register bit definitions

Bit	Function	Explanation
7	A/D running flag	1 = Running, 0 = Idle
6	A/D trigger flag	1 = Triggered, 0 = Not yet
5	D/A port buffer register flag	1 = Occupied, 0 = Empty
4	Timer/counter overflow event latch	1 = Overflow latched, 0 = Not yet
3	A/D conversion event latched (logic "OR" of A/D EOS and FIFO almost-full event latches)	1 = Either EOS or FIFO almost-full event has been latched 0 = Neither event has been latched yet
2	Data lost event latch	1 = Data lost latched, 0 = Not yet
1	A/D data FIFO almost-full flag	1 = FIFO almost full, 0 = Not yet
0	A/D data FIFO empty flag	1 = FIFO empty, 0 = Not empty

Bit 4 indicates the timer/counter overflow event. It is 1 each time the timer/counter overflow occurs (actually on the next rising edge of the select clock source after it reaches the final count). This bit is not cleared by reading the auxiliary status register. It can only be cleared by writing a 0 into bit 5 of the auxiliary control register. Refer to Section 3 and "Timer/counter port (base +10, base +11)" in this section for more information.

Bit 5 tells whether the D/A port buffer register is occupied (1) or empty (0). Refer to Section 3 or "D/A data port (base +8, base +9)" in this section for more information.

With the pre-trigger option selected, bit 6 is set to 1 when the external trigger comes. It remains 1 until the data acquisition is terminated by receiving the A/D stop command. Refer to "Stop A/D command." Bit 6 of 0 means the trigger has not activated yet. If the pre-trigger option is not selected (or bit 6 of the auxiliary control register is 0), this bit should be ignored.

Bit 7 is exactly the same as bit 6 in the status register (base + 2, read only). Refer to "Status register (base +2, read only)" for more information.

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Specifications are subject to change without notice.

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