KPCI-3160

Logic Inputs and Outputs

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Voltage, Input High	2.0	—	—	V
V_{IL}	Voltage, Input Low	—	—	0.8	V
I_{IH}	Current, Input High, V_{IN} = 2.7V	—	—	±1	µA
I_{IL}	Current, Input Low, V_{IN} = 0.5 V	—	—	±1	µA
I_{OZH}	High Impedance Output Current, V_{OUT} High	—	—	±1	µA
I_{OZL}	High Impedance Output Current, V_{OUT} Low	—	—	±1	µA
V_{OH}	Voltage, Output High, I_{OH} = –8 mA	2.4	3.3	—	V
V_{OH}	Voltage, Output High, I_{OH} = –15 mA	2.0	3.0	—	V
V_{OL}	Voltage, Output Low, I_{OL} = 64 mA	—	0.3	0.55	V
I_{OL}	Current, Output Low	—	—	64.0	mA
I_{OH}	Current Output High	—	—	–15	mA
I_{OS}	Short Circuit Current	–60.0	–120.0	–225.0	mA
I_{OFF}	Input/Output Power off leakage	—	—	±1	µA

Digital I/O

Each channel of the KPCI-3160 may be fully loaded provided the total sourcing current does not exceed the ratings of the KPCI-3160 and accessories/circuits used, i.e. each channel of Port A may simultaneously source 15mA for a total of 120mA with no risk of output driver overheating. Details of current capability via on-board power is discussed below.

Power Available To External Circuits

The KPCI-3160 provides current limited power available to external circuits via the 100 pin connector. The locations and requirements are summarized below.

KPCI-3160 PIN #	PARAMETER	MIN.	TYP.	MAX.	UNIT
1	+5 Volts	—	—	1.0	A
50	GND Return	—	0.0	—	V
51	+5 Volts	—	—	1.0	A
100	GND Return	—	0.0	—	V

Current drawn from pin pair #1 and #50 should not exceed 1.0A. Similarly, current drawn from pin pair #51 and #100 should not exceed 1.0A. Total current available to drive external circuits is limited to 2.0A. This power is supplied by the PC power supply.

Assuming power supply of +5VDC and full loading (2A), the KPCI-3160 requires a maximum of 10.5W of power.

KPCI-3160 100-Pin Connector

3160 Data Group 0		3160 Data Group 1		3160 Data Group 2		3160 Data Group 3	
Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
76	PA0	26	PA0	52	PA0	02	PA0
77	PA1	27	PA1	53	PA1	03	PA1
78	PA2	28	PA2	54	PA2	04	PA2
79	PA3	29	PA3	55	PA3	05	PA3
80	PA4	30	PA4	56	PA4	06	PA4
81	PA5	31	PA5	57	PA5	07	PA5
82	PA6	32	PA6	58	PA6	08	PA6
83	PA7	33	PA7	59	PA7	09	PA7
84	PB0	34	PB0	60	PB0	10	PB0
85	PB1	35	PB1	61	PB1	11	PB1
86	PB2	36	PB2	62	PB2	12	PB2
87	PB3	37	PB3	63	PB3	13	PB3
88	PB4	38	PB4	64	PB4	14	PB4
89	PB5	39	PB5	65	PB5	15	PB5
90	PB6	40	PB6	66	PB6	16	PB6
91	PB7	41	PB7	67	PB7	17	PB7
92	PC0	42	PC0	68	PC0	18	PC0
93	PC1	43	PC1	69	PC1	19	PC1
94	PC2	44	PC2	70	PC2	20	PC2
95	PC3	45	PC3	71	PC3	21	PC3
96	PC4	46	PC4	72	PC4	22	PC4
97	PC5	47	PC5	73	PC5	23	PC5
98	PC6	48	PC6	74	PC6	24	PC6
99	PC7	49	PC7	75	PC7	25	PC7

Board Address Mapping

No jumper placed on REG-MAP-SEL yields register map A. (DEFAULT)

There are 4 data groups with 4 control bytes. Each control byte is part of the corresponding 32 bit data word.

FORMAT:
Control/Data register: (MSB)[Control Byte X][Port C][Port B][Port A](LSB)

Base Address 1 + Offset 0×00	Group 0 Data	Read/Write
Base Address 1 + Offset 0×04	Group 1 Data	Read/Write
Base Address 1 + Offset 0×08	Group 2 Data	Read/Write
Base Address 1 + Offset 0×0C	Group 3 Data	Read/Write

Control Byte X Format REG MAP A:

Bit 7 - This bit to be ignored.

Bit 6 - Access Mode Select – For B5 and B6. See table below.

Bit 5 - Access Mode Select – For B5 and B6. See table below.

Bit 4 - PAx_DIR - Port A I/O direction, 1-input, 0-output

Bit 3 - PCHIx_DIR - Port C HI I/O direction, 1-input, 0-output

Bit 2 - This bit to be ignored.

Bit 1 - PBx_DIR - Port B I/O direction, 1-input, 0-output

Bit 0 - PCLOx_DIR - Port C LO I/O direction, 1-input, 0-output

B6	B5	
0	0	No input latching.
0	1	Latch group inputs on rising interrupt edge.
1	0	No input latching.
1	1	Latch group inputs on falling interrupt edge.

This emulates the 8255A standard.

Emulation of AMCC S5933 Interrupt Control/Status Register(INT_CSR)

Base Address 0 + Offset 0×38	Interrupt Status Register	Read/Write

Interrupt Status Register Format:

Bit 23 Interrupt missed =1 for missed interrupt. Write 1 to acknowledge/clear.

Bit 17 Interrupt pending = 1 for pending interrupt. Write 1 to acknowledge/clear.

Bit 12 Interrupt enable = 1, HW Interrupts enabled, 0 = HW Interrupts disabled.

Bit 06 Interrupt polarity select = 1 for falling edge, Write 0 for rising edge.

Base Address 0 + 0x34 (32 Bit Read) = ASCII “A” “0” “x” “x” – Firmware Revision.

GENERAL

POWER REQUIREMENTS: +5V, 0.07A min.
+5V, 1.5A typ.
+5V, 2.1A max.

EMC: Conforms to European Union Directive 89/336/EEC.

SAFETY: Meets EN61010-1/IEC 1010.

ENVIRONMENTAL:
Operating Temperature: 0° to 70°C
Storage Temperature: –40° to 100°C
Humidity (non condensing): 0 to 90%.

DIMENSION, WEIGHT: 127mm long × 108mm wide × 19mm high (5″ × 4.25″ × 0.75″) (half slot). Net weight 125g (4.4 oz).

Specifications are subject to change without notice.