TRG1
Analog Trigger Module

Introduction

The TRG1 Analog Trigger Module (Figure 1) contains circuitry for one channel of real-time, hardware-based triggering of analog data acquisition. The TRG1 module is designed for use with the Keithley AMM1A or AMM2 Analog Master Measurement module, revision D or later, which will be referenced hereout as "AMM module".

The TRG1 controls the AMM module's high-speed "auto-acquire" mode which is driven by a crystal oscillator located on the AMM. The TRG1 provides an A/D start signal which travels over a dedicated pathway and initiates A/D conversion on the AMM module. As an alternative to triggering on an analog input, the TRG1 can also initiate A/D conversion in response to a global strobe command sent from the data acquisition mainframe.

The TRG1 module has input ranges of 0 to +1V, 0 to -1V, 0 to +10V, and 0 to -10V with an input resistance of 10 megohms. Coupling is selectable for AC or DC signals. Input signals are applied to the TRG1 external signal input through a quick-disconnect screw terminal block located on the module, or to the TRG1 global amplifier input via a cable which connects to the AMM global amplifier output. The TRG1 triggering threshold is set by a programmable, 8-bit D/A converter. A programmable low-pass filter provides input filtering with eight cut-off frequencies from 300Hz to 1MHz. This filter can be used to eliminate noise on the trigger signal which may otherwise cause false triggering.

Beside starting an A/D conversion, the TRG1 trigger signal can also assert an Interrupt Request (IRQ) to the host computer via the IBIN interface card, which can then be used to implement special-purpose, user-written service routines. Check the documentation and revision level of your IBIN interface to determine whether this feature is implemented on the IBIN.

The number of possible trigger configurations is a function of the number of TRG1 modules in the system, and how the mode, reset, and cycling features are programmed. These programming tasks are handled automatically by higher-level languages such as Keithley's KDAC500.

Document Number 501-917-01 Rev. A

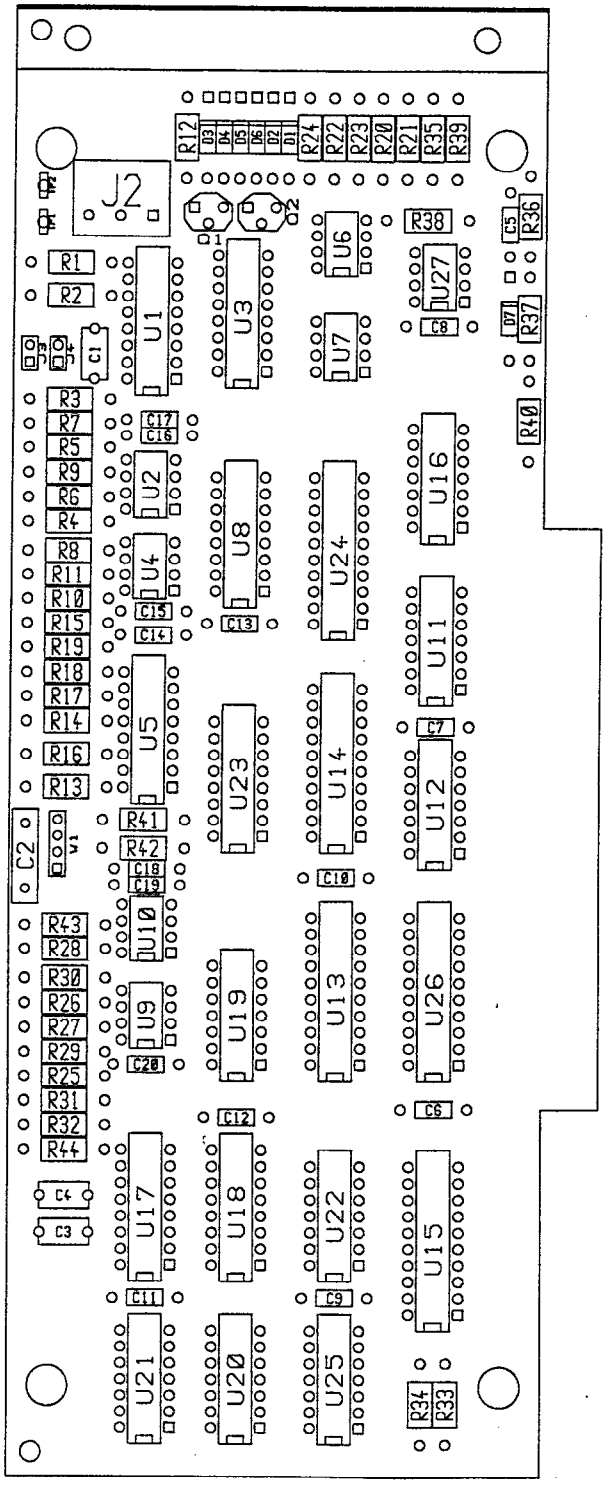


FIGURE 1. TRG1 MODULE

The TRG1 offers two trigger modes:

1. Single-event Mode, in which the TRG1 generates a single trigger start command the first time the programmed trigger condition is met, or

2. Normal Mode, in which the TRG1 generates a trigger start command each time the programmed trigger condition is met.

The trigger level generated by the TRG1 is latched when the programmed trigger condition is met. This trigger latch can be reset in one of two ways. The desired reset method must be programmed by writing the appropriate bits to the TRG1 CMDA register:

1. Manual reset - reset by reading of the CMDB control register, and

2. Automatic reset - reset automatically when the trigger condition is no longer met.

The cycling of the trigger operation can be programmed for two modes:

1. One-shot - take a single reading

2. Continuous - take readings continuously as long as the trigger condition is met.

Typical trigger modes include, but aren't limited to, the following (see Figure 2):

1. Trigger at a user-defined threshold on the falling slope of the trigger signal. Stop when the prescribed number of points has been acquired.

2. Trigger at a user-defined threshold on the rising slope of the trigger signal, and acquire data only when the signal is above the threshold. Stop when the prescribed number of points has been acquired.

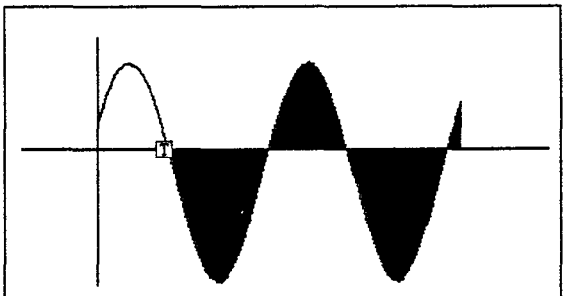
3. Trigger at a user-defined threshold on the falling slope of the trigger signal, and acquire data only the first time the signal is below the threshold level. Stop when the signal rises above the threshold.

4. Trigger at a user-defined threshold on the rising slope of the trigger signal and take only one reading. (Normally used to trigger a reading off another channel.)

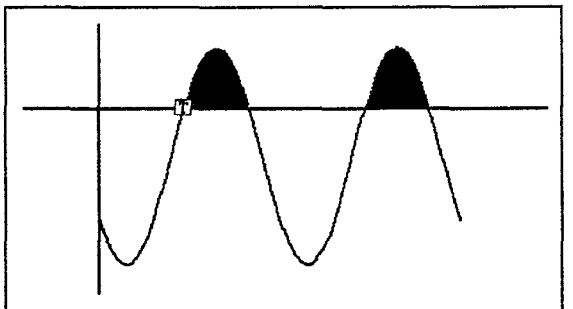
5. Trigger at a user-defined threshold on the falling slope of the trigger signal and acquire one reading. Repeat each time the trigger condition is met until the prescribed number of points has been acquired. (Normally used to synchronize readings to an external event.)

Information for implementing these trigger setups is included later in this manual.

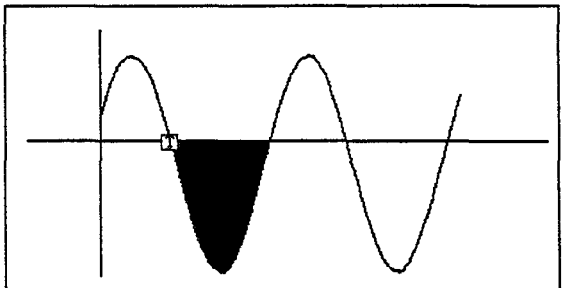
TRG1 • PROGRAMMABLE TRIGGER MODULE



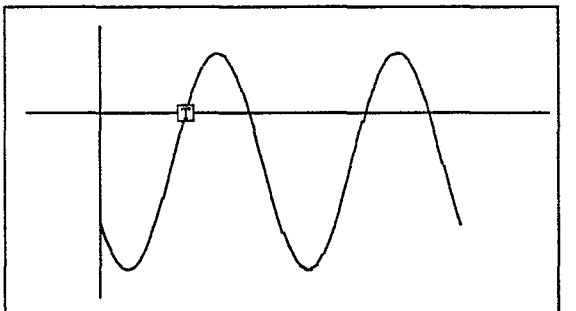
1. Trigger at a user-defined threshold on the falling slope of the trigger signal. Stop when the prescribed number of points have been acquired.



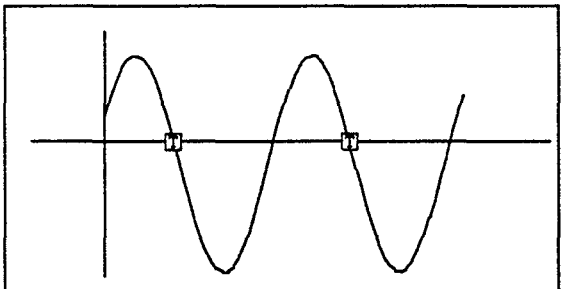
2. Trigger at a user-defined threshold on the rising slope of the trigger signal, and acquire data only when the signal is above the threshold. Stop when the prescribed number of points have been acquired.



3. Trigger at a user-defined threshold on the falling slope of the trigger signal, and acquire data only the first time the signal goes below the threshold level. Stop when the signal goes back up above the threshold



4. Trigger at a user-defined threshold on the rising slope of the trigger signal and take only one reading. *Normally used to trigger a reading off of another channel.*



5. Trigger at a user-defined threshold on the falling slope of the trigger signal and acquire one reading. Repeat each time the trigger condition is satisfied until the prescribed number of points have been taken. *Normally used to synchronize readings to an external event.*

FIGURE 2. TYPICAL TRG1 TRIGGER MODES

Hardware Compatibility

The TRG1 module is compatible with the Keithley 500A, 500P, and 575 data acquisition systems. When used with these systems, the TRG1 module requires that a revision D or later AMM1A or AMM2 Analog Master Measurement module be mounted in slot 1.

When one TRG1 module is to be used with a Model 500A or 500P, it must be used in slot 2. The 500-series systems can operate with two TRG1 modules, in which case the second TRG1 must be plugged into slot 3. The TRG1 pair can perform various trigger operations based on ANDing or ORing of the trigger input signals.

The Model 575 contains the equivalent of a TRG1 module built into its main circuit board. A TRG1 may be mounted in the Model 575 option slot (assigned as slot 3) to obtain the functionality of two TRG1 modules.

The TRG1 module is not compatible with the System 570, with the original AMM1 (pre rev "A" version) module, or with older AIM1/ADMx analog input module sets.

Software Compatibility

The TRG1 module can be programmed and operated using Keithley's KDAC500 software packages, or with any software which specifically supports the TRG1. All TRG1 features, such as input range, AC/DC input coupling, input filtering, and edge sensitivity are controlled through software.

In using the TRG1 module, you must decide whether you want to trigger from an input applied to the TRG1 external input terminals, or the TRG1 global amplifier input connector. Each method facilitates different trigger setups which may be better suited to a given application. This input selection is controlled through software.

When operated under KDAC500, the trigger function requires simultaneous use of the KDAC500 ANINQ and ANTRIG commands. To trigger from a signal connected to a TRG1 external input channel J2, set up an IONAME for ANTRIG which references the slot (and channel 0) of the specific TRG1. This automatically informs the software that triggering is to be based on the TRG1 external input J2.

Use of the TRG1 global amp input permits the TRG1 to trigger from any analog input signal connected to any AMM or AIM analog input module. Set up an IONAME parameter for ANTRIG which references the desired analog input slot and channel. This automatically sets the software for triggering on the signal at the TRG1 global amp input J3 or J4. That signal will automatically be routed through the global amplifier of the AMM module to the global amplifier input of the TRG1 module.

You may also program the TRG1 module by directly accessing its command registers. See Table 1 later in this manual for a complete listing of TRG1 command registers and functions.

Keithley's Soft500 and Quick500 do not directly support the TRG1, although BASIC PEEK and POKE commands can be used to access the TRG1 command locations.

Specifications

Channels: 1, differential input

Trigger Source: External trigger input terminals, Global Amplifier output of AMM1A or AMM2 analog module, or Software Strobe.

Input Ranges: 0 to +1V, 0 to -1V, 0 to +10V, or 0 to -10V.

Resolution: 8 bits

Level Accuracy: ±2% + 1 LSB

Input Impedance: 10 MΩ (external trigger input)

Input Protection: ±30V maximum (powered); ±15V maximum (unpowered)

Input Coupling: AC or DC

Trigger: Rising or falling edge (positive or negative slope)

Input Connector: 3-pin quick-disconnect screw terminal block for external input. Cable (CA-85-1) to AMM card global amplifier (supplied).

Input Filter: Software-selectable single pole low-pass filter with the following characteristics:

-3dB Frequency	Settling Time to 1/2 LSB
1 MHz	1 μS
300 kHz	3.3 μS
100 kHz	10 μS
30 kHz	33 μS
10 kHz	100 μS
3 kHz	333 μS
1 kHz	1 mS
300 Hz	3.3 mS

Output: 1. Low-true trigger signal to motherboard connector for triggering AMM1A or AMM2 in adjacent slot,

2. Interrupt Request (IRQ) to the host computer,

3. Status register

Note: IRQ is open-collector low-true pulse 500 nS typical. A/D trigger signal is software selectable to be either a 500nS low-true pulse, or a low-true level.

Note: The TRG1 requires a +10V reference signal to be present on the back-plane, which is typically provided by an AMM1A or AMM2 module used in slot 1. If one TRG1 is used in a system, it must be placed in slot 2. If two TRG1 modules are used in a system, they must be placed in slots 2 and 3.

Trigger Signal Connection

The trigger input signal may be connected to the TRG1 module by two methods.

The first method involves simply connecting the trigger signal leads to the external analog trigger input J2. This is a quick-disconnect block located on the rear of the TRG1 module. Three screw terminals provide for one channel of differential input. Connect the high (+) side of the trigger input signal to the HI terminal screw of J2. Connect the low (-) side of the trigger input signal to the LO terminal screw of J2. Connector J2 includes a ground terminal for connecting the shield of the input cable.

CAUTION: The differential inputs of the TRG1 module must both be within ±10V of module ground for proper operation. If either side of the signal is greater than ±30V, the TRG1 may be damaged.

The second method for connecting a trigger input is to attach a cable between the TRG1 Global Amplifier Input, J3 or J4, and the AMM module Global Amplifier Output J7. A special shielded cable CA-85-1 is supplied with the TRG1 module for this purpose. The CA-85-1 cable is constructed with a chamfer on one corner of the plastic housing which terminates the cable. This chamfer indicates the center, signal-carrying conductor of the cable, and should be positioned toward the front of the data acquisition system where the cable connects to the TRG1, and toward the rear of the system where the cable connects to the AMM module (see Figure 3).

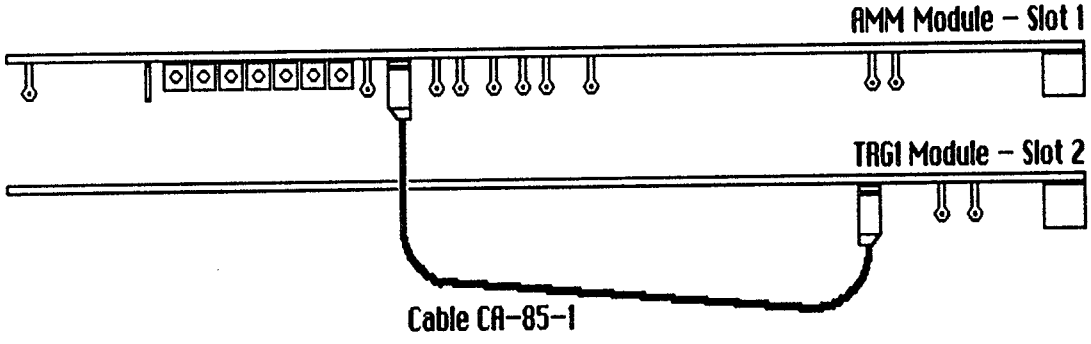


FIGURE 3. TRIGGER CABLE CA-85-1

In a 500-series system with two TRG1s, or a Model 575 with one TRG1, the trigger signals may be connected to the AMM global amp by using a pair of CA-85-1 cables. The high and low sides of J3 and J4 on the TRG1 are connected in parallel. For this application, connect J7 of the AMM to J3 of the first TRG1 module. Connect J4 of the first TRG1 module to J3 or J4 of the second TRG1.

CAUTION: Improper connection of the trigger cable may degrade the signal or introduce excessive noise into measurements.

Installation

Installation of the TRG1 module involves configuration, jumper placement, and interconnection of the TRG1 and AMM modules.

CAUTION: Turn off power to the data acquisition system before you insert or remove any module. To minimize the possibility of EMI radiation, always operate the data acquisition system with the cover in place and properly secured.

Installation of One or Two TRG1 Modules in a 500A or 500P

The TRG1 may be operated in slot 2, or slots 2 and 3 of a 500A or 500P data acquisition system. To install the TRG1 in a 500-series system, first remove the top cover.

Single Trigger Input - to trigger an AMM module off a single trigger signal, plug the TRG1 module into slot 2. Set jumpers and connections as follows:

TRG1 module - Locate the 4-pin jumper W1. Jumper pin 1 to pin 2. Connect the trigger signal to the TRG1 external or global input.

AMM module - place jumper J3 over pins 1 and 2. Connect the signal of interest to one of the AMM input channels.

Dual Trigger Inputs - to trigger an AMM module off some combination of two trigger signals, plug TRG1 modules into slots 2 and 3. Set jumpers and connections as follows:

"OR" Operation (data will be acquired when the trigger conditions assigned to either trigger input is satisfied):

Slot 2 TRG1 module - Locate the 4-pin jumper W1 on the TRG1 module. Jumper pin 1 to pin 2, and pin 3 to pin 4 (2 jumper blocks required). Connect one trigger signal to the TRG1 external or global input.

Slot 3 TRG1 module - Locate the 4-pin jumper W1 on the TRG1 module. Jumper pin 1 to pin 2, and pin 3 to pin 4 (2 jumper blocks required). Connect the other trigger signal to the TRG1 external or global input.

AMM module - place the jumper J3 over pins 1 and 2. Connect the signal of interest to one of the AMM input channels.

"AND" Operation (data will be acquired only when the trigger conditions assigned to both trigger inputs are satisfied):

Slot 2 TRG1 module - Locate the 4-pin jumper W1 on the TRG1 module. Jumper pin 2 to pin 3 (1 jumper block required). Connect one trigger signal to the TRG1 external or global input.

Slot 3 TRG1 module - Locate the 4-pin jumper W1 on the TRG1 module. Connect pin 1 to pin 2, and pin 3 to pin 4 (2 jumper blocks required). Connect the other trigger signal to the TRG1 external or global input.

AMM module - place the jumper J3 over pins 1 and 2. Connect the signal of interest to one of the AMM input channels.

Installation of TRG1 in the Model 575

You may add a TRG1 to the Model 575 for dual triggering capability. The TRG1 will involve additional jumper configurations on the AMM module and Model 575 motherboard. See the 575 manual for more information on jumper placement.

NOTE: Your Model 575 manual may identify TRG1 jumper W1 as "J3". This is an earlier jumper designation. W1 is the only 4-pin jumper on the TRG1.

NOTE: To gain access to the jumpers on the AMM module and 575 motherboard, you must remove the AMM module from slot 1. The TRG1 will occupy the option slot 3.

Dual Trigger Inputs - to trigger an AMM1A or AMM2 analog input module off some combination of two trigger signals, add a TRG1 module to slot 3. Set jumpers and connections as follows:

"OR" Operation (data will be acquired when the trigger condition assigned to either trigger input is satisfied):

575 trigger jumpers - Locate W201. Jumper pin 1 to pin 2, and pin 3 to pin 4 (2 jumper blocks required). Connect one trigger signal to the 575 external or global trigger input.

Optional TRG1 module - Locate 4-pin jumper W1. Jumper pin 1 to pin 2, and pin 3 to pin 4 (2 jumper blocks required). Connect the other trigger signal to the TRG1 external or global input.

AMM module - place the jumper J3 over pins 1 and 2. Connect the signal of interest to one of the AMM input channels.

"AND" Operation (data will be acquired only when the trigger conditions assigned to both trigger inputs are satisfied):

575 trigger jumpers - Locate W201. Jumper pin 2 to pin 3 (1 jumper block required). Connect one trigger signal to the 575 external or global trigger input.

Optional TRG1 module - Locate the 4-pin jumper W1. Connect pin 1 to pin 2, and pin 3 to pin 4 (2 jumper blocks required). Connect the other trigger signal to the TRG1 external or global input.

AMM module - place the jumper J3 over pins 1 and 2. Connect the signal of interest to one of the AMM input channels.

Theory of Operation

Refer to the TRG1 schematic drawings at the end of this manual for the following discussion:

The triggering circuit can be divided into three sections: the command decoding circuitry, the analog input and comparator circuitry, and the trigger/level selection circuitry.

In the command circuitry, input data from the PC bus is latched by octal latch/buffers U13, U14, and U15 (74LS273). Output data to the bus is buffered out by the octal transparent latch U15 (74LS373). Command and read/write information is decoded by U11, U12, and U16. Analog input selection is accomplished by quad analog SPST switch U1 (DG211). Component U23 (74LS153) selects either analog inputs (determined by U1) or digital (Global Strobe) triggering inputs, and provides the logic input for chaining two TRG1 modules together.

The CMDA write cycle controls trigger input and configures the trigger and IRQ outputs. The CMDB write cycle controls the selection of filter, range, AC or DC coupling, and triggering edge. The CMDC write cycle latches the trigger level data (in counts) into the D/A converter U8 (AD7523JN) by the octal latch/buffer U24 (74LS273).

The CMDA read cycle passes the trigger status information to the PC data bus with U15. The CMDB read cycle also retrieves status information. Additionally, it performs a manual reset of the trigger and IRQ latching circuits. A CMDC read is not implemented.

There are four possibilities of input selection: external analog input (EXT TRIG IN) at J2, global amplifier input (GLOBAL IN) at J3 and J4, update from the global strobe, and no trigger input. Input selection is accomplished by electrically switching the input with the quad SPST analog switch U1; by disabling both inputs and strobing the addressing of the demultiplexer at U23; or deselecting all inputs. Gain selection is performed by switching precision resistors in and out of the feedback circuitry of the dual JFET op amp U2 (LF412CN) with analog switch U3A. Input coupling for AC is selected by opening the analog switch U3B.

The trigger threshold voltage is subtracted from the amplified trigger signal via U4A which moves the trigger voltage to zero volts. Components Q1, Q2, R12, and D1 through D6 form an anti-saturation clamp circuit for the output of the differential amplifier U4A, which prevents the output of U4A from exceeding the +10V or -10V clamp reference voltages provided by U6A and U6B.

Filtering of the input signal is accomplished by a series of precision resistors (R213 through R219), an 8-channel analog demultiplexer U5 (IH6108) and a capacitor (C202). The filter cap is fed by switching in one of the seven (or no) resistors to form a single-pole low pass filter with cut-off frequencies of 300Hz, 1kHz, 3kHz, 10kHz, 30kHz, 100kHz, 300kHz, and 1 MHz. The eighth resistor is not used for the 1MHz filter because the ON resistance of U5 functions as the filter resistor.

Polarity selection is performed by switching the reference voltage on the D/A converter U8 between +10 and -10 volts. Edge selection is performed by demultiplexing the inputs from the dual one shot U17 (74LS221) in the 4-to-2 demultiplexer U18 (74LS153) to separate IRQ and trigger pulses dependent upon the trigger region status. The POS PULSE output from U17A is enabled whenever the input is above the trigger voltage. This 500nsec pulse is switched to the 2Y output of U18 when triggering on the rising edge is selected. Similarly, the NEG PULSE output from U17B is switched to the 2Y output when the input is below the trigger voltage and triggering on the falling edge is selected. The IRQ is handled similarly but is dependent upon the selection of IRQ on trigger start or trigger finished.

For input to the trigger circuit from the AMM global amplifier, a low-loss transmission line is included with the TRG1 module. Since the global output amplifier on the AMM card is capable of amplifying at relatively high frequency, a low capacitance connection is required to minimize distortion of the input to the trigger circuit. For low frequency applications, a regular wired connection would be sufficient. In any case, a wired path must be provided to the global amp input of the trigger circuit (if used) as none is provided on the motherboard.

Two jumpers are located on the TRG1 board in a single 4 pin header identified as W1. Applications using one or two trigger circuits require that these jumpers be set properly. Where a TRG1 module is used with a Model 575, the 575 trigger is functionally equivalent to a TRG1 module in slot 2. The TRG1 in the 575 option slot is functionally equivalent to a TRG1 in slot 3.

One Trigger Circuit

Jumper pins 1 to 2, and 3 to 4 to enable A/D triggering on the AMM module installed in slot 1.

Two Trigger Circuits

The use of two trigger circuits permits triggering A/D on (A or B) or (A and B).

LOGICAL OR (A or B) - Jumper pins 1 to 2 and 3 to 4 on the TRG1 in both slots.

LOGICAL AND (A and B) - Jumper pins 2 to 3 on the slot 2 TRG1. Jumper pins 1 to 2 and 3 to 4 on the slot 3 TRG1.

TRG1 Power-On State

The TRG1 module uses a power-up reset circuit to insure that the module energizes in a known state. All bits in the CMDA, CMDB, and CMDC control registers are set to 0, which results in the following power-up conditions:

The trigger voltage is 0V on the 1V range

Polarity is negative

No trigger input is selected

IRQ and A/D trigger are disabled

The trigger is set up for continuous mode on all events of the trigger condition

Trigger latching is disabled.

The 1MHz filter is selected

Trigger is set for falling edge and DC coupling.

TRG1 Commands and Command Locations

The command locations (control addresses) associated with the trigger function are Commands A, B, and C (CMDA, CMDB, and CMDC) for slots 2 and 3 of the 500A, 500P or Model 575. Any software packages which specifically support the TRG1 will normally communicate with these addresses directly, and the process will be transparent to the user.

In some cases, you may want to access the TRG1 command locations directly. An typical example might be where you are writing a program "from scratch" using only a general-purpose language such as BASIC, C, Assembler, etc.

See the following charts for detailed information.

TABLE 1. TRG1 COMMAND LOCATIONS AND FUNCTIONS

Read Functions:

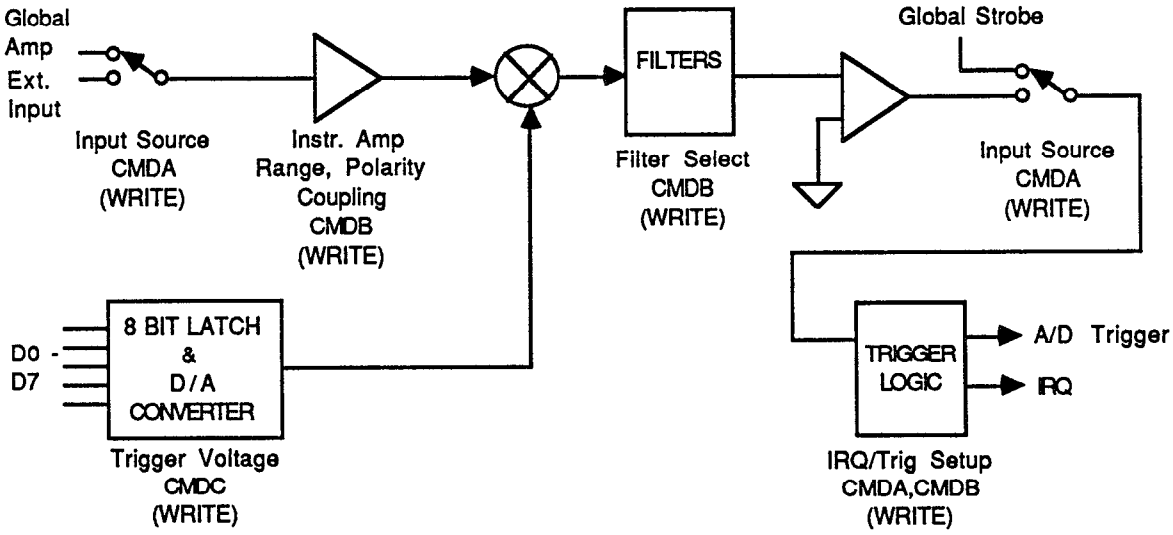
COMMAND	FUNCTION
CMDA	Read trigger status
CMDB	Read trigger status and reset TRG/IRQ latches

Write Functions:

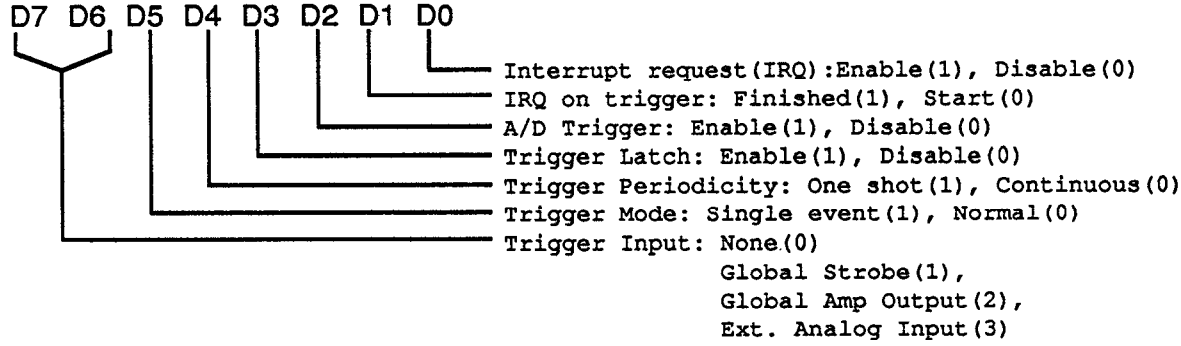
COMMAND	FUNCTION
CMDA	Interrupt and trigger setup
CMDB	Select filter, range, coupling, and edge
CMDC	Set trigger voltage

TABLE 1. TRG1 COMMAND LOCATIONS AND FUNCTIONS, cont'd

TRG1



CMDA (write) - IRQ and Trigger setup



CMDB (write) - Select Filter, Range, Coupling, Edge

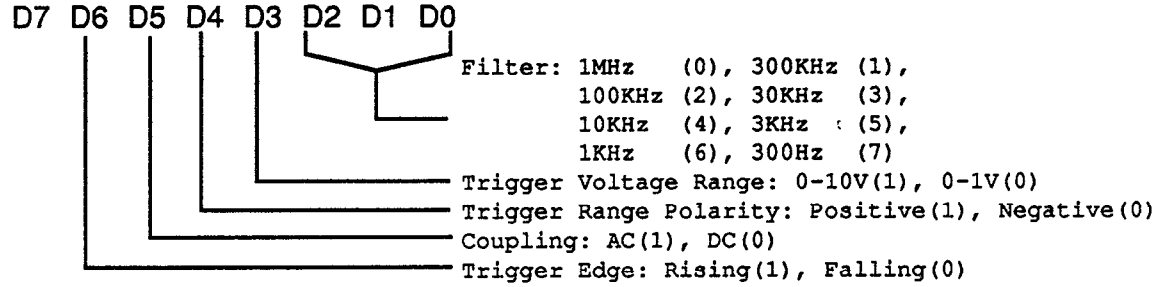
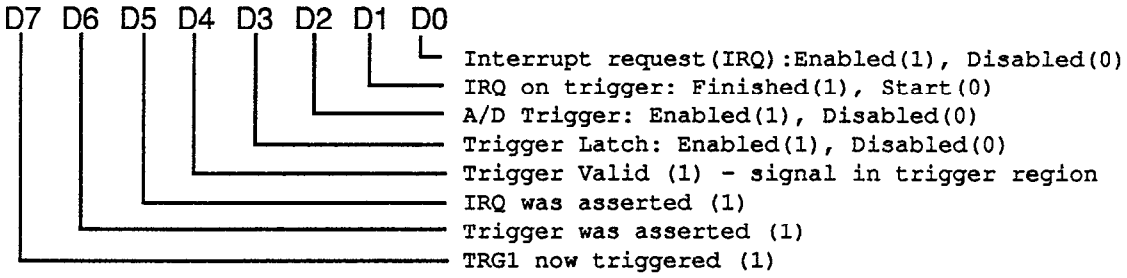


TABLE 1. TRG1 COMMAND LOCATIONS AND FUNCTIONS, concluded

CMDC (write) - Trigger Voltage (0 - 255)

CMDA (read) - Read Status



CMDB (read) - Reset Trigger and One Event Latch
Data same as CMDA Read Above

CMDC (read) - Not used

Command Locations in Numeric Order

The following information offers more details on the use of command locations for the TRG1 module, as well as applicable locations associated with the AMM1A and AMM2 analog input modules. The addresses shown presume that the TRG1 module is mounted in slot 2. For a TRG1 mounted in slot 3, use the second set of addresses which are shown in parentheses ().

The first three characters of each memory location are shown as "xxx". Normally, these characters would be "CFF", assuming that the IBIN interface card memory map switch is set for address CFF80.

For a further discussion of analog input commands, also refer to your AMM module manual.

CMD1A, Address xxx80 - SELECT A/D CHANNEL

The SELECT CHANNEL command is used to control the local signal multiplexer on the AMM module installed in slot 1. Refer to the appropriate AMM1A or AMM2 manual for a discussion of this command.

CMD1B, Address xxx81 - SELECT SLOT

The SELECT SLOT command controls the global multiplexer on the AMM module installed in slot 1. Refer to the appropriate AMM manual for a discussion of this command.

CMD2A, (CMD3A) - ANALOG TRIGGER AND IRQ CONFIGURATION

Control addresses are xxx82 for CMD2A, or xxx84 for CMD3A.

The analog trigger circuit can produce two separate outputs: a trigger signal that can start A/D conversion on the AMM module installed in slot 1, and an Interrupt Request (IRQ) that can divert the processor in the host PC to a servicing routine to perform programmed functions in the background.

Trigger input can come from any of 3 sources: from asserting a GLOBAL STROBE, from the external analog input (at J2), or from the output of the global amplifier on the AMM module in slot 1. The four possible selections for input include those mentioned above in addition to a no input setting, used at power up of the circuit.

Writing to this command location configures the interrupt request, trigger mode, and selects the trigger input for the analog trigger circuit. Reading this command location returns the contents of the trigger status register.

The triggering and IRQ output can operate in several modes. IRQ can be enabled or disabled, and asserted either on the beginning of a trigger condition, or when the trigger condition is no longer true. IRQ can operate even if the trigger is disabled. However, the triggering parameters must still be configured as if triggering were going to be used. Triggering can be enabled or disabled. The triggering can be latched or automatically reset. Additionally, the triggering can be used in one shot mode, where the trigger pulses for 500 nS when a triggering condition is satisfied; or in a continuous

mode where the trigger is latched into an asserted state until the triggering condition is no longer satisfied. Finally, the trigger can be set to trigger as a single event (where a reset must be performed before a trigger can be asserted again) or in a normal mode where the trigger asserts with each entry into the trigger region.

Reading from this location returns a byte that can be interpreted as the TRIGGER STATUS word. This should be used if status information is desired, but no reset of the trigger is to be asserted.

CMD2B, (CMD3B) - ANALOG TRIGGER INPUT CONFIGURATION

Control addresses are xxx83 for CMD2B, or xxx85 for CMD3B.

Writing to this command location allows the configuration of the input to the analog trigger circuit; selection of the input filter, trigger voltage range, trigger voltage polarity, input coupling, and triggering edge are selected by the appropriate binary data word. Reading this command location also returns the contents of the status register, and additionally performs a reset of the trigger and one event latch if the trigger is configured for one event or single mode triggering.

The main feature of the analog triggering circuit is its ability to provide a triggering signal with control similar to that of an oscilloscope. Therefore, the object input signal must be analyzed to determine if it meets a triggered condition. These conditions include input magnitude, input polarity, and whether the signal is on a rising edge or falling edge. These conditions, as well as filtering (8 ranges, from 300 Hz to 1 MHz) and input coupling, are selectable by writing to location CMD2B (CMD3B).

Performing a read of the CMD2B (CMD3B) location will return the same TRIGGER STATUS word as reading location CMD2A (CMD3A). However, reading the CMD2B (CMD3B) register will reset all the latches on the card.

CMD2C, (CMD3C) - ANALOG TRIGGER VOLTAGE (0-255 COUNTS)

Control addresses are xxx98 for CMD2C, or xxx99 for CMD3C.

Writing to this command location sets the output of the D/A converter in the analog triggering circuit to a voltage between 0 and 10 volts, with a resolution of approximately 47mV (1 part in 256). To determine the counts necessary, use the following formula:

$$\text{COUNTS} = \text{ABS}[(\text{VOLTS} / \text{RANGE}) \times 256]$$

where volts = the desired trigger voltage, range = the setting of the range bit (10V or 1V), and counts = number of DAC counts necessary for the desired output. This information must be written to CMDC for the desired slot.

Writing to this location sets the absolute magnitude at which triggering will occur in DAC counts. A conversion, based upon selected range and level, will give the proper number of counts (see the command description given above for the formula).

CMD1C, Address xxx9A - GLOBAL GAIN

The GLOBAL GAIN command controls the PGA (Programmable Gain Amplifier) located on the AMM module installed in slot 1. For a discussion of this command, refer to the appropriate AMM manual.

CMD1D, Address xxx9B - A/D START/STATUS

Writing to this command location starts A/D conversion on the AMM module installed in slot 1. Any value can be written to trigger conversion; however, a value of 255 should be written to minimize noise. Reading this location returns the status byte of the A/D conversion (busy or ready). A value of 255 (FF in hex) indicates that the conversion process is under way. A value of 127 (7F hex) indicates that the conversion is complete.

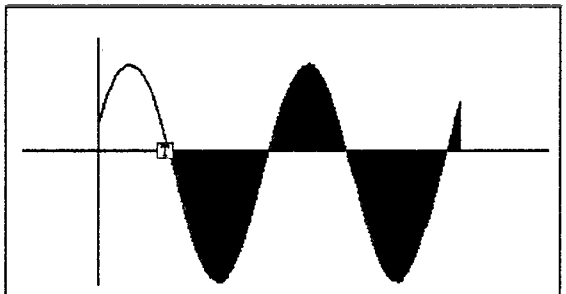
Typical Applications

The following examples illustrate some typical triggering modes. These are shown if Figure 4.

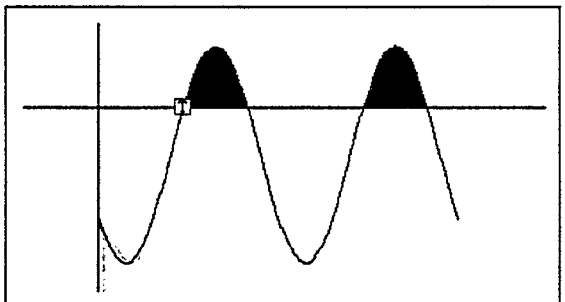
These routines can be implemented in any language by accessing the various command registers of the AMM and TRG1 modules. Higher level languages which support the TRG1 (such as KDAC500) will have commands which facilitate different trigger set-ups without requiring low-level access of the TRG1 and AMM command registers. The following information will still be useful in programming different trigger configurations.

The registers on the AMM1A or AMM2 module are identical, so all explanations are valid for both. In all the following examples, the program must go through four routines to acquire trigger-initiated data. The first example is described in detail. The other four examples note only the differences from the first example.

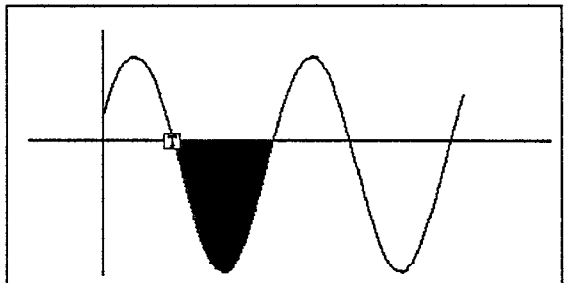
The first three examples presume that the input signal is a 6 Volt peak-to-peak 2 Hz sine wave connected to single-ended input channel 3 on the AMMx module. Triggering and acquisition are done on the same signal. The triggering threshold is set at +0.9 Volt.



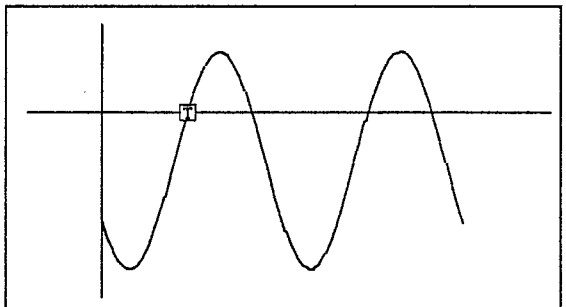
1. Trigger at a user-defined threshold on the falling slope of the trigger signal. Stop when the prescribed number of points have been acquired.



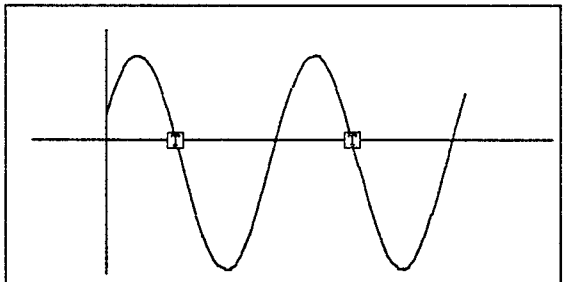
2. Trigger at a user-defined threshold on the rising slope of the trigger signal, and acquire data only when the signal is above the threshold. Stop when the prescribed number of points have been acquired.



3. Trigger at a user-defined threshold on the falling slope of the trigger signal, and acquire data only the first time the signal goes below the threshold level. Stop when the signal goes back up above the threshold



4. Trigger at a user-defined threshold on the rising slope of the trigger signal and take only one reading. *Normallly used to trigger a reading off of another channel.*



5. Trigger at a user-defined threshold on the falling slope of the trigger signal and acquire one reading. Repeat each time the trigger condition is satisfied until the prescribed number of points have been taken. *Normally used to synchronize readings to an external event.*

FIGURE 4. TYPICAL TRG1 TRIGGER MODES

Example 1. Trigger at a user-defined threshold on the falling slope of the trigger signal. Stop when the prescribed number of points has been acquired.

This example can be accomplished by a program which performs four main routines: setup, enabling of triggered acquisition, acquisition, and exit from the program.

Routine 1: Setup

The hardware is setup with the following sequence:

CMD1A (write) address xxx80, binary data = 01010011
CMD1B (write) address xxx81, binary data = 00110001
CMD2A (write) address xxx82: binary data = 10001000
CMD2B (write) address xxx83: binary data = 00010000
CMD2C (write) address xxx98: binary data = 11100110
CMD1A (read) address xxx80, discard data

(optional settling time loop here if needed)

The first two writes set up the AMMx card for the following conditions:

Bit	CMDA	CMDB
D0	Select channel 3	Select Slot 1
D1	"	"
D2	"	"
D3	"	"
D4	Single ended inputs	Read Data
D5	Local Gain X1	±10V Range
D6	50 kHz Auto Acquire	Global Gain X1
D7	100 kHz filter	(not used)

The next three writes set up the following conditions in the TRG1:

Bit	CMDA	CMDB
D0	IRQ disabled	1 MHz filter
D1	(don't care)	"
D2	A/D trigger disabled	"
D3	Trigger latching enabled	0 to 1 Volt range
D4	(don't care)	Positive range polarity
D5	(don't care)	DC coupling
D6	trigger input is	Falling slope
D7	global amp output	(not used)

CMDC data is figured to give a 0.9V threshold on the 1V range with the formula:

(0.9V / 1V) * 256 = 230 counts = binary 11100110

The read that follows the five writes is needed because the A/D converter must be reset and the previous old reading cleared out. This is done by reading an A/D data register and discarding the data.

The final step of the setup is waiting for the input filter to settle. The filter begins its settling time as soon as the initial setup conditions are written. Since this example uses the 1 MHz filter, the specified settling time is 1 μSec. More than 1 μSec elapses during the resetting process for the A/D converter, so no time delay is necessary for this example.

Routine 2: Enable Triggered Acquisition

Before acquisition is enabled, the program will typically test the TRG1 to determine if the input signal is out of the trigger region that was just set up. The test would be a loop as follows:

Loop: CMD2B (read) address xxx83, data is STATUS
If D4 of STATUS is 1, repeat Loop

This loop will wait for the input signal to be out of the trigger region before enabling the A/D. (If the input signal is in the trigger region when acquisition is enabled, acquisition will begin immediately. This is undesirable for this application.)

In this example, we have defined a trigger region of all voltages below +0.9 volts by setting the trigger threshold of +0.9 volts and selecting the falling slope. Bit D4 in the TRG1 status register indicates that the signal is in the trigger region. Reading CMDB on the TRG1 in a loop which repeats if bit D4 is 1 will continually reset the trigger circuit until the input signal leaves the trigger region.

Once D4 of the TRG1 Status register reads 0, the acquisition can be enabled. This is done by writing to the TRG1 CMDA register the same data as during setup with the exception that D2 bit will be a 1 to enable the A/D trigger. If the IRQ were also used, it would be enabled at the same time by setting D0 to a 1 also. The program should perform the following write:

CMD2A (write) address xxx82: binary data = 10001100

The acquisition will not begin until the trigger condition is satisfied.

Routine 3: Acquire data

The A/D status register is now polled to determine when a reading is completed. For this example, once the first reading has been triggered, the A/D will acquire readings at a 50 kHz rate until it is reset. The program must execute fast enough to be able to store readings at this acquisition rate.

A typical high speed acquisition program would perform the following steps:

Loop: CMD1D (read) address xxx9B, data is A/D STATUS
if D7 of A/D STATUS is a 1, repeat Loop

CMD1A (read) address xxx80, data is A/D low data byte
CMD1B (read) address xxx81, data is A/D high data byte

Store both A/D data bytes to memory

Routine 4: Exit

After every A/D data reading is stored, a test must be made to determine if the prescribed number of data points has been acquired. The program must:

Increment memory pointer, stop acquisition if enough data has been acquired. Otherwise, go back to Loop for next reading if not done.

The acquisition process is stopped when the desired number of readings have been taken.

Example 2. Trigger at a user-defined threshold on the rising slope of the trigger signal, and acquire data only when the signal is above the threshold. Stop when the prescribed number of points has been acquired.

This example is implemented the same way as the first example with the exception of the data written to the TRG1 in the setup routine. The setup for this example would be:

CMD1A (write) address xxx80, binary data = 01010011
CMD1B (write) address xxx81, binary data = 00110001
CMD2A (write) address xxx82: binary data = 10000000
CMD2B (write) address xxx83: binary data = 01010000
CMD2C (write) address xxx98: binary data = 11100110
CMD1A (read) address xxx80, discard data

(optional settling time loop here if needed)

There is a difference in the data written to address xxx82 and address xxx83. The D3 bit in CMDA is 0, which disables the trigger latching function, and bit D6 in CMDB is 1, which selects the rising slope. The trigger region is defined as voltages above +0.9 volts, and acquisition will proceed at a 50 kHz rate whenever the trigger voltage is above that level. Acquisition will halt when the trigger voltage falls below that level. This starting and stopping will continue until the prescribed number of samples has been taken.

Example 3. Trigger at a user-defined threshold on the falling slope of the trigger signal, and acquire data only the first time the signal goes below the threshold level. Stop when the signal goes above the threshold level.

This example operates the same way as example 1 with the exception of the way the acquisition process is terminated. The TRG1 will enable the A/D to take readings the first time the trigger signal falls below the threshold. The acquisition will proceed at a 50 kHz rate until the trigger signal rises above the trigger threshold. The TRG1 will then stop the acquisition and latch itself off, preventing further acquisition until it is reset.

There are two choices for how to terminate the program. The first choice has the program poll the TRG1 during the acquisition to determine when acquisition is to be stopped, and the second choice uses the IRQ to interrupt the computer when acquisition is finished. Both choices are described below.

The first choice requires adding a test to the acquisition loop which polls the A/D for conversion done, then reads the A/D and stores the reading to memory. A second test is added to the loop just after the test for A/D conversion done which reads the TRG1 CMDA status register, and stops acquisition when bit D7 is a 0. A drawback to this approach is the additional time is required to execute the additional code. Slower computers may not be able to execute the loop fast enough to keep up with the 50 kHz acquisition rate.

An implementation of the first choice requires changing the setup and acquire data routines as follows:

Routine 1: Setup

CMD1A (write) address xxx80, binary data = 01010011
CMD1B (write) address xxx81, binary data = 00110001
CMD2A (write) address xxx82: binary data = 10100000
CMD2B (write) address xxx83: binary data = 00010000
CMD2C (write) address xxx98: binary data = 11100110
CMD1A (read) address xxx80, discard data

(optional settling time loop here if needed)

Routine 3: Acquire data

Begin:	CMD1D (read) address xxx9B, data is A/D STATUS if D7 of A/D STATUS is a 0, go to Read: if D7 of A/D STATUS is a 1, go back to Begin

Loop:	CMD1D (read) address xxx9B, data is A/D STATUS
	if D7 of A/D STATUS is a 0, go to Read:
	if D7 of A/D STATUS is a 1, go to Done?:

Done?:	CMD2A (read) address xxx82: data is TRG1 STATUS if D7 of TRG1 STATUS is a 1, repeat Loop if D7 of TRG1 STATUS is a 0, stop acquisition
Read:	CMD1A (read) address xxx80, data is A/D low data byte CMD1B (read) address xxx81, data is A/D high data byte

Store both A/D data bytes to memory

The only difference in the setup routine is in CMDA of the TRG1. D3 is a 0, which disables the trigger latching, and D5 is a 1, which selects the single event mode. The changes in the acquire data routine are more extensive. The first three lines cause the program to wait for the trigger condition to become true before the first reading is taken. The next six lines take subsequent readings as long as the trigger signal is in the defined trigger region, and stops the acquisition when the signal goes out of the trigger region.

The second choice is to use the IRQ to interrupt the computer when the acquisition is completed. The TRG1 is set up to generate an IRQ when the trigger signal leaves the trigger region. The IBIN-A must be wired to pass through interrupts from the TRG1 to the computer's bus by installing jumper W2 on the IBIN-A. The user must turn off other interfering interrupts in the computer before enabling triggering, and must write an interrupt service routine to handle the IRQ generated by the TRG1. The IBIN-PS/2 does not support interrupts from the data acquisition mainframe at the time of this writing.

This example is setup as follows:

Routine 1: Setup

CMD1A (write) address xxx80, binary data = 01010011
CMD1B (write) address xxx81, binary data = 00110001
CMD2A (write) address xxx82: binary data = 10100010
CMD2B (write) address xxx83: binary data = 00010000
CMD2C (write) address xxx98: binary data = 11100110
CMD1A (read) address xxx80, discard data
CMD1B (read) address xxx81, discard data

(optional settling time loop here if needed)

Routine 2: Enable Triggered Acquisition

Loop: CMD2B (read) address xxx83, data is STATUS
If D4 of STATUS is 1, repeat Loop

CMD2A (write) address xxx82: binary data = 10100111

The setup routine is different from example 1 only in the data written to the TRG1 CMDA register. D1 is a 1, which selects an IRQ on the conclusion of the triggered acquisition, D3 is a 0, which disables the trigger latching, and D5 is a 1, which selects the single event mode.

The enable triggered acquisition routine the similar to example 1 except for the data written to the TRG1 CMDA. The IRQ enable bit D0 of the TRG1 is set to 1 at the same time as the A/D trigger enable bit D2 is set to 1 to enable the triggering.

The following two examples presume that the trigger signal and the signal to be acquired are different. The input signal is connected to single-ended input channel 12 on the AMMx module. The triggering signal is a 6 Volt peak-to-peak 2 Hz sine wave connected to the External Analog Input of the TRG1. Only the triggering signal is shown in the figure accompanying the examples. The triggering threshold is set to +0.9 Volt.

Example 4. Trigger at a user-defined threshold on the rising slope of the trigger signal and take only one reading. (Normally used to trigger a reading of another channel.)

This example will work with any computer, since execution speed is not important. Only one reading is acquired, but it is taken within 1 μSec of the trigger condition being satisfied. In a typical application, the trigger signal will be connected to the external input of the TRG1, and a different signal is actually measured by the A/D. Once the one reading is taken, the program can proceed to a different setup and take other readings if needed.

Routine 1: Setup

The hardware is setup with following sequence:

CMD1A (write) address xxx80, binary data = 01011100
CMD1B (write) address xxx81, binary data = 00110001
CMD2A (write) address xxx82: binary data = 11110000
CMD2B (write) address xxx83: binary data = 01010000
CMD2C (write) address xxx98: binary data = 11100110
CMD1A (read) address xxx80, discard data

(optional settling time loop here if needed)

The differences between the setup routine of example 1 and this example are as follows. The AMMx CMDA data bits D0, D1, D2, and D3 have been changed to select single ended channel 12 as the input to be acquired. The TRG1 CMDA and CMDB have been changed to select the following conditions:

Bit	CMDA	CMDB
D0	IRQ disabled	1 MHz filter
D1	(don't care)	"
D2	A/D trigger disabled	"
D3	Trigger latching disabled	0 to 1 Volt range
D4	One Shot periodicity	Positive range polarity
D5	Single Event mode	DC coupling
D6	trigger input is	Rising slope
D7	Ext Analog Input	(not used)

The TRG1 CMDC is still set for a 0.9 volt threshold, as in example 1.

Routine 2: Enable Triggered Acquisition

The acquisition is enabled the same way as in example 1:

Loop: CMD2B (read) address xxx83, data is STATUS
If D4 of STATUS is 1, repeat Loop

CMD2A (write) address xxx82: binary data = 11110100

The data written to CMDA reflects the different setup for this example.

The acquire data routine is the same as in example 1. This example will only acquire one data point, however.

Routine 4: Exit

There is no exit routine required by this example, since the setup used causes acquisition to stop after one reading is acquired. The one reading acquired will remain in the AMMx data buffer until it is read by the program, and further acquisition is initiated.

Example 5. Trigger at a user-defined threshold on the falling slope of the trigger signal and acquire one reading. Repeat each time the trigger condition is met until the prescribed number of points has been acquired. (Normally used to synchronize readings with an external event)

The setup for example 5 is the same as the setup for example 4, with the exception that the TRG1 CMDA bit D5 is set to a 0. This allows automatic reset of the triggering latch so that one reading will be acquired every time the signal crosses the prescribed trigger threshold of 0.9 volts on the falling slope of the trigger signal.

The enable triggered acquisition routine is the same as that for example 1, with the exception that the data used for the TRG1 CMDA reflects the setup data for this example with bit D2 set to a 1.

The acquire triggered data routine and exit routine are exactly the same as in example 1. The program will operate slightly differently, since the data acquisition rate will not be fixed at 50 kHz. The data will be acquired at a rate determined by the repetition frequency of the triggering signal, with one reading being taken every time the triggering signal crosses the trigger threshold going from above to below the threshold.

Calibration Procedure

There are no calibration procedures associated with the TRG1 module. However, the +10V precision reference of the AMM1A or AMM2 must be properly calibrated to insure accurate operation of the TRG1. The AMM module is calibrated at the factory, and will require additional calibration only if you specifically suspect a malfunction, or are performing an AMM module repair. Calibration is covered in the AMM module manual.

NOTE: If a function which had been working correctly suddenly becomes inaccurate by more than a few percent, the problem is more likely a malfunction and not a calibration problem. If you cannot calibrate your hardware after two attempts, you should return it to Keithley for repair or calibration at the factory.

Troubleshooting

This section contains information to aid in troubleshooting the TRG1. Any suspected or observed problem with the TRG1 module may result from malfunctions in any part of the total system. If you have spares, a suspected faulty system component can usually be verified most easily through simple substitution. The hierarchy of possible problem areas includes the following items. Refer to your data acquisition mainframe manual for additional instructions on troubleshooting the computer, interface card, cable, and mainframe.

1. Faulty software or applications programs - If a program which had been running properly begins to behave erratically, there is a possibility that either the supporting software package or the application program may have been corrupted. Compare your software files and application program to a back-up copy, or re-run an earlier, known good version of the software. If you have completed a new program which does not work as anticipated, review the program design and be certain that it actually will function as you assume.

2. Faulty computer - A malfunctioning computer or peripheral may have effects on the data acquisition software and hardware ranging from minor problems to total failure. These problems may be continuous or intermittent. If you suspect your computer, remove the data acquisition interface and run any diagnostics which came with the system to verify the computer's performance. Also try running other software with which you are familiar.

3. Defective data acquisition interface - A bad interface may prevent the computer from booting up and operating properly, or it can affect only the data acquisition system. Some monitor adapters and networking adapters may conflict with the Keithley interface. Such problems may result from address or interrupt conflicts, and will appear with both cards plugged into a system which otherwise operates properly with only one of the cards in place. Parity errors or other diagnostic error messages may result when the system is powered up. You can usually determine incompatibility by trying each suspected card individually, and then together in the system. Such incompatibility can often be overcome through switch settings or other configuration changes.

4. Defective data acquisition interface cable - Open conductors in a cable may disrupt the communication of essential power, control, or data signals. Cable shorts, especially in lines carrying system power supply voltages, may cause a total shutdown of the computer or data acquisition mainframe. You may note erratic operation of the computer, or a failure of the indicator lamps on the data acquisition system to light. If these problems exist, try disconnecting the interface cable from the computer and data acquisition system.

5. Defective data acquisition mainframe - Any and all data acquisition functions may malfunction if the mainframe is defective. The mainframe operations can be subdivided into analog and digital functions. An analog or digital failure may occur, leaving the other function unaffected. Analog input for any slot relies on the A/D converter and programmable gain amplifier of the analog master measurement module. If only the analog functions are faulty, you should also consider the A/D module.

An individual slot may also be bad. A known good module can be tried in various slots to determine the condition of individual mainframe slots.

6. Defective module(s) in the data acquisition system - With the exception of the AMM module, a malfunctioning module should not affect the TRG1 unless its address, data, or control circuitry has failed in such a way that it affects the data acquisition motherboard or power supply. If a faulty module is causing a data acquisition system to malfunction, you may be able to determine the faulty module by removing modules individually until the problem clears.

7. Defective TRG1 module - The TRG1 module can be verified to the module level by using it in conjunction with an AMM1A or AMM2 module. Use a known-good AMM module, or first check your AMM module for proper operation. Use KDAC500 or another software package with which you are familiar to write a few simple test programs for the TRG1. If the module does not perform as expected, you may assume that the module is defective. Since the TRG1 has no calibratable components, a problem at this point will normally indicate a failure within the TRG1 module.

A skilled technician who has access to electronic test equipment may then be able to troubleshoot individual circuits on the TRG1 to isolate the faulty parts. A full parts list and diagram set are included elsewhere in this manual to aid the technician.

If a defective component is found, replacement parts may be obtained from Keithley. If factory service is desired, the TRG1 module may be returned for repair. The TRG1 is warranted against defects in material and workmanship for a period of 1 year. For information on replacement parts or factory service, see the Parts List section of this manual.

Parts List

This section contains replacement parts information, component location drawings and schematic diagrams for the TRG1 module. Parts are listed alphanumerically in order of their circuit designations. You may obtain spares from Keithley Instruments, Inc., 28775 Aurora Road, Cleveland, OH 44139.

MODEL No: 500-TRG1 ANALOG TRIGGER MODULE

Part No.	Quantity	Title	Designation
C-305-.047	1	Cap, .047uF, 20%, 100V, polyester	C1
C-306-.001	1	Cap, .001uF, 10%, 100V, polypropylene	C2
C-365-.1	16	Cap, .1uF, 20%, 50V, ceramic	C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20
C-64-150P	2	Cap, 150pF, 10%, 1000V, ceramic	C3, C4
CS-339-2	2	Conn, 2 pin	J3, J4
CS-339-4	1	Conn, 4 Pin	W1
CS-553	2	Pin, test point	TP1, TP2

CS-521-1	1	Conn, strip, 3 pin	J2
IC-144	1	IC, dual D-type flip flop, 74LS74	U21
IC-163	2	IC, quad 2 input NAND, 74LS00	U16, U25
IC-173	3	IC, voltage comparator, LM311N	U9, U10, U27
IC-179	1	IC, quad 2 input NOR, 74LS02	U12
IC-186	1	IC, hex inverter, 74LS04	U11
IC-215	1	IC, quad 2 input pos AND, 74LS08	U19
IC-230	1	IC, octal buffer/line driver, 74LS244	U26
IC-231	1	IC, quad 2 input NAND, 74LS03	U22
IC-233	1	IC, triple 3 input NOR, 74LS27	U20
IC-246	2	IC, 18v OP-amp, 353	U6, U7
IC-263	3	IC, octal D-type latch, 74LS273	U13, U14, U24
IC-267	1	IC, 8 ch CMOS analog multi, 6108	U5
IC-320	2	IC, SPST CMOS analog switch, DG211	U1, U3
IC-321	1	IC, 8 bit DAC, AD7523	U8
IC-357	1	IC, octal D-type latch, 74LS373	U15
IC-386	2	IC, dual 4 to 1 data selector, 74LS153	U18, U23
IC-504	2	IC, dual JFET OP-amp, 412	U2, U4
IC-558	1	IC, dual one-shot, 74LS221	U17
R-176-8.76k	1	Res, 8.76k, .1%, 1/8w, metal film	R40
R-263-20k	8	Res, 20k, .1%, 1/10w, metal film	R8, R9, R10, R11, R20, R21, R22, R23
R-76-100	2	Res, 100, 5%, 1/4w, composition or film	R41, R42
R-76-100k	3	Res, 100k, 5%, 1/4w, composition or film	R12, R29, R30
R-76-10m	1	Res, 10m, 5%, 1/4w, composition or film	R3
R-76-1k	2	Res, 1k, 5%, 1/4w, composition or film	R1, R2
R-76-390	3	Res, 390, 5%, 1/4w, composition or film	R27, R28, R43
R-76-39k	1	Res, 39k, 5%, 1/4w, composition or film	R35
R-76-4.7k	8	Res, 4.7k, 5%, 1/4w, composition or film	R25, R26, R31, R32, R33, R34, R39, R44
R-76-470k	2	Res, 470k, 5%, 1/4w, composition or film	R24, R38
R-88-1.33k	1	Res, 1.33k, 1%, 1/8w, metal film	R14
R-88-150k	1	Res, 150k, 1%, 1/8w, metal film	R18
R-88-15k	1	Res, 15k, 1%, 1/8w, metal film	R16
R-88-301	1	Res, 301, 1%, 1/8w, metal film	R13
R-88-37.4k	1	Res, 37.4k, 1%, 1/8w, metal film	R36
R-88-4.99k	2	Res, 4.99k, 1%, 1/8w, metal film	R15, R37
R-88-49.9k	3	Res, 49.9k 1%, 1/8w, metal film	R4, R5, R17
R-88-499k	1	Res, 499k, 1%, 1/8w, metal film	R19
R-88-5.49k	2	Res, 5.49k, 1%, 1/8w, metal film	R6, R7
RF-28	7	Diode, silicon, 1N148 (DO-35)	D1, D2, D3, D4, D5, D6, D7
TG-47	1	Trans, NPN silicon, 2N3904 (TO-92)	Q1
TG-84	1	Trans, PNP, silicon, 2N3906 (TO-92)	Q2
6-32x1/2pph	2	Screw	
500-323	1	Cable clamp assy	
500-321	1	Cable clamp	
500-322	1	Strip rubber	
500-322	1	Strip rubber	
501-917-00A	1	Manual package	
501-917-01A	1	Manual	

To place an order, or obtain information concerning replacement parts, first contact the Keithley customer service department at (216)248-0400. When ordering parts, include the following information:

1. Model Number

2. Serial Number

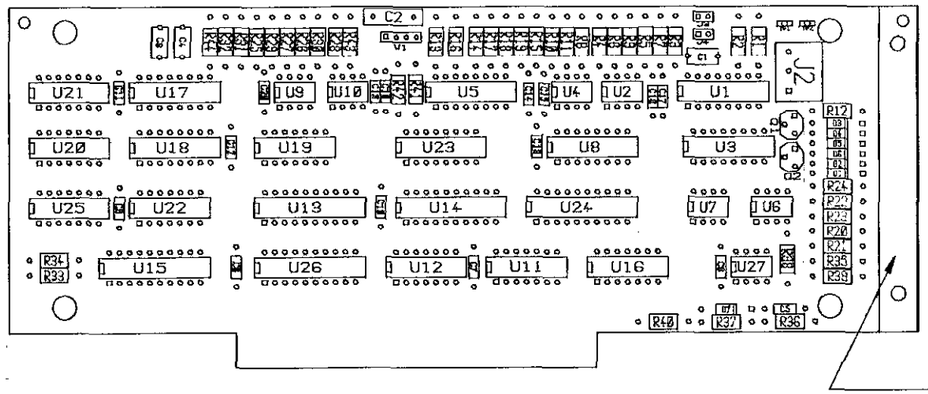
3. Part Description

4. Circuit Designation (if applicable)

5. Keithley Part Number

If an additional instruction manual is required, order the manual package, Keithley Part Number 575-917-01 Rev * ("*" indicates the revision level; the latest revision will be supplied). The manual package contains an instruction manual and any applicable addenda.

LTR	ECO NO.	REVISION	ENG.	DATE
A	13444	RELEASED	SAS	4-27-89
B	13537	ADD C41 - C25, R46 - R44, J1 AND REVISE ARTWORK	SAS	6-21-89



500-322
500-323
6-32X1/2"PPH (2 REQD)

NOTE:
FOR COMPONENT INFORMATION,
REFER TO BILL OF MATERIALS
(501-988)

MODEL	NEXT ASSEMBLY	QTY USED ON
500	500-TRG1	

DO NOT SCALE THIS DRAWING

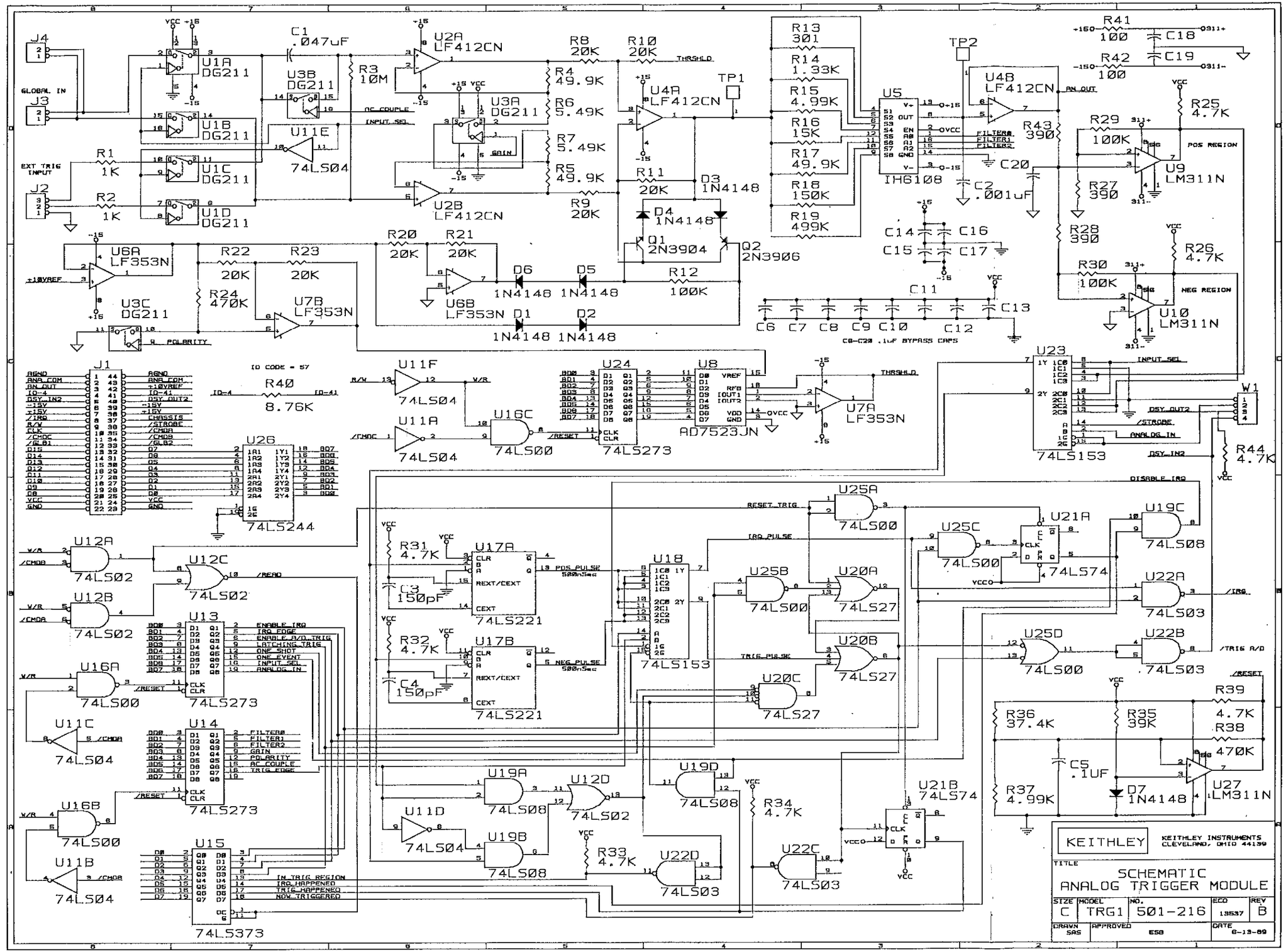
KEITHLEY Keithley Instruments Inc. Cleveland, Ohio 44139

DIMENSION TOLERANCES UNLESS OTHERWISE SPECIFIED
XX=+/-.015 ANG.=+/-1°
XXX=+/-.005 FRAC.=+/-1/64
SURFACE MAX. 63

DATE 6-13-89 | SCALE 1:1
DRN. SAS | ENG. APPR.
MATERIAL N/A
FINISH N/A

TITLE COMPONENT LAYOUT, ANALOG TRIGGER MODULE

C | NO. 501-210


GLOBAL IN
EXT TRIG INPUT
U1A DG211
U1B DG211
U1C DG211
U1D DG211
U3B DG211
U11E 74LS04
U2A LF412CN
U2B LF412CN
U3A DG211
U4A LF412CN
U4B LF412CN
U5 IH6108
U6A LF353N
U6B LF353N
U3C DG211
U7B LF353N
U7A LF353N
U8 AD7523JN
U9 LM311N
U10 LM311N
C1 .047uF
C2 .001uF
C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20
C8-C20 .1uF BYPASS CAPS
R1 1K
R2 1K
R3 10M
R4 49.9K
R5 49.9K
R6 5.49K
R7 5.49K
R8 20K
R9 20K
R10 20K
R11 20K
R12 100K
R13 301
R14 1.33K
R15 4.99K
R16 15K
R17 49.9K
R18 150K
R19 499K
R20 20K
R21 20K
R22 20K
R23 20K
R24 470K
R25 4.7K
R26 4.7K
R27 390
R28 390
R29 100K
R30 100K
R41 100
R42 100
R43 390
THRSHLD
NC COUPLE
INPUT SEL
GAIN
POLARITY
AC COUPLE
TRIG EDGE
FILTER0
FILTER1
FILTER2
AN OUT
POS REGION
NEG REGION
D1 1N4148
D2 1N4148
D3 1N4148
D4 1N4148
D5 1N4148
D6 1N4148
Q1 2N3904
Q2 2N3906
J1
J2
J3
J4
ID CODE = 57
R40 8.76K
ID-4
ID-41
U11F 74LS04
U11A 74LS04
U16C 74LS00
U24 74LS273
U26 74LS244
U23 74LS153
W1
R44 4.7K
DSY OUT2
/STROBE
ANALOG IN
DSY IN2
INPUT SEL
DISABLE IRQ
U25A 74LS00
U25B 74LS00
U25C 74LS00
U25D 74LS00
U21A 74LS74
U21B 74LS74
U19C 74LS08
U19D 74LS08
U22A 74LS03
U22B 74LS03
U22C 74LS03
U22D 74LS03
U20A 74LS27
U20B 74LS27
U20C 74LS27
/IRQ
/TRIG A/D
/RESET
RESET TRIG
IRQ PULSE
TRIG PULSE
U12A 74LS02
U12B 74LS02
U12C 74LS02
/READ
U13 74LS273
U14 74LS273
U15 74LS373
ENABLE IRQ
IRQ EDGE
ENABLE A/D TRIG
LATCHING TRIG
ONE SHOT
ONE EVENT
INPUT SEL
ANALOG IN
IN TRIG REGION
IRQ HAPPENED
TRIG HAPPENED
NOW TRIGGERED
U17A 74LS221
U17B 74LS221
U18 74LS153
R31 4.7K
R32 4.7K
R33 4.7K
R34 4.7K
C3 150pF
C4 150pF
C5 .1UF
R35 39K
R36 37.4K
R37 4.99K
R38 470K
R39 4.7K
D7 1N4148
U27 LM311N
KEITHLEY
KEITHLEY INSTRUMENTS
CLEVELAND, OHIO 44139
SCHEMATIC
ANALOG TRIGGER MODULE
SIZE C
MODEL TRG1
NO. 501-216
ECO 19537
REV B
DRAWN SAS
APPROVED ESB
DATE 6-13-89