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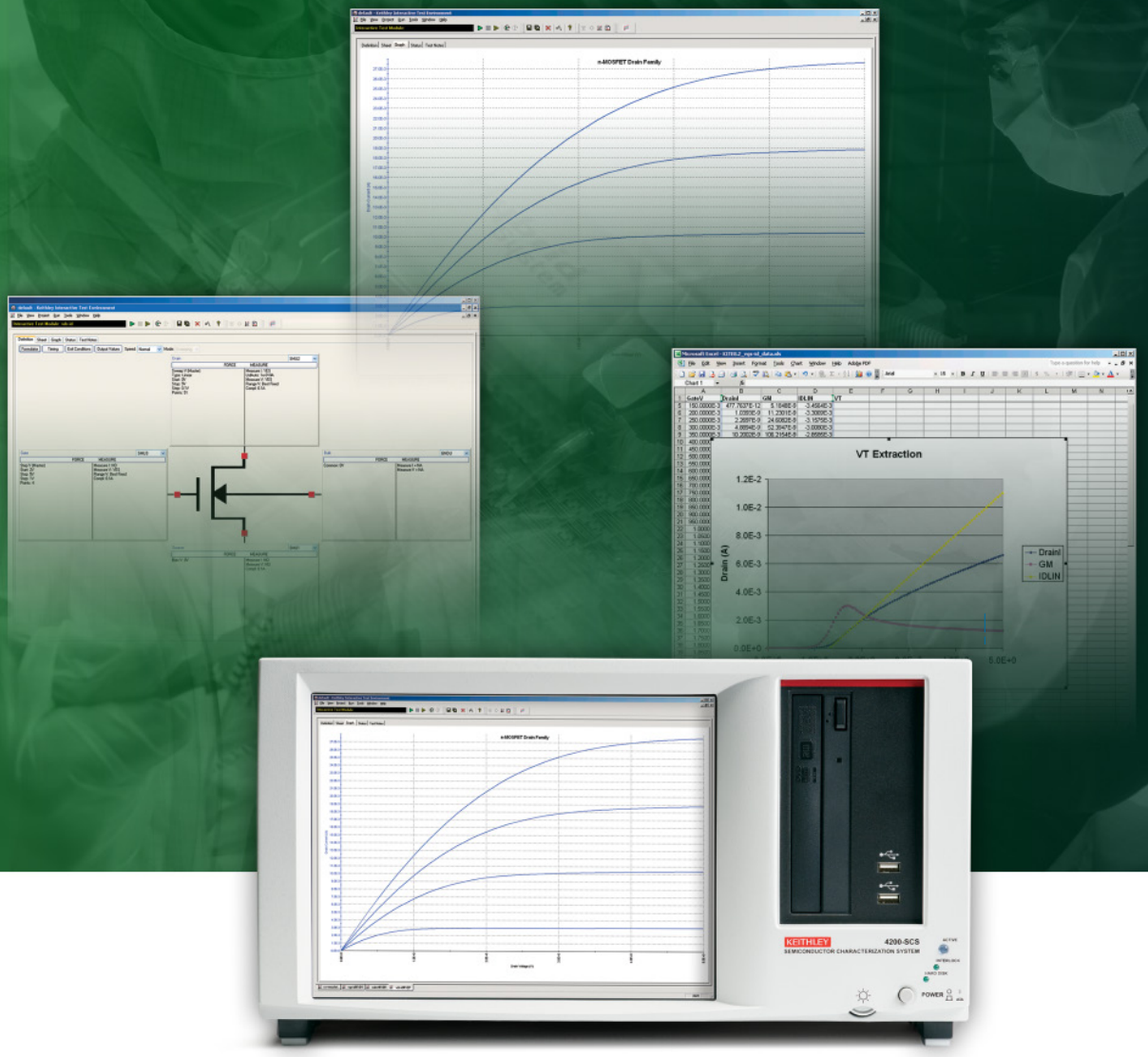
APPLICATIONS GUIDE



DC I-V Testing for Components and Semiconductor Devices

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KEITHLEY
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DC I-V Testing for Components and Semiconductor Devices

DC I-V measurements are the cornerstone of device and material testing. This DC I-V testing applications e-guide features a concentration of application notes on DC I-V testing methods and techniques using Keithley's Model 4200-SCS Parameter Analyzer. The Model 4200-SCS provides a wide range of I-V measurements including sub-pA leakage measurements and μΩ resistance measurements.

Contents

Optimizing Low Current Measurements with the Model 4200-SCS Parameter Analyzer

Introduction

Many critical applications demand the ability to measure very low currents—such as picoamps or less. These applications include determining the gate leakage current of FETs, testing sensitive nano-electronic devices, and measuring leakage current of insulators and capacitors.

The Model 4200-SCS Parameter Analyzer, when configured with the optional Model 4200-PA Remote Preamp, offers exceptional low current measurement capability with a resolution of 1E–16A. Making low current measurements successfully depends not only on using a very sensitive ammeter like the Model 4200-SCS's, but on choosing the proper settings in the system's Keithley Interactive Test Environment (KITE) software, using low noise fixtures and cabling, allowing sufficient settling time, and using techniques that prevent unwanted currents from reducing measurement accuracy. This application note describes Keithley's best-known methods recommendations for optimizing low current measurements using the Model 4200-SCS.

Measuring the Offset Current of the System

One of the first steps in setting up a system for making ultra-low current measurements is to determine the offset and leakage current of the entire measurement system, which includes the 4200-SCS itself, the connecting cables, switch matrix, test fixtures, and probes. This identifies the noise floor limit of the entire system and sets a starting point for making improvements to the system, if possible. Start by measuring the offset of the source measure unit (SMU) instruments and then continue to add components of the measurement circuit until everything is connected except the device under test (DUT). The measurements are made directly by the 4200-SMU with the 4200-PA Remote PreAmp using the KITE software.

Internal Offsets

The ideal ammeter should read zero current when its input terminals are left open. Practical ammeters, however, do have some small current that flows when the input is open. This current, which is known as the input offset current, is generated by bias currents of active devices and by leakage currents through insulators within the instrument. The offset current generated within the SMU instrument is included in the Model 4200-SCS's specifications. As shown in ***Figure 1***, the input offset current adds to the measured current so the meter measures the sum of the two currents:

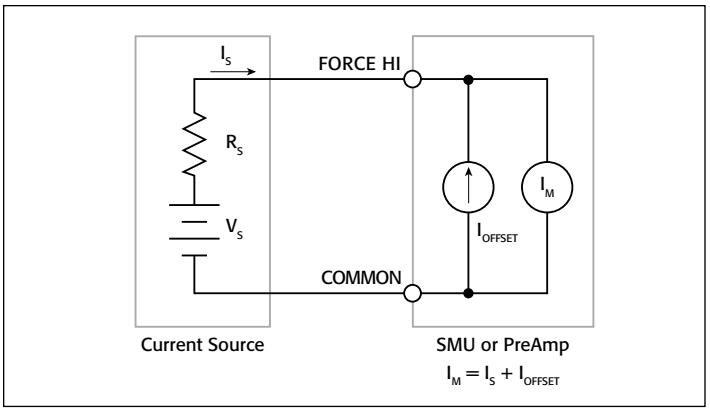


Figure 1. Input Offset Current of SMU Instrument

The offset of each 4200-SMU with the 4200-PA preamp is measured with nothing connected to the Force HI and Sense HI terminals except metal caps. These three-lug metal caps are included with the system. Before taking any measurements, the SMU instruments should be warmed up with the metal caps connected to the Force HI and Sense HI terminals of the preamps for at least one hour. If the system has KTEI software version 7.1 or later installed, the offset current can be measured using the project called "*LowCurrent*" located on the system in this directory: *C:\S4200\kiuser\Projects\LowCurrent*

Open this project and select the *SMU1offset* ITM. Click on the graph tab and run the test. The results should be similar to the graph shown in ***Figure 2***. It may be necessary to use the Auto Scale function to scale the curve appropriately. The Auto Scale function can be found by right-clicking on the graph. With the 4200-PA preamp connected to the SMU instrument, the offset current should be in the femtoamp range. The current offset can be positive or negative. Verify these results with the published ammeter specifications for the Model 4200-SCS.

This test should be repeated using a separate ITM for each SMU instrument in the system. The *LowCurrent* project has ITMs for performing offset current measurements on four SMU instruments with preamps.

It is also easy to measure the offset current for systems running versions of the KTEI software earlier than 7.1. Follow these steps to create a test to perform this measurement on SMU1:

1. Within a project that has already been created, open a new Device Plan for a generic 2-terminal device.
2. Create a new ITM called *SMU1Offset*. Select SMU1 for terminal A and the GNDU for terminal B.

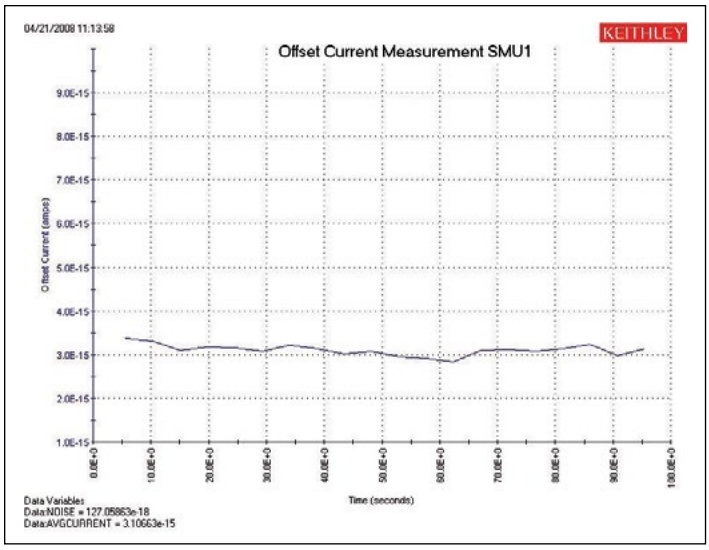


Figure 2. Offset Current Measurement of SMU1

3. Set up the following in the Definition Tab:

   SMU Force/Measure Configuration: Voltage bias 0V, 10pA fixed current range.

   Timing Menu: Quiet Speed, Sampling Mode, 0s Interval, 20 Samples, 1s Hold Time, Timestamp Enabled checked

   Formulator: Create a formula to measure noise using the standard deviation function, NOISE=STDDEV(A1).

   Also create a formula to measure the average offset current: AVGCURRENT=AVG(A1).

4. Set up the following in the Graph Tab (right-click on graph):

   Define Graph: X-axis: Time
   Y1-axis: Current (A1)

   Data Variables: Select NOISE to appear on graph. Select AVGCURRENT to appear on graph.

Once the test is configured, save the test and run it. The results should be similar to those shown in ***Figure 2***. Repeat the test for all the SMU instruments in the system.

The input offset current specification can be optimized by performing an auto calibration procedure in KITE. To perform an SMU auto calibration, go to the KITE Tools menu and click on SMU Auto Calibration. Before performing the auto calibration, allow the system to warm up for at least 60 minutes after power-up. Nothing should be connected to the SMU Force HI and Sense HI terminals except a metal cap. The auto calibration routine adjusts the current and voltage offsets for all source and measurement functions of all SMU instruments in the system. This should not be confused with a full system calibration, which should be performed once per year at the Keithley factory.

The offset current measurement can be repeated once the SMU auto calibration has been performed.

External Offsets

Once the offset current of the ammeter has been determined, verify the offset of the rest of the system by repeating (using the Append Run button shown in ***Figure 3***) the current (at zero volts) vs. time graph after adding each piece of the test circuit. Finally, make a measurement to the end of the probe in the "up" position or to the test fixture with no device connected. This process will help determine any trouble spots, such as a shorted cable or instability in the measurement circuit. However, be aware that connecting and disconnecting cables generates current in the circuit. For making ultra-low current measurements, it may be necessary to wait from a few minutes to hours for the spurious currents to decay after changing connections in the test circuit. ***Figure 4*** illustrates a graph showing the offset of 1) just the SMU instrument with a capped Force HI terminal, 2) with only a triax cable on the preamp, and finally 3) through the Keithley 7174A Low Current Switch Matrix to a probe station with a probe in the "up" position.

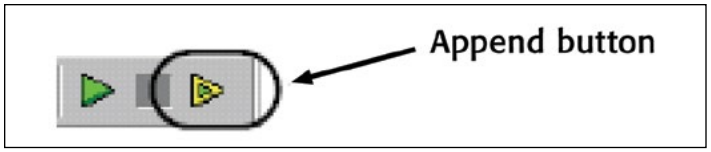


Figure 3. Append button

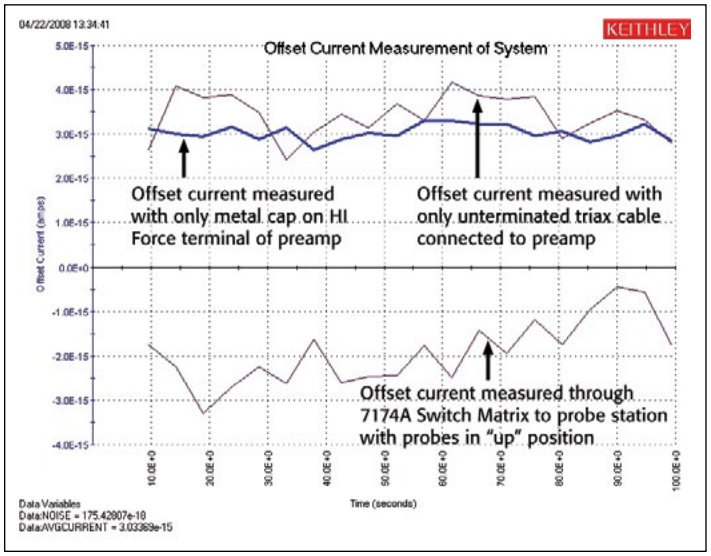


Figure 4. Offset Current Measurement of Entire Test System

This test should be repeated to determine any leakage circuit in the measurement circuit by applying a test voltage when generating the current vs. time graph. Rather than applying a zero volt bias, use the test voltage that will be used in the actual measurements of the DUT. Any leakage current in the test fixtures and cables will now be measured and graphed. If the leakage appears to be too high, adjustments can be made to the measurement circuit to reduce the leakage current. Refer to the section titled "Leakage Current and Guarding," which describes ways to reduce leakage current.

Sources of Measurement Errors and Ways to Reduce Them

Once the current offsets, leakage current, and any instability have been determined, taking steps to reduce measurement errors will help improve measurement accuracy. These sources of error include insufficient settling time, electrostatic inference, leakage current, triboelectric effects, piezoelectric effects, contamination, humidity, ground loops, light, and source impedance. ***Figure 5*** summarizes the magnitudes of some of the generated currents discussed in this section.

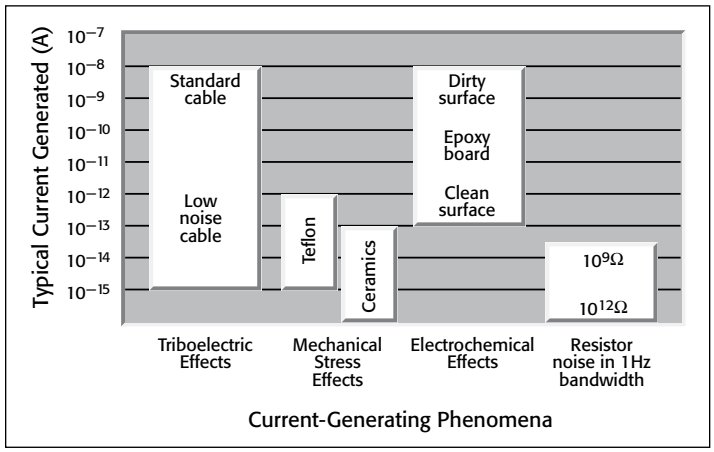


Figure 5. Typical Magnitudes of Generated Currents

Settling Time and Timing Menu Settings

The settling time of the measurement circuit is particularly important when making low current and high resistance measurements. The settling time is the time that a measurement takes to stabilize after the current or voltage is applied or changed. Factors affecting the settling time of the measurement circuit include the shunt capacitance (C_{SHUNT}) and the source resistance (R_S). The shunt capacitance is due to the connecting cables, test fixtures, switches, and probes. The higher the source resistance of the DUT, the longer the settling time. The shunt capacitance and source resistance are illustrated in the measurement circuit in ***Figure 6***.

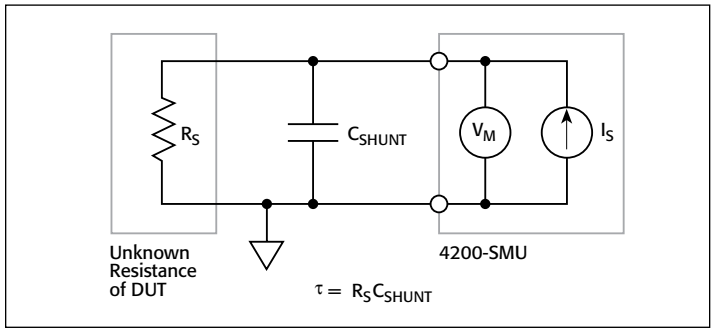


Figure 6. SMU Instrument Measurement Circuit Including C_{SHUNT} and R_S

The settling time is the result of the RC time constant, or τ, where:

$\tau = R_S C_{SHUNT}$

An example for determining the settling time can be calculated as follows, if C_{SHUNT} = 10pF and R_S = 1TΩ, then:

τ = 10pF × 1TΩ = 10 seconds

Therefore, a settling time of five τ, or 50 seconds, would be required for the reading to settle to within 1% of final value! ***Figure 7*** shows the exponential response of a step voltage into an RC circuit. After one time constant (τ = RC), the voltage rises to within 63% of final value.

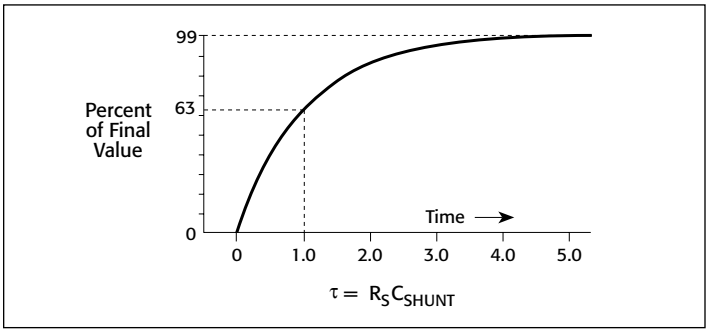


Figure 7. Exponential Response of Stepped Voltage Across RC Circuit

To make successful low current measurements, it's important to add sufficient time for each measurement, particularly when sweeping voltage. This settling time can be added in the Timing menu in the Sweep Delay field for the Sweeping Mode or the Interval time field for the Sampling Mode. To verify how much interval time to add, measure the settling time of the DUT by plotting the current vs. time to a stepped voltage. The stepped voltage should be the bias voltage that will be used in the actual measurement of the DUT. The ITMs in the *LowCurrent* project can be used to perform the settling time measurement. The #Samples in the Timing Menu will probably need to be increased to ensure settled readings will be displayed on the graph. When making low current measurements, use the Quiet Speed Mode or add extra filtering in the Timing Menu. Keep in mind that there is a noise/speed trade-off. With more filtering and delays, there will be less noise but a slower measurement speed.

Electrostatic Interference and Shielding

Electrostatic coupling or interference occurs when an electrically charged object approaches the circuit under test. At low impedance levels, the effects of the interference aren't noticeable because the charge dissipates rapidly. However, high resistance materials don't allow the charge to decay quickly, which may result in unstable, noisy measurements. Typically, electrostatic interference is an issue when making current measurements ≤1nA or resistance measurements ≥1GΩ.

To reduce the effects of the fields, the circuit being measured can be enclosed in an electrostatic shield. ***Figure 8*** illustrates the dramatic difference between an unshielded and a shielded measurement of a 100GΩ resistor. The unshielded measurements are much noisier than the shielded measurements.

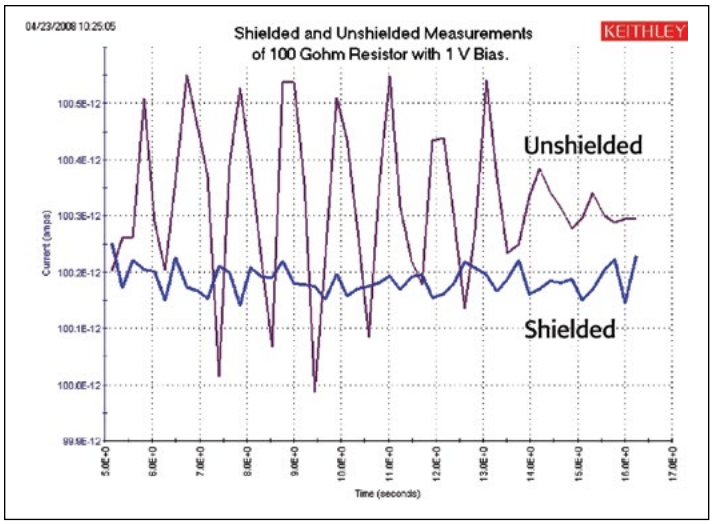


Figure 8. Shielded vs. Unshielded Measurements on a 100GΩ Resistor

The shield can be just a simple metal box or meshed screen that encloses the test circuit. Commercial probe stations often enclose the sensitive circuitry within an electrostatic shield. The shield is connected to the measurement circuit LO terminal, which is not necessarily earth ground. In the case of the Model 4200-SCS, the shield is connected to the Force LO terminal as shown in ***Figure 9***.

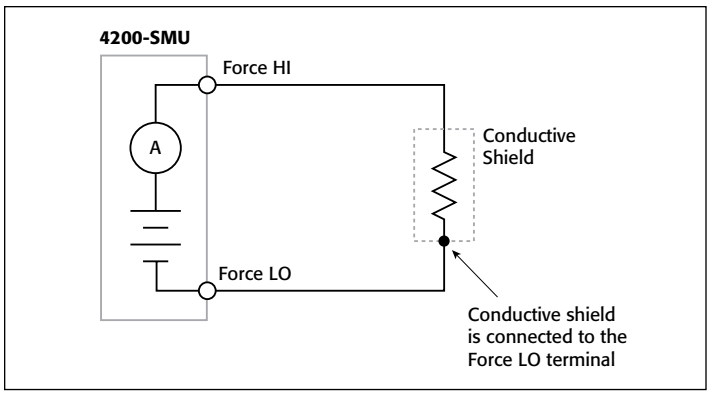


Figure 9. Shielding a High Impedance Device

To minimize error currents due to electrostatic coupling:

- Shield the DUT and connect the enclosure electrically to the test circuit common, the Force LO terminal of the 4200-SCS.
- Keep all charged objects (including people) and conductors away from sensitive areas of test circuit.
- Avoid movement and vibration near the test area.

Leakage Current and Guarding

Leakage current is an error current that flows (leaks) through insulation resistance when a voltage is applied. This error current becomes a problem when the impedance of the DUT is comparable to that of the insulators in the test circuit. To reduce leakage currents, use good quality insulators in the test circuit, reduce humidity in the test lab, and use guarding.

The guard is a conductor driven by a low impedance source whose output is at or near the same potential as the high impedance terminal. The guard terminal is used to guard test fixture and cable insulation resistance and capacitance. The guard is the inside shield of the triax connector/cable illustrated in ***Figure 10***.

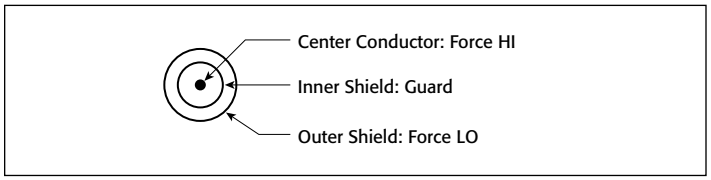


Figure 10. Conductors of 4200 Triax Connector/Cable

Guarding should not be confused with shielding. Shielding usually implies the use of a metallic enclosure to prevent electrostatic interference from affecting a high impedance circuit. Guarding implies the use of an added low impedance conductor, maintained at the same potential as the high impedance circuit, which will intercept any interfering voltage or current. A guard doesn't necessarily provide shielding. The following paragraphs outline two examples of guarding: 1) using guarding to reduce the leakage due to a test fixture and 2) using guarding to reduce leakage currents due to cabling.

Figure 11 shows how the guard can eliminate the leakage current that may flow through the stand-off insulators in a test fixture. In ***Figure 11a***, the leakage current (I_L) flows through the stand off insulators (R_L). This leakage current is added to the current from the DUT (I_{DUT}) and is measured by the SMU ammeter (I_M), adversely affecting the accuracy of the low current measurement.

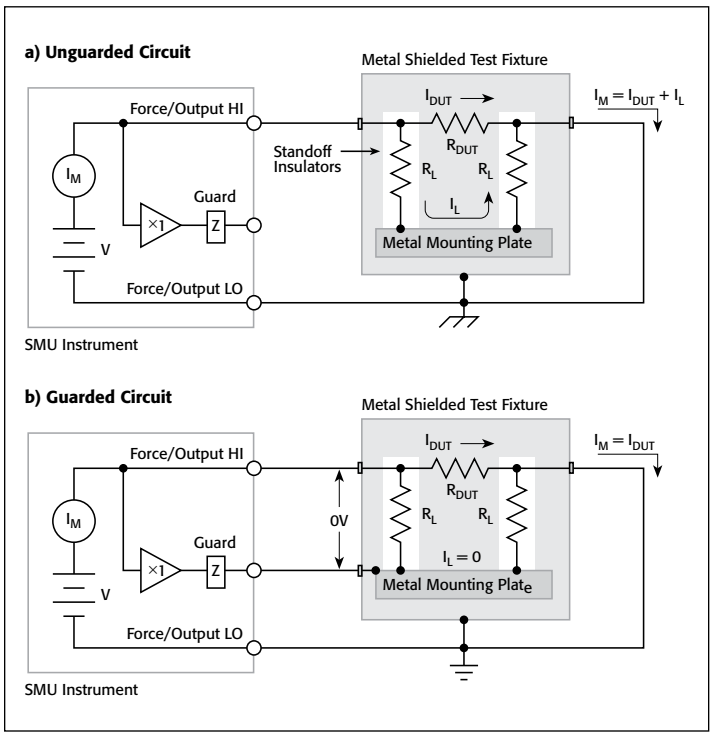


Figure 11. Using Guarding to Reduce Leakage in a Test Fixture

In ***Figure 11b***, the metal mounting plate is connected to the guard terminal of the SMU instrument. The voltages at the top and bottom of the stand off insulator are nearly at the same potential (0V drop), so no leakage current will flow through the standoffs to affect the measurement accuracy. For safety purposes, the metal shield must be connected to earth ground because the metal mounting plate will be at the guard potential.

Guarding can also be used to reduce leakage currents in cabling. ***Figure 12*** illustrates how a driven guard prevents the leakage resistance of a cable from degrading low current measurements. In the unguarded configuration, the leakage resistance of the coax cable is in parallel with the DUT (R_{DUT}), creating an unwanted leakage current (I_L). This leakage current will degrade very low current measurements.

In the guarded circuit, the inside shield of the triax cable is connected to the guard terminal of the SMU instrument. Now this shield is driven by a unity-gain, low impedance amplifier (guard). The difference in potential between the Force HI terminal and the Guard terminal is nearly 0V, so the leakage current (I_L) is eliminated.

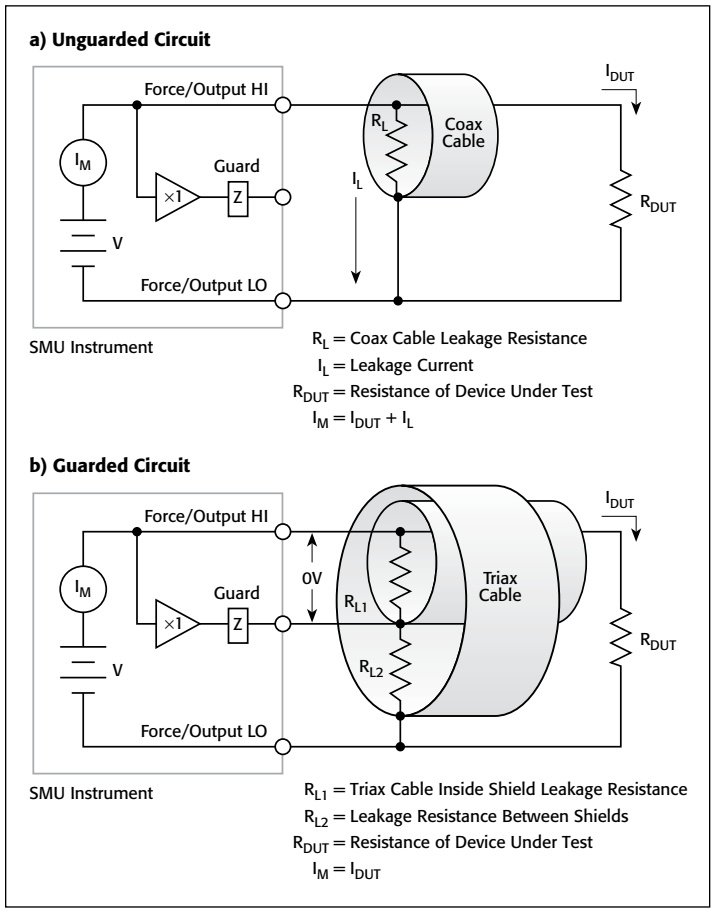


Figure 12. Using Guarding to Reduce Leakage Currents in Cabling

To see the results of using triax cable vs. coax cable when making a very high resistance measurement, ***Figure 13*** shows the results of measuring current vs. time of a 10V step function into a 100GΩ resistor. The triax cable enables guard, improving the measurement in two ways: 1) it reduces the effective cable capacitance and thus decreases the RC time constant or settling time of the measurement, and 2) it prevents the leakage resistance of the cable from degrading the measurement accuracy.

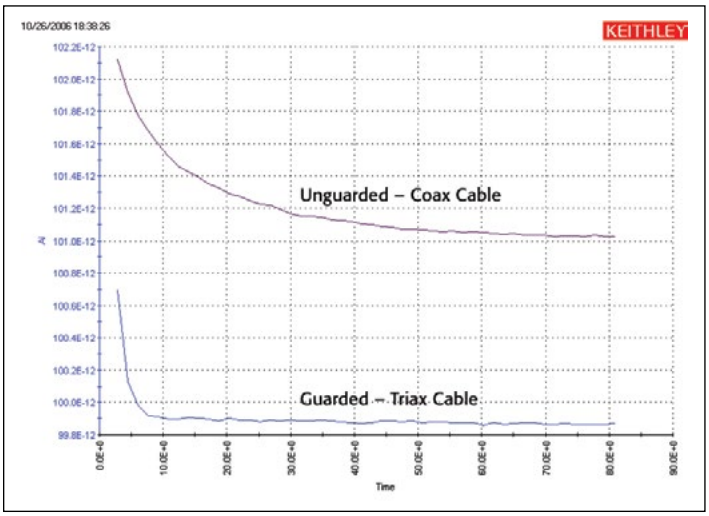


Figure 13. Results of Using a Coax Cable and a Triax Cable when Measuring a High Resistance

As you can see from the graph in ***Figure 13***, using triax cables with guarding resulted in measured currents that had lower leakage (a few picoamps lower) and had a faster settling time (about ten times faster).

If the SMU instruments must be connected to a test fixture with BNC connectors, use Keithley triax cables from the SMU instruments to the test fixture, and then BNC to triax adaptors (with guard removed) to attach the cables to the test fixture.

SMU Instrument Connections to DUT

In addition to using shielding and guarding when making connections to the DUT, it is very important to connect the appropriate terminal of the 4200-SCS to the appropriate terminal of the device. Improper connections of the SMU instrument Force HI and Force LO terminals can cause current offsets and unstable measurements. These errors are due to common mode current.

In general, always connect the high impedance terminal (Force HI) of the SMU instrument to the highest resistance point of the circuit under test. Likewise, always connect the low impedance terminal (Force LO) of the 4200-SCS to the lowest resistance point of the circuit under test. The lowest resistance point may be a common terminal or earth ground. If the Force HI terminal is connected to the lowest resistance point, common mode current can flow through the measurement circuit.

Figure 14 illustrates both a proper and an improper measurement connection. ***Figure 14a*** indicates a proper connection because the Force HI terminal of the 4200-SMU is connected to the gate of the device on a wafer, and the Force LO terminal is connected to the grounded chuck. The gate terminal on the wafer is the highest impedance point and the grounded

chuck is the low impedance point, so this circuit is a proper connection. Note that the common mode current flows from the Force LO terminal of the SMU instrument to the grounded chuck; however, the current does not flow through the ammeter, and therefore does not affect the measurement.

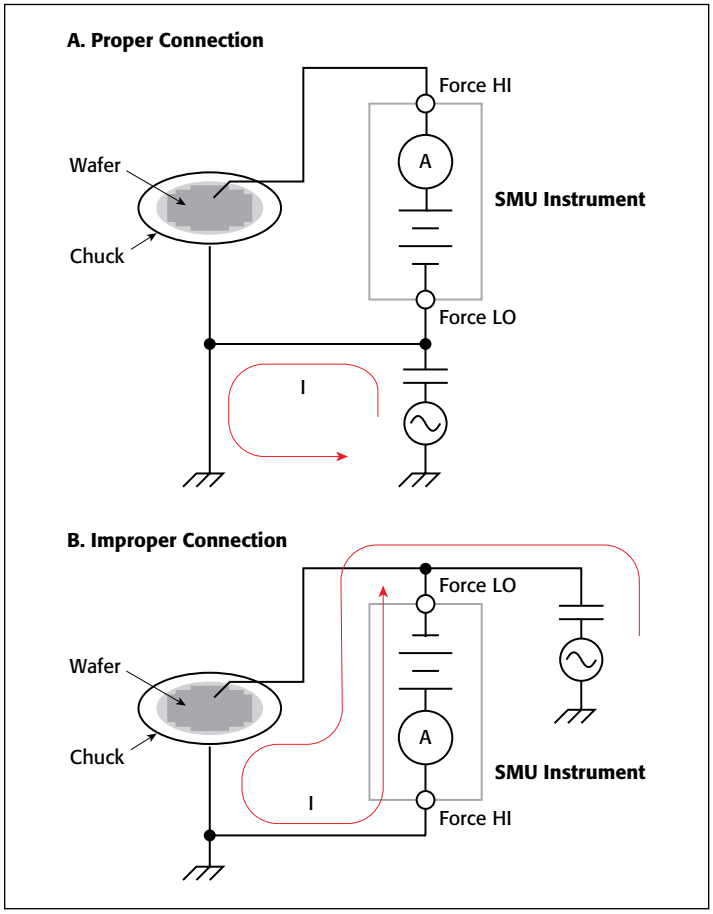


Figure 14. Making SMU Instrument Connections to a Device on a Grounded Chuck

Figure 14b illustrates an improper connection with the Force LO terminal of the SMU instrument connected to the high impedance gate terminal and the Force HI terminal of the SMU instrument connected to the grounded chuck. In this case, the common mode current will flow through the SMU instrument as well as the DUT. This will result in inaccurate, even unstable measurements.

Triboelectric Effects

Triboelectric currents are generated by charges created between a conductor and an insulator due to friction. Here, free electrons rub off the conductor and create a charge imbalance that causes the current flow. This noise current can be in the range of tens of nanoamps. ***Figure 15*** illustrates the flow of triboelectric current.

The triax cables supplied with the 4200-SCS greatly reduce this effect by using graphite-impregnated insulation beneath the outer shield. The graphite provides lubrication and a conducting cylinder to equalize charges and minimize charge generated by

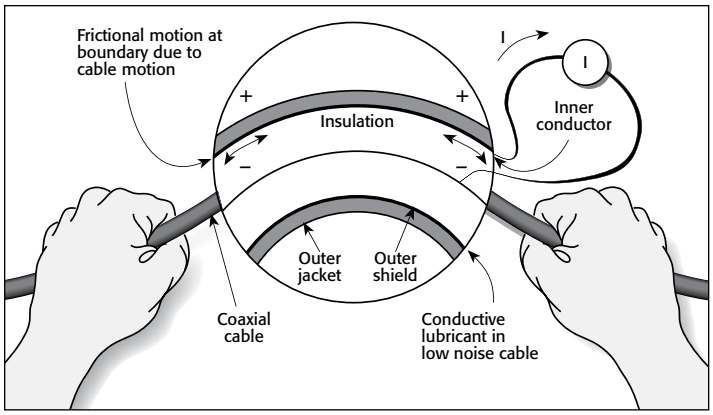


Figure 15. Offset Current Generated by the Triboelectric Effect

frictional effects of cable movement. However, even this type of triax cable creates some noise when subjected to vibration and expansion or contraction. Therefore, all connections should be kept short, away from temperature changes (which would create thermal expansion forces), and preferably supported by taping or wiring the cable to a non-vibrating surface such as a wall, bench, or rigid structure.

Other techniques should also be employed to minimize movement and vibration problems:

- Remove or mechanically decouple vibration sources such as motors, pumps, and other electromechanical devices.
- Securely mount or tie down electronic components, wires, and cables.
- Mount the preamps as close as possible to the DUT.

Piezoelectric and Stored Charge Effects

Piezoelectric currents are generated when mechanical stress is applied to certain crystalline materials when used for insulated terminals and interconnecting hardware. In some plastics, pockets of stored charge cause the material to behave in a manner similar to piezoelectric materials. An example of a terminal with a piezoelectric insulator is shown in ***Figure 16***.

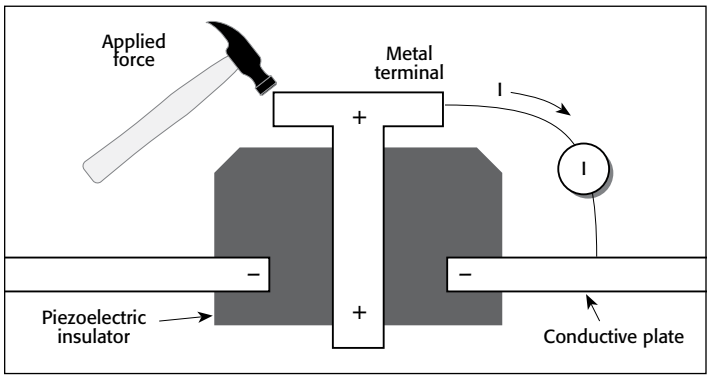


Figure 16. Current Generated by Piezoelectric Effects

To minimize these effects, remove mechanical stresses from the insulator and use insulating materials with minimal piezoelectric and stored charge.

Contamination and Humidity Effects

The insulation resistance of test fixtures can be dramatically reduced by high humidity or ionic contamination. High humidity conditions occur with condensation or water absorption, while ionic contamination may be the result of body oils, salts, or solder flux. A reduction in insulation resistance can have a serious effect on high impedance measurements. In addition, humidity or moisture can combine with any contaminants present to create electrochemical effects that can produce offset currents. For example, commonly used epoxy printed circuit boards, when not thoroughly cleaned of etching solution, flux, or other contamination, can generate currents of a few nanoamps between conductors (see ***Figure 17***).

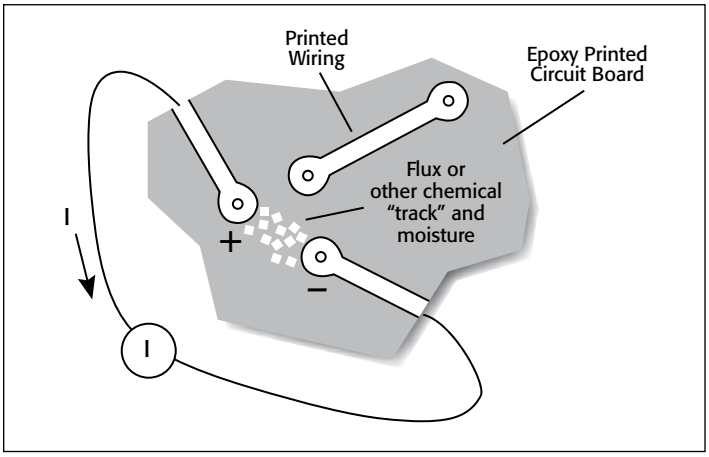


Figure 17. Current Generated from Contamination and Humidity

To avoid the effects of contamination and humidity, select insulators that resist water absorption, and keep humidity to moderate levels (ideally <50%). Also, be sure all components and test fixturing in the test system are kept clean and free of contamination.

Ground Loops

Ground loops can generate spurious signals that may be a DC offset or an AC signal (usually line frequency or multiples of line frequency). Ground loops are caused by multiple grounds in the test circuit. A typical example of a ground loop can be seen when a number of instruments are plugged into power strips on different instrument racks. Frequently, there is a small difference in potential between the ground points, which can cause large currents to circulate and create unexpected voltage drops.

The configuration shown in ***Figure 18*** shows a ground loop that is created by connecting both the 4200 signal common (Force LO) and DUT LO to earth ground. A large ground current flowing in the loop will encounter small resistances, either in the conductors or at the connecting points. This small resistance results in voltage drops that can affect performance.

To prevent ground loops, the test system should be connected to ground at only a single point. If it is not possible to remove the DUT ground, the ground link between the

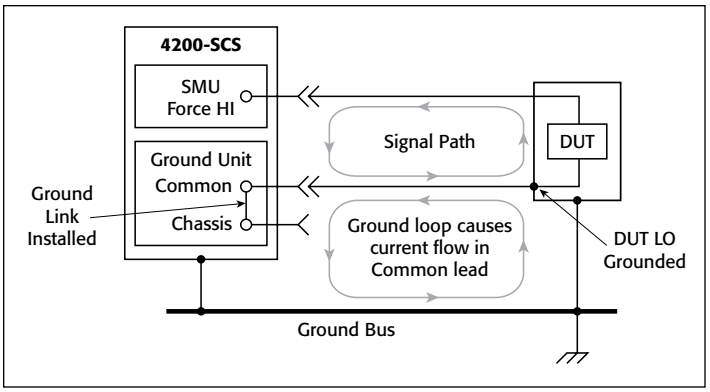


Figure 18. Ground Loops

4200 GNDU COMMON terminal and chassis ground should be removed, as shown in ***Figure 19***.

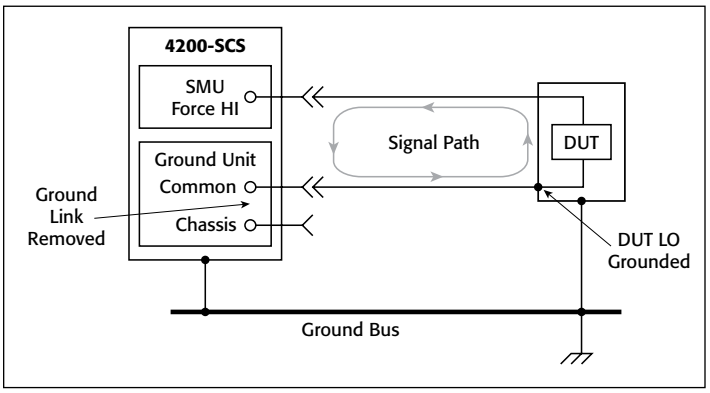


Figure 19. Eliminating Ground Loops

If a ground loop is suspected, unplug the suspect instrument from the AC power and try making a sensitive current measurement to verify the problem is gone. To eliminate ground loops, make as few grounds as possible, preferably, no more than one.

Light

Some components such as diodes and transistors are excellent light detectors. Consequently, these components must be tested in a light-free environment. To ensure measurement accuracy, check the test fixture for light leaks at door hinges, tubing entry points, and connectors or connector panels.

Noise and Source Impedance

Noise can seriously affect sensitive current measurements. Both the source resistance and the source capacitance of the DUT can affect the noise performance of the SMU instrument.

The source resistance of the DUT will affect the noise performance of the SMU instrument's feedback ammeter. As the source resistance is reduced, the noise gain of the ammeter will increase. ***Figure 20*** shows a simplified model of a feedback ammeter.

In this circuit:

R_S = source resistance

C_S = source capacitance

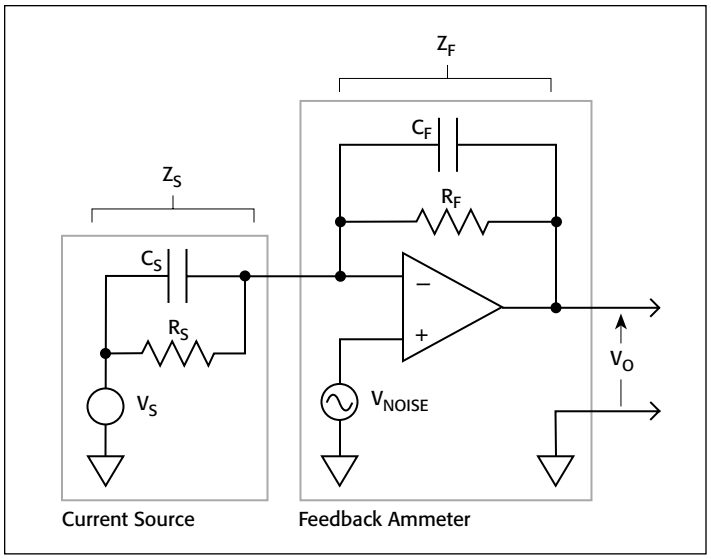


Figure 20. Simplified Model of a Feedback Ammeter

V_S = source voltage

V_{NOISE} = noise voltage of the ammeter

R_F = feedback resistor

C_F = feedback capacitance

The noise gain of the circuit can be given by this equation:

$$\text{Output } V_{NOISE} = \text{Input } V_{NOISE} \left(1 + \frac{R_F}{R_S}\right)$$

Note that as the source resistance (R_S) decreases, the output noise increases. Because decreasing the source resistance can have a detrimental effect on noise performance, there are minimum recommended source resistance values based on the current measurement range, which are summarized in ***Table 1***.

Table 1. Minimum Recommended Source Resistance Values

Range	Minimum Recommended Source Resistance
1pA to 100pA	1GΩ to 100GΩ
1nA to 100nA	1MΩ to 100MΩ
1μA to 100μA	1kΩ to 100kΩ
1mA to 100mA	1Ω to 100Ω

The source capacitance of the DUT will also affect the noise performance of the SMU instrument. In general, as source capacitance increases, so does the noise gain. Although there is a limit as to the maximum source capacitance value, it's usually possible to measure at higher source capacitance values by connecting a resistor or a forward-biased diode in series with the DUT. The diode acts like a variable resistance, low when the charging current to the source capacitance is high, then increasing in value as the current decreases with time.

Compensating for Offsets

After external errors have been determined and reduced, if possible, the internal and external offsets of the test system can be subtracted from future measurements. First, perform the SMU auto calibration with the capped input as described. Then, determine the offsets for each SMU instrument to the probe tip. This average offset current can be subtracted from subsequent current measurements in other projects using the Formulator tool in the software. For making very low current measurements, the average offset current should be remeasured periodically (at least monthly).

Conclusion

When configured with the optional Model 4200-PA Remote PreAmps, the Model 4200-SCS Parameter Analyzer can measure accurately currents of picoamps or less. The offset current of the entire measurement system should be measured to determine the system's limitations, so it can be adjusted if necessary. Sources of measurement errors can be reduced by using techniques such as shielding, guarding, and proper grounding of instruments, and by choosing appropriate settings in the KITE software, including allowing sufficient settling time. Keithley's *Low Level Measurements Handbook* provides further information on optimal low current measurement techniques.

For Further Reading

Keithley Instruments, *Model 4200-SCS Reference Manual*, Section 5 (Included as part of the system software)

Keithley Instruments, *Low Level Measurements Handbook*, 6th edition, 2004.

Performing Charge Pumping Measurements with the Model 4200-SCS Parameter Analyzer

Introduction

Charge pumping (CP) is a well-known measurement technique for analyzing the semiconductor–dielectric interface of MOS structures. Important information about the quality and degradation of a device can be extracted from charge pumping current (I_{CP}) measurement results, including the interface trap density and the mean capture cross section. Pulsing a gate voltage and measuring a DC substrate current simultaneously is the basis for the various charge pumping methods, so a pulse generator and sensitive DC ammeter are required to make these measurements.

The Model 4200-SCS Parameter Analyzer offers a complete solution for charge pumping measurements because it contains the necessary hardware to make the sensitive measurements, as well as software to automate the measurements and analyze the results. This system is provided with predefined tests for making most of the common charge pumping tests, such as a pulsed base voltage sweep or a pulsed voltage amplitude sweep. This application note explains how to make charge pumping measurements using the Model 4200-SCS with the optional Model 4225-PMU Ultra Fast I-V Module (PMU) or Model 4220-PGU Pulse Generator Unit (PGU).

Charge Pumping Overview

Figure 1 is a charge pumping measurement circuit diagram. Basically, the gate of the MOSFET is connected to a pulse generator, which repeatedly switches the transistor from accumulation to inversion. While the gate is pulsed, a recombination process of majority/minority carriers occurs on the rising and falling edges of the pulses. This causes a current to flow in the opposite direction of the normal drain-to-source current. This induced current is known as the charge pumping current (I_{CP}) and can be measured by connecting a sensitive ammeter to the substrate, or bulk terminal, of the MOSFET.

Although several charge pumping methods have been developed, the basic charge pumping technique involves measuring the substrate current while applying voltage pulses of fixed amplitude, rise time, and frequency to the gate of the transistor. The source and drain are either tied to ground or slightly reverse-biased. The voltage pulse can be applied with a fixed amplitude while sweeping the base voltage or with a fixed base voltage while sweeping the amplitude of the pulse.

In the fixed-amplitude/voltage-base sweep, the amplitude and period (width) of the pulse are kept constant while the base voltage is swept from inversion to accumulation. This waveform

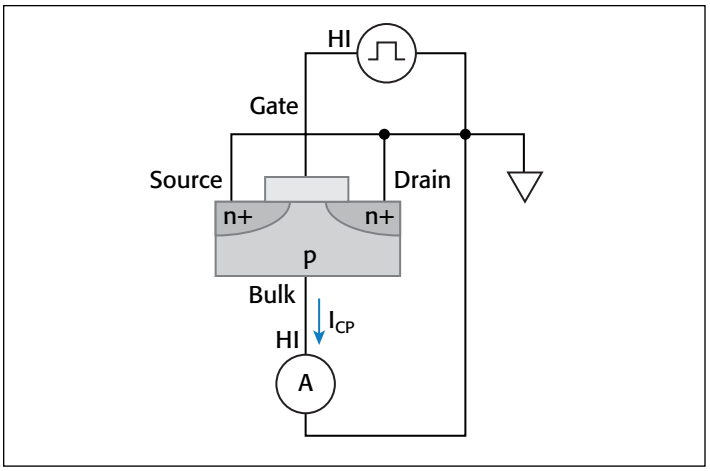


Figure 1. Basic charge pumping measurement circuit

and the corresponding curve of the charge pumping current shown as a function of the base voltage are both illustrated in ***Figure 2***. From the data, it's possible to extract the interface trap density (N_{it}) using this equation:

$$N_{it} = \frac{I_{CP}}{qfA}$$

where:

N_{it} = interface trap charge density (cm^{-2})

I_{CP} = charge pumping current (A)

f = test frequency (Hz)

q = electron charge, 1.6022×10^{-19} C

A = channel area (cm^2)

The interface trap density as a function of band bending can also be extracted from the following equation:

$$D_{it} = \frac{I_{CP}}{qfA\Delta E}$$

where:

D_{it} = interface trap charge density ($cm^{-2}eV^{-1}$)

I_{CP} = charge pumping current (A)

f = test frequency (Hz)

q = electron charge, 1.6022×10^{-19} C

A = channel area (cm^2)

ΔE = the difference between the inversion Fermi level and the accumulation Fermi level [1]

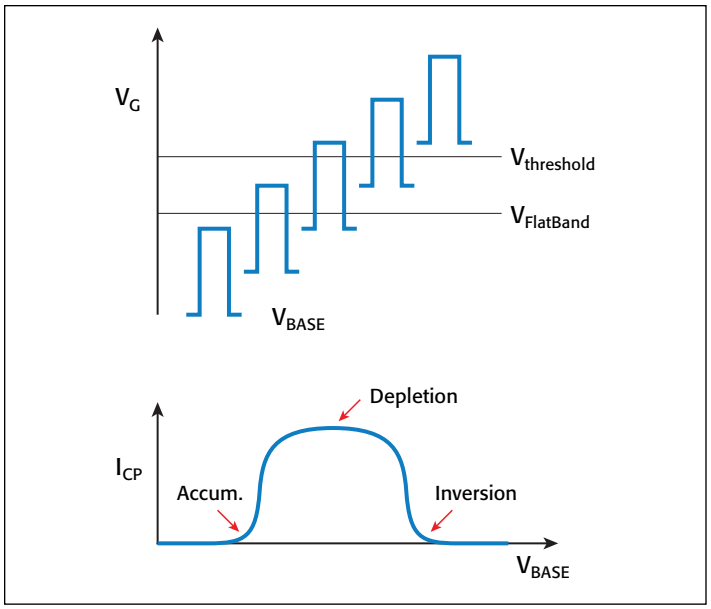


Figure 2. Pulse waveform for fixed-amplitude/voltage-base sweep and corresponding charge pumping current curve

The fixed-base/variable-amplitude sweep method is another common technique for determining the charge pumping current. With this method, the base voltage is kept constant in accumulation and the variable voltage amplitude is pulsed into inversion. As shown in ***Figure 3***, as the voltage amplitude (V_{AMP}) of the pulses increases, the charge pumping current saturates and stays saturated.

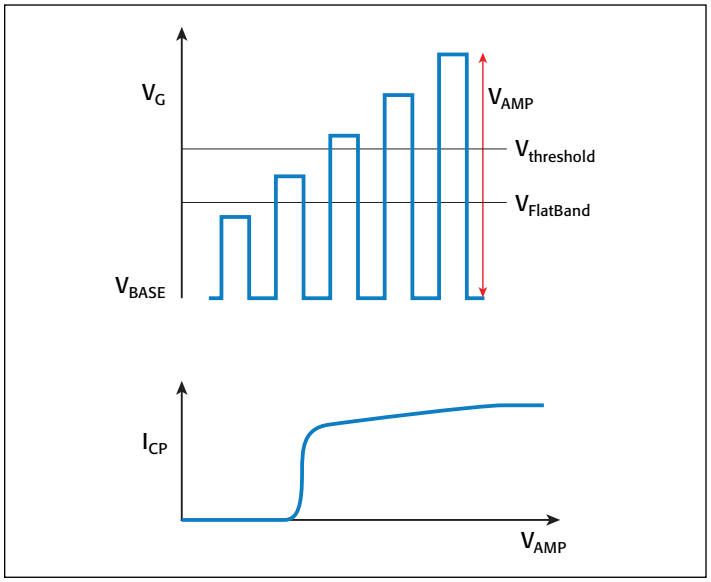


Figure 3. Pulse waveform for fixed-base/variable-amplitude sweep with corresponding charge pumping current curve

Other charge pumping techniques are used in addition to the fixed-amplitude/variable-base sweep and the fixed-base/variable-amplitude sweep. In some cases, the voltage waveform can have various shapes, the rise and fall times can be varied, or the charge pumping current can be measured as a function of frequency.

Hardware Configuration

Figure 4 is the basic circuit diagram for making charge pumping measurements using the Model 4200-SCS. For this application, the Model 4200-SCS is configured with either a Model 4220-PGU Pulse Generator Unit (PGU) or a Model 4225-PMU Ultra Fast I-V Module (PMU), one or two Model 4200-SMU Source Measure Unit (SMU) Instruments, and one Model 4200-PA Preamp.

The pulser (4225-PMU or 4220-PGU) is connected to the gate of the MOSFET in order to apply pulses of sufficient amplitude to drive the device between inversion and accumulation. Depending on the charge pumping method, the PGU or PMU can sweep the pulse amplitude, sweep the base voltage, vary the rise/fall time, and vary the test frequency. The test frequency is usually in the kilohertz to megahertz range.

SMU1 is connected to the Bulk terminal and measures the resulting substrate current. This charge pumping current (I_{CP}) is often in the nanoamp or picoamp range. For measuring currents of less than one nanoamp, the optional Model 4200-PA should be used.

The source and drain terminals of the MOSFET are tied together and connected to SMU2, which applies a slight reverse-bias (V_r). If $V_r = 0$, then the source/drain terminals can be connected to the ground unit (GNDU) instead of to SMU2. To prevent oscillations and minimize noise, it is very important to connect the LO (common) terminals of all the SMU instruments and the pulser (4225-PMU or 4220-PGU) as close as possible to the device. The LO terminal of the SMU instrument is the outside shell of the triax connector. The LO terminal of the PMU and PGU is the outside shield of the SMA cable.

To minimize noise in low current measurements due to electrostatic interference, make sure the device is shielded by placing it in a metal enclosure with the shield connected to the LO terminal of the SMU instrument. Further information on making low current measurements with the Model 4200-SCS is

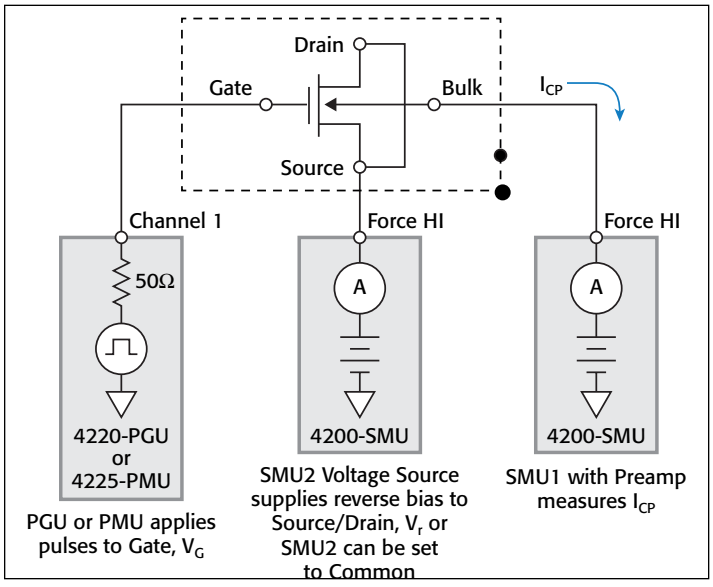


Figure 4. Model 4200-SCS configuration for charge pumping measurements

available in Keithley Application Note Number 2959, "Optimizing Low Current Measurements with the Model 4200-SCS Semiconductor Characterization System."

Using the KITE Software to Automate the Charge Pumping Measurements

The Model 4200-SCS comes with a project that contains a library of tests used in many of the common charge pumping measurement techniques. This *chargepumping* project is located in the projects folder: *C:\S4200\kiuser\Projects_Pulse*. When this project is opened, a list of the tests is displayed in the Project Navigator (***Figure 5***). ***Table 1*** lists the user test modules (UTMs) included in the project and a brief description of each test.

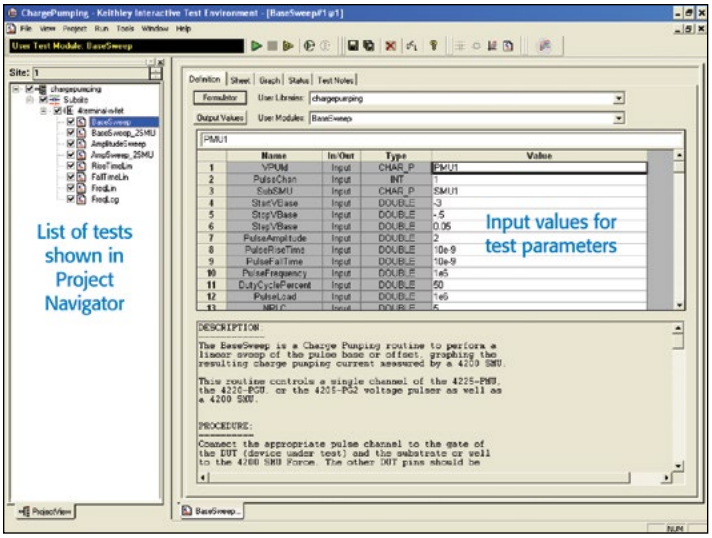


Figure 5. The *chargepumping* project

Table 1. Charge pumping user test modules

User Test Modules	Description
BaseSweep	The base voltage of the waveform is swept while the amplitude of the pulse is kept constant. The resulting charge pumping current is measured and graphed as a function of the base voltage. The source/drain terminals are tied to ground.
BaseSweep_2SMU	Same as *BaseSweep* test, except it adds a second SMU instrument to apply a DC voltage bias to the source/drain terminals.
AmplitudeSweep	The amplitude of the pulse is swept while the base voltage is kept constant. The charge pumping current is measured and graphed as a function of the pulse amplitude voltage. The source/drain terminals are tied to ground.
AmplitudeSweep_2SMU	Same as *AmplitudeSweep* test, except it adds a second SMU instrument to apply a DC voltage bias to the source/drain terminals.
RiseTimeLin	Performs a linear sweep of the rising transition time of the pulse. I_{CP} is measured and graphed as a function of the rise time. The source/drain terminals are tied to ground.
FallTimeLin	Performs a linear sweep of the falling transition time of the pulse. I_{CP} is measured and graphed as a function of the fall time. The source/drain terminals are tied to ground.
FreqLin	With the amplitude, offset voltage, rise/fall times constant, the I_{CP} is measured as a function of a linear sweep of the test frequency. The source/drain terminals are tied to ground.
FreqLog	With the amplitude, offset voltage, and rise/fall times constant, the I_{CP} is measured and graphed as a function of a log sweep of the test frequency. The source/drain terminals are tied to ground.

The user selects the desired test and then inputs the appropriate values for the test parameters on the Definition Tab. The parameters vary depending on the particular test, but they usually include the magnitude of the pulse, sweep values, rise/fall time, test frequency, duty cycle, etc. Specific information on these tests, including the test parameters, is available in Section 16 of the Model 4200-SCS Complete Reference Manual.

After the hardware and the software have been configured, the measurement can be executed in the project by clicking the on-screen Run button. The measurements are displayed in the Graph tab and listed in the Sheet tab. The Sheet tab is used to record and manipulate the data. The measurements (I_{CP}, Q_{CP}, pulsed voltage, etc.) can be saved in a worksheet as an .xls, .txt, or .csv file.

The graph from executing the *BaseSweep* user test module is shown in ***Figure 6***. This user test module measures the charge pumping current as a function of the base voltage.

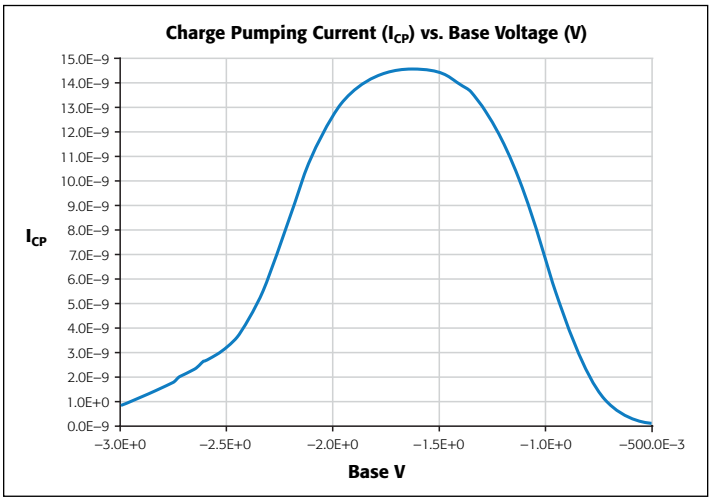


Figure 6. Graphical results of *BaseSweep* user test module

The input parameter values of a user test module can be updated and the measurements can be repeated. One way to do this is by using the on-screen Append Run button, which can be used to show multiple test results on one graph. ***Figure 7*** shows the test results of increasing the test frequency from 1MHz to 6MHz. The data is appended to the graph and a new worksheet is added in the Sheet tab for each appended test run.

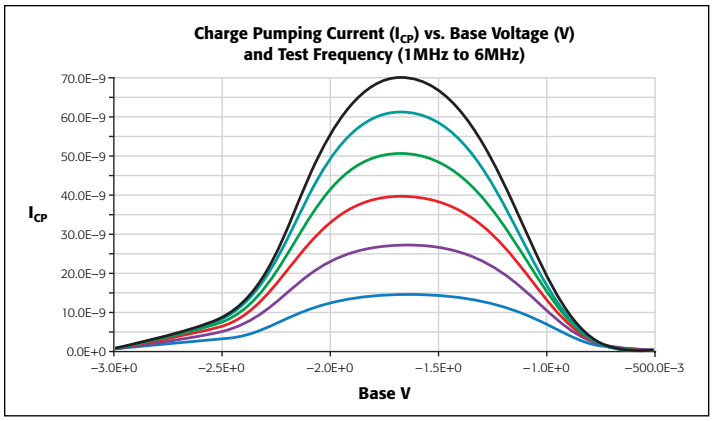


Figure 7. Charge pumping current measurement results at multiple test frequencies

The *AmplitudeSweep* is another common charge pumping test. It measures the charge pumping current as the amplitude of the pulse is swept. The base voltage is kept constant. The resulting charge pumping measurements are shown in ***Figure 8***.

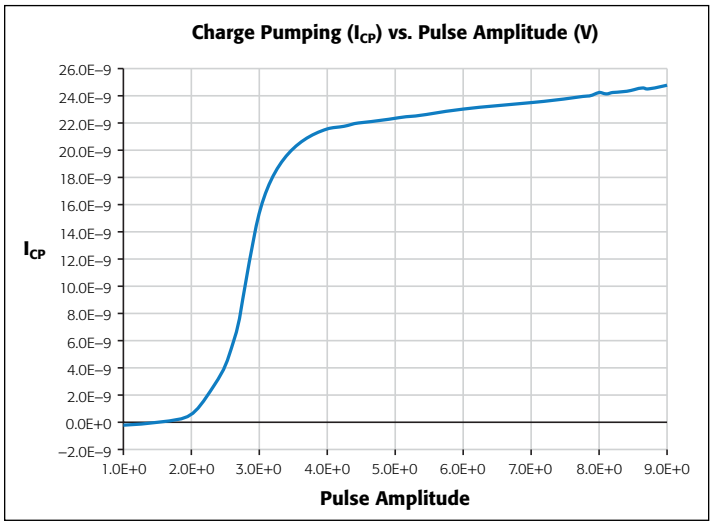


Figure 8. Charge pumping current as a function of pulse amplitude

Simple analyses, such as extracting the interface trap density, can be performed on the data using the built-in Formulator function. To activate this function, click the Formulator button on the Definition tab of the test setup window. Enter the formula for D_{it} as shown in ***Figure 9***. The resulting D_{it} value can also be plotted in the graph.

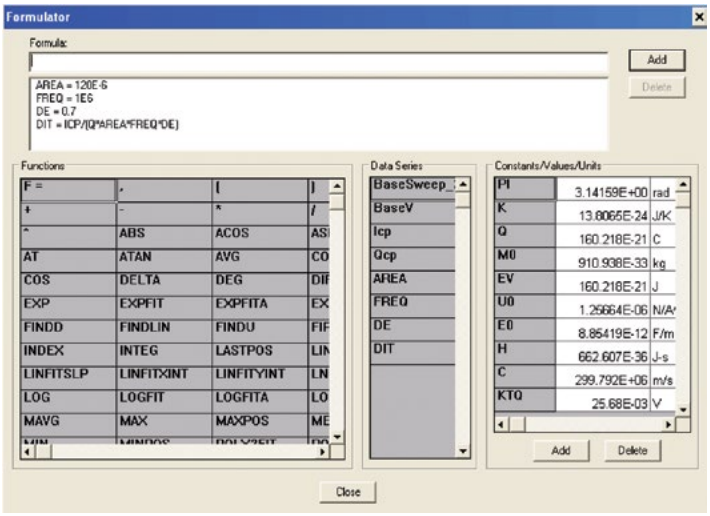


Figure 9. Entering formulas in the Formulator function

Conclusion

The Model 4200-SCS is the ideal tool for characterizing interface properties of gate dielectrics. With the built-in pulse generator, Model 4225-PMU or Model 4220-PGU, and the KTE Interface software, the user need not do any programming, which simplifies measurement and analysis. When equipped with the Model 4225-PMU, the Model 4200-SCS is a powerful tool for performing many tests commonly required in DC and ultra-fast I-V electrical characterization of devices, including the charge pumping application detailed here. The 4225-PMU is not simply a pulse generator; it can also measure current and voltage and be used for transient I-V (waveform capture) applications.

References

1. G. Groeseneken, H.E. Maes, N. Beltran, and R.T. De Keersmaecker, "A Reliable Approach to Charge-Pumping Measurements in MOS Transistors," *IEEE Trans. Electron. Dev.*, Vol. ED-31, pp. 42-53, 1984.

Monitoring Channel Hot Carrier (CHC) Degradation of MOSFET Devices using Keithley's Model 4200-SCS

Introduction

Channel Hot Carrier (CHC) induced degradation is an important reliability concern in modern ULSI circuits. Charge carriers gain kinetic energy as they are accelerated by the large electric field across the channel of a MOSFET. While most carriers reach the drain, hot carriers (those with very high kinetic energy) can generate electron-hole pairs near the drain due to impact ionization from atomic-level collisions. Others can be injected into the gate channel interface, breaking Si-H bonds and increasing interface trap density. The effect of CHC is time dependant degradation of device parameters, such as V_T, I_{DLIN}, and I_{DSAT}.

This channel hot carrier induced degradation (often called HCI or hot carrier injection) can be seen on both NMOS and PMOS devices and will affect device parameters in all regions, such as V_T, sub-threshold slope, Id-on, Id-off, Ig, etc. The rate of degradation of each parameter over stress time depends on the device layout and process used.

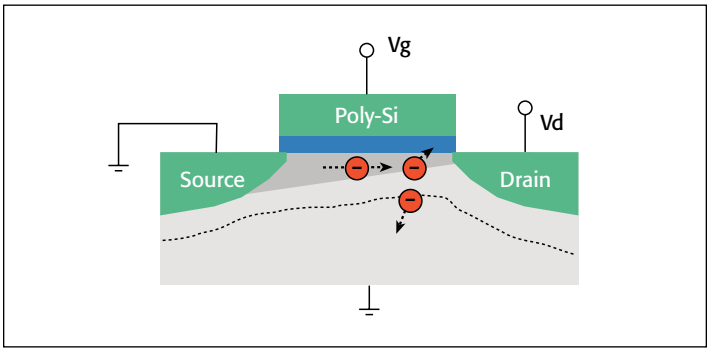


Figure 1. Channel Hot Carrier degradation

Procedures for CHC Degradation Test

A typical Channel Hot Carrier test procedure consists of a pre-stress characterization of the device under test (DUT), followed by a stress and measurement loop [1] (***Figure 2***). In this loop, devices are stressed at voltages higher than normal operating voltages. Device parameters, including I_{DLIN}, I_{DSAT}, V_T, Gm, etc, are monitored between stresses and the degradation of those parameters is plotted as a function of accumulated stress time. Prior to conducting this stress and measurement loop, the same set of device parameters is measured to serve as baseline values.

Stress bias conditions are based on worst-case degradation bias conditions, which are different for NMOS and PMOS FETs. Typically, for drain voltage stress, it should be less than 90% of the source drain breakdown voltage. Then, at the drain stress voltage, the gate stress voltage is different depending on the type

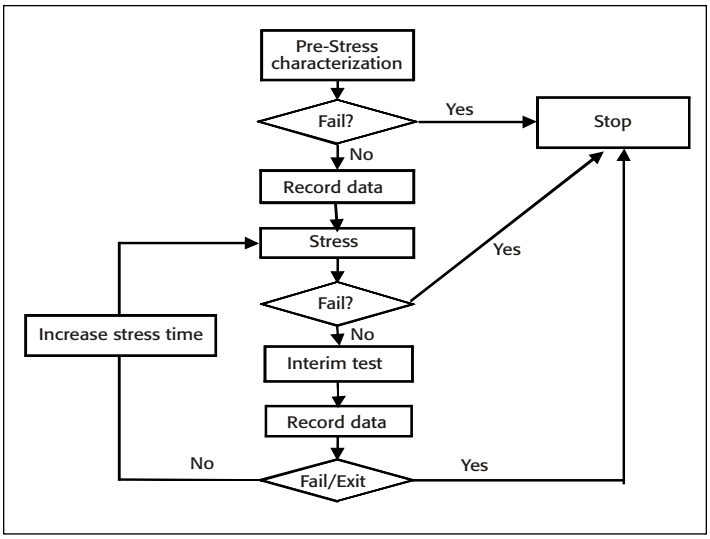


Figure 2. Typical CHC test procedure

of transistor and gate length. ***Table 1*** shows worst-case degradation bias conditions for NMOS and PMOS FETs created using different technologies [2].

Technology	L >= 0.35um	L < 0.25um
N-MOSFET	Vg (max Isub)	Vg (max Isub) or Vg = Vd
P-MOSFET	Vg (max Ig)	Vg = Vd

Table 1. Worst-case stress bias conditions for NMOS and PMOS FETs

The worst-case stress bias conditions can be easily determined using interactive test modules (ITMs) on the Model 4200-SCS Parameter Analyzer.

Device connections

It's easy to perform a CHC test on a single transistor. However, each CHC test typically takes a long time to complete, so it's desirable to have many DUTs stressed in parallel, then characterized sequentially between stresses to save time. To accomplish this, a switch matrix is needed to handle the parallel stresses and sequential measurements between stresses. ***Figure 3*** shows an example of a hardware configuration for a typical CHC test for multiple DUTs. The Model 4200-SCS provides the stress voltages and measurement capability, while the switch matrix enables parallel stress and sequential measurements of multiple devices. Depending on the number of devices under test, it's possible to use either the Model 708B mainframe, which accommodates one switch matrix card (12 device pins), or a Model 707B mainframe, with up to six matrix cards (72 pins maximum). The total number of different gate and drain stress biases is limited by the

number of source measure unit (SMU) instruments in the system. ***Figure 4*** illustrates a connection diagram using eight SMU instruments (for total of eight different drain and gate stress biases) plus a ground unit (for ground terminal) to stress 20 transistors in parallel.

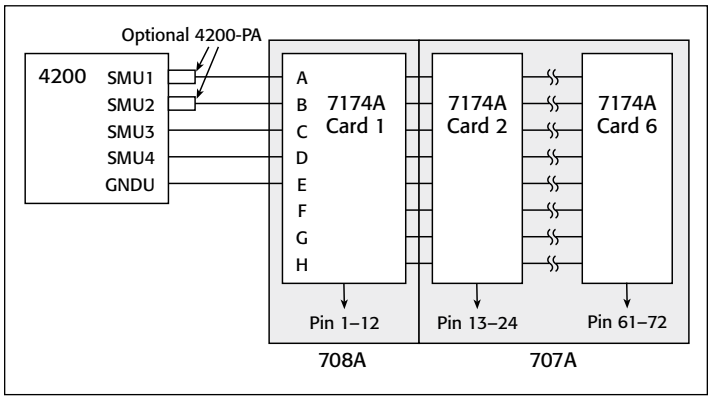


Figure 3. Hardware configuration example

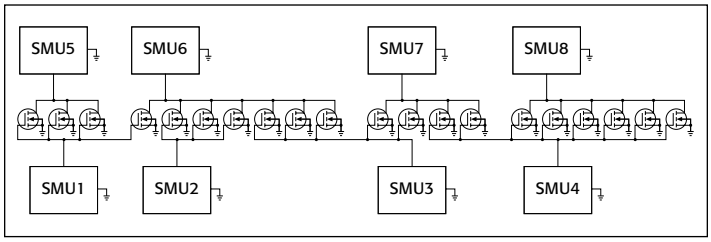


Figure 4. Example of using eight SMU instruments to stress 20 devices in parallel. A separate ground unit (GNDU) is used for common terminals.

Determining device parameters

Hot carrier parameters monitored include V_{TH}, GM, I_{DLIN} and I_{DSAT}. These parameters are initially measured before stress and re-measured at each cumulative stress time. The I_{DLIN} is the measured drain current with the device biased in the linear region, while I_{DSAT} is the measured drain current with the device biased in the saturation region. V_{TH} and GM can be determined using either constant current or extrapolation methods. In the extrapolation method, the V_{TH} is determined from the maximum slope of the I_{DS} vs. V_{GS} curve.

The Model 4200-SCS's Formulator Tool greatly simplifies extracting these parameters. Built-in functions include *Differentiate* to obtain GM, a *MAX* function to obtain the maximum GM (Gmext), and a least squares line-fit function to extract V_{TH} (Vtext). The formulas to calculate these parameters can be found in the HCI projects supplied with the Model 4200-SCS, and corresponding tests in test libraries. Some examples of these formulas include:

GM = DIFF(DRAINI,GATEV)

GMEXT = MAX(GM)

VTEXT = TANFITXINT(GATEV, DRAINI, MAXPOS(GM))

The last equation (VTEXT) is the x intercept of tangent fit of the I_D-V_G curve at the maximum GM point. ***Figure 5*** illustrates the Formulator Tool interface.

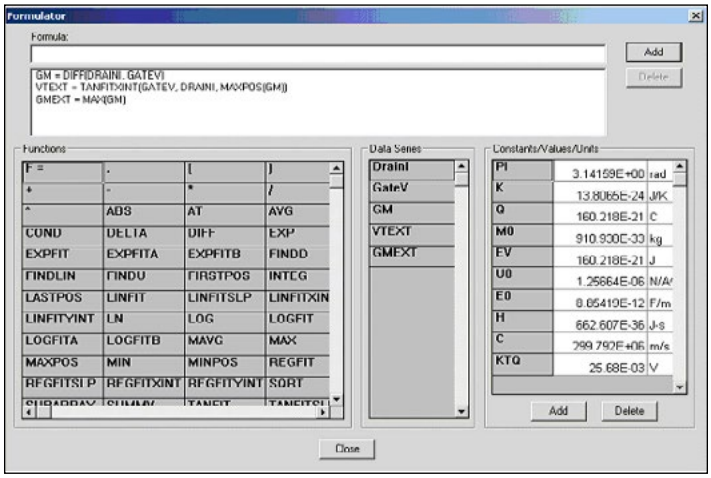


Figure 5. Model 4200-SCS's Formulator Tool interface

Once those parameters are calculated from individual tests, they can be exported by checking the check box in "Output Value" option for monitoring the degradation over stress time. For each test, an exit on compliance option can be selected, allowing the system either to skip the device or stop the overall CHC test in case of a device failure. For more details on these options, refer to the complete 4200-SCS Reference Manual.

Setting up stress conditions

One of the operating features of the Keithley Test Environment Interactive (KTEI) software for the Model 4200-SCS software is a stress cycle within the project tree structure with both voltage and current stress capabilities. Users can take advantage of the stress cycle to set up DC stresses on DUTs for preset durations. The duration of the stress for each cycle can be set up in either a linear or a logarithmic way (see ***Figure 6***). This feature is used in CHC/HCI, NBTI, EM (electromigration) and charge trapping applications to provide a constant DC stress (voltage or current). In stress/measure mode, the user can set up stress conditions for each terminal of the devices under test (***Figure 7***). After each stress cycle, the Model 4200-SCS goes through a measurement sequence, which can include any number and type of user-defined tests and parameter extractions. The degradation of those parameters over time is plotted in the stress graph. The Model 4200-SCS's "toolkit" architecture offers users tremendous flexibility in creating test sequences and stress-measure projects.

For critical parameters, a target degradation value can be set (see ***Figure 7***). Once the degradation of that parameter exceeds the target, that specific test will stop. This saves significant time by eliminating unnecessary stress and measure cycles on failed devices.

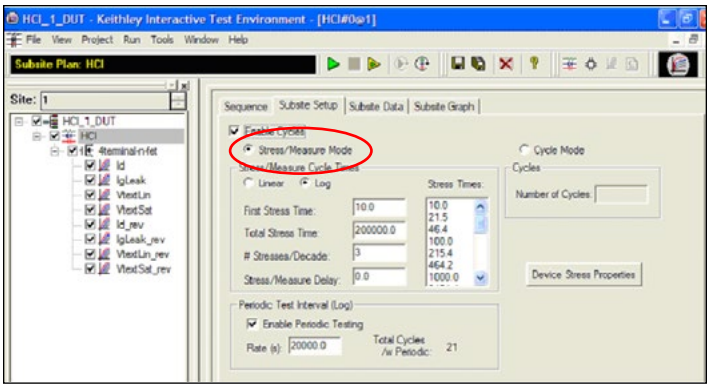


Figure 6. Stress cycle set-up page.

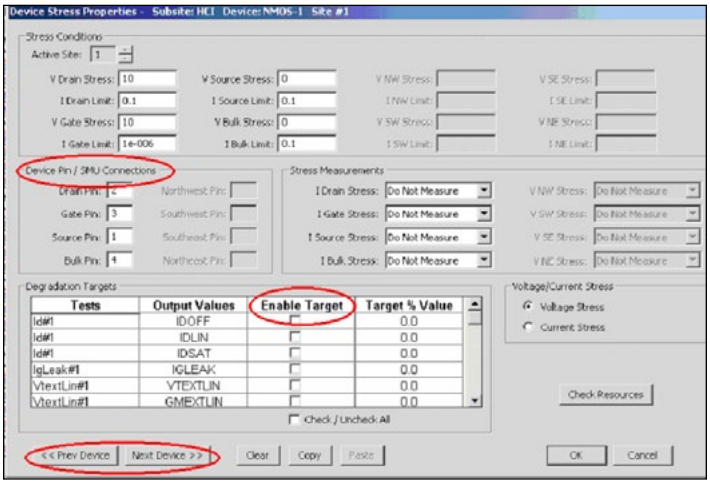
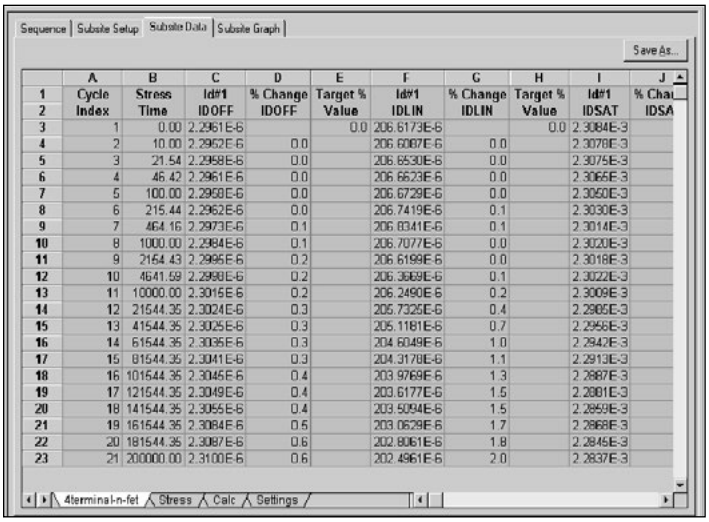


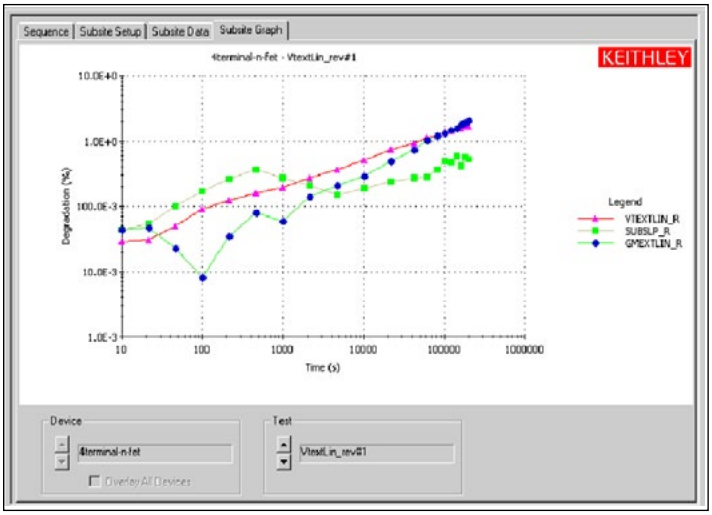
Figure 7. Device stress/pin connection/degradation target value set-up window.

If multiple DUTs are defined in the project, it's possible to toggle between devices using the "previous device" and "next device" buttons in the device stress set-up window (***Figure 7***). The "copy" and "paste" buttons can be used to copy stress settings from one device to the other without the need to re-enter all the information in all the input fields. With multiple devices stressed in parallel in different stress configurations, it can be difficult to correlate the number of different stress biases required and the number of SMU instruments available to apply them. Pressing the "check resource" button makes it easy to determine if there are enough SMU instruments for all the stress biases involved, and see how the SMU instruments are assigned to each of the different stress biases. A ground unit is used by default if the switch matrix is attached to the system and if the stress bias on the terminal is 0V.

A separate data sheet (***Figure 8a***) is incorporated within the stress set-up window to save information about cycle index, stress time, and monitored parameters extracted from the measurement between stresses, such as I_D and V_T. The data is saved automatically in Excel file format (.xls) in the project directory. It's possible to export the data to other locations as text or Excel files. If the system is in stress/measure mode, the degradation of the monitored parameters relative to pre-stress measurements is calculated automatically and can be plotted on the graph page (***Figure 8b***). For more information on the stress-measure capabilities provided in KTEI Software, consult the complete 4200-SCS Reference Manual.



a)



b)

Figure 8. a) Stress data sheet stores all stress information, including measurement results during stresses, and selected parameters measured between stresses. b) Plot of percentage degradation data as a function of stress time

Building a CHC project

The following steps outline a typical process for building a CHC project. For details on each step, consult the complete 4200-SCS Reference Manual.

1. Create the project structure
   a. Determine if switch matrix is available
   b. Determine if enough SMU instruments are available
   c. Build project structure
2. Build individual tests between stresses
   a. Make switch connection if switch matrix is used

b. Build new test using interactive test modules (ITMs)

c. Calculate device parameters using the formulator tool

d. Set up exit on compliance conditions

e. Export parameter values for degradation monitoring

f. Repeat steps b through e for monitoring more parameters

3. Repeat step 2 if there are multiple DUTs

4. Set up stress conditions in sub-site level

a. Set up stress time

b. Set up device stress conditions

i. Set up stress voltage

ii. Set up pin connections

iii. Set up target degradation values

iv. Go to next device

5. Run project and examine degradation data

Parameter degradation data and raw measurement data are saved automatically in Excel file format during the run time of the project. Therefore, even if the project is stopped before completion, the measured data has already been captured. The raw I-V curves between stresses can be overlaid on stress cycles, so it's easy to visualize how the I-V degrades as a function of stress time. ***Figure 9*** shows Vgs-Id curves from overlaying 21 stress cycles.

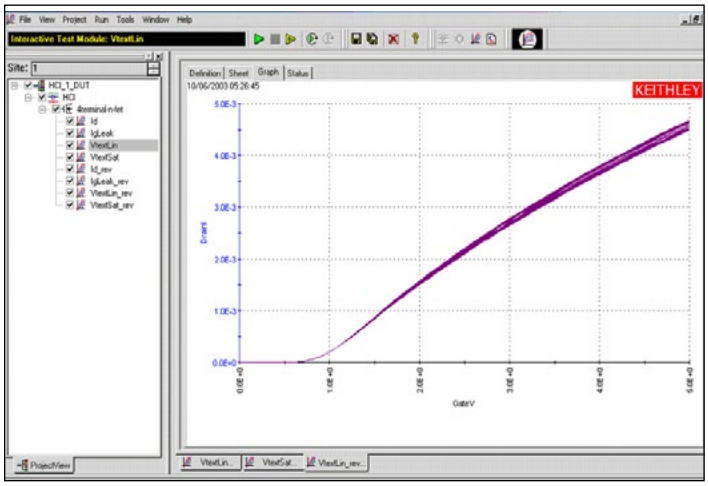


Figure 9. Plot of overlaid data from multiple stresses.

Figure 10 is an example of a CHC project that tests five sites on a wafer. The Model 4200-SCS controls prober movement from site to site through built-in drivers that are compatible with most common semi-automatic probe stations on the market.

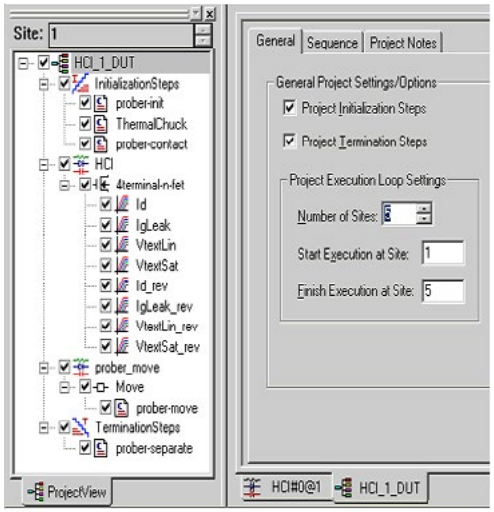


Figure 10. Example of a wafer level CHC test.

Conclusion

The enhanced stress-measure loop in KTEI Software allows setting up a CHC test without the need for any programming. Together with the interactive test interface, Formulator Tool, and powerful graphing capabilities, KTEI Software makes the Model 4200-SCS an ideal tool for evaluating device reliability parameters such as CHC induced degradation of MOSFETs, as well as its better-known role in device characterization.

References

1. JEDEC Standard 28-A, "Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress," 2001.
2. Vijay Reddy, "An introduction to CMOS semiconductor Reliability," IRPS Tutorial, 2004.

Electrical Characterization of Carbon Nanotube Transistors (CNT FETs) with the Model 4200-SCS Parameter Analyzer

Introduction

Carbon nanotubes (CNTs) have been the subject of a lot of scientific research in recent years, due not only to their small size but to their remarkable electronic and mechanical properties and many potential applications. The problems associated with attempting to scale down traditional semiconductor devices have led researchers to look into CNT-based devices, such as carbon nanotube field effect transistors (CNT FETs), as alternatives. Because they are not subject to the same scaling problems as traditional semiconductor devices, CNT FETs are being studied for a wide variety of applications, including logic devices, memory devices, sensors, etc. The research on these devices typically involves determining various electrical parameters, which may include current-voltage (I-V), pulsed I-V, and capacitance (C) measurements. Characterizing the electrical properties of delicate nanoelectronic devices requires instruments and measurement techniques optimized for low power levels and high measurement sensitivity.

The Model 4200-SCS Parameter Analyzer offers a variety of advantages for electrical characterization of CNT FETs. This configurable test system can simplify these sensitive electrical measurements because it combines multiple measurement instruments into one integrated system that includes hardware, interactive software, graphics, and analysis capabilities. The system comes with pre-configured tests for performing electrical measurements that have been optimized to ensure accurate results on CNT FETs. This application note explains how to optimize DC, pulsed I-V, and C-V measurements on a CNT FET using the Model 4200-SCS Parameter Analyzer. It includes detailed information on proper cabling and connections, guarding, shielding, noise reduction techniques, and other important measurement considerations when testing carbon nanotube transistors.

The Carbon Nanotube Transistor

A single semiconducting CNT can be used as the conducting channel between the source and drain of a FET. ***Figure 1*** illustrates a back-gated Schottky barrier CNT FET. Two metal contacts are located across both ends of the CNT to form the Source and Drain terminals of the FET. The CNT is placed atop an oxide that sits above a doped silicon substrate, which forms the Gate terminal. Connections are made to the three DUT terminals to perform the electrical measurements.

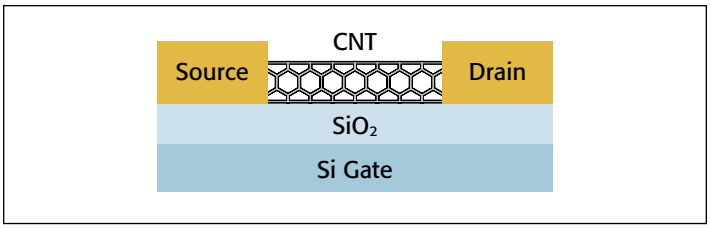


Figure 1. Back-gated carbon nanotube transistor

Making Electrical Measurements with the Model 4200-SCS

The Model 4200-SCS is supplied with a test project for making some of the most commonly used CNT FET measurements. This project (*CNTFET*) includes tests for I-V, pulsed I-V, and C-V measurements. The I-V tests are performed using two of the Model 4200-SMU Source Measure Unit (SMU) Instruments, both with the Model 4200-PA Preamp option. The pulsed and transient I-V measurements are made using the Model 4225-PMU Ultra Fast I-V Module with two Model 4225-RPM Remote/Preamplifier Switch options. Finally, the C-V measurements are

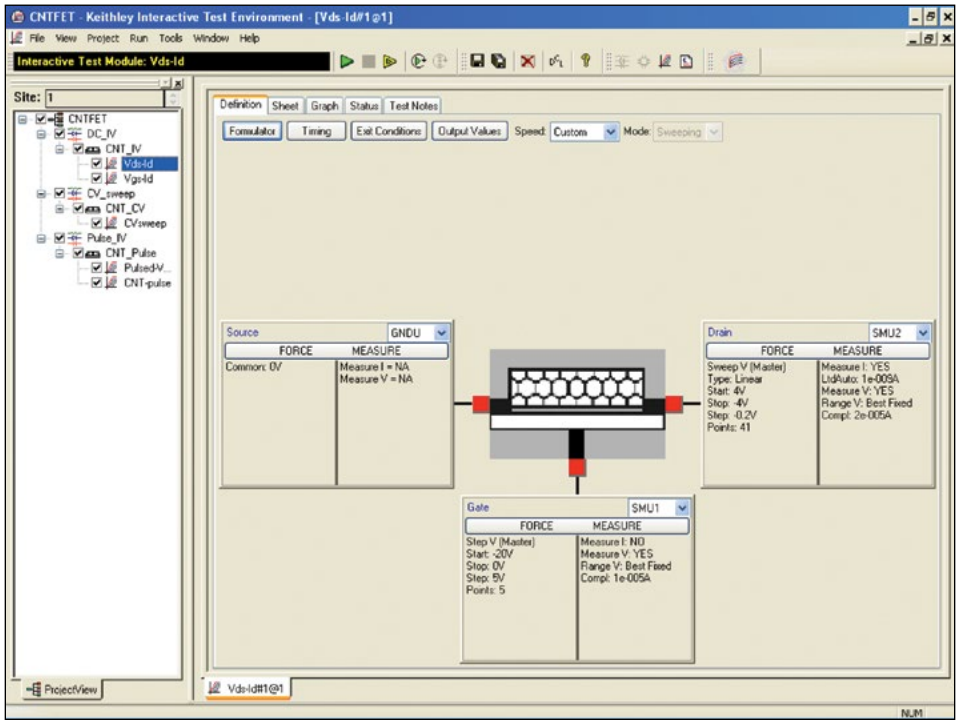


Figure 2. *CNTFET* project for the Model 4200-SCS

performed using the Model 4210-CVU C-V Measurement module.

The *CNTFET* project is included with all Model 4200-SCS systems running KTEI Version 8.1 or later. ***Figure 2*** shows the *CNTFET* project running in the Keithley Interactive Test Environment (KITE) software.

Current-Voltage Measurements

The I-V characteristics of a CNT transistor can be used to extract many of the device's parameters, study the effects of fabrication technique and process variations, determine the quality of the contacts, etc. ***Figure 3*** illustrates a DC I-V test configuration that incorporates two Model 4200-SMU Instruments. These SMU instruments are capable of sourcing and measuring both current and voltage; they have picoamp sensitivity and can be current-limited to prevent damage to the device. In this diagram, SMU1 is connected to the Gate of the CNT FET and SMU2 is connected to the Drain. The Source terminal is connected to the Ground Unit (GNDU) or to a third SMU instrument if it is necessary to source and measure from all three terminals of the FET.

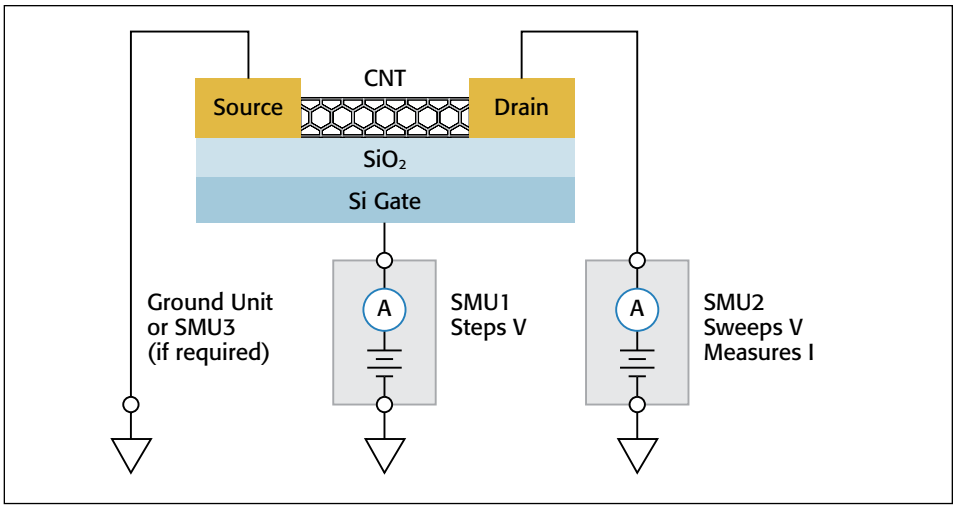


Figure 3. Circuit diagram for measuring the DC I-V characteristics of a CNT FET

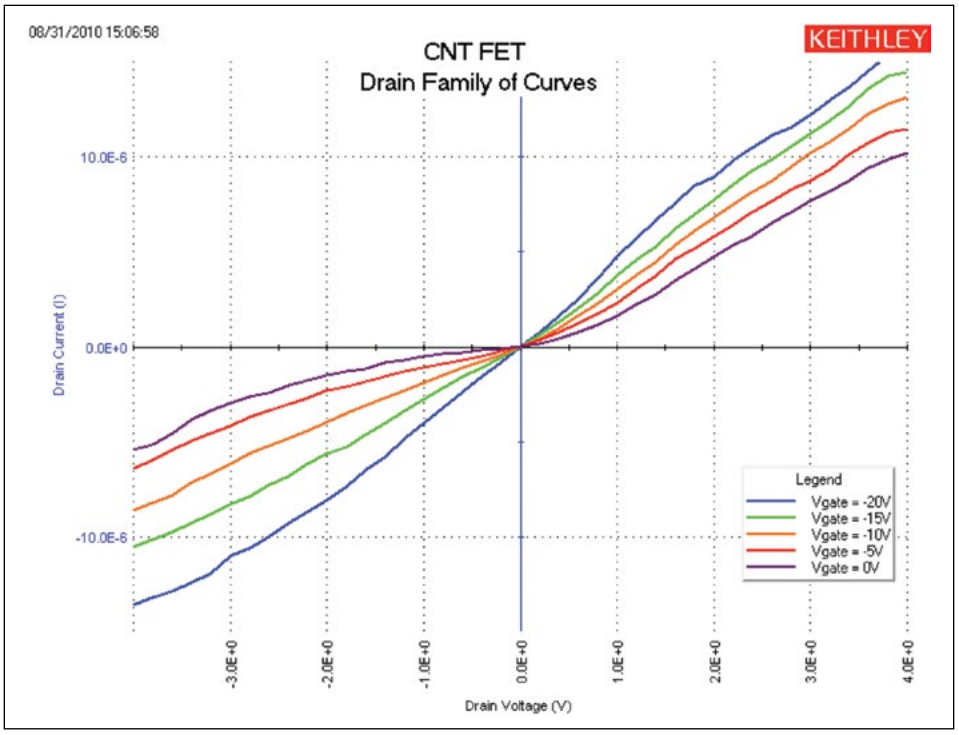


Figure 4. DC I-V drain family of curves measured by the Model 4200-SMU Source Measure Unit

In this example, the Model 4200-SCS's KITE software is set up to measure a DC drain family of curves (V_{ds}–I_d). As SMU1 steps the gate voltage (V_g), SMU2 sweeps the drain voltage (V_d) and measures the resulting drain current (I_d). ***Figure 4*** shows the resulting FET characteristics generated using the *CNTFET* project.

Without changing connections to the device, Model 4200-SCS's interactive KITE software simplifies performing other common I-V tests such as the drain current (I_d) vs. gate voltage (V_g) curves. For this test, the gate voltage is swept and the resulting drain current is measured at a constant drain voltage. The results of an I_d–V_g curve at a constant drain voltage are shown in ***Figure 5***. The drain voltage can also be stepped as the gate voltage is swept.

Optimizing DC measurements

The following techniques will improve the quality of DC measurements made on CNT FETs with the Model 4200-SCS:

- **Limit Current:** To prevent damage to the device while performing I-V characterization, the user should limit the amount of current that can flow through the device. This can be done in the software by setting the Current Compliance of each SMU to a safe level, such as 20μA. This is a programmed limit to ensure the current doesn't exceed the user-defined compliance.
- **Provide Sufficient Settling Time:** Because CNT FET measurements often involve measuring low current (<1μA), it is important to allow sufficient settling time to ensure the measurements are stabilized after a current or voltage has been applied. Some of the factors that affect the settling time of the measurement circuit include the cables, test fixtures, switches, probers, the DUT resistance, and the current range of the measurement instrument. To ensure settled readings,

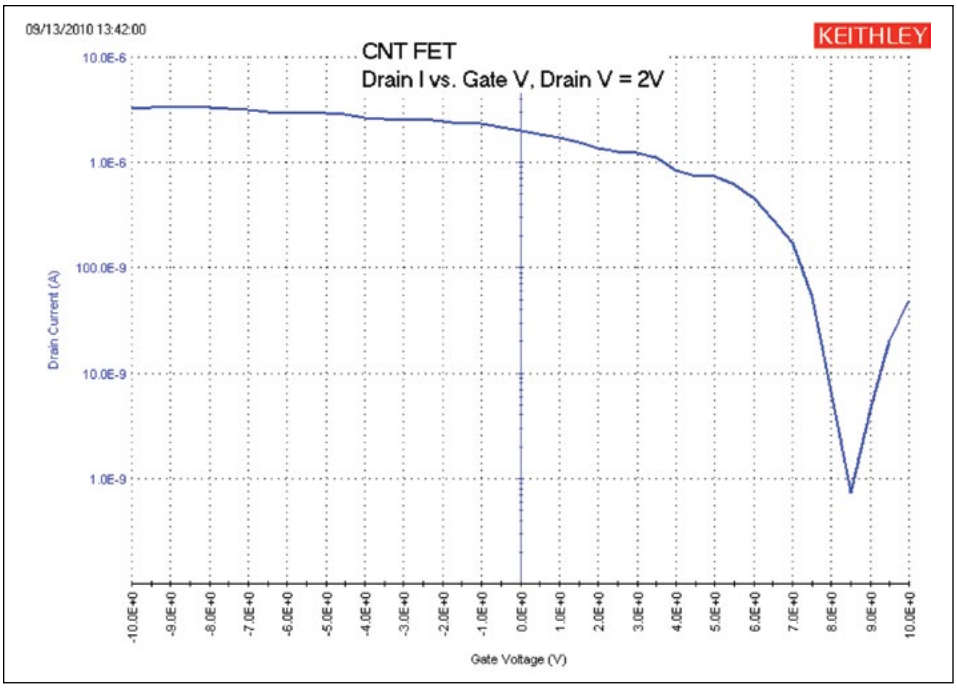


Figure 5. Drain current vs. gate voltage of CNT FET

additional delay time can be added to the voltage or current step time prior to the measurement. This delay time can be easily adjusted in the Timing Menu in the KITE software.

- **Use Proper Speed Modes:** The Timing Menu also offers Speed Modes, including Delay and Filter Factor settings, which affect the settling time of the reading, as well as the integration time of the measurement. Increasing the Delay Factor, Filter Factor, and the A/D Aperture Time can decrease noisy measurements.
- **Minimize Noisy Measurements:** Noise may be generated from a variety of sources, including particle collisions, defects, AC pick-up, and electrostatic interference. Noisy measurements result when a noise signal is superimposed on the DC signal being measured. This can result in inaccurate or fluctuating measurements.

  The most common form of external noise "pick-up" is 60Hz (or 50Hz) line cycle pick-up. This can be a common occurrence near fluorescent lights. Millivolts of noise are not uncommon. Keithley uses a technique called Line-Cycle Integration to minimize the effects of 60Hz (or 50Hz) line pick-up. Line-cycle noise will "average out" when the integration time is equal to an integral number of power line cycles. The number of power line cycles can be adjusted in the KITE software in the Timing Menu.

  Electrostatic interference is another cause of noisy measurements when measuring low currents. This coupling occurs when an electrically charged object approaches the circuit under test. In high impedance circuits, this charge doesn't decay rapidly and can result in unstable measurements. The erroneous readings may be due to either DC or AC electrostatic fields, so electrostatic shielding will help minimize the effects of these fields.

  The electrostatic shield can be just a simple metal box that encloses the test circuit. Probe stations often include an electrostatic/EMI shield or optional dark box. The shield should be connected to the measurement circuit LO, which is the Force LO terminal of the SMU. The Force LO terminal is the outside shield of the triax cable of the SMU or is located on the GNDU. All cables need to be of a low-noise design and shielded. Each Model 4200-SMU comes with two low-noise triax cables.
- **Keep Probes Up:** Make sure the probes are in the up position (not contacted to the device) when connecting and disconnecting instruments from the terminals of the device. The process of moving cables has the potential to inject charge into the device and cause damage. This is due to both triboelectric and piezoelectric effects.

Pulsed I-V Measurements

In addition to making traditional DC I-V measurements, it may be desirable to perform ultra-fast pulsed I-V measurements for various reasons. First, it may be important to observe the high speed response of the CNT device. In some cases, nanostructures can be destroyed by the heat generated when making traditional DC measurements. Pulsed I-V measurements can reduce the total energy dissipated in a device, and therefore reduce the potential for damage. Finally, pulsed electrical testing can prevent current drifting in measurements that can occur during DC measurements.

The pulsed I-V measurements on the CNT FET can be easily made using the Model 4225-PMU Ultra Fast I-V Module. The Model 4225-PMU provides two channels of high speed, multi-level voltage pulse output while simultaneously measuring current and voltage. This module replaces traditional pulse/measure test configurations, which consisted of a pulse generator, digital oscilloscope, interconnect hardware, and software.

The Model 4225-PMU has two modes of ultra-fast I-V source with measure: pulsed I-V and transient I-V. These two modes are illustrated in ***Figure 6***.

Pulsed I-V refers to any test with a pulsed source and a corresponding high speed, time-based measurement that provides DC-like results. The current and/or voltage measurement is an average of readings taken in a predefined measurement window on the pulse. This average of readings is called the "spot mean." The user defines the parameters of the pulse, including the pulse width, duty cycle, rise/fall times, amplitude, etc.

Transient I-V, or waveform capture, is a time-based current and/or voltage measurement that is typically the capture of a pulsed waveform. A transient test is typically a single pulse waveform that is used to study time-varying parameters, such as the drain current degradation versus time due to charge trapping or self-heating. Transient I-V measurements can be used to test a dynamic test circuit or as a diagnostic tool for choosing the appropriate pulse settings in the pulsed I-V mode.

Given that the Model 4225-PMU has two channels, only one module is needed to test a three-terminal CNT FET. A typical test configuration for connecting the PMU module to a CNT FET is shown in ***Figure 7***. In this diagram, Ch 1 of the PMU is connected to the Gate terminal and Ch 2 is connected to the Drain terminal. The Source terminal is connected to the PMU Common, which is the outside shield of the PMU coax connector. To connect this Common terminal to the probe tip, use a BNC or triax shorting plug that will connect the outside of the coax to the manipulator probe. To generate a V_{ds}–I_d curve, Ch 1 steps the gate voltage and Ch 2 sweeps the drain voltage and measures the resulting drain current.

Figure 8 illustrates a pulsed I-V drain family of curves taken with the Model 4225-PMU. For this measurement, a pulse width of 500μs was used to generate the curves. However, each PMU channel has the ability to output voltage pulses as short as 70ns with a rise time as short as 20ns. The minimum duration of the pulse width will depend on several factors, including the test circuit RC time constant and the magnitude of the test current. Each dot on the curves represents a "spot mean" measurement on the pulsed waveform.

The Model 4225-PMU has five ranges full scale from 800mA down to 100μA. To measure lower currents, using the Model 4225-RPM optional Remote Amplifier/Switch is recommended because it adds six measurement ranges, down to 100nA full scale. The pulsed I-V curves shown in ***Figure 8*** were taken on the 100μA range. The threshold current was set to 20μA so that the test will stop if the threshold current level is reached.

For some applications, it may be necessary to study the transient response of a CNT FET. If this is the case, the waveform capture mode (transient I-V) can be used to capture the current and voltage time-based response to the device. ***Figure 9*** shows the transient response of the CNT FET. The blue curve is the pulsed drain voltage and the red curve is the resulting current response as a function of time.

The blue voltage output curve looks close to the defined rise and fall times of 10μs with a pulse width of 50μs. Note that the pulse width is measured at one-half of the input amplitude of 1V. Therefore, the pulse width is measured at 500mV. The sample period in this example is 25ns (40MHz rate). With proper cabling and connections, the voltage shape should be output as defined by the user with minimal deviation.

The red curve shows the drain current and is plotted on the right Y-axis. The drain current is measured at constant drain and gate voltages. The peaks in the curve are caused by charging

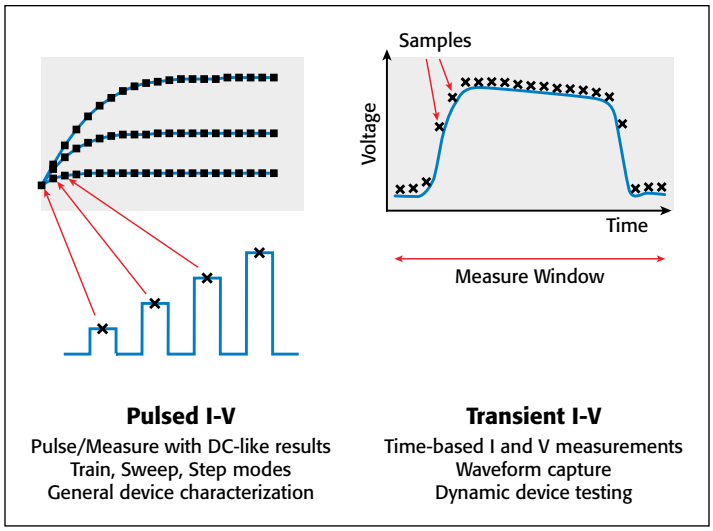


Figure 6. Two modes of ultra fast I-V source with measure: Pulsed I-V and Transient I-V

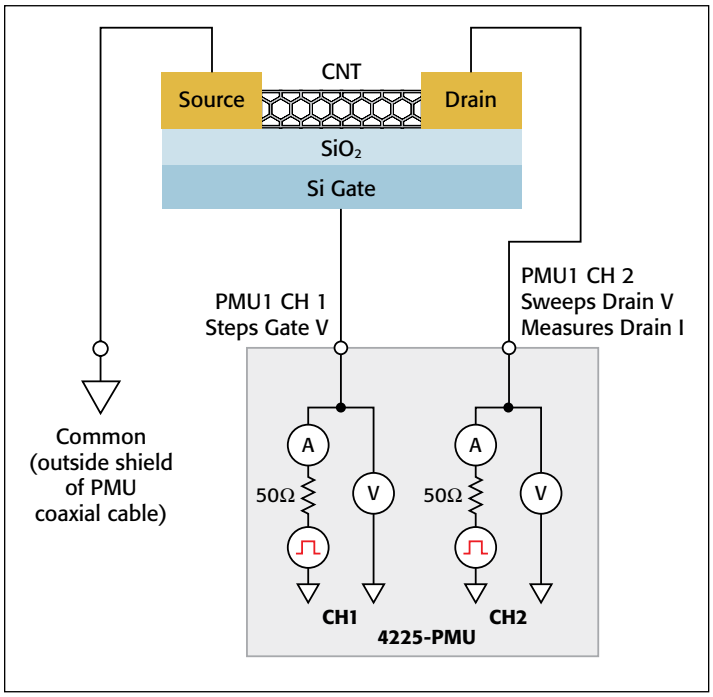


Figure 7. Circuit diagram for measuring the pulsed I-V characteristics of a CNT FET

and discharging of the cabling, as well as the current flow through the device. Note that these peaks occur during the pulse transitions. Reducing the pulse amplitude or increasing the pulse transition time reduces the dV/dt, which reduces the peak height.

Optimizing Pulsed I-V Measurements

To improve the quality of pulsed I-V measurements made with the Model 4200-SCS, follow these guidelines:

- **Use the Right Cables and Connections:** Using proper cabling and connections is important for ultra-fast I-V applications in order to achieve the highest frequency output and to avoid signal distortions and capacitive charging effects.

- Use cabling and connections optimized for high frequency (at least 150MHz).
- Use a signal path that matches the impedance of the instrument (50 ohms).
- Tie the low side of the DUT to the shield of the PMU coax cable.
- Connect the shields from each PMU channel together as close as possible to the DUT.
- Minimize the loop area once the center conductor and shield are separate in the test circuit.
- Minimize the cable length.

- **Make the Right Chuck Connections:** CNT FETs and other nanotransistors may be either back-gated or top-gated. For back-gated devices, one of the PMU channels needs to be connected to the chuck of the prober. When making PMU connections to the chuck, the user will give up some functionality of the PMU: fast transitions, high frequency, low current, etc. This is because the output of the high frequency PMU channel is connected to the chuck capacitance and the chuck cabling, which slows down the source response and couples noise into the measurement. If possible, it is better to use a third manipulator and probe directly to the chuck. For high speed sourcing and measuring, it is best to use all top-side connections and avoid connecting the PMU to the chuck.
- **Verify Pulse Width:** Ensure the pulse width is long enough to ensure a settled reading. Verify the resulting current measurement is settled by outputting a single pulse using the Waveform Capture mode. Both the current and voltage can be plotted as a function of time in the Graph tab.
- **Minimize Noise:** To minimize noisy results, multiple waveforms can be averaged or a moving average function can be created in the built-in Formulator to smooth out the measurements further.

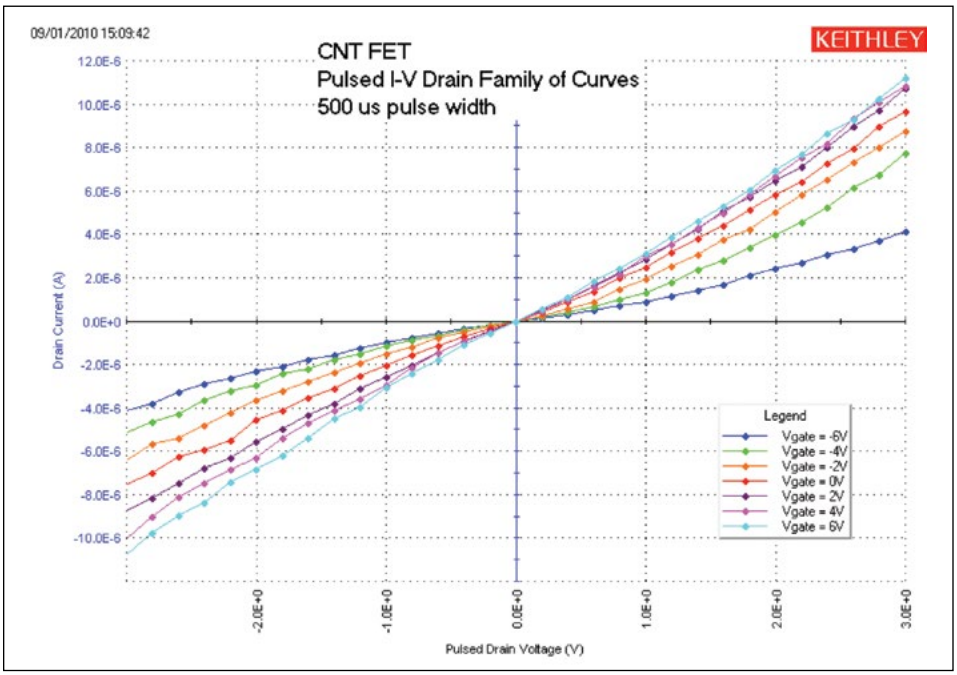


Figure 8. Pulsed I-V drain family of curves of CNT FET

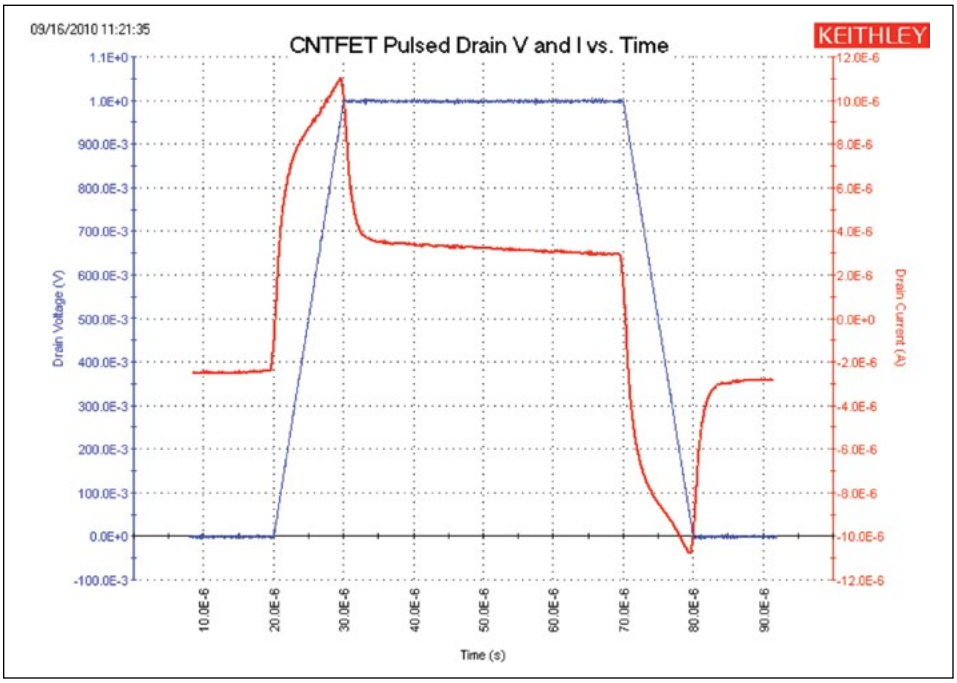


Figure 9. Waveform of single drain voltage pulse and resulting drain current of CNT FET

Capacitance-Voltage Measurements

In addition to performing DC and pulsed I-V measurements on CNT FETs, measuring the capacitance of the FET can also provide information about the device, including the mobility, timing effects, and gate dielectrics. ***Figure 10*** outlines the connections of the Model 4210-CVU to the CNT FET. In this configuration, the gate-to-drain capacitance is measured as a function of the gate voltage.

The HCUR/HPOT terminals that connect the high of the voltage source to the gate should be connected to the chuck. The LCUR/LPOT terminals that measure the capacitance should be connected to the drain terminal of the

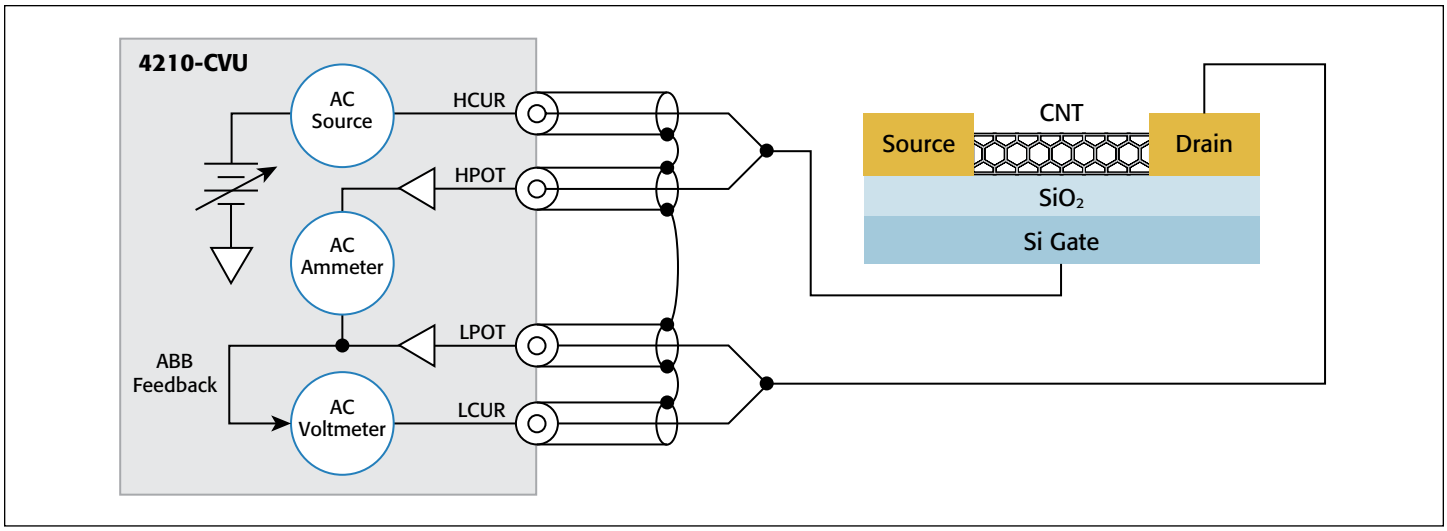


Figure 10. Connections of the Model 4210-CVU to a CNT FET

DUT. For best results, the measurement terminals should never be connected to the chuck. For top-gated CNT FETs, both the measure and voltage source can be output to the gate of the FET from the same terminals (either HCUR/HPOT or LPOT/LCUR) of the CVU. The HI and LO terminals of the CVU are interchangeable in the Force Measure Window of the CVU in the KITE software. The results of generating a C-V sweep between the gate and drain of the CNT FET are shown in ***Figure 11***.

Optimizing Capacitance Measurements

To improve the quality of capacitance measurements made with the Model 4200-SCS, follow these guidelines:

- **Perform Open Compensation (for Measurements <10pF):** The open correction feature compensates for capacitance offsets in the cabling and connections. Performing the correction is a two-part process. The corrections are performed, and then they are enabled within a test module.

  To perform the corrections, open the Tools Menu and select CVU Connection Compensation. For an Open correction, click on Measure Open. Probes must be up or the DUT removed from the test fixture. Enable the correction by clicking on the Compensation button in the Forcing Functions/Measure Options window.

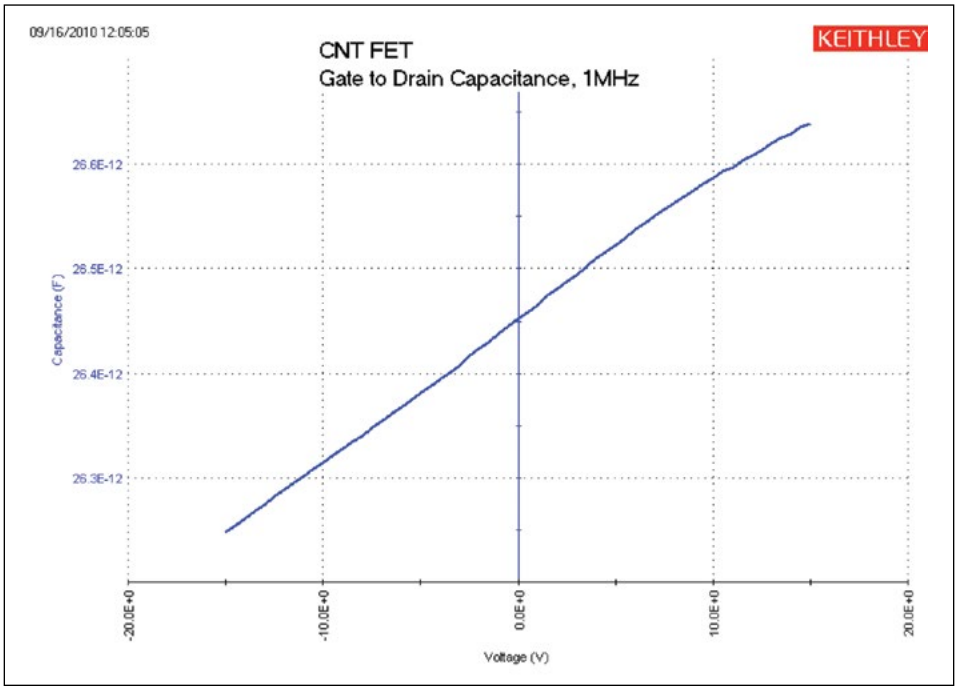


Figure 11. C-V sweep of gate-to-drain capacitance

- **Use Proper Shield Connections:** Connect the shields of the coax cables together as close as possible to the DUT. This reduces the loop area of the shields, which minimizes the inductance. This also helps to maintain the transmission line effects. If the shields are not connected together, offsets may occur. The higher the frequency, the more important this becomes.

- **Choose Appropriate Hold and Sweep Delay Times:** The condition of a device when all internal capacitances are fully charged after an applied voltage step is referred to as "equilibrium." If capacitance measurements are made before the device is in equilibrium, inaccurate results may occur.

  To choose the delay times for a C-V sweep, step an applied voltage using the Sampling Mode, and plot the

capacitance as a function of time. Observe the settling time from the graph. Use this time for the Hold Time for the initial applied voltage or for the Sweep Delay Time applied at each step in the sweep. The Sweep Delay Time may not need to be as long as the first step. The user will need to experiment to verify the appropriate time.

- **Choose Appropriate Speed Mode in Timing Menu:** The Speed mode function enables the user to adjust the time for settling and integration of the measurement. For small capacitances (pico-Farads or less) use the Quiet or Custom Speed modes for best results.
- **Use Guarding:** When making very small capacitance measurements, guarding will help prevent stray capacitance from unused terminals of the device from affecting measurement accuracy. For example, if measuring the capacitance between only the gate and drain terminals, the source terminal of the FET can be connected to the guard. The guard terminal of the Model 4210-CVU is the outside shield of the coax cable.

Conclusion

When using the appropriate instrumentation and measurement techniques, optimal electrical characterization of CNT FETs can be achieved. The Model 4200-SCS is an ideal tool for performing electrical characterization of CNT FETs and other nanostructures because of its integrated hardware, software, and analysis tools. The Model 4200-SMU Source Measure Unit Instrument can be used to determine V_{ds}–I_d, V_{GS}–I_d, resistance, and other I-V measurements on the CNT FET. The Model 4225-PMU Ultra-Fast I-V Module can be used to make pulsed I-V measurements or observe the transient response of a pulsed waveform applied to the DUT. The Model 4210-CVU Capacitance Meter can be used to generate C-V, C-f, or C-t curves. Using the *CNTFET* project that comes with the Model 4200-SCS can further simplify measurement setup and execution.

Acknowledgement

The author appreciates the assistance provided by Sandia National Labs, Livermore, California, who supplied the CNT FETs used in the device testing process during the development of this application note.

Making Proper Electrical Connections to Ensure Semiconductor Device Measurement Integrity

Introduction

Poor-quality electrical connections to the device under test (DUT) can compromise the measurement integrity of even the most powerful and sophisticated semiconductor test system. For high speed pulse measurements, interconnect quality typically determines maximum bandwidth; for low current measurements, it often affects measurement speed and accuracy. This application note discusses the problems created by poor connections. Although it specifically addresses MOSFET measurements, the techniques and results discussed also apply to many other devices.

V_{DS}–I_{DS} curves

The most straightforward way to assess a MOSFET's overall performance is to take V_{DS}–I_{DS} curves for a set of gate voltages because these curves define the operating regions of the device. Pulsed I-V characterization, wherein voltages and currents are applied for a very short time and at a limited duty cycle, is a common way to measure these curves. Pulsed I-V measurements can reduce test times and allow characterizing a device without exceeding its safe operating area or causing device self-heating and the associated parameter shifts.

Two pulsed I-V channels are typically used to measure these curves on a MOSFET, with one connected to the gate and the other to the drain. The ground of each channel is connected to the MOSFET source pin.

To construct the transistor curves, the gate channel first applies voltage to the gate, then the drain channel sweeps V_{DS} through a range of values, measuring the resulting current at each point. Next, the gate channel applies a different voltage to the gate and the process repeats, constructing the next transistor curve in the set.

Modern pulse instruments can produce very short voltage pulses (100ns or less) with rise times as fast as 20ns, so wide bandwidth is critical to obtaining good measurements. For optimal performance, both pulse generator channels should be connected with coaxial cables matched to the generator's 50Ω output impedance. However, it is impossible to maintain 50Ω impedance all the way to a device on a wafer in practice; at some point, the ground must be connected to one pin and the signal to another, breaking 50Ω characteristic impedance (***Figure 1***). Minimizing the length of these non-coaxial ground and signal connections is crucial.

Figures 2a and ***2b*** illustrate how inadequate grounding and coaxial cabling can produce erroneous data when

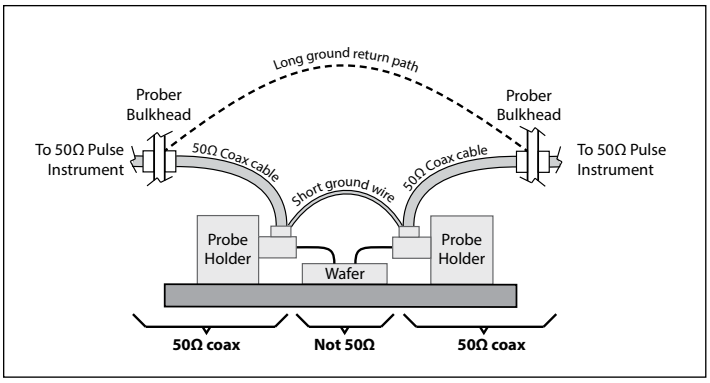


Figure 1. Prober hookups usually do not maintain 50W all the way to the DUT. If the short ground wire is not used, the much longer ground return path will limit bandwidth.

characterizing a MOSFET using pulses with 20ns rise times, 20ns fall times, and a width of 200ns. ***Figure 2a*** shows data taken with 100W impedance triaxial cables and 1–2 ft. ground connections. ***Figure 2b*** shows data taken with 50Ω impedance coaxial cables and ground connections just a few inches long. The difference is striking: the data from an improperly cabled system are compressed (***Figure 2a***), measuring about half the level expected, while the data from the correctly cabled system (***Figure 2b***) match conventionally measured data.

Maximum g_m and V_{TH}

Transconductance (g_m) is a critical parameter widely used to determine the threshold voltage (V_{TH}) of MOSFETs [1]. Pulsed I-V testing is ideal for this application because these parameters can be determined without violating safe operating area (SOA) limits or damaging the device.

For a small signal analysis about a given gate and drain bias point, g_m is defined as:

$$g_m = \frac{\partial i_{DS}}{\partial V_{GS}} \; g_m = \frac{\partial i_{DS}}{\partial V_{GS}} \qquad (1)$$

When measuring gm, the same connection scheme used to obtain the data in ***Figures 2A*** and ***2B*** is used, but this time a DC voltage is applied to the drain while the gate voltage (V_{GS}) is swept over the voltage range that transitions the device from off to on. Because the connections and pulsing speeds are the same, the earlier bandwidth discussion applies to g_m and V_{TH} testing as well.

Figures 3a and ***3b*** show the results of another example of g_m and V_{TH} measurement, with the data shown in each taken with the same pulse rise and fall times, pulse widths, connections, and grounding. As Eq. 1 states, calculating gm requires

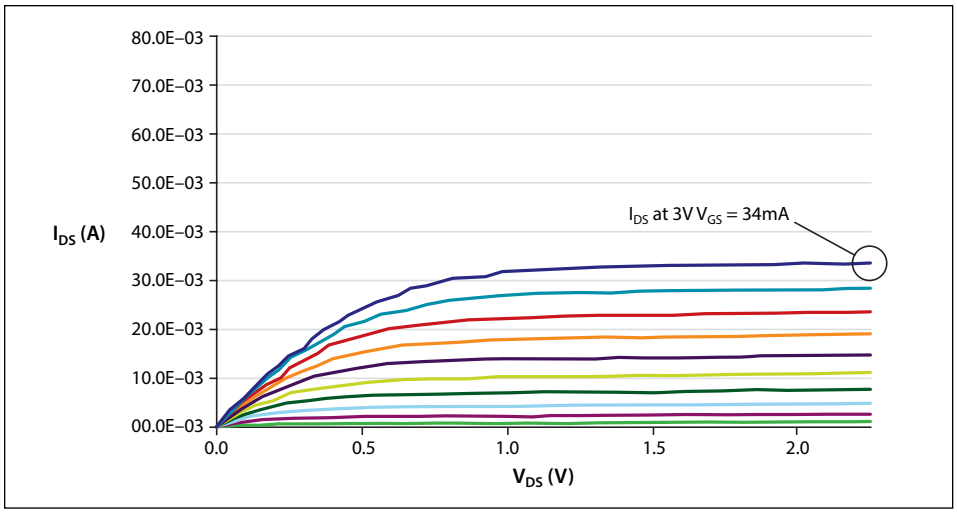


Figure 2A. MOSFET curves with poor cabling and grounding. I_{DS} at a V_{GS} of 3V is measured as 34mA.

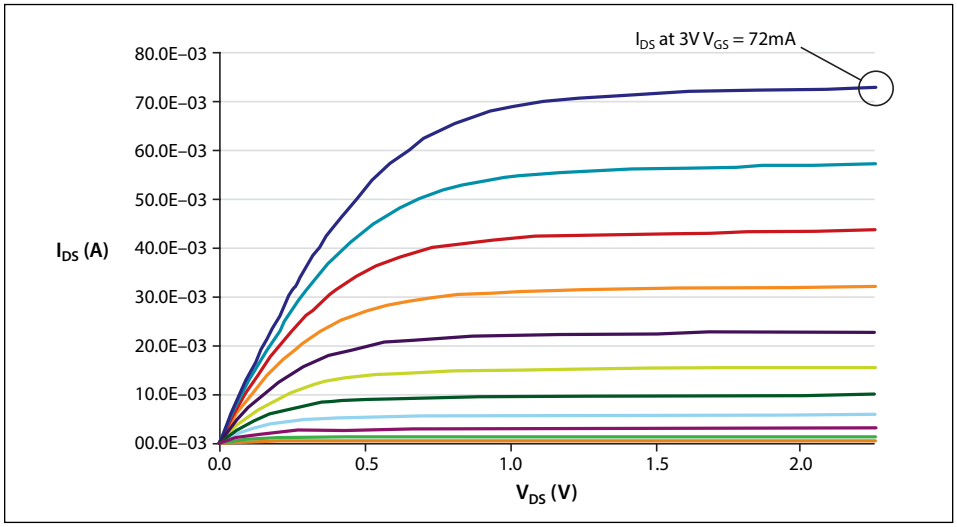


Figure 2B. MOSFET curves with optimal cabling and grounding. I_{DS} at a V_{GS} of 3V is measured as 72mA.

computing the first derivative of the drain current with respect to the gate voltage. The blue curve is the drain current and the red curve is its calculated derivative.

Just as with the V_{DS}–I_{DS} curves, the difference is significant. The results produced using the improperly cabled setup would mislead the user to think the DUT's gm is half its actual value and its V_{TH} roughly 200mV higher than it actually is.

Capacitance-Voltage Testing

Capacitance-voltage (C-V) measurements are often used to characterize a MOSFET's gate oxide thickness, oxide defect density, doping profiles, etc. In this measurement, as the gate voltage varies, the capacitance of the gate to the drain and source changes. The Model 4210-CVU option allows Keithley's Model 4200-SCS Parameter Analyzer to make 1kHz–10MHz C-V measurements. It has four terminals wired to two device connections: CVU high and CVU low. In a standard C-V measurement, the source, bulk, and drain of a MOSFET are connected together and tied to CVU low; the gate is connected to CVU high. The Model 4210-CVU applies a DC bias and a small AC voltage to bias the transistor and simultaneously measure its capacitance, returning capacitance values for a wide range of bias voltages.

C-V measurements can be made at many frequencies (sometimes greater than 1MHz), depending on the parameters to be extracted. At higher frequencies, transmission line effects and cable length can impact measurement integrity significantly. For optimal C-V measurements, DUTs must be connected to the instrumentation using coaxial cables of the proper length and impedance level; for example, the Model 4210-CVU uses 1.5-meter, 100Ω cables.

Although using cables longer than those provided with the instrument will cause large changes in data at high frequencies, a feature known as cable length compensation can mitigate this problem. Using cables of different characteristic impedances, such as when coaxial cables are improperly adapted to triaxial cables, will also produce increased measurement error at high frequencies.

Off-State Leakage

Characterizing off-state leakage is critical to understanding quiescent power dissipation and transistor quality for small-scale parameter transistors. A source measure unit (SMU) instrument capable of measuring picoamp-level (1E–12A) currents is essential.

As with any low current measurement, properly guarded triaxial cables are essential. Using coaxial cables will produce erroneous results due to high cable capacitance (50Ω coaxial cables typically have 30pF of capacitance per foot). This capacitance must be charged with high currents before small currents flowing in the DUT can be measured, extending settling times substantially.

Triaxial cables alleviate this problem by providing a third conductor between the center pin and shell, called the guard, driven at the same potential as the center pin. The guard conductor drastically reduces the effective capacitance and reduces settling times. Never use poor-quality triaxial cables, which can introduce problematic dielectric absorption, triboelectric effects, or high noise. Unguarded cable segments should be minimized. For best performance, triaxial cables should be run as close to the DUT as possible.

Match the Cable to the Measurement

As these examples illustrate, matching cabling and grounding to the measurement type enhances measurement integrity. However, changing cables for each measurement type is so time-consuming many users simply tolerate the suboptimal results. Moreover, whenever cables are rearranged, users run the risk of reconnecting them improperly, thereby causing errors and demanding extra troubleshooting time. Worse still, these errors may go unnoticed for a long time.

One alternative is to use a remote switch capable of handling I-V, C-V and pulsed I-V signals, such as Keithley's Model 4225-RPM Remote Amplifier/Switch. When combined with a multi-measurement performance cable kit, such as Keithley's 4210-MMPC kit, it can often eliminate the need to recable between tests. This kit delivers the correct impedance and cable type, allowing low current, high speed pulse, and C-V measurements with no manipulator reconnection, eliminating the need to reprobe wafers.

Given the importance of characterizing semiconductor devices quickly and accurately, the value that the latest cable solutions can provide to device researchers is obvious.

References

1. X. Zhou, K. Y. Lim, and D. Lim. A Simple and Unambiguous Definition of Threshold Voltage and Its Implications in Deep-Submicron MOS Device Modeling. IEEE Transactions on Electron Devices, Vol 46, No. 4, p. 807. April 1999.

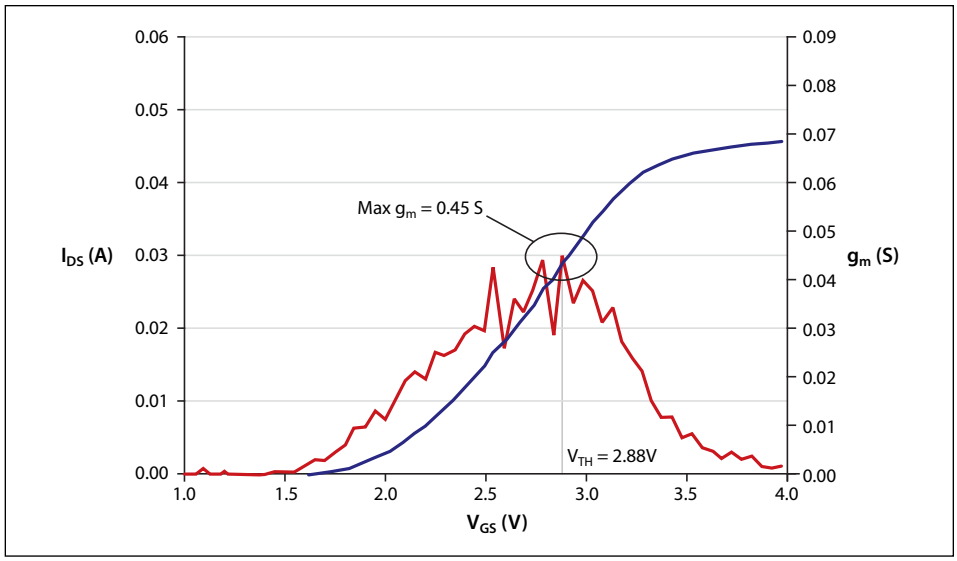


Figure 3a. g_m test with poor cabling and grounding.

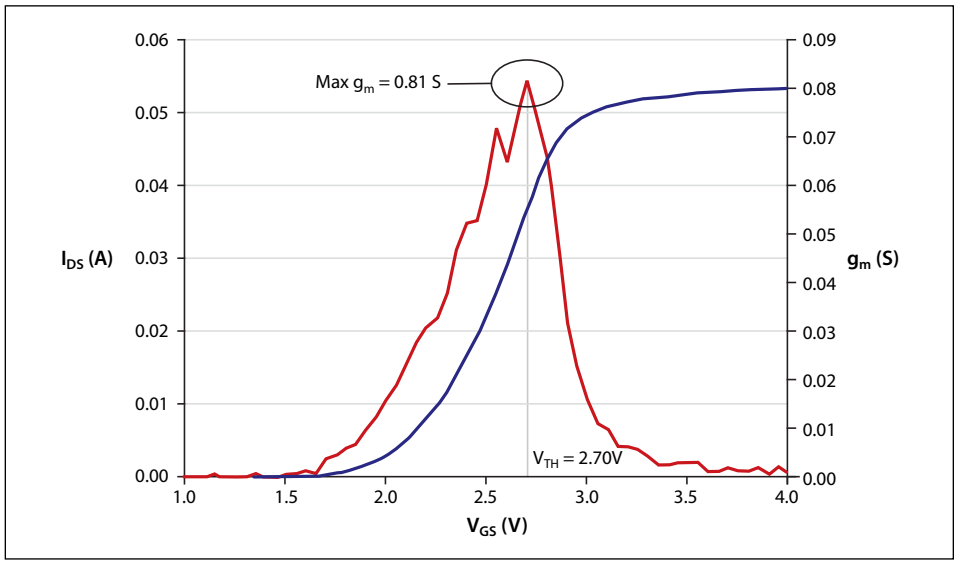


Figure 3b. g_m test with optimal cabling and grounding. From this measurement, g_m is 0.81 S and V_{TH} is 2.70V.

Four-Probe Resistivity and Hall Voltage Measurements with the Model 4200-SCS

Introduction

Semiconductor material research and device testing often involve determining the resistivity and Hall mobility of a sample. The resistivity of semiconductor material is primarily dependent on the bulk doping. In a device, the resistivity can affect the capacitance, the series resistance, and the threshold voltage.

The resistivity of the semiconductor is often determined using a four-point probe technique. With a four-probe, or Kelvin, technique, two of the probes are used to source current and the other two probes are used to measure voltage. Using four probes eliminates measurement errors due to the probe resistance, the spreading resistance under each probe, and the contact resistance between each metal probe and the semiconductor material. Because a high impedance voltmeter draws little current, the voltage drops across the probe resistance, spreading resistance, and contact resistance are very small.

Two common Kelvin techniques for determining the resistivity of a semiconductor material are the four-point collinear probe method and the van der Pauw method. The Model 4200-SCS Parameter Analyzer can be used for both. Because of its high input impedance ($>10^{16}\Omega$) and accurate low current sourcing, the Model 4200-SCS with preamps is ideal for high resistance samples. This application note explains how to make resistivity measurements of semiconductor materials using the Model 4200-SCS.

The Four-Point Collinear Probe Method

The most common way of measuring the resistivity of a semiconductor material is by using a four-point collinear probe. This technique involves bringing four equally spaced probes in contact with a material of unknown resistance. The probe array is placed in the center of the material, as shown in ***Figure 1***.

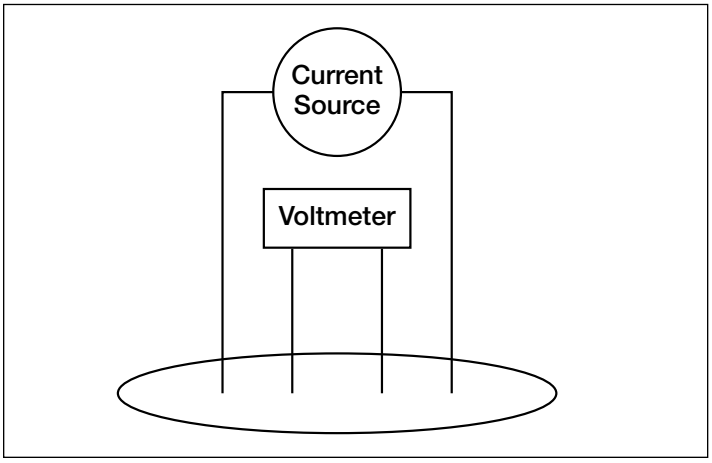


Figure 1. Four-Point Collinear Probe Resistivity Configuration

The two outer probes are used for sourcing current and the two inner probes are used for measuring the resulting voltage drop across the surface of the sample. The volume resistivity is calculated as follows:

$$\rho = \frac{\varpi}{\ln 2} \times \frac{V}{I} \times t \times k$$

where: ρ = volume resistivity (Ω-cm)
V = the measured voltage (volts)
I = the source current (amperes)
t = the sample thickness (cm)
k* = a correction factor based on the ratio of the probe to wafer diameter and on the ratio of wafer thickness to probe separation

* The correction factors can be found in standard four-point probe resistivity test procedures such as SEMI MF84-02—Test Method for Measuring Resistivity of Silicon Wafers With an In-Line Four-Point Probe.

Using the Model 4200-SCS to Make Four-Point Collinear Probe Measurements

The Model 4200-SCS can make four-point collinear probe measurements using either three or four source measure unit (SMU) instruments. When using three SMU instruments, all three are set to Current Bias (voltmeter unit). However, one SMU instrument will source current and the other two will be used to measure the voltage difference between the two inner probes. An example of how this can be set up with the Model 4200-SCS is shown in ***Figure 2***. One SMU instrument (SMU1) and the GNDU (ground unit) are used to source current between the outer two probes. Two other SMU instruments (SMU2 and SMU3) are used to measure the voltage drop between the two inner probes.

This four-point probe measurement can be set up in the Model 4200-SCS's Keithley Interactive Test Environment (KITE) by using the following steps:

1. Begin a new project.
2. Create a new sub-site plan.
3. Add a new device for a generic or custom-designed four-terminal device.
4. Add an ITM (Interactive Test Module) and set up the SMU instruments as shown in ***Figure 2***. Make sure that the Current Measurement option is checked for SMU1, which is set up as a Current Bias. This current source value will be used to calculate the resistivity. Click the check boxes for the

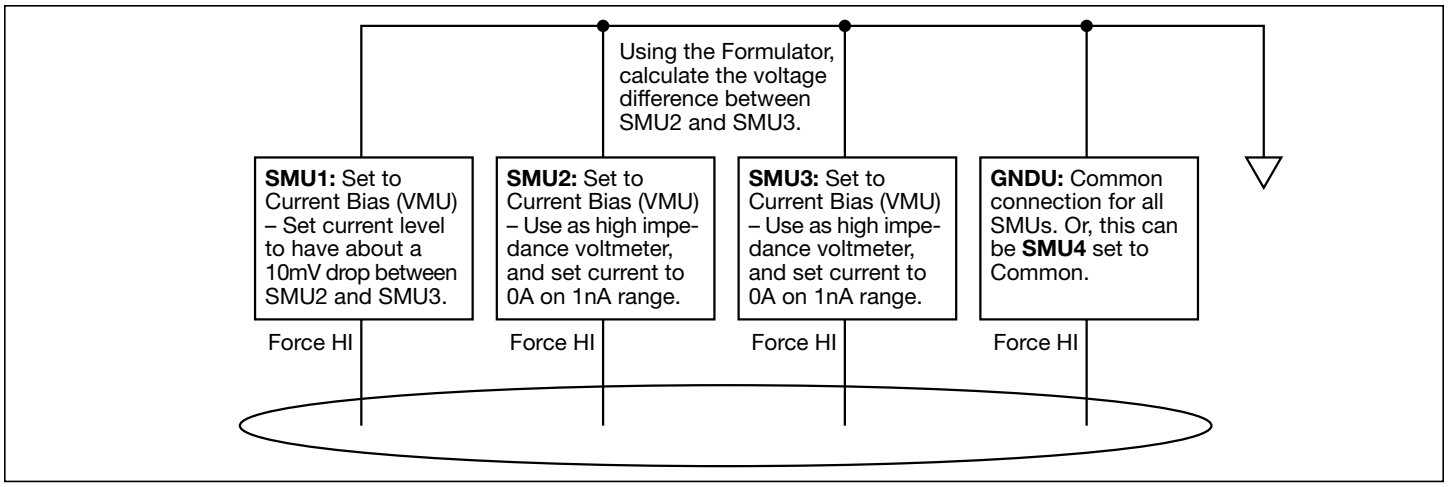


Figure 2. SMU Instrument Designation for Four-Point Collinear Probe Measurement

Voltage Measure options for SMU2 and SMU3. Set the source range for SMU2 and SMU3 to 1nA. In general, the current source range determines the input impedance of the SMU instrument as a voltmeter. The lower the current range is, the higher the input impedance will be.

5. Change the mode to "Sampling."
6. In the ITM Timing menu, choose the number of samples to take. If the Timestamp Enabled option is selected, graphs of voltage vs. time can be plotted and used to determine the settling time.
7. In the Formulator menu, type in the formula for the sheet resistivity. First, calculate the voltage difference between SMU2 (BV) and SMU3 (CV). This is VDIFF=BV-CV. For the sheet resistivity (ohms/square), RESISTIVITY=4.532*(VDIFF/AI). To determine the volume resistivity, multiply the sheet resistivity by the thickness of the sample in centimeters (cm).
8. After connecting the four-point probe to the wafer, run the program by clicking on the green arrow key. The final resistivity value will be shown in the RESISTIVITY column of the data sheet.

Example Application for Making Four-Point Collinear Probe Measurements with the Model 4200-SCS

An example four-point probe resistivity application has already been created for the Model 4200-SCS. This project was developed using the steps described previously. The name of the project is *FourPtProbe*. A screen capture of the project is shown in ***Figure 3***. A custom-designed device structure is used to illustrate the four-point measurement.

In this project, three SMU instruments and the GNDU (ground unit) are used to measure the resistivity. For SMU1, enter an appropriate test current, depending on the resistivity of the sample. The green arrow key is used to execute the project. Under the Sheet tab, the resistivity will appear. A correction factor may be applied by using the Formulator menu or by entering a formula on the Calc sheet within the Sheet tab.

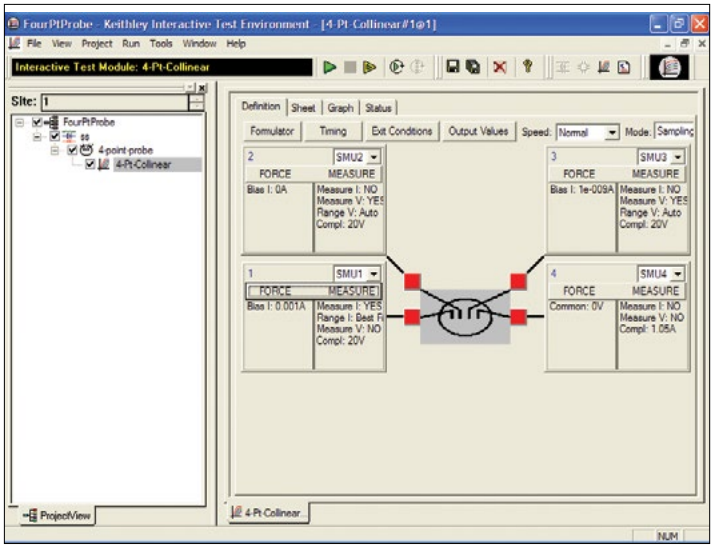


Figure 3. Screen Capture of Model 4200-SCS with the Four-Point Probe Project

van der Pauw Resistivity Measurement Method

The van der Pauw method involves applying a current and measuring voltage using four small contacts on the circumference of a flat, arbitrarily shaped sample of uniform thickness. This method is particularly useful for measuring very small samples because geometric spacing of the contacts is unimportant. Effects due to a sample's size, which is the approximate probe spacing, are irrelevant.

Using this method, the resistivity can be derived from a total of eight measurements that are made around the periphery of the sample with the configurations shown in ***Figure 4***.

Once all the voltage measurements are taken, two values of resistivity, ρ_A and ρ_B, are derived as follows:

$$\rho_A = \frac{\pi}{\ln 2} f_A t_s \frac{(V_1 - V_2 + V_3 - V_4)}{4I}$$

$$\rho_B = \frac{\pi}{\ln 2} f_B t_s \frac{(V_5 - V_6 + V_7 - V_8)}{4I}$$

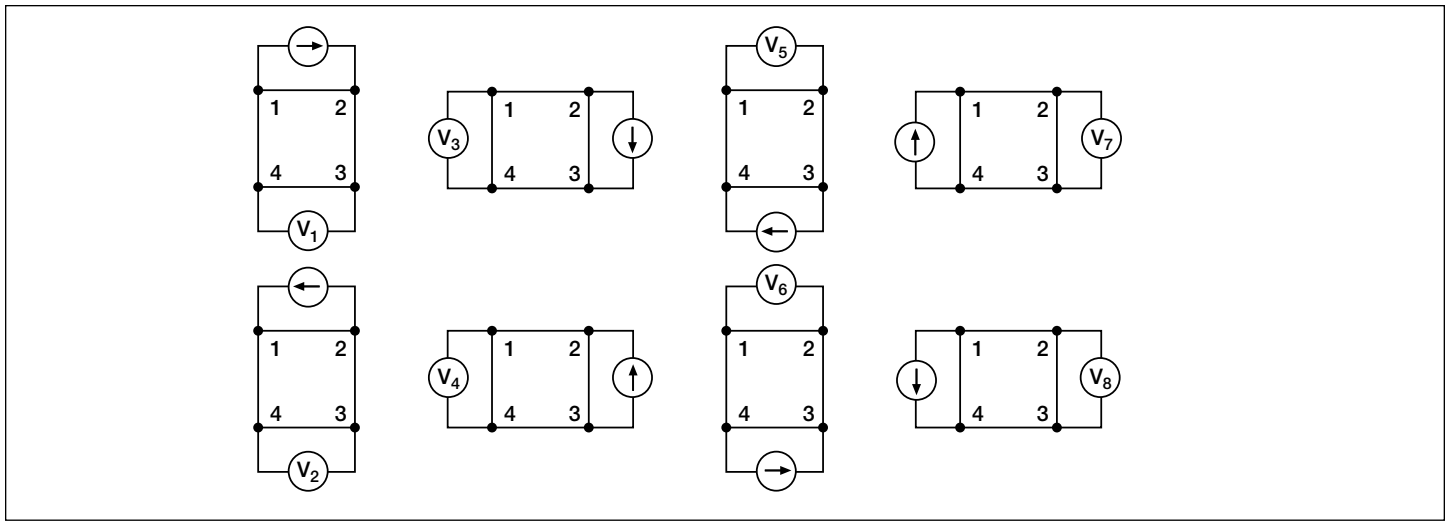


Figure 4. van der Pauw Resistivity Conventions

where: ρ_A and ρ_B are volume resistivities in ohm-cm;

t_s is the sample thickness in cm;

V_1–V_8 represents the voltages measured by the voltmeter;

I is the current through the sample in amperes;

f_A and f_B are geometrical factors based on sample symmetry. They are related to the two resistance ratios Q_A and Q_B as shown in the following equations ($f_A = f_B = 1$ for perfect symmetry).

Q_A and Q_B are calculated using the measured voltages as follows:

$$Q_A = \frac{V_1 - V_2}{V_3 - V_4}$$

$$Q_B = \frac{V_5 - V_6}{V_7 - V_8}$$

Also, Q and f are related as follows:

$$\frac{Q - 1}{Q + 1} = \frac{f}{0.693} \text{ arc cosh} \left(\frac{e^{0.693/f}}{2} \right)$$

A plot of this function is shown in ***Figure 5***. The value of f can be found from this plot once Q has been calculated.

Once ρ_A and ρ_B are known, the average resistivity (ρ_{AVG}) can be determined as follows:

$$\rho_{AVG} = \frac{\rho_A + \rho_B}{2}$$

Test Equipment

The electrical measurements for determining van der Pauw resistivity require a current source and a voltmeter. To automate measurements, one might typically use a programmable switch to switch the current source and the voltmeter to all sides of the sample. However, the Model 4200-SCS is more efficient than this.

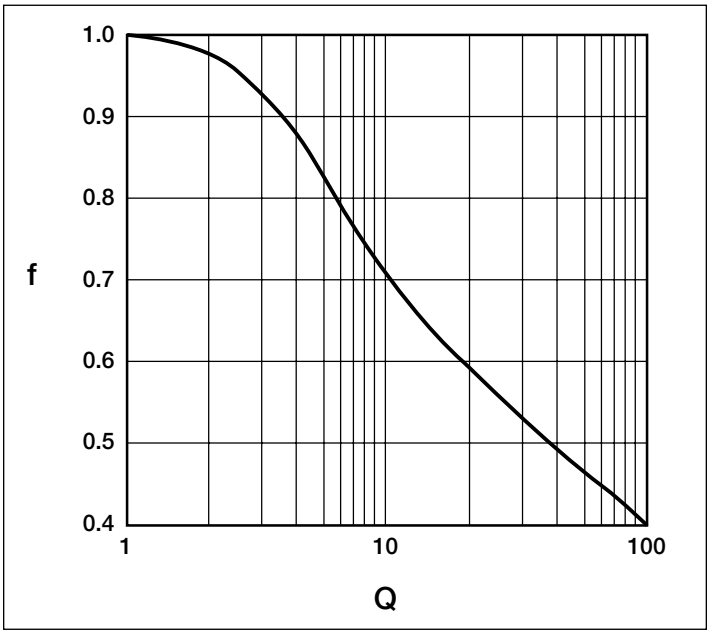


Figure 5. Plot of f vs. Q

The Model 4200-SCS with four SMU instruments and four preamps (for high resistance measurements) is an ideal solution for measuring van der Pauw resistivity, and should enable measurements of resistances greater than $10^{12}\Omega$. Since each SMU instrument can be configured as a current source or as a voltmeter, no external switching is required, thus eliminating leakage and offsets errors caused by mechanical switches. This removes the need for additional instruments and programming.

For high resistance materials, a current source that can output very small current with a high output impedance is necessary. A differential electrometer with high input impedance is required to minimize loading effects on the sample. On the lowest current source ranges (1pA and 10pA) of the Model 4200-SCS, the input resistance of the voltmeter is>$10^{16}\Omega$.

Using the Model 4200-SCS to Measure Resistivity with the van der Pauw Method

Each terminal of the sample is connected to one SMU instrument, so a Model 4200-SCS with four SMU instruments is required. A test project with four ITMs (Interactive Test Modules) is written using a generic or custom-designed four-terminal device. Each ITM is a different measurement setup. An example of how the four SMU instruments are configured in the four ITMs is shown in ***Figure 6***. For each ITM, three of the SMU instruments are configured as a current bias and a voltmeter (VMU). One of these SMU instruments applies the test current and the other two SMU instruments are used as high impedance voltmeters with a test current of zero amps on a low current range (typically 1nA range). The fourth SMU instrument is set to common. The voltage difference must be calculated between the two SMU instruments set up as high impedance voltmeters. This measurement setup is duplicated around the sample, with each of the four SMU instruments changing functions in each of the four ITMs.

Basic Procedure for Setting up a New Project for Measuring van der Pauw Resistivity:

1. Create a new project.
2. Create a new sub-site plan.
3. Add a new device plan. It must be either a generic or custom-designed four-terminal device.
4. Four ITMs will need to be created. In each ITM, one SMU instrument will be configured as the current source using the current list sweep function, two SMU instruments will be configured as voltmeters, and one will be configured as a common. Here is an example setup for a high resistance sample:

   Terminal A – SMU1: Set to a two-point Current List Sweep. Enter both the positive and negative values of the appropriate source current. Enter the Compliance level and use the Best Fixed source range. Averaging voltage measurements (from SMU2 and SMU3) taken at both a positive and negative test current will correct for voltage offsets in the circuit.

   Terminal B – SMU2: Set to Current Bias (VMU) with a test current of 0A. Set the appropriate compliance voltage, and check the Measure Voltage box (VB). Even though 0A will be output, select an appropriate current source range. The input impedance of the voltmeter is directly related to the current source range. The lower the current source range is, the higher the input impedance will be. However, the lower the current source range, the slower the measurement time will be. For most applications, the 1nA range may be used. However, for very high resistance measurements, use a lower current range.

   Terminal C – SMU3: Set up the same as Terminal B.

   Terminal D – SMU4: Set the Forcing Function to Common.

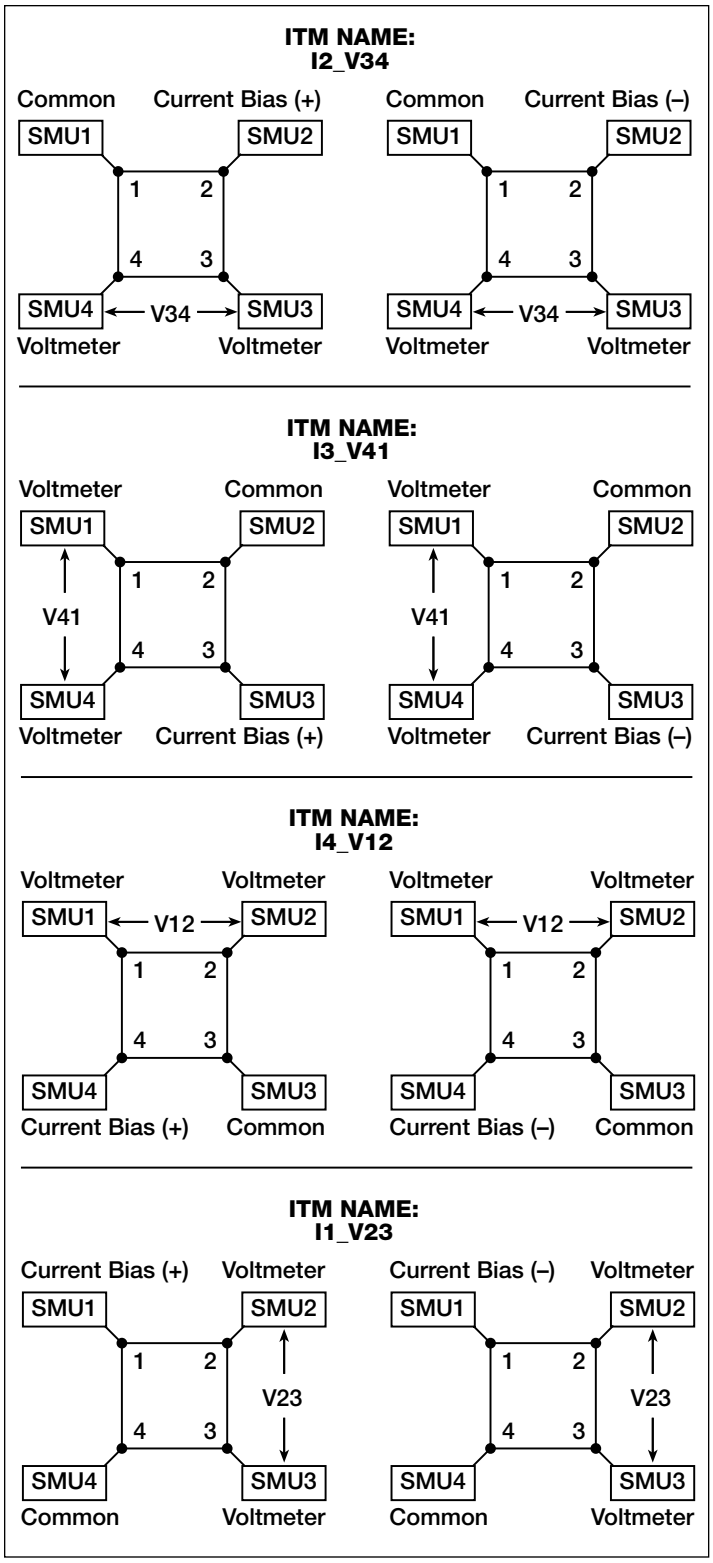


Figure 6. SMU Instrument Configurations for van der Pauw Measurements

In this example, the current will be sourced between Terminals A and D (SMU1 to SMU4). SMU2 will measure the voltage from Terminal B to Terminal D. SMU3 will measure the voltage from Terminal C to Terminal D.

Use the Formulator to calculate the voltage difference between SMU2 and SMU3 for both the positive and

negative test current. This can be done using an equation such as V23DIFF=VB-VC. Take the absolute values of these numbers (from both the positive and negative test current) using the ABS function with an equation such as V23ABS=ABS(V23DIFF). Then average the two voltage difference values using the AVG function with an equation, such as V23=AVG(ABSV23). In the Output Values window, check the average voltage (V23) so that it is sent to the sub-site data sheet, where it will be used in the resistivity calculation. The magnitude of the current source must also be sent to the sub-site data sheet, so click that check box (I1) as well.

Using four ITMs, this same procedure will need to be repeated around all sides of the sample as shown previously in ***Figure 4***. The average voltages from each ITM are then used to calculate the resistivity on the sub-site Calc sheet. A diagram showing how the SMUs are setup in each ITM is shown in ***Figure 6***.

5. To calculate the resistivity in the sub-site level, open up the sub-site plan. In the Subsite Setup tab, select Cycle Mode and enter "1" in the Number of Cycles field. The Output Values (voltage differences and test current) will appear on the data sheet at the sub-site level. The resistivity is calculated on the Calc sheet from the cell references on the Data sheet. The thickness, coefficients, and correction factors are also input on the Calc sheet for the resistivity equation.

Example van der Pauw Application Using the Model 4200-SCS

An example van der Pauw resistivity project, ***vdp_resistivity***, has been created for KITE 5.0 or higher versions. This project follows the example listed previously. A window of this project is shown in ***Figure 7***.

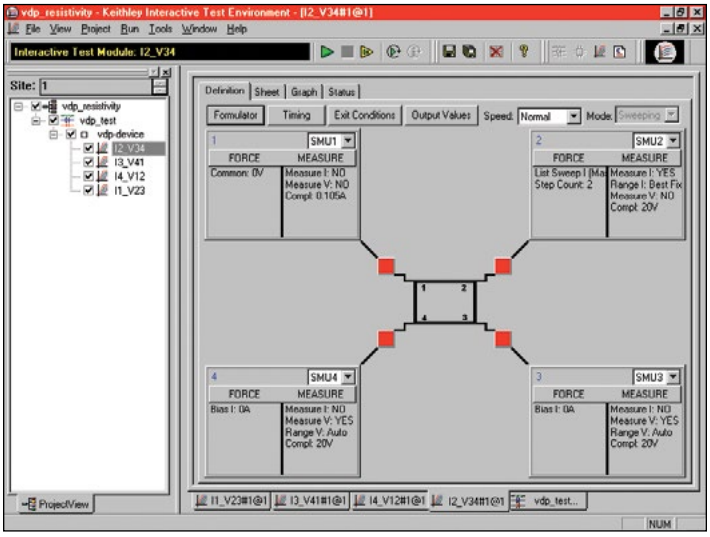


Figure 7. Screen Capture of van der Pauw Resistivity Application on Model 4200-SCS

This project has been written following the procedure previously described in this application note. Notice that a van der Pauw device structure is shown in the definition window. The user will need to adjust the source current, the thickness of the material, and the settling time of the measurement.

Adjusting the Source Current

The source current value will need to be modified according to the expected sample resistance. Adjust the current so that the voltage difference will not exceed 25mV (approximately). In each of the four ITMs (I2_V34, I3_V41, I4_V12, I1_V23), enter both polarities of the test current. The same magnitude must be used for each ITM.

Determining the Settling Time

For high resistance samples, it will be necessary to determine the settling time of the measurement. This can be accomplished by sourcing current into two terminals of the sample and measuring the voltage difference between the other two terminals. The settling time can be determined by graphing the voltage difference versus the time of the measurement.

Using the Model 4200-SCS, the voltage versus time graph can be easily created by modifying one of the ITMs described previously. In the Timing menu, take a few hundred or so readings with a sweep time of one second. Make sure that the Timestamp Enabled box is checked. After the readings are done, plot the voltage difference versus time on the graph. (You can choose the parameters to graph by right-clicking on the graph). The settling time is determined from the graph. A timing graph of a very high resistance material is shown in ***Figure 8***.

Determine the settling time by visually inspecting the voltage difference vs. time graph. Once the settling time has been determined, use this time as the Sweep Delay (in the Timing menu) for the four resistivity measurement ITMs listed previously. This settling time procedure will need to be repeated for different materials; however, it is not necessary for low resistance materials since they have a short settling time.

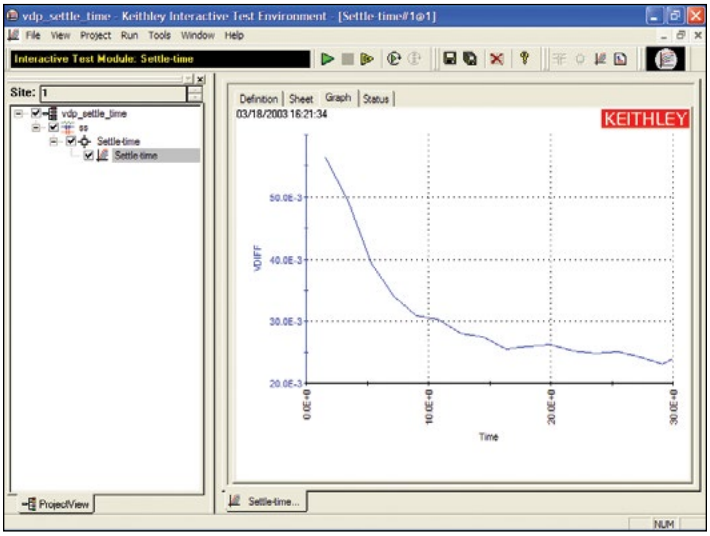


Figure 8. Voltage vs. Time Graph of Very High Resistance Sample

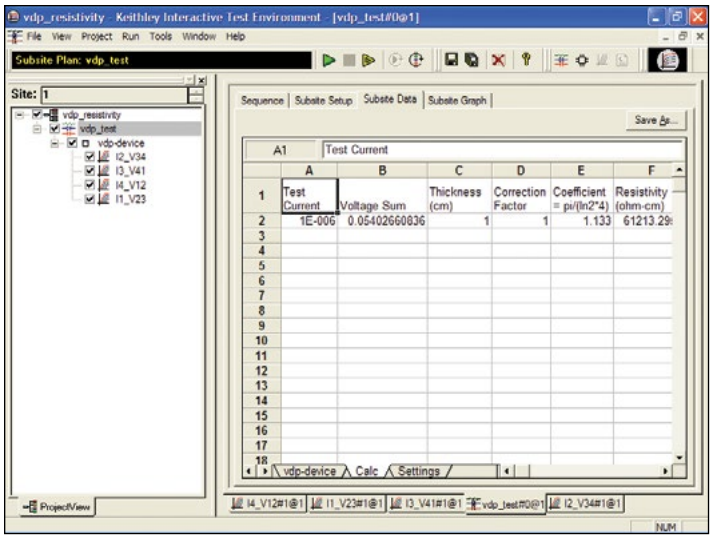


Figure 9. Subsite Data "Calc" Sheet with Resistivity Displayed

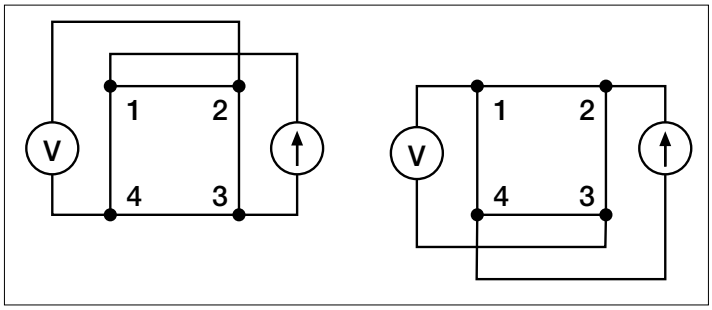


Figure 10. Hall Voltage Measurement Configurations

Inputting the Thickness of the Sample

The thickness of the material will also need to be entered into the Calc sheet in the sub-site level. Select the sub-site "vdp-test." Go to the Subsite Data tab. It contains the output values of the voltage differences and the test current. From the Calc Sheet tab, the thickness can be adjusted. The default thickness is 1cm. If necessary, a correction factor can also be applied to the resistivity equation.

Running the Project

The "vdp_resistivity" project must be run at the "vdp-test" sub-site level. Make sure that all boxes in the Project/View are checked and highlight "vdp-test." Execute the project by using the sub-site run button (circular arrow). Each time the test is run, the subsite data is updated. The voltage differences from each of the four ITMs (I2_V34, I3_V41, I4_V12, I1_V23) will appear in the Subsite Data "vdp-device" sheet. The resistivity will appear in the Subsite Data "Calc" sheet as shown in ***Figure 9***.

Hall Voltage Measurements

Hall effect measurements are important to semiconductor material characterization because from the Hall voltage, the conductivity type, carrier density, and mobility can be derived. With an applied magnetic field, the Hall voltage can be measured using the configurations shown in ***Figure 10***.

With a positive magnetic field, B, apply a current between terminals 1 and 3, and measure the voltage drop (V_{2-4+}) between terminals 2 and 4. Reverse the current and measure the voltage drop (V_{4-2+}). Next, apply current between terminals 2 and 4, and measure the voltage drop (V_{1-3+}) between terminals 1 and 3. Reverse the current and measure the voltage (V_{3-1+}) again.

Reverse the magnetic field, B, and repeat the procedure again, measuring the four voltages: (V_{2-4-}), (V_{4-2-}), (V_{1-3-}), and (V_{3-1-}).

From the eight Hall voltage measurements, the average Hall coefficient can be calculated as follows:

$$R_{HC} = \frac{t_s(V_{4-2+} - V_{2-4+} + V_{2-4-} - V_{4-2-})}{4BI}$$

$$R_{HD} = \frac{t_s(V_{3-1+} - V_{1-3+} + V_{1-3-} - V_{3-1-})}{4BI}$$

where: R_{HC} and R_{HD} are Hall coefficients in cm^3/C;

t_s is the sample thickness in cm;

V represents the voltages measured by the voltmeter;

I is the current through the sample in amperes;

B is the magnetic flux in Vs/cm^2 ($1\ Vs/cm^2 = 10^8$ gauss)

Once R_{HC} and R_{HD} have been calculated, the average Hall coefficient (R_{HAVG}) can be determined as follows:

$$R_{HAVG} = \frac{R_{HC} + R_{HD}}{2}$$

From the resistivity (ρ_{AVG}) and the Hall coefficient (R_{HAVG}), the mobility (μ_H) can be calculated:

$$\mu_H = \frac{|R_H|}{\rho_{AVG}}$$

Using the Model 4200-SCS to Measure the Hall Voltage

The setup to measure the Hall voltage is very similar to the setup for measuring resistivity. The difference is the location of the current source and voltmeter terminals. ***Figure 10*** illustrates the setup for Hall voltage measurements. (***Figure 4*** illustrates the setup for resistivity measurements.) If the user-supplied electromagnet has an IEEE-488 interface, a program can be written in KULT (Keithley User Library Tool) to control the electromagnet using the Model 4200-SCS.

Sources of Error and Measurement Considerations

For successful resistivity measurements, the potential sources of errors need to be considered.

Electrostatic Interference

Electrostatic interference occurs when an electrically charged object is brought near an uncharged object. Usually, the effects of the interference are not noticeable because the charge dissipates rapidly at low resistance levels. However, high resistance

materials do not allow the charge to decay quickly and unstable measurements may result. The erroneous readings may be due to either DC or AC electrostatic fields.

To minimize the effects of these fields, an electrostatic shield can be built to enclose the sensitive circuitry. The shield is made from a conductive material and is always connected to the low impedance (FORCE LO) terminal of the SMU instrument.

The cabling in the circuit must also be shielded. Low noise shielded triax cables are supplied with the Model 4200-SCS.

Leakage Current

For high resistance samples, leakage current may degrade measurements. The leakage current is due to the insulation resistance of the cables, probes, and test fixturing. Leakage current may be minimized by using good quality insulators, by reducing humidity, and by using guarding.

A guard is a conductor connected to a low impedance point in the circuit that is nearly at the same potential as the high impedance lead being guarded. The inner shield of the triax connector of the Model 4200-SCS is the guard terminal. This guard should be run from the Model 4200-SCS to as close as possible to the sample. Using triax cabling and fixturing will ensure that the high impedance terminal of the sample is guarded. The guard connection will also reduce measurement time since the cable capacitance will no longer affect the time constant of the measurement.

Light

Currents generated by photoconductive effects can degrade measurements, especially on high resistance samples. To prevent this, the sample should be placed in a dark chamber.

Temperature

Thermoelectric voltages may also affect measurement accuracy. Temperature gradients may result if the sample temperature is not uniform. Thermoelectric voltages may also be generated from sample heating caused by the source current. Heating from the source current will more likely affect low resistance samples, since a higher test current is needed to make the voltage measurements easier. Temperature fluctuations in the laboratory environment may also affect measurements. Since semiconductors have a relatively large temperature coefficient, temperature variations in the laboratory may need to be compensated for by using correction factors.

Carrier Injection

To prevent minority/majority carrier injection from influencing resistivity measurements, the voltage difference between the two voltage sensing terminals should be kept at less than 100mV, ideally 25mV, since the thermal voltage, kt/q, is approximately 26mV. The test current should be kept to as low as possible without affecting the measurement precision.

Alternative Solution

For characterizing low resistance materials, it may be necessary to use a configuration including a programmable current source (such as the Keithley Model 2450), programmable switch matrix (such as the Keithley Model 7001/7012), and the Keithley Model 2182A Nanovoltmeter. The Model 2182A can detect nanovolt-level voltage differences with just 30nV p-p noise (typical).

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Electrical Characterization of Photovoltaic Materials and Solar Cells with the Model 4200-SCS Parameter Analyzer

I-V, C-V, C-f, DLCP, Pulsed I-V, Resistivity, and Hall Voltage Measurements

Introduction

The increasing demand for clean energy and the largely untapped potential of the sun as an energy source is making solar energy conversion technology increasingly important. As a result, the demand for solar cells, which convert sunlight directly into electricity, is growing. Solar or photovoltaic (PV) cells are made up of semiconductor materials that absorb photons from sunlight and then release electrons, causing an electric current to flow when the cell is connected to a load. A variety of measurements are used to characterize a solar cell's performance, including its output and its efficiency. This electrical characterization is performed as part of research and development of photovoltaic cells and materials, as well as during the manufacturing process.

Some of the electrical tests commonly performed on solar cells involve measuring current and capacitance as a function of an applied DC voltage. Capacitance measurements are sometimes made as a function of frequency or AC voltage. Some tests require pulsed current-voltage measurements. These measurements are usually performed at different light intensities and under different temperature conditions. A variety of important device parameters can be extracted from the DC and pulsed current-voltage (I-V) and capacitance-voltage (C-V) measurements, including output current, conversion efficiency, maximum power output, doping density, resistivity, etc. Electrical characterization is important in determining how to make the cells as efficient as possible with minimal losses.

Instrumentation such as the Model 4200-SCS Parameter Analyzer can simplify testing and analysis when making these critical electrical measurements. The Model 4200-SCS is an integrated system that includes instruments for making DC and ultra fast I-V and C-V measurements, as well as control software, graphics, and mathematical analysis capability. The Model 4200-SCS is well-suited for performing a wide range of measurements, including DC and pulsed current-voltage (I-V), capacitance-voltage (C-V), capacitance-frequency (C-f), drive level capacitance profiling (DLCP), four-probe resistivity (ρ, σ), and Hall voltage (V_H) measurements. This application note describes how to use the Model 4200-SCS to make these electrical measurements on PV cells.

Making Electrical Measurements with the Model 4200-SCS

To simplify testing photovoltaic materials and cells, the Model 4200-SCS is supported with a test project for making many of the mostly commonly used measurements easily. These tests, which include I-V, capacitance, and resistivity measurements, also include formulas for extracting common parameters such as the maximum power, short circuit current, defect density, etc. The *SolarCell* project (***Figure 1***) is included with all Model 4200-SCS systems running KTEI Version 8.0 or later. It provides thirteen tests (***Table 1***) in the form of ITMs (Interactive Test Modules) and UTMs (User Test Modules) for electrical characterization.

Table 1. Test modules in the SolarCell project

Subsite Level	Test Module	Description
IV_sweep	fwd-ivsweep	Performs I-V sweep and calculates I_{sc}, V_{oc}, P_{max}, I_{max}, V_{max}, FF
	rev-ivsweep	Performs reversed bias I-V sweep
CV_sweep	cvsweep	Generates C-V sweep
	C-2vsV	Generates C-V sweep and calculates $1/C^2$
	cfsweep	Sweeps the frequency and measures capacitance
	DLCP	Measures capacitance as AC voltage is swept. DC voltage is applied so as to keep the total applied voltage constant. The defect density is calculated.
Pulse-IV	pulse-iv-sweep	Performs pulse I-V sweep using one channel of PMU
4PtProbe_resistivity	HiR	Uses 3 or 4 SMUs to source current and measure voltage difference for high resistance semiconductor materials. Calculates sheet resistivity.
	LoR	Uses 1 or 2 SMUs to source current and measure voltage using remote sense. Calculates sheet resistivity. Uses current reversal method to compensate for thermoelectric voltage offsets.
vdp_resistivity	I1_V23	First of 4 ITMs that are used to measure the van der Pauw resistivity. This ITM sources current between terminals 1 and 4 and measures the voltage difference between terminals 2 and 3.
	I2_V34	Sources current between terminals 2 and 1 and measures the voltage difference between terminals 3 and 4.
	I3_V41	Sources current between terminals 3 and 2 and measures the voltage difference between terminals 4 and 1.
	I4_V12	Sources current between terminals 4 and 1 and measures the voltage difference between terminals 1 and 2.

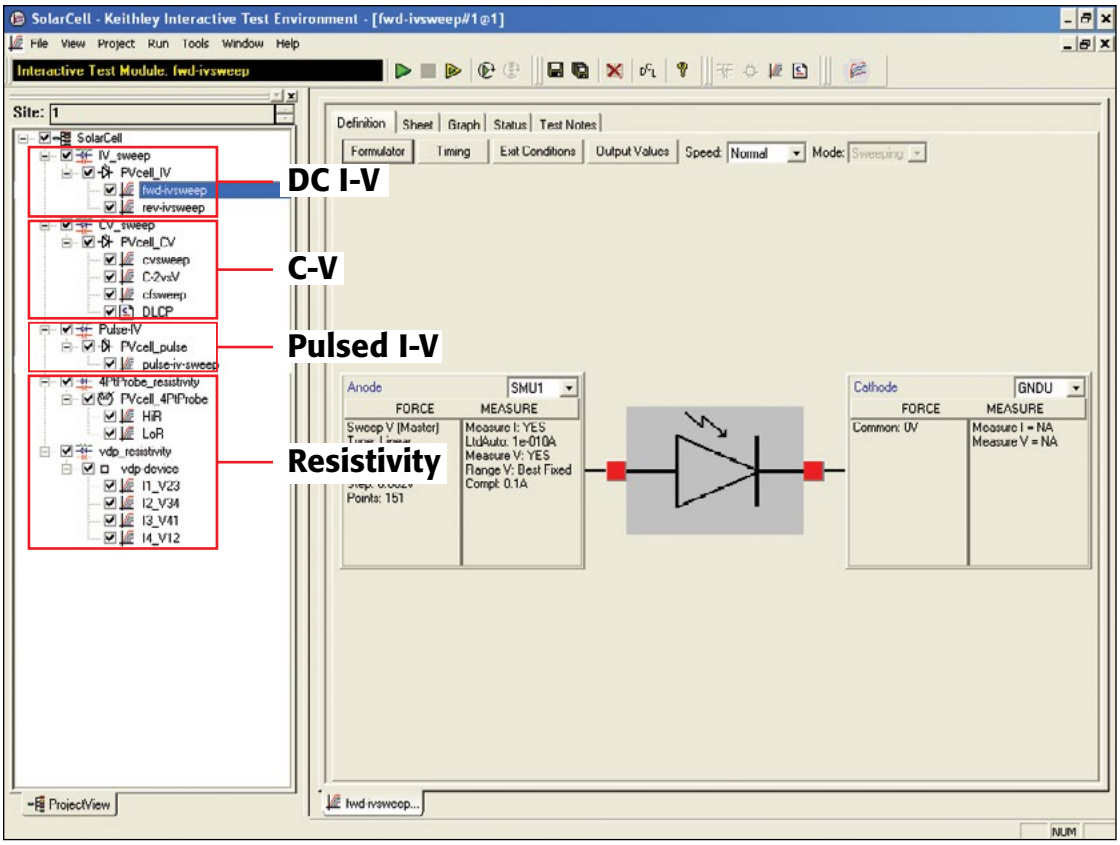

Figure 1. Screenshot of *SolarCell* project for the Model 4200-SCS

DC Current-Voltage (I-V) Measurements

As described previously, many solar cell parameters can be derived from current-voltage (I-V) measurements of the cell. These I-V characteristics can be measured using the Model 4200-SCS's source measure units (SMU) instruments, which can source and measure both current and voltage. Because these SMU instruments have four-quadrant source capability, they can sink the cell current as a function of the applied voltage. Two types of SMU instruments are available for the Model 4200-SCS: the Model 4200-SMU, which can source/sink up to 100mA, and the Model 4210-SMU, which can source/sink up to 1A. If the output current of the cell exceeds these current levels, it may be necessary to reduce it, possibly by reducing the area of the cell itself. However, if this is not possible, Keithley's Series 2400 or 2600B SourceMeter® SMU Instruments, which are capable of sourcing/sinking higher currents, offer possible alternative solutions.

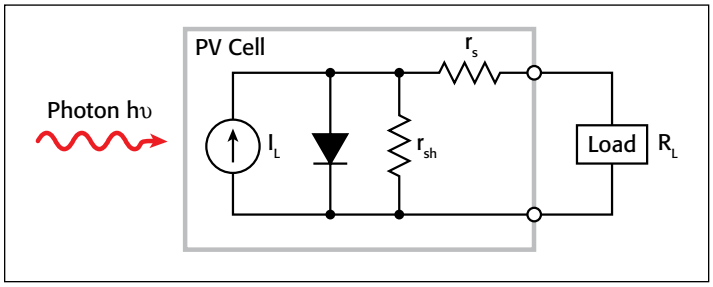

Figure 2. Idealized equivalent circuit of a photovoltaic cell

Parameters Derived from I-V Measurements

A solar cell may be represented by the equivalent circuit model shown in ***Figure 2***, which consists of a light-induced current source (I_L), a diode that generates a saturation current [$I_S(e^{qV/kT} - 1)$], series resistance (r_s), and shunt resistance (r_{sh}). The series resistance is due to the resistance of the metal contacts, ohmic losses in the front surface of the cell, impurity concentrations, and junction depth. The series resistance is an important parameter because it reduces both the cell's short-circuit current and its maximum power output. Ideally, the series resistance should be 0Ω ($r_s = 0$). The shunt resistance represents the loss due to surface leakage along the edge of the cell or to crystal defects. Ideally, the shunt resistance should be infinite ($r_{sh} = \infty$).

If a load resistor (R_L) is connected to an illuminated solar cell, then the total current becomes:

$$I = I_S(e^{qV/kT} - 1) - I_L$$

where:
I_S = current due to diode saturation
I_L = current due to optical generation

Several parameters are used to characterize the efficiency of the solar cell, including the maximum power point (P_{max}), the energy conversion efficiency (η), and the fill factor (FF). These points are illustrated in ***Figure 3***, which shows a typical forward bias I-V curve of an illuminated PV cell. The maximum power point (P_{max}) is the product of the maximum cell current (I_{max})

and the voltage (V_{max}) where the power output of the cell is greatest. This point is located at the "knee" of the curve.

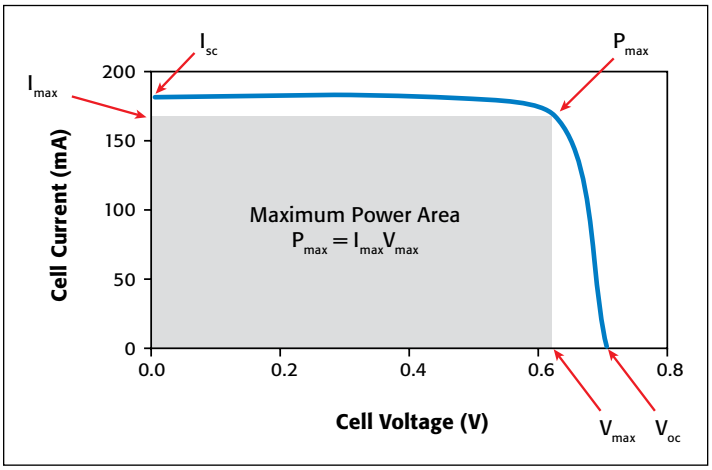

Figure 3. Typical forward bias I-V characteristics of a PV cell

The fill factor (FF) is a measure of how far the I-V characteristics of an actual PV cell differ from those of an ideal cell. The fill factor is defined as:

$$FF = \frac{I_{max}V_{max}}{I_{sc}V_{oc}}$$

where:

I_{max} = the current at the maximum power output (A)
V_{max} = the voltage at the maximum power output (V)
I_{sc} = the short-circuit current (A)
V_{oc} = the open-circuit voltage (V)

As defined, the fill factor is the ratio of the maximum power ($P_{max} = I_{max}V_{max}$) to the product of the short circuit current (I_{sc}) and the open circuit voltage (V_{oc}). The ideal solar cell has a fill factor equal to one (1) but losses from series and shunt resistance decrease the efficiency.

Another important parameter is the conversion efficiency (η), which is defined as the ratio of the maximum power output to the power input to the cell:

$$\eta = \frac{P_{max}}{P_{in}}$$

where:

P_{max} = the maximum power output (W)
P_{in} = the power input to the cell defined as the total radiant energy incident on the surface of the cell (W)

Making Connections to the Solar Cell for I-V Measurements

Figure 4 illustrates a solar cell connected to the Model 4200-SCS for I-V measurements. One side of the solar cell is connected to the Force and Sense terminals of SMU1; the other side is connected to the Force and Sense terminals of either SMU2 or the ground unit (GNDU) as shown.

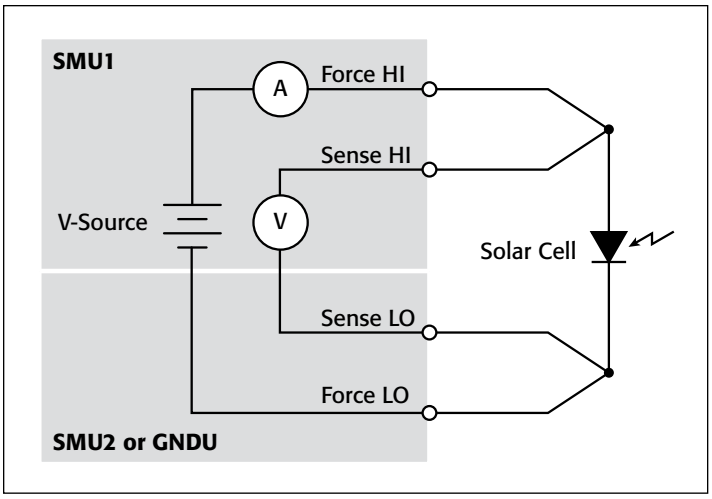

Figure 4. Connection of Model 4200-SCS to a solar cell for I-V measurements

Using a four-wire connection eliminates the lead resistance that would otherwise affect this measurement's accuracy. With the four-wire method, a voltage is sourced across the solar cell using one pair of test leads (between Force HI and Force LO), and the voltage drop across the cell is measured across a second set of leads (across Sense HI and Sense LO). The sense leads ensure that the voltage developed across the cell is the programmed output value and compensate for the lead resistance.

Forward-Biased I-V Measurements

Forward-biased I-V measurements of the solar cell are made under controlled illumination. The SMU instrument is set up to output a voltage sweep and measure the resulting current. This forward bias sweep can be performed using the "*fwd-ivsweep*" ITM, which allows adjusting the sweep voltage to the desired values. As previously illustrated in ***Figure 3***, the voltage source is swept from $V_1 = 0$ to $V_2 = VOC$. When the voltage source is 0 ($V_1 = 0$), the current is equal to the source-circuit current ($I_1 = I_{SC}$). When the voltage source is an open circuit ($V_2 = V_{OC}$), then the current is equal to zero ($I_2 = 0$). The parameters, V_{OC} and I_{SC}, can easily be derived from the sweep data using the Model 4200-SCS's built-in mathematical analysis tool, the Formulator. For convenience, the *SolarCell* project has the commonly derived parameters already calculated, so the values automatically appear in the Sheet tab every time the test is executed. ***Figure 5*** shows some of the derived parameters in the Sheet tab. These parameters include the short-circuit current (I_{SC}), the open circuit voltage (V_{OC}), the maximum power point (P_{max}), the maximum cell current (I_{max}), the maximum cell voltage (V_{max}), and the fill factor (FF).

Th user can easily add other formulas depending on the required parameters that need to be determined.

Using the Formulator, the conversion efficiency (η) can also be calculated if the user knows the power input to the cell and inputs the formula. The current density (J) can also be derived by using the Formulator and inputting the area of the cell.

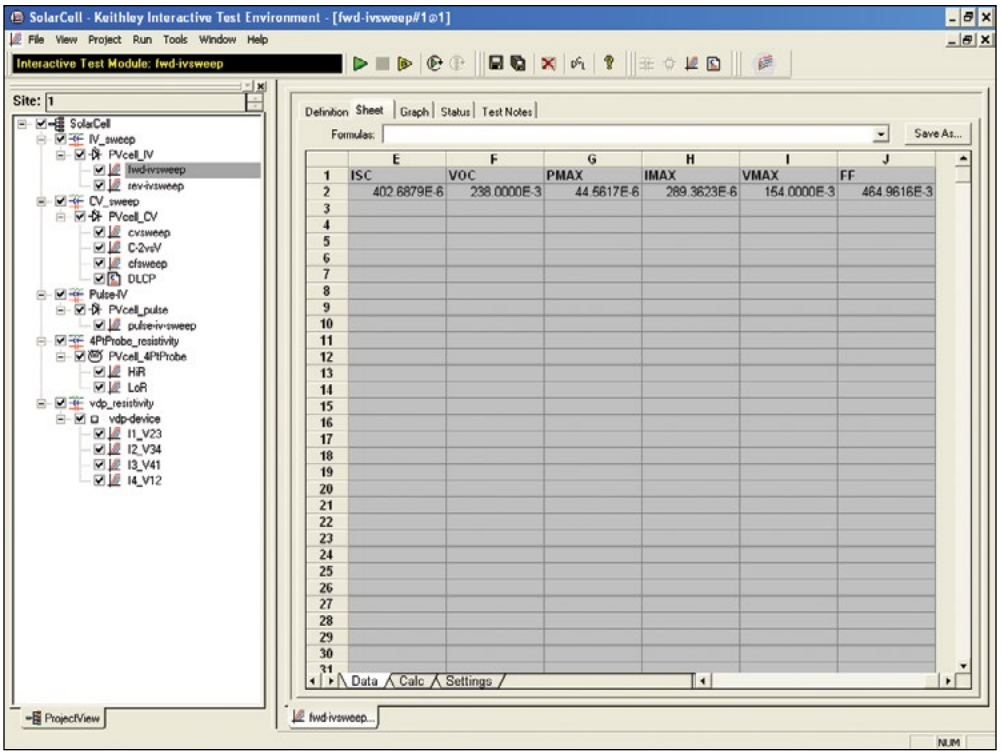

Figure 5. Results of calculated parameters shown in Sheet tab

Figure 6 shows an actual I-V sweep of an illuminated silicon PV cell generated with the Model 4200-SCS using the "*fwd-ivsweep*" ITM. Because the system's SMU instruments can sink current, the curve passes through the fourth quadrant and allows power to be extracted from the device (I–, V+). If the current output spans several decades as a function of the applied voltage, it may be desirable to generate a semilog plot of I vs. V. The Graph tab options support an easy transition between displaying data graphically on either a linear or a log scale.

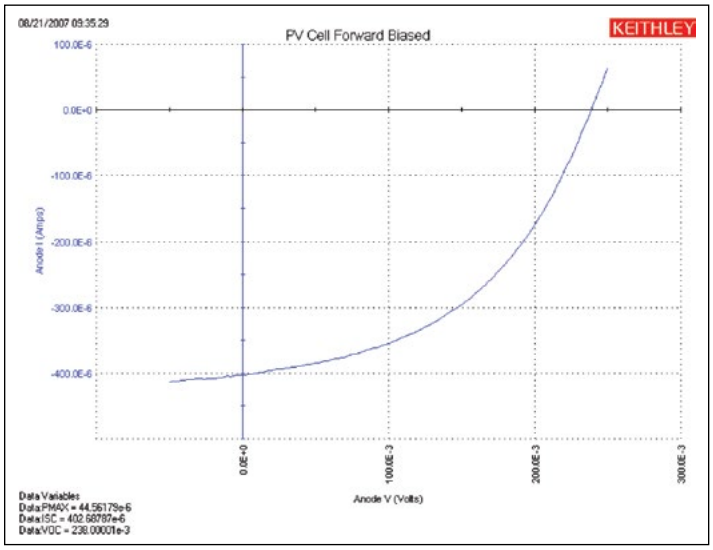

Figure 6. I-V sweep of silicon PV cell generated with the 4200-SMU

If desired, the graph settings functions make it easy to create an inverted version of the graph about the voltage axis. Simply go to the Graph Settings tab, select Axis Properties, select the Y1 Axis tab, and click on the Invert checkbox. The inverse of the graph will appear as shown in ***Figure 7***.

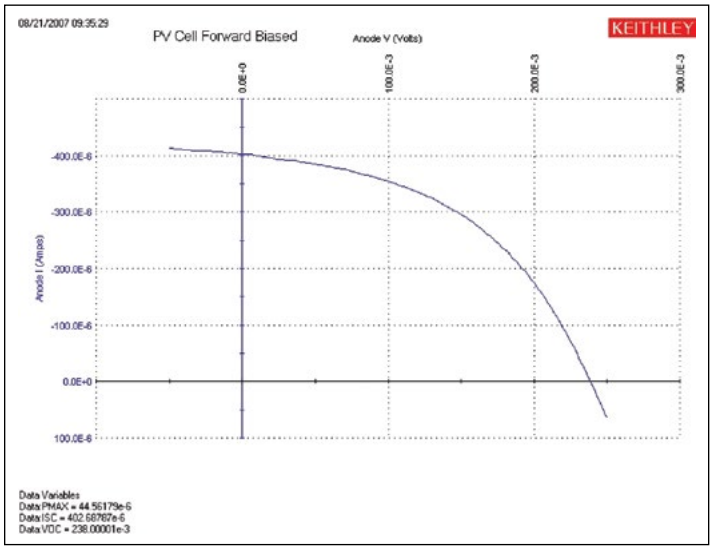

Figure 7. Inversion of the forward-biased I-V curve about the voltage axis

The series resistance (r_s) can be determined from the forward I-V sweep at two or more light intensities. First, make I-V curves at two different intensities (the magnitudes of the intensities are not important). Measure the slope of this curve from the far forward characteristics where the curve becomes linear. The inverse of this slope yields the series resistance:

$$r_s = \frac{\Delta V}{\Delta I}$$

By using additional light intensities, this technique can be extended using multiple points located near the knee of the curves. As illustrated in ***Figure 8***, a line is generated from which the series resistance can be calculated from the slope.

When considered as ammeters, one important feature of the Model 4200-SCS's SMU instruments is their very low voltage burden. The voltage burden is the voltage drop across the ammeter during the measurement. Most conventional digital multimeters (DMMs) will have a voltage burden of at least 200mV at full scale. Given that only millivolts may be sourced to the sample in solar cell testing, this can cause large errors. The Model 4200-SCS's SMU instruments don't produce more than a few hundred microvolts of voltage burden, or voltage drop, in the measurement circuit.

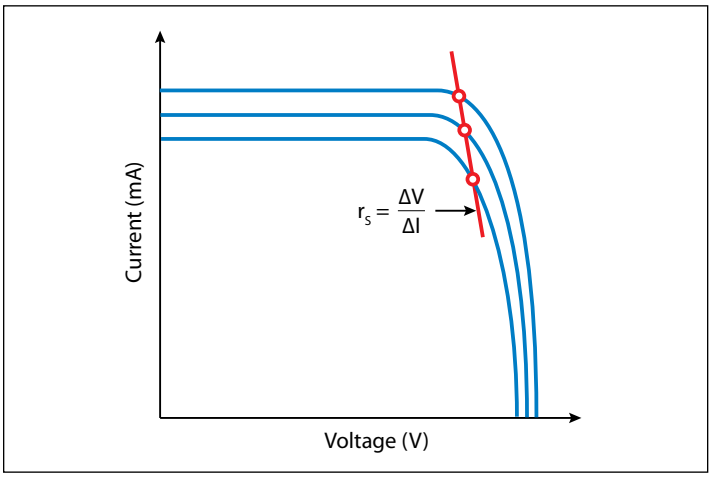

Figure 8. Slope method used to calculate the series resistance

Reverse-Biased I-V Measurements

The leakage current and shunt resistance (r_{sh}) can be derived from the reverse-biased I-V data. Typically, the test is performed in the dark. The voltage is sourced from 0V to a voltage level where the device begins to break down. The resulting current is measured and plotted as a function of the voltage. Depending on the size of the cell, the leakage current can be as small as picoamps. The Model 4200-SCS has a preamp option that allows making accurate measurements well below a picoamp. When making very sensitive low current measurements (nanoamps or less), use low noise cables and place the device in a shielded enclosure to shield it electrostatically. This conductive shield is connected to the Force LO terminal of the Model 4200-SCS. The Force LO terminal connection can be made from the outside shell of the triax connectors, the black binding post on the ground unit (GNDU), or from the Force LO triax connector on the GNDU.

One method for determining the shunt resistance of the PV cell is from the slope of the reverse-biased I-V curve, as shown in ***Figure 9***. From the linear region of this curve, the shunt resistance can be calculated as:

$$r_{sh} = \frac{\Delta V_{Reverse\ Bias}}{\Delta I_{Reverse\ Bias}}$$

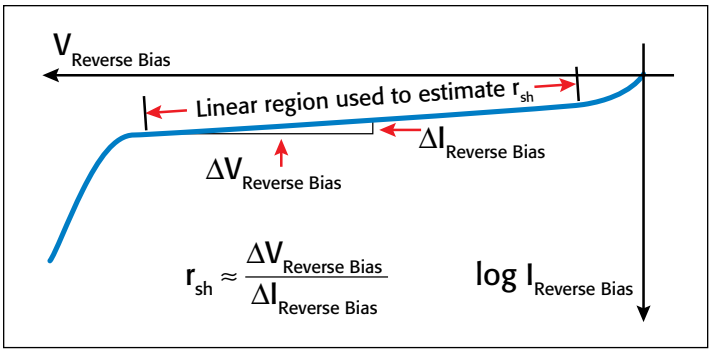

Figure 9. Typical reverse-biased characteristics of a PV cell

Figure 10 shows an actual curve of a reverse-biased solar cell, generated using the ITM "*rev-ivsweep*". In this semi-log graph, the absolute value of the current is plotted as a function of the reverse-biased voltage that is on an inverted x-axis.

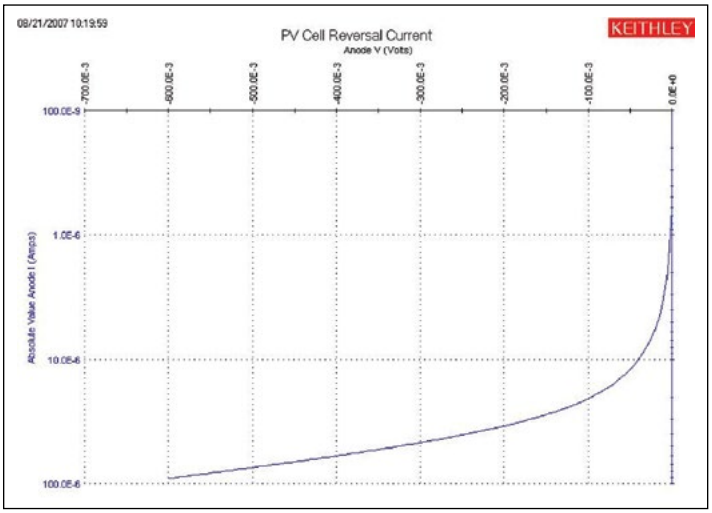

Figure 10. Reverse-biased I-V measurement of silicon solar cell using the Model 4200-SMU

Capacitance Measurements

Capacitance-voltage measurements are useful in deriving particular parameters about PV devices. Depending on the type of solar cell, capacitance-voltage (C-V) measurements can be used to derive parameters such as the doping concentration and the built-in voltage of the junction. A capacitance-frequency (C-f) sweep can be used to provide information on the existence of traps in the depletion region. The Model 4210-CVU, the Model 4200-SCS's optional capacitance meter, can measure the capacitance as a function of an applied DC voltage (C-V), a function of frequency (C-f), a function of time (C-t), or a function of the AC voltage. The Model 4210-CVU can also measure conductance and impedance.

To make capacitance measurements, a solar cell is connected to the Model 4210-CVU as shown in ***Figure 11***. Like I-V measurements made with the SMU instrument, the capacitance measurements also involve a four-wire connection to compensate for lead resistance. The HPOT/HCUR terminals are connected to

the anode and the LPOT/LCUR terminals are connected to the cathode. This connects the high DC voltage source terminal of the Model 4210-CVU to the anode.

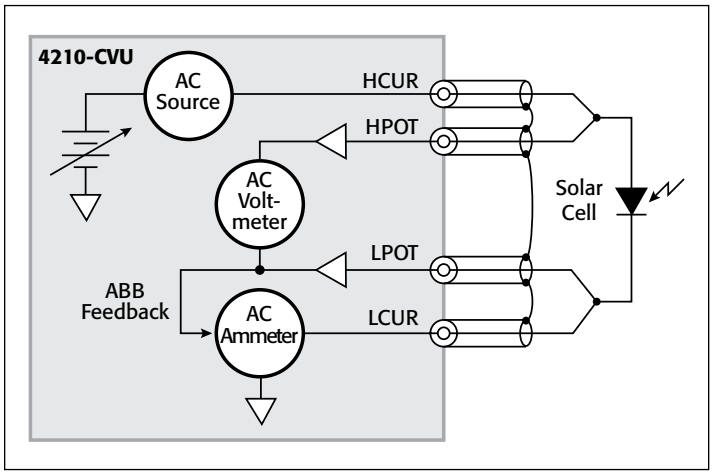

Figure 11. Connecting the solar cell to the Model 4210-CVU capacitance meter

Figure 11 shows the shields of the four coax cables coming from the four terminals of the capacitance meter. The shields from the coax cables must be connected together as close as possible to the solar cell to obtain the highest accuracy because this reduces the effects of the inductance in the measure circuit. This is especially important for capacitance measurements made at higher test frequencies.

Performing an Open and Short Connection Compensation will reduce the effects of cable capacitance on measurement accuracy. This simple procedure is described in Section 15 of the Model 4200-SCS Reference Manual.

Given that the capacitance of the cell is directly related to the area of the device, it may be necessary to reduce the area of the cell itself, if possible, to avoid capacitances that may be too high to measure. Also, setting the Model 4210-CVU to measure capacitance at a lower test frequency and/or lower AC drive voltage will allow measuring higher capacitances.

C-V Sweep

C-V measurements can be made either forward-biased or reverse-biased. However, when the cell is forward-biased, the applied DC voltage must be limited; otherwise, the conductance may get too high for the capacitance meter to measure. The maximum DC current cannot be greater than 10mA; otherwise, the instrument's DC voltage source will go into compliance and the DC voltage output will not be at the desired level.

Figure 12 illustrates a C-V curve of a silicon solar cell generated by the Model 4210-CVU using the "*cvsweep*" ITM. This test was performed in the dark while the cell was reversed-biased.

Rather than plotting dC/dV, it is sometimes desirable to view the data as $1/C^2$ vs. voltage because some parameters are related to the $1/C^2$ data. For example, the doping density (N) can be

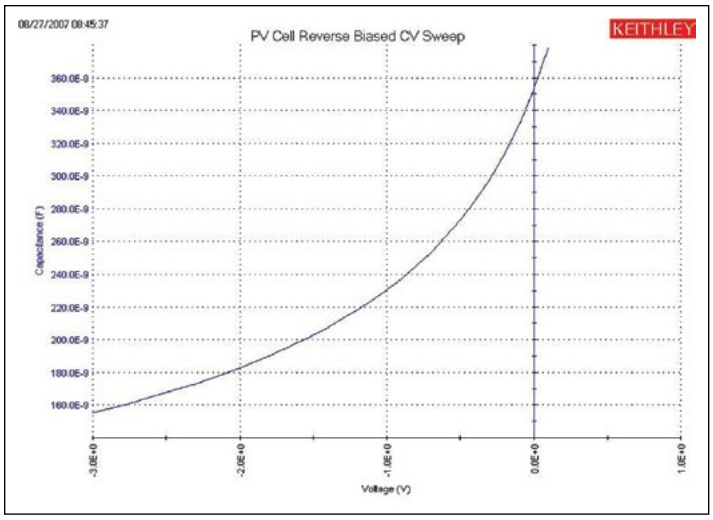

Figure 12. C-V sweep of a silicon solar cell

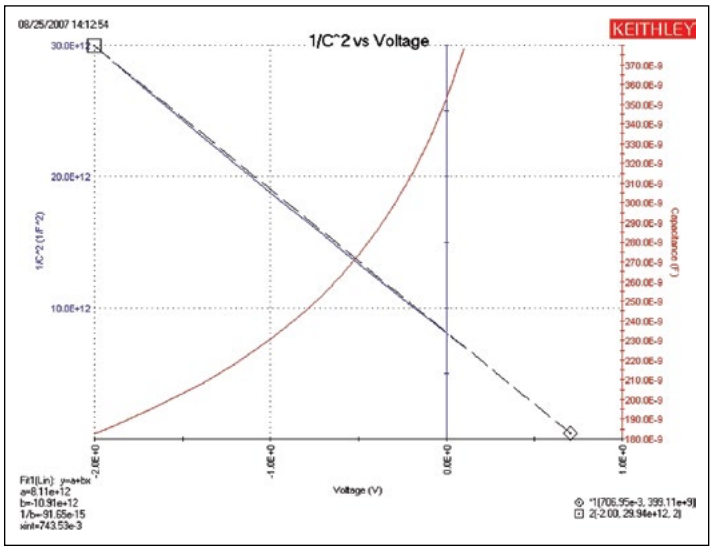

Figure 13. $1/C^2$ vs. voltage of a silicon solar cell

derived from the slope of this curve because N is related to the capacitance by:

$$N(a) = \frac{2}{qE_S A^2 [d(1/C^2)/dV]}$$

where:

N(a) = the doping density ($1/cm^3$)
q = the electron charge (1.60219×10^{-19}C)
E_s = semiconductor permittivity (1.034×10^{-12}F/cm for silicon)
A = area (cm^2)
C = measured capacitance (F)
V = applied DC voltage (V)

The built-in voltage of the cell junction can be derived from the intersection of the $1/C^2$ curve and the horizontal axis. This plot should be a fairly straight line. An actual curve taken with the Model 4210-CVU, generated using the "*C-2vsV*" ITM, is shown in ***Figure 13***. The Formulator function is used to derive both the doping density (N) and the built-in voltage on the x-axis (x-intercept). The doping density is calculated as a function of

voltage in the Formulator and appears in the Sheet tab in the ITM. The user must input the area of the cell in the Constants area of the Formulator. The built-in voltage source value is derived both in the Formulator and by using a Linear Line Fit option in the Graph settings. Notice the value of the x-intercept appears in the lower left corner of the graph.

C-f Sweep

The Model 4210-CVU option can also measure capacitance, conductance, or impedance as a function of the test frequency. The range of frequency is from 1kHz to 10MHz. The curve in ***Figure 14*** was generated by using the "*cfsweep*" ITM. Both the range of sweep frequency and the bias voltage can be adjusted. The desired parameters, such as the trap densities, can be extracted from the capacitance vs. frequency data. The measurements can be repeated at various temperatures.

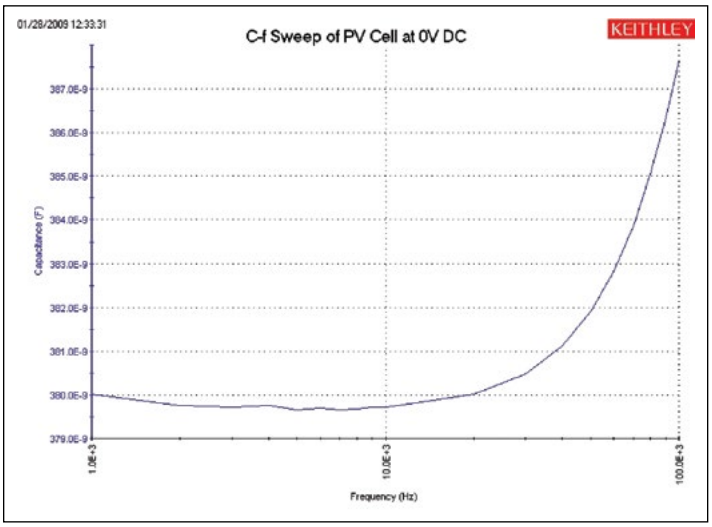

Figure 14. C-f Sweep of Solar Cell

Drive Level Capacitance Profiling (DLCP)

Drive Level Capacitance Profiling (DLCP) is a technique for determining the defect density (N_{DL}) as a function of depth of a photovoltaic cell[1]. During the DLCP measurement, the applied AC voltage (peak-to-peak) is swept and the DC voltage is varied while the capacitance is measured. This is in contrast to the conventional C-V profiling technique, in which the AC rms voltage is fixed and the DC voltage is swept.

In DLCP, the DC voltage is automatically adjusted to keep the total applied voltage (AC + DC) constant while the AC voltage is swept. By maintaining a constant total bias, the exposed charge density (ρ_e) inside the material stays constant up to a fixed location (x_e), which is defined as the distance from the interface where $E_F - E_v = E_e$. This is also in contrast to conventional C-V profiling, the analysis of which assumes that the only charge density changes occur at the end of the depletion region.[1]

1 J. T. Heath, J. D. Cohen, W. N. Shafarman, "Bulk and metastable defects in $CuIn_{1-x}Ga_xSe_2$ thin films using drive-level capacitance profiling," *Journal of Applied Physics*, vol. 95, no. 3, p. 1000, 2004

Thus, in DLCP, the position (x_e) can be varied by adjusting the DC voltage bias to the sample. This also allows determining the defect density as a function of the distance, or special profiling. The test frequency and temperature of the measurement can also be varied to show a profile that is energy dependent.

Once the measurements are taken, a quadratic fit of the C-V data is related to the impurity density at a given depletion depth as follows for a p-type semiconductor:

$$N_{DL} \equiv \frac{C_0^3}{2q\varepsilon A^2 C_1} = \frac{|\rho_e|}{q} = p + \int_{E_F^0}^{E_V+E_e} g(E, x_e)\,dE$$

where:

N_{DL} = defect density (cm^{-3})

C1, C0 = coefficients of quadratic fit of C-V data

q = electron charge (1.60×10^{-19}C)

ε = permittivity (F/cm)

A = area of solar cell (cm^2)

ρ_e = charge density (C/cm^3)

p = hole density (cm^{-3})

x_e = distance from interface where $E_F - E_v = E_e$

The coefficients C_0 and C_1 are determined via a full least-squares best fit of the data to a quadratic equation:

$$dQ/dV = C_2\,(dV)^2 + C_1*(dV) + C_0$$

However, only the C_0 and C_1 coefficients are used in the analysis.

The *"DLCP"* UTM allows making C-V measurements for drive level capacitance profiling. During these measurements, the total applied voltage remains constant as the DC voltage bias is automatically adjusted as the AC voltage drive level amplitude varies. The AC amplitude of the 4210-CVU can vary from $10mV_{rms}$ to $100mV_{rms}$ (14.14mV to $141.4mV_{p-p}$). The range of frequency can also be set from 1kHz to 10MHz. The capacitance is measured as the AC voltage is sweeping.

Table 2 lists the input parameters used in the UTM, the allowed range of input values, and descriptions. The user inputs the total applied voltage (VmaxTotal), the AC start, stop, and step voltages (VacppStart, VacppStop, and VacppStep), the time between voltage steps (SweepDelay), the test frequency (Frequency), the measurement speed (Speed), the measurement range (CVRange), and offset compensation (OpenComp, ShortComp, LoadComp, and LoadVal).

Once the test is executed, the capacitance, AC voltage, DC voltage, time stamp, frequency, and the defect density (N_{DL}) are determined and their values are listed in the Sheet tab. The defect density is calculated in the Formulator using a quadratic line fit of the C-V data. The coefficients (C_0 and C_1) of the quadratic equation are also listed in the Sheet tab. The user inputs the area and permittivity of the solar cell to be tested into the Constants/Values/Units area of the Formulator.

Figure 15 shows the measurement results in the graph of capacitance vs. AC voltage p-p. Notice the coefficients of the

Table 2. Adjustable parameters for the *DLCP* UTM

Parameter	Range	Description
VmaxTotal	–10 to 10 volts	Applied DC Volts and ½ AC Volts p-p
VacppStart	.01414 to .1414	Start Vac p-p
VacppStop	.02828 to .1414	Stop Vac p-p
VacppStep	.0007070 to .1414	Step Vac p-p
SweepDelay	0 to 100	Sweep delay time in seconds
Frequency	1E+3 to 10E+6	Test Frequency in Hertz
Speed	0, 1, 2	0=Fast, 1=Normal, 2=Quiet
CVRange	0, 1E–6, 30E–6, 1E–3	0=autorange, 1μA, 30μA, 1mA
OpenComp	1, 0	Enables/disables open compensation for CVU
ShortComp	1, 0	Enables/disables short compensation for CVU
LoadComp	1, 0	Enables/disables load compensation for CVU
LoadVal	1 to 1E+9	Load value

derived quadratic line fit and the defect density are displayed on the graph.

The capacitance measurements can be repeated at various applied total voltages in order to vary the position of x_e. The energy (E_e) can be varied by changing the test frequency (1kHz to 10MHz) or the temperature. To change the temperature of the measurement, the user can add a User Test Module (UTM) to control a temperature controller via the Model 4200-SCS's GPIB interface. The Model 4200-SCS is provided with user libraries for operating the Temptronics and Triotek temperature controllers.

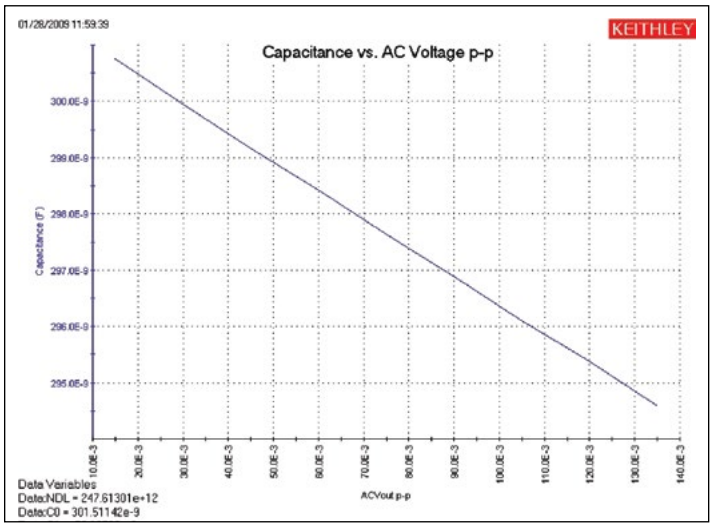

Figure 15. Capacitance vs. AC voltage p-p of a solar cell

Pulsed I-V Measurements

Pulsed I-V measurements can be useful for studying parameters of solar cells. In particular, pulsed I-V measurements have been used to determine the conversion efficiency, minimum carrier lifetime, and the effects of cell capacitance. The Model 4225-PMU, the Model 4200-SCS's optional Ultra-Fast I-V Module, can output pulsed voltage and measure current, and can capture ultra-high-speed current or voltage waveforms in the time domain. In addition to sourcing a pulsed voltage, the PMU can sink current so it can measure a solar cell's current output.

To make pulsed I-V measurements on a solar cell, the Model 4225-PMU is connected to the cell as shown in ***Figure 16***. Each PMU has two channels so the solar cell can be connected using either one or two channels. In the one-channel case shown, one end of the cell is connected to the HI terminal of PMU CH1 and the other side of the cell is connected to the shield of the coax cable, which is the LO terminal of the PMU.

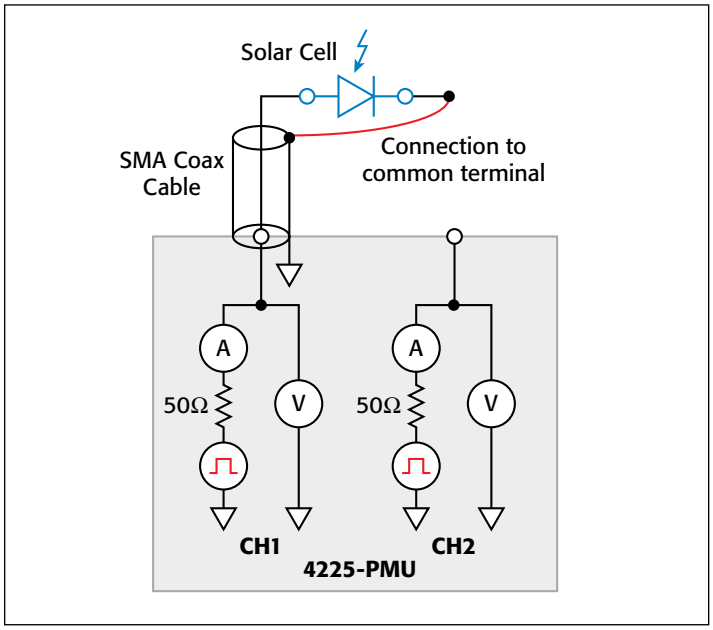

Figure 16. Connecting the solar cell to the Model 4225-PMU Ultra-Fast I-V Module

Unlike the DC I-V and C-V measurements, the 4225-PMU uses a two-wire technique. The Short Compensation feature can be used to "zero out" the voltage drops due to the cables so that a 4-wire measurement technique isn't necessary.

Because solar cells are fairly capacitive, it is important to ensure the pulse width is long enough for the pulsed I-V sweep.

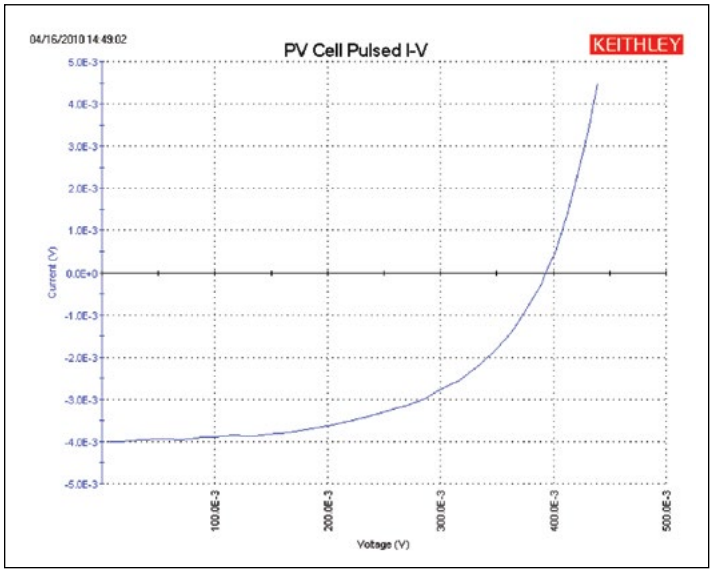

Figure 17. Pulsed I-V measurement on solar cell using Model 4225-PMU

The waveform capture mode should be used to verify the pulse width prior to generating the pulsed I-V sweep. The waveform capture mode enables a time-based current and/or voltage measurement that is typically the capture of a pulsed waveform. This can be used to perform a dynamic test on the cell or used as a diagnostic tool for choosing the appropriate pulse settings in the pulsed I-V mode. Given that larger solar cells have larger capacitances, it may be necessary to reduce the area of the cell itself to avoid a long settling time in the measurement.

The results of generating a pulsed I-V measurement sweep on a silicon solar cell are shown in ***Figure 17***. Note that the current is in the fourth quadrant of the curve. This indicates that the PMU is sinking current; in other words, the current is flowing out of the solar cell and into the PMU.

Resistivity and Hall Voltage Measurements

Determining the resistivity of a solar cell material is a common electrical measurement given that the magnitude of the resistivity directly affects the cell's performance. Resistivity measurements of semiconductor materials are usually performed using a four-terminal technique. Using four probes eliminates errors due to the probe resistance, spreading resistance under each probe, and the contact resistance between each metal contact and the semiconductor material. Two common techniques for determining the resistivity of a solar cell material are the four-point collinear probe method and the van der Pauw method. The *SolarCell* project contains several ITMs for making both types of measurements. More detailed information about making resistivity measurements on semiconductor materials using the Model 4200-SCS can be found in Keithley Application Note #2475, "Four-Probe Resistivity and Hall Voltage Measurements with the Model 4200-SCS."

Four-Point Collinear Probe Measurement Method

The four-point collinear probe technique involves bringing four equally spaced probes in contact with a material of unknown resistance. The probe array is placed in the center of the material as shown in ***Figure 18***. The two outer probes are used to source current and the two inner probes are used to measure the resulting voltage difference across the surface of the material.

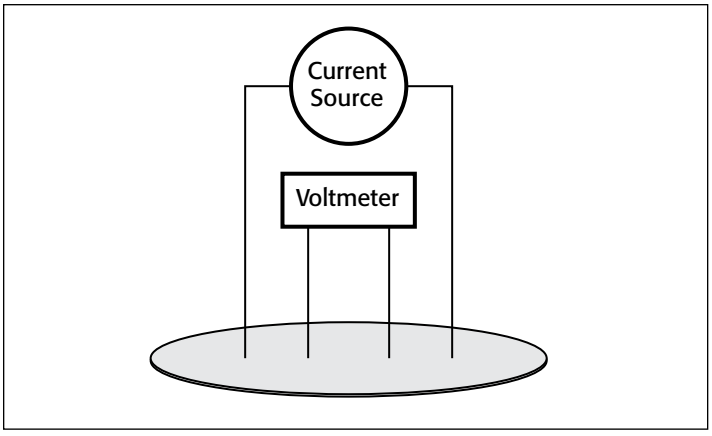

Figure 18. Four-point collinear probe resistivity configuration

From the sourced current and the measured voltage, the surface or sheet resistivity is calculated by:

$$\sigma = \frac{\pi}{\ln 2} \times \frac{V}{I}$$

where:
σ = surface resistivity (Ω/□)
V = the measured voltage (V)
I = the source current (A)

Note that the units for sheet resistivity are expressed as ohms per square (Ω/□) in order to distinguish this number from the measured resistance (V/I), which is simply expressed in ohms. Correction factors to the resistivity calculation may be required for extremely thin or thick samples or if the diameter of the sample is small relative to the probe spacing.

If the thickness of the sample is known, the volume resistivity can be calculated as follows:

$$\rho = \frac{\pi}{\ln 2} \times \frac{V}{I} \times t \times k$$

where:

ρ = volume resistivity (Ω-cm)

t = the sample thickness (cm)

k = a correction factor* based on the ratio of the probe spacing to wafer diameter and on the ratio of wafer thickness to probe spacing

* The correction factors can be found in a standard four-point probe resistivity test procedure such as *Semi MF84: Standard Test Method for Measuring Resistivity of Silicon Wafers With an In-Line Four-Point Probe*. This standard was originally published by ASTM International as ASTM F 84.

Using the Four-Point Probe ITMs, *HiR* and *LoR*

The *"HiR"* and *"LoR"* ITMs are both used for making four-point collinear probe measurements. The *"HiR"* ITM can be used for materials over a wide resistance range, ~1mΩ to 1TΩ. The Model 4200-PA preamps are required for making high resistance measurements (>1MΩ). The *"LoR"* ITM is intended for measurements of lower resistance materials (~1mΩ–1kΩ).

A screenshot of the *"HiR"* ITM for measuring four-probe resistivity is shown in ***Figure 19***.

The *"HiR"* ITM uses either three or four SMU instruments to make the resistivity measurements. One SMU instrument (SMU1) and the ground unit (GNDU) are used to source current between the outer two probes. Two other SMU instruments (SMU2 and SMU3) are used to measure the voltage drop between the two inner probes. The Force HI terminal of each SMU instrument is connected to each of the four probes. The SMU instrument designation for this configuration is shown in ***Figure 20***.

In the Formulator, the voltage difference between SMU2 and SMU3 is calculated and the resistance and sheet resistivity are derived from the voltage difference. The results appear in the Sheet tab of the ITM.

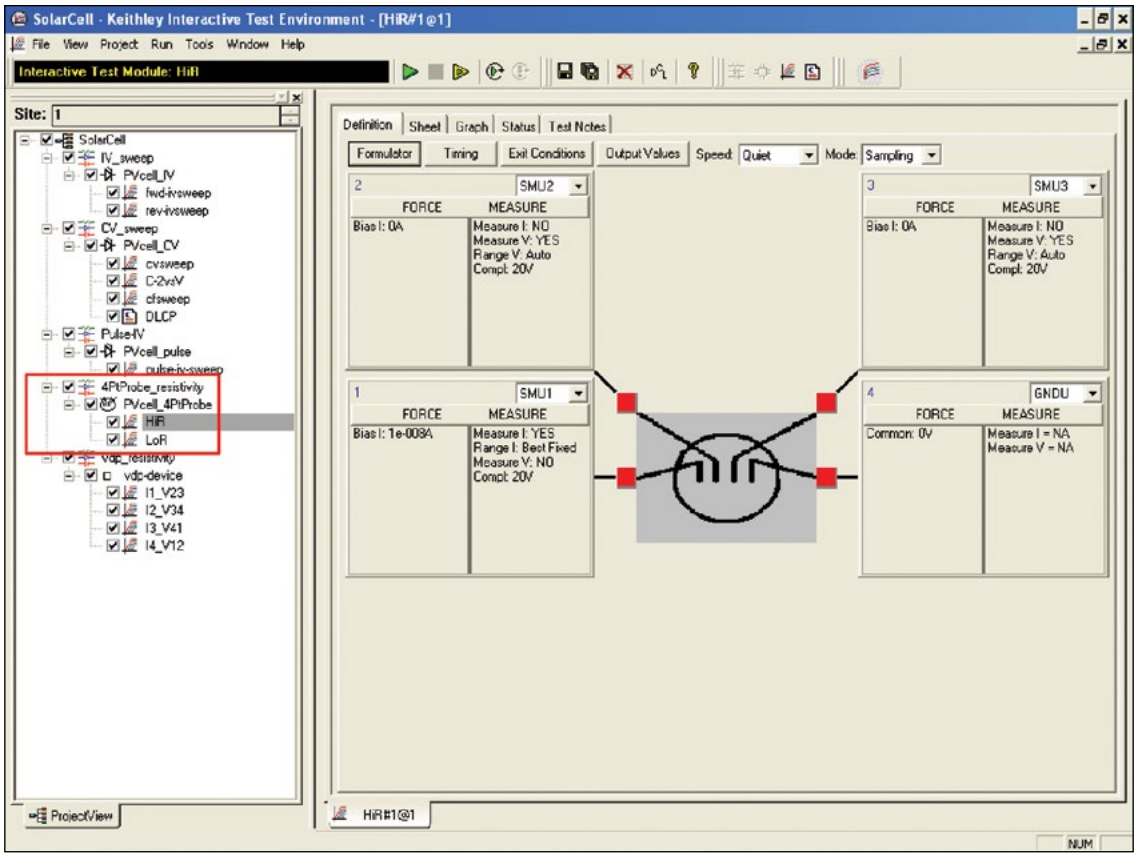

Figure 19. "HiR" test module for measuring resistivity

When making high resistance measurements, potential sources of error need to be considered in order to make optimal measurements. Use a probe head that has a level of insulation resistance between the probes that is sufficiently higher than the resistance of the material to be measured. This will help prevent errors due to leakage current through the probe head. Ensure that the measurement circuit is electrostatically shielded by enclosing the circuit in a metal shield. The shield is connected to the LO terminal of the 4200. The LO terminal is located on the GNDU or on the outside shell of the triax connectors. Use triax cables to produce a guarded measurement circuit. This will prevent errors due to leakage current and significantly reduce the test time. Finally, the Model 4200-PA preamp option is required to source very small currents (nanoamp and picoamp range) and to provide high input impedance (>1E16 ohms) to avoid loading errors when measuring the voltage difference.

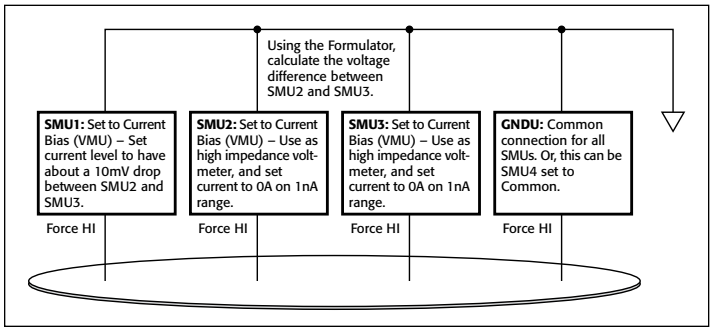

Figure 20. SMU instrument designation for four-point collinear probe measurements

The *"LoR"* ITM is only used for lower resistance materials and requires only one or two SMU instruments. In this case, the Force and Sense terminals of the SMU instruments are connected to the four-point probe as shown in ***Figure 20***.

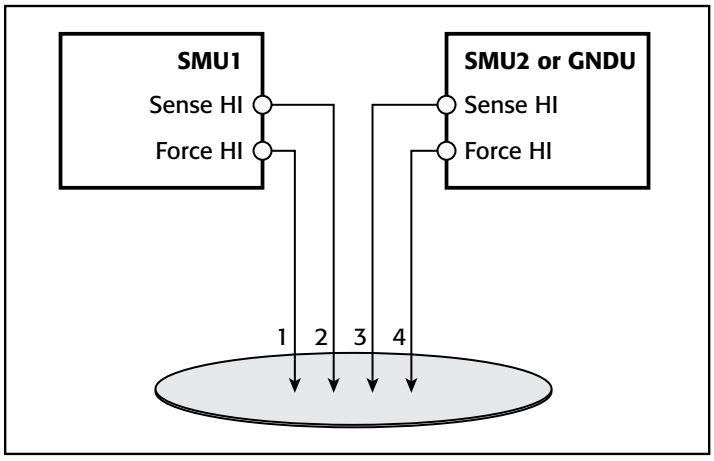

Figure 21. Connecting two SMU instruments for four-point probe measurements

In the configuration shown in ***Figure 21***, the Force HI terminal SMU1 sources the current through Probe 1. The voltage difference between Probes 2 and 3 is measured through the Sense terminals of the two SMU instruments.

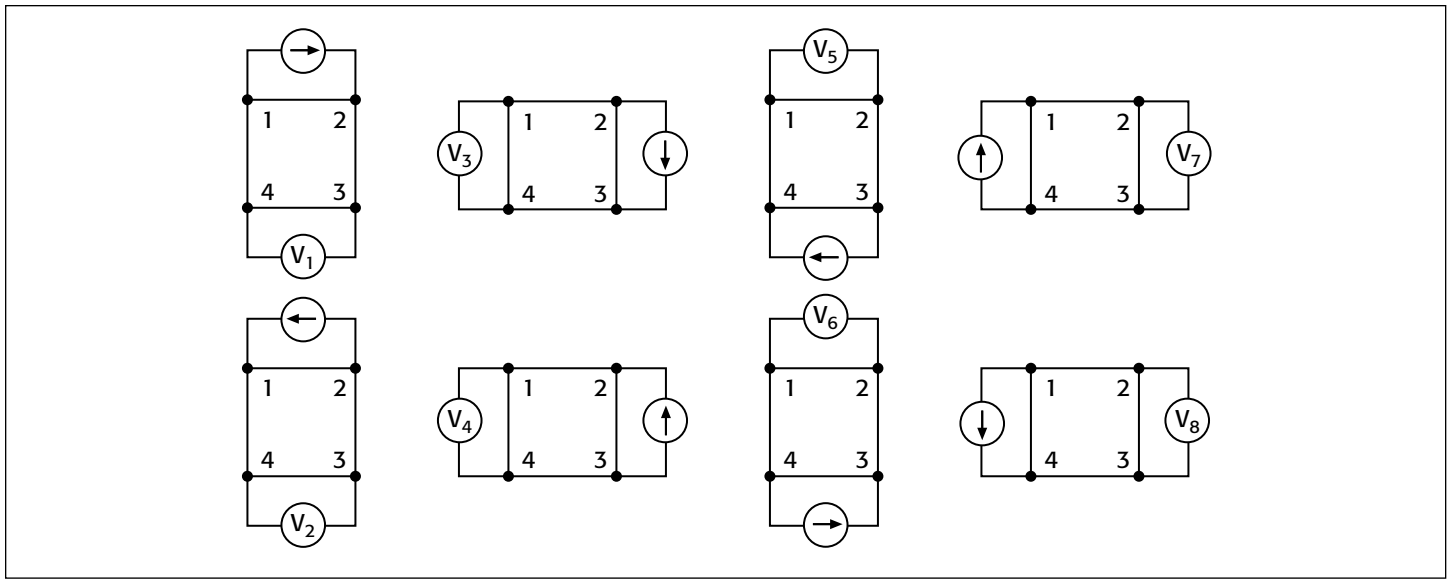

Figure 22. Van der Pauw resistivity measurement conventions

To compensate for thermoelectric offset voltages, two voltage measurements are made with currents of opposite polarity. The two measurements are combined and averaged to cancel the thermoelectric EMFs. The *"LoR"* ITM performs this offset correction automatically by sourcing the two current values in the List Sweep and then mathematically correcting for the offsets in the Formulator. The corrected resistance and sheet resistivity are displayed in the Sheet tab.

Measuring Resistivity with the van der Pauw Method

The van der Pauw (vdp) technique for measuring resistivity uses four isolated contacts on the boundary of a flat, arbitrarily shaped sample. The resistivity is derived from eight measurements made around the sample as shown in ***Figure 22***.

Once all the voltage measurements have been taken, two values of resistivity, ρ_A and ρ_B, are derived as follows:

$$\rho_A = \frac{\pi}{\ln 2} f_A t_s \frac{(V_2 + V_4 - V_1 - V_3)}{4I}$$

$$\rho_B = \frac{\pi}{\ln 2} f_B t_s \frac{(V_6 + V_8 - V_5 - V_7)}{4I}$$

where:

ρ_A and ρ_B are volume resistivities in ohm-cm;

t_s is the sample thickness in cm;

V_1–V_8 represent the voltages measured by the voltmeter;

I is the current through the sample in amperes;

f_A and f_B are geometrical factors based on sample symmetry, and are related to the two resistance ratios Q_A and Q_B as shown in the following equations ($f_A = f_B = 1$ for perfect symmetry).

Q_A and Q_B are calculated using the measured voltages as follows:

$$Q_A = \frac{V_2 - V_1}{V_4 - V_3}$$

$$Q_B = \frac{V_6 - V_5}{V_8 - V_7}$$

Also, Q and f are related as follows:

$$\frac{Q - 1}{Q + 1} = \frac{f}{0.693} \operatorname{arc\,cosh}\left(\frac{e^{0.693/f}}{2}\right)$$

A plot of this function is shown in ***Figure 23***. The value of "f" can be found from this plot once Q has been calculated.

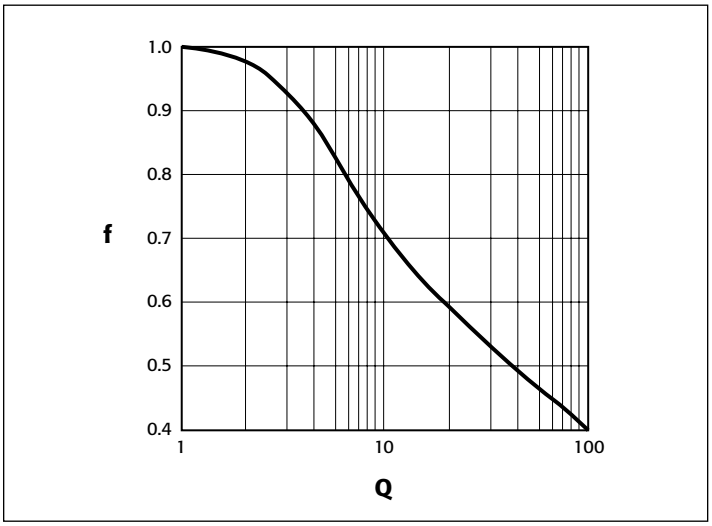

Figure 23. Plot of f vs. Q

Once ρ_A and ρ_B are known, the average resistivity (ρ_{AVG}) can be determined as follows:

$$\rho_{AVG} = \frac{\rho_A + \rho_B}{2}$$

Using the *vdp_resistivity* subsite and vdp method ITMs

To automate the vdp resistivity measurements, the *SolarCell* project has a *vdp-resistivity* subsite with four ITMs: *"I1_V23"*,

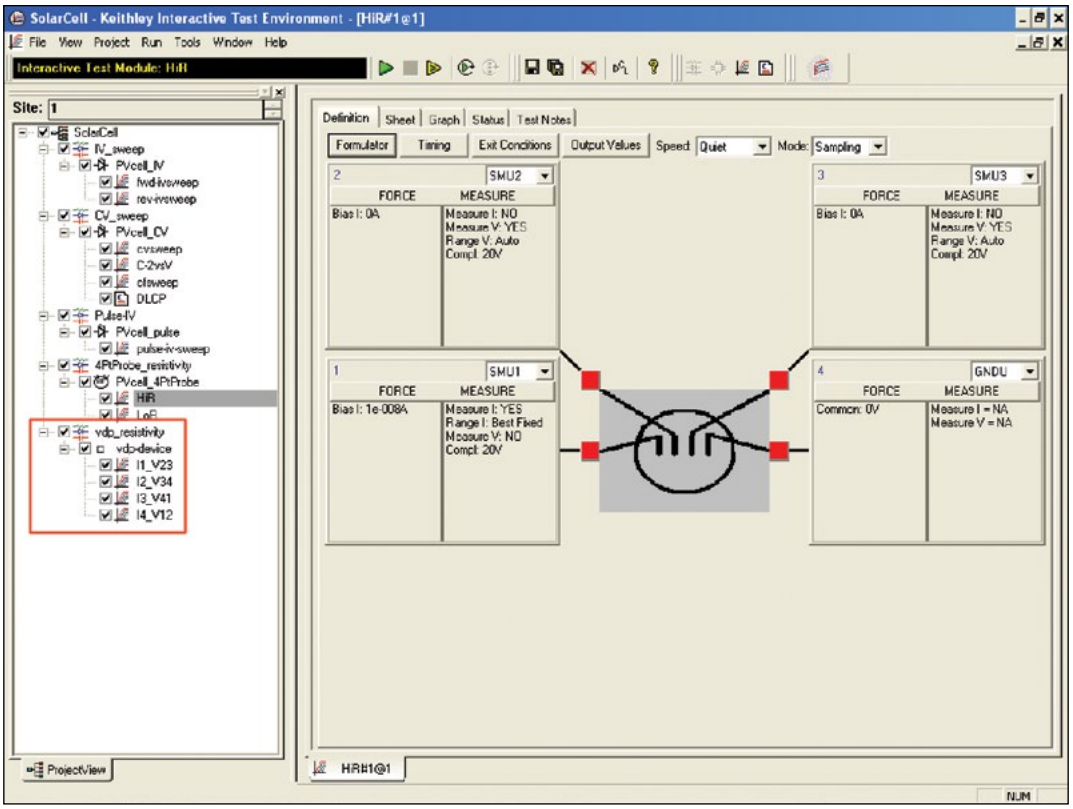

Figure 24. Screenshot of van der Pauw test

"*I2_V34*", "*I3_V41*", and "*I4_V12*." A screenshot of the test is shown in ***Figure 24***.

Each terminal of the sample is connected to the Force HI terminal of an SMU instrument, so a Model 4200-SCS with four SMU instruments is required. The four SMU instruments are configured differently in each of the four ITMs – one SMU instrument supplies the test current, two are configured as voltmeters, and one is set to common. This measurement setup is repeated around the sample, with each of the four SMU instruments serving a different function

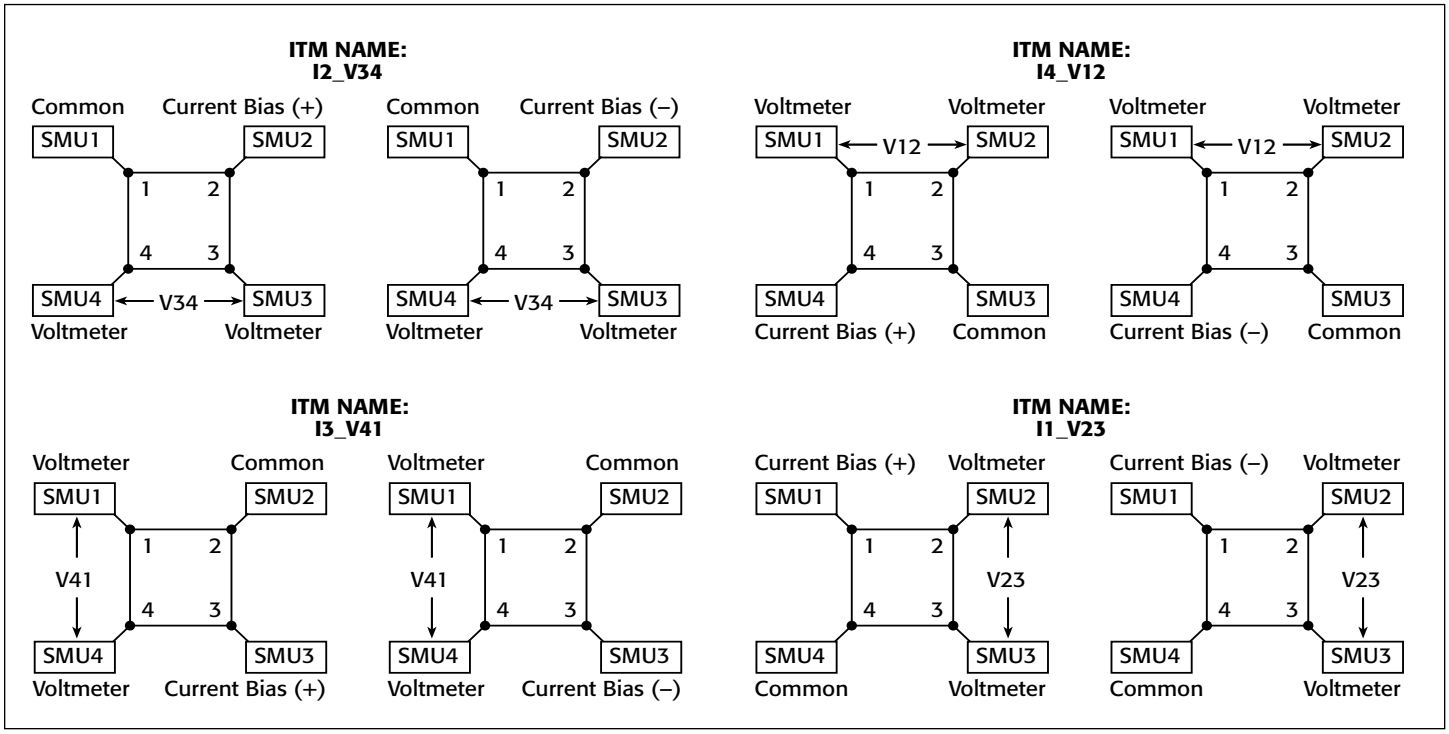

Figure 25. SMU instrument configurations for van der Pauw measurements

in each of the four ITMs. A diagram of the function of each SMU instrument in each ITM is shown in ***Figure 25***.

Adjusting the Test Parameters

Before executing the test, some of the test parameters must be adjusted based on the sample to be tested. In particular, it's necessary to specify the source current, the settling time, and the thickness of the material.

Input Source Current: Before running the project, input the current source values based on the expected sample resistance. Adjust the current so that the voltage difference will not exceed approximately 25mV to keep the sample in thermal equilibrium. In each of the four ITMs, enter both polarities of the test current. The same magnitude must be used for each ITM.

Input the Settling Time: For high resistance samples, it will be necessary to determine the settling time of the measurements. This can be accomplished by creating an ITM that sources current into two terminals of the samples and measures the voltage drop on the adjacent two terminals. The settling time can be determined by taking multiple voltage readings and then graphing the voltage difference as a function of time.

This settling time test can be generated by copying and then modifying one of the existing vdp ITMs. Switch the source function from the sweep mode to the sampling mode. Then, in the Timing menu, take a few hundred or so readings with a delay time of one second. Make sure that the "Timestamp Enabled" box is checked. After the readings are done, plot the voltage difference vs. time on the graph. The settling time is determined by observing the graph and finding the time when the reading is within the desired percentage of the final value.

Input the Thickness of the Sample: Enter the thickness of the sample into the Calc sheet at the subsite level. Select the subsite *vdp_resistivity*. Go to the Subsite Data *vdp-device* tab. It contains the output values of the voltage differences and test current. From the Calc tab, the thickness can be adjusted. The default thickness is 1cm.

Input Correction Factor: The resistivity formula found in the Calc sheet at the subsite level also allows inputting a correction factor, if necessary. The resistivity is multiplied by this number, which may be based on the geometry or uniformity of the sample. By default, the correction factor is 1.

Running the Project

The van der Pauw resistivity measurements must be run at the subsite level. Make sure that all four checkboxes in front of the vdp ITMs (*"I1_V23*," *"I2_V34*," *"I3_V41*," and *"I4_V12"*) are checked and then click on the subsite *vdp_resistivity*. Execute the project by using the subsite Run button (circular arrow). Each time the test is run, the subsite data is updated. The voltage differences from each of the four ITMS will appear in the Subsite Data

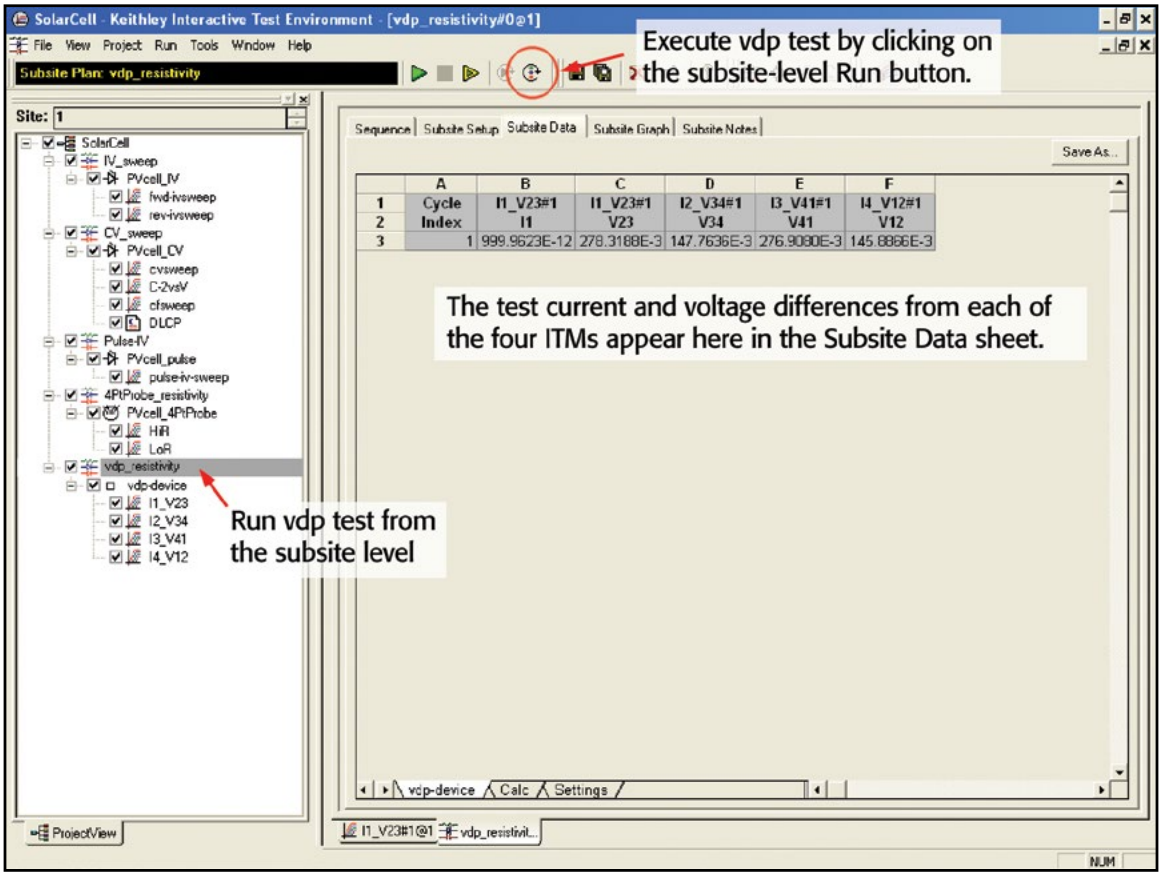

Figure 26. Executing the vdp_resistivity test

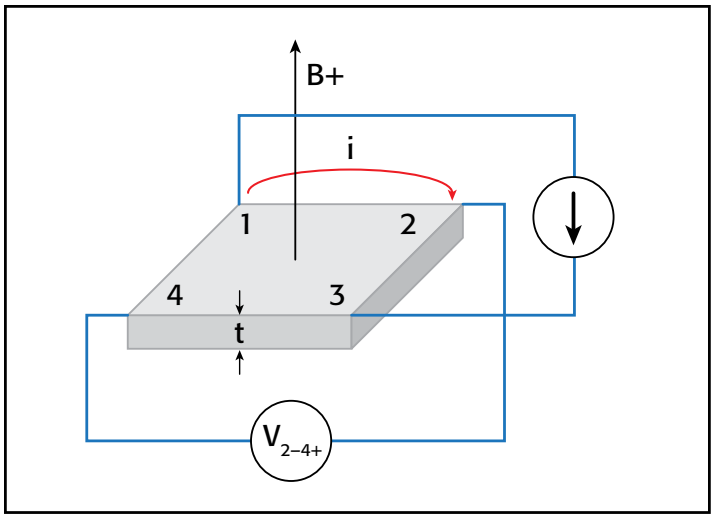

Figure 27. Hall voltage measurement

vdp-device Sheet tab. The resistivity will appear in the Subsite Data Calc sheet as shown in ***Figure 26***.

Hall Voltage Measurements

Hall effect measurements are important to semiconductor material characterization because the conductivity type, carrier density, and Hall mobility can be derived from the Hall voltage. With an applied magnetic field, the Hall voltage can be measured using the configuration shown in ***Figure 27***.

With a positive magnetic field (B–), apply a current between Terminals 1 and 3 of the sample, and measure the voltage drop (V_{2-4+}) between Terminals 2 and 4. Reverse the current and measure the voltage drop (V_{4-2+}). Next, apply current between Terminals 2 and 4, and measure the voltage drop (V_{1-3+}) between Terminals 1 and 3. Reverse the current and measure the voltage drop (V_{3-1+}) again.

Reverse the magnetic field (B–) and repeat the procedure, measuring the four voltages: (V_{2-4-}), (V_{4-2-}), (V_{1-3-}), and (V_{3-1-}). ***Table 3*** summarizes the Hall voltage measurements.

Table 3. Summary of Hall Voltage Measurements

Voltage Designation	Magnetic Flux	Current Forced Between Terminals	Voltage Measured Between Terminals
V2–4+	B+	1–3	2–4
V4–2+	B+	3–1	4–2
V1–3+	B+	2–4	1–3
V3–1+	B+	4–2	3–1
V2–4–	B–	1–3	2–4
V4–2–	B–	3–1	4–2
V1–3–	B–	2–4	1–3
V3–1–	B–	4–2	3–1

From the eight Hall voltage measurements, the average Hall coefficient can be calculated as follows:

$$R_{HC} = \frac{t(V_{4-2+} - V_{2-4+} + V_{2-4-} - V_{4-2-})}{4BI}$$

$$R_{HD} = \frac{t(V_{3-1+} - V_{1-3+} + V_{1-3-} - V_{3-1-})}{4BI}$$

where:

R_{HC} and R_{HD} are Hall coefficients in cm^3/C;

t is the sample thickness in cm;

V represents the voltages measured in V;

I is the current through the sample in A;

B is the magnetic flux in Vs/cm^2

Once R_{HC} and R_{HD} have been calculated, the average Hall coefficient (R_{HAVG}) can be determined as follows:

$$R_{HAVG} = \frac{R_{HC} + R_{HD}}{2}$$

From the resistivity (ρ_{AVG}) and the Hall coefficient (R_H), the Hall mobility (μ_H) can be calculated:

$$\mu_H = \frac{|R_H|}{\rho_{AVG}}$$

Using the Model 4200-SCS to Measure the Hall Voltage

The *SolarCell* project does not include a specific test to measure the Hall voltage; however, four ITMs can be added to the subsite for determining the Hall coefficient and mobility. Given that the configuration for the Hall measurements is very similar to the van der Pauw resistivity measurements, the vdp ITMs can be copied and modified for making the Hall voltage measurements. The modifications involve changing the functions of the SMU instruments. ***Figure 28*** illustrates how to configure the four SMU instruments in the ITMs to measure the Hall voltage. Use the Output Value checkboxes on the Definition tab to return the Hall voltages to the subsite-level Calc sheet.

User Test Modules (UTMs) must be added to control the magnet. For a GPIB-controlled electromagnet, users can write a program using KULT (the Keithley User Library Tool) to control the magnitude and polarity of the electromagnet. The code can be opened up in a UTM within the project. Information on writing code using KULT is provided in Section 8 of the Model 4200-SCS Reference Manual.

If a permanent magnet is used, UTMs can be employed to create a Project Prompt that will stop the test sequence in the project tree and instruct the user to change the polarity of the magnetic field applied to the sample. A Project Prompt is a dialog window that pauses the project test sequence and prompts the user to perform some action. See Section A of the Model 4200-SCS Reference Manual for a description of how to use Project Prompts.

Finally, the Hall coefficient and mobility can be derived in the subsite-level Calc sheet. These math functions can be added to the other equations for determining resistivity.

Conclusion

Measuring the electrical characteristics of a solar cell is critical for determining the device's output performance and efficiency. The Model 4200-SCS simplifies cell testing by automating the I-V, C-V, pulsed I-V, and resistivity measurements and provides

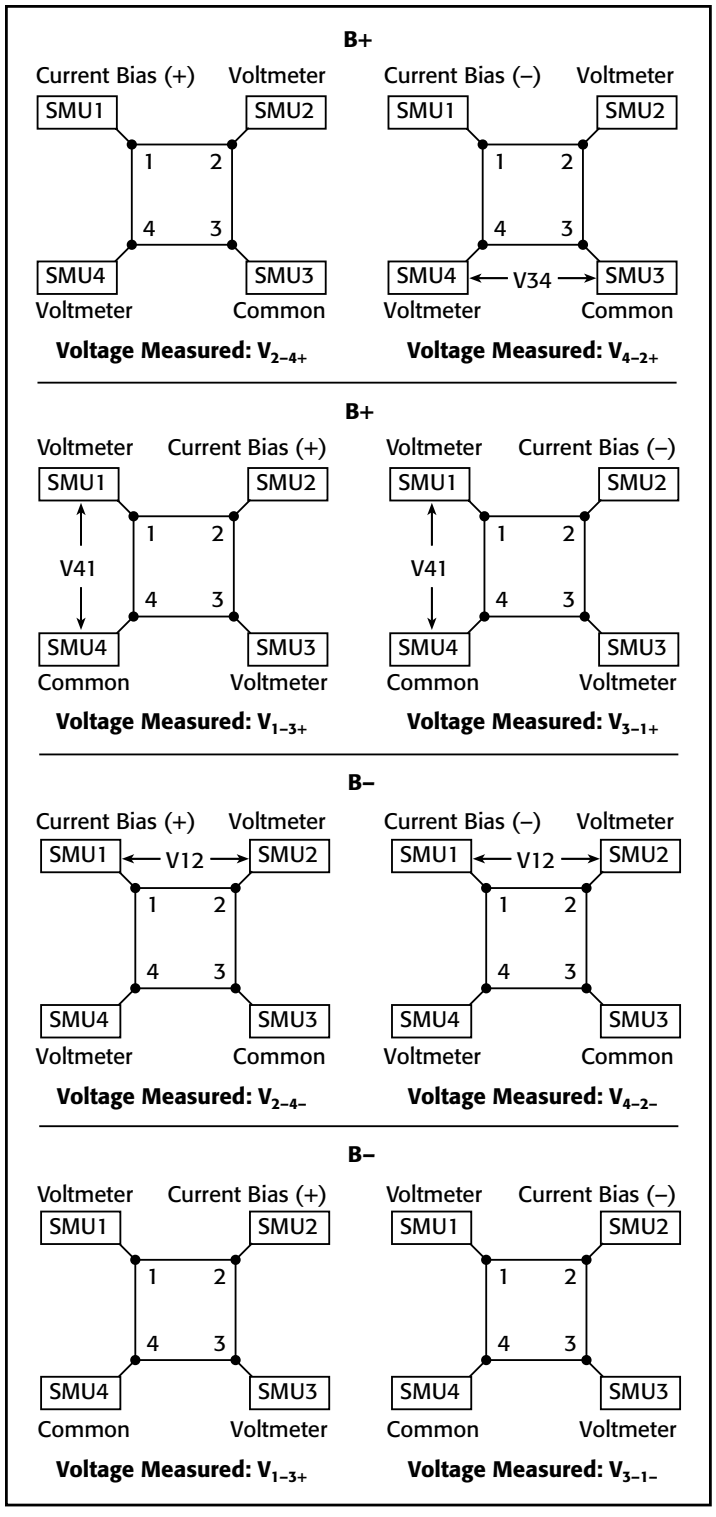

Figure 28. SMU configurations for Hall voltage measurements

graphics and analysis capability. For measurements of currents greater than 1A, Keithley offers Series 2400 and Series 2600B SourceMeter Instruments that can be used for solar cell testing. Information on these models and further information on making solar cell measurements can be found on Keithley's website: www.keithley.com.

Evaluating Oxide Reliability Using V-Ramp and J-Ramp Techniques

Introduction

Oxide integrity is an important reliability concern, especially for today's MOSFET devices, where oxide thickness has been scaled to a few atomic layers. The JEDEC 35 Standard (EIA/JESD35, Procedure for Wafer-Level Testing of Thin Dielectrics) describes two wafer level test techniques commonly used to monitor oxide integrity: voltage ramp (V-Ramp) and current ramp (J-Ramp). Both techniques provide fast feedback for oxide evaluation.

The instrumentation used to monitor oxide breakdown must provide the following capabilities:

- Accurate voltage and current forcing and measurement capability
- Precise step time control
- Automated device parameter extraction
- Advanced data analysis techniques

This application note describes how to use the Keithley Model 4200-SCS Parameter Analyzer to perform oxide reliability testing.

The V-Ramp and J-Ramp Test Techniques

While the V-Ramp test applies a linear voltage ramp, the J-Ramp test applies an increasing logarithmic current ramp until oxide breakdown. The V-Ramp test begins at a low oxide voltage, so it is better able to detect low electric field failures, but it provides poor resolution at high electric fields. The J-Ramp test is different—it starts at a relatively high oxide voltage, so it provides poor low electric field resolution but better resolution at high electric fields. This resolution difference has led to the V-Ramp test often being used to determine infant mortality and low electric field fallout on larger test structures (extrinsic failures), while the J-Ramp test is often used on smaller test structures, where the oxide failure mode is expected to be intrinsic.

The V-Ramp Test Procedure

Figure 1 illustrates the V-Ramp test procedure. The sequence begins with a pre-test to determine initial oxide integrity. During the pre-test, a constant voltage (V_{use}) is applied and the oxide leakage current measured. If the oxide is determined to be "good," a linear voltage ramp is applied to the device until oxide failure. Oxide failure is detected by a sudden increase in current that is ten times the expected value or a measured oxide current that exceeds a specified current compliance. A post-test, which is performed at V_{use}, is used to determine the final state of the tested device. Extracted V-Ramp measurement parameters include the breakdown voltage (V_{BD}) and the charge to breakdown (Q_{BD}).

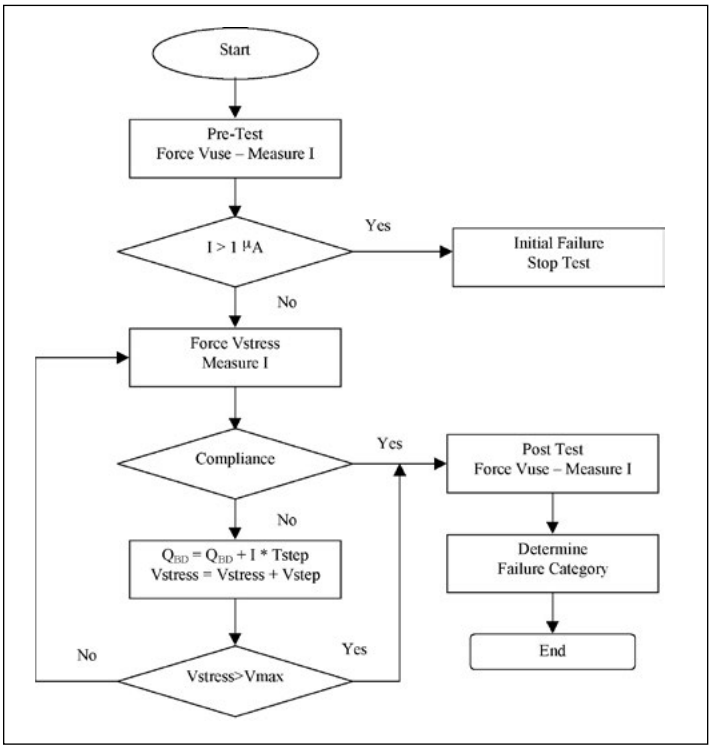

Figure 1. V-Ramp Flow chart

The J-Ramp Test Procedure

Figure 2 is an overview of the J-Ramp test methodology. The procedure begins with a pre-test to determine oxide integrity. In this pre-test, a constant current (typically 1μA) is applied and the voltage sustained across the oxide measured. If the device is "good," an increasing logarithmic step current [given by $I_{stress} = I_{prev} * F$ (where $F < 3.2$)] is applied until oxide failure. Oxide failure is detected when the voltage across the oxide drops 15% or more from the previous measured voltage (V_{prev}) or the charge limit is exceeded. A post constant current test is used to assess the final state of the tested device. Extracted J-Ramp oxide breakdown parameters include the breakdown voltage (V_{BD}) and the charge to breakdown (Q_{BD}).

Test Difficulties with V-Ramp and J-Ramp

Potential measurement difficulties can arise when implementing either test procedure. The voltage or current step time must be uniform and as precise as possible to determine Q_{BD} and V_{BD} accurately. In practice, this step time can be difficult to control

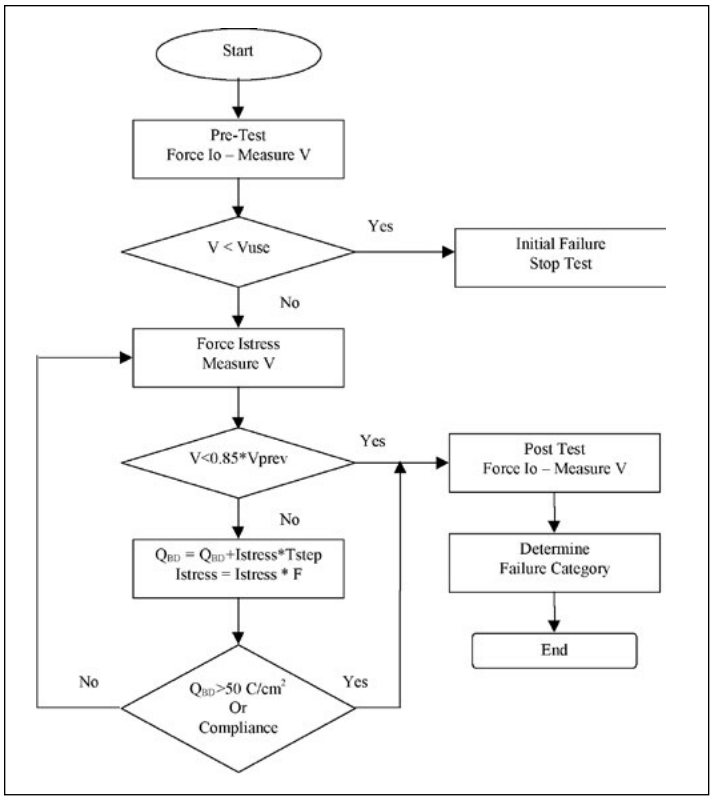

Figure 2. J-Ramp Flowchart

because of resolution and accuracy limitations associated with an external controller computer clock. In addition, instrument effects such as range changes can create unpredictable step time variations.

V-Ramp and J-Ramp Using the Keithley 4200-SCS

4200-SCS V-Ramp Test Setup

The Model 4200-SCS's built-in test sequencer and Interactive Test Module (ITM) capability simplifies implementing the V-Ramp and J-Ramp test algorithms. ***Figure 3*** shows the V-Ramp test sequence in the Project Navigator window and the V-Ramp module Definition Tab. The Project Navigator window displays the test sequence, which begins with a pre-test, followed by a linear voltage ramp (as defined in the V-Ramp module Definition Tab) to oxide breakdown. A post-test determines the final device state.

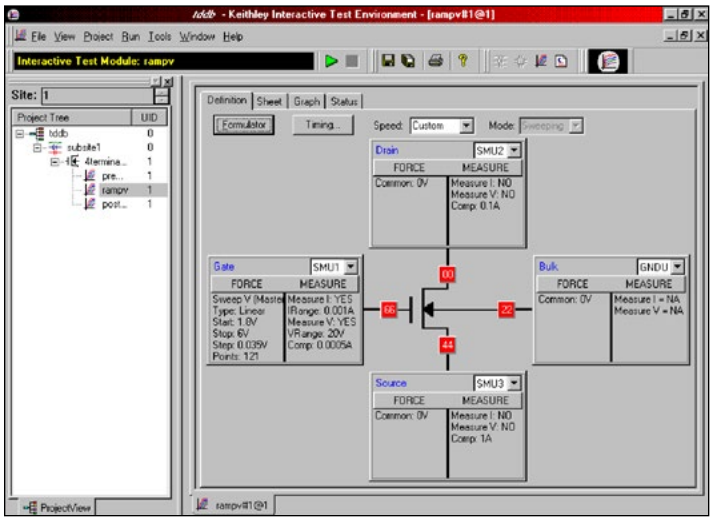

Figure 3. V-Ramp project test sequence and test definition.

The ITM Definition Tab makes it easy to specify source connections, Force-Measure options, and Timing. In the V-Ramp test illustrated in ***Figure 3***, the Gate source (SMU1) is set for a linear voltage sweep from 1.8V to 6.0V and a voltage step of 0.035V. The voltage step size is based on the JEDEC 35 Standard's 0.1MV/cm maximum voltage step height requirement (3.5nm oxide thickness). Specifying a fixed voltage source and current measurement ranges minimizes the effect of autoranging on voltage step time.

The linear voltage ramp rate is specified in the ITM Timing dialog entry screen (***Figure 4***), which is opened by clicking the Timing command button shown in ***Figure 3***. Source measure unit (SMU) instrument measurement time can be precisely controlled by selecting the Custom Speed option and specifying 1PLC A/D Integration Time (16.6ms). The sweep delay is the delay at each step before measurement.In this case, the sweep delay is chosen (83ms) so that the step time is ~100ms (83 + 16.6), yielding a voltage ramp rate of 1MV/cm*s, which is in accord with the JEDEC 35 Standard's 1MV/cm*s maximum ramp rate requirement. The 0.2s hold time, which occurs on the first voltage step, allows for displacement current settling before the voltage sweep begins. The ITM Timestamp Enabled feature is checked so that precise timing information is saved at each voltage step. This feature is extremely useful when determining Q_{BD} and verifying step timing precision. Post analysis of this data showed that voltage step time averaged 99.5ms (expected value 99.6ms) with a standard deviation of ±0.062ms.

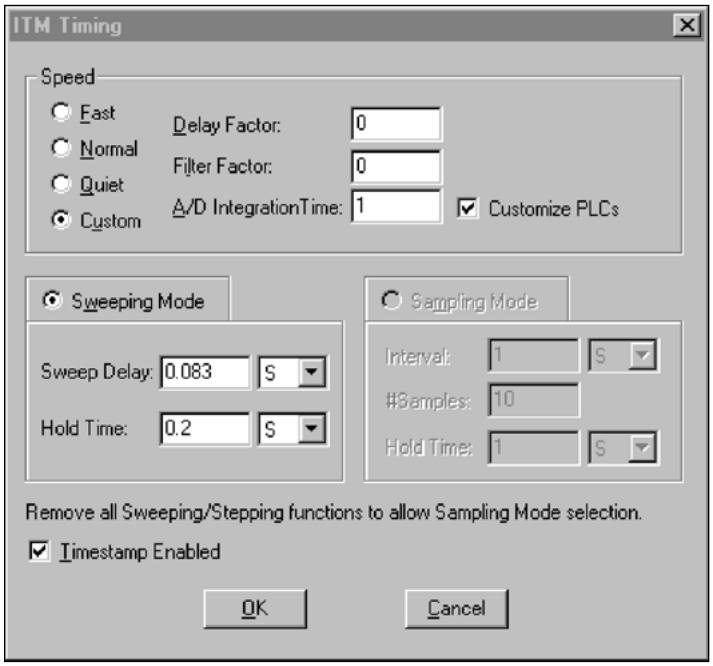

Figure 4. V-Ramp measurement and timing control.

4200-SCS V-Ramp Data Analysis

The Model 4200-SCS's powerful advanced data analysis capability can extract oxide breakdown parameters easily. This analysis feature is activated from the ITM Definition Tab by clicking the Formulator command button (see ***Figure 3***). The Formulator Dialog Entry screen (not shown) contains many functions for data analysis and extraction. A number of Formulator equations are used for automatically extracting the breakdown current (I_{BD}), breakdown voltage (V_{BD}), charge to breakdown (Q_{BD}) and time to breakdown (T_{BD}) from the V-Ramp measured gate current (I_G) vs. gate voltage (V_G) data:

QSUM = INTEG(TIME, IG)

FAILCURRENT = 0.5E-3

COLBD = COND(ABS(IG), ABS(0.98 * FAILCURRENT), 0, 1)

ROWBD = FINDD(COLBD, 1, FIRSTPOS(COLBD)) – 1

IBD = AT(IG, ROWBD)

VBD = AT(VG, ROWBD)

QBD = AT(QSUM, ROWBD)

TBD = AT(TIME, ROWBD)

The QSUM equation uses the integrate (INTEG) Formulator function to obtain the oxide charge. The oxide fail current (FAILCURRENT) is specified in the second equation. The equations employing the Conditional (COND) and Find Down (FINDD) functions determine the location of the breakdown row (ROWBD) in the Model 4200-SCS's built-in spreadsheet, which is compatible with Microsoft® Excel. The ROWBD is used in the AT Formulator function to extract I_{BD}, V_{BD}, Q_{BD}, and T_{BD}. Once extracted, parameters can be displayed automatically on the Model 4200-SCS's Graph Tab. ***Figure 5*** illustrates typical 4200-SCS V-Ramp data and extracted breakdown parameters from a 3.5nm oxide.

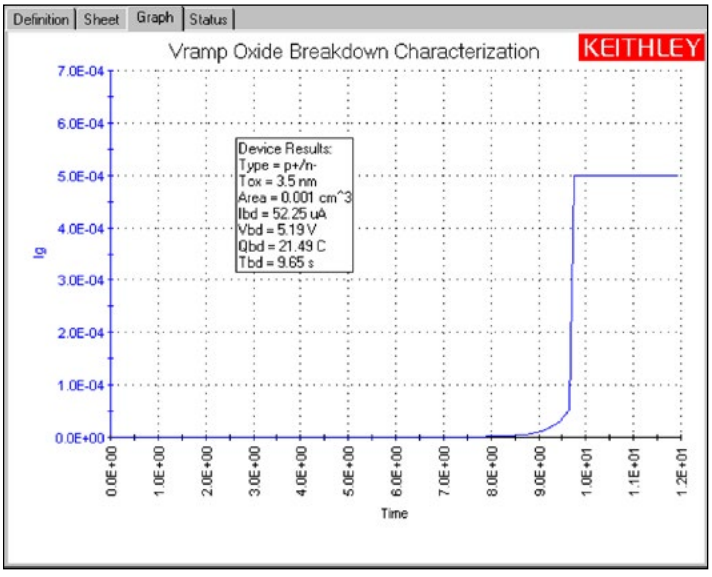

Figure 5. Typical 4200-SCS V-Ramp measurement results.

4200-SCS J-Ramp Test Setup

Figure 6 shows the J-Ramp test sequence in the Project Navigator window and the J-Ramp test module Definition Tab. The J-Ramp test sequence begins with a pre-test at a constant current to verify initial oxide integrity, followed by a logarithmic current ramp to oxide breakdown. A post-test determines the final device state.

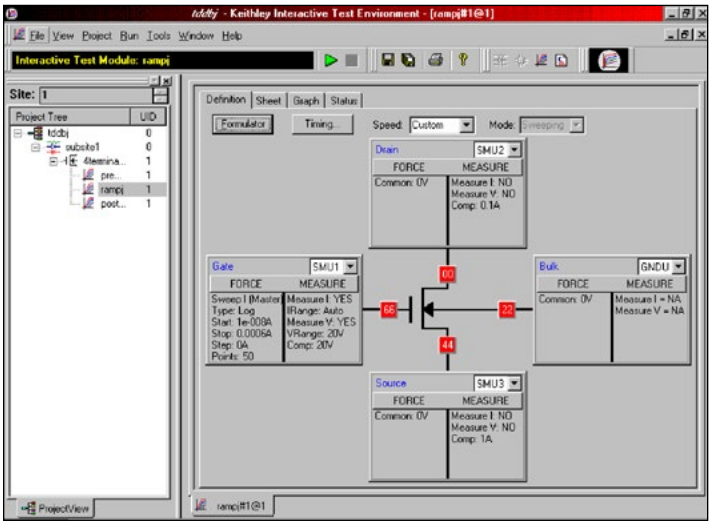

Figure 6. J-Ramp project test sequence and test definition.

The ITM Definition Tab in ***Figure 6*** specifies J-Ramp test conditions. In this case, the gate source (SMU1) is instructed to perform a logarithmic current sweep from 10nA to 0.6mA, where the number of steps in the current sweep is 50 (F = 1.25). Specifying a fixed voltage measurement range minimizes the effect of autoranging on step time.

As with the V-Ramp test, SMU instrument step time is precisely controlled by selecting the ITM Timing Custom Speed option and specifying the A/D Integration Time, sweep delay, hold time and the Timestamp Enabled feature (see ***Figure 4***). JEDEC Standard 35 specifies a current ramp rate of one decade/500ms.

4200-SCS J-Ramp Data Analysis

Just as with the V-Ramp test, the Formulator can be used to extract the J-Ramp oxide breakdown parameters (I_{BD}, V_{BD}, Q_{BD}, and T_{BD}) automatically. These equations are:

QSUM = INTEG(TIME, IG)

FAILRATIO = 0.85

RATIO = DELTA(VG)/(VG-DELTA(VG))

COLBD = COND(RATIO, FAILRATIO - 1, 0, 1)

ROWBD = FINDD(COLBD, 1, FIRSTPOS(COLBD)) – 1

IBD = AT(IG, ROWBD)

VBD = AT(VG, ROWBD)

QBD = AT(QSUM, ROWBD)

TBD = AT(TIME, ROWBD)

The QSUM equation determines the oxide charge. The second equation specifies the oxide fail ratio (FAILRATIO),

which corresponds to a 15% drop in the measured oxide voltage. The RATIO equation determines the ratio of the most recently measured V_G to the previous measured value. The next two equations use the COND and FINDD Formulator functions to determine the row location of the breakdown data (ROWBD). The last four equations use the AT Formulator function to extract the breakdown parameters (I_{BD}, V_{BD}, Q_{BD}, and T_{BD}) automatically. ***Figure 7*** shows typical Model 4200-SCS J-Ramp data and extracted breakdown parameters for a 3.5nm oxide.

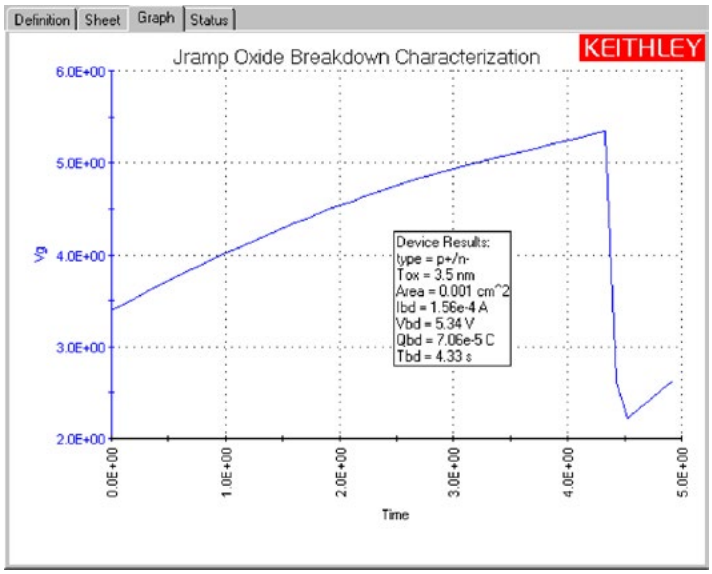

Figure 7. Typical 4200-SCS J-Ramp measurement results

Oxide Defect and Ultra-Thin Oxide Characterization

Oxide defects can create excessive tunneling currents at low electric fields. In addition, ultra-thin oxides (<6nm) show substantial direct tunneling oxide currents at low electric fields. To study these effects, it is necessary to monitor oxide currents in the femtoamp range, which makes the Model 4200-SCS an ideal tool for this application. ***Figure 8*** displays typical Model 4200-SCS voltage sweep data on a 3.5nm oxide, which was acquired using the SMU instrument's Quiet ITM Timing setting and autorange measurement options. These results demonstrate the Model 4200-SCS's excellent low current measurement sensitivity.

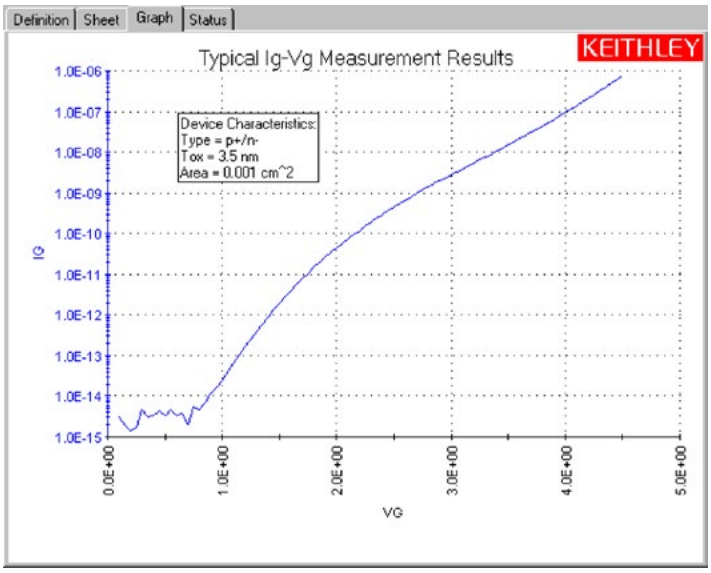

Figure 8. Typical 4200-SCS I-V measurement results.

Conclusion

The Model 4200-SCS's fast, flexible and easy-to-use test environment provides an ideal approach to characterizing oxide reliability. Its built-in software tools, such as the Project Navigator, the Formulator, and an Excel-compatible data format, greatly simplify creating test sequences and analyzing results. Custom SMU instrument timing controls and advanced SMU instrument technology set a new industry standard for measurement sensitivity, accuracy, and control.

References

1. EIA/JESD35. JC-14.2 Subcommittee. July 1992. "Procedure for Wafer Level Testing of Thin Dielectrics."

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