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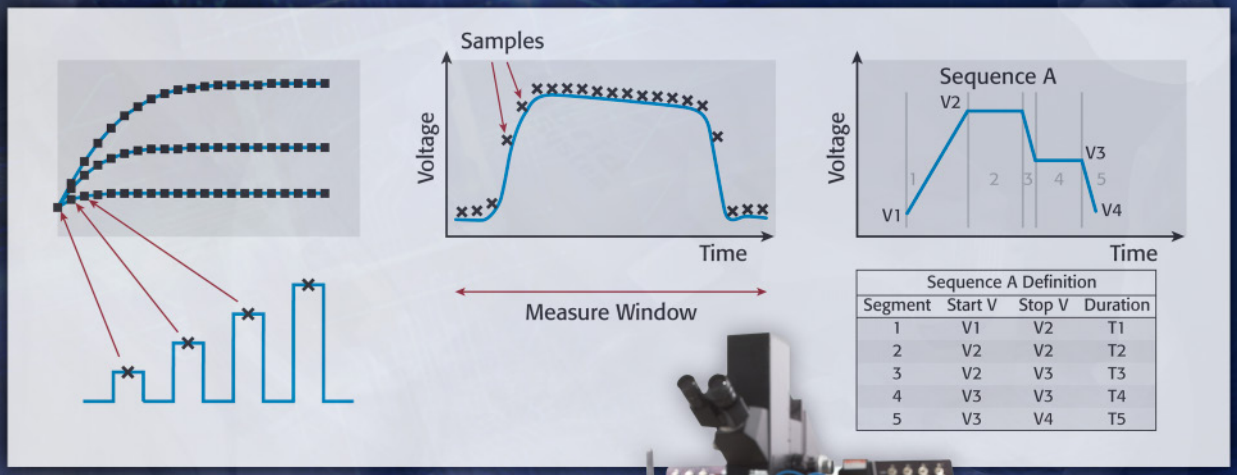
APPLICATIONS GUIDE



Sequence A Definition

Segment	Start V	Stop V	Duration
1	V1	V2	T1
2	V2	V2	T2
3	V2	V3	T3
4	V3	V3	T4
5	V3	V4	T5

Pulsed I-V Testing for Components and Semiconductor Devices

A GREATER MEASURE OF CONFIDENCE

KEITHLEY
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Pulsed I-V Testing for Components and Semiconductor Devices

Pulsed I-V testing is ideal for preventing device self-heating or minimizing charge trapping effects when characterizing devices. By using narrow pulses and/or low duty cycle pulses rather than DC signals, important parameters are extracted while maintaining the DUT performance. Transient I-V measurements allow scientists and engineers to capture ultra-high-speed current or voltage waveforms in the time domain in order to study dynamic properties. This pulsed I-V testing applications e-guide features a concentration of application notes on pulsed I-V testing methods and techniques using Keithley's Model 4200-SCS Parameter Analyzer.

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Making Proper Electrical Connections to Ensure Semiconductor Device Measurement Integrity

Introduction

Poor-quality electrical connections to the device under test (DUT) can compromise the measurement integrity of even the most powerful and sophisticated semiconductor test system. For high speed pulse measurements, interconnect quality typically determines maximum bandwidth; for low current measurements, it often affects measurement speed and accuracy. This application note discusses the problems created by poor connections. Although it specifically addresses MOSFET measurements, the techniques and results discussed also apply to many other devices.

V_{DS}–I_{DS} curves

The most straightforward way to assess a MOSFET's overall performance is to take V_{DS}–I_{DS} curves for a set of gate voltages because these curves define the operating regions of the device. Pulsed I-V characterization, wherein voltages and currents are applied for a very short time and at a limited duty cycle, is a common way to measure these curves. Pulsed I-V measurements can reduce test times and allow characterizing a device without exceeding its safe operating area or causing device self-heating and the associated parameter shifts.

Two pulsed I-V channels are typically used to measure these curves on a MOSFET, with one connected to the gate and the other to the drain. The ground of each channel is connected to the MOSFET source pin.

To construct the transistor curves, the gate channel first applies voltage to the gate, then the drain channel sweeps V_{DS} through a range of values, measuring the resulting current at each point. Next, the gate channel applies a different voltage to the gate and the process repeats, constructing the next transistor curve in the set.

Modern pulse instruments can produce very short voltage pulses (100ns or less) with rise times as fast as 20ns, so wide bandwidth is critical to obtaining good measurements. For optimal performance, both pulse generator channels should be connected with coaxial cables matched to the generator's 50Ω output impedance. However, it is impossible to maintain 50Ω impedance all the way to a device on a wafer in practice; at some point, the ground must be connected to one pin and the signal to another, breaking 50Ω characteristic impedance (***Figure 1***). Minimizing the length of these non-coaxial ground and signal connections is crucial.

Figures 2a and ***2b*** illustrate how inadequate grounding and coaxial cabling can produce erroneous data when

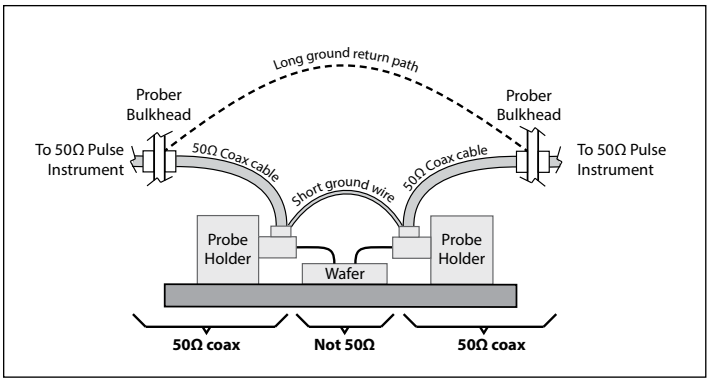

Figure 1. Prober hookups usually do not maintain 50W all the way to the DUT. If the short ground wire is not used, the much longer ground return path will limit bandwidth.

characterizing a MOSFET using pulses with 20ns rise times, 20ns fall times, and a width of 200ns. ***Figure 2a*** shows data taken with 100W impedance triaxial cables and 1–2 ft. ground connections. ***Figure 2b*** shows data taken with 50Ω impedance coaxial cables and ground connections just a few inches long. The difference is striking: the data from an improperly cabled system are compressed (***Figure 2a***), measuring about half the level expected, while the data from the correctly cabled system (***Figure 2b***) match conventionally measured data.

Maximum g_m and V_{TH}

Transconductance (g_m) is a critical parameter widely used to determine the threshold voltage (V_{TH}) of MOSFETs [1]. Pulsed I-V testing is ideal for this application because these parameters can be determined without violating safe operating area (SOA) limits or damaging the device.

For a small signal analysis about a given gate and drain bias point, g_m is defined as:

$$g_m = \frac{\partial i_{DS}}{\partial V_{GS}} \quad g_m = \frac{\partial i_{DS}}{\partial V_{GS}} \tag{1}$$

When measuring gm, the same connection scheme used to obtain the data in ***Figures 2A*** and ***2B*** is used, but this time a DC voltage is applied to the drain while the gate voltage (V_{GS}) is swept over the voltage range that transitions the device from off to on. Because the connections and pulsing speeds are the same, the earlier bandwidth discussion applies to g_m and V_{TH} testing as well.

Figures 3a and ***3b*** show the results of another example of g_m and V_{TH} measurement, with the data shown in each taken with the same pulse rise and fall times, pulse widths, connections, and grounding. As Eq. 1 states, calculating gm requires

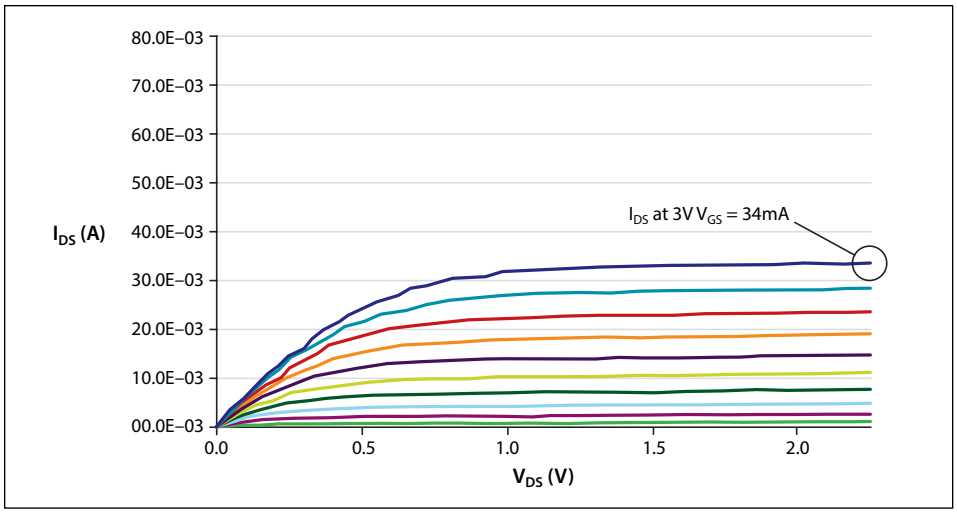

Figure 2A. MOSFET curves with poor cabling and grounding. I_{DS} at a V_{GS} of 3V is measured as 34mA.

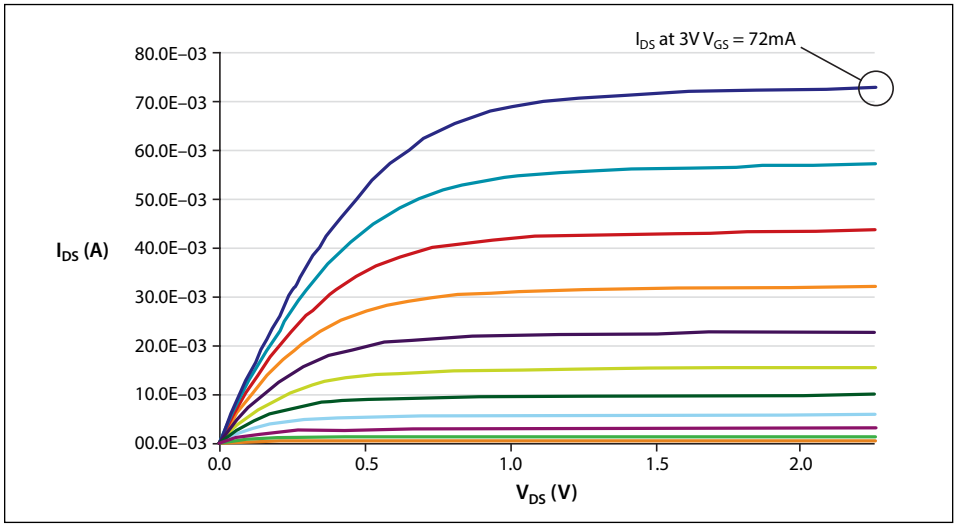

Figure 2B. MOSFET curves with optimal cabling and grounding. I_{DS} at a V_{GS} of 3V is measured as 72mA.

computing the first derivative of the drain current with respect to the gate voltage. The blue curve is the drain current and the red curve is its calculated derivative.

Just as with the V_{DS}–I_{DS} curves, the difference is significant. The results produced using the improperly cabled setup would mislead the user to think the DUT's gm is half its actual value and its V_{TH} roughly 200mV higher than it actually is.

Capacitance-Voltage Testing

Capacitance-voltage (C-V) measurements are often used to characterize a MOSFET's gate oxide thickness, oxide defect density, doping profiles, etc. In this measurement, as the gate voltage varies, the capacitance of the gate to the drain and source changes. The Model 4210-CVU option allows Keithley's Model 4200-SCS Parameter Analyzer to make 1kHz–10MHz C-V measurements. It has four terminals wired to two device connections: CVU high and CVU low. In a standard C-V measurement, the source, bulk, and drain of a MOSFET are connected together and tied to CVU low; the gate is connected to CVU high. The Model 4210-CVU applies a DC bias and a small AC voltage to bias the transistor and simultaneously measure its capacitance, returning capacitance values for a wide range of bias voltages.

C-V measurements can be made at many frequencies (sometimes greater than 1MHz), depending on the parameters to be extracted. At higher frequencies, transmission line effects and cable length can impact measurement integrity significantly. For optimal C-V measurements, DUTs must be connected to the instrumentation using coaxial cables of the proper length and impedance level; for example, the Model 4210-CVU uses 1.5-meter, 100Ω cables.

Although using cables longer than those provided with the instrument will cause large changes in data at high frequencies, a feature known as cable length compensation can mitigate this problem. Using cables of different characteristic impedances, such as when coaxial cables are improperly adapted to triaxial cables, will also produce increased measurement error at high frequencies.

Off-State Leakage

Characterizing off-state leakage is critical to understanding quiescent power dissipation and transistor quality for small-scale parameter transistors. A source measure unit (SMU) instrument capable of measuring picoamp-level (1E–12A) currents is essential.

As with any low current measurement, properly guarded triaxial cables are essential. Using coaxial cables will produce erroneous results due to high cable capacitance (50Ω coaxial cables typically have 30pF of capacitance per foot). This capacitance must be charged with high currents before small currents flowing in the DUT can be measured, extending settling times substantially.

Triaxial cables alleviate this problem by providing a third conductor between the center pin and shell, called the guard, driven at the same potential as the center pin. The guard conductor drastically reduces the effective capacitance and reduces settling times. Never use poor-quality triaxial cables, which can introduce problematic dielectric absorption, triboelectric effects, or high noise. Unguarded cable segments should be minimized. For best performance, triaxial cables should be run as close to the DUT as possible.

Match the Cable to the Measurement

As these examples illustrate, matching cabling and grounding to the measurement type enhances measurement integrity. However, changing cables for each measurement type is so time-consuming many users simply tolerate the suboptimal results. Moreover, whenever cables are rearranged, users run the risk of reconnecting them improperly, thereby causing errors and demanding extra troubleshooting time. Worse still, these errors may go unnoticed for a long time.

One alternative is to use a remote switch capable of handling I-V, C-V and pulsed I-V signals, such as Keithley's Model 4225-RPM Remote Amplifier/Switch. When combined with a multi-measurement performance cable kit, such as Keithley's 4210-MMPC kit, it can often eliminate the need to recable between tests. This kit delivers the correct impedance and cable type, allowing low current, high speed pulse, and C-V measurements with no manipulator reconnection, eliminating the need to reprobe wafers.

Given the importance of characterizing semiconductor devices quickly and accurately, the value that the latest cable solutions can provide to device researchers is obvious.

References

1. X. Zhou, K. Y. Lim, and D. Lim. A Simple and Unambiguous Definition of Threshold Voltage and Its Implications in Deep-Submicron MOS Device Modeling. IEEE Transactions on Electron Devices, Vol 46, No. 4, p. 807. April 1999.

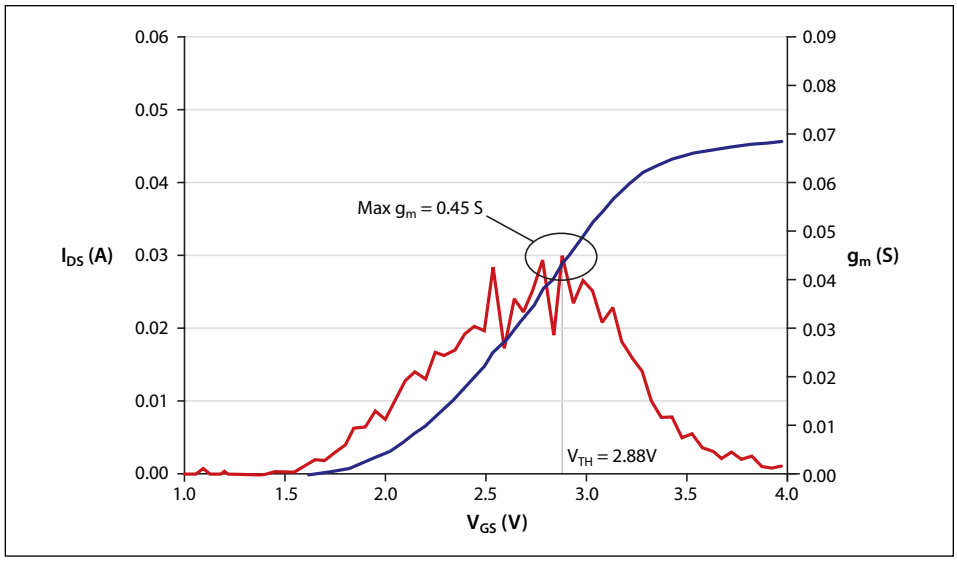

Figure 3a. g_m test with poor cabling and grounding.

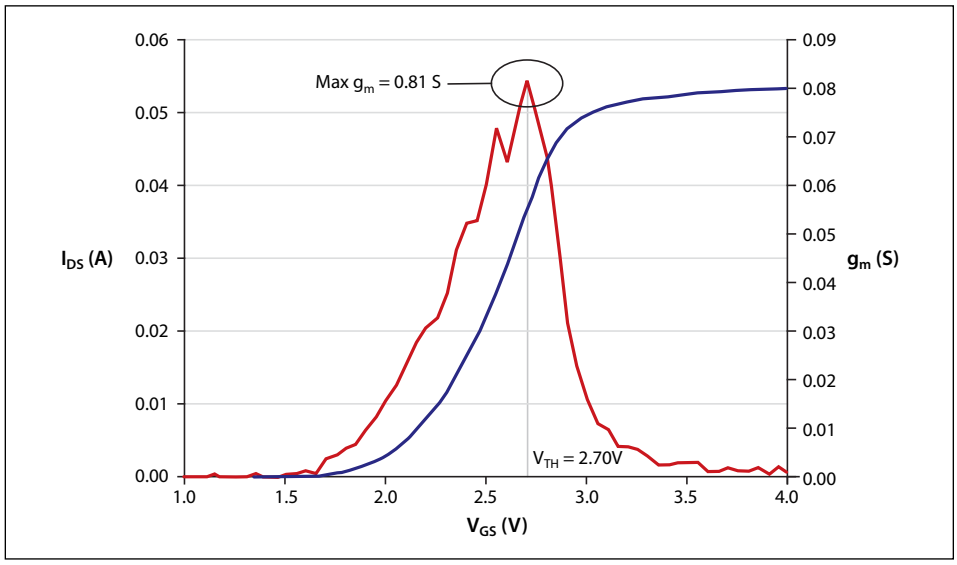

Figure 3b. g_m test with optimal cabling and grounding. From this measurement, g_m is 0.81 S and V_{TH} is 2.70V.

An Ultra-Fast Single Pulse (UFSP) Technique for Channel Effective Mobility Measurement

Introduction

The channel effective mobility (μ_{eff}) influences the MOSFET performance through the carrier velocity and the driving current. It is one of the key parameters for complementary metal-oxide-semiconductor (CMOS) technologies. It is widely used for benchmarking different processes in technology development and material selection [1, 2]. It is also a fundamental parameter for device modelling [3]. With device scaling down to Nano-size regime and the introduction of new dielectric materials, conventional measurement technique for mobility evaluation encountered a number of problems described in the following section, leading to significant measurement errors. As a result, a new mobility extraction technique is needed.

This application note describes a novel Ultra-Fast Single Pulse technique (UFSP) [4, 5] for accurate mobility evaluation, including the technique principle, how to connect the device, and how to use the provided software in the Model 4200-SCS Parameter Analyzer.

Conventional Mobility Measurement and Challenges

We use a p-channel device of gate length L and width W as an example. When the channel charge is fairly uniform from source to drain in the linear region, the channel effective mobility (μ_{eff}) can be written as

$$\mu_{eff} = \frac{L}{W} \cdot \frac{I_{cb}}{Q_i \cdot V_d} \quad (1)$$

where V_d is a small bias applied on the drain terminal of the device, Q_i is the mobile channel charge density (C/cm^2), and I_{ch} is the conduction current flowing in the channel.

Traditionally, I_{ch} is measured at the drain terminal of the device with the configuration shown in ***Figure 1(a)***. Q_i is extracted from integrating the measured gate-to-channel capacitance, C_{gc}, with respect to V_g, i.e.,

$$Q_i = \int_{+\infty}^{V_g} C_{gc}\, \mathrm{d}V_g$$

by using the connection configuration shown in ***Figure 1(b)***.

The principle of conventional mobility measurement is deceptively simple. However, many challenges and pitfalls are associated with this testing. Several sources of error are often ignored in the past.

Vd-dependence: The conventional technique applies a non-zero V_d (usually 50mV–100mV) for I_{ch} measurement but a zero V_d for Q_i measurement. This difference in V_d used in two measurements can lead to significant errors in evaluating mobility for thin oxides, especially in the low electric field region. One example is given in ***Figure 2***, where a higher $|V_d|$ results in a substantial reduction of mobility near its peak. This is because $|V_g–V_d|$ reduces for high $|V_d|$, so that the real charge carrier density for the I_{ch} is smaller than the Q_i measured at $V_d = 0$.

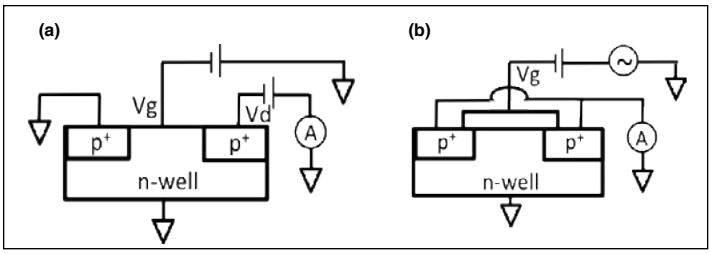

Figure 1. Configuration for (a) conduction current measurement and (b) gate-to-channel capacitance, C_{gc}, measurement.

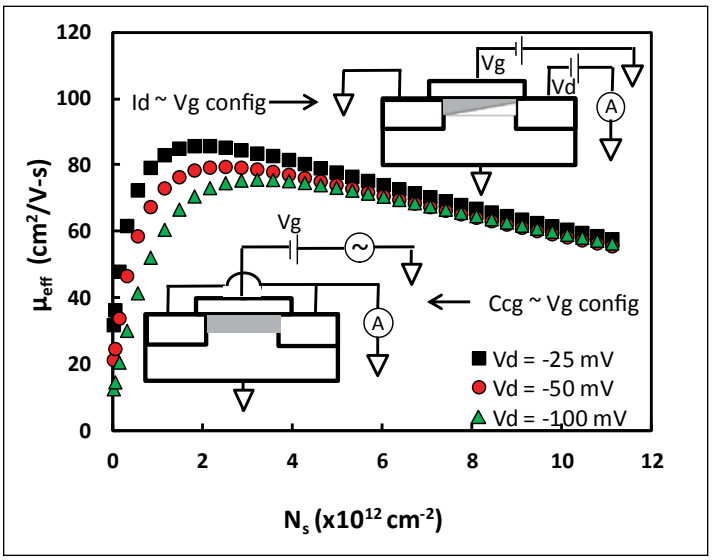

Figure 2. Effective channel mobility measured by conventional technique. I_{ch} was measured under various non-zero drain biases, V_{DS}, but Q_i was measured under $V_d = 0$. The extracted mobility clearly reduces for higher $|V_d|$. Insets illustrate the carrier distribution in the channel.

Charge trapping: The conventional technique used slow measurement with typical measurement time in seconds. The fast charge trapping becomes significant for both thin SiON and high-k dielectric. For slow measurements, trapping can respond during the measurement and give rising to hysteresis and stretch-out of the $C_{gc}–V_g$ curve and a reduction of I_{ch}. This results in an underestimation of mobility.

Leaky dielectric: As gate oxide downscales, high gate leakage current becomes a main challenge for mobility extraction. It affects both I_{ch} and Q_i measurements and in turn the mobility. To minimize its impact on C_{gc} measurement, frequency up to gigahertz has been used, which requires devices with RF structure. The RF structure requires more processing and die space and is not always available.

Cable switching: The conventional technique involves cable changing between I_{ch} and Q_i measurements. This slows down the measurement and can potentially cause breakdown of the device under test.

The Ultra-Fast Single Pulse Technique (UFSP Technique)

To overcome the challenges mentioned above, a novel technique called the Ultra-Fast Single Pulse technique (UFSP) is developed and described below.

A p-channel device is used here for illustrating the working principle of the UFSP technique as shown in ***Figure 3***. The considerations for n-channel devices are similar. To perform the UFSP measurement, a single pulse with edge time of several micro-seconds is applied on the gate terminal of the device. The gate voltage sweeps toward negative during the falling edge of the pulse and turns the device on. The transient currents are recorded at both the source and the drain terminal of the device. The device is then switched off during the subsequent rising edge where gate voltage are swept toward positive. The corresponding transient currents are also to be recorded. Channel effective mobility can be extracted from these four transient currents measured within several micro-seconds.

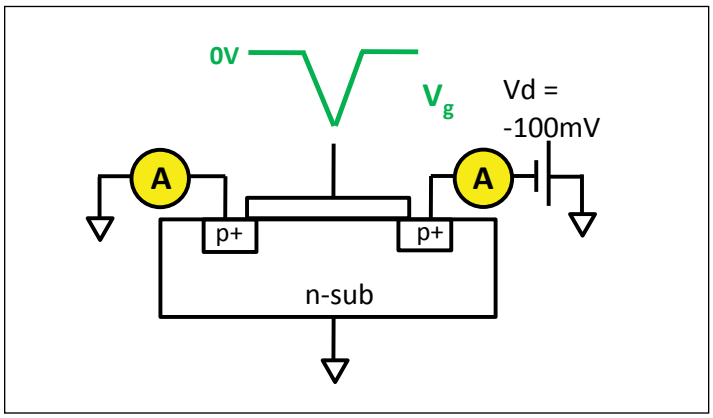

Figure 3. Illustration of the working principle of UFSP technique.

To facilitate the analysis, we define currents measured at drain and source terminal during switching on and off as I_d^{on}, I_s^{on}, I_d^{off}, and I_s^{off}. The current flow in the channel during the transient measurement is shown in ***Figure 4 (a)*** and ***(b)***. Three types of current are present: channel conduction current, I_{ch}, displacement current between gate and source/drain, I_{dis_s} and I_{dis_d}, and the leakage current between gate and source/drain, I_{g_s} and I_{g_d}. When device is switched off-to-on, the direction of I_{dis_s} and I_{dis_d} is toward the channel centre: I_{dis_s} has the same

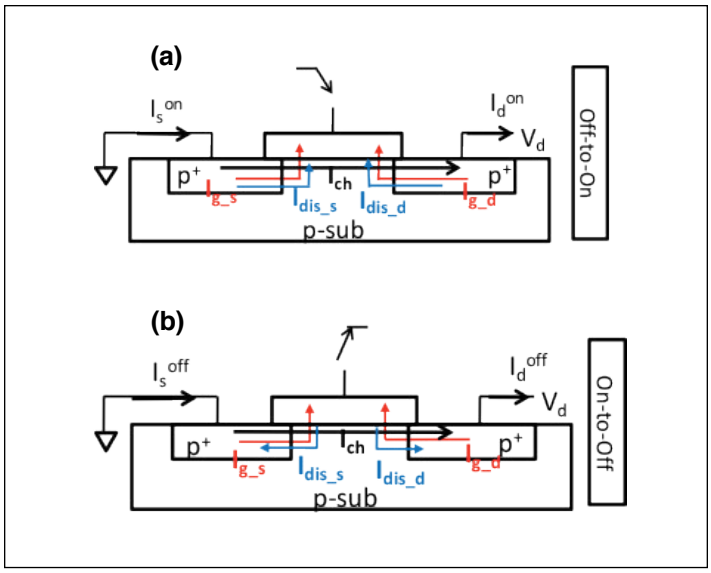

Figure 4. Schematic diagram of current flow during the transient measurement.

direction as I_{ch} at the source, but I_{dis_d} is in opposite direction to I_{ch} at the drain. When device is switched on-to-off, I_{dis_s} and I_{dis_d} change direction, but Ich does not. I_{g_s} and I_{g_d} are independent of V_g sweep direction and always flow from the source and drain towards gate under negative V_g. Based on the above analysis, channel current, I_{ch}, gate current, I_g, and displacement current, Idis can be separated by using Equations (2)–(4). C_{gc} can be calculated using (5).

$$I_{CH} = \frac{I_D^{ON} + I_D^{OFF} + I_S^{ON} + I_S^{OFF}}{4} \quad (2)$$

$$I_G = I_{G_S} + I_{G_D} = \frac{I_S^{ON} + I_S^{OFF} - I_D^{ON} - I_D^{OFF}}{2} \quad (3)$$

$$I_{DIS} = I_{DIS_S} + I_{DIS_D} = \frac{I_D^{OFF} - I_D^{ON} + I_S^{ON} - I_S^{OFF}}{2} \quad (4)$$

$$C_{GC} = \frac{I_{DIS}}{dV_G/dt} \quad (5)$$

To calibrate the UFSP technique, a p-channel MOSFET with thick oxide is used which has negligible I_G current. The measurement time (=edge time) is set at 3μs. the measured four currents are shown in ***Figure 5***. The extracted I_{ch}, I_g and C_{gc} by using Equations (2) to (5) are shown in ***Figure 6(a)***. Once C_{gc} and I_{ch} are evaluated accurately, Qi can be obtained by integrating C_{gc} against V_g and channel effective mobility, μeff, is calculated through Equation (1) as shown in ***Figure 6(b)***.

Since the UFSP measured I_{ch} and C_{gc} under the same V_d, μ_{eff} should be independent of V_d. The μ_{eff} evaluated under three different V_d biases is compared in ***Figure 7***. Good agreements are obtained confirming the errors induced by V_d for the conventional techniques has been removed.

The UFSP also works well on leaky gate dielectric of standard structure. When it was applied on one 'leaky' n-channel MOSFET with an EOT of 1.28nm, the four currents measured from the

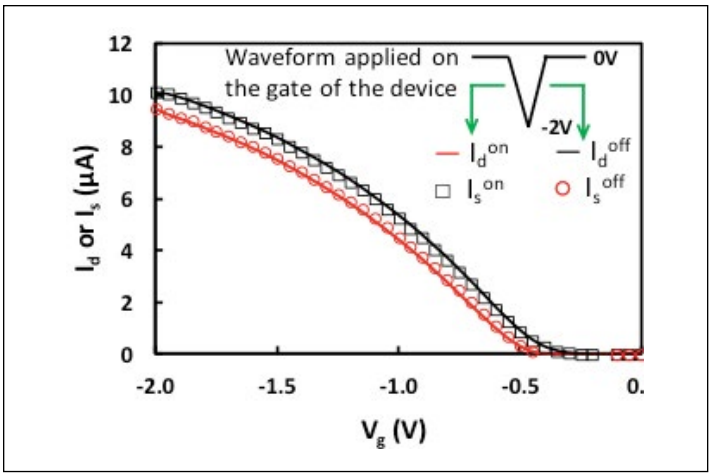

Figure 5. Four currents measured from source and drain corresponding to the off-to-on and on-to-off Vg sweep. Schematic Vg waveform is shown in inset.

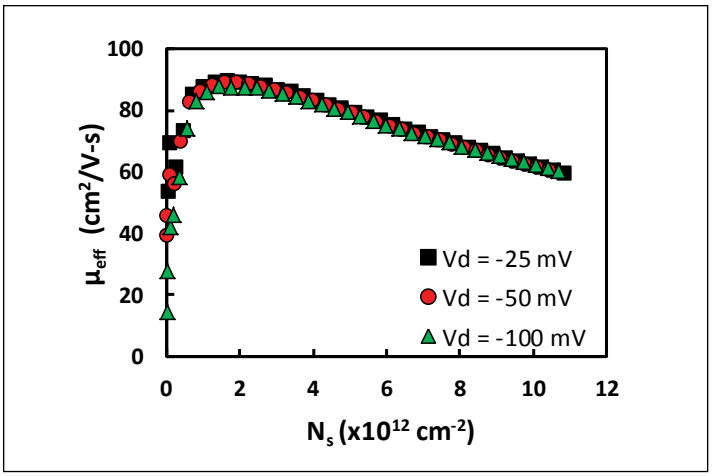

Figure 7. The effective channel mobility, μ_{eff}, extracted under three different V_d by using UFSP technique.

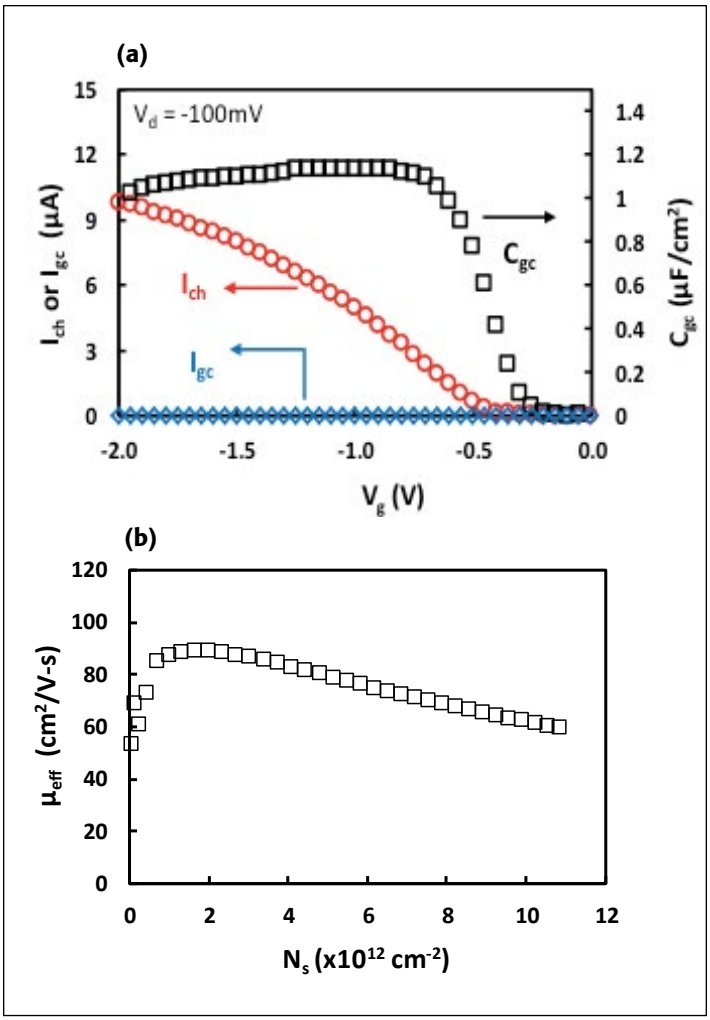

Figure 6.

(a). I_{ch}, I_g, and C_{gc} extracted simultaneously from the currents in Figure 5 by using Equations (2)–(5).

(b) Channel effective mobility extracted from I_{ch} and C_{gc} from (a).

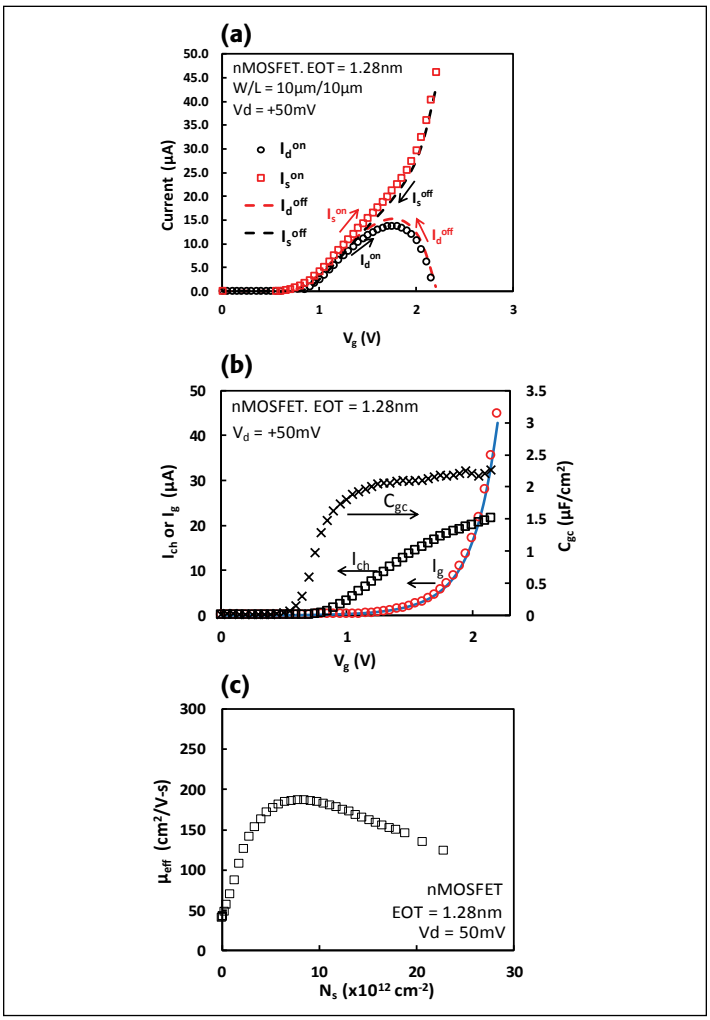

Figure 8.

(a) Four currents measured from the source and drain corresponding to the off-to-on and on-to-off V_g sweeps by UFSP technique on an nMOSFET with EOT of 1.28nm.

(b) I_{ch} ('□'), I_g ('o') and C_{gc} ('x') are extracted from the currents in (a) with Equations (2)-(5). The blue line is the leakage current obtained by DC measurement.

(c) Channel effective mobility, μeff, is calculated by using the extracted Ich and C_{gc} with Eqn (1).

source and drain terminals corresponding to the off-to-on and on-to-off V_G sweep are shown in ***Figure 8(a)***. By using Equations (2)–(5), I_{ch} ('□'), I_g ('o') and C_{gc} ('x') are extracted and plotted in ***Figure 8(b)***. I_g from DC measurement is also plotted for comparison in ***Figure 8(b)***. Good agreement is obtained. ***Figure 8(c)*** shows that electron mobility can be reliably measured for this leaky device where I_g is as high as 45A/cm². Since the UFSP can tolerate high gate leakage, it does not need using the special RF structure for mobility evaluation.

To demonstrate the applicability of UFSP to devices with significant charge trapping, one pMOSFET with HfO_2/SiO_2 stack was used. Large amount of traps locate close to the Si/SiO_2 interface in this dielectric stack and they can exchange charges with substrate rapidly. The conventional technique takes seconds, making them indistinguishable from channel mobile charges. As a result, inversion charges will be overestimated and in turn the channel effective mobility will be underestimated. The UFSP technique only takes microseconds, minimizing charge trapping effect. ***Figure 9*** compares the mobility extracted by these two techniques. It clearly shows that after suppressing the trapping, the mobility extracted from the UFSP is considerably higher than that by the conventional technique.

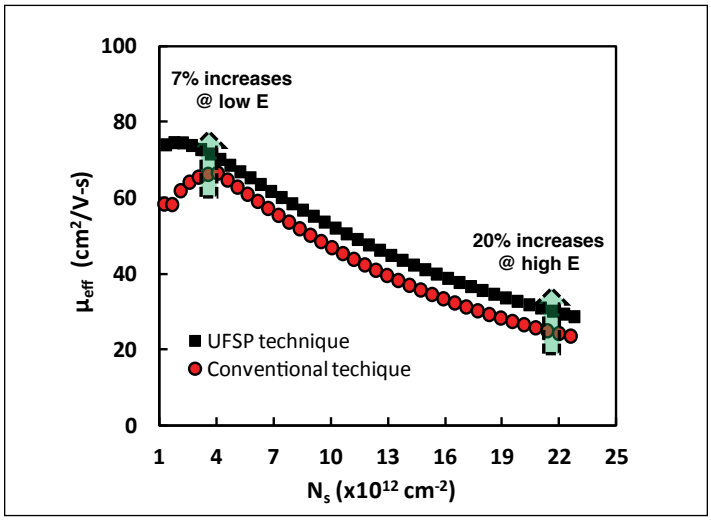

Figure 9. A comparison of mobility extracted by UFSP and conventional technique for a device with HfO_2/SiON dielectric of considerable fast trapping.

Required Hardware for UFSP Measurement

Selecting appropriate measurement equipment is critical to the success implementation of ultra-fast single pulse method. The following hardwares are required: Two Keithley Ultra-Fast I-V Modules (4225-PMU);

- Two Keithley Ultra-Fast I-V Modules (4225-PMU);
- Four Remote Amplifier/Switch (4225-RPM);
- 4 sets of high Performance Triaxial Cable Kit (4210-MMPC-C).

A photo of the cabling configuration for the test is shown in ***Figure 10***. 4225-PMU is the latest addition to the growing range of instrumentation options for the Model 4200-SCS

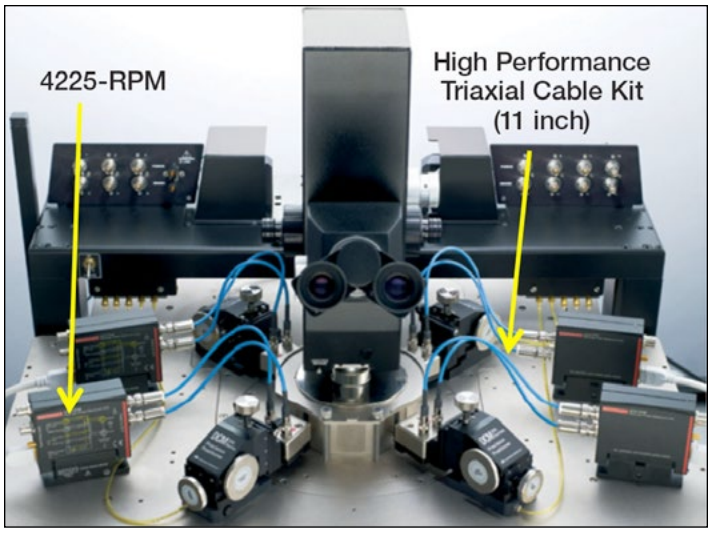

Figure 10. Photo of the UFSP technique setup using Keithley instruments.

Parameter Analyzer. The module integrates ultra-fast voltage waveform generation and signal observation capabilities into the Model 4200-SCS's already powerful test environment to deliver unprecedented I-V testing performance. It makes ultra-fast I-V sourcing and measurement as easy as making DC measurements with a traditional high resolution source measure unit (SMU) instrument. Each plug-in Model 4225-PMU module provides two channels of integrated sourcing and measurement. Each channel of the Model 4225-PMU combines high speed voltage outputs (with pulse widths ranging from 60 nanoseconds to DC) with simultaneous current and voltage measurements. 4225-RPM Remote Amplifier/Switch further expands the Model 4225-PMU's capabilities by providing ultra-low current measurement (below 100 nA) and reducing cable capacitance effects.

Connections to the Device

The connection for the UFSP measurement is shown in ***Figure 11***. Each terminal of the device is connected to one 4225-RPM using two 11-inch blue cables (provided in the cable set 4210-MMPC-C). Then each 4225-RPM is connected to one channel of PMU using two triaxial cables. All the measurements are controlled by the Keithley KTEI software.

Using the KTEI Software to Perform UFSP measurement

Performing UFSP for channel effective mobility measurement using Keithley 4200-SCS system is quite simple. One example project can be downloaded from http://www.keithley.com/data?asset=57747. As shown in ***Figure 12***, each terminal of the device is connected to one channel of PMU. Users can modify the parameters for each PMU channel in the definition tab. ***Table 1*** lists one set of user-defined parameters for a p-channel MOSFET.

In the timing tab, users can input the desired measurement speed which is the edge time of the pulse. The recommended values are listed in ***Table 2***.

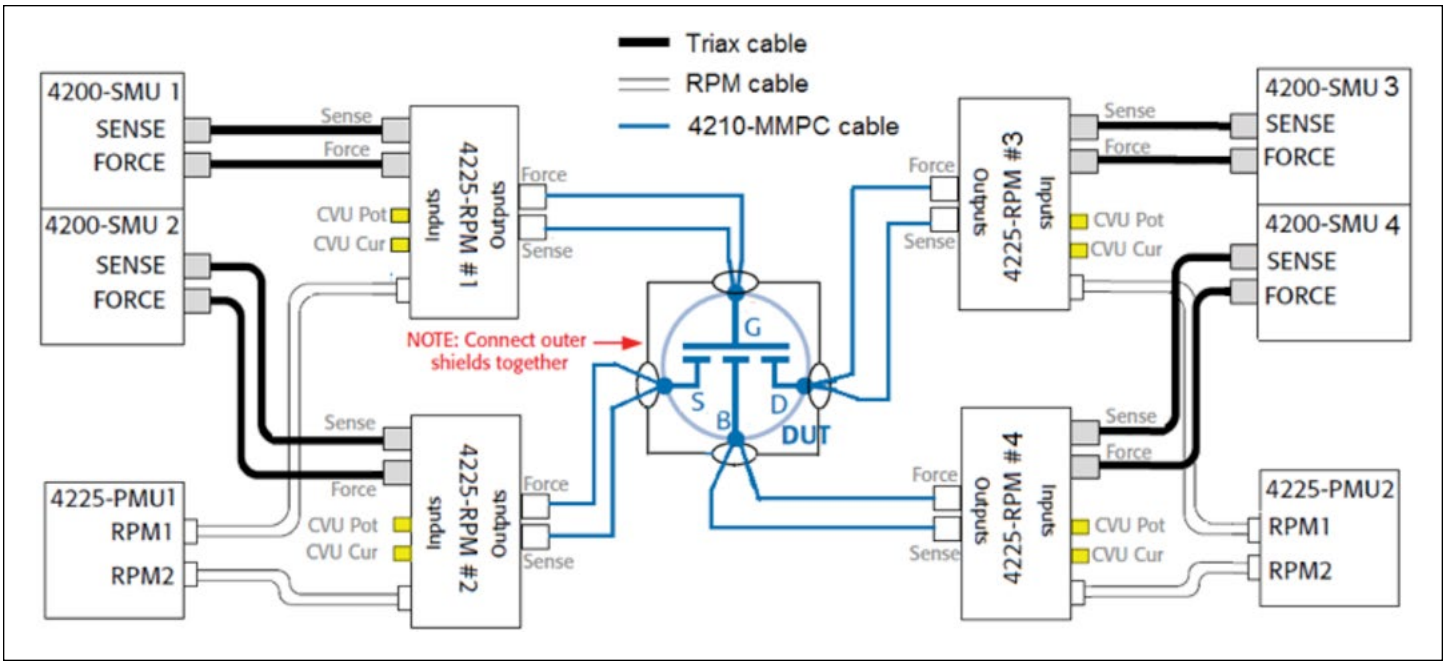

Figure 11. Experiment connection for the Ultra-fast Single Pulse (UFSP) technique. Two Keithley dual-channel 4225-PMUs are used for performing transient measurements. Four Keithley 4225-RPMs are used to reduce cable capacitance effect and achieve accurate measurement below 100nA.

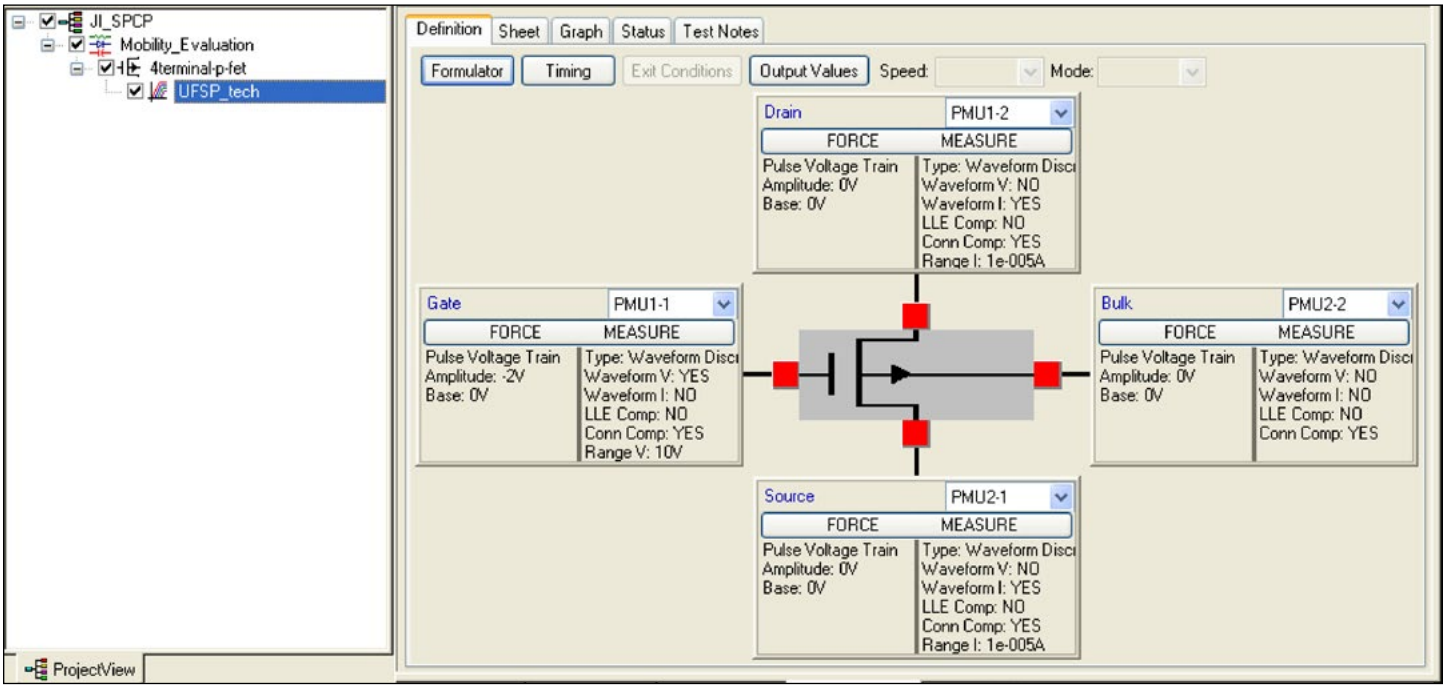

Figure 12. Example project in KTEI software for UFSP measurement. Each of the four terminals of the device is connected to one channel of PMU respectively.

Table 1. Recommended setting in the definition tab for each channel of PMU.

PMU Setting for Gate Terminal			
Parameters		**Value**	**Description**
Pulse Train Settings	Forcing Function	Pulse Train	To generate a single pulse or a pulse train with same shape
	Voltage Amplitude	–2V	To define the Vg sweep range
	Voltage Base	0V	
Measurement Range	Vrange	10V	Maximum possible voltage applied on the gate
	Irange	10µA	Measurement range for current
Measurement Setting	Sample I waveform	untick	Do not record current at the gate
	Sample V waveform	tick	Record applied voltage at the gate
	Timestamp	tick	Record total time for the measurement

PMU Setting for Drain Terminal			
Parameters		**Value**	**Description**
Pulse Train Settings	Forcing Function	Pulse Train	To generate a single pulse or a pulse train with the same shape
	Pulse Train Settings	DC voltage	To apply a constant Vd bias used for mobility measurement
	Voltage base (V)	–0.1	
Measurement Range	Vrange	10V	Maximum possible voltage applied on the gate
	Irange	10µA	Measurement range for current
Measurement Setting	Sample I waveform	tick	Record current at the drain
	Sample V waveform	untick	Do not record applied voltage at the drain
	Timestamp	untick	Do not record total time for the measurement

PMU Setting for Source Terminal			
Parameters		**Value**	**Description**
	Forcing Function	Pulse Train	To generate a single pulse or a pulse train with the same shape
	Pulse Train Settings	DC voltage	To apply a zero Vs bias used for mobility measurement
	Voltage base (V)	0	
Measurement Range	Vrange	10V	Maximum possible voltage applied on the gate
	Irange	10µA	Measurement range for current
Measurement Setting	Sample I waveform	tick	Record current at the source
	Sample V waveform	untick	Do not record applied voltage at the source
	Timestamp	untick	Do not record total time for the measurement

PMU Setting for Bulk Terminal			
Parameters		**Value**	**Description**
	Forcing Function	Pulse Train	To generate a single pulse or a pulse train with the same shape
	Pulse Train Settings	DC voltage	To apply a zero Vbulk bias used for mobility measurement
	Voltage base (V)	0	
Measurement Setting	Sample I waveform	untick	Do not record current at the bulk
	Sample V waveform	untick	Do not record applied voltage at the bulk
	Timestamp	untick	Do not record total time for the measurement

Table 2. Recommended setting in the timing tab.

Parameters	Value	Description
Test Mode	Waveform capture	
Measurement Mode	Discrete Pulses	Discrete Pulse and Average pulses, then you need to input number of Pulses, 10 is enough.
Sweep parameter	None	No sweeping required
Period (s)	5.00E-05	Period of the pulse
Width (s)	6.00E-06	Pulse width
Rise Time (s)	3.00E-06	Pulse rise time
Fall Time (s)	3.00E-06	Pulse fall time, set to be the same as rise time
Pulse Delay (s)	2.00E-06	Pulse delay time, keep the same as rise time

Once the test is executed, transient currents during switching on and off at source and drain terminals will be recorded and stored in the sheet tab and can be saved as an .xls file. These currents can also be plotted on the graph tab. From these currents, the channel effective mobility can be extracted based on Equations (2) to (5).

Conclusion

Channel carrier mobility is a key parameter for material selection and process development. The conventional technique suffers from several shortcomings: slow speed and vulnerability to fast trapping, V_d-dependence, cable-changing, sensitivity to gate leakage, and complex procedure. An ultra-fast single pulse technique (UFSP) has been proposed and developed to overcome these shortcomings. I_{CH} and Q_i can be simultaneously measured within several micro-seconds without cable switching. UFSP measurement can be easily performed using the Keithley 4200-SCS Parameter Analyzer with four 4225-RPMs. It provides a complete solution for robust and accurate mobility evaluation in a convenient way and serves as a tool for process development, material selection, and device modelling for CMOS technologies.

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1. P. R. Chidambaram, C. Bowen, S. Chakravarthi, C. Machala, and R. Wise, "Fundamentals of silicon material properties for successful exploitation of strain engineering in modern CMOS manufacturing," IEEE Trans. Electron Dev., vol. 53, no. 5, pp. 944-964, 2006.
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3. K. Chain, J. Huang, J. Duster, K. K. Ping, and C. Hu, "A MOSFET electron mobility model of wide temperature range (77 - 400 K) for IC simulation," Semiconductor Science and Technology, vol. 12, no. 4, pp. 355, 1997.
4. Z. Ji, J. F. Zhang and W. Zhang, "A New Mobility Extraction Technique Based on Simultaneous Ultrafast Id-Vg and Ccg-Vg Measurements in MOSFETs," IEEE Trans. Electron Dev., vol. 59, no. 7, pp. 1906, 2012.
5. Z. Ji, J. Gillbert, J. F. Zhang and W. Zhang, "A new Ultra-Fast Single Pulse technique (UFSP) for channel effective mobility evaluation in MOSFETs," IEEE Int. Conf. Microelectronic Test Structures, pp. 64, 2013.

Acknowledgements

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Performing Charge Pumping Measurements with the Model 4200-SCS Parameter Analyzer

Introduction

Charge pumping (CP) is a well-known measurement technique for analyzing the semiconductor–dielectric interface of MOS structures. Important information about the quality and degradation of a device can be extracted from charge pumping current (I_{CP}) measurement results, including the interface trap density and the mean capture cross section. Pulsing a gate voltage and measuring a DC substrate current simultaneously is the basis for the various charge pumping methods, so a pulse generator and sensitive DC ammeter are required to make these measurements.

The Model 4200-SCS Parameter Analyzer offers a complete solution for charge pumping measurements because it contains the necessary hardware to make the sensitive measurements, as well as software to automate the measurements and analyze the results. This system is provided with predefined tests for making most of the common charge pumping tests, such as a pulsed base voltage sweep or a pulsed voltage amplitude sweep. This application note explains how to make charge pumping measurements using the Model 4200-SCS with the optional Model 4225-PMU Ultra Fast I-V Module (PMU) or Model 4220-PGU Pulse Generator Unit (PGU).

Charge Pumping Overview

Figure 1 is a charge pumping measurement circuit diagram. Basically, the gate of the MOSFET is connected to a pulse generator, which repeatedly switches the transistor from accumulation to inversion. While the gate is pulsed, a recombination process of majority/minority carriers occurs on the rising and falling edges of the pulses. This causes a current to flow in the opposite direction of the normal drain-to-source current. This induced current is known as the charge pumping current (I_{CP}) and can be measured by connecting a sensitive ammeter to the substrate, or bulk terminal, of the MOSFET.

Although several charge pumping methods have been developed, the basic charge pumping technique involves measuring the substrate current while applying voltage pulses of fixed amplitude, rise time, and frequency to the gate of the transistor. The source and drain are either tied to ground or slightly reverse-biased. The voltage pulse can be applied with a fixed amplitude while sweeping the base voltage or with a fixed base voltage while sweeping the amplitude of the pulse.

In the fixed-amplitude/voltage-base sweep, the amplitude and period (width) of the pulse are kept constant while the base voltage is swept from inversion to accumulation. This waveform

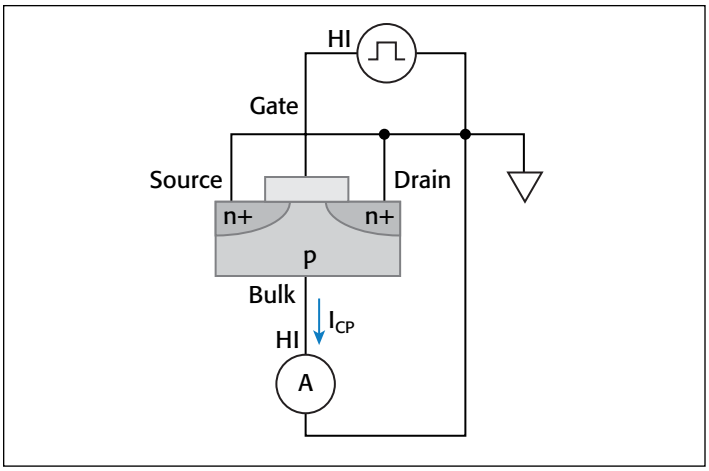

Figure 1. Basic charge pumping measurement circuit

and the corresponding curve of the charge pumping current shown as a function of the base voltage are both illustrated in ***Figure 2***. From the data, it's possible to extract the interface trap density (N_{it}) using this equation:

$$N_{it} = \frac{I_{CP}}{qfA}$$

where:

N_{it} = interface trap charge density (cm^{-2})

I_{CP} = charge pumping current (A)

f = test frequency (Hz)

q = electron charge, 1.6022×10^{-19} C

A = channel area (cm^2)

The interface trap density as a function of band bending can also be extracted from the following equation:

$$D_{it} = \frac{I_{CP}}{qfA\Delta E}$$

where:

D_{it} = interface trap charge density ($cm^{-2}eV^{-1}$)

I_{CP} = charge pumping current (A)

f = test frequency (Hz)

q = electron charge, 1.6022×10^{-19} C

A = channel area (cm^2)

ΔE = the difference between the inversion Fermi level and the accumulation Fermi level [1]

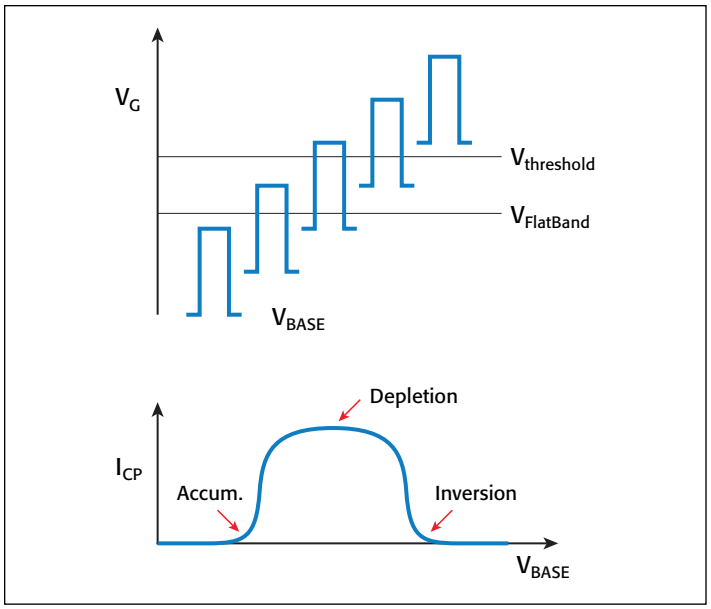

Figure 2. Pulse waveform for fixed-amplitude/voltage-base sweep and corresponding charge pumping current curve

The fixed-base/variable-amplitude sweep method is another common technique for determining the charge pumping current. With this method, the base voltage is kept constant in accumulation and the variable voltage amplitude is pulsed into inversion. As shown in ***Figure 3***, as the voltage amplitude (V_{AMP}) of the pulses increases, the charge pumping current saturates and stays saturated.

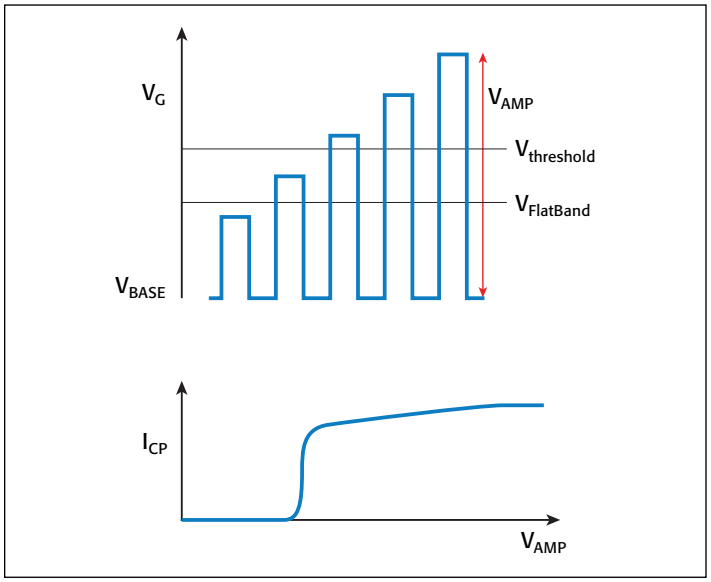

Figure 3. Pulse waveform for fixed-base/variable-amplitude sweep with corresponding charge pumping current curve

Other charge pumping techniques are used in addition to the fixed-amplitude/variable-base sweep and the fixed-base/variable-amplitude sweep. In some cases, the voltage waveform can have various shapes, the rise and fall times can be varied, or the charge pumping current can be measured as a function of frequency.

Hardware Configuration

Figure 4 is the basic circuit diagram for making charge pumping measurements using the Model 4200-SCS. For this application, the Model 4200-SCS is configured with either a Model 4220-PGU Pulse Generator Unit (PGU) or a Model 4225-PMU Ultra Fast I-V Module (PMU), one or two Model 4200-SMU Source Measure Unit (SMU) Instruments, and one Model 4200-PA Preamp.

The pulser (4225-PMU or 4220-PGU) is connected to the gate of the MOSFET in order to apply pulses of sufficient amplitude to drive the device between inversion and accumulation. Depending on the charge pumping method, the PGU or PMU can sweep the pulse amplitude, sweep the base voltage, vary the rise/fall time, and vary the test frequency. The test frequency is usually in the kilohertz to megahertz range.

SMU1 is connected to the Bulk terminal and measures the resulting substrate current. This charge pumping current (I_{CP}) is often in the nanoamp or picoamp range. For measuring currents of less than one nanoamp, the optional Model 4200-PA should be used.

The source and drain terminals of the MOSFET are tied together and connected to SMU2, which applies a slight reverse-bias (V_r). If $V_r = 0$, then the source/drain terminals can be connected to the ground unit (GNDU) instead of to SMU2. To prevent oscillations and minimize noise, it is very important to connect the LO (common) terminals of all the SMU instruments and the pulser (4225-PMU or 4220-PGU) as close as possible to the device. The LO terminal of the SMU instrument is the outside shell of the triax connector. The LO terminal of the PMU and PGU is the outside shield of the SMA cable.

To minimize noise in low current measurements due to electrostatic interference, make sure the device is shielded by placing it in a metal enclosure with the shield connected to the LO terminal of the SMU instrument. Further information on making low current measurements with the Model 4200-SCS is

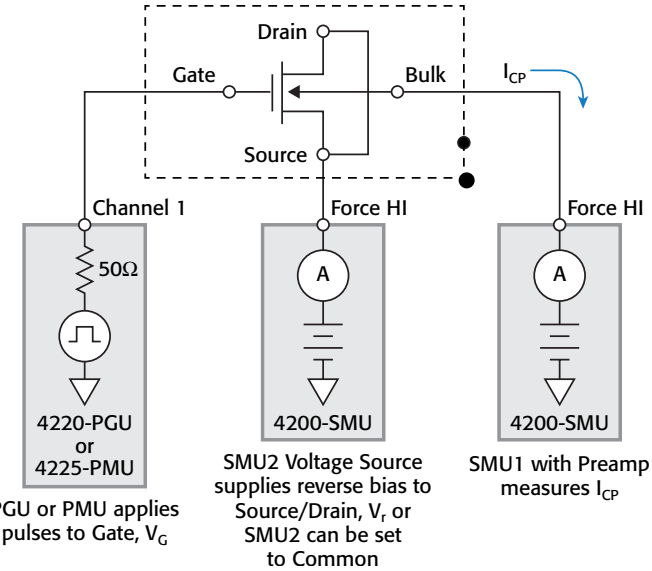

Figure 4. Model 4200-SCS configuration for charge pumping measurements

available in Keithley Application Note Number 2959, "Optimizing Low Current Measurements with the Model 4200-SCS Semiconductor Characterization System."

Using the KITE Software to Automate the Charge Pumping Measurements

The Model 4200-SCS comes with a project that contains a library of tests used in many of the common charge pumping measurement techniques. This *chargepumping* project is located in the projects folder: *C:\S4200\kiuser\Projects_Pulse*. When this project is opened, a list of the tests is displayed in the Project Navigator (***Figure 5***). ***Table 1*** lists the user test modules (UTMs) included in the project and a brief description of each test.

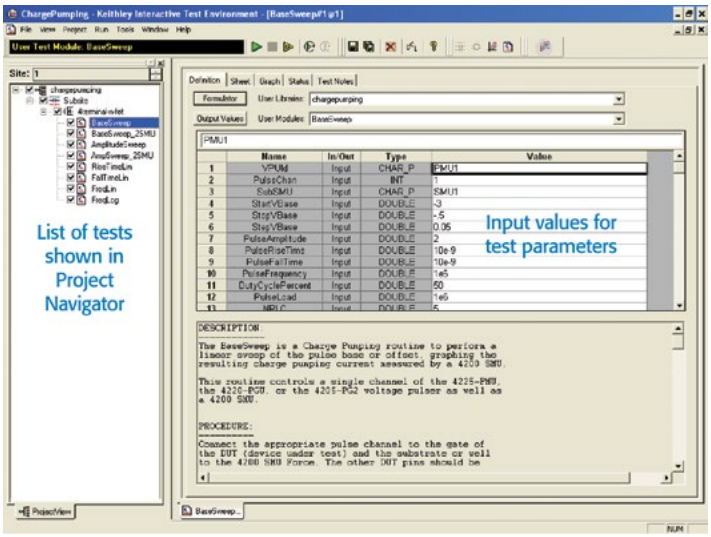

Figure 5. The *chargepumping* project

Table 1. Charge pumping user test modules

User Test Modules	Description
BaseSweep	The base voltage of the waveform is swept while the amplitude of the pulse is kept constant. The resulting charge pumping current is measured and graphed as a function of the base voltage. The source/drain terminals are tied to ground.
BaseSweep_2SMU	Same as *BaseSweep* test, except it adds a second SMU instrument to apply a DC voltage bias to the source/drain terminals.
AmplitudeSweep	The amplitude of the pulse is swept while the base voltage is kept constant. The charge pumping current is measured and graphed as a function of the pulse amplitude voltage. The source/drain terminals are tied to ground.
AmplitudeSweep_2SMU	Same as *AmplitudeSweep* test, except it adds a second SMU instrument to apply a DC voltage bias to the source/drain terminals.
RiseTimeLin	Performs a linear sweep of the rising transition time of the pulse. I_{CP} is measured and graphed as a function of the rise time. The source/drain terminals are tied to ground.
FallTimeLin	Performs a linear sweep of the falling transition time of the pulse. I_{CP} is measured and graphed as a function of the fall time. The source/drain terminals are tied to ground.
FreqLin	With the amplitude, offset voltage, rise/fall times constant, the I_{CP} is measured as a function of a linear sweep of the test frequency. The source/drain terminals are tied to ground.
FreqLog	With the amplitude, offset voltage, and rise/fall times constant, the I_{CP} is measured and graphed as a function of a log sweep of the test frequency. The source/drain terminals are tied to ground.

The user selects the desired test and then inputs the appropriate values for the test parameters on the Definition Tab. The parameters vary depending on the particular test, but they usually include the magnitude of the pulse, sweep values, rise/fall time, test frequency, duty cycle, etc. Specific information on these tests, including the test parameters, is available in Section 16 of the Model 4200-SCS Complete Reference Manual.

After the hardware and the software have been configured, the measurement can be executed in the project by clicking the on-screen Run button. The measurements are displayed in the Graph tab and listed in the Sheet tab. The Sheet tab is used to record and manipulate the data. The measurements (I_{CP}, Q_{CP}, pulsed voltage, etc.) can be saved in a worksheet as an .xls, .txt, or .csv file.

The graph from executing the *BaseSweep* user test module is shown in ***Figure 6***. This user test module measures the charge pumping current as a function of the base voltage.

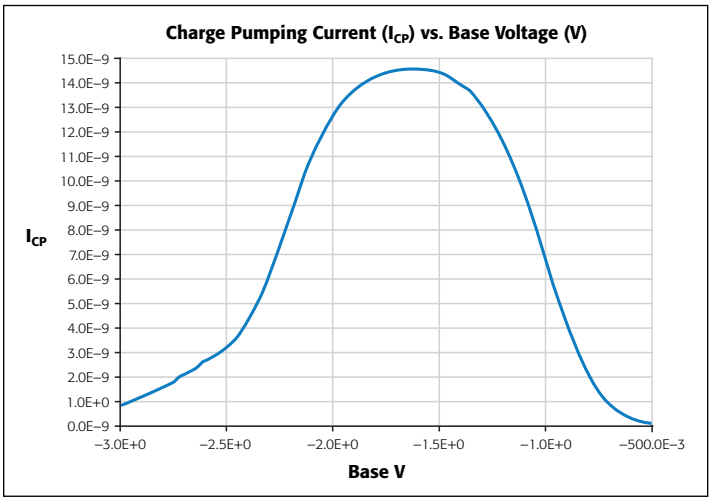

Figure 6. Graphical results of *BaseSweep* user test module

The input parameter values of a user test module can be updated and the measurements can be repeated. One way to do this is by using the on-screen Append Run button, which can be used to show multiple test results on one graph. ***Figure 7*** shows the test results of increasing the test frequency from 1MHz to 6MHz. The data is appended to the graph and a new worksheet is added in the Sheet tab for each appended test run.

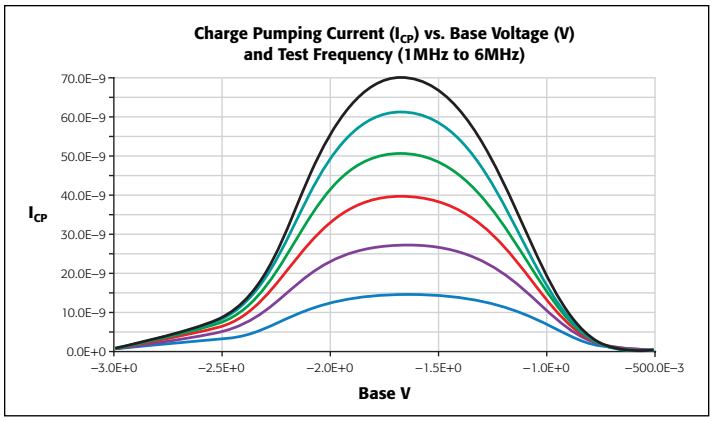

Figure 7. Charge pumping current measurement results at multiple test frequencies

The *AmplitudeSweep* is another common charge pumping test. It measures the charge pumping current as the amplitude of the pulse is swept. The base voltage is kept constant. The resulting charge pumping measurements are shown in ***Figure 8***.

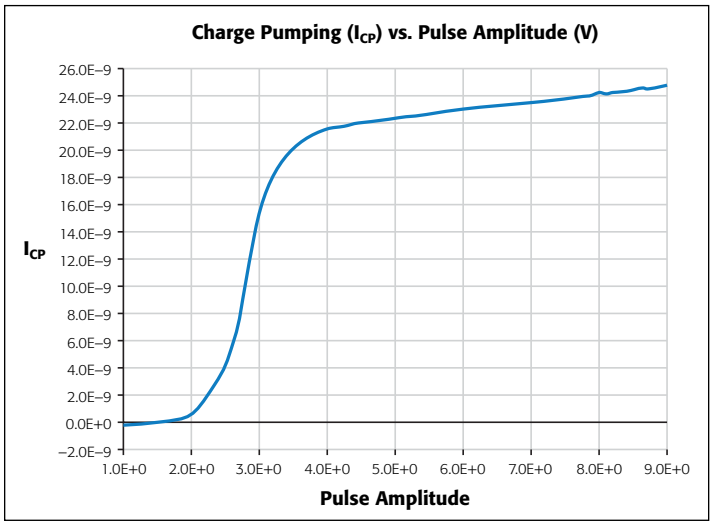

Figure 8. Charge pumping current as a function of pulse amplitude

Simple analyses, such as extracting the interface trap density, can be performed on the data using the built-in Formulator function. To activate this function, click the Formulator button on the Definition tab of the test setup window. Enter the formula for D_{it} as shown in ***Figure 9***. The resulting D_{it} value can also be plotted in the graph.

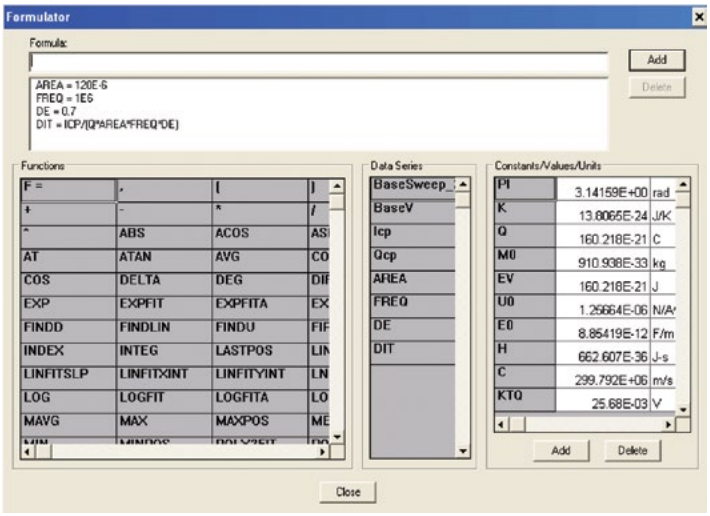

Figure 9. Entering formulas in the Formulator function

Conclusion

The Model 4200-SCS is the ideal tool for characterizing interface properties of gate dielectrics. With the built-in pulse generator, Model 4225-PMU or Model 4220-PGU, and the KTE Interface software, the user need not do any programming, which simplifies measurement and analysis. When equipped with the Model 4225-PMU, the Model 4200-SCS is a powerful tool for performing many tests commonly required in DC and ultra-fast I-V electrical characterization of devices, including the charge pumping application detailed here. The 4225-PMU is not simply a pulse generator; it can also measure current and voltage and be used for transient I-V (waveform capture) applications.

References

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Electrical Characterization of Carbon Nanotube Transistors (CNT FETs) with the Model 4200-SCS Parameter Analyzer

Introduction

Carbon nanotubes (CNTs) have been the subject of a lot of scientific research in recent years, due not only to their small size but to their remarkable electronic and mechanical properties and many potential applications. The problems associated with attempting to scale down traditional semiconductor devices have led researchers to look into CNT-based devices, such as carbon nanotube field effect transistors (CNT FETs), as alternatives. Because they are not subject to the same scaling problems as traditional semiconductor devices, CNT FETs are being studied for a wide variety of applications, including logic devices, memory devices, sensors, etc. The research on these devices typically involves determining various electrical parameters, which may include current-voltage (I-V), pulsed I-V, and capacitance (C) measurements. Characterizing the electrical properties of delicate nanoelectronic devices requires instruments and measurement techniques optimized for low power levels and high measurement sensitivity.

The Model 4200-SCS Parameter Analyzer offers a variety of advantages for electrical characterization of CNT FETs. This configurable test system can simplify these sensitive electrical measurements because it combines multiple measurement instruments into one integrated system that includes hardware, interactive software, graphics, and analysis capabilities. The system comes with pre-configured tests for performing electrical measurements that have been optimized to ensure accurate results on CNT FETs. This application note explains how to optimize DC, pulsed I-V, and C-V measurements on a CNT FET using the Model 4200-SCS Parameter Analyzer. It includes detailed information on proper cabling and connections, guarding, shielding, noise reduction techniques, and other important measurement considerations when testing carbon nanotube transistors.

The Carbon Nanotube Transistor

A single semiconducting CNT can be used as the conducting channel between the source and drain of a FET. ***Figure 1*** illustrates a back-gated Schottky barrier CNT FET. Two metal contacts are located across both ends of the CNT to form the Source and Drain terminals of the FET. The CNT is placed atop an oxide that sits above a doped silicon substrate, which forms the Gate terminal. Connections are made to the three DUT terminals to perform the electrical measurements.

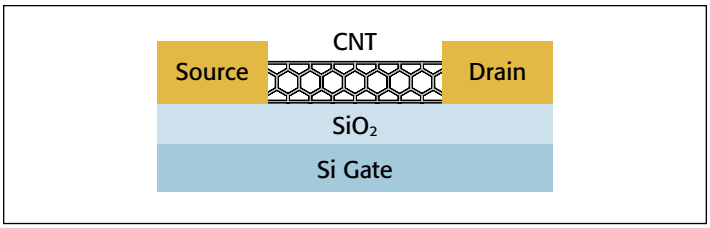

Figure 1. Back-gated carbon nanotube transistor

Making Electrical Measurements with the Model 4200-SCS

The Model 4200-SCS is supplied with a test project for making some of the most commonly used CNT FET measurements. This project (*CNTFET*) includes tests for I-V, pulsed I-V, and C-V measurements. The I-V tests are performed using two of the Model 4200-SMU Source Measure Unit (SMU) Instruments, both with the Model 4200-PA Preamp option. The pulsed and transient I-V measurements are made using the Model 4225-PMU Ultra Fast I-V Module with two Model 4225-RPM Remote/Preamplifier Switch options. Finally, the C-V measurements are

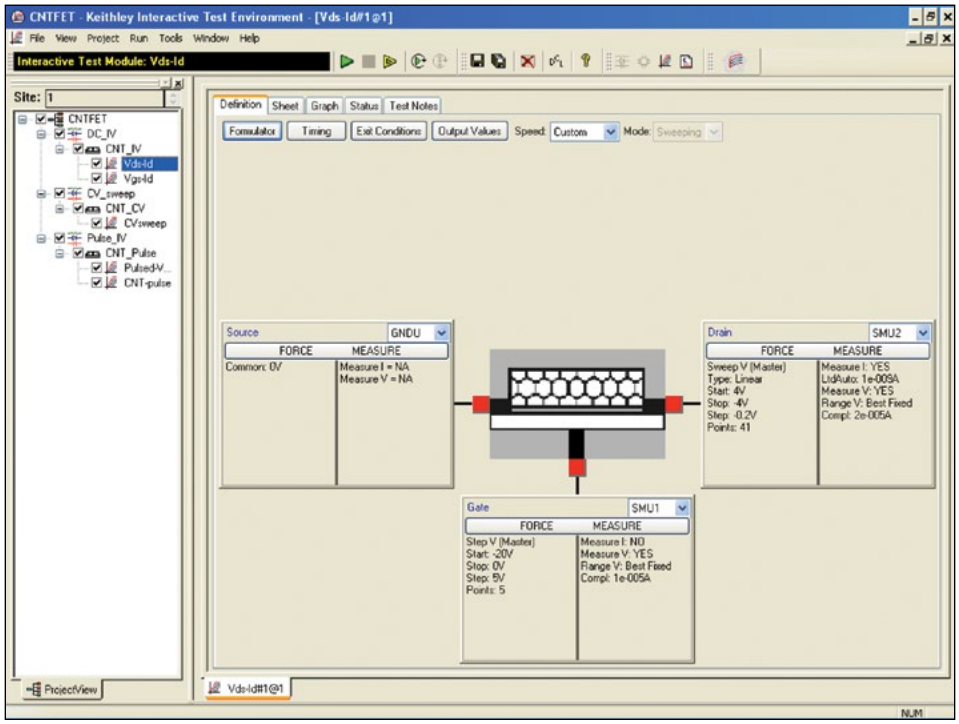

Figure 2. *CNTFET* project for the Model 4200-SCS

performed using the Model 4210-CVU C-V Measurement module.

The *CNTFET* project is included with all Model 4200-SCS systems running KTEI Version 8.1 or later. ***Figure 2*** shows the *CNTFET* project running in the Keithley Interactive Test Environment (KITE) software.

Current-Voltage Measurements

The I-V characteristics of a CNT transistor can be used to extract many of the device's parameters, study the effects of fabrication technique and process variations, determine the quality of the contacts, etc. ***Figure 3*** illustrates a DC I-V test configuration that incorporates two Model 4200-SMU Instruments. These SMU instruments are capable of sourcing and measuring both current and voltage; they have picoamp sensitivity and can be current-limited to prevent damage to the device. In this diagram, SMU1 is connected to the Gate of the CNT FET and SMU2 is connected to the Drain. The Source terminal is connected to the Ground Unit (GNDU) or to a third SMU instrument if it is necessary to source and measure from all three terminals of the FET.

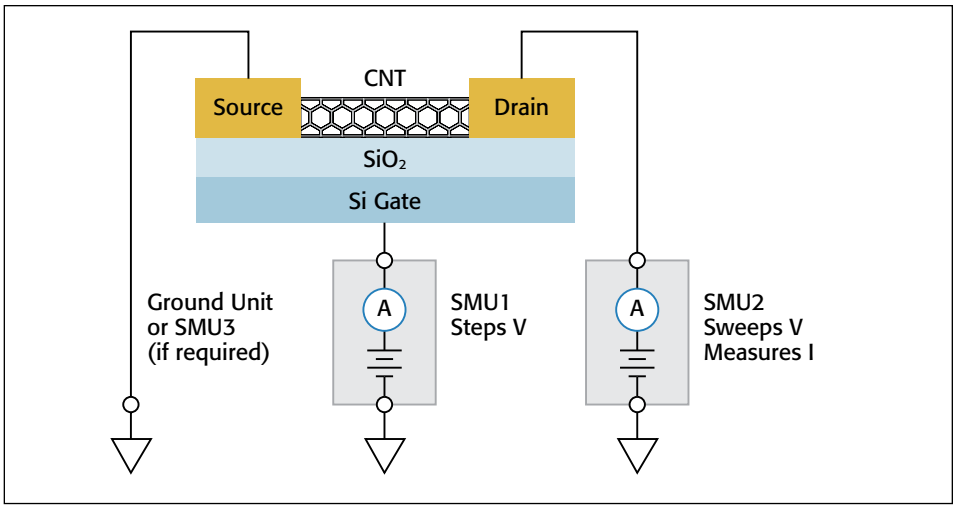

Figure 3. Circuit diagram for measuring the DC I-V characteristics of a CNT FET

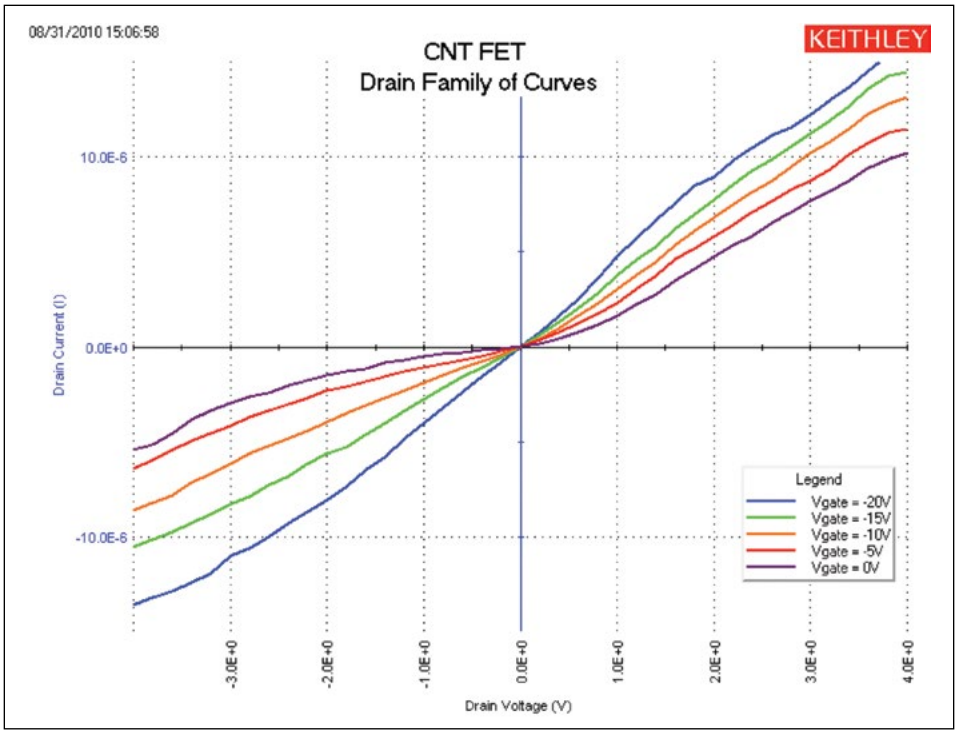

Figure 4. DC I-V drain family of curves measured by the Model 4200-SMU Source Measure Unit

In this example, the Model 4200-SCS's KITE software is set up to measure a DC drain family of curves (V_{ds}–I_d). As SMU1 steps the gate voltage (V_g), SMU2 sweeps the drain voltage (V_d) and measures the resulting drain current (I_d). ***Figure 4*** shows the resulting FET characteristics generated using the *CNTFET* project.

Without changing connections to the device, Model 4200-SCS's interactive KITE software simplifies performing other common I-V tests such as the drain current (I_d) vs. gate voltage (V_g) curves. For this test, the gate voltage is swept and the resulting drain current is measured at a constant drain voltage. The results of an I_d–V_g curve at a constant drain voltage are shown in ***Figure 5***. The drain voltage can also be stepped as the gate voltage is swept.

Optimizing DC measurements

The following techniques will improve the quality of DC measurements made on CNT FETs with the Model 4200-SCS:

- **Limit Current:** To prevent damage to the device while performing I-V characterization, the user should limit the amount of current that can flow through the device. This can be done in the software by setting the Current Compliance of each SMU to a safe level, such as 20μA. This is a programmed limit to ensure the current doesn't exceed the user-defined compliance.
- **Provide Sufficient Settling Time:** Because CNT FET measurements often involve measuring low current (<1μA), it is important to allow sufficient settling time to ensure the measurements are stabilized after a current or voltage has been applied. Some of the factors that affect the settling time of the measurement circuit include the cables, test fixtures, switches, probers, the DUT resistance, and the current range of the measurement instrument. To ensure settled readings,

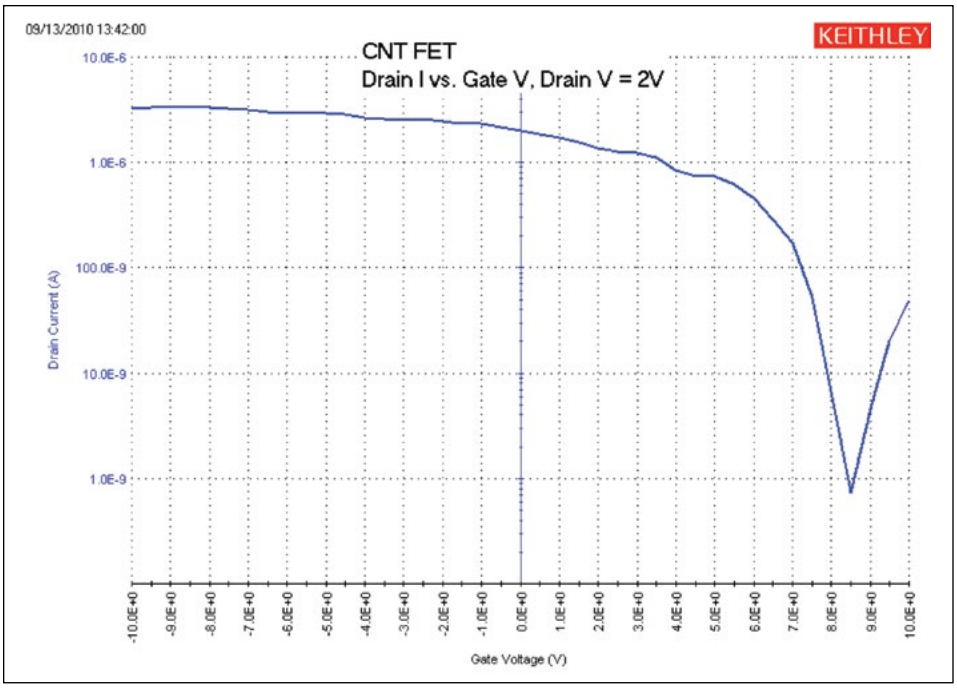

Figure 5. Drain current vs. gate voltage of CNT FET

additional delay time can be added to the voltage or current step time prior to the measurement. This delay time can be easily adjusted in the Timing Menu in the KITE software.

- **Use Proper Speed Modes:** The Timing Menu also offers Speed Modes, including Delay and Filter Factor settings, which affect the settling time of the reading, as well as the integration time of the measurement. Increasing the Delay Factor, Filter Factor, and the A/D Aperture Time can decrease noisy measurements.
- **Minimize Noisy Measurements:** Noise may be generated from a variety of sources, including particle collisions, defects, AC pick-up, and electrostatic interference. Noisy measurements result when a noise signal is superimposed on the DC signal being measured. This can result in inaccurate or fluctuating measurements.

  The most common form of external noise "pick-up" is 60Hz (or 50Hz) line cycle pick-up. This can be a common occurrence near fluorescent lights. Millivolts of noise are not uncommon. Keithley uses a technique called Line-Cycle Integration to minimize the effects of 60Hz (or 50Hz) line pick-up. Line-cycle noise will "average out" when the integration time is equal to an integral number of power line cycles. The number of power line cycles can be adjusted in the KITE software in the Timing Menu.

  Electrostatic interference is another cause of noisy measurements when measuring low currents. This coupling occurs when an electrically charged object approaches the circuit under test. In high impedance circuits, this charge doesn't decay rapidly and can result in unstable measurements. The erroneous readings may be due to either DC or AC electrostatic fields, so electrostatic shielding will help minimize the effects of these fields.

  The electrostatic shield can be just a simple metal box that encloses the test circuit. Probe stations often include an electrostatic/EMI shield or optional dark box. The shield should be connected to the measurement circuit LO, which is the Force LO terminal of the SMU. The Force LO terminal is the outside shield of the triax cable of the SMU or is located on the GNDU. All cables need to be of a low-noise design and shielded. Each Model 4200-SMU comes with two low-noise triax cables.
- **Keep Probes Up:** Make sure the probes are in the up position (not contacted to the device) when connecting and disconnecting instruments from the terminals of the device. The process of moving cables has the potential to inject charge into the device and cause damage. This is due to both triboelectric and piezoelectric effects.

Pulsed I-V Measurements

In addition to making traditional DC I-V measurements, it may be desirable to perform ultra-fast pulsed I-V measurements for various reasons. First, it may be important to observe the high speed response of the CNT device. In some cases, nanostructures can be destroyed by the heat generated when making traditional DC measurements. Pulsed I-V measurements can reduce the total energy dissipated in a device, and therefore reduce the potential for damage. Finally, pulsed electrical testing can prevent current drifting in measurements that can occur during DC measurements.

The pulsed I-V measurements on the CNT FET can be easily made using the Model 4225-PMU Ultra Fast I-V Module. The Model 4225-PMU provides two channels of high speed, multi-level voltage pulse output while simultaneously measuring current and voltage. This module replaces traditional pulse/measure test configurations, which consisted of a pulse generator, digital oscilloscope, interconnect hardware, and software.

The Model 4225-PMU has two modes of ultra-fast I-V source with measure: pulsed I-V and transient I-V. These two modes are illustrated in ***Figure 6***.

Pulsed I-V refers to any test with a pulsed source and a corresponding high speed, time-based measurement that provides DC-like results. The current and/or voltage measurement is an average of readings taken in a predefined measurement window on the pulse. This average of readings is called the "spot mean." The user defines the parameters of the pulse, including the pulse width, duty cycle, rise/fall times, amplitude, etc.

Transient I-V, or waveform capture, is a time-based current and/or voltage measurement that is typically the capture of a pulsed waveform. A transient test is typically a single pulse waveform that is used to study time-varying parameters, such as the drain current degradation versus time due to charge trapping or self-heating. Transient I-V measurements can be used to test a dynamic test circuit or as a diagnostic tool for choosing the appropriate pulse settings in the pulsed I-V mode.

Given that the Model 4225-PMU has two channels, only one module is needed to test a three-terminal CNT FET. A typical test configuration for connecting the PMU module to a CNT FET is shown in ***Figure 7***. In this diagram, Ch 1 of the PMU is connected to the Gate terminal and Ch 2 is connected to the Drain terminal. The Source terminal is connected to the PMU Common, which is the outside shield of the PMU coax connector. To connect this Common terminal to the probe tip, use a BNC or triax shorting plug that will connect the outside of the coax to the manipulator probe. To generate a V_{ds}–I_d curve, Ch 1 steps the gate voltage and Ch 2 sweeps the drain voltage and measures the resulting drain current.

Figure 8 illustrates a pulsed I-V drain family of curves taken with the Model 4225-PMU. For this measurement, a pulse width of 500µs was used to generate the curves. However, each PMU channel has the ability to output voltage pulses as short as 70ns with a rise time as short as 20ns. The minimum duration of the pulse width will depend on several factors, including the test circuit RC time constant and the magnitude of the test current. Each dot on the curves represents a "spot mean" measurement on the pulsed waveform.

The Model 4225-PMU has five ranges full scale from 800mA down to 100µA. To measure lower currents, using the Model 4225-RPM optional Remote Amplifier/Switch is recommended because it adds six measurement ranges, down to 100nA full scale. The pulsed I-V curves shown in ***Figure 8*** were taken on the 100µA range. The threshold current was set to 20µA so that the test will stop if the threshold current level is reached.

For some applications, it may be necessary to study the transient response of a CNT FET. If this is the case, the waveform capture mode (transient I-V) can be used to capture the current and voltage time-based response to the device. ***Figure 9*** shows the transient response of the CNT FET. The blue curve is the pulsed drain voltage and the red curve is the resulting current response as a function of time.

The blue voltage output curve looks close to the defined rise and fall times of 10µs with a pulse width of 50µs. Note that the pulse width is measured at one-half of the input amplitude of 1V. Therefore, the pulse width is measured at 500mV. The sample period in this example is 25ns (40MHz rate). With proper cabling and connections, the voltage shape should be output as defined by the user with minimal deviation.

The red curve shows the drain current and is plotted on the right Y-axis. The drain current is measured at constant drain and gate voltages. The peaks in the curve are caused by charging and discharging of the cabling, as well as the current flow through the device. Note that these peaks occur during the pulse transitions. Reducing the pulse amplitude or increasing the pulse transition time reduces the dV/dt, which reduces the peak height.

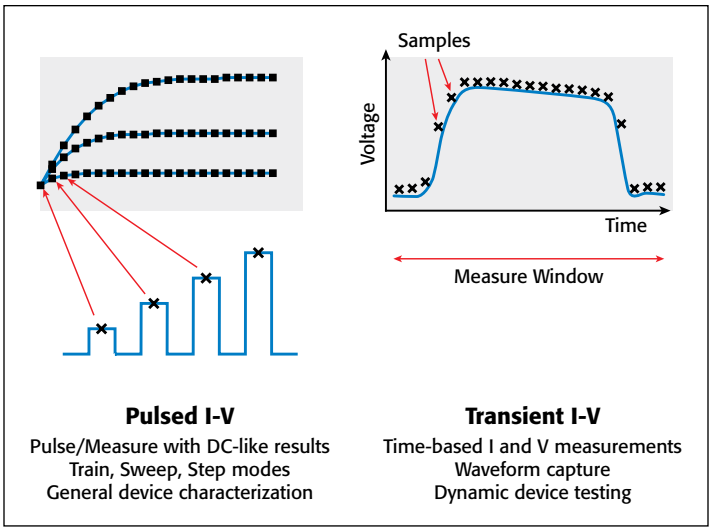

Figure 6. Two modes of ultra fast I-V source with measure: Pulsed I-V and Transient I-V

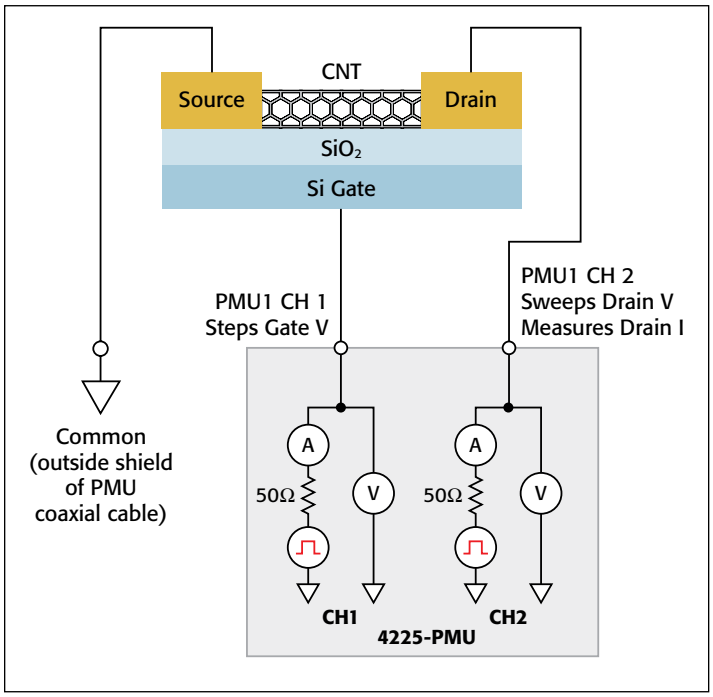

Figure 7. Circuit diagram for measuring the pulsed I-V characteristics of a CNT FET

Optimizing Pulsed I-V Measurements

To improve the quality of pulsed I-V measurements made with the Model 4200-SCS, follow these guidelines:

- **Use the Right Cables and Connections:** Using proper cabling and connections is important for ultra-fast I-V applications in order to achieve the highest frequency output and to avoid signal distortions and capacitive charging effects.

- Use cabling and connections optimized for high frequency (at least 150MHz).
- Use a signal path that matches the impedance of the instrument (50 ohms).
- Tie the low side of the DUT to the shield of the PMU coax cable.
- Connect the shields from each PMU channel together as close as possible to the DUT.
- Minimize the loop area once the center conductor and shield are separate in the test circuit.
- Minimize the cable length.

- **Make the Right Chuck Connections:** CNT FETs and other nanotransistors may be either back-gated or top-gated. For back-gated devices, one of the PMU channels needs to be connected to the chuck of the prober. When making PMU connections to the chuck, the user will give up some functionality of the PMU: fast transitions, high frequency, low current, etc. This is because the output of the high frequency PMU channel is connected to the chuck capacitance and the chuck cabling, which slows down the source response and couples noise into the measurement. If possible, it is better to use a third manipulator and probe directly to the chuck. For high speed sourcing and measuring, it is best to use all top-side connections and avoid connecting the PMU to the chuck.
- **Verify Pulse Width:** Ensure the pulse width is long enough to ensure a settled reading. Verify the resulting current measurement is settled by outputting a single pulse using the Waveform Capture mode. Both the current and voltage can be plotted as a function of time in the Graph tab.
- **Minimize Noise:** To minimize noisy results, multiple waveforms can be averaged or a moving average function can be created in the built-in Formulator to smooth out the measurements further.

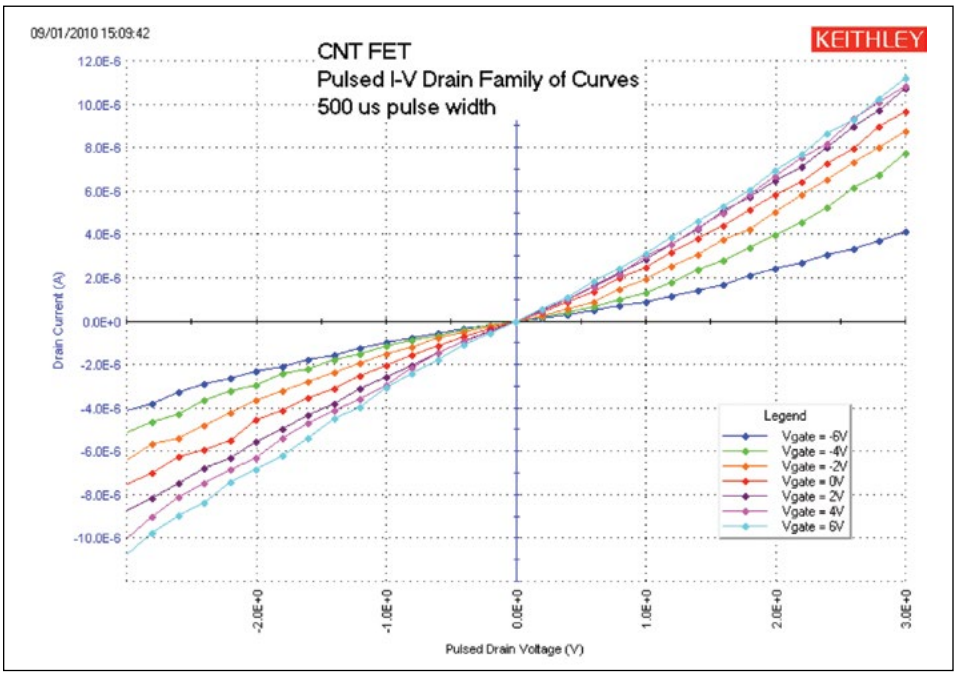

Figure 8. Pulsed I-V drain family of curves of CNT FET

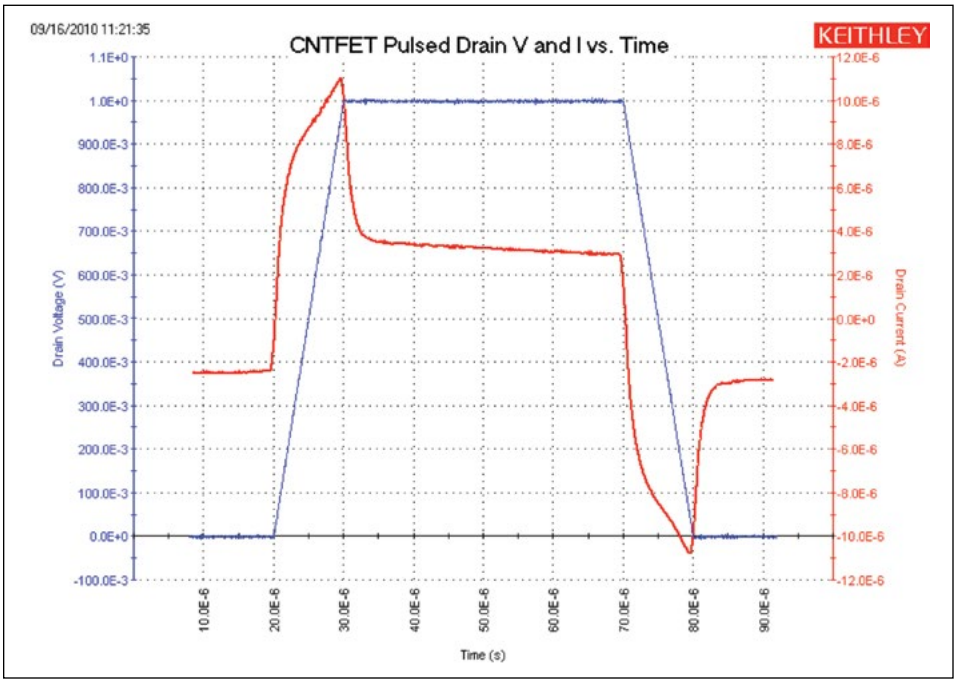

Figure 9. Waveform of single drain voltage pulse and resulting drain current of CNT FET

Capacitance-Voltage Measurements

In addition to performing DC and pulsed I-V measurements on CNT FETs, measuring the capacitance of the FET can also provide information about the device, including the mobility, timing effects, and gate dielectrics. ***Figure 10*** outlines the connections of the Model 4210-CVU to the CNT FET. In this configuration, the gate-to-drain capacitance is measured as a function of the gate voltage.

The HCUR/HPOT terminals that connect the high of the voltage source to the gate should be connected to the chuck. The LCUR/LPOT terminals that measure the capacitance should be connected to the drain terminal of the

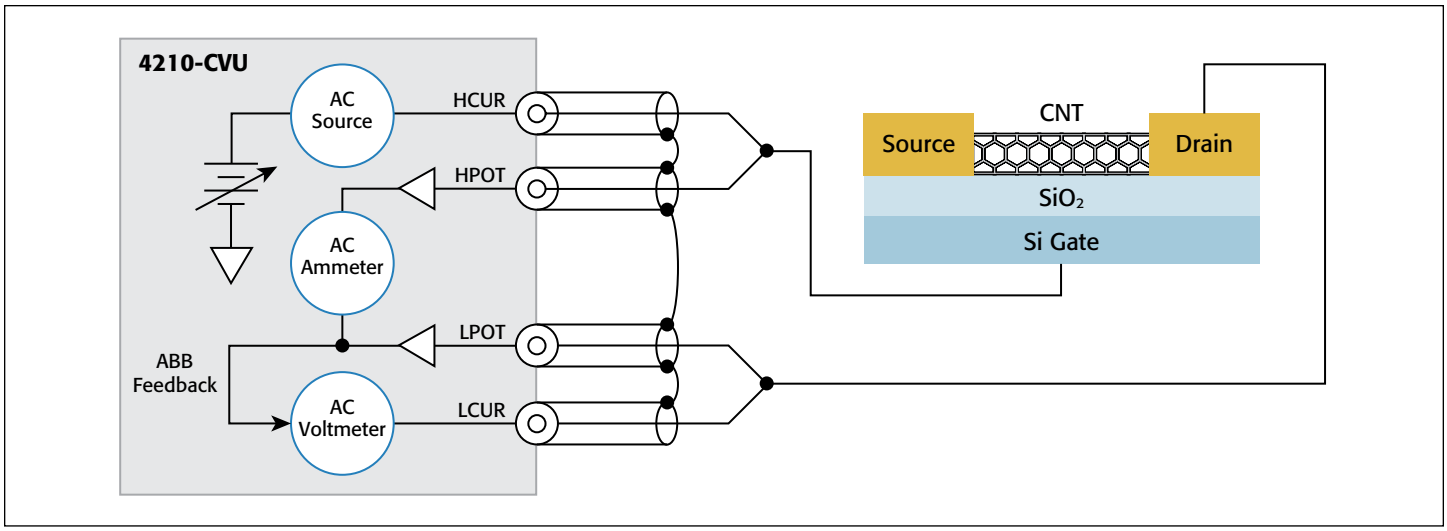

Figure 10. Connections of the Model 4210-CVU to a CNT FET

DUT. For best results, the measurement terminals should never be connected to the chuck. For top-gated CNT FETs, both the measure and voltage source can be output to the gate of the FET from the same terminals (either HCUR/HPOT or LPOT/LCUR) of the CVU. The HI and LO terminals of the CVU are interchangeable in the Force Measure Window of the CVU in the KITE software. The results of generating a C-V sweep between the gate and drain of the CNT FET are shown in ***Figure 11***.

Optimizing Capacitance Measurements

To improve the quality of capacitance measurements made with the Model 4200-SCS, follow these guidelines:

- **Perform Open Compensation (for Measurements <10pF):** The open correction feature compensates for capacitance offsets in the cabling and connections. Performing the correction is a two-part process. The corrections are performed, and then they are enabled within a test module.

  To perform the corrections, open the Tools Menu and select CVU Connection Compensation. For an Open correction, click on Measure Open. Probes must be up or the DUT removed from the test fixture. Enable the correction by clicking on the Compensation button in the Forcing Functions/Measure Options window.

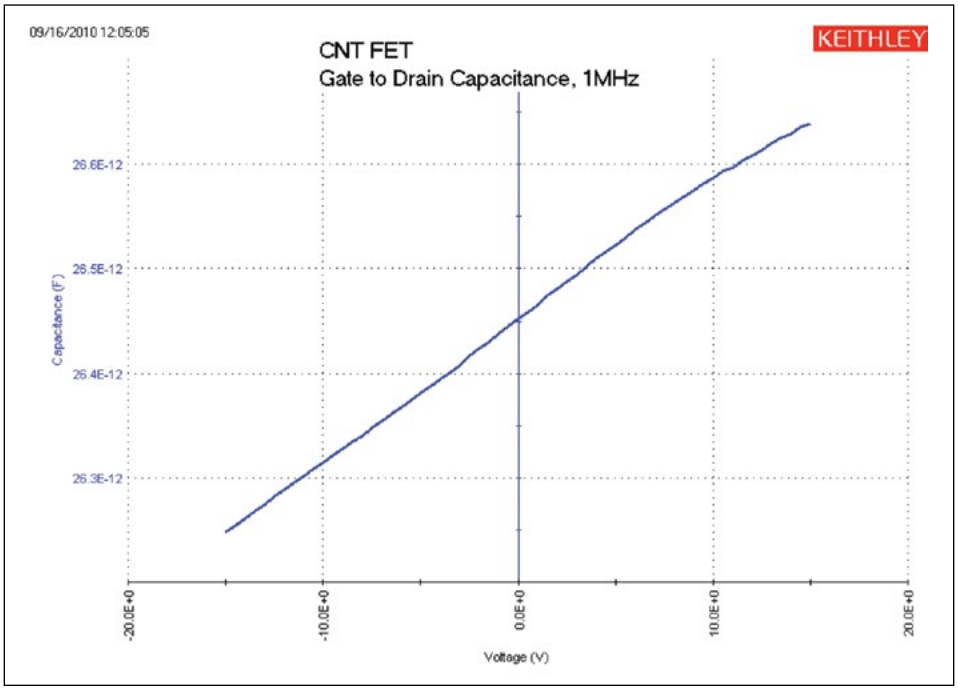

Figure 11. C-V sweep of gate-to-drain capacitance

- **Use Proper Shield Connections:** Connect the shields of the coax cables together as close as possible to the DUT. This reduces the loop area of the shields, which minimizes the inductance. This also helps to maintain the transmission line effects. If the shields are not connected together, offsets may occur. The higher the frequency, the more important this becomes.

- **Choose Appropriate Hold and Sweep Delay Times:** The condition of a device when all internal capacitances are fully charged after an applied voltage step is referred to as "equilibrium." If capacitance measurements are made before the device is in equilibrium, inaccurate results may occur.

  To choose the delay times for a C-V sweep, step an applied voltage using the Sampling Mode, and plot the

capacitance as a function of time. Observe the settling time from the graph. Use this time for the Hold Time for the initial applied voltage or for the Sweep Delay Time applied at each step in the sweep. The Sweep Delay Time may not need to be as long as the first step. The user will need to experiment to verify the appropriate time.

- **Choose Appropriate Speed Mode in Timing Menu:** The Speed mode function enables the user to adjust the time for settling and integration of the measurement. For small capacitances (pico-Farads or less) use the Quiet or Custom Speed modes for best results.
- **Use Guarding:** When making very small capacitance measurements, guarding will help prevent stray capacitance from unused terminals of the device from affecting measurement accuracy. For example, if measuring the capacitance between only the gate and drain terminals, the source terminal of the FET can be connected to the guard. The guard terminal of the Model 4210-CVU is the outside shield of the coax cable.

Conclusion

When using the appropriate instrumentation and measurement techniques, optimal electrical characterization of CNT FETs can be achieved. The Model 4200-SCS is an ideal tool for performing electrical characterization of CNT FETs and other nanostructures because of its integrated hardware, software, and analysis tools. The Model 4200-SMU Source Measure Unit Instrument can be used to determine V_{ds}–I_d, V_{GS}–I_d, resistance, and other I-V measurements on the CNT FET. The Model 4225-PMU Ultra-Fast I-V Module can be used to make pulsed I-V measurements or observe the transient response of a pulsed waveform applied to the DUT. The Model 4210-CVU Capacitance Meter can be used to generate C-V, C-f, or C-t curves. Using the *CNTFET* project that comes with the Model 4200-SCS can further simplify measurement setup and execution.

Acknowledgement

The author appreciates the assistance provided by Sandia National Labs, Livermore, California, who supplied the CNT FETs used in the device testing process during the development of this application note.

Pulsed Characterization of Charge-trapping Behavior in High-κ Gate Dielectrics

Introduction

This application note discusses charge trapping and the limitation of DC characterization techniques in quantifying trapped charge. It also describes an ultra-fast pulse I-V technique for characterizing the intrinsic ("trap free") performance of high-κ gate transistors that exhibit the fast transient charging effect (FTCE).

Development of High-κ Gates for Advances CMOS Devices

High dielectric constant (high-κ) materials, such as hafnium oxide (HfO_2), zirconium oxide (ZrO_2), alumina (Al_2O_3), and their silicates, have drawn a great deal of attention in recent years for potential use as gate dielectrics in advanced CMOS processes [1]. With high dielectric constants, gate dieletrics can be made thicker than SiO_2 while achieving the same capacitance. The result is leakage current that can be lower by as much as several orders of magnitude. However, there are still technical challenges to overcome, such as V_t instability [2-4], carrier channel mobility degradation [5-9], and long-term device reliability [10-13].

One of the important issues preventing implementation of high-κ gates is the trapping of charges in the pre-existing traps inside these dielectrics [14-15]. When the transistor is turned on, some of the channel carriers will be accumulated in the gate dielectric due to the vertical electrical field, resulting in a shift of threshold voltage and a reduction in drain current. Fully understanding charge-trapping and these related mechanisms is the key to understanding channel mobility degradation and device reliability problems. However, traditional DC testing techniques may not accurately characterize these mechanisms.

Limitation of DC Characterization Techniques

As charges are trapped in the gate dielectric, the threshold voltage of the transistor increases due to the built-in voltage in the gate capacitor; therefore, the drain current decreases. It appears that charge trapping and de-trapping times strongly depend on the composition of the gate stacks, i.e., physical thickness of the interfacial SiO_2 layer and high-κ film, as well as process techniques [16-18]. The time scale varies from several microseconds to tens of milliseconds [19]. The de-trapping of the charges is also strongly gate voltage and polarity dependent.

The wide dynamic range of charge trapping, and the voltage dependent trapping and de-trapping, make it very difficult to use one type of characterization technique (especially a DC technique) to get a complete picture of what is going on

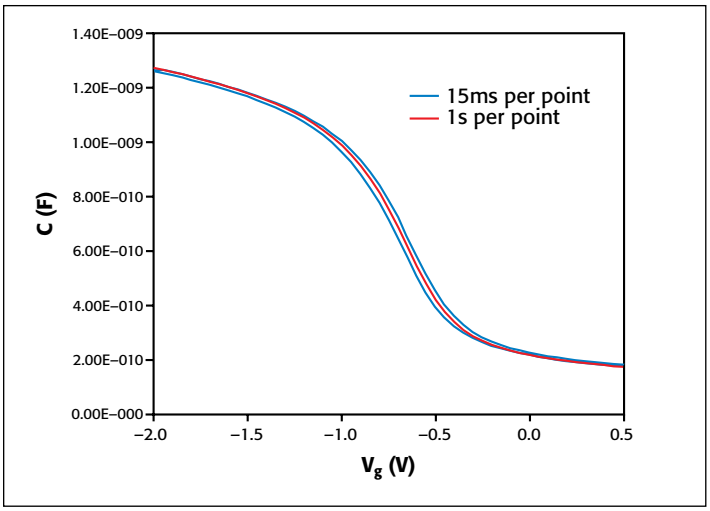

Figure 1. Time-dependent hysteresis of C-V: Slower measurements produce less hysteresis, indicating an equilibrium condition has been reached. Moreover, hysteresis cannot quantify fast transient trapping, since a significant portion of the fast transient trapping could be lost in the DC measurement.

inside the stacked gate dielectric. For example, commonly used methods employ a double sweep in either DC V_{gs}-I_d or high frequency C-V measurements. These techniques involve ramping gate voltage back and forth while drain current or gate capacitance is measured. If hysteresis is seen on the resulting I-V or C-V curves, it is a clear indication of charge trapping inside the gate stacks.

The issue with this technique is that the hysteresis is strongly dependent on measurement time. The hysteresis measured in the DC I-V test could be different from that in a C-V test, because the time taken for each measurement may be dramatically different. This is illustrated by dual sweep C-V measurements taken at different speeds (***Figure 1***). Test speed is strongly dependent on instrumentation and not easily controlled. Even if it were, there is no model to quantify how much charge is really trapped in the gate during the test; i.e., hysteresis cannot quantify the amount of charge trapped, since a significant portion of the fast transient trapping could be lost in the DC measurement.

Another method involves DC stress voltage to inject charges intentionally into the gate, then the use of C-V or I-V method to measure the flat band voltage or threshold voltage shift [20]. The amount of charge trapped can be calculated based on this formula:

$$Q_{trap} = C_{gate} \cdot \Delta V_{fb}, \text{ or } Q_{trap} = C_{gate} \cdot \Delta V1.$$

The issue with this technique is the transition period between DC stress and I-V or C-V measurement, when typically there is

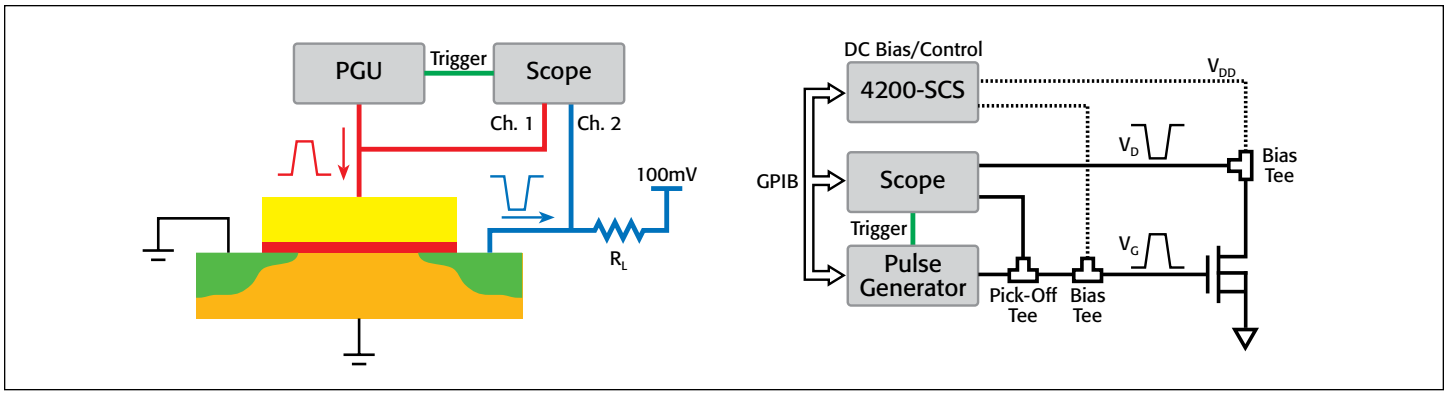

Figure 2. Two different pulse I-V test setups to study transient charge trapping: (a) pulse generator unit (PGU) and scope; (b) integrated test system with hardware and software designed specifically for fast transient trapping measurements.

no applied voltage, or voltage is very low compared to the stress condition. When stress voltage is off, the charges trapped in the gate can de-trap in as little as tens of microseconds. So, only a fraction of the total trapped charges are measured due to the relaxation effect, resulting in an overly "optimistic" view of the film's quality.

Ultra-short Pulse Characterization Techniques

Better methods have been developed over the past few years [3, 4, 19, 21] for capturing the fast transient behavior of charge trapping. ***Figure 2*** shows two different test configurations for a Single Pulse Charge Trapping (SPCT) measurement. In both setups a pulse is applied to the gate of the transistor while its drain is biased at a certain voltage. The change in drain current, resulting from the gate pulse, appears on the digital oscilloscope.

The difference between these two configurations is that the one in ***Figure 2b*** has much higher bandwidth than the one in ***Figure 2a***; therefore, it can capture much faster pulse responses (down to tens of nanoseconds). At such high speed, the bulk traps in a high-κ layer are unlikely to respond; therefore, an "intrinsic" transistor response with negligible charge-trapping effect can be measured.

The key to using SPCT is to look at charge trapping and de-trapping within a single, well-configured gate pulse (***Figure 3***). The pulse usually starts in a position that discharges the gate capacitor before the voltage ramp begins. This is to clean up any residual charges trapped in the gate. Then, during the rise time of the voltage ramp, the corresponding drain current response is captured, allowing a V_{gs}-I_d curve to be formed.

If the pulse rise time is fast enough that there is no charge trapping, then the V_{gs}-I_d curve represents the transistor's intrinsic behavior, free from error due to spurious charge-trapping effects [16]. During the plateau of the pulse, the transistor is turned on, and some of the channel carriers might be trapped in the gate, which changes the threshold voltage and causes the drain current to drop. During the fall time of the pulse, another V_{gs}-I_d curve is formed, but with the charge-trapping effect that should be measured.

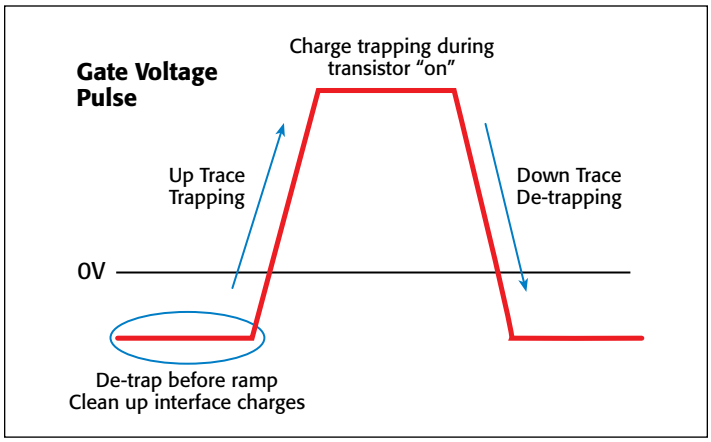

Figure 3. Trapping and de-trapping in single gate voltage pulse.

Figure 4a shows an example of a pulse I-V measurement with different pulse speeds using setups from ***Figures 2a*** and ***2b*** respectively. A DC I-V curve is overlaid for comparison. There is hysteresis with the slower pulse due to charge trapping. By using the faster pulse, hysteresis is eliminated because there's insufficient response time for charges to be trapped.

Slower pulse measurements should only be used for high-κ devices with relatively low charge-trapping effects. Although the hysteresis of a slower pulse I-V curve can quantify charge trapping better than a DC method, results must be interpreted with caution, since de-trapping effects are influenced by the specific structure of the gate stack and the pulse fall time. Also, when two traces in the tr and tf portions are not parallel, it is difficult to define the point at which hysteresis is measured.

An alternative approach is to plot pulse I_d versus time (***Figure 4b***). An evaluation of the pulse width portion of I_d (where I_d degrades) can be used to quantify trapped charge [15, 16]. Still, to ensure negligible charge trapping during the entire pulse, one can use a fast pulse with short rise and fall times. This can be achieved easily with the ultra-short-pulse test system in ***Figure 2b***. It produces I_d-V_g values by using a single pulse per point of less than 100ns.

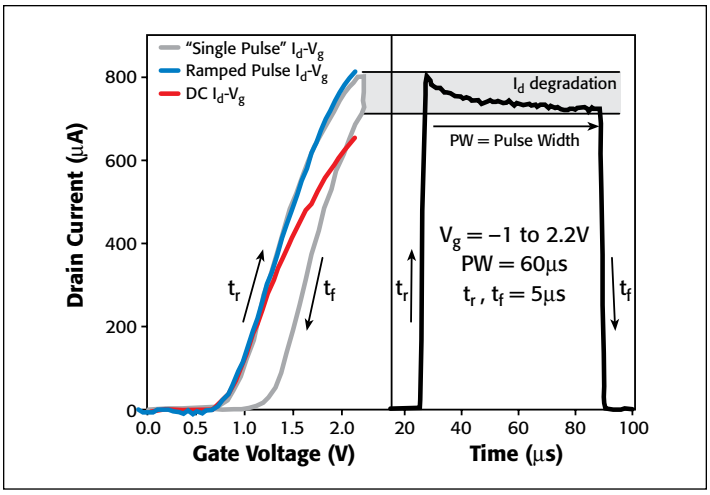

Figure 4. Single Pulse Charge Trapping measurements: (a) the ultra-short ramped pulse I_d-V_g and slow "single pulse" pulse with hysteresis (DC result is shown as a reference), and (b) corresponding slow pulse versus time illustrating an alternative approach to determine the degradation of I_d.

Benefits of Short Pulse Characterization

Since there is much less charge-trapping effect with very short pulse widths, the drain current measured is higher than under DC conditions (red curve, ***Figure 4a***). This results in a higher predicted channel carrier mobility when pulse I-V data are used to generate a model, which is more representative of transistors that are switching very fast (i.e., those that will not experience full charge-trapping effects). Another advantage of the ultra-short pulse system is that the pulse I-V measurements, with pulse widths on the order of nanoseconds, can be performed very easily and results can be compared to a DC measurement without resetting the system hardware or moving the wafer to another station. Such a comparison is shown in ***Figure 5***.

Drive current measured using the pulse I-V technique can be significantly higher than DC due to the lack of charge-trapping effects. This illustrates the close-to-intrinsic performance of transistors with high-κ gate dielectrics, and ultimately demonstrates the advantage of the ultra-short pulse I-V technique.

Because of complications associated with trying to characterize charge-trapping effects for transistors with different functionalities, including high frequency operation, the best solution for modeling engineers is to use instrumentation and a test configuration that avoids artifacts associated with DC or slower pulse measurements. The ultra-short pulse measurement technique provides a better depiction of real device performance [22], so the resulting models help optimize designs for actual operating conditions.

Process engineers also need these pulse measurement techniques to characterize and track improvements in their continuing efforts to improve film quality and remove charge-trapping degradation. Finally, an understanding of the intrinsic behavior of high-κ gate dielectric devices is key to understanding the physics of charge trapping and de-trapping. This physical-based understanding leads to the correct extrapolation of device lifetime.

Sources of Error

Although ultra-short pulse measurements are a powerful technique, recognize that speed characteristics are in the radio frequency (RF) domain. Therefore, it is easy to introduce measurement errors if the test system is not optimized for high bandwidth. There are three main sources of errors: signal losses due to cables and connectors, losses due to device parasitics, and contact resistance.

Signal losses due to cables and connectors, as well as contact resistance effects, can be calibrated out using a transistor with a SiO_2 gate, where there is no charge-trapping effect. The pulse I-V curve should overlay the DC I-V curve precisely once the calibration is complete.

However, device parasitics, usually parasitic capacitance between pad contacts, cannot be easily removed. This will reduce the pulse current from the drain terminal. This problem can be designed out by using RF-compatible transistor structures (Ground-Signal-Ground), and by increasing pad pitch so that

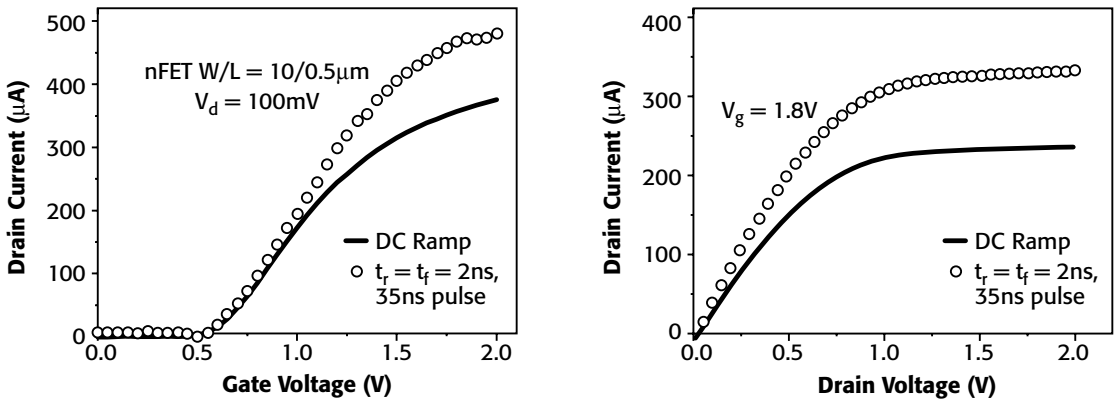

Figure 5. Overlay of ramped pulse I-V and DC I-V measurements on NMOSFET with high-κ (HfO_2) gate dielectric: (a) DC and pulsed I_d-V_g measurement at linear region, (b) DC and pulsed Id-Vd measurement. Short pulse parameters allowed close-to-intrinsic drive current to be measured and compared to the DC measurement.

capacitance between the pads is small enough not to affect pulse current measurements.

Conclusion

DC characterization techniques are inadequate for capturing the dynamic nature of charge trapping in high-κ gate stack structures. Pulse I-V is a powerful technique that allows characterizing transistors with high-κ gate stacks in a trap-free environment that permits assessing their intrinsic qualities. When current is measured in a shorter time than that associated with the charge-trapping time scale, improved intrinsic transistor characteristics can be achieved, including a drive current that is significantly higher than that measured with traditional DC I-V techniques.

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Pulse I-V Characterization of Non-Volatile Memory Technologies

Introduction

Until recently, floating gate (FG) NAND flash memory technology has successfully met the growing requirement for non-volatile memory (NVM) for digital cameras, MP3 players and smartphones. However, there is increasing concern in the consumer electronics industry that floating gate NVM may not be able to continue providing higher storage capacities at the ever-lower cost-per-bit requirements that drive the NVM market [1]. The potential for the floating gate approach to "hit the wall" means that research into alternative technologies has become increasingly critical.

This wide-ranging research into an expanding number of materials and technologies requires an electrical test system with wide dynamic range and flexible parameter control. This application note provides a brief history of NVM, an overview of the test parameters required for electrical characterization of NVM materials and devices, and an explanation of the capabilities of the Model 4225-PMU Ultra-Fast I-V Module with the Model 4225-RPM Remote Amplifier/Switch, two instrument options designed for use with Keithley's Model 4200-SCS Parameter Analyzer. The Model 4225-PMU/4225-RPM combination has integrated simultaneous measurement of current and voltage on each channel, making investigating transient pulse responses much simpler than with previous hardware. With the system's multi-pulse waveform generation capability, the Model 4200-SCS with the Model 4225-PMU may be used to characterize the memory device's switching mechanism in both the transient and I-V domains. After a discussion of emerging test requirements, this note provides an overview of the NVM project, tests, and parameters for testing floating gate flash, phase-change cell, and ferro-electric cell devices.

Brief History of NVM

Scientists around the world are investigating NVM alternatives that can replace FG NAND technology, including phase-change memory (PCM/PRAM), charge trap flash (CTF/SONOS), resistive memory (ReRAM), ferro-electric memory (FeRAM), and magnetoresistive memory (MRAM) (***Figure 1***). These device technologies have been studied for years, and each is currently available in the market in some form. Other NVM technologies, including spin-transfer torque (STT) MRAM, floating body (FBRAM), and various types of carbon-nanotube-based memory (CNT RAM), are being actively researched to determine their suitability for memory product applications.

In addition to the traditional uses of NVM in portable consumer electronic devices, the success of FG NVM has created new product categories, such the ubiquitous "thumb" or USB drive and, more recently, the high performance Solid State Disk (SSD) products now being used as replacements for traditional computer hard drives in high performance applications. These products, as well as the possibility of a "universal" memory that would replace both existing flash and dynamic memory (DRAM), have justified ongoing research at universities and semiconductor organizations and companies [2].

The ideal memory should have characteristics of both dynamic and non-volatile memory:

- Increasingly low cost and high density based on predictable scalability

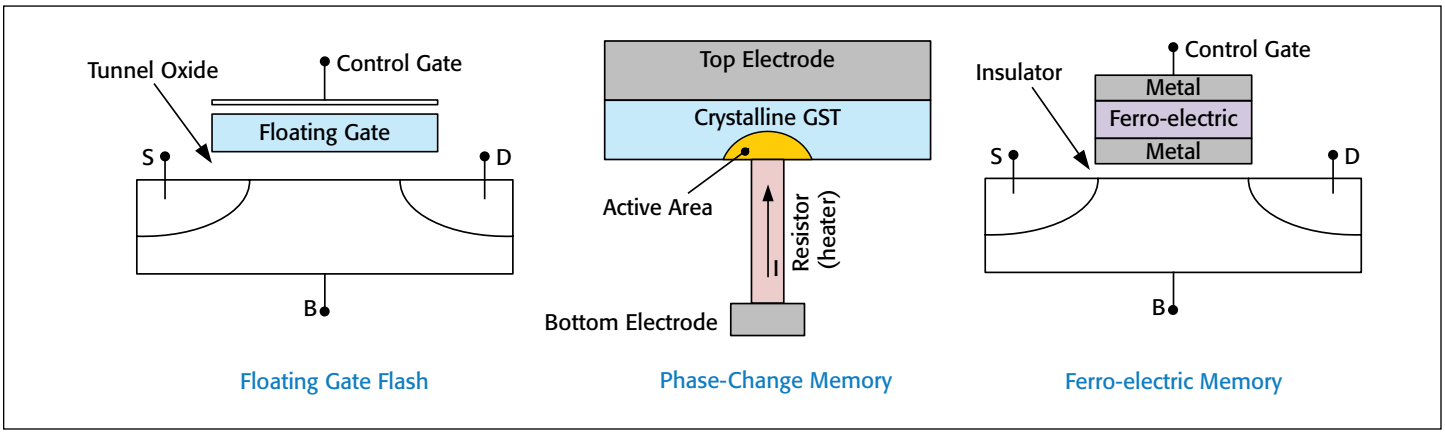

Figure 1. Various non-volatile memory devices.

- Fast read/write (similar to or faster than existing DRAM speeds)
- High endurance (to address DRAM or SSD applications)
- Long retention
- Low power and voltage requirements
- Compatible with existing logic circuits and semiconductor processes

As the applications for FG NVM devices have increased, so too has the pressure on the FG technology. This has opened up the market to multiple technologies that may replace the FG approach. The future may have multiple NVM technologies addressing the different requirements for each product type or category. In fact, the 2010 International Technology Roadmap for Semiconductors (ITRS) just recommended two additional NVM technologies that should receive accelerated research and development leading to commercial NVM products: Spin Transfer Torque MRAM (STT-MRAM) and Redox RRAM [1].

NVM Test Requirement Evolution and Overview

With floating gate flash memory, electrical characterization was traditionally performed using DC instruments, such as source measure unit (SMU) instruments, after pulse generators had programmed and/or erased the memory cell. This requires some type of switch to apply the DC or pulse signal alternately to the test device. Occasionally, oscilloscopes were used to verify pulse fidelity (pulse width, overshoot, pulse voltage level, rise time, fall time) at the device under test (DUT). Measuring the pulse is important because the flash memory state is quite sensitive to the pulse voltage level. However, the use of oscilloscopes was relatively rare, even in research, because the required setup for oscilloscope measurements differed from that for the pulse-source/DC-measure approach. Even when scopes were used for flash characterization, the complexity of measuring the transient current meant that voltage was the only measurement taken while pulsing.

Recently, standard instrumentation has improved, and now it is possible to measure the current and voltage simultaneously with a single instrument while applying pulses to a memory device or material. Although this capability was possible earlier, it required a rack of instruments and involved making various tradeoffs related to cost, performance, and complexity. In addition, these custom systems were typically created and maintained by an in-house test instrumentation expert who had the wide-ranging skills, experience, and significant time necessary to integrate the various instruments into a system that provided pulse source and measure. These earlier systems were functional, but they were typically one-off creations with limited test envelopes and cumbersome test controls and required time-consuming data extraction. The measurement approach typically used a load or sense resistor with an oscilloscope or digitizer to measure the current. This is a proven technique, but the effect of the load resistor on the voltage delivered to the device has significant downsides for many pulse measurements. Also, correlation across multiple systems and obtaining traceable system-level calibration was effectively impossible.

The new instrumentation provides researchers with additional data to gain a better understanding of NVM material and device behavior in less time. Applying pulses while simultaneously measuring the voltage and current with high-speed sampling provides better insight into the electrical and physical mechanisms that provide the memory behavior. Adding this transient characterization capability to DC characterization provides fundamental data on intrinsic material properties and device response.

Many materials and technologies are currently under investigation for NVM, and each has unique aspects for the physical memory behavior. However, the overall electrical characterization of these various approaches share important test parameters and methods. This commonality means that a single test instrument is useful for characterizing a wide range of memory technologies and device types.

Electrical characterization is crucial to a better understanding of the physical aspects of the underlying technology. Regardless of the particular memory technology under investigation, pulsing is required to exercise the switching behavior. Pulsing with simultaneous measurement provides the data necessary to understand the dynamic behavior of the switching mechanism. Different materials use different terms. For example, the terms *program/erase*, *set/reset*, and *write/erase* are used to indicate the fundamental storage of a 1 or 0 bit. These write/erase procedures are done in a pulse mode to provide the overall speed required for typical memory operations and simulate the final product environment. The next section addresses important test parameters that are common to a wide range of non-volatile memory technologies.

Common NVM Test Parameters

Pulse amplitude is the required pulse height used to program and erase the memory cell. Floating gate memory can require 15–20V, or even greater, during the write pulse. Most NVM candidates require 3–5V. The goal for replacement NVM technologies is lower pulse amplitudes, but early research prior to any dimensional scaling or material optimization can require 6–8V. Many technologies require bipolar pulses at these voltage levels, but some recent pulse I-V solutions do not provide these higher voltages when used in a bipolar sourcing mode.

Pulse amplitude fidelity is one of the most important parameters in NVM testing because memory state switching behaviors are non-linear (for example, Fowler-Nordheim current, phase transformation, filament creation/annihilation); therefore, these devices are sensitive to the amplitude of the voltage pulse. Pulse amplitude fidelity parameters are specified in terms of pulse level accuracy, **ringing**, **overshoot**, and **undershoot**. Minimizing the ringing, overshoot, and undershoot is critical to

the design of the pulse instrument. Modern pulse I-V systems can provide overshoot and ringing specifications of 3% or less. However, it's important to be aware that pulse shape fidelity at the test device is significantly affected by the connection setup, cables, pulse parameters, device impedance, timing, and impedance mismatches.

In addition to accurate pulse levels, newer technologies require complicated and easily adjustable waveforms, not just a single standard square pulse. For example, testing of ReRAM devices often requires pulse sweep up/sweep down profiles while simultaneously measuring the current. FeRam testing requires the PUND (Positive, Up, Negative, Down) four-pulse sequence. PRAM (phase-change memory) testing requires the ability to do sweeps of virtually any pulse parameter, such as sweeping the fall time of one of the four pulses in the RESET-measure-SET-measure multi-pulse waveform. All of these memory technologies require the ability to output **multi-pulse waveforms** consisting of arbitrary segments, together with multiple measurements within each waveform. Endurance testing requires the ability to output complex arbitrary waveforms quickly without the need for additional setup time or overhead. This requirement further separates the capabilities of newer pulse instrumentation from those of the traditional two-level pulse generator.

Pulse timing parameters, such as *rise time*, *fall time*, and *pulse width* in test equipment will continue to be very important, especially with the general trend toward faster pulsing, with pulse widths trending from 100ns down to <10ns. For some technologies, such as PRAM, fall time is a critical parameter to define how the RESET operation takes place. This is important because traditional pulse generators typically have limited rise/fall timing ranges and do not permit, for example, a 20ns rise time combined with a 2ms fall time. In general, shorter pulse widths and faster transition times are preferred, but there are practical limitations due to typical interconnect impedances, measurement constraints, and instrumentation tradeoffs.

The need for dynamic, simultaneous **ultra-fast current and voltage measurement** is driven by emerging NVM technologies such as the phase-change and ferro-electric approaches discussed previously. The Model 4225-PMU/4225-RPM combination provides simultaneous voltage and current measurement, which is important when the dynamic resistance of the material represents the electrical manifestation of the physical mechanism of the bit storage.

The scaling trend leads to smaller and smaller devices. This trend requires measuring smaller currents while pulsing, which calls for some type of a pre-amplifier for the current measurement. To minimize parasitic effects of the cable capacitance and have better control of the amount of energy to the test device, a **remote pulse amplifier**, connected within 15–25cm (6–10 inches) of the DUT, presents a significant benefit. This is especially important for phase change memory (PCM) and ReRAM characterization.

Current compliance or **current control** is important for testing some NVM technologies, such as ReRAM and PRAM. Usually, this is done using DC instruments and sometimes implemented in custom pulse setups. It is not clear if the current compliance in DC instrumentation is providing sufficiently fast control of the current to meet the typical requirements. For pulsing current control, it is desirable to install the current control device as close as possible to the test device to avoid the possibility of current discharging from the interconnect capacitance into the test device.

To simplify and speed up testing, **switching between pulse and DC instruments** is necessary. To float connections in flash program/erase cycles for endurance testing, switching has to be fast (10–100μs) because the switching must occur between the program and erase pulses to allow for a very large number of stress waveforms. This type of switch should be controlled directly by the pulse generator and located within the pulse instrument for fast control. Typically, this switching is performed by a solid state relay (**SSR**) for each pulse channel.

Channel synchronization is necessary for NVM testing that requires multiple pulse source and measure channels. Two channels are sufficient for PRAM and ReRAM characterization, to force and measure on both sides of two-terminal devices. For NVM that utilizes transistors as access devices, three or four channels of pulse I-V may be required. In flash memory, two or four channels are needed. Traditional pulse instruments are difficult to synchronize because there are a variety of trigger synchronization methods, each of which has different complexity/trigger performance tradeoffs associated with it. Modern pulse I-V instruments offer internal trigger routing and automatic synchronization in addition to the integrated measurement capability.

As mentioned previously, different NVM technologies have slightly different measurement needs. ***Table 1*** summarizes the important test parameters for a few memory technologies.

Capabilities of Model 4225-PMU and Model 4225-RPM for NVM Characterization

The Model 4225-PMU Ultra-Fast I-V Module (***Figure 2***) is a single-slot instrument card for the Model 4200-SCS. It has two channels of voltage pulse sourcing with integrated, simultaneous real-time current and voltage measure for each channel. There are two types of measurements: sample and spot mean. The sample type is used to capture the time-based current and voltage waveforms critical for understanding transient or dynamic behaviors. The spot mean type provides DC-like current and voltage measurements for I-V characterization. The real-time sampling capability is critical to capture the transient behavior of NVM materials in a single waveform, because applying repetitive waveforms will cause the memory switching behavior or even damage to the material itself.

Table 1. Summary of important test parameters for NVM technologies.

NVM Type	Pulse Level	Pulse Transition, Pulse Fidelity	Transient Measurement	Multi-Level Pulses	Multi-Channel Synch
Floating Gate Flash	15–20V+	Minimizing pulse overshoot is critical because of the non-linear nature of the tunneling current used to program or erase the cell.	Emerging need to increase understanding of charge transport.	Required for bipolar pulse waveform for write and erase. Also require high-speed control for solid state relay (high impedance) on source and drain during FN erase.	Emerging need
PRAM (PCRAM)	~±8V	Asymmetric rise and fall required: Fast fall time (≤20ns) for RESET pulse, slow fall time for crystallization (tens to hundreds of nanoseconds).	Critical to understand material and cell behavior.	Unipolar, multi-level pulsing for reset-measure-set-measure waveforms.	Necessary when transitioning to 1T1R [1] device
ReRAM	~±6V	Accurate pulse levels and transition control allow for the study of ion transport or filament formation.	Emerging requirement to help understand material and cell behavior, assist in search for lower-current variants.	Required for both unipolar and bipolar technologies.	Necessary for 1T1R [1] device structure
FeRAM	~±5V	Pulse transition control allows for polarization change characterization.	High speed charge measurements are critical to characterizing capacitive memory effect.	Bipolar pulsing for write and erase (PUND method).	Useful for 1T1C [2] device structure

1. 1T1R = memory cell consisting of one transistor and one resistor, with the transistor providing the control and access to the cell.
2. 1T1C = memory cell consisting of one transistor and one capacitor, with the transistor providing the control and access to the cell.

Figure 2. Model 4225-PMU Ultra-Fast I-V Module and two Model 4225-RPM Remote Amplifier/Switch Modules.

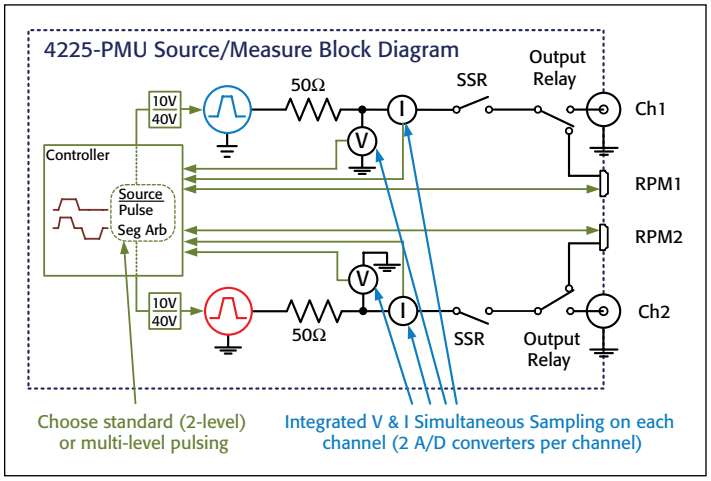

Figure 3. Model 4225-PMU Block Diagram. It is possible to use the Model 4225-PMU with two Model 4225-RPMs by using the RPM1 and RPM2 connections. The SSR shows the solid-state relay, which is useful for high impedance mode when performing program or erase on flash memory devices via Fowler-Nordheim tunneling.

The Model 4225-RPM Remote Amplifier/Switch is an optional addition to the Model 4225-PMU. This small box is located near the DUT and provides the lower-current measurement ranges necessary for characterization of many NVM materials and technologies. In addition, the Model 4225-RPM provides switching for the Model 4200-SCS's source measurement units (SMUs) and CVU signals to allow for high resolution DC measurements and C-V measurements. The Model 4225-RPM is a single-channel device, so two Model 4225-RPM modules are required to match the two channels from the Model 4225-PMU. The Model 4225-RPM module is designed to be located close to the test device (≤30cm or one foot), minimizing cabling effects to provide improved pulse shape and high speed measurements.

The PMU/RPM combination provides the test capabilities to characterize the existing and emerging NVM technologies described previously. ***Figure 3*** is a block diagram of the Model 4225-PMU. Note that both channels have both current and voltage measurement (two A/D converters per channel). Each channel can independently source ±10V or ±40V (into high impedance). ***Figure 4*** is a block diagram of the Model 4225-RPM: on the left side, note the inputs from the Model 4200-SCS

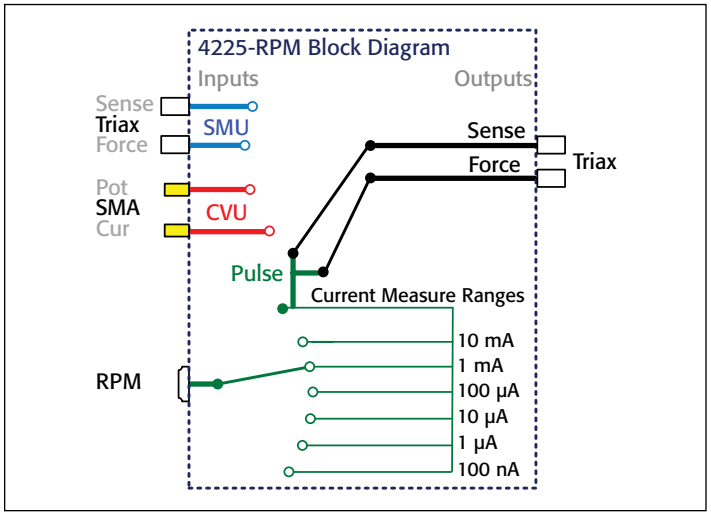

Figure 4. Model 4225-RPM Block Diagram. The Model 4225-RPM is both a current pre-amplifier for high speed current measure (in Pulse mode) and a switch for use in choosing between Pulse I-V, SMU, or C-V measurement modes for other instruments in the Model 4200-SCS chassis.

chassis; on the right side, note the output to the DUT. The top half (blue, red, and heavy green lines) is the switching part of the Model 4225-RPM. Note that the SMU and CVU pathways support four-wire connections throughout. The thinner green lines near the bottom represent the various pulse current measure ranges.

Pulse Level

Each Model 4225-PMU channel has two source ranges. The 10V source range can output from –10V to +10V (20V amplitude) into high impedance and covers most of the modern NVM candidates. For testing of existing floating gate flash or early non-optimized emerging materials that require higher voltages, the Model 4225-PMU also has a 40V range, outputting from –40V to +40V (80V amplitude) into high impedance. Because both source ranges are bipolar, both unipolar and bipolar memory technologies can be characterized.

Transient Measurement and Multi-Channel Synch

The Model 4225-PMU has two channels, each of which has two A/D converters that sample the voltage and current simultaneously. With the two channels, both the gate and drain of a device may be synchronously pulsed while sampling the voltage and current on both channels to capture the dynamic response of the DUT. If more than two channels of pulse I-V are required, multiple Model 4225-PMU cards may be installed in a single chassis and all channels will be automatically synchronized to within ±2ns. This simultaneous, synchronous measurement is critical to understanding the switching behaviors of NVM materials and devices.

The Model 4225-RPM adds measure ranges from 10mA down to 100nA to permit transient analysis of the small currents that are characteristic of the switching states. In addition, the RPM has switching capability to permit routing SMU instrument or C-V signals to the test device.

Pulse Transition and Multi-Level Waveforms

The Model 4225-PMU has two independent channels, with timing parameters adjustable from 20ns to 40s. The shortest pulse possible is 40ns (FWHM, Full Width at Half Maximum of pulse amplitude), but wider pulses are required to measure smaller currents.

Multi-level or multi-pulse waveforms can be created by linking together linear segments (voltage vs. time) using the Segment ARB® feature. Each channel has a maximum of 2048 segments that may be used in a single sequence or used across multiple sequences. A sequence is a set of segments that allows for looping, typically to provide stresses from a looped sequence interspersed with a measure sequence.

Measurements are controlled on a segment-by-segment basis, so only the required data is collected, maximizing the use of the available sample storage memory, similar to the segmented memory feature available in high-end oscilloscopes. In addition, two measurement types are available: sample and mean. The sample type is used to capture time-based signals, useful for capturing transient behaviors and validating proper connections by evaluating the pulse shape behavior. The mean measurement type is used when measuring I-V characteristics. Both types can be applied to the entire segment, a partial segment, or all segments in the waveform on a channel-by-channel basis.

The ability to output dozens or hundreds of unique pulses within a single waveform decreases test time over that of traditional pulse instruments, which could only pulse between two pulse levels. Traditional floating gate flash used two pulse channels to create a two-pulse waveform of three voltage levels for a single test device terminal (***Figure 5***). In addition, it required an external switch between the pulse generators and the DUT to route each pulse alternately to the terminal. This external switch added complexity and cost, and most importantly, increased test time. Pulsing the gain and drain simultaneously required four pulse channels and two sets of switches. ***Figure 6*** shows a more complicated waveform used for testing phase-change memory. The red boxes on the waveform represent measurements. Note that the entire waveform, consisting of four pulses of varying widths and heights, is output by a single Model 4225-PMU channel, using 16 segments out of a maximum of 2048.

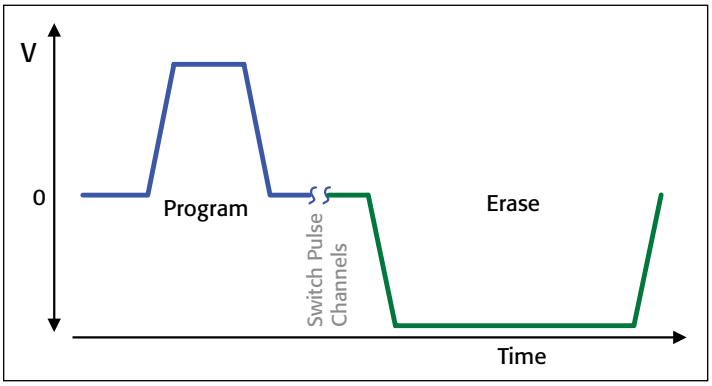

Figure 5. Flash memory Program and Erase waveform: two pulses, three levels. Traditional pulse generators can only output two level pulses, so flash testing required two pulse channels for each test pin and a time-costly switch to apply the second (negative) pulse to the test device. Note that this setup is only for one device terminal. For a typical pulsing on the gate and drain, this setup would have to be duplicated.

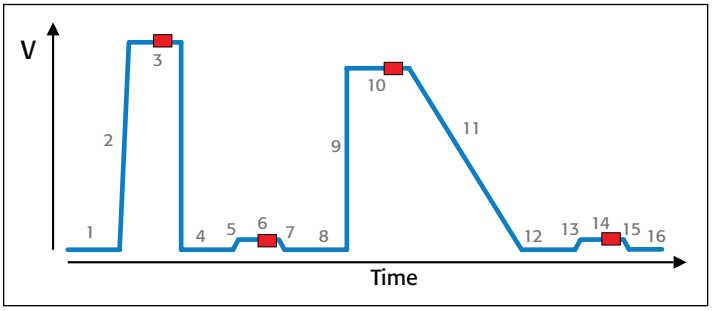

Figure 6. Multi-level pulse waveform consisting of 16 linear voltage segments (gray numbers) and four measurements (red boxes). New pulse source hardware allows creating multi-segment voltage waveforms to provide several pulses within a single waveform, as well as adding integrated V and I sampling (not shown).

Making Connections to the Device

Figure 7 shows the general method for connecting to a two-terminal device using two Model 4225-RPM Remote Amplifier/Switches. The Model 4225-RPM is an optional item for the dual-channel Model 4225-PMU Ultra-Fast I-V Module and is necessary for NVM characterization. Specific interconnect diagrams are shown for each of the three devices in the *NVM_Examples* project discussed later in this application note. Note that the ground connection for NVM devices, which is usually necessary on memory cells that use a transistor as the selection device, should be made to the local shield and the shields for each channel should be connected together (***Figure 8***). These shield connections are important to ensure the relatively high bandwidth required for the fast transitions and narrow pulses required for today's emerging NVM technologies.

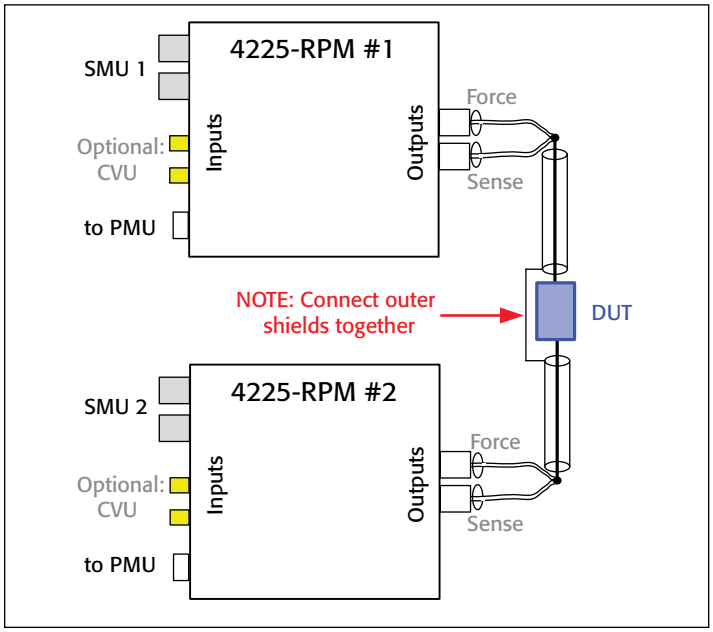

Figure 7. Connection to two-terminal test device.

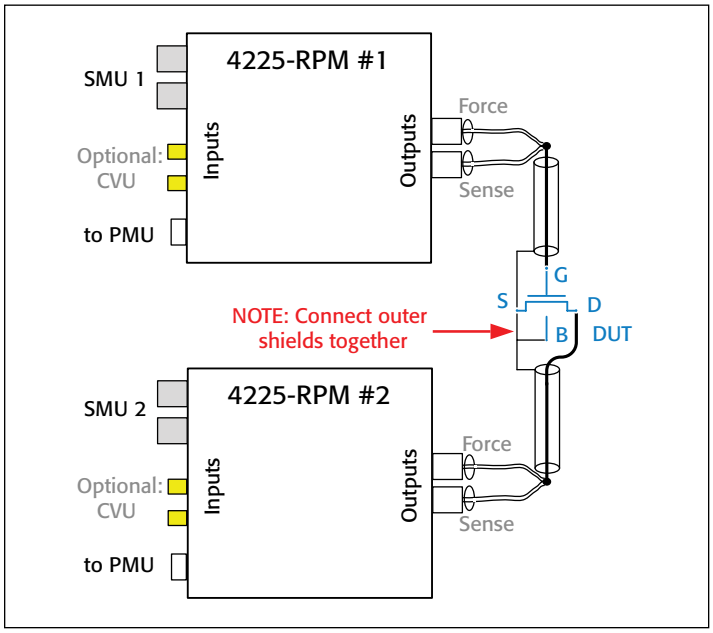

Figure 8. Connection to four-terminal test device with two Model 4225-RPMs.

It is possible to connect a two-terminal device using a single channel, with the low side of the device connected to the shield, or ground return, of the channel. This is the traditional way to test a simple two-terminal device and is reasonable for DC characterization. However, because of transient effects during the pulse, using two channels on a two-terminal device provides better results. See the "Optimizing Measurements" section for additional information.

Using the KTEI Software to Control the Models Model 4225-PMU and Model 4225-RPM for NVM Testing

A set of example tests for NVM characterization is included with KTEI 8.2 or higher, contained in the *NVM_Examples* project (in the *C:\sModel 4200\kiuser\Projects_Memory folder*). This project (***Figure 9***), which includes tests and data for flash, PRAM, and FeRAM devices, demonstrates the capabilities of the Model 4200-SCS and particularly the Model 4225-PMU with the Model 4225-RPM. The Model 4225-PMU/4225-RPM combination provides the fundamental pulse and transient I-V test capabilities to investigate and characterize a wide range of NVM materials and devices. A brief explanation of the user test modules (UTMs) follows.

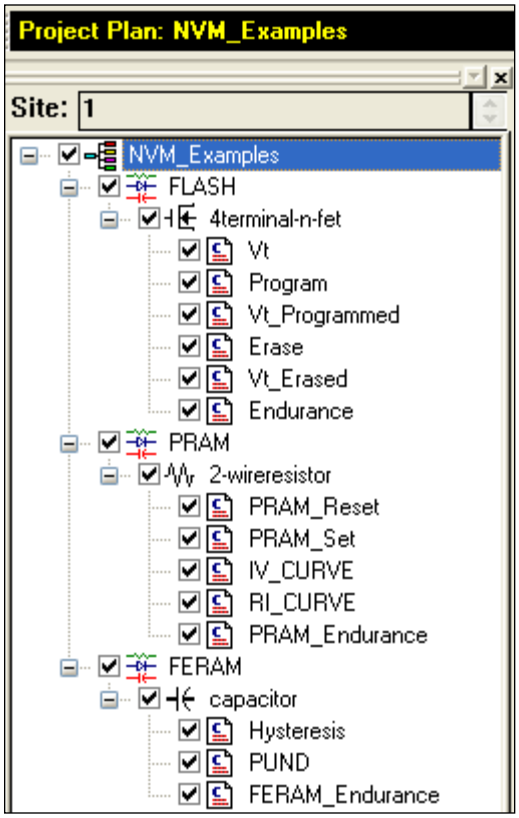

Figure 9. The devices and tests included in the *NVM_Examples* project for the Keithley Model 4200-SCS.

Table 2. User modules in the *nvm* user library.

User Module	Used in	Description
doubleSweep.c	N/A	Outputs one or two V-shaped waveforms while sampling the voltage and current. Also calculates the accumulated charge. Requires one Model 4225-PMU with two Model 4225-RPMs.
doubleSweepSeg.c	PRAM, FeRAM	Similar to *doublesweep* but returns the waveform data split into segments used by the PRAM I-V sweep. Also calculates the accumulated charge, used in FeRAM hysteresis test. Requires one Model 4225-PMU with two Model 4225-RPMs.
flashEndurance.c	Flash	Performs the pulse stress and DC measure cycling. Applies the maximum number of requested waveforms while measuring every log10 waveform count. The stress waveform is the typical program and erase and the measurement is performed by the SMU instruments. Requires two SMU instruments and one Model 4225-PMU with two Model 4225-RPMs.
flashProgramErase.c	Flash	Applies the program and erase pulse waveform while sampling the voltage and current. Can choose to output both program and erase or just one pulse. Requires one Model 4225-PMU with two Model 4225-RPMs.
nvmDebug.c		This utility module does not test but saves intra-test status information to a file (*C:\nvmlog.txt*). This is useful for debugging test issues, especially when modifying existing test modules or writing new ones.
pramEndurance.c	PRAM	Performs the stress and measure cycling for phase-change memory. The test uses the RESET-SET waveform for stresses and every log10 count uses a RESET-measure-SET-measure to obtain the resistance measurements post-RESET and post-SET. Requires one Model 4225-PMU with two Model 4225-RPMs.
pramSweep.c	PRAM	This outputs the RESET-measure-SET-measure waveform while sampling the voltage and current. Requires one Model 4225-PMU with two Model 4225-RPMs.
pulse_test.c	Flash, PRAM, FeRAM	This is the underlying test routine used by all of the tests. Requires one Model 4225-PMU with two Model 4225-RPMs. For additional information, see the *read_me.rtf* file in *C:\s4200\kiuser\usrlibs\nvm*.
pundEndurance.c	FeRAM	Performs the stress and measure cycling for FeRAM. The stress waveform is output a maximum number of times and is interrupted on a log10 basis to obtain the PUND and Psw and Qsw extractions.The stress waveform is the PUND waveform and the measure is the two V-pulses controlled by *doubleSweepSeg*. Requires one Model 4225-PMU with two Model 4225-RPMs.
pundTest.c	FeRAM	This test outputs the four-pulse PUND waveform while sampling voltage and current. The routine extracts the P, U, N, and D values from the waveform. Requires a Model 4225-PMU with two Model 4225-RPMs.
reramSweep.c	ReRAM	This test outputs 2 pulses, one pulse to be used for "SET" and another for "RESET". Pulses can be generated by the SMU instrument or by the PMU. SMU instrument sweeps are slow (ms range and higher) and PMU sweeps are fast (ns to ms range). Both voltage sweeps (PMU and SMU instrument) can be used with current limit. Requires one PMU with 2 RPMs and 2 SMU instruments.
reramEndurance.c	ReRAM	Performs the stress and measure cycling for ReRAM memory. The test uses the RESET-SET waveform for stresses and every log10 count uses a RESET-measure-SET-measure waveform to obtain the resistance measurements for the post-RESET and post-SET states. Requires one PMU with 2 RPMs and two SMU instruments.
util.c		This utility module does not test but has support routines for the other tests, such as hardware initialization, calculation of total points, and calculation of maximum allowable sample rate.
vt_ext.c	Flash	Performs a V_G-I_D sweep and extracts the voltage threshold (V_T). Requires two SMU instruments.

The tests in the *NVM_Examples* project are UTMs, which are customized for each memory type but share an underlying approach to minimize the effort required to accommodate additional NVM materials or device types. All of the UTMs used in this project are contained in the *nvm* user library (***Table 2***). These modules are used in *NVM_Examples* project, but they may also be added to another project. If additional capabilities or test types are required, the source code for the modules is included with the Model 4200-SCS and may be modified by using the Keithley User Library Tool (KULT) with the optional compiler (order number: 4200-Compiler).

Flash Testing

Flash cells are the dominant type of NVM and because they are implemented on the foundation of MOSFET transistors, they have standard source, gate (actually, control gate or CG), drain, and bulk/substrate connections (***Figure 12***). Fowler-Nordheim current tunneling through gate oxide and hot carrier injection represent the two standard methods for storing and removing charge from the floating gate (***Figure 10***). These methods are degradation mechanisms of standard (non-NVM) MOSFET transistors, which also explains the limited endurance of flash memory. Because the majority of the NVM market is Flash, this is an active area for research and development [3, 4].

Initial flash memory characterization usually consists of determining the appropriate values for the voltage pulse height and the pulse width to provide the target threshold values for the program and erase states. Instead of the traditional one-bit (1/0) cell, most modern flash memory utilizes two or three bits per cell, which maps to four or eight unique V_T levels. The increasing number of V_T levels requires more precise pulse level performance and higher pulse voltages.

There are six UTMs for the flash device in the *NVM_Examples* project (***Figure 11***), which is located in the *C:\sModel 4200\kiuser\Projects_Memory* folder. These tests support a stand-alone NAND or NOR cell. There are three tests that measure the

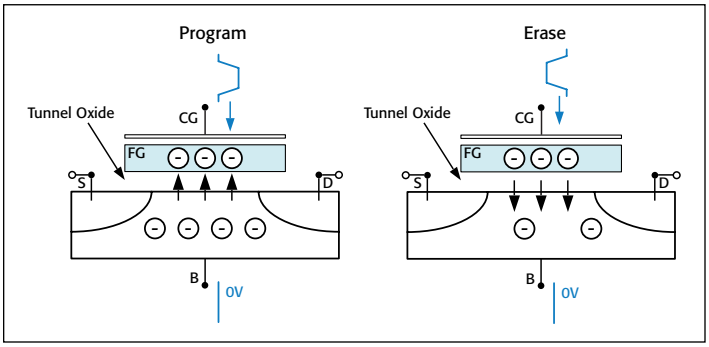

Figure 10. Flash memory structure, showing program and erase conditions for Fowler-Nordheim tunneling.

V_T of the flash memory transistor, two that apply program or erase pulses, and one endurance test. The connection to a stand-alone flash memory cell is shown in ***Figure 12***. In these tests, only two pulse I-V channels are used, so both the source and bulk are connected to the Model 4225-RPM shields. These tests require the following hardware:

- Model 4200-SCS with KTEI 8.2 or higher
- Two or more SMU instruments, either medium-power Model 4200-SMUs or high-power Model 4210-SMUs
- One Model 4225-PMU with two Model 4225-RPMs

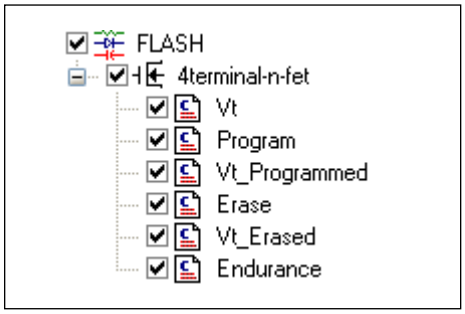

Figure 11. Tests for the flash device in the *NVM_Examples* project.

The three *Vt* tests are the same and use two SMU instruments to measure the V_T of the flash transistor. The *Program* and *Erase* tests apply pulse waveforms to program and erase a stand-alone flash memory cell. Because the Model 4225-PMU has integrated high speed sampling, the *Program* and *Erase* tests also capture the voltage and current waveforms (***Figure 13***). Both of these tests use Fowler-Nordheim tunneling to perform the charge transfer, so the drain voltage = 0V and the graphs show the gate voltage and current only. However, both the gate and drain current and voltages are measured in each test, so they can be displayed if desired.

Measuring the current while pulsing was not previously practical. Because the tunneling current is non-linear with the applied voltage, the measured current provides additional information on how close the voltage is to providing a sufficient electrical field for programming or erasing. The transient current provides

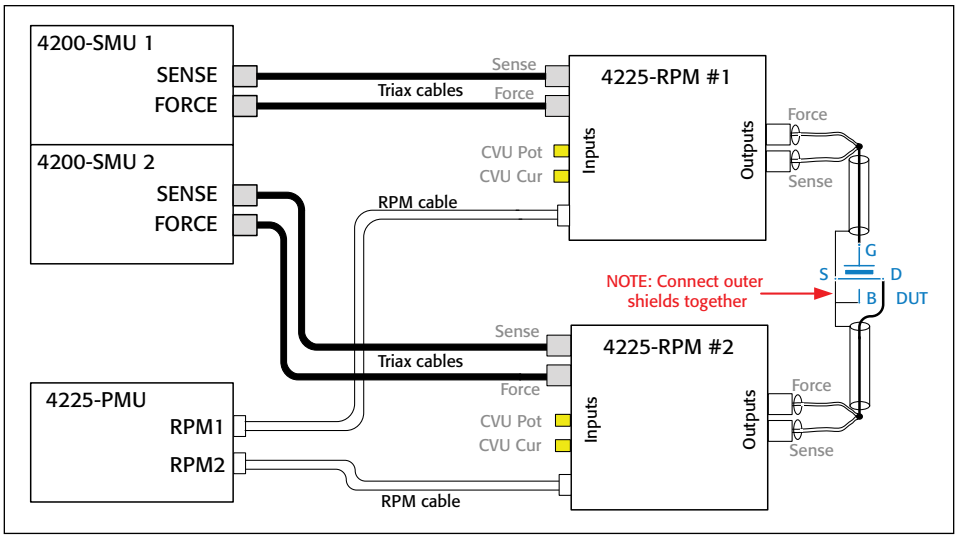

Figure 12. Connection to four-terminal floating gate flash device.

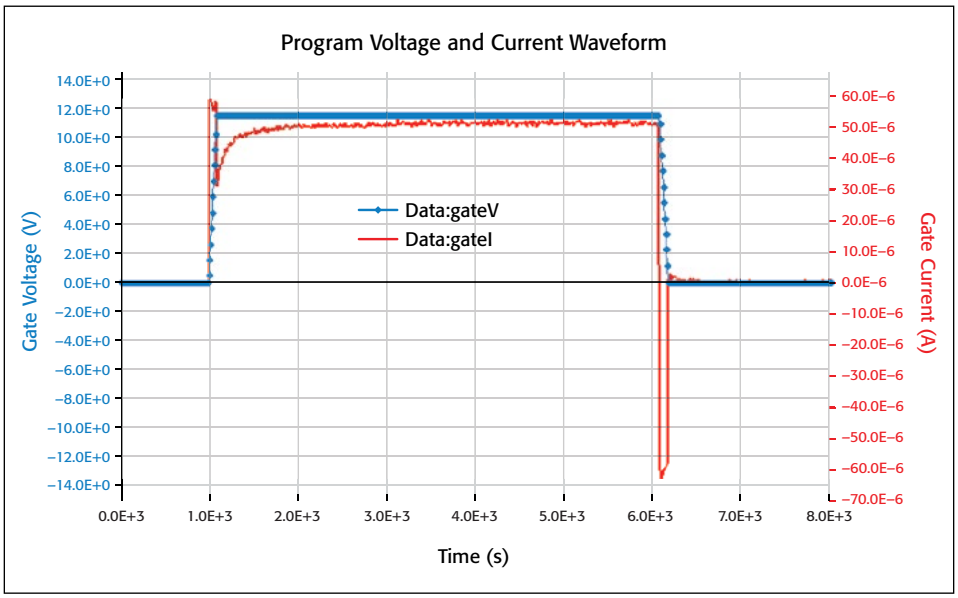

Figure 13. Pulse current and voltage waveforms for a *Program* pulse on a NAND cell using a Model 4225-PMU with Model 4225-RPMs. Note the capacitive charging and discharging current during the pulse transitions (see "Optimizing Measurements" for an explanation). This graph is from the *Flash Program* test (user module *flashProgramErase*).

information on the dynamic current flow and overall charge transfer. The use of the transient current and voltage information can be correlated to the DC-based V_T results to provide additional understanding of the program and erase processes, which may be unique for different structures, dimensions, and materials. The results of the program and erase pulses are in the *Vt_Programmed* and *Vt_Erased* tests (***Figure 14***).

The last test is *flashEndurance*, where the program+erase waveform is applied in increasing log intervals and then the program and erase V_T are measured and plotted (***Figure 15***).

Flash Test Modules

There are three modules for testing of either NAND or NOR floating gate devices: *flashProgramErase*, *vt_ext*, and *flashEndurance*. The *flashProgramErase* module applies a pulse waveform of either the program pulse, the erase pulse, or both. The *vt_ext* module performs a V_G-I_D sweep, using the

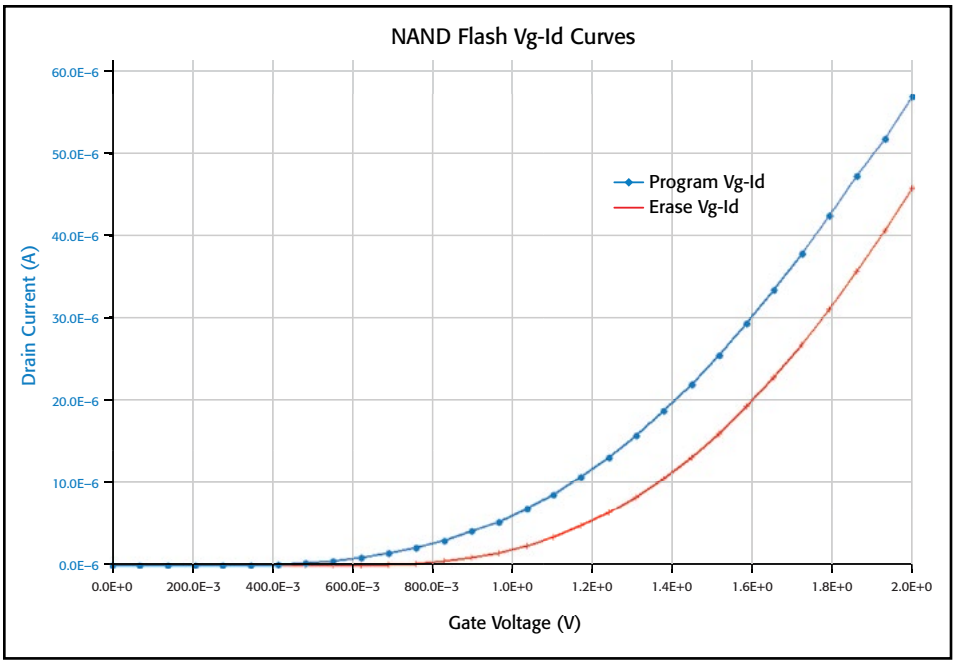

Figure 14. V_T sweeps for a programmed and erased cell taken with SMUs, from the *Vt_Erased* UTM (user module *vt_ext*). In this graph, the difference in the V_T after program and after erase is about 180mV.

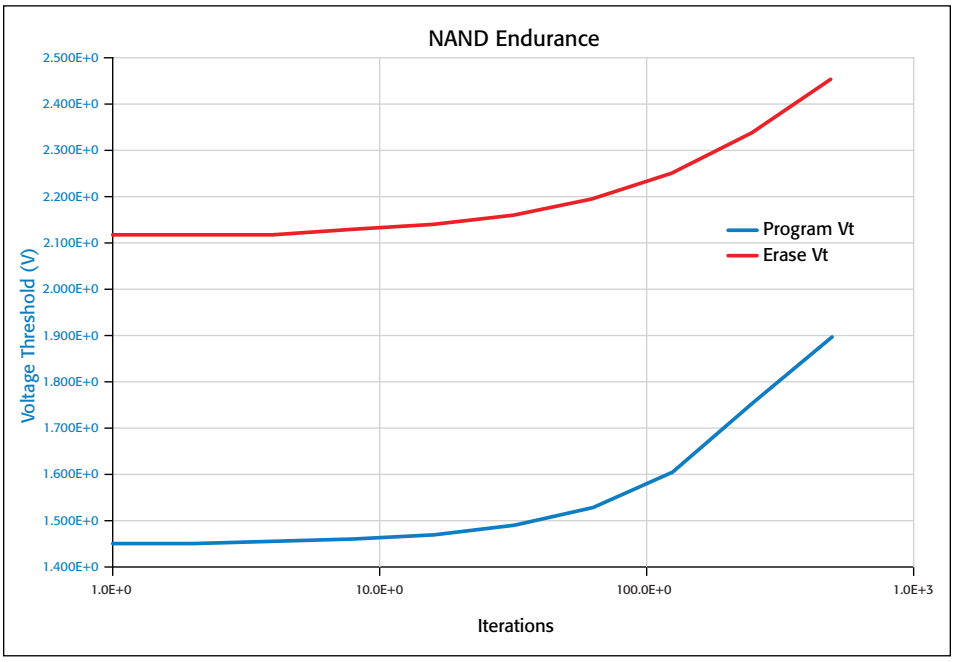

Figure 15. NAND flash endurance results from the *Flash UTM Endurance* test (user module *flashEndurance*).

SMU instruments, and extracts the threshold voltage. The *flashEndurance* module applies an increasing number of program+erase waveforms while periodically measuring (on a log interval of the number of waveforms applied) the program and erase voltage thresholds and plotting them.

For initial characterization and determination of appropriate pulse parameters for program and erase, the *flashProgramErase* and *vt_ext* modules allow for adjustments of the pulse parameters, then the measurement of the voltage threshold using the SMU instruments. Note that the Model 4225-RPM switching capability is used to apply the pulses or the SMU instrument voltages alternately to the device, so no recabling is required.

The *flashProgramErase* module uses the Model 4225-PMU and the Model 4225-RPMs to output single-pulse or dual-pulse waveforms using the Segment ARB feature of the Model 4225-PMU. The module supports the two channels of the Model 4225-PMU, so unique pulse voltages can be output for the gate and drain. This module also measures the waveforms for diagnostic purposes, such as verifying pulse shape performance and proper voltage levels.

Setting Up the Parameters in the *flashProgramErase* Module

Table 3 lists the input parameters for the *flashProgramErase* module. This module has the settings for both the gate and drain program and erase pulses. It uses both channels of the Model 4225-PMU, each connected to a Model 4225-RPM (***Figure 12***). This module defines and outputs Program and Erase waveforms as shown in ***Figure 16.*** To measure the voltage threshold after sending the program and/or erase pulses, use the *vt_ext* module, described in the next section.

If only one pulse is desired, set the other pulse levels to 0. For example, if the erase pulse is not desired, set drainE = gateE = 0. This will make the erase portion of the waveform stay at 0V.

For Fowler-Nordheim tunneling, usually the drain voltage is 0V, and just the gate pulse (gateP), is set to either pushing charge into the floating gate (gateP = +V) or clearing the charge from the floating gate (gateE = –V). For the hot carrier injection method, the drain voltage is positive, creating the field in the channel necessary to create the hot carriers.

Setting Up the Parameters in the *vt_ext* Module

Table 4 lists the input parameters for the *vt_ext* module. This module performs a V_{GS}-I_D sweep and returns transistor

threshold voltage using the maximum g_m method, where the threshold voltage is defined as:

$$V_T = V_{G\ MAX} - I_{D\ MAX} / g_{m\ MAX} - 1/2 * V_{DS}$$

$V_{G\ MAX}$ is the maximum gate voltage

$I_{D\ MAX}$ is the maximum drain current

$g_{m\ MAX}$ is the transconductance (g_m) at the maximum g_m.

The number of points in the V_T sweep is set by *vgs_pts* and *ids_pts*, *gm_pts*. Note that all three parameters must be set to the same value (*vgs_pts* = *ids_pts* = *gm_pts*). Typically, a 30-point sweep is sufficient to obtain a reliable V_T.

Note that this module assumes that *DrainSMU* is connected to RPM2 and *GateSMU* is connected to RPM1. As shown in ***Figure 12***, the test device Source and Bulk connections are to the RPM shield, so the appropriate setting in *vt_ext* are SourceSMU = BulkSMU = "".

Table 3. Parameters in the *flashProgramErase* module.

Parameter	Range	Description
gateP	–40V to +40V	Gate Program Pulse Voltage
drainP	–40V to +40V	Drain Program Voltage
widthP	20ns to 1s	Program Pulse top width
gateE	–40V to +40V	Gate Erase Pulse Voltage
drainE	–40V to +40V	Drain Erase Pulse Voltage
widthE	20ns to 1s	Erase Pulse top width
riseT	20ns to 33ms	Pulse transition time, both rise and fall for Program, Erase
delayT	20ns to 1s	Pulse delay time, before Program pulse and between the Program and Erase pulses
loops	1 to 10^{12}	Number of times to output the ProgramErase waveform

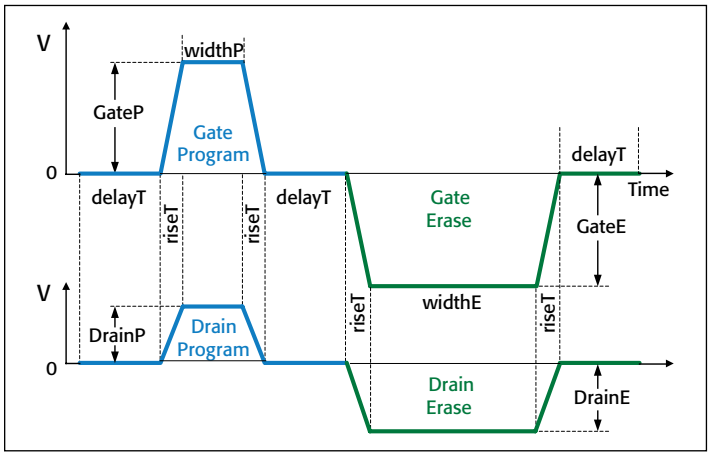

Figure 16. Waveform parameters for the *flashProgramErase* module.

Table 4. Parameters in the *vt_ext* module.

Parameter	Range	Description
DrainSMU	SMU1 to SMUn	SMU instrument for DUT Drain
GateSMU	SMU1 to SMUn	SMU instrument for DUT Gate
SourceSMU	SMU1 to SMUn	SMU instrument for DUT Source, if used
BulkSMU	SMU1 to SMUn	SMU instrument for DUT Bulk, if used
vlow	–40V to +40V	Starting sweep voltage for the Gate SMU instrument
vhigh	–40V to +40V	Final sweep voltage for the Gate SMU instrument
vds	–40V to +40V	Drain bias voltage for the Drain SMU instrument
vbs	–40V to +40V	Pulse delay time, before Program pulse and between the Program and Erase pulses
vgs_pts	10 to 100	Number of points in the Vgs-Id sweep
ids_pts	10 to 100	Number of points in the Vgs-Id sweep
gm_pts	10 to 100	Number of points in the Gm array
vt		Resulting voltage threshold from the max Gm calculation

Setting Up the Parameters in the *flashEndurance* Module

Table 5 lists the input parameters for the *flashEndurance* module. This module has the settings for both the gate and drain program and erase pulses and the maximum number of stress loops. It uses both channels of the Model 4225-PMU, each connected to a Model 4225-RPM (***Figure 12***). This module outputs a number (*max_loops*) of Program and Erase waveforms (***Figure 16***) to the test device. The module will use log10 stress counts from the *max_loops* and the desired number of iterations in *iteration_size* to determine how many program+erase pulse waveforms to apply for each stress interval. After each stress interval, the *vt_ext* is run, once after the program pulse is applied and once after erase. Note that *iteration_size*, *vtE_size*, and *vtP_size* must have the same value (*iteration_size* = *vtE_size* = *vtP_size*).

Table 5. Parameters in the *flashEndurance* module.

Parameter	Range	Description
gateP	–40V to +40V	Gate Program Pulse Voltage
drainP	–40V to +40V	Drain Program Voltage
widthP	20ns to 1s	Program Pulse top width
gateE	–40V to +40V	Gate Erase Pulse Voltage
drainE	–40V to +40V	Drain Erase Pulse Voltage
widthE	20ns to 1s	Erase Pulse top width
riseT	20ns to 33ms	Pulse transition time, both rise and fall for Program+Erase pulses
delayT	20ns to 1s	Pulse delay time, before Program pulse and between the Program and Erase pulses
max_loops	1 to 10^{12}	Number of times to output the Program+Erase waveform to stress the test device
vds	–40V to +40V	V_T sweep drain bias voltage for the Drain SMU
vgsstart	–40V to +40V	V_T sweep starting sweep voltage for the Gate SMU
vgsstop	–40V to +40V	V_T sweep final sweep voltage for the Gate SMU
vtP_size	2 to 100	Number of points in the V_{GS}-I_D sweep after the Program pulse
vtE_size	2 to 100	Number of points in the V_{GS}-I_D sweep after the Erase pulse
Iteration_size	2 to 100	Number of times to measure the V_T during the *max_loops* stress

PRAM Material Testing

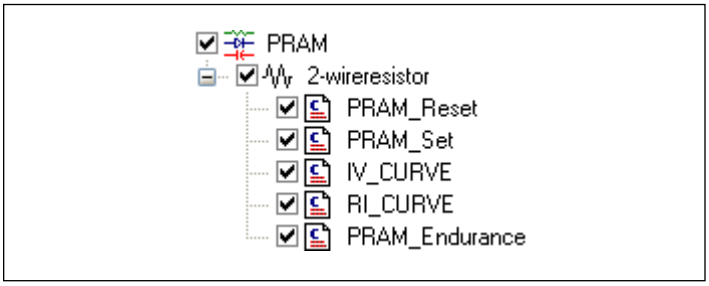

Figure 17. Tests for the PRAM two-terminal device in the *NVM_Examples* project.

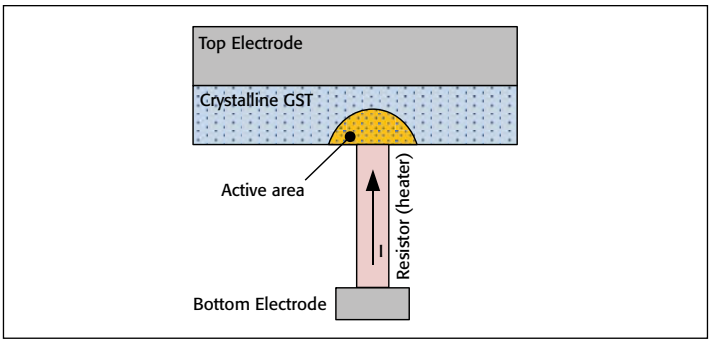

Figure 18. GST [Germanium (Ge), Antimony (Sb), and Tellurium (Te)] structure.

Phase-change memory (PRAM, PCRAM, or PCM) cells are made of a chalcogenide alloy (i.e., with at least one element from the VI group of the periodic table of the elements, plus one element each from the V and IV groups). These same types of materials are also widely used in the active layers of rewritable optical media such as CDs and DVDs. PRAM is one type of resistive memory. Other types of resistive memory include OxRRAM and TMO-RRAM (both are types of Redox RAM) and cation-based, conductive-bridge memory (CBRAM). ***Figure 17*** shows the tests included for phase-change memory testing in the *NVM_Examples* project (in the *C:\sModel 4200\kiuser\Projects_Memory* folder).

Through the application of heat in the form of an electrical pulse (or a laser pulse in CDs/DVDs), PCM cells can be switched rapidly from an ordered crystalline phase (which has low resistance) to a disordered, amorphous phase (which has much higher resistance). The switch from the crystalline to the amorphous phase and back is triggered by melting and quick cooling (or a slightly slower process known as re-crystallization). GST [germanium (Ge), antimony (Sb), and tellurium (Te)], with a melting temperature from 500° to 600°C, has emerged as one of the most promising materials for PCM devices (***Figure 18***).

These devices can store binary data because of the differing levels of resistivity of the crystalline and amorphous phases of these alloys. The high resistance amorphous state represents a binary 0; the low resistance crystalline state represents a 1. Multiple resistive levels will permit multi-bit PCM, which has been demonstrated, allowing PCM to scale and provide lower cost-per-bit. [5, 6]. These states are stable over time, which is important for any commercial application [7].

In the amorphous phase, the GST material has short-range atomic order and low free electron density, which means higher resistivity. This is sometimes referred to as the RESET phase because it is usually formed after a RESET operation, in which the temperature of the cell is raised slightly above the melting point, then the material is suddenly quenched to cool it. The cooling rate is critical to the formation of the amorphous state. If the rate is too slow, then the material will be less amorphous. For so-called "slow materials," the cooling rate is about 30 nanoseconds; for "'fast materials," it is in the range of single nanoseconds or faster [8]. The fall time of the pulse can be slower than the required speed; what is important is the fall rate at the top of the pulse, when the cell cools from melting point to crystallization. After reaching crystallization temperature, the crystalline order is frozen. For example, the pulse fall time may be 20ns, but it might take 5ns to go from T_{MELT} to $T_{CRYSTALLIZE}$. In addition, some PRAM structures have a "Select Diode" or "Protection Diode" integrated in series with the PRAM cell. In addition to some drawbacks for the I-V curve, this diode will make the effective fall time shorter. The current flowing through a diode is exponentially dependent on the voltage, so a small decrease in the voltage results in a dramatic reduction in the current flowing through the diode, especially at small currents (~<50μA). Therefore, when testing devices with the series selection diode, the pulse fall time is not as critical for small current test devices and permits testing with standard pulse I-V instrumentation, such as the models 4225-PMU and 4225-RPM.

Much like other types of NVM technologies, a PCRAM cell must be formed before it displays the consistent switching necessary to be a memory element. One way to explain the forming process is that it creates the active area of the PCRAM cell. The active area is the portion of the chalcogenide material that transitions between the amorphous and crystalline states. ***Figure 18*** shows a half-circle shape that represents the active area and is the result of the forming process. The goal of the forming process is reproducible cycling between the SET and RESET states. One challenge to testing a new or unknown cell is to determine the appropriate pulse parameters (amplitude, rise/fall, width) for the RESET and SET pulses. This is usually an iterative process, first starting with a reasonable RESET pulse, then optimizing the SET pulse. The *PRAM_Reset* and *PRAM_Set* tests are useful for this initial determination of the pulse parameters. Just as with flash memory, it is possible to over-stress the cell and permanently damage it. Because the RESET voltage is the largest, the search for the appropriate RESET voltage must be done with care.

There are five UTMs for testing phase-change memory devices in the *NVM_Examples* project (***Figure 17***). The first test applies a waveform with a RESET pulse and measure R pulse to the PRAM device (***Figure 20***). The second test is similar to the first test but applies a waveform consisting of a SET pulse followed by a measure pulse. There is an I-V sweep test that shows the switching effect (***Figure 22***). The next test shows the typical R-I

curve, which is the resistance of the cell vs. the current (R-I) of the SET pulse (***Figure 24***). The last test is an endurance test, showing the change in the SET resistance vs. the number of RESET-SET waveforms (***Figure 26***).

These tests require the following hardware:

- Model 4200-SCS with KTEI 8.2 or higher
- One Model 4225-PMU with two Model 4225-RPMs

The connection diagram is shown in ***Figure 19***. To obtain the best possible measurements, the connection uses the source high, measure low method described in the "Optimizing Measurements" section. No SMUs are used in these tests, although adding SMU tests is possible.

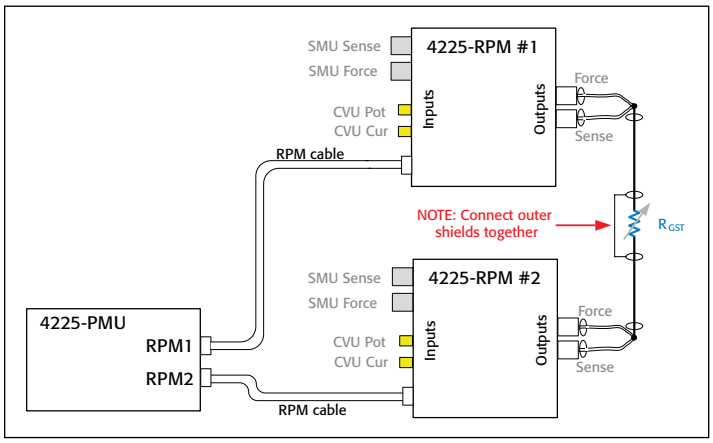

Figure 19. Connection diagram for PRAM tests. Note that the PRAM tests included with *NVM_Examples* do not use the SMUs or CVU.

The *Reset* test applies a two-pulse RESET and measure waveform to the test device and captures the voltage and current waveforms (***Figure 20***). This transient response data is useful to determine the resistance of the device and the degree of reset. This test and the *Set* test are used to determine the proper voltage and pulse width for reset and set pulses as well as a way to send a reset-only or set-only waveform to the test device. Use these tests to optimize the RESET and SET pulse parameters before performing an endurance test.

The I-V sweep test uses a single inverted-V-shaped pulse to capture the PRAM switching characteristics. Because this test uses a pulse with V and I sampling, there are two ways to view the data. ***Figure 21*** shows the waveform data, with I and V plotted vs. time. This is not the typical way to display the characteristics but shows how the test is performed. The second graph (***Figure 22***) shows the typical PRAM I-V curve (current vs. voltage).

The R-I curve is a typical phase-change measurement. The SET pulse voltage is increased while the RESET and SET resistance values are being measured. ***Figure 23*** shows the four-pulse waveform for one point in the R-I curve. For the curve, spot means are taken (green boxes) to capture the measurements for the R-I curve.(***Figure 24***). Note that the RESET resistance is traditionally displayed with the SET resistance, even though the RESET pulse is not changing throughout the sweep, causing the

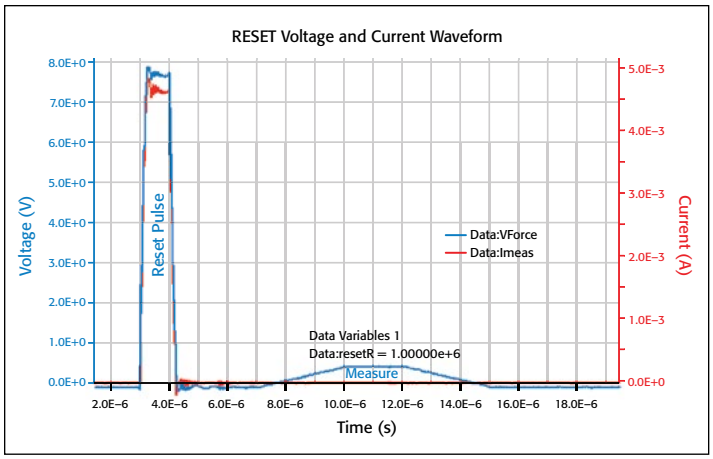

Figure 20. PRAM RESET waveform generated and measured by the Model 4225-PMU with Model 4225-RPMs (user module *pramSweep*).

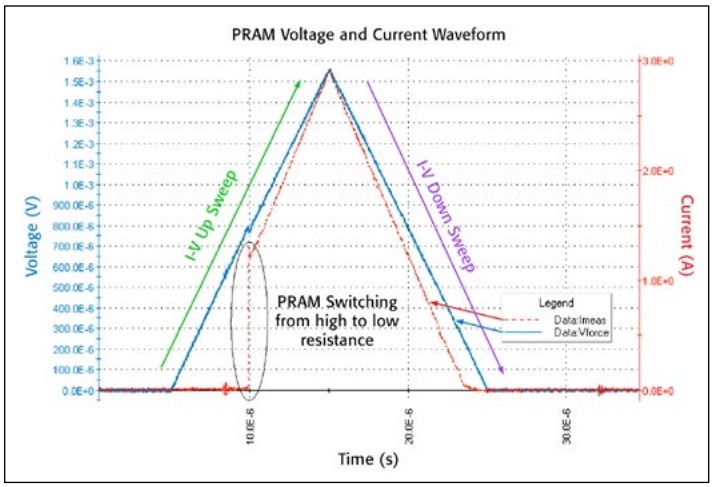

Figure 21. I-V waveform from the *PRAM IV_CURVE* test generated and measured by the Model 4225-PMU with Model 4225-RPMs (user module *doubleSweepSeg*).

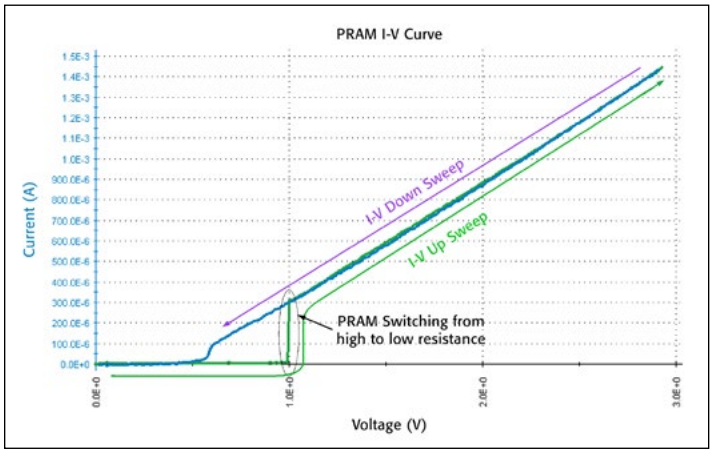

Figure 22. I-V curve from the *PRAM IV_CURVE* test generated and measured by the Model 4225-PMU with Model 4225-RPMs. This test uses the same data shown in Figure 21, but the curve plots I vs. V (user module *doubleSweepSeg*).

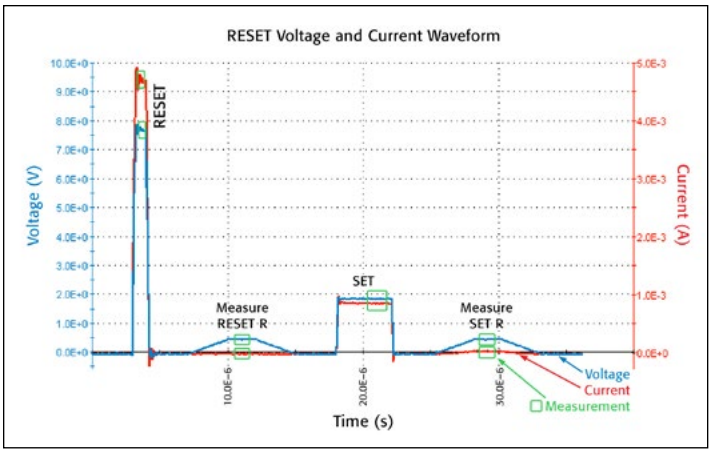

Figure 23. R-I RESET-Measure-SET-Measure waveform generated and measured by the Model 4225-PMU with Model 4225-RPMs (user module *pramSweep*). This graph shows the voltage (blue, left y-axis) and current (red, right y-axis) waveforms. There are four pulses within this waveform. The first pulse is the RESET pulse, which resets the PRAM material, putting it into a high resistance, amorphous state. The second pulse measures the resistance of the RESET state. The third pulse is the SET pulse, which will put the material into a low resistance, crystalline state. The fourth and last pulse measures the resistance of the material in the SET state. *Figure 24* is an R-I curve that results from sweeping the SET pulse height and plotting the results in the R-I curve.

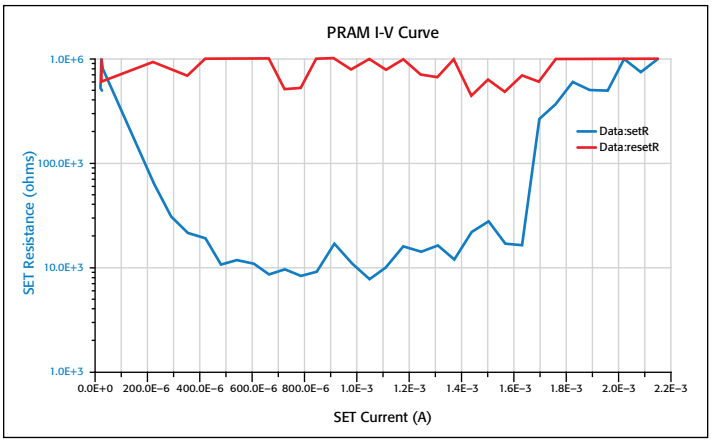

Figure 24. R-I curve shows the resistance variation of the SET state resistance generated and measured by the Model 4225-PMU with Model 4225-RPMs (user module *pramSweep*). This test uses the data captured from the tops of the pulses shown in *Figure 23*.

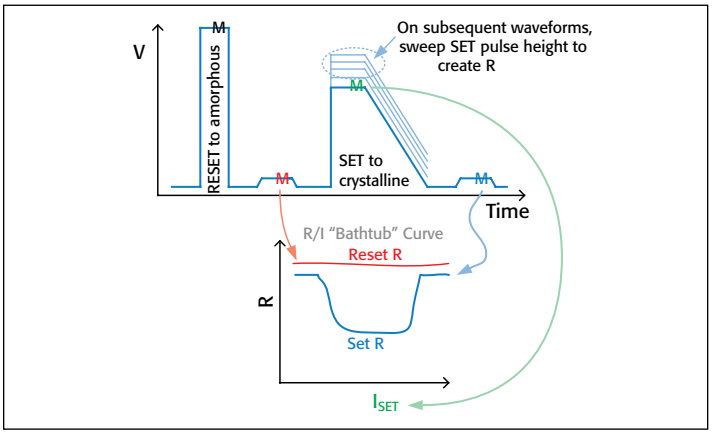

Figure 25. Diagram explains how the various measurements are used to define the R-I curve. The SET curve is swept while the RESET resistance (red M), SET current (green M), and SET resistance (blue M) are measured.

RESET R to be a straight line. Plotting the RESET R does indicate if the RESET pulse is adequately resetting the material after each SET pulse. ***Figure 25*** shows how the waveform measurements map to the R-I results. Some test systems may use SMU instruments for the resistance measurements, but this requires additional switching and much longer test times. The PMU+RPM combination measures the voltage and current simultaneously at multiple points in the test, providing flexibility while ensuring that the proper measurements are made.

The PRAM endurance test applies the RESET+SET waveform (***Figure 23***) and measures the SET resistance every log n iterations. ***Figure 26*** shows an example of an endurance curve. The routine also measures the RESET resistance, so it can also be graphed if desired.

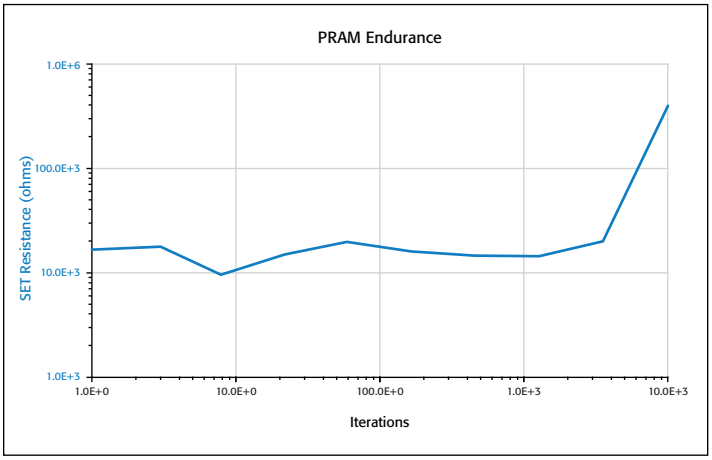

Figure 26. PRAM endurance curve generated and measured by the Model 4225-PMU with Model 4225-RPMs (user module *pramEndurance*).

PRAM Test Modules

There are three modules for testing of phase-change materials or devices: *doubleSweep*, *pramSweep,* and *pramEndurance*, using one Model 4225-PMU and two Model 4225-RPMs. The *doubleSweep* module applies a single V-shaped pulse while sampling the voltage and current.

Setting Up the Parameters in the *doubleSweep* and *doubleSweepSeg* Modules

Table 6 lists the input parameters for the *doubleSweep* module, which performs a transient I-V sweep by plotting the I-V samples from one or two V-shaped pulses (***Figure 27***) using one Model 4225-PMU and two Model 4225-RPMs. This module is useful for a variety of NVM technologies, whether unipolar (V1 and V2 +V) or bipolar (V1 = +V, V2 = –V). For PRAM, only the first pulse is used, so V2=0.

Two waveforms are returned from this test—the voltage waveform on RPM1 and the current waveform from RPM2. (See connection diagram, ***Figure 19***.) Note that the V1 and V2 can be of either polarity. The base voltage for the pulses is 0V. The returned data is the voltage from RPM1 (V_{FORCE}) and the current from RPM2 (I_{MEAS}). The data can be plotted vs. time (***Figure 21***,

showing V1 only) or as I-V (***Figure 22***). The difference between *doubleSweep* and *doubleSweepSeg* is that the *doubleSweepSeg* module returns each up and down segment as a separate array, which allows plotting each portion of the curve in a separate color to help distinguish the contributions of each to hysteresis or other relatively complicated I-V results. An example of this routine is shown in ***Figure 22***, with the upsweep in green and the downsweep in blue.

For FeRAM, both pulses are used (***Figure 31***). This module is also useful for material characterization for ReRAM, CBRAM, and other conductive bridge or ion transport technologies, many based on transition metal oxide (TMO) materials. This test returns data that can be used to create "butterfly" curves, which is the standard technique for TMO ReRAM characterization.

Setting up the Parameters in the *pramSweep* Module

Table 7 lists the input parameters for the *pramSweep* module. This module performs a SET voltage amplitude sweep from setStartV to setStopV, with the number of steps set by the parameter iteration. The waveform diagram is shown in ***Figure 28***. At each step in the sweep, several measurements are extracted (green boxes in ***Figure 28***) from the voltage waveform on RPM1 and the current waveform from RPM2: RESET resistance (measurement of cell resistance after the RESET pulse), SET resistance (measurement of cell resistance after the SET pulse), and Set V and Set I (current and voltage at the top of the SET pulse). Measurements are extracted from 30% to 90% of the pulse top (green boxes on ***Figure 28***), which avoids the current settling issue and provides a relatively wide window to reduce the noise in the measurements. In addition to the scalar measurements for each sweep (Reset R, Set V, Set I, Set R), this routine also returns one current and voltage waveform from one step of the sweep. The choice of which waveform is captured and returned is set by the value in *iteration*.

To enhance the visibility of the changes in the resistances, values >1MΩ are set equal to 1MΩ. This prevents the occasional current measurements at the noise floor of the range from causing a very large R value (5MΩ to hundreds of mega-ohms). Note that the size parameters (*setR_size*, *resetR_size*, *setV_size*, *setI_size*) for the pulse top measurements must all be the same value (*setR_size* = *resetR_size* = *setV_size* = *setI_size*). Similarly, for the sample waveform arrays, the sizes must be set to the same value (*VForce_size* = *IMeas_size* = *Time_size*).

Table 6. Parameters in the *doubleSweep* and *doubleSweepSeg* modules.

Parameter	Range	Description
riseTime	20ns to 33ms	Transition time for the pulses
V1	–10V to +10V	Voltage amplitude for first pulse
V2	–10V to +10V	Voltage amplitude for second pulse
Irange1	100nA to 10mA	Current measure range for RPM1 (RPM1 forces voltage)
Irange2	100nA to 10mA	Current measure range for RPM2 (RPM2 measures current)

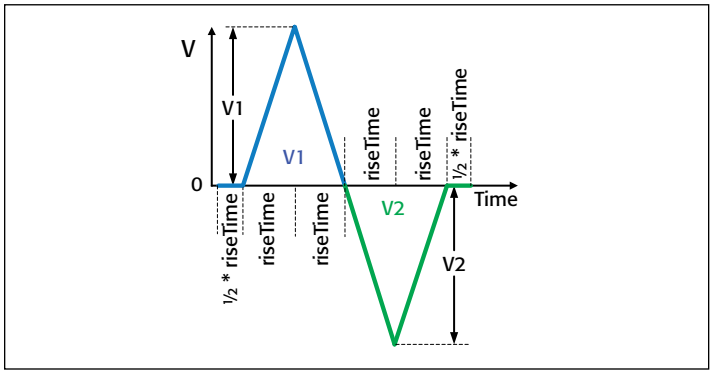

Figure 27. The multi-pulse waveform of *doubleSweep*.

Setting Up the Parameters in the *pramEndurance* Module

Table 8 lists the input parameters for the *pramEndurance* module. This module stresses the PRAM cell by applying the

Table 7. Parameters in the *pramSweep* module.

Parameter	Range	Description
riseTime	20ns to 10ms	Rise and fall time for the RESET pulse
resetV	–10V to +10V	Voltage for the RESET pulse
resetWidth	20ns to 1s	Pulse top width of the RESET pulse
measV	–10V to +10V	Voltage for the measure V pulse
measWidth	20ns to 1s	Pulse top width for the measure V pulse
Delay	20ns to 1s	Delay time between the pulses and rise/fall time for measure pulses
setWidth	20ns to 1s	Pulse top width for the SET pulse
setFallTime	20ns to 10ms	Fall time for the SET pulse
setStartV	–10V to +10V	Start voltage for the SET pulse amplitude sweep
setStopV	–10V to +10V	Stop voltage for the SET pulse amplitude sweep
Irange1	100 nA to 10 mA	Current measure range for RPM1 (RPM1 forces voltage)
Irange2	100 nA to 10 mA	Current measure range for RPM2 (RPM2 measures current)
iteration	1 to 10,000	Which waveform to capture from the SET sweep
setR_size, resetR_size, setV_size, setI_size	10 to 10,000	Number of steps in the SET sweep and the size of the measurement arrays. All sizes must be set to the same value.
pts	10 to 10,000	Number of waveform points returned

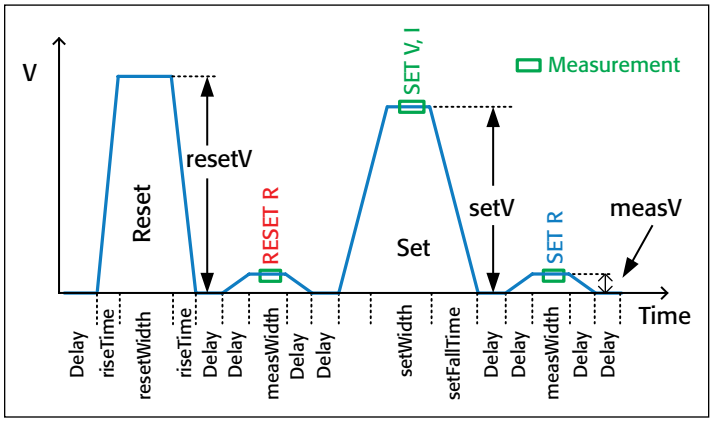

Figure 28. PRAM waveform definition.

Table 8. Parameters in the *pramEndurance* module.

Parameter	Range	Description
riseTime	20ns to 10ms	Rise and fall time for the RESET pulse
resetV	–10V to +10V	Voltage height of the RESET pulse
resetWidth	20ns to 1s	Pulse top width of the RESET pulse
measV	–10V to +10V	Voltage for the measure V pulse
measWidth	20ns to 1s	Pulse top width for the measure V pulse
delayT	20ns to 1s	Delay time between the pulses and rise/fall time for measure pulses
setWidth	20ns to 1s	Pulse top width for the SET pulse
setFallTime	20ns to 10ms	Fall time for the SET pulse
setV	–10V to +10V	Voltage height for the SET
Irange1	100nA to 10mA	Current measure range for RPM1 (RPM1 forces voltage)
Irange2	100nA to 10mA	Current measure range for RPM2 (RPM2 measures current)
max_loops	1 to 10^{12}	Maximum number of Reset+Set waveforms applied to the test device
setR_size, resetR_size, setI_size, iteration_size	2 to 10,000	Size of arrays for returned measurements. All sizes must be set to the same value.

RESET+SET waveform (**Figure *28***) *max_loops* times and measuring the RESET and SET resistances. The number of stress/measure cycles is determined by the value of *iteration_size*, which occurs in a log10 spacing within *max_loops*.

FeRAM Material Testing

The *NVM_Examples* project has three tests for two-terminal ferro-electric materials used in FeRAM (or FRAM) and stand-alone (1C) devices (***Figure 29***) in the *NVM_Examples* project (in the *C:\sModel 4200\kiuser\Projects_Memory* folder). The connection diagram is shown in ***Figure 30***. To obtain the best possible measurements, the connection uses the source high, measure low method described in the "Optimizing Measurements" section.

These tests require the following hardware:

- Model 4200-SCS with KTEI 8.2 or higher
- One Model 4225-PMU with two Model 4225-RPMs

FeRAM memory effect relies on charge storage in a capacitor but uses a ferro-electric layer instead of the dielectric layer of a typical capacitor. The memory mechanism for FeRAM is based on polarization shift in ferro-electric materials [9, 10, 11, 12]. Ferro-electric materials have strong non-linear dependency between applied electrical field (E) and polarization (P). When the electric field reaches a critical level, the ions inside the crystalline structure move from one stable location to another one. This shift is accompanied by a shift of the ferro-electric domain walls. Electrically, it is represented by the hysteresis chart (***Figure 32***), showing the dependency between electrical field and polarization. The switch between one state and another is characterized by the area of hysteresis, which represents the amount of charge moved during re-polarization.

The challenge of characterizing the ferro-electric capacitor is that the fundamental behavior is switching of the polarization

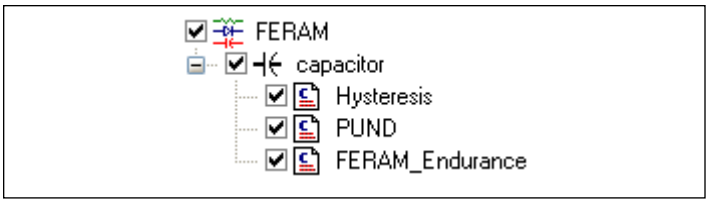

Figure 29. Tests for the FeRAM device in the *NVM_Examples* project.

state of the ferro-electric material, which requires measuring the polarization charge on the capacitor as it changes. Typically, a load capacitor, pulse generator, and oscilloscope are used, usually in a Sawyer-Tower circuit. In this approach, measuring the transient voltage, using an oscilloscope or sampler, across the load capacitor is a proxy for the charge flowing into the FE material. However, this method has several drawbacks.

The load capacitance must be relatively large compared to the FE capacitance to ensure that the voltage drop across the load capacitor is not significant; otherwise, some somewhat-unsatisfactory assumptions have to be applied to obtain the voltage across the FE element. However, this large load capacitance means that the sense voltage is fairly small. This small voltage is difficult to measure accurately with an oscilloscope or digitizer. The PMU+RPM solution does not require the load capacitor method because it measures the current and voltage directly and simultaneously so that the total charge can be accurately determined. The charge is calculated from the high speed current measurements, which are sampled consistently over time, resulting in high speed charge measurements. Note that the value reported is charge, not charge per unit area. However, it's easy to calculate the charge per unit area from the provided charge values by using the Formulator in the UTM definition tab.

Much like PCRAM and other NVM materials, FeRAM cells require a forming step or process before the cell exhibits reproducible switching behavior. The PUND or FERAM endurance tests can be used to apply the forming pulses. The PUND test is appropriate when a small number of pulses are required for forming, whereas the endurance test is better when a larger number of pulses are required. The hysteresis curve can indicate if the test device was sufficiently formed (see the gap at 0V in ***Figure 32***).

The hysteresis test applies positive and negative V-shaped pulses to measure the current. Because the current is sampled continuously, calculating the total charge is straightforward. ***Figure 31*** shows the test signal applied to the FE capacitor, as measured by the PMU+RPM. ***Figure 32*** shows the hysteresis curve, which was extracted from the data in ***Figure 31***. Proper test parameters on a good device should show a complete loop, with the beginning and end at 0V.

The characteristic shape of the hysteresis curve is not only a measure of the inherent ferro-electric material performance but may also show degradation due to the semiconductor processing that occurs after the FE capacitor fabrication.

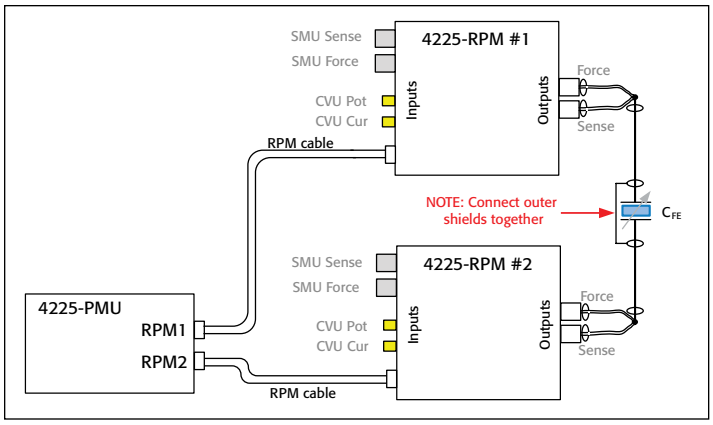

Figure 30. Connection for FeRAM tests. Note that the FeRAM tests included with *NVM_Examples* do not use the SMUs or CVU.

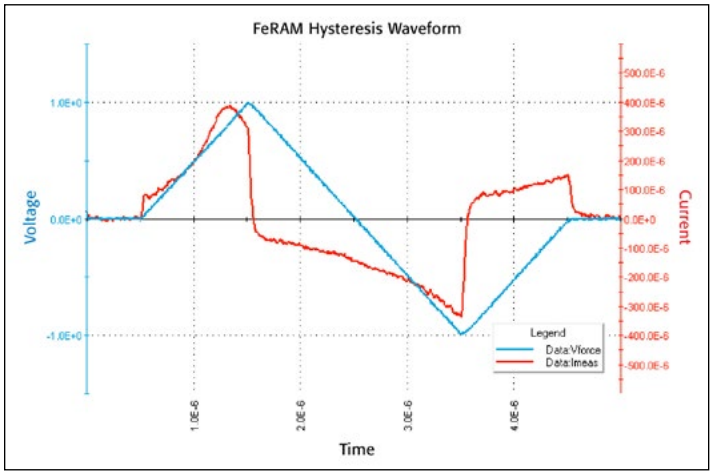

Figure 31. Hysteresis waveform generated and measured by the Model 4225-PMU with Model 4225-RPMs (user module *doubleSweepSeg*). This graph shows the voltage waveform (blue) applied to the FE capacitor. The red curve shows the current flow. *Figure 32* shows the typical hysteresis charge vs. voltage curve.

The PUND test characterizes the polarity change in the ferro-electric material. It is called PUND because four pulses are applied sequentially: Positive, Up, Negative, Down (***Figure 33***). Note the change in the shape of the current between the two up pulses (red P and red U) and similarly for the two down pulses (red N and red D). The first pulse requires additional charge/current to change the polarization (red P or red N), compared to the second pulse, which has the capacitive charging only (red U or red D). The difference between them (P-U or N-D) represents the polarization charge or memory effect. P_{SW} is the polarization change during the up pulses (P_{SW} = red P – red U). Q_{SW} is an average of the two charges from the two polarities (two up and two down pulses, Q_{SW} = ((red P – red U) + (red N – red D)) / 2). In addition to fundamental device and material characterization, the PUND test is used to determine the proper voltages and timing for the endurance test.

The endurance test shows the reduction in the polarization charge as the number of pulses applied increases. For some devices, the polarization charge may increase slightly during the initial pulse stress, before declining with an even larger number

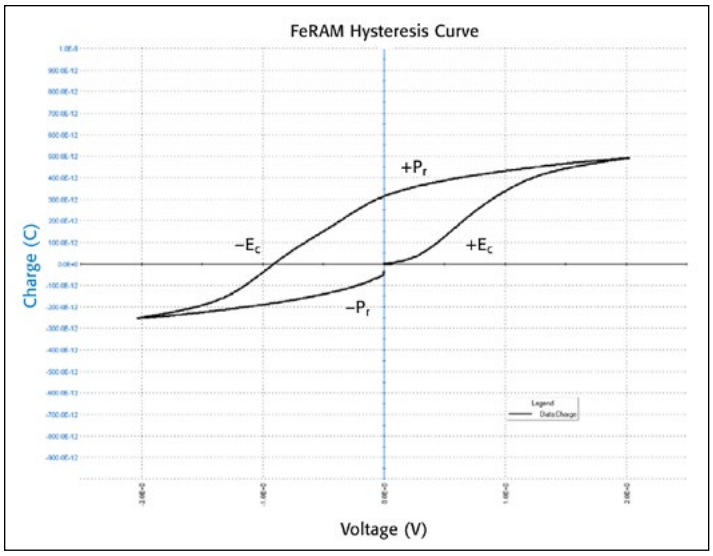

Figure 32. Hysteresis curve generated and measured by the Model 4225-PMU with Model 4225-RPMs (user module *doubleSweepSeg*). This graph shows the variation in the polarity charge as the voltage across the material varies. E_c is the coercive field and P_r is the remnant polarization, which are key parameters for FeRAM performance. Proper test parameters on a good, non-leaky device should show a complete loop, with the beginning and end at 0V.

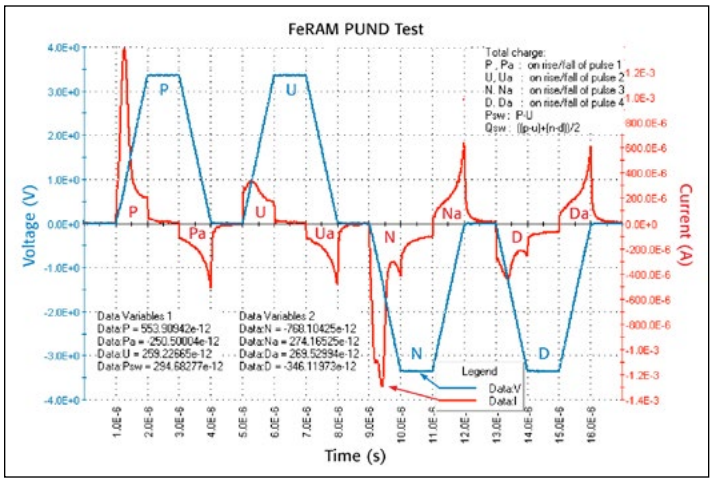

Figure 33. PUND waveforms generated and measured by the Model 4225-PMU with Model 4225-RPMs (user module *pundTest*). This graph shows the applied voltage pulses and the current response. The values for P, U, N, and D are extracted from the current waveform.

of stresses [13]. ***Figure 34*** shows example endurance results for Q_{SW} and P_{SW}. The degradation in Q_{SW} begins at 11 million cycles. The onset of degradation is a strong function of the pulse amplitude, so different materials and PUND voltages can provide significantly different degradation curves. ***Figure 35*** shows the change in the charges for P, U, N, and D, which determines the data shown in ***Figure 34***.

FeRAM Test Modules

There are three modules for testing ferro-electric materials or devices: ***doubleSweep***, ***pundTest***, and ***pundEndurance***.

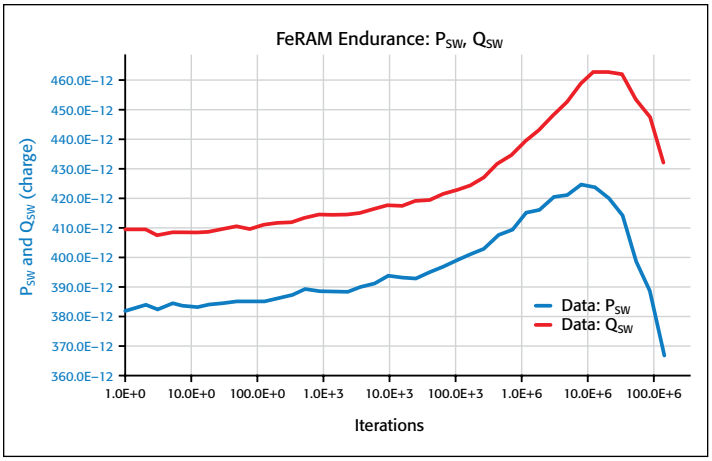

Figure 34. FeRAM endurance, showing the degradation in P_{SW} and Q_{SW} (user module *pundEndurance*). Some FeRAM endurance curves only show Q_{SW}. This data was taken by the Model 4225-PMU with Model 4225-RPMs.

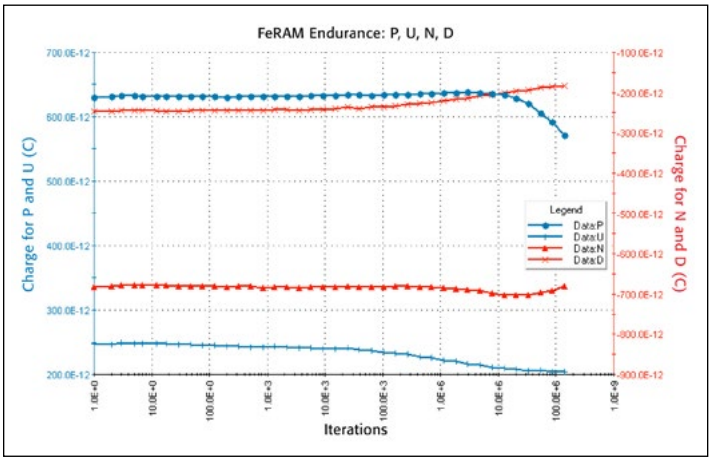

Figure 35. FeRAM endurance, showing the degradation in P, U, N, and D values (user module *pundEndurance*). This data is used to create the data in *Figure 34*. This data was taken by the Model 4225-PMU with Model 4225-RPMs.

Setting Up the Parameters in the *doubleSweep* Module

This module is the same module used in the PRAM test *IV_Curve*. However, the PRAM test used just one of the V-shaped pulses, while the FE capacitor hysteresis test uses two pulses (***Figure 27*** shows the definition, ***Figures 31*** and ***32*** show test results on FeRAM).

Table 6 lists the input parameters for the *doubleSweep* module.

Setting Up the Parameters in the *pundTest* Module

This module applies the four pulses that make up the PUND test, with the parameters briefly explained in ***Tables 9*** and ***10***. This test uses both Model 4225-RPMs connected to the first Model 4225-PMU in the Model 4200-SCS chassis (***Figure 30***). RPM1 outputs the voltage pulses and measures the applied voltage. RPM2 measures the current flowing through the test device. The returned values include the voltage (from RPM1), current (from RPM2), and time arrays. In addition, the charge for each pulse transition is returned. ***Figure 36*** shows the pulse parameter definitions.

Table 9. Input parameters in the *pundTest* module.

Parameter	Range	Description
V_p	–10V to +10V	Voltage level for the four PUND pulses. The first and second pulses are +Vp and the third and fourth pulses are at –Vp (***Figure 36***)
t_p	20ns to 1s	Width of each pulse top
t_d	20ns to 1s	Delay time between each pulse
trf	20ns to 10ms	Pulse transition time for all pulses
Irange1	100nA to 10mA	Current measure range for RPM1 (RPM1 forces voltage)
Irange2	100nA to 10mA	Current measure range for RPM2 (RPM2 measures current)

Table 10. Output parameters in the *pundTest* module.

Parameter	Type	Description
V	Double Array	Array of voltage measurements for the PUND waveform
I	Double Array	Array of current measurements for the PUND waveform
t	Double Array	Array of timestamps for the PUND waveform
P	Double	Total charge on rise of pulse 1
P_a	Double	Total charge on fall of pulse 1
U	Double	Total charge on rise of pulse 2
U_a	Double	Total charge on fall of pulse 2
N	Double	Total charge on rise of pulse 3
Na	Double	Total charge on fall of pulse 3
D	Double	Total charge on rise of pulse 4
D_a	Double	Total charge on fall of pulse 4
P_{sw}	Double	Polarization charge, defined as P – U
Q_{sw}	Double	Average polarization charge: ((p-u)+(n-d))/2
pts	Double	Total number of points recorded

Setting Up the Parameters in the *pundEndurance* Module

This module is a stress/measure test that applies the four pulses that make up the PUND test *max_loops* times to the test device, with the parameters briefly explained in ***Tables 11*** and ***12***. While applying the stress PUND waveform *max_loops* times, the number of measurement intervals is set by *fatigue_count*. The number of stress waveforms between each measurement is calculated on a log10 basis. The returned parameters are similar to *pundTest* and the pulse parameter definitions are shown in ***Figure 36***.

ReRAM and CBRAM Testing

As mentioned previously, ReRAM and CBRAM are types of Redox memory [14]. Both ReRAM and CBRAM are typically tested in the DC realm using SMU instruments, but SMU instruments may not be the best instrument for testing some memory types.

In traditional ReRAM test setups, to create, or form, the low resistance state initially, SMU instrument current compliance is used to limit the maximum current flowing through the test device during the forming or reset operation. The desire is to limit the amount of current to reduce the stress on the cell and

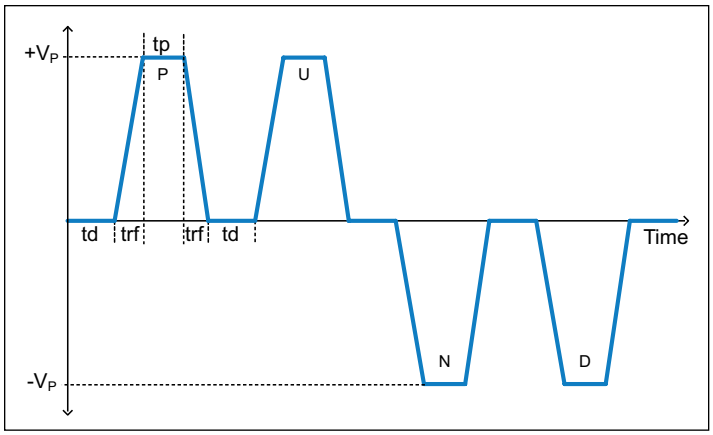

Figure 36. Pulse waveform parameters for *pundTest*.

Table 11. Input parameters in the *pundEndurance* module.

Parameter	Range	Description
V_p	–10V to +10V	Voltage level for the four PUND pulses. The first and second pulses are $+V_p$ and the third and fourth pulses are at $-V_p$
Vfat	–10V to +10V	Voltage pulse level for the two pulses of the fatigue waveform. First pulse is $+(V_p)$, last pulse is $-(V_p)$
T_p	20ns to 1s	Width of each pulse top
t_d	20ns to 1s	Delay time between each pulse.
Trf	20ns to 10ms	Pulse transition time for all pulses
Irange1	100nA to 10mA	Current measure range for RPM1 (RPM1 forces voltage)
Irange2	100nA to 10mA	Current measure range for RPM2 (RPM2 measures current)
pts_per_waveform	10 to 10,000	Number of measure points per PUND measure waveform
max_loops	1 to 10^{12}	Total number of stress waveforms applied to the test device
fatigue_count	2 to 100	Number of measurement intervals during *max_loops*.

Table 12. Output parameters in the *pundEndurance* module.

Parameter	Type	Description
Iteration	Integer: 1 to 100	Number of measurement intervals, must be same or greater than *fatigue_count*
P	Double	Total charge on rise of the P pulse
P_a	Double	Total charge on fall of the P pulse
U	Double	Total charge on rise of the U pulse
U_a	Double	Total charge on fall of the U pulse
N	Double	Total charge on rise of the N pulse
N_a	Double	Total charge on fall of the N pulse
D	Double	Total charge on rise of the D pulse
D_a	Double	Total charge on fall of the D pulse
P_{sw}	Double	Polarization charge, defined as P – U
Q_{sw}	Double	Average polarization charge: ((p-u)+(n-d))/2

also improve the quality of the switching process. However, the compliance circuit in an SMU instrument is not instantaneous, and takes microseconds to milliseconds to engage fully. Before the circuit is active, the amount of current flowing is not fully known or controlled. The actual transient response of the current compliance and the detailed interplay between the changing test device impedance and the reaction of the SMU instrument is complicated and not well understood.

Pulse I-V characterization improves the situation by providing strict timing control of the voltage signal applied to the test device. Tests in the ReRAM section of the *NVM_Examples* project can be used for characterization of ReRAM and CBRAM.

In the project, ReRAM device results are shown. ReRAM memory devices are two terminal devices, with a "low" and "high" side. A voltage pulse is applied across the oxide, and according to the mainstream literature, this creates conductive filaments. The process for creation of filaments is called "forming" and is considered the most important aspect that determines the ReRAM switching behavior. Forming is usually performed with DC voltage sweep with current limit enabled.

The following process takes place, as generally accepted. As voltage ramps up, the electrical field grows. When it becomes sufficient, a conductive filament begins to grow through the material from one electrode to the opposite electrode. As soon as it happens, the current limit engages and arrests the further growth of the conductive filament section. Resistance of the device drops from high resistance to low, for example, from several mega-ohms to the kilo-ohm range. This plausible explanation can bring into question that the speed of current-limit engagement may be important for ReRAM forming and therefore worthy of additional characterization. In the industry it still not common knowledge that the speed of a DC (SMU instrument) current limit is relatively slow, in the ~100μs range.

An ideal solution to this problem is to design structures with current-limiting control transistors directly on-wafer. This will ensure minimum parasitic capacitance and minimum response time. If, however, a current limit is not available on the wafer, it is suggested to use both SMU instrument current limiting and Model 4225-RPM current limiting to better understand forming mechanisms.

After forming, the applied RESET pulse changes resistance of the structure from low resistance to high. It is thought to be caused by the destruction of the conductive filament in the vicinity of the one of the electrodes. ReRAM structures can be symmetrical or polar. Polar devices require certain polarity of the forming pulse, and have non-symmetric material layouts. For polar devices, the Forming (and Set Pulse) have an opposite polarity from the Reset pulse.

Figure 37 shows the tests used for ReRAM testing. The first one is a standard characterization test, where a ReRAM device is tested and verified that it is valid and can be used.

The remaining tests include a Forming and a Set/Reset sequence, that is usually called the "Butterfly Curve." The last test is an Endurance test. ***Figure 38*** shows the connection diagram for a two terminal ReRAM device, showing both the pulse and SMU instrument connections. Note that if there is a chuck or backside connection, please connect RPM #1 to this terminal.

In ***Figure 39***, the blue curve, using the left y-axis, shows transient voltage applied to the ReRAM device. The red curve, using the right y-axis, is the current response. Note that the x-axis is time, in hundreds of microseconds. The voltage amplitude is ±2.3V. The same data is also plotted as I vs V as shown on the right. Exponential dependency of the current on the bias demonstrates that the device is not yet formed and can be used for characterization.

This data was collected with a PMU and two RPMs, using test routine, `reramSweep`; it can also be configured to use SMU instruments to collect similar data. There are several main differences between tests with PMU with RPMs and SMU instruments. First, the SMU instrument sweep takes significant time, up to several seconds, while the PMU+RPM sweep can be as fast as hundreds of nanoseconds. Second, the current limit capability for an RPM is much faster than an SMU instrument. An SMU instrument current compliance "engage time" is approximately 100–500μs, depending on the particular configuration and SMU instrument model, while an RPM limit can be as fast as several hundred nanoseconds, effectively ~3 orders of magnitude faster. While a control transistor, located on-wafer, would be faster and better in terms of energy control, the RPM current limit does provide research benefits

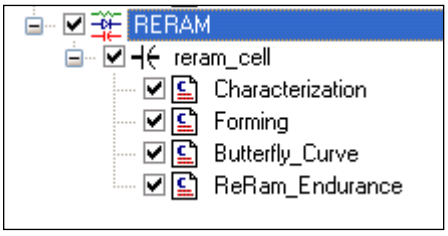

Figure 37: Screenshot of the tests for the ReRAM device in the NVM_ Examples project.

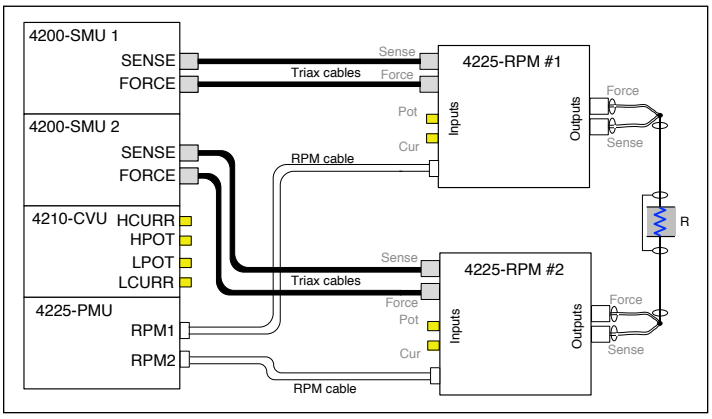

Figure 38. Connection to the 2 terminal ReRAM device.

compared to the SMU instrument testing. Using the PMU+RPM provides information that may help during the complicated and potentially costly transition to adding an on-wafer current limit capability. Another benefit to the pulse approach is using a second PMU+RPM channel to avoid capacitive charging effects by measuring the current through the test device on the low or side opposite the pulsing (***Figure 50***). The faster current limit is also useful during constant voltage stressing (CVS). Traditionally, CVS was performed using SMU instruments, but it can also be done using the PMU+RPM approach.

A detailed explanation of Capacitive Charging Effects during Pulse Transitions is given below.

ReRAM forming results are shown in the two graphs of ***Figure 40***. The graph to the left is voltage and current transients (V and I vs. time), and the graph to the right is the same data plotted as current vs voltage. Current exponentially grows as voltage reaches a certain value. When the filament is established, the device switches into low resistance state and the current limit prevents further growth of the filament. Forming was performed using a PMU+RPM with current limit enabled. A standard test configuration, used by most of the researchers in ReRAM field is to use DC instruments, SMU instruments, with current compliance. Forming performed with a PMU+RPM, unlike the the SMU instrument approach, is able to measure current and power transients during forming, while forming done with an SMU instrument completely hides details of the process. According to the literature, the forming process is controlled mostly by the value of the current limit and the speed of its activation. The right graphs shows the same data, but with the current plotted vs the voltage. The added arrows show the time progression of the curve, to allow for comparison to the time-based graph on the left.

The same test routine that was used for Characterization and Forming was applied to an already formed device to collect the "Butterfly" curve, as shown in ***Figure 41***. The chart to the left, as before, shows the current & voltage transient (I and V vs. time). The chart to the right is current vs. voltage in the shape of butterfly wings. The same routine, reramSweep [use fixed-width font], with different test conditions, can obtain both DC (SMU instrument) data and Pulse (PMU) data. This allows convenient switching between DC and PULSE modes of ReRAM characterization.

The left wing of the butterfly curve is a RESET transition, when resistance switches from low resistive state to high resistive state; note that the current limit is not enabled. Voltage polarity is opposite to the polarity used for forming and SET. During RESET process, it is commonly assumed, that conductive filament loses continuity from one electrode to another one, but this affects a small section of the filament. The SET process is very similar to the Forming process, in that it uses pulses of the same polarity to re-establish continuity of the conductive filament from one electrode to another one. Since the SET bias does not have to grow the whole filament, just reestablish the connection;

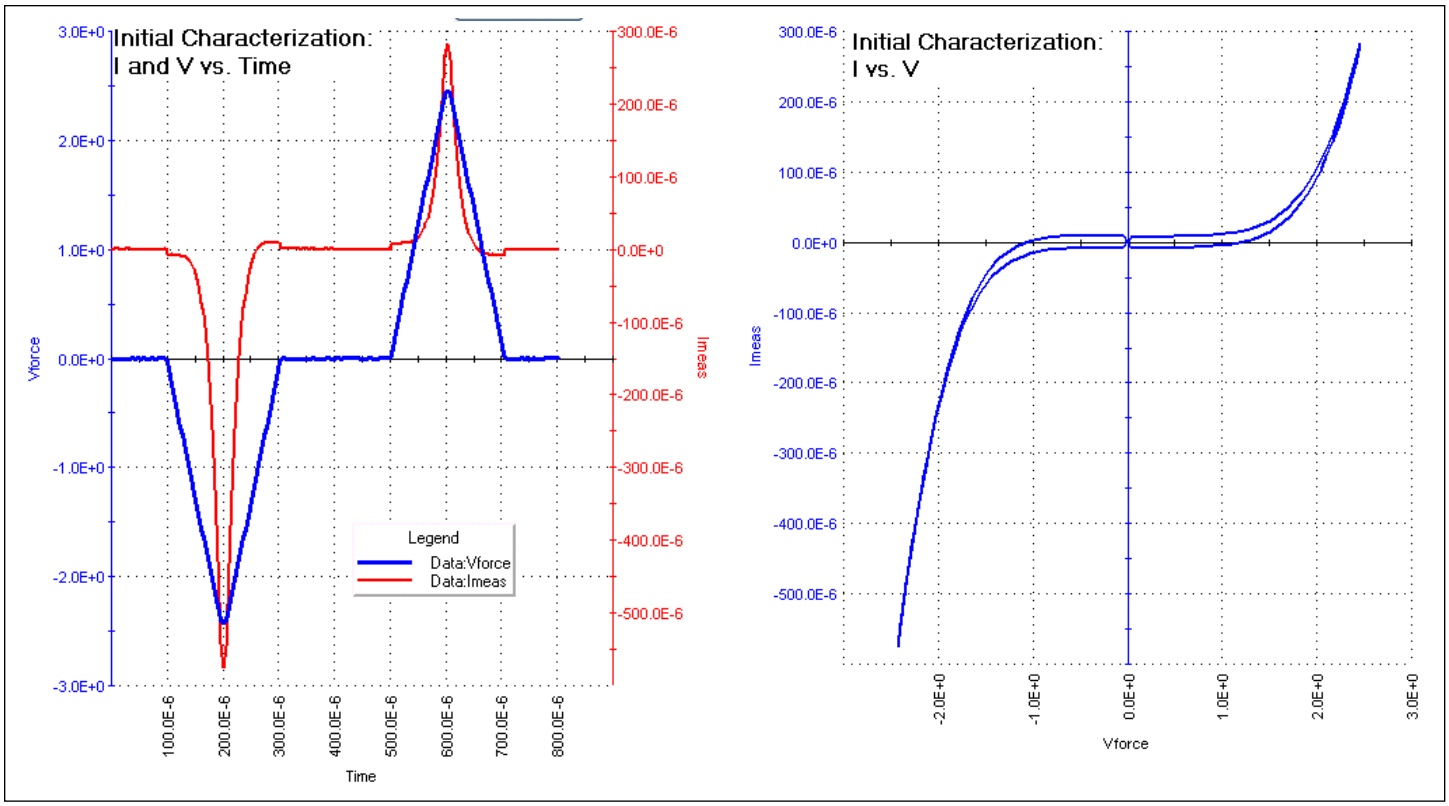

Figure 39. Characterization test of ReRAM structure.

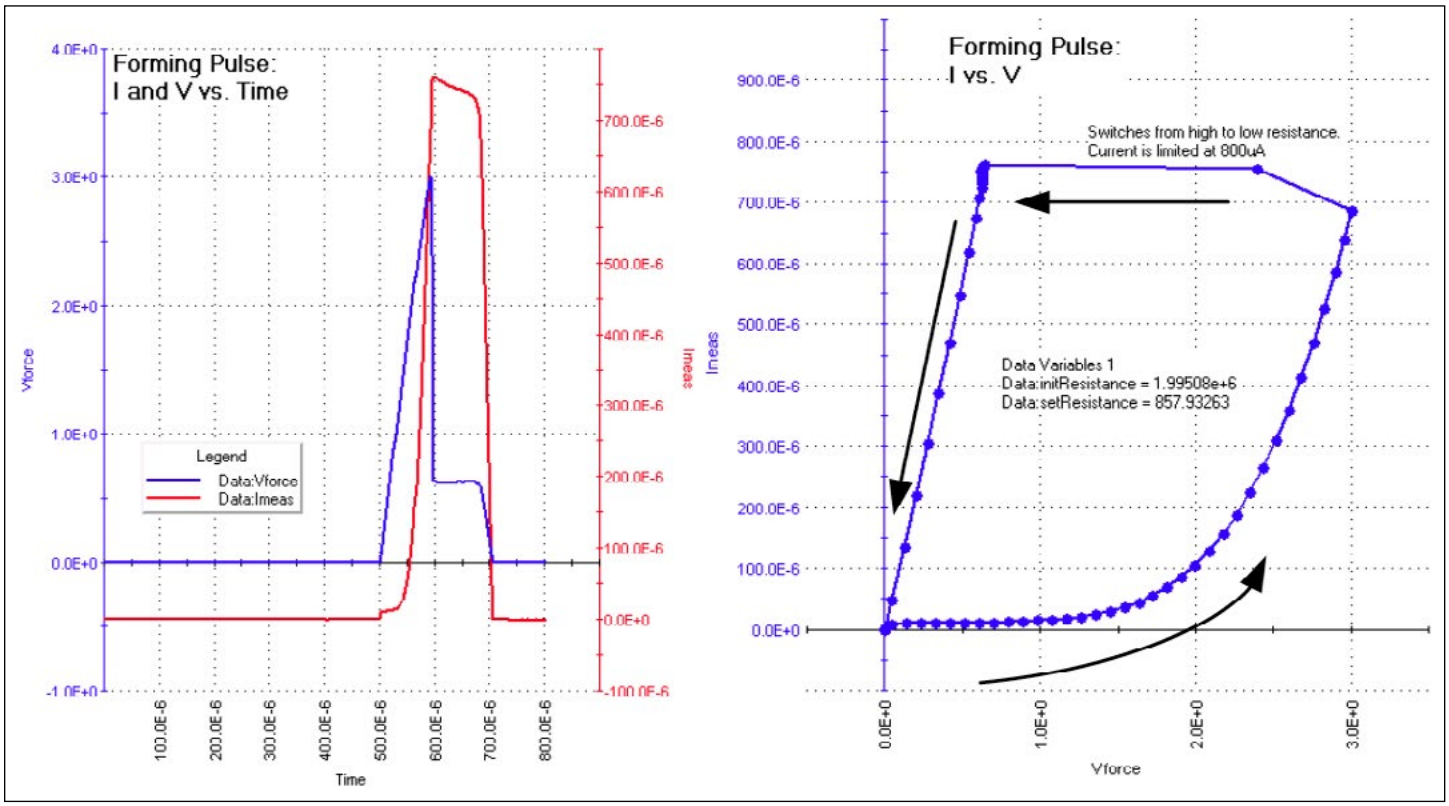

Figure 40. ReRAM forming.

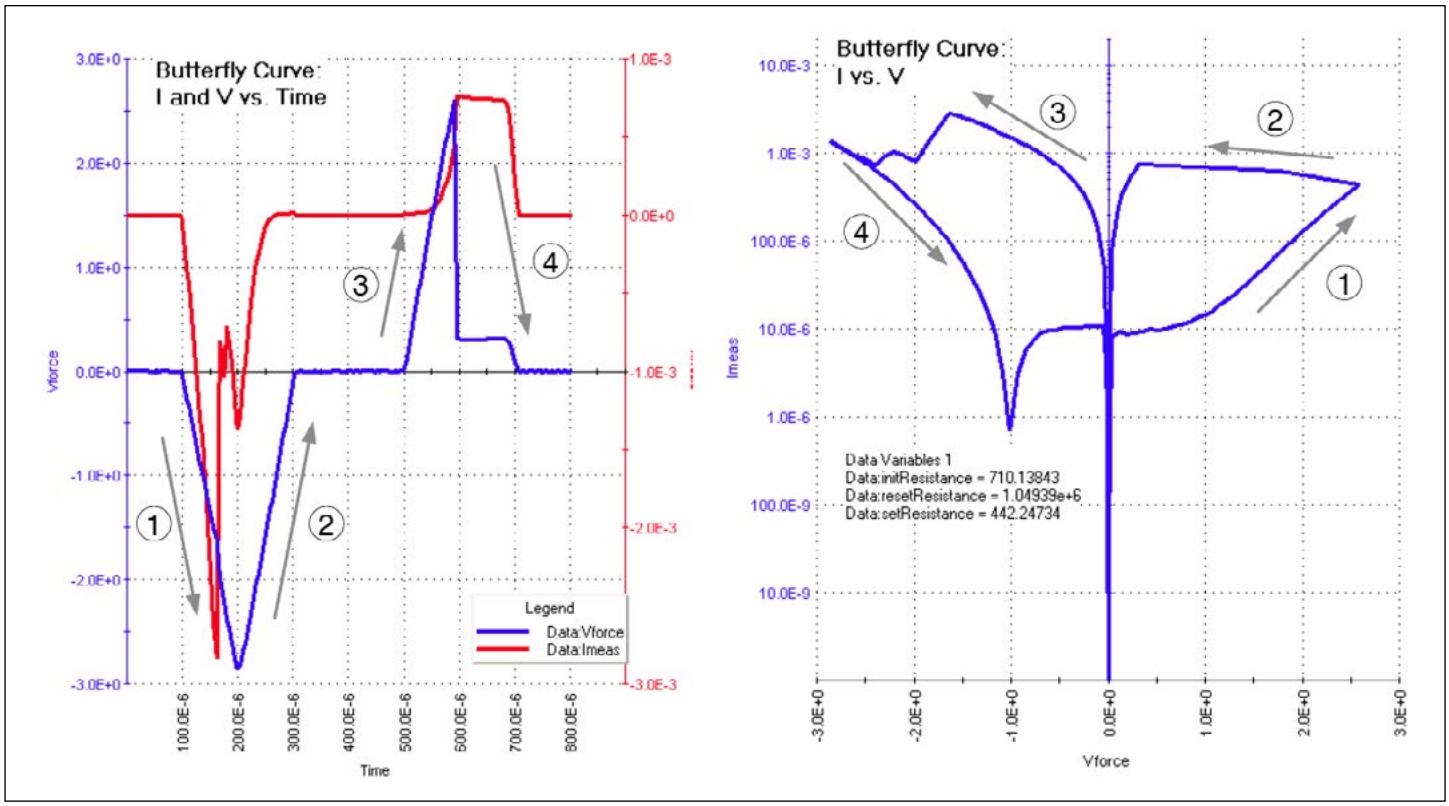

Figure 41. ReRAM "Butterfly" curve.

it requires less bias than the Forming process does. The SET procedure, similar to Forming, requires the use of the current limit capability but at a lower current level.

Selection of the test parameters for ReRAM testing, including Forming, SET, and RESET, follows a logical progression for initial forming and characterization.

1. First, prior to any forming, the test device is verified to be good and that it demonstrates a non-linear I-V dependency (***Figure 39***). During this initial pre-screening, care should be taken to use a voltage lower than the forming, SET, and RESET voltages.
2. Forming is a critical process (***Figure 40***). The value of the maximum bias should be selected to trigger filament growth. At the same time the current limit should be small enough, thereby preventing the filament from becoming too stable. If a conductive filament is too stable, than no amount of the Reset bias will disconnect the filament and no sufficient electrical field in the filament can be achieved. The value of the voltage bias for the RESET pulse should be just enough to break the filament.
3. Current limit for the SET bias, similar to Forming, should be just large enough to reconnect the filament, but not too large to prevent a "disconnect" in the next SET/RESET cycle. Selection of the Forming/SET and RESET parameters are somewhat tricky, require sufficient investigation, and in a critical way control the endurance of the ReRAM device. The endurance is defined as maximum number of SET/RESET cycles, where the LOW and HIGH resistance states are sufficiently different.

Figure 42 gives an example of the Endurance test of a ReRAM structure. The endurance test is similar to endurance tests for PRAM, Flash, and FeRAM. The control parameter, which in case of resistive memory, is resistance, and has two states, low and high. Low resistance corresponds to the state when conductive filament is formed and connected opposite electrodes across the oxide. High resistance is the state where a small section of the filament is converted back to high resistive material. Selection of the Forming, SET, and RESET processes defines how many cycles it will take for the low resistance state to become indistinguishable from the higher resistance state, which is one way to determine the maximum number of cycles for device endurance.

Setting up the Parameters in the reramSweep Module

The reramSweep module is used to perform a double sweep with a flat section at the peak of each sweep. To test a ReRAM device, the user chooses appropriate values for the two peaks, either positive or negative, and then sets the timing (***Figure 43***, ***Table 12***). Either SMU instruments or a PMU with 2 RPMs can be used, depending on the setting of useSmu parameter. The Low side (***Figure 38***)of the device needs to be connected to PMU channel 1 using a RPM. "Low" side is defined as the side connected to the bulk, substrate, or chuck if there is connection between DUT and the substrate. SMU1 is also connected to channel 1, RPM1. SMU2 is connected to the channel 2 RPM. The voltage bias is applied to channel 1, channel 2 is kept at virtual ground potential and current is measured on channel 2.

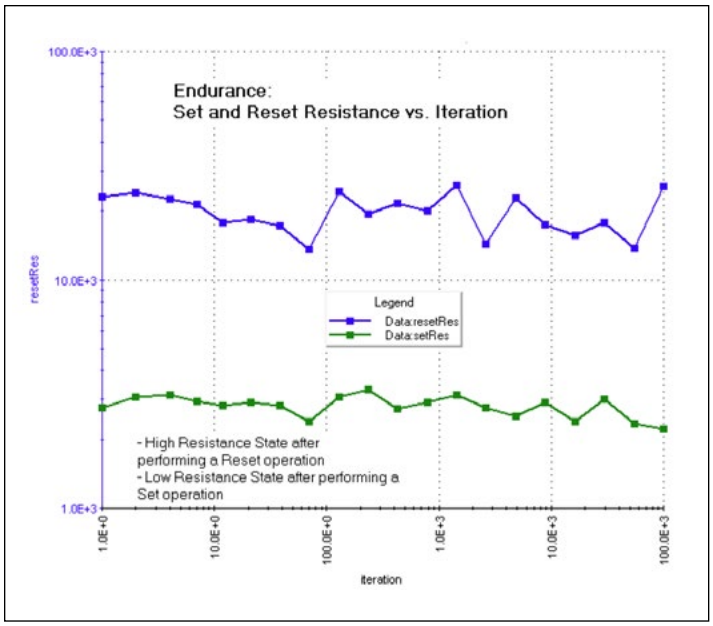

Figure 42: ReRAM endurance test.

Setting up the Parameters in the reramEndurance Module

The reramEndurance routine is used to perform a series of double sweeps (SET+RESET) using the same parameters used for the single sweeps as described in the `reramSweep` routine. To test a ReRAM device, choose appropriate values for the two peaks, either positive or negative, and then set the timing you would like to implement. Choose the number of times you would like to run the double sweep (`max _ loops`) and how often you want to take measurements (`fatigue _ count`). The routine will use a log10 approach to spacing the total number of measurements (`fatigue _ count`) across the total pulses (`max _ loops`). For example, if `max _ loops` = 10000 and `fatigue _ count` = 4, then there will be R_{SET} and R_{RESET} measurements after 10, 1000, 1000, and 10000 SET+RESET pulses applied to the test device.

RPM current limit calibration

The pulse current limiting capability is provided by the Model 4225-RPM. The short distance of the RPM to the DUT minimizes parasitic capacitance and time it takes for the current limit to activate and become effective. As mentioned above, this time is

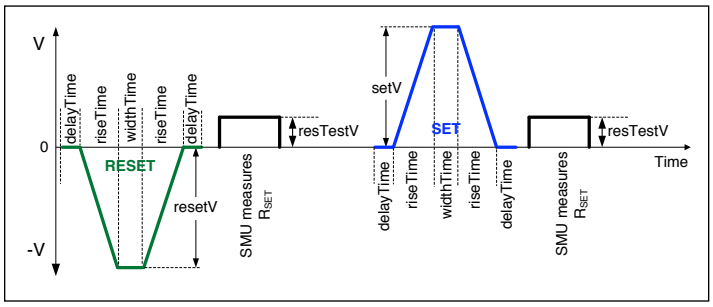

Figure 43. Pulse waveform with measure for reramSweep and reramEndurance.

Table 13. List of Input Parameters in the *reramSweep* module (see Figure 43)

Parameter	Range	Description
riseTime	2e-8s to 33 ms	The time it takes for voltage to ramp to the SET or RESET voltage. This value is slew rate-limited. To reach the slowest rise time, a higher voltage must be used.
widthTime	2e-8s to 1s	The time to wait at the top of the pulse at full voltage
delayTime	20 ns to 1 s	The time between the SET and RESET pulses
compliance	1 or 2	On which SMU instrument channel to enforce current compliance
resetV	–20V to 20V	The peak voltage of the reset pulse. For ReRAM devices, this value should be negative.
setV	–20V to 20V	The peak voltage of the set pulse. For ReRAM devices, this value should be positive.
Irange	100nA to 10mA for RPM 10 pA to 1A for SMU	The range at which to measure current. The SMU instrument has more ranges and also accept 0 for autorange.
resetIcomp	–100mA to +100mA	Please note that this variable is used both for PMU and SMU instrument control during RESET. If it is set to 0, then no current limit is applied. If useSmu = 1, and sweep is performed with the SMU instrument, and current limit is 0, autorange is used. With current limit not zero and useSmu = 1, the SMU instrument is set in the fixed current range.
setIcomp	–100mA to +100mA	Please note that this variable is used both for PMU and SMU instrument control during SET. If it is set to 0, then no current limit is applied. If useSmu = 1, and sweep is performed with the SMU instrument, and current limit is 0, autorange is used. With current limit not zero and useSmu = 1, the SMU instrument is set in the fixed current range.
resTestV	–10V to +10V	SMU instrument voltage used to measure device resistance.
takeRmeas	0 or 1	Whether or not to take resistance measurements. 1 means yes, take resistance measurements, while 0 means no, do not take resistance measurements.
useSmu	0 or 1	Whether or not to use an SMU instrument to take DC measurements instead of using the PMU+RPM for pulsing measurements. A 1 means yes, use the SMU instrument and a 0 means no, don't use the SMU instrument, use the PMU.
numIter	1 to 100	This parameter should be set to 1.
Vforce_size Imeas_size Time_size	10 to 10000	These three values should be the same and represent the number of items in the output arrays.

Table 14. List of Output Parameters in the *reramSweep* module.

Parameter	Range	Description
Vforce		Array of forced voltages
Imeas		Array of measured currents
Time		Array of measured times
resetResistance		Resistance of DUT after the reset pulse
setResistance		Resistance of DUT after the set pulse
initResistance		Resistance of DUT before any pulse

~3 orders of magnitude smaller than the current compliance activation time for a typical DC SMU instrument. The RPM current limit capability requires initial and periodic calibration. Before using the current limit feature of the Model 4225-RPM, calibration has to be performed manually by calling routine

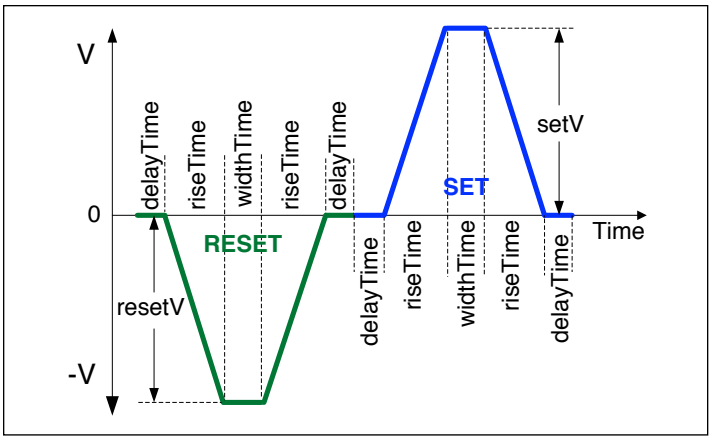

Figure 44. Pulse Waveform parameters for the stress reramEndurance.

Do_RPM_Ilimit_Cal (from user library RMP_ILimit_Control). This test is included in the NVM_Examples project in the Initialization Steps section at the top of the project tree.

Note that the Model 4225-RPM-LR does not have the current limit feature. Attempting to perform a current limit calibration on or set the current limit of a Model 4225-RPM-LR module will cause an error.

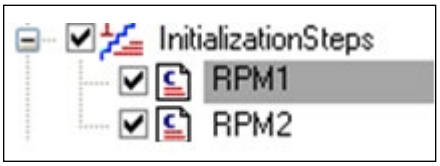

Figure 45. RPM Current limit UTMs in the NVM_Examples project tree.

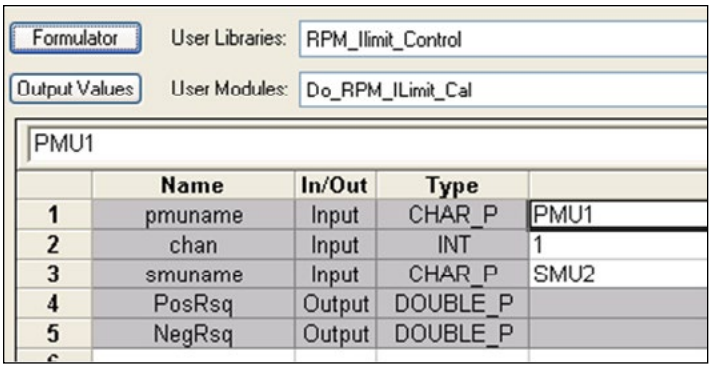

Figure 46. Settings for current limit calibration of the PMU channel 1 RPM.

Figure 47. Example good results for RPM Current limit calibration, as shown in the Sheet.

Here, two calls are shown to calibrate both RPMs (***Figure 45***). To execute a calibratation procedure for channel 1 of PMU1, set up input conditions to the routine as in ***Figure 46***, and connect SMU2 to the force output connector of the RPM1. To calibrate the channel 2 RPM, use the RPM2 test (***Figure 45***) and connect SMU1 to the force output connector RPM2 and use

Table 15. List of In put Parameters in the *reramEndurance* module (see Figure 43 and Figure 44).

Parameter	Range	Description
riseTime	4e-8 to 1e-2s	The time it takes for voltage to ramp to the final value
widthTime	4e-8 to 1e-2s	The time to wait at the top of the pulse at full voltage
delayTime	4e-8 to 1e-2s	The time between the two pulses and between the sweeps
useSmu	0 or 1	Should stay zero. Used for debugging purposes
compliance	CH 1 or 2	On which SMU instrument channel to enforce current compliance
resetV	–20 to 20V	The peak voltage of the reset pulse. For ReRAM devices, this value should be negative
setV	–20 to 20V	The peak voltage of the set pulse. For ReRAM devices, this value should be positive
Irange	0 to 0.2	The range at which to measure current
resetIcomp	–100mA to +100mA	Please note that this variable is used both for PMU and SMU instrument control during RESET. If it is set to 0, then no current limit is applied. If useSmu = 1, and sweep is performed with the SMU instrument, and current limit is 0, autorange is used. With current limit not zero and useSmu = 1, the SMU instrument is set in the fixed current range.
setIcomp	–100mA to +100mA	Please note that this variable is used both for PMU and SMU instrument control during SET. If it is set to 0, then no current limit is applied. If useSmu = 1, and sweep is performed with the SMU instrument, and current limit is 0, autorange is used. With current limit not zero and useSmu = 1, the SMU instrument is set in the fixed current range.
resTestV	0.1 to 2V	The voltage at which to measure the resistance of the DUT. This should be much less than the set and reset voltages as to not set or reset the DUT
max_loops	1 to 10^{12}	Number of pulses to output and stress the test device. Set the fatigue_count to determine the number of measure intervals within the max_loops number of pulse waveforms.
fatigue_count	2 to 100	Number of times to measure during the max_loops tests, using a log interval. For example, if max_loops = 1000 and fatigue_count = 4, there will be measurements of the SET and RESET resistance after 1, 10, 100, 1000 SET+RESET pulse waveforms are applied to the test device.

Table 16. List of Output Parameters in the *reramSweep* module.

Parameter	Range	Description
reset	Resistance	Resistance of DUT after the reset pulse
set	Resistance	Resistance of DUT after the set pulse
init	Resistance	Resistance of DUT before any pulse

SMU1 for parameter `smuname`. The quality of the calibration is determined by correlation factors called PosRsq and NegRsq. Calibration is considered successful if both these numbers are close to 1.000, with at least the first 4 or 5 digits = 9 (***Figure 47***, showing 999.995E-3 or 999.999E-3). The calibration will drift due to temperature, so for better performance, daily calibration is recommended. The current limit range is from ~10μA to 10mA.

Status and Error Codes for the *nvm* User Library

When debugging an error, start with the error code below (***Table 13***) and also look at the debug log file (*C:\nvmlog.txt*).

Optimizing Measurements

Because the Models 4225-PMU and 4225-RPM provide waveforms for each of the pulse waveform tests, determining the pulse fidelity is greatly simplified compared to source-only pulse systems. During initial setup, use the pulse waveforms to confirm proper voltage levels and timing response in addition to the extracted values (V_T, SET R, Hysteresis, PUND).

When measuring, there is always a tradeoff between the size of the measure window vs. the noise floor. A longer measure time will provide a less noisy result. The models 4225-PMU and 4225-RPM also follow this fundamental fact of measurement. However, because timing is a primary parameter, the tradeoff is more visible and therefore more controllable.

In addition to noise, note that lower current measure ranges have slower response than higher ranges. This is true for SMU current ranges, as well as Model 4225-PMU and Model 4225-RPM ranges. For example, the Model 4225-RPM current measurement settles much faster on the 10mA range (100ns best case) than the 100μA range (750ns best case). This means that sometimes using a higher current measure range will permit shorter pulse timing parameters because of the faster settling time but at the expense of a bit more noise.

Table 13. Error codes and descriptions for the *nvm* user library.

Code	Description
1	Test ran successfully
–10	Could not initialize NVM structure
–20	Return arrays are not the same size, or *iter_size* is smaller than *fatigue_count*
–40	Current range on one of the channels is too large, should be 10mA (10e-2) or less
–50	Error in *pg2_init*
–60	Error in *pulse_load*
–70	Error in *pulse_ranges*
–80	Error in *pulse_burst_count*
–90	Error in *pulse_output*
–100	Error in *pulse_standby*
–110	Error in *pulse_sample_rate*
–120	Error in *Set_RPM_ICompliance*
–130	Error in *seq_arb_sequence*
–140	Error in *pulse_exec*
–150	Error in *pulse_fetch*
–160	No points returned
–170	Error in *seg_arb_waveform*
–210	Error completing the test
–220	Error during measurement

Capacitive Charging Effects During Pulse Transitions

Figure 48 shows a simplified block diagram of a configuration used to create the waveforms shown in ***Figure 49***. During pulse transitions, current flows to charge and discharge capacitance in the test system. This current is not flowing through the DUT but does flow out from the instrument and into the cabling, as shown in ***Figure 48***. This charging current is measured by the PMU+RPM. ***Figure 49*** shows the capacitive charging effect using the pulse waveforms. The equation for this effect is:

$$I = C\ dV / dt$$

where:

I is the capacitive charging current.

C is the capacitance of the system (that is, the capacitance "seen" by the measurement circuit).

dV is the change in voltage.

dt is the change in time, in this case, the pulse transition or pulse rise and fall time.

This effect is fundamental and not implementation-specific, meaning that all instruments that measure high speed current will measure this effect. Note that measurements during the pulse top are not affected, which means that pulse I-V results are not affected by capacitive charging/discharging. This capacitive charging effect has not been previously seen because nearly all waveform measurements were voltage only.

Based on the equation, the effect is caused by the dV/dt and the C. Generally, the capacitance of the cable is larger than the DUT or instrument capacitance. The capacitance can be minimized by using shorter cable, but there will always be some capacitance in the instrument and in the interconnect. The dV/dt can be reduced by either reducing the voltage or increasing the rise and fall times. Reducing the voltage is usually not an option, as it is the desired signal level for characterization. Reducing the time may be possible in certain situations, but the time is a key test parameter for transient characterization.

The dV/dt provides the hint to a solution to the capacitive charging effect. Measuring the current on the other side of the DUT, away from the applied pulse, is the key to avoiding the effect. ***Figure 50*** shows the connection setup. Note that the side of the device connected to Channel 2 has a dV/dt that is essentially 0 for most cases. The results of the two-channel setup are shown in ***Figure 51***. Note that there is no charging or discharging effect seen during the pulse transitions. This approach is sometimes called pulsing on the high side (red curve in ***Figure 51***) and measuring the current on the low side. Note that high and low are referring to the relative voltages across the device.

Test Equipment

Minimum configuration:

- Model 4200-SCS with KTEI 9.0 or higher.

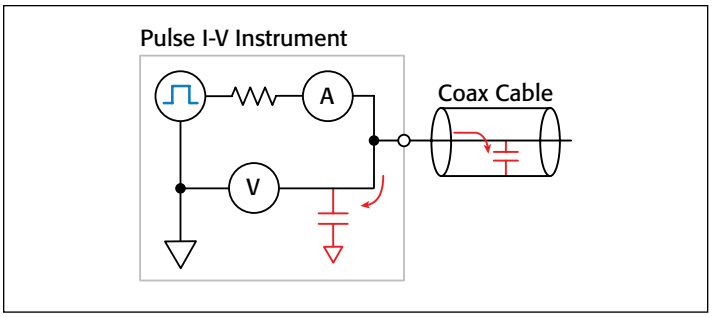

Figure 48. Block diagram of pulse I-V instrument showing the capacitive charging current during pulse transitions.

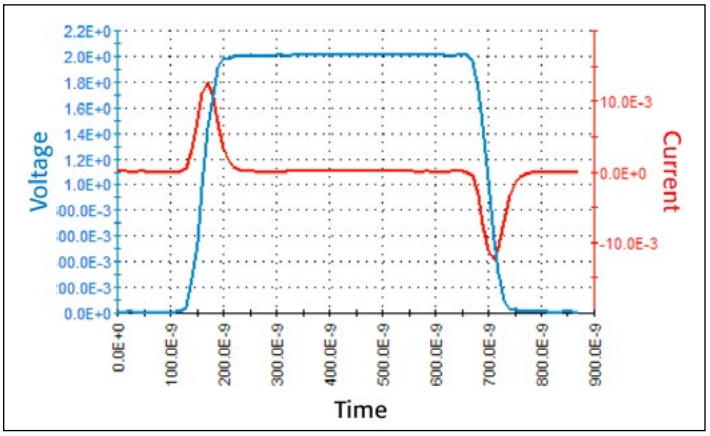

Figure 49. Capacitive charging effect. The blue curve is the voltage pulse applied to a short length of coax cable. The red curve is the resulting current flow, measured from the same side as the applied voltage pulse (*Figure 48*, or Channel 1 in *Figure 50*). The charging effects are the humps in the red curve during the voltge pulse transition.

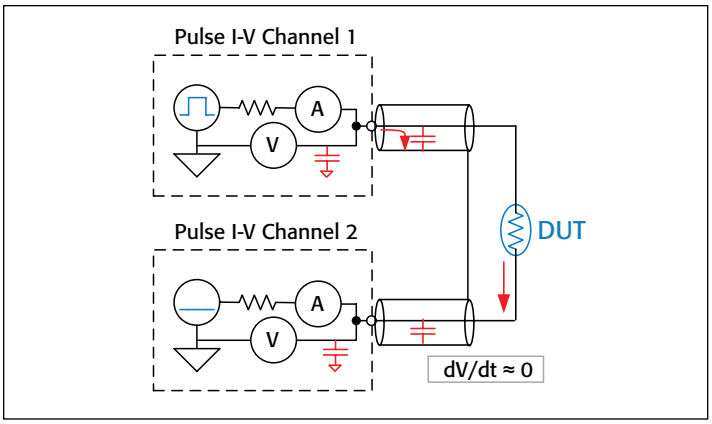

Figure 50. Block diagram of two pulse I-V channels connected to a two-terminal device.

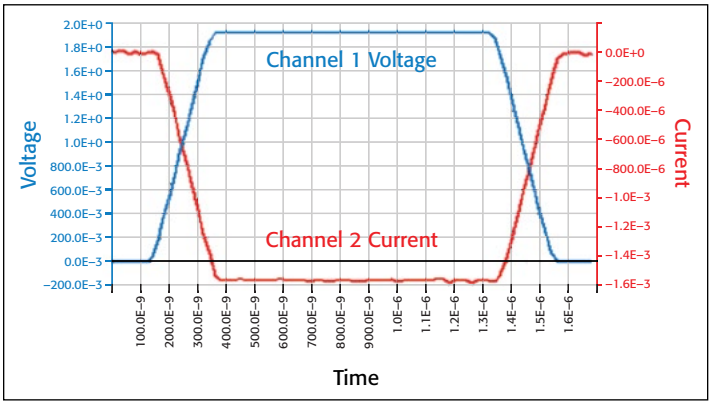

Figure 51. Pulse I-V waveforms for the configuration shown in *Figure 50*. No capacitive charging current is seen during the pulse transitions, only the current flowing through the resistor DUT.

- Two SMU instruments, either medium-power (Model 4200-SMU) or high-power (Model 4210-SMU). Note that the SMU instruments are used in the Flash and ReRAM tests only.
- One Model 4225-PMU with two Model 4225-RPMs
- Optional: Compiler to modify the *nvm* user modules (Order Number: 4200-Compiler)

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Electrical Characterization of Photovoltaic Materials and Solar Cells with the Model 4200-SCS Parameter Analyzer

I-V, C-V, C-f, DLCP, Pulsed I-V, Resistivity, and Hall Voltage Measurements

Introduction

The increasing demand for clean energy and the largely untapped potential of the sun as an energy source is making solar energy conversion technology increasingly important. As a result, the demand for solar cells, which convert sunlight directly into electricity, is growing. Solar or photovoltaic (PV) cells are made up of semiconductor materials that absorb photons from sunlight and then release electrons, causing an electric current to flow when the cell is connected to a load. A variety of measurements are used to characterize a solar cell's performance, including its output and its efficiency. This electrical characterization is performed as part of research and development of photovoltaic cells and materials, as well as during the manufacturing process.

Some of the electrical tests commonly performed on solar cells involve measuring current and capacitance as a function of an applied DC voltage. Capacitance measurements are sometimes made as a function of frequency or AC voltage. Some tests require pulsed current-voltage measurements. These measurements are usually performed at different light intensities and under different temperature conditions. A variety of important device parameters can be extracted from the DC and pulsed current-voltage (I-V) and capacitance-voltage (C-V) measurements, including output current, conversion efficiency, maximum power output, doping density, resistivity, etc. Electrical characterization is important in determining how to make the cells as efficient as possible with minimal losses.

Instrumentation such as the Model 4200-SCS Parameter Analyzer can simplify testing and analysis when making these critical electrical measurements. The Model 4200-SCS is an integrated system that includes instruments for making DC and ultra fast I-V and C-V measurements, as well as control software, graphics, and mathematical analysis capability. The Model 4200-SCS is well-suited for performing a wide range of measurements, including DC and pulsed current-voltage (I-V), capacitance-voltage (C-V), capacitance-frequency (C-f), drive level capacitance profiling (DLCP), four-probe resistivity (ρ, σ), and Hall voltage (V_H) measurements. This application note describes how to use the Model 4200-SCS to make these electrical measurements on PV cells.

Making Electrical Measurements with the Model 4200-SCS

To simplify testing photovoltaic materials and cells, the Model 4200-SCS is supported with a test project for making many of the mostly commonly used measurements easily. These tests, which include I-V, capacitance, and resistivity measurements, also include formulas for extracting common parameters such as the maximum power, short circuit current, defect density, etc. The *SolarCell* project (***Figure 1***) is included with all Model 4200-SCS systems running KTEI Version 8.0 or later. It provides thirteen tests (***Table 1***) in the form of ITMs (Interactive Test Modules) and UTMs (User Test Modules) for electrical characterization.

Table 1. Test modules in the SolarCell project

Subsite Level	Test Module	Description
IV_sweep	fwd-ivsweep	Performs I-V sweep and calculates I_{sc}, V_{oc}, P_{max}, I_{max}, V_{max}, FF
	rev-ivsweep	Performs reversed bias I-V sweep
CV_sweep	cvsweep	Generates C-V sweep
	C-2vsV	Generates C-V sweep and calculates $1/C^2$
	cfsweep	Sweeps the frequency and measures capacitance
	DLCP	Measures capacitance as AC voltage is swept. DC voltage is applied so as to keep the total applied voltage constant. The defect density is calculated.
Pulse-IV	pulse-iv-sweep	Performs pulse I-V sweep using one channel of PMU
4PtProbe_resistivity	HiR	Uses 3 or 4 SMUs to source current and measure voltage difference for high resistance semiconductor materials. Calculates sheet resistivity.
	LoR	Uses 1 or 2 SMUs to source current and measure voltage using remote sense. Calculates sheet resistivity. Uses current reversal method to compensate for thermoelectric voltage offsets.
vdp_resistivity	I1_V23	First of 4 ITMs that are used to measure the van der Pauw resistivity. This ITM sources current between terminals 1 and 4 and measures the voltage difference between terminals 2 and 3.
	I2_V34	Sources current between terminals 2 and 1 and measures the voltage difference between terminals 3 and 4.
	I3_V41	Sources current between terminals 3 and 2 and measures the voltage difference between terminals 4 and 1.
	I4_V12	Sources current between terminals 4 and 1 and measures the voltage difference between terminals 1 and 2.

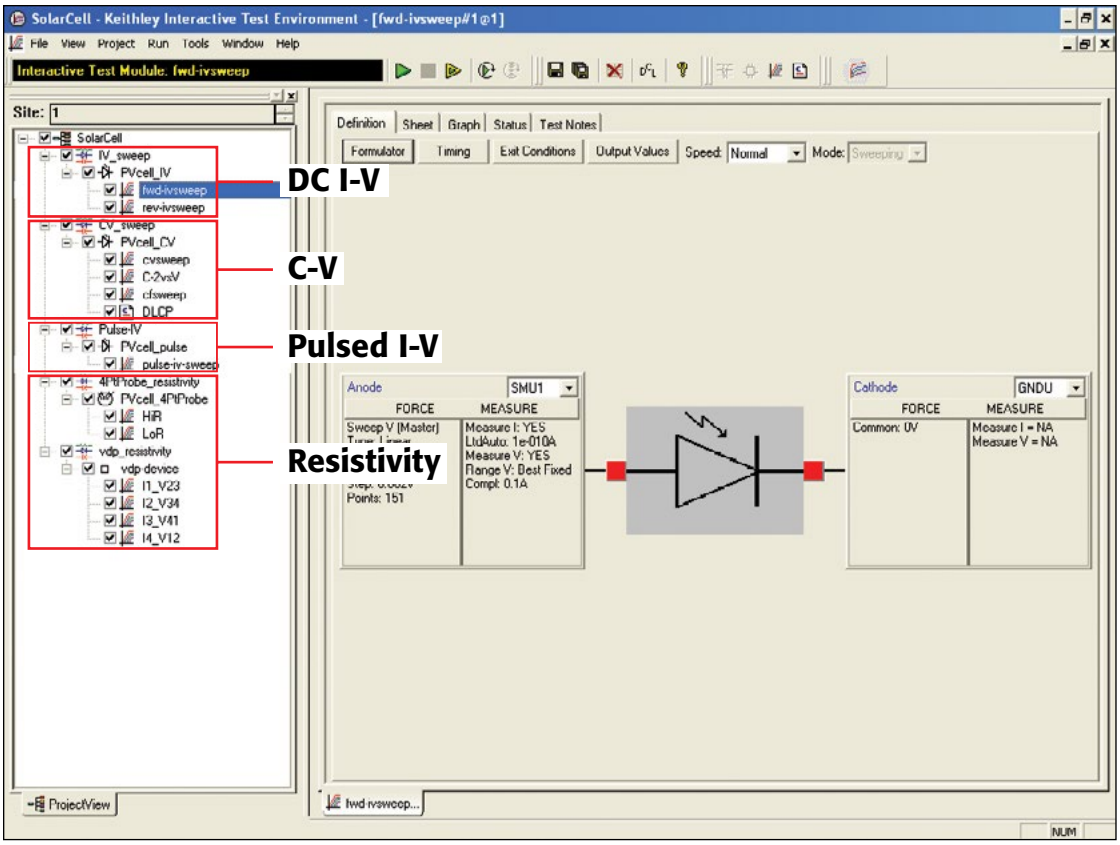

Figure 1. Screenshot of *SolarCell* project for the Model 4200-SCS

DC Current-Voltage (I-V) Measurements

As described previously, many solar cell parameters can be derived from current-voltage (I-V) measurements of the cell. These I-V characteristics can be measured using the Model 4200-SCS's source measure units (SMU) instruments, which can source and measure both current and voltage. Because these SMU instruments have four-quadrant source capability, they can sink the cell current as a function of the applied voltage. Two types of SMU instruments are available for the Model 4200-SCS: the Model 4200-SMU, which can source/sink up to 100mA, and the Model 4210-SMU, which can source/sink up to 1A. If the output current of the cell exceeds these current levels, it may be necessary to reduce it, possibly by reducing the area of the cell itself. However, if this is not possible, Keithley's Series 2400 or 2600B SourceMeter® SMU Instruments, which are capable of sourcing/sinking higher currents, offer possible alternative solutions.

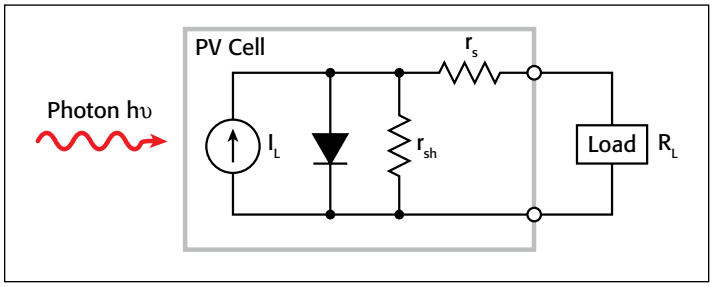

Figure 2. Idealized equivalent circuit of a photovoltaic cell

Parameters Derived from I-V Measurements

A solar cell may be represented by the equivalent circuit model shown in ***Figure 2***, which consists of a light-induced current source (I_L), a diode that generates a saturation current [$I_S(e^{qV/kT} - 1)$], series resistance (r_s), and shunt resistance (r_{sh}). The series resistance is due to the resistance of the metal contacts, ohmic losses in the front surface of the cell, impurity concentrations, and junction depth. The series resistance is an important parameter because it reduces both the cell's short-circuit current and its maximum power output. Ideally, the series resistance should be 0Ω ($r_s = 0$). The shunt resistance represents the loss due to surface leakage along the edge of the cell or to crystal defects. Ideally, the shunt resistance should be infinite ($r_{sh} = \infty$).

If a load resistor (R_L) is connected to an illuminated solar cell, then the total current becomes:

$$I = I_S(e^{qV/kT} - 1) - I_L$$

where:
I_S = current due to diode saturation
I_L = current due to optical generation

Several parameters are used to characterize the efficiency of the solar cell, including the maximum power point (P_{max}), the energy conversion efficiency (η), and the fill factor (FF). These points are illustrated in ***Figure 3***, which shows a typical forward bias I-V curve of an illuminated PV cell. The maximum power point (P_{max}) is the product of the maximum cell current (I_{max})

and the voltage (V_{max}) where the power output of the cell is greatest. This point is located at the "knee" of the curve.

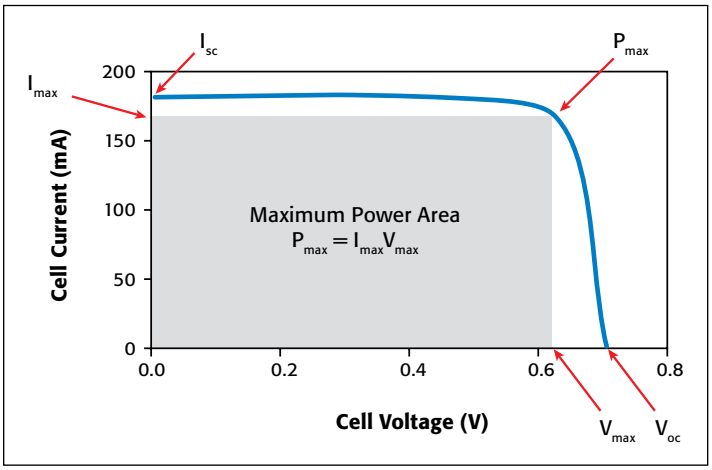

Figure 3. Typical forward bias I-V characteristics of a PV cell

The fill factor (FF) is a measure of how far the I-V characteristics of an actual PV cell differ from those of an ideal cell. The fill factor is defined as:

$$FF = \frac{I_{max}V_{max}}{I_{sc}V_{oc}}$$

where:

I_{max} = the current at the maximum power output (A)
V_{max} = the voltage at the maximum power output (V)
I_{sc} = the short-circuit current (A)
V_{oc} = the open-circuit voltage (V)

As defined, the fill factor is the ratio of the maximum power ($P_{max} = I_{max}V_{max}$) to the product of the short circuit current (I_{sc}) and the open circuit voltage (V_{oc}). The ideal solar cell has a fill factor equal to one (1) but losses from series and shunt resistance decrease the efficiency.

Another important parameter is the conversion efficiency (η), which is defined as the ratio of the maximum power output to the power input to the cell:

$$\eta = \frac{P_{max}}{P_{in}}$$

where:

P_{max} = the maximum power output (W)
P_{in} = the power input to the cell defined as the total radiant energy incident on the surface of the cell (W)

Making Connections to the Solar Cell for I-V Measurements

Figure 4 illustrates a solar cell connected to the Model 4200-SCS for I-V measurements. One side of the solar cell is connected to the Force and Sense terminals of SMU1; the other side is connected to the Force and Sense terminals of either SMU2 or the ground unit (GNDU) as shown.

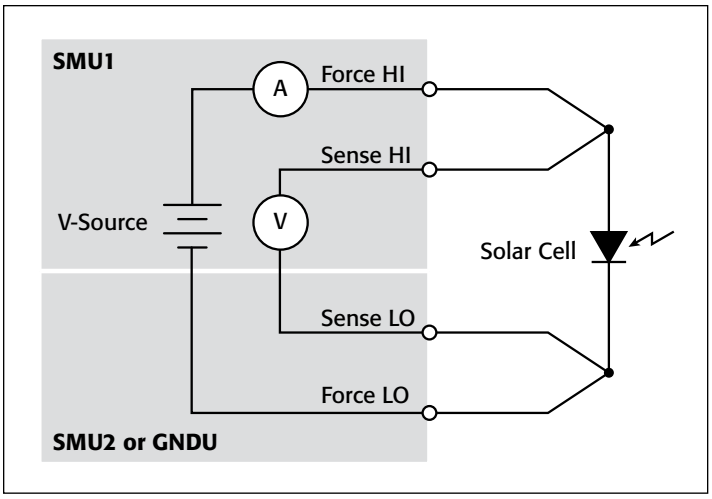

Figure 4. Connection of Model 4200-SCS to a solar cell for I-V measurements

Using a four-wire connection eliminates the lead resistance that would otherwise affect this measurement's accuracy. With the four-wire method, a voltage is sourced across the solar cell using one pair of test leads (between Force HI and Force LO), and the voltage drop across the cell is measured across a second set of leads (across Sense HI and Sense LO). The sense leads ensure that the voltage developed across the cell is the programmed output value and compensate for the lead resistance.

Forward-Biased I-V Measurements

Forward-biased I-V measurements of the solar cell are made under controlled illumination. The SMU instrument is set up to output a voltage sweep and measure the resulting current. This forward bias sweep can be performed using the "*fwd-ivsweep*" ITM, which allows adjusting the sweep voltage to the desired values. As previously illustrated in ***Figure 3***, the voltage source is swept from $V_1 = 0$ to $V_2 = VOC$. When the voltage source is 0 ($V_1 = 0$), the current is equal to the source-circuit current ($I_1 = I_{SC}$). When the voltage source is an open circuit ($V_2 = V_{OC}$), then the current is equal to zero ($I_2 = 0$). The parameters, V_{OC} and I_{SC}, can easily be derived from the sweep data using the Model 4200-SCS's built-in mathematical analysis tool, the Formulator. For convenience, the *SolarCell* project has the commonly derived parameters already calculated, so the values automatically appear in the Sheet tab every time the test is executed. ***Figure 5*** shows some of the derived parameters in the Sheet tab. These parameters include the short-circuit current (I_{SC}), the open circuit voltage (V_{OC}), the maximum power point (P_{max}), the maximum cell current (I_{max}), the maximum cell voltage (V_{max}), and the fill factor (FF).

Th user can easily add other formulas depending on the required parameters that need to be determined.

Using the Formulator, the conversion efficiency (η) can also be calculated if the user knows the power input to the cell and inputs the formula. The current density (J) can also be derived by using the Formulator and inputting the area of the cell.

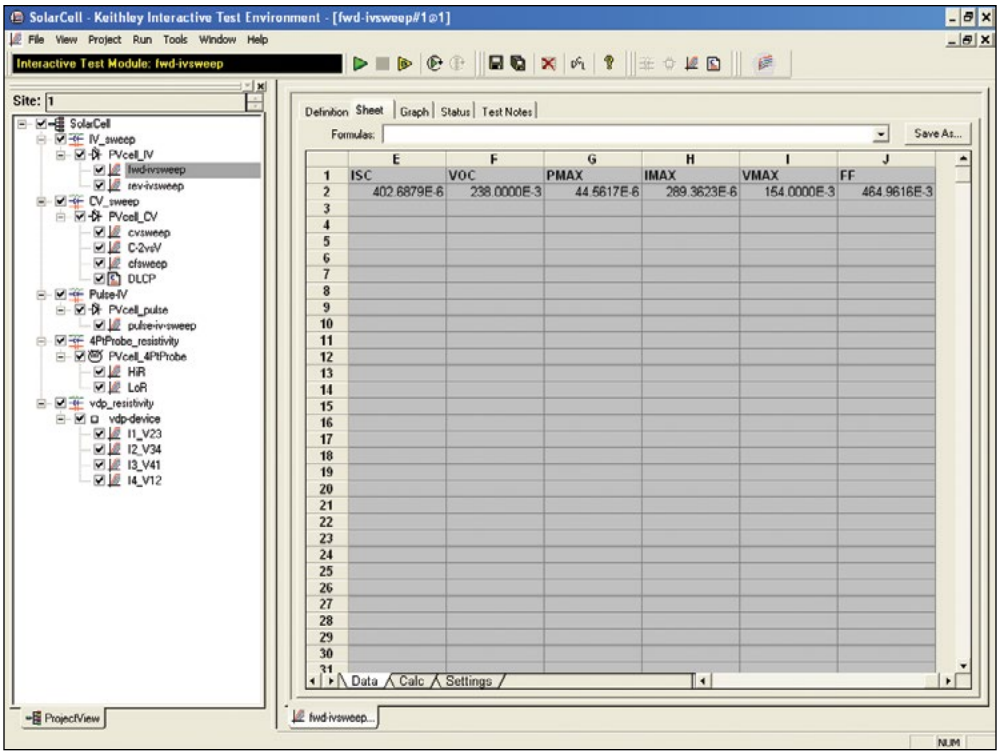

Figure 5. Results of calculated parameters shown in Sheet tab

Figure 6 shows an actual I-V sweep of an illuminated silicon PV cell generated with the Model 4200-SCS using the "*fwd-ivsweep*" ITM. Because the system's SMU instruments can sink current, the curve passes through the fourth quadrant and allows power to be extracted from the device (I–, V+). If the current output spans several decades as a function of the applied voltage, it may be desirable to generate a semilog plot of I vs. V. The Graph tab options support an easy transition between displaying data graphically on either a linear or a log scale.

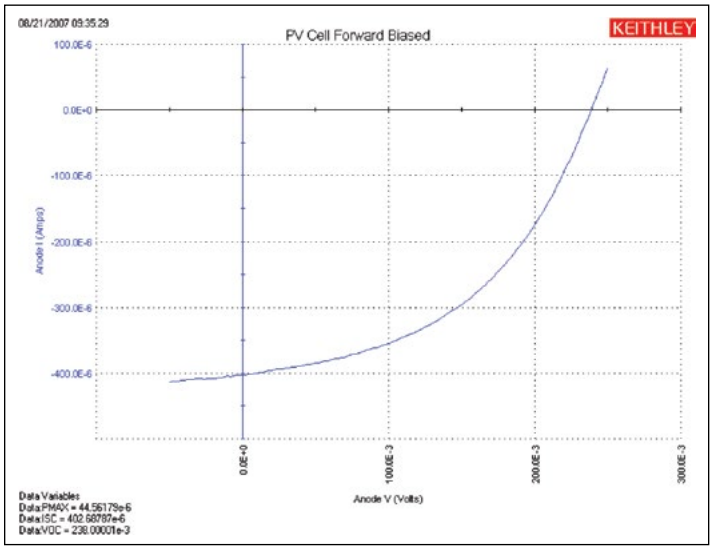

Figure 6. I-V sweep of silicon PV cell generated with the 4200-SMU

If desired, the graph settings functions make it easy to create an inverted version of the graph about the voltage axis. Simply go to the Graph Settings tab, select Axis Properties, select the Y1 Axis tab, and click on the Invert checkbox. The inverse of the graph will appear as shown in ***Figure 7***.

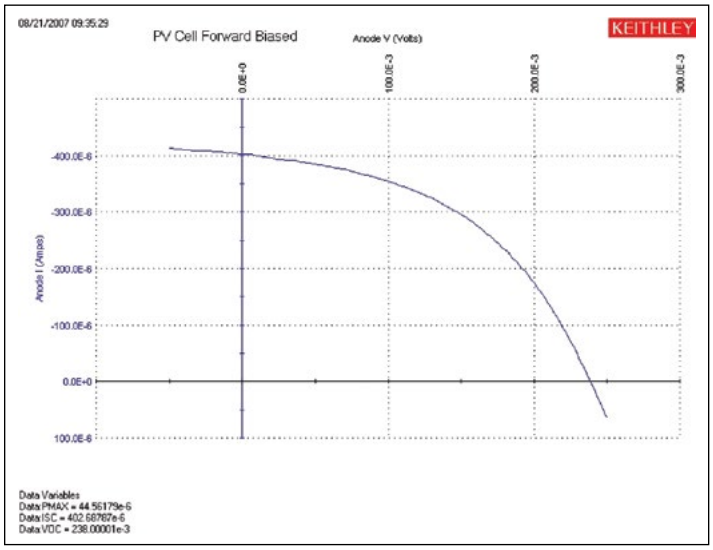

Figure 7. Inversion of the forward-biased I-V curve about the voltage axis

The series resistance (r_s) can be determined from the forward I-V sweep at two or more light intensities. First, make I-V curves at two different intensities (the magnitudes of the intensities are not important). Measure the slope of this curve from the far forward characteristics where the curve becomes linear. The inverse of this slope yields the series resistance:

$$r_s = \frac{\Delta V}{\Delta I}$$

By using additional light intensities, this technique can be extended using multiple points located near the knee of the curves. As illustrated in ***Figure 8***, a line is generated from which the series resistance can be calculated from the slope.

When considered as ammeters, one important feature of the Model 4200-SCS's SMU instruments is their very low voltage burden. The voltage burden is the voltage drop across the ammeter during the measurement. Most conventional digital multimeters (DMMs) will have a voltage burden of at least 200mV at full scale. Given that only millivolts may be sourced to the sample in solar cell testing, this can cause large errors. The Model 4200-SCS's SMU instruments don't produce more than a few hundred microvolts of voltage burden, or voltage drop, in the measurement circuit.

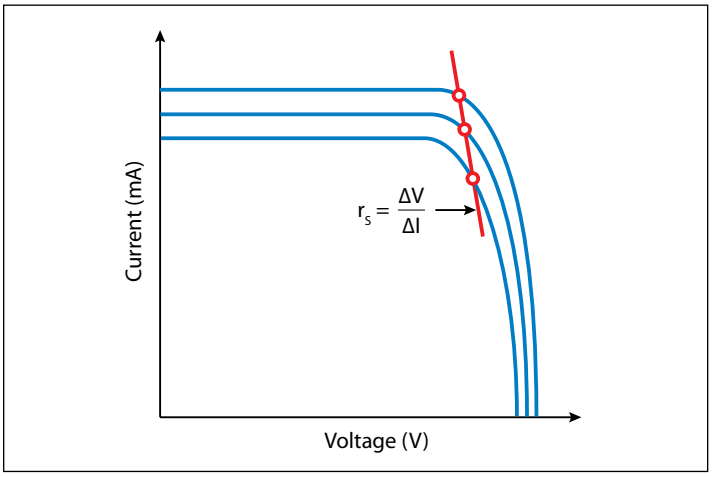

Figure 8. Slope method used to calculate the series resistance

Reverse-Biased I-V Measurements

The leakage current and shunt resistance (r_{sh}) can be derived from the reverse-biased I-V data. Typically, the test is performed in the dark. The voltage is sourced from 0V to a voltage level where the device begins to break down. The resulting current is measured and plotted as a function of the voltage. Depending on the size of the cell, the leakage current can be as small as picoamps. The Model 4200-SCS has a preamp option that allows making accurate measurements well below a picoamp. When making very sensitive low current measurements (nanoamps or less), use low noise cables and place the device in a shielded enclosure to shield it electrostatically. This conductive shield is connected to the Force LO terminal of the Model 4200-SCS. The Force LO terminal connection can be made from the outside shell of the triax connectors, the black binding post on the ground unit (GNDU), or from the Force LO triax connector on the GNDU.

One method for determining the shunt resistance of the PV cell is from the slope of the reverse-biased I-V curve, as shown in ***Figure 9***. From the linear region of this curve, the shunt resistance can be calculated as:

$$r_{sh} = \frac{\Delta V_{Reverse\ Bias}}{\Delta I_{Reverse\ Bias}}$$

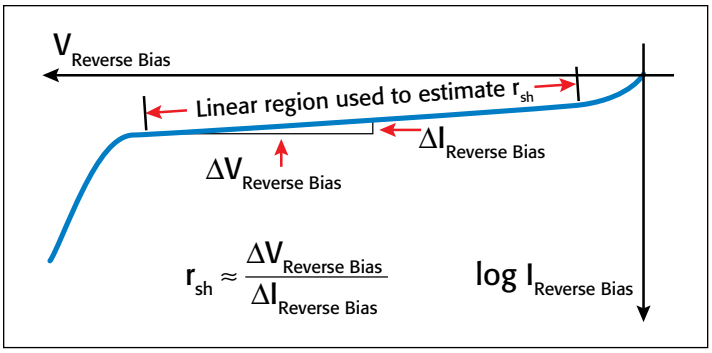

Figure 9. Typical reverse-biased characteristics of a PV cell

Figure 10 shows an actual curve of a reverse-biased solar cell, generated using the ITM "*rev-ivsweep*". In this semi-log graph, the absolute value of the current is plotted as a function of the reverse-biased voltage that is on an inverted x-axis.

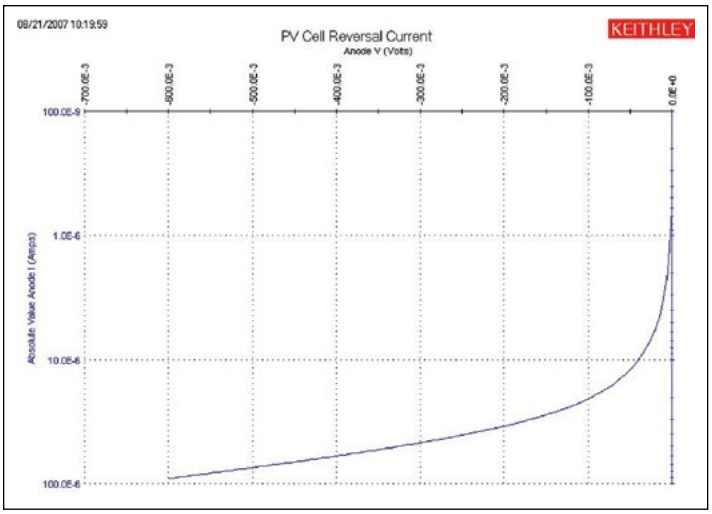

Figure 10. Reverse-biased I-V measurement of silicon solar cell using the Model 4200-SMU

Capacitance Measurements

Capacitance-voltage measurements are useful in deriving particular parameters about PV devices. Depending on the type of solar cell, capacitance-voltage (C-V) measurements can be used to derive parameters such as the doping concentration and the built-in voltage of the junction. A capacitance-frequency (C-f) sweep can be used to provide information on the existence of traps in the depletion region. The Model 4210-CVU, the Model 4200-SCS's optional capacitance meter, can measure the capacitance as a function of an applied DC voltage (C-V), a function of frequency (C-f), a function of time (C-t), or a function of the AC voltage. The Model 4210-CVU can also measure conductance and impedance.

To make capacitance measurements, a solar cell is connected to the Model 4210-CVU as shown in ***Figure 11***. Like I-V measurements made with the SMU instrument, the capacitance measurements also involve a four-wire connection to compensate for lead resistance. The HPOT/HCUR terminals are connected to

the anode and the LPOT/LCUR terminals are connected to the cathode. This connects the high DC voltage source terminal of the Model 4210-CVU to the anode.

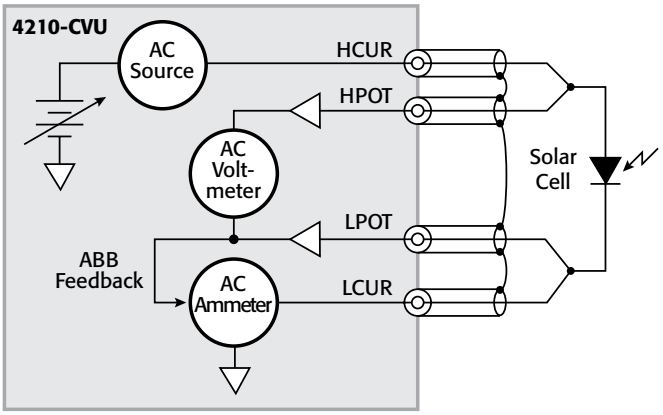

Figure 11. Connecting the solar cell to the Model 4210-CVU capacitance meter

Figure 11 shows the shields of the four coax cables coming from the four terminals of the capacitance meter. The shields from the coax cables must be connected together as close as possible to the solar cell to obtain the highest accuracy because this reduces the effects of the inductance in the measure circuit. This is especially important for capacitance measurements made at higher test frequencies.

Performing an Open and Short Connection Compensation will reduce the effects of cable capacitance on measurement accuracy. This simple procedure is described in Section 15 of the Model 4200-SCS Reference Manual.

Given that the capacitance of the cell is directly related to the area of the device, it may be necessary to reduce the area of the cell itself, if possible, to avoid capacitances that may be too high to measure. Also, setting the Model 4210-CVU to measure capacitance at a lower test frequency and/or lower AC drive voltage will allow measuring higher capacitances.

C-V Sweep

C-V measurements can be made either forward-biased or reverse-biased. However, when the cell is forward-biased, the applied DC voltage must be limited; otherwise, the conductance may get too high for the capacitance meter to measure. The maximum DC current cannot be greater than 10mA; otherwise, the instrument's DC voltage source will go into compliance and the DC voltage output will not be at the desired level.

Figure 12 illustrates a C-V curve of a silicon solar cell generated by the Model 4210-CVU using the "*cvsweep*" ITM. This test was performed in the dark while the cell was reversed-biased.

Rather than plotting dC/dV, it is sometimes desirable to view the data as $1/C^2$ vs. voltage because some parameters are related to the $1/C^2$ data. For example, the doping density (N) can be

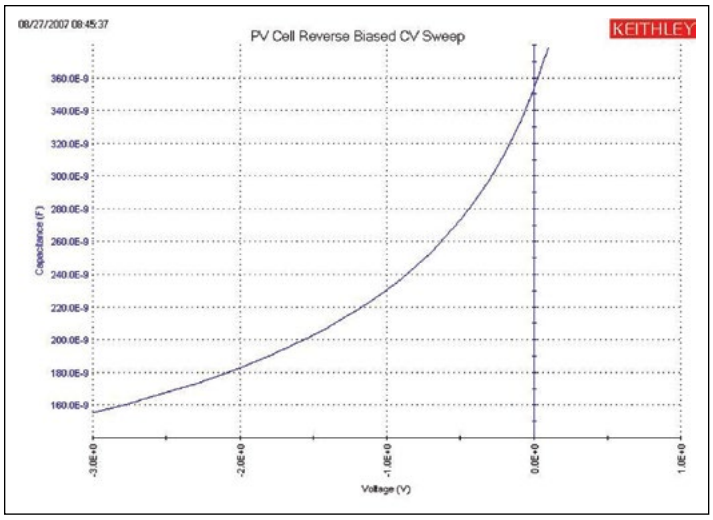

Figure 12. C-V sweep of a silicon solar cell

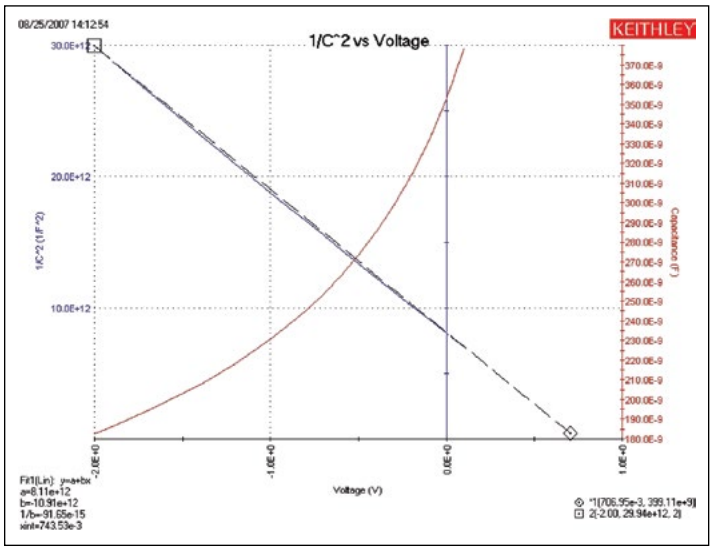

Figure 13. $1/C^2$ vs. voltage of a silicon solar cell

derived from the slope of this curve because N is related to the capacitance by:

$$N(a) = \frac{2}{qE_S A^2 [d(1/C^2)/dV]}$$

where:

N(a) = the doping density ($1/cm^3$)
q = the electron charge (1.60219×10^{-19}C)
E_s = semiconductor permittivity (1.034×10^{-12}F/cm for silicon)
A = area (cm^2)
C = measured capacitance (F)
V = applied DC voltage (V)

The built-in voltage of the cell junction can be derived from the intersection of the $1/C^2$ curve and the horizontal axis. This plot should be a fairly straight line. An actual curve taken with the Model 4210-CVU, generated using the "*C-2vsV*" ITM, is shown in ***Figure 13***. The Formulator function is used to derive both the doping density (N) and the built-in voltage on the x-axis (x-intercept). The doping density is calculated as a function of

voltage in the Formulator and appears in the Sheet tab in the ITM. The user must input the area of the cell in the Constants area of the Formulator. The built-in voltage source value is derived both in the Formulator and by using a Linear Line Fit option in the Graph settings. Notice the value of the x-intercept appears in the lower left corner of the graph.

C-f Sweep

The Model 4210-CVU option can also measure capacitance, conductance, or impedance as a function of the test frequency. The range of frequency is from 1kHz to 10MHz. The curve in ***Figure 14*** was generated by using the "*cfsweep*" ITM. Both the range of sweep frequency and the bias voltage can be adjusted. The desired parameters, such as the trap densities, can be extracted from the capacitance vs. frequency data. The measurements can be repeated at various temperatures.

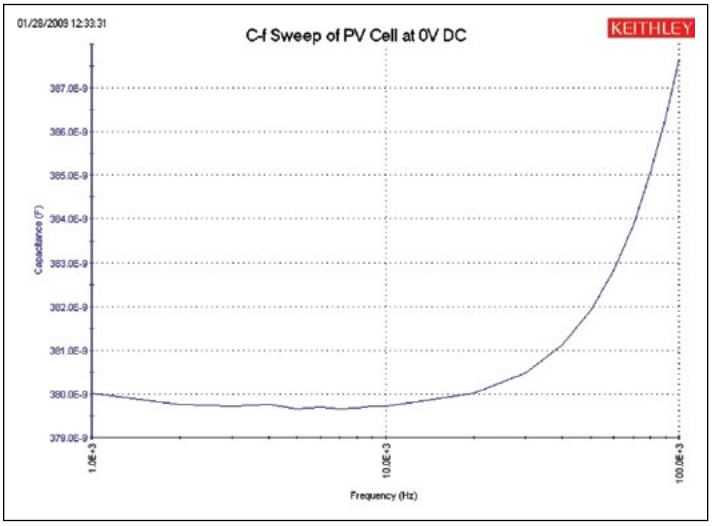

Figure 14. C-f Sweep of Solar Cell

Drive Level Capacitance Profiling (DLCP)

Drive Level Capacitance Profiling (DLCP) is a technique for determining the defect density (N_{DL}) as a function of depth of a photovoltaic cell[1]. During the DLCP measurement, the applied AC voltage (peak-to-peak) is swept and the DC voltage is varied while the capacitance is measured. This is in contrast to the conventional C-V profiling technique, in which the AC rms voltage is fixed and the DC voltage is swept.

In DLCP, the DC voltage is automatically adjusted to keep the total applied voltage (AC + DC) constant while the AC voltage is swept. By maintaining a constant total bias, the exposed charge density (ρ_e) inside the material stays constant up to a fixed location (x_e), which is defined as the distance from the interface where $E_F - E_v = E_e$. This is also in contrast to conventional C-V profiling, the analysis of which assumes that the only charge density changes occur at the end of the depletion region.[1]

Thus, in DLCP, the position (x_e) can be varied by adjusting the DC voltage bias to the sample. This also allows determining the defect density as a function of the distance, or special profiling. The test frequency and temperature of the measurement can also be varied to show a profile that is energy dependent.

Once the measurements are taken, a quadratic fit of the C-V data is related to the impurity density at a given depletion depth as follows for a p-type semiconductor:

$$N_{DL} \equiv \frac{C_0^3}{2q\varepsilon A^2 C_1} = \frac{|\rho_e|}{q} = p + \int_{E_F^0}^{E_V+E_e} g(E, x_e)dE$$

where:

N_{DL} = defect density (cm^{-3})
C1, C0 = coefficients of quadratic fit of C-V data
q = electron charge (1.60×10^{-19}C)
ε = permittivity (F/cm)
A = area of solar cell (cm^2)
ρ_e = charge density (C/cm^3)
p = hole density (cm^{-3})
x_e = distance from interface where $E_F - E_v = E_e$

The coefficients C_0 and C_1 are determined via a full least-squares best fit of the data to a quadratic equation:

$$dQ/dV = C_2 (dV)^2 + C_1*(dV) + C_0$$

However, only the C_0 and C_1 coefficients are used in the analysis.

The *"DLCP"* UTM allows making C-V measurements for drive level capacitance profiling. During these measurements, the total applied voltage remains constant as the DC voltage bias is automatically adjusted as the AC voltage drive level amplitude varies. The AC amplitude of the 4210-CVU can vary from $10mV_{rms}$ to $100mV_{rms}$ (14.14mV to $141.4mV_{p-p}$). The range of frequency can also be set from 1kHz to 10MHz. The capacitance is measured as the AC voltage is sweeping.

Table 2 lists the input parameters used in the UTM, the allowed range of input values, and descriptions. The user inputs the total applied voltage (VmaxTotal), the AC start, stop, and step voltages (VacppStart, VacppStop, and VacppStep), the time between voltage steps (SweepDelay), the test frequency (Frequency), the measurement speed (Speed), the measurement range (CVRange), and offset compensation (OpenComp, ShortComp, LoadComp, and LoadVal).

Table 2. Adjustable parameters for the *DLCP* UTM

Parameter	Range	Description
VmaxTotal	–10 to 10 volts	Applied DC Volts and ½ AC Volts p-p
VacppStart	.01414 to .1414	Start Vac p-p
VacppStop	.02828 to .1414	Stop Vac p-p
VacppStep	.0007070 to .1414	Step Vac p-p
SweepDelay	0 to 100	Sweep delay time in seconds
Frequency	1E+3 to 10E+6	Test Frequency in Hertz
Speed	0, 1, 2	0=Fast, 1=Normal, 2=Quiet
CVRange	0, 1E–6, 30E–6, 1E–3	0=autorange, 1μA, 30μA, 1mA
OpenComp	1, 0	Enables/disables open compensation for CVU

1 J. T. Heath, J. D. Cohen, W. N. Shafarman, "Bulk and metastable defects in $CuIn_{1-x}Ga_xSe_2$ thin films using drive-level capacitance profiling," *Journal of Applied Physics*, vol. 95, no. 3, p. 1000, 2004

ShortComp	1, 0	Enables/disables short compensation for CVU
LoadComp	1, 0	Enables/disables load compensation for CVU
LoadVal	1 to 1E+9	Load value

Once the test is executed, the capacitance, AC voltage, DC voltage, time stamp, frequency, and the defect density (N_{DL}) are determined and their values are listed in the Sheet tab. The defect density is calculated in the Formulator using a quadratic line fit of the C-V data. The coefficients (C_0 and C_1) of the quadratic equation are also listed in the Sheet tab. The user inputs the area and permittivity of the solar cell to be tested into the Constants/Values/Units area of the Formulator.

Figure 15 shows the measurement results in the graph of capacitance vs. AC voltage p-p. Notice the coefficients of the derived quadratic line fit and the defect density are displayed on the graph.

The capacitance measurements can be repeated at various applied total voltages in order to vary the position of x_e. The energy (E_e) can be varied by changing the test frequency (1kHz to 10MHz) or the temperature. To change the temperature of the measurement, the user can add a User Test Module (UTM) to control a temperature controller via the Model 4200-SCS's GPIB interface. The Model 4200-SCS is provided with user libraries for operating the Temptronics and Triotek temperature controllers.

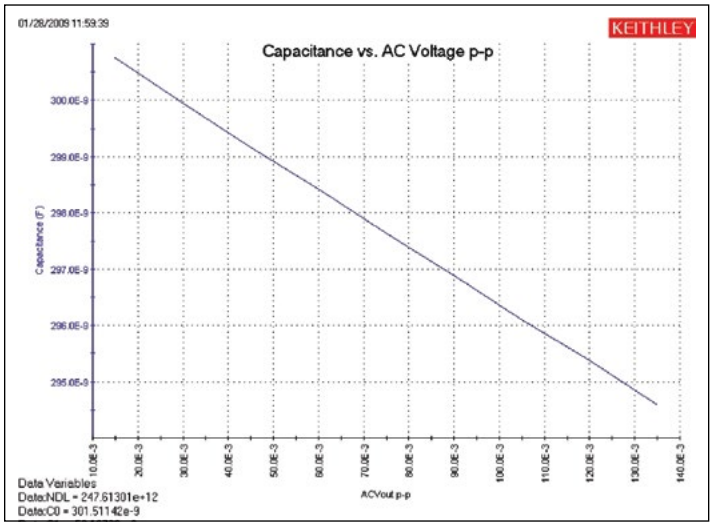

Figure 15. Capacitance vs. AC voltage p-p of a solar cell

Pulsed I-V Measurements

Pulsed I-V measurements can be useful for studying parameters of solar cells. In particular, pulsed I-V measurements have been used to determine the conversion efficiency, minimum carrier lifetime, and the effects of cell capacitance. The Model 4225-PMU, the Model 4200-SCS's optional Ultra-Fast I-V Module, can output pulsed voltage and measure current, and can capture ultra-high-speed current or voltage waveforms in the time domain. In addition to sourcing a pulsed voltage, the PMU can sink current so it can measure a solar cell's current output.

To make pulsed I-V measurements on a solar cell, the Model 4225-PMU is connected to the cell as shown in ***Figure 16***. Each PMU has two channels so the solar cell can be connected using either one or two channels. In the one-channel case shown, one end of the cell is connected to the HI terminal of PMU CH1 and the other side of the cell is connected to the shield of the coax cable, which is the LO terminal of the PMU.

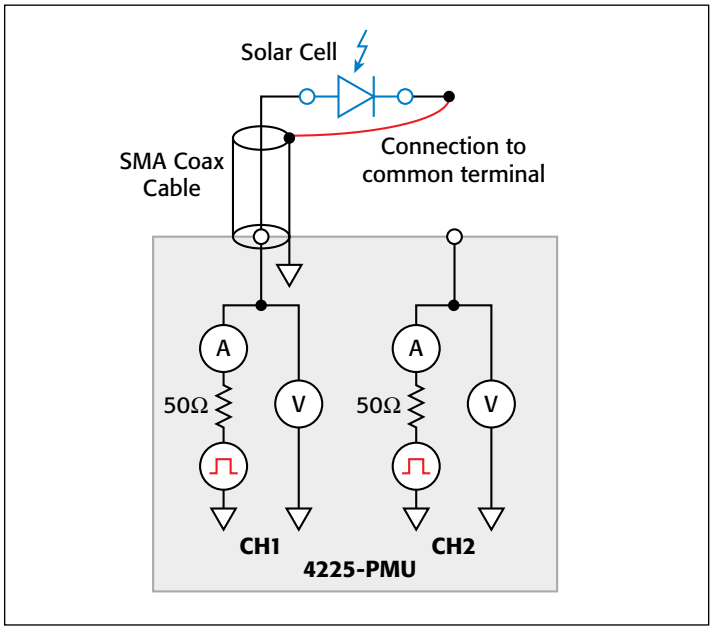

Figure 16. Connecting the solar cell to the Model 4225-PMU Ultra-Fast I-V Module

Unlike the DC I-V and C-V measurements, the 4225-PMU uses a two-wire technique. The Short Compensation feature can be used to "zero out" the voltage drops due to the cables so that a 4-wire measurement technique isn't necessary.

Because solar cells are fairly capacitive, it is important to ensure the pulse width is long enough for the pulsed I-V sweep. The waveform capture mode should be used to verify the pulse

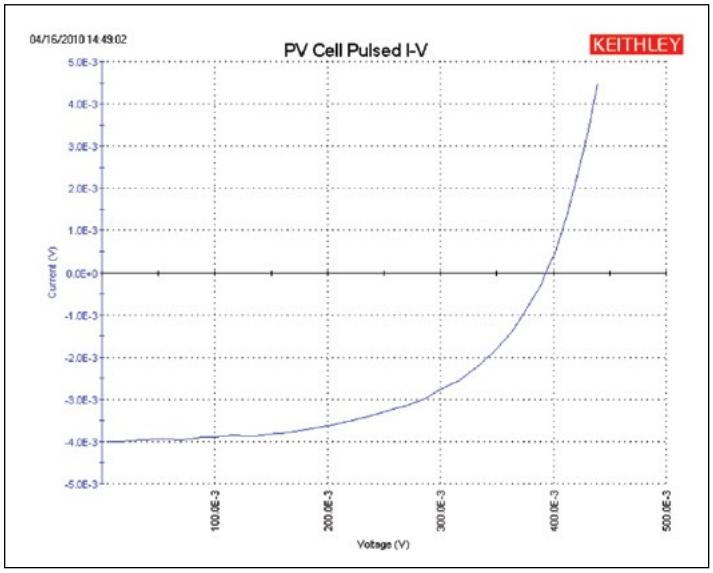

Figure 17. Pulsed I-V measurement on solar cell using Model 4225-PMU

width prior to generating the pulsed I-V sweep. The waveform capture mode enables a time-based current and/or voltage measurement that is typically the capture of a pulsed waveform. This can be used to perform a dynamic test on the cell or used as a diagnostic tool for choosing the appropriate pulse settings in the pulsed I-V mode. Given that larger solar cells have larger capacitances, it may be necessary to reduce the area of the cell itself to avoid a long settling time in the measurement.

The results of generating a pulsed I-V measurement sweep on a silicon solar cell are shown in ***Figure 17***. Note that the current is in the fourth quadrant of the curve. This indicates that the PMU is sinking current; in other words, the current is flowing out of the solar cell and into the PMU.

Resistivity and Hall Voltage Measurements

Determining the resistivity of a solar cell material is a common electrical measurement given that the magnitude of the resistivity directly affects the cell's performance. Resistivity measurements of semiconductor materials are usually performed using a four-terminal technique. Using four probes eliminates errors due to the probe resistance, spreading resistance under each probe, and the contact resistance between each metal contact and the semiconductor material. Two common techniques for determining the resistivity of a solar cell material are the four-point collinear probe method and the van der Pauw method. The *SolarCell* project contains several ITMs for making both types of measurements. More detailed information about making resistivity measurements on semiconductor materials using the Model 4200-SCS can be found in Keithley Application Note #2475, "Four-Probe Resistivity and Hall Voltage Measurements with the Model 4200-SCS."

Four-Point Collinear Probe Measurement Method

The four-point collinear probe technique involves bringing four equally spaced probes in contact with a material of unknown resistance. The probe array is placed in the center of the material as shown in ***Figure 18***. The two outer probes are used to source current and the two inner probes are used to measure the resulting voltage difference across the surface of the material.

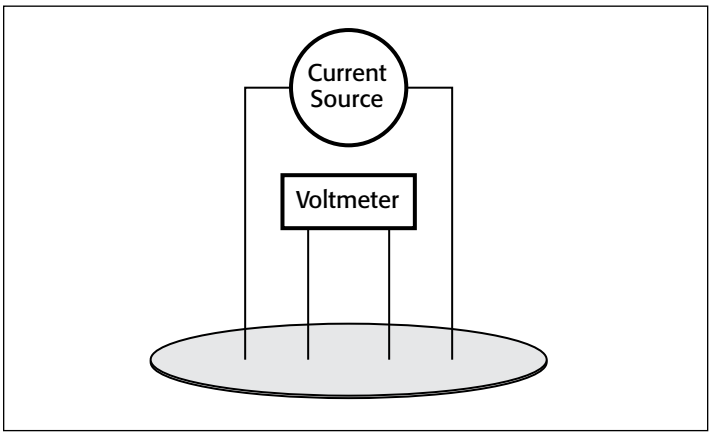

Figure 18. Four-point collinear probe resistivity configuration

From the sourced current and the measured voltage, the surface or sheet resistivity is calculated by:

$$\sigma = \frac{\pi}{\ln 2} \times \frac{V}{I}$$

where:
σ = surface resistivity (Ω/□)
V = the measured voltage (V)
I = the source current (A)

Note that the units for sheet resistivity are expressed as ohms per square (Ω/□) in order to distinguish this number from the measured resistance (V/I), which is simply expressed in ohms. Correction factors to the resistivity calculation may be required for extremely thin or thick samples or if the diameter of the sample is small relative to the probe spacing.

If the thickness of the sample is known, the volume resistivity can be calculated as follows:

$$\rho = \frac{\pi}{\ln 2} \times \frac{V}{I} \times t \times k$$

where:
ρ = volume resistivity (Ω-cm)
t = the sample thickness (cm)
k = a correction factor* based on the ratio of the probe spacing to wafer diameter and on the ratio of wafer thickness to probe spacing

* The correction factors can be found in a standard four-point probe resistivity test procedure such as *Semi MF84: Standard Test Method for Measuring Resistivity of Silicon Wafers With an In-Line Four-Point Probe*. This standard was originally published by ASTM International as ASTM F 84.

Using the Four-Point Probe ITMs, *HiR* and *LoR*

The *"HiR"* and *"LoR"* ITMs are both used for making four-point collinear probe measurements. The *"HiR"* ITM can be used for materials over a wide resistance range, ~1mΩ to 1TΩ. The Model 4200-PA preamps are required for making high resistance measurements (>1MΩ). The *"LoR"* ITM is intended for measurements of lower resistance materials (~1mΩ–1kΩ).

A screenshot of the *"HiR"* ITM for measuring four-probe resistivity is shown in ***Figure 19***.

The *"HiR"* ITM uses either three or four SMU instruments to make the resistivity measurements. One SMU instrument (SMU1) and the ground unit (GNDU) are used to source current between the outer two probes. Two other SMU instruments (SMU2 and SMU3) are used to measure the voltage drop between the two inner probes. The Force HI terminal of each SMU instrument is connected to each of the four probes. The SMU instrument designation for this configuration is shown in ***Figure 20***.

In the Formulator, the voltage difference between SMU2 and SMU3 is calculated and the resistance and sheet resistivity are derived from the voltage difference. The results appear in the Sheet tab of the ITM.

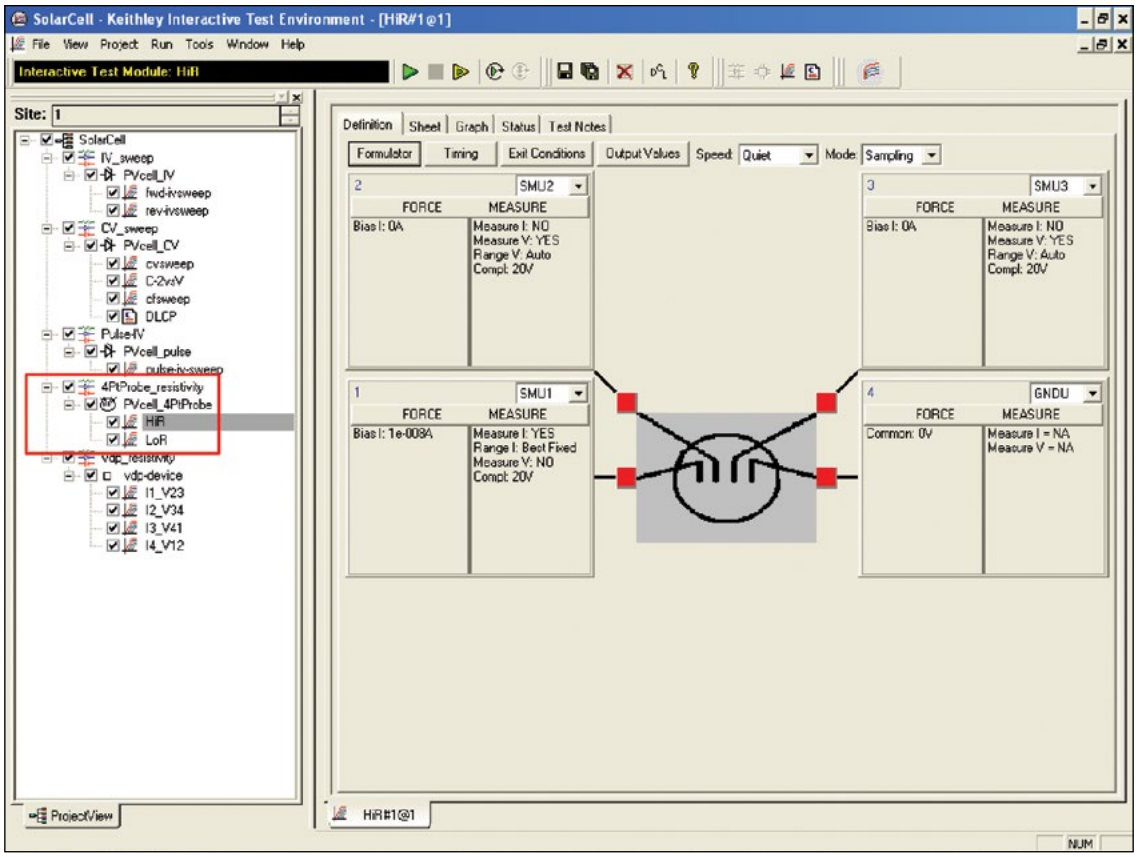

Figure 19. "HiR" test module for measuring resistivity

When making high resistance measurements, potential sources of error need to be considered in order to make optimal measurements. Use a probe head that has a level of insulation resistance between the probes that is sufficiently higher than the resistance of the material to be measured. This will help prevent errors due to leakage current through the probe head. Ensure that the measurement circuit is electrostatically shielded by enclosing the circuit in a metal shield. The shield is connected to the LO terminal of the 4200. The LO terminal is located on the GNDU or on the outside shell of the triax connectors. Use triax cables to produce a guarded measurement circuit. This will prevent errors due to leakage current and significantly reduce the test time. Finally, the Model 4200-PA preamp option is required to source very small currents (nanoamp and picoamp range) and to provide high input impedance (>1E16 ohms) to avoid loading errors when measuring the voltage difference.

The *"LoR"* ITM is only used for lower resistance materials and requires only one or two SMU instruments. In this case, the Force and Sense terminals of the SMU instruments are connected to the four-point probe as shown in ***Figure 20***.

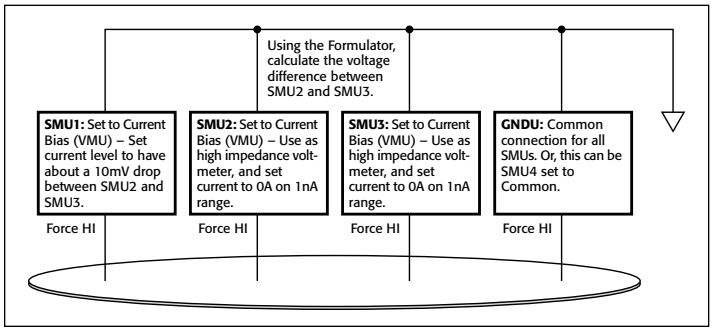

Figure 20. SMU instrument designation for four-point collinear probe measurements

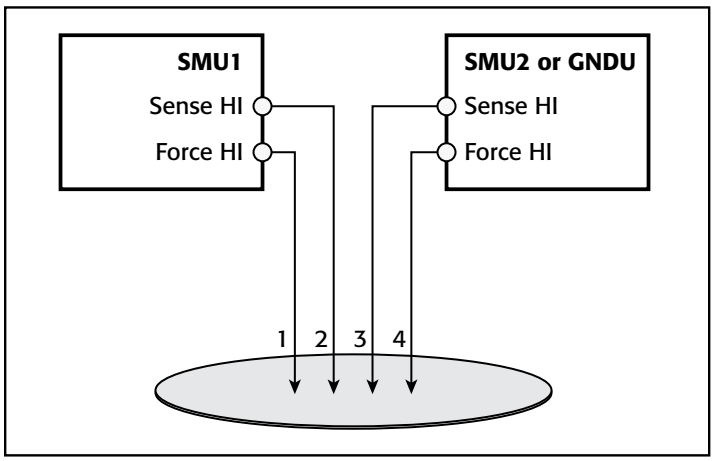

Figure 21. Connecting two SMU instruments for four-point probe measurements

In the configuration shown in ***Figure 21***, the Force HI terminal SMU1 sources the current through Probe 1. The voltage difference between Probes 2 and 3 is measured through the Sense terminals of the two SMU instruments.

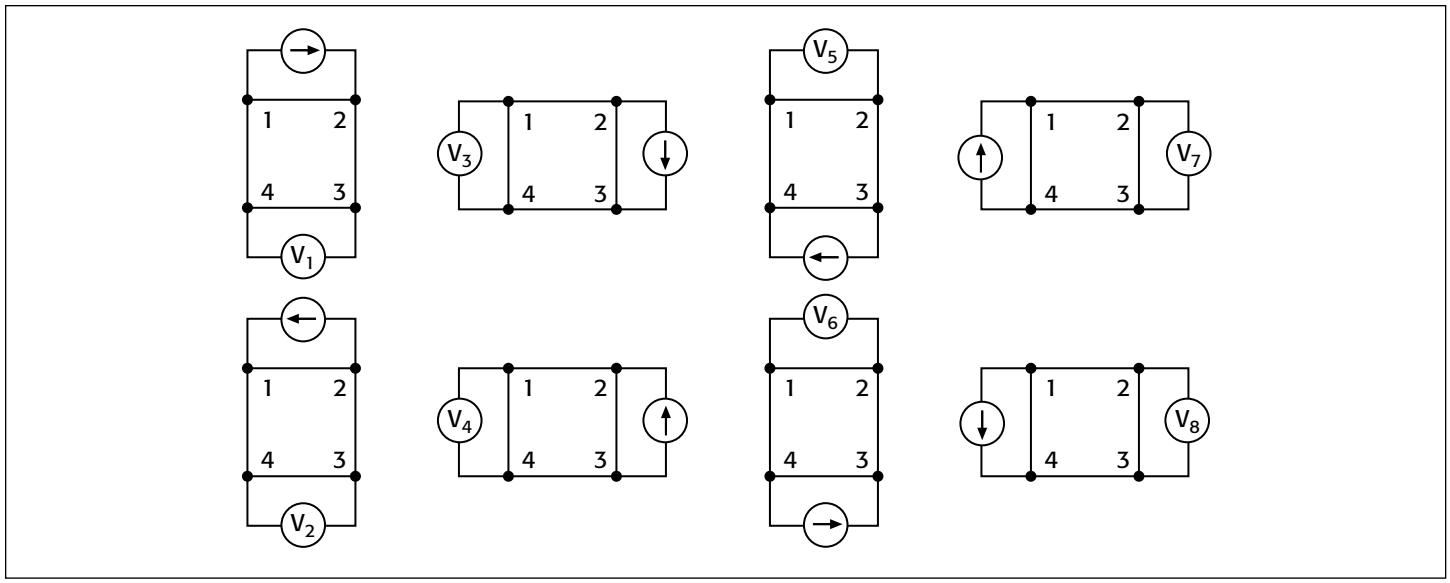

Figure 22. Van der Pauw resistivity measurement conventions

To compensate for thermoelectric offset voltages, two voltage measurements are made with currents of opposite polarity. The two measurements are combined and averaged to cancel the thermoelectric EMFs. The *"LoR"* ITM performs this offset correction automatically by sourcing the two current values in the List Sweep and then mathematically correcting for the offsets in the Formulator. The corrected resistance and sheet resistivity are displayed in the Sheet tab.

Measuring Resistivity with the van der Pauw Method

The van der Pauw (vdp) technique for measuring resistivity uses four isolated contacts on the boundary of a flat, arbitrarily shaped sample. The resistivity is derived from eight measurements made around the sample as shown in ***Figure 22***.

Once all the voltage measurements have been taken, two values of resistivity, ρ_A and ρ_B, are derived as follows:

$$\rho_A = \frac{\pi}{\ln 2} f_A t_s \frac{(V_2 + V_4 - V_1 - V_3)}{4I}$$

$$\rho_B = \frac{\pi}{\ln 2} f_B t_s \frac{(V_6 + V_8 - V_5 - V_7)}{4I}$$

where:

ρ_A and ρ_B are volume resistivities in ohm-cm;

t_s is the sample thickness in cm;

V_1–V_8 represent the voltages measured by the voltmeter;

I is the current through the sample in amperes;

f_A and f_B are geometrical factors based on sample symmetry, and are related to the two resistance ratios Q_A and Q_B as shown in the following equations ($f_A = f_B = 1$ for perfect symmetry).

Q_A and Q_B are calculated using the measured voltages as follows:

$$Q_A = \frac{V_2 - V_1}{V_4 - V_3}$$

$$Q_B = \frac{V_6 - V_5}{V_8 - V_7}$$

Also, Q and f are related as follows:

$$\frac{Q - 1}{Q + 1} = \frac{f}{0.693} \operatorname{arc\,cosh}\left(\frac{e^{0.693/f}}{2}\right)$$

A plot of this function is shown in ***Figure 23***. The value of "f" can be found from this plot once Q has been calculated.

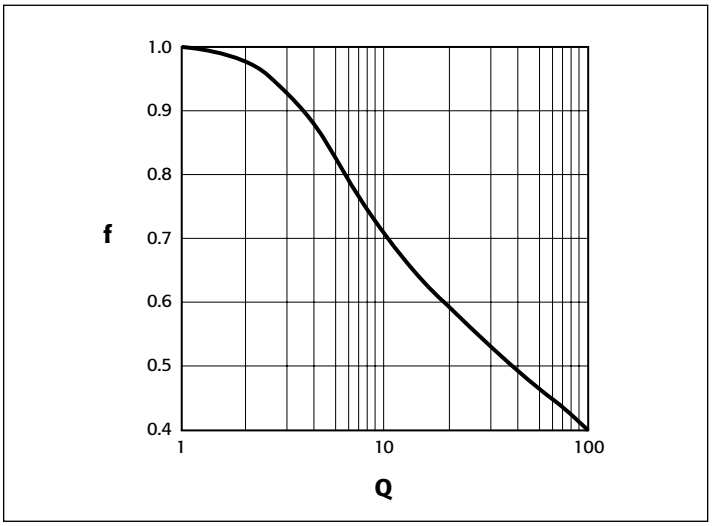

Figure 23. Plot of f vs. Q

Once ρ_A and ρ_B are known, the average resistivity (ρ_{AVG}) can be determined as follows:

$$\rho_{AVG} = \frac{\rho_A + \rho_B}{2}$$

Using the *vdp_resistivity* subsite and vdp method ITMs

To automate the vdp resistivity measurements, the *SolarCell* project has a *vdp-resistivity* subsite with four ITMs: *"I1_V23"*,

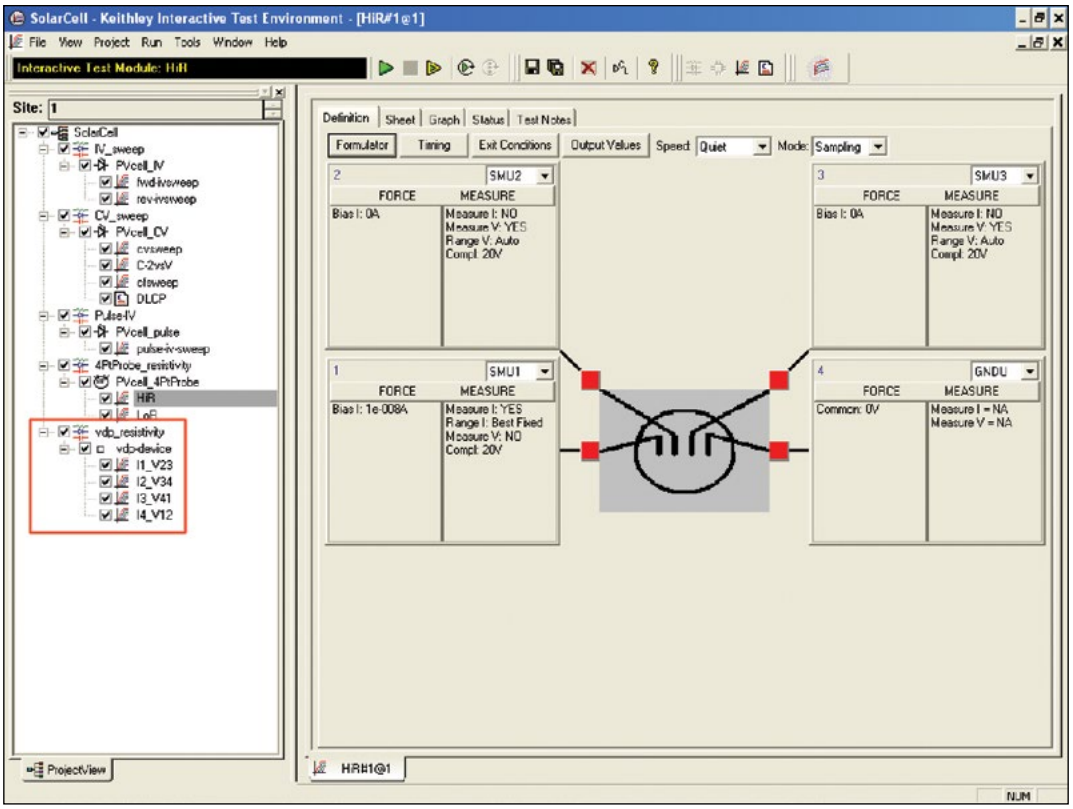

Figure 24. Screenshot of van der Pauw test

"*I2_V34*", "*I3_V41*", and "*I4_V12*." A screenshot of the test is shown in ***Figure 24***.

Each terminal of the sample is connected to the Force HI terminal of an SMU instrument, so a Model 4200-SCS with four SMU instruments is required. The four SMU instruments are configured differently in each of the four ITMs – one SMU instrument supplies the test current, two are configured as voltmeters, and one is set to common. This measurement setup is repeated around the sample, with each of the four SMU instruments serving a different function

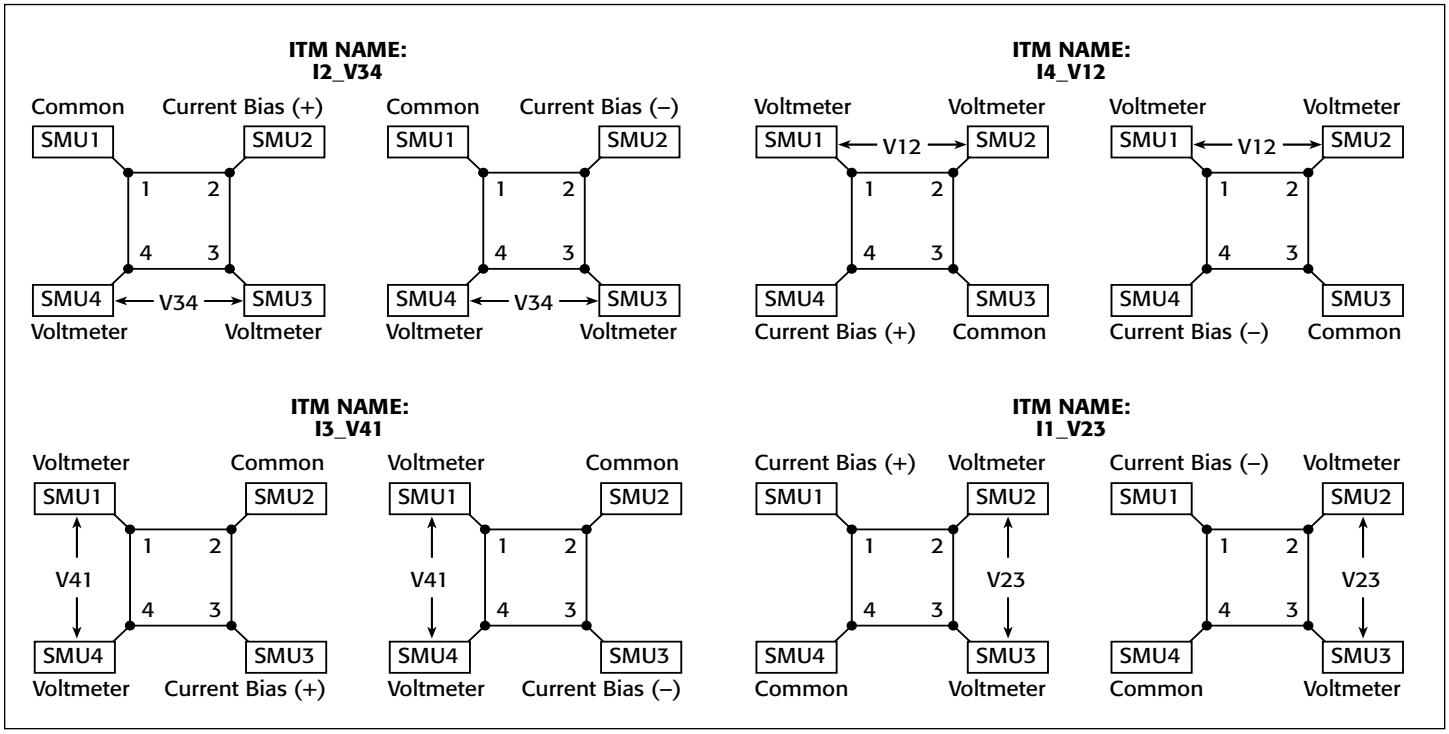

Figure 25. SMU instrument configurations for van der Pauw measurements

in each of the four ITMs. A diagram of the function of each SMU instrument in each ITM is shown in ***Figure 25***.

Adjusting the Test Parameters

Before executing the test, some of the test parameters must be adjusted based on the sample to be tested. In particular, it's necessary to specify the source current, the settling time, and the thickness of the material.

Input Source Current: Before running the project, input the current source values based on the expected sample resistance. Adjust the current so that the voltage difference will not exceed approximately 25mV to keep the sample in thermal equilibrium. In each of the four ITMs, enter both polarities of the test current. The same magnitude must be used for each ITM.

Input the Settling Time: For high resistance samples, it will be necessary to determine the settling time of the measurements. This can be accomplished by creating an ITM that sources current into two terminals of the samples and measures the voltage drop on the adjacent two terminals. The settling time can be determined by taking multiple voltage readings and then graphing the voltage difference as a function of time.

This settling time test can be generated by copying and then modifying one of the existing vdp ITMs. Switch the source function from the sweep mode to the sampling mode. Then, in the Timing menu, take a few hundred or so readings with a delay time of one second. Make sure that the "Timestamp Enabled" box is checked. After the readings are done, plot the voltage difference vs. time on the graph. The settling time is determined by observing the graph and finding the time when the reading is within the desired percentage of the final value.

Input the Thickness of the Sample: Enter the thickness of the sample into the Calc sheet at the subsite level. Select the subsite *vdp_resistivity*. Go to the Subsite Data *vdp-device* tab. It contains the output values of the voltage differences and test current. From the Calc tab, the thickness can be adjusted. The default thickness is 1cm.

Input Correction Factor: The resistivity formula found in the Calc sheet at the subsite level also allows inputting a correction factor, if necessary. The resistivity is multiplied by this number, which may be based on the geometry or uniformity of the sample. By default, the correction factor is 1.

Running the Project

The van der Pauw resistivity measurements must be run at the subsite level. Make sure that all four checkboxes in front of the vdp ITMs (*"I1_V23*," *"I2_V34*," *"I3_V41*," and *"I4_V12"*) are checked and then click on the subsite *vdp_resistivity*. Execute the project by using the subsite Run button (circular arrow). Each time the test is run, the subsite data is updated. The voltage differences from each of the four ITMS will appear in the Subsite Data

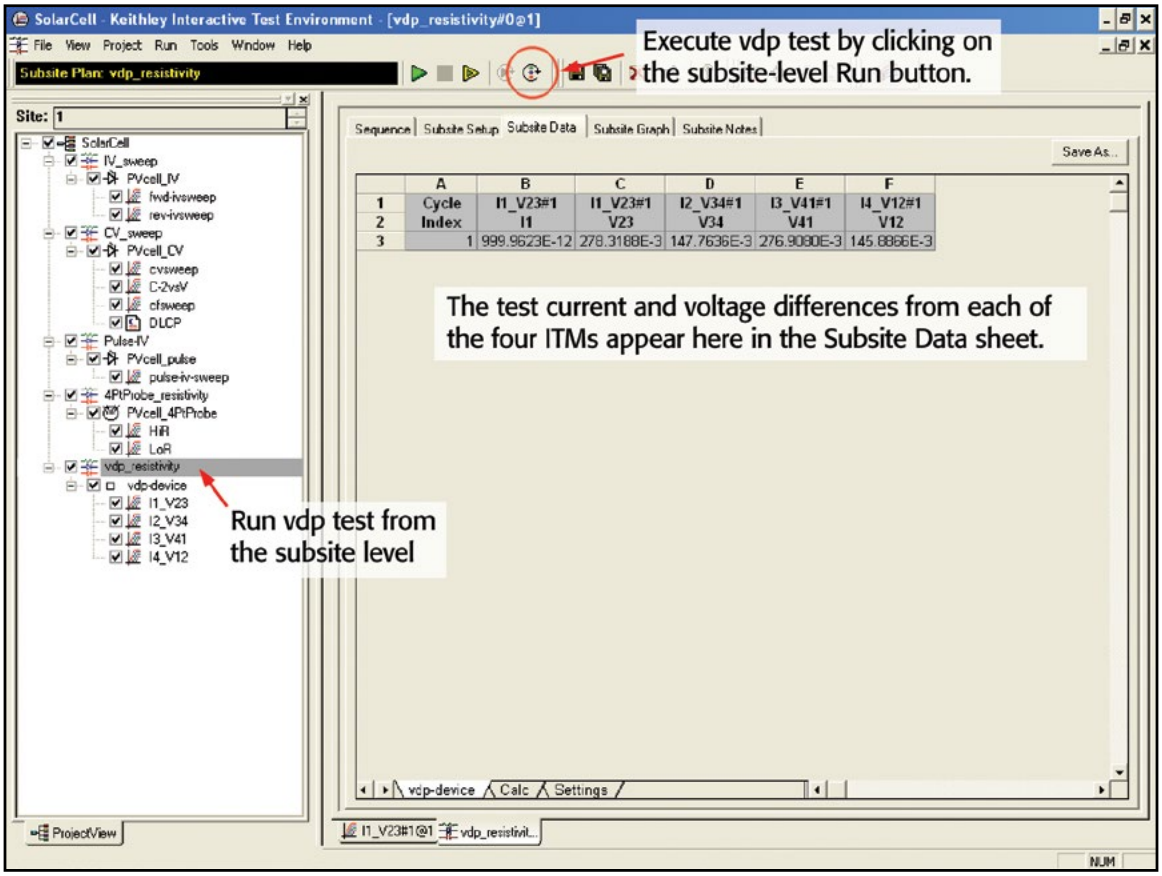

Figure 26. Executing the vdp_resistivity test

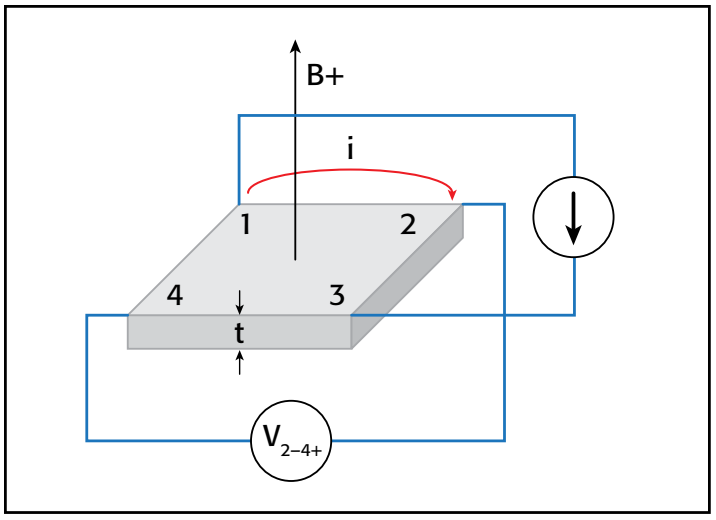

Figure 27. Hall voltage measurement

vdp-device Sheet tab. The resistivity will appear in the Subsite Data Calc sheet as shown in ***Figure 26***.

Hall Voltage Measurements

Hall effect measurements are important to semiconductor material characterization because the conductivity type, carrier density, and Hall mobility can be derived from the Hall voltage. With an applied magnetic field, the Hall voltage can be measured using the configuration shown in ***Figure 27***.

With a positive magnetic field (B–), apply a current between Terminals 1 and 3 of the sample, and measure the voltage drop (V_{2-4+}) between Terminals 2 and 4. Reverse the current and measure the voltage drop (V_{4-2+}). Next, apply current between Terminals 2 and 4, and measure the voltage drop (V_{1-3+}) between Terminals 1 and 3. Reverse the current and measure the voltage drop (V_{3-1+}) again.

Reverse the magnetic field (B–) and repeat the procedure, measuring the four voltages: (V_{2-4-}), (V_{4-2-}), (V_{1-3-}), and (V_{3-1-}). ***Table 3*** summarizes the Hall voltage measurements.

Table 3. Summary of Hall Voltage Measurements

Voltage Designation	Magnetic Flux	Current Forced Between Terminals	Voltage Measured Between Terminals
V2–4+	B+	1–3	2–4
V4–2+	B+	3–1	4–2
V1–3+	B+	2–4	1–3
V3–1+	B+	4–2	3–1
V2–4–	B–	1–3	2–4
V4–2–	B–	3–1	4–2
V1–3–	B–	2–4	1–3
V3–1–	B–	4–2	3–1

From the eight Hall voltage measurements, the average Hall coefficient can be calculated as follows:

$$R_{HC} = \frac{t(V_{4-2+} - V_{2-4+} + V_{2-4-} - V_{4-2-})}{4BI}$$

$$R_{HD} = \frac{t(V_{3-1+} - V_{1-3+} + V_{1-3-} - V_{3-1-})}{4BI}$$

where:

R_{HC} and R_{HD} are Hall coefficients in cm^3/C;

t is the sample thickness in cm;

V represents the voltages measured in V;

I is the current through the sample in A;

B is the magnetic flux in Vs/cm^2

Once R_{HC} and R_{HD} have been calculated, the average Hall coefficient (R_{HAVG}) can be determined as follows:

$$R_{HAVG} = \frac{R_{HC} + R_{HD}}{2}$$

From the resistivity (ρ_{AVG}) and the Hall coefficient (R_H), the Hall mobility (μ_H) can be calculated:

$$\mu_H = \frac{|R_H|}{\rho_{AVG}}$$

Using the Model 4200-SCS to Measure the Hall Voltage

The *SolarCell* project does not include a specific test to measure the Hall voltage; however, four ITMs can be added to the subsite for determining the Hall coefficient and mobility. Given that the configuration for the Hall measurements is very similar to the van der Pauw resistivity measurements, the vdp ITMs can be copied and modified for making the Hall voltage measurements. The modifications involve changing the functions of the SMU instruments. ***Figure 28*** illustrates how to configure the four SMU instruments in the ITMs to measure the Hall voltage. Use the Output Value checkboxes on the Definition tab to return the Hall voltages to the subsite-level Calc sheet.

User Test Modules (UTMs) must be added to control the magnet. For a GPIB-controlled electromagnet, users can write a program using KULT (the Keithley User Library Tool) to control the magnitude and polarity of the electromagnet. The code can be opened up in a UTM within the project. Information on writing code using KULT is provided in Section 8 of the Model 4200-SCS Reference Manual.

If a permanent magnet is used, UTMs can be employed to create a Project Prompt that will stop the test sequence in the project tree and instruct the user to change the polarity of the magnetic field applied to the sample. A Project Prompt is a dialog window that pauses the project test sequence and prompts the user to perform some action. See Section A of the Model 4200-SCS Reference Manual for a description of how to use Project Prompts.

Finally, the Hall coefficient and mobility can be derived in the subsite-level Calc sheet. These math functions can be added to the other equations for determining resistivity.

Conclusion

Measuring the electrical characteristics of a solar cell is critical for determining the device's output performance and efficiency. The Model 4200-SCS simplifies cell testing by automating the I-V, C-V, pulsed I-V, and resistivity measurements and provides

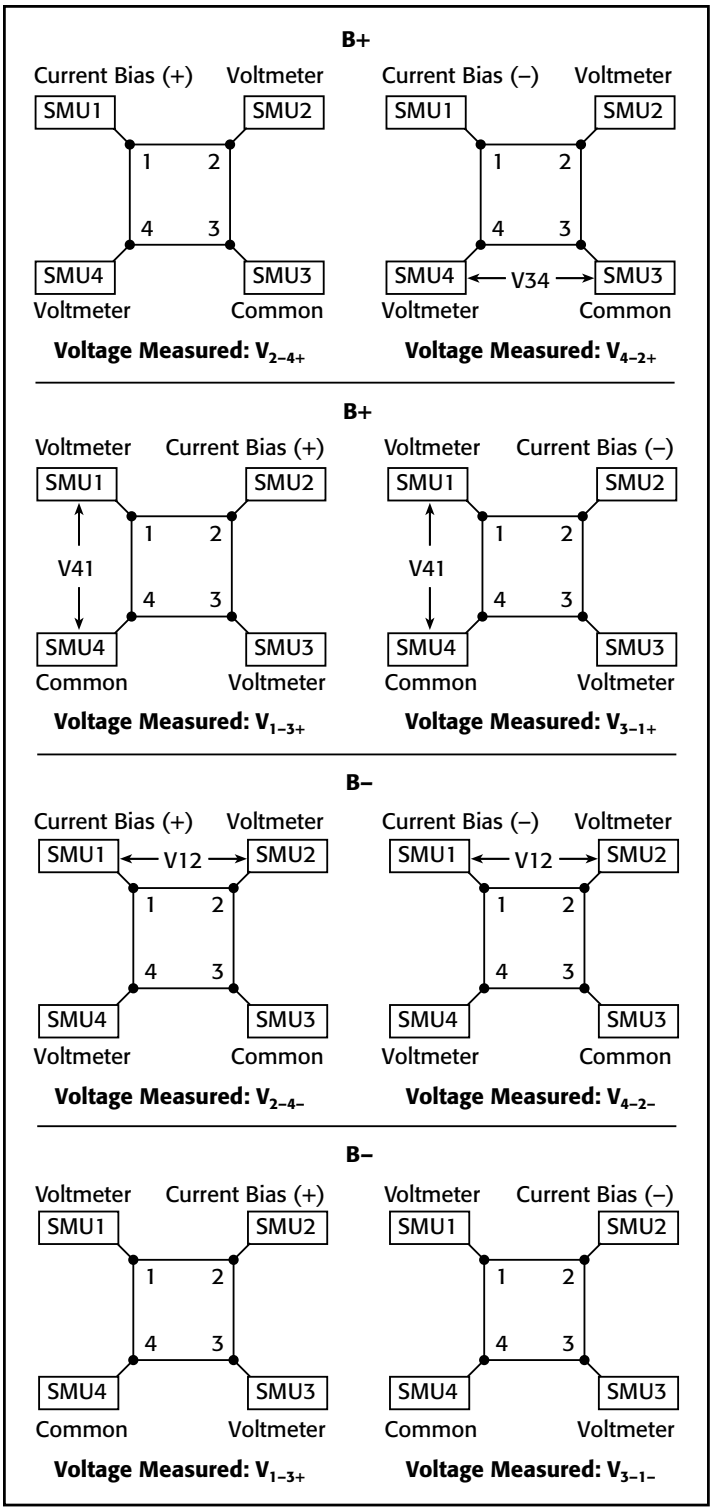

Figure 28. SMU configurations for Hall voltage measurements

graphics and analysis capability. For measurements of currents greater than 1A, Keithley offers Series 2400 and Series 2600B SourceMeter Instruments that can be used for solar cell testing. Information on these models and further information on making solar cell measurements can be found on Keithley's website: www.keithley.com.

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