

PCB Layout Considerations for Non-Isolated Switching Power Supplies

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Introduction

The best news when you power up a prototype supply board for the very first time is when it not only works, but also runs quiet and cool. Unfortunately, this does not always happen. A common problem of switching power supplies is “unstable” switching waveforms. Sometimes, waveform jittering is so pronounced that audible noise can be heard from the magnetic components. If the problem is related to the printed circuit board (PCB) layout, identifying the cause can be difficult. This is why proper PCB layout at the early stage of a switching supply design is very critical. Its importance cannot be overstated.

The power supply designer is the person who best understands the technical details and functional requirements of the supply within the final product. He or she should work closely with the PCB layout designer on the critical supply layout from the beginning. A good layout design optimizes supply efficiency, alleviates thermal stress, and most importantly, minimizes the noise and interactions among traces and components. To achieve these, it is important for the designer to understand the current conduction paths and signal flows in the switching power supply. The following discussion presents design considerations for a proper layout design for non-isolated switching power supplies.

PLAN OF THE LAYOUT

Location of the Power Supply in System Board

For the embedded DC/DC supply on a large system board, the supply output should be located close to the load devices in order to minimize the interconnection impedance and the conduction voltage drop across the PCB traces to achieve best voltage regulation, load transient response and system efficiency. If forced-air cooling is available, the supply should also be located close to the cooling fan or have good air flow to limit the thermal stress. In addition, the large passive components such as inductors

and electrolytic capacitors should not block the air flow to the low profile, surface mount semiconductor components such as power MOSFETs, PWM controller, etc. To prevent the switching noise from upsetting other analog signals in the system, avoid routing sensitive signal traces underneath the supply if possible. Otherwise, an internal ground plane between the power supply layer and small signal layer is needed for shielding.

It is necessary to point out that this power supply location and board real estate planning should be done at the early design/planning stage of the system. Unfortunately, sometimes people focus on other more “important” or “exciting” circuits on the big system board first. If power management/supply is the last thought and is relegated to whatever space is left on the board, this certainly does not help ensure efficient and reliable power supply design.

Placement of Layers

On a multilayer PCB board, it is highly desirable to place the DC ground or DC input or output voltage layers between the high current power component layer and the sensitive small signal trace layer. The ground and/or DC voltage layers provide AC grounds to shield the small signal traces from noisy power traces and power components. As a general rule, the ground or DC voltage planes of a multilayer PCB should not be segmented. If the segmentation is unavoidable, the number and length of traces in these planes must be minimized. The traces should also be routed in the same direction as the high current flow direction to minimize the impact.

Figures 1a and 1c provide examples of the undesired layer arrangement of the 6-layer and 4-layer PCB boards for switching power supply. In these examples, the small signal layer is sandwiched between the high current power layer and the ground layer. These configurations increase the

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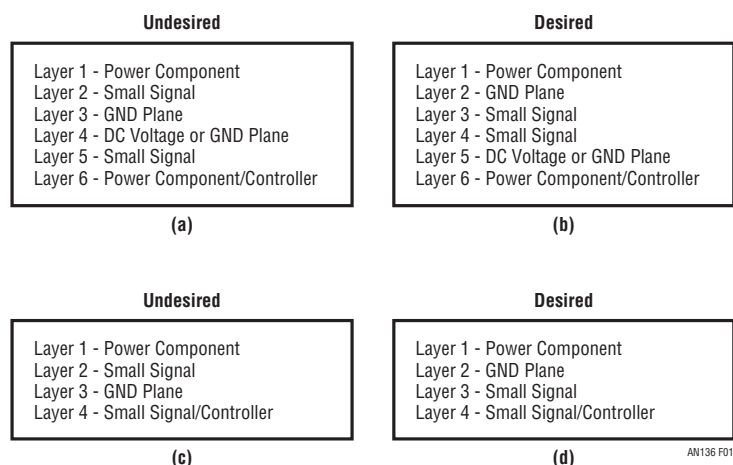


Figure 1. Desired and Undesired Layer Arrangement of 6-Layer and 4-Layer PCBs

capacitive noise coupling between the high current/voltage power layer and small analog signal layer. To minimize the noise coupling, Figures 1b and 1d show examples of desired layer arrangement for 4-layer and 6-layer PCB designs. In these two examples, the small signal layer is shielded by the ground layer(s). It is important to always have a ground layer next to the outside power stage layer. Finally, it is also desirable to have thick copper for the external high current power layers to minimize the PCB conduction loss and thermal impedance.

POWER STAGE COMPONENT LAYOUT

A switching power supply circuit can be divided into the power stage circuit and the small signal control circuit. The power stage circuit includes the components that conduct high current. In general, these components should be placed first. The small signal control circuitry is subsequently placed in specific spot in the layout. In this section, we will discuss the layout of power stage components.

Continuous and Pulsating Current Paths – Minimize Inductance in High di/dt Loop (Hot Loop)

The large current traces should be short and wide to minimize PCB inductance, resistance and voltage drop. This is especially critical for the traces with high di/dt pulsating current flow. Figure 2 identifies the continuous current and pulsating current paths in a synchronous buck converter.

The solid line represents the continuous current paths, and the dashed line represents the pulsating (switching) current paths. The pulsating current paths include the traces connected to the input decoupling ceramic capacitor, C_{HF} , the top control FET, Q_T , the bottom synchronous FET, Q_B , and its optional paralleled Schottky diode. Figure 3a shows the parasitic PCB inductors in these high di/dt current paths. Due to the parasitic inductance, the pulsating current paths not only radiate magnetic fields, but also generate high voltage ringing and spikes across the PCB traces and MOSFETs. To minimize the PCB inductance, this pulsating current loop (hot loop) should be laid out so that it has a minimum circumference and is composed of traces that are short and wide. The high frequency decoupling capacitor, C_{HF} , should be a 0.1 μ F to 10 μ F, X5R or X7R dielectric ceramic capacitor with very low ESL and ESR. Higher-capacitance dielectrics (such as Y5V) can allow a large reduction in capacitance over voltage and temperature. Therefore, these kinds of capacitors are not preferred for C_{HF} .

Figure 3b provides a layout example of the critical pulsating current loop (hot loop) in the buck converter. To limited resistive voltage drops and the number of vias, power components should be placed on the same side of board, with power traces routed on the same layer. When it becomes necessary to route a power trace to another layer, choose a trace in the continuous current paths. When vias are used to connect PCB layers in the high current loop, multiple vias should be used to minimize via impedance.

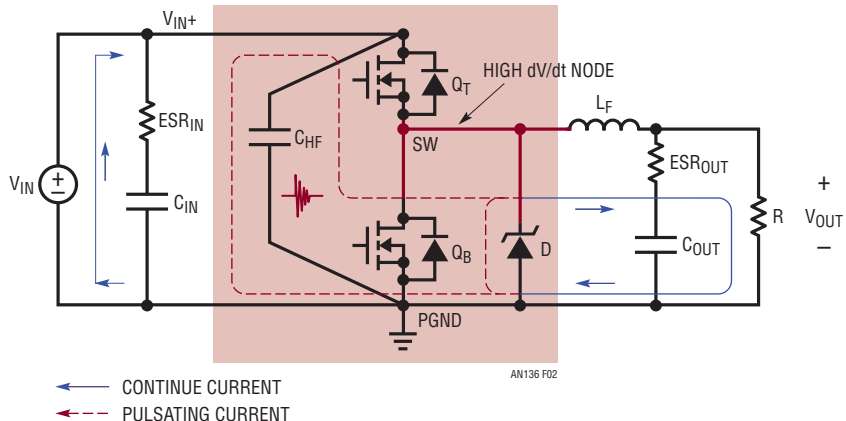


Figure 2. Continuous and Pulsating Current Paths of a Synchronous Buck Converter

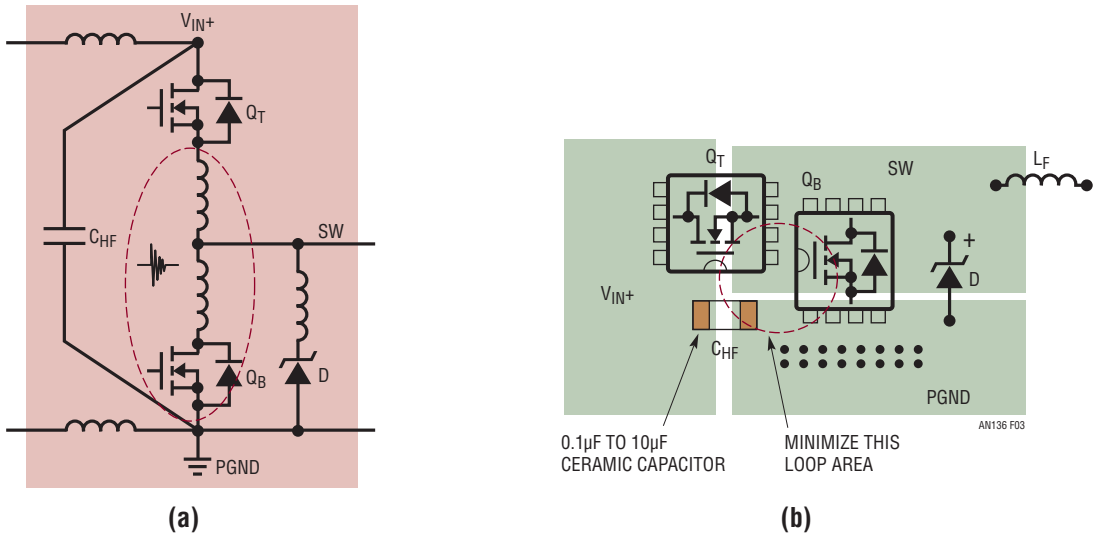


Figure 3. Minimize the High di/dt Loop Area in the Synchronous Buck Converter. (a) High di/dt loop (Hot Loop) and its Parasitic PCB Inductors, (b) Layout Example

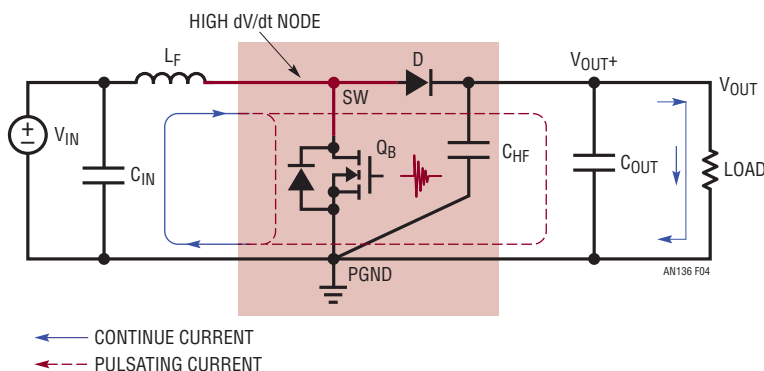


Figure 4. Continuous and Pulsating Current Paths of a Boost Converter

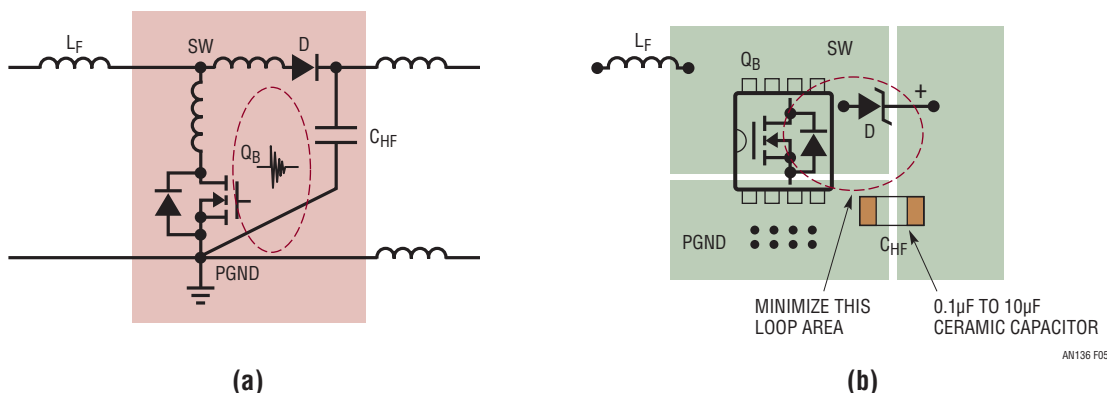


Figure 5. Minimize the High di/dt Loop Area in the Boost Converter.
(a) High di/dt Loop (Hot Loop) and its Parasitic PCB Inductors, (b) Layout Example

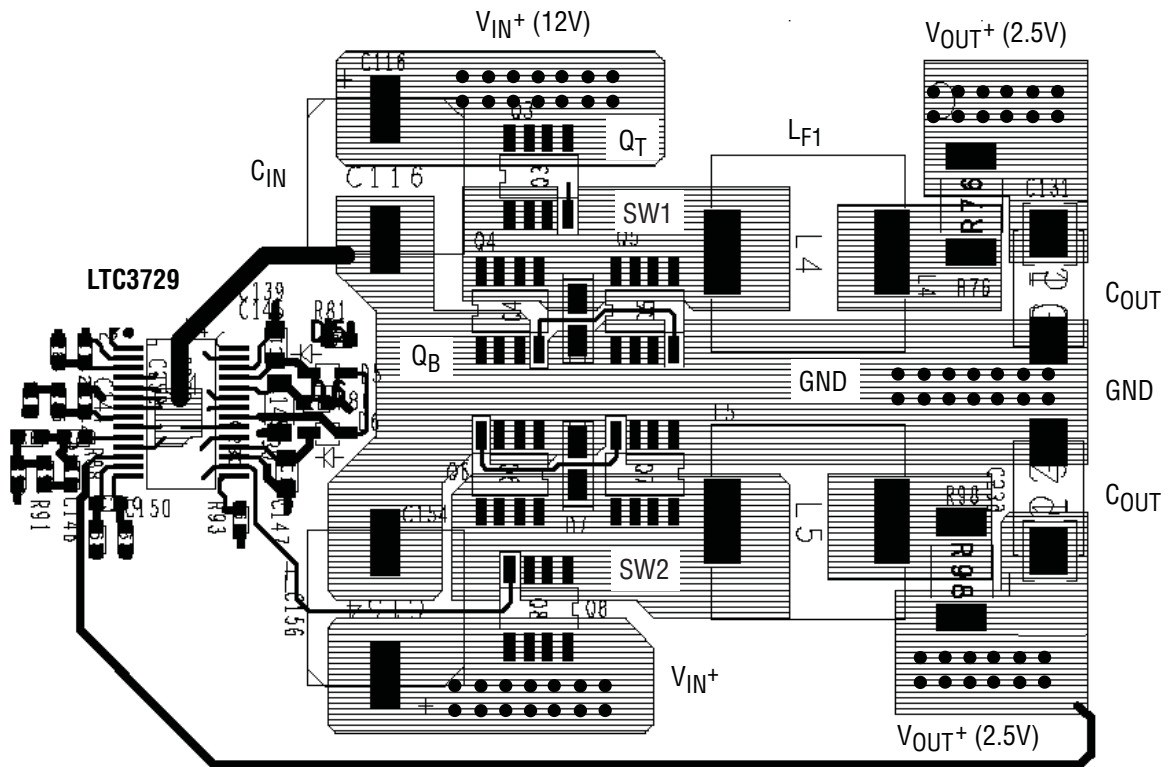
Similarly, Figure 4 shows the continuous and pulsating current loops (hot loop) in the boost converter. In this case, the high frequency ceramic capacitor, C_{HF} , should be placed on the output side close to the MOSFET, Q_B , and boost diode, D . The loop formed by switch, Q_B , rectifier diode, D , and high frequency output capacitor, C_{HF} , must be minimized. Figure 5 shows the layout example of the pulsating current loop in the boost converter.

To emphasize the importance of the decoupling capacitor C_{HF} , Figures 6 and 7 provide an actual example of a synchronous buck circuit. Figure 6a shows the layout of a dual phase, $12V_{IN}$ to $2.5V_{OUT}/30A$ max, synchronous buck supply using the LTC3729 2-phase, single V_{OUT} controller IC. As shown in Figure 6a, the switching nodes SW1 and SW2 and output inductor current i_{LF1} waveforms are stable at no load. But if the load current increases to above 13A, the SW1 node waveform starts missing cycles. The problem becomes even worse with higher load

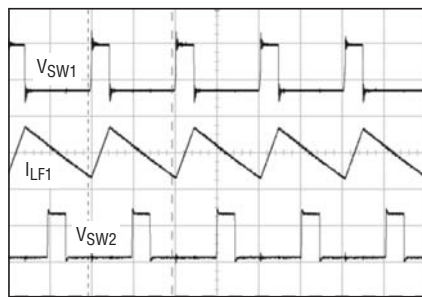
current. Figure 7 shows that adding one $1\mu F$ high frequency ceramic capacitors on each channel's input side solves the problem. It separates and minimizes the hot loop area of each channel. The switching waveform is stable even with maximum load current up to 30A.

Isolate and Minimize High dv/dt Switching Area

In Figures 2 and 4, the SW node voltage swings between V_{IN} (or V_{OUT}) and ground with a high dv/dt rate. This node is rich in high frequency noise components and is a strong source of EMI noise. To minimize the coupling capacitance between SW node and other noise-sensitive traces, the SW copper area should be minimized. However, on the other hand, to conduct high inductor current and provide a heat sink to the power MOSFET, the SW node PCB area cannot be too small. It is usually preferred to have a ground copper area placed underneath this SW node to provide additional shielding.



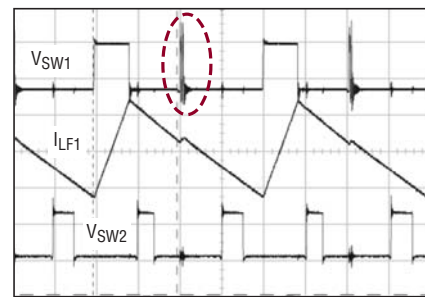
(a)



$I_{OUT} = 0A$

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(b)



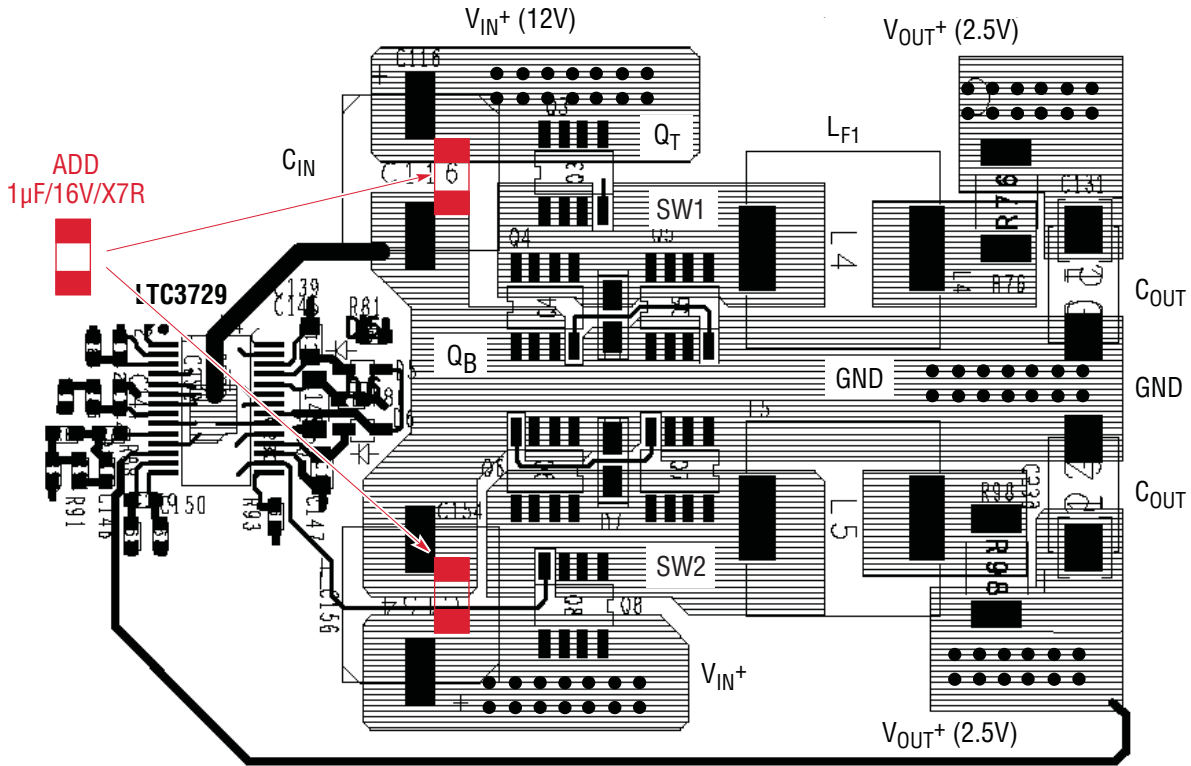
$I_{OUT} = 13.3A$

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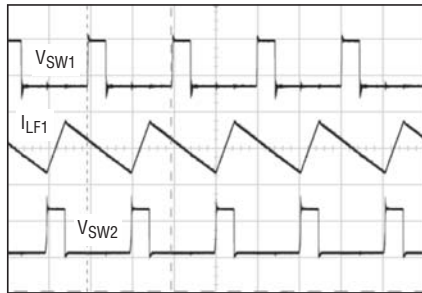
(c)

Figure 6. An Example of a 2-Phase, 2.5V/30A Output Buck Converter with Noise Problem.
 (a) Layout, (b) Switching Waveform at $I_{OUT} = 0A$, (c) Switching Waveform at $I_{OUT} = 13.3A$

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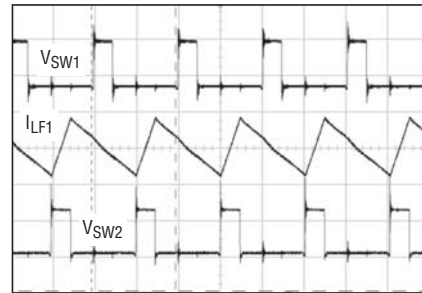


(a)



$I_{OUT} = 0A$

(b)



$I_{OUT} = 30A$

(c)

Figure 7. Adding Two 1µF High Frequency Input Capacitors Solves the Problem.
 (a) Layout with Added Capacitors, (b) Switching Waveform at $I_{OUT} = 0A$,
 (c) Switching Waveform at $I_{OUT} = 30A$

Sufficient Copper Area to Limit Power Component Thermal Stress

In a design without external heat sinks for surface mounted power MOSFETs and inductors, it is necessary to have sufficient copper area as a heat sink. For a DC voltage node, such as input/output voltage and power ground, it is desirable to make the copper area as large as possible. Multiple vias are helpful in further reducing thermal stress. For the high dv/dt SW nodes, the proper size of the SW node copper area is a design trade-off between minimizing the dv/dt related noises and providing good heat sinking capability for the MOSFETs.

Proper Land Pattern of Power Components to Minimize Impedance

It is important to pay attention to the land (or pad) pattern of power components, such as low ESR capacitors, MOSFETs, diodes and inductors. Figures 8a and 8b show examples of undesired and desired power component land patterns, respectively. As shown in Figure 8b, for a

decoupling capacitor, the positive and negative via pair should be as close to each other as possible to minimize the PCB equivalent series inductance (ESL). This is especially effective for capacitors with low ESL. Large valued low ESR capacitors are usually more expensive. Improper land pattern and poor routing can degrade their performance and thus increase overall cost. In general, the desired land patterns reduce the PCB noise, reduce thermal impedance, and minimize trace impedance and voltage drops for the high current components.

One common mistake in high current power component layout is the improper use of thermal relief land patterns, as shown in Figure 8a. Unnecessary use of thermal relief land patterns increases the interconnection impedance of power components. This results in higher power losses and decreases the decoupling effect of low ESR capacitors. If vias are used to conduct high current, sufficient numbers of via must be used to minimize via impedance. Similarly, the thermal relief should not be used for those vias.

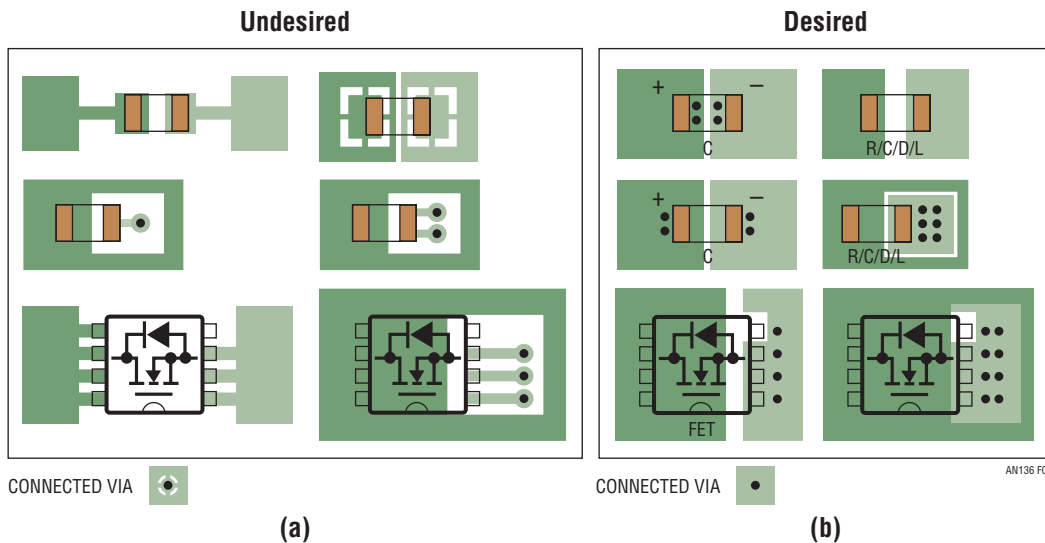


Figure 8. Desired and Undesired Land Patterns for Power Components.
(a) Improper Use of Thermal Relief for the Pads of Power Components,
(b) Recommended Land Patterns for Power Components

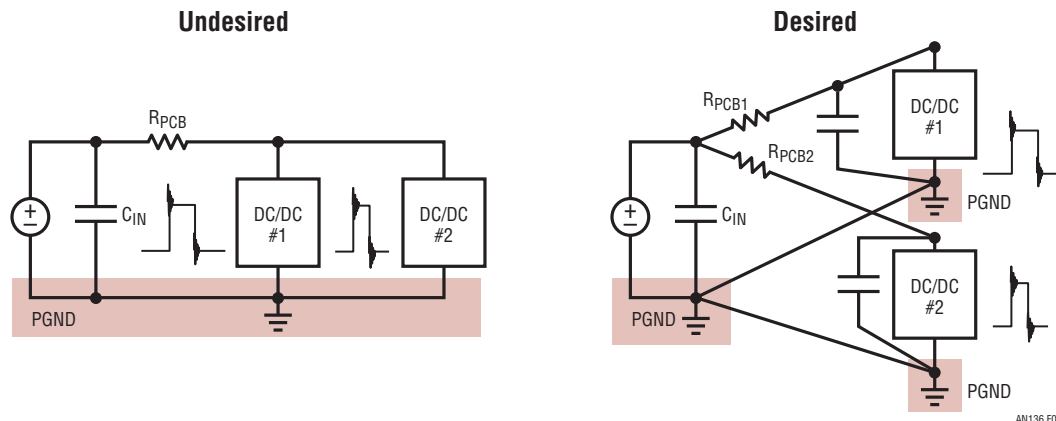


Figure 9. Separate the Input Current Paths Among Supplies

Separation of Input Current Paths Among Supplies

Figure 9 shows an application with several onboard switching supplies sharing the same input voltage rail. When these supplies are not synchronized to each other, it is necessary to separate the input current traces to avoid common impedance noise coupling between different power supplies. It is less critical to have local input decoupling capacitor for each power supply.

PolyPhase®, Single Output Converter

For a PolyPhase, single output converter, try to have symmetric layout for each phase. This helps to balance thermal stresses.

Layout Design Example – 1.2V/40A Dual Phase Buck Converter

Figure 10 provides a design example of a 4.5V to 14V_{IN} to 1.2V/40A max dual phase synchronous buck converter using PolyPhase current mode step-down controller, the LTC3855. Before the start of PCB layout, one good practice is to highlight the schematic traces for the high current traces, the noisy high dv/dt traces and the sensitive small signal traces with different colors, so the PCB designer understands the differences between these traces. Figure 11 shows the power stage layout example of the power component layer of this 1.2V/40A supply. In this figure, the Q_T is the top side control MOSFET and Q_B is the bottom side synchronous FET. An optional Q_B footprint is added for even more output current. A solid power ground plane layer is placed just underneath the power component layer.

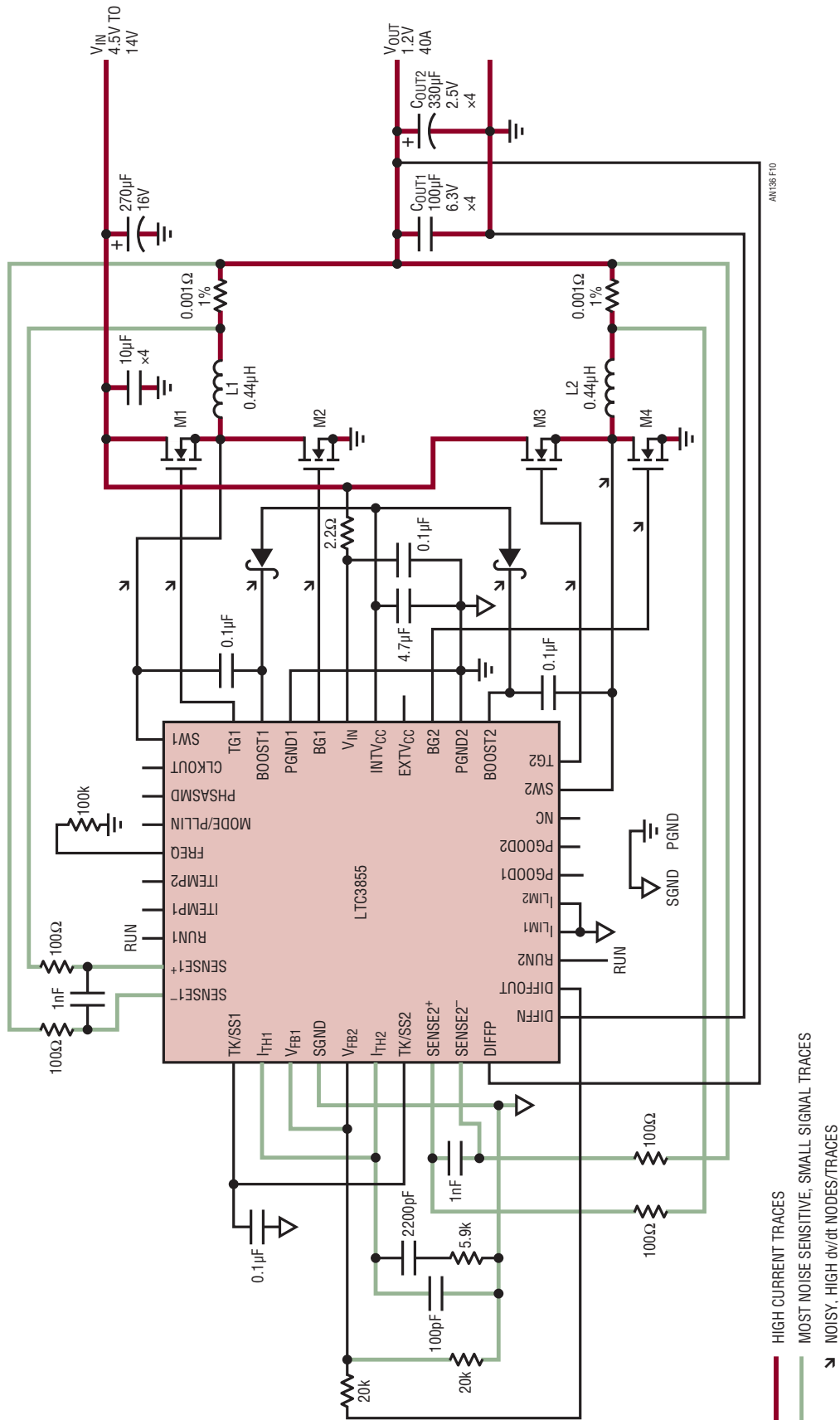


Figure 10. Dual Phase 1.2V/40A Max LTC3855 Buck Converter

- HIGH CURRENT TRACES
- MOST NOISE SENSITIVE, SMALL SIGNAL TRACES
- ↗ NOISY, HIGH dv/dt NODES/TRACES

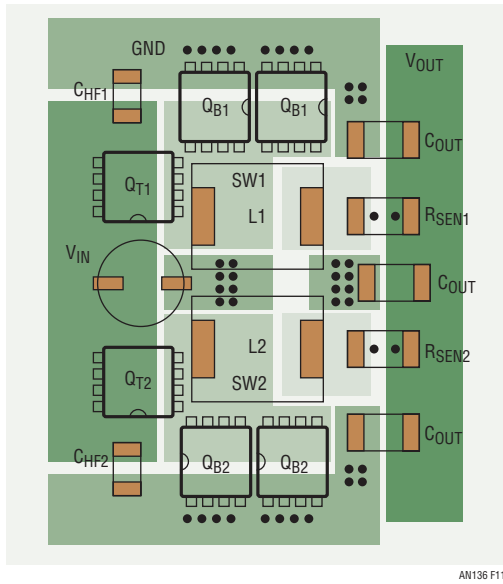


Figure 11. Example of Power Stage Layout of Dual-Phase, Single- V_{OUT} Buck Converter

CONTROL CIRCUITRY LAYOUT

Location of the Control Circuitry

The control circuitry should be located away from the noisy switching copper areas. It is preferable to have the control circuitry located close to the V_{OUT}^+ side for the buck converter and close to the V_{IN}^+ side for the boost converter, where the power traces carry continuous current. If space allows, locate the control IC a small distance (0.5–1") from the power MOSFETs and inductors, which are noisy and hot. However, if the space constraint forces the controller to be located close to power MOSFETs and inductors, special care must be taken to isolate the control circuitry from power components with ground planes or traces.

Separation of the Signal Ground and Power Ground

The control circuitry should have a separate signal (analog) ground island from the power stage ground. If there are separate signal ground (SGND) and power ground (PGND) pins on the controller IC, they should be routed separately. For controller ICs that have integrated MOSFET drivers, the small signal section of the IC pins should use the

SGND, as shown in Figure 12. Only one connection point between the SGND and PGND is required. It is desirable to return the SGND to a clean point of the PGND plane. The two grounds can be done by connecting both ground traces just under the controller IC. Figure 12 shows the preferred ground separation of the LTC3855 supply. In this example, the IC has an exposed GND pad. It should be soldered down to PCB to minimize electrical and thermal impedance. Multiple vias should be placed on this GND pad area.

Decoupling Capacitors for the Controller IC

The decoupling capacitors for the controller IC should be physically close to their pins. To minimize connection impedance, it is preferable to connect the decoupling capacitors directly to the pins without using vias. As shown in Figure 12, the following LTC3855 pins should have their decoupling capacitors closely located: current sensing pins, SENSE⁺/SENSE⁻, compensation pin, I_{TH} , signal ground pin, SGND, feedback voltage divider pin, FB, IC V_{CC} voltage pin, INTV_{CC}, and power ground pin, PGND.

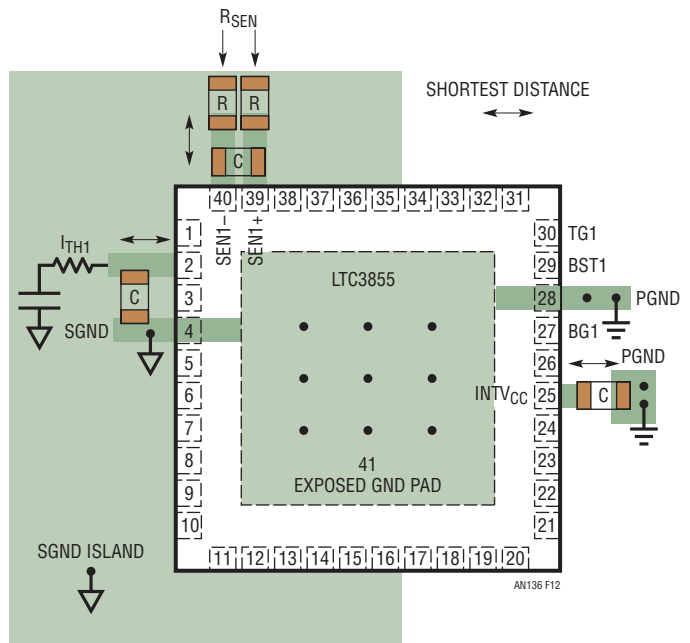


Figure 12. Decoupling Capacitors of Controller IC and Ground Separation

Minimize Loop Area and Crosstalk

Separate Noisy Traces and Sensitive Traces

Two or more adjacent conductors can be coupled capacitively. High dv/dt voltage change on one conductor will couple currents to another through the parasitic capacitor. To reduce the noise coupling from the power stage to the control circuitry, it is necessary to keep the noisy switching traces far from the sensitive small signal traces. If possible, route the noisy traces and sensitive traces on different layers, with an internal ground layer for noise shielding. As to the LTC3855 controller, the following pins have high dv/dt switching voltages: FET driver TG, BG, SW and BOOST. The following pins are connected to the most sensitive small signal nodes: SENSE⁺/SENSE⁻, FB, I_{TH} and SGND. If these sensitive signal traces are routed close to high dv/dt nodes, the ground traces or a ground layer must be inserted between these signal traces and high dv/dt traces to shield the noise.

Gate Driver Traces

It is desirable to use short and wide traces to route gate drive signals in order to minimize the impedance in gate drive paths. As shown in Figure 13, the top FET driver traces TG and SW should be routed together with minimum loop area to minimize the inductance and high dv/dt noise. Similarly, the bottom FET driver trace BG should be routed close to a PGND trace. If a PGND layer is placed under the BG trace, the AC ground return current of the bottom FET will be automatically coupled in a path close to the BG trace. AC current flows where it finds the minimum loop/impedance. In this case, a separate PGND return trace for the bottom gate driver is not required. It is best to minimize the number of layers that the gate driver traces are routed on. This prevents gate noise from propagating to other layers.

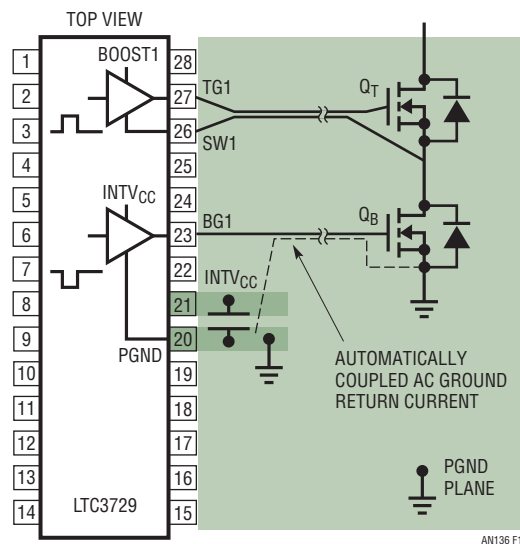


Figure 13. Gate Driver Trace Routing of the MOSFETs

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Current Sensing Trace and Voltage Sensing Trace

Of all the small signal traces, current sensing traces are most sensitive to noise. The current sensing signal amplitude is usually less than 100mV, which is comparable to the noise amplitude. In the LTC3855 example, its SENSE⁺/SENSE⁻ traces should be routed in parallel with minimum spacing (Kelvin sense) to minimize the chance of picking up di/dt-related noise, as shown in Figure 14. In addition, the filter resistors and capacitor for current sensing traces should be placed as close to the IC pins as possible. This provides the most effective filtering in case noise is injected into the long sense lines. If inductor DCR current sensing is used with an R/C network, the DCR sensing resistor, R, should be close to the inductor, while the DCR sensing capacitor, C, should be close to the IC. If via is used in the return path of the trace to SENSE⁻, this via should not contact another internal V_{OUT}⁺ layer. Otherwise, this via may conduct large V_{OUT}⁺ current and the resulting voltage

drop may distort the current sensing signal. Avoid routing the current sensing traces near the noisy switching nodes (TG, BG, SW, BOOST traces). If possible, place the ground layer between the current sensing traces and the layer with power stage traces.

If the controller IC has differential voltage remote sensing pins, use separated traces for the positive and negative remote sensing traces with Kelvin sense connection as well.

Trace Width Selection

Current level and noise sensitivity are unique to specific controller pins. Therefore, specific trace widths need to be selected for different signals. In general, the small signal nets can be narrow and routed with 10 to 15 mil wide traces. The high current nets (gate driving, V_{CC} and PGND) should be routed with short and wide traces. At least 20 mil width is recommended for these nets.

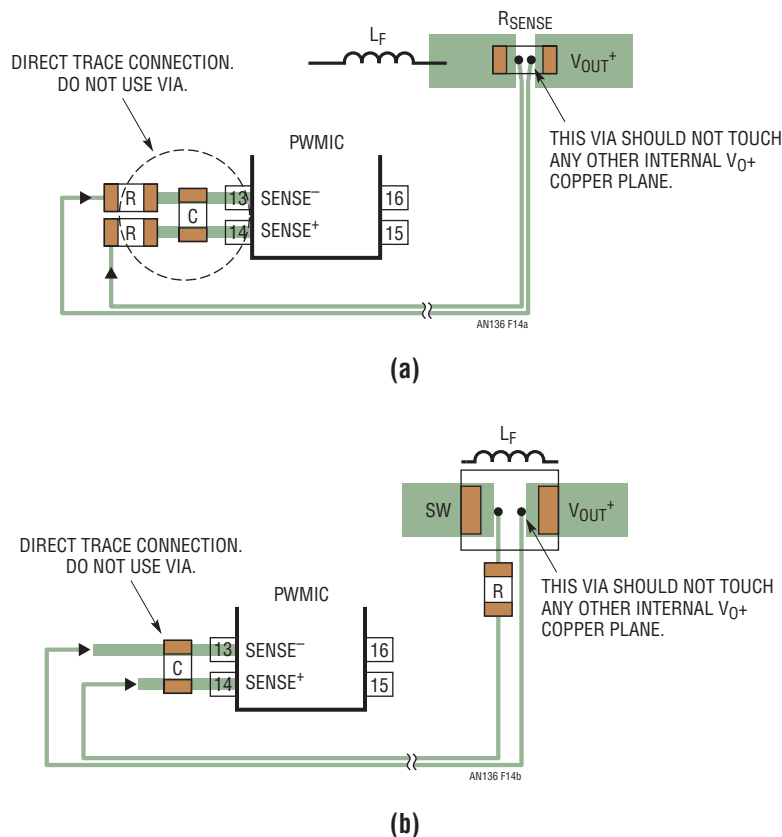


Figure 14. Kelvin Sensing for Current Sensing
(a) R_{SENSE}, and (b) Inductor DCR Sensing

SUMMARY

Power Design Layout Checklist

To summarize the layout design discussion in this article, Table 1 provides a sample checklist of the dual phase LTC3855 supply shown in Figure 10. Using such a checklist

will aid the designer to ensure that the result is a well laid out power supply design.

Table 1. Sample Layout Checklist for the LTC3855 Current Mode Buck Supply

	ITEM/COMMENTS	YES/NO
1. Plan of the Layout		
1.0	Understand the system mechanical and thermal constraints. Save sufficient board real estate/area for power supply in the beginning/planning stage of the big system. Don't wait to do it as the last step.	
1.1	Power supply output capacitors are located physically close to the supply load. – To minimize impedance between the output capacitors and the fast transient load.	
1.2	Locate power supply near cooling fan; ensure good air flow path. – For optimal cooling of the power supply.	
1.3	Ground layer is placed between the power layer and the small signal layer (Figure 1). – To return the current from the power component layer and to shield sensitive small signal traces from power stage switching noise.	
1.4	Highlight the schematic traces to identify high current traces, noisy traces and sensitive small signal traces.	
1.5	Decide the components on top and bottom sides of the PCB board. Try to keep all power components on the same side.	
2. Power Stage Layout		
2.1	Place the power components first. Please them in the way that minimizes the length of the high current flow paths through input capacitors, power FETs, inductors, R_{SENSE} and output capacitors. – To minimize the PCB impedance and conduction losses on high current paths.	
2.2	Have solid, low impedance land patterns for the power components, including capacitors, FETs, diodes, inductors and current sensing resistors. Use large copper plane for V_{IN} , V_{OUT} and GND (Figure 8). – To minimize the trace impedance and power component thermal stress.	
2.3	Use thick copper or multiple layers for high current power layers. – To minimize the PCB conduction loss and reduce thermal stress.	
2.4	If it is necessary to route a power trace to another layer, choose a trace in low di/dt paths and use multiple vias for interconnection. – To minimize noise propagation and connection impedance between layers.	
2.5	Minimize the pulsating current loop area that includes the top FET Q_T , bottom FET Q_B and ceramic input filter capacitor C_{HF} (Figure 3). – To minimize the pulsating loop (hot loop) inductance and absorb switching noise.	
2.6	Minimize and isolate/shield the high dv/dt SW node areas. – To minimize the EMI noise source from the high dv/dt SW nodes.	
2.7	Separate input current paths among supplies if there is more than one supply on the same input rail (Figure 9) and the supplies are not synchronized. Have local input decoupling capacitor for each supply. – To avoid common impedance noise coupling among supplies.	
2.8	PolyPhase converter. Try to have symmetric layout for each phase. Have local ceramic decoupling capacitor for each phase.	

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Table 1. Sample Layout Checklist for the LTC3855 Current Mode Buck Supply

	ITEM/COMMENTS	YES/NO
3. Control Circuit Layout		
3.1	Locate the control circuitry in a quiet location that is close to output capacitors or input capacitors. – To minimize the noise to the control circuitry.	
3.2	Use a separate SGND ground island for the components to the following small signal pins: I _{TH} , SGND, SENSE ⁺ /SENSE ⁻ , FB, V _{DIFFOUT} , FREQ, MODE/PLLIN, RUN, TK/SS, I _{LIM} , PHASMD and PGOOD (Figure 12). Ground connections are short and go directly to the SGND island. – To minimize the noise to the control circuitry.	
3.3	Use PGND the INTV _{CC} capacitors (Figure 12).	
3.4	Has a single connection point between SGND and PGND. One suggested location is underneath the IC (Figure 12). If the IC has an exposed ground thermal pad, connect this pad to PCB and have multiple vias to other SGND/PGND layers. – To minimize SGND noise and provide low impedance gate driver current return path.	
3.5	The following pins should have their ceramic decoupling capacitor located close by on the same controller layer and directly connected: SENSE ⁺ /SENSE ⁻ , I _{TH} , SGND, FB, INTV _{CC} and PGND (Figure 12). – To minimize the connection impedance and provide best noise decoupling with HF capacitors.	
3.6	Current sensing traces – Kelvin sensing is required with closely routed SENSE ⁺ /SENSE ⁻ traces (Figure 14). SENSE ⁻ via should not touch internal V _{OUT} ⁺ plane. SENSE ⁺ /SENSE ⁻ traces should be separated from the following nets: TG, SW, BOOST and BG. Have direct trace connections between SENSE ⁺ /SENSE ⁻ pins and their filtering capacitors. Filtering C must be close to SENSE ⁺ /SENSE ⁻ pins. – To minimize the noise pickup by SENSE ⁺ /SENSE ⁻ current sensing loop. SENSE ⁺ /SENSE ⁻ traces are the most sensitive small signal (< 75mV) traces.	
3.7	Remote voltage sensing traces – V _{OS} ⁺ /V _{OS} ⁻ traces should be routed together with a pair of traces. – To minimize the noise and sensing error.	
3.8	Gate driver traces – TG and SW traces should be routed together with minimum loop area (Figure 13). Try to route TG, SW and BG traces on one layer only. – To minimize the noise source from the high dv/dt gate driver traces.	
3.9	Maintain distance between sensitive small signal traces and noisy traces/planes. Most sensitive traces include SENSE ⁺ /SENSE ⁻ , FB, I _{TH} and SGND. Noisy traces/planes include SW, TG, BOOST and BG. If possible, place the ground trace/layer between the noisy trace/layer and the small signal trace/layer. – To minimize the capacitive noise coupling between noisy traces and small signal traces.	
3.10	Trace width – The following controller traces should be at least 20 mil wide: INTV _{CC} , PGND, TG, BG, SW and BOOST. – To minimize the trace impedance.	