Applications for a Switched-Capacitor Instrumentation Building Block

Jim Williams

CMOS analog IC design is largely based on manipulation of charge. Switches and capacitors are the elements used to control and distribute the charge. Monolithic filters, data converters and voltage converters rely on the excellent characteristics of IC CMOS switches. Because of the importance of switches in their circuits, CMOS designers have developed techniques to minimize switch induced errors, particularly those associated with stray capacitance and switch timing. Until now, these techniques have been used only in the internal construction of monolithic devices. A new device, the LTC®1043, makes these switches available for board-level use. Multi-pole switching and a self-driven, non-overlapping clock allow the device to be used in circuits which are impractical with other switches.

Conceptually, the LTC1043 is simple. Figure 1 details its features. The oscillator, free-running at 200kHz, drives a non-overlapping clock. Placing a capacitor from Pin 16 to ground shifts the oscillator frequency downward to any desired point. The pin may also be driven from an external source, synchronizing the switches to external circuitry. A non-overlapping clock controls both DPDT switch sections. The non-overlapping drive prevents simultaneous conduction in the series connected switch sections.

Charge balancing circuitry cancels the effects of stray capacitance. Pins 1 and 10 may be used as guard points for Pins 3 and 12 in particularly sensitive applications.

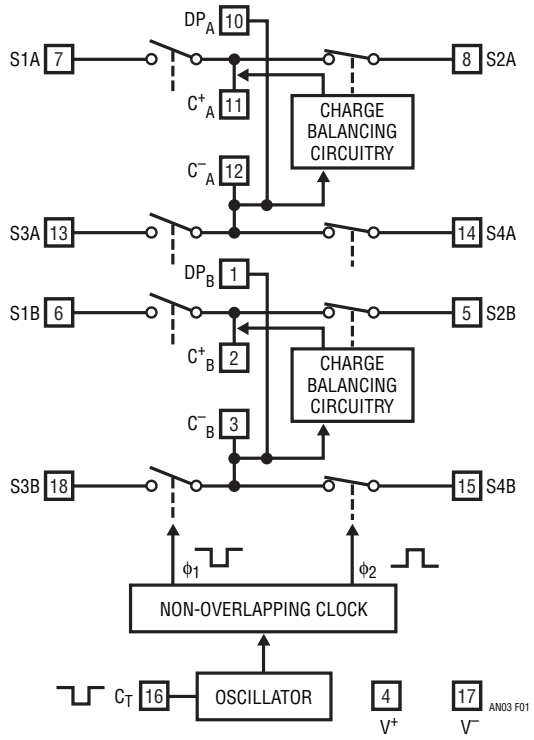


Figure 1. Block Diagram of LTC1043 Showing Individual Switches

Although the device's operation is simple, it permits surprisingly sophisticated circuit functions. Additionally, the careful attention paid to switching characteristics makes implementing such functions relatively easy. Discrete timing and charge-balance compensation networks are eliminated, reducing component count and trimming requirements.

Classical analog circuits work by utilizing continuous functions. Their operation is usually described in terms of voltage and current. Switched-capacitor based circuits are sampled data systems which approximate continuous functions with bandwidth limited by the sampling frequency. Their operation is described in the distribution of charge over time. To best understand the circuits which follow, this distinction should be kept in mind. Analog sampled data and carrier-based systems are less common than true continuous approaches, and developing a working familiarity with them requires some thought.

Switched-capacitor approaches have greatly aided analog MOS IC design. The LTC1043 brings many of the freedoms and advantages of CMOS IC switched-capacitor circuits to the board level, providing a valuable addition to available design techniques.

Instrumentation Amplifier

Figure 2 uses the LTC1043 to build a simple, precise instrumentation amplifier. An LTC1043 and an LT®1013 dual op amp are used, allowing a dual instrumentation amplifier using just two packages. A single DPDT section converts the differential input to a ground referred single-ended signal at the LT1013's input. With the input switches closed, C1 acquires the input signal. When the input switches open, C2's switches close and C2 receives charge. Continuous clocking forces C2's voltage to equal the difference between the circuit's inputs. The 0.01µF capacitor at Pin 16 sets the switching frequency at 500Hz. Common mode voltages are rejected by over 120dB and drift is low.

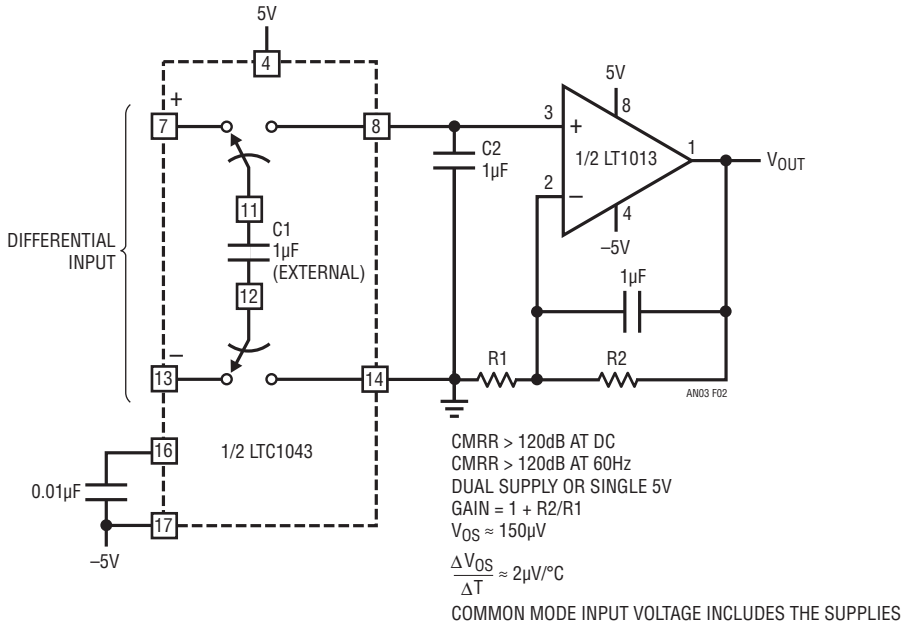


Figure 2. ±5V Precision Instrumentation Amplifier

Amplifier gain is set in the conventional manner. This circuit is a simple, economical way to build a high performance instrumentation amplifier. Its DC characteristics rival any IC or hybrid unit and it can operate from a single 5V supply. The common mode range includes the supply rails, allowing the circuit to read across shunts in the supply lines. The performance of the instrumentation amplifier depends on the output amplifier used. Specifications for an LT1013 appear in the figure. Lower figures for offset, drift and bias current are achievable by employing type LT1001, LT1012, LT1056 or the chopper-stabilized LTC1052.

Ultrahigh Performance Instrumentation Amplifier

Figure 3 is similar to Figure 2, but utilizes the remaining LTC1043 section to construct a low drift chopper amplifier. This approach maintains the true differential inputs while achieving 0.1µV/°C drift. The differential input is converted to a single-ended potential at Pin 7 of the LTC1043. This voltage is chopped into a 500Hz square wave by the switching action of Pins 7, 11 and 8. A1, AC-coupled, amplifies this signal. A1's square wave output, also AC-coupled, is synchronously demodulated by switches 12, 14 and 13. Because this switch section is synchronously driven with the input chopper, proper amplitude and polarity information is presented to A2, the DC output amplifier. This stage integrates the square wave into a DC voltage to provide the output. The output is divided down and fed back to Pin 8 of the input chopper where it serves as the zero signal reference. Because the main amplifier is AC-coupled, its DC terms do not affect overall circuit offset, resulting in the extremely low offset and drift noted in the specifications. This circuit offers lower offset and drift than any commercially available instrumentation amplifier.

Lock-In Amplifier

The AC carrier approach used in Figure 3 may be extended to form a "lock-in" amplifier. A lock-in amplifier works by synchronously detecting the carrier modulated output of the signal source. Because the desired signal information is contained within the carrier, the system constitutes an extremely narrow-band amplifier. Non-carrier related components are rejected and the amplifier passes only signals which are coherent with the carrier. In practice, lock-in amplifiers can extract a signal 120dB below the noise level.

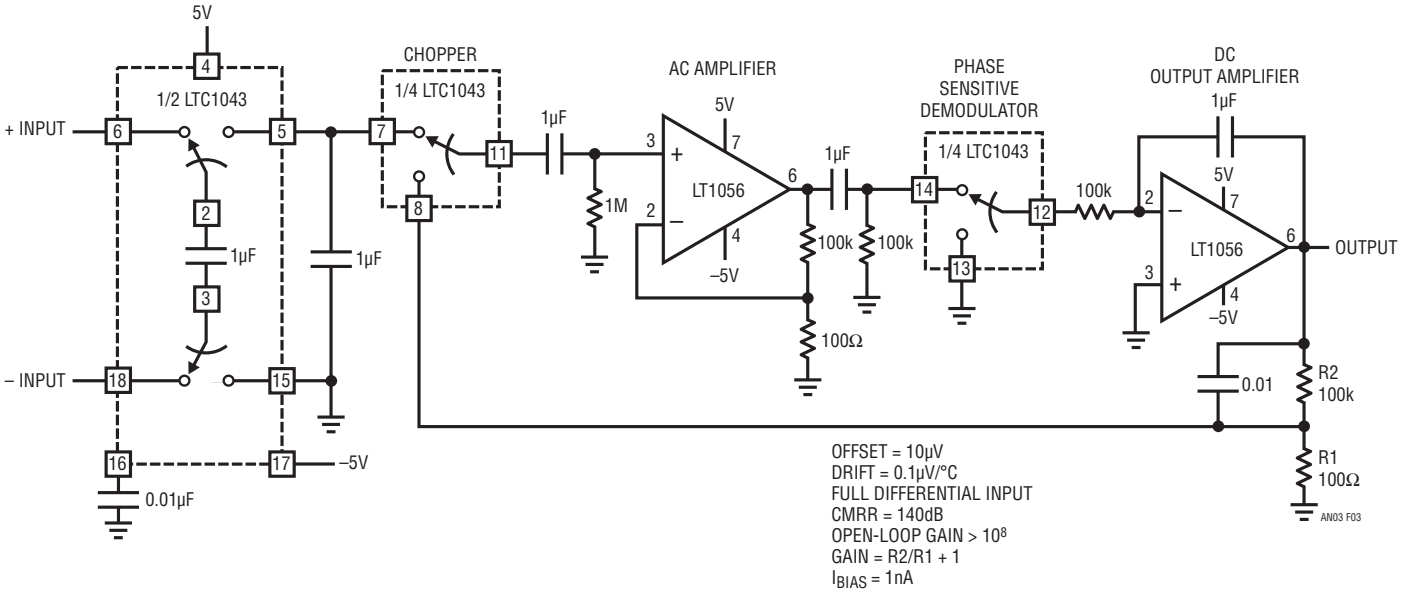


Figure 3. Chopper-Stabilized Instrumentation Amplifier

Figure 4 shows a lock-in amplifier which uses a single LTC1043 section. In this application, the signal source is a thermistor bridge which detects extremely small temperature shifts in a biochemical microcalorimetry reaction chamber.

The 500Hz carrier is applied at T1's input (Trace A, Figure 5). T1's floating output drives the thermistor bridge, which presents a single-ended output to A1. A1 operates at an AC gain of 1000. A 60Hz broadband noise source is also deliberately injected into A1's input (Trace B). The carrier's zero crossings are detected by C1. C1's output clocks the LTC1043 (Trace C). A1's output (Trace D) shows the desired 500Hz signal buried within the 60Hz noise source. The LTC1043's zero-cross-synchronized switching at A2's positive input (Trace E) causes A2's gain to alternate between plus and minus one. As a result, A1's output is synchronously demodulated by A2. A2's output (Trace F) consists of demodulated carrier signal and non-coherent components. The desired carrier amplitude and polarity information is discernible in A2's output and is extracted by filter averaging at A3. To trim this circuit, adjust the phase potentiometer so that C1 switches when the carrier crosses through zero.

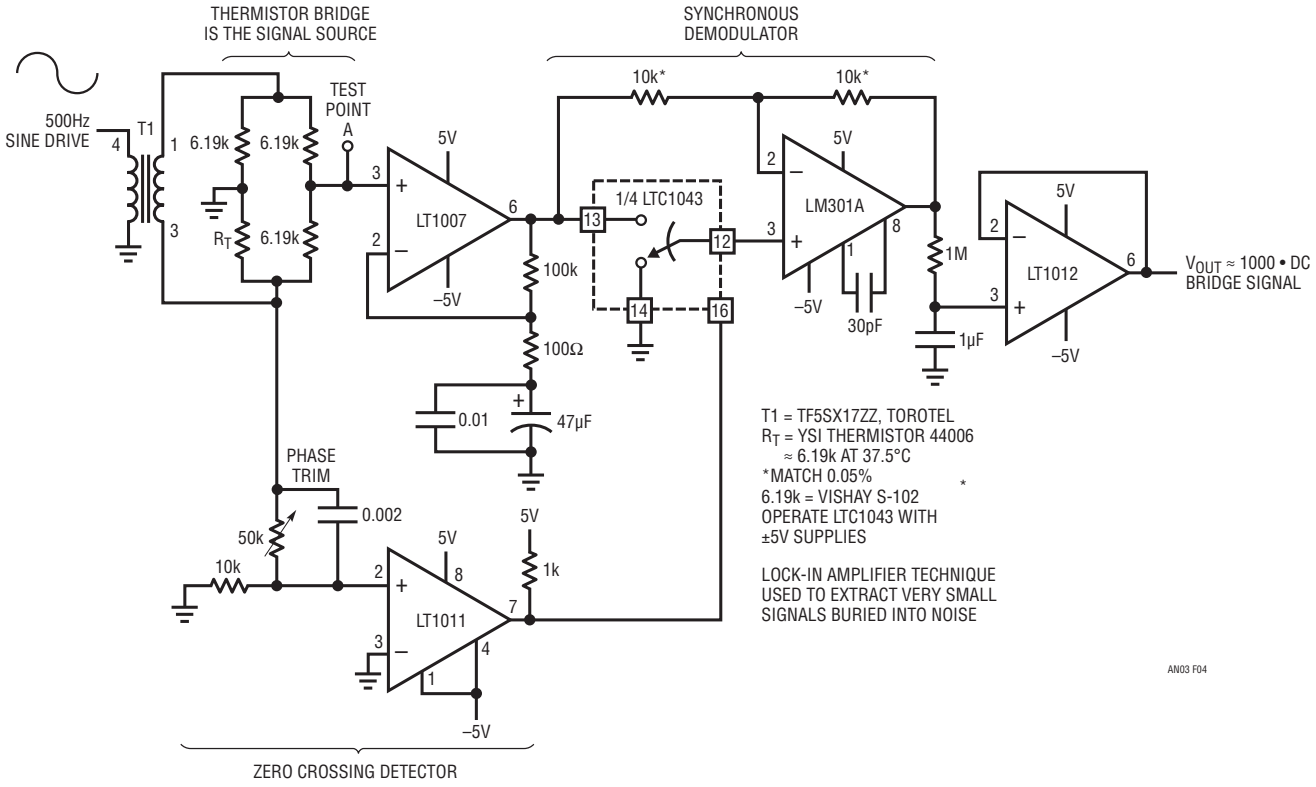


Figure 4. Lock-In Amplifer

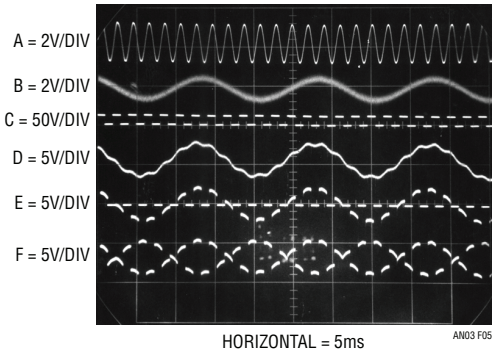


Figure 5

Wide Range, Digitally Controlled, Variable Gain Amplifier

Aside from low drift and noise rejection, another dimension in amplifier design is variable gain. Designing a wide range, digitally variable gain block with good DC stability is a difficult task. Such configurations usually involve relays or temperature compensated FET networks in expensive and complex arrangements. The circuit shown in Figure 6 uses the LTC1043 in a variable gain amplifier which features continuously variable gain from 0 to 1000, gain stability of 20ppm/°C and single-ended or differential input. The circuit uses two separate LTC1043s. Unit A is clocked by a frequency input which could be derived from a host processor. LTC1043B is continuously clocked by a 1kHz source which could also be processor supplied. Both LTC1043s function as the sampled data equivalent of a resistor within the bandwidth set by A1's 0.01µF value and the switched-capacitor equivalent feedback resistor. The time-averaged current delivered to the summing point by LTC1043A is a function of the 0.01µF capacitor's input-derived voltage and the commutation frequency at Pin 16. Low commutation frequencies result in small time-averaged current values, approximating a large input resistor. Higher frequencies produce an equivalent small input resistor. LTC1043B, in A1's feedback path, acts in a similar fashion. For the circuit values given, the gain is simply:

$$G = \frac{f_{IN}}{10} \bullet \frac{0.01\mu F}{100pF}$$

Gain stability depends on the ratiometric stability between the 1kHz and variable clocks (which could be derived from a common source) and the ratio stability of the capacitors. For polystyrene types, this will typically be 20ppm/°C. The circuit input, determined by the pin connections shown in the figure, may be either single-ended or fully differential. Additionally, although A1 is connected as an inverter, the circuit's overall transfer function may be either positive or negative. As shown, with Pins 13A and 7A grounded and the input applied to 8A, it is negative.

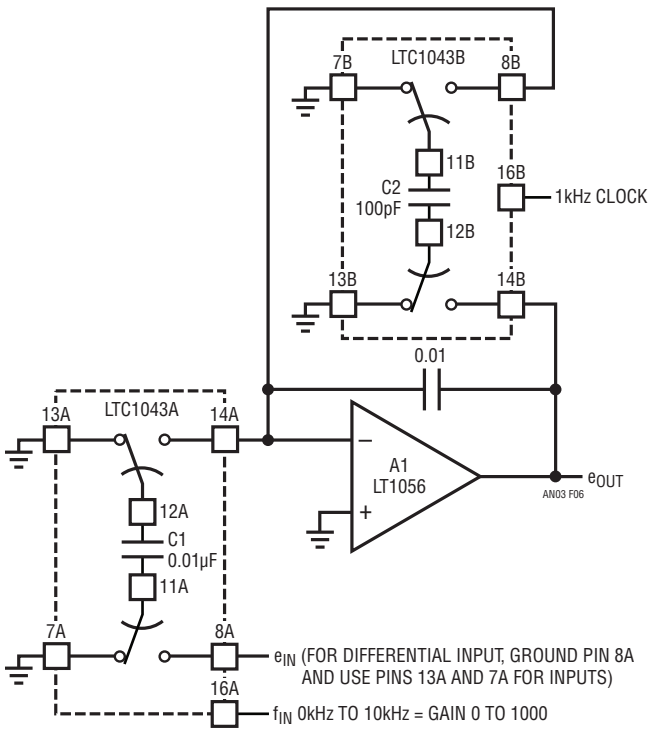


Figure 6. Variable-Gain Amplifier

Precision, Linearized Platinum RTD Signal Conditioner

Figure 7 shows a circuit which provides complete, linearized signal conditioning for a platinum RTD. One side of the RTD sensor is grounded, often desirable for noise considerations. This LTC1043 based circuit is considerably simpler than instrumentation or multi-amplifier based designs and will operate from a single 5V supply. A1 serves as a voltage-controlled ground referred current source by differentially sensing the voltage across the 887Ω feedback resistor. The LTC1043 section which does this presents a single-ended signal to A1's negative input, closing a loop. The 2k-0.1µF combination sets amplifier roll-off well below the LTC1043's switching frequency and the configuration is stable. Because A1's loop forces a fixed voltage across the 887Ω resistor, the current through R_P is constant. A1's operating point is primarily fixed by the 2.5V LT1009 voltage reference.

The RTD's constant current forces the voltage across it to vary with its resistance, which has a nearly linear positive temperature coefficient. The nonlinearity could cause several degrees of error over the circuit's 0°C to 400°C operating range. A2 amplifies R_P's output, while simultaneously supplying nonlinearity correction. The correction is implemented by feeding a portion of A2's output back to A1's input via the 10k to 250k divider. This causes the current supplied to R_P to slightly shift with its operating point, compensating sensor nonlinearity to within ±0.05°C. The remaining LTC1043 section furnishes A2 with a differential input. This allows an offsetting potential, derived from the LT1009 reference, to be subtracted from R_P's output. Scaling is arranged so 0°C equals 0V at A2's output. Circuit gain is set by A2's feedback values and linearity correction is derived from the output.

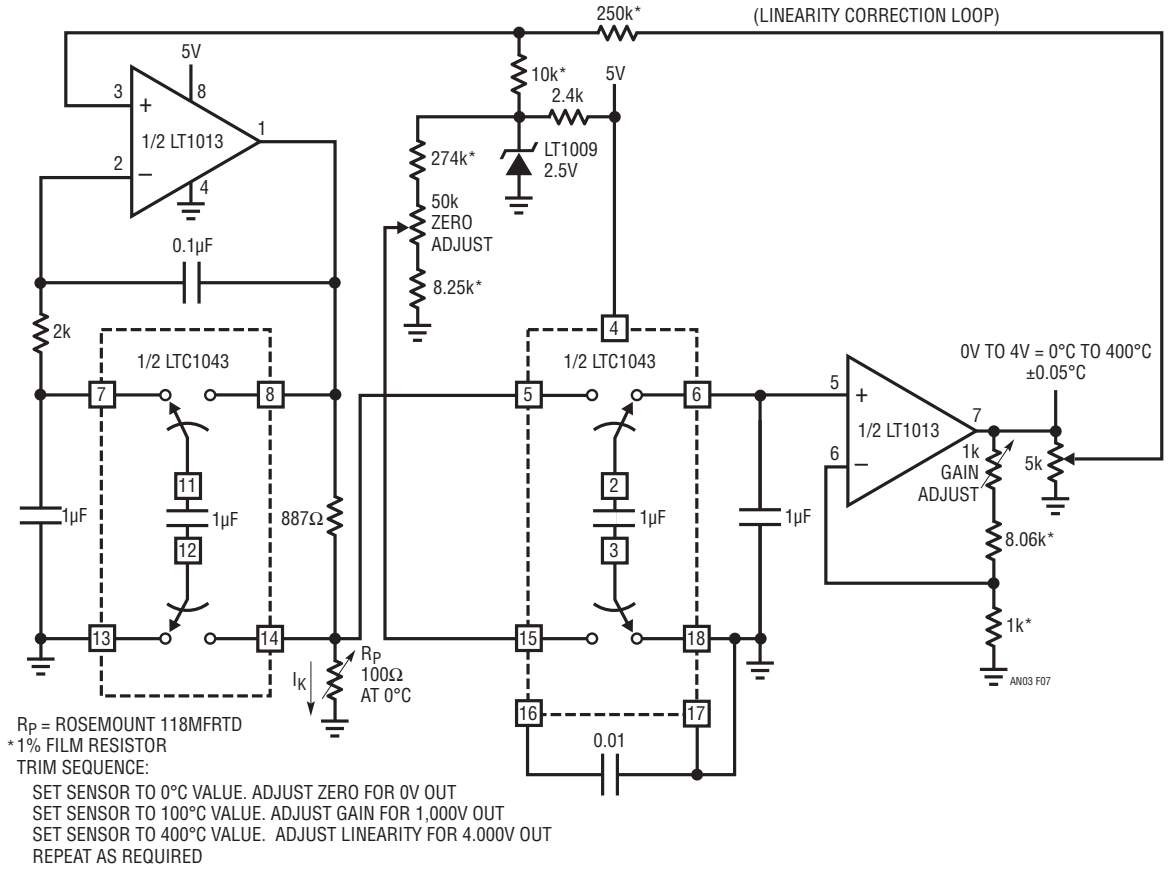


Figure 7. Linearized Platinum Signal Conditioner

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432k) for R_P. Set the box to the 0°C value (100.00Ω) and adjust the offset trim for a 0.00V output. Next, set the decade box for a 140°C output (154.26Ω) and adjust the gain trim for a 1.400V output reading. Finally, set the box to 249.0°C (400.00°C) and trim the linearity adjustment for a 4.000V output. Repeat this sequence until all three points are fixed. Total error over the entire range will be within ±0.05°C. The resistance values given are for a nominal 100.00Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 100.00Ω. This deviation, which is manufacturer specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and is a very small error term.

Note that A1 constitutes a voltage controlled current source with input and output referred to ground. This is a difficult function to achieve and is worthy of separate mention.

Relative Humidity Sensor Signal Conditioner

Relative humidity is a difficult physical parameter to transduce, and most transducers available require fairly complex signal conditioning circuity. Figure 8 combines two LTC1043s with a recently introduced capacitively based humidity transducer in a simple charge pump based circuit.

The sensor specified has a nominal 500pF capacitance at RH = 76%, with a slope of 1.7pF/% RH. The average voltage across this device must be zero. This provision prevents deleterious electrochemical migration in the sensor. LTC1043A inverts a resistively scaled portion of the LT1009 reference, generating a negative potential at Pin 14A. LTC1043B alternately charges and discharges the humidity sensor via Pins 12B, 13B and 14B. With 14B and 12B connected, the sensor charges via the 1µF unit to the negative potential at Pin 14A. When the 14B-12B pair opens, 12B is connected to A1's summing point via 13B. The sensor now discharges into the summing point through the 1µF capacitor. Since the charge voltage is fixed,

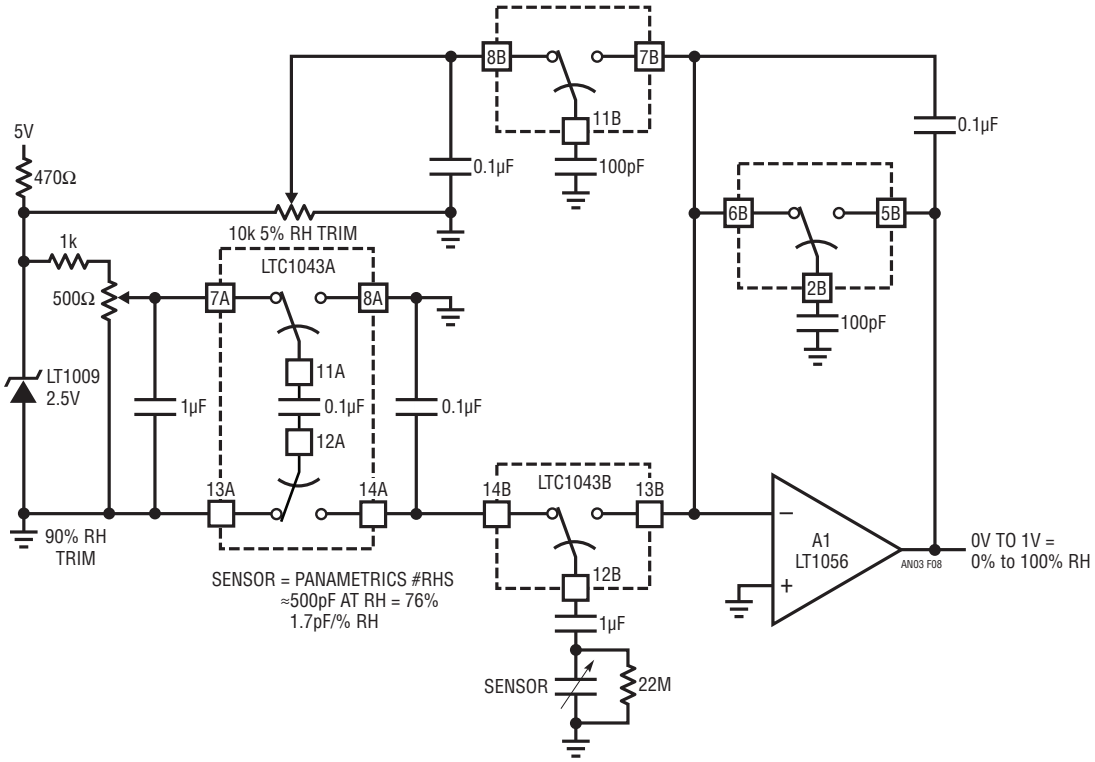


Figure 8. Relative Humidity Signal Conditioner

the average current into the summing point is determined by the sensor's humidity related value. The 1µF value AC couples the sensor to the charge-discharge path, maintaining the required zero average voltage across the device. The 22M resistor prevents accumulation of charge, which would stop current flow. The average current into A1's summing point is balanced by packets of charge delivered by the switched-capacitor network in A1's feedback loop. The 0.1µF capacitor gives A1 an integrator-like response, and its output is DC.

To allow 0% RH to equal 0V, offsetting is required. The signal and feedback terms biasing the summing point are expressed in charge form. Because of this, the offset must also be delivered to the summing point as charge, instead of a simple DC current. If this is not done, the circuit will be affected by frequency drift of LTC1034B's oscillator. Section 8B-11B-7B serves this function, delivering LT1009-referenced offsetting charge to A1.

Drift terms in this circuit include the LT1009 and the ratio stability of the sensor and the 100pF capacitors. These terms are well within the sensor's 2% accuracy specification and temperature compensation is not required. To calibrate this circuit, place the sensor in a known 5% RH environment and adjust the "5% RH trim" for 0.05V output. Next, place the sensor in a 90% RH environment and set the "90% RH trim" for 900mV output. Repeat this procedure until both points are fixed. Once calibrated, this circuit is accurate within 2% in the 5% to 90% RH range.

Figure 9 shows an alternate circuit which requires two op amps but needs only one LTC1043 package. This circuit retains insensitivity to clock frequency while permitting a DC offset trim. This is accomplished by summing in the offset current after A1.

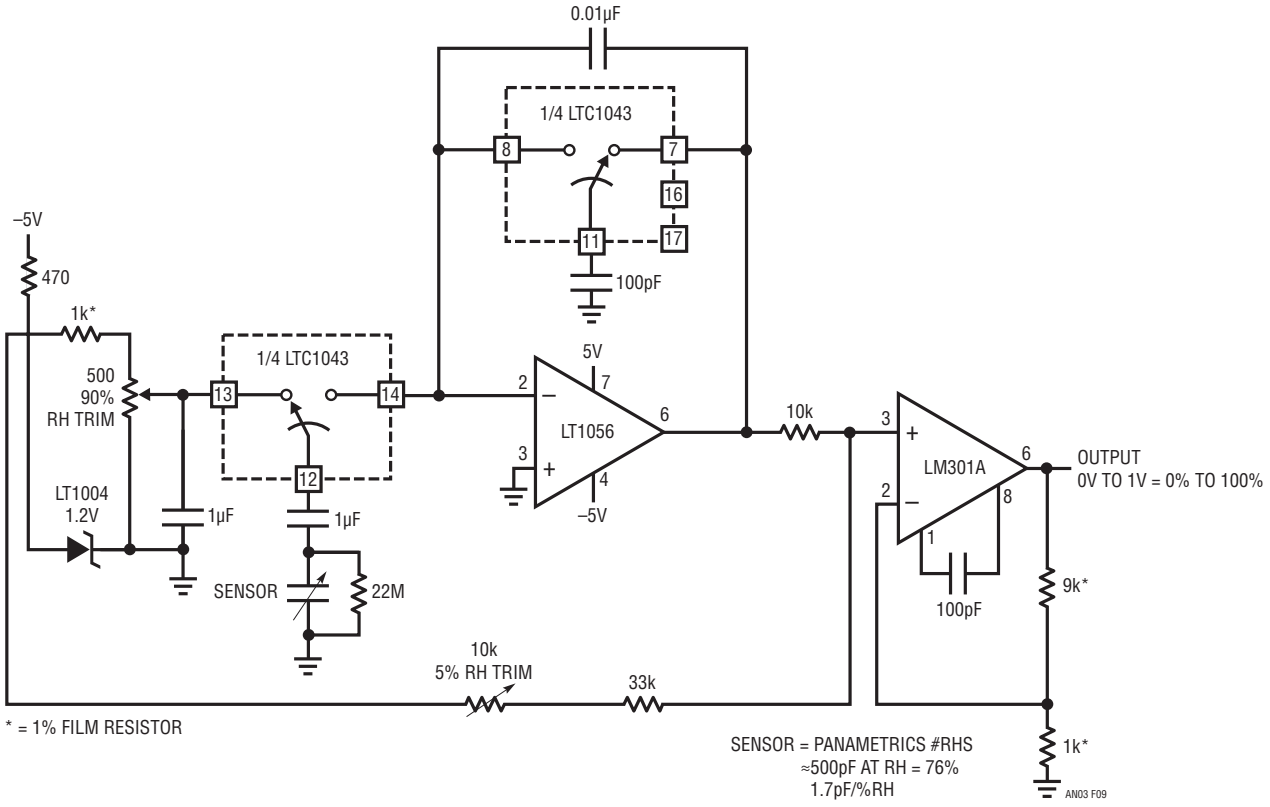


Figure 9. Relative Humidity Signal Conditioner

LVDT Signal Conditioner

LVDTs (linear variable differential transformers) are another example of a transducer which the LTC1043 can signal condition. An LVDT is a transformer with a mechanically actuated core. The primary is driven by a sine wave, usually amplitude stabilized. Sine drive eliminates error inducing harmonics in the transformer. The two secondaries are connected in opposed phase. When the core is positioned in the magnetic center of the transformer, the secondary outputs cancel and there is no output. Moving the core away from the center position unbalances the flux ratio between the secondaries, developing an output. Figure 10 shows an LTC1043 based LVDT signal conditioner. A1 and its associated components furnish the amplitude stable sine wave source. A1's positive feedback path is a Wein bridge, tuned for 1.5kHz. Q1, the LT1004 reference, and additional components in A1's negative loop unity-gain stabilize the amplifier. A1's output (Trace A, Figure 11), an amplitude stable sine wave, drives the LVDT. C1 detects zero crossings and feeds the LTC1043 clock pin (Trace B). A speed-up network at C1's input compensates LVDT phase shift, synchronizing the LTC1043's clock to the transformer's output zero crossings. The LTC1043 alternately connects each end of the transformer to ground,

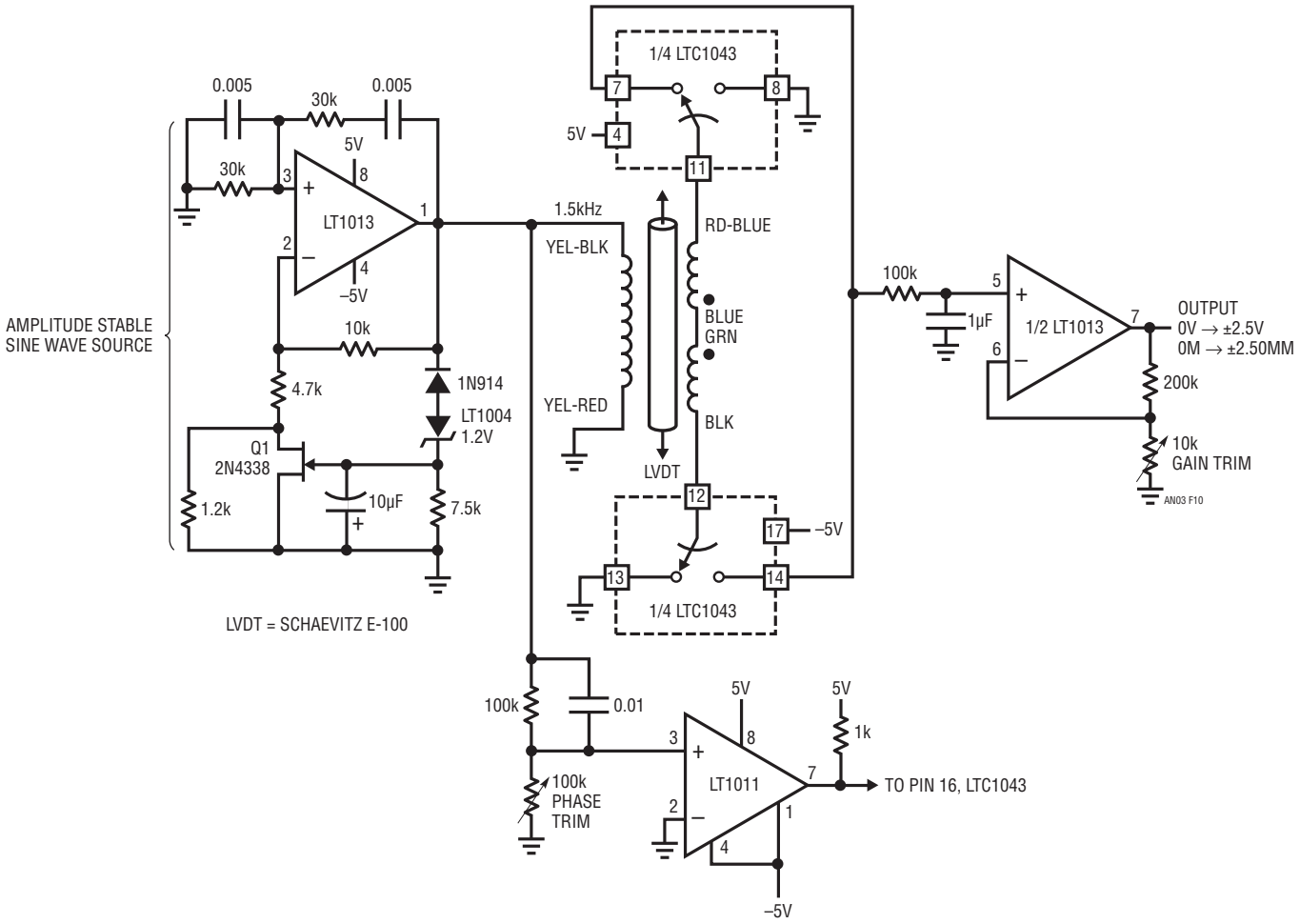


Figure 10. LVDT Signal Conditioner

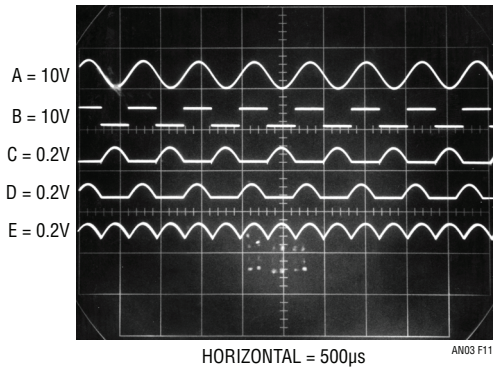


Figure 11

resulting in positive half-wave rectification at Pins 7 and 14 (Traces C and D, respectively). These points are summed (Trace E) at a lowpass filter which feeds A2. A2 furnishes gain scaling and the circuit's output.

The LTC1043's synchronized clocking means the information presented to the lowpass filter is amplitude and phase sensitive. The circuit output indicates how far the core is from center and on which side.

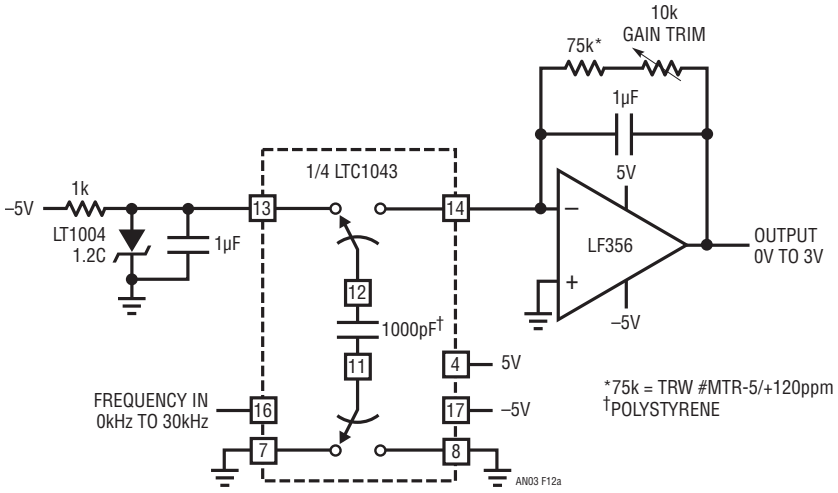
To calibrate this circuit, center the LVDT core in the transformer and adjust the phase trim for 0V output. Next, move the core to either extreme position and set the gain trim for 2.50V output.

Charge Pump F→V and V→F Converters

Figure 12 shows two related circuits, both of which show how the LTC1043 can simplify a precision circuit function. Charge pump F→V and V→F converters usually require substantial compensation for non-ideal charge gating behavior. These examples equal the performance of such circuits, while requiring no compensations. These circuits are economical, component count is low, and the 0.005% transfer linearity equals that of more complex designs. Figure 12A is an F→V converter. The LTC1043's clock pin is driven from the input (Trace A, Figure 13). With the input high, Pins 12 and 13 are shorted and 14 is open. The 1000pF capacitor receives charge from the 1µF unit, which is biased by the LT1004. At the input's negative-going edge, Pins 12 and 13 open and 12 and 14 close. The 1000pF capacitor quickly removes current (Trace B) from A1's summing node. Initially, current is transferred through A1's feedback capacitor and the amplifier output goes negative (Trace C). When A1 recovers, it slews positive to a level which resets the summing junction to zero. A1's 1µF feedback capacitor averages this action over many cycles and the circuit output is a DC level linearly related to frequency. A1's feedback resistors set the circuit's DC gain. To trim the circuit, apply 30kHz in and set the 10kΩ gain trim for exactly 3V output. The primary drift term in this circuit is the 120ppm/°C tempco of the 1000pF capacitor, which should be polystyrene. This can be reduced to within 20ppm/°C by using a feedback resistor with an opposing tempco (e.g., TRW #MTR-5/+120ppm). The input pulse width must be low for at least 100ns to allow complete discharge of the 1000pF capacitor.

In Figure 12B, the LTC1043 based charge pump is placed in A1's feedback loop, resulting in a V→F converter. The clock pin is driven from A1's output. Assume that A1's negative input is just below 0V. The amplifier output is positive. Under these conditions, LTC1043's Pins 12 and 13 are shorted and 14 is open, allowing the 0.01µF capacitor to charge toward the negative 1.2V LT1004. When the input-voltage-derived current forces A1's summing point (Trace A, Figure 13) positive, its output (Trace B) goes negative. This reverses the LT1043's switch states, connecting Pins 12 and 14. Current flows from the summing point into the 0.0µF capacitor (Trace C). The 30pF-22k combination at A1's positive input (Trace D) ensures A1 will remain low long enough for the 0.01µF capacitor to completely reset to zero. When the 30pF-22k positive feedback path decays, A1's output returns positive and the entire cycle repeats. The oscillation frequency of this action is directly related to the input voltage with a transfer linearity of 0.005%.

Start-up or overdrive conditions could force A1 to go to the negative rail and stay there. Q1 prevents this by pulling the summing point negative if A1's output stays low long enough to charge the 1µF-330k RC. Two LTC1043 switch sections provide complementary sink-source outputs. Similar to the F→V circuit, the 0.01µF capacitor is the primary drift term, and the resistor type noted above will provide optimum tempco cancellation. To calibrate this circuit, apply 3V and adjust the gain trim for a 30kHz output.



12a. Frequency-to-Voltage Converter

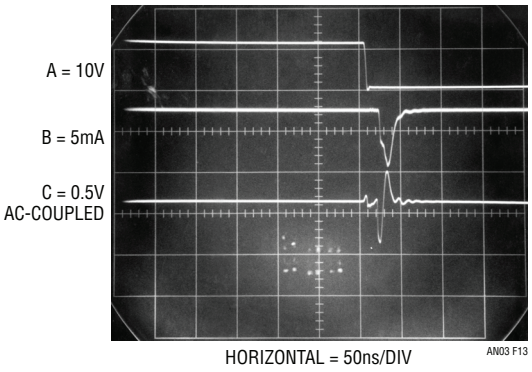
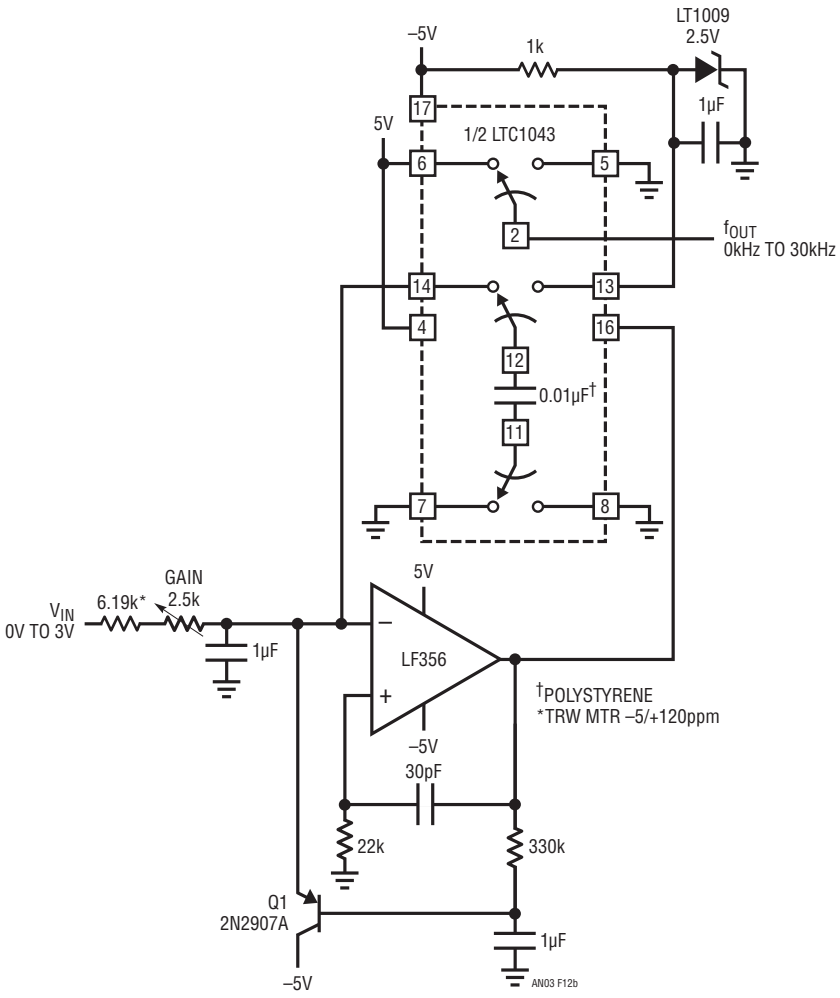


Figure 13



12b. Voltage-to-Frequency Converter

Figure 12

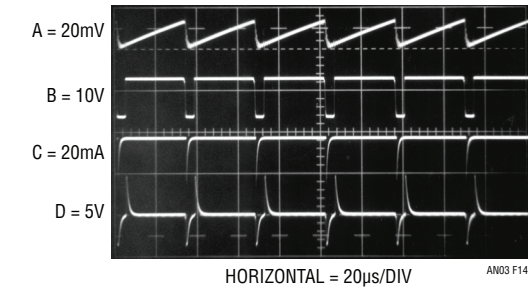


Figure 14

12-Bit A→D Converter

Figure 15 shows the LTC1043 used to implement an economical 12-bit A→D converter. The circuit is self-clocking, has a serial output, and completes a full-scale conversion in 25ms.

Two LTC1043s are used in this design. Unit A free-runs, alternately charging the 100pF capacitor from the LT1004 reference source and then dumping it into A1's summing point. A1, connected as an integrator, responds with a linear ramp output (Trace B, Figure 16). This ramp is compared to the input voltage by C1B. When the crossing occurs, C1B's output goes low (Trace C, just faintly visible in the photograph), setting the flip-flop high (Trace D). This pulls LTC1043's Pin 16 high, resetting A1's integrator capacitor via the paralleled switches. Simultaneously, Pin 14B opens,

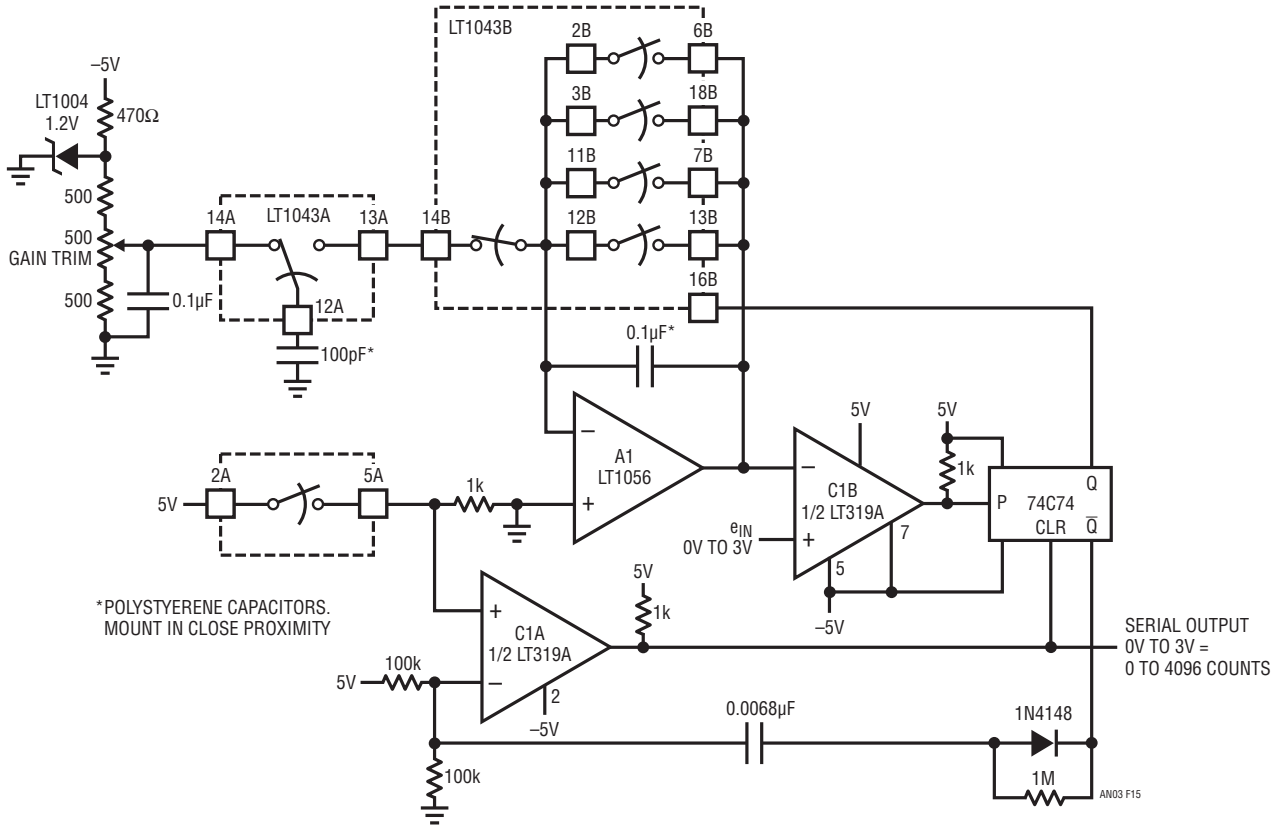
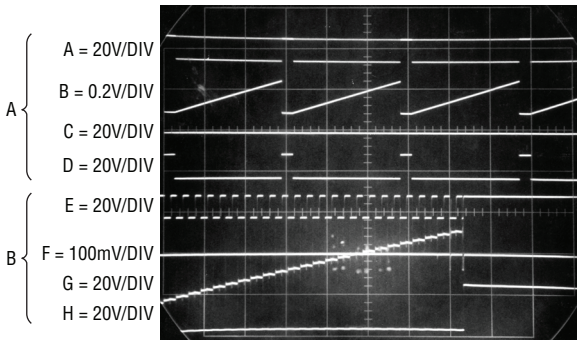


Figure 15. 12-Bit A→D Converter



A HORIZONTAL = 500µs/DIV
B HORIZONTAL = 20µs/DIV

Figure 16

preventing charge from being delivered to A1's summing point during the reset. The flip-flop's Q output, low during this interval, causes an AC negative-going spike at C1A. This forces C1A's output high, inserting a gap in the output clock pulse stream (Trace A). The width of this gap, set by the components at C1A's negative input, is sufficient to allow a complete reset of A1's integrating capacitor. The number of pulses between gaps is directly related to the input voltage. The actual conversion begins at the gap's negative edge and ends at its positive edge. The flip-flop output may be used for resetting. Alternately, a processor driven "time-out" routine can determine the end of conversion. Traces E through H offer expanded scale versions of Traces A through D, respectively. The staircase detail of A1's ramp output reflects the charge pumping action at its summing point. Note that drift in the 100pF and 0.1µF capacitors, which should be polystyrene, ratiometrically cancels. Full-scale drift for this circuit is typically 20ppm/°C, allowing it to hold 12-bit accuracy over 25°C + 10°C. To calibrate the circuit, apply 3V in and trim the gain potentiometer for 4096 pulses out between data stream gaps.

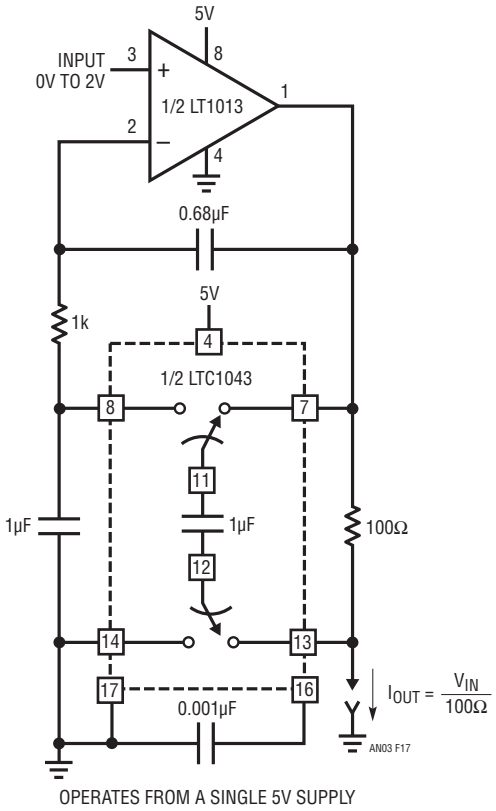


Figure 17. Voltage Controlled Current Source with Ground Referred Input and Output

Miscellaneous Circuits

Figures 17 to 22 show a group of miscellaneous circuits, most of which are derivations of applications covered in the text. As such, only brief comments are provided.

Voltage-Controlled Current Source—Grounded Source and Load

This is a simple, precise voltage-controlled current source. Bipolar supplies will permit bipolar output. Configurations featuring a grounded voltage control source and a grounded load are usually more complex and depend upon several components for stability. In this circuit, accuracy and stability are almost entirely dependent on the 100Ω shunt.

Current Sensing in Supply Rails

The LTC1043 can sense current through a shunt in either of its supply rails (Figure 18). This capability has wide application in battery and solar-powered systems. If the ground-referred voltage output is unloaded by an amplifier, the shunt can operate with very little voltage drop across it, minimizing losses.

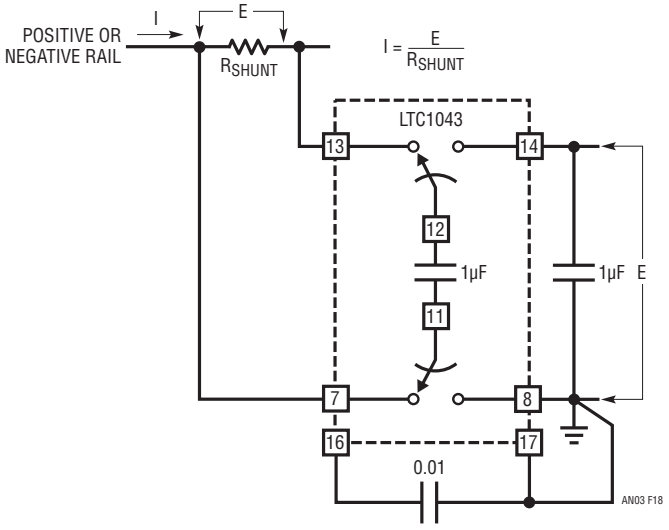


Figure 18. Precision Current Sensing in Supply Rails

0.01% Analog Multiplier

Figure 19, using the V→F and F→V circuits previously described, forms a high precision analog multiplier. The F→V input frequency is locked to the V→F output because the LTC1043's clock is common to both sections. The F→V reference is used as one input of the multiplier, while the V→F furnishes the other. To calibrate, short the X and Y inputs to 1.7320V and trim for a 3V output.

Inverting a Reference

Figure 20 allows a reference to be inverted with 1ppm accuracy. This circuit features high input impedance and requires no trimming.

Low Power, 5V Driven, Temperature Compensated Crystal Oscillator

Figure 21 uses the LTC1043 to differentiate between a temperature sensing network and a DC reference. The single-ended output biases a varactor-tuned crystal oscillator to compensate drift. The varactor-crystal network has high DC impedance, eliminating the need for an LTC1043 output amplifier.

Simple Thermometer

Figure 22's circuit is conceptually similar to the platinum RTD example of Figure 7. The thermistor network specified eliminates the requirement for a linearity trim, at the expense of accuracy and range of operation.

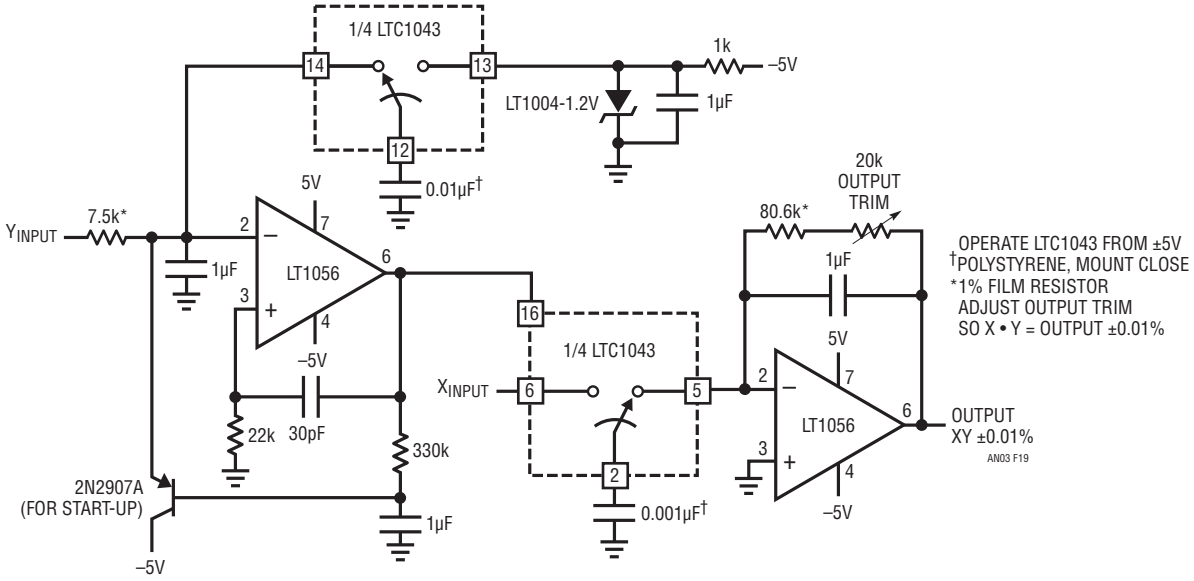


Figure 19. Analog Multiplier with 0.01% Accuracy

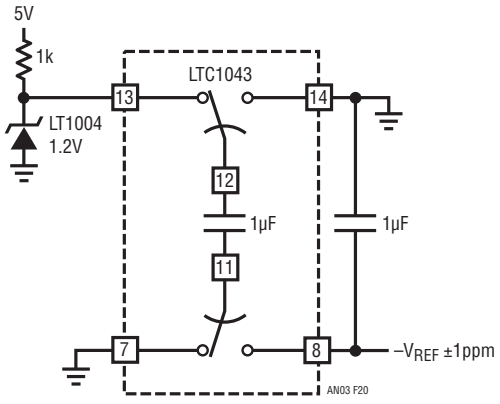


Figure 20. Precision Voltage Inverter

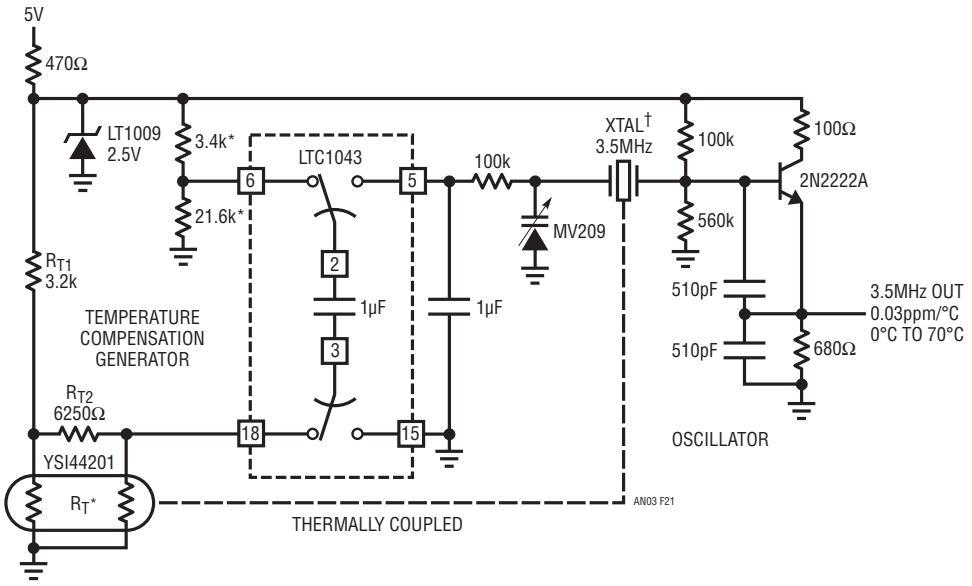


Figure 21. Temperature Compensated Crystal Oscillator

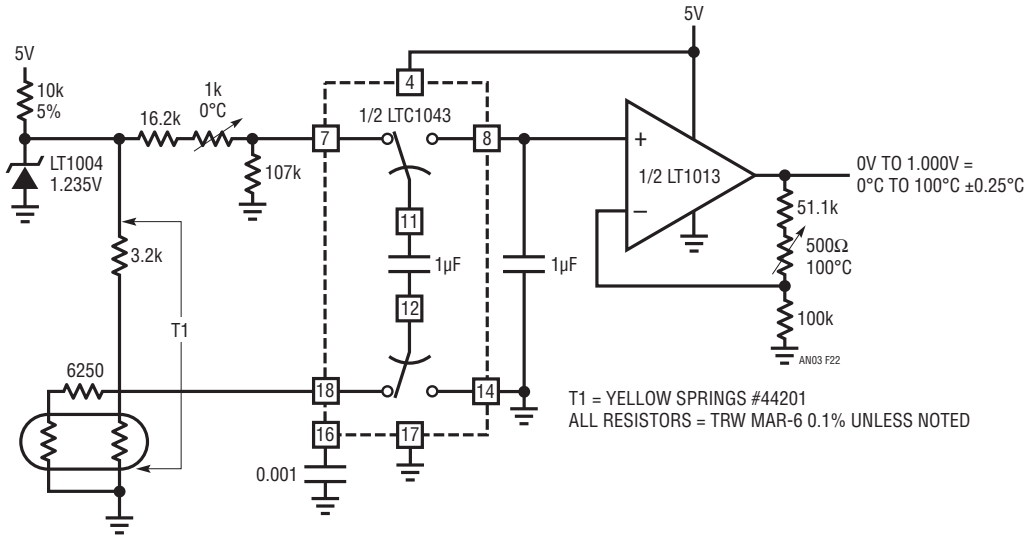


Figure 22. Linear Thermometer

High Current, "Inductorless," Switching Regulator

Figure 23 shows a high efficiency battery driven regulator with a 1A output capacity. Additionally, it does not require an inductor, an unusual feature for a switching regulator operating at this current level.

The LTC1043 switched-capacitor building block provides non-overlapping complementary drive to the Q1-Q4 power MOSFETs. The MOSFETs are arranged so that C1 and C2 are alternately placed in series and then in parallel. During the series phase, the 12V battery's current flows through both capacitors, charging them and furnishing load current. During the parallel phase, both capacitors deliver current to the load. Traces A and B, Figure 24, are the LTC1043-supplied drives to Q3 and Q4, respectively. Q1 and Q2 receive similar drive from Pins 3 and 11. The diode-resistor networks provide additional non-overlapping drive characteristics, preventing simultaneous drive to the series-parallel phase switches. Normally, the output would be one-half of the supply voltage, but C1 and its associated components close a feedback loop, forcing the output to 5V. With the circuit in the series phase, the

output (Trace C) heads rapidly positive. When the output exceeds 5V, C1 trips, forcing the LTC1043 oscillator pin (Trace D) high. This truncates the LTC1043's triangle wave oscillator cycle. The circuit is forced into the parallel phase and the output coasts down slowly until the next LTC1043 clock cycle begins. C1's output diode prevents the triangle down-slope from being affected and the 100pF capacitor provides sharp transitions. The loop regulates the output to 5V by feedback controlling the turn-off point of the series phase. The circuit constitutes a large-scale switched-capacitor voltage divider which is never allowed to complete a full cycle. The high transient currents are easily handled by the power MOSFETs and overall efficiency is 83%.

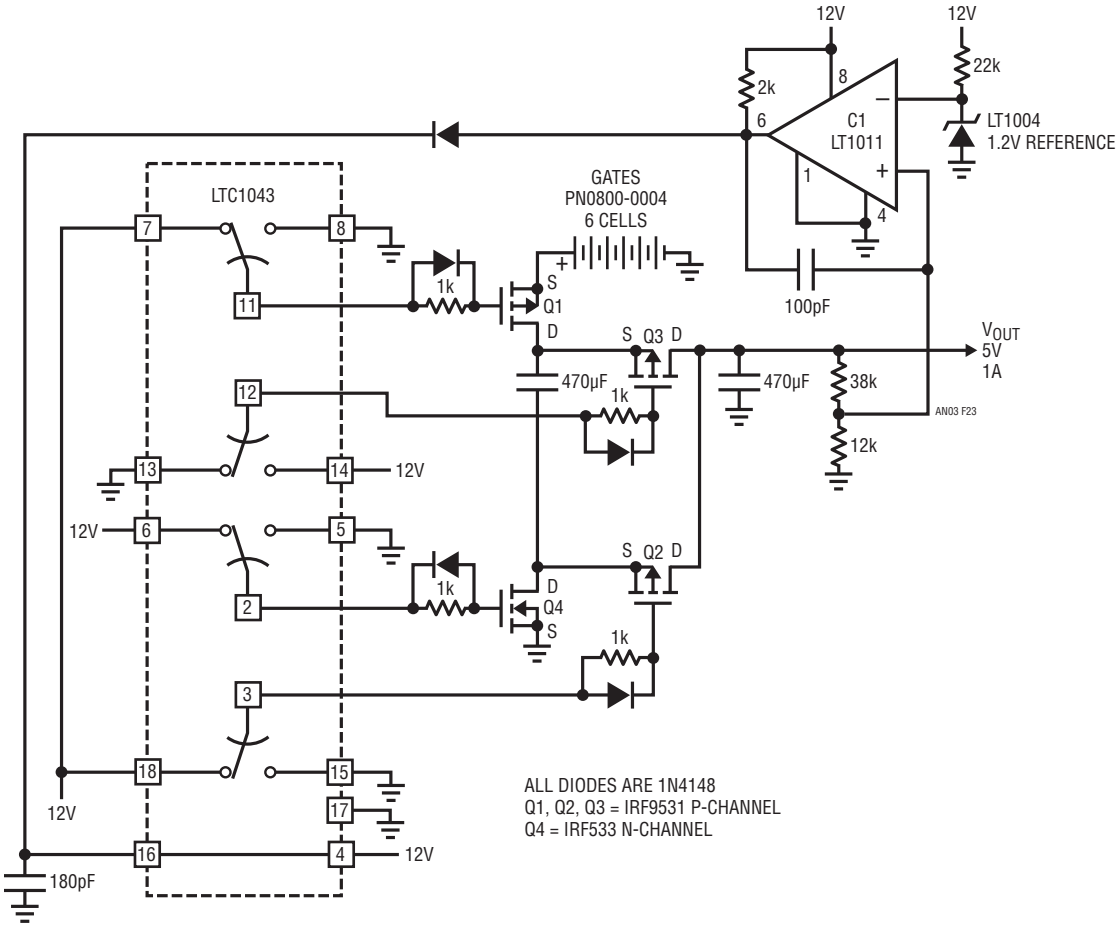


Figure 23. Inductorless Switching Regulator

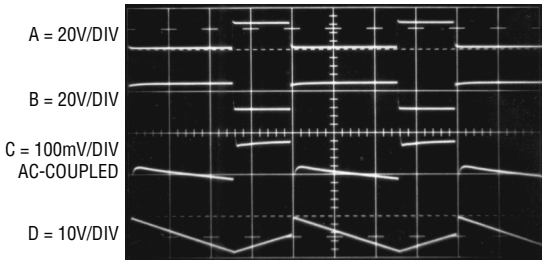


Figure 24

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

GP/IM 0785 10K • PRINTED IN USA