OPTI-LOOP Architecture Reduces Output Capacitance and Improves Transient Response

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INTRODUCTION

Removing output capacitors saves money and board space. Linear Technology's OPTI-LOOP™ architecture allows you to use the output capacitors of your choice and compensate the control loop for optimum transient response and loop stability. Figure 1 shows the dramatic improvement possible with the OPTI-LOOP architecture. With the improvement shown in Figure 1, less capacitance is required or less expensive capacitors can be used. Load dynamics and supply tolerances will predict the minimum output capacitance required. The quality of loop compensation determines how close you can get to this minimum capacitance requirement in a real world system.

One of the least understood areas of power supply design is control loop compensation. Because of this, some manufacturers provide loop compensation inside the regulator IC. Internal compensation works best with one set of operating conditions and is sensitive to output capacitor characteristics. Consequently, more expensive output capacitors may be required to stabilize the loop because of the sensitivities of the internal IC compensation. The OPTI-LOOP architecture is intended to allow circuit designers to squeeze the most performance out of the output capacitors of their choice.
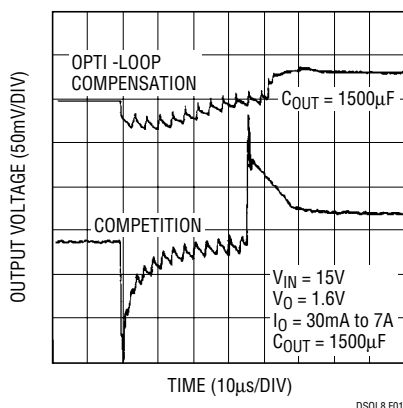

$V_{IN} = 15V$
$V_O = 1.6V$
$I_O = 30mA\ to\ 7A$
$C_{OUT} = 1500\mu F$

Figure 1. Improved Transient Response with OPTI-LOOP Architecture

WHAT IS LOOP COMPENSATION?

Loop compensation is the adjustment of the control loop frequency response to assure loop stability and optimize the transient response of the power supply. The frequency response is determined by the gain and phase of the loop's reaction to load current changes at all frequencies. A Bode plot is used to show the gain and phase of the frequency response.

LOOP COMPENSATION BASICS

This application note contains a brief refresher course in control loop basics. Frequency response is characterized by the effects of poles and zeros. Each pole has a corner frequency, caused by a resistance and capacitance, that determines the beginning of a 20dB/decade drop in voltage gain. The pole also causes the phase to decrease by 90°, starting roughly one decade before the corner frequency and ending about one decade after the corner frequency. A zero has the opposite effect of a pole. It causes the gain to increase by 20dB/decade starting at its "RC" corner frequency and it adds 90° of phase shift, starting one decade before the corner frequency and ending one decade after the corner frequency. The effects of poles and zeros are additive, so that two poles at the same frequency cause a 40dB/decade roll-off in gain and a 180° phase shift over two decades. If a pole and zero occur at the same frequency, their effects cancel.

The crossover frequency of the loop determines the bandwidth and transient response of the power supply. The crossover frequency is the frequency at which the loop gain is one (0dB). The higher the crossover frequency, the faster the power supply can respond to changes in load current.

In a voltage mode DC/DC switching regulator system, the buck inductor and output capacitor form a double pole at their resonant frequency, causing a 40dB/decade gain roll-off and 180° phase shift. Since the inductor's effect on a current mode control loop is largely cancelled by the current loop, it is generally easier to compensate a current mode regulator than a voltage mode regulator.

The first requirement of loop compensation is stability. If the error amplifier's feedback becomes positive when the loop gain equals one, the regulator will oscillate. A loop oscillation appears as a sine wave riding on the DC output voltage at the unity-gain frequency of the control loop. This oscillation will generally occur in the frequency range of 1kHz to 20kHz. Don't confuse switching frequency ripple or higher frequency ringing with a loop instability.

If a network analyzer is available, stability margins can be determined by measuring the gain and phase of the loop and observing the resulting Bode plot. The phase margin is the difference between the signal phase and −360° when the voltage gain is one (0dB). A 60° phase margin is preferred, but 45° is usually acceptable. The gain margin is the amount of negative gain present when the signal phase is zero (−360°). A gain margin of −10dB is normally considered acceptable. Generous gain and phase margins are very important because actual component values vary over temperature and component values differ from unit to unit in production, causing the loop's voltage gain and phase to vary accordingly. If the component values cause the phase to go to zero when the voltage gain is one, the regulator will oscillate. The goal is to provide the best gain and phase margins with the highest crossover frequency possible. A high crossover frequency results in a quick response to load current changes whereas high gain at low frequencies results in fast settling of the output voltage. Nonideal components and amplifier gain limitations generally force a trade-off between high crossover frequency and large stability margins.

THE CONTROL LOOP

Figure 2 shows the simplified control loop for the LTC®1628 and LTC1735/LTC1736 current mode, synchronous buck regulators. The control loop has both DC gain and AC frequency response characteristics. The DC loop consists of the feedback resistors, the error amplifier, the DC resistance of the I_{TH} pin components, the current comparator, the sense resistor and the load resistor. The AC loop consists of the DC loop plus the output capacitor, capacitors C1 and C2 and the AC impedance of the I_{TH} pin components.
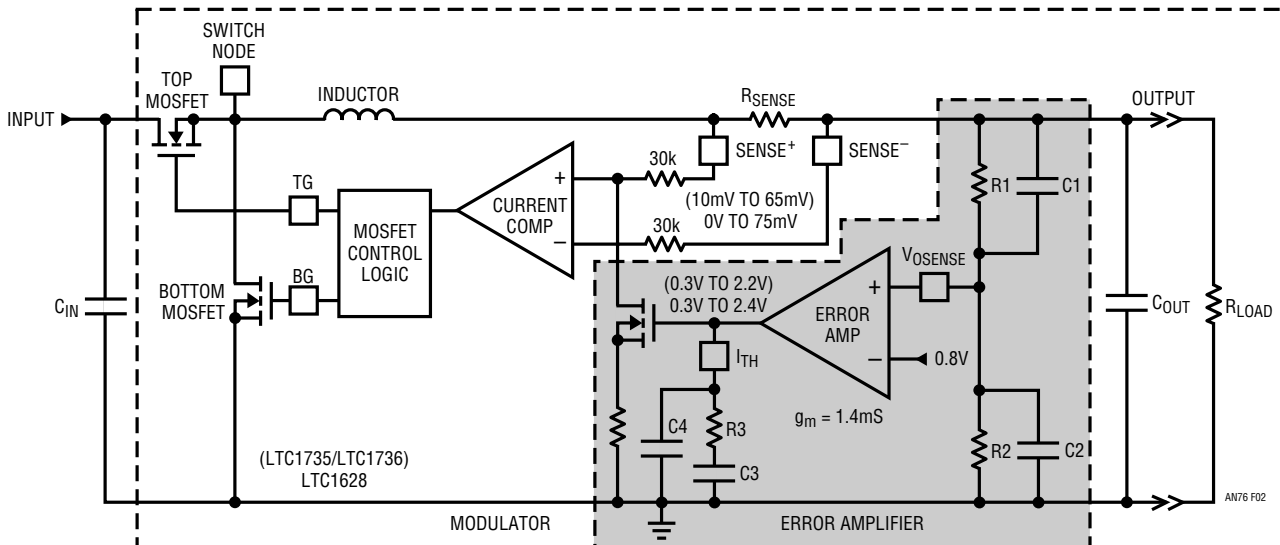

Figure 2. Basic Control Loop of Current Mode, Switching Regulator

DC GAIN

DC gain is the small-signal loop gain under static test conditions. Load regulation is determined by DC gain, so the higher the gain, the lower the change in output voltage for a given DC load current variation. The DC gain is the product of the feedback resistor attenuation, the error amplifier voltage gain and modulator gain. The modulator consists of the current comparator, the MOSFETs and their drivers, the inductor, sense resistor, output capacitor and load resistance: basically the power path.

The feedback divider attenuation is:

$$A_{V(FB)} = V_{REF}/V_{OUT}$$

where: V_{REF} is 0.8V for products in the LTC1735 family and V_{OUT} is the output voltage of the power supply.

The error amplifier voltage gain is:

$$A_{V(EA)} = g_{m(EA)}Z_{ITH}$$

where: $g_{m(EA)}$ is the transconductance of the error amplifier, 1.4mS for products in the the LTC1735 family and Z_{ITH} is the output impedance of the error amplifier in parallel with any impedance connected to the I_{TH} pin.

The transconductance of the modulator must be determined before calculating the modulator gain. The modulator transconductance is:

$$g_{m(MOD)} = (V_{RSENSE(MAX)}/R_{SENSE})/\Delta V_{ITH(MAX)}$$

where: $V_{RSENSE(MAX)}$ is listed in the data sheet as 75mV, R_{SENSE} is the value of the current sense resistor and $\Delta V_{ITH(MAX)}$ is 2.1V for the no-load to full-load output voltage swing of the error amplifier.

The DC voltage gain of the modulator is:

$$A_{V(MOD)} = g_{m(MOD)}R_{LOAD}$$

where: $g_{m(MOD)}$ is the transconductance of the modulator and $R_{LOAD} = V_{OUT}/I_{OUT}$.

As an example, the DC gain for the LTC1735/LTC1736 or the LTC1628 providing 3A at 3.3V is:

$$A_{V(FB)} = V_{REF} /V_{OUT} = 0.8V/3.3V = 0.242 = -12.3 \text{ dB}$$

$$A_{V(EA)} = g_{m(EA)}Z_{ITH} = (1.4mS)(3.28M) = 4592 = 73.2 \text{ dB}$$

where: 3.28M is the typical output impedance of the error amplifier without any external DC loading on the I_{TH} pin.

$$g_{m(MOD)} = (V_{RSENSE(MAX)}/R_{SENSE})/\Delta V_{ITH(MAX)}$$

$$= (0.075V/0.015\Omega)/2.1V = 2.38S$$

$$A_{V(MOD)} = g_{m(MOD)}R_{LOAD} = (2.38S)(3.3V/3A)$$

$$= 2.62 = 8.4dB$$

$$DC \text{ Gain} = (A_{V(FB)})(A_{V(EA)})(A_{V(MOD)})$$

$$= (0.242)(4592)(2.62) = 2911 = 69.3dB$$

FREQUENCY RESPONSE

Frequency response is the loop's reaction to perturbations at all frequencies and is shown as gain and phase measurements on a Bode plot. The output capacitor and load resistance largely determine where the error amplifier poles and zeros need to be placed for optimum transient response and loop stability.

Output Capacitor Pole and Zero

The gain at very low frequencies is equal to the DC gain. Normally the first departure from that gain is the pole created by the load resistance and the output capacitance. The corner frequency of this pole is:

$$f_P = 1/(2\pi R_L C_{OUT})$$

where: R_L is the load resistance and C_{OUT} is the output capacitance.

Notice that as the output current goes down, the equivalent load resistance goes up, causing the pole frequency to decrease. The same is true when the output capacitance increases, that is, the pole frequency moves lower.

The amount of phase margin is largely determined by the zero formed by the output capacitance and capacitor ESR. The corner frequency of this zero is:

$$f_Z = 1/(2\pi ESR \bullet C_{OUT})$$

It is interesting to note that doubling the number of like output capacitors will lower the pole frequency by half but will not change the zero frequency of the output capacitor. This is true because, as the capacitance doubles, the ESR is halved, yet the load resistance remains the same. Consequently, the product of R_L and C_{OUT} goes up, but the product of ESR and C_{OUT} remains the same. It is desirable that the crossover frequency be higher than the ESR zero

frequency because the phase shift of the ESR zero is very helpful in achieving adequate phase margin.

Different types of capacitors have different amounts of ESR per µF of capacitance. The ESR of the output capacitor determines the output ripple voltage under static load conditions and greatly affects the output response to transient loads. For a 3A output, the inductor ripple current should be about 1A$_{P-P}$. Therefore, the output capacitor ESR should be about 0.05Ω for a 50mV$_{P-P}$ output voltage ripple. The difference in frequency response between Panasonic's Specialty Polymer output capacitors and aluminum electrolytic output capacitors, with 0.05Ω of ESR, is shown in Figures 3 and 4.
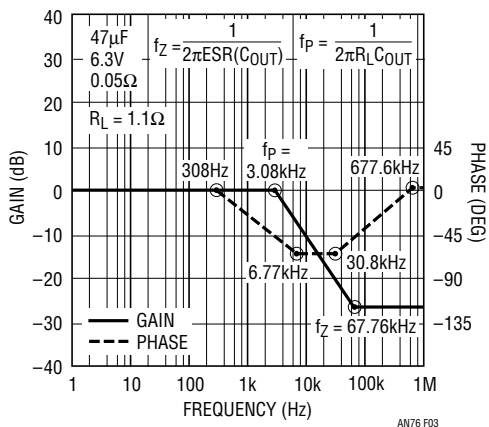

Figure 3. Frequency Response of Specialty Polymer Capacitor Used in 3.3V, 3A Power Supply Output
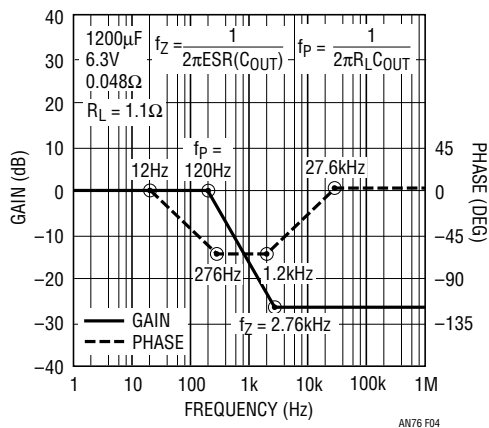

Figure 4. Frequency Response of Aluminum Electrolytic Capacitor Used in 3.3V, 3A Power Supply Output

Aluminum electrolytic capacitors are often selected for both the input and output of very low cost power supplies. Figure 3 shows a 3kHz pole for a 47µF, 6.3V, 0.05Ω Specialty Polymer capacitor. Figure 4 shows a 120Hz pole for a 1200µF, 6.3V, 0.05Ω aluminum electrolytic capacitor. In order to maintain the 0.05Ω ESR required to meet the output ripple requirement, the aluminum electrolytic capacitor requires 25 times the capacitance of the Specialty Polymer capacitor, causing the aluminum electrolytic capacitor to have a pole frequency at 4% of the specialty polymer capacitor.

The loop compensation must be quite different when aluminum electrolytic capacitors are used. It is unlikely that fixed internal compensation will work well with both types of capacitors. Although bandwidth will suffer when aluminum electrolytic capacitors are used, using an OPTI-LOOP architecture, the loop can be optimized for their use and stable operation achieved. The high ESR zero frequency of the Specialty Polymer capacitors makes the loop more difficult to compensate, but the bandwidth will be significantly higher as a result of the extra effort.

The Modulator

The modulator controls the inductor current as a function of the amplified error signal from the error amplifier. The transconductance of the modulator, calculated earlier, is determined by the maximum current allowed through the sense resistor divided by the maximum voltage swing of the error amplifier output at the I$_{TH}$ pin. The product of the modulator transconductance and the load resistance is the modulator gain for DC. The frequency response of the modulator is determined by multiplying the modulator gain at DC times the frequency response of the output capacitor and the load resistance. This is the same as changing the 0dB gain reference on Figures 3 and 4 to the modulator gain level. Consequently, the frequency response of the modulator is primarily determined by the output capacitor and the load resistance.

The Error Amplifier

The error amplifier provides most of the loop gain. After selecting the output capacitor, the control loop is compensated by tailoring the frequency response of the error amplifier. It has a transconductance of 1.4mS and an output resistance of 3MΩ, so it provides a low frequency gain of 4600 or 73dB. The loop gain is the product of the error amplifier gain and the modulator gain, so the frequency response of the error amplifier, the output capacitor and load resistor determine the frequency response of the loop.

The AC behavior of the error amplifier is determined by C1, C2, C3, C4, R1, R2 and R3 as shown in Figure 2. The following relationships are given as a first approximation, since there is some interaction between the parts. As an example, the low frequency pole of the error amplifier is the dominant pole and is determined primarily by C3 and the output resistance of the error amplifier as shown by:

$$f_P = 1/(2\pi R_{O(EA)}C3)$$

However, R3 and C4 have a small effect on the actual corner frequency, since the series combination of C3 and R3 are in parallel with C4, which is in parallel with $R_{O(EA)}$. Although all three impedances interact, the resistance of R3 is small compared to the impedance of C3 at the pole frequency, so its effect is small. The same is true of C4. Since the value of C4 is normally small compared to C3, the primary effect is determined by C3.

Resistor R3 adds a zero to the frequency response to control gain in the midfrequency range. This zero frequency is:

$$f_Z = 1/(2\pi R3C3)$$

Capacitor C4 adds a pole to reduce very high frequency gain. Although frequently unnecessary for loop stability, C4 helps to filter the effects of PCB noise and output ripple voltage from the loop. It is desirable to have the error amplifier gain be less than zero dB at the switching frequency. The high frequency pole created by C4 is:

$$f_P = 1/(2\pi R3C4)$$

The high frequency zero created by C1 and R1 can be very important for transient load applications. Capacitor C1 provides phase lead and acts like a speed-up capacitor to output voltage changes, so it tends to "short-out" R1 and

improve the high frequency response. This zero tends to produce a positive-going bump in the phase plot. Ideally, the peak of this bump is centered over the loop's crossover frequency. The R1, C1 zero is located at:

$$f_Z = 1/(2\pi R1C1)$$

The pole created by R2 and C2 is generally not critical for loop stability. It is frequently set at one half to one third of the switching frequency and is primarily used for noise filtering rather than loop compensation. The effect of C2 is normally countered by the value of R3. The R2, C2 pole frequency can be calculated by:

$$f_P = 1/(2\pi R2C2)$$

I_{TH} PIN COMPONENT VALUES

Selecting the best values for the loop compensation components is not as simple as selecting pole and zero frequencies for the ideal crossover frequency. Several other factors should be taken into account. The slew rate and amplitude of the load transient largely determine the ESR requirement of the output capacitor. The amount of capacitance used at the output is primarily determined by the type of capacitor used and partially determined by the load transient characteristics.

PCB-generated noise can have a considerable effect on the operation of a power supply. Problems caused by PCB noise should be corrected by layout improvements but this is not always possible. Proper decoupling and loop bandwidth limiting can significantly reduce the effects of PCB noise on regulator operation. However, reducing loop bandwidth will also reduce dynamic performance.

Good transient response and PCB noise reduction are opposing requirements when determining the values of the I_{TH} pin components. The final loop compensation must have good stability margins. There are no equations that will yield component values to optimize the loop transient response, give good PCB noise reduction and provide the required stability margins. The equations given for pole and zero frequencies are handy references for predicting the effect a part change will have on the frequency response. Although gain can be calculated reasonably accurately, phase calculations tend to have large errors because of the many parasitics in the power path.

The best procedure for optimizing the compensation component values in your circuit is to start with the values that are recommended in the regulator data sheet. This will generally result in a stable, but probably less than optimal loop compensation. Check the output for any signs of loop oscillation. If the loop is oscillating, try raising the value of C4 to a large value, 0.01uF. This will most likely produce a very sluggish but stable system to begin testing. Connect the load pulse test circuit of Figure 8 to the board and apply load steps approximately 25% of full load to see how the loop responds to these perturbations.

If the response is not as desired, remove the I_{TH} pin components R3, C3 and C4. Connect an RC substitution box, through a short twisted pair of wires, between the I_{TH} pin and SGND of the regulator. It is a good idea to terminate the wires from the RC substitution box with a 47pF capacitor located at C4. Set the substitution box for a series RC connection. Then, by adjusting the values of R and C, you can dial in the optimal response. Read the section "The Effect of Loop Compensation Components on Large-Signal Transients" presented later and use Figures 9 through 21 as a guide in determining which way to vary R and C.

Avoid excessive ringing in the transient waveform. Point C in Figures 6 and 7 shows a single overshoot bump that is acceptable. Two bumps constitute ringing which indicates poor phase margin. Once satisfactory compensation is obtained, install the selected component values on the board and verify the performance is similar to what was obtained with the RC box. Due to the effects of noise pickup and parasitics, there may be a little difference in the behavior of the system using the substitution box compared to using real parts on the board.

If stability margins cannot be measured, stable performance can be predicted if each compensation component value can be doubled or halved without causing excessive ringing in the transient waveform. The last step in the frequency compensation process should be to individually change the values of C1, C2, C3, C4 and R3 to 50% and to 200% of their final value. If one value causes excessive ringing because of this change, compensation component values should be revaluated.

One thing to keep in mind is that no amount of fiddling with the compensation will make up for having inadequate output capacitors for the desired transient response. The goal is to obtain the best possible response from the chosen power path components. If this doesn't meet the system requirements, the only solution is to add more output capacitors (to reduce ESR) or lower the inductor value and live with the increased output ripple.

In most cases, the final values selected for the loop compensation components will be a compromise between the best transient performance and the best PCB noise performance. Obviously, improving the board layout to decrease PCB noise is preferred over reducing loop bandwidth. The OPTI-LOOP architecture lets the designer decide how to optimize his circuit and still meet loop stability requirements. The final value set must provide adequate stability margins.

LARGE-SIGNAL vs SMALL-SIGNAL RESPONSE

As the load conditions change, the loop rapidly responds to the new requirements. The amount and rate of load change determines whether the loop response is called a large-signal response or a small-signal response. The difference between large-signal and small-signal response is whether the control loop maintains control of the output. Often this can be seen by looking at the output of the error amplifier. If the I_{TH} pin voltage is between 0.3V and 2.4V, the loop is normally in control of the output and the load variation creates a small-signal response. If the I_{TH} pin voltage is less than 0.3V or equal to 2.4V, the error amplifier is "railed" and the regulator is not operating in a linear region. An exception to the 0.3V to 2.4V rule is when the error amplifier is in slew limit. When the error amplifier is in slew limit, it does not control the loop because the load transient is occurring faster than the error amplifier can respond, so the output capacitors satisfy the transient current until the inductor current can "catch up." During static operation the voltage on the I_{TH} pin should be between 0.3V and 2.2V and is proportional to the load current.

The rules of loop compensation only apply to linear operation. Large-signal response temporarily takes the loop out of operation. However, the loop must respond gracefully going into and out of large-signal response. Large-signal response occurs when the amplitude and rate of load current change are beyond what the supply can respond to. The wider the loop bandwidth, the faster the load transient the loop can respond to.

The regulator's large-signal response is determined by the ESR of the output capacitor, the inductance of the inductor, the input voltage and the bandwidth of the control loop. When the load change requires a large-signal response from the regulator, the slew rate of the error amplifier is very important. If R3 is too small or capacitors C3 or C4 are too large, it will take longer for the error amplifier's output voltage to rail. During the time between the application of the load transient and the turn-on of the top MOSFET, the output capacitor must supply all of the current required by the load. Current supplied by the output capacitor develops a voltage drop across the ESR that subtracts from the output voltage. The lower the ESR, the lower the voltage loss when the output capacitor supplies load current.

After the top MOSFET turns on, the higher the input voltage and the lower the buck inductor value, the faster the output voltage will return to normal. The relationship of voltage, current and inductance is shown as:

$$\Delta t = \frac{L\Delta I}{E_L}$$

where: E_L is equal to $V_{IN} - V_{OUT}$, L = inductance value, ΔI = the inductor current change during Δt, where Δt = the time required for the inductor current to increase to the new load current level.

A lower inductor value produces a higher output current slew rate at the expense of higher output voltage ripple.

POWER SUPPLY TRANSIENT RESPONSE

System Supplies

One of the most important applications of the OPTI-LOOP architecture is loop compensation in transient load applications. The system supply in most products today includes 5V and 3.3V. Most load transients on 5V supplies are caused by digital circuits and motors. Digital circuit transients are short in duration and vary from a few miliamps to several amps in amplitude. Load transients caused by floppy drives and other motors range in current from 0.5A to several amps during a period of 50ms to seconds, depending on how long it takes the motor to spin up. A properly designed circuit with adequate bandwidth can easily handle motor load transients.

Most 3.3V supplies power digital and memory circuits where the transients are fast, short in duration and vary from miliamps to amps. The majority of digital circuit and memory transients should be handled by local decoupling capacitors at each IC. Local IC decoupling slows down and averages the actual transient load requirements of each IC so that the power supply control loop can handle the perturbations.

Core Voltage Supply

The transient requirements of modern CPU core supplies require large-signal response from the regulator. Consequently, the entire core voltage supply should be optimized for the needs of the CPU. The core voltage supply should be located as close to the CPU as possible, operate at the highest frequency possible with the lowest value of inductor possible and it should take its input power from the 5V power supply rather than the raw battery voltage. By operating the CPU regulator from the 5V supply, it can switch at a much higher frequency with a lower inductor value and higher efficiency. By keeping the voltage step-down ratio relatively small, the loop dynamics can be optimized.

Figure 5 shows the LTC1736 used as a core voltage regulator capable of supplying 10.2A from a 5V input supply at an output voltage selected by the five VID control lines. Typical output voltages range from 1.3V to 1.6V. Figure 6 shows a close-up of the large-signal response of the LTC1736 at the load. The load current changes from 0.2A to 10.2A in about 80ns. Point A shows the effect of ESL and trace inductance between the power supply and the load. Point B shows the effect of the ESR of the output capacitors and Point C shows where the buck inductor current starts to supply load current.

Figure 7 shows a picture of the output voltage when the load current rapidly changes from 10.2A to 0.2A. When the load current changes from full load to light load, the inductor current cannot change instantaneously so it discharges its stored energy into the output capacitor, developing a voltage drop across the capacitor ESR and producing an ESL spike due to the fast change of the load current. The ESL spike and the voltage drop across the ESR cause a temporary rise in output voltage.

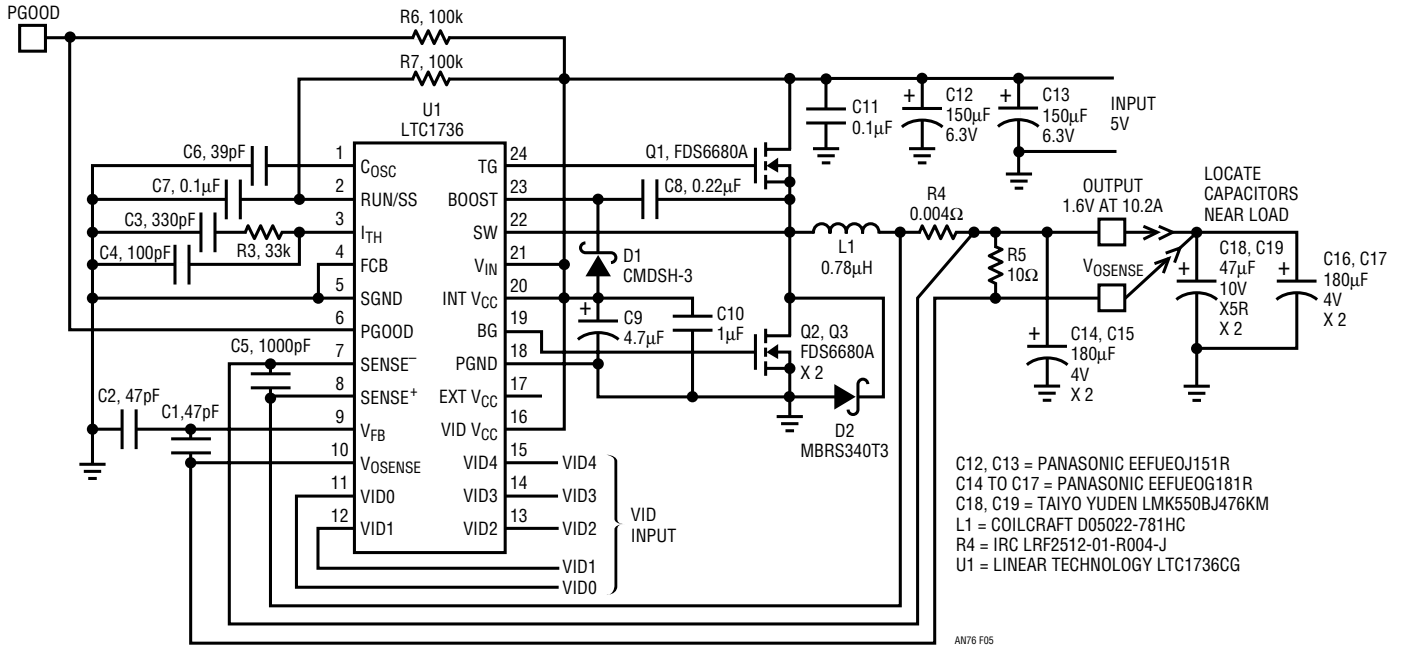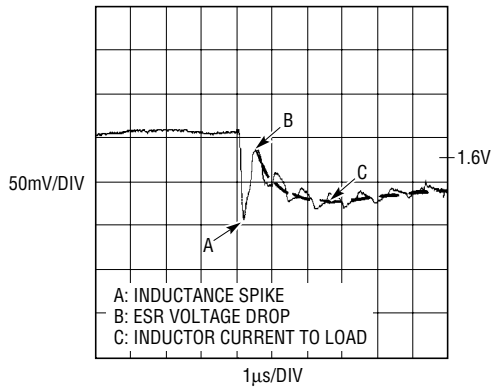**Figure 5. Core Voltage Supply with VID Control**

50mV/DIV

1.6V

A: INDUCTANCE SPIKE
B: ESR VOLTAGE DROP
C: INDUCTOR CURRENT TO LOAD

1μs/DIV

AN76 F06

Figure 6. Close-Up View of Output Voltage During Low Current-to-High Current Transistion

50mV/DIV

1.6V

A: INDUCTANCE SPIKE
B: ESR VOLTAGE
C: INDUCTOR CURRENT = LOAD CURRENT

1μs/DIV

AN76 F07
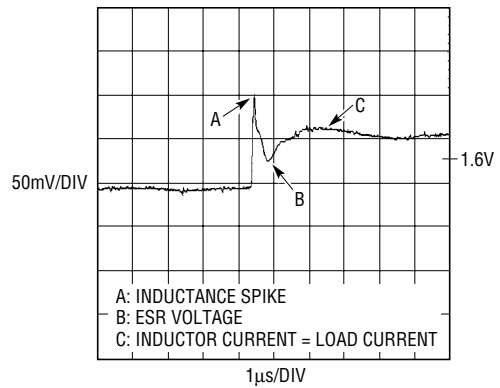
Figure 7. Close-Up View of Output Voltage During High Current-to-Low Current Transistion

Inductance Delays Transient Response

The load transient amplitude primarily determines the ESR required for the output capacitors. However, the inductance between the output capacitors and the CPU determines the initial voltage sag at the CPU. This inductance is made up of the ESL of the output capacitors, trace inductance and connector inductance.

The core voltage regulator should be located very close to the CPU but some of the output capacitors should be located even closer. The trace lengths should be absolutely as short as possible between the power inputs of the CPU and the body of the bulk ceramic capacitors. These ceramic capacitors should be selected to supply the leading edge transient current while the ESL of the other capacitors delays their contribution to the new load requirement. Additional low ESR tantalum or Specialty Polymer capacitors should be placed as close as possible to the ceramic capacitors. The rest of the output capacitors should be very close to the output of the core voltage regulator, but still less than 0.5" away from the filter capacitors located at the CPU.

A simple calculation shows the delaying effect of inductance at transient speeds.

$$X_L = 2\pi fL$$

where: X_L is the impedance of inductance, f is the frequency equal to 1/(actual load transition time) and L is the inductance of interest.

An X_L of 1.25Ω can be calculated using the general rule of 20nH per inch of trace length, two 0.5" traces and a 100ns transition time. Since package inductances and trace inductance are in series with the ESR, the delaying effect of X_L and ESR add to cause the leading edge voltage sag at the load. After ESL and the trace inductance charge up to the output current, the voltage drop across the ESR continues to decrease the output voltage. The effects of ESR and X_L are shown at points A and B in both Figures 6 and 7. Clearly, series inductance must be very low (less than 1nH) for these designs to operate successfully.

Measuring Transient Response

Transient response should be measured across a ceramic capacitor as close to the input power pins of the CPU or other dynamic load as possible. Good high frequency measurement techniques are required. A common practice is to solder bus wire leads to the ends of a 1µF capacitor nearest the power pins on the CPU. Extend these bus wire leads up from the board about 0.5". Disassemble the scope probe by removing the grabber so that the ground ring and center pin are exposed. Carefully touch the ground ring to the bus wire connected to the ground side of the 1µF capacitor and touch the probe center pin to the bus wire connected to the other side of the 1µF capacitor. This measurement technique will avoid most of the signal pickup common to oscilloscope measurements in noisy environments. Remember to check the transient response over the full range of input voltages and possible load current changes.

For preliminary testing, try using the load pulser circuit shown in Figure 8. It can be modified to test a wide variety of power supply circuits. Resistor R2 sets the minimum load current while both R1 and R2 determine the maximum load current. Resistor R4 provides a 50Ω termination for the square wave generator that drives Q1. The slew rate control, R3, controls the rate at which current is taken from the power supply under test.

For breadboard testing with the load pulser, change the values of R1, R2 and R3 as required. Measure the transient response across the last output capacitor using the raised-bus-wire and disassembled-scope-probe measurement technique.
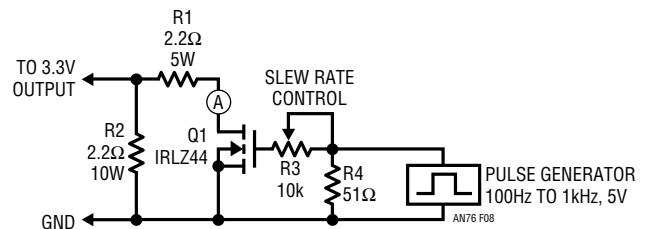

Figure 8. Load Pulser Circuit

The load pulser is a very simple circuit that can be used for general purpose loop response testing. The disadvantage of this circuit is the amount of inductance in the switched-current loop. This inductance slows the load current slew rate and causes ringing on the rising and falling edges. This simple test circuit is useful for observing the settling performance of the control loop but will not give good information on absolute transient response amplitude. A much more sophisticated test setup is required to evaluate this behavior. The best transient response testing can be done with the real load on the final PCB.

Another benefit of the OPTI-LOOP architecture is that simple passive component value changes can be made to fine tune the transient response and loop compensation on the final board, at any point in the development program, without board modifications.

The Effect of Loop Compensation Components on Large-Signal Transients

The circuit shown in Figure 5 was used to demonstrate the effect of individually changing the loop compensation component values by a factor of 10. Figure 9 shows the normal transient response with the values shown in the schematic. The frequency response of this circuit is shown in the Bode plot of Figure 10. The Bode plot indicates that this circuit has been optimized for fast transient response.

Figures 11 and 12 show the effects of changing C3 to 10pF and 3300pF, respectively. This capacitor normally determines the low frequency pole of the error amplifier. As the capacitance value goes down, the pole frequency goes up. Figure 11 shows a slight additional ringing as the overshoot returns to normal. Figure 12 shows the effect of decreasing the low frequency pole, thereby reducing the low frequency gain. Although the peak-to-peak amplitude of the transient didn't change, it took much longer for the loop to return the output to normal. The Figure 13 Bode plot shows that increasing C3 to 3300pF caused the phase margin to drop from 47° down to 33° and decreased the gain margin to –7dB.
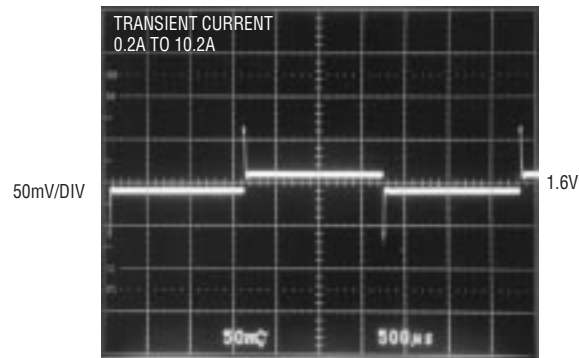

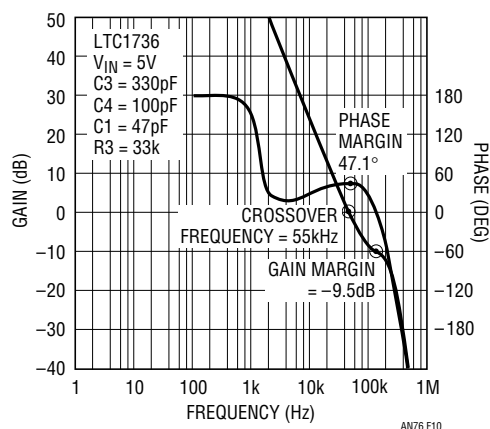**Figure 9. Transient Response with Normal Compensation Values Shown on Schematic**

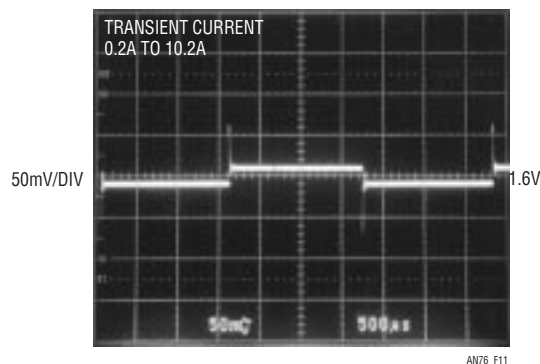**Figure 10. Bode Plot of LTC1736 Circuit**

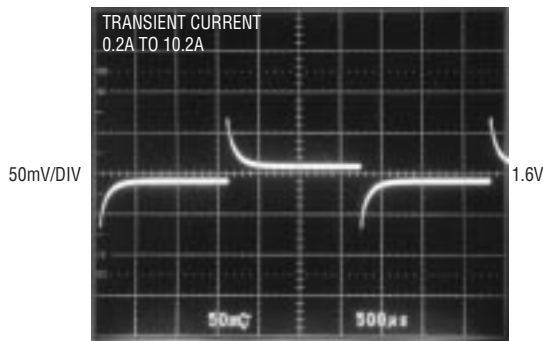**Figure 11. Transient Response with C3 Changed from 330pF to 10pF**

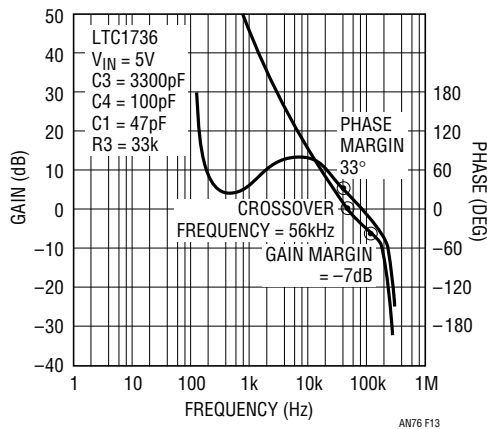**Figure 12. Transient Response with C3 Changed from 330pF to 3300pF**

LTC1736
V_{IN} = 5V
C3 = 3300pF
C4 = 100pF
C1 = 47pF
R3 = 33k

PHASE MARGIN 33°

CROSSOVER FREQUENCY = 56kHz

GAIN MARGIN = −7dB

Figure 13. Bode Plot of LTC1736 Circuit with C3 Changed from 330pF to 3300pF

Figure 14. Transient Response with R3 Changed from 33k to 330k

Figure 15. Transient Response with R3 Changed from 33k to 3.3k

LTC1736
V_{IN} = 5V
C3 = 330pF
C4 = 100pF
C1 = 47pF
R3 = 3.3k

PHASE MARGIN 20.4°

CROSSOVER FREQUENCY = 28.8kHz

GAIN MARGIN = −26dB

Figure 16. Bode Plot of LTC1736 Circuit with R3 Changed from 33k to 3.3k

Figures 14 and 15 show the effects of changing R3 to 330k and 3.3k, respectively. This resistor sets the midfrequency gain and the zero frequency of the error amplifier. Increasing R3 to 330k increased the midfrequency gain and decreased the zero frequency without much effect on the transient response. Decreasing R3 to 3.3k increased the zero frequency and decreased the midfrequency gain, which caused high frequency ringing and an increase in peak-to-peak transient response. The high frequency ringing is an indication that the phase margin is dangerously low. Figure 16 shows a phase margin of 20.4° and a gain margin of −26dB. This increase in gain margin cannot improve circuit stability with a phase margin of 20.4°.
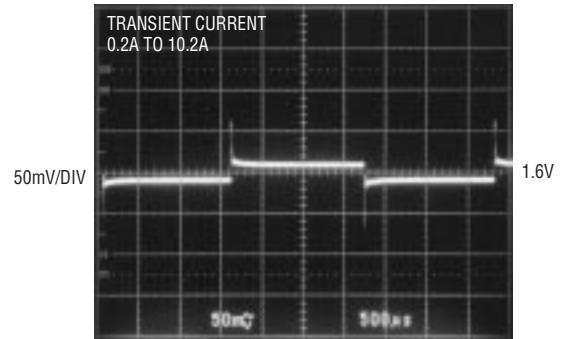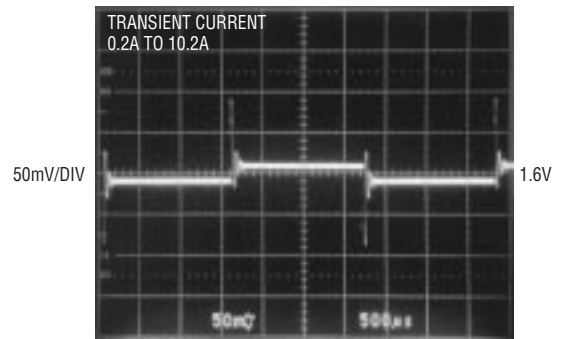
Figures 17 and 18 show the effects of changing C4 to 10pF and 1000pF, respectively. This capacitor normally determines the high frequency pole of the error amplifier. Decreasing C4 to 10pF increased the high frequency pole but had little effect on the transient response. This will make the circuit more susceptible to noise however. By increasing C4 to 1000pF, the high frequency pole decreased so far that the peak-to-peak transient response doubled, with significant high frequency ringing on the rising and falling edges of the transient waveform. Figure 19 shows a phase margin of 14.4°, about 30% of the phase margin obtained when C4 = 100pF.

Figures 20 and 21 show the effects of changing C1 to 5pF and 470pF. This capacitor provides a little phase lead to improve transient response. No change is apparent when the value drops to 5pF but a slight improvement in peak-to-peak transient response can be observed when the value is increased to 470pF.

These waveforms show the type of changes that occur as one value is changed at a time. No damage will occur to the circuit or the load if the incremental changes are within a 10-to-1 range. If the top feedback resistor is open, the connection to the V_{OSENSE} pin is opened or the I_{TH} pin is pulled high, the output voltage will increase until it equals the input voltage. Care should be taken to avoid this condition because output capacitors can be damaged, load resistors overtaxed or CPUs destroyed.

TRANSIENT CURRENT
0.2A TO 10.2A

50mV/DIV   1.6V

DSOL8 F18
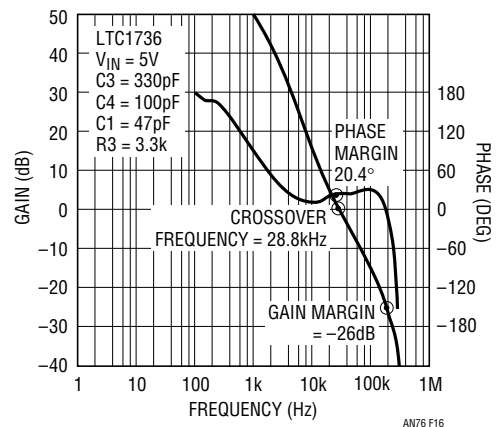
Figure 18. Transient Response with C4 Changed from 100pF to 1000pF

Figure 19. Bode Plot of LTC1736 Circuit with C4 Changed from 100pF to 1000pF

TRANSIENT CURRENT
0.2A TO 10.2A

50mV/DIV   1.6V

AN76 F17

Figure 17. Transient Response with C4 Changed from 100pF to 10pF

TRANSIENT CURRENT
0.2A TO 10.2A

50mV/DIV   1.6V

DSOL8 F20

Figure 20. Transient Response with C1 Changed from 47pF to 5pF

Figure 21. Transient Response with C1 Changed from 47pF to 470pF

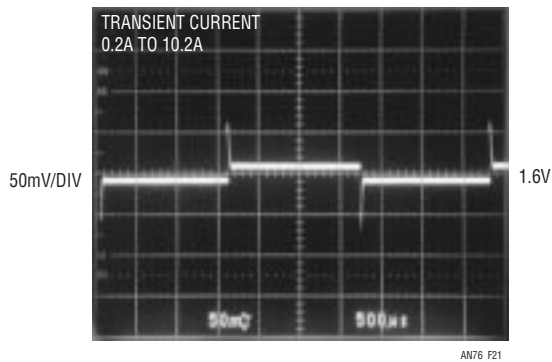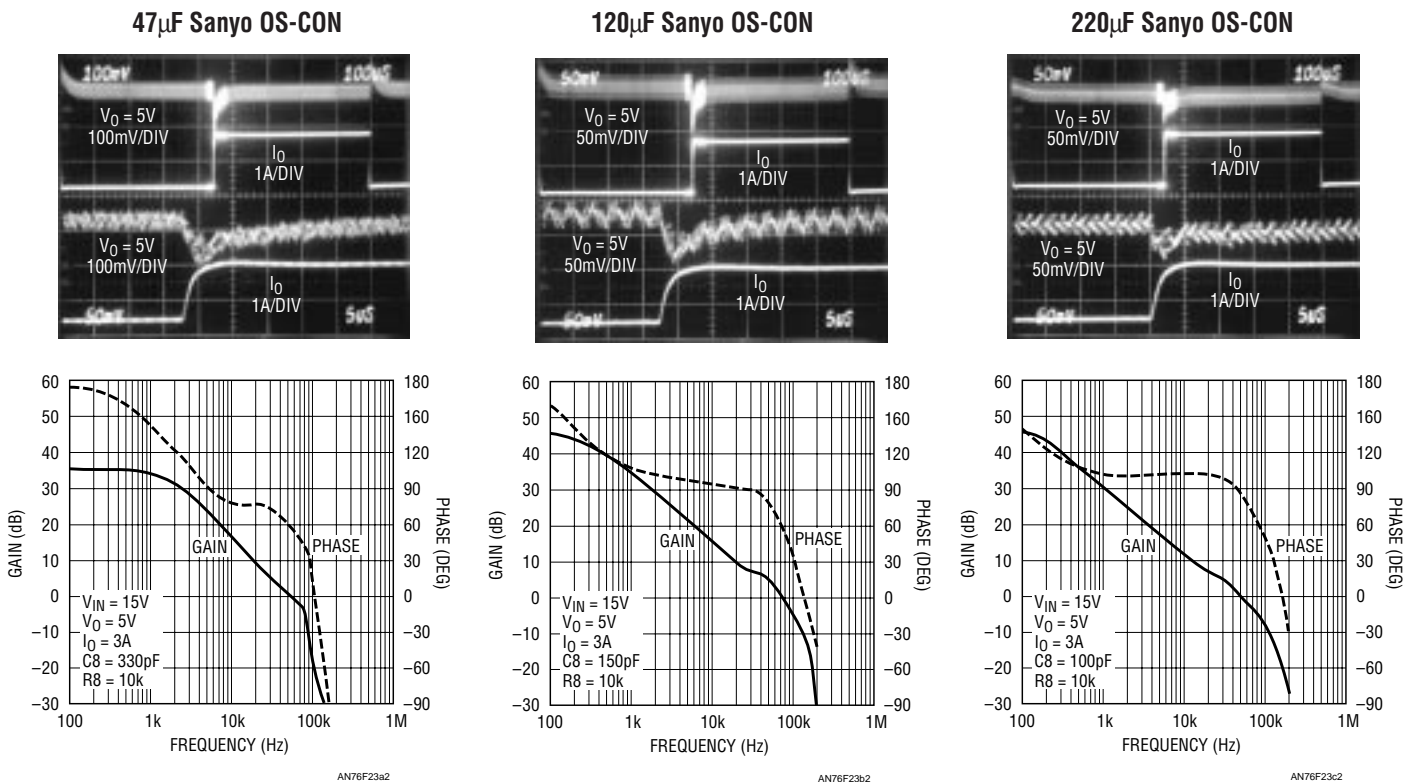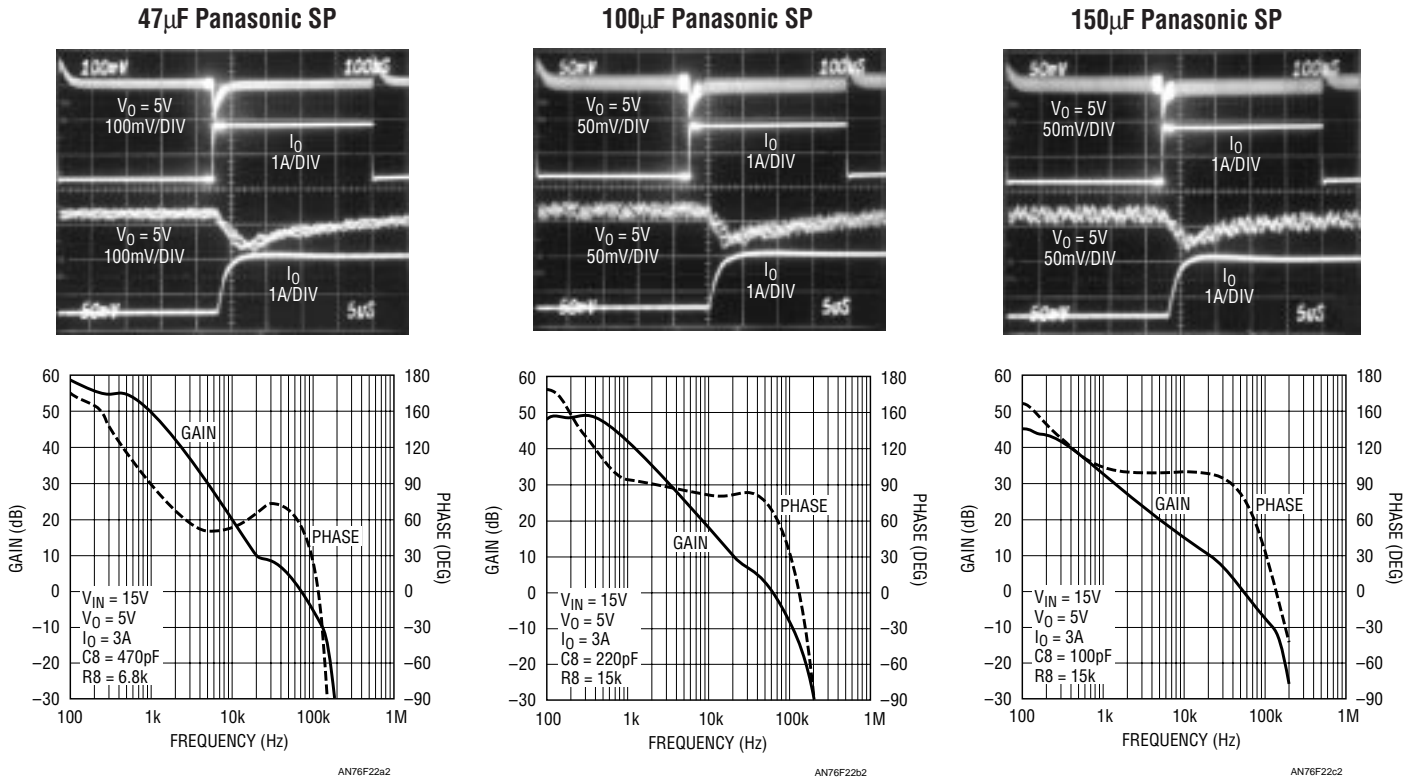## Common Values for System Supply Compensation

The dual version of the LTC1735, the LTC1628, shares the identical control circuitry of the LTC1735 and as such, has some distinct advantages over previous system power (5V and 3.3V) solutions. In addition, the LTC1628 operates the two controller top switches 180° out of phase to minimize RMS input current. Since the system power requirements are less stringent than the CPU core requirements, OPTI-LOOP architecture allows the use of significantly smaller output capacitors than were previously required. Special Polymer capacitors offer extremely low ESR but have less capacitance density than other capacitor types. OPTI-LOOP compensation provides the key to using the small capacitance values while providing extremely good performance, small physical size, and low overall cost.

Oscilloscope photos and Bode plots are included in Figures 22 and 23, illustrating the benefit of the OPTI-LOOP architecture for the LTC1628 5V output using the basic circuit in Figure 24. The compensation components are changed as indicated in each figure for different values and types of output capacitor. The top two waveforms in each photo are the output voltage at the vertical sensitivity indicated in the top left corner and the output current at 1 ampere per division with a time scale of 100μs per division. The lower two traces are the same as above but at a time scale of 5μs per division. A 0.5A to 2A load step is used for a typical transient condition. The expanded scale indicates the response time of the switching regulator is normally several microseconds. A 47μF capacitor having low ESR offers a very acceptable output capacitor solution in applications requiring lowest cost and/or size. A 100μF capacitor can be used where an extra margin of stability and low ripple voltage are required. The 150μF to 220μF capacitance may be required in applications that require extremely low ESR for zero to full designed load current transient steps. Using two small 47μF capacitors provide stability, low ESR *and* a margin of safety in the event of a single capacitor failure.

Table 1 lists suggested OPTI-LOOP compensation values for other types of output capacitors. Figure 24 was also used to verify the selected values in Table 1. Final compensation value selection should be fine tuned after the PC layout is done since the quality of the layout will affect the loop behavior.

47µF Panasonic SP

100µF Panasonic SP

150µF Panasonic SP

Figure 22. LTC1628 Transient Response and Frequency Response with Panasonic SP Capacitors

47µF Sanyo OS-CON

120µF Sanyo OS-CON

220µF Sanyo OS-CON

Figure 23. LTC1628 Transient Response and Frequency Response with Sanyo OS-CON Capacitors
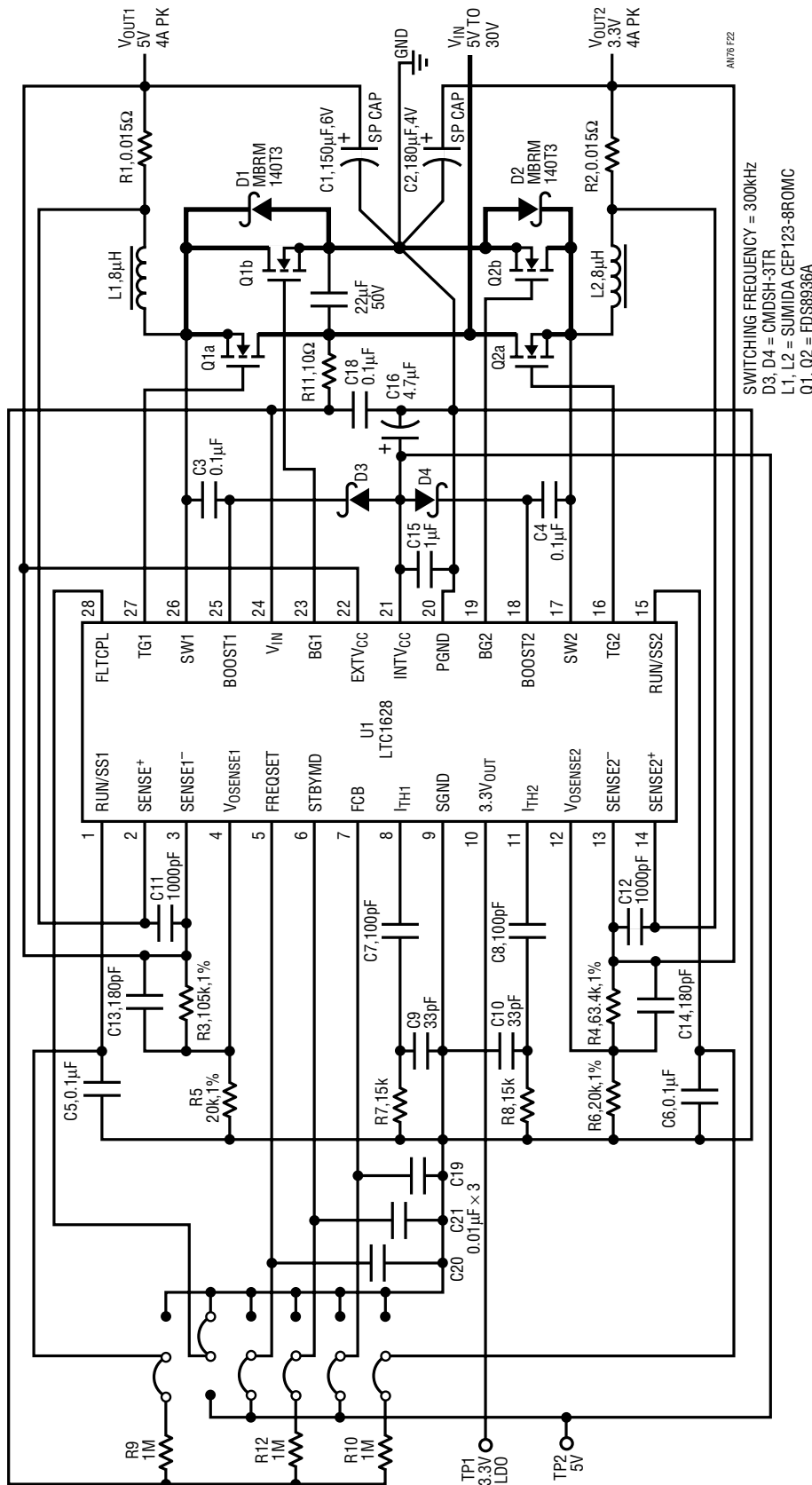
Figure 24. Dual Output System Supply for 5V and 3.3V

SWITCHING FREQUENCY = 300kHz
D3, D4 = CMDSH-3TR
L1, L2 = SUMIDA CEP123-8R0MC
Q1, Q2 = FDS8936A

Table 1. Output Capacitor and Compensation on DC236A (LTC1628 Demo Board)

Test Conditions: V_{IN} =15V, V_{OUT} = 3.3V/3A,
Switching Frequency = 265kHz, Load Step = 1.5A to 2.6A

Output Capacitor	Compensation			
	C13,C14	C7,C8	R7,R8	C9,C10
Panasonic SP 47µF/6.3V*1	27pF	100pF	22k	33pF
Sanyo Oscon 47µF/6.3V*1	27pF	470pF	15k	33pF
Sanyo Poscap TPC 150µF/4V*1	27pF	100pF	22k	33pF
Sanyo Poscap TPC 100µF/6V*1	27pF	100pF	22k	33pF
Sanyo Poscap TPC 68µF/10V*1	27pF	100pF	22k	33pF
AVX Tantalum TPS 220µF/6.3V+10µF Ceramic	27pF	100pF	33k	33pF

Test Conditions: V_{IN} =15V, V_{OUT} = 3.3V/3A,
Switching Frequency = 265kHz, Load Step = 0A to 2A

Panasonic SP 56µF/4V*1	100pF	150pF	15k	33pF

Test Conditions: V_{IN} =15V, V_{OUT} = 3.3V/3A,
Switching Frequency = 265kHz, Load Step = 0.5A to 3A

Panasonic SP*2 56µF/4V+10µF Ceramic	27pF	100pF	22k	33pF
Sanyo Oscon 150µF/6.3V+10µF Ceramic	27pF	100pF	22k	33pF
Sanyo Poscap TPC 150µF/4V*1+ Cer 10µF*2	27pF	100pF	33k	33pF
Sanyo Poscap TPB 150µF/6.3V*2+ Cer 10µF*2	27pF	100pF	33k	33pF
AVX Tantalum TPS 220µF/6.3V*1+ Cer 10µF*1	27pF	100pF	33k	33pF
AVX Tantalum TPS 330µF/6.3V*1+ Cer 10µF*1	27pF	100pF	33k	33pF

CONCLUSION

Control loop compensation is a very involved subject. The ability to improve the output voltage transient response is quite valuable. Optimizing circuit performance for transient load applications without constraints on output capacitors allows the designer to get the most out of the power components. The fear that fixed compensation inside a regulator IC can lead to loop oscillation under certain conditions is valid, since the loop frequency response varies so much with different types of output capacitors. The OPTI-LOOP architecture provides the mechanism for obtaining the maximum performance from the lowest cost power supply.