Ceramic Input Capacitors Can Cause Overvoltage Transients

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A recent trend in the design of portable devices has been to use ceramic capacitors to filter DC/DC converter inputs. Ceramic capacitors are often chosen because of their small size, low equivalent series resistance (ESR) and high RMS current capability. Also, recently, designers have been looking to ceramic capacitors due to shortages of tantalum capacitors.

Unfortunately, using ceramic capacitors for input filtering can cause problems. Applying a voltage step to a ceramic capacitor causes a large current surge that stores energy in the inductances of the power leads. A large voltage spike is created when the stored energy is transferred from these inductances into the ceramic capacitor. These voltage spikes can easily be twice the amplitude of the input voltage step.

Plug In the Wall Adapter at Your Own Risk

The input voltage transient problem is related to the power-up sequence. If the wall adapter is plugged into an AC outlet and powered up first, plugging the wall adapter output into a portable device can cause input voltage transients that could damage the DC/DC converters inside the device.

Building the Test Circuit

To illustrate the problem, a typical 24V wall adapter used in notebook computer applications was connected to the input of a typical notebook computer DC/DC converter. The DC/DC converter used was a synchronous buck converter that generates 3.3V from a 24V input.

The block diagram of the test setup is shown in Figure 1. The inductor L_{OUT} represents the lumped equivalent inductance of the lead inductance and the output EMI filter inductor found in some wall adapters. The output capacitor in the wall adapter is usually on the order of 1000µF; for our purposes, we can assume that it has low ESR—in the 10mΩ to 30mΩ range. The equivalent circuit of the wall adapter and DC/DC converter interface is actually a series resonant tank, with the dominant components being L_{OUT}, C_{IN} and the lumped ESR (the lumped ESR must include the ESR of C_{IN}, the lead resistance and the resistance of L_{OUT}).

The input capacitor, C_{IN}, must be a low ESR device, capable of carrying the input ripple current. In a typical notebook computer application, this capacitor is in the range of 10µF

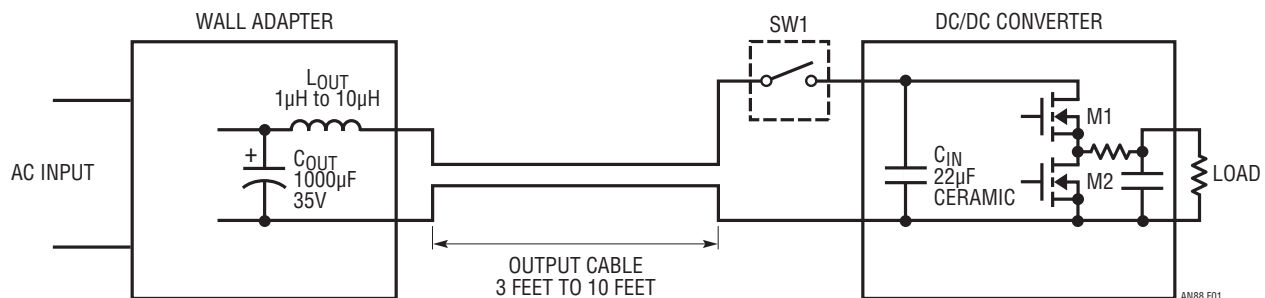**Figure 1. Block Diagram of Wall Adapter and Portable Device Connection**

to 100µF. The exact capacitor value depends on a number of factors but the main requirement is that it must handle the input ripple current produced by the DC/DC converter. The input ripple current is usually in the range of 1A to 2A. Therefore, the required capacitors would be either one 10µF to 22µF ceramic capacitor, two to three 22µF tantalum capacitors or one to two 22µF OS-CON capacitors.

Turning On the Switch

When switch SW1 in Figure 1 is turned on, the mayhem starts. Since the wall adapter is already plugged in, there is 24V across its low impedance output capacitor. On the other hand, the input capacitor C_{IN} is at 0V potential. What happens from t = 0s is pretty basic. The applied input voltage will cause current to flow through L_{OUT}. C_{IN} will begin charging and the voltage across C_{IN} will ramp up toward the 24V input voltage. Once the voltage across C_{IN} has reached the output voltage of the wall adapter, the energy stored in L_{OUT} will raise the voltage across C_{IN} further above 24V. The voltage across C_{IN} will eventually reach its peak and will then fall back to 24V. The voltage across C_{IN} may ring for some time around the 24V value. The actual waveform will depend on the circuit elements.

If you intend to run this circuit simulation, keep in mind that the real-life circuit elements are very seldom linear under transient conditions. For example, the capacitors may undergo a change of capacitance (Y5V ceramic capacitors will loose 80% of the initial capacitance under rated input voltage). Also, the ESR of input capacitors will depend on the rise time of the waveform. The inductance of EMI-suppressing inductors may also drop during transients due to the saturation of the magnetic material.

Testing a Portable Application

Input voltage transients with typical values of C_{IN} and L_{OUT} used in notebook computer applications are shown in Figure 2. Figure 2 shows input voltage transients for C_{IN} values of 10µF and 22µF with L_{OUT} values of 1µH and 10µH.

The top waveform shows the worst-case transient, with a 10µF capacitor and 1µH inductor. The voltage across C_{IN} peaks at 57.2V with a 24V DC input. The DC/DC converter may not survive repeated exposure to 57.2V.

The waveform with 10µF and 10µH (trace R2) looks a bit better. The peak is still around 50V. The flat part of the waveform R2 following the peak indicates that the synchronous MOSFET M1, inside of the DC/DC converter in Figure 1, is avalanching and taking the energy hit. Traces R3 and R4 peak at around 41V and are for a 22µF capacitor with 1µH and 10µH inductors, respectively.
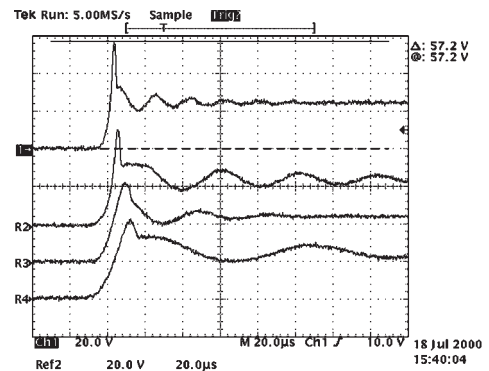

Figure 2. Input Voltage Transients Across Ceramic Capacitors

Table 1. Peak Voltages of Waveforms In Figure 2

TRACE	L_{IN} (µH)	C_{IN} (µF)	V_{IN} PEAK (V)
CH1	1	10	57.2
R2	10	10	50
R3	1	22	41
R4	10	22	41

Input Voltage Transients with Different Input Elements

Different types of input capacitors will result in different transient voltage waveforms, as shown in Figure 3. The reference waveform for 22µF capacitor and 1µH inductor is shown in the top trace (R1); it peaks at 40.8V.

The waveform R2 in Figure 3 shows what happens when a transient voltage suppressor is added across the input. The input voltage transient is clamped but not eliminated. It is very hard to set the voltage transient's breakdown voltage low enough to protect the DC/DC converter and far enough from the operating DC level of the input source (24V). The transient voltage suppressor P6KE30A that was used was too close to starting to conduct at 24V. Unfortunately, using a transient voltage suppressor with a higher voltage rating would not provide a sufficiently low clamping voltage.

The waveforms R3 and R4 are with a 22µF, 35V AVX TPS type tantalum capacitor and a 22µF, 30V Sanyo OS-CON capacitor, respectively. With these two capacitors, the transients have been brought to manageable levels. However, these capacitors are bigger than the ceramic capacitors and more than one capacitor is required in order to meet the input ripple current requirements.
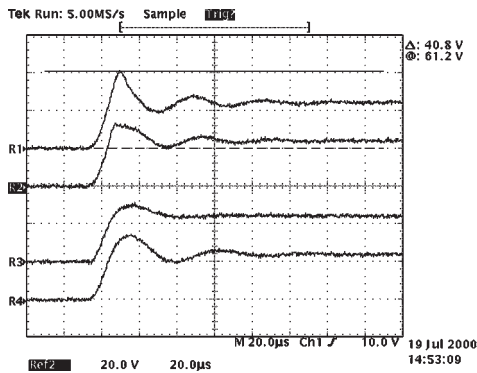

Figure 3. Input Transients with Different Input Components

Table 2. Peak Voltages of Waveforms In Figure 3

TRACE	C_{IN} (µF)	CAPACITOR TYPE	V_{IN} PEAK (V)
R1	22	Ceramic	40.8
R2	22	Ceramic with 30V TVS	32
R3	22	AVX, TPS Tantalum	33
R4	22	Sanyo OS-CON	35

Optimizing Input Capacitors

Waveforms in Figure 3 show how input transients vary with the type of input capacitors used.

Optimizing the input capacitors requires clear understanding of what is happening during transients. Just as in an ordinary resonant RLC circuit, the circuit in Figure 1 may have an underdamped, critically damped or overdamped transient response.

Because of the objective to minimize the size of input filter circuit, the resulting circuit is usually an underdamped resonant tank. However, a critically damped circuit is actually required. A critically damped circuit will rise nicely to the input voltage without voltage overshoots or ringing.

To keep the input filter design small, it is desirable to use ceramic capacitors because of their high ripple current ratings and low ESR. To start the design, the minimum value of the input capacitor must first be determined. In the example, it has been determined that a 22µF, 35V ceramic capacitor should be sufficient. The input transients generated with this capacitor are shown in the top trace of Figure 4. Clearly, there will be a problem if components that are rated for 30V are used.

To obtain optimum transient characteristic, the input circuit has to be damped. The waveform R2 shows what happens when another 22µF ceramic capacitor with a 0.5Ω resistor in series is added. The input voltage transient is now nicely leveled off at 30V.

Critical damping can also be achieved by adding a capacitor of a type that already has high ESR (on the order of 0.5Ω). The waveform R3 shows the transient response when a 22µF, 35V TPS type tantalum capacitor from AVX is added across the input.
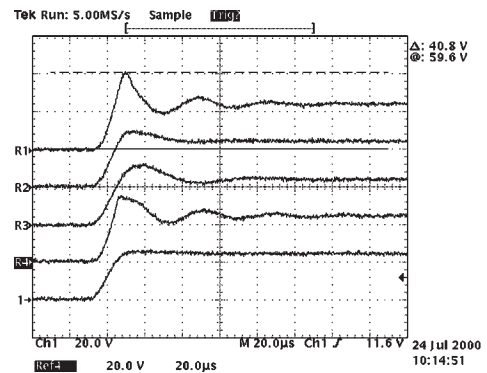

Figure 4. Optimizing Input Circuit Waveforms for Reduced Peak Voltage

Table 3. Peak Voltages of Waveforms In Figure 4 with 22µF Input Ceramic Capacitor and Added Snubber

TRACE	SNUBBER TYPE	V_{IN} PEAK (V)
R1	None	40.8
R2	22µF Ceramic + 0.5Ω In Series	30
R3	22µF Tantalum AVX, TPS Series	33
R4	30V TVS, P6KE30A	35
Ch1	47µF, 35V Aluminum Electrolytic Capacitor	25

The waveform R4 shows the input voltage transient with a 30V transient voltage suppressor for comparison.

Finally, an ideal waveform shown in Figure 4, bottom trace (Ch1) is achieved. It also turns out that this is the least expensive solution. The circuit uses a 47µF, 35V aluminum electrolytic capacitor from Sanyo (35CV47AXA). This capacitor has just the right value of capacitance and ESR to provide critical damping of the 22µF ceramic capacitor in conjunction with the 1µH of input inductance. The 35CV47AXA has an ESR value of 0.44Ω and an RMS current rating of 230mA. Clearly, this capacitor could not be used alone in an application with 1A to 2A of RMS ripple current without the 22µF ceramic capacitor. An additional benefit is that this capacitor is very small, measuring just 6.3mm by 6mm.

Conclusion

Input voltage transients are a design issue that should not be ignored. Design solutions for preventing input voltage transients can be very simple and effective. If the solution is properly applied, input capacitors can be minimized and both cost and size minimized without sacrificing performance.