LINEAR TECHNOLOGY

DESIGN NOTES

Auto-Zeroing A/D Offset Voltage

Design Note 26

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Introduction

Many A/D converters exhibit low offset errors with large full scale voltages. However, when the full scale voltage is decreased the V_{OS}, expressed in LSBs, increases. An A/D converter with 0.5 LSB of offset with a 5V full scale voltage can have 12.5 LSBs of offset with a 200mV full scale voltage. With the LTC®1090 family of data acquisition systems and a few external components it is now possible to reduce the V_{OS} to only 0.25 LSB even with only a 200mV full scale voltage. This allows a user to digitize signals from low voltage transducers without the need for a gain stage.

Circuit Description

The LTC1090 is a 10-bit data acquisition system with an eight channel multiplexer. The channel to be read is software selectable and all channels can be referred to the COM pin. In the circuit of Figure 1, CH0 is used to servo the COM pin giving the use a seven channel, offset corrected data acquisition system.

Figure 2 shows how the processor servos the COM pin to eliminate the A/D offset. CH0 is set to a 0.5 LSB voltage. The COM pin is servoed (by the pulse width

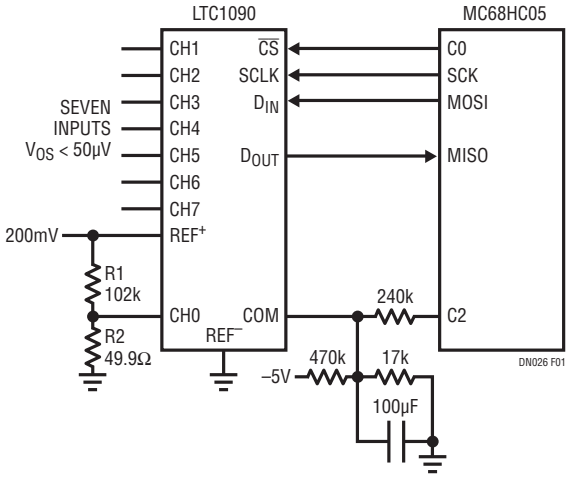

Figure 1. Circuit Provides Seven Channel 10-Bit Data Acquisition System with Less Than 50µV of Offset

modulated signal on port C2) so that the CH0 reading dithers between 0 and 1 LSB. The 100µF filters the PWM signal at the COM pin. Motorola MC68HC05 code is available from LTC to correct the LTC1090 offset and read the remaining seven channels. This algorithm will work in either unipolar or bipolar mode. (Unipolar is shown. For bipolar the 49.9Ω resistor is changed to 100Ω and the decision block is changed to "CH0≤0?".)

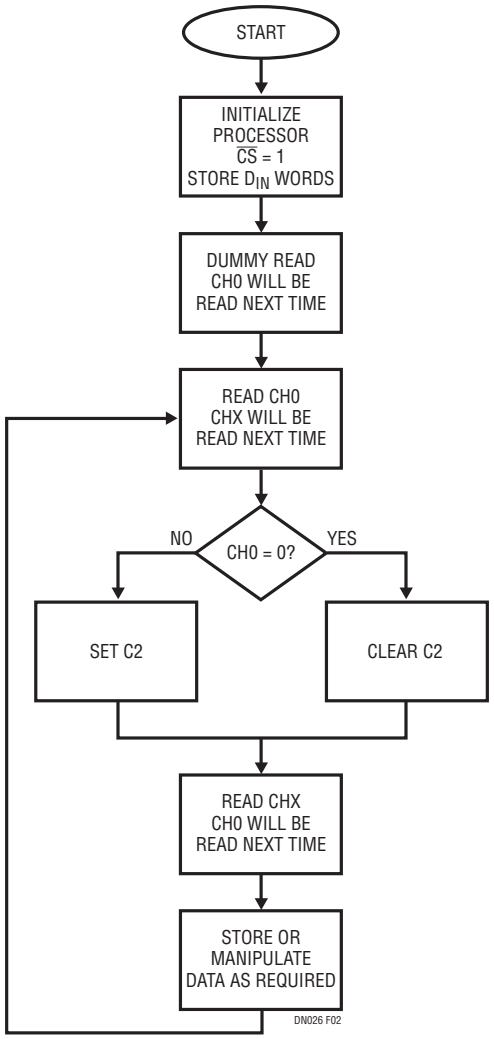

Figure 2. Auto-Zero Flowchart

After initializing the processor, the code sends a D_{IN} word to the LTC1090 requesting CH0 to be read with respect to COM. The next D_{IN} word that is sent will set up the A/D for the desired channel to be read while the CH0 data previously requested is shifted into the processor. If the CH0 D_{OUT} is 0 the C2 is cleared. If the CH0 D_{OUT} is greater than 0 then C2 is set. Another D_{IN} word requesting CH0 data is sent and the D_{OUT} data from the previously requested channel is read into the processor.

As can be seen from the LTC1090 data sheet the linearity and full scale errors with a 200mV full scale voltage are still within 0.5 LSB. To fully take advantage of the reduced offset of the auto-zero circuit the noise of the LTC1090 must be reduced. This can be done by averaging the data with the processor. Figure 3 shows a dynamic cross plot of the output data near half-scale after 64 averages. The top trace is the B9 transition of the LTC1090 while the bottom trace is a binary weight summation of B0 and B1. The horizontal scale is 1 LSB per major division. The averaged noise is much less than 1 LSB.

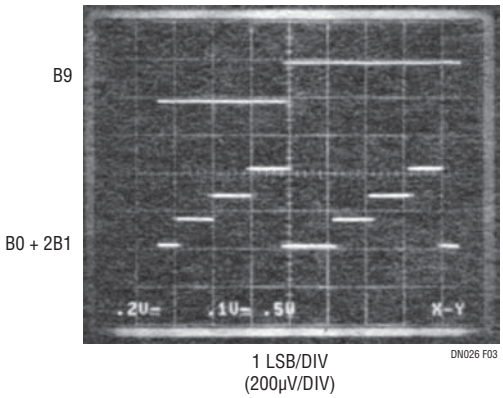

Figure 3. Dynamic Cross Plot Shows Excellent LTC1090 Performance with Only 200mV Full Scale

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