Power Conversion, Measurement and Pulse Circuits

Tales From the Laboratory Notebook, 2005-2007

Jim Williams

INTRODUCTION

This ink marks LTC's eighth circuit collection publication.[1] We are continually surprised, to the point of near mystification, by these circuit amalgams seemingly limitless appeal. Reader requests ascend rapidly upon publication, remaining high for years, even decades. All LTC circuit collections, despite diverse content, share this popularity, although just why remains an open question. Why is it? Perhaps the form; compact, complete, succinct and insular. Perhaps the freedom of selection without commitment, akin to window shopping. Or, perhaps, simply the pleasure of new recruits for the circuit aficionados intellectual palate. Locally based electrosociolgists, spinning elegantly contrived theories, offer explanation, but no convincing evidence is at hand. What is certain is that readers are attracted to these compendiums and that calls us to attention. As such, in accordance with our mission to serve customer preferences, this latest collection is presented. Enjoy.

JFET-Based DC/DC Converter Powered From 300mV Supply

A JFET's self-biasing characteristic can be utilized to construct a DC/DC converter powered from as little as 300mV. Solar cells, thermopiles and single-stage fuel cells, all with outputs below 600mV, are typical power sources for such a converter.

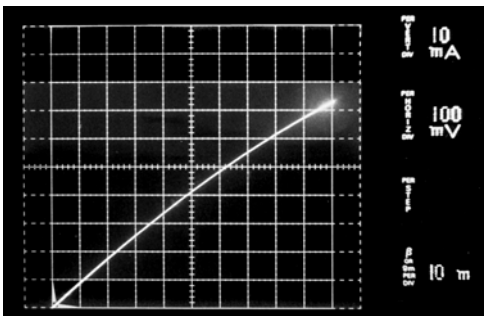

Figure 1. Zero Volt. Biased JFET I-V Curve Shows 10mA Conduction at 100mV, Rising Above 40mA at 500mV. Characteristic Permits DC/DC Converter Powered From 300mV Supply.

Figure 1, an N-channel JFET I-V plot, shows drain-source conduction under zero bias (gate and source tied together) conditions. This property can be exploited to produce a self-starting DC/DC converter that runs from 0.3V to 1.6V inputs.

Figure 2 shows the circuit. Q1 and T1 form an oscillator with T1's secondary providing regenerative feedback to Q1's gate. When power is applied, Q1's gate is at zero volts and its drain conducts current via T1's primary. T1's phase inverting secondary responds by going negative at Q1's gate, turning it off. T1's primary current ceases, its secondary collapses and oscillation commences. T1's primary action causes positive going "flyback" events at Q1's drain, which are rectified and filtered. Q2's ≈ 2V

Note 1. Previous efforts include References 4, 6, 7 and 23-26.

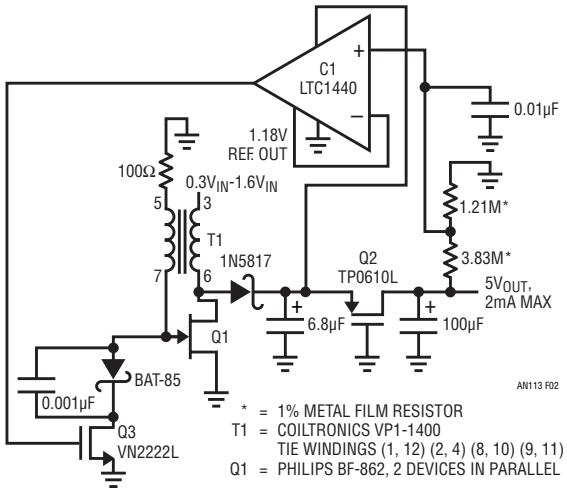

Figure 2. JFET-Based DC/DC Converter Runs From 300 Millivolt Input. Q1-T1 Oscillator Output Is Rectified and Filtered. Load Is Isolated Until Q2 Source Reaches ≈2V, Aiding Start-Up. Comparator and Q3 Close Loop Around Oscillator, Controlling Q1's On-Time to Stabilize 5V Output.

turn-on potential isolates the load, aiding start-up. When Q2 turns on, circuit output heads towards 5V. C1, powered from Q2's source, enforces output regulation by comparing a portion of the output with its internal voltage reference. C1's switched output controls Q1's on-time via Q3, forming a control loop.

Waveforms for the circuit include the AC coupled output (Figure 3, trace A), C1's output (trace B) and Q1's drain flyback events (trace C). When the output drops below 5V, C1 goes low, turning on Q1. Q1's resultant flyback events continue until the 5V output is restored. This pattern repeats, maintaining the output.

The 5V output can supply up to 2mA, sufficient to power circuitry or furnish bias to a higher power switching regulator when larger current is required. The circuit will start into loads of 300µA at 300mV input; 2mA loading requires a 475mV supply. Figure 4 plots minimum input voltage versus output current over a range of loads.

Q3's shunt control of Q1 is simple and effective, but results in 25mA quiescent current drain. Figure 5's modifications reduce this figure to 1mA by series switching T1's secondary. Here, Q3 switches series connected Q4, more efficiently controlling Q1's gate drive. Negative turn-off

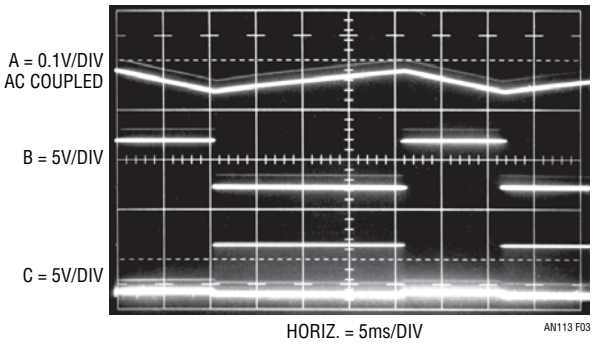

Figure 3. JFET-based Converter Waveforms. When Supply Output (Trace A) Decays, C1 (Trace B) Switches, Allowing Q1 to Oscillate. Resultant Flyback Events at Q1 Drain (Trace C) Restore Supply Output.

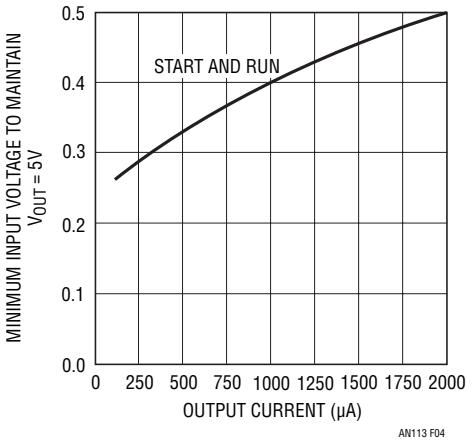

Figure 4. JFET-Based DC/DC Converter Starts and Runs into 100µA Load at V_{IN} = 275mV. Regulation to 2mA Is Possible, Although Required V_{IN} Rises to 500mV.

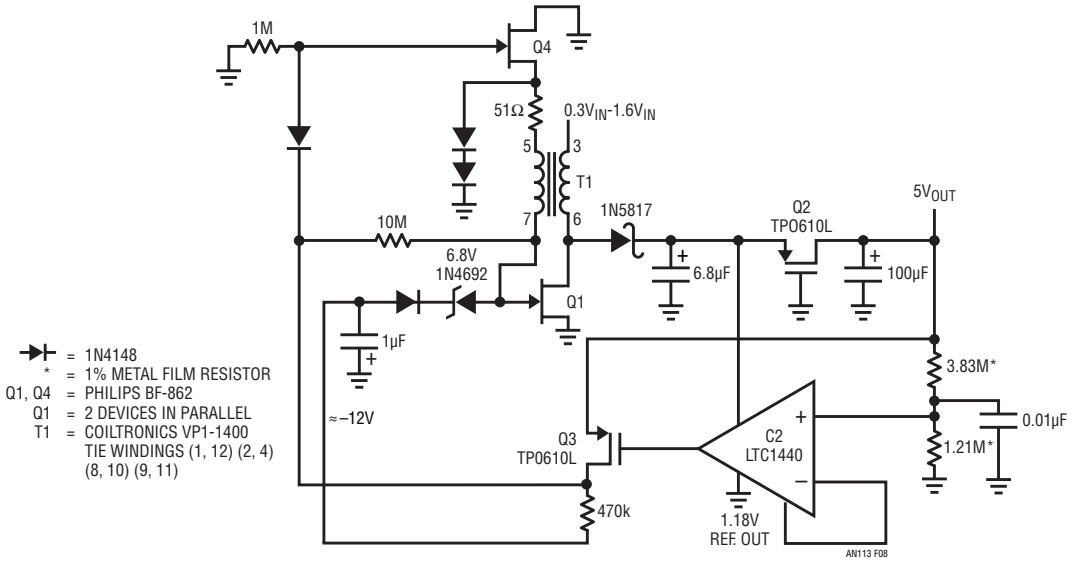

Figure 5. Adding Q3, Q4 and Bootstrapped Negative Bias Generator Reduces Quiescent Current. Comparator Directed Q3 Switches Q4, More Efficiently Controlling Q1's Gate Drive. Q2 and Zener Diode Isolate All Loading During Q1 Start-Up.

bias for Q4 and Q1 is bootstrapped from T1's secondary; the 6.8V zener holds off bias supply loading during initial power application, aiding start-up. Figure 6's plot of minimum input voltage versus output current shows minimal penalty (versus Figure 4's data) imposed by the added quiescent current control circuitry.

Bipolar Transistor-Based 550mV Input DC/DC Converter

Bipolar transistors may be used to obtain higher output currents, although their V_{BE} drop raises input supply requirements to 550mV. Figure 7's curve tracer plot shows base-emitter conduction just beginning at 450mV (25°C) with substantial current flow beyond 500mV. Figure 8's circuit operates similarly to FET-based Figure 2, although the bipolar transistor's normally off characteristic allows more efficient operation. Figure 9's operating waveforms are similar to Figure 3, except the comparator's output state is reversed to accommodate the bipolar transistor. Figure 10's start-run curves show 6mA output current at 550mV input—3 times the FET circuit's capacity. The "run" curve

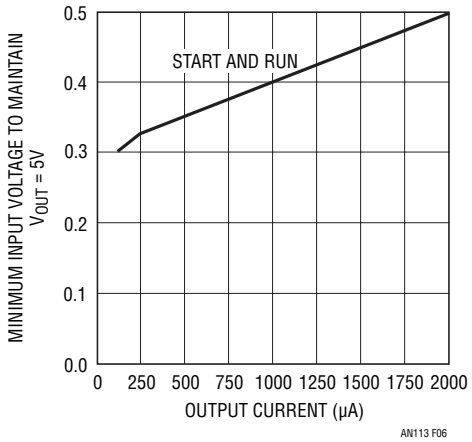

Figure 6. Start/Run Curve for Low Quiescent Current JFET-Based DC/DC Converter. Quiescent Current Control Circuitry Slightly Increases Input Voltage Required to Support Load.

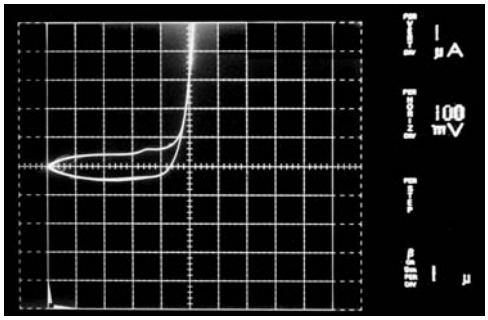

Figure 7. Bipolar Transistor Base Emitter Junction I-V Curve Shows Conduction Beginning at 450 Millivolts (25°C). Characteristic Forms Basis of DC/DC Converter Powered From 550 Millivolts.

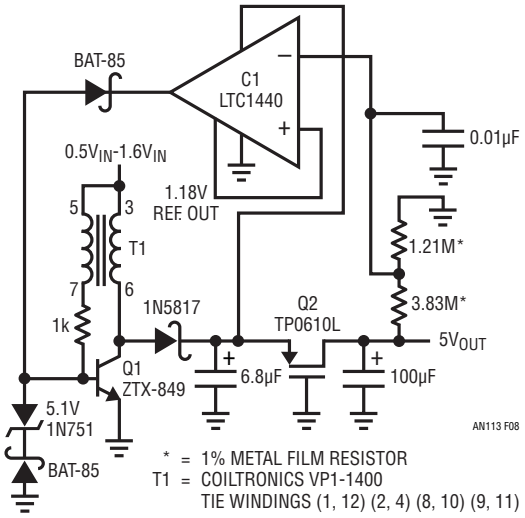

Figure 8. Bipolar Transistor-Based DC/DC Converter Runs From 500 Millivolt (25°C) Input. Q1-T1 Oscillator Output is Rectified and Filtered. Load is Isolated Until Q2's Source Reaches ≈2V, Aiding Start-Up. Comparator Closes Loop Around Oscillator, Controlling Q1's On-Time to Stabilize 5V Output.

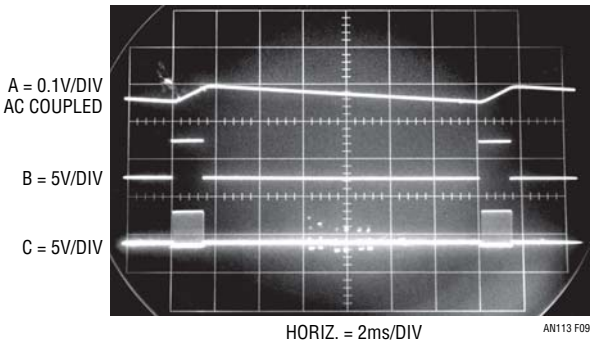

Figure 9. Converter Waveforms. When Output (Trace A) Decays, C1 (Trace B) Switches, Allowing Q1 to Oscillate. Resultant Flyback Events at Q1 Collector (Trace C) Restore Output.

indicates that, once started, the circuit will run at input voltages as low as 300mV depending on loading.

When considering these circuits' extremely low input voltages and output power limits it is worth noting that the transformer specified is a standard product. A transformer specifically optimized for these applications would likely enhance performance.

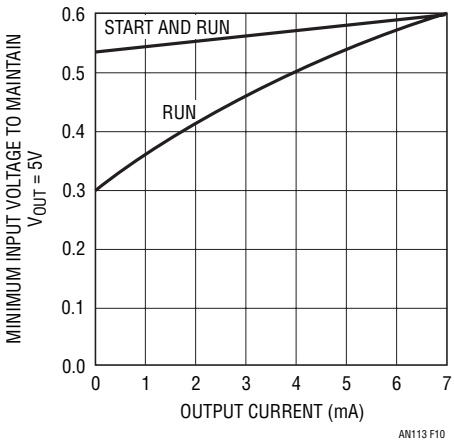

Figure 10. Bipolar Transistor-Based DC/DC Converter Requires ≈550mV (25°C) Input to Start into 0mA to 6mA Loading. Once Running, Converter Maintains Regulation Down to 300mV Inputs for 100µA Load.

5V to 200V Converter for APD Bias

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Avalanche photodiodes (APD) require high voltage bias. Figure 11's design provides 200V from a 5V input. The circuit is a basic inductor flyback boost regulator with a major important deviation. Q1, a high voltage device, has been interposed between the LT1172 switching regulator and the inductor. This permits the regulator to control Q1's high voltage switching without undergoing high voltage stress. Q1, operating as a "cascode" with the LT1172's internal switch, withstands L1's high voltage flyback events.[2] Diodes associated with Q1's source terminal clamp L1 originated spikes arriving via Q1's junction capacitance. The

Note 2. See References 1 (page 8), 2 (Appendix D), and 3.

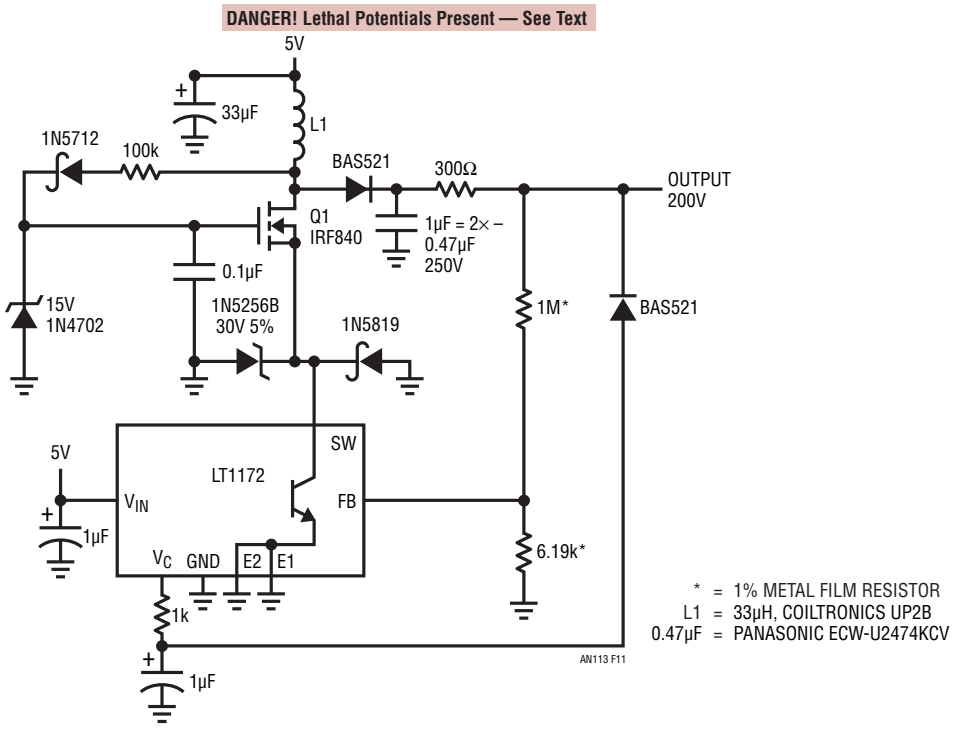

Figure 11. 5V to 200V Output Converter for APD Bias. Cascoded Q1 Switches High Voltage, Allowing Low Voltage Regulator to Control Output. Diode Clamps Protect Regulator from Transient Events; 100k Path Bootstraps Q1's Gate Drive from L1's Flyback Events. Output Connected 300Ω-Diode Combination Provides Short-Circuit Protection.

high voltage is rectified and filtered, forming the circuit's output. Feedback to the regulator stabilizes the loop and the RC at the V_C pin provides frequency compensation. The 100k path from L1 bootstraps Q1's gate drive to about 10V, ensuring saturation.[3] The output connected 300Ω-diode combination provides short-circuit protection by shutting down the LT1172 if the output is accidentally grounded.

Figure 12 shows operating waveforms. Traces A and C are LT1172 switch current and voltage, respectively. Q1's drain is trace B. Current ramp termination results in a high voltage flyback event at Q1's drain. A safely attenuated version of the flyback appears at the LT1172 switch. The sinosoidal signature, due to inductor ring-off between conduction cycles, is harmless.

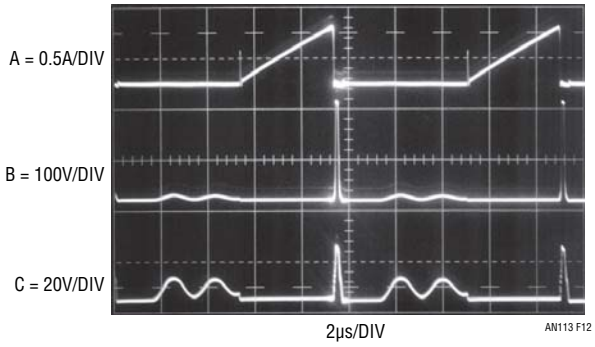

Figure 12. Waveforms for 5V to 200V Converter Include LT1172 Switch Current and Voltage (Traces A and C, Respectively) and Q1's Drain Voltage (Trace B). Current Ramp Termination Results in High Voltage Flyback Event at Q1 Drain. Safely Attenuated Version Appears at LT1172 Switch. Sinosoidal Signature, Due to Inductor Ring-Off Between Current Conduction Cycles, is Harmless. All Traces Intensified Near Center Screen for Photographic Clarity.

Battery Internal Resistance Meter

It is often desirable to determine a battery's internal resistance to evaluate its condition or suitability for an application. Accurate battery resistance determination is complicated by inherent capacitive terms which corrupt results taken with AC-based milliohmmeters operating in the kHz range. Figure 13, a very simplistic battery model, shows a resistive divider with a partial shunt capacitive term. This capacitive term introduces error in AC-based measurement. Additionally, the battery's unloaded internal resistance may significantly differ from its loaded value. As such, a realistic determination of internal resistance must be made under loaded conditions at or near DC.

Note 3. This circuit is not a fresh contribution but, rather, a belated *mea culpa*. The original version suffered temperature dependent output error due to its gate bias bootstrap scheme. See Reference 4.

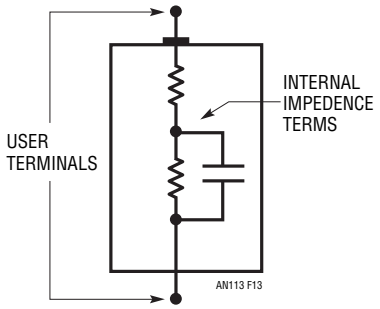

Figure 13. Simplistic Model Shows Battery Impedance Terms Including Resistive and Capacitive Elements. Capacitive Component Corrupts AC-Based Measurement Attempts to Determine Internal DC Resistance. More Realistic Results Occur if Battery Voltage Drop Is Measured Under Known Load.

Figure 14's circuit meets these requirements, permitting accurate internal resistance determination of batteries up to 13V over a range of 0.001Ω to 1.000Ω. A1, Q1 and associated components form a closed loop current sink which loads the battery via Q1's drain. The 1N5821 provides reverse battery protection. The voltage across the 0.1Ω resistor, and hence the battery load, is determined by A1's "+" input voltage. This potential is alternately switched, via S1, between 0.110V and 0.010V derived from the 2.5V reference driven resistor string. S1's 0.5Hz square wave switching drive comes from the CD4040 frequency divider. The result of this action is a 100mA biased 1A 0.5Hz square wave load applied to the battery. The battery's internal resistance causes a 0.5Hz amplitude modulated square wave to appear at the Kelvin-sensed S2-S3-A2 synchronous demodulator. The demodulator DC output is buffered by chopper stabilized A2 which provides the circuit output. A2's internal 1kHz clock, level shifted by Q2, drives the CD4040 frequency divider. One divider output supplies the 0.5Hz square wave; a second 500Hz output activates a charge pump, providing a –7V potential to A2. This arrangement allows A2 output swing to zero volts.

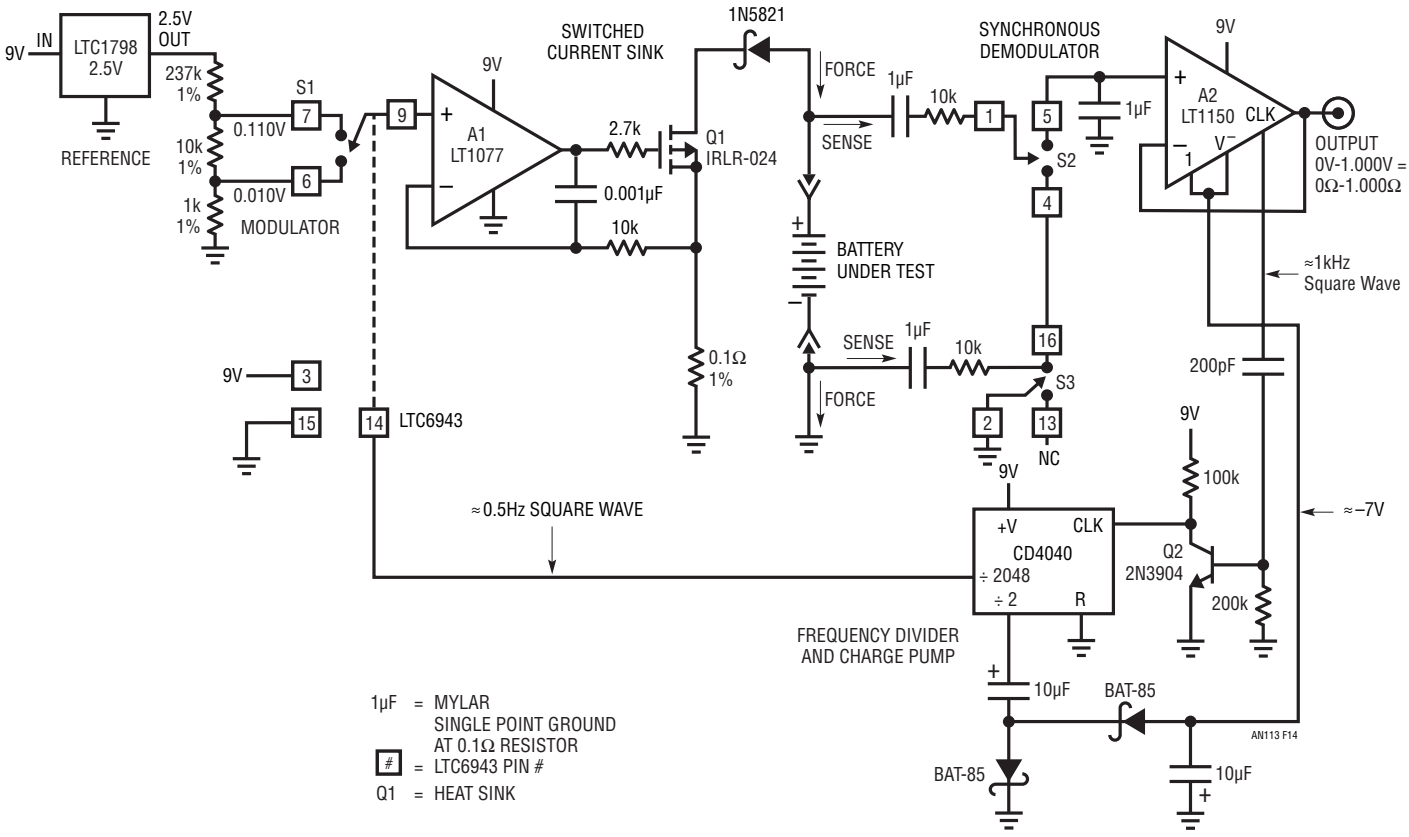

Figure 14. Battery Internal Resistance Is Determined by Repetitively Stepping Calibrated Discharge Current and Reading Resultant Voltage Drop. S1-Based Modulator, Clocked From Frequency Divider, Combines with A1-Q1 Switched Current Sink to Generate Stepped, 1 Ampere Battery Discharge Cycles. S2-S3-A2 Synchronous Demodulator Extracts Modulated Voltage Drop Information, Provides DC Output Calibrated in Ohms.

The circuit pulls 230µA from its 9V battery power supply, permitting about 3000 hours battery life. Other specifications include operation down to 4V with less than 1mV (0.001Ω) output variation, 3% accuracy and battery-under-test range of 0.9V to 13V. Finally, note that battery discharge current and repetition rate are easily varied from the values given, permitting observation of battery resistance under a variety of conditions.

Floating Output, Variable Potential Battery Simulator

Battery stack voltage monitor development (Reference 5) is aided by a floating, variable potential battery simulator. This capability permits monitor accuracy verification over a wide range of battery voltage. The floating battery simulator is substituted for a cell in the stack and any desired voltage directly dialed out. Figure 15's circuit is simply a battery powered follower (A1) with current boosted (A2) output. The LT1021 reference and high resolution potentiometric divider specified permits accurate output setting within 1mV. The composite amplifier unloads the divider and drives a 680µF capacitor to approximate a battery. Diodes preclude reverse biasing the output capacitor during supply sequencing and the 1µF - 150k combination provides stable loop compensation. Figure 16 depicts loop response to an input step; no overshoot or untoward dynamics occur despite A2's huge capacitive load. The battery monitor

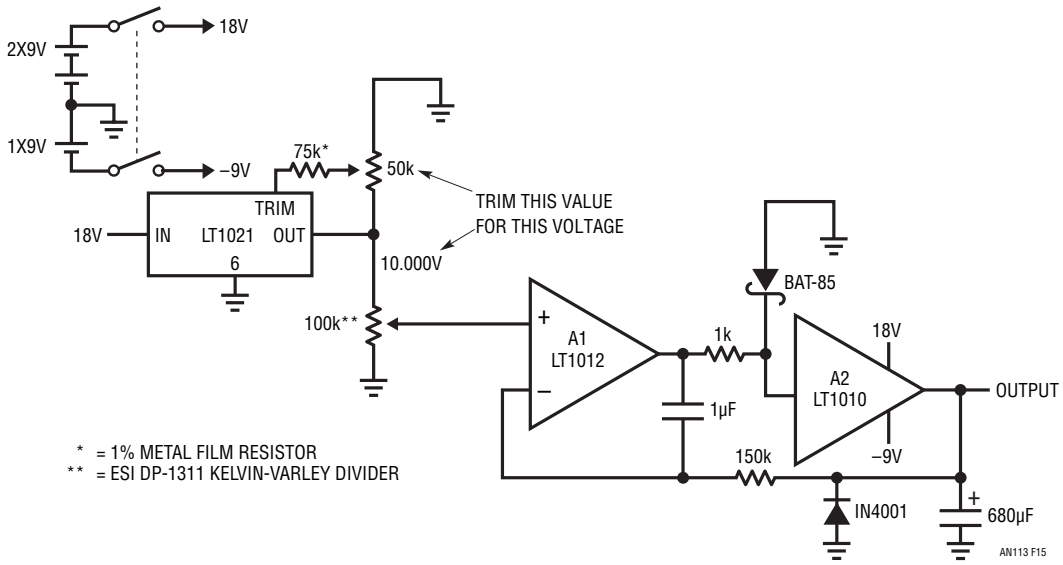

Figure 15. Battery Simulator Has Floating Output Settable within 1mV. A1 Unloads Kelvin-Varley Divider; A2 Buffers Capacitive Load.

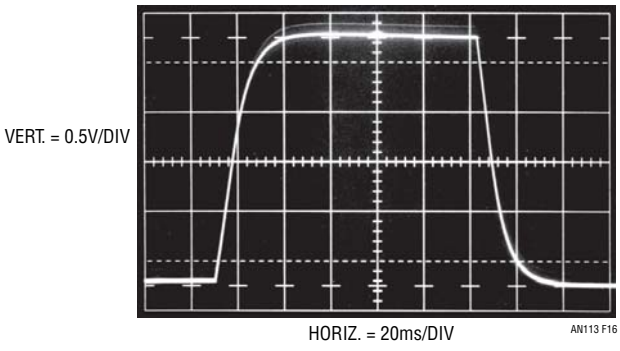

Figure 16. 150k-1µF Compensation Network Provides Clean Response Despite 680µF Output Capacitor.

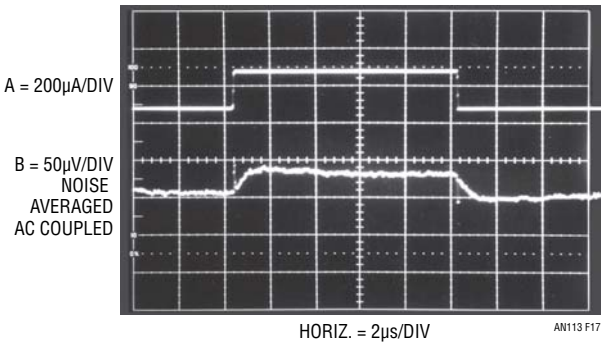

Figure 17. Battery Simulator Output (Trace B) Responds to Trace A's Monitor Current Pulse. Closed Loop Control and 680µF Capacitor Maintain Simulator Output within 30µV. Noise Averaged, 50µV/Division Sensitivity Is Required to Resolve Response.

determines battery voltage by injecting current into the battery and measuring resultant clamp voltage (again, see Reference 5). Figure 17 shows battery simulator response (trace B) to trace A's monitor current pulse into the output. Closed loop control and the 680µF capacitor limit simulator output excursion within 30µV. This error is so small that noise averaging techniques and a high gain oscilloscope preamplifier are required to resolve it.[4]

40nV$_{P-P}$ Noise, 0.05µV/°C Drift, Chopped FET Amplifier

Figure 18's circuit combines the LTC6241's rail-to-rail performance with a pair of extremely low noise JFETs configured in a chopper-based carrier modulation scheme to achieve extraordinarily low noise and DC drift. This circuit's performance suits demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

The LTC1799's output is divided down to form a 2-phase 925Hz square wave clock. This frequency, harmonically unrelated to 60Hz, provides excellent immunity to harmonic beating or mixing effects which could cause instabilities. S1 and S2 receive complementary drive, causing the FET-A1 based stage to see a chopped version of the input voltage. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to DC output amplifier A2. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. The AC coupled input stage's DC errors do not affect overall circuit characteristics, resulting in the extremely low offset and drift noted.

Note 4. This may be viewed as a historic event in some thinly populated circles. Figure 17 marks the author's first published use of a digital oscilloscope (Tektronix 7603/7D20), updating him to the 1980s.

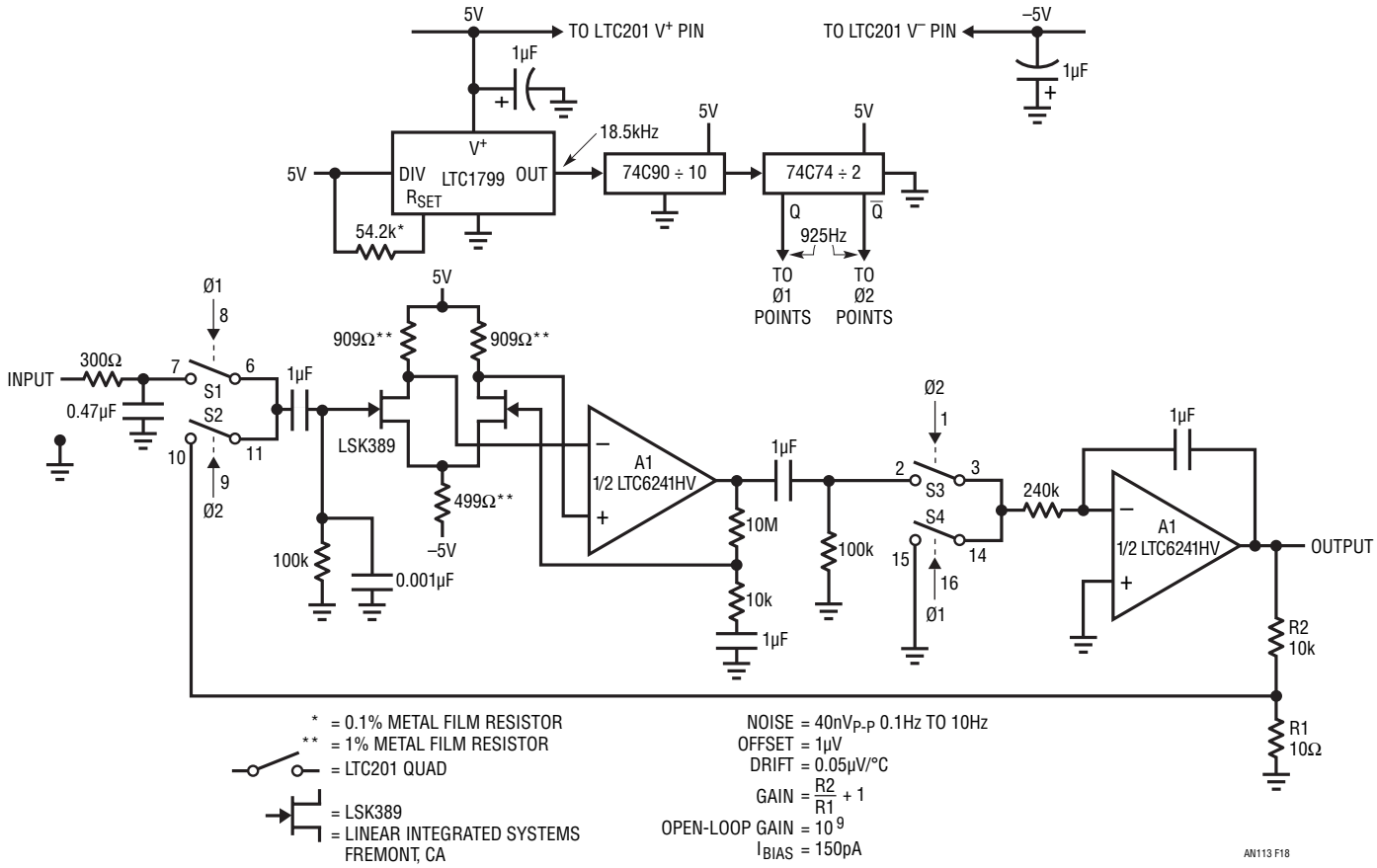

Figure 18. Chopped FET Amplifier Has 40nV$_{P-P}$ Noise and 0.05µV/°C Drift. DC Input Is Carrier Modulated, Amplified by A1, Demodulated to DC and Fed Back From A2. 925Hz Carrier Clock Prevents Interaction with 60Hz Line Originated Components.

Figure 19, measured over a 50 second interval, shows 40nV$_{P-P}$ noise in a 0.1Hz to 10Hz bandwidth. This is spectacularly low noise for a JFET-based design and is directly attributable to input pair area and current density.

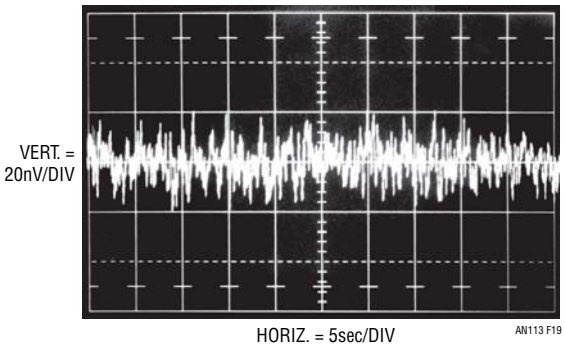

Figure 19. Amplifier 0.1Hz to 10Hz Noise Measures 40nV$_{P-P}$ in 50 Second Sample Period.

Wideband, Chopper Stabilized FET Amplifier

The previous circuit's bandwidth is limited because the chopping occurs within the signal path. Figure 20's circuit circumvents this restriction by placing the stabilizing element in parallel with the signal path. This maintains DC performance although noise triples to 125nV in a 0.1Hz to 10Hz bandpass.

FET pair Q1 differentially feeds A2 to form a simple low noise op amp. Feedback, provided by R1 and R2, sets closed loop gain (in this case 1000) in the usual fashion. Although Q1 has extraordinarily low noise characteristics, its offset and drift are relatively high. A1, a chopper stabilized amplifier, corrects these deficiencies. It does this by measuring the difference between the amplifier's inputs and adjusting Q1A's channel current to minimize the difference. Q1's drain values ensure that A1 will be able to capture the

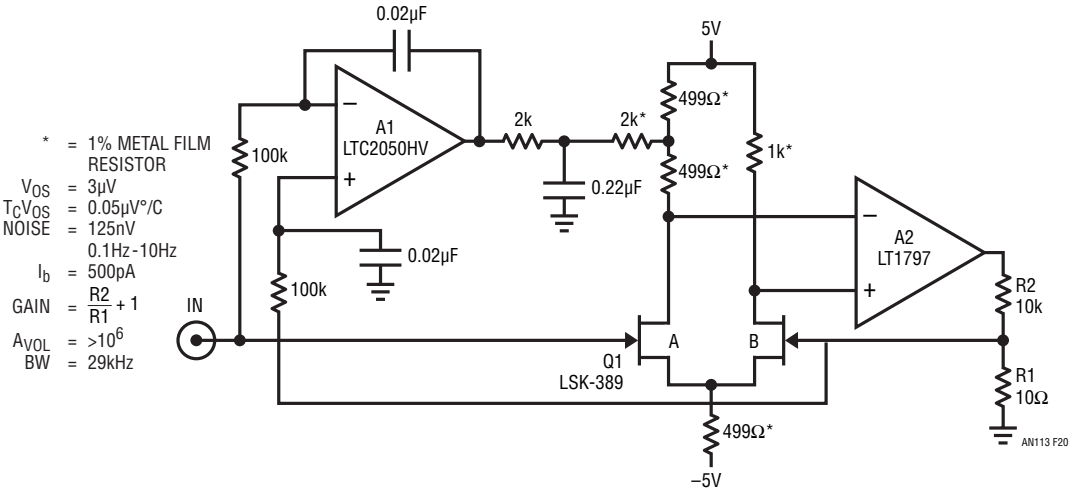

Figure 20. Placing Stabilizing Amplifier Outside Signal Path Permits Bandwidth Increase over Previous Circuit. Noise Triples to 125nV in 0.1Hz to 10Hz Bandpass.

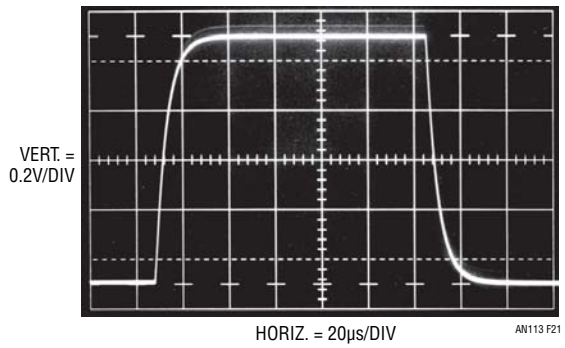

Figure 21. Figure 20 Responds to a 1mV Input. 12µs Rise Time Indicates 29kHz Bandwidth at A = 1000.

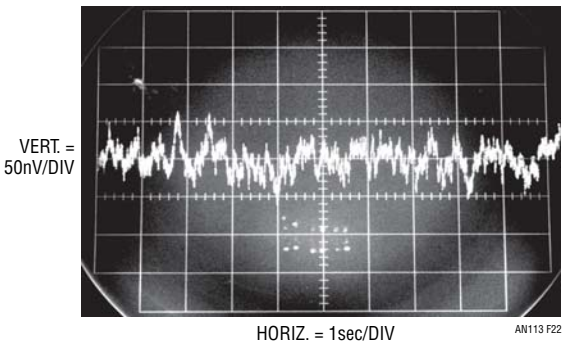

Figure 22. Chopper Stabilized FET Pair Noise Measures 125nV in 0.1Hz to 10Hz Bandpass.

offset. A1 supplies whatever current is required to Q1A's channel to force offset within 5µV. Additionally, A1's low bias current does not appreciably add to the overall 500pA amplifier bias current. As shown, the amplifier is set up for a noninverting gain of 1000, although other gains and inverting operation are possible.

Placing the offset correction in parallel with the signal path permits high bandwidth. Figure 21 shows response to a 1mV input. The 12µs risetime indicates 29kHz bandwidth at A = 1000.

Figure 22's photo measures noise in a 0.1Hz to 10Hz bandwidth. The performance obtained is almost 6 times better than any monolithic chopper stabilized amplifier, while retaining low offset and drift.

Submicroampere RMS Current Measurement for Quartz Crystals

Quartz crystal RMS operating current is critical to long-term stability, temperature coefficient and reliability. Accurate determination of RMS crystal current, especially in micropower types, is complicated by the necessity to minimize introduced parasitics, particularly capacitance, which corrupt crystal operation. Figure 23's high gain, low noise amplifier combines with a commercially available

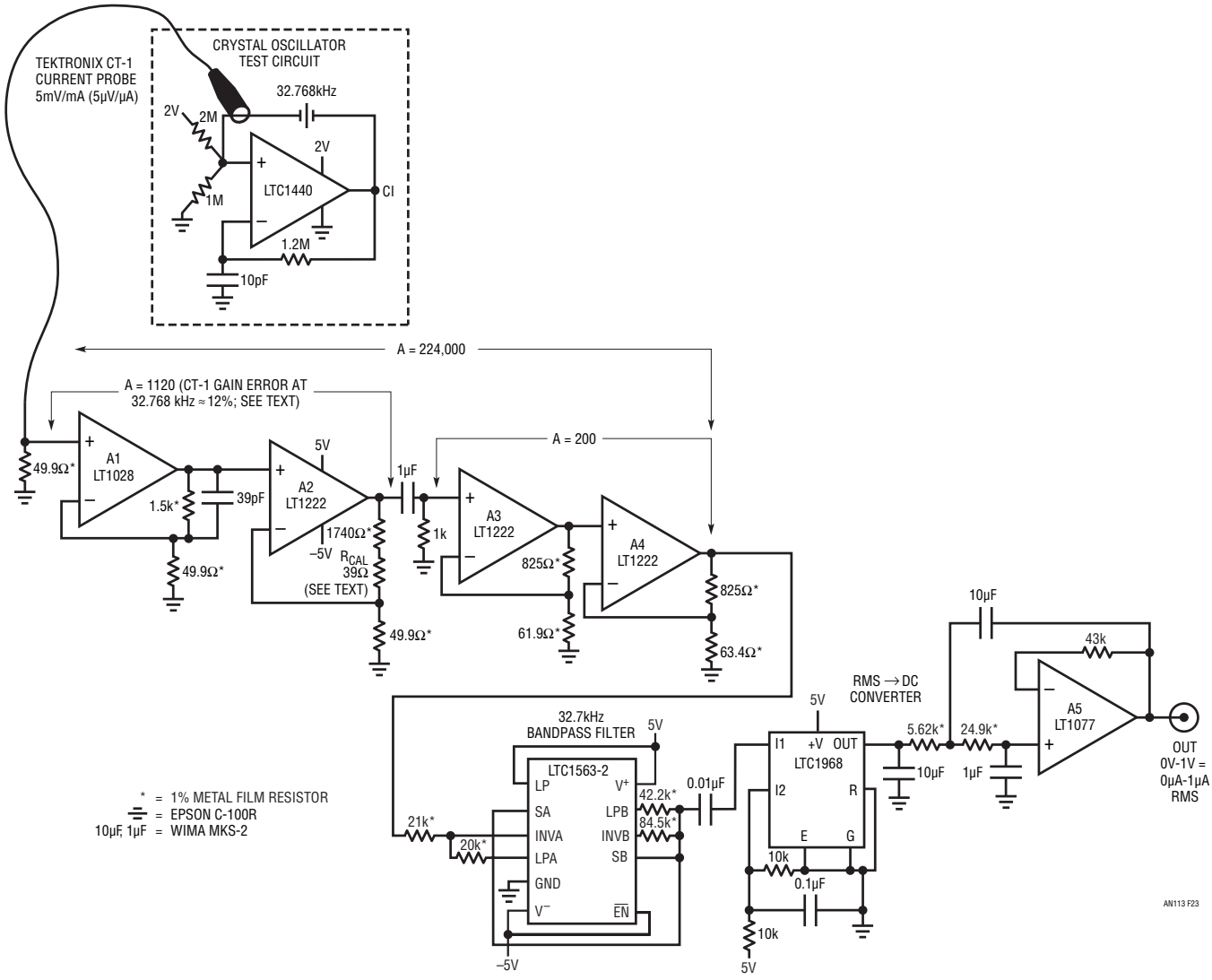

Figure 23. A1 to A4 Furnish Gain of >200,000 to Current Probe, Permitting Submicroamp Crystal Current Measurement. LTC1563-2 Bandpass Filter Smooths Residual Noise While Providing Unity Gain at 32.768kHz. LTC1968 Supplies RMS Calibrated Output.

closed core current probe to permit the measurement. An RMS-to-DC converter supplies the RMS value. The quartz crystal test circuit shown in dashed lines exemplifies a typical measurement situation. The Tektronix CT-1 current probe monitors crystal current while introducing minimal parasitic loading. The probe's 50Ω terminated output feeds A1. A1 and A2 take a closed loop gain of 1120; excess gain over a nominal gain of 1000 corrects for the CT-1's 12% low frequency gain error at 32.768kHz.[5] A3 and A4 contribute a gain of 200, resulting in total amplifier gain of 224,000. This figure results in a 1V/μA scale factor at A4 referred to the gain corrected CT-1's output. A4's LTC1563-2 bandpass filtered output feeds an LTC1968-A5 based RMS→DC converter which provides the circuits output. The signal processing path constitutes an extremely narrow band amplifier tuned to the crystal's frequency. Figure 24 shows typical circuit waveforms. Crystal drive, taken at C1's output (trace A), causes a 530nA RMS crystal current which is represented at A4's output (trace B) and the RMS→DC converter input (trace C). Peaking visible in trace B's unfiltered presentation derives from parasitic paths shunting the crystal.

Typical circuit accuracy is 5%. Uncertainty terms include the transformer's tolerances, its ≈1.5pF loading and resistor/RMS→DC converter error. Calibrating the circuit reduces error to less than 1%. Calibration involves driving the transformer with 1μA at 32.7kHz. This is facilitated by biasing a 100k, 0.1% resistor with an oscillator set at 0.100V output. The output voltage should be verified with an RMS voltmeter having appropriate accuracy (see Reference 8's Appendix B). Figure 23 is calibrated by padding A2's gain with a small resistive correction, typically 39Ω.

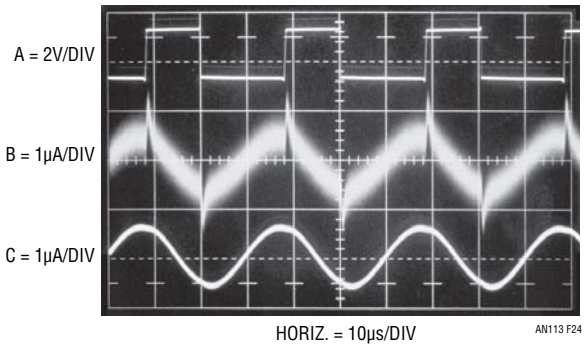

Figure 24. C1's 32.768kHz Output (Trace A) and Crystal Current Monitored at A4 Output (Trace B). RMS Converter Input Is Trace C. Peaks in Trace B's Unfiltered Waveform Derive From Inherent and Parasitic Paths Shunting Crystal.

Direct Reading Quartz Crystal-Based Remote Thermometer

Although quartz crystals have been used as temperature sensors (see References 7 and 10) there has been almost no adaptation of this technology. The primary impediment has been lack of standard product quartz crystal temperature sensors. The advantages of quartz-based temperature sensing include nearly purely digital signal conditioning, good stability and a direct, noise immune digital output ideally suited to remote sensing.

Figure 25 utilizes an economical, commercially available (Reference 9) quartz temperature sensor in a direct reading thermometer scheme suited to remote data collection. An LTC485 transceiver, set up in transmit mode, forms a quartz-based, Pierce class oscillator. The transceiver's differential line driving outputs provide frequency coded temperature data to a 1000 foot cable run. A second RS485 transceiver differentially receives the data, presenting a single ended output to the PIC-16F73 processor. The processor converts the frequency coded temperature data to its °C equivalent, which appears on the display. Figure 26 is a software listing of the processor's program.[6] Accuracy over a sensed –40°C to 85°C range is about 2%.

Note 5. The validity of this gain error correction at one sinusoidal frequency –32.768kHz—was investigated with a 7-sample group of Tektronix CT-1s. Device outputs were collectively within 0.5% of 12% down for a 1μA 32.768kHz sinusoidal input current. Although this tends to support the measurement scheme, it is worth noting that these results are as measured. Tektronix does not guarantee performance below the specified –3dB 25kHz low frequency roll-off.

Note 6. Mark Thoren of LTC designed the processor-based circuitry and authored Figure 26's software.

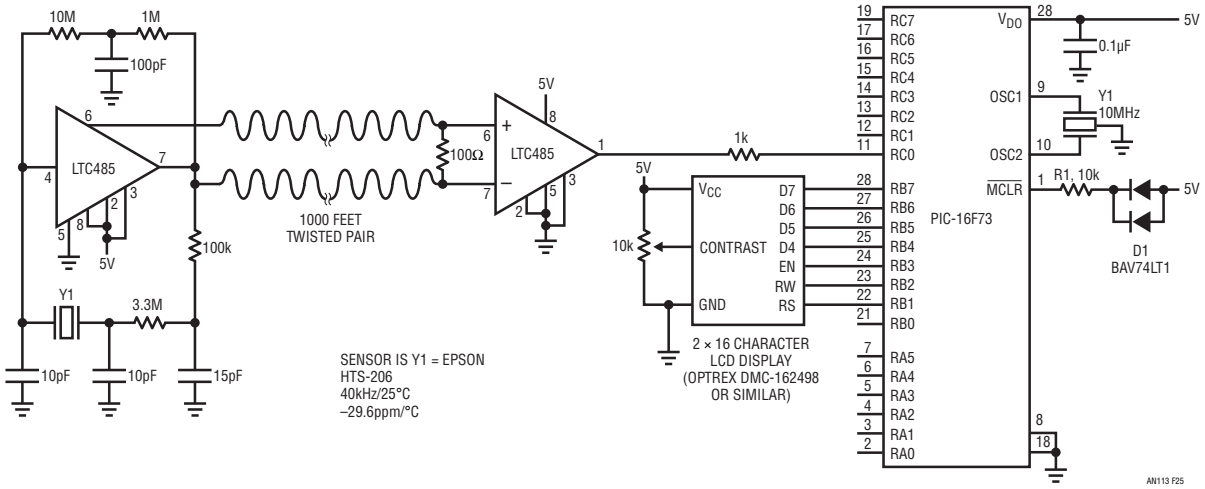

Figure 25. Quartz Crystal-Based Remote Thermometer Has 2% Accuracy over –40°C to 85°C Sensed Range, Drives 1000ft Cable. RS-485 Transceiver Oscillates at Y1 Quartz Sensor Determined Frequency and Drives Cable. Second Transceiver Receives Data and Feeds Processor. Display Reads Directly in °C.

```
/*
Thermometer based on Epson HT206 temperature sensing crystal.
Output is to a standard Epson HD447980 based alphanumeric
LCD display. LCD driver functions are part of compiler library

Written for CSS compiler version 3.182

*/

#include <16F73.h>
#device adc=8
#fuses NOWDT, HS, PUT, NOPROTECT, NOBROWNOUT
#use delay (clock=10000000) // Tell compiler how fast we're going
#use rs232(baud=9600, parity=N, xmit=PIN_C6, rcv=PIN_C7, bits=8)
#include "lcd.c" // LCD driver functions

void main( )
{
    int16 temp;
    unsigned int16 f;
    setup_adc_ports(NO_ANALOGS);
    setup_adc(ADC_OFF);
    setup_spi (FALSE);
    setup_counters (RTCC_INTERNAL, RTCC_DIV_1);
    setup_timer_1 (T1_EXTERNAL|T1_DIV_BV_1);
    setup_timer_2 (T2_DISABLED, 0, 1);
    lcd_init( ); // Initialize LCD

while(1)
    (
    set_timer1(0);                                  //  Reset counter
    setup_timer_1(T1_EXTERNAL|T1_DIV_BY_1);         //  Turn on counter
    delay_ms(845);                                  //  0.845412 is the magic time to count
    delay_us(412);                                  //  -it gives 1 less plus per degree C
    setup_timer_1(T1_DISABLED);                     //  turn off counter
    f = get_timer1();                               //  Read result
    temp = 33770 – f + 25;                          //  Convert to temperature

    //**  At this point 'f' is the temperature in degrees C              **//
    //**  For this experiment, dump to standard HD44780 type LCD display **//

    lcd_putc('\f');                                 //  Clear screen
    lcd_gotoxy(1, 1);                               //  Goto home position
    printf(lcd_putc, "%ld", temp);                  //  And display result
    }
}
```

Figure 26. Software Listing for PIC Processor Program. Code Converts Frequency to °C Equivalent, Drives Display.

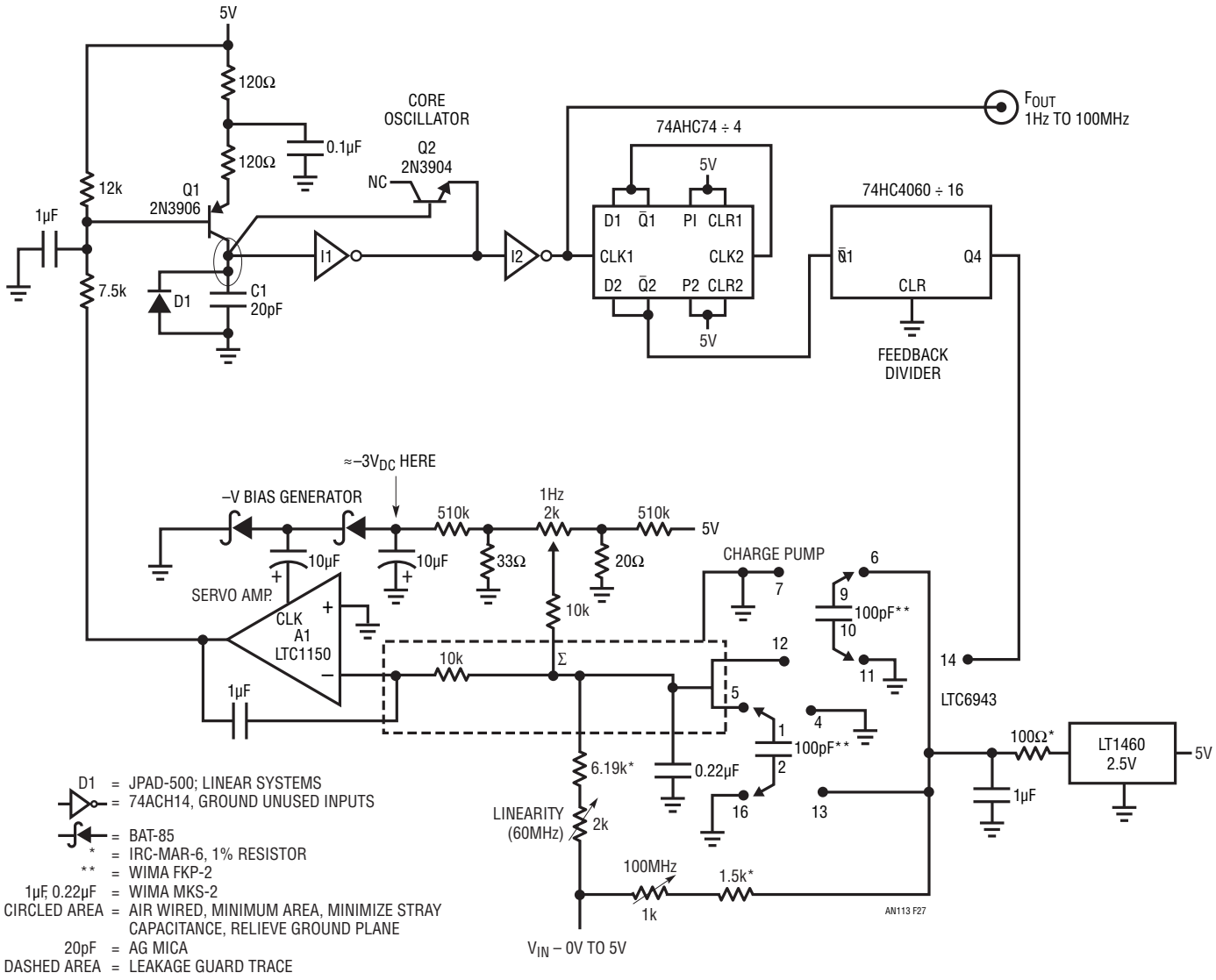

Figure 27. 1Hz to 100MHz V→F Converter Has 160dB Dynamic Range, Runs From 5V Supply. Input Biased Servo Amplifier Controls Core Oscillator, Stabilizing Circuit's Operating Point. Wide Range Operation Derives From Core Oscillator Characteristics, Divider/Charge Pump-Based Feedback and A1's Low DC Input Errors.

1Hz-100MHz V→F Converter

Figure 27's circuit achieves a wider dynamic range and higher output frequency than any commercially available voltage to frequency (V→F) converter. Its 100MHz full-scale output (10% overrange to 110MHz is provided) is at least ten times faster than available units. The circuit's 160dB dynamic range (8 decades) allows continuous operation down to 1Hz. Additional specifications include 0.1% linearity, 250ppm/°C gain temperature coefficient, 1Hz/°C zero shift, 0.1% frequency shift for V_{SUPPLY} = 5V ± 10% and a 0V to 5V input range. A single 5V supply powers the circuit.[7]

A1, a chopper stabilized amplifier, servo biases a crude but wide range core oscillator in Figure 27. The core oscillator drives a charge pump via digital dividers. The averaged difference between the charge pump's output and the circuit's input appears at a summing node (Σ) and biases A1, closing a control loop around the wide range core oscillator. The circuit's extraordinary dynamic range and high speed derive from core oscillator characteristics, divider/charge pump-based feedback and A1's low DC input errors. A1 and the LTC6943-based charge pump stabilize circuit operating point, contributing high linearity and low drift. A1's low offset drift allows the circuit's 50nV/Hz gain slope, permitting operation down to 1Hz at 25°C.

The positive input voltage causes A1 to swing negatively, biasing Q1. Q1's resultant collector current ramps C1 (trace A, Figure 28) until Schmitt trigger inverter I1's output (trace B) goes low, discharging C1 via Q2. C1's discharge resets I1's output to its high state, Q2 goes off and the ramp-and-reset action continues. D1's leakage dominates all parasitic currents in the core oscillator, ensuring operation down to 1Hz. The ÷64 divider chain's output clocks the LTC6943-based charge pump. The charge pump's two sections operate out-of-phase, resulting in charge transfer at each clock transition. Charge pump stability is primarily determined by the LT1460 2.5V reference, the switches low charge injection and the 100pF capacitors. The 0.22µF capacitor averages the pumping action to DC. The averaged difference between the input derived current and the charge pump feedback signal is amplified by A1, which biases Q1 to control circuit operating point. Core oscillator nonlinearity and drift are compensated by A1's servo action, resulting in the high linearity and low drift previously noted. A1's 1µF capacitor provides stable loop compensation. Figure 29 shows loop response (trace B) to an input step (trace A) is well controlled.

Some special techniques enable this circuit to achieve its specifications. D1's leakage current dominates all parasitic currents at I1's input; hence Q1 must always source current to sustain oscillation, assuring operation down to 1Hz. The 100MHz full-scale frequency sets stringent restrictions on core oscillator cycle time. Only 10ns is available for a

Note 7. Reference 12 (1986) contains a circuit with comparable specifications although considerably more complex than the one presented here. The advent of high speed CMOS logic permitted replacing the earlier designs ECL elements, facilitating a dramatic decrease in complexity. Comparing the designs permits viewing the impact a technology shift can have in realizing a circuit function. In this case, the effect is pervasive, directly or indirectly influencing nearly every aspect of circuit operation. While circuit architecture is consistent, this incarnation is substantially and favorably altered.

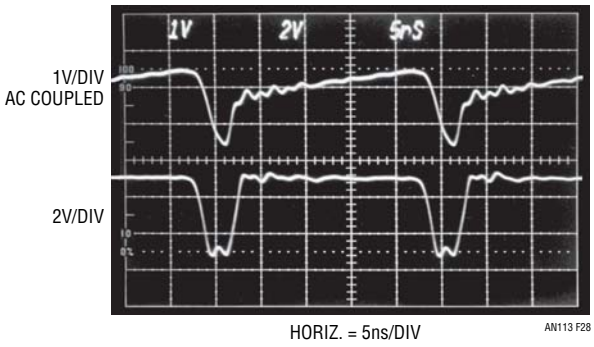

Figure 28. V→F Operation at 40MHz. Core Oscillator Waveforms Viewed in 670MHz Real Time Bandwidth Include Q1 Collector (Trace A) and Q2 Emitter (Trace B). Ramp-and-Reset Operating Characteristic Is Apparent; Reset Duration of 6ns Permits 100MHz Repetition Rate.

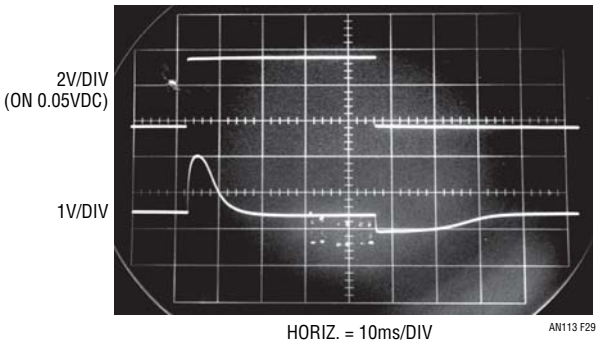

Figure 29. Response (Trace B) to an Input Step (Trace A) Shows 30ms Settling Time at Summing Junction (Σ). A1's 1µF Capacitor Shapes Response, Stabilizing Feedback Loop. Clamped Response on Negative Going Input Step is Due to Summing Junction Limiting.

complete ramp-and-reset sequence. The ultimate speed limitation is the reset interval. Figure 28, trace B, shows a 6ns interval, comfortably within the 10ns limit.

A scaled resistive path from the input to the charge pump corrects small nonlinearities due to residual charge injection. This input derived correction is effective because the charge injections effect varies directly with input determined frequency.

Prototype and small lot construction may proceed using the schematic and its notes, but component selection should be considered for volume production. Figure 30 lists applicable components and their selection targets.

To calibrate this circuit apply 5.000V and trim the 100MHz adjustment for a 100.0MHz output. Next, ground the input and adjust the 1Hz trim for 1Hz output. Allow for long settling time, as charge pump update rate at this frequency is once every 32 seconds. Note that this trim accommodates either offset polarity because of the –V bias derived from A1's clock output. Finally, set the 60MHz adjustment for 60.0MHz with 3.000V_{IN}. Repeat these adjustments until all three points are fixed.

Delayed Pulse Generator with Variable Time Phase, Low Jitter Trigger Output

Fast circuitry often requires a pulse generator that also supplies a variable time phase trigger output. It is desirable that the main output pulse occurrence be continuously settable from before to after the trigger output with low time jitter. Figure 31's circuit produces a 360ps risetime output pulse with trigger output time phase variable from –30ns to 100ns. Jitter is 40ps.

Q1 and Q2 form a current source that charges the 1000pF capacitor. When the LTC1799 clock is high (trace A, Figure 32) both Q3 and Q4 are on. The current source is off and A2's output (trace B) is at ground. C1's latch input prevents it from responding and its output remains high. When the clock goes low, C1's latch input is disabled and its output drops low. The Q3 and Q4 collectors lift and Q2 comes on, delivering constant current to the 1000pF capacitor. The resulting linear ramp at A2 (trace B) is applied to bounded current summing amplifiers A3 and A4. Both amplifiers compare ramp induced current with fixed, opposite polarity currents derived from A1 – Q6. A1-Q6, in turn, is referred to the +5 supply rail which also sets Q1-Q2 current and hence, ramp slope. This ratiometric connection promotes supply rejection. When A4 and A3 (traces C and F, respectively) come out of diode bound and cross zero, comparators C2 and C1 (traces D and G, respectively) are heavily overdriven and switch rapidly. C2's output path includes components which form trace E's trigger output pulse. C1 triggers output pulse generator Q5, operating in avalanche mode (trace H).[8]

The "delay adjust" control sets the ramp amplitude that A3-C1 switches the main output at, providing the desired variable time phase with respect to the A4-C2 controlled trigger output. Time jitter between C1 and C2 outputs is minimized because A3 and A4 effectively multiply ramp transition rate as their outputs enter the active region, provide gain and cross zero.

Note 8. Avalanche mode pulse generation is a subtle, arcane technique requiring extensive discussion. The text's cavalier treatment is deliberately brief in order to maintain focus on this circuit's low timing jitter characteristics. More studious coverage can be found in References 13-22.

COMPONENT	SELECTION PARAMETER (25°C)	TYPICAL YIELD (%)
Q1	I_{CER} < 20pA at 3V	90
Q2	I_{EBO} < 20pA at 3V	90
D1	I_{REV} < 500pA, > 75pA at 3V	80
I1	I_{IN} < 25pA	80
A1	I_B < 5pA at V_{SUPPLY} = 5V	90
74ACH74	Operate with 3.6nS Wide (50% Point) Input Pulse	80

Figure 30. Selection Criteria for Components Ensure V→F Performance. First Five Entries Enhance Operation Below 100Hz. Last Entry Assures Reliable Feedback Divider Operation.

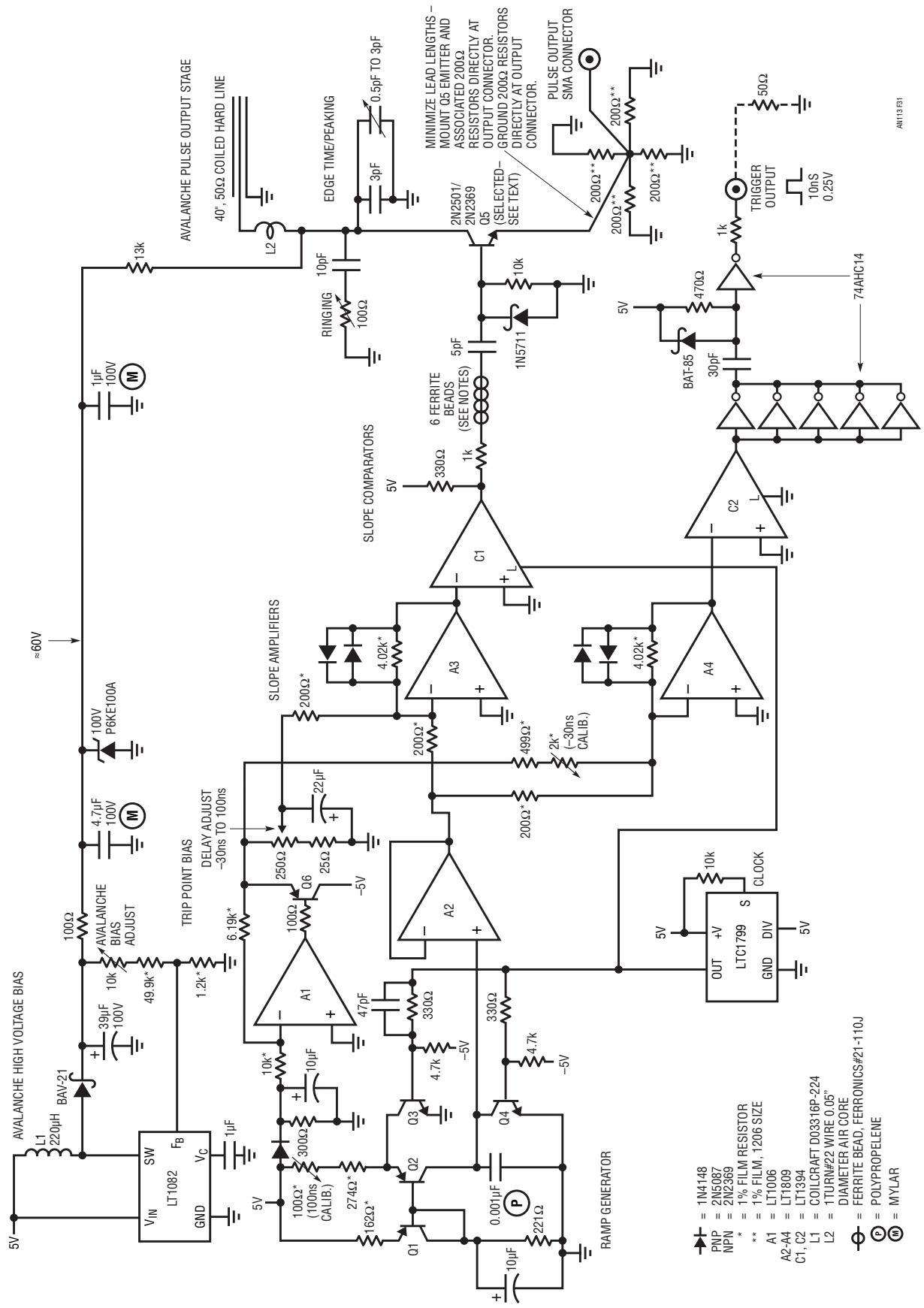

Figure 31. Pulse Generator Output Time Phase Varies –30ns to 100ns with Respect to Trigger Output; Jitter Is 40ps. Clocked Ramp at A2 Produces Variable (A3-C1) and Fixed (A4-C2) Delays Driving Pulse and Trigger Outputs, Respectively. A3-A4 Provide Gain to Comparators at Trip Point, Minimizing Time Jitter Between Outputs.

The A3-A4 amplifier gain is the key to low jitter between C1 and C2's switching times. The amplifiers augment the comparator's relatively low gain, promoting decisive switching despite the ramp input. Figure 33 shows A4 (trace A)-C2 (trace B) response to the ramp crossing the trip point. As the ramp nears the trip point A4 comes out of bound, providing an amplified version of the ramp's transition rate to C2. C2 responds by switching decisively 6ns after A4 crosses zero volts at center screen. A3-C1 waveforms are identical. Figure 34, Q5's pulse output, taken with the oscilloscope synchronized to the trigger output, shows 40ps jitter in a 3.9GHz sampled bandpass.

Circuit calibration is accomplished by first adjusting the "-30ns cal" so the main pulse output occurs 30ns before the trigger output with the "Delay Adjust" set to minimum. Next, with the "Delay Adjust" set to maximum, trim the "100ns cal" so the main pulse output occurs 100ns after the trigger output. Slight interaction between the 30ns and 100ns trims may require repeating their adjustments until both points are calibrated. As mentioned, the avalanche output stage is illustrative only and not detailed in this discussion. Its optimization and calibration are covered in Reference 13.

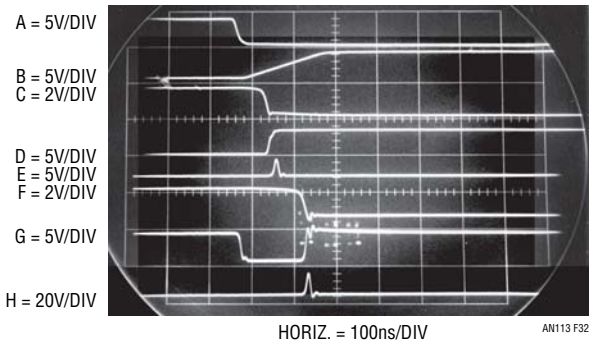

Figure 32. Low Jitter Delayed Pulser Waveforms Include Clock (Trace A), A2 Ramp (B), A4 (C), C2 (D), Trigger Output (E), A3 (F), C1 (G) and Delayed Output Pulse (H). Trigger-to-Output Pulse Delay Is Continuously Variable From –30ns to 100ns.

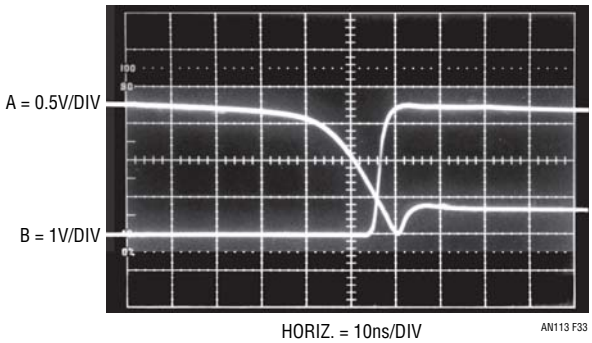

Figure 33. A4 (Trace A) - C2 (Trace B) Response to A2's Ramp Crossing Trip Point. C2 Goes High 6ns after A4 Crosses Zero (Center Screen). A3-C1 Waveforms Are Identical.

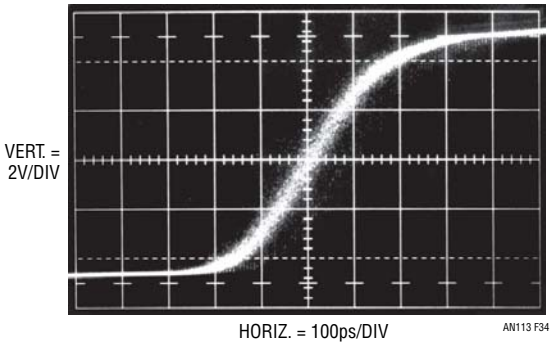

Figure 34. Main Pulse Output Synchronized to Trigger Output Shows 40ps Jitter in 3.9GHz. Sampled Bandpass.

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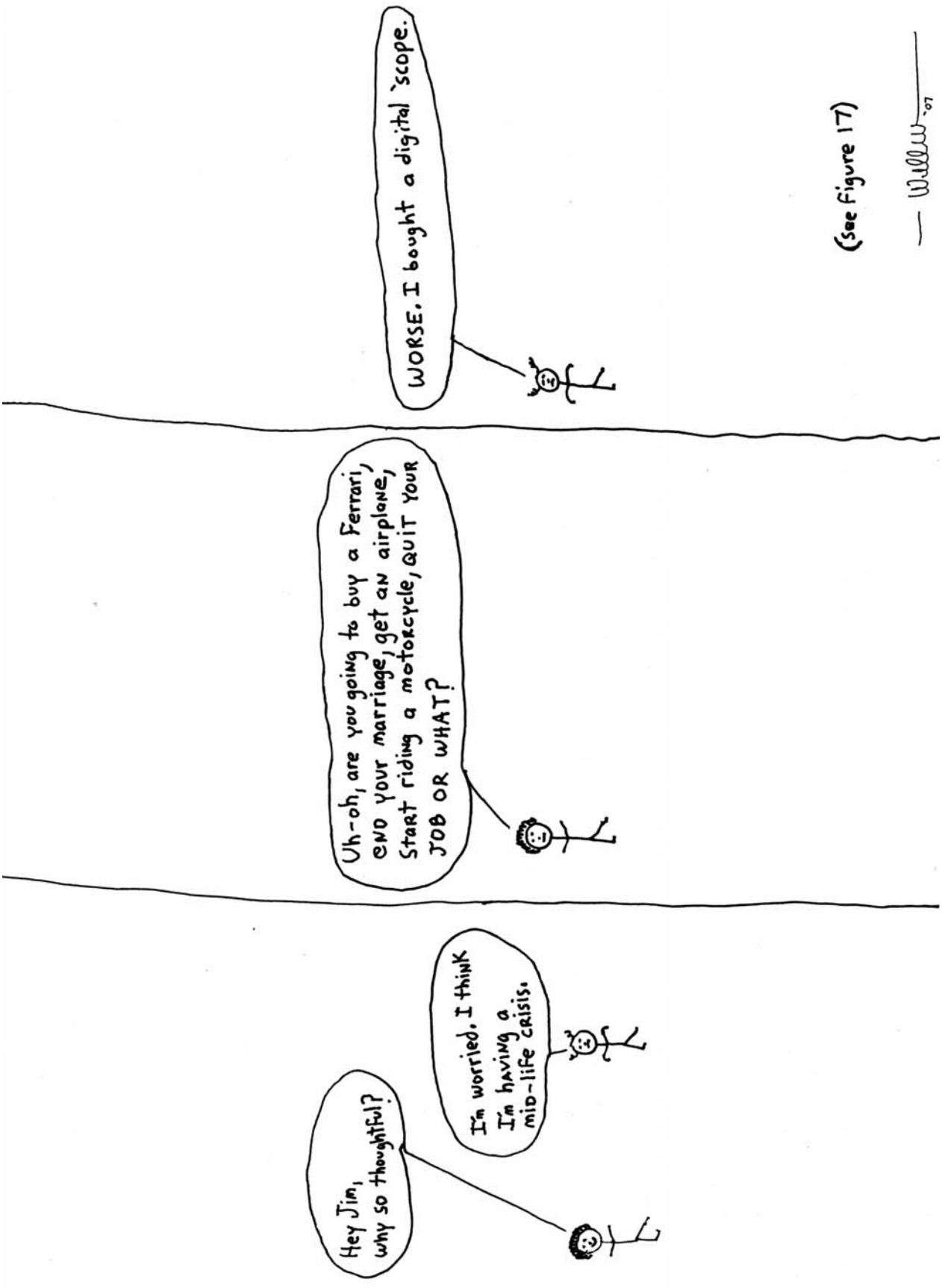

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