Linear Technology Magazine Circuit Collection, Volume III

Data Conversion, Interface and Signal Processing

Richard Markell, Editor

INTRODUCTION

Application Note 67 is a collection of circuits from the first five years of *Linear Technology*, targeting data conversion, interface and signal processing applications. This Application Note includes circuits such as fast video multiplexers for high speed video, an ultraselective bandpass filter circuit with adjustable gain and a fully differential, 8-channel, 12-bit A/D system. The categories included herein are data conversion, interface, filters, instrumentation, video/op amps and miscellaneous circuits. Application Note 66, which covers power products and circuits from *Linear Technology*'s first five years, is also available from LTC.

ARTICLE INDEX

Data Conversion

FULLY DIFFERENTIAL, 8-CHANNEL, 12-BIT A/D SYSTEM USING THE LTC1390 AND LTC1410

by Kevin R. Hoskins

The LTC1410's fast 1.25Msps conversion rate and differential ±2.5V input range make it ideal for applications that require multichannel acquisition of fast, wide bandwidth signals. These applications include multitransducer vibration analysis, race vehicle telemetry data acquisition and multichannel telecommunications. The LTC1410 can be combined with the LTC1390 8-channel serial interfaced analog multiplexer to create a differential ADC system with conversion throughput rates up to 625ksps. This rate applies to situations where the selected channel changes with each conversion. The conversion rate increases to 1.25Msps if the same channel is used for consecutive conversions.

Figure 1 shows the complete differential, 8-channel A/D circuit. Two LTC1390s, U1 and U2, are used as noninvert-

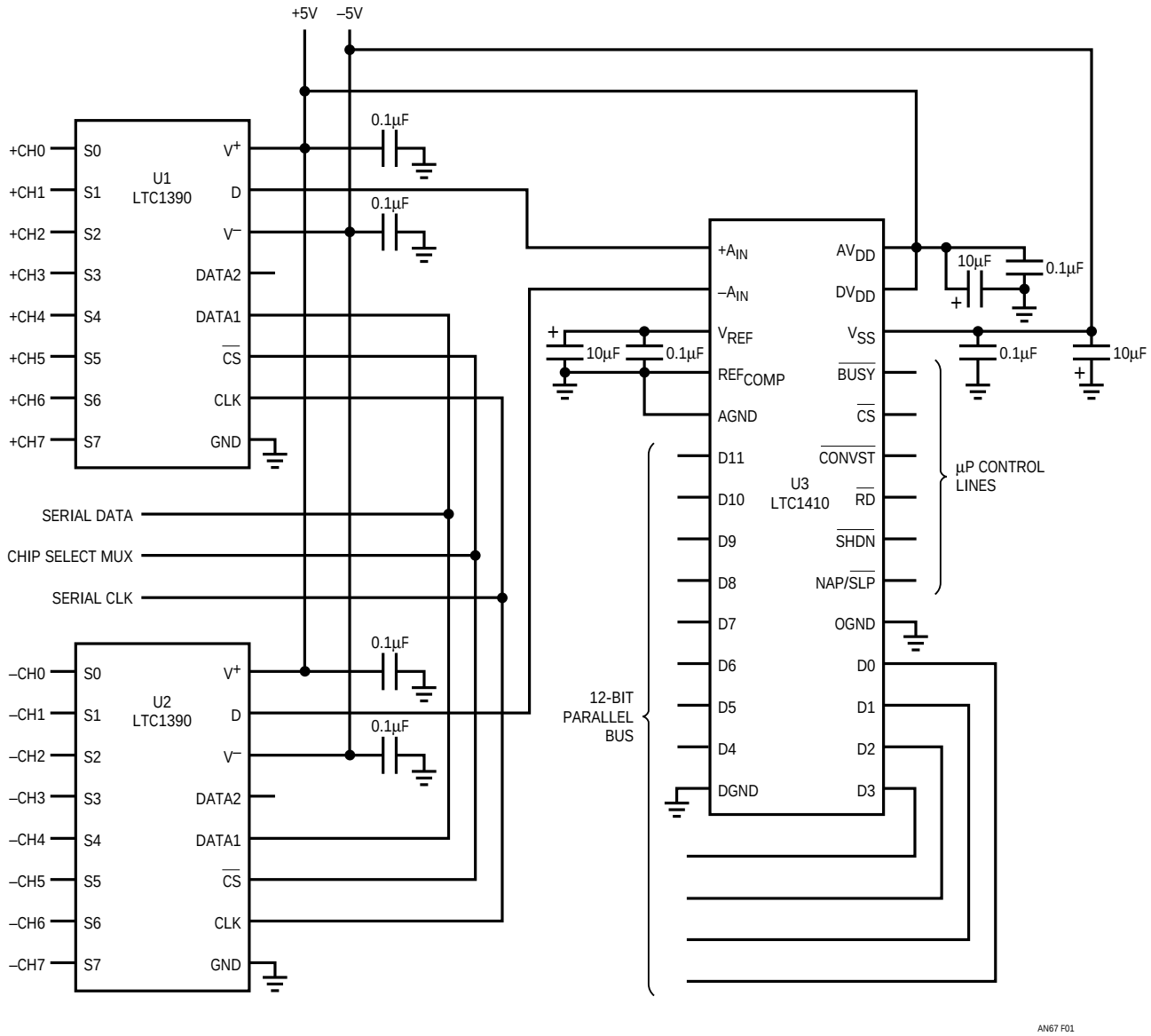


Figure 1. Fully Differential 8-Channel Data Acquisition System Achieves 625ksps Throughput

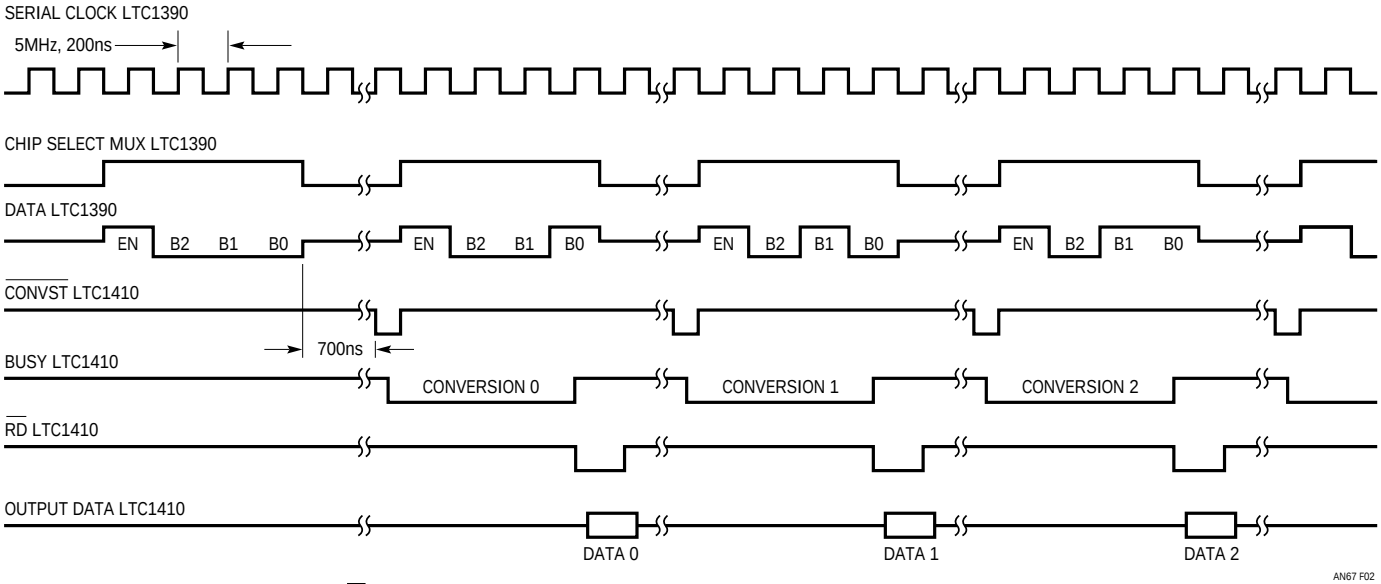
ing and inverting input multiplexers. The outputs of the noninverting and inverting multiplexers are applied to the LTC1410's $+A_{IN}$ and $-A_{IN}$ inputs, respectively. The LTC1390 share the Chip Select MUX, Serial Data and Serial Clock control signals. This arrangement simultaneously selects the same channel on each multiplexer: S0 for both +CH0 and –CH0, S1 for both +CH1 and –CH1, and so on.

As shown in the timing diagram (Figure 2), MUX channel selection and A/D conversion are pipelined to maximize the converter's throughput. The conversion process begins with selecting the desired multiplexer channel pair. With a logic high applied to the LTC1390's $\overline{CS}$ input, the channel pair data is clocked into each Data 1 input on the rising edge of the 5MHz clock signal. Chip Select MUX is then pulled low, latching the channel pair selection data. The signals on the selected MUX inputs are then applied to the LTC1410's differential inputs. Chip Select MUX is pulled low 700ns before the LTC1410's conversion start input, $\overline{CONVST}$, is pulled low. This corresponds to the maximum time needed by the LTC1390's MUX switches to fully turn on. This ensures that the input signals are fully settled before the LTC1410's S/H captures its sample.

The LTC1410's S/H acquires the input signal and begins conversion on $\overline{CONVST}$'s falling edge. During the conversion, the LTC1390's $\overline{CS}$ input is pulled high and the data for the next channel pair is clocked into Data 1. This pipelined operation continues until a conversion sequence is completed. When a new channel pair is selected for each conversion, the sampling rate of each channel is 78ksps, allowing an input signal bandwidth of 39kHz for each channel of the LTC1390/LTC1410 system.

To maximize the throughput rate, the LTC1410's $\overline{CS}$ input is pulled low at the beginning of a series of conversions. The LTC1410's data output drivers are controlled by the signal applied to $\overline{RD}$. The conversion's results are available 20ns before the rising edge of Busy. The rising edge of the Busy output signal can be used to notify a processor that a conversion has ended and data is ready to read.

This circuit takes advantage of the LTC1410's very high 1.25Msps conversion rate and differential inputs and the LTC1390's ease of programming to create an A/D system that maintains wide input signal bandwidth while sampling multiple input signals.



A LOGIC LOW IS APPLIED TO THE LTC1410S $\overline{CS}$ INPUT DURING A CONVERSION SEQUENCE.

Figure 2. The Figure 1 Circuit Timing Diagram

12-BIT DAC APPLICATIONS

by Kevin R. Hoskins

System Autoranging

System autoranging, adjusting an ADC's full-scale range, is an application area for which the LTC1257 is appropriate. Autoranging is especially useful when using an ADC with multiplexed inputs. Without autoranging only two reference values are used: one to set the full-scale magnitude and another to set the zero scale magnitude. Since it is common to have input signals with different zero scale and full-scale magnitude requirements, fixed reference voltages present a problem. Although the ranges selected for some of the inputs may take advantage of the full range of ADC output codes, inputs that do not span the same range will not generate all codes, reducing the ADC's effective resolution. One possible solution is to match the reference voltage span to each multiplexer input.

The circuit shown in Figure 3 uses two LTC1257s to set the full-scale and zero operating points of the LTC1296 12-bit, 8-channel ADC. The ADC shares its serial interface with the DACs. To further simplify bus connections, the DACs' data is daisy-chained. Two chip selects are used, one to select the LTC1296 when programming its multiplexer and the other to select the DACs when setting their output voltages.

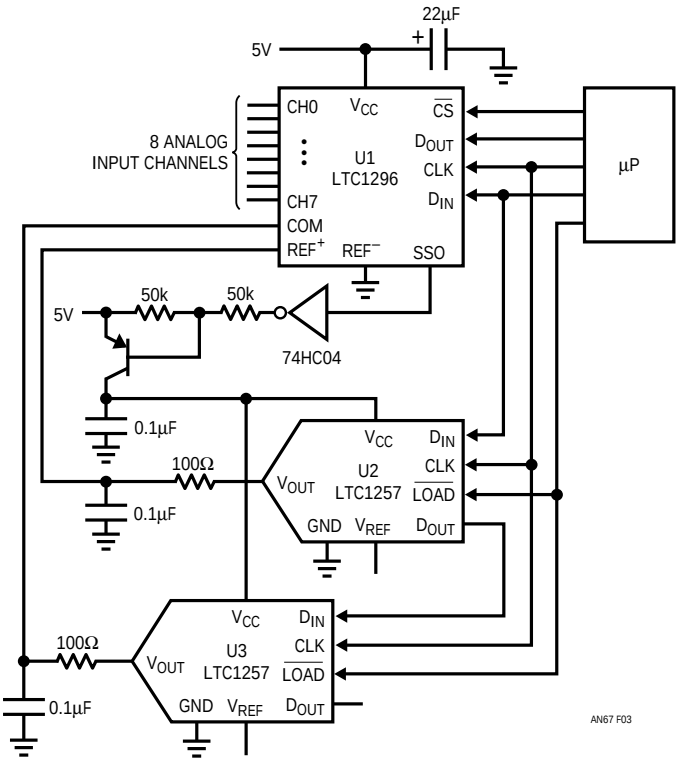


Figure 3. Using Two LTC1257 12-Bit Voltage Output DACs to Set the Input Span of the 12-Bit 8-Channel LTC1296

During the conversion process, U2 and U3 receive the full and zero scale codes, respectively, that correspond to a selected multiplexer channel. For example, let channel 2's span begin at 2V and end at 4.5V. When a host processor wants a conversion of channel 2's input signal, it first sends code that sets the output of U2 to 2V and U3 to 4.5V, fixing the span to 2.5V. The processor then sends data to the LTC1296 selecting channel 2. The processor next clocks the LTC1296 and reads the data generated during the conversion of the $3.5V_{P-P}$ signal applied to channel 2. As other multiplexer channels are selected the DAC outputs are changed to match their spans.

Computer-Controlled 4 – 20mA Current Loop

A common and useful circuit is the 4 – 20mA current loop. It is used to transmit information over long distances using varying current levels. The advantage of using current over voltage is the absence of IR losses and the transmission errors and signal losses they can create.

The circuit in Figure 4 is a computer-controlled 4 – 20mA current loop. It is designed to operate on a single supply over a range of 3.3V to 30V. The circuit's zero output reference signal, 4mA, is set by R1 and calibrated using R2, and its full-scale output current is set by R3 and calibrated using R4. The zero and full-scale output currents are set as follows: with a zero input code applied to the LTC1453, the output current, I_{OUT}, is set to 4mA by adjusting R2; next, with a full-scale code applied to the DAC the full-scale output current is set to 20mA by adjusting R4.

The circuit is self-regulating, forcing the output current to remain stable for a fixed DAC output voltage. This self-regulation works as follows: starting at t = 0, the LTC1453's fixed output (in this example, 2.5V) is applied to the left side of R3; instantaneously, the voltage applied to the LT1077's input is 1.25V; this turns on Q1 and the voltage across R_S starts increasing beginning from 1.25V; as the

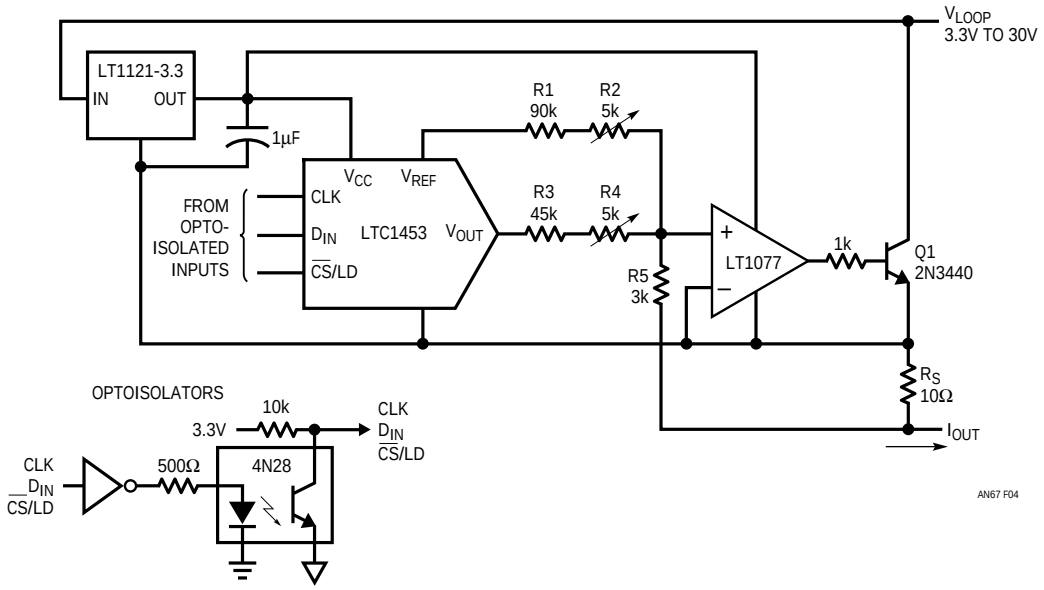


Figure 4. The LTC1453 Forms the Heart of This Isolated 4 – 20mA Current Loop

voltage across R_S increases it lifts the LTC1453's GND pin above 0V; the voltage across R_S continues to increase until it equals the DAC's output voltage.

Once the circuit reaches this stable condition, the constant DAC output voltage sets a constant current through R3 + R4 and R5. This constant current fixes a constant voltage across R5 that is also applied to the LT1077's noninverting input. Feedback from the top of R_S is applied to the inverting input. As the op amp forces its inputs to the same voltage, it will fix the voltage at the top of R_S. This in turn fixes the output current to a constant value.

Optoisolated Serial Interface

The serial interface of the LTC1451 family and the LTC1257 make optoisolated interfaces very easy and cost effective. Only three optoisolators are needed for serial data communications. Since the inputs of the LTC1451, LTC1452 and LTC1453 have generous hysteresis, the switching speed of the optoisolators is not critical. Further, because each of these DACs can be daisy-chained to others, only three optoisolators are required.

LTC1329 MICROPOWER, 8-BIT, CURRENT OUTPUT DAC USED FOR POWER SUPPLY ADJUSTMENT, TRIMMER POT REPLACEMENT

by K.S. Yap

Power Supply Voltage Adjustment

Figure 5 is a schematic of a digitally controlled power supply voltage adjustment circuit using a 2-wire interface. The LT1107 is configured as a step-up DC/DC converter, with the output voltage (V_{OUT}) determined by the values of the feedback resistors. The LTC1329's DAC current output is connected to the feedback node of these resistors, and an 8051 microprocessor is used to interface to the LTC1329.

By simply clocking the LTC1329, the DAC current output is decreased or increased (decreased if D_{IN} = 0, increased if D_{IN} = 1), causing V_{OUT} to change accordingly.

Trimmer Pot Replacement

Figure 6 is a schematic of a digitally controlled offset voltage adjustment circuit using a 1-wire interface. By clocking the LTC1329, the DAC current output is increased, causing V_{R2} to increase accordingly. When the DAC current output reaches full scale it will roll over to zero, causing V_{R2} to change from the maximum offset trim voltage to the minimum offset trim voltage.

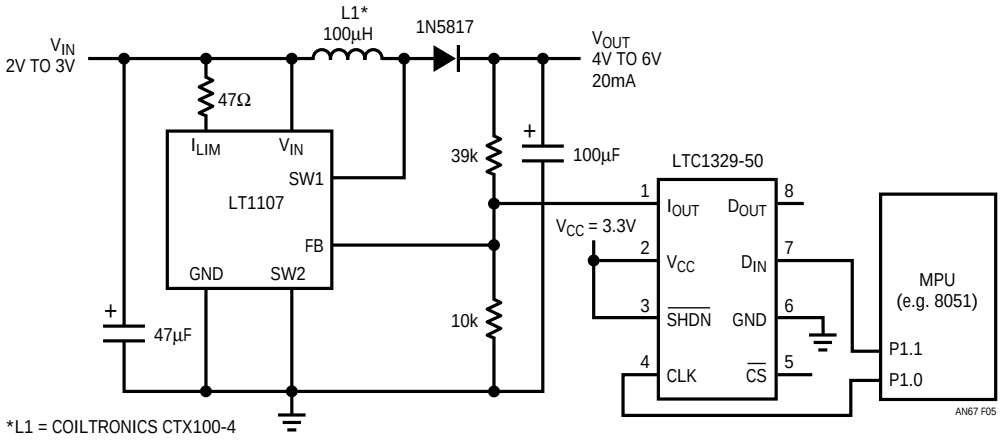


Figure 5. LTC1329 Digitally Controls the Output Voltage of a Power Supply

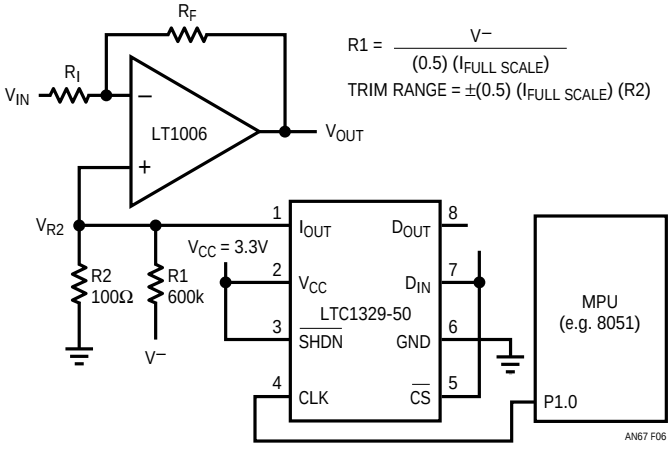


Figure 6. LTC1329 Used to Null Op Amp's Offset Voltage

12-BIT COLD JUNCTION COMPENSATED, TEMPERATURE CONTROL SYSTEM WITH SHUTDOWN
by Robert Reay

The circuit in Figure 7 is a 12-bit, single 5V supply temperature control system with shutdown. An external temperature is monitored by a J-type thermocouple. The LT1025A provides the cold junction compensation for the thermocouple and the LTC1050 chopper op amp provides signal gain. The 47kΩ, 1µF RC network filters the chopping noise before the signal is sent to the A/D converter. The LTC1297 A/D converter uses the reference of the LTC1257 after it has been filtered to set full scale. After the A/D measurement is taken $\overline{CS}$ is pulled high and everything except the LTC1257 is powered down, reducing the system supply current to about 350µA. A word can then be written to the LTC1257 and its output can be used as a temperature control signal for the system being monitored.

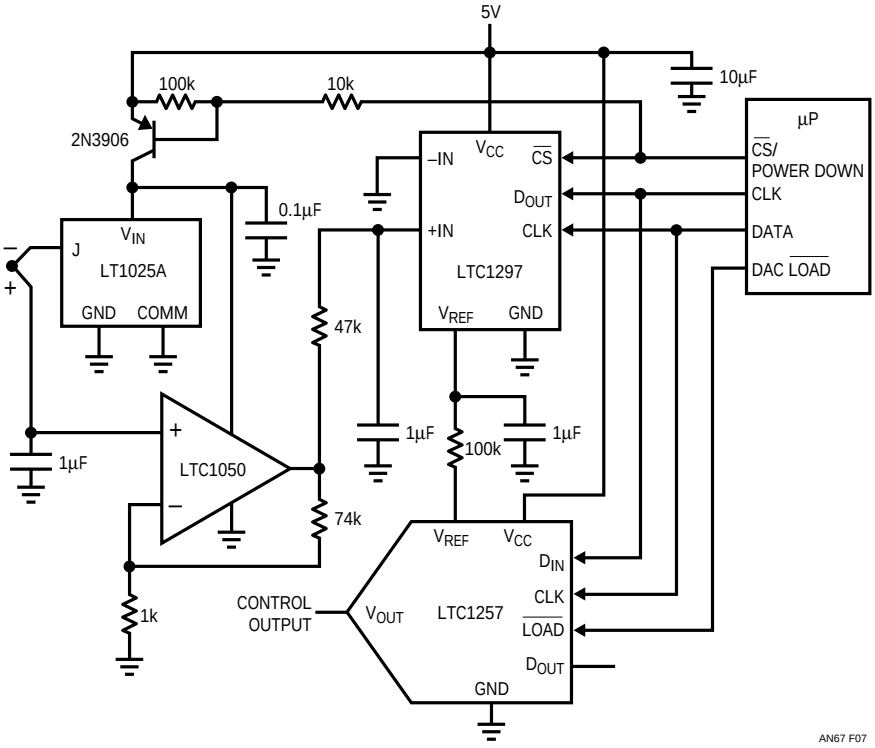


Figure 7. 12-Bit Single 5V Control System with Shutdown

A 12-BIT MICROPOWER BATTERY CURRENT MONITOR

by Sammy Lum

Introduction

The LTC1297 forms the core of the micropower battery current monitor shown in Figure 8. This 12-bit data acquisition system features an automatic power shutdown that is activated after each conversion. In shutdown the supply current is reduced to 6µA, typically. As shown in Figure 9, the average power supply current of the LTC1297 varies from milliamperes to a few microamperes as the sampling frequency is reduced. This circuit draws only 190µA from a 6V to 12V battery when the sampling frequency is less than 10 samples per second. Wake-up time is limited by that required by the LTC1297 (5.5µs). For long periods of inactivity, the circuit's supply current can be further reduced to 20µA by using the shutdown feature on the LT1121. More wake-up time is required when using this mode of shutdown. It is usually determined by the amount of capacitance in the circuit and the available charging current from the regulator.

The Battery Current Monitor

The battery voltage of 6V to 12V is regulated down to 5V by the LT1121 micropower regulator. A sense resistor of 0.05Ω is placed in series with the battery to convert the battery current to a voltage. Full scale is designed for 2A, giving a resolution of 0.5mA with the 12-bit ADC. The LTC1047 amplifies the voltage across the sense resistor

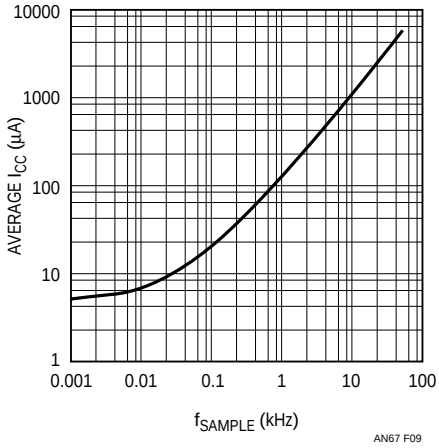


Figure 9. Power Supply Current vs Sampling Frequency for the LTC1297

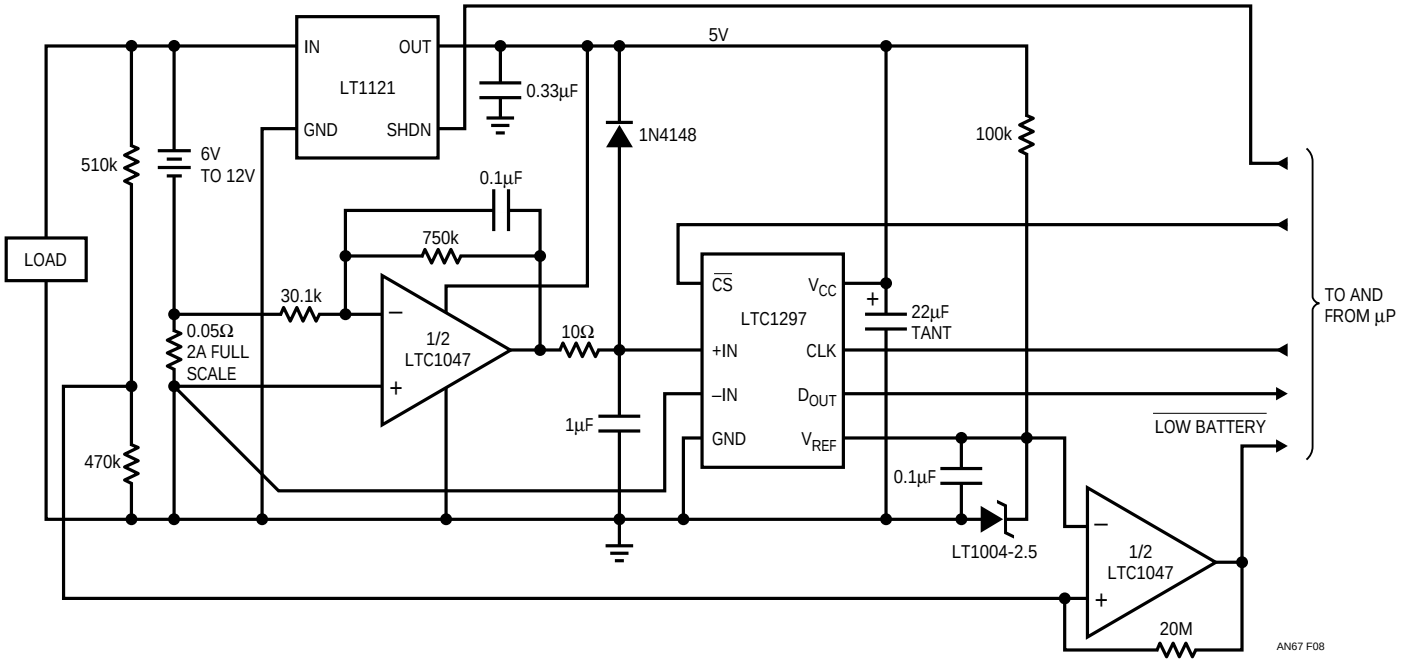


Figure 8. A Micropower Battery Current Monitor Using the LTC1297 12-Bit Data Acquisition System

by 25 V/V. This goes through an RC lowpass filter before being fed into the input of the LTC1297. The RC filter serves two functions. First it helps band limit the input noise to the ADC. Second the capacitor helps the LTC1047 recover from transients due to the switching input capacitor of the LTC1297. The LT1004 provides the full-scale reference for the ADC. A low-battery detection circuit has been created by using the other half of the LTC1047 as a comparator. Its trip point has been set to 5V plus the dropout voltage of the LT1121. Because data is transmitted serially to and from the microprocessor or microcontroller, this current monitor circuit can be located close to the battery.

Interface

V.35 TRANSCEIVERS ALLOW 3-CHIP V.35 PORT SOLUTION

by Y.K. Sim

Two new LTC interface devices, the LTC1345 and the LTC1346, provide the differential drivers and receivers needed to implement a V.35 interface. When used in conjunction with an RS232 transceiver like the LT1134A, they allow a complete V.35 interface to be implemented with just two transceiver chips and one resistor termination chip. The LTC1345 and LTC1346 provide the three differential drivers and receivers necessary to implement the high speed path and the LT1134A provides the four RS232 drivers and receivers required for the handshaking interface. Both the LTC1345 and the LT1134A provide onboard charge pump power supplies allowing a complete V.35 interface to be powered from a single 5V supply. For systems where ±5V supplies are present the LTC1346 is offered without charge pumps, representing a 30% power savings.

The differential transceivers are capable of operating at data rates above 10MBd in nonreturn-to-zero (NRZ) format.

The RS232 handshaking lines can be implemented with standard RS232 transceivers. The LT1134A provides four RS232 drivers and four receivers, enough to implement the extended 8-line handshaking protocol specified in V.35. The LT1134A also includes an onboard charge pump to generate the higher voltages required by RS232 from a single 5V supply, making it an ideal companion to the LTC1345. These two chips, together with the BI Technologies termination resistor network chip provide a complete surface mountable 5V-only V.35 data port. Systems that have multiple power supply voltages available and use only the simpler 5-signal V.35 handshaking protocol can use the LTC1346 with the LT1135A or LT1039 RS232 transceivers; this combination provides a complete port while saving board space and complexity. Figure 10 shows a typical LTC1345/LT1134A V.35 implementation with five differential signals and five basic handshaking signals with an option for three additional handshaking signals.

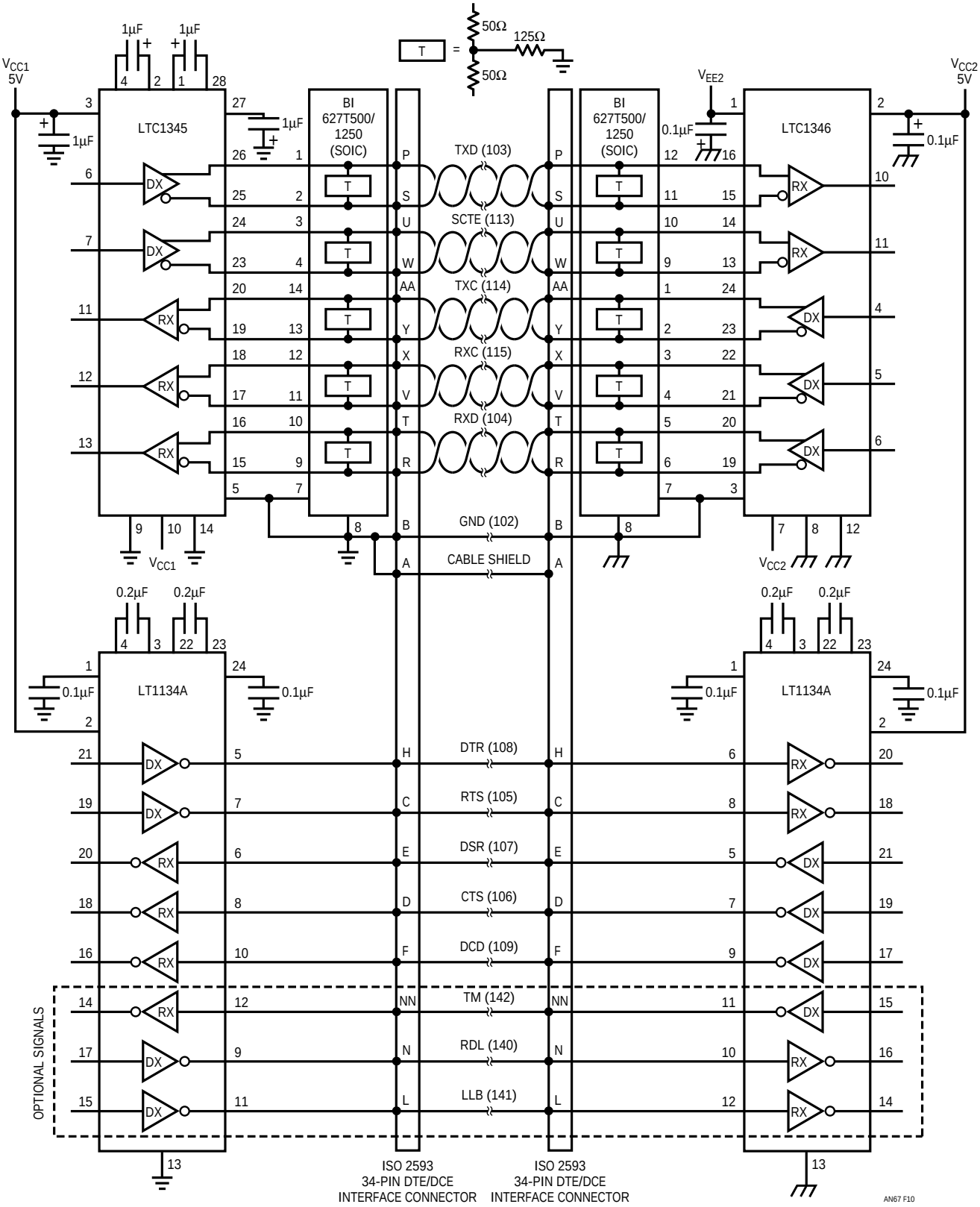


Figure 10. Typical V.35 Implementation Using LTC1345 and LTC1346

SWITCHING, ACTIVE GTL TERMINATOR

by Dale Eagar

Introduction

New high speed microprocessors, especially those used in multiprocessor workstations and video graphics terminals, require high speed backplanes that support peak data rates of up to 1Gbps. The backplane is a passive component, whereas all drivers and receivers are implemented in low voltage swing CMOS (also referred to as GTL logic). These applications require bidirectional terminators, terminators that will either source or sink current (in this case, at 1.55V). The current requirements of the terminator depended on the number of terminations on the backplane. Present applications may require up to 10A. This specification may, of course, be reduced if required.

Circuit Operation

The complete schematic of the terminator is shown in Figure 11. The circuit is based on the LT1158 half-bridge, N-channel, power MOSFET driver. The LT1158 is configured to provide bidirectional synchronous switching to MOSFETs Q1 through Q6. VR1, an LT1004-1.2, R1 and C1 generate a 1.25V reference voltage that programs the terminator's output voltage. U1A, an LT1215, is a moderate speed (23MHz GBW) precision operational amplifier that subtracts the error voltage at its inverting input from the 1.25V reference. U1A is also used to amplify this error signal. Components R3 and C2 tailor the phase and gain of this section and are selected when evaluating the system's load step response.

U1B and part of U2 provide the gain and the phase inversion necessary to form an oscillator. C3 and C4 provide positive feedback at high frequencies, which is necessary for the system to oscillate in a controlled manner while keeping the voltage excursions within the common mode range of U1B. R8, U2 and C6 provide phase inversion and negative feedback at the middle frequencies, causing U1B to oscillate at a frequency much higher than the feedback loop's response. The DC path for the oscillator is closed through the power MOSFETs Q1 to Q6, the output choke L1, the output capacitor C11 and through the feedback path with the error amplifier. R4 and R7 set the center of the common mode voltage of U1B and are selected to limit the maximum duty factor the oscillator can achieve.

R9, R10, R12 and C9 provide output current sense to U2, allowing it to shut down the oscillator via the Fault pin (Pin 5) to prevent catastrophic or even cataclysmic events from occurring. D2, C8 and the circuitry behind the Boost pin (Pin 16) of U2 work together to provide more than sufficient gate drive for the N-channel FETs Q1-3. D3, R11 and C7 allow the oscillator to start up regardless of the state of the oscillator on powerup.

Performance

The circuit provides excellent transient response, efficiencies in the source mode of better than 80% and efficiencies in the sink mode of better than 90%. Figure 12 shows the step response of the terminator.

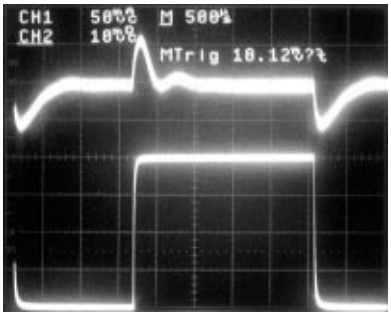
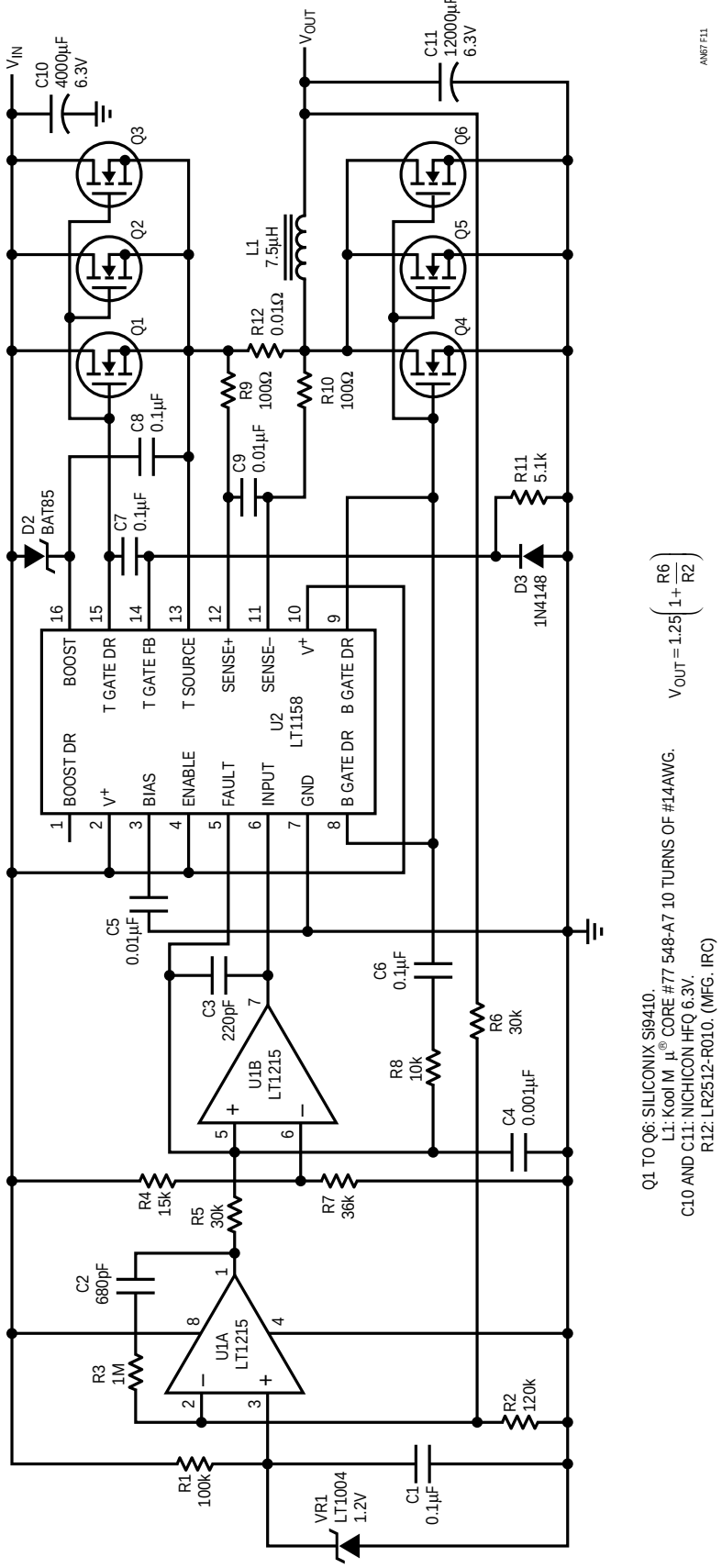


Figure 12. Step Response of LT1158-Based Terminator



$$V_{OUT} = 1.25\left(1+\frac{R6}{R2}\right)$$

Q1 TO Q6: SILICONIX Si9410.
L1: Kool M µ® CORE #77 548-A7 10 TURNS OF #14AWG.
C10 AND C11: NICHICON HFQ 6.3V.
R12: LR2512-R010. (MFG. IRC)

Kool M µ is a registered trademark of Magnetics, Inc.

Figure 11. GTL 1.55V Terminator Provides 10A Max Current

RS232 TRANSCEIVERS FOR DTE/DCE SWITCHING

by Gary Maulding

Switched DTE/DCE Port

There are situations where a data port is required to act alternately as either a DTE or a DCE. Examples include test equipment and data multiplexers. Figure 13 shows a circuit that can switch from a 9-pin DTE to a 9-pin DCE configuration while maintaining full compliance with the RS232 standards.

The circuit uses an LT1137A DTE transceiver and an LT1138A DCE transceiver. A DTE/DCE select logic signal alternately activates or shuts down one of the two transceivers. In addition to drawing no power, the OFF transceiver's drivers achieve a high impedance state, removing themselves from the data line. The receiver inputs will continue to load the line, but this presents no operational problem and does not violate the RS232 standard. The drivers on the activated transceiver can easily drive the extra load of the companion transceiver's inputs along with the termination at the opposite end of the cable. The scope photograph (Figure 14) shows the signal outputs of the DTE/DCE switched circuit driving 3k || 1000pF at 120kBd.

To the transceiver at the opposite end of the data line the data port always appears to be a normal fixed port. All signals into the port are properly terminated in 5k.

The schematic in Figure 13 shows the essential features needed to implement DTE/DCE switching but other features can be easily included. Shutdown of both transceivers could be implemented by adding an additional logic control signal. Multiplexing of the logic level signals is also possible since receiver outputs remain in a high impedance state when the transceivers are shut down. Two capacitors can be saved by sharing the V^+ and V^- filter capacitors between the two transceivers, but the charge pump capacitors must not be shared.

The circuits used in the demonstration circuit are bipolar, but Linear Technology's CMOS transceivers, such as the LTC1327 and 1328 could be substituted where the absolute minimum power dissipation is required.

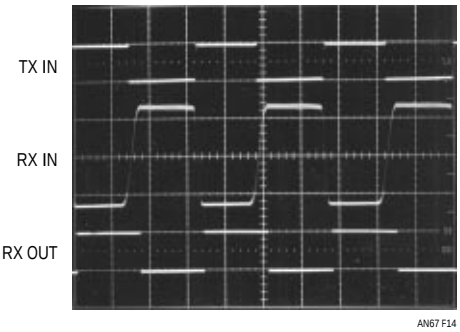


Figure 14. Oscillograph Showing Signal Outputs of the DTE/DCE Circuit of Figure 13 Driving 3k || 1000pF at 120kBd

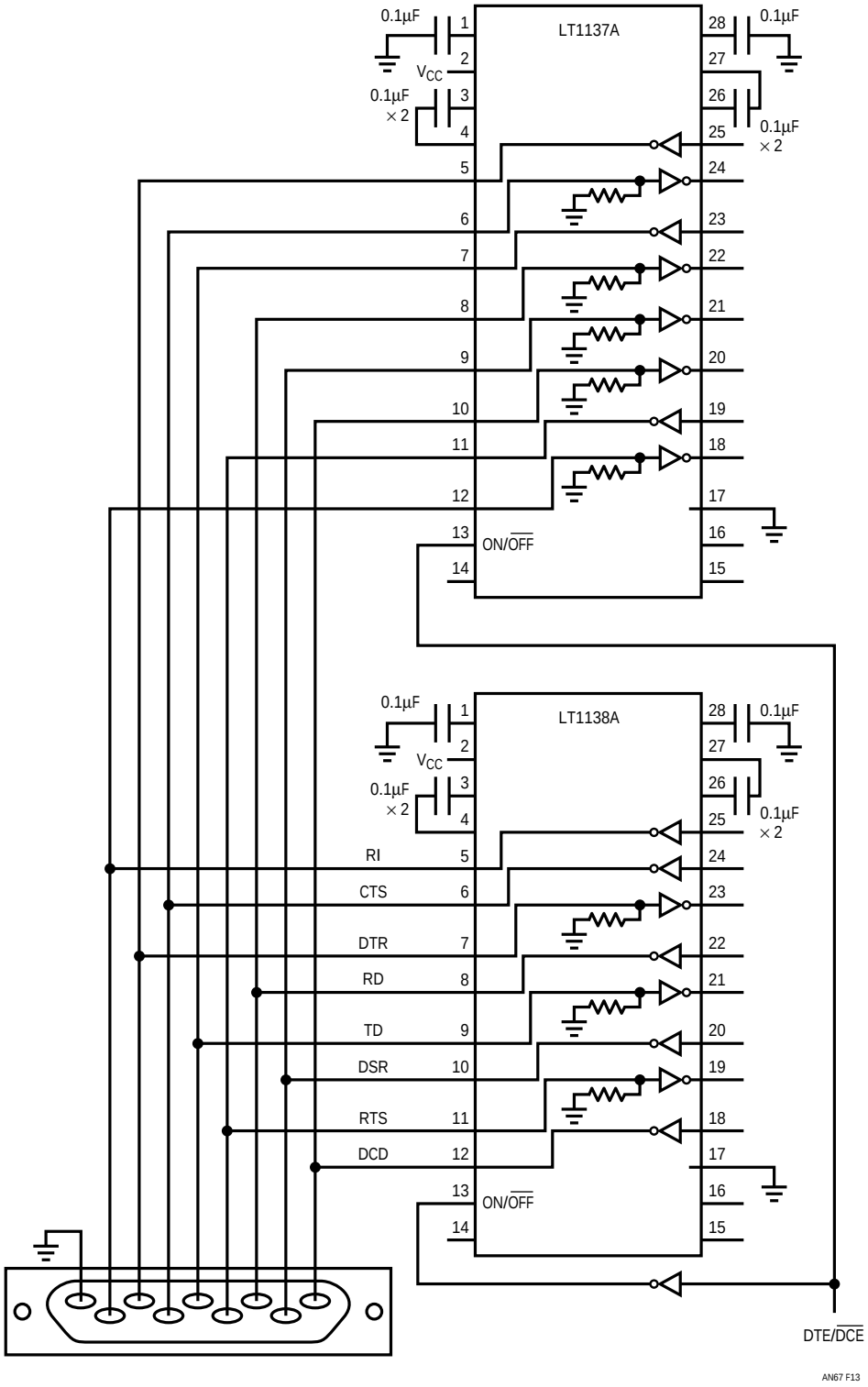


Figure 13. Switchable, 9-Pin DTE/DCE Data Port Circuitry

ACTIVE NEGATION BUS TERMINATORS

by Dale Eagar

High speed data buses require transmission line techniques, including termination, to preserve signal integrity. Lost data on a bus can be attributed to reflections of the signals from the discontinuities of the bus. The solution to this problem is proper termination of the bus.

Early designs of bus terminators were passive (see Figure 15). Passive termination works great but wastes lots of precious power, especially when the bus is not being used.

The ideal solution is a voltage source capable of both sourcing and sinking current. Such a voltage source, with termination resistors, is shown in Figure 16. This is called active negation. Active negation uses minimal quiescent current, essentially providing only the power needed to properly terminate the bus.

Active Negation Bus Terminator Using Linear Voltage Regulation

The active negation circuit shown in Figure 17 provides the power to the output at an efficiency of about 50%; the rest of the power is dissipated in either Q1 or U1 depending on the polarity of the output current.

The circuit will source or sink current. Current is sourced from the 5V supply through Q1, an NPN Darlington, to the output. The sink current flows through CR1 into the collector (Pin 1) of the LT1431, and to ground. The LT1431 regulates a scaled version of the output voltage against the

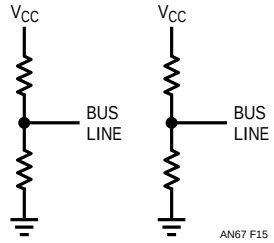


Figure 15. Passive Termination Technique

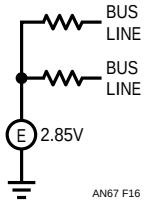


Figure 16. Active Negation Termination Technique

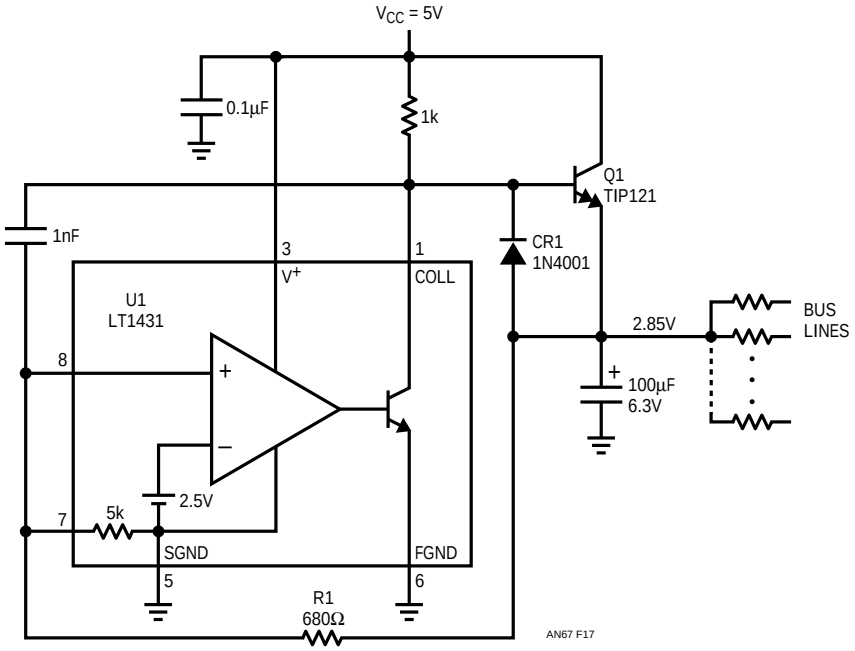


Figure 17. Linear Active Negation Voltage Source

internal 2.5V bandgap reference, driving the base of Q1 or drawing current through CR1 to regulate the output voltage. R1 and the internal 5k resistor of the LT1431 scale the output voltage.

Switching Power Supply, Active Negation Network

The switching active negation terminator shown in Figure 18 is a synchronous switcher. This solution further reduces dissipation and therefore achieves higher efficiency. This type of switcher can both source and sink current.

The switching power supply operates as follows. The 74AC04 hex inverters (U1 and U2) form a 1MHz variable duty factor oscillator. The duty factor is controlled by the output of the regulator, U3, and is maintained at the ratio of 2.85V/V_{IN}. V_{IN} is the 5V supply that powers U1, U2 and U3. The output voltage is the average voltage of the square wave (V_{IN})(duty factor) from the outputs of U1B–U1F and U2A–U2F. L1 and C2 filter the AC component of the 0V to 5V signal yielding a DC output voltage of 2.85V.

CR1 is added to prevent latchup of U1 and U2 during adverse conditions.

A logic gate could easily be added to the oscillator to add a disable function to this terminator, further lowering the quiescent power when termination is not needed.

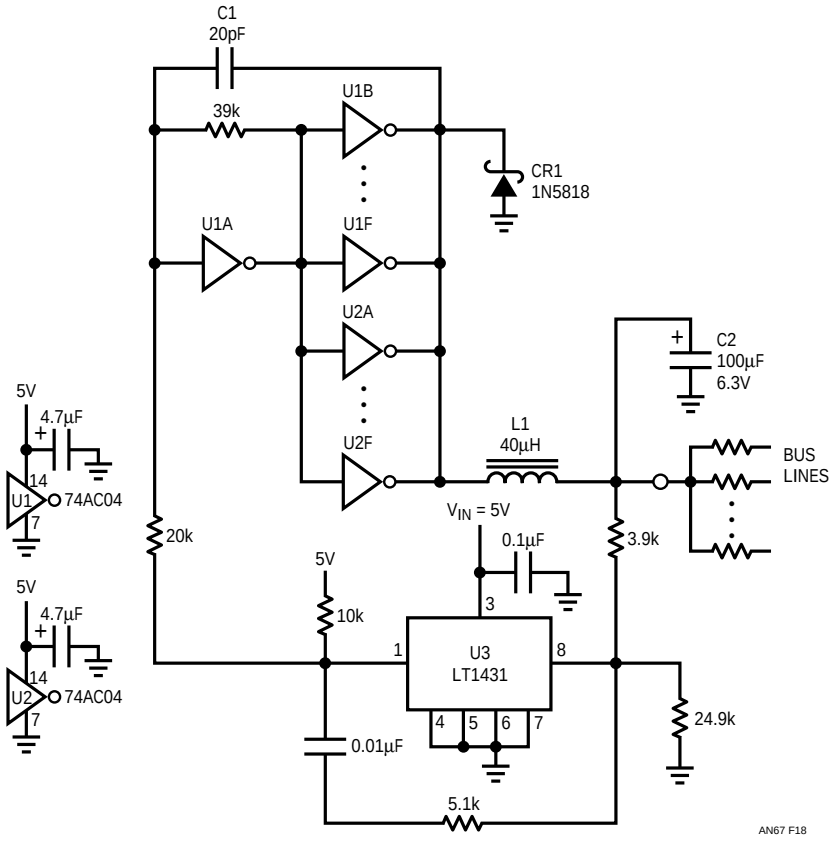


Figure 18. Switching Active Negation Termination

RS485 REPEATER EXTENDS SYSTEM CAPABILITY

by Mitchell Lee

RS485 data communications are specified for distances of up to 4000 feet. This limit is the consequence of losses in the twisted pair used to carry the data signals. Beyond 4000 feet, skin effect and dielectric losses take their toll, attenuating the signal beyond use.

If greater distances must be covered some means of repeating the data is necessary. One method is to terminate a long run of cable with a microprocessor-based node capable of relaying data to yet another length of cable.

A more simple solution* is shown in Figure 19. Two RS485 transceivers are connected back-to-back so as to relay incoming data from either side to the other. A pair of cross coupled one-shots furnish a means of "flow control" so that one and only one transmitter is turned on at any given time. Incoming data is sensed by detecting a 1-0 transition at the output of either idling receiver. The first receiver to spot such a transition triggers its associated one-shot, which, in turn, activates the opposite transmitter and ensures smooth data flow from one side to the other. At the same time the one-shot locks out the other receiver/transmitter/one-shot combination so that only one data path is open.

The one-shot is retriggered by successive 1-0 transitions and start bits, holding the data path in this configuration. The one-shot time constant is set slightly greater than the interval between any two start bits. When the received data stops, the line idles high, producing a 1 at the receiver's output. The one-shot resets, returning the opposite transceiver to the receive mode—ready for any subsequent data flow.

In order to allow adequate time for the one-shot to reset, the software protocol must wait one word length after the end of any data transmission before responding to a call or initiating a new conversation. As shown, the repeater is set up for 100kBd data rates and an 8-bit word length (plus start and stop bits).

*Honeywell Inc. patent 4, 670, 886 may apply.

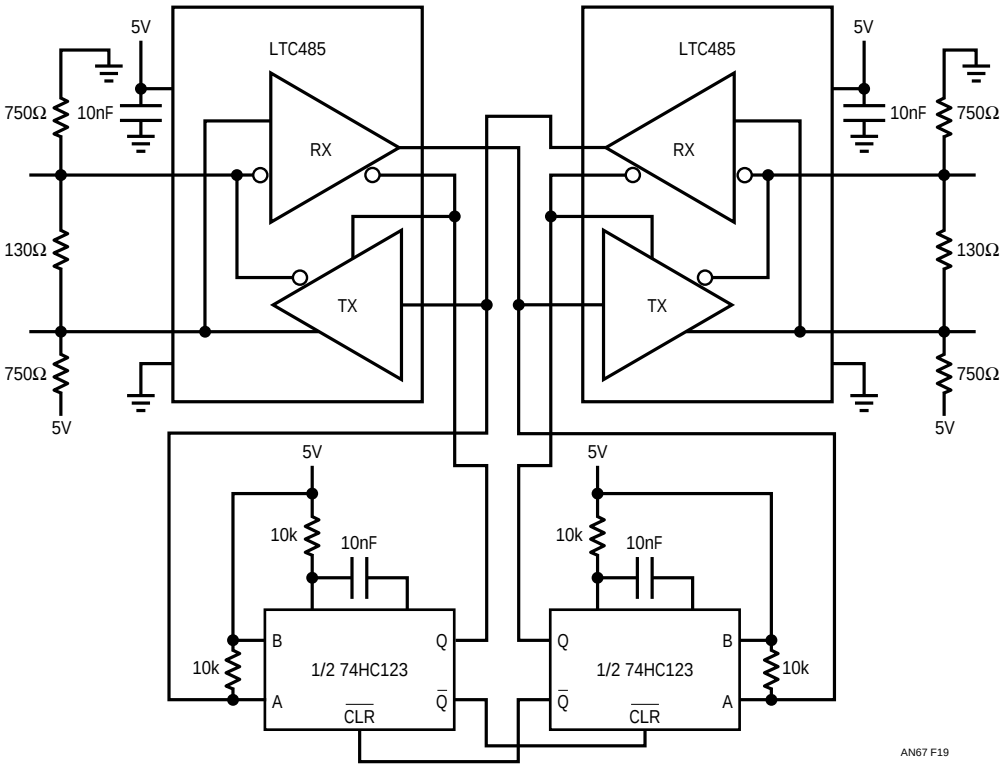


Figure 19. RS485 Repeater Schematic Diagram

AN LT1087-BASED 1.2V GTL TERMINATOR

by Mitchell Lee

A recent development in high speed digital design has resulted in a new family of logic chips called Gunning Transition Logic (GTL). Because of the speeds involved, careful attention must be paid to the transmission line characteristics of the interconnections between these chips; active termination is required.

The termination voltage is 1.20V and currents of several amperes are common in a complete system. One method of generating 1.2V is to use a linear regulator operating from 3.3V or 5V. Unfortunately, this method suffers from two major drawbacks. First, the minimum adjust voltage, without the aid of a negative supply, is 1.25V for most adjustable linear regulators. Second, most low voltage linear regulators do not feature low dropout characteristics, rendering them unusable on a 3.3V input. The LT1087 solves both of these problems with an output that can be adjusted to less than the reference voltage and a low dropout architecture.

Figure 20 shows the complete circuit. The LT1087 features feedback sense, which, in its original application, was used for remote Kelvin sensing. In the GTL terminator circuit the Sense pins are used to adjust the internal 1.25V reference downward. The result is a 1.20V, 5A regulator with 2% output tolerance over all conditions of line, load and temperature. To minimize power dissipation a 3.3V input source is recommended.

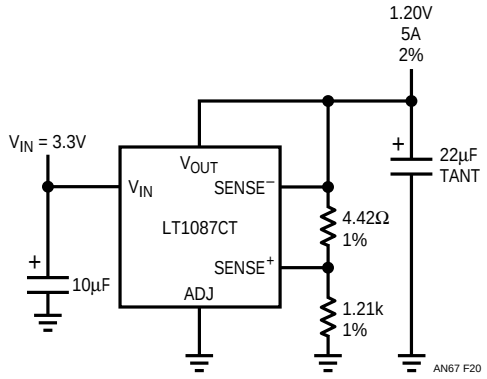


Figure 20. 1.2V GTL Termination Voltage Schematic Diagram

LTC1145/LTC1146 ACHIEVE LOW PROFILE ISOLATION WITH CAPACITIVE LEAD FRAME

by James Herr

The LTC1145 and LTC1146 are a new generation of signal isolators. Previously, signal isolation was accomplished by means of optoisolators. Light from an LED was detected across a physical isolation barrier by either a photo diode or transistor and converted to an electrical signal. Isolation levels up to thousands of volts were easily achieved.

Attempts have been made to provide signal isolation on a single silicon die. Problems arose due to reliability constraints of damage from ESD or overvoltage. A new technique, using a capacitive lead frame, overcomes the problems associated with single package signal isolation. Further, this technique is suitable for use in thin surface mount packages—a solution not available with optoisolators. The data rates are 200kbps for the LTC1145 and 20kbps for the LTC1146. Both parts can sustain over 1000V across their isolation barriers.

Applications

The LTC1145/LTC1146 can be used in a wide range of applications where voltage transients, differential ground potentials or high noise may be encountered, such as isolated serial data interfaces, isolated analog-to-digital converters for process control, isolated FET drivers and low power optoisolator replacement. One possible application is an isolated RS232 receiver. The D_{IN} pin of the LTC1145 is driven by an RS232 signal through a 5.1k resistor (Figure 21). The D_{OUT} pin of the LTC1145 presents

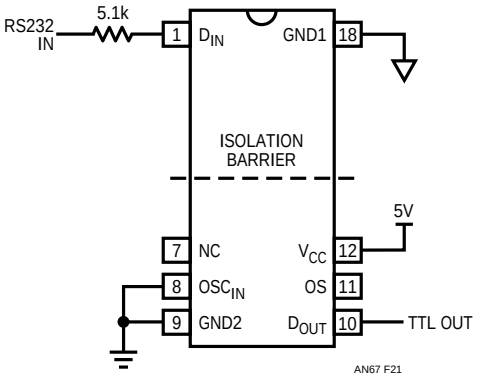


Figure 21. Isolated Low Power RS232 Receiver

isolated TTL-compatible output signals. The GND2 pin of the LTC1145 is connected to the same ground potential as the receiving end of the link. The isolator can accommodate differences of up to 1kV between GND1 and GND2.

Another application is an isolated, thermocouple-sensed temperature-to-frequency converter (see Figure 22). The output of I_3 produces a 0kHz to1kHz pulse train in response to a 0°C to 100°C temperature excursion (see LTC Application Note 45 for the details). The pulses from I_3 drive the D_{IN} pin of LTC1146. The GND1 pin is connected to the same ground potential as I_3. The D_{OUT} pin of LTC1146 presents isolated, TTL-compatible output signals. The circuit consumes only 460µA maximum, allowing it to operate from a 9V battery.

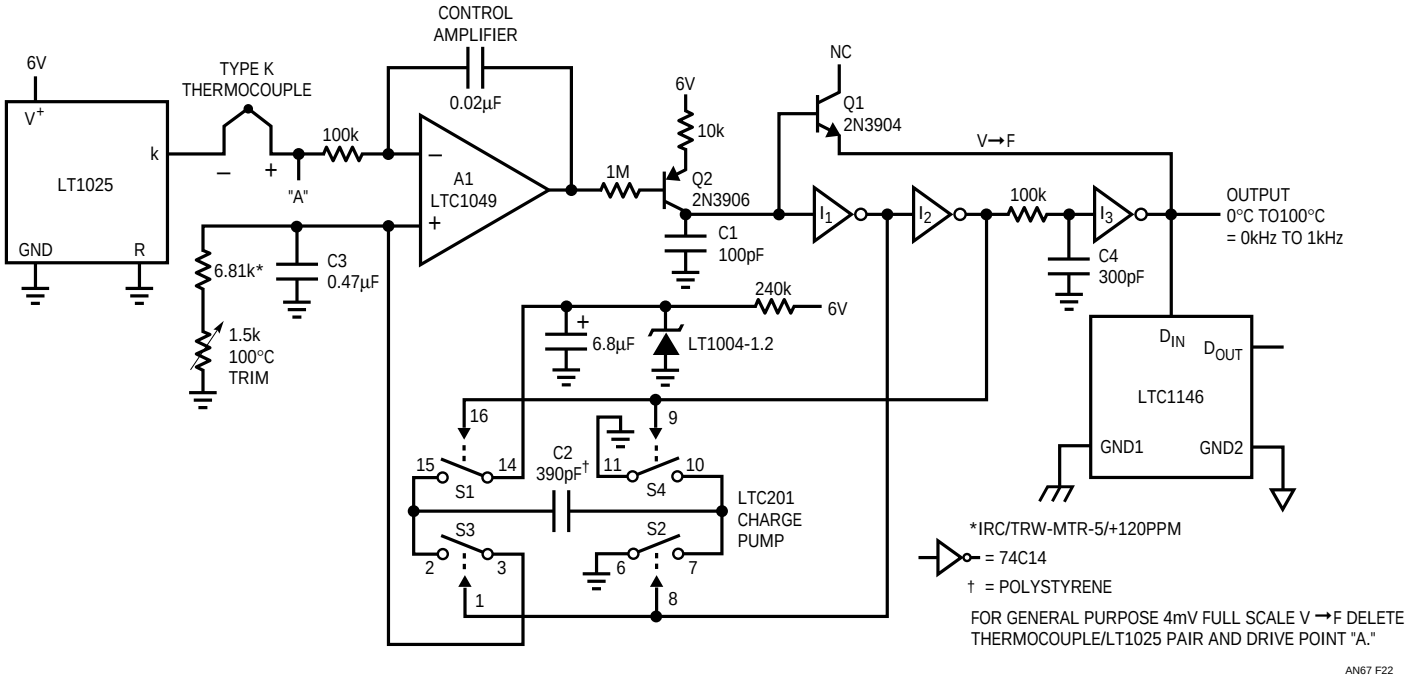


Figure 22. Isolated Temperature-to-Frequency Converter

LTC485 LINE TERMINATION

by Bob Reay

The termination of the data line connecting LTC485 transceivers is very important because an improperly terminated line can cause data errors. The data line is usually a 120Ω shielded twisted pair of wires that is terminated at each end with a 120Ω resistor (Figure 23). For some applications a problem occurs when the output of the drivers is forced into a high impedance state because the termination resistors short the inputs to the receivers. Since the receivers are differential comparators with built-in hysteresis, their output will remain in the last logic state.

For the applications that must force the outputs of the receivers to a known state, but still maintain low power consumption, the cable can be terminated as in Figure 24. A capacitor (typically 0.1µF) has been connected in series with the 120Ω termination resistor R2 and two bias resistors (R1 and R3) have been added. When data is being transmitted the capacitor looks basically like a short circuit and a differential signal is developed across the termination resistor. When the drivers are forced into a high impedance state, the bias resistors force the receiver into a logic 1 state. The receiver inputs can be reversed when the output must be a logic 0.

Because the capacitor is in series with the bias string, no DC current flows when data is not being transmitted. Care must be taken to transmit data at a high enough rate to prevent the bias resistors from charging the capacitor to the wrong state before the next data bit arrives. Also note that differences in the V^+ supplies or grounds will cause DC current to flow in the cable, but this can be kept to a minimum by using high value bias resistors.

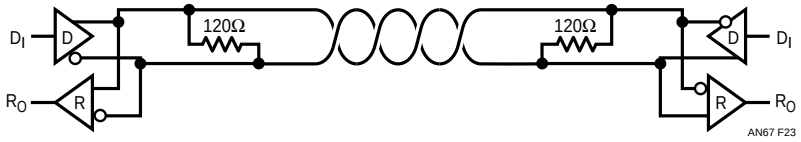


Figure 23. DC Coupled Termination

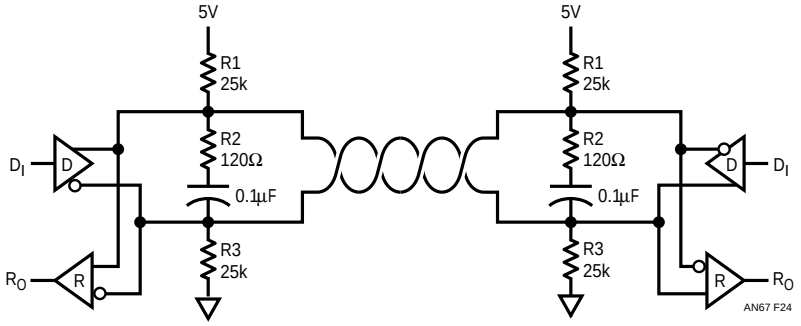


Figure 24. AC Coupled Termination

Filters

SALLEN AND KEY FILTERS USE 5% VALUES

by Dale Eagar

Lowpass filters designed after Sallen and Key usually take the form shown in Figure 25. In the classic Sallen and Key circuit, resistors R1, R2 and R3 are set to the same value to simplify the design equations.

When the three resistors are the same value, the pole placement, and thus the filter characteristics, are set by the capacitor values (C1, C2 and C3). This procedure, although great for the mathematician, can lead to problems. The problem is that, in the real world, the resistors, not the capacitors, are available in a large selection of values.

Taking advantage of the wider range of resistor values is not altogether trivial; the mathematics can be quite cumbersome and time consuming.

This Design Idea includes tables of resistor and capacitor values for third-order Sallen and Key lowpass filters. The resistor values are selected from the standard 5% value pool, and the capacitor values are selected from the standard 10% value pool. Frequencies are selected from the standard 5% value pool used for resistors. Frequencies are in Hertz, capacitance in Farads and resistance in Ohms.

Figure 26 details the PSpice™ simulation of a 1.6kHz Butterworth filter designed from these tables.

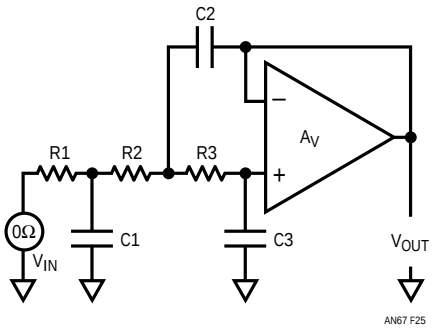


Figure 25. Sallen and Key Lowpass Filter

How to Design a Filter from the Tables:

Pick a cutoff frequency in Hertz as if it were a standard 5% resistor value in Ohms. (that is, if you want a cutoff frequency of 1.7kHz you must choose between 1.6k and 1.8k)

Select the component values from Table 1 or Table 2 as listed for the frequency (think of the first two color bands on a resistor).

Select a scale factor for the resistors and capacitors from Table 3 by the following method:

1. Select a diagonal that represents the frequency multiplier (think of the third color band on a 5% resistor).
2. Choose a particular diagonal box by either choosing a capacitor multiplier from the rows of the table that give you a desired capacitor value or by choosing a resistor multiplier from the columns of the table that gives you a desired resistance value.

Multiply the resistors and capacitors by the scale factors for the rows and columns that intersect at the chosen frequency multiplier box. (for example, 0.68 • 1µF = 0.68µF, 0.47 • 1kΩ = 470Ω).

PSpice is a trademark of MicroSim Corporation.

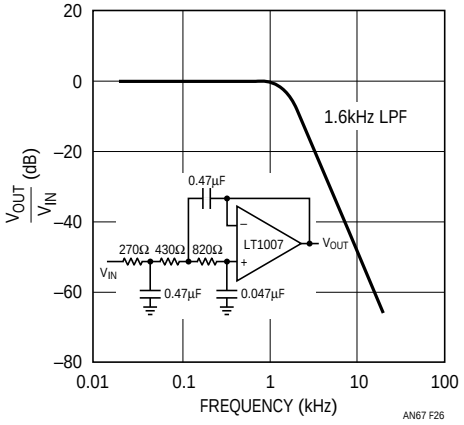


Figure 26. PSpice Simulation of 1.6kHz Butterworth Filter

Table 1. Bessel Lowpass Filter

FREQ	R1	R2	R3	C1	C2	C3
1.0	0.39	0.43	8.20	0.47	0.22	0.01
1.1	0.36	0.39	7.50	0.47	0.22	0.01
1.2	0.33	0.36	6.80	0.47	0.22	0.01
1.3	0.36	2.40	0.033	0.22	2.20	0.047
1.5	0.33	4.70	0.012	0.22	4.70	0.022
1.6	0.30	0.10	0.240	0.47	2.20	0.047
1.8	0.30	3.30	5.10	0.22	0.022	0.010
2.0	0.27	0.51	0.027	0.22	2.20	0.100
2.2	0.24	2.70	0.43	0.22	0.10	0.022
2.4	0.22	2.70	3.60	0.22	0.022	0.010
2.7	0.27	0.43	1.30	0.22	0.10	0.022
3.0	0.18	0.82	0.16	0.22	0.22	0.047
3.3	0.15	0.056	1.00	0.47	1.00	0.010
3.6	0.18	0.16	0.022	0.22	2.20	0.100
3.9	0.15	1.50	2.20	0.22	0.022	0.010
4.3	0.13	0.22	0.013	0.22	2.20	0.100
4.7	0.20	0.12	1.20	0.22	0.22	0.010
5.1	0.18	0.068	0.039	0.22	2.20	0.047
5.6	0.20	1.10	0.036	0.10	0.47	0.022
6.2	0.15	0.091	0.91	0.22	0.22	0.010
6.8	0.16	0.91	0.03	0.10	0.47	0.022
7.5	0.15	1.80	0.27	0.10	0.047	0.010
8.2	0.10	0.12	1.00	0.22	0.10	0.010
9.1	0.13	0.56	0.12	0.10	0.10	0.022

Table 2. Butterworth Lowpass Filter

FREQ	R1	R2	R3	C1	C2	C3
1.0	0.36	3.3	3.3	0.47	0.10	0.022
1.1	0.47	0.47	6.2	0.47	0.47	0.010
1.2	0.36	0.62	1.0	0.47	0.47	0.047
1.3	0.27	2.00	0.33	0.47	0.47	0.047
1.5	0.24	1.60	0.3	0.47	0.47	0.047
1.6	0.27	0.43	0.82	0.47	0.47	0.047
1.8	0.43	1.20	0.13	0.22	1.00	0.047
2.0	0.36	7.50	0.18	0.22	0.47	0.010
2.2	0.24	0.24	3.00	0.47	0.47	0.010
2.4	0.33	0.91	0.043	0.22	2.20	0.047
2.7	0.27	5.60	0.062	0.22	1.00	0.010
3.0	0.24	5.10	0.056	0.22	1.00	0.010
3.3	0.22	1.60	0.30	0.22	0.22	0.022
3.6	0.22	0.56	0.068	0.22	1.00	0.047
3.9	0.24	0.39	0.68	0.22	0.22	0.022
4.3	0.18	0.51	0.024	0.22	2.20	0.047
4.7	0.16	1.30	0.039	0.22	1.00	0.022
5.1	0.16	0.36	0.051	0.22	1.00	0.047
5.6	0.13	1.10	0.033	0.22	1.00	0.022
6.2	0.13	0.36	0.016	0.22	2.20	0.047
6.8	0.24	1.60	0.33	0.10	0.10	0.010
7.5	0.12	0.30	1.20	0.22	0.10	0.010
8.2	0.12	0.11	0.024	0.22	2.20	0.047
9.1	0.18	1.50	0.091	0.10	0.22	0.010

Table 3. Frequency Multipliers

	0.1Ω	1Ω	10Ω	100Ω	1k	10k	100k	1M	10M	100M
1F	10	1	0.1	0.001	—	—	—	—	—	—
0.1F	100	10	1	0.1	0.01	0.001	—	—	—	—
10,000µF	1k	100	10	1	0.1	0.01	0.001	—	—	—
1,000µF	10k	1k	100	10	1	0.1	0.01	0.001	—	—
100µF	100k	10k	1k	100	10	1	0.1	0.01	0.001	—
10µF	1M	100k	10k	1k	100	10	1	0.1	0.01	0.001
1µF	10M	1M	100k	10k	1k	100	10	1	0.1	0.01
0.1µF	100M	10M	1M	100k	10k	1k	100	10	1	0.1
0.01µF	1G	100M	10M	1M	100k	10k	1k	100	10	1
1,000pF	—	1G	100M	10M	1M	100k	10k	1k	100	10
100pF	—	—	1G	100M	10M	1M	1OOk	10k	1k	100

LOW POWER SIGNAL DETECTION IN A NOISY ENVIRONMENT

by Philip Karantzalis and Jimmylee Lawson

Introduction

In signal detection applications where a small narrowband signal is to be detected in the presence of wideband noise, one can design an asynchronous (nonphase sensitive) tone detector using an ultraselective bandpass filter, such as the LTC1164-8. The ultranarrow passband of the LTC1164-8 filter band limits any random noise and increases the detector's signal sensitivity.

The LTC1164-8 is an eighth-order, elliptic bandpass filter with the following features: the filter's f_{CENTER} (the center frequency of the filter's passband) is clock tunable and is equal to the clock frequency divided by 100; the filter's passband is from $0.995f_{CENTER}$ to $1.005f_{CENTER}$ (±0.5% from f_{CENTER}). Figure 27 shows a typical LTC1164-8 passband response and the area of passband gain variation. Outside the filter's passband, signal attenuation increases to more than 50dB for frequencies between $0.96f_{CENTER}$ and $1.04f_{CENTER}$. Quiescent current is typically 2.3mA with a single 5V power supply.

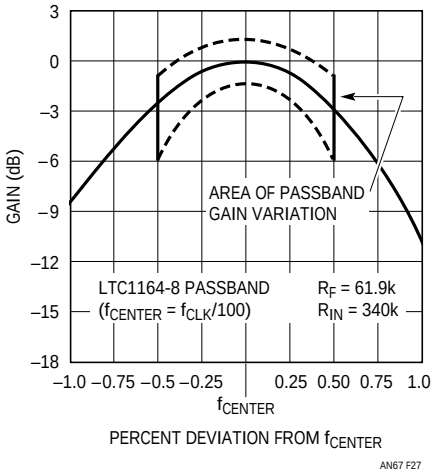


Figure 27. Detail of LTC1164-8 Passband

An Ultraselective Bandpass Filter and a Dual Comparator Build a High Performance Tone Detector

The LTC1164-8 has excellent selectivity, which limits the noise that passes from the input to the output of the filter. As a result, one can build a tone detector that can extract small signals from the "mud." Figure 28 shows the block diagram of such a tone detector. The detector's input is an LTC1164-8 bandpass filter whose output is AC coupled to a dual comparator circuit. The first comparator converts the filter's output to a variable pulsewidth signal. The pulsewidth varies depending on the signal amplitude. The average DC value of the pulse signal is extracted by a lowpass RC filter and applied to the second comparator. The identification of a tone is indicated by a logic high at the output of the second comparator.

One of the key benefits of using a high selectivity bandpass filter for tone detection is that when wideband noise (white noise) appears at the input of the filter, only a small amount of input noise will reach the filter's output. This results in a dramatically improved signal-to-noise ratio at the output of the filter compared to the signal-to-noise at the input of the filter. If the output noise of the LTC1164-8 is neglected, the signal-to-noise ratio at the output of the filter divided by the signal-to-noise ratio at the input of the filter is:

$$\frac{(S/N)_{OUT}}{(S/N)_{IN}} = 20\ \text{Log}\ \sqrt{\frac{(BW)_{IN}}{(BW)_f}}$$

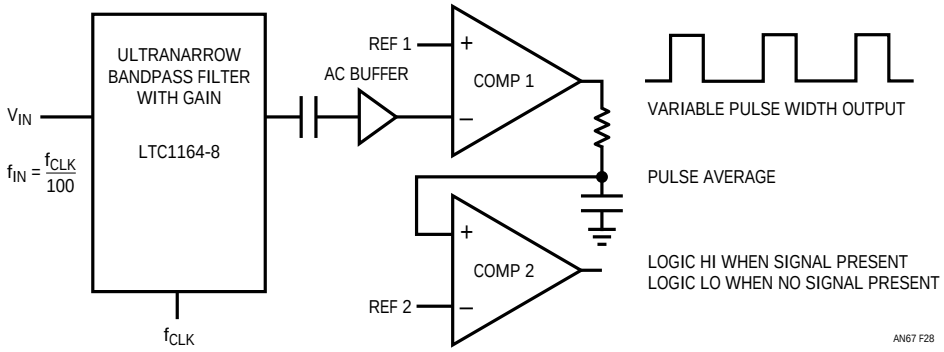


Figure 28. Tone Detector Block Diagram

where: $(BW)_{IN}$ = the noise bandwidth at the input of the filter and $(BW)_f = (0.01)(f_{CENTER})$ is the filter's noise equivalent bandwidth.

For example, a small 1kHz signal is sent through a cable that is also conducting random noise with a 3.4kHz bandwidth. An LTC1164-8 is used to detect the 1kHz signal. The signal-to-noise ratio at the output of the filter is 25.3db larger than the signal-to-noise ratio at the input of the filter:

$$\sqrt{\frac{(BW)_{IN}}{(BW)_f}} = 20\ \text{Log}\ \sqrt{\frac{3.4\text{kHz}}{(0.01)(1\text{kHz})}} = 25.3\text{dB}$$

Figure 29 shows the complete circuit for a 1kHz tone detector operating with a single 5V supply. An LTC1164-8 with a clock input set at 100kHz sets the tone detector's frequency at 1kHz ($f_{CENTER} = f_{CLK}/100$). A low frequency op amp (LT1013) and resistors R_{IN} and R_F set the filter's gain. In order to minimize the filter's output noise and maintain optimum dynamic range, the output feedback resistor R_F should be 61.9k. Capacitor C_F across resistor R_F is added to reduce the clock feedthrough at the filter's output.

To set the gain for the LTC1164-8, R_{IN} should be calculated by the equation:

R_{IN} = 340k/Gain

In Figure 29, the filter's gain is 10 (R_{IN} = 34k). Capacitor C1 and a unity-gain op amp (LT1013) AC couple the signal at the filter's output to an LTC1040 dual low power comparator. AC coupling is required to eliminate any DC offset caused by the LTC1164-8.

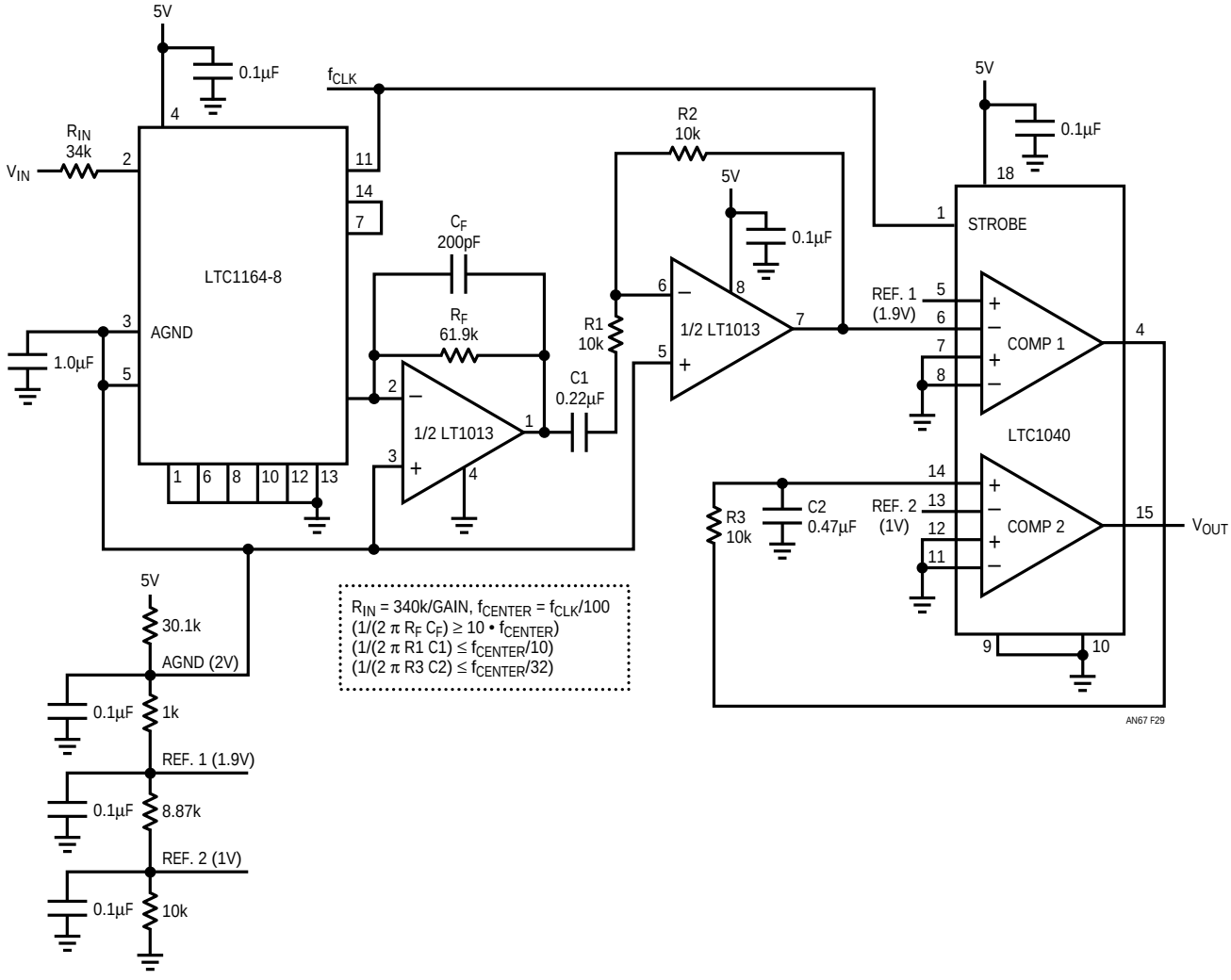


Figure 29. 1kHz Tone Detector with Gain of 10

A resistive divider generates a 2V bias for the LTC1164-8 "ground" (Pins 3 and 5) and the positive input of the LT1013 dual op amps. For single 5V operation the output swing of the LTC1164-8 is from 0.5V to 3.5V, centered at 2V. The divider also provides the reference voltages for the LTC1040 dual comparators (Ref. 1 = 1.9V and Ref. 2 = 1V). Power supply variations do not affect the performance of this circuit because all DC reference voltages are derived from the same resistor divider and will track any changes in the 5V power supply.

Theory of Operation

The tone detector works by looking at the negative peaks at the output of the filter. Signals below 1.9V at the output of the filter trip the first comparator. The second comparator has a 1V reference and detects the average value of the output of the first comparator. The R3/C2 time constant is set to allow detection only if the duty cycle of the first comparator's output exceeds 25%. Waveforms with duty cycles below 25% are arbitrarily assumed to carry false information

The circuitry is designed so that two or more negative signal peaks of 160mV at the filter's output produce a 25% duty cycle pulse waveform at the output of the first detector (the 1.9V and 1V references for comparators 1 and 2 respectively, set the $160mV_{PEAK}$ and the 25% duty cycle). The 25% duty cycle requirement establishes an operating point or "minimum detectable signal" for the detector circuit. Thus, the circuitry outputs a "tone present" condition only when the duty cycle is greater than or equal to 25%. The 25% duty cycle requirement sets two conditions for optimum tone detection at the detector's input.

The first input condition is the maximum input noise spectral density that will not trigger the detector's output to indicate the presence of a tone. When only noise is present at the filter's input, the maximum input noise spectral density is conservatively defined as the amount required to produce noise peaks at the filter's output of 160mV or lower amplitude. The 160mV maximum noise peak specification at the filter's output can be converted to output noise in mV_{RMS} by using a crest factor of 5 (the crest factor of a signal is the ratio of its peak value to its RMS value—a theoretical crest factor of 5 predicts 99.3% of the maximum peaks of wideband noise with uniform spectral density). Therefore, the maximum allowable noise at the filter's output is $32mV_{RMS}$ ($160mV_{PEAK}/5$). The noise at the filter's output depends on the filter's gain and noise equivalent bandwidth and the spectral density of the noise at the filter's input. Therefore, the maximum input noise spectral density for Figure 3's circuit is:

$$e_{IN} \leq 32mV_{RMS}/(Gain \bullet \sqrt{(BW)_f}) \frac{V_{RMS}}{\sqrt{Hz}}$$

where: Gain is the filter's gain at its center frequency and $(BW)_f$ is the filter's noise equivalent bandwidth.

Note: Compared to $32mV_{RMS}$ the $270mV_{RMS}$ output noise of the LTC1164-8 is negligible. The output noise of the LTC1164-8 is independent of the chosen filter signal gain.

The second input condition is the minimum input signal required so that a tone can be detected when it is buried by the maximum noise, as defined by the first input condition. When a tone plus noise is present at the filter's input, the output of the filter will be a tone whose amplitude is modulated by the bandlimited noise at the filter's output. If a maximum noise peak of 160mV modulates the tone's amplitude, a 320mV tone peak at the filter's output can be detected because the product of the noise and the tone crosses the (negative) $160mV_{PEAK}$ detection threshold and the 25% duty cycle requirement is exceeded. Therefore, a conservative value for the minimum signal at the filter's output can be set to $320mV_{PEAK}$ or $226mV_{RMS}$, but a value of $200mV_{RMS}$ was established experimentally. Therefore, the minimum input signal for reliable tone detection in the presence of the maximum input noise spectral density is:

$$V_{IN(MIN)} = 200mV_{RMS}/Gain$$

For optimum tone detection, the signal's frequency should be in the filter's passband, within $\pm 0.1\%$ of f_{CENTER}.

Conclusion

A very selective bandpass filter, the LTC1164-8, can be configured as a nonphase-sensitive tone detector. This allows signals to be detected in the presence of comparatively large amounts of noise or signal-to-noise ratios that are less than unity.

BANDPASS FILTER HAS ADJUSTABLE Q
by Frank Cox

The bandpass filter circuit shown in Figure 30 features an electronically controlled Q. Q for a bandpass filter is defined as the ratio of the 3dB pass bandwidth to the stop bandwidth at some specified attenuation. The center frequency of the bandpass filter in this example is 3MHz, but this can be adjusted with appropriate LC tank components. The upper limit of the usable frequency range is about 10MHz. The width of the passband is adjusted by the current into Pin 5 (set current or I_{SET}) of the transconductance amplifier segment of IC1, an LT1228. Figure 31 is a network analyzer plot of frequency response versus set current. This plot shows the variation in Q while the center frequency and the passband gain remain relatively constant.

The circuit's operation is best understood by analyzing the closed-loop transfer function. This can be written in the form of the classic negative feedback equation:

$$H(s) = \frac{A(s)}{1 + A(s)\,B(s)}$$

where A(s) is the forward gain and B(s) is the reverse gain. The forward gain is the product of the transconductance stage gain (g_m) and the gain of the CFA (A_{CFA}). For this circuit, g_m is ten times the product of I_{SET} and the impedance of the tank circuit as a function of frequency. This gives the complete expression for the forward gain as a function of frequency:

$$A(s) = 10\, I_{SET}\, A_{CFA}\left(\frac{sL}{1 + s^2\, LC}\right)$$

The reverse gain is simply:

$$B(s) = \frac{R7}{R6 + R7}$$

$$\text{and } A_{CFA} = \frac{R4 + R5}{R4}$$

$$\text{Setting } B(s) = \frac{1}{A_{CFA}}\, R_{RATIO}$$

and substituting these expressions into the first equation gives:

$$H(s) = \frac{1}{R_{RATIO}} \frac{10\, I_{SET}\left(\frac{sL}{1 + s^2\, LC}\right)}{1 + 10\, I_{SET}\left(\frac{sL}{1 + s^2\, LC}\right)}$$

The last equation can be rewritten as:

$$H(s) = \frac{1}{R_{RATIO}} \frac{S\left[\frac{1}{\sqrt{LC}}\left(\frac{10\, I_{SET}\sqrt{LC}}{C}\right)\right]}{S^2 + S\left[\frac{1}{\sqrt{LC}}\left(\frac{10\, I_{SET}\sqrt{LC}}{C}\right)\right] + \frac{1}{LC}}$$

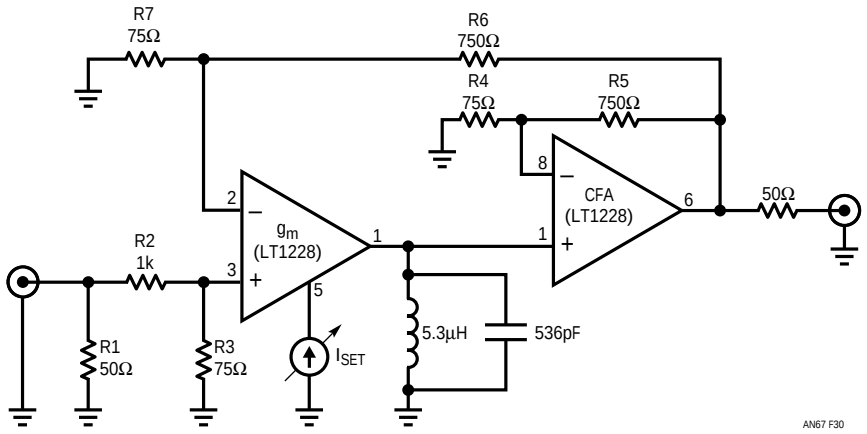


Figure 30. LT1228 Bandpass Filter Circuit Diagram

The transfer function of a second order bandpass filter can be expressed in the form[1]:

$$H(s) = H_{BP} \frac{S\,(\omega_O/Q)}{S^2 + S\,(\omega_O/Q) + \omega_O{}^2}$$

Comparing the last two equations note that

$$\omega_O = \frac{1}{\sqrt{LC}} \text{ and } \frac{1}{Q} = \frac{10\ I_{SET}\ \sqrt{LC}}{C}$$

$$\text{And therefore } Q = \frac{C}{10\ I_{SET}\ \sqrt{LC}}$$

It can be seen from the last equation that the Q is inversely proportional to the set current.

Many variations of the circuit are possible. The center frequency of the filter can be tuned over a small range by the addition of a varactor diode. To increase the maximum realizable Q, add a series LC network tuned to the same frequency as the LC tank on Pin 1 of IC1. To lower the minimum obtainable Q, add a resistor in parallel with the tank circuit. To create a variable Q notch filter, connect the inductor and capacitor at Pin 1 in series rather than in parallel.

A variable Q bandpass filter can be used to make a variable bandwidth IF or RF stage. Another application for this circuit is as a variable-loop filter in a phase locked loop phase demodulator. The variable Q bandpass filter is set for a wide bandwidth while the loop acquires the signal and is then adjusted to a narrow bandwidth for best noise performance after lock is achieved.

[1]Thanks to Doug La Porte for this equation hack.

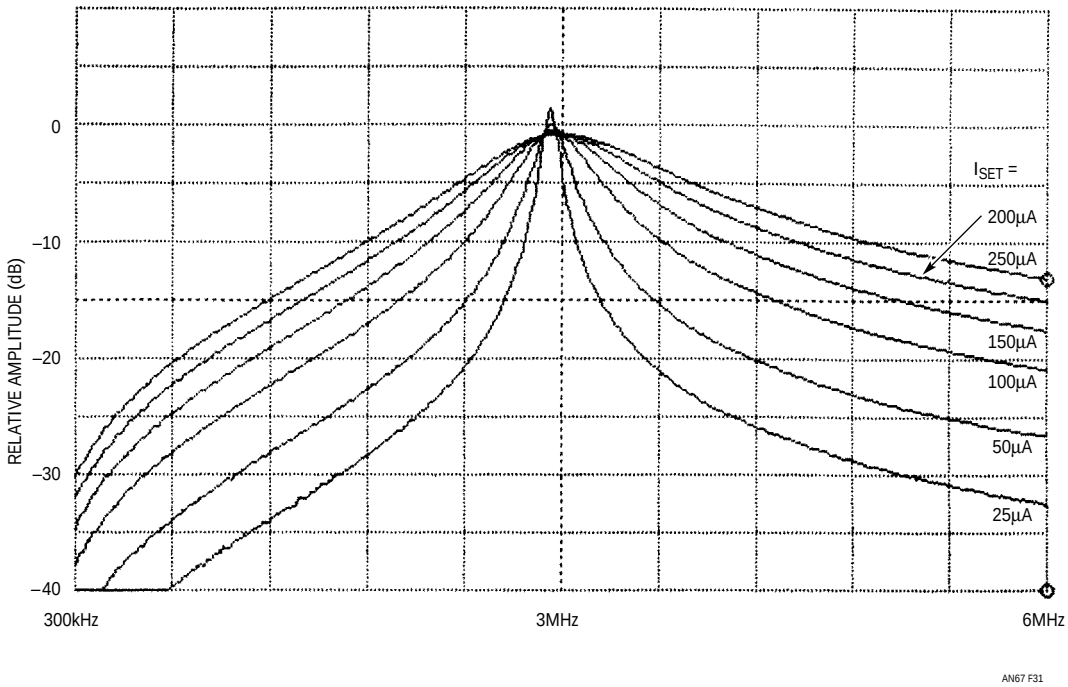


Figure 31. Network Analyzer Plot of Frequency Response vs "Set" Current

AN ULTRASELECTIVE BANDPASS FILTER WITH ADJUSTABLE GAIN

by Philip Karantzalis

Introduction

The LTC1164-8 is a monolithic, ultraselective, eighth order elliptic bandpass filter. The passband of the LTC1164-8 is tuned with an external clock; the clock-to-center-frequency ratio is 100:1. The stopband attenuation of the LTC1164-8 is greater than 50dB for input frequencies outside a narrow band defined as ±4% of the center frequency of the filter (see Figure 32).

One Op Amp and Two Resistors Build an Ultraselective Filter

The LTC1164-8 requires an external op amp and two external resistors. The filter's gain at its center frequency is equal to $3.4R_F/R_{IN}$. For optimum dynamic range with a gain equal to one, the external resistor R_F should be 90.9k and the external resistor R_{IN} should be 340k. For gains other than 1, R_{IN} = 340k/gain. Gains of up to 1000 are possible. The complete configuration is shown in Figure 33. Note that programming the filter's gain with input resistor R_{IN} is equivalent to providing the LTC1164-8 with noiseless preamplification, since the filter's internal noise is not amplified. The wideband noise of the LTC1164-8 measures $400\mu V_{RMS}$ at ±5V and is independent of the filter's gain and center frequency. A capacitor, C_F, across resistor R_F reduces clock feedthrough and provides a smooth sine wave output.

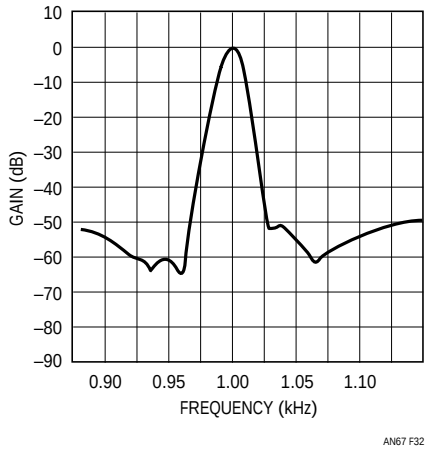


Figure 32. LTC1164-8 Gain vs Frequency Response

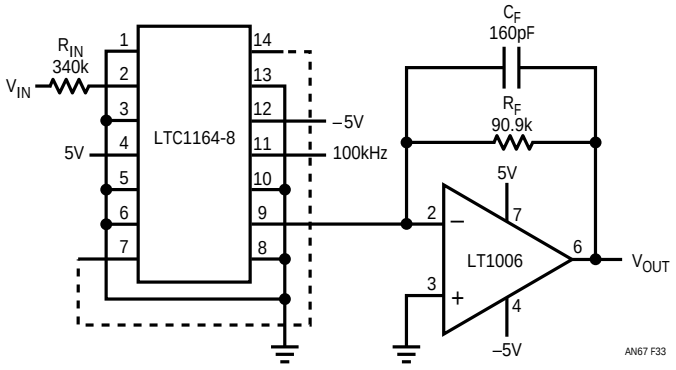


Figure 33. LTC1164-8 Ultranarrow, 1kHz Bandpass Filter with Gain (Gain = $340k/R_{IN}$, $1/2\pi R_F C_F = 10\ f_{CENTER}$)

Signal Detection in a Hostile Environment

An outstanding feature of the LTC1164-8 is its ultraselectivity. A bandpass filter with ultraselectivity is ideal for signal detection applications. One signal detection application occurs when two signals are very closely spaced in the frequency spectrum and only one of the signals has useful information. The LTC1164-8 can extract the signal of interest and suppress its unwanted neighbor. For example, a small 1kHz, $10mV_{RMS}$ signal is combined with an unwanted 950Hz, $40mV_{RMS}$ signal. The two signals differ in frequency by only 5% and the 950Hz signal is four times larger than the 1kHz signal. To detect the 1kHz signal, the LTC1164-8 is set to a gain of 100 and the clock frequency is set to 100kHz. At the filtered output of the LTC1164-8 the following signals will be present: an extracted 1kHz, $1V_{RMS}$ signal and a rejected 950Hz, $2.7mV_{RMS}$ signal, as shown in Figure 34. In a narrowband signal separation and extraction application, as described previously, the LTC1164-8 provides a simple and reliable detection circuit solution.

A second signal detection application occurs when a small signal is to be detected in the presence of noise. For example, a 1kHz, $10mV_{RMS}$ signal is mixed with a wideband noise signal that measures $5mV_{RMS}$ in a 400Hz frequency band. The signal-to-noise ratio is just 6dB. With the LTC1164-8 set for a center frequency of 1kHz (f_{CLK} is equal to 100kHz) and a gain of 100, the 1kHz, $10mV_{RMS}$ signal will be detected and amplified. The wideband noise will be band limited by the very narrow band gain response of the LTC1164-8. At the output of a LTC1164-8, the 1kHz signal will be $1V_{RMS}$ as shown in Figure 35. The total band limited

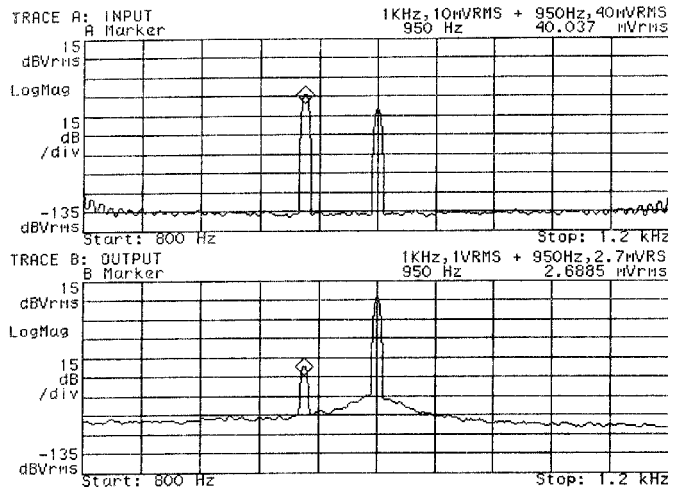


Figure 34. Narrow Band Signal Extraction Showing Input to and Output from the LTC1164-8 Filter. Filter f_{CENTER} set to 1kHz with Gain = 100

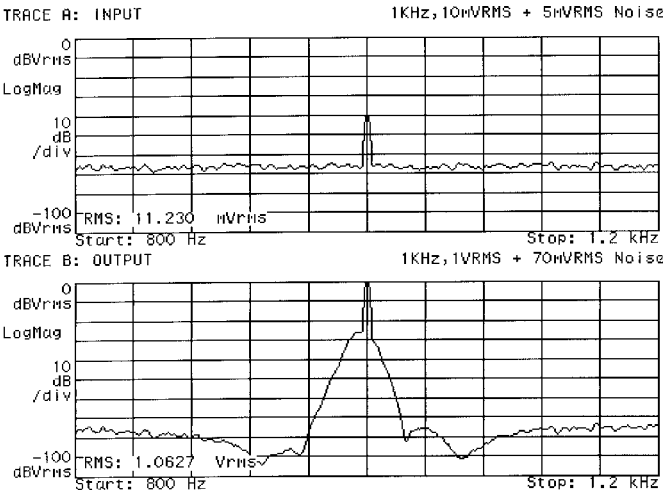


Figure 35. Signal Detection in the Presence of Noise Example Showing Input to and Output from the LTC1164-8 Filter. Filter f_{CENTER} set to 1kHz with Gain = 100

noise will be 70mV_{RMS} with a signal-to-noise ratio of more than 20dB, as shown in Figure 36. In applications of signal detection in the presence of noise, the LTC1164-8 provides asynchronous detection. Signal detection circuits such as synchronous demodulators and lock-in amplifiers require the presence of a reference or carrier signal to provide phase and frequency information of the signal to be detected. With an LTC1164-8, signal detection is accomplished by selecting a very narrow signal detection band around the frequency of the desired signal, which is defined as f_{CLK} divided by 100 (f_{CLK} is the clock frequency of the LTC1164-8), and by selecting the filter gain by choosing the value of a resistor.

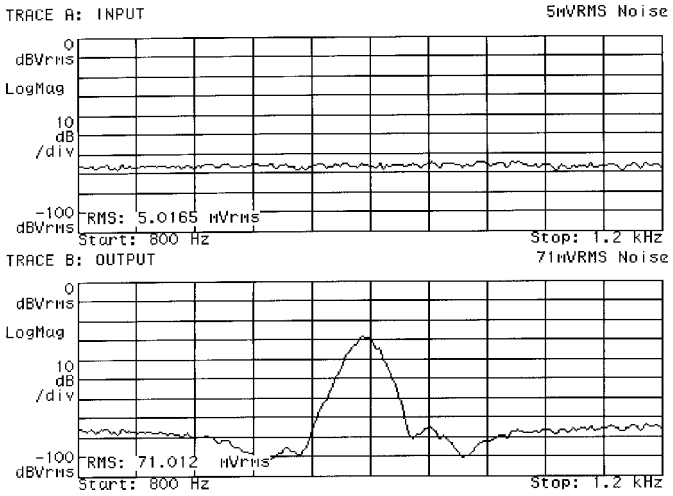


Figure 36. Wideband Noise Input to LTC1164-8 Filter. Plots Show Input to and Output from the Filter. Filter f_{CENTER} set to 1kHz with Gain = 100

LT1367 BUILDS RAIL-TO-RAIL BUTTERWORTH FILTER

by William Jett and Sean Gold

Single Supply 1kHz, 4th Order Butterworth Filter

The circuit shown in Figure 37 takes advantage of all four op amps in the LT1367 to form a 4th order Butterworth filter. The filter is a simplified state-variable architecture consisting of two cascaded second order sections. Each section uses the 360 degree phase shift around the two op amp loop to create a negative summing junction at A1's positive input.[1] The circuit has two-thirds the power dissipation and component count as the classic three op amp biquad,[2] yet it has the same low component sensitivities for center frequency, ω_0 and Q.

For cutoff frequencies other than the 1kHz example shown, use the following formula for each section:

$\omega_0^2 = 1/(R1\ C1\ R2\ C2)$,

where $R1 = 1/(\omega_0\ Q\ C1)$ and $R2 = Q/(\omega_0 C2)$

The DC bias applied to A2 and A4 for single supply operation is not needed when split supplies are available. The circuit's output can swing rail-to-rail and displays the maximally flat amplitude response with a 1kHz cutoff frequency with 80dB/decade rolloff (Figure 38).

[1] Hahn, James. 1982. State Variable Filter Trims Predecessor's Component Count. *Electronics*, April 21, 1982.

[2] Thomas, L.C. 1971. The Biquad: Part I—Some Practical Design Considerations. *IEEE Transactions on Circuit Theory*, 3:350-357, May 1971.

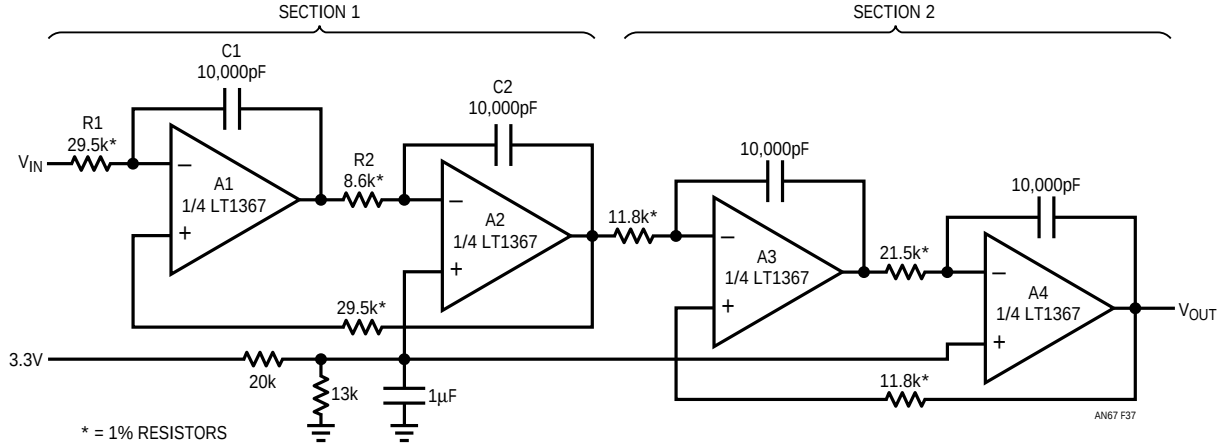


Figure 37. 1kHz 4th Order Butterworth Filter

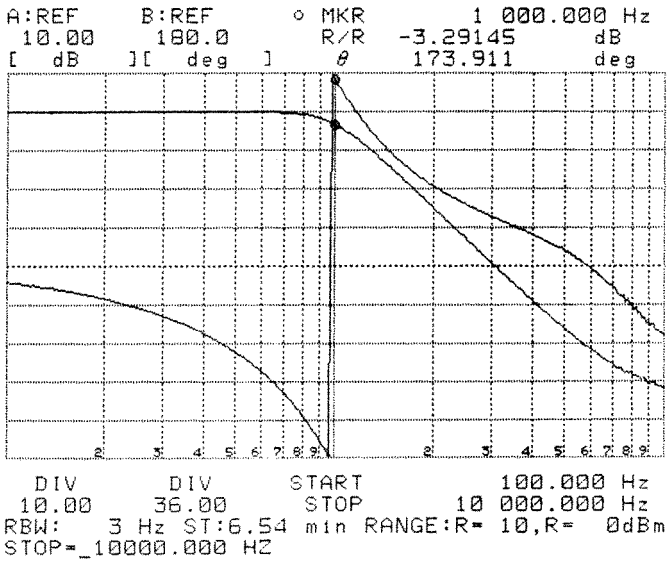


Figure 38. Frequency Response of 4th Order Butterworth Filter

DC ACCURATE, CLOCK TUNABLE LOWPASS FILTER WITH INPUT ANTIALIASING FILTER

by Philip Karantzalis

In a sampled data system, the sampling theorem says that if an input signal has any frequency components greater than one half the sampling frequency, aliasing errors will appear at the output. In practice aliasing is not always a serious problem. High order switched capacitor lowpass filters are band limited and significant aliasing occurs only for input signals centered around the clock frequency and its multiples.

Figure 39 shows the LTC1066-1 aliasing response when operated with a clock-to-f_C ratio of 50:1. With a 50:1 ratio, the LTC1066-1 samples its input twice during one clock period and the effective sampling frequency is twice the clock frequency. Figure 39 shows that the maximum aliased output is generated for inputs in the range of $2(f_{CLK} \pm f_C)$. (f_C is the cutoff frequency of the LTC1066-1.) For instance, if the LTC1066-1 is programmed to produce a cutoff frequency of 20kHz with a 1MHz clock, maximum aliasing will occur only for input signals in the narrow range of 2MHz ±20kHz and its multiples.

The simplest antialiasing filter is a passive 1st order lowpass RC filter. The –3dB frequency of the RC filter should be chosen so that the passband of the RC filter does not influence the passband of the LTC1066-1. When the LTC1066-1 clock frequency is 500kHz, an RC filter with the –3dB frequency set at 50kHz attenuates by 26dB any possible aliasing inputs in the range 1MHz ±10kHz. The passband shape of the 50kHz RC filter does not degrade the flat passband of the LTC1066-1 at 10kHz (the passband attenuation of the 50kHz RC filter for frequencies less than 10kHz is less than 0.2dB). If the LTC1066-1 is clock tuned to a cutoff frequency of 5kHz (with a clock frequency of 250kHz), the 50kHz RC filter will provide 20dB attenuation for aliasing inputs in the range of 500kHz ±5kHz. Therefore, a 1st order lowpass RC filter will attenuate all aliasing signals to the LTC1066-1 by a minimum of 20dB for a clock tunable range of one octave.

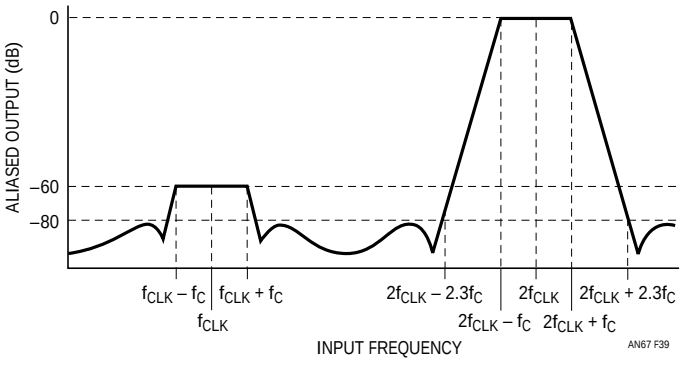


Figure 39. Aliasing vs Frequency f_{CLK}/f_C = 50:1 (Pin 8 to V^+); Clock is a 50% Duty Cycle Square Wave

For added antialiasing bandwidth, a 1st order lowpass RC filter can be tuned by the clock signal of LTC1066-1 to follow the cutoff frequency of the higher order filter. The circuit is shown in Figure 40. The circuit operation is as follows. The six comparators inside the LTC1045 detect the clock frequency. The clock signal of the LTC1066-1 is converted to a pulse output whose duty cycle changes with clock frequency. The average voltage of the pulse signal is delivered to a 4-window comparator whose outputs drive the four analog switches of the LTC202. When the LTC1066-1 clock frequency increases or decreases by more than one octave (2x or x/2), a capacitor is switched in or out of the 1st order lowpass filter formed by resistor R1 (1k) and capacitor C1. The –3dB frequency of the lowpass RC filter is therefore doubled or halved if the cutoff frequency of the LTC1066-1 is doubled or halved. Resistor R1 and capacitors C1 through C5 allow the lowpass RC filter to be tuned over a range of five octaves, providing at least 20dB attenuation to any LTC1066-1 input signals in the range $2(f_{CLK} \pm f_C)$ (the RC filter also attenuates all aliasing signals near any multiples of the clock frequency).

The circuit in Figure 40 can be used for any clock tunable, 5-octave range for cutoff frequencies from 10Hz to 80kHz (with ±5V supplies for LTC1066-1) or for cutoff frequencies as high as 100kHz (with ±8V supplies for the LTC1066-1). For cutoff frequencies greater than 50kHz, a 15pF capacitor in series with a 30k resistor should be connected between Pins 11 and 13 of the LTC1066-1 to minimize passband gain peaking.

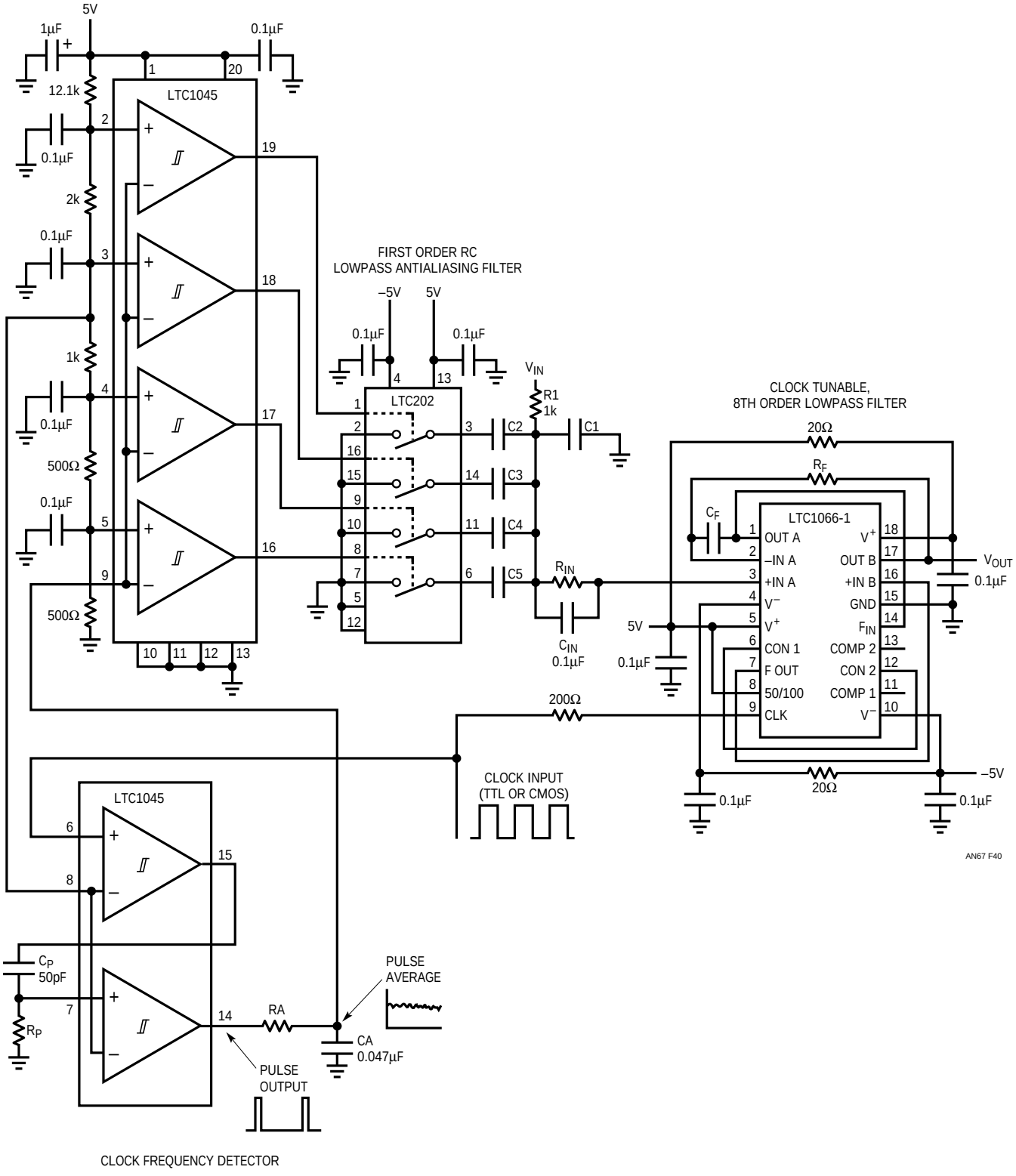


Figure 40. DC-Accurate, Clock-Tunable Lowpass Filter with Input Antialiasing

Use the following design guide for choosing the component values of R_A, R_P, R_F, R_{IN}, C_F, C1 through C5, C_P and C_A.

Definitions

1. The cutoff frequency of the LTC1066-1 is abbreviated as f_C.
2. $f_{C(LOW)}$ is the lowest cutoff frequency of interest
3. A range of five octaves is from $f_{C(LOW)}$ to 32 • $f_{C(LOW)}$

Component Calculations

$$\frac{1}{2\pi R_F C_F} = \frac{f_{C(LOW)}}{250}$$ $R_{IN} = R_F$ (If R_F can be chosen as 20k, R_{IN} and C_{IN} are not needed)

$$C1 = \frac{1}{f_{C(LOW)}}$$ ($f_{C(LOW)}$ in Hz); R1 = 1k

C2 = C1 ±5%, C3 = 2(C1) ±5%, C4 = 4(C1) ±5%, C5 = 8(C1) ±5%

$$C_P = 50pF,\ R_P = \frac{10^5}{50\ f_{C(LOW)}}\ k$$

$$C_A = 0.047\mu F,\ R_A = \frac{5(10^5)}{50\ f_{C(LOW)}}\ k$$

Example

For a five octave range from 1kHz to 32kHz:

$f_{C(LOW)}$ = 1kHz

Let C_F = 1µF ±20%, then R_F = 40.2k ±1%. $R_{IN} = R_F$ = 40.2k ±1%, C_{IN} = 0.1µF

C1 = 0.001µF ±5%, C2 = 0.001µF ±5%, C3 = 0.0022µF ±5%

C4 = 0.0039µF ±55, C5 = 0.0082µF ±5%

C_P = 50pF, R_P = 2k, C_A = 0.047µF, R_A = 10k

THE LTC1066-1 DC ACCURATE ELLIPTIC LOWPASS FILTER

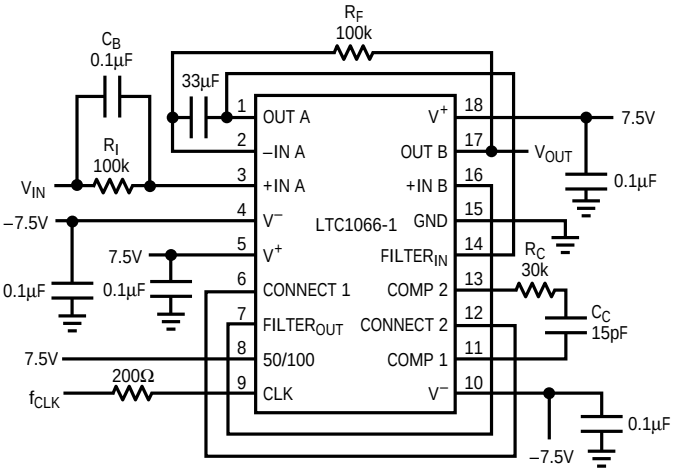
by Nello Sevastopoulos

Figure 41 shows an application allowing clock tunability from 10Hz to 100kHz. The R_CC_C frequency compensating components (needed only for cutoff frequencies above 60kHz) maintain a flat passband for cutoff frequencies between 50kHz and 100kHz. The input resistor, R_I, reduces the output DC offset caused by the op amp bias current through the 100k feedback resistor, R_F. The measured DC offset and the gain nonlinearity are 4mV and ±0.0063% (84dB), respectively. The 0.1µF bypass capacitor, C_B, helps keep the total harmonic distortion of the filter from being degraded by the 100k input resistor.

Clock Tunability

An external clock tunes the cutoff frequency of the internal switched capacitor network. The device has been optimized for a clock-to-cutoff-frequency ratio of 50:1. The internal double sampling greatly reduces the risk of aliasing.

The maximum obtainable cutoff frequency, $f_{CUTOFF(MAX)}$, depends on power supply, clock duty cycle and temperature; $f_{CUTOFF(MAX)}$ does not depend on the value of the external resistor/capacitor combination R_FC_F. The R_CC_C compensation is shown in Figure 41. The data detailed in



MAXIMUM OUTPUT VOLTAGE OFFSET = 4mV, DC LINEARITY = ±0.0063%, T_A = 25°C.

THE PIN 6 TO 12 CONNECTION SHOULD BE UNDER THE IC AND SHIELDED BY AN ANALOG SYSTEM GROUND PLANE.

RC COMPENSATION BETWEEN PINS 11 AND 13 REQUIRED ONLY FOR f_{CUTOFF} > 50kHz.

THE 33µF CAPACITOR IS A NONPOLARIZED, ALUMINUM ELECTROLYTIC, ±20%, 16V (NICHICON UUPIC 330MCRIGS OR NIC NACEN 33M16V 6.3 × 5.5 OR EQUIVALENT).

AN67 F41

Figure 41. DC Accurate, 10MHz to 100kHz 8th Order Elliptic Lowpass Filter, f_{CLK}/f_C = 50:1

Figure 42 reveals the important fact that for a cutoff frequency of 100kHz, the stopband attenuation still remains greater than 70dB for input frequencies up to 1MHz.

The minimum obtainable cutoff frequency depends on the R_FC_F time constant of the servo loop. For a given R_FC_F time constant, the minimum obtainable cutoff frequency of the LTC1066-1 is:

$f_{CUTOFF(MIN)} = 250(1/2\pi R_FC_F)$.

$f_{CUTOFF(MAX)} = 100kHz$

For instance, if $R_F = 20k$, $C_F = 1\mu F$, $f_{CUTOFF(MIN)} = 2kHz$, and $f_{CLOCK(MIN)} = 100kHz$.

Under these conditions, a clock frequency below 100kHz will "warp" the passband gain by more than 0.1dB. Please see the LTC1066-1 data sheet for more details.

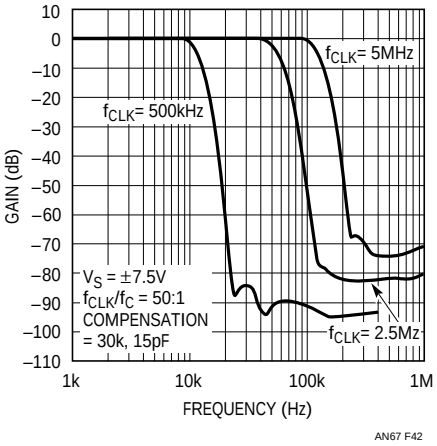


Figure 42. LTC1066-1 Amplitude vs Frequency

Dynamic Range

The LTC1066-1 wideband noise is $100\mu V_{RMS}$. Figure 43 shows the noise plus distortion versus RMS input voltage at 1kHz. With a ±5V supply, the filter can swing ±2.5V (5V full scale) with better than 0.01% distortion plus noise. The maximum signal-to-noise ratio, in excess of 90dB, is achieved with ±7.5V supplies. Unlike previous monolithic filters the data shown in Figure 43 is taken without using any input or output op amp buffers. The output buffer of the LTC1066-1 can drive a 200Ω load without dynamic range degradation.

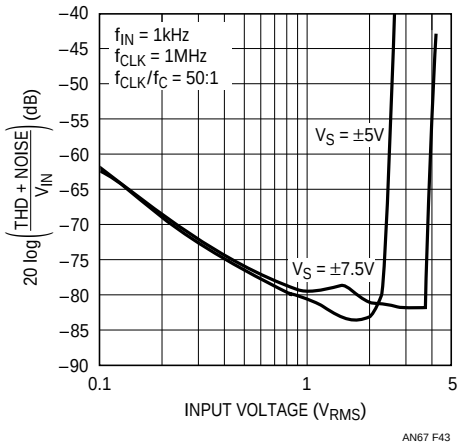


Figure 43. LTC1066-1 Dynamic Range

Aliasing and Antialiasing

All sampled data systems will alias if their input signals exceed half the sampling rate, but aliasing for high order, band limited, switched capacitor filters need not be a serious problem. The LTC1066-1, when operating with a 50:1 clock-to-cutoff-frequency ratio, will have significant aliasing only for input signals centered around twice the clock frequency and its even multiples. Figure 44 shows the input frequencies that will generate aliasing at the filter output. For instance, if the filter is tuned to a 50kHz cutoff frequency using a 2.5MHz clock, significant aliasing will occur only for input frequencies of 5MHz ±50kHz. The filter user should be aware of the spectrum at the input to the filter. Next, an assessment should be made as to whether a simple, continuous-time antialiasing filter in front of the LTC1066-1 is required. The antialiasing filter should do precisely what it is meant to do, that is, provide

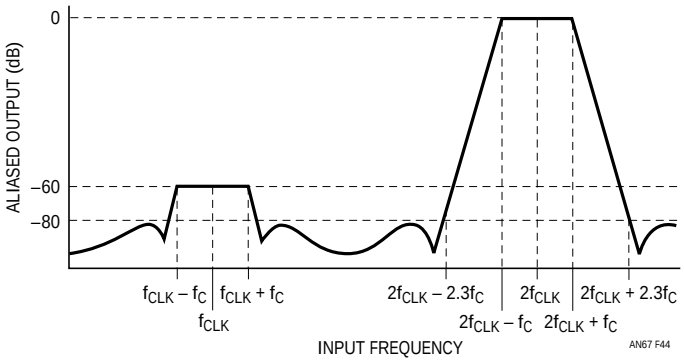


Figure 44. Aliasing vs Frequency f_{CLK}/f_C = 50:1 (Pin 8 to V^+). Clock is a 50% Duty Cycle Square Wave

band limiting. The antialiasing filter should not degrade the DC or AC performance of the LTC1066-1.

For fixed cutoff frequency applications, the antialiasing function is quite trivial. Figure 45 shows the internal precision input op amp configuration used to perform both the DC accurate function of the LTC1066-1 and the input antialiasing configuration. The cutoff frequency of the RC antialiasing filter is set three times higher than the cutoff frequency of the LTC1066-1. For the example shown in Figure 45 the input antialiasing filter provides a 62dB attenuation at twice the clock frequency of the switched capacitor filter.

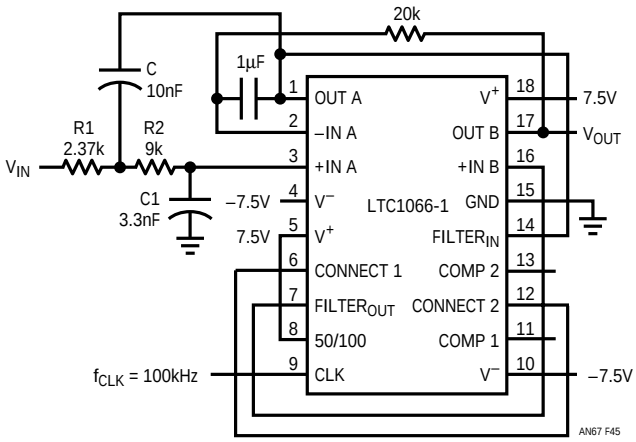
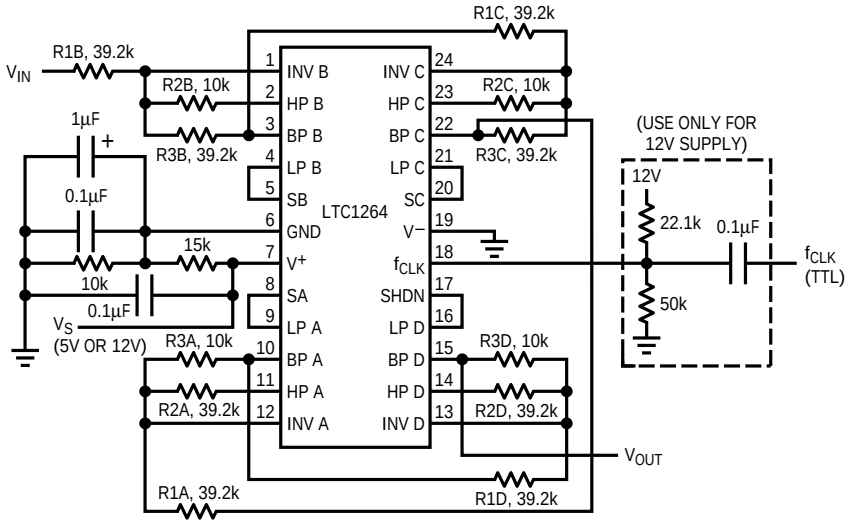


Figure 45. Adding a 2-Pole Butterworth Input Antialiasing Filter. Set C1 = 0.33C, R2 = 3.8(R1); f–3dB (Input Antialiasing) = 0.8993/(2πR1C)

CLOCK TUNABLE BANDPASS FILTER OPERATES TO 160kHz IN SINGLE SUPPLY SYSTEMS

by Philip Karantzalis

When the only available power supply in a system is 5V or 12V and a precision bandpass filter is needed at cutoff frequencies greater than 20kHz, the LTC1264 switched capacitor active filter building block can be configured to realize an 8th order bandpass filter accurate to ±1% or better over temperature (–40°C to 85°C). Figure 46 is a schematic diagram of an 8th order bandpass filter tunable with a TTL clock signal to any center frequency up to 70kHz with a 5V supply or to 100kHz with a 12V supply. The clock frequency-to-center frequency ratio is 20:1. The gain response for a 50kHz bandpass filter is shown in Figure 47 and the input dynamic range with a 5V supply is shown in Figure 48.



V_S	f_{CENTER}	R1 (EACH SECTION)
5V	80kHz	42.2k
5V	90kHz	47.5k
12V	120kHz	40.2k
12V	140kHz	42.2k
12V	160kHz	47.5k

Figure 46. Single Supply Bandpass Filter

The passband frequency range (the frequency range where the filter's attenuation is 3dB or less) is equal to the center frequency divided by ten. The stopband attenuation reaches 60dB at twice the center frequency and at one-half the center frequency. The typical gain variation at the center frequency is ±0.5dB at 25°C and ±1.5dB over temperature. (Note that an additional ±0.4dB should be added to account for the gain variation due to the 1% resistors). If the operating temperature range is 25°C (±20°C) and the power supply voltage can be controlled to ±2%, the center frequency can be extended to 90kHz for a 5V supply or 160kHz for a 12V supply. Note that the gain error for center frequencies greater than 70kHz with a 5V supply and greater than 100kHz with a 12V supply increases from 1dB to 7dB. Therefore, the value of resistor R1 for each LTC1264 section should be increased to reduce the error to ±1dB (see the table in Figure 46).

If the power supply for this filter is a switching regulator, the regulator's output noise can appear at the filter's output if the center frequency of the filter is tuned to the noise frequency of the regulator. This is due to the filter's low power supply rejection near its center frequency. The LTC1264 is not a low power device. The typical quiescent current is 11mA with a 5V supply or 18mA with a 12V supply.

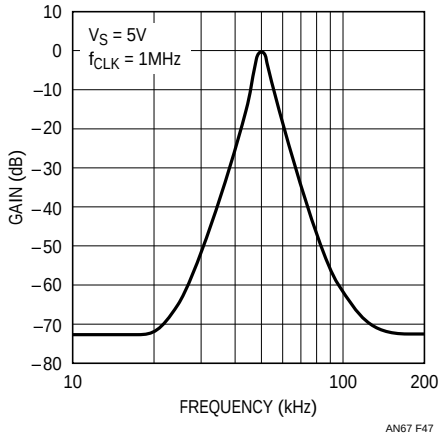


Figure 47. LTC1264 Single 5V Supply, 50kHz Bandpass Response

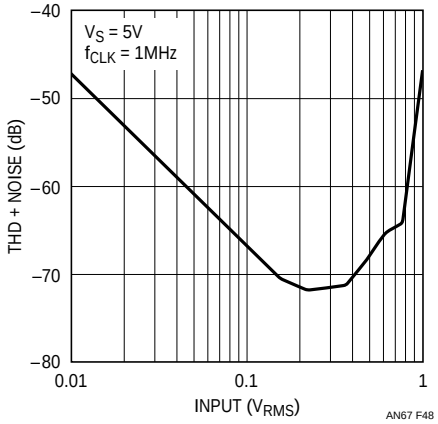


Figure 48. Dynamic Range vs Input Signal. LTC1264 Single 5V Supply, 50kHz Bandpass Filter

A LINEAR-PHASE BANDPASS FILTER FOR DIGITAL COMMUNICATIONS

By Philip Karantzalis

Bandpass filters with linear passband phase are useful for a variety of data-communications tasks, the most noteworthy of which may be in modulation-demodulation (modem) circuitry. Modems generate signals that must be processed without phase distortion to allow error free transmission and reception of information (or the closest approach to that ideal we can achieve).

Figure 49 shows a linear-phase bandpass filter using the LTC1264 high frequency, universal switched capacitor filter building block. This filter is an 8th order narrow bandpass filter, centered at 50kHz for a 1MHz clock input, with flat group delay in its passband. The f_{CLK}-to-f_{CENTER} frequency ratio is 20:1. Figure 50 shows the filter's narrowband gain response and Figure 51 shows the passband group delay.

An interesting feature of linear-phase bandpass filters is that their response to a step input produces a short transient sine wave burst with a symmetrical envelope. Figure 52 shows a comparison of the transient responses to a step input for the linear-phase bandpass filter of

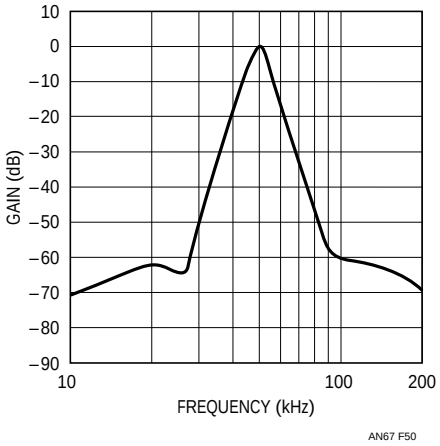


Figure 50. Filter Gain vs Frequency

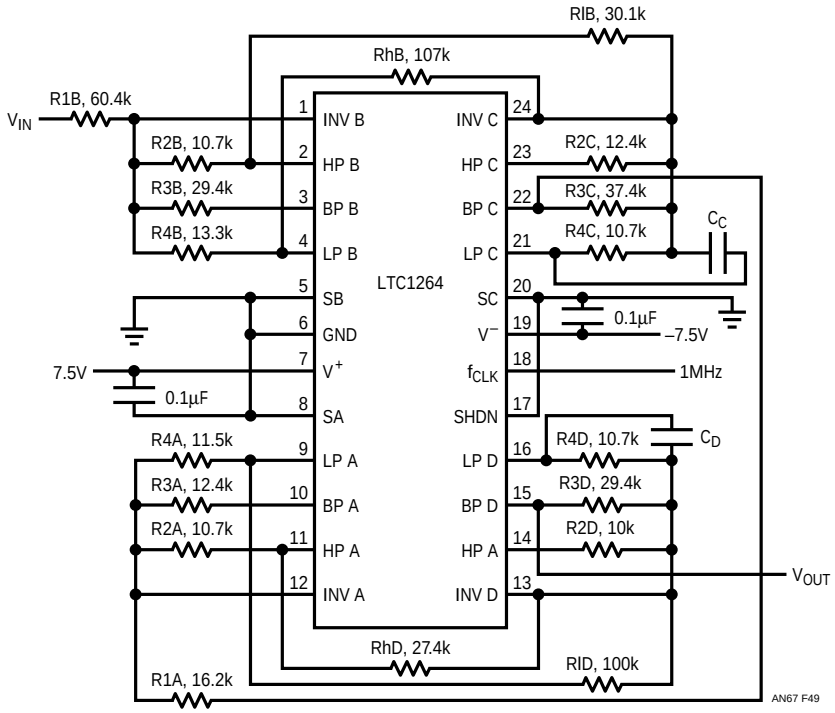


Figure 49. LTC1264 Linear Phase, 8th Order Bandpass Filter

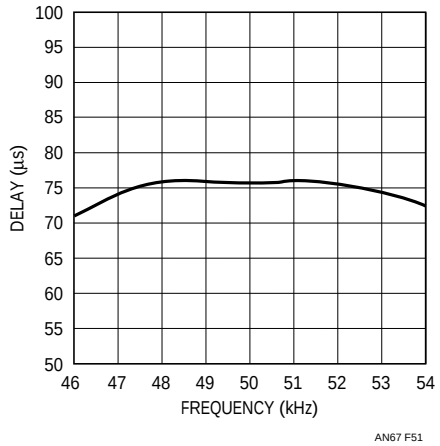


Figure 51. Filter Group Delay vs Frequency

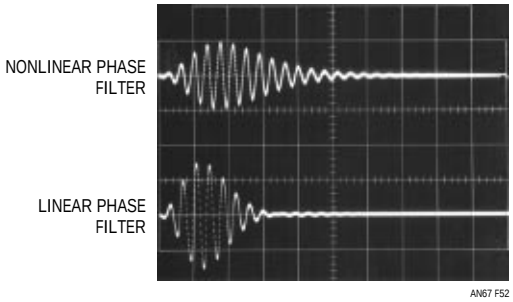


Figure 52. Step Response

Figure 49 and a bandpass filter with a similar passband and nonlinear phase response. The response of a bandpass filter to a step input is a simple qualitative test for determining the linearity of its phase response, although in data transmission systems the measurements are usually made with eye diagrams and constellation displays.

The maximum clock frequency for the filter is 2MHz with ±7.5V supplies. This allows bandpass filters with center frequencies up to 100kHz to be realized without significant phase distortion in the passband.

Capacitor C, across R4 in sections C and D, minimizes gain and phase variations when the filter is used with clock frequencies greater than 1.4MHz. For ±5V supplies the maximum clock frequency is 1.6MHz. Use the Table 1 as a guide for the selection of capacitor C.

Table 1. Capacitor Selection Guide

V_S	f_{CLK}	$C_C = C_D$
±7.5V	1.8MHz	3pF
	2.0MHz	5pF
±5V	1.6MHz	5pF
	1.4MHz	3pF

Instrumentation

WIDEBAND RMS NOISE METER

by Mitchell Lee

Recently, I needed to measure and optimize the wideband RMS noise of a power supply over about a 40MHz bandwidth. A quick calculation showed that the 12nV to 15nV/$\sqrt{Hz}$ noise floor of my spectrum analyzer would come up short—my circuit was predicted to exhibit a spot noise of perhaps 8nV to 10nV/$\sqrt{Hz}$. In fact, I didn't have a single instrument in my lab that would measure 50μV_{RMS} to 60μV_{RMS}.

For the 40MHz bandwidth, the HP3403C RMS voltmeter is a good choice but its most sensitive range is 100mV, about 66dB shy of my requirement. This obsolete instrument today carries a hefty price on the used market. The fact that here in the Silicon Valley HP3403Cs are a common sight at flea markets is of little consolation to most customers wishing to reproduce my measurements. We have several of these meters in the LTC design lab but they are in constant use and closely guarded by "The Keepers of the Secret RMS Knowledge." I resolved to build my own meter using an LT1088 thermal RMS converter.

Full scale on the LT1088 is 4.25V_{RMS}. To measure 50μV full scale, I'd need an amplifier with a gain of 100,000. At 40MHz bandwidth, this didn't sound like it would have a good chance of working first time—built by hand and without benefit of a custom casting.

Rather than build a circuit with 40MHz bandwidth and a gain of 100dB, I decided to use just enough gain to put my desired noise performance around twice minimum scale. Aside from gain, this amplifier would also need less than 5nV/$\sqrt{Hz}$ input noise, and the output stage would have to drive the 50Ω load presented by the LT1088.

It wasn't hard to find an appropriate output stage. The LT1206 (see Figure 53) can easily drive the required 120mA peak current into the LT1088 converter and there's plenty left over for handling noise spikes. To preserve 40MHz bandwidth, the LT1206 was set to run at a gain of 2.

The front end was harder to solve. I needed a low noise, high speed amplifier that could give me plenty of gain. Here I selected the LT1226. This is a 1GHz GBW op amp with only 2.6nV/$\sqrt{Hz}$ input noise. It has a minimum stable gain of 25 but in this circuit high gain is an advantage.

Cascading two LT1226s on the front end gives a gain of 625, a little shy of the 5,000 to 10,000 required. Another gain of 5, plus the gain of 2 in the LT1206 adds up to a gain of 6,250—just about right.

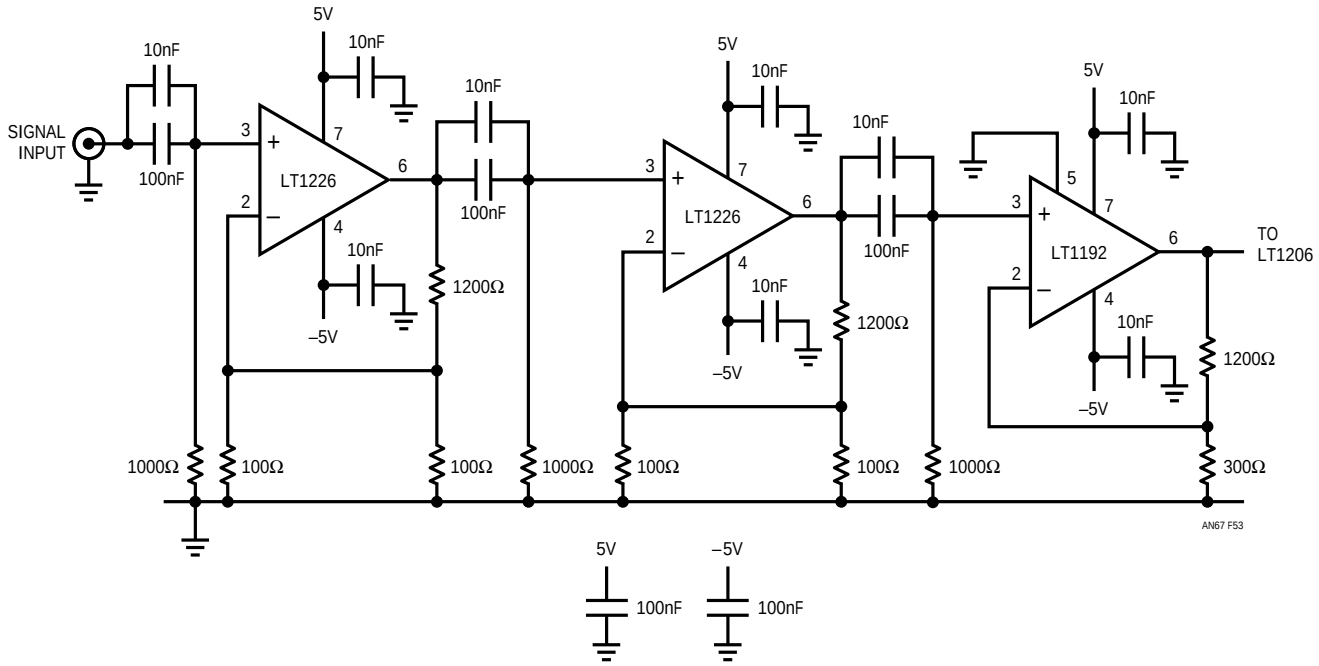


Figure 53 Noise Meter Gain Stage

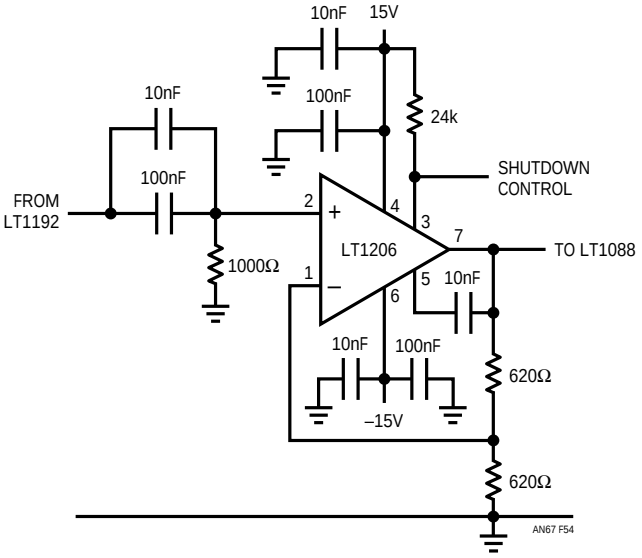


Figure 54. LT1206 Buffer/Driver Section

There are several ways to get 40MHz bandwidth at a gain of 5, including the LT1223 and LT1227 current feedback amplifiers, but I settled on the LT1192 voltage amplifier because it is the lowest cost solution. This brings the gain up to 6250, for a minimum scale sensitivity of 34μV_{RMS} and a full-scale sensitivity of 680μV_{RMS}.

My advice-filled coworkers assured me that there was no way I could build a wideband amplifier with a gain of 6250 and make it stable. Nevertheless, I built my amplifier on a 1.5" × 6" copperclad board, taking care to maintain a linear layout. The finished circuit was stable provided that a coaxial connection was made to the input. The amplifier was flat with 3dB points at 4kHz and 43MHz and some peaking at high frequencies.

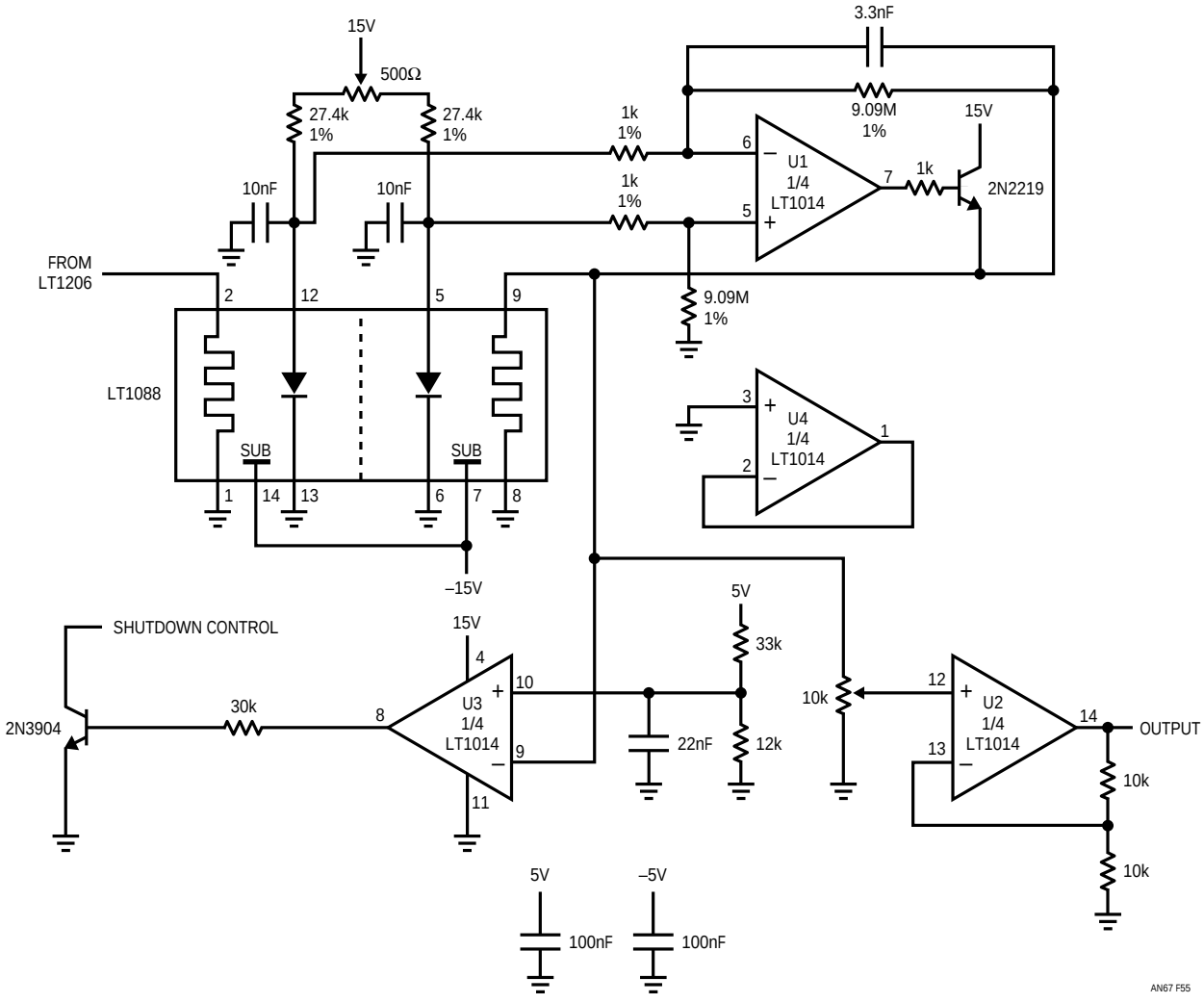


Figure 55. LT1088 RMS Detector Section

Coaxial Measurements

When measuring low level signals it is difficult to get a clean, accurate result. Scope probes have two problems. 10× probes attenuate the already small signal, and both 1× and 10× probes suffer from circuitous grounds. Coaxial adapters are a partial solution but these are expensive. They make for a lot of wear and tear on the probes and, without a little forethought, they can be a bear to attach to the circuit under test. My favorite way to get clean measurements of small signals is to directly attach a short length of coaxial cable as shown in Figure 56.

I use the good part of a damaged BNC cable, cutting away the shorter portion to leave at least 18" of RG-58/U and one good connector. At the cut, or as I call it, "real world" end of the cable, I unbraid, twist and tin a very small amount of outer conductor to form a stub 1/4" to 3/8" long. Next, I cut away the dielectric, exposing a similar length of center conductor, which I also tin. Now the probe is ready for use. It can be soldered directly to a circuit or breadboard, eliminating any lead length that might otherwise pick up stray noise, or worse, act as an antenna in a sensitive high gain circuit.

Small signals aren't the only beneficiaries of this technique. This works great for looking at ripple on the outputs of switching supplies. Ripple measurements are simplified because the large voltage swings associated with the switch node are completely isolated and no loop is formed where di/dt could inject magnetically coupled noise.

In some instances, I've found it important to retain the 50Ω termination impedance on the cable, but it is rarely possible to place a terminator at the "BNC" end of the cable, since this creates a DC path directly across the circuit under test. There is, however, another way as shown in Figure 57. Here, a technique known as back termination is used. No termination is used at the far end of the cable, but a 51Ω resistor is connected in series with the measurement end. Signals sent down the cable reach the BNC connector without attenuation, and fast edges that bounce off the unterminated end are absorbed back into the 51Ω source resistor. I've found this especially useful for measuring fast switch signals, or when measuring the RMS value of small signals, for ensuring that the amplifier input sees a properly terminated source. The resistor trick does not work if the node under test is high impedance; a FET probe is a better choice for high impedance measurements.

While I'm at it, I might as well give away my only other secret. We've all encountered ground loop problems, giving rise to 60Hz (50Hz for my friends overseas) injection into sensitive circuits. Every lab is replete with isolation transformers and "controlled substance" line cords with missing ground prongs for battling ground loops. There are similar problems at high frequencies, but the victim is wave fidelity, not AC pick up. To determine whether or not high frequency grounding, ground loops or common mode rejection is a problem for your oscilloscope, simply clamp a small ferrite E core around the probe lead while observing any effects on the waveform (see Figure 58). Sometimes the news is bad; the waveform really is messed up and there is some work to be done on the circuit. But occasionally the circuit is exonerated, the unexplainable aberrations disappear, proving that high frequency gremlins are at work. If necessary, several passes of the probe cable can be made through the E-Core and it can be taped together for as long as needed.

Figure 56. BNC Cable Used as a "Probe"

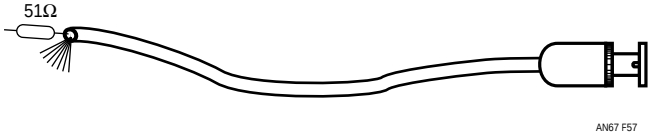


Figure 57. BNC Cable Probe Back Terminated

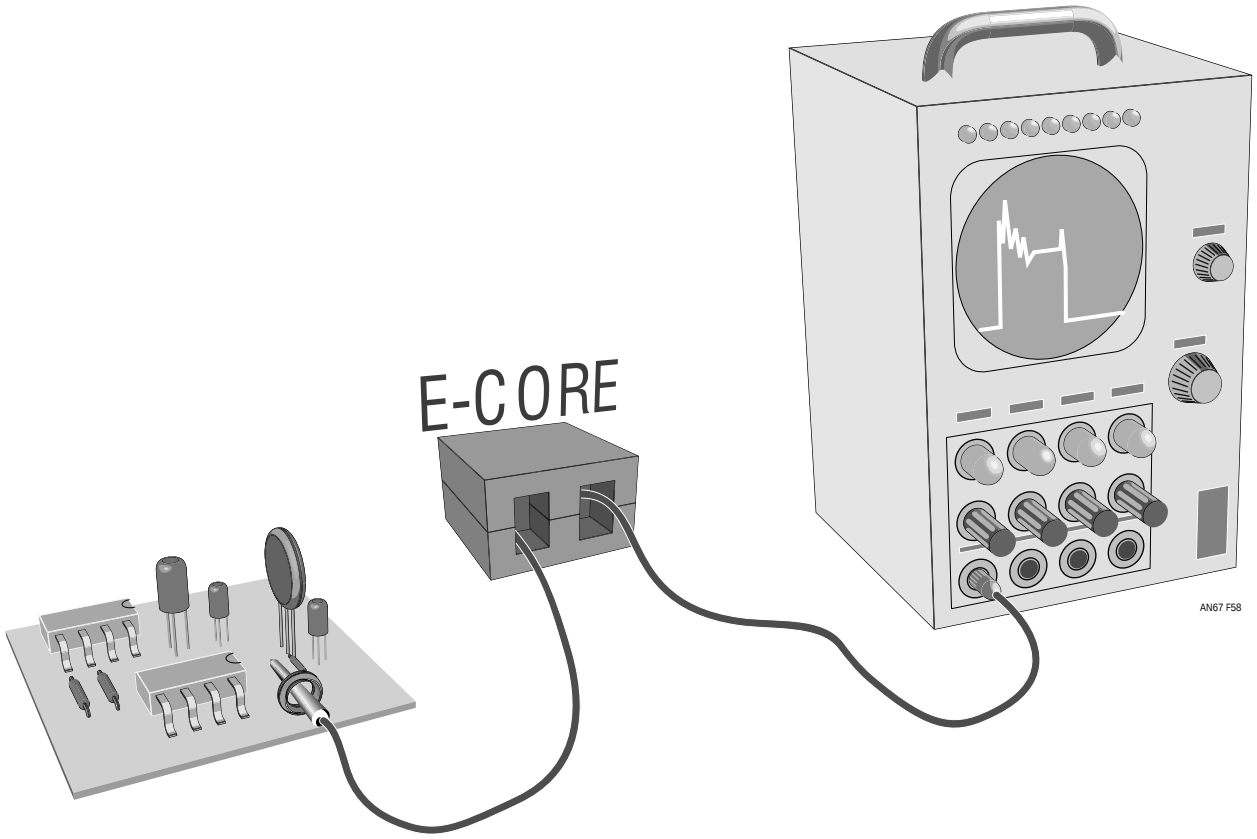


Figure 58. An E-Core Serves to Attenuate High Frequency Common Mode Currents from a Scope Probe

The performance of the amplifier and thermal converter can be optimized by adjusting the value of the feedback and gain setting resistors around the LT1206. Slightly more bandwidth can be achieved at the expense of higher peaking by reducing the resistor values 10%. Reducing the resistor values will decrease peaking effects at the expense of bandwidth. A good compromise value is 680Ω.

I've shown the LT1226 amplifiers operating from ±5 supplies, which puts their bandwidth on the edge at 40MHz. Their bandwidth can be improved by operating at ±15V.

Because the LT1206 operates on 15V rails, it is possible to overdrive the LT1088 and possibly cause permanent damage. One section of the LT1014 (U3) is used to sense an overdrive condition on the LT1088 and shut down the LT1206. Sensing the feedback heater instead of the input heater allows the LT1088 to accommodate high crest factor waveforms, shutting down only when the average input exceeds maximum ratings.

By the way, my power supply noise measured 200µV; filtering brought it down to less than 60µV.

LTC1392 MICROPOWER TEMPERATURE AND VOLTAGE MEASUREMENT SENSOR

by Ricky Chow and Dave Dwelley

The LTC1392 is a micropower data acquisition system designed to measure temperature, on-chip supply voltage and differential rail-to-rail common mode voltage. The device incorporates a temperature sensor, a 10-bit A/D converter, a high accuracy bandgap reference and a 3-wire half-duplex serial interface.

Figure 59 shows a typical LTC1392 application. A single point "star" ground is used along with a ground plane to minimize errors in the voltage measurements. The power supply is bypassed directly to the ground plane with a 1µF tantalum capacitor in parallel with an 0.1µF ceramic capacitor.

The conversion time is set by the frequency of the signal applied to the CLK pin. The conversion starts when the $\overline{CS}$ pin goes low. The falling edge of $\overline{CS}$ signals the LTC1392 to wake up from micropower shutdown mode. After the LTC1392 recognizes the wake-up signal, it requires an additional 80µs delay for a temperature measurement, or a 10µs delay for a voltage measurement, followed by a 4-bit configuration word shifted into D_{IN} pin. This word configures the LTC1392 for the selected measurement and initiates the A/D conversion cycle. The D_{IN} pin is then disabled and the D_{OUT} pin switches from three-state mode to an active output. A null bit is then shifted out of the D_{OUT} pin on the falling edge of the CLK, followed by the result of the selected conversion. The output data can be formatted as an MSB-first sequence or as an MSB-first followed by an LSB-first sequence, providing easy interface to either LSB-first or MSB-first serial ports. The minimum conversion time for the LTC1392 is 142µs in temperature mode or 72µs in the voltage conversion modes, both at the maximum clock frequency of 250kHz.

Conclusion

The LTC1392 provides a versatile data acquisition and environmental monitoring system with an easy-to-use interface. Its low supply current, coupled with space saving SO-8 or PDIP packaging, makes the LTC1392 ideal for systems that require temperature, voltage and current measurement while minimizing space, power consumption and external component count. The combination of temperature and voltage measurement capability on one chip makes the LTC1392 unique in the market, providing the smallest, lowest power multifunction data acquisition system available.

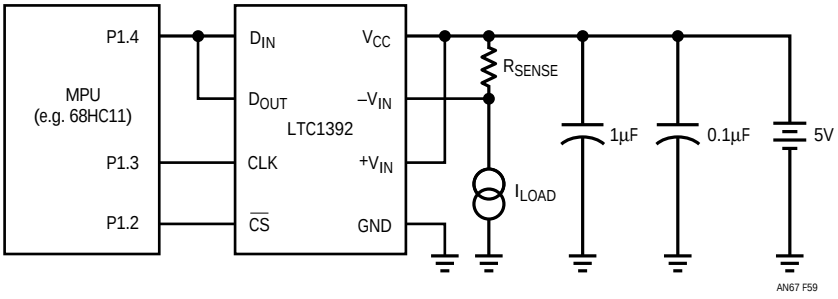


Figure 59. Typical LTC1392 Application

HUMIDITY SENSOR TO DATA ACQUISITION SYSTEM INTERFACE

by Richard Markell

Introduction

It can be difficult to interface humidity sensors to data acquisition systems because of the sensors' drive requirements and their wide dynamic range. By carefully selecting the devices that comprise the analog front end, users can customize the circuit to meet their humidity sensing requirements and achieve reasonable accuracy throughout the chosen range. This article details the analog front end interface between a Phys-Chem Scientific Corp.[1] model EMD-2000 humidity sensor and a user selected (probably microprocessor-based) data acquisition system.

Design Considerations

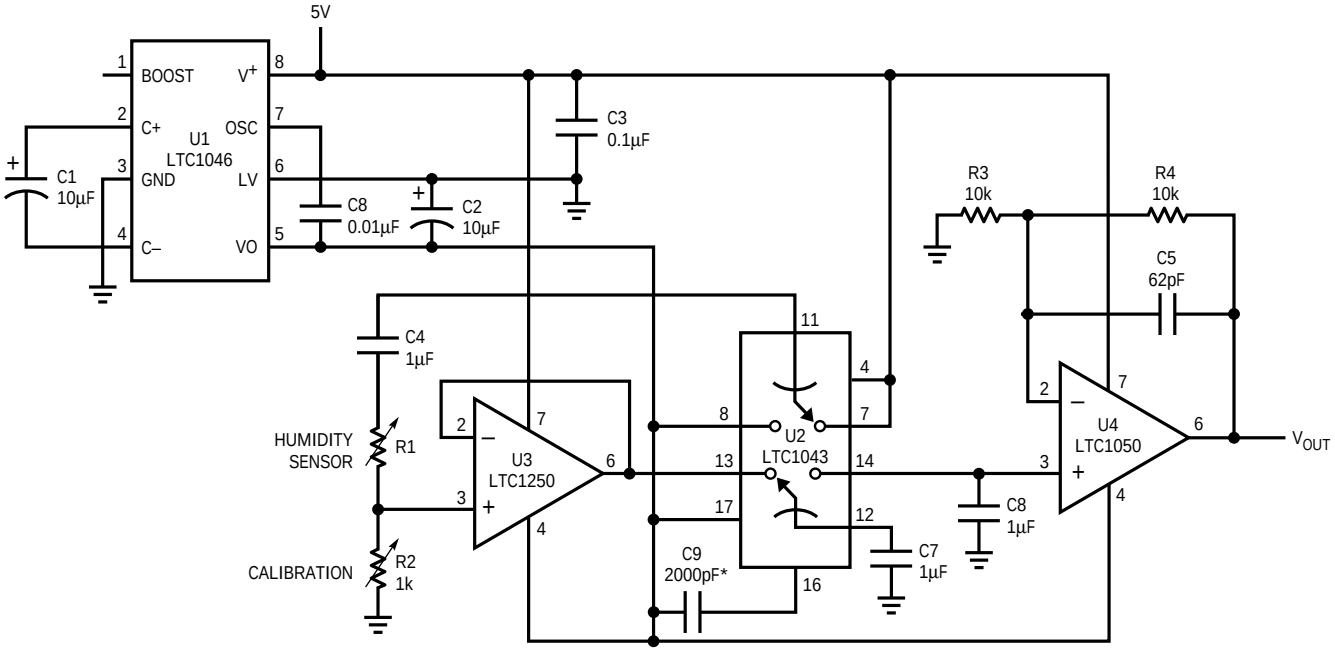
The Phys-Chem humidity sensor is a small, low cost, accurate resistance-type relative humidity (RH) sensor. This sensor has a well-defined stable response curve and can be replaced in circuit without system recalibration.

The design criteria call for a low cost, high precision analog front end that requires few calibration "tweaks" and operates on a single 5V supply. The sensor requires a square wave or sine wave excitation with no DC component. The sensor reactance varies over an extremely wide range (approximately 700Ω to 20MΩ). The wide dynamic range (approximately 90dB) required to obtain the full RH range of the sensor results in some challenges for the designer.

The circuit shown in the schematic features zero drift operational amplifiers (LTC1250 and LTC1050) and a precision instrumentation switched capacitor block (LTC1043). This design will maintain excellent DC accuracy down to microvolt levels. This method was chosen over the use of a true RMS-to-DC or log converter because of the expense and temperature sensitivity of these parts.

Circuit Description

Figure 60 is a schematic diagram of the circuit. Only a single 5V power supply is required. Integrated circuit U1, an LTC1046, converts the 5V supply to –5V to supply power to U2, U3 and U4. U2A, part of an LTC1043 switched capacitor building block, provides the excitation for the sensor, switching between 5V and –5V at a rate of approximately 2.2kHz. This rate can be varied, but we recommended that it be kept below approximately 2.4kHz, which is one-half the auto zero rate of U3. We believe the



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN OHMS, 1/4 W 5%
*C9 ADJUSTS OSC. FREQUENCY 2000pF YIELDS ~ 2.2kHz

AN67 F60

Figure 60. Schematic Diagram of Humidity Sensor Circuit

deviation from the Phys-Chem response curves taken at 5kHz is insignificant.

Variable resistor R2 sets the full-scale output. Since the sensor resistance is 700Ω at approximately 90% humidity, setting R2 at 700Ω will provide a 2:1 voltage divider that, when combined with the gain of U4 (×2), results in an overall gain of one. U3 must be included in order for the circuit to function properly; otherwise C4 and C7 form a voltage divider that is dependent on the resistance of the RH sensor. U3 is a precision auto zero operational amplifier with an auto zero frequency of approximately 4.75kHz. U2B (the "lower" switch) samples the output of U3 and provides this sample to the input of U4. U4 is set to provide a gain of 2.

It is easy to digitize the output of U4. Figure 61 is the schematic of a 12-bit converter that can be used for this purpose. The range of humidity that can be sensed depends on the resolution of the converter. The full-scale output (which is equivalent to approximately 90% humidity) is essentially independent of the number of bits in the A/D converter, but the dry (low RH) end of the scale is dependent on the A/D resolution. As an example, the above referenced 12-bit converter will process humidity signals that translate to approximately 20% RH, since the voltage output at this humidity is approximately 2.3mV, while 0.5LSB is 1.2mV. Digitization down to 10% RH requires the conversion of 350µV signals or a 16-bit converter. From a cost standpoint this seems unwieldy. It is much more economical to use a 2-channel 12-bit converter that changes ranges somewhere in the humidity range.

All of the above solutions measure output voltage from a voltage divider consisting of the RH sensor and a fixed "calibration" resistor. The resistance of the sensor at a fixed output voltage can be calculated from the formula

$$R\ (\Omega) = \frac{R2\ V_{FULL\ SCALE}}{V_{OUT}/2} - R2$$

In this case, if R2 is set to 700Ω and $V_{FULL\ SCALE}$ = 5.00V, then

$$R\ (\Omega) = \frac{3500}{V_{OUT}/2} - 700$$

Once R is calculated (probably by the microprocessor), the humidity can be calculated from the quadratic approximation in the Phys-Chem literature:

$$RH = \frac{LnR - 13.95 - \sqrt{(13.95 - LnR)^2 + 24.288}}{-0.184}$$

If a suitable humidity chamber is not available, the sensor can be removed and fixed resistors substituted. The circuit should then be calibrated from the EMD-2000 "typical response curve." This should provide approximately 2% accuracy.

[1]Phys-Chem Scientific Corporation, 26 West 20th Street, New York, NY 10011. (212) 924-2070 Phone, (212) 243-7352 FAX

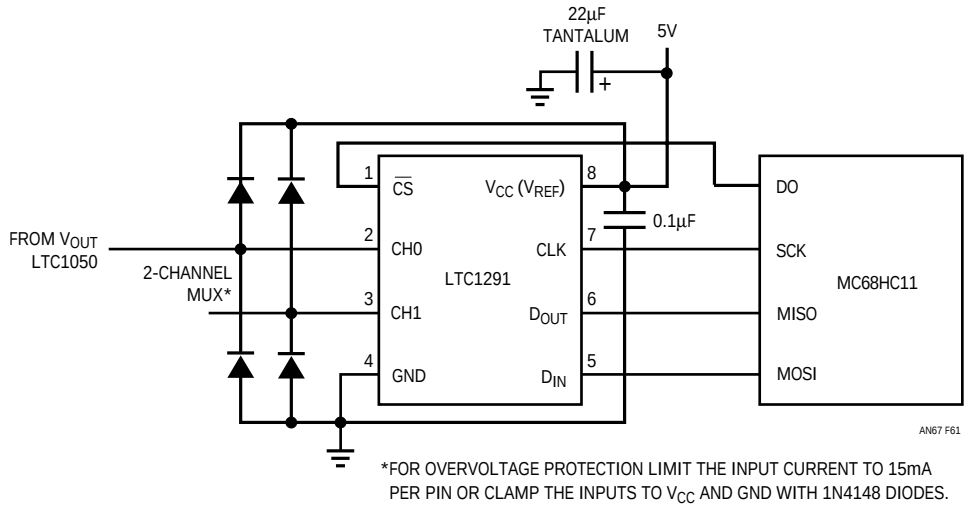


Figure 61. LTC1291 12-Bit A/D Converter Interfaced to MC68HC11

A SINGLE CELL BAROMETER

by Jim Williams and Steve Pietkiewicz

Figure 62, a complete barometric pressure signal conditioner, operates from a single 1.5V battery. Until recently, high accuracy and stability have been obtainable only with bonded strain gauge and capacitively-based transducers, which are quite expensive. This design, using a recently introduced semiconductor transducer, achieves 0.01"Hg (inches of mercury) uncertainty over time and temperature. The 1.5V powered operation permits portable application.

The 6kΩ transducer (T1) requires precisely 1.5mA of excitation, necessitating a relatively high voltage drive. A1's positive input senses T1's current by monitoring the voltage drop across the resistor string in T1's return path. A1's negative input is fixed by the 1.2V LT1004 reference. A1's output biases the 1.5V powered LT1110 switching regulator. The LT1110's switching produces two outputs from L1. Pin 4's rectified and filtered output powers A1 and T1. A1's output, in turn, closes a feedback loop at the regulator. This loop generates whatever voltage step-up is required to force precisely 1.5mA through T1. This arrangement provides the required high voltage drive while minimizing power consumption. This occurs because the switching regulator produces only enough voltage to satisfy T1's current requirements.

L1 Pins 1 and 2 source a boosted, fully floating voltage, which is rectified and filtered. This potential powers A2. Because A2 floats with respect to T1, it can look differentially across T1's outputs, Pins 10 and 4. In practice, Pin 10 becomes "ground" and A2 measures Pin 4's output with respect to this point. A2's gain scaled output is the circuit's output, conveniently scaled at 3.000V = 30.00"Hg.

To calibrate the circuit, adjust R1 for 150mV across the 100Ω resistor in T1's return path. This sets T1's current to the manufacturer's specified calibration point. Next, adjust R2 at a scale factor of 3.000V = 30.00"Hg. If R2 cannot capture the calibration, reselect the 200k resistor in series with it. If a pressure standard is not available, the transducer is supplied with individual calibration data permitting circuit calibration.

This circuit, compared to a high order pressure standard, maintained 0.01"Hg accuracy over months with widely varying ambient pressure shifts. Changes in pressure, particularly rapid ones, correlated quite nicely to changing weather conditions. Additionally, because 0.01"Hg corresponds to about 10 feet of altitude at sea level, driving over hills and freeway overpasses becomes quite interesting. The circuit pulls 14mA from the battery, allowing about 250 hours operation from one D cell.

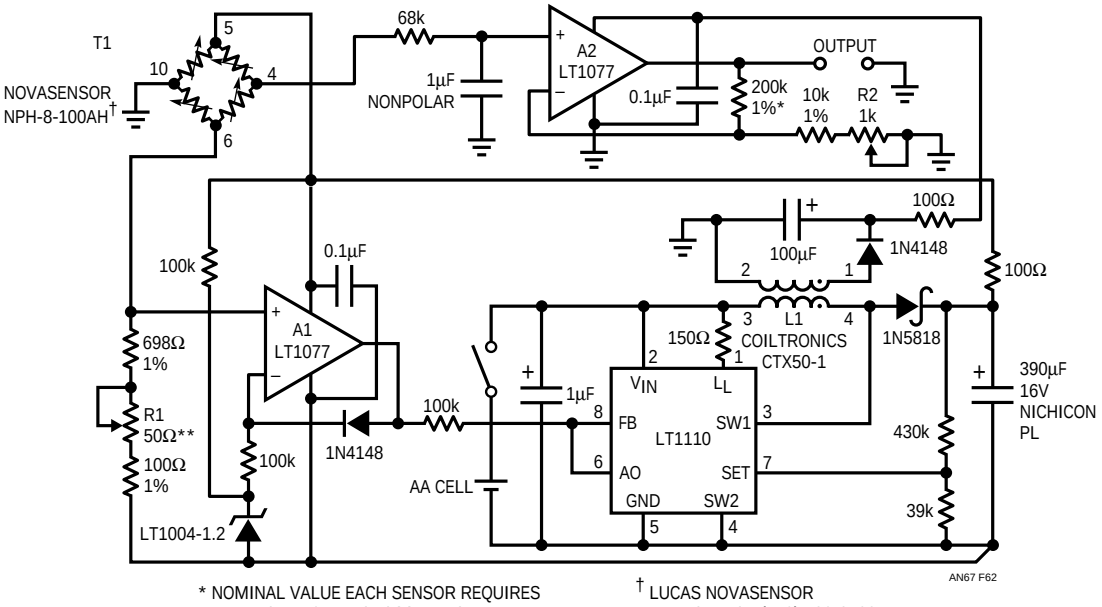


Figure 62. Single Cell Barometer Schematic Diagram

NOISE GENERATORS FOR MULTIPLE USES

A Broadband Random Noise Generator

by Jim Williams

Filter, audio and RF communications testing often require a random noise source. Figure 63's circuit provides an RMS amplitude regulated noise source with selectable bandwidth. RMS output is 300mV with a 1kHz to 5MHz bandwidth, selectable in decade ranges.

Noise source D1 is AC coupled to A2, which provides a broadband gain of 100. A2's output feeds a gain control stage via a simple, selectable lowpass filter. The filter's output is applied to A3, an LT1228 operational transconductance amplifier. A1's output feeds LT1228 A4, a current feedback amplifier. A4's output, which is also the circuit's output, is sampled by the A5-based gain control configuration. This closes a gain control loop to A3. A3's I_{SET} current controls gain, allowing overall output level control.

Figure 64 plots noise at a 1MHz bandpass, whereas Figure 65 shows RMS noise versus frequency in the same bandpass. Figure 66 plots similar information at full bandwidth (5MHz). RMS output is essentially flat to 1.5MHz, with about ±2dB control to 5MHz before sagging badly.

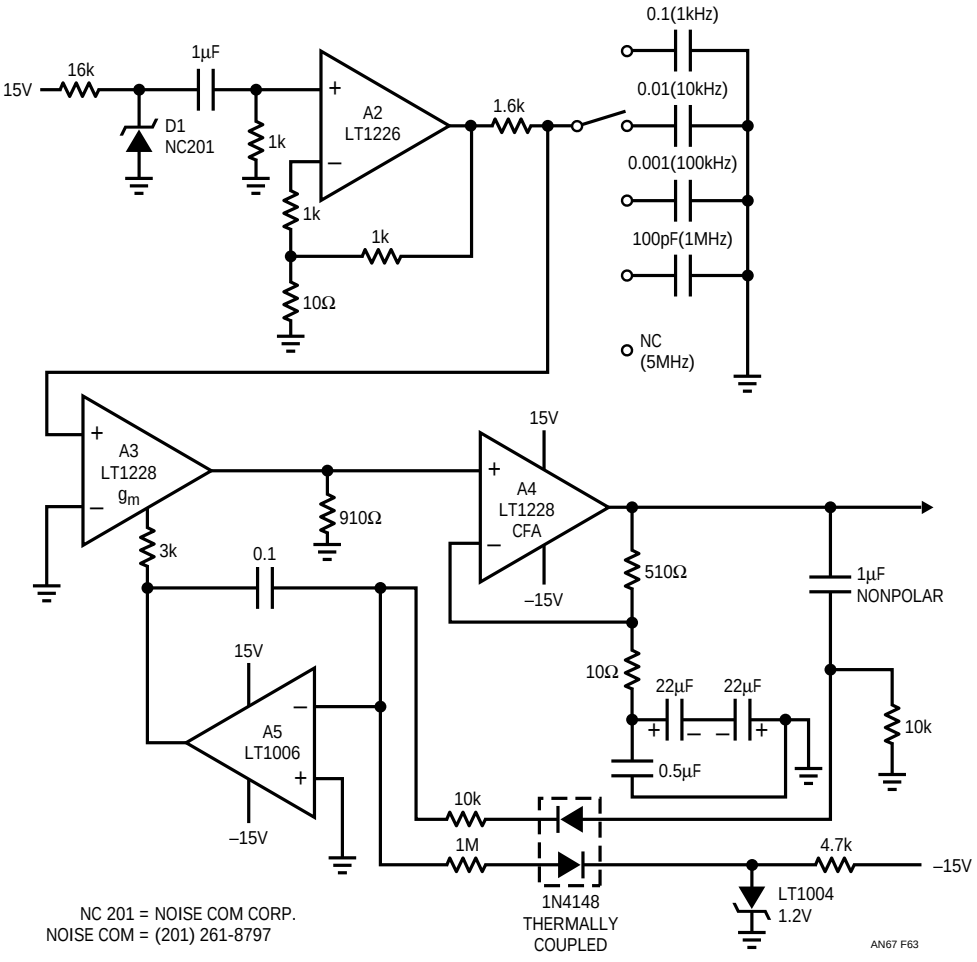


Figure 63. Broadband Random Noise Generator Schematic

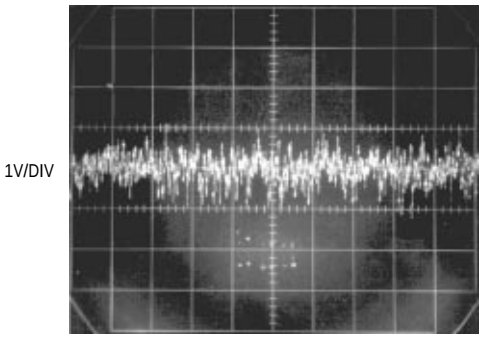


Figure 64. Figure 63's Output In the 1MHz Filter Position

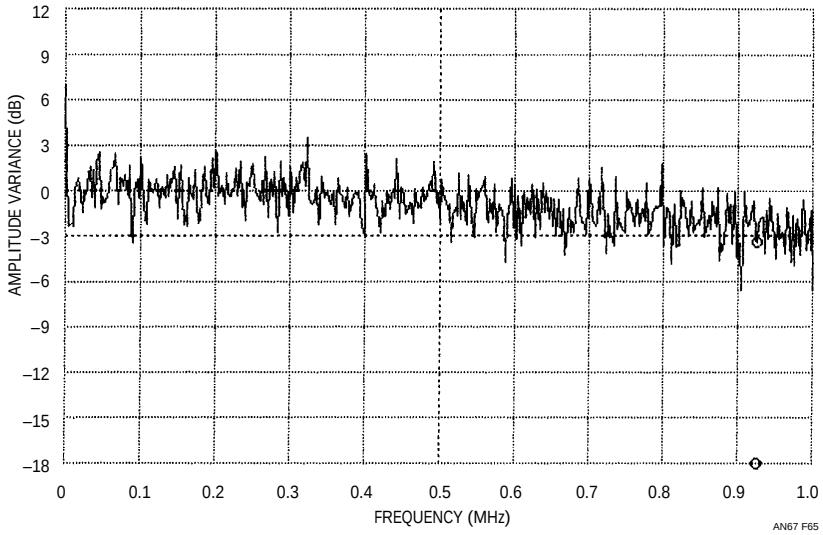


Figure 65. RMS Noise vs Frequency at 1MHz Bandpass

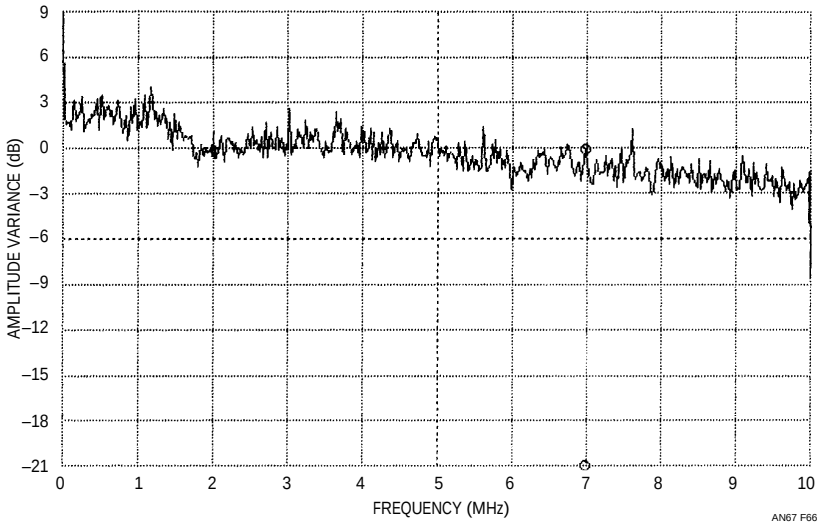


Figure 66. RMS Noise vs Frequency at 5MHz Bandpass

SYMMETRICAL WHITE GAUSSIAN NOISE

by Bent Hessen-Schmidt, NOISE COM, INC.

White noise provides instantaneous coverage of all frequencies within a band of interest with a very flat output spectrum. This makes it useful both as a broadband stimulus and as a power level reference.

Symmetrical white Gaussian noise is naturally generated in resistors. The noise in resistors is due to vibrations of the conducting electrons and holes as described by Johnson and Nyquist.[1, 2] The distribution of the noise voltage is symmetrically Gaussian, and the average noise voltage is:

$$\overline{V}_n = 2\sqrt{kTf\ R(f)\ p(f)\ df} \qquad (1)$$

where:

k = 1.38E-23 J/K (Boltzmann's constant)

T = temperature of the resistor in Kelvin

f = frequency in Hz

h = 6.62E-34 Js (Planck's constant)

R(f) = resistance in ohms as a function of frequency

$$p(f) = \frac{hf}{kT[\exp(hf/kT) - 1]} \qquad (2)$$

p(f) is close to unity for frequencies below 40GHz when T is equal to 290°K. The resistance is often assumed to be independent of frequency, and $f$df is equal to the noise bandwidth (B). The available noise power is obtained when the load is a conjugate match to the resistor, and it is:

$$N = \frac{\overline{V}_n^2}{4R} = kTB \qquad (3)$$

where the "4" results from the fact that only half of the noise voltage and hence only 1/4 of the noise power is delivered to a matched load.

Equation 3 shows that the available noise power is proportional to the temperature of the resistor; thus it is often called thermal noise power. Equation 3 also shows that white noise power is proportional to the bandwidth.

An important source of symmetrical white Gaussian noise is the noise diode. A good noise diode generates a high level of symmetrical white Gaussian noise. The level is often specified in terms of excess noise ratio (ENR).

$$\text{ENR (in dB)} = 10\text{Log}\ \frac{(Te - 290)}{290} \qquad (4)$$

Te is the physical temperature that a load (with the same impedance as the noise diode) must be at to generate the same amount of noise.

The ENR expresses how many times the effective noise power delivered to a nonemitting, nonreflecting load exceeds the noise power available from a load held at the reference temperature of 290°K (16.8°C or 62.3°F).

The importance of a high ENR becomes obvious when the noise is amplified, because the noise contributions of the amplifier may be disregarded when the ENR is 17dB larger than the noise figure of the amplifier (the difference in total noise power is then less than 0.1dB). The ENR can easily be converted to noise spectral density in dBm/Hz or $\mu V/\sqrt{Hz}$ by use of the white noise conversion formulas in Table 1.

Table 1. Useful White Noise Conversion

dBm = dBm/Hz + 10log(BW)
dBm = 20log($\overline{V}$n) – 10log(R) + 30dB
dBm = 20log($\overline{V}$n) + 13dB, for R = 50Ω
dBm/Hz = 20log(μVn$\sqrt{Hz}$ – 10log(R) – 90dB
dBm/Hz = –174dBm/Hz + ENR, for ENR > 17dB

When amplifying noise it is important to remember that the noise voltage has a Gaussian distribution. The peak voltages of noise are therefore much larger than the average or RMS voltage. The ratio of peak voltage to RMS voltage is called crest factor, and a good crest factor for Gaussian noise is between 5:1 and 10:1 (14dB to 20dB). An amplifier's 1dB gain compression point should therefore be typically 20dB larger than the desired average noise output power to avoid clipping of the noise.

For more information about noise diodes, please contact NOISE COM, INC. at (201) 261-8797.

[1] Johnson, J.B. "Thermal Agitation of Electricity in Conductors," *Physical Review*, July 1928, pp. 97-109.

[2] Nyquist, H. "Thermal Agitation of Electric Charge in Conductors," *Physical Review*, July 1928, pp. 110-113.

NOISE GENERATORS FOR MULITPLE USES

A Diode Noise Generator for "Eye Diagram" Testing

by Richard Markell

The circuit that Jim Williams describes evolved from my desire to build a circuit for testing communications channels by means of "eye diagrams." (See *Linear Technology*, Volume I, Number 2 for a short explanation of the eye diagram.) I wanted to replace my pseudorandom code generator circuit, which used a PROM, with a more "analog" design—one that more people could build without specialized components. What evolved was a noise source sampled by a very fast comparator (see Figure 67). The comparator outputs a random pattern of 1's and 0's.

The noise diode (an NC201) is filtered and amplified by the LT1190 high speed operational amplifier (U1). The output feeds the LT1116 (U2), a 12ns single supply, ground-sensing comparator. The 2kΩ pot at the inverting input of the LT1116 sets the threshold to the comparator so that a quasiequal number of 1's and 0's are output. U3 latches the output from U2 so that the output from the comparator remains latched throughout one clock period. The two-level output is taken from U3's Q0 output.

The additional circuitry shown in the schematic diagram allows the circuit to output four-level data for PAM (pulse amplitude modulation) testing. The random data from the two-level output is input to a shift register, which is reset on every fourth clock pulse. The output from the shift register is weighted by the three 5k resistors and summed into the LT1220 operational amplifier from which the output is taken. The filter network between the 74HC74 output and the 74HC4094 strobe input is necessary to ensure that the output data is correct.

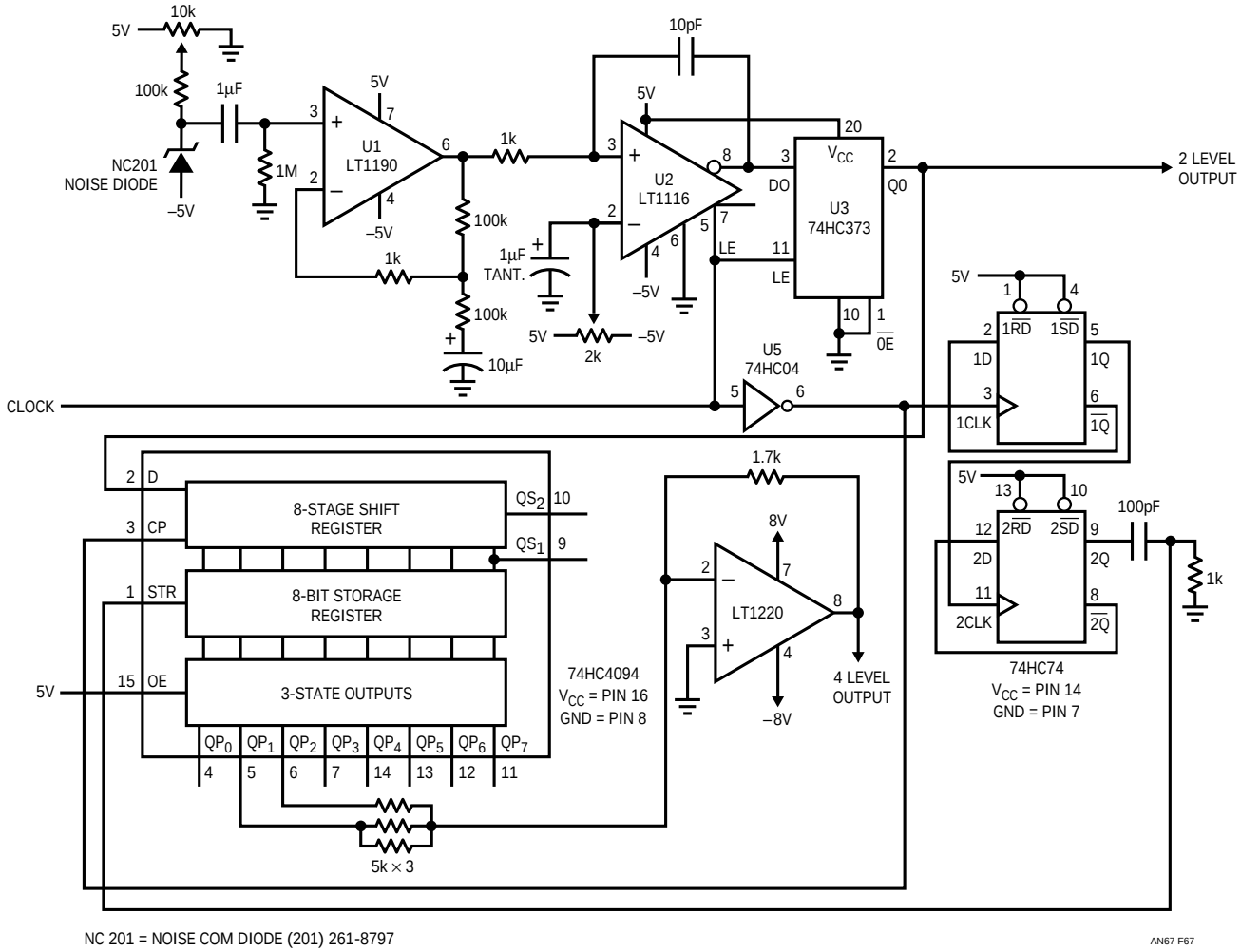


Figure 67. Pseudorandom Code Generator Schematic Diagram

Video/Op Amps

LT1251 CIRCUIT SMOOTHLY FADES VIDEO TO BLACK

by Frank Cox

When a video signal is attenuated, there is a point were the sync amplitude is too small for a monitor to process properly. Instead of making a smooth transition to black, the picture rolls and tears. One solution to this problem is to run a separate sync signal into the monitor. This may not be a viable solution in a system where cost and complexity are the prime concerns. What is needed is a simple video "volume control."

The circuit in Figure 68 can perform a smooth fade to black, while maintaining good video fidelity. U1, an LT1360 op amp, and its associated components form an elementary sync separator. C1, R1 and D1 clamp the composite video. D2 biases the input of U1 to compensate for the drop across D1. When D1 conducts, the most negative portion of the waveform containing the sync information is amplified by U1. The clamp circuit in the feedback network of U1 (D4 to D8) prevents the amplifier from saturating. D3 and the CMOS inverter U4 complete the shaping of the sync waveform. This sync separator works with most video signals but, because of its simplicity, will not work with very noisy or distorted video. The remainder of the circuit is an LT1251 video fader (U2) configured to fade between the original video and the sync stripped from that video. Thus, the video fades to black.

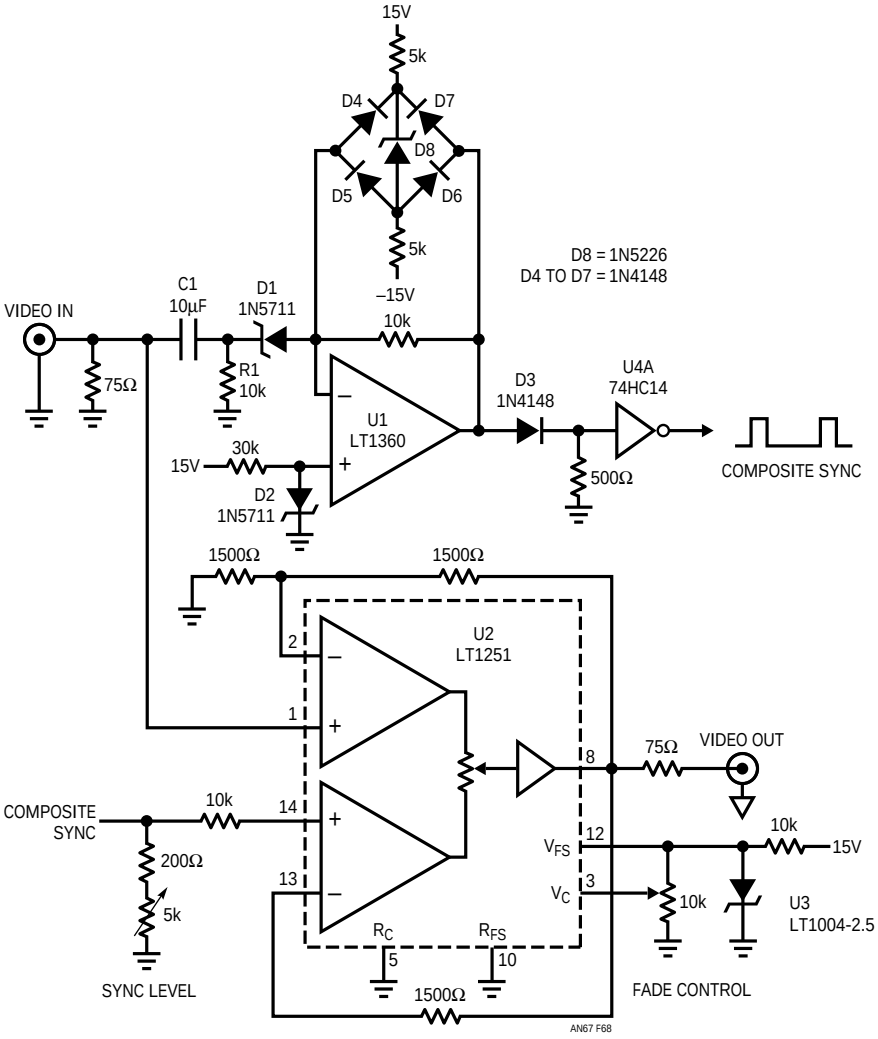


Figure 68. LT1251 Video Fader Schematic Diagram

The control voltage for the fader is generated by a voltage reference and a 10k variable resistor. If this control potentiometer is mounted an appreciable distance from the circuit or if the control generates any noise when adjusted, this node should be bypassed.

Figure 69 is a multiple exposure waveform photograph that shows the action of this circuit. Two linear ramp video test signals are shown in this photograph. The video is faded from full amplitude to zero amplitude in six steps. The sync waveform (lower center) remains unchanged. In Figure 70, a single video line modulated with color subcarrier is faded from full video amplitude to zero video amplitude. The monitor will eventually lose color lock and shut the color off as the amplitude of the color subcarrier is reduced. This is not a problem in this application because the color decoding circuits in the monitor are designed to work with a variety of signals from tape or broadcast, and so have a large dynamic range. Color portions of the picture will remain after the luminance portion is completely black.

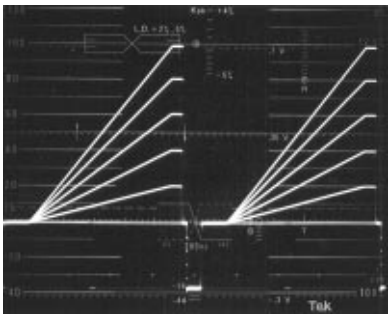


Figure 69. Multiple Exposure Photo Showing Circuit Operation

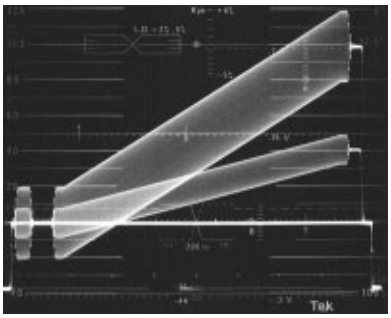


Figure 70. Photo Detailing a Single Video Line with Color Subcarrier Faded to Zero Amplitude

LUMA KEYING WITH THE LT1203 VIDEO MULTIPLEXER

by Frank Cox

In video systems, the action of switching between two or more active video sources is referred to as a "wipe" or a "key." When the decision to switch video sources is based on an attribute of the active video itself, the action is called keying. A wipe is controlled by a nonvideo signal such as a ramp. The circuit presented in Figure 71 is referred to as a "luma key" because it switches between two sources when the luminance ("luma") of a monochrome key signal reaches a set level. It is also possible to key on the color of the video source and this, not surprisingly, is called "chroma keying."

Figure 71's operation is very straightforward. A monochrome video source is used to generate the key signal. The LT1363 is used as a buffer and may not be needed in all applications. If the key signal is to be used as one of the switched signals, it is convenient to "loop through" the input of this buffer. The LT1016 comparator switches when the video level exceeds the DC reference on its inverting input, which is controlled by the "key sensitivity" control. The TTL key signal controls an LT1203 video multiplexer. Any two video sources may be connected to the inputs of the LT1203, as long as they are gen locked and within the common mode range (on ±5V supplies this is ±3V over 0°C to 70°C) of the multiplexer. The LT1203's fast switching speed, low offset and clean switching make it a natural for an active video switching application like this one. Composite color signals can be used, but the best results will be obtained if the key signal's horizontal sync is phase coherent with the color reference of the sources. The key source video should be monochrome to prevent the key comparator from switching on the color subcarrier.

Nonstandard video signals can be used for the inputs to the LT1203. For instance, it is possible to select between two DC input levels to construct a two-level image. Figure 72 is an example of an image constructed this way. A monochrome video signal is sliced and used to key between black (0V) and gray (approximately 0.5V) to

generate this image of a famous linear IC designer. An image formed in this way is not a standard video output until the blanking and sync intervals are reconstructed. The second LT1203 blanks the video and an LT1363 circuit sums composite sync to the video and drives a cable. For more information on this part of the circuit, see AN 57, page 7. A clamp is not used since the DC levels are arbitrarily set by the inputs, but one could be used, as in the figure on page 7 of AN57, if the sources were video. As another option, Figure 73 shows the same key signal used as one of the inputs to the multiplexer.

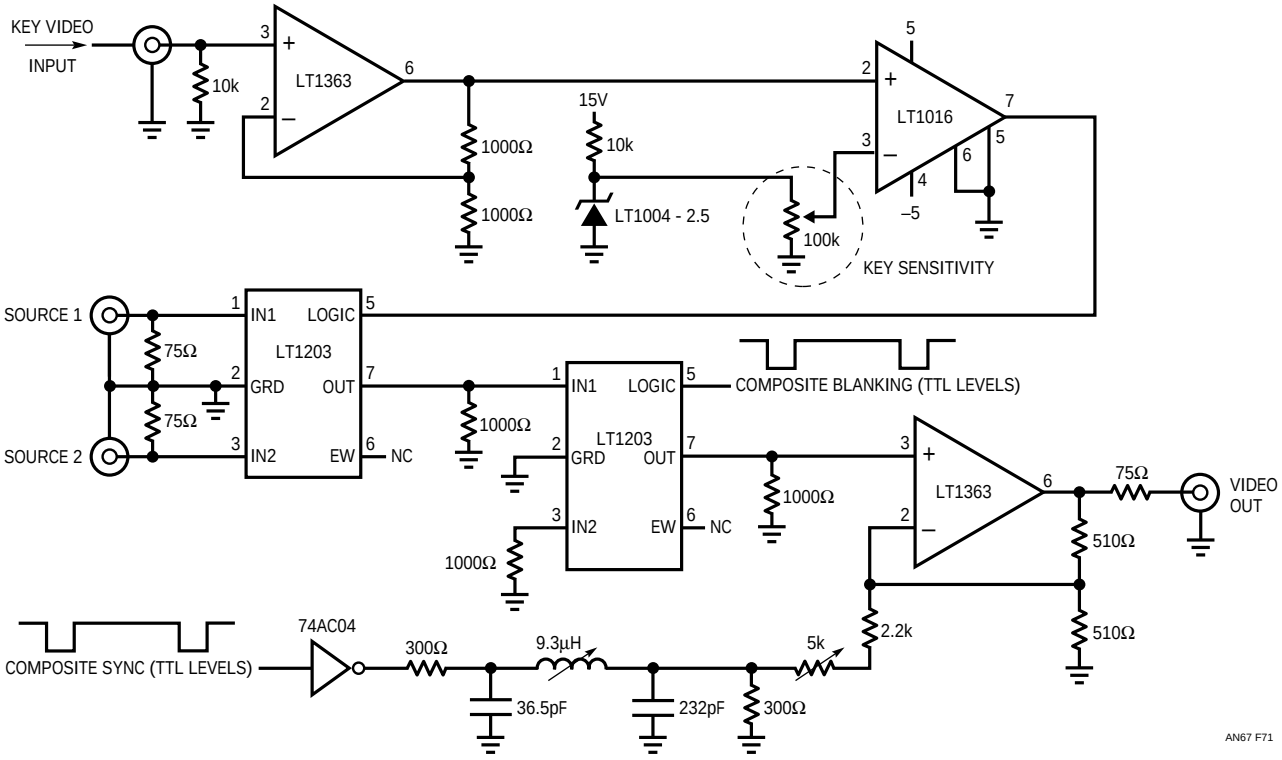


Figure 71. Luma Keyer Schematic Diagram

Figure 72. Two Level Image of IC Designer

Figure 73. Key Signal Used as Input to the MUX

LT1251/LT1256 VIDEO FADER AND DC GAIN CONTROLLED AMPLIFIER

by William H. Gross

The Video Fader

Figure 74 shows the LT1251/LT1256 configured as a fader with unity gain. A full-scale voltage of 2.5V is applied to Pin 12 and the control input drives Pin 3.

Figure 75 shows the true response of the control path. The control path is fast enough for quick switching between signals, as when keying on a color or luminance level. The control path introduces only a small (50mV), short (50ns) glitch when switched quickly.

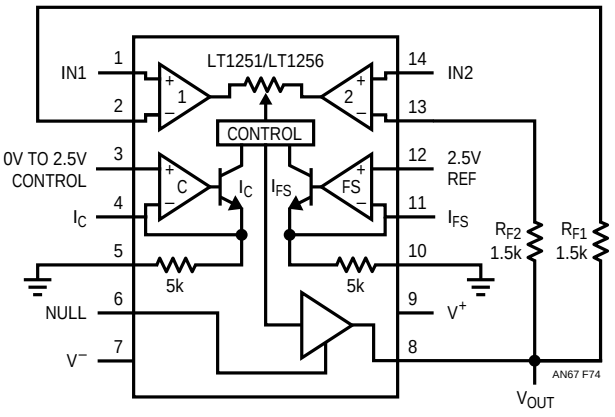


Figure 74. Two Input Video Fader

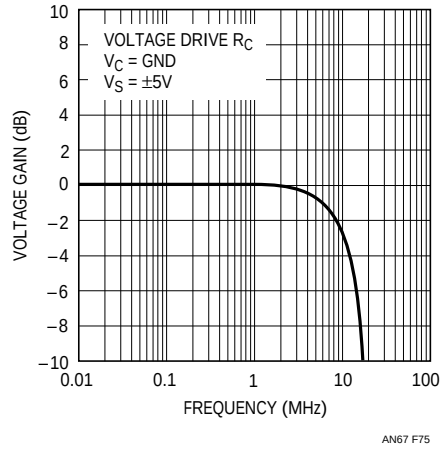


Figure 75. LT1251/56 Control Path Bandwidth

A summary of the LT1251/LT1256 performance operating on ±5V supplies in the configuration shown in Figure 74 is given in Table 1.

Table 1. LT1251/LT1256 Performance Summary

Slew Rate (at ±2V, R_L = 150Ω)	300V/µs
Full-Power Bandwidth ($1V_{RMS}$)	30MHz
Small-Signal Bandwidth	30MHz
Differential Gain (NTSC, R_L = 150Ω)	0.1%
Differential Phase (NTSC, R_L = 150Ω)	0.1°
Total Harmonic Distortion (1kHz, K = 1)	0.001%
(1kHz, K = 0.5)	0.01%
(1kHz, K = 0.1)	0.4%
Rise Time, Fall Time	11ns
Overshoot	3%
Propagation Delay	10ns
Settling Time (0.1%, V_O = 2V)	65ns
Quiescent Supply Current	13.5mA

Applications

Grounding IN2 of the LT1256 in Figure 74 results in a 2-quadrant multiplier. Figure 76 shows the 2-quadrant multiplier being used as an AM modulator. The output will deliver 10dBm into 50Ω. The LT1077 op amp senses the LT1256 output DC and drives the Null pin, eliminating any DC at the output. The Null pin voltage is nominally 100mV above the negative supply and therefore the op amp output must be able to swing within a few millivolts of the negative supply. Without the LT1077, the worst-case DC output voltage is 50mV.

By operating one input stage in an inverting configuration and the other in a noninverting configuration and driving both inputs, the LT1256 becomes a 4-quadrant multiplier. Figure 77 shows the 4-quadrant multiplier being used as a double-sideband, suppressed-carrier modulator. The LT1077 DC output nulling circuit could be added if necessary.

The LT1251/LT1256 can be used to implement numerous other functions, including voltage controlled filters, phase shifters and oscillators. Squaring and limiting circuits can be designed by feeding the output or input into the Control pins. Gamma correction and other compression circuits are created in a similar manner. The applications are limited only by the designer's imagination.

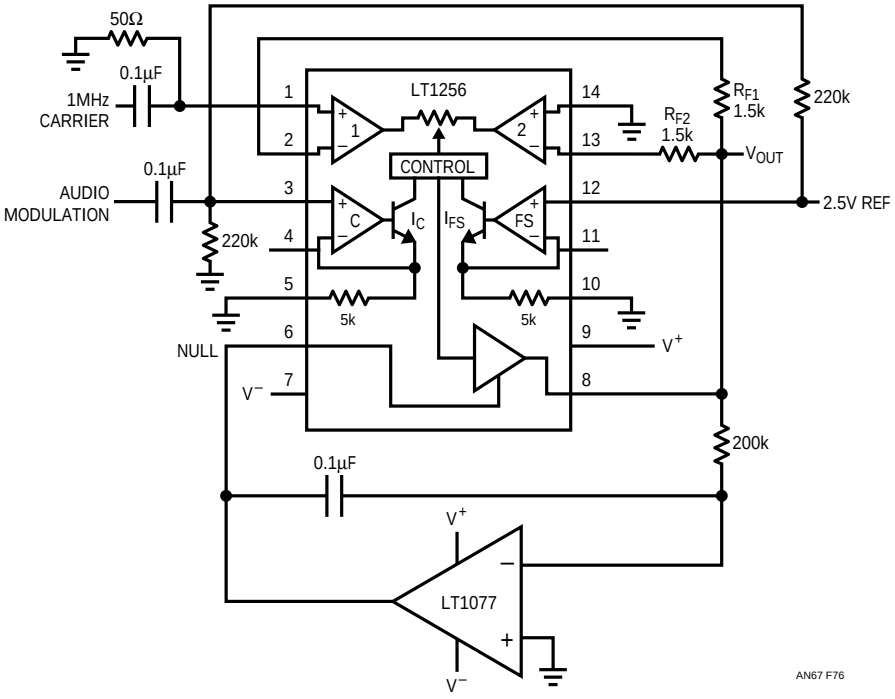


Figure 76. AM Modulator with DC Output Nulling Circuit

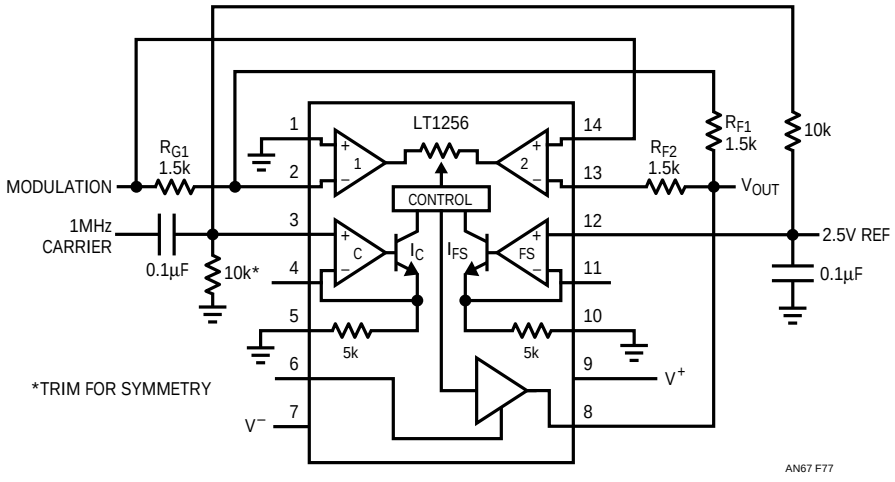


Figure 77. Four Quadrant Multiplier Uses as a Double Sideband, Suppressed Carrier Modulator

EXTENDING OP AMP SUPPLIES TO GET MORE OUTPUT VOLTAGE

by Dale Eagar

We often hear of applications that require high output voltage, low output impedance amplifiers. Here is a topology that allows you to extend an op amp's output voltage swing while still maintaining its short-circuit protection. The trick is to suspend the op amp between two MOSFET source followers so that the supply voltages track the op amp's output voltage (see Figure 78). The circuit shown in Figure 78 will perform very nicely with any run-of-the-mill ideal op amp. The problem is in the lead times of ideal op amps—they just keep getting pushed out to later dates.

Nonideal op amps have realistic lead times and can be made to work in the extended supply mode. They have bandwidth limitations in both CMRR and PSRR. The circuit shown in Figure 79 implements the extended supply as shown in Figure 78 and has several additional components: C1 is added to decouple the supply, improving high frequency PSRR; R3 and R5 decouple the gates of Q1 and Q2 from AC ground, preventing Q1 and Q2 from running off together to redirect local air traffic; R1, R2 and C4 form a snubber to de-Q the 2-pole system formed by the Miller capacitance of Q1 and Q2 and the high frequency CMRR of IC1; additionally, R4, R6, C2, C3, Z1 and Z2 form the two 15V voltage sources (E1 and E2 in Figure 78); CR1 and CR2 are protection diodes that allow the output to be instantaneously shorted to ground when the output is at any output voltage.

The values of R1, R2 and C4 vary with the MOSFETs' Miller capacitance and with the high frequency CMRR of the op amp used. They are selected to minimize the overshoot in the step response of the amplifier.

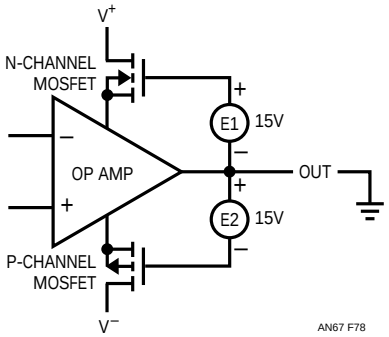


Figure 78. Block Diagram of Suspended Supply Op Amp

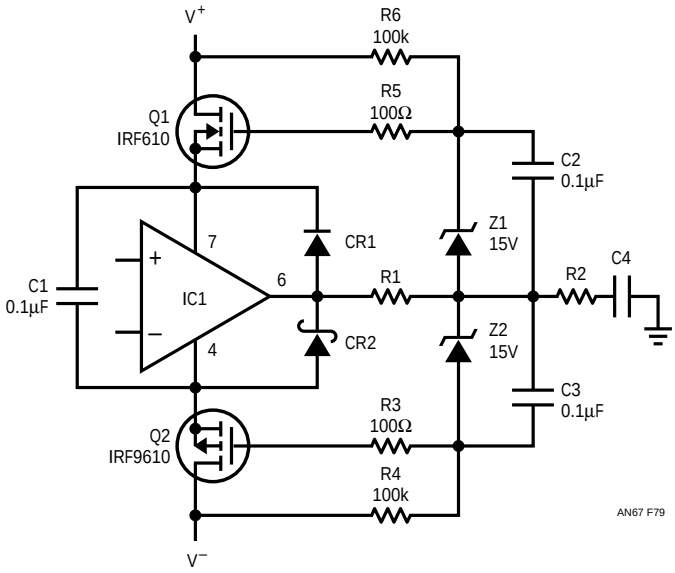


Figure 79. Detailed High Voltage Op Amp

High Voltage, High Frequency Amplifier

Using the LT1227 current feedback amplifier (CFA) in the extended supply mode as shown in Figure 79, it is relatively easy to get a 1MHz power bandwidth at $100V_{P-P}$ (see Figure 80 for component values). This circuit has short-circuit protection and is stable into all capacitive loads.

If One Is Good, Are Two Better?

Dual and quad op amps can also be configured with extended supplies, although the design gets just a wee bit tricky. When extending supplies of multiple stages and/or complete circuits, some design rules need to change. Op amp circuits generally require a ground against which to reference all signals. The problem encountered when

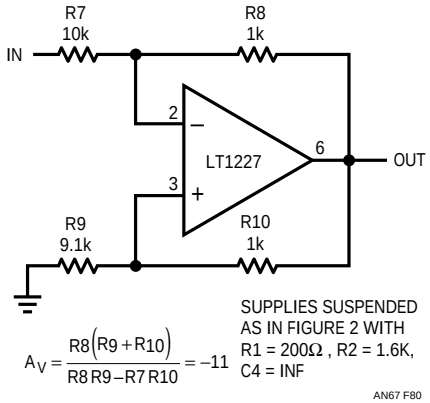


Figure 80. High Speed Suspended Op Amp

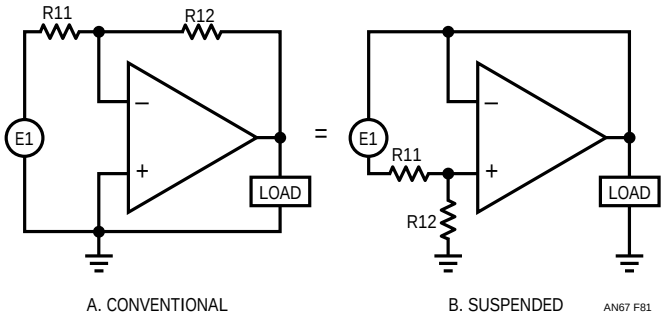


Figure 81. Inverting Amplifiers (A. Conventional, B. Suspended)

using extended supply mode is that "ground" is swinging through the common mode range of the op amp and beyond. This raises the following question: "If I cannot reference the signals to ground, to what can I reference them?" The answer? "Use the output as the signal reference." This works for all stages except the last stage, where using the output as the reference would simply discard the signal. In the last stage, ground is effectively the output and the feedback resistor is R12. This is shown in Figures 81a and 81b. Figure 81a shows a conventional inverting amplifier where the input and output signals are referred to ground. Figure 81b shows the equivalent circuit implemented in the extended supply mode.

Here are two rules for design in the extended supply mode, which will be demonstrated in the next application:

Rule 1: When designing multiple stages in the extended supply mode, reference the signals of all stages except the last to the output of the last stage.

Rule 2: Invert the signal using the circuit in Figure 81b at the last stage.

Ring-Tone Generator

Ring-tone generators are sine wave output, high voltage inverters for the specific purpose of ringing telephone bells. In decades past, the phone company generated their ring tones with motor generator sets with the capacity to ring numerous phones simultaneously. Often, ring tones are 20Hz at 90V with less than 10mA per bell output current capability. Since the power supplied is low one would think that the task is minimal. This is not always so. "It's simple—no problem," is often heard in response to queries about ring tone generators. "Just hook a couple of logic level FETs to two spare output bits of the microprocessor and hook their drains to the primary side of a transformer, with the center tap hooked to 5V or 12V or whatever." At this point everyone is happy until the transformer comes in. After a few phone calls to make sure that the transformer maker shipped the right one, the engineer (face covered with egg) asks if anyone needs a rather large paperweight. The engineer (still wiping egg from his face) then decides to use switching power supply technology to solve this "simple" problem.

Here is a simple ring-tone generator that can be turned on and off with a logic signal. It has a fully isolated output, is short-circuit protected and can be powered by any input voltage from 3V to 24V.

How It Works

Suspended along with the dual op amp in Figure 82 are two voltage references and an oscillator. Keep in mind when referring to Figure 82 that the node labeled "A" is the output; this is the reference common for the references, the oscillator and the first lowpass filter (U1a). The two references, VR1 and VR2, produce ±2.5V. The oscillator U2, running on the ±2.5V references, produces a 20Hz square wave rail-to-rail. U1a is a 2nd order, Sallen and Key lowpass filter that knocks off the sharp edges, presenting the somewhat smoothed signal at point "B."

Next comes the tricky stuff. U1b is a 2nd order, multiple-feedback (MFB) lowpass filter/amplifier that performs four functions: first, it subtracts the voltage at point "A" (its own output voltage) from the voltage at point "B" (the incoming signal), forming a difference that is the signal; second, it filters the difference signal with a 2-pole lowpass filter, smoothing out the last wrinkles in the signal; third, it amplifies the filtered difference signal with a gain of 34; and fourth, it references the amplified signal to ground, forming the output.

Note that R99 shown in Figure 82 is there to protect the input of U1b in the event that the output is shorted when the output voltage is very high. This measure is necessary because the bottom end of C99 is connected to ground, and C99 could have up to 100V across it. When the output is shorted to ground from a high voltage, R99 limits the current into the input of U1b to an acceptable level.

This circuit, when coupled with the switching power supply shown in Figure 83, implements a fully isolated sine wave ring tone generator.

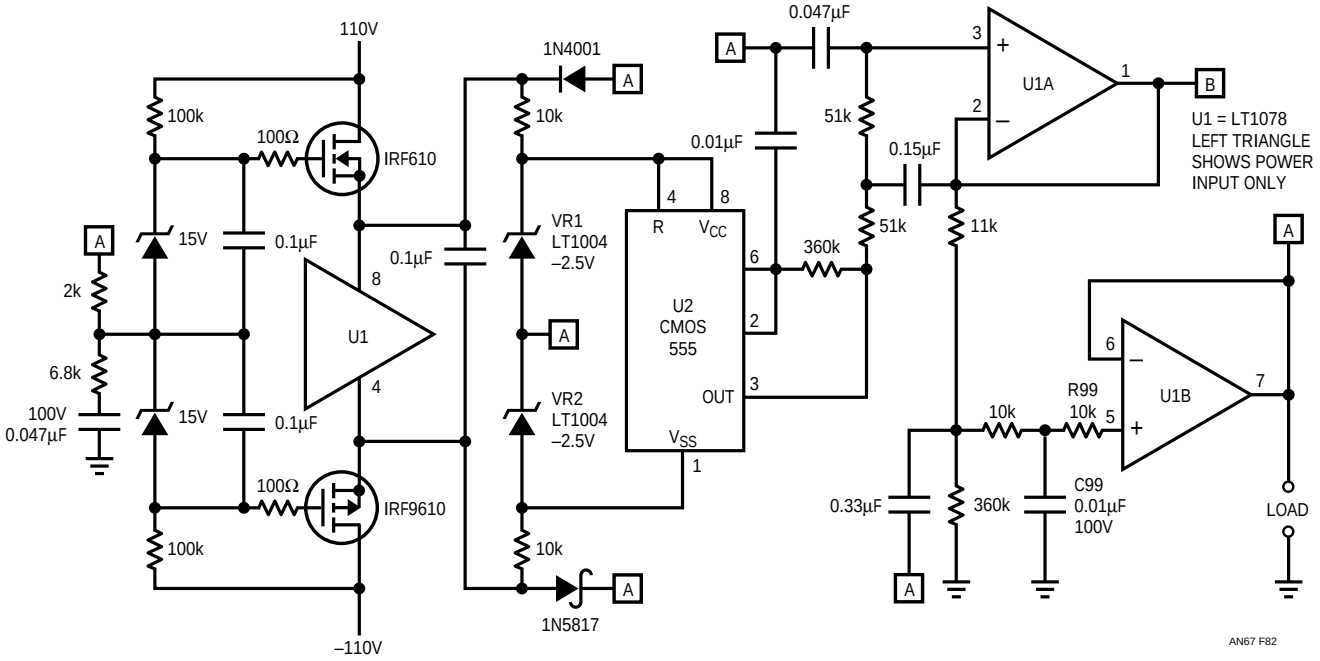


Figure 82. Ring Tone Generator: Oscillator, Filter and Driver

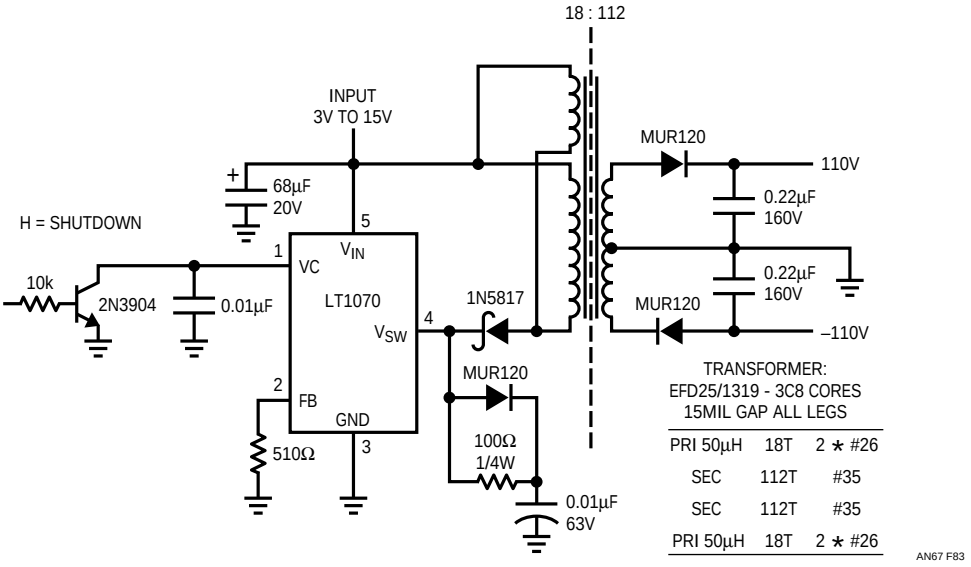


Figure 83. High Voltage Power Supply for Ring Tone Generator

The input current and power versus input voltage for the combination ring-tone generator (Figures 82 and 83) are shown in Figure 84. The output waveform (loaded with one bell) is shown in Figure 85 and the harmonic distortion is shown in Figure 86.

Although somewhat tricky at first, extended supply mode is a valuable tool to get out of many tight places. There is also a great deal of satisfaction to be gathered when making it work, for those of you who love a technical challenge.

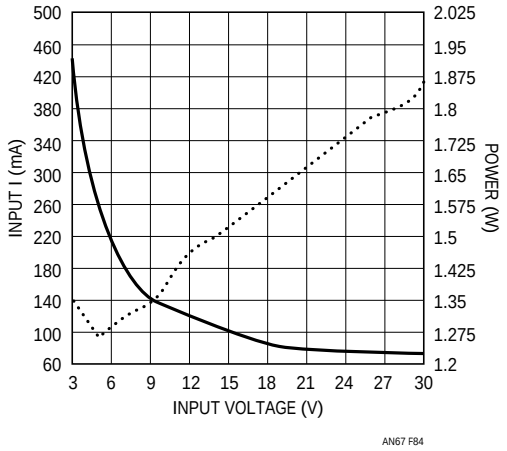


Figure 84. Input Current and Input Power vs Input Voltage While Ringing One Bell for Figure 82 Circuit

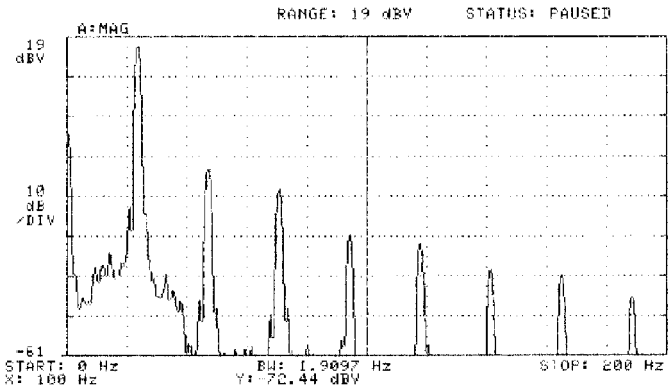


Figure 85. Ring-Tone Generator Frequency Spectrum Plot

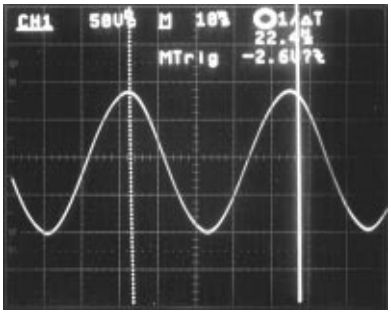


Figure 86. Sine Wave Output from Ring-Tone Generator

USING SUPER OP AMPS TO PUSH TECHNOLOGICAL FRONTIERS: AN ULTRAPURE OSCILLATOR

by Dale Eagar

The advent of high speed op amps allows the implementation of circuits that were impossible just a few years ago. This article describes a new topology that makes use of these new high speed circuits and makes astounding improvements in its performance. An oscillator using such op amps has distortion limits beyond our ability to measure.

An Ultralow Distortion, 10kHz Sine Wave Source for Calibration of 16-Bit or Higher A/D Converters

The path to low distortion in an amplifier or an oscillator begins with amplifiers with the lowest possible open-loop distortion and lots of excess open-loop gain in the frequency band of interest. The next step is closing the loop, thereby reducing open-loop distortion by an amount approximately equal to the loop gain. This is not easy, as certain stability criteria must be met by an amplifier that isn't an oscillator or by an oscillator that oscillates at a specified frequency.

The trick used in this circuit is to build an amplifier that has excessive gain where it is needed but no excess gain or phase shift where it isn't. In many applications the band from DC to 100kHz requires the above mentioned high gain; the gain should fall off when the open-loop gain falls through unity (around 5MHz). How this is done in the flesh (silicon) is shown here.

Circuit Operation and Circuit Evolution

A standard inverting amplifier topology, as shown in Figure 87, has a finite open-loop gain in the frequency band of interest (see Figure 88), with some open-loop harmonic distortion (about –60dB) and an open-loop output impedance of about 70Ω.

The amplifier shown in Figure 87 can achieve low distortion, but since the circuit has a limited loop gain, the curative effects of feedback can only be taken so far. The designer must also be careful to ensure that R_L is many times higher than the open-loop output impedance of U1.

Figure 89's circuit makes several improvements over the circuit of Figure 87. First, the open-loop gain of U1 is multiplied by $A_V(f)$, the gain of the composite amplifier stage A1. Second, the input impedance of A1 can be made very high, further improving both open-loop gain of U1 and the open-loop harmonic distortion of U1. Third, the output voltage swing of U1 is decreased, keeping its output circuitry in its lowest distortion area.

The composite circuit, A1, consists of three sections. The first section, as seen in Figure 90, has the gain/phase plot shown in Figure 92. Note the high gain at 10kHz (60dB) and the gain of 6dB at 5MHz, with only 17 degrees of phase contribution. In fact, this looks so nice that you might ask, "why not use two?" and thus reduce your distortion by an additional 60dB?

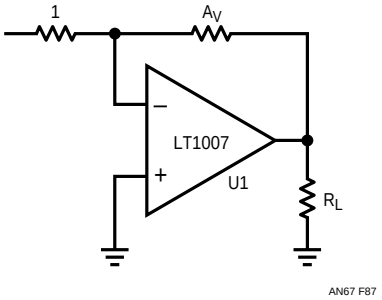


Figure 87. Conventional Inverting Op Amp Topology

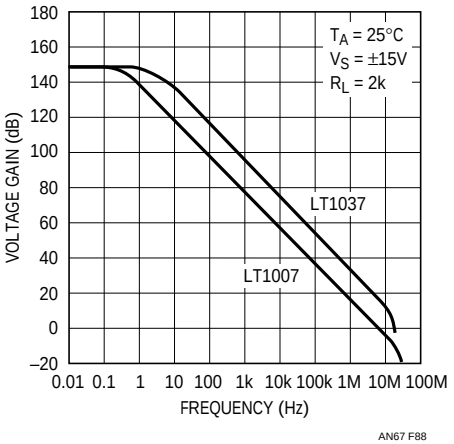


Figure 88. Voltage Gain vs Frequency

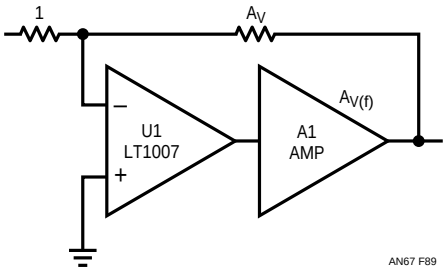


Figure 89. LT1007 Followed by Composite Amplifier A1

The second section, shown in Figure 91, has the gain/phase plot shown in Figure 93. Note that here the gain doesn't change significantly, but the phase is positive just where we want it (1MHz to 5MHz) to allow a very stable system to be built.

The third section, as you might guess, is the same as the first. In sum, the gain/phase plot of the composite amplifier A1 is shown in Figure 94. Note the gain, which is in

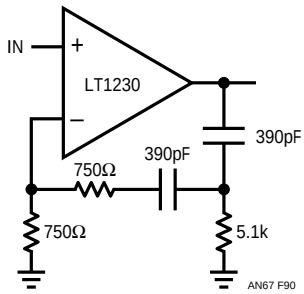


Figure 90. First Section of Composite Amplifier A1

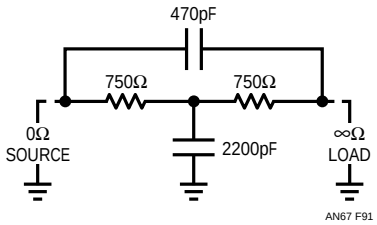


Figure 91. Second Section of Composite Amplifier A1

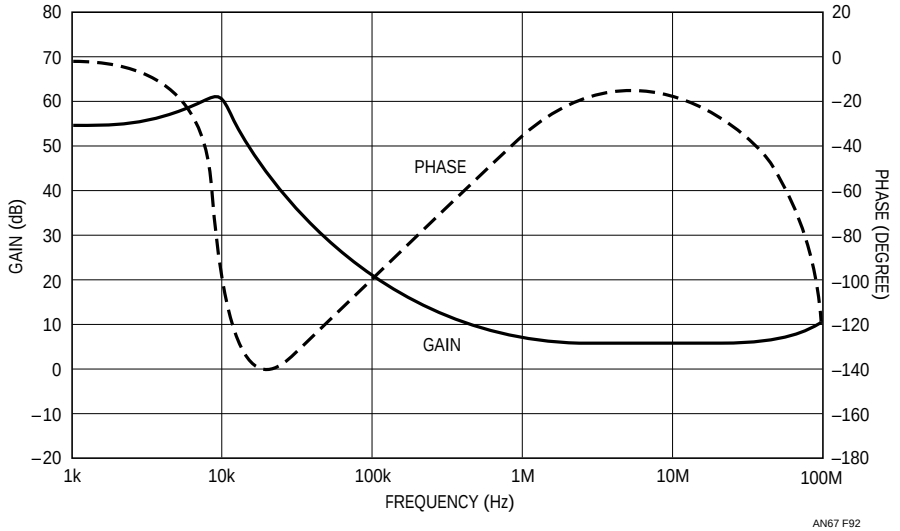


Figure 92. Gain/Phase Response of Circuit Shown in Figure 90

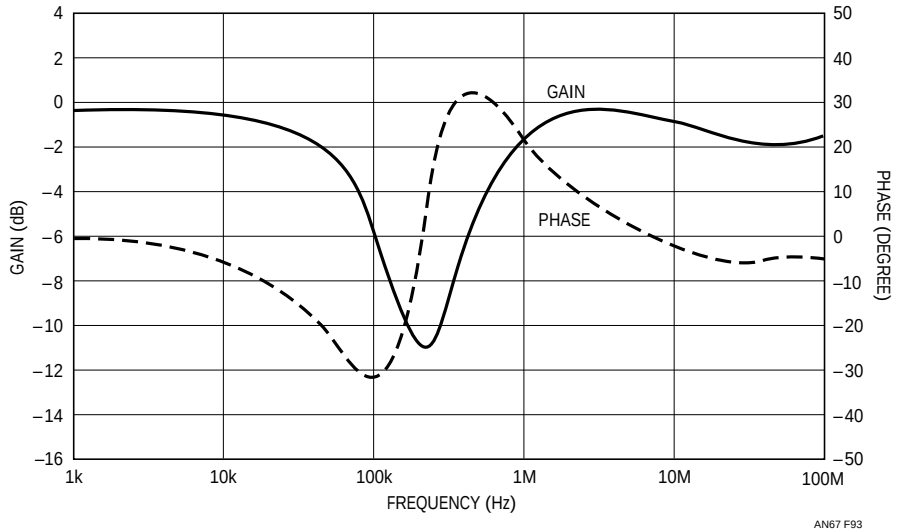


Figure 93. Gain/Phase Response of Circuit Shown in Figure 91

excess of 120db at 10kHz and the total phase contribution of about –20 degrees at 5MHz. The complete gain block is shown in Figure 95.

Super Gain Block Oscillator Circuitry

When A1, as described above is connected with U1, as shown in Figure 89, the resulting circuit is not only unity-gain stable but has open-loop gain of 180dB at 10kHz (yes, 1 billion). This means that the closed-loop harmonic distortion can easily be kept in the region of "parts per billion."

A Wien bridge oscillator with harmonic distortion in the parts per billion is shown in Figure 96. The super op amps S1 and S2 are the previously described composite amplifiers as shown in Figure 95. Note that the output is taken between the two outputs of S1 and S2. This topology gives the best signal-to-noise ratio, in addition to balancing the

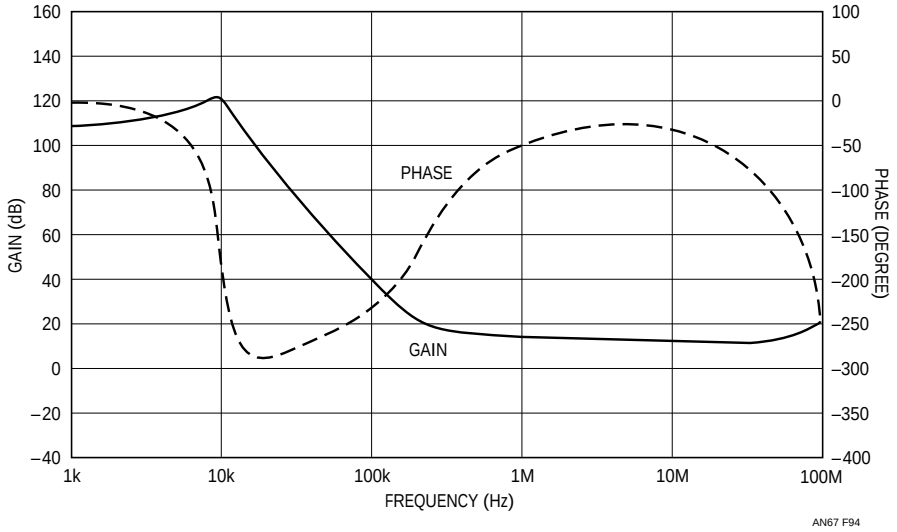


Figure 94. Gain/Phase Response of Composite Amplifier A1 (Shown in Figure 89)

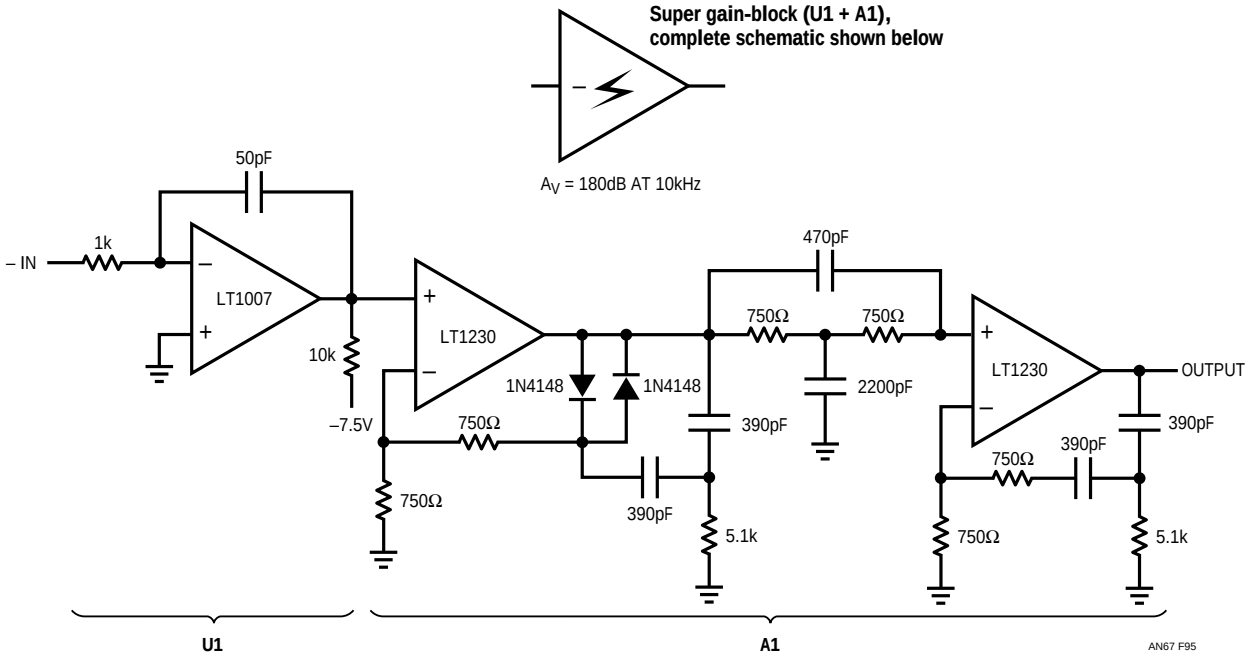


Figure 95. Super Gain Block S1 and S2 Schematic Diagram

power supply currents and their harmonics. Taking the output from one amplifier's output to ground is also valid.

To align the circuit, first center the output amplitude adjustment potentiometer. Next, adjust the gain trim for oscillation while also adjusting the output amplitude for $5V_{P-P}$ output (single ended). Next, adjust the gain trim to $1V_{P-P}$ at the output of the LT1228. Finally, connect a spectrum analyzer to the output of the LT1228 and adjust the second harmonic trim potentiometer for a null in the second harmonic of the oscillator frequency. The measurement of the harmonic distortion of this oscillator defies all of our resources, but appears to be well into the parts-per-billion range.

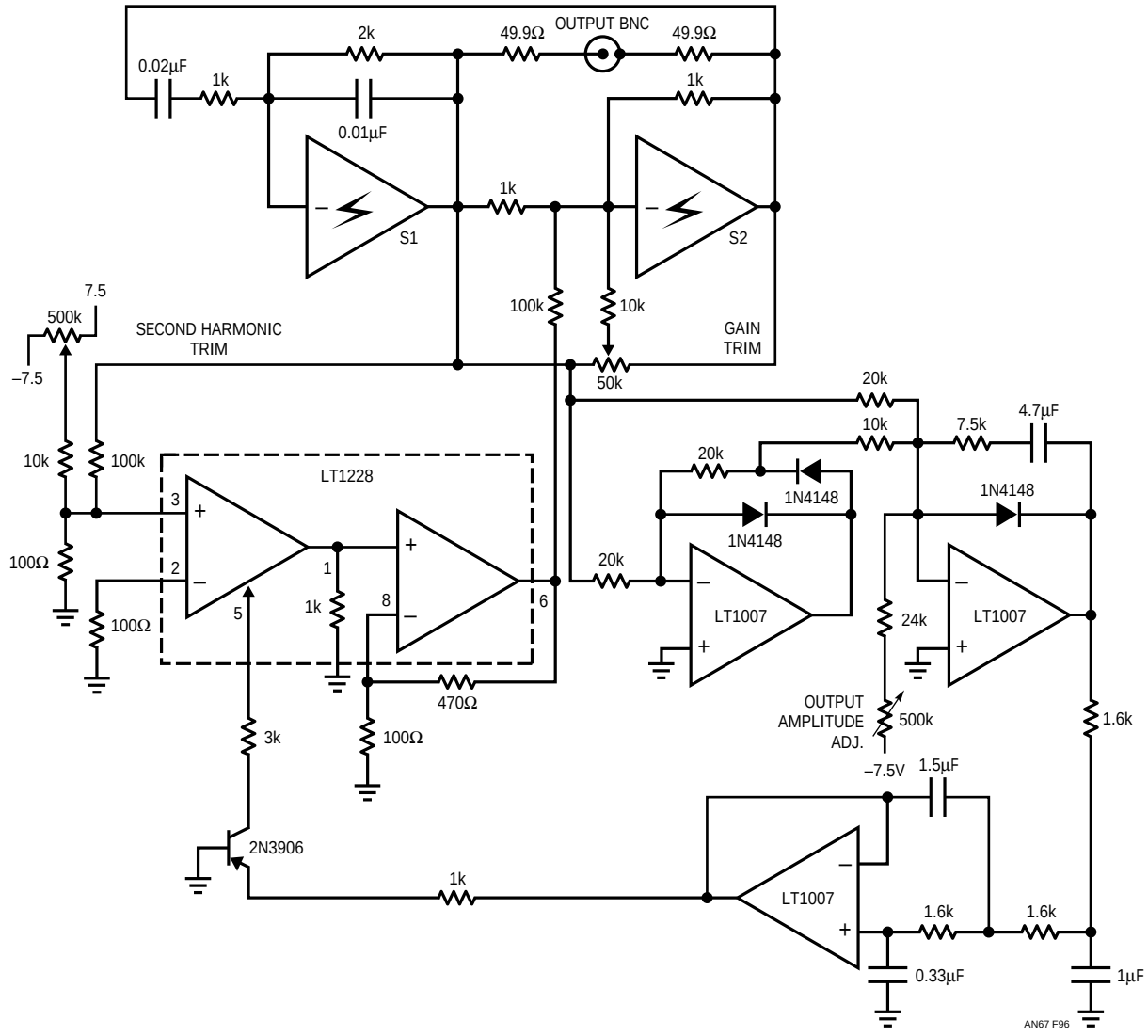


Figure 96. Schematic Diagram: Wien Bridge Oscillator with Distortion in the Parts-per-Billion Range

FAST VIDEO MUX USES LT1203/LT1205

by Frank Cox

To demonstrate the switching speed of the LT1203/LT1205, the RGB MUX of Figure 97 is used to switch the inputs of an RGB workstation with a 22ns pixel width. Figure 98a is a photo showing the workstation output and RGB MUX output. The slight rise time degradation at the RGB MUX output is due to the bandwidth of the LT1260 current feedback amplifier used to drive the 75Ω cable. In Figure 98b the LT1203 switches at the end of the first pixel to an input at zero and removes the following pixels.

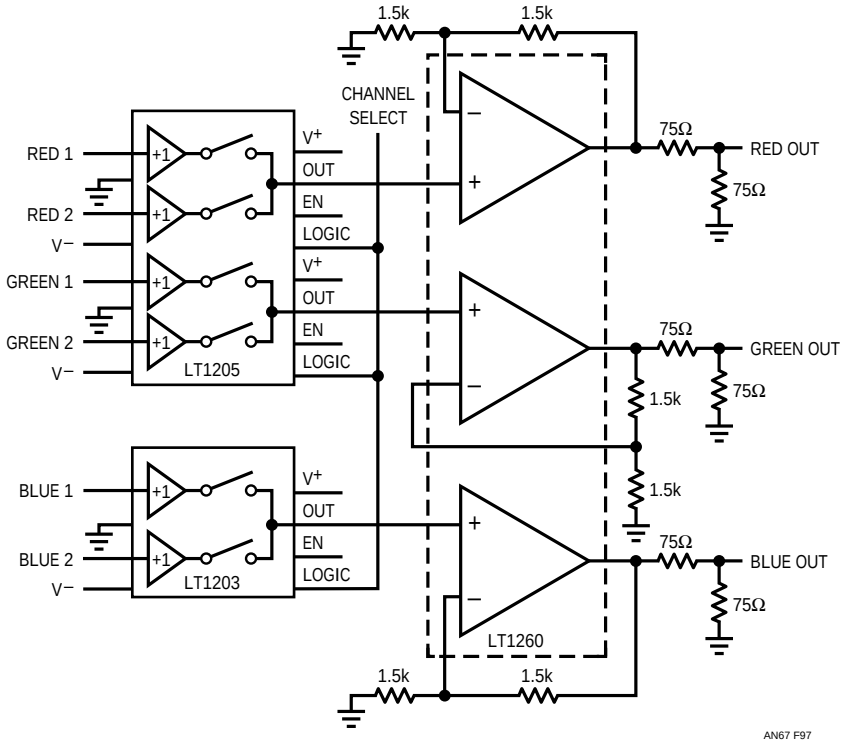


Figure 97. Fast RGB MUX

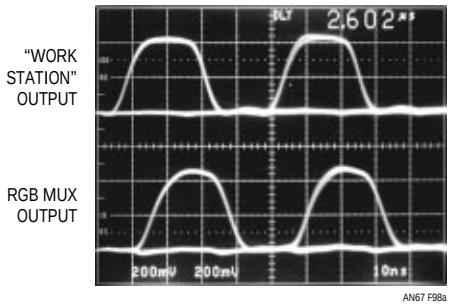


Figure 98a. Workstation and RGB MUX Output

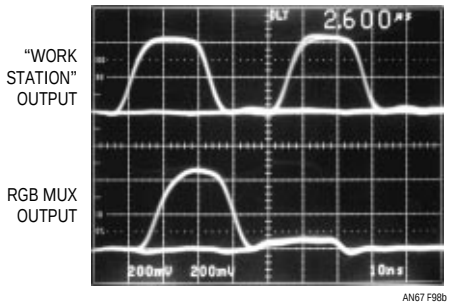


Figure 98b. RGB MUX Output Switched to Ground After One Pixel

USING A FAST ANALOG MULTIPLEXER TO SWITCH VIDEO SIGNALS FOR NTSC "PICTURE-IN-PICTURE" DISPLAYS

by Frank Cox

Introduction

The majority of production[1] video switching consists of selecting one video source out of many for signal routing or scene editing. For these purposes, the video signal is switched during the vertical interval in order to reduce visual switching transients. The image is blanked during this time, so if the horizontal and vertical synchronization and subcarrier lock are maintained, there will be no visible artifacts. Although vertical interval switching is adequate for most routing functions, there are times when it is desirable to switch two synchronous video signals during the active (visible) portion of the line to obtain picture-in-picture, key or overlay effects. Picture-in-picture or active video switching requires signal-to-signal transitions that are both clean and fast. A clean transition should have a minimum of preshoot, overshoot, ringing or other aberrations commonly lumped under the term "glitching."

Using the LT1204

A quality high speed multiplexer amplifier can be used with good results for active video switching. The important specifications for this application are small, controlled switching glitch, good switching speed, low distortion, good dynamic range, wide bandwidth, low path loss, low channel-to-channel crosstalk and good channel-to-channel offset matching. The LT1204 specifications match these requirements quite well, especially in the areas of bandwidth, distortion and channel-to-channel crosstalk (which is an outstanding 90dB at 10MHz). The LT1204 was evaluated for use in active video switching with the test setup shown in Figure 99. Figure 100 shows the video waveform of a switch between a 50% white level and a 0% white level about 30% into the active interval and back again at about 60% of the active interval. The switch artifact is brief and well controlled. Figure 101 is an expanded view of the same waveform. When viewed on a monitor, the switch artifact is just visible as a very fine

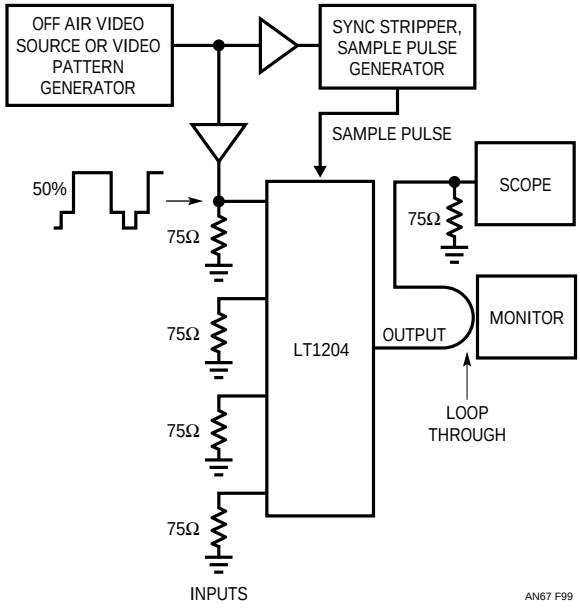


Figure 99. "Picture-in-Picture" Test Setup

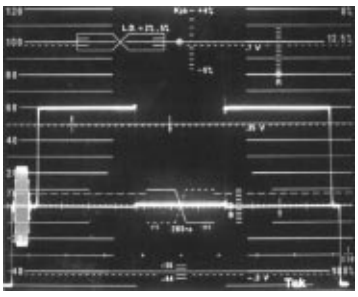


Figure 100. Video Waveform Switched from 50% White Level to 0% White Level and Back

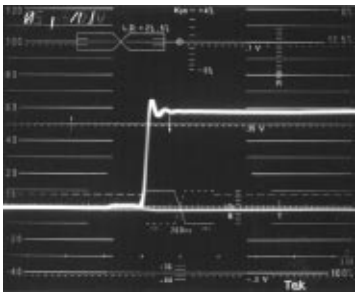


Figure 101. Expanded View of Rising Edge of LT1204 Switching from 0% to 50% (50ns Horizontal Division)

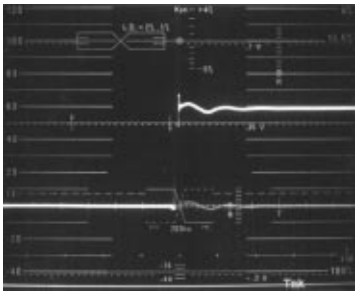


Figure 102. Expanded View of "Brand-X" Switch 0% to 50% Transition

line. The lower trace is a switch between two black level (0V) video signals showing a very slight channel-to-channel offset, which is not visible on the monitor. Switching between two DC levels is a worst-case test, as almost any active video will have enough variation to totally obscure this small switch artifact.

Video Switching Caveats

In a video processing system that has a large bandwidth compared to the bandwidth of the video signal, a fast transition from one video level to another (with a low amplitude glitch) will cause minimal visual disturbance. This situation is analogous to the proper use of an analog oscilloscope. In order to make accurate measurement of pulse waveforms, the instrument must have much more bandwidth than the signal in question (usually five times the highest frequency). Not only should the glitch be small, it should be otherwise well controlled. A switching glitch that has a long settling "tail" can be more troublesome (that is, more visible) than one that has more amplitude but decays quickly. The LT1204 has a switching glitch that is not only low in amplitude but well controlled and quickly damped. Refer to Figure 102, which shows a video multiplexer that has a long, slow-settling tail. This sort of distortion is highly visible on a video monitor.

Composite video systems, such as NTSC, are inherently band limited and thus edge-rate limited. In a sharply band limited system, the introduction of signals that contain significant energy higher in frequency than the filter cutoff will cause distortion of transient waveforms (see Figure 103). Filters used to control the bandwidth of these video systems should be group-delay equalized to minimize this pulse distortion. Additionally, in a band limited system, the edge rates of switching glitches or level-to-level transitions should be controlled to prevent ringing and other pulse aberrations that could be visible. In practice, this is usually accomplished with pulse-shaping networks (Bessel filters are one example). Pulse-shaping networks and delay equalized filters add cost and complexity to video systems and are usually found only on expensive equipment. Where cost is a determining factor in system design, the exceptionally low amplitude and brief duration of the LT1204's switching artifact make it an excellent choice for active video switching.

Some Definitions—

"Picture in picture" refers to the production effect in which one video image is inserted within the boundaries of another. The process may be as simple as splitting the screen down the middle or it may involve switching the two images along a complicated geometric boundary. In order to make the composite picture stable and viewable, both video signals must be in horizontal and vertical sync. For composite color signals the signals must also be in subcarrier lock.

"Keying" is the process of switching among two or more video signals, triggering on some characteristic of one of the signals. For instance, a chroma keyer will switch on the presence of a particular color. Chroma keyers are used to insert a portion of one scene into another. In a commonly used effect, the TV weather person (the "talent") appears to be standing in front of a computer generated weather map. Actually, the talent is standing in front of a specially colored background; the weather map is a separate video signal which has been carefully prepared to contain none of that particular color. When the chroma keyer senses the keying color, it switches to the weather map background. Where there is no keying color, the keyer switches to the talent's image.

[1] Video production, in the most general sense, means any purposeful manipulation of the video signal, whether in a television studio or on a desktop PC.

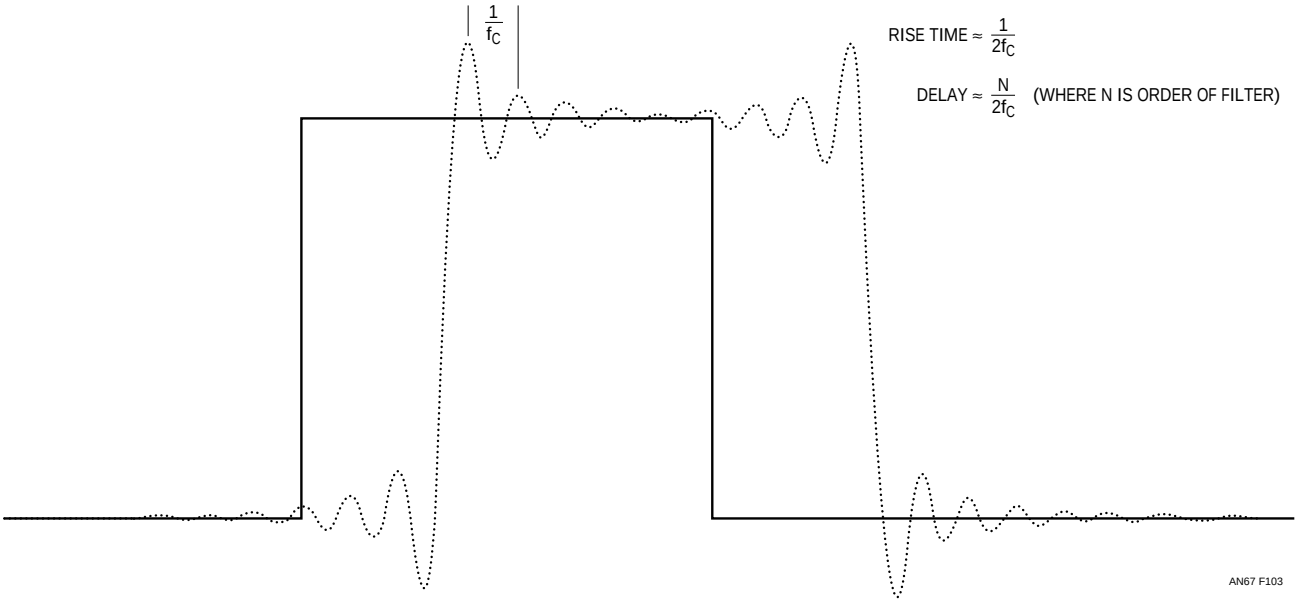


Figure 103. Pulse Response of an Ideal Sharp Cutoff Filter at Frequency f_C

APPLICATIONS FOR THE LT1113 DUAL JFET OP AMP

by Alexander Strong

Figure 104 shows a low noise hydrophone amplifier with a DC servo. Here one half (A) of the LT1113 is configured in the noninverting mode to amplify a voltage signal from the hydrophone, and the other half (B) of the LT1113 nulls errors due to voltage and current offsets of amplifier A and to null out DC errors of the hydrophone. The value of C1 depends on the capacitance of the hydrophone, which can range from 200pF to 8000pF. The time constant of the servo should be larger than the time constant of the hydrophone capacitance and the 100M source resistance. This will prevent the servo from canceling the low frequency signals from the hydrophone.

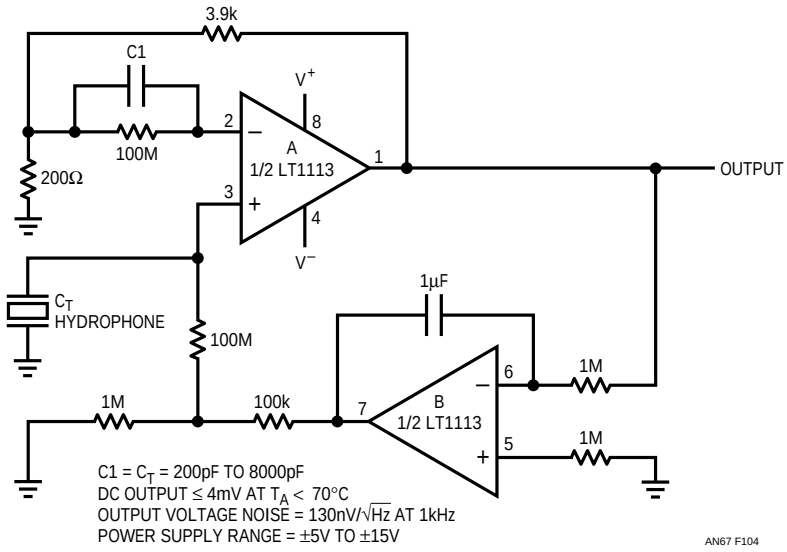


Figure 104. Low Noise Hydrophone Amplifier with DC Servo

Another popular charge-output transducer is the accelerometer. Since precision accelerometers are charge-output devices, the inverting mode is used to convert the transducer charge to an output voltage. Figure 105 is an example of an accelerometer with a DC servo. The charge from the transducer is converted to a voltage by C1, which should equal the transducer capacitance plus the input capacitance of the op amp. The noise gain will be 1 + C1/C_T. The low frequency bandwidth of the amplifier will depend on the value of R1 • C1 (or R1 (1 + R2/R3) for a Tee network). As with the hydrophone example, the time constant of the servo (1/R5C5) should be larger than the time constant of the amplifier (1/R1C1).

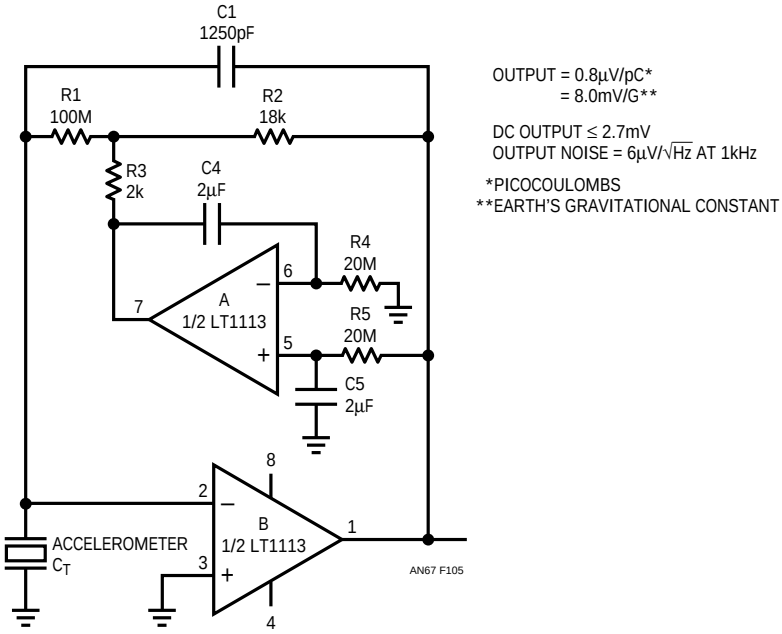


Figure 105. Accelerometer Amplifier with DC Servo

LT1206 AND LT1115 MAKE LOW NOISE AUDIO LINE DRIVER

by William Jett

Although the wide bandwidth and high output drive capabilities of the LT1206 make it a natural for video circuits, these characteristics are also useful for audio applications. Figure 106 shows the LT1206 combined with the LT1115 low noise amplifier to form a very low noise, low distortion audio buffer with a gain of 10. With a 32Ω load and a $5V_{RMS}$ output level (780mW), the THD + noise for the circuit is 0.0009% at 1kHz, rising to 0.004% at 20kHz. The frequency response is flat to 0.1dB from DC to 600kHz, with a –3dB bandwidth of 4MHz. The circuit is stable with capacitive loads of 250pF or less.

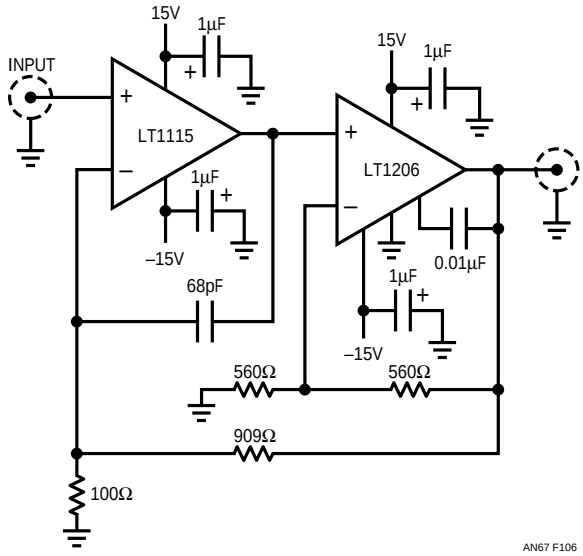


Figure 106. Low Noise × 10 Buffered Line Driver

DRIVING MULITPLE VIDEO CABLES WITH THE LT1206

by William Jett

The combination of a 60MHz bandwidth, 250mA output current capability and low output impedance makes the LT1206 ideal for driving multiple video cables. One concern when driving multiple transmission lines is the effect of an unterminated (open) line on the other outputs. Since the unterminated line creates a reflected wave that is incident on the output of the driver, a nonzero amplifier output impedance will result in crosstalk to the other lines.

Figure 107 shows the LT1206 connected as a distribution amplifier. Each line is separately terminated to minimize the effect of reflections. For systems using composite video, the differential gain and phase performance are also important and have been considered in the internal design of the device. The differential phase and differential gain performance versus supply is shown in Figures 108 and 109 for 1, 3, 5 and 10 cables. Figure 110 shows the output impedance versus frequency. Note that at 5MHz the output impedance is only 0.6Ω.

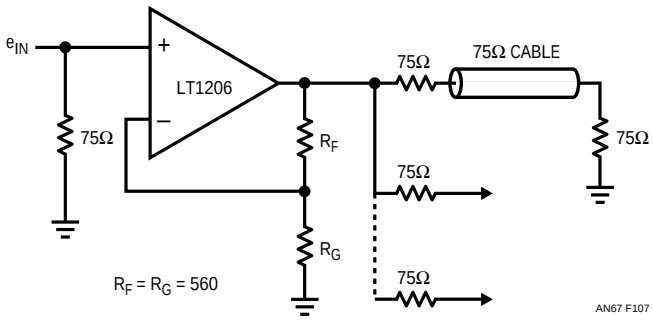


Figure 107. LT1206 Distribution Amplifier

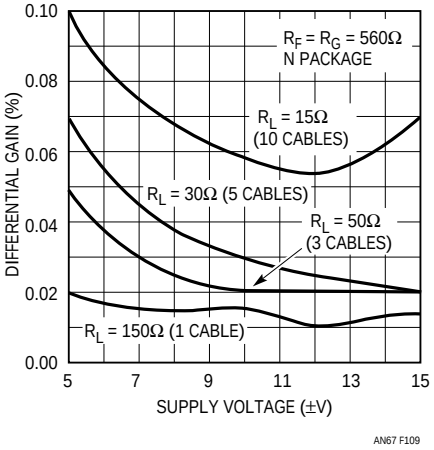


Figure 109. Differential Gain vs Supply Voltage

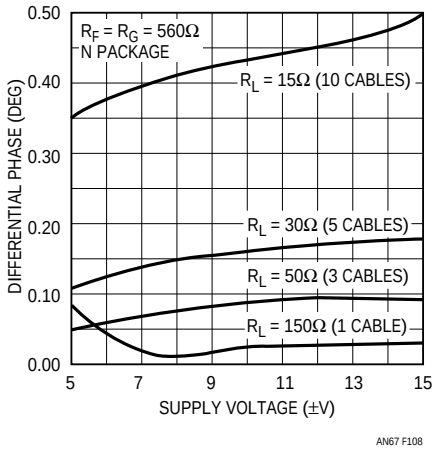


Figure 108. Differential Phase vs Supply Voltage

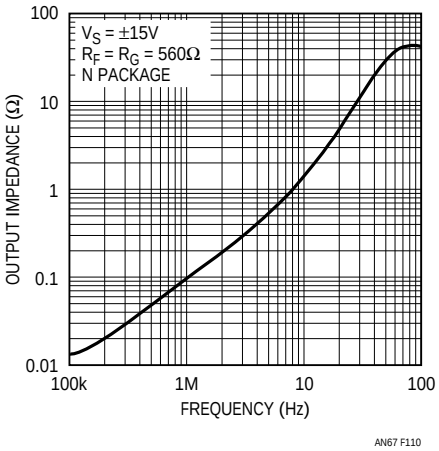


Figure 110. Output Impedance vs Frequency

OPTIMIZING A VIDEO GAIN CONTROL STAGE USING THE LT1228

by Frank Cox

Video automatic gain control (AGC) systems require a voltage- or current-controlled gain element. The performance of this gain-control element is often a limiting factor in the overall performance of the AGC loop. The gain element is subject to several, often conflicting, restraints. This is especially true of AGC for composite color video systems such as NTSC, which have exacting phase and gain distortion requirements. To preserve the best possible signal-to-noise ratio (S/N),[1] it is desirable for the input signal level to be as large as practical. Obviously, the larger the input signal the less the S/N will be degraded by the noise contribution of the gain control stage. On the other hand, the gain control element is subject to dynamic range constraints and exceeding these will result in rising levels of distortion.

Linear Technology makes a high speed transconductance (g_m) amplifier, the LT1228, which can be used as a quality, inexpensive gain control element in color video and some lower frequency RF applications. Extracting the optimum performance from video AGC systems takes careful attention to circuit details.

As an example of this optimization, consider the typical gain control circuit using the LT1228 shown in Figure 111. The input is NTSC composite video, which can cover a 10dB range, from 0.56V to 1.8V. The output is to be 1V peak-to-peak into 75Ω. Amplitudes were measured from peak negative chroma to peak positive chroma on an NTSC modulated ramp test signal (see page 74).

Notice that the signal is attenuated 20:1 by the 75Ω attenuator at the input of the LT1228, so the voltage on the input (Pin 3) ranges from 0.028V to 0.090V. This is done to limit distortion in the transconductance stage. The gain of this circuit is controlled by the current into the I_{SET} terminal, Pin 5 of the IC. In a closed-loop AGC system the loop control circuitry generates this current by comparing the output of a detector[2] to a reference voltage, integrating the difference and then converting to a suitable current. The measured performance for this circuit is presented in Table 1.

Table 1. Measured Performance Data (Uncorrected)

INPUT (V)	I_{SET} (mA)	DIFFERENTIAL GAIN	DIFFERENTIAL PHASE	S/N
0.03	1.93	0.5%	2.7°	55dB
0.06	0.90	1.2%	1.2°	56dB
0.09	0.584	10.8%	3.0°	57dB

All video measurements were taken with a Tektronix 1780R video measurement set, using test signals generated by a Tektronix TSG 120. The standard criteria for characterizing NTSC video color distortion are the differential gain and the differential phase. For a brief explanation of these tests see "Differential Gain and Phase" page 74. For this design exercise the distortion limits were set at a somewhat arbitrary 3% for differential gain and 3° for differential phase. Depending on conditions, this should be barely visible on a video monitor.

Figures 112 and 113 plot the measured differential gain and phase, respectively, against the input signal level (the

[1] Signal to noise ratio, S/N = 20 × log(RMS signal/RMS noise).

[2] One way to do this is to sample the colorburst amplitude (the nominal peak-to-peak amplitude of the colorburst for NTSC is 40% of the peak luminance) with a sample-and-hold and peak detector.

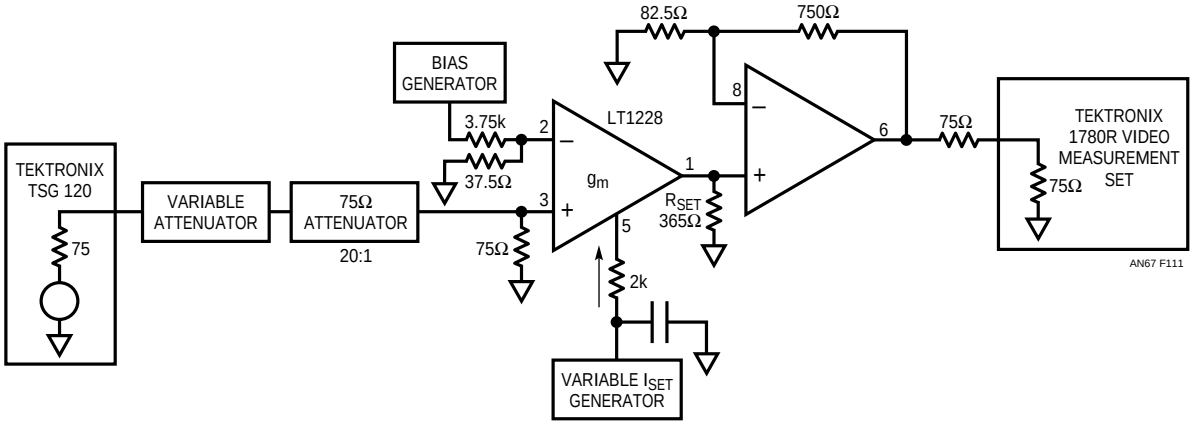


Figure 111. Schematic Diagram

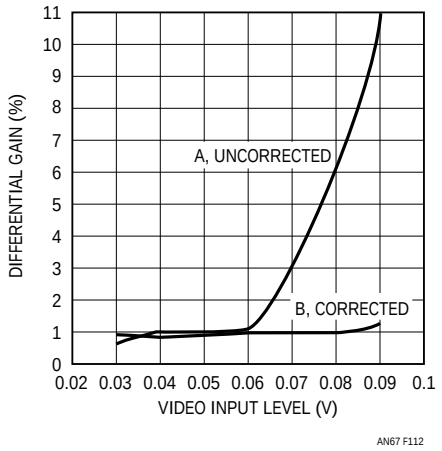


Figure 112. Differential Gain vs Input Level

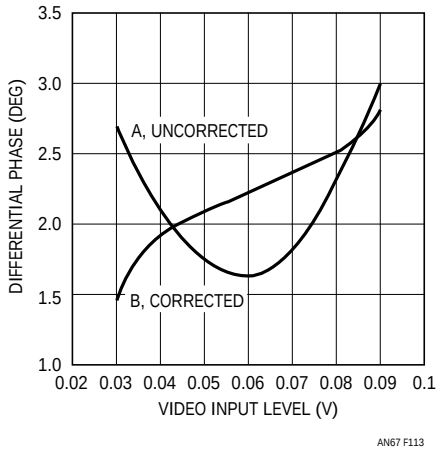


Figure 113. Differential Phase vs Input Level

curves labeled "A" show the uncorrected data from Table 1). The plots show that increasing the input signal level beyond 0.06V results in a rapid increase in the gain distortion, but comparatively little change in the phase distortion. Further attenuating the input signal (and consequently increasing the set current) would improve the differential gain performance but degrade the S/N. What this circuit needs is a good tweak.

Optimizing for Differential Gain

Referring to the small-signal transconductance versus DC input voltage graph (Figure 114), observe that the transconductance of the amplifier is linear over a region centered around 0V.[3] The 25°C g_m curve starts to become quite nonlinear above 0.050V. This explains why the differential gain (see Figure 112, curve A) degrades so quickly with signals above this level. Most RF signals do

[3]Notice also that the linear region expands with higher temperature. Heating the chip has been suggested.

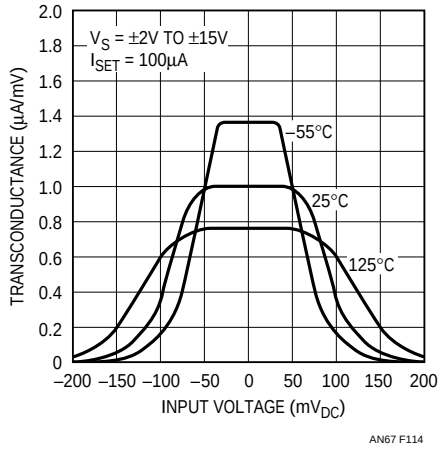


Figure 114. Small-Signal Transconductance vs DC Input Voltage

not have DC bias levels but the composite video signal is mostly unipolar.

Video is usually clamped at some DC level to allow easy processing of sync information. The sync tip, the chroma reference burst and some chroma signal information swing negative, but 80% of the signal that carries the critical color information (chroma) swings positive. Efficient use of the dynamic range of the LT1228 requires that the input signal have little or no offset. Offsetting the video signal so that the critical part of the chroma waveform is centered in the linear region of the transconductance amplifier allows a larger signal to be input before the onset of severe distortion. A simple way to do this is to bias the unused input (in this circuit the inverting input, Pin 2) with a DC level.

In a video system, it might be convenient to clamp the sync tip at a more negative voltage than usual. Clamping the signal prior to the gain-control stage is good practice because a stable DC reference level must be maintained.

The optimum value of the bias level on Pin 2 used for this evaluation was determined experimentally to be about 0.03V. The distortion tests were repeated with this bias voltage added. The results are reported in Table 2 and Figures 112 and 113 (curves B). The improvement to the differential phase is inconclusive, but the improvement in the differential gain is substantial.

Table 2. Measured Performance Data (Corrected)

INPUT (V)	BIAS VOLTAGE	I_{SET} (mA)	DIFFERENTIAL GAIN	DIFFERENTIAL PHASE	S/N
0.03	0.03	1.935	0.9%	1.45°	55dB
0.06	0.03	0.889	1.0%	2.25°	56dB
0.09	0.03	0.584	1.4%	2.85°	57dB

Differential Gain and Phase

Differential gain and phase are sensitive indications of chroma signal distortion. The NTSC system encodes color information on a separate subcarrier at 3.579545MHz. The color subcarrier is directly summed to the black and white video signal. (The black and white information is a voltage proportional to image intensity and is called luminance or luma.) Each line of video has a burst of 9 to 11 cycles of the subcarrier (so timed that it is not visible) that is used as a phase reference for demodulation of the color information of that line. The color signal is relatively immune to distortions, except for those that cause a phase shift or an amplitude error to the subcarrier during the period of the video line.

Differential gain is a measure of the gain error of a linear amplifier at the frequency of the color subcarrier. This distortion is measured with a test signal called a modulated ramp (shown in Figure 115). The modulated ramp consists of the color subcarrier frequency superimposed on a linear ramp (or sometimes on a stair step). The ramp has the duration of the active portion of a horizontal line of video. The amplitude of the ramp varies from zero to the maximum level of the luminance, which in this case, is 0.714V. The gain error corresponds to compression or expansion by the amplifier (sometimes called "incremental gain") and is expressed as a percentage of the full amplitude range. An appreciable amount of differential gain will cause the luminance to modulate the chroma, producing visual chroma distortion. The effect of differential gain errors is to change the saturation of the color being displayed. Saturation is the relative degree of dilution of a pure color with white. A 100% saturated color has 0% white, a 75% saturated color has 25% white, and so on. Pure red is 100% saturated, whereas pink is red with some percentage of white and is therefore less than 100% saturated.

Differential phase is a measure of the phase shift in a linear amplifier at the color subcarrier frequency when the modulated ramp signal is used as an input.

The phase shift is measured relative to the colorburst on the test waveform and is expressed in degrees. The visual effect of the distortion is a change in hue. Hue is that quality of perception which differentiates the frequency of the color, red from green, yellow-green from yellow, and so forth.

Three degrees of differential phase is about the lower limit that can unambiguously be detected by observers. This level of differential phase is just detectable on a video monitor as a shift in hue, mostly in the yellow-green region. Saturation errors are somewhat harder to see at these levels of distortion—3% of differential gain is very difficult to detect on a monitor. The test is performed by switching between a reference signal, SMPTE (Society of Motion Picture and Television Engineers) 75% color bars and a distorted version of the same signal, with matched signal levels. An observer is then asked to note any difference.

In professional video systems (studios, for instance) cascades of processing and gain blocks can reach hundreds of units. In order to maintain a quality video signal, the distortion contribution of each processing block must be a small fraction of the total allowed distortion budget[4] (the errors are cumulative). For this reason, high quality video amplifiers will have distortion specifications as low as a few thousandths of a degree for differential phase and a few thousandths of a percent for differential gain.

[4] From the preceding discussions, the limits on visibility are about 3° differential phase, 3% differential gain. Please note that these are not hard and fast limits. Tests of perception can be very subjective.

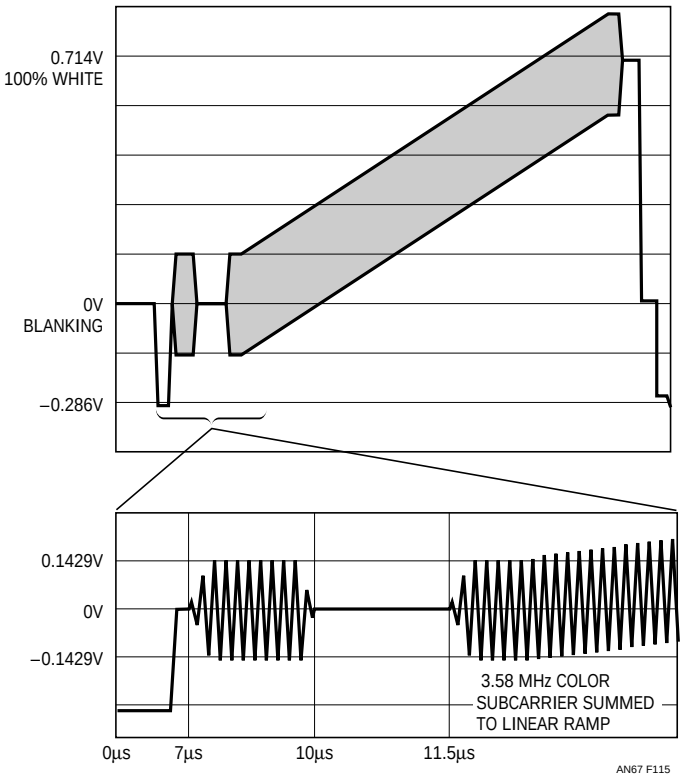


Figure 115. NTSC Test Signal

LT1190 FAMILY ULTRAHIGH SPEED OP AMP CIRCUITS

by John Wright and Mitchell Lee

Introduction

The LT1190 series op amps combine bandwidth, slew rate and output drive capability to satisfy the demands of many high speed applications. This family offers up to 350MHz gain bandwidth product and slew rates of 450V/µs while driving 150Ω (75Ω, double terminated) loads. In 50Ω systems, the LT1190 family can deliver 13.5dBm to a double terminated load. These parts are based on the familiar, easy-to-use, voltage mode feedback topology.

Small-Signal Performance

Figures 116 and 117 show the small-signal performance of the LT1190 and LT1191 when configured for gains of +1 and –1. The noninverting plots show peaking at 130MHz, which is characteristic of the socketed test fixture and supply bypass components. A tight PC board layout would reduce the LT1190 peaking to 2dB. The small-signal performance of an LM118 is shown for comparison.

Fast Peak Detectors

Fast peak detectors place unusual demands on amplifiers. The output stage must have a high slew rate in order to keep up with the intermediate stages of the amplifier. This condition causes either a long overload or DC accuracy errors. To maintain a high slew rate at the output, the amplifier must deliver large currents into the capacitive load of the detector. Other problems include amplifier instability with large capacitive loads and preservation of output voltage accuracy.

The LT1190 is the ideal candidate for this application, with a 450V/µs slew rate, 50mA output current and 70° phase margin. The closed-loop peak detector circuit of Figure 118 uses a Schottky diode inside the feedback loop to obtain good accuracy. A 20Ω resistor (R_O) isolates the 10nF load and prevents oscillation.

DC error with a sine wave input is plotted in Figure 119 for various input amplitudes. The DC value is read with a DVM. At low frequencies, the error is small and is dominated by the decay of the detector capacitor between cycles. As frequency rises, the error increases because capacitor charging time decreases. During this time the overdrive becomes a very small portion of a sine wave cycle. Finally, at approximately 4MHz, the error rises rapidly owing to the slew-rate limitation of the op amp. For comparison purposes, the error of an LM118 is also plotted for $V_{IN} = 2V_{P-P}$.

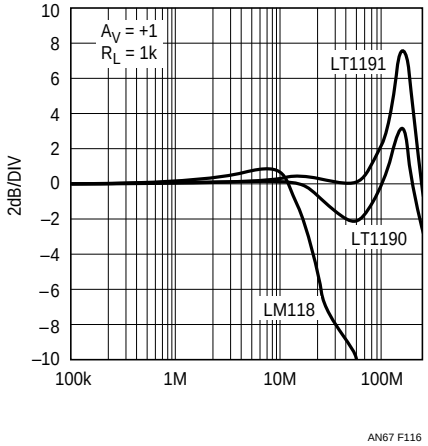


Figure 116. Small-Signal Response A_V = +1. 130MHz Peaking Due to Socket and Bypass Components

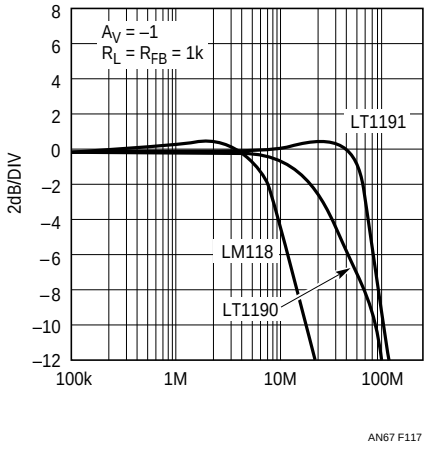


Figure 117. Small-Signal Response A_V = –1

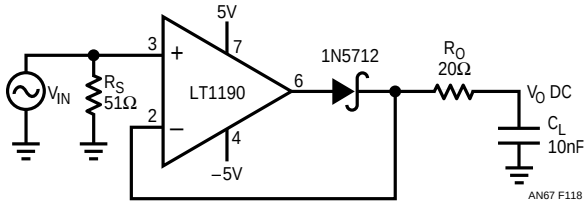


Figure 118. Closed-Loop Peak Detector

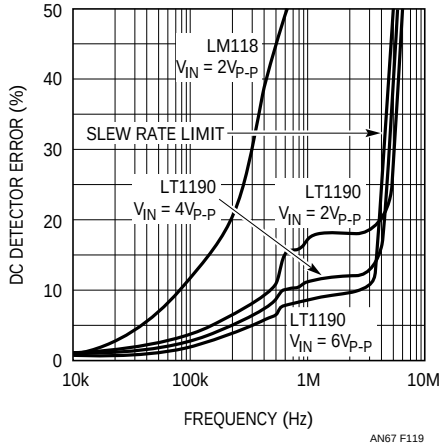


Figure 119. Closed-Loop Peak Detector Error vs Frequency

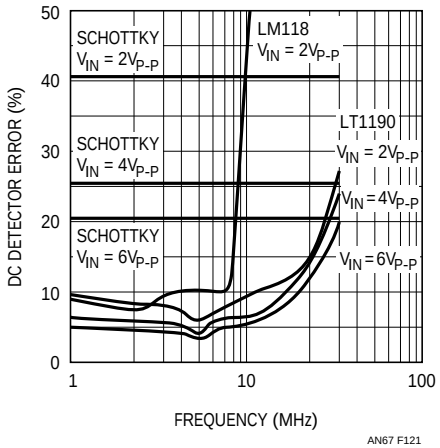


Figure 121. Open-Loop Peak Detector Error vs Frequency

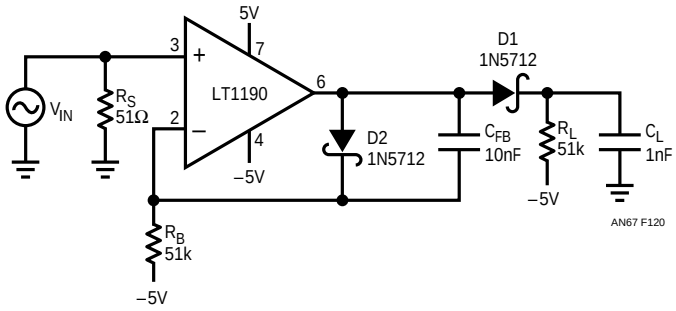


Figure 120. Open-Loop, High Speed Peak Detector

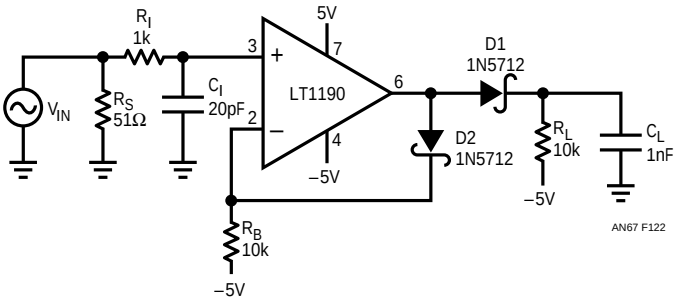


Figure 122. Fast Pulse Detector

A Schottky diode peak detector can be built with a 1nF capacitor and a 10kΩ pulldown. Although this simple circuit is very fast, it has limited usefulness because of the error of the diode threshold and its low input impedance. The accuracy of this simple detector can be improved with the LT1190 circuit of Figure 120.

In this open loop design, D1 is the detector diode and D2 is a level shifting or compensating diode. A load resistor, R_L, is connected to –5V and an identical bias resistor, R_B, is used to bias the compensating diode. Equal value resistors ensure that the diode drops are equal. Low values of R_L and R_B (1k to 10k) provide fast response, but at the expense of poor low frequency accuracy. High values of R_L and R_B provide good low frequency accuracy but cause the amplifier to slew rate limit, resulting in poor high frequency accuracy. A good compromise can be made by adding a feedback capacitor, C_{FB}, which enhances the negative slew rate on the (–) input.

The DC error with a sine wave input, as read with a DVM, is plotted in Figure 121. For comparison purposes the LM118 error is plotted as well as the error of the simple Schottky detector.

Pulse Detector

A fast pulse detector can be made with the circuit of Figure 122. A very fast input pulse will exceed the amplifier's slew rate and cause a long overload recovery time. Some amount of dV/dt limiting on the input can help this overload condition; however, it will delay the response.

Figure 123 shows the detector error versus pulse width. Figure 124 is the response to a 4V_{P-P} input pulse that is 80ns wide. The maximum output slew rate in the photo is 70V/µs. This rate is set by the 70mA current limit driving 1nF. As a performance benchmark, the LM118 takes 1.2µs to peak detect and settle, given the same amplitude input.

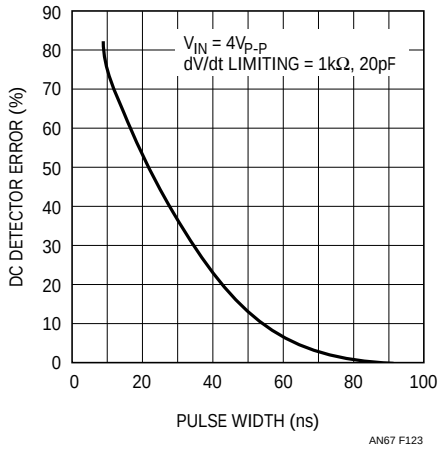


Figure 123. Detector Error vs Pulse Width

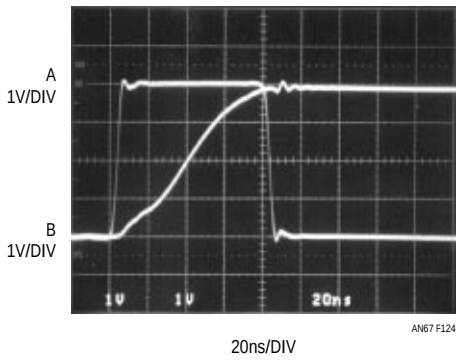


Figure 124. Open-Loop Peak Detector Response

This slower response is due in part to the much lower slew rate and lower phase margin of the LM118.

Instrumentation Amplifier Rejects High Voltage

Instrumentation amplifiers are normally used to process slowly varying outputs from transducers, rather than fast signals. However, it is possible to make an instrumentation amplifier that responds very quickly, with good common mode rejection. For the circuit of Figure 125, an LT1192 is used to obtain 50dB of CMRR from a 120V_{P-P} signal. In this application, the CMRR is limited by the matching of the resistors, which should match to better than 0.01%.

An LT1192 is used in this application because the circuit has a noise gain of 100 and because the higher gain

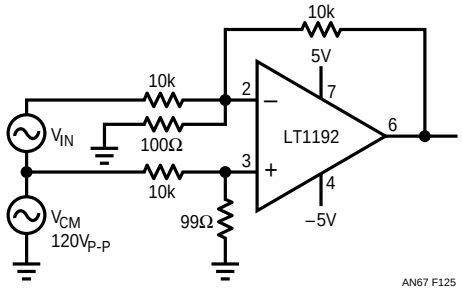


Figure 125. 3.5MHz Instrumentation Amplifier Rejects 120V_{P-P}

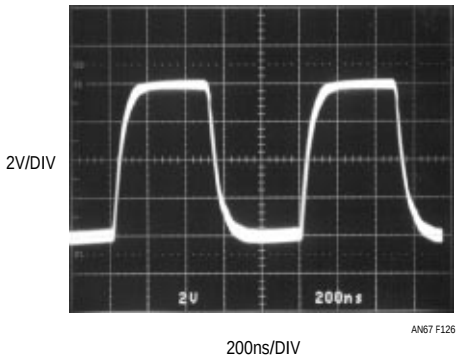


Figure 126. Open-Loop Peak Detector Response

bandwidth of the LT1192 allows a –3dB bandwidth of 3.5MHz. Note also that the 100:1 attenuation of the common mode signal presents a common mode voltage to the amplifier of only 1.2V_{P-P}. Figure 126 shows the amplifier output for a 1MHz square wave riding on a 120V_{P-P}, 60Hz signal. The circuit exhibits 50dB rejection of the common mode signal.

Crystal Oscillator

Op amps have found wide use in low frequency (≤100kHz) crystal oscillator circuits, but just haven't had the bandwidth to operate successfully at higher frequencies. The LT1190 and LT1191 make excellent gain stages for high-frequency Colpitts oscillators. A practical implementation is shown in Figure 127.

Gain limiting is provided by two Schottky diodes, which maintain the output at approximately +11dBm—sufficient to directly drive +7 or +10dBm diode-ring mixers. Output-stage clipping is not recommended as a means of gain

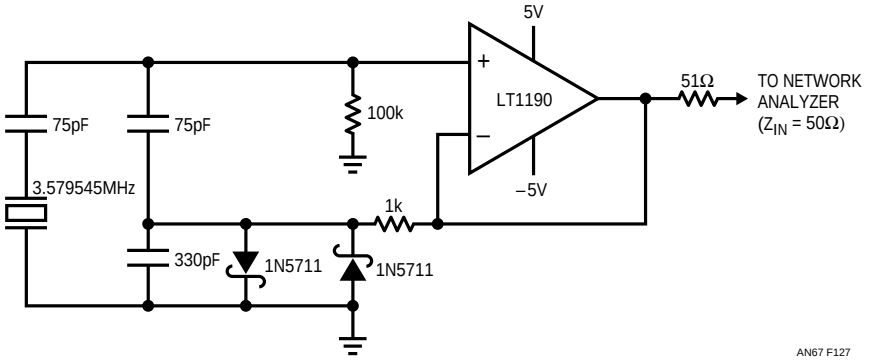


Figure 127. High Frequency Colpitts Oscillator

limiting, as this increases distortion and allows internal nodes to be overdriven. The recovery time would add excessive phase shift in the oscillator loop, degrading frequency stability.

Distortion performance is good, considering that the oscillator consists of one stage and can deliver useful output power. Figure 128 shows a spectral plot of the oscillator's output. The second harmonic is approximately 37dB down, limited primarily by the clipping action of the Schottky diodes. Power supply rejection is excellent, showing a frequency sensitivity of approximately 0.1ppm/V. The LT1190 gives acceptable performance to 10MHz, while the LT1191 extends the circuit's operating range to 20MHz.

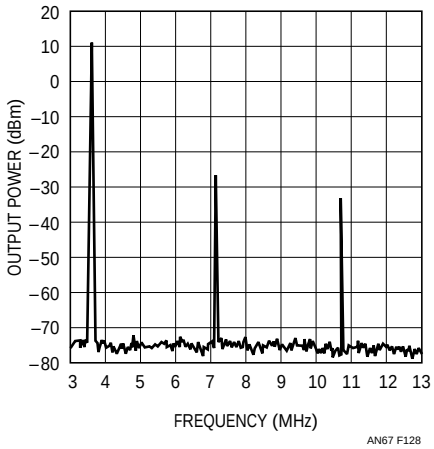


Figure 128. Oscillator Output Spectrum

AN LT1112 DUAL OUTPUT BUFFERED REFERENCE

by George Erdi

A dual output buffered reference application is shown in Figure 129.

Figure 129 works on two AA batteries, which can be discharged to ±1.3V. With two equal 20k resistors, two equal but opposite sign reference voltages are available. Changing the ratio of the two 0.1% resistors allows for other values: one positive and one negative.

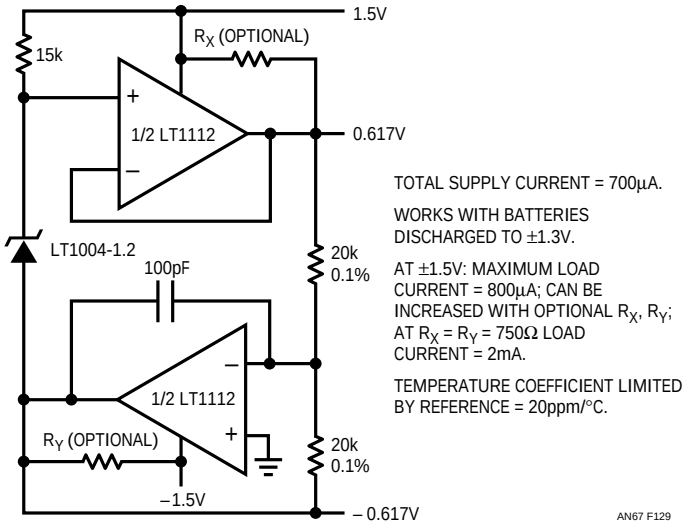


Figure 129. Dual Output Reference Operates on Two AA Cells

THREE OP AMP INSTRUMENTATION AMP USING THE LT1112/LT1114

by George Erdi

The LT1112/LT1114 are dual and quad universal precision op amps. All important precision specifications have been maintained:

1. Microvolt offset voltage; the low cost grades (including the small outline, 8-pin surface mount package) are guaranteed to 75µV.
2. Drift guaranteed to 0.5µV/°C (0.75µV/°C low cost grades)
3. Bias and offset currents are in the picoampere range, even at 125°C
4. Low noise: 0.32µV peak-to-peak, 0.1Hz to 10Hz
5. Supply current is 400µA max per amplifier
6. Voltage gain is in excess of one million

The LT1112/LT1114 also provide a full set of matching specifications, facilitating their use in such matching dependent applications as the three op amp instrumentation amplifier shown in Figure 130. The performance of this instrumentation amplifier depends only on the matching parameters not the specifications of the individual amplifiers.

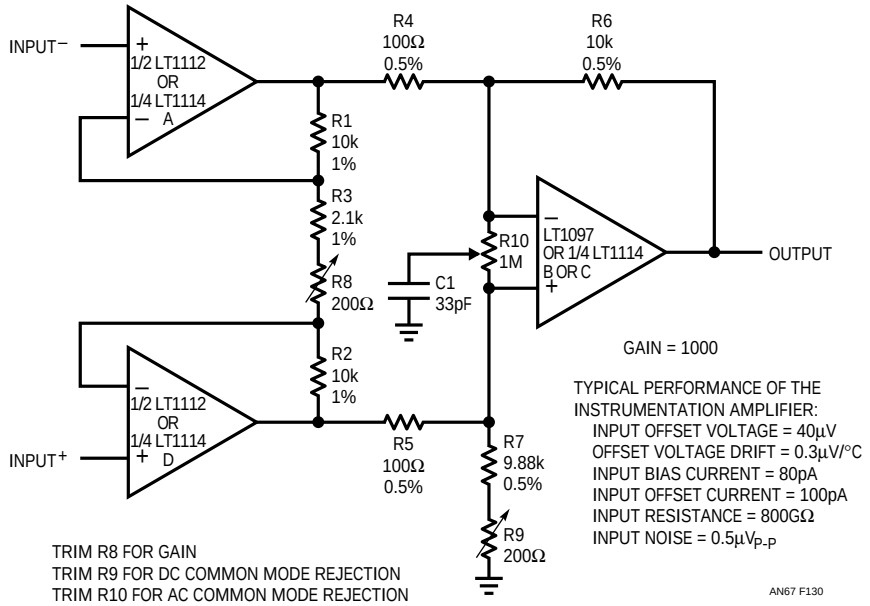


Figure 130. Three Op Amp Instrumetation Amp with Gain = 100

ULTRALOW NOISE, THREE OP AMP INSTRUMENTATION AMPLIFIER

by George Erdi and Alexander Strong

Op amp instrumentation amplifiers usually have op amps with a fixed gain greater than one at the input stage (Figure 131). At low frequencies, decompensated op amps work well, but at high frequencies and with one input grounded, the virtual ground begins to lose its integrity. As the frequency of the input signal increases, the amplitude at the virtual ground increases, making the virtual ground look inductive, eventually requiring a unity-gain stable amplifier. The LT1028 can be made stable under these conditions with bypass capacitors and a little experimenting, but the LT1128 is unconditionally stable.

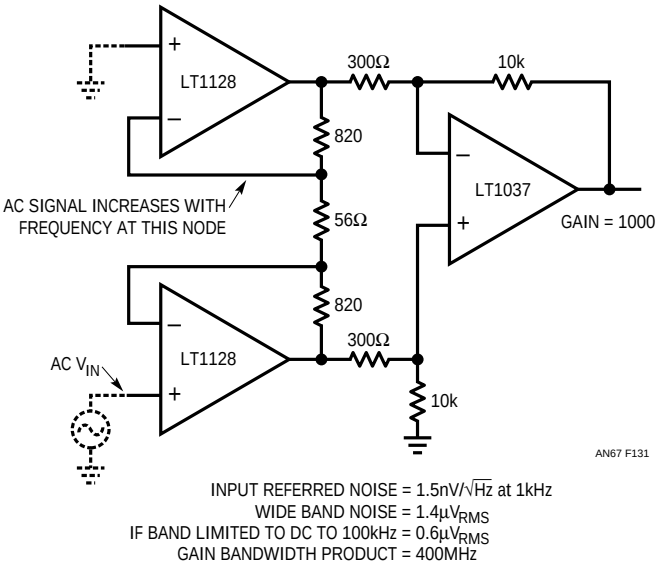


Figure 131. Three Op Amp, Ultralow Noise Instrumentation Amplifier

A TEMPERATURE COMPENSATED, VOLTAGE-CONTROLLED GAIN AMPLIFIER USING THE LT1228

by Frank Cox

It is often convenient to control the gain of a video or intermediate frequency (IF) circuit with a voltage. The LT1228, along with a suitable voltage-to-current converter circuit, forms a versatile gain control building block ideal for many of these applications. In addition to gain control over video bandwidths this circuit can add a differential input and has sufficient output drive for 50Ω systems.

The transconductance of the LT1228 is inversely proportional to absolute temperature at a rate of –0.33%/°C. For circuits using closed-loop gain control (i.e., IF or video automatic gain control) this temperature coefficient does not present a problem. However, open-loop gain control circuits that require accurate gains may require some compensation. The circuit described here uses a simple thermistor network in the voltage-to-current converter to achieve this compensation. Table 1 summarizes the circuit's performance.

Table 1. Characteristics of Example

Input Signal Range	0.5V to 3.0V pk
Desired Output Voltage	1.0V pk
Frequency Range	0Hz to 5MHz
Operating Temperature Range	0°C to 50°C
Supply Voltages	±15V
Output Load	150Ω (75Ω + 75Ω)
Control Voltage vs Gain Relationship	0V to 5V Min to Max Gain
Gain Variation Over Temperature	±3% from Gain at 25°C

Figure 132 shows the complete schematic of the gain control amplifier. Please note that these component choices are not the only ones that will work nor are they necessarily the best. This circuit is intended to demonstrate one approach out of many for this very versatile part and, as always, the designer's engineering judgment must be fully engaged. Selection of the values for the input attenuator, gain-set resistor and current feedback amplifier resistors is relatively straightforward, although some iteration is usually necessary. For the best bandwidth, remember to keep the gain-set resistor, R1, as small as possible and the set current as large as possible (with due regard for gain

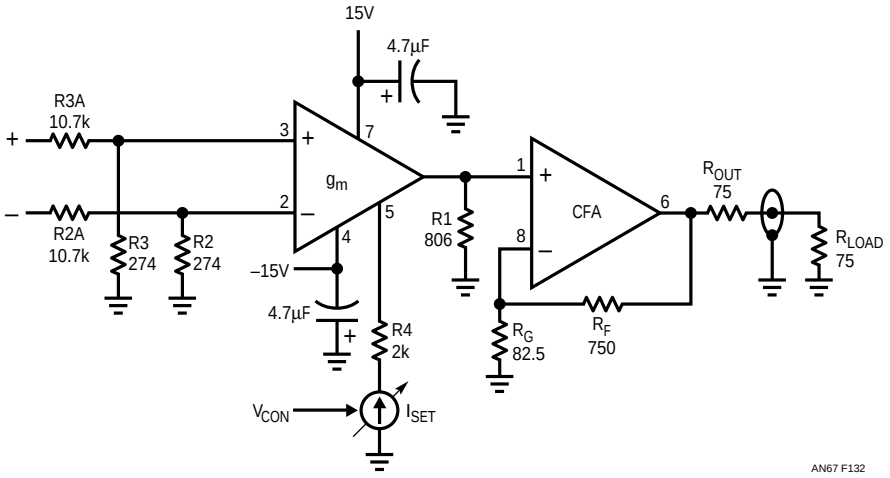


Figure 132. Differential Input, Variable Gain Amplifier

compression). The voltage-controlled current source (I_{SET}) is detailed in the boxed section.

Several of these circuits have been built and tested using various gain options and different thermistor values. Test results for one of these circuits are shown in Figure 133. The gain error versus temperature for this circuit is well within the limit of ±3%. Compensation over a much wider range of temperatures or to tighter tolerances is possible, but would generally require more sophisticated methods, such as multiple thermistor networks.

The VCCS is a standard circuit with the exception of the current set resistor R5, which is made to have a temperature coefficient of –0.33%/°C. R6 sets the overall gain and is made adjustable to trim out the initial tolerance in the LT1228 gain characteristic. A resistor (R_P) in parallel with the thermistor will tend, over a relatively small range, to linearize the change in resistance of the combination with temperature. R_S trims the temperature coefficient of the network to the desired value.

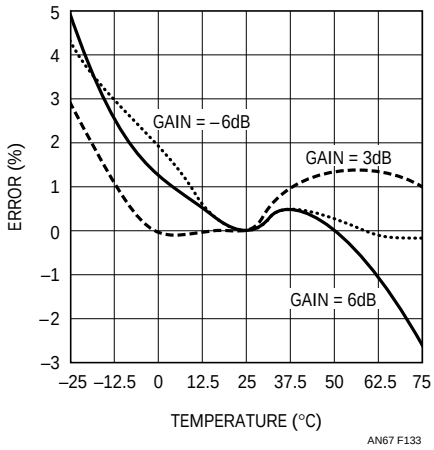


Figure 133. Gain Error for the Circuit in Figure 132 Plus the Temperature Compensation Circuit Shown in Figure 134 (Normalized to Gain at 25°C)

Voltage Controlled Current Source (VCCS) with a Compensating Temperature Coefficient

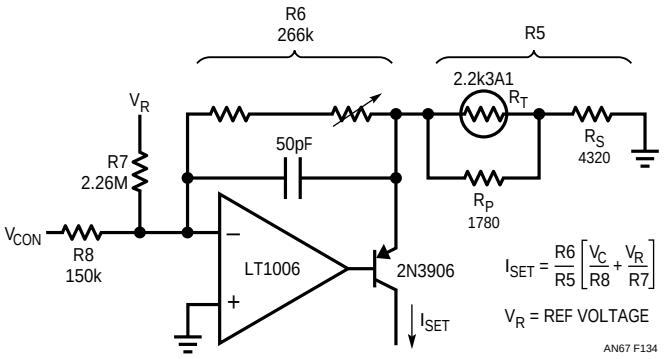


Figure 134. Voltage Controlled Current Source (VCCS) with a Compensating Temperature Coefficient

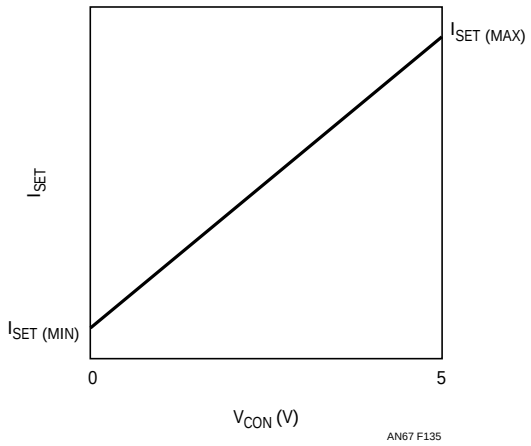


Figure 135. Voltage Control of I_{SET} with Temperature Compensation

VCCS Design Steps

1. Measure or obtain from the data sheet the thermistor resistance at three equally spaced temperatures (in this case 0°C, 25°C and 50°C). Find R_P from:

$$RP = \frac{(R0 \bullet R25 + R25 \bullet R50 - 2 \bullet R0 \bullet R50)}{(R0 + R50 - 2 \bullet R25)}$$

where: R0 = thermistor resistance at 0°C
R25 = thermistor resistance at 25°C
R50 = thermistor resistance at 50°C

2. Resistor R_P is placed in parallel with the thermistor. This network has a temperature dependence that is approximately linear over the range given (0°C to 50°C).

3. The parallel combination of the thermistor and R_P ($R_P||R_T$) has a temperature coefficient of resistance (TC) given by:

$$TC\ R_P||R_T = \left(\frac{R0||R_P - R50||R_P}{R25||R_P}\right)\left(\frac{100}{T_{HIGH} - T_{LOW}}\right)$$

where: T_{HIGH} = the high temperature
T_{LOW} = the low temperature
R_T = the thermistor

4. The desired temp. co. to compensate the LT1228 gain temperature dependence is –0.33%/°C. A series resistance (R_S) is added to the parallel network to trim its TC to the proper value. R_S is given by:

$$\left(\frac{TC\ R_P||R_T}{-0.33}\right)(R_P||R25) - (R_P||R_T)$$

5. R6 contributes to the resultant temperature and so is made large with respect to R5.

6. The other resistors are calculated to give the desired range of I_{SET}.

This procedure was performed using a variety of thermistors (one possible source is BetaTHERM Corporation—phone 508-842-0516). Figure 5 shows typical results reported as errors normalized to a resistance with a –0.33%/°C temperature coefficient. As a practical matter, the thermistor need only have about a 10% tolerance for this gain accuracy. The sensitivity of the gain accuracy to the thermistor tolerance is decreased by the linearization network, in the same ratio as is the temperature coefficient; the room temperature gain may be trimmed with R6. Of course, particular applications require analysis of aging stability, interchangeability, package style, cost, and the contributions of the tolerances of the other components in the circuit.

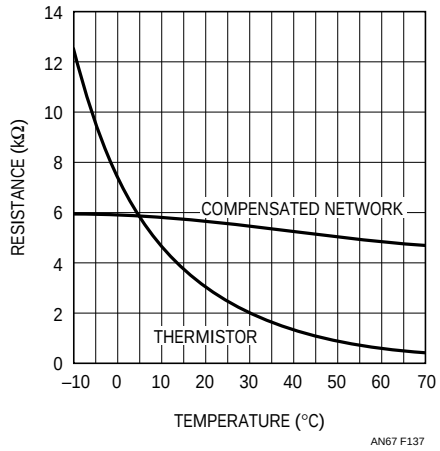


Figure 136. Thermistor and Thermistor Network Resistance vs Temperature

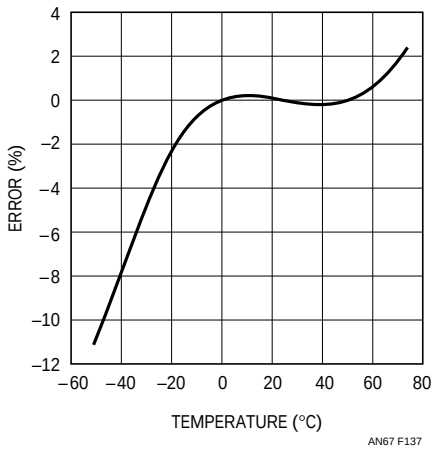


Figure 137. Thermistor Network Resistance Normalized to a Resistor with Exact –0.33%/°C Temperature Coefficient

THE LTC1100, LT1101 AND LT1102: A TRIO OF EFFECTIVE INSTRUMENTATION AMPLIFIERS

by George Erdi

Next to the universally used op amp, perhaps the most useful linear IC building block is the instrumentation amp, or "IA." Using IAs effectively can in some ways be more challenging than selecting op amps, because IAs have different specs and can also use different topologies. However, the basic task is a fixed gain, differential input, single-ended output amplifier, the definition of an IA. The differential signal typically rides on top of a common mode signal; the differential input is amplified and the common mode voltage is rejected by the IA.

The instrumentation amplifier can be implemented with dedicated IA designs, or with one to three op amps to realize the gain function, and a minimum of four ratio-matched precision resistors configured as two like ratio pairs.

The most familiar IA type is the single op amp variety, usually called a difference amplifier and shown in Figure 138. Using just two parts (one op amp and one resistor network), this IA is the height of simplicity and utility. For modest requirements it is built with just a general purpose op amp and four precision resistors. A drawback to this type of IA is that the resistor bridge loads the source. The three op amp configuration uses seven resistors and has high input impedance. It is obviously more difficult to implement than the single op amp version. A nice compromise between these two approaches is illustrated in Figure 139. This IA design uses two op amps to buffer the signal inputs and requires only four resistors. The use of two op

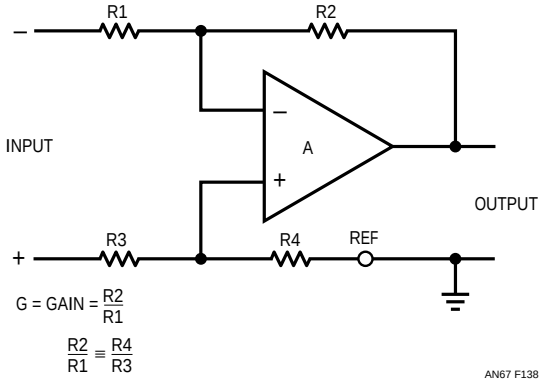


Figure 138. Basic Single Op Amp Instrumentation Amplifier

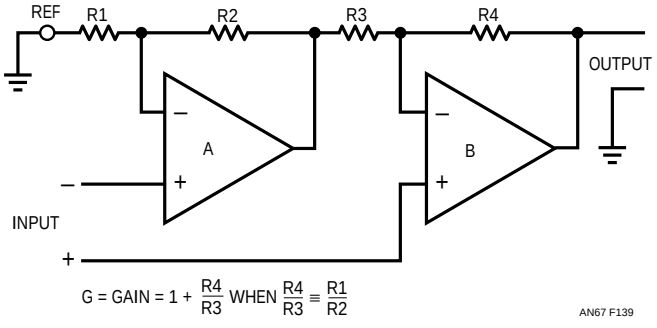


Figure 139. Buffered Dual Op Amp Instrumentation Amplifier

amps with modern dual devices causes no penalty, and in fact this arrangement has real virtues over the more basic setup of Figure 138.

This IA architecture presents minimum loading to the differential source, namely the bias current of the op amp used, which is balanced between the two inputs. The resistor network needs very precise trimming for high common mode rejection (CMRR) and gain accuracy. The trimming is noninteractive; first the R4/R3 ratio is trimmed for gain accuracy then the R1/R2 ratio is trimmed for high CMRR. Trimming compensates not only for resistor inaccuracies, but also for the finite gain and CMRR of the op amps. The amplified difference appears between the output terminal and the voltage applied to the REF terminal (normally grounded).

As a basic building block, this IA can be performance optimized for various applications by a choice of op amps. LTC has taken this step with the LTC1100, LT1101 and LT1102, an instrumentation amplifier series offered in an 8-pin footprint with connections as shown in Figure 140. As illustrated, the gain of these IAs is user programmed by taps on the resistor array, for pre-trimmed precision gains of either 10 or 100 for the LT1101 and LT1102. The 8-pin LTC1100 has a fixed gain of 100, but makes the summing points available for user connections. The key specifications of these three devices are summarized in Table 1.

Table 1. LTC Instrumentation Amplifier Specifications[1]

	LTC1100C	LT1101C/I/M	LT1102C/I/M
Available Gains	100[2]	10/100	10/100
Gain Error (%)	0.01	0.01	0.01
Gain Nonlinearity (ppm)	3	3	7
Gain Drift (ppm/°C)	2	2	10
V_{OS} (µV)	1	60	200
V_{OS} Drift (µV/°C)	0.005	0.5	3
I_B (pA)	2.5	6000	4
I_{OS} (pA)	10	150	4
e_n	1.9µV_{P-P} (DC to 10Hz)	0.9µV_{P-P} (0.1Hz to 10Hz)	20nV/(Hz)$^{1/2}$ (at 1kHz)
CMRR (dB)	110	112	98
PSRR (dB)	130	114	102
V_S (Total, Mode)	4V to 18V (Single/Dual)	1.8V to 44V (Single/Dual)	10V to 44V (Dual)
I_S (mA)	2.4	0.09	3.4
Gain Bandwidth (MHz)	2	0.37	35
SR (V/µs)	4	0.1	30

[1]Unless otherwise stated all specifications are typical at T_A = 25°C. V_S = ±15V for LT1101/LT1102 and ±5V for LTC1100.
[2]A gain option of 10/100 is available in LTC1100CS (16-Lead SW)

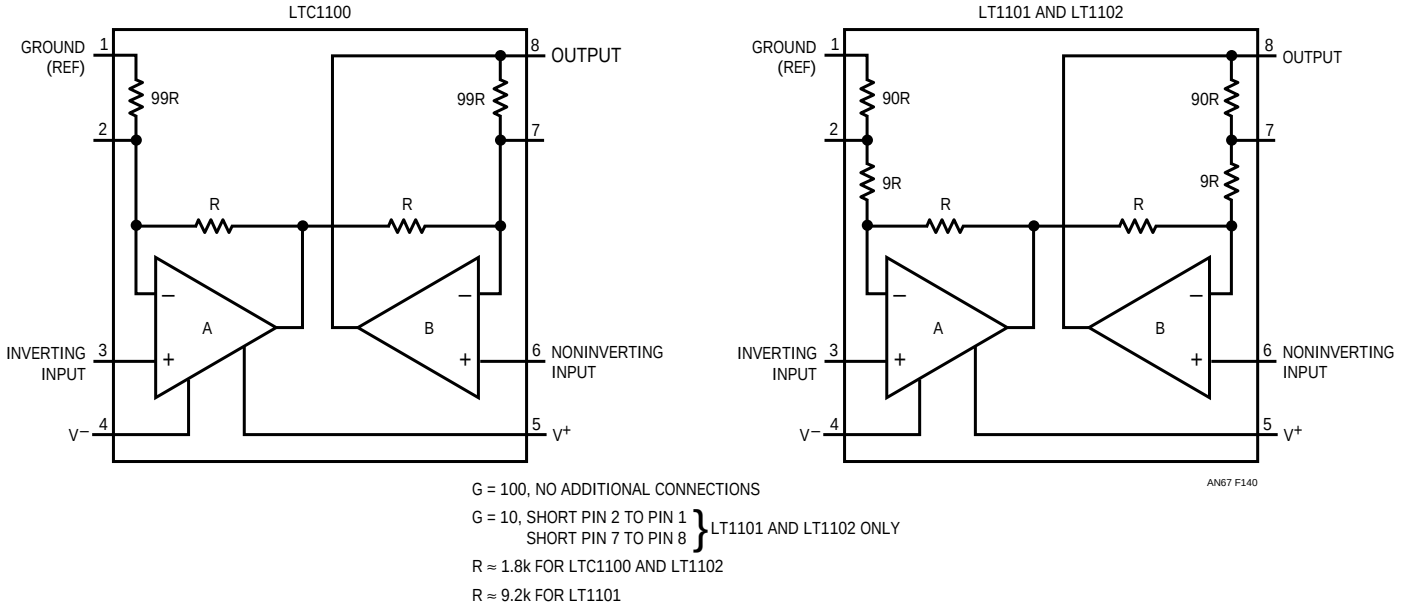


Figure 140. Instrumentation Amplifiers in 8-Pin Packages

It is apparent from Table 1 that for these three IAs, there are no output contributions to input errors. With dedicated IA's or with the three op amp configuration there are separate specifications for input and output offset voltage, input and output drift and noise, and input and output power supply rejection ratio. To calculate system errors these input and output terms must be combined. With the LTC1100/01/02 these error calculations are simple.

With these three IA choices, the user can optimize performance for a variety of factors. The LTC1100 operates with dual or single supplies ranging from 4V to 18V, whereas the LTC1101 accepts a supply range of from 1.8V to 40V. In addition, the LT1101 consumes only 100µA standby current. For applications that require very low offset voltage and drift, the LTC1100 excels with 1µV of offset and 5nV/°C drift. Where both high speed and low bias current are important, the LT1102 is the IA of choice, albeit at a cost of slightly higher power consumption and dual supplies. As can be seen from the table, all of these devices are outstanding with regard to gain accuracy, linearity and stability. The LTC1100, which is based on a dual chopper amplifier prototype (the LTC1051), is by far the best in terms of offset and drift. Either the LTC1100 or the LT1102 could be the unit of choice in terms of lowest bias current, with the LT1102 gaining an edge at higher temperatures.

Applications Considerations

While this IA type is generally outstanding in terms of performance and simplicity, independent of the op amps, some caveats apply to using it most effectively. One concern is AC CMRR. As noted in Figure 140, the first op amp (A) is configured for unity gain, and the second op amp (B) provides all of the voltage gain. This has the effect of making the respective CMRR's frequency mismatched, since the CMRR of the higher gain, "B" side, corners at a much lower frequency. The resulting differential CMRR will therefore degrade more quickly with frequency than that of a topology with better AC balance. On the LT1102 this problem is resolved by decompensating amplifier B to gain-of-ten stability. This increases slew rate and bandwidth and also matches the CMRR rolloff with the frequencies of the two op amps when G = 10. At a gain of 100, this rolloff match no longer holds. However, connecting an 18pF capacitor between Pins 1 and 2 matches the CMRRs

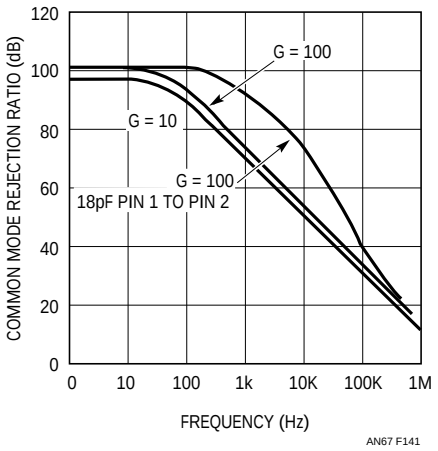


Figure 141. LT1102 Common Mode Rejection Ratio vs Frequency

of the two sides and improves CMRR by an order of magnitude in the 300Hz to 30kHz range (Figure 141). As shown on the LTC1100 and LTC1101 data sheets, similar improvements can be obtained from those devices by connecting external capacitors.

The LTC1100 and LT1101 also present some important usage considerations because of their single supply abilities, i.e., when operating with the V^- terminal tied to ground. In this configuration, these devices handle CM inputs near ground and voltage swings to ground and their reference terminals can be tied to ground. One of the most common uses of these two IAs is as bridge amplifiers in conjunction with single supply powered DC strain gauges. As such, these IAs have a unique ability to deliver high gain with precision, while operating with a 1/2 supply voltage CM input. At first glance, it appears that a dual supply IA could operate, for example, on a 9V battery supply with 4.5V common mode input, but its output will not swing to ground and its reference terminal cannot be tied to ground.

For SPICE simulation purposes, a model for the LT1101 is included in the LTC macromodel library. The model is configured as the resistor network shown for the LT1101, combined with a model for the LT1078. A similar model for the LTC1100 can be made by scaling the four resistors appropriately, and using an LTC1051 model from the same library. A close model approximation for the LT1102 can be made with the LT1102 resistor values, combined with an LT1057 model for the "A" side, and a LT1022 model for the "B" side (both also in the library).

Miscellaneous Circuits

DRIVING A HIGH LEVEL DIODE RING MIXER WITH AN OPERATIONAL AMPLIFIER

by Mitchell Lee

One of the most popular RF building blocks is the diode ring mixer. Consisting of a diode ring and two coupling transformers, this simple device is a favorite with RF designers anywhere a quick multiplication is required, as in frequency conversion, frequency synthesis or phase detection. In many applications these mixers are driven from an oscillator. Rarely does anyone try building an oscillator capable of delivering 7dBm for a "minimum geometry" mixer, let alone one of higher level. One or more stages of amplification are added to achieve the drive level required by the mixer. The new LT1206 high speed amplifier makes it possible to amplify an oscillator to 27dBm in one stage.

Figure 143 shows the complete circuit diagram for a crystal oscillator, LT1206 op amp/buffer and diode-ring mixer. Most of the components are used in the oscillator itself, which is of the Colpitts class. Borrowing from a technique used in Hewlett Packard's Unit Oscillator, the current of the crystal is amplified rather than the voltage. There are several advantages to this method, the most important of which is low distortion. Although the voltages present in this circuit have poor wave shape and are sensitive to loading, the crystal current represents essentially a filtered version of the voltage waveform and is relatively tolerant of loading effects.

The impedance, and therefore the voltage at the bottom of the crystal, is kept low by injecting the current into the summing node of an LT1206 current feedback amplifier. Loop gain reduces the input impedance to well under 1Ω. Oscillator bias is adjustable, allowing control of the mixer drive. This also provides a convenient point for closing an output power servo loop.

Operating from ±15V supplies, the LT1206 can deliver 32dBm to a 50Ω load, and with a little extra headroom (the absolute maximum supply voltage is ±18V), it can reach 2W output power into 50Ω. Peak guaranteed output current is 250mA.

Shown in Figures 144 to 148 are spectral plots for various combinations of single and double termination at power levels ranging from +17dBm to +27dBm — not bad for an inductorless circuit. Double termination may be used to present a 50Ω source impedance to the mixer, or to isolate two or more mixers driven simultaneously from one LT1206 amplifier.

Although a 10MHz example has been presented here, the LT1206's 65MHz bandwidth makes it useful in circuits up to 30MHz. In addition, the shutdown feature can be used to interrupt drive to the mixer. When the LT1206 is shut

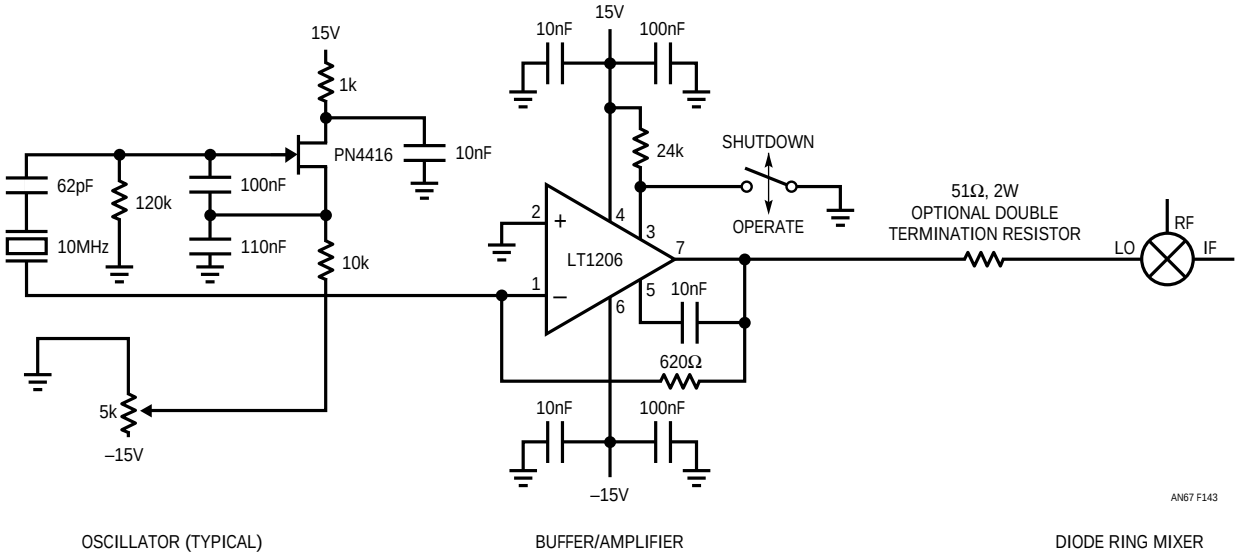


Figure 143. Oscillator Buffer Drives +17dBm to +27dBm Double Balanced Mixers

down, the oscillator will likely stop, since the crystal then sees a series impedance of 620Ω and the mixer itself. Upon re-enabling the LT1206 there will be some time delay before the oscillator returns to full power. The circuit works equally well with an LC version of the oscillator.

Note that the current feedback topology is inherently tolerant of stray capacitive effects at the summing node, making it ideal for this application. Another nice feature is the LT1206's ability to drive heavy capacitive loads while remaining stable and free of spurious oscillations.

For mixers below +17dBm, the LT1227 is a lower cost alternative, featuring 140MHz bandwidth in combination with the shutdown feature of the LT1206.

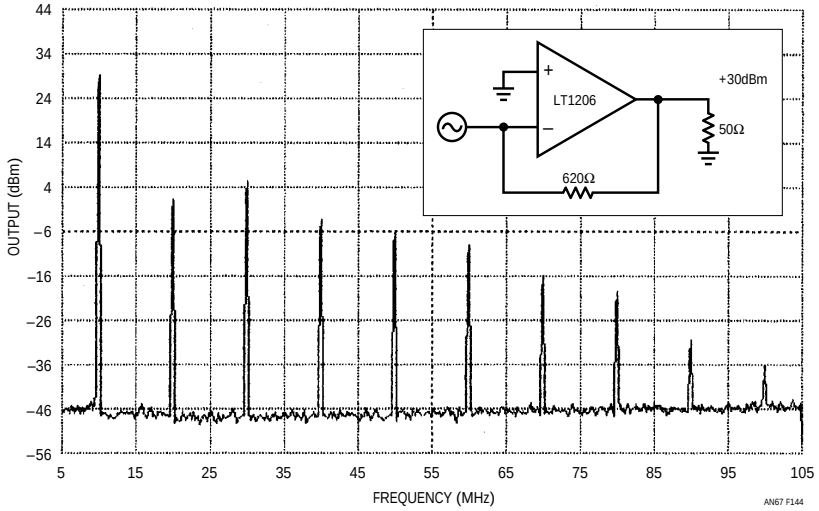


Figure 144. Spectrum Plot of Figure 143's Circuit Driving +30dBm into a 50Ω Load (Single Termination)

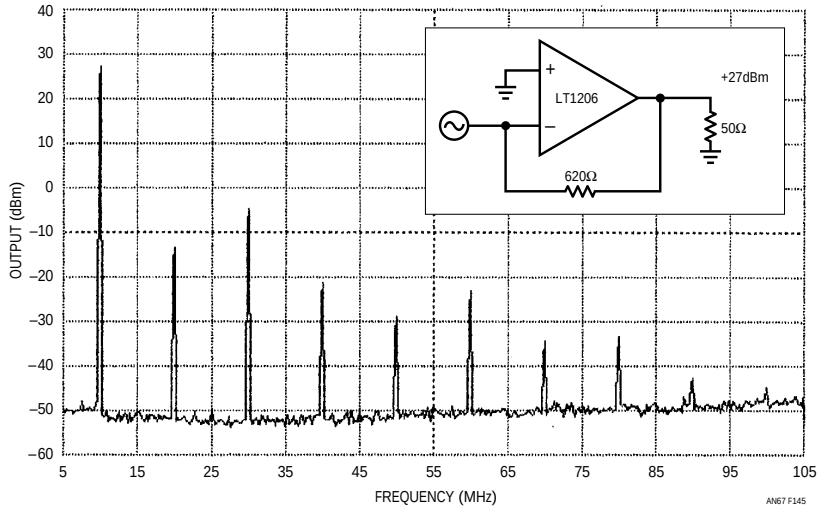


Figure 145. Spectrum Plot of Figure 143's Circuit Driving +27dBm into a 50Ω Load

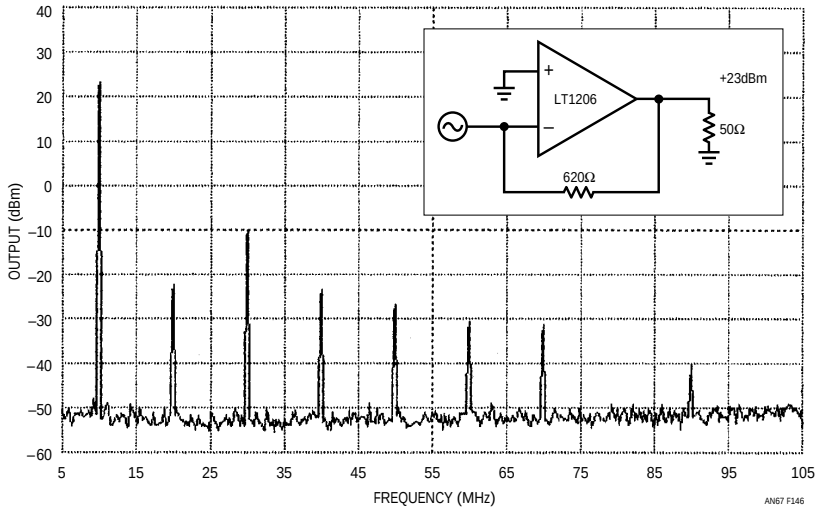


Figure 146. Spectrum Plot of Figure 143's Circuit Driving +23dBm into a 50Ω Load

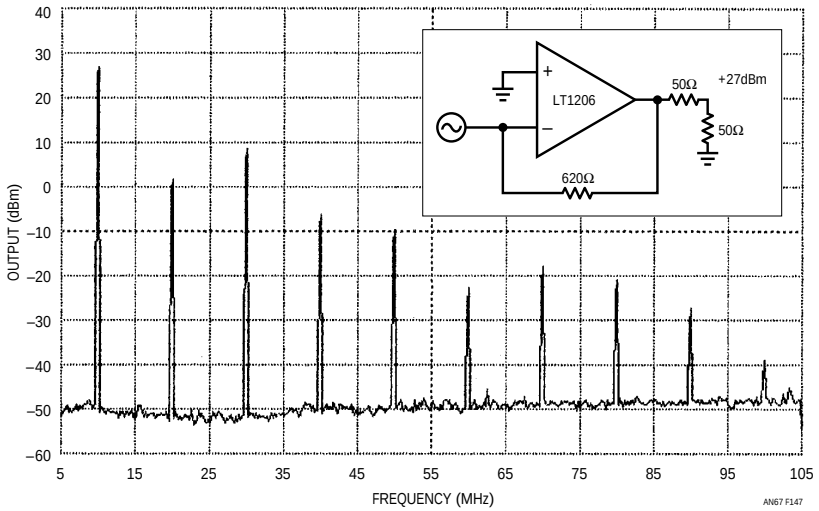


Figure 147. Spectrum Plot of Figure 143's Circuit Driving +27dBm into a 50Ω, Double Terminated Load

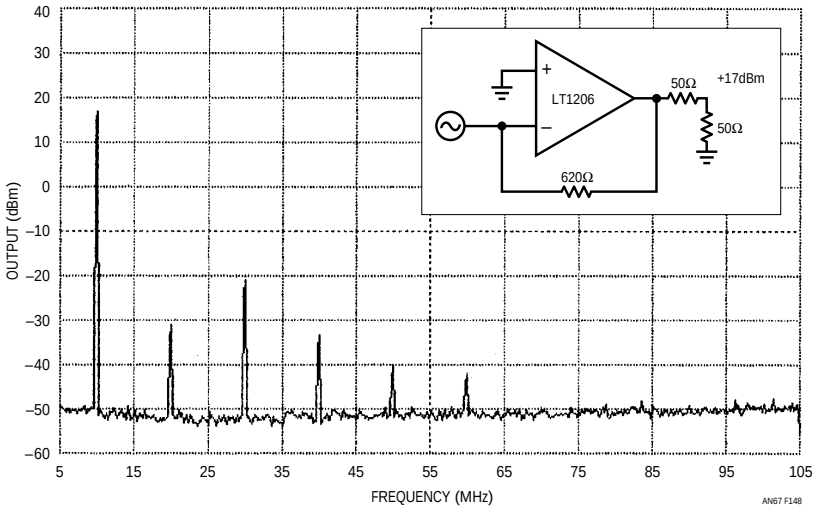


Figure 148. Spectrum Plot of Figure 143's Circuit Driving +17dBm into a 50Ω, Double Terminated Load

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