Understanding and Applying Voltage References

By Mitchell Lee

Specifying the right reference and applying it correctly is a more difficult task than one might first surmise, considering that references are only 2- or 3-terminal devices. Although the word “accuracy” is most often spoken in reference to references, it is dangerous to use this word too freely because it can mean different things to different people. Even more perplexing is the fact that a reference classified as a dog in one application is a panacea in another. This application note will familiarize the reader with the various aspects of reference “accuracy” and present some tips on extracting maximum performance from any reference.

As with other specialized electronic fields, the field of monolithic references has its own vocabulary. We’ve already learned the first word in our reference vocabulary, “accuracy.” This is the yardstick with which references are graded and compared. Unfortunately, there are at least five or six good units for gauging accuracy. To keep you from reaching a full understanding of the topic, industry pundits use a special technique called “unit-hopping” to confuse and confound everyone from newcomer to seasoned veteran. You mention an accuracy figure and the pundit quickly hops to a new unit so that you cannot follow his line of reasoning. Figure 1 neutralizes the pundits’ callous intentions and allows its possessor to unit-hop with equal ease and full comprehension. Refer to Figure 1 as you read this application note.

Today’s IC reference technology is divided along two lines: bandgap references, which balance the temperature coefficient of a forward-biased diode junction against that of a ΔV_{BE} (see Appendix B); and buried Zeners (see Appendix A), which use subsurface breakdown to achieve outstanding long-term stability and low noise. With few exceptions, both reference types use additional on-chip circuitry to further minimize temperature drift and trim output voltage to an exact value. Bandgap references are generally used in systems of up to 12 bits; buried Zeners take over from there in higher accuracy systems.

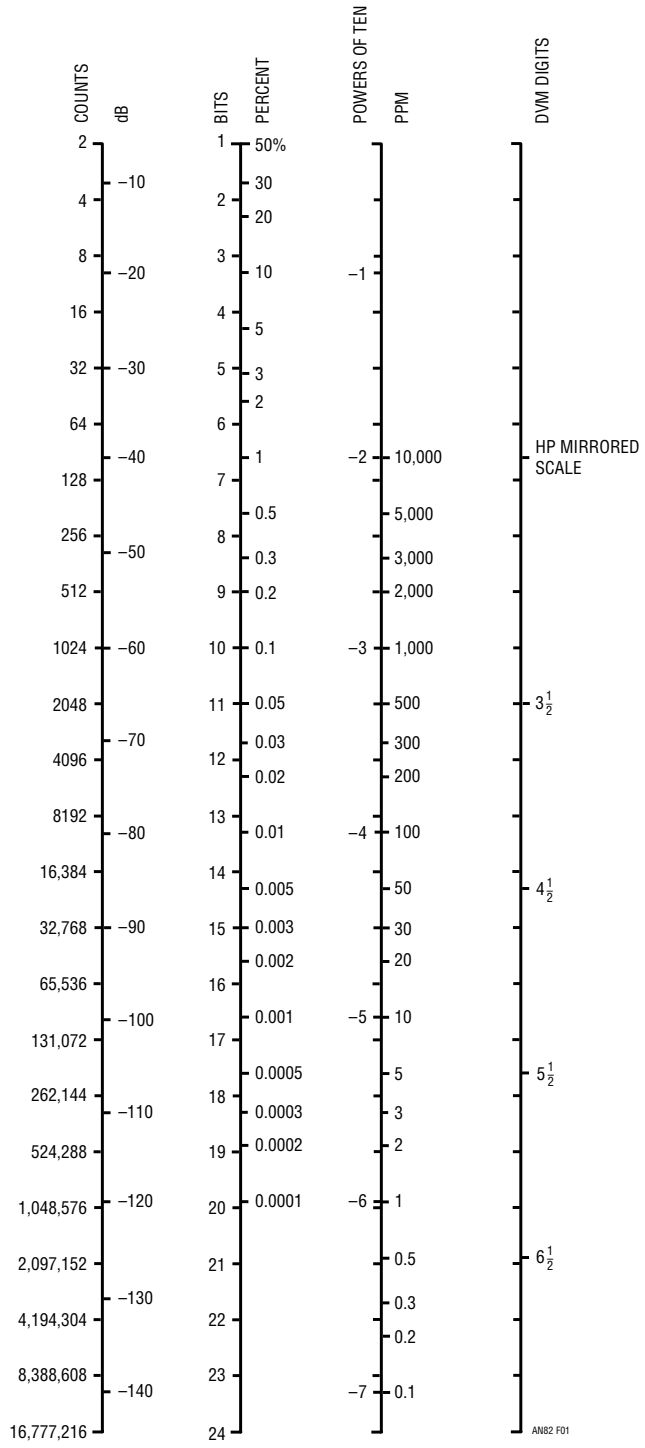

Figure 1. Accuracy Translator

In circuits and systems, monolithic references face competition from discrete Zener diodes and 3-terminal voltage regulators only where accuracy is not a concern. 5% Zeners and 3% voltage regulators are commonplace; these represent 4- or 5-bit accuracy. At the other end of the spectrum—laboratory standards—the performance of the best monolithic references is exceeded only by saturated Weston cells and Josephson arrays, leaving monolithic references in command of every conceivable circuit and system application.

Reference accuracy comprises multiple electrical specifications. These are summarized in Table 1. Most commonly specified by circuit designers is *initial accuracy*. This is a measure of the output voltage error expressed in percent or in volts. Initial accuracy is specified at room temperature (25°C), with a fixed input voltage and zero load current, or for shunt references, a fixed bias current.

Table 1. Reference Accuracy Specifications

PARAMETER	DESCRIPTION	PREFERRED UNIT(S)
Initial Accuracy	Initial Output Voltage at 25°C	V, %
Temperature Coefficient	$\frac{V_{MAX} - V_{IN}}{\text{Total Temperature Range}}$	ppm/°C
Long-Term Stability	Change in Output vs Time Measured Over 1000 Hours or More	$ppm\sqrt{kh}$
Noise	0.1Hz to 10Hz	μV_{P-P}, ppm_{P-P}
	10Hz to 1kHz	μV_{RMS}, ppm_{RMS}

Tight initial accuracy is a concern in systems where calibration is either inconvenient or impossible. More commonly, absolute accuracy is only a secondary concern, as a final trim is performed on the finished product to reconcile the summation of all system inaccuracies. A final trim affects considerable cost savings by eliminating the need for tight initial accuracy in every reference, DAC, ADC, amplifier and transducer in the system.

Monolithic reference initial accuracy ranges from 0.02% to 1%, representing 1LSB error in 6-bit to 12-bit systems. Weston cells and Josephson arrays clock in at 1ppm to 10ppm and 0.02ppm initial accuracy, respectively (0.02ppm is less than 1LSB error in a 25-bit system).

Temperature-induced changes in reference output voltage can quickly overshadow a tight initial accuracy specification. Considerable effort is therefore expended to minimize the *temperature coefficient* (tempco) of a reference. Most references are guaranteed in the range of 2ppm/°C to 40ppm/°C, with a few devices falling outside this range. A properly applied LTZ1000 temperature stabilized reference can demonstrate 0.05ppm/°C.

Tempco is specified as an average over the operating temperature range in units of ppm/°C or mV/°C. This average is calculated in what is called the "box" method. Figure 2 shows how box method tempco figures are defined and calculated. The reference in question (LT®1019 bandgap) is tested over the specified operating temperature range. The minimum and maximum recorded output voltages are applied to the equation shown, resulting in an average temperature coefficient expressed in V/°C. This is further manipulated to find ppm/°C, as used in the data sheet. The tempco is an average over the operating range, rather than an incremental slope measured at any specific point. In the case of the LT1021 and LT1236, the incremental slope at 25°C is also guaranteed.

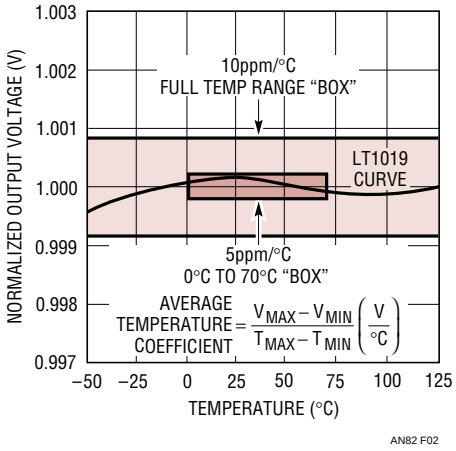

Figure 2. The Box Method Expresses Absolute Output Accuracy Over Temperature as a Drift Term

A data sheet figure for tempco can be used to directly calculate the output voltage tolerance over the entire operating temperature range. A device with a tempco of 10ppm/°C, specified for 0°C to 70°C, could drift up to 700ppm from the initial value (about 3 counts in a 12-bit system). A 0.1% reference with 700ppm tempco error is guaranteed 0.17% accurate over its entire operating temperature range.

Two exceptions to this rule are the LT1004 and LT1034, which simply guarantee absolute output voltage accuracy over the entire operating temperature range. The LT1009 and LT1029 use a combination of the two, called the "bow

tie" or "butterfly" method (see the LT1009 data sheet for a detailed explanation).

Neither the bandgap nor the buried Zener, in their basic form, are inherently low drift. Special on-chip circuitry is used to improve the tempco of the reference core. A buried Zener is first-order compensated against temperature changes by adding a P-N junction diode. The Zener itself measures +2mV/°C and the diode –2mV/°C. The combination of the two in series cancel to about 0.2mV/°C (≈30ppm/°C) out of a total of 7V. Interestingly, this is very close to the tempco of a saturated Weston cell, which measures –40μV/°C, or –39ppm/°C. Weston cells are held in a temperature-controlled bath; monolithic buried Zener references are further compensated against temperature changes by carefully adding fractional V_{BE} and/or ΔV_{BE} terms to the output. Post-manufacturing trims are used on both bandgap and buried Zener products to further minimize tempco of the finished reference.

Another detractor from accuracy is *long-term stability*. The output of a reference changes, usually in one direction, as it ages. The effect is logarithmic; that is, the output changes less and less as time progresses. The units of long-term stability, ppm/$\sqrt{kh}$ (kh = 1000 hours), reflect the logarithmic decline of the output change vs time. Because long-term changes in the output are small and occur over the course of months or years, it is impossible to devise an affordable manufacturing test to guarantee the true stability of all references. Instead, this parameter is characterized by aging dozens of units in a temperature-controlled chamber at 25°C to 30°C for 1000 hours or more. Note that the absolute temperature is unimportant, but it must remain invariant during the course of the test. Mathematically extrapolating long-term stability data from high temperature, accelerated life tests leads to erroneously optimistic room temperature results.

When long-term stability is guaranteed, it is done by means of a 4-week burn-in, during which multiple output voltage measurements are made. Even with this elaborate, costly procedure, the guaranteed limit is about three to four times the typical drift.

Unless the product is designed for frequent calibration or is relatively low performance, long-term stability may be an important aspect of reference performance. Products designed for a long calibration cycle must hold their accuracy for extended periods of time without intervention. These products demand references with good long-term stability. You can expect buried Zeners to perform better than 20ppm/$\sqrt{kh}$, and bandgaps between 20ppm and 50ppm/$\sqrt{kh}$. Some of this drift is attributed to the trim and compensation circuitry wrapped around the reference core. The LTZ1000 dispenses with trim and compensation overhead in favor of an on-chip heater. The remaining Zener/diode core drifts 0.5ppm/$\sqrt{kh}$ in the first year of operation, approaching the stability of a Weston cell.

Most of the long-term stability figures shown in LTC reference data sheets are for devices in metal can packages, where assembly and package stresses are minimized. You can expect somewhat less performance for the same reference in a plastic package.

One last factor that affects accuracy is short-term variation of output voltage, otherwise known as noise. Reference noise is typically characterized over two frequency ranges: 0.1Hz to 10Hz for short-term, peak-to-peak drift, and 10Hz to 1kHz for total "wideband" RMS noise. Noise voltage is usually proportional to output voltage, so the output noise expressed in ppm is constant for all voltage options of any given reference. Wideband noise ranges from 4ppm to 16ppm RMS for bandgap references, to 0.17ppm to 0.5ppm RMS for buried Zeners. Noise improves with increased reference current, regardless of reference type. But since the reference core operating current is set internally, the noise characteristics cannot be changed except by external filtering (the LT1027 features a noise filtering pin). The LT1034 and LTZ1000 buried Zeners are externally accessible, allowing the user to increase the bias current and reduce noise.

Adding output bypassing or external compensation will affect the character of a reference's noise. In particular, if the compensation is "peaky," the spot noise will likely rise to a peak somewhere in the 100Hz to 10kHz range. Critical damping will eliminate this noise peak.

Reference noise can affect the dynamic range of a high resolution system, obscuring small signals. Low frequency noise also complicates the measurement of output voltage. Modern, high accuracy digital voltmeters can average many readings to help filter low frequency noise effects and provide a stable reading of a reference's true output voltage.

ESSENTIAL FEATURES

There are two styles of references: shunt, functionally equivalent to a Zener diode; and series, not unlike a 3-terminal regulator. Bandgaps and buried Zeners are available in both configurations (see Figure 3). Some series references are designed to also operate in shunt mode by simply biasing the output pin and leaving the input pin open circuit. Series-mode references have the advantage that they draw only load and quiescent current from the input supply, whereas shunt references must be biased with a current that exceeds the sum of the maximum quiescent and maximum expected load currents. Since they are biased by a resistor, shunt references can operate on a very wide range of input voltages.

About half of LTC's reference offerings include a pin for external (customer) trimming. Some are designed for precision trimming of the reference output, whereas others have a wide trim range, allowing the output voltage to be adjusted several percent above or below the intended operating point.

If load current steps must be handled, transient response is important. Transient response varies widely from reference to reference and comprises three distinct qualities: turn-on characteristics, small-signal output impedance at high frequency and settling behavior when subjected to a fast, transient load. References exhibit these qualities because almost all contain an amplifier to buffer and/or scale the output.

The LT1009 is optimized for fast start-up characteristics, and it settles in a little over 1µs, as shown in Figure 4. For some references, optimum settling is obtained with an external compensation network. As shown in Figure 5, a 2µF/2Ω damper optimizes the settling and high frequency output impedance of an LT1019 reference. Fastest settling is obtained with an LT1027, which settles to 13 bits accuracy in 2µs. This impressive feat is illustrated by the oscillograph of Figure 6, which clearly shows the output recovering from a 10mA load step.

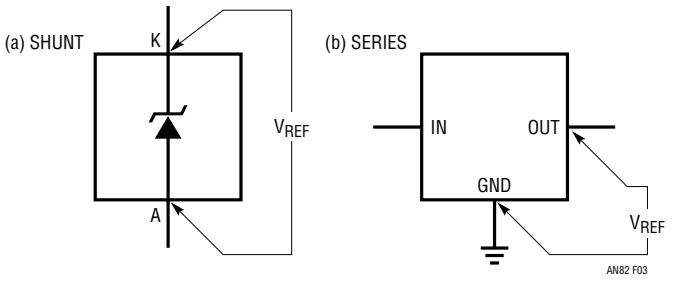

Figure 3. References Are Supplied in Either 2-Terminal Zener Style (a) or 3-Terminal Voltage Regulator Style (b)

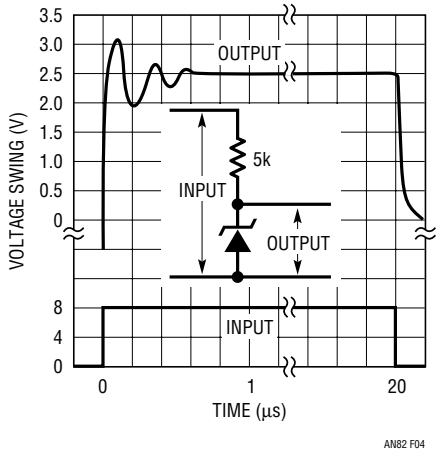

Figure 4. The LT1009 is Optimized for Rapid Settling at Power-Up

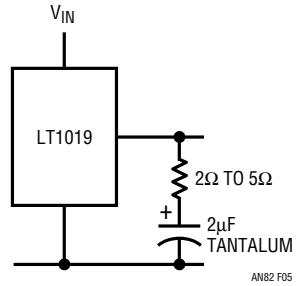

Figure 5. Optimum Settling Realized with RC Compensation at Output

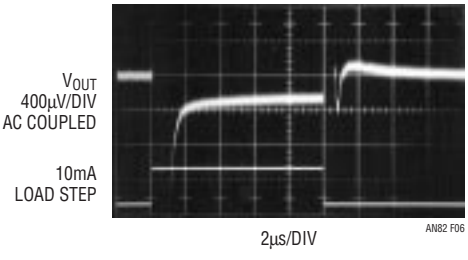

Figure 6. The LT1027 is Optimized for Fast Settling in Response to Load Steps

REFERENCE PITFALLS

References look deceptively simple to use, but like any other precision product, maximum performance is not necessarily easy to achieve. Here are a few common pitfalls reference users face, and ways to beat them.

Current-Hungry Loads

Most references are specified for maximum load currents (or shunt currents) of 10mA to 20mA. Nevertheless, best performance is not obtained by running the reference at maximum current. A number of effects, including thermal gradients across the die and thermocouples formed between the leads and external circuit connections, may limit the short-term stability of the output voltage. Adding an external pass transistor, as shown in Figure 7, removes the load current from the reference. For loads greater than 300µA, the pass transistor carries almost all of the current and eliminates short-term thermal drift. This circuit is also useful for applications requiring more than 20mA, and easily supports up to 100mA, limited only by transistor beta and dissipation.

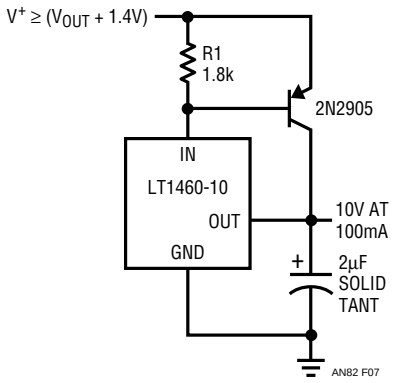

Figure 7. An External Transistor is Useful for Boosting Output Current as Well as for Removing Load Current from the Reference. This Trick Works On All 3-Terminal References

"NC" Pins

If references need only two or three external connections, why are they supplied in 8-pin packages? There are several reasons, but the one we'll cover here is post-package trimming. To guarantee tight output tolerances, some factory trimming is necessary after the device has been packaged. In packaged form we no longer have direct access to the die, so the extra pins on an 8-pin package are used to effect post-package trimming.

For some ICs, "NC" means "this pin is floating, you can hook it up to whatever you want." In the case of a reference, it means "don't connect anything to this pin." That includes ESD and board leakage, as well as intentional connections. External connections will, at best, cause output voltage shifts and, at worst, permanently shift the output voltage out of spec.

A similar caution applies to the TRIM pin on references with adjustable outputs. The TRIM pin is akin to an amplifier's summing node; do not inject current into a TRIM pin-unless you want to trim the output, of course. Here board leakage or capacitive coupling to noise sources are pitfalls to avoid.

Board Leakage

A new specter has entered the field of references: board leakage caused by the residues of water-soluble flux. The effect is not unlike that produced by the sticky juice extravasated from a ruptured electrolytic capacitor. Leakage from ground, supply rails and other circuit potentials into NC, trim and other sensitive pins through conductive flux residues will cause output voltage shifts. Even if the leakage paths do not shift the reference out of spec, external leakage can manifest itself as long-term output voltage drift, as the resistance of the flux residue changes with shifts in relative humidity and the diffusion of external contaminants. Water-soluble flux residues must be removed from the board and package surfaces, or completely avoided. In one case, the author observed an LT1009 shifted out of spec by a gross leakage path of approximately 80kΩ between the trim pin and a nearby power supply trace. The leakage was traced to water-soluble flux.

Figure 8 shows how a good reference can go bad with only a very small leakage. A hypothetical industrial control board contains an LT1027A producing 5V for various data acquisition circuits. A nearby trace carries 24V. Just 147MΩ leakage into the noise filtering pin (NR) causes a typical device to shift +200ppm, and out of spec. Clearly, a 24V circuit trace doesn't belong anywhere near a 0.02% reference. This example is oversimplified but clearly demonstrates the potential for disaster.

A tightly packed circuit board may leave no choice but to agglomerate incompatible traces. In this case, use a guard ring to eliminate reference shift (see Figure 9). The output of the reference is divided down to 4.4V, equal to the potential on the NR pin, and used to bias a guard ring encircling the trace connecting NR to the noise filter capacitor. This reduces the effect of board leakage paths by more than two orders of magnitude, shunting the errant leakage away from the guarded traces.

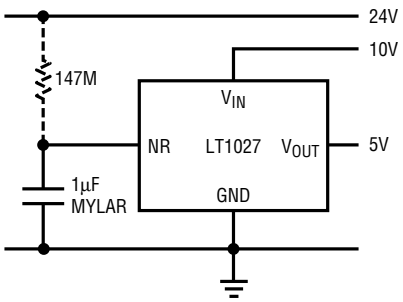

Figure 8. Board Leakage Can Wreak Havoc with a Precision Reference. Here, a 147MΩ Leakage Path to 24V Pushes the 5V Output Out of Spec

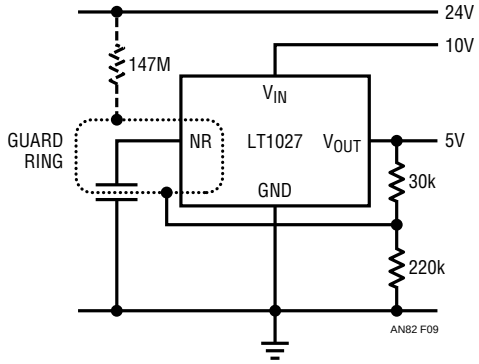

Figure 9. Adding a Guard Ring Protects Against Errant Leakage Paths

Trim-Induced Temperature Drift

About half of LTC's reference offerings include a pin for external (customer) trimming. Trimming may be necessary to calibrate the system, but it can also adversely affect the tempco of the reference. For example, in the LT1019 bandgap reference, external trim resistors won't match the tempco of the internal resistors. The mismatch causes a small (1ppm/°C) worst-case shift in the output voltage tempco, as explained on the data sheet. The LT1021-5 and LT1236-5 standard trim circuit can be modified, as shown in Figure 10, to prevent upsetting the references' inherently low temperature coefficients. Trimming the LT1027 has little effect on the output voltage tempco, and it needs no special consideration. Always check the reference data sheet for specific recommendations.

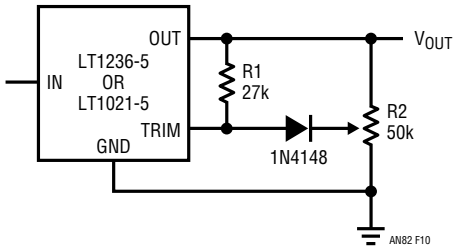

Figure 10. The LT1021 or LT1236 Output Trim is Made Temperature Insensitive by the Addition of a Diode and a Resistor

Burn-In

Most manufacturers of high-accuracy systems run their products through a burn-in procedure. Burn-in solves two problems at once: it relieves stresses built into the reference and circuit board during assembly and it ages the reference beyond the highest long-term drift region, which occurs when power is first applied to the part. A typical burn-in procedure calls for operating the board at 125°C ambient for 168 hours. If the main concern is stress relief, a shorter, unpowered burn-in cycle can be used.

Board Stress

Burn-in can help "relax" a stuffed board, but additional mechanical stress may be introduced when the board is mounted into the product. Stress has a directly measurable effect on reference output. If the stress changes over a period of time, it may manifest itself as unacceptable long-term drift. Circuit boards are not perfectly elastic, so bending forces may cause permanent deformation and a permanent step-change in reference output voltage. Devices in metal (TO-5 and TO-46) packages are largely immune to board stress, owing to the rigidity of the package and the flexibility of the leads. Plastic and surface mount packages are another matter.

Board stress effects are easily observed by monitoring the output of a reference while applying a bending force to the

board. A controlled experiment was performed to measure the effect of board stress on an LT1460CS8-2.5 surface mount reference. Devices were mounted in the center of 7" × 9" rectangular boards, as shown in Figure 11. The boards were then deflected out-of-plane 18 mils per inch, as shown in steps 1 through 4. Figure 12 shows the net effect on the output of one representative sample measured over eight cycles of flexure.

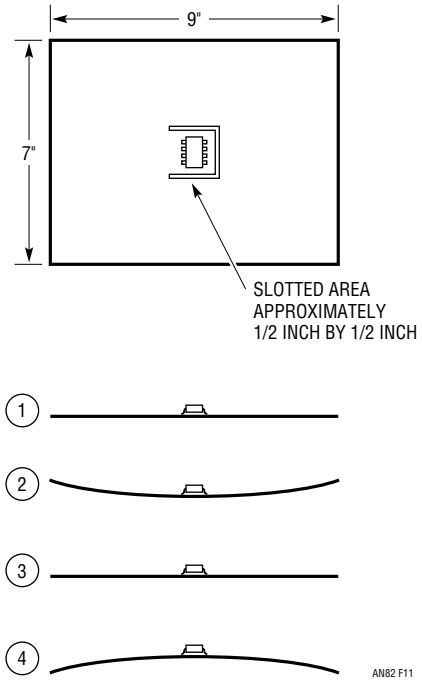

Figure 11. Reference Sensitivity to Stress Was Evaluated by Assembling Devices On a 7" × 9" Circuit Board and Flexing, as Shown in Steps 1 Through 4

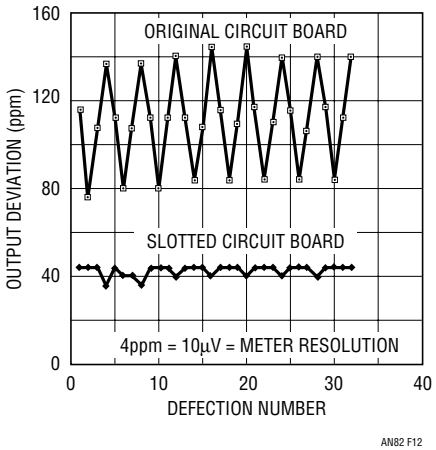

Figure 12. Isolating Stress by Slotting the Circuit Board Reduces Reference Variations by More Than an Order of Magnitude (LTC1460S8-2.5)

The original board showed about 60ppm peak-to-peak shift. The board was then slotted on a vertical mill, forming a 0.5" × 0.5" tab with the reference located in its center (also illustrated in Figure 11). The test continued with the slotted configuration, and the output voltage variations were reduced to ±1 count (10µV) on the meter, or approximately 4ppm peak-to-peak. This represents a tenfold improvement in stress-induced output voltage shift.

Several other techniques can be employed to minimize this effect, without resorting to a milled board. Anything that can be done to restrict the board from bending is helpful. A small, thick board is better than a large, thin board. Stiffeners help immunize the board against flexure. Mount the circuit board with grommets, flexible standoffs or card-cage style so that minimal force is applied to the mounting holes and board.

Part placement and orientation are just as important. If a board is squeezed from opposite edges, the bending force tends to concentrate in a line down the center. Locate the reference away from the middle of the board. Since the longer side of a board is more flexible than the shorter, locate the reference along the shorter edge. These recommendations are generalities; the placement, mounting method and orientation of other components and assemblies on the circuit board will influence the mechanical strengths and weaknesses of the circuit board.

Bench tests indicate that the strongest axis for plastic packages is along the shorter dimension of the body of the plastic. Figure 13 shows the correct orientation for surface mount parts. Note that the part's longest axis is placed perpendicular to that of the circuit board. The devices in Figure 13 are shown in the center of the board for illustrative purposes only; comments about placement still apply.

In spite of all precautions, extraneous effects may adversely affect the reference's resistance to board stress. Watch out for adhesives and solder and flux debris under the package. These will create pressure points and induce unpredictable stresses in the package. If a board has been subjected to a high bending force, some of the glass fibers and layers may break or shear apart, permanently weakening the board. Subsequent bending forces will concentrate their stress at points thus weakened.

Figure 14 shows various schemes for routing stress-relief slots on a circuit board, along with optimum package

orientation. Note that the longest axis of the reference is aligned with the tab, not the shortest axis of the circuit board. This is in anticipation of flexing forces transmitted into the tab. The best orientation for the tab is in line with the longest axis of the board as in (b), (c) and (d). Bending forces along the weaker (longer) axis of the board could be coupled into (a) and (e). Note that the ICs are aligned to resist this force. Use configuration (c) when the part is located along the longer edge of the board, and (d) when it is located along the shorter edge. Use (b) when the part is not located along any edge.

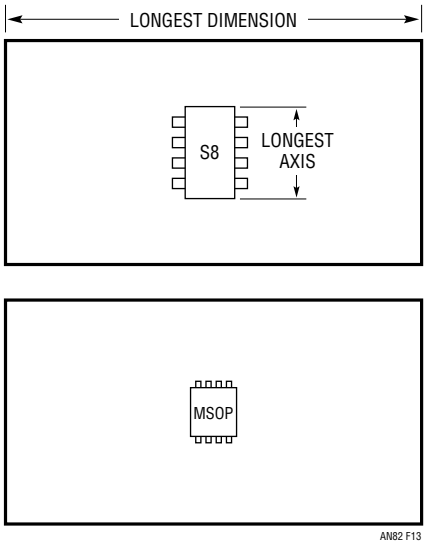

Figure 13. Arranging the Longest Axes of the Board and Package in Perpendicularity Minimizes Stress-Induced Output Changes

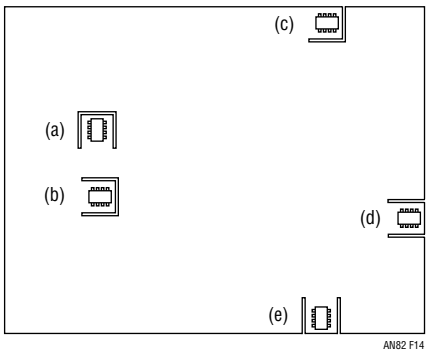

Figure 14. Slotting the Area Around the Reference Can Help Isolate it from Board Stress if Properly Applied (See Text)

Temperature-Induced Noise

Even though references operate on very meager supply currents, dissipation in the reference is enough to cause small temperature gradients in the package leads. Variations in thermal resistance, caused by uneven air flow, lead to differential lead temperatures, thereby causing thermoelectric voltage noise at the output of the reference. Figure 15 dramatically demonstrates this effect. The first half of the plot was made with an LT1021H-7 buried Zener reference, which was shielded from ambient air with a small foam cup (Dart Container Corporation Stock No. 8J8 or similar). The cup was removed at six minutes elapsed time for the second half of the test. Ambient in both cases was a lab bench-top with no excessive turbulence from air conditioners, opening/closing doors, foot traffic or 547 exhaust. Removing the foam cup increased the output noise by almost an order of magnitude in the 0.01Hz to 10Hz band.

The Kovar leads of the TO-5 working against copper circuit traces are the primary culprit. Copper lead frames used on DIP and surface mount packages are not nearly as sensitive to air turbulence because they are intrinsically matched. Still, external components create thermocouples of their own with potentials of 10µV/°C or more per junction. In a LT1021-7 reference, this represents more than 1ppm/°C shift from each thermoelectric generator. Temperature gradients across the circuit board and dissipation within external components can lead to the same kind of noise as shown in Figure 15.

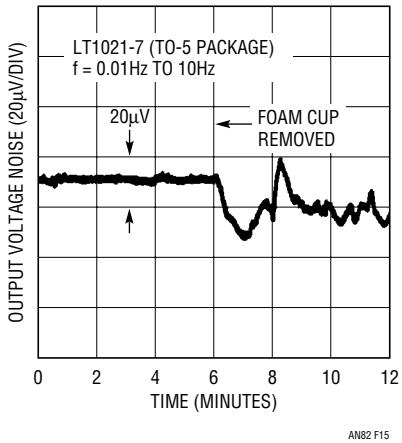

Figure 15. Air Turbulence Induces Low Frequency Noise and Compromises Reference Accuracy

Temperature gradients may arise from heat generators on the board. Position the reference and its associated external components far from heat sources and, if necessary, use routing techniques to create an isothermal island around the reference circuitry. Minimize air movement either by adding a small enclosure around the reference circuitry, or by encapsulating the reference circuitry in self-expanding polyurethane foam.

REFERENCE APPLICATIONS

The unique pocket reference shown in Figure 16 is a good match for a pair of AAA alkaline cells, because the circuit draws less than 16μA supply current. Two outputs are provided: a buffered, 1.5V voltage output, and a regulated 1μA current source. The current source compliance ranges from approximately 1V to –43V.

The reference is self-biased, completely eliminating line regulation as a concern. Start-up is guaranteed by the LT1495 op amp, whose output saturates at 11mV from the negative rail. Once powered, there is no reason to turn the circuit off. One AAA alkaline contains 1200mAH capacity, enough to power the circuit throughout the 5-year shelf life of the battery. Voltage output accuracy is about 0.17% and current output accuracy is about 1.2%. Trim R1 to calibrate the voltage (1kΩ per 0.1%), and R3 to calibrate the output current (250Ω per 0.1%).

Low noise synthesizers need quiet power supplies for their VCOs and other critical circuitry. 3-terminal regulators exhibit far too much noise for this application, calling instead for a regulator constructed from a reference. A practical example is shown in Figure 17. Current through the LT1021-5 reference is used to drive the base of a PNP pass device, resulting in an available output current of at least 1A. In this example, the current is intentionally limited to 200mA by the addition of emitter degeneration and base clamping. The low noise of the reference is preserved, giving a 100-fold improvement over the noise of an equivalent 5V, 3-terminal regulator, not to mention improved initial accuracy and long-term stability. Typical output noise is 7μV_{P-P} over a 10kHz bandwidth.

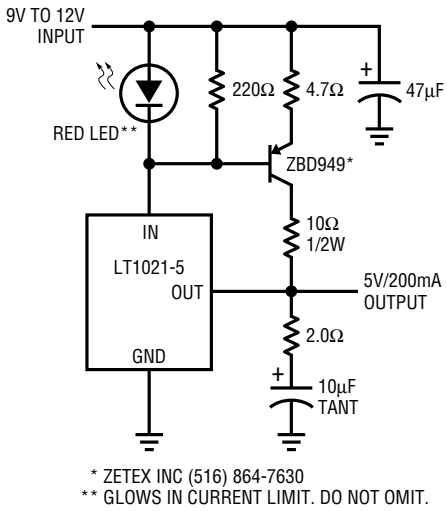

Figure 17. Ultralow Noise 5V, 200mA Supply Output Noise is 7μV_{RMS} Over a 10Hz to 10kHz Bandwidth. Reference Noise is Guaranteed to be Less Than 11μV_{RMS}. Standard 3-Terminal Regulators Have One Hundred Times the Noise and No Guarantees

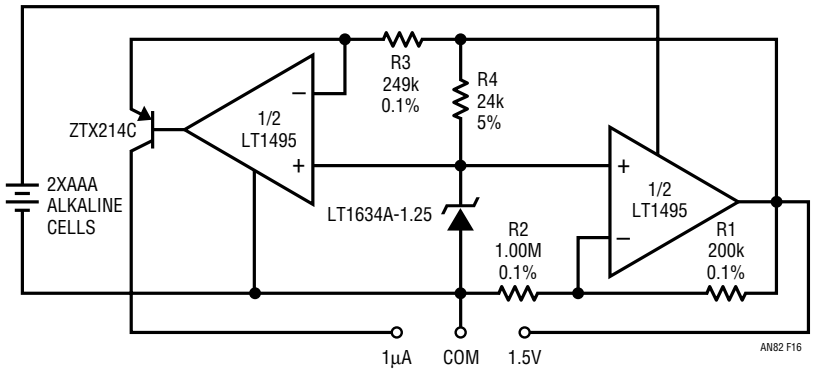

Figure 16. This Pocket Reference Operates for Five Years on One Set of AAA Cells

CONCLUSION

When specifying a reference, keep in mind that initial accuracy, temperature coefficient and long-term stability all play a role in overall accuracy of the finished product. By taking some care in applying the reference, and by avoiding some key pitfalls, the reference's inherent accuracy can be preserved.

FOR FURTHER READING

Spreadbury, Peter J. "The Ultra-Zener–A Portable Replacement for the Weston Cell?" by *IEEE Transactions on Instrumentation and Measurement*, Vol. 40, No. 2, April 1991, pp. 343-346

Huffman, Brian. Application Note 42: *Voltage Reference Circuit Collection*. Linear Technology Corporation, June 1991.

Lee, Albert. "4.5μA Li-Ion Battery Protection Circuit" *Linear Technology*, Volume 9, Number 2, June 1999, p.36.

APPENDIX A

BURIED ZENER: LOW LONGTERM DRIFT AND NOISE

The Zener diode has long been used in reference service in many noncritical applications. Integrated circuit designers sometimes use an NPN emitter-base junction operating in reverse breakdown as a Zener reference. Breakdown occurs at the surface of the die, where the effects of contamination and oxide charge are most pronounced. These junctions are noisy and suffer from unpredictable short- and long-term drift.

The buried Zener, developed as a precision IC reference, places the junction below the surface of the silicon, well away from contamination and oxide effects. The result is a Zener with excellent long-term stability, low noise, and relatively accurate initial tolerance.

Figure A–1 shows the first steps in fabricating a buried Zener. A region of n^+ buried layer is located beneath the Zener structure so as to shield subsequent diffusions from contact with the substrate. After growth of the n^- epitaxial layer, p^+ isolation is diffused through a small opening at the center of the Zener. At the same time, isolation is diffused around the periphery to form a separate tub containing the entire Zener structure.

Isolation diffuses both downward and laterally. The central diffusion is shielded from contact with the substrate by the buried layer, while the isolation walls are allowed to reach substrate and form an isolated tub. It is important to note that the highest concentration of p^+ occurs directly under the mask opening and that the dopant concentration is weakest at the fringes of a diffusion.

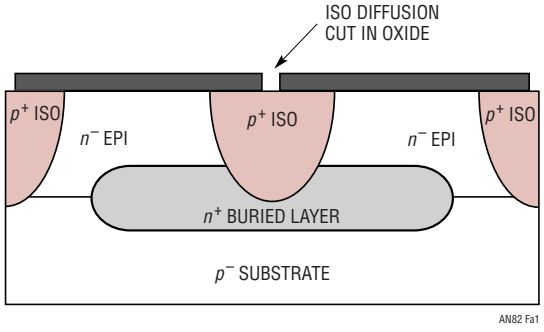

Figure A–1. Iso is Diffused to Form the Anode. Highest Dopant Concentration Occurs Directly Under the Mask Opening

The last steps include a p^- base diffusion and an emitter diffusion, located at the center of the Zener (see Figure A–2). The emitter becomes the cathode, whereas the combined isolation and base diffusion serve as the anode.

Breakdown occurs at the bottom of the of the cathode, where the emitter and isolation + base dopant concentrations are richest. Lighter doping concentrations result in a higher breakdown voltage at the iso-buried layer, base-epi and iso-epi junctions, and at the outer fringes of the emitter diffusion, ensuring that these areas are not active when the buried junction is biased into breakdown. The result is an extremely stable subsurface breakdown mechanism that has near-theoretical noise and is unaffected by surface contamination or oxide effects

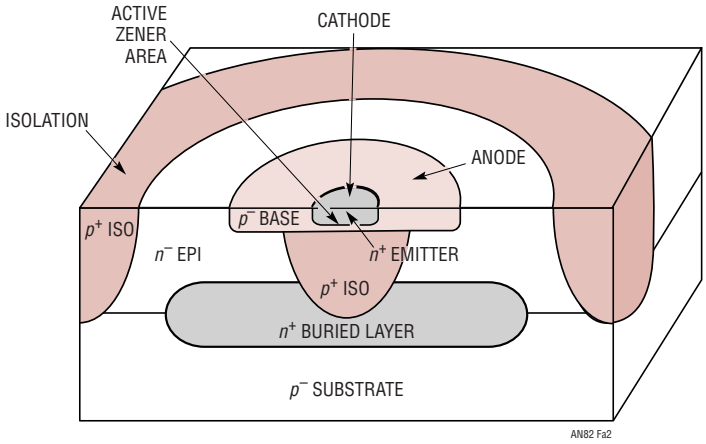

Figure A–2. An Emitter Diffusion Forms the Cathode. Breakdown Occurs Under the Center of the Emitter, Where Both Emitter and Iso + Base Dopant Concentrations are Highest

APPENDIX B

ΔV_{BE}: INTEGRATED CIRCUIT WORKHORSE

It is, perhaps, a cruel fate for IC designers that no single IC device or structure is invariant with changes in temperature. Various combinations of devices have been devised to stabilize circuits against changes in temperature. As explained in the text, Zener-based references use a Zener and a forward-biased diode connected in series to achieve near-zero temperature coefficient and a bandgap relies on a ΔV_{BE} in series with a forward-biased diode.

An indispensable technique in integrated circuit design, the ΔV_{BE} is not widely known in other fields. Before explaining the theory of ΔV_{BE}, let's skip ahead to the two most important results: two identical diode (or base emitter) junctions running different currents produce different voltage drops. The ratio of the currents controls the absolute value of the offset voltage. Further, this offset has a predictable, positive temperature coefficient of approximately 3.4μV/°C for each room-temperature millivolt of offset. By combining the positive TC of a ΔV_{BE} with the negative TC of a diode drop, a zero TC bandgap reference is formed. As we shall soon see, it takes a ΔV_{BE} offset of 650mV to cancel the –2.18mV/°C TC of a hypothetical diode.*

Two transistors (or diodes) produce an offset given by the following equation:

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = (kT/q)\ \ln(J_{E1}/J_{E2}) \quad (1)$$

where ΔV_{BE} = offset voltage, k = Boltzmann's constant ($1.381 \bullet 10^{-23}$ Joules/K), T = absolute temperature (298K at room), q = charge of an electron ($1.6 \bullet 10^{-19}$ Coulombs), and J_E = emitter current density. The actual units of area used to calculate J_{E1} and J_{E2} cancel each other, so that only the area ratio is important. Similarly, only the current ratio is important. If we restrict ourselves to using two identical transistors, Equation (1) reduces to

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = (kT/q)\ \ln(I_{C1}/I_{C2}) \quad (2)$$

where I_C = collector current (see Figure B–1). The temperature coefficient is given by

$$TC = d\Delta V_{BE}/dT = (k/q)\ \ln(I_{C1}/I_{C2}) \quad (3)$$

where k/q = 86.3μV/°C.

Calculating the current ratio required to produce +2.18mV/°C (corresponding to 650mV offset) we find that it is unmanageably large, about $9.44 \bullet 10^{10}$:1. In practice, a much smaller offset is generated by a ΔV_{BE} cell and then amplified to 650mV. As an example, see Figure B–2. Using a 10:1 current ratio,** we find a room temperature offset from Equation (2) of 59.2mV, and a temperature coefficient of 199μV/°C. Applying a gain of slightly less than eleven brings us to 650mV and +2.18mV/°C.

Adding a PNP emitter follower to the output of this circuit forms a crude "bandgap" reference, with an output voltage equal to the sum of 650mV and the PNP's V_{BE}. Assuming V_{BE} = 600mV, the output would be 1.25V. The reference could be further improved by trimming the gain of eleven so that the ΔV_{BE} exactly canceled the PNP's base-emitter temperature coefficient. IC bandgap references are constructed in a similar way.

*The numbers have been massaged for those who want to reproduce the calculations.

**or a combination of current and area scaling to achieve a 10:1 current density ratio in Equation (1).

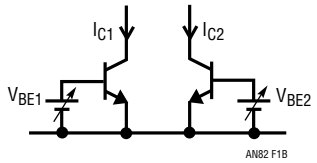

Figure B–1. The Current Ratio Required to Produce a Certain V_{BE} Offset is Defined by Equations (1) and (2)

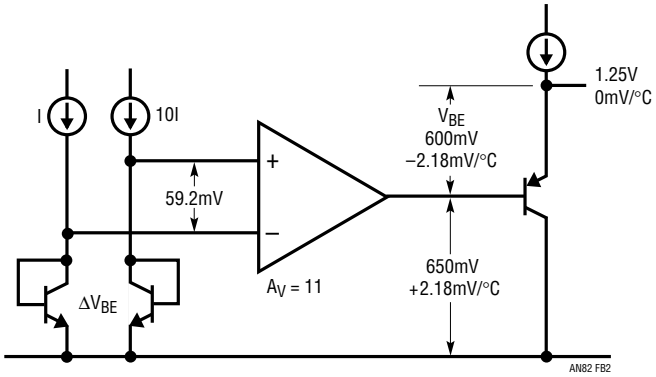

Figure B–2. A Bandgap Reference is Formed by Stacking a ΔV_{BE} Generator and a V_{BE}

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