40nV$_{P-P}$ Noise, 0.05µV/°C Drift, Chopped FET Amplifier

by Jim Williams

Figure 1's circuit combines the 5V rail-to-rail performance of the LTC6241 with a pair of extremely low noise JFETs configured in a chopper based carrier modulation scheme to achieve extraordinarily low noise and DC drift. This circuit's performance suits the demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

The LTC1799's output is divided down to form a 2-phase 925Hz square wave clock. This frequency, harmonically unrelated to 60Hz, provides excellent immunity to harmonic beating or mixing effects which could cause instabilities. S1 and S2 receive complementary drive, causing the A1-based stage to see a chopped version of the input voltage. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to DC output amplifier A2. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. Because the input stage is AC coupled, its DC errors do not affect overall circuit characteristics, resulting in the extremely low offset and drift noted.

Figure 2, noise measured over a 50 second interval, shows 40nV in a 0.1Hz to 10Hz bandwidth. This low noise is attributed to the input JFET's die size and current density.

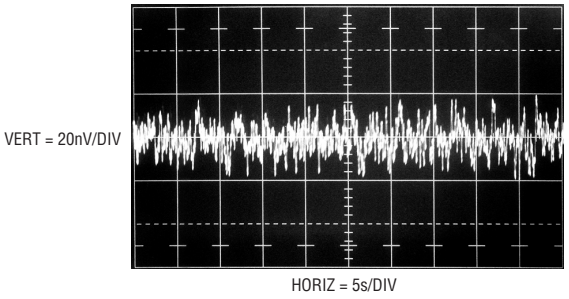

Figure 2. Noise measures 40nV$_{P-P}$ in 50s sample period

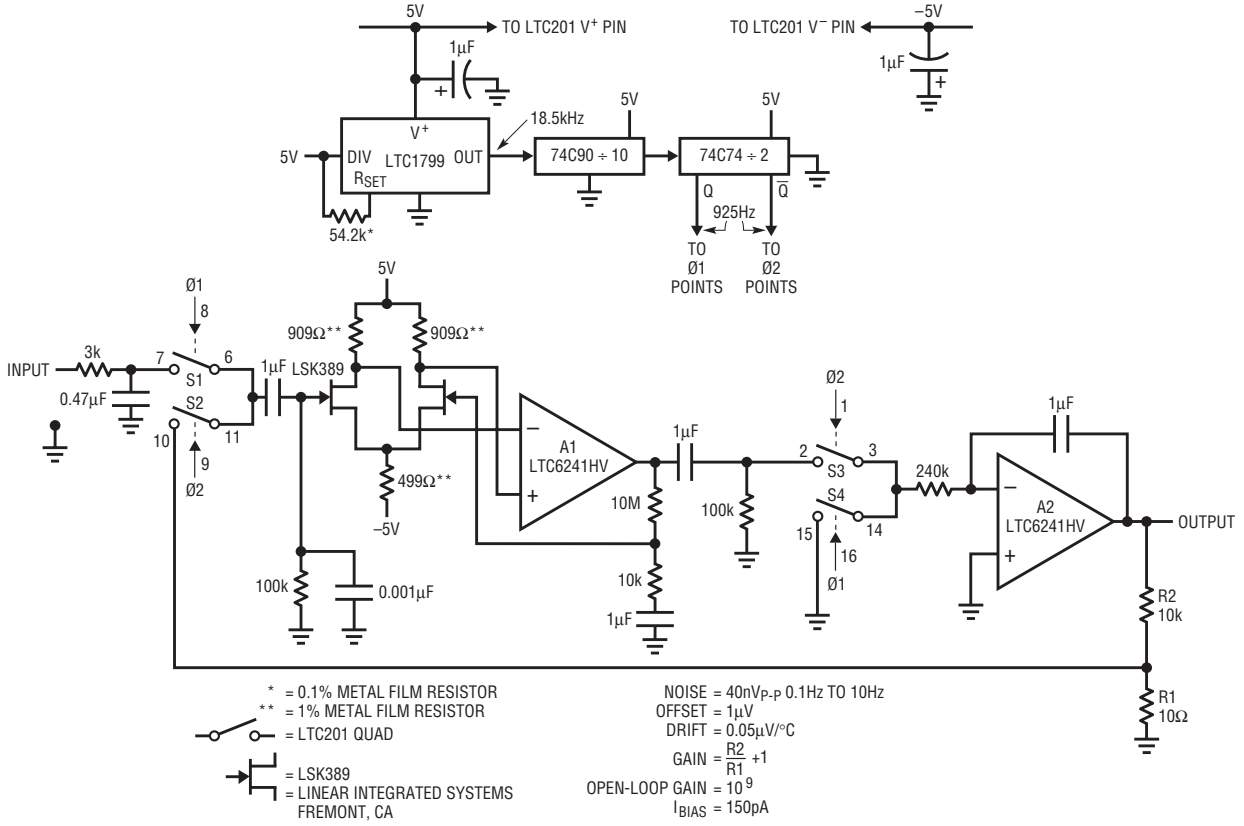

Figure 1. 40nV noise chopper amplifier