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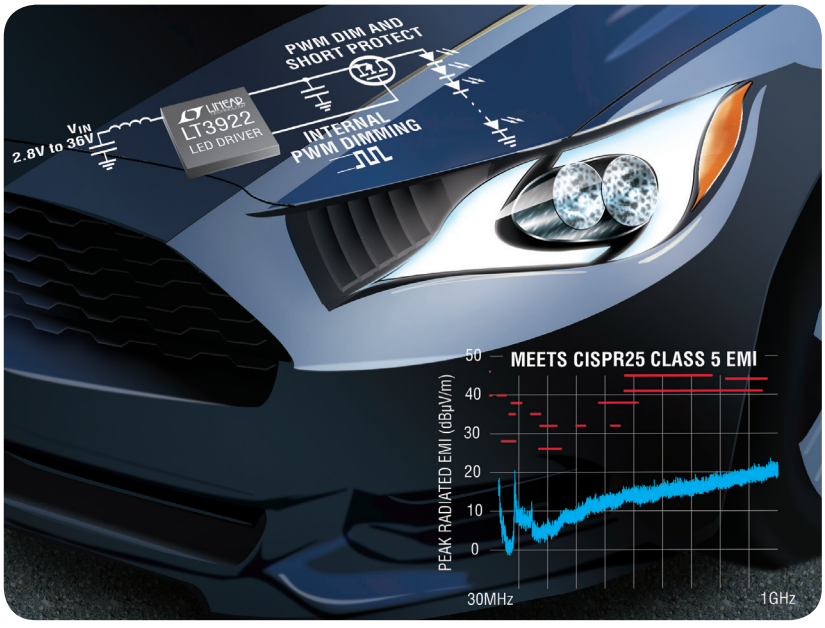
IN THIS ISSUE

Synchronous, Low EMI LED Driver Features Integrated Switches and Internal PWM Dimming

Keith Szolusha and Kyle Lawrence

The breadth of LED applications has grown to encompass everything from general lighting to automotive, industrial and test equipment, sign boards and safety equipment. As a result, the breadth of design requirements for LED drivers has expanded. The latest LED solutions require drivers that are compact, efficient, low noise, and feature high dimming ratios and advanced fault protection. The LT3922 easily meets these demands.



The LT3922 36V, synchronous LED driver with integrated 2A switches can be configured as a boost, buck or boost-buck LED driver.

THE LT3922 WITH INTEGRATED SWITCHES AND INTERNAL PWM DIMMING

The LT®3922 36V, synchronous LED driver with integrated 2A switches can be configured as a boost, buck or boost-buck LED driver. Its high efficiency synchronous and integrated power switches fit into a tiny 4mm × 5mm QFN package. This device integrates Linear's most advanced switching technologies, condensing high power capability into tight spaces while controlling the edge rates and mitigating unwanted field emissions. The integrated synchronous switches are run with controlled switching edges that do not ring—offering just the right balance of high efficiency and low noise—and can be run at up to 2.5MHz, resulting in compact solutions.

(continued on page 4)

In this issue...

Linear in the News

LINEAR TECHNOLOGY TO COMBINE WITH ANALOG DEVICES

On July 26, Analog Devices and Linear Technology announced a definitive agreement to combine the two companies. The planned combination will create a premier global analog company with strengths in data converters, power management, amplifiers, interface, RF and microwave products.

Bob Swanson, Executive Chairman and Co-founder of Linear Technology, added, "For 35 years, Linear Technology has had great success by growing its business organically. However, this combination of Linear Technology and Analog Devices has the potential to create a combination where one plus one truly exceeds two. Analog Devices is a highly respected company. By combining our complementary areas of technology strength, we have an excellent opportunity to reinforce our leadership across the analog and power semiconductor markets. Together, Linear Technology and Analog Devices will advance the technology and deliver innovative analog solutions to our customers worldwide."

"The combination of Analog Devices and Linear Technology brings together two of the strongest business and technology franchises in the semiconductor industry," said Vincent Roche, President and Chief Executive Officer of Analog Devices. "Our shared focus on engineering excellence and our highly complementary portfolios of industry-leading products will enable us to solve our customers' biggest and most complex challenges at the intersection of the physical and digital worlds. We are creating an unparalleled innovation and support partner for our industrial, automotive, and communications infrastructure customers."

For now, Linear will continue to operate as an independent company, with no impact on day-to-day operations, products or service. You can look for future news updates here as it develops.

LINEAR EXHIBITS AT HANNOVER FAIR

In April, Linear Technology exhibited at the Hannover Fair in Germany, the world's largest industrial fair. More than 5,200 exhibitors from the around the world exhibited, and the fair had over 130,000 visitors.

At its booth, Linear Technology showcased 10 working demos. The majority of these demos were based on the company's SmartMesh IP™ wireless sensor network solution for the industrial Internet of Things (IoT). These included VersaSense's MicroPnP, a plug-and-play IoT platform based on Linear's SmartMesh IP. Another demo, with partner Vicotee, enables companies to connect with traditional wired sensors over the Internet through a single wireless sensor network based on Linear's SmartMesh® technology. These IoT solutions

can be used in a wide range of applications, including building automation, environmental monitoring, offshore, green energy, smart cities and healthcare.

LINEAR IMPLEMENTS WIRELESS SENSOR NETWORK

Linear has installed a wireless sensor network to monitor gas cylinder usage in its Milpitas, California semiconductor manufacturing facility ("fab"). At Linear Technology's Silicon Valley fab, over 175 specialty gas cylinders are used in the wafer manufacturing process. Gas cylinders must be closely monitored to ensure uninterrupted supply, as an unplanned interruption of gas supply would result in wafer scrappage. Traditionally, technicians manually log the pressure of each gas cylinder in the fab three times a day, a process that is prone to human error and is expensive to maintain.

Manual logging is necessary because the nature of the fab makes communications wiring impractical. Cylinders are located throughout the facility, and for most cylinders, AC power or Ethernet jacks are locally unavailable. The buildings housing the cylinders are constructed of concrete walls for safety reasons, making it cost-prohibitive to install new wires. A large construction project to install power and communications wires would disrupt the manufacturing process, resulting in costly factory downtime. Even traditional wireless solutions would require power connections where none are available.

The SmartMesh IP Wireless Solution

The solution was to install a 32-mote SmartMesh IP wireless mesh network to monitor gas cylinders in the gas bunker. Each independent node monitors a single site and self-connects to the network to transmit measurement data. Each is powered by a pair of lithium AA L91 batteries for an approximate 8-year battery life. No additional wiring was necessary to install the network.

Linear management team rings the NASDAQ opening bell on June 1 to celebrate 30 years as a public company and 35 years since Linear's founding. At left, Linear Co-founder & Executive Chairman Bob Swanson; third from left CEO Lothar Maier; at right, CFO Don Zerio.

Despite the concrete confines of the gas bunker and the prevalence of metal structures in the fab, the network has proven extremely reliable. In its first few months, the network has remained continuously operational, and transmitted over 26 million data readings with >99.99999% reliability—100 times better than the stringent "5 nines" reliability expected of high availability communication and computer systems.

Results

By using real-time gas consumption rates, technicians can precisely predict when gas cylinders will need to be replaced, reducing waste from unused gas due to premature cylinder changes. The benefits extend beyond efficiencies in day-to-day operations. By centrally collecting gas usage data and making it readily available to plant management, this system enables trend analysis, which further identifies opportunities to streamline plant operations by correlating readings with specific semiconductor fab processes and geometries.

For the complete case study, see http://lt.linear.com/o1u. To view a video on the wireless sensor network installation, go to www.linear.com/solutions/7254.

CONFERENCES & EVENTS

The Battery Show/Electric & Hybrid Vehicle Tech Expo, Suburban Collection Showplace, Novi, Michigan, September 13–15, Booth 906—Presenting Linear's battery management system products. More info at www.thebatteryshow.com/

FPGA World Exhibition, Stockholm, Sweden, September 13—Showcasing Linear's high performance analog ICs and solutions. There will be working demos on display, demonstrating the latest products from Linear to enhance and power FPGAs. www.fpgaworld.com/

RADECS 2016 Exhibition and Space Power Conference, Bremen, Germany, September, 19–23—Showcasing Linear's broad line of high performance analog ICs designed specifically for the space market. http://www.radecs2016.com/joomla/

Maker Faire 2016, Rome, Italy, October 14–16—Showcasing Linear's high performance analog ICs, including the MicroPnP and Vicotee solutions based on SmartMesh IP. There will be working applications from European customers. www.makerfairerome.eu/en/ ■

The LT3922's versatility makes it useful in boost, buck and boost-buck applications for exterior daytime running lights, signal lights, tail lights, and headlight segments as well as interior dashboard and heads-up displays with high dimming ratio. Built-in flexibility and fault protection reduce the number of required components to protect against short and open LED strings.

(LT3922, continued from page 1)

CHOICE OF TOPOLOGIES: BOOST, BUCK MODE, BOOST-BUCK

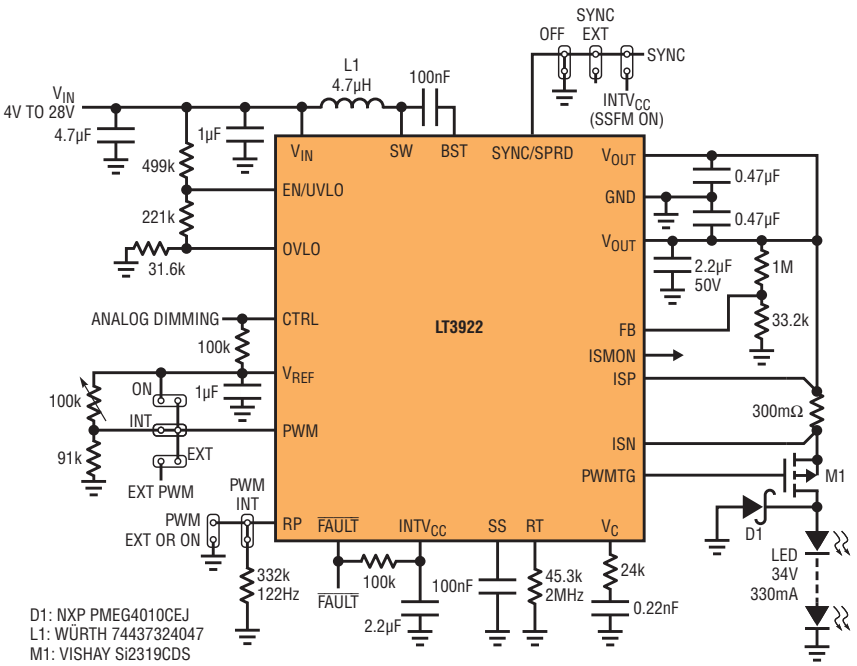
LED strings are driven by a controlled current that does not need to be returned directly to ground. Both LED$^+$ and LED$^-$, or either one, can be attached to non-ground potentials. This opens up the field of options for floating output DC/DC LED driver topologies, including buck mode (step-down) and boost-buck (step-up and step-down). The LT3922's high side PWMTG driver and synchronous switches can be configured as a boost, buck mode or boost-buck LED driver, while retaining use of all of the ICs features—namely, internal PWM dimming, SSFM, low EMI, ISMON output current monitor, and output fault protection carry over from the standard boost topology to the buck mode and boost-buck.

Boost

The LT3922 can power LEDs up to 34V when operated as a boost converter, leaving some headroom, below 40V, for open LED overshoot. The 2MHz, 4V to 28V boost LED driver shown in Figure 1 powers a 330mA string of LEDs at up to 34V. It can be externally PWM dimmed at 120Hz to a 2000:1 ratio or it can be internally dimmed to 128:1 ratio with an analog input voltage on the PWM pin.

It survives open LED and LED$^+$-to-ground short-circuits and reports these faults by asserting its FAULT pin. The output current can be monitored via the ISMON pin, even during PWM dimming. At 2MHz switching frequency, its fundamental EMI harmonic resides above the AM band, but its EMI is still low. Spread spectrum frequency modulation (SSFM) can be added to spread the switching frequency between 2MHz to 2.5MHz and reduce the EMI at the fundamental and its many harmonics. The efficiency of the 2MHz boost converter remains as high as 91% at $12V_{IN}$ due to the integrated synchronous switches. At lower V_{IN}, when the peak inductor current hits its limit, the output current is gracefully reduced without flicker while the LEDs remain on.

Figure 1. 2MHz regular boost schematic with 2000:1 PWM dimming at 120Hz



Buck

The input voltage can be as high as 36V and a string of LEDs can be driven at up to 1.5A when the LT3922 is used in a buck mode topology, as shown in Figure 2. The high side ISP and ISN current sense input and PWMTG PMOS driver are easily moved to the high side of the LEDs, which is connected to the input in buck mode. LED$^-$ is connected directly to the inductor and not to ground. When driving two, 1A LEDs at 6.5V, the synchronous buck mode efficiency is as high as 94% at 12V V_{IN} and remains as high as 89% at 36V V_{IN}. The high bandwidth of the buck mode converter allows it to work with a 1000:1 PWM dimming ratio at 100Hz.

Boost-Buck

The LT3922 boost-buck topology in Figure 3 supports an input voltage range extending above and below the LED string voltage. The sum of the LED string voltage and the input voltage must remain

The patented low EMI boost-buck topology features a boost-type low ripple input inductor and a buck mode-type low ripple output-facing inductor. A 4V–18V automotive input or multiple battery chemistry input (5V, 12V and 19V) boost-buck converter can drive an LED string voltage anywhere between 3V and 16V.

below 35V to keep the ISP and ISN voltage below the 40V absolute maximum.

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As in the other topologies, the PWMTG driver simplifies PWM dimming MOSFET connection. Open- and short-circuit protection are not compromised in the floating LED topologies. An optional diode on LED⁻ protects against LED⁻-to-GND short-circuits.

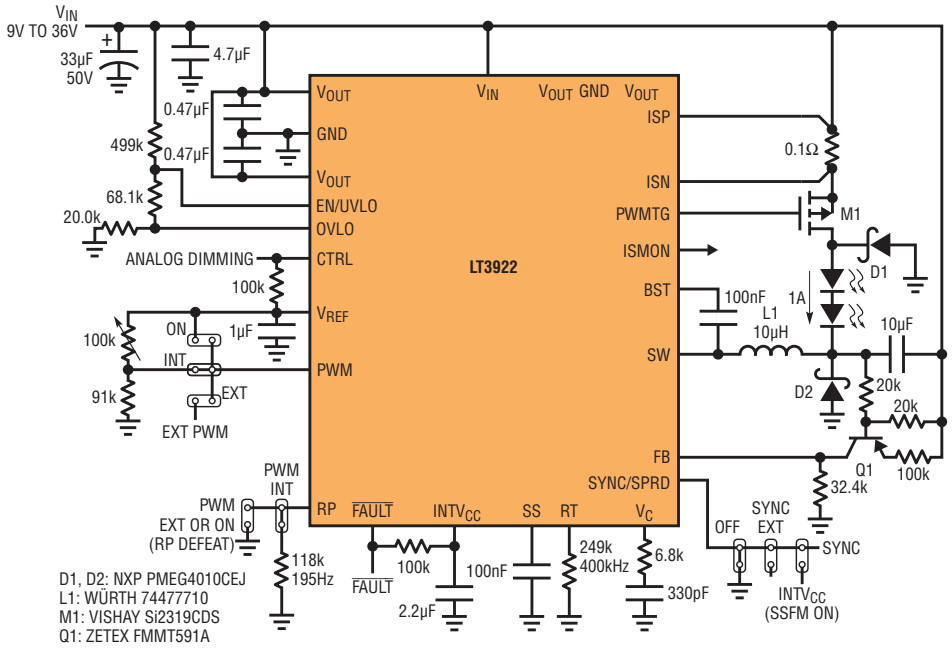

Figure 2. 400kHz buck mode LED driver with 1000:1 100Hz PWM dimming brightness control

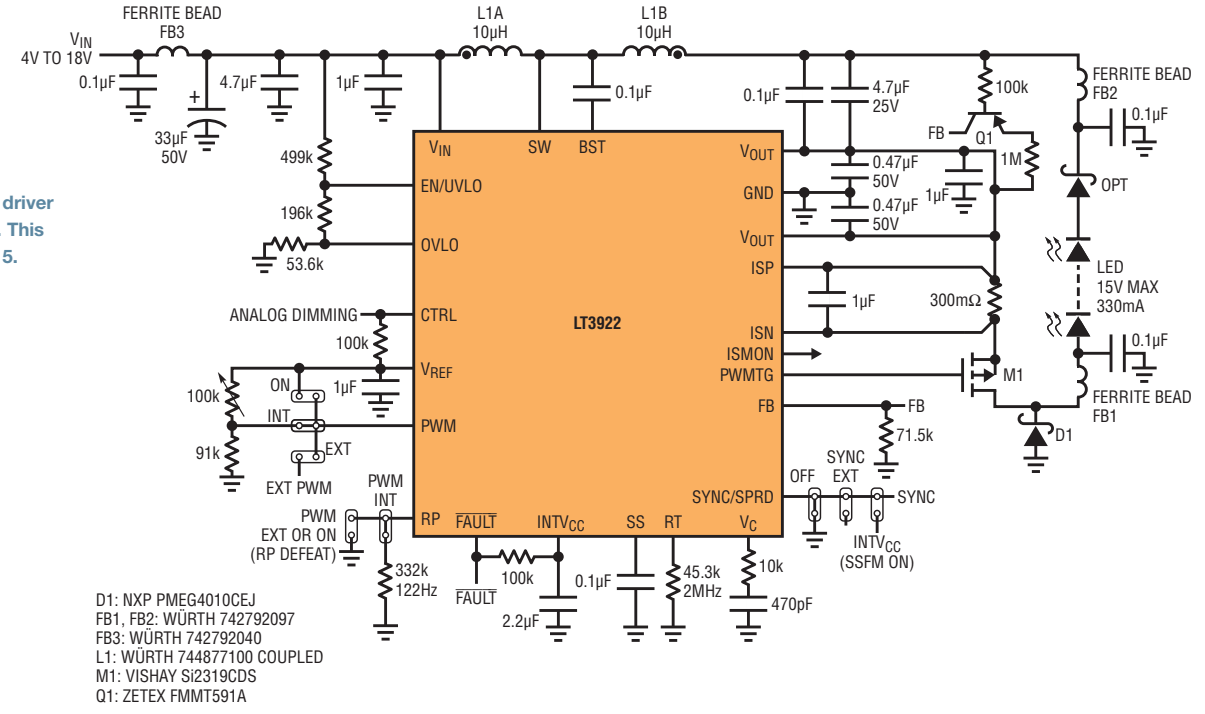

Figure 3. 2MHz boost-buck LED driver with low input and output ripple. This solution passes CISPR 25 Class 5.

The tiny LT3922 LED driver features low EMI, high efficiency and fault protection required in automotive environments. It can be powered from the automotive 9V–16V input range and operates to 36V in the face of transients and down to 3V (cold-crank conditions). Its low EMI Silent Switcher architecture, SSFM, and controlled switching edge rate make it ideal for powering LEDs with low EMI.

The 2MHz converter in Figure 3 features 85% efficiency (87% without EMI filters) at 12V V_{IN}, 15V V_{LED}, 330mA I_{LED} and up to 2000:1 PWM dimming ratio at 120Hz. This solution fits the requirements of an automotive daytime running light, signal light, or tail light LED driver, due to its size, versatility and low EMI.

AUTOMOTIVE LIGHTING

So much about LEDs make them ideal for use in automotive lighting. There is a visual appeal of LED tail and daytime running lights. Efficient LED headlights are robust, with lifetimes orders of magnitude longer than their relatively burn-out-prone filament-based predecessors. Drivers are small and efficient with wide input and output voltage ranges, and should feature low EMI.

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The 400kHz automotive boost LED driver in Figure 4 passes CISPR 25 Class 5 EMI tests, as shown in Figure 5, which shows conducted and radiated EMI test results of the LT3922 along with class 5 EMI limits. This is a result of a combination of LT3922 low EMI features, including, but not limited to, controlled switching edges and spread spectrum frequency modulation (SSFM). Of course, proper layout and a small amount of ferrite bead filtering (FB1 and FB2) should be used for best EMI results.

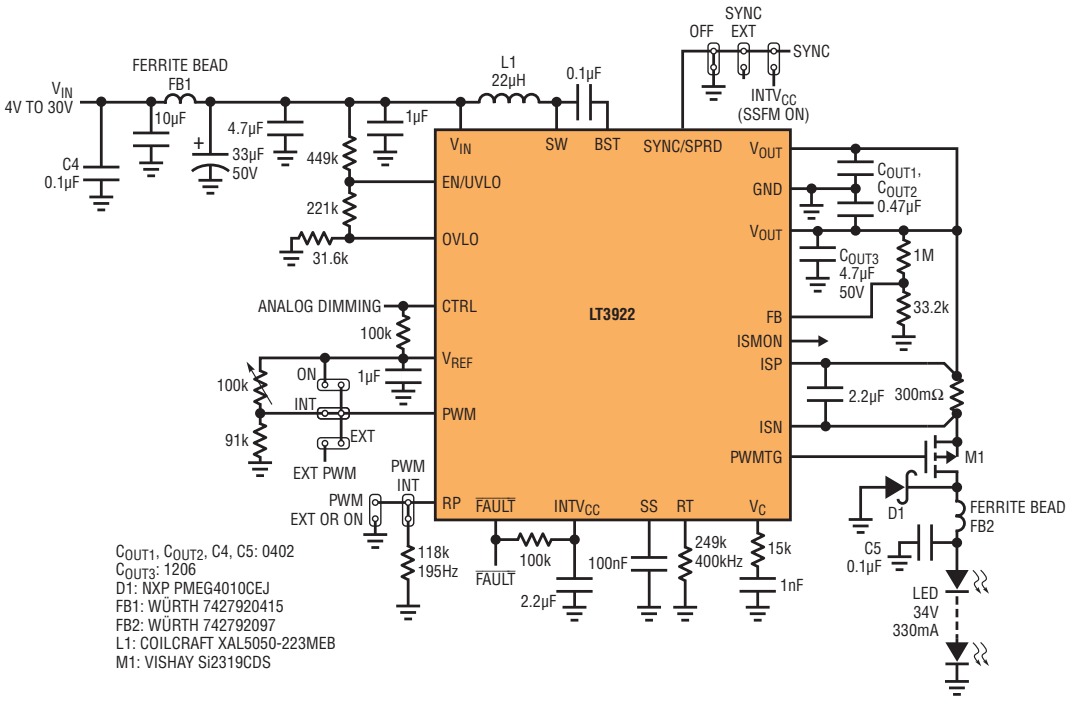


Figure 4. 400kHz automotive boost LED driver with filters for low EMI and option for 100%, 10% or 1% internally generated PWM dimming. EMI tests (Figure 5) show that this solution passes CISPR 25 Class 5.

The switching edge rate is controlled by the LT3922, eliminating high frequency ringing that is common in switching converters without this feature. This is enough to reduce the power switch high frequency EMI without trading off efficiency and power capabilities of this converter. SSFM decreases both the peak and average EMI in the converter at low and high frequencies.

BUILT-IN FEATURES FOR LOW EMI

The LT3922 includes a number of features that enable designers to easily achieve low EMI solutions. First of all, LT3922 incorporates Linear's patented Silent Switcher architecture, where internal synchronous switches minimize hot-switching-loop size and controlled switching edges do not ring.

Figure 6 shows how the LT3922's pinout enables placement of small, high frequency capacitors near the two V_{OUT} pins to minimize hot-loop size and EMI.

The switching edge rate is controlled by the LT3922, eliminating high frequency ringing that is common in switching converters without this feature. The LT3922's controlled switching edges reduce power switch high frequency EMI without degrading efficiency and power capability.

SSFM in the LT3922 spreads the resistor-set switching frequency up and down from 100% to 125% of its value at a rate of 1.6kHz for the 400kHz converter. This decreases both the peak and average EMI in the converter at low and high frequencies. The feature is easy to turn on and off by connecting the SYNC/SPRD pin to $INTV_{CC}$ or GND, respectively.

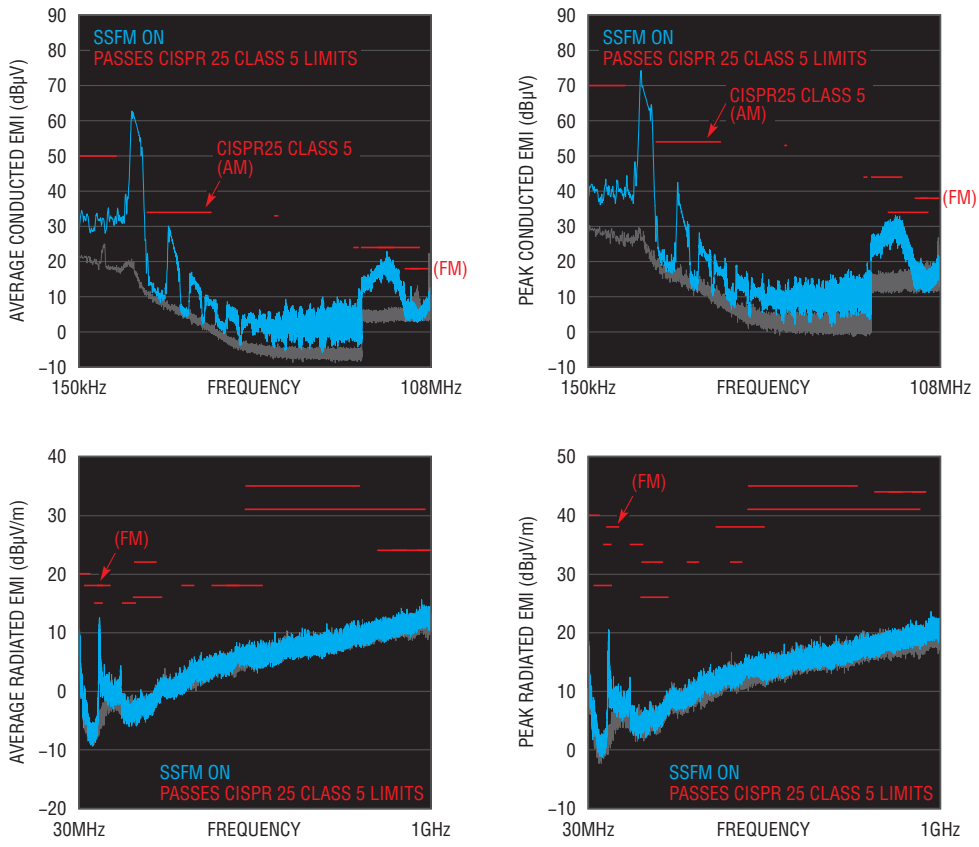


Figure 5. EMI profile of the 400kHz LED driver shown in Figure 4, which passes CISPR 25 Class 5 with minimal EMI filters. A larger LC filter can be added to the input if further EMI reduction is needed for specific manufacturer EMI requirements.

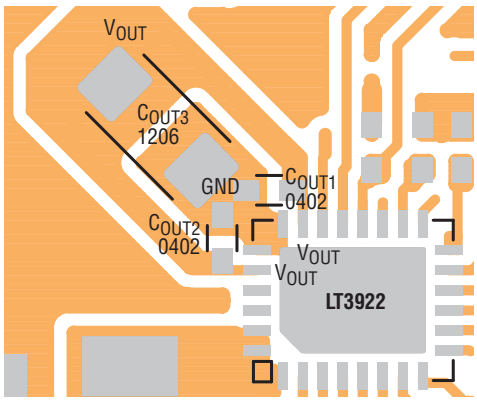


Figure 6. The dual-loop layout and high frequency 0402 split capacitors create small, opposing hot-loops that help reduce high frequency EMI

The LT3922 features an internally generated PWM dimming signal, which enables duty cycle control via a simple voltage applied to the PWM pin, making PWM dimming at a 128:1 ratio as easy to implement as analog dimming—no external PWM signal or microcontroller required. The PWM period, such as 122Hz, is set by a single resistor on the RP pin.

INTERNALLY GENERATED PWM DIMMING

Analog dimming via adjustable voltage on the CTRL pin has always been easier to implement than the more accurate PWM dimming. Until now, PWM dimming required an external clock or micro signal whose duty cycle controlled the brightness via the PWM input pin. However, the LT3922 features an internally generated PWM dimming signal that only requires an external voltage on the PWM pin to set the duty cycle for 128:1 PWM dimming. The PWM period, such as 122Hz, is set by a single resistor on the RP pin.

LED current accuracy is a necessity for vehicles with redundant light clusters. The brightness of both sides must match for obvious reasons. Identically manufactured LEDs can produce different brightnesses at the same drive current. The internal dimming feature of the LT3922 can be used for brightness trimming near or just below 100% duty cycle and then set to accurate 10:1 or 100:1 ratios. This can save the light cluster manufacturer from paying extra for specially binned LEDs.

When higher dimming ratios are needed, the LT3922 can be externally dimmed in the usual manner. The high bandwidth 400kHz buck mode LED driver in Figure 2 yields a 1000:1 PWM dimming ratio at 100Hz. The 2MHz boost LED driver in Figure 1 can achieve 2000:1 dimming ratio at 120Hz as shown in Figure 7a. The same circuit can be set up for internally generated PWM dimming by placing a 122Hz frequency resistor on the RP pin and setting the PWM pin voltage between 1.0V and 2.0V for up to 128:1 dimming as shown in Figure 7b. The LT3922 can be set up to run with up to 5000:1 external PWM dimming in some applications and PWM dimming can be combined with LT3922's analog dimming for over 50,000:1 brightness control.

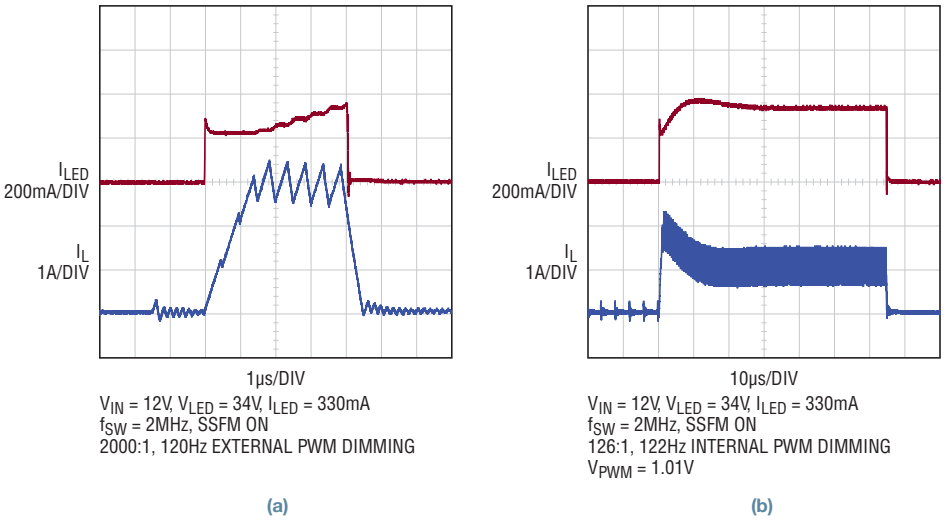


Figure 7. (a) Externally generated 2000:1 or 4000:1 PWM dimming of Figure 1 and (b) internally generated 128:1 PWM dimming of Figure 1.

MACHINE VISION

In industrial assembly line applications, machine vision (Figure 8) provides rapid visual feedback of devices using high speed digital photography in conjunction with digital image processing. This helps rapidly identify and isolate defective products with little or no human inspection. The lighting used for machine vision systems must be synchronized with the speed of the assembly line processes while maintaining the ability to produce a consistent pulse of light for an indefinite period of off-time.

Conventional LED drivers are unable to maintain their output voltage after the PWM input signal is held low for any sustained amount of time. This is due to the gradual discharge of the output capacitor, making generic LED drivers unsuitable for these types of applications. However, the LT3922 digitally samples the output state of the converter during the falling edge of the PWM signal. It then maintains its output voltage during prolonged off-times by performing "maintenance switching" during the PWM off-time while the LEDs are disconnected by the high side PMOS. During standard PWM dimming at frequencies above 100Hz, the longest off-time is 10ms or less, and not much leakage current can be pulled off the output at that time. Machine vision and strobe applications can have long off-times between 100ms and 5s (or longer), allowing for tens to hundreds times more leakage.

Maintenance switching ensures that the output capacitor maintains the voltage recorded during the LT3922's previous sample cycle. The digital sample of the state of the converter is stored indefinitely, assuming uninterrupted input power is provided to the IC. This allows the LT3922 to have a consistent output current waveform for any given off-time, as demonstrated in Figure 9.

CONCLUSION

The LT3922 36V LED driver with internal, synchronous, 2A switches is a compact and versatile LED driver. It can be easily used in boost, buck and boost-buck topologies. Regardless of topology, all of its features are available, including high PWM dimming capability and internally generated PWM dimming. Low EMI is easily achievable with its Silent Switcher layout and SSFM. Its compact and synchronous switches maintain high efficiency, even at frequencies up to 2MHz. With robust fault protection, this IC easily meets the requirements of automotive other demanding applications. ■

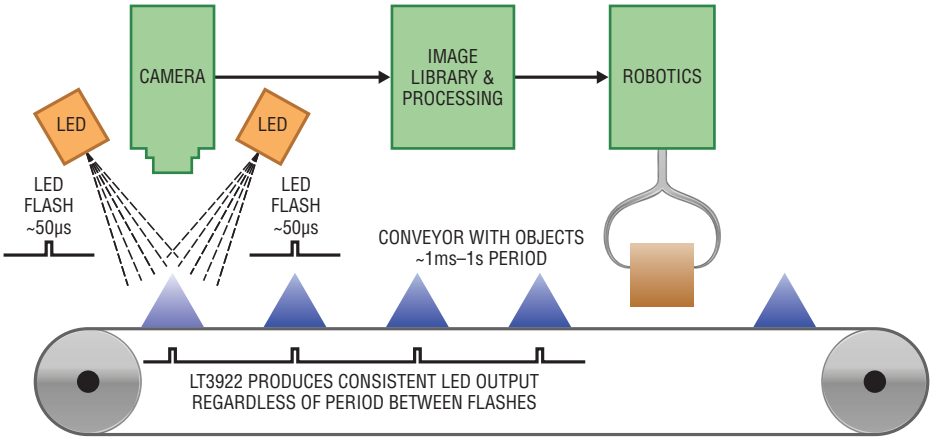


Figure 8. Assembly line system overview with machine vision application

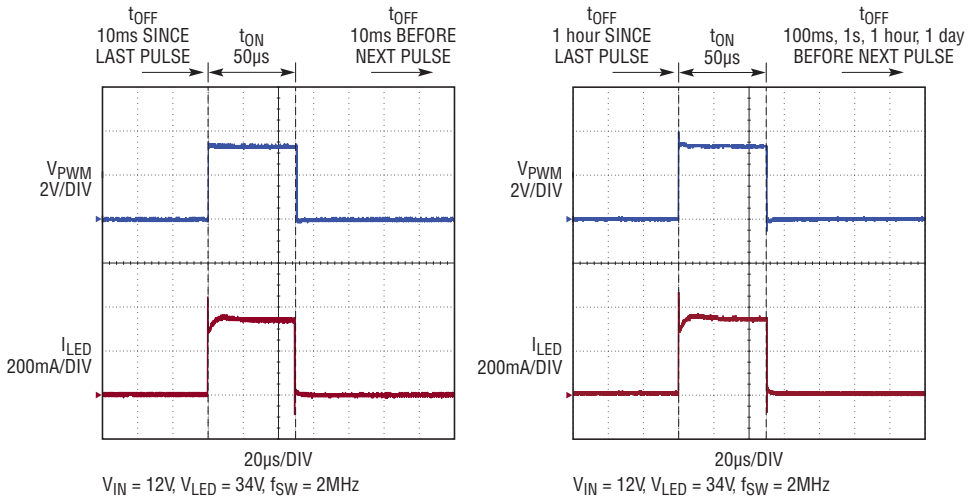


Figure 9. Camera flash waveform looks the same regardless of idle or down time. Waveforms show pulse after 10ms and after one hour. The flash looks the same after sitting idle for one hour as it does after 10ms. These results are for the circuit shown in Figure 1.

Table 1. Wide input range LED drivers

	LT3922	LT3795	LT8391	LT3952	LT3518
V_{IN} Range	2.8V–36V	4.5V–110V	4V–60V	3V–42V	3V–30V (40V transient)
Synchronous	✓		✓		
Frequency Range	200kHz–2.5MHz	100kHz–1MHz	150kHz–650kHz	200kHz–3MHz	250kHz–2.5MHz
Peak Switch Current	2A	10A+	10A+	4A	2.3A
SSFM	✓	✓	✓	✓	
TG PWM	✓	✓	✓	✓	✓
Internal PWM Dimming	✓		✓	✓	
Short-Circuit Proof	✓	✓	✓	✓	
Package	4mm × 5mm QFN	28-Lead TSSOP	4mm × 5mm QFN	28-Lead TSSOP	4mm × 4mm QFN
Power Switches	two internal	single external	four external	single internal	single internal

Power Supply Sequencing Simplified

Nathan Enger

The challenges in designing a multiple power supply multiply with each additional supply rail. The designer must consider the dynamic environment of coordinated power supply sequencing and timing, generating power-on reset, monitoring for faults and responding appropriately to protect the system. An experienced designer recognizes that flexibility is key to successfully navigating the ebb and flow as a project moves from prototype to production. The ideal solution minimizes the number of hardware and software changes during development.

The ideal multisupply design tool is a single IC that resides in a design from beginning to end, requiring no wiring changes through the life cycle of the product. It autonomously supervises and sequences multiple power rails, cooperating with other ICs to seamlessly supervise many power regulators in the system, and provides fault and reset management. The designer can use powerful PC-based software to configure, visualize and debug system behavior in real time when connected to an I²C bus.

The LTC®2937 fits this bill. It is a 6-channel voltage sequencer and high accuracy supervisor with EEPROM. Each of the six channels has two dedicated comparators to accurately monitor over- and undervoltage conditions to within ±0.75%. The comparator thresholds are individually programmable over a range of 0.2V to 6V with 8-bit resolution. The comparators are fast, with deglitched propagation delays of 10µs. Each sequencer channel has an enable output that can control an external regulator, or the gate of a pass FET. All aspects of supervisor voltage and sequencer timing are individually configurable, including up- and down-sequence order, sequence timing parameters, and fault response. The built-in EEPROM makes the part completely autonomous and able to power-up in the correct state to control the system. In addition, multiple LTC2937s can cooperate to autonomously sequence up to 300 supplies in a system, all using a single-wire communication bus.

Power supply faults are controllable, visible and manageable through the LTC2937's autonomous fault response behaviors, and through debug registers. The LTC2937 automatically detects fault conditions and can power down the system in a coordinated manner. It can remain off, or attempt to resequence the supplies after the fault. In a system with a microcontroller and an I²C/SMBus, the LTC2937 provides detailed information regarding the type and cause of the fault, and the state of the system. The microcontroller can make decisions about how to respond, or allow the LTC2937 to respond on its own.

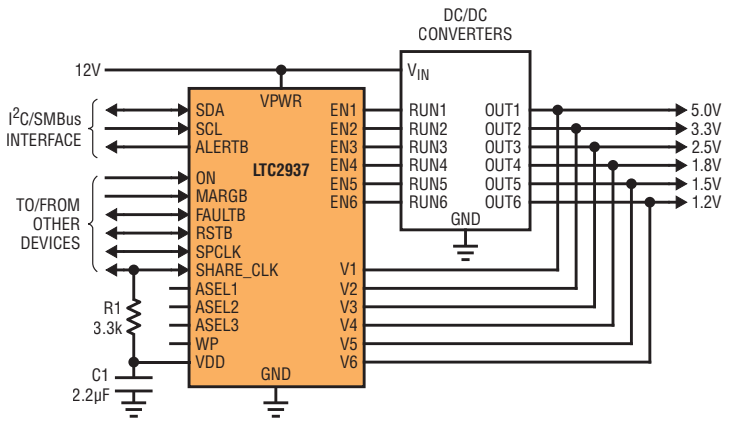


Figure 1. LTC2937 sequencing six supplies

THREE STEPS OF POWER SUPPLY CONTROL

A power supply cycle has three operating steps: sequence-up, monitoring and sequence-down. Figure 2 shows these phases for a typical system. During up-sequencing, each power supply must wait its turn, and then power up to the correct voltage in a designated amount of time. During the monitoring phase each power supply must remain within designated over- and undervoltage

Each of the LTC2937's six channels has two dedicated comparators to accurately monitor over- and undervoltage conditions to within ±0.75%. The comparator thresholds are individually programmable over a range of 0.2V to 6V with 8-bit resolution.

limits. During down-sequencing, each supply must wait its turn (often in a different order from up-sequencing), then power down within a configured time limit. At any point, something can go wrong, causing a fault in the system. The design challenge is to create a system in which all of these steps, and all of the variables, are easily configurable, but carefully controlled.

Sequence-up begins when the ON input transitions to active. The LTC2937 advances through its up-sequence, enabling each supply in turn, and monitoring to ensure that the supply voltage rises above the configured threshold before the configured time. Any supply that fails to meet its assigned timing triggers a sequencing fault.

A unique benefit of the LTC2937 is its sequence position clock. Each channel is assigned to a sequence position (1–1023), and receives its enable signal when the LTC2937 counts to the given number in the sequence. A channel with sequence position 1 is always enabled before a channel with sequence position 2. If a system specification changes, requiring these

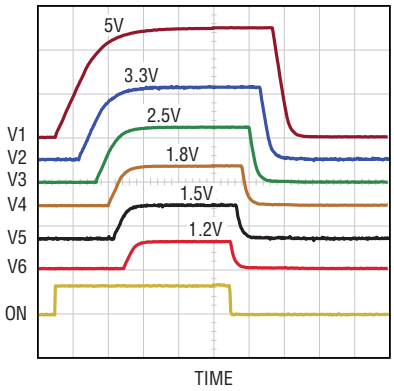


Figure 2. Power supply sequencing waveforms

two channels to sequence in a different order, then the sequence positions can be swapped, powering the second channel in sequence position 1, and the first in position 2. Multiple LTC2937s can share sequence position information, so that sequence position N happens at the same time for all LTC2937 chips, and channels controlled by different chips can participate in the same sequence (see Figure 3).

The monitoring phase begins when the last channel sequences up and crosses its undervoltage threshold. During monitoring, the LTC2937 uses its high accuracy comparators to continuously monitor the voltage at each input against over- and undervoltage thresholds. It ignores minor glitches on the inputs, only triggering if the voltage crosses the threshold with sufficient magnitude for sufficient time. When the LTC2937 detects a fault, it responds immediately according to its configured supervisor fault response. In a typical scenario, it shuts down all supplies simultaneously, asserting RESETB to the system, then it attempts to resequence up according to the normal start-up sequence. This prevents the supplies from powering parts of the system while others are unpowered, or executing an uncoordinated recovery after the fault. Multiple LTC2937s in a system can share fault state, and respond to each other's faults, maintaining complete coherence between cooperating channels during fault recovery. The LTC2937 offers numerous programmable fault response behaviors to satisfy many different system configurations.

The sequence-down phase begins when the ON input transitions low. The sequence position clock begins its count

Table 1. Programmable 6-channel sequencer and supervisors with EEPROM

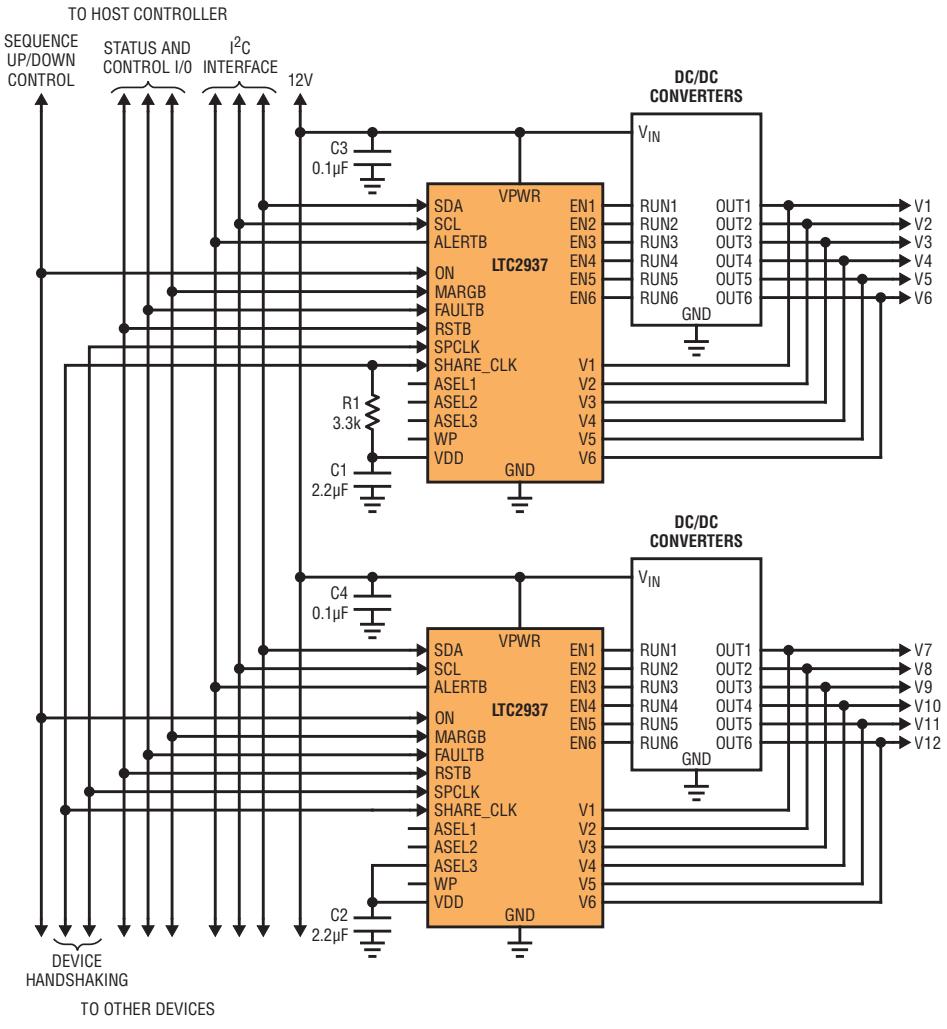
	LTC2933	LTC2936	LTC2937
Sequencer	No	No	Yes
Comparator Outputs	No	Yes	No
Threshold Range	1V to 13.9V (1×) 0.2V to 5.8V (5×)	0.2V to 5.8V (6×)	0.2V to 6V (6×)
Threshold Accuracy	±1%	±1%	±0.75%
Power Supply	3.4V to 13.9V	3.13V to 13.9V	2.9V to 16.5V
Package (mm × mm)	5×4 DFN-16, SSOP-16	4×5 QFN-24, SSOP-24	5×6 QFN-28

The LTC2937's extensive register set is powerful, yet mastering it is simple. The LTpowerPlay graphical user interface (GUI) displays all of the status and debug register information in one convenient interface.

again to bring the supplies down, but all of the sequence-down parameters are independent from the sequence-up parameters. Channels can sequence down in any order, and multiple LTC2937 chips coordinate sequencing of all controlled supplies. During the down-sequence, each supply must fall below its discharge threshold within its configured time limit, or trigger a sequencing fault. The LTC2937 can pull down on the supply with an optional current source to actively discharge slow moving supplies.

The sequence position clock enforces event-based sequence order, with each event waiting for preceding events before it can continue. The LTC2937 also allows time-based sequencing, and can participate in systems that enable supply rails at predetermined time points. Reconfigurable registers function in either time-based or event-based mode.

Figure 3. Typical connections between multiple LTC2937s



LTpowerPlay MAKES IT SIMPLE

The LTC2937's extensive register set is powerful, yet mastering it is simple. The LTpowerPlay® graphical user interface (GUI) displays all of the status and debug register information in one convenient interface. The GUI communicates with any Linear Technology power system management IC (including the LTC2937) on the I²C/SMBus. Configuring one or more LTC2937s is as simple as a few clicks of the mouse.

LTpowerPlay saves settings on the PC, and can write them into the LTC2937 EEPROM. The GUI also shows all of the debug information for system malfunctions. LTpowerPlay can show when any supply is over- or undervoltage, or if a supply has failed sequence timing. After a fault, the GUI allows complete control over restarting the system. In every stage of the design—start-up, configuration, debug, and operation—LTpowerPlay is an indispensable window into system performance.

CONCLUSION

The LTC2937 simplifies power system sequencing and supervision. It requires very little board real estate for a complete system. It is flexible and reconfigurable, yet autonomous through its EEPROM memory. It can operate on its own, or in concert with other chips in a large system, seamlessly orchestrating the operations of up to 300 power supplies. ■

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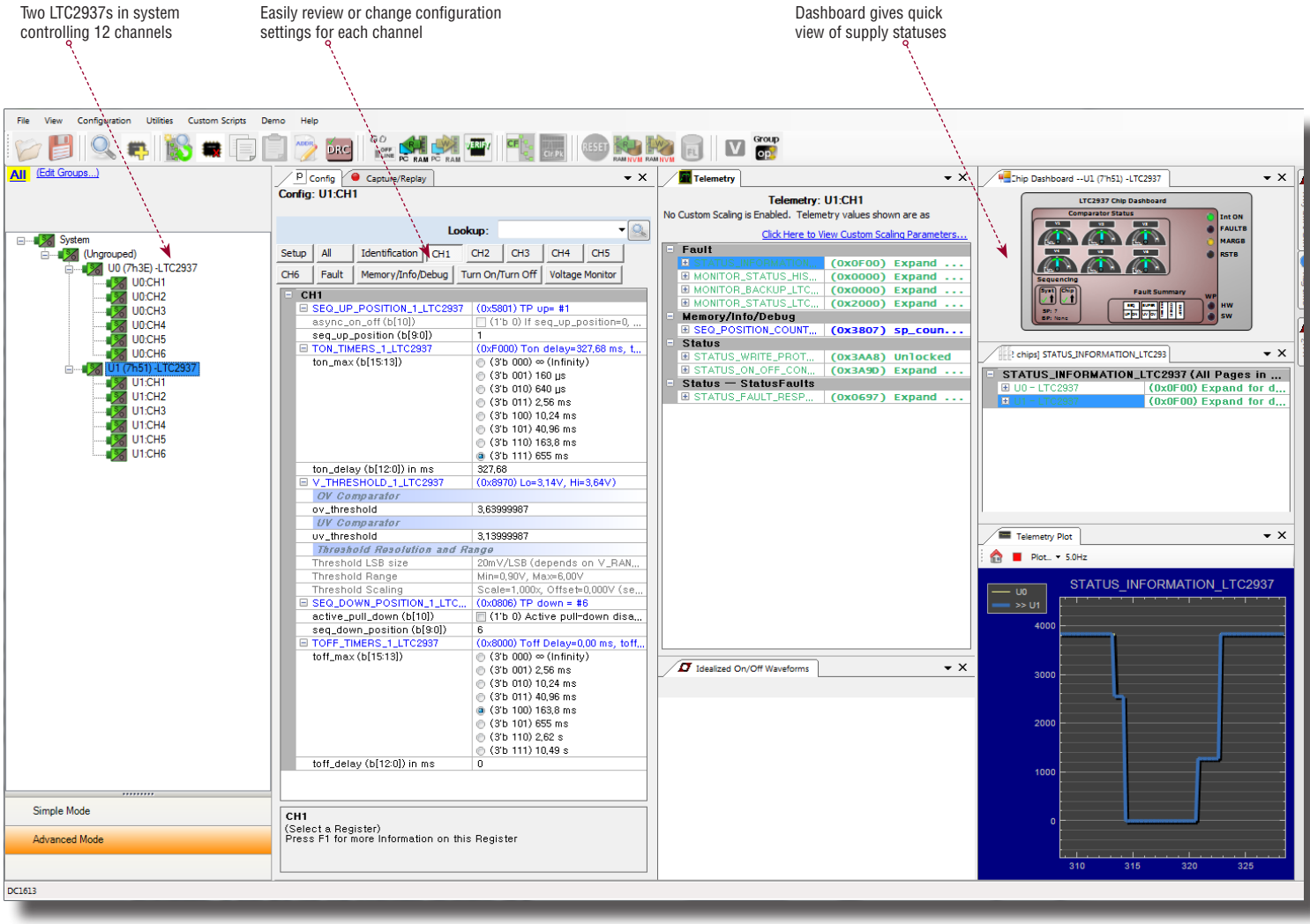
Figure 4. LTpowerPlay graphical user interface (GUI) displays all of the status and debug register information in one convenient interface. Configuring one or more LTC2937s is as simple as a few clicks of the mouse. LTpowerPlay saves settings on the PC, and can write them into the LTC2937 EEPROM.



Ultrathin Triple Output µModule Regulator for DDR, QDR and QDR-IV SRAM Fits 0.5cm² Area and Backside of PCB

Sam Young and Afshin Odabaee

Delivering the highest RTR (random transaction rate) of QDR (quad data rate) SRAMs, QDR-IV provides up to 400Gbps data transfer for high bandwidth networking, high performance computing and intensive data processing applications. A key challenge at these faster data rates is maintaining the integrity of the data transferred between the SRAM and devices such as high speed FPGAs and processors.

A good solution is to place the SRAM—QDR-IV, QDR or DDR, for example—very close to the interfaced devices on the PCB's topside. To conserve PCB area and minimize induced PCB parasitic noise on data bus lines, the DC/DC regulator circuit powering the QDR-IV SRAM data bus drivers should be placed nearby. The challenge is finding space for regulators on a densely populated PCB.

Using a complete DC/DC regulator with onboard inductor and MOSFETs housed in a compact package is one solution. But the scarcity of area on the top of the PCB can render even compact solutions insufficient. If the footprint, height and weight of the DC/DC regulator solution can be reduced enough, it can be placed on the backside of the PCB where space is available.

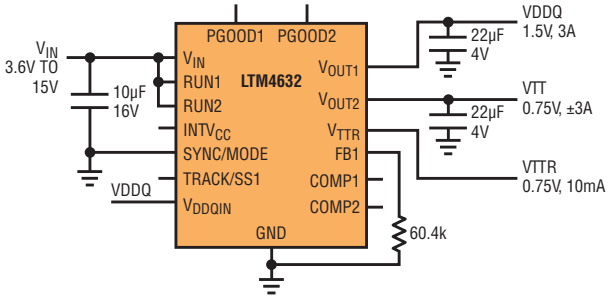


Figure 1. Typical LTM4632 DDR3 application

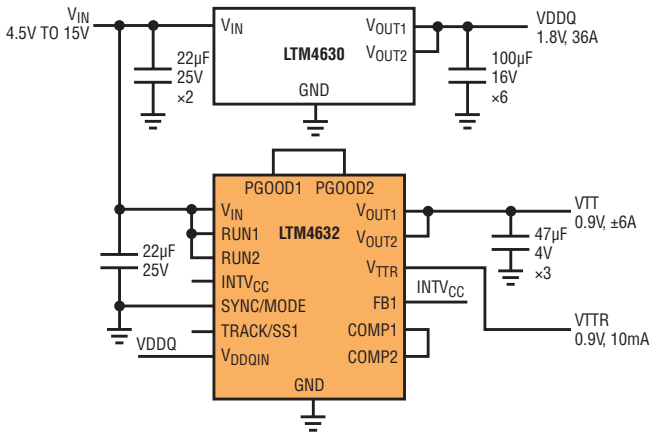


Figure 2. LTM4632 two phase single output ±6A VTT with 36A LTM4630 VDDQ supply

VTT, VDDQ, V_{REF} FROM $12V_{IN}$ IN A TINY ULTRATHIN PACKAGE

The LTM®4632 is a complete triple output step-down µModule® regulator specifically designed to support all three voltage rails required by the new QDR-IV and older DDR RAMs, housed in a 0.21g miniature ultrathin profile LGA package (6.25mm × 6.25mm × 1.82mm).

Included in the package are the switching controllers, divide-by-2 circuit, power FETs, inductors and support components. Its tiny footprint and low external component count (as low as one resistor and three capacitors) occupies only 0.5cm² (dual-sided) or 1cm² (single-sided) while its thin profile enables mounting on the PCB bottom side to free up space on the topside for super-compact board designs.

The LTM4632 operates from an input voltage between 3.3V and 15V, providing precision output rail voltages between 0.6V and 2.5V. Its two switching regulator outputs, V_{OUT1} and V_{OUT2}, provide up to 3A for VDDQ and ±3A for VTT bus termination rails, respectively. Its third output provides a low noise buffered 10mA output for the termination reference (VTTR) tracking voltage. Figure 1 shows the LTM4632 circuit in a typical DDR3 application, illustrating its simple solution and small component count.

The ultrathin LTM4632 provides a complete high performance regulator solution for all three rails required in DDR/QDR RAM applications. Its wide operating range, features and compact solution size make it highly flexible and robust, and capable of fitting into the tightest spaces on the topside and backside of a PCB.

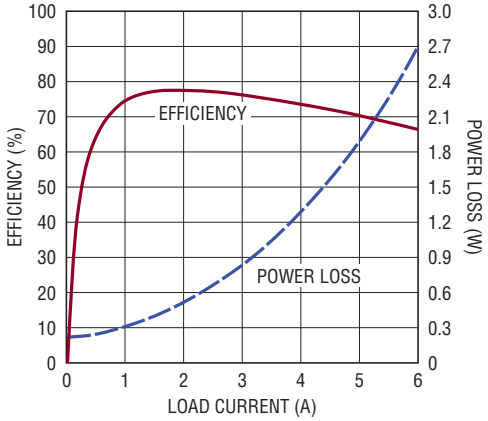


Figure 3. LTM4632 efficiency and power loss. 12V input. (Figure 2 design)

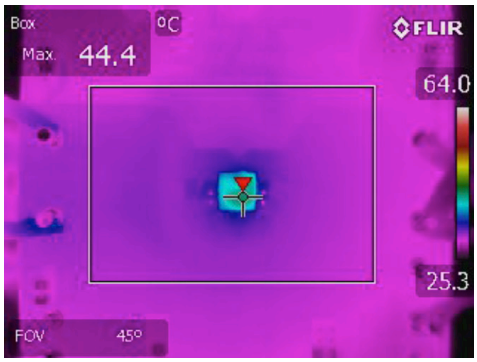


Figure 4. LTM4632 thermal performance. 12V input, 3A. (Figure 2 design)

POWERING MORE SRAM MODULES

The LTM4632's design flexibility enables it to support a broad range of application requirements. For example, its VDDQIN input allows the VTT and V_{REF} rail voltages to be set as either a typical ½ × VDDQ voltage or programmed by an external reference voltage for other values. The LTM4632 can be configured as a two phase single output rail for VTT in applications needing more than a ±3A termination rail current. These features allow the LTM4632 to support voltage requirements for many different SRAMs and increase load current requirements for larger memory arrays.

Figure 2 illustrates the flexibility of the LTM4632. The two switching regulator outputs of the LTM4632 are connected in a PolyPhase® current sharing configuration to provide up ±6A VTT for larger memory banks. For more than 6A VDDQ, the LTM4632 can be combined with other µModule regulators, such as the LTM4630, to provide up to 36A for large SRAM arrays. Efficiency and power loss are shown in Figure 3, with thermal performance for the LTM4632 shown in Figure 4.

TIGHT REGULATION WITH FAST TRANSIENT RESPONSE

The LTM4632's unique controlled on-time current mode architecture and internal loop compensation allow for a fast transient response with good loop stability over a wide range of operating conditions and output capacitance. Voltage regulation for its switching regulator outputs is precise, with guaranteed low ±1.5% maximum total DC output voltage error over line, load and temperature.

Figures 5 and 6 show the fast transient performance and tight load regulation of the LTM4632 VTT rail of the Figure 2 circuit.

CONCLUSION

The ultrathin LTM4632 provides a complete high performance regulator solution for all three rails required in DDR/QDR RAM applications. Its wide operating range, features and compact solution size make it highly flexible and robust, and capable of fitting into the tightest spaces on the topside and backside of a PCB. ■

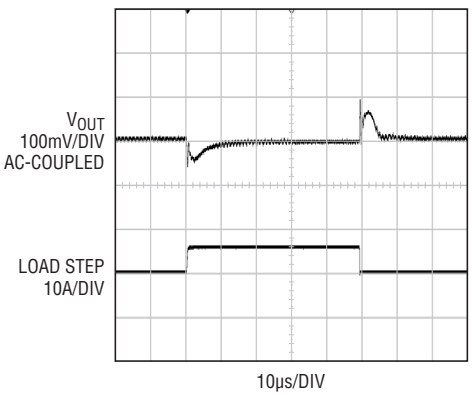


Figure 5. VTT load step, –3A to 3A (Figure 2 design)

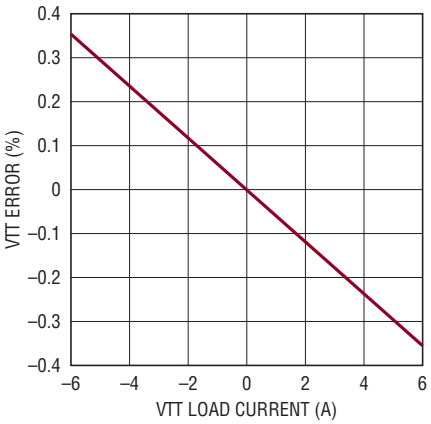


Figure 6. VTT load regulation (Figure 2 design)

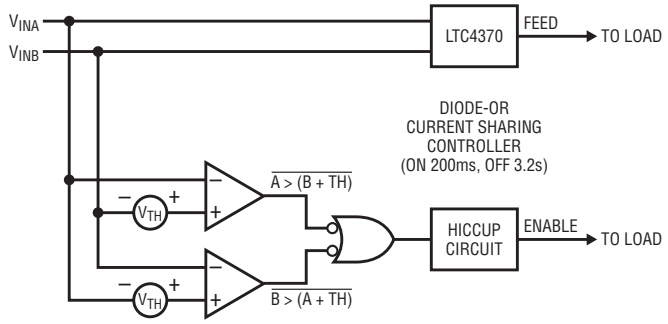
Using a Current Sharing Controller when the Sum Current of Both Supplies is Required to Support the Load

Bob Smith

The LTC4370 is a 2-supply current sharing, diode-ORing controller that uses MOSFETs to form ideal diodes. In this way, the LTC4370 can actively balance the output currents of two supplies, even those with unequal output voltages. For two unequal voltage input supplies, the forward voltage of the higher voltage supply diode is servoed to balance the shared load current. The maximum allowable voltage drop is programmed by a resistor at the RANGE pin of the LTC4370.

Normally the LTC4370 is used to current share the outputs of two supplies, either of which is capable of providing the entire load current when its mate drops below the sharing voltage threshold set by the RANGE pin of the LTC4370 (see sidebar).

Figure 1. Block diagram of current summing circuitry



Load Summing Advantage

A typical diode-OR system is a winner-take-all system where the highest voltage supply sources the entire load current. This one-supply-at-a-time scheme underutilizes the two supplies. The LTC4370's current sharing diode-OR solution, on the other hand, reaps the benefits of sourcing and sharing current from both supplies:

- Supply lifetimes are extended if each takes on half the load, spreading the supply heat and reducing thermal stresses on supply components.
- Because the lower voltage supply is always operational, there is no surprise when transitioning to a backup supply that may have already silently failed—a possibility in a simple diode-OR system.
- The recovery dynamics on supply failure are smoother and faster, since the supply changes are on the order of less and more, not off and on.
- A DC/DC converter formed by two supplies running at half capacity has better overall conversion efficiency than a single supply running near full capacity.

Nevertheless, the advantages of using the current sharing function can still be reaped in a non-redundant system, where the sum load current of two supplies is equal to, or in excess of that required by the load.

In normal operation, the LTC4370 allows the higher voltage supply to source all of the load current, however, in the case where the remaining supply is incapable of providing the full current, it is necessary to prevent such operation. This article describes a solution that disables the downstream load when this situation occurs.

PRINCIPAL OF OPERATION

In normal operation, the LTC4370 monitors the current of both supplies. Normally, with a perfect diode, the supply with the higher voltage would source all of the current to the load. The LTC4370 prevents this by linearly controlling the MOSFET of the higher voltage supply to provide current equal to that of the lower voltage supply. The maximum voltage difference allowed is determined by the resistor between the RANGE pin and ground.

When the input supply voltage difference rises beyond the programmed range, the LTC4370 disables the current sharing function. There are two alarm outputs, each monitoring the control voltage at the gate of each MOSFET. In normal operation, when either MOSFET is turned off (indicating a voltage difference beyond the programmed range) its associated FETON signal is set to a logic low.

In theory it seems that if these signals were passed through a logic AND function, they could be used to control the downstream load, disabling it when a MOSFET is

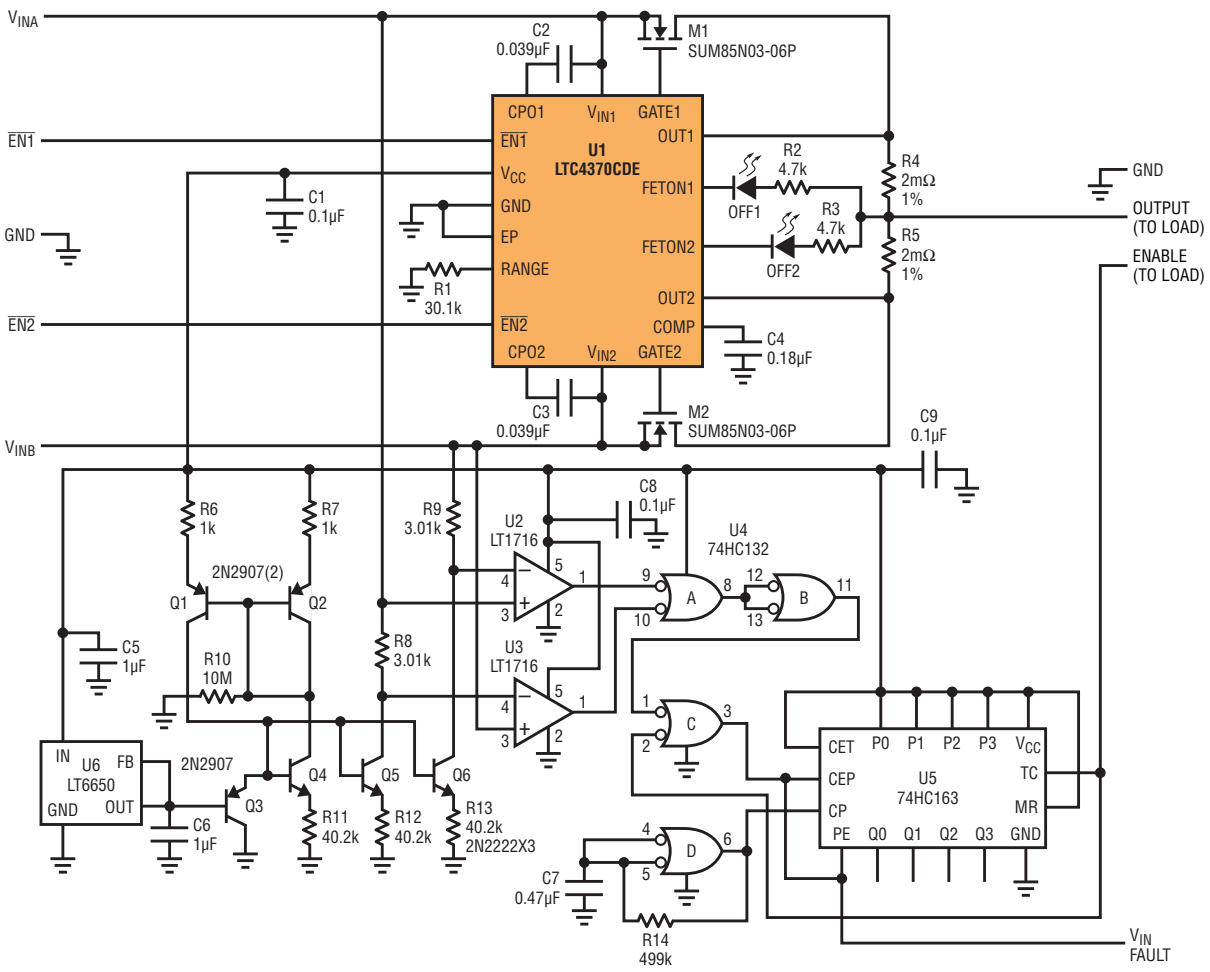
The LTC4370 is designed primarily as a current sharing, diode-OR controller for two redundant supplies. With a few additional components, it can be easily be used in a non-redundant supply environment as a robust load sharing controller, where both of the supplies are necessary to support the entire load. The solution described here provides that function.

turned off (indicating the loss of current sharing). These signals, however, both revert to logic low when zero current is passing through the MOSFET. In this situation, with the downstream load disabled and drawing no current, the system would remain in this state indefinitely.

The solution described here senses input voltage differences and disables the downstream load when a defined voltage difference between the supplies is detected. This voltage difference is programmed to be below the maximum voltage threshold of the LTC4370. If an out of balance condition is detected, the downstream power supply is disabled. To prevent an oscillatory condition, the circuit enters hiccup mode, where the supply is cycled on for 200ms every 3.2 seconds. The block diagram is shown in Figure 1.

As shown in the block diagram, two comparators are used to sense when the absolute value of the difference between power supply inputs VINA and VINB is beyond that allowed for proper current sharing. When this happens, the output of the negative true OR gate is a logic high,

Figure 2. Complete load sharing design



A typical diode-OR system is a winner-take-all system where the highest voltage supply sources the entire load current. This one-supply-at-a-time scheme under-utilizes the two supplies. The LTC4370's current sharing diode-OR solution, on the other hand, reaps the benefits of sourcing and sharing current from both supplies.

enabling the hiccup circuit. Normally, the output of the hiccup circuit is a logic high, enabling the downstream load. When the out of range fault condition is detected, the hiccup circuit is activated, causing a logic low to disable the downstream load. The hiccup circuit monitors the voltage differential during the 200ms on period and is disabled when the fault condition is cleared.

CIRCUIT DESCRIPTION

Figure 2 shows the complete solution. In Figure 2, U2 and U3 are LT1716 Over-The-Top® voltage comparators used to detect voltage differences between V_{INA} and V_{INB}.

Threshold offset voltage to the comparators is provided by current sink transistors Q5 and Q6 in combination with R8 and R9. Current at the collectors of Q5 and Q6 is stabilized at 100µA by transistors Q1, Q2, Q3, and U6, an LT6650 voltage reference. In this case, R8 and R9 are set to 3.01k, resulting in an offset of 300mV. These resistor values can be changed to provide a different offset to match that of the LTC4370.

When either comparator U2 or U3 reaches the threshold determined by the offset, their output becomes logic low, enabling the hiccup circuit.

U4 is a 74HC132 quad CMOS NAND gate with hysteresis on each input. U5 is a 74HC163 4-bit programmable CMOS counter.

The output of U4A is logic low when VINA and VINB is within the threshold determined by R8 and R9. When VINA and VINB is beyond this threshold, the corresponding comparator output becomes logic low, causing the output of U4A to become a logic high.

A logic high output of U4A is inverted by U4B, producing a logic low at one input of NOR gate U4C. The resulting logic high output of U4C causes counter U5 to begin counting. The first count is zero, causing the TC (terminal count) pin to become logic low. This output remains low for the next 15 counts regardless of the input from U11B, due to the feedback from its output to the other input of NOR gate U4C. On count 16, the TC becomes high for a period of 200ms. During this period, the downstream load is enabled. If the comparators determine the voltage difference is within limits, the counter stops with the TC output remaining logic high, enabling the load. If the voltage difference is not within limits, the counter begins again, counting to 15 with the TC output a logic low. In this way, the load is enabled for 200ms every 3.2 seconds until the fault condition is cleared.

The clock is provided by U4D, a hysteretic relaxation oscillator with a period of 200ms determined by R14 and C7.

U1 is the LTC4370, which provides the current sharing function. The threshold is set to 300mV by R1. Operation of this device is described in the data sheet.

Power for the additional circuitry is derived from VCC of the LTC4370.

CONCLUSION

The LTC4370 is designed primarily as a current sharing, diode-OR controller for two redundant supplies. With a few additional components, it can be easily used in a non-redundant supply environment as a robust load sharing controller, where both of the supplies are necessary to support the entire load. The solution described here provides that function. ■

Simple, Fast Pulse Source Outpaces Expensive Lab Equipment

Mitchell Lee

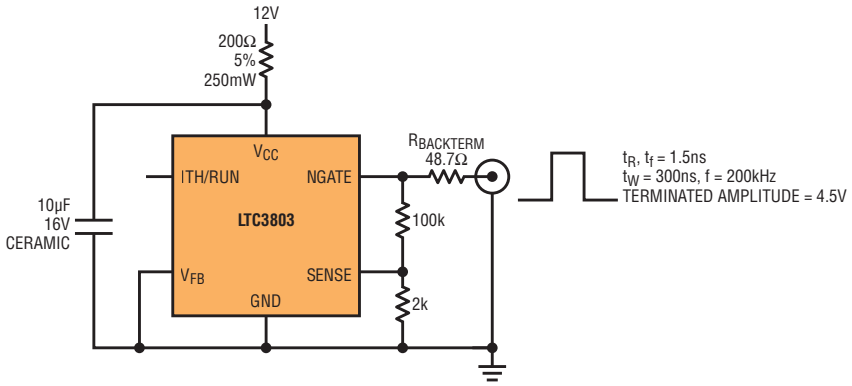
A source of fast pulse edges, simulating a step function, is often useful in making lab measurements of one kind or another. For example, it is possible to evaluate the rise time of RG-58/U or other coaxial cables using lengths of only 10 to 20 feet if an edge rate on the order of 1ns–2ns is available. The ubiquitous HP8012B pulse generator, a workhorse in many labs, falls short at 5ns, and is not quite fast enough for the task at hand. The gate drive output rise and fall times of certain switching regulator controllers are faster than 2ns, making such devices potentially ideal pulse sources.

Figure 1 shows a simple implementation using an LTC3803 constant frequency flyback controller. The controller self-clocks at 200kHz; applying a sample of the output to the SENSE pin causes the device to operate at its minimum duty cycle, producing a 300ns output pulse width. Supply bypassing is important, as the output delivers upwards of 180mA into a 50Ω load. The 10µF bypass and 200Ω decoupling components minimize pulse top aberration without compromising droop.

The output directly drives a 50Ω termination to nearly 9V. If pulse fidelity is of prime importance, back termination (as shown) is recommended to suppress triple transit echos by absorbing reflections from cabling and the far-end termination. Back termination is also useful when driving passive filters and other attenuators, which expect to see a specific generator impedance. The LTC3803 output impedance is about 1.5Ω, which should be borne in mind when choosing a back termination resistor. Back termination works well up to impedances of at least 2k, beyond which it is difficult to support the necessary bandwidth in the resistor and circuit connections, degrading pulse fidelity.

In a back-terminated 50Ω system the output characteristics are as follows: pulse amplitude 4.5V, symmetric rise and fall times of 1.5ns, pulse top aberration less than 10% and droop well under 5%. The rise and fall times are not degraded when directly driving 50Ω. For best pulse fidelity, connect the 10µF supply bypass capacitor as close as possible to the V_{CC} and GND pins of the LTC3803, and route the output directly to the back termination resistor and/or connector using stripline techniques. A 100-mil trace width on 1/16-inch, double-sided board approximates a 50Ω surge impedance. ■

Figure 1. Switching regulator controller produces 1.5ns edges into 50Ω



42V High Power Density Buck Regulators in a Tiny QFN Package

Ying Cheng

Power dissipation is a significant problem facing the designers of DC/DC converters in industrial and automotive applications, where high currents are required, but space is limited. It is possible to produce a highly efficient regulator from high performance discrete components, but expense and solution footprint make this approach prohibitive. The LT8612/LT8613 high efficiency buck regulators integrate all the necessary components into a single IC, significantly reducing the DC/DC converter size, even when faced with high step-down ratios. These devices can also be paralleled to increase the output current capability and spread the load and heat.

Other desirable features included in these regulators are ultralow quiescent current to maximize battery life, and high switching frequency to minimize solution size and avoid noise-sensitive frequency bands.

HIGHLY EFFICIENT 42V, 6A REGULATORS IN 3mm × 6mm PACKAGE

The LT8612/LT8613 are 42V, 6A step-down monolithic regulators. The low power dissipation of the integrated high efficiency power switches allows these switches, the boost diode, internal compensation and all necessary circuitry to be encapsulated in a tiny 3mm × 6mm QFN package without overheating. Figure 1 shows a typical 5V/30W LT8612 converter; its efficiency and power loss are demonstrated in Figure 2. Even with an input voltage of 24V, the LT8612 can produce a 30W output with no more than 50°C temperature rise. At the other end of the load spectrum, the LT8612/LT8613 uses low ripple Burst Mode® operation to enhance efficiency in ultralow load situations.

The minimum on-times of LT8612/LT8613 are as low as 40ns, allowing for high VIN/VOUT ratios even at high switching frequencies. High switching frequencies, up to 2.2MHz, minimize the size and value of the power inductor and output capacitor. Furthermore, the inductor can be confidently sized based on the output load requirement—no need to use a larger inductor to provide design overhead—a result of the devices' high speed peak-current mode architecture and robust switch design.

MULTIPHASE DESIGN TO INCREASE OUTPUT CURRENT CAPABILITY

Loads more than 6A are not uncommon in automotive and industrial applications. For these relatively high current conditions, a multiphase design can extend the output capabilities of the LT8612/LT8613 regulators. The LT8613 has a built-in rail-to-rail current sense amplifier with monitor and control pins, enabling accurate input or output average current regulation. This current loop modulates

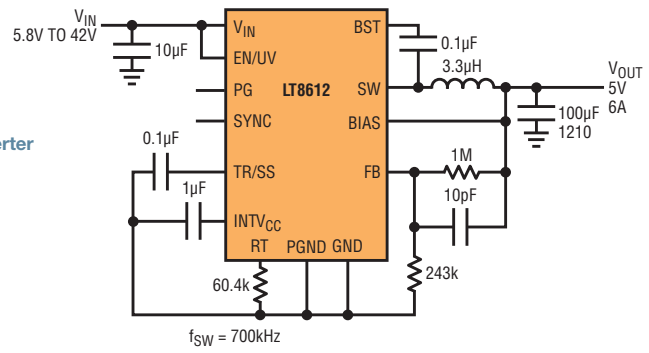
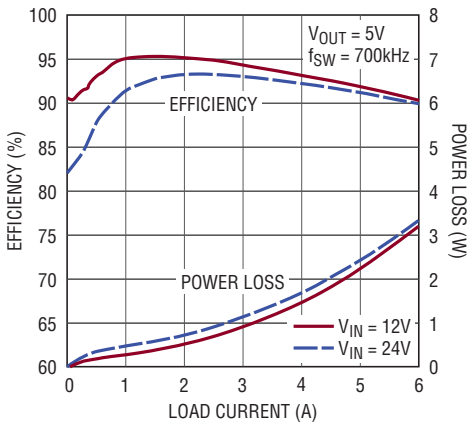


Figure 1. A 5V/30W step-down converter using the LT8612

Figure 2. Efficiency and power loss of the 5V/30W LT8612 step-down converter in Figure 1.



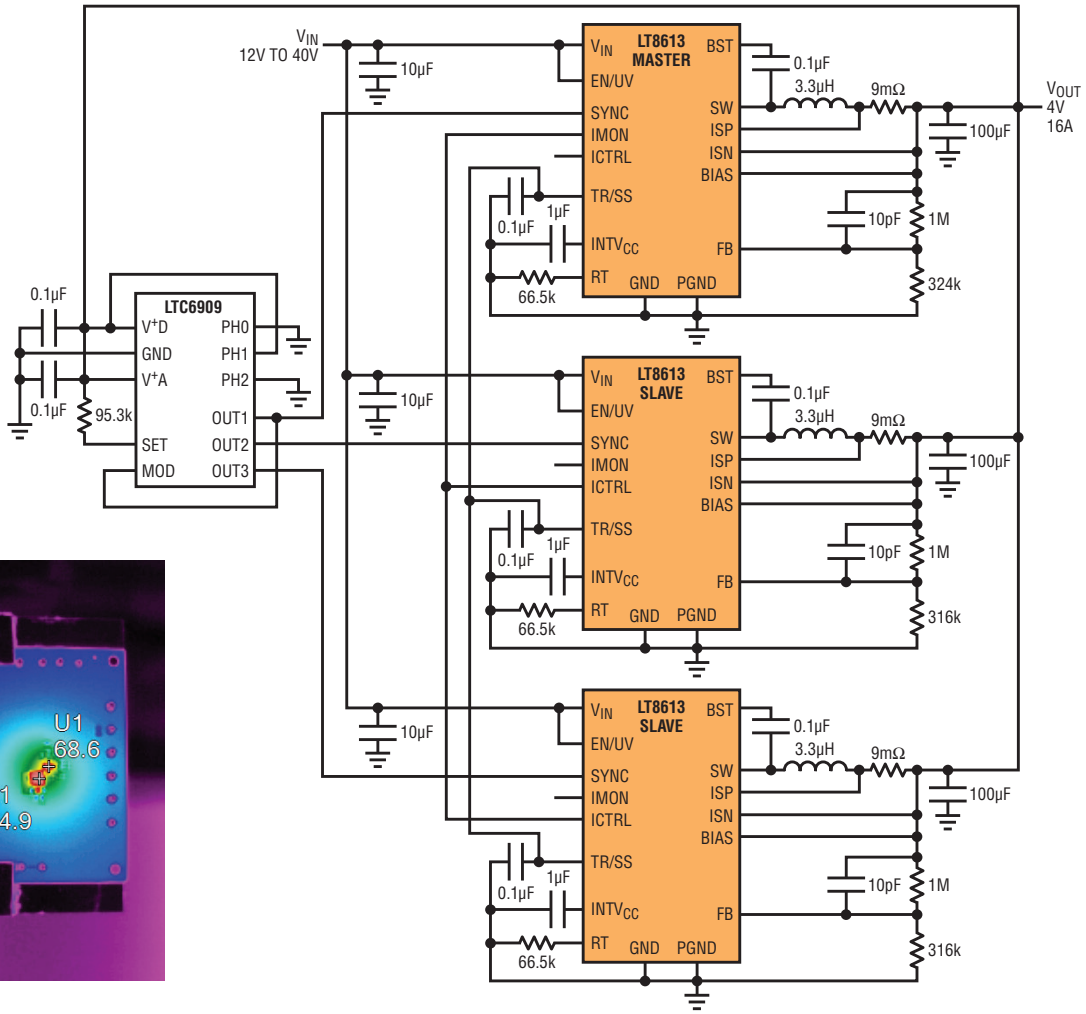
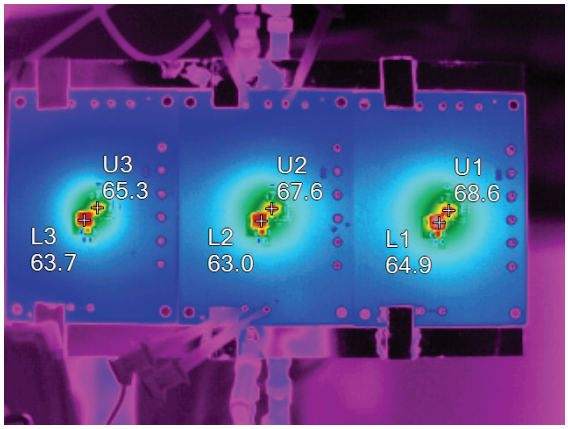


Figure 3.Three parallel LT8613s in a 3-phase design deliver 16A at 4V V_{OUT}

Figure 4. Thermal image of 3-phase LT8613 design shows balanced current sharing



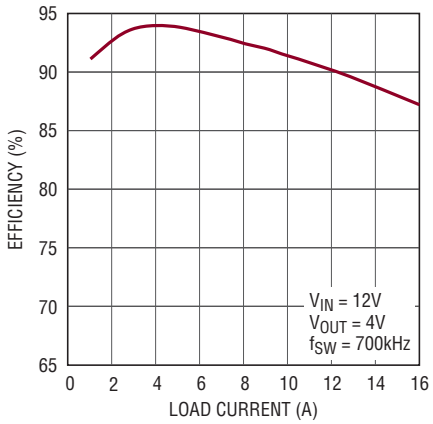


Figure 5. Typical efficiency of 3-phase LT8613 design shown in Figure 3

the internal switch current limit such that the voltage across the ISP/ISN pins does not exceed the voltage set by the ICTRL pin. Another IMON pin is used to monitor the average current that is measured through the ISP/ISN pins. This current control feature makes accurate current sharing among several LT8613s possible without any additional control circuitry.

Figure 3 shows three LT8613s paralleled for up to 16A output. The top LT8613 is the master regulator with its output voltage set to 4V, while the other two LT8613s are slave regulators with their output voltages set a little higher than 4V.

In order to share current among the three LT8613 regulators, the IMON pin of the master LT8613 is connected to the ICTRL pins of the slave LT8613s. The three LT8613 regulators are synchronized by the 3-phase 700kHz clock signals (120° phase shift) generated from the LTC6909 oscillator. Figure 4 shows a thermal image of this 3-phase LT8613 design.

The similarity in temperatures of the LT8613s indicates even current sharing among the three phases. The efficiency of this design is shown in Figure 5.

If it is desirable to weight the current sharing among the phases—that is to unbalance the current sharing—simply adjust the values of the sense resistors across ISP and ISN pins.

CONCLUSION

The LT8612 and LT8613 are fully integrated high power density monolithic step-down regulators that satisfy challenging automotive and industrial requirements. They can be easily paralleled for efficient, high current applications and compact solution footprints. ■

Measuring 18 2-Wire RTDs with the LTC2983 High Accuracy Digital Temperature Measurement System

Tom Domanski

The LTC2983 measures a wide variety of temperature sensors and digitally outputs the result, in °C or °F, with 0.1°C accuracy and 0.001°C resolution. It can measure the temperature of virtually all standard (type B, E, J, K, N, S, R, T) or custom thermocouples, automatically compensate for cold junction temperatures and linearize the results. The device can also measure temperature with standard 2-, 3-, or 4-wire RTDs, thermistors and diodes.

A single LTC2983 temperature measurement device can support up to 18 2-wire RTD probes, as shown in Figure 1. Each RTD measurement involves simultaneous sensing of two voltages developed across R_{SENSE} and the RTD probe RTDx due to the current I_S. Each voltage is sensed differentially, and given the LTC2983's high common mode rejection ratio, the number of RTDs in the stack does not adversely affect the individual measurements.

The choice of the RTD probe depends on the system accuracy and sensitivity requirements. For example, given that 2-wire probes are used, the PT-1000 may prove more robust in the presence of wiring's parasitic resistance.

Once the RTDs are selected, I_S and R_{SENSE} should be chosen so that voltage at the top of the resistor stack (V at the CH1 input) does not exceed the input common mode limit of the LTC2983 over the operating temperature range of the system. This requirement is expressed as:

$$V_{DD} - 0.3 \geq \left(R_{SENSE} + \sum_{i=1}^{N} RTD_i\right) I_S,\ N = 1,2 \ldots 18$$

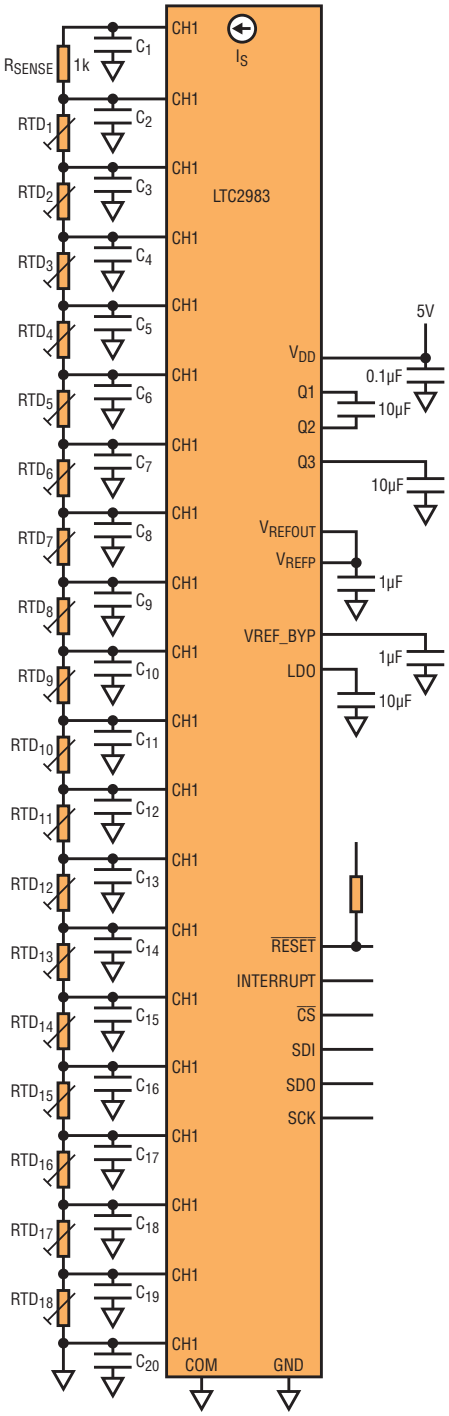
Consider the system shown in Figure 1 and assume the following constraints: 5V supply rail, all RTD probes are PT-100, and the maximum expected temperature measurement is at 150°C. Table 1 shows the channel assignment word for each one of the PT-100 probes. Consult the "Channel Assignment Memory Map" in the LTC2983 data sheet. Note that in this example, CH3 senses the RTD1 probe, CH4 senses RTD2, etc.

RTD STACK SETTLING TIME

Once the excitation current source is enabled, it takes a finite amount of time for the R and C chain to settle, t_S, where t_S is dependent on the number and value of the individual resistors (R_{SENSE} and RTDs) and capacitors at each input node. The upper bound on t_S can be estimated by lumping the total RC, but that yields an overly pessimistic result. Another method to obtain t_S is to simply simulate a circuit, as shown in Figure 2.

The results of simulation are shown in Figure 3. Here all capacitors are chosen to be 100nF, and R_{SENSE} is 1k. Each line represents settling time t_S to within 0.1% of the final value of the voltage

Figure 1. LTC2983 with 18 RTD sensors



The LTC2983 can interface to as many as 18 2-wire RTD probes, but be sure to take into account the settling delay incurred by RC systems. The issue may be exacerbated by the number and type of RTD probes used. The delay issues can be examined using the model and simulation presented here.

across last RTD in the stack. For each graph, all RTDs are of the same type.

The LTC2983, by default, inserts a delay time t_{DELAY} = 1ms between enabling the excitation source and the beginning of the ADC conversion. This, however, is insufficient for any more than two PT-100 probes in the RTD stack (see Figure 3).

The t_{DELAY} may be increased by setting the value in the MUX configuration register, 0x0FF. By default the register is cleared. Each LSB added to the register value represents 100µs added to default t_{DELAY}. Consult the "Supplemental Information" section in the data sheet for more detail on the MUX delay. For example, writing 0x10 into 0x0FF results in:

$$t_{DELAY} = 1ms + 0x10 \bullet 100\mu s = 2.6ms$$

Note that the maximum value of programmable delay is 26.5ms, which is sufficient for settling of at most six PT-1000 devices, given the C = 100nF. See Figures 3 and 4.

The t_{DELAY} is inserted prior to each individual ADC cycle. Each RTD measurement consists of two ADC cycles. Therefore the total conversion time of the stack of RTDs is approximately:

$$t_{TOTAL} = (2t_{DELAY} + t_{CONV})N$$

Where t_{DELAY} is programmable by the user, t_{CONV} is given in the "Complete System Electrical Characteristics" table in the data sheet, typically 164ms including the default MUX delay, and N is the number of RTDs to be measured. t_{TOTAL} is summarized in Figure 4.

Table 1. CH2 through CH20 RTD channel assignment word

FUNCTION		BIT FIELD	VALUE	DESCRIPTION
Sensor Type		31:27	01100	PT-100
Sense Resistor Channel Pointer		26:22	00010	CH2
Sensor Configuration		21:18	0001	2-Wire
Excitation Current		17:14	1000	1mA
RTD Curve		13:12	01	American Curve
Custom RTD Data Pointer	Address	11:6	000000	NA
	Length	5:0	000000	NA

The sense resistor, connected to CH2, is configured as shown in Table 2.

Table 2. Sense resistor channel assignment word

FUNCTION		BIT FIELD	VALUE	DESCRIPTION
Sensor Type		31:27	11101	Sense Resistor (29)
Sense Resistor Value	Integer	26:10	000000 1111101000	1kΩ
	Fraction	9:0	0000000000	

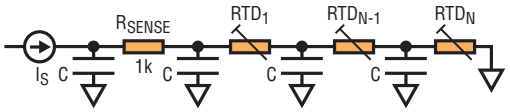


Figure 2. Delay line model of the RTD stack

CONCLUSION

The LTC2983 can interface to as many as 18 2-wire RTD probes, but be sure to take into account the settling delay incurred by RC systems. The issue may be exacerbated by the number and type of RTD probes used. The delay issues can be examined using the model and simulation presented here. ■

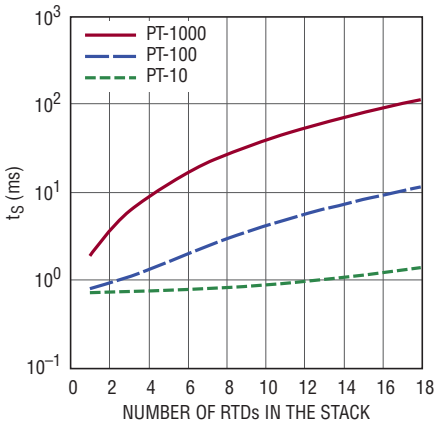


Figure 3. Simulated settling time of the RTD stack

Low Power, Precision Op Amp Simplifies Driving of MUXed ADCs

Guy Hoover

The high speed op amps required to buffer a modern 16-/18-bit analog-to-digital converter (ADC) typically dissipate as much power as the ADC itself, often with a maximum offset spec of about 1mV, well beyond that of the ADC. If multiple multichannel ADCs are required, the power dissipation can quickly rise to unacceptable levels.

The simple buffer presented here is capable of driving the LTC2372-18 8-channel ADC and achieving near data sheet SNR, THD and offset performance with very low power dissipation if the input signals involved are in the range of DC to 1kHz.

CIRCUIT DESCRIPTION

The LTC2372-18 is a low noise, 500ksps, 8-channel, 18-bit successive approximation register (SAR)ADC. Operating from a single 5V supply, the LTC2372-18 achieves –110dB THD (typical), 100dB (fully differential)/95dB (pseudo-differential) SNR (typical) with an offset of ±11LSB (maximum) while dissipating only 27mW (typical).

The LT6016 is a dual rail-to-rail input op amp with input offset voltage less than 50µV (maximum) that draws only 315µA per amplifier (typical). It is also available as a single and a quad (LT6015/LT6017).

The circuit of Figure 1 shows the LT6016 op amp configured as a noninverting buffer driving the analog inputs of the LTC2372-18. Typical power dissipation of each op amp is only 3.7mW. For all eight channels, this is a power dissipation of only 30mW, approximately the same power dissipation as the ADC. Running the LT6016 on a single 5.25V supply and enabling the ADC's digital gain compression mode reduces the total op amp power consumption by more than half, to 13mW, at the expense of a slight decrease in the SNR.

The RC filter at the buffer output minimizes the noise contribution of the LT6016 and reduces the effect of the sampling transient caused by the MUX and the input sampling capacitor.

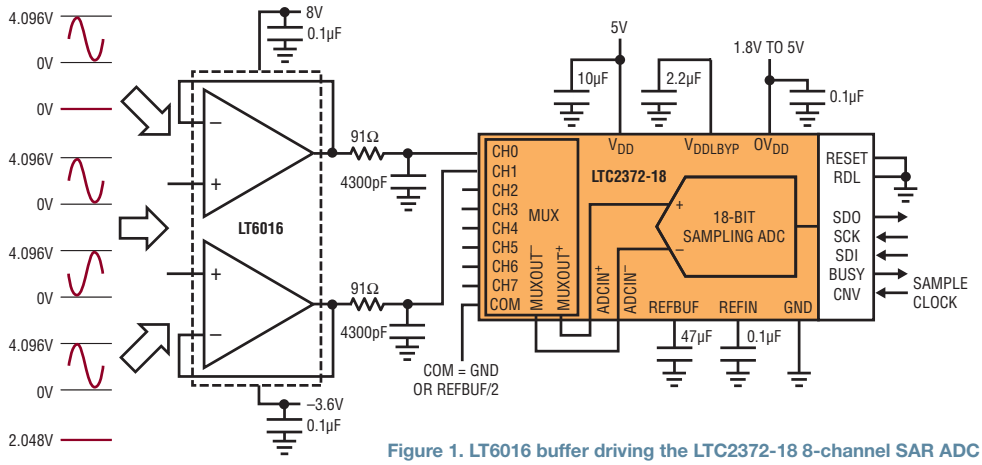


Figure 1. LT6016 buffer driving the LTC2372-18 8-channel SAR ADC

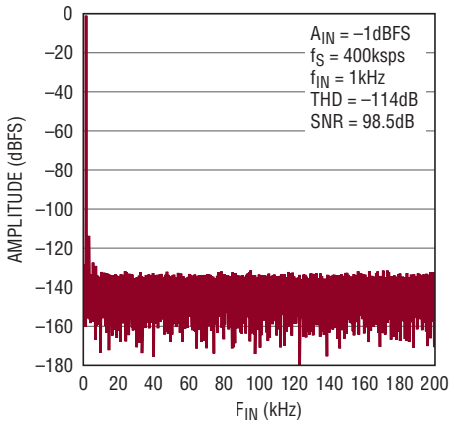


Figure 2. 32768-point FFT for the circuit of Figure 1

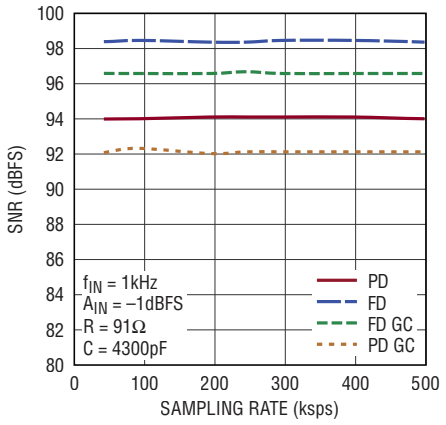


Figure 3. SNR vs sampling rate for the circuit of Figure 1 in pseudo-differential and fully differential modes

The simple buffer presented here is capable of driving the LTC2372-18 8-channel ADC and achieving near data sheet SNR, THD and offset performance with very low power dissipation if the input signals involved are in the range of DC to 1kHz.

CIRCUIT PERFORMANCE

Figure 2 shows a 32768-point FFT of the LTC2372-18 driven fully differentially by the circuit of Figure 1. THD is –114dB and SNR is 98.5dBFS at 400ksps, which compares well with the typical specs of the LTC2372-18.

Figure 3 shows SNR vs sampling rate with digital gain compression off and on for both pseudo-differential and fully differential modes of the LTC2372-18. With digital gain compression off, the supply voltage for the LT6016 is +8V/–3.6V. With digital gain compression on, the LT6016 runs off a single 5V supply. SNR stays fairly flat at 94dBFS (pseudo-diff)/98.5dBFS (fully diff) with digital gain compression off, and 92.1dBFS(pseudo-diff)/96.6dBFS(fully diff) with digital gain compression on, up to 500ksps for all modes.

Figure 4 shows THD vs sampling rate with digital gain compression off and on for both pseudo-differential and fully differential modes of the LTC2372-18. Here THD starts to rise above –110dB at 300ksps for pseudo-differential mode and rises above –115dB at 400ksps for fully differential mode. Digital gain compression has only a minimal effect on the THD performance. In fully differential mode, THD is never worse than –100dB up to the full 500ksps sampling rate of the LTC2372-18.

Figure 5 shows the combined offset error of the buffer and ADC vs sampling rate in pseudo-differential mode with digital gain compression off. Offset is initially less than 3LSB and does not degrade until the sampling rate reaches 400ksps.

Figure 6 shows distortion vs input frequency for a 400ksps sampling rate. Above 1kHz, distortion rises for all modes.

CONCLUSION

A simple driver for the LTC2372-18 18-bit, 500ksps, 8-channel SAR ADC—consisting of the LT6016 low power precision dual op amp configured as noninverting buffer is demonstrated. The driver dissipates only 3.7mW per op amp (typical), and can be reduced to 1.6mW by running off a single 5V supply with the ADC in digital gain compression mode.

At sampling rates less than 300ksps, SNR is measured at 94dB (pseudo-diff)/98.5dB (fully diff) with gain compression off and 92.1dBFS (pseudo-diff)/96.6dBFS(fully diff) with digital gain compression on; THD is measured at –110dB (pseudo-diff)/–115dB (fully diff) with digital gain compression off or on. Offset measures less than 3LSB (pseudo-diff) with gain compression off. Above 300ksps, performance gradually declines up to the full 500ksps sampling rate of the LTC2372-18. ■

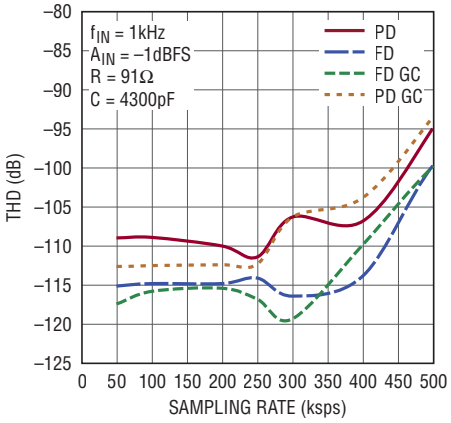


Figure 4. Pseudo-differential, fully differential THD vs sampling rate for the circuit of Figure 1 with and without gain compression

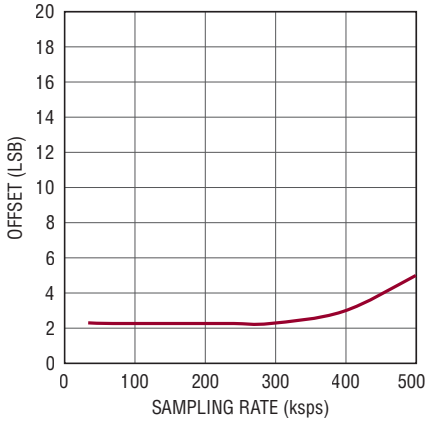


Figure 5. Offset error vs sampling rate for the circuit of Figure 1 in pseudo-differential mode

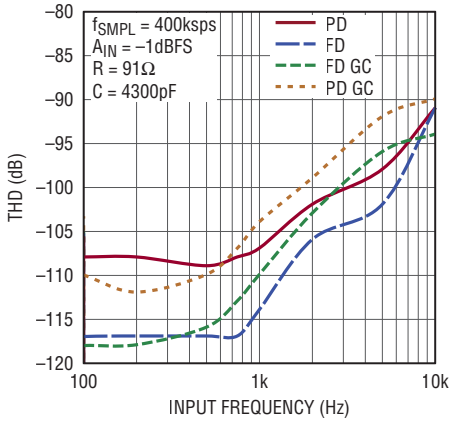


Figure 6. Distortion vs input frequency for the circuit of Figure 1

Avoid Debugging Cycles in Power Management for FPGA, GPU and ASIC Systems

Afshin Odabaee

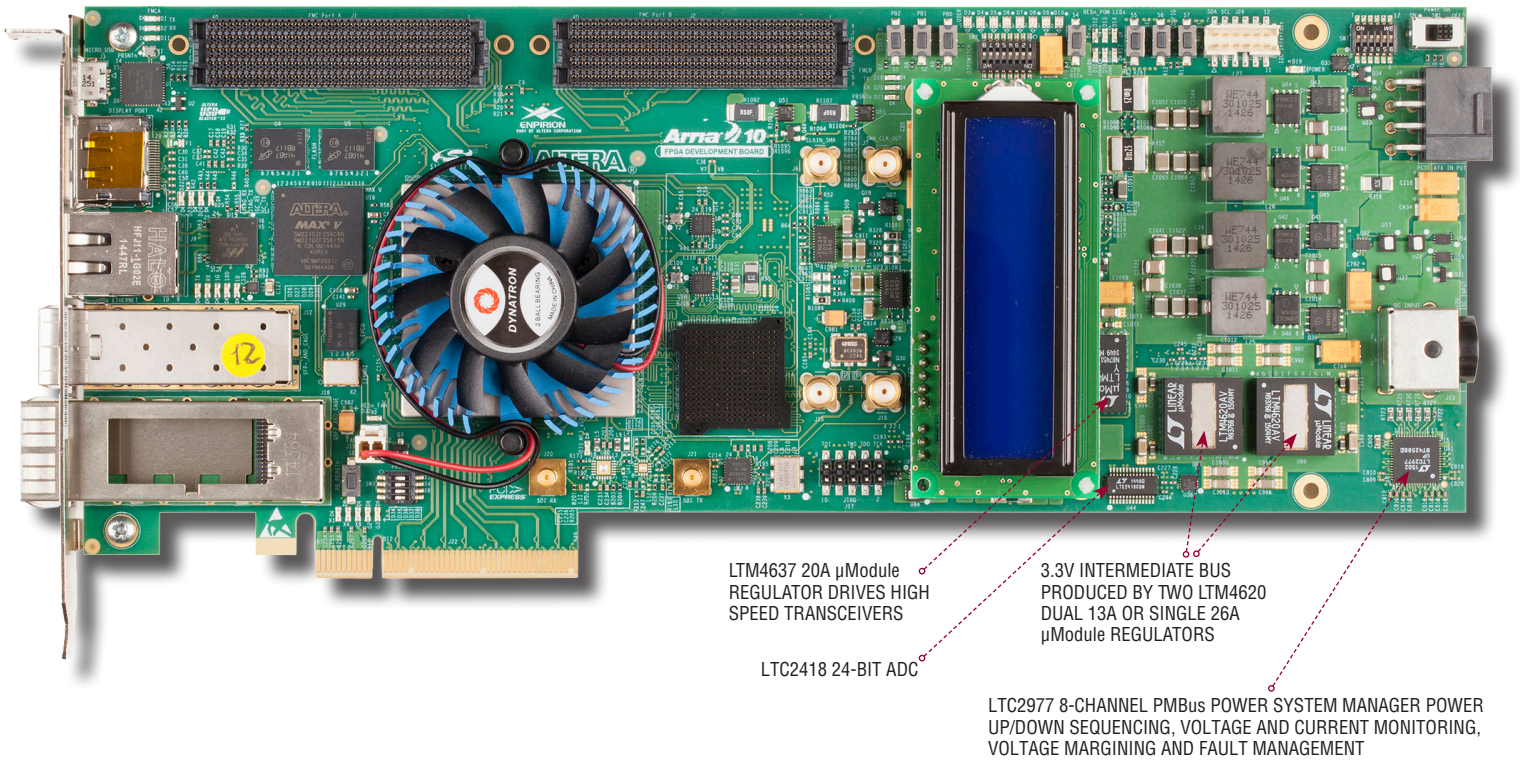
When it comes to designing FPGA, GPU or ASIC controlled systems, the number of design challenges related to power management and analog systems pale in comparison to those related to digital design. Nevertheless, it is risky to assume that power system design can be left to "later," or taken in line with digital design. Even seemingly innocuous problems in power supply design can significantly delay the release of a system, as any added time to the power system debugging cycle can halt all work on the digital side.

A good way to put DC/DC regulation issues to rest is to use a verified development kit offered by the FPGA, GPU or ASIC vendor. Often, the design itself or a similar design is available as a board/kit by the suppliers of power products and FPGA, GPU and ASIC manufacturers. Using a tested and verified kit unburdens system designers of most power system and analog issues, allowing them instead to focus their energies on configuring the complex digital systems. The optimum power system layout is taken care of before significant design is undertaken.

THOUGHTFUL POWER MANAGEMENT IS CHALLENGING AT THE START

Every design task is initially daunting, and power management design is no exception. This is the case when power is required in a complex system incorporating transceivers, memory modules, sensors,

Figure 1. Arria 10 GX FPGA development kit board. All functions for power panagment and interfacing to LTpowerPlanner® (graphical softwared control) are included on the board and factory tested and verified. System debugging is minimized and performance testing (including margining) is simplified. See Table 1 for a summary of included power management components.



Using a tested and verified kit unburdens system designers of most power system and analog issues, allowing them instead to focus their energies on configuring the complex digital systems. The power system is left to experts in power design and board layout.

Table 1. Power management bill-of-materials for the Arria 10 GX FPGA development kit shown in Figure 1

RAIL/FUNCTION	PART NUMBER	DESCRIPTION
FPGA Core Power	LTC3877 + LTC3874	105A at 0.9V Regulator Seamlessly Interfaces with Arria 10 SmartVID
High Speed Transceivers	LTM4637	20A µModule Regulator
Power UP/DOWN Sequencing, Voltage And Current Monitoring, Voltage Margining And Fault Management	LTC2977	8-Channel PMBus Power System Manager
PowerPath™ Management	LTC4357	High Voltage Ideal Diode Controller
3.3V Intermediate Bus from 12V V_{IN}	LTM4620	Dual 13A or Single 26A µModule Regulator
Input Overvoltage Protection	LTC4365	Overvoltage, Undervoltage and Reverse Supply Protection Controller
Housekeeping System Power and Power Management	LT1965, LT3082, LTC4352, LTC3025-1, LTC2418	Low Noise Linear Regulators, 24-Bit ADC; Low Voltage Ideal Diode

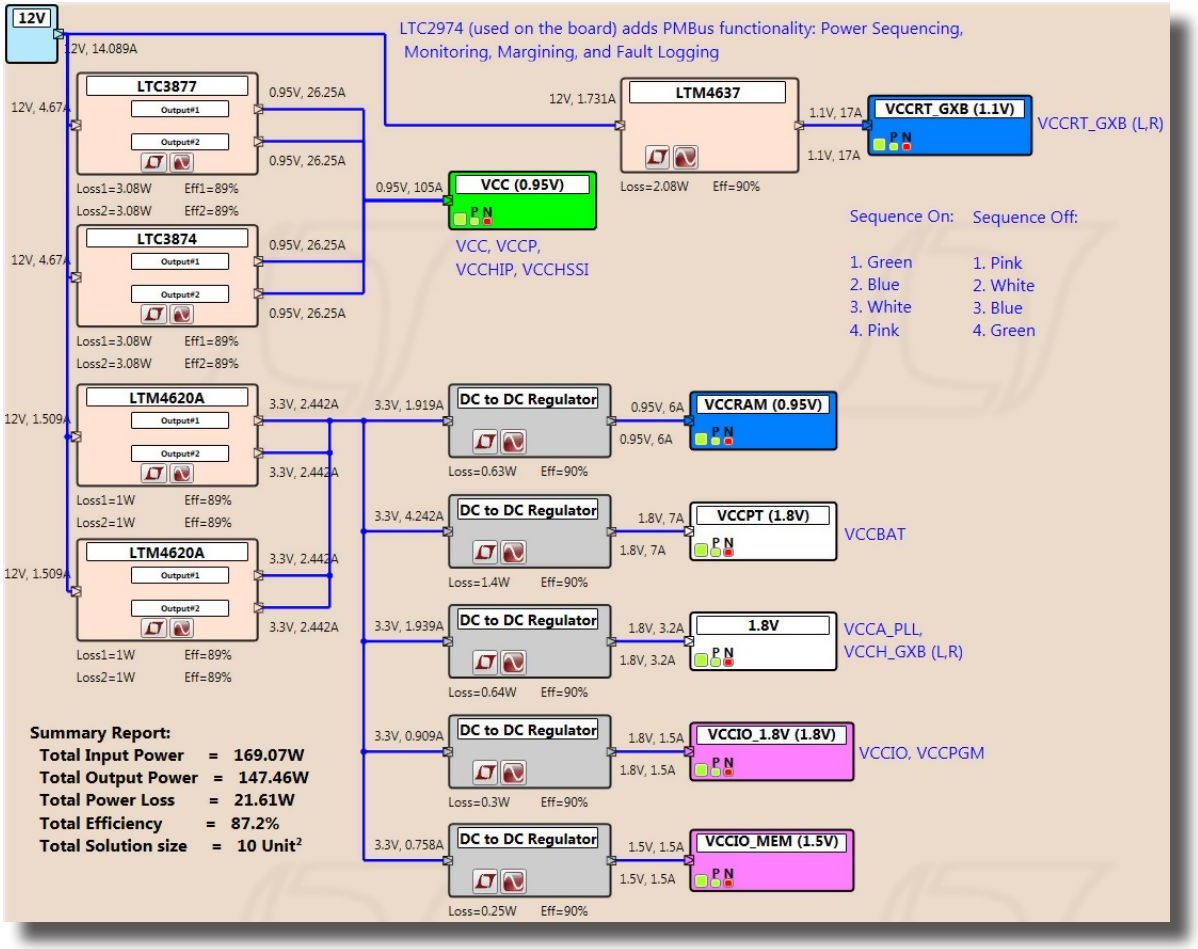


Figure 2. Power tree for Arria 10 GX FPGA board (Figure 1). Designed in LTpowerPlanner, an analytical and simple first step design tool for mapping power requirements.

The power management solution for high end FPGAs, including the Arria 10, should be carefully selected. A well thought out power management design can reduce PCB size, weight and complexity, as well as minimize power consumption and cooling costs. This is essential to achieve optimal system performance.

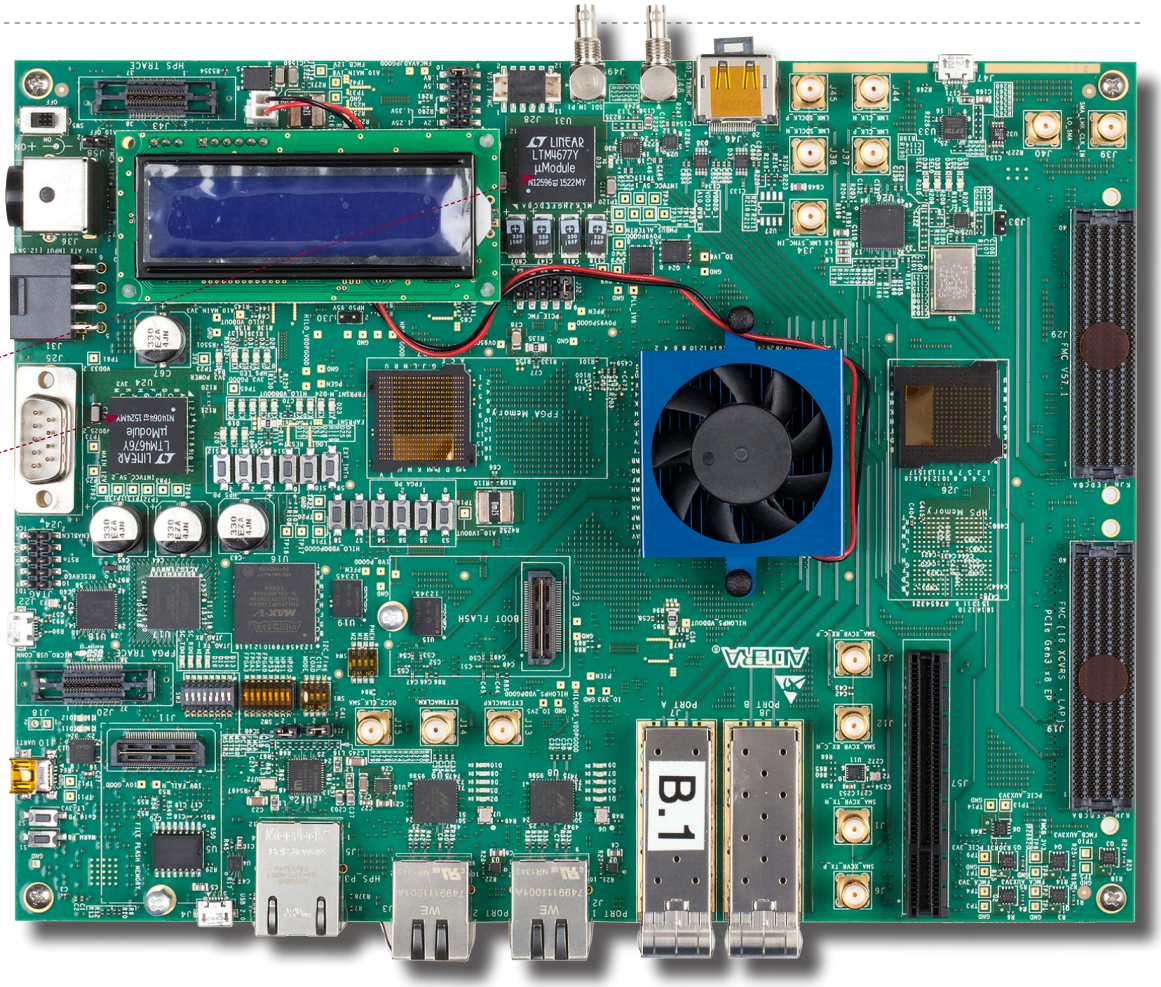


Figure 3. Arria 10 SoC development kit board

line connectors and mesh of PCB traces and layers of PCB planes. Haphazardly addressing system power management with numerous DC/DC regulators, capacitors, inductors, heat removal and heat sinks and layout of components can lead to downstream design problems. Simply throwing in a DC/DC regulator with the right input/output requirements will at some point inhibit progress, and lead to time-intensive debugging procedures.

WHERE TO BEGIN POWER MANAGEMENT

Just as with digital design and coding, power management design should be approached systematically. Careful analysis and is accurate modeling of power management system should be undertaken before PCB assembly. A power management guide is already tested and verified to meet the requirements of the FPGAs, ASICs, GPUs and microprocessors and the systems that use these and other digital components. Mapping a power system with proven power management solutions ensures that the project is initiated with high confidence. This is key to quickly turn a design from its prototyping stage to production—spending less time on debugging power.

CASE STUDY: POWERING THE ARRIA 10 FPGA AND ARRIA 10 SoC

As noted above, FPGA development kits enable system developers to evaluate an FPGA without having to design a complete system from scratch. Figures 1 and 2 show Altera's new 20nm Arria 10 FPGAs and Arria 10 SoCs (system-on-chip)

Mapping a power system with proven power management solutions ensures that the project is initiated with high confidence. This is key to quickly turn a design from its prototyping stage to production—spending less time on debugging power.

Table 2. Power management bill-of-materials for the arria Arria 10 SoC development kit board shown in Figure 3

RAIL / FUNCTION	PART NUMBER	GENERAL DESCRIPTION OF PART
0.9V: V_{CC} (FPGA Core Power)	LTM4677	Dual 18A or Single 36A µModule Regulator with Digital Power System Management
3.3V: System Power	LTM4676	Dual 13A or Single 26A µModule Regulator with Digital Power System Management
1.2V: AVDD_PLL	LTC3026-1	1.5A Low Input Voltage VLDO™ Linear Regulator
1.0V: ENET_DVDD	LTC3025-1	500mA Micropower VLDO Linear Regulators
1.8V: USB_FPGA	LT3010	50mA, 3V to 80V Low Dropout Micropower Linear Regulator
Voltage Monitor and Control	LTC2977	8-Channel PMBus Power System Manager Featuring Accurate Output Voltage Measurement
16-Bit ADC for Analog Input	LTC2497	16-Bit 8-/16-Channel Delta Sigma ADC with Easy Drive™ Input Current Cancellation and I^2C Interface
1.25V Voltage Reference	LT1389	Nanopower Precision Shunt Voltage Reference

development boards. These boards are tested and verified by Altera, exemplifying best design practices in layout, signal integrity and power management.

Power Management for Core, System and I/O.

The power management solution for high end FPGAs, including the Arria 10, should be carefully selected. A well thought out power management design can reduce PCB size, weight and complexity, as well as minimize power consumption and cooling costs. This is essential to achieve optimal system performance.

For example, the 0.95V at 105A, supplied by the 12V DC/DC regulator powering the core of the Arria 10 GX FPGA in Figure 1, has several features that complement the power saving schemes of the SoC:

- The DC/DC regulator's integrated 6-bit parallel VID interface is used by the Arria 10's SmartVID to control the DC/DC regulator and reduce FPGA power consumption during static and dynamic states.
- The DC/DC regulator's very low value DCR current sensing improves efficiency by minimizing power loss in the inductor. Temperature compensation maintains the accuracy or the DCR value at higher inductor temperature.

Table 1 summarizes the Arria 10 development kit's power rails and functions as shown in Figure 1. The table lists the parts and descriptions for each function. Visit www.linear.com/altera and click on Arria and access technical details for the two boards presented here.

Customize the Power Tree with the LTpowerPlanner Design Tool

What if your power requirements differ from the designs exemplified in a development kit? In these cases, use the LTpowerPlanner® PC-based design tool to personalize and optimize a system's power tree.

Start with the suggestions given in the development kit; then reorganize power blocks, alter power ratings, compute efficiency and power loss, simulate each power block, select DC/DC regulator part numbers and authenticate a customized solution.

LTpowerPlanner was used to generate the power trees (Figure 3) for the Arria 10 development kit's FPGA and system requirements, and is available within the more encompassing LTpowerCAD®

Start your power management layout with confidence. Tools such as LTpowerCAD and LTpowerPlanner simplify the task of mapping point-of-load regulators and anlalyzing overall performance before any digital system design is undertaken.

design tool, available for free download at www.linear.com/ltpowercad.

LTpowerCAD enables users to:

- Select specific Linear Technology DC/DC regulators to match a given power specification
- Select appropriate power components such as inductors, resistors and capacitors
- Optimize efficiency and power loss
- Optimize regulator loop stability, output impedance and load transient response
- Export the design to LTspice®

CONCLUSION

Start your power management layout with confidence. Tools such as LTpowerCAD and LTpowerPlanner simplify the tasks of mapping point-of-load regulators and analyzing overall performance. The examples shown here specifically outline the benefits of using development kit design guides for Altera Arria 10 FPGAs and SoCs. These are available at www.linear.com/altera. For Xilinx-based FPGA development kits, refer to www.linear.com/xilinx. Available development kits have been tested and verified by Altera, Xilinx or other developers. ■

Contributors
Sharad Khanal, Gerard Velcelean, Guneet Chadha and Masa Iwasaki

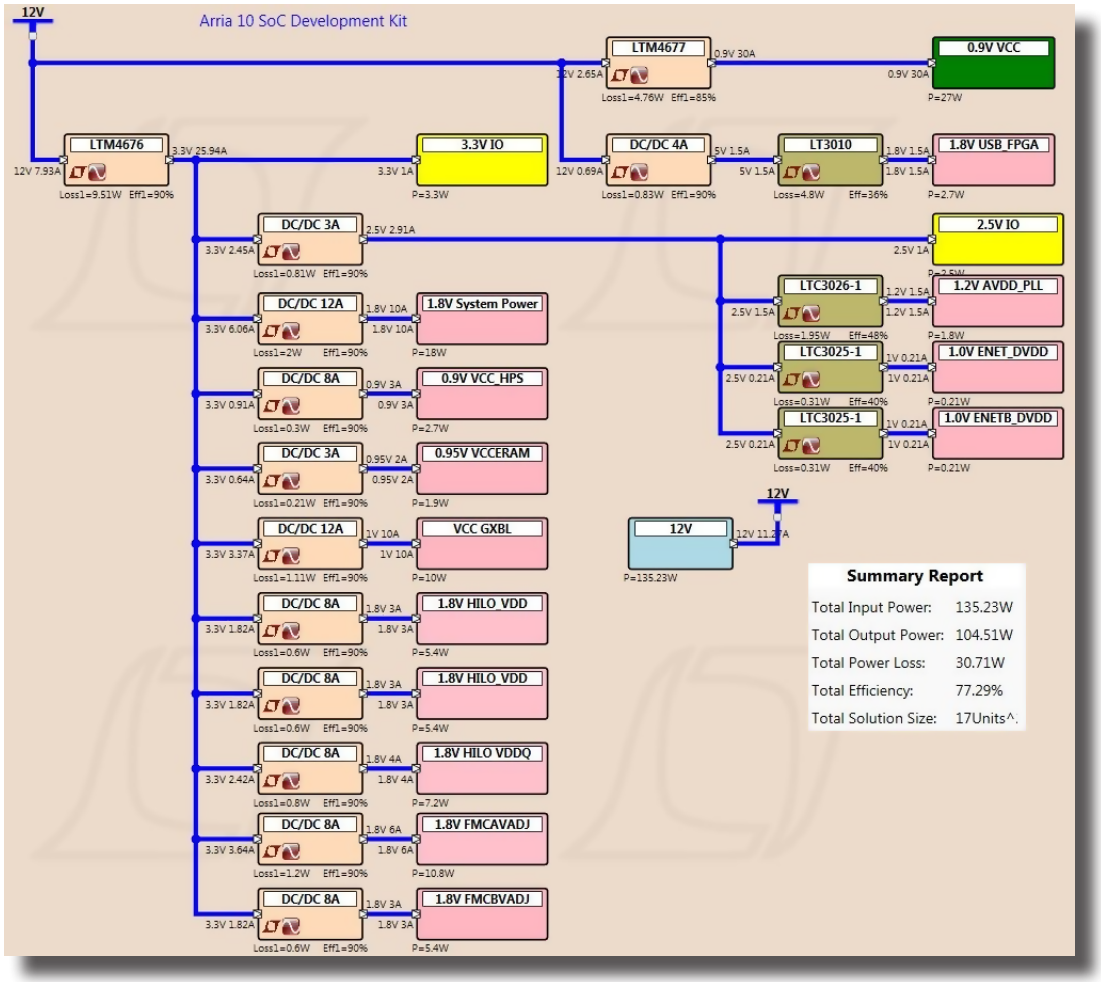


Figure 4. Power tree for Arria 10 SoC development kit board (Figure 3).

New Product Briefs

60V, 4A SYNCHRONOUS STEP-DOWN REGULATOR FOR INVERTING OUTPUTS

The LTC7149 is a high efficiency, 60V, 4A synchronous buck regulator for negative output voltage supplies. It incorporates a current mode architecture with user-selectable internal or external loop compensation and an output voltage that is programmed with a single external resistor. The LTC7149 operates from an input voltage range of 3.4V to 60V and provides an adjustable output voltage from 0V to –28V, while delivering up to 4A of continuous output current. Its wide input and output voltage ranges make it ideal for a wide range of test, measurement and industrial applications. The LTC7149's unique design includes an accurate internally generated 50µA current source on the ISET pin that enables it to deliver outputs as low as –28V with the use of a single external programming resistor. Furthermore, the LTC7149 offers ±0.8% output voltage accuracy. Its switching frequency is user-programmable from 300kHz to 3MHz, enabling the use of tiny, low cost capacitors and inductors. Combined with a 28-lead 4mm × 5mm QFN or thermally enhanced TSSOP package, it offers a very compact solution footprint.

The LTC7149 uses internal switches with $R_{DS(ON)}$ of only 110mΩ and 50mΩ to deliver efficiencies as high as 92%. Burst Mode® operation offers high efficiency at light loads, requiring only 440µA of quiescent current. For noise-sensitive applications, the LTC7149 can run in forced continuous mode, offering very low output ripple. It also includes ground-referenced clock and PGOOD pins, eliminating the need for level shifters. Additional features include a power good voltage monitor, programmable wire drop compensation, external synchronization capability and thermal protection.

The LTC7149EUFD is available in a 4mm x 5mm QFN-28, and the LTC7149EFE is offered in a 28-lead, thermally enhanced TSSOP package. Industrial grade versions, the LTC7149IUFD and LTC7149IFE, are guaranteed to operate over the –40°C to 125°C operating junction temperature range.

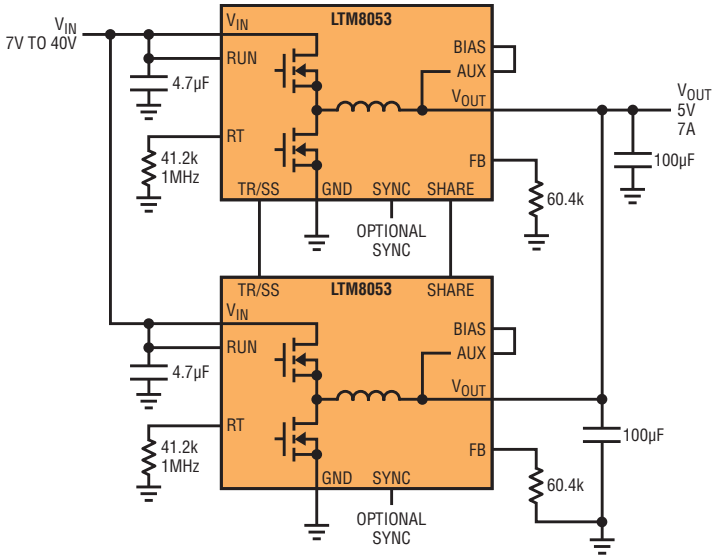
45V 500mA LDO OFFERS LOW 25µV_{RMS} NOISE, 60DB PSRR AT 1MHz AND ACTIVE OUTPUT DISCHARGE FOR LOAD PROTECTION

The LT3066 is a high voltage, low noise, low dropout voltage linear regulator offering precision, programmable current limit, active discharge, a power good flag and improved power supply rejection ratio (PSRR) capability. The device delivers up to 500mA output current with a 300mV dropout voltage at full load. The LT3066 includes an internal NMOS pull-down that discharges the output voltage if either the SHDN pin is driven low or the input voltage is turned off. This rapid active output discharge helps protect the load in applications requiring power conditioning on both start-up and shut-down, such as high end imaging sensors.

The LT3066 features a wide 1.8V to 45V input voltage range and output voltage is adjustable from 0.6V to 19V. A single REF/BYP pin capacitor provides low noise operation of only 25µV_{RMS} across a 10Hz to 100kHz bandwidth, and also reference soft-start functionality, preventing output voltage overshoot at turn-on. Output voltage tolerance is highly accurate at ±2% over line, load and temperature. An additional single INFILT pin capacitor improves PSRR by 15dB to 20dB for frequencies from 20kHz to 1MHz, with 1MHz PSRR reaching 60dB.

The LT3066 operates with a very small, low cost, 3.3µF ceramic output capacitor, optimizing stability and transient response. The device's PWRGD flag indicates output regulation. One resistor programs the external precision current limit (±10% over temperature). Moreover, the device's internal protection circuitry includes reverse-battery protection, reverse-current protection, current limit with foldback, and thermal limiting. The device's wide input and output voltage ranges, fast transient response, low quiescent current of 64µA (operating) and <2µA (in shutdown) make it an excellent choice for industrial power supplies, avionic power supplies, automotive power supplies, battery-powered systems and instruments requiring optimum run time, and high reliability power supplies requiring more extensive protection.

The LT3066 is available in thermally enhanced 12-lead 3mm x 4mm DFN and 12-lead MSOP packages, both with a compact footprint. ■



PIN NOT USED IN THIS CIRCUIT: PG

USING TWO PARALLEL LTM8053 µModule REGULATORS TO INCREASE LOAD CAPABILITY: 7V–40V INPUT TO 5V OUTPUT AT 7A

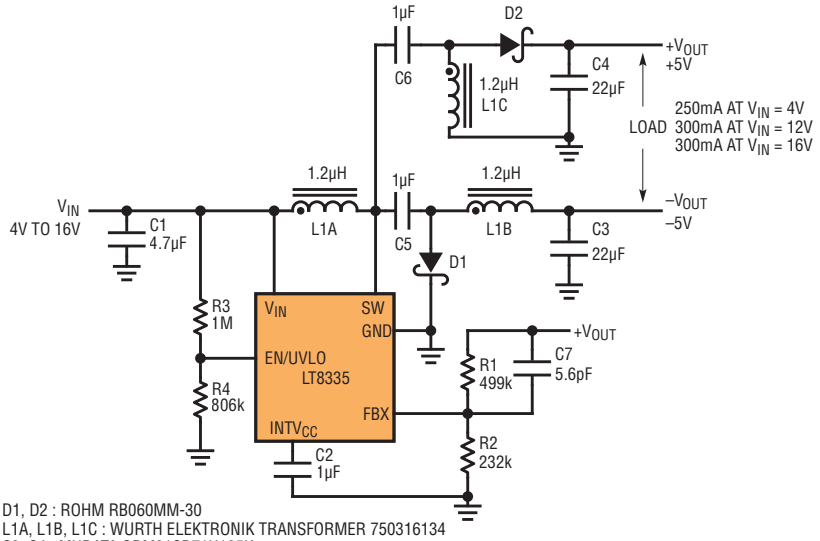
The LTM8053 is a 40V V_{in}, 3.5A (continuous) step-down µModule (power module) regulator. Included in the package are the switching controller, power switches, inductor, and all support components. Operating over an input voltage range of 3.4V to 40V, the LTM8053 supports an output voltage range of 0.97V to 15V and a switching frequency range of 200kHz to 3MHz, each set by a single resistor. Only the input and output filter capacitors are required to finish the design.

http://www.linear.com/solutions/7330

LT8335 3V TO 6V INPUT, 24V BOOST CONVERTER

The LT8335 is a current mode DC/DC converter capable of generating either positive or negative output voltages using a single feedback pin. It can be configured as a boost, SEPIC or inverting converter consuming as low as 6µA of quiescent current. Low ripple Burst Mode operation maintains high efficiency down to very low output currents while keeping the output ripple below 15mV in a typical application. The internally compensated current mode architecture results in stable operation over a wide range of input and output voltages. Integrated soft-start and frequency foldback functions are included to control inductor current during start-up. The 2MHz operation, combined with the small 8-lead DFN package, enables low cost, area efficient solutions.

http://www.linear.com/solutions/7345



D1, D2 : ROHM RB060MM-30
L1A, L1B, L1C : WURTH ELEKTRONIK TRANSFORMER 750316134
C3, C4 : MURATA GRM31CR71H105K

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