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New LTC1435–LTC1439 DC/DC Controllers Feature Value and Performance

by Randy Flatness, Steve Hobrecht and Milton Wilcox

Introduction

The new LTC1435–LTC1439 multiple-output DC/DC controllers bring unprecedented levels of value to supplies for notebook computers and other battery-powered equipment, while eliminating previous performance barriers. For example, a new Adaptive Power™ output stage allows two previously incompatible parameters, constant frequency operation and good low current efficiency, to coexist in the same power supply. A second breakthrough allows N-channel power MOSFETs to be used exclusively, while maintaining low dropout operation previously available only with P-channel MOSFETs. Other innovations include an auxiliary linear regulator loop, a phase-locked loop (PLL) to synchronize the oscillator to an external source, a self-contained power-on-reset (POR) timer and programmable run delays useful for staging output voltages.

Excellent system functionality means that 1-, 2-, 3- or even 4-output power supplies are easily constructed using a minimum number of inductors. Table 1 illustrates a few of the many possible output combinations and the magnetics required.

For maximum flexibility, internal resistive feedback dividers are selectable via programming pins for 3.3V, 5V and 12V output voltages, or a regulator may be configured with an adjustable output voltage to meet any processor requirement.

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Table1. Examples of possible output voltage combinations

Part Number	Package	Output Voltages	Magnetics*
LTC1435	16-pin SO	Adjustable 1.5V–9V	(1) L
LTC1436	24-pin QSOP	3.3V/2.9V	(1) L
LTC1437	28-pin SSOP	5V/12V	(1) T
LTC1438	28-pin SSOP	5V/3.3V	(2) L
LTC1439	36-pin SSOP	5V/3.3V/2.9V	(2) L
		5V/3.3V/2.9V/12V	(1) L, (1) T

*L = Inductor, T = Transformer

On Breadboarding

by Richard Markell

New integrated circuits don't come easy these days. Marketeers would have you build a new Pentium® Pro class microprocessor in a few months. Never mind the half-million transistors that all have to work correctly for the product to come out right the first time.

Simulation may be the way to go when faced with one-half million transistors and a year's time to market, but what about in the analog world where LTC excels? No analog product in this or perhaps even the next century will have one-tenth the transistor count of a microprocessor. The semiconductor world has come to rely heavily on simulations; and, in fact, we at LTC do our share of simulations; but, as the photo shows, we also do our share of breadboarding.

It may be that the mere mention of breadboarding shows my age. What could be simpler than building a circuit from discrete transistors, diodes, resistors, chewing gum and piano wire? Once built, the circuit can be tested node by node, and after the design is proven to work over its required electrical and environmental parameters, it can be put into production.

In the IC design world, the simulation is king because breadboarding is hard. Transistors don't come out of a catalog; instead they are "kit parts"—the types of transistors that can be made on a particular wafer-fab process. All capacitors must be small values, since only these are supported by the IC process; and so forth and so on. The implementation is not easy, but the reward justifies the labors. What is the reward?

The reward is an IC that works the first time—or at least the second time. Breadboarding makes you look at the circuit from a system point of view. Can it be integrated into the system in which it is intended to work? Are all the hooks there? Breadboarding is not always an option because of the increased complexity of today's ICs, but we try to use it whenever we can to complement simulation. Breadboarding helps us get it right "the first time."

This issue of *Linear Technology* begins our sixth year of publication. We have expanded our publishing schedule to four times per year. We continue to ask for feedback from our readership. Call, FAX or write to us at the numbers on the back page.

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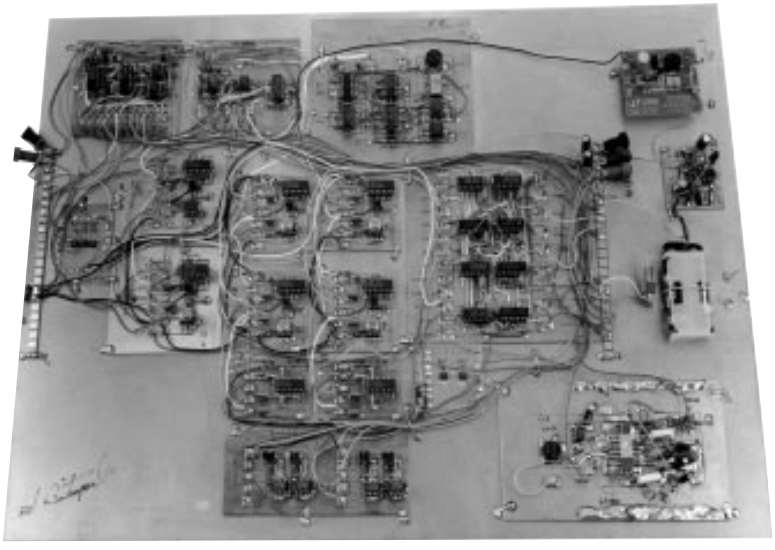

Figure 1. Breadboard of upcoming LTC microprocessor product?

LTC in the News...

The only company in the history of Silicon Valley to achieve continuous sales growth over 40 consecutive quarters is Linear Technology Corp. In January, LTC announced record second-quarter net sales of more than $96 million, an increase of 55% over the same quarter of 1995.

"This solid 10-year record validates both the strength of our market and the effectiveness of our strategy to be a broad-based supplier of high performance analog circuits," said Robert Swanson, president and CEO. "We attained record levels of sales and profits and generated an additional $20 million in cash," he said.

Shortly before LTC ended its second fiscal quarter, *Forbes* magazine again listed the company on its "Honor Roll" of "The Best Small Companies in America." It was the sixth year in a row in which Linear Technology was included among "only a handful of companies (that) have what it takes to be a long-term repeater on our 200 Best Small Companies in America list." The magazine made special mention of LTC and observed that a $10,000 investment in Linear six years ago would be worth about $170,000 today.

"All chip companies are not created equal," said the influential *Cabot Market Letter* for investors in its December 1, 1995, issue. "Linear Technology is ... the leader in its market. (The company's) chips don't deal with data. They interact with the real world to monitor, amplify or transform continuous analog signals associated with real-world phenomena like temperature, pressure, weight, position, height, speed or sound.

"That's diversity in the extreme. In fact, LTC markets over 4,700 different products to over 9,000 manufacturers worldwide. Industrial applications use 40% of the firm's output, computers 30%, telecommunications 15%, military 10% and other 5%. International sales account for about half of the total." LT

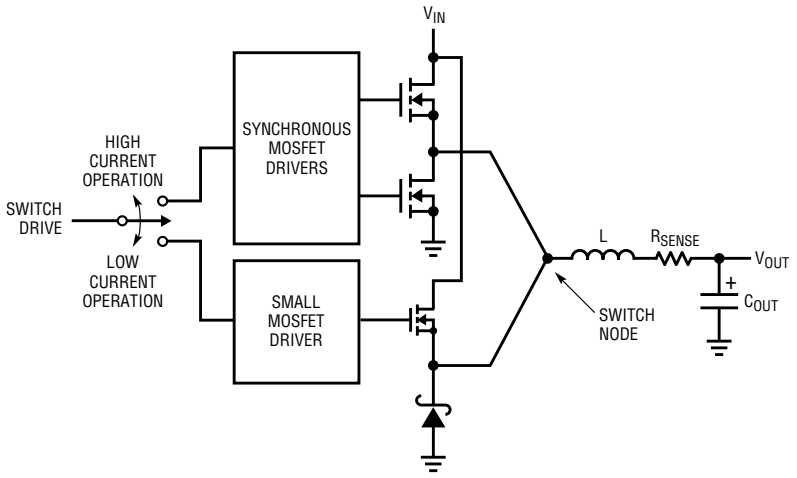

Figure 1. Adaptive Power output stage automatically switches to efficiency-saving small MOSFET at low currents, while continuing to operate at a constant frequency.

LTC1435–LTC1439, continued from page 1

A Brief History of High Efficiency DC/DC Conversion

The 90% efficiency barrier was demolished several years ago, at least at high output currents, by DC/DC controllers adapted to drive external synchronous power MOSFETs, which largely eliminated the catch-diode losses. However, the efficiency of these converters plummeted when the output current dropped, because the fixed-gate-charge losses for the large MOSFETs became an increasing percentage of the power delivered to the load. Expressed differently, the quiescent (unloaded) current was unacceptably high—often over 10mA.

Linear Technology's LTC1148 family of DC/DC controllers introduced in late 1992 was the first in the industry to extend high efficiency operation over the entire load range required by notebook computers and other portable electronics. This breakthrough was achieved through Burst Mode™ operation, which turns *both* synchronous MOSFETs off for increasing periods as the load current drops. In this way, the gate charge losses are made proportional to the load current, thus maintaining high efficiency. Along with the gate-charge savings came an attendant reduction in quiescent current, to less than 200µA for the LTC1148.

Burst Mode operation received immediate acceptance and is in use today in a wide range of battery-powered electronics. However, the approach of intermittently operating large power MOSFETs at low output currents carries one drawback: the operating frequency must inherently be variable, and will enter the audio range at some currents. This drawback, while not a problem in many applications, is becoming an increasing concern as communications and multimedia features are added to portable computers.

The LTC143X family controllers use a constant frequency, current mode PWM architecture in which the user can set the oscillator frequency from 50kHz to 400kHz via an external capacitor. But how to break through the constant frequency/low current efficiency barrier?

Adaptive Power Mode—Constant Frequency without the Efficiency Hit

Adaptive Power mode, available in all family members except the LTC1435 and LTC1438, optimizes efficiency without changing frequency by automatically switching between the two output stages shown in Figure 1. The first stage uses large synchronous N-channel MOSFETs when operating at high currents, and the second uses a small (0.5Ω) N-channel MOSFET and Schottky diode when operating at low currents. The transition point between the two output stages scales with the maximum current, which is set by the current sense resistor for each regulator. The large MOSFETs operate above approximately 5% of the maximum output current, whereas the small MOSFET operates below this current level, but at the same constant frequency.

Because the low current "baby" MOSFET (available in SOT-23) has much lower gate charge than the large synchronous MOSFETs, far less efficiency loss is incurred as the load current drops. Eventually, as the load current is reduced below approximately 1% of the maximum current, the loop begins skipping cycles and the frequency does begin to decrease. However, it does not enter the audio region until the load current has fallen even further. This performance comes at little penalty in quiescent current, which, at around 200µA, is nearly as low as that of the LTC1148.

Burst Mode operation is also possible in all LTC1435–LTC1439 controllers for even higher efficiencies at the expense of more frequency variability. To activate Burst Mode operation, the small MOSFET is simply not installed. When the load current falls to where both large MOSFETs are turned off, the output capacitor supports the load until the error amplifier increases the I_{TH} pin

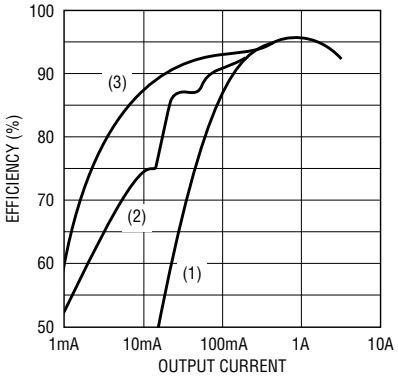

Figure 2. 10V to 5V conversion efficiency versus output current for three operating modes: 1) forced continuous operation; 2) Adaptive Power mode (constant frequency); and 3) Burst Mode.

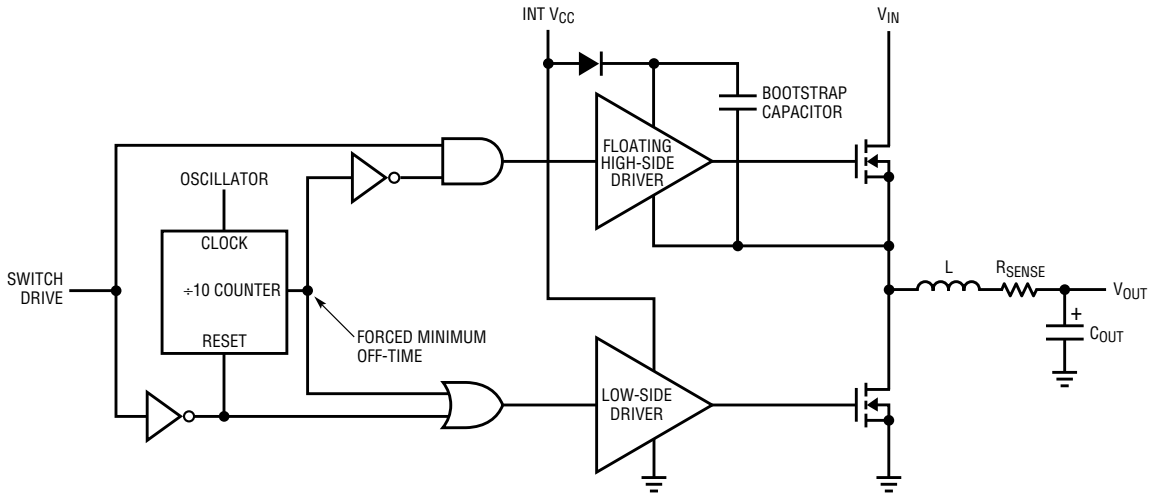

Figure 3. Operation at up to 99% duty cycle is made possible by ÷ 10 counter logic, which ensures low dropout.

voltage to 0.6V, at which point the large MOSFETs resume operation.

Whether in Adaptive Power mode or Burst Mode, the large MOSFETs can always be forced into continuous operation, independent of load current, by forcing the SFB pin low (more on this later). Figure 2 gives a comparison of efficiencies in a 3A regulator for the three possible operating modes: forced continuous operation, Adaptive Power mode and Burst Mode.

Low Dropout without P-Channel MOSFETs

An important feature of the LTC1148 family is its ability to stay in regulation with the input voltage only slightly above the output, a condition known as low dropout. The LTC1148 achieves this by using a P-channel MOSFET switch that can operate at up to 100% duty cycle; in other words, it can connect the output to the input in dropout mode. This feature is important because it allows the maximum energy to be extracted from low voltage battery packs such as two lithium-ion cells (5.4V typical end-of-life voltage).

The LTC143X family changes to an all N-channel output stage to accrue the benefits of lower $R_{DS(ON)}$ and lower cost than corresponding P-channel MOSFETs. Driving N-channel MOSFETs requires the floating high-side driver shown in Figure 3; however, the bootstrap capacitor powering the floating driver requires periodic recharging, which can occur only when the top MOSFET is turned off and the bottom MOSFET is turned on. In past N-channel controllers, this recharge interval was guaranteed by forcing a minimum off-time during every oscillator cycle.

To relieve the duty cycle limitation resulting from minimum off-time control, the LTC1435–LTC1439 detect the onset of dropout by counting the number of oscillator pulses that have passed without the top MOSFET turning off. Only when the count reaches 10 is a minimum off-time forced. This extends the duty cycle capability from around 90% to 99% while still guaranteeing that the top MOSFET bootstrap capacitor remains charged. Thus, dropout performance comparable to the LTC1148 can be achieved.

Auxiliary Output Voltages Made Easy

The new LTC143X family of DC/DC controllers has also been designed with many "hooks" to make the addition of extra output voltages easy, as can be seen from two representative applications. The first, shown in Figure 4, is a cost effective LTC1437 switcher/linear combination with 5V/3A and 12V/200mA outputs. The main switcher loop is set to 5V by strapping the V_{PROG} pin high. Other output options include 3.3V (V_{PROG} low) and adjustable (V_{PROG} open).

The 12V output in Figure 4's circuit is provided by the auxiliary linear regulator operating in conjunction with a secondary winding feedback loop using the SFB pin mentioned earlier. The turns ratio for the transformer is 1:2.2, resulting in a secondary output voltage of approximately 15V. The secondary resistive divider causes the SFB pin voltage to drop below the internal 1.19V reference if the secondary output is loaded and the 5V output has little or no load. This forces continuous operation as necessary to guarantee sufficient headroom for the linear regulator to maintain 12V regulation independent of the 5V load. The auxiliary output is turned on and off with the AUX ON pin.

The auxiliary regulator can also be used in an adjustable mode, determined by the voltage on the AUX DR pin. When the AUX DR voltage is higher than 9.5V, as is the case in Figure 4, the regulator automatically configures itself for fixed 12V operation using an internal AUX FB resistive divider. When AUX DR is less than 8.5V, the internal divider is removed and the user can adjust the output voltage via an external divider referenced to 1.19V. The external auxiliary regulator PNP pass transistor is sized for the desired output current;

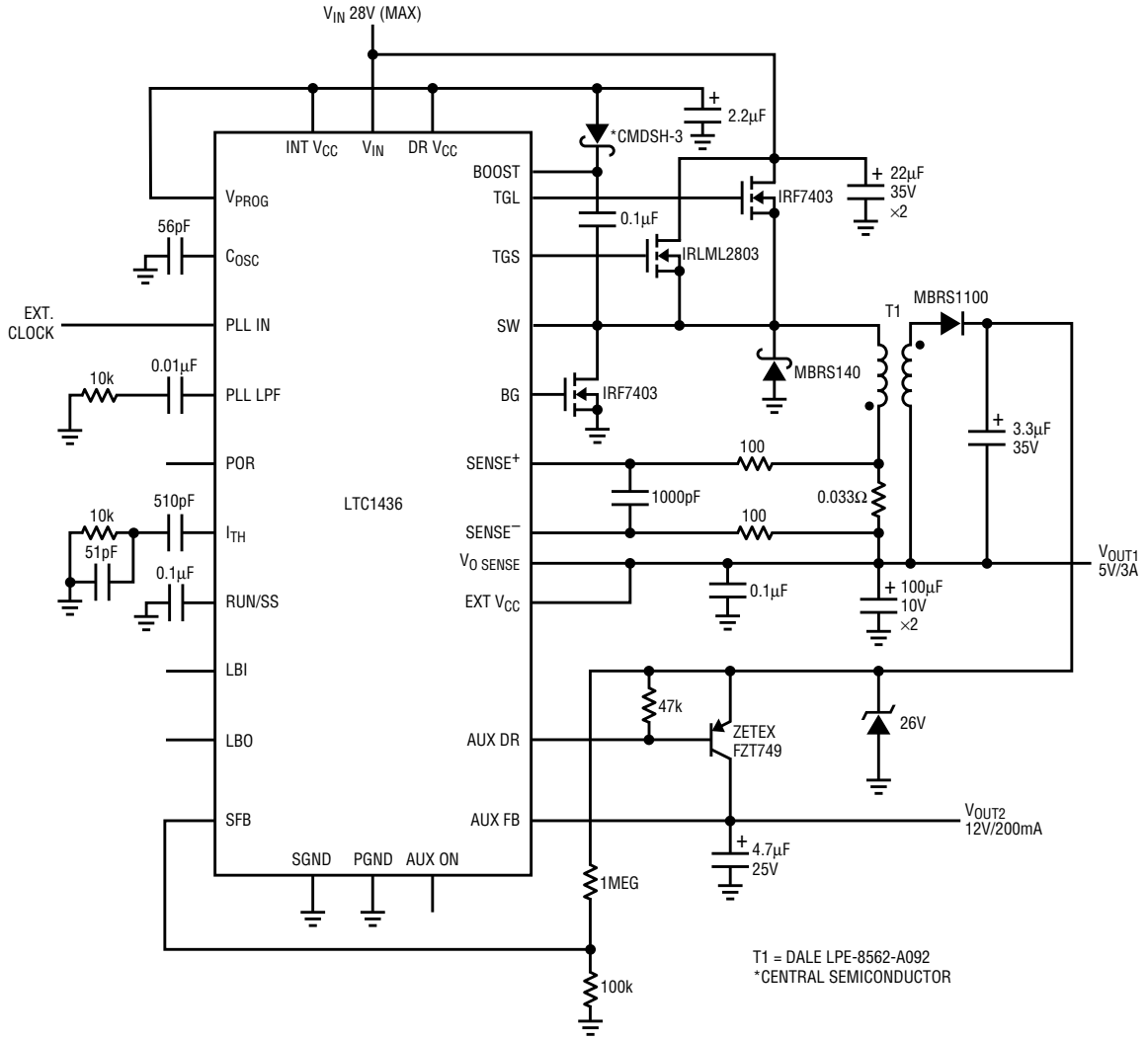

Figure 4. High efficiency, constant-frequency, dual-output supply delivers 3A at 5V and 250mA at 12V.

in this case a SOT-223 device is used to deliver up to 200mA.

Synchronizable, Triple-Output, Low Dropout Supply

The LTC1439-based supply shown in Figure 5 is an example of how three logic supply voltages, 5V, 3.3V and 2.9V, can be easily derived using only two simple inductors. The two main DC/DC controller loops are used to supply 5V/3A and 3.3V/5.5A. Up to 2.5A of the 3.3V output current is then used to supply a 2.9V output using the adjustable capability of the auxiliary linear regulator.

The 2.9V output also illustrates the use of an external NPN pass transistor with the auxiliary regulator. Because only 0.4V is dropped across the NPN transistor, 2.9V efficiency remains in the 85% range. And thanks to the 99% duty cycle capability of the switcher loops, Figure 5's supply can maintain all three output voltages in regulation down to V_{IN} = 5.2V with a 2A load on the 5V output.

The phase-locked loops built into the LTC1437 and LTC1439 offer a convenient means of synchronization for the applications in Figures 4 and 5. The internal oscillator is actually a voltage-controlled oscillator (VCO) controlled by the voltage on the PLL LPF pin. When no PLL IN signal is present, the PLL LPF goes low, causing the oscillator to run at its minimum frequency (f_{MIN} = 180kHz with C_{OSC} = 56pF). Applying a 3.3V or 5V logic signal of any duty cycle to the PLL IN pin will cause the oscillator frequency to lock to the logic signal frequency and to track it up to a maximum of $f_{MAX} = 2 \times f_{MIN}$. A logic signal may also be coupled to PLL LPF to effect a 2:1 frequency shift, provided that the initial frequency has been set to less than 200kHz.

Starting Up in Sequence

Power supply sequencing upon initial application of input power is a critical issue. This is particularly true in applications where the controllers are left on continually, which will frequently be the case since the quiescent current is very low. The LTC143X family has unique combined run and soft-start pins and power-on-reset

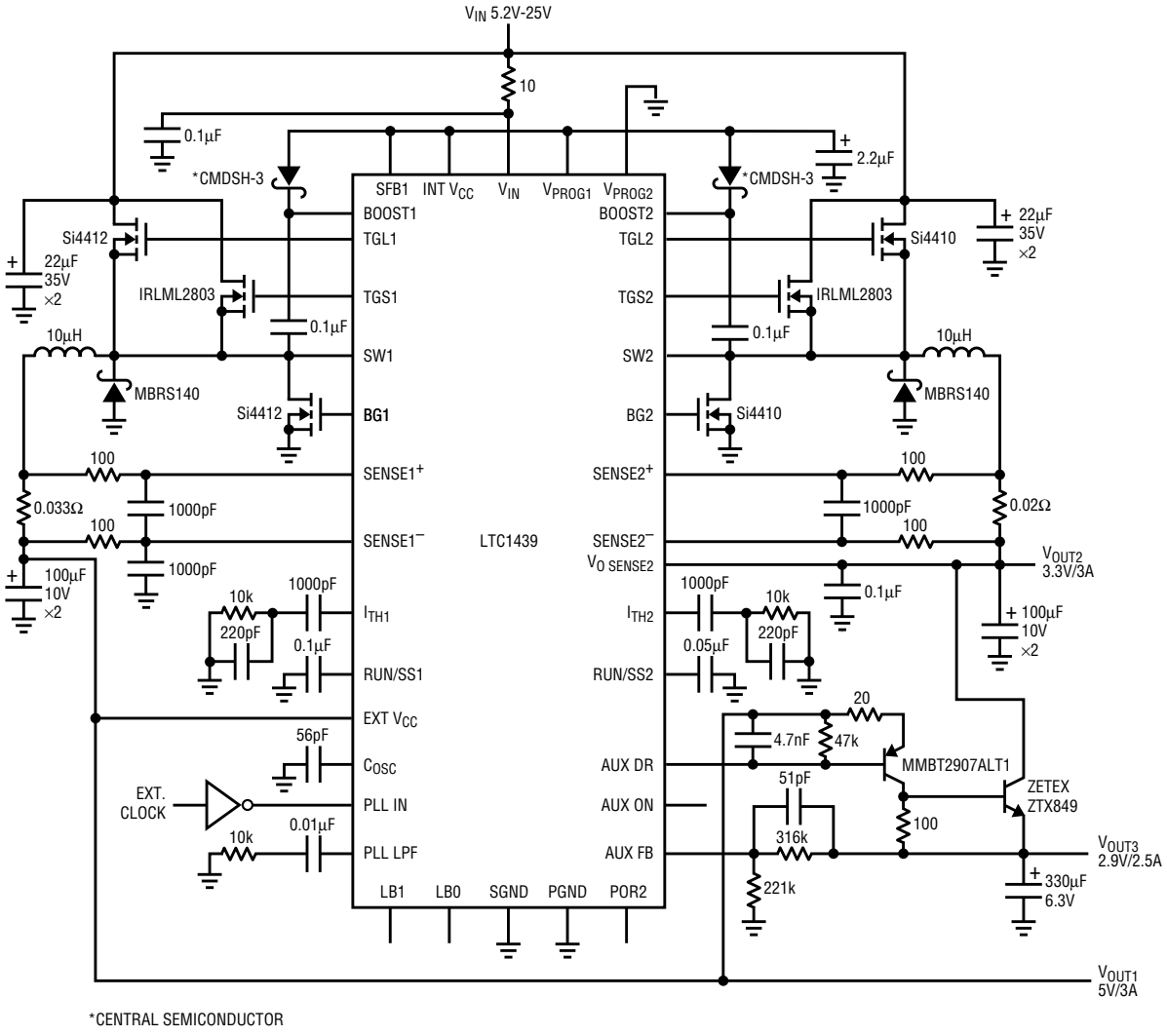

Figure 5. High efficiency, constant-frequency, triple-output logic supply features 200mV dropout.

outputs that greatly ease start-up sequencing and reset issues.

The RUN/SS pins have internal 3µA pull-ups whenever V_{IN} is present. An external capacitor to ground is charged by this current to provide both a start delay and soft-start characteristic. At initial application of input power, or following a shutdown, the RUN/SS voltage will be low. As the RUN/SS voltage ramps up, the associated controller remains shut down until the voltage reaches 1.3V. Thus by using different value capacitors for the two RUN/SS pins in an LTC1438 or LTC1439, one controller can be forced to always start before the other.

Once the RUN/SS voltage passes 1.3V, the controller starts with the initial peak inductor current at approximately one third of its maximum value and ramps up from there, reaching normal operation at 3V. Figure 6 is a photograph showing the 3.3V output staged to start 10ms before the 5V output when power is first applied to Figure 5's circuit.

Power-On Reset Monitor Included

An internal regulation monitor is continually monitoring the main controller output in the LTC1436/LTC1437, and the controller 2 output (3.3V in Figure 5) in the LTC1438/LTC1439. When out of regulation or in shutdown mode, the POR open drain output pulls low. At start-up, once the output voltage has reached 5% of its final value, an internal timer is started, after which the POR pin is released. The timer is accomplished by counting 2^{16} oscillator cycles, yielding a delay-to-release reset of approximately 300ms in a typical application.

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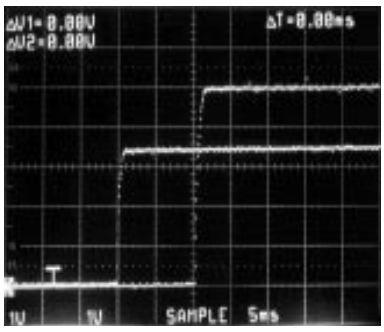

Figure 6. Start-up of 3.3V and 5V supplies is easily staged upon initial application of input power.

New 12-Bit ADC Squeezes 100ksps from 10mW

by William C. Rempfer and Ringo Lee

Until now, 12-bit 100ksps ADCs have needed as much as 100mW to do their jobs. That has changed with the new LTC1274 and LTC1277. These complete, parallel-output 12-bit ADCs sample at 100ksps while drawing only 10mW. They have some new features that make them very attractive for applications in the 100ksps range and below:

- ❏ Complete ADC with reference and sample-and-hold
- ❏ 10mW power dissipation from 5V or ±5V supplies
- ❏ Nap and Sleep power-down modes
- ❏ Reference Ready (REFRDY) signal indicating wake-up from Sleep mode
- ❏ Unipolar/bipolar conversions
- ❏ Separate conversion-start input
- ❏ High-Z analog inputs can be MUXed or AC coupled
- ❏ 12-bit or 2-byte parallel I/O
- ❏ 3V logic supply interface (LTC1277)

This article will describe the new devices and show how they can be used to save power, improve performance and simplify the design of new systems.

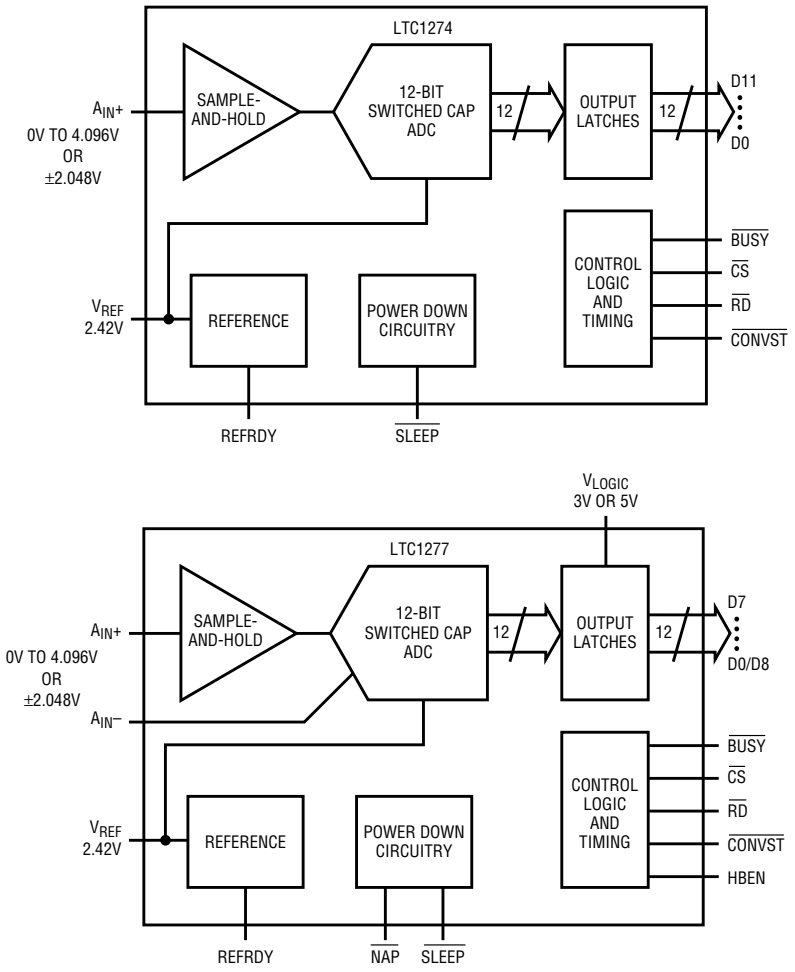

Figure 1. The new ADCs come complete with wideband sample-and-hold and reference. They sample at 100ksps on 10mW and provide novel power-down options.

10mW, 100ksps and More

As Figure 1 shows, the LTC1274 and LTC1277 come complete with a switched capacitor ADC, a very wide band sample-and-hold, a reference and power-down circuitry. They provide parallel I/O in a 12-bit (LTC1274) or 8-bit (LTC1277) format. In addition to the normal microprocessor interface signals, they have conversion start inputs and data ready outputs for latching the parallel data when the conversion is complete. Two power-down modes are available: Nap mode drops the supply current from 2mA to 160µA and provides instant wake-up. Sleep mode drops supply current below 1µA, and has a longer wake-up time. A power-good signal (REFRDY) is provided to indicate when wake-up from Sleep has been achieved and to ensure that the system is operating correctly. The devices are available in 24-pin SO-packages in commercial and industrial temperature ranges.

New Features Save Power

Figure 2 shows how the LTC1274 and LTC1277 add to LTC's low power, high speed ADC family. At 10mW, these new ADCs have the lowest power dissipation available today. In

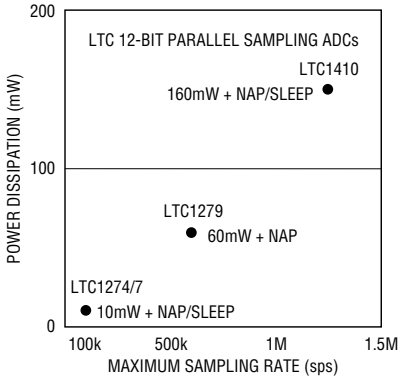

Figure 2. The LTC1274/LTC1277 offer very low power consumption for applications at 100ksps and below.

Table 1. LTC1277 Shutdown Options

LTC1277 LOGIC INPUTS		OPERATING	SUPPLY	WAKE-UP
$\overline{NAP}$	$\overline{SLEEP}$	MODE	CURRENT	TIME
1	1	ACTIVE	2mA	—
0	1	NAP	160 µA	400ns
X	0	SLEEP	0.3 µA	4ms

addition, they have two power-down modes that save even more power.

Take a Nap and Wake Up Quickly

Table 1 shows the shutdown options available. Nap mode allows the LTC1277 to be powered down and reawakened quickly. When $\overline{NAP}$ is taken low, everything but the reference shuts down and the supply current drops from 2mA to 160µA. When $\overline{NAP}$ is brought back high, the device wakes up instantly (400ns typical). Figure 3 shows the conversion timing when using Nap mode. First, $\overline{NAP}$ is taken high and one or more conversions are performed. After the last conversion, the $\overline{NAP}$ pin is taken back low. This method can reduce the power dissipation by a factor of up to 12.5 for slower sample rates (see Figure 4). At sample rates below 10ksps, the current flattens out at the Nap-mode value of 160µA.

Sleep Mode: More Restful but Slower Wake-Up.

Power drain can be reduced even further with Sleep mode. Taking $\overline{SLEEP}$ low invokes a complete shutdown of the ADC. The internal reference powers off and the supply current drops to less than 1µA. When the reference is turned off, its output bypass capacitor starts to discharge.

Bringing $\overline{SLEEP}$ high powers the device back up. A wake-up time is required for the internal reference to slew its output back to the desired value and settle. This time is relatively slow and variable. It depends on the reference bypassing and loading, on the slewing current of the internal reference and on how far the reference has fallen away from its desired value. The longer the device is shut down, the farther the reference output will discharge and the longer the wake-up time will be. Depending on these factors, Sleep-mode wake-up time can vary from less than 1ms to 40ms.

The LTC1274 and LTC1277 are attractive new converters. They bring new levels of power savings, performance and versatility to the 12-bit 100ksps ADC arena

How Do I Know You're Awake?... REFRDY!

In the past, ADCs with complete shutdown (including the reference) have offered no indication of when the converter's reference was powered up and ready to operate. Users had to wait some arbitrarily long time to allow a worst-case device to wake up under worst-case conditions. This caused two problems: first, the full-power drain of the converter was wasted during this long delay time. Even worse, since no assurance was given that enough time had elapsed, conversion results may have been erroneous.

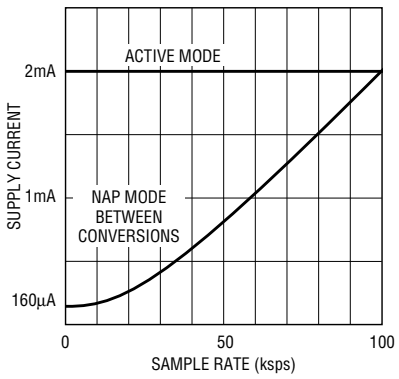

Figure 4. Using Nap mode between conversions cuts power by a factor of up to 12.5 as the sample rate is reduced. Sleep mode cuts power even more.

The LTC1274 and LTC1277 solve both problems with a new output signal called REFRDY (reference ready), which monitors the internal reference and indicates when it has settled. This signal tells the user exactly when the system is ready to convert. No extra power need be wasted in some arbitrarily long delay time. Also, full assurance is given that the device is ready to go and that the results will be accurate. Figure 5 shows the power-up sequence from Sleep mode. The REFRDY signal indicates readiness to convert.

Power the Reference First, Then the ADC

The LTC1277 can save even more power during wake-up from Sleep mode. If a converter is awakened from Sleep mode directly to full-power mode, it draws its full supply current as the reference slews. This is unnecessary and wastes power. The

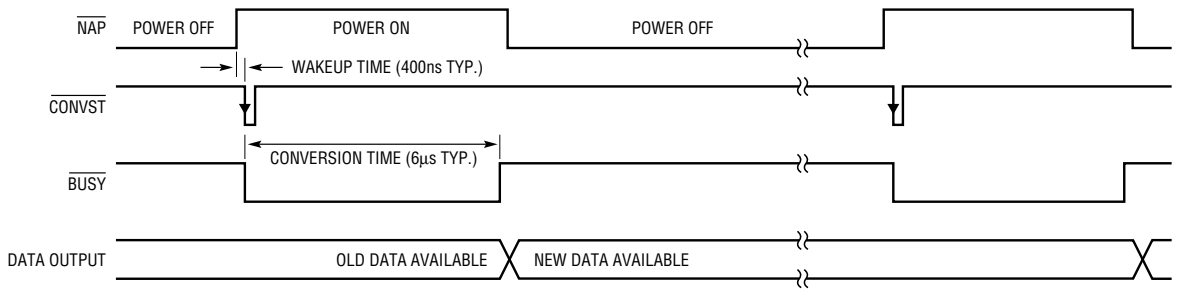

Figure 3. The LTC1277 wakes up from Nap mode quickly, converts and is then powered down. Data can be read at any time, even in shutdown.

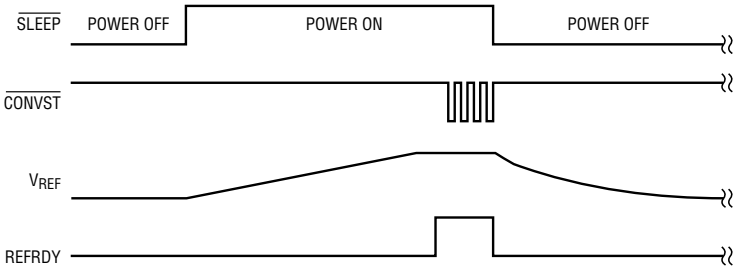

Figure 5. On power-up from Sleep mode, the REFRDY signal indicates when the ADC's reference has fully awakened from sleep mode and is ready for conversions.

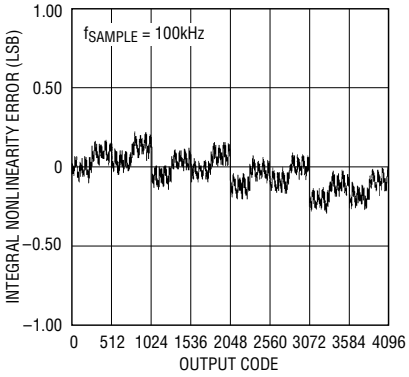

Figure 7. Typical linearity is better than 12 bits (typically 14 bits). Linearity is guaranteed to be ±1LSB maximum over temperature.

LTC1277 can prevent this waste if the REFRDY output is tied to the $\overline{NAP}$ input (see Figure 6). This connection allows the device to go from Sleep mode to Nap mode until the reference is ready. REFRDY then releases the ADC from Nap mode and the device is ready to convert. Figure 6 shows how the converter draws only 160µA during the reference settling time instead of the full 2mA current. This can cut power dissipation by a factor of two to four in applications where Sleep mode is used.

Unbeatable AC and DC

The LTC1274 and LTC1277 bring unusually high performance to the 100ksps speed range. They offer excellent DC and AC specifications and an extremely linear, wideband sample-and-hold, which is suitable for undersampling. DC specifications include maximum INL and DNL of ±1LSB with no missing codes guaranteed. Figure 7 shows a typical linearity of far better than 12 bits (typically 14 bits). Drift of the internal reference is 30ppm/°C max.

AC specifications such as signal to noise and distortion (SINAD) and THD are specified at 71dB and 76dB minimum. These are very good specifications for a 12-bit ADC, but the impressive thing is that they are specified at twice the Nyquist frequency. This AC performance is made possible by an extremely linear, wideband sample-and-hold design. Figure 8 shows a plot of the ADC performance as the analog input frequency is increased. This is the real test of a sample-and-hold because, as the input frequency increases, the sample-and-hold must slew faster without distortion in order to track the signal accurately. Also, at high input slew rates, any excess aperture jitter of the sample-and-hold shows up as a degradation of the noise floor. As the Figure shows, the devices excel in this area with good noise and distortion at 1, 2, 5 or even 10 times the Nyquist frequency.

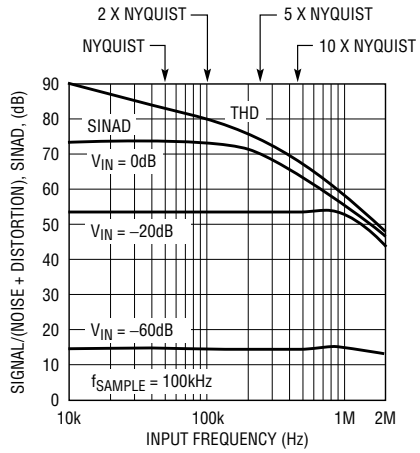

Figure 8. The LTC1274/LTC1277 can accurately sample very wideband input signals. Their SINAD and THD are nearly theoretical at up to five times Nyquist and still usable at ten times Nyquist.

Simplify the System Design

The new converters have both analog and digital features that make them easier to use and eliminate external hardware.

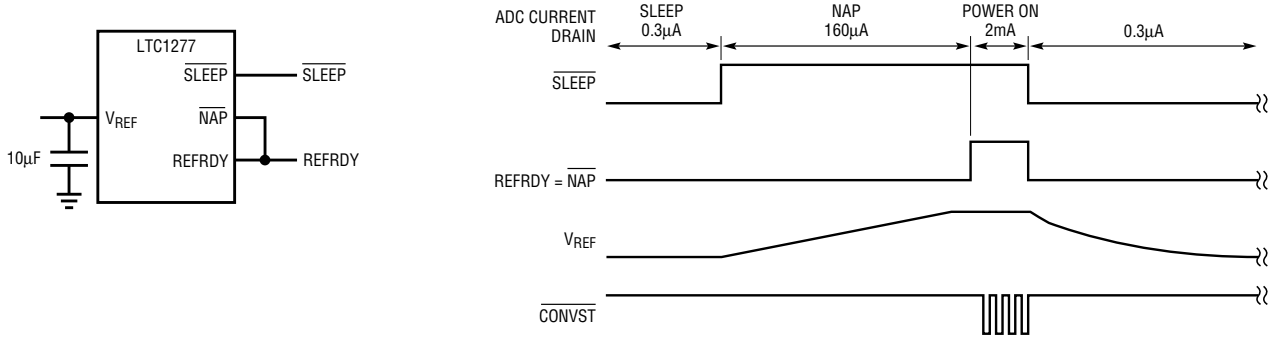

Figure 6. Tying the LTC1277's $\overline{NAP}$ input to its REFRDY output saves power by delaying the turn-on of power until the reference is settled.

Analog Flexibility

Figure 9 shows some of the analog features of the ADCs. Both devices contain a sample and hold. The LTC1277 has a differential input that allows the input range to be offset. The input range for both converters automatically switches from 0V–4.096V unipolar with V_{SS} grounded, to ±2.048V bipolar when V_{SS} is tied to –5V. The internal reference can be overdriven with an external 2.5V reference to improve the full-scale temperature coefficient. In bipolar mode, the reference pin can be driven with an op amp to provide a 2:1 AGC function.

The analog inputs are high impedance, making them easy to multiplex with an inexpensive CMOS MUX. No errors are caused because no DC currents are drawn through the MUX's on resistance. The high-Z inputs also eliminate the AC-coupling problems found on competitive devices. (Many of these other converters use internal, resistive level shifters to generate bipolar input spans. These internal resistors charge up the AC-coupling cap and pull the input up toward full scale; as a result, part of the signal gets clipped.) To AC couple the LTC1274 and LTC1277, simply use a series C and an R to ground (or to wherever you desire the DC level to be) on the analog input.

Digital Simplicity

The digital interface is shown in Figure 10. In addition to the well known microprocessor interface signals ($\overline{CS}$, $\overline{RD}$, etc.), the LTC1274 and LTC1277 provide several new signals. A separate convert-start input ($\overline{CONVST}$) allows operation from an external sample clock, if desired. This frees the microprocessor from having to request conversions at precise sample intervals, which is often impossible. In this mode, the sample signal starts a conversion. When it is complete, the ADC interrupts the microprocessor (with the $\overline{BUSY}$ signal) and the microprocessor reads the data asynchronously. Alternatively, $\overline{CONVST}$ can be tied to $\overline{RD}$, which allows the microprocessor to read data and start conversions in the old fashioned way.

Output data is available as a 12-bit word (LTC1274) or as two 8-bit bytes (LTC1277). Both converters have $\overline{BUSY}$ signals that indicate when output data is ready to be latched. An output logic supply allows the LTC1277 to interface directly to 3V systems.

Conclusion

The LTC1274 and LTC1277 are attractive new converters. They bring new levels of power savings, performance and versatility to the 12-bit 100ksps ADC arena. Their 10mW power levels and novel shutdown modes must be considered by power-sensitive designers. The clean wideband sampling capability and low noise make them ideal for signal-capture applications. And the flexible feature set can simplify the system design. These devices are a "must see" for users of sampling ADCs.

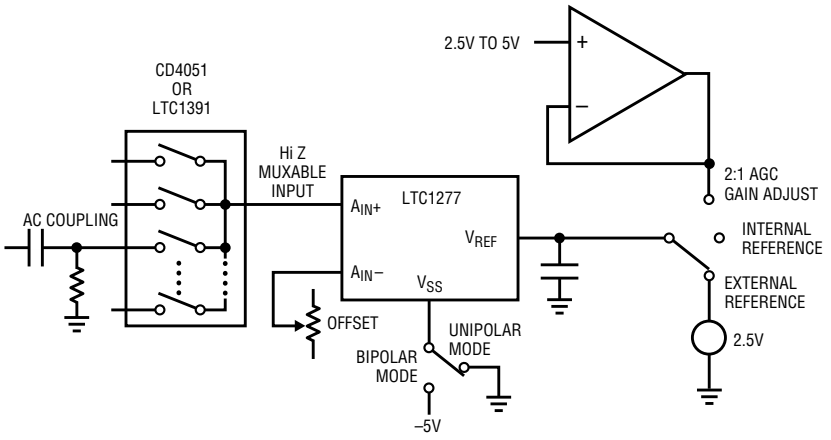

Figure 9. Analog flexibility includes easy AC coupling and MUXing, offsetting the input span, unipolar or bipolar inputs and a reference pin that can be overdriven.

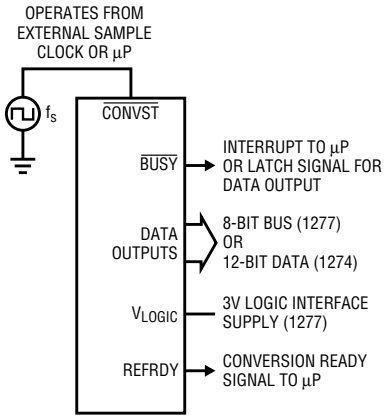

Figure 10. The digital hookup is simple, with an external conversion start input, 8- or 12-bit data outputs, data-ready signal ($\overline{BUSY}$), reference-ready signal (REFRDY) and a 3V logic-interface supply (LTC1277).

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The LT1511 3A Battery Charger Charges All Battery Types, Including Lithium-Ion

by Chiawei Liao

The LT1511 current mode PWM battery charger is the simplest, most efficient solution for fast charging modern rechargeable batteries, including lithium-ion (Li-Ion), nickel-metal-hydride (NiMH) and nickel-cadmium (NiCd) that require constant-current and/or constant-voltage charging. The internal switch is capable of delivering 3A DC current (4A peak current). Full charging current can be programmed by resistors or by a DAC to within 5%, and the trickle charge current can be programmed to 10% accuracy. With 0.5% reference voltage accuracy, the LT1511 meets the critical

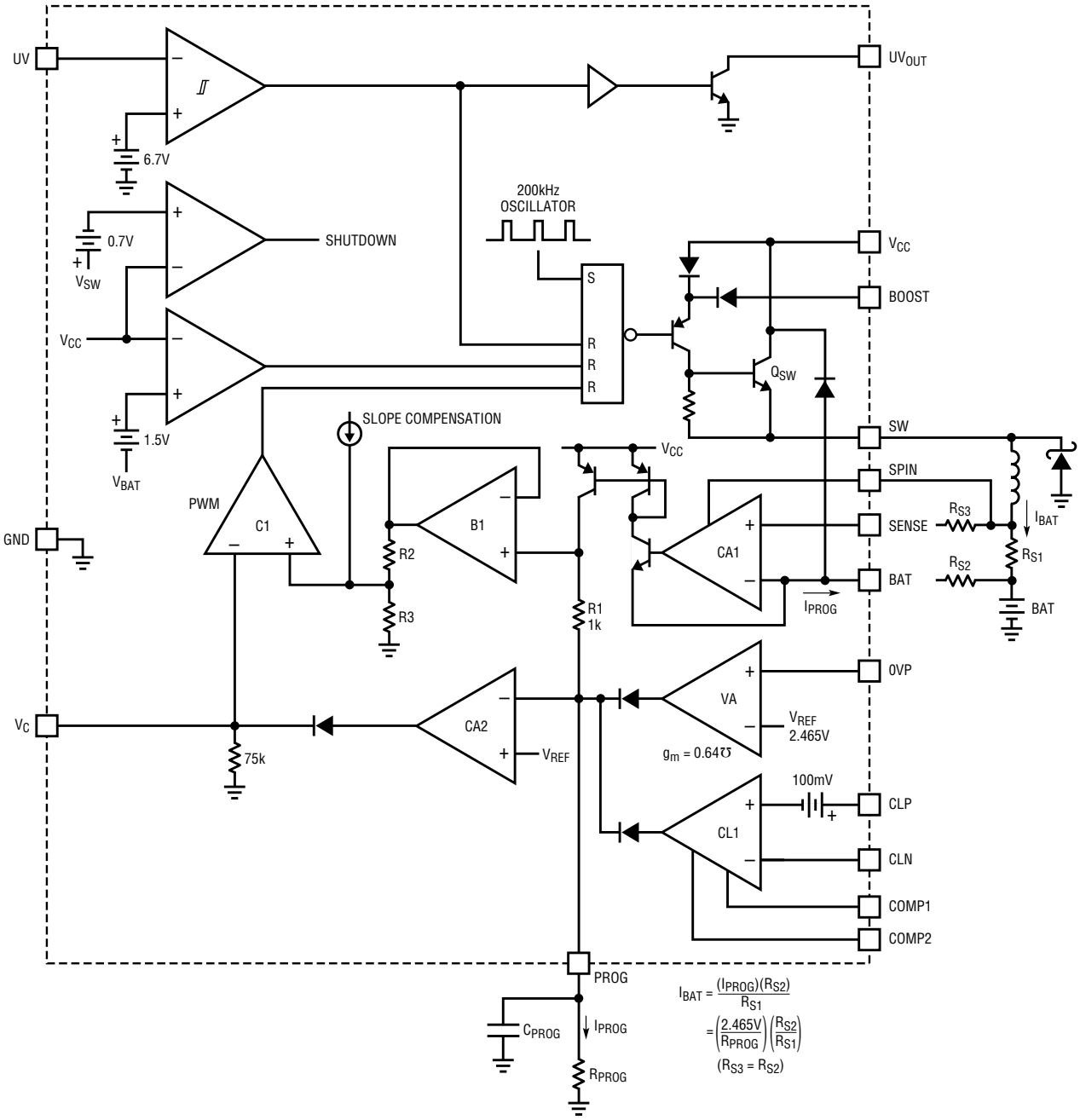

Figure 1. LT1511 block diagram

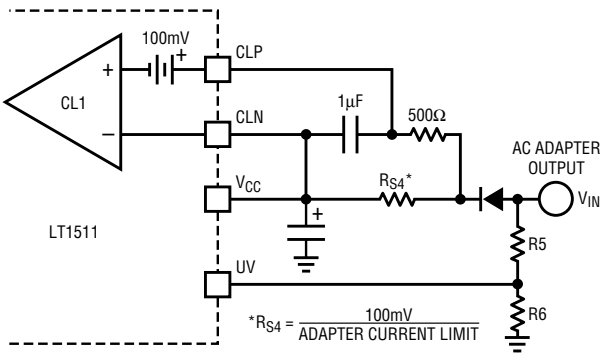

Figure 2. Adapter current limiting

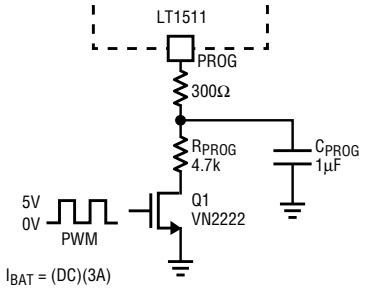

Figure 3. PWM current programming

constant-voltage charging requirement for lithium cells.

The LT1511 is equipped with a voltage-control loop to control charging voltage and a current-control loop to control charging current. A third control loop is provided to regulate the current drawn from the AC adapter. This allows simultaneous equipment operation and battery charging without overloading the adapter. Charging current is reduced to keep the adapter current within specified levels.

The LT1511 can charge batteries ranging from 1V to 20V. Ground sensing of current is not required and the battery's negative terminal can be tied directly to ground. A saturating switch running at 200kHz gives high charging efficiency and small inductor size. A blocking diode is not required between the chip and the battery because the chip goes into sleep mode and drains only 3µA when the wall adapter is unplugged. Soft-start and shutdown features are also provided. The LT1511 is available in a 24-pin fused-lead power SO wide package with a thermal resistance of 30°C/W.

Operation

The LT1511 is a current mode PWM step-down (buck) switcher. The DC battery-charging current is programmed by a resistor, R_{PROG} (or by a DAC output current), at the PROG pin (see the block diagram in Figure 1). Amplifier CA1 converts the charging current through R_{S1} to a much lower current, I_{PROG}, fed into the PROG pin. Amplifier CA2 compares the output of CA1 with the programmed current and drives the PWM loop to force them to be equal. High DC accuracy is achieved with averaging capacitor C_{PROG}. Note that I_{PROG} has both AC and DC components. I_{PROG} goes through R1 and generates a ramp signal that is fed to the PWM control comparator C1 through buffer B1 and level-shift resistors R2 and R3, forming the current mode inner loop. The Boost pin drives the switch NPN Q_{SW} into saturation and reduces power loss. For batteries such as lithium-ion that require both constant-current and constant-voltage charging, the 0.5%, 2.465V reference and the amplifier VA reduce the charging current when the battery voltage reaches the preset level. For NiMH and NiCd, VA can be used for overvoltage protection. When the input voltage is not present, the charger goes into low current (3µA typically) sleep mode as the input drops 0.7V below the battery voltage. To shut down the charger, simply pull the V_C pin low with a transistor.

Adapter Limiting

An important feature of the LT1511 is the ability to automatically adjust charging current to a level that avoids overloading the wall adapter. This allows the product to operate at the same time that batteries are being charged, without requiring complex load-management algorithms. Additionally, batteries will automatically be charged at the maximum possible rate of which the adapter is capable. This feature is created by sensing total adapter output current and adjusting charging current downward if a preset adapter-current limit is exceeded. True analog control is used, with closed-loop feedback ensuring that adapter load current remains within limits. Amplifier CL1 in Figure 2 senses the voltage across R_{S4}. When this voltage exceeds 100mV, the amplifier will override the programmed charging current and limit adapter current to $100mV/R_{S4}$. A lowpass filter formed by 500Ω and 1µF is required to eliminate switching noise.

Charging Current Programming

The basic formula for charging current is

$$I_{BAT} = I_{PROG}\left(\frac{R_{S2}}{R_{S1}}\right) = \left(\frac{2.465V}{R_{PROG}}\right)\left(\frac{R_{S2}}{R_{S1}}\right)$$

where R_{PROG} is the total resistance from PROG pin to ground.

For example, 3A charging current is needed. To have low power dissipation in R_{S1} and enough signal to drive the amplifier CA1, let R_{S1} = 100mV/3A = 0.0033Ω. This limits R_{S1} power to 0.3W. Let R_{PROG} = 5k, then

$$R_{S2} = R_{S3} = \frac{(I_{BAT})(R_{PROG})(R_{S1})}{2.465V}$$

$$= \frac{(3A)(5k)(0.033)}{2.465V} = 200\Omega$$

Charging current can also be programmed by pulse-width modulating I_{PROG} at a frequency higher than a few kHz (Figure 3). Charging current will be proportional to the duty cycle of the switch, with full current at 100% duty cycle.

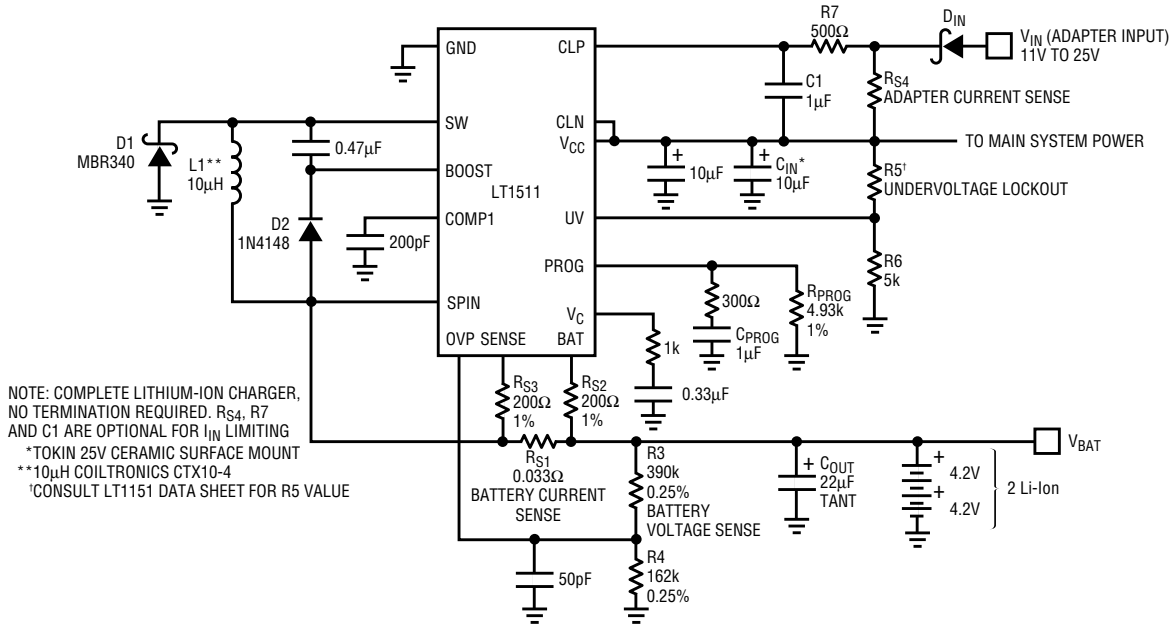

Figure 4. 3 Amp lithium-ion battery charger

Lithium-Ion Charging

The 3A lithium battery charger (Figure 4) charges lithium-ion batteries at a constant 3A until the battery voltage reaches a limit set by R3 and R4. The charger will then automatically go into a constant-voltage mode, with the current decreasing to zero over time as the battery reaches full charge. This is the normal regimen for lithium-ion charging, with the charger holding the battery at "float" voltage indefinitely. In this case no external sensing of full charge is needed.

Current though the R3/R4 divider is set at 15µA to minimize battery drain when the charger is off. The input current to the OVP pin is 3nA and this error can be neglected.

With divider current set at 15µA, R4 = 2.465/15mA = 162k and

$$R3 = \frac{(R4)(V_{BAT} - 2.465)}{2.465} = \frac{162k(8.4 - 2.465)}{2.465}$$

$$= 390k$$

Lithium-ion batteries typically require float-voltage accuracy of 1% to 2%. The accuracy of the LT1511 OVP voltage is ±0.5% at 25°C and ±1% over full temperature. This leads to the possibility that very accurate (0.1%) resistors might be needed for R3 and R4. Actually, the temperature of the LT1511 will rarely exceed 50°C in float mode because charging currents have tapered off to a low level, so 0.25% will normally provide the required level of overall accuracy.

Nickel-Cadmium and Nickel-Metal-Hydride Charging

The circuit in the 3A lithium battery charger (Figure 4) can be modified as shown in Figure 5 to charge NiCd or NiMH batteries. For example, two-level charging is needed; 2A when Q1 is on and 200mA when Q1 is off. For 2A full current, the current sense resistor (R_{S1}) should be increased to 0.05Ω, so that enough signal (10mV) will be across R_{S1} at 0.2A trickle charge to keep charging current accurate.

For a two-level charger, R1 and R2 are found from

$$R1 = \frac{(2.465)(4000)}{I_{LOW}} \qquad R2 = \frac{(2.465)(4000)}{I_{HI} - I_{LOW}}$$

All battery chargers with fast charge rates require some means to detect the full-charge state in the battery in order to terminate the high charging current. NiCd batteries are typically charged at high current until temperature rise or battery voltage decrease is detected as an indication of nearly full charge. The charging current is then reduced to a much lower value and maintained as a constant trickle charge. An intermediate "top off" current may be used for a fixed time period to reduce 100% charge time.

NiMH batteries are similar in chemistry to NiCd but have two differences related to charging. First, the inflection characteristic in battery voltage as full charge is approached is not nearly as pronounced. This makes it more difficult to use dV/dt as an indicator of full charge, and temperature change is more often used, with a temperature sensor in the battery pack. Second, constant trickle charge may not be recommended. Instead, a moderate level of current is used on a pulse basis (1% to 5% duty cycle) with the time-averaged value substituting for a constant low trickle.

If overvoltage protection is needed, R3 and R4 should be calculated according to the procedure described in lithium-ion charging section. The OVP

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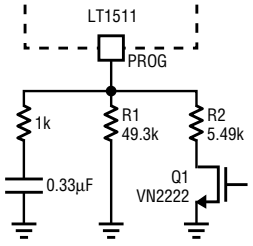

Figure 5. 2-step charging

LTC1520 High Speed Line Receiver Provides Precision Propagation Delay and Skew

by Victor Fleury

Introduction

The LTC1520 is a 50Mbit/s, low power, precision quad line receiver that translates differential input signals into CMOS/TTL output logic levels. The receivers employ a unique architecture that guarantees excellent performance over process and temperature, with propagation delay of 18ns ±2ns. The architecture affords low same-channel skew ($|t_{PHL} - t_{PLH}| < 600ps$), and low channel-to-channel propagation-delay variation (< 600ps). A new short-circuit detection technique permits indefinite shorts to power or ground.

Circuit Description

Short-channel CMOS circuitry typically has very wide performance variations. This is due in part to the large percentage variation in channel length and to second-order mobility and threshold effects. Increasing channel length not only decreases the drive capability of CMOS devices, but also increases the devices' gate capacitance (less current charging more capacitance). In effect, we see CMOS propagation delays varying as L^2 (square of the channel length). For example, the propagation delay of typical CMOS line receivers can vary as much as 500% over process and temperature. In applications where high speed clock and data waveforms are sent over long distances, propagation delay and skew uncertainties pose system design constraints. The LTC1520 addresses this problem. The propagation delays change by ±20%, a better than 10 times performance improvement.

The design was fabricated using Linear Technology's high performance CMOS process. The CMOS design makes it possible to achieve high speed and low DC power consumption without sacrificing ruggedness against overload or ESD damage. CMOS also allows for tighter propagation-delay skew. Figure 1 shows a block diagram of the LTC1520 signal path. The input differential pair amplifies the minimum 500mV (at speed) input signal level. Note the input resistor network, which expands the input common mode range (the LTC1520 has an input common mode range extending from 0V to 5V, whereas the LTC1518 and LTC1519 are future products that will have an input common mode range from –7V to +12V). The output is fed into another differential amplifier that switches a specified amount of current into its load capacitance. These two stages must have enough gain to switch all the available current. The output of the second stage is a valid logic level that feeds inverters.

High Data Rates

The LTC1520 can propagate pulses (Figure 2) of shorter duration than its propagation delay (20ns maximum). To obtain this high data rate (throughput), it is necessary to distribute the total propagation delay as evenly as possible between the stages. This allows rail-to-rail swing at the output of each stage. For example, if the output of the second stage has a 3V to 5V output swing, the succeeding inverter will never trip high. The minimum number of stages is also limited by the maximum rise/fall times allowed at the output (~3.5ns). However, the

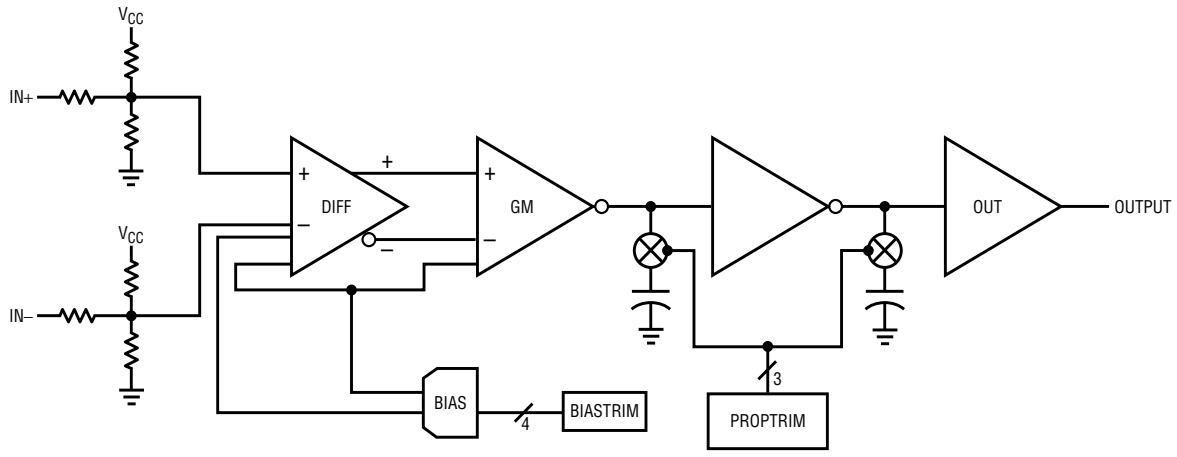

Figure 1. LTC1520 block diagram

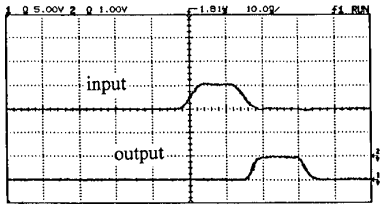

Figure 2. Typical propagation delay: V_{IN} = 500mV, 15ns pulse width

maximum number of stages is limited by the maximum propagation delay (latency).

Consistent Propagation Delay

The inherent temperature and process tolerance, along with bias and delay trimming, make it possible to guarantee a propagation delay window more than an order of magnitude tighter than that of the typical CMOS line receiver.

Temperature Stability

For large V_{GS} and a given channel length, the propagation delay of inverters increases with temperature. To keep temperature stability, the first two stages must have a delay that decreases with temperature. This was accomplished via a current source whose current is inversely proportional to mobility. Therefore, with increasing temperatures, the inverter's delay goes up as the delays of the first two stages go down.

Process Tolerance

At a given temperature and V_{GS}, the inverter delays vary as $\mu C_{OX} W/L$. The delays of the first and second stages vary inversely with μC_{OX} W/L. The effect of process variations on total propagation delay are canceled out to the extent that we are able to match the μC_{OX} W/L of the bias, inverters and differential stages. We include trims in both the bias network and in the signal path. For short channel length processes, we add capacitance evenly between one inverter and the second differential stage to maintain temperature stability.

Low Skew

Skew is typically caused by the unequal charging versus discharging of both internal and external capacitances. Unequal excitation of high frequency zeroes also contributes to skew. Therefore, it is necessary to keep the signal in differential form as much as possible. The first stage is differential-in/differential-out. It switches a multiple of the tail current into its capacitive load. Two differential stages are used to maintain charging versus discharging symmetry and to equalize feedthrough effects. Figure 3 shows two adjacent channels.

Low Overshoot

The LTC1520 can achieve maximum speeds with all four receivers operating simultaneously (500mV input differential signal), while maintaining low output overshoot. Small on-chip resistors help mitigate the effect of parasitic bond wire and leadframe inductances. Note that the system designer also needs to minimize printed circuit board parasitic inductances by placing surface mount ceramic bypass capacitors very close to the LTC1520. Low overshoot and ringing is desirable to reduce electromagnetic interference.

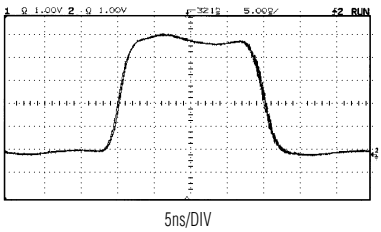

Figure 3. Typical channel-to-channel propagation delay is <600ps. (Two channels are overlaid here; the differences cannot be distinguished on this oscillograph.)

Short-Circuit Protection and Automatic Reset

Typical foldback short-circuit protection can lead to oscillation, slower rise/fall times and exaggerated skew. This family's novel short-circuit protection method avoids these problems by sensing the output voltage. If the output remains in the wrong state for longer than about 60ns, the output is shut off and a small, known current (~20mA, positive or negative, depending on V_{CC}/Gnd short) is dumped into the output. The circuit then detects when the short is removed and takes itself out of short-circuit mode. This avoids having to power the part up/down after detecting a short.

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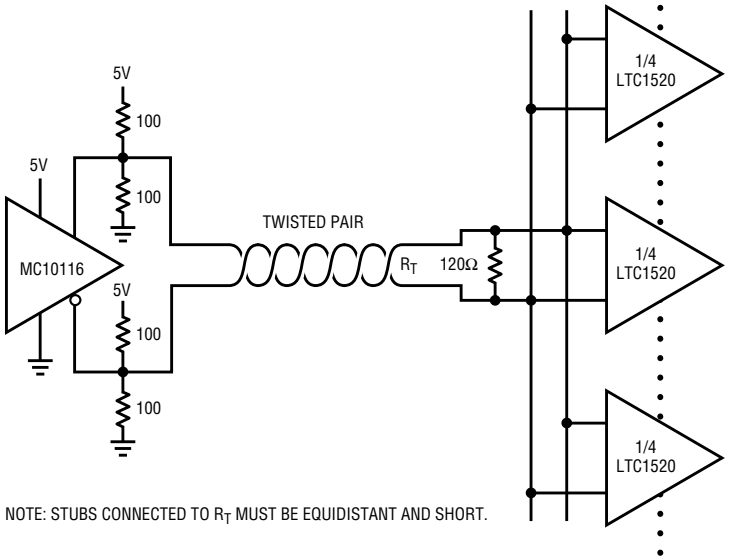

Figure 4. Typical LTC1520 application

The LTC1446 and LTC1446L: World's First Dual 12-Bit DACs in SO-8 Packages

by Hassan Malik and Jim Brubaker

Dual 12-Bit Rail-to-Rail Performance in a Tiny SO-8

The LTC1446 and LTC1446L are dual 12-bit, single-supply, rail-to-rail voltage output digital-to-analog converters. Both of these parts include an internal reference and two DACs with rail-to-rail output buffer amplifiers, packed in a small, space-saving 8-pin SO or PDIP package. These are 12-bit monotonic DACs with DNL guaranteed to be less than 0.5LSB. They have an easy-to-use SPI-compatible interface, with a digital output pin that allows several DACs to be daisy-chained to save board space. A power-on reset initializes the outputs to zero-scale at power-up.

The LTC1446 has an output swing of 0V to 4.095V, making each LSB equal to 1mV. It operates from a single 4.5V to 5.5V supply, dissipating 3.5mW (I_{CC} typical = 700µA). The LTC1446L has an output swing of 0V to 2.5V. It can operate on a single supply with a wide range of 2.7V to 5.5V. It dissipates 1.35mW (I_{CC} typical = 450µA) at a 3V supply.

Circuit Topology

Complete Stand-Alone Performance

Figure 1 shows a block and pin diagram of the LTC1446 and LTC1446L. Both parts have rail-to-rail output buffer amplifiers and an internal reference, offering the user convenient stand-alone performance. The data inputs for both DAC A and DAC B are clocked into one 24-bit shift register. The first 12-bit segment is for DAC A and the second is for DAC B. The MSB is loaded first and LSB last in both of these 12-bit segments. The data is latched into the shift register on the rising edge of clock. The clock pin has a hysteresis of about 150mV to make it less sensitive to noise. When all the data has been shifted in, it is loaded into the DAC registers when $\overline{CS}$/LD goes high. This also updates both 12-bit DACs and internally disables the CLK signal. Data in the 24-bit shift register is also available on the D_{OUT} pin, allowing the user to daisy-chain several DACs together. An internal power-on reset clears the shift regis-

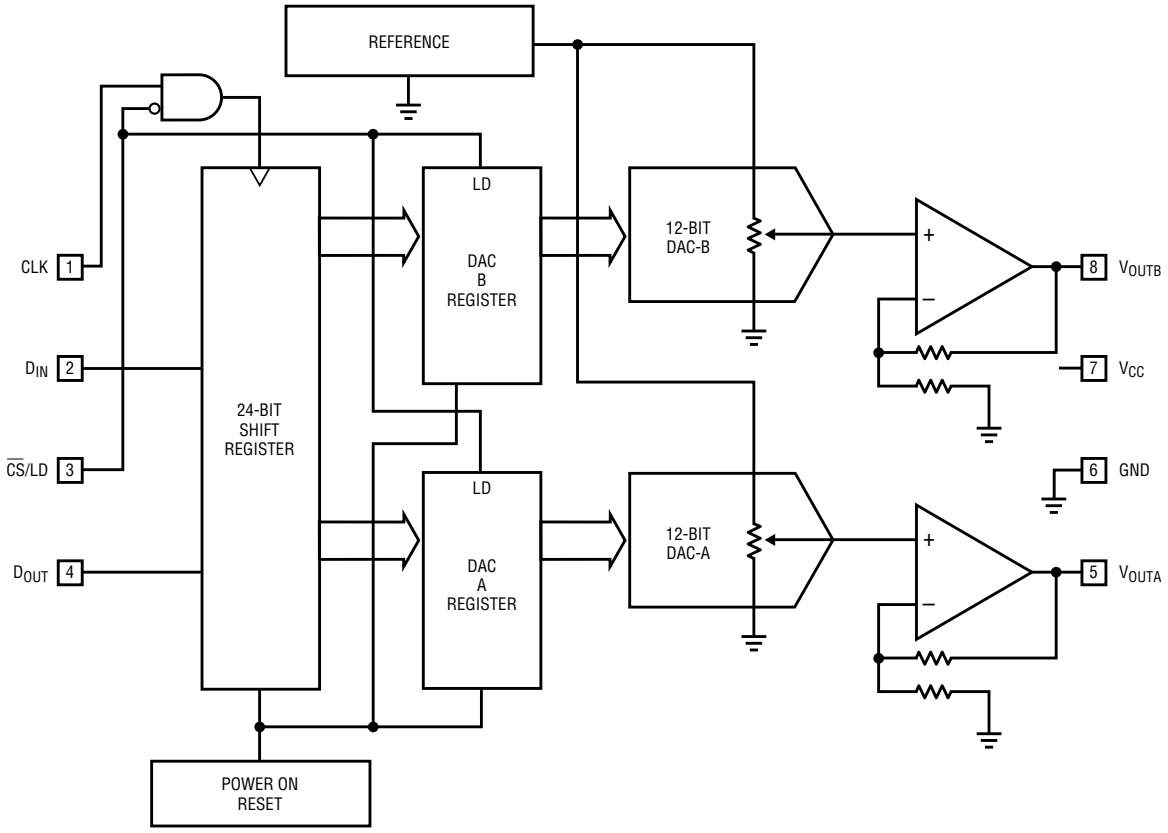

Figure 1. 12-bit rail-to-rail performance in an SO-8 package

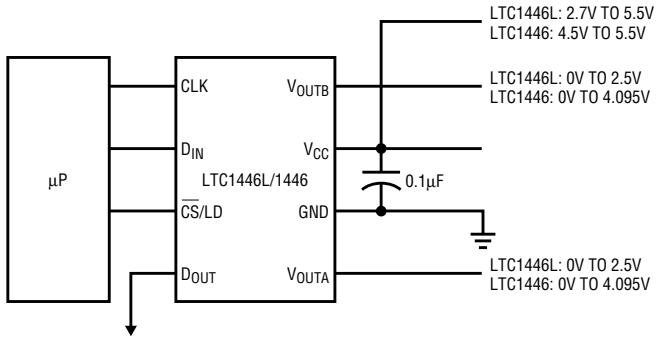

Figure 2. Typical application for the LTC1446L or LTC1446

ters and DAC registers to all zeros and forces both the buffer amplifier outputs to zero-scale. The LTC1446L has an internal reference of 1.22V and the amplifier gain is about 2.05, giving a convenient full scale of 2.5V. The LTC1446 reference is 2.048V and the amplifier gain is 2.0, giving it a full scale of 4.095V.

High Performance Rail-to-Rail Buffers

The rail-to-rail amplifiers on these parts can swing to within a few millivolts of either rail when unloaded, giving them true rail-to-rail performance. When swinging close to the rails, the effective output impedance is about 50Ω. The op amps are capable of sinking or sourcing over 5mA at a 5V supply. The mid-scale glitch at the output is 20nV-s and the digital feedthrough is a negligible 0.15nV-s.

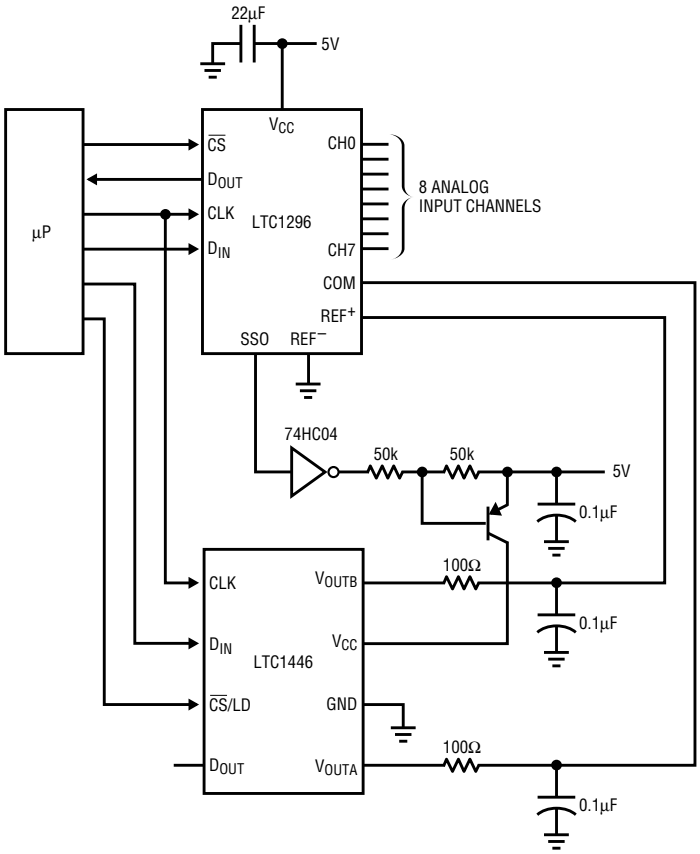

Figure 3. An autoranging 8-channel ADC with shutdown

Patented Architecture Guarantees Monotonicity

The LTC1446 family uses a proprietary architecture that was first used in the LTC1257 and is described in more detail in Volume III, Number 3 of *Linear Technology*. This novel architecture is inherently monotonic and has excellent 12-bit DNL, with a maximum specification of 0.5LSB.

The LTC1446 and LTC1446L are the world's only DACs that offer dual 12-bit stand-alone performance in an 8-pin SO or PDIP package. ...these DACs do not compromise on performance...

A Wide Range of Applications

Some of the typical applications for these parts include digital calibration, industrial process control, automatic test equipment, cellular telephones and portable, battery-powered applications. Figure 2 shows how these parts are typically used.

An Autoranging 8-Channel ADC with Shutdown

Figure 3 shows how to use one LTC1446 to make an autoranging ADC. The microprocessor sets the reference span and the common pin for the analog input by loading the appropriate digital code into the LTC1446. $V_{OUT\,A}$ controls the common pin for the analog inputs to the LTC1296 and $V_{OUT\,B}$ controls the reference span by setting the REF+ pin on the LTC1296. The LTC1296 has a shutdown pin that goes low in shutdown mode. This will turn off the PNP transistor supplying power to the LTC1446. The resistor and capacitor on the LTC1446 outputs act as a lowpass filter for noise.

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LT1490/LT1491 Over-the-Top Dual and Quad Micropower Rail-to-Rail Op Amps

by Jim Coelho-Sousae

Introduction

The LT1490 is Linear Technology's lowest power, lowest cost and smallest dual rail-to-rail input and output operational amplifier. The ability to operate with its inputs above V_{CC}, its high performance-to-price ratio and its availability in the MSOP package, sets the LT1490 apart from other amplifiers. A unique input stage allows the LT1490 to operate with input common mode voltages up to 30V above the positive supply. The LT1490 has a quiescent current of less than 50µA per amplifier, and can operate with supply voltages from 2.5V to 44V. The ability to withstand reverse supply voltages of up to 25V is another unique feature of the LT1490. For single 5V supply operation, typical specifications include 300µV input offset voltage, 3nA input bias current, 200pA input offset current, open-loop voltage gain of one million into a 10k load, 0.07V/µs slew rate, 100dB common mode rejection ratio and 98dB power supply rejection ratio. The output can swing to within 22mV of either rail with no load. The output current drive is typically ±20mA, and the part is stable with capacitive loads of up to 5000pF. Additional performance specifications are shown in Table 1.

The LT1490 dual is available with industry-standard pinout in 8-pin MSOP, 8-pin SO or 8-pin mini-DIP packages. The LT1491 quad is available with industry-standard pinout in 14-pin SO or 14-pin mini-DIP packages.

Table 1. Typical DC performance, 25°C

	Conditions	V_S = 3V	V_S = 5V	V_S = ±15V
Offset Voltage	V_{CM} = V_{EE} to V_{CC} – 1V	300µV	300µV	400µV
	= V_{EE} + 44V	600µV	600µV	600µV
Input Bias Current	V_{CM} = V_{EE} to V_{CC} – 1V	3nA	3nA	3nA
	= V_{EE} + 44V	4µA	4µA	4µA
Input Offset Current	V_{CM} = V_{EE} to V_{CC} – 1V	200pA	200pA	200pA
	= V_{EE} + 44V	60nA	60nA	30nA
Offset Voltage Shift	V_{CM} = V_{EE} to V_{CC} – 1V	50µV	100µV	300µV
	= V_{EE} to V_{EE} + 44V	500µV	500µV	500µV
Open-Loop Gain	R_L = 10k	1000k	1000k	200k
Output Voltage (low)	No load	22mV	22mV	–14.978V
	I_{SINK} = 10mA	500mV	500mV	–14.5V
Output Voltage (high)	No load	2.978V	4.978V	14.978V
	I_{SOURCE} = 10mA	2.6V	4.6V	14.6V
Output Current	Source	12mA	22mA	24mA
	Sink	22mA	27mA	38mA
Supply Current per Amp		40µA	40µA	50µA

Going Over the Top

Key to the unique operation of the LT1490 is the input stage, shown in Figure 1. Similar to other rail-to-rail op amps, the LT1490 uses two input stages to achieve input rail-to-rail operation. Device Q7 controls which stage is active by steering the tail current between the two stages as a function of the input common mode voltage. The LT1490 has three modes of operation.

Mode 1: $V_{EE} < V_{CM} < V_{CC} - 1V$

For input common mode voltages between V_{EE} and V_{CC} – 1V, the PNP stage (Q5–Q6) is active, and Q7 and the NPN stage (Q1–Q4) are off. Since Q7 is off, 2µA of current flows through Q5–Q6. The input bias current is the base current of Q5 or Q6, typically 4nA, as shown in Figure 2. The input offset voltage for this stage is trimmed to less than 300µV.

Mode 2: $V_{CC} - 1V < V_{CM} < V_{CC}$

When the input common mode voltage reaches V_{CC} – 1V, Q7 turns on, diverting the current from Q5–Q6 to the NPN stage. When the PNP stage is completely off, 2µA flows through the 2× current mirror D3–Q8. The 4µA current through Q8 sets the bias for the NPN input stage. In this mode, Q1–Q2 act as emitter followers, driving a differential amplifier formed by Q3–Q4. The input bias current for this mode of operation is the base current of Q1 or Q2, typically 20nA.

When the common mode voltage reaches V_{CC} – 0.2V, Q1–Q2 begin to saturate due to the forward voltage of D1–D2, as shown in Figure 2. This

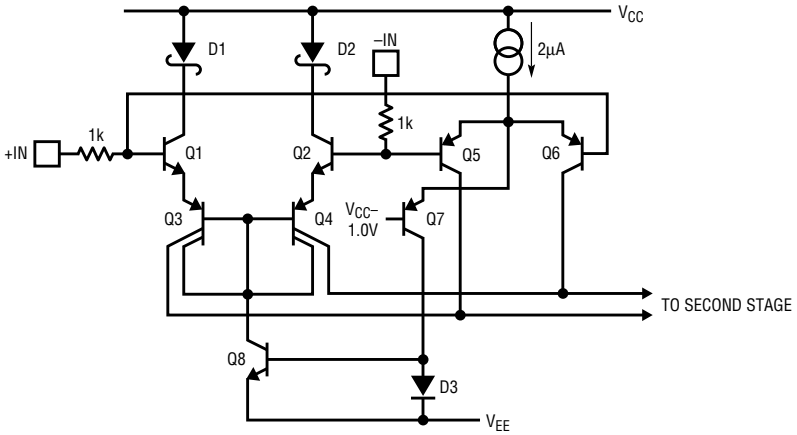

Figure 1. LT1490 input stage

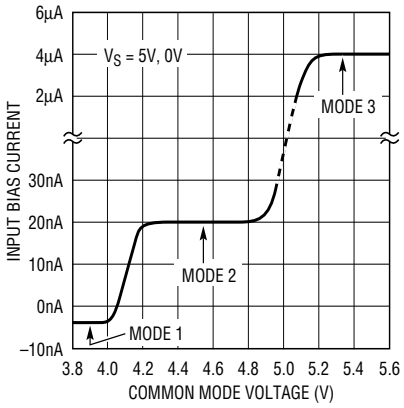

Figure 2. Input bias current characteristics over all three modes of operation

causes the input bias current to increase. At $V_{CM} = V_{CC}$ the input bias current is typically 200nA. The input offset voltage of the NPN stage is not trimmed, but is typically 600µV.

Mode 3: $V_{CC} < V_{CM} < V_{CC} + 44V$

As Figure 2 shows, when $V_{CM} = V_{CC}$ the NPN input stage is beginning to saturate but is not yet fully saturated. When V_{CM} is approximately equal to V_{CC} + 0.2V, Schottky diodes D1–D2 reverse bias, causing Q1–Q2 to fully saturate. In this condition, the base current of Q1–Q2 is equal to the emitter current, typically 4µA. The Schottkys, in combination with special geometries for the input devices Q1–Q2, are the key to the unique above-the-rail operation of the LT1490. The input offset voltage for this mode of operation is typically 600µV.

Reverse Battery Protection

The LT1490 can withstand reverse supply voltages of up to 25V. The inputs are also protected for excursions below V_{EE}. The protection consists of a 1k resistor in series with each input, which limits the current through the associated substrate diode. The part will not be damaged if the current through the substrate diode is less than 10mA.

An Over-the-Top Application

The battery current monitor circuit shown in Figure 3 demonstrates the LT1491's ability to operate with its inputs above the positive supply rail. In this application, a conventional amplifier would be limited to a battery voltage between 5V and ground, but the LT1491 can handle battery voltages as high as 44V. The LT1491 can be shut down by removing V_{CC}. With V_{CC} removed the input leakage is less than 0.1nA. No damage to the LT1491 will result from inserting the 12V battery backward.

When the battery is charging, Amp B senses the voltage drop across RS. The output of Amp B causes QB to drain sufficient current through RB to balance the inputs of Amp B. Likewise, Amp A and QA form a closed loop when the battery is discharging. The current through QA or QB is proportional to the current in RS; this current flows into RG, which converts it back to a voltage. Amp D buffers and amplifies the voltage across RG. Amp C compares the output of Amp A

continued on page 22

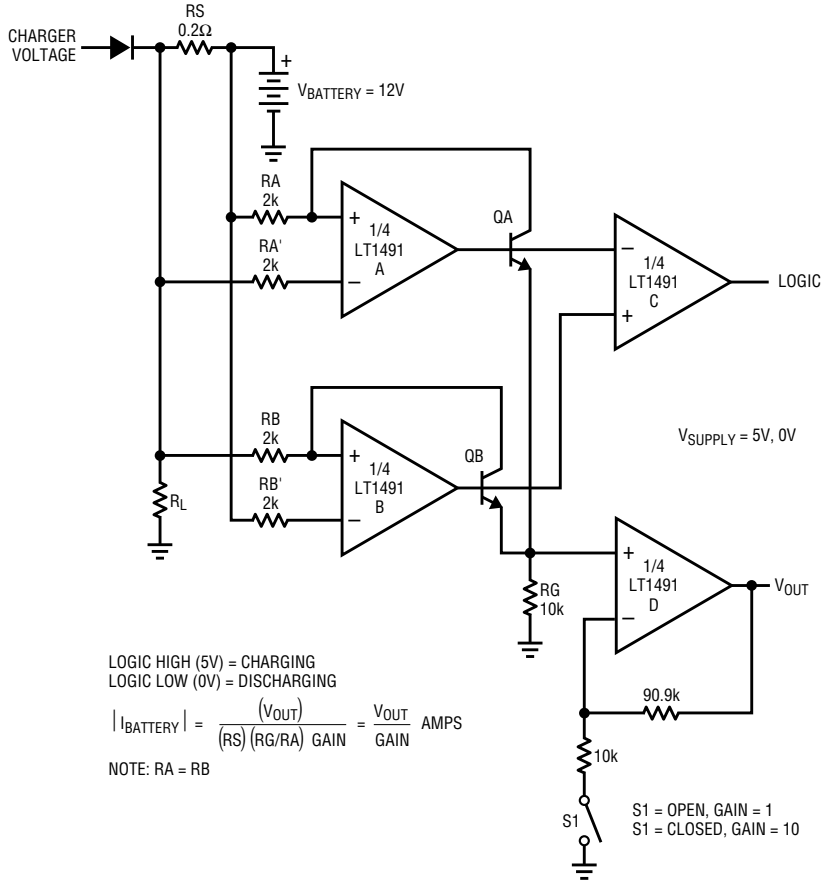

Figure 3. LT1491 battery current monitor—an "over-the-top" application

LT1512/LT1513 Battery Chargers Operate with Input Voltages Above or Below the Battery Voltage

by Bob Essaff

Introduction

The LT1512 and LT1513 form a unique family of constant-current, constant-voltage battery chargers that can charge batteries from input voltages above or below the battery voltage. This feature can help simplify system design and add product flexibility by allowing battery charging from multiple sources, such as a wall adapter, a 12V automotive system or a 5V power supply, all with the same circuit. The constant-current, constant-voltage architecture makes the LT1512 and LT1513 well suited for charging NiCd, NiMH, lead-acid or lithium-ion batteries.

Both devices are current mode switching regulators that operate at a fixed frequency of 500kHz. Product features include a ±1% reference-voltage tolerance, 2.7V minimum input voltage, easy external synchronization and 12µA supply current in shutdown mode. The LT1512 and LT1513 also include low loss on-chip power switches rated for 1.5 Amps and 3 Amps respectively. High frequency switching allows the use of small surface mount inductors and capacitors, and the battery can be directly grounded.

Operation

The LT1512 and LT1513 are specifically optimized to use the SEPIC converter topology, which is shown in Figure 1's typical application. The SEPIC (single-ended primary inductance converter) topology has several advantages for battery-charging applications. It will operate with input voltages above or below the battery voltage, has no path for battery discharge when turned off, and eliminates the snubber losses of flyback designs. It also has a current sense point that is ground referred and need not be connected directly to the battery. The two inductors shown are actually two identical windings on one inductor core, although two separate inductors can be used.

The LT1512 and LT1513 form a unique family of constant-current, constant-voltage battery chargers that can charge batteries from input voltages above or below the battery voltage. This feature can help simplify system design and add product flexibility...

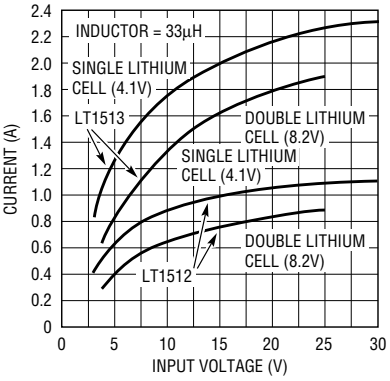

Figure 2. Maximum charging current

The topology is essentially identical to a 1:1 transformer-flyback circuit except for the addition of capacitor C2, which forces identical AC voltages across both windings. This capacitor performs three tasks: it eliminates the power loss and voltage spikes usually caused by a flyback-converter's leakage inductance; it forces the input current and the current in resistor R3 to be a triangle wave riding on top of a DC component instead of forming a large amplitude square wave; and it eliminates the voltage spikes across the output diode when the switch turns on.

When the battery is below its float voltage, set by R1 and R2, the charger is in the constant-current mode. The suggested value for R2 is 12.4k. R1 is calculated from:

$$R1 = \frac{V_{OUT} - 1.245}{\frac{1.245}{R2} + (3 \times 10^{-7})}$$

where V_{OUT} = battery float voltage

Charging current in the battery, which also flows through R3, develops a voltage on the I_{FB} pin. The I_{FB} pin's 100mV sense voltage sets the

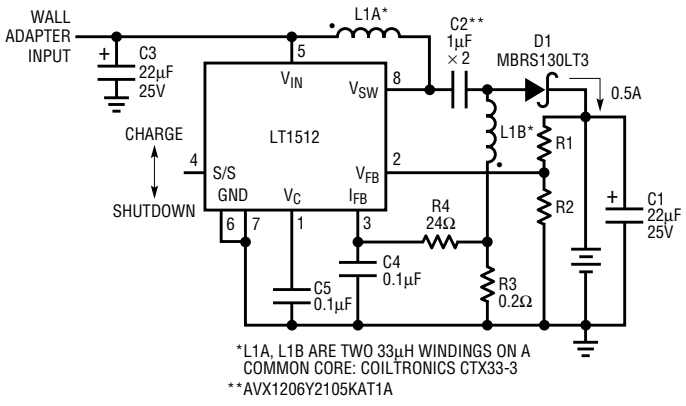

Figure 1. Battery charger with 0.5A output current

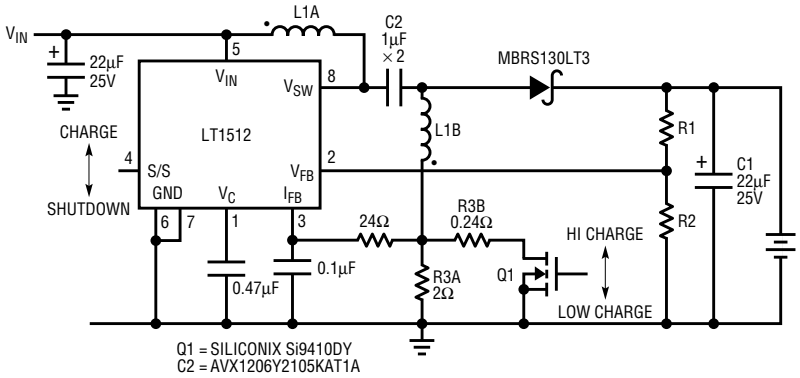

Figure 3. 50mA/400mA programmable battery charger

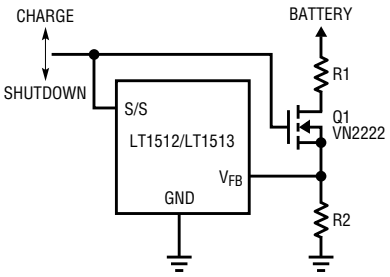

Figure 4. Shutdown controlled disconnect

programmed charging current to I_{CHG} = 100mV/R3. The RC filter formed by R4 and C4 smoothes the signal presented to the I_{FB} pin.

Charging current remains constant until the battery reaches its float voltage, at which point the LT1512/LT1513 changes to the constant-voltage mode. In this mode, the charging current will taper off as required to keep the battery at its float voltage. The circuit's maximum input voltage is partly determined by the battery voltage. When the switch is off, the voltage on the V_{SW} pin is equal to the input voltage, which is stored across C2, plus the battery voltage. Both the LT1512 and LT1513 have a maximum input voltage rating of 30V and a maximum rated switch voltage of 35V, thereby limiting input voltage to 30V or 35V minus the battery voltage, whichever is less.

Figure 2 shows the maximum available charging current for a single-cell or double-cell lithium battery pack. Note that the actual programmed charging current will be independent of the input voltage if it does not exceed the values shown.

Programming the Charge Current

As mentioned earlier, charging current is set by R3, where I_{CHG} = 100mV/R3. The charge current is programmed by changing the effective value of R3, as shown in Figure 3. In the low charge mode, Q1 is off, setting charge current to $I_{CHG\ LOW}$ = 100mV/R3A, or 100mV/2Ω = 50mA. In the high-charge mode, Q1 is on, and charge current is $I_{CHG\ HI}$ = 100mV/R3A + 100mV/(R3B + Q1's $R_{DS(ON)}$), or 100mV/2Ω + 100mV/(0.24Ω + 0.04Ω)) = 50mA + 357mA = 407mA. Note that Q1's $R_{DS(ON)}$ is a factor in the high-charge mode, requiring the use of a low $R_{DS(ON)}$ FET.

Off-State Leakage

Charging can be terminated by placing the LT1512/LT1513 into shutdown mode. If the battery remains connected to the charger when in the off state, two leakage paths that load the battery must be considered.

The first is the 100µA resistor-divider feedback current that flows through R1 and R2. This current can be eliminated with the addition of a FET, Q1, between R1 and the R2/V_{FB} junction, as shown in Figure 4. In this example, pulling the charge/shutdown input above 3.75V will activate charging and turn on Q1, whereas driving the charge/shutdown input below 0.6V will shut down the LT1512/LT1513 and turn off Q1.

The second leakage path to consider is in the output diode, D1 (Figure 1). When the charger is in the off state, the output diode sees a reverse voltage equal to the battery voltage. Though the Schottky diode reverse leakage may typically be only 10µA, its guaranteed specifications are much worse, up to 1mA. One solution is to change the output diode to an ultra-fast silicon diode, such as an MUR-110. The higher forward voltage of the silicon diode will decrease the circuit's efficiency, but these diodes have reverse leakage specifications below 5µA.

Conclusion

With the ability to operate from input voltages above or below the battery voltage, the LT1512 and LT1513 battery chargers offer increased flexibility for portable systems.

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LTC1435–LTC1439, continued from page 6

The POR output can also help stage output voltages. For example, if the auxiliary regulator is on in Figure 5, the 2.9V output will come up simultaneously with the 3.3V output. In other applications, however, the POR output could be used to hold the AUX ON pin low, thus delaying the auxiliary start-up until POR releases.

EXT V_{CC} Pin Reduces Quiescent Current

Power for the top and bottom MOSFET drivers and for most of the other control circuitry is derived from the INT V_{CC} pin. When the EXT V_{CC} pin is open or at a low voltage, an internal 5V low dropout regulator supplies INT V_{CC} power from V_{IN}. If EXT V_{CC} is taken above 4.7V, the 5V regulator is turned off and an internal switch is turned on to connect EXT V_{CC} to INT V_{CC}.

The EXT V_{CC} pin is normally connected to the 5V output to allow INT V_{CC} power to be derived from the regulator itself. Quiescent current is then reduced because driver and control currents are scaled by a factor approximately equal to the 5V controller duty cycle. EXT V_{CC} can also be connected to other external high efficiency sources, up to a maximum of 10V.

In addition to the other features discussed above, most versions of the LTC143X family also contain an uncommitted comparator referenced to 1.19V with an open-drain output pin, useful in a wide variety of applications. The auxiliary regulator error amplifier is also usable as a second comparator.

Conclusion

The LTC1435–LTC1439 multiple output DC/DC controllers offer a tremendous amount of flexibility and functionality while removing many of the trade-offs that previously existed in battery-powered supplies. With these new controllers it is possible to have high efficiency and low quiescent current without giving up constant frequency operation, and to have low dropout without giving up N-channel MOSFETs. The wide variety of output voltage and current levels achievable using minimum magnetics makes these parts the logical choice for next-generation designs.

Editor's Page, continued from page 2

In this issue we introduce the LTC1439. This IC is a constant-frequency, synchronous, triple output DC/DC converter optimized for battery operated applications. The part (and its brethren) are the next-generation of ICs designed for the rapidly expanding portable computer and equipment marketplace. These devices were developed in conjunction with many customers and incorporate many requested features. We continue to highlight new products in the Design Features section. In this issue, we spotlight several new battery-charging products, including the LT1511, LT1512 and LT1513. Also featured are some new converter products, the LTC1446 and LTC1446L D-to-A converters, and the LTC1277 and LTC1273 A-to-D converters. Many other products are introduced in this issue. We also include our usual complement of circuit ideas and applications.

LT1511, continued from page 13

pin should be grounded if not used. When a microprocessor DAC output is used to control charging current, it must be capable of sinking current at a compliance up to 2.5V if connected directly to the PROG pin.

Conclusion

The LT1511 is a simple, cost effective solution for charging batteries at currents of up to 3A. Battery packs ranging from 1V to 20V can be charged, independent of their chemistry.

...a royally screwed-up circuit represents a learning opportunity...

—Derek Bowers

A circuit always works the way it is supposed to. It never disobeys any laws of physics...

—Tom Fredericksen

The circuit doesn't care about fair.

—Jim Williams

There is always a way out.

—George Philbrick

From *Analog Circuit Design: Art, Science and Personalities*. Edited by Jim Williams. Butterworth-Hienemann, 1991.

LT1490, continued from page 19

and Amp B to determine the polarity of the current through RS. The scale factor for V_{OUT} with S1 open is 1V/A. With S1 closed the scale factor is 1V/100mA, and current as low as 5mA can be measured.

Conclusion

The LT1490 provides features not previously available in an operational amplifier. The combination of "Over-the-Top" operation, reverse battery protection, micropower operation and MSOP package enables the LT1490/LT1491 to solve application problems beyond the reach of previous operational amplifiers.

LTC1518–LTC1520, continued from page 15

Other Features

- ❑ The part can be "hot swapped" without dragging the line down or causing latchup
- ❑ Output high with shorted or floating inputs
- ❑ Three-state outputs
- ❑ High input resistance (>20k) to allow multiple parallel receivers

Applications

The LTC1520 is designed for high speed data/clock transmission over short to medium distances. Its rail-to-rail input common mode range allows it to be driven via long PC board traces, coaxial lines or long (hundreds of feet) twisted pairs. It can be used in networking hubs, servers, routers, bridges, repeaters and other local-area and telecommunications switching networks. Figure 4 shows a typical LTC1520 application. The LTC1518/LTC1519, plannned for future release, are RS485 compatible (LTC488, LTC489 pin-for-pin compatible) high speed (50Mbit/s) line receivers. The high input resistance (>20k) allows more receivers to be connected on one line. The LTC1518/LTC1519 will conform to the expanded RS485 input common mode range (–7V to +12V), while providing nearly the same performance as the LTC1520.

Conclusion

The LTC1520 high speed, low power line receiver uses a unique architecture with propagation delay and skew performance unmatched by any CMOS, TTL or ECL line receiver/comparator. Its ruggedness, precise timing control and fault detection features make it easy to use in a wide variety of high speed data transmission applications.

LTC1446, continued from page 17

A Wide-Swing, Bipolar-Output DAC with Digitally Controlled Offset

Figure 4 shows how to use an LTC1446 and an LT1077 to make a wide bipolar-output-swing 12-bit DAC with an offset that can be digitally programmed. V_{OUTA}, which can be set by loading the appropriate digital code for DAC A, sets the offset. As this value changes, the transfer curve for the output moves up and down, as shown in the figure.

Conclusion

The LTC1446 and LTC1446L are the world's only DACs that offer dual 12-bit stand-alone performance in an 8-pin SO or PDIP package. Along with their amazing density, these DACs do not compromise on performance, offering excellent 12-bit DNL and very low power dissipation. This allows the user to use circuit board space very efficiently, without sacrificing performance.

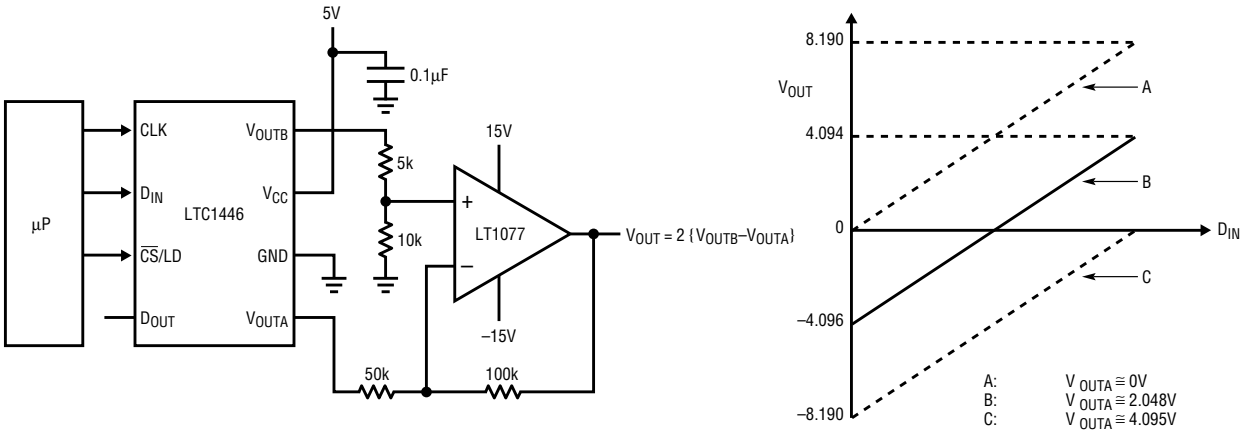

Figure 4. A wide-swing, bipolar output DAC with digitally controlled offset

500kHz Buck-Boost Converter Needs No Heat Sink

by Mitchell Lee

Thanks to an efficient 0.25W switch, the LT1371 SEPIC converter shown in Figure 1 operates at full power with no heatsink. Up to 9W at 5V output is available, and the circuit works over a wide range of input voltages extending from the LT1371's 2.7V minimum to 20V, limited by the rating of the capacitors.

A 1:1 bifilar-wound toroid is used as the magnetic element. A careful analysis showed that, in spite of the 500kHz operating frequency, a high permeability (μ_r = 125) Magnetics Inc. Kool Mμ® core exhibited the best efficiency when compared to powdered iron materials. Copper loss is minimized by the use of the high-perm Kool Mμ material, with only a slight core-loss penalty.

Maximum available output current varies with input voltage, and is shown (for 3A peak switch current) in Figure 2. Efficiencies for several input voltages are shown in Figure 3. At a 2.7V input, most of the loss is tied up in the LT1371 switch, whereas the output diode is the dominant source of loss with high inputs. Because these losses are small, surface mount construction provides adequate dissipation, eliminating the need for heatsinks.

In this application, the synchronization feature of the LT1371 is not used. When driven with an external clock signal at the shutdown/sync pin (S/S), the chip can be synchronized to any frequency between 600kHz and 800kHz.

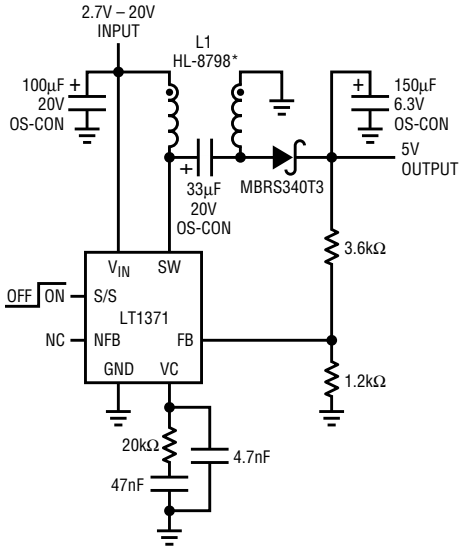

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Figure 1. 5V, 9W converter operates over wide input range with good efficiency.

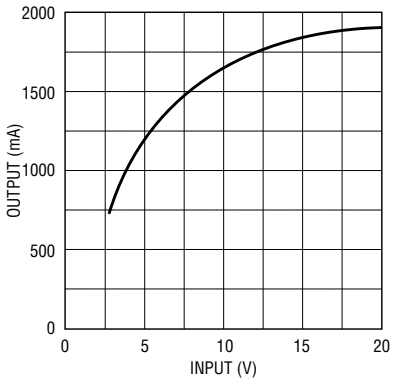

Figure 2. Maximum available output current

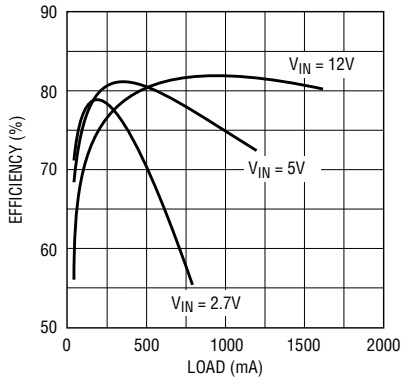

Figure 3. Efficiency of Figure 1's circuit

Kool Mμ is a registered trademark of Magnetics, Inc.

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Power Management and High Efficiency Switcher Maximize Nine-Volt Battery Life

by Vince Salvidio

The LTC1174 (3.3V, 5V and adjustable versions) can convert a 9V battery source to system power with very high efficiency. Efficiency is over 90% at load currents from 20mA to 425mA and over 85% at a load current of 4mA. For a given load, maximum battery life can be obtained by minimizing shutdown current during system shutdown and maximizing converter efficiency during operation. A single control line to the LTC1174 can be used to select shutdown mode or operational mode, as required.

For this circuit, power-up is initiated by a low level signal on the NAND gate. This signal could come from any front-panel switch or from an external interrupt signal. The system power is turned off by means of a low level signal from a controller/logic device. In either case, the control signal to the LTC1174 must be latched. (A latched turn-off signal ensures a known state on the LTC1174 shutdown pin during the collapse of the +5V supply.)

The CD4012 and CD4013 are powered from the battery; the 2N2222 provides simple level shifting to the battery rail. R1 and C1 ensure that the circuit remains in power-down mode during battery replacement. The circuit shown here provides approximately 90% efficiency at 250mA load current, and consumes less than 1µA shutdown current. Turn-on and turn-off transitions are very clean.

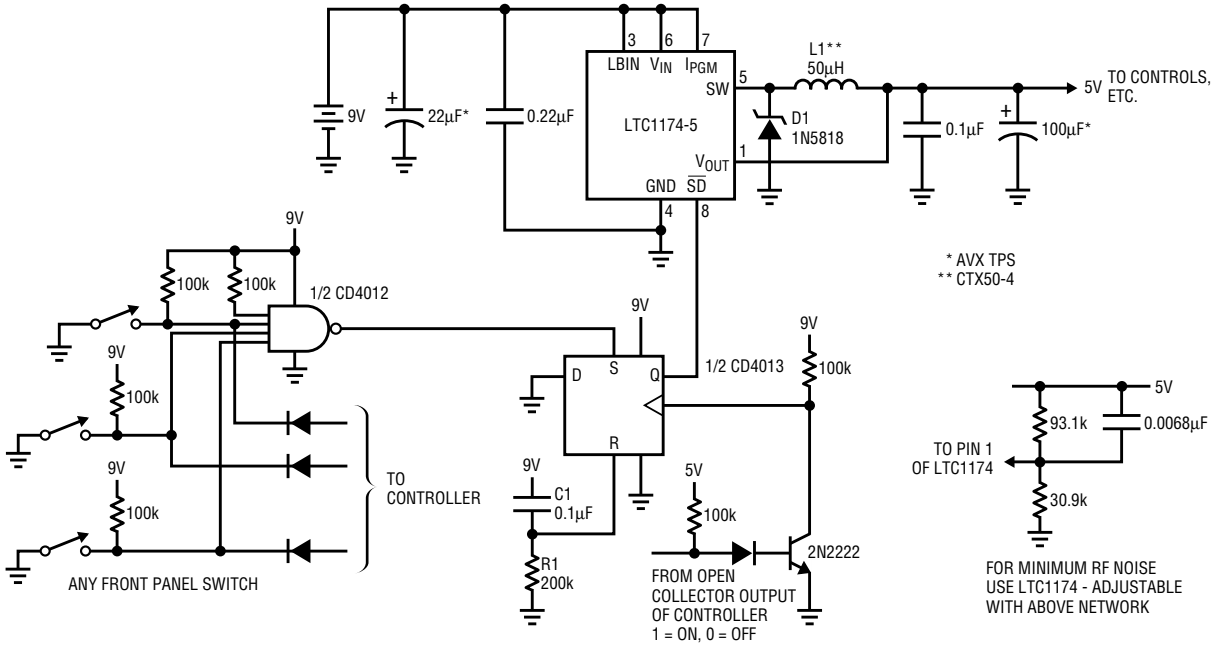


Figure 1. Schematic diagram, high efficiency DC/DC converter

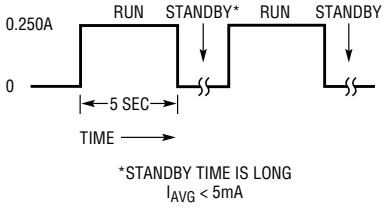


Figure 2. Load profile

Testing and Troubleshooting an IRDA Link Using the LT1319

by Frank Cox

Introduction

This Design Idea presents a complete infrared receiver that transforms modulated photodiode signals into digital levels. It is intended to facilitate the evaluation of the LT1319 infrared receiver building block in IR serial communication links. The circuit can be configured for IRDA SIR (InfraRed Data Association Serial InfraRed), IRDA FIR[1] (InfraRed Data Association Fast InfraRed) or Sharp/Newton modulations with the appropriate jumpers.

LT1319 Receiver Description

A block diagram of the LT1319 with the external filters for IRDA-SIR and Sharp/Newton is shown in Figure 1. This diagram is simplified for clarity and shows only the basic components for IRDA-SIR and Sharp modulations. The preamp is a low noise (2pA$\sqrt{Hz}$), high bandwidth (7MHz) current-to-voltage converter that transforms the photocurrent to a voltage. The 7MHz bandwidth supports data rates up to 4MBaud. The low noise allows for links of 2 meters or more. When full bandwidth is not required, sensitivity can be increased by reducing the noise further with a lowpass filter on the preamp output.

Encircling the preamp is a loop formed by GM1, C_{F1}, a buffer and R_{L1}. For low frequency signals, the loop forces the output of the preamp to the bias voltage (2V). High frequency signals are unaffected by the loop, so the preamp output is effectively AC coupled. The break frequency set by GM1, C_{F1} and the ratio of R_{FB} to R_{L1} is easily modified, since C_{F1} is a single capacitor to ground.

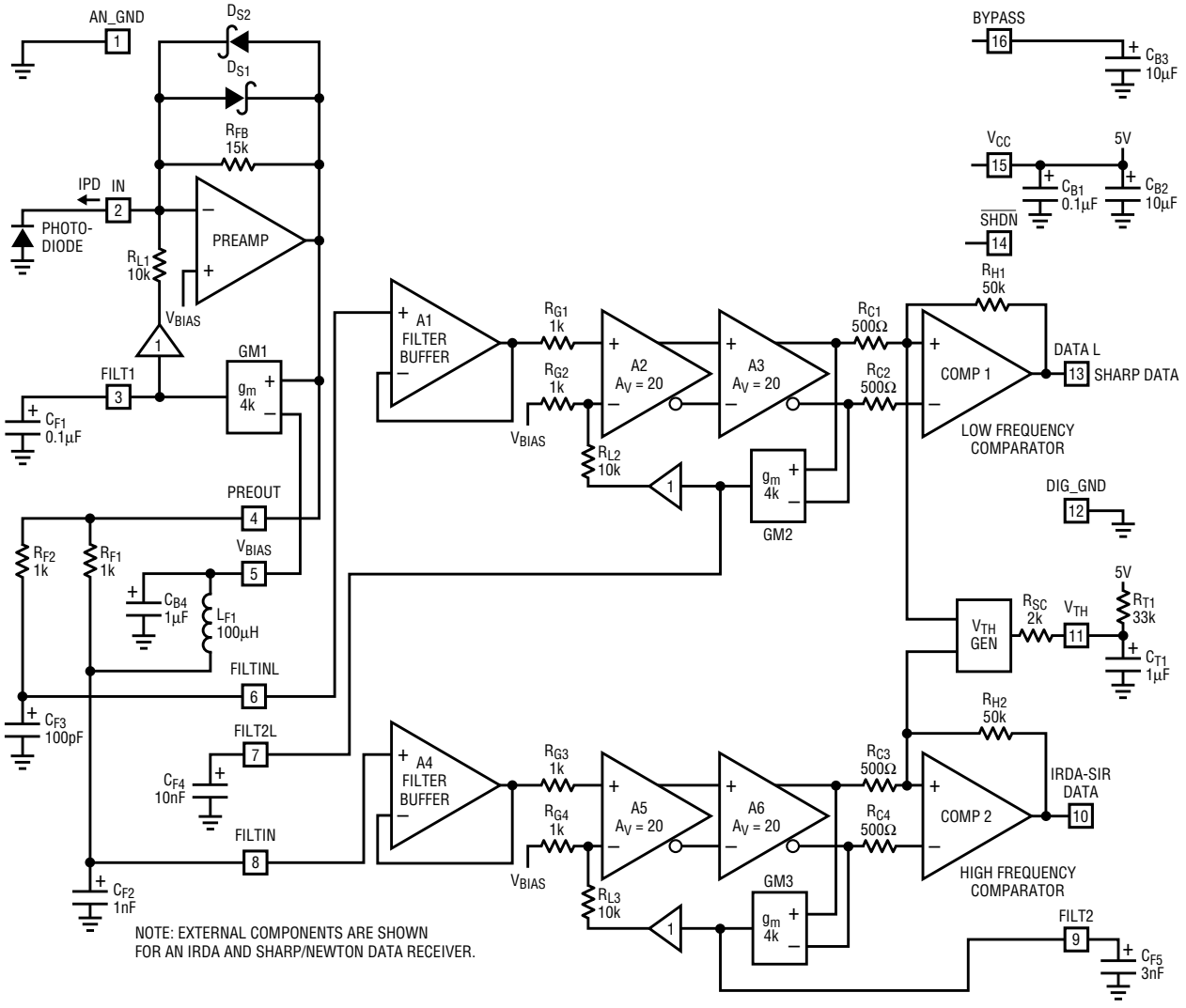


Figure 1. Block diagram of LT1319 with external filters for IRDA SIR and Sharp modulations

After the preamp stage there are two separate channels, each containing a high input impedance filter buffer, two gain stages with lowpass loops, and a comparator. The main difference between the channels is the response times of the comparators—25ns and 60ns. For modulation schemes with pulse widths down to 125ns, the 25ns comparator with its active pull-up output stage is ideal. The 60ns comparator with its open collector output and 5kΩ internal pull-up resistor is suitable for more modest speeds, such as the 1.6ms pulses seen with IRDA-SIR.

Buffers A1 and A4 allow the use of a wide range of external filtering options to optimize sensitivity and selectivity for specific modulation methods. The external components shown are a 4.8MHz lowpass for IRDA-SIR/FIR, formed by R_{F1} and C_{F2}, and a 500kHz LC tank circuit with a Q of 3 for Sharp/Newton, formed by R_{F2}, C_{F3} and L_{F1}.

The loops containing GM2 and GM3 surround the gain stages and function similarly to the preamp loop. They also provide accurate threshold setting at the comparator inputs by forcing the DC level of the differential gain stages to zero. The threshold is set by the current into pin 11, which is multiplied by 4 in the V_{TH} generator and then sunk through R_{C1} and R_{C3}. For an R_{T1} of 30kΩ the current into pin 11 is about 130µA. Referred to the filter buffer inputs, the comparator threshold is 0.65mV. The circuit has jumper-selected capacitors to optimize the AC loop highpass filters for the modulation in use. These and a squelch circuit are not shown here; for complete details see the LT1319 data sheet.

Other features of the LT1319 include a shutdown pin that reduces the supply current from a nominal 14mA to 500µA. The shutdown feature is active low. In this circuit, the supply current in shutdown mode also includes the current in the mode-selection jumpers, which can range from 0mA to 2mA.

To reduce false output transitions due to power supply noise, the preamp and gain stages have separate analog grounds and are operated off an internally regulated 4V supply bypassed at pin 16. The comparators, shutdown and threshold circuitry operate directly off the 5V supply and are returned to digital ground. To provide a low noise bias point for the amplifiers an internal 1.9V reference is generated and is bypassed externally at pin 5.

For more detailed information about the LT1319, consult the LT1319 data sheet.

Filtering

For IRDA-SIR modulations, the preamp AC loop is set for a corner frequency of less than 1kHz and the RC lowpass section after the preamp is set for a break frequency of 4.8MHz. The AC loop highpass on the gain stage for the fast frequency comparator is set at 400kHz for SIR and 2.5MHz for FIR.

The low speed channel has an LC tank circuit with a center frequency of 500kHz and a Q of 3, which is set by R_{F2}. This forms a bandpass filter for signals using the Sharp modula-

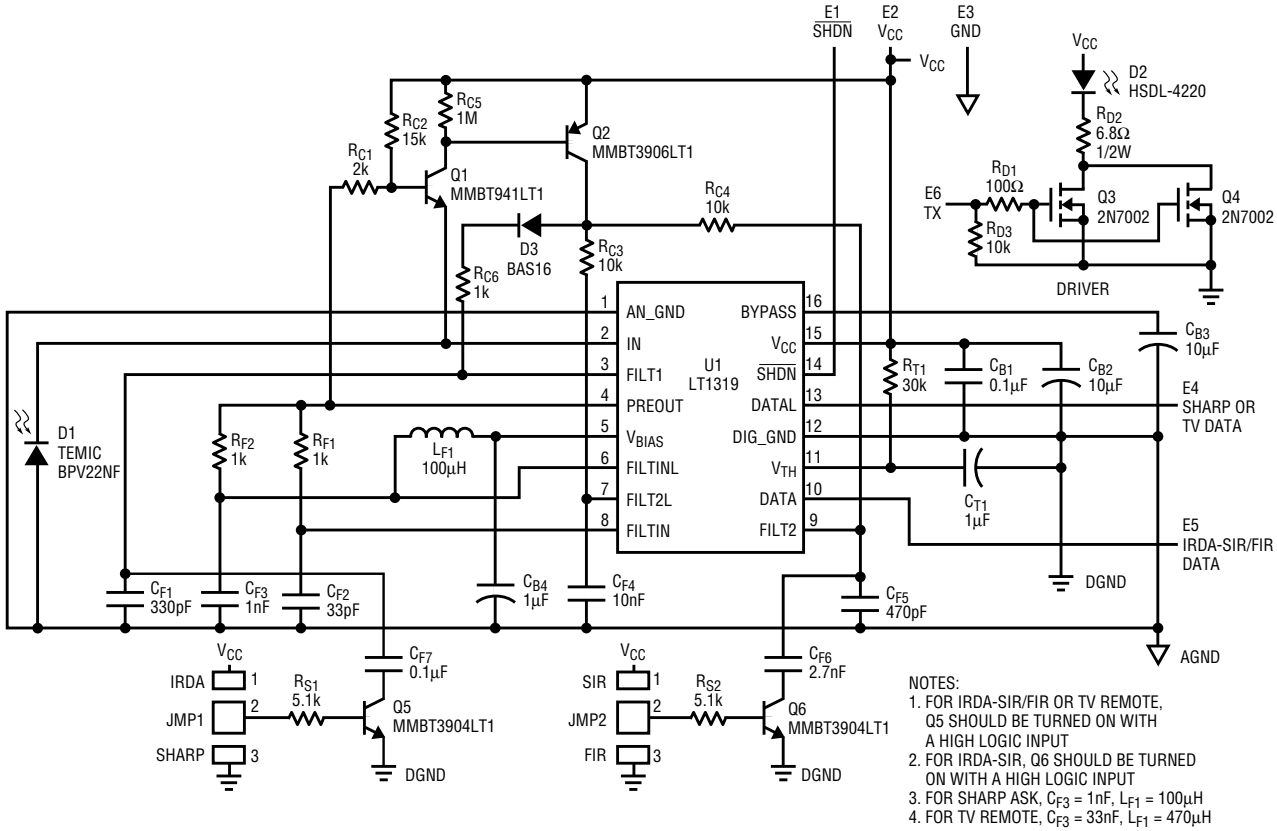


Figure 2. Schematic diagram

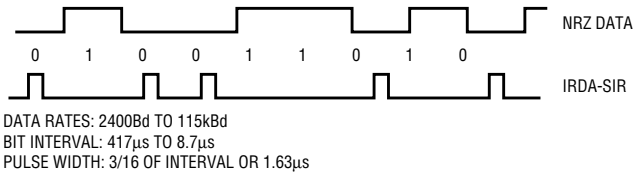
tion. The preamp AC-loop highpass corner is set to about 200kHz by C_{F1} and the gain stage highpass is set to 130kHz.

Operation

The most straightforward way of evaluating IR links with the LT1319 infrared receiver is to have a separate LED transmitter, such as that shown in the upper right-hand corner of Figure 2, that can be placed a measured distance from the receiver. The pulses to drive this transmitter can be obtained from a suitable pulse generator that has a TTL output, or from the system that will use the IR link, if available. Use coax cable and place a suitable termination on the input of the transmitter board to ensure good pulse fidelity.

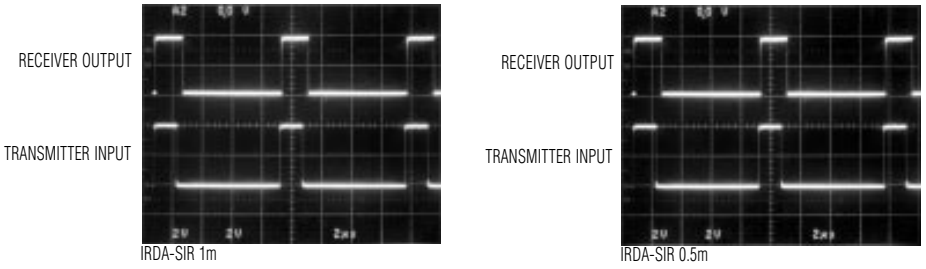
The onboard jumpers should be set for the modulation desired. For example, for IRDA-SIR modulation set the IRDA/Sharp jumper to the IRDA side and the SIR/FIR jumper to the SIR side. Connect an oscilloscope to the appropriate output of the circuit and apply a 5V power source capable of supplying greater than 25mA to the E2 (V_{CC}) and E3 (GND) terminals. Set the transmitter close to the receiver (~10cm), input an appropriate modulated signal to E4 or E5, and verify the basic operation of the receiver using the modulation photographs (Figures, 3, 4 and 5) as a guide.

From here you can test the receiver over the desired range, transmitter power, angle of incidence or whatever. It is helpful to set up a space for an optical range that is clear of obstacles, reflections and interference. Later, when the basic operation of the IR link is established, the receiver can be tested against any interference that the final system may encounter. For more sophisticated testing a bit-error-rate test (BERT) set is usually required, as are the circuits to modulate and demodulate the digital signals.

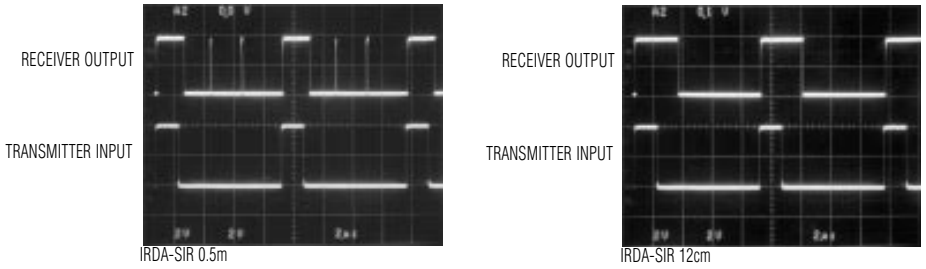


DATA RATES: 2400Bd TO 115kBd
BIT INTERVAL: 417µs TO 8.7µs
PULSE WIDTH: 3/16 OF INTERVAL OR 1.63µs

(3a)

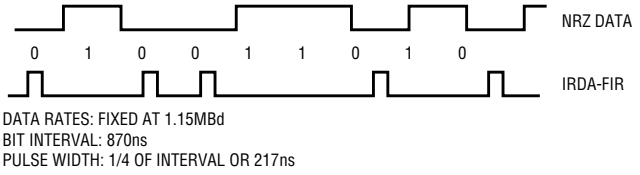


(3b) **(3c)**



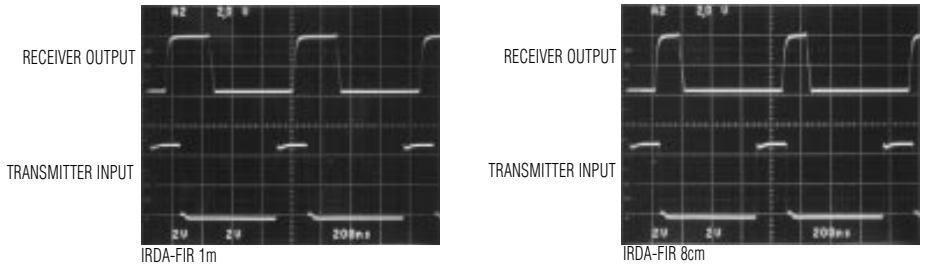
(3d) **(3e)**

Figure 3. IRDA-SIR modulation



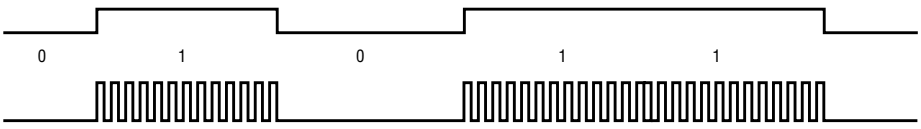
DATA RATES: FIXED AT 1.15MBd
BIT INTERVAL: 870ns
PULSE WIDTH: 1/4 OF INTERVAL OR 217ns

(4a)



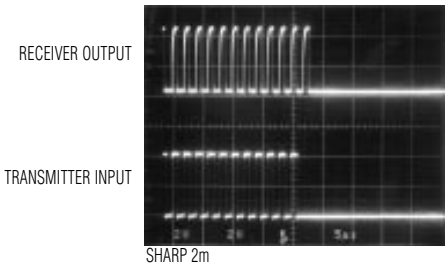
(4b) **(4c)**

Figure 4. IRDA-FIR modulation

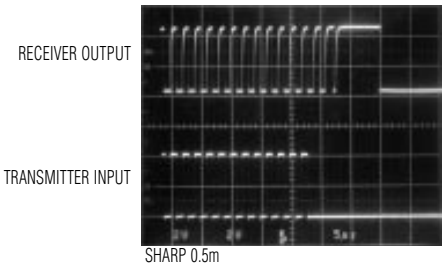


DATA RATE: 9600Bd TO 38.4kBd
AMPLITUDE SHIFT KEYING ON 500kHz CARRIER
A ONE IS ENCODED AS A BURST FROM 52 CYCLES
TO 13 CYCLES OF THE CARRIER DEPENDING ON THE MODULATION RATE

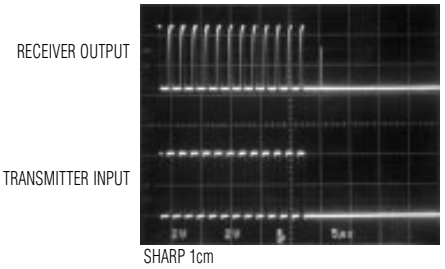
(5a)



(5b)



(5c)



(5d)

Figure 5. Sharp modulation

IRDA-SIR

Because SIR systems transmit a pulse for a zero and nothing for a one (refer to the IRDA-SIR modulation diagram, Figure 3a), the four photographs demonstrating the SIR modulation show a sequence of zeros. In all these photographs the input data to the transmitter is shown on the bottom and the output of the IR receiver is shown on the top. The Figures 3b and 3c show received data at 1m and 0.5m. The only difference is a slight increase of the received pulse width, which presents no problem.

The third photograph of data from a range of 0.5m (Figure 3d) shows extraneous narrow pulses caused by interference from the Sharp data output of the circuit. Because of the sensitivity of the LT1319, transitions on this output can couple back into the receiver. This problem can be avoided either by shielding this output or, if it is not to be used, tying it to ground.

The last photograph in the sequence (Figure 3e) shows receiver data from a range of 12cm. As the range is decreased from 1m the pulse width on the output increases, reaching a maximum at this point. Here, a squelch circuit (see data sheet for operational details) takes over. Eventually, at very close range, the squelch is overwhelmed and the pulse width begins to widen again, but at no time should the pulse be wider than 8ms over the full IRDA range of 1cm to 1m.

IRDA-FIR

With the exception of data rate and pulse width, FIR is very similar to SIR (refer to the FIR modulation diagram—Figure 4a). The same precautions about interference from the other output apply to both FIR and SIR. The first FIR photograph shows the receiver output at a range of 1m. The output pulse is slightly wider than the input, but this is acceptable. As the range is decreased, the pulse width narrows until about 8cm, where it reaches a minimum. Further decreasing the range causes the pulse to widen, but to no more than 800ns over the IRDA-FIR operating range of 1m to 4cm.

Sharp

Sharp IR modulation encodes a one as a burst of 500kHz square waves and a zero as nothing (refer to the Sharp modulation diagram, Figure 5a). The photographs show a one followed by a zero pattern at a modulation rate of 38.4kHz (13 cycles of carrier). The first photograph (Figure 5b) shows data received at a range of 2m. Note that there are 14 pulses in the received burst. An LC tank bandpass circuit is used to filter the Sharp modulation in Figure 1's circuit. Ringing in the time-domain response of this filter causes the receiver output to have extra pulses or be otherwise distorted. The next photograph (Figure 5c), showing data received at 0.5m, has the most pulse distortion. However, the output still does not intrude into the next bit interval enough to obscure the difference between a one or a zero. To ensure correct demodulation, a valid zero should have a minimum of 12 pulses. The last photograph (Figure 5d) shows the received data at 1cm, where filter ringing causes one extra pulse.

Conclusion

The infrared transmission of data between peripherals is in its infancy. As is usual in the computer world, every manufacturer wants to transmit as rapidly as possible. This article has presented methods of testing IR transmission via several modulation schemes. As the technology of IR data transmission matures, LTC will be at the forefront with applications support.

Note:

[1]The IRDA prefers the title "High Speed Extension to SIR" for this modulation.

The LTC1266 Operates From ≥12V and Provides 3.3V Out at 12A

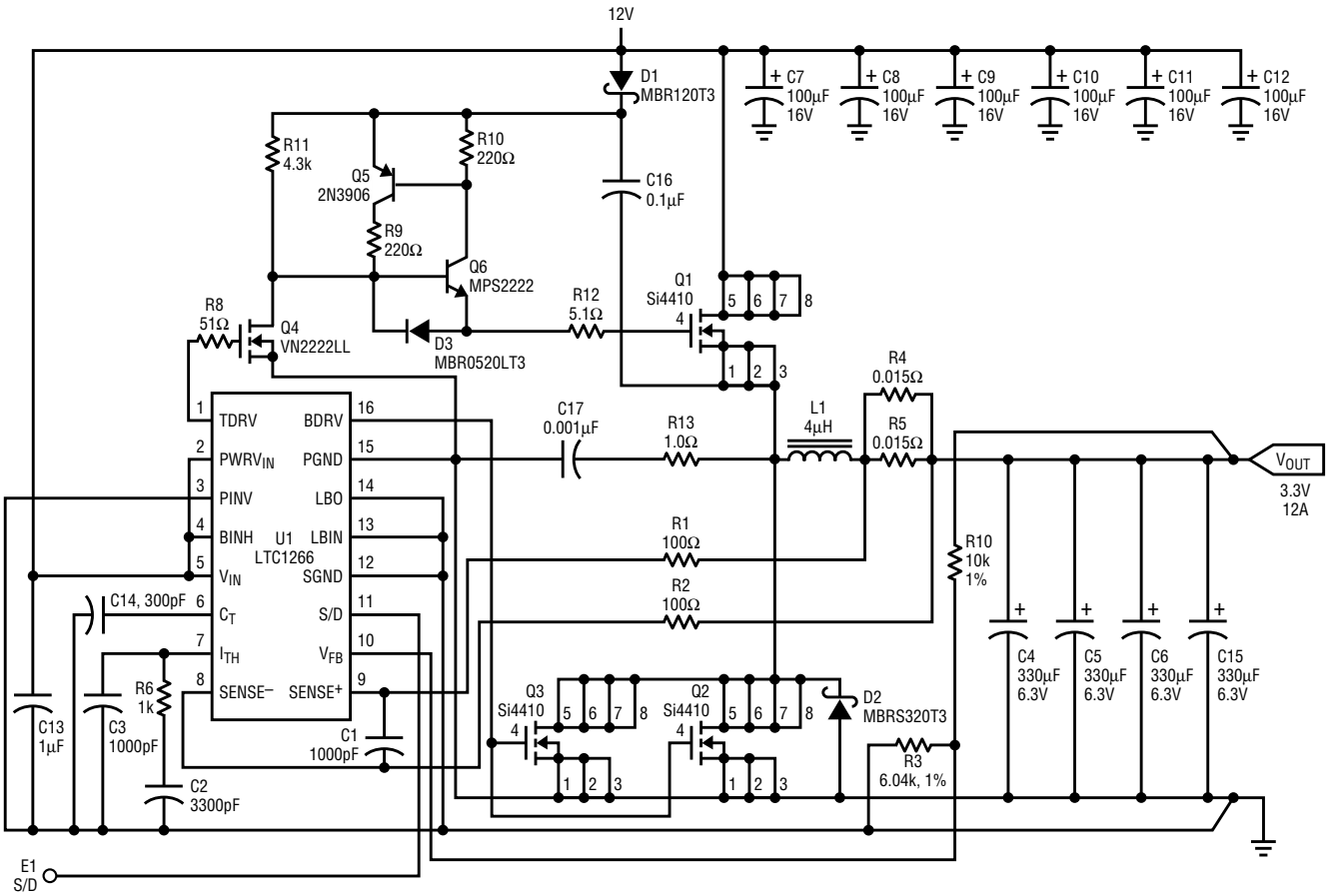
by Craig Varga

Introduction

The LTC1266 synchronous buck controller is specified for an absolute maximum voltage of 20V on either its V_{CC} input or its gate-drive supply. If it is acceptable to the designer to drive a P-type high-side MOSFET switch, the part will handle input voltages of up to 18V while providing reasonable design margin. However, if the output current is fairly high, making it desirable to use an N-type high-side MOSFET, the highest safe nominal input is approximately 11V. If 5V is also available, a bootstrap circuit can be used to provide high-side gate drive while maintaining adequate design margin on the gate-drive supply. However, if still higher input voltages are to be used reliably, this approach will no longer prove adequate. The simple, low-cost circuits presented here solve this problem, adding an incremental cost that is probably less than the cost difference between N- and P-type FETs.

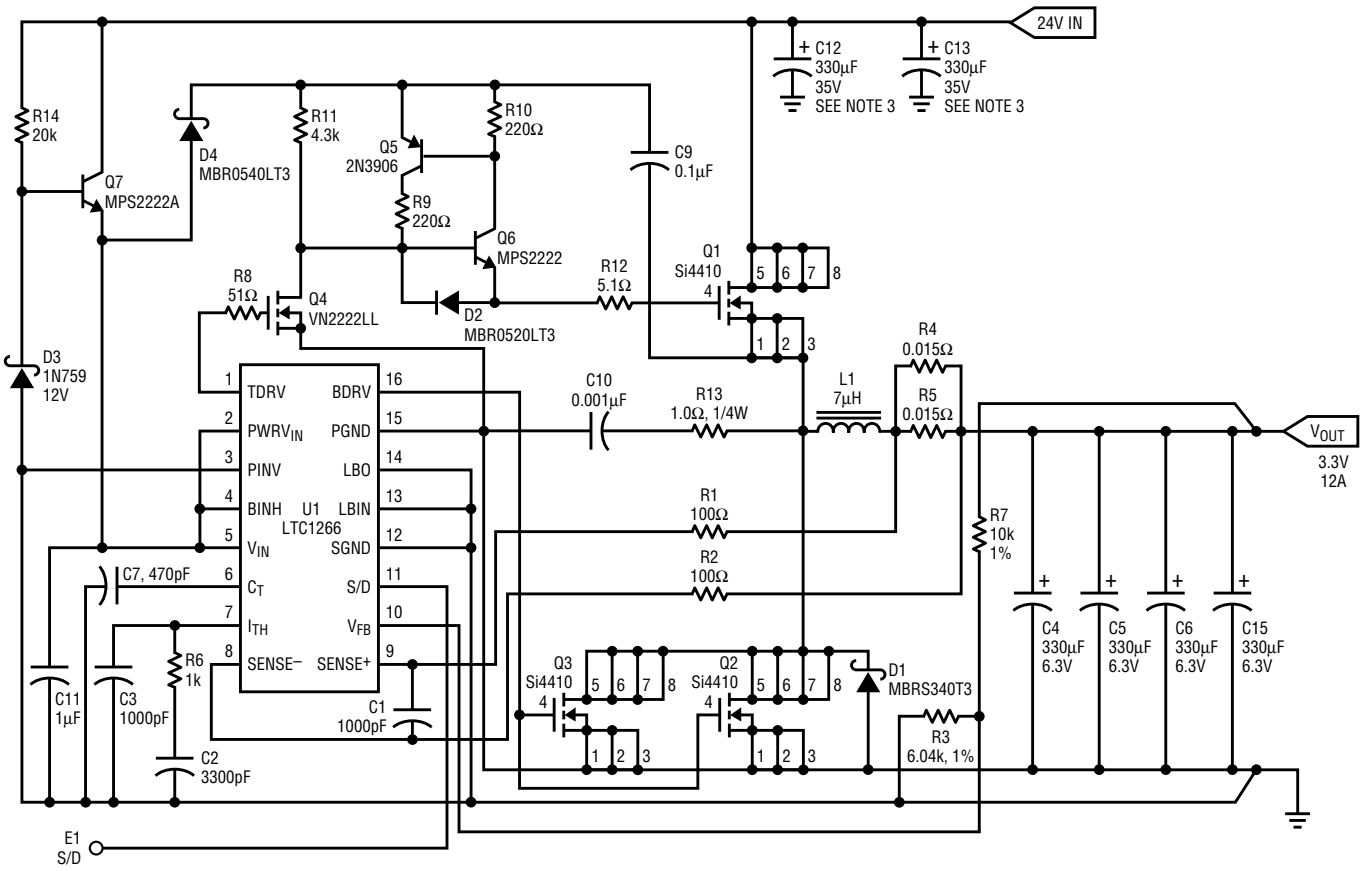
Circuit Description and Operation

The design in Figure 1 relies on a floating high-side driver that provides enough gate-drive capability to easily switch a large power MOSFET. The LTC1266 is configured to drive a P-channel MOSFET by tying pin 3 (PINV) to ground. This is required because there will be a net inversion by the floating driver. Q4 controls the driver stage and provides gate-discharge capability through D3. When the low-side switches are on, C16 charges to 12V through D1. When the LTC1266 signals Q1 to turn on, Q4 is turned off. R11 provides base current for Q6, which, in conjunction with Q5, acts like an SCR. Once fired, the regenerative behavior of Q5 and Q6 rapidly charges the gate of Q1. Since C16 is referenced to the source of Q1, the top of C16 rises above the 12V supply rail as Q1 turns on, forcing



1. ALL POLARIZED CAPACITORS ARE AVX TYPE TPS OR EQUIVALENT

Figure 1. 12V in to 3.3V out at 12A



1. ALL POLARIZED CAPACITORS ARE AVX TYPE TPS OR EQUIVALENT UNLESS NOTED OTHERWISE.
2. L1 CONSISTS OF 15 TURNS OF #16 AWG ON MAG. INC. 77848-A7 Kool Mµ CORE
3. C12 AND C13 ARE PANASONIC TYPE HF OR EQUIV.

Figure 2. 24V in to 3.3V out at 12A

the gate of Q1 to nearly 24V above ground. When the LTC1266 takes pin 1 high, Q4 turns on, pulling charge from the gate capacitance of Q1 through D3. This back biases the base-emitter junction of Q6, forcing the pull-up circuit, and therefore Q1, off.

Since the input voltage is high relative to the output, the nominal duty factor of the high-side switch is small (in this case approximately 31%). As a result, the RMS current through Q1 is relatively low. By contrast, the low-side switches are on nearly 70% of the time, and therefore see a much higher RMS current. This explains why the low-side switch employs two MOSFETs, whereas the high-side switch uses only one. Schottky diode D2 is used to help keep the body diodes of Q2 and Q3 from turning on during the short dead time before switching transitions. These body diodes exhibit relatively long reverse recovery times, contributing to commutation losses. The Schottky diode improves overall efficiency several percent, but the circuit will function correctly without it. Switching losses in the two low-side switches are nearly zero, since these devices are turned on and off into nearly zero volts (the forward drop of the Schottky).

There is no fundamental limitation on how high the maximum input voltage can be with this approach. The drive level shift is limited by the breakdown rating of Q4. Obviously, the power transistors and input capacitors must be rated for the intended input voltage. A low power 12V supply is needed to provide power for the LTC1266 and voltage for the bootstrap supply. Figure 2 shows a 24V input design. As the input supply voltage is increased, one thing to watch for is the potential for overlap in the high- and low-side turn-on/turn-off transitions. The LTC1266 is designed to prevent shoot-through by actually waiting until the gate voltage of one switch is low before allowing the other switch to be turned on. Using the floating driver defeats this capability, so this condition must be checked for. The high-side drive turn-on time may be reduced by lowering the value of R11. Using a larger device for Q4 will speed up the turn-off transition. The value of C16 may also need to be a bit larger if R11 is reduced to limit drooping of the bootstrap supply voltage.

±12 Volt Output from the LT1377

by John Seago

Many applications use positive and negative voltages, with only one voltage requiring tight regulation. Often, cost and board space are more important than regulation of the second output. An equal output of opposite polarity can be added to a boost configuration by means of a negative charge pump. This two-output configuration is shown in Figure 1. The 1MHz switching frequency of the LT1377 decreases required board space, and the availability of both positive and negative feedback amplifiers allows regulation of either positive or negative output.

In the circuit of Figure 1, the LT1377 with L1, D1, D2 and C6 make up a positive boost circuit. As the internal power switch in the IC turns on, the voltage at pin 8 goes low and energy is stored in inductor L1. When the power switch turns off, L1 transfers energy through diodes D1 and D2 to capacitor C6 and the positive output load. C6 supplies load current when the power switch is on. Resistors R2 and R3 provide feedback from the positive output. R1, C3 and C4 provide loop compensation. C1 is the input capacitor and C2 provides local decoupling for the IC.

The charge pump consists of two capacitors, two diodes and a small inductor. When the power switch turns off, L1 also replenishes the charge on C5, forward biasing D3. When the power switch turns on, the charge on C5 reverse biases D3, forward biases D4 and supplies energy to C7 and the negative output load. L2 attenuates capacitive current spikes. D2 was added so that the voltage drop across both D1 and D2 would be approximately equal to the sum of the voltage drops of D3, D4 and the saturation voltage of the power switch in the LT1377. This makes both output voltages approximately equal but opposite in polarity. D1 and D2 can be replaced with a single Schottky diode if equal outputs are not required.

Voltage and current waveforms of the internal power switch are shown in Figure 2. These measurements were taken at pin 8 of the LT1377 with the circuit powered from a 5V supply. Figure 3 shows the ripple voltage from each output. The high frequency spikes can be attenuated with a small LC filter if necessary.

The circuit of Figure 1 was intended to operate from a 5V supply and provide ±12V outputs at 100mA each. It operates over an input range of 4V to 10V and load current variations from 15mA to 100mA. The regulated positive output voltage remains constant for changes in the input voltage and load current, while the voltage of the unregulated negative output changes as shown in Figure 4. Line and load regulation of the unregulated output will improve with smaller changes of input voltage or load current.

A common requirement is for the positive output to regulate the majority of power while the negative output supplies a much smaller, unregulated bias current. Measurements taken on the test circuit of Figure 1 showed the unregulated –12V output had less than ±1% variation for a fixed 15mA load while the input voltage changed from 4V to 10V with a load current change of 15mA to 200mA on the regulated positive output.

Occasionally, it is more important to regulate the negative output than the positive output. The circuit in Figure 5 is the same as that shown in Figure 1, except feedback resistors R2 and R3 have different values and

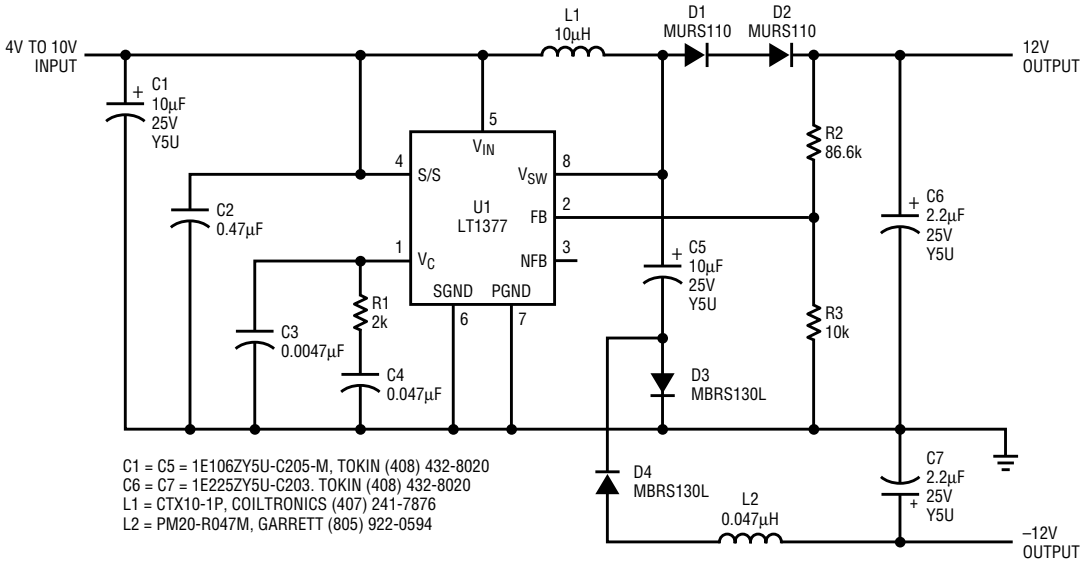


Figure 1. Positive output regulated supply

provide feedback from the negative output to the negative feedback amplifier of the LT1377. Figure 6 shows the variation in unregulated positive output for input voltage and load current variations.

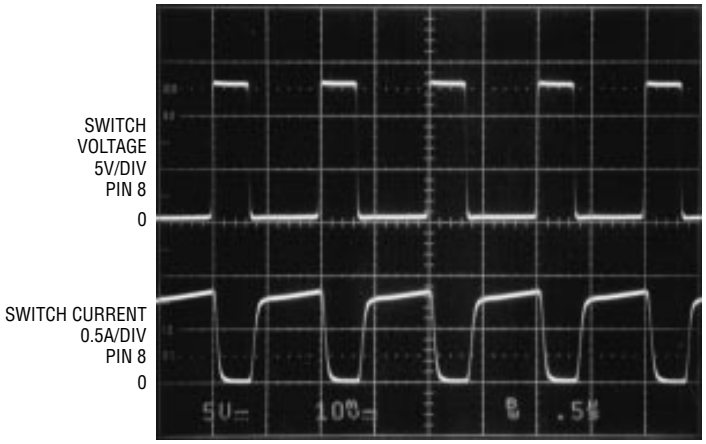


Figure 2. Switch voltage and current waveforms

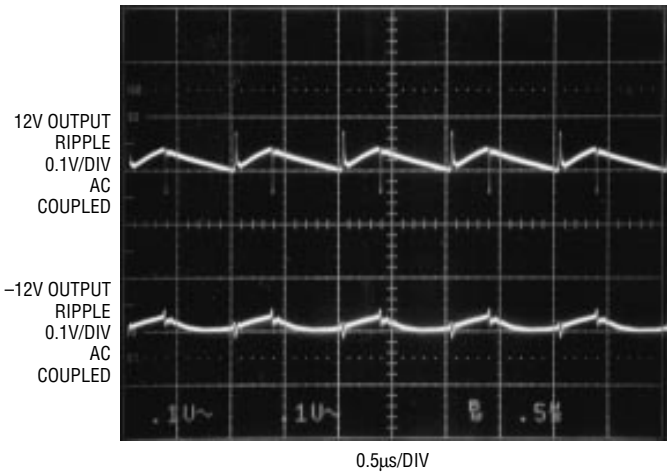


Figure 3. Output ripple voltage

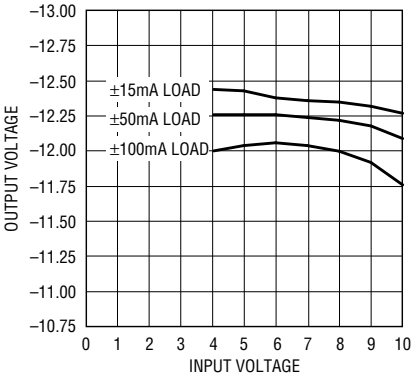


Figure 4. Unregulated negative output voltage with positive output voltage regulated

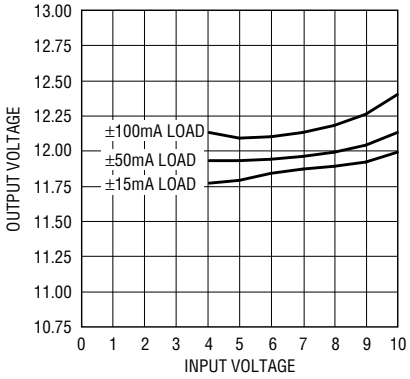


Figure 6. Unregulated positive output voltage with negative output voltage regulated

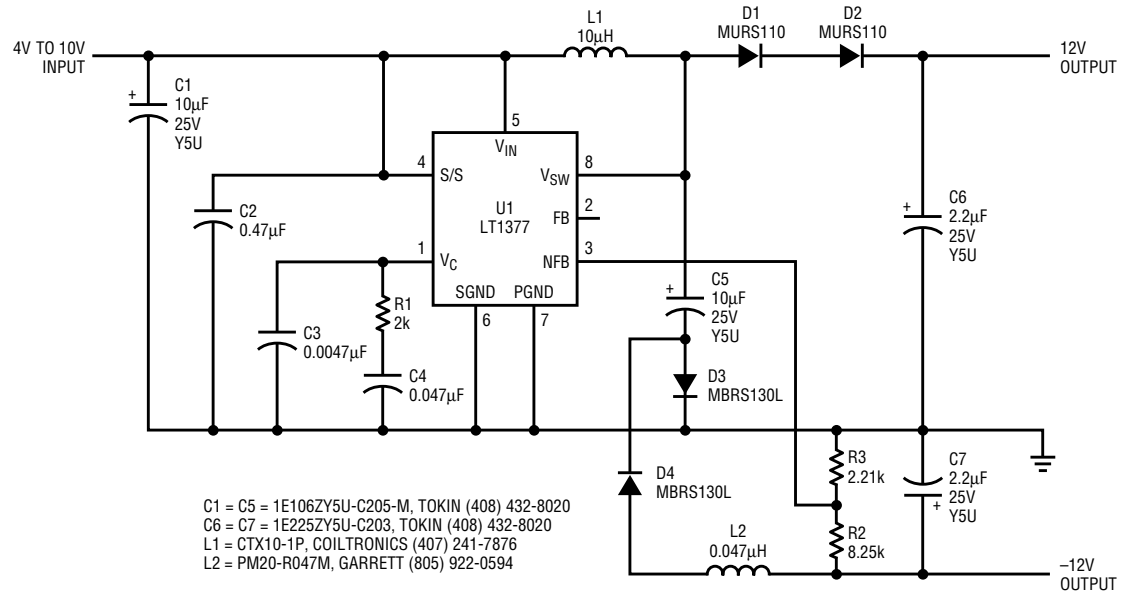


Figure 5. Negative output regulated dual supply

The LTC1516 Converts Two Cells to 5V with High Efficiency at Extremely Light Loads

by Sam Nork

Many battery-powered applications require very small amounts of load current from the regulated supply over long periods of time, followed by moderate load currents for short periods of time. In these types of applications (for example, remote data-acquisition systems, hand-held remote controls, and the like), the discharge rate of the battery is dominated by the overall current demands under low load conditions. In such low load systems, a primary source of battery drain is the DC/DC converter that converts the battery voltage to a regulated supply.

The circuit shown in Figure 1 converts an input voltage from two cells to 5V using a switched-capacitor charge-pump technique. An integral comparator on the LT1516 senses the output voltage and enables the charge pump as the output begins to droop. The charge pump's 2-phase clock controls the internal switching of flying caps C1 and C2. (See Figure 2.) On phase one of the clock, the flying caps are connected between V_{IN} and GND. On phase two, the negative plate of C1 is connected to V_{IN}, the negative plate of C2 is connected to the positive plate of C1, and the positive plate of C2 is connected to the output. During this phase of the clock, the potential on the top plate of C2 is approximately $3 \times V_{IN}$ and the charge is dumped from C2 onto the output cap to raise the output voltage. The repeated charging and discharging of C1 and C2 continues at a nominal frequency of 600kHz until the output voltage has risen above the internal comparator's trip point.

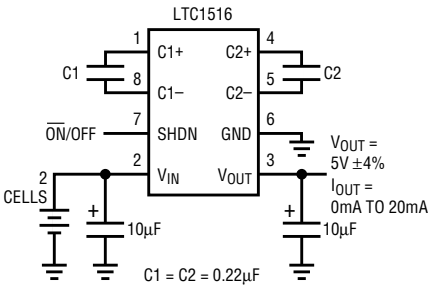


Figure 1. 2-cell to 5V converter

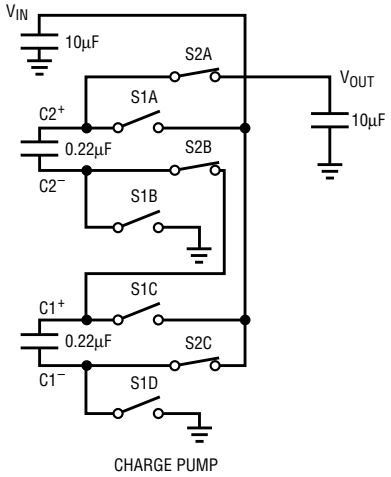


Figure 2. LT1516 charge pump in tripler mode, discharge cycle

When the battery cells are fully charged (approximately 1.5V per cell, for a nominal 3V V_{IN}), the circuit operates as a voltage doubler to maintain regulation. In doubler mode, only C2 is charged to V_{IN} and discharged onto V_{OUT} when the charge pump is enabled. As the batteries discharge and/or the load increases, the circuit will change from doubler mode to tripler mode. Under light load conditions, the part will remain in doubler mode until V_{IN} has dropped below 2.55V. Under heavier loads, the part will go into tripler mode at a higher V_{IN} to maintain regulation. By switching operating modes as the V_{IN} and the load conditions change, the LTC1516 optimizes overall efficiency for the life of the batteries. As shown in Figure 3, Figure 1's circuit achieves better than 70% efficiency with load currents from 50µA to 20mA for almost the entire life of the batteries.

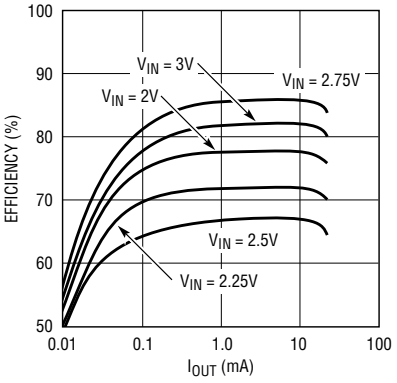


Figure 3. Efficiency versus V_{OUT} for Figure 1's circuit

Authors can be contacted at (408) 432-1900

Multichannel A/D Uses a Single Antialiasing Filter

by Sean Gold and
Kevin R. Hoskins

The circuit in Figure 1 demonstrates how the LTC1594's independent analog multiplexer can simplify the design of a 12-bit data acquisition system. All four channels are MUXed into a single 1kHz, fourth-order Sallen-Key antialiasing filter, which is designed for single-supply operation. Since the LTC1594's data converter accepts inputs from ground to the positive supply, rail-to-rail op amps were chosen for the filter to maximize dynamic range. The LT1368 dual rail-to-rail op amp is compensated for the 0.1µF load capacitors (C1 and C2) that help reduce the amplifier's output impedance and improve supply rejection at high frequencies. The filter contributes less than 1LSB of error due to offsets and bias currents. The filter's noise and distortion are less than –72dB for a 100Hz, $2V_{P-P}$ offset sine input.

The combined MUX and A/D errors result in an integral nonlinearity error of ±3LSB (maximum) and a differential nonlinearity error of ±3/4LSB (maximum). The typical signal-to-noise plus distortion ratio is 68dB, with approximately –78dB of total harmonic distortion. The LTC1594 is programmed through a 4-wire serial interface that allows efficient data transfer to a wide variety of microprocessors and microcontrollers. Maximum serial clock speed is 200kHz, which corresponds to a 10.5kHz sampling rate

The complete circuit consumes approximately 800µA from a single 5V supply. For ratiometric measurements, the A/D's reference can also be taken from the 5V supply. Otherwise, an external reference should be used.

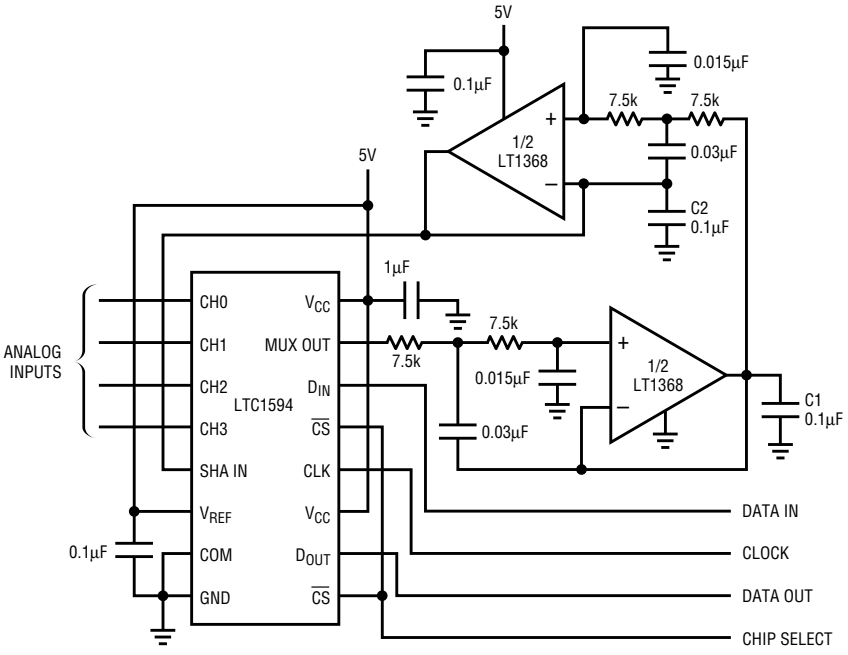


Figure 1. Simple data acquisition system takes advantage of the LTC1594's MUX OUT/SHA IN loop to filter analog signals prior to A/D conversion

Simple Resistive Surge Protection for Interface Circuits

by Bryan Nevins

Surges and Circuits

Many interface circuits must survive surge voltages such as those created by lightning strikes. These high voltages cause the devices within the IC to break down and conduct large currents, causing irreversible damage to the IC. Engineers must design circuits that tolerate the surges expected in their environments. They can quantify the surge tolerance of circuitry by using a surge standard. Standards differ mainly in their voltage levels and wave forms. At LTC, we test surge resistance using the circuit of Figure 1. We describe the voltage wave form (Figure 2) by its peak value V_P, the "front time" T_F (roughly, the rise time), and the "time to half-value" $T_{1/2}$ (roughly, the time from the beginning of the pulse to when the pulse decays to half of V_P). Surges are similar to ESD, but challenge circuits in a different way. A surge may rise to 1kV in 10ms, whereas an ESD pulse might rise to 15kV in only a few ns. However, the surge lasts for more than 100ms, whereas the ESD pulse decays in about 50ns. Thus, the surge challenges the power dissipation ability of the protection circuitry, whereas the ESD challenges the turn-on time and peak current handling. The Linear Technology LT1137A has on-chip circuitry to withstand ESD pulses up to 15kV (IEC 801-2). This circuitry also increases the surge tolerance of the LT1137A relative to a standard 1488/1489.

Designing for Surge Tolerance

Many designers enhance the surge tolerance of a circuit by placing a transient voltage suppressor (TVS) in parallel with the vulnerable IC pins, as shown in Figure 3. The TVS contains Zener diodes, which break down at a certain voltage and shunt the surge current to ground. Thus, the TVS clamps the voltage at a level safe for the IC. The TVS, like any protection circuitry increases the manufacturing cost and complexity of the circuit. Alternately, designers can use a series resistor to protect the vulnerable pins, as shown in Figure 4. The resistor reduces the current flowing into the IC to a safe level. Resistive protection simplifies design and inventory and may offer lower cost. The resistance must be large enough to protect the IC, but not so large that it degrades the frequency performance of the circuit. Larger surge amplitudes require increased resistance to protect the IC. More robust ICs need less resistance for protection against a given surge amplitude. Linear's LT1137A is protected by a much smaller resistor than a 1488, as shown in Figure 5. These curves are empirical "rules of thumb." You should test actual circuits.

The series resistor may have an adverse effect on the frequency performance of the circuit. When protecting a receiver, the resistor has little effect. Figures 6a and 6b show the effect of a 600Ω resistor on the driver-output wave form. A 600Ω resistor is adequate for 1kV surges, but has minimal effect on the driver wave form up to 130kbaud, even with a worst-case load of 3kΩ||2.5nF.

You must choose the series resistor carefully to withstand the surge. Unfortunately, neither voltage ratings nor power ratings provide an adequate basis for choosing surge-tolerant resistors. Usually, through-hole resistors will withstand much larger

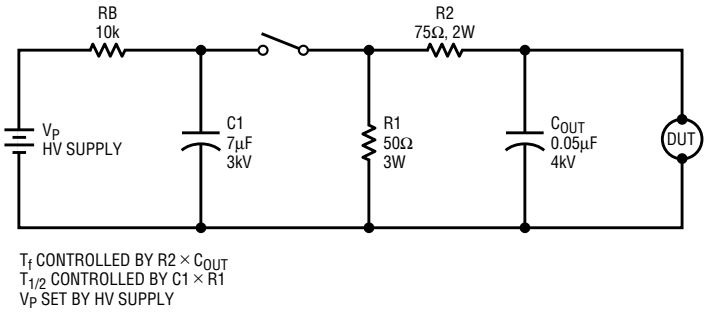


Figure 1. LTC surge-test circuit: T_F controlled by R2 × C_{OUT}; $T_{1/2}$ controlled by C1 × R1; V_P set up by HV supply

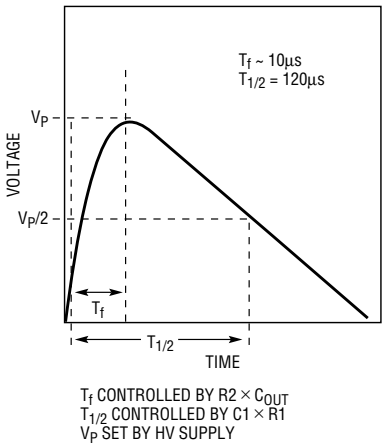


Figure 2. LTC surge-test waveform

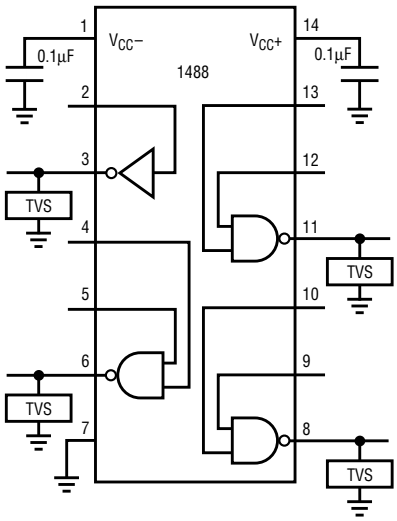


Figure 3. 1488 line driver with TVS surge protection

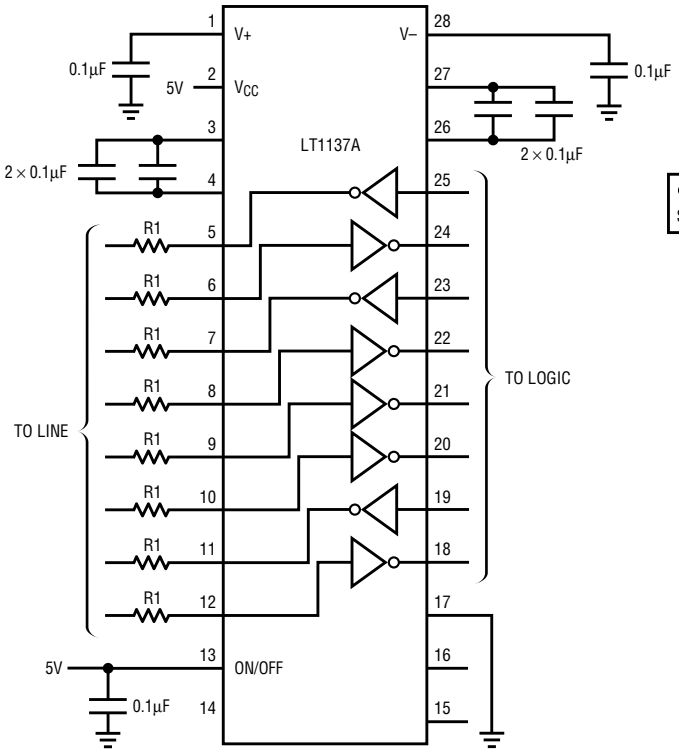


Figure 4. 1137A with resistive surge protection

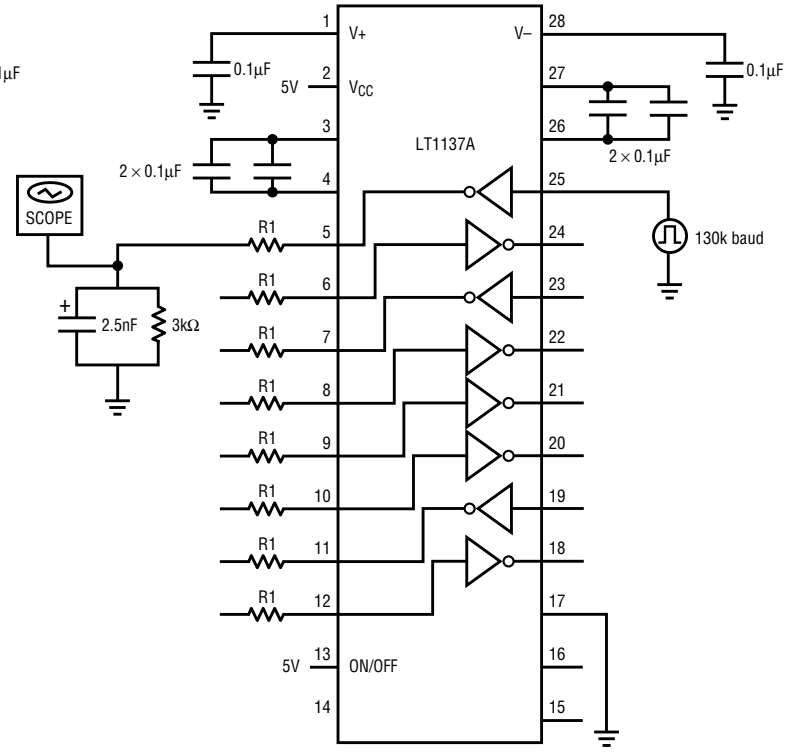


Figure 6a. Testing line driver output wave form

surges than surface mount resistors of the same value and power rating. Typical 1/8 Watt surface mount resistors are not suitable for protecting the LT1137A. If you use surface mount components, you may need ratings of 1W or more. With the LT1137A, you can use carbon film 1/4W through-hole resistors against surges up to about 900V, and 1/2W carbon film resistors against surges up to about 1200V. Unfortunately, using series or parallel combinations of resistors *does not* increase the surge handling as one would expect.

Resistive Surge Protection

The LT1137A has proprietary circuitry that makes it more robust against ESD and surges than the standard 1488/1489. The greater surge tolerance of the LT1137A makes it practical to use resistive surge protection, reducing inventory and component cost relative to TVS surge protection. The major considerations are the surge tolerance required, the resulting resistor value needed, resistor robustness and frequency performance.

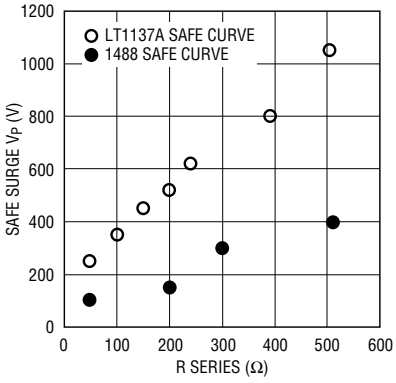


Figure 5. Safe curves for 1488 (SN75188N) and LT1137A. Safe curves represent the highest V_P for which no IC damage occurred after 10 surges.

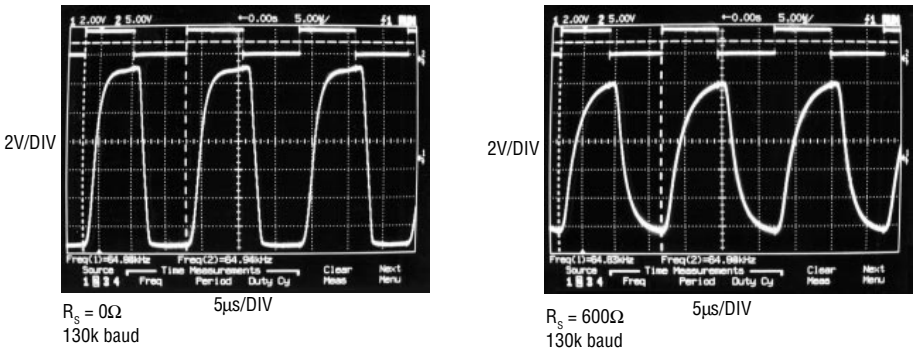


Figure 6b. Output wave forms with series resistor

New Device Cameos

LT1351: 250µA, 3MHz, 200V/µs C-Load™ Op Amp with Shutdown

The LT1351 is an ideal operational amplifier for low power applications that also require high speed, low distortion, outstanding output drive, fast settling or stability with a capacitive load.

The LT1351 slews at 200V/µs and has a gain bandwidth of 3MHz while drawing a frugal 250µA of supply current. Output drive is not compromised: the LT1351 can drive a 1kΩ load to ±12V on ±15V supplies or 20V peak-to-peak at 20kHz with less than .03% THD + Noise. Settling time is a remarkable 700ns for a 10V step settling to 0.1% and 1250ns for 0.01%. The LT1351 is stable with any capacitive load, so it is excellent as a buffer or for driving A-to-D converters.

The DC specifications are outstanding for an amplifier with such stellar AC credentials. Maximum input specifications include 600µV offset voltage, 50nA bias current and 15nA offset current. Voltage gain is 30V/mV minimum driving 2kΩ.

The LT1351 is specified for supply voltages from ±2.5V to ±15V. The shutdown pin reduces supply current to a mere 10µA.

The LT1351 comes in the industry standard pinout in 8-lead plastic SO and MSOP surface mount packages, as well as the venerable 8-lead mini-DIP.

LT1207 Dual 60MHz, 250mA Current Feedback Amplifier

The LT1207 is a dual version of the LT1206 high speed current feedback amplifier. Like the LT1206, each CFA in the dual version has excellent video characteristics: 60MHz bandwidth, 250mA minimum output-drive current, 400V/µs minimum slew rate, low differential gain (0.02% typical) and low differential phase (0.17° typical). The LT1207 includes a pin for an optional compensation network, which can help stabilize the amplifier for heavy capacitive loads. Both amplifiers have thermal and current limit circuits that provide protection against fault conditions. These capabilities make the LT1207 well suited for driving difficult loads, such as cables in video or digital communications systems.

Operation is fully specified for supplies from ±5V to ±15V. Supply current is typically 20mA per amplifier, and there are two separate micropower shutdown controls that drop supply current to less than 200µA per amplifier. When shut down, the outputs assume high impedance states. The shutdown controls can also be used to lower supply current for reduced-bandwidth applications.

The LT1207 is available in a low thermal resistance, 16-lead SOIC package. Consult the factory regarding industrial grade parts.

LTC1400 Complete SO-8, 12-Bit, 400ksps ADC with Shutdown

The LTC1400 is a complete 2.1µs, 400ksps, serial 12-bit A-to-D converter that draws only 75mW from 5V or ±5V supplies. It is the first complete 12-bit ADC to be offered in an SO-8 package. This easy-to-use device comes complete with a 200ns sample-and-hold and a precision reference. Unipolar and bipolar conversion modes add to the ADC's flexibility. The LTC1400 has both Nap and Sleep modes. In the Nap mode, it consumes only 6mW and can wake up and convert immediately after shutdown. In the Sleep mode, it typically consumes 30µW. On power-up from Sleep mode, a reference-ready (REFRDY) signal is available in the serial data word to indicate that the reference has settled and the chip is ready to convert.

The LTC1400 converts 0V to 4.096V unipolar inputs from a single 5V supply and ±2.048V bipolar inputs from ±5V supplies. Maximum DC specs include ±1LSB INL, ±1LSB DNL and 25ppm/°C drift over commercial and industrial temperature ranges. Outstanding AC performance includes 70dB S/(N + D) and 78dB THD at the input frequency of 100kHz over temperature.

The 3-wire serial port allows efficient data transfers over a compact interface to a wide range of microprocessors, microcontrollers and DSPs.

LT1371 and LT1373: High Frequency, Low Supply Current, High Efficiency Switching Regulators

The LT1371 and LT1373 are monolithic, high frequency, current mode switching regulators. They feature faster switching with increased efficiency and use small inductors—4.7µH for the LT1371 or 15µH for the LT1373—and both can be used in all standard switching configurations, including boost, buck, flyback, forward, inverting and "Cuk." A high efficiency switch is included on the die, along with all oscillator, control and protection circuitry.

The LT1371 switches at 500kHz, typically consumes only 4mA and has higher efficiency than previous parts; the LT1373 switches at 250kHz, typically consumes only 1mA and has even higher efficiency. High frequency switching allows small inductors to be used with both devices. The surface mount versions of the LT1371 and LT1373 DC/DC converter circuitry consume less than 0.6 square inches of board space.

New design techniques increase flexibility and maintain ease of use. Switching is easily synchronized to an external logic-level source. A logic low on the shutdown pin reduces supply current to 12µA. Unique error-amplifier circuitry can regulate positive or negative output voltage while maintaining simple frequency-compensation techniques. Nonlinear error-amplifier transconductance reduces output overshoot on start-up

or overload recovery. Oscillator frequency shifting protects external components during overload conditions.

The LT1371 is available in SO, 7-lead TO220 and DD packages; the LT1373 is available in 8-pin SO or DIP packages.

LT1501: Adaptive-Frequency Current Mode, Micropower Switching Regulator

The LT1501, LT1501-3.3 and LT1501-5 are adaptive-frequency current mode, step-up switching regulators with internal loop compensation. In contrast with pulse-skipping type switching regulators, this family uses a current mode topology that provides low noise operation and excellent system performance. The LT1501 family also features a low battery comparator and light-load Burst Mode operation.

The LT1501 has a 750mA power switch and can be set to operate at frequencies up to 600kHz. This family of devices can operate from supply voltages as low as 1.8V. The quiescent current of 160µA can be further reduced to 6µA in shutdown mode.

Available in 8-pin SO packaging, the LT1501 is a versatile switcher family featuring both current mode performance and simple system design.

LTC1538-AUX/LTC1539: High Efficiency Dual Synchronous DC/DC Controllers for Portable and Notebook Computer Applications

The LTC1538-AUX/LTC1539 are dual synchronous step-down switching regulator controllers that drive external N-Channel power MOSFETs in a fixed-frequency architecture. The LTC1539 Adaptive Power™ output stage drives synchronous N-Channel MOSFETs at high currents, and switches to a low power output stage at low currents to maintain high efficiency without resorting to variable frequency operation. The LTC1538-AUX employs Burst Mode operation at low currents to achieve low quiescent current.

Key features that distinguish the LTC1538-AUX/LTC1539 from the similar LTC1438/LTC1439 devices are the circuits that remain active even when both of the switching controllers are shut down—a 5V linear regulator (LTC1538-AUX and LTC1539) and a voltage comparator (LTC1539 only). The 5V regulator is capable of supplying 25mA (typical) with a dropout of less than 0.5V while exhibiting an output impedance of less than 1Ω. The comparator has its positive input tied to the 2% accurate, internal 1.19V voltage reference. A CMOS open-drain output can be externally pulled up to a power supply of 12V or less and can sink more than 10mA. The standby supply current with the 5V linear regulator and voltage comparator active is only 50µA.

An auxiliary 0.5A linear regulator, available in both the LTC1538-AUX and LTC1539, uses an external PNP pass device to provide a low noise, low dropout 12V or adjustable output. This same regulator can be configured to provide a linear 3.3V to 2.9V/3A supply with the addition of a low saturation NPN pass device. A secondary feedback control pin, SFB, guarantees regulation on secondary windings regardless of the primary load by forcing continuous operation as required.

Internal resistive dividers provide pin-selectable output voltages of 3.3V and 5V on the first controller of both devices. The second controller in the LTC1539 can be programmed to 3.3V, 5V or adjustable according to the connection of the V_{PROG} pin, whereas the second controller in the LTC1538 is adjustable.

The LTC1539 features a phase-locked loop (PLL) for synchronization to an external source, and a power-on reset timer (POR) that generates a signal delayed by $65536/F_{CLK}$ (typically 300ms) after the output is within 7.5% of the regulated output voltage. The LTC1539 is further differentiated from the LTC1439 by the fact that POR monitors the first controller rather than the second.

The operating current levels are user programmable via external current sense resistors. A wide input supply range allows operation from 3.5V to 36V (maximum). The LTC1538-AUX is available in a 28-pin SSOP package and the LTC1539 comes in a 36-pin SSOP.

LTC7545A: Multiplying 12-Bit DAC

The LTC7545A is a 4-quadrant multiplying, current-output 12-bit DAC. It is a superior, pin-compatible replacement for the industry standard AD7545A. It has improved accuracy and stability, reduced sensitivity to external amplifier VOS, lower output capacitance and reduced cost.

The LTC7545A has a parallel 12-bit-wide microprocessor-compatible interface. This DAC has excellent accuracy and stability, with INL and DNL guaranteed at 1/2 LSB MAX over temperature. Gain error is 1 LSB MAX, eliminating adjustments in most applications. Typical applications are process control, and software programmable gain, attenuation and filtering.

The LTC7545A comes in 20-pin SO and PDIP packages and is available in commercial and industrial temperature grades. LT

For further information on the above or any of the other devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number: 1-800-4-LINEAR. Ask for the pertinent data sheets and application notes.

DESIGN TOOLS

Applications on Disk

NOISE DISK
This IBM-PC (or compatible) progam allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate noise using specs for any op amp. Available at no charge.

SPICE MACROMODEL DISK
This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models, and a demonstration copy of PSPICE™ by MicroSim. Available at no charge.

Technical Books

1990 Linear Databook • Volume I — This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook Supplement — This 1248 page supplement to the *1990 Linear Databook* is a collection of all products introduced since then. The catalog contains full data sheets for over 140 devices. The *1992 Linear Databook Supplement* is a companion to the *1990 Linear Databook*, which should not be discarded. $10.00

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1993 Linear Applications Handbook • Volume II — Continues the stream of "real world" linear circuitry initiated by the *1990 Handbook*. Similar in scope to the 1990 edition, the new book covers Application Notes 41 through 54 and Design Notes 33 through 69. Additionally, references and articles from non-LTC publications that we have found useful are also included. $20.00

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SwitcherCAD Handbook — This 144 page manual, including disk, guides the user through SwitcherCAD—a powerful PC software tool which aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. $20.00

1995 Power Solutions Brochure, *First Edition* — This 64 page collection of circuits contains real-life solutions for common power supply design problems. There are over 45 circuits, including descriptions, graphs and performance specifications. Topics covered include PCMCIA power management, microprocessor power supplies, portable equipment power supplies, micropower DC/DC, step-up and step-down switching regulators, off-line switching regulators, linear regulators and switched capacitor conversion. Available at no charge.

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