20 MHz
Level Oscillator
TF 2356

Code No. 52356-900D
Serial Nos. commencing 145601

AMENDMENT RECORD

The following amendments are incorporated in this manual.

Amendment No.	*Date*	*Applies to Ser. Nos. commencing*

MARCONI INSTRUMENTS LIMITED
ST. ALBANS HERTFORDSHIRE ENGLAND.

CONTENTS

PRELIMINARIES

CHAPTERS

Note...

Each page bears the date of the original issue or the code number and date of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus ▶ ..... ◀ to show the extent of the change. When a chapter is reissued the triangles do not appear.

Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2 etc.

NOTES AND CAUTIONS

ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been tested according to IEC Publication 348, 'Safety Requirements for Electronic Measuring Apparatus, and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

Removal of covers

Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be discharged; to discharge mains filter capacitors, if fitted, short together the L (live) and N (neutral) pins of the mains plug.

Mains plug

The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

Fuses

Note that the supply fuse is connected in series with the brown (live) wire of the supply lead. If the equipment is connected to the supply via a two-pin plug, it will be possible for the fuse to become connected to the neutral side depending upon the orientation of the plug in its socket. In these circumstances certain parts of the instrument could remain at supply potential even after the fuse has ruptured.

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external supply fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A.

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided.

CAUTION : STATIC SENSITIVE COMPONENTS

Components identified with the symbol  on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange discs, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disc or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with an earthed conductive surface.

Metallic tools earthed either permanently or by repeated discharges.

A low-voltage earthed soldering iron.

An earthed wrist strap and a conductive earthed seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

RADIO FREQUENCY INTERFERENCE

This equipment conforms with the requirements of EEC Directive 76/889 as to limits of r.f. interference.

WARNING : HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges care should be taken, particularly when servicing the equipment, to avoid minor cuts.

WARNING : TOXIC HAZARD

Many of the electronic components used in this equipment employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

Chapter 4-2

TECHNICAL DESCRIPTION

CONTENTS

Para.

Fig. Page

INTRODUCTION

1. The following description should be read in conjunction with the appropriate diagrams in this chapter and with the circuit diagrams in Chap. 7. The circuits are summarized in paras. 2 to 21 and then described in detail in paras. 22 to 151.

CIRCUIT SUMMARY

General

2. TF 2356 is, essentially, a beat frequency oscillator covering the frequency range 100 Hz to 20 MHz. A microprocessor is used to translate the front panel instructions into control signals to select output impedance and set frequency and to precisely control output level by means of programmable attenuators. The frequency synthesized local oscillator, which is phase locked to a 10 MHz temperature-compensated crystal oscillator, uses three phase locked loops to generate frequencies from 30 to 50 MHz in 5 Hz steps. Output level accuracy is controlled by an a.l.c. detector which is tailored to match the frequency response of the output attenuators. A simplified block diagram of the sender is shown in Fig. 1.

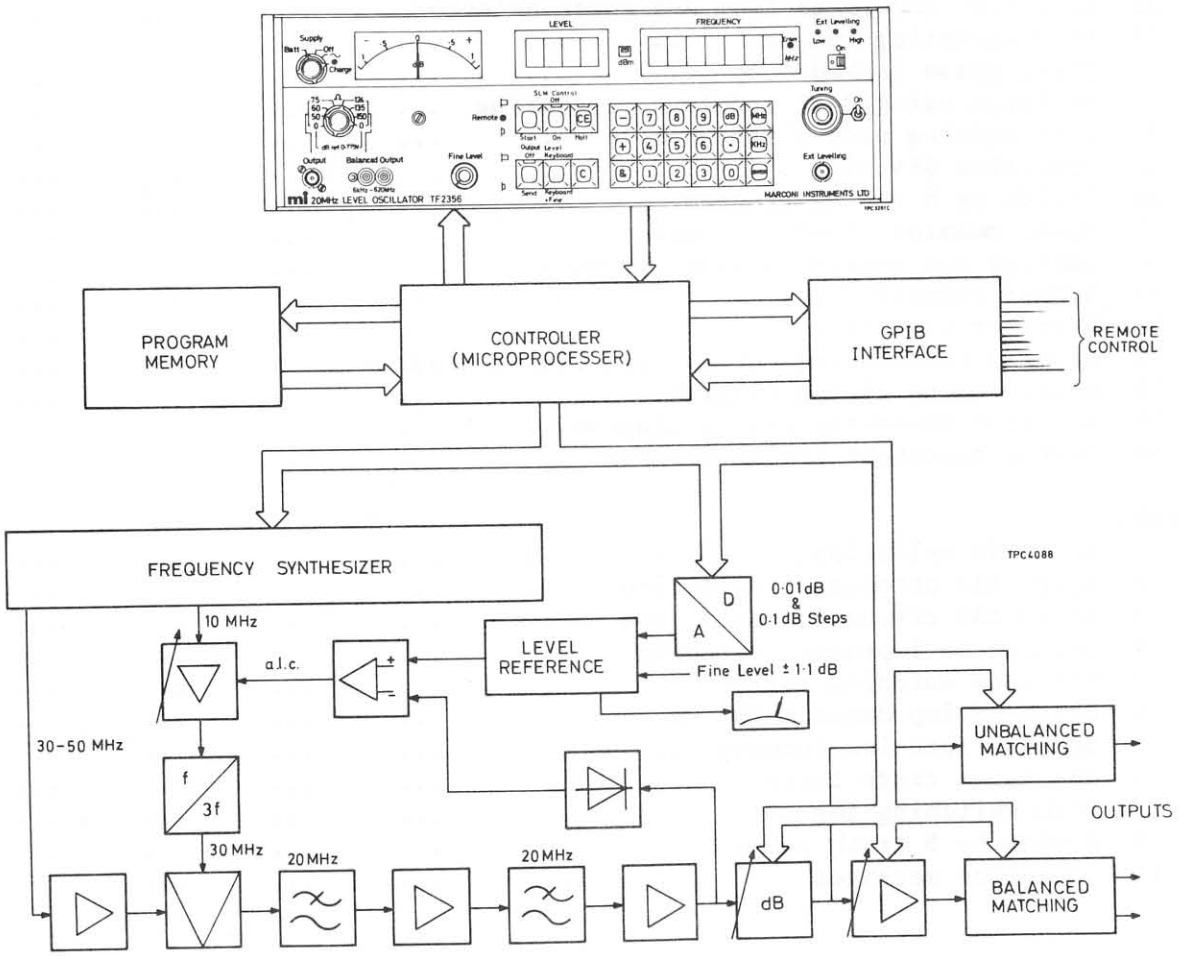


Fig. 1 Simplified block diagram

Signal path

3. The 30 to 50 MHz local oscillator signal is mixed with the third harmonic of the 10 MHz frequency standard and the difference frequency is selected by low-pass filters. This signal is amplified in low distortion amplifiers to provide a maximum output of +10 dBm from a 75 Ω source impedance. The signal is then sensed using a circuit which has a frequency response which matches that of the attenuators and is compared with a controlled d.c. reference, the error signal being fed back to a controlled gain amplifier to level the output. The d.c. reference is controlled either by a D/A converter to give 0.1 dB steps or a continuously variable potentiometer to give a control range of ±1.1 dB. The levelled signal is fed via the programmable attenuators to the output after impedance matching.

Microprocessor and memory

4. The microprocessor controls the operation of the instrument by implementing a series of instructions which are stored in the program memory. Typical operations are:- display level and frequency, read the positions of push-buttons

and switches, set attenuators or frequency, select matching, communicate with other instruments via the GPIB etc. (see Fig. 2).

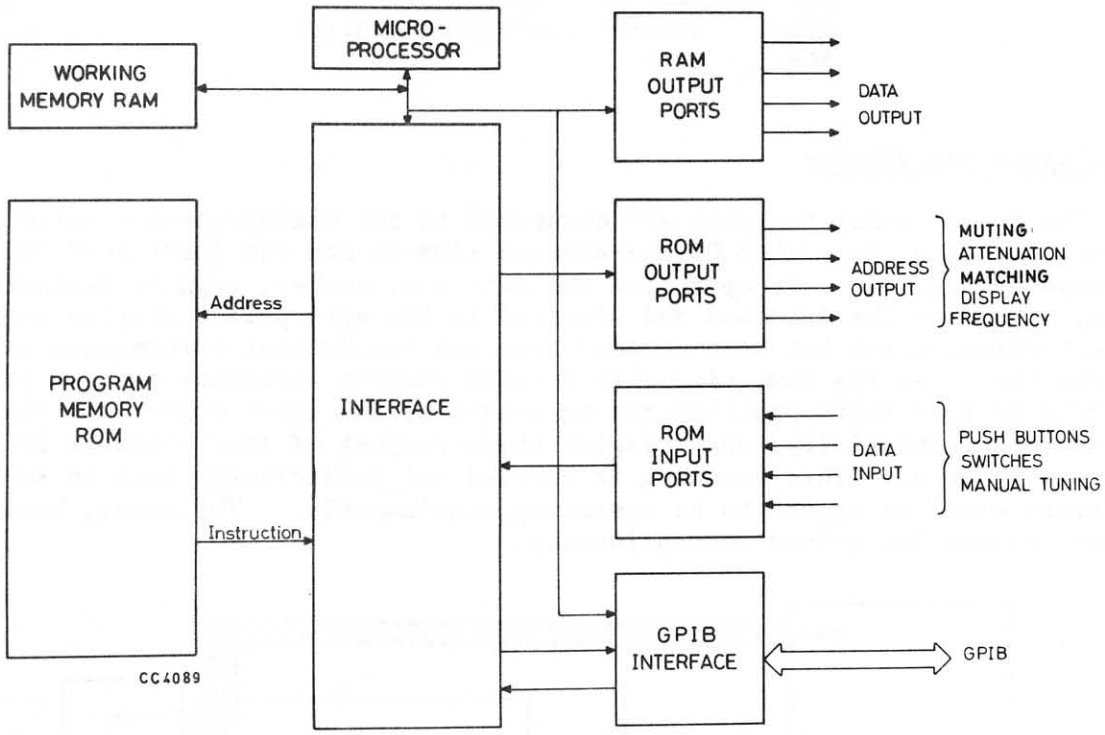


Fig. 2 Microprocessor operation

5. The instructions which form the program (identity) for the microprocessor are stored in the program memory in sequence. In order to control the instrument, the microprocessor executes the instructions in turn while keeping count of where it is (instruction address) using its internal program counter. However, operations which need to be carried out more than once, e.g. reading switch positions, illuminating display digits, addition, setting frequency etc., are generally included in the program as sub-routines. When a JUMP TO SUBROUTINE instruction is encountered, the address of the next sequential instruction is stored and the address of the start of the subroutine is placed in the program counter. At the end of the subroutine, the program jumps back to the stored address so that operation can recommence from the point where the jump occurred. A sub-routine may call up a second subroutine to perform a particular function before returning to the main program. Up to seven subroutines may be nested in this way. Results, i.e. switch positions, frequencies etc., are stored in the working memory (RAM).

Sender control

6. In order to implement the control of the instrument the microprocessor receives information from the switches, push-buttons, GPIB and detectors, processes these, and then sends instructions to the various parts of the instrument. Control lines are minimized by adopting a bus system. One output port, RAM 1 is used to route the data in either hexadecimal or b.c.d. format. The destinations for this data (addresses) are designated by four separate 4 line

output ports thus giving a maximum direct addressing capability of 64 destinations. These ports are allocated as follows:-

ROM 0 - Front panel
ROM 1 - Frequency synthesizer
ROM 2 - General instrument control
ROM 3 - GPIB

Front panel and display

7. The front panel controls are connected to the microprocessor using two output ports i.e. data (RAM 0) and address (ROM 0) and one input port (ROM 0) as shown by Fig. 3. In operation the data e.g. number, sign or decimal point, is set on the data bus and directed to the appropriate display module by the address which has been decoded from the hexadecimal information on the address bus. At the same time this decoded address activates one set of four controls so that their position can be sensed by the input port. By changing the address sequentially, each display character/set of four controls is accessed in turn. This scanning is carried out sufficiently fast to enable the front panel to appear to be operating continuously. The meter, however, is not scanned bur driven conventionally.

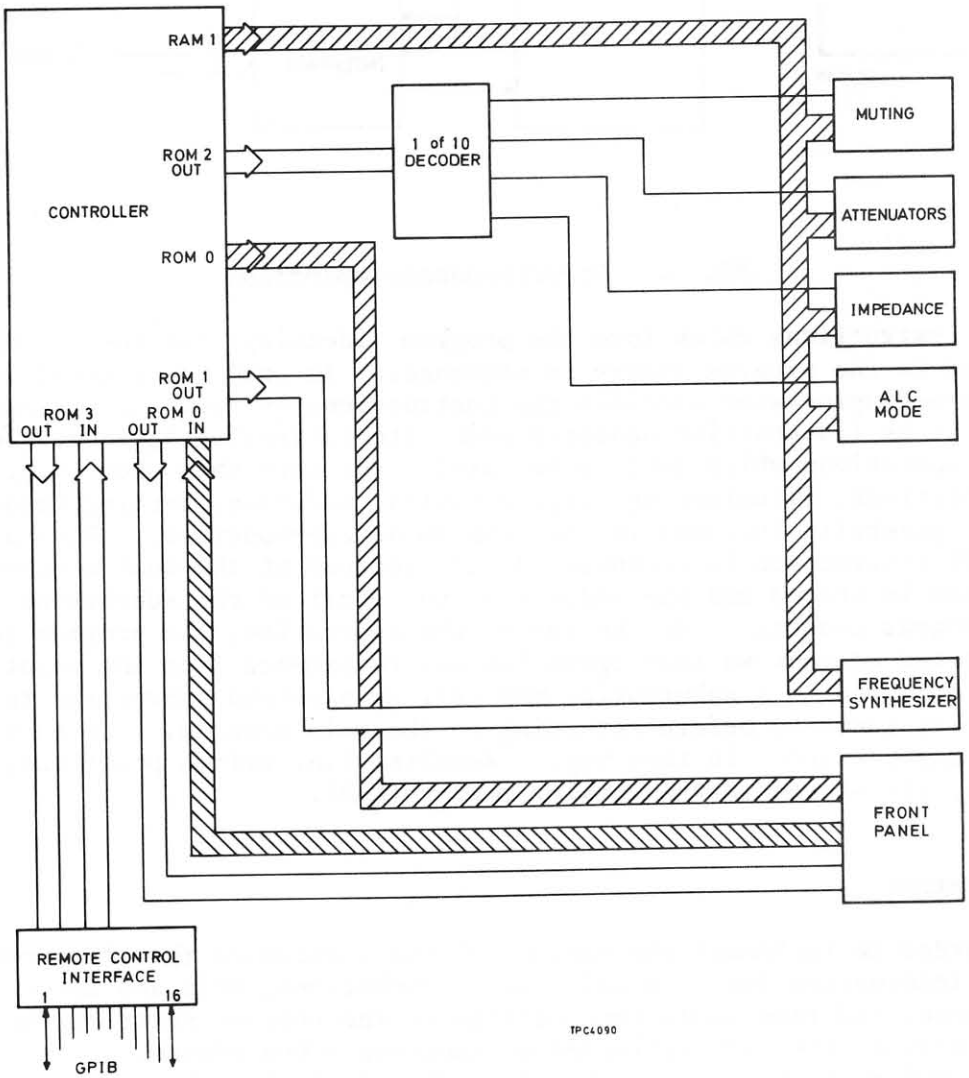


Fig. 3 Sender control system

Manual tuning control

8. To provide a manual tuning facility the TUNING knob is connected to a motor armature so that when turned a voltage is generated which is used to produce pulses at a rate proportional to the speed of rotation and hence rate of tuning. These pulses are counted and, at approximately 60 ms intervals, a number proportional to the count is added to or subtracted from the frequency information to the local oscillator and the counter is reset. If the tuning knob is given a spin a window detector senses this condition and the motor is latched on so that it rotates continuously while the pulse generator produces pulses at its maximum rate. Under these conditions the sender tunes at a rate dependent upon the frequency selected.

Local oscillator

General

9. The local oscillator which uses a frequency synthesizer tracks 30 MHz above the output signal frequency and operates in the range 30 MHz to 50 MHz. A variable output in this range is produced using dividers in three phase locked loops. Included in the dividers are presettable variable dividers dividing by N1 and N2 for fine and coarse frequency division respectively. In order to understand the overall operation of the local oscillator for any frequency it is helpful to develop its expression from the simple expressions for the outputs of each of the three phase locked loops. The resulting expression is introductory to the explanation of the operation of the presettable dividers.

Frequency division

10. Consideration of Fig. 4 enables the following expressions for each of the three phase locked loops to be derived :-

$$\text{(i)} \quad f1 = fb + N1fa$$

$$\text{(ii)} \quad f2 = fc + \frac{f1}{N2N4}$$

$$\text{(iii)} \quad f3 = \frac{N2}{N3} f2$$

Substituting (i) and (ii) into (iii) the expression becomes :-

$$\text{(iv)} \quad f3 = \frac{N2}{N3} fc + \frac{1}{N3N4} fb + \frac{N1}{N3N4} fa$$

where fa = 500 Hz, fb = 10 MHz, fc = 2 MHz, N3 = 200 and N4 = 5.

Substituting the values given results in the final equation :-

$$\text{(v)} \quad \underline{f3 = 100{,}000 + 5N1 + 10{,}000N2 \quad (Hz)}$$

11. Design considerations determine that coarse frequency divider N2 outputs must be multiples of 10 kHz so that for a local oscillator operating 30 MHz above the r.f. input, i.e. 30 to 50 MHz, its division range should be 2000. And for the remaining frequencies up to 10 kHz the division ratio range for

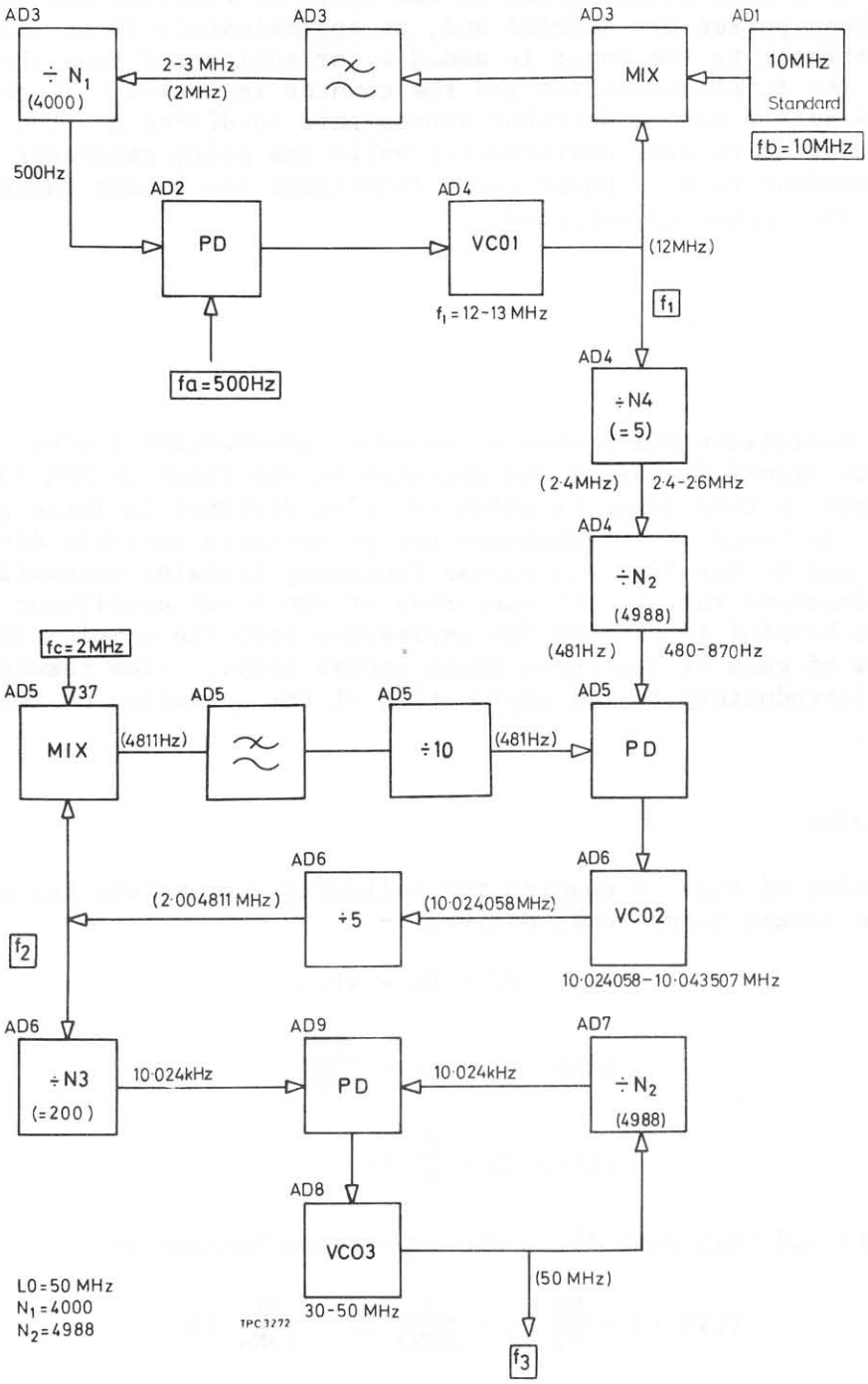


Fig. 4 Local oscillator operation - example values given in brackets are for 50 MHz operation

fine frequency divider N1 should also be 2000 to achieve a required resolution of 5 Hz. Counter range limits are derived below.

Dividers

12. N1 division requirement is satisfied by a triple decade divider preceded by a ÷2 counter and this is achieved with a 4059 presettable counter. With the exception of three jam inputs which are hard-wired, the counters are programmed by b.c.d. presets on the jam inputs. Mode select inputs determine the modulus (division ratio) of the first and last counting sections. The modulus at any frequency for the counters (both N1 and N2) is found from:-

N = (mode) (1000 x preset 5 + 100 x preset 4 + 10 x preset 3 + 1 x preset 2) + preset 1.

The N1 counters are shown in Fig. 5. Preset 5 on jam inputs 2, 3 and 4 is hard-wired to b.c.d. 2; the remaining presets are set to their maximum b.c.d. value of 9. Mode selection (not shown) is set to 2. Counter range limits are therefore:-

$$N_{max} = 2(2000 + 900 + 90 + 9) + 1 = 5999 \text{ and}$$

$$N_{min} = 2(2000 + 0 + 0 + 0) + 0 = 4000$$

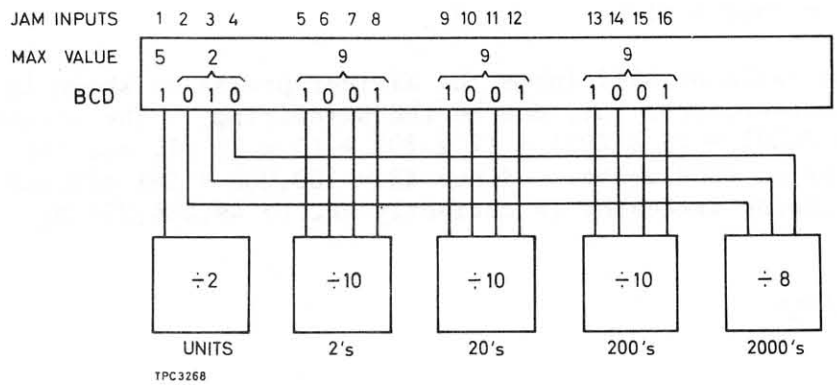


Fig. 5 Presettable N1 counter at maximum preset values

13. Division ratios for N2 are determined by those for N1 when substituted in the equation derived previously for f3. Counter range limits are therefore 2988 at 30 MHz, to 4988 at 50 MHz.

Example

14. Fig. 6 shows a presettable counter example where dividers N1 and N2 are preset for an r.f. input of 19,236,235 Hz. For the purpose of the example the local oscillator output frequency may be expressed by :-

$$f3 = ABCDE \cdot FGH + 30{,}000 \text{ (kHz)}$$

where A to G are b.c.d. 0 to 9, and H is 0 or 1 to signify 0 or 5 (i.e. the 5 Hz resolution of the system).

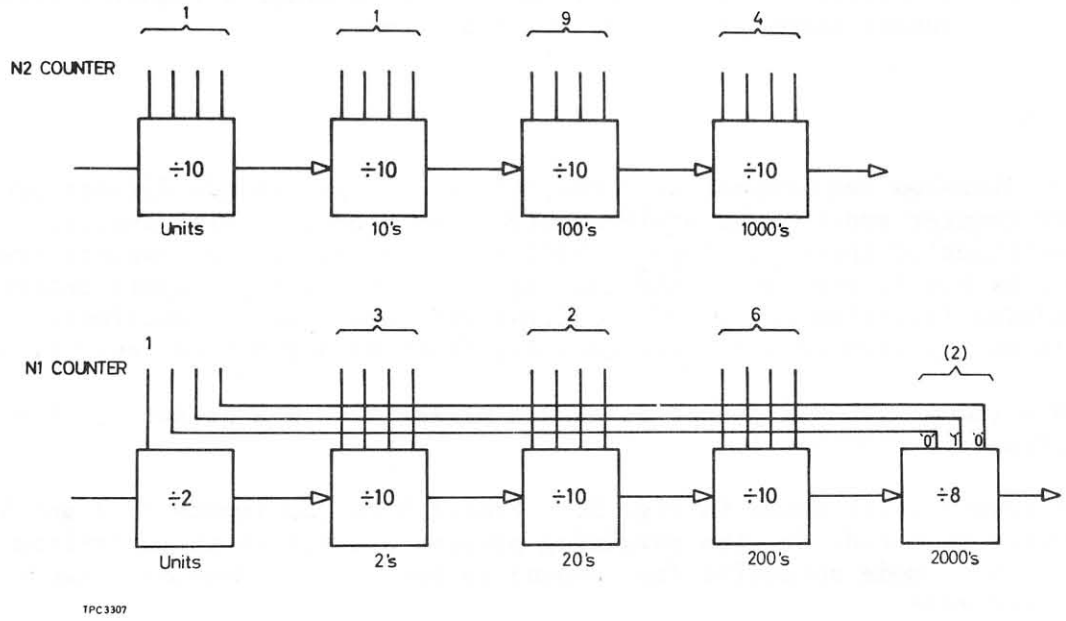


Fig. 6 Presettable counters - example showing counter presets for an r.f. of 19,236,235 Hz

Thus ABCD = 1923 and EFGH = 6231.
Then N1 = 4000 + 2EFG + H = 5247
and N2 = 2988 + ABCD = 4911.

The N2 division ratio of 4911 forms the divider preset as shown in the figure. The N1 ratio however, does not, due to the hardwiring. The preset used is 6231 i.e. (2 x 2000) + (6 x 200) + (2 x 20) + (3 x 2) +1, and this value equates directly to EFGH above. Since f3 = 100,000 + 5N1 +10,000 N2 (Hz) the local oscillator frequency is correctly set to 49,236,235 Hz.

GPIB and interface

General

15. The GPIB interface boards fitted in this instrument enable the level oscillator to form part of an automatic measuring system. Such a system is illustrated in Fig. 7 where the instrument is shown used as part of a selective level measuring set formed with a selective level meter and with the addition of a coaxial switch unit. All instruments are interconnected by the general purpose interface bus and are working under the direction of a controller. The controller directs the flow of data on the bus mainly by designating which instruments are to send data and which are to receive data. Data are sent over the bus by a talker to listeners enabled to receive such data. Since the level oscillator has a limited control capability it is equipped to act as controller, talker and listener but when operating with a GPIB controller the sender acts as a listener as shown in Fig. 7.

General purpose interface bus

16. The bus, which is entirely passive, uses 16 signal lines to connect all units of a system in parallel. These lines are functionally sub-divided into data, transfer and interface management buses (see Fig. 7).

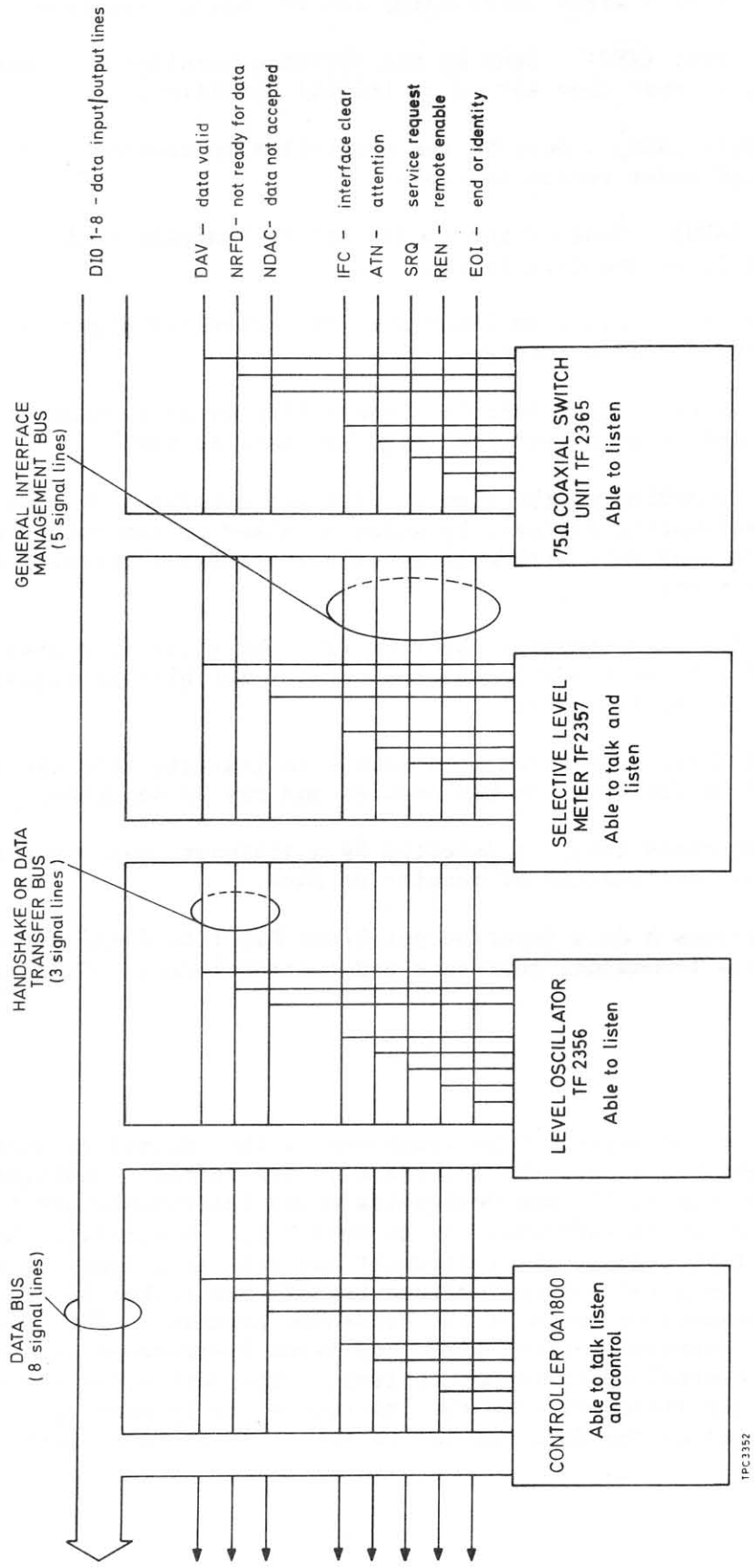


Fig. 7 Interface bus structure example

Interface management bus : Manages the orderly flow of data across the interface and consists of 5 wires which carry the following signals:-

Interface clear (IFC) : Sent by the system controller to clear all interfaces so that they set to an initial condition.

Remote enable (REN) : Sent by the controller to enable instruments to be placed under remote control.

Attention (ATN) : Sent by the controller to indicate that an address or command is on the data lines.

End or identify (EOI) : An instrument or controller signal sent to indicate the end of a message.

Service request (SRQ) : Sent to a controller by an instrument to indicate that it needs service (e.g. has data to pass).

Transfer bus : Co-ordinates the flow of data and comprises 3 lines which are used for the handshaking process, by which a talker or controller synchronizes its readiness to send data with a listener's readiness to receive data. The handshake signals are:-

Not ready for data (NRFD) : Asserted (low) by a listener when it is active and not yet ready to receive data. Set high to signal its readiness to receive data.

Data valid (DAV) : Asserted by a talker to indicate that the data it has placed on the data bus has settled and may be accepted.

Not data accepted (NDAC) : Asserted by a listener when receiving data. Set high as confirmation of receipt of data.

Data bus : Comprises 8 data input/output lines DIO 1 to 8 and is used to transfer the data (commands, addresses and instructions) in bit parallel, byte serial form.

Bus operation

17. A sequence of messages may be commenced by the controller asserting IFC on the management bus to set the interface to its initial condition. The controller then asserts ATN and designates which instruments are to be listeners by sending their listen addresses on the data bus. Similarly, the controller designates the talker (only one instrument may talk at a time) by sending its talk address. Upon the controller removing ATN the talker is free to send data to the listeners by means of the handshake process. The talker concludes the sequence by carriage return, line feed (some instruments send EOI) and this tells the controller to resume control. The controller may now switch the talker and all listeners into the inactive state by sending UNT (untalk) and UNL (unlisten) on the data bus before selecting the next participants.

Handshake

18. The handshake is used whenever data are transferred on the bus. When a signal is asserted the function indicated by the line is carried out, e.g. NRFD is asserted to signify the listener's unreadiness to receive data, and unasserted or removed when ready to receive data. Briefly, a typical hand-

shake is as follows:-

(1) Talker (or controller) places a byte on the data bus with DAV initially unasserted to show data are not yet valid.

(2) When all listeners are ready to receive data NRFD is removed, with NDAC at this time asserted.

(3) After a delay to allow data bus to settle, talker asserts DAV to show data are valid and may be accepted.

(4) Data byte is transferred, then listeners assert NRFD. When all listeners have accepted the byte NDAC is removed to signify receipt.

(5) Talker removes DAV, listeners assert NDAC, and bus reverts to its initial condition ready for next data byte.

Handshake timing diagrams are given under the appropriate board descriptions.

Interface operation

19. The interface takes care of data transfer between the GPIB and the sender as well as decoding data bus control messages. Block diagram Fig. 8 shows the overall interface operation. Control messages and addresses are passed in by means of the handshake process and since ATN is asserted by the controller with these messages they are decoded by the FPLA (field programmable logic array). Control messages such as, e.g. SPE, SPD used for serial poll, are decoded by the FPLA and the function carried out. The FPLA also performs address recognition. Data on DIO lines 1 to 5 are compared for equivalence with data set on the 5 rear panel address switches. When a possible address is recognized and providing certain other conditions are satisfied, the data on DIO lines 6 and 7 are decoded to determine whether the instrument is being addressed as a talker or a listener. When designated a talker, the interface transfers its status byte by means of a talk handshake to the controller via the talk buffer and transceivers. When designated a listener, instruction

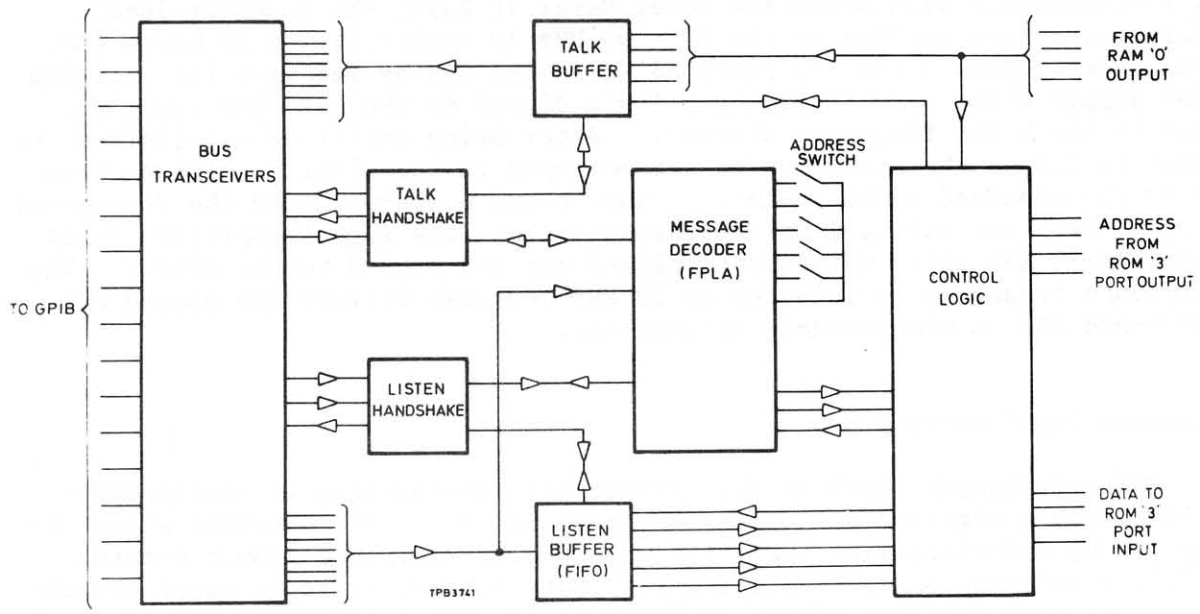


Fig. 8 GPIB interface operation

data is transferred via the transceivers by means of the listen handshake and stored in a FIFO (first-in, first-out memory).

20. By means of the FIFO, which has a capacity for 64 words, but waiting time is avoided while the processor reads the messages since instructions may now be processed asynchronously without slowing down data transfer. Internal address inputs to the control logic section direct the received instruction byte out from the FIFO in two 4-bit words onto the internal data bus to the processor. When the instruction bytes are received by the processor they are checked for validity and, if an error is detected the SRQ (service request) message is sent to the remote controller. All instructions consist of identifying letters followed by numerals so that there is generally a recognisable relationship between a function and its identifier, e.g. F = frequency, L = level etc.

Power supply

21. Provision is made for the instrument to operate from either an a.c. supply in the ranges 95 to 130 V or 190 to 260 V at between 45 and 65 Hz or from a battery unit of NiCd cells which allow approximately 4 hours of continuous operation. However, when operating from the battery, power is not supplied to the GPIB interface. Regulated d.c. is supplied at ±7.5 V and ±5 V as well ±12 V for the memory, GPIB interface and battery trickle charge to a maximum of 400 mA.

RF UNIT

Signal generation and a.l.c.

Signal generation

22. Sender output in the range 100 Hz to 20 MHz is derived from the difference frequency between a 30 to 50 MHz signal and a 30 MHz signal. During normal operation the 30 to 50 MHz signal is supplied by local oscillator board AD8 and fed to mixer board AA1 (see Fig. 9). When however, the sender is operating synchronously with Selective Level Meter TF 2357, the receiver local oscillator output applied at the 30 - 50 MHz IN socket is fed to board AA1. During synchronous operation board AA1 disables AD8 by removing its positive power supply while also supplying a logic signal to the microprocessor in order to blank the frequency display. After being amplified and limited the signal is fed to the mixer. The second input to the mixer is derived from the 10 MHz standard to board AA11. This board operates under the control of a signal from the a.l.c. loop to precisely limit the signal amplitude after which the 30 MHz third harmonic is picked out and passed to the mixer. The difference frequency is selected by 20 MHz low-pass filters and passed out from board AA3 to programmable attenuators.

Automatic level control

23. The r.f. output level to the programmable attenuators is continuously monitored by a negative peak detector on board AA3. The detected signal is compared by a differential amplifier with a d.c. reference from a summing amplifier on board AA12. When the r.f. output level is at an exact dB multiple, the peak detector output is balanced against a reference voltage corresponding to +10 dBm r.f. input. But if the FINE LEVEL control is operated, or a level change in 0.1 dB steps is selected on the keyboard, or the micro-

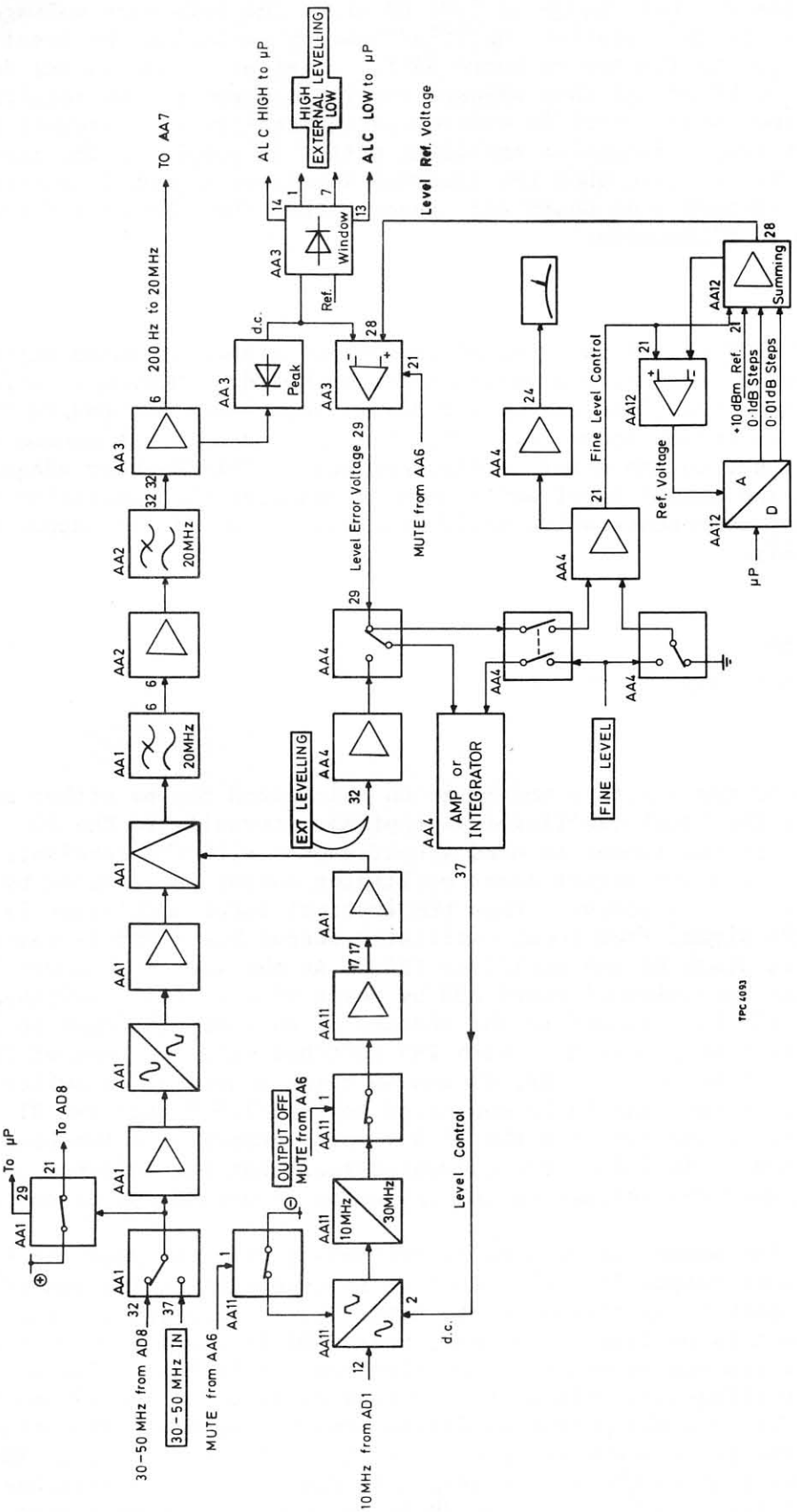


Fig. 9 Signal generation and a.l.c.

processor selects a level change in 0.01 dB steps the reference voltage changes. This unbalances the differential amplifier thereby adjusting the level control signal voltage to the limiter on board AA11. Limiter output to the double balanced mixer on board AA1 then adjusts the r.f. output to the required new level. When the output level is controlled externally, the external levelling signal replaces the differential amplifier output in supplying the level control signal. To indicate when the external levelling signal is outside range limits a window detector on board AA3 causes either the HIGH or LOW EXTERNAL LEVELLING lamp to illuminate.

Muting

24. When AUTO MUTE ENABLE is selected the output signal is muted during changes in level or frequency entered on the keyboard. Muting is effected in two stages : in the first the muting signal from board AA6 causes the level control signal to reduce board AA11 limiter output, and in the second the 30 MHz signal input to the mixer is disconnected. This ensures adequate attenuation of the output level while greatly reducing the generation of unwanted frequency components which would otherwise occur if the output were muted too quickly.

Board AA1 - Mixer

Circuit diagram : Chap. 7, Fig. 3

Switching

25. The 30 to 50 MHz input to the mixer on this board may be either supplied internally from the local oscillator or applied externally to the 30 - 50 MHz IN socket when the instrument is used synchronously with the receiver. For the latter operation the sender local oscillator output is disabled by electronic switches on this board. When the internal local oscillator is used, the 30 to 50 MHz signal from local oscillator output board AD8 is passed in at contact 32 to diode D1 and amplifier TR4. At the same time power is supplied for the operation of board AD8 by means of electronic switches TR1, TR2 and TR3. TR3 is held off in the absence of an external input to forward bias its base-emitter junction. With TR3 switched off, the base of TR2 is connected to earth by means of R2, R5 and R4 which causes it to switch on. This action causes TR1 base to be connected to the -7.5 V rail via R1 and TR2. TR1 conducts and connects the +7.5 V power supply from the positive rail to board AD8. To inform the microprocessor that the internal oscillator is being used the voltage on TR3 collector is passed out at contact 29.

26. To enable the sender to be used synchronously with the receiver the tracking generator output from the receiver is connected to the sender's 30 - 50 MHz IN socket and passed in via diode D2. Since the internal local oscillator output is no longer required, board AD8 is disabled when its power supply is removed by means of the electronic switches. The connection of the receiver effectively places 50 Ω across contacts 36 and 37 and this forward biases TR3 via the potential divider R6, R7 and R8. TR3 saturates, switching off TR2 and disconnecting R1 from the -7.5 V rail so that TR1 also switches off and removes the +7.5 V supply to AD8. When TR3 switches on it connects the negative rail to contact 29 to indicate to the microprocessor that an external local oscillator is connected. The microprocessor then blanks the sender frequency display.

Mixer

27. After amplification by TR4 the local oscillator input is limited by TR5 and TR6 and coupled by transformer T2 to a further stage of amplification. TR7 and TR8 form a current feedback pair which provides approximately 19 dB of current gain. Balun T3 and transformer T4 pass the output to drive the double balanced mixer. The second mixer input is provided by the 30 MHz input from frequency multiplier board AA11 at contact 17. For harmonic suppression the signal is fed to common-base amplifier TR9 whose collector feeds to the 30 MHz tuned load L1, C15 and C16. Balun T6 and transformer T5 couple the 30 MHz signal to the mixer. After the mixing process the difference frequency at up to 20 MHz is selected by the 20 MHz low-pass filter for passing out to board AA2 via contact 6. A high-pass filter provides a matched 50 Ω termination for mixer products above 20 MHz.

Board AA11 - Frequency multiplier

Circuit diagram : Chap. 7, Fig. 3

28. An input from the 10 MHz standard is coupled from contacts 11 and 12 by transformer T1 and passed to the limiter formed by IC1a and b. The amplitude of the resulting square wave is determined by current mirror IC1c and e under the control of the d.c. input to contact 2. Common-base transistor IC1a performs a frequency multiplier function in that its collector is tuned to the third harmonic of the input signal by L1, C5 and C6 so that 30 MHz is picked out. This is passed to amplifiers TR1 and TR2 which are connected in cascode to minimise signal feedback. TR1 collector is tuned to 30 MHz by L2, C8 and C11 and the amplified signal is coupled to the mixer on board AA1 by transformer T2.

29. When muting of the signal is required a high input from AA6 to contact 1 switches on IC1d which in turn switches off the current mirrors to disable the limiter. The high muting signal also disables the cascode amplifier by switching on f.e.t. TR3 which takes TR1 base and emitter to the same potential.

Board AA12 - Fine level control

Circuit diagram : Chap. 7, Fig. 3

30. Microprocessor selection logic to contacts 13 to 16 form the data inputs to D-type latches IC1 and IC2 which, with associated ladder networks, perform the D/A conversion. The resulting analogue signal provides a level reference voltage which is used for comparison with the r.f. signal level. IC1 provides adjustment in steps of 0.1 dB while for converting dBm to dB, IC2 additionally provides level steps of 0.01 dB. The finer steps are necessary for e.g. converting 10 dBm to the equivalent 0.97 dB. The outputs from these latches are taken via inverting buffers IC3 and IC4 to the ladder networks which feed to summing amplifier IC5. Also taken to IC5 are two other inputs. One input is the +10 dBm reference level supplied from R26 with fine adjustment (±0.25 dB) by R35, and the other is the fine level control signal from contact 21. The fine level control signal is adjusted by R24 to ensure that the meter f.s.d. corresponds to ±1.1 dB, The output from the summing amplifier is fed to contact 28 to provide the negative reference voltage to board AA3. D/A conversion is exponential and for this purpose IC5 output is also taken in a feedback loop to the inverting input of differential amplifier IC6. The other, non-inverting, input is from the fine level control signal. IC6 output provides the reference voltage for the two ladder networks as well as the vcc

input to the inverting buffers whose output levels thus switch between -7.5 V and the reference voltage.

Digital to analogue conversion

31. When, for example, the latch outputs to the ladder networks are all taken low, the inverting buffer outputs will all be taken to the reference voltage level. This feeds pin 2 of the summing amplifier with current from, effectively, a 75 kΩ resistor connected to the reference voltage. This is because, in the case of the 0.1 dB ladder network, resistors R16 and R17 will be in parallel with each other and in series with R18, and the resulting 150 kΩ combination will be in parallel with R19 etc. To decrease the output level by 0.1 dB the input to R17 is taken low. This causes the current from the ladder network to decrease causing the output from the summing amplifier to become less negative. Positive feedback through IC6 reduces the reference voltage to the D/A converter thus giving an exponential change in the level reference voltage on contact 28. If the inputs to R19, R21 and R23 are sequentially taken low and restored, the current from the ladder network is decreased each time by the exponent of twice the previous level causing the r.f. signal level to change in steps of 0.2 dB, 0.4 dB and 0.8 dB respectively.

Board AA2 - Low-pass filter and amplifier

Circuit diagram : Chap. 7, Fig. 3

32. The 100 Hz to 20 MHz signal from board AA1 is passed in at contact 6 to the 3 stage amplifier formed by TR2 and TR3 with a feedback path to TR1. Overall amplifier voltage gain is approximately 28 dB. Following the amplifier is a 20 MHz low-pass filter which feeds to AA3 via balun T1.

Board AA3 - Power amplifier and a.l.c. detector

Circuit diagram : Chap. 7, Fig. 3

Power amplifier

33. The three stage power amplifier comprises TR3 and TR4 in a class A push-pull configuration driven by TR2, and with TR1 in a feedback loop. Overall amplifier voltage gain is 24 dB with a 1 dB adjustment provided by R42. L3 and X1 serve to reduce spurious signals. Amplifier output is fed to AA7 via contact 6.

Level control

34. Level control is accomplished by means of a peak detector comprising D3, R20 and C17 which feeds to the inverting input of differential amplifier IC1. Here the signal is compared with a reference voltage applied from contact 28 to the non-inverting input. The reference voltage supplied from board AA12, allows up to +1.1 dB of level adjustment either from the front panel FINE LEVEL control or for steps of 0.1 dB entered on the keyboard or 0.01 dB set by the microprocessor. Any difference between the detected output and the reference voltage results in a level error signal from IC1 to a.l.c. control board AA4 via contact 29. Diode D4 is co-located with D3 to provide temperature compensation and is fed with a constant current via R26. This together

with s.i.c. load resistor R46 ensures a linear change in output level for a linear change in reference voltage. During output muting contact 21 is held at logical '1' to ensure saturation of the a.l.c. loop. This prevents a transient rise to maximum output when the muting is removed. C14 to C16 and R16 to R18 form a compensation network to match the frequency response of the r.f. attenuators which follow.

ALC range

35. The level in or out of range condition is sensed by the window detector formed by comparators IC2 and IC3. The output signal is detected by negative peak detector D3 and the d.c. applied to the non-inverting input of IC2 and the inverting input of IC3. Reference levels for the comparators are preset by R31 and R30 which form part of a potential divider chain. Diodes D6 and D7 provide temperature compensation. Comparator outputs to contacts 13 and 14 are scanned by the microprocessor and those to contacts 7 and 1 control the operation of the EXT LEVELLING warning lamps. When the output level is within the range +4 dBm to +11.1 dBm the outputs from the comparators are all low (see Fig. 10) and when EXT LEVELLING is selected, the microprocessor causes the green lamp to flash to indicate that the level is within limits. When the range limits are exceeded by external levelling either the HIGH or the LOW warning lamp illuminates and the microprocessor informed. For a high out of range level, for example, D8 is forward biased to illuminate the HIGH EXT LEVELLING lamp. Contact 14 is also taken high causing the microprocessor to extinguish the green in-range lamp and, if under remote control, the controller is informed of the fault condition via the GPIB interface. For a low out of range level contacts 7 and 13 are taken high to inform the microprocessor and to illuminate the LOW lamp. With contact 7 directly connected to the LOW lamp this also switches on whenever OUTPUT OFF is selected. To prevent these lamps from flashing whenever AUTO MUTE ENABLE is selected, C23 is used to slow the reaction of the comparators to changes in signal level.

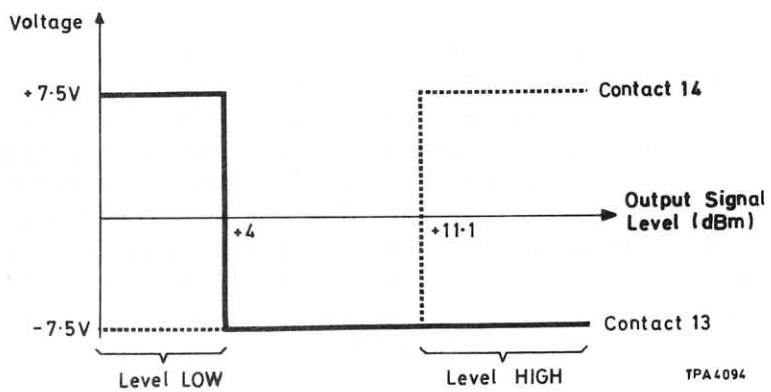


Fig. 10 ALC range limit signals - AA3

Board AA4 - ALC control

Circuit diagram : Chap. 7, Fig. 3

Mode selection

36. This board enables the sender to operate in the four ALC modes, internal local, external local, internal remote and external remote. Bilateral switches IC6 and IC7 under the control of latch IC5 are used to variously interconnect sections of the circuit to provide the different signal paths which define each mode. For the internal local mode the FINE LEVEL control may be used to adjust the output signal level. For both local and remote operation an external levelling signal may be used when selected by the EXT LEVELLING switch. The settings of the bilateral switches for each a.l.c. mode are shown in Table 1, and block diagrams of the four a.l.c. modes are shown in Fig. 11.

TABLE 1 ALC MODE SELECTION

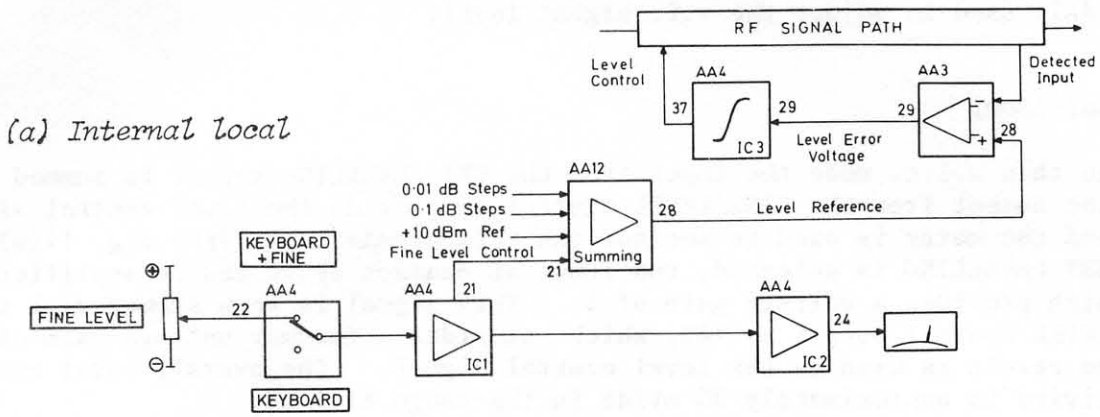
Operating mode	*Board AA4 contacts*				*IC switches closed*							
	13	*14*	*15*	*16*	*6a*	*6b*	*6c*	*6d*	*7a*	*7b*	*7c*	*7d*
INTERNAL LOCAL, KEYBOARD above 6 kHz	L	H	L	L			X	X			X	
" " KEYBOARD below 6 kHz	L	H	L	H			X	X			X	X
" " KEYBOARD + FINE above 6 kHz	L	L	L	L			X				X	
" " KEYBOARD + FINE below 6 kHz	L	L	L	H			X				X	X
EXTERNAL LOCAL	H	L	H	L	X	X			X	X		
INTERNAL REMOTE, above 6 kHz	L	H	L	L			X	X			X	
" " below 6 kHz	L	H	L	H			X	X			X	X
EXTERNAL REMOTE	H	H	L	L			X	X	X	X		

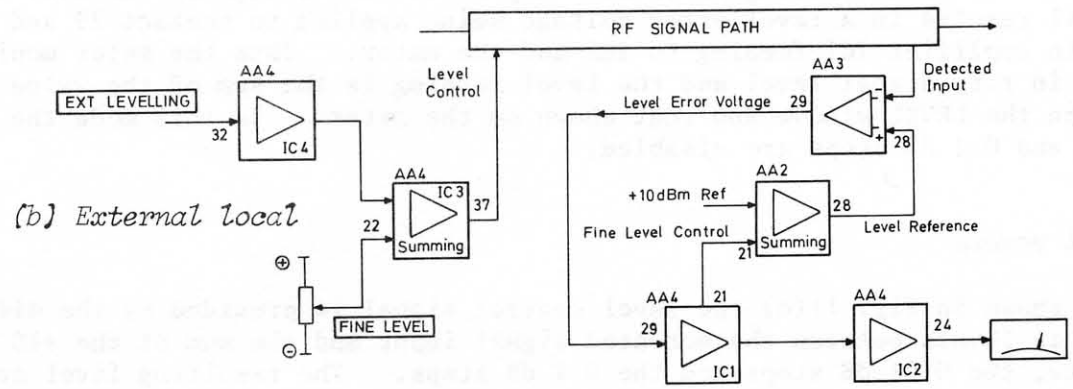
H = +7.5 V; L = -7.5 V

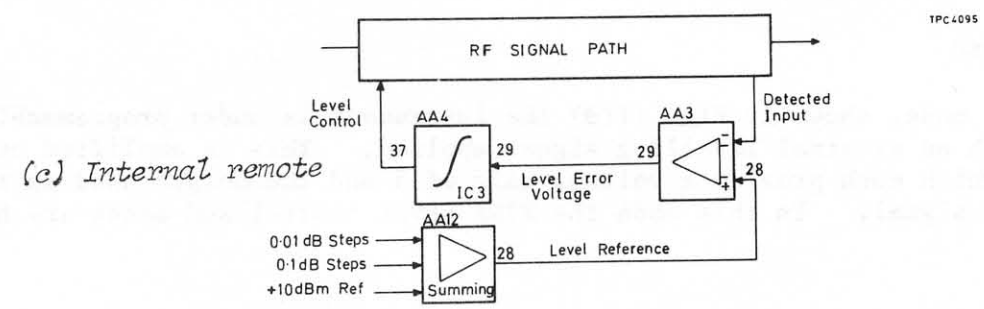
Internal local mode

37. This mode is shown in Fig. 11(a). For this a.l.c. mode the level control signal is formed by the difference between the detected signal input from AA3 and the sum of +10 dBm reference, the 0.01 dB steps, and either the 0.1 dB steps or the FINE LEVEL control output. When KEYBOARD + FINE is selected, the d.c. signal from the FINE LEVEL control is taken via IC2 to the meter for display and in order to linearize the meter reading IC2 amplification factor changes depending upon the polarity of the input signal. When the FINE LEVEL control, which is connected across the supply rails, is set for a maximum output level a negative voltage is applied to the inverting input of IC1. IC1 output is further inverted by IC2 causing diode D1 to be forward biased. With D1 conducting the feedback path for IC2 is through R5 and the meter drive current is through R6 in series with R7. When the FINE LEVEL control is set to its minimum position D2 is forward biased causing R5 and R6 to form the amplifier feedback path thus increasing IC2 gain and the meter drive is now through R7 alone.

38. IC1 output is also taken as the fine level control signal to board AA12 where it is used to change the level of the voltage by +1.1 dB. AA12 output is taken to the differential amplifier on board AA3 and any difference between this signal and the detected input results in a level error voltage back to board AA4 contact 29. This signal is applied to IC3 which, with C2 switched into circuit, behaves as an integrator. For frequencies below 6 kHz an additional capacitor, C3 is switched in parallel with C2 to provide a longer







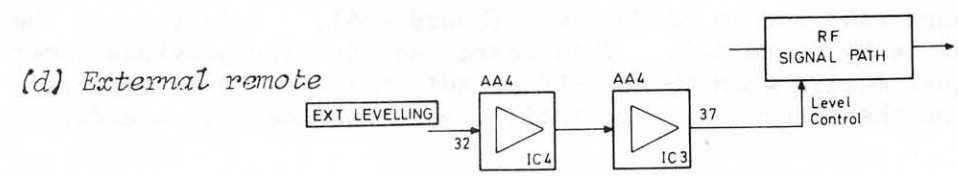


Fig. 11 Board AA4 a.l.c. mode selection

integrator time constant. IC3 output forms the level control signal to board AA11 used to adjust the r.f. signal level.

External local

39. In this a.l.c. mode the input from the EXT LEVELLING socket is summed with the output from the FINE LEVEL control to provide the level control signal, and the meter is used to monitor the r.f. signal level (see Fig. 11(b)). When EXT LEVELLING is selected, the input at contact 32 is fed to amplifier IC4 which provides a voltage gain of 5. This signal is then summed with the FINE LEVEL control output by IC3, which provides a further voltage gain of 5, and the result is used as the level control signal. The overall level control sensitivity is approximately 30 mV/dB in the range ±1.1 dB.

40. When the detected r.f. signal level to the differential amplifier on board AA3 is balanced by the level reference from the summing amplifier on board AA12 the meter reading is zero. Any subsequent change in the r.f. signal level results in a level error voltage being applied to contact 29 and to high gain amplifier IC1 feeding to IC2 and the meter. Thus the meter monitors changes in r.f. signal level and the level reading is the sum of the value displayed on the LEVEL window and that shown on the meter. In this mode the 0.01 dB and 0.1 dB steps are disabled.

Internal remote

41. As shown in Fig. 11(c) the level control signal is provided by the difference in levels between the detected signal input and the sum of the +10 dBm reference, the 0.01 dB steps and the 0.1 dB steps. The resulting level error voltage is integrated by IC3 by C2 being switched into circuit. For frequencies below 6 kHz C3 is switched in parallel with C2 to provide a longer integrator time constant. In this mode the FINE LEVEL control and meter are both disabled.

External remote

42. For this mode, shown in Fig. 11(d) the instrument is under programmable operation with an external levelling signal applied. This is amplified by IC4 and IC3 which each provide a voltage gain of 5 and the output used as the level control signal. In this mode the FINE LEVEL control and meter are both disabled.

Programmable attenuators

43. Attenuators operating under microprocessor control (see Fig. 12) attenuate the output signal in 1 dB, 2 dB, 4 dB and 8 dB steps (board AA7), in 16 dB and 20 dB steps (board AA6) and in 32 dB steps (board AA5). Selection of the AA5 32 dB attenuator is by board AA6. This board additionally provides control signals for signal muting when OUTPUT OFF or AUTO MUTE ENABLE is selected, as well as providing the return to local (rtl) signal for the GPIB boards.

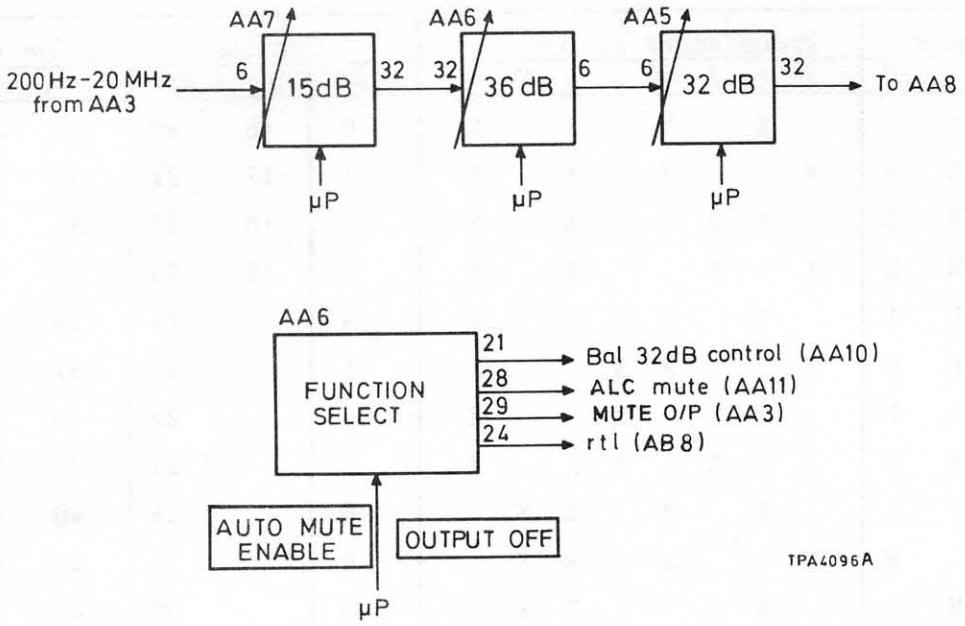


Fig. 12 Programmable attenuators

Board AA7 - Programmable attenuator

Circuit diagram : Chap. 7, Fig. 4

44. Microprocessor selection logic to contacts 13 to 16 operate quad bilateral switch IC1 whose outputs control relay drive transistors TR1 to TR8. These are arranged in complementary pairs so that for either logic level applied from IC1 only one transistor of a pair switches on. This causes the associated pairs of latching relays to be energized in the desired direction so that an attenuator is either selected or bypassed. A high, for example, on pin 3 IC1 will reverse bias TR2 while switching on TR1 thus connecting the relay coils of RLA and RLB to the positive rail. This causes the signal input from balun T1 to be fed through the 1 dB attenuator. The following attenuators act in a similar manner to provide 2 dB, 4 dB and 8 dB of attenuation. Together with the following boards AA6 and AA5, up to 80 dB of attenuation is provided (see Table 2).

Board AA6 - Programmable attenuator

Circuit diagram : Chap. 7, Fig. 4

45. The attenuators on this board operate in a similar manner to those described under board AA7. Microprocessor selection logic to contacts 14 to 16 control relay drive transistors TR1 to TR6 via quad bilateral switch IC1. The complementary pairs of transistors TR1, TR2 and TR3, TR4 operate the 20 dB and 16 dB attenuators respectively. When it is required to attenuate an unbalanced signal by 32 dB TR5 and TR6 supply the relay drive for the attenuator on board AA5. For a balanced signal however, this attenuation is provided by AA10. A high from the microprocessor to contact 13 causes IC1 to take contact 21 high for this purpose. Attenuator selection logic is shown in Table 3.

TABLE 2 BOARD AA7 ATTENUATOR SELECTION

Data lines				Transistors switched on								Overall attenuation (dB)					
13	14	15	16	1	2	3	4	5	6	7	8	AA7	AA6 & AA7		AA5, AA6 & AA7		
L	L	L	L		X		X		X		X	0	16	20	32	48	68
L	L	L	H	X			X		X		X	1	17	21	33	49	69
L	L	H	L		X	X			X		X	2	18	22	34	50	70
L	L	H	H	X		X			X		X	3	19	23	35	57	71
L	H	L	L		X		X	X			X	4		24	36	52	72
L	H	L	H	X			X	X			X	5		25	37	53	73
L	H	H	L		X	X		X			X	6		26	38	54	74
L	H	H	H	X		X		X			X	7		27	39	55	75
H	L	L	L		X		X		X	X		8		28	40	56	76
H	L	L	H	X			X		X	X		9		29	41	57	77
H	L	H	L		X	X			X	X		10		30	42	58	78
H	L	H	H	X		X			X	X		11		31	43	59	79
H	H	L	L		X		X	X		X		12			44	60 64	80
H	H	L	H	X			X	X		X		13			45	61 65	
H	H	H	L		X	X		X		X		14			46	62 66	
H	H	H	H	X		X		X		X		15			47	63 67	

H = +7.5 V; L = -7.5 V

TABLE 3 BOARD AA6 ATTENUATOR SELECTION

Data lines				Transistors switched on						Attenuation (dB)
13	15	14	16	1	2	3	4	5	6	
L	L	L	L		X		X		X	0 - 15
L	L	L	H		X	X			X	16 - 19
L	L	H	L	X			X		X	20 - 31
H†	H*	L	L		X		X	X		32 - 47
H†	H*	L	H		X	X		X		48 - 63
H†	H*	H	L	X			X	X		64 - 67
H†	H*	H	H	X		X		X		68 - 80

H = +7.5 V; L = -7.5 V

* For unbalanced outputs only, otherwise 'L'.

†For a balanced output only, otherwise 'L'.

Board AA5 - Programmable attenuator

Circuit diagram : Chap. 7, Fig. 4

46. This board contains the 32 dB attenuator and operating relays. Relay drive is supplied by TR5 and TR6 on board AA6 (see Table 2).

Impedance matching and output

47. When an unbalanced output is selected on the impedance switch the signal from the programmable attenuators is matched on board AA8 and then fed either via board AA9 buffer for 0 Ω or directly for 50 Ω, 60 Ω or 75 Ω, to the OUTPUT socket (see Fig. 13). When a balanced output is selected the signal is taken to AA9 buffer amplifier then matched on board AA10 before being fed to the BALANCED OUTPUT socket. The 32 dB balanced output attenuator on AA10 follows the buffer amplifier in order to ensure a good signal to noise ratio for low output levels.

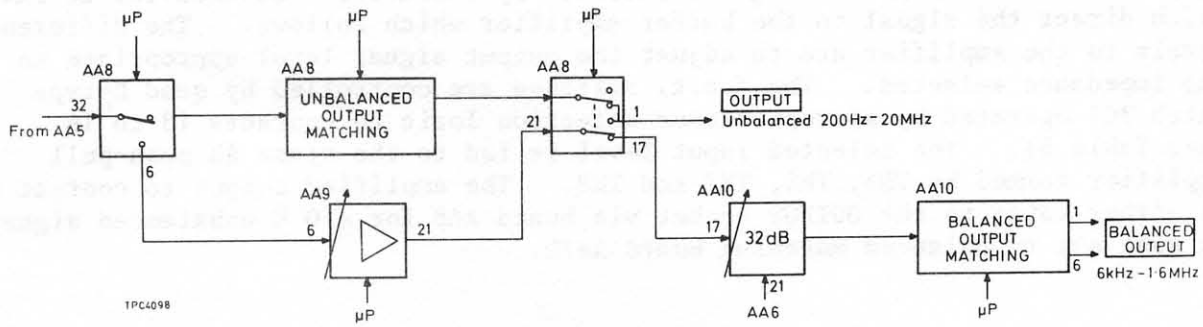


Fig. 13 Impedance matching and output

Board AA8 - Unbalanced matching

Circuit diagram : Chap. 7, Fig. 5

48. This board performs the unbalanced impedance matching as selected on the front panel Ω switch. Microprocessor selection logic to contacts 13 to 16 provide the data for clocked D-latch IC1 which controls relay drive transistors TR1 to TR4. These electronic switches, with diodes D2, D3, D7 and D8, form a decoder for defining the signal path to select the correct output impedance match. A high, for example, on pin 11 IC1 will switch on TR2 as well as forward biasing D3 and D8 so that relays RLA, RLC and RLD are energized. This causes the signal input from balun T1 to be led by RLA and RLC through the 50 Ω unbalanced match formed by R14, R15, R16 and R18, and out to contact 1 and the OUTPUT socket by RLD. The impedance matching for the remaining unbalanced positions of the Ω switch is shown in Table 4. For balanced matching the board relays are not energized and the signal is led by the relays to contact 6 and the balanced matching buffer on board AA9.

TABLE 4 UNBALANCED IMPEDANCE MATCHING

Data lines				*Relays energized*					*Output impedance (and maximum level)*	
13	*14*	*15*	*16*	*A*	*B*	*C*	*D*	*E*		
L	L	L	H					X	Unbalanced	0 Ω (0 dBV)
L	L	H	L	X		X	X		"	50 Ω (3 dBm)
L	H	L	L	X	X		X		"	60 Ω (3 dBm)
H	L	L	L				X		"	75 Ω (10 dBm)
L	L	L	L						Balanced	

Board AA9 - Balanced matching buffer

Circuit diagram : Chap. 7, Fig. 5

49. For a balanced (or a 0 Ω unbalanced) output the signal from contact 6 is fed to a potential divider formed by R7, R8, R9, R10, R30 and R11. Here a proportion of the input voltage is selected by electronic switches TR1 to TR4 which direct the signal to the buffer amplifier which follows. The different levels to the amplifier are to adjust the output signal level appropriate to the impedance selected. The f.e.t. switches are controlled by quad D-type latch IC1 operated by microprocessor selection logic to contacts 13 to 16 (see Table 5). The selected input level is fed to the class AB push-pull amplifier formed by TR5, TR6, TR7 and TR8. The amplified output to contact 6 is either taken to the OUTPUT socket via board AA8 for a 0 Ω unbalanced signal, or sent out to balanced matching board AA10.

TABLE 5 BALANCED MATCHING BUFFER

Data lines				*Transistors switched on*				*Matching*
13	*14*	*15*	*16*	*TR1*	*TR2*	*TR3*	*TR4*	
H	L	L	L				X	0 Ω
L	L	L	H			X		124 Ω
L	L	H	L		X			135 Ω
L	H	L	L	X				150 Ω

H = +7.5 V; L = -7.5 V

Board AA10 - Balanced matching

Circuit diagram : Chap. 7, Fig. 5

50. Latching relay RLA connects the input signal from contact 17 either directly to the output matching circuits or to the preceding 32 dB attenuator. This relay is driven by a complementary pair of transistors TR2 and TR5 which are controlled by logic from board AA6 to contact 21. When, for example, this contact is taken high, TR2 switches on and the signal is directed through the attenuator. Unbalanced to balanced transformer T1 couples the signal to the output matching resistors. These are selected by logic from the microprocessor to contacts 13, 15 and 16 which provide the data for D-type latch IC1 controlling the relay drive transistors TR1, TR2 and TR3. When a transistor is switched on by a high output from IC1, pairs of relays are energized

as shown in Table 6 and the signal is directed to the BALANCED output socket via the appropriate matching resistors. Capacitor C9 provides balanced ratio compensation while C10 provides high frequency return loss compensation.

TABLE 6 BALANCED IMPEDANCE MATCHING

Data lines			*Relays energized*						*Output impedance*
13	*15*	*16*	*B*	*C*	*D*	*E*	*F*	*G*	*(and maximum level)*
L	L	L							0 Ω (0 dBV)
L	L	H		X			X		124 Ω (10 dBm)
L	H	L	X					X	135 Ω (10 dBm)
H	L	L			X	X			150 Ω (10 dBm)

CONTROL UNIT

Microprocessor and memory

51. Microprocessor board AB2 comprises, besides the microprocessor, a clock generator, a RAM bank, a ROM interface and the output ports. Memory board AB3 primarily contains the ROM bank and the input ports. The microprocessor controls the operations of the other component parts by implementing a series of instructions which are stored in memory. Block diagram Fig. 14 shows in simplified form the operation of the microprocessor and memory boards. The microprocessor is shown communicating with the program memory (ROM bank) via the interface by means of a bidirectional 4-line bus. All addresses and instructions to and from the memories are passed on this 4 parallel wire bus. The bus is used to access two types of memory; the read only memory (ROM) contains permanently fixed instructions and data which can only be read out, whilst the random access memory (RAM) is used as a working memory for the temporary storage of data which can be both written into or read out from memory. Unlike the ROM the RAM loses its stored data when the instrument

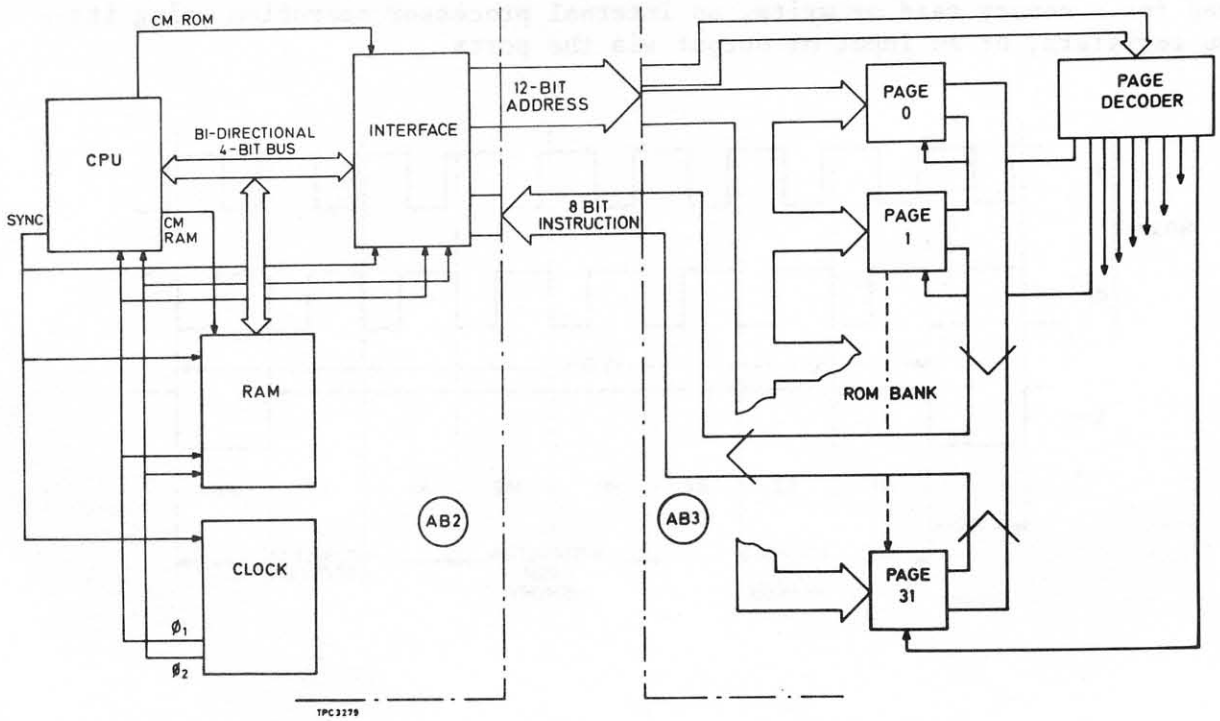


Fig. 14 Microprocessor and memory

is switched off. From the ROM interface, three 4-bit groups are latched out to form a 12-bit address which is sent to access the program memory and results in an 8-bit instruction being returned as shown. Part of the memory address is decoded by the page decoder which selects one of the 32 pages of memory held in the ROM bank. Each new instruction cycle is identified by a synchronizing pulse sent out from the microprocessor on the SYNC line. The clock generator supplies the necessary two-phase timing for the processor.

Board AB2 - Microprocessor

Circuit diagram : Chap. 7, Fig. 12

Clock generator

52. Clock generator IC1 provides two clock outputs at the different phases necessary for the overall timing of the microprocessor, RAMs and memory interface. The output from external crystal XL1 is divided by 7 internally by IC1 to provide clock outputs at 740 kHz at phases Φ1 (pin 14) and Φ2 (pin 3). To ensure that the program is restarted when the instrument is switched on, a reset pulse is generated from pin 13 with a power-on delay period determined by the time constant of R4 and C7.

Microprocessor

53. Microprocessor IC2 controls the overall activities of the microprocessor and memory boards. In order to synchronize these activities a SYNC pulse is generated at pin 16 to indicate the start of an instruction cycle. The complete instruction cycle takes 10.8 µs and is divided into 8 equal periods by the Φ1 and Φ2 clock inputs from IC1 (see Fig. 15). The first three periods A1, A2, and A3 are used to present a 12 bit (three groups of 4 bits) instruction address to the memory. Fourth and fifth periods M1 and M2 are used to read the instruction byte from the memory. The remaining three periods X1, X2 and X3 are used for program execution. These execution periods may be used for a memory read or write, an internal processor operation using its own registers, or an input or output via the ports.

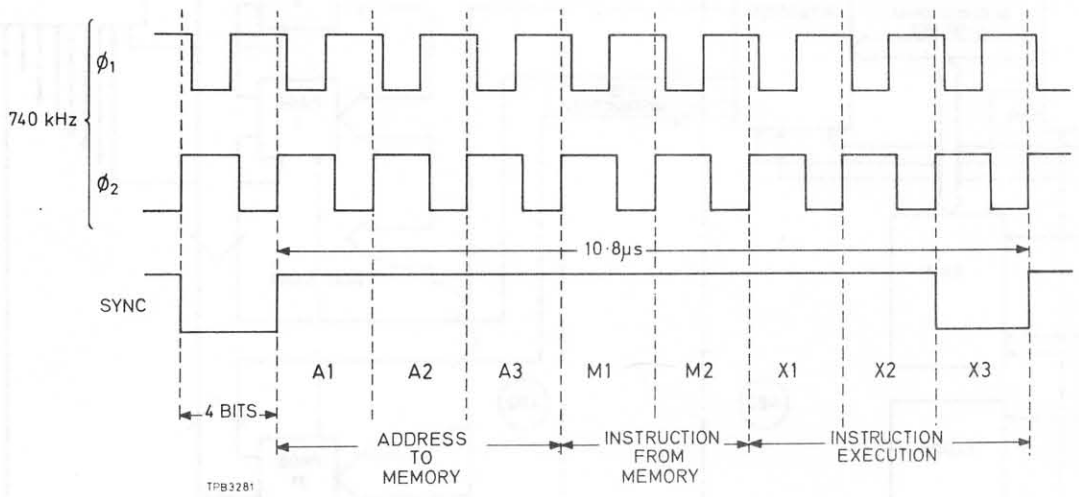


Fig. 15 Microprocessor timing

54. Pins 1 to 4 of the microprocessor connect to the bi-directional data bus which conveys addresses and data to and from the RAMs as well as addresses to and instructions from the ROMs via memory interface IC3. Outputs from pins 22 and 23 provide the CM ROM signals used for ROM bank selection.

Memory interface

55. The purpose of interface IC3 is to communicate with the ROM banks on board AB3 containing the program memory and input ports. Address information sent by the microprocessor during periods A1, A2 and A3 (see Fig. 15) on pins 1 to 4 is latched out by IC3 and presented as a 12-bit address to the memory as the ADDRESS signal on pins 23 to 26 during period A1, pins 27 to 30 during period A2 and as the CHIP SELECT signal on pins 31 to 34 during period A3. The 8 bit instruction code returned from the memory is passed to pins 5 to 8 as operator OPR, and pins 9 to 12 as operand OPA. These are then multiplexed in the interface and transferred to the microprocessor by means of the data bus to pins 1 to 4 in two 4 bit words during periods M1 and M2.

56. Overall command of the interface and hence of the ROM bank is exercised by the microprocessor. Pins 18 (IN) and 19 (OUT) control the direction of data flow to and from front panel, GPIB etc. IN enables data and instructions to be accepted from ROM board AB3 on the I/O lines to pins 36 to 39 of the interface. When OUT is set low it enables binary-to-decimal decoder IC4 to select one of the latches IC9 to IC1 for passing data out from the interface. Latch selected is determined by the logic on the CHIP SELECT lines.

Random access memories

57. IC5 and IC6 perform two distinct functions. As memories they each store 320 bits arranged in 4 registers of sixteen 4-bit characters plus four special, status characters (see Fig. 16). The registers are used for temporary storage and are similar to the pages of the ROMs. The RAMs also provide output ports via output buffers IC7 and IC8. IC5 output provides the main data bus for sending information to various parts of the instrument, e.g. frequency synthesizer, programmable attenuators. IC6 output provides data for the front panel.

Board AB3 - Memory

Circuit diagram : Chap. 7, Fig. 12

Read only memories

58. The memory bank comprises IC1, IC3, IC5 and IC8. These are ultra-violet erasable, programmable, ROMs each consisting of 8 pages of memory. Each page may be considered as a matrix of 16 rows each of 16 words with each word comprising 8 bits (see Fig. 16). Total memory capacity of the four IC memory is therefore 8192 8-bit instructions. Access to the memory is by a 12-bit address from the interface on board AB2 and comprises three 4-bit groups which are sent in the timing periods A1, A2 and A3. Period A1 is used to define the page, A2 the row and A3 the word.

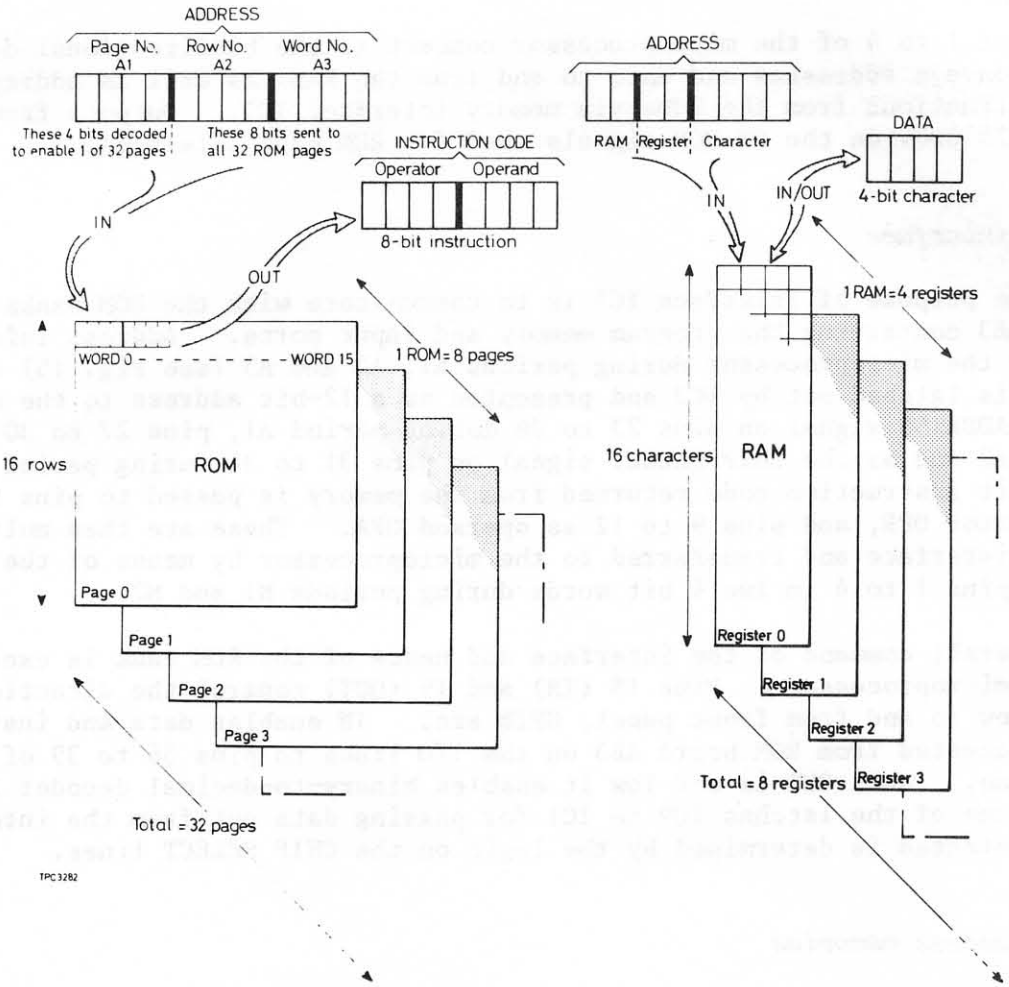


Fig. 16 Memory operation

59. Eleven of the twelve address inputs from board AB2 are passed through a level shifter formed by ICs 11, 12a and 13a and then on the ADDRESS lines to the ROMs. Thus all ROMs are addressed simultaneously; all that remains is to enable the appropriate ROM in order to select just one of the 2048 instructions in each ROM. This is the function of the CM ROM lines to R-S latch IC4a and the C3 CHIP SELECT line to the binary to 1 of 4 decoder IC2a. One of IC2a $\overline{Q}$ outputs goes low to enable a ROM to place the addressed byte onto the output lines to board AB3 via buffers IC9. A block diagram showing board AB2 and AB3 operation is given in Fig. 17. Decoder IC2a is enabled by the interface IC on board AB2 setting the IN line high to the base of electronic switch TR1 which then switches on to set pin 1 low.

Input ports

60. Data from the ROM input ports is taken via the interface to the microprocessor from quad bilateral switches IC6 and IC7. Operation of the switches is determined by the settings of the CHIP SELECT lines C0 and C1 which control binary decoder IC2b. A low output from either $\overline{Q0}$ or $\overline{Q3}$ is inverted in Schmitt NANDs IC4b to enable all four switches in either IC6 or IC7. GPIB messages are received at ROM port 3 and those from the front panel switches and display are fed in to ROM port 0.

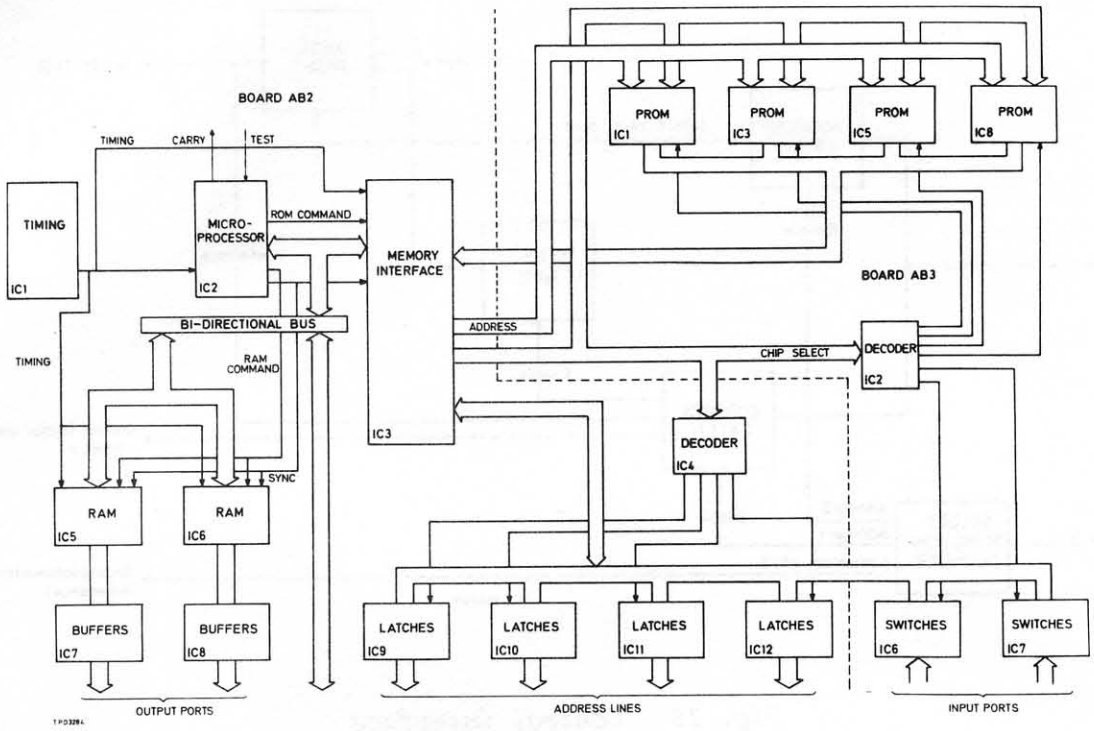


Fig. 17 Microprocessor boards

Board AB4 - Control interface

Circuit diagram : Chap. 7, Fig. 14

Function selection

61. Inputs from ROM 2 to contacts 3 to 6 implement general instrument control by means of address decoder IC5. IC5 decoded addresses 2 to 9 provide enable signals for such functions as attenuation and impedance matching (see Fig. 18) for which the data are supplied by RAM 1. Decoder address 1 provides the enable signal for 8-bit addressable latch IC4 whose outputs supply control signals for such purposes as stopping the tuning motor or providing the SYNC output. To select the required operation, decoder address 1 is taken high to switch on IC6d which sets write enable pin 4 of IC4 low to allow the input of new data from RAM 0.

Test signals

62. Decoder address 0 enables the operation of address latch IC2 whose RAM 0 data inputs control multiplexer IC3. This IC selects 1 of 8 test inputs for passing to the microprocessor test input via contact 24. One of the multiplexer inputs is from 16 Hz timer IC1. This signal determines the rate at which the display flashes for an out of range condition or an invalid data entry. Timer output is also used by the microprocessor for the time delay in seconds between the steps of a sequence mode operation. To indicate when the GPIB boards are fitted, board AB16 links the negative rail to contact 8 and this signal is passed out to the microprocessor when the base of IC6c is taken high by latch IC4.

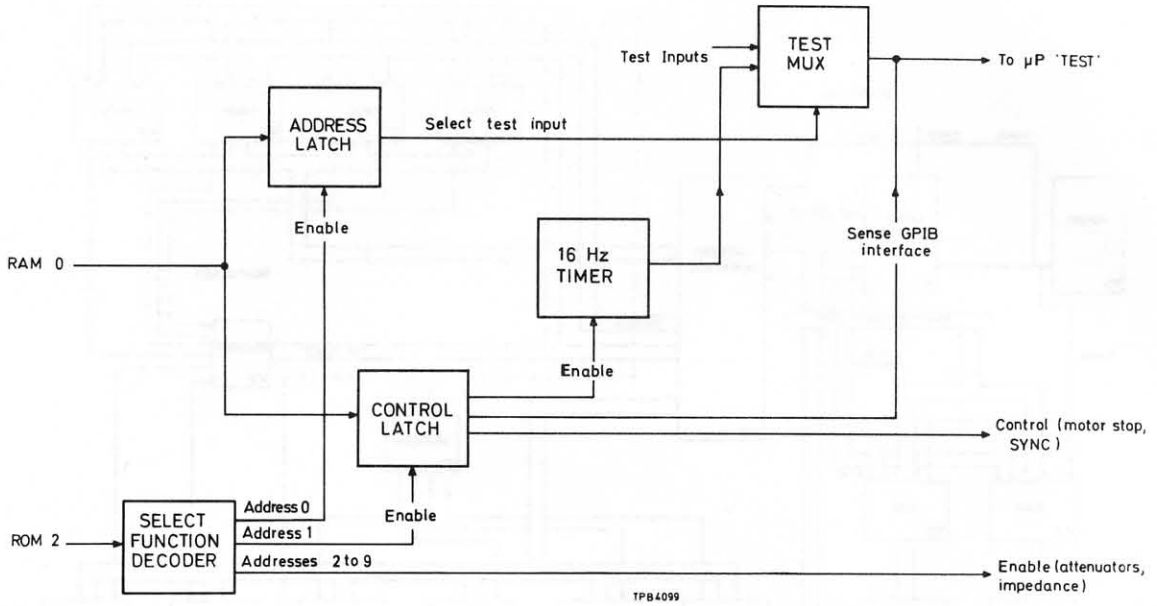


Fig. 18 Control interface

POWER SUPPLY UNIT

63. The a.c. supply is fed from the supply connector and filter and then via the SUPPLY selector and a.c. fuse to the 115/230 V voltage selector and the primary of the mains transformer. The two halves of the primary of the transformer are connected in series for 230 V and in parallel for 115 V according to the position of the SUPPLY VOLTAGE selector. There are two secondary windings. One secondary and bridge rectifier feeds to the GPIB interface while the other provides power for both battery charging and instrument operation.

64. With the SUPPLY selector set to ∿ for a.c. operation both secondary windings of the mains transformer supply power (see Fig. 19). Instrument power is supplied from two full-wave rectifiers, to 12 V regulators on board AB12 feeding to 5 V regulators on board AB15 and 7.5 V regulators on boards AB1. 12 V regulated outputs also fedd to the memory (+12 V) and GPIB interface (-12 V) boards. This secondary also supplies a trickle charge for the battery during a.c. operation to a maximum of 40 mA. The other secondary and bridge rectifier feeds to the +5 V regulator on board AB15 which supplies power to the GPIB interface board.

65. When the SUPPLY selector is set to CHARGE, the CHARGE lamp lights and the output from the secondary normally supplying instrument power is fed to the battery via the charge control circuit on board AB11 (see Fig. 20). Maximum charge is 400 mA.

66. For battery operation the SUPPLY selector is set to BATT and the output provides power for normal instrument operation except that power is not supplied to the GPIB interface board (see Fig. 21).

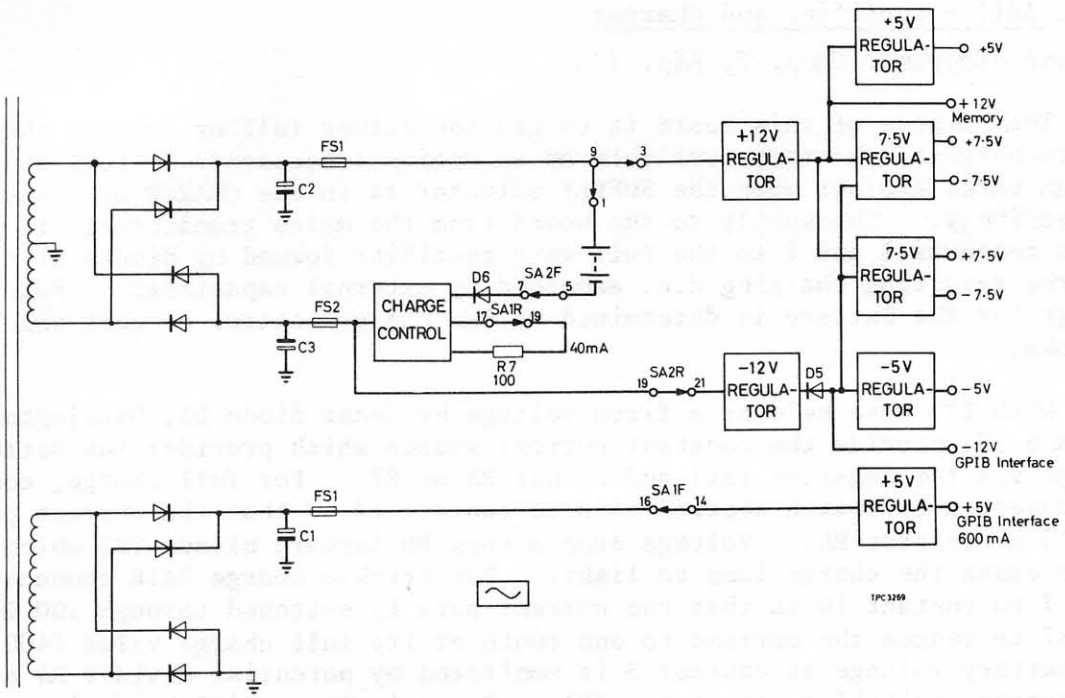


Fig. 19 AC operation with SUPPLY switch set to ∿

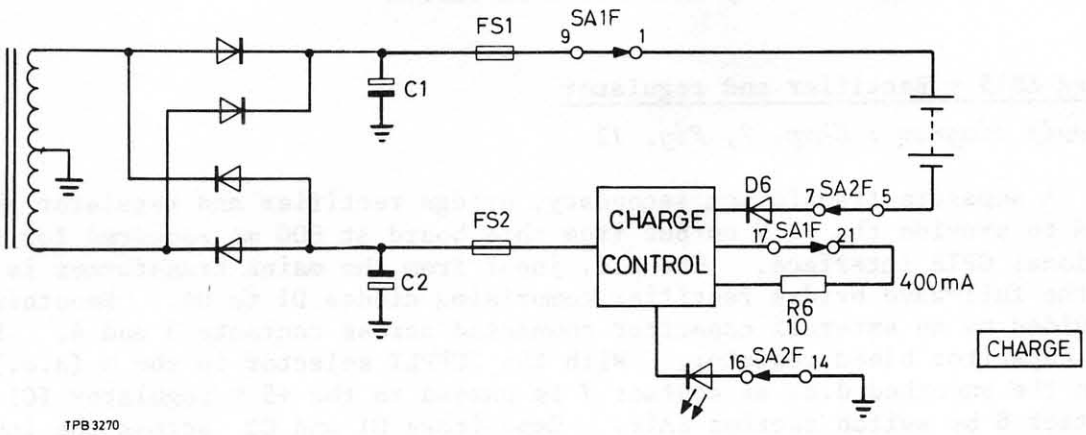


Fig. 20 Charge operation with SUPPLY selector set to CHARGE

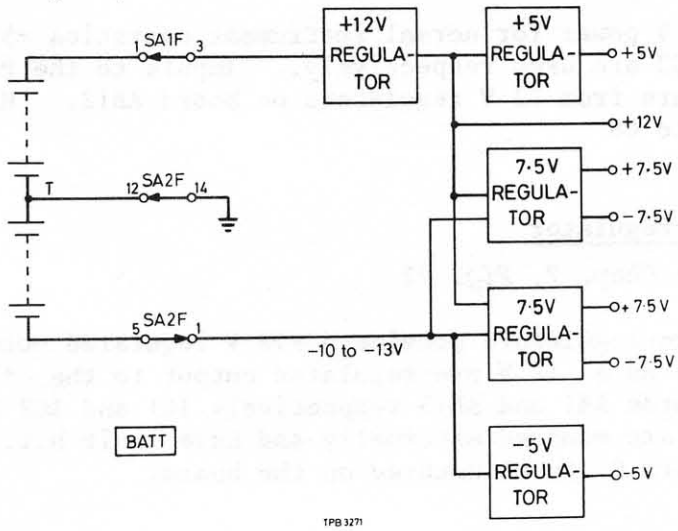


Fig. 21 Battery operation with SUPPLY selector set to BATT

Board AB11 - Rectifier and charger

Circuit diagram : Chap. 7, Fig. 11

67. The purpose of this board is to provide either full or trickle charge for the rechargeable battery available as an optional accessory. Full and trickle charge rates are set when the SUPPLY selector is in the CHARGE or ∿ positions respectively. The supply to the board from the mains transformer is passed in at contacts 1 and 2 to the full-wave rectifier formed by diodes D1 to D4 and the resulting charging d.c. smoothed by external capacitors. Rate of charge for the battery is determined by the charge control circuit which follows.

68. With TR3 base held at a fixed voltage by Zener diode D5, Darlington pair TR3 and TR4 provide the constant current source which provides the battery charge via the negative rail and either R6 or R7. For full charge, contact 7 is connected by switch section SA1R to contact 17 so that the current path is via 10 Ω resistor R6. Voltage drop across R6 forward biases TR2 which switches on to cause the charge lamp to light. For trickle charge SA1R connects contact 7 to contact 10 so that the current path is switched through 100 Ω resistor R7 to reduce the current to one tenth of its full charge value (400 mA). The battery voltage at contact 3 is monitored by potential divider R4 and R5 and current switching transistor TR1. For a fault condition causing contact 3 voltage to rise (e.g. due to faulty battery cells) TR1 conducts causing TR3 and TR4 to switch off to prevent charging taking place. Diode D6 protects against accidental battery connection reversal.

Board AB15 - Rectifier and regulator

Circuit diagram : Chap. 7, Fig. 11

69. A separate transformer secondary, bridge rectifier and regulator are used to provide the +5 V output from this board at 600 mA required for the optional GPIB interface. The a.c. input from the mains transformer is passed to the full-wave bridge rectifier comprising diodes D1 to D4. Smoothing is provided by an external capacitor connected across contacts 3 and 4. R1 is the capacitor bleed resistor. With the SUPPLY selector in the ∿ (a.c.) position the smoothed d.c. at contact 7 is passed to the +5 V regulator IC1 at contact 8 by switch section SA1F. Capacitors C1 and C2 across the input and output of IC1 respectively serve to prevent h.f. oscillation.

70. To supply 5 V power for normal instrument operation +5 V and -5 V regulators IC2 and IC3 are used respectively. Inputs to the regulators at contacts 10 and 11 are from 12 V regulators on board AB12. HF oscillation is prevented by C3 to C6

Board AB12 - Pre-regulator

Circuit diagram : Chap. 7, Fig. 11

71. The ±12 V pre-regulators provide a ±12 V regulated output to memory board AB3 as well as a 12 V pre-regulated output to the ±7.5 V and ±5 V regulators on boards AB1 and AB15 respectively. IC1 and IC2 are the voltage regulators which are mounted externally and have their h.f. oscillation suppression capacitors C1 to C4 mounted on the board.

Board AB1 - ±7.5 voltage regulator

Circuit diagram : Chap. 7, Fig. 11

Positive regulator

72. In the +7.5 V regulator, TR6 and TR7 provide a constant current source for the low temperature coefficient Zener diode D1. D1 thus provides a very stable reference of 5.6 V to the inverting input of differential amplifier IC1. The non-inverting input to IC2 is supplied by the output voltage sensing circuit formed by potential divider R7, R8 and R9. IC1 output supplies the base drive for the high current gain combination TR2 with power transistor TR1 which together form a series pass amplifier. Protection is provided by TR3.

Negative regulator

73. The -7.5 V regulator is similar to the +7.5 V regulator and comprises differential amplifier IC2 and series pass amplifier TR9 and TR10. In this regulator the inverting input to IC2 is connected to earth which supplies the reference voltage. Since the non-inverting input of IC1 is connected to the mid-point of potential divider R19 and R20 across the two output rails, the negative regulator is caused to track the positive regulator.

Regulator operation

74. Any decrease in output voltage, for example from the positive regulator, is detected by the potential divider which decreases the voltage applied to the non-inverting input of differential amplifier IC1. This decreases IC1 output voltage which thus increases the potential difference between IC1 pin 6 and the positive rail. This causes TR2 base drive to rise so increasing its collector current. Since TR2 collector defines the base current for power amplifier TR1 the current through the output load is increased which raises the output voltage to its former value.

Protection

75. Protection against short circuit or a faulty battery condition is provided. Under such fault conditions both 7.5 V output voltages are reduced immediately. In the case of the positive rail being shorted to earth IC1 non-inverting input is taken low which drives TR2 and TR3 hard on. This current, which is limited by R3 and R5 causes the +12 V pre-regulator IC1 to cut off which in turn shuts down the AB1 positive regulator. Since the negative regulator tracks the positive regulator, this will also switch off. A negative voltage is applied to the non-inverting input to IC2 whose output reduces the potential difference across potential divider R14, R15 and R16 so that TR9 base is no longer foward biased. With TR9 off, the base of TR10 is taken to earth via R22 causing the transistor to switch off.

76. When the -7.5 V rail is shorted to earth, IC2 non-inverting input sets the output high and TR9 and TR10 are driven hard on. The high current from the -12 V pre-regulator IC2 causes the IC to cut-off which in turn disables the AB1 negative regulator. Shorting the -7.5 V rail also shuts down the positive regulator and this is the function of electronic switch TR3. The short circuit connects potential divider R19 and R20 across the positive rail and earth so that TR3 is forward biased and it switches on. This shorts out

the reference voltage across D1 causing the positive output voltage to collapse.

DISPLAY UNIT

Summary

77. The display unit is shown in block diagram form in Fig. 22. The unit has at its heart a multiplexer on board AB9 by means of which the ADDRESS INPUT selects data either to be passed to the microprocessor to show e.g. a switch has been operated, or to cause a display or panel l.e.d. to illuminate. The associated manual tuning operation is shown in block diagram Fig. 23. The manual TUNING control generates signals to signify direction and rate of tuning.

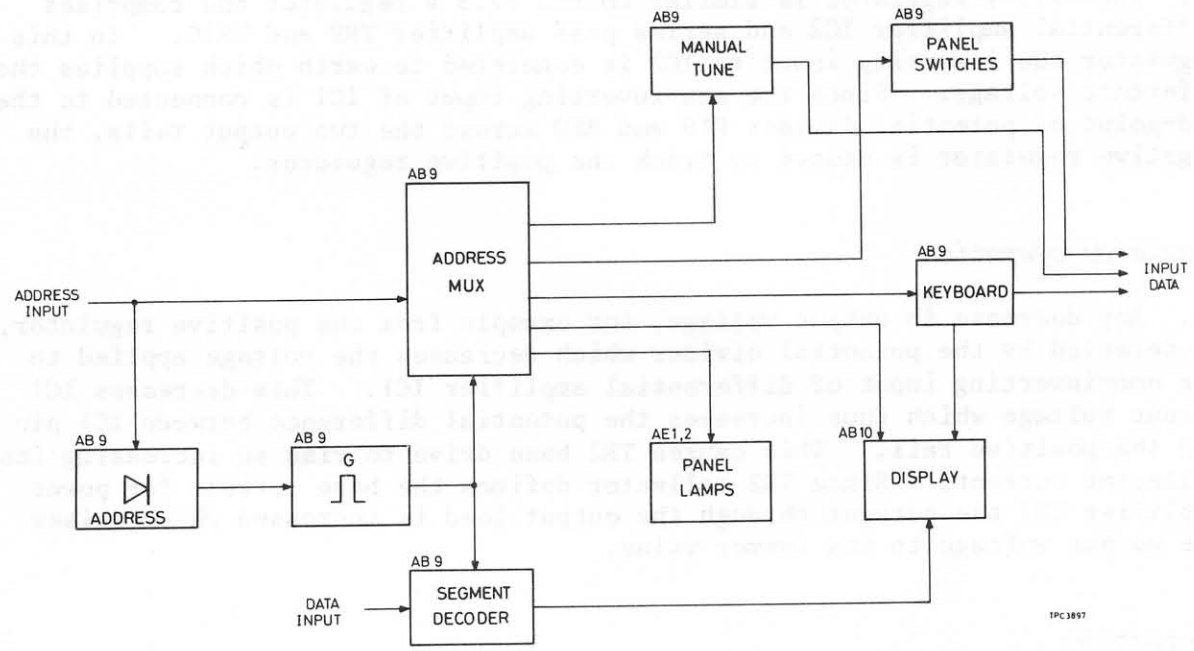


Fig. 22 Display unit

Display operation

78. Flow diagram Fig. 24 shows the operation of the system. At the commencement of a cycle address 00000001 is sent by the microprocessor which selects RAM 0 and register 0 and automatically selects RAM 0 output port and ROM 0 input and output ports. The contents of line 1, describing the first character to be displayed, is sent from RAM 0 output port. Data is sent from ROM 0 output port as the address for the first display module. Thus the character described in line 1 of register 0 of RAM 0 is displayed on module 1. The data on the ROM 0 output bus is then returned to zero in

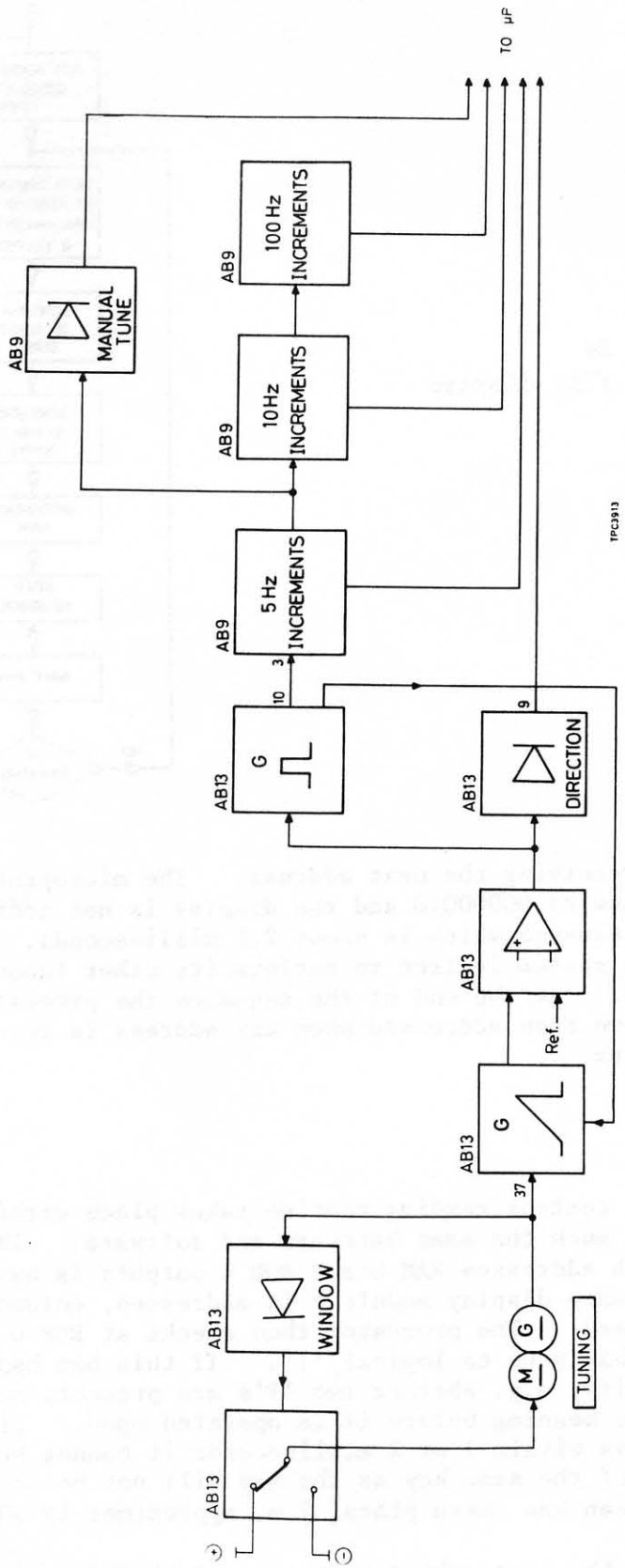


Fig. 23 Manual tuning

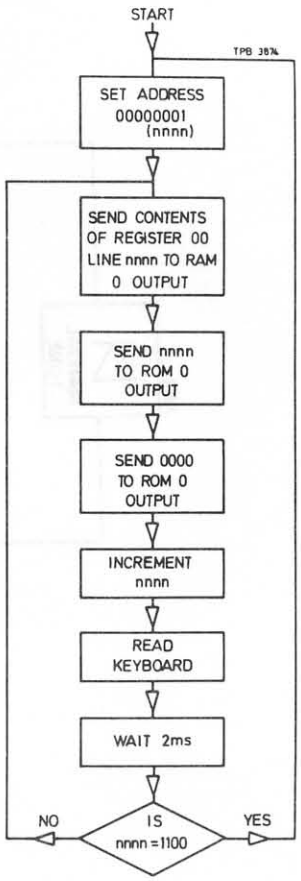


Fig. 24
Display system flow diagram

in preparation for receiving the next address. The microprocessor then increments the address to 00000010 and the display is not addressed again until the end of a sequence which is about 2.5 milliseconds. During this period the processor system is free to perform its other functions such as reading the keyboard. At the end of the sequence the process is repeated until all modules have been addressed when the address is reset to 00000001 and the cycle restarts.

Keyboard operation

79. The front panel control reading routine takes place within the display scan period and uses much the same hardware and software. This is because the instruction which addresses RAM 0 and ROM 0 outputs is used to address ROM 0 input. Thus when display module 1 is addressed, column 1 of the keyboard is also addressed. The processor then checks at ROM 0 input to see if any of the lines has gone to logical '1'. If this has happened, the input is checked for validity, e.g. whether two '1's are present, and then decoded to give its effective meaning before it is operated upon. Since contact bounce normally decays within 1 or 2 milliseconds it cannot be interpreted as repeated operations of the same key as the key will not be accessed again until a complete display scan has taken place, i.e. approximately 30 milliseconds.

80. The majority of the keys make momentary contact and can be serviced as described above. However, where the switches are 'permanently' closed, e.g. impedance and external levelling selectors, the readings on successive scans are compared and action is only taken when a change is observed.

Board AB13 - Motor control

Circuit diagram : Chap. 7, Fig. 13

Sensing circuits

81. When the tuning knob is rotated a voltage, the polarity of which is determined by the direction of rotation, is generated and applied to the input of the integrator formed by IC3 and C1. When the output from the integrator exceeds the threshold voltage at the input of either of the comparators IC4 or IC5, the monostable formed by IC6c and IC6d is triggered producing a pulse which is fed via IC6e to output contact 10 and then to the gate of f.e.t. TR4 thus discharging C1. At the same time the output of the relevant comparator triggers the R-S bistable formed by IC6a and IC6b to give an UP/DOWN indication at contact 9. Continuous rotation thus results in a train of pulses whose rate is proportional to the speed of rotation, at contact 10, and direction information at contact 9. Overall operation is shown in Fig. 25.

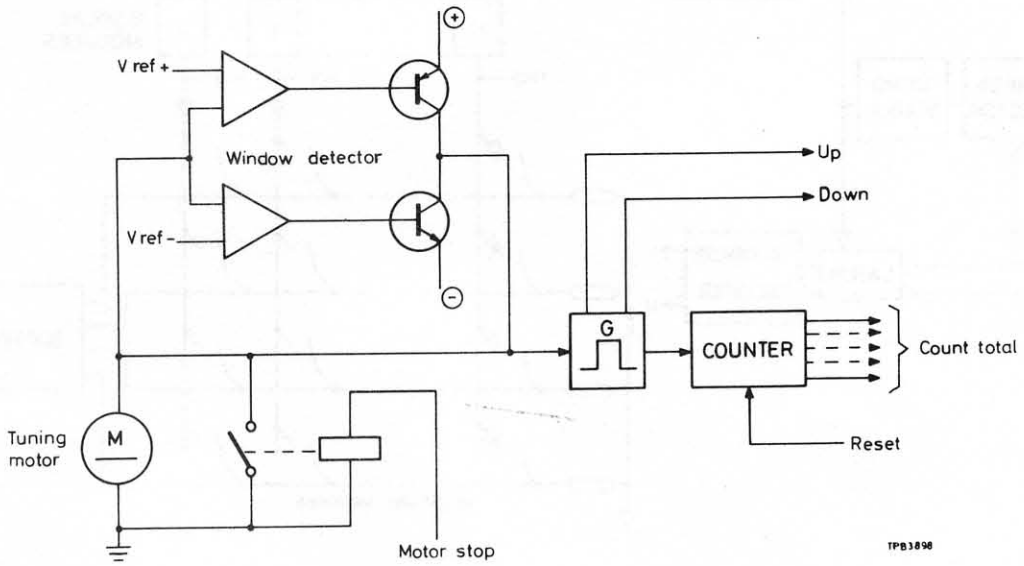


Fig. 25 Manual tuning system

Electronic flywheel

82. When the manual tuning knob is spun quickly tuning continues automatically because of the electronic flywheel action of the circuit. A clockwise spin results in a positive voltage being generated by the motor. If this voltage exceeds the threshold of comparator IC1, TR1 is switched on which connects the motor via Zener diode D1 and the resistor R1 to the positive rail thus latching the motor on so that it runs continuously. Similarly, giving the tuning knob an anti-clockwise spin will switch on TR2 connecting the motor via Zener diode D2 and resistor R2 to the negative rail. At the end of the tuning range or when a data key is pressed, motor stop relay RLA short circuits the motor to stop the tuning. Eddy current braking also stops the motor from continuing to spin.

Board AB9 - Keyboard

Circuit diagram : Chap. 7, Fig. 13

Summary

83. Front panel switch or keyboard operation is converted by the circuits on this board into uniquely identified signals to the microprocessor. The microprocessor responds by performing the function and/or illuminating the display. For the latter purpose, microprocessor ADDRESS INPUT lines to the board are decoded to determine which 1.e.d. on display board AB10 is to be illuminated, while the DATA INPUT lines determine the character to be displayed. Board AB9 also translates manual tuning inputs from motor control board AB13 into rate and direction of tuning signals for passing to the microprocessor. Overall operation of the board is shown in Fig. 26 while the functions the decoder performs are summarized in Table 7.

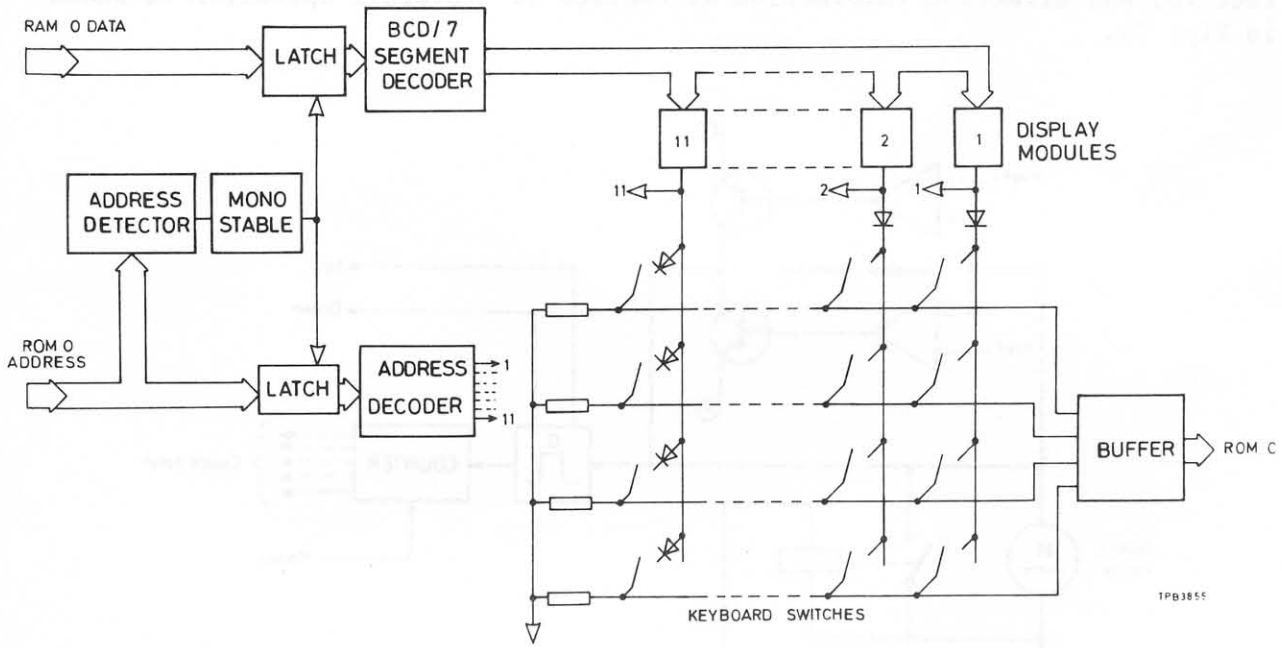


Fig. 26 Keyboard and display operation

TABLE 7 DECODER FUNCTION SUMMARY

Decoder address	*Functions*
1 - 7	Read keyboard. Enable frequency display.
8 - 11	Enable level display.
8	Enable EXT LEVELLING indicators. Unbalanced output selected.
9	Enable ENTER lamp. Balanced output selected.
10	Read OUTPUT OFF/SEND, manual tune direction and 5 Hz increments.
11	Read 10 Hz increments.
12	Read 100 Hz increments.
14	Reset.

Display operation

84. Selection of a particular l.e.d. to be illuminated is achieved by microprocessor signals on ADDRESS INPUT lines 4 to 7 which form the data inputs to D-type latch IC5. A high on any of these lines is detected by diodes D30 to D33 which form a 4-input OR gate, and the positive-going edge of the detected signal is used to trigger monostable IC4. The resulting negative pulse clocks IC5 transferring the data to the decoder formed by ICs 6 and 7. The multiplexed outputs form addresses which activate the functions shown in Table 7. Thus for high outputs on IC5 Q1 and Q3 address 10 is selected by IC7. Address 10 performs multiple functions; the signal to diodes D12 and D13 enables manual tuning to be detected by the microprocessor, while the output to D27 selects a display l.e.d. for illumination and passes the state of the OUTPUT OFF/SEND switch out to the microprocessor.

85. Selection of the character to be displayed is achieved by microprocessor signals on DATA INPUT lines 21 to 24 and passed to b.c.d. to 7 segment decoder IC1 and exclusive-OR gates IC2. IC1 converts the b.c.d. inputs to outputs to drivers on board AB10 which select the segments for illumination to produce the displayed character. The purpose of IC2 and IC3 is to provide selection of decimal point and negative sign. For this purpose, IC2 gating performs the character recognition function such that only when all gate outputs are high will a logical '1' be passed to latch IC3. The high on pin 13 IC3 is clocked by the negative-going pulse from monostable IC4 to pin 8 IC3 and this sets output pin 3 high (see Table 8). This output is taken to a drive transistor on board AB10 which causes a decimal point or a negative sign to be displayed when selected by decoders IC6 and IC7.

Manual tuning logic

86. There are two inputs from motor control board AB13. These inputs are logic signals to input line 2 which provide the direction of tuning indication and a pulse train at input line 3 indicating the amount by which the frequency is to be incremented or decremented. These two inputs enable the pulses to be counted and then added to, or subtracted from, the current frequency. The displayed frequency is then seen to alter as the manual TUNING knob is turned.

TABLE 8 AB9 LATCH TRUTH TABLE

IC3				
Inputs				*Output*
Pin 8	*Pin 13*	*Pin 6*	*Pin 1*	*Pin 3*
H	L	L	L	L
H	H	L	L	L
L	H	H	L	H
L	L	L	H	L

H = +7.5 V; L = -7.5 V

Tuning indication

87. When the instrument is tuned manually, the tuning pulses clock IC11a whose $\bar{Q}$ output is connected to its D input so that it divides by 2. The Q output of IC11a is connected to the clock input of the D-type bistable IC11b so that when manual tuning is taking place, its Q output SENSE TUNING is set high. This information is accessed on line 3 (contact 11) when the gate formed by D14, TR3 and D20 is enabled at address 9. At the end of the front panel scan, i.e. address 14, the Q outputs of ICs 11a and 11b are reset low.

Tuning direction

88. Direction information UP/DOWN from the motor control circuit is accessed on line 2 (contact 14) when the gate formed by D12, TR1 and D19 is enabled at address 10. The microprocessor uses this information to determine whether to increment or decrement the frequency of the synthesizer.

Frequency incrementing

89. The output of IC11a is also used as the least significant bit of count and is taken via the gate formed by D13, TR2 and D15 to line 0 (contact 16) at address 10. If it is a high this signal causes the microprocessor to increment or decrement the frequency synthesizer by 5 Hz.

90. The $\bar{Q}$ output of IC11a representing 10 Hz frequency increments is used to clock a two decade counter consisting of IC13, least significant decade, and IC12, most significant decade. By connecting the CARRY output of IC12 via exclusive-OR gate IC2c (wired to act as an inverter) to the clock enable input of IC13, the maximum count is limited to 90. Thus the maximum frequency count is limited to 905 Hz. The count data is accessed by means of bilateral switches IC16 and IC14 at addresses 11 and 12 respectively. This information is read by the microprocessor which then increments or decrements the frequency synthesizer accordingly. As with the tuning indication, the counter is reset at address 14.

Keyboard and switch operation

91. When a key is pressed it connects one of the microprocessor input lines to a diode which is connected to one of the output lines from the address decoder. As the address line is normally at '0' the diode is reverse biased so that the input line is unaffected. When that diode is addressed, the address line goes high, forward biasing the diode and connecting a logical '1' to the appropriate microprocessor input line. The information is read by the microprocessor which can then identify which key has been pressed and take suitable action. For example, pressing key 3 will be interpreted as the b.c.d. number 0011 which will be stored in RAM and also sent to the b.c.d./7-segment decoder to display the figure 3.

92. For switches which are latched, individual diodes are used to isolate them from the input data lines when they are not addressed. Similarly the multi-position impedance selector is isolated by means of D17 and D18.

Board AB10 - Display

Circuit diagram : Chap. 7, Fig. 13

Frequency display

93. The seven frequency display 1.e.d's D5 to D11 are sequentially selected for illumination by addresses 1 to 7 from board AB9. All have 7 cathode segments except for the display 1.e.d. selected by address 7 which has only three. This is because it need only display the figure 1 for a frequency between 10 MHz and 19 MHz and the minus sign for a frequency decrement. Selection of the 1.e.d. for illumination is by a high address input from the multiplexed decoder output from board AB9 to one of the bases of electronic switches TR13 to TR19, while cathode segment selection is by drivers TR1 to TR7. The floating decimal point is selected by addresses 1 to 16 and the negative sign by address 7 with the cathode driven by TR8.

Level display

94. Level is displayed on 1.e.d's D1 to D4 which are sequentially illuminated by addresses 8 to 11. Address 11 selects the three-segment 1.e.d. which displays the negative sign and the figure 1 for a minimum level reading. LED illumination selection is by drivers TR9 to TR12. Driver TR8 performs a multiple role. Besides that of illuminating the figure 1, it also illuminates the ENTER 1.e.d. for address 9 and the EXT LEVELLING 1.e.d.s on board AE1 for address 8. For the level display the decimal point position is fixed.

Board AE1 - Lamps

Circuit diagram : Chap. 7, Fig. 13

95. This small board contains a switching transistor and the three EXT LEVELLING 1.e.d.s which illuminate to show when the level is in or out of range. Logic to activate electronic switch TR1 is supplied from display board AB10. When the level is within range, 1.e.d. D3 illuminates. When the level is out of range either D4 or D5 illuminates by being switched into circuit and in parallel across 1.e.d. D3 and diodes D1 and D2. This action reduces the voltage applied to D3 which then extinguishes.

Board AE2 - Remote lamp

Circuit diagram : Chap. 7, Fig. 13

96. The REMOTE lamp on this board illuminates when the instrument is operating under remote control. A high input applied to the base of electronic switch TR1 switches it on which connects the positive rail to the anode of 1.e.d. D1 causing it to illuminate.

LOCAL OSCILLATOR UNIT

Crystal oscillator

97. A temperature compensated crystal oscillator provides the internal 10 MHz standard on local oscillator board AD1. This standard may be automatically disabled by the connection of an external standard, e.g. from the receiver for synchronous operation, to the 10 MHz STD - EXT IN socket. An output at 10 MHz is provided for the frequency tripler on board AA11, while for internal use a 10 MHz output provides the reference for the first p.l.l. mixer on board AD3. The 10 MHz signal is then divided by 5 and the resulting 2 MHz is taken to the second p.l.l. mixer on board AD5. Further division by 10 results in a 200 kHz output and this is fed to the first p.l.l. phase detector on board AD2. Fig. 27 shows the circuit block diagram.

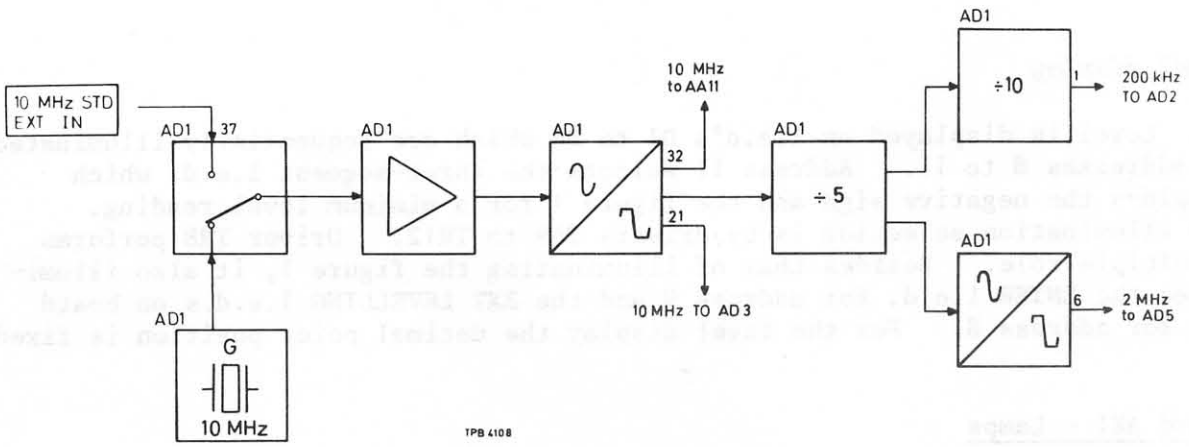


Fig. 27 Crystal oscillator circuits

Board AD1 - Crystal oscillator

Circuit diagram : Chap. 7, Fig. 6

Standard selection

98. Switching is performed automatically to enable the instrument to operate from either the internal or an external 10 MHz frequency standard. This is achieved by electronic switches TR1 and TR2 with diodes D1 and D2. With no external standard connected, TR1 connects the negative power supply to the crystal oscillator to enable it to operate, while D1 connects the output to amplifier TR3. When an external standard is connected to the 10 MHz STD - EXT IN socket a d.c. path is formed between contact 37 and earth. This switches TR2 on switching TR1, and hence the crystal oscillator, off. At the same time the junction of R5 and R20 is taken negative reverse biasing D1 and ensuring that D2 is forward biased providing a path for the external oscillator signal to the base of TR3.

Limiters

99. From amplifier TR3 the oscillator output is passed to emitter follower TR4. TR4 with grounded-base amplifiers TR5, TR6 and TR7 form limiters which provide three buffered outputs. Outputs to transformers T2 and T3 respectively couple the 10 MHz square wave to frequency tripler board AA11, and to interpolation variable divider board AD3. A third output, from TR5, is taken to IC1 which divides by 5 to produce an output of 2 MHz. This output takes two paths. From IC1 pin 8 one path is to D5 and TR8. D5 is used to shift the bias level to ensure the correct operation of grounded-base amplifiers TR9 and TR10 which each form limiters in conjunction with TR8. Output from TR10 is taken via contact 6 to phase detector board AD5.

Decade divider

100. The output of IC1 at the t.t.l. logic levels (necessary to achieve the high operating frequency) is converted to the c.m.o.s. logic levels for decade divider IC2 by the action of electronic switch TR11. When the output of IC1 goes positive, TR11 switches on taking the input of IC2 to approximately -7 V. The negative excursion is clamped at -0.7 V relative to the emitter of TR11 by D4 so that TR11 switches off taking the input of IC2 to the positive rail. The resulting 200 kHz is fed to board AD2 via contact 1.

First phase locked loop

101. The first phase locked loop is formed by boards AD2, AD3 and AD4 (see block diagram, Fig. 28). The 200 kHz input from AD1 is divided by 400 to provide a 500 Hz reference to the phase detector. Phase comparison is achieved by sampling a ramp generated by an integrator and the 500 Hz reference frequency at a rate determined by the output from the programmable divider on board AD3. The resultant d.c. is added to the coarse tuning voltage and fed to the v.c.o. on board AD4 to tune it over the frequency range from 12 to 12.9995 MHz. The coarse tuning voltage is derived by a digital to analogue converter from the most significant digit information to the programmable divider. In the context of overall operation, an r.f. increment of 5 Hz causes the v.c.o. to increment by 500 Hz. The v.c.o. range thus represents an r.f. excursion of 10 kHz to a resolution of 5 Hz. At, for example 1 MHz, oscillator operating frequency is 12 MHz, at 1.001 MHz it is 12.1 MHz and at 1.01 MHz it is again 12 MHz.

102. VCO output is mixed on board AD3 with 10 MHz from the freuqncy standard and the resulting 2 to 3 MHz signal is fed to the programmable divider. The fine frequency divider output at 500 Hz is us4d to control the operation of the sample and hold circuit forming part of the phase detector on board AD2. VCO output is also fed via a divide by 5 counter to the programmable dividers on AD4 providing coarse frequency division. For the coarse frequency multiples of 10 kHz, v.c.o. output is fixed at 12 MHz and only the division ratio changes. For every 10 kHz increment the modulus is incremented by 1.

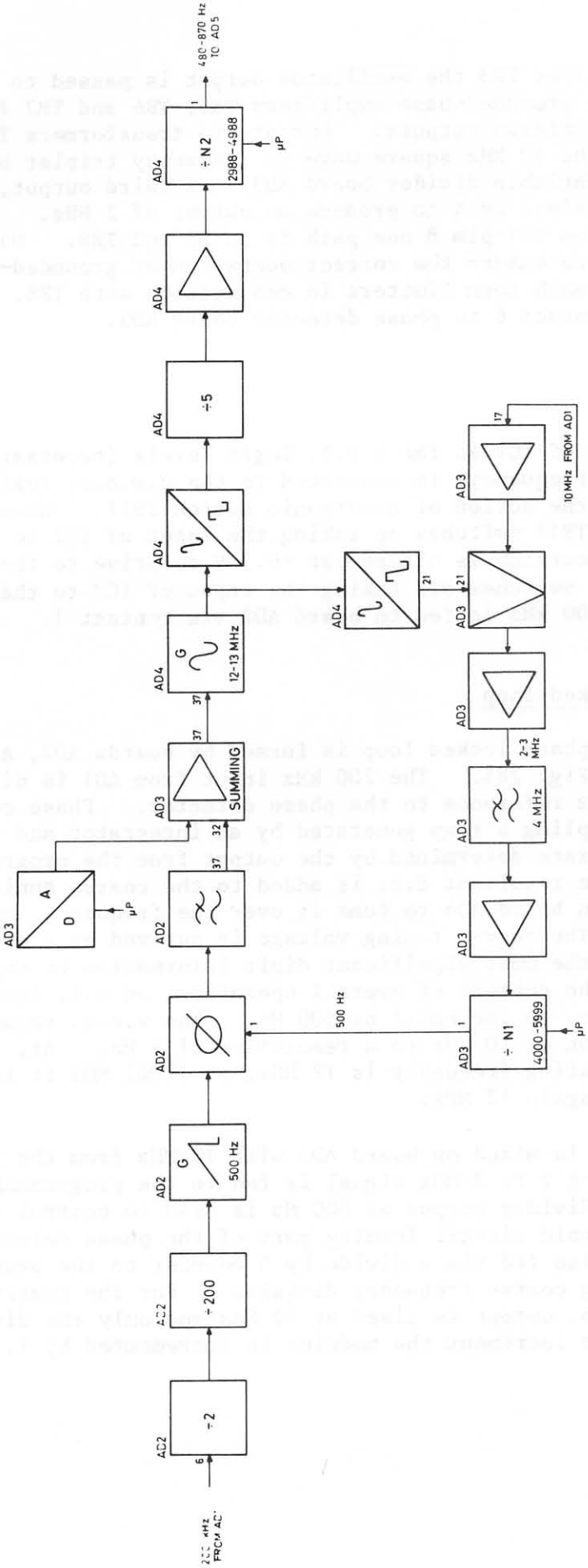


Fig. 28 First phase locked loop

Board AD2 - Interpolation phase detector

Circuit diagram : Chap. 7, Fig. 7

Dividers

103. The 200 kHz square wave input at contact 6 derived from the 10 MHz standard is divided by 2 by IC1a. This IC toggles because its J and K inputs are both connected to the positive rail. The resulting 100 kHz output is further divided by two by IC1b and the 50 kHz output is fed to the clock input of decade divider IC2. The CARRY output is fed to a second decade divider IC3. The resulting 500 Hz signal with a mark to space ratio of 1:9 is then used to control the ramp generator circuit based on IC4.

Ramp generator

104. The ramp generator forms part of the phase detector and comprises operational amplifier IC4 with switches TR3 and TR4. IC4, in conjunction with C8, forms an integrator. Under initial conditions with C8 discharged, the voltage at the output of the integrator is -5 V, both TR3 and TR4 are switched off and D4 prevents the bias reaching the base of TR4. By integrator action the voltage across C8 rises so that a ramp appears at the output of IC4. TR3 and hence TR4 are switched on for 0.2 ms every 2 ms by the 500 Hz output from IC3. When this happens, C8 is discharged through TR4 and the voltage at the output of IC4 is reset to -5 V.

Sample and hold circuit

105. The sample and hold circuit performs two functions, phase detector and loop filter. Phase detection is achieved by sampling the output from the ramp generator using pulses derived via the programmable N1 counter on board AD3. The sampled voltage is then shared between the two hold capacitors C11 and C13. The effective time constant of the filter is fixed by the ratio between the two capacitors and the sampling rate. The 500 Hz signal derived from the programmable counter is fed via contact 1 to emitter follower TR8. Three successive positive-going pulses are generated at the collectors of TR7, TR6 and TR5 with time constants controlled by C14, R25 (0.12 ms), C12, R22 (0.06 ms) and C10, R19 (0.12 ms). The first pulse from TR7 is fed to bilateral switch IC5a to sample the ramp from IC4 output, storing the voltage on C11. The second pulse from TR6 acts as a delay and the third pulse from TR5 is used to share the charge between C11 and C13. Ramp and sample waveforms are shown in Fig. 29. FET source follower TR9 passes the resulting voltage to contact 37 and the summing amplifier on AD3.

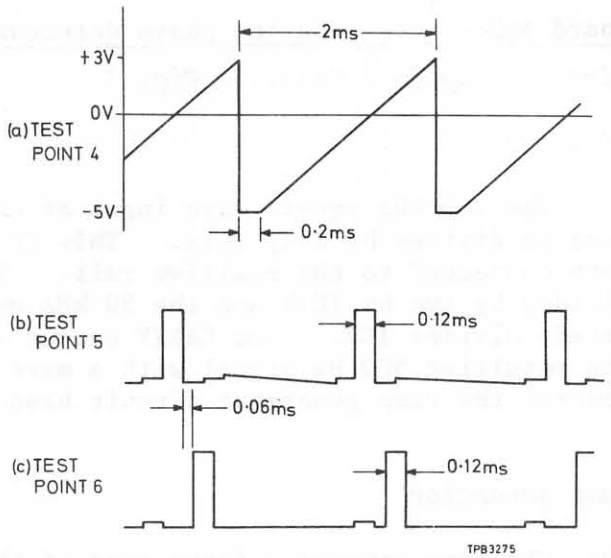


Fig. 29
Ramp generator waveforms

Board AD3 - Interpolation variable divider

Circuit diagram : Chap. 7, Fig. 7

Mixer

106. The input at contact 21 from the board AD4 v.c.o. at between 12 MHz and 12.9995 MHz is coupled to mixer IC3 by transformer T2. The second input to the mixer is from tuned amplifier TR1 whose input at contact 17 is provided by the 10 MHz frequency standard. The 2 to 3 MHz difference frequency resulting from the mixing process is selected by a 4 MHz low-pass filter after amplification by TR2. Triple NOR gate IC5 which follows functions as an amplifier with its bias point set by R22. Amplifier output at ±7.5 V provides the drive for the c.m.o.s. programmable divider IC4.

Variable ratio divider

107. IC4 is a divide by N (where N has a value between 4000 and 5999) programmable divider which provides the fine frequency (5 Hz) control of the v.c.o. on board AD4. Frequency division is described in detail under Circuit Summary at the beginning of this chapter. With the exception of J2, J3 and J4 which are hard-wired, the divider is programmed by b.c.d. presets on the jam inputs. BCD inputs from synthesizer latch board AD10 represent 10s of Hz on contacts B8 to B11, 100s of Hz on contacts B12 to B15 and 1000s of Hz on contacts B16 to B19. The high or low applied to contact B4 represents 5 Hz or 0 Hz respectively. The microprocessor sets the modulus via board AD10 so that for a 2 to 3 MHz input at pin 1 IC4 the output at pin 23 is at 500 Hz. Thus for a 2 MHz input to the divider the modulus is set to 4000 to produce a 500 Hz output.

108. Contacts B16 to B19 which carry the most significant digits of the divider setting also provide the source for the coarse frequency control of the v.c.o. on AD4. The b.c.d. data is passed to the inputs of quad latch IC1 which is enabled each time the 500 Hz output from IC4 goes positive. The inverting outputs are connected via binary weighted resistors to the inverting input (summing junction) of the adding amplifier IC2. Thus a '0' sends current into the summing junction and a '1' bleeds current from it. The total current into the junction depends on the b.c.d. number preset at the input. The '0'

level of the current is set by R27, the gain of the summing-amplifier is set by R26 and the proportion of error voltage from the phase detector (contact 32) by R25. As the coarse tuning voltage provided by the D/A converter is linear and the actual tuning law of the v.c.o. is curved, these three controls are set to provide the best compromise between settling time and loop stability.

D/A converter and adding amplifier

109. When the oscillator frequency is to be increased, the division ratio of IC4 is increased so that the output frequency from the variable divider decreases. However, as the most significant bit of the required frequency (kHz bit) is fed to the D/A converter, the control voltage to the v.c.o. is increased, increasing the frequency of oscillation of the v.c.o. and hence the output from the frequency divider. Thus coarse frequency tuning steps set the frequency of the v.c.o. near its correct value and help reduce the settling time for the p.l.l. Final tuning adjustment is made by the error voltage derived from the phase detector.

Board AD4 - Interpolation oscillator

Circuit diagram : Chap. 7, Fig. 7

Oscillator

110. The d.c. input signal from interpolation phase detector board AD3 is applied from contact 37 to varactor diode D1. Fig. 30 shows a graph of voltage against frequency. D1 controls the frequency of the voltage controlled oscillator comprising f.e.t. TR1, tapped coil T1 and capacitors C2 and C10. Oscillation amplitude is set by D2 and D5. From the oscillator the signal in the range 12 to 13 MHz is taken via emitter follower TR2 to TR3 and TR4. Both these transistors are grounded base buffer amplifiers which both form limiters in conjunction with TR2 to provide two signal outputs. One square wave output is taken via coupling transformer T2 and contact 21 to the mixer on board AD3. The other output is taken to divide by 5 IC1 to produce a signal between 2.4 and 2.6 MHz. This is fed to double NAND gate IC2 which functions as an amplifier with its bias point set by R17 and which provides a ±7.5 V clock input for c.m.o.s. variable ratio divider IC3.

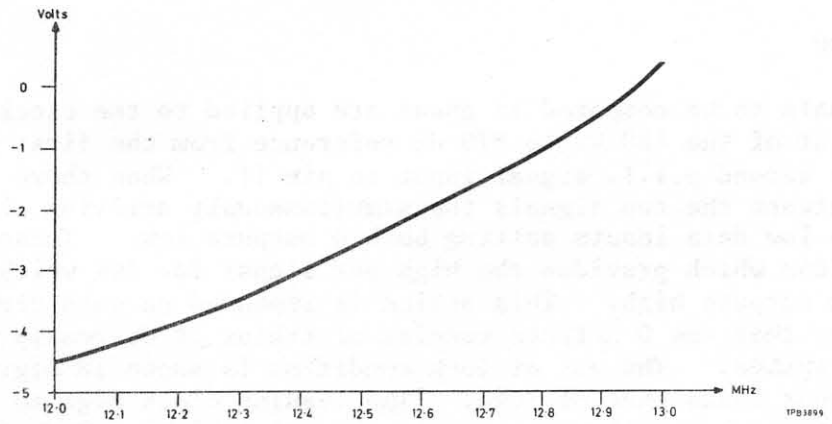


Fig. 30 VCO characteristic

Variable ratio divider

111. IC3 is a divide by N (where N is a value in the range 2988 to 4988) programmable divider which provides the reference for the phase detector on translation-phase detector board AD5. BCD inputs on contacts B4 to B18 from synthesizer latch board AD10 provide the division ratios (moduli). Inputs on contacts B4 to B7 represent 10s of kHz, those on B8 to B11 represent 100s of kHz, B12 to B15 indicate units of MHz while B16 to B18 represent 10s of MHz. The modulus is set by the microprocessor via board AD10 so that an input at pin 1 IC3 of between 2.4 and 2.6 MHz results in an output at pin 23 of between 480 and 870 Hz respectively. This means that for a local oscillator frequency of 50 MHz a modulus of 4988 is selected which converts the 2.4 MHz input to an output of 480 Hz. Divider output is taken to AD5 from contact 1.

Second phase locked loop

112. The signal from the first p.l.l. in the range 480 Hz to 870 Hz provides the reference for the second p.l.l. detector on board AD5 (see block diagram Fig. 31). Any difference in phase between the reference and the signal from board AD5 mixer results in pulses which are converted to d.c. error signals for adjustment of the frequency of the 10 MHz v.c.x.o. on board AD6. After division by 5 the signal at approximately 2 MHz is mixed with a 2 MHz input derived from the 10 MHz standard on board AD1. The difference frequency is further divided to provide the 480 Hz to 870 Hz signal input to the phase detector. The 10 MHz v.c.x.o. output is also divided on board AD6 to provide a nominal 10 kHz output to the third p.l.l.

113. The reference frequencies of 480 Hz and 870 Hz mentioned above result when the N1 and N2 presettable dividers are operating at their division ratio limits. Selecting 19.99 MHz sets the instrument to its maximum coarse frequency value and minimum fine frequency value. N1 and N2 are then at their limits of 4000 and 4987 respectively and board AD5 input is 480 Hz. With the instrument set to 9.995 kHz the maximum fine frequency and minimum coarse frequency values are selected. N1 and N2 are then set to 5999 and 4987 respectively and N2 output is at 870 Hz.

Board AD5 - Translation phase detector

Circuit diagram : Chap. 7, Fig. 8

Phase detector

114. The signals to be compared in phase are applied to the clock inputs to IC4 and consist of the 480 Hz to 870 Hz reference from the first p.l.l. to pin 3 and the second p.l.l. signal input to pin 11. When there is no phase difference between the two signals the simultaneously arriving clock pulses clock out the low data inputs setting both Q outputs low. These are passed to NOR gate IC5c which provides the high set signal for IC4 which immediately returns the Q outputs high. This action is repeated on each clock signal rising edge so that the Q outputs consist of trains of extremely narrow negative voltage spikes. The out of lock condition is shown in Fig. 32 where IC4b clock input leads that of IC4a. The leading clock edge to IC4b causes the Q output to go low while IC4a Q output remains high. When the later clock edge arrives IC4a Q output also goes low and this causes IC5c to set IC4 Q outputs back to their original high state. Successive clocking produces a train of negative pulses from IC4b with the width of the pulses being

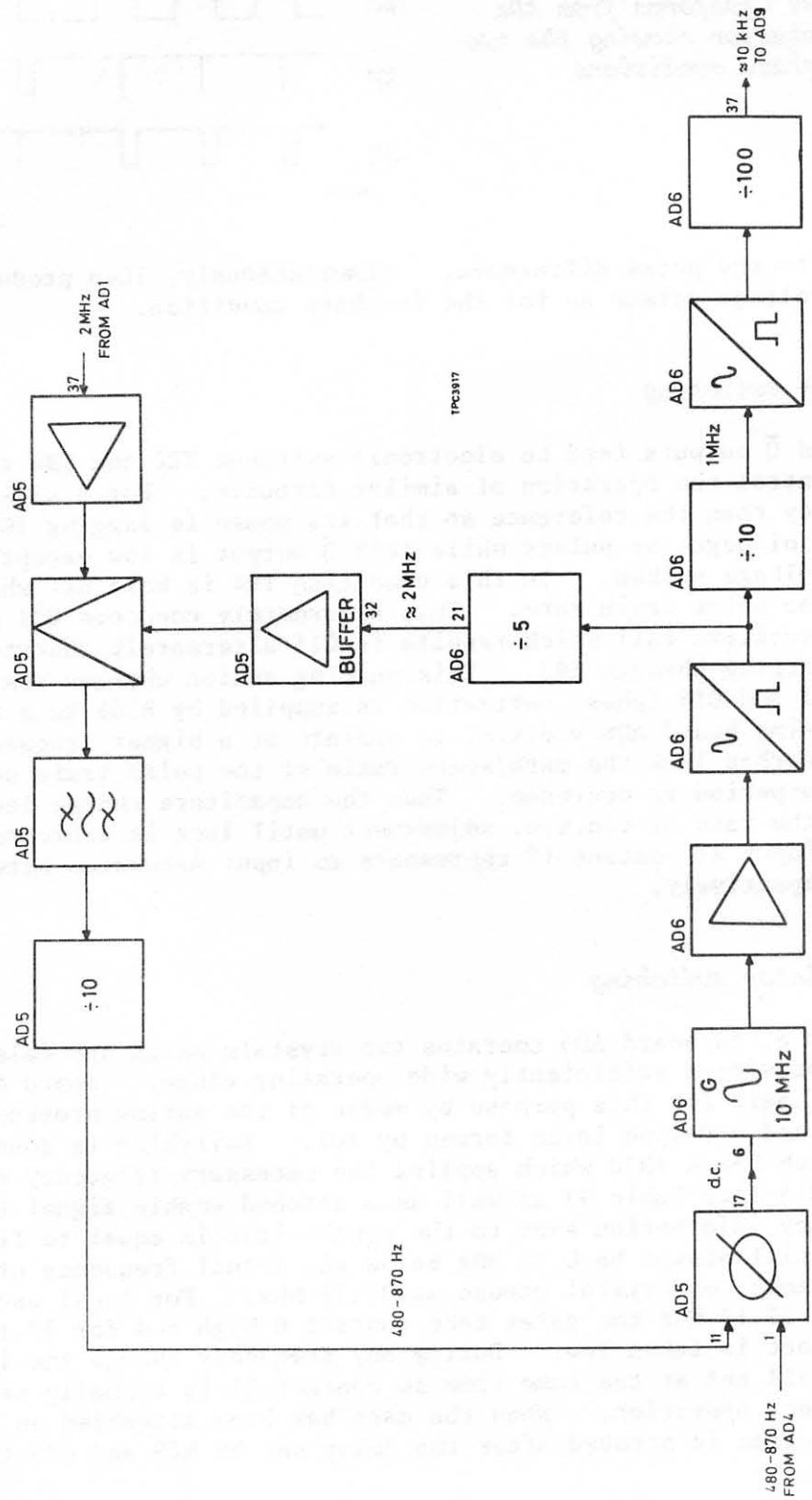


Fig. 31 Second phase locked loop

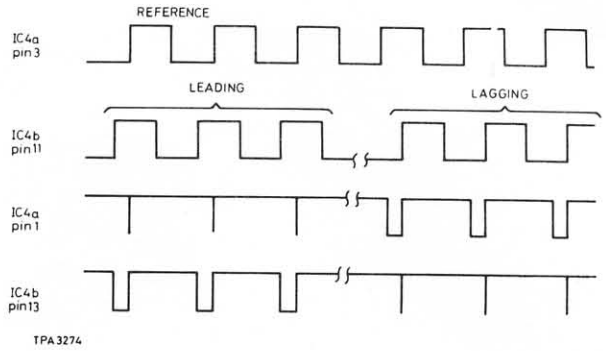


Fig. 32
Idealized waveforms from AD5 phase detector showing the two out of phase conditions

proprotional to the phase difference. Simultaneously, IC4a produces a train of negative voltage spikes as for the in-phase condition.

Phase detector switching

115. IC4 Q and $\overline{Q}$ outputs feed to electronic switches TR2 and TR4 respectively, which each control the operation of similar circuits. For a signal at a lower frequency than the reference so that its phase is lagging IC4a Q output emits a train of negative pulses while IC4b $\overline{Q}$ output is low except for the presence of voltage spikes. In this condition TR4 is held off while TR2 is switched at the pulse train rate. This alternately connects C11 negative plate to the positive rail which results in C11 alternately charging through D3 then discharging through TR3. This pumping action charges the loop filter capacitors C13 and C14 (phase correction is supplied by R20) to a higher d.c. potential causing board AD6 v.c.x.o. to operate at a higher frequency. As the loop approaches lock the mark/space ratio of the pulse train decreases causing TR2 on-period to decrease. Thus the capacitors charge less and less slowing down the rate of v.c.x.o. adjustment until lock is achieved. The -5 V to +2 V d.c. input at contact 17 represents an input excursion between 480 Hz and 870 Hz respectively.

Crystal oscillator switching

116. The v.c.x.o. on board AD6 contains two crystals which are selected as necessary to provide a sufficiently wide operating range. Board AD5 supplies the switching logic for this purpose by means of the gating provided by IC6, IC5a and IC5b and a D-type latch formed by IC7. Switching is controlled from sythesizer latch board AD10 which applies the necessary frequency data to contacts B11 to B16 (see Table 9) as well as a strobed enable signal to contact 21. As the frequency information sent to the synthesizer is equal to frequency +29.88 MHz it will always be 0.12 MHz below the actual frequency of oscillation. Thus the changeover of crystal occurs at 37.12 MHz. For local oscillator frequencies below 37.12 MHz the gates take contact 6 high and for 37.12 MHz and above the contact is taken low. During any frequency change the input logic lines are not all set at the same time so contact 21 is normally held low to prevent incorrect operation. When the data has been assembled on the input lines the selection is strobed after the delay set by R29 and C23 to allow the data to settle.

TABLE 9 AD5 VCXO SWITCHING LOGIC

Frequency (MHz)	*B11*	*B16*	*B15*	*B14*	*B13*	*B12*	*Detecting gate*
37	L	H	L	H	H	H	IC6a
38	L	H	H	L	L	L	IC6b
39	L	H	H	L	L	H	IC6b
40	H	L	L	L	L	L	IC5b

H = +7.5 V; L = -7.5 V

Mixer

117. A 2 MHz input derived from the frequency standard is applied to contact 37 and taken via tuned buffer amplifier TR1 to mixer IC1. The second input to the mixer from buffer TR6 is derived from board AD6 v.c.o. This signal is a square wave at between 2,004,800 Hz and 2,008,700 Hz. The 4800 Hz to 8700 Hz difference frequency is selected by low-pass filter IC2 and associated components and fed to divider IC3. After division by 10 the 480 Hz to 870 Hz output is fed to the board phase detector.

Board AD6 - Translation oscillator

Circuit diagram : Chap. 7, Fig. 8

Crystal oscillator

118. For frequency adjustment of the voltage controlled crystal oscillator the d.c. input from AD5 phase detector at contact 6 is fed to varactor diodes D6 to D9. These control the frequencies of the two crystals which are necessary to provide a wide operating range. Selection of either XL1 or XL2 is by board AD5 logic to contact 9. A high to contact 9 switches TR7 on taking the junction of R22 and R30 low. This switches TR6 off by taking its base and emitter to the same potential while also forward biasing diode D5. The low impedance path now formed from TR2 emitter via D5 and XL1 to TR1 activates the crystal which now provides the v.c.x.o. higher frequency range. As TR6 is switched off, D4 is reverse biased through R21 and R29. This effectively disconnects XL2. To select XL2, contact 9 is taken low which forward biases D4 and this crystal is brought into operation instead of XL1. Oscillator voltage control and crystal selection is shown in Fig. 33. Output from either crystal is fed to tuned amplifier TR1 which with TR2 completes the long-tailed pair oscillator.

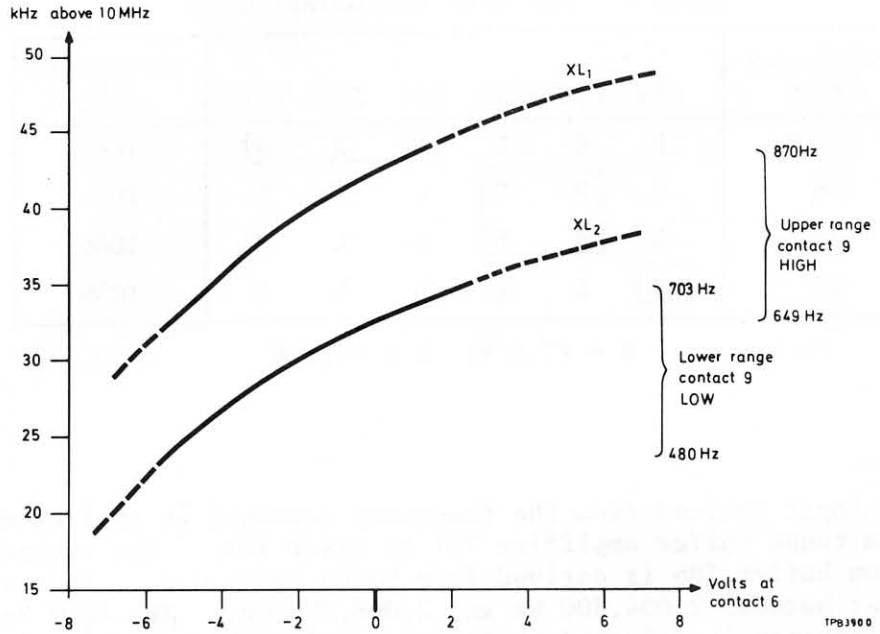


Fig. 33 Board AD6 voltage controlled crystal oscillator showing switched ranges of operation

Dividers

119. TR2 output is passed to amplifier TR3 whose collector is tuned by L2 and C7. The sine wave output from the amplifier is converted to a square wave by TR4 and used to clock the divider which follows. IC1 has dual division ratios of 5 and 10. IC1 divides by 5 to produce an output in the range 2,004,800 to 2,008,700 Hz and this supplies the carrier for the mixer on board AD5. To supply an output to board AD9 and the third phase locked loop IC1 also divides by 10. The output in the range 1,002,400 to 1,004,350 Hz is converted from t.t.l. to c.m.o.s. logic levels by TR5 and fed to decade dividers IC2 and IC3. Divider output at a nominal 10 kHz is fed out at contact 37.

Third phase locked loop

120. From the second p.l.l. the signal at approximately 10 kHz provides the reference for the second p.l.l. detector on board AD9. When a change in frequency is detected an out of lock signal is passed via board AD10 to the microprocessor and a d.c. error signal adjusts the frequency of the 30 to 50 MHz v.c.o. on board AD8 (see Fig. 34). One output from AD8 is mixed with 30 MHz on board AA1 to supply the sender output of up to 20 MHz. A second output is looped back via dividers on board AD7 which convert the signal to approximately 10 kHz for the phase detector.

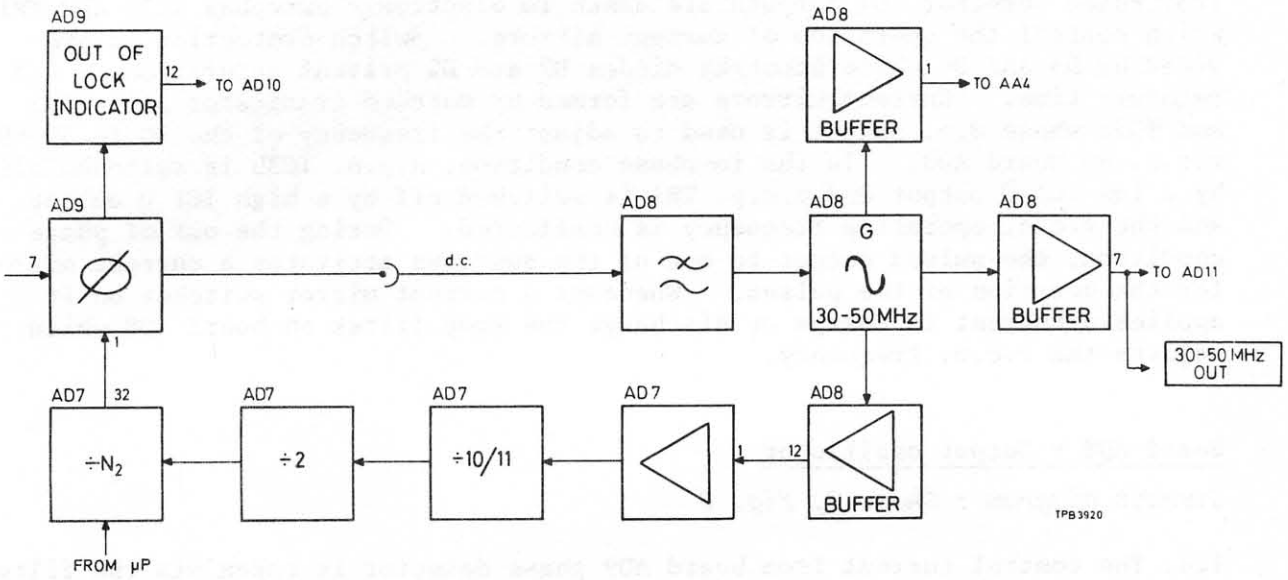


Fig. 34 Third phase locked loop

Board AD9 - Output phase detector

Circuit diagram : Chap. 7, Fig. 9

Phase detector

121. The signals to be compared in phase are applied to the clock inputs of IC1 and consist of a nominal 10 kHz reference from the second p.l.l. to pin 7 and a nominal 10 kHz signal from variable divider board AD7 to pin 1. When there is no phase difference between the two signals the simultaneously arriving clock pulses clock out the low data inputs taking both Q outputs low. This causes NOR gate IC2a to provide the high set signal for IC1 and both Q outputs immediately return high. This action is repeated on each clock signal rising edge so that the Q outputs consist of trains of extremely narrow negative voltage spikes (the spikes are subsequently filtered out). The out of lock condition where IC1b clock input leads that of IC1a is next considered. The leading clock edge to IC1b causes the Q output to go low while IC1a Q output remains high. When the later clock edge arrives, IC1a output also goes low and this causes IC2a to set IC1 Q outputs back to their original high state. Successive clocking produces a train of negative pulses from IC1b with the width of the pulse being proportional to the phase difference. Simultaneously, IC1a produces a train of negative voltage spikes as for the in-phase condition.

Out of lock indicator

122. An out of lock indication to the microprocessor is provided by the circuit formed by ICs 2b and 2c with D1 and C3. Phase detector IC1 $\overline{Q}$ outputs provide the two inputs to NOR gate IC2b. When an in-phase condition exists, both inputs are low, except for positive voltage spikes whose effect is absorbed by C3. Inversion by IC2c results in a low in-lock signal being passsed to the microprocessor from contact 12. For an out of phase condition, positive pulses from phase detector IC1 set IC2b output low which forward biases D1 and enables C3 to discharge. The resulting low is inverted by IC2c to form a high out of lock signal to the microprocessor.

Current mirrors

123. Phase detector IC1 outputs are taken to electronic switches IC3b and TR1 which control the operation of current mirrors. Switch protection is provided by D3 and D4 while Schottky diodes D2 and D5 prevent saturation to and recovery time. Current mirrors are formed by matched transistor pairs TR2 and IC3a whose d.c. output is used to adjust the frequency of the 30 to 50 MHz v.c.o. on board AD8. In the in-phase condition, n.p.n. IC3b is switched off by a low IC1 $\overline{Q}$ output and p.n.p. TR1 is switched off by a high IC1 Q output and the v.c.o. operating frequency is unaffected. During the out of phase condition, the pulsed output to one of the switches activates a current mirror for the duration of the pulses. Whenever a current mirror switches on it applies a current to charge or discharge the loop filter on board AD8 which adjusts the v.c.o. frequency.

Board AD8 - Output oscillator

Circuit diagram : Chap. 7, Fig. 9

124. The control current from board AD9 phase detector is taken via the filter formed by C3, C10 and R1 to the 30 to 50 MHz voltage controlled oscillator. The v.c.o. comprises varactor diodes D1 to D8, tunable inductor L1 and low noise f.e.t. TR1. Oscillation amplitude is limited by diodes D9 and D10. Emitter-follower TR2 feeds into three output buffer amplifiers TR3, TR4 and TR5. These grounded base transistors form limiters in conjunction with TR2 and the resulting square wave outputs are coupled out by transformers T1 to T3.

Board AD7 - Output variable divider

Circuit diagram : Chap. 7, Fig. 9

General

125. The purpose of board AD7 is to divide the 30 to 50 MHz variable frequency input from the v.c.o. on board AD8 in order to obtain a fixed 10 kHz output for the third phase locked loop. To do this, the division ratios must be variable so as to produce a constant frequency output as the local oscillator is tuned during normal operation. This is achieved by divider circuits which include a prescaler whose division ratios (moduli) are selected by presettable counters. For ease of explanation these counters may be considered to be grouped into A counters for controlling division by the upper modulus of 21 and B counters for controlling division by the lower modulus of 20. In operation, both groups of counters are preset and then start counting down with the prescaler dividing by 21. When the A counters, which are loaded with the least significant digits, finish counting they cause the prescaler to change to division by 20 and the B counters, loaded with the most significant digits, continue the count. Both groups reset at the end of the count and the sequence restarts.

Division

126. Apart from the prescaler, the method of division is similar to that for a normal decade counter of the form :

$$N = B1 + 10B2 + 100B3 + 1000B4$$

where N is the overall division ratio, B1 is the number of units, B2 is the number of tens etc.

Board AD7 counters are, however, grouped into A and B counters and additionally the least significant tens input is 'borrowed' from the B counters and included in the A counters (see Fig. 35). Because of these modifications the above simple expression changes to :

$$N = A1 + 10A2 + B1 + 5B2 + 50B3$$

Initially, division is at the prescaler upper modulus of 21 and the A and B counters are clocked by the number loaded into the A counters i.e. the A counters decrement to zero after 21 A pulses. The count now remaining in the B counters when the A counters have reached zero is B-A so that the number of further pulses for the B counters to reach zero is 20 (B-A) pulses. Thus the total count for a complete countdown is 21A + 20 (B-A) and the complete expression for the counter becomes :

$$N = 21\ (A1 + 10A2) + 20\ [B1 + 5B2 + 50B3 - (A1 + 10A2)]$$

where N is the overall division ratio and the variables are the counter presets.

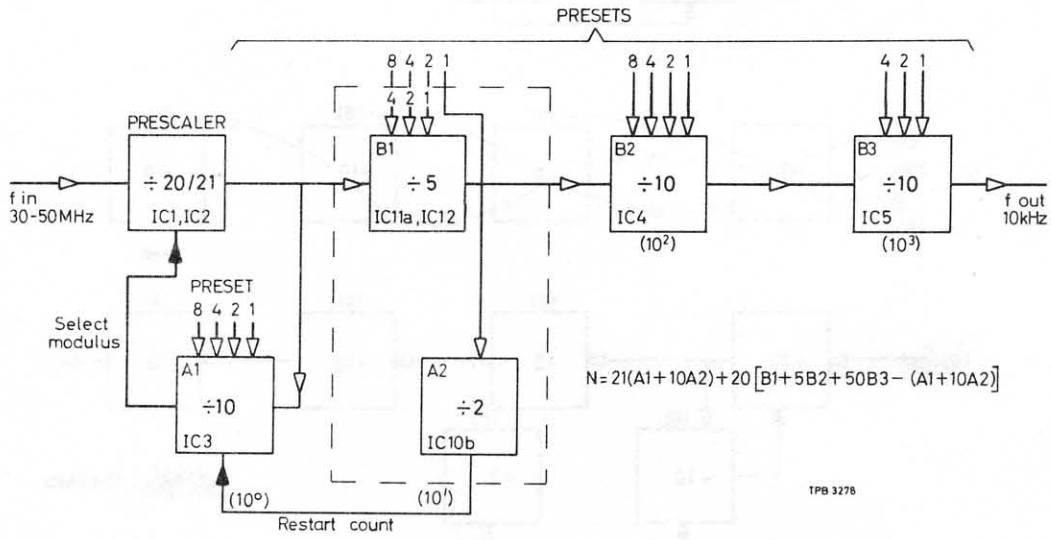


Fig. 35 Method of division using dual modulus prescaling. The expression is for the overall division ratio.

Division example

127. In the example shown in Fig. 36 the instrument is set to 280 kHz and the 30 MHz higher local oscillator frequency of 30.28 MHz is fed as the clock input to the prescaler and following counters for conversion to a nominal 10 kHz output. Before countdown commences, the counters are preset to an N2 division ratio (see Introduction) in the range 2988 to 4988. This preset represents an initial value of 2988 plus the number of 10 kHz multiples in the instrument setting. For a frequency of 100 Hz the preset would thus be 2988. In the example where the instrument frequency is 280 kHz the preset is 3016 i.e. 2988 + 28. The counters are preset as follows : B3 = 3, B2 = 0, B1 = 0, A2 = 1 and A1 = 6 (see Fig. 36a). Note here that the least significant of the B1 counter inputs is 'borrowed' to provide the A2 preset as previously explained (see Fig. 35). For example, for a preset of 3046 the presets would be B3 = 3, B2 = 0, B1 = 2, A2 = 0 and A1 = 6.

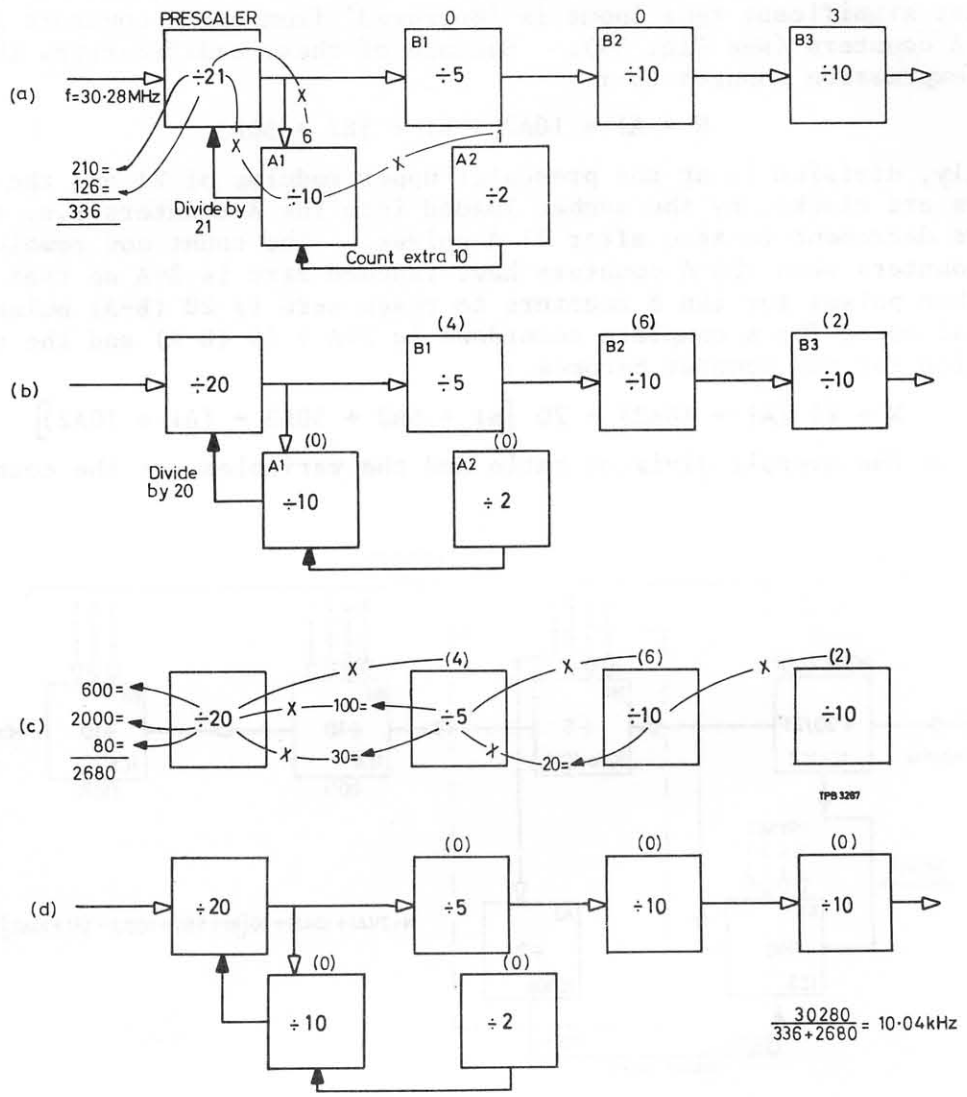


Fig. 36 Example of frequency division using dual modulus prescaling showing conversion of 30.28 MHz input to nominal 10 kHz output

128. Countdown commences with the prescaler dividing by 21 and both A and B counters counting down the number preset on the A counters. In the example the A counters are preset to 16. A1 counts down to zero and since A2 is preset to 1 it causes A1 to count down a further 10 pulses from the prescaler. The A counters thus reach zero after 21 x 16 = 336 prescaler input pulses (Fig. 36a). Meanwhile the B counters have also counted down their preset by 16. Since these counters consist of two decade counters and a divide by five counter the first pulse from the prescaler counts down B3 from 3 to 2, B2 from 0 to 9, and B1 from 0 to 4. After the sixteenth pulse, when the A counters have finished counting B3 = 2, B2 = 6 and B1 = 4 as shown in Fig. 36(b). The modulus is now changed to 20 due to the A counters having completed their count and the B counters continue counting down alone. After a further 2680 pulses (see Fig. 36c) the countdown sequence is completed and a new sequence starts. Output frequency is now at the required nominal 10 kHz, i.e. 30.28 MHz ÷ (2680 + 336) = 10.04 kHz as shown in Fig. 36(d).

Overall operation

129. Transformer T1 couples the 30 to 50 MHz input to current feedback pair amplifier TR1 and TR2 whose output clocks presettable divider IC1. This divider forms the first part of a prescaler whose division ratios are selected according to the logic states on pins 2 and 3 of IC1. When either of these pins is set high, IC1 divides by 10 and when both are low division is by 11. The second part of the prescaler is formed by IC2 which divides by 2 to provide the overall prescaler division ratios of 20 and 21. Modulus selection is by IC10a Q output to pin 2 IC1. To select division by 20, pin 2 of IC1 is held high so that IC1 divides by 10 while IC2 is dividing by 2. To select the modulus of 21, IC10a holds pin 2 low. The effect of this is to cause IC1 to divide by 11 when the logic states of pins 2 and 3 are coincident low every other clock pulse, and to divide by 10 when pin 3 goes high. Under these conditions prescaler division is by 21 as shown in Fig. 37.

130. Prescaler output is fed to the upper modulus counter via amplifier IC6a and inverter IC6b. This counter is formed by presettable divider IC3 (counter A1) and D-type bistable IC10b (counter A2). Presets are applied from contacts B4 to B7 which carry the 10 kHz units inputs, and from contact B8 which carries the 'borrowed' least significant 100 kHz input. Signals A and B from IC11b control overall counter operation.

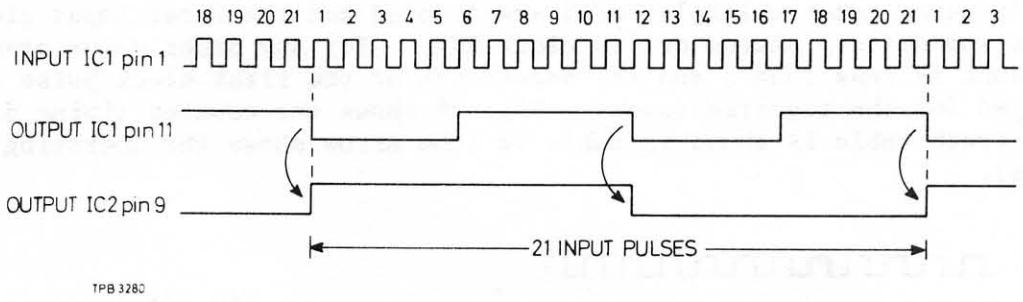


Fig. 37 Prescaler division by upper modulus of 21 when pin 2 IC1 held low

131. Prescaler output is also fed to the lower modulus counters. IC6b output is taken via the remaining gates of IC6 to the divide by five counter (counter B1) formed by D-type bistables IC11a, IC12a and IC12b. This counter is loaded by a system of gates from contacts B9 to B11 which carry the remaining 100 kHz inputs. These gates load the counter by controlling the set function of IC11a and the reset functions of ICs 12a and 12b. IC12b $\overline{Q}$ output is used to clock the most significant counters formed by presettable dividers IC4 (counter B2) and IC5 (counter B3). IC4 is preset by contacts B12 to B15 which carry the MHz inputs while IC5 is loaded from contacts B16 to B18 which carry the 10 MHz inputs.

Counting sequence

132. Towards the end of a counting sequence (during division by 20) IC12b Q output as well as IC4 pin 12 both go high signifying count completed. These signals cause NAND gate IC9d to set the data input low to bistable IC11b which controls the overall counter operation by means of output signals A and B. Counting continues and after 20 input pulses IC11b is clocked setting signal A high. This signal sets IC10a output to the prescaler high so that division

by 20 continues, as well as enabling all counters to preset to the b.c.d. inputs. The loading operation causes IC4 to take pin 12 low causing IC11b data input to go high. This is clocked out after a further 20 input pulses so that signal A is set low and signal B, in its turn, is set high. The B signal disables the preset inputs to the gates now that the counters have loaded, as well as removing the set input to modulus selector IC10a. This allows the first clock pulse of the new sequence to IC10a to clock out the logic level on its data input to recommence the counting sequence. If the upper modulus counters are loaded, IC10a data input will be low and this is clocked out to select division by 21. If however, these counters are preset to zero, IC10a data input is high so that initial division by 21 is omitted and the counters commence division by 20. Note from the preceding description that counting continues after the count completed signal has been received; this is due to the division method used by the divide by five counter.

Divide by five operation

133. When signal B from IC11b is set low it enables the b.c.d. inputs to preset the divide by five counter. Signal A at this time is high to NOR gate IC6c which prevents the counters from being clocked while also allowing the remaining counters to load and count down. The clock input from IC6b to the control bistable IC11b is not inhibited and when the count completed signal from IC4 pin 12 is received signal B is set high. This disables the divide by five presets while also enabling counter operation. If the counter is preset to zero, exact multiples of 5 are counted and the first input clock pulse is immediately passed out to clock IC4. For any other value preset the first count is less than 5 and the occurrence of the first clock pulse to IC4 is delayed for the required count. Fig. 38 shows the counter timing diagram and the truth table is shown in Table 10 (the arrow shows the operating sequence).

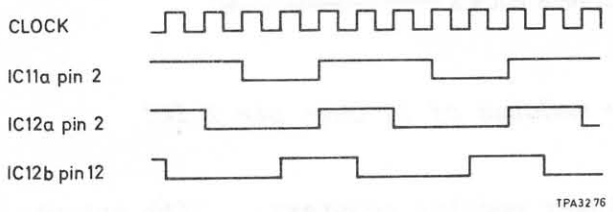


Fig. 38
Divide by 5 timing diagram

TABLE 10 DIVIDE BY 5 TRUTH TABLE

BCD inputs			*Set*	*Reset*		*$\overline{Q}$ outputs*		
B9	*B10*	*B11*	*IC11a*	*IC12a*	*IC12b*	*IC11a*	*IC12a*	*IC12b*
L	L	H	H	L	H	L	L	H
H	H	L	L	H	H	H	H	H
L	H	L	L	H	L	H	H	L
H	L	L	L	L	L	H	L	L
L	L	L	H	L	L	L	L	L

H = +7.5 V; L = -7.5 V

(arrow shows sequence)

Upper modulus counter operation

134. The operation of these counters is shown by the example in Fig. 39 in which the upper modulus counters are preset to 15. At (a) the counters have finished the previous sequence so that IC3 pin 12 is high and IC10b Q output is low to indicate count complete. This causes NOR gate IC7d to take IC10a data input high and this is clocked out to select prescaler division by 20 and the lower modulus counters continue counting down. At (b) these counters have finished their count so that signal A is high and signal B is low. These signals enable the upper modulus counters to commence operation. With signal A high, IC3 (counter A1) is preset to 5 and with signal B low IC10b (counter A2) is effectively preset to 10. When IC3 loads, the count complete signal on pin 12 goes low and clocks out the high on IC10b data input. This causes IC7d to remove IC3 inhibit while also selecting the upper modulus of 21 when clocked out from IC10a. Counting can now commence. At (c) counting is taking place so that signal B is high which inhibits IC10b reset from affecting

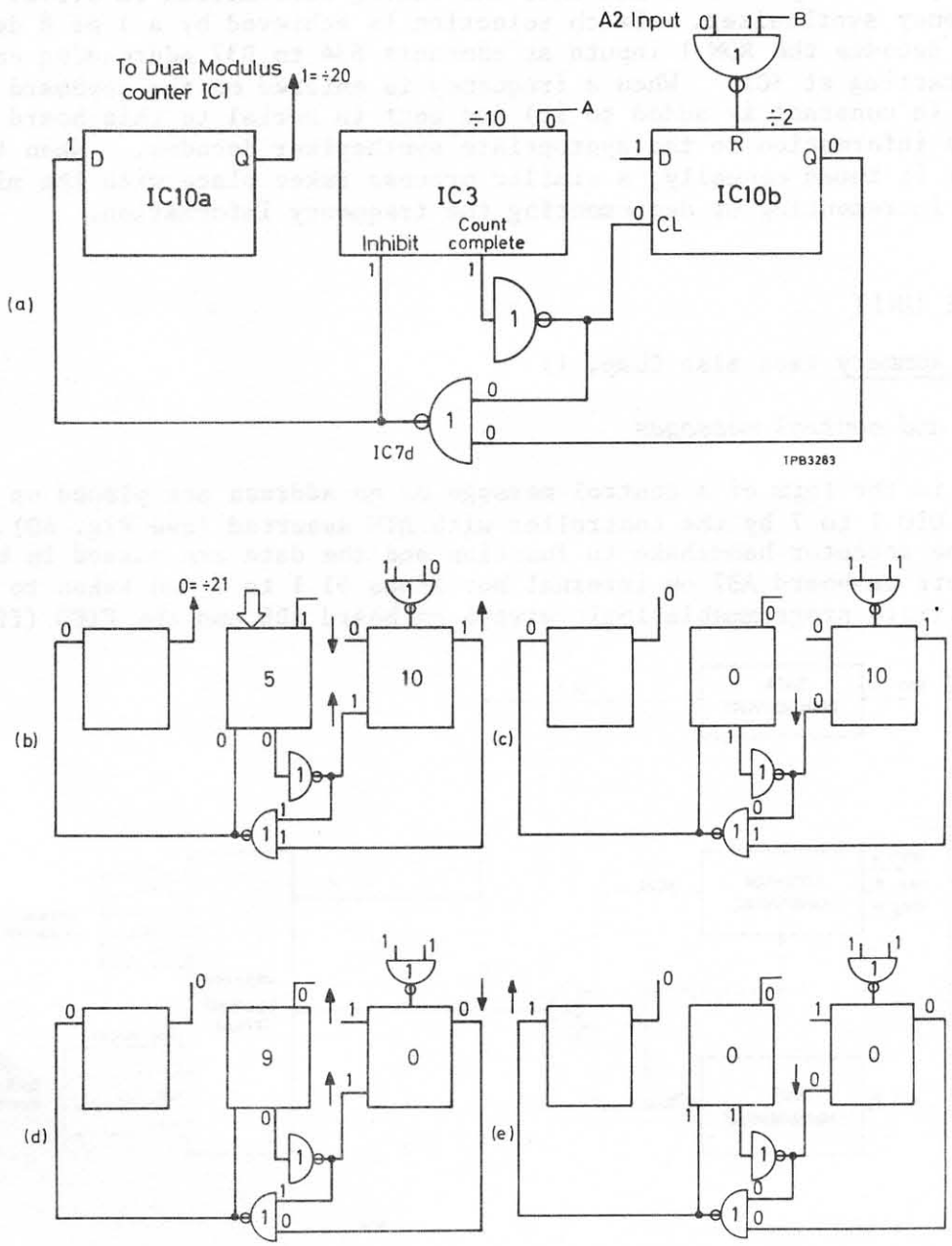


Fig. 39 Example of upper modulus counter operation showing count of 15

further operation. IC3 has counted down to zero and pin 12 goes high to indicate count complete. However, this signal is prevented from inhibiting IC3 by the high Q output from IC10b to IC7d. As shown in (d) decade counter IC3 now recommences counting down, this time from 10. This causes the count complete signal to go low which clocks out the low on IC10b data input. The end of the upper modulus count is shown in (e) where IC3 count complete signal sets IC10a data input high. This will be passed out by the next clock pulse to select division by 20 for the remainder of the counting sequence.

Board AD10 - Synthesizer latch

Circuit diagram : Chap. 7, Fig. 10

Synthesizer outputs

135. RAM 0 inputs to contacts 34 to 37 provide the data input to D-type latches IC1 to IC8, the outputs of which feed the tuning information in b.c.d. form to the frequency synthesizer. Latch selection is achieved by a 1 of 8 decoder IC9 which decodes the ROM 1 inputs at contacts B34 to B37 addressing each latch in turn starting at IC1. When a frequency is entered on the keyboard it is processed (a constant is added to it) and sent in serial to this board which routes the information to the appropriate synthesizer decades. When the instrument is tuned manually, a similar process takes place with the microprocessor incrementing or decrementing the frequency information.

INTERFACE UNIT

Operation summary (see also Chap. 1)

Addresses and control messages

136. Data in the form of a control message or an address are placed on data bus lines DIO 1 to 7 by the controller with ATN asserted (see Fig. 40). ATN enables the acceptor handshake to function and the data are passed in by the transceivers on board AB7 on internal bus lines DI 1 to 7 and taken to both the FPLA (field programmable logic array) on board AB6 and the FIFO (first-in,

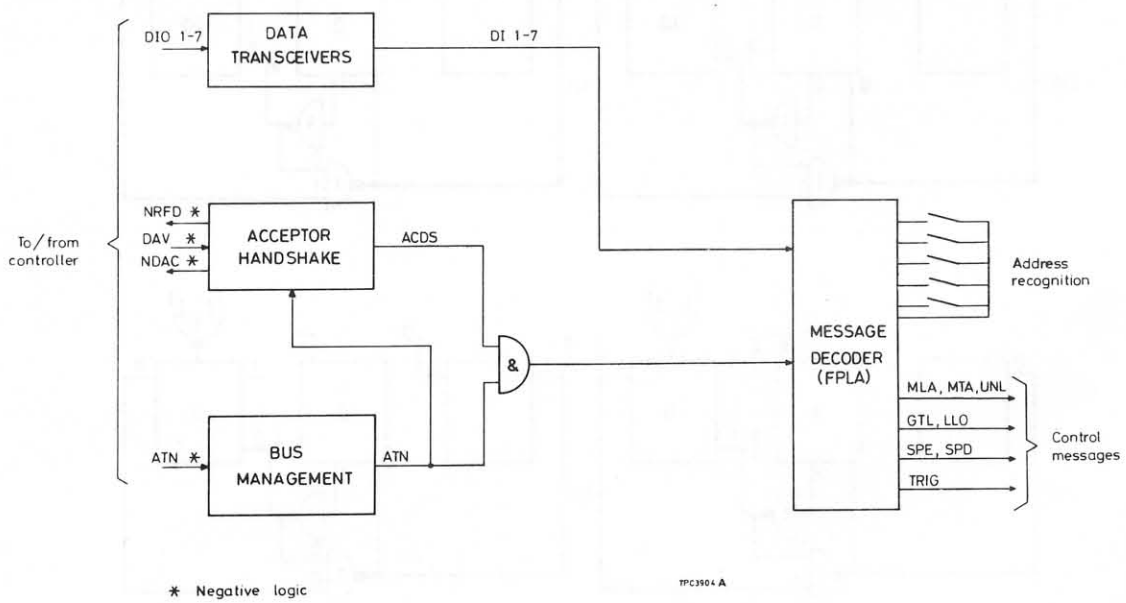


Fig. 40 Address and control message acceptance summary

first-out memory) on board AB5. Since ATN is asserted with the data, the interface is prevented from entering either LACS or TACS (see message references in Table 11). LACS unasserted prevents the 'shift-in' signal from enabling the FIFO so that it ignores the data on the bus. And with TACS simultaneously unasserted, the send transceivers are disabled so that any data latched onto the internal DO 1 to 7 lines are prevented from being passed out onto the data bus.

TABLE 11 INTERFACE MESSAGES MENTIONED IN THE TEXT

Remote messages	*Local messages*
ATN = attention	lon = listen only
DAV = data valid	nba = new byte available
EOI = end or identify	pon = power on
GET = group execute trigger	rdy = ready
GTL = go to local	rsv = request service
IFC = interface clear	rtl = return to local
LLO = local lockout	ton = talk only
MLA = my listen address	*Some interface states*
MTA = my talk address	
NDAC = data not accepted	ACDS = accept data state
NRFD = not ready for data	AIDS = acceptor idle state
OTA = other talk address	ACRS = acceptor ready state
REN = remote enable	LACS = listener active state
RFD = ready for data	LADS = listener addressed state
SPD = serial poll disable	LOCS = local state
SPE = serial poll enable	REMS = remote state
SRQ = service request	TACS = talker active state
UNL = unlisten	SPAS = serial poll active state
UNT = untalk	SPMS = serial poll mode state

137. The data sent with ATN asserted are thus fed into the FPLA for action. Control messages are decoded and the functions are carried out. The data on the bus are also compared with data from the rear panel address switches. If the instrument's address is recognized and certain other conditions are met, either MLA or MTA results depending upon whether DI lines 6 and 7 designate the instrument a listener or a talker.

Talker function summary

138. The talker function is summarized in Fig. 41 which shows the operation of the interface immediately following the address phase. Recognition of the instrument's talk address by the FPLA results in MTA which causes TADS to be latched out. When ATN is removed with the address it causes both the acceptor handshake and the FIFO to be disabled since these are not required for the talk operation. TADS is gated to assert TACS which enables the send transceivers. When ready to transfer data, the processor places the data byte on the data bus

with nba asserted to show that the data are valid. The data are then transferred to the listeners by means of the source handshake process.

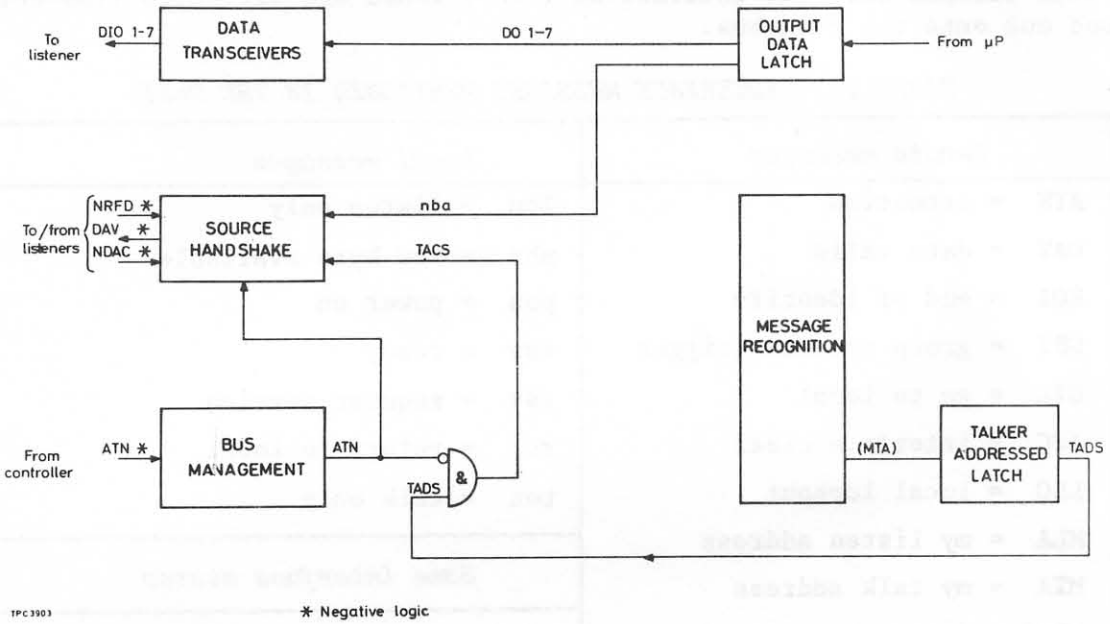


Fig. 41 Talker summary

Listener function summary

139. The listener function is summarized in Fig. 42.

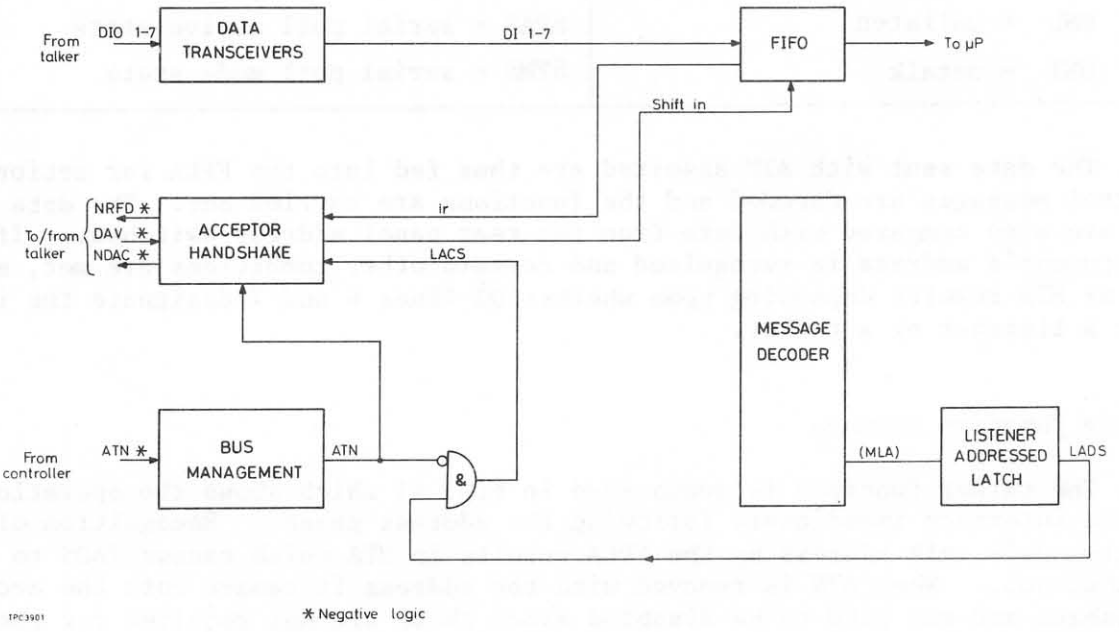


Fig. 42 Listener summary

The instrument responds to being addressed as a listener by the FPLA asserting MLA which causes LADS to be latched out. When the controller removes ATN with the address, LACS and $\overline{\text{TACS}}$ are gated out. $\overline{\text{TACS}}$ disables both the source handshake and the send transceivers since these are not required for the listen operation. LACS is gated with ir and this removes NRFD to indicate the interface's readiness to receive data. This happens when DAV is received from the talker during the handshake when the data is transferred. LACS is also gated with ACDS to set 'shift in' high to enable the FIFO to load the incoming data byte.

Board AB5 - Input buffers

Circuit diagram : Chap. 7, Fig. 16

Data input control

140. Most of the operations performed by the interface board including data input and output are controlled by b.c.d. to decimal decoder IC7. When the interface accepts data it is fed to the FIFO formed by ICs 1 and 2 and then passed out to the microprocessor in two 4-bit words. Decoder decimal 1 output going high enables the A inputs to AND/OR select gate IC5 to be passed out to the B inputs of a second AND/OR select gate IC6. The A inputs to IC5 are supplied by IC2, and these consist of the upper data bits plus the FIFO 'output ready' signal. The same activating signal at input contact B16 that selected the decimal 1 output is used to pass the B inputs to IC6 out to the microprocessor via the internal data bus from contacts B24 to B27. When in its turn decoder decimal 2 output goes high, the A inputs to IC6 are enabled and the second 4-bits of the data word are passed out to the microprocessor. The next data word may now be presented at the FIFO outputs and this is done when decimal 4 output goes high. This provides the FIFO 'shift out' signal which allows the old data to be replaced by new.

Data output control

141. Data is transferred out by D-type latches IC8 and IC9 when clocked by decoder IC7. The same decimal 1 and 2 outputs used to pass data in are used to sequentially latch data out in two 4-bit words from the microprocessor. Included with the upper data bits is nba which triggers the source handshake.

Control functions

142. This board is common to both the receiver TF 2357 as well as the sender and since the sender has a limited control capability provision is made on this board for asserting ATN, IFC, REN etc. The receiver, which has no control capability, does not send these signals.

Board AB6 - Decoder

Circuit diagram : Chap. 7, Fig. 16

Address selection

143. Address recognition is carried out by field programmable logic array IC1. During the address phase, the address placed on the data lines is passed into FPLA IC1 from contacts 24 to 28 for internal comparison with the address set on contacts 33 to 37. The address for these contacts is set on the instrument rear panel ADDRESS switches. At the same time the logic on input contacts 21 and 22 determines whether the instrument is being addressed as a talker or a listener. If the addresses are compatible, the outputs from decimal decoder IC2 assert either MLA by the decimal 6 output or MTA by the decimal 7 output. MLA or MTA going high provides the data input to either pin 9 or pin 5 respectively of dual D-type bistable IC3. The clock input for IC3 is provided via AND gate IC11 by the F6 IC1 output (high when the instrument is addressed) and the MLA/MTA STROBE input from contact B16.

144. When dual bistable IC3 is clocked during the address phase with either MTA or MLA set high on its data inputs, the resulting $\overline{Q}$ outputs assert $\overline{\text{TADS}}$ or $\overline{\text{LADS}}$. $\overline{\text{LADS}}$ is passed to provide the I14 input to FPLA IC1 while $\overline{\text{TADS}}$ is ANDed with ATN to provide the TACS output at contact B10. The I14 input is necessary for GET, GTL and SDC since for these signals the instrument must be in the listener addressed state. IC3 $\overline{\text{TADS}}$ output is enabled by the set signal ton and disabled by the reset signals OTA and UNT via OR gate IC10a. Similarly, IC3 $\overline{\text{LADS}}$ output is enabled by lon and disabled by UNL via OR gate IC10b. Both $\overline{\text{TADS}}$ and $\overline{\text{LADS}}$ are disabled by power on (initally) and by interface clear signals to the two OR gates.

Service request and serial polling

145. When the attention of the controller is required, i.e. when faulty information is received, the microprocessor originates a request service (rsv) message which is passed via board AB5 to contact B8. The high rsv signal is applied to the bistable formed by IC7a and IC4d and sets the service request SRQ output high to contact 8. This is passed to board AB7 which asserts SRQ to the controller by means of the interface management bus (see timing diag. Fig. 43). Having received SRQ the controller uses serial polling to find out the source of the request - necessary since all devices use the same SRQ line. The SPE (serial poll enable) message is sent, all devices are unlistened and then sequentially addressed to talk. When the interface receives the SPE message decoder IC2 decimal output 4 goes high to assert SPE. SPE sets the bistable formed by the cross-coupled NOR gates IC4b and IC4c which sets SPMS high. During SPMS the microprocessor prepares the status byte.

146. When addressed as a talker, the interface enters SPAS via NOR gates IC7c and IC4d which resets the bistable to remove SRQ. During this period the microprocessor sends the status byte with bit 7 indicating that the sender is the instrument requesting service. The contents of the remainder of the byte indicate the reason for requesting service. The interface exits SPAS when either OTA or UNT is received from the controller. The serial poll disable SPD signal from IC2 decimal 5 output ends the sequence by resetting IC4b/c bistable.

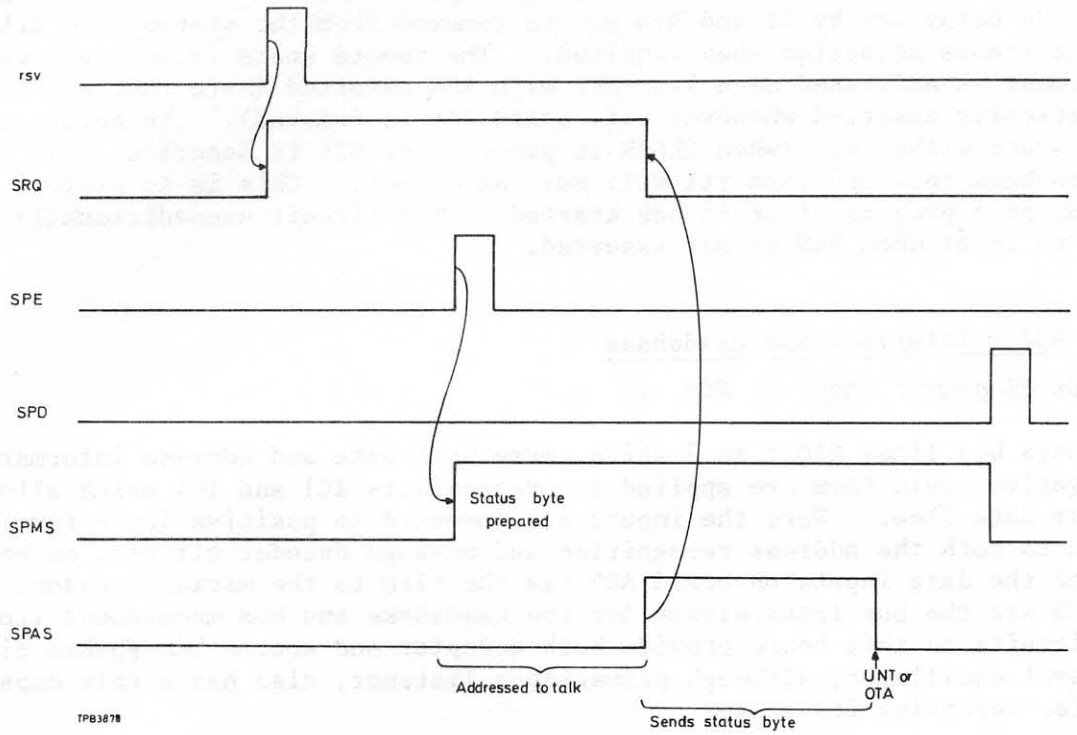


Fig. 43 Simplified timing diagram of service request and serial poll (arrows go from cause to effect)

Local/remote selection

147. The local/remote selection circuit basically comprises bistables IC8c with IC7b, and IC8a with IC6a. Fig. 44 shows the simplified timing diagram for the circuit. At switch-on, the instrument automatically enters the local state and responds to the settings of the front panel controls. The initial local state is achieved by means of the microprocessor reset signal to contact 6.

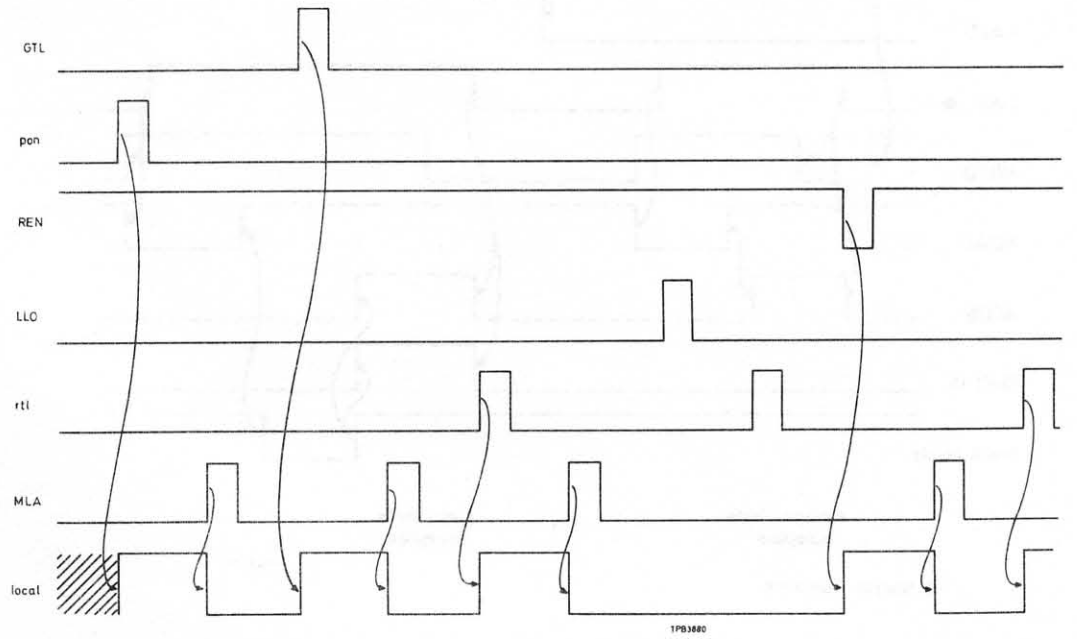


Fig. 44 Simplified local/remote timing diagram (arrows go from cause to effect)

This asserts pon which resets the local/remote bistable and takes contact 10 low. When the microprocessor has powered up, contact 6 is taken high so that after the delay set by C6 and R18 pon is removed from the bistable to allow subsequent remote selection when required. The remote state is achieved when the instrument is addressed as a listener with REN asserted (note that REN is also automatically asserted whenever r.f. board AA6 is removed). To return to the local state either rtl (when CLEAR is pressed) or GTL is asserted. If however, LLO has been received then rtl will have no effect. This is to prevent interruption of a program after it has started. The circuit unconditionally reverts to local when REN is not asserted.

Board AB7 - Interface and handshake

Circuit diagram : Chap. 7, Fig. 16

148. Data bus lines DIO 1 to 7 which carry both data and address information in negative logic form are applied to transceivers IC1 and IC4 which allow two-way data flow. Here the inputs are inverted to positive logic form and passed to both the address recognition and message decoder circuits on board AB6 and the data inputs on board AB5 via the FIFO to the microprocessor. IC2 and IC3 are the bus transceivers for the handshake and bus management lines. The circuits on this board provide both acceptor and source handshakes since the level oscillator, although primarily a listener, also has a talk capability e.g. for reporting its status.

Acceptor handshake

149. The operation of the acceptor handshake is shown in the simplified timing diagram Fig. 45. The sequence is started by the controller designating the sender to be a listener by placing the sender's listen address on the DIO data

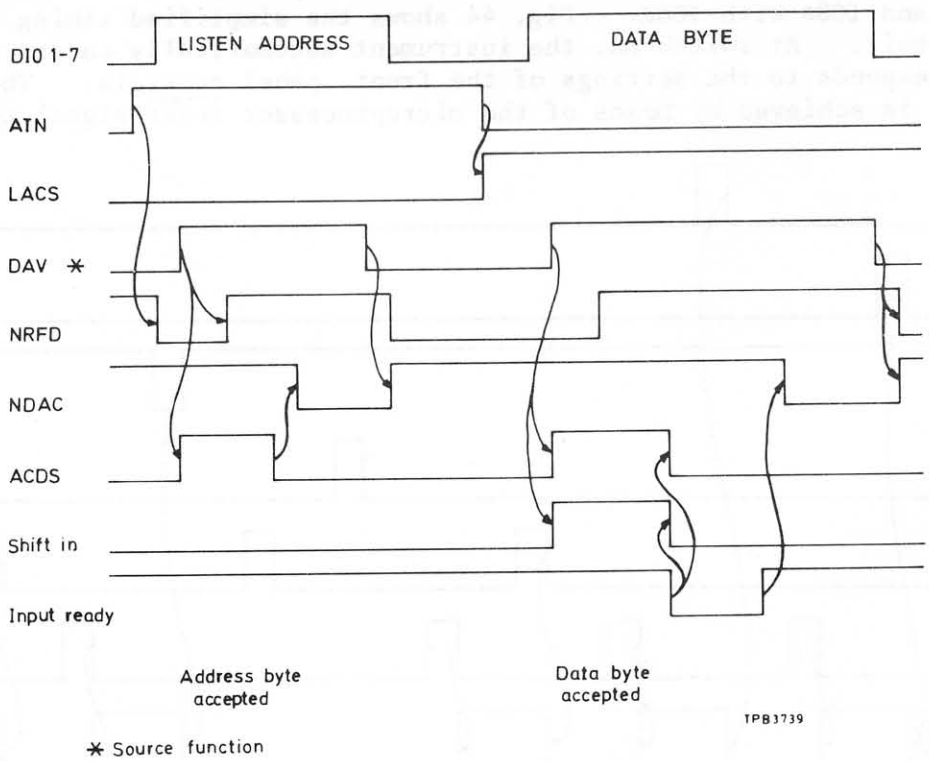


Fig. 45 Simplified timing diagram of acceptor handshakes showing the sender being designated a listener and then the listener accepting a data byte from a designated talker

lines with ATN asserted and DAV unasserted to indicate that the data are not yet settled and valid. ATN asserted by the controller causes the $\overline{\text{AIDS}}$ line to go high to contact B9 via board AB6. With the $\overline{\text{AIDS}}$ line high and the DAV line low to AND gate IC10b, the R-S latch IC6a and IC6b and gating remove NRFD to indicate the interface's readiness to receive data. Upon this, the controller asserts DAV which sets the ACDS line high via IC10d and the address byte is accepted. The DAV line going high asserts NRFD via IC11b and IC10a. The high on the ACDS line to IC11d causes C6 to discharge until Schmitt trigger IC9b switches to provide a positive delay pulse. This pulse resets the R-S latch which takes the ACDS line low to IC11d. C6 then charges until IC9b triggers to end the delay pulse. This removes NDAC via NOR gates IC11c and IC11a to signify acceptance of the data byte. To end the address handshake the controller removes DAV. This asserts NDAC via IC11a and removes NRFD via IC11b ready for the following data byte.

150. Data is transferred in a similar manner to that used for the address but with ATN removed by the controller to enable the designated talker to pass the data byte or bytes to the listeners. ATN unasserted takes the LACS line high at contact B11 to put the interface into the listener active state. To start the handshake the talker asserts DAV which is passed in via IC11b and IC10a to assert NRFD. DAV also causes the interface to enter ACDS via IC10b and IC10d, and puts 'shift in' high via IC10c to the FIFO on board AB5. The data byte is loaded into the FIFO and the input ready signal goes low. When ready to accept a second data byte ir from the FIFO goes high. This removes NDAC to indicate receipt of data via IC9a,d and IC11c,a. The data handshake is completed by the talker removing DAV which resets the R-S latch to assert NDAC and remove NRFD to indicate readiness for further data.

Source handshake

151. After the sender has been addressed to talk by the controller TACS is asserted from board AB6 which takes contact B10 high. The high on the TACS line and the high on the NDAC line are gated by IC6d and passed via IC8b to set rfd high at contact 29. The rfd signal is taken to board AB5 and results in the microprocessor placing a data byte on the data output lines. The high on the TACS line also enables transceivers IC1 and IC4 so that the byte is placed on the DIO lines and transferred to the designated listener by the handshake process shown in Fig. 46. The nba (new byte available) signal to contact 30 goes low then high to indicate that the two 4-bit words forming the data byte have both been placed on the data output lines from AB5. When nba transits from low to high, D-type bistable IC12 is clocked and, with the data line to earth, $\overline{Q}$ goes high which sets rfd low. C7 then charges through R2 and after this delay to allow the data lines to settle Schmitt trigger IC9c switches. When the listeners remove NRFD, i.e. they are ready for data, IC12b $\overline{Q}$ output is taken low via NOR gate IC8d. This asserts DAV to indicate that the data lines have settled. After the data has been accepted, the listeners remove NDAC and this removes DAV via the set input to IC12a and Schmitt trigger IC9c. Finally, NDAC is asserted by the listeners when ready for the next data byte and this takes rfd high.

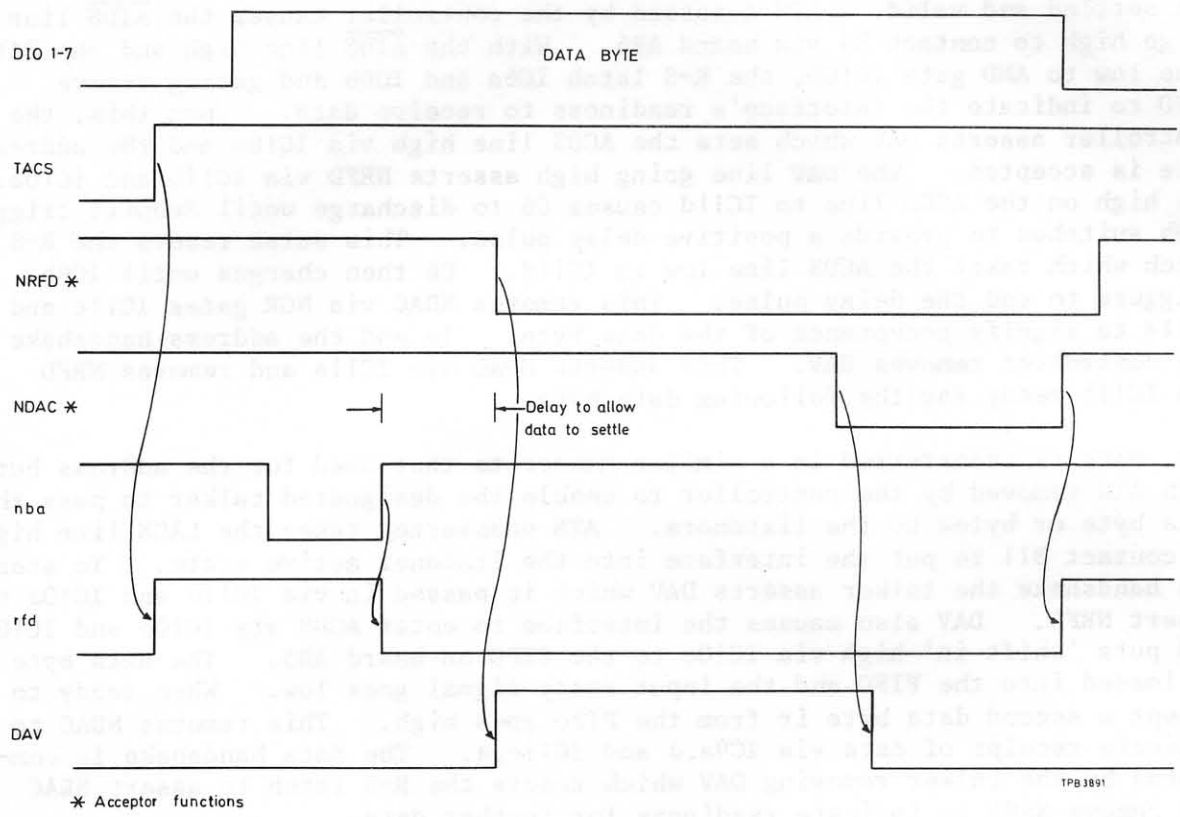


Fig. 46 Simplified timing diagram of source handshake

Board AB16 - Level shifter

Circuit diagram : Chap. 7, Fig. 16

152. This board performs level shifting between the t.t.l. and c.m.o.s. logic levels used by the GPIB interface and the microprocessor boards respectively. Data transferred to the GPIB boards are shifted in level by resistors R2 to R9 each of which forms a potential divider with a pull-up resistor on board AB5. Data transferred to the microprocessor is shifted in level by electronic switches TR1 to TR6 which switch the output between the +7.5 V and -7.5 V power rails.

Chapter 5

MAINTENANCE

CONTENTS

GENERAL

1. This chapter contains information for keeping the instrument in good working order and checking its overall performance, and to assist in fault finding and repairing the instrument. For these purposes this chapter should be read in conjunction with the Technical Description Chap. 4, and the Circuit Diagrams Chap. 7.

2. Integrated circuits and semiconductor devices are used throughout this instrument and, although these have inherent long term reliability and mechanical ruggedness, they are susceptible to damage by overloading, reversed polarity and excessive heat or radiation. Avoid hazards such as prolonged soldering, strong r.f. fields or other forms of radiation and the use of insulation testers.

3. In case of difficulties which cannot be resolved with the aid of this book, please contact our Service Division at the address given inside the rear cover, or your nearest Marconi Instruments representative. Always quote the type and serial number found on the data plate at the rear of the instrument.

PERFORMANCE TESTS

4. Test procedures described in this chapter may be simplified and of restricted range compared with those that relate to the generally more comprehensive factory test facilities which are necessary to demonstrate complete compliance with the specifications.

5. Performance limits quoted are for guidance and should not be taken as guaranteed performance specifications unless they are also quoted in the Performance Data in Chap. 1.

6. When making tests to verify that the instrument meets the stated performance limits, allowance must always be made for the uncertainty of the test equipment used.

ACCESS TO BOARDS AND COMPONENTS

Removal of case

7. The case is in two sections. Both upper and lower halves are secured by four M4 screws which are located at the sides of the instrument.

Removal of covers

8. The top of the instrument is protected by three covers which are fastened by M3 screws and captive studs. To release a cover, remove the screws (if fitted) and turn the studs approximately a quarter turn anti-clockwise until the slots in the stud heads are aligned with the bars marked on the cover. The cover may now be lifted off to expose the boards and units.

Removal of boards

9. The majority of components are mounted on plug-in printed circuit boards which may be lifted out from above the instrument. Note that to prevent damage to the flexistrip connecting microprocessor and memory boards AB2 and AB3 always remove these boards as a pair.

Access to front panel

10. Access to the rear of the front panel is obtained after removing the four handle fixing screws and detaching the handles. The panel will then hinge forwards. The two display boards may now be removed after releasing the 4 corner screws. Shouldered hexagonal pillars separate the boards which may be parted after removing the centre screw.

Access to test points

11. Access to board contacts for test purposes without having to remove boards or units may be made via the underboard sockets or, in the case of the control unit assembly, via the mother board accessible from the underside of the assembly. To obtain access to board components and test points the boards may be removed and reconnected to the instrument via the extender boards which are available as optional accessories.

Access to adjustment points

12. Many adjustment points are accessible from above. Adjustment locations for each of the three main assemblies, r.f. unit, control unit and local oscillator unit are shown in the top views in Figs. 1 to 3. The lower views identify board socket locations. For ease of identification these illustrations all show the instrument as viewed when it is supported by its side feet.

FUSE REPLACEMENT

13. Two cartridge-type fuses are located on the rear panel. These main supply fuses are slow blow, 800 mA for 95 to 130 V a.c. and 400 mA for 190 to 260 V a.c. Two 2 A quick acting fuses on board AB11 protect the battery charge and instrument d.c. power supplies. A 1 A quick acting fuse on board AB15 protects the d.c. power supply to the GPIB boards. Switch off the power supply when replacing a fuse.

TRANSISTOR AND DIODE CHECKING

14. Transistors may be checked by measuring the electrode voltages and/or by measuring the resistance between electrodes by means of a multimeter. So that the meter voltage does not damage the transistors or diodes use the lowest voltage and the maximum source resistance available, e.g. the Ω range on the AVO 8 or the SEI Selectest Super 50.

TEST EQUIPMENT

15. The test equipment required for the maintenance and repair of the instrument is listed in Table 1.

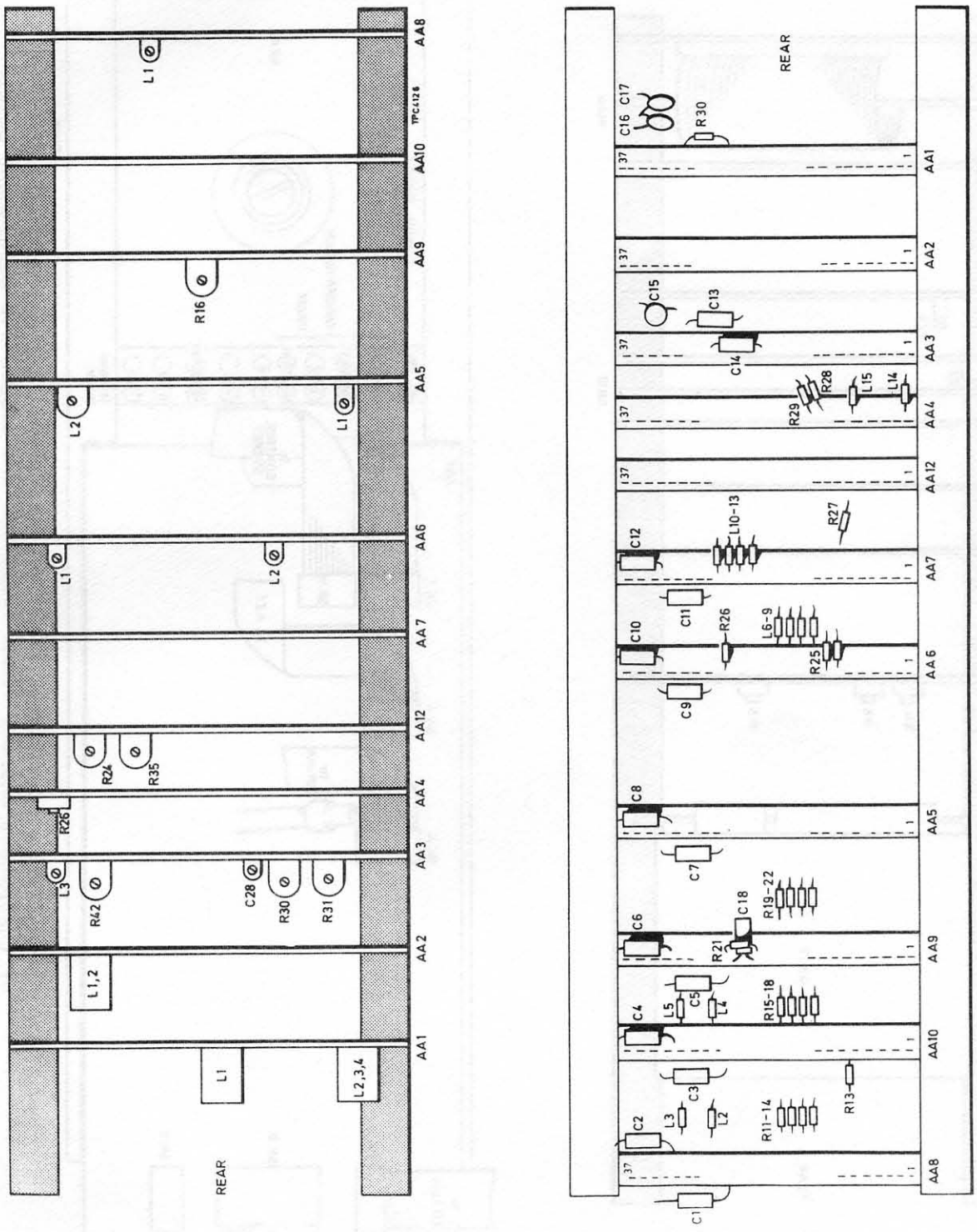


Fig. 1 RF unit assembly. Views of top (above) and bottom (below) of instrument showing board locations and accessible adjustment points

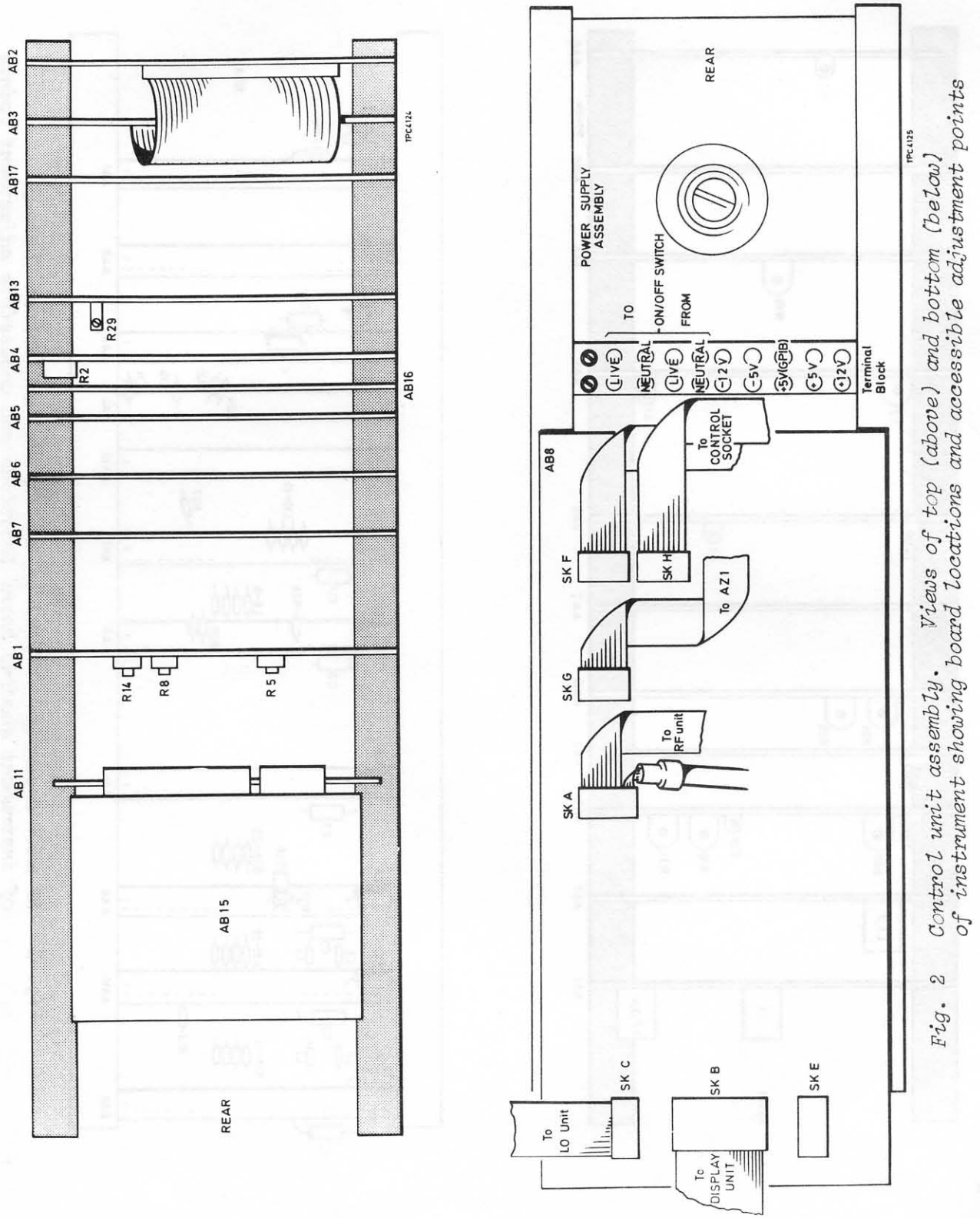


Fig. 2 Control unit assembly. Views of top (above) and bottom (below) of instrument showing board locations and accessible adjustment points

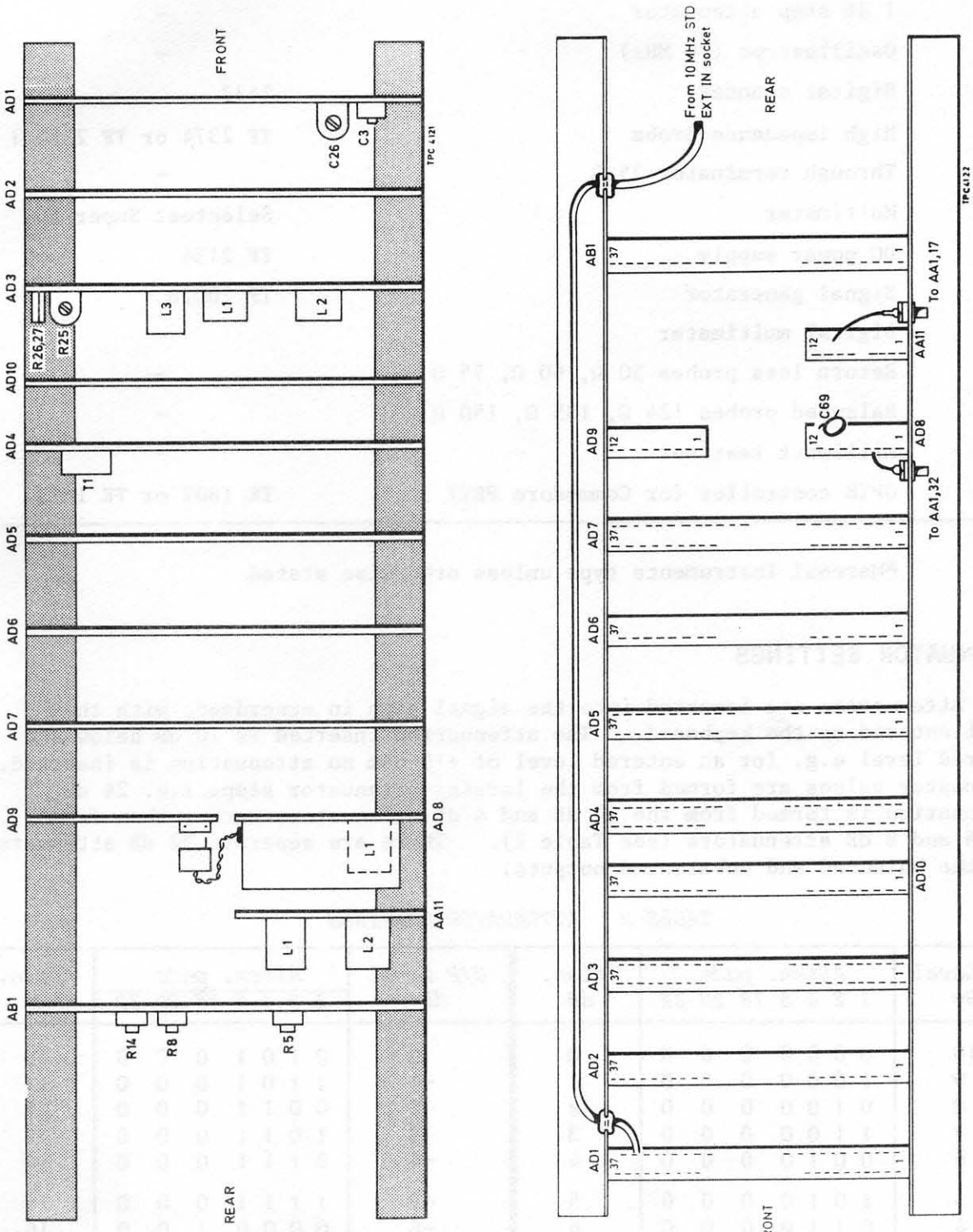


Fig. 3 Local oscillator unit assembly. Views of top (above) and bottom (below) of instrument showing board locations and accessible adjustment points

TABLE 1 TEST EQUIPMENT

Item	*Description*	*Recommended model**
a	Spectrum analyser	TF 2370 or TF 2370/1
b	1 dB step attenuator	-
c	Oscilloscope (50 MHz)	-
d	Digital counter	2437
e	High impedance probe	TF 2374 or TF 2374/1
f	Through terminator 75 Ω	-
g	Multimeter	Selectest Super 50
h	DC power supply	TF 2154
i	Signal generator	TF 2002B
j	Digital multimeter	-
k	Return loss probes 50 Ω, 60 Ω, 75 Ω	-
l	Balanced probes 124 Ω, 135 Ω, 150 Ω	-
m	Milliwatt test set	-
n	GPIB controller (or Commodore PET)	TK 1802 or TK 1813

*Marconi Instruments type unless otherwise stated

ATTENUATOR SETTINGS

16. Attenuators are inserted into the signal path in accordance with the level entered on the keyboard. The attenuation inserted is 10 dB below the entered level e.g. for an entered level of +10 dBm no attenuation is inserted. Attenuator values are formed from the largest attenuator steps i.e. 24 dB attenuation is formed from the 20 dB and 4 dB attenuators rather than from 16 dB and 8 dB attenuators (see Table 2). There are separate 32 dB attenuators for the balanced and unbalanced outputs.

TABLE 2 ATTENUATOR SETTINGS

O/P Level dBm	*Atten. pads* 1 2 4 8 16 20 32	*Atten. dB*	*O/P Level dBm*	*Atten. pads* 1 2 4 8 16 20 32	*Atten. dB*
10	0 0 0 0 0 0 0	0	0	0 1 0 1 0 0 0	10
9	1 0 0 0 0 0 0	1	-1	1 1 0 1 0 0 0	11
8	0 1 0 0 0 0 0	2	-2	0 0 1 1 0 0 0	12
7	1 1 0 0 0 0 0	3	-3	1 0 1 1 0 0 0	13
6	0 0 1 0 0 0 0	4	-4	0 1 1 1 0 0 0	14
5	1 0 1 0 0 0 0	5	-5	1 1 1 1 0 0 0	15
4	0 1 1 0 0 0 0	6	-6	0 0 0 0 1 0 0	16
3	1 1 1 0 0 0 0	7	-7	1 0 0 0 1 0 0	17
2	0 0 0 1 0 0 0	8	-8	0 1 0 0 1 0 0	18
1	1 0 0 1 0 0 0	9	-9	1 1 0 0 1 0 0	19

TABLE 2 ATTENUATOR SETTINGS (continued)

O/P Level dBm	Atten. pads 1 2 4 8 16 20 32	Atten. dB	O/P Level dBm	Atten. pads 1 2 4 8 16 20 32	Atten. dB
-10	0 0 0 0 0 1 0	20	-40	0 1 0 0 1 0 1	50
-11	1 0 0 0 0 1 0	21	-41	1 1 0 0 1 0 1	51
-12	0 1 0 0 0 1 0	22	-42	0 0 0 0 0 1 1	52
-13	1 1 0 0 0 1 0	23	-43	1 0 0 0 0 1 1	53
-14	0 0 1 0 0 1 0	24	-44	0 1 0 0 0 1 1	54
-15	1 0 1 0 0 1 0	25	-45	1 1 0 0 0 1 1	55
-16	0 1 1 0 0 1 0	26	-46	0 0 1 0 0 1 1	56
-17	1 1 1 0 0 1 0	27	-47	1 0 1 0 0 1 1	57
-18	0 0 0 1 0 1 0	28	-48	0 1 1 0 0 1 1	58
-19	1 0 0 1 0 1 0	29	-49	1 1 1 0 0 1 1	59
-20	0 1 0 1 0 1 0	30	-50	0 0 0 1 0 1 1	60
-21	1 1 0 1 0 1 0	31	-51	1 0 0 1 0 1 1	61
-22	0 0 0 0 0 0 1	32	-52	0 1 0 1 0 1 1	62
-23	1 0 0 0 0 0 1	33	-53	1 1 0 1 0 1 1	63
-24	0 1 0 0 0 0 1	34	-54	0 0 1 1 0 1 1	64
-25	1 1 0 0 0 0 1	35	-55	1 0 1 1 0 1 1	65
-26	0 0 1 0 0 0 1	36	-56	0 1 1 1 0 1 1	66
-27	1 0 1 0 0 0 1	37	-57	1 1 1 1 0 1 1	67
-28	0 1 1 0 0 0 1	38	-58	0 0 0 0 1 1 1	68
-29	1 1 1 0 0 0 1	39	-59	1 0 0 0 1 1 1	69
-30	0 0 0 1 0 0 1	40	-60	0 1 0 0 1 1 1	70
-31	1 0 0 1 0 0 1	41	-61	1 1 0 0 1 1 1	71
-32	0 1 0 1 0 0 1	42	-62	0 0 1 0 1 1 1	72
-33	1 1 0 1 0 0 1	43	-63	1 0 1 0 1 1 1	73
-34	0 0 1 1 0 0 1	44	-64	0 1 1 0 1 1 1	74
-35	1 0 1 1 0 0 1	45	-65	1 1 1 0 1 1 1	75
-36	0 1 1 1 0 0 1	46	-66	0 0 0 1 1 1 1	76
-37	1 1 1 1 0 0 1	47	-67	1 0 0 1 1 1 1	77
-38	0 0 0 0 1 0 1	48	-68	0 1 0 1 1 1 1	78
-39	1 0 0 0 1 0 1	49	-69	1 1 0 1 1 1 1	79
			-70	0 0 1 1 1 1 1	80

FAULT FINDING

17. The fault finding tables which follow provide a systematic procedure for localizing faults to board level or to comparatively small groups of components. Fig. 4 summarizes the fault finding procedure. Start at Table A and observe the display while carrying out the steps in the table. This should indicate the fault in one of three probable areas each of which is checked by means of tables. These areas are control unit (entered via Table B), local oscillator unit (Table I) and r.f. unit (Tables D and F). The local oscillator and r.f. units are covered in detail by secondary tables. Those for the local oscillator check the three phase locked loops (Tables J to L) while the r.f. unit tables check the signal source and attenuators and work towards the output (Tables D to H). Following this procedure the fault may be traced to component level using the board checks detailed under 'Board Testing'.

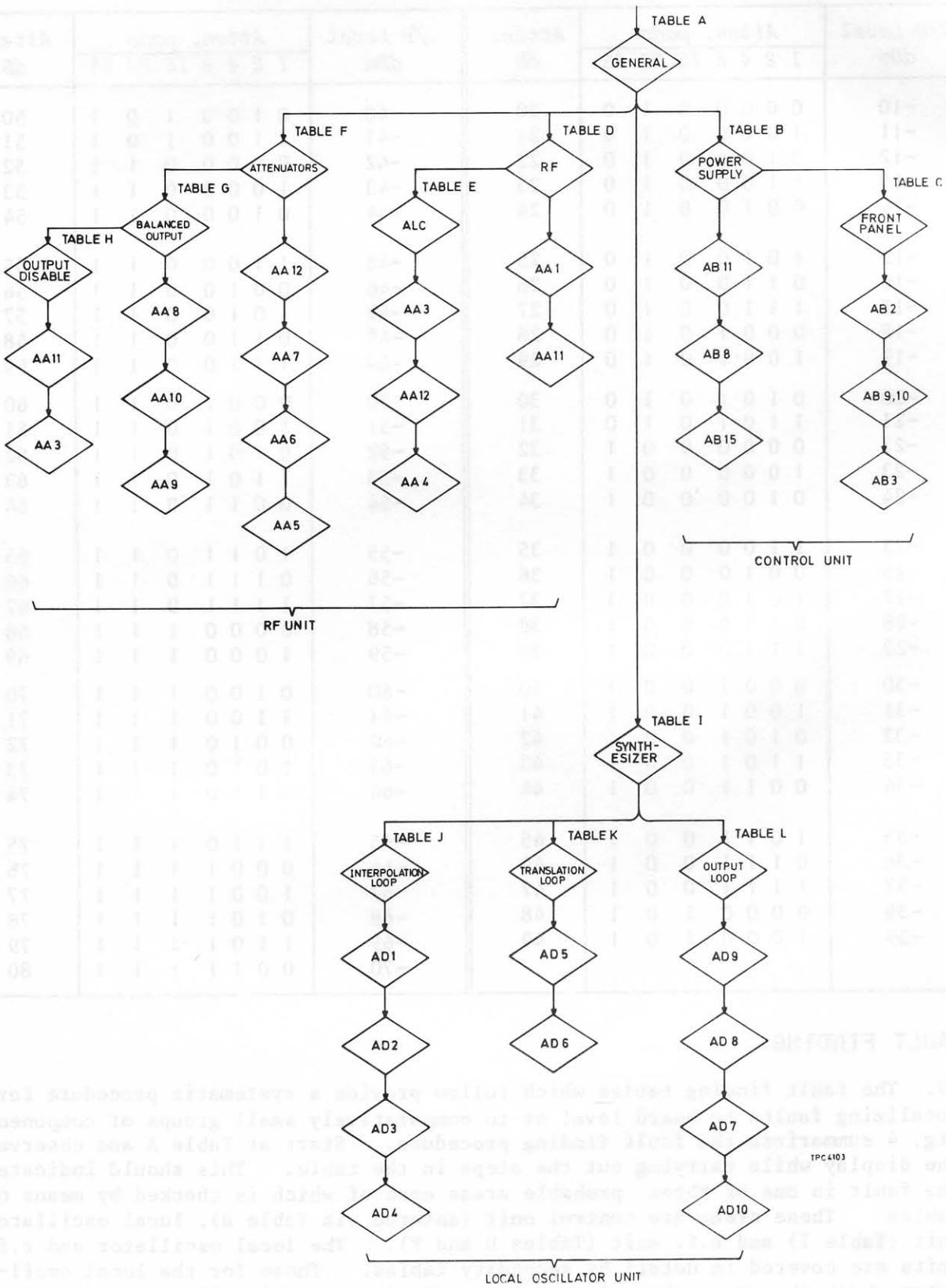


Fig. 4 Fault finding procedure summary

TABLE A FAULT FINDING - GENERAL

01. Set supply switch to ∿. If display does not light up go to Table B.

02. Select SLM CONTROL OFF, KEYBOARD, dBm and OUTPUT SEND. Check that no loads are connected to 10 MHz STD EXT IN or 30-50 MHz IN sockets. Check OUTPUT socket for 1 MHz. If not, go to Table I.

03. Display should read -70.0 dBm, 1000.00 kHz. If not, go to Table C.

04. If EXT LEVELLING HIGH or LOW lamps are lit go to Table D.

05. Select 75 Ω output impedance. If level from OUTPUT socket is not 2.45 V p-p go to 10.

06. Select KEYBOARD + FINE. Adjust FINE LEVELcontrol to indicate f.s.d. on meter. If level at OUTPUT socket varies by ±1.1 dB go to Table F.

07. If AA4, 22 changes ±7.5 V as FINE LEVEL control is varied there is a fault on AA4.

08. Check AA4, 26/27 for +7.5 V and AA4, 30/31 for -7.5 V. If not, go to Table B.

09. FINE LEVEL potentiometer is faulty.

10. If AA3, 6 is not at +10 dBm go to Table D.

11. If AA7, 32 is not at +10 dBm there is a fault on AA7 (or with data input to board).

12. If AA6, 6 is not at +10 dBm there is a fault on AA6 (or with data input to board).

13. If AA5, 32 is at +10 dBm there is a fault on AA8 (or with data input to board).

14. Press ENTER and check AA5, 17 for positive-going +7.5 V pulse. If not, data input to AA6 is faulty or there is a fault on AA6 (check power supplies, IC1, TR5, TR6).

15. There is a fault on AA5 (check power supplies, RLA, RLB).

16. If fault is still unidentified return instrument to Marconi Instruments Service Division.

TABLE B FAULT FINDING - POWER SUPPLY

01. Check supply fuses.
02. If voltage on AB8, +12 V tag is +12 V ±0.6 V go to 10.
03. If voltage on AB11, PLA contact 11 is +28 V nominal there is a fault on AB12.
04. If voltage on AB11, PLA contact 7 is +28 V nominal, replace AB11 FS1.
05. If voltage on AB11, tag 2 is 22 V a.c. rectifier circuit is faulty.
06. Either wiring or mains transformer is faulty.
10. If voltage on AB8 -12 V tag is -11.4 V go to 20.
11. If voltage on AB15 tag 10 is -12 V, AB15 D5 is faulty.
12. If voltage on AB11, PLA contact 8 is -28 V nominal there is a fault on AB12.
13. If voltage on AB11, tag 5 is -28 V nominal, replace AB11 FS2.
14. If voltage on AB11, tag 1 is 22 V a.c. rectifier circuit is faulty.
15. Wiring or supply transformer is faulty.
20. If voltage on AB8, +7.5 V tag is +7.5 V ±0.02 V go to 25.
21. AB1 is faulty or there is a short on +7.5 V supply rail.
25. If voltage on AB8, -7.5 V tag is -7.5 V ±0.04 V go to 30.
26. AB1 is faulty or there is a short on -7.5 V supply rail.
30. If voltage on AB8, +5 V tag is +5 V ±0.25 V go to 35.
31. AB15 is faulty or there is a short on +5 V rail.
35. If voltage on AB8, -5 V tag is -5 V ±0.25 V go to 40.
36. AB15 is faulty or there is a short on -5 V rail.
40. If voltage on AB8, tag 13 is +5 V ±0.25 V go to 45.
41. AB15 is faulty or there is a short on +5 V (GPIB) rail.
45. If battery selection is not needed go to Table C.
46. Connect 62 Ω 12 W resistor across + and - battery connections with centre-tap open circuit.
47. If measured voltage is not 27 V ±20%, AB11 trickle charger section is faulty.
48. Set SUPPLY selector to CHARGE.
49. Check that CHARGE lamp lights.
50. If measured voltage is not 27 V ±20% AB11 charge section is faulty.
51. Set SUPPLY selector to OFF and disconnect resistor.
52. Switch SUPPLY to ON and go to Table C.

TABLE C FAULT FINDING - PROCESSOR/FRONT PANEL

01.	Check AB2, 29 for processor clock waveform. If not go to 10.
02.	Check AB2, 31 for SYNC waveform (see Fig. 5). If not, IC2 is probably faulty.
03.	Check AB8 tags 26, 27, 29, 30 for 'random' data at ±7.5 V when ENTER is pressed. If levels incorrect, remove AA4 to AA10 in turn until fault found. If not, AB2 faulty (probably IC7).
04.	Check AB8 ROM 0 OUT tags 9, 10, 16 and 17 for 'random' data switching between +7.5 V and -7.5 V. If not present, there is a fault on AB2 (probably IC9).
05.	Check that 24-way lead from AB8, SKB to front panel is firmly plugged in.
06.	If display still does not light up, then fault lies in front panel circuits i.e. AB9, AB10.
07.	Monitor AB8, tag 29 using oscilloscope. Press ENTER and CLEAR alternately. Waveform should alter each time either key is pressed. If yes, keyboard is being 'read' and fault lies in display section. If no, address decoder/latch circuits are probably faulty.
10.	If AB2, B11/B12 is not at +7.5 V there is a fault on AB20, AB2 or AB3. Remove AB2/AB3 and recheck.
11.	If AB2, B7/B8 is not at -7.5 V there is a fault on AB20, AB2 or AB3. Remove AB2/AB3 and recheck.
12.	There is a fault on AB2 (probably IC1).
13.	If fault is still unidentified return instrument to Marconi Instruments Service Division.

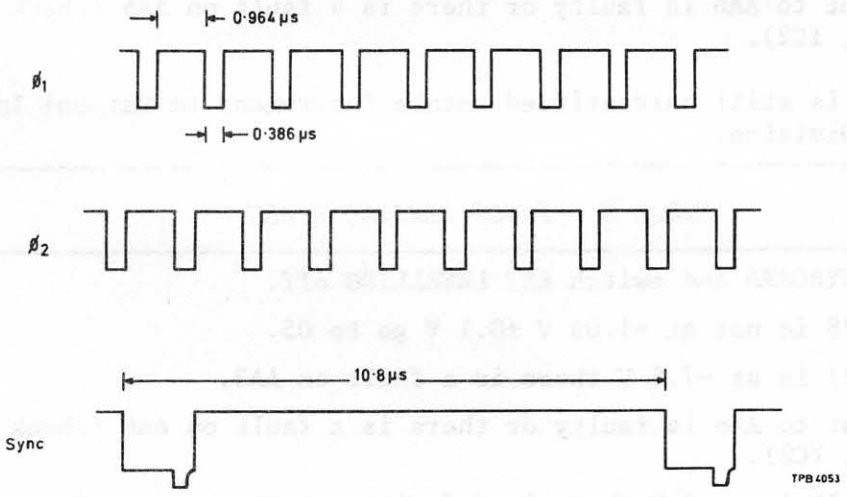


Fig. 5 Microprocessor timing

TABLE D FAULT FINDING - RF

01.	If AA1, 32 is not at 30.1 MHz, -10 dBm ±2 dB into 50 Ω go to 05.
02.	If AA11, 12 is not at 10 MHz, -14 dBm ±2 dB into 50 Ω there is a fault on AD1 (check power supplies, TR6).
03.	Go to 10.
05.	If AA1, 4 is at +7.3 V ±0.2 V go to Table I.
06.	There is a fault on AA1 (check power supplies, TR1, TR2, TR3).
10.	Switch EXT LEVELLING ON with no connection to EXT LEVELLING socket.
11.	If FINE LEVEL control can be adjusted to give 0 V on AA11, 2 go to 15.
12.	If AA4, 22 changes ±7.5 V at FINE LEVEL control is varied there is a fault on AA4.
13.	If ±7.5 V supplies are correct FINE LEVEL potentiometer is faulty.
15.	With AA11, 2 at 0 V is AA11, 7 at 30 MHz, -22 dBm ±1 dB? If not, go to 20.
16.	If AA1, 6 is not at -28 dBm ±1 dB into 50 Ω there is a fault on AA1.
17.	If AA2, 32 is not at -8 dBm ±1 dB into 75 Ω there is a fault on AA2.
18.	Go to Table E.
20.	If AA11, 1 is at -7.5 V there is a fault on AA11.
21.	Data input to AA6 is faulty or there is a fault on AA6 (check power supplies, IC2).
22.	If fault is still unidentified return instrument to Marconi Instruments Service Division.

TABLE E FAULT FINDING - ALC

01.	Select KEYBOARD and switch EXT LEVELLING off.
02.	If AA3, 28 is not at -1.05 V ±0.1 V go to 05.
03.	If AA3, 21 is at -7.5 V there is a fault on AA3.
04.	Data input to AA6 is faulty or there is a fault on AA6 (check power supplies, IC2).
05.	If AA12, 21 is at 0 V there is a fault on AA12.
06.	If AA4, 22 changes ±7.5 V as FINE LEVEL control is varied there is a fault on AA4.
07.	If ±7.5 V supplies are correct FINE LEVEL potentiometer is faulty.
08.	If fault is still unidentified return instrument to Marconi Instruments Service Division.

TABLE F FAULT FINDING - ATTENUATORS

01.	Check for operation of 0.1, 0.2, 0.4 and 0.8 dB attenuator steps. If not, data input to AA12 is faulty or there is a fault on AA12 (check IC1, IC3, IC4).
02.	Check for operation of 1, 2, 4 and 8 dB attenuator steps. If not, data input to AA7 is faulty or there is a fault on AA7.
03.	Check for operation of 16 and 20 dB attenuator steps. If not, data input to AA6 is faulty or there is a fault on AA6.
04.	If 32 dB attenuator step operates go to 10.
05.	With 32 dB attenuator step selected check AA5, 17 for +7.5 V 6 ms pulse each time ENTER is pressed. Select 32 dB attenuator step out and check AA5, 17 for -7.5 V 6 ms pulse each time ENTER is pressed. If not, data input to AA6 is faulty or AA6 is faulty (check TR5, TR6, IC1).
06.	There is a fault on AA5 (check RLA, RLB).
10.	Enter 0 dBm on keyboard.
11.	Check at OUTPUT socket for 0.632 V pk-pk across 50 Ω load when 50 Ω impedance selected, and for 0.693 V pk-pk across 60 Ω when 60 Ω impedance selected. If so go to Table G.
12.	Data input to AA8 is faulty or there is a fault on AA8 (check IC1, TR1, TR2, TR3, RLA, RLB, RLC).
13.	If fault is still unidentified return instrument to Marconi Instruments Service Division.

TABLE G FAULT FINDING - BALANCED OUTPUT

01. Select 150 Ω impedance. Load BALANCED OUTPUT socket with 150 Ω and check for 1.095 V pk-pk. If so, go to 10.

02. Check AA9, 6 for 775 mV pk-pk. If so, data input to AA8 is faulty or there is a fault on AA8 (check IC1, TR3, RLD).

03. Check AA10, 17 for 6.9 V pk-pk. If so, data input to AA10 is faulty or there is a fault on AA10.

04. Check AA9, 21 for 6.9 V pk-pk. If so, data input to AA8 is faulty or there is a fault on AA8 (check IC1, TR4, RLE).

05. Data input to AA9 is faulty or there is a fault on AA9.

10. Select in turn 135 Ω, 124 Ω and 0 Ω balanced impedances and load BALANCED OUTPUT socket with 135 Ω, 124 Ω and 150 Ω respectively. Check for 1.039 V, 0.996 V and 1.095 V respectively. If not, data input to AA10 is faulty or AA10 is faulty.

11. If, with balanced impedance selected, 32 dB attenuator step operates go to 15.

12. With 32 dB attenuator step selected, check AA10, 21 for +7.5 V 6 ms pulse each time ENTER is pressed. Select 32 dB attenuator step out and check AA10, 21 for -7.5 V 6 ms pulse each time ENTER is pressed. If not, data input to AA6 is faulty or AA6 is faulty (check IC1).

13. There is a fault on AA10 (check TR2, TR5, RLA).

15. Select 0 Ω unbalanced impedance. Load OUTPUT socket with 75 Ω load and check for 775 mV pk-pk. If so, go to Table H.

16. Data input to AA8 is faulty or there is a fault on AA8 (check IC1, TR4, RLE).

17. If fault is still unidentified return instrument to Marconi Instruments Service Division.

TABLE H FAULT FINDING - OUTPUT DISABLE

01. Select 0 dBm and 75 Ω output impedance.

02. Check at OUTPUT socket that level drops by at least 60 dB when OUTPUT OFF is selected. If so, go to 12.

03. If, with OUTPUT OFF selected, level at AA11, 2 is less than -6.5 V go to 10.

04. If, with OUTPUT OFF selected, AA3, 21 is at +7.5 V there is a fault on AA3 (check D5).

05. Data input to AA6 is faulty or there is a fault on AA6 (check IC2).

10. If, with OUTPUT OFF selected, AA11, 1 is at +7.5 V there is a fault on AA11 (check IC1, TR3, D1).

11. Data input to AA6 is faulty or there is a fault on AA6 (check IC2).

12. If fault is still unidentified return instrument to Marconi Instruments Service Division.

TABLE I FAULT FINDING - SYNTHESIZER

01. Set instrument to 1 MHz and measure frequency on AD4, TP1. If this is not 12 MHz go to Table J.

02. Increment in 5 Hz steps from 1 MHz to 1.009995 MHz. If AD4, TP1 does not increment from 12 MHz in 500 Hz steps go to Table J.

03. Set instrument to frequencies listed. If frequencies on AD4,1 are not as shown there is a fault on AD4.

Instrument	*AD4 Contact 1*
1 MHz	777.2 Hz
2 MHz	752 Hz
5 MHz	688.07 Hz
15 MHz	534.76 Hz
19.999995 MHz	521.3 Hz

04. Set instrument to frequencies listed. If frequencies on AD6,21 are not as shown go to Table K.

Instrument	*AD6 Contact 21*
1 MHz	2.007772 MHz
2 MHz	2.00752 MHz
5 MHz	2.0068807 MHz
15 MHz	2.0053476 MHz
19.999995 MHz	2.005213 MHz

05. Set instrument to frequencies listed. If frequencies on AD6,37 are not as shown there is a fault on AD6.

Instrument	*AD6 Contact 37*
1 MHz	10.0389 kHz
2 MHz	10.0376 kHz
5 MHz	10.0344 kHz
15 MHz	10.0267 kHz
19.999995 MHz	10.0261 kHz

06. Set instrument to frequencies listed. If frequencies at AD8,12 are not as shown go to Table L.

Instrument	*AD8 Contact 12*
1 MHz	31 MHz
2 MHz	32 MHz
5 MHz	35 MHz
15 MHz	45 MHz
19.999995 MHz	49.999995 MHz

07. Tune instrument over entire frequency range and if level on AD8, 1 is not -10 dBm ±2 dBm there is a fault on AD8.

08. If fault is still unidentified return instrument to Marconi Instruments Service Division.

TABLE J FAULT FINDING - INTERPOLATION LOOP

01. Measure signal on AD3, 17. If it is not -10 dBm at 10 MHz there is a fault on AD1.

02. Measure frequency on AD2, 6. If it is not 200 kHz ±7.5 V there is a fault on AD1.

03. Set instrument to 1.005 MHz and examine signal on AD2, TP4. If it is a -5 V to +3 V ramp at 500 Hz go to 10.

04. Examine signal on AD2, IC3 pin 9. If it is a 500 Hz pulse train at 1:9 mark/space ratio ramp generator IC4 operation is faulty.

05. The operation of divider IC1, IC2 or IC3 is faulty.

10. Examine signal on AD2, 1. If it is a 500 Hz train of 0.5 µs pulses go to 20.

11. Examine signal on AD3, TP3. If it is a 2 to 3 MHz square wave divider IC4 operation is faulty or there is a fault on AD10.

12. Examine signal on AD4, 21. If it is a 12 to 13 MHz signal at -10 dBm go to 15.

13. Remove AD3 and connect AD4, 37 to earth. If a 13 MHz signal is not present on AD4 TR2 emitter, the v.c.o. operation is faulty.

14. Buffer TR3 is faulty.

15. Examine signal on AD3, tag 6. If it is not 0 dBm at 2 to 3 MHz mixer operation is faulty.

16. Amplifier TR2 operation is faulty.

20. Examine signal on AD2, TP5 and TP6. If 120 µs sampling pulses are not present pulse generator operation is faulty.

21. If sampling pulses separated by 200 µs occur regularly and during ramp rise time go to 30.

22. Check AD10 latched outputs.

23. Examine d.c. on AD2, 37. If level is fixed there is a fault with IC5 or TR9 of phase detector.

24. Examine d.c. on AD3, 37. If level is fixed there is a fault with D/A conversion and summation with error voltage.

25. There is a fault with AD4 v.c.o. operation.

30. Increment instrument from 1 MHz in 5 Hz steps to 1.009995 MHz. If frequency at AD4, TP1 does not increment from 12 MHz in 500 Hz steps to 12.9995 MHz repeat 10 and subsequent steps at the faulty frequency.

TABLE J FAULT FINDING - INTERPOLATION LOOP (contd.)

31. Set instrument to frequencies listed. If frequencies on AD4 contact 1 are not as shown there is a fault with dividers IC1 and IC3 operation.

Instrument	*AD4 Contact 1*
1 MHz	777.2 Hz
2 MHz	752 Hz
5 MHz	688.07 Hz
15 MHz	534.76 Hz
19.999995 MHz	521.3 Hz

32. If fault is still unidentified return instrument to Marconi Instruments Service Division.

TABLE K FAULT FINDING - TRANSLATION LOOP

01. Set instrument to frequencies listed. If frequencies on AD5,1 are not as shown go to Table J.

Instrument	*AD5 Contact 1*
1 MHz	777.2 Hz
2 MHz	752.82 Hz
5 MHz	688.07 Hz
15 MHz	534.76 Hz
19.999995 MHz	521.3 Hz

02. Measure frequency on AD5, 37. If it is not 2 MHz 0.1 V pk-pk there is a fault on AD1.

03. Examine signals on AD5, 1 and IC4 pin 11. If signals are in lock go to 15.

04. Remove AD5. Apply voltages listed to AD6, 6 and 9. If frequencies on IC1 pin 1 are not as shown there is a fault either with AD6 v.c.x.o. or with AD5 v.c.x.o. switching circuit.

Contact 6	*Contact 9*	*IC1 pin 1 (levels 0.8 V & 2 V)*	
-7 V	-7.5 V	10.0225 MHz	±2.5 kHz
0 V	-7.5 V	10.032 MHz	
+4 V	+7.5 V	10.045 MHz	

05. Measure frequency on AD6, 21 with AD5 replaced. If it is not approx. 2 MHz divide by five IC1 is faulty.

06. Disconnect link between AD5, 17 and AD6, 6. Set instrument to 8 MHz and AD6, 6 to 0 V. If AD5, IC3 pin 14 is not at approx. 6.5 kHz ±7.5 V mixer or low-pass filter is faulty.

07. If AD6, TP1 is not at approx. 650 Hz with link removed and AD6, 6 at 0 V, divider IC3 is faulty.

08. Remove board AD4 and connect AD5, IC4 pin 3 to pin 11. With link removed and AD6, 6 at 0 V check for positive voltage spikes at approx. 650 Hz on IC5 pin 6. If not present IC4 or IC5 is faulty. Disconnect pin 3 from pin 11. Reconnect link.

09. With AD4 removed and contact 1 disconnected, check that TR2 is off and TR4 is on. If not, TR2 or TR4 switching operation is faulty.

10. With AD4 removed and contact 1 disconnected, check that contact 17 is at 0 V. If not there is a fault with charge pump operation of TR3 or TR5. Replace board AD4.

TABLE K FAULT FINDING - TRANSLATION LOOP (contd.)

15. Set instrument to 7.12 MHz and check AD5, 6 is at -7.5 V. If not, there is a v.c.x.o. switching circuit fault.

16. Decrement instrument frequency by 5 Hz and check AD5, 6 is at +7.5 V. If not, there is a v.c.x.o. switching circuit fault.

17. Set instrument to the frequencies listed. If frequencies on AD6, IC1 pin 12 are not as shown IC1 operation is faulty.

Instrument	*IC1 pin 12*
1 MHz	1.00389 MHz
2 MHz	1.00376 MHz
5 MHz	1.00344 MHz
15 MHz	1.00267 MHz
19.999995 MHz	1.00261 MHz

18. Set instrument to frequencies listed. If frequencies on AD6, 37 are not as shown AD6, IC2 or IC3 is faulty.

Instrument	*AD6 Contact 37*
1 MHz	10.0389 MHz
2 MHz	10.0376 MHz
5 MHz	10.0344 MHz
15 MHz	10.0267 MHz
19.999995 MHz	10.0261 MHz

19. If the fault is still unidentified return instrument to Marconi Instruments Service Division.

TABLE L FAULT FINDING - OUTPUT LOOP

01. Set instrument to frequencies listed. If frequencies on AD9,7 are not as shown go to Table K.

Instrument	*AD9 Contact 7*
1 MHz	10.0389 kHz
2 MHz	10.0376 kHz
5 MHz	10.0344 kHz
15 MHz	10.0267 kHz
19.999995 MHz	10.0261 kHz

02. If pulse train on AD9, 1 is locked with that on contact 7 go to 50.

03. Check AD8, 4 for +7.5 V. If not, TR1, TR2 or TR3 on AA1 is faulty.

04. Disconnect AD8 input connector and set input to 0 V. If 39.5 MHz ±1 MHz 1 V pk-pk is not present on TR2 emitter, v.c.o. operation is faulty.

05. If AD8, 12 is not at 39.5 MHz ±1 MHz and -10 dBm, output buffer TR3 is faulty.

06. Set instrument to 10 MHz and check AD7, 32. If 0.5 µs pulses present at approx. 10 kHz go to 30.

10. Check for e.c.l. threshold voltages of -1.1 V and -1.5 V on AD7, IC1 pin 1. If levels incorrect, there is a fault with TR1 or TR2.

11. Set instrument to frequencies listed. If frequencies on AD7,1 are as shown go to 55.

Instrument	*AD7 Contact 1*
6 kHz	30.006 MHz
6.89 MHz	36.89 MHz
9.99 MHz	39.99 MHz
10.12 MHz	40.12 MHz
10.31 MHz	40.31 MHz

TABLE L FAULT FINDING - OUTPUT LOOP (contd.)

12. Set instrument to 10.12 MHz. If AD7, TP2 is not at v.c.o. frequency ÷20 at ±7.5 V then IC1 or IC2 divider operation is faulty.

13. Check AD7, TP6. If not permanently high go to 20.

14. If clock input to AD7, IC11 pin 11 is not present IC6 gating operation is faulty.

15. If AD7, IC11 pin 9 is low IC11 is faulty.

16. If AD7, IC9 pin 13 is low IC9 is faulty.

17. Presettable divider IC4 or IC5 reload operation is faulty.

20. Check that AD7, TP3 is at v.c.o. frequency ÷20 at ±7.5 V. If not, IC6c or IC6d is faulty.

21. Check that AD7, TP4 is at v.c.o. frequency ÷100. If not, divide by 5 operation is faulty.

22. Check that AD7, IC4 pin 12 is at v.c.o. frequency ÷4000. If not, IC4 or IC5 divider operation is faulty.

23. Check that AD7, TP5 is at v.c.o. frequency ÷4000. If not, IC9d or IC11b is faulty.

24. Check that AD7, IC3 pin 12 is at v.c.o. frequency ÷4000. If not, IC3 or IC11b is faulty.

25. Check for 0.5 µs negative pulses on AD7, IC3 pin 4. If not, IC10b or IC7 is faulty.

26. Change instrument frequency to 10.31 MHz and check AD7, IC3 pin 4 for negative pulses whose widths equate to 19 TP2 pulses (i.e. approx. 10 µs).

27. Check for one clock period delay (approx. 0.5 µs) between negative pulses on AD7, IC3 pin 4 and TR1. If not, IC10a operation is faulty.

28. Check for 1:1 mark/space ratio pulses on AD7, IC1 pin 3. If not, IC2 operation is faulty.

29. Set instrument to 10.14 MHz. Check that when AD7, TP1 goes low, widths of following first two pulses on TP2 are greater than remaining pulses.

30. Reconnect AD8 input connector. Check for high set pulses on AD9, IC2 pin 3. If present go to 35.

31. Check that AD9, IC1 pins 1 and 13 are clocked low. If not, IC1 is faulty.

32. IC2 is faulty on AD9.

35. Remove board AD7. Check that AD9, IC1 pins 1 and 12 are high. If not, there is a fault on IC1.

36. Check that AD9, IC3b is on and TR1 is off. If not, switch operation is faulty.

TABLE L FAULT FINDING - OUTPUT LOOP (contd.)

37. Check for +7.5 V at AD9, d.c. output plug. If not, current mirror operation is faulty. Replace AD7.

38. Remove board AD6. Check that AD9, IC1 pins 1 and 12 are low. If not, there is a fault on IC1.

39. Check that AD9, TR1 is on and IC3b is off. If not, switch operation is faulty.

40. Check for -7.5 V at AD9 d.c. output plug. If not, current mirror operation is faulty.

41. Check for +7.5 V at AD9, 12. If not, out of lock indicator operation is faulty.

42. Connect AD9, 1 and 7 together. Check for a low with positive-going spikes on IC1 pin 12, and a high with negative-going spikes on IC1 pin 1. If not, IC1 or IC2a is faulty.

43. Check that AD9, IC3b and TR1 are both off. If not, switch operation is faulty.

44. Check for 0 V at AD9 d.c. output plug. If not, current mirror operation is faulty.

45. Check for -7.5 V at AD9, 12. If not out of lock indicator operation is faulty. Remove connection between contacts 1 and 7. Replace board AD6.

50. Set instrument to 0.1 kHz and check AD8, 12 is at 30.0001 MHz, -10 dBm ±2 dBm. If not, AD8 v.c.o. operation is faulty.

55. Set instrument to frequencies listed. If frequencies at AD8, 12 are not as shown, suspect AD8 v.c.o. operation for errors at frequency limits, otherwise suspect AD7 division error and return to 10.

Instrument	*AD8 Contact 12*
1 MHz	31 MHz
2 MHz	32 MHz
5 MHz	35 MHz
15 MHz	45 MHz
19.999995 MHz	49.999995 MHz

56. If frequencies at AD8, 12 are at a fixed offset other than 30 MHz there is a fault on board AD10.

57. Check AA11, 12 for 10 MHz, -10 dBm into 50 Ω. If not, there is a fault on AD1.

58. If fault is still unidentified return instrument to Marconi Instruments Service Division.

BOARD TESTING

18. The board tests which follow may be used for fault finding to component level as well as being used to ensure correct board operation following repair or replacement. When testing at board level note that the various tests are carried out sequentially. This often means that test equipment and instrument settings for the second and subsequent tests in a sequence are dependent upon those used for the first test in the sequence.

19. Tables 3 to 5, which are intended for use with Figs. 1 to 3, summarize the board tests which are associated with the various adjustment points. Adjustment points shown in the tables but not in the figs. are normally only adjustable following board unit removal. Note however, that in the majority of cases adjustment should only be necessary following component replacement. Adjustments may then be made in accordance with the details given under the appropriate board headings.

TABLE 3 RF UNIT ASSEMBLY ADJUSTMENT GUIDE

Adjustment	*Board*	*Component*
30 MHz buffer	AA1	L1
20 MHz l.p. filter alignment	AA1	L2,L3,L4
31.1 MHz rejection	AA2	L1
46.1 MHz rejection	AA2	L2
RF gain	AA3	R42
Amplifier frequency response	AA3	L3
Level comparators	AA3	R30,R31
Levelled frequency response	AA3 AA12	C28 R35
RF level	AA4	R26
Output return loss	AA5 AA6 AA8	L1,L2 L1,L2 L1
Balanced output accuracy	AA9	R16
Output level	AA11	L1,L2
Output level accuracy	AA12	R35
Fine level	AA12	R24

Note...

Refer to relevant procedures detailed under board headings before attempting any adjustment.

TABLE 4 CONTROL UNIT ASSEMBLY ADJUSTMENT GUIDE

Adjustment	*Board*	*Component*
Voltage regulation	AB1	R8
Current limiting	AB1	R5,R14
Timing	AB4	R2
Ramp generation	AB13	R29

Note...

Refer to relevant procedures detailed under board headings before attempting any adjustment.

TABLE 5 LOCAL OSCILLATOR UNIT ADJUSTMENT GUIDE

Adjustment	*Board*	*Component*
Frequency multiplier output level	AA11	L1,L2
TCXO frequency	AD1	C3,C26
LP filter rejection	AD3	L1,L2
Mixer input level	AD3	L3
D/A conversion	AD3	R25,R26,R27
Ramp settling time	AD3	R26,R27
Oscillator frequency	AD4	T1
30-50 MHz v.c.o.	AD8	L1

Note...

Refer to relevant procedures detailed under board headings before attempting any adjustment.

AA1 - Mixer board

Test equipment : Items a, e and g.

Checking switching

20. The operation of electronic switches TR1, TR2 and TR3 controlling the +7.5 V supply to AD8 is checked as follows:-

(1) Connect a $\frac{1}{4}$ W resistor of less than 10 kΩ between AA1, 36 and 37 (or to 30-50 MHz IN socket on rear panel). Check for 0 V on AA1, 21.

(2) Remove resistor and check AA1, 21 for +7.5 V. Disconnect meter.

Checking limiter and mixer drive

21. Check the operation of limiter and mixer drive amplifiers TR4 to TR8 as follows:-

(1) Set analyser controls :

REFERENCE FREQUENCY	:	CENTRE 10 MHz
HORIZONTAL SCALE	:	2 MHz/div.
VERTICAL SCALE RANGE	:	1 dB/div.
VERTICAL SCALE	:	-25 dBm
FILTER BANDWIDTH	:	NORMAL
SWEEP MODE	:	SINGLE
STORE	:	REFRESH A
DISPLAY	:	A & B

(2) Connect analyser STD 10 MHz socket to its INPUT socket via probe fitted with x10 multiplier. Press analyser START button and read one sweep into STORE A as reference.

(3) Transfer probe to AA1, TP2.

(4) Enter 10 MHz on sender keyboard. Set analyser REFERENCE FREQUENCY to CENTRE 40 MHz and select REFRESH B.

(5) Press analyser START button, and adjusting VERTICAL SCALE as necessary, check that level is +12 dBm ±1 dB i.e. 22 dB above reference. If not, check limiter output.

(6) Check that level is within ±1 dB between 200 Hz and 20 MHz. If not, check limiter output.

Checking limiter output

22. If levels in (5) and (6) above are incorrect, check limiter TR5 and TR6 as follows:-

(1) Remove C11 and transfer probe to junction of C11 and R17 (do not use TP1 since capacitive loading may affect the measurement).

(2) Press analyser START button and check that level is -11 dBm ±1 dB i.e. 1 dB below stored reference.

(3) Check that level is within ±0.5 dB between 200 Hz and 20 MHz. Disconnect analyser and probe.

Adjusting 30 MHz buffer

23. This may be necessary following component replacement. Proceed as follows:-

(1) Select EXT LEVELLING ON and set FINE LEVEL control to centre of range. Observe sender meter and adjust L1 for maximum indicated output level. Switch EXT LEVELLING off.

Checking output filter

24. The 20 MHz low-pass filter and high-pass termination are factory set and should normally not require further adjustment. Following component replacement however, it may be necessary to make adjustments (note that power is not required for setting up the filter). Proceed as follows:-

(1) Remove link between AA1, TP5 and TP6.

(2) Set analyser controls :

REFERENCE FREQUENCY	:	CENTRE 33.4 MHz
HORIZONTAL SCALE	:	2 MHz/div.
VERTICAL SCALE RANGE	:	10 dB/div.
VERTICAL SCALE	:	-5 dBm
FILTER BANDWIDTH	:	NORMAL
SWEEP MODE	:	AUTO
DISPLAY	:	A & B

(3) Connect analyser TRACKING GENERATOR socket to AA1, TP6 (earth to TP4). Connect AA1, 6 via probe to analyser INPUT socket.

(4) Check for notch at 33.4 MHz. If not, adjust L4.

(5) Transfer probe to AA1, TP3.

(6) Reset analyser controls :

REFERENCE FREQUENCY	:	CENTRE 40 MHz
HORIZONTAL SCALE	:	0.5 MHz/div.
VERTICAL SCALE RANGE	:	1 dB/div.
VERTICAL SCALE	:	-10 dBm
SWEEP MODE	:	SINGLE
STORE	:	REFRESH A
DISPLAY	:	A

(7) Press analyser START button and read one sweep into STORE A as reference.

(8) Reset REFERENCE FREQUENCY to CENTRE 24 MHz. Select REFRESH B and DISPLAY B. Press analyser START button and check that level at 24 MHz is 6 dB ±0.5 dB below level at 40 MHz. If not, adjust L2.

(9) Remove probe and reconnect analyser INPUT socket to AA1, 6.

(10) Select REFRESH A and DISPLAY A. Set REFERENCE FREQUENCY to CENTRE 10 MHz. Press analyser START button and check that level at 24 MHz is 6 dB ±0.5 dB below that at 10 MHz. If not, adjust L3. Disconnect analyser and reconnect link.

Checking pass band response

25. The pass band response may be checked as follows:-

(1) Set analyser controls :

REFERENCE FREQUENCY	:	CENTRE 30 MHz
HORIZONTAL SCALE	:	2 MHz/div.
VERTICAL SCALE RANGE	:	1 dB/div.
VERTICAL SCALE	:	-15 dBm
FILTER BANDWIDTH	:	NORMAL
SWEEP MODE	:	AUTO
DISPLAY	:	HIGH DEFN

(2) Connect analyser INPUT socket via probe to AA1, 17. Select EXT LEVELLING ON and adjust FINE LEVEL control until analyser shows -22 dBm.

(3) Transfer probe to AA1, 6. Enter frequencies listed below in turn on sender keyboard, each time adjusting analyser reference frequency to conform. Check that levels agree with those shown:-

Frequency	*Output level*
6 kHz	-28 dBm ±1 dB
100 kHz	-28 dBm ±1 dB
1 MHz	-28 dBm ±1 dB
5 MHz	-28 dBm ±1 dB
10 MHz	-28 dBm ±1 dB
15 MHz	-28 dBm ±1 dB
19.99999 MHz	-28 dBm ±1 dB

Disconnect analyser and probe.

AA2 - Low-pass filter and amplifier board

Test equipment : items a, b and e.

Checking amplifier

26. The power amplifier gain and response may be checked as follows:-

(1) Set analyser controls :

REFERENCE FREQUENCY	:	CENTRE 10 MHz
HORIZONTAL SCALE	:	2 MHz/div.
VERTICAL SCALE RANGE	:	1 dB/div.
VERTICAL SCALE	:	-25 dBm
FILTER BANDWIDTH	:	NARROW
SWEEP MODE	:	SINGLE
STORE	:	A
DISPLAY	:	A & B

(2) Remove board AA1. Disconnect link between AA2, TP1 and TP2. Connect analyser TRACKING GENERATOR socket to AA2, 6 via attenuator set to 18 dB attenuation.

(3) Connect analyser INPUT socket via probe to AA2, 6. Press analyser START button and read one sweep into STORE A as reference.

(4) Transfer probe to TP1 (earth to TP3). Select REFRESH B. Press START button and check output level at 10 MHz is 21.6 dB ±0.5 dB above reference (adjusting VERTICAL SCALE as necessary).

(5) Check frequency response is within ±0.3 dB from 200 Hz to 20 MHz. Disconnect probe and reconnect link.

Checking l.p. filter

27. To check the 20 MHz low-pass filter continue as follows:-

(1) Transfer probe to AA2, 32. Check that frequency response is within ±0.5 dB from 200 Hz to 20 MHz.

(2) Reset analyser controls :

REFERENCE FREQUENCY	:	CENTRE 31.1 MHz
HORIZONTAL SCALE	:	1 MHz/div.
VERTICAL SCALE RANGE	:	10 dB/div.
VERTICAL SCALE	:	0 dB
SWEEP MODE	:	AUTO

(3) Check for rejection frequency at 31.1 MHz. If not, adjust L1.

(4) Reset analyser controls :

REFERENCE FREQUENCY	:	CENTRE 46.1 MHz
VERTICAL SCALE	:	-10 dBm

(5) Check for rejection frequency at 46.1 MHz. If not, adjust L2.

(6) Check that total stop band rejection is greater than -38 dB. Disconnect probe and analyser. Replace AA1.

AA3 - Power amplifier and a.l.c. detector board

Test equipment : items c, f, j and m.

Checking amplifier gain

28. Check amplifier TR1 to TR4 gain as follows:-

(1) Select EXT LEVELLING off, KEYBOARD + FINE and enter 10 MHz on keyboard.

(2) Connect oscilloscope to AA3, 32. Adjust FINE LEVEL control until AA3, 32 is at 300 mV pk-pk.

(3) Transfer to AA3, 6 and check that level is 2.4 V pk-pk ±150 mV. If not, r.f. gain setting must be adjusted. Disconnect oscilloscope.

Setting r.f. gain

29. R42 on AA3 compensates for gain variations on AA2 and AA3. To set the gain continue as follows:-

(1) Adjust FINE LEVEL control to display 0 dB on sender meter.

(2) Switch EXT LEVELLING ON and adjust R42 for 0 dB on meter.

Checking amplifier frequency response

30. To check amplifier frequency response continue as follows:-

(1) Switch EXT LEVELLING ON and enter 1 MHz, -70 dBm on keyboard.

(2) Connect oscilloscope to AA3, 6. Adjust oscilloscope to display positive peaks of waveform (using maximum gain) at a convenient reference level.

(3) Zero instrument meter using FINE LEVEL control.

(4) Enter 19 MHz on keyboard. Adjust FINE LEVEL control to bring displayed level to previously selected reference. Note meter reading (this indicates attenuator response and should be within -0.5 dB and -1 dB).

(5) Transfer oscilloscope to AA3, 37. Enter 1 MHz on keyboard and adjust FINE LEVEL control to zero meter.

(6) Reset displayed level to previously selected reference adjusting oscilloscope controls as necessary.

(7) Enter 19 MHz on keyboard. Adjust FINE LEVEL control to return oscilloscope display to previously selected reference.

(8) Check that instrument meter reading is within ±0.25 dB of reading in (4) above. If not, adjust L3.

Checking level comparators

31. The operation of level comparators IC2 and IC3 may be checked as follows:-

(1) Select KEYBOARD, EXT LEVELLING off and 75 Ω output impedance. Enter 10 MHz, 0 dBm on keyboard.

(2) Connect oscilloscope with 75 Ω termination to OUTPUT socket. Adjust oscilloscope to display positive peaks of waveform (using maximum gain) at a convenient, low, reference level.

(3) Select EXT LEVELLING ON and adjust FINE LEVEL control until displayed level is 57 mV (1.2 dB) above reference.

(4) Transfer oscilloscope to AA3, TP1 and check for >+5 V and that EXT LEVELLING HIGH lamp is lit. If not, adjust R30 until comparator just trips.

(5) Connect 1 MΩ ¼ W resistor from AA4, 32 to +7.5 V rail to provide external levelling input.

(6) Switch EXT LEVELLING off. Reconnect oscilloscope to OUTPUT socket and adjust oscilloscope to display positive peaks of waveform (using maximum gain) at a convenient, high, reference level.

(7) Switch EXT LEVELLING ON and adjust FINE LEVEL control until display is 194 mV (6 dB) below reference.

(8) Transfer oscilloscope to AA3, TP2 and check for >+5 V and that EXT LEVELLING LOW lamp is lit. If not, adjust R31 until comparator just trips.

(9) Recheck (4) above and, if readjustment is necessary, repeat (4) to (8). Disconnect oscilloscope.

Checking a.l.c. control voltage and muting

32. The operation of IC1 is checked as follows:-

(1) Select KEYBOARD and EXT LEVELLING off.

(2) Connect d.v.m. to AA3, 28 and check for approx. -1.05 V. Transfer to AA3, 29 and check for approx. 0 V.

(3) Remove AA11. Check AA3, 29 for -5.7 V approx.

(4) Select OUTPUT OFF and check AA3, 21 for +7.5 V. Transfer to AA3, 29 and check for approx. +5.8 V. Disconnect d.v.m. and replace AA11.

Checking levelled frequency response

33. Check the frequency response as follows:-

(1) Select 75 Ω output impedance and enter 100 kHz, 0 dBm on keyboard.

(2) Connect milliwatt test set to OUTPUT socket. Select ±0.2 dB range.

(3) Check that test set shows 0 dBm. If not, adjust AA12, R35.

(4) Check that AA4, TP5 is within ±1 V.

(5) Enter 19 MHz on keyboard. Check test set for 0 dBm. If not, adjust AA3, C28.

(6) Check that AA4, TP5 is within ±4 V.

(7) Spin manual TUNING control and check that frequency response is within specification (see Chap. 1) over frequency range. Disconnect milliwatt test set and voltmeter.

Resetting level error gain

34. Following component replacement it may be necessary to change the value of s.i.c. resistor R46. Proceed as follows:-

(1) Select KEYBOARD + FINE and 75 Ω output impedance. Enter 0 dBm on keyboard. Connect milliwatt test set in ±0.2 dB range to OUTPUT socket.

(2) Adjust FINE LEVEL control for 0 dBm on milliwatt test set. Connect d.v.m. to AA12, TP3 and note voltage as reference.

(3) Adjust FINE LEVEL control until voltage on AA12, TP3 increases by 1 dB (±0.01 dB).

(4) Check for +1 dB ±0.02 dB on milliwatt test set. If not, replace R46 with resistor of lower value for a positive error, or with resistor of higher value for a negative error, and repeat (2) to (4). Disconnect milliwatt test set and d.v.m.

AA4 - ALC controller board

Test equipment : items c and g.

ALC mode selection

35. ALC mode selection by IC5, IC6 and IC7 is checked as follows:-

(1) Select internal local mode by switching EXT LEVELLING off. Select KEYBOARD and enter a frequency above 6 kHz.

(2) Refer to Table 6 and check that logic levels on IC5 output pins conform to those shown for internal local, KEYBOARD above 6 kHz.

(3) Select remaining operating modes shown in Table 6 and check that logic levels on IC5 are correct.

TABLE 6 ALC MODE SELECTION LOGIC - AA4

Operating mode	*IC5 pins*					
	1	*15*	*2*	*10*	*9*	*11*
INTERNAL LOCAL, KEYBOARD above 6 kHz	L	H	L	L	H	H
INTERNAL LOCAL, KEYBOARD below 6 kHz	L	H	H	L	H	H
INTERNAL LOCAL, KEYBOARD + FINE above 6 kHz	L	H	L	L	H	L
INTERNAL LOCAL, KEYBOARD + FINE below 6 kHz	L	H	H	L	H	L
EXTERNAL LOCAL	H	L	L	H	L	L
INTERNAL REMOTE, above 6 kHz	L	H	L	L	H	H
INTERNAL REMOTE, below 6 kHz	L	H	H	L	H	H
EXTERNAL REMOTE	H	L	L	L	H	H

H = +7.5 V; L = -7.5 V

(4) Select EXT LEVELLING ON. Refer to Table 7 and check that switch IC6a is closed by measuring a resistance (typically 100 Ω) across IC6, pins 1 and 2. Switch EXT LEVELLING off and check that pins 1 and 2 are open circuit.

(5) Check operation of remainder of switches by means of Table 7.

TABLE 7 BILATERAL SWITCH OPERATION (KEYBOARD selected) - AA4

Switch IC	*Switch position when function selected*	
	Closed	*Open*
6a	EXT LEVELLING ON	EXT LEVELLING off
6b	EXT LEVELLING ON	EXT LEVELLING off
6c	EXT LEVELLING off	EXT LEVELLING ON
6d	EXT LEVELLING off	EXT LEVELLING ON
7a	EXT LEVELLING ON	EXT LEVELLING off
7b	EXT LEVELLING ON	EXT LEVELLING off
7c	EXT LEVELLING off	EXT LEVELLING ON
7d	Below 6 kHz	Above 6 kHz

Checking amplifier operation

36. Check the operation of the board amplifiers as follows:-

(1) Switch EXT LEVELLING off and select KEYBOARD + FINE. Connect voltmeter to AA4, TP1 and check for ±7.5 V as FINE LEVEL control is varied between limits. Transfer to AA4, TP2 and check for ±4.2 V as FINE LEVEL control is varied. This checks operation of FINE LEVEL CONTROL amplifier IC1.

(2) Connect AA4, TP1 by jumper lead to TP6. Using FINE LEVEL control set +1 V on TP6. Check TP7 for +5 V. Repeat for -1 V on TP6, checking for -5 V on TP7. This checks operation of EXT LEVELLING amplifier IC4. Disconnect jumper lead.

(3) Switch EXT LEVELLING ON and check AA4, 37 for ±2.5 V as FINE LEVEL control is varied between limits. This checks operation of LEVEL CONTROL amplifier IC3.

(4) Switch EXT LEVELLING off. Adjust FINE LEVEL control to display +1.1 dB on sender meter (corresponding to -0.25 V on TP3) and check TP2 for +3.7 V. Readjust FINE LEVEL control to display -1.1 dB on meter (corresponding to 0.25 V on TP3) and check TP2 for -3.3 V.

Checking r.f. level control

37. To check the level control operation continue as follows:-

(1) Adjust FINE LEVEL control for 0 dB on sender meter. Switch EXT LEVELLING ON and check for -28 dBm 50 Ω on AA1, 6 (this is difficult with an oscilloscope and may require spectrum analyser and probe). If not, adjust R26.

AA5 - 32 dB programmable attenuator board

Test equipment : None

Checking attenuator operation and frequency response

38. The procedures for checking attenuator operation and frequency response and adjusting L1 and L2 are included in the checks for board AA6.

AA6 - Programmable attenuator board

Test equipment : items a, c, f, k and n.

Checking attenuator operation

39. Check the operation of the 16 dB and 20 dB attenuators on AA6 and the 32 dB attenuator on AA5 as follows:-

(1) To check bilateral switch IC1 operation select +10 dBm, 75 Ω followed by sequence:-

1 MHz & + 1 MHz 1 MHz ENTER • • ENTER

(2) Press SLM CONTROL START key. This will cause data to be continuously clocked into AA6.

(3) Using dual beam oscilloscope trigger from and display positive-going 6 ms clock pulses on AA6, 10. Connect second channel to IC1 pins 11, 4, 9 and 2 in turn. Check that IC1 outputs are all at 0 V when clock is low (-7.5 V) and -7.5 V when clock is high (+7.5 V).

(4) Refer to Table 8 first column and enter levels shown in turn (changing output impedance when necessary) followed by sequence in (1) above. Check each time that logic on IC1 output pins agrees with that in table during positive clock pulse period.

TABLE 8 BOARDS AA5 AND AA6 ATTENUATOR SELECTION

Output Impedance	*Keyboard entry*	*Attenuation*	*AA6 IC1 pins*				*Transistor emitter junctions*		
			11	*4*	*9*	*2*	*TR3,4*	*TR1,2*	*TR5,6*
75 Ω	+10 dBm	0 dB	L	L	L	L	L	L	L
75 Ω	-6 dBm	16 dB	H	L	L	L	H	L	L
75 Ω	-10 dBm	20 dB	L	H	L	L	L	H	L
75 Ω	-22 dBm	32 dB	L	L	H	L	L	L	H
150 Ω	-22 dBm	32 dB	L	L	L	H	L	L	L

H = +7.5 V; L = -7.5 V

(5) Transfer oscilloscope to emitter junctions of transistor switches TR1 to TR6 and check that logic levels agree with those in Table 8 as level is changed on keyboard.

(6) Reselect +10 dBm and 75 Ω output impedance. Connect oscilloscope to OUTPUT socket terminated with 75 Ω and display level at top of screen as reference.

(7) Enter in turn -6 dBm, -10 dBm and -22 dBm on keyboard and check that level falls 16 dB, 20 dB and 32 dB below reference respectively.

Checking muting and rtl

40. Check the operation of latch IC2 supplying muting and return to local signals as follows:-

(1) Select OUTPUT SEND and check AA6, 28 and 29 for -7.5 V. Change to OUTPUT OFF and check AA6, 28 and 29 for +7.5 V.

(2) Set rear panel AUTO MUTE ENABLE switch to 1 followed by sequence:-

1 MHz & + 1 MHz 1 MHz ENTER • • ENTER and press SLM CONTROL START key.

(3) Trigger from and display AA6, 29 MUTE pulses. Connect second channel to AA6, 28 and display ALC MUTE pulses. Check display is as shown in Fig. 6(a).

(4) Transfer oscilloscope to OUTPUT socket and check that shape of envelope conforms to that shown in Fig. 6 (b). Switch AUTO MUTE ENABLE to 0.

(5) With GPIB boards installed, place sender in remote condition using controller (or bus analyser) and check AA6, 24 for -7.5 V. Press C (clear) button and check AA6, 24 for +7.5 V.

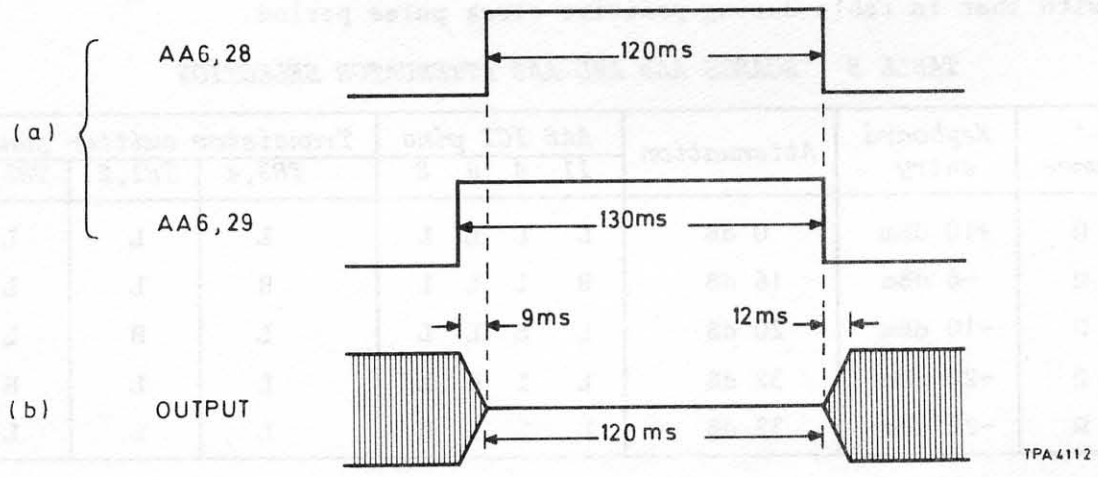


Fig. 6 Auto mute enable signals (approx. values given) - AA6

Checking output return loss

41. The output return loss is factory set and should normally not require further adjustment. Following component replacement likely to affect the return loss on boards AA5 to AA8 however, adjustment may be necessary. Proceed as follows:-

(1) Set analyser controls :

REFERENCE FREQUENCY	:	CENTRE 10 MHz
HORIZONTAL SCALE	:	2 MHz/div.
VERTICAL SCALE RANGE	:	10 dB/div.
VERTICAL SCALE	:	As required
FILTER BANDWIDTH	:	NORMAL
SWEEP MODE	:	AUTO
STORE	:	REFRESH A
DISPLAY	:	A & B

75 Ω return loss

(2) Connect TRACKING GENERATOR socket to 75 Ω return loss probe and connect probe detected output to analyser INPUT socket. Leave probe Z input disconnected.

(3) Position trace at top of analyser screen as reference using VERTICAL SCALE control.

(4) Select REFRESH B on analyser and connect probe input to sender OUTPUT socket. Remove AA11.

(5) Select 75 Ω output impedance and enter -22 dBm on keyboard to switch in 32 dB attenuator. Check for return loss of greater than 36 dB from 6 kHz to 20 MHz. If not, adjust L2 on AA5 and L1 on AA8 (see Table 9).

TABLE 9 OUTPUT RETURN LOSS

Output level	*Attenuator pads* 1 2 4 8 16 20 32	*Min. return loss* 6 kHz - 20 MHz	*Adjustment*
-22 dBm	X	36 dB	AA5,L2. AA8,L1
-10 dBm	X	36 dB	AA5,L1
-6 dBm	X	36 dB	AA6,L2
-5 dBm	X X X X	36 dB	AA6,L1

(6) Enter remaining output levels shown in first column of Table 9 and check that return losses agree with those given in table. If not, adjust as shown in last column of table.

(7) With -5 dBm entered on keyboard increase level in dB increments up to +10 dBm and check for return loss of at least 36 dB from 6 kHz to 20 MHz.

60 Ω return loss

(8) Replace 75 Ω probe with 60 Ω return loss probe and select 60 Ω output impedance. Connect analyser TRACKING GENERATOR socket to probe input and connect probe detected output to analyser INPUT socket. Leave probe Z input disconnected.

(9) Position trace at top of screen as reference using VERTICAL SCALE control.

(10) Select REFRESH A on analyser and connect probe input to sender OUTPUT socket. Enter 0 dBm on keyboard and check that return loss is at least 32 dB from 6 kHz to 20 MHz (60 Ω return loss does not change signficantly with attenuator setting so that it is only necessary to check at one level).

50 Ω return loss

(11) Repeat (8) to (10) using 50 Ω return loss probe and selecting 50 Ω output impedance. Disconnect analyser and probe and replace AA11.

AA7 - Programmable attenuator board

Test equipment : item c.

Checking attenuator operation

42. Check the operation of the 1 dB, 2 dB, 4 dB and 8 dB attenuators as follows:-

(1) To check bilateral switch IC1 operation select +10 dBm, 75 Ω followed by sequence:-

1 MHz & + 1 MHz 1 MHz ENTER • • ENTER

(2) Press SLM CONTROL START key. This will cause data to be continuously clocked into AA7.

(3) Using dual beam oscilloscope trigger from and display positive-going 6 ms clock pulses on AA7, 10. Connect second channel to IC1 pins 3, 8, 10 and 2 in turn. Check that IC1 outputs are all at -7.5 V during +7.5 V clock pulse, and that they rise to 0 V during -7.5 V clock period.

(4) Refer to Table 10 first column and enter levels shown in turn followed by sequence in (1) above. Check each time that logic on IC1 output pins agrees with that in table during positive clock pulse period.

(5) Transfer oscilloscope to emitter junctions of transistor switches TR1 to TR8 and check that logic levels agree with those in Table 10 as level is changed on keyboard.

TABLE 10 BOARD AA7 ATTENUATOR SELECTION

Keyboard entry	*Attenuation*	*IC1 pins*				*Transistor emitter junctions*			
		3	*8*	*10*	*2*	*TR1,2*	*TR3,4*	*TR5,6*	*TR7,8*
+10 dBm	0 dB	L	L	L	L	L	L	L	L
+9 dBm	1 dB	H	L	L	L	H	L	L	L
+8 dBm	2 dB	L	H	L	L	L	H	L	L
+6 dBm	4 dB	L	L	H	L	L	L	H	L
+2 dBm	8 dB	L	L	L	H	L	L	L	H

H = +7.5 V; L = -7.5 V

(6) Reselect +10 dBm and 75 Ω output impedance. Connect oscilloscope to OUTPUT socket terminated with 75 Ω and display a level at top of screen as reference.

(7) Enter in turn +9 dBm, +8 dBm, +6 dBm and +2 dBm on keyboard and check that level falls 1 dB, 2 dB, 4 dB and 8 dB below reference respectively. Disconnect oscilloscope.

AA8 - Unbalanced matching board

Test equipment : items c or j.

Checking switch operation

43. Check the unbalanced matching operation as follows:-

(1) Enter 6 kHz, 0 dBm on keyboard. Select 150 Ω unbalanced output impedance and check that IC1 pins 10, 11, 2 and 1 are all low (see Table 11). Check transistor switches TR1 to TR4 are all off and that diodes D2, D3, D7 and D8 are not conducting. Check for no signal at OUTPUT socket to check relay operation.

(2) Select remaining output impedances shown in first column of Table 11 and check that transistor, diode and relay operations agree with those given in table. Use d.v.m. or oscilloscope to check that voltages on OUTPUT socket agree with table when correctly terminated (use 75 Ω termination for 0 Ω).

TABLE 11 UNBALANCED MATCHING - AA8

Output impedance	*Supply voltage*		*IC1 pins*				*Transistors conducting*				*Diodes conducting*				*Output level r.m.s. (0 dBm)*
	H	*L*	*10*	*11*	*2*	*1*	*TR1*	*TR2*	*TR3*	*TR4*	*D2*	*D3*	*D7*	*D8*	
Balanced 150 Ω	+7.5	-7.5	L	L	L	L									-
Unbalanced 0 Ω	+6.0	-6.1	L	L	L	H				X					775 mV
Unbalanced 50 Ω	+4.8	-4.9	L	H	L	L		X				X		X	224 mV
Unbalanced 60 Ω	+4.7	-4.8	H	L	L	L	X				X		X		245 mV
Unbalanced 75 Ω	+6.1	-6.1	L	L	H	L			X						274 mV

AA9 - Balanced matching buffer board

Test equipment : items c, j, 1 and m.

Level switching

44. Check the level switching operation of IC1 and TR1 to TR4 as follows:-

(1) Select in turn 0 Ω, 124 Ω, 135 Ω and 150 Ω balanced output impedances and using oscilloscope, check IC1 pins 1, 2, 10 and 11 respectively for +7.5 V. At each selection check remaining output pins of IC1 for -7.5 V. Disconnect oscilloscope.

(2) Connect 150 Ω load across BALANCED OUTPUT socket. Select KEYBOARD and 150 Ω output impedance. Enter 6 kHz, 0 dBm on keyboard.

(3) Connect d.v.m. to AA9, 21 and check for approx. 0.79 V r.m.s. Note exact reading as reference.

(4) Change to 135 Ω output impedance. Check that level on AA9, 21 is 0.46 dB below reference.

(5) Change to 124 Ω output impedance. Check that level on AA9, 21 is 0.83 dB below reference.

(6) Change to 0 Ω balanced output impedance and check AA9, 21 for 0.775 ±0.015 V r.m.s. (0 dB).

(7) Change to 0 Ω unbalanced output impedance and terminate OUTPUT socket with 75 Ω load. Check AA9, 21 for 0.775 ±0.015 V r.m.s. (0 dB). Disconnect d.v.m.

Balanced output accuracy

45. Check the balanced output level accuracy as follows:-

(1) Select 150 Ω output impedance and enter 100 kHz, 0 dBm on keyboard. Connect milliwatt test set via 150 Ω balanced probe to BALANCED OUTPUT socket.

(2) Select ±0.2 dB range on milliwatt test set and check for 0 dBm ±0.15 dB. If not, adjust R16.

(3) Tune from 6 kHz to 1.6 MHz using TUNING control and check that output level varies by less than ±0.07 dB from 6 kHz to 620 kHz, and ±0.1 dB from 620 kHz to 1.6 MHz.

(4) If 124 Ω and 135 Ω balanced probes are available, repeat (1) to (3) above but do not readjust R16. Alternatively, use 150 Ω balanced probe and substitute 0 dBm in (2) above with -0.01 dBm for 124 Ω and with -0.04 dBm for 135 Ω.

(5) With 150 Ω balanced probe connected to BALANCED OUTPUT socket, select 0 Ω balanced output impedance and enter 100 kHz, -6 dB on keyboard. Check for +0.02 dBm ±0.15 dB. Repeat (3) above.

0 Ω unbalanced output accuracy

46. Check the 0 Ω unbalanced output level accuracy as follows:-

(1) Select 0 Ω unbalanced output impedance and enter 100 kHz, -9 dBm on keyboard. Connect 75 Ω milliwatt test set to OUTPUT socket and check for +0.03 dBm.

(2) Using TUNING control check that response is within ±0.5 dB over range 200 Hz to 20 MHz.

AA10 - Balanced matching board

Test equipment : items c and j.

Checking switch operation

47. Check the balanced matching operation as follows:-

(1) Enter 6 kHz, 0 dBm on keyboard. Select 0 Ω balanced output impedance and check that IC1 pins 1, 10 and 2 are all low (see Table 12). Check transistor switches TR1, TR3 and TR4 are all off. Check resistance across R12 and R17 is 0 Ω with BALANCED OUTPUT socket unterminated.

(2) Terminate BALANCED OUTPUT socket with 150 Ω and check socket for 775 mV to check relay operation.

(3) Select remaining output impedances shown in first column of Table 12 and repeat (1) and (2) above using correct terminations and check that transistor and relay operations agree with those given in table. Disconnect multimeter.

Checking 32 dB attenuator relay

48. Check the operation of electronic switches TR2 and TR5 and relay RLA as follows:-

(1) To check transistor switch operation select +10 dBm, 150 Ω followed by sequence:-

1 MHz & + 1 MHz 1 MHz ENTER • • ENTER

(2) Press SLM CONTROL START key. This will cause continuous switching pulses to be applied to AA10, 21.

(3) Connect oscilloscope to emitter junctions of TR2 and TR5 and check for 0 V pulsing to -6 V as TR5 switches on. Enter -22 dBm on keyboard and check for +6 V as TR2 switches on.

(4) Transfer oscilloscope to BALANCED OUTPUT socket terminated with 150 Ω load. Reselect +10 dBm on keyboard and display a reference level at top of screen.

(5) Enter -22 dBm on keyboard and check level on BALANCED OUTPUT socket falls 32 dB below reference as RLA operates. Disconnect oscilloscope.

TABLE 12 BALANCED MATCHING - AA10

Output impedance	*Supply voltage*		*IC1 pins*			*Transistors conducting*			*Relays energized*						*Resistance across*	*Output level r.m.s.*
	H	*L*	*1*	*10*	*2*	*TR1*	*TR3*	*TR4*	*B*	*C*	*D*	*E*	*F*	*G*	*R12 & R17*	*(0 dBm)*
Balanced 0 Ω	+7.0	-7.0	L	L	L										0 Ω	775 mV
Balanced 124 Ω	+7.0	-7.0	L	L	H			X		X			X		60.5 Ω	352 mV
Balanced 135 Ω	+7.0	-7.0	L	H	L		X		X					X	66 Ω	367 mV
Balanced 150 Ω	+7.5	-7.5	H	L	L	X					X	X			74 Ω	387 mV

AA11 - Frequency multiplier board

Test equipment : item c.

Checking output level

49. Check the board output level as follows:-

(1) Switch EXT LEVELLING ON and set FINE LEVEL control to centre of range. Observe sender meter and adjust L1 and L2 for a maximum indicated output level.

(2) Switch EXT LEVELLING off and select KEYBOARD + FINE. Adjust FINE LEVEL control to display 0 dB on meter.

(3) Switch EXT LEVELLING ON and check AA11, 7 for 30 MHz, -22 dBm 50 Ω (this may be done using an oscilloscope but requires care due to the high frequency involved and a spectrum analyser and probe is recommended). If not, reselect EXT LEVELLING off and carry out r.f. level control check detailed under board AA4.

Checking level control operation

50. The level control operation may be checked as follows:-

(1) Select EXT LEVELLING ON and enter 1 MHz, +10 dBm on keyboard. Adjust FINE LEVEL control for 0 V on AA4, TP5.

(2) Connect oscilloscope to OUTPUT socket and set a reference.

(3) Adjust FINE LEVEL control for -2 V on AA4, TP5 and check that level at OUTPUT socket drops >3 dB below reference.

(4) Readjust FINE LEVEL control for +2 V on AA4, TP5 and check that level at OUTPUT socket rises +2 dB above reference.

Checking muting operation

51. To check the muting operation continue as follows:-

(1) Select OUTPUT OFF and check AA11, 1 for +7.5 V. Transfer to AA11,2 and check for less than -6.5 V.

(2) Select OUTPUT SEND and 75 Ω output impedance. Connect oscilloscope to OUTPUT socket and set a reference level at top of screen. Switch to OUTPUT OFF and check that output level drops by at least 60 dB (this can be checked to 50 dB below reference to check operation using oscilloscope or measured to greater than 60 dB using spectrum analyser). Disconnect oscilloscope.

AA12 - Fine level control board

Test equipment : items c, j and m.

Checking level reference voltage

52. Check level reference as follows:-

(1) Select KEYBOARD. Check AA12, TP3 for approx. -1.05 V using d.v.m. Note value as reference.

(2) Change to KEYBOARD + FINE. Observe sender meter and adjust FINE LEVEL control to display +1 dBm. Check that AA12, TP3 is 1 dB above reference.

(3) Adjust FINE LEVEL control to display -1 dBm on meter. Check that AA12, TP3 is 1 dB below reference. Disconnect d.v.m.

Checking output level accuracy and fine level control

53. To check output level accuracy and fine level control accuracy continue as follows:-

(1) Check that meter is mechanically zeroed. If not, adjust zeroing screw under meter.

(2) Select KEYBOARD and 75 Ω output impedance. Enter 0 dBm, 100 kHz on keyboard.

(3) Connect milliwatt test set on ±0.2 dB range to OUTPUT socket and check for 0 dBm. If not, adjust R35.

(4) Select KEYBOARD + FINE and adjust FINE LEVEL control to display +1 dBm on sender meter. Adjust R24 for +1 dBm on milliwatt test set.

(5) Adjust FINE LEVEL control for -1 dBm on sender meter. Check that level shown on milliwatt test set is -1 dBm. If not, readjust R24 slightly to halve the deviation. Disconnect milliwatt test set.

Checking D/A conversion

54. To check the 0.1 dB and 0.01 dB step operation continue as follows:-

0.1 dB steps

(1) Select KEYBOARD and 75 Ω output impedance and enter 0 dBm on keyboard. Connect d.v.m. to AA12, TP3 and note voltage as reference.

(2) Select -0.1 dB on keyboard and using oscilloscope check IC1, pin 2 for +7.5 V and IC1, pins 10, 11 and 1 for -7.5 V. Check that level on AA12, TP3 drops 0.1 dB below reference.

(3) Select in turn -0.2 dB, -0.4 dB and -0.8 dB on keyboard and check IC1, pins 10, 11 and 1 respectively for +7.5 V. With each selection check remaining IC1 output pins for -7.5 V. Check each time that AA12, TP3 level drops by the entered decrement.

0.01 dB steps

(4) Switch to dB and enter e.g. -10.1 dB on keyboard (entering least significant digit of .1 ensures 0.1 dB step attenuators are not activated). Check IC2, pins 10, 11 and 1 for +7.5 V and pin 2 for -7.5 V. Check that level on AA12, TP3 drops 0.07 dB below reference (see Table 13).

TABLE 13 0.01 dB STEPS ATTENUATION - AA12

Output impedance	*Least significant digit*	*IC2 pin*				*Attenuation dB*
		2	*10*	*11*	*1*	
Unbalanced 75 Ω	.1	L	H	H	H	0.07
Unbalanced 60 Ω	.1	H	L	L	H	0.09
Unbalanced 50 Ω	.8	L	L	L	H	0.01
Unbalanced 0 Ω	.0	L	L	L	L	0
Balanced 124 Ω	.9	L	H	L	H	0.05
Balanced 135 Ω	.5	L	L	H	L	0.02
Balanced 150 Ω	.1	H	L	L	L	0.08
Balanced 0 Ω	.0	L	L	L	L	0

H = +7.5 V; L = -7.5 V

(5) Select remaining output impedances given in first column of Table 13 (changing l.s.d. of level enter on keyboard as required) and check logic levels and attenuation conform to those given in table. Disconnect oscilloscope and d.v.m.

AB1 - ±7.5 voltage regulator board

Test equipment : item j.

Preliminary

55. Following component replacement it may be necessary to readjust the regulation, limiting and short circuit protection operations. For these purposes it is necessary to simulate 'no load' and 'full load' conditions. Proceed as follows:-

Full load : Position board under test in AB1 socket in control unit assembly (max. supply 1.2 A).

No load : Remove all other removable boards with board under test in AB1 socket in control unit assembly. Alternatively, position board under test in AB1 socket in local oscillator unit assembly (max. supply 250 mA).

Adjusting regulation

56. The voltage regulation operation is adjusted as follows:-

(1) Set R14 and R5 fully anti-clockwise. Select no load and apply d.v.m. to AB1, 26 and check for +7.5 V ±0.02 V. If not, adjust R8. If at end of adjustment, reselect R9 in range 9.1 kΩ to 13 kΩ.

(2) Transfer d.v.m. to AB1, 30 and check for -7.5 V ±0.04 V. If not, adjust R8 then repeat (1) and (2) until voltages are within limits.

Adjusting current limiting

57. To adjust current limiting continue as follows:-

(1) Select full load and note if voltage on AB1, 30 has dropped. If so, turn R14 slowly clockwise until voltage reaches its former value and then stops rising. Stop turning R14 slightly after this point is reached.

(2) Check AB1, 26 and note whether voltage has fallen under full load. If so, turn R5 slowly clockwise until voltage reaches its former value and then stops rising. Stop turning R5 slightly after this point is reached.

Checking protection

58. Short circuit protection is checked as follows:-

(1) With full load selected, momentarily connect AB1, 26 to earth and check voltage on AB1, 30 immediately drops to between 0 V and -1 V.

(2) Transfer d.v.m. to AB1, 26 and momentarily connect AB1, 30 to earth. Check that positive rail voltage immediately drops to less than 2 V. Disconnect d.v.m.

AB2 and AB3 - Microprocessor and memory boards

Test equipment : item c.

Checking timing

59. Check the operation of clock generator IC1 as follows:-

(1) Connect oscilloscope to AB2, 29 and check for 7.5 V pulse train (Φ1) at approx. 740 kHz. Check AB2, 30 for similar non-overlapping pulse train at different phase (Φ2).

Checking microprocessor

60. Check the operation of microprocessor IC2 as follows:-

(1) Connect oscilloscope to RESET AB2, 28 and check for negative-going reset pulse when power first applied.

(2) Transfer oscilloscope to CARRY AB2, 33 and check for ±7.5 V 'random' data.

(3) Transfer to CM ROM AB2, 17 and 32 and check for 'random' data at, typically, +6.2 V and -3.6 V.

(4) Transfer to DATA AB2, B31 to B34 and check for ±7.5 V 'random' data.

(5) Transfer oscilloscope to SYNC AB2, 31 and check for train of 1.3 µs negative pulses at approx. 93 kHz.

(6) Connect oscilloscope to CM RAM 1 AB2, 34 and check for 65 µs group of 8 negative-going pulses with group interval 180 ms.

Checking ROM output ports

61. Check the operation of interface IC3 and ROM output ports as follows:-

(1) Connect oscilloscope to ROM 0 AB2, 11 to 14 and check for ±7.5 V data.

(2) Transfer to ROM 1 AB2, 1, 2, 7 and 8 and check for 'active'±7.5 V data when TUNING control is adjusted.

(3) Transfer to ROM 2 AB2, 3 to 6 and check for ±7.5 V data.

(4) Transfer to ROM 3 AB2, 9, 10, 15 and 16 and check for 'active' ±7.5 V data when data is sent remotely. For local operation check that AB2, 9 and 16 are at +7.5 V and AB2, 10 and 15 are at -7.5 V.

Checking RAM output ports

62. Check the operation of the RAM output ports as follows:-

(1) Connect oscilloscope to RAM 0 AB2, 19 to 22 and check for ±7.5 V 'random' data.

(2) Transfer to RAM 1 AB2, 24 to 27 and check for 'active' ±7.5 V data when TUNING control is adjusted.

AB4 - Control interface board

Test equipment : item c.

Checking address decoder

63. Check the operation of address decoder IC5 as follows:-

(1) Connect oscilloscope to AB4, 30 and check for a positive-going 22 µs pulse each time EXT LEVELLING switch it operated.

(2) Remove d.i.l. plug from AB8, SKA. Set AUTO MUTE ENABLE to '1', select OUTPUT SEND and 0 dB balanced output impedance.

(3) Enter -70 dBm on keyboard and key in sequence :-

1 MHz & + 1 MHz 1 MHz ENTER • • ENTER

and press SLM CONTROL START key.

(4) Transfer oscilloscope to AB4, 31, 32, 34, 35 and 36 in turn and check for 64 µs positive-going pulses.

(5) Transfer to AB4, 33 and 37 and check for approx. 7 ms positive-going pulses.

(6) Transfer to IC5 pins 3 and 14 and check for positive-going 22 µs pulses. Check IC4 pin 4 for inverse of IC5, 14.

(7) Press C to clear sequence and replace d.i.l. plug.

Checking control latch

64. To check the operation of control latch IC4 continue as follows:-

(1) Connect oscilloscope to INTERFACE SENSE MULTIPLEXER AB4, 26 and check for positive-going 126 µs pulses at approx. 50 Hz. Connect second channel to AB4, 24. If GPIB interface is fitted, check that AB4, 24 is low during period when AB4, 26 is high. If GPIB interface not fitted, check AB4, 24 remains low during this period.

(2) Transfer oscilloscope to MOTOR STOP AB4, 18 and check for low logic level. Press C key and check AB4, 18 goes high and then returns low when ENTER is pressed.

(3) Transfer to SYNC O/P AB4, 10 and check for +5 V. Press ENTER and check AB4, 10 returns to 0 V for approx. 140 ms (t.t.l.).

(4) Check IC4 pin 12 for +7.5 V.

(5) Check GPIB LISTEN AB4, 9 for -7.5 V (when in local mode).

Checking timer

65. To check the operation of timer IC1 continue as follows:-

(1) Connect oscilloscope to AB4, 14 and check for p.r.f. of 16 Hz. If not, adjust R2 for 16 Hz within ±0.1 Hz (turning R2 clockwise increases frequency).

Test input multiplexer

66. Checking the operation of multiplexer IC3 requires that the oscilloscope used be d.c. coupled in order to act as a pull-up resistor. Note also that the pulse widths may differ from those found in practice due to the resistance and capacitance of the probe in use. Continue as follows:-

(1) Connect oscilloscope to IC3 pin 12 and check for approx. 0 V. Temporarily short rear panel REMOTE COMMAND socket and check IC3 pin 12 for 11 ms pulses at approx. +7.5 V.

(2) Connect oscilloscope second channel to AB4, 24 and check that logic level corresponds to that on channel 1 during same time interval.

(3) Transfer oscilloscope to IC3 pin 15 and check for approx. -7.5 V. Temporarily connect a load of <10 kΩ to rear panel 30-50 MHz IN socket and check that display blanks. Check IC3 pin 15 for 0 V pulsing to +7.5 V for 0.35 ms. Repeat (2).

(4) Switch EXT LEVELLING ON and set FINE LEVEL control to mid-position. Connect oscilloscope to AB4, 29 and check for <-6 V pulsing to approx. +1 V for 0.25 ms. Repeat (2).

(5) Select OUTPUT OFF and check AB4, 29 for >+6 V and that EXT LEVELLING LOW lamp illuminates. Reselect OUTPUT ON.

(6) Transfer oscilloscope to AB4, 28 and check for <-6 V pulsing to approx. +1 V for 0.5 ms. Repeat (2).

(7) Turn FINE LEVEL control clockwise until EXT LEVELLING HIGH lamp illuminates. Check AB4, 28 for >+6 V. Reselect EXT LEVELLING off.

(8) With AUTO MUTE ENABLE set to '0' check AB4, 25 for 0 V. Set AUTO MUTE ENABLE to '1' and check for 14 ms, +7.5 V pulses. Repeat (2).

AB9 and AB10 - Keyboard and display boards

Test equipment : item c.

Checking function enable

67. Check the operation of AB9 function enable as follows:-

(1) Connect oscilloscope to monostable IC4, pin 11 and check for a train of 14 µs negative-going pulses.

(2) Enter -10 dBm, 10 MHz on keyboard. Connect oscilloscope to IC6 and IC7 output pins supplying addresses 1 to 11 and check for presence of positive-going address pulses of various pulse widths.

Checking manual tuning operation

68. Check decoder IC7 and manual tuning switches TR1, TR2 and TR3 as follows:-

(1) Connect oscilloscope to IC7 address 12 and check for 0.33 ms pulses when frequency is changed by slowly turning manual TUNING control.

(2) Spin TUNING control to produce electronic flywheel effect. Check for 630 µs pulses in range 100 Hz to 100 kHz, 1.3 ms pulses in range 100 kHz to 1 MHz, and 1.8 ms pulses in range 1 MHz to 20 MHz. Stop tuning.

(3) Transfer oscilloscope to IC7 address 14 and spin TUNING control. Check for positive-going reset pulses of 2.9 ms when increasing frequency and 3.1 ms when decreasing frequency.

(4) Trigger oscilloscope from and display IC7 address 10 pulses. Connect second oscilloscope channel to AB9, tag 6 and check for pulses while decreasing frequency using TUNING control. Check that pulses do not appear when frequency is increased.

(5) Transfer second channel to AB9, tag 3 and check for pulses when frequency is changed by TUNING control. Check that pulses do not appear when tuning is stopped.

(6) Trigger from and display IC7 address 9 pulses. Connect second channel to AB9, tag 5 and check for pulses while adjusting frequency by TUNING control. Stop tuning and check that pulses do not appear.

(7) Select OUTPUT OFF. Trigger oscilloscope from and display address 11 pulses to IC16 pin 13. Spin TUNING control and connect second channel to AB9, tags 3, 4, 6 and 5 in turn and check for data pulses.

(8) Trigger oscilloscope from and display address 12 pulses to IC14 pin 13. Spin TUNING control and connect second channel to AB9, tags 3, 4, 6 and 5 in turn and check for data pulses.

Checking keyboard and switches

69. The operation of the keyboard and other front panel switches is checked as follows:-

(1) Select 0 Ω balanced output impedance, KEYBOARD and SLM CONTROL OFF.

(2) Trigger oscilloscope from address 1 (anode side of AB9, D25) and display pulse on lower trace.

(3) Connect second channel to AB9, tag 3. Select in turn 0, 4, 8, +, KEYBOARD + FINE, SLM ON, 0 Ω unbalanced and 124 Ω output impedance and check at each selection that pulses appear in positions shown in Fig. 7 (note that pulse widths appear to vary irregularly; this is normal).

(4) Transfer oscilloscope input to AB9, tag 4. Select in turn functions shown in second column of Fig. 7 and check positions of pulses.

(5) Continue above procedure for remainder of functions shown in Fig. 7. Disconnect oscilloscope.

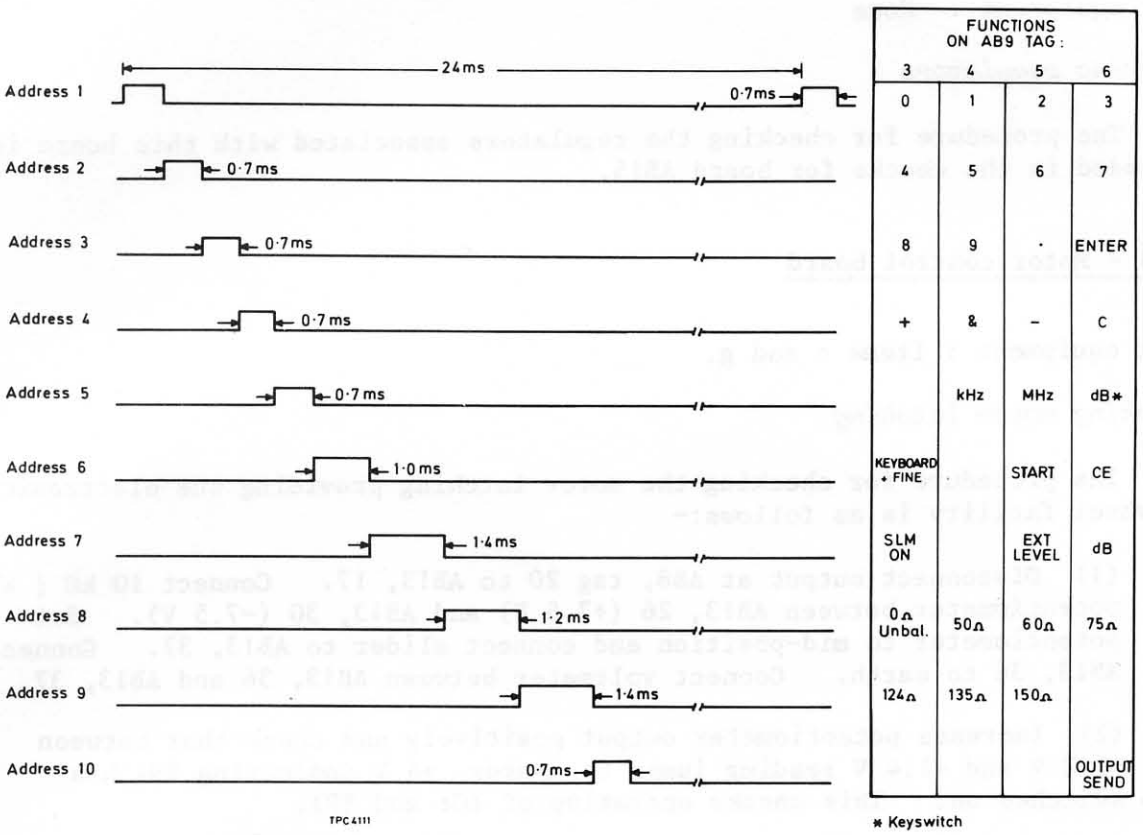


Fig. 7 Keyboard and switch operation summary - AB9

AB11 - Rectifier and charger board

Test equipment : Item g.

Checking rectifier operation

70. Check the rectifier as follows:-

(1) Set SUPPLY selector to ∿ and check alternating voltage is 22 V nominal across AB11, tags 3 and 1 and across AB11, tags 3 and 2.

(2) Check rectified voltage is 28 V nominal across AB11, tags 3 and 7 and -28 V nominal across tags 3 and 5.

Checking charger operation

71. To check the charge operation continue as follows:-

(1) *Trickle charge* : Connect 62 Ω 12 W resistor across rear panel BATTERY connector. Check that voltage across resistor is 2.7 V ±0.6 V.

(2) *Full charge* : Set SUPPLY selector to CHARGE and check that CHARGE lamp lights. Check that voltage across resistor is 27 V ±6 V. Disconnect resistor.

AB12 - Pre-regulator board

Test equipment : None

Checking regulators

72. The procedure for checking the regulators associated with this board is included in the checks for board AB15.

AB13 - Motor control board

Test equipment : Items c and g.

Checking motor latching

73. The procedure for checking the motor latching providing the electronic flywheel facility is as follows:-

(1) Disconnect output at AB8, tag 20 to AB13, 17. Connect 10 kΩ ¼ W potentiometer between AB13, 26 (+7.5 V) and AB13, 30 (-7.5 V). Set potentiometer to mid-position and connect slider to AB13, 37. Connect AB13, 36 to earth. Connect voltmeter between AB13, 36 and AB13, 37.

(2) Increase potentiometer output positively and check that between +1.2 V and +1.4 V reading jumps to approx. +4 V indicating TR1 has switched on. This checks operation of IC1 and TR1.

(3) Increase potentiometer output negatively and check that between -1.2 V and -1.4 V reading jumps to approx. -4 V indicating TR2 has switched on. This checks operation of IC2 and TR2.

(4) Connect jumper between motor stop AB13, 28 and positive rail and check that meter reading changes to 0 V. This checks operation of TR3 and RLA. Disconnect potentiometer and remove jumper to AB13, 28.

Checking ramp generation

74. Check the operation of ramp generator IC3 and TR4 as follows:-

(1) Connect jumper lead between AB13, 36 and AB13, 37 and check for 0 V at AB13, TP1. If not, adjust R29 for 0 V. Disconnect jumper.

(2) Reconnect potentiometer between AB13, 26 and AB13, 30. Set potentiometer to mid-position and connect slider to AB13, 37. Connect oscilloscope to AB13, TP1. Slowly increase potentiometer output positively and check for generation of negative ramps whose rate increases as input voltage is increased.

(3) Increase potentiometer output negatively and check for generation of positive ramps whose rate increases as input voltage is increased.

Checking window comparator

75. Check the operation of window comparator IC4 and IC5 and R-S bistable IC6ab as follows:-

(1) Connect oscilloscope to IC6 pin 6 and check for negative-going 50 µs triangular pulses. Check IC4 pin 6 for +5 V, and AB13, 9 for -7.5 V.

(2) Increase potentiometer output positively and check IC4 pin 6 for negative-going 50 µs triangular pulses. Check IC5 pin 6 for +5 V and AB13, 9 for +7.5 V.

Checking pulse generator

76. Check the operation of pulse generator IC6cde as follows:-

(1) Connect oscilloscope to AB13, 10 and check for positive-going pulse train of 25 µs pulses. Increase potentiometer output positively and check pulse rate decreases until no further pulses are generated.

(2) Continue increasing potentiometer output positively and check that positive-going pulse train reappears and pulse rate increases with increasing input voltage. Disconnect potentiometer and earth lead. Reconnect AB13, 37 to AB8 tag 20.

(3) Spin TUNING control in both directions and observe oscilloscope. Check for positive-going pulse train showing tuning motor is operating correctly. Disconnect oscilloscope.

AB15 - Rectifier and regulator board (includes AB12)

Test equipment : Item g.

Checking regulator operation

77. The following procedure is used to check the +5 V regulator operation both off load and on load (i.e. with GPIB boards fitted):-

(1) Set SUPPLY selector to ∿ check alternating voltage across AB15, tags 1 and 2 is 11 V (on load 10 V).

(2) Check rectified voltage on AB15 tag 6 is 14 V (12 V on load).

(3) Check IC1 regulated output on AB15, tag 13 is +5 V ±0.25 V.

78. The following procedure is used to check the operation of the ±5 V and the ±12 V regulators:-

(1) Check regulated voltage on AB15, tag 11 is +12 V ±0.6 V. This checks operation of heat sink mounted +12 V regulator IC1.

(2) Check regulated voltage on AB15, tag 10 is -12 V ±0.6 V. This checks operation of heat sink mounted -12 V regulator IC2.

(3) Check output on AB15, tag 14 is -11.2 V ±0.6 V. This checks operation of diode D5.

(4) Check regulated voltage on AB15, tag 15 is +5 V ±0.25 V.

(5) Check regulated voltage on AB15, tag 16 is -5 V ±0.25 V.

AD1 - Crystal oscillator board

Test equipment : items a, c, d and e.

Checking levels

79. Check board output levels as follows:-

(1) Set analyser controls :

REFERENCE FREQUENCY	:	CENTRE 10 MHz
HORIZONTAL SCALE	:	10 kHz/div.
VERTICAL SCALE RANGE	:	1 dB/div.
VERTICAL SCALE	:	-10 dBm
FILTER BANDWIDTH	:	WIDE
SWEEP MODE	:	AUTO
STORE/DISPLAY	:	HIGH DEFN

(2) Connect AD1, 21 to analyser INPUT socket via probe and check level is -10 dBm ±2 dBm. This checks operation of internal standard amplifiers.

(3) Transfer probe to AD1, 32 and check level is -4 dBm ±2 dBm. Disconnect analyser and probe.

(4) Connect oscilloscope to AD1, 1 and check for 200 kHz square wave of ±7.5 V. This checks operation of frequency dividers.

(5) Transfer to AD1, 6 and check for 2 MHz square wave of 60 mV to 100 mV p-p. Disconnect oscilloscope.

Checking frequencies

80. The following procedure is used to check output frequency accuracy as well as internal standard disable switch operation:-

(1) Connect counter to AD1, 32 and check for 10 MHz ±20 Hz. If not adjust C3 and C26.

(2) Connect $\frac{1}{4}$ W resistor of less than 10 kΩ between AD1, 36 and 37 and and check on counter that output is disabled. This checks operation of internal standard disable switches.

(3) Connect output from TF 2370 STD 10 MHz -10 dBm socket to TF 2356 10 MHz STD - EXT IN socket, still with resistor in (2) providing d.c. path. Connect sender OUTPUT socket to TF 2370 INPUT socket. Enter 10 MHz, -10 dBm on keyboard and check for this output. Remove resistor and interconnections.

(4) Connect counter to AD1, 6 and check for 2 MHz ±4 Hz. This checks operation of 2 MHz dividers IC1.

(5) Transfer counter to AD1, 1 and check for 200 kHz ±2 Hz. This checks operation of 200 kHz divider IC2. Disconnect counter.

AD2 - Interpolation phase detector board

Test equipment : Item c.

Checking divider operation

81. The operation of the 500 Hz divider is checked as follows:-

(1) Connect oscilloscope to AD2, 21 and check for 200 kHz square wave of approx. 14 V p-p.

(2) Transfer oscilloscope input to AD2, 32 and check for 100 kHz with 3 V p-p fast rising edge.

(3) Transfer input to IC3 pin 9 and check for 500 Hz square wave of 15 V p-p.

Checking phase detector operation

82. Check phase detector operation as follows:-

(1) Connect oscilloscope channel 1 to AD2, TP4 and check for 500 Hz ramp rising from -5 V to +3 V. This checks operation of 500 Hz dividers and ramp generator.

(2) Connect oscilloscope channel 2 to AD2, TP5 and trigger from TP4. Display 500 Hz train of approx. 120 µs pulses occurring during rise time of TP4 ramp. This checks generation of first sampling pulse.

(3) Use manual spin tuning in 5 Hz steps and check that pulse position w.r.t. ramp changes. This checks phase detector operation.

(4) Stop frequency incrementing and transfer oscilloscope channel 1 input to TP6. Check that displayed pulse on channel 1 is delayed approx. 180 µs w.r.t. pulse on channel 2. This checks generation of second sampling pulse.

(5) Connect oscilloscope to AD2, 37 and using manual spin tuning in 5 Hz steps check that d.c. level varies. This checks operation of sample and hold circuit. Disconnect oscilloscope.

AD3 - Interpolation variable divider board

Test equipment : Items a, c, d and e.

Checking low-pass filter

83. To check the 4 MHz l.p. filter proceed as follows:-

(1) Remove AD3 link between tags 4 and 6.

(2) Set analyser controls :

REFERENCE FREQUENCY	:	CENTRE 5 MHz
HORIZONTAL SCALE	:	1 MHz/div.
VERTICAL SCALE RANGE	:	10 dB/div.
VERTICAL SCALE	:	0 dBm
FILTER BANDWIDTH	:	NORMAL
SWEEP MODE	:	AUTO
STORE/DISPLAY	:	HIGH DEFN

(3) Connect analyser TRACKING GENERATOR socket to TP4 with earth to TP5. Connect TP7 via probe to analyser INPUT socket.

(4) Check for dip at 7.5 MHz. If not, adjust L2.

(5) Reset analyser HORIZONTAL SCALE to 2 MHz/div and check that rejection in the stop band between 8 MHz and 20 MHz is at least 50 dB below pass band. If not, adjust L1 (and L2 if necessary).

(6) Reset analyser HORIZONTAL SCALE to 0.5 MHz/div and VERTICAL SCALE RANGE to 1 dB/div. Check that ripple in pass band is no greater than 2.5 dB in pass band up to 3 MHz. If not, adjust L1 (and L2 if necessary).

(7) Replace link, disconnect analyser.

Checking mixer operation

84. Check the operation of mixer IC3 as follows:-

(1) Connect oscilloscope to AD3, TP1 and check for 10 MHz signal of at least 220 mV p-p. If not, adjust L3. Disconnect oscilloscope.

(2) Enter 1 MHz on keyboard. Connect counter to AD3, TP7 and check that frequency is 2 MHz.

(3) Decrement 5 Hz and check that AD3, TP7 frequency is 2.9995 MHz. Disconnect counter.

Checking amplifier operation

85. To check the operation of squaring amplifier IC5 continue as follows:-

(1) Connect oscilloscope to AD3, TP3 and check for square wave of 7.5 V p-p.

(2) Change frequency to 1 MHz and check AD3, TP3 that square wave amplitude is unchanged.

Checking divider operation

86. To check the variable ratio divider IC4 continue as follows:-

(1) Transfer oscilloscope input to AD3, 1 and check for 500 Hz train of 0.5 µs pulses.

(2) Change frequency to 1.009995 MHz and check that AD3, 1 pulse repetition frequency is unchanged.

Checking D/A operation

87. The procedure for checking the variable ratio divider operation is as follows:-

(1) Enter 1.00999 MHz on keyboard. Set R25 fully clockwise. Connect oscilloscope to AD3, 37 and check for approx. -1.5 V. If not, adjust R27.

(2) Enter 1 MHz on keyboard and check for approx. -5 V on AD3, 37. If not, adjust R26.

(3) Transfer oscilloscope to AD2, TP4. Trigger from and display 500 Hz ramp. Connect second oscilloscope channel to AD2, TP5. Check that pulses on AD2, TP5 are locked approximately to centre of ramp. If not, adjust R25 on AD3.

(4) Increment in 1 kHz steps and check that pulses do not become unlocked from ramp.

(5) Connect oscilloscope to AD3, 37. Select 5 kHz increments and, while spin tuning, adjust R26 and R27 to minimize ramp restart settling time. Disconnect oscilloscope.

AD4 - Interpolation oscillator board

Test equipment : Items a, c, d and h.

Checking oscillator operation

88. Check the v.c.o. output frequencies as follows:-

(1) Remove board AD3. Connect d.c. power source set to 0 V to AD4, 37. Connect counter to AD4, 21 and check for 13 MHz ±250 kHz. If not, adjust T1.

(2) Change power source to -4 V and check AD4, 21 for 12 MHz ±250 kHz. Disconnect counter.

89. To check the oscillator output levels continue as follows:-

(1) Connect analyser INPUT socket to AD4, 21 and set the controls as follows:-

REFERENCE FREQUENCY	:	CENTRE 13 MHz
HORIZONTAL SCALE	:	1 MHz/div.
VERTICAL SCALE RANGE	:	1 dB/div.
VERTICAL SCALE	:	0 dBm
FILTER BANDWIDTH	:	WIDE
SWEEP MODE	:	AUTO
STORE/DISPLAY	:	HIGH DEFN

(2) Reset d.c. input to 0 V and check that amplitude at 13 MHz is -10 dBm ±2 dBm. Check other responses, apart from harmonics at multiples of 13 MHz, are less than -60 dBm. Disconnect analyser.

Checking counter operation

90. To check counter IC1 and amplifier IC2 operation continue as follows:-

(1) Connect oscilloscope to AD4, TP2 and check for square wave of not less than 12 V p-p. Replace oscilloscope with counter and check frequency is 2.6 MHz ±0.005 MHz. Remove power source and replace board AD3.

Checking presettable divider operation

91. Check divider IC3 operation as follows:-

(1) Connect counter to AD4, 1 and check for 777 Hz. This checks operation of presettable divider. Disconnect counter.

AD5 - Translation pnase detector board

Test equipment : Items c and i.

Checking mixer operation

92. Check mixer IC1, l.p. filter IC2 and divider IC3 operation as follows:-

(1) Remove board AD6. Connect signal generator set to 2.001 MHz +12 dBm to AD5, 32.

(2) Connect oscilloscope to AD5, TP1 and check for stable 1 kHz square wave of at least 12 V p-p. Disconnect oscilloscope and replace AD6.

Checking phase detector operation

93. The in-phase operation is checked as follows:-

(1) Set instrument to 8 MHz and remove board AD4. On AD5 connect jumper lead between pins 3 and 11 of IC4.

(2) Disconnect link between AD5 and AD6 at contact 17 and connect AD5, 6 to earth. Check input frequency at IC4 pin 11 is approx. 650 Hz.

(3) Connect oscilloscope to IC4 pin 12 and check for -7.5 V with positive-going spikes at approx. 650 Hz. Transfer to IC4 pin 1 and check for +7.5 V with negative-going spikes.

(4) Transfer oscilloscope to IC5 pin 6 and check for high set signals.

(5) Check that TR2 and TR4 are both off.

(6) Check TR3 and TR5 operation by checking for 0 V at AD5, 17 (either transistor faulty will cause +7.5 V or -7.5 V at contact 17).

94. To check the out of phase operation continue as follows:-

(1) Remove jumper lead between pins 11 and 3 of IC4. Check that IC4 pins 1 and 12 are both high.

(2) Check that TR4 is on and TR2 is off and check AD5, 17 for 0 V.

(3) Remove AD6, insert AD4 and check that AD5, IC4 pins 1 and 12 are both low and AD5, 17 is at 0 V. Replace AD6 and replace link to contact 6.

Checking v.c.x.o. selection logic

95. Check the crystal selection operation as follows:-

(1) Connect oscilloscope to AD5, B12 and check for positive-going spikes as TUNING knob is turned. This checks operation of latch strobe.

(2) Enter 7.12 MHz on keyboard. Connect oscilloscope input to AD5, 6 and check for -7.5 V. Decrement 5 Hz and check for +7.5 V. This checks gating of B12, B13 and B14 inputs.

(3) Enter 8.12 MHz on keyboard and check for -7.5 V on AD5, 6. This checks gating of B15 and B16 inputs.

(4) Change keyboard entry to 10.12 MHz and check that AD5, 6 remains at -7.5 V. This checks gating of B11 input. Disconnect oscilloscope.

AD6 - Translation oscillator board

Test equipment : Items c, d and h.

Checking v.c.x.o. operation

96. The procedure for checking the operation of the crystal oscillator, crystal selection switches and dividers is as follows:-

(1) Remove board AD5. Apply power source to AD6, 6 and connect counter to IC1 pin 1.

(2) Apply -7.5 V to AD6, 9 by connecting it to negative rail to select low frequency crystal XL2. Set power source voltages to values given in Table 14, column 2 and check that output frequencies (levels 0.8 V to 2 V min.) are as given in Table 14, column 3.

(3) Connect AD6, 9 to positive rail to apply +7.5 V for high frequency crystal XL1 selection. Set power source as before to values given in Table 14, column 2 and check that output frequencies (levels 0.8 V to 2 V min.) are as given in Table 14, column 3.

(4) Transfer counter to AD6, 21 and check that for -6 V applied to AD6, 6 the output frequency is 2.006 MHz ±500 Hz i.e. one fifth input frequency (see Table 14).

(5) Transfer counter to AD6, 37 and check that output frequency is 10.03 kHz ±5 Hz i.e. one thousandth input frequency (see Table 14). Disconnect counter.

TABLE 14 VCXO OPERATION - AD6

1 *Voltage applied to contact 9*	2 *Voltage applied to contact 6*	3 *IC1 pin 1 (±7.5 kHz)*	4 *Output frequency at contact 21 (±500 Hz)*	5 *Output frequency at contact 37 (±5 Hz)*
	+6 V	10.0380MHz	2.0075MHz	10.0380kHz
-7.5 V	0 V	10.0320MHz	2.0064MHz	10.0320kHz
	-6 V	10.0215MHz	2.0043MHz	10.0215kHz
	+6 V	10.0480MHz	2.0096MHz	10.0480kHz
+7.5 V	0 V	10.0420MHz	2.0084MHz	10.0420kHz
	-6 V	10.0300MHz	2.0060MHz	10.0300kHz

Checking output levels

97. To check the counter output levels continue as follows:-

(1) Connect oscilloscope to AD6, 21. Check for stable square wave, '0' = +0.8 V max., '1' = +2 V min. Check that the voltage levels remain unchanged as power source (frequency control) voltage is varied between +6 V and -6 V.

(2) Reconnect AD6, 9 to negative rail and repeat (1).

(3) Transfer oscilloscope to AD6, 37 and check for stable square wave of at least 12 V p-p and remains so as power source (frequency control) voltage is varied between +6 V and -6 V.

(4) Reconnect AD6, 9 to positive rail and repeat (3). Remove jumper lead, disconnect oscilloscope and power source and replace AD5.

AD7 - Output variable divider board

Test equipment : Items c and d.

98. The following procedure is used to check board operation:-

(1) Remove twisted pair to board AD8 input and connect AD8 socket to earth to supply 0 V control voltage. Connect counter to AD7, 1 and check for 39.5 MHz ±1 MHz at -10 dBm.

(2) Enter 10.12 MHz on keyboard and using oscilloscope check that AD7, B4 to B17 are all low (-7.5 V) and AD7, B18 is high (+7.5 V).

(3) Check input amplifier TR1 and TR2 operation by checking for e.c.l. threshold voltages of -1.1 V and -1.5 V on pin 1 IC1.

(4) Check prescaler operation by checking for v.c.o. frequency ÷10 (approx. 4 MHz) on IC1 pin 11, and v.c.o. frequency ÷20 (approx. 2 MHz) on IC2 pin 9. Levels 0 V and -5 V.

(5) Check IC6 operation by checking for v.c.o. frequency ÷20 ±7.5 V on AD7, TP2 and TP3.

(6) Check divide by five operation by checking for v.c.o. frequency ÷100 (approx. 400 kHz) ±7.5 V on AD7, TP4.

(7) Check most significant counters operation by checking for v.c.o. frequency ÷4000 (approx. 10 kHz) ±7.5 V on AD7, TP5 and TP6.

(8) Check for 0.5 µs pulses at approx. 10 kHz on IC3 pin 4.

(9) Enter 10.31 MHz on keyboard and ensure all data inputs are low except for AD7, B4, B7, B8 and B18. Trigger oscilloscope from negative edge of pulse on AD7, TP1 and display pulse. On second trace display AD7, TP2 clock pulses. Check duration of negative pulse equates to 19 clock periods (approx. 10 µs).

(10) Check IC10a operation by connecting oscilloscope to AD7, TP1 and while triggering from and displaying waveform on IC3 pin 4, check that display approximates to that shown in Fig. 8.

(11) Ensure prescaler now dividing by 21 by counting 21 input pulses on IC1 pin 1 during one complete cycle of IC2 pin 9.

(12) Enter 10.14 MHz on keyboard and ensure all data input contacts are low except AD7, B5 and B18. Connect oscilloscope input to AD7, TP2 and trigger from and display negative pulse on AD7, TP1. Check that after AD7, TP1 goes low, widths of first two pulses (indicating ÷11) on AD7, TP2 are slightly greater than widths of remainder of pulses (indicating ÷10). Check that rising edge of second of these pulses terminates negative pulse (see Fig. 9). Disconnect oscilloscope and reconnect twisted pair.

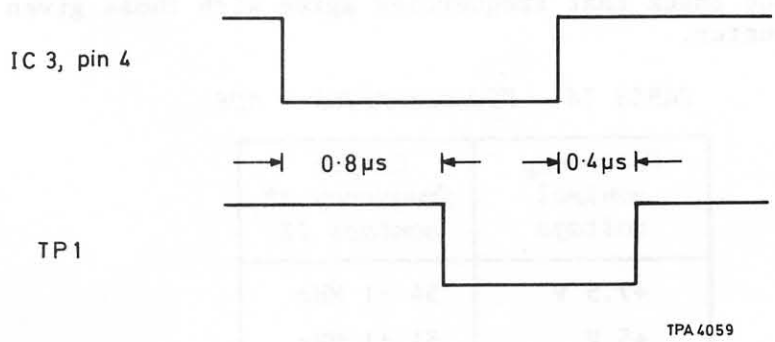


Fig. 8 Modulus selection - AD7

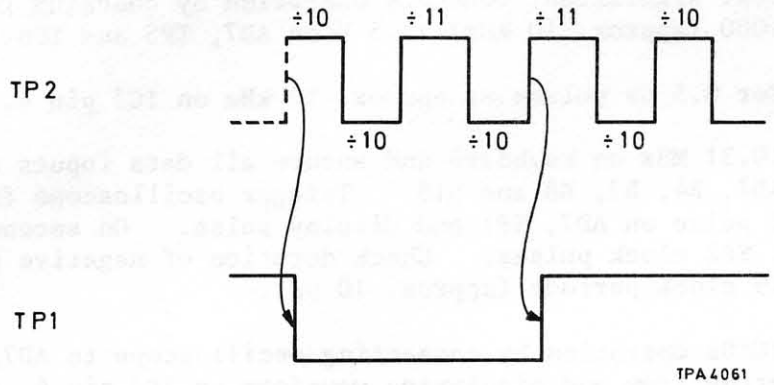


Fig. 9 Dual modulus operation - AD7
(pulse widths exaggerated for clarity)

AD8 - Output oscillator board

Test equipment : Items a, c, d, e and h.

Checking oscillator operation

99. Use the following procedure to check v.c.o. operation:-

(1) Remove twisted pair to board input and connect power source set to 0 V to AD8 input socket to supply control voltage. Check TR2 emitter for 0.5 V p-p signal at 39.5 MHz ±1 MHz. If not, adjust L1.

(2) Transfer counter to AD8, 12. Set power source to voltages given in Table 15 and check that frequencies agree with those given in Table. Disconnect counter.

TABLE 15 VCO OPERATION - AD8

Frequency control voltage	*Output frequency at contact 12*
+7.5 V	54 ±1 MHz
+5 V	51 ±1 MHz
-5 V	29 ±1 MHz
-7 V	23 ±2 MHz

Checking output levels

100. To check the output levels continue as follows:-

(1) Set analyser controls:-

REFERENCE FREQUENCY	:	CENTRE 50 MHz
HORIZONTAL SCALE	:	0.02 MHz/div.
VERTICAL SCALE RANGE	:	10 dB/div
VERTICAL SCALE	:	0 dB
FILTER BANDWIDTH	:	WIDE
SWEEP MODE	:	AUTO
DISPLAY	:	HIGH DEFN

(2) Remove connector from AD8, 1 and replace with lead to analyser INPUT socket. Set power source to +5 V and check that level at 50 MHz is -11 ±2 dBm. Replace connector.

(3) Ensure that 30-50 MHz OUT socket on rear panel is terminated with supplied 50 Ω load. Connect analyser INPUT to AD8, 7 via probe and check level is 11 ±2 dBm.

(4) Transfer probe to AD8, 12 and check for -11 ±2 dBm. Disconnect power source analyser and probe.

AD10 - Synthesizer latch board

Test equipment : Item c.

Checking in-phase operation

101. The in-phase operation is checked as follows:-

(1) Remove boards AD7 and AD8. Connect jumper lead between AD9, 1 and 7.

(2) Connect oscilloscope to IC1 pin 12 and check for -7.5 V with positive-going spikes at approx. 10 kHz. Transfer to IC1 pin 1 and check for +7.5 V with negative-going spikes.

(3) Transfer oscilloscope input to IC2 pin 3 and check for high set signals

(4) Transfer to AD9, 12 and check for -7.5 V in-lock signal.

(5) Check that electronic switches TR1 and IC3b are both off.

(6) Check current mirror operation by checking for 0 V at d.c. output plug.

Checking out-of-phase operation

102. To check the out-of-phase operation continue as follows:-

(1) Remove jumper lead between AD9, 1 and 7. Check IC1 pins 1 and 12 are both high.

(2) Check for high out of lock signal at AD9, 12.

(3) Check that IC3b is on and TR1 is off.

(4) Transfer to d.c. output and check for +7.5 V.

(5) Replace boards AD7 and AD8 and remove board AD6. Check IC1 pins 1 and 12 are both low.

(6) Check for high out of lock signal on AD9, 12.

(7) Check that TR1 is on and IC3b is off.

(8) Transfer to d.c. output and check for -7.5 V. Replace board AD6 and disconnect oscilloscope. Reconnect AD8 control voltage input.

AD9 - Output phase detector board

Test equipment : Item c.

Checking frequency divisor outputs

103. The overall selection of the N_1 and N_2 division ratios may be checked as follows:-

(1) Enter 1 MHz on keyboard and check all output contacts are low as shown in Table 16. Enter remaining frequencies given in Table each time checking logic levels conform to those given in Table.

(2) Refer to Table 17 and enter frequencies given, each time checking that associated logic levels are correct.

TABLE 16 N_1 DIVISION RATIO OUTPUTS - AD10

Frequency (MHz)	*Output contacts*												
	4	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*	*16*	*17*	*18*
1.000000	L	L	L	L	L	L	L	L	L	L	L	L	L
1.009995	H	H	L	L	H	H	L	L	H	H	L	L	H
1.006660	L	L	H	H	L	L	H	H	L	L	H	H	L

L = -7.5 V; H = +7.5 V

TABLE 17 N_2 DIVISION RATIO OUTPUTS - AD10

Frequency (MHz)	*Output contacts*														
	B4	*B5*	*B6*	*B7*	*B8*	*B9*	*B10*	*B11*	*B12*	*B13*	*B14*	*B15*	*B16*	*B17*	*B18*
0.006	L	L	L	H	L	L	L	H	H	L	L	H	L	H	L
6.89	H	H	H	L	H	H	H	L	L	H	H	L	H	H	L
9.99	H	H	H	L	L	L	L	H	H	L	L	H	H	H	L
10.12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
10.31	H	L	L	H	H	L	L	L	L	L	L	L	L	L	H
10.14	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H

L = -7.5 V; H = +7.5 V

Checking v.c.x.o. inhibit

104. Check inhibit signal to board AD5 as follows:-

(1) Connect oscilloscope to AD10, 6 and check for positive-going spikes as manual TUNING knob is turned.

Checking decoder operation

105. Check operation of decoder IC9 as follows:-

(1) Trigger oscilloscope from pin 14 IC9 and connect input in turn to pins 2, 15, 1, 6, 7, 4 and 9. Check each time that displayed pulse occurs 150 µs later than previously displayed pulse (note that triggering is difficult owing to time variations for each cycle).

Chapter 5, Annex A

GPIB INTERFACE FAULT FINDING GUIDE

CONTENTS

CONTENTS (continued)

INTRODUCTION

1. This Annex is intended to be used as an aid to fault finding on the GPIB interface when fitted in the TF 2356 or TF 2357. For this purpose the Annex should be read in conjunction with the technical description in Chap. 4-2 and the servicing diagrams in Chap. 7 of the Service Manual. Detailed information on GPIB interface operation will be found in IEEE Standard 488-1978 and IEC Publication 625-1.

2. The tests which follow, which are not exhaustive, are based upon the use of a bus analyser in order that the interface may be single-stepped through its operating modes. Tests commence with a main sequence during which the bus analyser and instrument displays are used to indicate the probable fault area. Fault finding checks are then used to diagnose faults down to component level or to comparatively small groups of components.

FAULT FINDING PROCEDURE

3. Commence fault finding using the main sequence and ensure that no equipment other than the bus analyser is connected to the instrument under test. When following the sequence take care in entering data since if an error is made it will often be necessary to backtrack to an earlier part of the sequence in order to repeat the check correctly. If in doubt, restart the sequence, this may be tedious but will prevent incorrect diagnosis.

4. A fault indicated by the analyser or instrument display normally leads to one or more fault finding checks. For these checks, apart from the limited use of a logic analyser, only an oscilloscope need be used. When a fault is diagnosed and a statement such as 'there is a fault with IC1' is made, it implies also that the fault may be with e.g. an associated pull-up resistor, rather than with the designated component.

5. In case of difficulty, return the interface boards to Marconi Instruments Service Division whose address will be found inside the rear cover of the Service Manual.

Addressing

6. To carry out an instruction to set the analyser DIO lines to MLA or MTA proceed as follows:-

(1) Set DIO lines 1 to 5 to conform to TF 2357 or TF 2356 rear panel ADDRESS switch settings.

(2) For MLA set DIO line 6 high and line 7 low.

(3) For MTA set DIO line 6 low and line 7 high.

Pressing the EXECUTE button will then operate the handshake to designate the instrument as a listener or a talker.

MAIN SEQUENCE

Preliminary

7. Set initial conditions as follows:-

(1) Connect instrument alone to bus analyser and switch analyser on.

(2) Set instrument ADDRESS switches on rear panel to 0001010 (TF 2357) or 0000010 (TF 2356).

(3) Set analyser to INT CLOCK on rear panel and set the following controls:-

REN	:	0
MEMORY	:	OFF
COMP	:	OFF
TALK/LISTEN	:	TALK
FAST/SLOW/HALT	:	HALT
SRQ	:	0
EOI	:	0

ATN	:	0
DIO	:	00101010 (TF 2357)
		00100010 (TF 2356)

Interface power-on

8. To check interface power-on continue as follows:-

(1) Switch instrument on and check display shows 1000.00 kHz. If not, go to 'Power-up fault'.

(2) Check REMOTE lamp is off. If not, go to 'Remote lamp fault'.

(3) Enter 1 kHz on instrument keyboard and check that it is displayed correctly. If not, go to 'Incorrect local operation'.

(4) On analyser check that the following lamps are off:-

NDAC - If not, go to 'Acceptor handshake control fault (a)'.
DAV - If not, go to 'Source handshake fault'.
NRFD - If not, go to 'Acceptor handshake control fault (a)'.
SRQ - If not, go to 'Service request fault'.
EOI - If not, there is a fault with AB7 transceiver IC4.
ATN - If not, go to 'ATN output fault'.
IFC - If not, there is a fault with AB7 transceiver IC3.
REN - If not, go to 'REN output fault'.

(5) Temporarily switch analyser to LISTEN and check that analyser data display shows 000 octal or 00 hex. Switch back to TALK.

Acceptor handshake, addressing and remote

9. Handshake, addressing and remote/local operation are checked as follows:-

Acceptor handshake

(1) On analyser check that NDAC lamp comes on and NRFD lamp remains off when REN and ATN are both set to 1. If not, go to 'Acceptor handshake control fault (a)'.

(2) Press and hold EXECUTE button. Check NRFD lamp comes on and NDAC lamp goes off (DAV lamp will be on). If not, go to 'Acceptor handshake control fault (b)'.

(3) Release EXECUTE button and check that NDAC lamp comes on and NRFD lamp goes off. If not, go to 'Acceptor handshake control fault (a)'.

Listen address

(4) Set ATN to 0 and check NDAC lamp remains on. If not, go to 'Data input and message decoder fault'.

(5) Check NDAC lamp goes off when IFC switch is pressed. If not, go to 'Unlisten fault'.

(6) Set analyser DIO switches to 00110101 (TF 2357) or 00100011 (TF 2356) for other listen address. Set ATN to 1 (NDAC lamp comes on) and press EXECUTE.

(7) Check NDAC lamp goes off when ATN is set to 0. If not, to to 'Data input and message decoder fault'.

(8) Set instrument ADDRESS switches to 0010101 (TF 2357) or 0000011 (TF 2356).

(9) Set ATN to 1 and press EXECUTE. Reset ATN to 0 and check NDAC lamp stays on. If not, go to 'Data input and message decoder fault'.

(10) Set analyser DIO lines to 00111111 (to assert UNL). Set ATN to 1 and press EXECUTE.

(11) Check NDAC lamp goes off when ATN set to 0. If not, go to 'Programmed unlisten fault'.

Local/remote

(12) Check instrument REMOTE lamp is on. If not, go to 'Remote/local fault'.

(13) Check REMOTE lamp goes off when REN is set to 0. If not, go to 'Remote fault'.

(14) Reset REN to 1 and set DIO lines to 00110101 (TF 2357) or 00100011 (TF 2356). Set ATN to 1 and press EXECUTE. Check REMOTE lamp comes on.

(15) Check REMOTE lamp goes off when C key on instrument is pressed (to assert rtl). If not, go to 'rtl fault'. Restore TF 2357 display by re-entering 1 kHz.

(16) Press EXECUTE (REMOTE lamp comes on).

(17) Set DIO lines to 00010001 (LLO) and press EXECUTE.

(18) Press C key on instrument and check REMOTE lamp remains on. If not, go to 'LLO fault'.

(19) Set DIO lines to 00000001 (GTL). Check REMOTE lamp goes off when EXECUTE is pressed. If not, go to 'GTL fault'.

(20) Set DIO lines to 00110101 (TF 2357) or 00100011 (TF 2356) and press EXECUTE (REMOTE lamp comes on).

Service request

10. To check the service request operation continue as follows:-

(1) Response to incorrect data: Check SRQ lamp is off. If not, go to 'NPRS fault'. Set ATN to 0 and press EXECUTE (to send incorrect data) and check SRQ lamp comes on (TF 2356 display will blank). If not, go to 'Service request fault'.

(2) Set ATN to 1 and set DIO lines to 01010101 (TF 2357) or 01000011 (TF 2356) and press EXECUTE to send MTA.

(3) Set DIO lines to 00011000 (SPE) and press EXECUTE (TF 2356 display shows dots).

(4) Set analyser to LISTEN (TF 2357 display blanks, TF 2356 no visible response). Check that SRQ lamp goes off. If not, go to 'SPE fault'.

(5) Check DAV lamp comes on. If not, go to 'SPAS fault'.

(6) Check analyser display shows 140 octal or 60 hex. If not, go to 'Data output latch fault'.

(7) Check DAV lamp goes off when EXECUTE is pressed and held. If not, go to 'Source handshake fault'.

(8) Release EXECUTE button and check analyser display shows 061 octal or 31 hex. If not, go to 'Data output latch fault'.

(9) Check DAV lamp goes off when analyser set to TALK. If not, AB6 IC7c is faulty.

(10) Set DIO lines to 01010100 (TF 2357) or 01000010 (TF 2356) and press EXECUTE to send OTA.

(11) Switch analyser to LISTEN and check DAV lamp remains off. If not, go to 'OTA fault'.

(12) Check analyser display shows 000 octal or 00 hex. If not, there is a fault with AB7 IC7e.

(13) Switch analyser to TALK. Set DIO lines to MTA and press EXECUTE.

(14) Set DIO lines to 00011001 (SPD) and press EXECUTE. Check instrument display is restored. If not, go to 'SPIS fault'.

(15) Set DIO lines to 00011000 (SPE) and press EXECUTE. TF 2356 display shows dots, TF 2357 display is unaffected.

(16) Set DIO lines to MTA and press EXECUTE. Switch analyser to LISTEN. DAV lamp comes on and TF 2357 display blanks.

(17) Send IFC and check display is restored. If not, go to 'IFC fault'.

Transfer of data and commands

11. During the course of these checks any incorrect data received will cause the SRQ lamp to illuminate - for a mistake made in entering data switch instrument off, then on and repeat 11(1) onwards. To check the transfer of data continue as follows:-

(1) Set analyser to TALK. Set DIO lines to 00110101 (TF 2357) or 00100011 (TF 2356) and press EXECUTE to send MLA.

(2) Set ATN to 0. Set DIO lines to 01000110 (ISO F) and press and hold EXECUTE button. Check NDAC lamp goes off. If not, go to 'Acceptor handshake control fault (b)'.

(3) Release EXECUTE button and check SRQ lamp is off. If not, go to 'Binary/decimal decoder fault'.

(4) Set DIO lines to 00110001 (ISO 1) and press EXECUTE. Check Instrument shows 1 in FREQUENCY window and ENTER lamp comes on. If not, go to 'Binary/decimal decoder fault'.

(5) Set DIO lines to 00110010 (ISO 2) and press EXECUTE. Check Instrument shows 12 in FREQUENCY window. If not, go to 'Binary/decimal decoder fault'.

(6) Set DIO lines to 00110100 (ISO 4) and press EXECUTE. Check Instrument shows 124 in FREQUENCY window. If not, go to 'Binary/decimal decoder fault'.

(7) Set DIO lines to 00111000 (ISO 8) and press EXECUTE. Check Instrument shows 1248 in FREQUENCY window. If not, go to 'Binary/decimal decoder fault'.

(8) Set DIO lines to 01001011 (ISO K - for kHz) and press EXECUTE. Check instrument shows 1248.00 kHz in FREQUENCY window. If not, go to 'Binary/decimal decoder fault'.

(9) Set DIO lines to 00001101 (CR) and press EXECUTE. Check ENTER lamp goes off. If not, go to 'Binary/decimal decoder fault'.

(10) TF 2357 only: Set ATN to 1 and set DIO lines to 00001000 (GET) and press EXECUTE. Check that SRQ lamp comes on. If not, go to 'GET fault'.

Device clear

(11) Set ATN to 1 and set DIO lines to 00000100 (SDC) and press EXECUTE while watching instrument display. Check that it blanks briefly, shows software version number, then displays 1000.00 kHz. If not, go to 'SDC fault'.

(12) Set DIO lines to 00010100 (DCL) and press EXECUTE while watching instrument display. Check that it blanks briefly, shows software version number, then displays 1000.00 kHz. If not, AB6, IC1 is faulty, go to 'Data input and message decoder fault'.

(13) Set DIO lines to 00000100 (SDC) and press EXECUTE. Check that instrument display is unaffected.

Controller functions TF 2356

12. The sender controller functions may be checked (but not comprehensively) as follows:-

(1) Set analyser to FAST and LISTEN. Set sender rear panel switch to SLM CONTROLLER.

(2) Switch SLM CONTROL to ON (display goes off briefly, then is restored). Check analyser REN lamp comes on.

(3) Set analyser to HALT. Set sender SLM control to START (display will be replaced by 6 dots).

(4) Check that analyser displays 030 octal or 18 hex. If not, check data bus on analyser rear panel using Table 1 to localize faulty signal (note signals are asserted low).

(5) Single step through bus operations using EXECUTE button. Check at each step that analyser display agrees with Table 1. If not, check data bus to localize faulty signal.

TABLE 1 CONTROLLER FUNCTIONS - TF 2356

Display		*Signals Asserted*	*DIO Lines*								*ATN*
Oct	*Hex*		*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	
030	18	SPE	H	H	H	L	L	H	H	H	L
101	41	TAD	H	L	H	H	H	H	H	L	L
137	5F	UNT	H	L	H	L	L	L	L	L	L
031	19	SPD	H	H	H	L	L	H	H	L	L
077	3F	UNL	H	H	L	L	L	L	L	L	L
041	21	MLA	H	H	L	H	H	H	H	L	L
106	46	F	H	L	H	H	H	L	L	H	H

H $\geq$ 3.4 V ; L $\leq$ 0.8 V

FAULT FINDING

Power-up fault

13. Check for a power-up fault as follows:-

(1) Remove GPIB boards then switch on and confirm that instrument powers-up correctly. If not, fault does not lie in interface boards.

(2) Replace boards in instrument with AB16 on extender board. Switch on and check RESET AB16,29 (TF 2357) or AB16,28 (TF 2356) for +7.5 V. If not, check AB16,B30 (TF 2357) or AB16,B28 (TF 2356) for 0 V. If not, SDC or DCL signal is faulty, go to 'Data input and message decoder fault'.

(3) Switch off, then on while checking AB16,B31 (TF 2357) or AB16,B29 (TF 2356) for 0.5 s +5 V pulse. If not, there is possibly a fault in power reset circuitry, go to 'Power-on reset fault'.

(4) Check AB16 IC1 pin 3 (TF 2357) or pin 10 (TF 2356) for 0 V. If not, latch IC1 is faulty.

(5) There is a fault with level shifter TR6 (TF 2357) or TR5 (TF 2356).

Power-on reset fault

14. Check for a power-on reset fault as follows:-

(1) Switch instrument off, then on while checking for initial 0.5 s negative pulse on AB6,6. If not present, there is possibly a faulty connection to RESET OUT AB2,28.

(2) Switch off, then on while checking for 0.5 s positive pulse on AB6,5. If not present IC9b is faulty.

(3) Switch off, then on while checking for negative pulse on AB6,B5. If not present IC9a is faulty.

SDC fault

15. Check for a selected device clear fault as follows:-

(1) Check AB6,6 for 30 µs positive pulse when EXECUTE is pressed. If not, go to 'Data input and message decoder fault'.

(2) Check AB16,28. If low, there is a fault with AB2,D8 or RESET INPUT of IC1.

(3) There is a fault with AB16 IC1 or inverter TR5.

Remote lamp fault

16. Check for a remote lamp fault as follows:-

(1) If AB6,10 is 0 V there is a fault on AE2.

(2) If AB6,10 is +5 V there is a fault in remote/local logic on AB6. Go to 'Remote/local fault'.

Incorrect local operation

17. Check for incorrect local operation as follows:-

(1) Check AB16,24 for a steady +7.5 V. If so, fault is not with GPIB boards and instrument is probably misreading remote message from interface. Fault probably lies with AB3 IC7.

(2) Check AB16, B24 for 0 V. If so, there is a fault with inverter TR1.

(3) Check AB6,10 for 0 V. If so, there is a fault with AB5 data selectors. Go to 'Data selector fault'.

(4) There is a fault with remote/local logic on AB6. Go to 'Remote/ local fault' and fault on REMOTE lamp driver on board AE2.

rtl fault

18. Check for a return to local fault as follows:-

(1) Place AB6 on extender board and switch on. With REN and ATN at 1 press EXECUTE to send MLA (REMOTE lamp comes on).

(2) Check AB6,9 for positive rtl pulse when C key is pressed. If not, fault in RAM 1 output port or interconnections.

(3) Localize fault by comparing logic levels with those shown in Fig. 1.

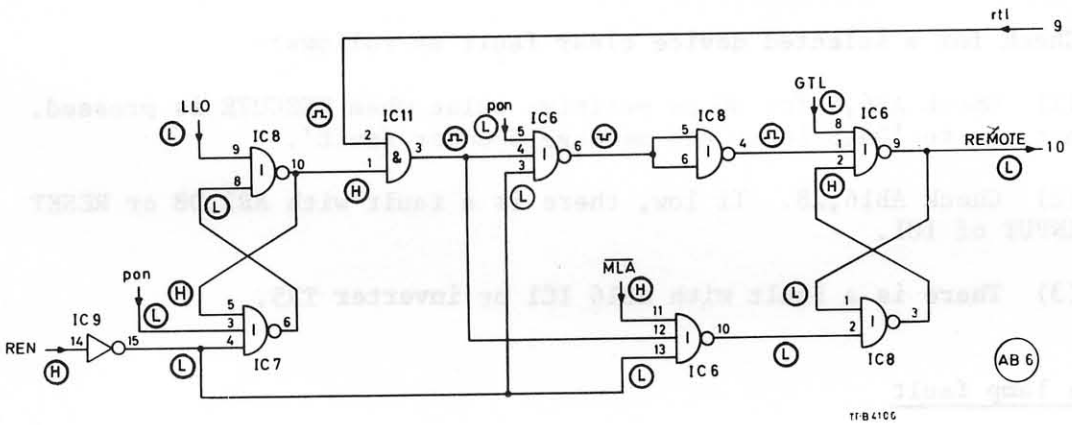


Fig. 1 'rtl fault' logic levels (pulse occurs when C key is pressed)

LLO fault

19. Check for a local lockout fault as follows:-

(1) Place AB6 on extender board and switch on. Set DIO lines to MLA and with REN and ATN at 1 press EXECUTE (REMOTE lamp comes on).

(2) Set DIO lines to 00010001 (LLO). Check AB6 IC8 pin 9 for positive pulse each time EXECUTE is pressed. If not present, go to 'Data input and message decoder fault'.

(3) Localize fault by comparing logic levels with those shown in Fig. 2.

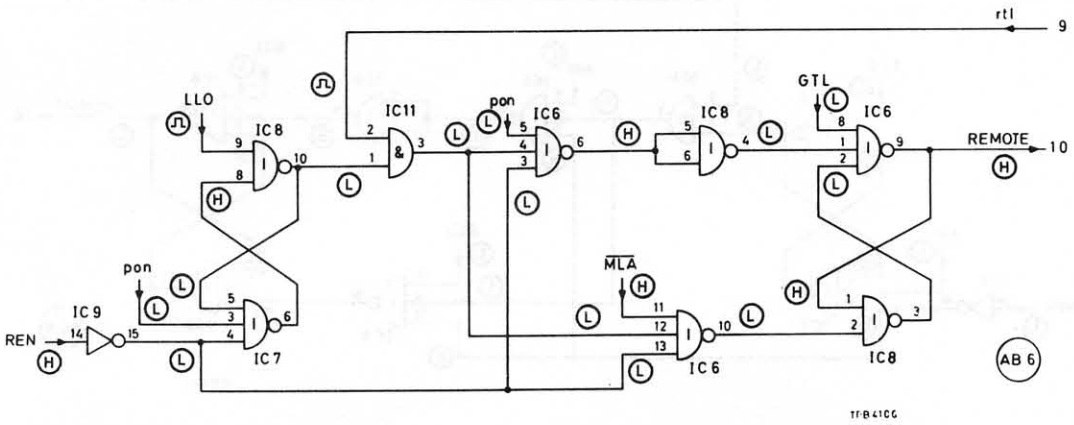


Fig. 2 'LLO fault' logic levels (LLO pulse occurs when analyser EXECUTE button is pressed, rtl pulse occurs when instrument C key is pressed).

GTL fault

20. Check for a go to local fault as follows:-

(1) Place AB6 on extender board and switch on. Set DIO lines to MLA and with REN and ATN at 1 press EXECUTE (REMOTE lamp comes on).

(2) Set DIO lines to 00000001 (GTL). Check AB6 IC6 pin 8 for positive pulse each time EXECUTE is pressed. If not present, go to 'Data input and message decoder fault'.

(3) IC6a is faulty.

Remote fault

21. Check for a remote fault as follows:-

(1) Place AB6 on extender board and switch on. Check AB6,10 is low. If not, go to 'Power-on reset fault'.

(2) Localize fault by comparing logic levels with those shown in Fig. 3.

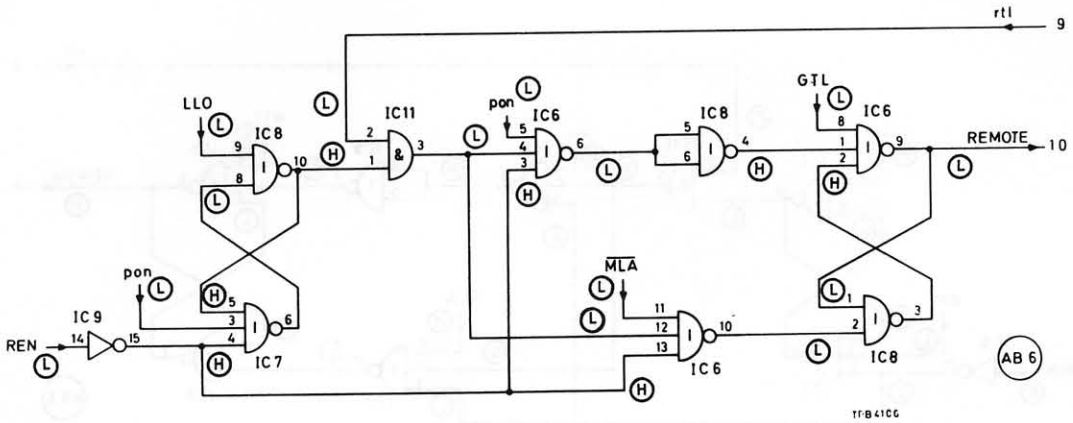


Fig. 3 'Remote fault' logic levels (>1 s after switch-on)

Remote/local fault

22. Check for a remote/local fault as follows:-

(1) Place AB6 on extender board. Set REN and ATN to 0 and switch instrument on. If AB6,10 is low and REMOTE lamp is on, there is a fault with board AE2.

(2) Check AB6,14. If high, there is a transceiver or interconnection fault.

(3) Set REN and ATN to 1. Press EXECUTE while checking AB6 IC6 pin 11 for negative $\overline{\text{MLA}}$ pulse. If not present, there is probably a fault with IC1.

(4) Localize fault by comparing logic levels with those given in Fig. 4.

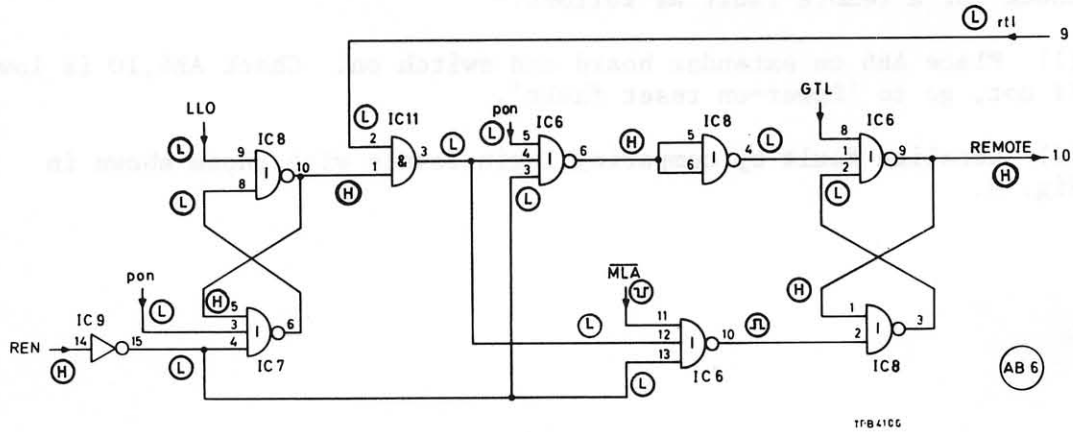


Fig. 4 'Remote/local fault' logic levels (pulses occur when EXECUTE pressed)

Service request fault

23. Check for a service request fault as follows:-

(1) Switch off, then on and set ATN to 1. Set DIO lines to MLA and press EXECUTE.

(2) Set ATN to 0 and press EXECUTE (to send faulty data) while watching AB6,B8. Check for a positive pulse (TF 2356) or continuous pulsing (TF 2357). If not, either AB5 IC7 or ROM 3 output port is faulty.

(3) Place AB6 on extender board. Repeat steps (1) and (2) above then localize fault by comparing logic levels with those given in Fig. 5 (to generate TF 2356 rsv pulse repeat steps (1) and (2) above).

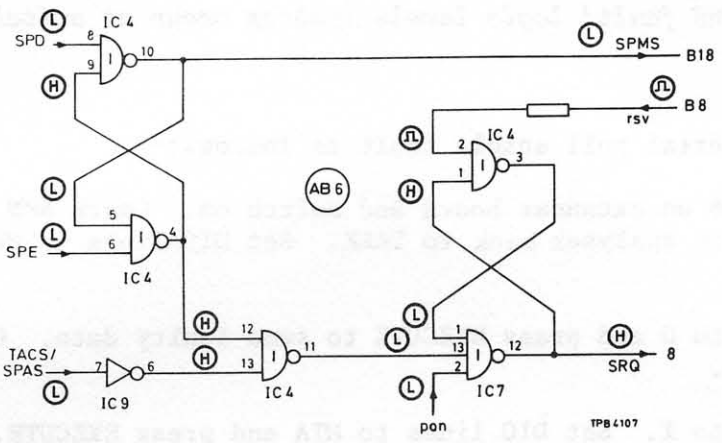


Fig. 5 'Service request fault' logic levels (see text for rsv pulse generation)

(4) Check AB6,8 is high. If not, there is a fault with transceiver IC2.

NPRS fault

24. Check for a negative poll response state fault as follows:-

(1) Place AB6 on extender board and switch on. If SRQ lamp is still on, localize fault by comparing logic levels with those given in Fig. 6.

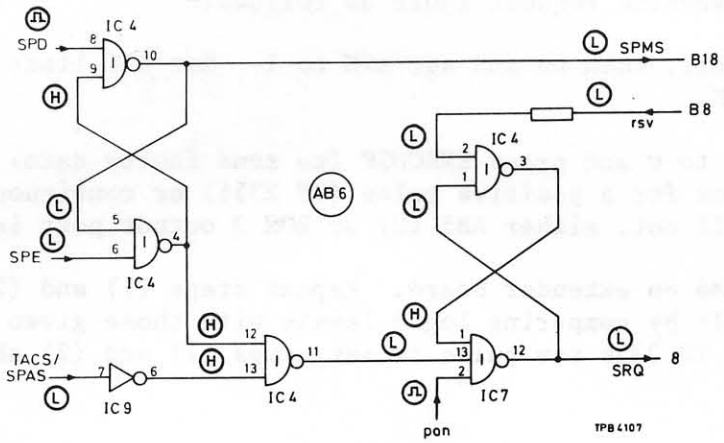


Fig. 6 'NPRS fault' logic levels (pulses occur at switch-on)

SPE fault

25. Check for a serial poll enable fault as follows:-

(1) Place AB6 on extender board and switch on. Check REN and ATN are at 1 and switch analyser back to TALK. Set DIO lines to MLA and press EXECUTE.

(2) Set ATN to 0 and press EXECUTE to send faulty data. Check SRQ lamp comes on.

(3) Set ATN to 1. Set DIO lines to MTA and press EXECUTE.

(4) Set DIO lines to 00011000 (SPE). Check IC4 pin 6 for positive pulse each time EXECUTE is pressed. If not, go to 'Data input and message decoder fault'.

(5) Set analyser to LISTEN and localize fault by comparing logic levels with those shown in Fig. 7.

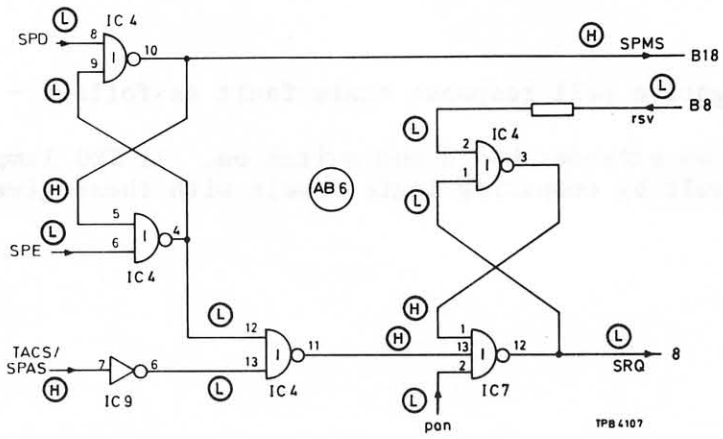


Fig. 7 'SPE fault' logic levels

SPAS fault

26. Check for a serial poll active state fault as follows:-

(1) Check AB7,B10 is high. If not, go to 'Talker addressed latch fault'.

(2) Check AB7,30 is high. If not, go to 'Data output latch fault'.

(3) Place AB7 on extender board and switch on. Check REN and ATN are at 1 and switch analyser back to TALK. Set DIO lines to MLA and press EXECUTE.

(4) Set ATN to 0 and press EXECUTE to send faulty data. Check SRQ lamp comes on.

(5) Set ATN to 1. Set DIO lines to MTA and press EXECUTE.

(6) Set DIO lines to 00011000 (SPE) and press EXECUTE.

(7) Set analyser to LISTEN and localize fault by comparing logic levels with those shown in Fig. 8.

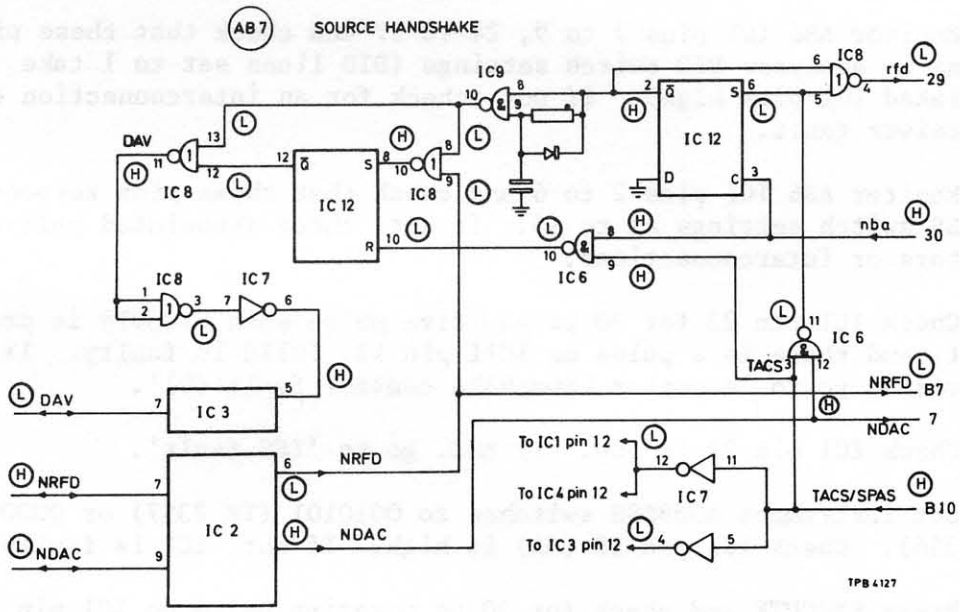


Fig. 8 'SPAS fault' logic levels

SPIS fault

27. Check for a serial poll idle state fault as follows:-

(1) Check AB6,B18 is low. If not, go to 'SPD fault'.

(2) Check AB5,B18 is low. If not, go to 'Data selector fault'.

SPD fault

28. Check for a serial poll disable fault as follows:-

(1) Place AB6 on extender board and switch on. Check REN and ATN are at 1. Set DIO lines to MLA and press EXECUTE.

(2) Set ATN to 0 and press EXECUTE to send faulty data. Check SRQ lamp comes on.

(3) Set ATN to 1. Set DIO lines to MTA and press EXECUTE.

(4) Set DIO lines to 00011001.

(5) Check IC4 pin 8 for positive pulse each time EXECUTE is pressed. If not, go to 'Data input and message decoder fault'.

(6) There is a fault with IC4.

Data input and message decoder fault

29. Check for a data input and message decoder fault as follows:-

(1) Place AB6 on extender board. Switch analyser to TALK and set ATN and REN to 1. Send IFC.

(2) Monitor AB6 IC1 pins 7 to 9, 24 to 27 and check that these pins respond to analyser DIO switch settings (DIO lines set to 1 take associated IC1 pins high). If not, check for an interconnection or transceiver fault.

(3) Monitor AB6 IC1 pins 2 to 6 and check that these pins respond to ADDRESS switch settings A1 to A5. If not, check associated pull-up resistors or interconnections.

(4) Check IC1 pin 23 for 30 µs positive pulse when EXECUTE is pressed. If not, and there is a pulse on IC11 pin 12, IC11d is faulty. If pulse not present go to 'Acceptor handshake control fault (b)'.

(5) Check IC1 pin 22 is low. If not, go to 'IFC fault'.

(6) Set instrument ADDRESS switches to 0010101 (TF 2357) or 0000011 (TF 2356). Check IC1 pin 18 (MA) is high. If not, IC1 is faulty.

(7) Press EXECUTE and check for 30 µs negative pulse on IC1 pin 10 ($\overline{\text{MLA}}$). If not, pull-up resistor or IC1 is faulty.

(8) Press EXECUTE and check for positive pulse on IC1 pin 11 (MLA/MTA). If not, pull-up resistor or IC1 is faulty.

(9) Press EXECUTE and check for positive pulse on IC2 pin 7 (MLA). If not, there is a fault with IC1 or IC2 (see Tables 2 and 3 for logic levels).

(10) Check for low on IC1 pin 21. If not, go to 'Listener addressed latch fault'.

TABLE 2 FPLA INPUT AND OUTPUT LOGIC - AB6

Message	*IC1 Input Variable (Pins)*																*IC1 Output Variable (Pins) Active Level*							
	6	*5*	*4*	*3*	*2*	*27*	*26*	*25*	*24*	*9*	*8*	*7*	*20*	*21*	*22*	*23*	*17*	*13*	*12*	*16*	*10*	*11*	*18*	*15*
GET	-	-	-	-	-	L	L	L	H	L	L	L	-	L	L	H	L	L	L	L				
GTL	-	-	-	-	-	L	L	L	L	L	L	H	-	L	L	H	L	L	L					
LLO	-	-	-	-	-	L	L	H	L	L	L	H	-	-	L	H	L	L		L				
SDC	-	-	-	-	-	L	L	L	L	H	L	L	-	L	L	H	L	L						
DCL	-	-	-	-	-	L	L	H	L	H	L	L	-	-	L	H	L	L						
SPE	-	-	-	-	-	L	L	H	H	L	L	L	-	-	L	H	L		L	L				
SPD	-	-	-	-	-	L	L	H	H	L	L	H	-	-	L	H	L	L						
IFC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	H	-	L	L						
MLA	-	-	-	-	-	L	H	-	-	-	-	-	H	-	L	H	L			L	L	H		
MTA	-	-	-	-	-	H	L	-	-	-	-	-	H	-	L	H	L					H		
UNL	-	-	-	-	-	L	H	H	H	H	H	H	-	-	L	H		L	L					
OTA	-	-	-	-	-	H	L	-	-	-	-	-	L	-	L	H								H
MAO	L	L	L	L	L	-	-	L	L	L	L	L	-	-	-	-							H	
MAI	L	L	L	L	H	-	-	L	L	L	L	H	-	~~-~~	-	-							H	

L = 0 V; H = +5 V

H 52356-900D
H 52357-900Z

TABLE 3 MESSAGE DECODER - AB6

Command Asserted	*IC2 Input Pins*				*IC2 Output Pins*								
	11	*10*	*12*	*13*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*14*	*15*
SPE	L	L	H	L	H	L	L	L	L	L	L	L	L
LLO	L	L	L	H	L	H	L	L	L	L	L	L	L
GET	L	L	L	L	L	L	H	L	L	L	L	L	L
MTA	L	H	H	H	L	L	L	H	L	L	L	L	L
UNL	H	H	L	L	L	L	L	L	H	L	L	L	L
SPD	L	H	H	L	L	L	L	L	L	H	L	L	L
MLA	L	L	H	H	L	L	L	L	L	L	H	L	L
GTL	L	H	L	L	L	L	L	L	L	L	L	H	L
SDC,DCL	L	H	L	H	L	L	L	L	L	L	L	L	H
	(L = 30 µs negative pulse)				(H = 30 µs positive pulse)								

H = +5 V; L = 0 V

(11) Set DIO lines on analyser to send addressed commands GET, SDC, GTL and lastly UNL while checking IC2 pins 15, 3, 14 and 5 respectively for 30 µs positive pulse each time EXECUTE is pressed. If not, there is a fault with IC1 or IC2 (see Tables 2 and 3 for logic levels).

(12) Set DIO lines to send universal commands DCL, LLO, SPE and SPD while checking IC2 pins 15, 2, 1 and 6 for 30 µs positive pulse each time EXECUTE is pressed. If not, there is a fault with IC1 or IC2 (see Tables 2 and 3 for logic levels).

(13) Set DIO lines to MLA and press EXECUTE. Reset DIO lines to MTA and check IC1 pin 11 for 30 µs positive pulse when EXECUTE is pressed. If not, IC1 is faulty.

(14) Press EXECUTE while checking for pulse on IC2 pin 4. If not, IC1 or IC2 is faulty (see Tables 2 and 3 for logic levels).

(15) Set DIO lines to 01010100 (TF 2357) or 01000010 (TF 2356) to assert OTA. Press EXECUTE while checking for pulse on IC1 pin 15. If not, IC1 or pull-up resistor is faulty. Replace AB6.

Listener addressed latch fault

30. Check for a listener addressed latch fault as follows:-

(1) Place AB6 on extender board. Set analyser to TALK and check REN and ATN are at 1. Set DIO lines to MLA and press EXECUTE.

(2) Set DIO lines to 00111111 (UNL) and press EXECUTE.

(3) Check logic levels agree with those shown in Fig. 9.

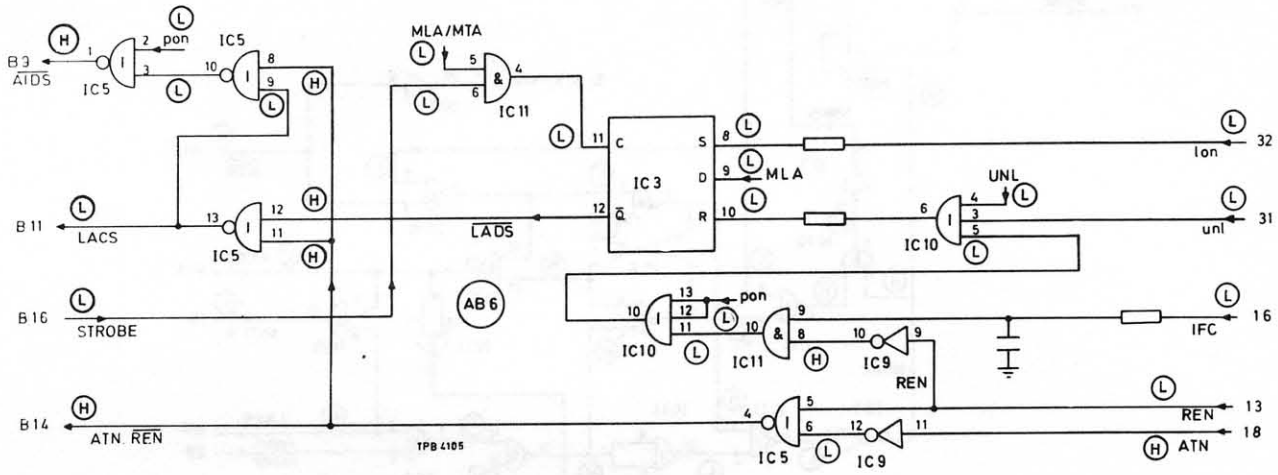


Fig. 9 'Listener addressed latch fault' logic levels

(4) Check IC11 pin 6 for positive pulse when EXECUTE is pressed. If not, go to 'Address recognition strobe fault'.

(5) Check IC3 pin 11 for positive pulse when EXECUTE is pressed. If not present, and there is a pulse on IC11 pin 5 when EXECUTE is pressed, then IC11b is faulty.

(6) Check IC3 pin 12 goes low when EXECUTE is pressed to send MLA. If not, check IC3 pin 9 for 30 µs positive pulse each time EXECUTE is pressed. If pulse not present, go to 'Data input and message decoder fault'; if pulse present, there is a fault with IC3b.

(7) Set ATN to 0 and check AB6,B11 is high. If not, and AB6,B14 is low, then IC5d is faulty.

(8) If AB6,B14 is high, go to 'REN and ATN gating logic fault'.

Address recognition strobe fault

31. Check for an address recognition strobe fault as follows:-

(1) Place AB7 on extender board. Check REN and ATN are at 1. Set DIO lines to MLA.

(2) Check AB7,B16 for positive pulse when EXECUTE is pressed to send MLA. If not, localize fault by comparing logic levels with those shown in Fig. 10.

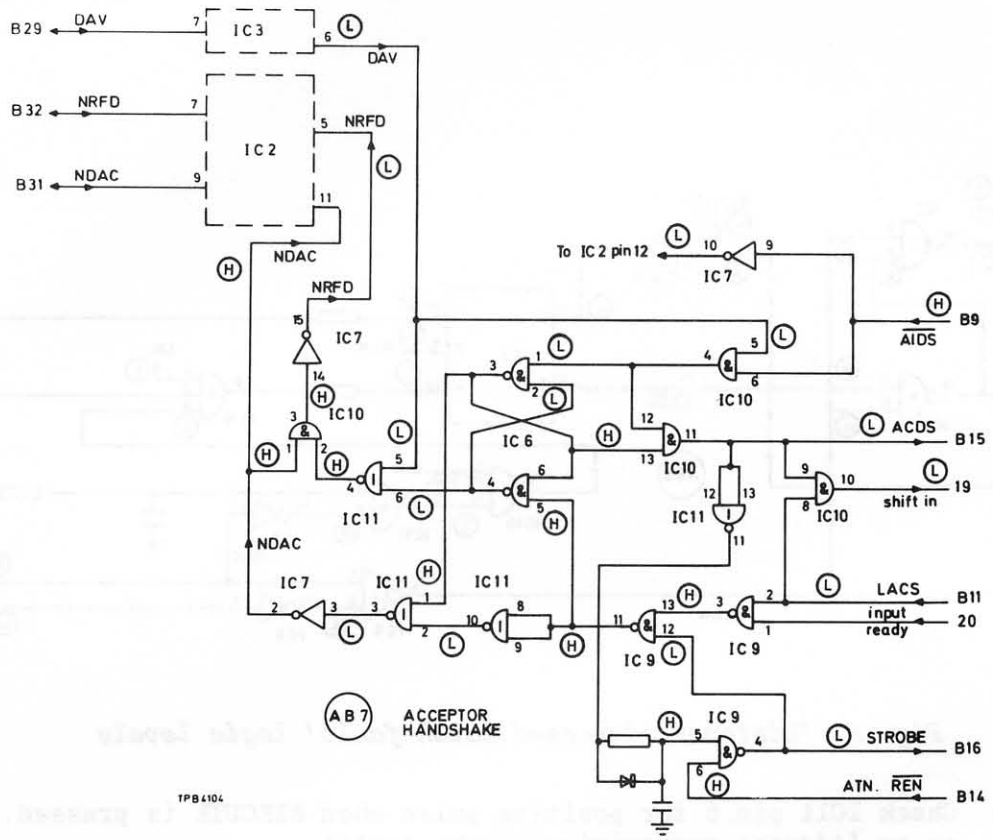


Fig. 10 'Address recognition strobe fault' and 'Acceptor handshake control fault (b)' logic levels

Unlisten fault

32. Check for an unlisten fault as follows:-

(1) Place AB6 on extender board and switch on. Set REN and ATN to 1. Set DIO lines to MLA and press EXECUTE.

(2) Set ATN to 0. Hold IFC asserted and check AB6 IC3 pin 10 is high. If not, localize fault by comparing logic levels with those shown in Fig. 11.

(3) Release IFC. Check IC3 pin 12 is high. If not, IC3b is faulty.

(4) Check AB6,B11. If low, go to 'Acceptor handshake control fault (a)'.

(5) If AB6,B11 is high, IC5d is faulty.

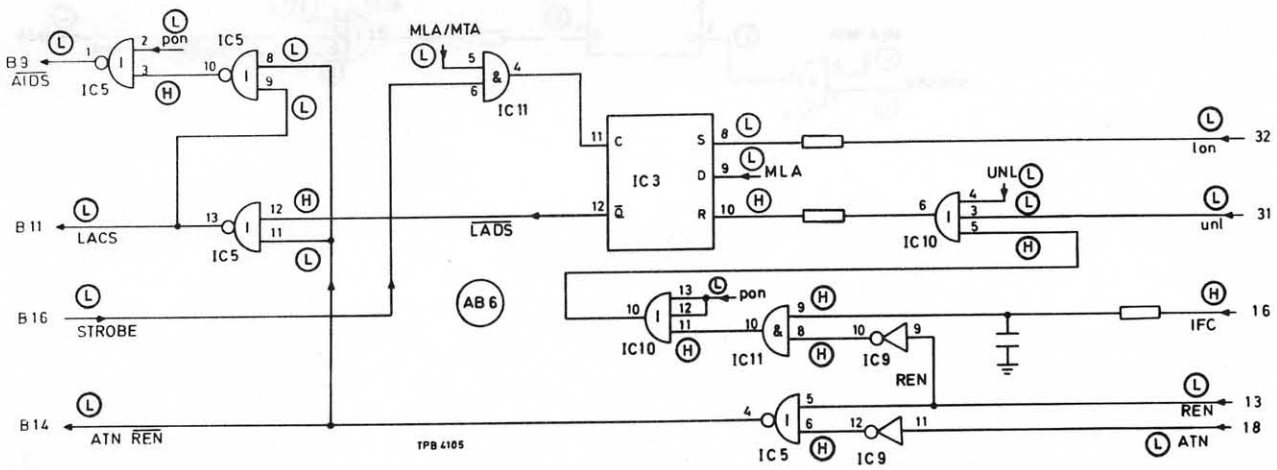


Fig. 11 'Unlisten fault' logic levels

Programmed unlisten fault

33. Check for a programmed unlisten fault as follows:-

(1) Place AB6 on extender board and switch on. Set REN and ATN to 1. Set DIO lines to MLA and press EXECUTE.

(2) Set DIO lines to 00111111 (UNL).

(3) Check IC2 pin 5 for decoded UNL pulse when EXECUTE is pressed. If not present, go to'Data input and message decoder fault'.

(4) Check IC3 pin 12. If low, IC3b or IC10b is faulty.

(5) Set ATN to 0 and check AB6,B11. If low, go to 'Acceptor handshake control fault (a)'.

(6) IC5d is faulty.

Talker addressed latch fault

34. Check for a talker addressed latch fault as follows:-

(1) Place AB6 on extender board and switch on. Switch analyser to TALK and check REN and ATN are at 1. Set DIO lines to MLA and press EXECUTE.

(2) Set DIO lines to 00111111 (UNL) and press EXECUTE.

(3) Check logic levels agree with those shown in Fig. 12.

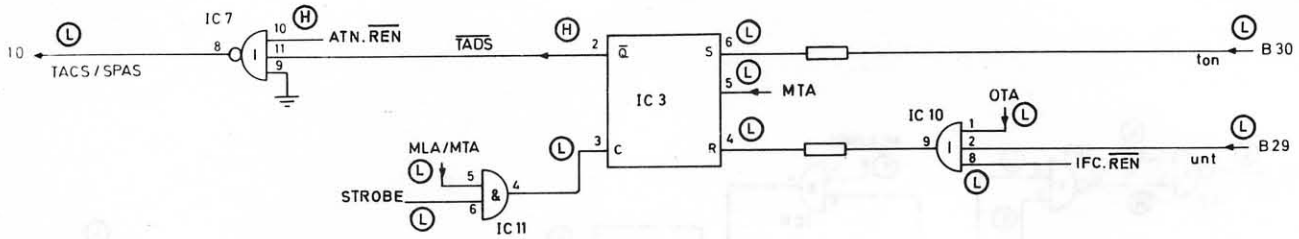


Fig. 12 'Talker addressed latch fault' logic levels

(4) Check IC11 pin 6 for positive pulse when EXECUTE is pressed. If not, go to 'Address recognition strobe fault'.

(5) Set DIO lines MTA.

(6) Check IC3 pin 3 for positive pulse when EXECUTE is pressed. If not present, and there is a pulse on IC11 pin 5 when EXECUTE is pressed, then IC11b is faulty.

(7) Check IC3 pin 2 goes low when EXECUTE is pressed. If not, check IC3 pin 5 for positive pulse each time EXECUTE is pressed. If pulse not present, go to 'Data input and message decoder fault'; if present there is a fault with IC3a.

(8) Set ATN to 0 and check AB6,B10 is high. If not, and AB6,B14 is low, then IC7c is faulty.

(9) If AB6,B14 is high, go to 'REN and ATN gating logic fault'.

Acceptor handshake control fault (a)

35. Check for an acceptor handshake fault when instrument is not addressed as a listener as follows:-

(1) Switch off, then on to return instrument to local. Compare logic levels on AB7 B29, B32 and B31 with analyser DAV, NRFD and NDAC lamps respectively. A lamp lit corresponds with a low on the relevant contact. If not, check rear panel interconnections.

(2) Set REN and ATN to 1. Send instrument to remote by setting DIO lines to MLA and pressing EXECUTE.

(3) Set DIO lines to 00111111 (UNL) and press EXECUTE.

(4) With ATN at 1 check AB7,B9 is high and AB7,B11 is low. Set ATN to 0 and check AB7,B9 and AB7,B11 are both low. If not, go to 'Listener addressed latch fault'.

(5) Set ATN to 1 and check AB7,B14 is high. Set ATN to 0 and check AB7,B14 is low. If not, go to 'REN and ATN gating logic fault'.

(6) Localize fault by comparing logic levels with those shown in Fig. 13.

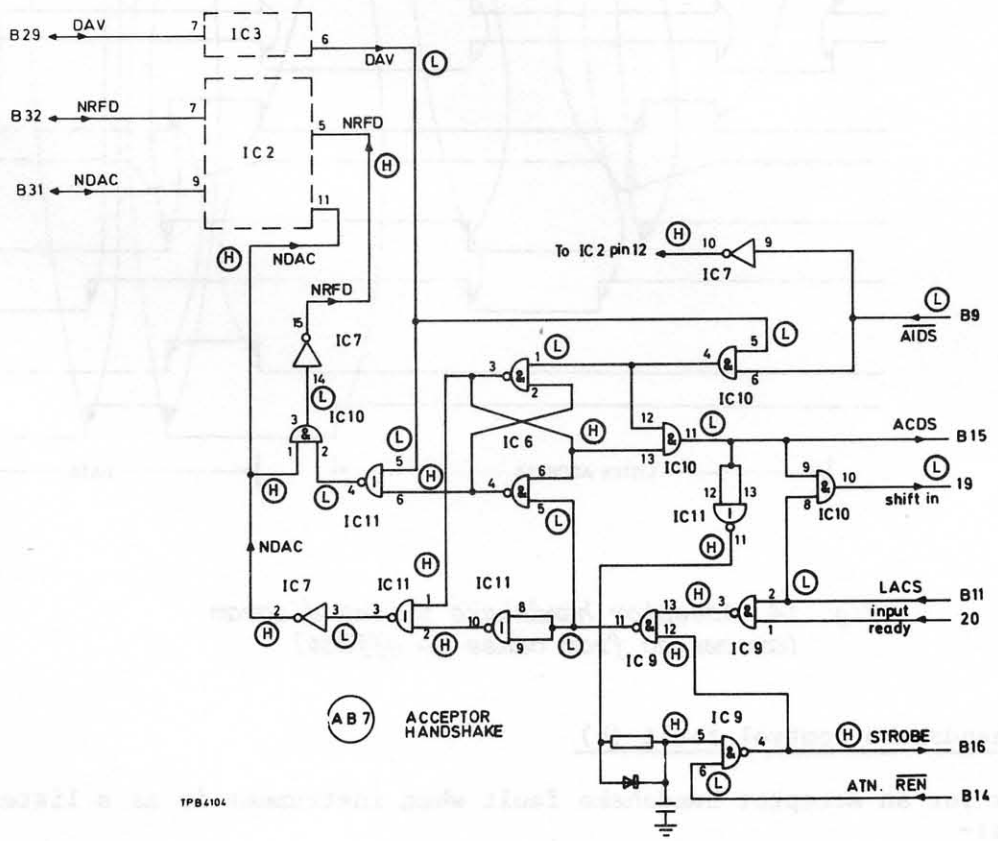


Fig. 13 'Acceptor handshake control fault (a)' logic levels

The acceptor handshake timing diagram is shown in Fig. 14.

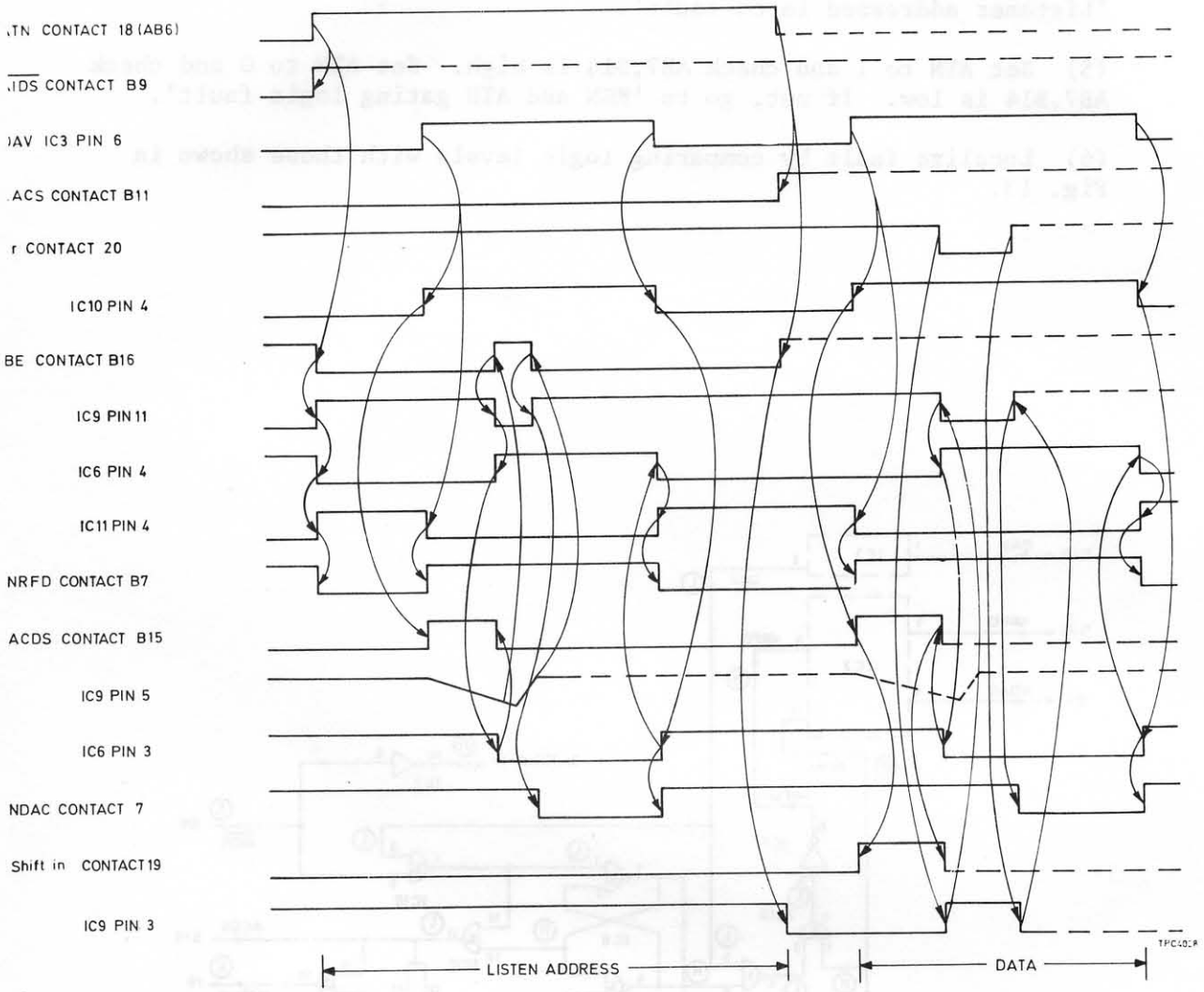


Fig. 14 Acceptor handshake timing diagram (arrows go from cause to effect)

Acceptor handshake control fault (b)

36. Check for an acceptor handshake fault when instrument is as a listener as follows:-

(1) Place AB7 on extender board and switch on. Set REN and ATN to 1. Set DIO lines to MLA and press EXECUTE.

(2) Localize fault by comparing logic levels with those shown in Fig. 10.

The acceptor handshake timing diagram is shown in Fig. 14.

REN and ATN gating logic fault

37. Check for a REN and ATN gating logic fault as follows:-

(1) Place AB6 on extender board. Switch instrument back on (instrument goes to local). Set ATN to 1.

(2) Check AB6,13 is low. If not, go to 'REN output fault'.

(3) Check AB6,18 is high. If not, there is a fault with AB7 IC3 or interconnections.

(4) Check AB6,5 is low. If not, go to 'Power-on reset fault'.

(5) Localize fault by comparing logic levels with those shown in Fig. 15.

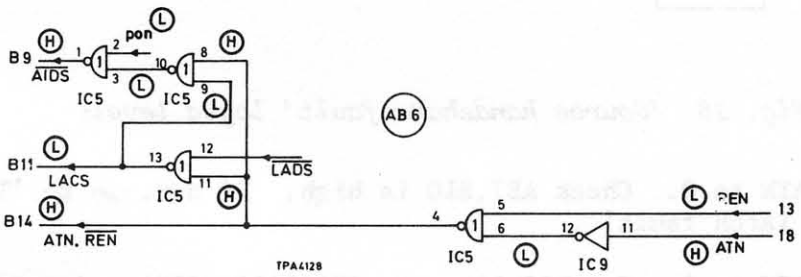


Fig. 15 'REN and ATN gating logic fault' logic levels

Source handshake fault

38. Check for a source handshake fault as follows:-

(1) Place AB7 on extender board and switch on. Switch analyser to TALK and check REN and ATN are at 1. Set DIO lines to MLA and press EXECUTE.

(2) Set DIO lines to 00111111 (UNL) and press EXECUTE.

(3) Check AB7,B10 is low. If not, go to 'Talker addressed latch fault'.

(4) Set ATN to 0 and check logic levels agree with those shown in Fig. 16.

(5) Set ATN to 1. Set DIO lines to MLA and press EXECUTE.

(6) Set ATN to 0 and press EXECUTE to send incorrect data. Check SRQ lamp comes on. If not, go to 'Service request fault'.

(7) Set ATN to 1. Set DIO lines to MTA and press EXECUTE.

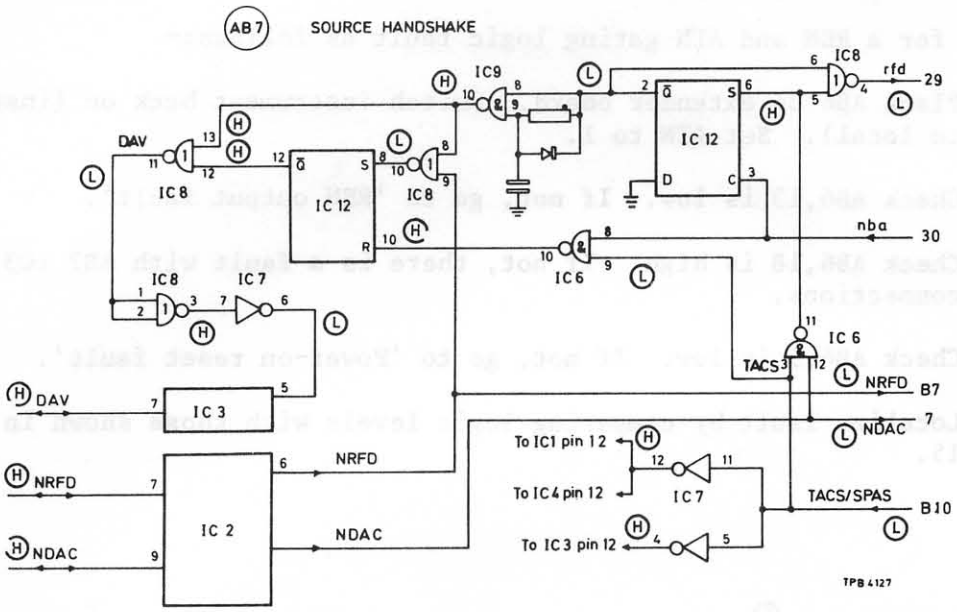


Fig. 16 'Source handshake fault' logic levels

(8) Set ATN to 0. Check AB7,B10 is high. If not, go to 'Talker addressed latch fault'.

(9) Set ATN to 1. Set DIO lines to 00011000 (SPE) and press EXECUTE (TF 2356 display shows dots).

(10) Set analyser to LISTEN (TF 2357 display blanks). Check NDAC and DAV lamps are lit.

(11) Check AB7,30 is high. If not, go to 'Data output latch fault'.

(12) Check AB7,7 is high. If not, check transceiver IC2. Check IC7 pin 6 is high. If not, there is a gating fault, check IC s 7c and 8a.

(13) Check AB7,30 for a narrow negative pulse when EXECUTE is pressed. If not, go to 'Data output latch fault'.

(14) Check AB7,29 for a positive pulse when EXECUTE is pressed. If not, there is a gating fault, checks IC s 6d and 8b.

The source handshake timing diagram is shown in Fig. 17.

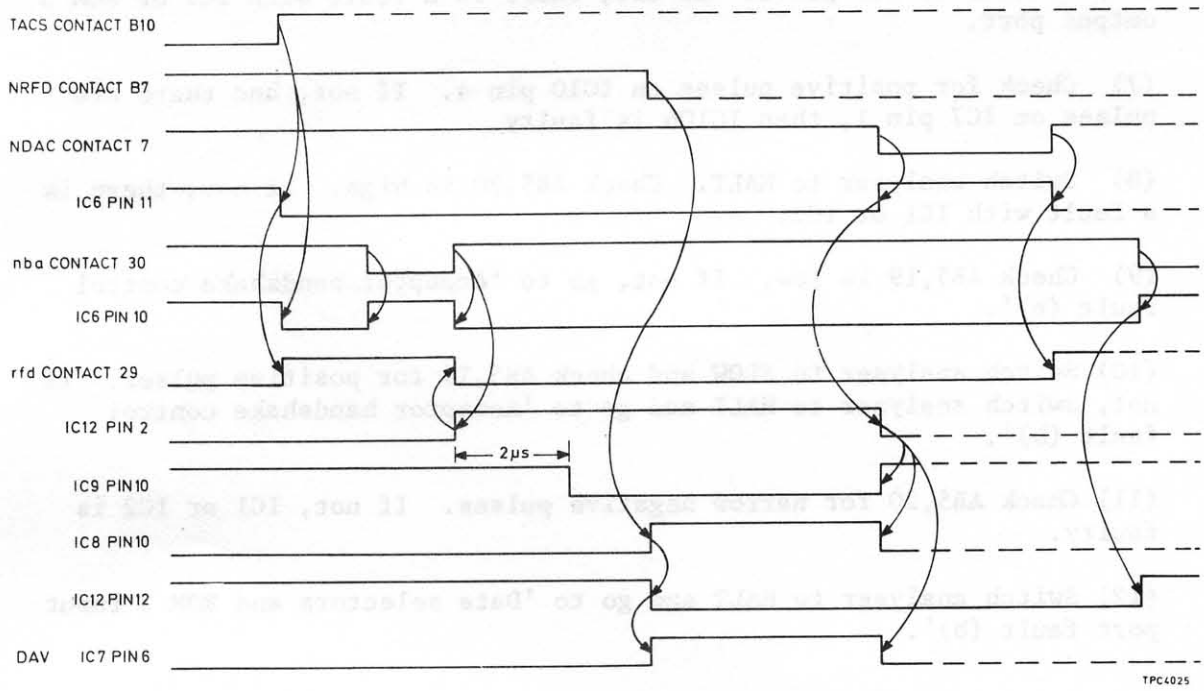


Fig. 17 Source handshake timing diagram (arrows go from cause to effect)

Binary/decimal decoder fault

39. Check for a binary/decimal decoder fault as follows:-

(1) Place AB5 on extender board. Check REN and ATN are at 1 and set DIO lines to MLA and press EXECUTE.

(2) TF 2357 only: Check IC7 pin 14 for 0.1 ms positive pulses at approx. 40 Hz. Check IC7 pin 15 for 0.6 ms negative pulses at approx. 40 Hz. If not, there is a fault with IC7 or ROM 3 output port.

(3) TF 2356 only: Check IC7 pin 14 for 1.4 ms positive pulses at approx. 500 Hz. Check IC7 pin 15 for 0.6 ms positive pulses occurring when pin 14 goes low. If not, there is a fault with IC7 or ROM 3 output port.

(4) Load bus analyser memory in every location with CR (015 octal, 0D hex) to prevent instrument asserting SRQ. Switch analyser to SLOW.

(5) TF 2357 only: Check IC7 pin 2 for 2 MS positive pulses directly following pulses on IC7 pin 14. Check IC7 pin 1 for 60 µs positive pulses following negative transitions of pulses on IC7 pin 15. If not, there is a fault with IC7 or ROM 3 output port.

(6) TF 2356 only: Trigger oscilloscope from and display pulses on IC7 pin 2. Check for 50 µs pulse followed 250 µs later by 20 µs pulse. Transfer to IC7 pin 1 and check for 20 µs pulses directly following 50 µs pulses on IC7 pin 2. If not, there is a fault with IC7 or ROM 3 output port.

(7) Check for positive pulses on IC10 pin 4. If not, and there are pulses on IC7 pin 1, then IC10b is faulty.

(8) Switch analyser to HALT. Check AB5,20 is high. If not, there is a fault with IC1 or IC2.

(9) Check AB5,19 is low. If not, go to 'Acceptor handshake control fault (b)'.

(10) Switch analyser to SLOW and check AB5,19 for positive pulses. If not, switch analyser to HALT and go to 'Acceptor handshake control fault (b)'.

(11) Check AB5,20 for narrow negative pulses. If not, IC1 or IC2 is faulty.

(12) Switch analyser to HALT and go to 'Data selectors and ROM 3 input port fault (b)'.

Data output latch fault

40. Check for a data output latch fault as follows:-

(1) Place AB5 on extender board and switch on. Check REN and ATN are at 1 and switch analyser back to TALK. Set DIO lines to MLA and press EXECUTE.

(2) Set ATN to 0 and press EXECUTE to send faulty data. Check SRQ lamp comes on.

(3) Set ATN to 1. Set DIO lines to MTA and press EXECUTE.

(4) Set DIO lines to 00011000 (SPE) and press EXECUTE.

(5) Set analyser to LISTEN (to clock in first status byte). Check IC8 pins 2, 10, 11 and 1 are all low. If not, check IC8 pin 5 for 0.1 ms positive pulse each time EXECUTE is pressed. If pulse present, go to 'RAM 0/1 output port to latches fault'; if pulses not present, go to Binary/decimal decoder fault'.

(6) Check IC9 pin 2 is low, and 1, 10 and 11 are high. If not, check IC9 pin 5 for positive pulse each time EXECUTE is pressed. If pulse present, go to 'RAM 0/1 output port to latches fault'; if not present, go to 'Binary/decimal decoder fault'.

(7) Press EXECUTE (clocks in second status byte) and check IC8 pins 10, 11 and 1 are low, and 2 is high. Check AB5 IC9 pins 1, 2 and 10 are high and 11 is low. If not, go to 'RAM 0/1 output port to latches fault'.

(8) Check transceivers for fault.

RAM 0/1 output port to latches fault

41. Check for a RAM 0 (TF 2357) or a RAM 1 (TF 2356) output port to latches fault as follows:-

(1) Place AB5 on extender board and switch on. Check REN and ATN are at 1 and switch analyser to TALK. Set DIO lines to MLA and press EXECUTE.

(2) Set ATN to 0 and press EXECUTE to send faulty data.

(3) Set ATN to 1. Set DIO lines to MTA and press EXECUTE.

(4) Set DIO lines to 00011000 (SPE) and press EXECUTE.

(5) Set analyser to LISTEN (to clock in first status byte) and check analyser display shows 140 octal or 60 hex. If not, there is a RAM output port fault (further checks may be made using logic analyser to monitor RAM output port lines - trigger from IC9 pin 5).

(6) Press EXECUTE (to clock in second status byte) and check analyser display shows 061 octal or 31 hex. If not, there is a RAM output port fault.

(7) If logic is correct but levels (+5 V, 0 V) are incorrect, check AB16 resistors R6 to R9.

(8) IC8 or IC9 is faulty.

REN output fault

42. Check for a REN output fault as follows:-

(1) Place AB5 on extender board and switch on.

(2) Confirm that IC10 pin 6 is high (fault condition).

(3) Check IC4 pin 13. If low, IC10c is faulty.

(4) Switch off, then on while checking for positive-going pon pulse on AB5 IC4 pin 10. If not present, go to 'Power-on reset fault' preceded by interconnection check.

(5) Switch off, then on while checking AB5 IC4 pin 11 for absence of positive-going clock pulse. If pulse present, there is a fault with IC7 or its data input, go to 'Binary/decimal decoder fault'.

(6) IC4b is faulty.

ATN output fault

43. Check for an ATN output fault as follows:-

(1) Place AB5 on extender board and switch on.

(2) Confirm that IC10 pin 12 is high (fault condition).

(3) Check IC4 pin 1. If low, IC10e is faulty.

(4) Switch instrument off, then on while checking for positive-going pon pulse on IC4 pin 4. If not, go to 'Power-on reset fault' preceded by interconnection check.

(5) Switch instrument off, then on while checking IC4 pin 3 for absence of positive-going clock pulse. If pulse present there is a fault with IC7 or its data input, go to 'Binary/decimal decoder fault'.

(6) IC4a is faulty.

IFC fault

44. Check for an IFC fault as follows:-

(1) Place AB6 on extender board and switch on. Check for high on IC10 pin 9 when IFC is sent. If not, IC10a is faulty.

(2) IC3a is faulty.

Data selector fault

45. Check for a data selector fault as follows:-

(1) Place AB5 on extender board and switch on.

(2) Check IC6 pin 14 for high logic level. If not, there is a fault with ROM 3 output port.

(3) Check IC7 pin 15 for high logic level (TF 2357) or positive pulses (TF 2356). If not, there is a fault with IC7.

(4) Check IC5 pin 3. If high, go to 'Remote/local fault'.

(5) There is probably a fault with IC5 or IC6, go to 'Data selectors and ROM 3 input port (a)'.

OTA fault

46. Check for an other talker addressed fault as follows:-

(1) Place AB6 on extender board and switch on. Check REN and ATN are at 1 and switch analyser back to TALK. Set DIO lines to MLA and press EXECUTE.

(2) Set DIO lines to MTA and press EXECUTE.

(3) Set DIO lines to 01010100 (TF 2357) or 01000010 (TF 2356) and press EXECUTE to send OTA.

(4) Check IC3 pin 2 is high. If not, check IC1 pin 15 for positive OTA pulse each time EXECUTE is pressed. If pulse not present, go to 'Data input and message decoder fault'.

(5) There is a fault with IC3a or IC10a.

GET fault

47. Check for a receiver GET fault as follows:-

(1) Set DIO lines to 00110101 (MLA) and press EXECUTE.

(2) Check AB16,28 is high. If not, and AB16,B28 and B29 are low, then fault lies with IC1ab or TR5.

(3) If AB16,B28 is high, go to 'Data input and message decoder fault'.

(4) If AB16,B29 is high, go to 'Binary/decimal decoder fault'.

(5) Set DIO lines to 00001000 (GET) and check AB16,28 for negative pulse when EXECUTE is pressed. If so, AB5, IC7 providing rsv signal is probably faulty, go to 'Binary/decimal decoder fault'.

(6) Check AB16,B28 for positive pulse when EXECUTE is pressed. If so, there is a fault with IC1ab or TR5. If not, IC1 or IC2 on AB6 is probably faulty.

(7) Check AB16,B29 for a positive pulse when EXECUTE is pressed. If not, there is a fault with AB6 IC7 or ROM 3 output port.

Data selectors and ROM 3 input port fault (a)

48. Check for a data selector or ROM 3 input port fault as follows:-

(1) Place AB5 on extender board and switch on. Check REN and ATN are at 1 and set DIO lines to MLA and press EXECUTE.

(2) Set ATN to 0 and set DIO lines to 01000110. Press EXECUTE to send ISO F.

(3) Set DIO lines to 00110001 and press EXECUTE to send ISO 1.

(4) Check AB5 IC5 pin 1 is high. If not, IC3a is faulty.

(5) Check IC5 pin 5 is low. If not, go to 'Service request fault'.

(6) Check IC5 pin 3 is high. If not, go to 'Remote/local fault'.

(7) Check IC5 pin 7 is low. If not, go to 'Source handshake fault'.

(8) Trigger oscilloscope from IC7 pin 15 and when high check IC5 pins 10 and 11 are low and pins 12 and 13 are high. If not, IC5 is faulty.

(9) Trigger oscilloscope from IC7 pin 15 and when high check B26 and B27 are low and B24 and B25 are high. If not, IC6 is faulty.

Data selectors and ROM 3 input port fault (b)

49. Check for a data selector or ROM 3 input port fault as follows:-

(1) Place AB5 on extender board and switch on. Check REN and ATN are at 1 and set DIO lines to MLA and press EXECUTE.

(2) Set ATN to 0 and set DIO lines to 01000110. Press EXECUTE to send ISO F.

(3) Set DIO lines to 00110001 (ISO 1) and press EXECUTE.

(4) Check IC1 pin 13 is high and pins 12, 11 and 10 are all low. If not, IC1 is faulty.

(5) Check IC2 pins 13 and 12 are high and pin 11 is low. If not, IC2 is faulty.

(6) Trigger oscilloscope from IC7 pin 14 and when high check IC5 pins 10 and 11 are high and pin 12 is low. If not, IC5 is faulty.

(7) Trigger oscilloscope from IC7 pin 14 and check B26 and B27 are high and B24 is low. If not, IC6 is faulty.

(8) Trigger oscilloscope from IC7 pin 2 and check B26 is high and B27, B24 and B25 are all low when EXECUTE is pressed and IC7 pin 2 is high. If not, IC6 is faulty.

(9) Trigger oscilloscope from AB5 IC7 pin 2 and check for a negative pulse on AB16,26 when EXECUTE is pressed. If not, inverter TR4 is faulty.

(10) Trigger oscilloscope from AB5 IC7 pin 2 and when high check for a high logic level on AB16, 27, 24 and 25. If not, there is a fault with TR3, TR1 or TR2 respectively (note that low level on contact 24 is 0 V).

REPLACEABLE PARTS

Chapter 6

CONTENTS

INTRODUCTION

1. Each sub-assembly or printed circuit board in this instrument has been allocated a unit identification, e.g. A0, AA2, AB1 etc.

2. The complete component reference carries its unit number as a prefix e.g. AB3C3 (capacitor C3 on the memory board) but for convenience in the text and on circuit diagrams the prefix is not used. However, when ordering replacements or in correspondence the complete component reference must be quoted.

ABBREVIATIONS

3. The components are listed in alphanumerical order of the complete circuit reference and the following abbreviations are used :

C	: capacitor	Plas	: plastic
Carb	: carbon	R	: resistor
Cer	: ceramic	S	: switch
D	: semiconductor diode	SK	: socket
Elec	: electrolytic	T	: transformer
FS	: fuse	Tant	: tantalum
IC	: integrated circuit (package)	TP	: terminal
L	: inductor	TR	: transistor
LP	: lamp	Var	: variable
Max	: maximum	W	: watts at 70°C
ME	: meter	WW	: wirewound
Met	: metal	X	: ferrite bead
Mic	: mica	XL	: crystal
Min	: minimum	†	: values selected during test; nominal value listed
Ox	: oxide		
PL	: plug	Ø	: lead through

COMPONENT VALUES

4. One or more of the components fitted in this instrument may differ from those listed in this chapter for any of the following reasons:

(a) Components indicated by a † have their values selected during test to achieve particular performance limits.

(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the instrument is maintained.

(c) As part of a policy of continuous development, components may be changed in value or type to obtain detail improvements in performance.

5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the instrument.

ORDERING

6. When ordering replacements, address the order to our Service Division (address inside rear cover) or nearest agent and specify the following for each component required :

(1) Type* and serial number of instrument.

(2) Complete circuit reference.

(3) Description.

(4) Marconi Instruments code number.

* As given on the serial number label at the rear of the instrument; if this is superseded by a model number label, quote the model number instead of the type number.

COMPONENTS

7. Unit A0 - Main chassis

When ordering prefix with A0.

Circuit ref.	Description	Code no.
	Ribbon cable assembly (ADDRESS)	43129-372F
	(CONTROL) 24-way	43129-203F
	(TO L.O.) 16-way	43129-219K
	(DISPLAY) 24-way	43129-267F
	(TO RF UNIT)	43129-324K
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	LED, green, CHARGE	28624-111X
	LED, yellow, ENTER (D12,AB10)	28624-112M
	Set of 4 pre-programmed EPROMs (AB3)	44553-007L
M1	Motor, TUNING	23535-401M
ME	Meter	44559-016M
R1	Fine level control	25641-199W
	Met film 11kΩ 2% 1/4W (R9†,AB1)	24773-298C
R101	Met film 10Ω 2% 1/4W	24773-225W
C101	Elec 1000µF +100-20% 10V	26415-824S
SA	SUPPLY, wafer	44340-095H
SB	Impedance, wafer	44340-101H
SC	EXT LEVELLING, slider	23467-117L
SD	dB/dBm, slider	23467-117L
SF	TUNING, toggle	23462-252Z
SKA	BALANCED OUTPUT, earth	33525-109M
SKB,C	BALANCED OUTPUT 2/SSO/14 (plated)	43149-006M
SKD	OUTPUT BNC 75Ω	23443-527G
SKE	SYNC OUT, BNC 50Ω	23443-443K
SKF	REMOTE COMMAND, BNC 50Ω	23443-443K
SKG	30-50 MHz IN bulkhead 75Ω	23443-512B
SKH	Control	23435-084F
SKK	EXT LEVELLING, BNC 50Ω	23443-443K
	Edge connector, 20-way, single sided	23435-068K
T1	Ring core, ferrite	23635-916U

8. Unit A1 - RF unit

When ordering prefix with A1.

Circuit ref.	Description	Code no.
	Complete assembly	44990-192B
C1	Plas 0.1µF 10% 160V	26511-350N
C2	Plas 0.1µF 10% 160V	26511-350N
C3	Plas 0.1µF 10% 160V	26511-350N
C4	Plas 0.1µF 10% 160V	26511-350N
C5	Plas 0.1µF 10% 160V	26511-350N
C6	Plas 0.1µF 10% 160V	26511-350N
C7	Plas 0.1µF 10% 160V	26511-350N
C8	Plas 0.1µF 10% 160V	26511-350N
C9	Elec 47µF +100-20% 10V	26415-809E
C10	Elec 47µF +100-20% 10V	26415-809E
C11	Elec 47µF +100-20% 10V	26415-809E
C12	Elec 47µF +100-20% 10V	26415-809E
C13	Elec 47µF +100-20% 10V	26415-809E
C14	Elec 47µF +100-20% 10V	26415-809E
C15	Cer 0.047µF +80-20% 12V	26383-016E
C16	Cer 0.047µF +80-20% 12V	26383-016E
C17	Cer 0.047µF +80-20% 12V	26383-016E
C18	Cer 150pF 2% 63V	26343-479W
C19	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C20	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C21	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C22	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C23	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C24	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
L1	RF choke 1000µH	23642-567C
L2	RF choke 1000µH	23642-567C
L3	RF choke 1000µH	23642-567C
L4	RF choke 1000µH	23642-567C
L5	RF choke 1000µH	23642-567C
L6	RF choke 1000µH	23642-567C
L7	RF choke 1000µH	23642-567C
L8	RF choke 1000µH	23642-567C
L9	RF choke 1000µH	23642-567C
L10	RF choke 1000µH	23642-567C
L11	RF choke 1000µH	23642-567C
L12	RF choke 1000µH	23642-567C
L13	RF choke 1000µH	23642-567C
L14	RF choke 1000µH	23642-567C
L15	RF choke 1000µH	23642-567C
L16	Choke assembly	44290-603T
L17	Choke assembly	44290-603T
L18	Choke assembly	44290-603T
L19	Choke assembly	44290-603T

Unit A1 - RF unit (continued)

Circuit ref.	Description	Code no.
R11	Met film 33kΩ 2% 1/4W	24773-309Z
R12	Met film 33kΩ 2% 1/4W	24773-309Z
R13	Met film 33kΩ 2% 1/4W	24773-309Z
R14	Met film 33kΩ 2% 1/4W	24773-309Z
R15	Met film 33kΩ 2% 1/4W	24773-309Z
R16	Met film 33kΩ 2% 1/4W	24773-309Z
R17	Met film 33kΩ 2% 1/4W	24773-209Z
R18	Met film 33kΩ 2% 1/4W	24773-309Z
R19	Met film 33kΩ 2% 1/4W	24773-309Z
R20	Met film 33kΩ 2% 1/4W	24773-209Z
R21	Met film 33kΩ 2% 1/4W	24773-309Z
R22	Met film 33kΩ 2% 1/4W	24773-309Z
R23	Met film 100kΩ 2% 1/4W	24773-321L
R24	Met film 33kΩ 2% 1/4W	24773-309Z
R25	Met film 33kΩ 2% 1/4W	24773-309Z
R26	Met film 33kΩ 2% 1/4W	24773-309Z
R27	Met film 33kΩ 2% 1/4W	24773-309Z
R28	Met film 33kΩ 2% 1/4W	24773-309Z
R29	Met film 33kΩ 2% 1/4W	24773-309Z
R30	Met film 100kΩ 2% 1/4W	24773-321L
R31	Met film 75Ω 2% 1/4W	24773-246Y
	Edge connector, 37-way, single sided (1 of 11)	23435-080Y

Circuit ref.	Description	Code no.
T2	Ferrite ring core	23635-910B
T3	Ferrite ring core	23635-910B
T4	Ferrite ring core	23635-910B
T5	Ferrite ring core	23635-910B
T6	Ferrite ring core	23635-910B
T8	Ferrite ring core	23635-913Z
X1	Ferrite bead	23635-812H
X2	Ferrite bead	23635-812H
X3	Ferrite bead	23635-812H
X4	Ferrite bead	23635-812H
X5	Ferrite bead	23635-812H
X6	Ferrite bead	23635-812H
X7	Ferrite bead	23635-812H
X8	Ferrite bead	23635-812H
X9	Ferrite bead	23635-812H
X9	Ferrite bead	23635-812H
X10	Ferrite bead	23635-812H
X11	Ferrite bead	23635-812H
X12	Ferrite bead	23635-812H

Circuit ref.	*Description*	*Code no.*
9.	Unit A2 - Local oscillator	
	When ordering prefix with A2.	
	Complete assembly	44990-184P
	Lead assembly (10 MHz STD-EXT IN)	43129-310V
C51	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C52	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C53	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C54	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C55	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C56	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C57	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C58	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C59	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C60	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C61	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C62	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C63	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C64	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C65	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C66	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C67	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C68	Cer Ø 0.0047µF +80-20% 500V	26373-665Z
C69	Cer 0.047µF +80-20% 25V	26383-017U
L51	Choke assembly	44290-603T
	Edge connector, 12-way, single sided (1 of 3)	23435-092D
	Edge connector, 37-way, single sided (1 of 3)	23435-080Y
	Edge connector, 37-way, double sided (1 of 6)	23435-070B
10.	Unit A3 - Power supply	
	When ordering prefix with A3.	
	Complete assembly	44990-174F
C1	Elec 4700µF +50-10% 25V	26426-076L
C2	Elec 4700µF +50-10% 40V	26426-077J
C3	Elec 4700µF +50-10% 40V	26426-077J
C4	Plas 0.47µF 10% 250V	26512-264N
C5	Plas 0.47µF 10% 250V	26512-264N
FS1,FS2	Fuse, 400mA (230V)	23411-053D
	Fuse, 800mA (115V)	23411-059R
	Holder (1 of 2)	23416-192R
	Cover (1 of 2)	23416-198E
	Spacer (1 of 2)	33900-714L

Circuit ref.	Description	Code no.
	Unit A3 - Power supply (contd.)	
IC1	µA7812	28461-708V
IC2	µA7912	28461-718M
PL1	Connector/supply filter	23423-150L
	Cover	37590-150P
	Spacer (1 of 2) Nominal length	33313-422L
	Support 3/4 in or 19 mm	37590-202U
R1	Met film 100kΩ 2% 1/4W	24773-321L
R2	Met film 100kΩ 2% 1/4W	24773-321L
S1	Supply range, d.p.c.o.	23467-161W
	Cover	37590-211G
	Locking plate	35901-630H
11.	Unit A4 - Display	
	When ordering prefix with A4.	
	Complete assembly	44990-193K
D1 to D11	Display diode set, LEVEL and FREQUENCY	44529-034T
	Keyboard switch, momentary (1 of 2)	23465-408B
	Keyboard switch, latching (1 of 3)	23465-409K
	Flexstrip jumper, 25-way	23436-105J
12.	Board AA1 - Mixer	
	When ordering prefix with AA1.	
	Complete assembly	44827-786P
C1	Cer 0.001µF +80-20% 500V	26383-242P
C2	Cer 0.001µF +80-20% 500V	26383-242P
C3	Cer 0.001µF +80-20% 500V	26383-242P
C4	Cer 0.001µF +80-20% 500V	26383-242P
C6	Cer 0.001µF +80-20% 500V	26383-242P
C7	Cer 0.001µF +80-20% 500V	26383-242P
C8	Cer 0.001µF +80-20% 500V	26383-242P
C9	Cer 0.001µF +80-20% 500V	26383-242P
C10	Cer 0.001µF +80-20% 500V	26383-242P
C11	Cer 0.001µF +80-20% 500V	26383-242P
C12	Cer 0.022µF +80-20% 18V	26383-007R
C13	Cer 0.001µF +80-20% 500V	26383-242P

Board AA1 - Mixer (contd.)

Circuit ref.	Description	Code no.
C14	Cer 0.001µF +80-20% 500V	26383-242P
C16	Plas 556pF 2% 63V	26538-622L
C17	Cer 0.047µF +80-20% 25V	26383-017U
C18	Cer 0.001µF +80-20% 500V	26383-242P
C19	Cer 82pF 2% 63V	26343-476G
C20	Cer 82pF 2% 63V	26343-476G
C21	Cer 150pF 2% 63V	26343-479W
C22	Cer 47pF 5% 63V	26343-473L
C23	Cer 100pF 2% 63V	26343-477V
C24	Cer 47pF 5% 63V	26343-473L
C25	Cer 0.047µF +80-20% 25V	26383-017U
C26	Cer 15pF 5% 63V	26343-467U
D1	1N4148	28336-676J
D2	1N4148	28336-676J
IC1	CA3039	28461-906Y
L1	Inductor	44290-547E
L2	Inductor	44290-553N
L3	Inductor	44290-652E
L4	Inductor	44290-562S
R1	Met film 6.2kΩ 2% 1/4W	24773-292W
R2	Met film 47kΩ 2% 1/4W	24773-313H
R3	Met film 56Ω 2% 1/4W	24773-243H
R4	Met film 7.5kΩ 2% 1/4W	24773-294T
R5	Met film 3.9kΩ 2% 1/4W	24773-287V
R6	Met film 7.5kΩ 2% 1/4W	24773-294T
R7	Met film 47kΩ 2% 1/4W	24773-313H
R8	Met film 15kΩ 2% 1/4W	24773-301P
R9	Met film 56Ω 2% 1/4W	24773-243H
R10	Met film 2.0kΩ 2% 1/4W	24773-280U
R11	Met film 20Ω 2% 1/4W	24773-232X
R12	Met film 3.0kΩ 2% 1/4W	24773-284J
R13	Met film 470Ω 2% 1/4W	24773-265M
R14	Met film 100Ω 2% 1/4W	24773-249J
R15	Met film 7.5kΩ 2% 1/4W	24773-294T
R16	Met film 100Ω 2% 1/4W	24773-249J
R17	Met film 51Ω 2% 1/4W	24773-242Z
R18	Met film 150Ω 2% 1/4W	24773-253F
R20	Met film 1.2kΩ 2% 1/4W	24773-275H
R21	Met film 390Ω 2% 1/4W	24773-263P
R22	Met film 51Ω 2% 1/4W	24773-242Z
R23	Met film 22Ω 2% 1/4W	24773-233M
R24	Met film 100Ω 2% 1/4W	24773-249J
R25	Met film 150Ω 2% 1/4W	24773-253F
R26	Met film 56Ω 2% 1/4W	24773-243H
R27	Met film 100Ω 2% 1/4W	24773-249J
R28	Met film 4.7kΩ 2% 1/4W	24773-289W

Circuit ref.	Description	Code no.
	Board AA1 - Mixer (contd.)	
R29	Met film 10kΩ 2% 1/4W	24773-297M
R30	Met film 51Ω 2% 1/4W	24773-242Z
R31	Met film 7.5kΩ 2% 1/4W	24773-294T
T1	Transformer	43590-031A
T2	Transformer	43590-032Z
T3	Transformer	43590-031A
T4	Transformer	43590-029Z
T5	Transformer	43590-029Z
T6	Transformer	43590-031A
T7	Transformer	43590-031A
TR1	BC308	28433-455R
TR2	BC238B	28452-781A
TR3	BC238B	28452-781A
TR4	BSX20	28452-197H
TR5	BSX20	28452-197H
TR6	BSX20	28452-197H
TR7	BSX20	28452-197H
TR8	BSX20	28452-197H
TR9	BSX20	28452-197H

Circuit ref.	Description	Code no.
13.	Board AA2 - Low-pass filter and amp.	
	When ordering prefix with AA2.	
	Complete assembly	44827-787X
C1	Elec 220µF +100-20% 10V	26423-251A
C2	Elec 220µF +100-20% 10V	26423-251A
C3	Elec 220µF +100-20% 10V	26423-251A
C4	Elec 220µF +100-20% 10V	26423-251A
C5	Elec 47µF +100-20% 25V	26423-231F
C6	Elec 220µF +100-20% 10V	26423-251A
C7	Cer 0.047µF +80-20% 25V	26383-017U
C8	Cer 0.047µF +80-20% 25V	26383-017U
C9	Cer 0.047µF +80-20% 25V	26383-017U
C10	Cer 0.047µF +80-20% 25V	26383-017U
C11	Cer 3.3pF ±0.5pF 63V	26343-459K
C12	Cer 10pF ±0.5pF 63V	26343-465H
C13	Cer 68pF 2% 63V	26343-475F
C14	Cer 10pF ±0.5pF 63V	26343-465H
C15	Cer 3.9pF ±0.5pF 63V	26343-460R
C16	Cer 47pF 5% 63V	26343-473L
C17	Cer 150pF 2% 63V	26343-479W
C18	Cer 10pF ±0.5pF 63V	26343-465H
C19	Cer 18pF 5% 63V	26343-468Y
C20	Cer 100pF 2% 63V	26343-477V

Circuit ref.	Description	Code no.
	Board AA2 - Low-pass filter and amp. (contd.)	
L1	Inductor	44290-551U
L2	Inductor	44290-551U
R1	Met film 51Ω 2% 1/4W	24773-242Z
R2	Met film 10Ω 2% 1/4W	24773-225W
R3	Met film 2kΩ 2% 1/4W	24773-280U
R4	Met film 3.3kΩ 2% 1/4W	24773-285F
R5	Met film 10kΩ 2% 1/4W	24773-297M
R6	Met film 2.7kΩ 2% 1/4W	24773-283L
R7	Met film 10Ω 2% 1/4W	24773-225W
R8	Met film 75Ω 2% 1/4W	24773-246Y
R9	Met film 100Ω 2% 1/4W	24773-249J
R10	Met film 1.3kΩ 2% 1/4W	24773-276E
R11	Met film 10Ω 2% 1/4W	24773-225W
R12	Met film 750Ω 2% 1/4W	24773-270R
R13	Met film 680Ω 2% 1/4W	24773-269K
R14	Met film 27Ω 2% 1/4W	24773-235R
R15	Met film 75Ω 2% 1/4W	24773-246Y
R16	Met film 10Ω 2% 1/4W	24773-225W
R17	Met film 10Ω 2% 1/4W	24773-225W
T1	Transformer	43590-031A

Circuit ref.	Description	Code no.
TR1	2N5179	28451-697Y
TR2	2N5179	28451-697Y
TR3	2N5179	28451-697Y
14.	Board AA3 - Power amp. and a.l.c. detector	
	When ordering prefix with AA3.	
	Complete board	44827-788M
C1	Elec 100µF +100-20% 25V	26423-243M
C2	Elec 100µF +100-20% 25V	26423-243M
C3	Elec 220µF +100-20% 10V	26423-251A
C4	Elec 47µF +100-20% 25V	26423-231F
C5	Elec 100µF +100-20% 25V	26423-243M
C6	Elec 47µF +100-20% 25V	26423-231F
C7	Cer 0.047µF +80-20% 25V	26383-017U
C8	Plas 0.1µF 10% 100V	26582-211B
C9	Cer 10pF ±0.5pF 63V	26343-465H
C10	Cer 10pF ±0.5pF 63V	26343-465H
C11	Cer 2.2pF ±0.5pF 63V	26343-457R
C12	Cer 10pF ±0.5pF 63V	26343-465H
C14	Cer 27pF 5% 63V	26343-470U
C15	Cer 270pF 2% 63V	26343-482W
C16	Cer 0.0047µF 10% 63V	26383-591B

Board AA3 - Power amp. and a.l.c. detector (contd.)

Circuit ref.	Description	Code no.
C17	Plas 0.47µF 10% 63V	26582-402V
C18	Cer 0.001µF +80-20% 500V	26383-242P
C19	Cer 0.001µF +80-20% 500V	26383-242P
C20	Cer 0.001µF +80-20% 500V	26383-242P
C21	Cer 0.001µF +80-20% 500V	26383-242P
C22	Cer 0.001µF +80-20% 500V	26383-242P
C23	Tant 2.2µF 20% 20V	26486-540K
C25	Cer 0.047µF +80-20% 25V	26383-017U
C26	Cer 0.047µF +80-20% 25V	26383-017U
C28	Var. plas 0.25pF-8pF	26876-031L
C29	Cer 10pF ±0.5pF 63V	26343-465H
D3,4	Matched set	44529-045A
D5	1N4148	28336-676J
D6	1N4148	28336-676J
D7	1N4148	28336-676J
D8	1N4148	28336-676J
D9	1N4148	18336-676J
IC1	µA741C	28461-304T
IC2	µA741C	28461-304T
IC3	µA741C	28461-304T
L1	Inductor	44290-601W
L2	Inductor	44290-601W
L3	Inductor	44290-741P

Circuit ref.	Description	Code no.
R1	Met film 75Ω 2% 1/4W	24773-246Y
R2	Met film 10Ω 2% 1/4W	24773-225W
R3	Met film 750Ω 2% 1/4W	24773-270R
R4	Met film 820Ω 2% 1/4W	24773-271B
R5	Met film 4.3kΩ 2% 1/4W	24773-288S
R6	Met film 1.2kΩ 2% 1/4W	24773-275H
R7	Met film 22Ω 2% 1/4W	24773-233M
R8	Met film 75Ω 2% 1/4W	24773-246Y
R9	Met film 1.1kΩ 2% 1/4W	24773-274Z
R10	Met film 10Ω 2% 1/4W	24773-225W
R11	Met film 10Ω 2% 1/4W	24773-225W
R12	Met film 6.8kΩ 2% 1/4W	24773-293D
R13	Met film 820Ω 2% 1/4W	24773-271B
R14	Met film 1.5kΩ 2% 1/4W	24773-277U
R15	Met film 1.2kΩ 2% 1/4W	24773-275H
R16	Met film 180Ω 2% 1/4W	24773-255V
R17	Met film 82Ω 2% 1/4W	24773-247N
R18	Met film 39Ω 2% 1/4W	24773-239Z
R19	Met film 75Ω 0.25% 1/4W	24732-313V
R20	Met film 47kΩ 2% 1/4W	24773-313H
R21	Met film 35.2kΩ 0.1% 1/4W	24723-350K
R22	Met film 675kΩ 0.1% 1/4W	24723-352Z
R23	Met film 675kΩ 0.1% 1/4W	24723-352Z
R24	Met film 35.2kΩ 0.1% 1/4W	24723-350K
R25	Met film 10kΩ 2% 1/4W	24773-297M

Circuit ref.	*Description*	*Code no.*
	Board AA3 - Power amp. and a.l.c. detector (contd.)	
R26	Met film 470kΩ 2% 1/4W	24773-337R
R27	Met film 100Ω 2% 1/4W	24773-249J
R28	Met film 2.4kΩ 2% 1/4W	24773-282N
R29	Met film 7.5kΩ 2% 1/4W	24773-294T
R30	Var cermet 1kΩ 10% 1/2W	25711-503F
R31	Var cermet 220Ω 10% 1/2W	25711-501L
R32	Met film 12kΩ 2% 1/4W	24773-299R
R33	Met film 100kΩ 2% 1/4W	24773-321L
R36	Met film 1.5kΩ 2% 1/4W	24773-277U
R37	Met film 39Ω 2% 1/4W	24773-239Z
R38	Met film 82Ω 2% 1/4W	24773-247N
R39	Met film 680Ω 2% 1/4W	24773-269K
R40	Met film 47Ω 2% 1/4W	24773-241A
R41	Met film 120Ω 2% 1/4W	24773-251L
R42	Var cermet 100Ω 10% 1/2W	25711-507W
R43	Met film 2.7kΩ 2% 1/4W	24773-283L
R44	Met film 1.5kΩ 2% 1/4W	24773-277U
R45	Met film 820Ω 2% 1/4W	24773-271B
R46†	Met film 390kΩ 2% 1/4W	24773-335M
R47	Met film 1.3kΩ 2% 1/4W	24773-276E
R48	Met film 10kΩ 2% 1/4W	24773-297M
TR1	BFY90	28452-157R
TR2	BFY90	28452-157R
TR3	BFY90	28452-157R
TR4	BFY90	28452-157R
X1	Ferrite bead	23635-812H

15. Board AA4 - ALC controller

When ordering prefix with AA4.

	Complete assembly	44827-789C
C1	Plas 0.47µF 10% 100V	26582-215H
C2	Plas 0.33µF 10% 63V	26582-408X
C3	Plas 0.47µF 10% 100V	26582-215H
C4	Cer 100pF 2% 63V	26343-477V
C5	Elec 47µF +100-20% 10V	26415-809E
C6	Elec 47µF +100-20% 10V	26415-809E
C7	Plas 0.47µF 10% 100V	26582-215H
C8	Plas 0.01µF 10% 250V	26582-202T
C9	Plas 0.01µF 10% 250V	26582-202T
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
IC1	µA741C	28461-304T
IC2	µA741C	28461-304T

Circuit ref.	Description	Code no.
	Board AA4 - ALC controller (contd.)	
IC3	µA741C	28461-304T
IC4	µA741C	28461-304T
IC5 ⚠	CD4042	28462-404A
IC6 ⚠	CD4066	28469-383S
IC7 ⚠	CD4066	28469-383S
R1	Met film 270kΩ 2% 1/4W	24773-331D
R2	Met film 220kΩ 2% 1/4W	24773-329T
R3	Met film 150kΩ 2% 1/4W	24773-325V
R4	Met film 10kΩ 0.1% 1/4W	24723-348A
R5	Met film 7.5kΩ 0.1% 1/4W	24723-345R
R6	Met film 400Ω 0.25% 1/4W	24732-373L
R7	Met film 4.66kΩ 0.1% 1/4W	24723-344C
R8	Met film 30kΩ 2% 1/4W	24773-308A
R9	Met film 30kΩ 2% 1/4W	24773-308A
R10	Met film 150kΩ 2% 1/4W	24773-325V
R11	Carb film 10MΩ 10% 1/8W	24321-885W
R12	Met film 10kΩ 2% 1/4W	24773-297M
R13	Met film 10kΩ 2% 1/4W	24773-297M
R14	Met film 12kΩ 2% 1/4W	24773-299R
R15	Met film 3kΩ 2% 1/4W	24773-284J
R16	Met film 1kΩ 2% 1/4W	24773-273A
R17	Met film 30kΩ 2% 1/4W	24773-308A
R18	Met film 150kΩ 2% 1/4W	24773-325V
R19	Carb film 1MΩ 5% 1/8W	24311-945Y
R20	Carb film 1MΩ 5% 1/8W	24311-945Y
R21	Carb film 1MΩ 5% 1/8W	24311-945Y
R22	Carb film 1MΩ 5% 1/8W	24311-945Y
R23	Carb film 1MΩ 5% 1/8W	24311-945Y
R24	Met film 150Ω 2% 1/4W	24773-253F
R25	Met film 220kΩ 2% 1/4W	24773-329T
R26	Var cermet 4.7kΩ 10% 1/2W	25711-542W
T1	Transformer	43590-031A
16.	Board AA5 - Programmable attenuator	
	When ordering prefix with AA5.	
	Complete assembly	44827-790X
C7	Cer 0.01µF +80-20% 100V	26383-055L
L1	Inductor	44290-719E
L2	Inductor	44290-719E
R4	Met film 4.7kΩ 2% 1/4W	24773-289W
R7	Met film 78.86Ω 0.1% 1/4W	24723-378B
R8	Met film 1.492kΩ 0.1% 1/4W	24723-377R
R9	Met film 78.86Ω 0.1% 1/4W	24723-378B

Circuit ref.	Description	Code no.
	Board AA5 - Programmable attenuator (contd.)	
RLA	Latching relay	23486-106D
RLB	Latching relay	23486-106D
T1	Transformer	43590-045V
17.	Board AA6 - Programmable attenuator	
	When ordering prefix with AA6.	
	Complete assembly	44827-791M
C1	Elec 220µF +100-20% 10V	26415-817J
C2	Elec 220µF +100-20% 10V	26415-817J
C9	Cer 0.01µF +80-20% 100V	26383-055L
C10	Cer 0.01µF +80-20% 100V	26383-055L
C13	Cer 0.047µF +80-20% 25V	26383-017U
C14	Cer 0.047µF +80-20% 25V	26383-017U
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4148	28336-676J
D6	1N4148	28336-676J

Circuit ref.	Description	Code no.
IC1 ⚠	CD4016	28469-364K
IC2 ⚠	CD4042	28462-404A
L1	Inductor	44290-720Z
L2	Inductor	44290-720Z
R1	Met film 220kΩ 2% 1/4W	24773-329T
R2	Met film 103.3Ω 0.1% 1/4W	24723-382K
R3	Met film 230.7Ω 0.1% 1/4W	24723-379K
R4	Met film 103.3Ω 0.1% 1/4W	24723-382K
R5	Met film 15kΩ 2% 1/4W	24773-301P
R6	Met film 15kΩ 2% 1/4W	24773-301P
R7	Met film 91.67Ω 0.1% 1/4W	24723-381B
R8	Met film 371.3Ω 0.1% 1/4W	24723-380R
R9	Met film 91.67Ω 0.1% 1/4W	24723-381B
R10	Met film 15kΩ 2% 1/4W	24773-301P
R11	Met film 220kΩ 2% 1/4W	24773-329T
RLA	Latching relay	23486-106D
RLB	Latching relay	23486-106D
RLC	Latching relay	23486-106D
RLD	Latching relay	23486-106D
T1	Transformer	43590-045V

Circuit ref.	*Description*	*Code no.*
	Board AA6 - Programmable attenuator (contd.)	
TR1	BC238	28452-781A
TR2	BC308	28433-455R
TR3	BC238	28452-781A
TR4	BC308	28433-455R
TR5	BC238	28452-781A
TR6	BC308	28433-455R
18.	Board AA7 - Programmable attenuator	
	When ordering prefix with AA7.	
	Complete assembly	44827-792C
C4	Cer 0.047µF +80-20% 25V	26383-017U
C5	Cer 0.047µF +80-20% 25V	26383-017U
C10	Cer 0.01µF +80-20% 100V	26383-055L
C11	Cer 0.01µF +80-20% 100V	26383-055L
C12	Cer 0.01µF +80-20% 100V	26383-055L
C13	Cer 0.01µF +80-20% 100V	26383-055L
C15	Cer 15pF 5% 63V	26343-467U
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4148	28336-676J
D6	1N4148	28336-676J
IC1 ⚠	CD4016	28469-364K
L1	Inductor	34900-510Y
L2	Inductor	34900-450S
L3	Inductor	34900-509L
L4	Inductor	34900-509L
R1	Met film 1.304kΩ 0.25% 1/4W	24732-374J
R2	Met film 8.65Ω 0.25% 1/4W	24732-375F
R3	Met film 1.304kΩ 0.25% 1/4W	24732-374J
R4	Met film 220kΩ 2% 1/4W	24773-329T
R5	Met film 8.60Ω 0.25% 1/4W	24732-376G
R6	Met film 322.9Ω 0.1% 1/4W	24723-387U
R7	Met film 8.60Ω 0.25% 1/4W	24732-376G
R8	Met film 15kΩ 2% 1/4W	24773-301P
R9	Met film 15kΩ 2% 1/4W	24773-301P
R10	Met film 15kΩ 2% 1/4W	24773-301P
R11	Met film 15kΩ 2% 1/4W	24773-301P
R12	Met film 16.97Ω 0.1% 1/4W	24723-384Z
R13	Met film 157.2Ω 0.1% 1/4W	24723-385H
R14	Met film 16.97Ω 0.1% 1/4W	24723-384Z
R15	Met film 174.2Ω 0.1% 1/4W	24723-386E
R16	Met film 79.27Ω 0.1% 1/4W	24723-383A
R17	Met film 174.2Ω 0.1% 1/4W	24723-386E

Circuit ref.	Description	Code no.
	Board AA7 - Programmable attenuator (contd.)	
RLA	Latching relay	23486-106D
RLB	Latching relay	23486-106D
RLC	Latching relay	23486-106D
RLD	Latching relay	23486-106D
RLE	Latching relay	23486-106D
RLF	Latching relay	23486-106D
RLG	Latching relay	23486-106D
RLH	Latching relay	23486-106D
T1	Transformer	43590-045V
TR1	BC238	28452-781A
TR2	BC308	28433-455R
TR3	BC238	28452-781A
TR4	BC308	28433-455R
TR5	BC238	28452-781A
TR6	BC308	28433-455R
19.	Board AA8 - Unbalanced matching	
	When ordering prefix with AA8.	
	Complete board	44827-793R
C1	Elec 100µF +100-20% 25V	26415-813U
C2	Elec 100µF +100-20% 25V	26415-813U
C3	Cer 0.01µF +80-20% 100V	26383-055L
C4	Cer 0.01µF +80-20% 100V	26383-055L
C5	Cer 0.01µF +80-20% 100V	26383-055L
C6	Cer 0.01µF +80-20% 100V	26383-055L
C7	Cer 0.01µF +80-20% 100V	26383-055L
C8	Cer 0.01µF +80-20% 100V	26383-055L
C9	Cer 18pF 5% 63V	26343-468Y
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4148	28336-676J
D6	1N4148	28336-676J
D7	1N4148	28336-676J
D8	1N4148	28336-676J
D9	1N4148	28336-676J
IC1 ⚠	4042	28462-404A
L1	Inductor	44290-741P
R1	Carb film 1MΩ 5% 1/8W	24311-945Y
R2	Carb film 1MΩ 5% 1/8W	24311-945Y
R3	Carb film 1MΩ 5% 1/8W	24311-945Y
R4	Carb film 1MΩ 5% 1/8W	24311-945Y
R5	Met film 100kΩ 2% 1/4W	24773-321L

Circuit ref.	Description	Code no.
	Board AA8 - Unbalanced matching (contd.)	
R6	Met film 15kΩ 2% 1/4W	24773-301P
R7	Met film 10kΩ 2% 1/4W	24773-297M
R8	Met film 10kΩ 2% 1/4W	24773-297M
R9	Met film 15kΩ 2% 1/4W	24773-301P
R10	Met film 100Ω 2% 1/4W	24773-249J
R11	Met film 100Ω 2% 1/4W	24773-249J
R14	Met film 37.5Ω 1% 1/4W	24762-529A
R15	Met film 6.2Ω 2% 1/4W	24773-220J
R16	Met film 68.7Ω 0.1% 1/4W	24723-322E
R17	Met film 14.97Ω 0.25% 1/4W	24732-392R
R18	Met film 6.8Ω 2% 1/4W	24773-221F
RLA	Relay	23486-104S
RLB	Relay	23486-104S
RLC	Relay	23486-104S
RLD	Relay	23486-104S
RLE	Relay	23486-104S
T1	Transformer	43590-045V
TR1	ZTX108BL	28452-781A
TR2	ZTX108BL	28452-781A
TR3	ZTX108BL	28452-781A
TR4	ZTX108BL	28452-781A

Circuit ref.	Description	Code no.
20.	Board AA9 - Balanced matching buffer	
	When ordering prefix with AA9.	
	Complete board	44827-794B
C1	Cer 0.047µF +80-20% 25V	26383-017U
C2	Cer 0.047µF +80-20% 25V	26383-017U
C3	Elec 47µF +100-20% 10V	26415-809E
C4	Plas 0.1µF 10% 100V	26582-211B
C5	Elec 47µF +100-20% 10V	26415-809E
C6	Plas 0.1µF 10% 100V	26582-211B
C7	Elec 47µF +100-20% 10V	26415-809E
C8	Cer 0.047µF +80-20% 25V	26383-017U
C9	Plas 0.1µF 10% 100V	26582-211B
C10	Tant 47µF 20% 20V	26486-594T
C11	Cer 100pF 2% 63V	26343-477V
C12	Cer 0.047µF +80-20% 25V	26383-017U
C13	Cer 3.3pF ±0.5pF 63V	26343-459K
C14	Cer 2.2pF ±0.5pF 63V	26343-457R
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4148	28336-676J

Circuit ref.	Description	Code no.
	Board AA9 - Balanced matching buffer (contd.)	
D6	1N4148	28336-676J
IC1 ⚠	CD4042	28462-404A
R1	Met film 220kΩ 2% 1/4W	24773-329T
R2	Carb film 1MΩ 5% 1/8W	24311-945Y
R3	Carb film 1MΩ 5% 1/8W	24311-945Y
R4	Carb film 1MΩ 5% 1/8W	24311-945Y
R5	Carb film 1MΩ 5% 1/8W	24311-945Y
R6	Carb film 1MΩ 5% 1/8W	24311-945Y
R7	Met film 4.7Ω 2% 1/4W	24773-217J
R8	Met film 22Ω 2% 1/4W	24773-233M
R9	Met film 3.0Ω 2% 1/4W	24773-212E
R10	Met film 2.4Ω 2% 1/4W	24773-210Z
R11	Met film 23.8Ω 0.1% 1/4W	24723-353H
R12	Carb film 1MΩ 5% 1/8W	24311-945Y
R13	Carb film 1MΩ 5% 1/8W	24311-945Y
R14	Carb film 1MΩ 5% 1/8W	24311-945Y
R15	Carb film 1MΩ 5% 1/8W	24311-945Y
R16	Var cermet 47Ω 20% 1/2W	25711-513P
R17	Met film 180Ω 2% 1/4W	24773-255V
R18	Met film 220Ω 2% 1/4W	24773-257W
R19	Met film 360Ω 2% 1/4W	24773-262T
R20	Met film 3.3Ω 2% 1/4W	24773-213U
R21	Met film 10Ω 2% 1/4W	24773-225W
R22	Met film 470Ω 2% 1/4W	24773-265M
R23	Met film 820Ω 2% 1/4W	24773-271B
R24	Met film 10Ω 2% 1/4W	24773-225W
R25	Met film 10Ω 2% 1/4W	24773-225W
R26	Met film 10Ω 2% 1/4W	24773-225W
R27	Met film 10Ω 2% 1/4W	24773-225W
R28	Met film 22kΩ 2% 1/4W	24773-305R
R29	Met film 2.2Ω 2% 1/4W	24773-209E
R30	Met film 42.2Ω 0.1% 1/4W	24723-319E
R31	Met film 47Ω 2% 1/4W	24773-241A
R32	Met film 10Ω 2% 1/4W	24773-225W
TR1	TIS74	28459-016X
TR2	TIS74	28459-016X
TR3	TIS74	28459-016X
TR4	TIS74	28459-016X
TR5	BFR99	28433-336F
TR6	BSX20	28452-197H
TR7	2N2905	28434-879X
TR8	2N2219	28453-847F
X1	Ferrite bead	23635-812H

Circuit ref.	*Description*	*Code no.*
21.	Board AA10 - Balanced matching	
	When ordering prefix with AA10.	
	Complete board	44827-795K
C1	Cer 0.01µF +80-20% 100V	26383-055L
C2	Elec 47µF +100-20% 10V	26415-809E
C3	Cer 0.01µF +80-20% 100V	26383-055L
C4	Elec 47µF +100-20% 10V	26415-809E
C5	Cer 0.01µF +80-20% 100V	26383-055L
C6	Cer 0.01µF +80-20% 100V	26383-055L
C7	Cer 0.01µF +80-20% 100V	26383-055L
C8	Cer 0.01µF +80-20% 100V	26383-055L
C9	Cer 120pF 2% 63V	26343-478S
C10	Cer 33pF 5% 63V	26343-471Y
C11†	Var cer. 10-60pF	26847-267D
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4148	28336-676J
IC1 ⚠	CD4042	28462-404A

Circuit ref.	*Description*	*Code no.*
R1	Carb film 1MΩ 5% 1/8W	24311-945Y
R2	Carb film 1MΩ 5% 1/8W	24311-945Y
R3	Met film 15kΩ 2% 1/4W	24773-301P
R4	Carb film 1MΩ 5% 1/8W	24311-945Y
R5	Met film 220kΩ 2% 1/4W	24773-329T
R6	Met film 47kΩ 2% 1/4W	24773-313H
R7	Met film 47kΩ 2% 1/4W	24773-313H
R9	Met film 47kΩ 2% 1/4W	24773-313H
R10	Met film 132.1Ω 0.1% 1/4W	24723-354E
R11	Met film 6.8Ω 0.5% 1/4W	24753-550B
R12	Met film 75Ω 2% 1/4W	24773-246Y
R13	Met film 620Ω 2% 1/4W	24773-268B
R14	Met film 330Ω 2% 1/4W	24773-261D
R15	Met film 330Ω 2% 1/4W	24773-261D
R16	Met film 620Ω 2% 1/4W	24773-268B
R17	Met film 75Ω 2% 1/4W	24773-246Y
R18	Met film 5.1kΩ 2% 1/4W	24773-290V
R19	Met film 6.8Ω 0.5% 1/4W	24753-550B
RLA	Latching	23486-106D
RLB	Reed	23486-446W
RLC	Reed	23486-446W
RLD	Reed	23486-446W
RLE	Reed	23486-446W

Circuit ref.	Description	Code no.
	Board AA10 - Balanced matching (contd.)	
RLF	Reed	23486-446W
RLG	Reed	23486-446W
T1	Transformer	43590-080V
TR1	BC238	28452-781A
TR2	BC238	28452-781A
TR3	BC238	28452-781A
TR4	BC238	28452-781A
TR5	BC308	28433-455R
22.	Board AA11 - Frequency multiplier	
	When ordering prefix with AA11.	
	Complete board	44827-818W
C1	Cer 0.01µF +80-20% 100V	26383-055L
C2	Cer 0.001µF +80-20% 500V	26383-242P
C4	Cer 0.001µF +80-20% 500V	26383-242P
C6	Cer 330pF 2% 63V	26343-483D
C7	Cer 0.047µF +80-20% 25V	26383-017U
C9	Cer 0.001µF +80-20% 500V	26383-242P
C10	Cer 0.01µF +80-20% 100V	26383-055L
C11	Plas 556pF 2% 63V	26538-622L
D1	1N4148	28336-676J

Circuit ref.	Description	Code no.
IC1	CA3046	28461-901A
L1	Inductor	44290-546H
L2	Inductor	44290-547E
R1	Met film 100Ω 2% 1/4W	24773-249J
R2	Met film 620Ω 2% 1/4W	24773-268B
R3	Met film 100Ω 2% 1/4W	24773-249J
R4	Met film 1kΩ 2% 1/4W	24773-273A
R5	Met film 10kΩ 2% 1/4W	24773-297M
R6	Met film 10kΩ 2% 1/4W	24773-297M
R7	Met film 39kΩ 2% 1/4W	24773-311A
R8	Met film 5.1kΩ 2% 1/4W	24773-290V
R9	Met film 100Ω 2% 1/4W	24773-249J
R10	Met film 10kΩ 2% 1/4W	24773-297M
R11	Met film 10kΩ 2% 1/4W	24773-297M
R12	Met film 270Ω 2% 1/4W	24773-259T
R13	Met film 3.9kΩ 2% 1/4W	24773-287V
R14	Met film 100Ω 2% 1/4W	24773-249J
R15	Met film 560Ω 2% 1/4W	24773-267R
R16	Carb film 1MΩ 5% 1/8W	24311-945Y
T1	Transformer	43590-032Z
T2	Transformer	43590-032Z

Circuit ref.	Description	Code no.
	Board AA11 - Frequency multiplier (contd.)	
TR1	BSX20	28452-197H
TR2	BSX20	28452-197H
TR3	TIS74	28459-016X
23.	Board AA12 - Fine level control	
	When ordering prefix with AA12.	
	Complete board	44827-997R
C1	Plas 0.47µF 10% 100V	26582-215H
C2	Elec 47µF +100-20% 10V	26415-809E
C3	Elec 47µF +100-20% 10V	26415-809E
C4	Plas 0.01µF 10% 250V	26582-202T
C5	Plas 0.01µF 10% 250V	26582-202T
IC1 ⚠	CD4042	28462-404A
IC2 ⚠	CD4042	28462-404A
IC3 ⚠	CD4049	28469-162Z
IC4 ⚠	CD4049	28469-162Z
IC5	µA741C	28461-304T
IC6	µA741C	28461-304T
R1	Carb film 1MΩ 5% 1/8W	24311-945Y
R2	Carb film 1MΩ 5% 1/8W	24311-945Y
R3	Carb film 1MΩ 5% 1/8W	24311-945Y
R4	Carb film 1MΩ 5% 1/8W	24311-945Y
R5	Carb film 1MΩ 5% 1/8W	24311-945Y
R6	Carb film 1MΩ 5% 1/8W	24311-945Y
R7	Met film 150kΩ 2% 1/4W	24773-325V
R8	Met film 150kΩ 2% 1/4W	24773-325V
R9	Met film 75kΩ 2% 1/4W	24773-318L
R10	Met film 150kΩ 2% 1/4W	24773-325V
R11	Met film 75kΩ 2% 1/4W	24773-318L
R12	Met film 150kΩ 2% 1/4W	24773-325V
R13	Met film 75kΩ 2% 1/4W	24773-318L
R14	Met film 150kΩ 2% 1/4W	24773-325V
R15	Met film 675kΩ 0.1% 1/4W	24723-352Z
R16	Met film 150kΩ 2% 1/4W	24773-325V
R17	Met film 150kΩ 2% 1/4W	24773-325V
R18	Met film 75kΩ 2% 1/4W	24773-318L
R19	Met film 150kΩ 2% 1/4W	24773-325V
R20	Met film 75kΩ 0.5% 1/4W	24753-541T
R21	Met film 150kΩ 0.5% 1/4W	24753-542P
R22	Met film 75kΩ 0.5% 1/4W	24753-541T
R23	Met film 150kΩ 0.5% 1/4W	24753-542P
R24	Var cermet 1kΩ 10% 1/2W	25711-503F
R25	Met film 35.2kΩ 0.1% 1/4W	24723-350K
R26	Met film 8.59kΩ 0.1% 1/4W	24723-346B
R27	Met film 1.13kΩ 0.1% 1/4W	24723-342X
R28	Met film 1.5kΩ 0.1% 1/4W	24723-302S

Circuit ref.	Description	Code no.
	Board AA12 - Fine level control (contd.)	
R29	Met film 33.5kΩ 0.1% 1/4W	24723-349Z
R30	Met film 8.72kΩ 0.1% 1/4W	24723-347K
R31	Met film 78.8kΩ 0.1% 1/4W	24723-351A
R32	Met film 2.37kΩ 0.1% 1/4W	24723-343M
R34	Met film 330kΩ 2% 1/4W	24773-333P
R35	Var cermet 100kΩ 10% 1/2W	25711-511D
24.	Board AB1 - ±7.5 voltage regulator	
	When ordering prefix with AB1.	
	Complete board	44827-838U
C1	Elec 220µF +100-20% 10V	26415-817J
C2	Elec 220µF +100-20% 10V	26415-817J
C3	Elec 220µF +100-20% 10V	26415-817J
C4	Cer 0.01µF +80-20% 100V	26383-055L
D1	1N825	28371-494Z
IC1	µA741C	28461-034T
IC2	µA741C	28461-034T
R1	Met film 75Ω 2% 1/4W	24773-246Y
R2	Met film 47kΩ 2% 1/4W	24773-313H
R3	Met film 3.3kΩ 2% 1/4W	24773-285F
R5	Var cermet 220kΩ 10% 1/2W	25711-551C
R6	Met film 10kΩ 2% 1/4W	24773-297M
R7	Met film 1.8kΩ 2% 1/4W	24773-279N
R8	Var cermet 470Ω 10% 1/2W	25711-541S
R14	Var cermet 220kΩ 10% 1/2W	25711-551C
R15	Met film 3.3kΩ 2% 1/4W	24773-285F
R16	Met film 47kΩ 2% 1/4W	24773-313H
R19	Met film 10kΩ 0.25% 1/4W	24732-304Y
R20	Met film 10kΩ 0.25% 1/4W	24732-304Y
R21	Met film 9.1kΩ 2% 1/4W	24773-296X
R22	Met film 9.1kΩ 2% 1/4W	24773-296X
TR1	2N3055	28456-567W
TR2	2N2905	28434-879X
TR3	BC108	28452-787W
TR6	BCY72	28433-487R
TR7	BCY72	28433-487R
TR9	BFY51	28455-827T
TR10	MJ491	28435-876Z
25.	Board AB2 - Microprocessor	
	When ordering prefix with AB2.	
	Complete board	44827-839Y

Board AB2 - Microprocessor (contd.)

Circuit ref.	Description	Code no.
C1	Elec 100µF +100-20% 25V	26415-813U
C2	Elec 100µF +100-20% 25V	26415-813U
C3	Cer 0.01µF +80-20% 100V	26383-055L
C4	Cer 0.01µF +80-20% 100V	26383-055L
C5	Cer 33pF 5% 63V	26343-471Y
C6	Cer 33pF 5% 63V	26343-471Y
C7	Plas 0.22µF 10% 63V	26582-406T
C8	Cer 0.01µF +80-20% 100V	26383-055L
C9	Cer 0.01µF +80-20% 100V	26383-055L
C10	Cer 0.01µF +80-20% 100V	26383-055L
C11	Cer 0.01µF +80-20% 100V	26383-055L
C12	Cer 0.01µF +80-20% 100V	26383-055L
C13	Cer 0.01µF +80-20% 100V	26383-055L
C14	Cer 0.01µF +80-20% 100V	26383-055L
C15	Cer 0.01µF +80-20% 100V	26383-055L
C16	Cer 0.047µF +80-20% 25V	26383-017U
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
IC1 ⚠	CD4201	28469-374N
IC2 ⚠	CD4040	28469-376J
IC3 ⚠	CD4289	28469-375L
IC4 ⚠	CD14028	28465-023Y
IC5 ⚠	CD4002-1	28469-303H
IC6 ⚠	CD4002-1	28469-303H
IC7 ⚠	CD4049	28469-162Z
IC8 ⚠	CD4049	28469-162Z
IC9 ⚠	CD4042	28462-404A
IC10 ⚠	CD4042	28462-404A
IC11 ⚠	CD4042	28462-404A
IC12 ⚠	CD4042	28462-404A
L1	RF choke	23642-561W
L2	RF choke	23642-561W
R1	Met film 100Ω 2% 1/4W	24773-249J
R2	Met film 100Ω 2% 1/4W	24773-249J
R3	Met film 10kΩ 2% 1/4W	24773-297M
R4	Carb 1MΩ 5% 1/8W	24311-945Y
R5	Met film 10Ω 2% 1/4W	24773-225W
R6	Met film 27kΩ 2% 1/4W	24773-307K
R7	Met film 27kΩ 2% 1/4W	24773-307K
R8	Met film 10kΩ 2% 1/4W	24773-297M
R9	Met film 100kΩ 2% 1/4W	24773-321L
R10	Met film 100kΩ 2% 1/4W	24773-321L
R11	Met film 100kΩ 2% 1/4W	24773-321L
R12	Met film 100kΩ 2% 1/4W	24773-321L
R13	Met film 100kΩ 2% 1/4W	24773-321L
R14	Met film 100kΩ 2% 1/4W	24773-321L
R15	Met film 100kΩ 2% 1/4W	24773-321L

Circuit ref.	*Description*	*Code no.*
	Board AB2 - Microprocessor (contd.)	
R16	Met film 100kΩ 2% 1/4W	24773-321I
R17	Met film 100kΩ 2% 1/4W	24773-321L
R18	Met film 100kΩ 2% 1/4W	24773-321L
R19	Met film 100Ω 2% 1/4W	24773-249J
R20	Met film 10Ω 2% 1/4W	24773-225W
R21	Met film 10Ω 2% 1/4W	24773-225W
R22	Met film 10Ω 2% 1/4W	24773-225W
R23	Met film 10Ω 2% 1/4W	24773-225W
R24	Met film 10Ω 2% 1/4W	24773-225W
R25	Met film 10Ω 2% 1/4W	24773-225W
R26	Met film 10Ω 2% 1/4W	24773-225W
R27	Met film 18kΩ 2% 1/4W	24773-303M
R28	Met film 6.8kΩ 2% 1/4W	24773-293D
R29	Met film 6.8kΩ 2% 1/4W	24773-293D
XL1	5.185MHz	28312-053L
26.	Board AB3 - Memory	
	When ordering, prefix with AB3.	
	Complete board	44827-840E
C1	Cer 0.01µF +80-20% 100V	26383-055L
C2	Cer 0.01µF +80-20% 100V	26383-055L
C3	Cer 0.01µF +80-20% 100V	26383-055L

Circuit ref.	*Description*	*Code no.*
C4	Cer 0.01µF +80-20% 100V	26383-055L
C5	Cer 0.01µF +80-20% 100V	26383-055L
C6	Cer 0.01µF +80-20% 100V	26383-055L
C7	Cer 0.01µF +80-20% 100V	26383-055L
C9	Tant 68µF 20% 15V	26486-597M
C10	Tant 47µF 20% 6V	26486-593D
C11	Tant 47µF 20% 6V	26486-593D
C12	Cer 0.01µF +80-20% 100V	26383-055L
D1	Zener 3V	28371-203G
IC2 ⚠	CD4556	28465-021E
IC4 ⚠	CD4093	28469-203U
IC6 ⚠	CD4016	28469-364K
IC7 ⚠	CD4016	28469-364K
IC9	74LS26	28466-350U
IC10	74LS26	28466-350U
IC11	Resistor network 8 x 10kΩ	24681-511P
IC12	Resistor network 15 x 4.7kΩ	24681-510T
IC13	Resistor network 8 x 10kΩ	24681-511P
IC14	Resistor network 9 x 1.8kΩ	24681-605V
	Set of 4 pre-programmed EPROMS - see Unit A0.	
L1	RF choke	23642-561W
L3	RF choke	23642-561W
L4	RF choke	23642-561W

Circuit ref.	Description	Code no.
	Board AB3 - Memory	
R4	Met film 10kΩ 2% 1/4W	24773-297M
R5	Met film 4.7kΩ 2% 1/4W	24773-289W
R6	Met film 1kΩ 2% 1/4W	24773-273A
R7	Met film 10kΩ 2% 1/4W	24773-297M
R8	Met film 10kΩ 2% 1/4W	24773-297M
R9	Met film 10kΩ 2% 1/4W	24773-297M
TR1	BSX20	28452-197H
27.	Board AB4 - Control interface	
	When ordering prefix with AB4.	
	Complete board	44827-796A
C1	Plas 0.22µF 10% 63V	26582-406T
C2	Tant 22µF 20% 15V	26486-583L
C3	Tant 22µF 20% 15V	26486-583L
IC1 ⚠	555	28468-304P
IC2 ⚠	CD4042	28462-404A
IC3 ⚠	CD4051	28469-708K
IC4 ⚠	CD4099	28462-405Z
IC5 ⚠	MC14028	28465-023Y
IC6	CA3046	28461-901A

Circuit ref.	Description	Code no.
R1	Met film 39kΩ 2% 1/4W	24773-311A
R2	Var cermet 100kΩ 10% 1/2W	25711-631E
R3	Met film 160kΩ 2% 1/4W	24773-326S
R4	Met film 160kΩ 2% 1/4W	24773-326S
R5	Met film 160kΩ 2% 1/4W	24773-326S
R6	Met film 160kΩ 2% 1/4W	24773-326S
R7	Met film 39kΩ 2% 1/4W	24773-311A
R8	Met film 160kΩ 2% 1/4W	24773-326S
R9	Met film 22kΩ 2% 1/4W	24773-305R
R10	Met film 22kΩ 2% 1/4W	24773-305R
R11	Met film 160kΩ 2% 1/4W	24773-326S
R12	Met film 160kΩ 2% 1/4W	24773-326S
R13	Met film 22kΩ 2% 1/4W	24773-305R
R14	Met film 22kΩ 2% 1/4W	24773-305R
R15	Met film 22kΩ 2% 1/4W	24773-305R
R16	Met film 39kΩ 2% 1/4W	24773-311A
R17	Met film 39kΩ 2% 1/4W	24773-311A
R18	Met film 22kΩ 2% 1/4W	24773-305R
28.	Board AB5 - Data buffer	
	When ordering prefix with AB5.	
	Complete board	44827-700A
C1	Tant 6.8µF 20% 6V	26486-560W

Circuit ref.	Description	Code no.
	Board AB5 - Data buffer (contd.)	
C2	Tant 6.8µF 20% 6V	26486-560W
C3	Tant 22µF 20% 15V	26486-583L
C4	Tant 47µF 20% 6V	26486-593D
C5	Cer 15pF 5% 63V	26343-467U
C6	Cer 15pF 5% 63V	26343-467U
C7	Cer 15pF 5% 63V	26343-467U
C8	Cer 15pF 5% 63V	26343-467U
C9	Cer 15pF 5% 63V	26343-467U
C10	Cer 15pF 5% 63V	26343-467U
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
IC1	3341	28467-518W
IC2	3341	28467-518W
IC3 ⚠	CD4013	28462-608A
IC4 ⚠	CD4013	28462-608A
IC5 ⚠	CD4019	28466-452U
IC6 ⚠	CD4019	28466-452U
IC7 ⚠	MC14028	28465-023Y
IC8 ⚠	CD4042	28462-404A
IC9 ⚠	CD4042	28462-404A
IC10 ⚠	CD4050	28469-161A
IC11 ⚠	CD4050	28469-161A
IC12	Resistor package 100kΩ	24681-508P
IC13	Resistor package 22kΩ	24681-509X
R1	Met film 100kΩ 2% 1/4W	24773-321L
R2	Met film 100kΩ 2% 1/4W	24773-321L
R3	Met film 100kΩ 2% 1/4W	24773-321L
R4	Met film 100kΩ 2% 1/4W	24773-321L
R5	Met film 100kΩ 2% 1/4W	24773-321L
R6	Met film 220kΩ 2% 1/4W	24773-329J
R7	Met film 100kΩ 2% 1/4W	24773-321L

29. Board AB6 - Address and message decoder

When ordering, prefix circuit reference with AB6.

Circuit ref.	Description	Code no.
	Complete board	44827-701Z
C1	Tant 6.8µF 20% 6V	26486-560W
C2	Tant 47µF 20% 6V	26486-593D
C3	Tant 6.8µF 20% 6V	26486-560W
C4	Cer 180pF 10% 63V	26383-594Z
C5	Cer 180pF 10% 63V	26383-594Z
C6	Tant 0.68µF 20% 35V	26486-507Z
IC1 ⚠	82S101	44535-001B
IC2 ⚠	MC14028	28465-023Y
IC3 ⚠	CD4013	28462-608A

Circuit ref.	Description	Code no.
	Board AB6 (continued)	
IC4 ⚠	CD4001	28466-207Z
IC5 ⚠	74LS02	28466-214Y
IC6 ⚠	CD4025	28466-209E
IC7	74LS27	28466-216L
IC8 ⚠	CD4001	28466-207Z
IC9 ⚠	CD4049	28469-181D
IC10 ⚠	CD4075	28466-107E
IC11 ⚠	CD4081	28466-009L
IC12	Resistor package 100kΩ	24681-508P
IC13	Resistor package 22kΩ	24681-509X
R1	Met film 4.7kΩ 2% 1/4W	24773-289W
R2	Met film 4.7kΩ 2% 1/4W	24773-289W
R3	Met film 4.7kΩ 2% 1/4W	24773-289W
R4	Met film 18kΩ 2% 1/4W	24773-303M
R5	Met film 18kΩ 2% 1/4W	24773-303M
R6	Met film 220kΩ 2% 1/4W	24773-329T
R7	Met film 220kΩ 2% 1/4W	24773-329T
R8	Met film 220kΩ 2% 1/4W	24773-329T
R9	Met film 220kΩ 2% 1/4W	24773-329T
R10	Met film 220kΩ 2% 1/4W	24773-329T
R11	Met film 220kΩ 2% 1/4W	24773-329T
R12	Met film 220kΩ 2% 1/4W	24773-329T
R13	Met film 18kΩ 2% 1/4W	24773-303M
R14	Met film 220kΩ 2% 1/4W	24773-329T
R15	Met film 220kΩ 2% 1/4W	24773-329T
R16	Met film 4.7kΩ 2% 1/4W	24773-289W
R17	Met film 220kΩ 2% 1/4W	24773-329T
R18	Met film 18kΩ 2% 1/4W	24773-303M
R19	Met film 18kΩ 2% 1/4W	24773-303M
R20	Met film 220kΩ 2% 1/4W	24773-329T
R21	Met film 100kΩ 2% 1/4W	24773-321L
R22	Met film 100kΩ 2% 1/4W	24773-321L
R23	Met film 100kΩ 2% 1/4W	24773-321L

30. Board AB7 - Interface and handshake

When ordering, prefix circuit reference with AB7.

	Complete board	44827-702H
C1	Tant 6.8µF 20% 6V	26486-560W
C2	Tant 6.8µF 20% 6V	26486-560W
C3	Tant 6.8µF 20% 6V	26486-560W
C4	Tant 6.8µF 20% 6V	26486-560W
C5	Tant 47µF 20% 6V	26486-593D
C6	Cer 180pF 10% 63V	26383-594Z
C7	Cer 180pF 10% 63V	26383-594Z
D1	1N4148	28336-676J
D2	1N4148	28336-676J

Circuit ref.		Description	Code no.
		Board AB7 - Interface and handshake (contd.)	
IC1		MC3441	28469-166Y
IC2		MC3440	28469-173F
IC3		MC3440	28469-173F
IC4		MC3441	28469-166Y
IC6	⚠	CD4011	28466-340R
IC7	⚠	CD4049	28469-162Z
IC8	⚠	CD4001	28466-207Z
IC9	⚠	CD4093	28469-203U
IC10	⚠	CD4081	28466-009L
IC11	⚠	CD4001	28466-207Z
IC12	⚠	CD4013	28462-608A
IC13		Resistor package 22kΩ	24681-509K
R1		Met film 180kΩ 2% 1/4W	24773-327W
R2		Met film 27kΩ 2% 1/4W	24773-307K
31.		Board AB8 - Mother board	
		When ordering prefix with AB8.	
		Complete board	44827-797Z
C1		Cer 0.001µF 10% 63V	26383-585M
C2		Cer 0.001µF 10% 63V	26383-585M
C3		Cer 0.001µF 10% 63V	26383-585M
C4		Cer 0.001µF 10% 63V	26383-585M

Circuit ref.	Description	Code no.
D1	Zener 6.2V	28371-482T
D2	Zener 6.2V	28371-482T
D3	Zener 8.2V	28371-672U
D4	Zener 15V	28372-302X
D5	Zener 8.2V	28371-672U
D6	Zener 6.2V	28371-482T
D7	Zener 15V	28372-302X
L1	Choke	44290-693F
L2	Choke	44290-693F
L3	Choke	44290-693F
L4	Choke	44290-693F
L5	Choke	44290-693F
L6	Choke	44290-693F
L7	Choke	44290-693F
R1	Met film 4.7kΩ 2% 1/4W	24773-289W
SKA	16-way	28488-041E
SKB	24-way	28488-044N
SKC	16-way	28488-041E
SKE	16-way	28488-041E
SKF	14-way	28488-040H
SKG	14-way	28488-040H
SKH	14-way	28488-040H
	37-way, single-sided (1 of 6)	23435-137B
	37-way, double-sided (1 of 5)	23435-131T

32. Board AB9 - Keyboard

When ordering, prefix circuit reference with AB9.

Circuit ref.	Description	Code no.
	Complete board	44827-798H
C1	Plas 820pF 2% 63V	26538-658V
C2	Cer 0.1µF +50-25% 30V	26383-031S
C3	Cer 0.1µF +50-25% 30V	26383-031S
C4	Cer 0.1µF +50-25% 30V	26383-031S
C5	Cer 0.1µF +50-25% 30V	26383-031S
C6	Cer 0.1µF +50-25% 30V	26383-031S
C7	Cer 0.1µF +50-25% 30V	26383-031S
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D6	1N4148	28336-676J
D7	1N4148	28336-676J
D8	1N4148	28336-676J
D9	1N4148	28336-676J
D10	1N4148	28336-676J
D11	1N4148	28336-676J
D12	1N4148	28336-676J
D13	1N4148	28336-676J
D14	1N4148	28336-676J
D15	1N4148	28336-676J
D16	1N4148	28336-676J
D17	1N4148	28336-676J
D18	1N4148	28336-676J
D19	1N4148	28336-676J
D20	1N4148	28336-676J
D21	1N4148	28336-676J
D22	1N4148	28336-676J
D23	1N4148	28336-676J
D24	1N4148	28336-676J
D25	1N4148	28336-676J
D26	1N4148	28336-676J
D27	1N4148	28336-676J
D30	1N4148	28336-676J
D31	1N4148	28336-676J
D32	1N4148	28336-676J
D33	1N4148	28336-676J
IC1 ⚠	CD4511	28465-014K
IC2 ⚠	CD4070	28466-402T
IC3 ⚠	CD4001	28466-207Z
IC4 ⚠	CD4047	28468-307C
IC5 ⚠	CD4042	28462-404A
IC6 ⚠	CD4028	28465-013B

Circuit ref.	Description	Code no.
	Board AB9 - Keyboard (contd.)	
IC7 ⚠	CD4028	28465-013B
IC8 ⚠	CD4050	28469-161A
IC9 ⚠	CD4050	28469-161A
IC11 ⚠	CD4013	28462-608A
IC12 ⚠	CD4029	28464-009G
IC13 ⚠	CD4029	28464-009G
IC14 ⚠	CD4016	28469-364K
IC16 ⚠	CD4016	28469-364K
R1	Met film 100kΩ 2% 1/4W	24773-321L
R2	Met film 100kΩ 2% 1/4W	24773-321L
R3	Met film 100kΩ 2% 1/4W	24773-321L
R4	Met film 100kΩ 2% 1/4W	24773-321L
R5	Met film 24kΩ 2% 1/4W	24773-306B
R6	Met film 100kΩ 2% 1/4W	24773-321L
R7	Met film 100kΩ 2% 1/4W	24773-321L
R8	Met film 100kΩ 2% 1/4W	24773-321L
R9	Met film 100kΩ 2% 1/4W	24773-321L
R10	Met film 6.2kΩ 2% 1/4W	24773-292W
R19	Met film 24kΩ 2% 1/4W	24773-306B
R27	Met film 47kΩ 2% 1/4W	24773-313H
R28	Met film 47kΩ 2% 1/4W	24773-313H
R29	Met film 47kΩ 2% 1/4W	24773-313H
R30	Met film 47kΩ 2% 1/4W	24773-313H
R32	Met film 100kΩ 2% 1/4W	24773-321L
R34	Met film 16kΩ 2% 1/4W	24773-302X
R35	Met film 16kΩ 2% 1/4W	24773-302X
R36	Met film 16kΩ 2% 1/4W	24773-302X
TR1	BC238B	28452-781A
TR2	BC238B	28452-781A
TR3	BC238B	28452-781A

33. Board AB10 - Display

When ordering, prefix circuit reference with AB10.

	Complete board	44827-799E
C1	Elec 220µF +100-20% 10V	26415-817J
R11	Met film 10kΩ 2% 1/4W	24773-297M
R12	Met film 10kΩ 2% 1/4W	24773-297M
R13	Met film 10kΩ 2% 1/4W	24773-297M
R14	Met film 10kΩ 2% 1/4W	24773-297M
R15	Met film 10kΩ 2% 1/4W	24773-297M
R16	Met film 10kΩ 2% 1/4W	24773-297M
R17	Met film 10kΩ 2% 1/4W	24773-297M
R18	Met film 150Ω 2% 1/4W	24773-253F
R20	Met film 150Ω 2% 1/4W	24773-253F
R21	Met film 150Ω 2% 1/4W	24773-253F

Circuit ref.	Description	Code no.
	Board AB10 - Display (contd.)	
R22	Met film 150Ω 2% 1/4W	24773-253F
R23	Met film 150Ω 2% 1/4W	24773-253F
R24	Met film 150Ω 2% 1/4W	24773-253F
R25	Met film 150Ω 2% 1/4W	24773-253F
R26	Met film 150Ω 2% 1/4W	24773-253F
R27	Met film 150Ω 2% 1/4W	24773-253F
R31	Met film 10kΩ 2% 1/4W	24773-297M
TR1	BC238B	28452-781A
TR2	BC238B	28452-781A
TR3	BC238B	28452-781A
TR4	BC238B	28452-781A
TR5	BC238B	28452-781A
TR6	BC238B	28452-781A
TR7	BC238B	28452-781A
TR8	BC238B	28452-781A
TR9	2N2219	28453-847F
TR10	2N2219	28453-847F
TR11	2N2219	28453-847F
TR12	2N2219	28453-847F
TR13	2N2219	28453-847F
TR14	2N2219	28453-847F
TR15	2N2219	28453-847F
TR16	2N2219	28453-847F
TR17	2N2219	28453-847F
TR18	2N2219	28453-847F
TR19	2N2219	28453-847F

34. Board AB11 - Rectifier and charger

When ordering, prefix circuit reference with AB11.

Circuit ref.	Description	Code no.
	Complete board	44827-706N
D1	1N4004	28357-028K
D2	1N4004	28357-028K
D3	1N4004	28357-028K
D4	1N4004	28357-028K
D5	Zener 5.6V	28371-434Y
D6	1N4004	28357-028K
FS1	Q.A. 2A	23411-007N
FS2	Q.A. 2A	23411-007N
R1	Met film 2.2kΩ 2% 1/4W	24773-281Y
R2	Met film 100Ω 2% 1/4W	24773-249J
R3	Met film 120Ω 2% 1/4W	24773-251L
R4	Met film 10kΩ 2% 1/4W	24773-297M
R5	Var cermet 1kΩ 10% 1/2W	25711-544T
R6	WW 10Ω 5% 3W	25125-320A
R7	Met ox 100Ω 2% 1/2W	24573-049B

Circuit ref.	Description	Code no.
	Board AB11 - Rectifier and charger (contd.)	
TR1	BC238B	28452-781A
TR2	BFY51	28455-827T
TR3	BF338	28458-577X
TR4	2N3055	28456-567W
35.	Board AB12 - ±12V pre-regulator	
	When ordering prefix with AB12.	
	Complete board	44827-707L
C1	Plas 0.33µF 10% 63V	26582-401G
C2	Plas 0.33µF 10% 63V	26582-401G
C3	Plas 0.33µF 10% 63V	26582-401G
C4	Plas 0.33µF 10% 63V	26582-401G
36.	Board AB13 - Motor control	
	When ordering, prefix with AB13.	
	Complete board	44827-843N
C1	Plas 0.22µF 10% 100V	26582-226G
C2	Elec 47µF +100-20% 10V	26415-809E
C3	Elec 47µF +100-20% 10V	26415-809E
C4	Cer 270pF 2% 63V	26343-482W

Circuit ref.	Description	Code no.
D1	Zener 3.0V	28371-203G
D2	Zener 3.0V	28371-203G
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4148	28336-676J
D6	1N4148	28336-676J
D7	1N4148	28336-676J
D8	1N4148	28336-676J
IC1	µA741C	28461-304T
IC2	µA741C	28461-304T
IC3	OP02EJ	28461-326J
IC4	µA741C	28461-304T
IC5	µA741C	28461-304T
IC6 ⚠	CD4049	28469-181D
R1	Met film 39Ω 2% 1/4W	24773-239Z
R2	Met film 39Ω 2% 1/4W	24773-239Z
R3	Met film 10kΩ 2% 1/4W	24773-297M
R4	Met film 10kΩ 2% 1/4W	24773-297M
R5	Met film 47kΩ 2% 1/4W	24773-313H
R6	Met film 10kΩ 2% 1/4W	24773-297M
R7	Met film 10kΩ 2% 1/4W	24773-297M
R8	Met film 10kΩ 2% 1/4W	24773-297M
R9	Met film 10kΩ 2% 1/4W	24773-297M
R10	Met film 47kΩ 2% 1/4W	24773-313H

Circuit ref.	Description	Code no.
	Board AB13 - Motor control (contd.)	
R11	Met film 27kΩ 2% 1/4W	24773-307K
R12	Met film 2.2kΩ 2% 1/4W	24773-281Y
R13	Met film 2.2kΩ 2% 1/4W	24773-281Y
R14	Carb 2.2MΩ 10% 1/8W	24321-877J
R15	Met film 100kΩ 2% 1/4W	24773-321L
R16	Met film 91kΩ 2% 1/4W	24773-320N
R17	Met film 15kΩ 2% 1/4W	24773-301P
R18	Met film 10kΩ 2% 1/4W	24773-297M
R19	Met film 10kΩ 2% 1/4W	24773-297M
R20	Met film 15kΩ 2% 1/4W	24773-301P
R21	Met film 91kΩ 2% 1/4W	24773-320N
R23	Met film 270kΩ 2% 1/4W	24773-331D
R24	Met film 270kΩ 2% 1/4W	24773-331D
R25	Met film 100kΩ 2% 1/4W	24773-321L
R26	Met film 270kΩ 2% 1/4W	24773-331D
R27	Met film 100kΩ 2% 1/4W	24773-321L
R28	Met film 15kΩ 2% 1/4W	24773-301P
R29	Var cermet 10kΩ 10% 0.3W	25748-507X
R30	Met film 100kΩ 2% 1/4W	24773-321L
RLA	Reed relay	23486-445S
TR1	BC308	28433-455R
TR2	BC238B	28452-781A
TR3	BC238B	28452-781A
TR4	TIS74	28459-016X

Circuit ref.	Description	Code no.
37.	Board AB15 - Rectifier and regulator	
	When ordering prefix with AB15.	
	Complete board	44827-857X
C1	Plas 0.33µF 10% 63V	26582-408X
C2	Plas 0.33µF 10% 63V	26582-408X
C3	Plas 0.33µF 10% 63V	26582-408X
C4	Plas 0.33µF 10% 63V	26582-408X
C5	Plas 0.33µF 10% 63V	26582-408X
C6	Plas 0.33µF 10% 63V	26582-408X
C7	Tant 0.47µF 20% 35V	26486-207L
D1	1N4004	28357-028K
D2	1N4004	28357-028K
D3	1N4004	28357-028K
D4	1N4004	28357-028K
D5	1N4004	28357-028K
FS1	1A Q.A.	23411-006Y
IC1	LM309K	28461-704L
IC2	µA7805	28461-707G
IC3	µA7905	28461-717X
R1	Met film 10kΩ 2% 1/4W	24773-297M
R2	WW 10Ω 5% 1½W	25123-020F
R3	WW 10Ω 5% 1½W	25123-020F

38. Board AB16 - Level shifter

When ordering, prefix circuit reference with AB16.

Circuit ref.	Description	Code no.
	Complete board	44827-909Y
C1	Elec 2.2µF 20% 20V	26486-540K
C2	Cer 15pF 5% 63V	26343-467U
C3	Cer 15pF 5% 63V	26343-467U
C4	Cer 15pF 5% 63V	26343-467U
C5	Cer 15pF 5% 63V	26343-467U
IC1 ⚠	CD4001	28466-207Z
R1	Met film 33Ω 2% 1/4W	24773-237K
R2	Met film 150kΩ 2% 1/4W	24773-325V
R3	Met film 150kΩ 2% 1/4W	24773-325V
R4	Met film 150kΩ 2% 1/4W	24773-325V
R5	Met film 150kΩ 2% 1/4W	24773-325V
R6	Met film 150kΩ 2% 1/4W	24773-325V
R7	Met film 150kΩ 2% 1/4W	24773-325V
R8	Met film 150kΩ 2% 1/4W	24773-325V
R9	Met film 150kΩ 2% 1/4W	24773-325V
R10	Met film 15kΩ 2% 1/4W	24773-301P
R11	Met film 68kΩ 2% 1/4W	24773-317N
R12	Met film 390kΩ 2% 1/4W	24773-335M
R13	Met film 5.6kΩ 2% 1/4W	24773-291S
R14	Met film 15kΩ 2% 1/4W	24773-301P
R15	Met film 68kΩ 2% 1/4W	24773-317N
R16	Met film 390kΩ 2% 1/4W	24773-335M
R17	Met film 5.6kΩ 2% 1/4W	24773-291S
R18	Met film 15kΩ 2% 1/4W	24773-301P
R19	Met film 68kΩ 2% 1/4W	24773-317N
R20	Met film 390kΩ 2% 1/4W	24773-335M
R21	Met film 5.6kΩ 2% 1/4W	24773-291S
R22	Met film 15kΩ 2% 1/4W	24773-301P
R23	Met film 68kΩ 2% 1/4W	24773-317N
R24	Met film 390kΩ 2% 1/4W	24773-335M
R25	Met film 5.6kΩ 2% 1/4W	24773-291S
R26	Met film 15kΩ 2% 1/4W	24773-301P
R27	Met film 68kΩ 2% 1/4W	24773-317N
R28	Met film 390kΩ 2% 1/4W	24773-335M
R29	Met film 5.6kΩ 2% 1/4W	24773-291S
R30	Met film 15kΩ 2% 1/4W	24773-301P
R31	Met film 68kΩ 2% 1/4W	24773-317N
R32	Met film 390kΩ 2% 1/4W	24773-335M
R33	Met film 5.6kΩ 2% 1/4W	24773-291S
R34	Met film 150kΩ 2% 1/4W	24773-325V
R35	Met film 150kΩ 2% 1/4W	24773-325V
R36	Met film 150kΩ 2% 1/4W	24773-325V
R37	Met film 150kΩ 2% 1/4W	24773-325V
R38	Met film 150kΩ 2% 1/4W	24773-325V

Circuit ref.	Description	Code no.
	Board AB16 - Level shifter (contd.)	
TR1	BC308	28433-455R
TR2	BC308	28433-455R
TR3	BC308	28433-455R
TR4	BC308	28433-455R
TR5	BC308	28433-455R
TR6	BC308	28433-455R
39.	Board AB17 - Auxiliary RAM	
	When ordering prefix with AB17.	
	Complete board	44827-953V
C1	Tant 2.2µF 20% 20V	26486-540K
C2	Tant 2.2µF 20% 20V	26486-540K
IC1 ⚠	CD4002-1	28469-303H
40.	Board AB20 - Supply filter	
	When ordering prefix with AB20.	
	Complete board	44827-995W
C1	Elec 100µF +100-20% 25V	26415-813U
C2	Cer 0.01µF +80-20% 100V	26383-055L
C3	Elec 100µF +100-20% 25V	26415-813U

Circuit ref.	Description	Code no.
L1	Choke	44290-602D
L2	Choke	44290-602D
L3	Choke	44290-602D
L4	Choke	44290-602D
41.	Board AD1 - Crystal oscillator	
	When ordering prefix with AD1.	
	Complete board	44827-823T
C1	Elec 47µF +100-20% 25V	26423-231F
C2	Cer 0.022µF +50-25% 18V	26383-007R
C3	Var cer 10-60pF	26847-267D
C4	Cer 0.01µF +80-20% 100V	26383-055L
C5	Cer 0.01µF +80-20% 100V	26383-055L
C6	Cer 0.001µF +80-20% 500V	26383-242P
C7	Cer 0.01µF +80-20% 100V	26383-055L
C8	Cer 0.001µF +80-20% 500V	26383-242P
C9	Cer 0.01µF +80-20% 500V	26383-055L
C10	Cer 0.01µF +80-20% 100V	26383-055L
C11	Cer 0.01µF +80-20% 100V	26383-055L
C12	Cer 0.01µF +80-20% 100V	26383-055L
C13	Cer 0.01µF +80-20% 100V	26383-055L
C14	Cer 0.022µF +50-25% 18V	26383-007R
C15	Cer 0.022µF +50-25% 18V	26383-007R

Board AD1 - Crystal oscillator (contd.)

Circuit ref.	Description	Code no.
C16	Cer 0.022µF +50-25% 18V	26383-007R
C17	Cer 0.022µF +50-25% 18V	26383-007R
C18	Cer 0.047µF +50-25% 12V	26383-016E
C19	Cer 0.047µF +80-20% 25V	26383-017U
C20	Cer 0.022µF +50-25% 18V	26383-007R
C21	Cer 0.022µF +50-25% 18V	26383-007R
C22	Cer 0.022µF +50-25% 18V	26383-007R
C23	Cer 0.047µF +80-20% 25V	26383-017U
C24	Cer 68pF +50-25% 18V	26343-475F
C25	Cer 0.01µF +80-20% 100V	26383-055L
C26	Var cer 3-9pF	26847-109K
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4148	28336-676J
IC1	74LS90	28464-014S
IC2 ⚠	CD4017	28464-008F
L1	RF choke	23642-561W
R1	Met film 330Ω 2% 1/4W	24773-261D
R2	Met film 330Ω 2% 1/4W	24773-261D
R3	Met film 10kΩ 2% 1/4W	24773-297M
R4	Met film 20kΩ 2% 1/4W	24773-304C
R5	Met film 5.1kΩ 2% 1/4W	24773-290V
R6	Met film 10kΩ 2% 1/4W	24773-297M
R7	Met film 15kΩ 2% 1/4W	24773-301P
R8	Met film 10kΩ 2% 1/4W	24773-297M
R9	Met film 56Ω 2% 1/4W	24773-243H
R10	Met film 1kΩ 2% 1/4W	24773-273A
R11	Met film 20Ω 2% 1/4W	24773-232X
R12	Met film 1kΩ 2% 1/4W	24773-273A
R13	Met film 1kΩ 2% 1/4W	24773-273A
R14	Met film 220Ω 2% 1/4W	24773-257W
R15	Met film 330Ω 2% 1/4W	24773-261D
R16	Met film 47Ω 2% 1/4W	24773-241A
R17	Met film 22Ω 2% 1/4W	24773-233M
R18	Met film 33Ω 2% 1/4W	24773-237K
R19	Met film 82Ω 2% 1/4W	24773-247N
R20	Met film 240Ω 2% 1/4W	24773-258D
R21	Met film 560Ω 2% 1/4W	24773-267R
R22	Met film 220Ω 2% 1/4W	24773-257W
R23	Met film 1.3kΩ 2% 1/4W	24773-276E
R24	Met film 220Ω 2% 1/4W	24773-257W
R25	Met film 220Ω 2% 1/4W	24773-257W
R26	Met film 2.7kΩ 2% 1/4W	24773-283L
R27	Met film 100Ω 2% 1/4W	24773-249J
R28	Met film 220Ω 2% 1/4W	24773-257W

Circuit ref.	Description	Code no.
	Board AD1 - Crystal oscillator (contd.)	
R29	Met film 100Ω 2% 1/4W	24773-249J
R30	Met film 240Ω 2% 1/4W	24773-258D
R31	Met film 100Ω 2% 1/4W	24773-249J
R32	Met film 620Ω 2% 1/4W	24773-268B
R33	Met film 620Ω 2% 1/4W	24773-268B
R34	Met film 220Ω 2% 1/4W	24773-257W
R35	Met film 220Ω 2% 1/4W	24773-257W
R36	Met film 7.5kΩ 2% 1/4W	24773-294T
R37	Met film 3.3kΩ 2% 1/4W	24773-285F
R38	Met film 100Ω 2% 1/4W	24773-249J
R39	Met film 20kΩ 2% 1/4W	24773-304C
TR1	BC238B	28452-781A
TR2	BC238B	28452-781A
TR3	BSX20	28452-197H
TR4	BSX20	28452-197H
TR5	BSX20	28452-197H
TR6	BSX20	28452-197H
TR7	BSX20	28452-197H
TR8	BSX20	28452-197H
TR9	BSX20	28452-197H
TR10	BSX20	28452-197H
TR11	BSX20	28452-197H
T1	Transformer	43590-031A
T2	Transformer	43590-032Z
T3	Transformer	43590-032Z
T4	Transformer	43590-031A
X1	10MHz crystal oscillator TCXO	28313-862L
42.	Board AD2 - Interpolation p.d.	
	When ordering prefix with AD2.	
	Complete board	44827-824P
C1	Cer 0.047µF +80-20% 25V	26383-017U
C2	Cer 0.047µF +80-20% 25V	26383-017U
C3	Cer 0.047µF +80-20% 25V	26383-017U
C4	Cer 0.047µF +80-20% 25V	26383-017U
C5	Elec 47µF +100-20% 10V	26415-809E
C6	Elec 47µF +100-20% 10V	26415-809E
C7	Plas 10pF 2% 350V	26516-010V
C8	Plas 0.01µF 10% 250V	26582-202T
C9	Cer 0.047µF +80-20% 25V	26383-017U
C10	Plas 470pF 2% 160V	26516-406H
C11	Plas 0.68µF 10% 63V	26582-412M
C12	Plas 220pF 2% 350V	26516-329B
C13	Plas 0.1µF 10% 100V	26582-211B
C14	Plas 470pF 2% 160V	26516-406H
C15	Cer 0.047µF +80-20% 25V	26383-017U

Board AD2 - Interpolation p.d. (contd.)

Circuit ref.	Description	Code no.
C16	Cer 0.047µF +80-20% 25V	26383-017U
C17	Cer 0.047µF +80-20% 25V	26383-017U
C18	Cer 0.047µF +80-20% 25V	26383-017U
C20	Cer 0.047µF +80-20% 25V	26383-017U
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4148	28336-676J
D6	1N4148	28336-676J
D7	1N4148	28336-676J
IC1 ⚠	CD4027	28462-018C
IC2 ⚠	CD4017	28464-008F
IC3 ⚠	CD4017	28464-008F
IC4	µA741C	28461-304T
IC5 ⚠	CD4016	28469-364K
R1	Carb 1MΩ 5% 1/8W	24311-945Y
R2	Met film 20kΩ 2% 1/4W	24773-304C
R3	Met film 20kΩ 2% 1/4W	24773-304C
R4	Met film 1kΩ 2% 1/4W	24773-273A
R5	Met film 47kΩ 2% 1/4W	24773-313H
R6	Met film 100kΩ 2% 1/4W	24773-321L
R7	Met film 100Ω 2% 1/4W	24773-249J
R8	Met film 47kΩ 2% 1/4W	24773-313H
R9	Met film 100Ω 2% 1/4W	24773-249J
R10	Met film 2kΩ 2% 1/4W	24773-280U
R11	Met film 200kΩ 2% 1/4W	24773-328D
R12	Met film 470kΩ 2% 1/4W	24773-337R
R13	Met film 51kΩ 2% 1/4W	24773-314E
R14	Met film 10kΩ 2% 1/4W	24773-297M
R15	Met film 100Ω 2% 1/4W	24773-249J
R16	Met film 100Ω 2% 1/4W	24773-249J
R17	Met film 30kΩ 2% 1/4W	24773-308A
R18	Met film 100kΩ 2% 1/4W	24773-321L
R19	Met film 240kΩ 2% 1/4W	24773-330W
R20	Met film 30kΩ 2% 1/4W	24773-308A
R21	Met film 100kΩ 2% 1/4W	24773-321L
R22	Met film 240kΩ 2% 1/4W	24773-330W
R23	Met film 30kΩ 2% 1/4W	24773-308A
R24	Met film 100kΩ 2% 1/4W	24773-321L
R25	Met film 240kΩ 2% 1/4W	24773-330W
R26	Met film 7.5kΩ 2% 1/4W	24773-294T
R27	Met film 10kΩ 2% 1/4W	24773-297M
R28	Met film 100Ω 2% 1/4W	24773-249J
R29	Met film 20kΩ 2% 1/4W	24773-304C
R30	Met film 10kΩ 2% 1/4W	24773-297M
R31	Met film 1kΩ 2% 1/4W	24773-273A

Circuit ref.	Description	Code no.
	Board AD2 - Interpolation p.d. (contd.)	
R32	Met film 2kΩ 2% 1/4W	24773-280U
R33	Met film 10kΩ 2% 1/4W	24773-297M
R34	Met film 470kΩ 2% 1/4W	24773-337R
TR1	BC308	28433-455R
TR2	BSX20	28452-197H
TR3	BC238B	28452-781A
TR4	BC308	28433-455R
TR5	BC238B	28452-781A
TR6	BC238B	28452-781A
TR7	BC238B	28452-781A
TR8	BC238B	28452-781A
TR9	BF244B	28459-011S
43.	Board AD3 - Interpolation var. divider	
	When ordering, prefix with AD3.	
	Complete board	44827-825X
C1	Cer 0.001µF +80-20% 500V	26383-242P
C2	Cer 0.01µF +80-20% 100V	26383-055L
C3	Cer 0.01µF +80-20% 100V	26383-055L
C4	Cer 0.01µF +80-20% 100V	26383-055L
C5	Cer 0.01µF +80-20% 100V	26383-055L
C6	Cer 0.022µF +50-25% 18V	26383-007R
C7	Cer 0.022µF +50-25% 18V	26383-007R
C8	Cer 120pF 2% 63V	26343-478S
C9	Cer 150pF 2% 63V	26343-479W
C10	Cer 10pF ±0.5pF 63V	26343-465H
C11	Cer 120pF 2% 63V	26343-478S
C12	Cer 0.022µF +50-25% 18V	26383-007R
C13	Cer 0.022µF +50-25% 18V	26383-007R
C14	Elec 47µF +100-20% 10V	26415-809E
C15	Elec 47µF +100-20% 10V	26415-809E
C16	Cer 0.047µF +80-20% 25V	26383-017U
C17	Elec 47µF +100-20% 10V	26415-809E
C18	Elec 47µF +100-20% 10V	26415-809E
C19	Plas 0.0033µF 2% 160V	26516-609Z
C20	Cer 150pF 2% 63V	26343-479W
C21	Cer 0.047µF +80-20% 25V	26383-017U
C22	Cer 0.047µF +80-20% 25V	26383-017U
C23	Cer 0.048µF +80-20% 25V	26383-017U
C24	Cer 150pF 2% 63V	26343-479W
C25	Cer 150pF 2% 63V	26343-479W
C26	Cer 33pF 5% 63V	26343-471Y
D1	1N4148	28336-676J
D2	1N4148	28336-676J

Board AD3 - Interpolation var. divider (contd.)

Circuit ref.	Description	Code no.
IC1 ⚠	CD4042	28462-404A
IC2 ⚠	µA741C	28461-304T
IC3 ⚠	MC1496	28461-911L
IC4 ⚠	CD4059	28464-011F
IC5 ⚠	CD4001	28466-207Z
L1	Inductor	44290-543K
L2	Inductor	44290-544A
L3	Inductor	44290-551U
R1	Met film 560Ω 2% 1/4W	24773-267R
R2	Met film 75Ω 2% 1/4W	24773-246Y
R3	Met film 7.5kΩ 2% 1/4W	24773-294T
R4	Met film 100Ω 2% 1/4W	24773-249J
R5	Met film 100Ω 2% 1/4W	24773-249J
R6	Met film 10kΩ 2% 1/4W	24773-297M
R7	Met film 1kΩ 2% 1/4W	24773-273A
R8	Met film 10kΩ 2% 1/4W	24773-297M
R9	Met film 100Ω 2% 1/4W	24773-249J
R10	Met film 130Ω 2% 1/4W	24773-252J
R11	Met film 1.6kΩ 2% 1/4W	24773-278Y
R12	Met film 6.8kΩ 2% 1/4W	24773-293D
R13	Met film 3.9kΩ 2% 1/4W	24773-287V
R14	Met film 1kΩ 2% 1/4W	24773-273A
R15	Met film 3.9kΩ 2% 1/4W	24773-287V
R16	Met film 620Ω 2% 1/4W	24773-268B
R17	Met film 100Ω 2% 1/4W	24773-249J
R18	Met film 100Ω 2% 1/4W	24773-249J
R19	Met film 100Ω 2% 1/4W	24773-249J
R20	Met film 620Ω 2% 1/4W	24773-268B
R21	Met film 20kΩ 2% 1/4W	24773-304C
R22	Carb 2.2MΩ 10% 1/8W	24321-877J
R24	Met film 6.2kΩ 2% 1/4W	24773-292W
R25	Var cermet 47kΩ 10% 1/2W	25711-506S
R26	Var cermet 4.7kΩ 10% 1/2W	25711-504G
R27	Var cermet 220kΩ 10% 1/2W	25711-509T
R28	Met film 220Ω 2% 1/4W	24773-257W
R29	Met film 100kΩ 2% 1/4W	24773-321L
R30	Met film 220Ω 2% 1/4W	24773-257W
R31	Met film 100kΩ 2% 1/4W	24773-321L
R32	Met film 200kΩ 2% 1/4W	24773-328D
R33	Carb 820kΩ 5% 1/8W	24311-943E
R34	Met film 390kΩ 2% 1/4W	24773-335M
R35	Met film 22kΩ 2% 1/4W	24773-305R
R36	Met film 22kΩ 2% 1/4W	24773-305R
R37	Carb 1MΩ 5% 1/8W	24311-945Y
R38	Carb 1MΩ 5% 1/8W	24311-945Y
R39	Carb 1MΩ 5% 1/8W	24311-945Y
R40	Carb 1MΩ 5% 1/8W	24311-945Y
R41	Carb 1MΩ 5% 1/8W	24311-945Y
R42	Carb 1MΩ 5% 1/8W	24311-945Y

Circuit ref.	Description	Code no.
	Board AD3 - Interpolation var. divider (contd.)	
R43	Carb 1MΩ 5% 1/8W	24311-945Y
R44	Carb 1MΩ 5% 1/8W	24311-945Y
R45	Carb 1MΩ 5% 1/8W	24311-945Y
R46	Carb 1MΩ 5% 1/8W	24311-945Y
R47	Carb 1MΩ 5% 1/8W	24311-945Y
R48	Carb 1MΩ 5% 1/8W	24311-945Y
R50	Carb 2.2MΩ 10% 1/8W	24321-877J
R52	Carb 1MΩ 5% 1/8W	24311-945Y
T2	Transformer	43590-032Z
TR1	BSX20	28452-197H
TR2	BC238B	28452-781A
TR3	BC238B	28452-781A
44.	Board AD4 - Interpolation oscillator	
	When ordering prefix with AD4.	
	Complete board	44827-826M
C1	Cer 0.01µF +80-20% 100V	26383-055L
C2	Cer 0.01µF +80-20% 100V	26383-055L
C3	Elec 47µF +100-20% 10V	26415-809E
C4	Elec 47µF +100-20% 10V	26415-809E
C5	Cer 0.01µF +80-20% 10V	26383-055L
C6	Cer 0.01µF +80-20% 10V	26383-055L
C7	Cer 0.01µF +80-20% 10V	26383-055L
C8	Cer 0.01µF +80-20% 10V	26383-055L
C9	Cer 0.047µF +80-20% 25V	26383-017U
C10	Cer 15pF 10% 500V	26343-127Y
C11	Cer 0.047µF +80-20% 25V	26383-017U
C12	Cer 0.047µF +80-20% 25V	26383-017U
C13	Cer 0.047µF +80-20% 15V	26383-017U
C14	Plas 0.15µF 10% 100V	26582-212K
D1	BB105	28381-096S
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4148	28336-676J
IC1	7490	28464-002E
IC2 ⚠	CD4011	28466-340R
IC3 ⚠	CD4059	28464-011F
IC4	Resistor network 220kΩ	24681-606S
IC5	Resistor network 220kΩ	24681-606S
IC6	Resistor network 15kΩ	24681-507T
IC7	Resistor network 15kΩ	24681-507T
IC8 ⚠	CD4070	28466-402T
R1	Met film 1kΩ 2% 1/4W	24773-273A

Circuit ref.	Description	Code no.
	Board AD4 - Interpolation oscillator (contd.)	
R2	Met film 220Ω 2% 1/4W	24773-257W
R3	Met film 330Ω 2% 1/4W	24773-261D
R4	Met film 47Ω 2% 1/4W	24773-241A
R5	Met film 1kΩ 2% 1/4W	24773-273A
R6	Met film 47Ω 2% 1/4W	24773-241A
R7	Met film 47Ω 2% 1/4W	24773-241A
R8	Met film 680Ω 2% 1/4W	24773-269K
R9	Met film 20Ω 2% 1/4W	24773-232X
R10	Met film 47Ω 2% 1/4W	24773-241A
R11	Met film 82Ω 2% 1/4W	24773-247N
R12	Met film 560Ω 2% 1/4W	24773-267R
R13	Met film 4.7kΩ 2% 1/4W	24773-289W
R14	Met film 33Ω 2% 1/4W	24773-237K
R15	Met film 47Ω 2% 1/4W	24773-241A
R16	Met film 47Ω 2% 1/4W	24773-241A
R17	Carb 1MΩ 5% 1/8W	24311-945Y
R18	Met film 100kΩ 2% 1/4W	24773-321L
R19	Carb 2.2MΩ 10% 1/8W	24321-877J
T1	Transformer	43590-030K
T2	Transformer	43590-032Z
TR1	BF244B	28459-011S
TR2	BC239C	28452-771P
TR3	BC239C	28452-771P
TR4	BC239C	28452-771P

Circuit ref.	Description	Code no.
45.	Board AD5 - Translation phase detector	
	When ordering prefix with AD5.	
	Complete board	44828-070U
C1	Elec 47µF +100-20% 40V	26423-232G
C2	Elec 47µF +100-20% 40V	26423-232G
C3	Cer 0.01µF +80-20% 100V	26383-055L
C4	Tant 0.47µF 20% 35V	26486-207L
C5	Cer 180pF 2% 63V	26343-480V
C6	Cer 0.01µF +80-20% 100V	26383-055L
C7	Plas 0.001µF 2% 160V	26516-481L
C8	Plas 0.1µF 10% 100V	26582-211B
C9	Cer 330pF 2% 63V	26343-483D
C10	Cer 100pF 2% 63V	26343-477V
C11	Tant 4.7µF 20% 35V	26486-219P
C12	Tant 4.7µF 20% 35V	26486-219P
C13	Plas 3.3µF 5% 63V	26582-419H
C14	Plas 0.22µF 10% 100V	26582-226G
C15	Tant 0.47µF 20% 35V	26486-207L
C16	Cer 0.047µF +80-20% 100V	26383-017U
C17	Cer 0.047µF +80-20% 100V	26383-017U
C18	Cer 0.047µF +80-20% 100V	26383-017U
C19	Cer 0.047µF +80-20% 100V	26383-017U
C20	Cer 10pF ±0.5pF 63V	26343-465H
C21	Cer 10pF ±0.5pF 63V	26343-465H

Board AD5 - Translation phase detector (contd.)

Circuit ref.	Description	Code no.
C22	Cer 100pF 2% 63V	26343-477V
C23	Cer 47pF 5% 63V	26343-473L
D1	5082-2800	28349-007E
D2	5082-2800	28349-007E
D3	BAY72	28337-126P
D4	BAY72	28337-126P
L1	RF choke	23642-558W
IC1	MC 1496G	28461-911L
IC2	NE531	28461-317H
IC3 ⚠	CD4017	28464-008F
IC4 ⚠	CD4013	28462-608A
IC5 ⚠	CD4025	28466-209E
IC6 ⚠	CD4023	28466-341B
IC7 ⚠	CD4011	28466-340R
R1	Met film 47Ω 2% 1/4W	24773-241A
R2	Met film 100Ω 2% 1/4W	24773-249J
R3	Met film 47Ω 2% 1/4W	24773-241A
R4	Met film 10kΩ 2% 1/4W	24773-297M
R5	Met film 1kΩ 2% 1/4W	24773-273A
R6	Met film 5.1kΩ 2% 1/4W	24773-290V
R7	Met film 1kΩ 2% 1/4W	24773-273A
R8	Met film 3.3kΩ 2% 1/4W	24773-285F
R9	Met film 300Ω 2% 1/4W	24773-260W
R10	Met film 6.8kΩ 2% 1/4W	24773-293D
R11	Met film 3kΩ 2% 1/4W	24773-284J
R12	Met film 47kΩ 2% 1/4W	24773-313H
R13	Carb 1MΩ 5% 1/8W	24311-945Y
R14	Met film 17kΩ 2% 1/4W	24773-313H
R15	Met film 17kΩ 2% 1/4W	24773-313H
R16	Met film 6.8kΩ 2% 1/4W	24773-293D
R17	Met film 6.8kΩ 2% 1/4W	24773-293D
R18	Met film 6.8kΩ 2% 1/4W	24773-293D
R19	Met film 6.8kΩ 2% 1/4W	24773-293D
R20	Met film 3.9kΩ 2% 1/4W	24773-287V
R21	Carb 1MΩ 5% 1/8W	24311-945Y
R22	Carb 1MΩ 5% 1/8W	24311-945Y
R23	Carb 1MΩ 5% 1/8W	24311-945Y
R24	Carb 1MΩ 5% 1/8W	24311-945Y
R25	Carb 1MΩ 5% 1/8W	24311-945Y
R26	Met film 4.7kΩ 2% 1/4W	24773-289W
R27	Met film 3.9kΩ 2% 1/4W	24773-287V
R28	Carb 1MΩ 5% 1/8W	24311-945Y
R29	Met film 20kΩ 2% 1/4W	24773-304C
R30	Carb 1MΩ 5% 1/8W	24311-945Y
TR1	BCY71	28435-235L

Circuit ref.	*Description*	*Code no.*
	Board AD5 - Translation phase detector (contd.)	
TR2	BCY71	28435-235L
TR3	BCY71	28435-235L
TR4	BC239C	28452-771P
TR5	BC239C	28452-771P
TR6	BCY71	28435-235L
46.	Board AD6 - Translation oscillator	
	When ordering prefix with AD6.	
	Complete board	44828-071Y
C1	Elec 47µF +100-20% 40V	26423-232G
C2	Tant 0.47µF 20% 35V	26486-207L
C3	Elec 47µF +100-20% 40V	26423-232G
C4	Cer 47pF 5% 63V	26343-473L
C5	Cer 0.01µF +80-20% 100V	26383-055L
C6	Cer 0.047µF +80-20% 25V	26383-017U
C7	Cer 39pF 5% 63V	26343-472N
C8	Cer 0.047µF +80-20% 25V	26383-017U
C9	Cer 0.047µF +80-20% 25V	26383-017U
C10	Tant 0.47µF 20% 35V	26486-207L
C11	Cer 0.047µF +80-20% 25V	26383-017U
C12	Tant 0.47µF 20% 35V	26486-207L
C13	Tant 0.47µF 20% 35V	26486-207L
C14	Elec 47µF +100-20% 40V	26423-232G
C15	Cer 0.001µF +100-20% 40V	26387-252X
C16	Cer 0.001µF +100-20% 40V	26387-252X
C17	Tant 0.47µF 20% 35V	26486-207L
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	5082-3379	28383-997T
D5	5082-3379	28383-997T
D6	MV109	28381-130J
D7	MV109	28381-130J
D8	MV109	28381-130J
D9	MV109	28381-130J
IC1	74LS90	28464-014S
IC2 ⚠	CD4017	28464-008F
IC3 ⚠	CD4017	28464-008F
L1	RF choke	23642-553J
L2	RF choke	23642-554F
L3	RF choke	23642-557S
L4†	RF choke	23642-553J
L5	RF choke	23642-557S
L6†	RF choke	23642-553J
R1	Met film 47Ω 2% 1/4W	24773-241A

Circuit ref.	Description	Code no.
	Board AD6 - Translation oscillator (contd.)	
R2	Met film 6.2kΩ 2% 1/4W	24773-292W
R3	Met film 3.6kΩ 2% 1/4W	24773-286G
R4	Met film 1kΩ 2% 1/4W	24773-273A
R5	Met film 470Ω 2% 1/4W	24773-265M
R6	Met film 1kΩ 2% 1/4W	24773-273A
R7	Met film 68Ω 2% 1/4W	24773-245U
R8	Met film 10kΩ 2% 1/4W	24773-297M
R9	Met film 10kΩ 2% 1/4W	24773-297M
R10	Met film 10kΩ 2% 1/4W	24773-297M
R11	Met film 5.1kΩ 2% 1/4W	24773-290V
R12	Met film 1kΩ 2% 1/4W	24773-273A
R13	Met film 150Ω 2% 1/4W	24773-253F
R14	Met film 51Ω 2% 1/4W	24773-242Z
R15	Met film 47Ω 2% 1/4W	24773-241A
R16	Met film 680Ω 2% 1/4W	24773-269K
R17	Met film 47Ω 2% 1/4W	24773-241A
R18	Met film 3.9kΩ 2% 1/4W	24773-287V
R19	Met film 47Ω 2% 1/4W	24773-241A
R20	Met film 3.9kΩ 2% 1/4W	24773-287V
R21	Met film 1kΩ 2% 1/4W	24773-273A
R22	Met film 1kΩ 2% 1/4W	24773-273A
R23	Met film 10kΩ 2% 1/4W	24773-297M
R24	Met film 10kΩ 2% 1/4W	24773-297M
R25	Met film 47kΩ 2% 1/4W	24773-313H
R26	Met film 47kΩ 2% 1/4W	24773-313H
R27	Met film 100kΩ 2% 1/4W	24773-321L
R28	Met film 100kΩ 2% 1/4W	24773-321L
R29	Met film 10kΩ 2% 1/4W	24773-297M
R30	Met film 47kΩ 2% 1/4W	24773-313H
R31	Met film 10kΩ 2% 1/4W	24773-297M
R32	Met film 47kΩ 2% 1/4W	24773-313H
R33	Met film 22Ω 2% 1/4W	24773-233M
R34	Met film 47Ω 2% 1/4W	24773-241A
TR1	BC239C	28452-771P
TR2	BC239C	28452-771P
TR3	BC239C	28452-771P
TR4	BSX20	28452-197H
TR5	BSX20	28452-197H
TR6	BC239C	28452-771P
TR7	BC239C	28452-771P
XL1	10.046MHz	28312-052N
XL2	10.036MHz	28312-051Y
47.	Board AD7 - Output variable divider	
	When ordering prefix with AD7.	
	Complete board	44827-829B

Board AD7 - Output variable divider (contd.)

Circuit ref.		Description	Code no.
C1		Cer 0.001µF +80-20% 500V	26383-242P
C2		Cer 0.022µF +50-20% 18V	26383-007R
C3		Cer 0.022µF +50-20% 18V	26383-007R
C4		Cer 0.022µF +50-20% 18V	26383-007R
C5		Cer 0.022µF +50-20% 18V	26383-007R
C6		Elec 47µF +100-20% 25V	26423-231F
C7		Cer 0.022µF +50-20% 18V	26383-007R
C8		Cer 0.022µF +50-20% 18V	26383-007R
C9		Cer 0.022µF +50-20% 18V	26383-007R
C10		Cer 0.022µF +50-20% 18V	26383-007R
C11		Cer 0.022µF +50-20% 18V	26383-007R
C12		Elec 47µF +100-20% 25V	26423-231F
C13		Cer 0.001µF +80-20% 500V	26383-242P
D1		1N4148	28336-676J
D2		1N4148	28336-676J
D3		1N4148	28336-676J
IC1		SP8646B	28464-015W
IC2		74LS74	28462-611A
IC3	⚠	CD4522	28464-113F
IC4	⚠	CD4522	28464-113F
IC5	⚠	CD4522	28464-113F
IC6	⚠	HEF4001BP	28466-223V
IC7	⚠	CD4001	28466-207Z
IC8	⚠	CD4001	28466-207Z
IC9	⚠	CD4011	28466-340R
IC10	⚠	CD4013	28462-608A
IC11	⚠	CD4013	28462-608A
IC12	⚠	CD4013	28462-608A
IC14		Resistor package 220kΩ	24681-606S
IC15		Resistor package 220kΩ	24681-606S
R1		Met film 47Ω 2% 1/4W	24773-241A
R2		Met film 47Ω 2% 1/4W	24773-241A
R3		Met film 13Ω 2% 1/4W	24773-228P
R4		Met film 2.7kΩ 2% 1/4W	24773-283L
R5		Met film 470Ω 2% 1/4W	24773-265M
R6		Met film 47Ω 2% 1/4W	24773-241A
R7		Met film 330Ω 2% 1/4W	24773-261D
R8		Met film 200Ω 2% 1/4W	24773-256S
R9		Met film 680Ω 2% 1/4W	24773-269K
R10		Met film 2.0kΩ 2% 1/4W	24773-280U
R11		Met film 1.5kΩ 2% 1/4W	24773-277U
R12		Carb 1MΩ 5% 1/8W	24311-945Y
R13		Carb 1MΩ 5% 1/8W	24311-945Y
R16		Carb 1MΩ 5% 1/8W	24311-945Y
R17		Met film 4.7kΩ 2% 1/4W	24773-289W
T1		Transformer	43590-031A

Circuit ref.	Description	Code no.
	Board AD7 - Output variable divider (contd.)	
TR1	BSX20	28452-197H
TR2	BSX20	28452-197H
48.	Board AD8 - Output oscillator	
	When ordering prefix with AD8.	
	Complete board	44827-830C
C1	Elec 47µF +100-20% 25V	26423-231F
C2	Cer 0.01µF +80-20% 100V	26383-055L
C3	Plas 0.47µF 10% 100V	26582-215H
C4	Elec 47µF +100-20% 25V	26423-231F
C5	Cer 0.001µF +80-20% 500V	26383-242P
C6	Cer 0.01µF +80-20% 100V	26383-055L
C7	Cer 0.001µF +80-20% 500V	26383-242P
C8	Cer 0.001µF +80-20% 500V	26383-242P
C9	Cer 0.001µF +80-20% 500V	26383-242P
C10	Plas 0.047µF 10% 250V	26582-206C
C11	Cer 0.01µF +80-20% 100V	26383-055L
D1	MV109	28381-130J
D2	MV109	28381-130J
D3	MV109	28381-130J
D4	MV109	28381-130J
D5	MV109	28381-130J
D6	MV109	28381-130J
D7	MV109	28381-130J
D8	MV109	28381-130J
D9	1N4148	28336-676J
D10	1N4148	28336-676J
L1	Inductor	44290-570K
L2	Inductor	44290-601W
L3	Inductor	44290-601W
R1	Met film 2.2kΩ 2% 1/4W	24773-281Y
R2	Met film 220Ω 2% 1/4W	24773-257W
R3	Met film 330Ω 2% 1/4W	24773-261D
R4	Met film 47Ω 2% 1/4W	24773-241A
R5	Met film 560Ω 2% 1/4W	24773-267R
R6	Met film 47Ω 2% 1/4W	24773-241A
R7	Met film 560Ω 2% 1/4W	24773-267R
R8	Met film 47Ω 2% 1/4W	24773-241A
R9	Met film 82Ω 2% 1/4W	24773-247N
R10	Met film 33Ω 2% 1/4W	24773-237K
R11	Met film 82Ω 2% 1/4W	24773-247N
R12	Met film 47Ω 2% 1/4W	24773-241A
R13	Met film 560Ω 2% 1/4W	24773-267R
R14	Met film 240Ω 2% 1/4W	24773-258D
R15	Met film 47Ω 2% 1/4W	24773-241A
R16	Met film 560Ω 2% 1/4W	24773-267R

Circuit ref.	Description	Code no.
	Board AD8 - Output oscillator (contd.)	
R17	Met film 47Ω 2% 1/4W	24773-241A
R18	Met film 910Ω 2% 1/4W	24773-272K
T1	Transformer	43590-032Z
T2	Transformer	43590-032Z
T3	Transformer	43590-032Z
TR1	BF244B	28459-011S
TR2	BSX20	28452-197H
TR3	BSX20	28452-197H
TR4	BSX20	28452-197H
TR5	BSX20	28452-197H
49.	Board AD9 - Output phase detector	
	When ordering prefix with AD9.	
	Complete board	44827-831R
C1	Cer 0.022µF +50-25% 18V	26383-007R
C2	Cer 0.022µF +50-25% 18V	26383-007R
C3	Plas 0.015µF 10% 250V	26582-203P
C4	Elec 47µF +100-20% 25V	26423-231F
C5	Elec 47µF +100-20% 25V	26423-231F
C6	Cer 10pF ±0.5pF 63V	26343-465H
C7	Cer 10pF ±0.5pF 63V	26343-465H
D1	1N4148	28336-676J
D2	HP5082-2800	28349-007E
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	HP5082-2800	28349-007E
IC1 ⚠	CD4013	28462-608A
IC2 ⚠	CD4001	28466-207Z
IC3	CA3046	28461-901A
L1	RF choke	23642-557S
L2	RF choke	23642-557S
R1	Carb 1MΩ 5% 1/8W	24311-945Y
R2	Carb 1MΩ 5% 1/8W	24311-945Y
R3	Met film 47Ω 2% 1/4W	24773-241A
R4	Met film 47Ω 2% 1/4W	24773-241A
R5	Met film 100kΩ 2% 1/4W	24773-321L
R6	Met film 30kΩ 2% 1/4W	24773-308A

Circuit ref.	Description	Code no.
50.	Board AD10 - Synthesizer latch	
	When ordering prefix with AD10.	
	Complete board	44827-832B
C1	Elec 47µF +100-20% 10V	26415-809E
C2	Elec 47µF +100-20% 10V	26415-809E
C3	Cer 270pF 2% 63V	26343-482W
C4	Cer 270pF 2% 63V	26343-482W
C5	Cer 270pF 2% 63V	26343-482W
C6	Cer 270pF 2% 63V	26343-482W
C7	Cer 270pF 2% 63V	26343-482W
C8	Cer 270pF 2% 63V	26343-482W
C9	Cer 270pF 2% 63V	26343-482W
C10	Cer 270pF 2% 63V	26343-482W
C11	Cer 0.01µF +80-20% 100V	26383-055L
C12	Cer 0.01µF +80-20% 100V	26383-055L
C13	Cer 0.01µF +80-20% 100V	26383-055L
IC1 ⚠	CD4042	28462-404A
IC2 ⚠	CD4042	28462-404A
IC3 ⚠	CD4042	28462-404A
IC4 ⚠	CD4042	28462-404A
IC5 ⚠	CD4042	28462-404A
IC6 ⚠	CD4042	28462-404A
IC7 ⚠	CD4042	28462-404A
IC8 ⚠	CD4042	28462-404A
IC9 ⚠	CD4028	28465-023Y
IC10 ⚠	CD4028	28465-023Y
IC11 ⚠	CD4016	28469-364K
IC12 ⚠	CD4016	28469-364K
IC13 ⚠	CD4016	28469-364K
IC14 ⚠	CD4016	28469-364K
R3	Met film 15kΩ 2% 1/4W	24773-301P
R4	Met film 15kΩ 2% 1/4W	24773-301P
R5	Met film 15kΩ 2% 1/4W	24773-301P
R6	Met film 15kΩ 2% 1/4W	24773-301P
R7	Met film 15kΩ 2% 1/4W	24773-301P
R8	Met film 15kΩ 2% 1/4W	24773-301P
R9	Met film 15kΩ 2% 1/4W	24773-301P
R10	Met film 15kΩ 2% 1/4W	24773-301P
R11	Met film 100kΩ 2% 1/4W	24773-321L
R12	Met film 100kΩ 2% 1/4W	24773-321L
R13	Met film 100kΩ 2% 1/4W	24773-321L
R14	Met film 100kΩ 2% 1/4W	24773-321L
R15	Met film 100kΩ 2% 1/4W	24773-321L
R16	Met film 100kΩ 2% 1/4W	24773-321L
R17	Met film 100kΩ 2% 1/4W	24773-321L
R18	Met film 100kΩ 2% 1/4W	24773-321L

Circuit ref.	*Description*	*Code no.*
	Board AD10 - Synthesizer latch (contd.)	
R19	Met film 2kΩ 2% 1/4W	24773-280U
R20	Met film 2kΩ 2% 1/4W	24773-280U
R21	Met film 2kΩ 2% 1/4W	24773-280U
R22	Met film 2kΩ 2% 1/4W	24773-280U
R23	Met film 2kΩ 2% 1/4W	24773-280U
R24	Met film 2kΩ 2% 1/4W	24773-280U
R25	Met film 2kΩ 2% 1/4W	24773-280U
R26	Met film 2kΩ 2% 1/4W	24773-280U
51.	Board AE1 - Lamps	
	When ordering prefix with AE1.	
	Complete board	44828-104E
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	LED green	28624-111X
D4	LED yellow	28624-112M
D5	LED yellow	28624-112M
R1	Met film 750Ω 2% 1/4W	24773-270R
R2	Met film 220Ω 2% 1/4W	24773-257W
R3	Met film 15Ω 2% 1/4W	24773-229X
TR1	BC308	28433-455R

Circuit ref.	*Description*	*Code no.*
52.	Board AE2 - Remote lamp	
	When ordering prefix with AE2.	
	Complete board	44828-145F
D1	LED green, REMOTE	28624-111X
R1	Met film 150Ω 2% 1/4W	24773-253F
TR1	BC238	28452-781A
53.	Board AZ1 - Address select	
	When ordering prefix with AZ1.	
	Complete board	44827-741N
SA	ADDRESS switch bank	23467-311R

MECHANICAL PARTS

54.	Order without prefix.	
Item no.		
1	Upper cover, excluding fixing screws	35901-558E
2	Lower cover, excluding fixing screws	35901-922D
3	Front panel cover assembly complete	41690-219Z

Item no.	Description	Code no.
4	Trim (1 of 2)	37490-316N
5	Catch (1 of 2)	37574-540P
6	Spring (1 of 2)	31119-008V
7	Cover plate, excluding arm, clips, studs and screws	35902-326X
	Locating arm (1 of 2)	34900-453T
	Swivel clip, r.h.	34900-455X
	Swivel clip, l.h.	34900-456M
	Stud (1 of 2)	21186-365V
	Stud retaining washer (1 of 2)	21186-362J
8	Front foot (1 of 2) excluding fixing screws	37588-111K
9	Rear foot (1 of 2) excluding fixing screws and nut	22315-663B
10	Side foot (1 of 4)	22315-661C
11	Tilt stand	35116-109M
12	Rear stand plate (l.h.) excluding side feet and screws	34900-635K
13	Rear stand plate (r.h.) excluding screws	34900-636A
14	Front handle (1 of 2)	35852-115V
15	Trim	34217-122B
16	Plate, excluding side feet	35902-924E
17	Side carrying handle (1 of 2)	35890-011P
18	Casting (1 of 2)	35838-128G
19	Plate (1 of 2) excluding fixing screws	35464-122J
20	Spring (1 of 2)	35523-707E
21	Front panel (fascia only)	35901-790C
22	Window, FREQUENCY & LEVEL	37490-305B
23	Window, METER	37490-317L
24	Knob, SUPPLY	41149-029P
25	Knob, impedance	41146-011X
26	Knob, TUNING	41149-028T
27	Knob, FINE LEVEL	41149-017L
28	Keycap, kHz	37590-180D
29	Keycap, MHz	37590-181T
30	Keycap, dB	37590-182P
31	Keycap, white bar (1 of 3)	37590-183X
32	Keycap set, 0 to 9	23465-446Z
33	Keycap, C	37590-215D
34	Keycap, ENTER	23465-461G
35	Keycap, •	23465-460F
36	Keycap, +	23465-464W
37	Keycap, -	23465-463S
38	Keycap, &	37590-214W
39	Keycap, START	23465-450H
40	Keycap, CE	37590-216T
41	Heat sink assembly complete	44990-178W
42	LO lid assembly	41690-228L
43	Control unit lid assembly	41690-227N
44	RF unit lid assembly	41690-207T

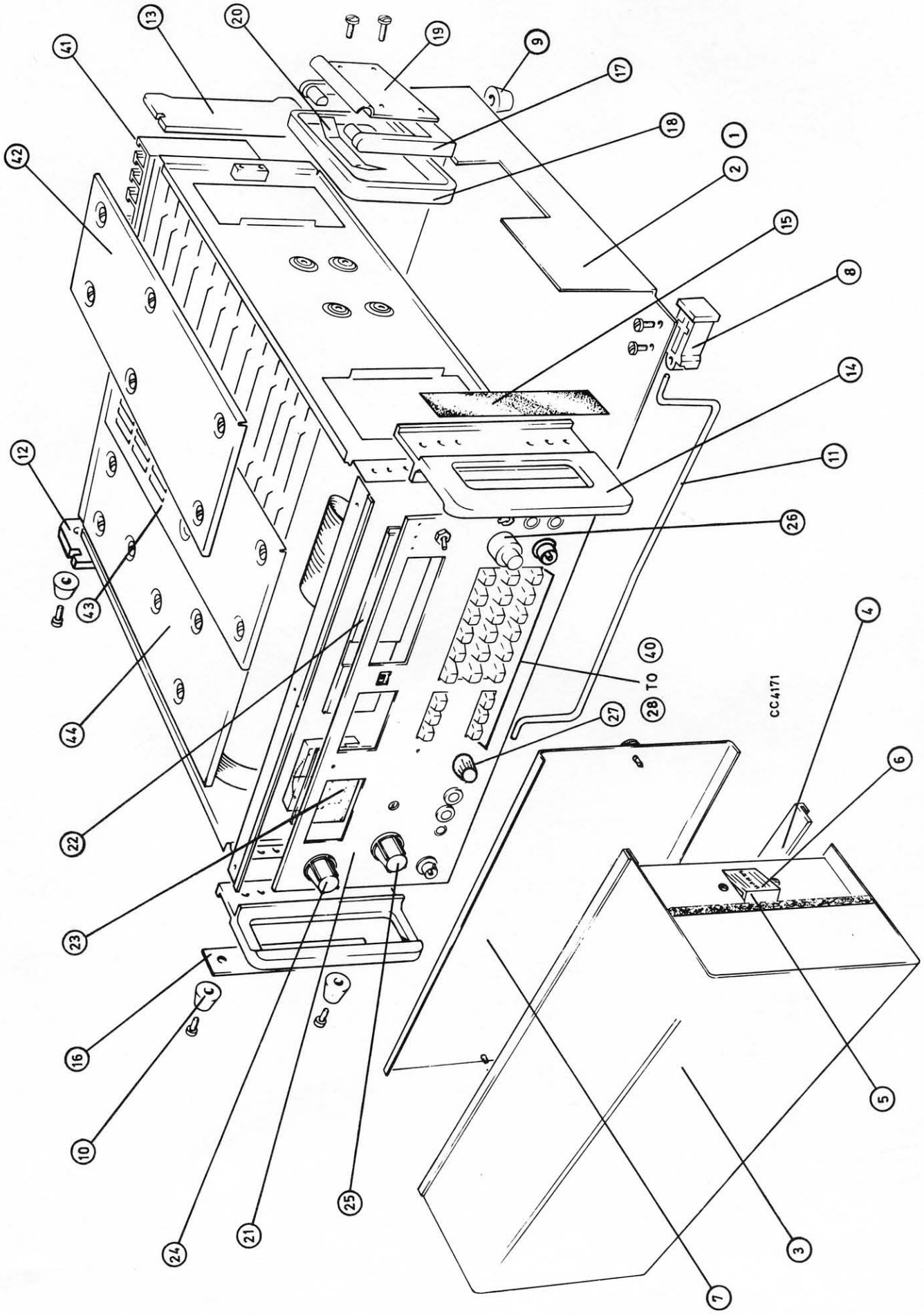


Fig. 1 TF 2357 - Mechanical parts

Chapter 7

SERVICING DIAGRAMS

CONTENTS

CIRCUIT NOTES

Component values

1. Resistors : No suffix = ohms, k = kilohms, M = Megohms.
Capacitors : No suffix = microfarads, p = picofarads.

Symbols

2. Symbols are to BS 3936 with the following additions :


Static sensitive component


Tag

Test point


Edge connector

Ferrite bead

Unit identification

PCB layouts

3. PCB layouts are shown as viewed from the component side.

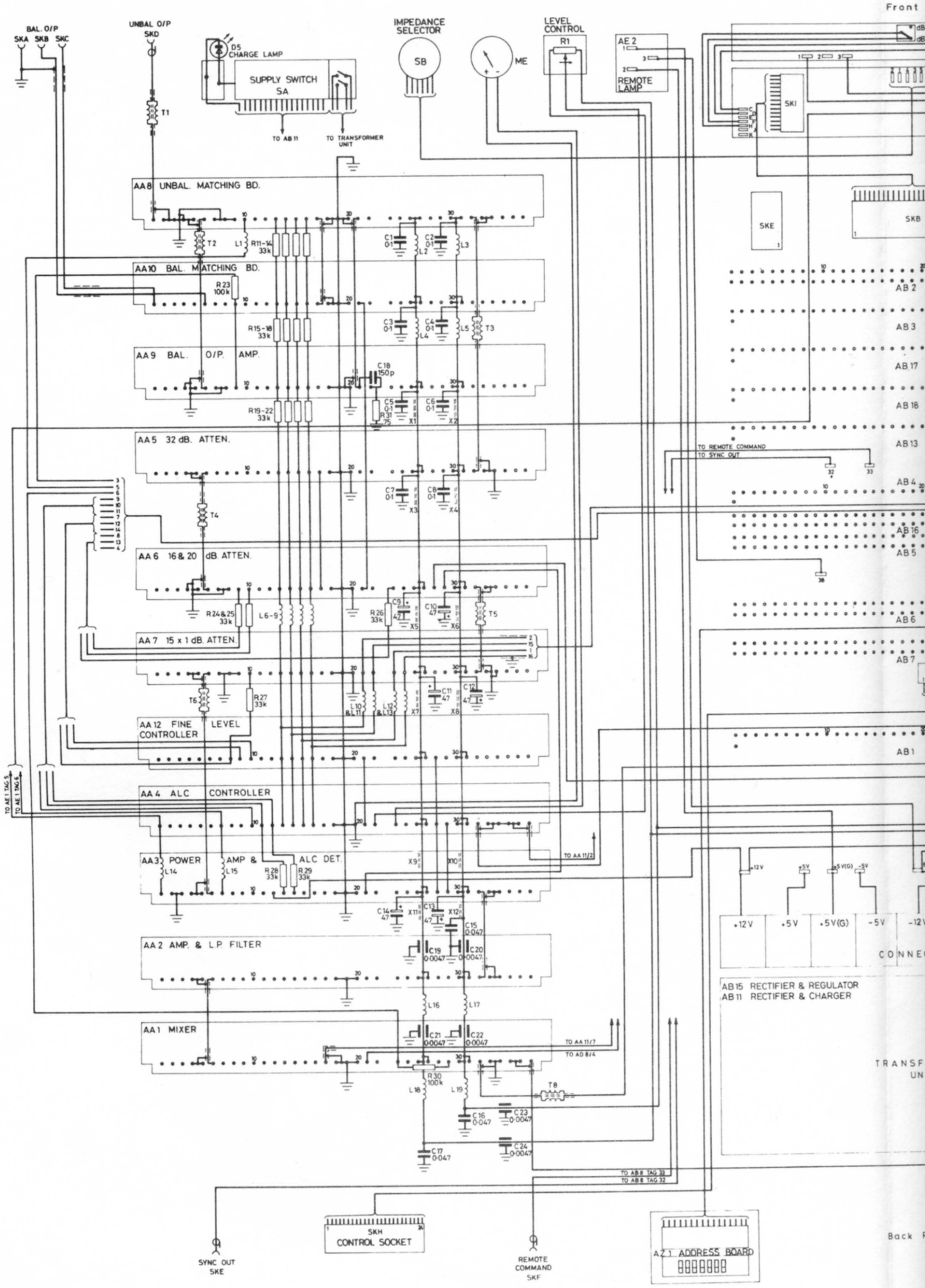
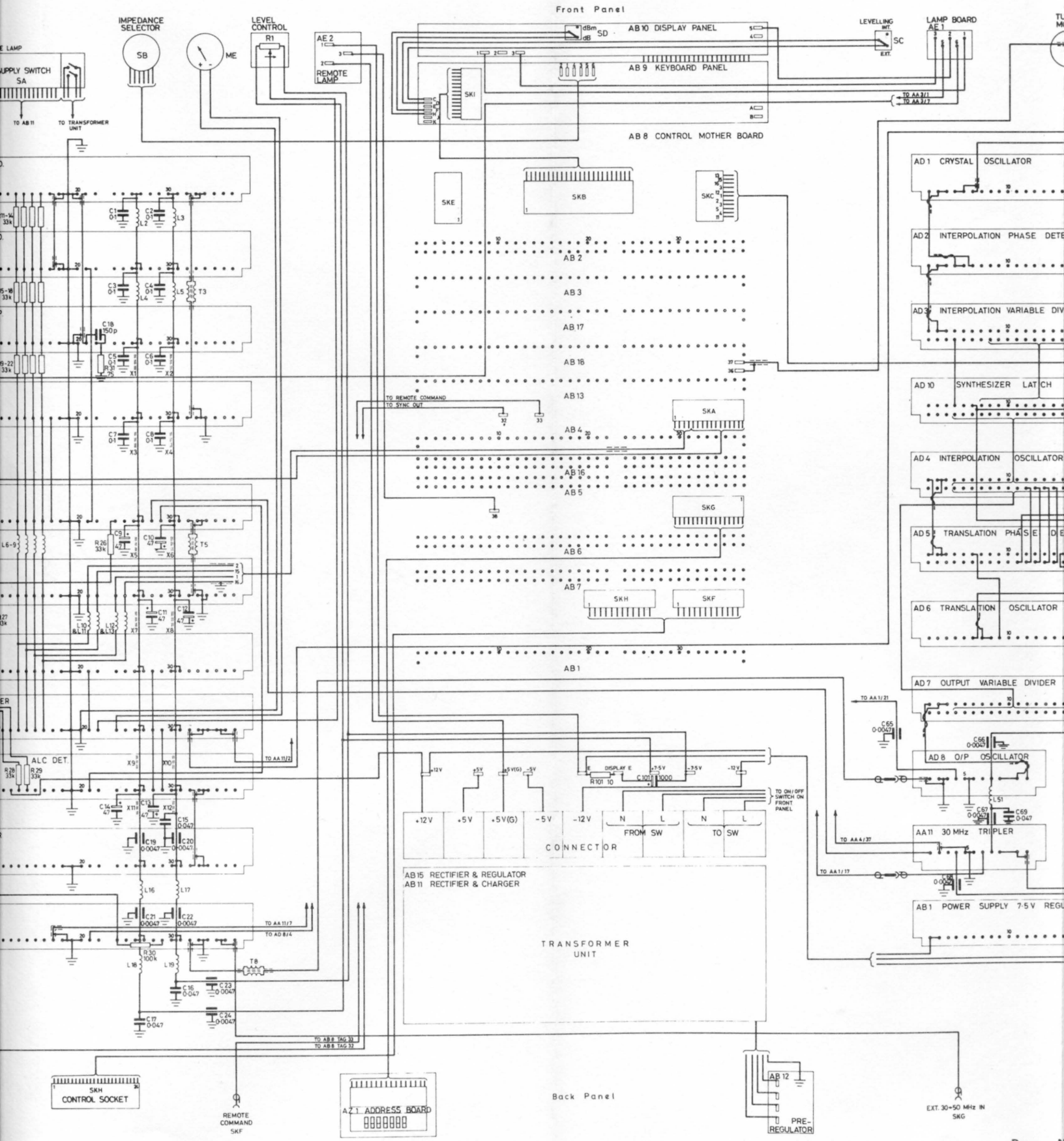


Fig. 1
May 80

Interco



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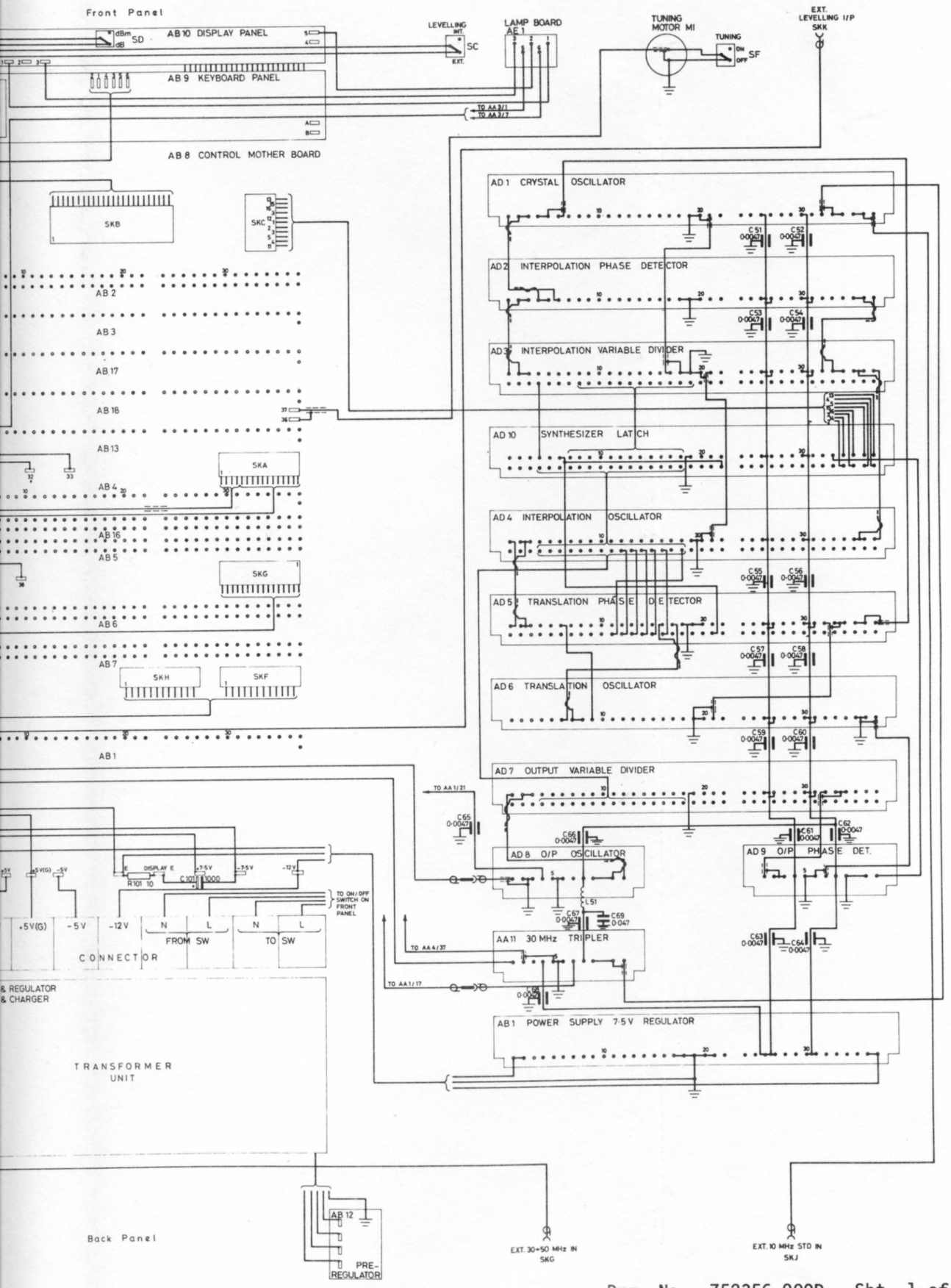
Interconnection diagram



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Interconnection diagram

Fig. 1

AB8 SKA (RF UNIT CONTROL)

SOURCE	PIN	DESTINATION	FUNCTION
AB2,26	1	AA4,15 AA12,15 AA7,15 AA6,15 AA5,15 AA9,15 AA10,15 AA8,15	RAM 1 OUT '1'
AB2,24	2	AA4,13 AA12,13 AA7,13 AA6,13 AA5,13 AA9,13 AA10,13 AA8,13	RAM 1 OUT '3'
AB4,32	3	AA9,9 AA10,9	BAL IMPEDANCE LATCH ENABLE
AB4,34	4	AA6,9	MUTE LATCH ENABLE
AB4,35	5	AA8,10	UNBAL IMPEDANCE LATCH ENABLE
AB4,27	6	AA1,29	EXT 30 to 50 MHz DETECT
AB4,37	7	AA7,10	1dB STEP LATCH ENABLE
AB6,9	8	AA6,24	RETURN TO LOCAL
AB4,30	9	AA4,10	ALC MODE LATCH ENABLE
AB4,29	10	AA3,13	LEVEL LOW
AB4,28	11	AA3,14	LEVEL HIGH
AB4,36	12	AA12,9	0.01 dB STEP LATCH ENABLE
AB4,33	13	AA6,10	16,20,32 BAL 32 dB STEP LATCH ENABLE
AB4,31	14	AA12,10	0.1 dB STEP LATCH ENABLE
AB2,27	15	AA4,14 AA12,14 AA7,14 AA6,14 AA5,14 AA9,14 AA10,14 AA8,14	RAM 1 OUT '2'
AB2,25	16	AA4,16 AA12,16 AA7,16 AA6,16 AA5,16 AA9,16 AA10,16 AA8,16	RAM 1 OUT '0'

AB8 SKB (FRONT PANEL)

SOURCE	PIN	DESTINATION	FUNCTION
0V	1		DISPLAY EARTH
AB13,9	2		COUNTER UP/DOWN
AB13,10	3		MOTOR LINE
AB2,11	4		ROM 0 OUT '2'
AB2,14	5		ROM 0 OUT '3'
AB2,13	6		ROM 0 OUT '0'
AB2,12	7		ROM 0 OUT '1'
	8		
	9		
	10		
AB3,32	11		ROM 0 IN '3'
+7.5V ~	12		
-7.5V ~	13		
AB3,31	14		ROM 0 IN '2'
AB3,35	15		ROM 0 IN '1'
AB3,36	16		ROM 0 IN '0'
	17		
	18		
	19		
	20		
AB2,20	21		RAM 0 OUT '0'
AB2,19	22		RAM 0 OUT '3'
AB2,21	23		RAM 0 OUT '1'
AB2,22	24		RAM 0 OUT '2'

AB8 SKC

SOURCE	PIN	DESTI
AB18,37	1	AD10,
AB2,8	2	AD10,
AB2,7	3	AD10,
AB2,2	4	AD10,
AB2,1	5	AD10,
	6	
	7	
	8	
	9	
	10	
	11	
AB2,37	12	AD10,
AB2,24	13	AD10,
AB2,26	14	AD10,
AB2,25	15	AD10,
AB2,27	16	AD10,

AB8 SKF (GPIB)

SOURCE	PIN	DESTINATION	FUNCTION
AB7,B17,B18	1	SKH,18	TWISTED PAIR EARTH (DAV)
AB7,B26	2	SKH,17	REN
AB7,B21	3	SKH,16	DIO 8
AB7,B22	4	SKH,15	DIO 7
AB7,B24	5	SKH,14	DIO 6
AB7,B25	6	SKH,13	DIO 5
	7		
	8		
AB7,B37	9	SKH,1	DIO 1
AB7,B36	10	SKH,2	DIO 2
AB7,B35	11	SKH,3	DIO 3
AB7,B34	12	SKH,4	DIO 4
AB7,B33	13	SKH,5	EOI
AB7,B29	14	SKH,6	DAV

AB8 SKG (GPIB ADDRESS)

SOURCE	PIN	DESTINATION	FUNCTION
EARTH	1		
EARTH	2		
EARTH	3		
EARTH	4	AZ1	EARTH RETURN
EARTH	5		
EARTH	6		
EARTH	7		
AB4,25	8	S7	AUTO MUTE ENABLE
AB16,B29	9	S6	CONTROLLER ENABLE
AB6,33	10	S5	ADDRESS A5
AB6,34	11	S4	ADDRESS A4
AB6,35	12	S3	ADDRESS A3
AB6,36	13	S2	ADDRESS A2
AB6,37	14	S1	ADDRESS A1

AB8 SKH

SOURCE	PIN	DESTI
AB7,B19,B20	1	SKH,2
AB7,B17,B18	2	SKH,2
AB7,B17,B18	3	SKH,2
AB7,B17,B18	4	SKH,2
AB7,B17,B18	5	SKH,2
AB7,B17,B18	6	SKH,1
AB7,B17,B18	7	
	8	
AB7,B32	9	SKH,7
AB7,B31	10	SKH,8
AB7,B28	11	SKH,9
AB7,B30	12	SKH,1
AB7,B27	13	SKH,1
	14	

Motherboard term

Fig. 2

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AB8 SKB (FRONT PANEL)

ON	SOURCE	PIN	DESTINATION	FUNCTION
OUT '1'	0V	1		DISPLAY EARTH
	AB13,9	2		COUNTER UP/DOWN
	AB13,10	3		MOTOR LINE
OUT '3'	AB2,11	4		ROM 0 OUT '2'
	AB2,14	5		ROM 0 OUT '3'
PEDANCE LATCH ENABLE	AB2,13	6		ROM 0 OUT '0'
ATCH ENABLE	AB2,12	7		ROM 0 OUT '1'
IMPEDANCE LATCH ENABLE		8		
to 50 MHz DETECT		9		
EP LATCH ENABLE		10		
TO LOCAL	AB3,32	11		ROM 0 IN '3'
DE LATCH ENABLE	+7.5V ~~~	12		
LOW	-7.5V ~~~	13		
HIGH	AB3,31	14		ROM 0 IN '2'
B STEP LATCH ENABLE	AB3,35	15		ROM 0 IN '1'
32 BAL 32 dB STEP LATCH ENABLE	AB3,36	16		ROM 0 IN '0'
STEP LATCH ENABLE		17		
OUT '2'		18		
		19		
		20		
OUT '0'	AB2,20	21		RAM 0 OUT '0'
	AB2,19	22		RAM 0 OUT '3'
	AB2,21	23		RAM 0 OUT '1'
	AB2,22	24		RAM 0 OUT '2'

AB8 SKC (SYNTHESISER)

SOURCE	PIN	DESTINATION	FUNCTION
AB18,37	1	AD10,20	ANALOGUE TEST
AB2,8	2	AD10,B34	ROM 1 OUT '0'
AB2,7	3	AD10,B35	ROM 1 OUT '3'
AB2,2	4	AD10,B37	ROM 1 OUT '2'
AB2,1	5	AD10,B36	ROM 1 OUT '1'
	6		
	7		
	8		
	9		
	10		
	11		
AB2,37	12	AD10,21	TEST
AB2,24	13	AD10,37	RAM 1 OUT '3'
AB2,26	14	AD10,34	RAM 1 OUT '1'
AB2,25	15	AD10,36	RAM 1 OUT '0'
AB2,27	16	AD10,35	RAM 1 OUT '2'

AB8 SKE (EXPANSION SKT)

SOURCE	PIN	DESTINATION	FUNCTION
	1		
	2		
	3		
AB2,37	4		TEST
AB2,6	5		ROM 2 OUT '0'
AB2,4	6		ROM 2 OUT '1'
AB2,3	7		ROM 2 OUT '2'
AB2,5	8		ROM 2 OUT '3'
AB2,24	9		RAM 1 OUT '3'
AB2,27	10		RAM 1 OUT '2'
AB2,26	11		RAM 1 OUT '1'
AB2,25	12		RAM 1 OUT '0'
	13		
	14		
	15		
	16		

AB8 SKG (GPIB ADDRESS)

N	SOURCE	PIN	DESTINATION	FUNCTION
D PAIR EARTH (DAV)	EARTH	1		
	EARTH	2		
	EARTH	3		
	EARTH	4	AZ1	EARTH RETURN
	EARTH	5		
	EARTH	6		
	EARTH	7		
	AB4,25	8	S7	AUTO MUTE ENABLE
	AB16,B29	9	S6	CONTROLLER ENABLE
	AB6,33	10	S5	ADDRESS A5
	AB6,34	11	S4	ADDRESS A4
	AB6,35	12	S3	ADDRESS A3
	AB6,36	13	S2	ADDRESS A2
	AB6,37	14	S1	ADDRESS A1

AB8 SKH (GPIB)

SOURCE	PIN	DESTINATION	FUNCTION
AB7,B19,B20	1	SKH,24	DATA EARTH
AB7,B17,B18	2	SKH,23	TWISTED PAIR EARTH (ATN)
AB7,B17,B18	3	SKH,22	TWISTED PAIR EARTH (SRQ)
AB7,B17,B18	4	SKH,21	TWISTED PAIR EARTH (IFC)
AB7,B17,B18	5	SKH,20	TWISTED PAIR EARTH (NDAC)
AB7,B17,B18	6	SKH,19	TWISTED PAIR EARTH (NRFD)
AB7,B17,B18	7		
	8		
AB7,B32	9	SKH,7	NRFD
AB7,B31	10	SKH,8	NDAC
AB7,B28	11	SKH,9	IFC
AB7,B30	12	SKH,10	SRQ
AB7,B27	13	SKH,11	ATN
	14		

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Motherboard terminations

AB8 SKC (SYNTHESISER)

SOURCE	PIN	DESTINATION	FUNCTION
AB18,37	1	AD10,20	ANALOGUE TEST
AB2,8	2	AD10,B34	ROM 1 OUT '0'
AB2,7	3	AD10,B35	ROM 1 OUT '3'
AB2,2	4	AD10,B37	ROM 1 OUT '2'
AB2,1	5	AD10,B36	ROM 1 OUT '1'
	6		
	7		
	8		
	9		
	10		
	11		
AB2,37	12	AD10,21	TEST
AB2,24	13	AD10,37	RAM 1 OUT '3'
AB2,26	14	AD10,34	RAM 1 OUT '1'
AB2,25	15	AD10,36	RAM 1 OUT '0'
AB2,27	16	AD10,35	RAM 1 OUT '2'

AB8 SKE (EXPANSION SKT)

SOURCE	PIN	DESTINATION	FUNCTION
	1		
	2		
	3		
AB2,37	4		TEST
AB2,6	5		ROM 2 OUT '0'
AB2,4	6		ROM 2 OUT '1'
AB2,3	7		ROM 2 OUT '2'
AB2,5	8		ROM 2 OUT '3'
AB2,24	9		RAM 1 OUT '3'
AB2,27	10		RAM 1 OUT '2'
AB2,26	11		RAM 1 OUT '1'
AB2,25	12		RAM 1 OUT '0'
	13		
	14		
	15		
	16		

AB8 SKH (GPIB)

SOURCE	PIN	DESTINATION	FUNCTION
AB7,B19,B20	1	SKH,24	DATA EARTH
AB7,B17,B18	2	SKH,23	TWISTED PAIR EARTH (ATN)
AB7,B17,B48	3	SKH,22	TWISTED PAIR EARTH (SRQ)
AB7,B17,B18	4	SKH,21	TWISTED PAIR EARTH (IFC)
AB7,B17,B18	5	SKH,20	TWISTED PAIR EARTH (NDAC)
AB7,B17,B18	6	SKH,19	TWISTED PAIR EARTH (NRFD)
AB7,B17,B18	7		
	8		
AB7,B32	9	SKH,7	NRFD
AB7,B31	10	SKH,8	NDAC
AB7,B28	11	SKH,9	IFC
AB7,B30	12	SKH,10	SRQ
AB7,B27	13	SKH,11	ATN
	14		

AB8 TAGS (TEST POINTS UNLESS DESTINATION SHOWN)

SOURCE	TAG	DESTINATION	FUNCTION
AB3,32	1		ROM 0 IN '3'
AB3,36	2		ROM 0 IN '0'
AB3,35	3		ROM 0 IN '1'
AB3,31	4		ROM 0 IN '2'
AB2,8	5		ROM 1 OUT '0'
AB2,7	6		ROM 1 OUT '3'
AB2,1	7		ROM 1 OUT '1'
AB2,2	8		ROM 1 OUT '2'
AB2,11	9		ROM 0 OUT '2'
AB2,12	10		ROM 0 OUT '1'
AB3,26	11		ROM 3 IN '0'
AB2,22	12		RAM 0 OUT '2'
AB2,21	13		RAM 0 OUT '1'
AB2,20	14		RAM 0 OUT '0'
AB2,19	15		RAM 0 OUT '3'
AB2,14	16		ROM 0 OUT '3'
AB2,13	17		ROM 0 OUT '0'
AB2,10	18		ROM 3 OUT '2'
AB2,6	19		ROM 2 OUT '0'
AB2,3	20		ROM 2 OUT '2'
AB2,5	21		ROM 2 OUT '3'
AB2,4	22		ROM 2 OUT '1'
AB2,16	23		ROM 3 OUT '0'
AB2,15	24		ROM 3 OUT '3'
AB2,37	25		TEST
AB2,27	26		RAM 1 OUT '2'
AB2,26	27		RAM 1 OUT '1'
AB3,25	28		ROM 3 IN '3'
AB2,24	29		RAM 1 OUT '3'
AB2,25	30		RAM 1 OUT '0'
AB2,9	31		ROM 3 OUT '1'
AB4,10	32	SKE. REAR PANEL	SYNC OUTPUT
AB4,15	33	SKF. REAR PANEL	REMOTE COMMAND INPUT
AB3,24	34		ROM 3 IN '2'
AB3,27	35		ROM 3 IN '1'
AB13,36	36	MOTOR. FWONT PANEL	MOTOR EARTH RETURN } J0-AX
AB13,37	37	MOTOR, FRONT PANEL	MOTOR FEED } J0-AX
AB6,10	38	AE2,3 FRONT PANEL	"REMOTE LAMP" OUTPUT

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therboard terminations

Fig. 2

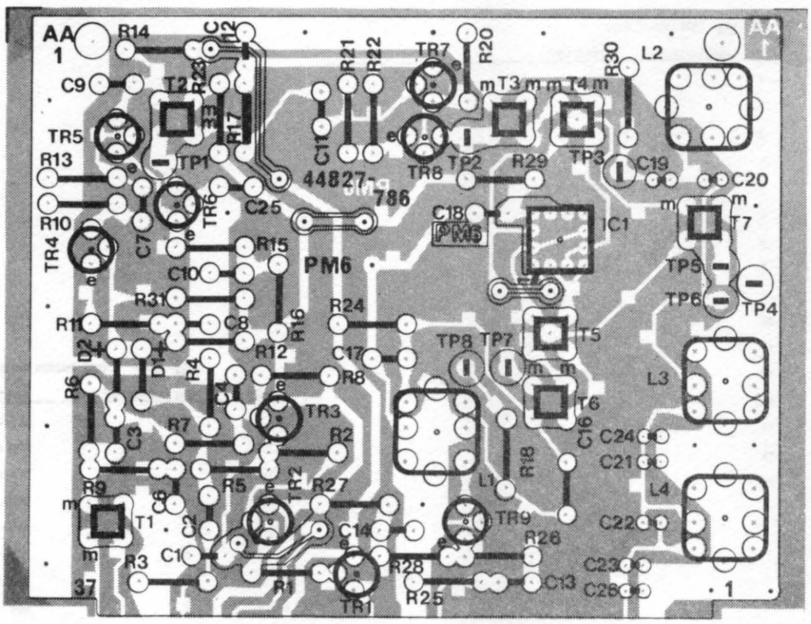


Fig. 3a Board AA1

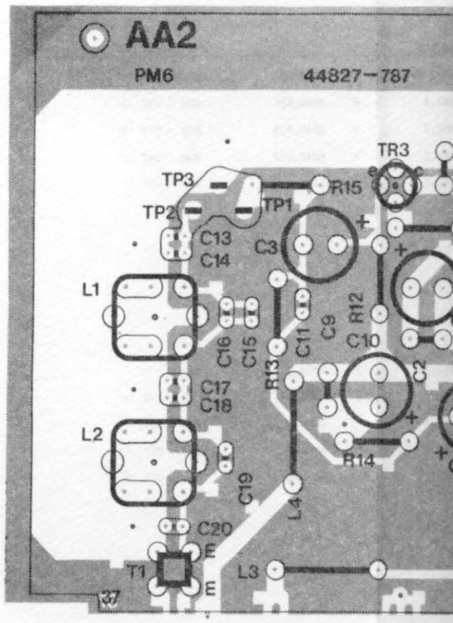


Fig. 3b Boar

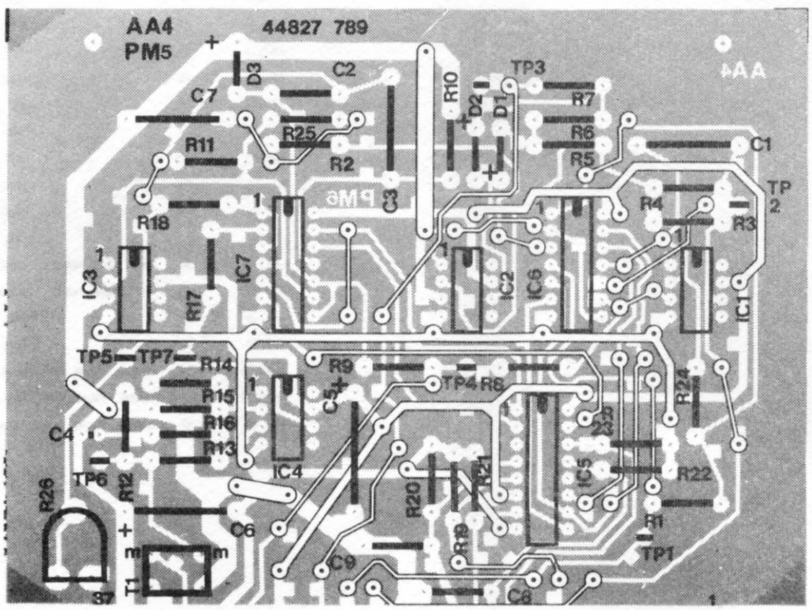


Fig. 3d Board AA4

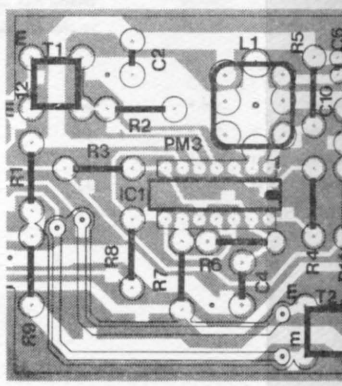
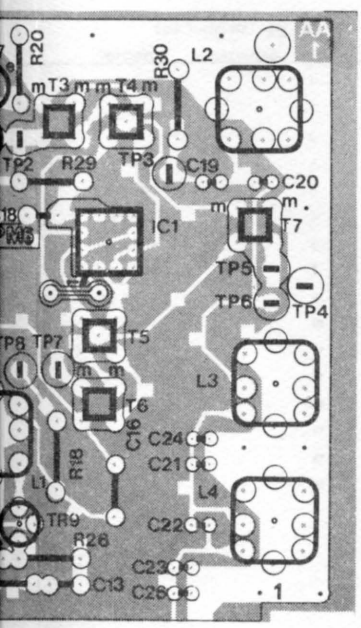


Fig. 3e Boar

Component layout



oard AA1

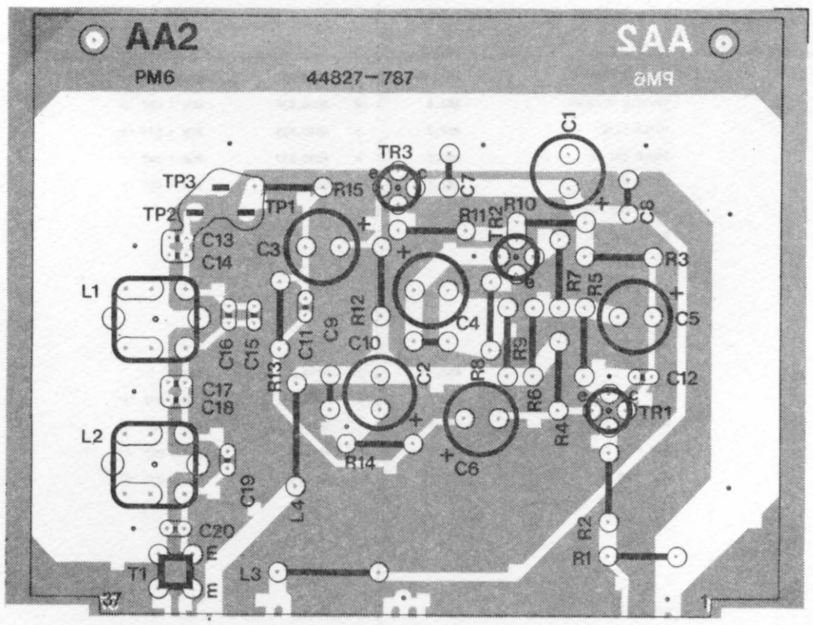
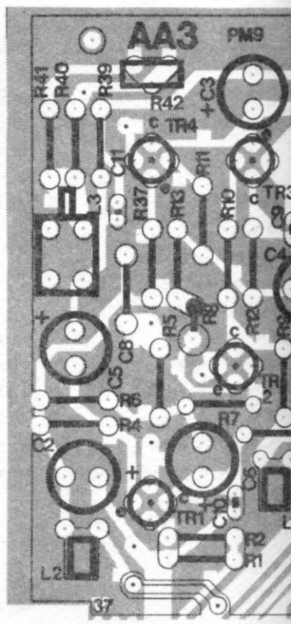


Fig. 3b Board AA2



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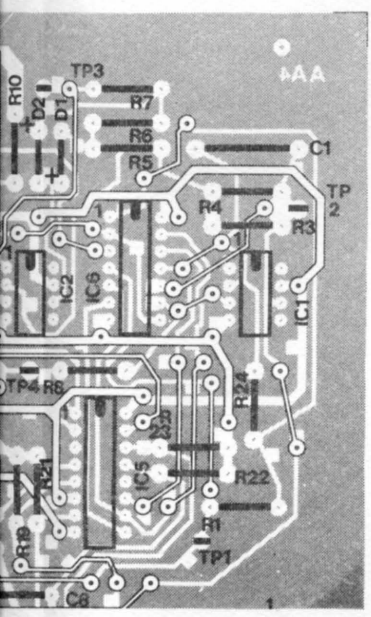


ard AA4

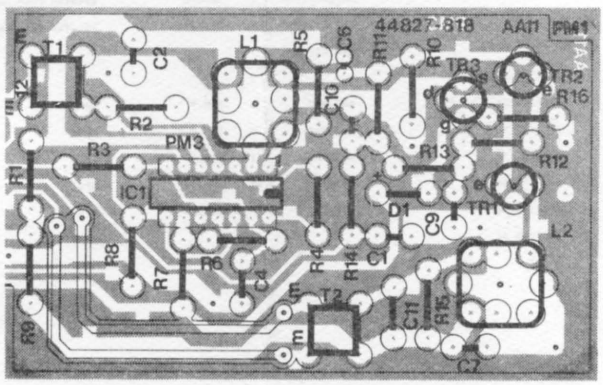
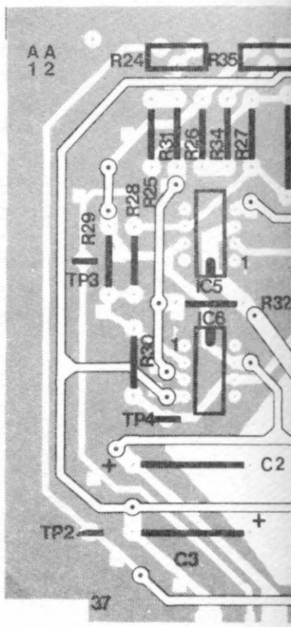


Fig. 3e Board AA11



Fig

Component layouts

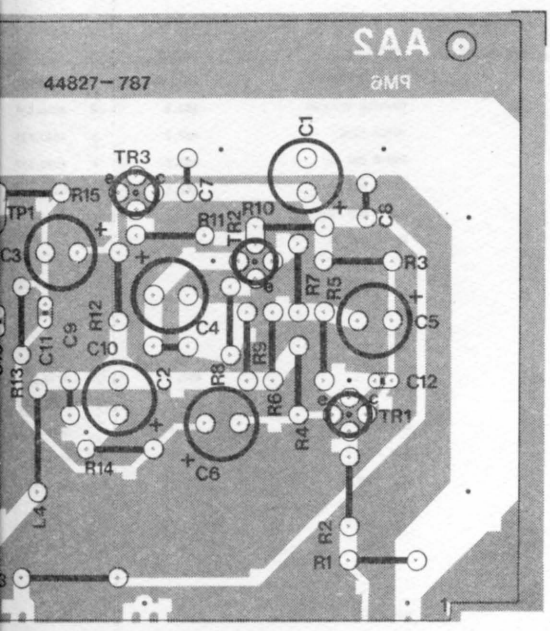


Fig. 3b Board AA2

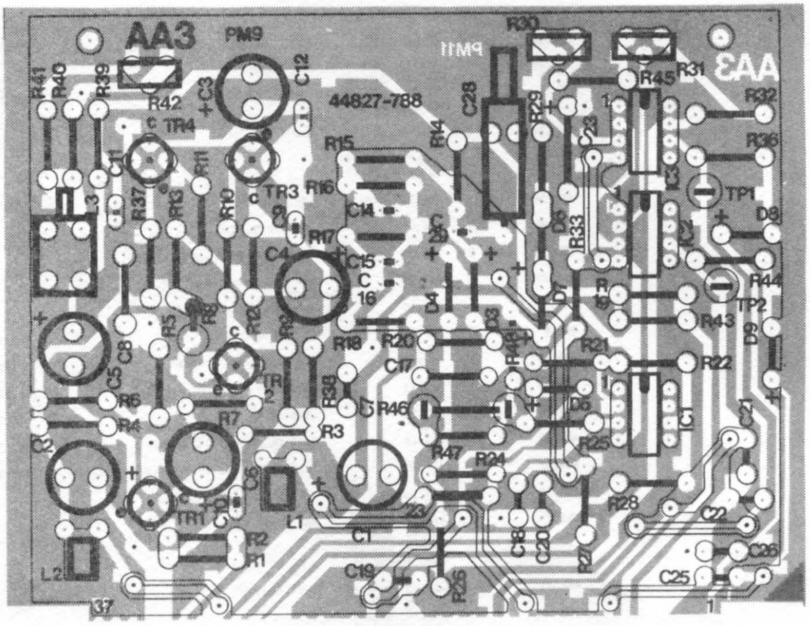


Fig. 3c Board AA3

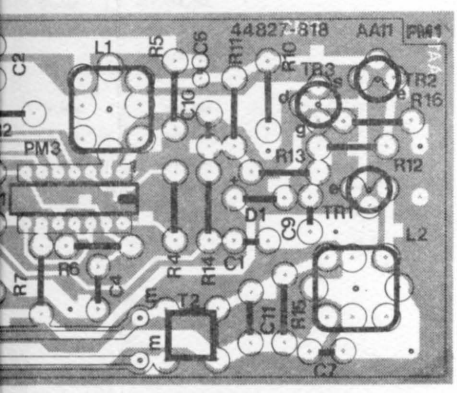


Fig. 3e Board AA11

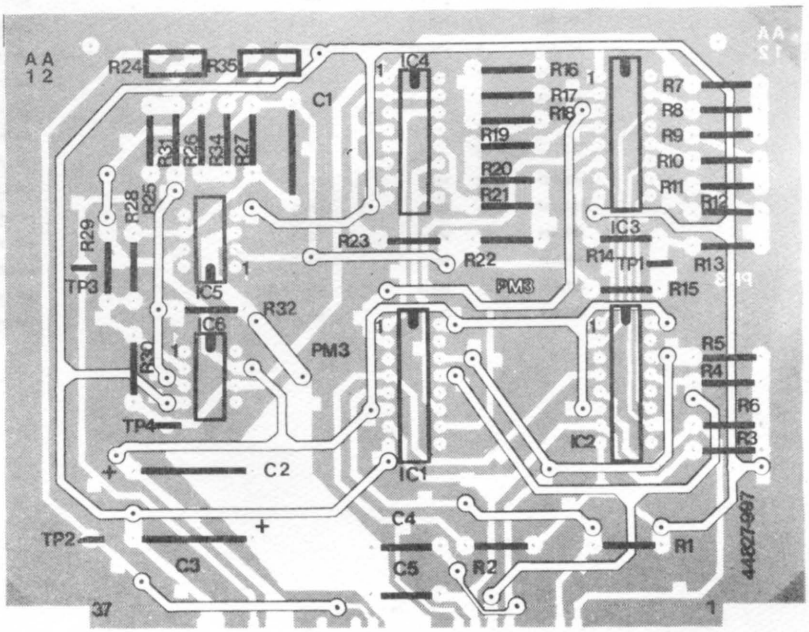
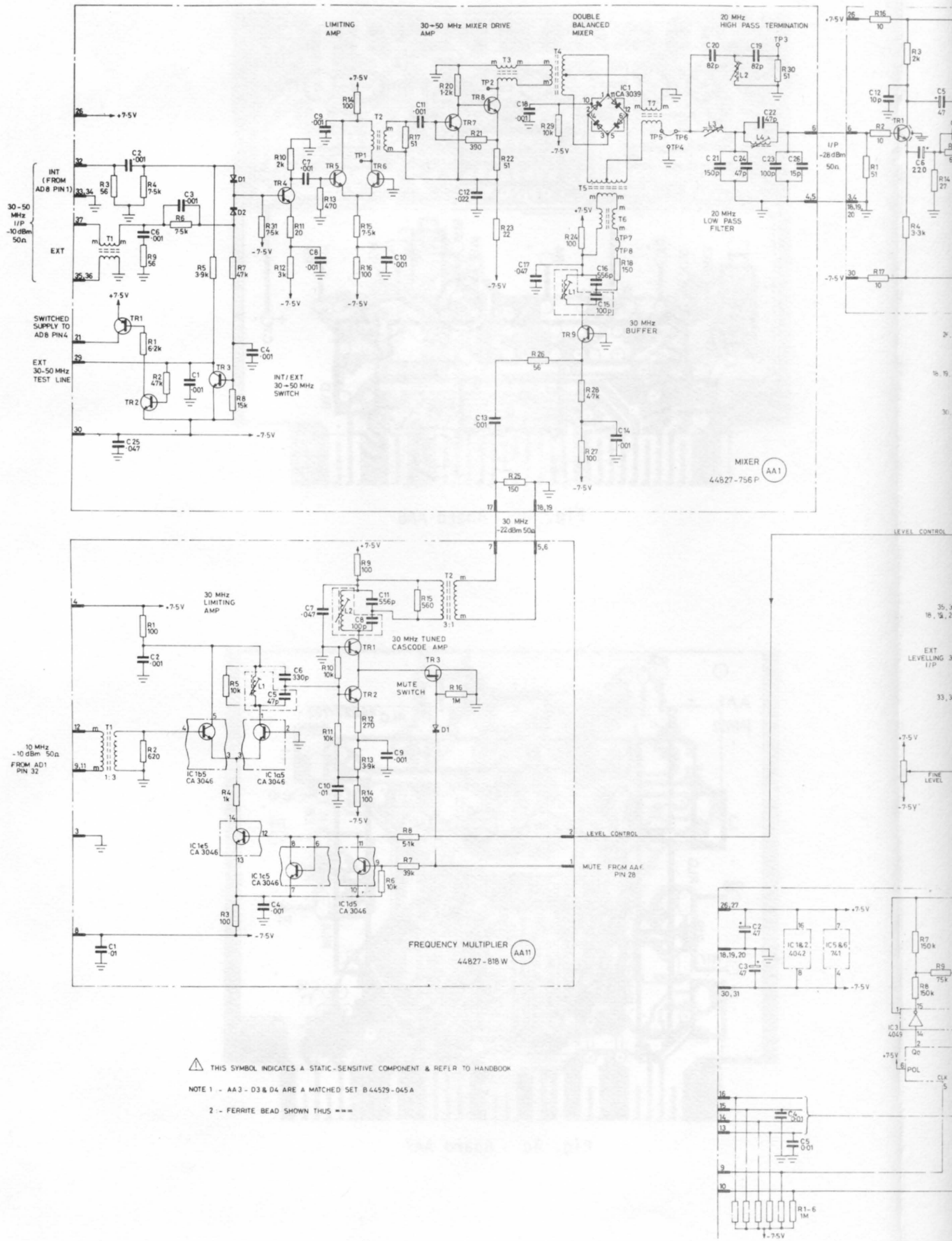


Fig. 3f Board AA12

omponent layouts

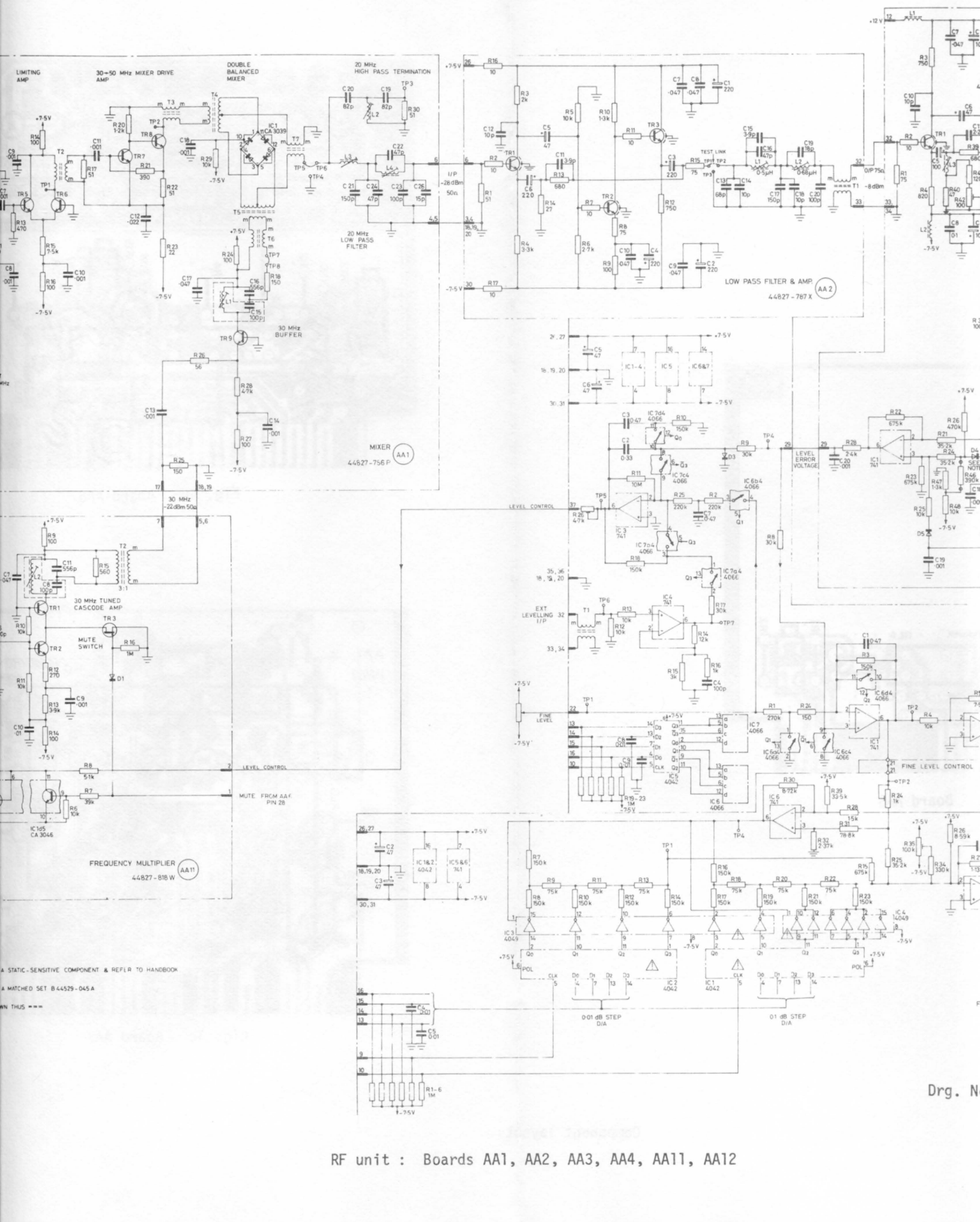


⚠ THIS SYMBOL INDICATES A STATIC-SENSITIVE COMPONENT & REFER TO HANDBOOK

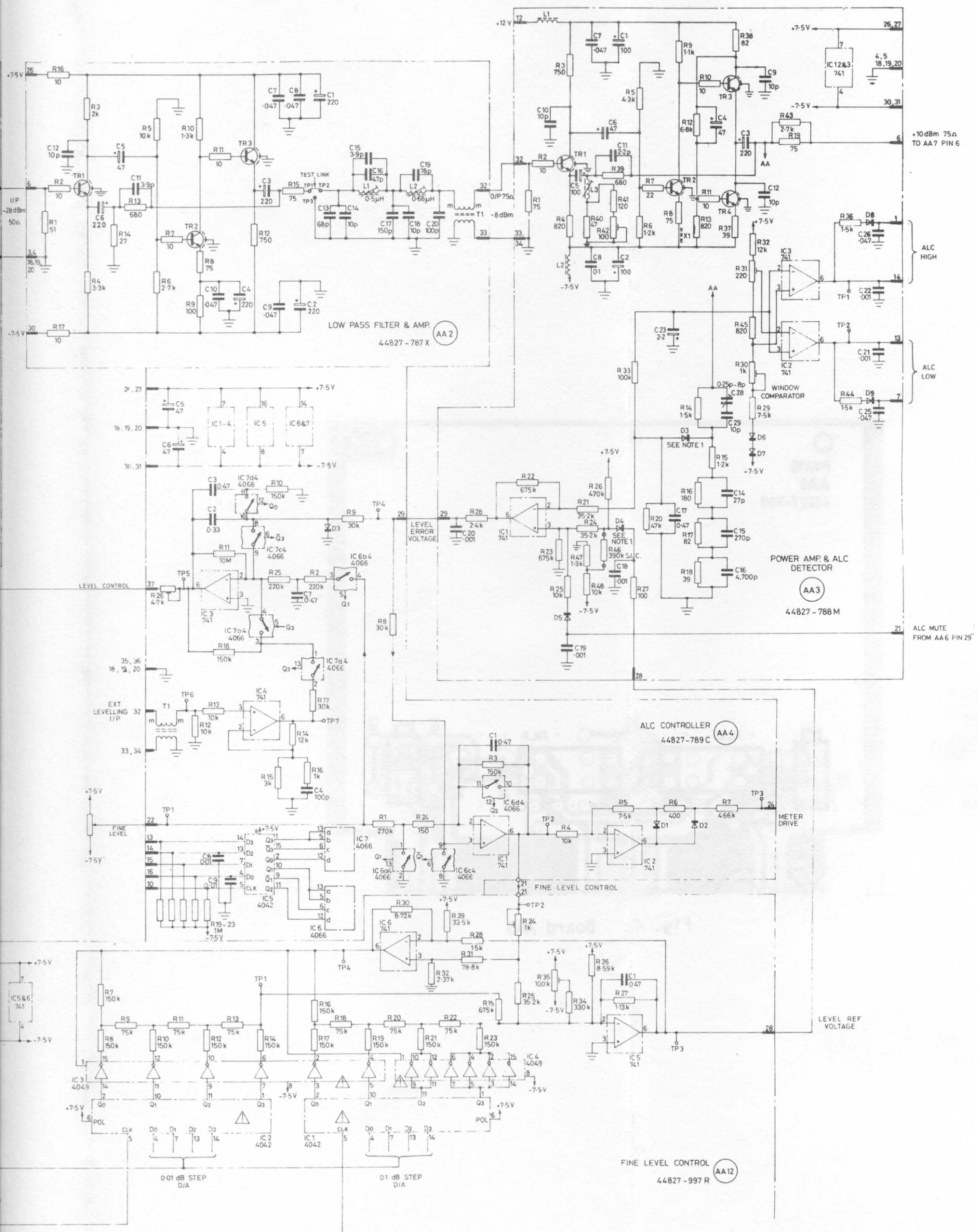
NOTE 1 - AA3-03 & 04 ARE A MATCHED SET B44529-045A

2 - FERRITE BEAD SHOWN THUS ===

RF unit : Boards AA1, AA2,



RF unit : Boards AA1, AA2, AA3, AA4, AA11, AA12



Drg. No. Z 44990-192B Sht. 1 of 3 Iss. 2

Fig. 3

ards AA1, AA2, AA3, AA4, AA11, AA12

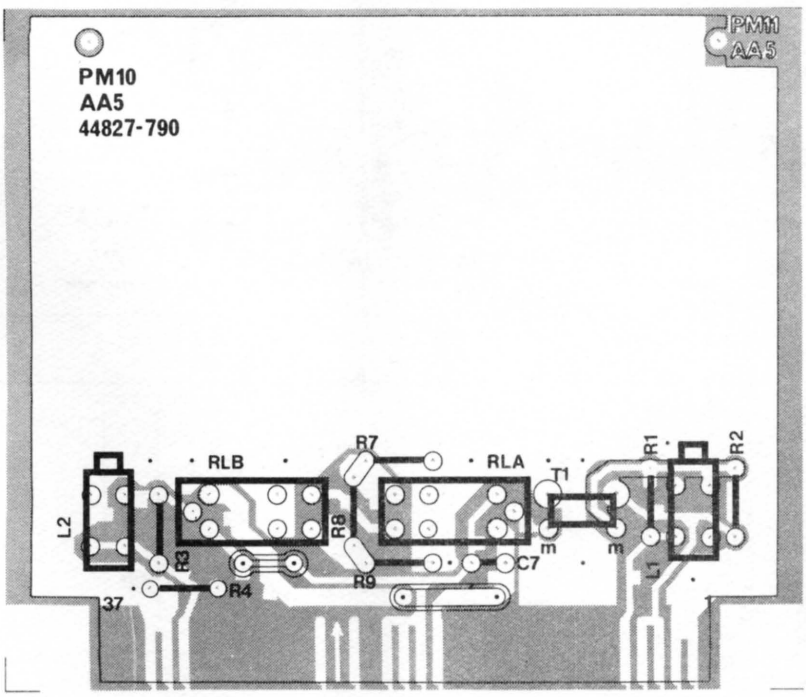


Fig. 4a Board AA5

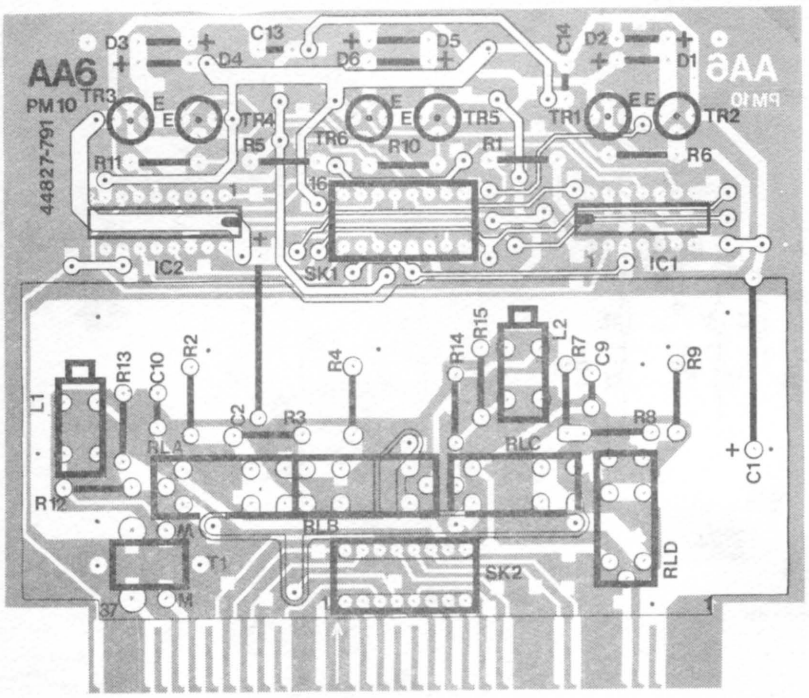


Fig. 4b Board AA6

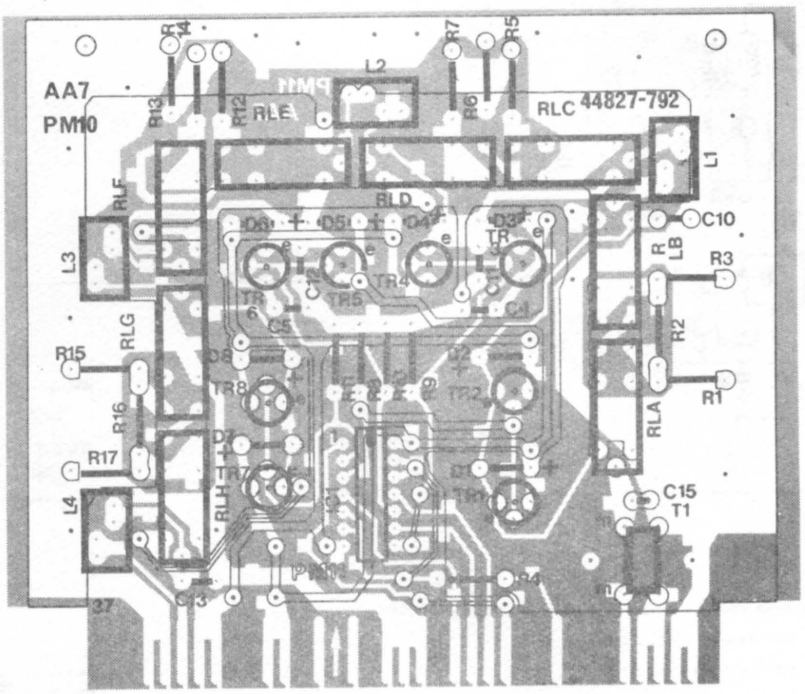


Fig. 4c Board AA7

ent layouts

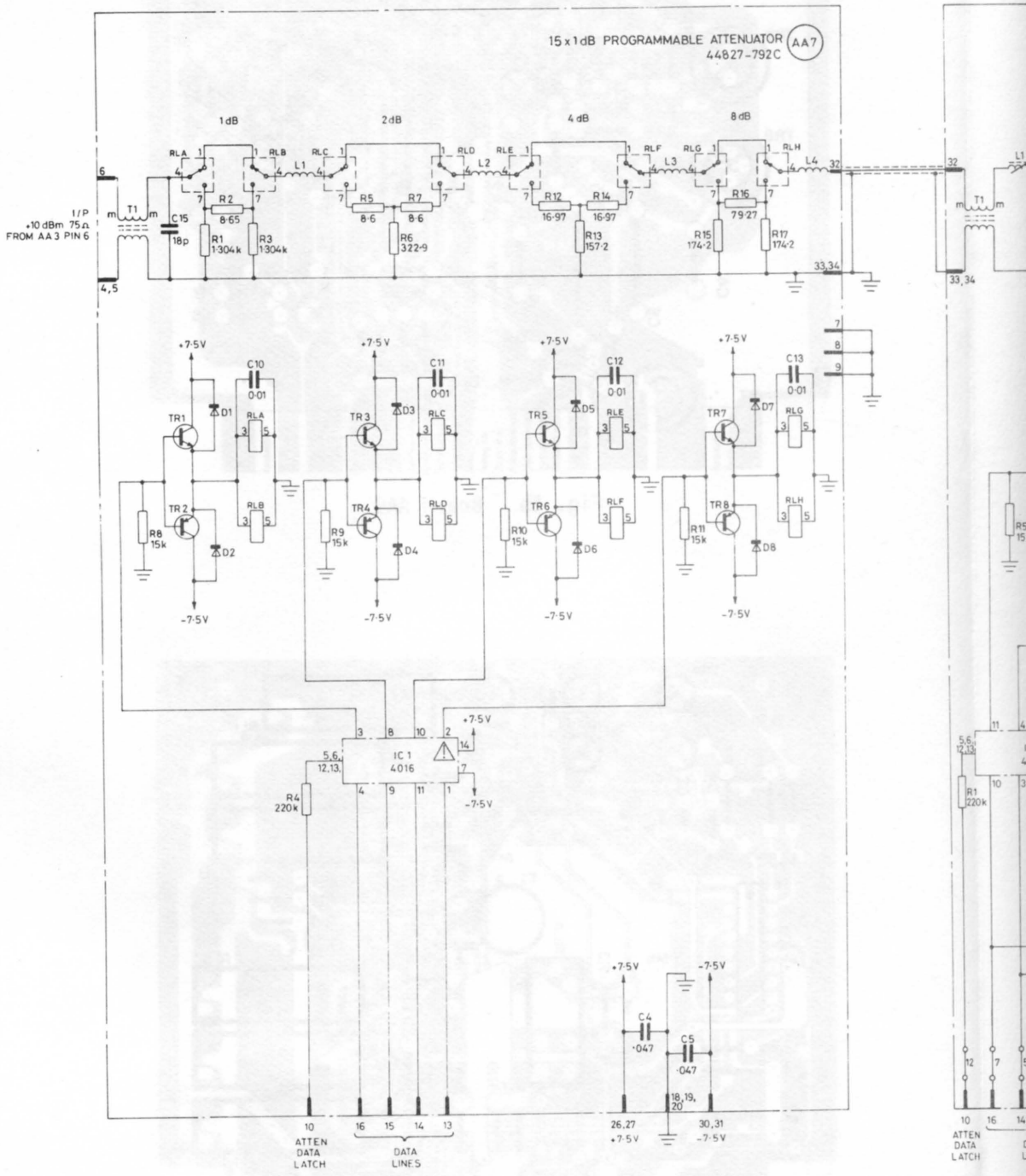


Fig. 4

RF unit : Boards A

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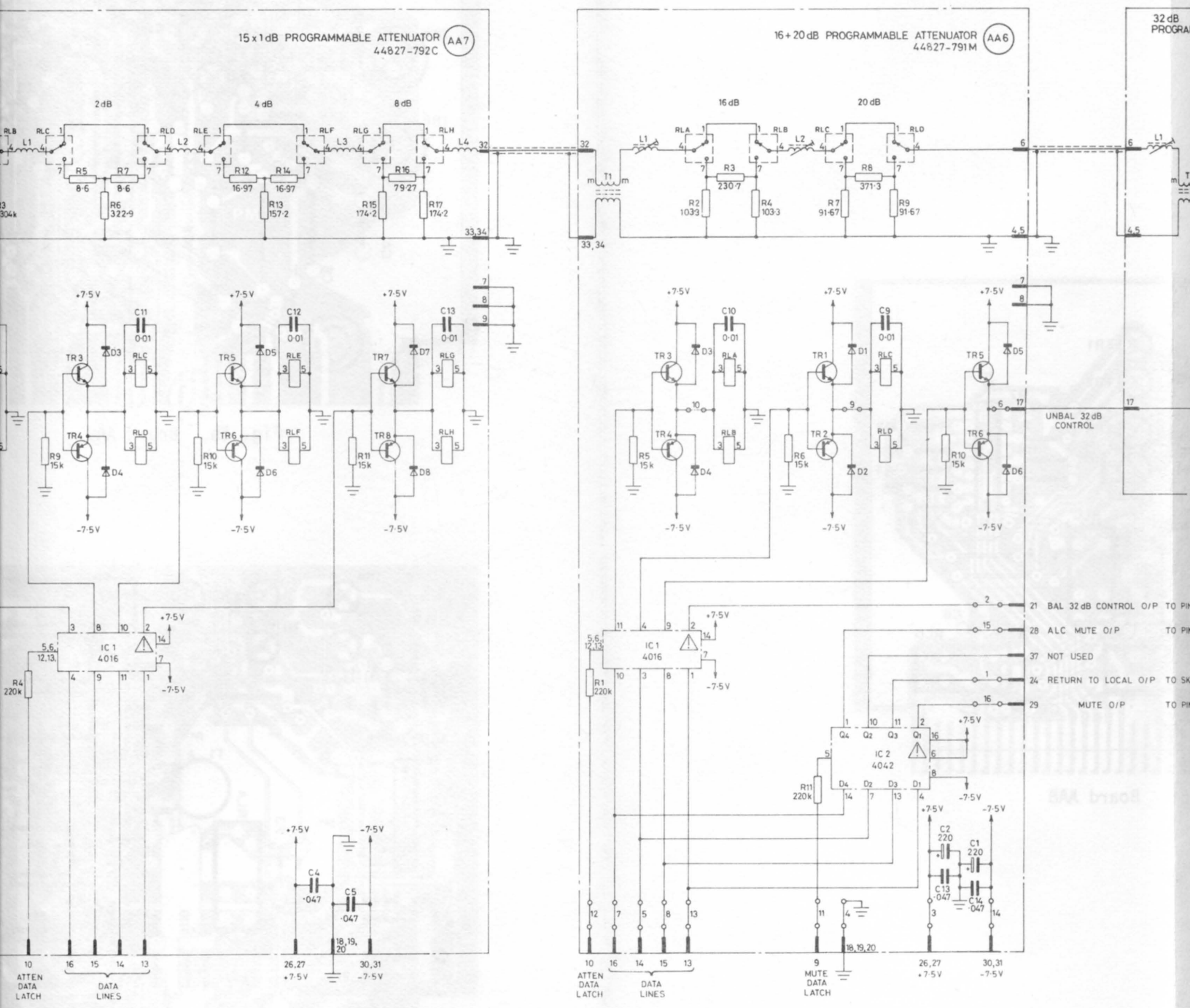
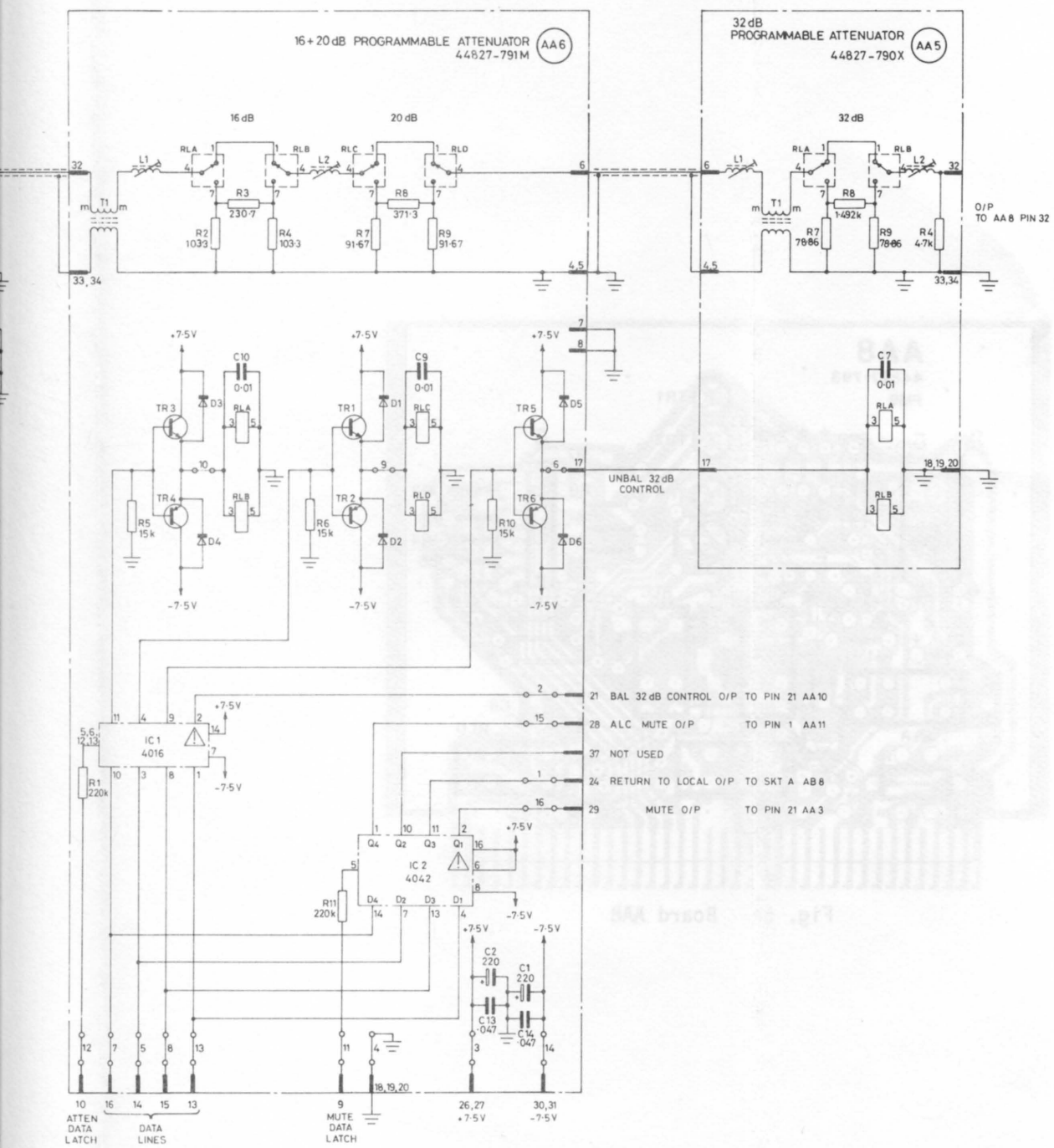


Drg. No. Z 44990-192B S

RF unit : Boards AA5, AA6, AA7



Drg. No. Z 44990-192B Sht. 2 of 3, Iss. 1

it : Boards AA5, AA6, AA7

Fig. 4

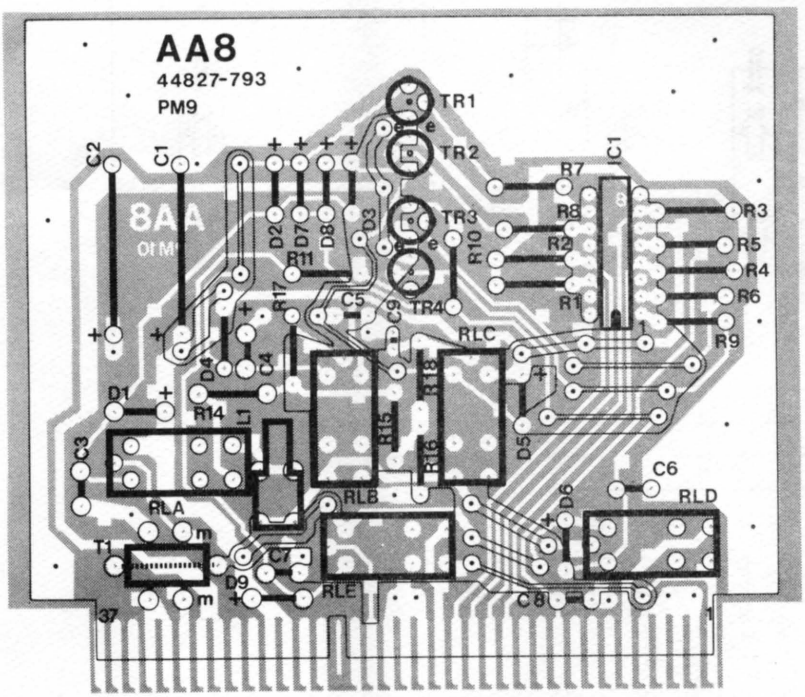


Fig. 5a Board AA8

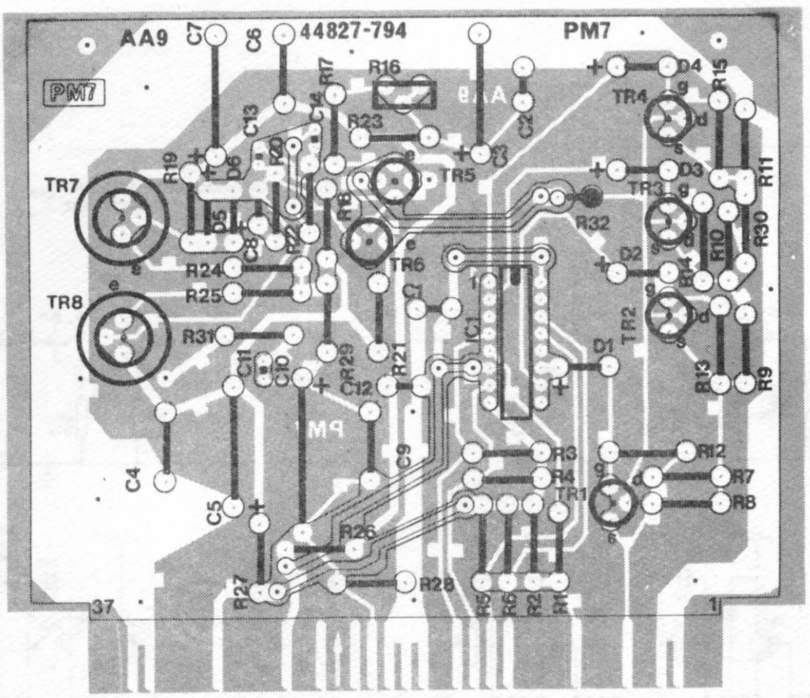


Fig. 5b Board AA9

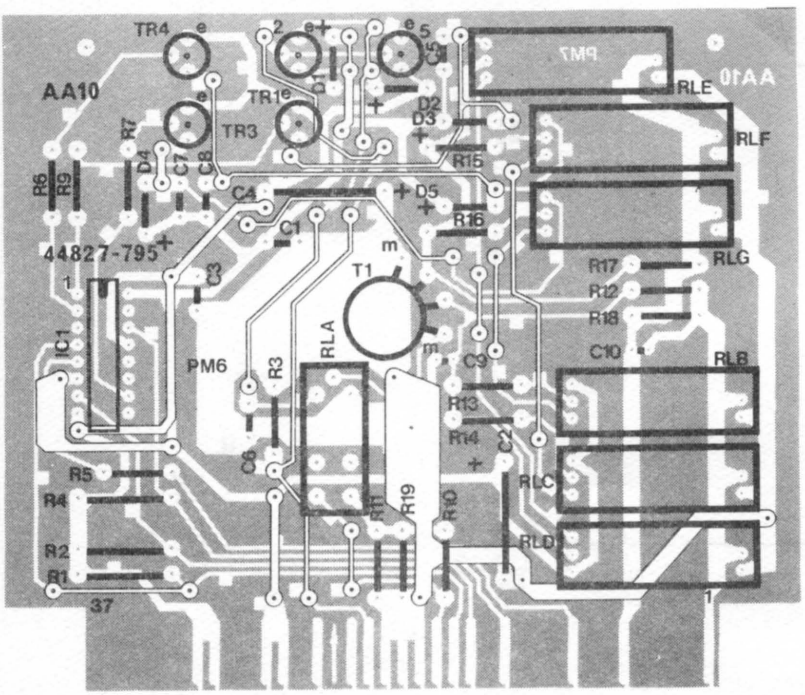


Fig. 5c Board AA10

ment layouts

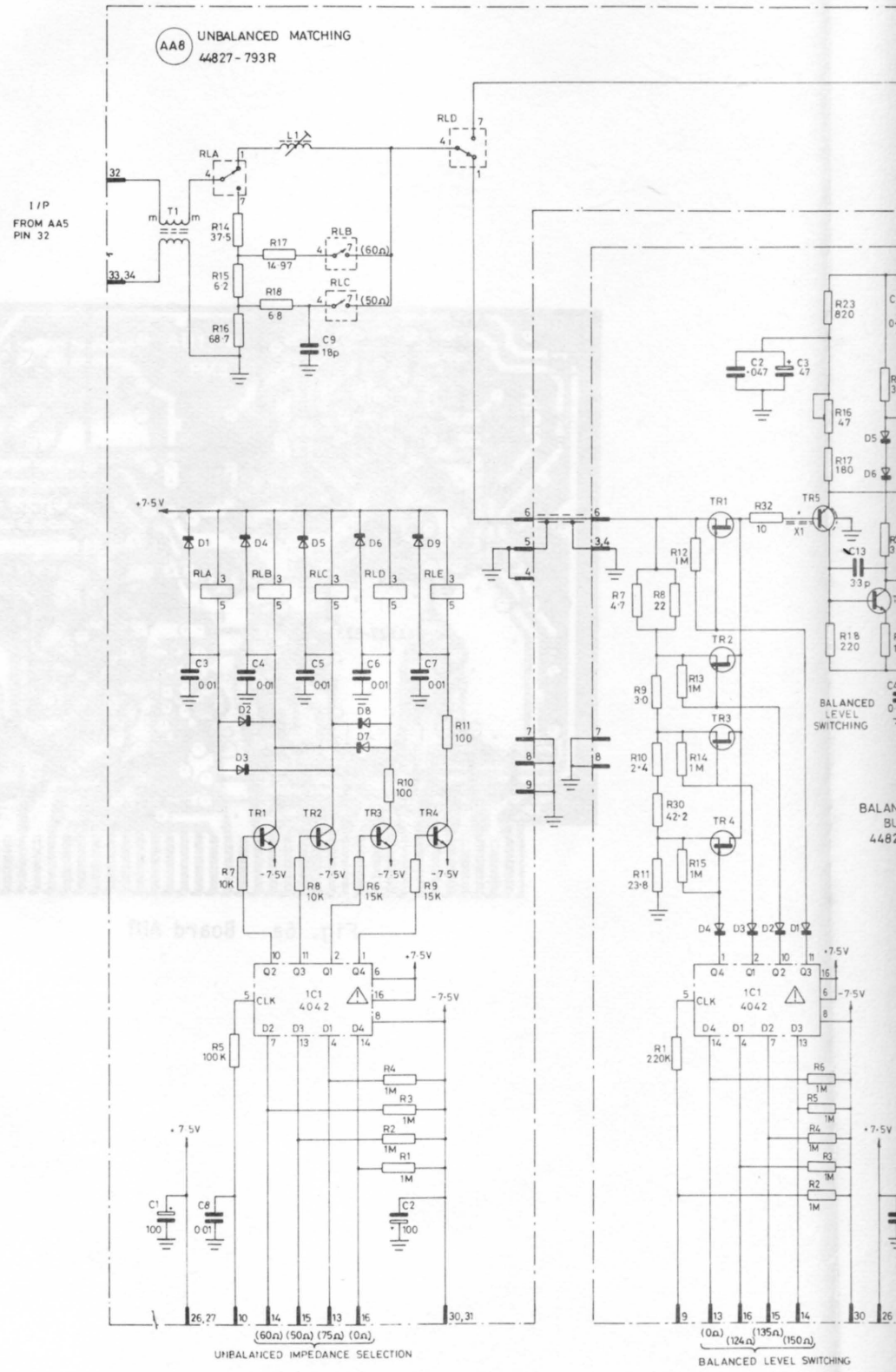
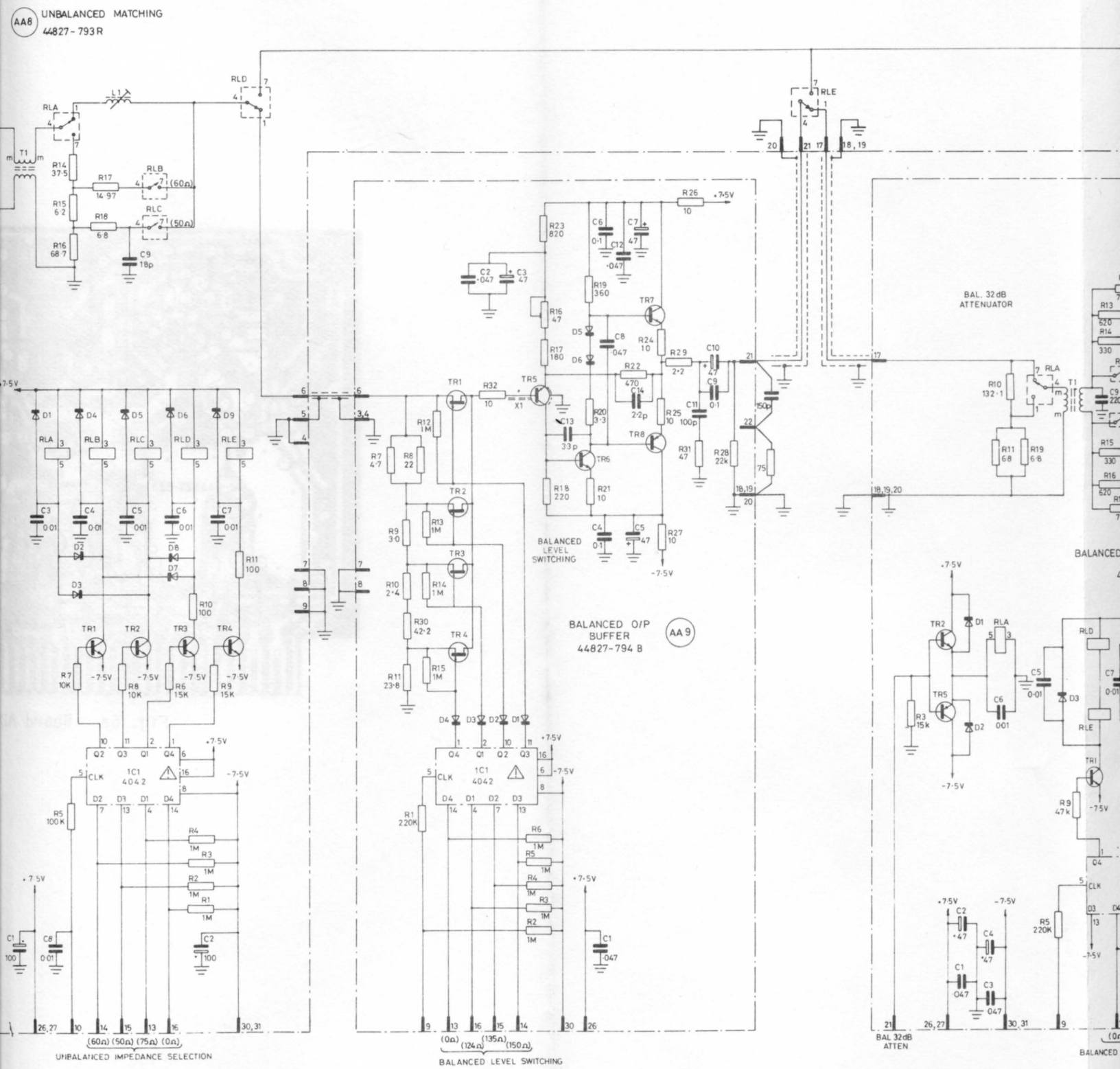


Fig. 5

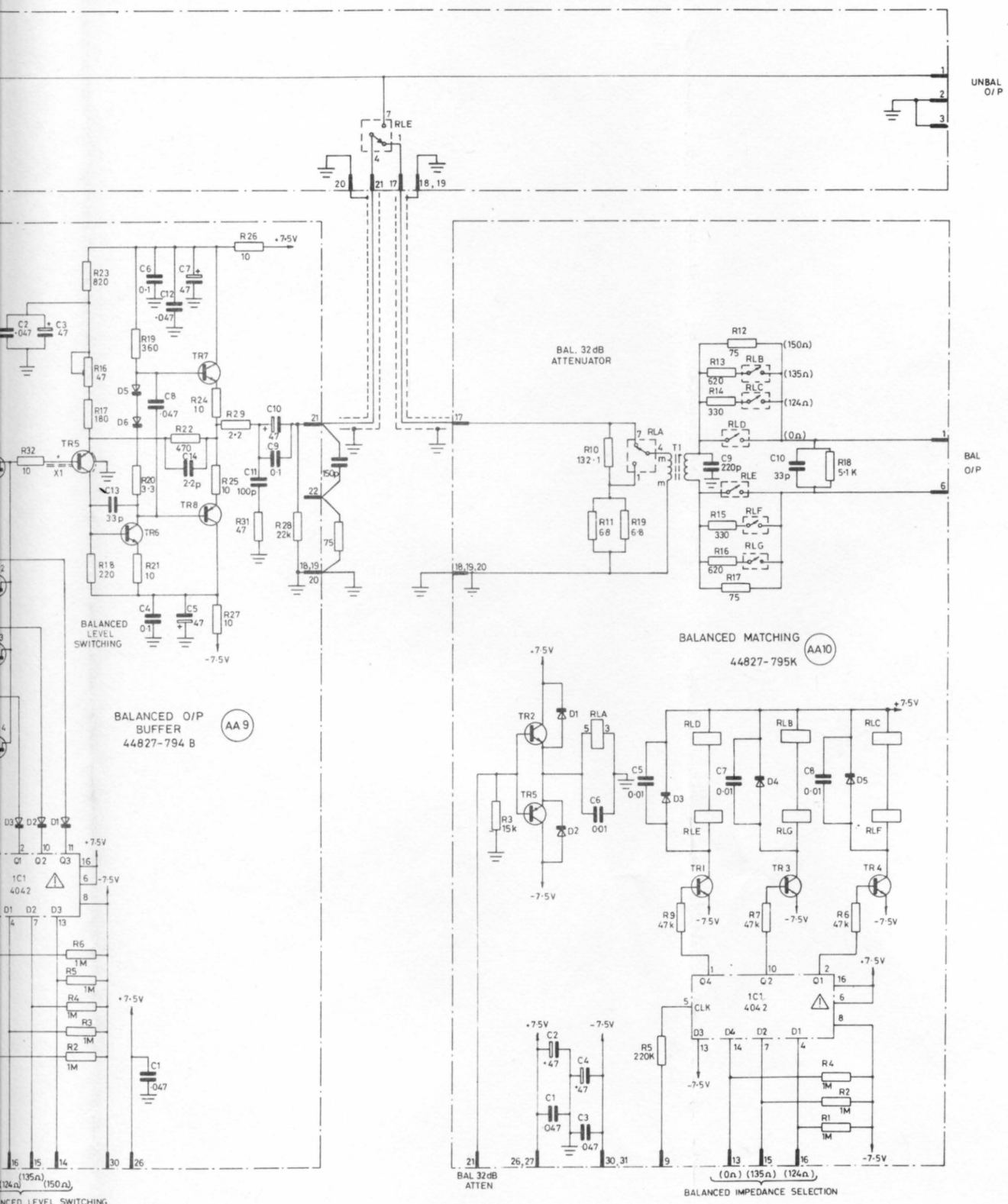
RF unit : Boards

May 80



Drg. No. Z 44990-192B Sht

RF unit : Boards AA8, AA9, AA10



Drg. No. Z 44990-192B Sht. 3 of 3, Iss. 3

unit : Boards AA8, AA9, AA10

Fig. 5

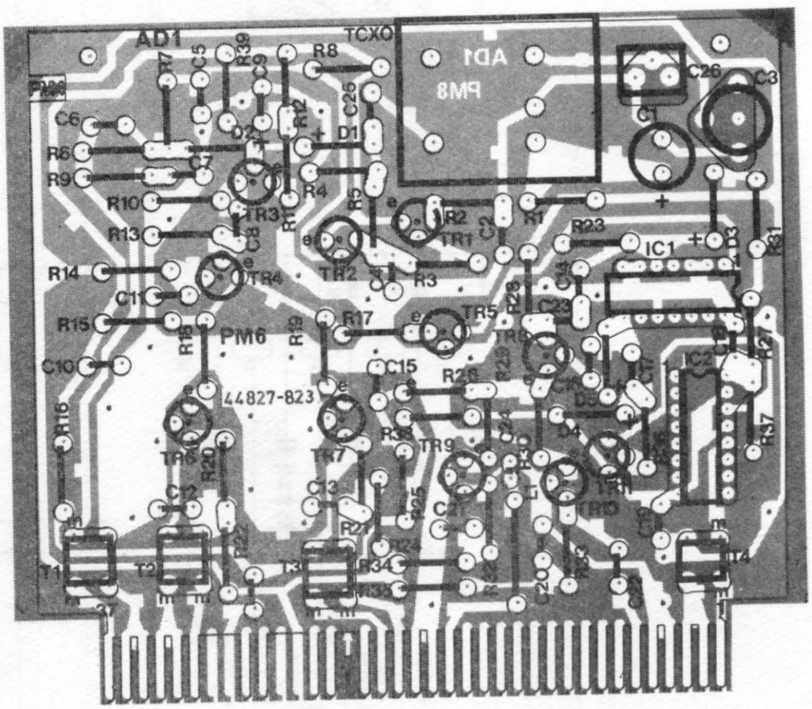


Fig. 6a Board AD1

mponent layout

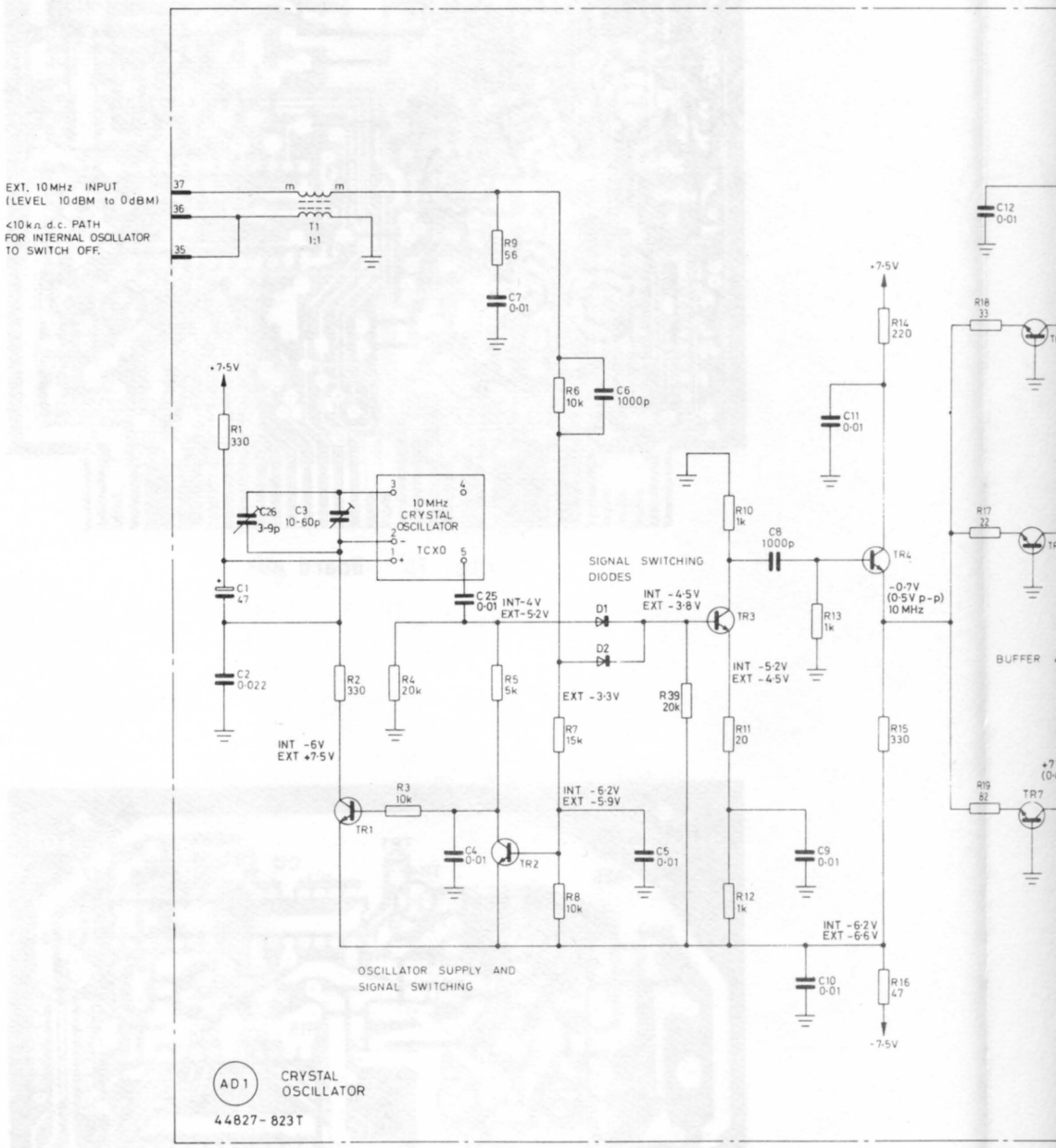
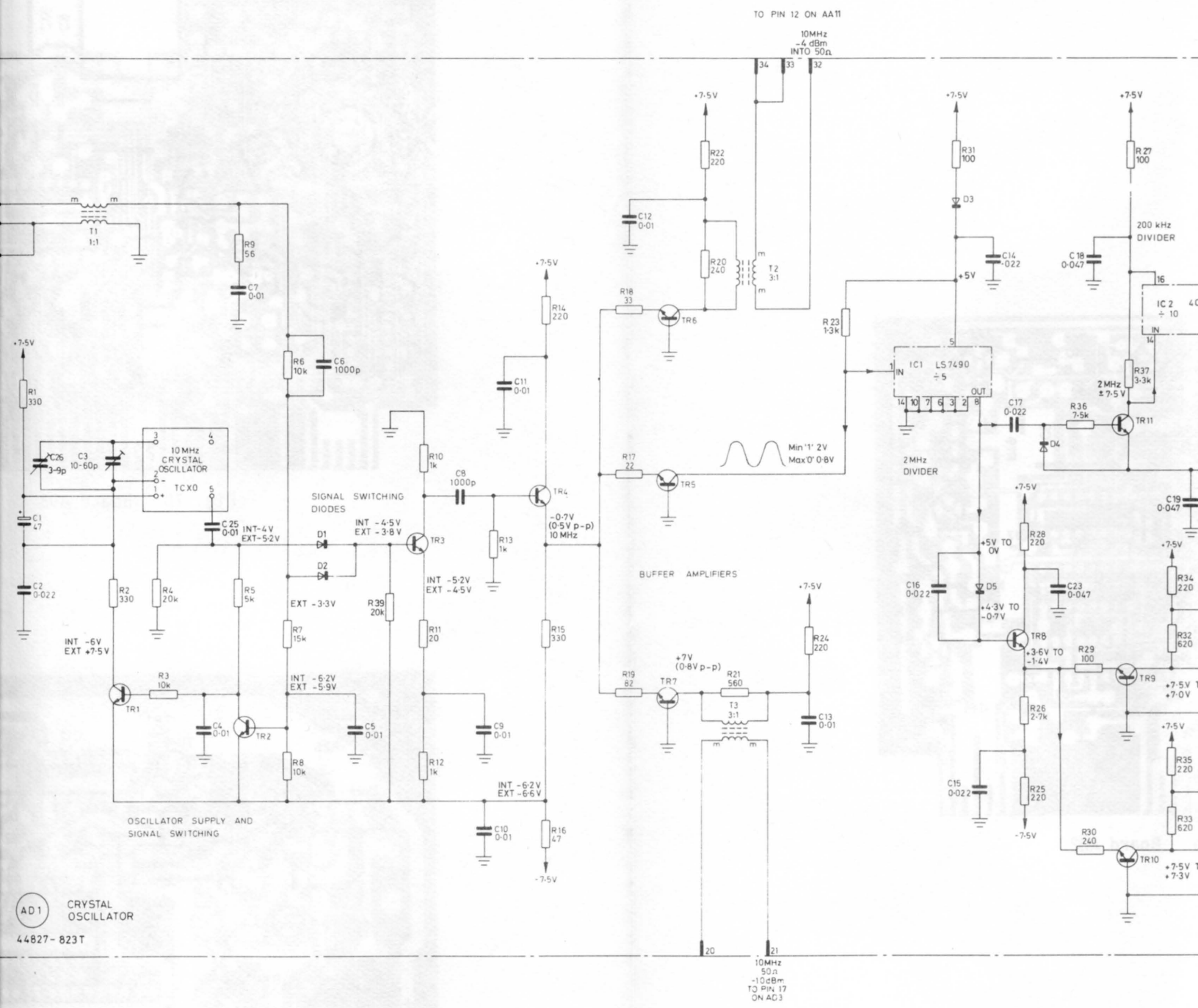


Fig. 6

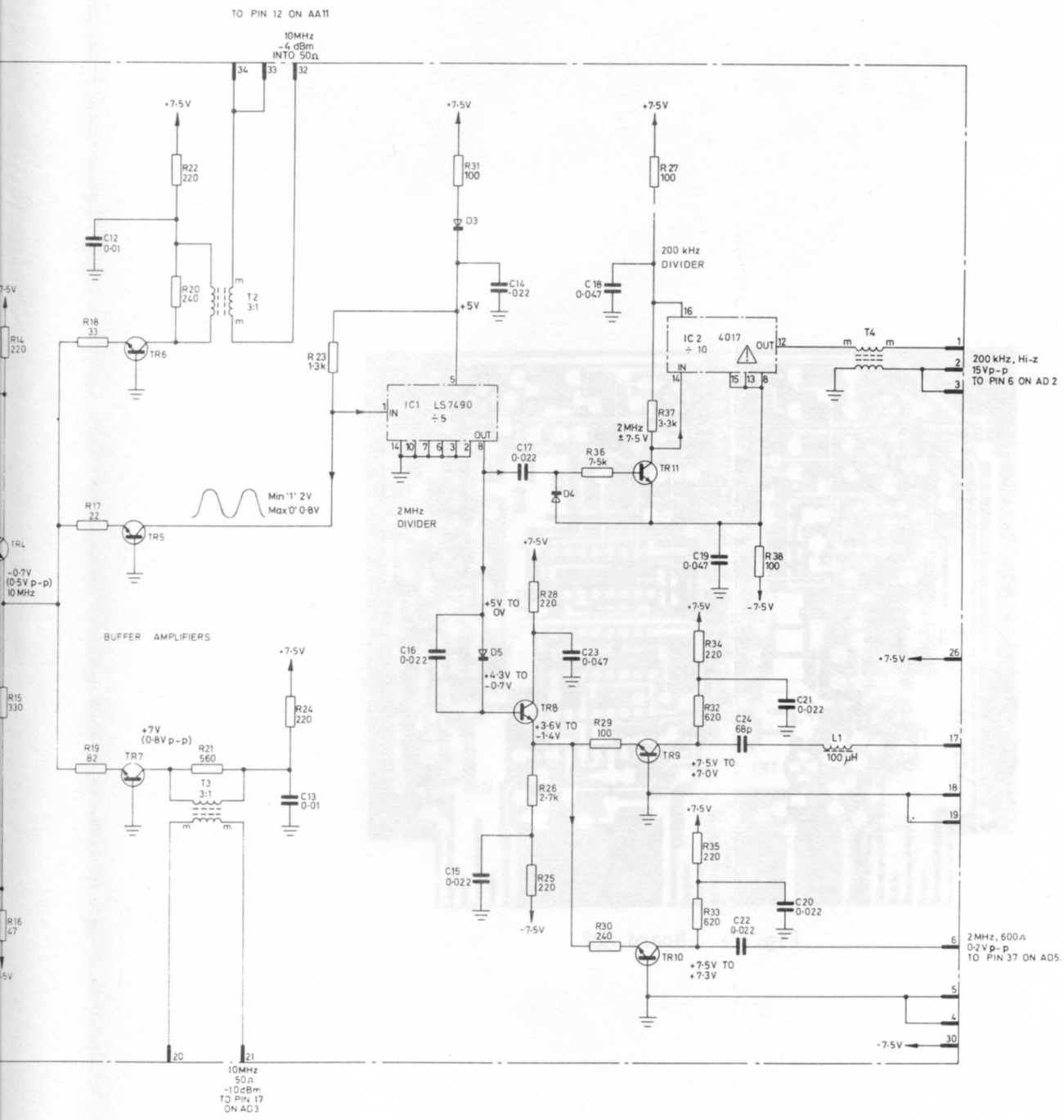
May 80

LO unit :



Drg. No. Z 44990-184

LO unit : Board AD1



Drg. No. Z 44990-184P Sht. 1 of 5, Iss. 2

LO unit : Board AD1

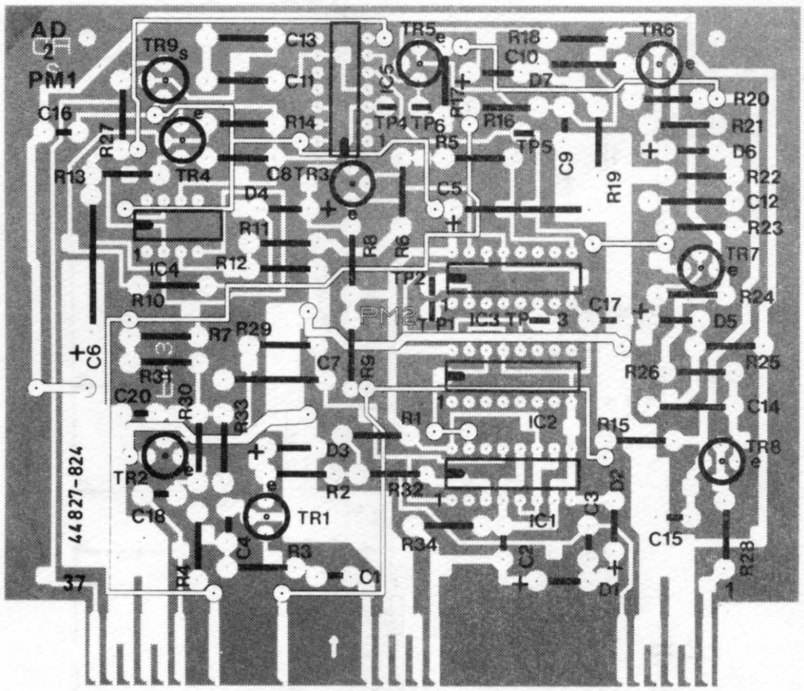


Fig. 7a Board AD2

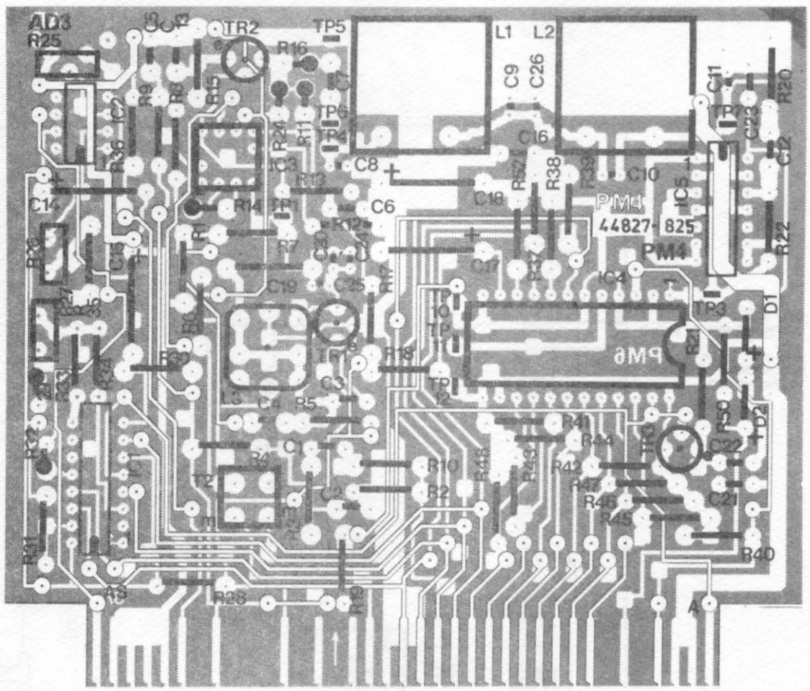


Fig. 7b Board AD3

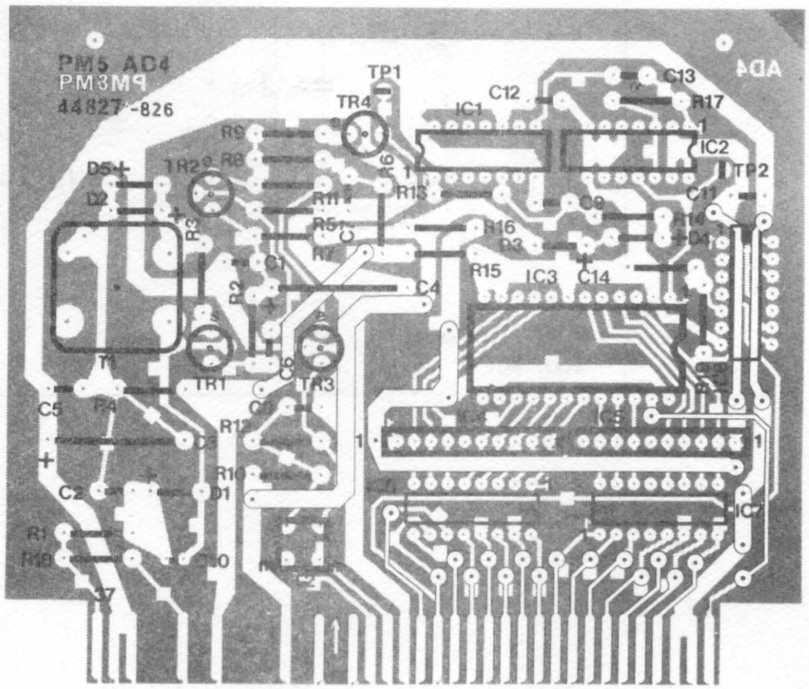


Fig. 7c Board AD4

onent layouts

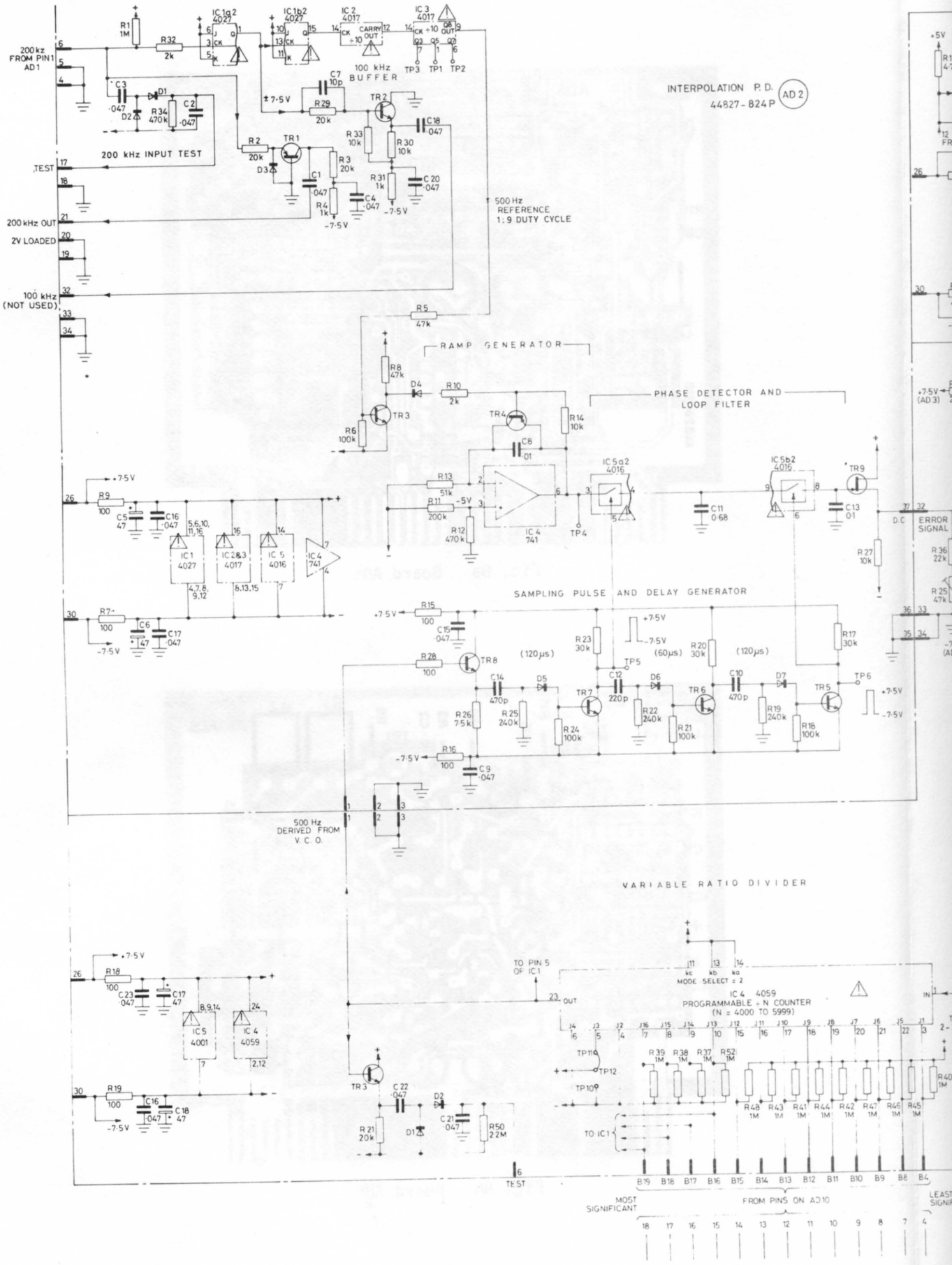
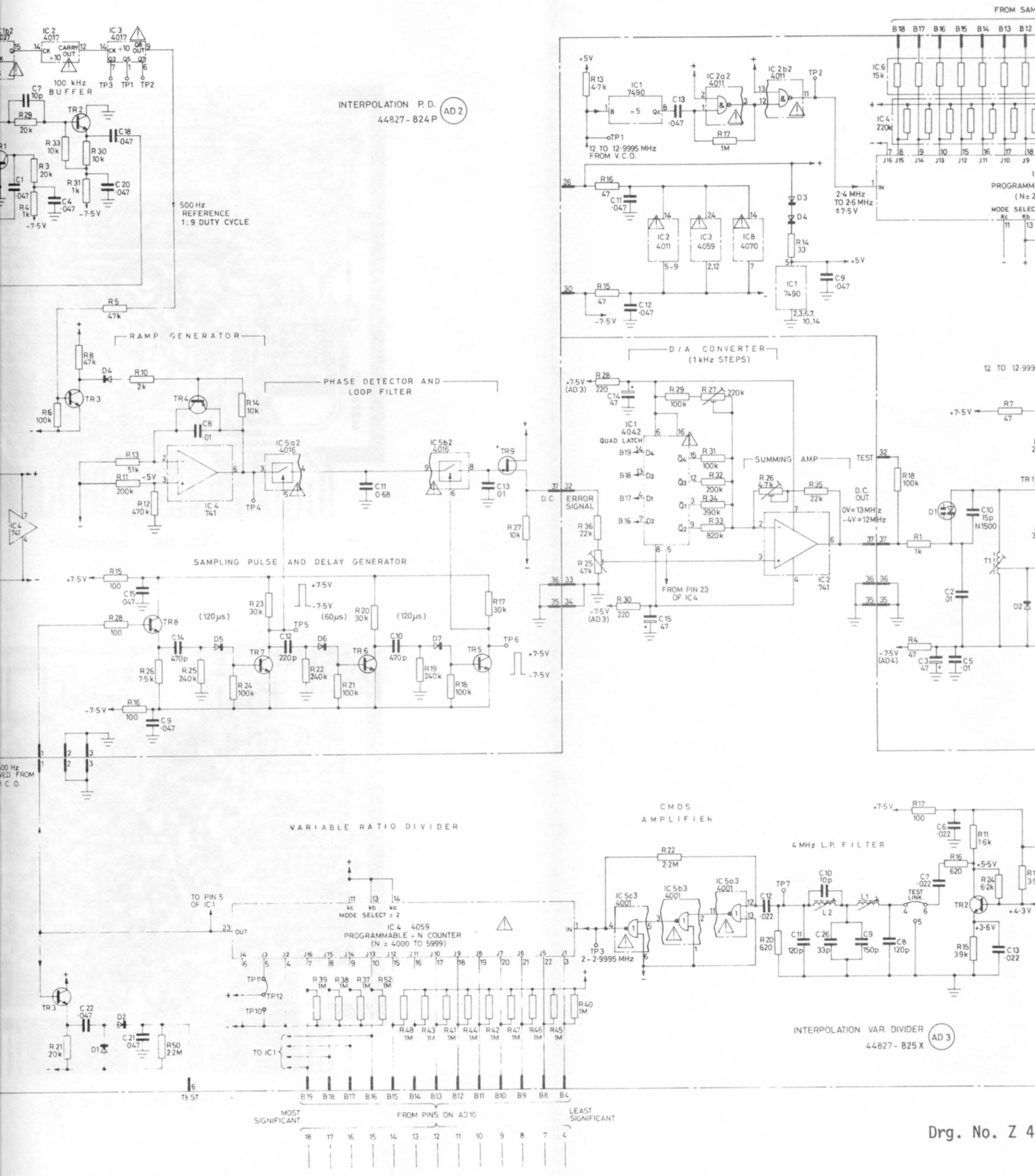


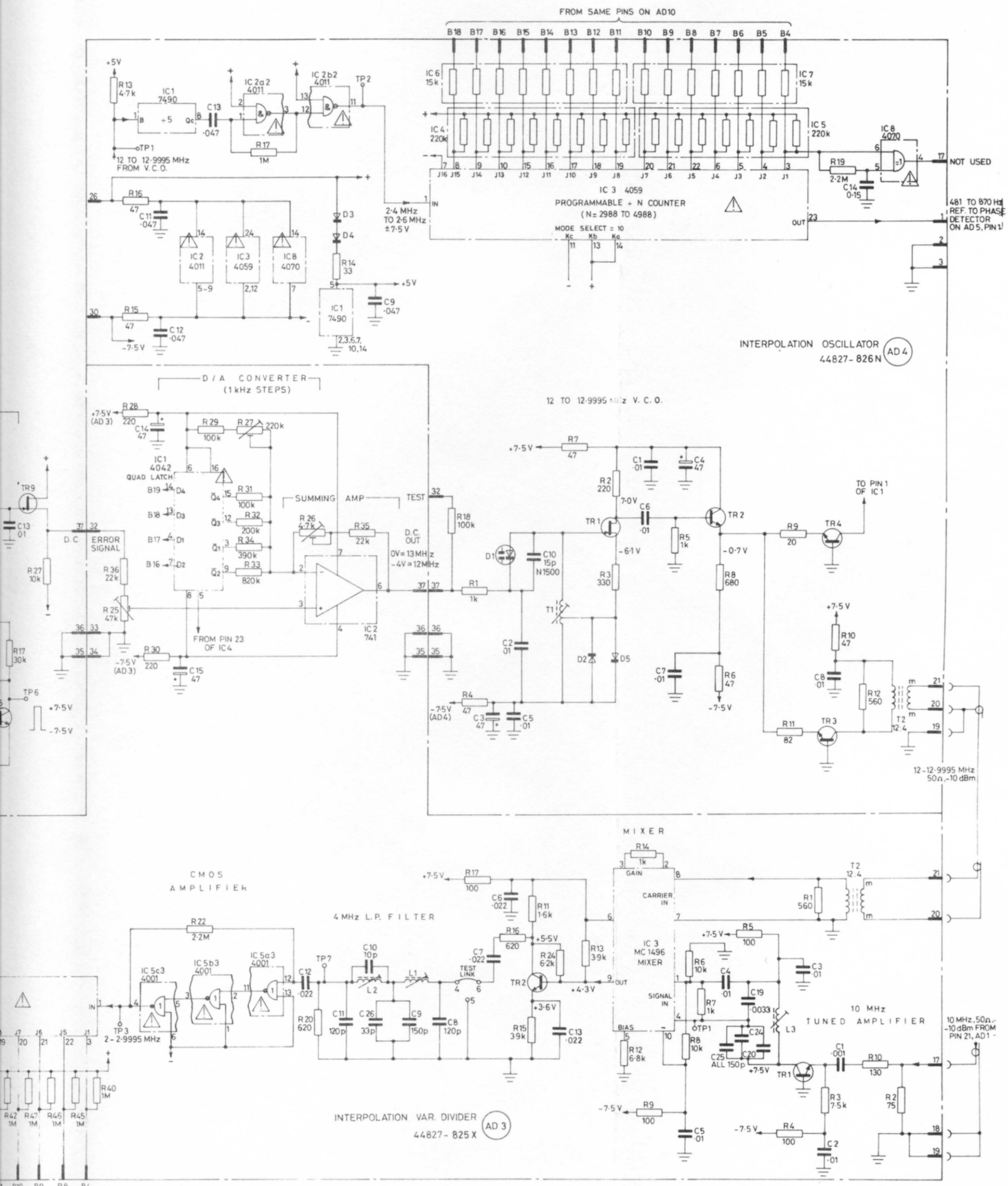
Fig. 7

LO unit : Boards AD

May 80



LO unit : Boards AD2, AD3, AD4



Drg. No. Z 44990-184P Sht. 2 of 5, Iss. 1

t : Boards AD2, AD3, AD4

Fig. 7

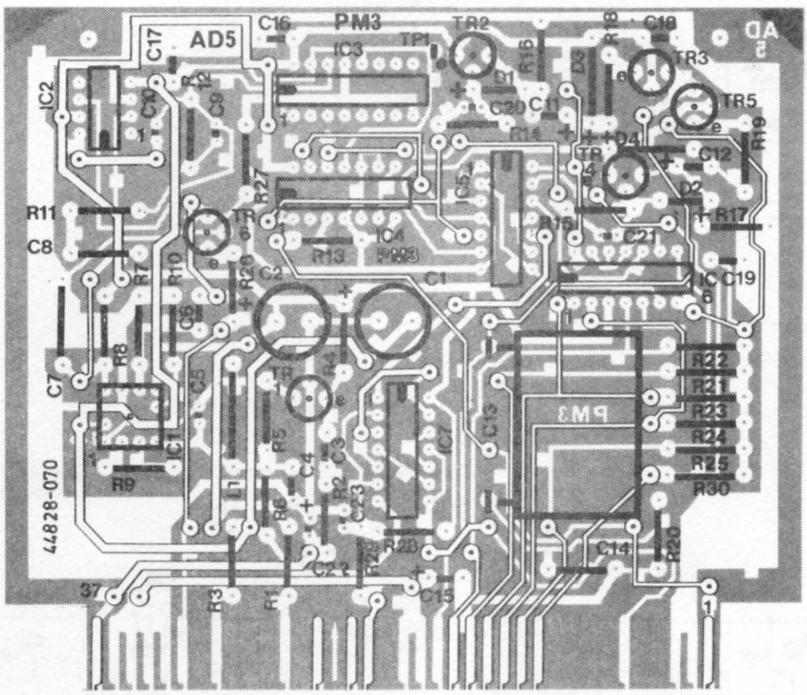


Fig. 8a Board AD5

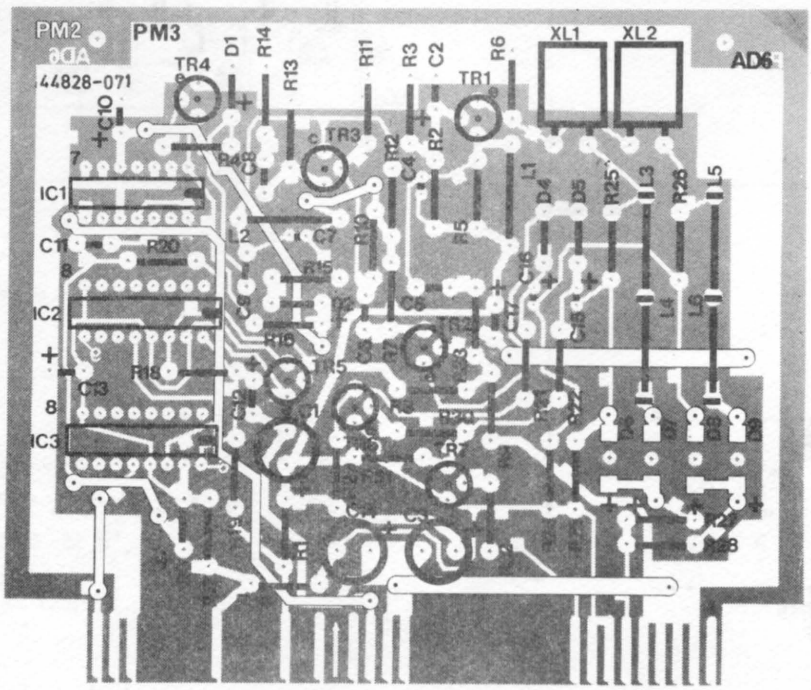


Fig. 8b Board AD6

ment layouts

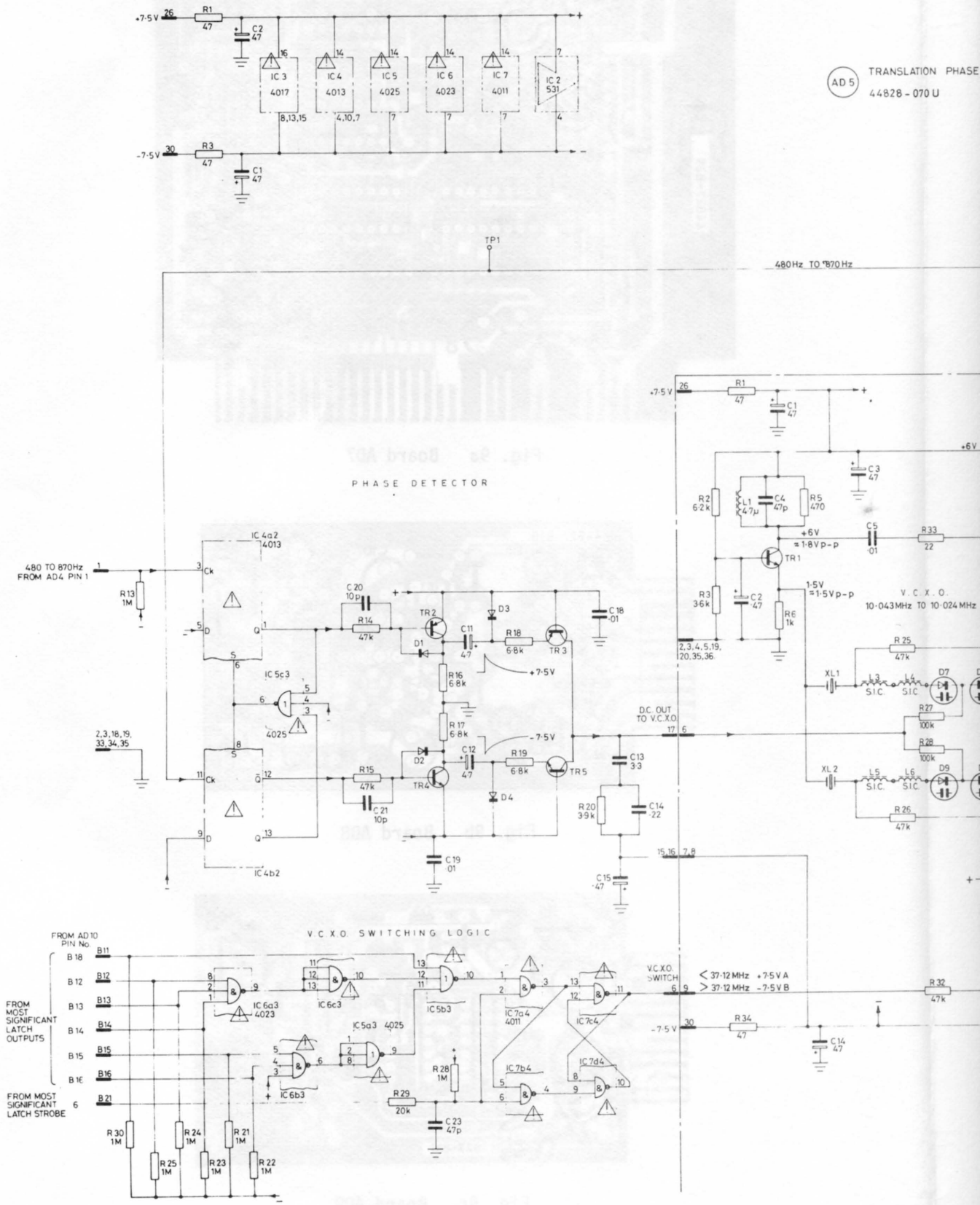
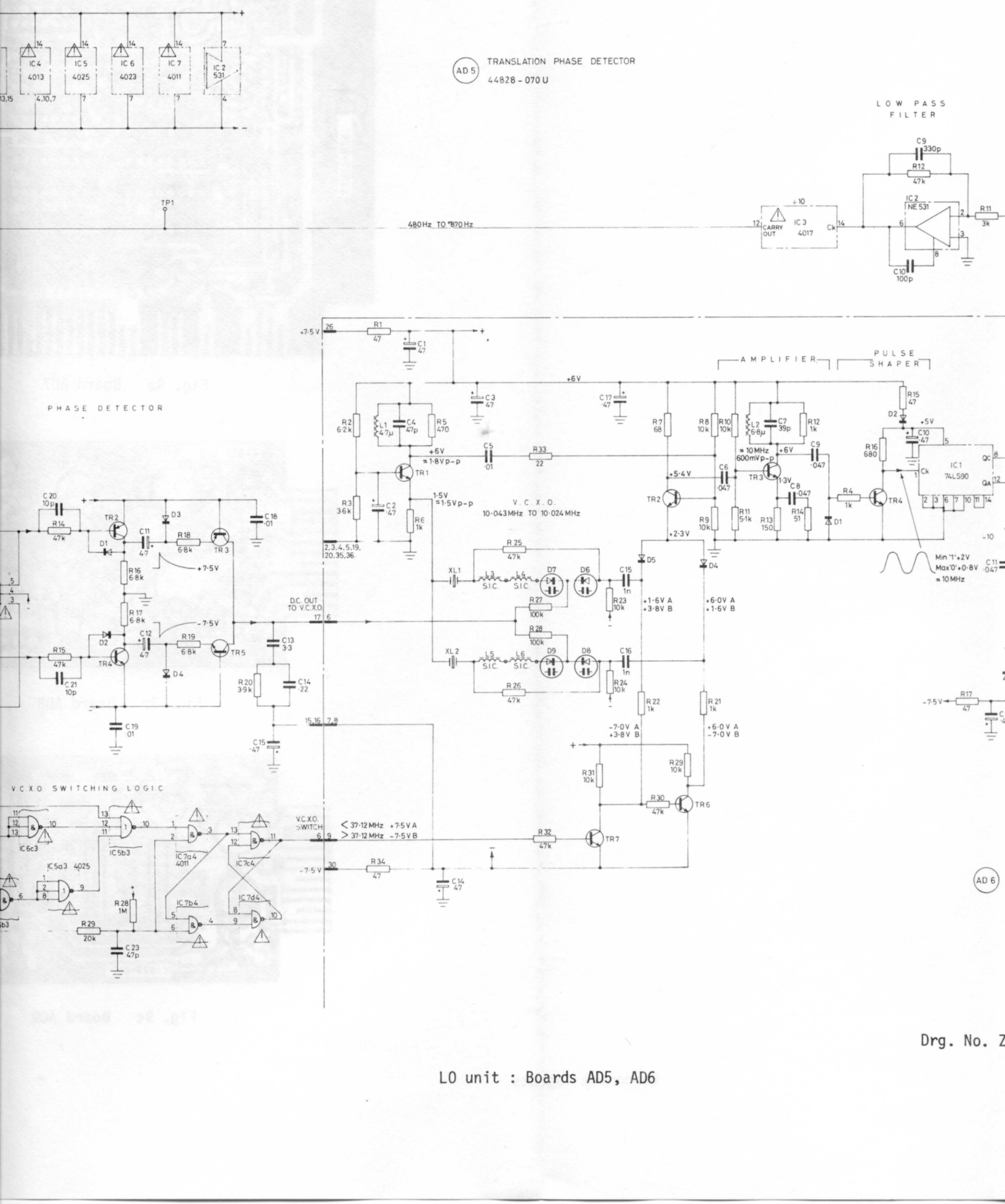


Fig. 8

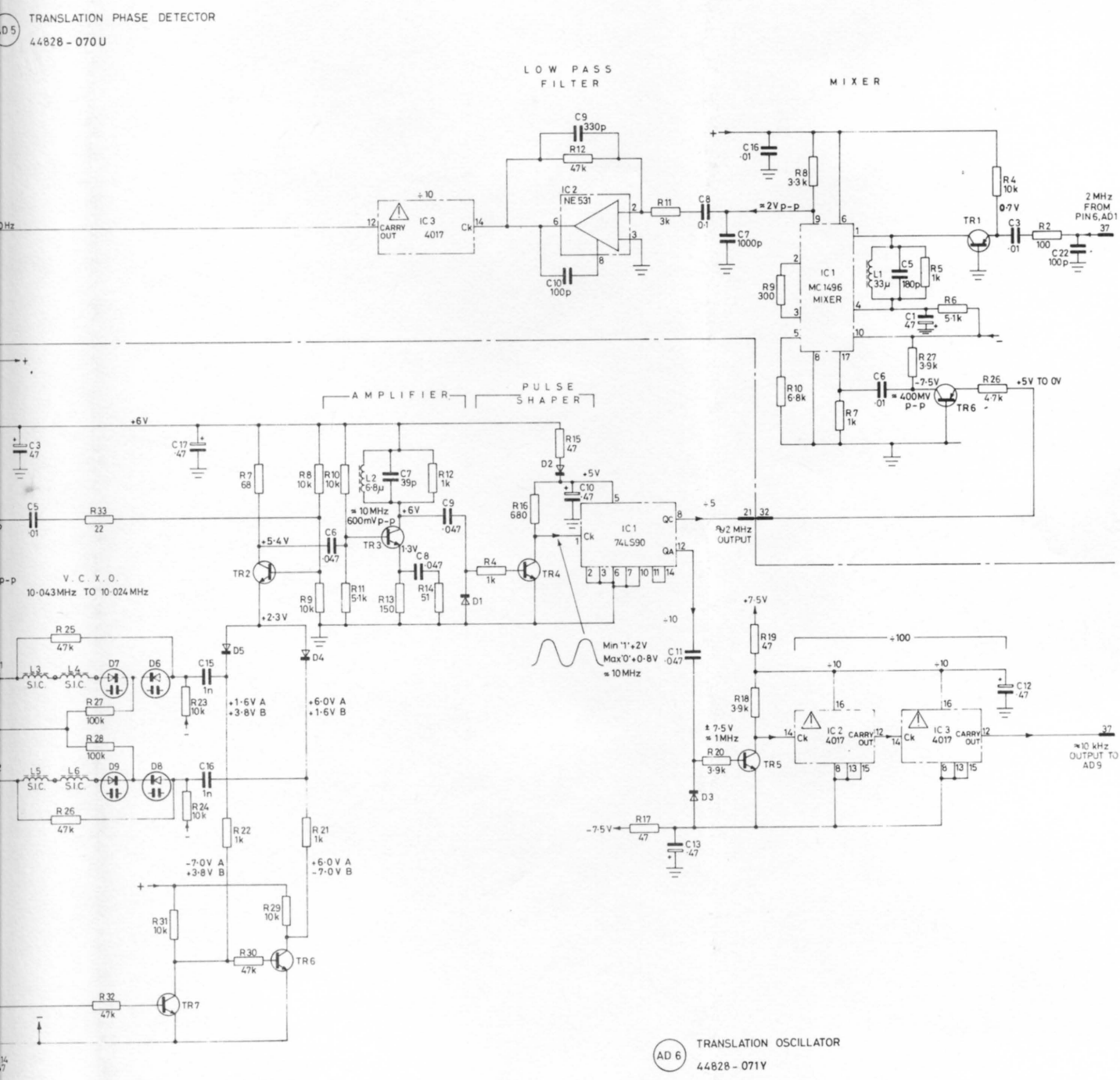
LO unit : Boards

May 80



Drg. No. Z

LO unit : Boards AD5, AD6



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unit : Boards AD5, AD6

Fig. 8

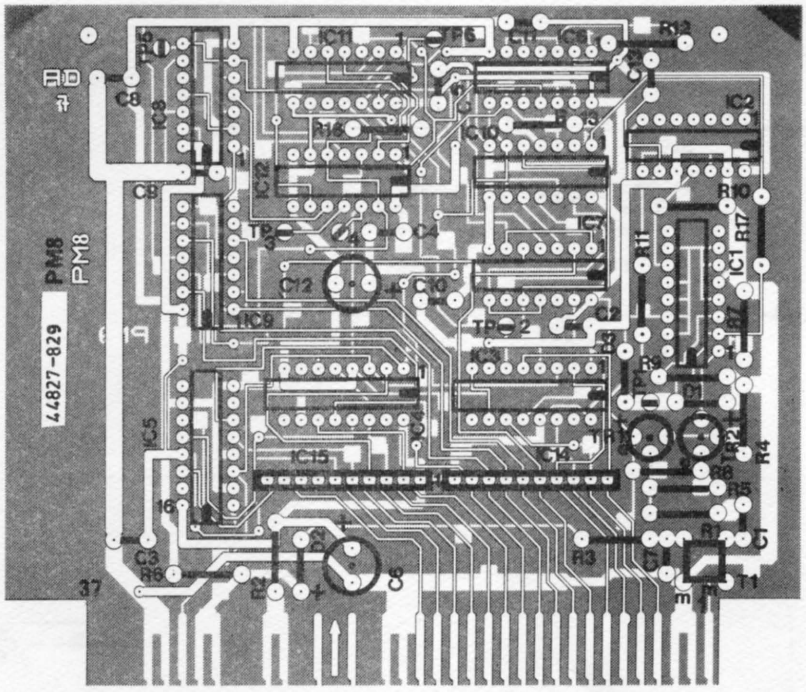


Fig. 9a Board AD7

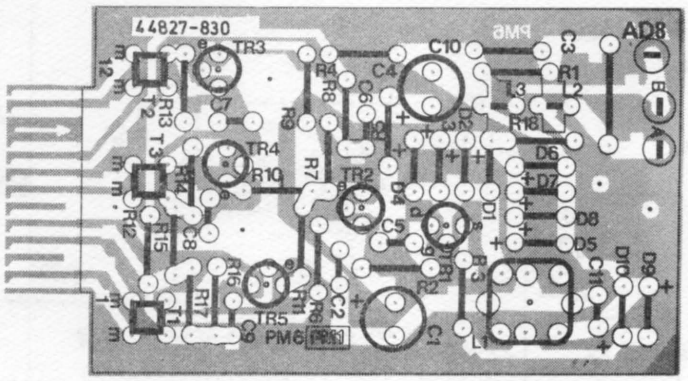


Fig. 9b Board AD8

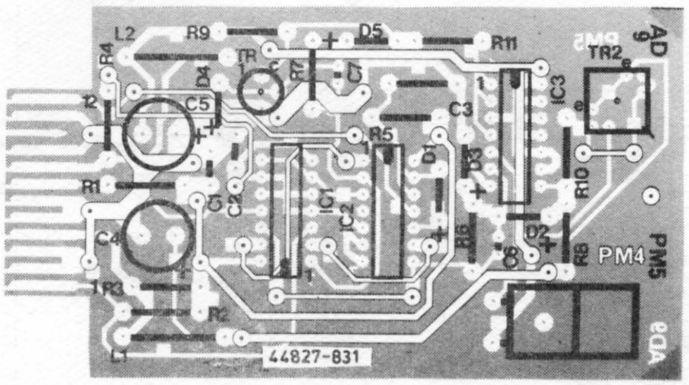
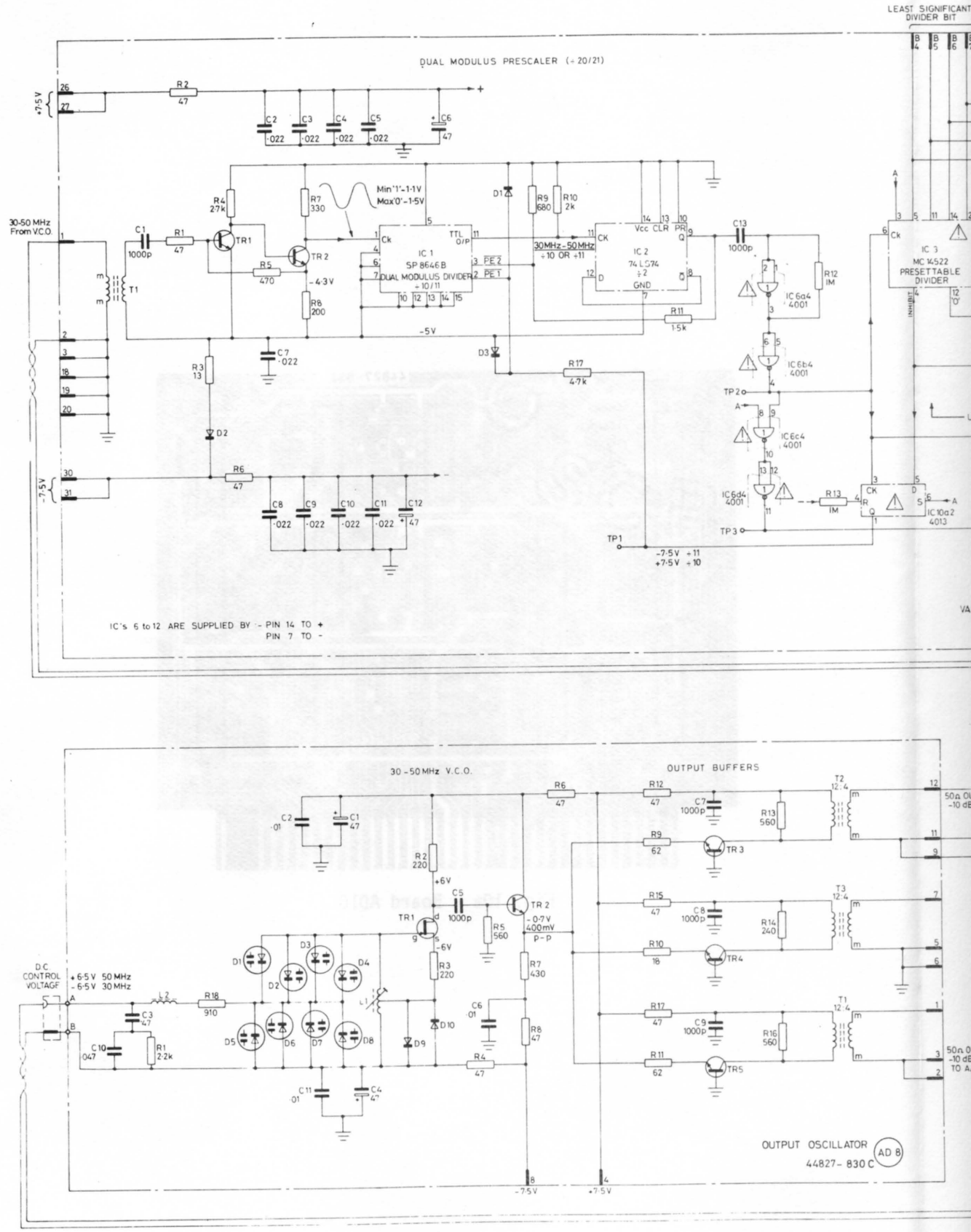


Fig. 9c Board AD9

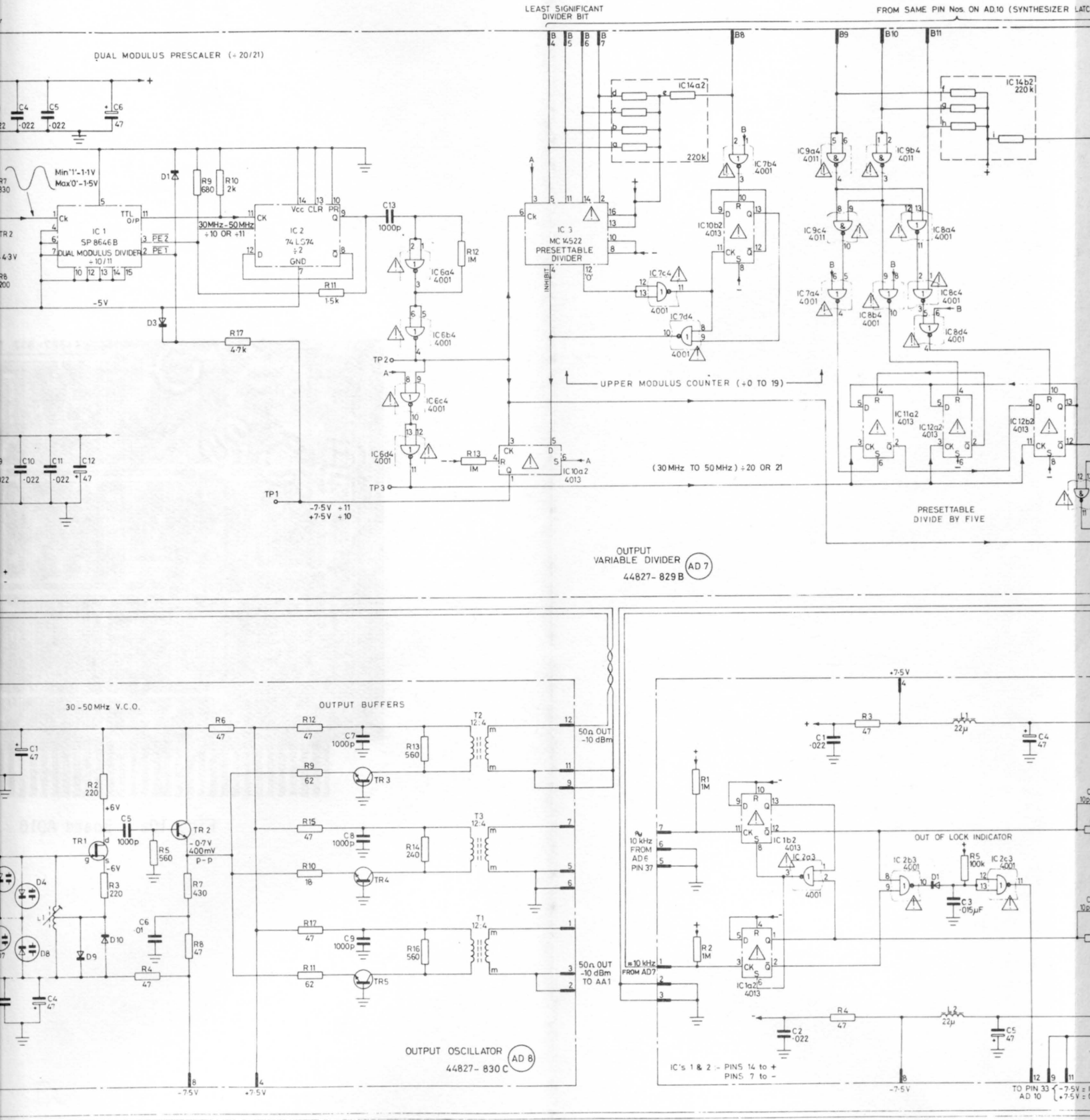
ment layouts



LO unit : Boards

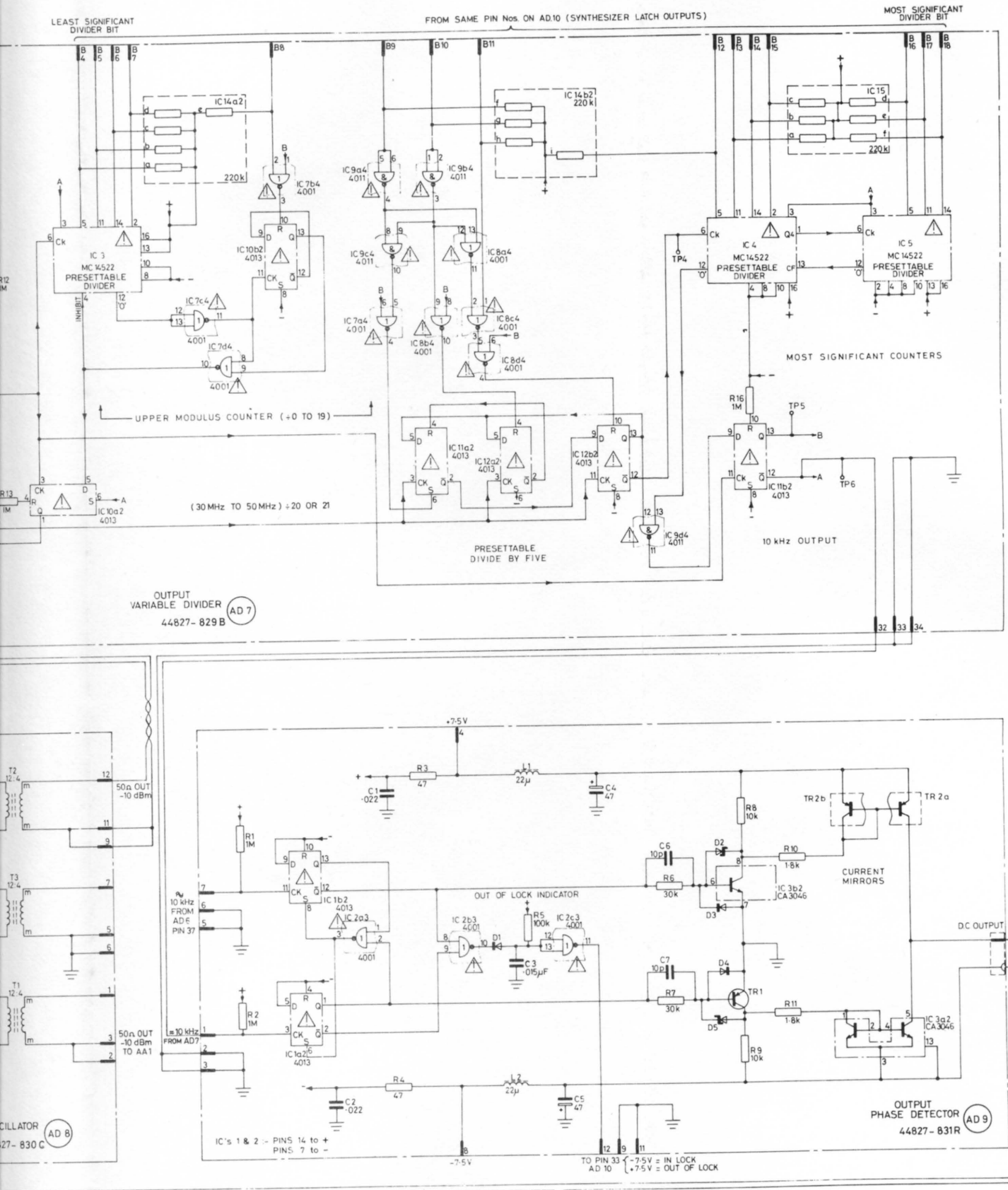
Fig. 9

May 80



Drg. No. Z

LO unit : Boards AD7, AD8, AD9



Drg. No. Z 44990-184P Sht. 4 of 5, Iss. 2

0 unit : Boards AD7, AD8, AD9

Fig. 9

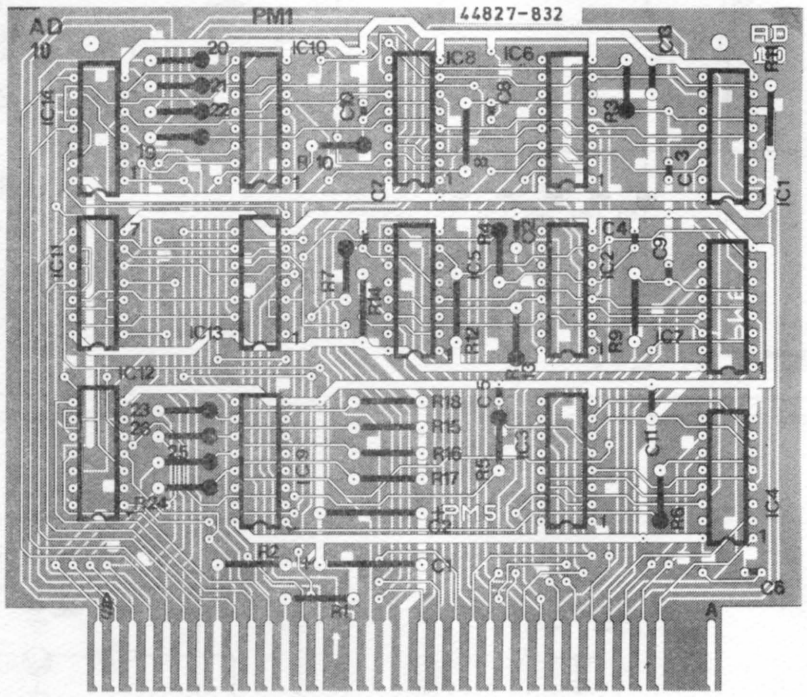


Fig. 10a Board AD10

omponent layout

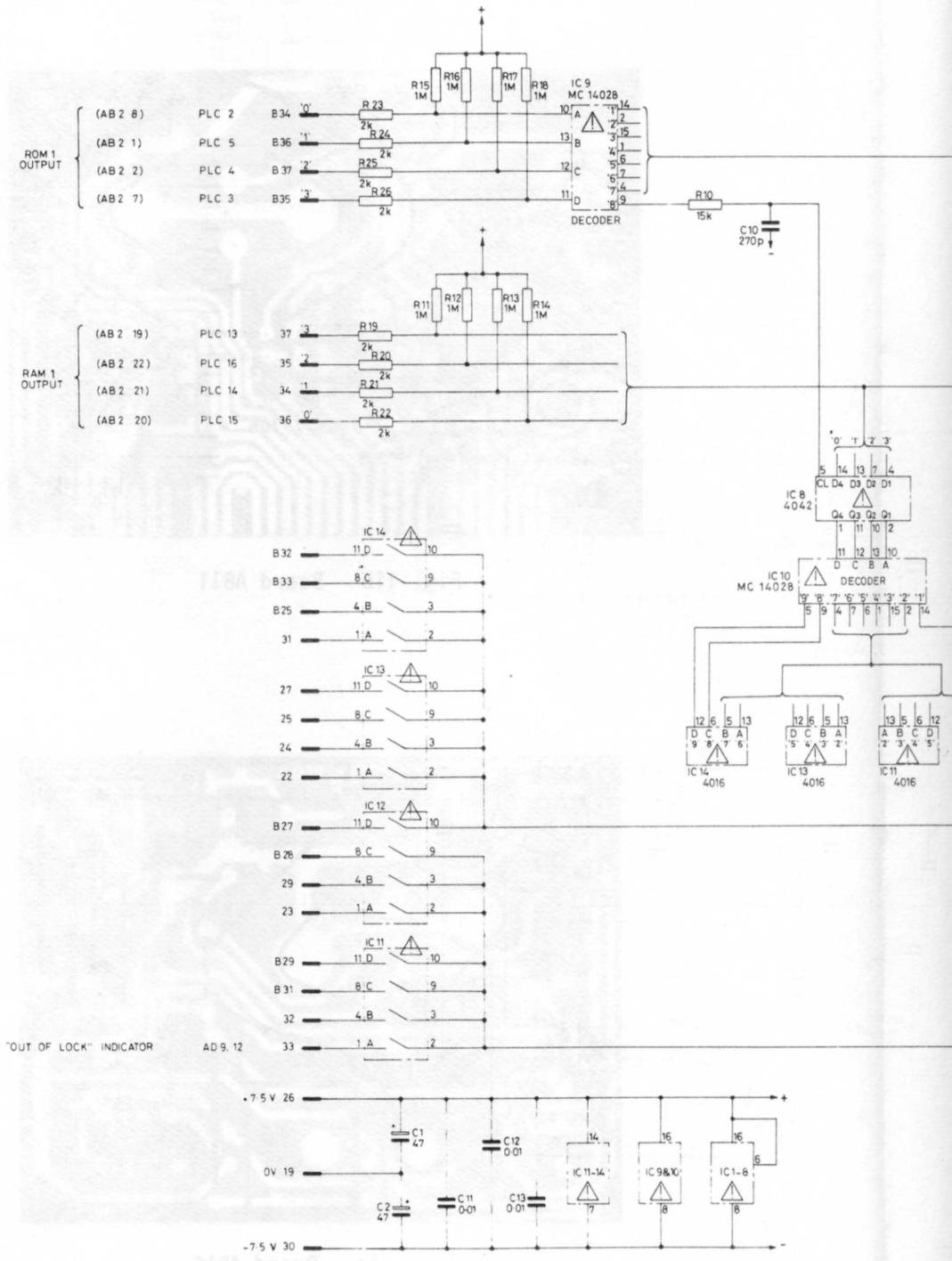
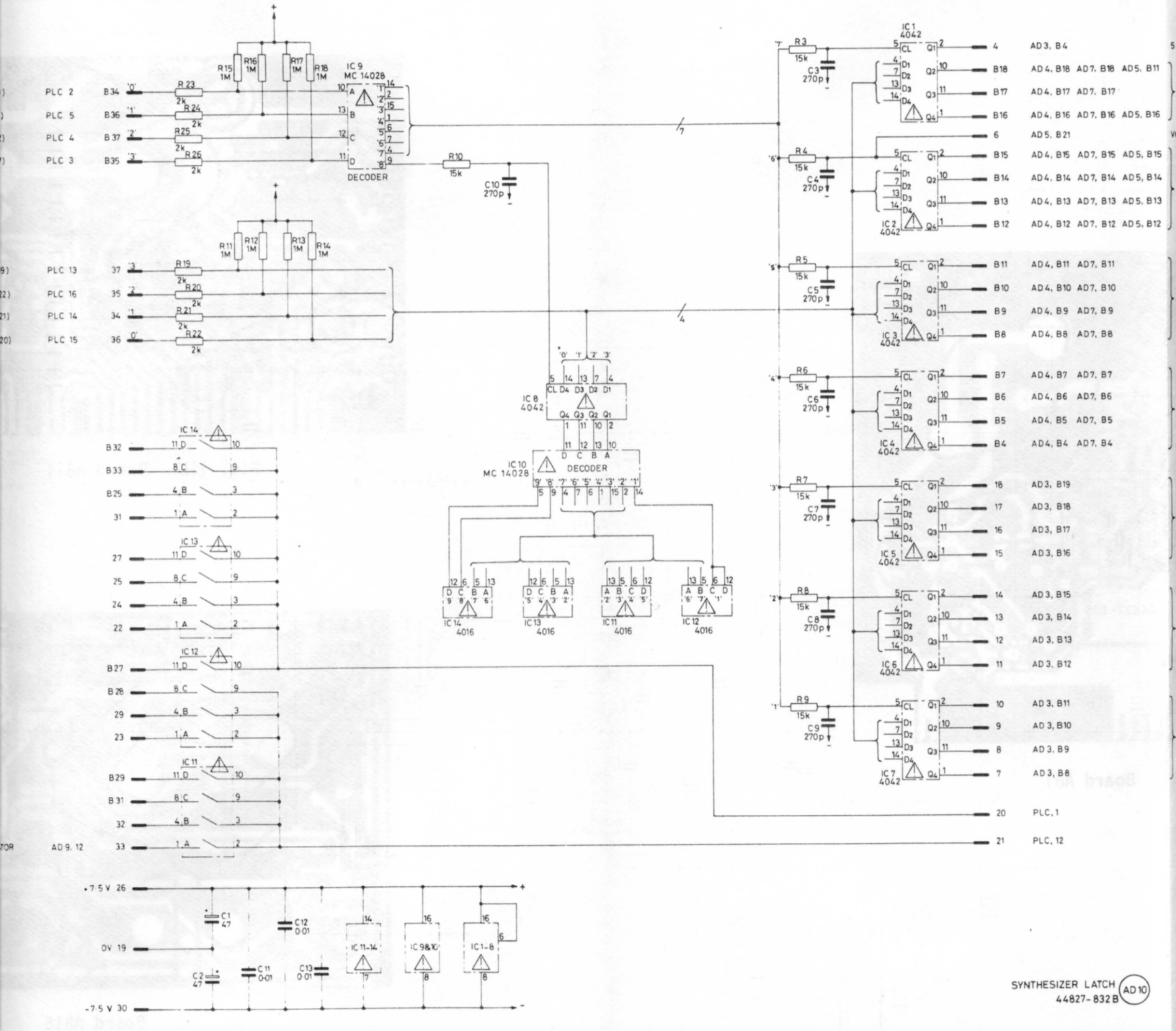


Fig. 10

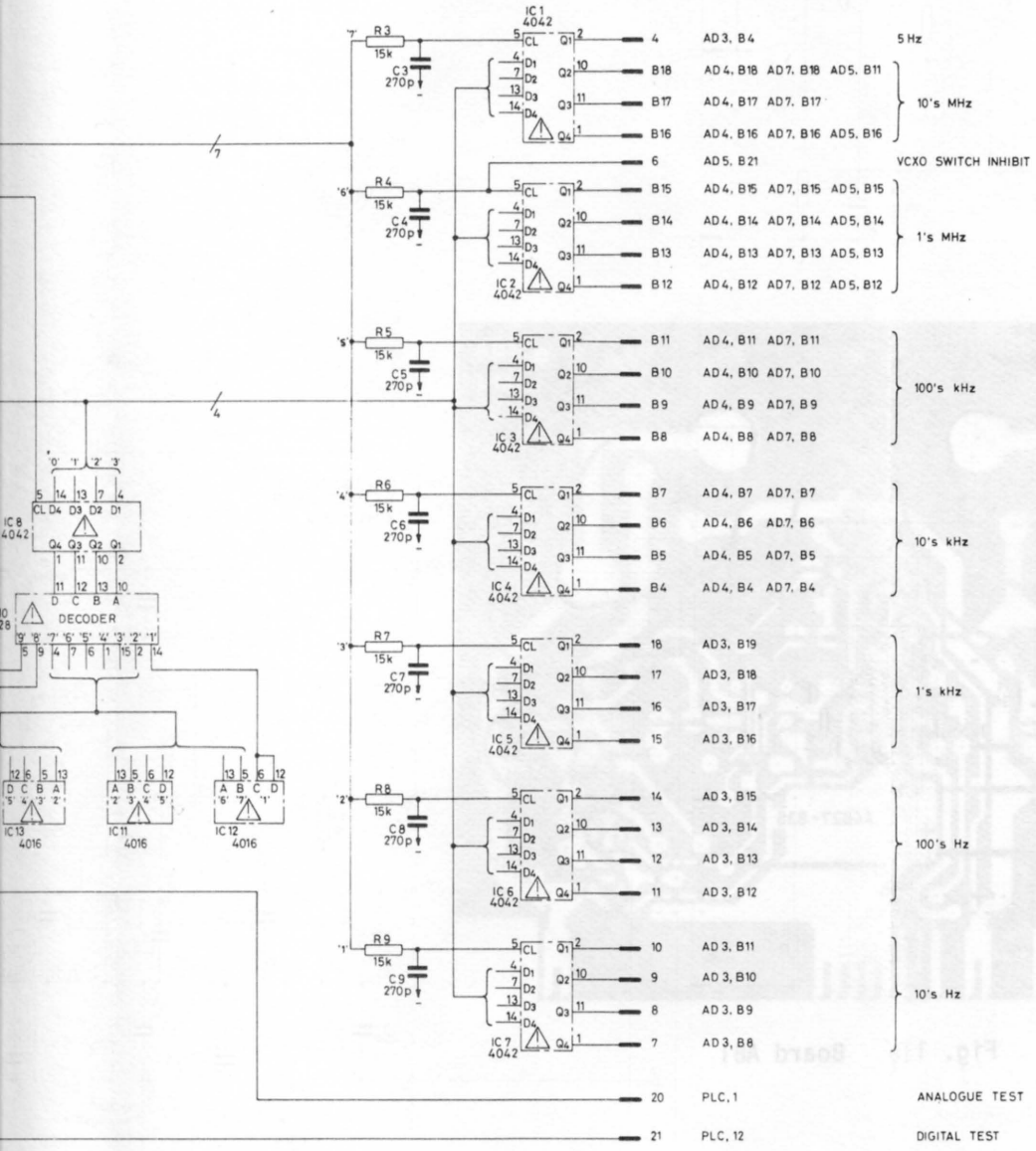
LO unit :

May 80



Drg. No. Z 44990-184P Sht. 5 of 5

LO unit : Board AD10



Drg. No. Z 44990-184P Sht. 5 of 5, Iss. 1

LO unit : Board AD10

Fig. 10

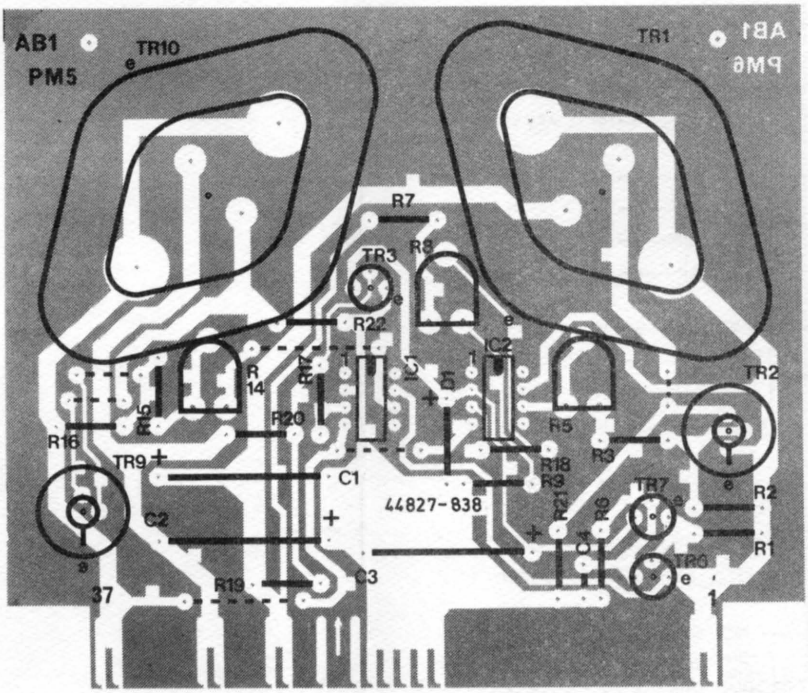


Fig. 11a Board AB1

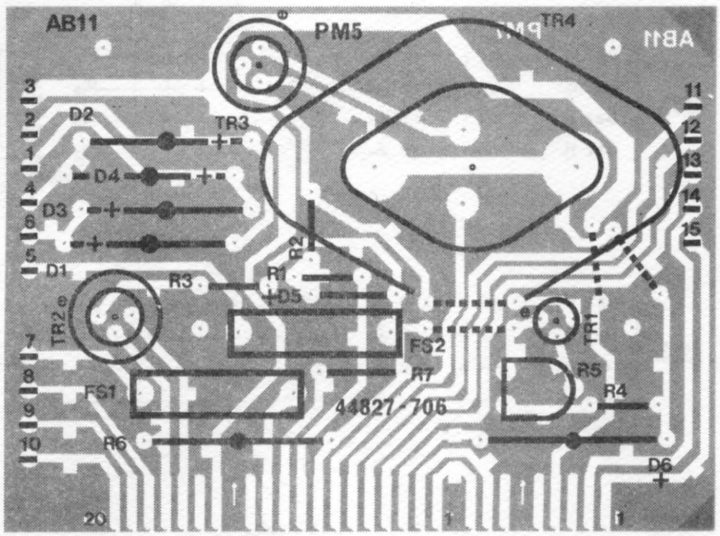


Fig. 11b Board AB11

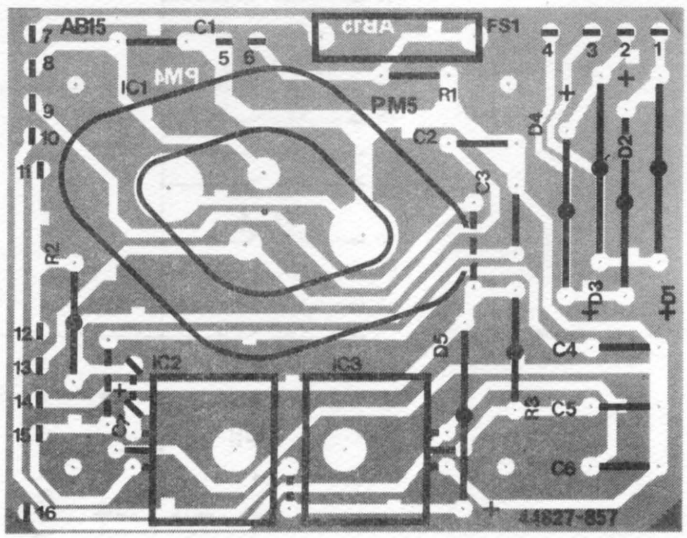


Fig. 11c Board AB15

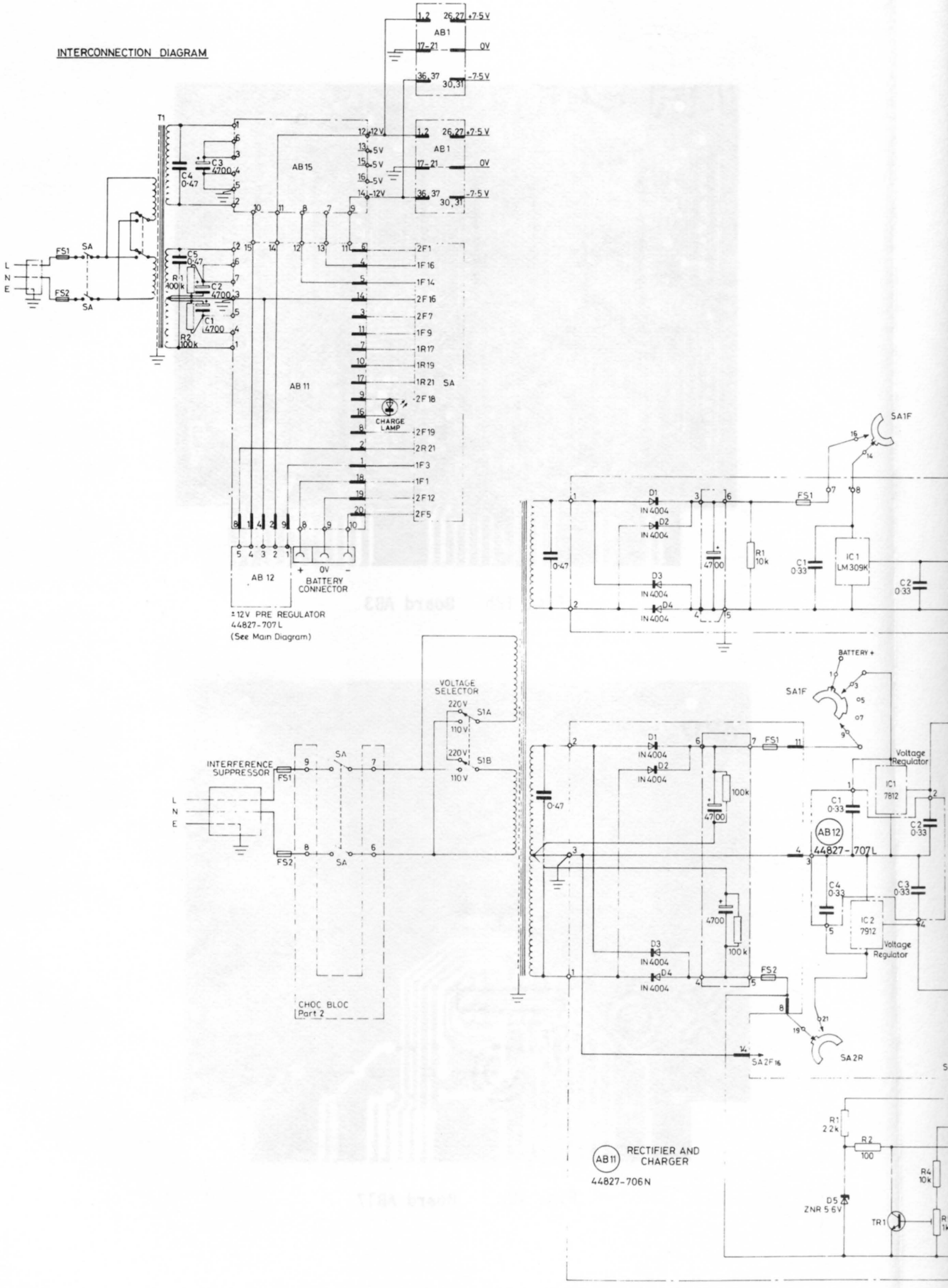
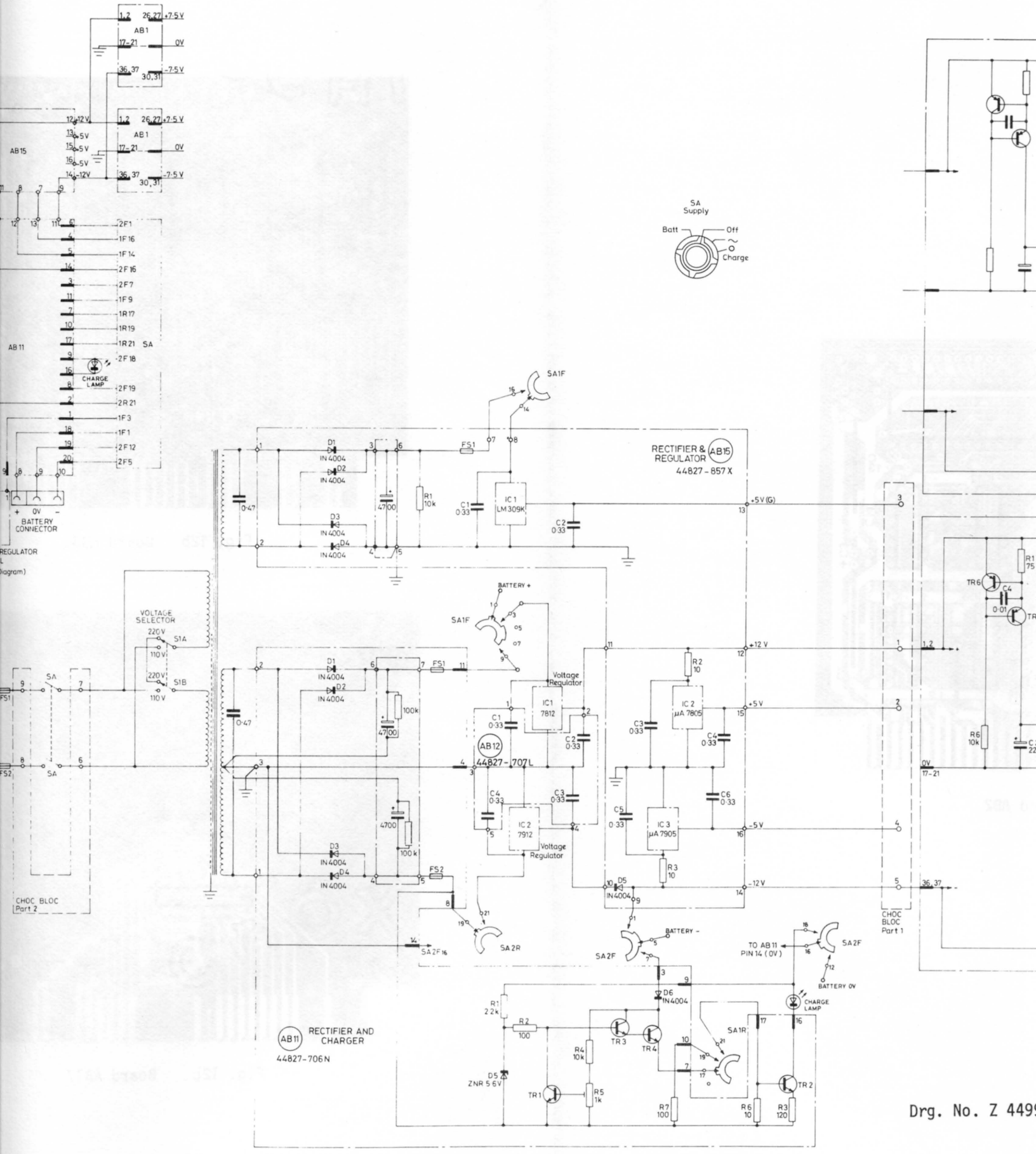


Fig. 11

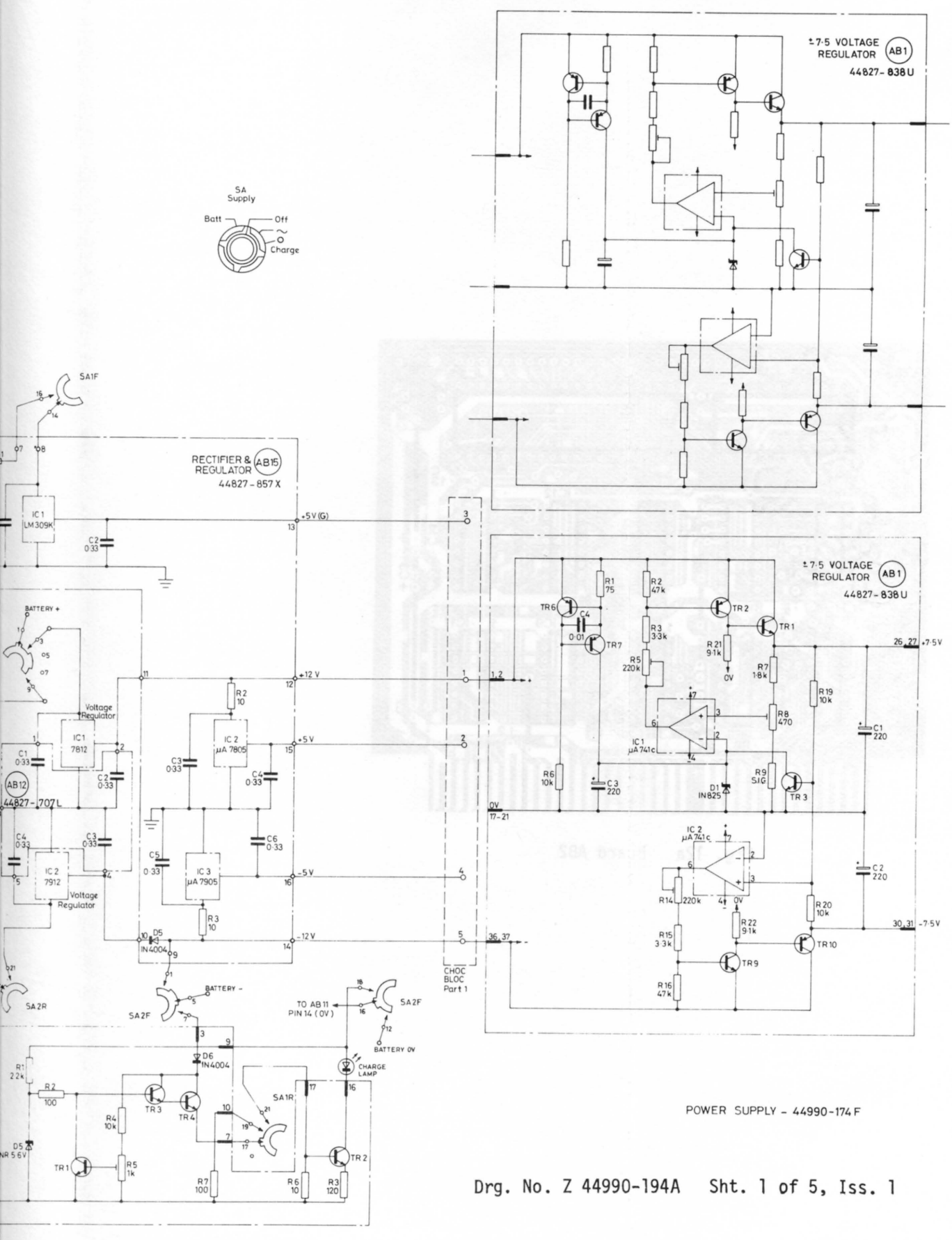
Power supply : Boards AB1,

May 80



Drg. No. Z 449

Power supply : Boards AB1, AB11, AB12, AB15



POWER SUPPLY - 44990-174F

Drg. No. Z 44990-194A Sht. 1 of 5, Iss. 1

: Boards AB1, AB11, AB12, AB15

Fig. 11

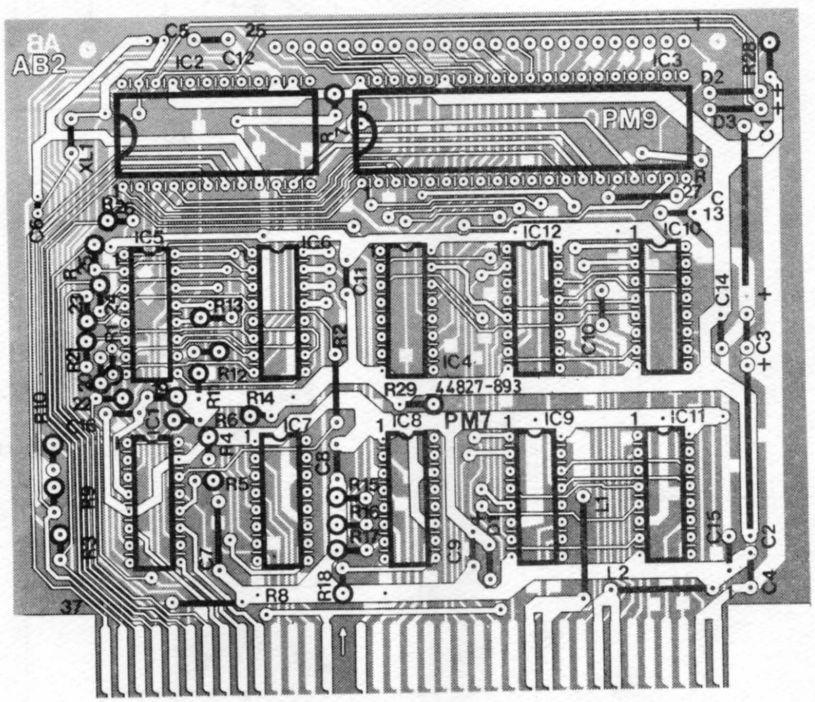
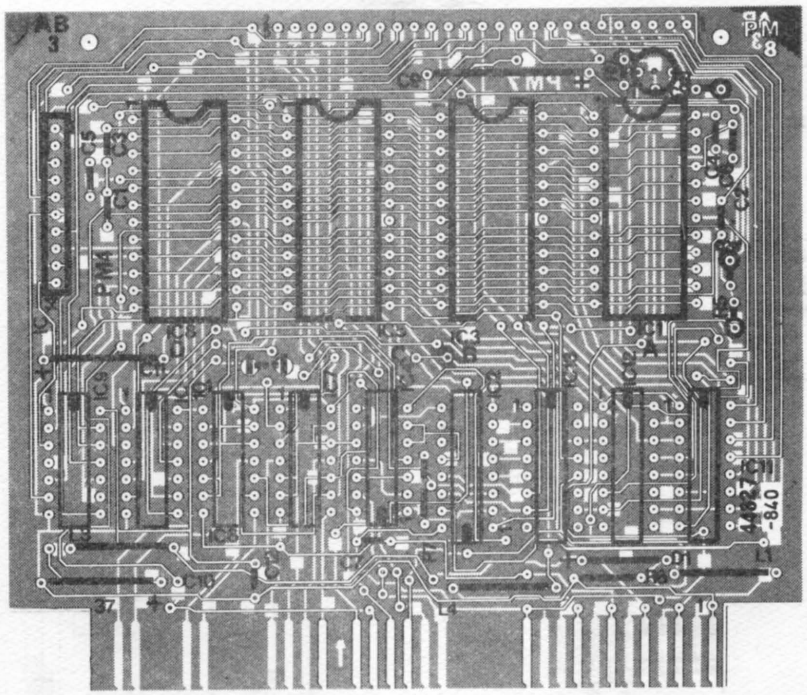


Fig. 12a Board AB2



Fig, 12b Board AB3

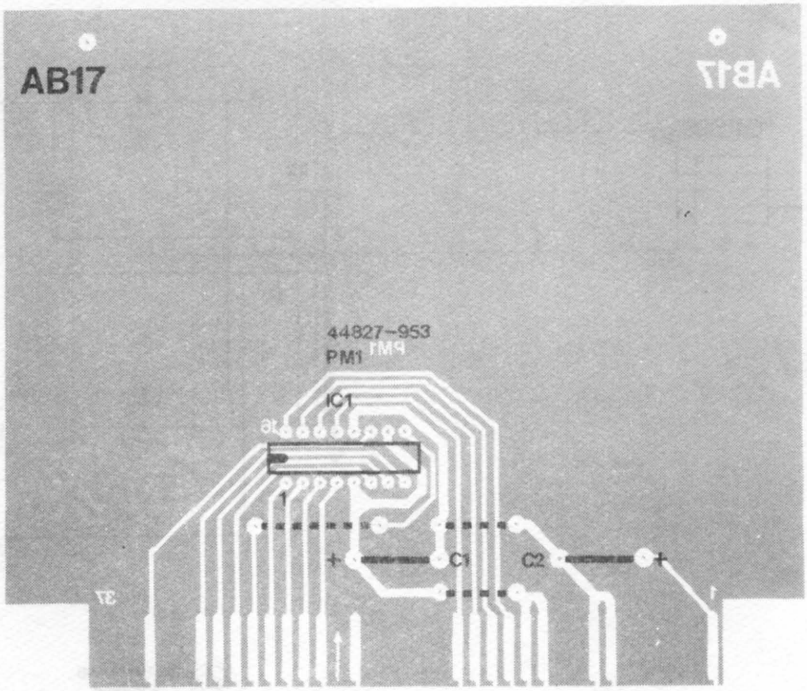


Fig. 12c Board AB17

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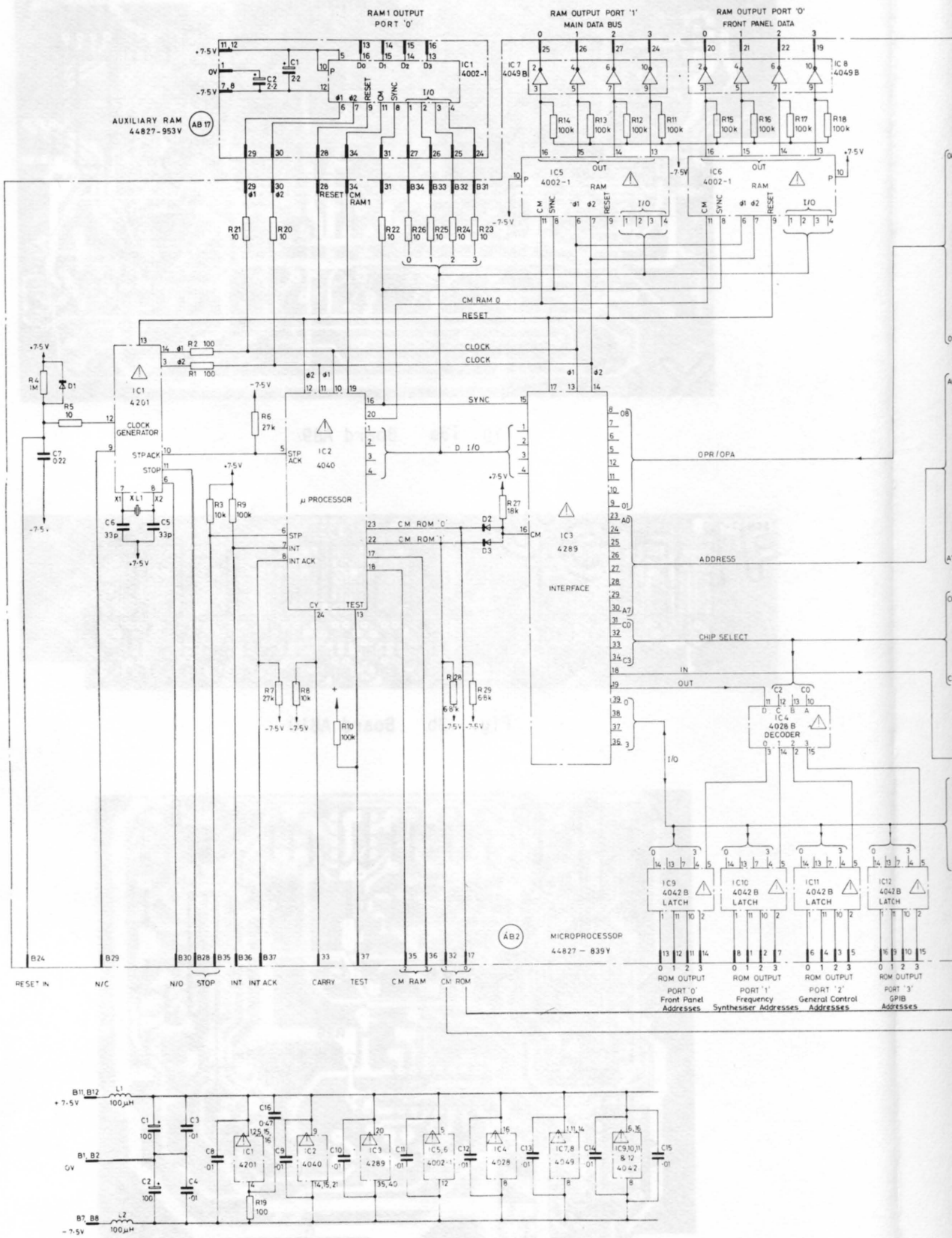

Fig. 12

Control unit : Boards

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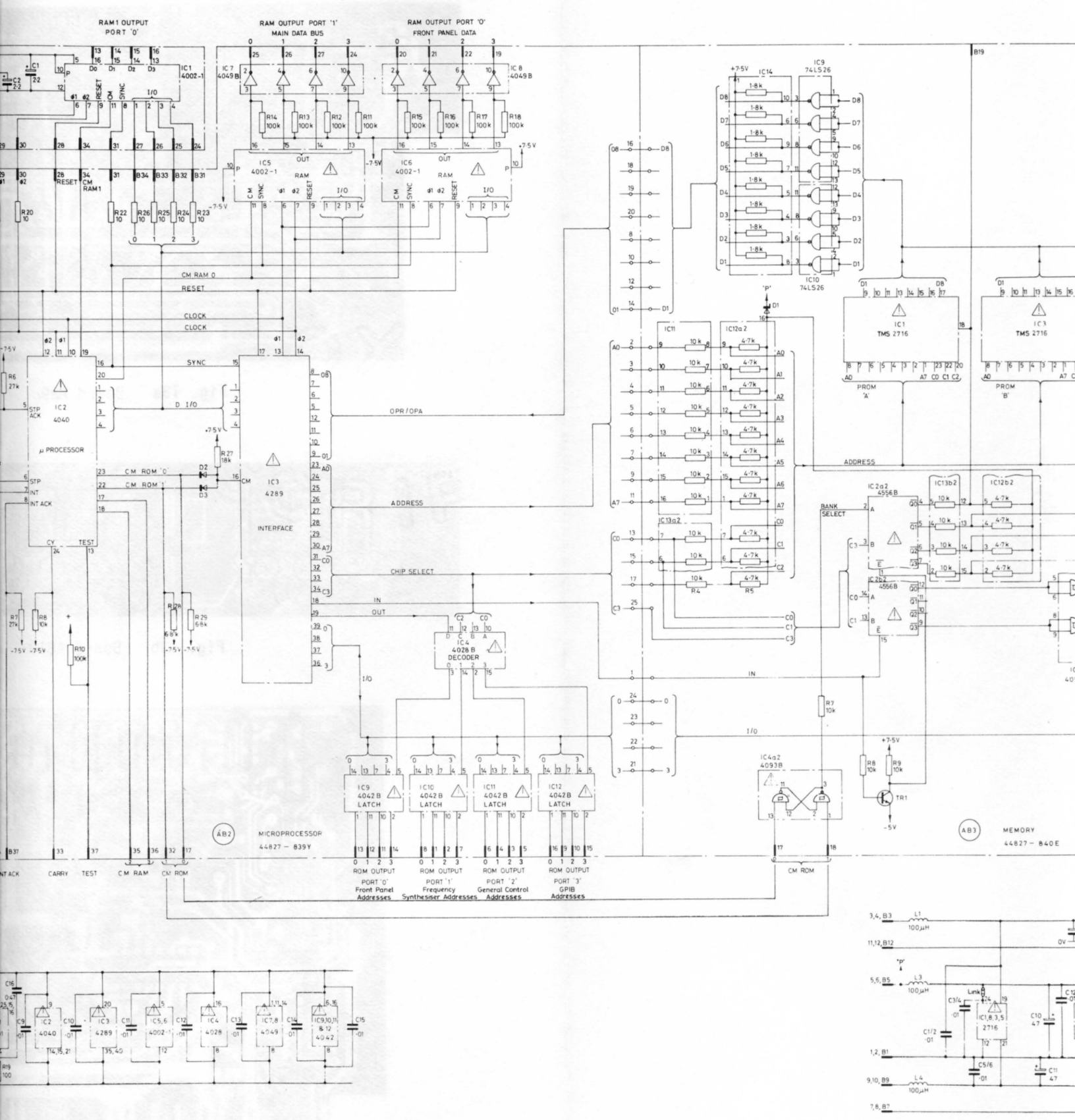
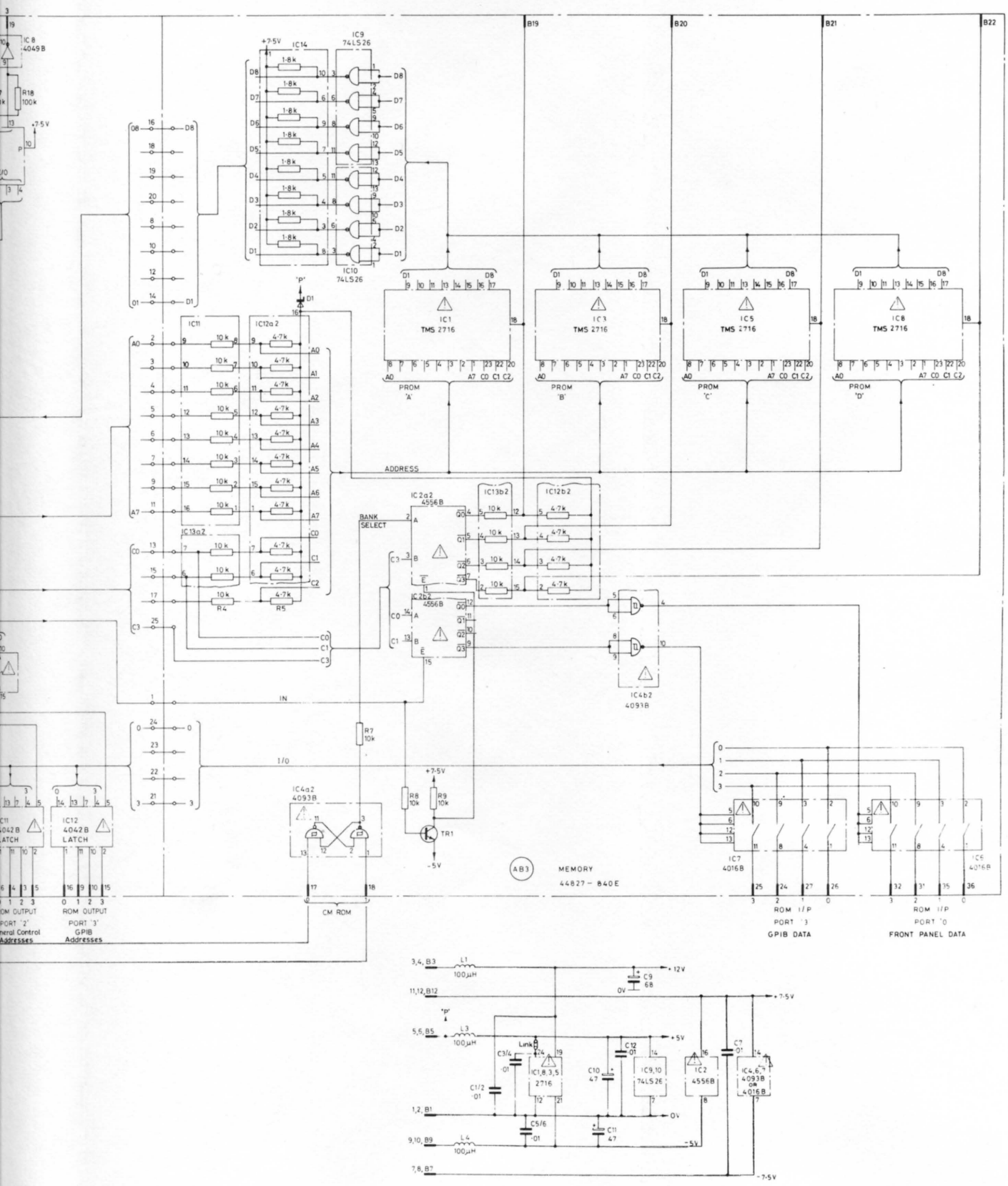


Drg. No. Z 44990-194A

Control unit : Boards AB2, AB3, AB17



Drg. No. Z 44990-194A Sht. 2 of 5, Iss. 1

unit : Boards AB2, AB3, AB17

Fig. 12

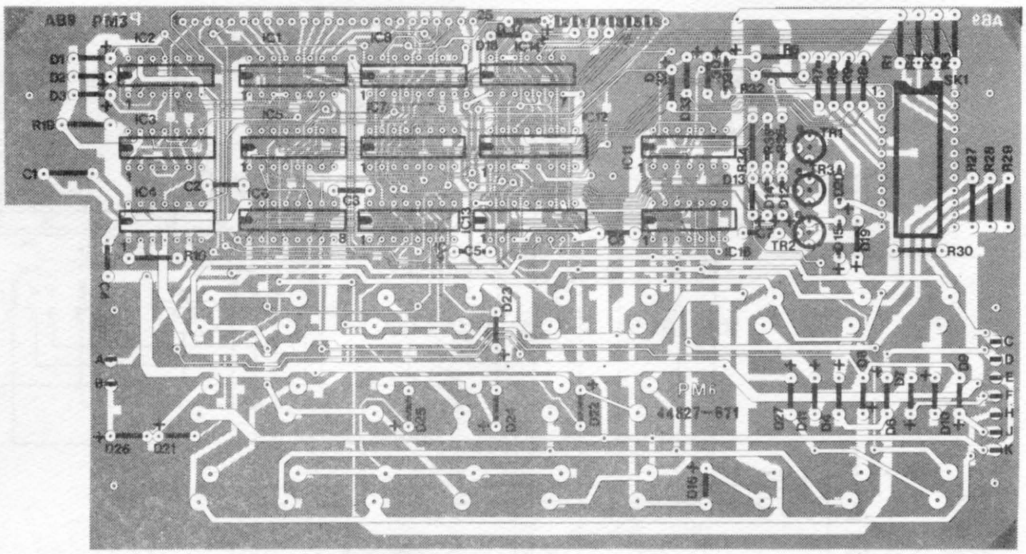


Fig. 13a Board AB9

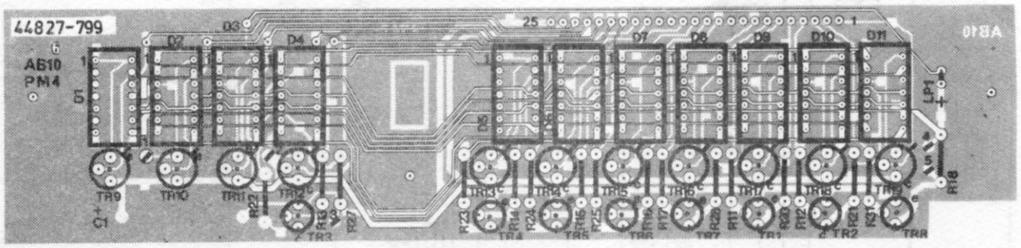


Fig. 13b Board AB10

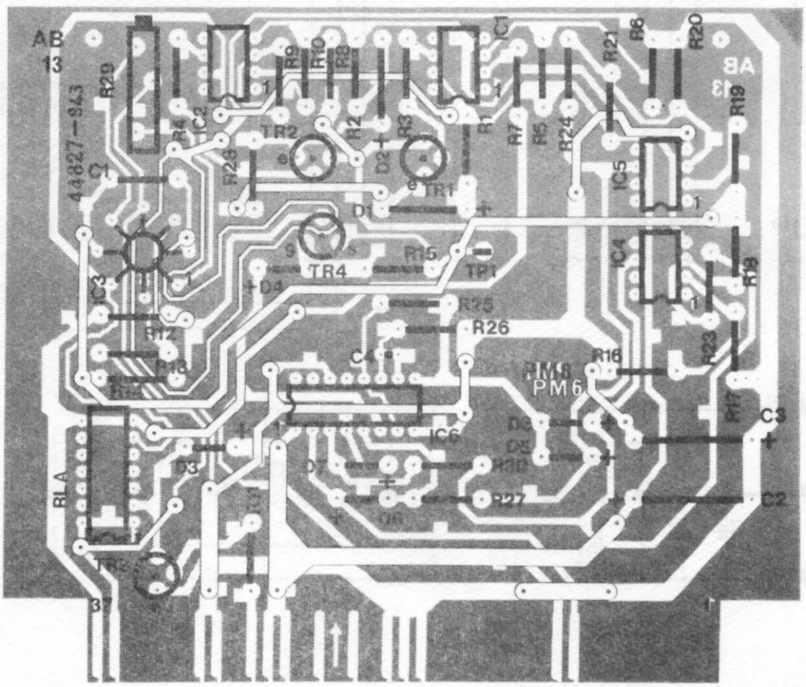


Fig. 13c Board AB13

ment layouts

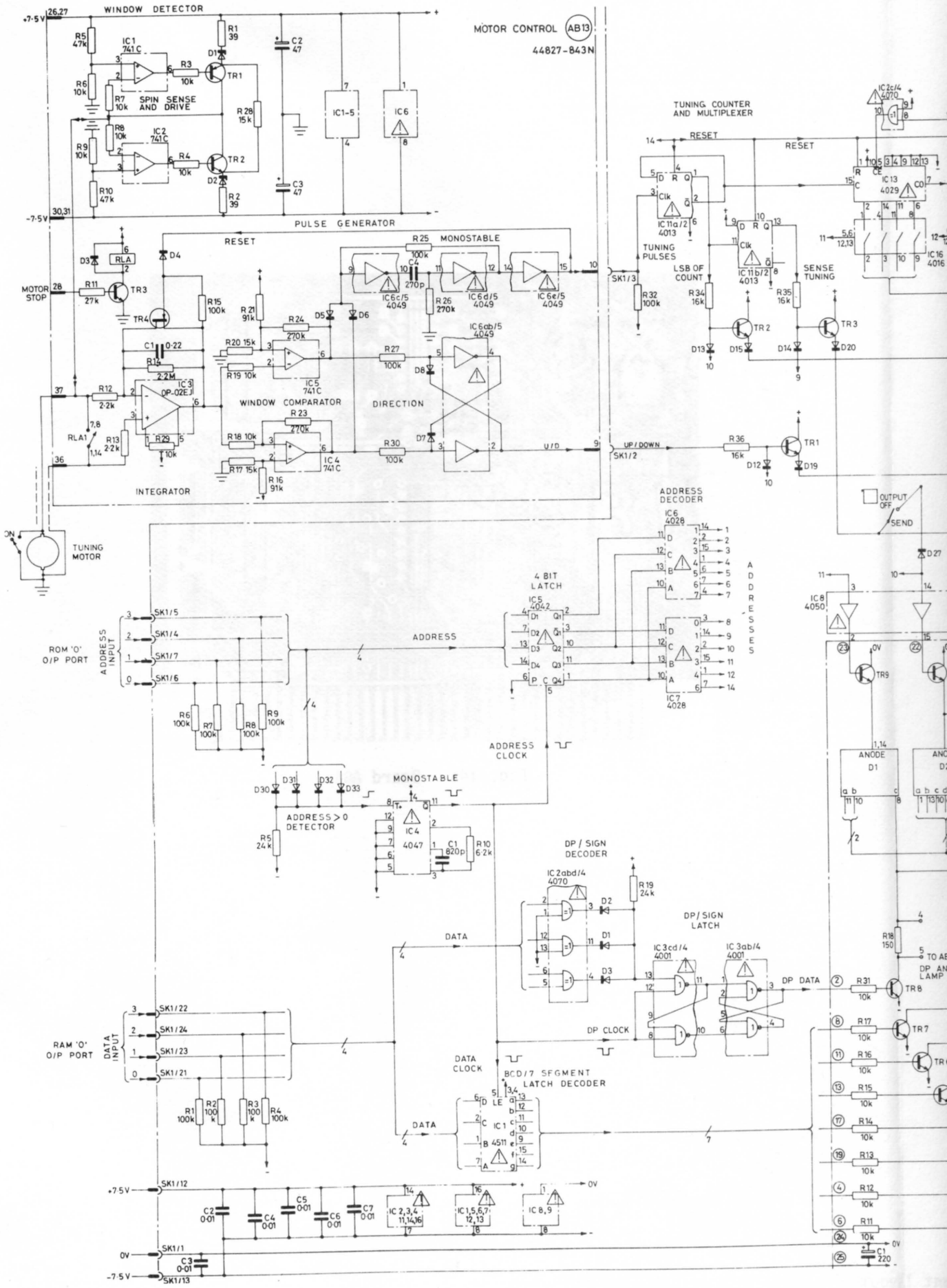


Fig. 13

Display unit : Boards AB9, AB

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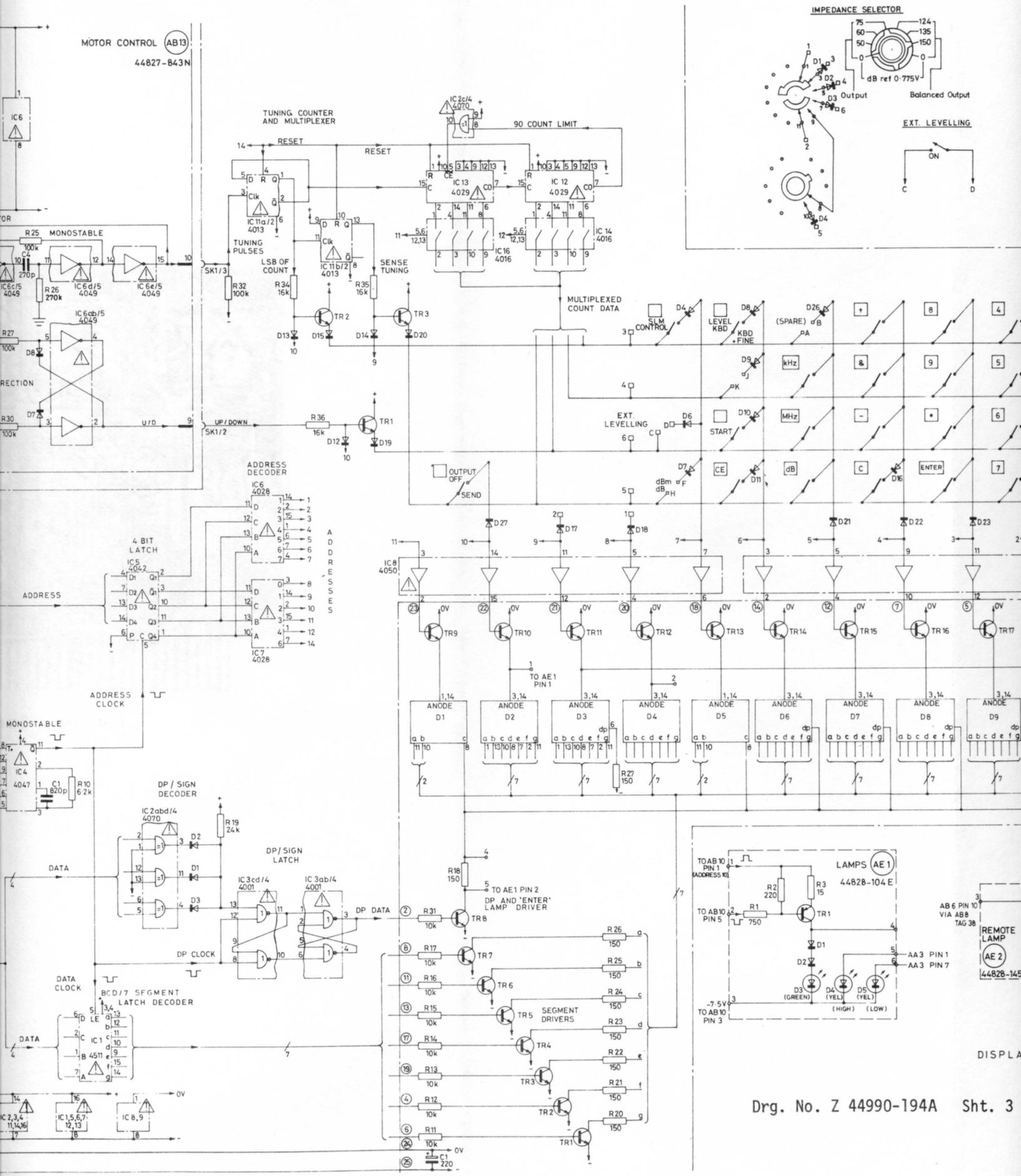
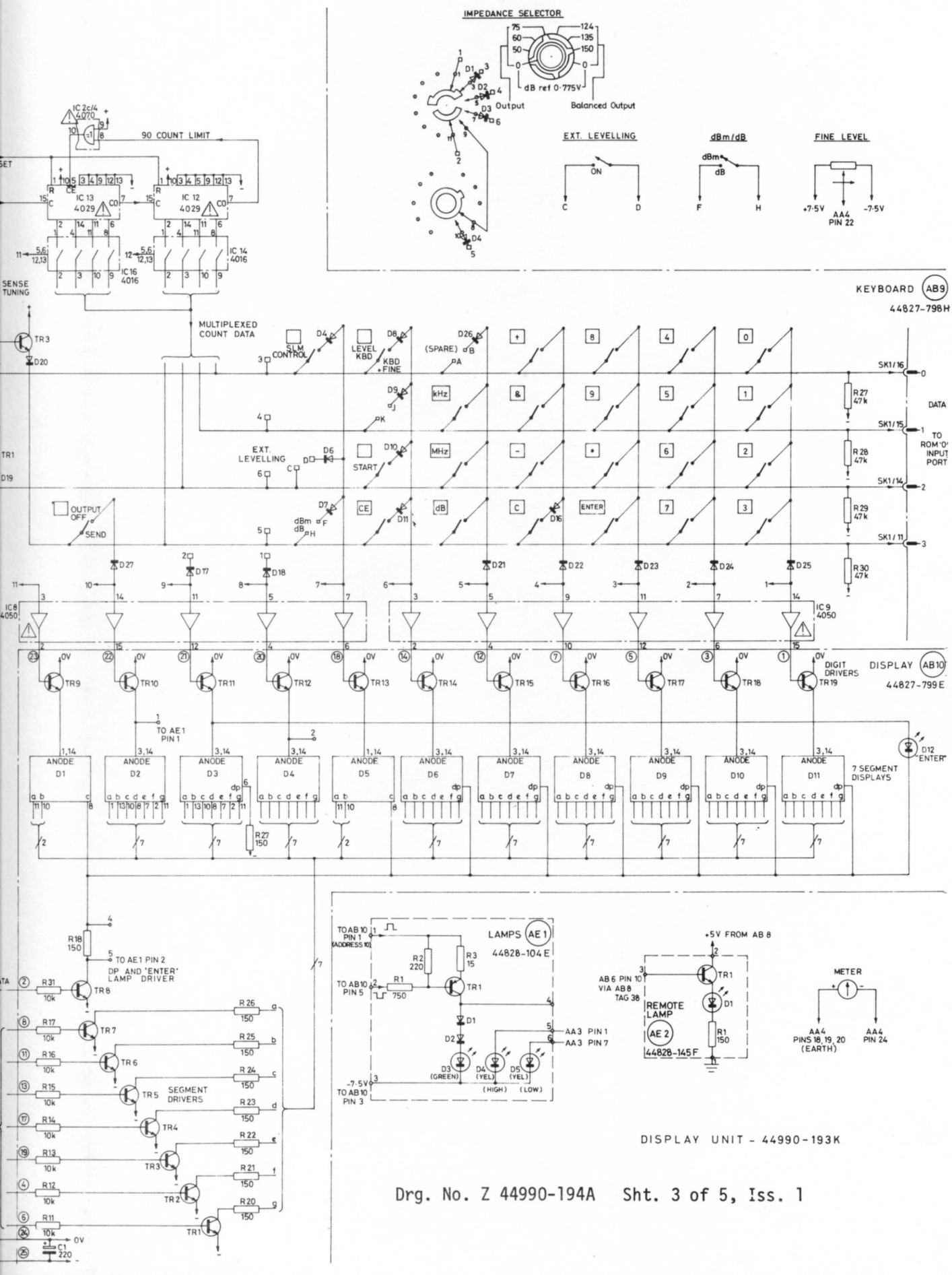


Drg. No. Z 44990-194A Sht. 3

Display unit : Boards AB9, AB10, AB13, AE1, AE2



DISPLAY UNIT - 44990-193K

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Boards AB9, AB10, AB13, AE1, AE2

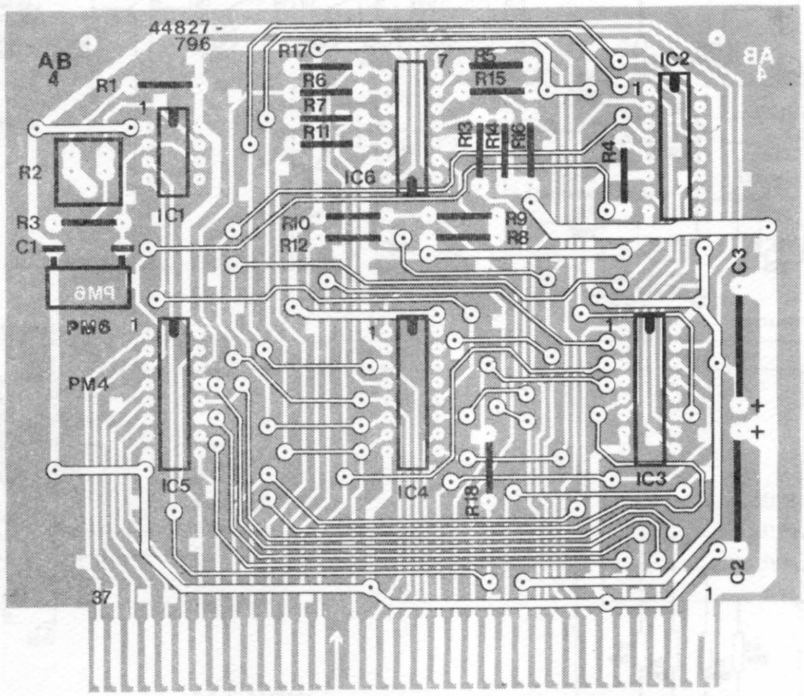

Fig. 14a Board AB4

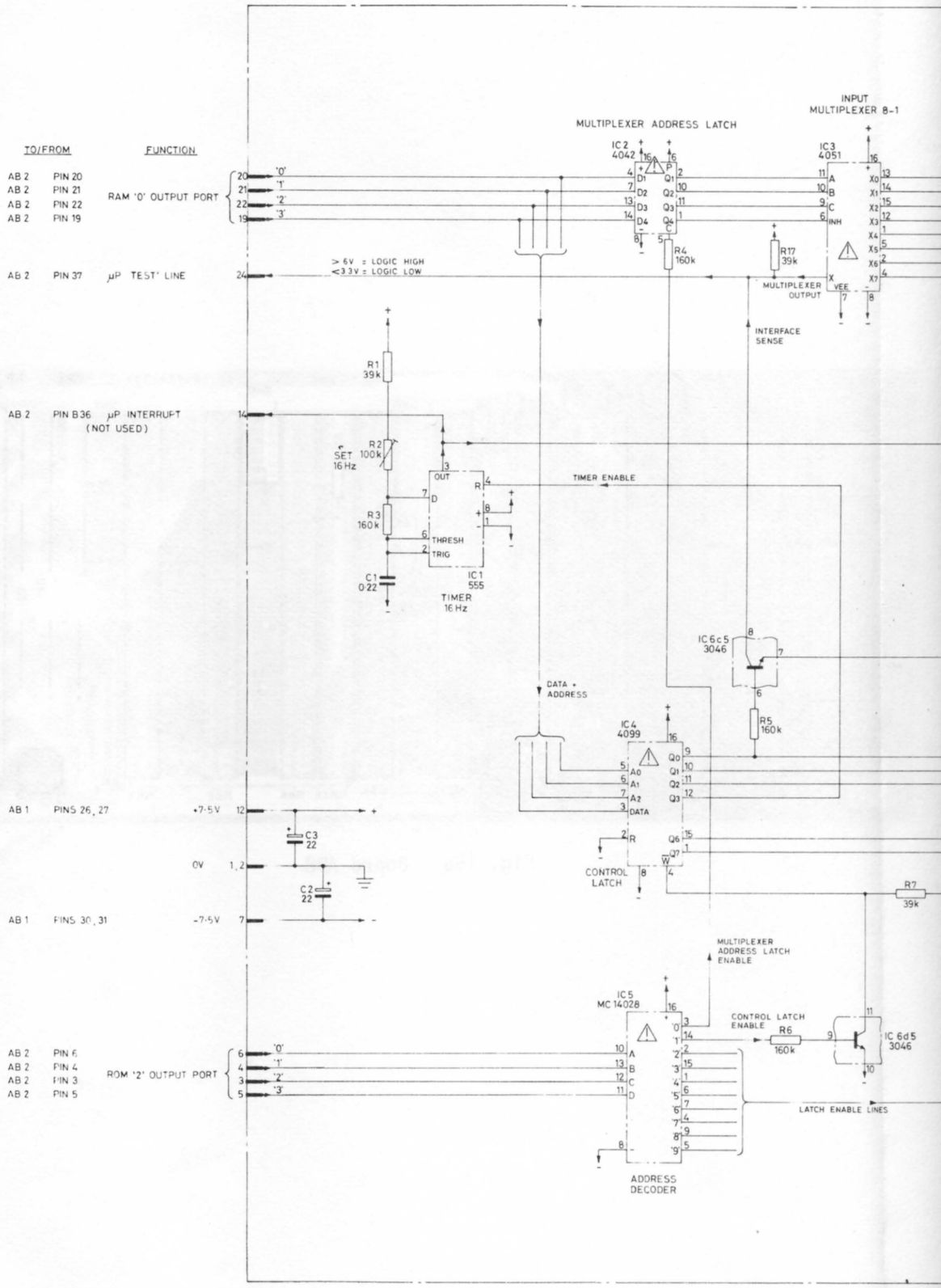

Fig. 14

Control unit : B

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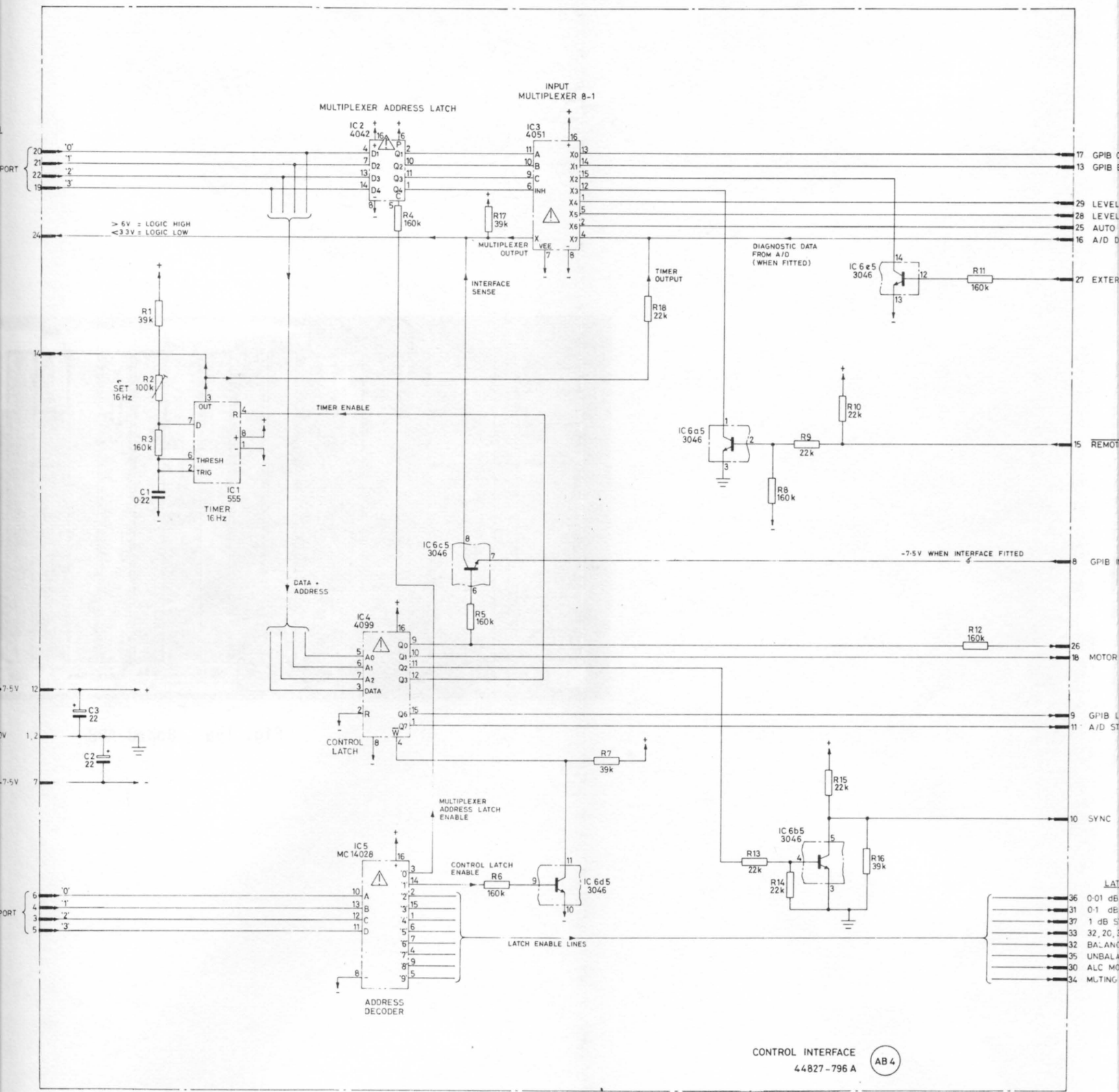
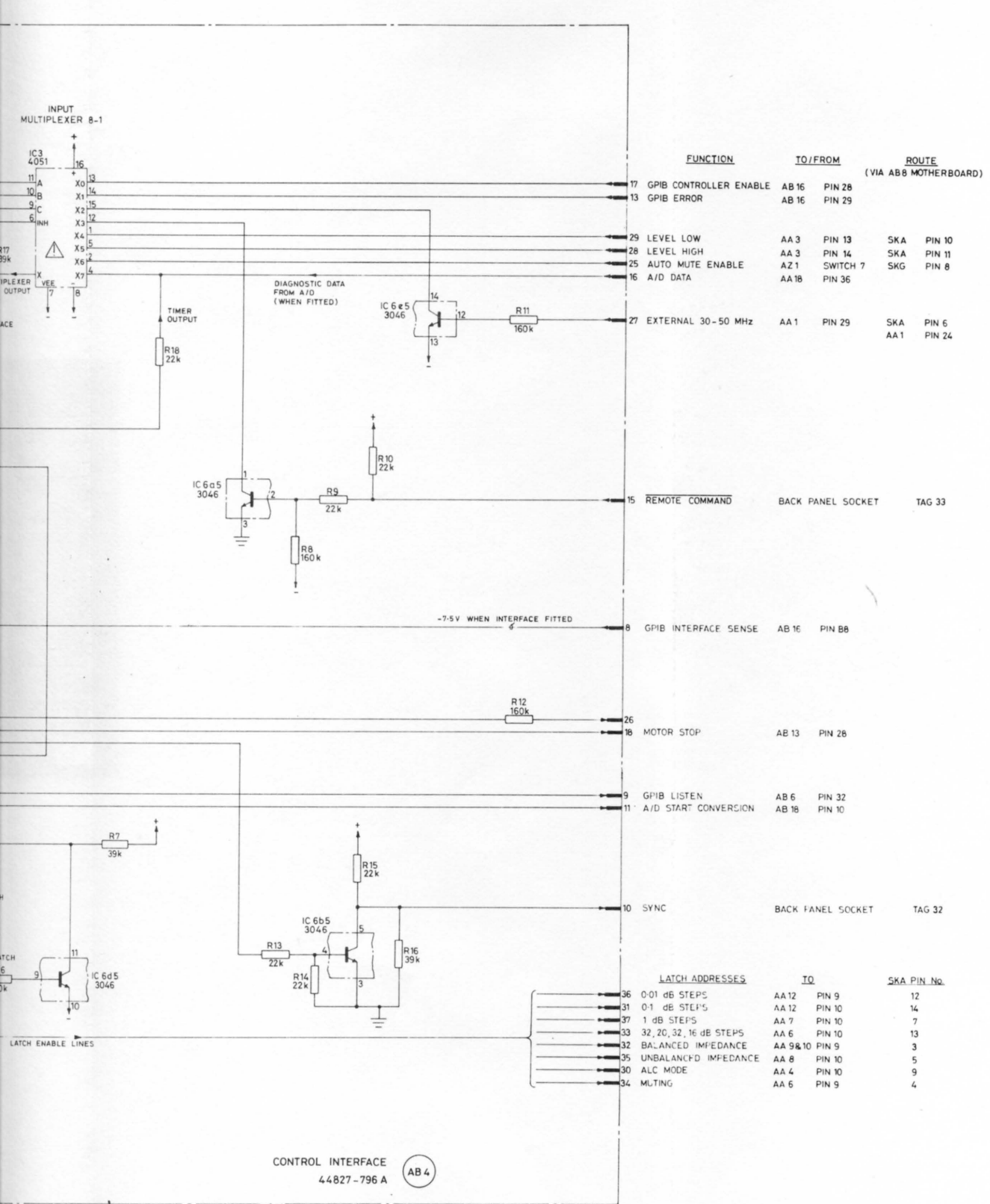


Drg. No. Z 44990-194A Sht. 4

Control unit : Board AB4



	FUNCTION	TO/FROM		ROUTE (VIA AB8 MOTHERBOARD)	
17	GPIB CONTROLLER ENABLE	AB 16	PIN 28		
13	GPIB ERROR	AB 16	PIN 29		
29	LEVEL LOW	AA 3	PIN 13	SKA	PIN 10
28	LEVEL HIGH	AA 3	PIN 14	SKA	PIN 11
25	AUTO MUTE ENABLE	AZ 1	SWITCH 7	SKG	PIN 8
16	A/D DATA	AA 18	PIN 36		
27	EXTERNAL 30-50 MHz	AA 1	PIN 29	SKA AA 1	PIN 6 PIN 24
15	$\overline{\text{REMOTE COMMAND}}$	BACK PANEL SOCKET		TAG 33	
8	GPIB INTERFACE SENSE	AB 16	PIN B8		
26					
18	MOTOR STOP	AB 13	PIN 28		
9	GPIB LISTEN	AB 6	PIN 32		
11	A/D START CONVERSION	AB 18	PIN 10		
10	SYNC	BACK PANEL SOCKET		TAG 32	

	LATCH ADDRESSES	TO		SKA PIN No.
36	0·01 dB STEPS	AA 12	PIN 9	12
31	0·1 dB STEPS	AA 12	PIN 10	14
37	1 dB STEPS	AA 7	PIN 10	7
33	32, 20, 32, 16 dB STEPS	AA 6	PIN 10	13
32	BALANCED IMPEDANCE	AA 9&10	PIN 9	3
35	UNBALANCED IMPEDANCE	AA 8	PIN 10	5
30	ALC MODE	AA 4	PIN 10	9
34	MUTING	AA 6	PIN 9	4

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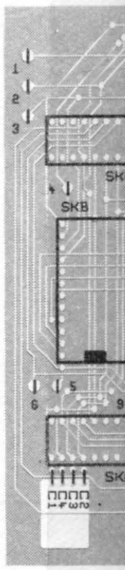
ntrol unit : Board AB4

Fig. 14



Component layout

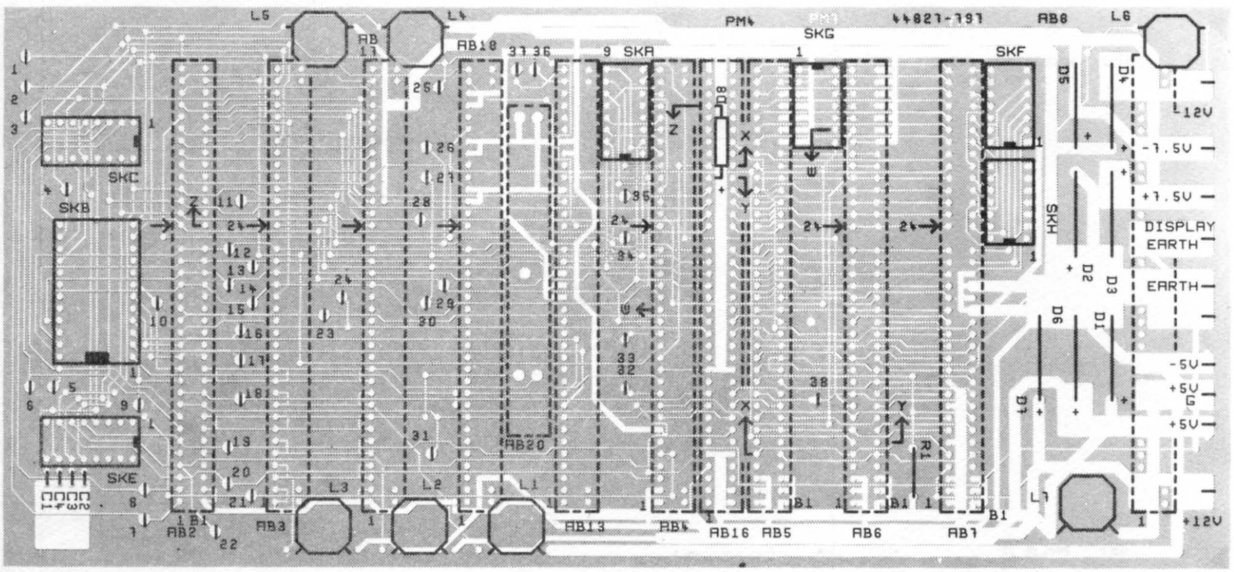
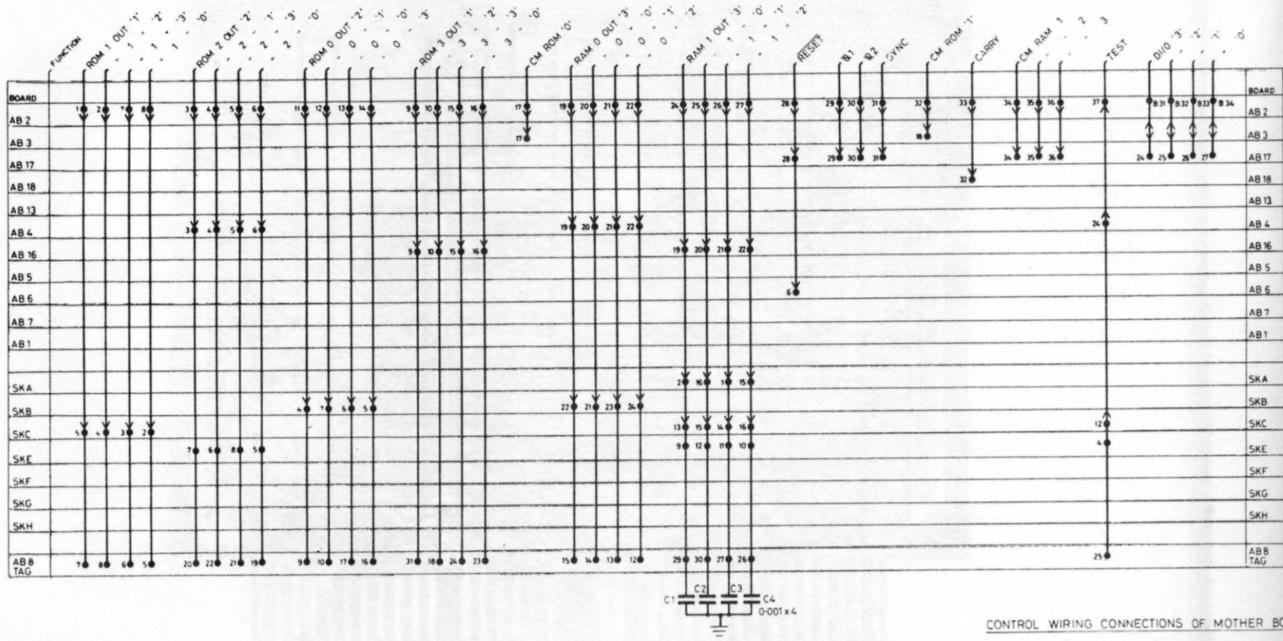
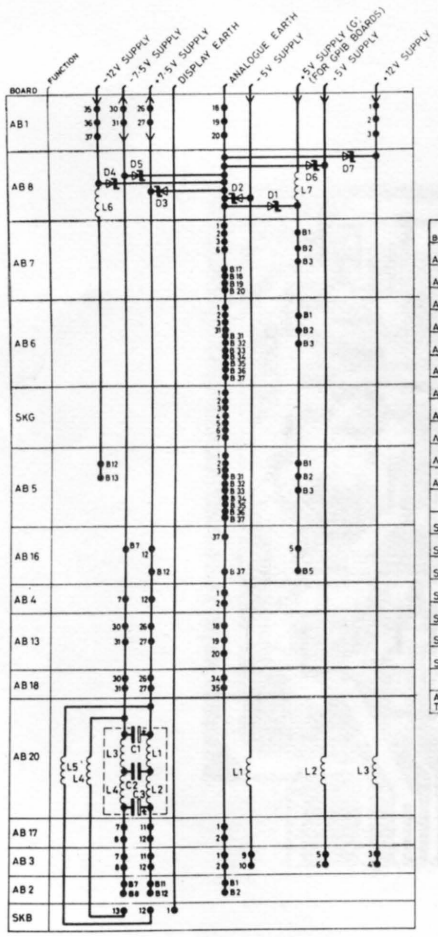


Fig. 15a Board AB8

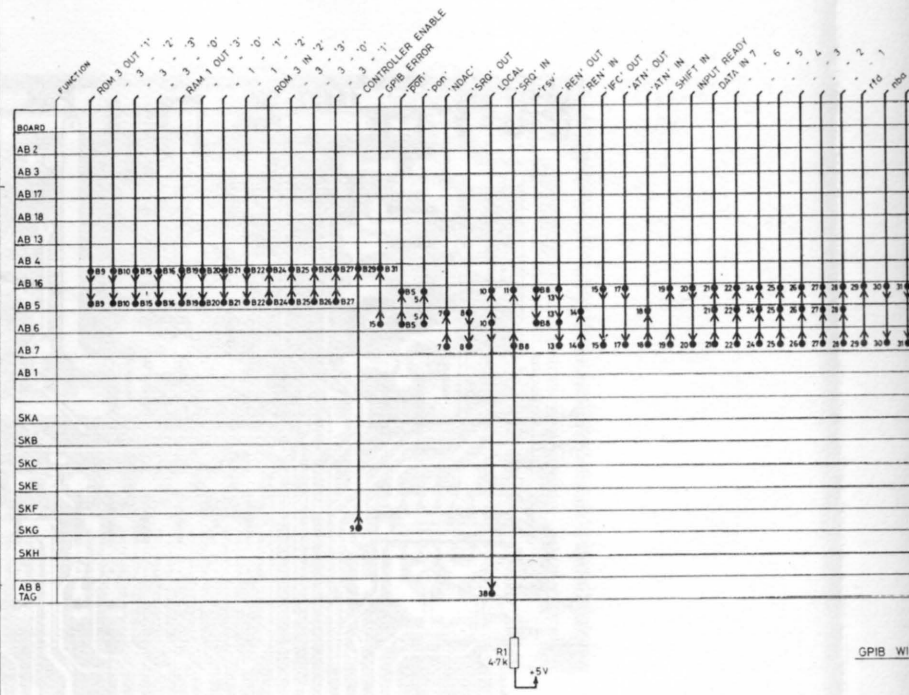
nent layout



CONTROL WIRING CONNECTIONS OF MOTHER BO



POWER SUPPLY ON AB 8



GPIB WI

Fig. 15

Control unit : Board AB8 GPIB

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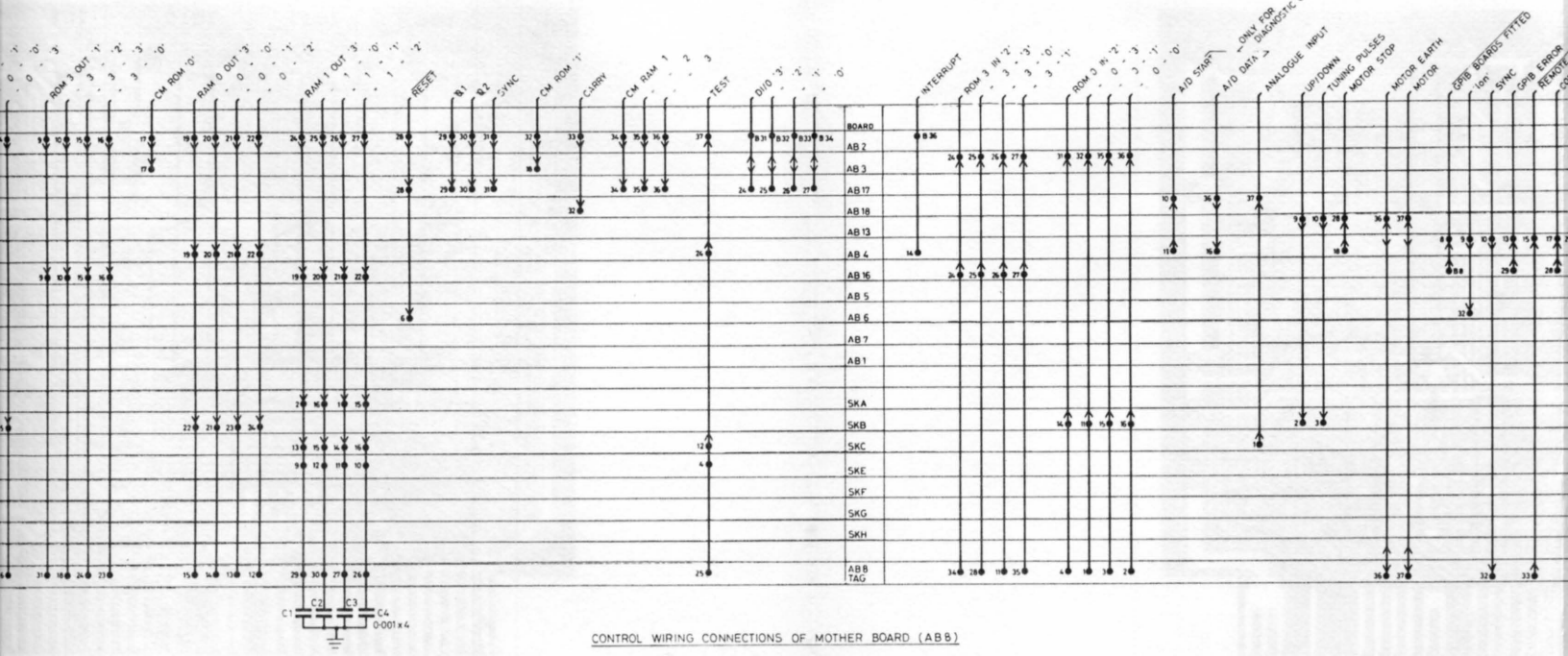
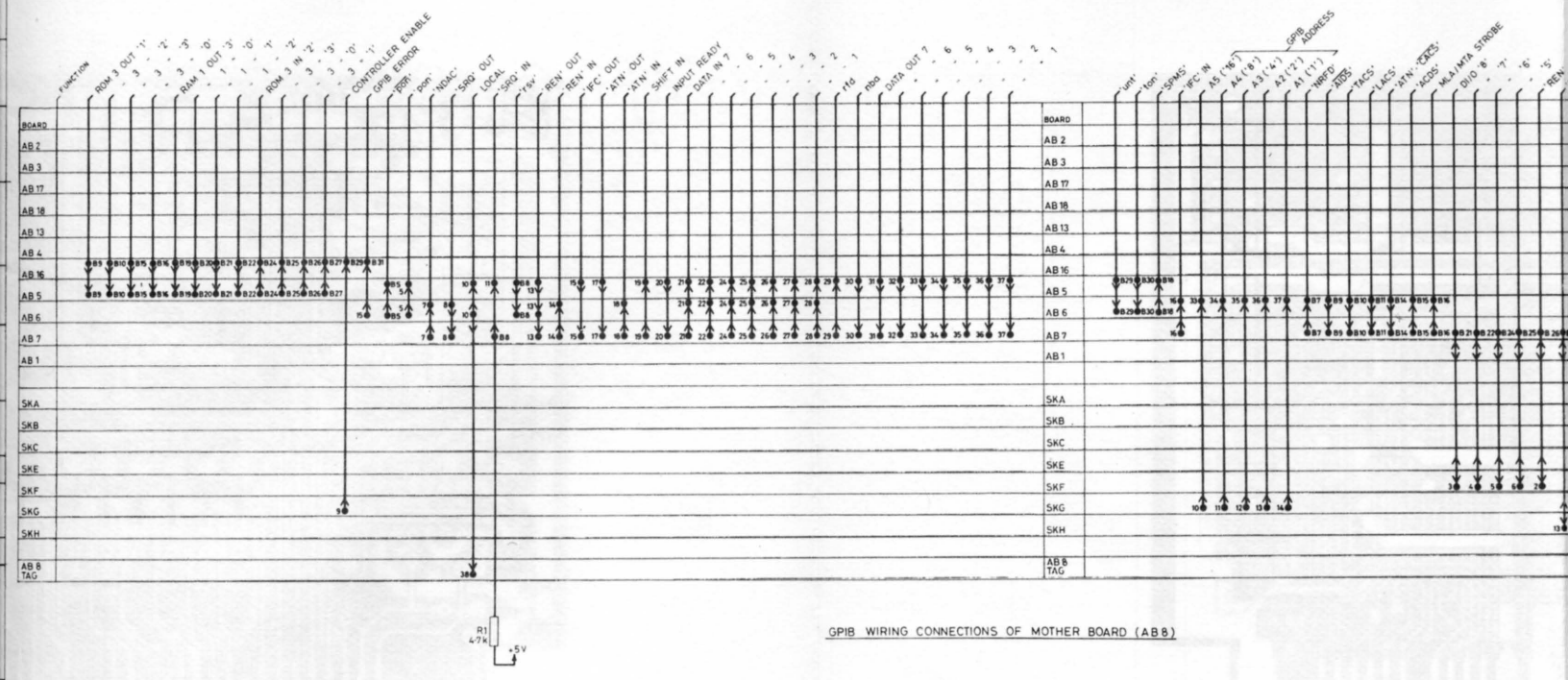


CONTROL WIRING CONNECTIONS OF MOTHER BOARD (AB8)

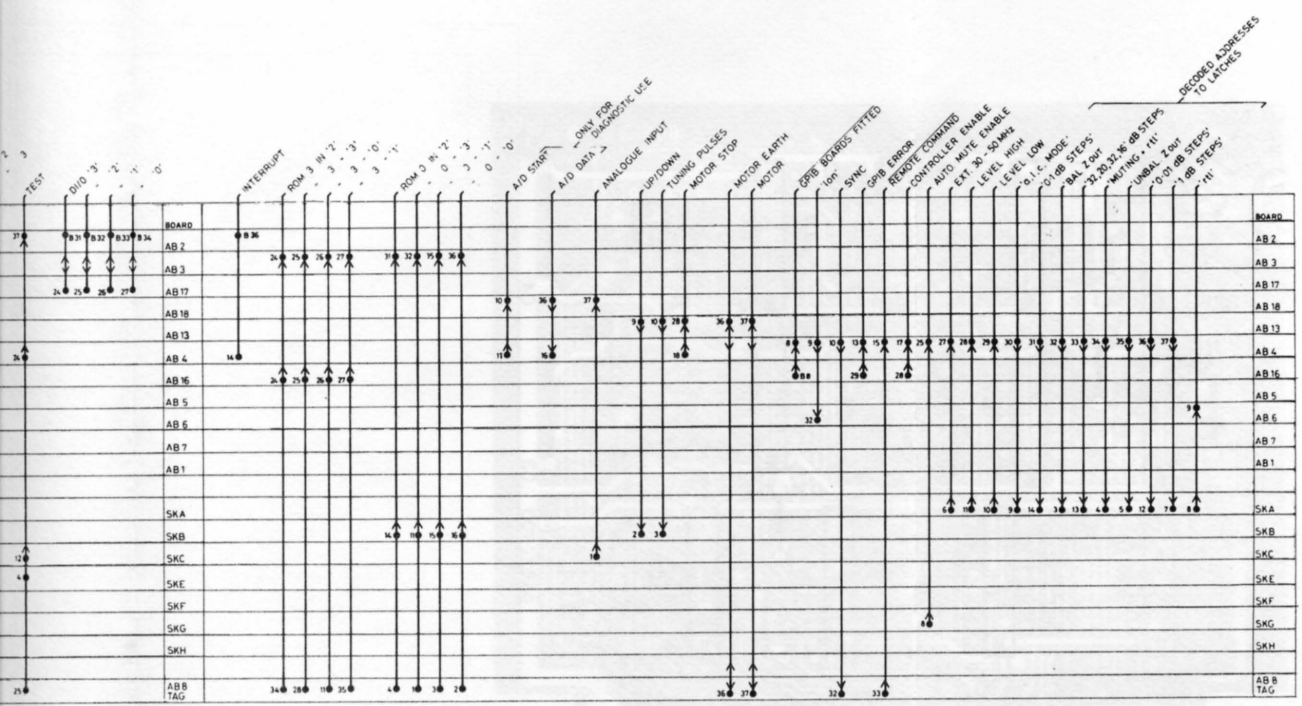


GPIB WIRING CONNECTIONS OF MOTHER BOARD (AB8)

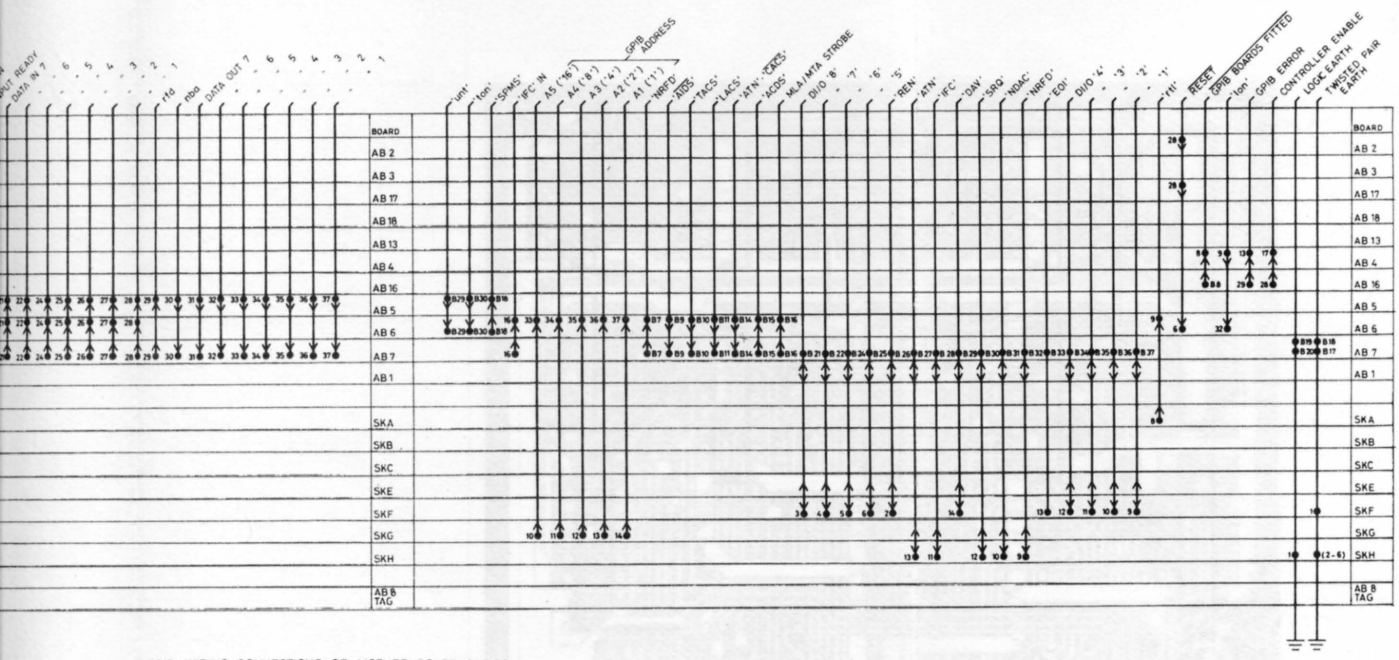
NOTE : SOME UNUSED CONNECTIONS ARE NOT SHOWN ON THIS DIAGRAM.

Drg. No. Z 44990-

Control unit : Board AB8 GPIB wiring connections



NG CONNECTIONS OF MOTHER BOARD (AB8)



GPIB WIRING CONNECTIONS OF MOTHER BOARD (AB8)

NOTE SOME UNUSED CONNECTIONS ARE NOT SHOWN ON THIS DIAGRAM.

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Board AB8 GPIB wiring connections

Fig. 15

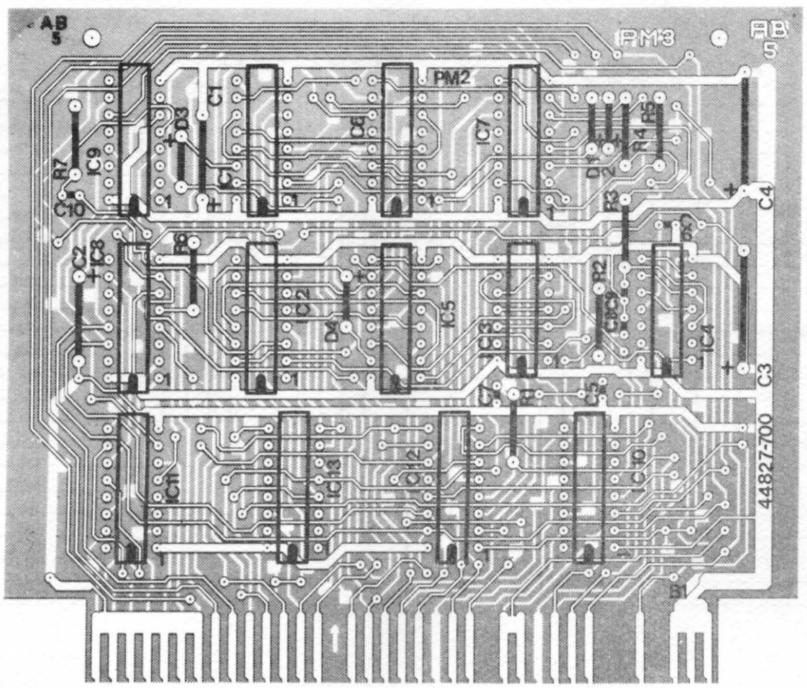

Fig. 16a Board AB5

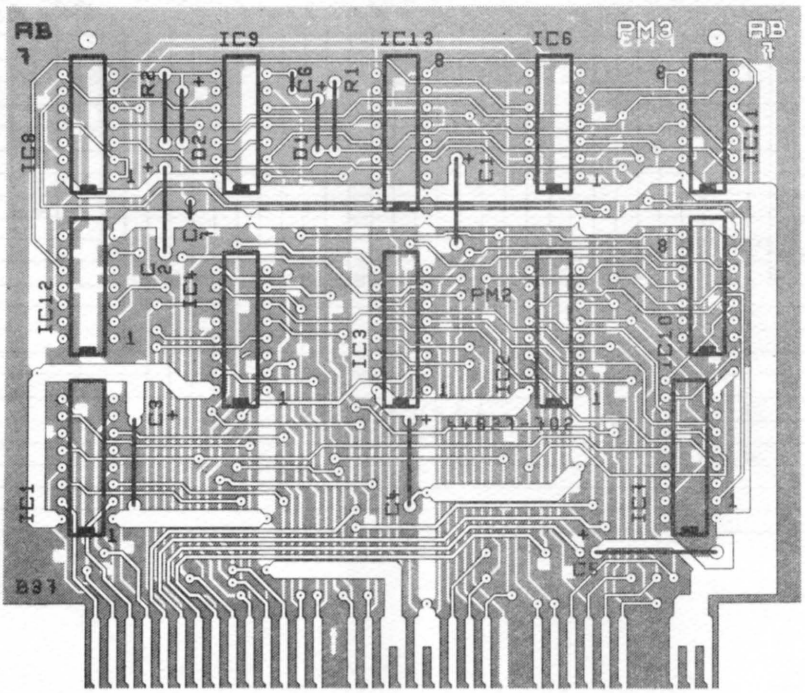

Fig. 16c Board AB7

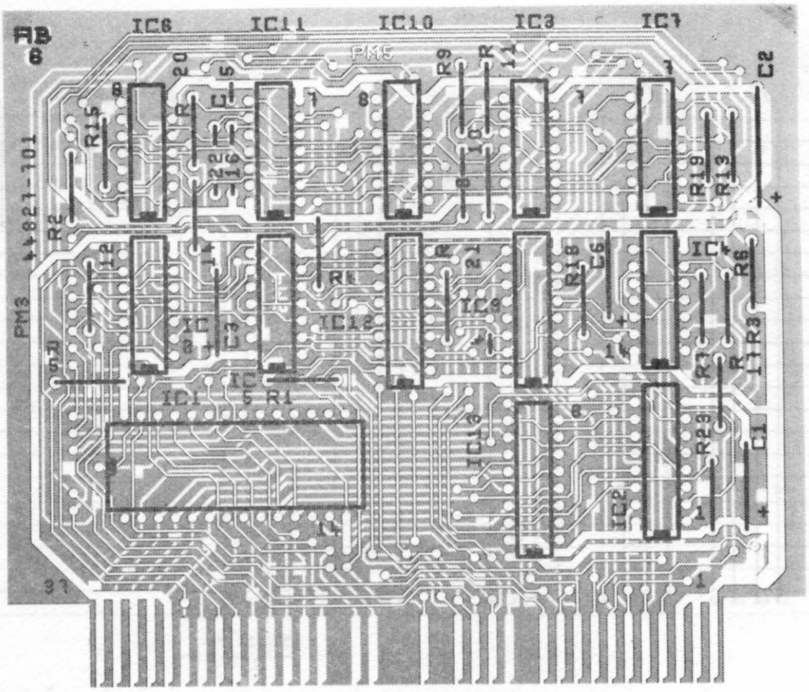

Fig. 16b Board AB6

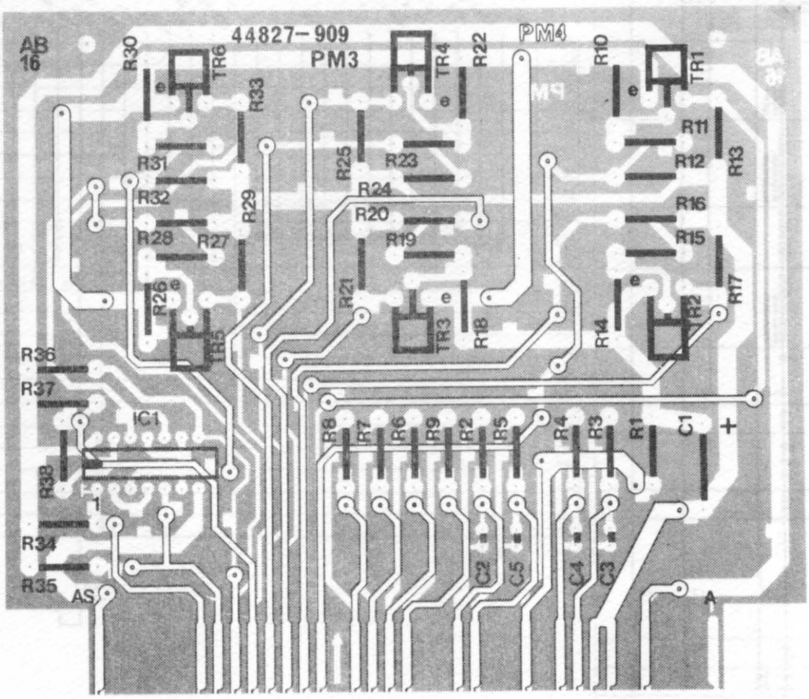

Fig. 16d Board AB16

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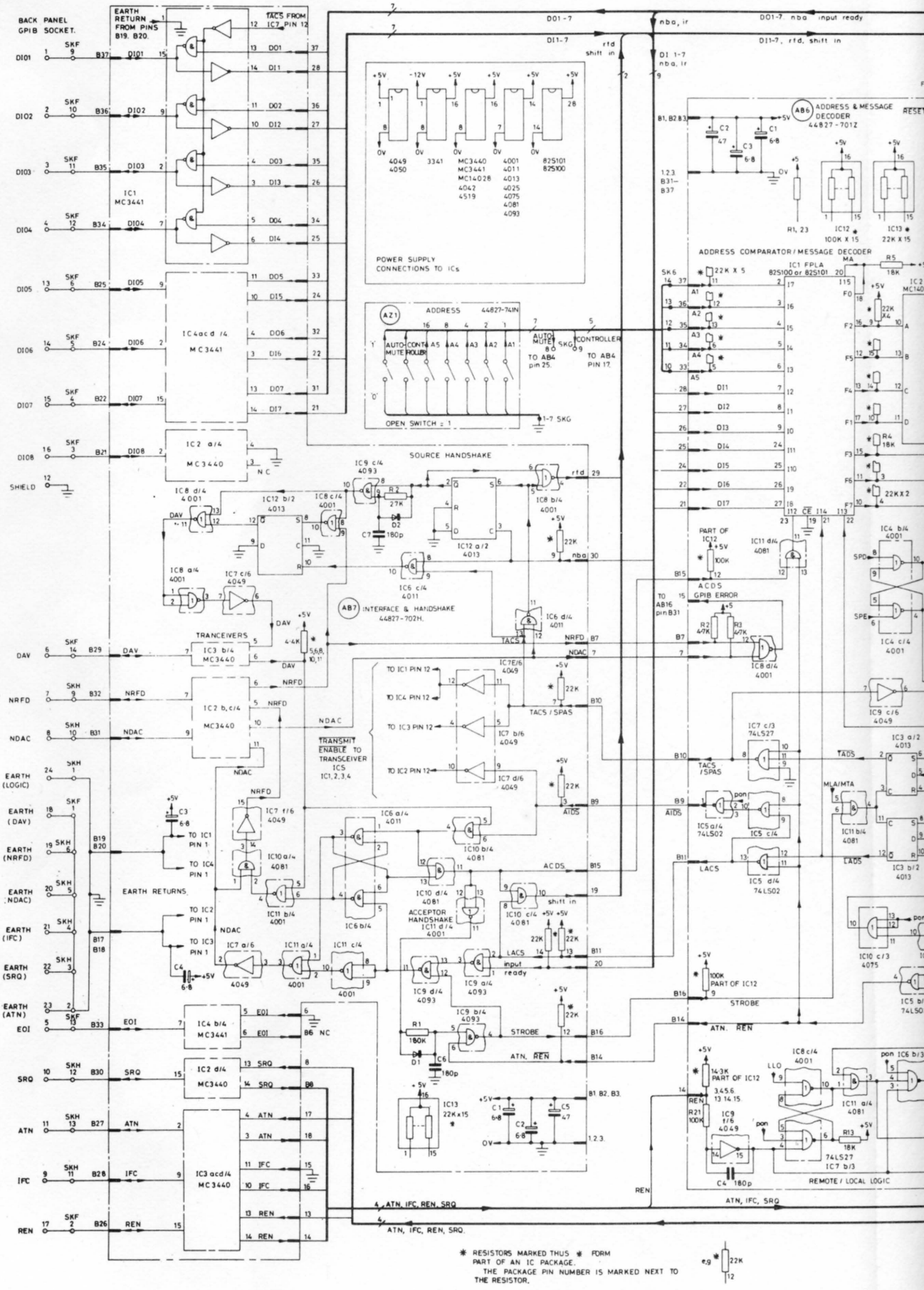

Fig. 16

Interface : Boards AB5,

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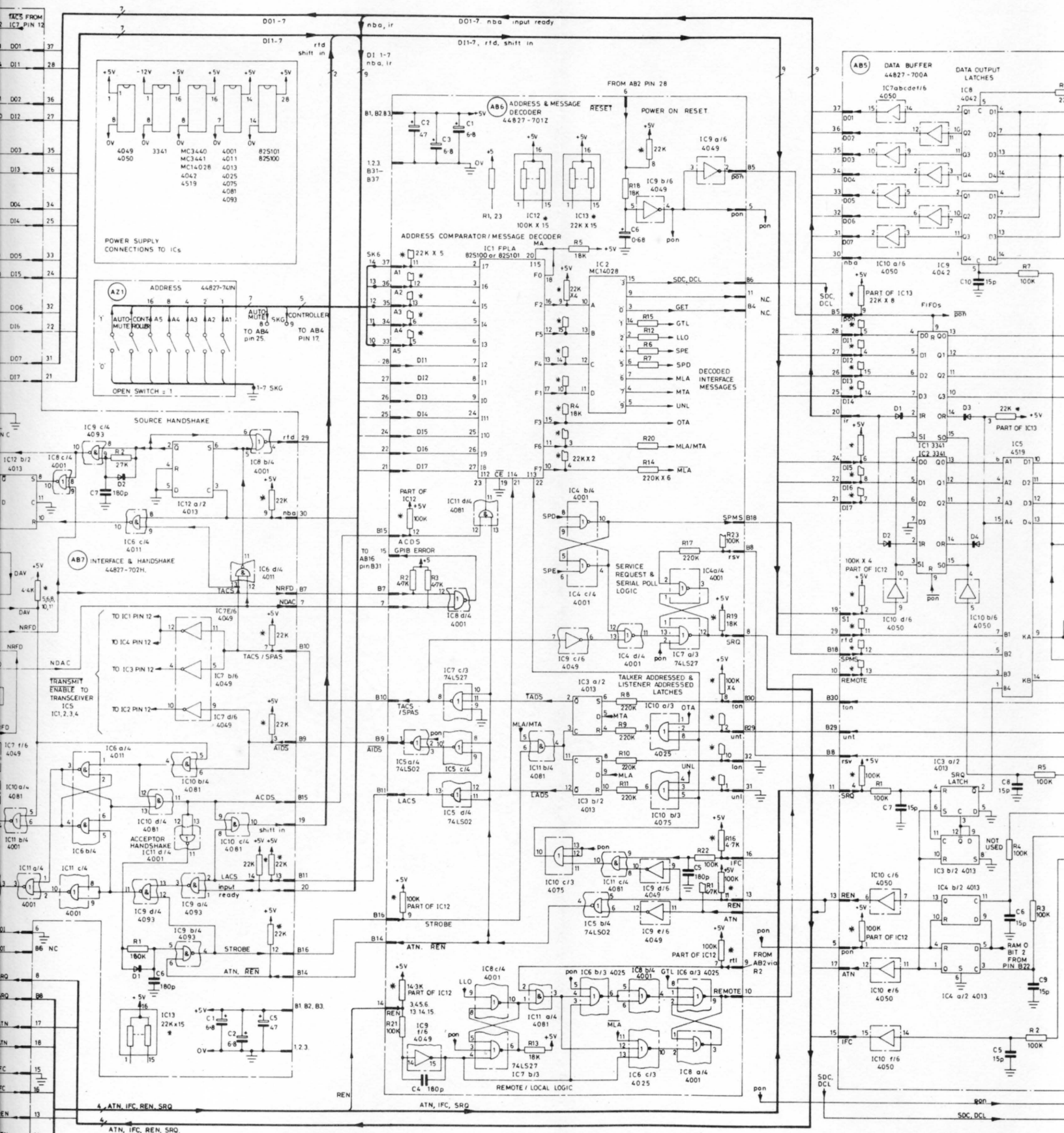
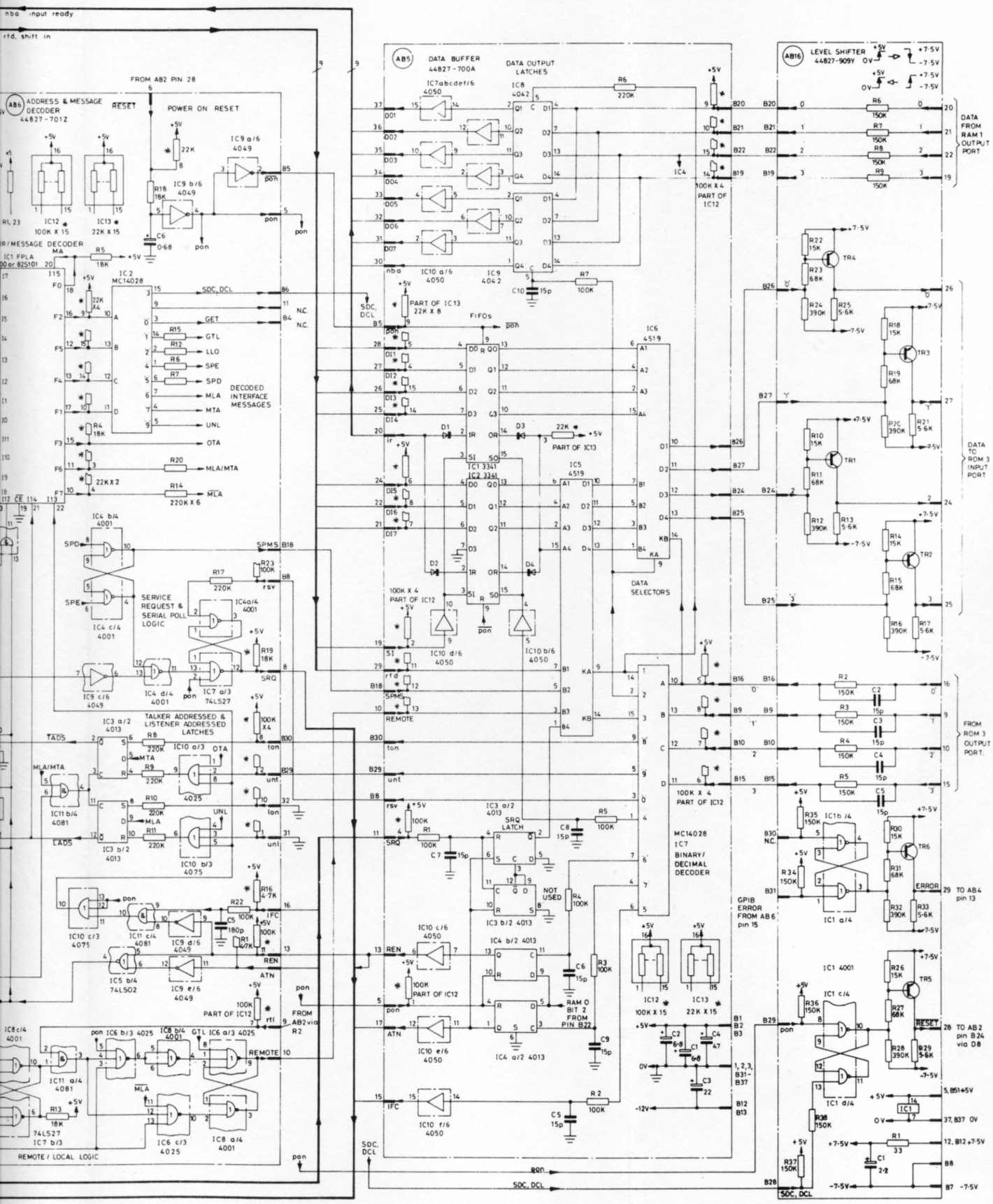


* RESISTORS MARKED THUS * FORM PART OF AN IC PACKAGE.
THE PACKAGE PIN NUMBER IS MARKED NEXT TO THE RESISTOR.

e.g * 22K 12

Drg. No. Z 4

Interface : Boards AB5, AB6, AB7, AB16



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: Boards AB5, AB6, AB7, AB16