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Instruction Manual
No. EB 2370-015
for

110 MHz Spectrum Analyser
TF 2370

Model No. 52370-015

MARCONI INSTRUMENTS LIMITED
ST. ALBANS HERTFORDSHIRE ENGLAND

GL 0.53c
1/86/N

Part No. 46881-240E

EB 2370-015
1j - 1/86

Sweep speed :	100 ms to 100 seconds in 1, 2, 5 sequence automatically selected to match the selected SWEEP RANGE and FILTER BANDWIDTH. A x5 speed up over the optimum is available by press button operation. A 100 sec. sweep is available for use with an X-Y recorder.
Filter bandwidth :	-3 dB filter bandwidths of 5 Hz, 50 Hz, 500 Hz, 5 kHz and 50 kHz. These are automatically selected to give up to three filter bandwidths (NARROW, NORMAL and WIDE) to match the selected sweep range.
Bandwidth accuracy :	±20% of stated 3 dB bandwidth.
Bandwidth selectivity :	60 dB/3 dB filter bandwidth ratio better than 10:1.
Resolution and noise sidebands :	Using the 5 Hz filter, signals 100 Hz away from a response at 0 dB can be measured to -70 dB.
Long term frequency drift :	After 2 hours warm-up (at constant local ambient temperature): Range switch in kHz position : 10 Hz/min.; 100Hz/10 min.
Temperature drift :	Range switch in kHz position : 100 Hz/°C.

Counter

A nine digit counter having the following modes of operation enables frequency measurement to be made on any part of the spectral display.

PAST CENTRE : After a sweep the counter memorizes the centre frequency of that sweep.

BRIGHT LINE : Counter measures that part of the stored display identified by the bright line electronic cursor.

DIFF : Counter measures the frequency difference between the above two measurements.

Accuracy :

AUTO : ±0.0002%, ±20 Hz, ±1% of full sweep display.

MANUAL : ±0.0002%, ±2 Hz, ±1% of full sweep display. (After 60 minutes warm-up using the internal frequency standard).

Display

An electronic storage system giving infinite persistence with 100 ms minimum data renewal time provides the following STORE/DISPLAY modes of operation.

HIGH DEFN : Full capacity of electronic store (500 x 200 elements) is used to display the spectrum.

DISPLAY 'A' : Half capacity of electronic store (250 x 200 elements) is used to display the spectrum.

DISPLAY 'B' : Remaining half capacity of electronic store (250 x 200 elements) is used to display the spectrum.

Store :

REFRESH 'A' : In this mode, DISPLAY 'A' is continuously refreshed as in HIGH DEFN, DISPLAY 'B' is permanently stored.

Output level

0 dBm, ±3 dB, into 600 Ω load for 100% a.m. signal. Maximum undistorted output level occurs if the unmodulated carrier is set to the top of the screen on 1 dB/div. or 40 dB down from the top of the screen on 10 dB/div.

Probe supply

Supply available at front panel socket to power active probe TK 2374.

X–Y recorder outputs

Enable TF 2370 to be used with X-Y recorder.

X-output - 10 V max. amplitude. 100 s sweep time.

Y-output - 2 V corresponds to top of screen.

Pen-lift - A pair of contacts open during flyback to enable pen lift.

Power requirements

Voltage : 200 to 250 V or 100 to 130 V a.c. at any frequency between 45 and 440 Hz.

Regulation : ±10% on the nominal supply voltage.

Power consumption : Approximately 130 W (170 VA).

Safety regulations

Complies with IEC 348 and BS 4743 Safety Requirements.

Limit range of operation

Temperature : $0^{\circ}C$ to $55^{\circ}C$.

Storage and transport

Temperature : $-40^{\circ}C$ to $+70^{\circ}C$.

Humidity : Up to 90% relative humidity.

Altitude : Up to 2500 m (pressurized freight at 27 kPa differential i.e. 3.9 lbf/in^2.

Dimensions and weight

	Height	*Width*	*Depth*	*Weight*
Display unit (with covers) :	172 mm (6 3/4 in)	440 mm (17 5/16 in)	516 mm (20 5/16 in)	20 kg (44 lb)
RF unit (with covers and clips) :	156 mm (6 1/8 in)	453 mm (17 13/16 in)	516 mm (20 5/16 in)	19.5 kg (43 lb)

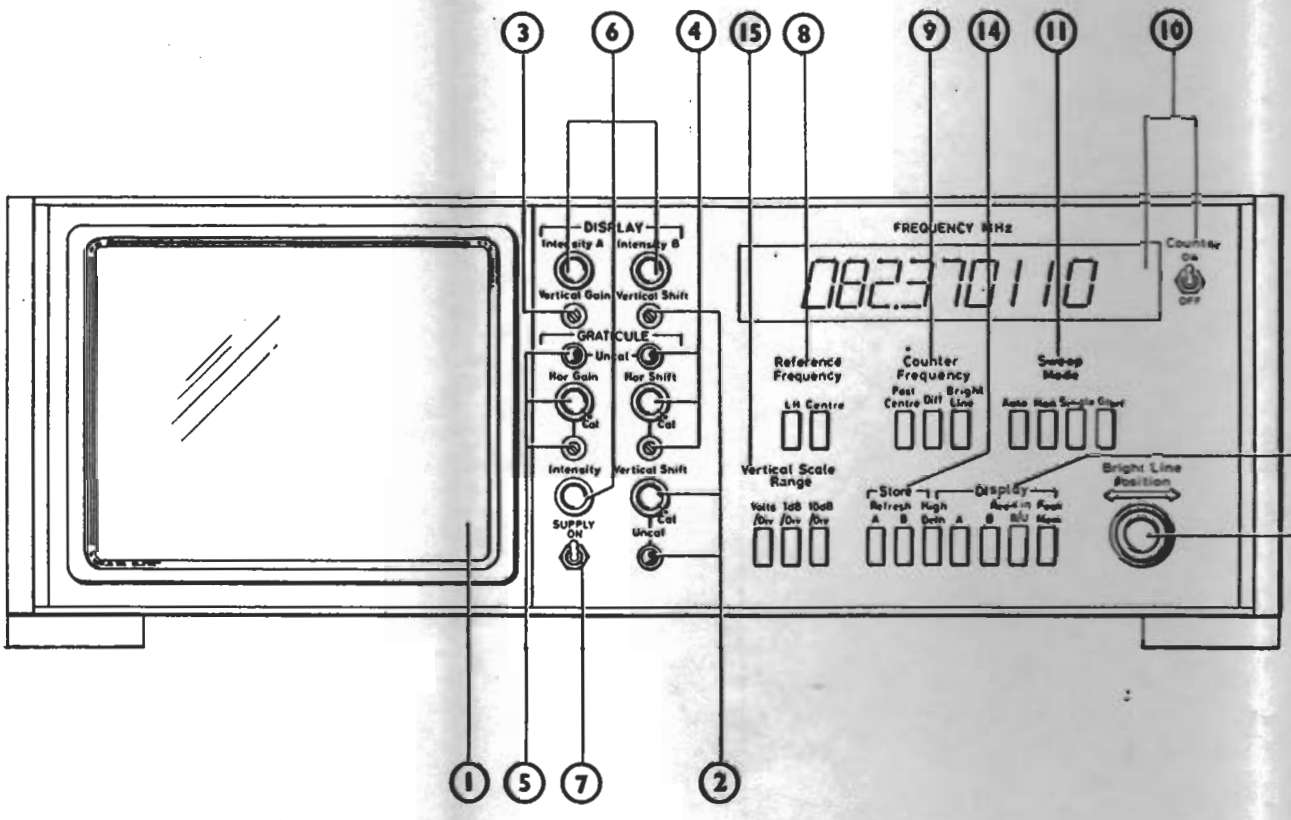
1.3 ACCESSORIES

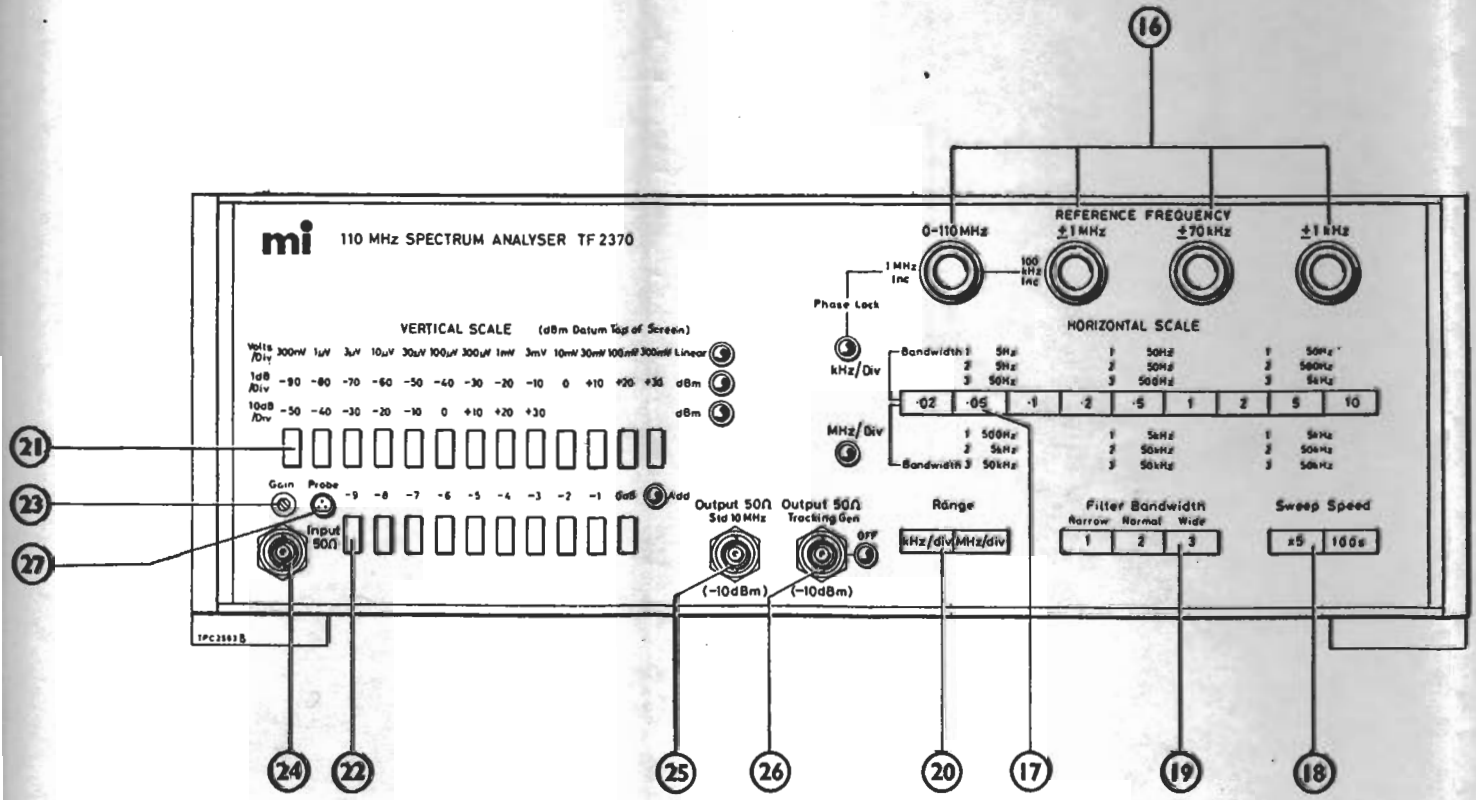
Supplied

Mains lead, 43123-076.
Connector assembly (umbilical), 2 off, 43169-005.
Extender board 44827-235.
Board extractor 41700-048.
Stay assembly 34900-209.
Fuse kit 46883-219.
Plug, 15-way 23435-406.
Plug shell, 15-way 23435-464.
Operating manual EBS 2370-015, Part no. 46881-241U.
Protective cover, 2 off, 41690-087N.

Optional

Adapter (BNC to phone jack) 43168-016.
RF fuse unit, RM 9884, 43281-007.
Carrying case, 2 off, 54112-111.
Rack mounting kit 54127-211.
Connector assembly (for servicing) 2 off, 43169-010.
Camera hood 46883-267.
Proprietary pack 37136-412.
Instruction manual EB 2370-015, Part no. 46881-240E.





Chapter 2

Operation

2.1 PREPARATION FOR USE

The instrument is constructed in two halves, the upper display unit, and the lower r.f. unit, which are connected at the rear by connector assemblies (43169-005), and are held in position by four toggle latches. The instrument is normally supplied with the units connected. The units, which are adjusted to work together, are identified by identical serial numbers, and may be disconnected for ease of transporting.

Supply voltage adjustment

The voltage selection panel, located on the rear panel of the display unit, is adjusted as follows :

Remove the bar plug, and re-insert in the socket panel so that the arrow points to the correct supply voltage. Normally, the instrument is dispatched with the voltage set to 240 V a.c.

Supply lead

The supply lead is a free cable fitted at one end with a female plug which connects to the instrument. When fitting a suitable supply plug, note that the wires are colour coded as follows :

Earth (ground)	-	Green/Yellow
Neutral	-	Blue
Line (phase)	-	Brown

Supply fuses

Check that the rear panel supply fuses are correctly rated for the supply in use; 2A, time lag, for the 200 to 250 V range, 4 A, time lag, for the 100 to 130 V range.

2.2 CONTROLS AND CONNECTORS

Front panel

(1) CATHODE RAY TUBE : 13 x 10 cm camera viewfinder display. The electronic graticule consists of 50 minor divisions and 10 major divisions vertically and 12 major divisions horizontally. The first, middle and last vertical frequency calibration lines are dashed to aid easy identification of the centre frequency point and edges of calibrated scan and also to group the dB scale into easily counted 2 division groups.

(2) VERTICAL SHIFT : The variable GRATICULE SHIFT permits vertical movement of the electronic graticule by ±0.6 major division about the nominal setting. A preset DISPLAY SHIFT control permits the correct calibrated value to be set. This control moves the spectral display behind the graticule and thus cannot be set on a stored picture.

(3) VERTICAL DISPLAY GAIN : Permits the gain of the vertical display to be set so that each graticule division corresponds to 1 dB or 10 dB as appropriate. As with the associated preset SHIFT control this cannot be adjusted on a stored picture.

(4) HORIZONTAL GRATICULE SHIFT : The variable SHIFT control permits horizontal shift of the electronic graticule by at least ±1 division.

The preset control enables the graticule to be set, in the CAL position of the variable control, so that it agrees with the counter readout.

(5) HORIZONTAL GRATICULE GAIN : The variable GAIN control permits horizontal expansion of the electronic graticule by at least ±20% about the first dashed line. The preset control enables the graticule calibration to be set, in the CAL position of the variable control.

⑥ DISPLAY 'A', DISPLAY 'B' & GRATICULE INTENSITY : When using the A and B split store mode, these controls operate the individual contrasts of each display. In the HIGH DEFN (13), (14) mode only the DISPLAY 'A' control operates the contrast level. In all cases the GRATICULE control operates the graticule background contrast independently of either display.

⑦ SUPPLY ON switch.

⑧ REFERENCE FREQUENCY : With the CENTRE button pressed, the swept display will expand about the centre line as the sweep width is narrowed (using buttons (17)) whilst if the LH button is pressed it will expand about the left-hand dashed graticule line. The latter mode is particularly useful if the sweep is required from d.c.

⑨ COUNTER FREQUENCY

PAST CENTRE : Every time data is completely renewed on the display the centre frequency is measured and will be displayed on the counter when this button is pressed.

BRIGHT LINE : Whenever the electronic cursor is displayed on the screen (viz. using MANUAL or SINGLE shot modes (11) and the BRIGHT LINE POSITION control (12)) the frequency of any spectral line corresponding to the position of the electronic cursor will be displayed on the counter when this button is pressed.

DIFFERENCE : When this button is used the counter displays the modulus of the difference between the above two frequency values. In all cases the counter resolution is appropriate to the sweep width.

⑩ COUNTER READOUT : Nine digit, 9 segment Burrough Panaplex neon display panel. Readout is in MHz with automatic decimal point location.

COUNTER ON/OFF switch : When OFF, prevents counter leakage from interfering with the instrument sensitivity. The signal at the TRACKING GENERATOR OUTPUT (26) is also switched OFF and the adjacent amber light glows.

To measure the frequency of very low level signals, produce a single sweep with the counter OFF. When the sweep is completed, switch the counter ON and measure the frequency with the BRIGHT LINE POSITION control (12).

Note If the system under test is poorly screened, the counter leakage is greater and it becomes essential to switch the counter OFF when it is not in use.

⑪ SWEEP MODE

AUTO : In this position, the read-in sweep runs continuously, permitting the counter to record the centre frequency during the retrace of each sweep.

SINGLE : In this mode, a single read-in sweep will be initiated every time the START button is pressed and released. After the completion of a sweep, the centre frequency is recorded during retrace as in AUTO. After retrace, a vertical bright line appears on the screen which is an electronic cursor. This line may be positioned anywhere on the screen by means of the BRIGHT LINE POSITION 5-turn potentiometer (12) and the frequency corresponding to that point on the screen may be read from the counter display using the BRIGHT LINE button (9).

MANUAL : When this button is pressed, the read-in sweep stops at whatever point has been reached, and the bright line cursor appears. As for SINGLE, the BRIGHT LINE POSITION potentiometer may be used to position this line anywhere on the screen and the counter reads the frequency if switched to the BRIGHT LINE position. However, as the electronic cursor is moved across the screen, the store will record the input signal levels existing at that time at the frequency corresponding to the bright line position. If it is required to selectively edit the stored display, switch between SINGLE (for movement of cursor with no data renewal) and MANUAL as required. A video filter of 1.5 Hz is included in this position for noise averaging. If the rate of movement of the electronic cursor is too fast, some of the original stored picture will be left on the display and the displayed amplitude of some spectral lines will be too small.

START : In the SINGLE sweep mode, press and release this button to initiate a fresh sweep. In both AUTO and SINGLE modes, the pressing of this button will stop the read-in sweep at whatever point it might have reached. When the button is released a complete new sweep will be initiated and then will continue to run if the AUTO mode is being used. If it is desired to keep the picture present when this button has been operated press MANUAL before releasing START button, then switch to SINGLE if no trace editing is required.

(12) BRIGHT LINE POSITION : This 5-turn potentiometer allows the electronic cursor to be positioned anywhere across the display on the manual and SINGLE sweep modes (11).

(13) DISPLAY

A : Press this button to display signals stored in the 'A' part of the store.

B : Press this button to display signals stored in the 'B' part of the store.

HIGH DEFN : Press this button to put the store into a single recording high definition mode.

READ IN B/U : Press this button to add artificial 'persistence' to the display in order to help to identify the data renewal point on slow sweeps.

PEAK MEMORY : If this button is pressed, the store remembers the biggest signal ever to be applied at each point across the screen. This simulates infinite persistence and is useful for displaying oscillator frequency responses and for measuring fine spectral lines using the MANUAL edit mode (11).

(14) STORE : This facility allows selection of a single high definition (500 lines) stored display on HIGH DEFN or two low definition (250 lines) superimposed stored pictures arbitrarily designated A and B.

(15) VERTICAL SCALE RANGE : These three buttons allow selection of 10 dB/division (100 dB display), 1 dB/division (10 dB display) or r.m.s. volts/division. Three blue lights adjacent to the VERTICAL SCALE buttons (21) show the correct scale to read off the absolute signal level.

(16) REFERENCE FREQUENCY : Four five-turn potentiometers permit the centre frequency (or left-hand frequency - see (8)) to be set to any value between d.c. and 110 MHz.

0-110 MHz : When using the MHz/DIV (20) position of the RANGE switch, this control adjusts the reference frequency continuously over the band. When using the kHz/DIV position of the RANGE switch, this control sets the first local oscillator and hence the reference frequency to phase-locked intervals of 1 MHz in the range 0 to 110 MHz. For lowest noise and most stable operation, take care when setting this control to avoid the less stable transition areas encountered between phase-locked frequency steps. To speed up any tuning-in process, select FILTER BANDWIDTH WIDE (19) or use SWEEP SPEED x5 or x20 (18) buttons to shorten counter gate time.

±1 MHz : This control operates in exactly the same manner as the 0-110 MHz control described above except that it covers a 2 MHz range. When using the MHz/DIV (20) position of the RANGE switch the control adjusts the reference frequency continuously and acts as a fine control to the 0-110 MHz control. In the kHz/DIV (20) position it covers the 2 MHz range in 100 kHz phase locked steps and thus complements the 1 MHz settings of the 0-110 MHz control. As before, for the most stable operating point, set the control roughly midway between the two lock points, as seen on the display or counter.

±70 kHz, ±1 kHz : Operation of these controls cause continuous variation of the 2nd local oscillator to permit interpolation between the lock points of the 1st local oscillator.

PHASE LOCKING PRECAUTIONS : When switched to the kHz/DIV position of the RANGE switch a phase lock tuning system operates on the 0-110 MHz and ±1 MHz REFERENCE FREQUENCY controls.

To avoid malfunction of the system the 0-110 MHz control should be adjusted at a slow or moderate rate. If the control is operated too quickly it is possible to break phase lock. If this happens the effect will be obvious from the unstable appearance of the display and the counter readout. Locking can easily be restored by a small movement of the 0-110 MHz control.

(17) HORIZONTAL SCALE : This nine position push button switch selects sweep widths from 20 Hz/division to 10 MHz/division when used in conjunction with the RANGE (20) switch. Normally it is unnecessary to know the filter bandwidth in use at any given time, as this is automatically selected. Should the bandwidth need to be known, however, it can be read from the table above the push buttons for kHz/division and below for MHz/division; the numbers 1, 2 and 3 referring to the NARROW/NORMAL/WIDE setting of the FILTER BANDWIDTH push buttons (19).

(18) SWEEP SPEED : On all occasions, the sweep speed automatically selected is the fastest sweep possible for negligible loss of amplitude of the spectral lines. However, for tuning in, counter setting or tracking generator use, it is sometimes desired to sweep more quickly even though it causes loss of amplitude and line broadening. To this end, the x5 button is provided which increases sweep speed by approximately the value stated up to 100 ms which is the fastest input data rate permitted by the storage system. The button is spring loaded to avoid it being left in the operated, and thus uncalibrated, state. The 100 s button provides a slow sweep for use with the X-Y recorder facility.

(19) FILTER BANDWIDTH : In the NORMAL '2' position a filter of approximately 1% of the sweep width (-3 dB point) is selected on all ranges. In the NARROW '1' position a filter 10 times narrower than this is selected (where possible) and in the WIDE '3' position a filter 10 times as wide is selected (where possible). The filter bandwidth selected at any time can be read from the table either side of the HORIZONTAL SCALE push buttons - see (17) above.

(20) RANGE : The kHz/DIV and MHz/DIV buttons are multipliers for the HORIZONTAL SCALE buttons. As the first local oscillator is phase locked in the kHz/DIV position and free running in the MHz/DIV position there can be several hundred kHz shift in centre frequency between the two positions. When changing from kHz/DIV to MHz/DIV this is no problem. When changing from MHz/DIV to kHz/DIV it is suggested that this should only be done using the 0.02 MHz/DIV position (200 kHz sweep) before switching to 10 kHz/DIV position (100 kHz sweep) and using the counter readout to assist if necessary.

(21) VERTICAL SCALE : Thirteen push buttons give input sensitivities in 10 dB steps from +30 dBm to -150 dBm (300 mV r.m.s./division to 300 nV r.m.s./division on LINEAR). The gain and attenuation throughout the receiver is automatically adjusted, depending on the filter in use, such that the i.f. amplifier noise is at the bottom of the 100 dB display consistent with the first signal mixer not operating at an input level greater than -20 dBm. See Fig. 2.2 for signal levels at first signal mixer.

(22) VERTICAL SCALE : Ten push buttons give an i.f. gain change of 9 dB in 1 dB steps to interpolate between the 10 dB steps of the above scale switch. A yellow ADD light reminds the user to add the requisite number of dB to the table when in any position other than 0 dB. This switch is not calibrated for the VOLTS/DIV position of the VERTICAL SCALE RANGE switch.

(23) GAIN : Permits adjustment of i.f. amplifier gain.

(24) INPUT 50 Ω : Maximum continuous input +25 dBm (4 V r.m.s.).

(25) STANDARD 10 MHz OUTPUT : Provides a nominal square wave whose fundamental is at a level of -10 dBm when terminated in 50 Ω.

(26) TRACKING GENERATOR OUTPUT : Provides a sinusoid output at a level of -10 dBm when terminated in 50 Ω. Frequency as indicated on BRIGHT LINE (9) position of counter. The output is switched OFF by the COUNTER ON/OFF switch (10), and adjacent amber light glows.

(27) PROBE SOCKET : Provides -7.5 V output to power Zero Loss Probe TK 2374.

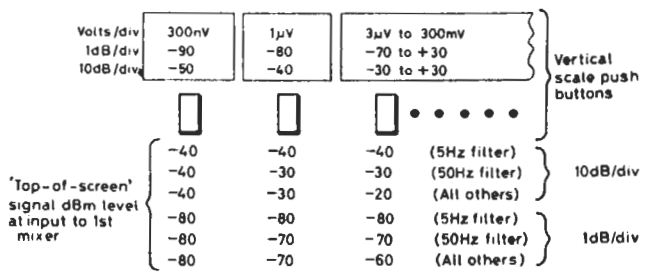


Fig. 2.2 Signal levels at input of first mixer

Rear panel

(28) EXTERNAL STANDARD : Converts an external 1 MHz standard input to a 10 MHz standard which replaces the internal 10 MHz standard.

(29) DETECTED OUTPUT : Provides audio monitoring of a.m. transmissions displayed by the instrument.

(30) SUPPLY VOLTAGE SELECTION : Bar plug selects 100 to 130 V or 200 to 250 V.

(31) SUPPLY socket : pin a.c. supply input connector.

(32) SUPPLY fuses : 2A for the 200 to 250 V range or 4 A for the 100 to 130 V range.

(33) 3 A fuses : Provide protection for the +5 V d.c. regulated lines.

(34) X-Y RECORDER socket : Provides drive for X and Y coordinates and a pen lift control by contact closure.

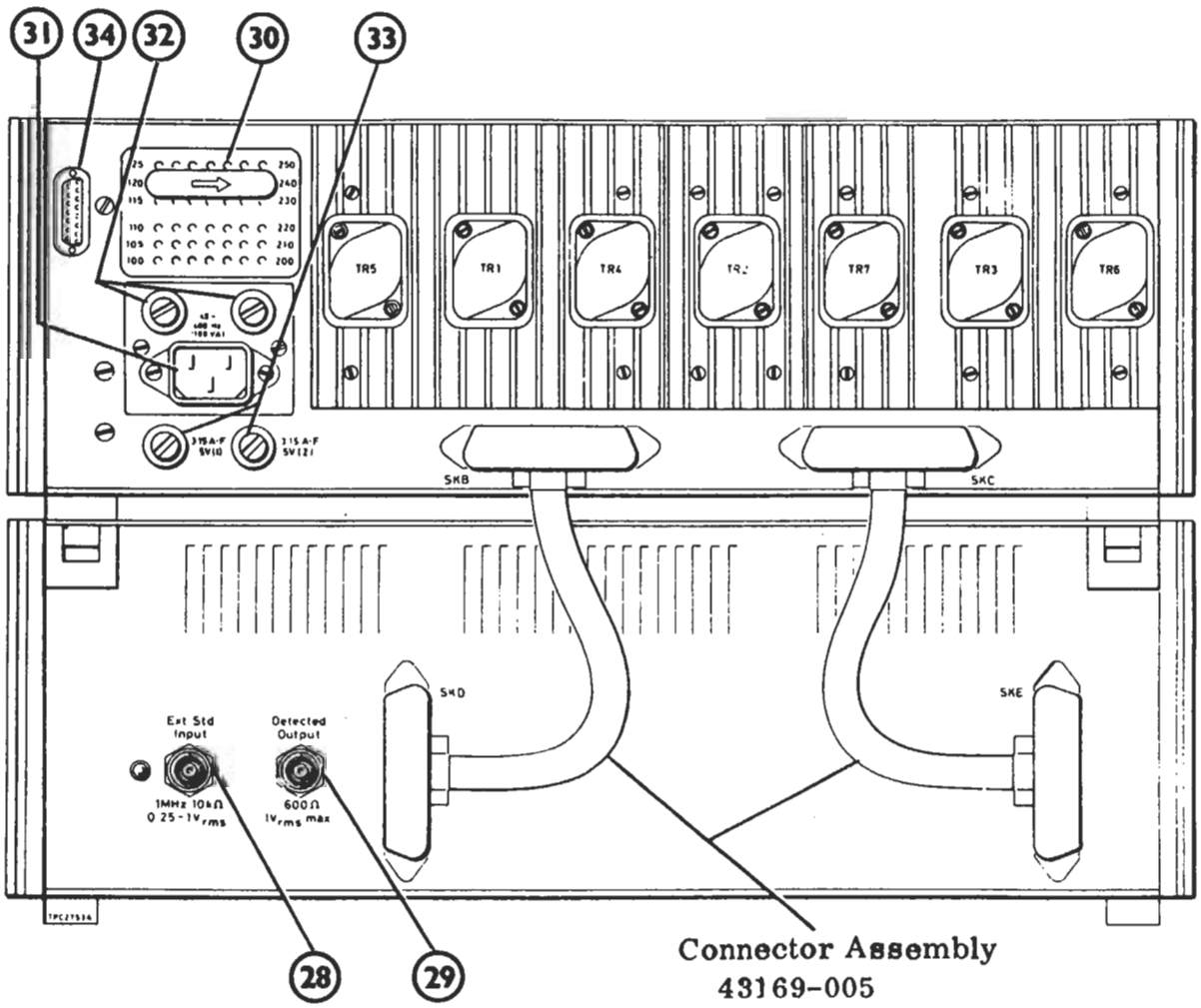


Fig. 2.3 Rear panel controls and connectors

2.3 FIRST TIME OPERATING INSTRUCTIONS

2.3.1 Obtaining a display

Switch on SUPPLY (7). After about half a minute, a display on the c.r.t. should appear. Adjust GRATICULE INTENSITY (6) as required.

Select the following push buttons :

LH	(8)
PAST CENTRE	(9)
AUTO	(11)
HIGH DEFN	(13)/(14)
10 dB/DIV	(15)
10	(17)
NORMAL '2'	(19)
MHz/DIV	(20)
0	(21)
0	(22)

All other DISPLAY buttons should be in the unpressed state.

Adjust INTENSITY DISPLAY 'A' (6) until a suitable display of noise can be seen. Using the 0-110 MHz and ±1 MHz controls (16) position the d.c. marker onto the left-hand vertical dashed line. Now connect a 50 Ω BNC cable between the STD 10 MHz OUTPUT (25) to the INPUT (24). The screen should display vertical bright lines corresponding to the 10 MHz input signal and its harmonics These will appear adjacent to every vertical cursor line as 10 MHz/division has been selected.

The height of the 10 MHz component should be 1 major division down from the top of the screen, corresponding to -10 dBm.

Press the '5', then '2', then '1' etc. buttons of the HORIZONTAL SCALE (17) and watch the sweep expand the display around the d.c. marker on the left-hand dashed line, adjusting the 0-110 MHz and ±1 MHz controls (16) as necessary. Return the HORIZONTAL SCALE button to 10.

Adjust the VERTICAL SCALE buttons (21) and (22) to become familiar with their operation and then return them to their original positions.

2.3.2 General use

Press CENTRE (8) and adjust 0-110 MHz (16) so that the 10 MHz line is positioned on the centre dashed line. As before, sequentially expand the display using the HORIZONTAL SCALE buttons (17), adjusting the 0-110 MHz, ±1 MHz and ±70 kHz controls (16) as required to keep the display on the centre line. When the '.02' button (17) has been pressed, expansion is at maximum (20 kHz/div) in the unphase-locked mode. Note the counter frequency. Switch to '10' (17) and kHz/DIV (20) and adjust the REFERENCE FREQUENCY control (16) so that the counter returns to its original number; the 10 MHz signal should then appear central again. It will be observed that in this position the 0-110 MHz control phase locks every MHz, the ±1 MHz control phase locks every 100 kHz whilst the last two controls cause continuous variation of tuning. It might be advantageous to press the x5 or 100 s SWEEP SPEED buttons (18) whilst carrying out the above adjustment.

If the above operations have been correctly executed the 10 MHz signal should be displayed at the screen centre on a sweep width of 100 kHz (10 kHz/div). As the sweep rate will now be fairly slow, it is sometimes advantageous to switch in READ IN B/U (13). This adds an artificial persistence to the display, showing clearly on the screen where the data is being renewed. The display shown is using a 500 Hz filter. If NARROW '1' (19) is now pressed, a 50 Hz filter is selected and the sweep will automatically be 100 times slower (press and release START (11) to initiate a fresh complete sweep if the switch-over is made in mid-sweep). Similarly press WIDE '3' to select the 5 kHz filter. Because of the fast sweep in this position it will probably be desirable to remove the artificial persistence by releasing the READ IN B/U button. Return the FILTER BANDWIDTH button (19) to NORMAL '2' and re-press READ IN B/U button.

2.3.3 Single shot use

Press the SINGLE (11) button. The sweep in progress will be completed and then the bright line electronic cursor will appear on the screen, the position of which may be adjusted by means of BRIGHT LINE POSITION control (12). The counter readout will be showing the centre frequency of the stored single shot. If now, the BRIGHT LINE button (9) is pressed, the counter will read the frequency corresponding to the position of the electronic cursor. Adjust the BRIGHT LINE POSITION control (12) and measure several frequency points to become familiar with the position.

Now switch to DIFFERENCE (9). The counter will now read the difference between the past centre frequency of the recorded single sweep and the current frequency of the bright line cursor. Adjust BRIGHT LINE POSITION control (12) until it is superimposed on the dashed centre graticule line. If the counter reading is not zero (±1 count) adjust either the ±70 kHz or ±1 kHz REFERENCE FREQUENCY controls (16) until the zero is established. This operation takes out any drift that may have occurred in the local oscillators since the single sweep was stored. Movement of the electronic cursor will now enable measurements of difference frequency relative to the centre frequency of the stored display to be made.

2.3.4 Manual use

Position the BRIGHT LINE POSITION control (12) so that the bright line cursor is on the left-hand side of the stored display. Now press the MANUAL button (11). As in 2.3.3, if the BRIGHT LINE counter button (9) is pressed, the counter will display the frequency corresponding to the cursor position. Unlike 2.3.3, however, the store is being refreshed at the bright line cursor point. If the cursor is now moved slowly to the right, a new recording of the input signals, as present at that moment, will be recorded on the screen. If the cursor is moved too fast, some of the original data will be left on the screen and the coherent spectral lines will be displayed at too small an amplitude due to the time constant of a 1.5 Hz video filter included for noise averaging in this mode. On some sweeps and filter combinations, the total width of a spectral response might be less than a store line width. In these cases the PEAK MEMORY button (13) should be pressed. This ensures that the store only remembers the largest input to any store location and thus does not miss spectral lines, however fine.

Note The PEAK MEMORY button must be unlatched when it is not being used.

If it is required to selectively edit the stored picture (for example either side of the 10 MHz carrier), simply press the SINGLE (11) button when it is required to move the cursor without recording new information and MANUAL (11) when it is required to record.

2.3.5 Split store mode

The controls should be set as follows :

CENTRE	(8)
PAST CENTRE	(9)
AUTO	(11)
HIGH DEFN	(13)/(14)
10 dB/DIV	(15)
10	(17)
NORMAL '2'	(19)
kHz/DIV	(20)
0	(21)
0	(22)

All other display buttons should be in the unpressed state. Using the counter as a guide, if required, adjust the REFERENCE FREQUENCY controls (16) to recentre the 10 MHz signal. Use SWEEP SPEED buttons (18) as required.

Now press '2' (17) - the display will run a little faster and be displayed at a horizontal calibration of 2 kHz/division.

Now press STORE 'A' (14) and DISPLAY 'A' (13) buttons. The same picture will be seen but at half the horizontal definition.

Now press SINGLE sweep mode button (11) - the low definition A sweep will be stored.

Now press STORE 'B' (14), DISPLAY 'B' (13) (STORE 'A' button will be released but DISPLAY 'A' button will stay in) and AUTO (11). Now the instrument is recording on the 'B' part of the store whilst simultaneously displaying the previously stored 'A' image superimposed on the current signal. Adjust 'B' DISPLAY INTENSITY (6) as required. Shift the signal using the ±70 kHz REFERENCE FREQUENCY control (16) to become familiar with the two part store. Adjust relative brightnesses of the two displays by means of the 'A' and 'B' DISPLAY controls (6).

Return the store mode buttons to normal by pressing HIGH DEFN (13), (14).

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2.3.6 Memory mode

This mode is useful if it is required to imitate the infinite persistence of a storage tube to record the frequency response of say, an oscillator. With the buttons as set, press PEAK MEMORY (13). Now if the ±70 kHz REFERENCE FREQUENCY control (16) is rotated slowly a series of recordings of each successive read-in sweep will be left on the display. The envelope of these points is the frequency response of the system. Normally, of course, the frequency that would be varying is that of the input signal. This position can be used whenever it is desired to store the largest signal ever presented to the analyser. An application of this has been described under Sect. 2.3.4 'Manual use'. To erase the screen of clutter simply release the PEAK MEMORY button (13).

2.3.7 Tracking generator use

All modes so far described also apply to this usage of the instrument. Select the sweep width required, and connect the TRACKING GEN OUTPUT (26) into the INPUT (24) having removed the previous signal lead. Select the VERTICAL SCALE (21) so that 0 dBm is at the top of the display. The signal should be displayed at a constant height of -10 dBm i.e. bright below the -10 dBm level. Store this reference level in STORE 'A' as described in Sect. 2.3.5 and then switch to STORE 'B'. Connect the 50 Ω system under test between the TRACKING GEN OUTPUT (26) and INPUT (24). The display should now show the characterization of the network under test as a frequency response with the frequency response of the spectrum analyser displayed for error correction.

When using the narrow filters, the sweep speed automatically selected may be unnecessarily slow if no comparable fine detail occurs in the network frequency response. The SWEEP SPEED buttons (18) may be used with advantage here if no loss of detail is observed as they are pressed.

2.3.8 Graticule calibration

Over any particular sweep range (before or after a single shot has been stored) the counter can be used to calibrate the frequency graticule to an accuracy of better than ±1% f.s.d. The following example will serve to illustrate the method which can, of course, be applied to any desired range.

Set the controls as follows :

SWEEP MODE (11) to SINGLE
COUNTER FREQUENCY (9) to BRIGHT LINE
HORIZONTAL SCALE (17) to '1'
RANGE (20) to MHz/DIV

Suppose it is desired to have an absolute calibration at 1 MHz/division around a centre frequency of 25 MHz :

First adjust the bright line electronic cursor to the centre dashed graticule line by means of the BRIGHT LINE POSITION control (12). Now rotate the appropriate REFERENCE FREQUENCY control (16) until the counter reads 25.00 MHz. Rotate the BRIGHT LINE POSITION control counter-clockwise until the counter reads 20.00 MHz. If the left-hand dashed graticule line is not coincident with the cursor line, rotate the HORIZONTAL GRATICULE SHIFT control clockwise away from its uncalibrated position until it is. Finally move the cursor line towards the right-hand side until the counter reads 30.00 MHz. Adjust the right-hand dashed graticule line for coincidence with the cursor using the HORIZONTAL GRATICULE GAIN control. As a check, measure each graticule line on the counter to establish sweep linearity. If an accurate frequency is now applied the absolute accuracy can be checked.

The vertical scale calibration graticule can be shifted 1.2 major divisions by means of the VERTICAL SHIFT control (2). This allows a major graticule line to be positioned against any signal of interest so that all other signals can be measured relative to it. The dashed lines on the frequency graticule serve also as group markers enabling any interval to be quickly measured viz. 20, 40, 60, 70, 73 dB instead of 10, 20, 30, 40, 50, 60, 70, 73 dB.

2.3.9 Front panel presets

VERTICAL DISPLAY GAIN (3)

Using the 10 dB/DIV (15) position a WIDE '3' FILTER BANDWIDTH (19) and 10 kHz/division sweep, apply a suitable input signal via a precision attenuator (or use the VERTICAL SCALE (21) push buttons if not available). By adjusting the input in 10 dB steps adjust the VERTICAL DISPLAY GAIN (3) preset for best fit to the top 7 or 8 divisions of the graticule. The STD 10 MHz OUTPUT signal (25) can be used for this purpose.

VERTICAL DISPLAY SHIFT (2)

This control positions the spectral display behind the graticule and should be adjusted so that consistent readings are obtained between the 1 dB/DIV and 10 dB/DIV (15) positions. This is set in conjunction with the SET GAIN preset (23) as follows :

Apply the 10 MHz calibrating signal from OUTPUT (25) to the INPUT (24). Press the 1 dB/DIV (15) button and the -10 VERTICAL SCALE (21) button. Ensure the 1 dB interval buttons (22) are at 0. Press PAST CENTRE (9) and HIGH DEFN (13), (14) and tune to 10 MHz.

Adjust the GAIN (23) preset until the top of the response is on the line at the top of the display. Now switch to 10 dB/DIV (15), '0' VERTICAL SCALE (21) and set the VERTICAL SHIFT preset (2) to bring the top of the response to the first major division from the top of the screen (-10 dBm). Repeat this adjustment as necessary.

HORIZONTAL GRATICULE SHIFT (4) AND GAIN (5)

Select the following push button positions :

CENTRE	(8)
PAST CENTRE	(9)
AUTO	(11)
10	(17)
MHz/DIV	(20)
HIGH DEFN	(13)/(14)
10 dB/DIV	(15)
0	(21)
NORMAL '2'	(19)

Set the INTENSITY 'A' control (6) fully counter-clockwise to avoid a cluttered display.

Set the counter to read 50.0 MHz by means of the 0-110 MHz and ±1 MHz (16) controls. Switch to SINGLE (11) and BRIGHT LINE (9). Press LH (8) and adjust the BRIGHT LINE POSITION control (12) so that the counter again reads 50.0 MHz.

Adjust the preset SHIFT control (4) (with the main control in its calibrated position) so that the left-hand dashed graticule line coincides with the electronic cursor.

Now press CENTRE (8) button and readjust the BRIGHT LINE POSITION control (12) so that the counter reads 50.0 MHz again. Adjust the preset GAIN control (5) (with the main control in its calibrated position) so that the centre dashed line coincides with the electronic cursor.

2.3.10 Ancillary facilities

DETECTED OUTPUT (at rear of instrument)

The controls should be set as follows :

CENTRE	(8)
PAST CENTRE	(9)
AUTO	(11)
HIGH DEFN	(13)/(14)
10 dB/DIV	(15)
10	(17)
NORMAL	(19)
MHz/DIV	(20)
0	(21)
0	(22)

All other DISPLAY buttons should be in the unpressed state.

Apply a signal, amplitude modulated at 1 to 10 kHz, to the INPUT (24). Adjust the REFERENCE FREQUENCY controls (16) to centre the signal. Expand the frequency scale using the HORIZONTAL SCALE (17) buttons, recentring the display as necessary, until a dispersion of 0.02 MHz/div. is reached. Select a NARROW (19) filter so that the carrier and sidebands are separately resolvable. Adjust the VERTICAL SCALE (21), (22) buttons until the carrier is 40 dB down from the top of the display. Press MANUAL (11) and WIDE (19) filter, and tune using the BRIGHT LINE POSITION control (12). The brightened-up portion of the electronic cursor should be adjusted to maximum (-34 to -40 dB from the top of the display depending on the modulation depth). The detected output socket at the rear of the instrument will now carry the demodulated signal at 0 dB into 600 Ω for 100% modulation or proportionately less for smaller modulation depths.

Experiment with different modulation frequencies and filter bandwidths using the kHz/DIV (20), HORIZONTAL SCALE (17), REFERENCE FREQUENCY (16) and FILTER BANDWIDTH (19) controls as appropriate. At all times keep the displayed signal at approximately 40 dB down from the top of the display (10 dB/div.) or at the top of the display (1 dB/div.) for maximum undistorted detected output.

FM signals may be detected for identification purposes by tuning the signal down the skirt of the filter appropriate to the deviation of the signal.

EXTERNAL STANDARD INPUT

To use this facility, apply a 1 MHz ±0.1 Hz signal, at between 0.25 V and 1 V r.m.s., to the appropriate rear BNC socket. A green light will glow to indicate that the external signal has replaced the internal standard.

To check the correct functioning, connect the STANDARD 10 MHz OUTPUT (25) to one channel of a dual trace oscilloscope, and the external standard signal to the other channel. If the oscilloscope is triggered by the 1 MHz external standard, the internal 10 MHz signal will drift across the oscilloscope screen due to the frequency error between the two standards. If the external signal is also fed to the external standard input socket (rear panel) the drift of the 10 MHz signal will cease showing that the 10 MHz standard is now in phase with the external 1 MHz standard.

X-Y RECORDER

Signals for an X-Y recorder drive are provided on rear panel socket SKR at the following pins :-

	Pin No.
X output	10
Y output	11
Pen-lift relay contacts	3
	2
Relay coil	9
Earth	1

(1) When the pen-lift facility is required it is necessary to link pin 9 to pin 1 so as to energize the relay drive circuit. Pins 2 and 3 then present a pair of electrically isolated contacts which are made during the sweep.

Note To prolong relay contact life the link between pins 9 and 1 should be removed when pen-lift is not required.

(2) Make connection to the recorder via the 15-way mating plug supplied with the instrument.

(3) Select SWEEP SPEED 100 s when using a recorder.

2.4 USEFUL PROCEDURES

2.4.1 Sweep width

If the frequency of the input signal is not accurately known, the method of starting with a wide sweep and successively narrowing the sweep around the signal must be used. However, if the signal frequency is known, for example within ±1 kHz, the following method enables a narrow sweep of the signal to be directly obtained.

Set the controls as follows :

CENTRE	(8)
BRIGHT LINE	(9)
MAN	(11)
10 dB/DIV	(15)
HIGH DEFN	(13)/(14)
BRIGHT LINE POSITION	(12) to position electronic cursor on centre dashed line
0.2	(17)
kHz/DIV	(20)
WIDE	(19)
REFERENCE FREQUENCY	(16) to approximately centre the ±70 kHz and ±1 kHz controls

Using the REFERENCE FREQUENCY (16) adjust the 0-110 MHz control and obtain a counter readout to the nearest MHz of the input signal. Set the ±1 MHz control to the nearest 100 kHz increment, and then tune the ±70 kHz and ±1 kHz controls to the exact frequency required.

Select the NORMAL (19) and AUTO (11) buttons. A sweep covering ±1 kHz around the input signal, together with the input signal, should be displayed. The VERTICAL SCALE (21) buttons may now be adjusted as required.

By re-centring the input signal with the ±70 kHz controls (16), the frequency scan may be further narrowed to 20 Hz/div. using the SWEEP SPEED (18) buttons or the WIDE (19) button to speed the process.

Note If during this procedure the signal trace disappears, check the counter with MAN (11) and WIDE (19) buttons. If the counter is exactly 1 MHz or 100 kHz in error, the phase locking

system will have jumped to an adjacent lock position, and the REFERENCE FREQUENCY controls (16) should be adjusted. The 0-110 MHz control will correct a 1 MHz error, and the ±1 MHz control corrects a 100 kHz error.

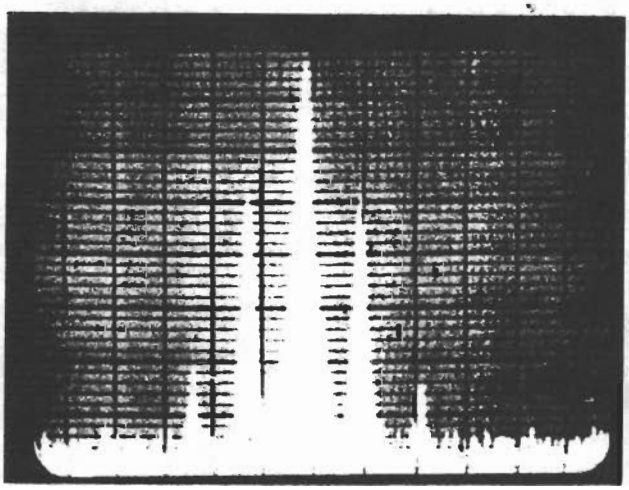
2.4.2 Spectral line frequency

To measure the frequency of any of the displayed spectral lines accurately, press SINGLE (11) button and wait for completion of the scan. Then superimpose the electronic cursor onto the required spectral line using the BRIGHT LINE POSITION control (12), and read the counter frequency. For the greatest possible accuracy, press MAN (11) button and adjust the electronic cursor to give a peak value on the required response, and read the counter while maintaining this condition.

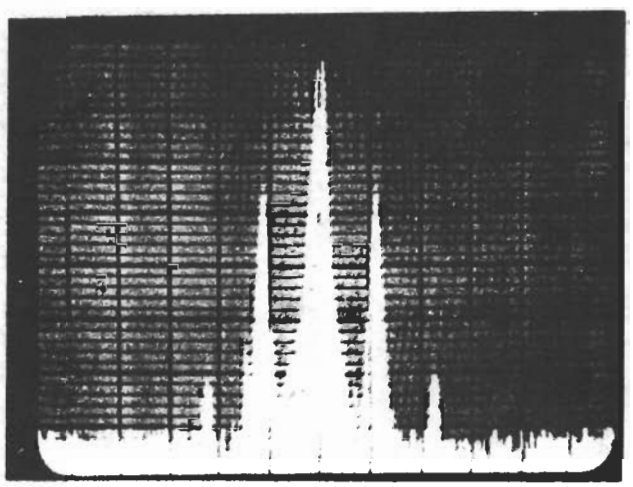
2.5 APPLICATION NOTES

The electronically produced graticule is superimposed on the raster, and may be shifted vertically, and/or horizontally shifted and scaled before or after an image is stored, see Fig. 2.4.

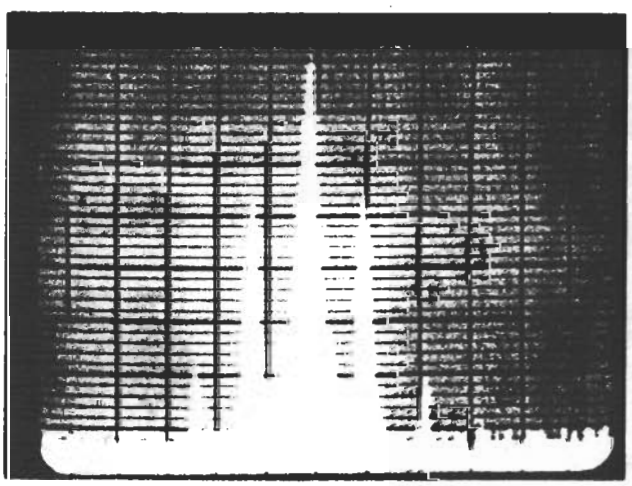
Fig. 2.4(a) shows a single shot recording of a 50 MHz carrier with 500 Hz f.m. sidebands using a 50 Hz filter. This recording took 20 seconds. In general, such a recording will not be ideally positioned with respect to the graticule. With a fixed graticule, several 20 second recordings would have to be taken before precise alignment is achieved. With the electronic graticule only one single shot recording is required. This is because the graticule can be shifted vertically to make relative carrier sideband ratios easy to read (Fig. 2.4(b)), shifted horizontally to centre on the carrier (Fig. 2.4(c)), and horizontally scaled against the internal counter to give an exact frequency calibration (Fig. 2.4(d)).



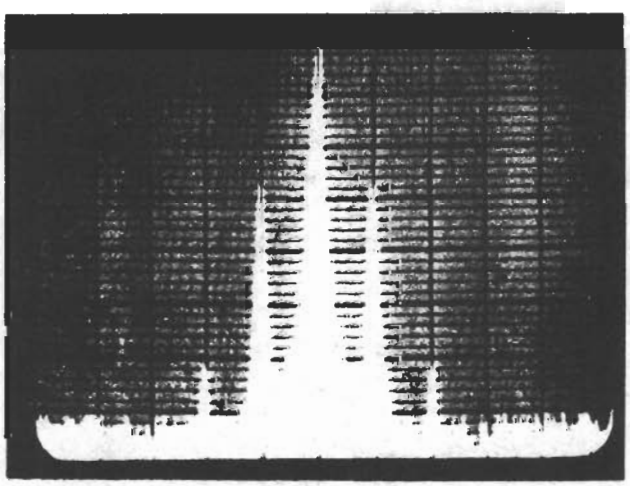
(a) Display before horizontal and vertical alignment of graticule



(c) Horizontal calibration scale centred on carrier

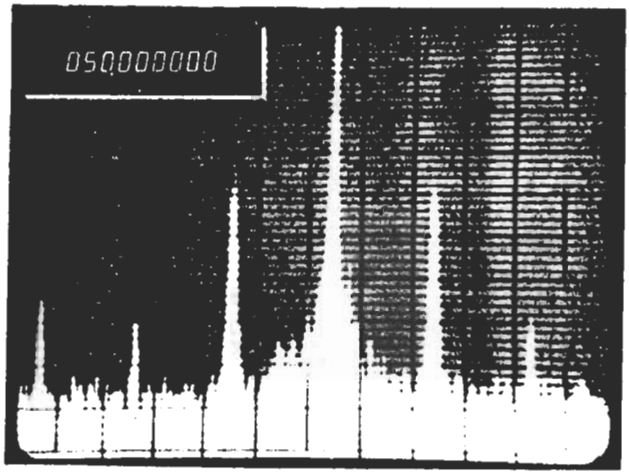


(b) Vertical calibration scale aligned with carrier level

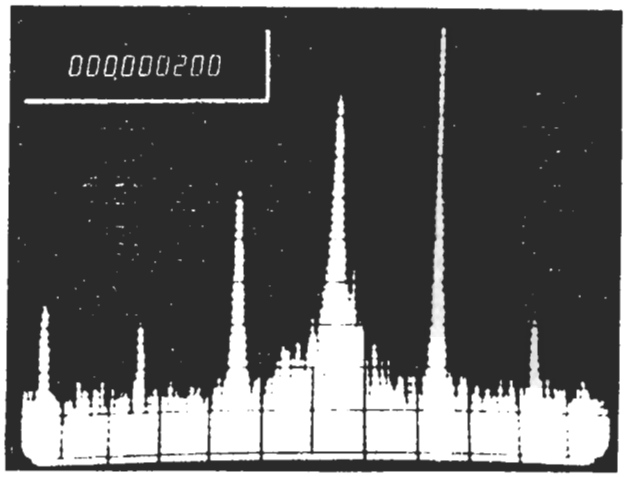


(d) Horizontal calibration scale adjusted against counter readout for exact frequency intervals

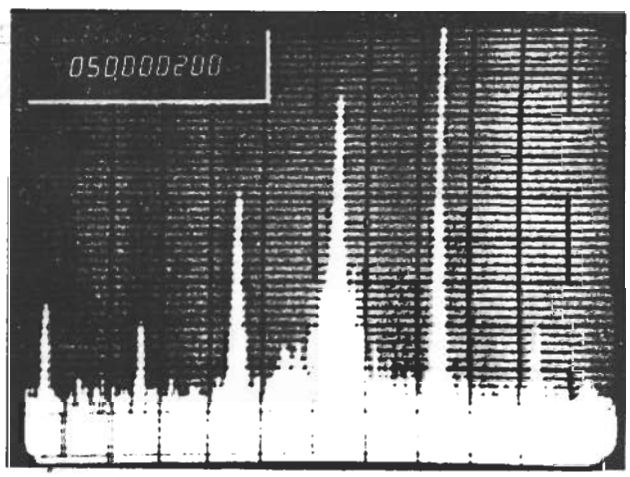
Fig. 2.4 Single shot record of 50 MHz carrier with 500 Hz f.m. sidebands using the 50 Hz filter. Scales: 500 Hz/div., 10 dB/div.



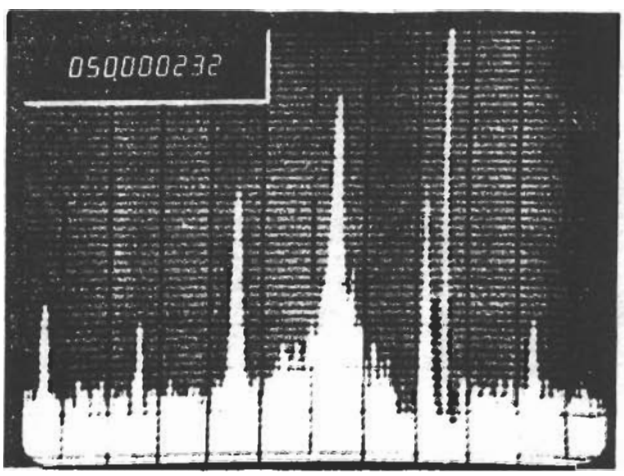
(a) *Counter measures carrier frequency using bright line cursor*



(c) *Counter measures difference frequency between carrier and first upper sideband*



(b) *Counter measures first upper sideband*



(d) *Bright line cursor used as edit pointer to manually refresh display around first upper sideband*

Fig. 2.5 Methods of frequency measurement using the counter. Scale 100 Hz/div., 10 dB/div.

After any single sweep recording a bright line electronic cursor is available to be positioned anywhere across the screen so that the frequency at that point may be measured by the internal counter. The COUNTER READOUT will display either the absolute frequency at that point or the difference frequency between the bright line value, and the centre of screen value of the stored display, see Fig. 2.5.

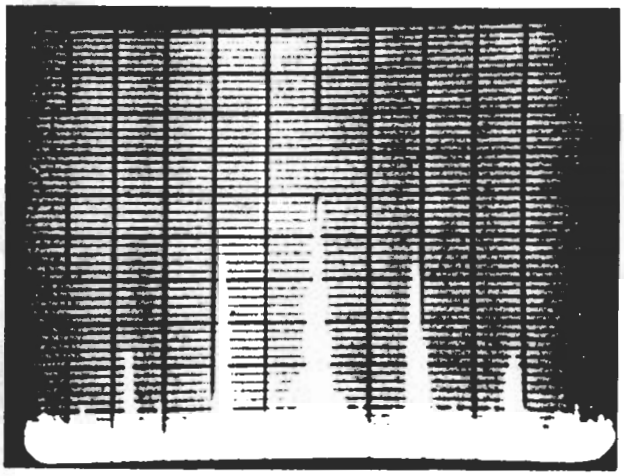
In the MANUAL mode of the store, the electronic cursor becomes an edit pointer enabling the display around any points of interest to be selectively updated (Fig. 2.5(d)). In this mode the instrument behaves as a selective level measuring set.

To enable two recorded displays to be superimposed, the digital store is used in two parts designated A and B. Fig. 2.6 shows the received signal from the BBC FM Station at Wrotham, with the carrier at 93.5 MHz and the stereo pilot tones at 19 kHz away. Fig. 2.6(a) shows the signal during a quiet passage. Fig. 2.6(b) shows a typical speech spectrum, and Fig. 2.6(c) shows how the two displays can be superimposed for comparison.

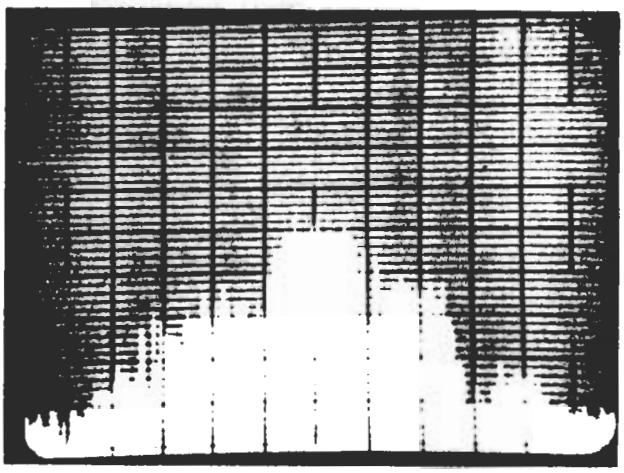
The persistence of the image on a storage tube display must be adjusted so that the decay rate is roughly comparable to the sweep speed, otherwise flickering or cluttered displays result. With the digital store, the persistence is infinite until renewed by the new sweep when it becomes zero. Read-in bright-up may be added as required to help identify old and new data when using slow sweeps (Fig. 2.7).

TWO-TONE TESTING

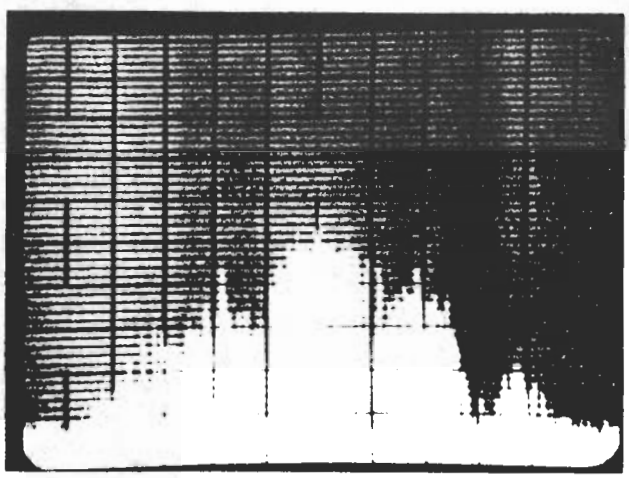
When using two equal-level tones for intermodulation testing it is important to ensure that the level of each tone is no higher than -40 dBm at the input of the first mixer. In practice this



(a) *Signal with stereo pilot tones at 19 kHz during a quiet passage. Display stored in A store*



(b) *Typical speech spectrum obscuring the pilot tones. Display stored in B store*



(c) *A and B stores displayed simultaneously thus allowing Figs. 3(a) and 3(b) spectra to be superimposed*

Fig. 2.6 Received signal of BBC FM Station at 93.5 MHz. Scales 10 kHz/div., 10 dB/div.

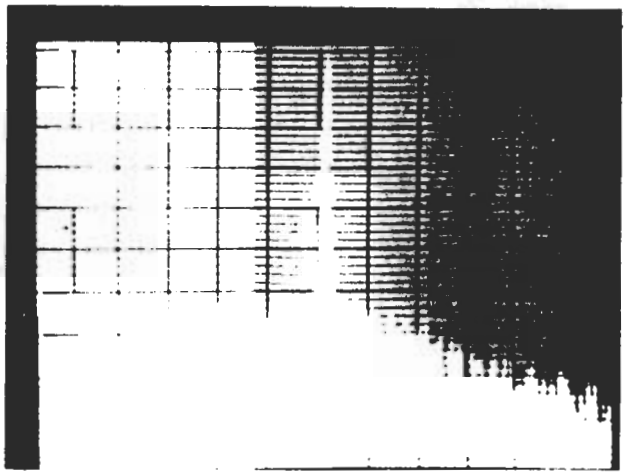


Fig. 2.7 Slow sweep in progress with the data renewal region identified by the read-in bright-up. Scales: 200 Hz/div., 10 dB/div.

means restricting the level of the displayed tones to -20 dB relative to the top of the screen except when using the narrowest (5 Hz) filter bandwidth and/or the most sensitive (-50 dBm) vertical scale, in which case the tones can be increased to the top of the screen.

Even with a tone level of -20 dB an adequate dynamic range is available for most intermodulation distortion measurements. However, tone levels intermediate between -20 dB and the top of the screen may be used at various combinations of filter bandwidth and vertical sensitivity - see Fig. 2.2 and the calibration table on Fig. 7.7.

DISTORTION MEASUREMENT

When measuring low levels of non-linear distortion the signal level at the input of the first mixer must not exceed -40 dBm, otherwise the 'spurious responses' performance quoted in the Data Summary may not be realized.

The signal level at the mixer depends on the settings of the VERTICAL SCALE, VERTICAL SCALE RANGE and FILTER BANDWIDTH as shown in Fig. 2.2. Where the combination of settings produces a figure higher than -40 dBm, i.e. -30 or -20 dBm, the signal level at the analyser INPUT socket must be reduced by a corresponding amount, i.e. by 10 or 20 dB.

BROAD BAND NOISE MEASUREMENT

When measuring broad band noise the analyser should only be used in the MANUAL sweep mode. The correct relationship between displayed level and bandwidth is only obtained on the 3 narrowest filter positions and for this reason the 5 and 50 kHz filters should not be used. To obtain the equivalent noise bandwidth of the recommended filters their 3 dB bandwidth should be multiplied by 1.06.

Chapter 3

Technical description

3.1 SYSTEM OPERATION

In this section the overall operation of TF 2370 is explained with reference to block diagrams Fig. 3.1 to Fig. 3.9.

3.1.1 Digital display

A m.o.s. f.e.t. recirculatory digital store is used.

The detected output from the receiver section is analogue to digital converted to form a 256 level by 512 ordinate representation of the display area. This stored information is continuously displayed on a bright 130 x 100 mm camera viewfinder tube at a flicker free rate of 76 Hz as a brightness modulated vertically scanned raster. Superimposed on this raster is an electronically produced graticule which may be shifted vertically, and/or horizontally shifted and scaled before or after an image is stored.

The electronic graticule can be shifted vertically to make relative carrier/sideband ratios easy to read, shifted horizontally to centre on the carrier, and horizontally scaled against the internal counter to give an exact frequency calibration.

After any single sweep recording a bright line electronic cursor is available to be positioned anywhere across the screen so that the frequency at that point may be measured on the internal counter to a resolution down to 2 Hz. The counter readout will display either the absolute frequency at that point or the difference frequency between the bright line value and the centre of screen value of the stored display.

In the manual mode of the store, the electronic cursor becomes an edit pointer enabling the user to selectively update the display around any points of interest. In this mode the instrument behaves as a recording selective level measuring set.

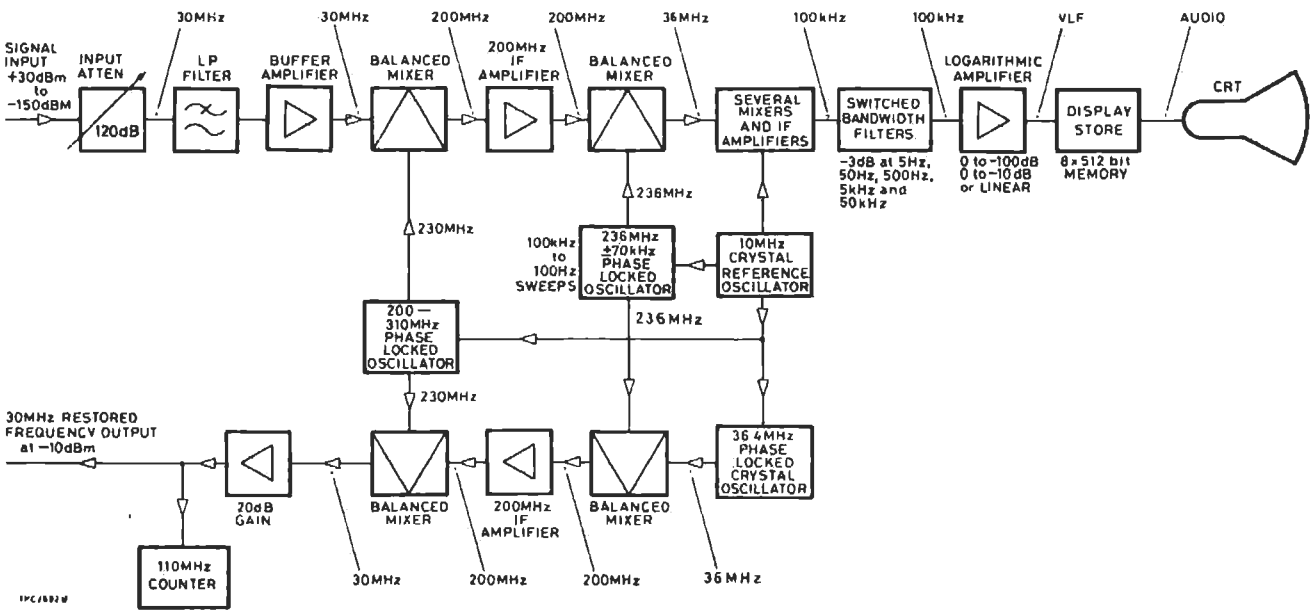


Fig. 3.1 Simplified overall impression of TF 2370

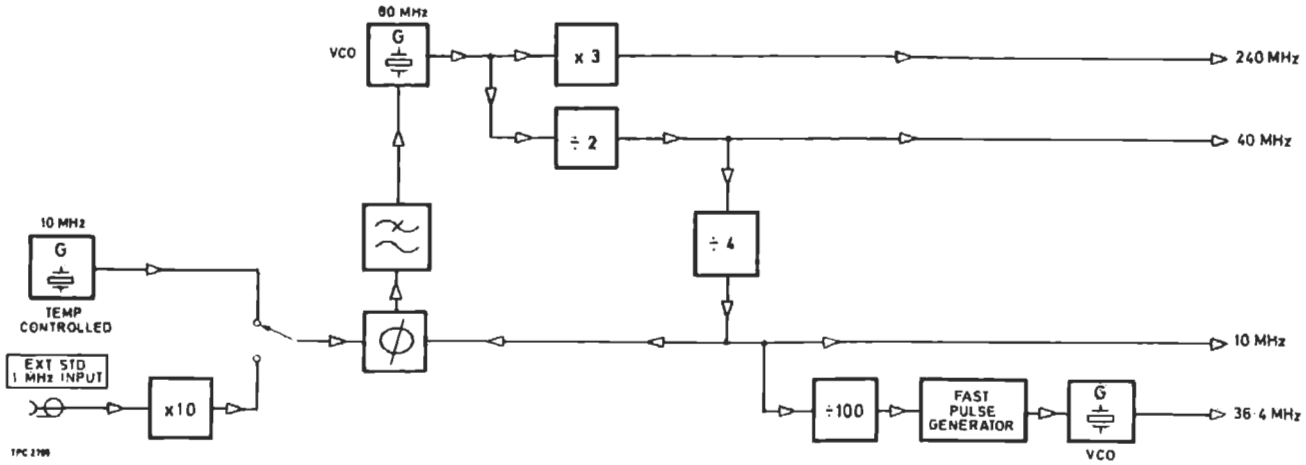


Fig. 3.2 Block diagram of the fixed oscillator system

To enable two recorded displays to be superimposed, the digital store is used in two parts, each of 256 lines arbitrarily designated 'A' and 'B'.

The persistence is infinite until renewed by the new sweep when it becomes zero. Read in bright-up may be added as required to help identify old and new data when using slow sweeps.

In most cases, the complete erasure of the old image is ideal. However, there are some uses where the old image is required to be kept, simulating infinite persistence. Such applications might be for checking the frequency response or drift rate of an oscillator. Selection of the peak memory button on the display unit puts the store into this mode.

3.1.2 Timing system

Fig. 3.2 shows a block diagram of the fixed oscillator system.

An 80 MHz varactor controlled crystal oscillator produces a pure high level signal. This is multiplied by 3 to produce a reference frequency for the second local oscillator, and divided by 2 to produce a 40 MHz drive for the fixed i.f. chain. It is further divided by 4 to produce 10 MHz, then compared in a phase detector with the 10 MHz signal from a temperature compensated crystal oscillator, which is operated at low level to achieve a stable frequency.

The output from the phase discriminator is passed through the low-pass filter to control the 80 MHz oscillator. The 10 MHz signal is finally divided by 100 to produce a 100 kHz signal which drives a fast pulse generator producing a 100 kHz comb. A 36.4 MHz varactor controlled crystal oscillator is phase locked to the 364th harmonic of this to produce a coherent source for the tracking generator signal.

A facility is also provided for the system to be locked to an external reference frequency standard at 1 MHz. If this is used, the counter accuracy will be as good as the standard ±2 Hz.

Fig. 3.3 shows the receiver front end and tracking generator schematic. The input signal is fed via a programmable attenuator to an a.c. coupled amplifier which permits the attenuator to be correctly matched into 50 Ω. This gives good v.s.w.r. performance at zero input attenuation and a low frequency 3 dB point of < 30 Hz. Additionally it lessens the noise contribution of the front end circuitry.

The first local oscillator driving the double balanced ring bridge mixer up-converts the input signals to an i.f. of 200.2 MHz, whilst the second local oscillator down-converts to the second i.f. of 36.4 MHz.

The first oscillator is a varactor controlled system of phase locked loops giving an output drive which is either in discrete steps of 1 MHz and 100 kHz on narrow sweeps, or continuously swept on ranges of 20 kHz/div. and wider. The second local oscillator at 236.6 MHz has a range of ±150 kHz which is used for sweeps of 10 kHz/div. or less, and permits fine tuning when the first local oscillator is phase locked.

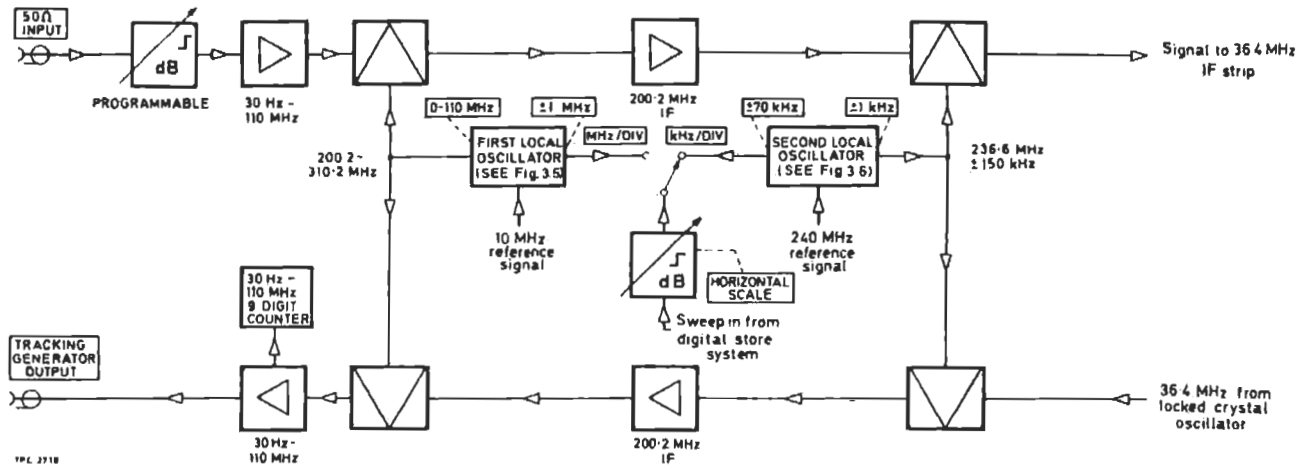


Fig. 3.3 Block diagram of receiver front end and tracking generator

Each oscillator has its own diode shaper network to produce a linear voltage/frequency relationship. The tuning controls are summed with the attenuated sweep which, in turn, is obtained from an integrated digital to analogue converter in the digital store.

3.1.3 Tracking generator

The tracking generator output signal is produced by taking the previously generated 36.4 MHz signal (Fig. 3.3) and reverse processing the signal with the second and first local oscillators.

The signal level is kept low through the mixers and 200.2 MHz i.f. to minimize leakage through the common signal paths to the first and second local oscillators. As the signal sensitivity in the 200.2 MHz i.f. mixer region can be as great as -140 dBm, the total isolation due to the buffer and mixers must be in excess of 115 dB over the range 0 to 110 MHz and at 200 MHz. Similar isolation levels are required between first and second local oscillators. As a result, all these units are formed of discrete circuits in screened boxes.

The tracking generator output amplifier feeds a signal to the front panel at a level of -10 dBm and also a signal to the counter.

3.1.4 Fixed i.f. chain

Fig. 3.4 shows the arrangement of the fixed i.f's.

Because a high degree of mirror channel rejection is required, the ratio of successive i.f's is chosen to be 10:1 or less. To avoid harmonic beats and spurious inter-modulation products between the several i.f's, the oscillator drives to the mixers are harmonically related. This has been achieved by simple division from the 40 MHz reference frequency. The square wave drive from integrated circuit dividers form ideal drives for the double balanced ring bridge mixers, and ensure that the last three mixers negligibly worsen the inter-modulation products produced in the first and second mixers.

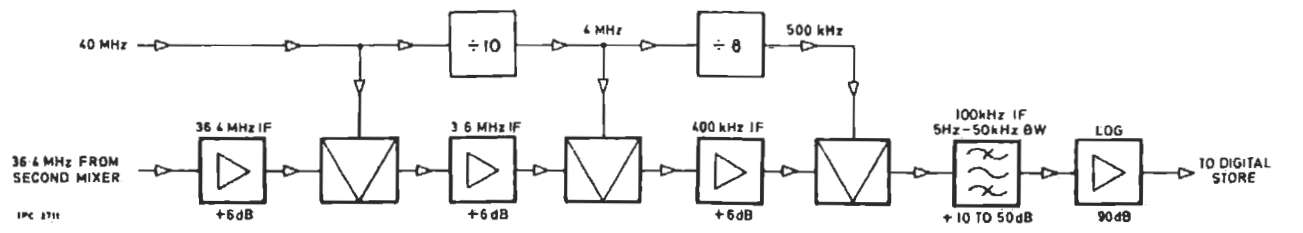


Fig. 3.4 Block diagram of the fixed i.f. chain, switched filters and logarithmic amplifier

The final i.f. is at 100 kHz. It is at this frequency that the switched filtering and logarithmic shaping is performed. The 5 Hz and 50 Hz filters are of the crystal type whilst the 500 Hz, 5 kHz and 50 kHz filters are LC type.

The method of making the 'oscillator' drives to the fixed i.f. chain phase coherent by means of digital dividers is extended to cover most other circuit areas. For instance, the 10 MHz standard signal controls all the counter circuitry and the digital store takes this signal to derive its clock frequency. This in turn produces the c.r.t. line scan rate of 19.532 kHz by direct division which is also used to drive the e.h.t. unit. Thus any interfering signals from these sources are crystal controlled.

The logarithmic amplifier is of the successive limiting gain blocks type, each block being current summed to give a segmented approximation to a logarithmic law.

Two functions are performed. One comprises ten gain blocks summed to give a 100 dB range with a law accuracy of ±1 dB whilst the other is produced from four 2.5 dB gain blocks giving a 10 dB range with a law accuracy of ±0.1 dB. A linear output position is also included. The detected signal from the logarithmic amplifier is passed to the digital store circuitry.

3.1.5 Variable oscillator system

First local oscillator

The first local oscillator is required to sweep between approximately 200 and 300 MHz for a voltage change of 10 V, which is the sweep drive provided by the circuitry associated with the digital store.

The schematic diagram of the first local oscillator system is shown in Fig. 3.5.

The system consists of three variable oscillators. The first is tuned over the range of 200 to 310 MHz nominal frequency and is always phase locked. This oscillator provides the drive for the first input mixer and the tracking generator output mixer, and is called the slave first local oscillator. A similar oscillator tuned over the range 205 to 315 MHz nominal is the master first local oscillator. A third oscillator always phase locked at intervals of 100 kHz, tuned ±1 MHz about 4.8 MHz, provides a variable offset between the master and slave.

Although the slave receives a sweep drive via the shaper circuit as does the master, this is only to set it approximately on the desired frequency. The precise frequency is set by phase locking it to the difference between the master and 4.8 MHz oscillators.

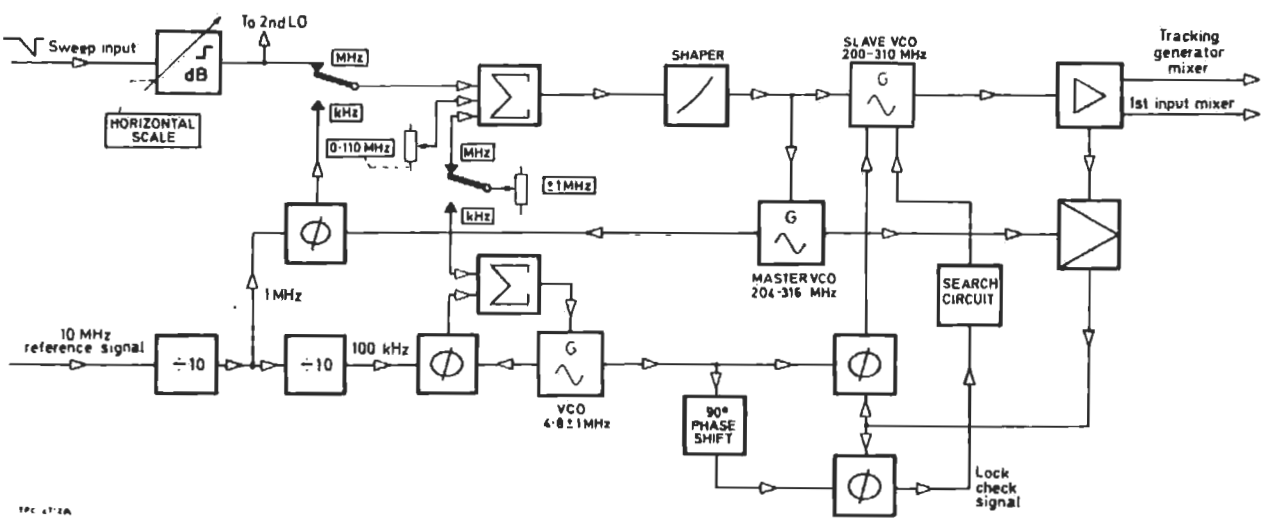


Fig. 3.5 Block diagram of first local oscillator system

Contents

REFRESH 'B' : In this mode, DISPLAY 'B' is continuously refreshed as in HIGH DEFN, DISPLAY 'A' is permanently stored.

READ IN B/U : Display 'Bright-up' indicates the data renewal point on the display.

PEAK MEM : The peak signal level of a spectrum (whose level may be changing) is stored and displayed.

CRT : Camera viewfinder tube with 100 x 130 mm viewing area.

Intensity 'A' : Controls brightness of display on HIGH DEFN and DISPLAY 'A' modes of operation.

Intensity 'B' : Controls brightness of display on DISPLAY 'B' mode of operation.

Vertical gain : Provides preset adjustment of the display amplitude.

Vertical shift : Provides preset adjustment of the display position.

Graticule Nominal 1 cm vertical calibration lines and 1 cm horizontal calibration lines sub-divided to 2 mm, are electronically displayed on the c.r.t.

Horizontal gain : Enables the electronic graticule to be expanded. Cover greater than ±15%. An indicator lamp shows when the control is being operated in the uncalibrated position.

Horizontal shift : Enables the electronic graticule to be positioned over at least ±1.5 major divisions. An indicator lamp shows when the control is being operated in the uncalibrated position.

Vertical shift : Enables the electronic graticule to be positioned over at least 1 major division. An indicator lamp shows when the control is being operated in the uncalibrated position.

Intensity : Controls background brightness of the electronic graticule.

External standard input Rear BNC socket permits internal 10 MHz standard to be locked to external 1 MHz standard. Green light next to socket glows when adequate signal is applied at the correct frequency to achieve satisfactory lock.

Input impedance : Approx. 10 kΩ shunted by 100 pF.

Signal level required : 0.25 V to 1.0 V r.m.s.

Frequency : 1 MHz.

Accuracy required : Better than 1 in 10^7.

Detected output Rear panel BNC socket provides demodulated output.

Output impedance : Approx. 600 Ω.

Frequency response : -3 dB at less than 30 Hz to greater than 20 kHz using 50 kHz filter, relative to level at 1 kHz.

The differential action of TR9, TR10 helps balance out hum on the +14 V, -14 V lines, reducing the level of hum applied to varactor diodes D1 and D2 on AB3. Potentiometer R42, whose attenuated output is taken to the base of TR10, allows a d.c. preset bias to be applied across varactor diodes D1 and D2 on AB3.

10 MHz output of IC1b, pin 15, is applied to emitter followers TR4 and TR5. The output of TR5 drives three parallel 10 MHz output stages, TR6, TR7 and TR8.

The first 10 MHz signal is routed to potentiometer R30 in the emitter circuit of TR6. Output of TR6 is fed via pin 10 to the front panel standard 10 MHz socket. The output level at the socket is -10 dBm when terminated with 50 Ω, and is set by R30.

A second signal from TR5 is fed via C18 to the emitter of TR7. Output of TR7 is taken via pin 12 to AE3. This 10 MHz signal is used, after being divided by four, as the clock drive for the digital store.

The third output of TR5 is routed via C21 to the emitter of TR8. The output of this buffer is taken via pin 14 to AA2, and used to produce a comb for the phase locking of the first local oscillator.

3.8 FIXED OSCILLATOR DIVIDER CHAIN —AB2

Circuit diagram— Fig. 7.9
Block diagram—Fig. 3.10

40 MHz output of AB3 is taken to IC1a via pin 6. IC1a divides the signal by 5, and IC1b further divides the signal by 2.

The 4 MHz signal at pin 15, IC1b, is applied to emitter follower TR1. The output of TR1 is fed to the base of amplifier TR3. The amplifier produces an output which passes via pin 7 to AB7 as the 4 MHz mixer drive. C20 reduces the high frequency components of the 4 MHz square wave output.

A second output of TR1 is applied to the base of TR2, which amplifies the 4 MHz signal to sufficient level to operate IC2. IC2 divides the signal by eight, producing 500 kHz. This signal is passed via NAND gates IC4b and IC4c to amplifier TR4. The output of TR4 is taken via pin 9 to AB6 to be used as a local oscillator drive.

A further input to IC4c turns off the 500 kHz output to the i.f. mixer during T time. The T time input is taken via pin 13.

T time suppression of the 500 kHz local oscillator output during flyback open circuits the i.f. path. This avoids any spurious response at the start of scan due to the filter memory of a previous response.

Diode D1 clips the top of the 500 kHz square wave output of IC4c to remove any residual modulation.

A second output of IC2 is passed via NAND gate IC4a to IC3. IC4a acts as a buffer to prevent signals from IC3 appearing on the output of IC2. IC3 divides the 500 kHz signal down to 100 kHz, and the output is taken via pin 11 to AB1.

3.9 36.4 MHz CRYSTAL OSCILLATOR—AB1

Circuit diagram— Fig. 7.9
Block diagram—Fig. 3.10

The 100 kHz square wave output of AB2 is passed to amplifier TR1 via pin 2. TR1 output is tuned to 36.4 MHz by L1 and C5. TR2, whose collector is tuned to 36.4 MHz, further amplifies the signal, and a comb of 100 kHz signals about 36.4 MHz is produced at its collector. This output is tapped at L2, and fed to T2 which is part of a ring bridge, used as a phase comparator. The signal is compared with output of 36.4 MHz phase locked crystal oscillator TR3.

TR3 output is amplified by TR4, TR5 and provides drive to the phase comparator IC1. The d.c. output of the phase comparator is amplified by IC2 and applied to D1 via R8 to control the oscillator frequency. Potentiometer R30 optimizes the d.c. bias in the phase locked loop.

Diodes D2, D3 and D4 form a clamp circuit which prevents the phase locked loop going into a locked state during switch on.

TR3 is tuned by C12, C14, C15, inductor L3, varactor diode D1 and crystal XL1.

An additional output at 36.4 MHz is taken from TR5 via R23, attenuator pad R24, R34 and R35, and isolating transformer T3. The signal passes via pins 7 and 8 to AC1. The output level of this 'tracking generator reference' signal is adjusted by variable resistor R23.

Chapter 4 MAINTENANCE

Chapter 5 REPAIR

Chapter 6 REPLACEABLE PARTS

Chapter 7 CIRCUIT DIAGRAMS

Notes (1) Panel markings are shown throughout this manual in capital letters.

(2) References to board codes AE1, AF2, AG2, etc., should be taken to include versions AE1(A), AF2(A), AG2(B) etc.

Chapter 1

General information

1.1 INTRODUCTION

TF 2370 is a spectrum analyser/tracking signal generator/counter covering the range 30 Hz to 110 MHz in sweep widths varying from 200 Hz to 100 MHz and with resolutions varying from 50 kHz to 5 Hz. The user selects input sensitivity, sweep width, centre frequency and filter resolution and a wired logic programme selects best r.f./i.f. gain ratio, sweep rate and filter bandwidth.

One of the disadvantages of high resolution swept-filter type spectrum analysers is the long sweep times necessary to scan the required frequency band. In TF 2370 the longest sweep time is 100 seconds. To enable the data scanned during this time to be clearly presented and subsequently analysed, a digital store, consisting of a 256 x 512 bit m.o.s. f.e.t. dynamic shift register, records the processed signal from the wide range logarithmic amplifier and displays this stored data at a flicker free 70 Hz rate on a bright 13 x 10 cm camera monitor cathode ray tube. Superimposed on this display is an electronic graticule which may be moved in both vertical and horizontal directions to facilitate accurate measurements. The stored display of a single shot scan can be measured in frequency to counter accuracy by positioning an electronic cursor in the desired position. Additionally the electronic cursor can be used to manually edit or update the stored image or can be used as a meter, thus providing the facilities of a selective level test set.

The instrument is constructed in two halves, an upper display unit, and a lower r.f. unit, which are connected at the rear by two connector assemblies.

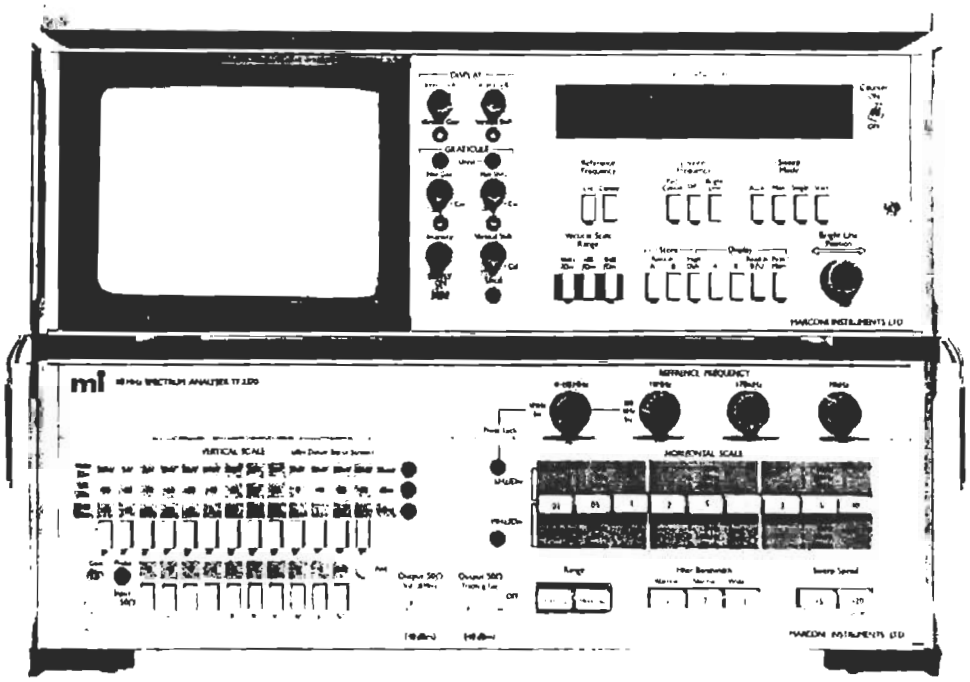


Fig. 1.1 110 MHz Spectrum Analyser TF 2370

1.2 DATA SUMMARY

Amplitude measurement

Input impedance :	50 Ω (BNC type socket).
Input v.s.w.r. :	Less than 1.2 : 1.
Maximum input :	+30 dBm for five minutes (7.1 V r.m.s.). +25 dBm continuous (4 V r.m.s.).
Vertical scale range :	+30 to -159 dBm at 10 dB/div. (1 div. = approx. 1 cm). +30 to -109 dBm at 1 dB/div.
Vertical scale display :	Log : 10 dB/div. for a 100 dB full screen display. 1 dB/div. for a 10 dB full screen display. Linear : 300 mV/div. to 300 nV/div. in a 1, 3, 10 sequence on a 10 division display.
Frequency response : (relative to 10 MHz level)	±1 dB from 100 Hz to 110 MHz. -3 dB at less than 30 Hz.
Gain :	Preset control for adjustment of vertical scale display.
Vertical scale range accuracy :	10 dB steps : ±0.3 dB/10 dB; cumulative error less than ±1.5 dB. 1 dB steps : ±0.1 dB/1 dB; cumulative error less than ±0.3 dB.
Vertical scale display accuracy :	Log : 10 dB/div. Overall law accuracy 0 to -80 dB, ±1 dB; -80 to 100 dB, ±1.5 dB. 1 dB/div. Overall law accuracy ±0.1 dB. Volts/div. linearity : ±1.5% of full-scale range. Quantization error : ±0.25% of full-scale range for 5 Hz to 5 kHz filter bandwidths.
Bandwidth/dispersion switching accuracy :	Maximum error when switching between bandwidths and Hz/div. settings (15 to 25 °C) : Log : ±1 dB, ±1% f.s.d. Linear : ±10%.
Average noise level : (between 100 kHz and 110 MHz)	Less than -120 dBm with counter 'ON'. Less than -130 dBm with counter 'OFF'. (Both measurements made on MANUAL sweep with 50 Hz filter selected.)
Spurious responses :	70 dB below a single signal at a level of -40 dBm at input mixer.
Intermodulation display :	-70 dB (two tone test) with signals at -40 dBm at input mixer and 500 Hz apart (measurements made on MANUAL sweep).
Residual responses :	30 Hz to 20 kHz less than -90 dBm. 20 kHz to 110 MHz less than -100 dBm (measured at input mixer or INPUT socket, whichever is greater).
Amplitude stability :	±0.1 dB/°C

Calibrator

Output impedance :	50 Ω nominal (BNC type socket).
Frequency :	10 MHz ±20 Hz.
Amplitude :	-10 dBm ±0.3 dB.

Tracking generator output

Enables the transfer characteristic of any network to be measured over a dynamic range of up to 120 dB.

Output impedance :	50 Ω (BNC type socket).
Output v.s.w.r. :	Less than 1.2 : 1.
Frequency :	Within ±2 Hz of the input tuned frequency.
Amplitude :	-10 dBm ±2 dB at 10 MHz.
Frequency response : (relative to 10 MHz level)	±1 dB from 100 Hz to 100 MHz. -3 dB at less than 30 Hz and greater than 110 MHz.

Frequency measurement

Range :	30 Hz to 110 MHz. Four REFERENCE FREQUENCY controls provide frequency cover of 0-110 MHz minimum. Three of the controls give adequate incremental coverage across the frequency range of approx. ±1 MHz, ±70 kHz and ±1 kHz.
Reference frequency :	The reference frequency may be positioned to the centre or left-hand edge of the graticule display by front panel push button selection. Accuracy : see 'Counter'.
Sweep modes :	Auto : Analyser sweep free runs. Manual : Sweep position determined by the BRIGHT LINE POSITION control which is continuously variable across the display in either direction. In this mode the instrument may be used as a selective level measuring set, a video filter for noise averaging being automatically selected. Single : A single sweep may be initiated by the START control. Start : Sweeps may be terminated at any time by pressing this button. The sweep will re-commence when this button is released.
Sweep range :	18 calibrated sweep widths in two bands : 10 MHz/div. to 0.02 MHz/div. and 10 kHz/div. to 0.02 kHz/div. In the kHz/div. mode, the 0-110 MHz and ±1 MHz REFERENCE FREQUENCY controls are phase locked to frequency increments of 1 MHz and 100 kHz respectively.
Sweep range accuracy :	±10% of full-scale ±20 Hz, against electronic graticule. May be set to within ±1% ±20 Hz using internal counter.

Together, the master and 4.8 MHz offset oscillators control the frequency of the slave, which is always phase locked to the difference frequency even during a sweep. The 4.8 MHz oscillator is not swept, but provides precise incremental steps of 100 kHz, since it is phase locked.

When phase locked, the phase difference between the slave and master oscillator is compared in a quadrature mixer arrangement to check whether the slave oscillator has locked above or below the frequency of the master oscillator. The search oscillator is not stopped until the correct frequency relationship of the two oscillators is achieved.

The master is swept on the MHz/div range setting, the amount of sweep depending on the degree of attenuation inserted by the horizontal scale button, or is phase locked at 1 MHz intervals on the kHz/div range.

When on kHz/div, the offset oscillator is able to give the cover in 100 kHz steps between the 1 MHz lock points of the master. When set to MHz/div, the offset oscillator is not varied but fixed, and the '±1 MHz' control acts directly on the master as a fine control.

All phase lock loops have automatic search circuits incorporated although not all of them are shown in the diagram.

Second local oscillator

When the first local oscillator is phase locked, the sweep must be performed by another oscillator which is stable enough so that a 5 Hz filter can be used to advantage. This is effected by an oscillator of 3.4 MHz nominal frequency swept by ±150 kHz.

The varactor sensitivity of approx. 30 kHz/V keeps the problems of noise and spurious sidebands within reason, and provides enough sweep to take over sweeping from the first local oscillator at the point where the stability of the latter becomes inadequate.

The change over from sweeping the first local oscillator to the second local oscillator while phase locking the first local oscillator, is achieved automatically when selecting the desired sweep width. Thus sweeps of 10 MHz/div to 0.02 MHz/div are provided by the horizontal scale push button switch when the range switch is set to MHz/div. In this condition sweeping is accomplished by the first local oscillator (which is then, of course, not phase locked) and the reference frequency controls '0-110 MHz' and '±1 MHz' act together on the first local oscillator as coarse and fine controls.

The '±70 kHz' and '±1 kHz' controls act in the same way for the second local oscillator but the '±1 kHz' control is too fine to be useful in this condition.

When the kHz/div button is pressed the horizontal scale factor is changed by 1000 and so sweeps of 10 kHz/div to 0.02 kHz/div are provided by the second local oscillator. The first local oscillator is phase locked in this condition and may be altered in 1 MHz steps by the '0-110 MHz' control and in 100 kHz steps by the '±1 MHz' control. Thus in this mode all four controls provide successively finer alterations of centre frequency about which the second local oscillator sweeps.

The schematic of the second local oscillator is shown in Fig. 3.6. Many features are similar to those of the first oscillator. Quadrature mixer phase detector and lock check circuits are used. The shaper is separate from the first, but the attenuator used for the horizontal scale is the same and the sweep is switched to the appropriate oscillator.

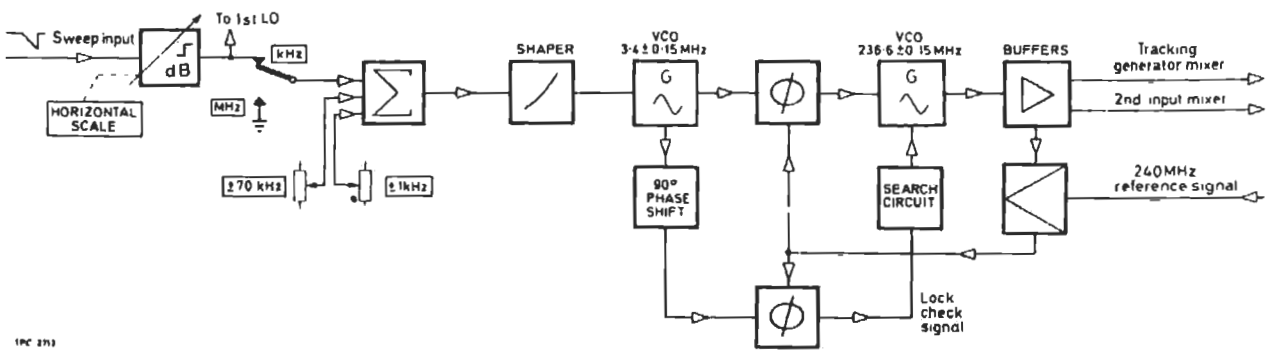


Fig. 3.6 Block diagram of second local oscillator system

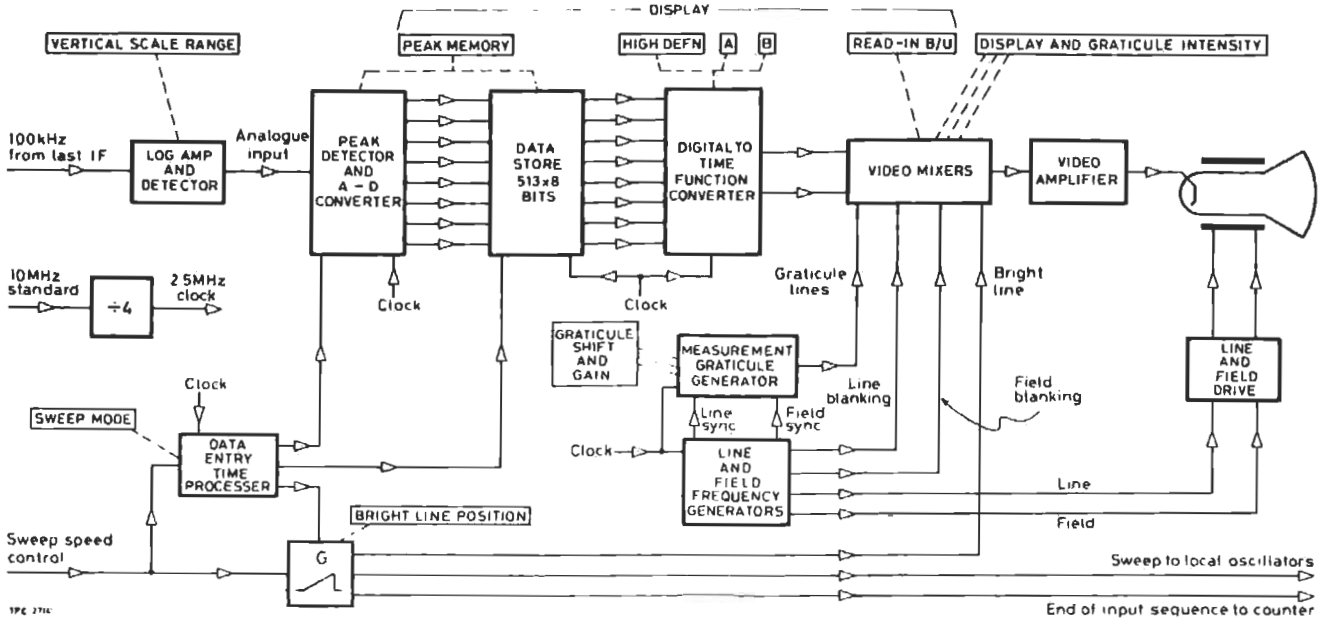


Fig. 3.7 Overall block diagram of data store and display

The 240 MHz reference input, like the 10 MHz to the first oscillator, is derived from the crystal standard.

The total tuning range of the second oscillator is ±150 kHz. This is needed to accommodate both centre frequency and left-hand side frequency expansion called up by the display section, as well as '±70 kHz' control and the sweep itself.

3.1.6 Data store and display

The 100 kHz signal from the last i.f. passes to the logarithmic amplifier and detector - see Fig. 3.7. This detected signal must now be converted into a set of digital words which can be stored prior to displaying. The analogue to digital converter must be capable of working to at least the accuracy of the preceding circuitry, and at the same time be fast enough to gather information correctly from the fastest sweeps.

Analogue to digital converter

Conversion takes place at precise times which are controlled by a set of counters dividing the basic clock frequency by a preset number. Since these times do not necessarily correspond to peaks in the detected output, there is a further requirement for the analogue to digital converter. This is to hold the peak value of the detector output between conversion times, so that any spectrum spike occurring between these times is presented to the store and displayed at the next data point.

To capture and hold these spikes a second peak detector is used as shown in Fig. 3.8. Both peak detectors can be discharged once their output has been read into the peak store, which must be capable of reaching the maximum value in a very short time, and also retain this value accurately until the next conversion time. The peak voltage is converted into its digital form in a conventional ramp converter.

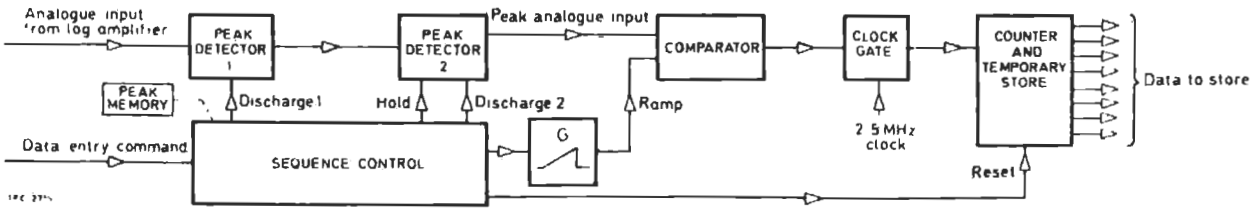


Fig. 3.8 Block diagram of peak detector and analogue to digital converter

Considering the conversion sequence, the output from detector 2 is frozen at the latest peak value, and then converted to the equivalent binary number and presented ready for storing. During the conversion time detector 1 is operating. Immediately after conversion the freeze signal is removed from the second detector and it is discharged. When the discharge is ended detector 2 is able to take the peak value as recorded by detector 1, which is discharged just prior to detector 2 being frozen for the next conversion. Any peak signal occurring during this discharge time is not lost as the output of detector 1 follows the input during the discharge. As soon as detector 1 is discharged the sequence is repeated.

After conversion, the digital number is temporarily stored in the counter. It is transferred to the main store at the beginning of the next conversion time.

The capacity of the store is 513 eight bit words. When the spectrum analyser is used in in its high definition mode the display uses 470 of these words. The remaining words can be accessed from the store only during scan flyback.

Display technique

A magnetically deflected display tube is used.

The display method is to use the vertically scanned raster as a framework on which the electronic graticule is displayed; the data is displayed by brightening up the raster lines to a height representing the input voltage. The maximum number of spectrum lines displayed is limited by the number of raster lines, viz 470 per displayed area. As the line rate is fixed there is no problem in achieving 0.5% accuracy and, as both data display and graticule undergo the same deflection distortion, the accuracy can be ±1 bit.

Data accession

To obtain the greatest accuracy on the display, digital data accessed from the store is converted from the digital form to a time function which is as accurate as the crystal standard. The amplitude graticule is also timed by this same crystal standard.

The time function is produced by presetting a counter to the binary inverse of the number stored in the store, at the beginning of each line scan. The raster is brightened up until the preset counter clocked by the standard clock, reaches its maximum count. At this instant the raster line is dimmed to the graticule brightness level. Obviously, the larger the digital number in the store, the smaller the number preset in the counter, and the longer the time taken before the maximum count is reached and the raster dimmed.

As the data input rate, data access rate and the electronic requirements of the shift registers used in the store are not directly compatible, data in the store is multiplexed. Data is accessed from the store at line rate. As there are 513 words in the store and the maximum line rate using standard techniques is about 20 kHz, the total contents of the store can be accessed every 25.65 ms. In a simple display, this rate would cause excessive flicker, but this is eliminated by using dual interlace.

Data input to the store is arranged so that each time data is recirculated in the store shift registers, one word may be entered. To obtain different input rates the shift register is allowed to recirculate once, twice, five times etc. in 1, 2, 5, 10 ... 1000 sequence, before the next data word is entered.

The fastest sweep required is 100 ms. In this time 513 words must be entered to fill the store, i.e. 1 word per 194.9 μs. In this time the store must recirculate once. Hence the clock rate required is $1/(194.9 \times 10^{-6} \div 513) = 2.63$ MHz. In practice a slightly slower sweep is allowed and a 2.5 MHz clock is used.

Considering the data access from the store, a clock rate of 2.5 MHz and a line rate of 20 kHz means that lines occur every 125 clock pulses. By reducing the line rate to 19.53125 kHz, it becomes equal to clock rate divided by 128, which provides the basis for the store multiplexing. By using a line frequency of 19.53125 kHz and clock frequency of 2.5 MHz, four 8 bit words are removed from the store every 512 clock pulses, and the store, having 513 words, is one word removed from the start. Hence the next four words bring the store back to a similar position but two bits removed from the start.

Continuing this sequence 64 times, the store is 64 bits removed from the start and has accessed 64 x 4 = 256 words. This is half the store. Remembering that a double interlaced scan is being used, the second frame is now ready to start. This continues until the final 256 words are removed from the store.

Data entry

It can be seen that the first word in each frame accessed from the store are positioned 64 words apart in the store. Similarly the second words are 64 words removed from the first and 64 words apart. Hence the input data must be inserted so that the second word is 64 words after the first and the third 64 words behind the second and so on. This is combined with the data input criteria by allowing the store to recirculate one whole revolution and 64 words each time data is put in on the fastest sweep, two revolutions and 64 words on the second fastest sweep and so on. As there are 64 x 8 + 1 words in the store the 9th word will correctly place itself one word in front of the first which fits in with the data readout criteria.

Sweep generator

The sweep supplied to the local oscillators in the r.f. section must be in synchronism with the data input to the store, and be of exactly the correct amplitude and duration on each sweep speed. This enables an accuracy of ±1 line in the data display to be achieved.

The method used is to take each data input command pulse and, by means of a counter and digital to analogue converter, use it to produce a staircase waveform. This staircase can be reset each time a complete set of data has entered the store - or at any time if the sweep is interrupted by operator intervention. As there are the same number of data input pulses no matter what sweep speed is selected, the staircase is of constant size but of variable rate. Its amplitude at any time corresponds exactly to the data input point to the store.

The steps in the staircase waveform are removed by an integrator with a relatively short time constant which is switched with sweep speed. The accuracy of the time constant is not critical.

Each time 512 words have been entered in the store, the input sequence stops. A signal is passed to the frequency counter enabling the 'count centre frequency' sequence to begin. Whilst the centre frequency of the scan is being calculated, the scan voltage is held constant at half the maximum scan voltage by presetting the staircase generator. When the centre frequency has been measured, and stored in the counter memory latches, a signal is passed to the input sequence circuitry.

In the auto mode, the input sequence is re-synchronized to the start of the data in the recirculating shift register and the read-in sequence is repeated. Should a single sweep have been selected, the resynchronizing pulse is inhibited hence inhibiting the start of another read-in sequence.

When operating in the manual mode data is placed in the store at the point where the bright line is displayed. This method of data renewal is easily achieved as data is accessed from the store at the beginning of a line scan, and by detecting the bright line signal at the start of a line scan and gating it with a data access pulse, a 'manual data input' pulse is produced.

Dual store

In the dual store mode the input and output sequence to the store is slightly modified. Alternate data input pulses are inhibited, the ones inhibited being odd or even depending on the selection of A or B store refresh.

Referring back to the data readout sequence described earlier, it can be seen that these two stores will be accessed alternately each field scan.

The method employed is to display both A and B stores on each field. To do this a latch is used to store one word of data. When store A is being accessed directly by line rate pulses, store B may be accessed at a time 64 clock pulses earlier and stored in the latch. Hence by using two presettable counters and two sets of raster bright-up circuits, one operated directly from the store, and the other from the word stored in the latch, the required display of A and B stores can be achieved.

To obtain a display of A store only, the bright-up circuit is switched between the outputs of the two presettable counters. As during one field store A is accessed by line pulses; during the next, as B is being accessed directly, A is accessed by the latch operating 64 clock pulses earlier. Similarly B is accessed by a similar process operating 180^{o} out of phase.

Not only can a signal be measured accurately in amplitude, it can also be compared accurately using the dual store mode with another signal which need not be at the same frequency.

Measurement graticule

Measurement of frequency is very accurate using the graticule, and can be set so that permanent records using photographs can be taken without the need for any note of the frequency graticule error.

The frequency graticule is generated by an astable circuit. Its output pulses are synchronized by field scan, and delayed after field scan by a settable time. The period of the oscillation of the astable circuit is also alterable. By changing the delay and period, the frequency graticule can be both shifted and expanded.

Thus, with the help of the frequency counter, the graticule can be adjusted in two simple operations to be exactly correct to the accuracy of the counter, over any sweep width chosen. Hence not only can a signal be measured accurately and easily in amplitude, it can be calibrated on a frequency graticule, and a permanent record kept at the high accuracy.

The dashed lines on the frequency graticule are added to serve a dual purpose. The lines are positioned to be the first, centre and last graticule lines. The first and last are marked to show the extent of the calibrated sweep, and the centre for ease of identifying the point at which the counter measures the centre frequency. The lines also enable the operator to calculate relative levels of signals more easily by grouping the dB lines in sets of two major divisions.

To produce the dashed lines, the first, centre (sixth) and last (eleventh) frequency graticule lines are detected using a ÷ 5 counter preset to a count of 4 each field flyback. Each time a count of 5, 10 or 15 is reached, the standard graticule line is gated out and a new line introduced, by counting major amplitude graticule divisions and dividing by 4 to produce alternate dashes of 2 bright and 2 dim divisions. When the third dashed frequency line has been produced, all frequency graticule lines are inhibited so that the 11th frequency graticule line - producing 10 divisions - is the last line displayed.

The amplitude graticule lines are produced from the standard clock. They are generated by two counters - see Fig. 3.9. The first is a ÷ 128 counter operating on the clock rate to produce a pulse at line rate. This counter is synchronized at field rate, but delayed from the start of the field. Pulses at line rate are hence produced slightly delayed by the same amount. They are used to preset the graticule generator counter which counts clock rate producing a narrow line each count, and a wider line each 5th count as set by the pulse time of two monostables.

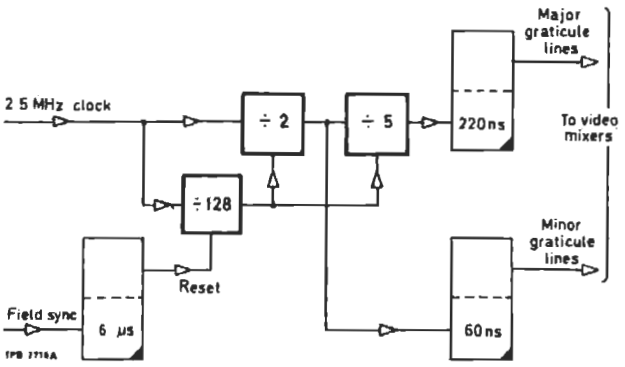


Fig. 3.9 Block diagram of amplitude graticule generator

All the signals finally come to the video mixers and amplifier. The bright line signal is added at a constant level. The frequency and amplitude graticule are gated together and fed to the video signal at an adjustable level, the data display is added at an adjustable level, and both A and B stores can be adjusted independently. Line and field blanking is added and the final signal, which is very similar to that of a standard television video signal, is presented as modulation to the display tube electrodes.

3.2 PROGRAMMABLE INPUT ATTENUATOR—AH1

Circuit diagram— Fig. 7.7

This is a stepped attenuator giving up to 120 dB loss in 10 dB steps.

The pad sections consist of resistive π networks with a characteristic impedance of 50 Ω.

Electrical shielding is provided by a metal casting divided into compartments which house the pads. The dimensions of the casting, together with the pads, bypass links and microswitches, are designed to maintain the characteristic impedance. Provision is made by controlling the spacing of components, and the adjustment of stray reactance, to ensure maintenance of performance up to 110 MHz.

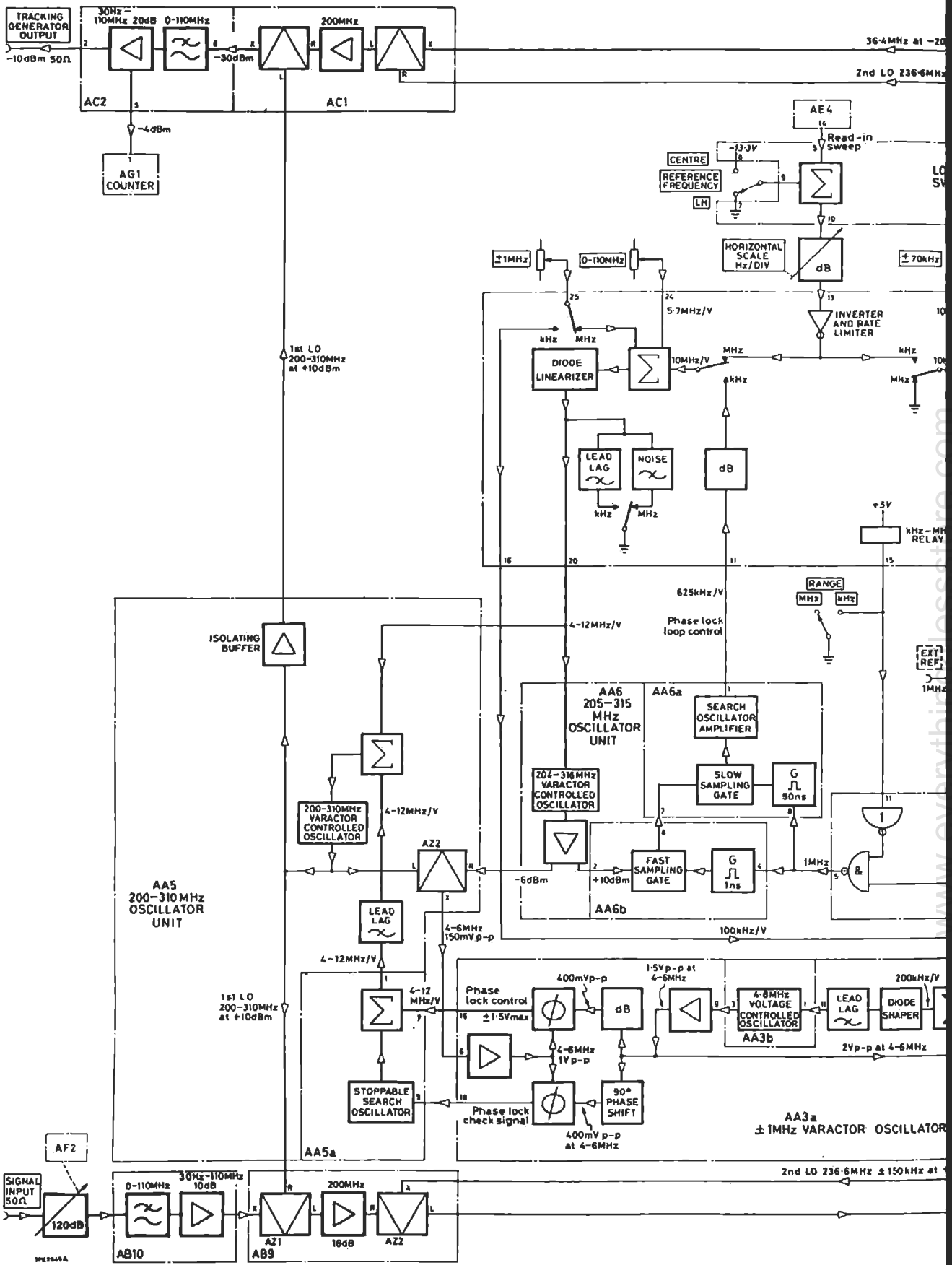
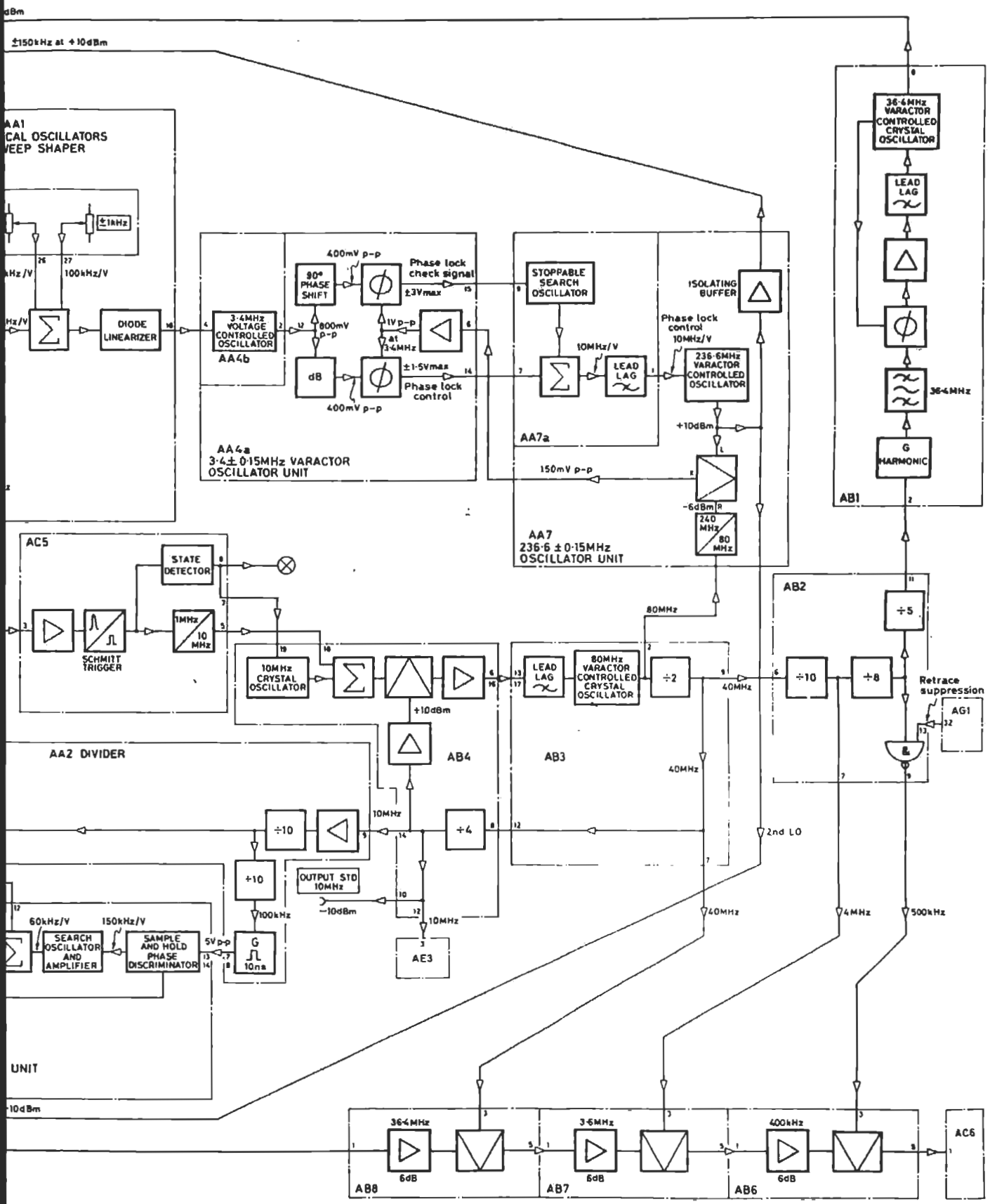


Fig. 3.10 Block diagram – Oscillator system



Pads are taken out of circuit by micro-switches, housed inside the screened compartments, which are operated in pairs by solenoids energized by drivers on AF2.

Signal input is via the input 50 Ω socket on the front panel. Output is fed to AB10.

3.3 30 Hz to 110 MHz INPUT SIGNAL AMPLIFIER—AB10, AB10a and AB10b

Circuit diagram—Fig. 7.7
Block diagram—Fig. 3.10

This stage consists of low-pass filter AB10, 10 dB wide band amplifier AB10a, and supply line cleaner AB10b. Input is via the 120 dB programmable attenuator.

Low-pass filter AB10 is preset to curve (a) in Fig. 3.11, and C7 is selected for optimum v.s.w.r.

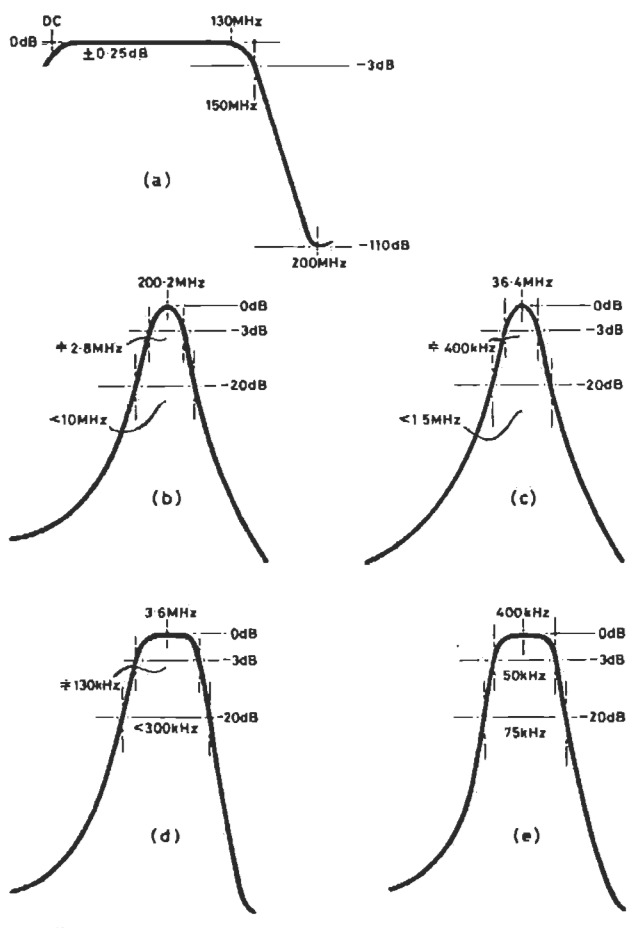


Fig. 3.11 Response curves of input low-pass filter and i.f. signal amplifiers

The signal is passed to wide band amplifier TR1 to TR6 (AB10a) via pin 6. The amplifier has a nominally flat response between 100 Hz and 100 MHz, with a gain of 10 dB. Adjustment of R19 balances the d.c. output, and C14, C16 are chosen to give a flat response. TR1, TR2 are an input pair, and with TR3, TR4 form two balanced feedback pairs, which are a.c. coupled with balanced output transistors TR5, TR6. Amplifier output is taken via double screened coaxial cables to the input balanced mixer of 200.2 MHz i.f. signal amplifier AB9.

Line cleaner AB10b provides stable, current limited supplies of approximately +11.5 V and -11.5 V for board AB10a .

R1 sets the reference voltage for the +11.5 V line. R3, R4 provide the feedback voltage to comparator IC1, which is short circuit protected. C2 provides the frequency characteristic roll-off point, and R2 sets the circuit protection current limit.

The -11.5 V line is similar to the +11.5 V line :

R5, R6 provide the reference voltage, R7, R8 the feedback voltage to comparator IC2, and C4 the frequency characteristic roll-off point. TR1, with R9, R10, D1, D2 and D3, forms a series regulator external to IC1, which is capable of withstanding up to 5 s short circuit.

3.4 200.2 MHz IF SIGNAL AMPLIFIER—AB9

Circuit diagram—Fig. 7.7
Block diagram—Fig. 3.10

Output of AB10a is fed to input balanced mixer AZ1, which also receives swept frequency output of the first local oscillator of 200 to 310 MHz. AZ1 output of 200.2 MHz is fed via R1 to TP1 emitter.

TR1 to TR4 are cascaded grounded base amplifiers, each tuned to 200.2 MHz (see curve (b) in Fig. 3.11), with an overall gain of approximately 8 dB. Output is passed to output balanced mixer AZ2. Also fed to AZ2 is the variable output (236.6 MHz ±150 kHz) of the second local oscillator.

Mixer output of 36.4 MHz is fed to 36.4 MHz i.f. signal amplifier AB8.

3.5 36.4 MHz IF SIGNAL AMPLIFIER—AB8 3.6 MHz IF SIGNAL AMPLIFIER—AB7 400 kHz IF SIGNAL AMPLIFIER—AB6

Circuit diagram—Fig. 7.8
Block diagram—Fig. 3.10

These boards form a group of three i.f. amplifiers with an overall gain of unity. Each amplifier is designed for a particular frequency response. The response curves (AB8 curve (c), AB7 curve (d), AB6 curve (e)) are shown in Fig. 3.11.

36.4 MHz output of AZ2 on AB9 is fed to AB8 at pin 1. AB8 contains three transistor stages, TR1, TR2 and TR3, with frequency responses shaped by four tuned circuits. Potentiometer R12 adjusts the overall amplifier and mixer gain to unity. L8, C17, at the output of TR3, provide increased rejection at 200 MHz. Output of TR3 is transformer coupled (T2) into balanced mixer IC1. The mixer is also fed with 40 MHz output of AB3. Mixer output of 3.6 MHz is transformer coupled (T3) into AB7.

AB7 consists of three transistor stages, TR1, TR2 and TR3. 3.6 MHz from AB8 is taken via pin 1.

The first stage contains tuned circuit L1, C4 which is overcoupled to tuned circuit L2, C6 via C5. Stage two tuned circuit L3, C8 is undercoupled to L4, C11 via C10. The overall amplifier and mixer gain is set to unity by R16. TR2 output is transformer coupled into balanced mixer IC1, which is also fed with 4 MHz output of AB3. Mixer output of 400 kHz is passed to AB6.

AB6 has three transistor stages; the first, TR1, is followed by an overcoupled pair of tuned circuits, and the second, TR2, by an undercoupled pair of tuned circuits. R16 sets the overall amplifier and mixer gain to unity. L6 and C18, in the output of TR1, increase the rejection at the mirror channel of 600 kHz.

Output of TR3 is transformer coupled (T2) into balanced mixer IC1, which is also fed with 500 kHz from AB2. Mixer output of 100 kHz is taken to the switched gain amplifier AC6.

3.6 80 MHz CRYSTAL OSCILLATOR—AB3

Circuit diagram—Fig. 7.9
Block diagram—Fig. 3.10

Transistor TR1 and associated circuit forms an 80 MHz varactor controlled crystal oscillator. The main tuning components are L1, C5, C7, C8, varactor diodes D1 and D2, and crystal XL1. The output signal is passed to TR2.

The output of the tapped inductor in the collector circuit of TR2 is fed two ways; to emitter follower TR3, and then out to AA7, and also to IC1.

IC1 is a high frequency bistable which divides the 80 MHz signal to 40 MHz. The signal is passed via emitter follower TR4 to three paralleled output stages. One path, via C19, is to cascade amplifier TR5, TR6 which provides an output to AB8. A second path via C23 to AB2, and a third path via C25 and amplifier TR7 to AB4.

3.7 10 MHz REFERENCE CRYSTAL OSCILLATOR—AB4

Circuit diagram—Fig. 7.9
Block diagram—Fig. 3.10

A 40 MHz signal is fed to pin 8 from AB3. The signal is taken to IC1 which is a high frequency dual bistable connected as a divide by four.

The 10 MHz output at pin 9, IC1b, is fed to emitter follower TR2. The signal at TR2 emitter drives amplifier TR3 which contains transformer T2 in its collector. T2 forms a ring bridge modulator with T1 and IC2, which is used as a phase comparator comparing the signal from TR3 with the output signal of temperature controlled crystal oscillator X1. The output of X1 is fed via C7 and amplifier TR11 to the other side of the ring bridge modulator. The 10 MHz signal output of TR3 is at sufficient level to drive alternate pairs of diodes of IC2 into conduction on alternate half cycles.

The output of the phase comparator at the centre tap of T1 is fed via R7 and R8 to the base of TR9. TR9 and TR10 form a long tailed pair, differential amplifier. The signals at TR9, TR10 collectors are fed via pins 6 and 16 to the varactor diodes on AB3.

The differential action of TR9, TR10 helps balance out hum on the +14 V, -14 V lines, reducing the level of hum applied to varactor diodes D1 and D2 on AB3. Potentiometer R42, whose attenuated output is taken to the base of TR10, allows a d.c. preset bias to be applied across varactor diodes D1 and D2 on AB3.

10 MHz output of IC1b, pin 15, is applied to emitter followers TR4 and TR5. The output of TR5 drives three parallel 10 MHz output stages, TR6, TR7 and TR8.

The first 10 MHz signal is routed to potentiometer R30 in the emitter circuit of TR6. Output of TR6 is fed via pin 10 to the front panel standard 10 MHz socket. The output level at the socket is -10 dBm when terminated with 50 Ω, and is set by R30.

A second signal from TR5 is fed via C18 to the emitter of TR7. Output of TR7 is taken via pin 12 to AE3. This 10 MHz signal is used, after being divided by four, as the clock drive for the digital store.

The third output of TR5 is routed via C21 to the emitter of TR8. The output of this buffer is taken via pin 14 to AA2, and used to produce a comb for the phase locking of the first local oscillator.

3.8 FIXED OSCILLATOR DIVIDER CHAIN —AB2

Circuit diagram— Fig. 7.9
Block diagram—Fig. 3.10

40 MHz output of AB3 is taken to IC1a via pin 6. IC1a divides the signal by 5, and IC1b further divides the signal by 2.

The 4 MHz signal at pin 15, IC1b, is applied to emitter follower TR1. The output of TR1 is fed to the base of amplifier TR3. The amplifier produces an output which passes via pin 7 to AB7 as the 4 MHz mixer drive. C20 reduces the high frequency components of the 4 MHz square wave output.

A second output of TR1 is applied to the base of TR2, which amplifies the 4 MHz signal to sufficient level to operate IC2. IC2 divides the signal by eight, producing 500 kHz. This signal is passed via NAND gates IC4b and IC4c to amplifier TR4. The output of TR4 is taken via pin 9 to AB6 to be used as a local oscillator drive.

A further input to IC4c turns off the 500 kHz output to the i.f. mixer during T time. The T time input is taken via pin 13.

T time suppression of the 500 kHz local oscillator output during flyback open circuits the i.f. path. This avoids any spurious response at the start of scan due to the filter memory of a previous response.

Diode D1 clips the top of the 500 kHz square wave output of IC4c to remove any residual modulation.

A second output of IC2 is passed via NAND gate IC4a to IC3. IC4a acts as a buffer to prevent signals from IC3 appearing on the output of IC2. IC3 divides the 500 kHz signal down to 100 kHz, and the output is taken via pin 11 to AB1.

3.9 36.4 MHz CRYSTAL OSCILLATOR—AB1

Circuit diagram— Fig. 7.9
Block diagram—Fig. 3.10

The 100 kHz square wave output of AB2 is passed to amplifier TR1 via pin 2. TR1 output is tuned to 36.4 MHz by L1 and C5. TR2, whose collector is tuned to 36.4 MHz, further amplifies the signal, and a comb of 100 kHz signals about 36.4 MHz is produced at its collector. This output is tapped at L2, and fed to T2 which is part of a ring bridge, used as a phase comparator. The signal is compared with output of 36.4 MHz phase locked crystal oscillator TR3.

TR3 output is amplified by TR4, TR5 and provides drive to the phase comparator IC1. The d.c. output of the phase comparator is amplified by IC2 and applied to D1 via R8 to control the oscillator frequency. Potentiometer R30 optimizes the d.c. bias in the phase locked loop.

Diodes D2, D3 and D4 form a clamp circuit which prevents the phase locked loop going into a locked state during switch on.

TR3 is tuned by C12, C14, C15, inductor L3, varactor diode D1 and crystal XL1.

An additional output at 36.4 MHz is taken from TR5 via R23, attenuator pad R24, R34 and R35, and isolating transformer T3. The signal passes via pins 7 and 8 to AC1. The output level of this 'tracking generator reference' signal is adjusted by variable resistor R23.

3.10 LINE CLEANERS – AB5

Circuit diagram—Fig. 7.5

These are positioned in h.t. lines remote from the power supply to provide supplies free from spurious interfering signals. The cleaners consist of a.c. coupled shunt regulators connected to reduce any unwanted h.t. line signals by greater than 30 dB over the range 50 Hz to 50 kHz.

+6 V line cleaner

The reference earth on pin 10 is a.c. coupled to pin 3 of IC2 via C5 and emitter follower TR3. Because of the inherent high open loop gain of IC2, the feedback loop from pin 6 of IC2, via emitter follower TR4, ensures that the voltage on pin 2 of IC2 is within a few μV of that on pin 3.

As the level of the interfering signal on the +6 V line is approximately 5 mV, TR4 has to produce a correction current of 10 mA through R17, R18 to achieve zero signal level on the +5.5 V line. Therefore, TR4 is biased to operate at a quiescent current level of approximately 20 mA. To achieve this, the current through TR4 collector is sensed by the voltage developed across R19. This voltage is fed to the base of TR3 via potential divider R11, R12 and series resistor R13, producing stable biasing conditions even if the +6 V line is altered by about one volt.

R13 and C5 set the limit for low frequency performance. TR3 is a low leakage transistor operated at low collector/base potential, produced by the divider R14, R16.

Diode D4 achieves fast initial turn on by charging C5 to near its final value.

L2 and C6 provide smoothing at frequencies above those at which IC2 operates.

The -6 V line cleaner is similar to the +6 V line cleaner.

The +15 V and -15 V line cleaners are also similar, and include Zener diodes D2, D3 and D5, D6, respectively, to provide correct biasing.

3.11 OVERALL DESCRIPTION OF FIRST AND SECOND LOCAL OSCILLATORS AA1 to AA7

Block diagram—Fig. 3.10

The read in sweep from the digital store enters at pin 5 on AA1, at a level between 0 V and +10 V. The sweep is summed with the centre left-hand reference frequency level and then attenuated by the horizontal scale Hz/division attenuator. This produces a signal at the correct size to produce the desired frequency sweep.

The output of the attenuator at pin 13 of AA1 is inverted and rate limited in the negative-going direction. Rate limiting is necessary to ensure that the slave oscillator does not lose phase lock with the master oscillator during flyback on the faster sweeps. After rate limiting, the saw-tooth signal is routed to the second local oscillator in the kHz/div. mode, where it operates at a sensitivity of 10 kHz/volt, or fed to the first local oscillator where it operates at sensitivity of 10 MHz/volt.

In the kHz/division mode, the sweep is summed with the ±70 kHz and ±1 kHz reference frequency controls, and then diode linearized. This distorts the sweep and reference signals to produce a linear frequency change from the 3.4 MHz voltage controlled oscillator on AA4b.

The frequency changes of the 3.4 MHz voltage controlled oscillator are converted to 236.6 MHz, the desired frequency for the second local oscillator, using a phase locked loop. The output of the 236.6 MHz varactor controlled oscillator is compared with a reference signal of 240 MHz which is derived from the 80 MHz reference signal sent to AA7.

The difference frequency resulting from this comparison appears at the X output of the mixer in which the two signals are compared. The difference signal enters AA4a at pin 6. The difference frequency is then compared, by a phase discriminator, to the 3.4 MHz leaving the voltage controlled oscillator on AA4b. The d.c. control signal leaving the phase discriminator is fed via pin 14 (AA4a) to pin 7 (AA7a) and thus via a summer and lead lag filter to control the 236.6 MHz varactor controlled oscillator.

To prevent the oscillator locking onto the unwanted upper sideband, at 243.4 MHz, an additional loop is included to check the phase relationship at lock between the 3.4 MHz voltage controlled oscillator on AA4b and the difference signal derived from the 236.6 MHz oscillator.

Should the phase be in the correct relationship, the output of the phase comparator of the phase lock check signal loop will produce +3 V at pin 15 of AA4a. This in turn stops the stoppable search oscillator on AA7 which leaves the 236.6 MHz oscillator at this particular frequency.

Should the signals be in anti-phase at the phase comparator, the output will be at -3 V which will not stop the stoppable search oscillator, and the search continues until the correct phase lock is achieved.

In the kHz/division mode, the 1st local oscillator, consisting of boards AA3, AA5 and AA6, is operated in a phase lock mode at intervals of every 100 kHz over its range, 200 to 310 MHz. This is achieved by synthesis of two oscillator units, one the AA3 oscillator at 4.8 MHz ±1 MHz, which phase locks at 100 kHz intervals, and the other the AA6 oscillator, operating between 205 to 315 MHz in 1 MHz increments.

The two oscillators are combined in slave oscillator unit AA5 by a phase locked loop. The final oscillator locks from 200 to 310 MHz in 100 kHz increments.

A 10 MHz reference frequency enters AA2 divider board at pin 9, and is divided to produce the 1 MHz and 100 kHz drive signals.

The 1 MHz signal leaves AA2, at pin 5, to drive the sampling gates in the phase locked loop of AA6 oscillator. The sampled signal from the sampling gate leaves AA6a at pin 1 and enters AA1 at pin 11. It is then routed via an attenuator and a summer, which combines the potential of the 0 to 110 MHz reference potentiometer, through the diode linearizer and lead lag filter back to AA6a via pin 20. Here it controls the 204 to 316 MHz varactor controlled oscillator on AA6.

The 100 kHz drive from AA2 enters AA3 as a balanced drive at pins 13 and 14 to drive the sample and hold phase discriminator. The output of the phase discriminator is fed to a search oscillator and amplifier, and a summer circuit which adds the potential of the ±1 MHz reference frequency potentiometer; then fed via a diode shaper and lead lag filter to control the 4.8 MHz voltage control oscillator so that it locks at 100 kHz steps over the range 3.8 to 5.8 MHz. In both this, and the AA6 oscillator loops, a search oscillator is incorporated so that if either of the oscillators is not locked onto an appropriate increment, the search oscillator will start and then sweep the oscillator through a correct lock point.

The slave oscillator on AA5 combines the two phase locked loops as follows :

An output of the 200 to 310 MHz oscillator on AA5 is compared with the output of the 204 to 316 MHz oscillator on AA6 in a mixer on AA5. The difference frequency resulting from this comparison, at pin X of the mixer, is taken to pin 6 on AA3 and compared in phase with the 4.8 MHz frequency derived from the oscillator on AA3. The difference signal leaving the phase comparator on AA3, at pin 16, controls the 200 to 310 MHz slave oscillator so that its frequency becomes exactly the difference between the oscillators on AA6 and AA3.

In the second local oscillator, an additional phase locked check loop is used to ensure that the slave oscillator is locking onto the difference signal and not the sum. This 'check' signal leaves AA3 at pin 18, and stops the stoppable search oscillator if its level becomes +3 V indicating the correct sideband. Otherwise, the search continues until the correct sideband is found.

When the instrument is used in the MHz/division mode, the first local oscillator is not phase locked but swept. The slave/master relationship between AA5 and AA6 is maintained, but the reference frequency control potentiometer is switched out at pin 12 on AA3, and the 4.8 MHz oscillator rests at approximately 5.7 MHz. This ±1 MHz reference frequency control is switched into the summer of the control signal to AA6, and replaces the frequency shift in this oscillator which is lost in AA3.

The attenuated sweep entering pin 13 on AA1 is now added to the potential from the two reference frequency controls in a summer, and passed via a diode linearizer and noise filter to control the 205 to 315 MHz varactor controlled oscillator.

As previously described, AA5 is a slave oscillator to AA6, the difference frequency being that of the AA3 oscillator.

3.11.1 Sweep shaper and local regulator AA1

Circuit diagram — Fig. 7.10

The sweep generated on AE4 of the digital store enters at pin 5, at a level of 0 V to +10 V. Operation of the centre frequency button adds a suitable offset voltage which is summed by IC3a. The sweep signal leaves at pin 10, and is fed to the horizontal scale (Hz/division) control. Here it is attenuated in 1-2-5 sequence down to the lowest level of 20 mV peak-to-peak, and then returned via pin 13.

The signal is inverted and rate limited by IC3b. D30 is cut off if the fly-back rate exceeds a pre-determined rate. This is necessary to prevent the slave oscillator losing phase lock with the master oscillator should the fly-back rate be exceeded.

In the MHz/division position, the sweep signal is fed to the first local oscillator shaper after combination with signals from the reference frequency control (0 to 110 MHz) and ±1 MHz in the current summing stage IC4a.

The first local oscillator shaper consists of seven biased diodes (D6 to D12) which successively limit to distort the signal into semi-parabolic shape. This diode network forms the gain determining resistance element in an amplifier comprising IC4b and TR10. The output of the stage is fed via noise filter R63, C14 to output pin 20.

In the kHz/division position, the 0 to 110 MHz reference frequency control feeds IC4a which steers the first local oscillator over its total range. The ±1 MHz reference control is fed to board AA3, via pin 16, to control the oscillator in its 100 kHz steps from 3.8 to 5.8 MHz.

The sweep at TR7 output is fed to summer IC5, where it is combined with outputs of the ±70 kHz and ±1 kHz reference frequency controls, and then pre-distorted by the second local oscillator shaper consisting of biased diodes (D15 to D28).

The diode network forms one of the two gain determining resistor elements in amplifier IC5b. Overall gain and offset voltages are set by R107 and R104. The output of the amplifier is fed via noise filter R109, C20, and pin 18 to control the 3.6 MHz oscillator on AA4.

IC1 and IC2a form a double regulator system that produces a +20 V line from the +30 V line entering at pin 1. This locally referenced h.t. line is stable with low noise content, and is used on the varactor controlled oscillators and shaper networks.

Similarly, IC2b produces a -13.3 V regulated line from the -15 V line entering the board at pin 4.

3.11.2 Frequency divider and pulse generator — AA2

Circuit diagram — Fig. 7.11

The 10 MHz signal, at a nominal level of 0 dBm, enters at pin 9. TR1 raises the signal level for t.t.l. working (i.e. 2 V peak-to-peak).

IC1 divides the signal by 10 to produce a 1 MHz signal which is fed, via gate IC2b and pin 5, to AA6 where it phase locks the 204 to 316 MHz master oscillator in 1 MHz increments.

The 1 MHz signal is also fed via isolating buffers IC2c and IC2d to the second ÷ 10 stage IC3. The resultant 100 kHz signal turns on TR2 which forms a very fast negative-going step at its collector. This step activates tuned circuit C6, L3 producing a raised cosine pulse shape at the collector of TR3. The fast pulse is applied to transformer T1 which produces a balanced drive at output pins 7 and 8.

The output signal is fed to the sampling gate on AA3, and causes the 4.8 MHz oscillator to phase lock in 100 kHz increments.

C2, L1, C3, L2 and C4 form decoupling networks necessary to prevent amplitude to phase modulation in the divider chain.

3.11.3 4.8 MHz interpolating oscillator — AA3a and AA3b

Circuit diagram — Fig. 7.12

L1 and TR1 on AA3b form a Hartley oscillator. Varactor diodes D2, D3 and D4 tune the frequency of the oscillator by ±1 MHz. Diode D1, biased by R3 and R4, limits the amplitude of oscillation to a constant level. The output of the oscillator is taken from the tap on L1, buffered by emitter follower TR2, and leaves AA3b at pin 3.

TR2 on AA3a is a shunt feedback stage taking the current from R9 on AA3b and converting it to a low impedance output voltage of 1.5 V peak-to-peak.

The signal is further isolated by passing it through shunt feedback stage TR4 and complementary emitter followers TR5, TR6. These form a symmetrical low impedance output stage to couple the signal via C19, C31, R61 to the sampling gate bridge IC3. The bridge is driven by the balanced signals from AA2 entering at pins 13 and 14. The self-rectification action of C20, C24, R38, R39, in conjunction with the diode bridge, form the correct bias level.

If a step function input signal is applied across R37, the input to the sampling gate, memory capacitor C23 will not charge to the full amplitude in the period of time of one sampling pulse. This is because of the finite resistance of the turned-on diodes. The ratio of C22 and C23 is chosen so that this error in the sampled amplitude is countered by feedback action around the feedback loop of IC4 during the interval between the sampling pulses. By correct choice of the capacitance ratio, the output reaches the correct amplitude of the input signal in one sampling interval, i.e. 10 μs.

The sampled signal is fed to search oscillator and amplifier IC5. When the loop is in the phase locked condition, IC5 acts as an amplifier to the loop signal. In the absence of phase lock, positive feedback around R43, C26, R42, C25 turns IC5 into a Wien bridge oscillator, oscillating at approximately 7 Hz, 2 V peak-to-peak. Diodes D1 and D2 limit the amplitude of oscillations.

The sinusoidal output of IC5 ensures that the oscillator on AA3b sweeps through one of the phase lock points, and the loop obtains lock; the overall negative feedback action round the loop inhibiting any further oscillations at 7 Hz within IC5 stage.

The signal is applied to summing amplifier IC6, where the potential on the slider of the ±1 MHz reference frequency control enters the board at pin 12, and is summed. The amplifier output is shaped by diodes D3, D4 and coupled, via emitter follower TR7, lead lag filter R49, R50, C30, and pin 11, to AA3b. Here it controls the frequency of the 4.8 MHz voltage controlled oscillator.

TR2 (on AA3a) output is also fed to balanced modulator IC1. A second input to IC1 is taken from TR1 (AA3a) via test point 1. The signal at the collector of TR1 (AA3a) is an amplified version of the difference frequency which arrives from the ring bridge mixer on AA5 at pin 6. The output of IC1 is fed via pin 16 to control the 200 to 310 MHz slave oscillator on AA5.

After phase shifting by 90^{o} at TR3, the signal from TR2 (AA3a) collector is again compared with that at TR1 (AA3a) collector by balanced modulator IC2 to produce a phase lock 'check' signal. This signal is positive when the correct phase lock has been obtained, and negative should the oscillator have locked on to the unwanted sideband.

3.11.4 3.6 MHz master second local oscillator - AA4a and AA4b

Circuit diagram— Fig. 7.11

TR1 on AA4b and its associated circuit form a Colpitts oscillator which produces the variable part of the second local oscillator system. Varactors D2, D3 and D4 tune the oscillator over the range ±150 kHz around 3.4 MHz, and are driven from the shaper circuit on AA1. Biased diode D1 stabilizes the amplitudes of oscillation.

The output of the oscillator is taken from between C2 and C3 of the tuned circuit, and is coupled via emitter followers TR2 (AA4b) and TR2 (AA4a) to IC1 (AA4a) which is a balanced modulator. The second input to IC1 is fed via C9 from the collector of TR1 (AA4a). This signal is the difference frequency of the 236.6 MHz oscillator on AA7 and the reference frequency at 240 MHz.

The two signals are compared by IC1 which produces the phase locked 'control' signal that is taken via pin 14 to control the 236.6 MHz oscillator on AA7.

As with board AA3, the 3.4 MHz oscillator signal from TR2 (AA4a) is 90^{o} phase shifted at TR3, and applied to balanced modulator IC2. This is also compared with the difference frequency of the 236.6 MHz oscillator, and the 240 MHz reference frequency, to produce a phase lock 'check' signal. This signal is either positive if the correct sideband has been locked on, or negative if the incorrect sideband has been locked on. The signal is fed via pin 15 to the stoppable search oscillator on AA7a.

3.11.5 200 to 310 MHz slave first local oscillator - AA5 and AA5a

Circuit diagram - Fig. 7.13

TR1 (unit AA5) with associated circuit, forms a varactor tuned Colpitts oscillator. The amplitude of oscillation is limited by back to back diodes D2 and D3. The output of the oscillator is taken via C17 and buffer TR2, TR3 to an isolating buffer.

The unit contains four isolating buffers, consisting of transistor pairs, TR6 and TR7, TR8 and TR9, TR4 and TR5.

Isolating buffer TR4, TR5 drives the ring bridge mixer on board AZ2. This compares the slave and master oscillators and produces an output difference frequency which is fed to AA3.

The first local oscillator output drive of buffer TR6, TR7 is coupled via C40 to drive the first signal mixer on AB9; and first local oscillator output of buffer TR8, TR9 is taken via C48 to drive the tracking generator output signal mixer on AC1.

The control signal to oscillator TR1 (unit AA5) is coupled via lead lag filter R26, R27, C51, pin 1 on AA5a and r.f. filter L1, R14 from its entry at pin 7 (AA5a). The signal is derived from the phase comparator on AA3a.

Should the phase locked loop be not locked, or locked onto the incorrect sideband, the signal entering pin 9 (AA5a) will be zero or negative. This cuts off TR1 (AA5a) and its collector voltage becomes +5.5 V. This unbalances long tailed pair TR2, TR3 so that diodes D1 to D4 are reverse biased. This permits IC1 to oscillate at approximately 7 Hz, its amplitude limited at 25 V peak-to-peak by the feedback action of R12, C2, R11, C1 which form a Wien bridge feedback network.

This circuit will continue to oscillate, thus sweeping the varactor tuned oscillator over its range, until the correct phase lock has been acquired. When this occurs, a positive voltage enters at pin 9 turning on TR1, and reversing the state of long tailed pair TR2, TR3 so that the diode bridge is now fully forward biased. This puts a very low impedance between IC1 pin 3 and earth, and stops the feedback action of Wien bridge oscillator IC1.

3.11.6 205 to 315 MHz master first local oscillator AA6, AA6a and AA6b

Circuit diagram - Fig. 7.14

This is a combination of units previously described. The Colpitts oscillator TR1 (unit AA6) is identical to that on AA5. The buffer units, TR2 to TR7, are identical to those on AA5. The slow sampling gate, and the search oscillator and amplifier are the same as those on AA3.

The 1 ns pulse generator comprises step recovery diode D1 (AA6b) which is driven by transistor switch TR1 (AA6b). TR1 is driven by the rectangular 1 MHz waveform from AA2. The fast pulse produced by D1 is coupled via unbalanced to balanced transformer T1, and a.c. couplings C7, C8 to the fast sampling bridge D2 to D5.

The fast sampling gate (AA6b) is self biased by the action of the diode bridge, the time constant for the rectification circuit being effected by R5, C7, R6 and C8. Capacitors C9, C10 form a positive feedback divider. This ensures that the inadequacy of the charge obtained by C10, in the sampling period due to the finite resistance of the diode bridge, is made good by positive feedback action round IC1 during the interval between sampling pulses.

The output is taken via r.f. filter L17 to AA6a where it is re-sampled in the slow sampling gate at 1 MHz.

The slow sampling gate has large value, memory capacitor C8, which minimizes the amount of 1 MHz ripple at the gate output. This in turn reduces the amount of 1 MHz sideband on the final oscillator.

3.11.7 236 MHz slave second local oscillator AA7 and AA7a

Circuit diagram - Fig. 7.15

This is similar to AA5, except that the first local oscillator becomes the second local oscillator, board connections are with AA4a instead of AA3a, and x3 multiplier TR10 is added.

The 80 MHz reference signal from AB3 is applied to the base of TR10 which greatly distorts the signal. The collector incorporates tuned circuit L17, C55 which resonates at 240 MHz. This stage is a x3 multiplier which produces the 240 MHz reference signal.

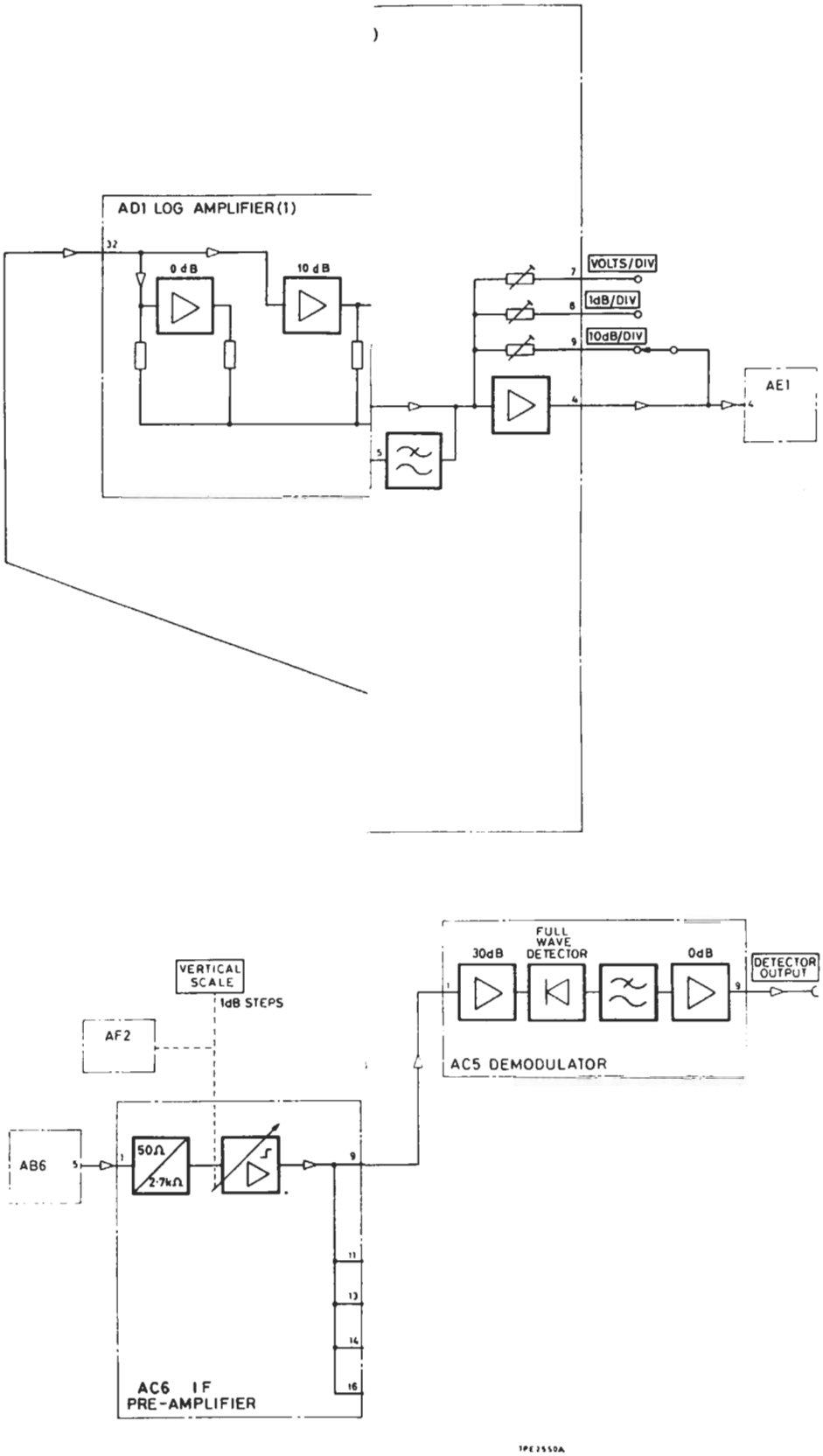


Fig. 3.12 Block diagram — Logarithmic am

3.12 200.2 MHz IF AMPLIFIER FOR TRACKING GENERATOR SIGNAL—AC1 30 Hz to 110 MHz OUTPUT AMPLIFIER FOR TRACKING GENERATOR SIGNAL—AC2 and AC2a

Circuit diagram—Fig. 7.7

Block diagram—Fig. 3.10

The fixed frequency of 36.4 MHz from AB1 is fed to input balanced mixer AZ1. The mixer is driven by second local oscillator AA7 at 236.6 MHz ±160 kHz, and the required mixer output of 200.2 MHz ±150 kHz is fed to the emitter of TR1 via R1, C1. Inductors L1, L3, L5 tune the four stage i.f. amplifier AC1 to 200.2 MHz, and provide rejection at the mirror frequency of 273 MHz.

Signal input to output balanced mixer AZ2 is taken from the collector of TR4. The mixer is driven by first local oscillator AA5 via matching buffer TR5. Output of the mixer X port is fed via the low-pass filter on AC2 to the base of TR1 on AC2a. The signal level is at -30 dBm, at a frequency of 0 to 110 MHz depending upon the setting of the first local oscillator.

The output amplifier on AC2a consists of transistors TR1, TR2, TR3, TR4 which form a series shunt feedback stage, followed by balanced output stage TR5, TR6. R19 is adjusted to produce zero d.c. component on the output signal at TR5 collector which is taken to the tracking generator output socket. R26 provides 50 Ω source impedance for the signal. The output at TR6 collector is used to drive frequency counter front end AG1.

Components C14, C15, L1, L2, C11 provide frequency response compensation. C9, R14, R16, C10, R15, R17 determine the low frequency roll-off characteristic.

Because the coaxial lead carrying AC2a output is routed via panel plugs and sockets, small compensating capacitors are added to these connectors to minimize mismatch and improve the h.f. frequency response.

3.13 DETECTOR AND EXTERNAL REFERENCE SIGNAL AMPLIFIER—AC5

Circuit diagram— Fig. 7.16

Block diagrams —Fig. 3.10 and Fig. 3.12

This board provides two functions :

External standard

This section converts an external 1 MHz standard input frequency to a 10 MHz standard which replaces the instrument's internal 10 MHz standard. Input is via the external standard socket on the rear panel.

The external 1 MHz standard is fed to emitter follower TR1 via pin 3 and C1. Output of TR1 is taken to tuned amplifier TR2. This amplifier is tuned to 1 MHz by L1 and C2, and ensures that the circuit does not respond to other input frequencies.

Tapped output of L1 is fed to emitter follower TR3 which drives Schmitt trigger TR4, TR5. The 1 MHz square wave output of TR4, TR5 is taken to shaper TR6 which in conjunction with C6 and R16 provides a differentiated input at the emitter of TR7. This causes tuned circuit C7, L2 in TR7 collector to resonate at 10 MHz. The output of the tuned circuit is routed to AB4 via emitter follower TR17, and attenuator pad R59, R60.

TR8 is switched by output of TR6, fed via R18, C9, and turns off the internal 10 MHz standard on AB4 via pin 7.

TR10 is switched on when TR6 is driven due to the d.c. voltage drop across R15, R56, which is smoothed by C8, and causes LP7 to illuminate.

Detector

This section provides audio monitoring of a.m. transmissions displayed by the instrument.

AM signal input from AC7 is fed to emitter follower TR11 via pin 1 and C10.

Output of feedback amplifier TR12, TR13 is taken to transistors TR14, TR15, TR16 which, with diode bridge D3 to D6, form a full-wave detector. Detector output is developed across R39 and fed to balanced to unbalance amplifier IC1.

IC1 output, which contains carrier frequency, is passed to an active low-pass filter formed by feedback amplifier IC2, with associated circuit. The cut-off point of the filter is 30 kHz. Audio output of the filter is fed to the detected output socket on the rear panel, via R48 and pin 9.

3.14 SWITCHED GAIN AMPLIFIER—AC6

Circuit diagram—Fig. 7.8
Block diagram—Fig. 3.12

The main function of this board is to maintain the overall analyser gain constant when the bandwidth is changed. As each bandwidth filter is selected, changes in gain are compensated by the selection of an appropriate amplifier.

Input of 100 kHz is taken from AB6 via pin 1, and coupled by matching transformer T1 to TR1 base. TR1 to TR5 are cascaded series feedback amplifiers. R2 and R4 in TR1 collector are switched by the vertical scale control so that the gain of the instrument is changed to a 1, 3, 10 sequence, instead of a 10 dB sequence, when using the volts/division mode.

The gains of amplifiers TR2, TR3, TR5 are preset to either 0 or 10 dB, and TR4 to 0 or 7 dB, by variable resistors in their emitters. Each collector load is shunted by a resistor which is switched by diodes D3 to D9. The diodes are controlled by d.c. commands on pins 4 to 7 which are connected to the 0 to 9 dB vertical scale control.

The final gain of each amplifier is determined by logic signals from AF2 (pins 18 to 21), and the setting of the vertical scale 0 to 9 dB control.

For example : with the 0 to 9 dB control set at 0 dB, the collector load of each stage is unshunted, and a '1' state at pin 21 produces an amplifier output of 10 dB; a '0' state gives a 0 dB gain.

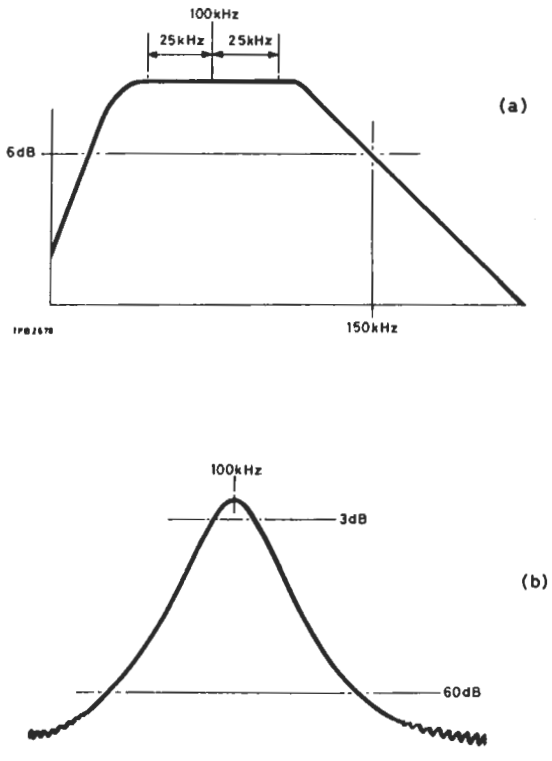
Outputs to bandwidth filters AC3, 4, 7 and 8 are diode switched via D11 to D15, and diodes on the relevant boards, by control signals from AF2.

3.15 LOW-PASS FILTER—AC7

Circuit diagram—Fig. 7.17
Block diagram—Fig. 3.12

When 50 kHz bandwidth is selected, the output of AC6 is diode switched on command from AF2 to TR1 base via D4.

TR1 is a series feedback amplifier whose collector contains a low-pass filter, tuned by L1, L2 to the response curve shown in Fig. 3.13(a). The front panel gain control is connected to TR1 emitter via pin 12, and sets the overall amplifier gain.



	f_3 (3dB)	f_{60}(60dB)
AC3	5	40
AC4	50	400
AC8	500	4k
	5k	40k

Fig. 3.13 Response curves of 100 kHz filters

Output is fed via isolating transformer T1 to logarithmic amplifier AD1 (pins 10, 11). Output is also fed (pin 15) to demodulator AC5.

3.16 500 Hz and 5 kHz BANDWIDTH, 100 kHz FILTERS—AC8

Circuit diagram—Fig. 7.17
Block diagram—Fig. 3.12

This board contains two filters :

With 5 kHz bandwidth selected, AC6 output is diode switched to TR4 base via D9. This filter consists of two stages, TR4 and TR5, which are coupled by a pair of band-pass filters. The band-pass filters are tuned to 100 kHz by L5, L6 (see Fig. 3.13(b)). Overall gain is set to 7 dB by R31.

The collector of TR5 contains a further pair of band-pass filters, tuned to 100 kHz by L7, L8.

Output (pin 12) is diode switched on command from AF2 via D11 to AC7.

With 500 Hz bandwidth selected, AC6 output is switched via D4 to the base of TR1. Transistors TR1, TR2 and TR2, TR3 are coupled by pairs of band-pass filters inductively tuned to 100 kHz.

Overall amplifier gain is set to 10 dB by R12 in the emitter of TR2. Output is fed to TR4 via diodes D5, D8 when the command signals at pins 7 and 8 are calling the 500 Hz filter.

3.17 50 Hz BANDWIDTH, 100 kHz FILTER—AC4

Circuit diagram—Fig. 7.17
Block diagram—Fig. 3.12

When 50 Hz bandwidth is selected, AC6 output is diode switched via D4 to TR1 base. Transistors TR1, TR2 are coupled by band-pass crystal filter pair XL1, XL2; TR3 and TR4 are similarly coupled by XL3, XL4. See Fig. 3.13(b) for response curve.

R8 in the collector of buffer TR1 varies the skirt response of crystal filter XL1, XL2. R17 in the collector of TR3 similarly varies the skirt response of XL3, XL4.

TR5 is a series feedback amplifier set to give an overall gain of 10 dB by R27.

Output of AC4 (pin 8) is diode switched on command from AF2 via D6 to AC8.

3.18 5 Hz BANDWIDTH, 100 kHz FILTER—AC3

Circuit diagram—Fig. 7.17
Block diagram—Fig. 3.12

Selecting 5 Hz bandwidth switches AC6 output via D5 to the base of TR1. TR1 and TR2 are coupled by 100 kHz band-pass crystal filter pair XL1, XL2; TR4 and TR5 are similarly coupled by XL3, XL4. See Fig. 3.13(b) for response curve.

R9 in the collector of buffer TR1 alters the skirt response of XL1, XL2. R20 in the collector of buffer TR4 alters the skirt response of XL3, XL4.

Emitter follower TR2 feeds the signal to the base of series feedback amplifier TR3. Emitter follower TR5 feeds series feedback amplifier TR6. R29 in the emitter of TR6 sets the overall amplifier gain to 10 dB.

Trimmer capacitors C8, C10, C18 and C20 provide fine frequency adjustment of the crystal filters.

3.19 OVERALL DESCRIPTION OF THE LOGARITHMIC AMPLIFIERS—AD1 and AD2

Block diagram—Fig. 3.12

The logarithmic amplifier operates at a centre frequency of 100 kHz, and contains a number of limiting amplifiers in cascade. The output of each amplifier is current summed, and then detected to produce a logarithmic output.

The amplifier consists of two main sections; nine 10 dB gain amplifiers plus one unity gain amplifier provide the 100 dB dynamic range for the 10 dB/division mode, and four 2.5 dB gain amplifiers produce the 10 dB range required for the 1 dB/division mode.

In the 1 dB/division mode, the signal is amplified approximately 30 dB by three 10 dB amplifiers in the main chain on AD1, and fed to four 2.5 dB amplifiers on AD2. The amplifier outputs are current summed, selected by the vertical scale control, converted to voltage, detected and then passed via an operational amplifier to the digital store.

In the 10 dB/division mode, the first amplifier on AD1 is current summed separately from the other 10 dB amplifiers, and the last two amplifiers (on AD2) are summed separately depending upon the mode of operation.

When the spectrum analyser is used on wide bandwidths, the automatic programming of the instrument does not permit the full resolution of the 100 dB range because of the noise level of the receiver section. In this mode, good linearity to the bottom of the screen is not important as it is always drowned by noise. Fast response of the logarithmic amplifier is, however, important because only a few cycles at 100 kHz are available on some sweeps for the signal to be recognized and measured. In this mode, designated 'fast', output of the last two 10 dB amplifiers is routed through a diode switch, which is controlled by AF2, and fed to the main current summing bar. The output is then routed via the vertical scale control to be detected and passed to the digital store.

On the narrower filter positions, notably at 500 Hz, 50 Hz and 5 Hz, the response time of the logarithmic amplifier is not important because many thousands of cycles are present as the instrument sweeps through each spectral line.

To improve the linearity of the logarithmic amplifier display on the screen, output of the last two 10 dB amplifiers is separately converted and detected by an auxiliary detector. The output is then low-pass filtered to reduce the noise content before being current summed, together with the output of the other eight 10 dB amplifiers.

3.19.1 Logarithmic amplifier – AD1

Circuit diagram— Fig. 7.18

Limiting amplifier TR1 is a shunt feedback stage with unity gain, and is not cascaded with the main amplifier chain.

Diodes D3, D4, D5, D6 form a current limiting bridge which limits the output voltage swing at the collector of TR1 to 4 V peak-to-peak.

TR1 output is taken via R12 to TR2 emitter. TR2 collector output is fed to the current summing lead. A fraction of the input signal is taken via R3 and R6 to TR2 base; this provides part of the current of the overall current summing necessary to produce the correct logarithmic shape.

Transistors TR3, TR4 form a low noise amplifier at the start of the cascade chain. The amplifier is similar to TR1 except that it has a gain of 10 dB.

R1 and diodes D1, D2 maintain the input impedance approximately constant at higher levels of input signal.

Output of TR3, TR4 amplifier is taken via R16 to TR2 emitter, and is current summed in TR2 collector.

Amplifier IC1a is a shunt feedback stage similar to the first two stages. The diode bridge is, however, replaced by a diode pair, and the circuit values are arranged so that in the absence of an input signal, the current through diode D11 equals the current through D12. This is effected by providing current through D11 via negative feedback loop R21, R22; this allows symmetrical limiting of any sinusoidal signal applied. If limiting of the previous stages has been asymmetrical, the d.c. coupled negative feedback loop operates to minimize the error.

The signal path is coupled via C9, and the gain at 100 kHz is determined by the ratio of R25 and R26 to R22. Capacitor C11 reduces the high frequency response to avoid overshoots on previously limited signals. Resistor R25 sets the overall gain of the first three amplifiers to 30 dB.

The output voltage is divided by R28, R29, and converted to current by IC1b. The current is then summed with the previous stages.

The fourth amplifier IC1c is similar to IC1a, except that variable gain adjustment is not provided. The output is taken in current form via C15 and R35 to IC1b to be summed.

The remaining four amplifiers are similar to IC1c. All perform identically, each limiting its output to 4 V peak-to-peak, with a gain of approximately 10 dB.

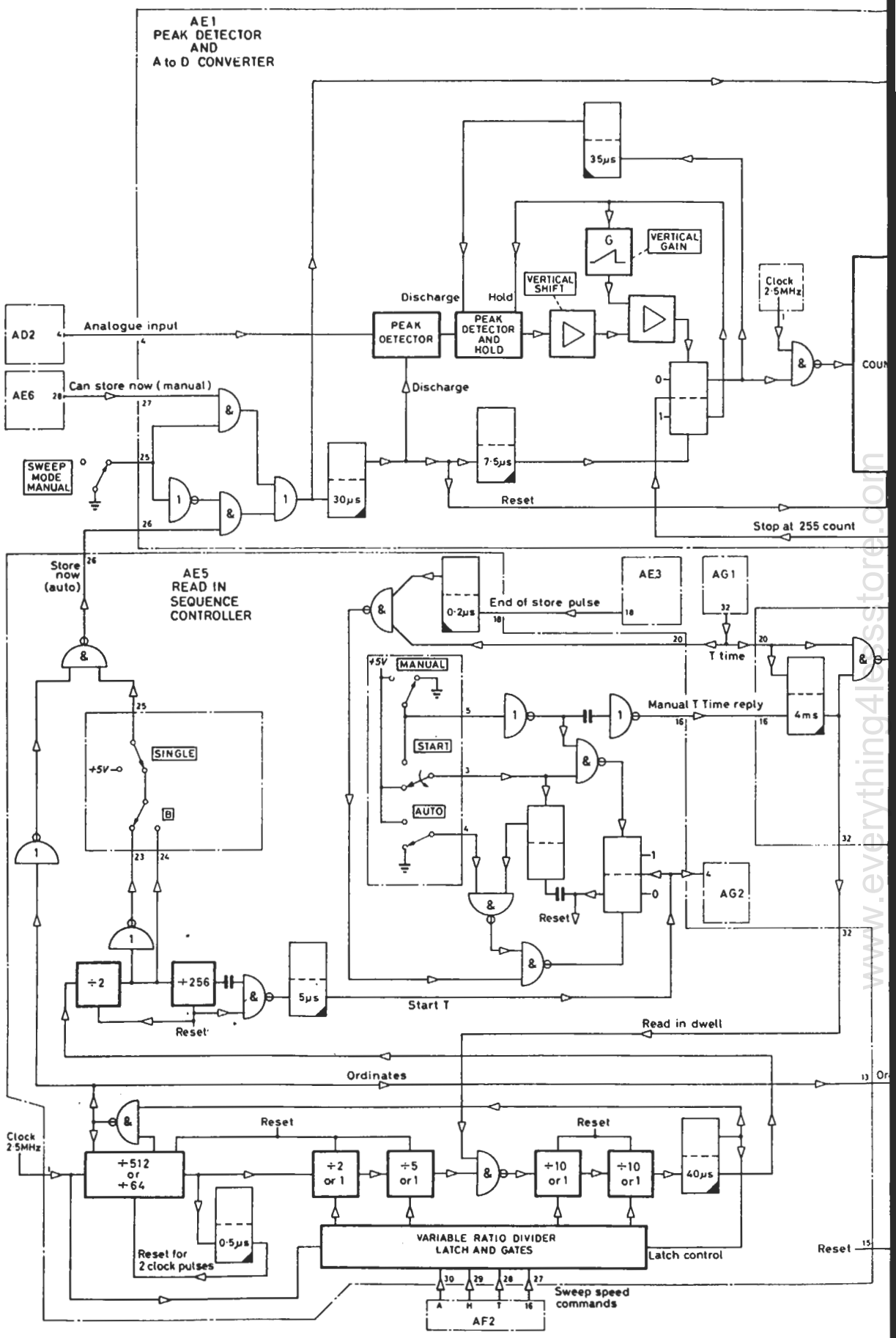
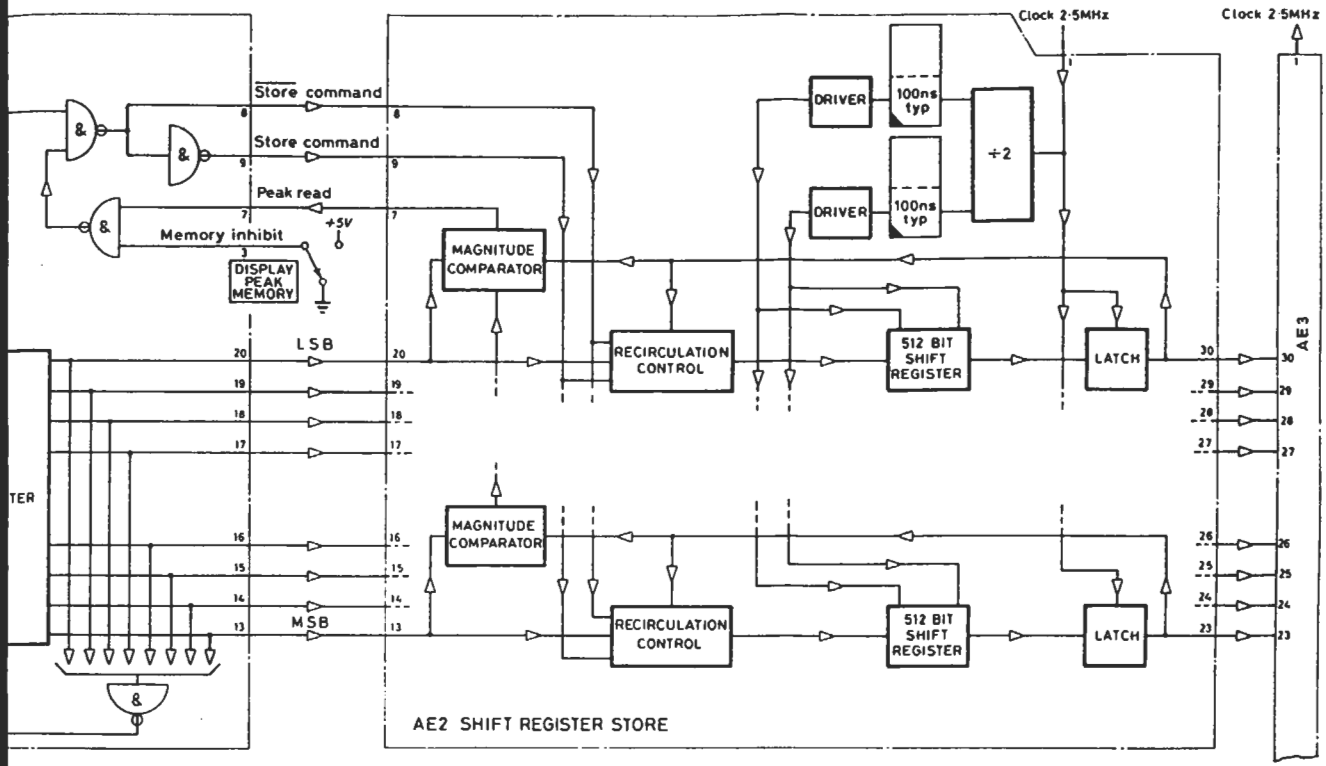
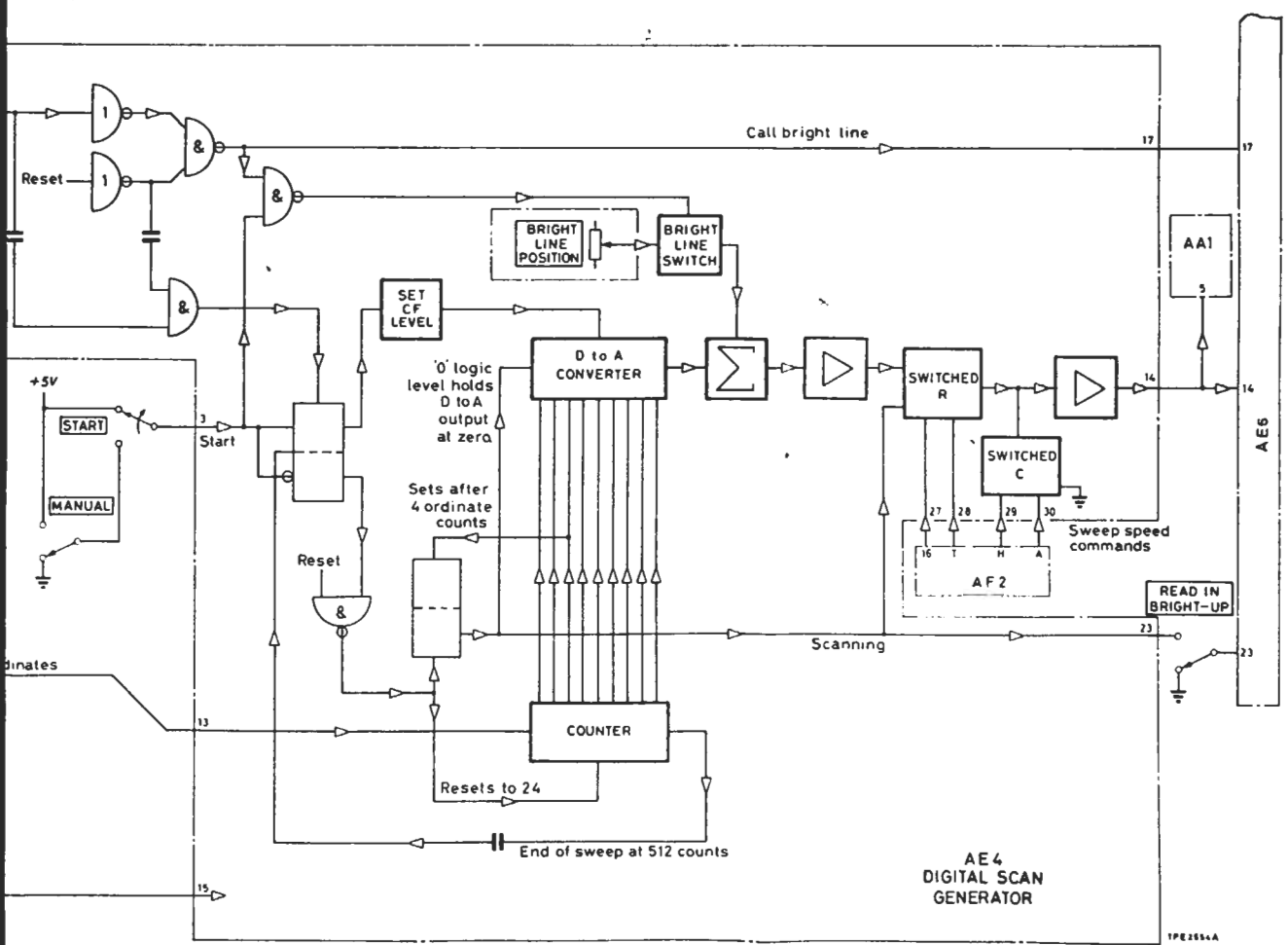


Fig. 3.14 Block diagram — Digital store (part 1)





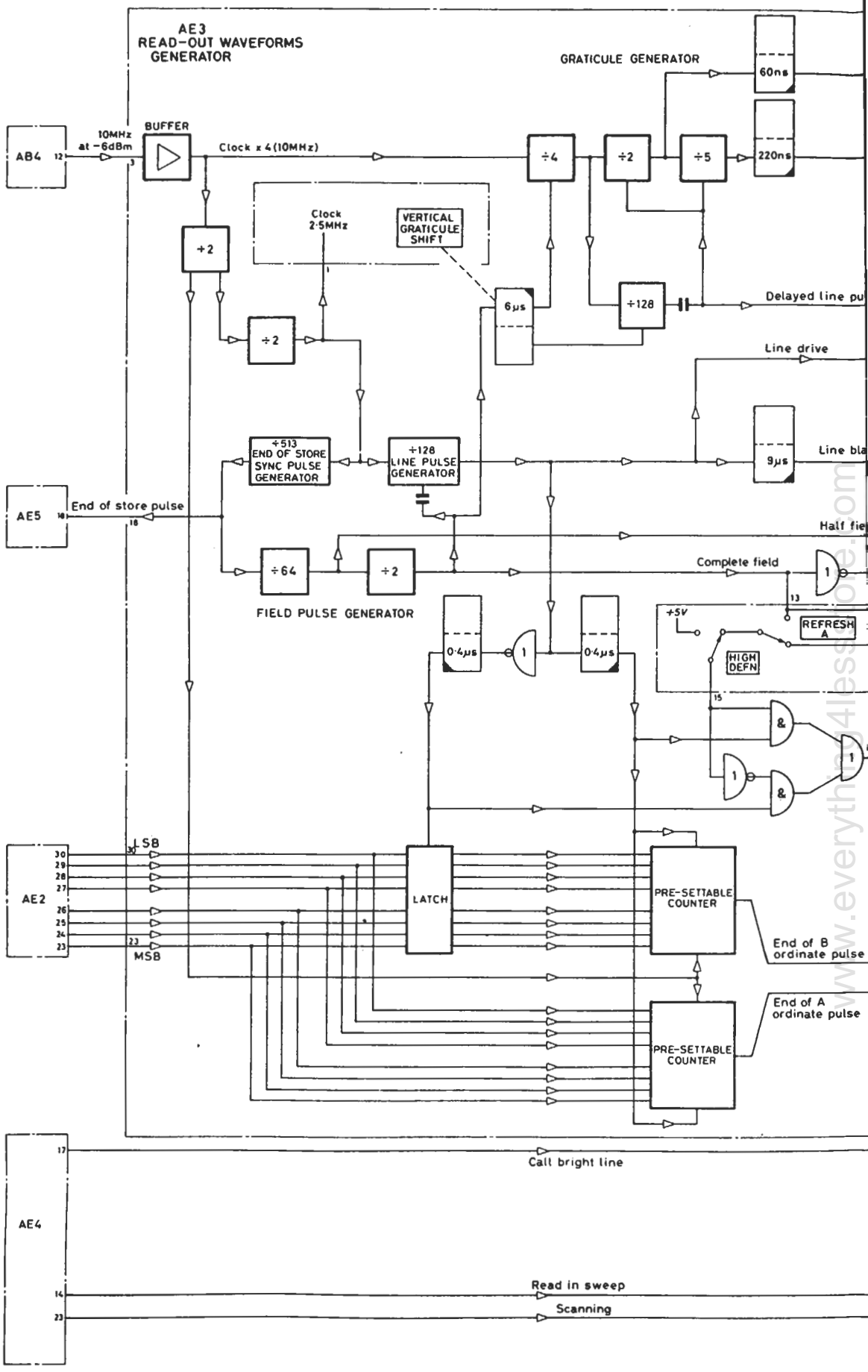
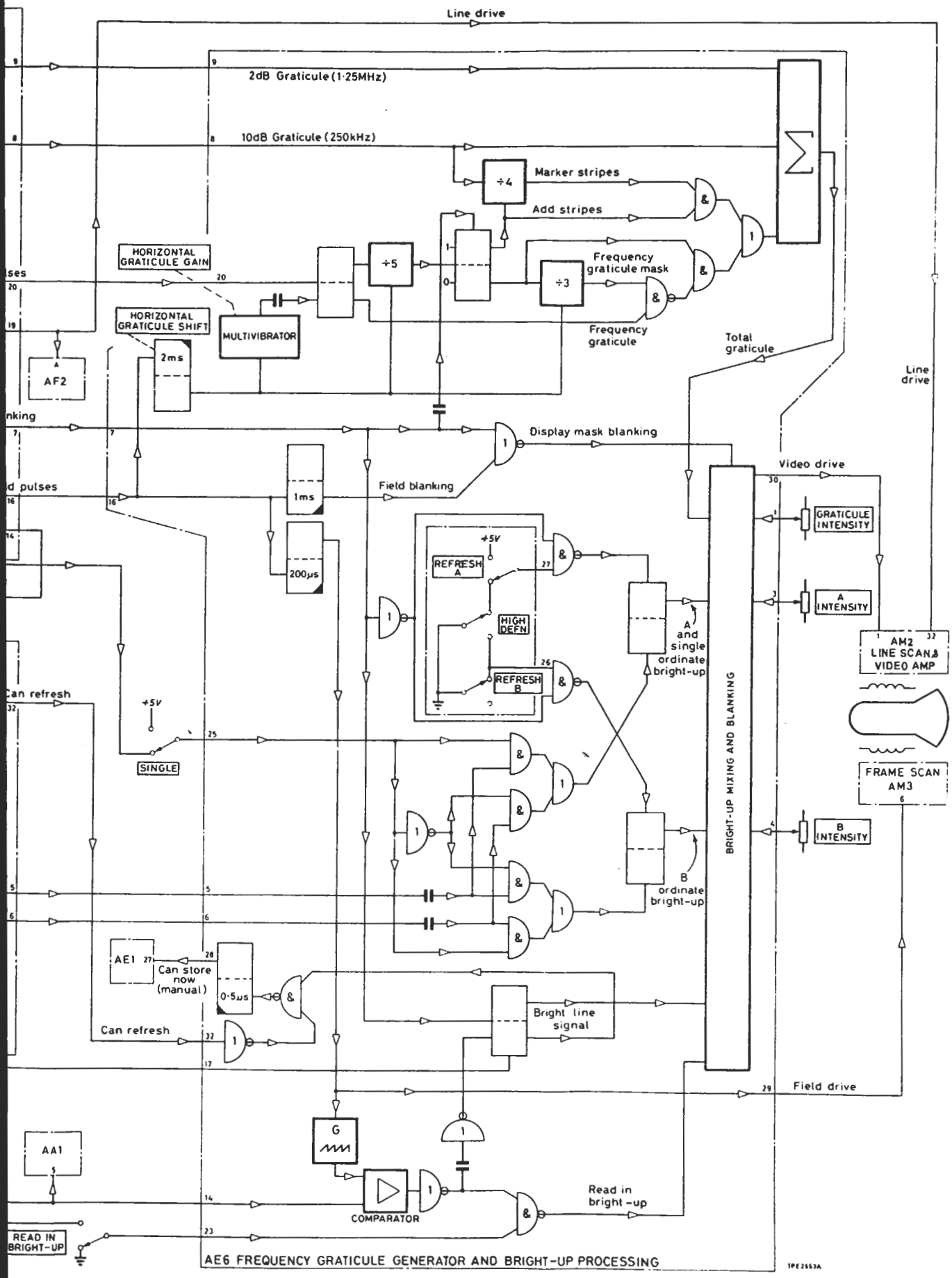


Fig. 3.15 Block diagram — Digital store (part 2)



AE6 FREQUENCY GRATICULE GENERATOR AND BRIGHT-UP PROCESSING

TPE2552A

Output of IC2a is fed, via R62, C28 and pin 1, to the detector on AD2 so that when volts/division is selected, a linear response is obtained on the display screen.

Output of the seven amplifiers is fed via pin 13 to AD2, where it drives the last two 10 dB amplifiers in the chain. The summed current leaves at pin 3, and is taken to the front panel switching.

3.19.2 Logarithmic amplifier—AD2

Circuit diagram— Fig. 7.18

Integrated circuit IC3 forms the last two 10 dB amplifiers, which are cascaded together at the end of the amplifier chain on AD1. The amplifier output of AD1 arrives at pin 13, and is fed to IC3a. The summed current at pin 14 of IC3b is taken via pin 15 to the front panel switches.

If the 10 dB/division mode is selected, the summed current is routed to input pin 1, and flows either through D13 or D14 depending upon the control voltage at pin 29.

With a control voltage of +15 V, the summed output is routed through D14, C27, R62, R64, and develops a voltage at the input of long tailed pair IC4b, which with TR2 forms the auxiliary detector.

If the control voltage is -6 V, the summed output flows via D13 into the current summing bar common to all amplifiers. The signal is then routed, via the front panel switches and input pin 6, to drive shunt feedback stage IC4a. Here, the summed current is converted to a summed voltage. The summed voltage is coupled via C29 to main detector IC4c.

The main detector output is fed either direct to IC5, and thereby out to the digital store, or when the sweep mode manual button is operated earthing pin 5, via low-pass filter R73, C35.

Output of the auxiliary detector produces the d.c. level at the input of the main detector, permitting both detector outputs to be summed.

IC1 and IC2 form four 2.5 dB amplifiers which comprise the 1 dB/division logarithmic amplifier. The amplifiers function the same as the 10 dB amplifiers on AD1, and differ only in the values of certain components.

Resistor R5 samples the input signal, and provides an amount of current to the current summing bar which enables the production of a correct logarithmic shape.

Emitter follower TR1 prevents R3 loading the output stage of amplifier IC1c on AD1, and thus retains the correct logarithmic law when switched to 10 dB/division.

The auxiliary detector IC4b, TR2, contains a feedback loop, which ensures that the voltage at pin 4 of IC4b always equals the voltage applied to pin 2, IC4b. Any fast positive-going signals at pin 2, IC4b, are followed at pin 4, IC4b, because TR2 is able to charge C30 to its correct value quickly. Negative-going signals at pin 2, however, are not followed at pin 4 because of the long time constant of C30 and R67. The circuit is a peak detector operating in the positive direction. Output is passed via R69 to IC4c.

R69 and C29 form a low-pass filter which reduces the noise content of the auxiliary output.

The summed voltage signal at the collector of IC4a is coupled via C29 to IC4c. Thus, the output of the main detector is the sum of the d.c. signal fed from the auxiliary detector, and the peak positive potential of the a.c. component of the signal coupled via C29.

If the manual sweep mode button is not pressed, pin 5 is open circuit, and R73, L1, C33, C35 couple the signal at TR3 collector to amplifier IC5. IC5 output is fed to the digital store via pin 4. The time constant of C31, R72 is short so that the signal at TR3 collector has considerable ripple at 100 kHz imposed upon it. The peaks of this ripple are the correct amplitude, and the peaks of these signals are passed to the digital store.

When the manual sweep mode button is pressed pin 5 is earthed, and C33 greatly increases the detector time constant. This produces an accurate peak representation of the signal at TR3 collector. R73 and C35 form a low-pass audio filter. L1 eliminates parasitic oscillations in the main detector due to long lead length between pin 5 and the front panel. R75, R76, R77 are adjustable gain controls which allow the calibration of 10 dB/division, 1 dB/division and volts/division modes, respectively.

Signal transfer between the logarithmic amplifier (pin 4), and the digital store is achieved between the levels 0 V and +2 V d.c.

In the volts/division mode, no voltage input corresponds with 0 V d.c. output. In both logarithmic modes, however, the zero output condition corresponds to a finite a.c. signal into the detector and must, therefore, be backed-off by input offset potentials. This is effected in the 1 dB/division mode by potential divider R52, R55. Divider voltage is switched via pin 26 to produce the bias input potential for the auxiliary detector. R25 on AD1 adjusts the gain of the amplifiers preceding the detector so that with the correct level of input signal, zero volts can be obtained at the detector output.

In the 10 dB/division mode, the bias potential is adjusted by potentiometer R56. The bias voltage is switched via pin 26 as above.

3.20 OVERALL DESCRIPTION OF THE DIGITAL STORE—AE1 to AE6

Block diagrams—Fig. 3.14 and Fig. 3.15

The store consists of eight 513 bit shift registers which store a maximum of 513 eight bit words. The information is arranged so that 513 frequency points can be stored, and on each point one of 256 levels. Before entering the store, information is converted to digital form, and then passed to the re-circulating shift register for storage.

Digital information taken from the store is converted into a time function, which in turn is converted to a bright line on the display tube, the length being proportional to the stored value.

A 2.5 MHz standard clock frequency is generated, and an 'end of store' pulse is produced which occurs in synchronism with the store, every 513 clock pulses. A read-in sequence controller governs the time at which information is taken from the peak detector/digital converter and placed in the store, and is synchronized by the 'end of store' pulse.

Each time the read-in sequence controller commands the digital converter to take a reading of the input, it also passes a pulse to a digital scan controller which advances a ramp signal by one increment. This sweep is used to drive the swept oscillators.

The display is in the form of a scanned raster in which the lines are scanned vertically. Therefore, spectrum lines are brightened up raster lines.

The amplitude and horizontal graticules are generated electronically, and can be moved to fit any display after it is stored.

Organization of the store

As the store re-circulates it is possible to gain access to any one point in the store every 513 clock pulses. To enter one bit of information into the store each time the store re-circulates requires 513 x 513 clock pulses for a complete set of information. To obtain the fastest read-in, the shift register must be driven at a maximum clocking rate (i.e. 100 ms read-in requires a clock speed of 513 x 513/0.1 Hz = 2.65 MHz). In practice this will be slower due to an allowance of 10% for sweep flyback time, i.e. 2.36 MHz.

To read out the store on a television type display, it is necessary to take the element data rate from the shift register at about 15 kHz or every 66 μs. If the shift register is clocked at 2.65 MHz to satisfy the input requirements, this produces data at 0.38 μs per element which is 174 times faster than required. If the clock rate is 10% lower because of the flyback allowance, and the line scan is permitted to be as high as 18 kHz, and also the output is interlaced, a time of 0.38 x 2 x 1.1 x 18/15 = 1 μs per element is achieved. This is 66 times faster than required. To reduce this ratio to unity only 513 $\div$ 66 must be taken out, which is 7.8 elements for each two circulations of the shift register instead of 513. This is approximately equal to four extractions per shift register re-circulation, and can be achieved without the use of an auxiliary store by the encoding sequence shown in Table 3.1.

This sequence enables the 513 bits of the store to be divided into eight blocks of 64, plus one extra bit. If data enters the store every 64 clock pulses, the 8th entry will be on the 512th clock pulse. This is one bit removed from the first data entry as the store is 513 bits long. Thus after 64 repeats of this sequence the store will be full. The data readout sequence is identical except that the interval between the readout points is 128 clock pulses.

Table 3.1

Read-in/read-out sequence of shift register

Read-in		Readout
Dual	High defn.	
1A	1	1
253B	506	510
249B	498	506
245B	490	502
"	"	"
9B	18	266
5B	10	262
1B	2	258
254A	507	254
250A	499	250
246A	491	246
"	"	"
10A	19	10
6A	11	6
2A	3	2
254B	508	511
250B	500	507
246B	492	503
"	"	"
10B	20	267
6B	12	263
2B	4	259
255A	509	255
251A	501	251
247A	493	247
"	"	"
11A	21	11
7A	13	7
3A	5	3
255B	510	512
251B	502	508
247B	494	504
"	"	"
11B	22	268
7B	14	264
3B	6	260
256A	511	256
252A	503	252
248A	495	248
"	"	"
12A	23	12
8A	15	8
4A	7	4
256B	512	513
252B	504	509
248B	496	505
"	"	"
12B	24	269
8B	16	265
4B	8	261

Table 3.1 (*continued*)

257A	513	257
253A	505	253
249A	497	249
"	"	"
9A	17	9
5A	9	5
1A	1	1
253B	506	510

The fastest read-in sweep is 100 ms. To achieve this, 513 clock pulses are added to the 64 pulses in the read-in sequence. On slower read-in sweeps a variable divider introduces an extra n x 513 clock pulses in a 1-2-5 sequence. The read-in sweep time is effected by board AE5. Command signals from system control logic board AF2 are connected to AE5, dictating the sweep speed required.

The basic counter on AE5 is a 513 bit counter. It can be converted to a 64 bit counter when commanded. At the beginning of the read-in sweep a 513 bit counter is synchronized with the 'end of store' pulse from AE3. The 513 bit counter begins to count at clock frequency for a number of times depending on the sweep speed required, ranging from 1 for the 100 ms sweep to 1000 for the 100 s sweep. When the required number of counts has been performed, the counter is converted to a $\div$ 64 counter, and at the end of the 64th count an output pulse is fed to AE1 to command it to take information from the logarithmic amplifier. The counter is not re-synchronized to the 'end of store' pulse but continues to divide by 513 until it again is commanded to divide by 64. This continues until the entire store is filled.

A $\div$ 512 bit counter on AE5, counting the commands to AE1, provides the 'store full' information. When all the data has been stored a pulse is sent to AG2 of the counter unit, which informs the counter that the read-in sweep has been completed and commands it to measure the centre frequency.

At the time AE5 is commanding the frequency counter to count, a pulse is passed to a D-type bistable, the output of which resets all the counters on AE5. The counters will not start counting again until the frequency counter on AG2 has completed its measurement, and the next 'end of store' pulse from AE3 has arrived. The counters will be further inhibited if the single shot mode is selected.

Operating the start button will remove this inhibition. Also, if the manual mode is selected, counters will not start until the mode is returned either to single shot or auto.

The 'can store now' signals from AE5 are passed to AE1. AE1 consists of a peak detector and an analogue to digital converter which are controlled by logic on AE1. The peak detector stores any spectrum line occurring between 'can store now' commands and consists of two parts, one peak detecting while the other is discharged. Thus no spectrum line will be missed. The output of the peak detector is fed to an amplifier which contains the front panel vertical shift control.

The output of the amplifier is connected to one input of a comparator. The other comparator input is taken from a ramp generator. The ramp generator commences to sweep at the same time the counter on AE1 begins to count. When the comparator gives an output informing that the ramp generator is at the same amplitude as the output from the peak detector, the ramp detector and the counter are stopped. The counter outputs are then ready for passing to AE2, being the digital form of the input signal. The larger the input signal the longer the ramp generator has to run before the comparator gives the output signal.

The counter stores its outputs until it is time to pass them on to the store at the next 'store now' command. The sequence of events on AE1 when a 'store now' command has been received is (a) discharge the first peak detector, (b) hold the value in the second peak detector, set off ramp generator and counter, (c) stop the ramp generator and counter when the comparator has given its signal and (d) discharge second detector. The preset gain control on the front panel alters the slope of the ramp generator, and hence the number of counts during the run-up time of the ramp.

AE2 is normally set in the re-circulation mode, but on command from AE5 through AE1, a changeover switch on the input to the shift register is operated to read the output of AE1. The switch is held over for 1 bit-length. Therefore, 1 bit of information is fed into the shift register at the correctly synchronized time as governed by AE5.

The shift register is clocked by a two-phase clock. The clock rate is half that of the data rate because the data is multiplexed internally by the shift register integrated circuit. The shift register consists of a 512 bit m.o.s. shift register plus a one bit latch. The outputs of the latch are available for re-circulation and also as outputs to AE3.

A small additional circuit on AE2 is a magnitude comparator which is used in the peak memory mode. In this mode, information already in the store is compared with information on the outputs of AE1, and is only entered into the store if the information on AE1 is of greater amplitude.

The output of the store is taken by eight parallel lines to AE3 which, when commanded, stores it in presettable counters.

Apart from the clock amplifier and generator on AE3 there are several counters which govern the readout waveforms :

A $\div$ 128 counter divides the clock frequency of 2.5 MHz producing 19.53 kHz, which is the line frequency. This line drive is fed to the scan and video amplifier AM2 to operate the raster scan.

Also triggered from the line drive waveform is a monostable which is used for line blanking. This is a variable monostable which can be set by a trimming potentiometer.

A $\div$ 513 bit counter generates the 'end of store' pulse which, when divided by 64, produces a pulse every half field, and a further division by two produces field pulses.

A division of eight on the 10 MHz fast clock rate provides the 2 dB graticule markings, and a further division by five produces the 10 dB graticule. The width of these markings is governed by the pulse duration of two monostables. A 'delayed line' pulse is generated from this graticule counter for use on AE6. Movement of the graticule with respect to the display is achieved by inhibiting the graticule counter by the output of a monostable for a variable period starting at the beginning of a line.

As the line frequency is the clock frequency divided by 128, it is exactly the correct rate for taking information from the store. Therefore, the edge of the line drive is used to trigger a monostable which opens the preset gate on the eight bit presettable counter. The period of the monostable enables it to capture one bit of information from the store. When it has been loaded into the presettable counter, the counter immediately begins to count and produces a pulse, the timing of which depends on the number entered into the presettable counter.

As the counter will only count in the forward direction, the complement of the number in the store is entered so that the counter is full after a number of clock pulses equal to the original number in the store. The output pulse of the presettable counter is called the 'end of ordinate' pulse and is passed to AE6.

On AE6, at the beginning of a line, a D-type bistable is triggered, and the output to the video amplifier on AM2 produces a bright line. The bright line is terminated when the end of ordinate pulse from AE3 re-triggers the bistable to its '0' state.

Another signal generated on AE6 is the 'horizontal' or 'frequency' graticule. Half field pulses from AE3 trigger a monostable which is used to vary the start of the horizontal graticule. The output of the monostable triggers a multivibrator, whose period is also variable, so that the horizontal graticule can be expanded or contracted about its calibrated position.

The half field pulse also triggers a monostable used for field drive, and another monostable used for field blanking. The field blanking is mixed with line blanking in a NAND gate whose output is connected to the bright up mixing circuit.

The horizontal graticule is modified before it is displayed. The first, central and last lines are dashed, and horizontal graticules after the tenth division of frequency are blanked out. The first, middle and last lines are markers for the beginning, middle and end of the sweep. The stripes or dashes placed on them are generated by counting the 10 dB graticule lines; each dash is two lines long. The alternate black and white dashes help in the calculation of the dB level of any spectral line, enabling the user to count in 20 dB steps. The modified horizontal graticule is added to the vertical dB graticule by a NAND gate whose output feeds into the bright up mixing circuit.

A further 'bright up' signal is generated on AE6 which allows the operator to identify the point at which information is being read into the store during a sweep. This circuit is also used to produce a bright line which appears after a single sweep has been used, and the bright line used for manual recording.

Separate contrast controls are available for the graticule and the store output.

AE4 is the digital scan generator board. The board receives pulses from AE5 each time a new bit of information enters the store. These pulses are counted by a counter whose output is fed to a digital to analogue converter. The output of the converter is in the form of a fine step staircase. After the summing of a voltage from the bright line position potentiometer on the front panel, which is normally switched out during the auto sweeps, the signal is passed to an amplifier whose gain is variable so that an accurate sweep amplitude can be set.

The output of the amplifier contains staircase steps, which must be filtered before it can be used to sweep the oscillators. This is achieved by a switched RC filter whose time constant is switched depending on the sweep speed.

To eliminate filter distortion of the ramp signal, the first step of the staircase is 28 times the height of each succeeding step. The height of the step is exactly equal to the aiming potential needed to produce the required rate of change at the output. To achieve the step, during flyback the counter is reset to 24 but the analogue to digital converter is held at '0' state. After the first four counts have reached the counter the converter is released and the first staircase step is produced. As the counter is preset to 24 it reaches its maximum count of 512, 24 counts before the store is completely full, but this occurs during the flyback of each sweep so it is not displayed.

During the count of 24, the analogue to digital converter is held at a centre frequency level by gates which override the counter outputs. Thus its output is set at centre frequency level before the frequency counter is ready to count the centre frequency during the flyback of the sweeps and, therefore, a stable centre frequency voltage can be achieved.

The output of the RC switched filter is fed to an amplifier where a shift potential is applied. The output of the amplifier is then passed to the remainder of the instrument.

When set, the ramp rises from 0 to 10 V with a step on the falling edge at 5 V, the centre frequency voltage.

When a single shot has been produced and the counter has counted the centre frequency, the digital to analogue converter is switched out, and the bright line position potentiometer is switched in. The signal which passes to the bright line potentiometer control circuit also passes to the bright up mixing circuit on AE6 to allow the bright line to be displayed. The position of the bright line depends on the setting of the bright line position potentiometer.

If at any time during the sweep, or after a single shot sweep, the manual button is pressed, the digital to analogue converter is again overridden and the bright line position potentiometer is switched into circuit.

To satisfy the condition that there must be a signal from the frequency counter before the bright line potentiometer can be switched in, a 'manual T time' reply is fabricated on AE5 when the manual button is pressed. 'T time' is the pulse length from the frequency counter given while it is counting.

A further signal from AE4 is derived from its counter drive circuit, and passed onto AE6 while the counter is counting and the scan is being produced. AE6 combines this signal with the read-in point to provide artificial persistence to show where new information is being read into the store.

When the manual button is pressed, the information is read into the store at a point coincident with the bright line. When a particular raster line is being brightened up, information is being accessed from the store at that time.

To enter information at the bright line point, the bright line is detected on AE6, and the detected signal is gated with 'access' pulse to produce a 'read-in' pulse. This pulse is passed to AE1 to produce a 'manual read-in' pulse. The pulse is called 'can store now manual', and is of similar duration to the 'can store now auto' pulse produced by AE5 during the normal auto read-in sweep.

The circuit producing the bright line on AE6 consists of a ramp generator which is operated in synchronism with the field drive to the display unit. The generator produces a ramp with the same amplitude as that generated to sweep the oscillators. This is compared with the oscillator ramp, and at the comparison point the bright line is produced. The bright line coincides with the read-in point.

During normal sweeping of the spectrum analyser, the display is slightly brightened up at the beginning of a field. This 'bright up' is removed when the ramp comparator reaches its comparison point and, therefore, the display to the left of the reading point is slightly brighter than that to the right and a mock persistence is produced. This persistence can be switched out on the faster sweep by cancelling the read-in 'bright up'.

The dual store mode

To achieve the dual store mode, information is fed into the store on alternate read-in commands, and by switching between either the odd or the even commands, two separate sets of information can be stored.

If one set of information only is to be displayed during the first field scan, the readout is in the normal fashion. If, however, it continues this way during the second field scan, the interlaced picture would be that of the alternative store. To overcome this, the original information is accessed from the store, and held in a latch until the counter on AE3 is ready to process it. Therefore, both fields of the interlaced display are identical and the definition of the display is halved. Similarly if the other set of information from the store is to be displayed, the first field scan will be that taken from the latch, and the second field scan will be that normally derived from the store.

When displaying both stores simultaneously, each field displays both sets of information. This is achieved by displaying the information accessed directly from the store with information held in the latch. The information from each store has separate bright-up facilities to allow store identification.

3.20.1 Peak detector and digital to analogue converter AE1

Circuit diagram— Fig. 7.19

The two 400 ns wide pulses 'can store now manual' and 'can store now auto' arrive at input pins 27 and 26. A set of gates of IC3 form a changeover switch. The manual button on the front panel operates via pin 25, and controls the switch.

The selected pulse is routed two ways :

In one direction the pulse passes to IC4 where it is gated with signals during the peak read mode. To record only the peak signals of a sweep the peak read button is operated. The level at pin 3 then rises to '1' state (+5 V); this opens the first gate of IC4 to allow signals from AE2 to enter. If these signals are '0', the information in the store is of smaller amplitude than presented to the store at its inputs from AE1. In this case, the output on the first NAND gate of IC4 will be '1'. This, when gated with the selected 'can store now' signal, produces a pulse which is passed onto AE2 to command it to accept the new information. An inverted version of this pulse is produced by IC4c. The pulses 'store command' and 'store command' leave at pins 9 and 8, and are fed to AE2.

The second route of the selected 'can store now' signal is to monostable IC5a, which produces a pulse of 30 μs duration. This pulse discharges the first peak detector. The falling edge of the pulse fires monostable IC5b which produces a 7.5 μs pulse. This triggers J-K bistable IC6 whose outputs control four functions. Output at pin 8 opens gate IC4d to allow the clock pulse at input pin 1 through to counters IC8 and IC9. Pin 6 output is fed to the second peak detector and holds the value on the detector for the duration of the count. This output also turns off TR12 permitting the constant current through TR13 to produce a ramp across C18, which is compared with the outputs of the peak detectors. Additionally, pin 8 output triggers monostable IC7 at the end of the bistable pulse.

The bistable pulse can be terminated by either one of two ways. When the ramp generator has attained a value similar to that of the output of the peak detector, comparator IC2 gives an output which resets the bistable. However, if the output of the detector is too high, the counter reaches a count of 255 before the ramp has reached the correct value. In this condition gate IC10, at the output of the counter, detects the count of 255 and terminates the pulse by clocking the bistable.

The falling edge of the pulse of bistable IC6 triggers monostable IC7, which produces a 35 μs wide pulse that discharges the second peak detector capacitor C7. When the bistable pulse has terminated, the ramp generator is discharged and the clock gate to the counter is closed.

The ramp generator consists of a current source feeding a constant current into capacitor C18. The constant current source is a transistor (TR13) with its base voltage controlled by Zener diode D7, and its emitter current set by gain control R40. At the end of the ramp, TR12 discharges C18 and sinks the current supplied by TR13. A second variable resistor in the emitter of TR13 is the front panel vertical gain preset control.

The analogue input of logarithmic amplifier IC1 is at input pin 4, which is connected via R4 to the base of one of the transistors (TR2a) of a long tailed pair. The other base of the pair is connected to the emitter of current amplifying transistor TR5, whose base is connected to C4 on which the input voltage is stored. C4 is charged via diode D1 from p.n.p. transistor TR3 situated in a feedback loop round the long tailed pair. As the input voltage falls diode D1 is cut off and the charge is retained on capacitor C4. Thus the peak input voltage is recorded. The capacitor is discharged by a current through TR4 during the time that monostable IC5a is giving its output pulse. However, should there be an input signal during this time, the feedback loop is capable of supplying enough current to keep the capacitor charged to within 0.2% of the correct value.

The first peak detector is followed by a second peak detector. The first peak detector must keep the charge on C4 accurately when the second peak detector is being discharged, and when its output is being compared with that of the ramp generator. This time is approximately 130 μs.

The second peak detector is similar to the first but because the charge on C7 must be stored for up to 0.5 s on the slow sweeps, the components used to charge the capacitor and to detect the voltage on it must be very low leakage. For this reason, both the charging (D3) and discharging (D4) diodes are low leakage silicon types. Low leakage field effect transistor TR10 samples the voltage on the capacitor. The field effect transistor is in common drain configuration, and is followed by emitter follower transistor TR11 which further reduces the output impedance, to provide a suitable drive to the base of long tailed pair TR6a, TR6b.

It is essential to control the stability of the peak detectors. PNP transistor TR7 in the feedback loop is a shunt feedback stage which provides close current control. The rise time of the voltage on capacitors C4, C7 is limited by 100 Ω resistors (R10, R21) in series with diodes D1, D3. The emitter follower in the first peak detector, and the field effect transistor and emitter follower in the second detector are bypassed by capacitors C3, C6 which act as a.c. paths. When pin 6 of IC6 goes negative, TR7 is turned on and the second detector output voltage is held for the duration of the comparison; immediately the comparison is made C7 is discharged by TR11. The discharge is governed by the output pulse of IC7.

The output of long tailed pair TR6a, TR6b is amplified approximately twice by IC1, and a shift potential is applied by the vertical shift control on the front panel. The amplifier output is passed via a protection circuit to comparator IC2. The protection circuit (R33, D5) prevents the input to IC2 going more negative than -0.7 V; thus keeping the maximum voltage between the two inputs of the comparator at less than 5 V. The output of the comparator passes to bistable IC6 to terminate the counting period.

When the counting period is terminated, the outputs of the counter are available at output pins 13 to 20, pin 13 being the most significant bit. The digitized number is read into the store as soon as the next 'can store now' pulse triggers the input circuit. Therefore, the information is displaced by one line from the time it is recorded. This displacement is removed by moving the graticule one line to the right.

3.20.2 Shift register store AE2

Circuit diagram Fig. 7.20

This board contains the shift register memory and the drive circuit.

In order to store information in the shift register a two phase clock signal is required. Each of the eight 512 bit shift registers consist of two 256 bit registers multiplexed within the integrated circuit. The two clock signals driving the integrated circuit are 180° out of phase. The first shift register of 256 bits uses phase 1 of the clock to shift the information and phase 2 to input the information. The second 256 bit shift register uses the opposite phases. In this way information can be taken in and read out from the shift register on both phases of the clock, and the combined 512 bit shift register then has a data rate of twice the clocking frequency.

The shift register is a m.o.s. dynamic shift register where the inputs and outputs of data are t.t.l. compatible. The clock, however, is not t.t.l. compatible requiring special clock driver IC4. This is a high power two phase clock driver requiring an input pulse from t.t.l. gates, and producing the required output swing of 16 V.

The two phase input pulses to the clock driver are taken from IC2a and IC2b monostables via high current buffer IC3. The inputs to the monostables are fed from bistable IC1, which divides the standard clock frequency by two. Potentiometers R1 and R2 set the clock pulse width delivered to the shift registers. This is between 100 and 120 ns.

Inputs to the eight 512 bit shift registers are connected to IC's 7, 8, 9 and 10 which act as changeover switches. The inputs to these switches are taken from the output of the shift register chain, and from input pins which receive the stored data of the counters on AE1. The switches operate when a 'store command' is received from AE1, allowing the data stored on AE1 to be synchronously entered into the shift register. Information being re-circulated in the store is inhibited for the one clock pulse and, therefore, old information in the store is replaced by the new information as it arrives from AE1.

In order to achieve a store length of 513 bits, the outputs of the 512 bit shift registers are connected to latches IC15 and IC16. As the latches are not multiplexed, their clocking frequency must be that of the standard clock. Because the output of the changeover switches is negated, the $\overline{Q}$ output of the latches is used to re-circulate through the store. However, as board AE3 requires a negated output, the Q output of the latches is passed to AE3.

The $\overline{Q}$ output of the latches is also fed to comparators IC5 and IC6. These compare the input data with that being re-circulated in the store. If the peak memory mode is chosen, the output of the comparators is used to decide whether to read in new information or to keep that which is re-circulating in the store.

The output of the store is available at pins 23 to 30, pin 23 being the most significant bit.

As the clock drive to the store has to feed a high capacitance, special de-coupling of the power supplies is used. The +5 V line at pin 12 is divided two ways so that the logic on the board is not subjected to the large clock spikes. These are de-coupled by L1 before the clock line is connected to the main power supply.

As the negative excursion of the clock is -11 V, a separate -11 V supply is produced from the -15 V power line. This is effected by TR1.

In order to help line de-coupling, an earth plane is introduced which circles the 512 bit shift registers, and capacitors are connected directly between lines and earth at various points.

Resistors R7 to R22 provide interface between the t.t.l. and m.o.s. circuits.

3.20.3 Readout waveforms generator AE3

Circuit diagram Fig. 7.21

Input pin 3 is connected by coaxial cable to AB1. The cable carries a 10 MHz signal at a level of -6 dBm. The signal is amplified by TR1, TR2 to produce a level compatible with t.t.l. logic. Dual D-type bistable IC1 divides the 10 MHz frequency by four to produce a standard clock frequency of 2.5 MHz. This is available at output pin 1, buffered by IC2 to produce sufficient output drive.

The 5 MHz output is used by the presettable counters.

The line scan rate used by the display is directly related to the clock frequency. IC's 3 and 4 are $\div$ 16 counters connected together to divide by 128. The output of the counters, after being buffered by IC2d, is available at output pin 19 as the 'line drive' signal. The second output of the counters drives monostable IC5a which provides line blanking for the display. The period of the line blanking is preset by R8.

The square wave 'line drive' also fires monostables IC18a and IC18b, on its negative and positive edges. The monstables produce pulses of 400 ns duration. The line pulse generator is synchronized by the 'end of store' pulse at the start of each field scan so that the monostables pulses are also in synchronism with the store. These pulses are used to remove information from the store IC18a being 64 places in advance of IC18b. The advance information is stored by IC19 and IC20 which are quadruple latches. The latch output is fed to the inputs of presettable counters, IC23 and IC24. A further pair of presettable counters, IC21 and IC22, are connected to the output of the store.

Monostable IC18b opens the input to both pairs of counters just as the 'line drive' waveform begins a new line on the display. Therefore, the output of IC21, IC22 is that of an ordinate taken directly from the store, and the output of IC23, IC24 is that of an ordinate taken 64 pulses earlier.

The output of the second pair of counters is the same as that produced by the first pair during the last field scan. Therefore, in the dual store mode, the interlaced picture can consist of two identical field scans by combining the outputs of the two sets of presettable counters.

Both pairs of presettable counters are clocked at 5 MHz. This enables the count of 256 to be achieved during the line period of 128 standard clock pulses.

A pulse which is in synchronism with the recirculation of the store is produced by the 'end of store' pulse generator (IC's 11, 12, 13 and 14).

The generator is a ÷ 513 counter, produced by a standard ÷ 512 counter whose output is fed to monostable IC14, which inhibits the count for 1 count after 512 counts. The 'end of store' pulse is taken from the output of the monostable and fed to output pin 18.

As there are 513 lines per field, a division by 128 of the 'end of store' pulse will produce field pulses, and a division by 64 produces half field pulses which occur twice for each interlaced field. Field pulses are not used on other boards but are used by the front panel switches, together with their inverted form; these outputs are fed via pins 13 and 14.

Just as control pulses to the presettable counters select information from either field, the 'complete field' pulse and its inverse activate a changeover switch to select one of two pulses. The pulses feed the counters which feed in information on the manual scan mode. The selected pulse is available at pin 32 as 'can refresh' and is fed to AE6.

A further output of TR1, TR2 is fed to the graticule generator. The generator consists of IC6a, IC6b and IC7 which provide division by eight and forty. These outputs are taken to monostables IC8a, IC8b which produce the 2 and 10 dB graticule lines. The position of these lines is thus movable with respect to the start of the line scan, using the vertical graticule shift potentiometers.

The output of IC6b is also fed to counter IC9, IC10 via test point 5. The counter divides the output by 128, and is synchronized by the graticule shift monostable IC5b, to produce a pulse at line frequency, but delayed from the line frequency by the period of IC5b. The counter output is processed by R21, R22, R23, C13 to produce a pulse edge which resets the graticule generator at the start of each line, and also provides an output, at pin 20, of 'delayed line' pulses which are used by AE6.

3.20.4 Digital scan generator AE4

Circuit diagram — Fig. 7.22

The main function of this board is to provide a distortion free signal to sweep the oscillators of the spectrum analyser.

Ordinate pulses from AE5, at pin 13, are counted by a ÷ 512 counter (IC's 10, 11 and 12). The outputs of each stage of the counter are fed to a digital to analogue converter. As the counter counts the ordinates, the output of the converter rises in staircase form. The most significant digits of the converter have to be preset to obtain the correct voltage steps. To achieve this, the current through TR13, TR15, TR17 is adjusted by the settings of R23, R27 and R31.

During the flyback of the scan, the ÷ 512 counter is preset to 24, but gates of IC9 prevent this preset number reaching the converter. The gates are closed by the output signal of D-type bistable IC7b. When the counter has reached a count of 4, IC6c passes a signal to the trigger input of IC7b, whose output then changes state and opens the gates to the converter. The output of the converter rises to the count of 28 on the counter.

When the counter has reached a count of 512, the output of IC12 goes to '0' state sending a pulse via IC6f, which clocks the D-type bistable IC7a. The outputs of the bistable feed two integrated circuits. The Q output goes to gate IC8b which resets the counter to zero. The $\overline{Q}$ output feeds through IC4b to the base of TR3 via diode D3. When the output of IC4b is at '0', the potential at TR3 output drops from +12 V to 0 V. This causes the converter to produce an output which is equivalent to half the staircase height.

After a further count of 24, the counters of AE5 produce a 'reset' pulse which arrives at input pin 15. This pulse is fed two ways. It is gated at IC8b with the signal from IC7a, and also fed via IC8a to dual input NAND gate IC5b. When IC5b is open, its output turns off TR28 which causes the 'call bright line' signal to go high. This turns on gate IC5a and hence gives a '1' state signal which turns on the bright line position control described below. IC5b is only turned on if the output of IC5c is low.

The inputs to NAND gate IC5c are controlled by signal 'T time', and the output of monostable IC3 triggered by the signal's rising edge. The output of IC5c is high during 'T time', and for a time of 18 ms after 'T time'. Therefore, the bright line position control circuit is switched out during 'T time' and for 18 ms after 'T time', and no bright line is displayed on the screen.

The 'T time' monostable IC3 can be fired by two signals. The first is 'T time' which arrives at pin 20 from AG1 of the counter unit. The second arriving at pin 16 from AE5. This line carries a single positive-going pulse whenever manual is selected. The output of IC3 monostable in addition to being fed to IC5c is taken to pin 32, and routed to AE5.

The output of the converter is amplified by IC1, which incorporates variable gain control R38. The output waveform is a 5 V staircase where the first step is 28 times higher than each succeeding step, and the falling edge has a step at half amplitude.

To remove the steps of the staircase, and produce a smooth ramp, an integrator is used. As the period of the staircase can vary from 100 ms to 100 s, the time constant of the integrator is programmed by the four lines that control the sweep speed on AE5. Control lines A and B vary the integrator resistor in a 1-10-100 series, and control lines C and D vary the capacitance in a 1-2-5 series.

During flyback, the integrator is switched out of circuit by turning on f.e.t. TR19, and the capacitor is discharged quickly via the output of IC1.

The resistors of the integrator are selected by f.e.t's TR20 and TR21. The gates to the transistors are controlled by open collector integrated circuits, IC13b and IC13c. The capacitors are selected by f.e.t's TR22, TR23 and TR24. The gates to these transistors are controlled by the output voltages on the collectors of TR25, TR26 and TR27, which are in turn controlled by the control logic on lines C and D, fed via gates of IC13 and IC8.

The control lines to each of the field effect transistors in the resistance and capacitance arms of the integrator are routed via test points 10, 11, 12, 13, 14 and 15.

The signal at test point 10 is fed from TR18, which is turned off whenever the integrator capacitors are to be discharged. The control to its base is derived from IC7b which is a D-type bistable, controlling the inputs to the converter during the first count of 28 on the counter. The signal is also available at output pin 23 for routeing to the read-in bright-up switch on the front panel.

The output of the integrator is at a high impedance level and, therefore, is fed to low bias current integrated circuit IC2. Here it is amplified by a factor of 2, and a shift potential is applied through potentiometer R49. The output is set to produce a 0 to 10 V positive-going sweep, and is taken to output pin 14 for use on AE6 and sweep shaper AA1.

Three front panel controls operate from this board :

The bright line position potentiometer is connected via pin 4. This control varies the voltage of the output of the converter via transistors TR1 and TR2, whenever TR1 is not shorted by the output of IC4a.

The start control is connected to pin 3. When this button is pressed, circuits on AE5 cause the reset line at pin 15 to go low, resetting counter IC10, IC11 and IC12. If the output of IC12 were to be high, the negative-going step resulting from the resetting would pass via C10, IC6f, and would clock the D-type bistable IC7a. The Q output of the bistable would go to '1' state, and call centre frequency level, resulting in a lock-out state since there would be no 'T time' reply from the frequency counter on AG1. To avoid this, pin 12 of IC7a is wired to the start button.

The manual and start controls are interconnected so that a new sweep is not initiated during manual scan if the start button is accidentally pressed.

3.20.5 Read-in sequence controller—AE5

Circuit diagram— Fig. 7.23

This board controls the input of data to the store on AE2. It is synchronized to the store recirculation time by the 'end of store' pulse at pin 18. The 'end of store' pulse is shaped and gated to trigger D-type bistable IC21b which removes the resets on the counters whenever a new sweep is to be started.

IC's 1, 2, 3 and 4 form a ÷ 513 counter. IC's 1 and 2 are presettable counters, and IC4 is a monostable which inhibits the count on IC1 for one clock pulse. Outputs of the counter, therefore, occur every 513th clock pulse.

The output of counter IC3 is connected to the variable ratio counters IC's 5, 12 and 13 which are programmed by the sweep speed commands. These commands enter at pins 27 to 30, and operate through latch IC10 to control gates IC's 6, 7, 11 and 14. Counter IC5 is used in two parts, as a ÷ 2 counter and a ÷ 5 counter. IC12 and IC13 are ÷ 10 counters controlled by the sweep speed commands.

Different counters are gated into circuit, and a 1-2-5 sequence division ratio is achieved. The output of the final counter is connected to monostable IC4b. The monostable output is a pulse 40 μs wide which is set to be between 64 and 128 clock pulses wide.

The Q output of IC4b is fed to gate IC8a whose output feeds the preset enable of IC2. The gate is opened when IC1 and IC2 have counted to 64 on the next ÷ 513 cycle, and the counter is preset to zero on the next clock pulse. The output of IC8a is, therefore, a pulse of one clock pulse duration.

As counters IC1 and IC2 are reset to zero, the ÷ 513 counter must start again. Before the next count of 64 is reached, the output of monostable IC4b will have gone back to its zero state, and gate IC8a is closed. The count of 513 then continues, undisturbed.

The 'preset enable' pulses of IC8a occur when new information should be entered into the store. However, to enable dual store modes, these pulses must be inverted by IC9b, gated by IC8b and further inverted by IC9c, before they are fed out at pin 26.

Ungated pulses are taken via pin 13 to AE4 to operate the ramp generator.

Thus the read-in point moves 64 clock pulses through the store each time new information is read in, and the correct store sequence is achieved. Since the ÷ 513 counter will have completed its counts a certain number of times plus a further count of 64 clock pulses.

To stop the read-in sequence when the store is filled, the number of read-in points must be limited to 512; the 513th bit is never read in.

IC's 15, 16 and 17 form a ÷ 512 bit counter, counting the outputs of monostable IC4b. The output of the counter is passed via differentiating circuit C3, R3, R4, R5, and after invertion by IC9f is passed to gate IC8c.

The output of IC8c triggers monostable IC18b, the 'start T' monostable. This monostable sends a pulse to AG2 via pin 19, indicating to the frequency counter that the sweep has been completed, and that it should measure the centre frequency.

The output of monostable IC18b also clocks the D-type bistable IC21b. The output of the bistable resets all counter chains, except IC1, back to zero. IC1 is preset to a count of two, to correct the phase of the 'end of store' pulse during the fly-back of the display.

The input pulses to IC18b are gated by IC8c so that should the output of IC17 be high when the start button is pressed, the resultant negative-going edge on the output of IC17 will not trigger the 'start T' pulse. This is because the gate will already be closed by the reset line to the counters.

To operate in the dual store mode, the outputs of bistable IC15 are connected to the front panel A, B and single store refresh buttons via pins 23 and 24. The selected signal returns to AE5 at pin 25 and is fed to gate IC8b, selecting the ordinate pulses. These are then passed out at pin 26 to AE1 as 'can store now auto' pulses.

When a total of 512 new bits of information have been stored, D-type bistable IC21b is clocked and its output, going high, resets the counters as previously described. This bistable is reset by a selected 'end of store' pulse. IC20a gates the pulses so that no 'end of store' pulses can be used during 'T time' when the counter is counting the centre frequency. These pulses are further gated by IC20c in the single sweep mode so that only one pulse will reset IC21b. The gating signal at IC20c is taken from the output of IC20b.

In the auto mode, input at pin 4 is high ('1' state). This, after inversion through IC19, presents a low signal ('0' state) to one input of IC20b. The resultant '1' state signal at IC20b output allows the pulse waveform at the other input of IC20c through to D-type bistable IC21b.

If the single mode is selected, the input at pin 4 is at '0' and hence the signal at IC20b input is in '1' state. IC20b output, therefore, is at '0' closing gate IC20c to any pulses, and the D-type bistable will not reset. The output of IC20b will not go to '1' unless the output of D-type bistable IC21a goes to '0'. This is triggered low whenever the start button is pressed.

The start button signal is also gated (IC20d) with the 'manual' signal to set bistable IC21b, so that all the counters are reset. This ensures that the sweep restarts at the beginning.

When the start button is released, the reset is removed, and IC21a output is at '0'; this opens gate IC20c allowing the 'end of store' pulses to be fed to the reset input of IC21b. As soon as the output of IC21b goes to '0', the reset input of IC21a is triggered through differentiating network C7, R15, R16, R17. The reset lines to the counters are also removed.

If the manual button be pressed, the reset signal is applied by triggering IC21b via gate IC20d. Pressing the start button no longer triggers IC21a because the start and manual buttons are interconnected so that pin 3 does not go to '0'.

Pin 5 carries the manual signal which, after inversion at IC9d, is differentiated (C6, R12, R13, R14) further inverted (IC9e) and fed to pin 16. This signal is used on AE4 as a 'manual T time' reply, imitating the output of the frequency counter at the end of the centre frequency period.

Pin 32 carries the 'read-in dwell' signal from AE4. This inhibits the variable ratio counter during the 4 ms duration of the pulse. No information is read into the store during the first 4 ms after the end of 'T time', and the scan and sweep are not started for a similar period. This enables the swept oscillators to settle after the flyback of the scan.

By inhibiting the variable ratio divider, the input ÷ 513 counter, IC's 1, 2 and 3, continues to count 513 until the pulse is removed. In this way the 'read-in' signals continue in synchronism with the store as soon as the sweep is allowed to start.

3.20.6 Frequency graticule generator and bright-up processing — AE6

Circuit diagram— Fig. 7.24

This board provides the video drive to line scan and video amplifier AM2.

Half field pulses at pin 16 are used by three monostables :

The first monostable, IC2b, produces a 0.8 ms wide pulse which is used for field blanking. The second monostable, IC2a, provides (pin 29) a 200 μs wide pulse used to produce field drive to the field scan circuit on AM3. This waveform is also used to drive the saw-tooth generator on AE6. The third monostable IC1a has a variable pulse width, and is used to start the first line of the frequency graticule. The start of the frequency graticule can be moved by ±1 ms about the calibrated 2 ms time. Hence, the first frequency graticule line can be moved from zero to 2 calibrated divisions from the start of the scan.

The outputs of monostable IC1a feed the reset line to the frequency graticule counter, the add stripes circuit, and frequency graticule multivibrator IC1b.

Multivibrator IC1b is a monostable with a calibrated period of 1 ms. By varying this period the interval between the frequency graticule lines can be varied. Both the shift and gain potentiometers are front panel controls.

The output of IC1b is inverted at IC3a, and then connected to J-K bistable IC4a where it is synchronized with the beginning of a line by delayed line pulses (pin 20) from AE3. IC4a output is then gated at IC8a.

In order to display only eleven lines of frequency graticule, the frequency graticule is masked after the eleventh count by a signal applied to the second input of gate IC8a. The combined signal is then passed through IC8c where the first, sixth and eleventh lines are masked so that the striped line can be added at IC8d.

The 'frequency graticule mask' signal is obtained by counting the number of striped lines. IC5b and IC6a divide by three so that after the third striped line the 'frequency graticule mask' signal is produced at the output of IC6a. This counter is reset every field by the output of IC1a.

The 'add stripes' signal is produced by IC5a and IC4b. IC5a counts the number of frequency graticule lines and divides by five. The output clocks bistable IC4d producing the 'add stripes' signal. This bistable is reset at line rate by a differentiated 'line blanking' pulse. The 'add stripes' signal is started by a 'delayed line' pulse, and ended by the 'line blanking' pulse. Hence the signal is just under one line long, the gap being during the flyback period of the line scan.

The 'add stripes' signal opens gate IC8b. The second input of the gate is the output of counter IC7a, IC7b, which is two D-type bistables connected to divide by four. This divides the 10 dB 'graticule' signal producing a square wave pulse lasting for two 10 dB graticule counts every fourth graticule line. This signal, when gated with the frequency graticule, produces striped lines.

The 2 and 10 dB graticule signals at pins 9 and 8 are gated with the combined frequency graticule at IC9a, producing the 'total graticule' signal This signal is routed to the bright-up mixers via R33. Two further signals, 'bright line' and 'read-in bright-up', are also fed to the mixers at TR6 emitter. TR6 base is taken to potential divider R41, R42 which is connected to the graticule intensity potentiometer.

The saw-tooth generator circuit, driven by the 'field drive' signal, produces a saw-tooth in synchronism with field drive. The read-in sweep from AE4 enters at pin 14. The signals are fed to input pins 3 and 2, respectively, of comparator IC12. The comparator output is connected via R26, D2, D3 and R27 to inverter IC13a.

The output of IC13a is a rectangular pulse; the start of each pulse is in synchronism with the field frequency. The termination of the pulse depends on the read-in sweep potential. As the read-in sweep progresses, the pulse becomes longer, and as it is in synchronism with field drive it can be used to denote the read-in point on the display.

The pulse is gated at IC9b with the 'scanning' signal entering at pin 23. The 'read-in bright-up' pulse then passes via test point 14 and R13 to the emitter of TR6. Pin 23 is connected to the read-in bright-up switch. If the input signal at the pin is low, the 'read-in bright-up' signal is inhibited by IC9b. The signal at pin 23 is low if 'read-in bright-up' is not selected or, if it is selected, if the 'scanning' signal from AE4 at pin 23 is low.

The ungated 'read-in bright-up' signal passes through differentiation network C11, R28, R29, R30 to inverter IC13d as a negative-going pulse, and is then fed to the K input of bistable IC6b. This bistable is clocked by the 'line blanking' signal which is at line rate.

During scanning IC6b is held in reset mode by the 'bright line' signal (pin 17) from AE4. However, after a single shot, or during the manual mode, this reset is removed and the bistable is triggered at line rate whenever the 'bright-up' signal produces a negative-going edge.

The output of J-K bistable IC6b is of one line duration, and is used to 'bright-up' the line as set by the bright line position control on AE4. The 'bright line' signal passes via test point 13 and R34 to join the 'total graticule and read-in bright-up' signal at the emitter of TR6.

In the manual mode data enters the store coincident with the bright line. To effect this, the 'bright line' signal is gated (IC10d) with the 'can refresh' signal from AE3 (pin 32). IC10d output is connected to monostable IC15, which produces a 'can store now manual' pulse of 0.5 μs duration that is fed to pin 28.

C13 at the input of the monostable removes a small spike caused by the delay through IC6b which would otherwise trigger IC15.

'Line blanking' entering at pin 7 is gated at IC10a with the 'field blanking' pulse. The combined pulse after inversion at IC3d becomes the 'dispiay mask' signal, and is coupled via level shifter R32, R31 to the base of TR4. When this signal is in '0' state, TR4 is turned on, turning off TR5, and causing the video drive to blank out the screen.

The 'end of ordinate' pulses (pins 5 and 6) from AE3 are routed through IC11a and b by the signal at pin 25 to either IC14a or IC14b, which are reset by the negative edge of the 'end of ordinate' pulses.

Pin 25 is connected to the display switch. If high defn is selected, pin 25 is at '1' state. If either display A or B is selected, pin 25 passes a switching signal of 'complete field' from AE3. This waveform switches, at half field rate, the input to IC14a and IC14b from input pins 6 and 5. Thus the input signal to IC14a is that of store A, and the signal to IC14b is that of store B when in dual store mode.

In the single display mode only the output of IC14a is used, i.e. only the set control of IC14a is set by the differentiated 'line blanking' pulse. In the dual store mode, both IC14a and IC14b are set by this pulse depending on the setting of display switches A and B, whose outputs are routed via IC10b and IC10c. The output pulses of IC14a and b are passed to the emitters of TR7 and TR8, whose bases are controlled by the A and B intensity potentiometers on the front panel.

The voltage on the potentiometers is switched by the A, B single display store buttons, so that when both potentiometers are used in the dual store mode, the maximum combined brightness is the same as when only one control is used.

The collectors of TR6, 7 and 8 are connected to the current summing emitter of TR5. The collector of TR5 is connected to pin 30 via R39, which is included so that a voltage waveform can be produced at TP17.

It is essential that the read-in point on manual is the same as on auto mode in order to avoid inaccuracies in tracking. The saw-tooth generator (TR2, TR3) must, therefore, be very stable in amplitude and level. Zener diode D1 is chosen to have a temperature coefficient similar to that of the base emitter junction of current source TR3.

The amplitude and voltage level of the saw-tooth are adjusted by potentiometers R20 and R22, which affect the gain and shift of the saw-tooth generator.

3.21 SYSTEM CONTROL LOGIC (1)—AF1 SYSTEM CONTROL LOGIC (2)—AF2

Circuit diagrams—Fig. 7.25 and Fig. 7.26

A main feature of the response analyser is push-button control. Four groups of push-buttons, i.e. vertical scale, horizontal scale, horizontal range and filter bandwidth, are combined by logic circuits and output buffers on these boards to provide signals which select the following :

(1) Degree of attenuation of the input attenuator.

(2) Required filter.

(3) Amount of gain required by 100 kHz i.f. amplifier in accordance with the filter selection in (2) above.

(4) Fastest permissible sweep speed.

(5) Appropriate counter time base.

Board—AF1

The horizontal scale, range and filter bandwidth control buttons provide inputs to this board. The board consists mainly of AND gates, and produces the following three groups of outputs:

(a) 4 lines, at pins 6, 4, 14, 13, carrying information to determine the sweep speed of the display.

(b) 2 lines, at pins 17 and 18, carrying information to determine the counter gate time.

(c) 5 buffered outputs, at pins AL, 28, 30, 32, 29, which are routed to AF2.

(d) 1 line, at pin 16, normally high, which is set low to move the decimal point when Frequency Extender TK 2373 is used.

Board—AF2

This board controls the sweep speed, programmable attenuator drive, and select filter drive circuits.

Input from AF1, at pins AF, AL, 32, AJ, AH, is further buffered by TR7 to TR11, and gated by D31 to D36 and D40, to give 5 pairs of lines to select each of 5 filters. Also derived is a slow/fast control line taken via pin 29 to AD2, and a group of 3 lines, at pins AL, AF, 27, which are routed to the vertical scale buttons on the front panel.

The vertical scale buttons have 12 output lines which are taken to diode gates, D6 to D30, on AF2. Outputs of the gates drive four buffer output stages, TR2 to TR6, to operate the 10, 20, 30 and 60 dB solenoids of the programmable attenuator.

Four lines, at output pins 16, T, H, A, control the sweep speed. Truth Table 3.2 shows the logic states required on each line to command each sweep time. The lines are designated code A, code B, code C and code D.

Truth Table 3.2

Logic states of sweep speed control lines

Sweep time	Code A	Code B	Code C	Code D
100 s	1	1	1	1
50 s	1	1	1	0
20 s	1	1	0	1
10 s	1	0	1	1
5 s	1	0	1	0
2 s	1	0	0	1
1 s	0	1	1	1
0.5 s	0	1	1	0
0.2 s	0	1	0	1
0.1 s	0	1	0	0

It is required that by pressing the x5 sweep speed button, the sweep time is decreased by two steps, in Truth Table 3.2 On releasing the button, the sweep speed must return to its former state. This is achieved as follows :

Note Although the button is labelled x5, in some instances the increase in sweep speed is x4.

When the x5 button is not pressed, all inputs to IC5c are in '1' state. IC5c output is in '0' state, and IC4f output is in '1' state. This holds divider IC6 reset, and the following gates open : IC1a, b, c, d and IC2a, b, c, d.

The required sweep speed code (from the front panel controls), at pins R, P, D, F, is stored at J-K bistables IC7a, b, and IC8a, b, via the open gates of IC1 and IC2. The output of the bistables passes via pins 16, T, H, A to AG4 to determine the sweep speed.

IC5, IC7 and IC8 form a counter which, when not locked into a particular state by signals arriving through open gates IC1, IC2, counts down Truth Table 3.2 on receipt of clock pulses at IC7 pin 1.

If the x5 button is pressed, IC1 and IC2 gates are closed so that the code entering at pins R, P, D, F no longer affects the stored information. Also IC6 reset is removed, and either IC3c or IC3d is opened.

As IC6 is normally held reset, the $\div 4$ and $\div 8$ outputs at IC6 pins 8 and 11, respectively, are at '0' state. Therefore, outputs of gates IC3c, IC3d are in '1' state, and gate IC3b is open to pulses arriving at input pin 1. However, the integrated circuits to which these pulses are routed are inhibited.

When its reset is removed IC6 begins counting the pulses at input pin 1. After 2 pulses, the output at IC6, pin 8, goes to '1' and if the x5 button is pressed the output of IC3d goes to '0', closing IC3b to further pulses.

Thus operating the x5 button allows IC3b to pass 2 pulses to clock the counter.

Pressing the x5 button, therefore, allows the initial sweep time code to progress two steps down Truth Table 3.2, and thereby increase the sweep speed by 5.

After the 2 or 4 steps are completed, no further change occurs until releasing the x5 button restores the initial sweep speed code.

If the initial sweep time is near the bottom of Truth Table 3.2, and pressing a sweep speed button attempts to drive the counter beyond 0100, the condition is detected by negative logic gate D38, D39, R38. Gate IC3b is then closed, via D37, to further pulses making it impossible to decrease the sweep time beyond 0.1 s.

3.22 OVERALL DESCRIPTION OF THE FREQUENCY COUNTER—AG1 to AG5

Block diagram—Fig. 3.16

The input signal is amplified, shaped and pre-scaled in frequency by a factor of two. The signal is then gated into a chain of reversible decade counters.

At the end of each count, the information present in the decade counters is transferred to a main latch, and then to the display to provide a visual readout of the count.

At the end of the first count, after a 'start-T' pulse, the information present in the decade counters is also transferred to a centre frequency latch. This frequency is the centre frequency of the preceding sweep.

The stored centre frequency may be recalled and displayed at any time by operating the past centre frequency switch.

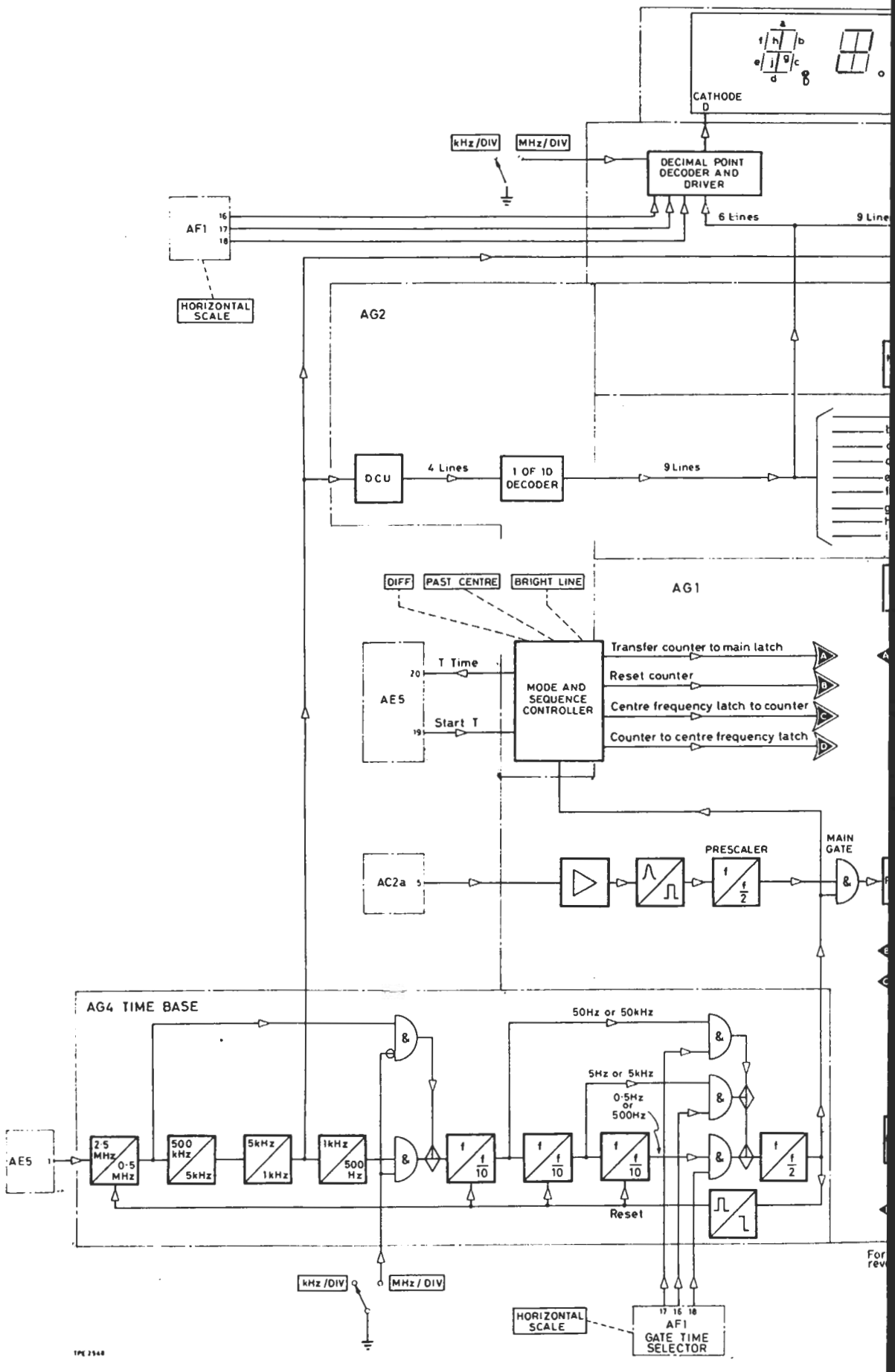


Fig. 3.16 Block diagram – Frequency counter

In the difference frequency mode, a chain of decade dividers is loaded with the stored centre frequency instead of being reset to zero, and the count is changed from forward to reverse. A count of the input frequency is then obtained by opening the gate for the required period. A count down from past centre frequency to zero is then initiated. If the count reaches zero, the direction of count of the decade chain is changed from reverse to forward. The final count in the decade chain is then the modulus of the difference between the past centre frequency and the input frequency, and is displayed in the normal way.

In the mode bright line frequency, the input signal is continuously measured and displayed.

3.22.1 Counter time base AG4

Circuit diagram Fig. 7.27

Intergrated circuits IC1 to IC7 form a cascaded chain of decade counters which make up the dividing chain for the time base.

Selection gates associated with IC10a and b and IC11a, b and c, increase the period of a reference 2.5 MHz signal entering at pin 1 from 10^2 to 10^7, to form the various time base gating intervals.

The variable gating interval is present at pin 7. The negative-going edge of the output of IC1b is used to re-set the time base divider chain via C1 and IC10d. This reduces the waiting period to 5 cycles at 2.5 MHz (i.e. 2 μs) if the MHz/div. switch is operated, and 1000 times this (i.e. 2 ms) if the kHz/div. switch is pressed.

The gating period is chosen to give sufficient resolution of the counter display for an 0.5% accuracy of the total dispersion of the display. If the wide '3' filter bandwidth is selected and the kHz/div switch is pressed, the gating period is selected to be 20 ms irrespective of dispersion.

The counter gating period against dispersion is shown in Table 3.3.

The gating times are effected by gates associated with IC8, IC9 and IC16. If neither the kHz/div or the wide '3' filter bandwidth switch is operated, the output of IC8b is at '1' state. Therefore, the gating interval is selected via IC8, IC9, IC16 and IC11, according to which of the horizontal scale triple group lines is at '1'. Two of these lines enter at pins 5 and 6.

Table 3.3

Counter gating period against dispersion

Dispersion	Counter Gating Period Filters 1 and 2	Filter 3
0.02 0.05 kHz/div. 0.1	2 s	20 ms
0.2 0.5 kHz/div. 1	200 ms	20 ms
2 5 kHz/div. 10	20 ms	20 ms
0.02 0.05 MHz/div. 0.1	2 ms	2 ms
0.2 0.5 MHz/div. 1	200 μs	200 μs
2 5 MHz/div. 10	20 μs	20 μs

If, however, the kHz/div and the wide '3' filter bandwidth switches are pressed, the output of IC8b ensures that no matter which of the three horizontal scale triple group lines are at '1', IC11a only will be enabled, thus producing a 20 ms gating interval. The three gating interval select lines to IC11 are fed out at pins 14, 15 and 16.

Since the decrease by a factor of 10 of the gating interval means a shift to the left by 1 digit of the decimal point, the position of the decimal point in the display is determined from the gating interval. The three gating interval select lines, therefore, operate on the multiplexing logic of AG5 to determine the position of the decimal point in the counter display. Pin 9 is fed a 'start-T' pulse from AG2 which resets the divider chain via IC10. This ensures the correct measurement of past centre frequency which would not be the case if the measurement began after the start of a gating interval. Pin 4 inputs the decimal point position when Frequency Extender TK 2373 is in use.

The $\div$ 5 output of IC4 is fed to pin 3. This output after processing by IC3 and IC4 of AG2 provides a suitable 1 kHz reference frequency for the multiplexing of the digits of the counter display.

X-Y recorder circuit

The X axis signal is the read-in sweep waveform taken from the output amplifier of the digital scan generator AE4. This signal is passed to the output socket SKR, pin 10 via short circuit protection resistor R14 on board AG4. The Y signal is taken from AE1 TP5 via pin 24, this being the output of the peak detectors and is directly before the signal is digitized. As with the X signal, a short circuit protection resistor R75 on board AG4 is included.

The pen-lift signal, which is generated from the scan signal generator on board AE4, is a +ve going 5 V pulse during the read-in sweep. This signal is passed via pin 23 AE4 to pin 32 AG4 and through a 2-transistor non-inverting buffer TR2, TR3 and used to drive a dry reed relay RLA, the relay having normally open contacts. One side of the relay coil is taken to the rear socket, and it is necessary to earth this point to operate the relay.

A latching push button provides a 100 s sweep. The sweep rate is controlled by a 4-bit word,which determines the input signal rate to the digital scan generator. This 4-bit word is established by the sweep width and filter buttons operated. The four controlling signal wires are taken from pins 16, T, H, A AF2 to AG4A pins 21, 19, 27, 26 where they are presented to four AND-OR-NOT gates which enable the signal either to pass normally or whenever the 100 s sweep button is pressed, in order to establish the correct code for a 100 s sweep. The sweep code is then passed from AC4 to AE5 where it is used to set a variable ratio divider which produces the clock signal for the digital scan generator. This enables the instrument to sweep at a rate compatible with an X-Y recorder with no loss of resolution.

3.22.2 Counter display AG5

Circuit diagram — Fig. 7.28

The 9 digit display panel of the counter is driven in a multiplexing mode. Transistor pairs TR1 to TR18 form the drivers to the 9 anodes. The inputs to the driver-pairs, at pins 1, 3, 5, 7, 9, 11, 13, 15 and 17, are derived from the outputs of IC4 on AG2, which is a one of ten decoder, used to strike the 9 anodes in a cycling, or multiplexing, mode. The frequency of striking an anode is 1 kHz, i.e. the period between striking a particular anode and the next time that it is struck is 1 cycle of 100 Hz (10 ms).

Transistors TR19 to TR27 form the drivers to the cathode segments of the display. The inputs to the drivers are derived from IC1. This integrated circuit is a 7 segment decoder which translates the four bit b.c.d. information per decimal digit, entering at pins 36, 37, 38 and 39, into 7 lines of information for driving a 7 segment display.

In a standard 7 segment display the digit 1 is off centre, and the digits 6 and 9 have no top or bottom bars, respectively. To overcome this, the information present at the outputs of IC1 is processed before driving the display panel.

If the four bit b.c.d. information represents any decimal digit other than 4, the output of IC2c is at '1' state. If also, the decimal digit to be displayed contains the cathode segment g (pin 14, IC1), the output of IC4a will be at '0'. This overrides the inputs to IC4b and IC4d, which in turn causes TR19 and TR20 to drive segments a and d into illumination. This ensures that the digits 6 and 9 have a top or bottom bar. If the four bit binary information represents the decimal digit 1, the output of IC3b will be at '1'. This will turn off TR24 and TR25 but turn on TR26, and thus ensure a central digit 1. With alternative Display Panel BRO 9450 a central digit 1 is not available and, therefore, TP2 is earthed.

The four bit b.c.d. information from the main count chain memory is selected, one decimal digit at a time by the outputs of IC4 on AG2, decoded, and then displayed by striking the relevant anode in synchronism with the selection of the four bit binary information.

TR27 is the driver for the decimal point. The combination of '1' states on pins 31, 32, 33 and 34, which represent the length of the gating interval, determine which of the gates of IC5 and IC6 are to be enabled. Each gate is enabled when its third input, at pins 13, 15, 11, 5, 9 or 7, is at '1'. These lines select after which digit the decimal point will be displayed. When one of the gates of IC5 or IC6 is enabled, their wired outputs go to '0'. This turns on driver TR27 and illuminates the decimal point in the relevant position.

Pin 35 also receives the 1 kHz reference signal, from AG4, that is used to drive the display anodes. The signal has a mark-space ratio of 1 to 4. The positive part of the waveform is used to blank (turn off) all the drives to the segments of the display either directly, as in the case of

TR26 and TR27, or indirectly by applying a blanking pulse to pin 4 of IC1, which causes all the outputs of IC1 to go to '0'. The blanking pulse, being the same 1 kHz reference frequency that is used to drive the multiplexed anodes, occurs at the moment that one anode is extinguished and the adjacent anode is struck. Because of the mark-space ratio of 1 to 4, the blanking is applied for the first 1/5th of the duration of an anode being struck.

Blanking is necessary to eliminate the effect of after glow on the digit.

Truth Table 3.4

Logic states of first reversible decade counter

Forward mode

Q outputs				
IC2a (Pin 5)	IC2b (Pin 9)	IC3a (Pin 5)	IC3b (Pin 9)	Decimal
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9

Reverse mode

Q outputs				$\overline{Q}$ outputs				
IC2a (Pin 5)	IC2b (Pin 9)	IC3a (Pin 5)	IC3b (Pin 9)	IC2a (Pin 6)	IC2b (Pin 7)	IC3a (Pin 6)	IC3b (Pin 7)	Decimal
1	1	1	1	0	0	0	0	0
0	1	1	0	1	0	0	1	9
1	1	1	0	0	0	0	1	8
0	0	0	1	1	1	1	0	7
1	0	0	1	0	1	1	0	6
0	1	0	1	1	0	1	0	5
1	1	0	1	0	0	1	0	4
0	0	1	1	1	1	0	0	3
1	0	1	1	0	1	0	0	2
0	1	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0	0

3.22.3 Counter front end – AG1

Circuit diagram— Fig. 7.29

The 'restored frequency' signal enters at pin 1, and is fed to Schmitt trigger TR3, TR4. The Schmitt output is buffered by emitter follower TR5. The now square wave signal is pre-scaled in frequency by a factor of 2 by IC1 to ensure reliable division by the first reversible decade counter.

After pre-scaling, the signal is fed to level translater TR7 which produces nominally 4.5 V spikes coincident with the rising edge of the input waveform. These spikes drive the input of the first reversible decade counter. This consists of four J-K bistables, IC2 and IC3, with gating provided by IC9b and c, IC10a and b, and IC11b.

Outputs 5 and 6 of J-K bistable IC4b provide the inputs to gates IC10a and IC10b. These lines decide the direction of count, forward or reverse, of the first reversible decade counter. If the Q output of IC4b (pin 5) is at '0' and the $\overline{Q}$ output of IC4b (pin 6) is at '1', the counter will count in a forward mode. If the two outputs are in the reverse logic mode, the counter counts in the reverse direction.

Truth Table, 3.4 gives logic states for counting in both forward and reverse directions of the first reversible decade counter.

Table 3.4 shows that the Q outputs of IC's 2 and 3 present the four bit b.c.d. information for the first decade when counting in a forward mode. Also, the $\overline{Q}$ outputs of IC's 2 and 3 present the four digit binary information of the first decade when counting in the reverse mode.

To read out the information present in the first decade, either the Q or the $\overline{Q}$ outputs must be accessed depending on whether the last counting operation was done in a forward or reverse mode.

The outputs are accessed by gates IC12 and IC13. The gates IC12c, IC12d, IC13c, IC13d access the $\overline{Q}$ information which after inversion through the gates becomes the Q information. To enable the gates, the $\overline{Q}$ output of IC4b (pin 6) must be at '1', which is the same condition as for a forward counting mode. To access the Q information in a reverse counting mode, gates IC12a, IC12b, IC13a and IC13b are used. The gates access the Q information which after inversion through the gate becomes the $\overline{Q}$ information. To enable the gates, the Q output of IC4b (pin 5) must be at '1', which is the same condition as in the reverse counting mode.

The accessed Q or $\overline{Q}$ outputs of the first decade are fed to IC6, the main latch, or memory, of the first decade. The outputs of IC6, which are taken to pins 16, 19, 17 and 15, are the inverse of the inputs, and are fed to multiplexing gate IC20 on AG3. The four bit b.c.d. information is re-inverted after passing through IC20 on AG3 and restored to the same polarity as before entering IC6 on AG1.

IC14d is a gate producing a main latch memory transfer pulse for IC6 and all the other main latches.

IC7 is the centre frequency latch. At the end of a centre frequency measurement, IC4a is triggered by the end of the main gate pulse which enters at pin 9. This causes the outputs of IC4a, at pin 9 and pin 7, to change state; this will only occur once due to the polarity of the J and K inputs of IC4. The change of state of the output triggers IC5b producing a centre frequency memory transfer pulse which enters IC7 at pins 4 and 13. This results in the past centre frequency measurement just obtained being stored in the centre frequency latch. The information thus stored in IC7 may be used to pre-set the decade counter via IC's 15, 16 and 17.

At the beginning of a difference frequency measurement, IC4b is pre-set so that its Q output is at '1' and its $\overline{Q}$ output is at '0'. This will enable gate IC14b, and when a 'transfer centre frequency latch to counter' pulse arrives via pin 27, the $\overline{Q}$ outputs of the first decade are pre-set to the centre frequency information via gates IC's 15, 16, 17, and the counter is ready for a count in the reverse mode.

If the past centre frequency switch is pressed, IC4b is reset so that its Q output is in '0' state and its $\overline{Q}$ output in '1' state. This will enable IC14c, and when a 'transfer centre frequency latch to counter' pulse arrives, the Q outputs of the counter are pre-set to the information contained in the centre frequency latch. The counter is in the forward mode, and therefore any information accessed will be from the Q outputs.

At the end of a count, without a 'transfer centre frequency latch to counter' pulse, the wired outputs of IC16 and 17 are at '1' and a positive 'reset' pulse entering at pin 13 resets the Q outputs of the decade to '0' via IC15. The 'reset' pulse is derived from IC1b, IC13b, IC12b and IC14a on AG2.

IC11a and IC9a form part of a chain of gates which detect a full register of zeros when counting in the reverse mode.

When counting in the reverse mode, as the count reaches zero, i.e. all the b.c.d. outputs of all the decades are momentarily at '0', the output of IC11a also goes to '0'. This changes the state of IC4b which reverses the direction of count to the forward mode. This process is used in the difference mode when the counter is pre-set with the centre frequency information, and a count is initiated down to zero at which point the counter must be reversed to count in the forward mode. At the instant of reaching zero in the reverse mode, before counting in the forward mode is possible, the Q outputs of the first decade must be changed from '1' to '0'; this is the correct condition for zero in the forward mode, and the first decade must be reset. This is effected by the 'detect zero' pulse from IC11a and IC8.

Monostable IC5a is triggered by the falling edge at the end of a gating period; the gating waveform enters at pin 9. The output of the monostable, after passing through gate IC14a, is used as a 'transfer centre frequency latch to counter' pulse via the route switch S10 on A01, and gate IC13c on AG2.

At the end of a centre frequency count, IC5b is triggered by J-K bistable IC4a, and the output of IC5b inhibits gate IC14a, which in turn inhibits the first 0.4 μs of the 0.8 μs pulse produced simultaneously by IC5a. This inhibition is necessary to prevent a 'transfer counter to centre frequency latch' pulse, and a 'transfer centre frequency latch to counter' pulse being applied to the decades simultaneously, which may result in a loss of information.

3.22.4 Counter control and dividers AG2

Circuit diagram— Fig. 7.30

The output of the first decade enters at pin AF, where it is shaped by monostable IC18a, IC18b which has a nominal pulse period of 40 ns. The monostable is triggered by the negative edge of the input waveform.

Consider the counter working in the difference mode :

The counter is pre-loaded with the past centre frequency, and a count-down is initiated until it reaches zero; at this point the direction of count is reversed to a forward mode and a count-up is initiated. As the direction of the count is reversed, the Q output of IC3b on AG1 (see Truth Table 3.4) changes from '1' to '0' at the time of re-setting. This, however, is interpreted by the next decade as a carry pulse which

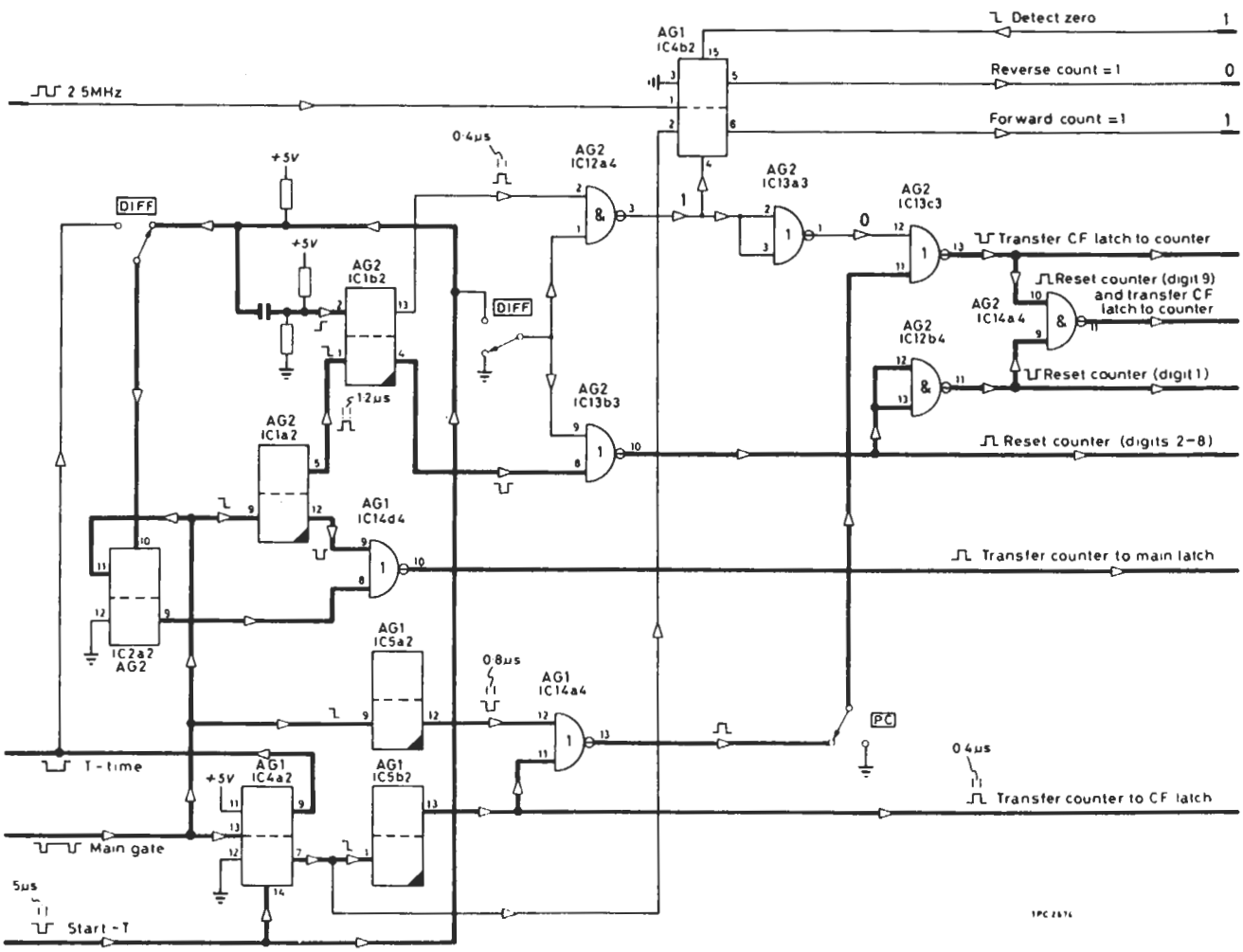


Fig. 3.17 Flow diagram past centre mode

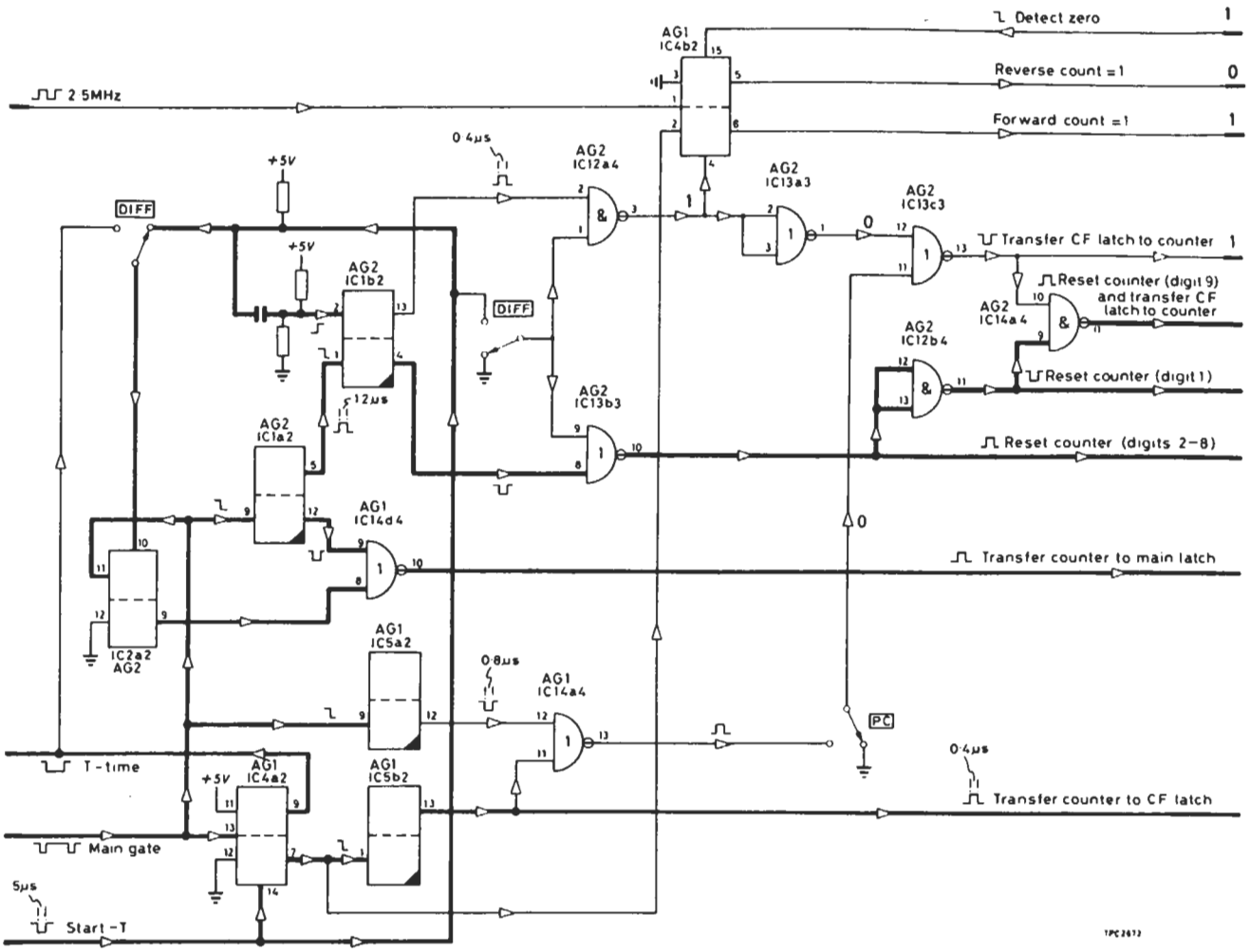


Fig. 3.18 Flow diagram—bright line mode

would lead to an error. To overcome this, a blanking circuit consisting of R1, R5, R3, C2, C4 and D1, operates via gate IC18b, to blank the carry pulse through the monostable when the logic level at pin AH changes from '1' to '0'. This pin is fed from the output of IC4b on AG1, which is the logic line to denote a reverse count. Thus the blanking is performed at the time of changeover from a reverse count to a forward count. D1 presents a small time constant to the positive-going transition at pin AH.

After the monostable pulse has been inverted by IC18c, it passes through gate IC12d or IC12c to the forward and reverse counting inputs of IC1 on AG3. Steering the monostable pulse onto the correct input of IC1 on AG3, forward or reverse count, is achieved via pins AD and AII. These pins are the $\overline{Q}$ and Q outputs, respectively, of IC4b on AG1, and determine the direction of count.

The end of a gating interval input at pin K triggers monostable IC1a. The negative-going output at pin AA, after passing through gate IC4d on AG1, is used as a 'transfer counter into main latch' pulse. The positive-going output of IC1a triggers IC1b. The positive-going output of IC1b, after gating through IC12a, IC13a and IC13c, is used as a 'transfer centre frequency latch to counter' pulse. The negative-going output of IC1b, after gating via IC13b, becomes a 'reset main count chain' pulse.

IC12b inverts the positive-going 're-set' pulse to a negative-going 're-set' pulse which is then gated via IC14a to re-set the first decade.

IC2a inhibits a 'transfer counter into main latch' pulse after a centre frequency measurement in the difference mode. This is to ensure that in the difference mode, the first reading to be displayed is not the past centre frequency but a true difference.

When the difference frequency switch is pressed, the pre-set input of IC2a, which enters at pin A, is connected to the Q output of IC4a on AG1. Up to the end of the past centre frequency measurement, this output is at '0', which holds the Q output of IC2a at '1'. This in turn inhibits gate IC14d on AG1, and thus prevents a 'transfer counter into main latch' pulse being initiated at the end of a centre frequency measurement.

After a past centre frequency measurement, the Q output of IC4a on AG1 goes to '1', which allows IC2a to be triggered at the end of the next gating interval. The Q output of IC2a then goes to '0', which does not inhibit gate IC14d on AG1, and will thus allow a 'transfer counter into main latch' pulse to be initiated at the end of this gating interval. Therefore, the first 'transfer counter into main latch' pulse is initiated at the end of the first true difference measurement.

In the past centre or bright line frequency modes, the pre-set input of IC2a is fed from a 'start-T' pulse. This is at '1' at the end of a past centre frequency measurement, and IC2a is triggered by the end of the first gating period which enters at pin K, causing the Q output of IC2a to go to '0'. This does not inhibit the gate IC14d on AG1, and thus a 'transfer counter into main latch' pulse is initiated at the end of a past centre frequency measurement.

Flow diagrams, Figs. 3.17, 3.18 and 3.19, of 're-set' and 'transfer' pulses for past centre, bright line and difference modes, respectively, illustrate how the outputs of the four monostables, IC1 of AG2, and IC5 of AG1, are gated and routed in the operating modes of the counter. The bright line switch is mechanically ganged to the past centre and difference switches, and when pressed automatically releases these two switches.

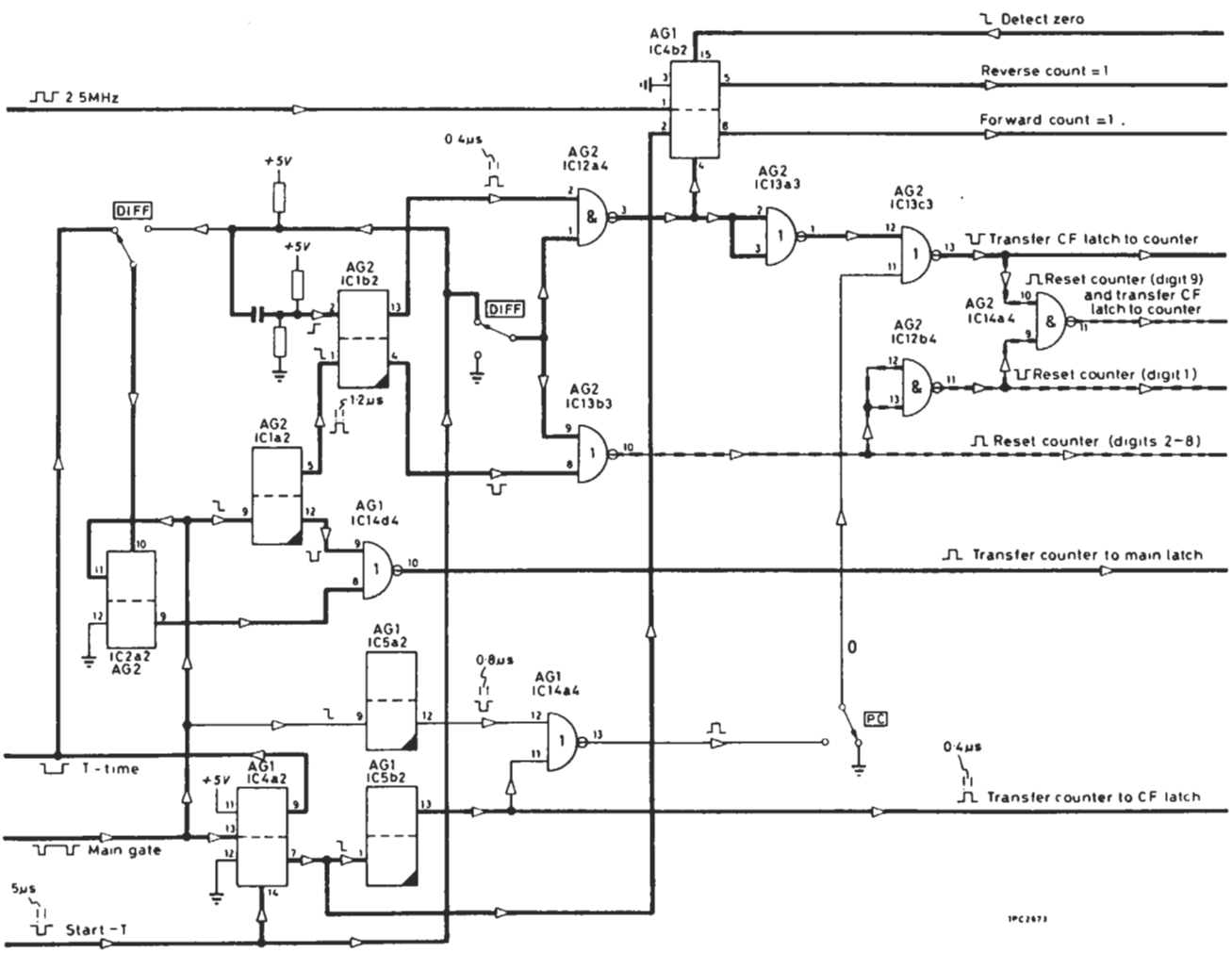


Fig. 3.19 Flow diagram difference mode

IC5 and IC8 are pre-settable reversible decade counters, and IC2b is a D-type bistable. These integrated circuits produce the three most significant digits of the display.

IC7, IC10 and IC11a form the main latch for the three digits, and IC's 6, 9 and 11b form the centre frequency latch. The operation of the latches is the same as for the least significant digit decade (see Sect. 3.22.3).

IC15 forms part of the detect zero circuit for detecting a complete register of zeros in the counter chain when counting down in the difference mode (see Sect. 3.22.3).

The outputs of the main latches are gated to AG3 via IC's 19, 20 and 21.

A 1 kHz 'reference frequency' signal enters via pin 1. The signal is divided by ten by IC3, and the four bit b.c.d. information is decoded by IC4 into 9 lines. IC's 16 and 17 invert the outputs of IC4. As the '1' state cycles through the 9 outputs in turn, IC's 19, 20 and 21 are enabled, one at a time, to allow the four bit b.c.d. information per decade digit to pass to the common information lines in a multiplexed manner.

The common information lines are fed via pins 14, 15, 20 and 18 to AG5, where the four bit b.c.d. information is decoded and displayed by the relevant digit of the display.

3.22.5 Main divider chain AG3

Circuit diagram— Fig. 7.31

IC's 1, 4, 7, 10 and 13 are pre-settable reversible decade counters, cascaded to form part of the main count chain. Pins 5 and 12 of each integrated circuit form the input and output drives, respectively, when counting in the forward mode. Pins 4 and 13 form the input and output drives when counting in the reverse mode.

IC's 3, 6, 9, 12 and 15 are the main latches for each of the decades in the count chain. IC's 2, 5, 8, 11 and 14 are the centre frequency latches for each of the decades in the count chain.

The operation of the main latches and the centre frequency latches for these decades is the same as described in Sect. 3.22.3.

IC's 16, 17, 18 and 19 form part of the detect zero circuit for detecting a full register of zeros in the count chain when counting in a reverse direction in the difference mode. The function of the detect zero circuit is described in Sect. 3.22.3.

The four bit b.c.d. information outputs of the main latches are fed to gates IC20 to IC25; the outputs of the gates are wired together to form the common information lines at pins 14, 23, 20 and V.

The inverted outputs of the 1 of 10 decoder IC4 on AG2, enter at pins K, 24, 28, H, F and 13. The lines enable, one at a time, IC20, IC21, IC22, IC23, IC24 and IC25 (see Sect. 3.22.4), allowing the four bit b.c.d. information for each decade of the count chain to pass to the common information lines. The common information lines are fed to AG5 where they are decoded and displayed in the relevant position of the counter display.

3.23 POWER SUPPLY—AK0

Circuit diagram— Fig. 7.32

This provides unregulated lines of +190 V and +80 V, and regulated lines of +30 V, +15 V, -15 V, +6 V, -6 V and +5 V. Also 6.3 V a.c., or alternatively 11.5 V a.c., is supplied to the c.r.t.

The e.h.t is generated in a sub-assembly mounted on the power supply chassis, and is described under EHT unit.

3.23.1 Diode bridges AK1

Circuit diagram— Fig. 7.32

The supply is fed via supply fuses FS1 and FS4, SKTA, and the mains voltage selection panel to transformer T1, which is mounted on power supply chassis AK0. Secondary windings of T1 are connected to bridge rectifiers formed by diodes D1 to D20.

Fuse FS1 in the +190 V line protects diode bridge D1 to D4. Reservoir capacitor C1 (AK0) provides smoothing, and R1 (AK0) discharges C1 if FS1 is blown.

The +80 V unregulated line is produced similarly to the +190 V unregulated line.

The outputs of bridge rectifiers D9 to D12, D13 to D16, and D17 to D20 are taken to regulator board AK3 to produce the +30 V, +15 V and -15 V regulated supplies.

Reservoir capacitors C2, C3, C4 are mounted on chassis AK0.

R1 and D21 together with thyristor CSR1 (AK0) provide over-voltage protection for the +5 V (1) line. Similarly, R2, D22 and CSR2 (AK0) provide over-voltage protection for the +5 V (2) line.

3.23.2 Diode bridges AK2

Circuit diagram Fig. 7.32

T1 secondary windings LT4, LT3 are connected to rectifier bridges D1 to D4 and D5 to D8, whose outputs are taken to AK3 to provide the +6 V and -6 V regulated lines.

Centre tapped windings LT2 and LT1 are taken to full-wave rectifiers D9, D10 and D11, D12. Outputs of these rectifiers are routed to AK3 via FS2 (AK0), FS3 (AK0) to provide the regulated +5 V (2) and +5 V (1) lines.

LT7 provides the c.r.t. heater current (6.5 V a.c.); an alternative 11.5 V a.c. supply is available for use with other manufacturers tubes.

3.23.3 Regulator AK3

Circuit diagram— Fig. 7.33

-15 V line :

Input at pins 38, 39 is passed to series regulator transistor TR3, mounted on the rear heat sink section of the power supply chassis AK0, which is controlled by regulator IC7. Line output voltage is adjusted by R39.

R37, in series with TR3 (AK0) emitter, provides sensing for the current limiting facility of IC7. R36 ensures equal source resistance at IC7, pin 3, with that at IC7 pin 2. C18 provides external frequency compensation to IC7 to prevent instability.

C19 is an output de-coupling capacitor.

The other regulators are similar to the -15 V line regulator, and are referenced to the -15 V line. Voltage outputs are fed back to pin 3 of the integrated circuit regulators via potential dividers.

Additional protection for regulators IC4 and IC5, against switch transients and line shorts, are provided by diodes D2, D3 and D4, D5.

3.24 EHT UNIT—AL1

Circuit diagram—Fig. 7.32

A 19 kHz square wave drive is fed from AM2 (via SKTA) to the base of TR2 on e.h.t. unit chassis AL0, and switches the transistor on and off. TR2 has an inductive load formed by transformer T1 (AL0), which resonates with C6.

When TR2 is switched off, a pulse of approximately 90 V peak-to-peak is present at its collector. This is stepped up to a peak voltage of 4 kV by T1, and fed to voltage multiplier VM1 (AL0). The multiplier is a tripler stage which feeds +14 kV d.c. to the c.r.t. final anode.

R4 senses the current drawn by the c.r.t., and the voltage developed across this resistor is used to control the voltage applied to T1. This control is effected via TR1 (AL0) which with IC1 forms a power supply regulator. R4 is adjusted to minimize the change in e.h.t. for changes in c.r.t. beam current. R7 sets the e.h.t. voltage with no current drawn by the c.r.t.

Zener diode D1 protects the input of IC1.

3.25 LINE SCAN AND VIDEO AMPLIFIER—AM2

Circuit diagram—Fig. 7.34

19 kHz square wave 'line drive' signals (pin 32) from AE3 switch transistor TR2 on and off via TR1. This produces a rectangular waveform of approximately 60 V peak-to-peak at the collector of TR2, which is fed to transformer T1. The transformer has two secondary windings; one winding feeds driver TR2 on board AL1, and the other feeds a current drive to the base of transistor TR3.

When switched on, TR3 has an inductive load consisting of transformer T2 and line drive coils L3, L4, which is switched across the +30 V d.c. supply. Current through L3, L4 rises in a sawtooth waveform, and provides the scanning current.

When TR2 is switched off, L3, L4, T2 and C2 form a resonant tuned circuit clamped by diode D3. The output of the tuned circuit provides the first part of the scan via D3.

The pulse output of TR3 collector is rectified via D4 to provide 350 V d.c. to the c.r.t. (V1) anode A1.

The 'switching off' delay of TR3 is set to 2 μs by R9 which varies the excess base current. R10 alters the voltage applied to T2 to adjust the scan height.

'Video drive' current signals (pin 1) from AE6 develop a voltage across R14, R15 which, depending upon the setting of set peak white level potentiometer R15, varies the voltage to TR4 base.

Video amplifier TR4, TR5 gives an approximate output of 60 to 110 V to the cathode of the c.r.t. Amplifier h.f. compensation is provided by C6 and L1.

Diode D6 suppresses the display centre spot at at switch off.

3.26 FIELD SCAN AND CRT BIAS—AM3

Circuit diagram— Fig. 7.34

'Field drive' signals (pin 6) from AE6 are fed to TR2, which with TR1 forms an integrator circuit. The integrator produces a linear saw-tooth of approximately 13 V peak-to-peak at the collector of TR2.

Diodes D2 to D5 form a shaper network which distorts the saw-tooth waveform into an 'S' shaped saw-tooth.

Source follower TR3 is a buffer stage.

R17 varies the amplitude of the signal which is fed to feedback amplifier TR4 to TR7. R28 samples the scanning current which is compared by TR4, TR5 with the signal at TR4 base. The action of the loop is to make the scanning current identical in shape to the input saw-tooth.

The output is coupled via frame output transformer T1 to the frame coils.

TR8 is a d.c. amplifier which varies the c.r.t. grid voltage via set black level potentiometer R30.

3.27 CRT CIRCUIT--AM1

Circuit diagram—Fig. 7.34

The frame coils are damped by R1, R2 to prevent oscillations caused by shock excitation from the line coils.

A linearity sleeve is positioned in the deflector coil system to effect line linearity at the start of the scan.

Spark gaps are introduced into the c.r.t. grid, cathode and anode leads to protect devices connected to the electrodes. The gaps limit the voltages which can occur during flash over inside the tube.

Current flow is limited by series resistors R12 on AM2, R32 on AM3, and R3 on AM1.

Chapter 4

Maintenance

4.1 INTRODUCTION

This chapter contains information for checking the instrument's performance. Many of the methods used are simplified and of restricted range compared with those which would be needed to demonstrate complete compliance with the specification. They should be regarded only as providing a check procedure, for use during routine maintenance, to determine whether repair is needed.

Performance limits quoted are for guidance only and should not be taken as guaranteed performance specifications unless they are also quoted in Sect. 1.2, Data Summary.

4.2 PERFORMANCE CHECKS

4.2.1 Test equipment required

This section provides a list of test equipment required to carry out the performance checks detailed in this chapter.

Item	Description
a	Frequency counter, e.g. mi TF 2424A.
b	Signal generator, e.g. mi TF 2002B.
c	Sensitive voltmeter (standardized at -10 dBm into 50 Ω at 10 MHz), e.g. mi TF 2600A.
d	RF attenuator, e.g. mi TF 2163.
e	RF amplifier, e.g. mi TF 2175.
f	Comb generator (or narrow pulse generator).
g	VHF detector, e.g. mi TM 9701.
h	Oscilloscope, general purpose, 15 MHz.

4.2.2 Calibrator

Test equipment : items a, b, c.

Frequency :

(a) Connect the counter to the STANDARD 10 MHz OUTPUT of TF 2370. Check that the output frequency is ±20 Hz of 10 MHz.

(b) Remove counter.

Amplitude :

Set the controls to the following positions :

VERTICAL SCALE RANGE	- 1 dB/DIV
VERTICAL SCALE	- -7 dBm
HORIZONTAL SCALE	- 10 kHz/DIV
FILTER BANDWIDTH	- WIDE '3'

(a) Set the signal generator frequency to 10 MHz and its level, using the voltmeter (item c), to -10 dBm. Apply the signal to INPUT 50 Ω, and note the level.

(b) Disconnect the signal, and connect the STANDARD 10 MHz OUTPUT to INPUT 50 Ω. Check that the level is within ±0.3 dB of the level in (a).

4.2.3 Tracking generator

Test equipment : items d, g, h.

Frequency (tracking accuracy) :

Set the controls as follows :

HORIZONTAL SCALE	- 0.02 kHz/DIV
FILTER BANDWIDTH	- WIDE '3'
VERTICAL SCALE RANGE	- 1 dB/DIV
VERTICAL SCALE	- -10 dBm
COUNTER FREQUENCY	- BRIGHT LINE
SWEEP MODE	- MANUAL
STORE	- REFRESH 'A'
BRIGHT LINE POSITION	- CENTRAL

(a) Connect the STANDARD 10 MHz OUTPUT to INPUT 50 Ω, and tune the analyser using the REFERENCE FREQUENCY control and the COUNTER READOUT.

(b) Using the BRIGHT LINE control carefully position the top of the 50 Hz filter response on the 1 dB/DIV display.

(c) Switch the FILTER BANDWIDTH to NORMAL '2' and the STORE to REFRESH 'B'. Carefully bring in the 5 Hz filter by rotation of the BRIGHT LINE POSITION control. Note the difference in amplitude between the two responses.

(d) Return FILTER BANDWIDTH to WIDE '3' and STORE to REFRESH 'A'. Replace STANDARD 10 MHz signal with TRACKING GENERATOR OUTPUT, and establish a new reference level by rotating the BRIGHT LINE POSITION control.

(e) Switch to NORMAL '2' and REFRESH 'B'. Slowly rotate the BRIGHT LINE POSITION control, and note the difference between this level and the level in (d).

(f) Subtract the difference obtained in (c) from the difference obtained in (e) and use this value to find the error in frequency shown in Fig. 4.1. This should be within ±2 Hz of the input tuned frequency.

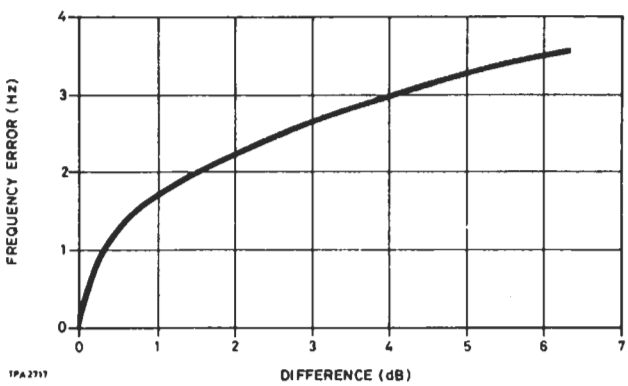


Fig. 4.1 Frequency error

Amplitude and frequency response

Set the controls to the following positions :

VERTICAL SCALE RANGE	- 1 dB/DIV
VERTICAL SCALE	- 0 dBm (-7 dB on 1 dB step)
HORIZONTAL SCALE	- 10 kHz/DIV
FILTER BANDWIDTH	- NORMAL '2'
SWEEP MODE	- AUTO

(a) Connect the STANDARD 10 MHz OUTPUT to INPUT 50 Ω, and tune the analyser to 10 MHz using the COUNTER READOUT. If necessary adjust the GAIN control to calibrate the analyser to the -10 dBm input level taking into account any error of the STANDARD signal indicated in the amplitude check in Section 4.2.2.

(b) Disconnect the STANDARD 10 MHz OUTPUT, and connect the TRACKING GENERATOR. Measure the TRACKING GENERATOR output level at 10 MHz. This should be -10 dBm ±2 dB.

(c) Disconnect the TRACKING GENERATOR from the INPUT 50 Ω, and connect it to the attenuator. Connect the output of the attenuator to the detector, and monitor the detector output with the oscilloscope.

(d) Adjust the attenuator from 0 to 1 dB, and calibrate the oscilloscope gain and shift controls so that a 2 division change occurs. The oscilloscope will now read 0.5 dB/division.

(e) Remove the attenuator and connect the detector direct to the TRACKING GENERATOR OUTPUT. Measure the frequency response at 1 MHz and at every 10 MHz up to 110 MHz, adjusting the 0-110 MHz REFERENCE FREQUENCY control, and using the COUNTER READOUT. Note results.

(f) Replace the detector with the voltmeter, and re-set the following controls :

HORIZONTAL SCALE	- 0.1 kHz/DIV
SWEEP MODE	- MANUAL

(g) Using all four REFERENCE FREQUENCY controls, as necessary, tune to 10 MHz using the COUNTER READOUT. Note the voltmeter reading this being the new reference level. Tune to 100 kHz, 10 kHz, 1 kHz, 100 Hz and 30 Hz, and measure the frequency response.

The frequency response, relative to the 10 MHz level, should be ±1 dB from 100 Hz to 100 MHz, and -3 dB at less than 30 Hz and greater than 110 MHz.

4.2.4 Amplitude measurement

Test equipment : items d, e.

Frequency response :

(a) Connect the TRACKING GENERATOR OUTPUT to INPUT 50 Ω, and set the controls as follov

HORIZONTAL SCALE	- 10 MHz/DIV
FILTER BANDWIDTH	- NARROW '1'
VERTICAL SCALE RANGE	- 1 dB/DIV
SWEEP MODE	- AUTO
VERTICAL SCALE	- -5 dBm

(b) Adjust the REFERENCE FREQUENCY controls so that the d.c. marker is positioned on the left-hand dashed graticule line. Shift the dB graticule to normalize the response at 10 MHz.

(c) Check the combined TRACKING GENERATOR/analyser frequency response at 10 MHz intervals from 1 MHz to 110 MHz, and note results.

(d) Reset the following controls :

HORIZONTAL SCALE	- 0.02 kHz/DIV
VERTICAL SCALE RANGE	- 10 dB/DIV
VERTICAL SCALE	- 0 dBm
SWEEP MODE	- MANUAL
COUNTER FREQUENCY	- BRIGHT LINE
BRIGHT LINE POSITION	- CENTRAL

(e) Reset the reference level by adjusting the dB graticule at 10 MHz. Tune the analyser to 100 kHz, 10 kHz, 1 kHz, 100 Hz and 30 Hz, and measure the error in the displayed signal at each frequency. Note the response figures.

(f) Subtract the response obtained in (c) from the response in (e), and ensure that the input frequency response is ±1 dB, relative to the 10 MHz level, from 100 Hz to 110 MHz, and -3 dB at less than 30 Hz.

Vertical scale range accuracy :

(a) Connect the equipment as in Fig. 4.2.

(b) Set the analyser to 1 dB/DIV at +30 dBm, and COUNTER ON/OFF switch to ON. Set the attenuator (item d) to 0 dB, and select the VERTICAL SCALE (1 dB step attenuator) position that gives a display at the centre of the screen.

(c) Set the analyser sweep width to 0.02 kHz/DIV, FILTER BANDWIDTH to NORMAL '2', and SWEEP MODE to MANUAL. Tune the analyser to 2 MHz as indicated by COUNTER READOUT.

(d) Using the 'slideback' technique, check the accuracy of the analyser input attenuator from +30 to -90 dBm (10 dB steps) against the attenuator (item d); the error being the change in level of the analyser display. The accuracy should be ±0.3 dB/10 dB; cumulative error less than ±1.5 dB.

Note Take into account any attenuation error present in item d.

(e) Repeat check (d) from -90 dBm to -50 dBm using 2 kHz/DIV. Accuracy should be ±0.3 dB/10 dB; cumulative error less than ±1.5 dB.

(f) Select 0 dBm position of the analyser input attenuator, and set 1 dB step attenuator to 0 dB. Adjust attenuator (item d) for a display in the centre of the screen, using the GAIN control if necessary.

(g) Repeat check (d) on the 1 dB step attenuator. Accuracy should be ±0.1 dB/1 dB; cumulative error less than ±0.3 dB.

(h) Repeat (c) and (d) at 100 MHz.

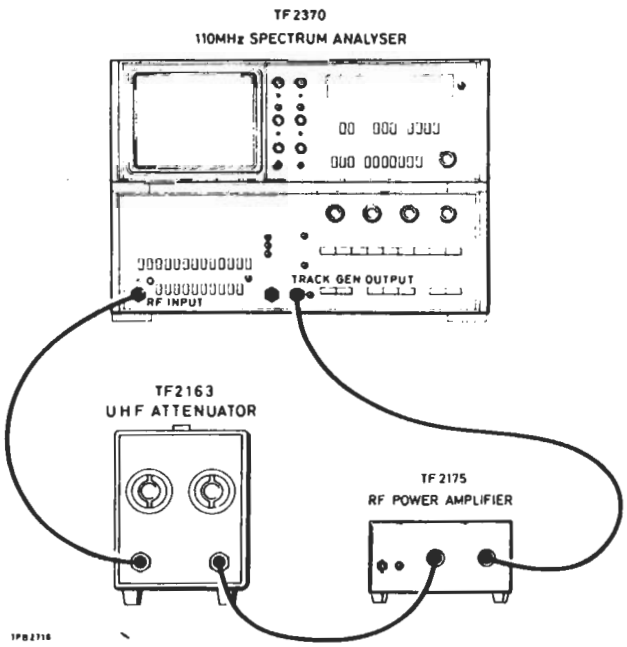


Fig. 4.2 Connection diagram—vertical scale range accuracy

Gain :

(a) Connect STANDARD 10 MHz OUTPUT and INPUT 50 Ω together using a short length of 50 Ω coaxial cable.

(b) Set the controls as follows :

HORIZONTAL SCALE	- 1 kHz/DIV
FILTER BANDWIDTH	- WIDE '3'
VERTICAL SCALE RANGE	- VOLTS/DIV
VERTICAL SCALE	- 10 mV/DIV

(c) Set the zero signal level to the zero datum graticule line using the VERTICAL SHIFT control. Switch to 10 dB/DIV, and adjust the VERTICAL DISPLAY GAIN control to align the displayed

signal with the -10 dBm graticule line (1 major division from the top of the screen). Switch to 1 dB/DIV, set the VERTICAL SCALE to -10 dBm, and adjust the GAIN control until the displayed signal just touches the top graticule line (-10 dBm). Repeat these adjustments for optimum setting.

(d) Switch VERTICAL SCALE RANGE control to VOLTS/DIV, and the VERTICAL SCALE to 10 mV/DIV, and check that the STANDARD 10 MHz signal is displayed at a level between 67 and 74 mV.

(e) Switch in 3 dB's of gain using the VERTICAL SCALE control (1 dB step attenuator), and adjust the GAIN control so that the STANDARD 10 MHz signal is displayed at the top graticule line. Switch to 30 mV/DIV and check that the displayed signal is between 3.2 and 3.4 major divisions from the bottom graticule line. Reset the GAIN control to the calibrated position.

(f) Check that the cover of the GAIN control allows the signal to be increased at least 5 dB, and decreased at least 2 dB about the correct calibration level. Finally calibrate the analyser to the correct level.

Vertical scale display accuracy :

(a) Connect the equipment as in Fig. 4.2 and repeat section (b) of vertical scale range accuracy.

(b) Switch to 1 dB/DIV, and adjust the display to the top of the screen using the GAIN control. Switch in 1 dB steps of attenuator (item d), and check the accuracy of the screen display. This should be : overall law accuracy ±0.1 dB.

(c) Switch to 10 dB/DIV, and repeat (b), switching in 10 dB steps of the attenuator (item d). The accuracy should be : overall law accuracy 0 to -80 dB, ±1 dB; -80 to -100 dB, ±1.5 dB.

Bandwidth dispersion switching accuracy :

(a) Connect STANDARD 10 MHz OUTPUT and INPUT 50 Ω together with a short length of 50 Ω coaxial cable.

(b) Switch to 10 dB/DIV, and set a reference level on the screen with the 5 kHz filter in use. Switch through all combinations of FREQ/DIV and FILTER BANDWIDTH noting any changes in level. The maximum error should be ±1.0 dB ±1% f.s.d. on LOG, and ±10% on LINEAR.

Average noise level :

Set the controls as follows :

VERTICAL SCALE RANGE	- 10 dB/DIV
VERTICAL SCALE	- -50 dBm
HORIZONTAL SCALE	- 1 kHz/DIV
FILTER BANDWIDTH	- NORMAL '2'
COUNTER ON/OFF	- OFF
SWEEP MODE	- MANUAL

(a) Observe the average noise level displayed on the screen. This should be below -130 dBm (i.e. 8 major divisions from the top of the screen).

4.2.5 Frequency measurement

Test equipment : items a, f.

Range of controls :

Set the controls to the following positions :

COUNTER FREQUENCY	- BRIGHT LINE
SWEEP MODE	- MANUAL
REFERENCE FREQUENCY	- CENTRE
HORIZONTAL SCALE	- 0.1 MHz/DIV
FILTER BANDWIDTH	- NARROW
COUNTER ON/OFF	- ON

(a) Connect the counter (item a) to the TRACKING GENERATOR OUTPUT. Turn the REFERENCE FREQUENCY controls fully counter-clockwise.

(b) Tune the 0-110 MHz control over the frequency range, and check that it continuously covers from below zero to above 110 MHz. Select kHz/DIV RANGE, and check that the control tunes in 1 MHz phase locked steps over the same frequency range.

(c) Set the 0-110 MHz control to a convenient frequency, for example 10 MHz, and check the total cover of the other three REFERENCE FREQUENCY controls. This should be nominally 2 MHz, 140 kHz and 2 kHz respectively.

Note The 2 MHz cover control is phase locked every 100 kHz in the kHz/DIV mode.

Reference frequency selection :

Set the controls as follows :

COUNTER FREQUENCY	- PAST CENTRE
REFERENCE FREQUENCY	- CENTRE
HORIZONTAL SCALE	- 1 MHz/DIV
FILTER BANDWIDTH	- WIDE '3'
SWEEP MODE	- AUTO

(a) Set COUNTER READOUT with REFERENCE FREQUENCY controls at zero, then switch from CENTRE to LH.

(b) Adjust HORIZONTAL GRATICULE SHIFT to align the d.c. marker to the left-hand dashed frequency graticule line.

(c) Switch from LH to CENTRE, and adjust HORIZONTAL GRATICULE GAIN control to align centre dashed frequency graticule line behind the d.c. marker.

(d) Set HORIZONTAL SCALE control to 0.02 MHz/DIV, and FILTER BANDWIDTH to NARROW '1'. Align the d.c. marker to coincide with the centre dashed frequency graticule line.

(e) Switch HORIZONTAL SCALE control to 10 MHz/DIV, reset FILTER BANDWIDTH to WIDE '3', and ensure that the d.c. marker is still on the centre line, ±1% of f.s.d. This may be measured by moving the d.c. marker into alignment with the centre graticule line using the REFERENCE FREQUENCY controls, and measuring the shift in MHz on the counter, item a, (1 MHz = 1% f.s.d.).

Sweep mode function :

(a) Select AUTO, and READ IN B/U display. Switch through all HORIZONTAL SCALE MHz/DIV and kHz/DIV ranges, and check that they automatically sweep.

(b) Select MANUAL, and check that the analyser does not automatically sweep but may be manually swept by adjustment of the BRIGHT LINE POSITION control.

(c) Select SINGLE, and check that one sweep may be initiated by depressing the SWEEP MODE START switch.

Sweep range accuracy :

Set the controls as follows :

SWEEP MODE	- AUTO
COUNTER FREQUENCY	- PAST CENTRE
REFERENCE FREQUENCY	- LH
VERTICAL SCALE RANGE	- 10 dB/DIV
HORIZONTAL SCALE	- 0.5 MHz/DIV
FILTER BANDWIDTH	- NORMAL '2'
COUNTER ON/OFF	- ON

(a) Connect the comb generator to INPUT 50 Ω.

(b) Select analyser sensitivity to give a satisfactory display of 1 MHz comb markers across the screen.

(c) Adjust REFERENCE FREQUENCY controls to check every 5 MHz increment of the 0 to 110 MHz range. Note the frequencies of maximum and minimum error of the displayed comb, with respect to the display graticule.

(d) At both frequencies found in (c), check all positions of the HORIZONTAL SCALE control, using the appropriate comb frequency for each range. Ensure that all ranges are within ±10% of full-scale ±20 Hz, against the electronic graticule.

(e) Set the 0-110 MHz and ±1 MHz REFERENCE FREQUENCY controls to give a counter reading of approximately 1 MHz. Adjust the ±70 kHz REFERENCE FREQUENCY control fully counter-clockwise, and press the CENTRE, REFERENCE FREQUENCY control. Switch to WIDE '3', FILTER BANDWIDTH, and apply a 10 kHz comb on the 10 kHz/DIV sweep range.

(f) Using the counter reading as a guide, check the total range of the ±70 kHz control noting the frequencies of the maximum and minimum graticule errors. With the control fully clockwise switch the REFERENCE FREQUENCY to LH, and check the comb calibration.

(g) At both frequencies found in (f), check all positions of the HORIZONTAL SCALE using the appropriate comb frequency for each range, with the FILTER BANDWIDTH at NORMAL '2'. All ranges should be within ±10% of full-scale ±20 Hz, against the electronic graticule.

Sweep speed function :

(a) This check ensures that the nominal sweep speeds are being correctly selected. Table 4.1 shows sweep speeds derived by HORIZONTAL SCALE and FILTER BANDWIDTH selection. Visual observation of the trace on the screen is sufficient to determine any errors of selection.

Table 4.1

Sweep speed against HORIZONTAL SCALE and FILTER BANDWIDTH selection

Horizontal scale	Filter 1 Narrow	Filter 2 Normal	Filter 3 Wide
10 MHz/div	10 s	100 ms	100 ms
5	5 s	100 ms	100 ms
2	2 s	100 ms	100 ms
1	1 s	100 ms	100 ms
0.5	500 ms	100 ms	100 ms
0.2	200 ms	100 ms	100 ms
0.1	10 s	100 ms	100 ms
0.05	5 s	100 ms	100 ms
0.02	2 s	100 ms	100 ms
10 kHz/div	100 s	1 s	100 ms
5	50 s	500 ms	100 ms
2	20 s	200 ms	100 ms
1	10 s	10 s	100 ms
0.5	5 s	5 s	100 ms
0.2	2 s	2 s	100 ms
0.1	100 s	100 s	1 s
0.05	50 s	50 s	500 ms
0.02	20 s	20 s	200 ms

(b) Repeat check (a) for HORIZONTAL SCALE positions shown in Table 4.2, using the x5 SWEEP SPEED control.

4.2.6 Frequency counter

Counter functions and accuracy :

Set the controls to the following positions :

HORIZONTAL SCALE	- 10 MHz/DIV
FILTER BANDWIDTH	- WIDE '3'
VERTICAL SCALE RANGE	- 10 dB/DIV
VERTICAL SCALE	- -10 dBm
SWEEP MODE	- AUTO
COUNTER FREQUENCY	- BRIGHT LINE

(a) Adjust the REFERENCE FREQUENCY controls so that the d.c. marker aligns with the left-hand dashed frequency graticule line.

(b) Connect STANDARD 10 MHz OUTPUT and INPUT 50 Ω together, and dim out the graticule using the GRATICULE CONTRAST control. Switch the SWEEP MODE to SINGLE.

(c) Align the BRIGHT LINE cursor behind the d.c. marker, using the BRIGHT LINE POSITION control, and check the COUNTER READOUT. This should indicate between 0 and 1 MHz.

(d) Shift the BRIGHT LINE cursor behind the 10th harmonic of the STANDARD 10 MHz signal, and check the COUNTER READOUT which should indicate between 99 and 101 MHz.

(e) Set the COUNTER FREQUENCY controls to DIFFERENCE. Check that the COUNTER READOUT indicates approximately zero when the BRIGHT LINE cursor is central, and approximately 50 MHz when the BRIGHT LINE cursor is either on the d.c. marker or the 100 MHz line.

Table 4.2

Sweep speeds using × 5 SWEEP SPEED control

Horizontal scale	Filter 1 Narrow x5	Filter 2 Normal x5	Filter 3 Wide x5
10 kHz/div	20 s	-	-
5	10 s	-	-
2	5 s	-	-
1	2 s	-	-
0.5	1 s	-	-
0.2	500 ms	-	-
0.1	-	-	200 ms
0.05	-	-	100 ms
0.02	-	-	100 ms
0.02 MHz/div	-	-	100 ms

(f) Reset the COUNTER FREQUENCY controls to BRIGHT LINE. Reset to AUTO sweep and PAST CENTRE. Switch the COUNTER ON/OFF switch OFF, and check that the counter stops functioning (reads zero). Check also that the amber light adjacent to the TRACKING GENERATOR OUTPUT is illuminated.

Note If the COUNTER FREQUENCY controls are set to DIFFERENCE when the COUNTER ON/OFF switch is OFF, the COUNTER READOUT will display the contents of the latch.

4.2.7 Display

Display functions :

Set the controls as follows :

SWEEP MODE	- AUTO
VERTICAL SCALE RANGE	- 10 dB/DIV
STORE/DISPLAY	- HIGH DEFN
HORIZONTAL SCALE	- 0.05 MHz/DIV
FILTER BANDWIDTH	- WIDE '3'
VERTICAL SCALE	- 0 dBm

(a) Connect STANDARD 10 MHz OUTPUT and INPUT 50 Ω together.

(b) Adjust the REFERENCE FREQUENCY controls to position the STANDARD 10 MHz signal to the left-hand side of the graticule.

(c) Press the STORE, REFRESH 'A', and the DISPLAY 'A' and 'B' buttons, then re-position the display to the right-hand side of the graticule. The stored 'B' display will now be on the left, and the refreshed 'A' display on the right. By switching the 'A' and 'B' DISPLAY buttons ensure that either signal can be removed from the screen.

(d) With both 'A' and 'B' pictures displayed, press the REFRESH 'B' button and re-position the display on the left-hand side of the graticule. Display 'A' should now be observed as before but in reverse. Repeat the DISPLAY 'A' and 'B' checks in (c).

(e) Press the HIGH DEFN button, and check that the DISPLAY 'A' and 'B' switches have no effect.

(f) Press the PEAK MEMORY button, and check that the largest noise signal applied at each point across the screen is stored on the display.

(g) Press the READ IN B/U button and select FILTER BANDWIDTH, NARROW '1'. The display should be brightened up at the data renewal point as it is swept across the screen.

Display controls :

(a) Set the analyser as for display functions check, sections (a), (b) and (c).

(b) Check that the INTENSITY 'A' control varies the brightness of display 'A', and the INTENSITY 'B' control varies the brightness of display 'B'. Both controls should be capable of producing very bright (excessive brilliance) displays down to low brilliance (but not cut-off).

(c) Press the HIGH DEFN button, and check that INTENSITY 'A' control is the only control which varies the display brilliance.

(d) Position the signal to the centre of the screen. Check that the cover of the VERTICAL SHIFT control is at least 1 major division; reset to initial level.

(e) Check that the cover of the VERTICAL DISPLAY GAIN control is at least ±10% of the signal amplitude; reset to initial level.

Chapter 5

Repair

5.1 INTRODUCTION

This chapter contains information for the repair and overall realignment of the instrument, and is to be used in conjunction with the circuit diagrams at the rear of the manual. Performance limits mentioned are for guidance only, and should not be taken as guaranteed performance specifications unless they are also quoted in the Data Summary section.

CAUTION

Integrated circuits and semiconductor devices are used throughout this instrument and, although these have inherent long term reliability and mechanical ruggedness, they are susceptible to damage by overloading, reversed polarity and excessive heat or radiation. Avoid hazards such as prolonged soldering, strong r.f. fields or other forms of radiation and the use of insulation testers.

In case of difficulties which cannot be resolved with the aid of this book, please contact our Service Division at the address given on the rear cover, or your nearest Marconi Instruments representative. Always mention the type and serial number of your instrument.

5.2 SCREW FASTENERS

Most screws used in this instrument are ISO metric and are the following sizes : M1.6, M2, M2.5, M3 and M4.

Other screws used are 4BA nylon and 4BA brass.

5.3 ACCESS AND REMOVAL OF UNITS

WARNING

The following operations are performed with the instrument switched OFF, and disconnected from the supply unless otherwise stated.

Display unit—removal of covers and access

Remove top cover by withdrawing four M4 screws (two at each side), and lifting away. The bottom cover is similarly removed.

Extender Board 44827-235 is available for use with boards AD, AE, AF and AG series. The boards are removed by being carefully pulled from the edge connector sockets using Board Extractor 41700-048.

RF unit—removal of covers and access

Remove the display unit by unplugging Connector Assemblies 43169-005 from the rear of the r.f. unit, and releasing two toggle latches at each side of the r.f. unit. The display unit can now be lifted clear. Remove the top and bottom covers of the r.f. unit by withdrawing four M4 screws from each cover (two at each side) and lifting away.

Turn the display and r.f. units on their sides and position as illustrated in Fig. 5.1. Two blocks of wood approximately 50 mm x 25 mm x 300 mm are best positioned beneath each unit to give clearance for the side handles, and provide stability on the bench.

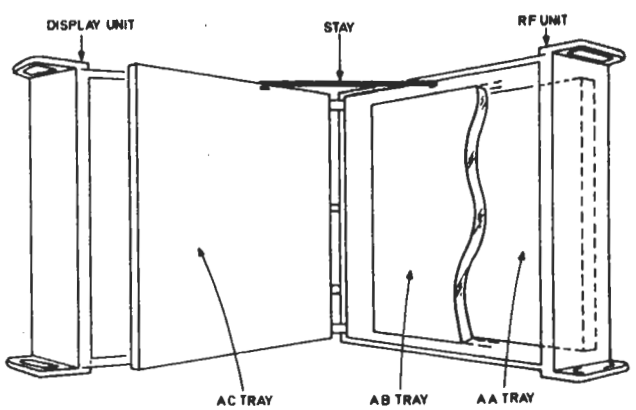


Fig. 5.1 Instrument positioned for access to r.f. unit

For access to the AB and AC trays, hinge out the AC tray to an approximate right angle after removing two M4 screws at each side of the tray, which fix the tray to the unit side panels. Secure the tray in position with Stay Assembly 34900-209. One end of the stay is attached to an anchor nut midway along the side of the tray. The other, anchor nut end, by an M4 screw inserted through a hole in the top edge of the unit side panel, and screwed into the stay anchor nut.

CAUTION

When the AC tray is hinged in position, ensure that it does not short against the display unit.

Re-connect connector assemblies.

EHT unit—removal

WARNING

Before attempting any work on the e.h.t. unit make sure that the supply is disconnected from the instrument. Detach the final anode lead from the c.r.t. and short it against the e.h.t. chassis several times immediately it is unplugged.

The c.r.t. also retains a charge which must be shorted to earth before handling. This is best done by inserting a screwdriver into the final anode cavity and shorting it to the main chassis.

The e.h.t. unit has a red cover and is situated at the rear, left-hand side of the display unit. To remove the unit, lift off the cover which is secured by two M4 nuts. Remove two M4 nuts from studs protruding through board AL1, which is positioned across the top of the e.h.t. unit. Hinge board AL1 upwards on its back edge, and unsolder the red/white lead on AL1 tag 8, and the screened lead on AL1, TR2 base.

Remove four M4 nuts from the underside of the display unit, which secure the e.h.t. unit to the power supply chassis. Take off c.r.t. cover (lift and pull cover at rear). Disconnect final anode plug from c.r.t.

The e.h.t. unit may now be lifted out.

Cathode ray tube—replacement

WARNING

The c.r.t. retains a charge for a considerable time after switch-off, and must be shorted to earth as detailed in the WARNING above. Also see above WARNING for discharging final anode lead.

Take off the c.r.t. cover, and carefully remove the c.r.t. base connector. Remove the final anode plug from the c.r.t. Loosen the 4BA cheese head screw in the deflector coil clamp ring. Release the spring harness hook from the front panel frame. With extreme care manoevre the c.r.t. backwards free of the front bezel, slip the magnetic focusing ring off the end of the c.r.t., and withdraw the c.r.t. from the deflector coils.

Reverse the above procedure when replacing the c.r.t. ensuring that the moulded rubber seal is fitted to the front of the c.r.t. Before tightening the deflector coil clamp ring make the following adjustments :

(a) Connect the instrument to the supply and switch ON. Obtain an electronic graticule display.

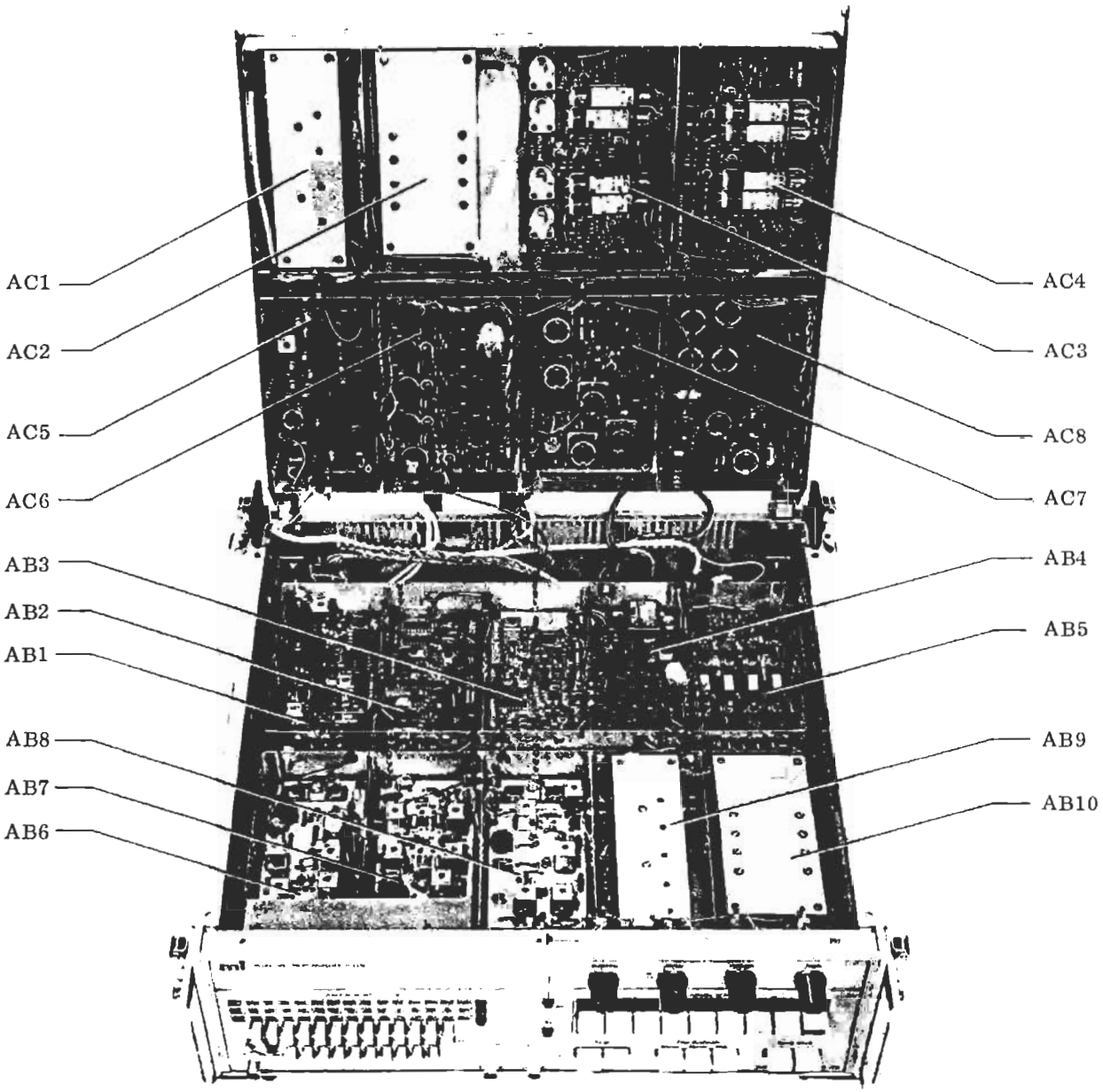
(b) Turn the plastic clamp moulding of the deflector coil assembly until the vertical graticule lines are upright.

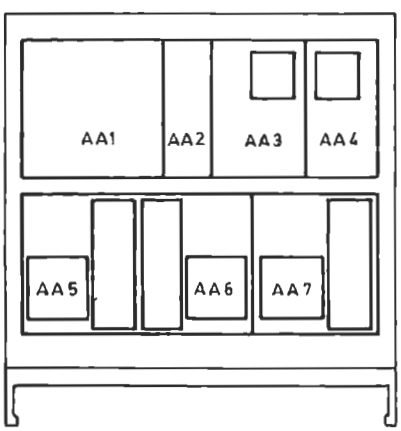
(c) Adjust, by turning, the shuffle plates to centralize the c.r.t. picture.

(d) By gripping the linearity sleeve lugs, gently slip the linearity sleeve into the deflector coil assembly until best spacing of the horizontal graticule lines is achieved, consistent with good picture shape.

(e) Re-set the shuffle plates, if necessary, and tighten the deflector coil clamp ring.

(f) With the magnet of the magnetic focusing ring uppermost, gently turn the ring, as necessary, to improve the graticule line focusing at the corners of thc picture.





Unit viewed from below

Fig. 5.3 Location of units—r.f. unit

Power supply chassis—removal

WARNING

Discharge c.r.t. and final anode lead as previously described.

The power supply chassis, which houses the e.h.t. and power supply units, is situated across the rear of the display unit, and is removed as follows :

Take off c.r.t. cover and disconnect final anode plug. Remove e.h.t. cover. Withdraw two M4 screws at each side of display unit which fix the black guard strips to the rear panel. Remove three M4 screws fixing the power supply chassis to the main chassis, situated along the front edge of the power supply chassis.

Remove four M2.5 screws fixing sockets SKB and SKC to the rear panel, and withdraw the sockets through the panel. Disconnect the main frame connector, underneath the main chassis.

The power supply chassis is now free to lift out.

5.4 TEST POINTS

A number of test points are available on the printed boards, and may be located using the circuit diagrams in Chapter 7.

Waveforms are given on the circuit diagrams for most test points, together with control settings of the TF 2370. The waveforms were monitored and photographed on a dual trace, 100 MHz bandwidth, oscilloscope using a x10 (10 MΩ) probe. Horizontal and vertical sensitivities (at the probe tip) are given together with details of external triggering where applicable.

Photographs containing more than two waveforms were compiled by multiple exposure.

5.5 LOCATION OF SUB-ASSEMBLIES

Fig. 5.2 and Fig. 5.3 show the location of sub-assemblies. The display and r.f. unit outer and inner covers are removed, and the AC tray of the r.f. unit is hinged out.

5.6 COMPONENT LOCATION

All printed boards are marked with a legend which allows the precise location of a component part by its circuit reference number.

5.7 FAULT LOCATION

The following sections comprise fault finding charts and test schedules which provide a systematic procedure for localizing faults to comparatively small groups of components. The system operates as follows:

1. Start with the overall fault finding chart, Fig. 5.4, which gives a branched sequence of checks, symptoms and actions related to the display. This will enable you, without removing the covers, to localize the fault to one of 9 functional areas, indicated by a boxed title, e.g. STORE.

2. Go to the section corresponding to the suspected functional area; this includes an area fault finding chart and/or a step-by-step test schedule. If there is a fault finding chart, start with this to further localize the fault; if the branch ends with a boxed title or code, e.g. AE4a, go to that part of the associated test schedule for further instructions.

To assist fault finding it is advisable to study the appropriate part of the circuit description in Chap. 3 and to check the waveforms and voltages included on the circuit diagrams.

In the event of failure of the 1st local oscillator boards AA5 and AA6 or the shaper circuit on AA1 (as diagnosed by fault-finding chart Fig. 5.5) do not attempt to recalibrate locally but return the complete instrument to Marconi Instruments Ltd. - see rear cover for addresses.

Note After completing a repair it is advisable to carry out the appropriate part of the realignment procedure in Sect. 5.8.

5.7.1 Overall equipment

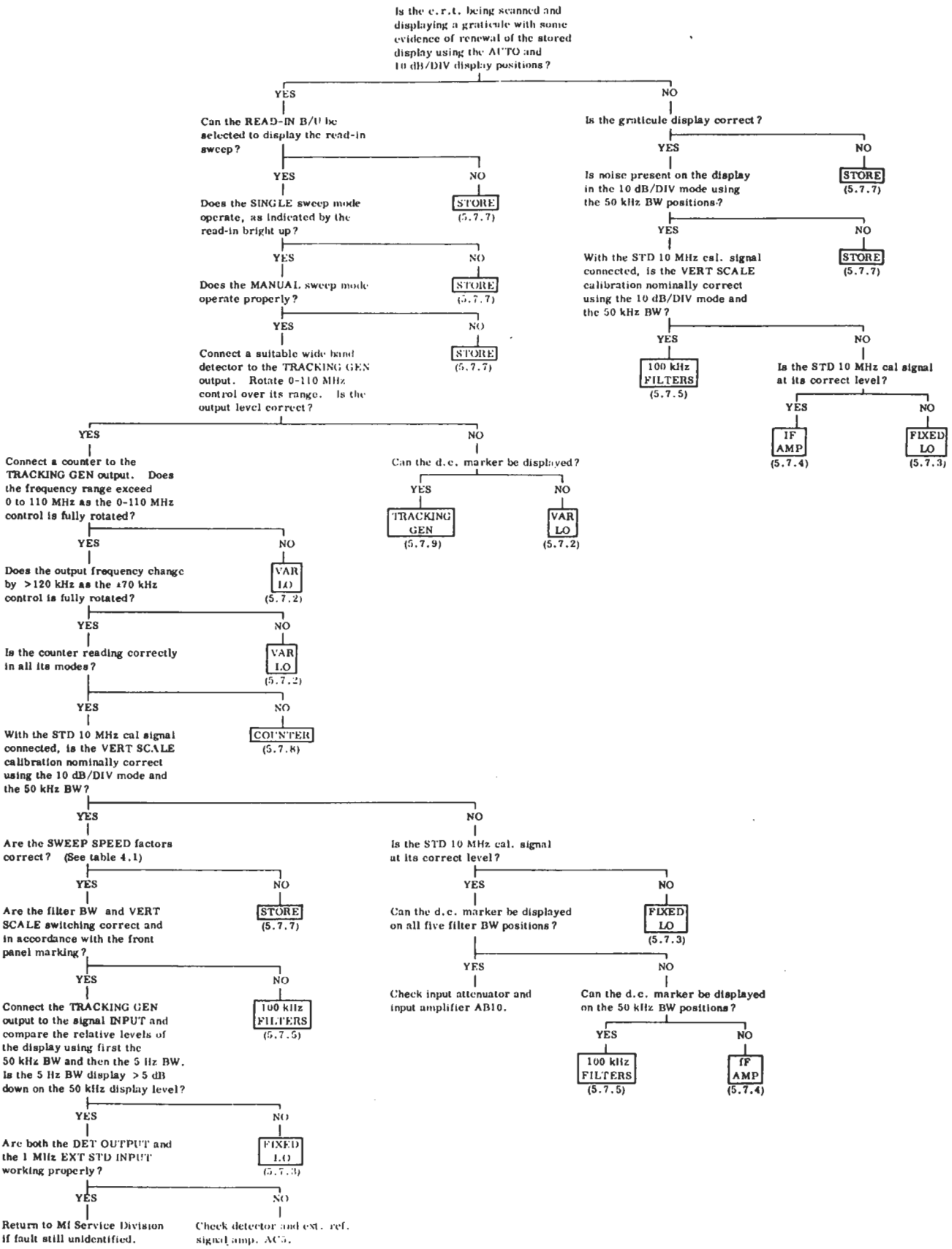


Fig. 5.4 Fault finding chart—OVERALL EQUIPMENT

5.7.2 Variable local oscillators - AA1 to AA7

Circuit diagrams—Figs. 7.10 to 7.16

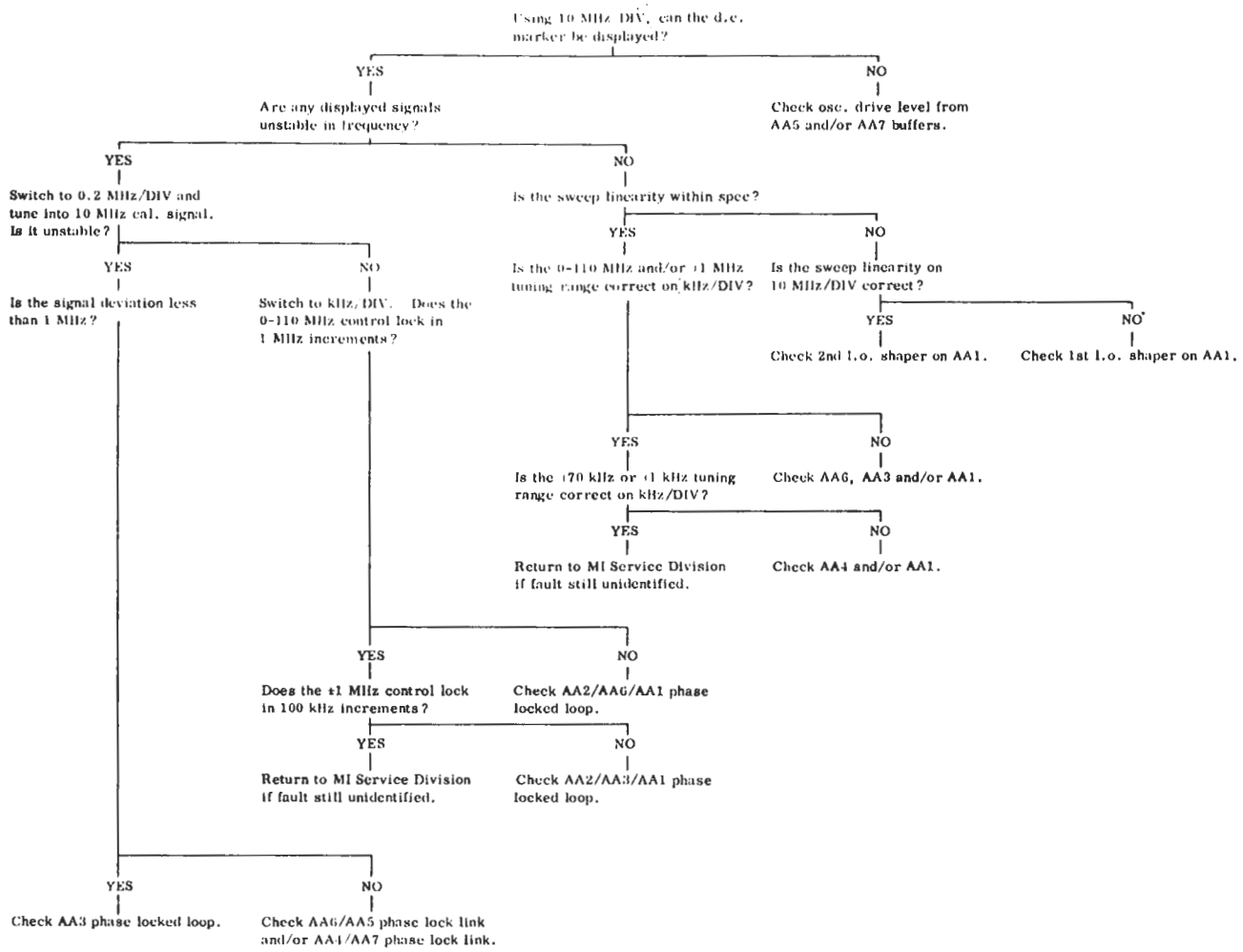


Fig. 5.5 Fault finding chart—VARIABLE LOCAL OSCILLATORS

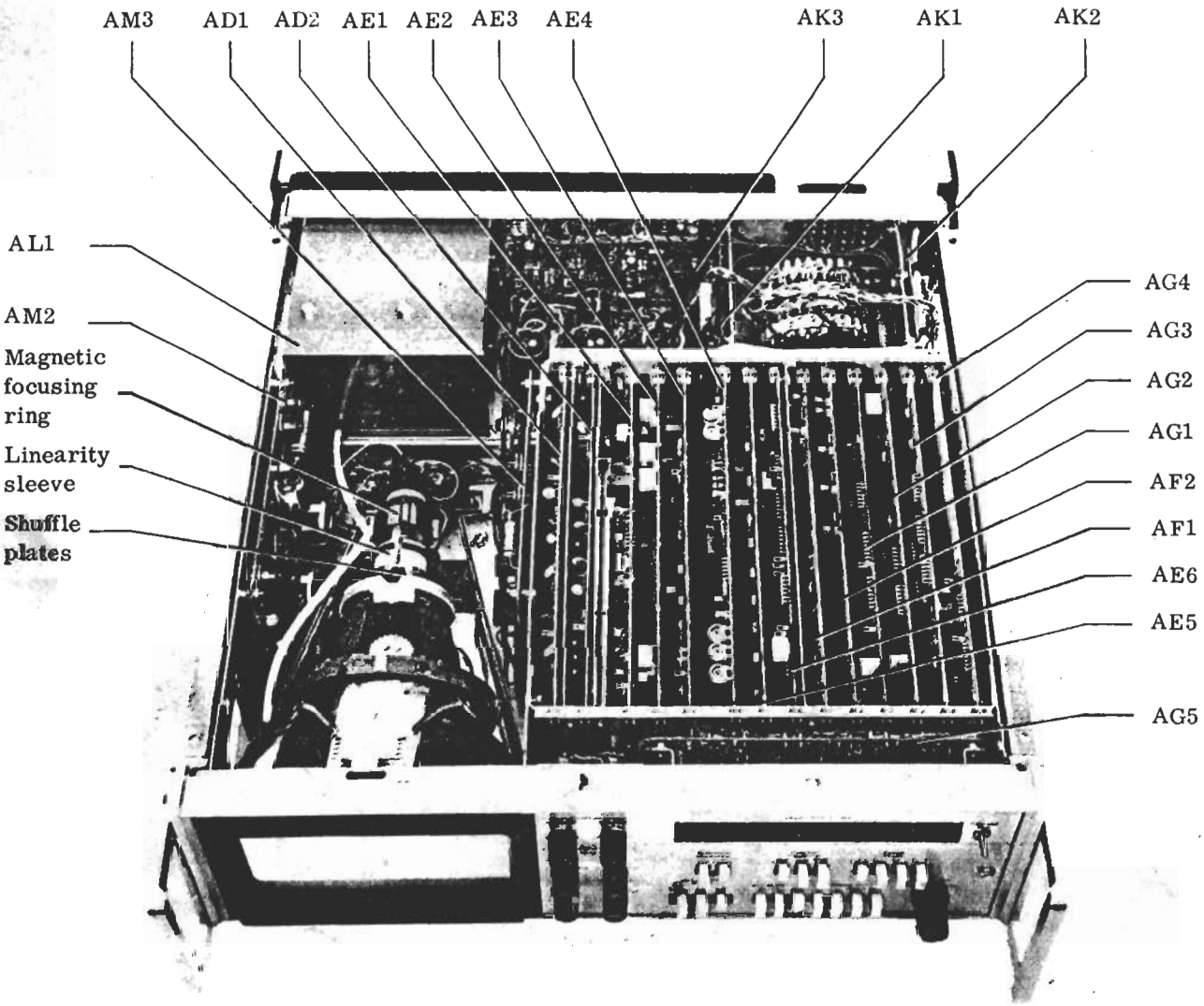


Fig. 5.2 Location of units—display unit

5.7.3 Fixed local oscillators - AB1 to AB4

Circuit diagram—Fig. 7.9

(1) If the STD 10 MHz cal signal is at the incorrect level or absent, check back through AB4 TR6, TR5, TR4 and dividers IC1b2, IC1a2 for fault.

(2) If the STD 10 MHz cal signal is more than 20 Hz in error, suspect the 80 MHz phase locked crystal oscillator is in error or the 10 MHz reference standard (AB4 X 1) has stopped.

(3) If the TRACKING GEN output signal is off tune, suspect the 36.4 MHz phase locked crystal oscillator on AB1 is not phase locked.

(4) To remedy, check for the presence of the 100 kHz drive signal on AB1 pin 2. Check that TR2 produces a pulse, ringing at approximately 36 MHz, across the primary of AB1 T2.

(5) If the fault has still not been found, break the link between AB1 pins 9 & 10. Connect a high impedance voltmeter to pin 10 and arrange a pair of resistors to bias pin 9 to -3 V. Adjust AB1 R30 so that the voltage on pin 10 reads -3 V also. Connect a counter to the link between AB1 pins 11 and 12, and check that frequency of oscillator is 36.400 MHz, if not adjust core of L3 on AB1 until the frequency is correct. Reconnect the link between pins 9 & 10.

5.7.4 IF amplifiers - AB6 to AB10

Circuit diagrams—Figs. 7.7 and 7.8

Note A calibration table showing internal signal levels is given on circuit diagram Fig. 7.7.

(1) Check that the STD 10 MHz cal signal is present and accurate; then apply this to the INPUT socket. Select 0.02 MHz/DIV, WIDE filter, MANUAL mode and the BRIGHT LINE counter position and tune in to 10.0 MHz. Select 10 dB/DIV and an indicated input sensitivity of -10 dBm at the top of the screen.

(2) Measure the signal level on AB8 pin 5; it should be -17 dBm at 3.6 MHz. If the signal is low enough to account for fault, check levels as in (3). If the level is approximately right, proceed as in (4).

(3) Check that the following signal levels are present on board AB8:-

pin 3:	+8 dBm	at 40 MHz
TP4:	-12 dBm	at 36.4 MHz
TP3 :	-15 dBm	
TP2 :	-18 dBm	
TP1 :	-14 dBm	
pin 1 :	-19 dBm	

If the fault is still not found, check the following signals are present on board AB10a:-

pin 2 :	-26 dBm	at 10 MHz
pin 3 :	-26 dBm	
TR3 collector :	-18 dBm	
TR4 collector :	-18 dBm	
pin 6 :	-30 dBm	

If the fault is still not found, remove the inner lid from AB9 and check that the following signals are present:-

R port of AZ1 :	+13 dBm	at 210 MHz
L port of AZ1 :	-22 dBm	at 200 MHz
L1 tap :	-14 dBm	
L3 tap :	-11 dBm	
L5 tap :	- 8 dBm	
L7 tap	-10 dBm	
R port of AZ2 :	-13 dBm	
X port of AZ2 :	+ 8 dBm	at 236.6 MHz
L port of AZ2 :	-20 dBm	at 36.4 MHz

(4) As the level is correct on AB8 pin 5, measure the signal level at :-

AB7 pin 5 :	-17 dBm	at 400 kHz
AB6 pin 5 :	-17 dBm	at 100 kHz

This will establish where the signal loss is occurring and the following list of approximate signal levels will help locate the fault :-

AB7	TP1 :	- 4 dBm	at 3.6 MHz
	TP2 :	- 2 dBm	at 3.6 MHz
	TP3 :	- 3 dBm	at 3.6 MHz
	TP4 :	-13 dBm	at 3.6 MHz
	pin 3:	+ 9 dBm	at 4.0 MHz
AB6	TP1 :	+ 2 dBm	at 400 kHz
	TP2 :	-10 dBm	at 400 kHz
	TP3 :	- 8 dBm	at 400 kHz
	TP4 :	-12 dBm	at 400 kHz
	pin 3:	+10 dBm	at 500 kHz
AC6	TP1 :	0 dBm (640 mV p-p)	at 100 kHz
AC6	TP6 :	+17 dBm (4.5 V p-p)	at 100 kHz
AC7	pin 10:	+20 dBm (6.4 V p-p)	at 100 kHz

5.7.5 100 kHz filters—AC3, AC4 and AC8

Circuit diagram—Fig. 7.17

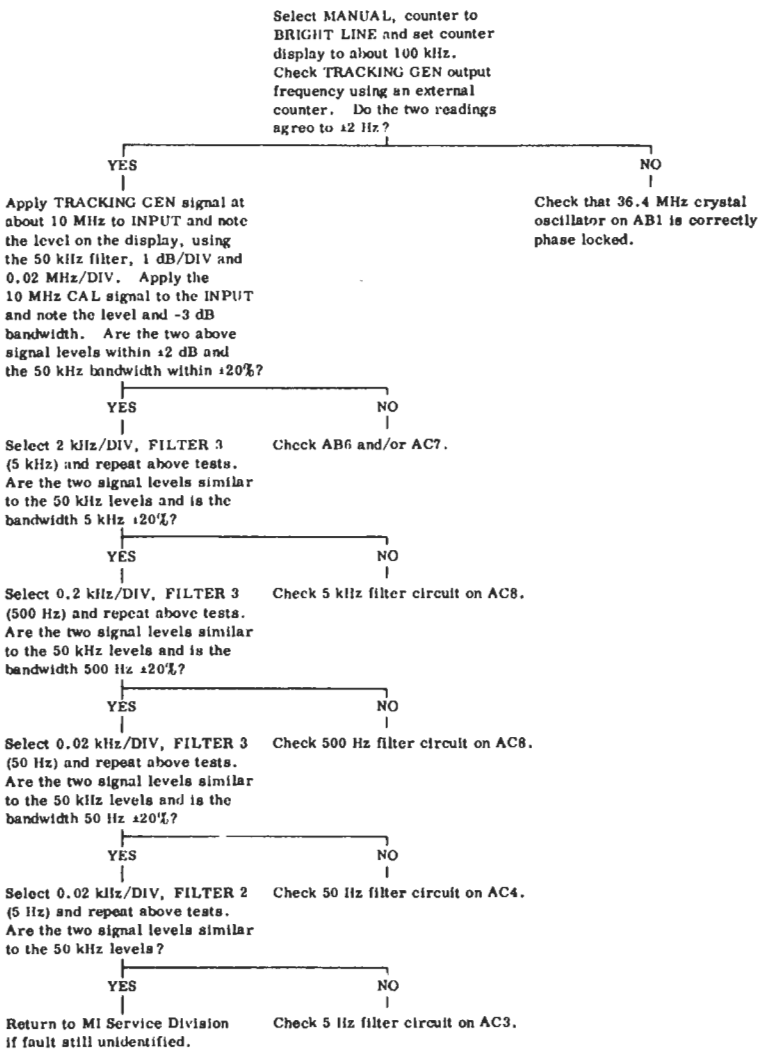


Fig. 5.6 Fault finding chart—100 kHz FILTERS

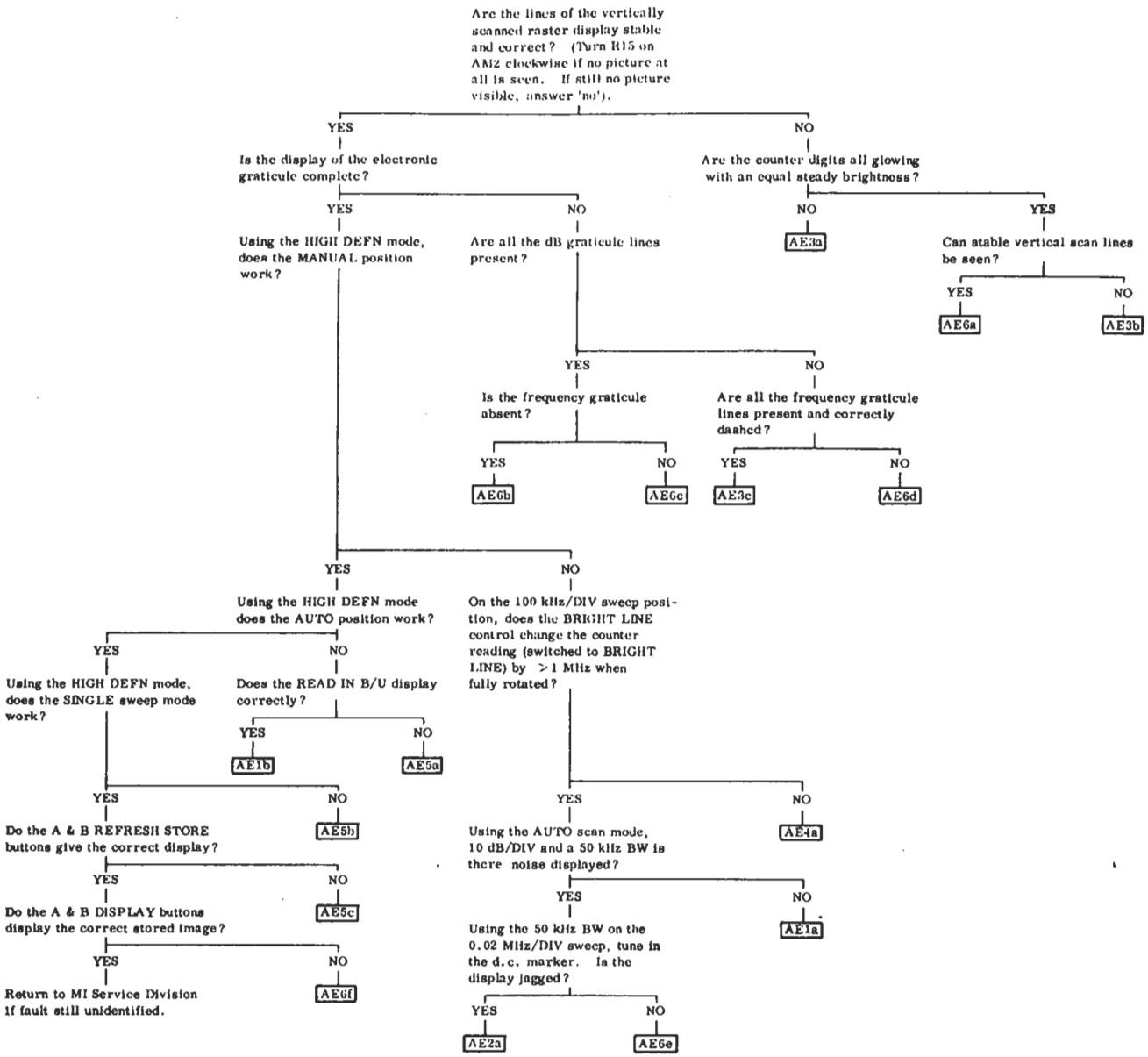


Fig. 5.7 Fault finding chart—DIGITAL STORE

5.7.6 Log amplifier—AD1 and AD2

Circuit diagrams—Figs. 7.8, 7.17 and 7.18

(1) Select a 50 kHz filter position and MANUAL mode. The most insensitive VERTICAL SCALE button (300 mV or +30 dBm) should be used, and the 0 dB button used on the lower row.

(2) Apply a signal from a calibrated 50 Ω signal generator at 100 kHz (±10 kHz) to SK K (-see Fig. 7.8). Attach a 10:1 oscilloscope probe to AD1 pin 32 to monitor the signal level at the input to the log amplifier.

Volts/DIV

If the instrument was not faulty in this position, proceed to the 10 dB/DIV section. If it was faulty in this position, proceed as follows:-

(i) Adjust the level of the signal generator output until the monitoring oscilloscope displays a peak-to-peak level of 2.5 V. Switch in 40 dB of attenuation to produce an input signal of 25 mV p-p.

(ii) Transfer the probe to AD1 TP6; the signal level should be 2.5 V p-p. If it is not, check back through TP5, TP4 and TP3 to see where the gain discrepancy occurs; the signal level at each test point should be 10 dB larger than the previous one.

If the level is correct at TP6, check the level at AD2 TP5; it should be 2.7 V p-p. If it is not, check AD2 IC4a3, R57, R58, R59 and C23, the Volts/DIV switching and AD1 R62, R63 and C28.

If the level is correct at TP5, measure the d.c. level on AD2 TP7; it should be 1.3 V d.c. If it is not, check detector circuit IC4c3, TR3.

If the level is correct at TP7, check the output at AD2 pin 4; it should be +2 V d.c. If it is not, check IC5 and associated switching and circuitry.

If the level is correct at pin 4, and the screen does not display top of the screen signal level, see AE1 fault finding guide in Sect. 5.7.7.

10 dB/DIV

If the instrument is only faulty on the 1 dB/DIV position proceed to the next section; if not, proceed as follows:-

(i) Replace the oscilloscope probe on AD1 pin 32 and adjust the signal generator output such that the oscilloscope displays 6.4 V p-p. Check that the d.c. level at AD2 pin 29 is -6 V and that it changes to +15 V when the 500 Hz, 50 Hz and 5 Hz filters are selected. Switch back to the 50 kHz filter if correct.

(ii) Measure the signals at AD1 TP2 to 9 and AD2 TP10 and 11. They should all be limiting at 4 V p-p with a mean level of about +3 to +4 V. If this is so, measure the signal at AD2 TP5. This should be about 3 V p-p. If it is not, reduce the input signal in 10 dB steps and observe if the signal on TP5 reduces by 0.27 V for each step. If there is a fault in the current summing transistors (TR2, IC1b3, IC2b3, IC3b3 on AD1 and IC3b3 on AD2) some indication of where the fault might lie can be obtained by noting at what input level the signal at AD2 TP5 departs from 0.27 V/10 dB. The offending stage will be at or near the point in the signal chain where the signal is just limiting.

(iii) If the signal on AD2 TP5 is correct and the output at AD2 pin 4 is still wrong, the fault can only be in switching of the leads from AD2 pins 1, 3, 7, 8, 9 and 26 as the detector circuit is known to be working on Volts/DIV.

1 dB/DIV

(i) Replace the oscilloscope probe on AD1 pin 32 and adjust the signal generator output such that the oscilloscope displays 6.4 V p-p. Now add 40 dB of attenuation so that the input signal is 64 mV p-p.

(ii) Measure the signal level at AD2 pin 17; it should be 2.0 V p-p. If this is so, check the signal level at AD2 TP1; this should be a just limiting sinewave of 4 V p-p. Similarly, check the signal at AD2 TP2, 3 and 4 for 4 V p-p signals, each successive one limiting rather more severely.

(4) Check at AE5 pin 26 for 400 ns +ve pulses. If present, check the connection from AE5 pin 26 to AE1 pin 26.

(5) If pulses are not present here, and the 'ordinates' pulses on pin 13 are present (read-in bright up would not work if these were absent), check pin 25 is at logic '1'.

(6) Check 'ordinates' pulses through IC9b and c and IC8b.

AE2a

(1) Select WIDE BANDWIDTH, SINGLE, .02 MHz/DIV and tune to the d.c. marker.

(2) Connect AE1 TP10 to earth.

(3) Check inputs at AE2 pins 20 to 13 in sequence for square waves increasing in duration by factors of 2 from 0.8 μs at pin 20 to 102.4 μs at pin 13.

(4) If any input is faulty, check outputs on AE1.

(5) Select AUTO and disconnect TP10 from earth.

(6) Check that outputs at AE2 pins 23 to 30 perform logic level transitions. If not, check at TP1 and TP2 for 100 ns -ve going pulses of +5 to -11 V excursion every 800 ns, with the TP2 waveform displaced half a period from that of TP1.

AE3a

(1) Disconnect the drive to the line scan and e.h.t. units by removing board AM2.

(2) Check at AE3 pin 3 for a 10 MHz 180 mV p-p square wave input from AB4.

(3) Check the following supply lines :-

pin 10 : + 6 V
pin 11 : +15 V
pin 12 : + 5 V
pin 21 : -15 V
pin 22 : - 6 V

(4) Check at pin 1 for 2.5 MHz square wave clock output with rise and fall times of about 50 ns. With this drive the counter should multiplex correctly.

AE3b

(1) Disconnect the drive to the line scan and e.h.t. units by removing board AM2.

(2) Check the following supply lines :-

pin 10 : + 6 V
pin 11 : +15 V
pin 12 : + 5 V
pin 21 : -15 V
pin 22 : - 6 V

(3) Check at pin 19 for a 51.2 μs squarewave (at logic levels).

(4) Check pin 7 for a 9 μs -ve pulse every 51.2 μs. With these two drives the line scan and e.h.t. should work. However, as a precaution, turn down all INTENSITY controls before operating the instrument with board AM2 replaced.

AE3c

(1) If the fault is in the graticule shift, go to (5).

(2) Check at AE3 pin 8 for 220 ns -ve pulses every 4 μs. Trigger from +ve edge at TP3 and check that the pulses can be moved in time by operating the GRATICULE VERTICAL SHIFT control.

(3) Check at pin 9 for 60 ns -ve pulses every 0.8 μs.

(4) If both (2) and (3) are present, check connections to IC9 on AE6. If not, check drives from IC7 to monostables IC8.

(5) Check at AE3 pin 13 for a 26.26 ms square wave.

(6) Check at TP4 for 6 μs +ve pulses every 26.26 ms, the width being variable by the GRATICULE VERTICAL SHIFT control.

(7) Check at TP5 that the 2.5 MHz square wave is stopped during this 6 μs interval.

(8) Check that IC7 pins 11 and 12 reset to '1' when there is a -ve going pulse on pin 20.

(9) Check that the -ve pulse on pin 20 occurs every 51.2 μs.

(iii) If these signals are correct and the output at AD2 pin 4 is not +2 V d.c., then the fault must lie in the current summing transistors IC1b3, IC2b3 or the range switching on leads from AD2 pins 14, 6, 7, 8 and 9.

5.7.7 Digital store - AE1 to AE6

Circuit diagrams—Figs. 7.19 to 7.24

Use the fault finding chart, Fig. 5.7, to localize the fault to one of these 17 functional areas.

AE1a, AE1b, AE2a, AE3a, AE3b, AE3c, AE4a, AE4b, AE5a, AE5b AE5c, AE6a, AE6b, AE6c, AE6d, AE6e, AE6f.

Then carry out the procedure detailed under the appropriate heading below:

Note Waveform levels in this section are all t.t.l. compatible unless otherwise specified.

AE1a

(1) Select WIDE BANDWIDTH, AUTO, 10 dB/DIV and 10 MHz/DIV. Ensure PEAK MEM is off.

(2) Check at AE1 pin 4 for a signal of greater than 0 V d.c. If not, go to Sect. 5.7.6.

(3) Check AE1 pin 26 for 400 ns +ve pulses every 230 μs.

(4) Check that IC4 pin 8 is at logic '1'.

(5) Check for pulse waveforms at TP8, TP9, TP10, pin 9 and pin 8 as in Fig. 5.8.

(6) Select MANUAL and check that TP2 and TP5 are at the same potential as pin 4.

(7) Select AUTO and connect pin 4 to earth.

(8) Check for waveform at TP12 as in Fig. 5.8.

(9) Select MANUAL and disconnect pin 4 from earth.

(10) Check at TP6 for about twice the voltage at TP2 +1 V.

(11) Connect pin 4 to earth again and check at TP13 for a waveform as in Fig. 5.8 with voltage excursion from 0 V to the new potential at TP6.

(12) Check at IC4 pin 11 for burst of 2.5 MHz clock pulse as in Fig. 5.8 while TP11 is low.

(13) Switch to SINGLE and connect TP10 to earth.

(14) Check outputs at pins 20 to 13 in sequence for square waves increasing in duration by factors of 2 from 0.8 μs at pin 20 to 102.4 μs at pin 13.

(15) Remove earth connections.

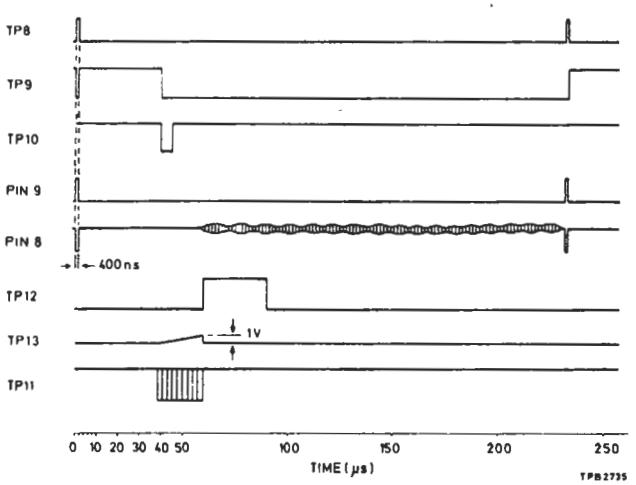


Fig. 5.8 AE1a waveforms

AE1b

(1) Select WIDE BANDWIDTH, AUTO, HIGH DEFN, 10 dB/DIV and 10 MHz/DIV. As MANUAL operation is correct, the fault must lie in IC3 or the switching and pulses to it.

(2) Check that AE1 pin 25 is at logic '0'.

(3) Check at AE1 pin 26 for 400 ns +ve pulses.

(i) If present, check TP8 for similar pulses;

(ii) If not present, check AE5 as follows :

AE4a

(1) If the fault condition is the bright line sticking at the centre of the screen as the BRIGHT LINE POSITION control is moved counter clockwise :-

(a) Select SINGLE and MANUAL alternately and see if the fault clears.

(b) If it clears, select AUTO and check that AUTO sweeps run normally. It is most likely if AUTO sweeps fail to run that the 'T time' pulse on AE4 pin 20 is not working.

(c) To check this, remove AG1 and check if all troubles have cleared (except that the counter will not now operate). If this is the case, the fault lies on AG1 and associated circuitry.

(2) No bright line appears in SINGLE or MANUAL :-

(a) Check that TP1 is at 6 V or greater. If not, check that pin 17 and pin 20 are at logic '1'.

(b) Check that TP4 voltage varies between <7.5 V and >11.5 V as the BRIGHT LINE POSITION control is operated. If TP4 is correct, check for a similar voltage swing on TP5 and TP6.

(c) Check at pin 14 for an output of 0 to >10 V.

If sweep on TP4 is correct :-

(a) Check waveform at TP5 and TP6. The waveform at TP5 is similar to that on TP4 except for a slight increase in gain, and that on TP6 is similar except that it lacks the small -ve step.

(b) If TP5 is correct, or TP6 is faulty, check pins 27, 28, 29, 30 are at logic '0', '1', '0' and '0' respectively.

(c) Check at the following points :-

TP10 and TP12 : 0 V
TP11 : +15 V
TP13, TP14 and TP15 : -12 V or below

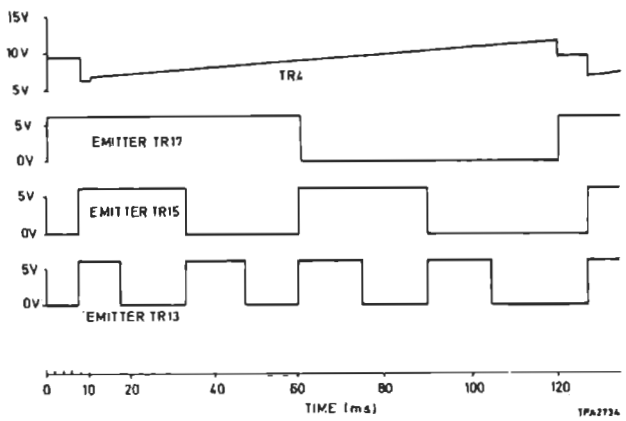


Fig. 5.9 AE4b waveforms

AE4b

(1) If fault is ±10% tracking error between the bright-up and the auto read-in point, check at AE4 pin 14 for an output of 0 to 10 V exactly on AUTO sweep.

(2) If 0 to 10 V is correct, readjust the tracking error using AE6 R20 and R22.

If 0 to 10 V is not correct, select AUTO, MHz/DIV and WIDE BANDWIDTH and check sweep on TP4 as in Fig. 5.9.

(3) If sweep on TP4 is not correct, check at emitters of TR4, 5, 6, 7, 9, 11, 13, 15 and 17 for 6 V square wave, the last three as shown in Fig. 5.9.

AE5a

(1) Select WIDE BANDWIDTH, AUTO, HIGH DEFN and .02 MHz/DIV.

(2) If fault is incorrect sweep speeds go to (11).

(3) If the fault is a failure of auto sweeps to run, remove board AG1 and re-check. If this is a cure, check that 'T time' pulses from AG1 to AE5 pin 20 are 2 ms -ve pulses every 120 ms.

(4) If fault is otherwise, or fails to be cured, connect TP7 to earth and check that pin 15 is at logic '1'. If at '0', check that TP8 is at '1'. Keep TP7 earthed and check at TP4 for 40 μs, +ve pulses every 231 μs.

(5) If not present, check back through the divider chain (TP1 and TP2). If the pulse repetition rate is incorrect, check inputs on pins 27, 28, 29 and 30 for logic '0', '1', '0' and '0' respectively.

(6) Check at pin 13 for 400 ns -ve pulses every 231 μs.

(7) Check at TP5 for a 118 ms square wave.

(8) Check at pin 19 for 5 μs -ve pulses every 118 ms.

(9) Disconnect TP7 from earth and check at TP7 for 0.2 μs -ve pulses every 205 μs. If not present, remove board AG1 and recheck. Check also at TP6 for +ve 0.2 μs pulses.

(10) Check at pin 26 for 400 ns +ve pulses every 231μs.

(11) For incorrect sweep speed operation check the following logic states :-

Pins					
27	28	29	30	Switch to	
0	1	0	0	0.2 MHz/DIV, WIDE, AUTO	
0	1	0	1	0.2 MHz/DIV	NARROW, AUTO
0	1	1	0	0.5 MHz/DIV	
0	1	1	1	1.0 MHz/DIV	
1	0	0	1	2.0 MHz/DIV	
1	0	1	0	5.0 MHz/DIV	
1	0	1	1	10.0 MHz/DIV	
1	1	0	1	2.0 kHz/DIV	
1	1	1	0	5.0 kHz/DIV	
1	1	1	1	10.0 kHz/DIV	

If correct, check at TP4 for 40 μs +ve pulse every 231 μs, 436 μs, 1051 μs, 2078 μs etc., in a roughly 1-2-5-10 series.

If this is correct, go to AE4a and check table against similar pins and logic on this board.

If AE4a is incorrect, check connections to board AG4.

AE5b

(1) Select WIDE BANDWIDTH, SINGLE and MHz/DIV.

(2) Check that TP8 goes to logic '0' when the START button is pressed and held in.

(3) Check also that IC21 pin 8 is at logic '0' (with START pressed).

(4) Check at TP7 for 0.2 μs -ve pulses every 205 μs (with START pressed).

(5) Check on releasing START that IC21 pin 8 goes to logic '1' (triggered from -ve going edge on IC21 pin 13).

AE5c

(1) Select REFRESH A, WIDE BANDWIDTH, AUTO and MHz/DIV.

(2) Check at pins 23 and 24 for 462 μs square waves in antiphase to each other.

(3) Check that on REFRESH A the waveform at pin 23 is in phase with that at pin 25, and on REFRESH B the waveform at pin 24 is the same as at pin 25.

(4) By comparing the waveforms at pins 13 and 26 check that alternate pulses at pin 13 are gated out by the square waves at pin 25.

AE6a

(1) Disconnect the drive to the line scan and e.h.t. units by removing board AM2.

(2) Check at pin 29 for 200 μs +ve pulse every 13.13 ms. Check that the pulse amplitude is >2 V starting from -150 mV. This is the only drive to the field scan board AM3.

AE6b

(1) Check at pin 20 for 400 ns -ve pulses every 51.2 μs.

(2) Check at TP3 for 51.2 μs +ve pulses approx. every 1 ms (depending on calibration of graticule gain.) If not present, check at IC1b pin 5 and the trigger signal to IC1b at TP1, where there should be 2 ms +ve pulses every 13.13 ms.

If pulses are present on TP3, connect TP4 to earth and proceed with (3).

(3) Check for partial frequency graticule (no dashed lines).

If the partial graticule is present, check signals to IC7 and IC4.

If the partial graticule is not present, determine why signals from TP3 do not arrive at IC8 pin 8.

AE6c

If extra graticule lines are present (12th, 13th etc.) excepting the 16th (dashed) line, check at TP2 for 'frequency graticule mask' pulses every 13.13 ms. These blank out all but the eleven lines normally displayed.

If the dashed lines are missing, check TP4 and TP5. TP4 has three -ve pulses during the duration of the +ve pulse at TP5, as in Fig. 5.10.
If non-dashed lines are missing, check at TP2 and TP3. If no lines are dashed, check at TP5 and IC8 pin 12 for 'add stripes' signal.

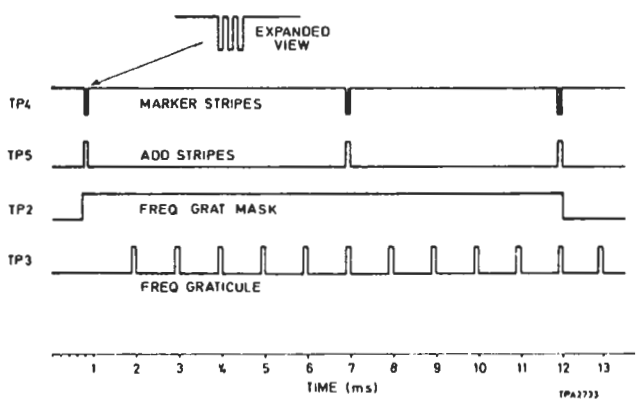


Fig. 5.10 AE6c waveforms

AE6d

(1) Check at pin 20 for 400 ns -ve pulses every 51.2 μs. If absent, go to AE3c.

(2) If the frequency graticule lacks the dashed lines only, and the amplitude graticule lacks the major divisions, check at pin 8 for 220 ns -ve pulses every 4 μs.

If absent, go to AE3c.
If present, check drive to IC7 pin 3 and IC9 pin 1.

(3) Check at pin 9 for 60 ns -ve pulses every 0.8 μs.

(4) Check that the pulses on pins 8 and 9 appear inverted and added at TP6.

If there is no signal on TP6, check that IC9 pin 2 is at logic '1'. If '0', go to AE6c. If '1', suspect IC9 or the tracks associated with IC9 pins 1, 2, 13 or 12.

AE6e

(1) Check if READ IN B/U and AUTO work satisfactorily. If B/U only is faulty, check:-

TP9 : 10 V ramp every 13.13 ms, starting from 0.3 V.

TP10 : (with AUTO, WIDE and MHz/DIV selected) 10 V ramp every 120 ms.

TP11 : (with SINGLE selected and using BRIGHT LINE) a +ve pulse should appear as TP9 voltage passes that of TP10.

If B/U and AUTO are faulty go to AE4b.

If AUTO and READ IN B/U are correct, proceed with (2).

(2) Select HIGH DEFN and check pin 32 for 400 ns -ve pulses every 51.2 μs.

(3) Select MAN and check at IC10 pin 12 for 51.2 μs +ve pulses every 13.13 ms, i.e. at the pulse repetition rate on TP11.

(4) Check at pin 28 for 400 ns +ve pulses every 13.13 ms.

If all correct, check for this pulse on AE1 pin 27 and check through to AE1 TP8.

AE6f

If fault is in A, B or A+B only go to (1), (2) or (3) as appropriate.

(1) Select DISPLAY A and check :-

pin 25 : 26.26 ms square wave
pin 27 : logic '1'
pin 26 : logic '0'
TP15 : -ve pulses (triggered from -ve edge on TP7)

Select DISPLAY B and check that TP15 is at logic '1'.

(2) Select DISPLAY B and check :-

pin 25 : 26.26 ms square wave
pin 27 : logic '0'
pin 26 : logic '1'
TP16 : -ve pulses (triggered from TP7)

Select display A and check that TP16 is at logic '1'.

(3) Select DISPLAY A + B and check :-

pin 25 : 26.26 ms square wave
pins 27 and 26 : both logic '1'
pins 5 and 6 : 3.2 μs +ve pulses occurring at random times within the 51.2 μs between line rate pulses on TP7 (timing depends on the data stored in the shift register).
TP15 & TP16: -ve pulses (triggered from TP7) of varying durations according to the data in the store.

If all is correct, check the video mixer transistors TR7 and TR8 and their associated base drive resistors, potentiometers and switching.

5.7.8 Frequency counter—AG1 to AG5

Circuit diagrams—Figs. 7.27 to 7.31

Use the fault finding chart, Fig. 5.11, to localize the fault to one of these five functional areas :

AG1a, AG1b, AG2 & AG5, AG4a & AF1, AG4b. Then carry out the procedure detailed under the appropriate heading below.

Note Waveform levels in this section are all t.t.l. compatible unless otherwise specified.

CAUTION Counter display AG5. Remove link across current limiting resistor R59 prior to work on circuitry associated with transistors Nos. 1 to 18.

AG1a

(1) Select MANUAL and BRIGHT LINE and set the REFERENCE FREQUENCY to about 200 kHz. Check at AG1 pin 1 for a sine wave of 200 kHz, 400 mV p-p.

(2) Check at TP8 for a sine wave of 1.2 V p-p about a d.c. level of +7.8 V.

(3) Check at TP1 for a square wave with a slight ring on the leading edges and lying between +4.0 V (or greater) and +3.675 V (or less); adjust R8 if necessary. Increase the frequency to at least 110 MHz and check that the waveform becomes a distorted sine wave but maintains the voltage levels.

(4) Return to 200 kHz and check at TP7 for a 100 kHz square wave between +4.15 V (or greater) and +3.50 V (or less).

(5) Check at TP3 for 100 kHz, 75 ns +ve pulses between +4.5 V (or greater) and +0.4 V (or less). Check that pulses of the same size are still present when the input frequency is lowered to 27 Hz. Check that when the input frequency is raised to at least 110 MHz the pulses are still there, at a p.r.f. of half the input frequency and lying between +2.4 V (or greater) and +0.4 V (or less).

Is counter display illuminated?

YES

Are all digits evenly illuminated?

YES

Is the display of the decimal point correct?

YES

Select BRIGHT LINE, 0.1 kHz/DIV, MANUAL, FILTER 1. Is correct frequency displayed i.e. frequency of TRACKING GEN output?

YES

Are correct frequencies displayed on all ranges and filters?

YES

Position BRIGHT LINE cursor onto centre dashed graticule line and select AUTO, PAST CENTRE. Is the displayed frequency the same as in the previous bright line case?

YES

Enter a past centre frequency about 110 MHz into the centre frequency latch and then select DIFF mode. Does the counter 'difference' correctly for bright line frequencies slightly less than 110 MHz?

YES

Does the counter 'difference' correctly for bright line frequencies slightly greater than 110 MHz?

YES

Return to MI Service Division if fault still unidentified.

NO

Are control circuit waveforms correct to Fig. 5.14 (b)?

YES

Examine the centre frequency latch(es) appropriate to the incorrect digit(s).

NO

Examine control circuits on AG1 and AG2.

NO

Are control circuit waveforms correct to Fig. 5.14(c)?

YES

Examine the counter-down mode of the main divider chain.

NO

Examine control circuits on AG1 and AG2.

NO

Examine zero detection on AG1, AG2 and AG3, steering on AG2 and count direction change on AG1.

NO

Examine data multiplexing circuits on AG2 and AG5. Chock waveforms to Figs. 5.12 and 5.13.

NO

Check AG5 : IC5 and 6 and AG4 : IC8 and 9.

NO

Check time base on AG1 pin 9 to truth table below. Is it correct?

YES

SUBROUTINE 1

NO

AG1 a and AG4 b & AF1

NO

Is there 190 V d.c. on AG5 pin 28?

YES

Are there 1 kHz +ve pulses on AG5 pin 35?

YES

Examine data multiplexing circuits in AG2 and AG5. Check waveforms to Figs. 5.12 and 5.13.

NO

Is there a 2.5 MHz square wave on AG4 pin 1?

YES

AG4 a from step (2)

NO

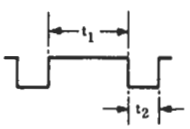
Look for broken wires etc.

NO

Check power supply.

TRUTH TABLE for AG1 pin 9

Filter	Range	Horiz. scale	t_1	t_2
1,2	kHz/DIV	.02, .05, .1	2 s	2 ms
3	"	.02, .05, .1	20 ms	2 ms
1,2	"	.2, .5, 1	200 ms	2 ms
3	"	.2, .5, 1	20 ms	2 ms
ANY	"	2, 5, 10	20 ms	2 ms
ANY	MHz/div	.02, .05, .1	2 ms	2 µs
ANY	"	.2, .5, 1	200 µs	2 µs
ANY	"	2, 5, 10	20 µs	2 µs



SUB-ROUTINE 1

Stay switched to BRIGHT LINE. Is the waveform at AG1 TP3 +ve 75 ns pulses at p.r.f. of f/2 (where f = tracking generator frequency)?

YES

Inhibit time base by connecting AG4 TP10 to 0 V at the correct time so that the main gate is held open, i.e. AG1 pin 9 is permanently in the '1' state. Is the waveform at AG1 pin 28 +ve pulses of 1:4 m/s at p.r.f. of f/20?

YES

Is the waveform on AG3 pin AH +ve 40 ns pulses at p.r.f. of f/20?

YES

Is the waveform on AG2 pin 26 +ve 40 ns pulses at p.r.f. of $f/2 \times 10^{-6}$?

YES3

Is the waveform on AG2 pin 19 a square wave of frequency $f/4 \times 10^{-8}$?

YES

If this applies to all values of f from 30 Hz to 110 MHz the main divider is working correctly and the fault must be in the main latch or control circuits. Are control circuit waveforms correct to Fig. 5.14(a)?

YES

Examine (i) BCD outputs of main divider and (ii) the main latch.*

NO

AG1a

NO

AG1b

NO

Examine AG2 steering : IC18 and IC12 (c), (d).

NO

Examine AG3 - see circuit description, Sect. 3.22.5.

NO

Examine AG2 dividers - see circuit description, Sect. 3.22.4.

NO

Examine AG1 IC5 and AG2 IC1.

* (i) comprises AG1 : IC2, 3, 9b, 9c, 10, 11b,
AG3 : IC1, 4, 7, 10, 13,
AG2 : IC2b, 5, 8.

(ii) comprises AG1 : IC6,
AG3 : IC3, 6, 9, 12, 15,
AG2 : IC7, 10, 11a.

Fig. 5.11 Fault finding chart --COUNTER

AG1b

Inhibit the time base with the main gate open as described in sub-routine 1 of Fig. 5.11.

(1) Check that AG1 pin 26 is in the '1' state and AG1 pin 29 is in the '0' state.

(2) Set the REFERENCE FREQUENCY to a suitable frequency (still on MANUAL, BRIGHT LINE) and check for waveforms as shown in Fig. 7.29.

Note that the waveforms shown relate to an input frequency of 2 MHz. As the frequency is increased the 75 ns pulses at TP3 deteriorate in shape and amplitude.

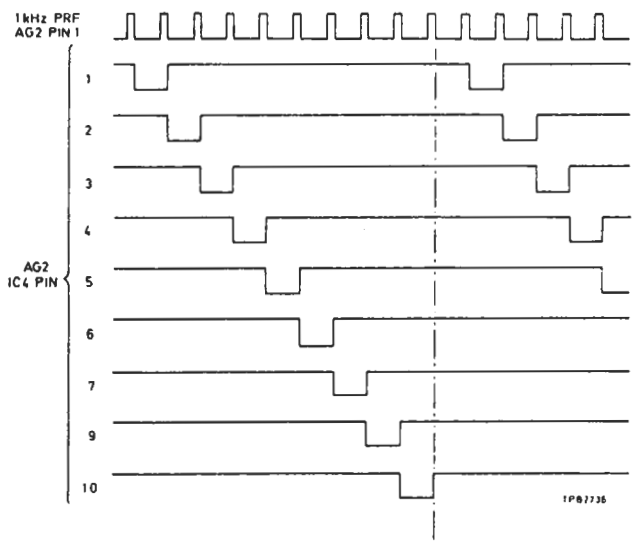


Fig. 5.12 AG2 waveforms

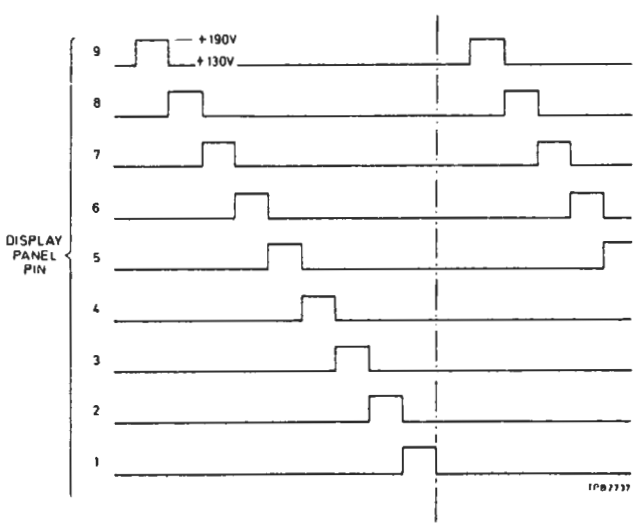


Fig. 5.13 Display panel waveforms

(3) Check for decoding as follows :-

Disconnect the 8 wires on AG5 pins 31,32,33, 34,36,37,38 and 39, and connect each of these pins via a 2 kΩ resistor to AG5 pin 29. Connect to earth (AG5 pin 30) as in the table below and check the display.

AG5 pins connected to earth	Display
ALL	000000000
31,32,33,36,37,38	111.111111
31,32,34,36,37,39	2222.22222
31,33,34,36,37	33333.3333
32,33,36,38,39	444444.444
32,34,36,38	5555555.55
33,34,36,39	66666666.6
36	777777.7.7.7
37,38,39	888888.8.8.8
37,38	999999.9.9.9

AG4a

Check that waveforms are as follows:-

AG4 pin 1 : 2.5 MHz square wave. If not, look for broken wires, dry joints etc.

TP1 : 500 kHz +ve pulses of 1:4 mark/space ratio. If not, check in order,

(i) Normally 0 V with 5 μs +ve reset pulses on IC1 pin 3.

(ii) IC1a, IC2 and IC10a.

TP2 (with TP8 connected to 0 V) : 50 kHz +ve pulses of 1:4 mark/space ratio. If not, check IC2 and IC3.

TP3 : 5 kHz +ve pulses of 1:4 mark/space ratio. If not, check IC3 and IC4.

AG4 pin 3 : 1 kHz +ve pulses of 1:4 mark/space ratio. If not, check IC4 and check that AG4 pin 3 is not being held externally.

TP4 : 500 Hz square wave. If not, check IC4 and IC10c.

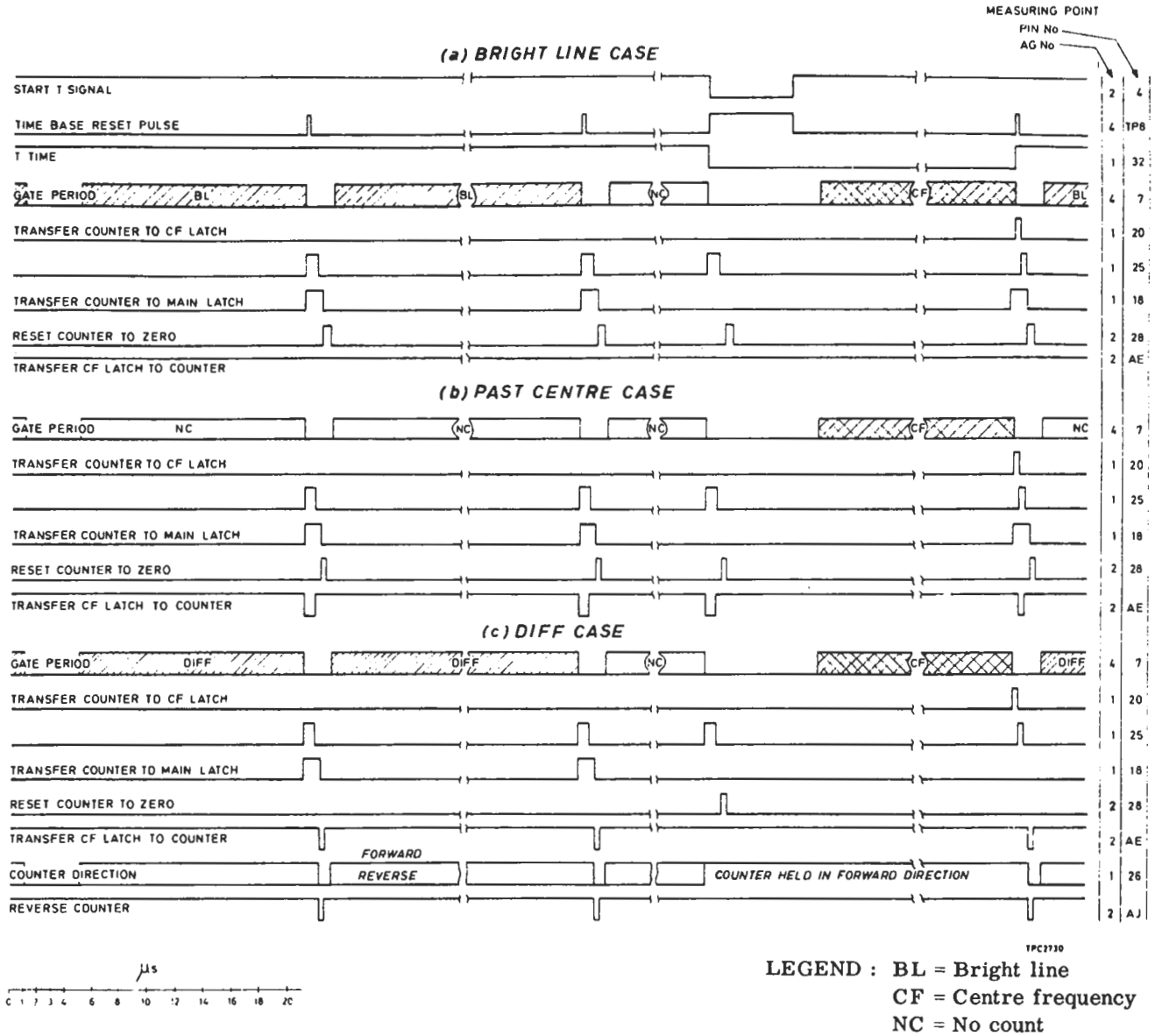


Fig. 5.14 Counter waveforms

AG4b & AF1

(1) Verify the table below :-

Filter	Range	Horiz. scale	AG4 pins 14	15	16
1,2	kHz/DIV	.02, .05 .1	0	0	1
3	"	"	1	0	0
1,2	"	.2 .5, 1	0	1	0
3	"	"	1	0	0
ANY	"	2, 5, 10	1	0	0
"	MHz/DIV	.02, .05, .1	0	0	1
"	"	.2, .5, 1	0	1	0
"	"	2, 5, 10	1	0	0

If satisfactory, go to (3). If not, proceed as below.

(2) Verify the table below :-

Filter	Range	Horiz. scale	AG4 pins 5	4	6	8	13
ANY	ANY	.02, .05, .1	0	0	1	-	-
"	"	.2, .5, 1	0	1	0	-	-
"	"	2, 5, 10	1	0	0	-	-
"	kHz/DIV	ANY	-	-	-	0	-
"	MHz/DIV	"	-	-	-	1	-
1,2	ANY	"	-	-	-	-	0
3	"	"	-	-	-	-	1

If satisfactory, examine the appropriate gates on AF1 and the RANGE, SCALE and FILTER switches; if not, examine AG4 IC8 and IC9.

(3) Connect TP8 to 0 V. Check that the waveform on TP5 is :-

(i) 500 Hz square wave with kHz/DIV selected
(ii) 500 kHz +ve pulses of 1:4 mark/space ratio with MHz/DIV selected.

If not, check IC10a,b,c and TR1.

(4) With TP8 still at 0 V, select MHz/DIV and check waveforms :-

(i) TP6 : 50 kHz +ve pulses of 1:4 mark/space ratio
(ii) TP7 : 5 kHz +ve pulses of 1:4 mark/space ratio
(iii) TP8 : 500 Hz +ve pulses of 1:4 mark/space ratio

If not, check IC5, IC6, IC7 and IC11a,b,c as appropriate.

(5) With TP8 still at 0 V and still on MHz/DIV, check waveforms at TP10 :-

(i) 50 kHz +ve pulses 1:4 mark/space ratio with HORIZ SCALE at 10
(ii) 5 kHz +ve pulses 1:4 mark/space ratio with HORIZ SCALE at 1
(iii) 500 Hz +ve pulses 1:4 mark/space ratio with HORIZ SCALE at 0.1

If not, check IC11.

(6) With TP8 still at 0 V and still on MHz/DIV, select HORIZ SCALE 10. Check that the waveform on AG4 pin 7 is a 25 kHz square wave.

If not, check IC1b and check that AG4 pin 7 is not held externally.

If the waveform is correct, then the reset circuit consisting of IC10d, IC7, IC6, IC5 and IC1a is faulty.

5.7.9 Tracking generator AC1 and AC2

Circuit diagram—Fig. 7.7

(1) If the tracking generator output level is only a few dB low (say, 10 dB max.), try peaking AC1 L1,3 and 5.

(2) Check that the signal level on the 'X' port AZ1 mixer is -20 dBm (63 mV p-p) at 36.4 MHz. Check that the frequency is stable and has the correct absolute value to within 50 Hz.

(3) Check that the signal level on the 'L' port of AZ1 mixer is -20 dBm at 200.2 MHz. This signal level is produced by the combination of the 6 dB mixer conversion loss and the 1:2 step-up transformer in the signal path. If this level is low, check the level of the local oscillator drive at the 'R' port. This should be $\geq$ +7 dBm at 236.6 MHz. If this level is low, check the buffer amplifier on AA7.

(4) Check that the signal level on the 'L' port of AZ2 is not less than -24 dBm. If the level is low, check through the 200.2 MHz i.f. amplifier for the following approximate levels:-

L1 tap : -15 dBm
L3 tap : -10 dBm
L5 tap : - 6 dBm

(5) Turn the 0-110 MHz REFERENCE FREQUENCY control fully counter-clockwise. Check the local oscillator drive on the 'R' port of the AZ2 mixer for a level of $\geq$+9 dBm at about 200 MHz. If the level is low, check through the AC1 TR5 buffer stage to the input coaxial lead for a level of $\geq$+5 dBm. If this level is low, check the buffer amplifier on AA5.

(6) Check the signal level at the 'X' port of the AZ2 mixer. It should be -30 dBm (20 mV p-p) at a frequency of 0-5 MHz with the controls as set in (5).

(7) Check that the output of the low pass filter (R1 on AC2) is at the same -30 dBm level.

(8) Finally, with the front panel TRACKING GENERATOR OUTPUT socket terminated in 50 Ω, check that the signal on AC2a pin 2 is -10 dBm and that on AC2a pin 5 is -4 dBm.

5.7.10 Scanning and e.h.t.—AM1, AM2, AM3 and AL1

Circuit diagrams—Figs. 7.32 and 7.34

Line scan and e.h.t.

If no e.h.t. or line scan is suspected, check the signal at AM2 TP4. It should be a positive going pulse of about 400 V peak, 10:1 mark/space ratio with a period of 51.2μs. If it is absent, check AM2 TR1, 2 and 3 and associated circuitry

Also check the scan coils for a line coil short. If the pulse is present at TP4, check the d.c. level on TP5 using a high resistance voltmeter. It should be at least +300 V. If this is present and there is still no display, check the difference potential between pin 7 and pin 2 of the c.r.t. base. If pin 7 is more than +10 V above the potential of pin 2, adjust R30 on AM3 so that it is reduced to this value.

If the raster is still not visible, there must be no e.h.t. or a tube fault, e.g. heater open-circuit etc. Remove the red cover of the e.h.t. unit and hinge out AL1 board after removing the two fixing nuts. Measure the d.c. level on the positive end of C4. This should be within the limits stated, i.e. +19 V to +28 V.

If the voltage is correct, check the waveform at the collector of AL0 TR2. It should be a positive going pulse of approx. 100 V peak. If it is not, check the drive to AL1 TR2 base, TR2 itself, T1 and D2 and C6. If it is, and no e.h.t. is present, replace AL0 VM1.

Field scan

If no field scan is present, check that the field drive waveform enters AM3 on pin 6. Check that there is an S-shaped saw-tooth of about 10 V peak-to-peak on TP2. If this is correct, check that the mean level of the emitter of AM3 TR7 is about 2.5 V. If not check TR4, 5, 6 and 7 and associated circuitry.

5.8 REALIGNMENT

This section contains information for the overall realignment of the instrument. All presets used are readily accessible; those inside internal covers are accessible through holes marked with the preset's circuit reference number.

Note Before any adjustments are made, all screening covers, with the exception of the one covering AA1 to AA4, must be fitted with at least half of their screws.

After completing repairs under Section 5.7, it may be necessary to realign affected circuits. Any adjustments additional to those detailed in this section should be carried out only after consulting Chapter 3, and the circuit diagrams in Chapter 7.

If the full overall realignment procedure is not required, individual steps may be performed providing they do not interact with other adjustments. It is recommended that the effects of any readjustment are considered with reference to the circuit diagrams.

5.8.1 Test equipment required

This section provides a list of test equipment required to carry out the overall realignment of the instrument.

Item	Description
a	Signal generator, e.g. mi TF 2002B.
b	RF attenuator, e.g. mi TF 2163.
c	Digital Multimeter, e.g. mi TF 2671.
d	Sensitive voltmeter (standardized at -10 dBm into 50 Ω at 10 MHz), e.g. mi TF 2600A.

5.8.2 Calibrator and tracking generator levels

Test equipment : items a, b, d

Set the controls as follows :

VERTICAL SCALE RANGE	- 1 dB/DIV
VERTICAL SCALE	- -10 dBm
HORIZONTAL SCALE	- 0.02 MHz/DIV
FILTER BANDWIDTH	- WIDE '3'
SWEEP MODE	- AUTO
STORE	- REFRESH 'A'
DISPLAY	- 'A'
COUNTER FREQUENCY	- PAST CENTRE
REFERENCE FREQUENCY	- CENTRE

(a) Tune to 10 MHz using the REFERENCE FREQUENCY controls.

(b) Set the signal generator to 10 MHz and its output level, using the voltmeter, to -10 dBm into 50 Ω (terminate the voltmeter input at 50 Ω).

(c) Connect the output of the signal generator to INPUT 50 Ω via the attenuator (item b). Adjust the attenuator until the displayed 10 MHz signal is 1 to 2 major divisions down from the top of the screen.

(d) Switch SWEEP MODE to MANUAL and the COUNTER FREQUENCY to BRIGHT LINE. Slowly rotate the BRIGHT LINE POSITION control, and trace a manual scan. Switch STORE to REFRESH 'B'and press DISPLAY'B' button.

(e) Remove the attenuator lead from the signal generator, and connect it to the STANDARD 10 MHz OUTPUT. Maintain the attenuator setting as in (c) above for this and subsequent tests in this section, and also section 5.8.3.

(f) Slowly rotate the BRIGHT LINE POSITION control and trace a manual scan. Position the bright line on the peak of this signal, and adjust R30 on AB4 until this level is the same as that of the reference signal on trace A. This sets the STANDARD 10 MHz OUTPUT amplitude. Trace out the scan to check that R30 is set accurately.

(g) Re-connect the attenuator input to TRACKING GENERATOR OUTPUT, and maintain the attenuator level as in (c) above.

(h) Adjust R23 on AB1 so that the bright line level is at the same level as the reference signal on trace A. This sets the TRACKING GENERATOR OUTPUT level. Trace a manual scan to check that R23 is accurately set.

5.8.3 Filter gain balancing

Test equipment : items a, b, d.

Set controls and equipment as for check 5.8.2(g).

(a) Rotate the BRIGHT LINE POSITION control to produce a trace over, for example, ±2 divisions around the centre. Switch to STORE 'A'and AUTO SWEEP MODE. The new trace will be approximately 0.4 dB higher than the stored B trace, due to noise. Adjust the VERTICAL SHIFT to align a major graticule line with the mid-point of the two traces. This is to be the reference level for the remainder of the filters. The stored B trace may be left on as a reminder of which major graticule line is being used, or alternatively, the STORE control can be returned to HIGH DEFN.

(b) Switch the HORIZONTAL SCALE to 0.1 MHz/DIV, the FILTER BANDWIDTH to NORMAL '2', and the SWEEP MODE to MANUAL. Use the BRIGHT LINE POSITION control to indicate a portion of sweep. Note this level with respect to the reference graticule line as defined in (a). Re-connect the attenuator to STANDARD 10 MHz OUTPUT, and use the same attenuation level at in check 5.8.2(c). Tune in and note the signal level. Switch COUNTER FREQUENCY to PAST CENTRE, HORIZONTAL SCALE to 2 kHz/DIV and FILTER BANDWIDTH to WIDE '3'. Tune to 10 MHz using the REFERENCE FREQUENCY controls and COUNTER READOUT, and note signal level. Adjust R31 on AC8 to centre these three levels around the reference graticule line. This sets the 5 kHz filter gain.

(c) Switch the HORIZONTAL SCALE to 1 kHz/DIV, and the FILTER BANDWIDTH to WIDE '3'. Note the signal level. Switch the HORIZONTAL SCALE to 0.2 kHz/DIV. Re-connect the attenuator input to TRACKING GENERATOR OUTPUT. Switch SWEEP MODE to MANUAL, and indicate a portion of the sweep using the BRIGHT LINE POSITION control. Set the 500 Hz filter gain by adjusting R12 on AC8 to centre the three levels around the reference graticule level.

(d) Switch the HORIZONTAL SCALE to 0.02 kHz/DIV, and indicate a portion of the manual scan using the BRIGHT LINE POSITION control. Note this level. Re-connect the attenuator input to the STANDARD 10 MHz OUTPUT, and switch SWEEP MODE to AUTO. Re-centre the displayed signal with the REFERENCE FREQUENCY controls, if necessary. Note the signal level. Set the 50 Hz filter gain by adjusting R27 on AC4 to centre the above two values around the reference graticule.

(e) Set the FILTER BANDWIDTH to NORMAL '2', and add READ IN B/U to identify the read-in point. Note this signal level. Connect the attenuator input to TRACKING GENERATOR OUTPUT, and switch SWEEP MODE to MANUAL. Indicate a portion of the manual sweep using the BRIGHT LINE POSITION control, and note its level. Set the 5 Hz filter gain by adjusting R29 on AC3 to centre the above two values around the reference graticule.

Note If these two values vary one from the other by more than 0.5 dB, suspect the frequency accuracy of the tracking generator.

5.8.4 Front panel gain control setting

(a) Switch the HORIZONTAL SCALE to 1 kHz/DIV, FILTER BANDWIDTH to WIDE '3', SWEEP MODE to AUTO, and the READ IN B/U OFF. Remove the attenuator from circuit, and directly connect the TRACKING GENERATOR OUTPUT to INPUT 50 Ω. Turn the VERTICAL DISPLAY GAIN preset fully counter-clockwise, and set the VERTICAL SCALE buttons to give a sensitivity of -10 dBm at the top of the screen. Set the 36.4 MHz i.f. amplifier gain by adjusting R12 on AB8 to give a display 3 dB down from the top of the screen.

(b) Using the VERTICAL SCALE buttons, select 0 dBm at the top of the screen, and ensure that the VERTICAL DISPLAY GAIN preset, when turned fully clockwise, will move the displayed image 7 dB up from the bottom of the screen. If not, readjust R12 on AB8 for a minimum of 5 dB increase and 2 dB decrease of gain around the calibrated level.

Note If R12 on AB8 cannot be set, covers should be removed and individual i.f. amplifier gains checked.

5.8.5 Sweep generator voltage levels

Test equipment : item c.

Set the controls as follows :

HORIZONTAL SCALE	- 10 MHz/DIV
FILTER BANDWIDTH	- NORMAL '2'
BRIGHT LINE POSITION	- fully counter-clockwise

(a) Remove board AG1. Connect the d.m.m. (switched to the 10 V range) to pin 14 of AE4.

(b) Press the SWEEP MODE, MANUAL then SINGLE, then START buttons, and hold pressed. Adjust R49 on AE4 until the d.m.m. indicates zero.

(c) Release the START button and adjust R38 on AE4 until the d.m.m. indicates 5 V.

(d) Because of interaction between these two adjustments, repeat (b) and (c) until no further improvement results.

(e) Replace board AG1.

5.8.6 Bright line tracking adjustments

Set the controls as follows :

VERTICAL SCALE RANGE	- 10 dB/DIV
VERTICAL SCALE	- -10 dBm
HORIZONTAL SCALE	- 10 MHz
FILTER BANDWIDTH	- WIDE '3'
COUNTER FREQUENCY	- BRIGHT LINE
SWEEP MODE	- AUTO
STORE	- HIGH DEFN

(a) Fit Extender Board 44827-235 to AE6.

(b) Using the REFERENCE FREQUENCY controls, position the d.c. marker approximately on the left-hand dashed graticule line. Connect the STANDARD 10 MHz OUTPUT to INPUT 50 Ω (using 50 Ω coaxial cable). Switch SWEEP MODE to SINGLE and dim out the graticule. Adjust the BRIGHT LINE POSITION control to achieve a COUNTER READOUT of zero. Adjust R22 on AE6 so that the bright line cursor is coincident with the d.c. marker.

(c) Adjust the BRIGHT LINE POSITION control to achieve a COUNTER READOUT of 100.0. Set R20 on AE6 so that the bright line cursor is coincident with the 10th harmonic of the calibration signal. If the adjustment of R20 has been more than 1% of f.s.d., recheck the setting of R22.

(d) Refit board AE6.

Index to Units

Unit designation	Description	Parts list page	Circuit diagram Fig.
A01	Front panel (part 1)	181	Fig. 7.1
	Upper front panel (part 2)	-	Fig. 7.2
A02	Lower control panel	181	Fig. 7.3
AA0a	AA tray	182	Fig. 7.4
AA0b	AA tray	182	Fig. 7.4
AA1	Sweep shaper and local regulator	119	Fig. 7.10
AA2	Frequency divider and pulse generator	122	Fig. 7.11
AA3	4.8 MHz interpolating oscillator assembly	123	Fig. 7.12
AA3a	4.8 MHz interpolating oscillator board	123	Fig. 7.12
AA3b	4.8 MHz interpolating oscillator board	125	Fig. 7.12
AA4	3.6 MHz master second local oscillator assembly	126	Fig. 7.11
AA4a	3.6 MHz master second local oscillator board	126	Fig. 7.11
AA4b	3.6 MHz master second local oscillator board	127	Fig. 7.11
AA5	200 to 310 MHz slave first local oscillator unit	127	Fig. 7.13
AA5a	200 to 310 MHz master first local oscillator board	129	Fig. 7.13
AA6	205 to 315 MHz master first local oscillator unit	130	Fig. 7.14
AA6a	205 to 315 MHz master first local oscillator board	132	Fig. 7.14
AA6b	205 to 315 MHz master first local oscillator board	133	Fig. 7.14
AA7	236 MHz slave second local oscillator unit	133	Fig. 7.15
AA7a	236 MHz slave second local oscillator board	135	Fig. 7.15
AB0a	AB tray	182	Fig. 7.5
AB0b	AB tray	182	Fig. 7.5
AB1	36.4 MHz crystal oscillator	136	Fig. 7.9
AB2	Fixed oscillator divider chain	137	Fig. 7.9
AB3	80 MHz crystal oscillator	138	Fig. 7.9
AB4	10 MHz reference crystal oscillator	140	Fig. 7.9
AB5	Line cleaners	141	Fig. 7.5
AB6	400 kHz i.f. signal amplifier	142	Fig. 7.8
AB7	3.6 MHz i.f. signal amplifier	143	Fig. 7.8
AB8	36.4 MHz i.f. signal amplifier	144	Fig. 7.8
AB9	200.2 MHz i.f. signal amplifier	145	Fig. 7.7
AB10	30 Hz to 110 MHz input signal amplifier unit	146	Fig. 7.7
AB10a	30 Hz to 110 MHz input signal amplifier board	147	Fig. 7.7
AB10b	30 Hz to 110 MHz input signal amplifier board	147	Fig. 7.7
AC0a	AC tray		Fig. 7.6

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