NASA Electronic Parts and Packaging (NEPP) Program

NEPP Task:

Effect of Manual-Soldering-Induced Stresses on Ceramic Capacitors

(Part I)

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1. Introduction.

Cracking in ceramic capacitors is an old problem; it appeared in the 1970s when the first surface mount technology (SMT) chip capacitors were introduced to the market and began to be employed in NASA applications [1, 2]. According to J. Maxwell [3], one of the most experienced specialists in manufacturing of ceramic capacitors, this problem will continue to be with us in the foreseeable future. Two main factors contribute to the problem: brittleness of the ceramic materials, and thermal and mechanical stresses associated with the SMT assembly process. Both factors are intrinsic to chip ceramic capacitors and explain the persistence of the problem. Based on the analysis by the Center for Advanced Life Cycle Engineering (CALCE) of over 150 electronic product failures over a 4-year period, capacitors are responsible for a larger proportion of failures than any other component [4].

1.1. Factors affecting cracking.

Factors affecting the propensity of multilayer ceramic capacitors (MLCCs) to cracking can be divided into two categories: internal and external. Internal factors are related to the property of materials used, presence of internal defects, and the size of capacitors. Fracture toughness characterized by the critical-stress intensity factor K1C, thermal diffusivity, and Young's modulus are among the most important characteristics of ceramic materials affecting the thermal shock behavior of MLCCs [5]. Generally, the mechanical stability of capacitors and fracture toughness increase in a row: NPO > X7R > Z5U, Y5V [4, 6]. Multiple studies and manufacturers' guidelines indicate that the larger the size of capacitor, the greater the probability of cracking either due to soldering stresses or to handling after assembly [4, 5, 7-10].

External factors are related mostly to the thermal and mechanical stresses caused by the soldering process and post-soldering handling of the board. However, cracking in ceramic capacitors can occur at any step during the lifespan of the parts, starting from manufacturing and continuing through assembly and applications [11-14]. Note that the compressive strength of ceramic materials significantly exceeds their tensile strength, by five to 13 times according to the data presented in [15]. Considering that coefficients of thermal expansion (CTEs) of printed wiring boards (PWBs) are larger than those of ceramic capacitors, soldering of MLCCs onto polymer boards results in development of compressive stresses. Typically, these stresses do not cause fractures in the parts; however, bending of the board might cause tensile stresses sufficient for cracking.

A brief description of different causes of cracking is given below. In some cases the appearance of the crack can indicate its origin [11].

I Manufacturing.

- I.1 Rapid cooling of the laminates can cause so-called firing cracks that typically propagate perpendicular to the plane at the terminals.
- I.2 Insufficient binding strength and/or the presence of foreign materials might result in knit-line cracks that typically extend parallel to the electrodes.
- I.3 Oxidation of palladium electrodes in air is accompanied with volume expansion and might cause cracks and delaminations [16]. It is assumed that thermal cracks might initiate at internal flaws such as voids and delaminations, and the larger the delamination the greater the probability of thermal shock failures.

II Assembly.

II.1 Pick-and-place machines can damage parts by excessive stresses created by centering jaws or vacuum picks.

II.2 Thermal shock cracks are due to a sharp temperature increase during soldering; they originate at the surface and propagate to the interior at angles of ~45^{o}. Thermal shock stresses might form large, visible U-shaped cracks on the surface of capacitors.

II.3 Thermal shock cracks might also occur when liquid cleaners are applied to a board that has not sufficiently cooled after soldering reflow. To prevent this type of cracking the boards should be cooled slowly, preferably by natural cooling, or at a rate not exceeding 2 ^{o}C to 3 ^{o}C/sec., to temperatures below 60 ^{o}C.

II.4 Tensile stresses and cracking might develop in MLCCs after soldering them onto alumina boards. This is due to the differences in CTEs between the ceramic material and substrate, with the latter having lower CTEs. These stresses are responsible for many observed failures in ceramic chip capacitors mounted on alumina substrates [1].

III Board-level handling.

Due to the lack of stress relief in mounted chip capacitors, deformation and flexing of the PWB might create significant tensile stresses resulting in so-called flex cracking. These cracks mostly originate at the bottom surface near the edge of the termination margin and propagate inside at angles close to 45^{o} (or 60^{o} to 65^{o} per [9]). Typical sources of the flex cracking are de-paneling, test probing, screw or standoff attachments, handling during visual examinations, insertion of connectors, board-to-board vertical connections, etc.

IV Application.

IV.1 Deformation of the board caused by temperature cycling, vibration, or mechanical shocks that occur during applications might cause flexing of the board sufficient for cracking of MLCCs. Multiple guidelines for design and board layout have been developed to reduce the probability of this type of failure [3].

IV.2 Due to electrostriction in ceramic materials, voltage cycling might create mechanical stresses that would further develop preexisting microcracks, resulting in failure. This mechanism might be especially important for high-voltage ceramic capacitors [17, 18].

Board flexing and soldering-induced thermal shocks are considered major reasons of cracking in MLCCs. A breakdown of about 40 different mechanical failures of capacitors that were analyzed by CALCE shows that 25% were caused by flex cracking, 23% by thermal shock cracking, and 34% were due to manufacturing defects [4, 14].

Various designs of MLCCs have been suggested by manufacturers to decrease the probability of flex cracking [9, 19]. Most of these solutions simply involve removing the deleterious effects caused by flex cracking even though the parts are still cracking:

- Flexible termination. The application of relatively soft and/or tear-away termination layers made of conductive polymers reduces the stress in ceramic and restricts flex cracks within a safe zone away from the body of the MLCC.
- Fail open design. In this design, the end margins are widened, so if a crack occurs, it does not cross electrodes with opposite polarity, and thus prevents short-circuit failures.

- Floating electrodes. This design creates two separate capacitors in series within an individual case size, so the probability of shorting cracks is reduced substantially.
- Clip-on lead frame. Attachment of J-shaped leads mechanically decouples the MLCC from the PWB and allows for stress relief. A layer of solder resist at the bottom of the MLCC prevents solder from wicking and causing short circuits.

Because industry is now using lead-free solders, concerns regarding thermal shock cracking have increased substantially. Also, the lead-free solders are stiffer and have a higher yield stress, so changing eutectic solder to either Sn3.5Ag or Sn4.0Ag0.5Cu might lead to increased flex cracking of the capacitors [20]. However, experiments showed that the probability of flex cracking in capacitors assembled with high-temperature Pb-free solders is lesser compared to those assembled with Sn/Pb eutectic solder [4]. Cooling of assemblies after high-temperature soldering places capacitors under greater compressive stresses, and respectively more bending is necessary to create tensile stresses and cracks in the part.

Standardized test methods have been developed to assess the susceptibility of MLCCs to cracking due to board flexing and to thermal shocks. The first is performed using so-called flex-testing that is typically performed per EIAJ Specification RC-3402, Multilayer Ceramic Capacitors (Chip-type). According to these tests, the part is soldered onto a PWB made with standard material and of a standard size, and is deflected with the component face-down to the required level, while its capacitance is monitored. A decrease in capacitance below the acceptable limit (typically 0.2% or 2% [9]) is used to characterize the robustness of a capacitor to board flexing. By creating sufficiently large deflection of the board, cracking can be achieved in most cases. This makes this testing convenient and effective for analysis of factors affecting failures in capacitors related to board handling. Note that similar testing is also standardized by the automotive industry (AEC Q-200, Stress Test Qualification for Passive Components) to assure reliability of MLCCs after assembly, and it would be reasonable to include a similar standard in MIL-PRF-123 also.

The thermal shock test or so-called solder-dip testing is described in MIL-STD-202. According to this method that in MIL-PRF-123 is referred to as the resistance-to-soldering-heat test, MLCCs are immersed two times into molten solder at a temperature of +230 °C for 5 seconds. However, most capacitors are passing the standard solder-dip test without failures, and likely for this reason many manufacturers are using more stringent test conditions by increasing the temperature during this test to 260 °C. Even higher temperatures might be needed to characterize the lead-free capacitors.

A simplified model of thermal-shock-induced stresses in MLCCs predicts that the stress increases proportionally to the elastic modulus, the coefficient of thermal expansion of ceramic, and the square of the thickness of the part [5]. Based on this model, thermal shock behavior of capacitors can be dramatically improved by utilizing thinner geometries of capacitors. However, experiments showed that the thermal shock resistance is inversely proportional to the total area of the ceramic surface, rather than to its thickness [8]. This was explained by the effect of preexisting flaws on the surface of ceramic capacitors that dominate the crack initiation process, and are therefore primarily responsible for the thermal shock resistance of MLCCs.

1.2. Effect of cracks on performance of capacitors.

The presence of cracks might not affect capacitance and dissipation factors of the part substantially [9, 10], but can cause avalanche breakdown failures [21] or increase leakage currents [10, 11, 22]. The majority of field failures of MLCCs are caused by low insulation resistance that is often due to cracks. In low-impedance applications, a decrease in resistance might cause catastrophic failures. Although cracks in ceramic capacitors might not lead to immediate failures, they create defects that would cause degradation with time (hours to months) resulting eventually in field failures. In this regard, microcracks generated during assembly can be considered as a "time bomb" [11] that causes increased leakage currents, opens, or intermittent contacts as cracks propagate with time during application.

Cracks in ceramic capacitors might cause life test failures. Acceleration testing of various lots of commercial ceramic capacitors was performed in [23]. Some correlation between the life test results and the presence of delaminations in MLCCs was observed.

Increased leakage currents in MLCCs having cracks might be due to various mechanisms. A virgin surface of the crack might have increased electron conductivity due to the presence of a high concentration of surface traps; however, this conductivity is not great enough to cause failures and likely will not increase with time. A substantial increase in leakage current occurs when a conductive media fills the crack. This is possible either by moisture condensation, when the part is exposed to humid environments, and/or by formation of metal dendrites, when dry or wet electromigration of electrode metal occurs in the crack. In both cases the presence of ionic contaminations substantially enhances the degradation process.

Moisture can penetrate inside the capacitor along a crack if it is initiated from the surface, or along the micropores. It is also possible that moisture can enter the part though the porous termination and electrode interfaces [24]. Note that due to a capillary effect, as well as polarity and affinity of ceramics to water molecules, the condensation can develop with time even at relatively low-humidity environments.

Silver was initially used as a metal of choice for electrodes in MLCCs. However, this metal has a high propensity for electromigration in humid and even in dry environments. In the absence of moisture, silver can migrate through glasses at relatively high temperatures (more than 150 ^{o}C) by a field-induced diffusion mechanism [25]. This behavior is likely unique for silver, but in the presence of moisture a variety of metals, including gold, palladium, and nickel, are susceptible to migration and might form shorting dendrites. It is assumed that the replacement of silver with Pd/Ag alloys or nickel in contemporary capacitors somewhat inhibited electromigration. However, electromigration in humid environments is still possible, and for this reason biased high-humidity/high-temperature testing is still considered an effective technique to inspect capacitors for dielectric cracks [21].

Excessive degradation of the parts with microcracks in humid environments might be related to so-called low-voltage failures in ceramic capacitors [2, 26]. Although the occurrence of this type of failure is substantially decreased, and most manufacturers believe that their parts are now impervious to this effect [27], there are some indications that this effect is still present [21]. Recent results on biased MLCCs at 85 ^{o}C/85% RH reported by CALCE showed that intermittent failures do happen, but they are more likely to occur at higher voltages [28]. More study is necessary to assess the probability of failures of contemporary ceramic capacitors in humid environments and to understand the effect of electrode materials and voltage acceleration factors.

1.3. Techniques for revealing cracks.

According to Tarr [13], the cracks might be visible in less than 2% of affected parts, so only a small minority can be identified as potential failures before use. This requires development of more effective methods to reveal cracks in MLCCs. A variety of techniques have been suggested for screening of capacitors during mass production, during post-soldering examinations, or for investigation purposes. A brief description of these techniques is given below.

- Visual inspection. This is the most simple and inexpensive test, but unfortunately it is not very effective due to the insidious character of most cracks in MLCCs. Nevertheless, thorough optical examination is necessary as a screening procedure. The effectiveness of this test can be increased substantially by application of the vicinal examination technique [29, 30].
- X-ray radiography. Radiography has a low success rate in revealing cracks [13, 31]. X-ray microcomputer tomography might be more effective, but it is not suitable for large-scale screening [32]. Also, termination layers with high absorption (e.g., solder) may shield the minor changes in X-ray intensity resulting from the crack.
- Acoustic microscopy. This technique was proven to be effective in some cases, and scanning laser acoustic microscopy (SLAM) testing was implemented as a screen for incoming capacitors [12]. Acoustic microscopy can successfully reveal large voids and delaminations, but it is much less successful on cracks, especially those propagating at 45^{o} or more [31]. Also, ultrasonic systems have difficulties penetrating through the multiple layers of the device under the curved surface of the termination. Most of the defects detected by acoustic microscopy have been caused by delaminations or cracks that occur before attachment, and in the center section of the capacitor.
- Laser ultrasonic and interferometric measurement. According to this technique, a pulsed infrared laser excites a specimen into vibration through laser-generated ultrasound, and the vibration displacement is measured using an interferometer [31]. Although this method is able to detect cracks, further testing and refinements are required to account for the process-induced manufacturing variations in different part sizes.
- Electrical measurements. Measurements of insulation resistance (IR) are considered more sensitive to the presence of cracks compared to measurements of capacitance and the dissipation factor. According to Tarr [13], IR measurements can reveal approximately 60% of damaged capacitors, and this technique is considered as having a medium success rate [31]. The effectiveness of capacitance measurements can be increased substantially if the part is mechanically loaded during the test. This was achieved in [32] by exploiting the thermal mismatch between the capacitor and the organic board. During these measurements, the part was heated up so that the capacitor experienced a tensile force, thus causing opening of the existing cracks. The crack openings manifested themselves as a capacitance decrease in discrete steps over temperature. However, ceramic capacitors have pronounced temperature dependence of capacitance that might mask the presence of cracks and overlay the decay in capacitance caused by cracking.
- Environmental testing. The presence of microcracks can be detected if a conductive liquid fills the crack, thus substantially increasing leakage current in the capacitor. Water is

obviously a suitable liquid, and direct quenching of preheated capacitors in ice water has been successfully used to reveal cracks in MLCCs [8]. A standard 85 ^{o}C/85% RH test has been widely used to evaluate reliability of ceramic capacitors. However, conductivity of water might be not sufficiently high, and likely for this reason no failures in parts after solder-dip test were revealed by this technique in [5], whereas 1 hour of boiling the parts in 1.3 N NaCl solution resulted in IR failures.

- Methanol test. Methanol is a conductive, low-viscosity liquid with a perfect capillary action for allowing penetration into tiny cracks in ceramics. This test has been extensively used for revealing cracks in MLCCs. However, several other factors may also lower the insulation resistance, thus obscuring the effect of cracks. These factors include contaminated cleaning solvents or large amounts of dissolved flux residue [13].

1.4. Manual soldering.

Volumes of literature have been written over the years about cracks in ceramic capacitors, mechanisms of their formation, and factors affecting the probability of their occurrence. Based on the studies performed, substantial progress in the quality of materials and manufacturing processes has been made. This, together with development of detailed application guidelines, resulted in a significant decrease in cracking-related failures, and allowed for application of MLCCs in high-reliability systems including space instruments. Still, failures related to cracking in capacitors after assembly onto PWBs do occur, and further analysis is necessary. Several cases of crack-related failures in large ceramic capacitors were observed recently by the aerospace community [29]. In some cases, cracking was observed after manual soldering of MLCCs that is often used during assembly of cards for space projects.

Manual soldering of ceramic capacitors is known to have a high risk of causing cracks in the parts. The major reason for this is that hand-soldering does not allow for proper control over the process, and is subject to variability of individual operators and mistakes. Of particular concern are the variability of temperature, the possibility of overheating, touching the part with the soldering iron tip, and an excessive amount of applied solder [7, 33, 34]. The risk of cracking during hand-soldering is increasing with the size of capacitors, so J. Maxwell [3] plainly stated to “never use soldering irons” for parts with a case size of more than 1210.

All manufacturers are warning against manual soldering of MLCCs and provide detailed guidelines to reduce the risk of cracking in case rework or hand-soldering has to be used. These guidelines can be summarized as follows:

1. Direct contact by a soldering iron tip often causes thermal cracks, so the tip should be applied to the contact pad only. Use a soldering tip no greater than 0.120" [3.0 mm] in diameter (Vishay), and apply the transmission of heat through the soldering material so as not to allow the tip to make contact.
2. Preheat the chip capacitor to + 150 °C minimum. Use a hot plate or hot air flow for preheating.
3. Use the lowest tip temperature setting possible and a maximum soldering time of 5 seconds. The tip temperature should be less than 300 °C (280 °C maximum per Vishay guidelines, and 285 °C per ATC [33]). Note that according to MIL-STD-202 TM 210, condition A regarding use of a soldering iron, the testing should be performed at a much higher temperature of the soldering iron, 350 °C ±10 °C.

4. The wattage of the soldering iron should not exceed 30 W.
5. If lands are different, solder the smaller land first, and remove the tip quickly when the fillet is formed [33]. The fillet should have a concave profile and be at least 25% of the chip height.
6. Excess solder might cause mechanical stresses on components, thereby diminishing reliability. All thermal shock studies supported a moderate amount of solder, with excessive solder leading to a greater susceptibility to fault [7].
7. When removal of a chip capacitor is necessary, a hot air pencil is the preferred tool.
8. After soldering, allow the chip to cool at room ambient conditions. Using forced cool air or refrigerated air for expediting the cooling process is not recommended and can create thermal shock cracks.

1.5. Purpose of work.

Unfortunately, manual soldering has to be used sometimes for unique space assemblies or during rework. To estimate the risk associated with manual soldering, it is important to obtain a better understanding of the mechanism of soldering-induced cracking and factors affecting the probability of its occurrence. An obvious reason for the risk associated with manual soldering is poor reproducibility of the process and the possibility of operator mistakes. Still, it is not clear whether there are any intrinsic deficiencies in this process that would increase the probability of failures compared to solder reflow processes even when all the necessary precautions are used, and assembly is carried out according to the most stringent guidelines for manual soldering.

Possible factors causing increased cracking of MLCCs during manual soldering include the following:

1. Insufficient preheating resulting in thermal shock. Contrary to the chamber soldering that stresses the whole surface of the capacitor, during manual soldering the shock might be experienced mostly by the terminals.
2. Excessive solder resulting in increased stresses caused by the mismatch of CTE between solder and ceramic.
3. Specifics of the PWB deformation caused by local heating might result in local deflection of the board that would cause flex-like cracking upon cooling.
4. Heating of the ceramic to a higher temperature than the board that might cause formation of tensile stresses and cracking upon cooling.

Note that in the two last cases, the rate of cooling is likely a decisive factor affecting the probability of cracking because solder creeping allows for stress relaxation when the system slowly cools down from the melting temperature. These factors will be analyzed in next year's (2009) part of the work conducted on soldering-induced stresses in ceramic capacitors. In the 2008 part of the work reported below, effects of thermal shocks and thermomechanical stresses caused by excessive solder were studied using seven types of large-size MLCCs. The capacitors have been characterized mechanically by measurements of CTE, hardness, and fracture toughness. External visual examination, electrical characteristics, and methanol tests were used to evaluate the susceptibility of the parts to cracking under multiple thermal shock and thermal cycling conditions.

2. Experiment.

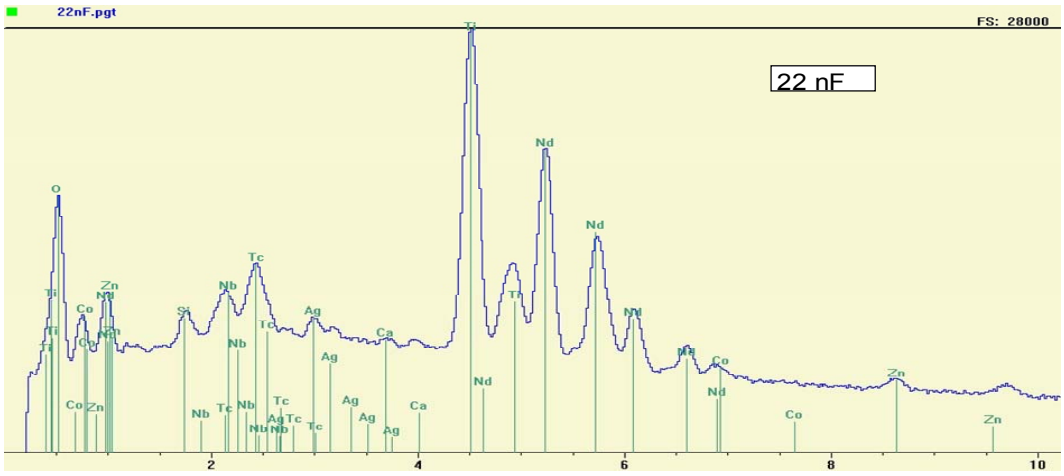
Seven types of large-size ceramic capacitors with sizes varying from 2220 to 2225 were used for this study. Table 1 displays vendors and characteristics of the part types used; W, L, and H indicate the width, length, and thickness of the parts. Six out of seven parts had high CV values and were made using X7R or X5R dielectrics (EIA class II) and one part, 22 nF 50 V, was made using a stable, temperature-compensating COG (or NPO) dielectric (EIA class I).

Table 1. Characteristics of MLCCs used.

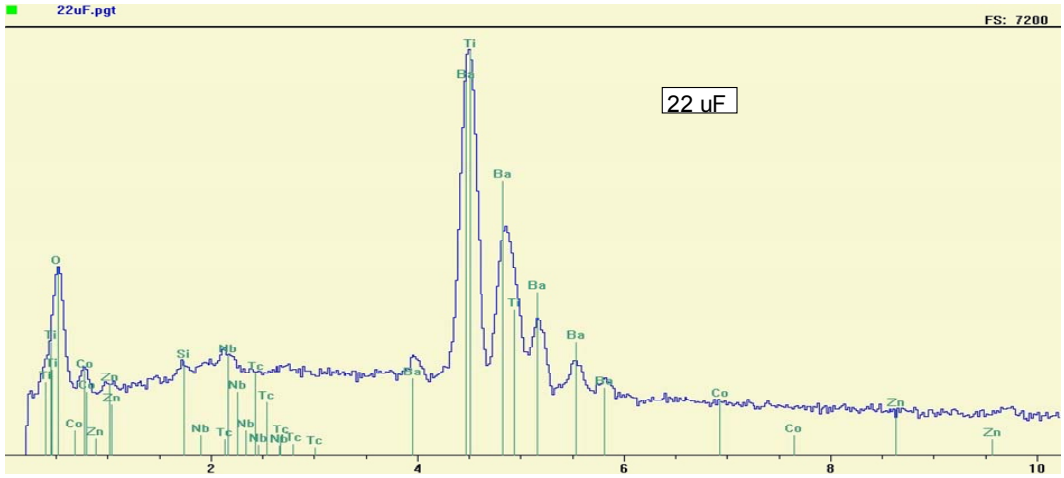
Part	C and V	Vendor	Mater.	Size	W, mm	L, mm	H, mm
GRM55RR71H105KA01L	1.0 µF, 50 V	Murata Electronics	X7R	2220	4.79	5.78	1.85
GRM55FR60J107KA01L	100 µF, 6.3 V	Murata Electronics	X5R	2220	4.82	5.79	3.21
C2225C225K5RACTU	2.2 µF, 50 V	Kemet	X7R	2225	6.22	5.49	1.27
C5750X7R1H106M	10 µF, 50 V	TDK Corp.	X7R	2220	4.95	5.61	2.21
C5750X5R1C476M	47 µF, 16 V	TDK Corp.	X5R	2220	5.36	5.9	2.37
N2223H223K5GAC	22 nF, 50 V	Kemet	NPO	2223	6.11	5.71	1.05
C5750X7R1E226M	22 µF, 25 V	TDK Corp.	X7R	2220	5.28	5.89	2.47

Energy dispersive spectroscopy (EDS) analysis showed that the major component in the 22 nF capacitors was neodymium titanium oxide ($Nd_2Ti_2O_7$), while most EIA class II capacitors were made of barium titanate ceramics (see Figure 1).

To estimate post-soldering thermomechanical stresses in capacitors, coefficients of thermal expansion were measured using a thermal mechanical analyzer, TMA2940, manufactured by TA Instruments. The measurements were carried out at a rate of 3 °C/min. during several cycles of heating and cooling from room temperature to 350 °C. The CTE values were calculated after the first cycle was completed to anneal the samples and eliminate possible errors related to the built-in mechanical stresses. Measurements of deformation were carried out in three directions, along (X and Y) and across (Z) the plates. These directions corresponded to the length, width, and thickness of the part. Prior to the measurements, metal terminals were ground off and polished to avoid errors related to the presence of metal layers and solder.



a)



b)

Figure 1. Results of X-ray microanalysis of 22 nF 50 V (a) and 22 µF 25 V (b) capacitors.

Hardness and fracture toughness of the ceramic materials were measured using Vickers microindention tests. Prior to the testing, the parts were molded in epoxy low-stress room-temperature cure compound, ground using sand papers up to #2400 grit, and polished using a 0.5 µm diamond paste. The indenter was attached to a Metek AccuForce III gauge, and the testing was carried out on three samples of each type of capacitor at four load levels: P = 2 N, 4 N, 6 N, and 10 N. From five to 12 indentions were made on the cover layers at each force, and the size of the impressions (indent prints) and the length of cracks were measured in each of the capacitors using a scanning electron microscope (SEM). Figure 2 shows molded capacitors after Vickers testing, and Figure 3 shows typical optical and SEM views of the indents and radial cracks emanating from the corners of the imprints. The sizes of each imprint and crack were measured using Photoshop software, and the respective average values were used for calculations of the hardness and fracture toughness of the parts.

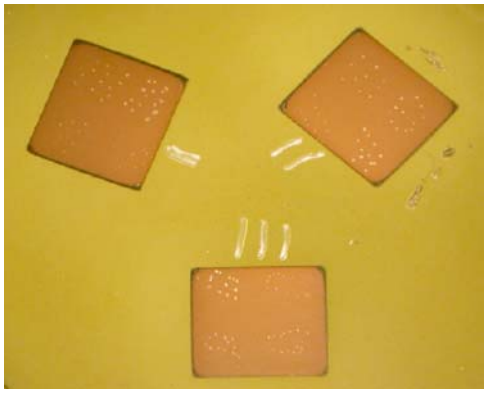


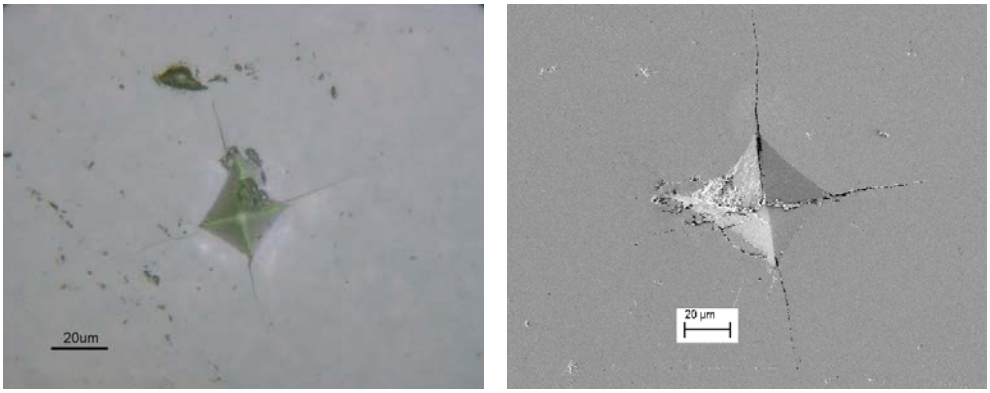
Figure 2. 22 µF 25 V capacitors after Vickers hardness testing. Dots indicate marks after indention testing made at different levels of the load.

The Vickers hardness (VH) and fracture toughness (K1C) were calculated based on the average diagonal size of the imprints, D:

$$VH = \frac{1.854 \times P}{D^2}, \quad (1)$$

$$K_{1c} = \varsigma \left[\frac{E}{H}\right]^{0.5} \left[\frac{P}{c^{1.5}}\right], \quad (2)$$

where E is the Young's modulus (~200 GPa [1, 35, 36]), c is the radial crack length measured from the center of the indent, and ζ is an empirically determined ''calibration'' constant usually taken equal to 0.0167 for Vickers indents.



(a) (b)

Figure 3. Typical optical (a) and SEM (b) views of imprints after Vickers indention testing.

It should be noted that measurements of the fracture toughness based on the Vickers indention testing have been criticized recently by Quinn and Bradt [37] because the results are not reliable and differ significantly compared to the standard fracture toughness tests. However, the Vickers indention fracture test allows in-situ evaluation of mechanical parameters directly on small

components, and ceramic capacitors in particular, and it is still widely used for analysis of mechanical behavior of MLCCs [35, 38] and of various high-brittleness materials [39-41].

To assess the probability of cracking, the parts were subjected to multiple thermal shocks and temperature cycles, and their characteristics, including capacitance (C), dissipation factor (DF), equivalent series resistance (ESR), and leakage current (DCL) were measured periodically through the testing. Although not specified for ceramic capacitors, ESR values were measured at 100 kHz to assess possible variations in the contact resistances of the parts.

To increase the sensitivity to cracking, DCL measurements were carried out at twice-rated voltages. Considering that per MIL-PRF-123 the minimum specified insulation resistance is determined as IR = 1E9*C, where C is in µF and IR is in Ohms, the maximum leakage current that is supposed to be measured after 2 minutes after voltage application can be calculated as DCL_{max} = 0.002*VR/C, where DCL is in µA, rated voltage (VR) is in volts, C is in µF.

Figure 4 shows typical examples of current relaxation with time for 20 samples in each part type. The results indicate that leakage currents decrease with time by one to two orders of magnitude, and they continue decreasing even after 1,000 seconds of electrification. To evaluate possible effect of cracking, the leakage currents were monitored for 1,000 seconds after voltage application to assure that no interruptions occurred, and the DCL reading for further analysis was taken after 1,000 seconds.

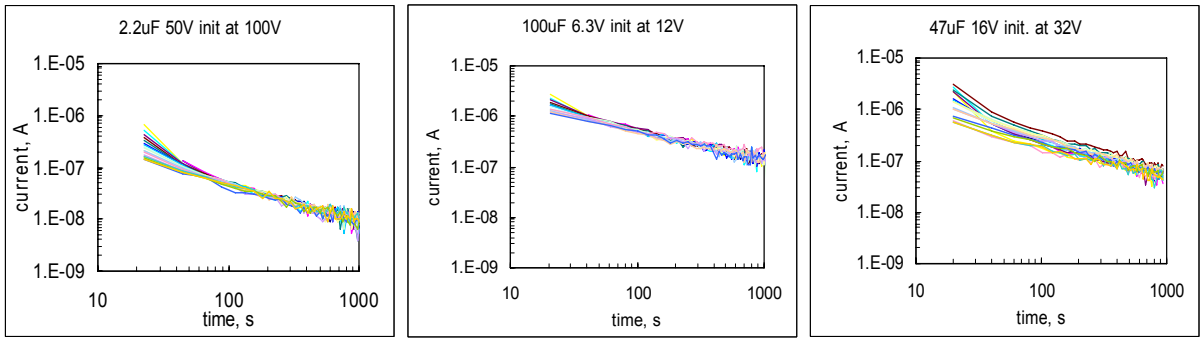
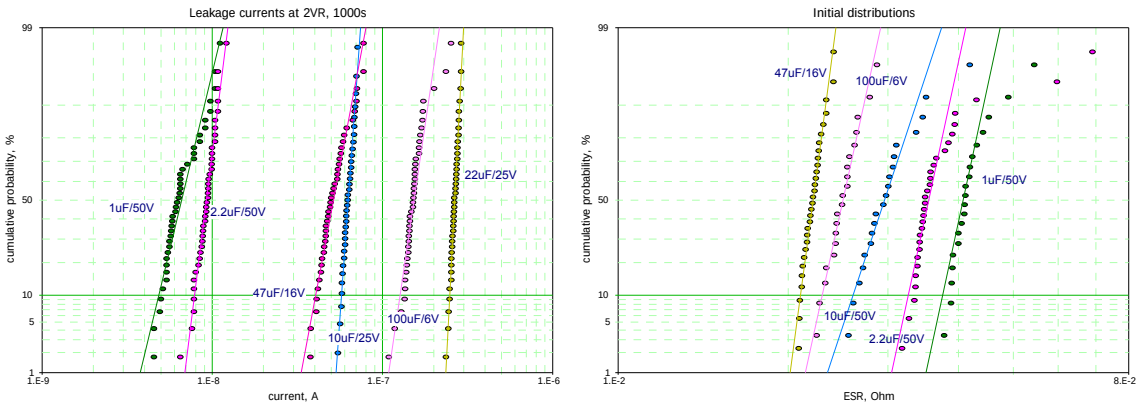


Figure 4. Current relaxation in three types of capacitors at twice-rated voltages.

Typical distributions of DCL and ESR values for six types of capacitors are shown in Figure 5. Note that for both parameters, DCL and ESR, the best fit was obtained using log-normal functions. Distributions of DCL values had relatively low standard deviations, varying from 0.05 to 0.18, indicating good reproducibility of the measurements. The leakage currents were five to 20 times below the specified limits, and the lots had no outliers. This increases the probability of revealing defects during testing of the parts by using DCL measurements.

ESR distributions in some lots had a relatively large spread, and one to three samples can be considered as ESR outliers in 10 µF 50 V, 2.2 µF 50 V, and 1 µF 50 V capacitors (see Figure 5.b).



a) b)

Figure 5. Log-normal distributions of leakage currents (a) and ESR (b) for different types of capacitors.

A methanol test was used to further increase the sensitivity of leakage current measurements to cracking [26]. During this testing, the parts were preheated to 85 ^{o}C for 15 minutes and then immersed into methanol at room temperature for 3 minutes. DCL measurements were repeated after methanol removal and drying the part for ~1 minute.

3. Mechanical characteristics of capacitors.

Results of measurements of CTE, hardness, and fracture toughness of the capacitors used in this study are described below.

3.1. Thermomechanical characteristics.

Figure 6 shows variations of deformation and calculated CTE values with temperature for six types of ceramic capacitors. Analysis of these data indicates a significant variation of the rate of deformation below and above the Curie temperature (Tc). These variations result in extreme temperature dependencies of CTE that for barium titanate, class II, ceramics has a minimum in the range from 120 ^{o}C to 130 ^{o}C, which correspond to Tc values for these capacitors.

Anomalous deformation of ceramic capacitors at temperatures close to Tc were also reported by He [42]. Similar behavior is known for perovskite oxides, and is due to changes of the crystalline lattice over the ferroelectric transition. Careful examination of the thermal expansion curves revealed that within the narrow temperature range of the ferroelectric transition, the thermal expansion becomes negative [42].

Results in Figure 6 show that at temperatures above Tc, T ~140 ^{o}C, CTE values calculated for the three directions are close and vary in the range from 10 to 12 ppm/K for different part types. As temperature increases from ~130 ^{o}C to 350 ^{o}C, CTE values are slightly increasing at a rate varying from 0.008 ppm/K^2 to 0.017 ppm/K^2.

Due to relatively minor variations with temperature, CTE values below (CTE1) and above (CTE2) Curie temperature were calculated as average values for these two regions. Results of these calculations based on measurements of deformations across (Z), along the length (X), and along the width (Y) of the parts are presented in Table 2. Average high-temperature CTE values

(in the range from 140 ^{o}C to 350 ^{o}C) are close, and for different types of capacitors vary from 12.1 ppm/^{o}C to 14.4 ppm/^{o}C. These data are similar to those typically reported for $BaTiO_3$ ceramics [1, 43]. At T < Tc CTE varies with temperature significantly, but on average remains much lower (from 3.1 ppm/^{o}C to 9.6 ppm/^{o}C) than for the high-temperature region. Based on He's data, low-temperature CTE values for different manufacturers of X7R capacitors vary for 5.5 ppm/^{o}C to 7 ppm/^{o}C, and the high-temperature data are in the range from 12 ppm/^{o}C to 14 ppm/^{o}C, which is in agreement with our results.

Table 2. CTE values (in ppm/^{o}C) calculated based on measurements along three directions for ceramic capacitors.

Capacitor	CTE_Z_1	CTE_Z_2	CTE_X_1	CTE_X_2	CTE_Y_1	CTE_Y_2
1.0 µF, 50 V	8.1	12.1	8.4	12.5	8.8	12.2
100 µF, 6.3 V	3.1	13.6	11.3	13	12.3	13.1
2.2 µF, 50 V	8.7	13.8	8.9	12.2	-	-
10 µF, 50 V	7.6	12.65	9	12.3	-	-
47 µF, 16 V	4.5	12.9	-	-	-	-
22 nF, 50 V	8.9	13.3	10.3	12.2	-	-
0.1 µF, 50 V	9.6	14.4	-	-	-	-
Average	8.6*	13.2	9.6	12.4	10.6	12.7

*Calculated without data for high-C capacitors (47 µF and 100 µF).

Figure 6 shows that in most cases the CTE values measured across the capacitors (Z direction) are slightly higher than CTE measured along the plates. This difference is more significant for 10 µF and 100 µF capacitors compared to 1 µF parts and might be related to the built-in mechanical stresses in MLCCs. It has been shown that due to the difference between CTE of ceramics and metal electrodes (Ni or Pd/Ag have greater CTE), there is a compressive in-plane stress in the active layers of the MLCC [44]. The residual stress increases with the number of dielectric layers, and changes electrical characteristics of capacitors depending on the direction of applied force [45]. It is possible that these stresses result also in anisotropy of deformation with temperature that is more pronounced for parts with high capacitance value. The effect is more obvious for large-value capacitors comprised of many layers of ceramic and electrode materials, and for this reason likely the anisotropy of CTE was not observed in other studies [1, 42].

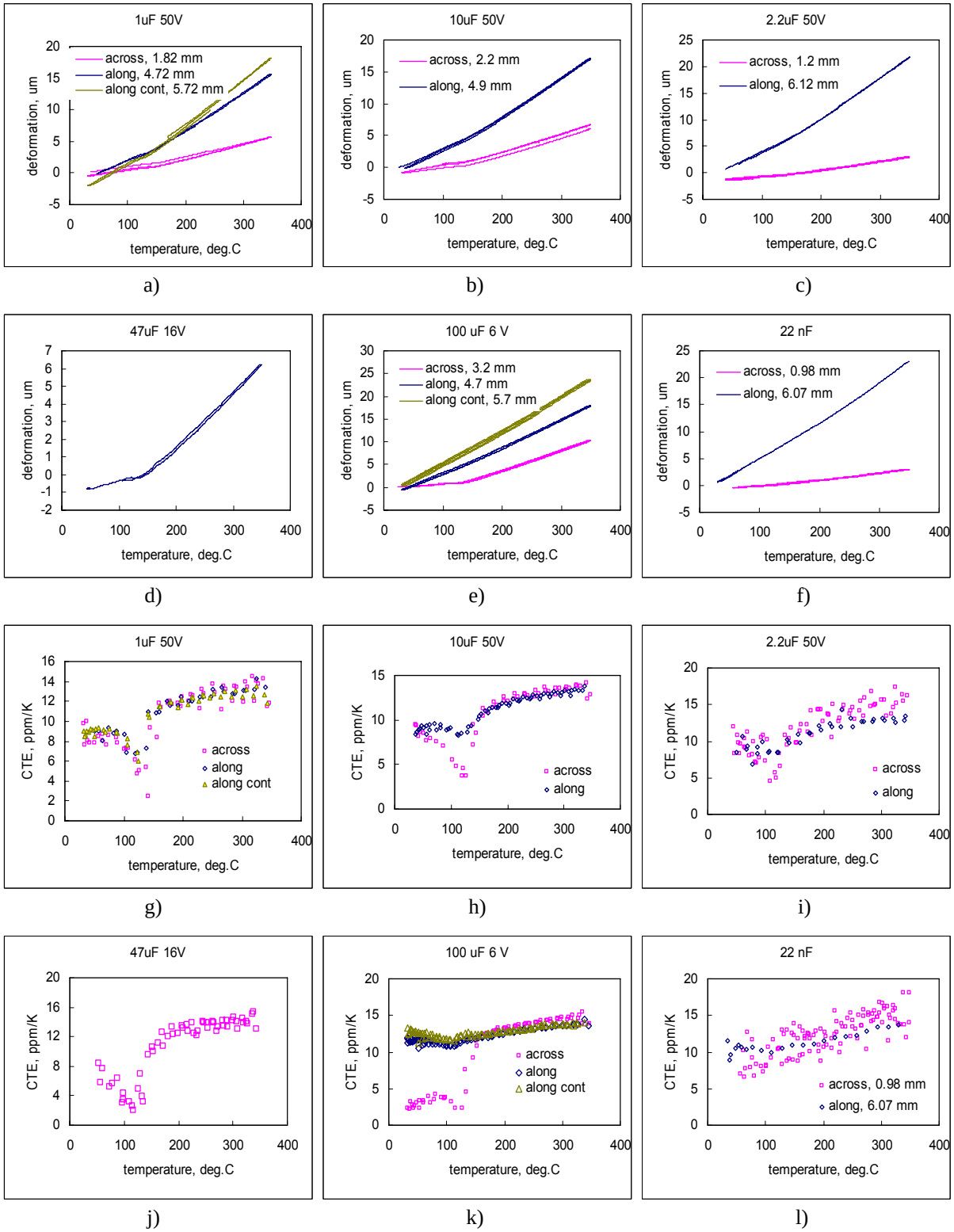


Figure 6. Temperature dependencies of deformation (a-f) and CTE (g-l) for six different types of capacitors.

3.2. Vickers indention test.

Average values of the size of imprints and crack lengths for different types of capacitors were measured using a SEM, and variations of these parameters with load are plotted in Figure 7. The imprint size increases with load sublinearly, and the spread of data obtained for three samples is relatively small, below 9%, indicating a high reproducibility of hardness measurements. As expected, the spread of the crack lengths was greater, but it still remained within 20%, indicating a reasonable level of reproducibility of the measurements. Note that cracks radiating from the corners of the imprints were observed in all samples and at all levels of the load, except for 22 nF capacitors at a load of 2 N. This is due to a higher fracture toughness of COG dielectrics compared to X7R materials.

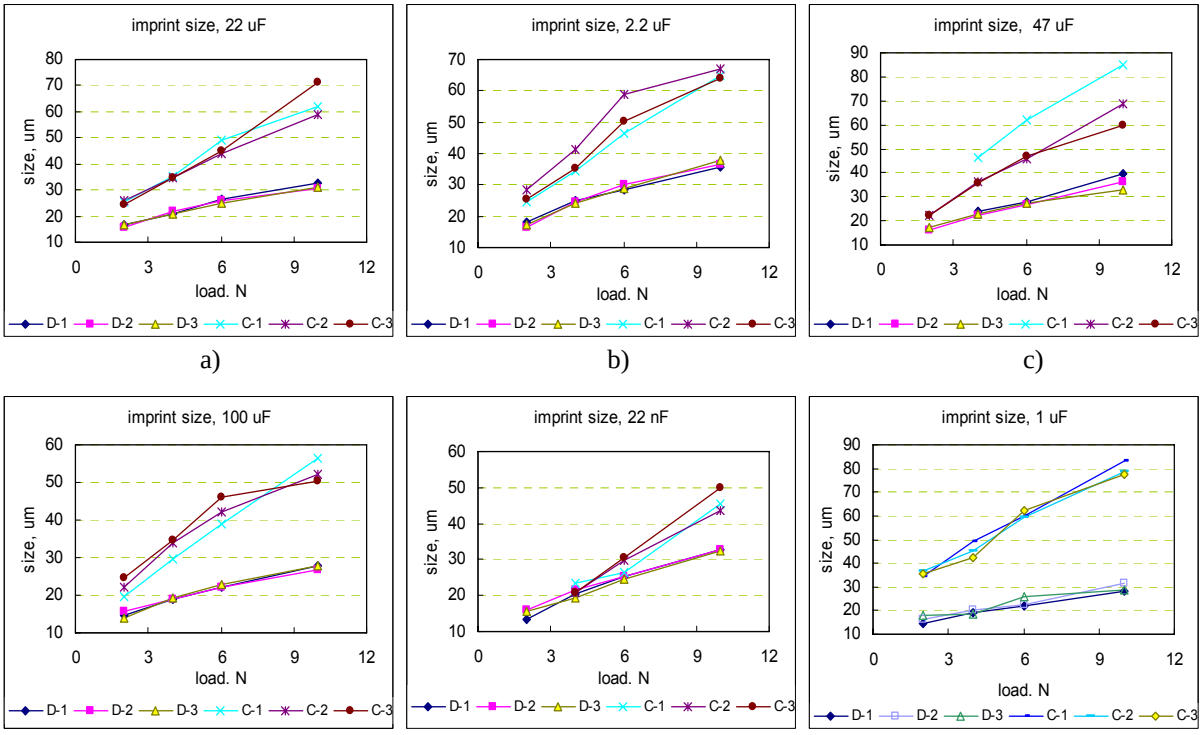


Figure 7. Variations of the size of imprints (D) and the length of radial cracks (C) in different types of capacitors. Each mark corresponds to an average value calculated for five to 12 impressions.

Based on results presented in Figure 7 and using Eq. (1), Vickers hardness was calculated for different load levels. Results of these calculations are presented in Figure 8 and indicate a relatively minor increase of VH with the load. This allowed for characterization of each part type with an average value of hardness. The average values together with the respective standard deviations are displayed in Table 3. Indentation fracture toughness was calculated using Eq. (1) and (2) and is shown in Figure 9. The values of K1C were virtually independent of the load for all part types, thus also allowing characterization of the capacitors with an average fracture toughness and standard deviation (see Table 3).

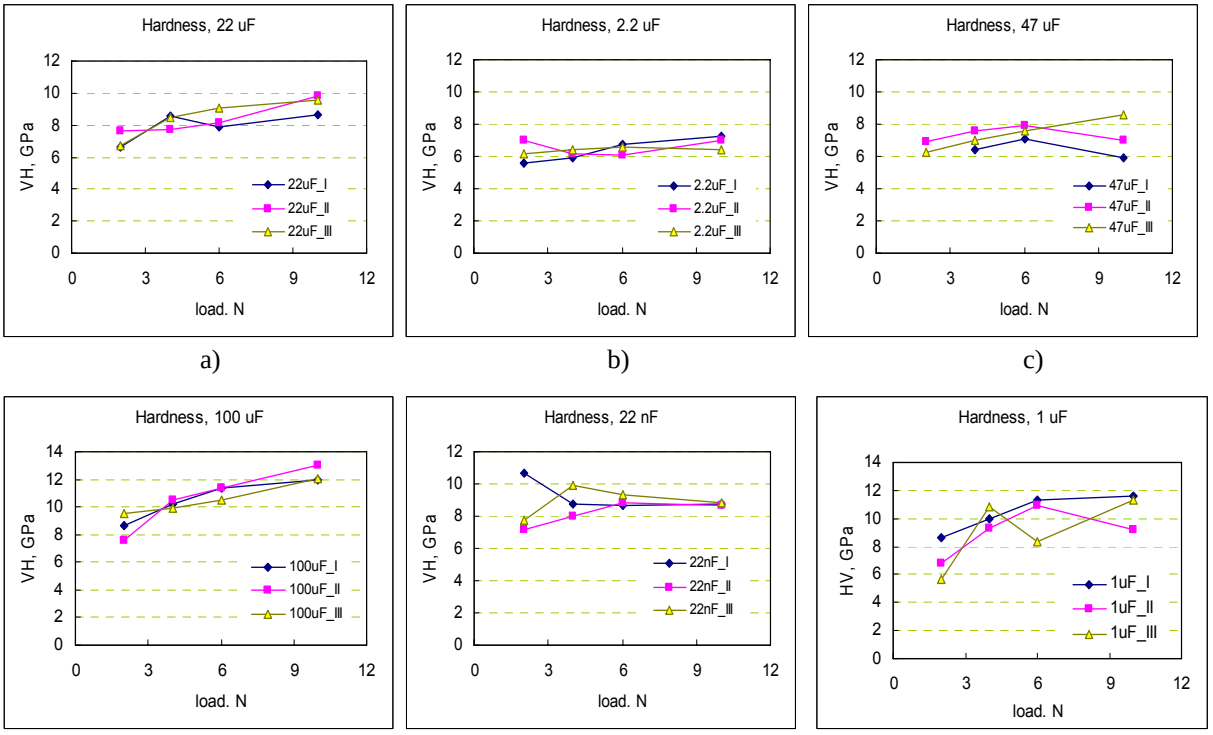


Figure 8. Variations of Vickers hardness with load for six different types of capacitors.

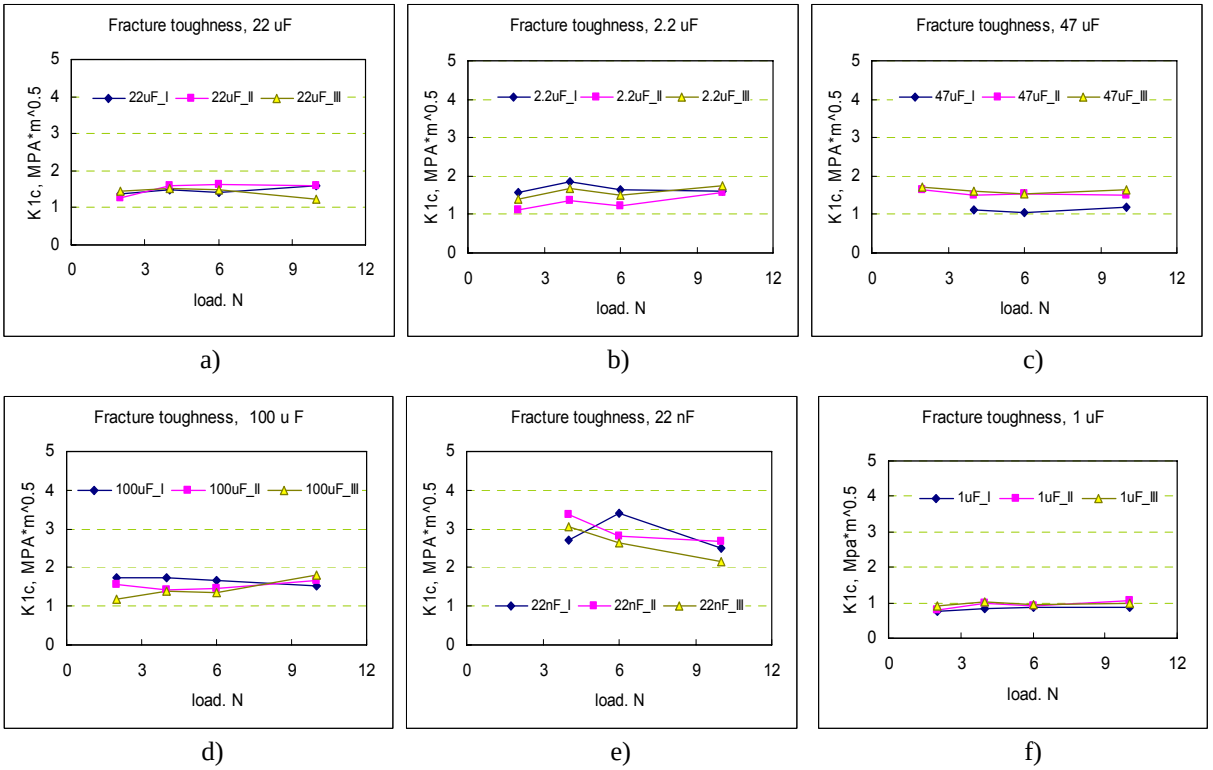


Figure 9. Variations of fracture toughness with load for six different types of capacitors.

Hardness of different capacitors varied in the range from 6.5 GPa to 10.6 GPa and did not depend on the type of materials used. According to Wereszczak et al. [35], the hardness of X7R materials was in a narrow range of 11 GPa to 12 GPa, which is close to our data. The reason for relatively low values obtained for 2.2 µF 50 V and 47 µF 16 V capacitors is not clear. Although VH does not indicate the potential mechanical robustness of MLCCs directly, its value can provide some insight into the effects of porosity and grain size because hardness is typically an inverse function of the amount of porosity [35].

Table 3. Hardness and fracture toughness of ceramic capacitors.

Capacitor	HV, GPa	STD	K1C, MPa-m$^{0.5}$	STD
1.0 µF, 50 V	9.49	1.66	0.91	0.07
100 µF, 6.3 V	10.57	1.57	1.55	0.09
2.2 µF, 50 V	6.45	0.30	1.52	0.14
10 µF, 50 V	10.37	1.03	1.06	0.13
47 µF, 16 V	6.62	1.22	1.37	0.08
22 nF, 50 V	8.78	0.19	2.81	0.32
22 µF, 25 V	8.24	0.97	1.47	0.07

Analysis of results presented in Table 3 shows that for X7R dielectrics the fracture toughness varies from 0.9 to 1.55 MPa-m$^{0.5}$, and it is much higher for the NPO dielectric, 2.8 MPa-m$^{0.5}$. These results are in agreement with the data reported by other authors [5, 35, 38]. Based on statistically significant variations of K1C, capacitors can be arranged in a row with increased fracture toughness: 1 µF 50 V ≈ 10 µF 50 V < 47 µF 16 V < 22 µF 25 V ≈ 2.2 µF 50 V ≈ 100 µF 6 V << 22 nF 50 V. The mechanical stability of the parts was expected to increase in the same sequence.

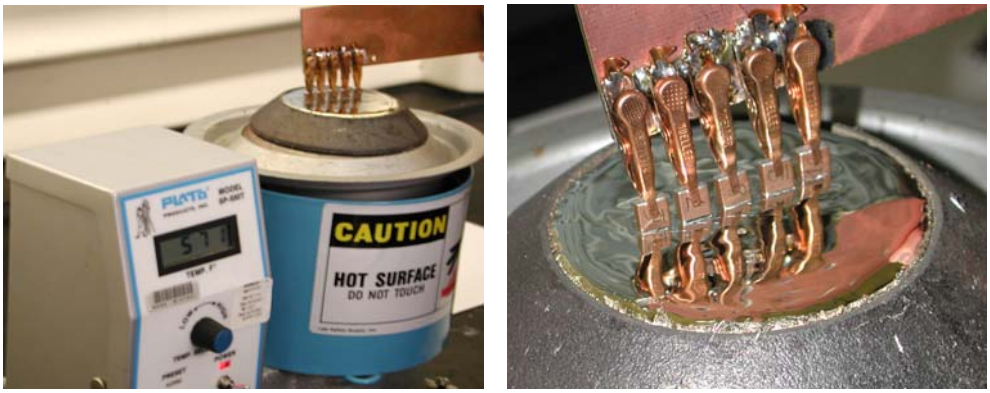
4. Effect of thermal shock.

When temperature at the surface of a ceramic capacitor that is stabilized at temperature T_o suddenly changes to temperature T, the surface areas experience deformation compared to the internal areas of the part that remain at T_o. This causes development of mechanical stresses that depend on the thermal and mechanical characteristics of the ceramic and vary with time due to changes in temperature distribution through the part. The value of temperature difference $\Delta T = T - T_o$, at which cracking is observed, can be used to characterize the thermal shock resistance of the part, ΔT_f.

Experiments for assessment of the robustness of MLCCs to thermal shocks were carried out by preheating the parts to a certain temperature and then quenching them into water at room temperature [38] or at 0 ^oC (ice water) [8, 46]. The value of the thermal shock resistance temperature, ΔT_f, was estimated using measurements of leakage currents of the capacitors after water quenching. Depending on the part type and size of capacitors, experimental values of ΔT_f for X7R materials varied in the range from 120 ^oC to 440 ^oC.

At relatively low ΔT_f temperatures, the probability of cracking is extremely small. The effect of preheating of ceramic capacitors having sizes 1206 and 0805 at temperatures ranging from 155 ^oC to 100 ^oC on results of wave reflow soldering at 235 ^oC did not reveal any thermal cracking or leakage current failures [22].

To simulate the effect of thermal shock conditions that a capacitor might experience during manual soldering, the parts were installed in a fixture as is shown in Figure 10, and their terminals were brought into thermal contact for 5 seconds with molten solder maintained at 300 ^{o}C. After that, the parts were cooled at room temperature for 5 minutes, and the procedure was repeated. Twenty samples of each part type were subjected to this terminal-thermal-shock testing. Considering that in our experiments the temperature during thermal shock increased rapidly by 280 ^{o}C, and the capacitors experienced 100 shocks, it was expected that cracking would appear at least in some lots. However, none of the parts manifested cracking or failures during this testing.



a) b)

Figure 10. Overall (a) and close-up (b) views of the parts during terminal-thermal-shock testing.

Electrical measurements and visual control using an optical microscope were carried out after 10, 30, and 100 thermal shocks. Results of DCL measurements are presented in Figure 11. Note that the DCL levels for 22 nF 50 V NPO capacitors were below 1 nA, which is the sensitivity level for the measurement system used in this study. For this reason, data for the NPO parts are not presented.

No anomalies during I-t measurements or any substantial increase in the leakage currents were detected during the post-cycling current monitoring. No defects were found during multiple optical examinations at 10X magnification. Measurements of AC characteristics (see Figure 12) also did not reveal any anomaly. The vicinal illumination technique [30] used to examine surface areas of the capacitors near terminals at 200X magnification upon test completion failed to reveal any cracks.

The results indicate that manual-soldering-induced thermal shocks do not cause damage to normal-quality large ceramic capacitors. If parts are not susceptible to thermal-shock cracking, multiple-shock stresses likely will not cause formation of defects after up to 100 thermal shocks.

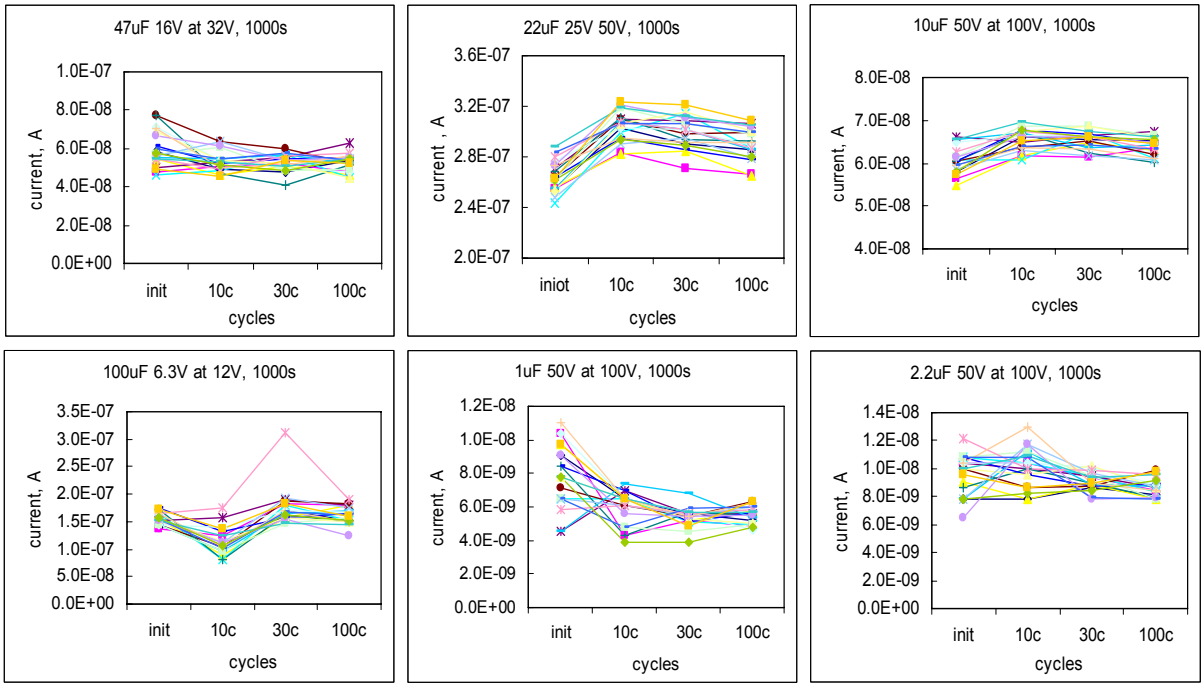


Figure 11. Variations of leakage currents during terminal-thermal-shock cycling for six types of MLCCs. Each chart shows data for 20 samples.

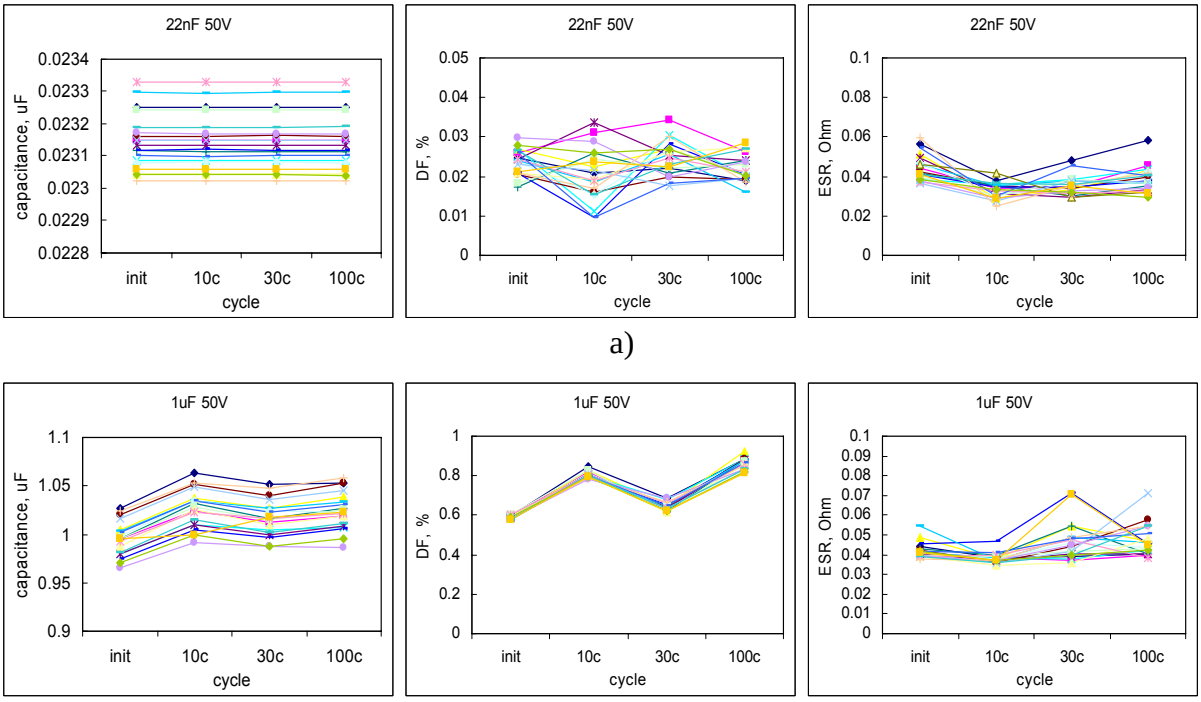
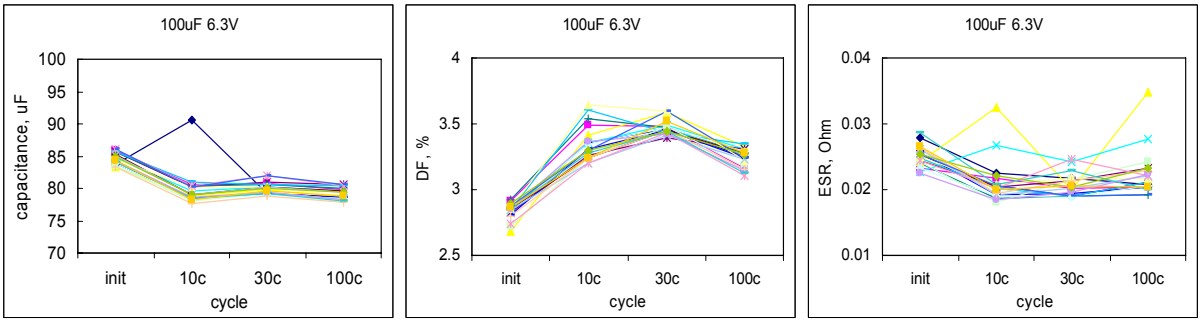


Figure 12.a. Variations of capacitance, dissipation factors, and equivalent series resistances during terminal-thermal-shock cycling for two types of capacitors. Each chart shows data for 20 samples.



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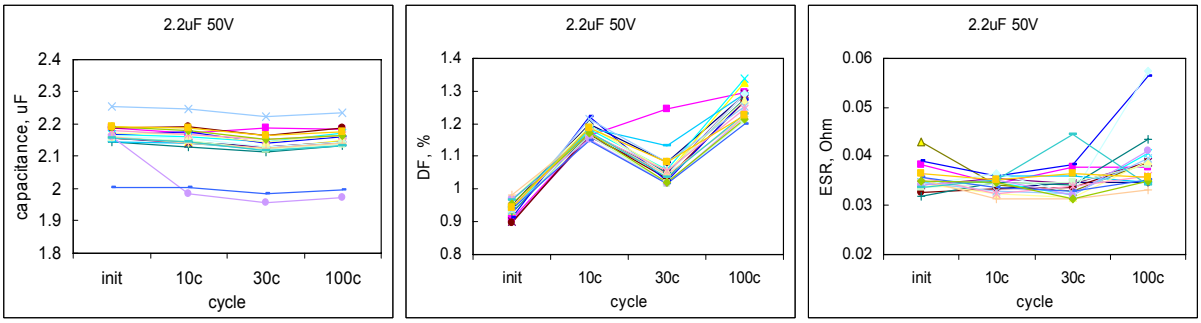

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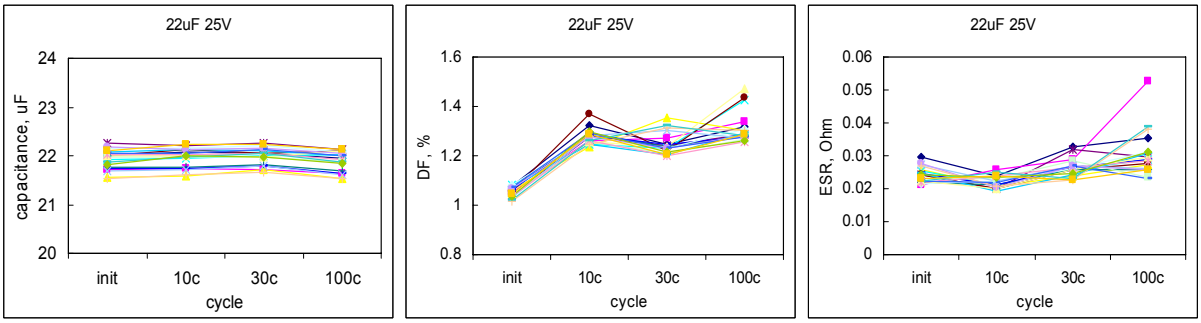
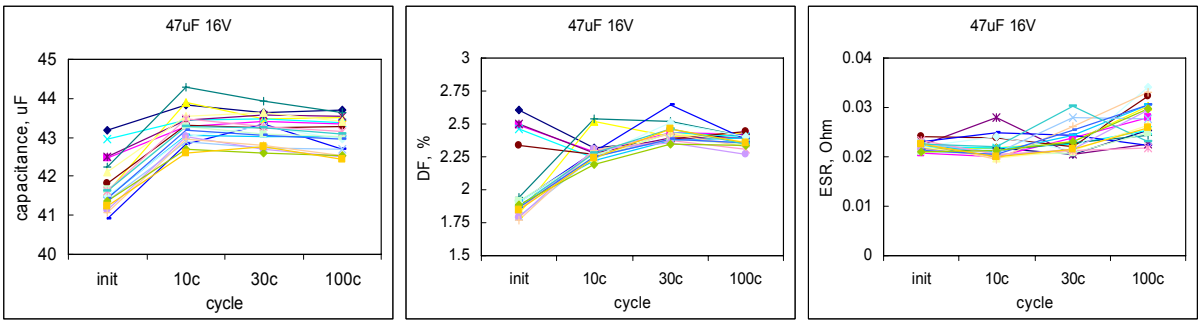


e)

Figure 12.b. Variations of capacitance, dissipation factors, and equivalent series resistances during terminal-thermal-shock cycling for three more types of capacitors. Each chart shows data for 20 samples.



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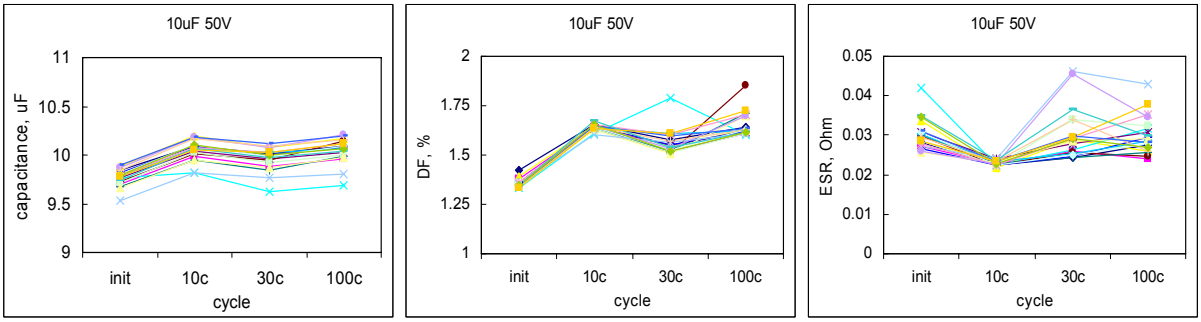


g)

Figure 12.c. Variations of capacitance, dissipation factors, and equivalent series resistances during terminal-thermal-shock cycling for two types of capacitors. Each chart shows data for 20 samples.

5. Effect of excessive solder.

Due to the difference between CTE of solder (~24 ppm/K) and ceramic materials (10 to 14 ppm/K), an excessive amount of solder might create significant compressive stresses at the terminals of capacitors upon cooling to room temperature. As ceramic materials have a very high compressive strength, these stresses likely will not cause cracking. However, relaxation of stresses with time due to solder creeping might result in formation of tensile stresses when the part is heated after some time of being stored at normal conditions. It is also possible that solder-induced compression at the terminals would cause a moment of force and form tensile stresses at the surface of the ceramic near the terminals.

To evaluate the effect of solder-induced stresses, large solder blocks were attached to one of the terminals of each capacitor tested. To form these blocks uniformly, a eutectic solder was molten in a cylindrical depression made in a Teflon plate. One terminal of each of the capacitors was immersed into the solder that was then solidified forming blocks shown in Figure 13. Five samples of each part type were prepared using this technique.

Figure 13. Examples of solder blocks attached to terminals of different types of capacitors to simulate the effect of stresses caused by excessive solder.

Capacitance, dissipation factor, and leakage currents of the parts were measured after various tests shown in Table 4. Methanol testing was used after each of the stress tests to better reveal possible cracks. For this reason DCL measurements were made twice, first right after completion of the stress testing, and second after methanol application.

Table 4. Test flow for capacitors with solder blocks.

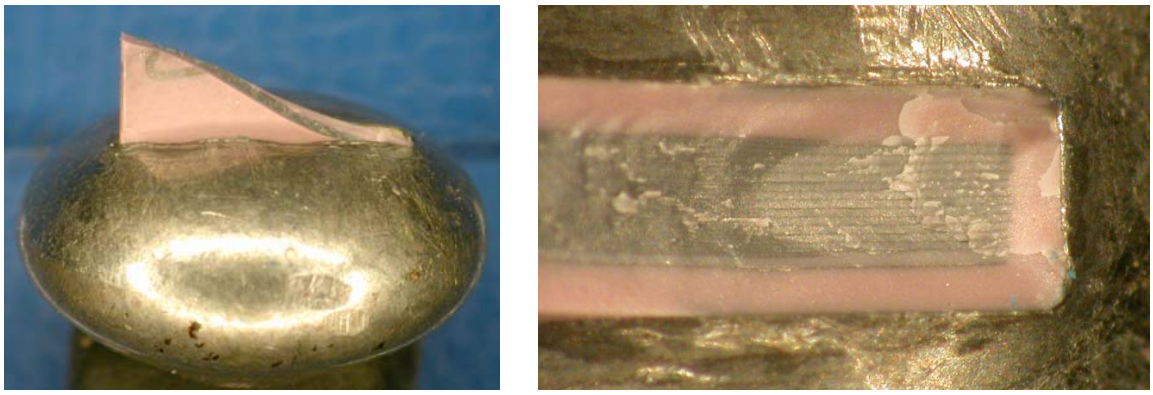
Test Type	Index	Temperature Range, ^{o}C	Condition	Number of Cycles
Temp. Cycle	TC1	+25 to +165	Dwell 10 min., ramp 10 min.	20
Temp. Cycle	TC2	+25 to -65	Dwell 10 min., ramp 10 min.	20
Temp. Cycle	TC3	-65 to +150	Dwell 10 min., ramp 10 min.	20
Thermal Shock	TS	-65 to +150	Dwell 10 min., ramp 0.1 min.	20
Immersion into Liquid Nitrogen	LN	+25 to -196	Dwell 1 min., ramp 0.1 min.	1

The parts were subjected to different types of temperature cycles and thermal shocks according to a test flow shown in Table 4. During TC1 test, the parts were subjected to 20 cycles between room temperature and +165 ^{o}C to create tensile stresses at high temperatures. During the next test, TC2, the parts were stressed at negative temperatures (to -65 ^{o}C) to squeeze the terminals by compressive stresses induced by solder, and possibly create local tensile stresses in ceramic along the edges of the solder chunk. Test TC3 combined the effects of both previous tests.

The thermal shock test, TS, was performed at the same temperature conditions as temperature cycling test TC3, but with the temperature ramp increased by more than 100 times. It is possible that at slow temperature variations the stress relaxation is significant, so the TS test was carried out to reveal the effect of temperature rate on test results. During the last test, LN, the parts were immersed directly into liquid nitrogen at -196 ^{o}C to create extreme thermal shock conditions and further increase the level of compressive stresses.

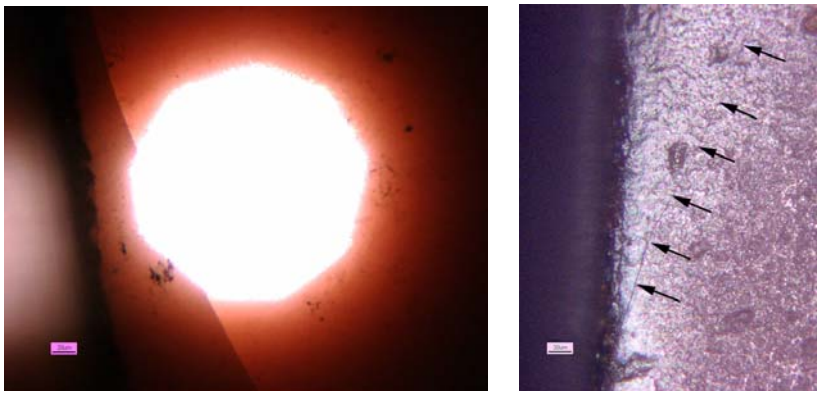
Fractures were observed only in samples of 22 nF 50 V NPO capacitors. One sample, SN 23, fractured after TC2 testing (see Figure 14). Another sample from this lot, SN 22, was found shorting at ~70 kOhm during post-TC2 methanol testing. However, low-power optical microscope examinations did not reveal any anomalies. After testing, all parts were examined using the vicinal illumination technique [30] and cracks originating from the solder edge, similar

to those shown in Figure 15, were revealed in all 22 nF 50 V capacitors. No cracks were found in X7R capacitors even after exposure to the liquid nitrogen temperature.



a) b)

Figure 14. Side (a) and top (b) views of a 22 nF 50 V sample that fractured after TC2. Note that the crack originated from the surface of the capacitor at the edge of solder chunk.



a) b)

Figure 15. A typical crack exposed in 22 nF 50 V capacitors by the vicinal illumination technique (a). Figure b) shows a crack observed at X100 magnification.

Results of electrical testing of the parts are shown in Figures 16 and 17 and can be summarized as follows:

1. Temperature cycling affected the value of capacitance in all parts with X7R dielectrics. Exposure to high temperatures increased C by ~4% to 5%, and exposure to low temperatures decreased capacitance by ~5% to 7%.
2. Dissipation factors increased in X7R parts through the testing by 30% to 50%. The most significant variations happened after TC1, when the parts were exposed to high temperatures only.
3. Leakage currents were stable through the testing in three out of seven of the tested lots: 47 µF 16 V, 100 µF 6 V, and 22 µF 25 V capacitors.

4. Three lots had instances of increased DCL:
   4.1. One sample in the 1 µF 50 V lot of capacitors increased DCL by an order of magnitude after TC3; however, further testing did not confirm the presence of cracking.
   4.2. An increase in DCL of more than an order of magnitude was detected in one of the samples from the 10 µF 50 V lot. However, this increase occurred during the first DCL measurements and was not confirmed by the methanol test.
   4.3. Three out of five samples increased in DCL values by up to two orders of magnitude through the testing after TC2 in a lot of 2.2 µF 50 V capacitors.
5. In a lot of 22 nF 50 V NPO capacitors, one sample fractured and two more showed anomalously high leakages after TC2 cycling. These parts also manifested anomalies during C and DF measurements.

An increase of capacitance upon exposure to high temperatures is a known phenomenon and is related to the aging of MLCCs that results in changes of the domain structure and causes a linear capacitance decrease with the logarithm of time. Annealing of the parts at temperatures exceeding the Curie temperature (de-aging) restores the value of capacitance and explains increase in C after high-temperature cycling, TC1. Most likely the observed increase in dissipation factors after TC1 is also due to the de-aging effect that reverses decrease of dielectric losses with time of aging. Note that the last temperature the parts experienced during TC3 cycling was 150 ^{o}C. For this reason similar values of C were measured after TC1 and TC3. NPO dielectrics do not exhibit this phenomenon. This explains stability of capacitance after TC1 for 22 nF 50 V capacitors.

Possible reasons of decrease of capacitance are less obvious. Most likely this effect is due to stress-induced variations of the dielectric constant in barium titanate ceramics. It is known that mechanical stresses lead to development of 90^{o} domains in $BaTiO_3$ materials that might decrease polarization [47]. Experiments with MLCCs showed that compressive stresses applied perpendicular to electrode plates might significantly decrease dielectric constant of ceramic materials [44, 45, 48]. The decrease of C by 5% to 7% that was observed during experiments might be due to relatively minor stresses in the range from 20 MPa to 40 MPa. It is possible to assume that substantial tensile stresses developed in solder at low temperatures due to CTE mismatch between solder and ceramic cause formation of additional compressive stresses in ceramic when the part is brought back to room temperature. Note that for all part types the values of C after exposure to -65 ^{o}C and to -196 ^{o}C remain the same, thus indicating that the effect does not increase significantly with the temperature swing.

Although temperature conditions for TC3 and TS were similar, capacitance of the parts after TS was lower than after TC1 or TC3. This might be due to more substantial residual compressive stresses created by fast changes of temperature when creeping of the solder does not have time to develop.

Optical examinations revealed cracks on all 22 nF 50 V capacitors; however, two parts did not have any significant degradation of leakage currents. It is possible that cracks in these two parts were shallow and did not cross opposite electrodes.

Five samples in three lots of X7R capacitors had DCL anomalies, but optical examinations revealed no cracks. A failure analysis might be necessary to confirm the presence of cracks in

these parts. However, in the absence of hard shorts, the probability of revealing possible microcracks is not high.

Analysis shows some correlation between the thickness of capacitors and the probability of cracking and/or having a DCL anomaly. The thinnest parts, 22 nF 50 V capacitors with H = 1.05 mm, had the largest proportion of fractures and DCL failures. Multiple DCL anomalies were observed in 2.2 µF 50 V capacitors with H = 1.27 mm. Two part types, 1 µF 50 V and 10 µ /50 V capacitors, had one sample each with increased DCL values; these parts had thicknesses of 1.85 mm and 2.2 mm, respectively. The thickness in the rest of parts that had no anomalies exceeded 2.3 mm.

Interestingly, in several cases application of methanol for parts with excessive DCL values decreased leakage currents, thus casting some doubt on the effectiveness of this test. It is possible that these results are due to preheating at 85 ^{o}C that was used before immersing capacitors into methanol. The purpose of this preheating was to expand the crack and enhance penetration of methanol. However, preheating results also in moisture removal that might have an adverse effect on the leakage currents.

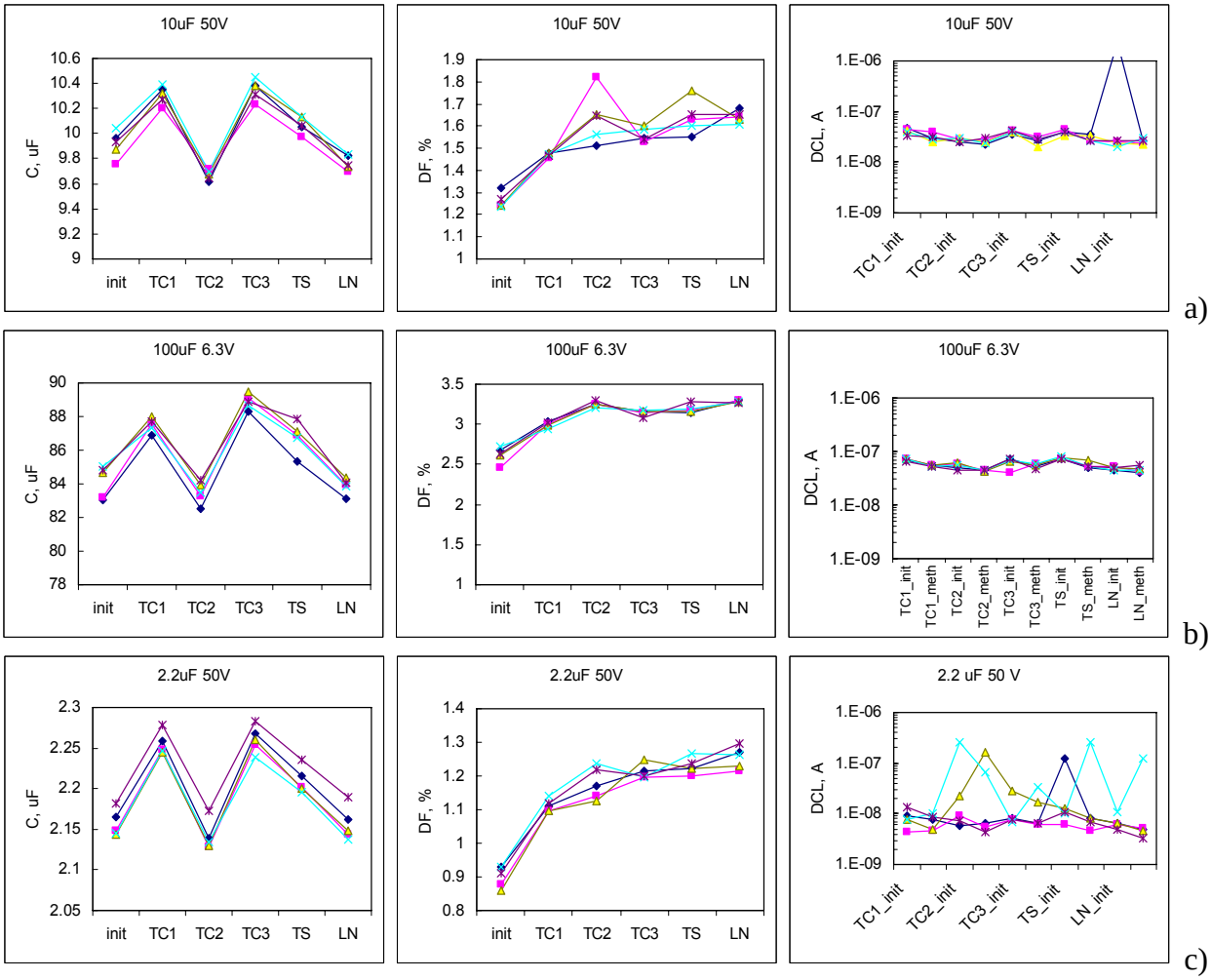
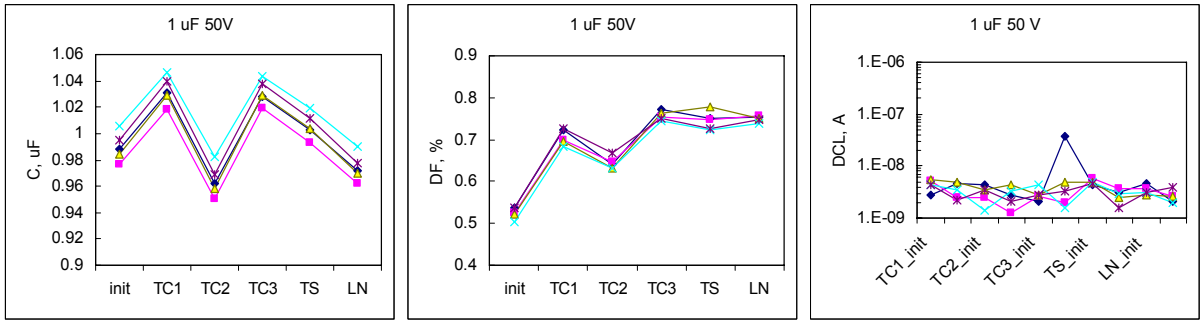


Figure 16. Effect of temperature cycling and thermal shocks for 10 µF 50 V (a), 100 µF 6 V (b), and 22 µF 50 V (c) ceramic capacitors with solder blocks.



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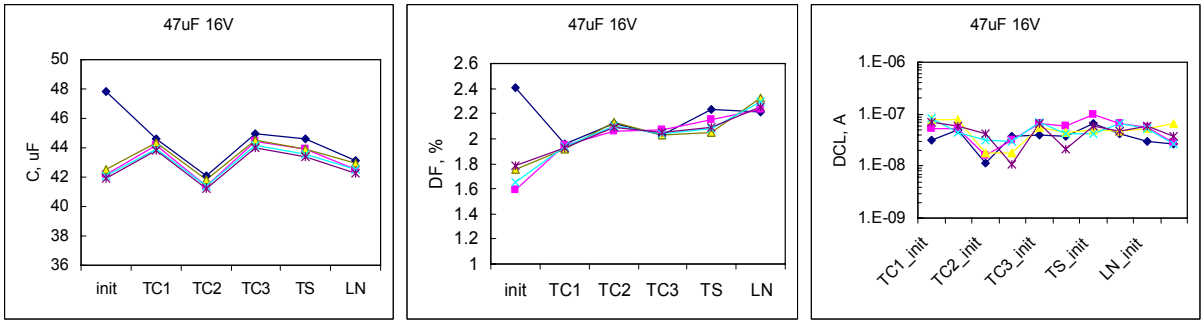

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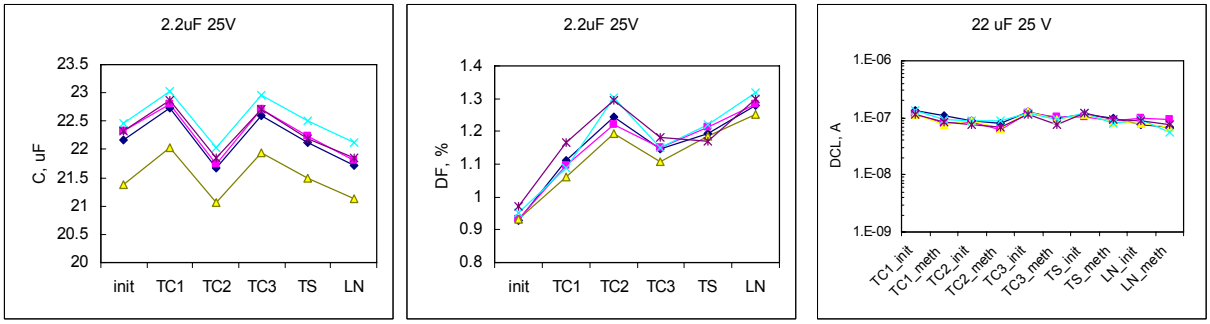

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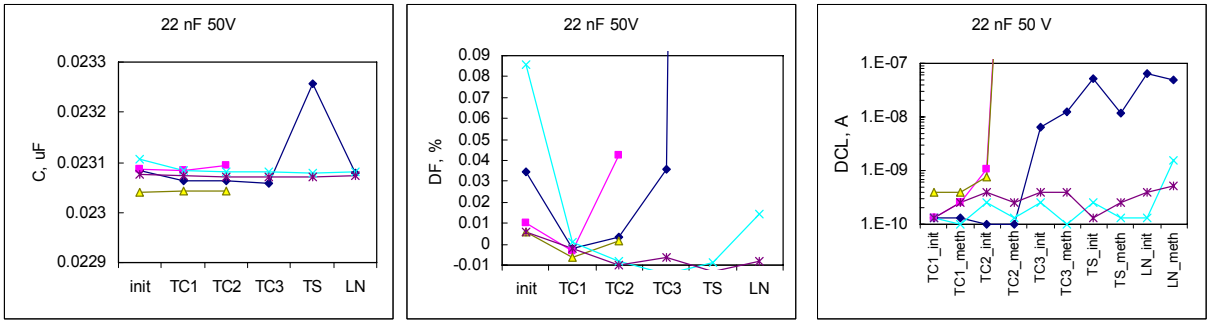

d)

Figure 17. Effect of temperature cycling and thermal shocks for 1 µF 50 V (a), 47 µF 16 V (b), 22 µF 25 V (c), and 22 nF 50 V (d) ceramic capacitors with solder blocks.

6. Effect of TC after soldering onto an FR4 board.

To evaluate the effect of thermomechanical stresses developed in capacitors mounted onto a PWB during temperature excursions on the probability of cracking, 10 samples from four different lots (100 µF 6 V, 22 µF 25 V, 47 µF 16 V, and 10 µF 50 V) were soldered onto a 3.1 mm thick FR4 board and subjected to temperature cycling between -65 ^{o}C and +150 ^{o}C. An overall view of the board is shown in Figure 18. Leakage currents at the twice rated voltages were monitored during 1,000 seconds of electrification. These measurements were carried out on loose capacitors, after soldering, and after 200 and 1,000 thermal cycles. It was expected that by using a relatively thick FR4 board and a wide range of temperature variations, cycling would eventually result in cracking and increase of leakage currents in the parts.

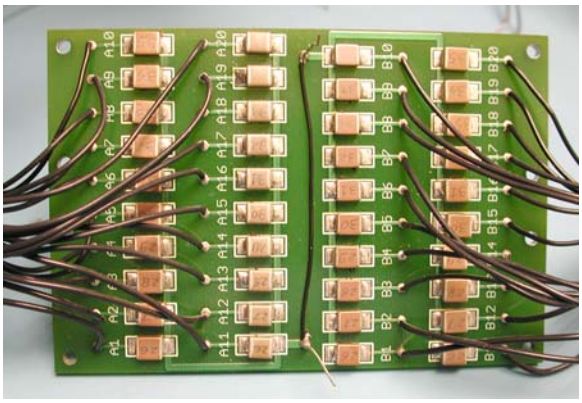

Figure 18. A test board with soldered capacitors.

Results of temperature cycling tests are presented in Figure 19. The leakage currents were stable through the testing in three out of four lots. After 1,000 cycles, one out of 20 samples from a 10 µF 50 V lot had unstable currents indicating intermittency, likely inside the part. This intermittency could be related to microcracking; however, external examinations did not reveal any anomaly. Additional analysis is required to verify this failure.

A high mechanical stability of large MLCCs subjected to temperature cycling is likely due to the fact that ceramic capacitors soldered onto an FR4 board remain under compressive stresses even at temperature extremes. For space projects, temperature extremes during box-level thermal cycling are typically within the range from -40 ^{o}C and +85 ^{o}C. Assuming the exponent in the Coffin-Manson equation for the acceleration factor of temperature cycling test is equal to 3, the 1,000 cycles between -65 ^{o}C and +150 ^{o}C would be equivalent to more than 5,000 box-level cycles. Our results show that at these conditions no wear-out failures in ceramic capacitors would be likely to occur.

These experiments, as well as solder-dip cycling tests, showed that cracking does not occur even after multiple cycles of exposure to extreme temperatures. It is possible that cracking is related to the preexisting flaws. Additional analysis of conditions that possibly might cause cracking during manual soldering of large MLCC is planned for next year's NASA Electronic Parts and Packaging (NEPP) Program task.

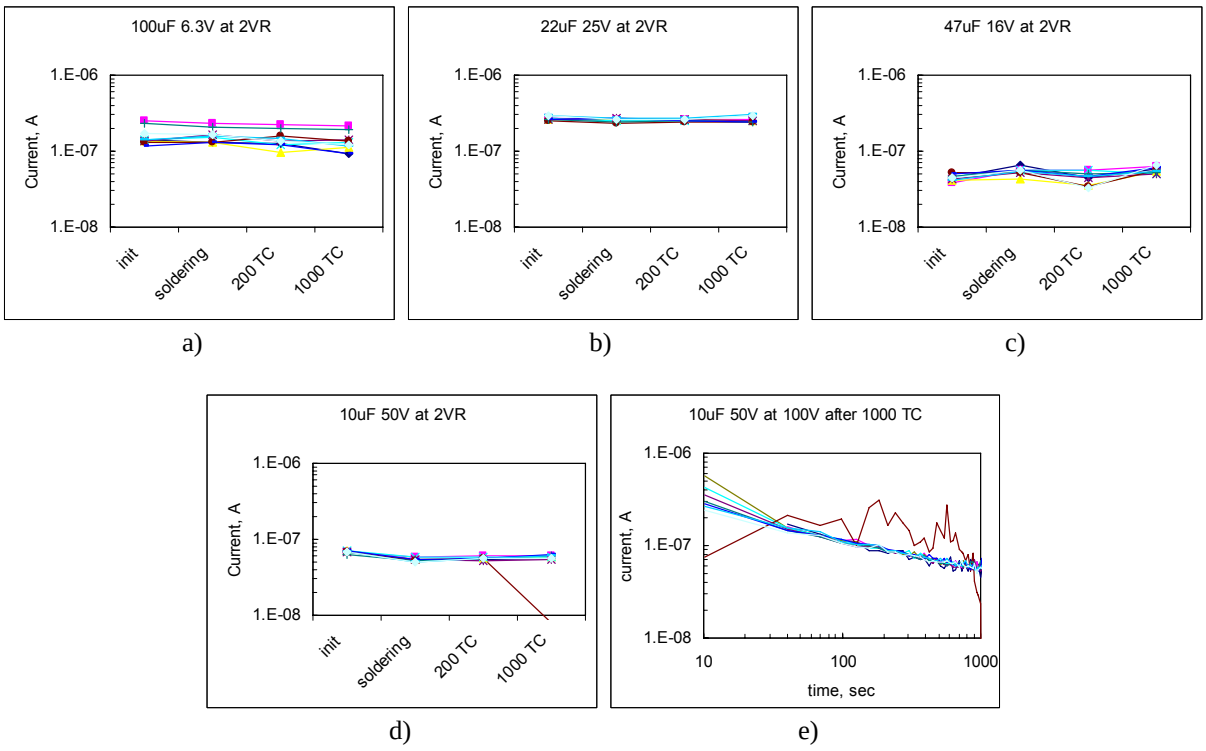

Figure 19. Leakage currents in four part types after soldering them onto an FR4 board and temperature cycling between -65 ^{o}C and +150 ^{o}C (a-d). Figure e) shows relaxation of leakage currents in 10 µF 50 V capacitors after 1,000 thermal cycles.

7. Summary.

1. Based on literature data, major sources, mechanisms of formation, and techniques for revealing cracking in MLCCs have been analyzed and classified. Possible reasons of manual-soldering-induced cracking have been discussed and areas of investigation have been determined.

2. Coefficients of thermal expansion were measured on six types of capacitors in the range of temperatures from room to 350 ^{o}C. All X7R capacitors had extreme temperature dependencies of CTE with the minimal values at Curie temperature. Average CTE values at T > Tc were in the range from 12.1 ppm/K to 14.4 ppm/K for all part types. At T < Tc CTE values were lower, and for different lots varied from 3.1 ppm/K to 9.6 ppm/K. CTE values in X7R capacitors measured perpendicular to the plates were ~10% greater than those measured along the plates. This anisotropy is likely due to built-in compressive stresses that are caused by CTE mismatch between ceramic materials and metal electrode plates, and were formed during sintering of capacitors.

3. Mechanical behavior of the parts was characterized by measurements of Vickers hardness and fracture indention toughness, K1C. Hardness of different types of capacitors varied in the range from 6.5 GPa to 10.6 GPa and did not depend significantly on the type of materials used. Estimations of the fracture toughness showed that X7R dielectrics had K1C values in the range from 0.9 to 1.55 MPa-m$^{0.5}$, whereas capacitors with COG

dielectric had a much larger value, 2.8 MPa-$m^{0.5}$. According to these measurements, the mechanical stability of the parts was expected to increase in the sequence 1 µF 50 V ≈ 10 µF 50 V < 47 µF 16 V < 22 µF 25 V ≈ 2.2 µF 50 V ≈ 100 µF 6 V << 22 nF 50 V.

4. To simulate thermal shock conditions that are specific to manual soldering, 20 samples of each of the seven lots of MLCCs were subjected to the molten solder (300 ^{o}C) terminal dip test. Characteristics of the parts were measured after 10, 30, and 100 solder pot cycles. No cracking or significant parametric variations were observed during this testing. This indicates that for normal-quality parts, thermal shock associated with manual soldering is likely not the major reason for cracking.

5. The effect of mechanical stresses created by excessive solder was investigated using ceramic capacitors with large solder chunks attached to the terminals. The parts were subjected to various temperature cycling and thermal shock tests while their characteristics were measured periodically.
   a. Contrary to what was expected, the worst mechanical stability was observed in 22 nF 50 V NPO capacitors. Note that these parts were relatively thin, H = 1 mm, and it is possible that for solder-induced damage the thickness of the part plays a more important role than the fracture toughness. Cracks at the edges of terminals were revealed using the vicinal illumination technique in all 22 nF 50 V samples, while only three out of five parts had increased leakage currents.
   b. Three lots of X7R capacitors had no anomalies, two lots had one sample each with a one-time instance of DCL increase, and one lot had three out of five samples manifesting unstable leakage currents through the testing. All anomalies were observed after exposure of the parts to low temperatures (-65 ^{o}C), whereas no failures occurred after cycling between room temperature and +165 ^{o}C. Optical examinations revealed no cracks in X7R parts. Analysis showed that all failures occurred in relatively thin capacitors, and that the probability of solder-induced damage increases as the thickness of capacitors diminishes.
   c. TC and TS tests revealed a memory effect in all X7R capacitors with attached solder chunks. The value of C measured at room temperature changed systematically on 4% to 7% depending on the last temperature during the cycling. Capacitance increased after exposure to high temperatures (150 ^{o}C to 165 ^{o}C), and decreased after exposure to negative temperatures (-65 ^{o}C to -196 ^{o}C). The first effect is due to de-aging of MLCCs at T > Tc, and the second is likely related to formation of solder-induced compressive stresses. These stresses are known to decrease dielectric constant in ferroelectric materials. No significant variations of capacitance were observed in 22 nF 50 V parts employing NPO dielectric.

6. To estimate the effect of mechanical stresses related to CTE mismatch between the capacitors and the FR4 board, 40 X7R capacitors from four different lots were subjected to 1,000 temperature cycles between -65 ^{o}C and +150 ^{o}C. All parts passed 200 cycles, and only one part showed erratic leakage currents after 1,000 cycles. These data show that no wear-out failures would likely occur in PWB cards with soldered MLCCs during box-level temperature cycling tests in the range of temperatures from -40 ^{o}C to +85 ^{o}C.

7. The most effective methods for revealing cracks are monitoring of leakage currents at twice rated voltages and vicinal illumination optical microscopy technique. The success of using the methanol test was less than expected.

References.

[1] D. L. Kinser, S. M. Graff, and S. V. Caruso, "The relationship between reliability and bonding techniques in hybrid systems," *IEEE Transactions on Parts, Hybrids, and Packaging*, vol. PHP-11, 1975, pp. 195-201.

[2] T. Brennan, "Ceramic capacitor insulation resistance failures accelerated by low voltage," *IEEE Transactions on Electron Devices*, vol. ED-26, 1979, pp. 102-108.

[3] J. Maxwell, "Capacitor cracks: Still with us after all these years," 2006, http://www.johansondielectrics.com/technicalnotes/cra/.

[4] M. Keimasi, M. H. Azarian, and M. G. Pecht, "Flex cracking of multilayer ceramic capacitors assembled with Pb-free and tin-lead solders," *IEEE Transactions on Device and Material Reliability*, vol. 8, 2008, pp. 182-192.

[5] B. Rawal, M. Childs, A. Cooper, and B. McLaughlin, "Reliability of multilayer ceramic capacitors after thermal shock," Proceedings of the 38th Electronics Components Conference, 1988, pp. 371-375.

[6] "Multilayer ceramic capacitors. Effects of mechanical, thermal and electrical stress," 2006, www.epcos.com.

[7] J. D. Prymak and J. Bergenthal, "Capacitance monitoring while flex testing," *IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A*, vol. 18, 1995, pp. 180-186.

[8] F. Yeung, Y. Chan, Y. Wang, Z. Gui, and L. Li, "Thermal shock resistance of miniaturized multilayer ceramic capacitors," *Journal of Material Science: Materials in Electronics*, vol. 5, 1994, pp. 339-343.

[9] B. Sloka, D. Skamser, A. Hill, M. Laps, R. Grace, J. Prymak, M. Randall, and A. Tajuddin, "Flexure robust capacitors," Proceedings of the 27th Symposium for Passive Components, CARTS'07, Albuquerque, NM, 2007.

[10] J. Prymak, M. Prevallet, P. Blais, and B. Long, "New improvements in flex capabilities for MLC chip capacitors," Proceedings of the 26th Symposium for Passive Components, CARTS'06, Orlando, FL, 2006, pp. 63-76.

[11] J. Maxwell, "Cracks: The hidden defect," Proceedings of the 38th Electronics Components Conference, 1988, pp. 376-384.

[12] L. Condra, G. Johnson, M. Pecht, and A. Christou, "Evaluation of manufacturing variables in the reliability of surface mount capacitors," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 15, 1992, pp. 542-552.

[13] M. Tarr, "Failure mechanisms in ceramic capacitors," Proceedings of Online Postgraduate Courses for the Electronics Industry, 2007, http://www.ami.ac.uk/courses/topics/0179_fmcc/index.html.

[14] N. Blattau, P. Gormally, V. Iannaccone, L. Harvilchuck, and C. Hillman, "Robustness of surface mount multilayer ceramic capacitors assembled with Pb-free solder," *DfR Solutions Publication*, 2006, http://www.dfrsolutions.com/pdfs/Capcracking_whitepaper_2005.pdf.

[15] J. Sergent, "Ceramic materials," *Ceramic Interconnect Technology Book*, F. Barlow and A. Elshabini, Eds.: CRC Press, 2007, pp. 163-196.

[16] T. Nomura, J. Miura, T. Arashi, Y. Nakano, and A. Sato, "Multilayer ceramic capacitors: Recent trends," Proceedings of the 10th IEEE International Symposium on Applications of Ferroelectrics, ISAF '96, 1996, pp. 135-141.

[17] S. Haishan and C. Shoutian, "Charge-discharge breakdown of dielectric ceramic," Proceedings of the 6th International Conference on Properties and Applications of Dielectric Materials, Xi'an, China, 2000, pp. 1029-1032.
[18] L. Bin, C. Wei, Z. Yajie, and C. Shoutian, "Distribution regularity of breakdown field strength of high voltage ceramic capacitor," Proceedings of the 6th International Conference on Properties and Applications of Dielectric Materials, 2000, pp. 1037-1040.
[19] M. Stewart, "A soft termination MLCC solution to guard against capacitor crack failures," Proceedings of the 25th Symposium for Passive Components, CARTS'05, Palm Springs, CA, 2005, pp. 219-224.
[20] N. Blattau, D. Barker, and C. Hillman, "Lead free solder and flex cracking failures in ceramic capacitors," Proceedings of the 24th Symposium for Passive Components, CARTS'04, San Antonio, TX, 2004, pp. 101-105.
[21] M. Cozzolino, "Electrical shorting in multilayer ceramic capacitors," Proceedings of the 24th Symposium for Passive Components, CARTS'04, San Antonio, TX, 2004, pp. 57-68.
[22] D. D. Chang and F. R. Anderson, "Effect of board design and assembly process on leakage currents of ceramic chip capacitors," *40th Electronic Components and Technology Conference*, vol. 2, 1990, pp. 1035-1041.
[23] J. Brusse and M. Sampson, "COTS ceramic chip capacitors: An evaluation of the parts and assurance methodologies," Proceedings of the 24th Symposium for Passive Components, CARTS'04, San Antonio, TX, 2004, pp. 128-141.
[24] H. C. Ling and A. M. Jackson, "Correlation of silver migration with temperature-humidity-bias (THB) failures in multilayer ceramic capacitors," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 12, 1989, pp. 130-137.
[25] G. D. Giacomo, "*Reliability of Electronic Packages and Semiconductor Devices,"* McGraw Hill, 1996.
[26] R. Chittick, E. Gray, J. Alexander, M. Drake, and E. Bush, "Non-destructive screening for low-voltage failure in multilayer ceramic capacitors," Proceedings of the 3rd Capacitor and Resistor Technology Symposium, CARTS'83, Phoenix, AZ, 1983, pp. 61-69.
[27] N. H. Chan and B. S. Rawal, "Low-voltage performance of multilayer ceramic capacitors," *AVX Technical Information*, 2000, pp. 1-5.
[28] G. Brook, M. Azarian, and M. Pecht, "Evaluation of surface mount MLCCs," *Fall PHM Consortium*, College Park, MD, 2008.
[29] J. Brussay, "General guidelines for optical inspection techniques to detect cracks in MLCCs," 2008.
[30] S. Hull, "Nondestructive detection of cracks in ceramics using vicinal illumination," Proceedings of the 25th International Symposium for Testing and Failure Analysis, ISTFA, Santa Clara, CA, 1999, pp. 217-223.
[31] D. S. Erdahl and I. C. Ume, "Online-offline laser ultrasonic quality inspection tool for multilayer ceramic capacitors," *IEEE Transactions on Advanced Packaging*, vol. 27, 2004, pp. 647-653.
[32] B. Wunderle, T. Braun, D. May, and A. Mazloum, "Non-destructive failure analysis and modeling of encapsulated miniature SMD ceramic chip capacitors under thermal and mechanical loading," Proceedings of the 13th International Workshop on Thermal Investigation of ICs and Systems, THERMINIC 2007, 2007, pp. 104-109.

[33] "Recommended attachment techniques for ATC multilayer chip capacitors," Proceedings of Bulletin 201, AT#001-119, 2007, www.atceramics.com.
[34] J. Vivari, "Manual soldering options for high reliability applications," Proceedings of IMAPS, Providence, RI, 2008, pp. 666-672.
[35] A. Wereszczak, L. Riester, and K. Brederl, "In-situ mechanical property evaluation of dielectric ceramics in multilayer capacitors," 1998, www.osti.gov/bridge/servlets/purl/755654-4MKsH7/native/755654.pdf.
[36] J. d. Toonder, C. Rademaker, and C. Hu, "Residual stresses in multilayer ceramic capacitors: Measurement and computation," *Journal of Electronic Packaging*, vol. 125, 2003, pp. 506-511.
[37] G. D. Quinn and R. C. Bradt, "On the Vickers indentation fracture toughness test," *Journal of the American Ceramic Society*, vol. 80, 2007, pp. 673-680.
[38] C. Koripella, "Mechanical behavior of ceramic capacitors," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 14, 1991, pp. 718-724.
[39] K. Strecker, S. Ribeiro, and M. Hoffmann, "Fracture toughness measurements of LPS-SiC: A comparison of the indentation technique and the SEVNB method," *Materials Research*, vol. 8, 2005, pp. 121-124.
[40] F. Sergejev and M. Antonov, "Comparative study on indentation fracture toughness measurements of cemented carbides," *Proceedings of Estonian Academy of Science and Engineering*, vol. 12, 2006, pp. 388-398.
[41] M. Pharr, Y. Katoh, and H. Bei, "Dependence of fracture toughness on crystallographic orientation in single-crystalline silicon carbide," *Journal of Undergraduate Research U.S. Department of Energy*, 2007, pp. 59-64, http://www.scied.science.doe.gov.
[42] Y. He, "Heat capacity, thermal conductivity, and thermal expansion of barium titanate-based ceramics," *Thermochimica Acta*, vol. 419, 2004, pp. 135-141.
[43] G. Scott and G. Astfalk, "Thermal stresses in multilayer ceramic capacitors: Numerical simulations," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 13, 1990, pp. 1135-1145.
[44] G. Yang, Z. Yue, T. Sun, W. Jiang, X. Li, and L. Liz, "Evaluation of residual stress in a multilayer ceramic capacitor and its effect on dielectric behaviors under applied DC bias field," *Journal of American Ceramic Society*, vol. 91, 2008, pp. 887-892.
[45] Y. Nakano, T. Nomura, and T. Takenaka, "Residual stress of multilayer ceramic capacitors with Ni-electrodes (Ni-MLCCs)," *Japanese Journal of Applied Physics*, vol. 42, 2003, p. 6041.
[46] Y. C. Chan and F. Yeung, "Failure analysis mechanisms of miniaturized multilayer ceramic capacitors under normal service conditions," Proceedings of 43rd Electronic Components and Technology Conference, 1993, pp. 1152-1155.
[47] A. J. Moulson and J. M. Herbert, "*Electroceramics,"* Willey, 2003.
[48] G. Yang, Z. Yue, T. Sun, H. Gou, and L. Li, "Effect of combined external uniaxial stress and DC bias on the dielectric property of BaTiO3-based dielectrics in multilayer ceramic capacitor: Thermodynamics and experiments," *Journal of Physics D: Applied Physics*, vol. 41, 2008, pp. 1-6.