CY7C1399BN

256-Kbit (32 K × 8) Static RAM

Features

- Temperature Ranges
  - Industrial: –40 °C to 85 °C
  - Commercial: 0 °C to 70 °C
  - Automotive-A: –40 °C to 85 °C
- Single 3.3 V power supply
- Ideal for low-voltage cache memory applications
- High speed: 12 ns
- Low active power
  - 180 mW (max)
- Low-power alpha immune 6T cell
- Available in pb-free and non pb-free plastic SOJ and TSOP- I packages

Functional Description

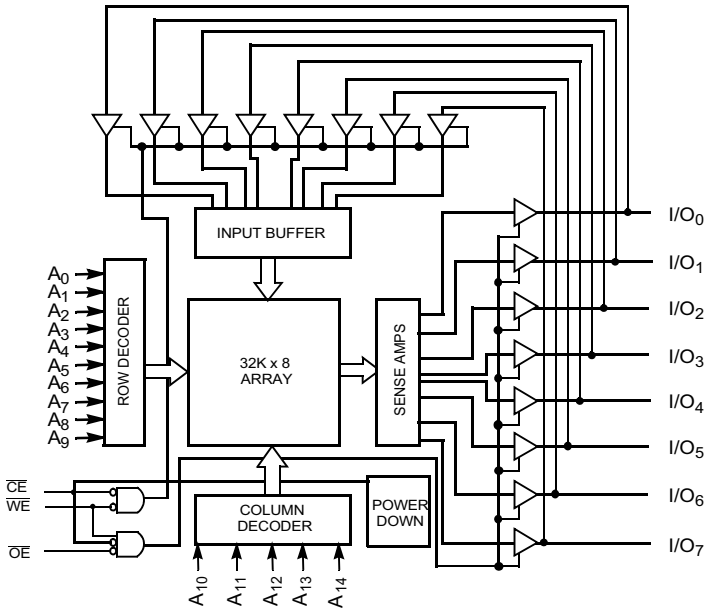
The CY7C1399BN is a high-performance 3.3 V CMOS Static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and active LOW Output Enable ($\overline{OE}$) and tristate drivers. The device has an automatic power-down feature, reducing the power consumption by more than 95% when deselected.

An active LOW Write Enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and Write Enable ($\overline{WE}$) is HIGH. The CY7C1399BN is available in 28-pin standard 300-mil-wide SOJ and TSOP Type I packages.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pin Configurations

Figure 1. 28-pin TSOP pinout (Top View)

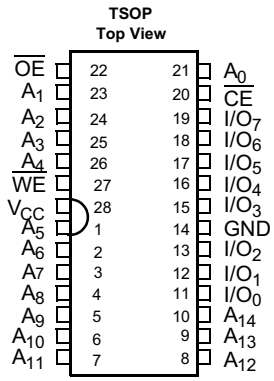
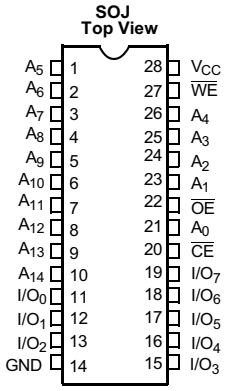


Figure 2. 28-pin SOJ pinout (Top View)



Selection Guide

Description	Condition	-12	-15
Maximum access time (ns)		12	15
Maximum operating current (mA)		55	50
Maximum CMOS standby current (μA)	Commercial	500	–
	Commercial (L)	50	–
	Industrial	500	500
	Automotive-A	–	500

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND [1] .....–0.5 V to +4.6 V

DC voltage applied to outputs in high Z State [1] .....–0.5 V to V_{CC} + 0.5 V

DC input voltage [1] .....–0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 300 mV
Industrial	–40 °C to +85 °C	
Automotive-A	–40 °C to +85 °C	

Electrical Characteristics

Over the Operating Range

Parameter [1]	Description	Test Conditions		-12		-15		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	Min V_{CC}, I_{OH} = –2.0 mA		2.4	–	2.4	–	V
V_{OL}	Output LOW voltage	Min V_{CC}, I_{OL} = 4.0 mA		–	0.4	–	0.4	V
V_{IH}	Input HIGH voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL} [1]	Input LOW voltage			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input leakage current			–1	+1	–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_{IN} ≤ V_{CC}, Output disabled		–5	+5	–5	+5	µA
I_{CC}	V_{CC} operating supply current	Max V_{CC}, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$		–	55	–	50	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH}, or V_{IN} ≤ V_{IL}, f = f_{MAX}	Commercial	–	5	–	–	mA
			Commercial (L)	–	4	–	–	mA
			Industrial	–	5	–	5	mA
			Automotive-A	–	–	–	5	mA
I_{SB2}	Automatic CE Power-down current – CMOS inputs [2]	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, WE ≥V_{CC} – 0.3 V or WE ≤ 0.3 V, f = f_{MAX}	Commercial	–	500	–	–	µA
			Commercial (L)	–	50	–	–	µA
			Industrial	–	500	–	500	µA
			Automotive-A	–	–	–	500	µA

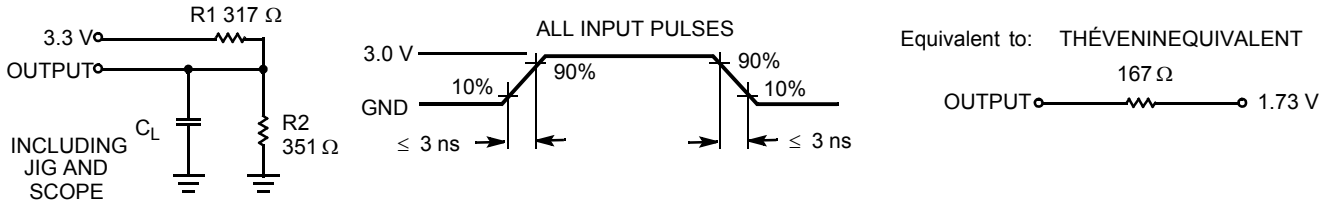
Notes
1. Minimum voltage is equal to –2.0 V for pulse durations of less than 20 ns.
2. Device draws low standby current regardless of switching on the addresses.

Capacitance

Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}: Addresses	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	5	pF
C_{IN}: Controls			6	pF
C_{OUT}	Output capacitance		6	pF

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [4]



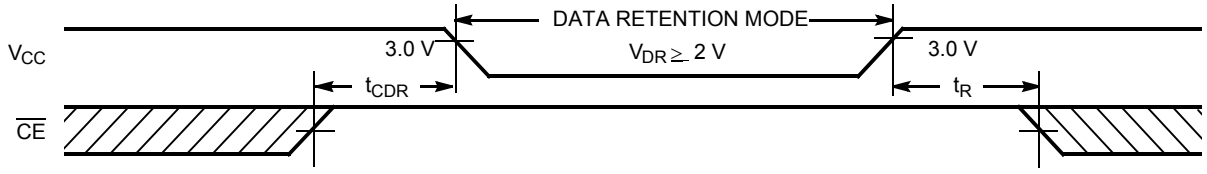
Data Retention Characteristics

(Over the Operating Range - L version only)

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2.0	–	V
I_{CCDR}	Data retention current	V_{CC} = V_{DR} = 2.0 V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	0	20	µA
t_{CDR}	Chip deselect to data retention time		0	–	ns
t_R	Operation recovery time		t_{RC}	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

3. Tested initially and after any design or process changes that may affect these parameters.
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and capacitance C_L = 30 pF.

Switching Characteristics

Over the Operating Range

Parameter [5]	Description	-12		-15		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	12	–	15	–	ns
t_{AA}	Address to data valid	–	12	–	15	ns
t_{OHA}	Data hold from address change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	12	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5	–	6	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [6]	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [6, 7]	–	5	–	6	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [6]	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [6, 7]	–	6	–	7	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	12	–	15	ns
Write Cycle [8, 9]						
t_{WC}	Write cycle time	12	–	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	8	–	10	–	ns
t_{AW}	Address setup to write end	8	–	10	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	8	–	10	–	ns
t_{SD}	Data setup to write end	7	–	8	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ low to high Z[8]	–	7	–	7	ns
t_{LZWE}	$\overline{WE}$ high to low Z[6]	3	–	3	–	ns

Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and capacitance C_L = 30 pF.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, t_{HZWE} are specified with C_L = 5 pF as in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle #3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1 [10, 11]

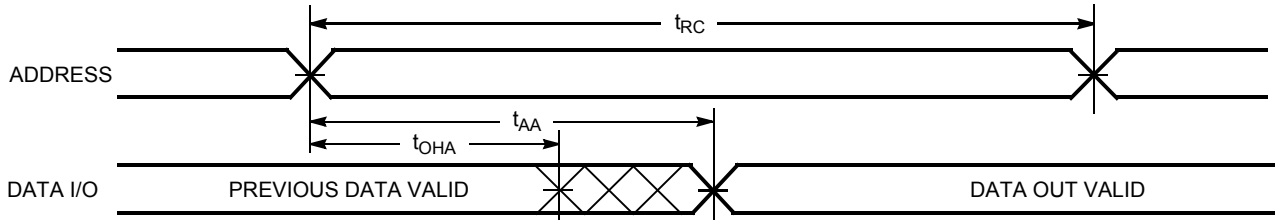
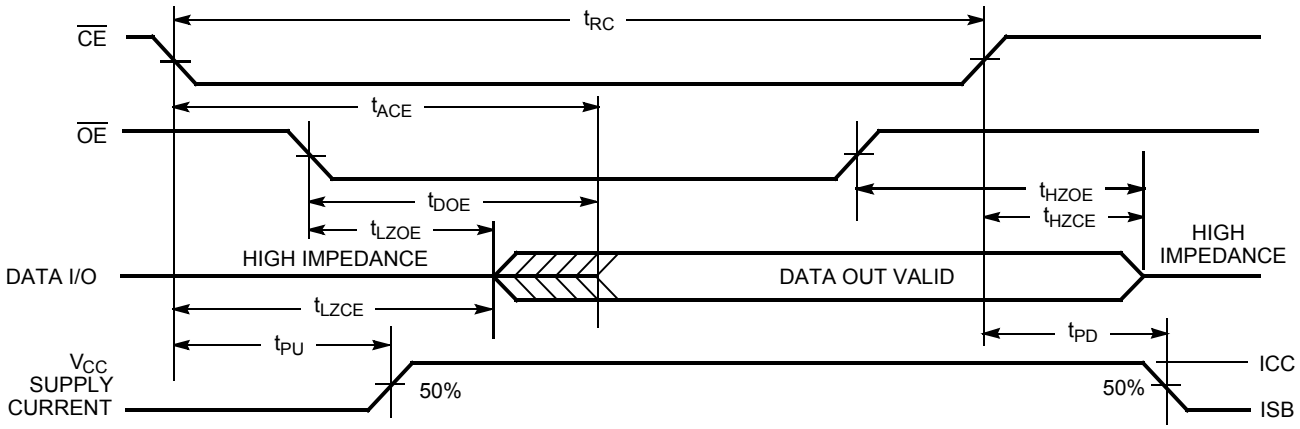


Figure 6. Read Cycle No. 2 [11, 12]



Notes
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled) [13, 14, 15]

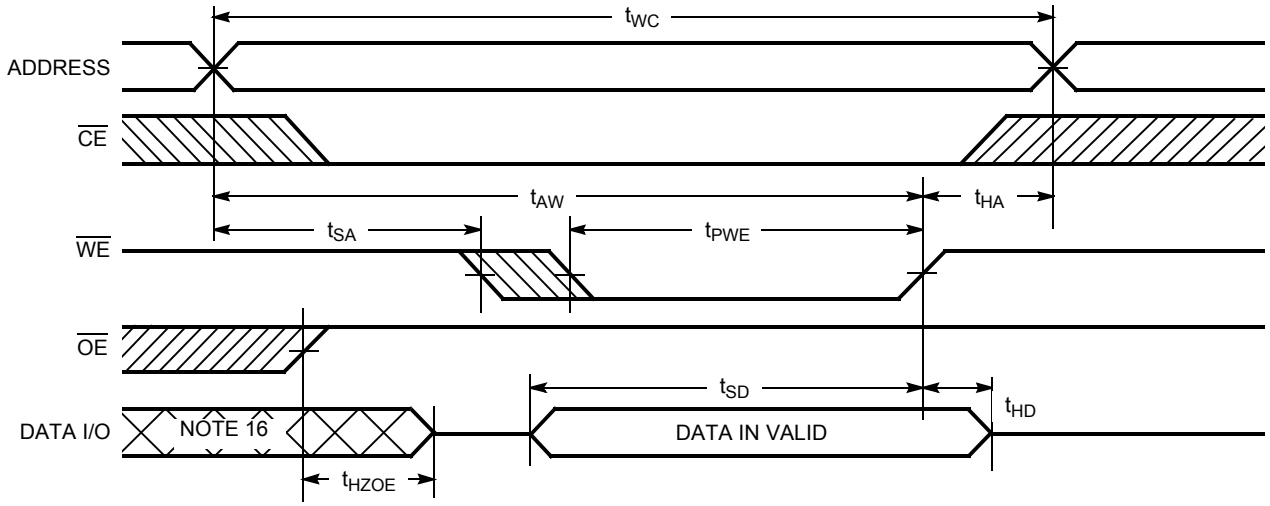
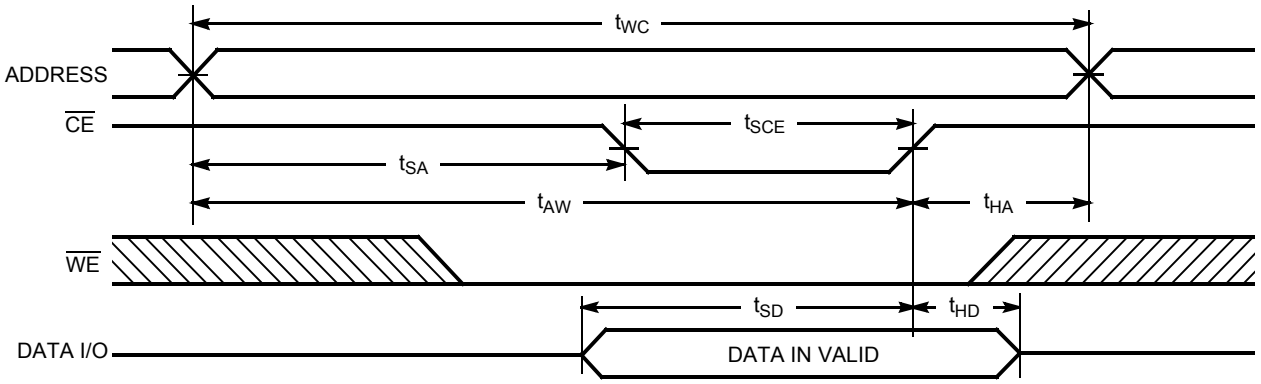


Figure 8. Write Cycle No. 2 ($\overline{CE}$ Controlled) [13, 14, 15]

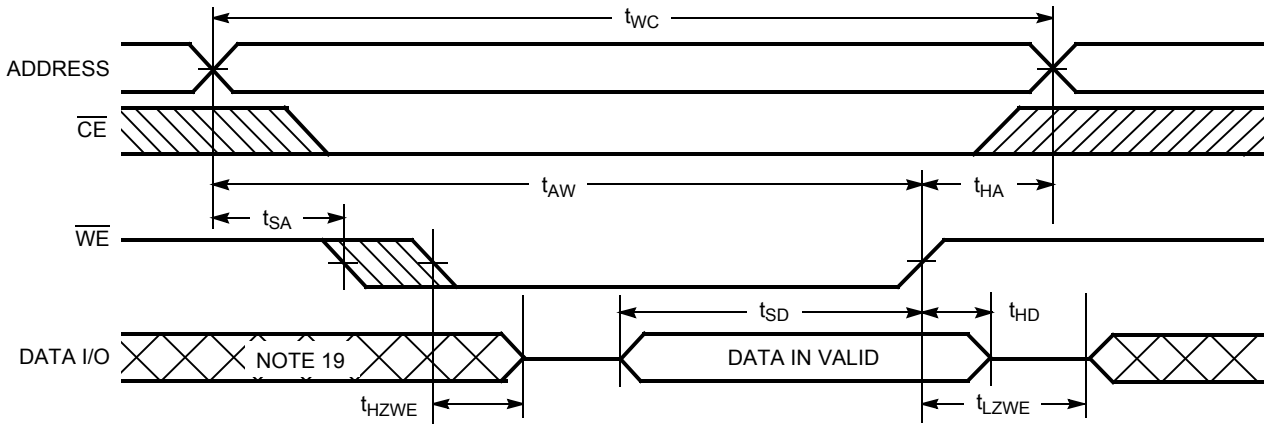


Notes

13. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [17, 18]



Notes
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
18. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD}.
19. During this period, the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output disabled	Active (I_{CC})

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.
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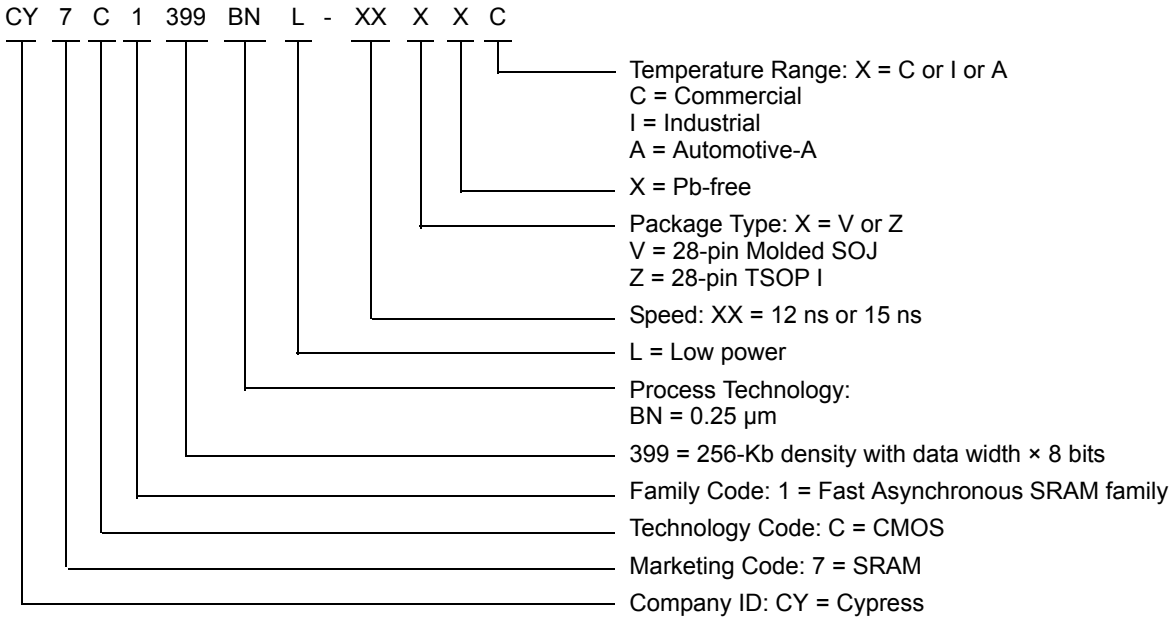
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1399BN-12ZXC	51-85071	28-pin TSOP I (Pb-free)	Commercial
	CY7C1399BNL-12ZXC		28-pin TSOP I (Pb-free)	
	CY7C1399BN-12VXI	51-85031	28-pin molded SOJ (Pb-free)	Industrial

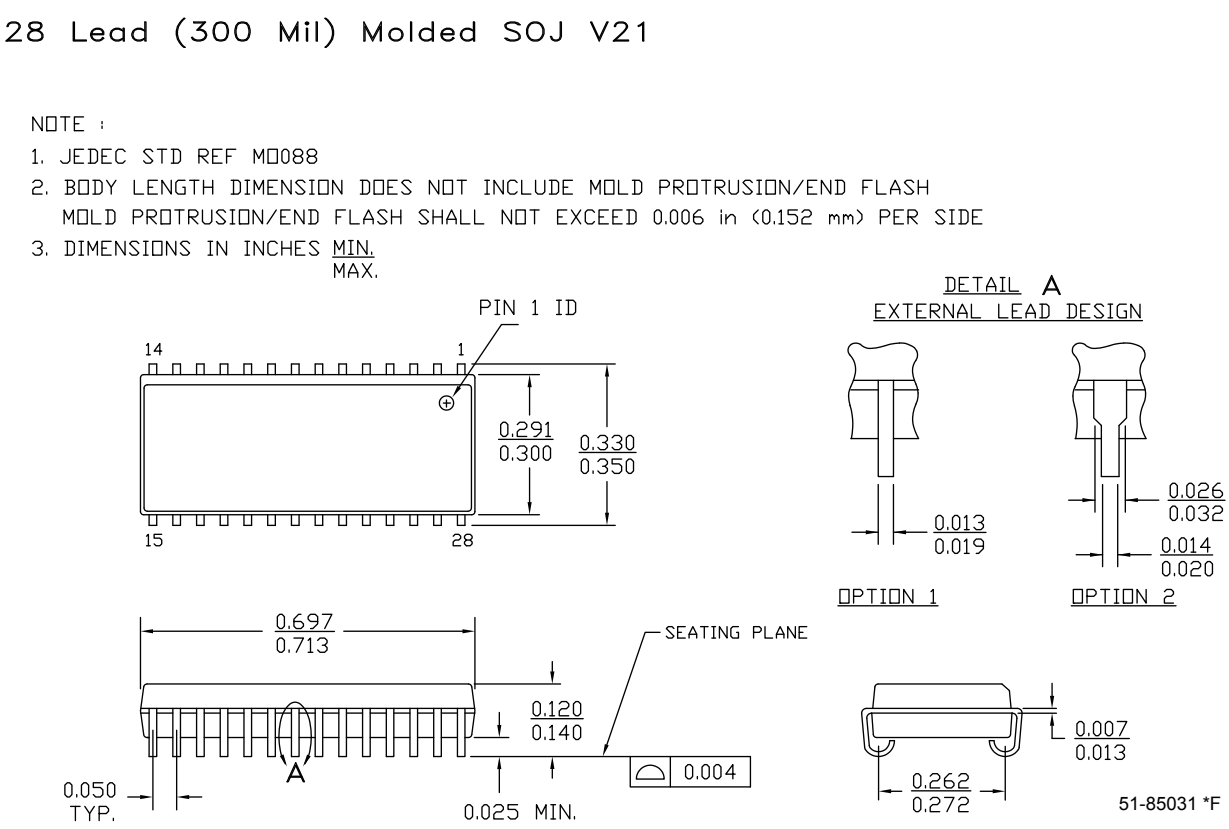
Contact your local sales representative regarding availability of these parts.

Ordering Code Definitions



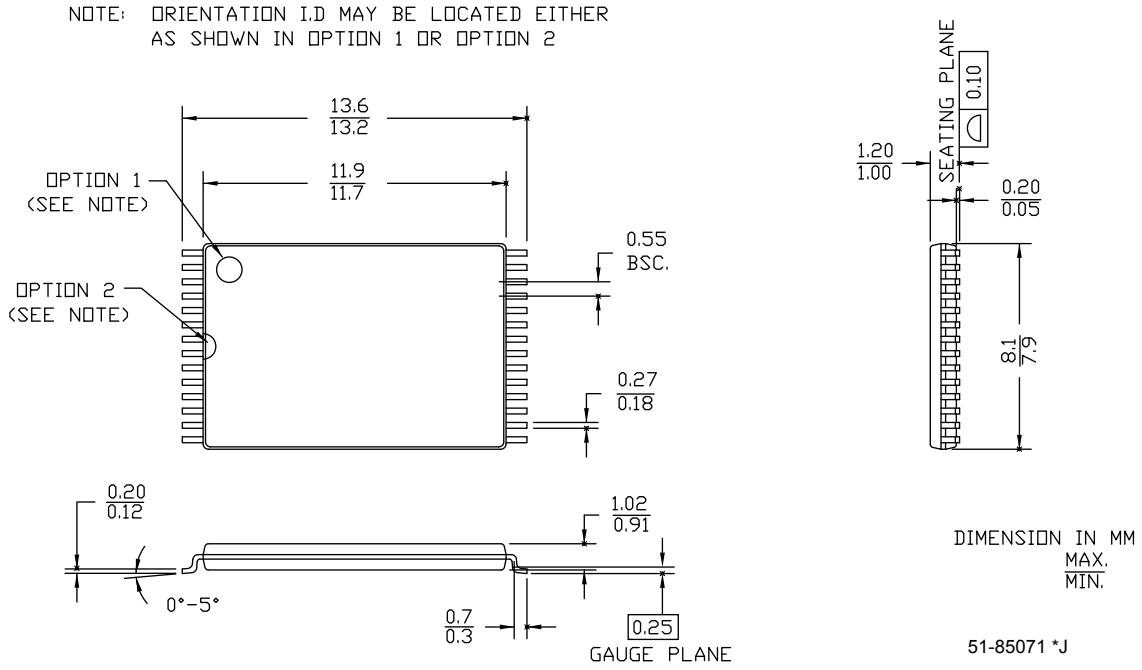
Package Diagrams

Figure 10. 28-pin SOJ (300 Mils) V28.3 (Molded SOJ V21) Package Outline, 51-85031



Package Diagrams (continued)

Figure 11. 28-pin TSOP I (8 × 13.4 × 1.2 mm) Z28 (Standard) Package Outline, 51-85071



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1399BN, 256-Kbit (32 K × 8) Static RAM Document Number: 001-06490				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	423877	NXR	See ECN	New data sheet.
*A	498575	NXR	See ECN	Added Automotive-A range. Removed I_{OS} parameter from DC Electrical Characteristics table. Updated Ordering Information table.
*B	2896382	AJU	03/19/2010	Removed obsolete part numbers from Ordering Information table. Updated package diagrams.
*C	3053362	PRAS	10/08/2010	Removed pruned part numbers CY7C1399BNL-15VXC and CY7C1399BNL-15VXCT. Added Ordering Code Definitions.
*D	3383869	TAVA	09/26/2011	Added Commercial temperature range under Features section on page 1. Removed reference to AN1064-SRAM System Design Guidelines on page 1. Modified the notes in figures under Read cycle and Write cycle sections. Rearranged sections for better clarity. Revised package diagrams. Added Acronyms and Units of measure. Updated template according to current Cypress standards.
*E	4121360	VINI	09/12/2013	Updated in new template. Completing Sunset Review.
*F	4540416	VINI	10/16/2014	Updated Switching Waveforms: Updated Note 18. Updated Package Diagrams: spec 51-85071 – Changed revision from *I to *J. Completing Sunset Review.
*G	4578447	VINI	01/16/2015	Added related documentation hyperlink in page 1. Removed the prune part numbers CY7C1399BN-12VXC and CY7C1399BN-15VXA in Ordering Information. Updated Figure 10 in Package Diagrams (spec 51-85031 *E to *F).

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