9 Function and circuit description, SNA-20/-23

9.1 Description of complete instrument function

In the following description, it is assumed that the Description and Operating Manual has been read and understood. The descriptions refer to the block circuit diagram located in the Annex to this Service Manual.

The descriptions refer to the SNA-23 but may be considered as applying also to the SNA-20, since the instruments are practically identical. The only difference is that the signal path for Bands 1, 2 and 3 is not present in the SNA-20, i.e. the circuits (3) YIG filter control and (4) fundamental mixer are not fitted. The instruments are practically identical for Band 0.

The SNA-20/-23 comprises the following function groups:

- Frequency converter
- IF measurement section
- Synthesizer
- Controller
- AC power supply unit

9.2 Frequency converter, input section BN 2101 (2), (3), (4), (5), (6)

In the input section, the measurement signal at the input socket is converted to an intermediate frequency of 422 MHz (421.99 MHz) by single or double mixing and passed on to the IF modules after amplification (compare block diagram in Appendix).
When the instrument is set to frequencies between 9 kHz and 3.2 GHz (Band 0 operation), the input signal first passes through the step attenuator and is then fed from the coaxial switch (replaced from series C by the diplexer 2DX1) via the 7 GHz coaxial low-pass filter to the Band 0 frequency converter (2) [2101-ZA] (Integration Band 0) microwave module.
The first frequency conversion to the IF (above the Band 0 frequency range) of 4.422 GHz (4.42199 GHz). The heterodyne signal required for this is supplied by the synthesizer OD-11 and fed in via the fundamental mixer module in the input section. The input mixer is protected against impermissibly high RF drive levels by limiter diodes.
The IF signal next passes through a combination of filter and amplifier, which filters out the remains of the carrier signal and unwanted mixer products and amplifies the signal level such that the following second mixer is optimally driven.
This mixer requires a carrier signal with a fixed frequency of 4 GHz in order to convert to the second IF of 422 MHz. The 4 GHz heterodyne signal is generated by locking a voltage-controlled oscillator to harmonics of the 400 MHz reference frequency from synthesizer OD-11.
When the instrument is set to input frequencies from 3.1 to 26.5 GHz (Band 1 to 3 operation), the 422 MHz IF signal is generated from the input signal at the input socket using a different method.
In this case, the coaxial switch (diplexer from series C) feeds the input signal to the YIG filter. The center frequency of this bandpass filter can be tuned in the range 3 to 26.5 GHz (30 GHz) by means of a DC voltage. Controlled from the "YIG filter controller" board, it is synchronized to the actual receive frequency of the instrument and serves to suppress image frequencies, because single conversion directly to the 422 MHz IF is used for bands 1 to 3.
The circuitry required for this frequency conversion is contained in the fundamental mixer microwave module.
A broadband mixer circuit converts the input signal directly to 422 MHz with relatively low losses of about 10 dB. The is fed on the LO side by a carrier signal which has a frequency of one, two or four times the synthesizer frequency, depending on the input frequency range (band). The

output frequency of the YIG oscillator (OD-11) is multiplied for this purpose by a combination of amplifiers, switches and doublers in the fundamental mixer.
The module also provides an output of the simple YIG oscillator frequency for the Band 0 frequency converter (Integration Band 0) module [2101-ZA] and for the back panel socket for connection to a tracking generator or external mixer.
The 422 MHz IF switch module (2) [2101-AQ1] takes the IF signal from the Integration Band 0 module or from the fundamental mixer and equalizes the level differences for the different paths. A third path is provided here for directly feeding in an external measurement signal of 422 MHz (e.g from an external mixer).
The amplified IF signal leaves the input section chassis with a nominal level of approx. -33 dBm (Band 0) and is then fed to the 422 MHz bandpass filter (interdigital filter (6) IF-1) in the "422/ 22 MHz converter" module. The 422 MHz IF signal is converted here to the last IF (21.99 MHz).
The various switching states of the input section modules are controlled by the input section controller board via the peripheral bus (AT CPU). Depending on the different instrument operating modes, the bus information is processed on this circuit board so as to keep the circuitry needed in the microwave modules to the minimum

9.2.1 Input section controller (5) [2101-AR]

The input section controller board is the central supply and control circuit for the input section chassis. The various DC voltages from the AC PSU are fed to the microwave and IF modules via this circuit board, being pre-filtered if necessary. Only the YIG filter controller board is connected directly by its own cable to the AC PSU.
The main task of the "input section controller" is, however, the conditioning of the digital control signals from the peripheral bus for direct control of the microwave components of the input section.
The information is written from the bus data lines (8 bits) to a LSI module (PIO, U11) or written from the PIO to the bus data lines when addresses in the range specified for the input section are also present on the address lines.
The following control functions are realized on the "input section controller" board:

- **PIO Port 0:** Intermediate storage and loop-through of data for the YIG filter controller (3) [2101-AS1] including the associated control logic.
- **PIO Port 1:** Intermediate storage and conditioning of the control signals for band switching (coaxial relay, 422 MHz IF switch, Integration Band 0 module and fundamental mixer) as well as for Signal Identifier operating mode (VCO 400/402 MHz).
- **PIO Port 2:** Intermediate storage of a data word and conversion to a (bipolar) DC voltage for setting the working point of an externally-connected mixer via the 422 MHz IF switch.
- **PIO Port 3:** Intermediate storage of the data word for controlling the step attenuator including level conversion.
- **PIO Port 4:** Transfer of register contents towards the CPU depending on the address, either from the output register of the YIG filter controller or from the error register of the input section controller (which contains information about the operating status of the microwave modules) or from the input section control status register (in which bit 0 indicates error states in the input section).

9.2.2 Frequency converter band 0 (2) [2101-ZA] (Integration Band 0)

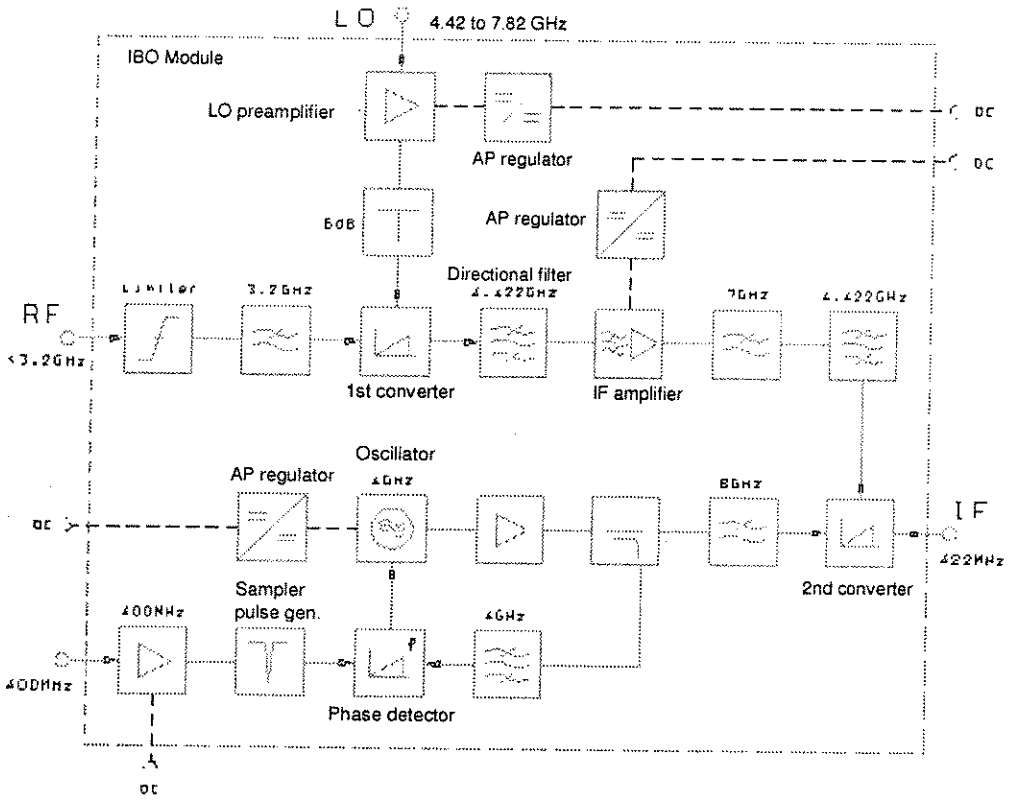

Fig. 9-1 "Frequency converter Band 0" microwave module [2101-ZA] block diagram

A limiter, comprising two PIN diodes connected in antiparallel at the input of the module, protects the first converter from input signals which are too high (max. 1 W RF power). The subsequent low-pass filter suppresses the LO signal and its image frequencies which are travelling back towards the input socket (RF input).
The first converter is a simple push-pull converter which uses the LO signal to convert the input signal to the 1st IF of 4.422 GHz. The subsequent directional filter provides wideband termination for the converter. The input LO signal (4.42 to 7.82 GHz) is amplified to approx. 23 dB by the LO amplifier.
The 1st IF signal is amplified by 16 dB by the two-stage selective IF amplifier and is then fed to a filter combination of a low-pass and a bandpass filter with a bandwidth of b_{5dB} = 3.5%. The subsequent 2nd converter uses a 4 GHz carrier to convert the 1st IF (4.422 GHz) to the 2nd IF (422 MHz) which exits from the module via the IF output. The mixer losses are about 4 dB.
The oscillator (VCO) generates the LO frequency (4 GHz) required for the 2nd conversion. The 4 GHz signal is frequency-locked to a 400 MHz signal derived from the timebase.
The 4 GHz signal is fed to the VCO low-pass filter via the amplifier and the directional coupler. The output power level is 13 to 16 dBm. The VCO low-pass filter (f_g = 8.2 GHz) suppresses the high-frequency components in the carrier which must not get into the second converter.
A 400 MHz signal derived from the timebase is fed into the module, amplified by the driver amplifier and is used to control the pulse sampler. The pulses generated are fed to the sampling mixer which is used as a phase meter. The 4 GHz signal from the oscillator which is coupled out by the directional coupler is fed via the 4 GHz band-pass filter to the phase meter. The mixer

product thus generated in the locked state is a DC voltage which is fed to a PLL integrator. The working point regulators for the amplifier are thick film circuits. They are PI regulators and guarantee that the gates of the RF transistors are negatively-biased in all operating states.

9.2.2.1 Integration Band 0 controller (2) [2101-CF]

The Integration Band 0 controller board performs the following tasks:

- Voltage filter
- PLL integrator and seek circuit
- Band 0 switch-off
- Voltage stabilization
- Working point control
- Error signal generation

Voltage filter

AC voltages which may be superimposed on the ± 12 V supply voltages are removed by the filters L1 through L4, C16 through C19 and C34, C35. Low-frequency interference is filtered out by the components around transistors Q5 or Q8. Transistor Q6 switches the negative supply voltage off if the positive supply voltage fails.

PLL integrator and seek circuit

The phase detector output signal is fed to the board via sockets J1 and J2. This signal contains the phase difference between the 400 MHz signal and the 4 GHz signal and is a DC voltage in the locked state. If not locked, a beat frequency is present at the output of impedance converter U1, which causes the signal comparator U5 to trigger the monostable U6.1 which then supplies an output voltage of 5 V. This causes the seek oscillator U3 to oscillate at f_{osc} = 80 Hz. This generates a sawtooth tuning voltage (J3) for the VCO varactor (VCO TUNING VOLTAGE). R54 is used to adjust the tuning voltage in the locked state.

Band 0 switch off

When the instrument is tuned in the higher receive frequency bands, the 4 GHz carrier must be switched off. The VCO is disabled by a voltage of 0 V at MP10.8, shorting out the VCO oscillator transistor. The VCO settles within approx. 20 ms when switched on again (MP10.8: 5 V).

Voltage stabilization

A stabilized +5 V supply voltage is required for the hybrid working point controller on the module (J6 and J7). This voltage must be controlled so that it is only switched through to the RF circuits when the negative supply voltage (-11.2 V) is present. This protects the RF amplifier (self-conducting FETs) from damage.

Working point controller

The working point controller for the 400 MHz amplifier is made up from operational amplifier U4 and transistor Q4.

Error signal generation

The +5 V supply voltage for the hybrid working point controller is protected using a foldback current limiter. At the same time, the voltage is compared with a reference value. If it is below the reference value, an error signal (MP10.9) is generated and LED DS3 lights up.
If the VCO is not locked, the integrator output voltage U2 tends towards ± 11 V and the window discriminator U7 generates a further error signal (MP10.10) causing LED DS1 to light up.

9.2.3 YIG filter control (3) [2101-AS1]

The YIG filter (FL1) serves as a preselector for bands 1, 2 and 3 at the input of the instrument. The main job of the YIG filter is to suppress image frequencies, harmonic and all interference signals which are not close to the measurement frequency. The YIG filter is a magnetic field-dependent microwave bandpass filter. The filter is tuned using an very precisely controlled current through the COIL connections of the filter (magnetic field).
The YIG filter controller (3) has the task of providing this tuning current for the YIG filter for the entire tuning range (3 to 30 GHz) with the necessary precision. As the relationship between tuning frequency and tuning current is non-linear, the characteristics of each filter must be measured and stored (in Flash EPROMs). The characteristic is then taken into account when controlling the YIG filter during measurement operation.

The YIG filter control comprises several function groups:

- Microcontroller unit (MCU)
- State controller (function decoder)
- Memory (FIFO)
- CPU latch
- Synthesizer latch
- Hardware summing circuit (adder)
- Flash EPROMs
- DAC latch
- Precision reference
- Precision DAC
- V/I converter
- YIG filter heater voltage

Apart from the above function groups, other functions are built in to the YIG filter controller board. To preserve clarity, these are not shown in the simplified block diagram. They include:

- Generation of the Flash EPROM programming voltage
- Temperature sensor
- Supply voltage filters, etc.

The tasks and functions of the individual units are described with the aid of the simplified block diagram (see figure 9-2).

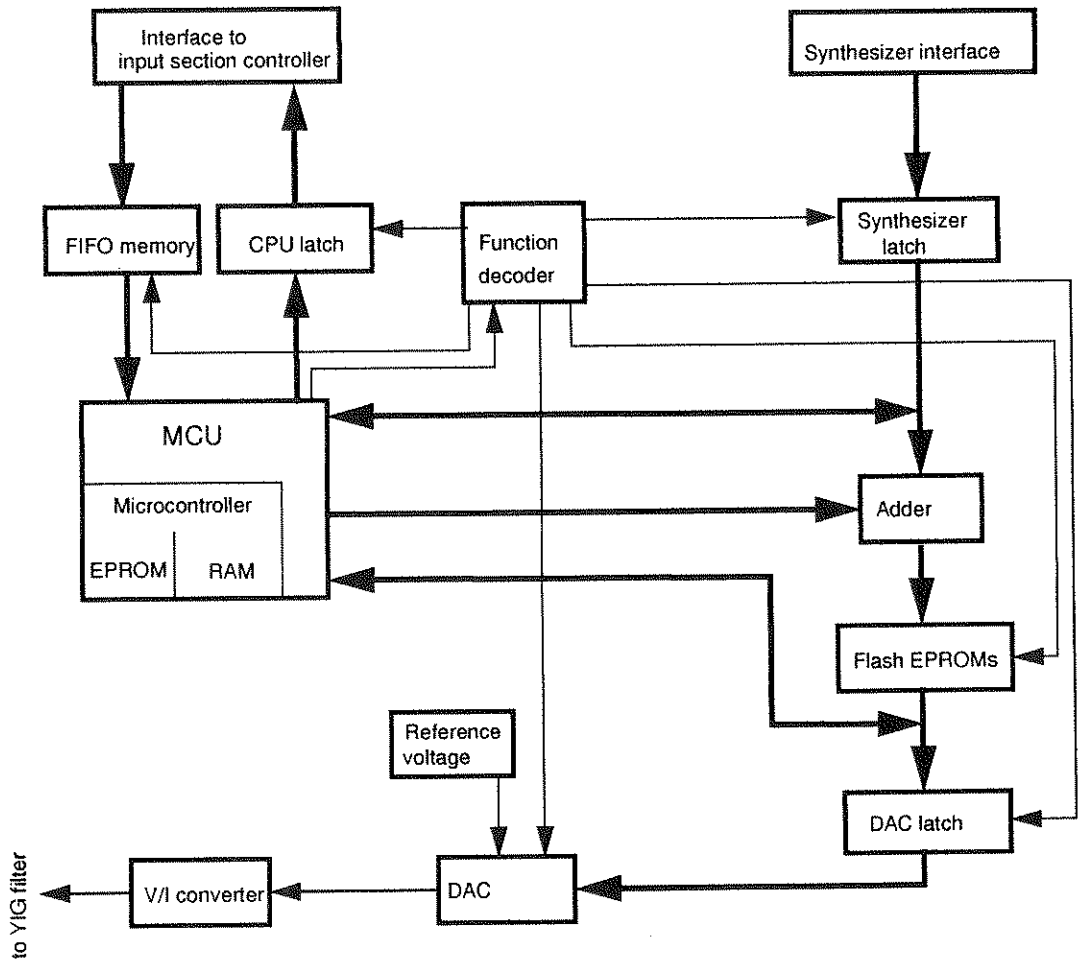

Fig. 9-2 YIG filter controller (3) simplified block diagram

Microcontroller unit (MCU)

The SIEMENS 8-bit microcontroller SAB80C537 (U29) is used. The microcontroller has an external program memory (U27) and external RAM (U31). The MCU independently controls all processes in the YIG filter controller (YFC). For this, it receives commands from the control computer (AT-CPU) which are transferred via the input section controller/FIFO memory. The frequency information is supplied to the MCU by the synthesizer controller (51).

State controller (function decoder)

The state controller manages all path states, i.e. the operating direction of bidirectional buffers, the port enables for the output drivers and the switching of functions (e.g. program voltage to the Flash EPROMs).
The MCU uses 4 control lines to control the states (P0 through P3). Two completely different types of state can be set in this way:

- permanent states (Y0 to 7)
- transition states (Y8 to 15)

All states are indicated by LEDs, so that each change of state can be followed visually (see "Function decoder" circuit in circuit diagrams).

FIFO memory

The data transfer from the control computer (via the input section controller) to the YIG filter controller is processed via the FIFO memory U30. The FIFO memory (U30) is 64 x 9bit deep and is coupled directly to the MCU via port P7. This allows the FIFO to be read in any operational state. The input section controller and the control computer can only detect overflow of the FIFO by monitoring the number of bytes written but not yet acknowledged. Line SI is supplied by the input section controller, i.e. is decoupled from the YIG filter controller logic. This makes the write operation completely independent of the read operation by the YIG filter controller.

CPU latch

The data are passed via (U26) from the YIG filter controller to the control computer (via the input section controller). The data transfer is triggered by state (Y10). The latch enable input is served from the control computer via the input section controller. An automatic lock-up prevents new data from being loaded into the latch when the latch output is enabled (write access lock).
The CPU latch (U26) is written to via the C/F data channel which also transfers the frequency addresses (lower byte) between the MCU and the synthesizer EPROM path. The path to the frequency addresses (FR (15:0)) is disconnected via U16 by (Y2; function decoder) for operation of the CPU latch.
The value on P3.4 (C/F8) is written to the error register (U22.1) at the same time as writing to the CPU latch. The is passed directly to the error interrupt (and linked to other error circuits via the input section controller). This allows fatal errors to be indicated to the control computer.

Synthesizer latch

The data provided by the synthesizer (frequency information) is latched by U1 and U2, i.e. the current frequency of the synthesizer is always available at this point. If, in the meantime, a different value is set on the frequency addresses (FR (15:0)), e.g. by the MCU, or if the YIG filter is disabled in the meantime, the YIG filter can be set to the latest valid frequency value at any time by reading the data from the synthesizer latch. Storage in the latch is triggered by the strobe from the synthesizer, without being affected by the YIG filter controller.

Hardware summing circuit (adder)

Here, offset values are simply added to the frequency word coming from the synthesizer or from the MCU itself. The adder operates purely on a hardware basis without any functional control by the MCU.

Flash EPROMs

The Flash EPROMs store the characteristics of the YIG filter, outputting a corresponding code for every value to which the synthesizer can be set (frequency information). The conversion of this code by the DAC (U42) and subsequent V/I conversion produces the YIG filter setting current. This guarantees that the pass-band of the YIG filter is correctly set for every input frequency (synthesizer frequency).
The hardware required for programming (program voltage generator) is included in the circuit (U39.1, U25.1, Q1). Programming is done by the MCU without removal of the Flash EPROMs.

DAC latch

The output data from the characteristics Flash EPROMs is buffered by latches (U12, U13) and fed from these to the DAC (U42).

Precision reference

The voltage reference is produced using a thermally-controlled regulator diode (U44) and external reference elements. This ensures the excellent thermal stability required for the reference voltage.

Precision DAC

The DAC (U42; AD 7846) used is a 16-bit device with voltage output and high thermal constancy. The excellent thermal stability required for correctly controlling the YIG filter in the entire nominal operating temperature range is achieved in conjunction with the precision reference (reference voltage generator).

V/I converter

The output voltage from the DAC corresponding to the YIG filter characteristic is converted into the corresponding current for controlling the YIG filter (current interface J21; approx. 0 to 1 A).

YIG filter heater voltage

The heater voltage is available from P11, pins P11.1 and P11.3. This is limited to a maximum of approx. 0.5 A by U46 (LM317).

9.2.4 Fundamental mixer (4) [2101-ZC]

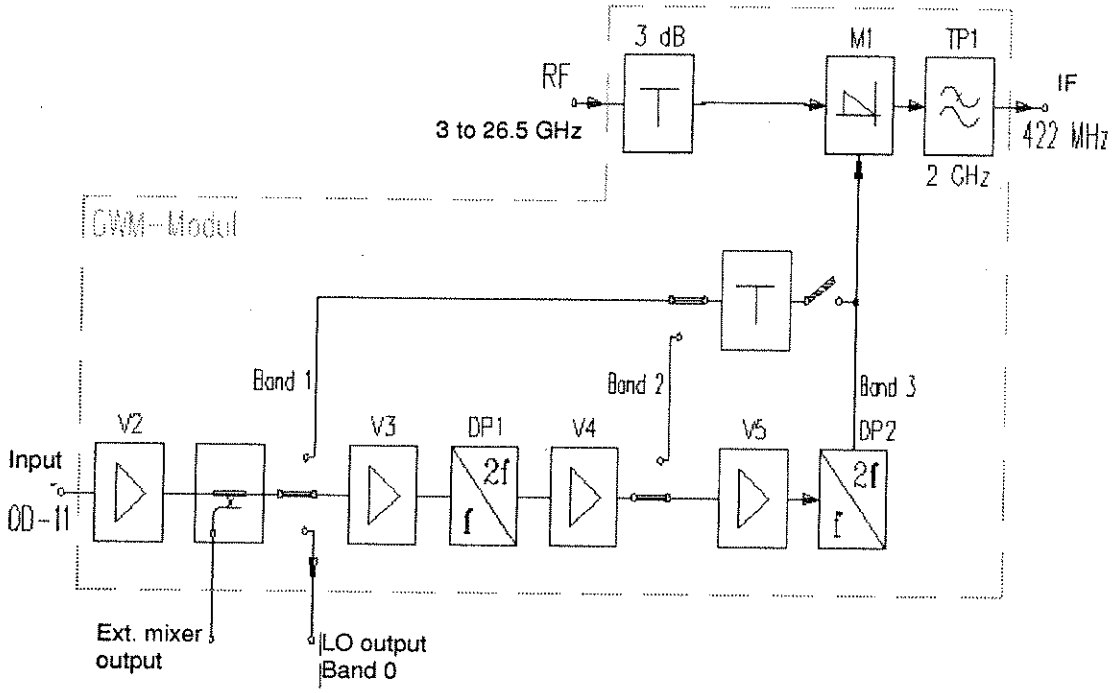

Fig. 9-3 Fundamental mixer [2101-ZC] block diagram

The microwave module contains a mixer stage with low-pass filter and carrier frequency conditioning.
The high frequency RF input signal passes through an attenuator (3 dB) to improve the input reflection coefficient. The push-pull mixer stage M1 is controlled by a carrier spaced at f_{IF} = 422 MHz above the input frequency f_{RF}. This converts the RF signal to a constant, low-frequency IF of422 MHz. A low-pass filter TP1 leads to the module's IF output.
The carrier frequency conditioning raises the synthesizer signal (OD-11) to an approximately constant level and limits it. This signal is then either passed on directly to the mixer stage M1 (Band 1) or multiplied by switching in frequency doubler stages (Band 2 and 3) before it is fed to the mixer stage.
For controlling the separate input section in Band 0, the carrier signal can be switched to an output (LO output Band 0). The carrier signal is also available from a further output as a local oscillator for control of an external mixer.

9.2.4.1 Fundamental mixer controller (4) [2101-AV1]

The fundamental mixer controller performs the following tasks:

- Voltage stabilization
- Error signal generation
- Working point regulation
- Band switching

Voltage stabilization

Several voltage stabilizer circuits are fitted to this board.
Voltages of +10 V and -10 V are also generated for the band switching.

Error signal generation

The +5 V voltage is protected using a foldback current limiter. At the same time, the voltage is compared with a reference value. If it is below the reference value, an error signal is generated at MP2.4 (open collector).

Working point regulators

The working point regulators for amplifiers V2 and V3 are thick-film modules in the RF circuits. The circuits guarantee that the gates of the RF transistors are negatively-biased in all operating states.

Band switching

The band information is available as a 2-bit data word at MP 2.1 and MP 2.2. Control voltages for the microwave switch (LO multiplier switching) in the fundamental mixer are generated from this data word.

9.2.5 422 MHz IF switch (2) [2101-AQ1]

Various IF paths are switched through the "422 MHz IF switch" module depending on the input frequency of the spectrum analyzer (9 kHz to 3.2 GHz, Band 0; 3.1 to 26.5 GHz (30 GHz), Band 1 to 3; external 422 MHz input) (see circuit diagrams and block diagram).
The input signals for the IF switch are the 422 MHz IF output signals from the "Integration Band 0" [2101-ZA] and "Fundamental mixer" [2101-ZC] microwave modules, together with a third input for directly inputting a signal of frequency 422 MHz.
The IF switch thus corresponds in function to a 3-way single-pole signal source switch. The output signal is fed to the "422/22 MHz converter" board via the 422 MHz interdigital bandpass filter.

The three input signals (Band 0; Band 1 to 3; external 422 MHz input) have different levels. The various signal paths therefore include amplifiers and attenuators to set the overall gain to give approximately the same output level, regardless of operating mode.

Control and power supply are from the input section controller (5) [2101-AR]. The lines "Band 0" and "external" control four CMOS switches in the IF switch, which in turn control current sources for PIN diode switches.
A third control line allows a digitally-controlled current to be fed into the modules connected to the "422 MHz external" input socket of the IF switch to allow e.g. the diode working point of an external mixer to be optimized.

9.2.6 422 MHz/22 MHz converter (6) [2101-X]

The 422 MHz/22 MHz converter converts the IF signal from 421.99 MHz to 21.99 MHz. It contains the following components:

- 422 MHz bandpass filter
- 400 MHz carrier generator
- 422 MHz/22 MHz converter
- Power supply

422 MHz bandpass filter IF-1

The 422 MHz bandpass filter, IF-1, suppresses the image receive point of the 422 MHz/22 MHz converter and unwanted products from the previous conversion. At the same time, it provides the 10 MHz resolution bandwidth (RBW).
The 422 MHz bandpass filter is an interdigital filter with capacitive truncated resonator.

400 MHz carrier generator

The 400 MHz carrier generator supplies the 400 MHz carrier for the 422 MHz/22 MHz converter. The carrier generator consists of a VCO, a switchable frequency divider and a phase-locked loop.

VCO

The VCO consists of active elements T 10 and T 11. A strip circuit serves as resonator; this is electrically expanded by the series circuit comprising C 66 and the varicap diodes GL 3 through GL 5. The signal is coupled out to the mixer via T 8 and T 9 and further to the frequency divider via T 5.

Frequency divider

The frequency divider divides the VCO frequency by 40 or 40.2. It comprises IC4.2, IC6 and the switchable 40/41:1 divider IC7.

Phase-locked loop

The PLL locks the VCO frequency to a 20 MHz reference frequency. It consists of a phase meter and a control amplifier. The phase meter IC3, IC4.1 compares the divided VCO frequency with the 20 MHz reference frequency divided by 2.
The output signals of the phase meter are each integrated by a RC low-pass filter and fed to a control amplifier, IC5. This sets the working point for the VCO varicap diodes.

422 MHz/22 MHz converter

The 422 MHz/22 MHz converter converts the IF Signal from 421.99 MHz to 21.99 MHz. It comprises input amplifier IC13, ring mixer IC9, and 22 MHz amplifier IC8, each of which is decoupled from the other by attenuators, and carrier amplifier T 12. Amplifier IC15 is for adjusting the input section gain and compensates for the thermal drift of the input section.

Power supply

The power supply provides +10.5 V, -10 V and +5.2 V for the circuit.

9.3 IF measurement section (7), (8), (9), (10), (11)

The IF measurement section contains the following modules:

- IF selection (7) [2101-L], [2101-R], [2101-S]
- Logarithmizer (8) [2101-M], [2101-Q]
- IF converter (9) [2101-O]
- Calibration generator (11) [2101-N]
- measurement section controller (10) [2101-P]

The IF measurement section evaluates the input signal after conversion to the last IF (21.99 MHz).

IF selection and logarithmizer board

Firstly, the signal is filtered to the required resolution bandwidth and the input level is matched to the logarithmizer and AD converter section (IF filter and IF amplifier on the IF selection board). The signal is then logarithmized. The rectifier is integrated into the logarithmizer, i.e. an AC voltage is present at the input to the logarithmizer and the video signal, which is a DC voltage proportional to the logarithm of the input amplitude, is present at the output.

The logarithmizer also has an AC output (with virtually constant amplitude) which is required for the FM and search demodulators.

Calibration generator board

The FM demodulator can demodulate a frequency modulated input signal and output this as an audio signal to loudspeaker or headphones. The search demodulator can be used to audibly detect signals which are swamped by noise.

When AM signals are present, the video signal is the demodulated signal; this can be switched directly to the loudspeaker or headphones. The demodulators are on the calibration generator board.
A further function of the calibration generator is to generate the internal and external calibration levels. The calibration generator is a synthesizer, tunable from 17 to 27 MHz, having an extremely accurate output level over the entire frequency range. The signal can be switched to the IF selection input for calibration purposes. It is also available from a socket on the front panel to permit external calibration.
The calibration generator board also includes the power supply connection for the entire IF measurement section module.

IF converter board

The video signal now passes through a low-pass filter, the limit frequency of which is variable; this is the video filter. This has the task of attenuating the rectifier ripple and, where required, averaging the display (e.g. for noise signals).

An r.m.s. value generator can be connected in front of the video filter, to produce the real r.m.s. value of a mixed signal. After the video filter follow the two ADCs, one a fast 8-bit converter with a sampling rate of 20 MHz (a 10-bit converter is used from series C onwards) and one slow 16-bit converter running at 40 kHz. They convert in parallel. The 8-bit converter handles fast events, such as pulse measurements or measurements using fast sweep times in zero span mode. The slow, high-resolution converter is for the 'normal' measurements.

Measurement section controller board

The selection from the mass of converted values and their compression into a measurement value is the job of gate array 1. It supports the DSP in the further processing of the data.

Gate array 2 contains a 32-bit frequency counter, to which various signal sources can be connected. For example, the IF can be precisely counted and the input frequency exactly determined. Gate array 2 also contains the trigger generator. This allows complex trigger conditions to be set and processed for zero span operation.

The measurement section controller board also includes the address logic and the clock conditioning for the entire module.

A further part of the IF measurement section is the calibration generator. This is a synthesizer, tunable from 17 to 27 MHz, having an extremely accurate output level over the entire frequency range. The signal can be switched to the IF selection input for calibration purposes. It is also available from a socket on the front panel to permit external calibration (calibration generator board).

The calibration generator board also includes the power supply connection for the entire IF measurement section module.

9.3.1 IF selection (7) [2101-L]

Bu1 carries the measurement signal, Bu2 the calibration signal (internal calibration, -30 dBm). The switching between the two signals is by means of relay Rel1. The unused signal path is shorted to ground through diodes Gl2 or Gl3. For high measurement signal levels, (>-10 dBm) there is a 14 dB attenuator, comprising R43, R44, R45 and R52. This is switched in by relay Rel2.
The 3rd order high-pass filter comprising C14, C23 and L6, shapes the 10 MHz bandwidth of the bypass path and prevents overdriving the preamplifier stages with 7 MHz signal components.
After the high-pass filter, there is a 12 dB wideband amplifier (Z_0 = 50 Ω). This consists of T2 and UE1, the gain being determined by the transformer ratio of UE1. After this, amplifier stage V1 amplifies the signal by a quasi-continuous (256 bit) factor of 0 to +6 dB. The gain depends on the control current through the PIN diodes Gl4 [2101-L] and Gl61 [2101-S], and the size of the control current depends on the data word at the input of DAC IC11. If link Br17.1-18 is closed, the maximum gain of V1 = V_{max} = 6 dB (approx.), if link 17 is removed, the gain is V = 0 dB. In measurement mode, Br17.1-17.2 is closed.
The signal can be passed into one of the three possible paths with the aid of the multiplexer IC1.1, IC2, IC6 or IC7.

- Bypass path, with a bandwidth of more than 10 MHz
- LC filter path, bandwidths 3 MHz to 100 kHz
- Crystal filter path, bandwidths 30 kHz to 1 kHz.

The signal collected by IC2 is passed to the input of the first (V2) of four wideband amplifiers (amplifier stages V2, V3, V4, V5).
The overall gain can be set in 1 dB steps in a range covering 61 dB.

The center-band frequency of the selection paths is 21.99 MHz.

The quasi-continuous (255 bit) alteration of the bandwidths is achieved with the aid of PIN diodes which have the function of a controllable damping resistor for the LC or crystal filter circuits. The control current through the PIN diodes is derived from the data word at the input of the DAC IC12.

S1 is only operated for adjusting the LC bandpass filters or for troubleshooting. The operational position is all switches set to "off".

The band center frequency of the LC circuits is pulled back to F = 21.99 MHz if drift occurs within about ± 100 kHz. Varicap diodes (GI82) on the LC bandpass filter board [2101-R] are used for this. The pulling voltage is generated in the DAC IC12 and can be checked at wire link BR15.1.

The thermal variation in the insertion loss of the LC circuits is compensated approximately by making the degree of positive feedback temperature dependent using R97 (NTC).

The signal selected by IC7 is fed to the output amplifier (IC19). The gain is +12 dB.

At the output of IC19 the signal branches to Bu3, TP14 and to Bu4 or Bu10 [60] (IF output) on the instrument back panel via T 303.

The input of the logarithmizers is connected to Bu3. The nominal level (calibration) at this point is +12 dBm or +3 dB or 1.5 V_{pk}. A voltage divider with a = 23 dB and Ri = 50 Ω is connected to the output of T303, so that the nominal level (calibration) at Bu4 is -20 dB.

Level detectors are directly connected to the input and output of the IF selection (T3,4,5 and GL6 with TP2 or GL300). Detection of the presence of the calibration level takes place in the comparator pair IC10. If the calibration level is present, TP20 or TP21 are "LOW".

GL103 is a 6.4 V voltage reference element. IC5 and T102 generate a working point of approx. -7.8 V referred to the +5 V supply voltage for the multiplexer IC3 and IC4. This voltage can also be measured at TP10. This ensures that the gain of the amplifier stages V2, V3, V4 and V5 is independent of variations in the +5 V supply voltage. To compensate for the thermal effects, NTC resistor R136 is inserted in the feedback path to IC5.1.
A -10 V reference voltage is present at TP15. This is generated by inversion of +10 V at GL400 by IC9.1 and T401 (reference voltage for DAC IC12). All current sources (gain V1, bandwidths in LC and crystal paths) are referred to this reference voltage.

Link BR15 is closed for normal operation. For adjusting the LC bandpass filters, an average control voltage of +5 V can be fed to the varicap diodes GI82 [2101-R] by closing the link BR15.2-16.

The LC circuits can be trimmed by ± 100 kHz (at least ± 75 kHz) with control voltages in the range +(2.5 to 10 V) and thus held to the band center frequency (21.99 MHz) to compensate for thermal drift or aging.

The addresses IF A1, IF A2, IF A3, IF A4, BGS IF SEL, the control data IF D0 to IF D7 and the +12 V, -12 V supply voltages are fed, preselected, from the "measurement section controller" board and are fed onto the "IF selection" board [2101-L] via plug St1.

HIGH level at BGS IF SEL activates the IF selection board for accepting addresses and data. The addresses are used to select operations, e.g. "fine level setting", "select filter type", "IF gain", "DAC register" and "update". The data (IF D0 to IF D7) indicate the value to be set.

9.3.2 Logarithmizer (8) [2101-M]

The simplified block diagram (see figure 9-4 on page 9-15) shows the interworking of the various function blocks. The logarithmizer basically consists of a chain of 10 amplifier stages, each with 10 dB gain, with a rectifier connected to each of their outputs. The rectifiers must all have the same characteristic which must also have a defined lower threshold (i.e. a response threshold for low levels) and an upper saturation limit for large levels. The rectifier outputs supply a current to the input of the adder stage. The sum current is a direct measure of the logarithm of the level at the input of the amplifier chain. After passing through a video low-pass filter with an upper limit frequency of 10 MHz, the signal is amplified to the required level by the output amplifier. The output of this amplifier feeds the output sockets to the ADC and, via an RC high-pass filter on the calibration generator board, to the demodulator.

At the input of the logarithmizer, there is first a 10 MHz bandpass filter with a center frequency of 22 MHz. The filter function requires an input source impedance of 50 Ω. The filter is unbalanced in order to compensate for the rectifier frequency response. A balun is connected to the filter, followed by a 0 dB buffer amplifier/impedance converter. The first 10 dB amplifier and rectifier are connected to the output of this buffer amplifier.

The noise filter is connected between the sixth and seventh 10 dB amplifier stages. The bandwidth of this filter can be switched in up to 4 steps. The filter band limits the wideband noise which is generated and amplified by the preceding stages.
This prevents the last four amplifier or rectifier stages from being saturated by wideband noise when narrow resolution bandwidths are set in the selection section. The bandwidth of the noise filter must, however, be matched to the resolution bandwidth (see table 9-1). A calibration facility must also be used to ensure that the center frequency is exactly 21.99 MHz and that the insertion loss of the filter is 0 dB.

Noise bandwidth	Use for resolution bandwidth (RBW)
> 10 MHz (bypass path)	≥ 1 MHz
1 MHz	300 kHz
400 kHz	1 kHz to 100 kHz
170 kHz	not used in SNA

Table 9-1 Relationship between noise filter bandwidth setting and selected resolution bandwidth (RBW)

For linear rectification, one of the total of 11 rectifier stages can be selected (i.e. the other 10 are disabled). For linear rectification, the lower response threshold of the rectifier is reduced and the gain of the output amplifier increased.

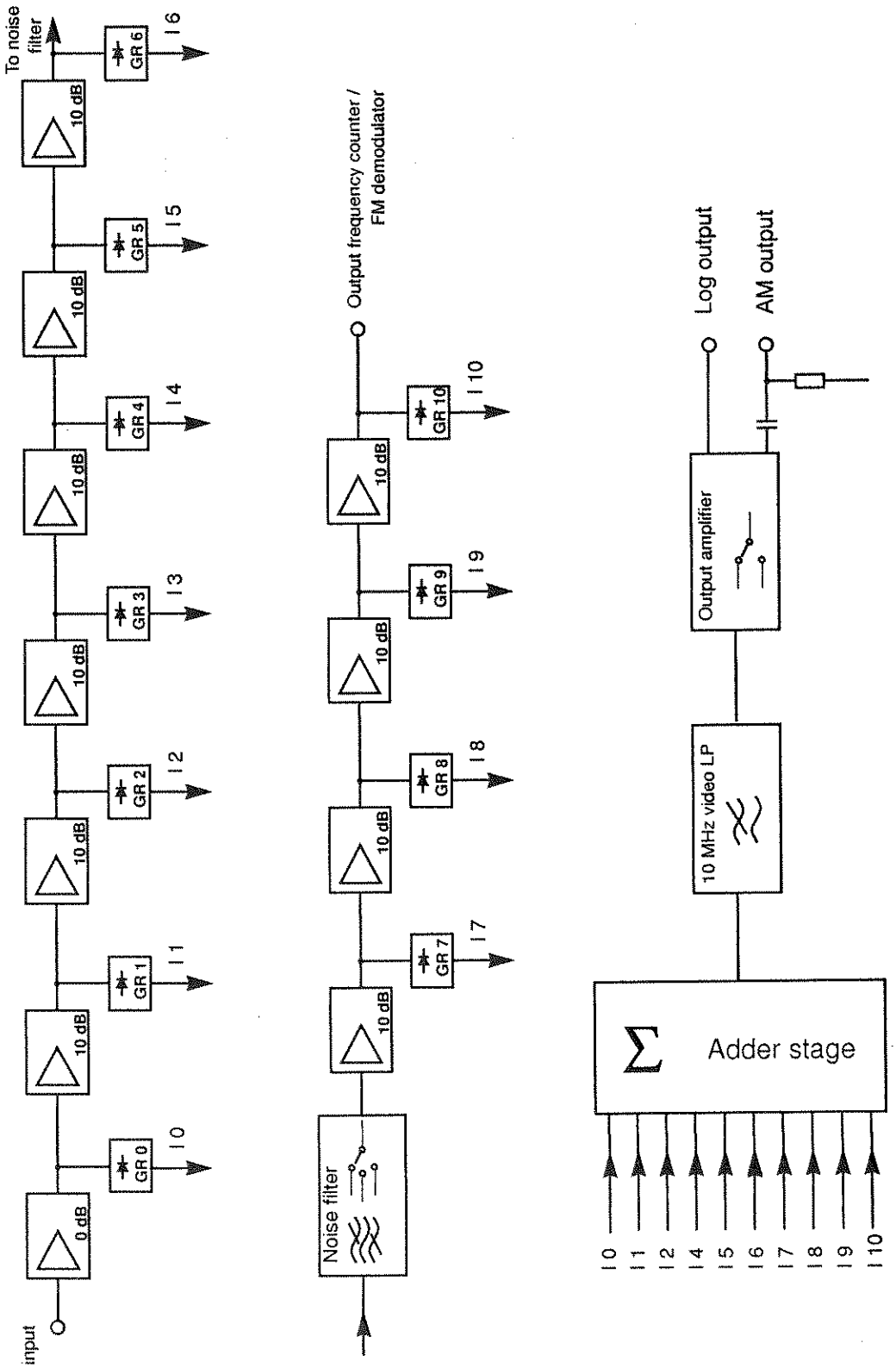

Fig. 9-4 Simplified block diagram of the logarithmizer (8)

The 10 dB log stages

The balanced layout of the 10 dB log stages (8) [2101-Q] is shown in the circuit diagram. The transistors T152 and T153 supply the gain and work in push-pull. They are coupled by the common emitter current source comprising T151 and emitter resistor R151. The coarse gain is determined by the ratio of the emitter resistors R155 and R156 to the collector resistors R158 and R161. P151 allows fine adjustment of the gain. R157 and C158 provide frequency response correction. Transistors T154 and T155 are connected as emitter follower and act as buffer stages for low-impedance drive of the rectifier and the subsequent amplifier stages.

The rectifier circuit is shown separately in figure 9-5 on page 9-16. L1, L2, R5 and R6 form two current sources together with the -10.9 V voltage source. In the idle state, their current flows through the diodes D1 and D2, via resistors R1und R2 and the balun to the rectifier voltage source (approx -5.1 V). If a signal of sufficient amplitude is supplied from the previous stage, the current is divided between the resistor pairs R1/R2 and R3/R4 with increasing amplitude. This leads to a signal current on the collective line (X). The maximum signal current (saturation state) is reached when half of the saturation current of each current source flows on the collective line. The bias voltage of the collective current line can be altered for linear rectification such that a small idle current flows on the line (switched on the main board [2101-M]). The field effect transistors for disabling the rectifiers are also located on the main board.

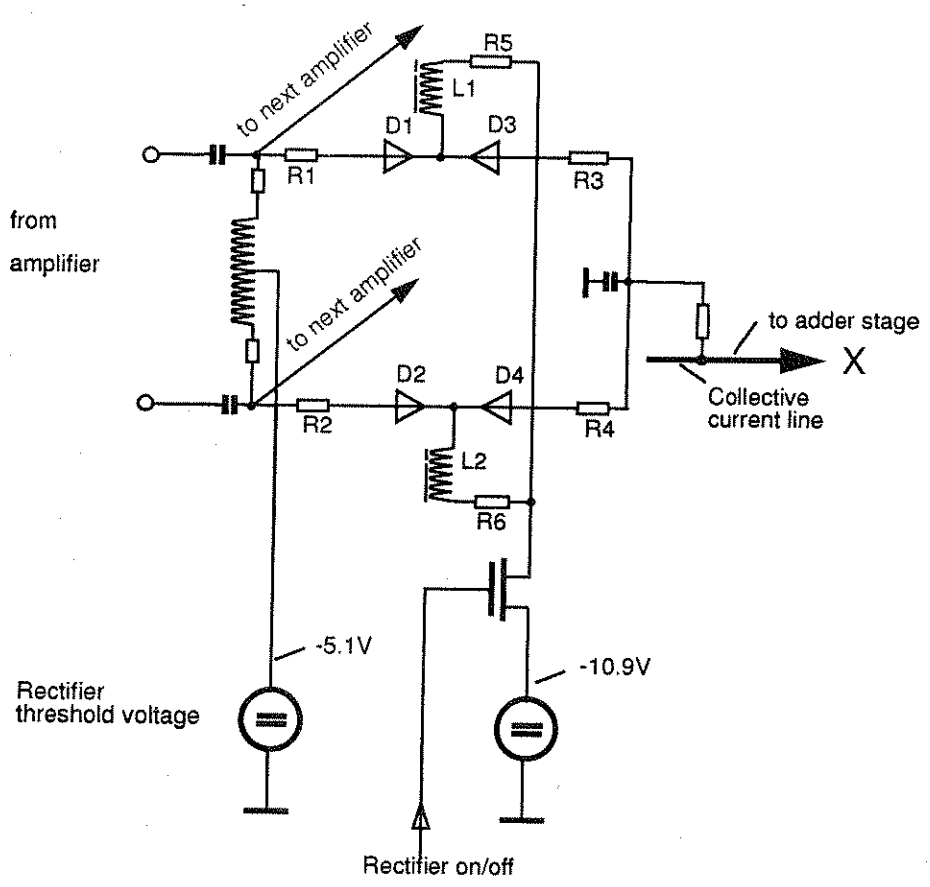

Fig. 9-5 Rectifier stage circuit diagram

The noise filter

The transistors T200 to T203 are connected as a balanced buffer with 0 dB gain. The outputs pass via two decoupling capacitors and a balun to the filter and a bypass path.
The bypass path serves for transmitting the wideband signals (1 to 10 MHz). The bypass path components form a bandpass filter with a bandwidth of >10 MHz. The signal is passed on to the buffer amplifier IC21 and IC22 via analog switch IC20 and on to the next log stage.
The actual filter comprises a deattenuated LC circuit, several resistors for fixing the bandwidths and several control elements. The LC circuit comprises L208, C215 to C218 and varicap diodes GL204 to GL207. The varicap diodes allow the center frequency to be set by a computer via a DAC.
The deattenuation is realized by analog switch IC20, buffer amplifiers IC21, IC22, diodes GL208/GL209 and R230/R231. The DC through the PIN diodes (GL208, GL209) can be varied using a DAC, so allowing the degree of positive feedback to be changed. In this way, the gain of the noise filter is set to 0 dB by the computer. The control current for the PIN diodes is fed in via resistors R227 and R228.
The narrowest bandwidth of about 400 kHz is set by R215 and R216. They are in series with the output impedance of the preceding buffer amplifier and damp the LC circuit. The PIN diodes GL200 to GL203 can be switched to low impedance via the control lines P (400 kHz NBW) and O (1 MHz NBW), the damping of the LC circuit being further increased through the resistors R213 and R218 or R218 and R219.
The analog switch selects between the bypass and the filter path via control line N (10 MHz NBW).

Adder circuit and video filter/amplifier

The rectifier currents are collected together on the collective current line (X) to form a sum signal. To eliminate feedback, the bias voltage on the collective line must be kept constant (Z = 0 Ω). This is achieved by the adder circuit.
The collective line is fed into the inverting input of the OP IC40.2. This is held to the same bias voltage as the non-inverting input by feedback (T400). When "Log scale" is selected, this voltage is about -6.0 V; for linear scale, it is approx. -5.5 V. The current is available from high impedance at the collector of T400, and is passed on to the finite input impedance of the 10 MHz video filter. To ensure the function for frequencies up to 10 MHz, T400 takes up the higher frequency signals in common base mode. The base impedance is reduced for this by C403 and R406. Additionally, an idle current is forced on the emitter of the transistor to ensure correct function of the circuit at low input signal levels. The double transistor T401 serves as current source for this. The second transistor generates an identical current which is subtracted from the signal current again via IC40.1 to restore the correct zero point. T402 and T403 (FET) switch the gain, the additional elements being required for gain-independent frequency response.

Threshold and bias voltage generators

All important voltages are based on the same reference, the Zener diode GL500. One rectifier threshold voltage (-5 VT) is derived directly from this reference via buffer stage IC51.2/T503. IC50.2 forms a current source with T502 and R514, P501 being used to set the current. This current produces a voltage drop across R516 and GL506 which is added to the reference voltage at the output of IC50.1. This voltage is used as the bias voltage via the adder for the collective current line in the "Logarithmic" setting. For the "Linear" setting, the bias voltage is switched to a value between the threshold voltage and the "Log" bias voltage using analog switch IC60.1. This intermediate voltage is set by P502. The -10.9 V for the rectifier current sources are generated in a similar way. They are based on the "Log" bias voltage. IC50.1 with T500 and R500 are used as current source. This current produces a voltage drop across R506 which is added to the above-mentioned bias voltage and the threshold voltages of diodes GL507 and GL508 which provide thermal compensation.

The working point setting (i.e. generation of the base voltages for the current source transistors in the 10 dB log stages) is referred to the -12 V supply. The base voltage is around 4 V higher than the -12 V supply.

9.3.3 IF converter (9) [2101-O]

The following functions are implemented on the IF converter board [2101-O]:

- Video filter
- 8-bit ADC (10-bit from series C)
- 16-bit ADC
- Multiplexers for gate time, frequency counter and trigger conditions for the 16-bit ADC
- RMS detector

Video filter

The first main part of the module is the video filter (resistors and capacitors between IC2 and IC7). These are simple RC lowpass filters, switchable in decade steps of in 3, 10, 30 from 3 Hz to 3 MHz. There is also a wideband path for the 10 MHz video bandwidth.
At the input of the video filter is a multiplexer (IC2) which switches the following signals to the video filter:

- the video signal; voltage range 0 to 5 V
- an external signal fed in to BU2 (y external)
  Voltage range: 0 to 1V (Gate of T304 HIGH)
  -0.5 to +0.5 V (Gate of T304 LOW)
- signal from r.m.s. rectifier; 0 to 5 V

The multiplexer IC7 together with the transistors T100 to T105 serves for selecting the video bandwidths.

8-bit and 16-bit ADCs

The signal is fed to the fast 8-bit ADC (IC16) via a buffer stage (IC13) and matching amplifier with subsequent driver (IC14 and T301). The output data from the ADC are fed via a latch (IC17) to the plug to the measurement section controller (ST1).
The same signal as is fed to the fast 8-bit ADC is also fed to the 16-bit ADC (IC20) via another matching amplifier (IC18). The data from this converter are read out serially and converted into a parallel 16-bit word by shift registers (IC21 and 22); this is also fed to the plug to the measurement section controller (ST1).
Latch IC24 is used to set the status word of the converter.
The reference voltages for the converters are derived from the reference voltage source IC11. IC12 and T300 generate -2 V for then 8-bit converter; IC19 generates +5 V for the 16-bit converter.
T304 (on IC11) can be used to insert an offset of half the screen area into the signal path. This allows a signal balanced about earth to be fed into the y external input.

Multiplexers for gate time, frequency counter and trigger conditions

The multiplexers for gate time, trigger and frequency counter functions (IC27, 28 and 29) are fitted on this board. The multiplexers are used to switch between the different input signals. IC25 is a comparator which triggers when the video signal exceeds a threshold which can be set via the DAC (IC26).

RMS detector

The rms detector is also on this board (IC8, 9, 10, 15 and 33)
The signal from the logarithmizer (video signal) is divided (R207-R210, R221), buffered (IC9) and antilogged by IC33.1. It is then averaged by R205 and C202 and fed via current mirror (IC8.1 with R203 and T202 with R204) to transistor IC33.4 where it is re-logarithmized. It is then coupled out via IC8.2 and amplified to correspond with the input attenuation.

9.3.4 Calibration generator (11)[2101-N]

Two completely separate function units are realized on the calibration generator board:

- Calibration synthesizer with level regulation
- Demodulators (FM, AM and search demodulator) with loudspeaker output stage

9.3.4.1 Calibration synthesizer with level regulation

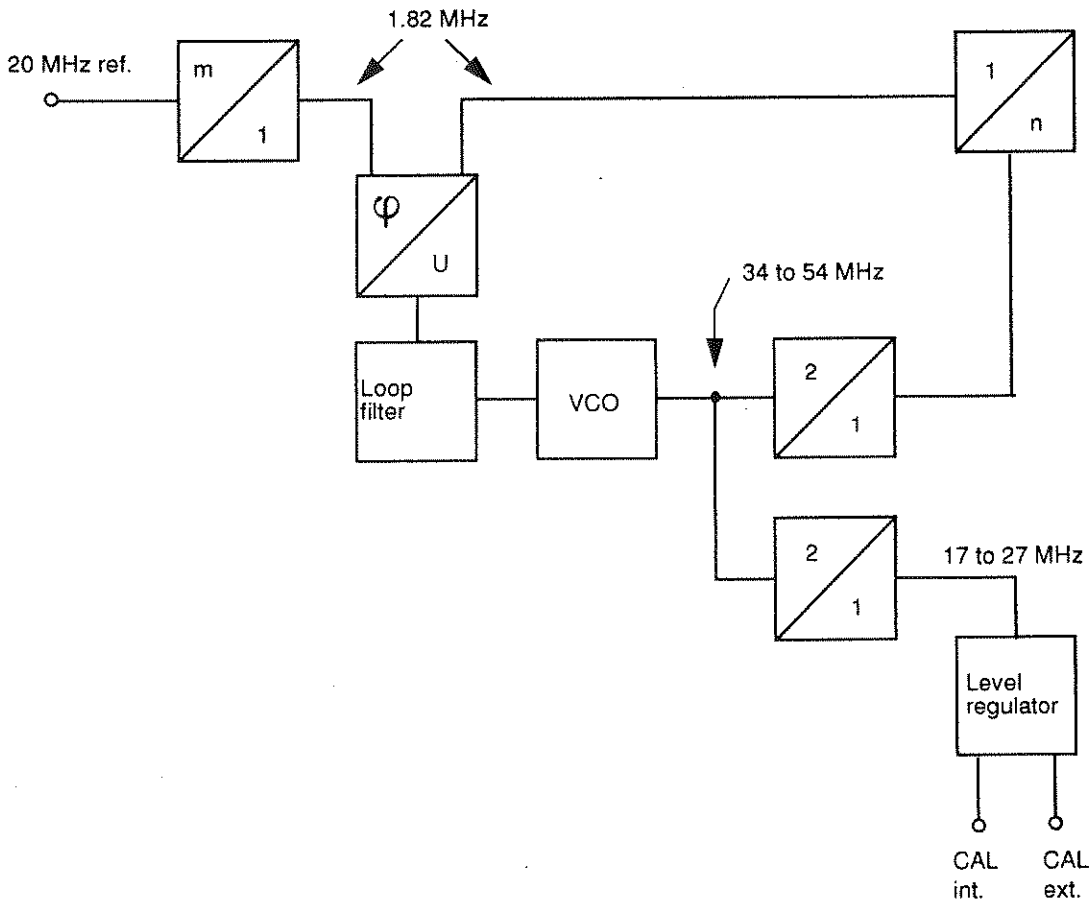

Fig. 9-6 Simplified block diagram of the calibration synthesizer

Synthesizer

The m/1 divider (IC6 and IC7) is normally set to m = 11 but can be set by software to other values.
The phase meter (IC2, IC3 and IC4) basically comprises an up/down counter (IC4) which counts back and forth between states 1 and 2 when locked. In the unlocked state, the counter either remains in state 0 (VCO frequency too high) or in state 3 (VCO frequency too low) until the control loop locks again.
The loop filter comprises IC1, R100-R109, C100-C108. The VCO comes next. It operates in the frequency range 34 to 54 MHz. It can be disabled via GL101.
IC10 forms the two 2/1 dividers. The n/1 divider is formed from the programmable divider PLLIA (IC8), together with IC9 for synchronization. The value of n for the PLLIA - and hence the output frequency - is set via the data lines IF D(0) to IF D(7) by the measurement section controller [2101-P]. The selection of the calibration generator module [2101-N] is via the address lines IF A1 to IF A4.
The IDBY(7:0) of the PLLIA are status bits which can be read by the main processor.

Level regulator

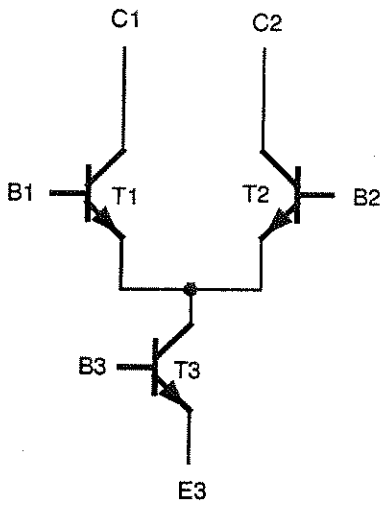

Fig. 9-7 Basic circuit, IC20.1, IC20.2

IC20 consists of two differential stages with current source transistors (see figure 9-7). The differential stages are connected as squarewave generators. Square waves with a duty cycle of exactly 1:1 are present at IC20.11 and 12. The current I in the second stage is controlled by keeping the voltage across R228 constant (IC21 forms an integrator with R242 and C213). The square wave drive causes T1 and T2 to pas the complete current I alternately. The output amplitudes at Bu2 and Bu3 are thus only dependent on the (controlled) current I and the collector resistances. Current I can be set with P2. P1 sets the level of the CAL EXT output separately.

9.3.4.2 Demodulators and output amplifier

FM demodulator

The FM demodulator is made up from IC31 and the resonant circuit formed by UE2 and C317/ C318. IC31 contains an active demodulator, on to one input (Pin1 and 4) of which the input signal (balanced by UE3) is passed. The other input (Pin8 and 10) is connected to the resonant circuit UE2 and C317/C318. This is coupled to the input signal via C319 and C320 and adjusted to the center frequency (21.99 MHz) by C317. For frequencies other than the center frequency, a phase offset is produced between the input signal and the resonant circuit which is proportional to the frequency difference; causing a change in DC voltage at the output (Pin 12).

Search demodulator

The search demodulator has the task of rendering audible weak signals which are practically swamped by noise. It comprises IC30, the demodulator, and Q1 with C300, C302 and C303, the oscillator. The signal is input to one input of the demodulator (Pin8); the other (Pin1 and 4) is connected to the oscillator which runs at 21.99 MHz. The difference frequency appears at IC30.12. If the search demodulator is not selected, the oscillator is disabled via IC32.

AM demodulator

The video signal of the logarithmizer is the AM demodulated signal. It is output directly to the output amplifier via the multiplexer IC32.

Output amplifier

The headphone output has two identical channels (IC36.1 and 36.2) for stereo headphones. The volume is set via IC34. The loudspeaker output volume is also set via IC34.

The computer warning beep is output to the SNA loudspeaker via the beep circuit. Loud and soft can be selected with T300.

9.3.5 Measurement section controller (10) [2101-P]

The function of the measurement section controller is basically to process the analog levels measured by the IF measurement section digitally in such a way that they can be displayed on the screen by the graphics processor. Calculations such as frequency response and level correction are included in the function. This module also includes the complete trigger circuitry for the instrument and the facilities for frequency measurement.

In "Spectrum analysis" mode, the entire SWEEP is split into max. 4000 equidistant measurement intervals. The IF level values sampled by the two ADCs in one interval are processed by a gate array (IC44) so that the characteristic data such as MINIMUM, MAXIMUM, etc. for the measurement interval are made available to a digital signal processor (DSP). The collection of measurement values is controlled by the synthesizer via a port reserved for this purpose, so that the sampled values can be correctly assigned to their corresponding frequency settings. The signal processor (DSP) stores these (4000) pairs of values processed by the gate array in memory. After appropriate further processing, the measurement data are compressed to 500 pairs of values and read by the graphics processor via a port and displayed on the screen. The collection and storage of 4000 values has the advantage that the trace can be expanded (zoomed) by up to a factor of 8 after the measurement.
As well as the above-mentioned MINIMUM and MAXIMUM values, the gate array also provides the information required for realizing e.g. the "AVERAGE FUNCTION", which is also calculated by the DSP.
The measurement is started with a trigger signal which is generated by gate array 2 (IC46).

The array IC44 is configured and "operated" via the signal processor, which in turn is in direct communication with the main processor. In contrast, the trigger array IC46 is controlled directly by the AT CPU via an 8-bit wide data bus.
The trigger array gets the signal from the 8-bit ADC. Various conditions can be set via the main processor for generating and outputting a trigger signal. The further processing of this trigger signal depends on the operating mode and the instrument settings. This signal can be used to start a measurement or to synchronize an external test instrument as the trigger signal is also output to the ext. trigger connection.
As well as the trigger circuits, this gate array also contains a 32-bit wide frequency counter which can make frequency measurements with fixed gate times and period duration measurements over a selectable (limited range) of periods. It is also possible to control the gate time externally and subsequently calculate the frequency. The input signal of the frequency counter is digital, coming from a multiplexer on the IF converter board, so that the frequencies of various signal sources can be measured.

9.4 Synthesizer BN 2101 (OD-11)

The synthesizer OD-11 is used in several instruments. Not all of the features of this universal module are used for the SNA-20/-23. The following circuit description includes all possible features of the synthesizer. Those features not used in the SNA are marked accordingly.

9.4.1 Standard frequency oscillator, NFO adapter (50) [2101-C]

The standard frequency oscillator supplies a 10 MHz sinewave signal (ST101 or BU101 Pin 9 "10MHZRF") which is used as a reference by the synthesizer and from which it derives its frequency accuracy (long- and short-term stability). The short-term stability (phase noise) of the synthesizers for a control bandwidth of, say, 10 kHz is set by the standard frequency oscillator up to a frequency offset of 1 kHz. The standard frequency oscillator is a thermally stabilized crystal oscillator (OCXO). The absolute frequency can be set via potentiometer P101 or via the control input "UVCO" BU101.5 or ST101.5 (for external 10 MHz synchronization).

9.4.2 YIG oscillator OS1 (50), YTO

The YIG oscillator is a current-controlled oscillator for the frequency range 3.1 to 8 GHz which can be synchronized by the synthesizer to the standard frequency oscillator via a PLL (internal control) or operated as a voltage controlled oscillator. The YIG oscillator is controlled using two control coils: The tuning coil serves for setting the frequency and has a large control slope at high inductance; the FM coil has low control slope and inductance and is used for frequency modulation (rapid tuning). The frequency modulation function is not used by the SNA.

9.4.3 Timebase/YTO driver [2101-B]

9.4.3.1 Central filter (DC-PREFILTER)

The central filter serves as a pre-filter and suppresses interference voltages for the supply voltages from the AC PSU before they are fed to the individual modules of the synthesizer. The ± 6.5 V and ± 12 V supplies are filtered by a low-noise OP filter in each case and the +18 V supply by a passive filter. The function is described using the +12 V OP filter as an example. The OP filter +12 V compares the ground potential IC41 Pin 3 as nominal value with the AC coupled +11.8 V actual value at IC41 Pin 2. The resulting amplified correction voltage at IC41 Pin 6 is input in antiphase to the interference voltage. The filter circuits for -12 V and ± 6.5 V operate in the same way.

9.4.3.2 Timebase

The timebase circuit provides various frequency reference signals for internal and external modules. The circuit basically comprises the following function units:

- Timebase filter
- Timebase 1 (external synchronization control circuit)
- Timebase 2 (400 MHz PLL)

Timebase filter

The supply voltages from the central filter are filtered by this circuit again using low-noise active filters similar to those in the central filter (see section 9.4.3.1) to give the required suppression of AC interference voltages for the timebase reference signals. OP filters (IC8, 9) are used to derive +5 V and -5.2 V from the +6.3 V and -6.3 V rails and transistor filters (T2, T8 and T9) to derive ± 10.5 V from the ± 11.8 V rails.

Timebase 1 (external synchronization, 10 MHz)

A 10 MHz signal at the "Fext10Mz" input (BU1), after conversion to TTL level (IC1) and amplification (T1) is detected by a peak value detector (GL3, GL4,C4,C6 and R12) and closes a slow PLL via the control signal IC4.4 Pin 8 *(control bandwidth approx. 14 Hz)*. The standard frequency oscillator (OS101) is operated as a voltage controlled oscillator (control input "UVCO" ST101 or BU101 Pin 5). Its 10 MHz signal ("10MHZRF" ST101 or BU101 Pin 9) is fed to the comparator side of a FACT frequency/phase detector (IC31 and IC15.4) after conversion to FACT level by the limiter amplifier (T3) and is compared in phase and frequency with the external 10 MHz signal. The resulting control voltage pulls the frequency or phase of the standard frequency oscillator via PI controller (IC6.2) to achieve synchronization to the external 10 MHz signal.

A signal that the operating frequency accuracy of the standard frequency oscillator has been reached after a cold start is given by the "OVEN_WARM" status signal. This signal is derived from the current detected (via R14) drawn from the oven of the standard frequency oscillator.

Timebase 2 (400 MHz PLL)

The 400 MHz oscillator [2101-F] is locked to the standard frequency oscillator by a PLL. For this, the 400 MHz signal is passed through a frequency divider chain (10:1 Ecl divider IC3 and two 2:1 Fact dividers IC12) to divide it by 40 and fed to the comparator side of a FACT frequency/ phase detector (IC32 and IC5.1) and is compared with the 10 MHz signal of the standard frequency oscillators ("10MHz" IC32.2 Pin 11). The resulting control voltage pulls the frequency or phase of the 400 MHz oscillator via PI controller (IC35) and locks the loop. As the 400 MHz PLL has a control bandwidth of 1 kHz, the short-term stability (phase noise) for offset frequencies above 1 kHz is determined by the free-running 400 MHz oscillator.

The following timebase output signals are provided from this module:

- 400 MHz sinewave, 0 dBm/50 Ω ("400MHZ" at BU7)
- three 20 MHz signals with Fact level ("20MHZ_1", BU3 to "20MHZ_3" BU5)
- an inverted 20 MHz pulse with a pulse width of approx. 4 nsec at ECL level ("PD_20MHz" at BU8)
- 10 MHz, 0 dBm/75 Ω ("10MHZ_RW" at BU2)

9.4.3.3 Controller/YTO driver

This circuit module includes the switchable control amplifier (PI controller) for the YTO PLL and the voltage/current converter for driving the YTO.

Controller/YTO driver 1 (PLL mode)

The differential output signal of the phase meter [2101-K] at (50) IC18 and TP 13) is first passed parallel to the controller signal path of the YTO PLL to a double-way rectifier with following Schmitt trigger (IC17) to generate the signal "YTO_SYNC". This status signal indicates synchronicity of the YTO PLL in fixed frequency operation (in CW mode, the phase meter output voltage is approx. 0 V in the locked state).
The phase meter correction voltage can be weighted with two separately switched filters (IC22 and C62 to C66, L33, L34) in the signal path. These serve to suppress the incremental frequency and its harmonics during a frequency sweep, switching being every 19.2 µs. The gain of the subsequent non-inverting amplifier (IC19) can be controlled via the "VLIN" circuit (compare Controller/YTO driver 2). After this, the gain and corner frequency required for a particular control bandwidth are set in the first part of the circuit (IC23). Four control bandwidths are available; these are set by the analog switch (IC25) which is programmed from the DSP (synthesizer controller). The control bandwidths are 100 Hz, 3 kHz, 10 kHz (default setting) and 30 kHz (rapid tuning). The "INTEGRATOR" control signal is fed to an integrating voltage-controlled current source (IC26 and T16) and drives the YIG TC coil in the case of internal control. A resistor in parallel with the YTO TC coil (R221) which serves to reduce the frequency dependent slope of the YTO TC coil (1st order low-pass filter) is switched out for the 30 kHz control bandwidth by a switchable inductor (L11).

Controller/YTO driver 2 (VLD mode)

When the YTO is controlled externally (this function is not required in the SNA), a relay (REL1) is used to switch to a parallel voltage-controlled current source (IC36 and T17). This allows the YTO to be controlled via the differential "VC/VC_N" input ST15 Pin 2 and 1.

In both cases, the current-proportional voltages across the measurement resistors of the YIG driver (R152 or R153) are tapped to generate frequency-proportional control signals. This signal (TP22) can be used to realize linearization of the control loop gain for the internal PLL. For this, the loop gain is incremented in two steps by reducing the resistance (R109) with the frequency via the signal line "VLIN" (compare Controller/YTO driver 1), to compensate for the frequency dividing factor which drops with the frequency.

A frequency span provided for an internal 18 Hz sinusoidal sweep can be switched on to the differential output signal "F_MON" via bandpass filter IC24 at connections HO24 and 25 for evaluation by the DSP. For externally controlled operation (signal tapped from TP23), a superimposed frequency span can also be switched on to the differential output signal "F_MON" via high-pass amplifier IC47 for measurement by the DSP (this function is not used in the SNA).

YTO frequency limiter

Regardless of the YIG driver which is used, a limiter circuit (IC38 and T10,T11) operates when the YTO frequency limits are exceeded. The YTO current is detected via a measuring resistor (R206) and compared with an upper (IC38.2 Pin 6) and a lower (IC38.3 Pin 10) limit value. Depending on the result, an additional current is fed in via T10 or the excess current drained via T11.
The low-noise active OP filters IC28, IC29 and T23, and IC40 and T22 on this circuit section are used to generate the reference voltages "+5 VREF", "-5 VYTO" and "+15 VYTO".

Serial interface to synthesizer controller

The programmable switches are set by the synthesizer controller DSP using the static control signals "DS(0)" to "DS(15)" via the serial interface to the synthesizer controller (IC45 and IC46 with the signals "DATA" ST9 Pin 24, "SHIFTCLK" ST9 Pin 23 and "LATCHCLK" ST9 Pin 22).

Synthesizer interface to frequency modulation

A synthesizer interface to frequency modulation is provided at BU17 by bringing out the connections to the YTO FM coil (not used in the SNA).

9.4.4 400 MHz oscillator ([2101-F]

The 400 MHz oscillator is a voltage controlled LC oscillator which is synchronized to the standard frequency oscillator by a PLL (compare Timebase 2).

9.4.5 Synchronous divider/phase meter (52), [2101-K]

9.4.5.1 Synchronous divider

In this part of the module, the YTO signal predivided by a factor of 16 in the SHF predivider module ("FYTO/16" at (52) BU20) is passed to a further frequency divider. This is a fractional divider which allows non-integer fractions of the 20 MHz reference frequency of the YTO PLL. This consists of an integer ECL frequency divider (IC2), the programming inputs of which are time-weighted with the aid of a computing algorithm realized in the gate array PLLIA (IC1). This produces frequency division which is fractional when averaged. The fractional division factor is written to the gate array (IC1) via the DSP (the synthesizer controller) from where it is passed to the ECL divider in the form of a specific sequence of whole-number program values.

Before the divided YTO signal ("ST_20MHZ" and "ST_20MHZ_N") reaches the comparator side of the frequency/phase detectors, it is resynchronized by passing through the D flip-flop IC6 (edge jitter limiting) and several gates (IC4 and IC5) which function as buffer stages for the ECL signal peaks. The output signal of the fractional divider is also used as the processor clock for the PLLIA gate array after conversion from ECL to HCMOS level and pulse widening (IC7 and T1 to T3).

In externally controlled YTO mode, the output signal of the fractional divider can be switched on to output "FYTO/400" (52) BU21 (T4 to T7). This output is used e.g. for YTO frequency measurement under external control. When the fractional divider is set to a fixed factor of 25, the overall factor with the predivider factor of 16 is 400 for the YTO signal.

9.4.5.2 Phase meter

The digital frequency/phase detector IC58 compares the 20 MHz reference signal "PD_20MHz" from the timebase at (52) BU40 with the divided YTO signal "ST_20MHz" or "ST_20MHzN" and thus generates a correction signal which re-locks a free running YTO by means of two-point regulation (frequency-sensitive range, synchronization to standard frequency oscillator) and which holds the YTO in a PLL if the YTO is locked (phase sensitive range, specific control bandwidth, e.g. 10 kHz). Gates (IC53 and IC54) are used to decouple the 20 MHz reference signal as in the synchronous divider. The correction signal must also be filtered by a 3rd order lowpass filter to remove the switching interference generated by the computing algorithm in the PLLIA gate array and to suppress the 20 MHz reference frequency.

9.4.6 Synthesizer controller (51), [2101-A]

The ADC interface (ADC PORT) consists of an ADC IC31 with preceding digitally programmable amplifiers (IC35, IC21 and IC36). A signal at the differential analog input "F_MON" ST12 Pin 2 and 1 can thus be sampled at intervals corresponding to the interrupt period of 19.2 µs (signal line "NIRQA") and read in by the DSP using digitally set scaling from DAC IC35.
In the INTERRUPT GENERATION circuit, the interrupt periods are generated by frequency division (IC33, IC34, IC32 and IC10.2) of the signal "CLK_10MHz". The signal "CLK_10MHz" is itself derived by division (IC17.1) of the DSP 20 MHz clock. The interrupt period "PINT" (19.2 µs) is programmable from the DSP. The "INTB" (3.35 s) interrupt period is fixed.
The address decoding for the I/O ports of the DSP (DSP-BUS ADDRESS DECODER) is realized using IC24, IC25, IC27, IC28, IC10.1 and IC10.4. The following components are selected via chip-select lines:

- Gate array PLLIA (compare "Synchronous divider" (52)IC1) via "CS1N"
- ADC IC31 via "CSADWN"
- DAC IC35 via "CSDACN".

The ports, which are passed via a flip-flop, receive a clock pulse when selected which switches the input data for the relevant port through to the port outputs:

- IC19 is activated via "SIC19CLK"
- IC18 is activated via "SIC18CLK"
- IC30 is activated via "SIC30CLK".

The serial output interface for setting the programmable switches on the timebase/YTO driver board and for "PINT" interrupt programming (IC19) are brought out to ports. The input interface for querying the status signals from the timebase/YTO driver board is also present (IC18). The interfaces (IC18 and IC30) are for various trigger input and output signals and for storing or reading synthesizer-specific information to/from the EEPROM (IC7).
The synthesizer controller has two 16-bit output ports. The first is the YTF port (IC2 and IC3) with its attendant data valid signal (YTFSTROBE) IC9.1. The X-ADDRESS PORT is formed by IC4 and IC5 and IC9.2 (XW_STROBE), and is the interface to the measurement section controller.
The PLLIA BUS (IC29, DSP data bus) for controlling the gate array PLLIA (52) IC1 is another interface.
The DSP-RAM module (IC6) expands the RAM available in the DSP.
Coupling of the DSP to the AT processor is realized via the DSP address decoder (IC15 and IC14), the read/write switch (IC22, IC17.2, IC10.3, IC13.1 to IC13.3) and the data bus direction switch (IC37).
The DSP can be set to RESET mode with the aid of the DSP control register (IC11 and IC16).
The DSP clock can be generated asynchronously using the 20 MHz crystal (Q1) or synchronous to the timebase via the 20 MHz timebase signal "20MHZ_1" BU11.
The SYNC.PORT interface which can be used to synchronize two synthesizers, is not used in the SNA. The "PINT" interrupt circuit the period of which (19.2 µs) is used to increment the frequency during frequency sweeps can be looped from master to slave to achieve interrupt synchronization. Master/Slave switching is via the DSP control register, i.e. via the AT processor.

Controller filters

Active OP filters are used to filter the supply voltages. These operate in addition to those on the central filter board. The filters for the synchronous divider/phase meter (IC201,IC202, IC203) and the SHF predivider module (IC20) are also present in this circuit diagram.

9.4.7 SHF pre-divider module (53) [2101-ZG]

The YTO signal "FYTO" is (a) directly looped through the SHF predivider module to give the synthesizer RF output "1.LO", and (b) coupled in to a microwave amplifier (U3). This amplifier serves to isolate the subsequent microwave frequency predivider U2 from the YTO, as the divided frequency ("FYTO":8) and its harmonics are present as crosstalk on the divider input and would therefore appear at the YTO output if not decoupled. The YTO signal, predivided by 8 is then divided further by a factor of 2 in another frequency divider U1 to give the division factor 16. This signal ("FYTO/16") is then fed to the synchronous divider.

9.5 Controller (16), (17), (18), (19), (20), (21), (92)

The controller of the SNA-20/-23 contains the following modules:

- AT CPU (18)
- Memory (17) [2101-AF]
- Interface board (16) [2101-AG]
- Display control board (92) [4111-A]
- Keyboard (20) [2101-AJ]
- Rotary control (21) [2101 AK]
- Keyboard controller (19) [2101-AL]

9.5.1 AT CPU (18)[] series A through E (3011.9305.006)

The STANDARD SYSTEM MODULE 386-WGR is used as CPU in this instrument. This is an AT CPU with 80386SX/25 MHz processor, 4 MB RAM (expandable to 8MB) and 32 KB CACHE RAM. The circuit board is fitted with an EEPROM for storing and reading out instrument-specific data. This compact CPU board provides the following interfaces:

- AT bus interface with all address, data and control lines at P1 and P2
- Two serial interfaces (SERIAL PORT 1 and 2) at J1, J4 (port 2 is not fitted)
- One parallel interface at J5
- Interface for floppy disk (HD format, 1.44 MB)

9.5.2 Memory (17) [2101-AF] (series A through E only)

The memory board occupies the address range 580000hex to 5FFFFFhex and 920000hex to FBFFFFhex. It is connected electrically to the AT CPU (SIM386-WGR) via the 96-way and 48-way three-row strip connectors (J1, J2; CONTROL-BUS). All circuits on the 96-way and 48-way strip connectors are taken directly to the three 50-way ribbon cable connectors (P1, P2, P3) which also feed all of the CONTROL BUS lines to the interface board.

Power supply

The memory board requires the following supply voltages:

- 5V ±5%; I = 400 mA
- 12V ±5%; I = 60 mA

The supply voltages are fed from the interface board via the three 50-way ribbon cables. TTL levels are present on the signal circuits to the AT CPU and to the interface board. Memory board accesses are all 16-bit and are in the CPU memory area. The following timing is used: The bus clock is 8 MHz; one command delay and two wait states are inserted per cycle.

Decoding (see block circuit diagram)

The decoding is realized using seven PALs (U202 to U208). A "chip select" (NCSxy) signal is generated for each memory component. The address range for which the chip select is active is determined from the addresses and the signals ZWEIMB and NCSE. The NCSE signal is active-low and enables the chips selects when no RESET is present and memory access is required.
The memory control has EVEN and ODD or low byte and high byte structure, due to the 8-bit chip organization. If SA0 is LOW, the low byte is activated; if SBHE is LOW, the high byte is

activated. For 16-bit access, A0 and SBHE are LOW within one cycle.
Since SA0 is used to distinguish between EVEN and ODD, the lowest address for the memories is SA1.

Important: "Low byte components" have even chip select numbers (EVEN addresses).
"High byte components" have odd chip select numbers (ODD addresses).

RAM: (U300 to U304)

The SRAM capacity is 512 KB; it is battery-buffered (V_{batt} > 2.0 V). The chip organization is 128K x 8. The switch from +5 V to V_{batt} and vice-versa when switching the instrument on or off is realized using U306.
The lithium battery (BT1) which buffers the SRAMs is fitted on the memory board. It is plugged in for easy replacement. The SRAM contents may be partially or completely lost when the battery is replaced. The battery capacity is (depending on type) 1000 mAh or 750 mAh. The memory status port (U201.1) indicates whether the battery voltage is sufficient (V_{batt} >2.2 V) or too low to retain the SRAM contents (V_{batt} <2.2 V) (see memory status port).

Correction value memory (U512, U513)

This memory area is reserved for correction tables (e.g. frequency response corrections). This area is not used at present in the SNA, as the correction tables are stored in the battery buffered RAM.

These FLASH-EPROMs can be organized as 128 K x 8 (standard) or 256 K x 8 modules. The memory size must be the same as that of U400 to U413 and U500 to U511.
Jumper P210 must be set to match the memory modules used.

P210:
Pin 2,3 ON: 1 Mbit chips
Pin 1,2 ON: 2 Mbit chips. ON = Jumper fitted

To set the program voltage (+12 V ± 5%), the address 920000hex must be set. The program voltage is present until the address 920200hex is set. Decoding of this address range is by means of the PAL U204 (SVPP). The +12 V is switched to VPROG via Q701. VPROG is +5 V in read mode for the FLASH EPROMs.

Program memory (U400 to U413 and U500 to U511)

The SNA instrument software is stored in this memory area. The memory can be configured in four ways, depending on the settings of jumpers P210 and P211. The components must be fitted in pairs, because control is via low byte and high byte. The memory must be the same size as that of U512 and U513 (correction value memory).

Possible configurations:

P210 controls the input "ZWEIMB" of the decoder PALs.
Pin 2,3 ON; ZWEIMB = Low ==> 1 Mbit chips
Pin 2,1 ON: ZWEIMB = High ==> 2 Mbit chips

P211 sets whether EPROMs or FLASHs (U400 to U413 and U500 to U511) are fitted. The link setting feeds either "+5 V" or "VPROG" to the Vpp pin of the components.
Pin 2,3 ON; Vpp = +5 V ==> EPROMs fitted
Pin 2,1 ON: Vpp = VPROG ==> FLASHs fitted

Extended BIOS(U400...U401)

The extended BIOS is 64 kB and is part of the program memory.

Memory status port (U201.1)

The memory status port can be addressed in the range 921800hex to 9218FFhex. It is a 4-bit read port which provides the following information signals:

Data circuit D0

D0 is driven by the signal line "ZWEIMB".

HIGH	2 Mbit chips fitted	(U400 to U413 and U500 to U513)
LOW	1 Mbit chips fitted	(U400 to U413 and U500 to U513)

Data circuit D1

D1is driven by the signal line "NLOW_BAT".

HIGH	VBatt > 2.2 V	Battery o.k.
LOW	VBatt < 2.2 V	Battery requires immediate replacement.

Data circuit D2

D2 is driven by the signal line "HOT", which is fed to the memory board from the AC PSU via the interface board.

HIGH	Instrument temperature > Max. allowed component temperature ==> too hot
LOW	Instrument temperature < Max. allowed component temperature ==> o.k.

Data circuit D3

D3 is driven by the signal line "FLASH".

HIGH	FLASHs fitted	(U400 to U413 and U500 to U511)
LOW	EPROMs fitted	(U400 to U413 and U500 to U511)

Test points

MP200	NID-CS3	Chip select for the ID-EEPROM U200, active-low.
MP201	ID-SK	Clock for the ID-EEPROM U200.
MP202	ID-DATA	Data circuit for the ID-EEPROM U200.
MP203	NMEMCS16	Active-low output to CPU for enabling 16-bit access. NMEMCS16 is high-impedance outside the memory board address range.
MP204	MEMORY _STATUS	Chip select for the memory status port, active-low.
MP308	VCC1	Instrument on: VCC1 = 5 V Instrument off: 3,7 V>VCC1> 2,1 V.
MP309	NLOW_BAT	LOW if battery voltage is 2.2 V; otherwise HIGH.
MP700	SVPP	HIGH: Program voltage for the FLASHs = on. VPROG = +12 V. LOW: Program voltage for the FLASHs = off. VPROG = +5 V.

9.5.3 Interface board (16) [2101-AG]

The interface board is connected to the AT CPU, the memory board and the display control board via the CONTROL BUS. The CONTROL BUS signals are fed in via three 50-way ribbon cables via connectors ST1,ST2 and ST3 from the memory board (17) [2101-AF].The CONTROL BUS signals are fed from the interface board to the display control board via sockets BU1 and BU2.
The supply voltages from the voltage distribution board (1) [2101-BD] are fed to the interface board via ST16. The AT CPU, memory and display control boards are supplied with the supply voltages from the interface board (via the corresponding CONTROL BUS connections). Apart from distribution of the supply voltages and transfer of the CONTROL BUS, the following functions are found on the interface board:

- Chip select generation/control logic
- Timer
- IEC bus interface
- Interrupt controller
- Bus brake
- DMA bus interface
- Bus driver
- ID-EEPROM

Chip select generation/control logic

The various chip select signals are generated by IC10, IC11, IC13, IC14 (PAL), e.g. for IC12 (Interrupt Controller), IC15 (IEC bus), IC28 (Timer), IC21 (Bus brake) etc.Various control signals required on the interface board are also generated from logical combinations of CONTROL BUS signals and other control signals.

Timer

The timer is realized with time module IC28. The clock signals required for this module are derived by multiple division (IC9.2, IC26, IC27) from the 8 MHz CONTROL BUS clock. The timer generates the interrupt requests INT_TIMER0, INT_TIMER1 and INT_TIMER2 for the interrupt controller IC12.

IEC bus interface

The IEC bus interface is formed by the GPIB controller TMS9914 (IC15) and the bus drivers IC16 and IC17. The IEC bus of the SNA can be operated as a system controller.

Interrupt controller

A 92C59 (IC12) is used as interrupt controller. It generates the interrupt signal IEC_INT which is fed as IRQ10 to the CONTROL BUS from bus driver IC5.2 and which accesses the AT CPU for interrupt processing.

Bus brake

The bus brake circuit links the CONTROL BUS to the PERIPHERAL BUS. The circuit is formed by IC23, IC24 and IC33 (8-bit D latch) for the address bus and by IC22, IC25 (bus transceiver with register; bus transceiver) for the bidirectional data bus. The clock signals required for driving the components are generated by OS1, IC29.2 and IC21. The bus brake circuit is designed to minimize interference in the analog measurement sections caused by continual level changes on the address and data lines. The levels on these circuits are kept constant until renewed access to the peripheral bus is necessary.

DMA bus interface

IC30, IC31 and IC29.1 form a DMA interface. This allows the measurement section controller DSP (10) to directly access (DMA) the memory areas connected to the CONTROL BUS.

Bus drivers

The address, data and control lines of the CONTROL BUS are driven by bus drivers (IC1), (IC2), (IC3), (IC4), (IC5), (IC6), (IC19) and (IC32).

ID-EEPROM

Specific information about the interface board can be stored in or read from the ID-EEPROM (e.g. hardware status). The SNA's serial number is also stored in this EEPROM.

9.5.4 Display control board (92) [4111-A] (series A through E only)

The display control board (BSK-3) contains a VGA controller from Chips & Technology which is operated in EGA mode, and a graphic processor from TI, the TMS 34010. These two controllers make it possible to drive an EL display from FINLUX and an EGA monitor with TTL interface. Switching between the controllers and displays is via software (Instrument software menu: Mode, Configuration, Display, Display Screen INT/EXT).

The AT bus (CONTROL BUS) is fed to the BSK-3 via the 96-way and 48-way three-row connectors (P1, P2). The addresses (SA(19:0)) and various control signals are decoupled from the AT bus via bus drivers U38, U40, U5 and U39. The VGA chip requires a multiplexed address and data bus (IB). This is formed by bus drivers U35 and U37 for the addresses and U10 and U11 for the data. The VGA BIOS EPROM U71 is also connected to the internal 'IB' bus.

The VGA controller (82C455) is driven with a clock frequency of 32 MHz, with a pixel clock of 25 MHz for the CRT monitor (external monitor) and 16 MHz for the EL display. The VGA chip has 1 MB of video RAM (U12, U56 to U62).

For switching the TI processor (U63), the I/O decoding of the AT bus (CONTROL BUS) is needed. U31 (PAL22V10) decodes the higher value address lines for U4 (EP 910 -30), as well as MEMCS16 for the AT bus. U4 generates all the control signals required for the AT bus drivers and the host interface of the TI processor.

The TI processor can access local memory. This consists of 512 kB DRAM (U25 to U27) as TI processor program memory and 512 kB VRAM (U13 to U16) as video memory. A further 4 EPROMs (U17, U18, U21,U24) can be fitted as program memory for the TI processor (not used in the SNA).

The local memory access bus of the TI processor is a multiplexed address and data bus (TB_LAD(15:0)). The circuit for controlling the local memory of the TI processor is formed by the address multiplexer (U29, U23) for the addresses LB_MA(8:0) and the address latches U9 and U22 (LB_A(29:9)) for the EPROMs (U17, U18, U21,U24). The data lines for the memory bus (LB_D (15:0)) are generated by the bus drivers U19 and U53 from the multiplexed address and data bus (TB_LAD). U54 (PAL 22V10) decodes the addresses for the TI chip. The "CAS-before-RAS" refresh cycle logic is implemented with U30 and U6.

The TI processor has a 16-bit pixel bus (TS) with 4 bits per pixel. Each word therefore contains 4 pixels. This in turn requires 4 to 1 pixel multiplexing. U32 and U36 form the first 2:1 multiplexer and U51 (PAL) forms the second. U51 also switches the pixel clock for the TI processor. Clock signal blanking for the serial VRAMs (U13 to U16) is done with U47, U6 and counter U90.

U8 forms the EL interface register and U20 is the CRT interface register for selecting the mapping EPROMs U44, U43 and blanking the CRT monitor. U41 latches the data pixels of the VGA chip. The individual pixels from the TI and VGA controllers are stored in U42 and U45 to provide synchronization with the clock signals and stable addresses for the color table EPROMs U43 and U44.

Up to 16 mapping tables can be stored for each controller in the CRT EPROM U44. The selection of individual bits is via multiplexer U48, the bits being latched by U49. The EL EPROM U43 contains twice as many color tables as U44, as the EL display only requires two pixels for driving in each case.

The complex EL interface in U54 (ELINTER, EP910-30) includes a 4:1 multiplexer which is controlled by bits 3 and 4 in the ELREG control register U8.

The synchronization and clock signals for the EL display and CRT monitor are switched with U46 (PAL). U46 basically takes care of switching the processors to the various displays. The output signals to the EL display are latched via U2 to achieve synchronization between the SYNC signals, the EL clock and the pixel data for the EL display.

9.5.5 Keyboard (20) [2101-AJ]

There are three function blocks on the keyboard board.

Front panel LED controller

The LED controller is formed by two 8-bit latches (IC3,IC4) connected to the keyboard controller data bus. The latches accept data on the rising edges of control signals "CSW_LED_P1" and CSW_LED_P2".

Key matrix

The rows are driven sequentially with a LOW signal from the 1 from 8 decoder (IC2) (CS_ROWxy) and the columns read each time via IC1 (CSR_INT_DATA = LOW) from the keyboard controller.

STANDBY key and ON/OFF-LED

(see "Standby function" on page 9-37)

9.5.6 Rotary control (21) [2101 AK]

The rotary control board requires three operating voltages +5 V, +12 V and -12 V which are fed to the board via ST4. Of the 4 function blocks, three evaluate the rotary sensor and one handles the probe operating voltage:

- Control and evaluation logic
- Continuous operation
- Locked operation

The probe power supply is not fitted when this board is used in the SNA as no probes are used.

Initialization

The keyboard controller initialization routine sets the following states on the rotary control when the instrument is switched on:

- "RAST" = HIGH ==> continuous operation
- SPERR_DREHKNOPF" = HIGH ==> rotary control active
- 16-bit counter is set to 8000 Hex
- The counter high byte is read out to enable the clock

Communication to the keyboard controller

The interface to the keyboard controller is formed by the 8-bit data bus, via which the counter values are read or the counter is set, and to which one read and one write port are connected. IC15, IC16 IC23 and IC24 make up the counter. The write port (latch, IC18) is written to using the active-low control signal "CSW_STAT_DREHK". IC17 serves as the read port, which is read with the active-low signal "CSR_DREHKNOPF". The keyboard controller polls the read port. If the signal "DREHKNOPF" (IC7, PIN 13) is HIGH during the read operation, the rotary control was moved and the counter value is read out and then reset to 8000Hex. The rotary control is disabled during read, to ensure that the counter value does not change between reading the high byte and the low byte. The rotary control is then reactivated by the active-low signal "CSW_RES_DREHK".
The rotary control can be disabled, i.e. the signal "DREHKNOPF" is blanked, by setting the signal "SPERR_DREHK" at the write port to LOW.

Continuous operation

In continuous operation, the signal "RAST" is HIGH. The inverted RAST signal is used to enable the clock generator monostable (IC6.1) via IC3 and IC4.2. The rotary sensor B1 operates as a generator in continuous operation.

Rotary control idle state

The motor does not supply voltage and the capacitors C11, C12, C51, C53, C35 are discharged. TP1 is at +2.5 V, the D input of IC3.2 is at +5 V and the D input of IC3.1 is at 0 V. The outputs of IC3 assume the following values with the clock generated by IC7.4, R34 and C34:

IC3.1 Q = HIGH
IC3.2 Q = LOW

These signals reset the monostable IC6.1 via IC4.2 and thus hold the clock for the 16-bit counter to HIGH via IC8.2 and IC7.2.
The signal "DREHKNOPF" is set to LOW via IC8.3 and IC11.2; this signals to the keyboard controller that the rotary control was not moved.

Rotary control clockwise rotation

The rotary sensor generates a negative voltage when turned clockwise. If the voltage level is below -1.4 V (rapid turning), the capacitors C11, C12, C51, C53 and C35 are negatively charged via R3 or via R11 if the control is turned slowly. The counter value changes in proportion to the rotation speed if the capacitors are charged via R11, or over-proportionally when they are charged via R3 (rapid rotation). The negative voltage on the capacitors is amplified by IC9. TP1 is then at 0 V. The D input of IC3.2 is LOW which enables the clock generator monostable (IC6.1) via IC4.2. The clock pulses cause the capacitors C11, C12, C51, C53 to discharge via IC1.2 and T1. The idle state is present at TP1again when the capacitors are discharged.

The direction of rotation is detected at the $\overline{Q}$ output of IC3.2 and passed on to the counter via IC4.3. The $\overline{Q}$ output of IC3.2 is HIGH for clockwise rotation, i.e. the counter increments starting from 8000Hex. Incrementing can only be halted by reading out the counter or disabling the clock.

Rotary control anticlockwise rotation

The rotary sensor generates a positive voltage when turned anticlockwise. The voltage polarity generates the direction of rotation signal at the $\overline{Q}$ output of IC3.2. The $\overline{Q}$ output is set LOW for anticlockwise turing, i.e. the counter decrements starting from 8000Hex. The remaining function is as for clockwise operation.

Locked operation

The signal "RAST" is LOW for locked operation, as the rotary sensor is not used as a generator but as a motor. The rotary sensor is the control element in a control loop. The arrangement of reflected light barriers and the voltage gain for controlling the motor simulate the 16 stable changeover switching points of a mechanical switch. An additional audible "click" (LSP1 and IC.7.6) enhances the effect of a mechanical switch each time changeover occurs.

Rotary control idle state

The rotary sensor is held at a stable locking point, i.e. the motor voltage is 0 V. The counter does not receive clock pulses and stays set to 8000H.

Clock and direction signal for 16-bit counter

The comparators IC14 and IC21 amplify the signals from the reflected light barriers to TTL level. The reflected light barriers generate different phase-shifted pulses, depending on the direction of rotation. Turned clockwise, EK3 lags 90 degrees behind EK2 and EK1 is 180 degrees out of phase with EK2.
Turned anticlockwise, EK3 leads EK2 by 90 degrees and EK1 is 180 degrees out of phase with EK2.
IC19.1 generates a 190 s pulse on the negative edge of EK2 and IC19.2 on the positive edge. IC4.4 blanks out the pulses on the positive edge during clockwise rotation and the pulses on the negative edge during anticlockwise rotation. The output signal from IC4.4 is passed to the counter (IC16, IC15, IC23, IC24) via an enable gate.
The direction of the counter is derived directly from EK2. This is HIGH on the positive clock edge of the 16-bit counter for clockwise rotation and LOW for anticlockwise rotation.

Motor controller

When the rotary sensor is turned a voltage is induced which opposes the rotation until the voltage at EK2 is reversed, i.e. the reflected light barrier changes its logical level and the rotary control pulls itself to the next stable state.

9.5.7 Keyboard controller (19) [2101-AL]

The keyboard controller is IBM-MF2 compatible. It uses the German character set (if KEYBYY=GR in the file B:\Auto2.bat of the SNA is selected).
An external MF2 keyboard (AT keyboard) can also be connected to the controller. Both keyboards (internal instrument keyboard and external keyboard) can then be used simultaneously.
The keyboard controller is made up from the following function groups:

- Processor core
- Interface to AT CPU (SIM386)
- Internal keyboard driver
- External keyboard driver
- Rotary control driver

The initial delay (500 ms) and the repetition rate (10 Hz) are fixed for the internal keyboard. The external keyboard can be set as desired from the AT CPU (from the AT CPU setup).
The electrical signals on the interface have TTL level.

Processor core

The microcontroller 80C39 is clocked with 10 MHz. The RESET of the 80C39 is linked to the instrument reset.

P10 to P13	serve for communication with the AT CPU
P14 to P16	serve for communication with the external keyboard.
P20 to P23	are the address lines A8 to A11 during read operations from EPROM and otherwise are four I/O circuits.

Interface to AT CPU (SIM386)

The data traffic between the keyboard and the AT CPU is via the circuits "AT_KEY_CLK" and "AT_KEY_DATA". Each data word comprises 1 start bit (LOW), 8 data bits, 1 parity bit and 1 stop bit (HIGH).

Interface to internal keyboard

P24 to P27 are fed to the keyboard board. They control the 16 rows of the key matrix. The row information for the keys is read with signal "CSR_INT_DATA".
When P13 is LOW, the processor detects that the AT CPU has data to transmit.
Among other things, the EPROM (IC3) contains a table of key codes to be transmitted when a key is pressed. Since the processor can only drive a maximum of 4Kb EPROM, the jumpers ST2, ST3 and ST4 are used to select one of eight pages in the 32Kb EPROM. Page 0 (no jumpers set) contains the program with the KEYBOARD conforming codes for the internal keys. Page 1 (jumper ST4 set) contains the key number conforming codes for the internal keys.
The LEDs on the internal keyboard are driven by two latches on the keyboard (20IC3 and 20IC4) which are driven by the signals LED_1 and LED_2.

Interface to external keyboard

When the external keyboard is operated, the keyboard scan codes are transmitted unchanged to the AT.
The codes from the external keyboard are inverted and read into shift register IC11 or IC12 by the signals "EXT_KEY_CLK" and "EXT_KEY_DATA". Once all the bits have been received by the shift register, output IC11/5 is HIGH. This signal disables the external keyboard for further transmission via the open collector driver IC14.5. The same signal is continuously polled by the processor via circuit T0, the processor thus detects that the external keyboard has transmitted

a character. The characters from the external keyboard are read in via ports IC9 and IC10 and put in the stack before being transmitted to the AT-CPU. After reading the external characters, the shift register is reset with "CSW:RESET".
Commands to the external keyboard are transmitted using the same protocol as is used by the AT CPU to the internal keyboard controller. This communication is via ports P14 to P16.

Rotary control driver

The keyboard controller initialization routine sets the following states on the rotary control:

- "RAST" = HIGH ==> continuous operation
- SPERR_DREHKNOPF" = HIGH ==> rotary control active
- 16-bit counter is set to 8000 Hex
- The counter high byte is read out to enable the clock

The controller software monitors the rotary control by polling the read port (21IC17) on the rotary control board which is activated by the control line "CSR_DREHKNOPF" = LOW. If the pulse generator is moved, D(1) = HIGH.
"CSR_DREHZAEHLER_LOW" and "CSR_DREZAEHLER_HIGH" are used to read out the 16-bit counter on the rotary control board (both signals active-low).
The write port (21IC18) on the rotary control is written to on the positive edge of the signal "CSW_STAT_DREHK". The contents of the write port sets whether the rotary control is active or disabled. The port also includes the information whether the rotary control was locked or continuously operated.

Lock on	==> D(0) = LOW
Lock off	==> D(0) = HIGH
Rotary control active	==> D(1) = HIGH
Rotary control disabled	==> D(1) = LOW

The signal "CSW_RES_DREHK" (dynamic, active-low) enables the rotary control after initialization.

9.6 Power supply unit

The SNA uses the AC PSU CG 44 manufactured by Gossen. This AC PSU supplies the following voltages and control signals to sockets BUX1 and BUX2:

BUX1	BUX2
+5 V	TOO HOT
+23 V	SAVE DATA
+6,8 V	SYNSIG
-6,5 V	-21 V
+18 V	+12 V
+12 V	FAN
-12 V	STDBY

Table 9-2 Output voltages and control signals from the AC PSU

9.6.1 Voltage distribution (1) [2101-BD]

The module-specific supply voltages are fed to the voltage distribution board (1) [2101-BD] from the AC PSU (plug X1) and then to the individual modules.

Plug 4 ===> 16 J16 interface board (CPU, memory, BSK-3)
Plug 5 ===> Floppy (AT-CPU)
Plug 6 ===> 3 P10 controller YIG filter
Plug 7 ===> 5 ST8 controller input section
Plug 8 ===> 50 ST13 Timebase/YTO driver (synthesizer)
Plug 9 ===> 12 ST10 IF distortion (radio link), not used in SNA
Plug 10 ===> 11 ST1 calibration generator, demodulator, IF measurement unit
Plug 16 ===> Tracking generator (instrument back panel)

A further plug (X2) from the AC PSU carries two auxiliary voltages, -21 V and +12 V, the AC PSU fan connection and the following data circuits for plug ST1 on the voltage distribution board:

- TOO HOT
- SAVE DATA
- SYNCHRONIZATION
- STANDBY

The instrument fan is connected to plug ST 3 on the voltage distribution board. The speed of the fan is controlled between 30°C and 50°C by connecting a NTC thermistor to ST14. If ST14 is shorted out (standard for SNA), the fan runs at full speed. Comparator IC5.2 switches the fan on at 10 °C.

Plug ST 2 connects the standby key and the standby LED to the controller.

The following voltages are available via the connection from plug ST12 to socket BU15 on the back panel:
From voltage regulators IC9 and IC10: +5 V/0.5 A; +15 V/0.35 A. Also, -12 V/0.1 A at Ri = 10 Ω is available. The two voltage regulators IC9 and IC10 operate without heatsinks to ensure that they switch off thermally when the current load is too high. The -12 V supply is fed to ST 12 via a 6.04 Ω resistor. The voltage source thus has a source impedance of about 10 Ω.

Standby function

With AC power "on" and "standby" selected, all supply voltages except the +12 V auxiliary voltage are switched off, the standby LED is on and the AC PSU and instrument fans are off. Retriggerable monostable IC8.1 debounces the standby key. The monostable hold time is about 2.5 seconds. This pulse drives bistable relay Rel1 which is used as a notching relay with the adapter module IC4.

Synchronization signal

A 50 Hz sinewave signal is fed from the AC PSU ST X2 to voltage distribution board ST1.3. This is converted to a 50 Hz square wave by OP IC5.1 and connected to ST10.15 on the voltage distribution board. This signal (SYN50HZ) is fed to the IF measurement section (calibration generator) (11) ST1.

Save data

This signal is supplied directly to ST X2.2 by the AC PSU and is connected to ST1.2 on the voltage distribution board, from where it is taken via (1)ST4.2 to the interface board (16) on plug (16)ST16.

Too hot

The "too hot" signal can be generated by the AC PSU (overtemperature) and switches the to standby mode (LED = flashing) if overheating occurs. The signal can also be generated by temperature monitor IC5.3. This OP is set to about 4.3 V on pin 9 using potentiometer P1, which corresponds to a cutoff (standby) temperature of 55 °C. The "too hot" signal is fed via (1)ST4.3 to the interface board (16)ST16 where it is evaluated by the controller.

Too cold

"Too cold" is generated by temperature monitor IC5.4. If the temperature inside the instrument at sensor NTC R40 is below 0 °C, the "too cold" signal is HIGH. This signal is fed via (1)ST 4.1 to the interface board (16)ST16 where it is evaluated by the controller (LED = flashing).

9.6.2 24/12 V switching regulator

The switching regulator provides the supply voltage for the EL display. The regulator supplies 2.0 A at 12 V and a switching frequency of approx. 100 kHz, is fitted with 'soft start' and internal current limit functions.

Wandel & Goltermann Worldwide (Sales Organizations)

Europe

Austria
Wandel & Goltermann GmbH
P.O. Box 13
Elisabethstraße 36
A-2500 Baden
Tel. 022 52-8 55 21-0
Fax 022 52-80 727
Telex 14 375 wgo a

Belgium/Luxembourg
Wandel & Goltermann nv/sa
Imperialstraat 10
B-1930 Zaventem
Tel. 2-725 18 19
Fax 2-725 41 42

The Netherlands
Wandel & Goltermann bv
Monnickskamp 8
NL-1273 JS Huizen
Tel. 02152-66 122
Fax 02152-67 937

France
Wandel & Goltermann France
46 bis, rue Pierre Curie
B. P. 10
Zone Industrielle Les Gâtines
F-78373 Plaisir Cédex
Tél. (1) 30 81 50 50
Fax (1) 30 55 87 75
Telex 698 955 f

Germany
Wandel & Goltermann GmbH & Co.
Vertriebsgesellschaft
P.O. Box 1155
D-72794 Eningen u.A.
Tel. 07121/86-15 11
Fax 07121/86-2028
Telex 7 29 833 wug d

Italy
Wandel & Goltermann S.R.L.
Technologie di Misure Elettroniche
Via Pomponazzi 25
I-20 141 Milano
Tel. 2-895 12 381
Fax 2-895 11 780

United Kingdom
Wandel & Goltermann Ltd.
Burrington Way
GB-Plymouth, Devon PL5 3LZ
Tel. 7 52 77 27 73
Fax 7 52 78 30 00
Telex 45 155 wagply

Spain/Portugal
Wandel & Goltermann
Sucursal de España
Bueso Pineda No 7
Apartado de Correos 48008
E-28043 Madrid
Tel. 1519 4624/15 19 48 24
Fax 15 19 59 81

Scandinavia
Wandel & Goltermann AB
Box 6044
Ellen Keys Gata 60
S-126 06 Hägersten
Tel. 8-88 04 08
Fax 8-88 38 90

Switzerland
Wandel & Goltermann (Schweiz) AG
P.O. Box 779
Morgenstrasse 83
CH-3018 Bern 18
Tel. 31-991 77 81
Fax 31 991 47 07
Telex 912 350 wg ch

Poland
see Austria

East and South East Europe
see Austria

North America

Canada
Wandel & Goltermann Inc.
21 Rolark Drive
Scarborough, Ontario M1R 3B1
Tel. 416-291-7121
Fax 416-291-26 38

USA
Wandel & Goltermann Inc.
2200 Gateway Centre Blvd.
Morrisville, NC 27560-9228
Tel. 919-460-33 00
Fax 919-481-43 72

Latin America

Argentina/Uruguay
Wandel & Goltermann S.A.
Montañeses 2599
RA-1428 Buenos Aires
Tel. 1-7 84 66 42
Fax 1-1 12 788
Telex 24 543 wglas ar

Brazil/Chile/Peru/Bolivia/Paraguay
Wandel & Goltermann
Instrumtacão Ltda. & Cia.
Av. Eng. L. C. Berrini, 936-9. andar
04571 Sào Paulo - SP
Tel. 11-241 15 88
Fax 11-241 96 62
Telex 11 56 569 wgep br

Guatemala/Central America/ Caribbean Islands
Wandel & Goltermann & Co
Gerencia Regional
Apartado Postal 458-AG
GCA-01901 Guatemala Ciudad
Tel. 2 31 80 65
Fax 2 31 86 82

Mexico
Wandel & Goltermann de México, S.A. de C. V.
San Francisco No. 6
Col. Del Valle
México D.F.
C.P. 03100 México
Tel. 5-543 66 44, 5-543 85 99
Fax 5-543 86 60

Colombia/Venezuela/Ecuador
Wandel & Goltermann Andina Ltda.
A.P. 55052
Cra. 14 No. 85-82, Oficina 401
Santa Fé de Bogotá DC
Colombia
Tel. 1 256 4001, 1 616 3584
Fax 1 616 3267

Asia

Middle East
see France

South East Asia
see Hong Kong

India
see United Kingdom

Israel
see Germany

Iran/Turkey/Pakistan
see Austria

Hong Kong
Wandel & Goltermann Ltd.
1905 Lippo Centre, EIE Tower
89 Queensway, Central Hong Kong
Tel. 8 68 31 13
Fax 8 68 54 82
Telex 77787 WANGO HX

Korea
Wandel & Goltermann Ltd.
4th Floor, Kamyung Building
153-29 Samsung 1-dong
Kangnam-ku
Seoul 135-091
Republic of Korea
Tel. 2 563-22 36/7
Fax 2 563-22 39

Japan
Wandel & Goltermann K.K.
German Industry Center 207
1-18-2 Hakusan-cho, Midori-ku
Yokohama-shi, Japan 226
Tel. 45-931-57 25
Fax 45-931-57 28

China
Wandel & Goltermann
Beijing Office
Room 728
Wang Fu Jing Grand Hotel
57 Wang Fu Jing Street
Beijing 100006
China
Tel. 86 1 522 41-70/71/72/73
Fax 86 1 522 41 74

Australia/Pacific Islands New Zealand
Wandel & Goltermann Pty. Ltd.
P.O. Box 419
World Trade Centre
Melbourne, Victoria 3005
Tel. 3 690 67 00
Fax 3 690 67 50
Telex AA 34 801 wg aus

Africa

North and West Africa
see France

East and South Africa
see Switzerland

For all other countries please contact
Wandel & Goltermann
Management Holding GmbH
Corporate Communications
Postfach 1262
D-72795 Eningen u.A.
Tel. +49 7121 86-1816
Fax +49 7121 86-1848

A closely linked network of more than 20 affiliated companies and more than 60 agencies ensures that our customers receive the best possible advice in solving specific measurement problems. For more detailed information, please turn to your local sales agency or to our International Information Service.