Data Library
July 1985

The following RS data sheets issued later than July 1985 are also included at the rear.....

5982 --- Modem IC 6926 CCIT V21 Data Format --- November 1985

6092 --- Heatsink Performance Guide --- November 1985

6115 --- Switching Regulator L296 --- November 1985

6200 --- Suppression --- November 1985

6345 --- Audio Preamplifiers LM381, HA12017, 6270 --- March 1986

6424 --- Adjustable Voltage and Current Regulator L200 --- March 1986

6610 --- Fixed Voltage Series Regulators --- July 1986

7196 --- Regulating Pulse Width Modulator --- November 1986

7310 --- Dual Switched Capacitor LTC1043 --- November 1986

7348 --- 5th Order Low Pass Filter LTC1062 --- November 1986

7512 --- STE Bus Computer Boards --- March 1987

10906 --- Pyroelectric Detector Kit --- March 1992

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	Optical communications receiver RS LH0082	**4563**	Mar 82
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4195	Dual regulator	2040	298
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7211	LCD Decoder driver i.c.	3964	310
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7224	LCD counter/decoder/driver i.c.	3970	309
7225	Keyless lock i.c.	4305	327
7226	Quad 8-bit D to A converter i.c.	5522	312
7226A	Universal counter i.c.	4412	308
7231	Triplex LCD driver i.c.	4787	310
7240	Programmable timer i.c.	3942	306
7525	3½ Digit BCD potentiometer i.c.	4686	303
7528	Dual 8-Bit D to A converter i.c.	4995	312
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7581JN	8-Channel, 8-bit A to D converter i.c.	4507	311
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7652	Chopper stabilised operational amplifier i.c.	4434	295
7660	Voltage converter i.c.	4248	299

Type	Device	Data Sheet Number	July 85 Catalogue Page
7663BCPA	Micropower adjustable voltage regulator	**5819**	298
7664BCPA	Micropower adjustable voltage regulator	**5819**	298
8038	Waveform generator i.c.	**2141**	326
8211	Micropower voltage detector i.c.	**3576**	300
8629	Prescaler i.c.	**3059**	307
8680	Prescaler i.c.	**4923**	307
8703	CMOS A to D converter i.c.	**3554**	311
9400CT	V/F and F/V converter i.c.	**3021**	304
HA12017	Low noise preamplifier i.c.	**4664**	287
50395	6 Decade counter driver i.c.	**3863**	309
54104	Speech synthesis system	**4822**	326
58174	Real time clock i.c.	**4298**	320
58274	Real time clock i.c.	**5875**	320
146818	Microprocessor compatible real time clock i.c.	**4945**	320

RS data

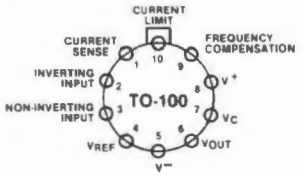
Voltage regulators L123 Metal can. L723 D.I.L.

Stock numbers 305-440 and 306-005

Absolute maximum ratings

	TO-100	DIL
Continuous voltage from V+ to V−	40V	
Input/output voltage differential	40V	
Maximum output current	150mA	
Current from V ref.	15mA	
Power dissipation (Tamb 25°C)	800mW	660mW
Ambient temperature derating	6.8mW/°C	5.6mW/°C
Operating & storage junction temp. range	0° to +70°C	
Ambient operating temp. range	−65°C to +150°C	
Lead temp. (soldering 10 sec. time limit)	+300°C	

Pin connections



NOTE: PIN 5 CONNECTED TO CASE

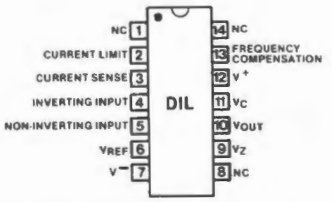
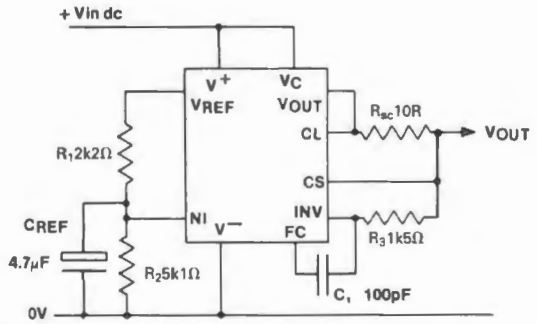


Figure 2: **Fixed output voltage** (circuit shown for +5V)

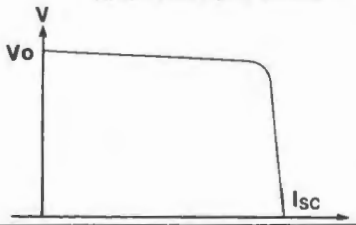


2-6V Regulator

with s/c current limit (ie no foldback characteristic and hence overloading of the regulator could occur under fault conditions).

Input voltage ____ 9-11V
Max. input ripple ____ 2Vpp
Ripple rejection ____ 74dB
Load regulation ____ 0.6% (1-50mA)
Line regulation ____ 0.3% (9-11V)
S/C current ____ 65mA
(Output current to 22mA for example shown)

Figure 3: **Output characteristic for regulator with current limit.**

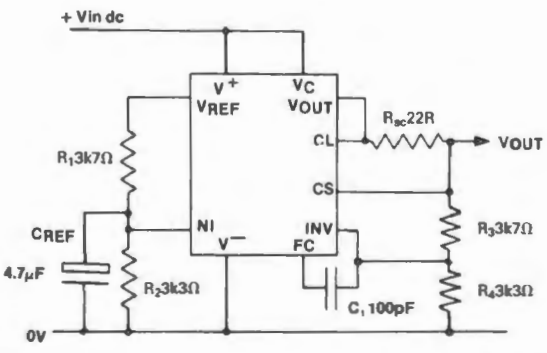


Output characteristic

For other voltages in the range 2-6V adjust R_1 and R_2 so that the voltage appearing at the non-inverting input (3) is the same as the desired output voltage. The voltage at V_{REF} (4) is 7.2V (nom) and R_1+R_2 should be between 5-15kΩ. R_3 should be chosen so that $R_3=\frac{R_1 \times R_2}{R_1+R_2}$.

R_{SC} so that $R_{SC}=\frac{0.65}{I_{S/C}}$

Figure 4: **Fixed output voltage** (circuit shown for +7V)



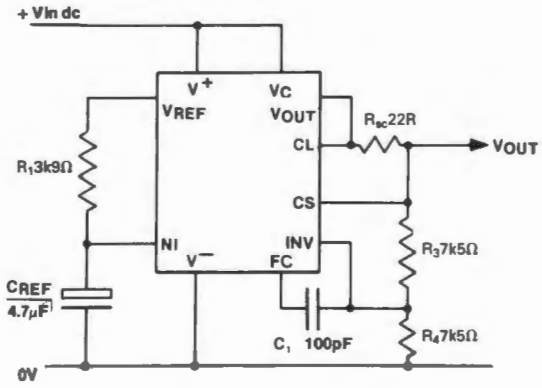
6-8V Regulator with s/c current limit

Input voltage ____ 10-17V
Max. input ripple ____ 3Vpp
Ripple rejection ____ 74dB
Load regulation ____ 0.4% (1-22mA)
Line regulation ____ 0.3% (10-17V)
S/C current ____ 30mA
(Output current to 50mA for example shown)

For other voltages in the range 6-8V adjust R_1 and R_2 so that the voltage appearing at the non-inverting input (3) = 3V and adjust R_3 and R_4 so that the voltage appearing at the inverting input (2) = 3V. R_1+R_2 & R_3+R_4 should be between 5 & 15kΩ

RS data

Figure 5 **Fixed output voltage** (circuit shown for +15V)



8-37V Regulator

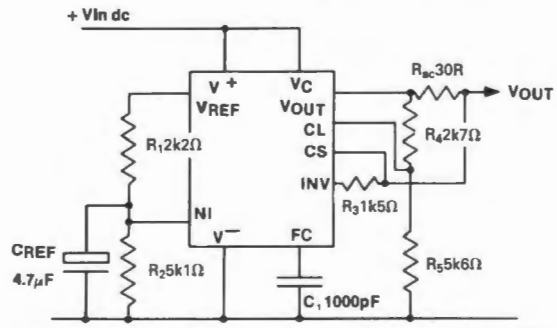
with s/c current limit

Input voltage — 19-20V
Max. input ripple — 2Vpp
Ripple rejection — 74dB
Load regulation — 0.4% (1-22mA)
Line regulation — 0.3% (19-20V)
S/C current — 30mA
(Output current to 22mA for example shown)

For other voltages in the range 8-37V adjust R_3 and R_4 so that the voltage appearing at the inverting input (2) = 7.2V. R_3+R_4 should be between 5 to 15k and R_1 should be chosen so that

$$R_1=\frac{R_3\times R_4}{R_3+R_4}$$

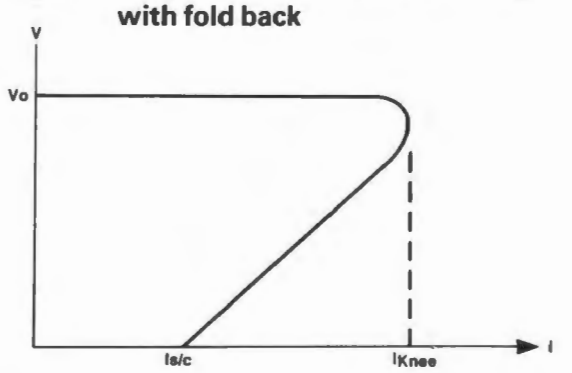
Figure 6 **Fixed output voltage with current foldback** (circuit shown for +5V output)



Regulator with foldback characteristics

Input voltage — 9-11V
Max. input ripple — 2Vpp
Ripple rejection — 74dB
Load regulation — 1.4% (0-110mA)
Line regulation — 0.3% (9-11V)
I_{KNEE} — 110mA
$I_{S/C}$ — 70mA

Figure 7 **Output characteristic for regulator with fold back**



Output characteristic

Other output voltages may be obtained using arrangements shown in Figs. 2 & 4.

For other values of I_{KNEE} and $I_{S/C}$ the values of R_{SC}, R_4 & R_5 should be adjusted according to the following formulae.

$$I_{KNEE}=\frac{V_O R_4+V_{SENSE}(R_4+R_5)}{R_{SC}R_5}$$

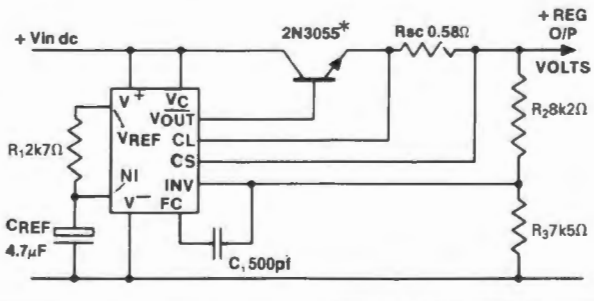
$$I_{S/C}=\frac{V_{SENSE}\times(R_4+R_5)}{R_{SC}R_5}$$

R_4+R_5 should be in the range 5 to 15kΩ.

V_{SENSE}=0.65V (nom)

V_O=Output voltage, under regulated conditions.

Figure 8 **Fixed output voltage at higher currents** (circuit shown for +15V)



Regulator with increased current output

Input voltage — 19-22V
Max. input ripple — 2Vpp
Ripple rejection — 74dB
Load regulation — 0.2% (0-1A)
Line regulation — 0.02% (19-22V)
S/C current — 1.1A

* 2N3055 transistor should be mounted on 2°C/W heatsink.

Other voltages may be obtained by using Fig. 2 & 4.

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RS data

Component colour codes

Four band resistors

1st band	
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

2nd band	
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

3rd band	
Silver	Divide by 100
Gold	Divide by 10
Black	Multiply by 1
Brown	Multiply by 10
Red	Multiply by 100
Orange	Multiply by 1,000
Yellow	Multiply by 10,000
Green	Multiply by 100,000
Blue	Multiply by 1,000,000

4th band (tolerance)	
Red	± 2%
Gold	± 5%
Silver	± 10%

Five band resistors

1st band	
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

2nd band	
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

3rd band	
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

4th band	
Silver	Divide by 100
Gold	Divide by 10
Black	Multiply by 1
Brown	Multiply by 10
Red	Multiply by 100
Orange	Multiply by 1,000
Yellow	Multiply by 10,000
Green	Multiply by 100,000
Blue	Multiply by 1,000,000

5th band (tolerance)	
Brown	± 1%
Red	± 2%
Gold	± 5%
Silver	± 10%

Six Band resistors

1st band	
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

2nd band	
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

3rd band	
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

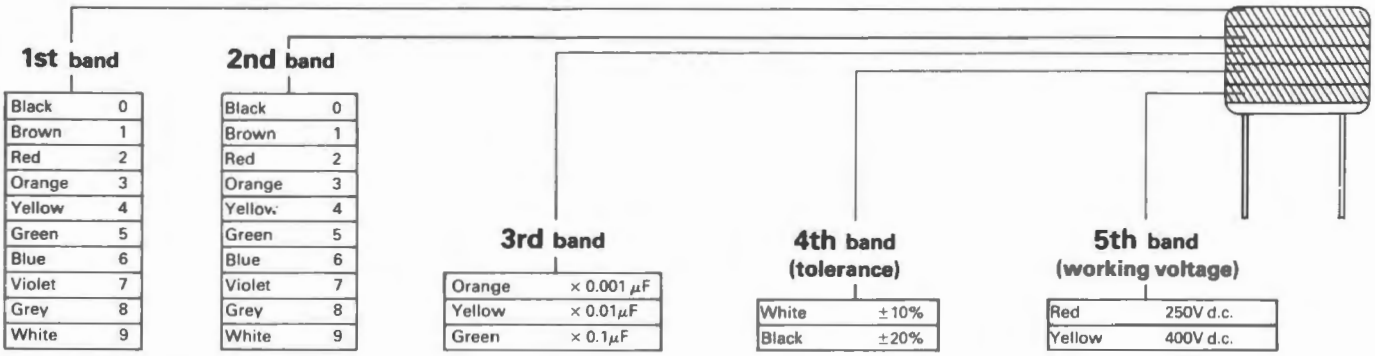
4th band	
Silver	Divide by 100
Gold	Divide by 10
Black	Multiply by 1
Brown	Multiply by 10
Red	Multiply by 100
Orange	Multiply by 1,000
Yellow	Multiply by 10,000
Green	Multiply by 100,000
Blue	Multiply by 1,000,000

5th band (tolerance)	
Brown	±1%
Red	±2%
Gold	±5%
Silver	±10%

6th band (Temp. Coef. PPM/°C)	
Brown	100
Red	50
Yellow	25
Orange	15
Blue	10
Violet	5
White	1

RS data

Polyester capacitors



1st band

Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

2nd band

Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

3rd band

Orange	× 0.001 μF
Yellow	× 0.01 μF
Green	× 0.1 μF

4th band (tolerance)

White	±10%
Black	±20%

5th band (working voltage)

Red	250V d.c.
Yellow	400V d.c.

Standard decade values

E24	10	11	12	13	15	16	18	20	22	24	27	30	33	36	39	43	47	51	56	62	68	75	82	91
E12	10		12		15		18		22		27		33		39		47		56		68		82	
E6	10				15				22				33				47				68			

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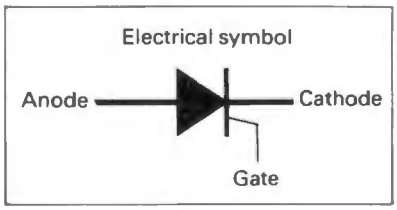
RS data

Thyristors

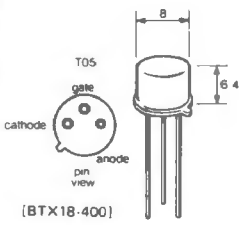
A range of thyristors for power control and similar applications.

Features

Device No.	RS Stock No.	V_{DRM}	V_{RRM}	$I_{T(AV)}$	I_{GT}	V_{GT}
BTX18-400	262-012	400 V	500 V	1.0 A	5 mA	2 V
BT106	261-249	500 V	700 V	1.0 A	50 mA	3.5 V
C106	261-817	400 V	400 V	2.55 A	0.2 mA	0.8 V
2N4443	261-946	400 V	400 V	5.1 A	30 mA	1.5 V
2N4444	262-034	600 V	600 V	5.1 A	30 mA	1.5 V
BT152-600	262-488	600 V	600 V	13 A	32 mA	1 V
BTY79-400R	261-255	400 V	400 V	6.4 A	30 mA	3 V
BTY79-800R	262-387	800 V	800 V	6.4 A	30 mA	3 V
THY500-12	261-514	500 V	500 V	12 A	60 mA	3 V
THY800-12	262-191	800 V	800 V	12 A	60 mA	3 V
THY1200-12	262-208	1200 V	1200 V	12 A	60 mA	3 V
THY500-26	261-520	500 V	500 V	26 A	40 mA	3 V
THY800-26	262-214	800 V	800 V	26 A	40 mA	3 V
THY500-40	261-889	500 V	500 V	40 A	60 mA	2.5 V
RS HIIC4	308-001	**Opto-coupled SCR – See RS Data 2135**				



Mechanical details



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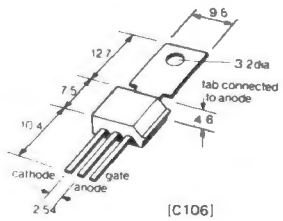
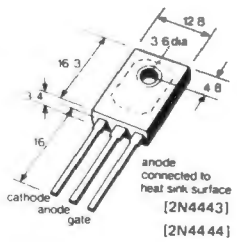
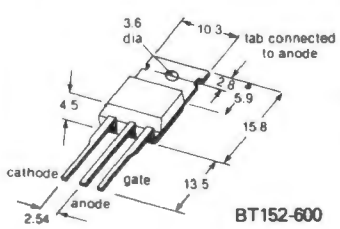


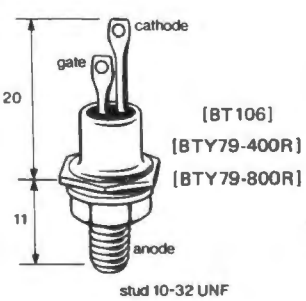
[C106]



[2N4443]
[2N4444]



BT152-600



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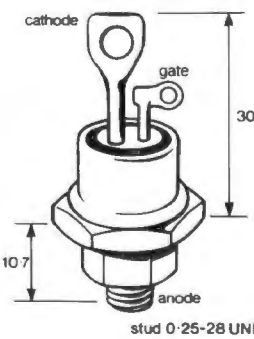
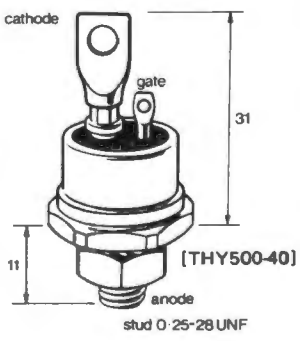
[BTY79-800R]
stud 10-32 UNF



[THY500-12]
[THY800-12]
[THY1200-12]
[THY500-26]
[THY800-26]
stud 0·25-28 UNF



[THY500-40]
stud 0·25-28 UNF

Absolute maximum ratings T_C = case temperature. T_j = junction. T_{amb} = ambient temperature

	Units	BTX 18 – 400	BT 106	C 106	2N 4443	2N 4444	THY 500 – 40
V_{DRM}	V	400 T_C = 125°C	500 T_C = 100°C	400 T_j = 110°C	400 T_j = 100°C	600 T_j = 100°C	500 T_j = 125°C
V_{RRM}	V	500 T_C = 125°C	700 T_C = 100°C	400 T_j = 110°C	400 T_j = 100°C	600 T_j = 100°C	500 T_j = 125°C
$I_{T(AV)\ 180°}$	A	1 T_C = 105°C	1 T_C = 90°C	2.55 T_j = 110°C	5.1 T_C = 73°C	5.1 T_C = 73°C	40 T_C = 85°C
I_{TSM}	A	10 Tj = 125°C	80 T_j = 100°C	20	80		500
di/dt	Aμs	100 Tj = 125°C	50 T_j = 100°C	50 T_j = 110°C	–		100
I_{FGM}	A	0.2	2	0.2	2		5
P_{GM}	W	0.5	5	0.5	5		20
$P_{G(AV)}$	W	0.05	0.5	0.1	0.5		1
T_j	°C	125	110	110	100		125

	Units	BTY 79 – 400R	BTY 79 – 800R	THY 500 – 12	THY 800 – 12	THY 1200 – 12	THY 500 – 26	THY 800 – 26	BT 152 – 600
V_{DRM}	V	400 T_C = 125°C	800 T_C = 125°C	500 T_C = 125°C	800 T_C = 125°C	1200 T_C = 125°C	500 T_C = 125°C	800 T_C = 125°C	600
V_{RRM}	V	400 T_C = 125°C	800 T_C = 125°C	500 T_C = 125°C	800 T_C = 125°C	1200 T_C = 125°C	500 T_C = 125°C	800 T_C = 125°C	600
$I_{T(AV)\ 180C°}$	A	6.4 T_C = 90°C		12A T_C = 85°C			26 T_C = 80°C		13
I_{TSM}	A	85 T_j = 125°C		200 T_j = 125°C			375 T_j = 125°C		200
d_1/dt	Aμs	20 T_j = 125°C		150 T_j = 125°C			175 T_j = 125°C		200
I_{FGM}	A	2		8			8		–
P_{GM}	W	5		25 for 100 μs			50 for 100 μs		20
$P_{G(AV)}$	W	0.5		1			1		0.5
T_j	°C	135		135			135		115

Electrical characteristics T_C = 25°C unless otherwise stated)

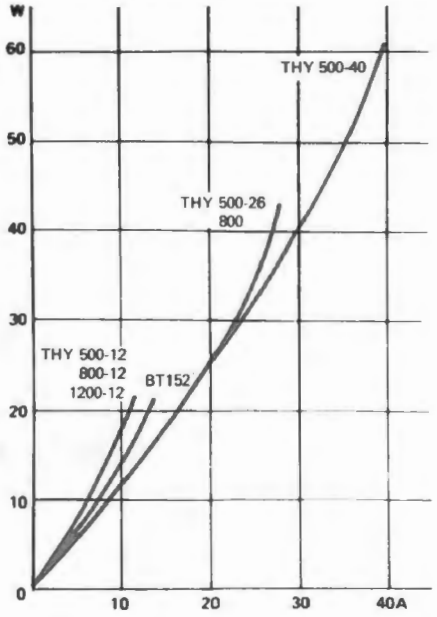
	Units	BTX 18 – 400				BT 106				C 106			
		condition	min	typ.	max	condition	min	typ.	max	condition	min	typ.	max
V_{TM}	V	at 1 A_{pk}	–	–	1.5	at 20 A_{pk}	–	–	2.3	at 4 A_{pk}	–	1.8	2.2
dv/dt	V μs	T_C = 125°C	20	–	–	T_C = 100°C	50	–	–	T_C = 110°C	–	8	–
I_H	mA		–	5	–		–	15	–		0.3	1	3
I_L	mA		–	6	–		–	20	–		0.3	1.5	4
I_{RRM}	mA		–	–	0.16	T_C = 100°C	–	–	1.5	T_C = 110°C	–	0.01	0.1
I_{DRM}	mA		–	–	0.16	T_C = 100°C	–	–	1.5	T_C = 110°C	–	0.01	0.1
V_{GT}	V		–	–	2		–	–	3.5		0.4	0.5	0.8
V_{GD}	V	T_C = 125°C	–	–	0.2	T_C = 100°C	–	–	0.25		–	0.3	–
I_{GT}	mA		–	–	5		–	–	50		–	0.03	0.2

	Units	2N 4443, 2N 4444				BT 152 – 600				BTY 79 – 400/800R				THY 500/800/1200 – 12			
		condition	min	typ.	max	condition	min	typ.	max	condition	min	typ.	max	condition	min	typ.	max
V_{TM}	V	at 5 A_{pk}	–	1	1.5	at 40A_{pk}	–	–	1.75	at 20 A_{pk}	–	–	2.3	at 32 A_{pk}	–	–	2
dv/dt	V μs	T_j = 100°C	–	50	–	T_j = 115°C	–	–	200	T_C = 125°C	50	–	–	T_C = 125°C	200	–	–
I_H	mA		–	6	40		–	–	60		–	15	–		–	25	–
I_L	mA			–			–	–	80		–	20	–		–	42	300
I_{RRM}	mA	T_j = 100°C	–	–	2	T_j = 115°C	–	–	1	T_C = 125°C	–	–	2.5	T_C = 125°C	–	–	5
I_{DRM}	mA	T_j = 100°C	–	–	2	T_j = 115°C	–	–	1	T_C = 125° C	–	–	2.5	T_C = 125°C	–	–	5
V_{GT}	V		–	0.75	1.5		1	–	–		–	–	3		–	1.2	3
V_{GD}	V			–		T_j = 115°C	–	–	0.25	T_C = 125°C	–	–	0.25	T_C = 125°C	–	–	0.25
I_{GT}	mA		–	7	30		32	–	–		–	–	30		–	35	60

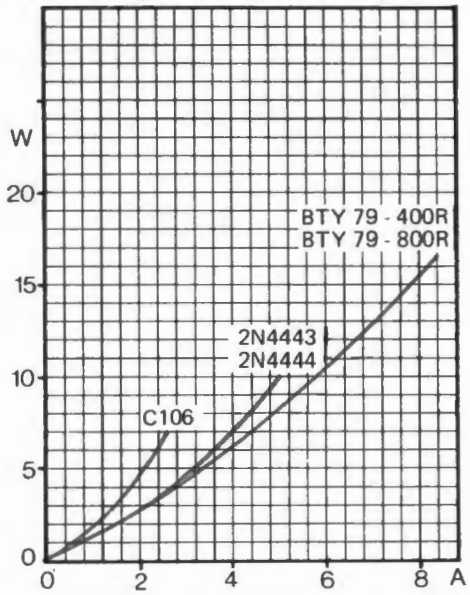
	Units	THY 500/800 – 26				THY 500 – 40			
		condition	min	typ.	max	condition	min	typ.	max
V_{TM}	V	at 75 A_{pk}	–	–	1.85	at 126 A_{pk}	–	–	1.7
dv/dt	V μs	T_C = 125°C	200	–	–		200	–	–
I_H	mA		–	25	–		–	–	100
I_L	mA		–	49	300		–	–	100
I_{RRM}	mA	T_C = 125°C	–	–	5		–	–	10
I_{DRM}	mA	T_C = 125°C	–	–	5		–	–	10
V_{GT}	V		–	1.04	3		–	–	2.5
V_{GD}	V	T_C = 125°C	–	–	0.25		–	–	0.25
I_{GT}	mA		–	25	60		–	–	60

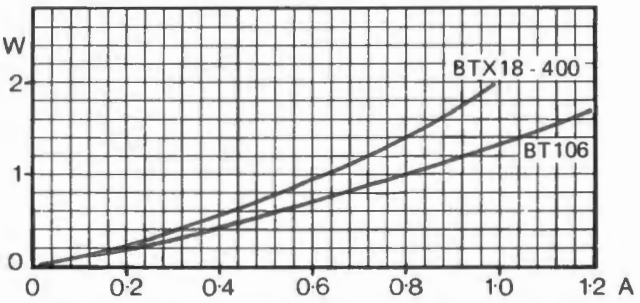
Thermal characteristics

	BTX 18 – 400	BT 106	C 106	2N 4443, 2N 4444	BT 152 – 600	BTY 79 – 400/ 800R	THY 500/ 800/1200 – 12	THY 500/ 800 – 26	THY 500 – 40
θ_j to case °C/W	10	3.1	10	2.5	1.1	3.1	1.8	1.1	0.5
θ_j to amb ° C/W	200	40	80	40	–	–	–	–	–

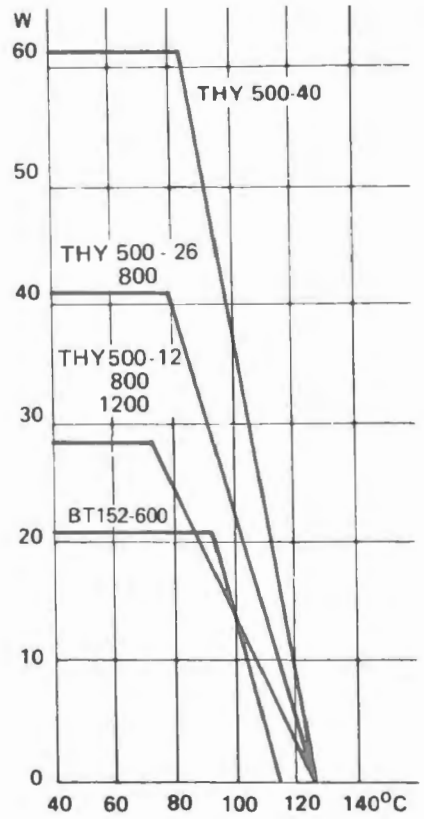


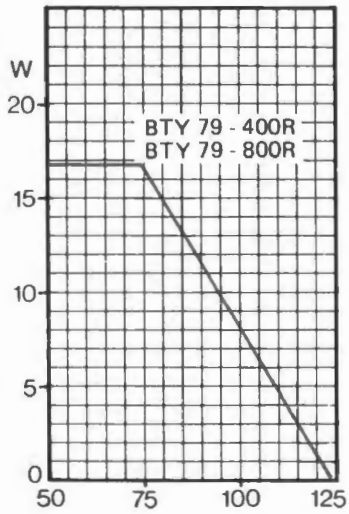
Power dissipation v average current (180° sine conduction)

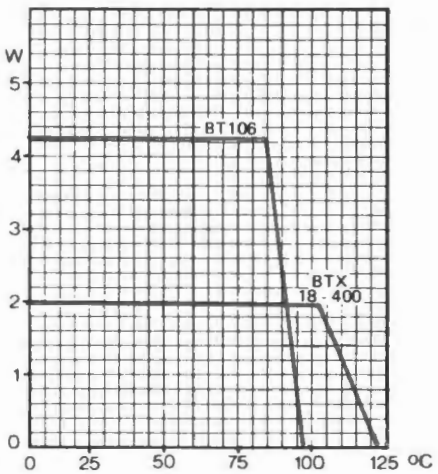




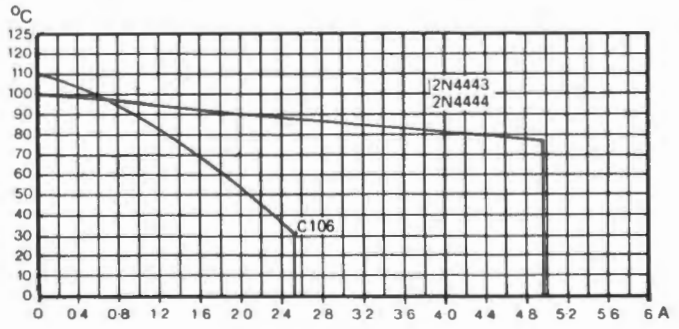
Power dissipation v case temperature (180° sine conduction)







Maximum allowable case temperature (180° sine conduction)

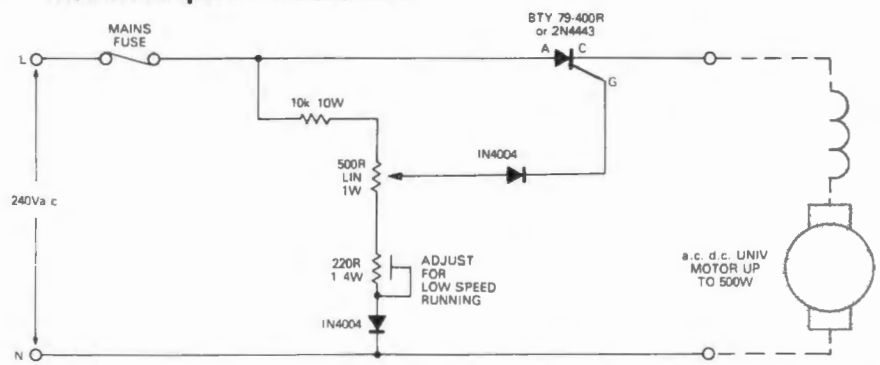


RS data

Applications

The circuit in figure 1 gives reasonable speed control on AC-DC universal motors, with good torque characteristics due to the feedback provided by the motor. It is thus suitable for use with motors subject to varying load conditions such as electric drills. Not suitable for use with induction or synchronous motors.

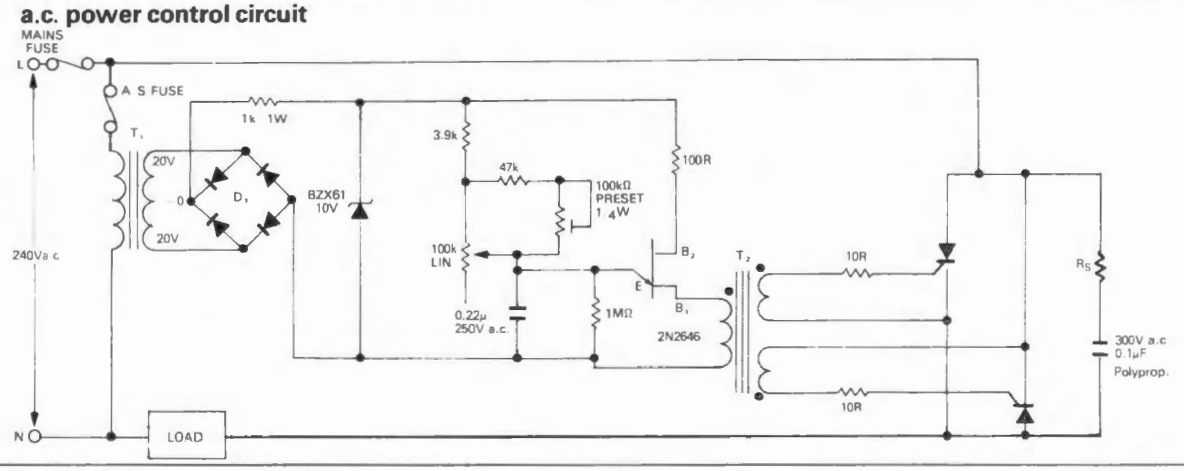
Figure 1 **Half wave speed control circuit**



Notes
(1) The Thyristor should be mounted on a 4° C/W heatsink (401-497)
(2) With a lightly loaded motor running at slow speed some erratic rotation may be experienced. This results from feedback induced 'skip-cycling' and can be eliminated by adjustment of the 220 Ω preset.

The circuit in figure 2 features a parallel inverse pair of thyristors with improved surge current capability and better dv/dt characteristics than an equivalent triac circuit. It is thus suitable for industrial control applications and the dimming of large incandescent filament lamps such as stage spot lamps. Care should be taken that the selected thyristor caters for maximum worst case load conditions.

Figure 2 **a.c. power control circuit**



Ratings for Ta ⩽ 35°C				
Max. Resistive/ Inductive Load Current	**Max. Lamp Load**	**S.C.R. Type**	**Heatsink per S.C.R.**	**Basic Values of RS**
75A	6000W	40A, 500V (261-889)	1.1° C/W (401-807)	47Ω
40A	4500W	26A, 500V (261-520)	2.1° C/W (401-403)	47Ω
24A	2000W	12A, 500V (261-514)	2.1° C/W (401-403)	68Ω
12A	1000W	6.4A, 400V (261-255)	4° C/W (401-497)	100Ω
10A	750W	2N4443 (261-946)	4° C/W (401-497)	100Ω

Notes
T_1:20-0-20V 30mA (196-280)
T_2.Pulse Transformer (196-375)
D_1:1.6A, 200V Bridge (261-491)
Except where indicated resistors are ½ W types.

Notes on circuits
These circuits are intended to serve as an introduction to RS SCRs and their possible applications.
However RS cannot undertake further design or modifications to these circuits for specific applications, nor the testing of completed circuits.
Attention is drawn to the care needed to select suitable fuses to protect the SCRs used and also the need in some situations to suppress the radio frequency interference (RFI) produced by these circuits to meet legal requirements. Both these points depend on the actual circuit conditions and specific recommendations cannot be made. When purchasing components refer to the current RS Components catalogue for details of device specifications, prices and Stock Numbers.

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RS data

Thermistors

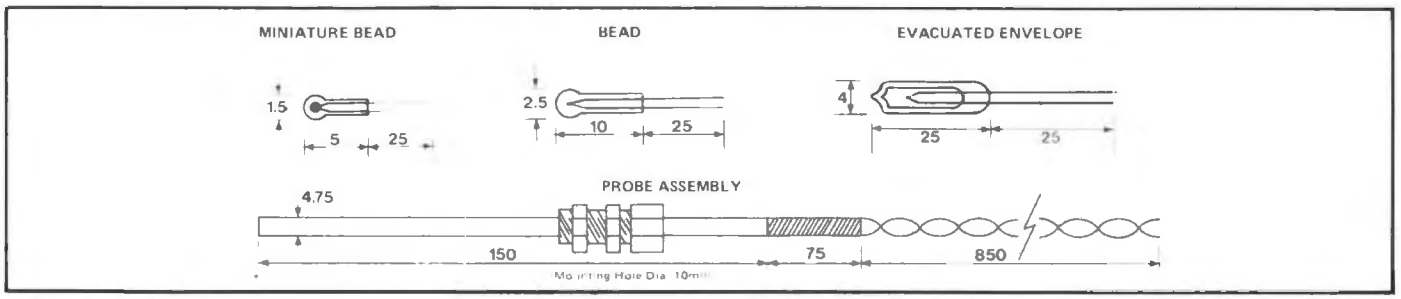
NTC Thermistors

The RS range of NTC thermistors includes standard tolerance negative temperature coefficient thermistors, plus a range of small close tolerance R/T curve matched thermistors.

Standard Tolerance Thermistors

A range of 9 negative temperature coefficient bead thermistors constructed from a compound of nickel mangenite. Six types sealed in glass together with two stainless steel probe assemblies designed primarily for temperature measurement and control, flow measurement and liquid level detection. The remaining type, suspended in an evacuated glass envelope, is designed for applications in amplitude control, temperature compensation and time delay circuits.

		Miniature beads				Beads		Probe ass.		Evac type
Characteristic Resistance	**UNITS**	151-136	151-142	151-158	151-164	151-029	151-013	151-120	151-170	151-114
R_{BEAD} 20°C	Ω	—	—	—	—	2k	1M	—	—	5k
25°C	Ω	1k	4.7k	47k	470k	—	—	4.7k	1.0M	—
R_{MIN} (HOT)	Ω	59	271	338	440	115	170	500	800	79
R_{BEAD} TOLERANCE	%	±20	±20	±20	±20	±20	±20	±2	±2	±20
T_A max ambient temp range maximum dissipation	°C	−80 to +125	−80 to +125	−60 to +200	−25 to +300	−80 to +300	−25 to +300	−30 to +100	−30 to +250	0 to +155
Maximum dissipation	mW	70	70	120	190	130	340	50	50	3·0
Derate to zero at	°C	125	125	200	300	125	300	100	250	225
Dissipation constant	mW/°c	0.7	0.7	0.7	0.7	1.2	1.2	5.0	5.0	12.5×10^{-3}
Thermal time constant	s	5	5	5	5	19	19	180	180	11
B constant (25 to 100 C)	°K	3000	3390	3980	4320	3200	4850	3275	5000	3250
B tolerance	%	±3	±3	±3	±3	±5	±5	±2	±2	±5
Equivalent types		GM102 VA3400	GM472 VA3404	GM473 VA3410	GM474	GL23	GL16	JA03	JA09	RA53



Basic Formulae

The temperature coefficient α at any temperature within the operating range may be obtained from the formula:-

$$\alpha = -\frac{B}{T^2} \text{ (per °C)}$$

To determine the resistance at any temperature within the operating range may be obtained from the formula:-

$$R_2 = R_1 \cdot e^{\left(\frac{B}{t_2} - \frac{B}{t_1}\right)}$$

where

B = characteristic temperature constant (°K)

T = bead temperature in (°K)

R_1 = resistance of thermistor at temperature t_1(Ω)

R_2 = resistance of thermistor at temperature t_2(Ω)

e = 2.7183

(Temperature in °K = temperature in °C + 273)

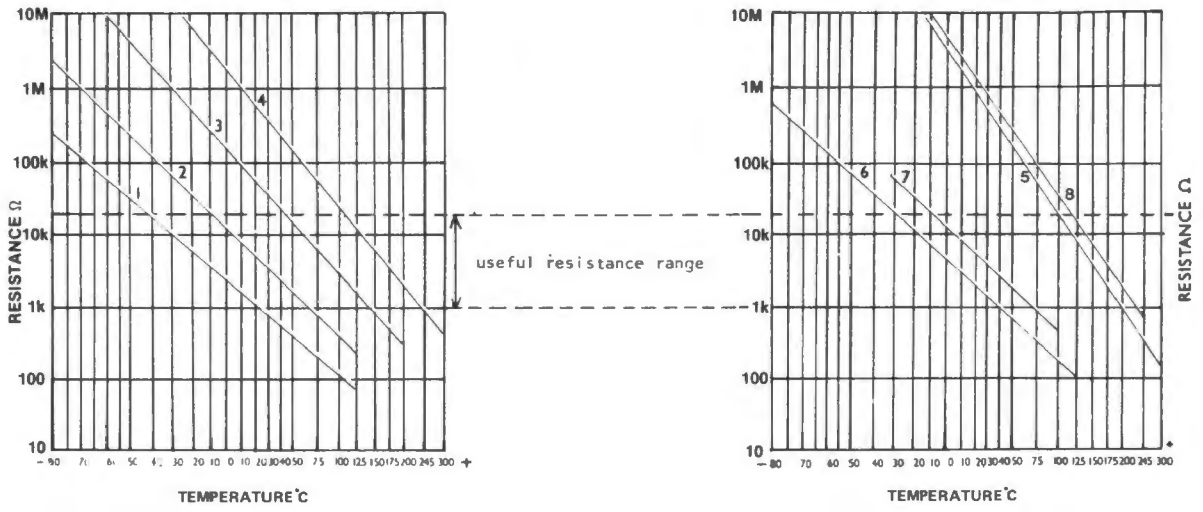
Application Notes

Typical applications include temperature control of ovens, deep freezers, rooms and for process control, etc. Can also be used to drive high and low temperature alarms.

In the basic circuit below, calibration should be carried out by comparison with a known standard (e.g. a thermometer or thermocouple). In the case of 0°C a mixture of ice and water can be used and for 100°C use boiling water.

Note than non-linearity should be expected at extended temperatures.

Figure 1 **Graphs of resistance Vs temperature at zero power**



Key

Miniature Beads	Beads	Envelope
1) 151-136	5) 151-013	9) 151-114
2) 151 142	6) 151-029	
3) 151 158	Probes	
4) 151-164	7) 151-120	
	8) 151-170	

Figure 2 **Graph of voltage Vs current for evacuated envelope type**

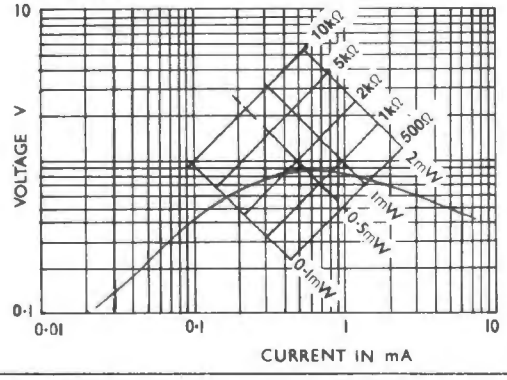


Figure 3 **Basic temperature measuring circuit and add- on temperature controller**

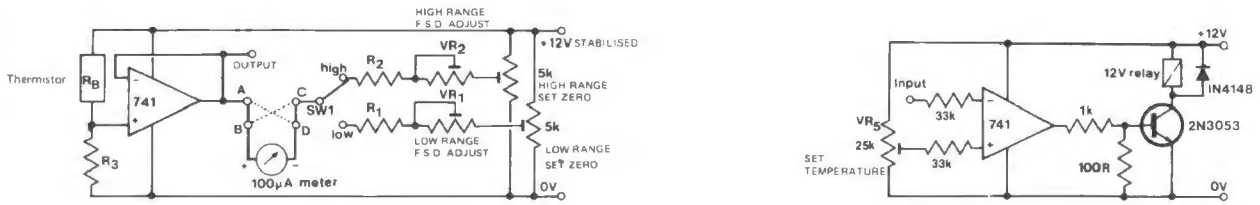


Table 1 Typical Resistor Values for Temperature Measuring Circuit (above)

Thermistor		Temperature in (°C)		Resistor values (kΩ)				
		LOW	HIGH	R_1	R_2	R_3	VR_1	VR_2
Miniature	151-136	0 to −60 *	0 to 30	56	6.8	22	50	5
	151-142	0 to 30	0 to 100	18	33	22	10	20
	151-158	50 to 100	100 to 150	27	8.2	22	10	5
	151-164	150 to 200	200 to 250	12	3.9	22	5	2
Beads	151-029	0 to −30 *	0 to 30	27	10	22	20	5
	151-013	100 to 150	150 to 200	39	8.2	22	20	5
Probe Assy.	151-120	0 to −30 *	0 to 100	33	33	22	20	20

NOTE
*For negative ranges reverse meter by linking A to D and B to C

R-T Curve Matched Thermistors

A range of high quality precision curve matched thermistors, available in four characteristic resistances. They offer true interchangeability over a wide temperature range and eliminate the need for individual circuit adjustments or padding. These thermistors provide accurate and stable temperature sensing capability for applications such as temperature measurement and compensation.

Table 2 Resistance/temperature characteristics

RS Stock No. **151-215**		RS Stock No. **151-221**		RS Stock No. **151-237**		RS Stock No. **151-243**	
Temp C	Res. Ω	Temp C	Res. Ω	Temp C	Res. Ω	Temp C	Res. Ω
−80	2,210,400	−80	3,684,000	−80	7,368,000		
−70	935,250	−70	1,558,800	−70	3,117,500		
−60	421,470	−60	702,450	−60	1,404,900		
−50	201,030	−50	335,050	−50	670,100		
−40	100,950	−40	168,250	−40	336,500	−40	4,015,500
−30	53,100	−30	88,500	−30	177,000	−30	2,064,000
−20	29,121	−20	48,535	−20	97,070	−20	1,103,400
−10	16,599	−10	27,665	−10	55,330	−10	611,870
0	9,795.0	0	16,325	0	32,650	0	351,020
10	5,970.0	10	9,950.0	10	19,900	10	207,850
20	3,747.0	20	6,245.0	20	12,490	20	126,740
25	3,000.0	25	5,000.0	25	10,000	25	100,000
30	2,417.1	30	4,028.5	30	8,057.0	30	79,422
40	1,598.1	40	2,663.3	40	5,327.0	40	51,048
50	1,080.9	50	1,801.5	50	3,603.0	50	33,591
60	746.40	60	1,244.0	60	2,488.0	60	22,590
70	525.60	70	876.00	70	1,752.0	70	15,502
80	376.50	80	627.50	80	1,255.0	80	10,837
90	274,59	90	457.65	90	915,30	90	7,707.7
100	203.49	100	339.15	100	678.30	100	5,569.3
110	153.09	110	255.15	110	510.30	110	4,082.9
120	116.79	120	194.65	120	389.30	120	3,033.3
130	90.279	130	150.47	130	300.93	130	2,281.0
140	70.581	140	117.64	140	235.27	140	1,734.3
150	55.791	150	92.985	150	185.97	150	1,331.9

Dimensions (mm)

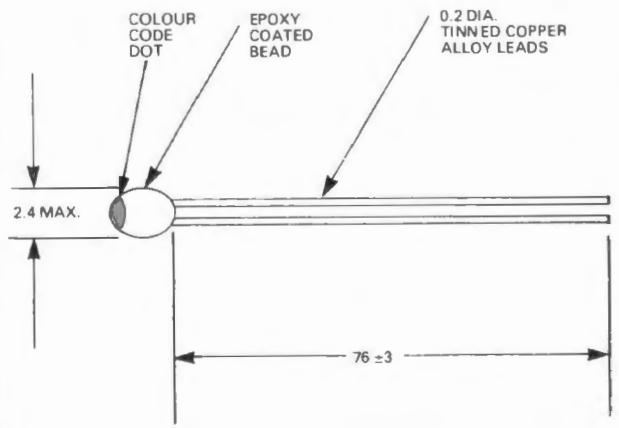


Table 3 **Electrical characteristics**

RS Stock No	151-215	151-221	151-237	151-243
Colour Code Dot	**Red**	**Orange**	**Yellow**	**Violet**
Resistance at 25°C	3kΩ	5kΩ	10kΩ	100kΩ
Temperature Range	−80°C to +150°C			
Tolerance (0 to 70°C)	±0.2°C			
Dissipation Constant	1mW			
Time Constant	10s			

Definitions

Dissipation constant. Represents the amount of power required to raise the temperature of the thermistor. 1 C above its ambient temperature, expressed in milliwatts.

Time constant. The time required for the thermistor dissipating zero power is change 63% of the difference between its initial temperature value and that of a new impressed temperature environment.

PTC Thermistors

The RS range of PTC thermistors includes three types for over-temperature protection and three types for over-current protection.

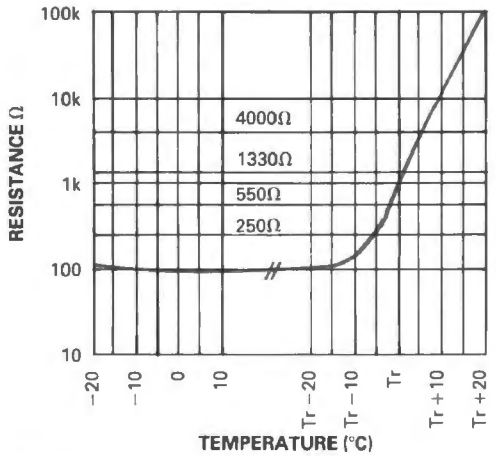
Over-temperature Protection

A range of three positive temperature coefficient (PTC) thermistors, manufactured from a compound of barium lead and strontium titanates. The range consists of two disc types and one stud mounted version. These devices are primarily designed for temperature sensing and protection of semiconductor devices, transformers and motors etc. As can be seen from the resistance/temperature characteristic of fig. 6, the resistance of the PTC thermistor is low and relatively constant at low temperatures. As the ambient temperature increases, the resistance rises. The rate of increase becomes very rapid at the reference temperature (Tr) of the device. Tr is also known as the threshold, critical or switching temperature. Above Tr the characteristic becomes very steep and attains a high resistance value.

Specification		Stud	Disc
RS Stock Nos.		158-250	158-266 158-272
Maximum operating and storage temperature		155°C	Tr + 100°C
Minimum operating and storage temperature		−20°C	−55°C
Typical thermal resistance (embedded)	(1)	—	0.05°C/mW
Typical dissipation constant (embedded)	(1)	—	20mW/°C
Maximum power dissipation at 25°C	(2)	—	690mW
Maximum applied voltage at 25°C	(2)	—	40V
Insulation between stud and lead		500V d.c.	—
Typical resistance at or below Tr −20°C		100Ω	
Maximum resistance at or below Tr −20°C		250Ω	
Maximum resistance at Tr −5°C	(3)	550Ω	
Typical resistance at Tr	(3)	1000Ω	
Minimum resistance at Tr +5°C	(3)	1330Ω	
Minimum resistance at Tr + 15°C	(4)	4000Ω	

Notes
(1) Dependent on method of insulation and mounting
(2) Self heating in free air
(3) Measured at 2.5V d.c.
(4) Measured at 7.5V d.c.

Figure 6



Resistance temperature graph

Calibration

Calibration should be carried out by heating the thermistor to the appropriate reference temperature and adjust R_2 such that the appropriate L.E.D. lights.

Series Connection

In temperature sensing circuits two or more devices may be connected in series. The sensing circuit will then indicate if any of the thermistors exceeds the reference temperature. An increase in the value of R_1 may be necessary to compensate for the additional volt drop across the thermistor.

Figure 4

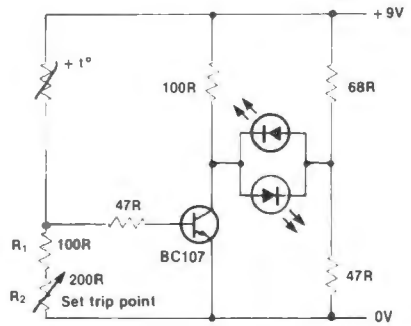
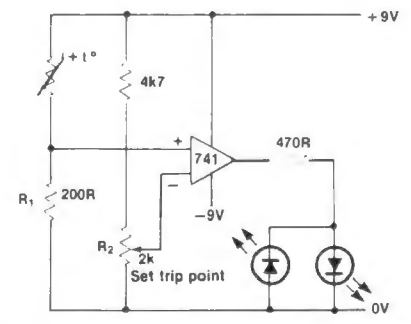


Figure 5



Application Notes

Basic Temperature Sensing Circuits

Figure 4 shows a basic circuit which indicates when the temperature of the PTC thermistor is below Tr (i.e. safe operation) and will also indicate when Tr is exceeded. When both LEDs are off this indicates the Tr is being approached (approx. Tr −5°C).

Figure 5 shows a circuit which has a more defined 'trip point' than Figure 4 (set by R_2).

Over-current Protection

Switching type Positive Temperature Coefficient (PTC) thermistors are prepared from compounds of barium, lead and strontium titanates to give a ceramic disc. Electrical contacts are made by the metallising of the disc faces using nickel, silver, etc; the completed disc is then provided with soldered lead wires.

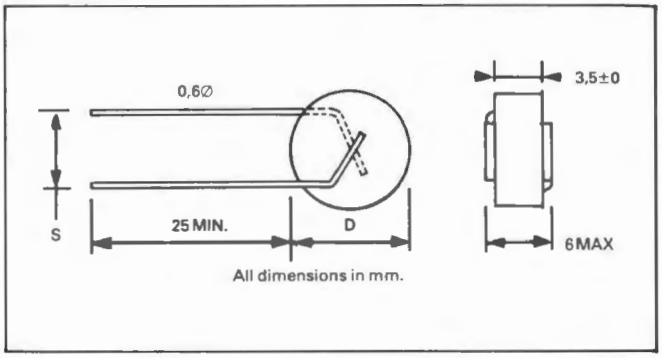
Definition of terms

R_{min} – Resistance of PTC at lowest point of R v T curve.
R_{25} – Resistance of PTC at 25°C.
I_{max} – Current value at turnover point of I/V curve at a specified temperature.
I_{rest} – Current value at V_{max}.
I_{peak} – Maximum allowable current through PTC.
V_{max} – Maximum voltage that may be applied to thermistor.

Specification

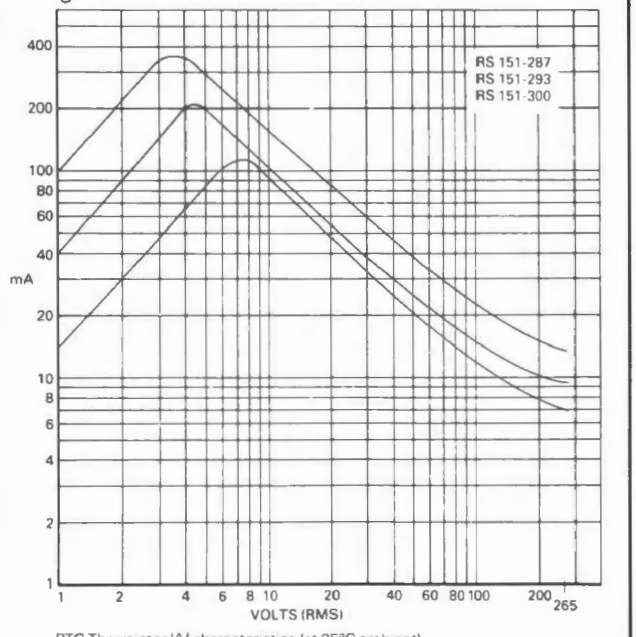
Ratings
Resistance tolerance at 25°C ..... ±25%
V_{max} ..... 265V rms

Ambient temperature range
Operating ..... 0-55°C
Storage ..... –40 to +155°C



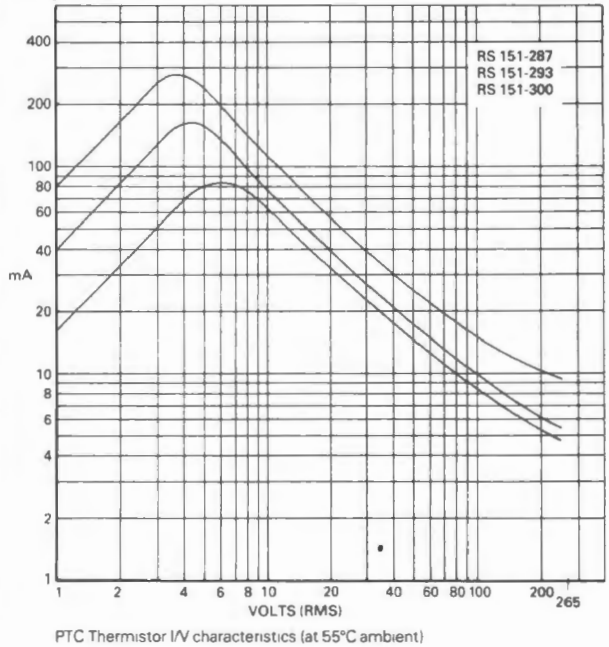
RS stock No	Switch	I_{max} (Typ.) 25°C	I_{max} (Typ.) 55°C	I_{REST}	I_{PEAK}	Rs MIN	@ < 1mA d.c. R_{25}	@ < 1mA d.c. R_{120}	@ < 1mA d.c. R_{155}	Dimensions (mm) D	Dimensions (mm) S
151-287	125°C	350	280	<11,5	1,65A	150Ω	10	< 30	> 30k	15	5
151-293		200	155	< 8,0	815mA	300Ω	25	< 80	> 80k	10	5
151-300		110	86	< 7,0	250mA	1kΩ	70	<218	>220k	6	5

Figure 7



PTC Thermistor I/V characteristics (at 25°C ambient)

Figure 8

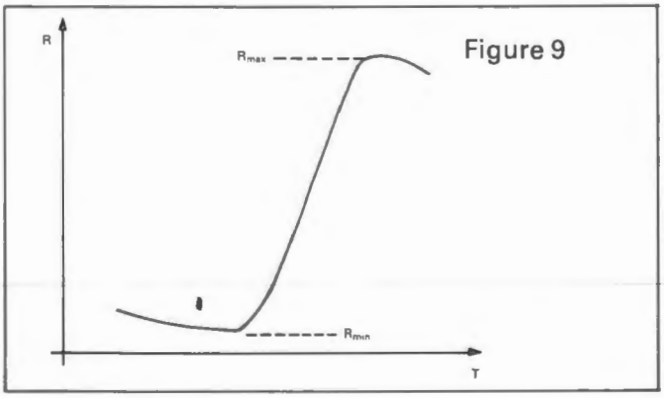


PTC Thermistor I/V characteristics (at 55°C ambient)

Theory of operation

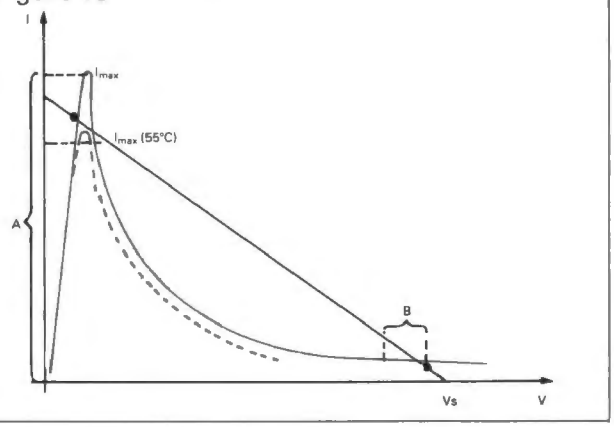
The shape of the PTC thermistor resistance vs temperature characteristic, (Figure 9) can be considered in three distinct parts. The region from below 0°C to R_{min} has a negative temperature coefficient of the order of 1%/°C; the region from R_{min} to R_{max} has a positive temperature coefficient in which values as high as 100%/°C can be realised. Beyond R_{max} the TC is again negative. As a PTC Thermistor is sensitive to voltage variation, R v T curves are usually measured at a constant voltage. Figure 10 shows the characteristics of the load to be protected, together with the I/V of the thermistor on a linear scale. Region 'A' indicates the permissible load current range for normal operation. An increase in load current beyond the I_{max} value will cause the thermistor to self-heat to a high resistance state thereby shifting its operating point to the region B. This reduces the current through and voltage across the load, effectively protecting the equipment etc.

Figure 9



RS data

Figure 10



Similarly, if the ambient temperature surrounding the thermistor should, due to a fault condition, increase, the I/V curve will depress towards the dotted position. The load attempts to consume more than I_{max} (55°C) and the thermistor will again self-heat and shift its operating point into the low current region.

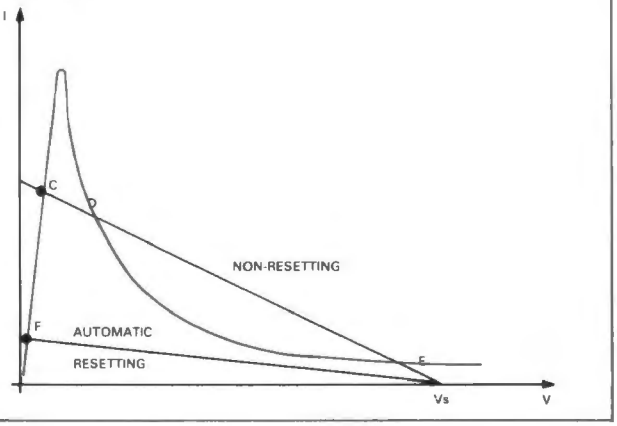
Selection

In order to ensure that the load is protected at the desired level and in the required reset mode, the following parameters must be taken into account:

1. Normal operating current range – Region 'A'.
2. 'Overload' current – I_{max}.
3. Operating temperature range – I/V curve shift.
4. Operating voltage range, (Vs).
5. Time response – position in Region 'A'.
6. Thermistor tolerances.
7. Permissible voltage drop across device.
8. Mounting arrangement.

The reset mode required, i.e. return to the 'A' region, is decided by the position of the load line in relation to the I/V curve. Figure 11 shows load line positions for the two modes, the auto-reset line intersects the I/V curve at only one point (F), thereby restricting stable operation to this point for normal load conditions. The manual or non-resetting line crosses the I/V curve at three positions, giving the possibility of operation at either point. However, point D is in an unstable region so that in practice operation only occurs at points C or E.

Figure 11



If response time is a particularly important factor, the position of the operating point within region 'A', for a given device, (Figure 10) and the switch temperature of the PTC must be carefully considered. In circumstances where the circuit being protected is subject to short term overloads (which may be tolerated), the operating point should be the lower portion of region 'A'. Alternatively, where response time must be rapid, the operating point must be as close to the I_{max} value as practicable, not forgetting the shift in characteristic with temperature.

Tolerances are usually quoted on the room temperature resistance (zero power), the higher values of R_{25} giving the lower I_{max}.

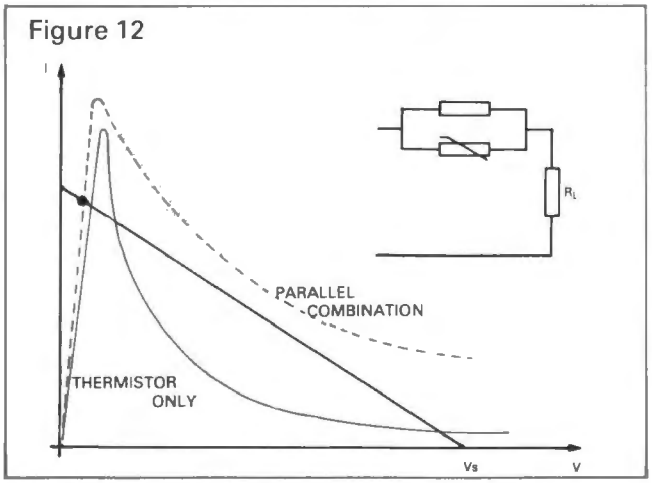
As a thermistor is a resistive device there will inevitably be a voltage drop across it when in circuit. The maximum permissible voltage drop for the circuit concerned will dictate the room temperature or R_{25} resistance value. It is usual to make the R_{25} value in the order of 10% of the circuit resistance (or impedance).

The thermistor should be positioned in the equipment such that the surrounding air is reasonably still and unconfined. Moving air will effectively increase the I_{max} value (at a given temperature) whilst confining the device will create a high ambient temperature, and therefore a lower I_{max}.

Modification of I/V characteristics

In certain applications it is necessary to modify the I/V curve in order to produce the necessary characteristics. To obtain an auto-resetting device with a relatively high current rating, a resistor may be connected in parallel with the thermistor to 'lift' the characteristic to the dotted position, (Figure 12). This permits the load line to occupy a position in the upper 'A' region, but still crossing the combination curve at one stable point.

Figure 12



Parallel operation

In instances where a sufficiently high I_{max} value cannot be realised with existing devices, it is permissible to parallel connect two or more devices to achieve the required values; this may also be used to obtain lower R_{25} resistances.

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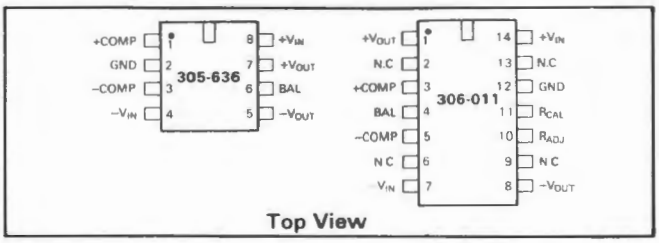
RS data

Dual regulators

Stock numbers 305-636,306-011

Two monolithic regulators in D.I.L. packages fixed or variable complementary outputs.

Pin-out diagrams



Top View

Features

- Output currents up to 100 mA
- Internal current limiting
- Thermal shutdown feature
- Fixed voltage ±15 V **(305-636)**
- Variable voltage ±0.5 to ±30 V **(306-011)**

Fixed 305-636

Absolute maximum ratings at T_{AMB} 25 °C

Input voltage	±30 V
Power dissipation	600 mW
Junction temperature	+175 °C
Storage temperature	−65 to +175 °C

Electrical characteristics

at T_J = 25°C, V_{IN} ±20V, C_o = 10 μF, I_o = ±1mA; unless otherwise stated .

	305 – 636			
Parameter	**Min**	**Typ**	**Max**	**Unit**
V_{out} (positive or negative wrt GND)	±14.5	±15.0	±15.5	V
V_{IN} (positive or negative wrt GND)	±18	–	±30	V
Input/Output Diff. Voltage @ 50 mA	3	–	–	V
Output Voltage Balance	–	±0.3	±1.8	$\%V_{out}$
Line Regulation	–	0.01	0.1	$\%V_{out}$
Load Regulation (to 100 mA)	–	0.03	0.2	$\%V_{out}$
Ripple Rejection	–	75	–	dB
Output Voltage Temp. Coeff.	–	0.005	0.005	%/°C
Short Circuit Current (set internal)	–	220	–	mA
Standy-by Current $\pm I_o = 0$	–	1.5	3.0	mA
Output Noise Voltage 100 Hz – 10 kHz	–	60	–	μV rms
Internal Shutdown Temp.	–	175	–	°C

Variable 306-011

Absolute maximum ratings at T_{AMB} 25 °C

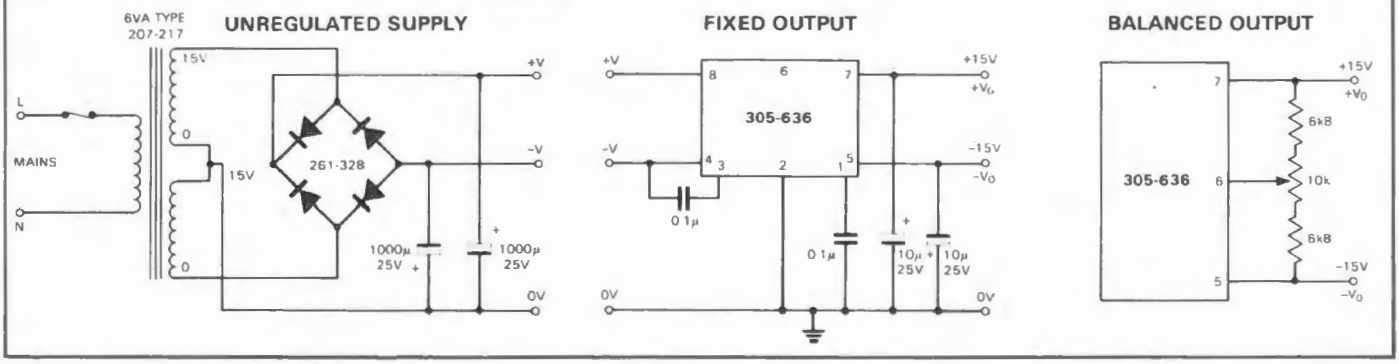
Input voltage	±35 V
Power dissipation	900 mW
Junction temperature	+175 °C
Storage temperature	−65 to +175 °C

Electrical characteristics

at T_J = 25°C, V_{IN} ±20 V, C_o = 10 μF, I_o = ±1mA; unless otherwise stated .

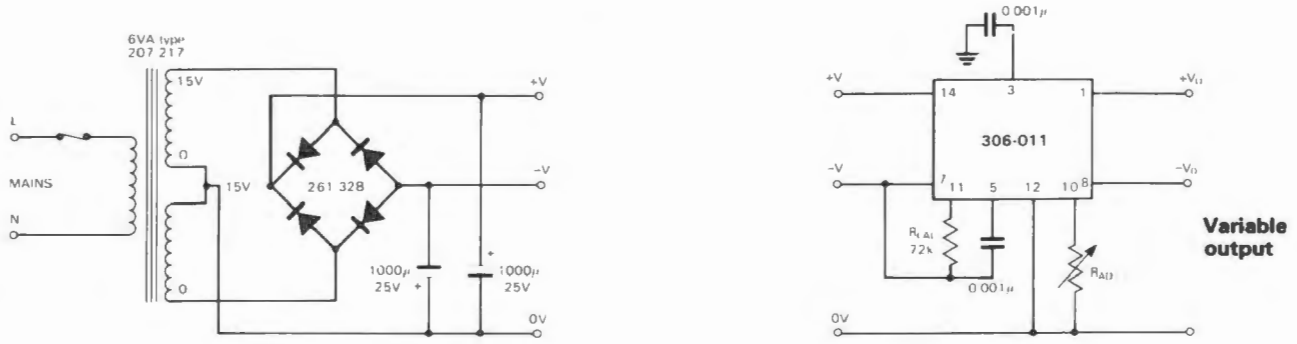
	306 – 011			
Parameter	**Min**	**Typ**	**Max**	**Unit**
V_{out} (positive or negative wrt GND)	±0.05	–	±30	V
V_{IN} (positive or negative wrt GND)	±9.5	–	±35	V
Input/Output Diff. Voltage @ 50 mA	3	–	–	V
Output Voltage Balance	–	±1.5	–	$\%V_{out}$
Line Regulation	–	0.02	0.2	$\%V_{out}$
Load Regulation (to 100 mA)	–	0.1	0.4	$\%V_{out}$
Ripple Rejection	–	70	–	dB
Output Voltage Temp. Coeff.	–	0.015	–	%/°C
Short Circuit Current (set internal)	–	300	–	mA
Standy-by Current $\pm I_o = 0$	–	1.2	3.0	mA
Output Noise Voltage 100 Hz – 10 kHz	–	250	–	μV rms
Internal Shutdown Temp.	–	175	–	°C

Figure 1 **Basic diagram for fixed output regulator**



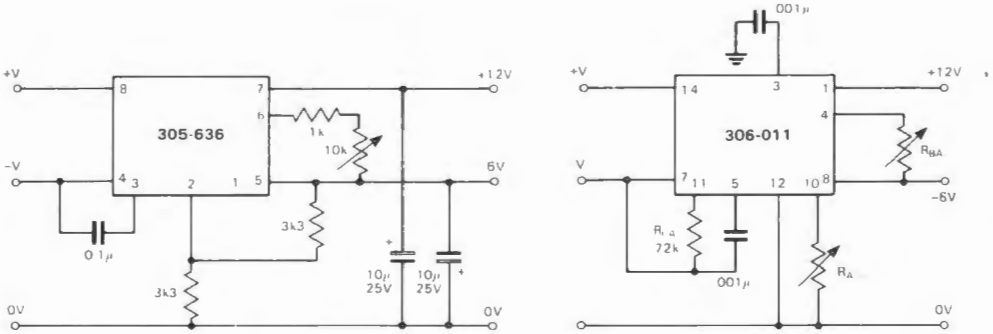
RS data

Figure 2 **Basic diagram for variable output regulator**



R_{CAL} is equivalent to (120kΩ +180kΩ) in parallel
R_{ADJ} = 2.5kΩ per Volt output
(For ±15V use 50kΩ lin. pot)

Figure 3 **Modifications to give non-symmetrical operation**



Note
+ 12V and −6V are typical requirements for RS 710 comparator i.c.

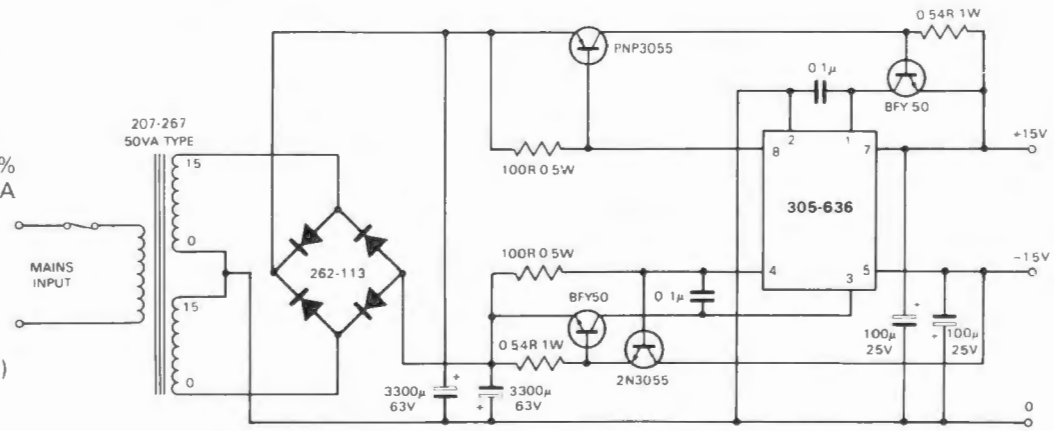
R_{ADJ} = 2.5kΩ per Volt of output
R_{ADJ} for -6V = 15kΩ, then
R_{BAL} for +12V = 20kΩ

Figure 4 **Typical current boost circuit for ±15 V, 1A**

Performance at 20°C T_{amb}

I_O	±1A
Load reg. (0-1A)	1.1%
Ripple rejection	60db
Line reg. (18-30V)	0.065%
Current limit	±1.02A

Heatsinks for each 3055 transistor 4°C/W (401-497)
0.54Ω limit resistors are 2 x 0.27Ω½W in series.



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RS data

Light dependent resistor ORP12

Stock number. 305-620

A Cadmium Sulphide photo-conductive cell with a spectral response similar to that of the human eye, making it ideal for visible light sensing circuits. The cell resistance falls with increasing light intensity and follows a logarithmic law. Applications include smoke detection, automatic lighting control, batch counting and burglar alarm systems, etc.

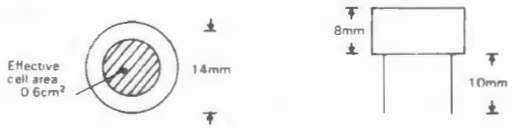
Features

- Wide spectral response
- Sensitive to wide range of light intensities

Absolute maximum ratings

Cell Voltage, d.c. or a.c. peak _____ 110V
Cell dissipation * _____ 220mW
Ambient temperature range _____ −10 to +60°C
* Derate by 10mW/°C above 40°C

Dimensions

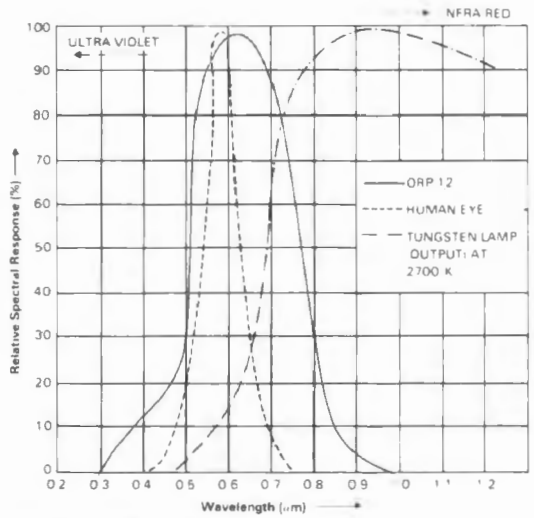


Electrical characteristics

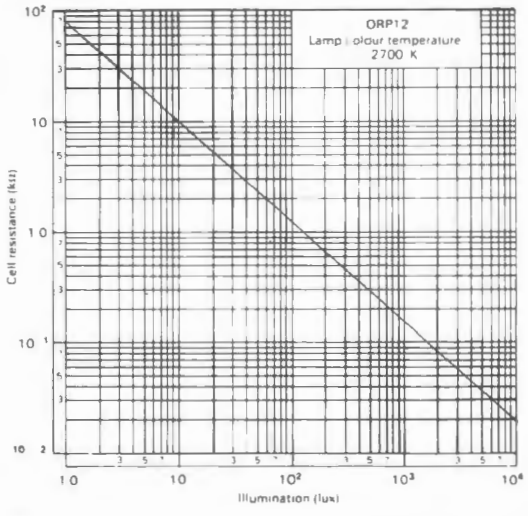
T_A = 25°C. 2700°K tungsten light source

Parameter	Symbol	Conditions	Typical Value	Units
Cell resistence	R_{CELL}	1000 lux	150	Ω
		50 lux	2.4	kΩ
		dark	≥10	MΩ
Rise time of R_{CELL}	t_R	50 lux to dark	75	ms
Fall time of R_{CELL}	t_F	dark to 50 lux	350	ms

Spectral response



Cell resistance v illumination



Guide to source illuminations

Light source	Illumination (Lux)
Moonlight	0.1
60W bulb at 1m	50
1W M.E.S. bulb at 0.1m	100
Fluorescent lighting	500
Bright sunlight	30,000

Circuit symbol

RS data

Typical application circuits

Figure 1 **Simple light operated relay suitable for use with RS miniature relays**

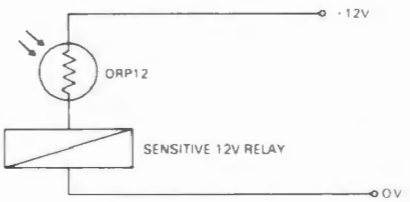
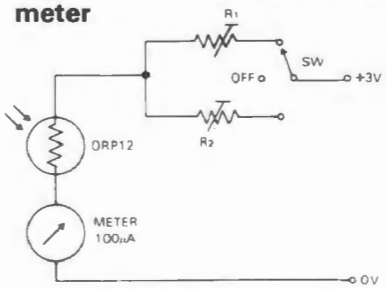
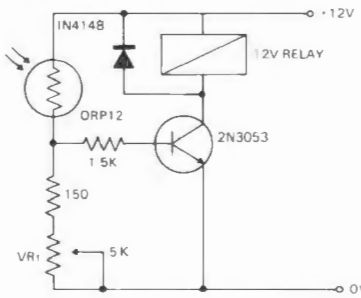


Figure 2 **Logarithmic Law photographic light meter**



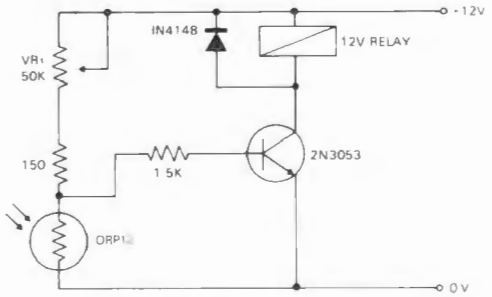
Typical value $R_1 = 100\Omega$
$R_2 = 200\Omega$ preset to give two overlapping ranges. (Calibration should be made against an accurate meter).

Figure 3 **Sensitive light operated relay**



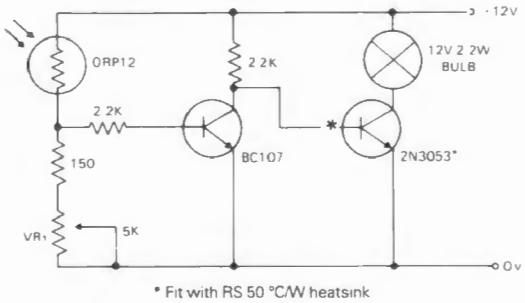
Relay energised when light level increases above the level set by VR_1

Figure 4 **Light interruption detector**



As Figure 3 relay energised when light level drops below the level set by VR_1

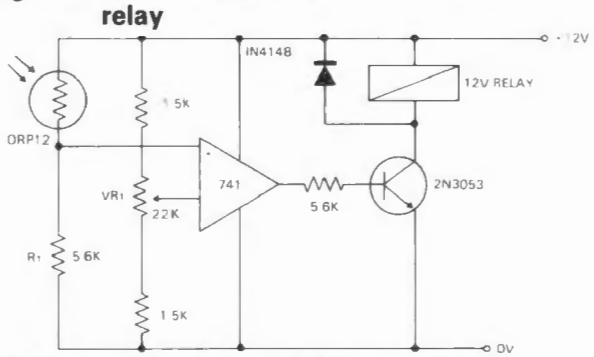
Figure 5 **Automatic light circuit**



* Fit with RS 50 °C/W heatsink

Adjust turn-on point with VR_1

Figure 6 **Extremely sensitive light operated relay**



(Relay energised when light exceeds preset level). Incorporates a balancing bridge and op-amp. R_1 and ORP12 may be interchanged for the reverse function.

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company
Telephone: 0536 201234
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RS Data Library

Light dependent resistor ORP12

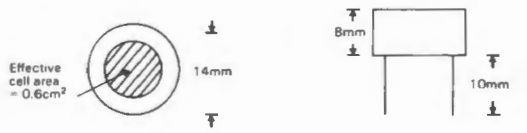
Stock number 305-620

A Cadmium Sulphide photo-conductive cell with a spectral response similar to that of the human eye, making it ideal for visible light sensing circuits. The cell resistance falls with increasing light intensity and follows a logarithmic law. Applications include smoke detection, automatic lighting control, batch counting and burglar alarm systems, etc.

Features

- Wide spectral response
- Sensitive to wide range of light intensities

Dimensions



Absolute maximum ratings

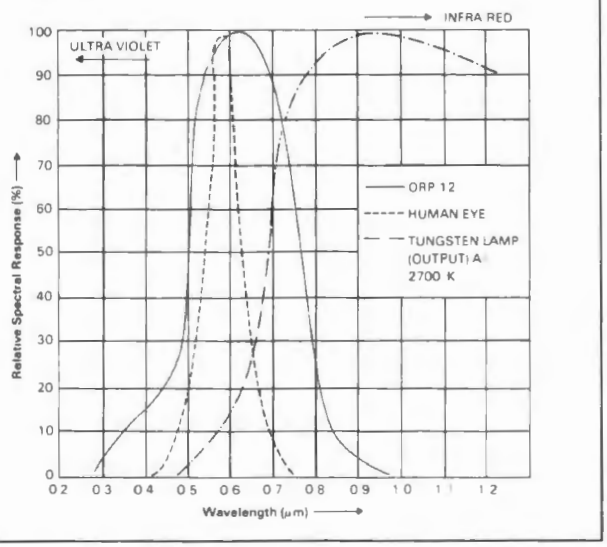
Cell Voltage, d.c. or a.c. peak ——— 110V
Cell dissipation ——— 220mW
Ambient temperature range ——— −10 to +60°C
*Derate by 10mW/°C above 40°C

Electrical characteristics

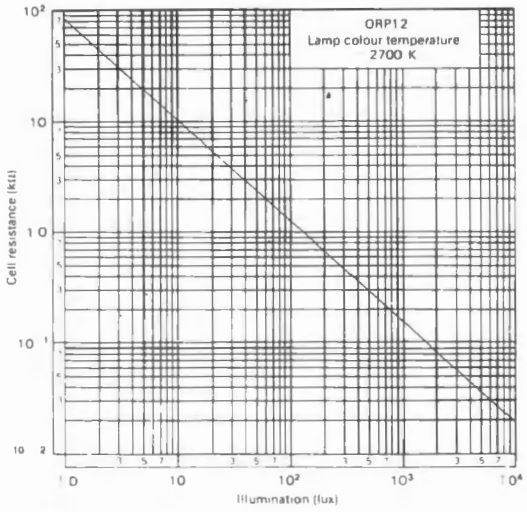
T_A = 25°C. 2700°K tungsten light source

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Cell resistance	R_{CELL}	1000 lux	75	150	300	Ω
		50 lux	–	2.4	–	kΩ
		dark	–	≥10	–	MΩ
Recovery rate	–	–	–	>200	–	kΩ/s

Spectral response



Cell resistance v illumination



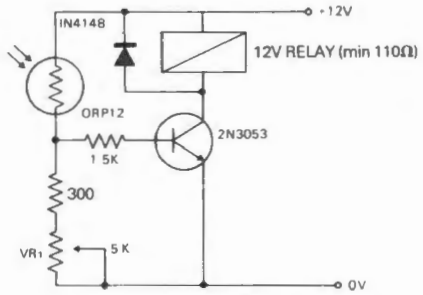
Guide to source illuminations

Light source	Illumination (Lux)
Moonlight	0.1
60W bulb at 1m	50
1W M.E.S. bulb at 0.1m	100
Fluorescent lighting	500
Bright sunlight	30,000

Circuit symbol

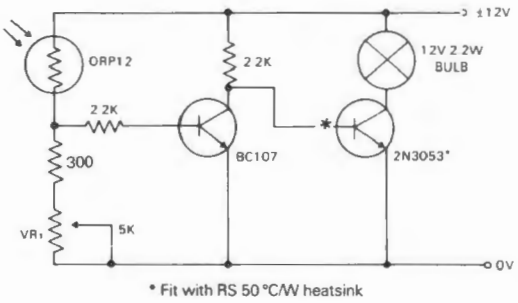
Typical application circuits

Figure 1 **Sensitive light operated relay**



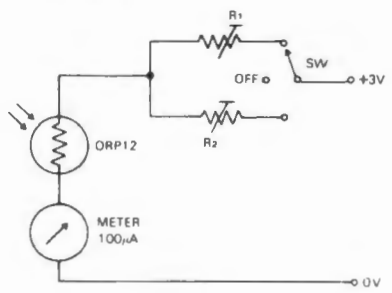
Relay energised when light level increases above the level set by VR_1

Figure 2 **Automatic light circuit**



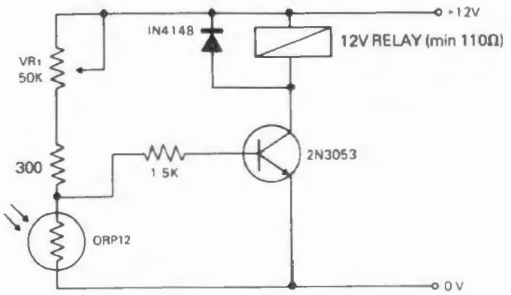
Adjust turn-on point with VR_1

Figure 3 **Logarithmic Law photographic light meter**



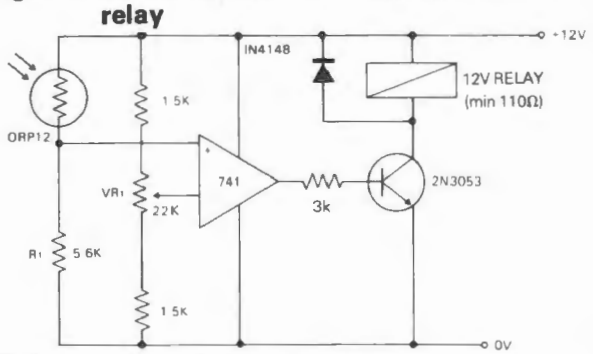
Typical value $R_1 = 100k\Omega$
$R_2 = 200k\Omega$ preset to give two overlapping ranges. (Calibration should be made against an accurate meter).

Figure 4 **Light interruption detector**



As Figure 1 relay energised when light level drops below the level set by VR_1

Figure 5 **Extremely sensitive light operated relay**



(Relay energised when light exceeds preset level). Incorporates a balancing bridge and op-amp. R_1 and ORP12 may be interchanged for the reverse function.

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RS data

Light activated switches

Stock numbers 305-327
305-434

Highly versatile integrated circuit devices incorporating a silicon planar photodiode with TTL output (5 V type) and MOS output (15 V type), also TTL compatible. Both devices are sensitive to a wide range of light sources, e.g. led's, tungsten lamps, sunlight and are packaged in a four lead TO-18 metal can with window.

Applications

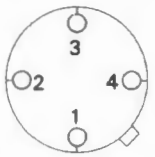
Logic driving	Automatic door opening
Batch counter	Daylight/night switch for street laterns
Burglar alarm	Light coupled isolator

Absolute maximum ratings

	5 V type	15 V type
Maximum power dissipation @ 25 °C	115 mW	120 mW
Working temperature range (ambient)	0 °C to +70 °C	−55 °C to +85 °C

Pin connections

(view from pin side)



Pin	5 V type 305-434	15 V type 305-327
1	Supply +ve	Sensitivity control
2	Sensitivity control	Output
3	Supply −ve	Supply +ve
4	Output	Supply −ve

Outputs HIGH when illuminated

Note:| Can connected to Pin 3

Electrical characteristics

Parameter	Test conditions		5 V type 305-434 Min	Typ	Max	15 V type 305-327 Min	Typ	Max	Units
V_{CC} Supply voltage	Working range		4.75	5.0	5.25	15		20	V
	TTL Compatible		4.75	5.0	5.25	16	17	18	V
I_{CC} Supply current	Zero output current			16	22		1.1	2	mA
	15 V	5 V							
V_{OH} High level output voltage	I_o = 1 mA, V_{CC} = 17 V	I_o = 0.12 mA, V_{CC} = 4.75 V	2.4				16.75		V
V_{OL} Low level output voltage	I_o = 0.1 mA, V_{CC} = 17 V	I_o = 10 mA, V_{CC} = 4.75 V			0.4		8.3		V
I_{OH} High level output current	V_o = 12 V, V_{CC} = 17 V	V_o = 2.4 V, V_{CC} = 4.75 V		0.12		16	29		mA
I_{OL} Low level output current	V_o = 12 V, V_{CC} = 17 V	V_o = 0.4 V, V_{CC} = 4.75 V	−10			−2.5	−4.4		mA

Sensitivity *	2870 °K tungsten source	10^4		10	10^4		10	$\mu W/cm^2$
Sensitivity adjustment	External R	2		10^2	10^2		10^3	kΩ
(see circuit applications)	External C	15 x 10^2		15 x 10^4	50		10^5	pF
Peak spectral response			850			750		nm
Hysteresis			15			1		%

Switching characteristics

Propagation delay time #			0.5		0.005		50	ms
Switching frequency				50	0.01		100	kHz

Notes: * Light Sources: (Approx. irradiation at a distance of 10 cm)
Propagation delay time will vary with external R and C used –longer delays for higher RC product.

Source	Irradiation (Sensitivity)
1.2 watt MES 586-201	1200 $\mu W/cm^2$
LED 586-447	400 $\mu W/cm^2$

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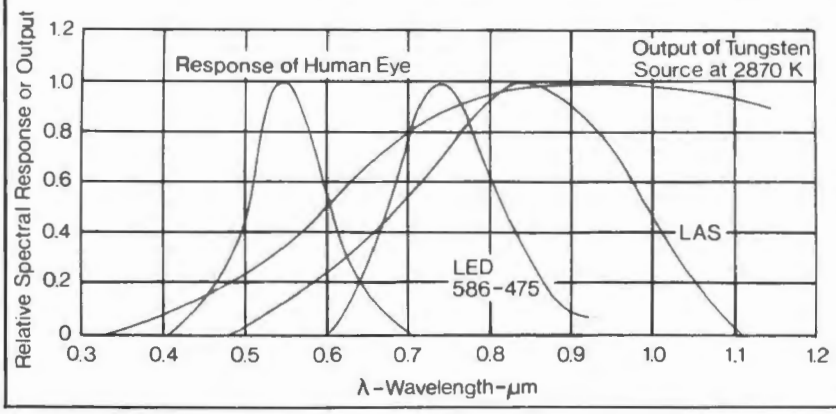
Relative spectral response



Note

Light level at which devices switch is set by time constant of external RC (see table overleaf). Large values of RC give high sensitivity. Outputs go high with increase in incident light at threshold point.

Applications

Figure 1 **Direct TTL driver circuits**

Recommended R & C values shown. For full range see table overleaf.

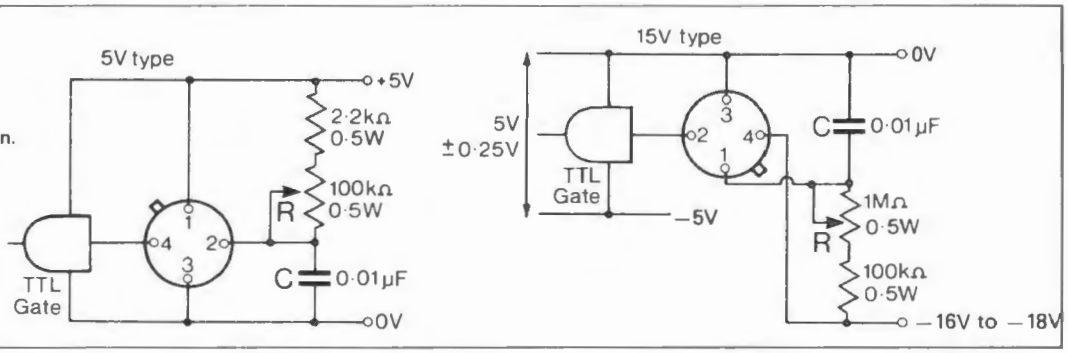


Figure 2 **Light operated relay**

Note use internal diode as shown, otherwise connect a IN4148 externally.

NOTE 15V type will also operate transistor relay 349-254

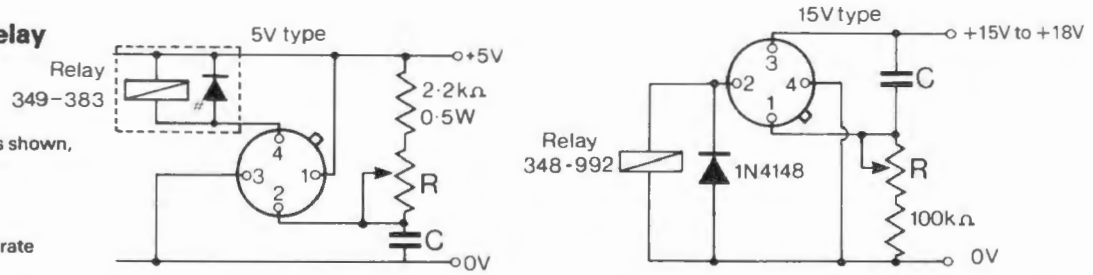
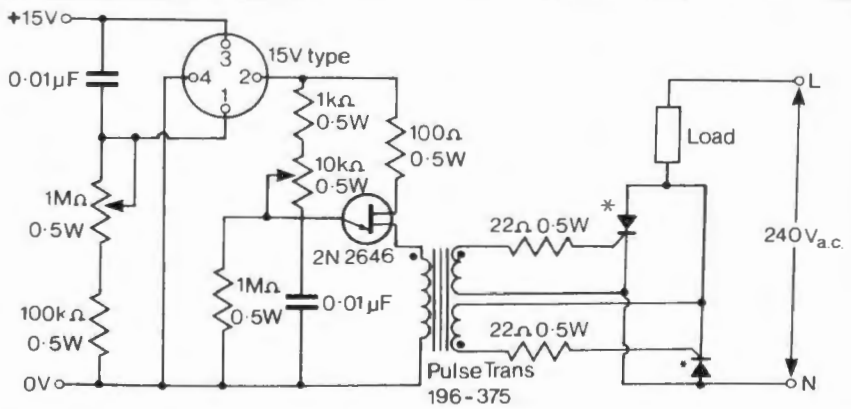


Figure 3 **Light operated solid state switch**

*using BTX-18-400 with heat sink 401-548; max load current 500 mA @ Tamb = 50°C



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RS data

i.c. timers 555 and 556

A range of i.c. Timers suitable for monostable or astable operation. In the monostable mode these timers are capable of producing accurate delays over a very wide timing range. In the astable mode a wide frequency coverage is coupled with variable duty cycle capability. These versatile devices provide effective solutions for many timing and pulse circuit applications. The 556 timer is a dual version of the 555 single timer. The C-MOS versions offer improved characteristics for particular applications. For further information on 555 timers and their applications, please refer to the Technical Library section of the current RS catalogue for suitable reference books.

Absolute maximum ratings – bipolar

Supply voltage	+18 V
Output current	200 mA
Power dissipation	600 mW
Operating temperature	0 to +70°C
Storage temperature	−65 to +150°C
Lead temperature (60 sec)	+300°C

Features

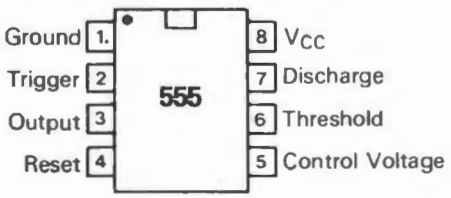
- Bipolar and C-MOS versions
- Low external component count
- Wide operating voltage range
- Low power and supply current

Absolute maximum ratings – C-MOS

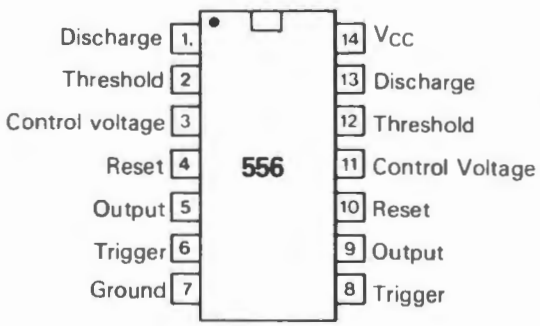
Supply voltage	+18 V
Output current	100 mA
Power dissipation, 555	200 mW
556	300 mW
Operating temperature	0 to +70°C
Storage temperature	−65 to +150°C
Lead temperature (60 sec)	+300°C

Note:
Due to the SCR structure inherent in the C-MOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ +0.3 V or less than V^- −0.3 V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the C-MOS i.c. must be turned on first.

Bipolar pin out diagrams

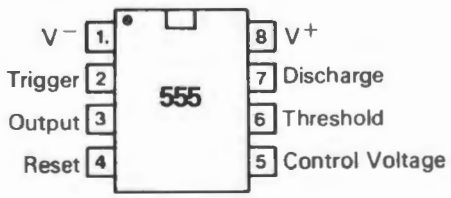


TOP VIEW

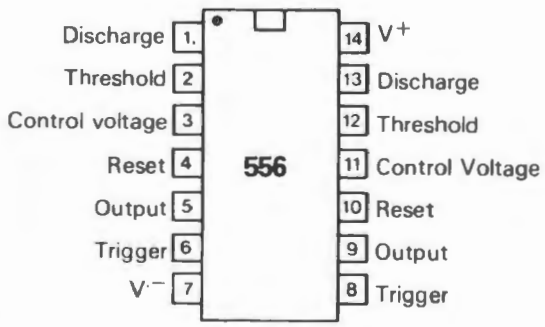


TOP VIEW

C-MOS pin out diagrams



TOP VIEW

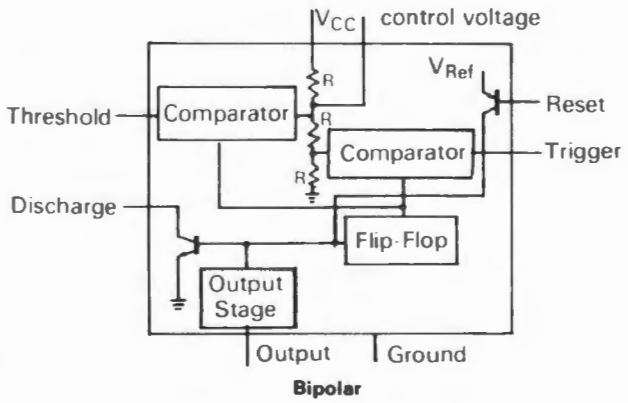


TOP VIEW

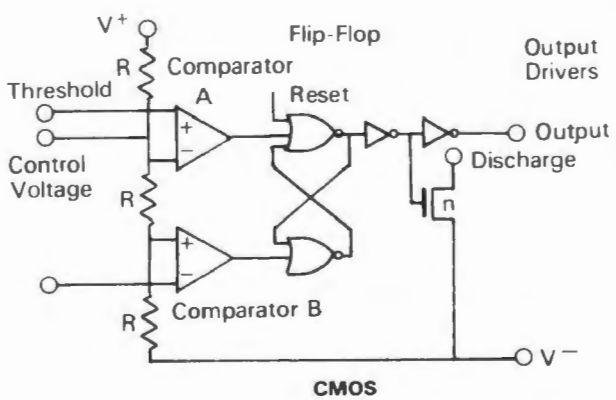
Electrical characteristics bipolar $T_A = 25°C$, $V_{CC} = 5\ V$ to $15\ V$ unless specified

Parameter	Test Conditions	556			555			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		16	4.5		16	V
Supply Current	$V_{CC} = 5\ V\ R_L = \infty$		6	12		3	6	mA
	$V_{CC} = 15\ V\ R_L = \infty$		20	30		10	15	mA
Timing Error (astable)	$R_A, R_B = 1\ k\Omega$ to $100\ k\Omega$ $C = 0.1\mu F$							
Initial accuracy	$V_{CC} = 15\ V$		2.25			2.25		%
Drift with temperature			150			150		ppm/°C
Drift with supply voltage			0.3					%/Volt
Threshold Voltage			2/3 V_{CC}			2/3 V_{CC}		V
Threshold Current (Ith)			30	100		100	250	nA
Trigger Voltage			$V_{CC}/3$			$V_{CC}/3$		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0		0.7	1.0	V
Reset Current			0.1			0.1		mA
Control Voltage Level	$V_{CC} = 15\ V$	9.0	10	11		10	11	V
	$V_{CC} = 5\ V$	2.6	3.33	4		3.33	4	V
Output Voltage (low)	$V_{CC} = 15\ V\ I_{SINK} = 10\ mA$		0.1	.25		0.1	.25	
	$I_{SINK} = 50\ mA$		0.4	.75		0.4	.75	V
	$I_{SINK} = 100\ mA$		2.0	3.2		2.0	.25	V
	$V_{CC} = 5\ V\ I_{SINK} = 5\ mA$		.15	.25		.25	.35	V
Output Voltage (high)	$V_{CC} = 15\ V\ I_{SOURCE} = 100\ mA$	12.75	13.3		12.75	13.3		V
	$I_{SOURCE} = 200\ mA$		12.5			12.5		
	$V_{CC} = 5\ V\ I_{SOURCE} = 100\ mA$	2.75	3.3		2.75	3.3		V
Rise Time of Output 10% to 90%			100			100		ns
Fall Time of Output 10% to 90%			100			100		ns
Discharge Leakage Current			20	100				nA
Timing error (monostable)	$R_A = 2\ k\Omega$ to $100\ k\Omega$ $C = 0.1\mu F$							
Initial accuracy			0.75	3.0		1.0	3.0	%
Drift with temperature			50			50		ppm/°C
Drift with supply voltage			0.1	0.5		0.1	0.5	%/Volt

Figure 1 **Schematic diagrams**



Bipolar



CMOS

Electrical characteristics – C-MOS $T_A = 25°C$, V^+ to V^- = 2 V to 15 V unless specified

Parameter	Test Conditions	Min	Typ	Max	Units
Supply Voltage	$-20°C < T_A < +70°C$	2		18	V
Supply Current	V^+ to V^- = 2 V (555)		0.06	0.2	mA
	V^+ to V^- = 18 V (555)		0.12	0.3	mA
	V^+ to V^- = 2 V (556)		0.12	0.4	mA
	V^+ to V^- = 18 V (556)		0.24	0.6	mA
Timing Error (astable)	R_A, R_B = 1 k to 100 k C = 0.1 µF				
Initial accuracy			2.0		%
Drift with temperature			50		ppm/°C
Drift with supply voltage	V^+ to V^- = 5 V		1.0		%/Volt
Threshold Voltage			2/3 V+		V
Threshold Current (I_{th})	V^+ to V^- = 5 V		0.01		nA
Trigger Voltage			V+/3		V
Trigger Current	V^+ to V^- = 5 V		10		pA
Reset Voltage		0.4	0.7	1.0	V
Reset Current	V^+ to V^- = 5 V		20		pA
Control Voltage Level	V^+ to V^- = 15 V		10		V
	V^+ to V^- = 5 V		3.33		V
Output Voltage (low)	I_{SINK} = 3.2 mA				
	V^+ to V^- = 18 V		0.1	0.4	V
	V^+ to V^- = 5 V		0.15	0.4	V
					V
Output Voltage (high)	V^+ to V^- = 18 V, I_{SOURCE} = 1.0 mA	17.25	17.8		V
	V^+ to V^- = 5 V, I_{SOURCE} = 1.0 mA	4.0	4.5		V
Rise Time of Output 10% to 90%	R_L = 10 MΩ C_L = 7 pF		40		ns
Fall Time of Output 10% to 90%	V^+ to V^- = 5 V		40		ns
Discharge Leakage Current					nA
Timing error (monostable)	R_A, R_B = 1 k to 100 k C = 0.1 µF				
Initial accuracy			2.0		%
Drift with temperature			50		ppm/°C
Drift with supply voltage	V^+ to V^- = 5 V		1.0		%/Volt

Figure 2 **Basic modes of operation**

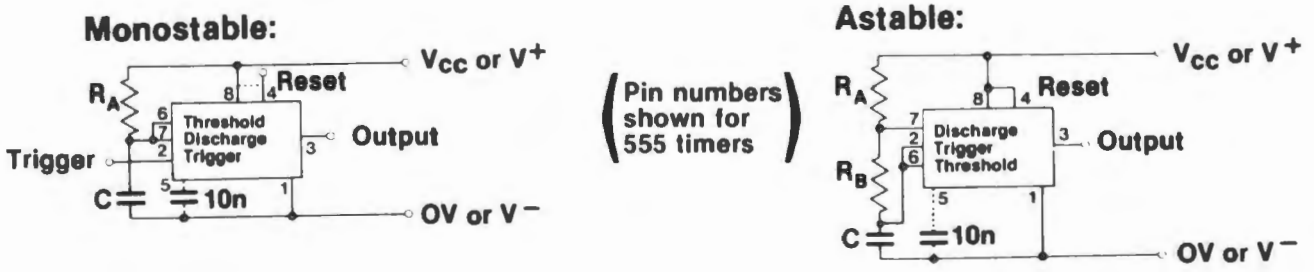
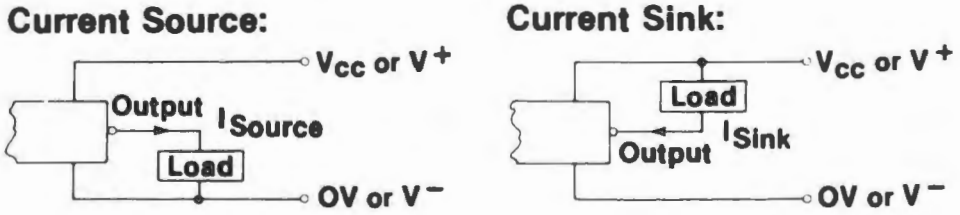


Figure 3 **Load connection options**



Operation

Trigger input

This input is used to initiate a monostable timing period. Triggering occurs on the negative going edge AB of the pulse shown in the diagram below, at a voltage level less than ⅓ of the V_{CC} or V^+ supply rail. The trigger pin must be returned to a level above ⅓ of the OV or V^- supply rail before the end of the set timing period 'T'. Should the trigger pulse interval 't' be greater than the timing period 'T' then the output will remain in the active state (output high) for time 't'. Once triggered the trigger input is disabled and any trigger pulses occurring during the timing period 'T' have no effect on the set time.

The necessity to return the trigger input to a voltage above ⅓ of the OV or V^- rail and because the trigger input impedance is very high and hence susceptible to external noise, a.c. coupling of this pin is desirable. The figure below shows an arrangement for a.c. coupling of the trigger input.

Figure 4a

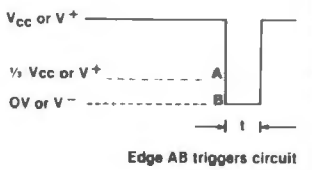
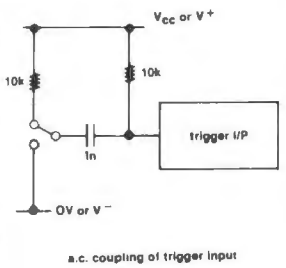


Figure 4b

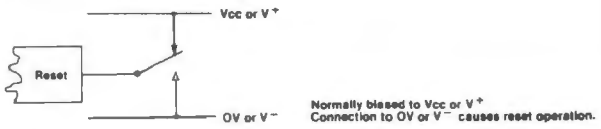


The minimum pulse width required for triggering and the propagation delay versus voltage of trigger pulse are shown in Fig. 6 for both the bipolar and C-Mos timers.

Reset input

The reset function is used to return the timer output to the steady state (output low) when interruption of a monostable timing period is required. When not required the reset should be connected to V_{CC} or V^+. This avoids a false reset occurring.

Figure 5 **Reset input**



Control voltage

As can be seen from the timer schematics on Page 2 the open circuit voltage at the control pin is set at ⅔ V_{CC} or V^+ by the internal resistors R. This resistor network sets the threshold comparator trip level at ⅔ supply and the trigger comparator at ⅓ supply. By imposing an external voltage on this pin the comparator reference levels may be shifted above or below the nominal levels hence affecting the timing in both the monostable and astable modes. In the monostable mode this pin can be swung between 45% to 90% of V_{CC} or V^+. In the astable mode a variation of 33% to 100% of the supply rail is possible. This feature extends the versatility of the timer to voltage controlled oscillators, pulse width modulators etc.

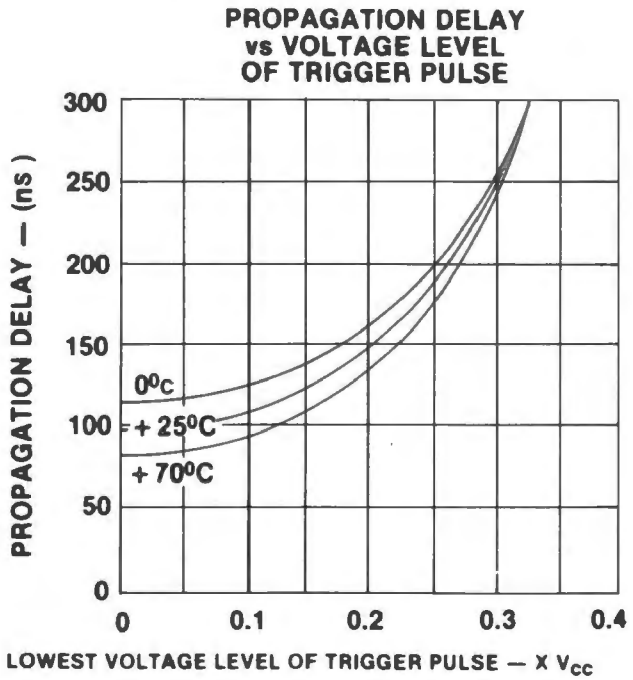
For applications where this facility is not required the control voltage terminal should be decoupled to OV by a 10 nF capacitor.

The C-MOS i.c.'s, in most applications, will not require the control voltage terminal to be decoupled and should be left unconnected.

Output

The output voltage dependence on load current in sink and source modes is shown in Fig. 2.

Figure 1a: **Input characteristics – Bipolar 555, 556**



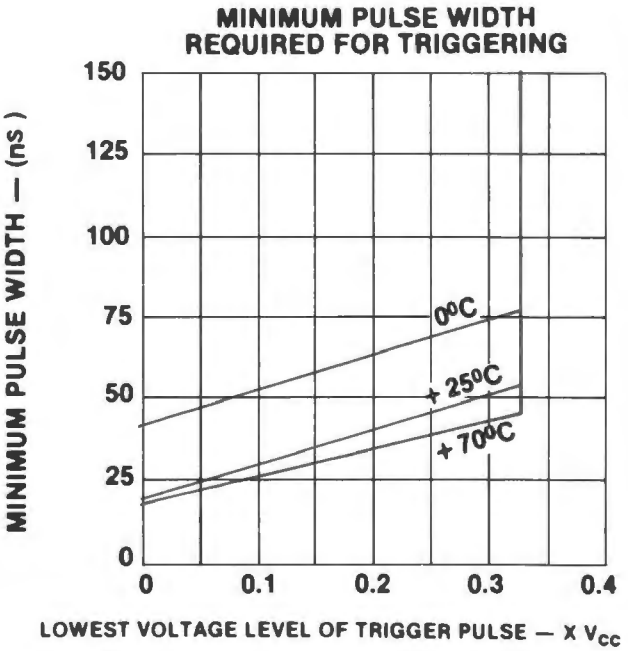
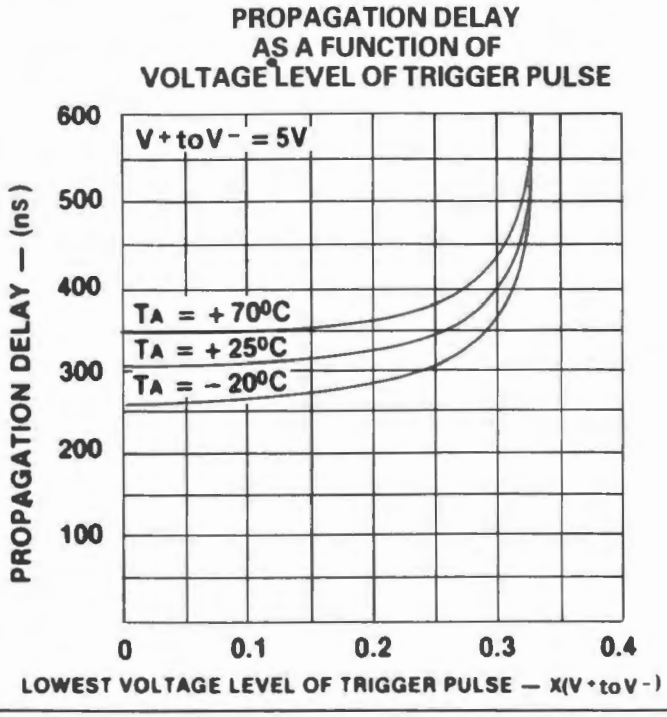


Figure 6b **Input characteristics – C-MOS 555, 556**



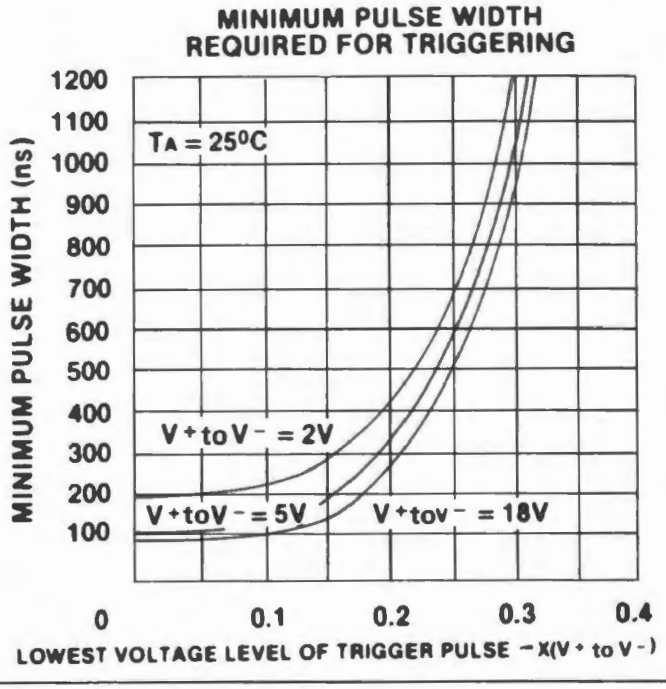
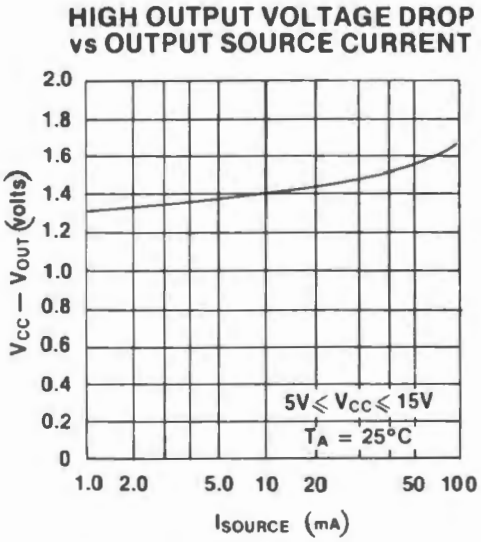


Figure 7a **Output characteristics – Bipolar 555, 556**



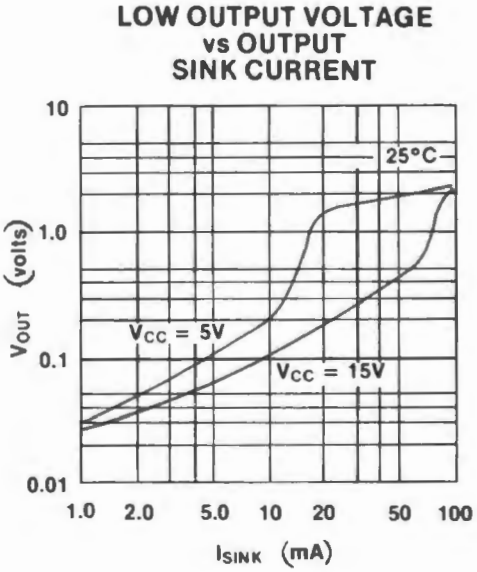
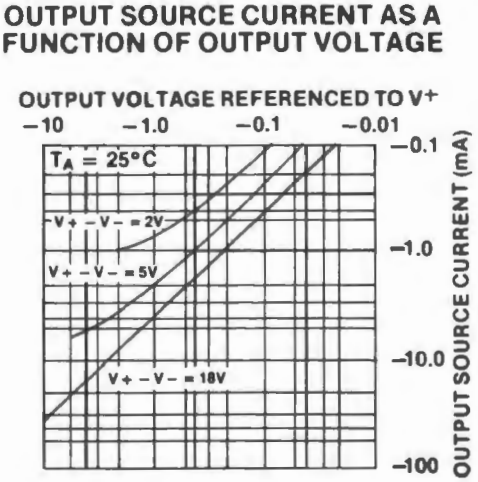
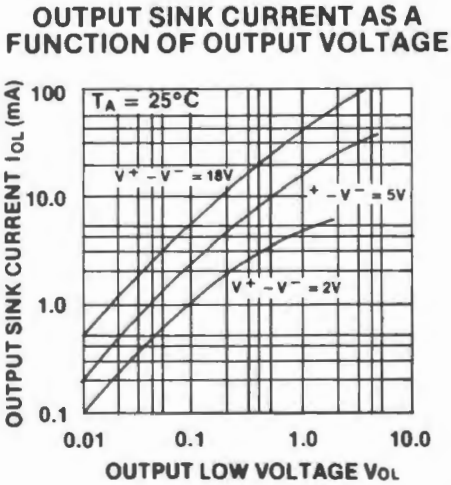


Figure 7b **Output characteristics – C-MOS 555, 556**





Timing formulae

Monostable operation:

$T \approx 1.1\, R_A C$ sec C in F R_A in Ω

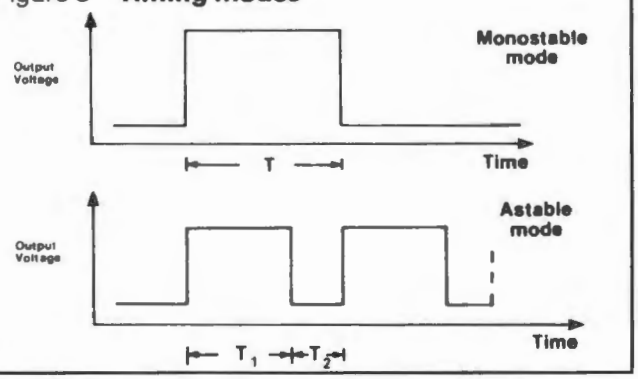
Astable operation:

$T_1 \approx 0.7\,(R_A + R_B)C$ sec

$T_2 \approx 0.7\, R_B C$ sec C in F R_A & R_B in Ω

$$f = \frac{1}{T_1 + T_2} \approx \frac{1.44}{(R_A + 2R_B)\,C} \text{ Hz}$$

Figure 8 **Timing modes**



The minimum recommended values for the timing resistors are $R_A = 5\,k\Omega$ & $R_B = 3\,k\Omega$. These values are consistent with reliable operation at extremes of supply voltage, however, at intermediate levels lower value resistors may prove satisfactory.

The maximum value of these resistors is governed by the typical value of threshold current and varies for each of the timers.

$$R_A \text{ max or } (R_A + R_B) \text{ max} = \frac{0.33 V_s}{I_{th} \times 10^{-9}} \ \Omega$$

where $V_s = V_{CC}$ or V^+ to V^- in volts

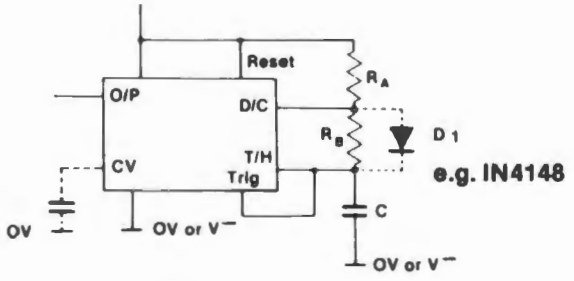
I_{th} = Threshold current in nA for the timer i.c.

The duty cycle in the astable mode is:

$$\frac{T_1}{T_1 + T_2} = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%$$

The minimum duty cycle using the recommended values is approximately 62%. By adding a diode across R_B the charging path for the timing capacitor C changes from $(R_A + R_B)$ to $(R_A + D_1)$ hence $t_1 < 0.7\,(R_A + R_B)$ and duty cycles from 5 to 95% are possible.

Figure 9 **Duty cycle**



Timing capacitor – IMPORTANT

The capacitor employed must have a leakage current less than $0.1 I_{th}$ for satisfactory operation. Suitable types are silvered mica, polycarbonate, polystyrene, polypropylene, but not ceramic disc which are unstable in capacitance for RC network applications, or electrolytics due to high leakage current.

Technical hints

The bipolar timers have a 'totem pole' type output stage and during switching, large current spikes can appear on the supply line. Effective by-passing is necessary to eliminate noise retriggering the input and a 47 μF tantalum capacitor mounted close to the device supply pins is suggested.

To prevent the possibility of double triggering when driving TTL loads a 1 nF capacitor connected between the timer output and ground should be found suitable.

Applications

Figure 10 **Time delay**

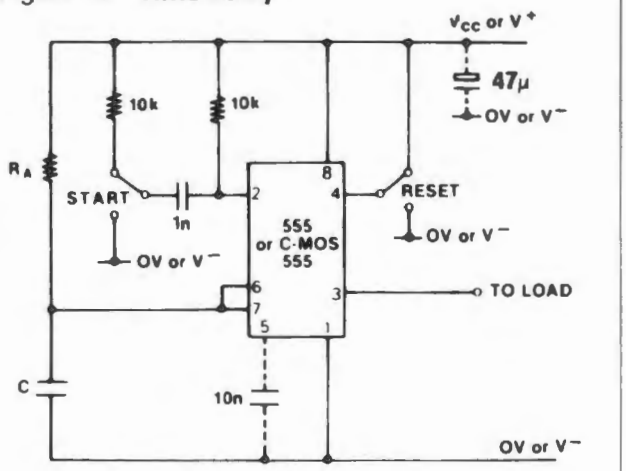


Figure 11 **Load options**

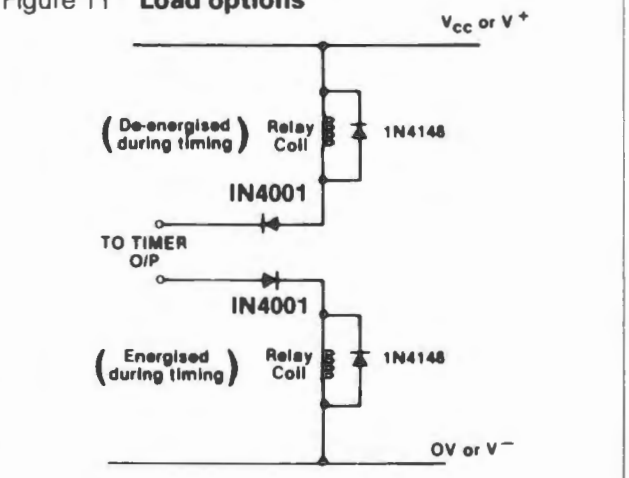
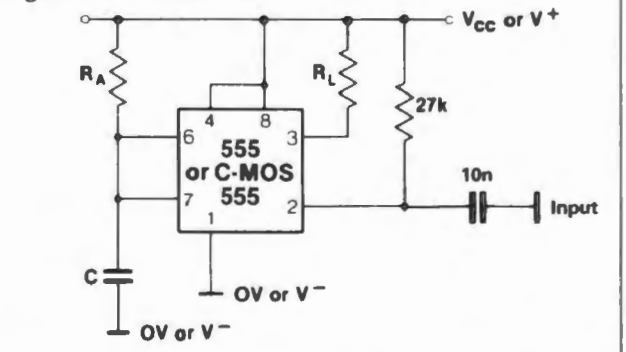
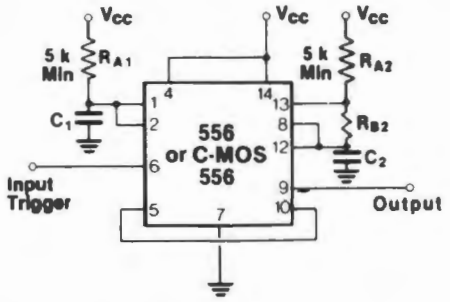


Figure 12 **Touch control**



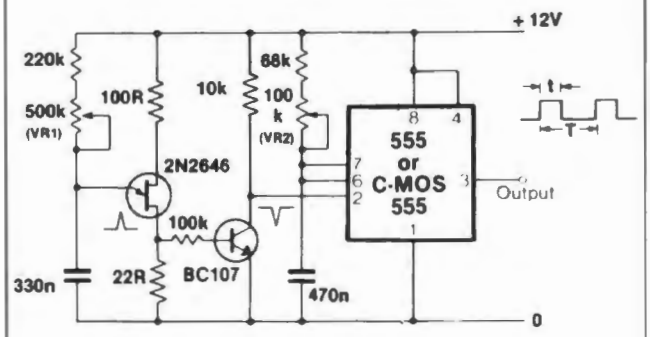
The value of the 27 kΩ resistor is suitable for industrial or public environments. With lower ambient noise, a higher value of resistor may be necessary.

Figure 13 **Tone burst generator**
The 556 Dual Timer makes an excellent Tone Burst Generator. The first half is connected as a one shot and the second half as an oscillator.



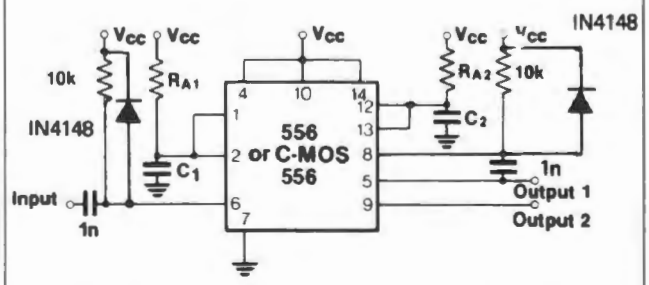
The pulse established by the one shot turns on the oscillator allowing a burst of pulses to be generated.

Figure 14 **Simple pulse generator**



Pulse width (t) adjusted by VR2
Pulse repetition frequency ($1/_T$) adjusted by VR1
Circuit as shown gives
$t = 20 \rightarrow 80\,ms$ $T = 100 \rightarrow 250\,ms$

Figure 15 **Sequential timing**
One feature of the Dual Timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 1 nF coupling capacitor sequential timing may be obtained. Delay T_1 is determined by the first half and T_2 by the second half delay.



The first half of the timer is started by momentarily connecting pin 6 to ground. When it has timed out (determined by $1.1\ R_{A1}\ C_1$) the second half begins.
(Its time duration is determined by $1.1\ R_{A2}\ C_2$).

Figure 16 **Missing pulse detector**
Using the circuit shown below, the timing cycle is continuously reset by the pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses.

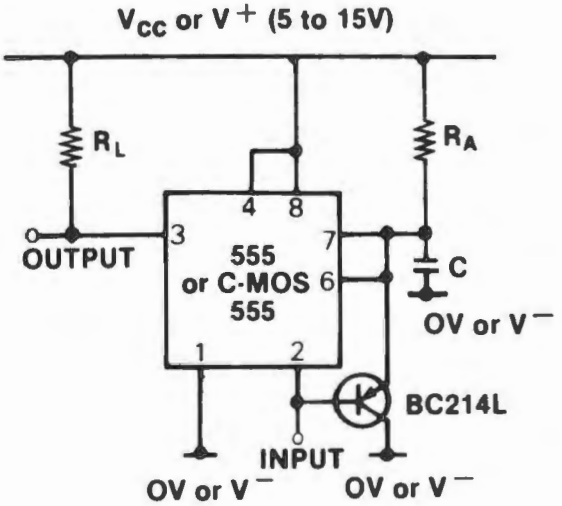
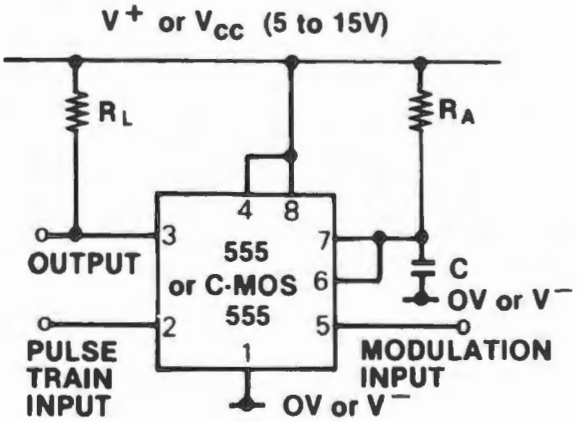


Figure 17 **Pulse width modulation (PWM)**
In this application, the timer is connected in the monostable mode as shown below. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (pin 5). This has the effect of modulating the pulse width as the control voltage varies.



RS data

Figure 18 **Pulse position modulation (PPM)**

This application uses the timer connected for astable (free-running) operation, shown below, with a modulating signal again applied to the control terminal. Now the pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.

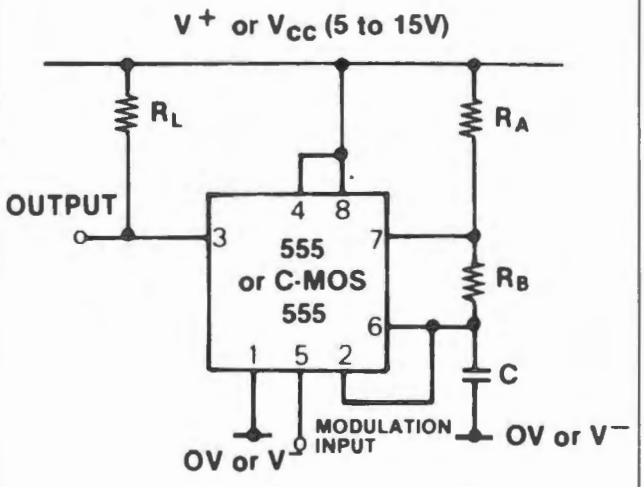


Figure 19a **Tachometer circuit**

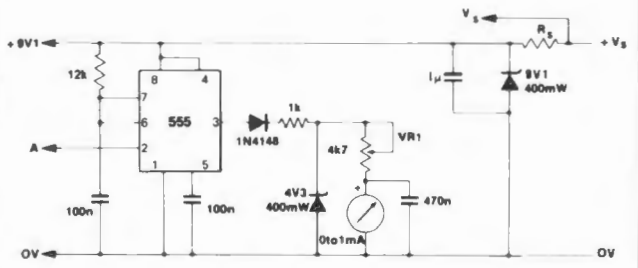
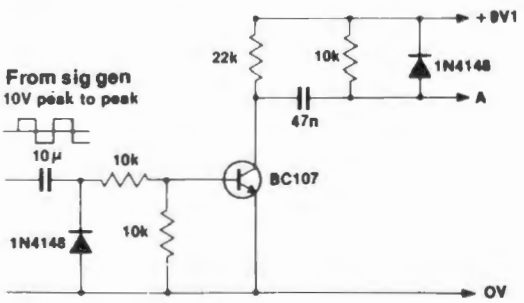


Figure 19b **Calibration interface**



To calibrate: adjust VR1 for known reading against signal generator using circuit shown and values in table.

Minimum input pulses from slotted opto switch or Proximity detector should be > 1 ms.	At slow speeds needle will flicker. For very low speeds use more than one hold on disc and multiply reading in table by number of holes.

Rpm	Tachometer pulse per sec (or Hz on sig. gen.)
600	10
1200	20
2400	40
3600	60
6000	100

Figure 20a **Interface with inductive proximity detector**

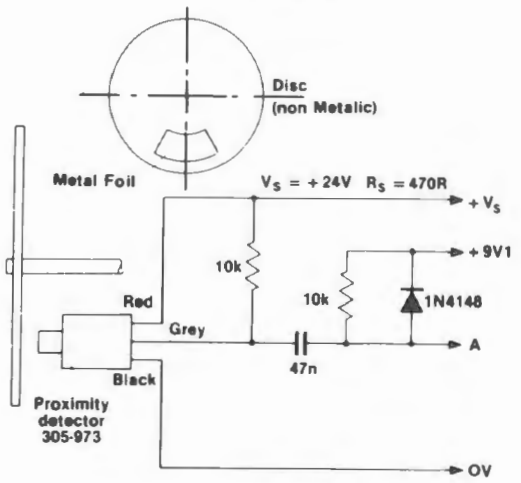
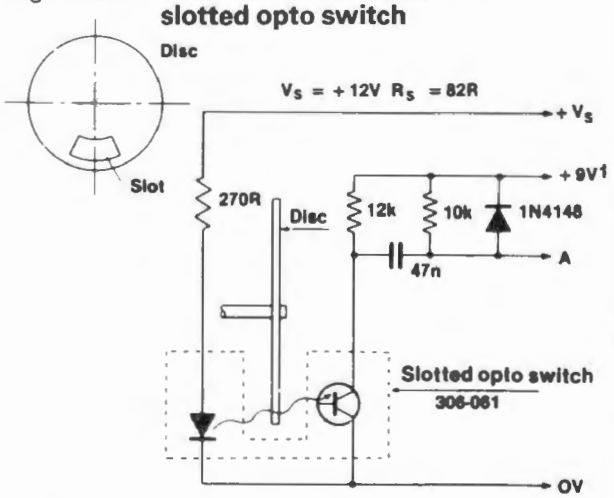


Figure 20b **Interface for use with slotted opto switch**



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RS data

Zero voltage switch

Stock number 305-800

A silicon monolithic zero voltage switch for firing triacs in burst firing and proportional control applications, (resulting in negligible R.F.I.). Housed in plastic 16 lead D-I-L package. Equivalent to L121.

Brief description of zero voltage firing:-

With phase control the power in a load is controlled by delaying the turn on of the current.
But this results in radio frequency interference (R.F.I.).

With zero point firing the current is turned on at the zero voltage point thus reducing the amount of R.F.I. The power in a load is controlled by the number of half cycles of current allowed to the load in a given period. This technique can only be applied to certain types of load, particularly heater elements.

Proportional control allows just sufficient bursts of power to reach the load to make up the system losses and is achieved by using the internally generated ramp. This results in very accurate control.

Absolute maximum ratings		
I_9	AC supply current	60mA
V_{8-12}	Positive AC clamp voltage	15V
V_{10-12}	Negative AC clamp voltage	−15V
V_{1-2}	Differential input voltage	±7V
V_{3-5}	Differential input voltage	±7V
P_{tot}	At Tamb 70°C	45mW
T_S	Storage temp. range	−55° to + 150°C
T_{amb}	Operating temp. range	0° to + 70°C

Generating a ramp

The width (tb) of the ramp appearing at pin 1 is determined by the value of capacitor C_1 and resistor R_{16}. (Where C_1 is capacitor going to pin 1 and R_{16} is resistor going to pin 16).

$$tb = \frac{R_{16} \times C_1}{1.2} \text{secs}$$

Where R_{16} is in ohms
C_1 is in farads

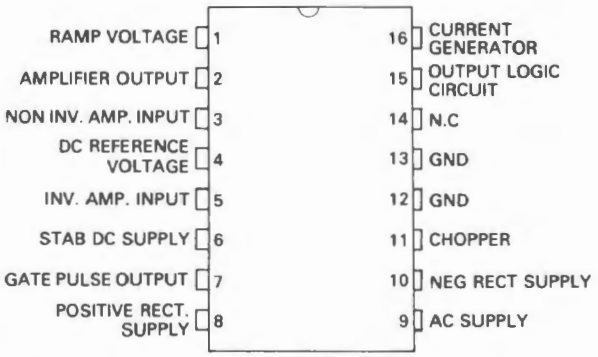
With R_{16} = 100KΩ following table gives nearest preferred value of C_1 for various ramp widths.

tb Ramp width secs	C_1 Capacitor µF
100	1000µF
40	470µF
10	100µF
4	47µF
1	10µF

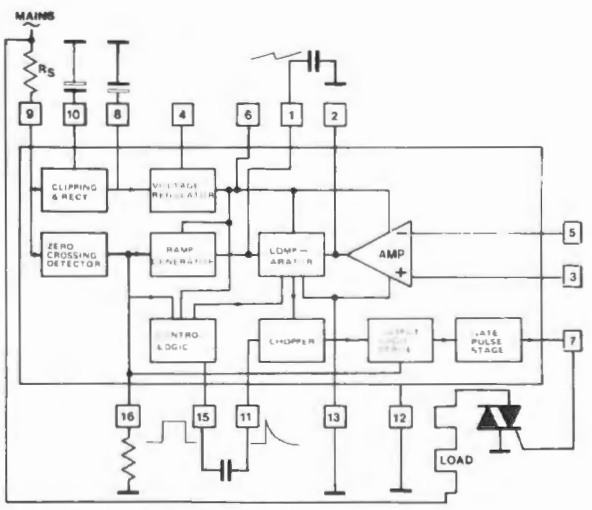
Features

- A.C. supply 50/60Hz
- Internal ramp generator
- Output short circuit protection

Pin connection (top view)



Block diagram



Electrical characteristics

(At Tamb = 25°C and referred to test circuit unless otherwise stated)

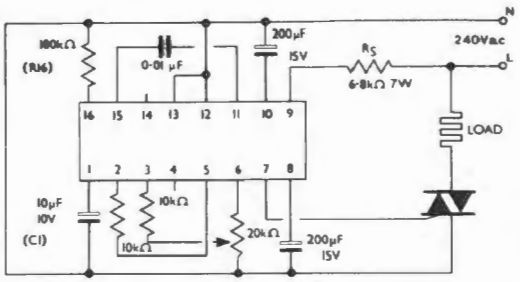
Parameter		Test conditions	Min.	Typ.	Max.	Units
V_{8-12}	Pos. clamp voltage		–	12	15	V
V_{10-12}	Neg. clamp voltage		–	−12	−15	V
V_{9-12}	Sync. input threshold	$V_S = 220V_{ac}$	–	±12	–	V
V_{1-12}	Ramp discharge level	$R_S = 6.8K\Omega$	–	–	1.2	V
V_{1-12}	Ramp maximum level		5	–	–	V
V_{1-2}	Comparator diff. trigger level.		–	70	100	mV
V_{1-13}, V_{2-13}	Comparator voltage range	$V_{6-13} = 8V$	0	–	7	V
G_V	Amp. large signal voltage gain	$V_{2\,p-p} = 6V$ $V_{6-13} = 8V$ $R_{2-13} = 10K\Omega$	60	70	–	dB
ΔV_{2-13}	Amp output voltage swing	$V_{6-13} = 8V$ $R_{2-13} = 20K\Omega$	5.5	–	–	V
V_{3-13}, V_{5-13}	Input offset Voltage	$V_{6-13} = 8V$ R_{3-13} $R_{5-13} = 50K\Omega$	–	3	6	mV
I_b	Input bias current		–	0.1	1	μA
V_{3-5}	Amp. diff. input voltage	$V_{6-13} = 8V$	–	–	±7	V
V_{3-13}, V_{5-13}	Amp. input Voltage range		0	–	8	V
C_{MRR}	Common mode rejection ratio	$V_{6-13} = 8V$ R_{3-13} & $R_{5-13} = 1K\Omega$	–	60	–	dB
V_{6-13}	Reg. output voltage	$V_S = 220V_{ac}$ $R_S = 6.8K\Omega$	7.5	–	8.7	V
I_6	Reg. output current	$V_S = 220V_{ac}$ $R_S = 6.8K\Omega$ $C_8 = 250\mu F$	–	–	3	mA
$\frac{\Delta V6}{V6}$	Load regulation	$V_S = 220V_{ac}$ $R_S = 6.8K\Omega$ $I_6 = 0$ to 2mA $C_8 = 250\mu F$	–	0.5	1	%
$\frac{\Delta V6}{\Delta V8}$	Line regulation	$V_8 = 12$ to 14V $I_6 = 0$	–	46	–	dB
V_4	Reference voltage	$V_S = 220V_{ac}$ $R_S = 6.8K\Omega$	–	1.5	–	V
V_{7-12}	Fringe pulse amplitude	$V_S = 220V_{ac}$ $R_S = 6.8K$ $R_{7-12} = 1K\Omega$ $C_8 = 250\mu F$ POS	–	5.5	–	V
		NEG	–	−9.5	–	V
I_7	Max. output current	$V_S = 220V_{ac}$ $R_S = 6.8K\Omega$ $R_{7-12} = 10K$ $C_8 = 250\mu F$	80	–	–	mA
tpw	Output pulse width	$V_S = 220V_{ac}$ $R_S = 6.8K\Omega$ $R_{7-12} = 50\Omega$ $C_8 = 250\mu F$	–	200	–	μS
tr	Output pulse rise time	$C_{11-15} = 10\mu F$	–	200	–	μS
R_{16-13}	Typical resistor value to operate ramp	$V_{6-12} = 8V$	–	100	–	KΩ

Setting up a "reference" voltage on pin 1

If C_1 is replaced with a resistor a constant voltage level can be set up on (pin 1 of) the comparator for applications where the ramp is not required. Its level can be set by adjustment of R_{16} and R_1 according to the formulae:-

$$V_1 = \frac{6.8 \times R_1}{R_{16}} \text{ VOLTS}$$

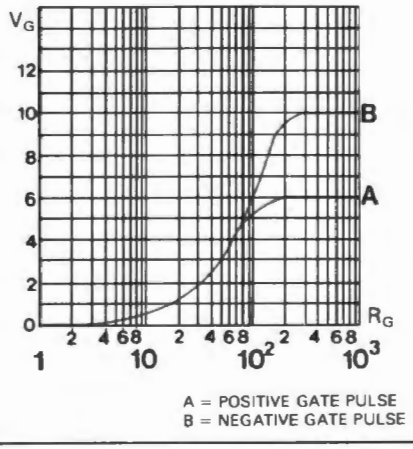
Figure 1 **Test circuit**



Variation of output pulse amplitude

The amplitude of the output pulse will vary according to the gate resistance of the triac. This amplitude can be determined from the graph shown. (Fig. 2)

Figure 2 **Typical gate pulse amplitude vs. gate resistance**



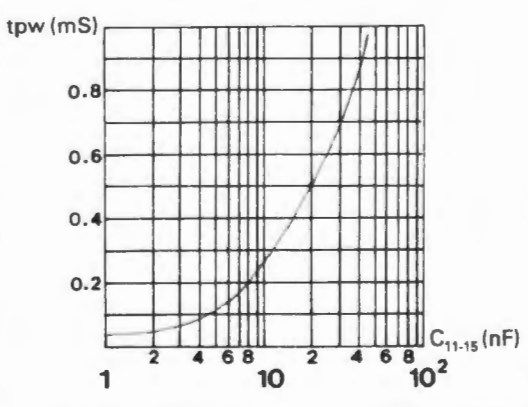
A = POSITIVE GATE PULSE
B = NEGATIVE GATE PULSE

Adjustment of output pulse width

The width of the output pulse can be adjusted by varying the value of capacitor C_{11-15}.
(It is important on inductive loads that the output pulse width is long enough to fire the triac correctly).

The value of C_{11-15} can be selected from the graph shown. (Fig. 3)

Figure 3 **Typical gate pulse width vs. C_{11-15}**



Typical applications

On/off control

With this circuit an AC load can be turned on and off at the zero-voltage points, thus producing negligible radio-frequency interference (R.F.I.). Grounding pin 3 applies power to the load and this can be achieved using a SPST switch. If isolation is required a reed relay or opto-isolator can be used as shown.

For details of triac see table below.

Figure 4

Using reed relay **Using opto-isolator**

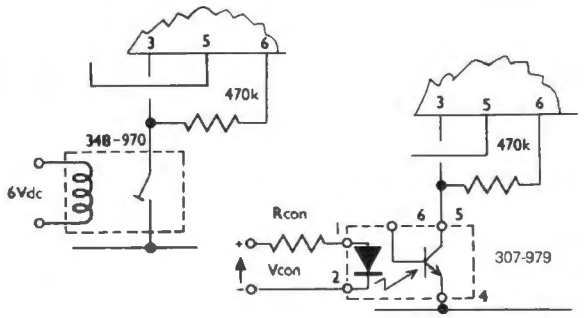
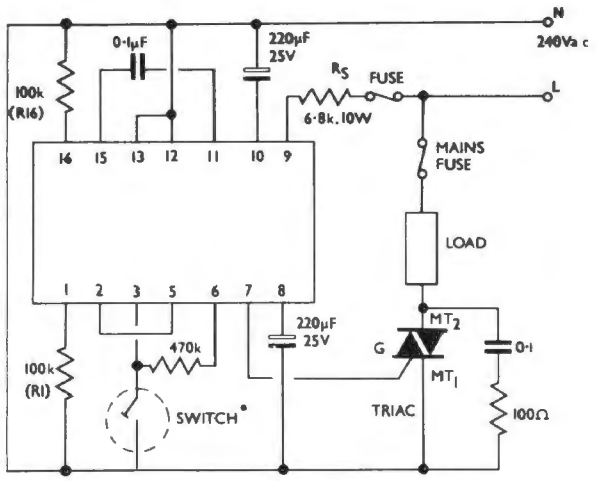


Figure 5 **On/Off control**



V_{CON}	R_{CON}
6V	2.2K
12V	4.7K
24V	10K

Temperature control (on/off type)

This circuit shows a simple on/off temperature control circuit, the load being a heater element and the sensor a thermistor. When temperature is low the heater is turned on and when the temperature is high the heater is turned off. With the components shown temperature control in the region of 20 – 50°C is achievable, by means of the potentiometer control. When pin 2 is at a lower voltage than pin 1 the heater is turned on. The block diagram shows how this is achieved with the internal op-amp and comparator. Other temperature settings can be achieved by adjusting the component values.

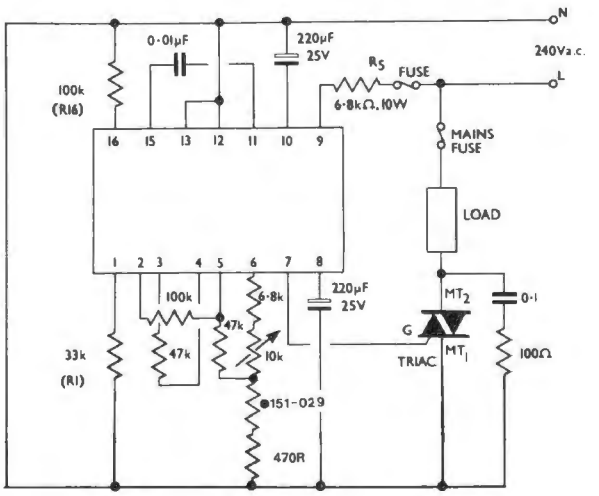
$$V_C \simeq \frac{R2}{R3}(1.5 - V_T) \text{ volts}$$

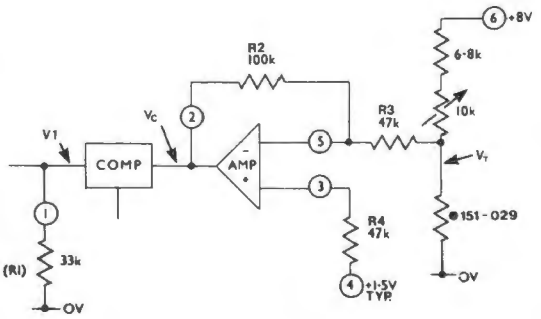
(with R3 = R4)

$$V_I \simeq \frac{6.8 \times R1}{R16} \text{ volts}$$

For details of triac see table below.

Figure 6 **Temperature control (on/off type)**





Triacs	Max heater current	Heat sink
15A 600V (262-494)	13A	2.1°C/W (401-403)

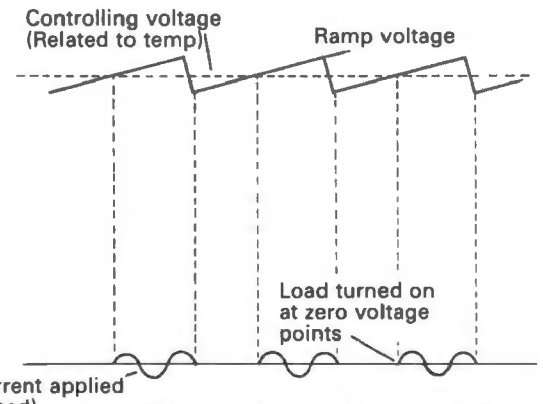
Ratings at Tamb ≤ 35°C.

RS data

Proportional temperature control

This circuit shows a proportional temperature control circuit, the load being a heater and the sensor a thermistor. When the temperature is low the heater is turned on. At the desired temperature just sufficient power is applied to the heater to make up the system losses. This results in extremely accurate temperature control. With the components shown temperature control in the region 20°–60° is achievable by means of the potentiometer control. When pin 2 is at a lower voltage than the bottom of the ramp voltage the heater is on and when the voltage is higher than the top of the ramp the heater is off. Voltages on pin 2 lying between the bottom and top of the ramp produces bursts of power to the load. Other temperature settings can be achieved by adjusting the component values. The ramp period should be much shorter than the thermal constant of the system (i.e. room or oven) but long enough to accommodate many cycles of the mains. For adjustment of the ramp period see page 2.

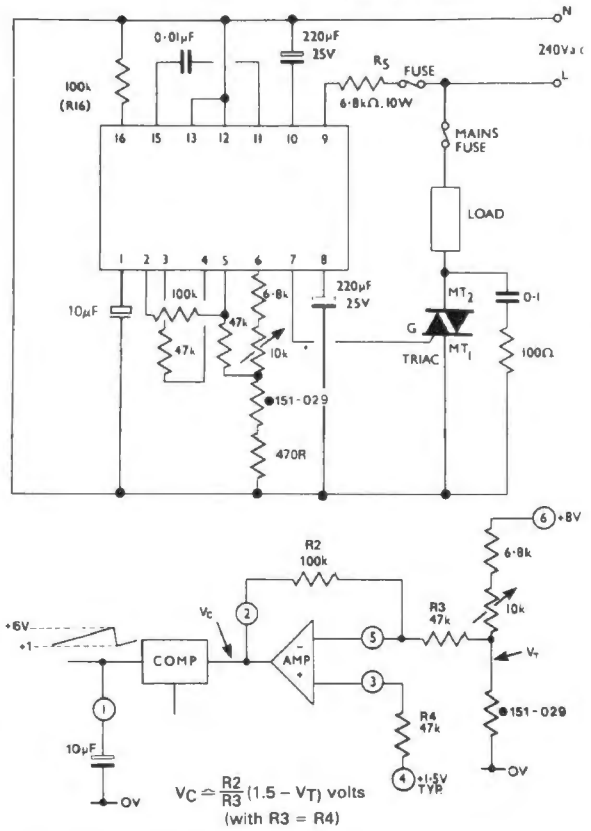
Figure 7 **Proportional control**



Notes on circuits

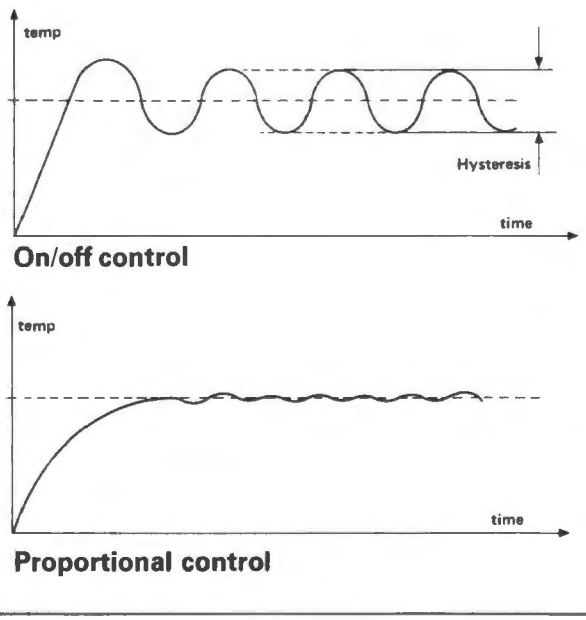
These circuits are intended to serve as an introduction to the zero voltage switch and its possible applications. However RS Components Ltd. cannot undertake further design or modifications to these circuits for specific applications, nor the testing of completed circuits.

Figure 8 **Proportional temperature control**



Effect of proportional control compared to on/off control

Figure 9



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RS data — Opto devices

The following range of discrete opto devices are described, each of which may be used in a variety of sensing applications:

General purpose photodiode, stock no. 305-462
BPX 65, High speed photodiode, stock no. 305-346
Low power and high power discrete infra-red pairs
Large area photodiode, stock no. 303-674

Separate data sheets are available covering the following optical products:

General purpose photodiode

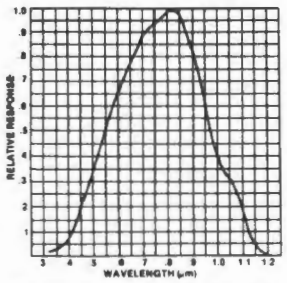
Stock number 305-462

A planar diffused photodiode in a 2-lead TO-18 can with glass window. A very linear output of current versus light level can be obtained over a wide range of inputs. Light falling on the diode induces current in the diode, thus when the device is reversed biased thereby conducting very low leakage currents, it behaves as a current source controlled by the incident illumination.

Absolute maximum ratings at 25°C (unless stated)

Reverse voltage V_R ——— 80V
Forward current I_F ——— 100mA
Operating temp. range ——— 0°C to +70°C
Storage temp. range ——— −55°C to +125°C
Power dissipation Pd ——— 200mW

Normalised spectral response



Case is connected to Pin 2.

Chip placement accuracy ± 0.25mm of can centre.
Nominal photosensitive area 850 Mils (near square).

	Parameter	Value			Units	Test conditions
		Min	Typ	Max		
$V_{(BR)}$	Breakdown voltage	80			V	Dark; rev. current 10μA
I_D	Dark current		1.4	14	nA	Dark; rev. bias 20V
R_e	Responsivity	0.35	0.7	1.4	μA/mW/cm²	Zero bias; 400μW/cm²
C	Capacitance		12		pF	Dark; rev. bias 10V
t_R	Response time		250		ns	10-90% levels
—	Temp. coeff. of responsivity		0.35		% per °C	0°C to +70°C
—	Temp. coeff. of dark current		X2		per 10°C rise	0°C to +70°C

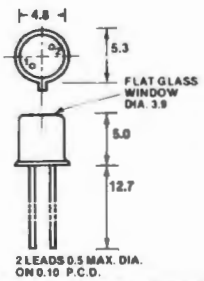


Figure 1 **Photo-current vs Irradiation**

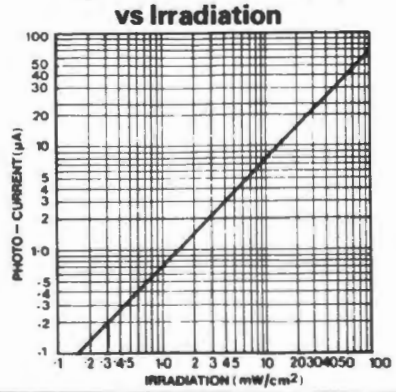


Figure 2 **Open Circuit Voltage vs Irradiation**

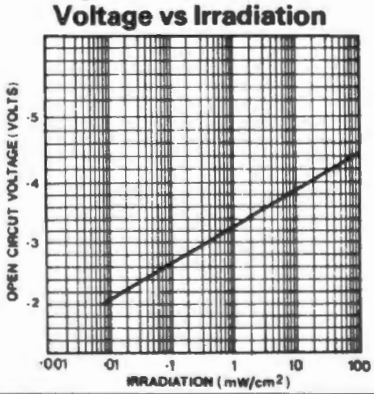
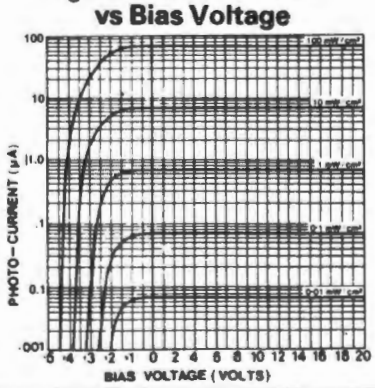


Figure 3 **Photo-current vs Bias Voltage**



BPX 65 High speed photodiode

Stock number 304-346

The BPX 65 is a planar silicon PIN photodiode housed in a modified TO-18 case incorporating a plain glass flat window which has no influence on the beam path of optical lens systems. The cathode is electrically connected to the case. Because the BPX 65 is capable of detecting wide bandwidth signals due to its excellent high frequency response, this coupled with its high sensitivity makes the device ideal for signal detection applications. This photodiode is outstanding for low junction capacitance and short switching times.

Absolute maximum ratings at 25°C (unless stated)

Reverse voltage V_R ——— 50 V
Forward current I_F ——— 10 mA (200 mA pulsed 1us 1 % duty cycle)
Operating temp. range ——— − 25 to + 70°C
Storage temp. range ——— − 55 to + 125°C
Junction temp. T_J ——— 125°C
Power dissipation Pd ——— 250 mW
(derate linearly 2.5 mW/°C above 25°C)

Shape and dimensions

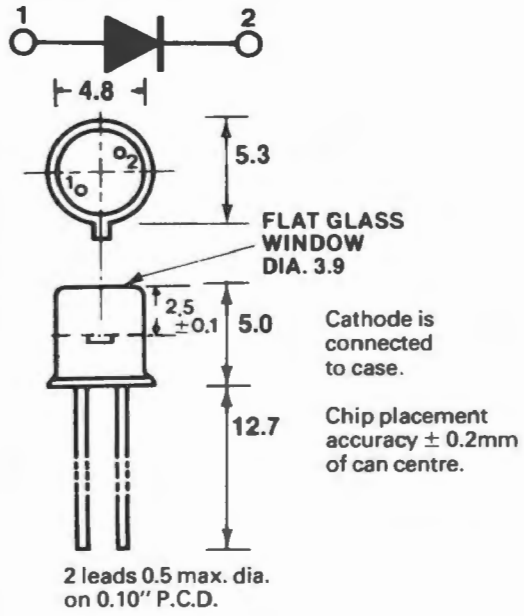


Figure 4: **Normalised spectral response s (λ) and quantum yield η (λ)**

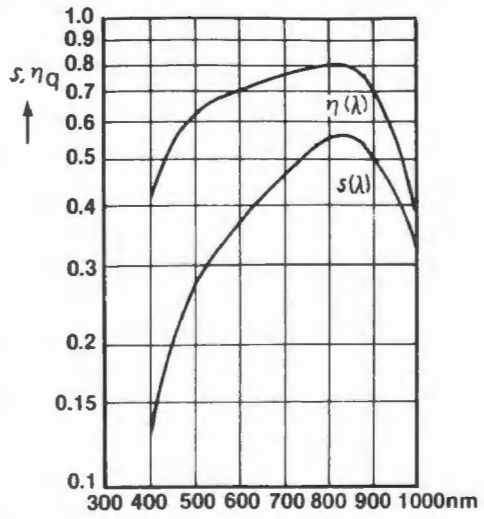
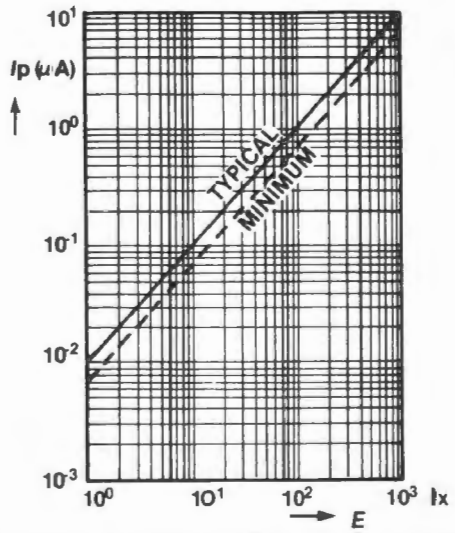


Figure 5: **Variation of output current with illumination**



Note 1) The illuminance indicated refers to unfiltered radiation of a tungsten filament lamp at a colour temperature of 2856°K (standard light A in accordance with DIN 5033 and IEC publ. 306-1).

Electrical characteristics
at 25°C (unless stated)

	Parameter	Test conditions	Value min	Value typ	Value max	units
A	Radiant sensitive area			1		mm²
λ s max η	Wavelength of max. sensitivity Quantum yield (Electrons/photon)	λ = 850 nm		850 0.8		nm Electrons/photon
R_e	Responsivity	λ = 850 nm		0.55		A/W
t_r	Response time (10.90 % Levels)	R_L = 50Ω; V_R = 20 V; λ = 900 nm		0.5	1	ns
C_O	Capacitance V_R = 0V 0V			15		pF
C_1	V_R = 1V			12		pF
C_{20}	V_R = 20V			3.5		pF
fg	Cut-off frequency			500		MHz
1_p	Dark current	V_R = 20V, Dark (E = 0)		1	5	nA
S	Spectral sensitivity	V_R = 20V; see Note 1	7	10		nA/Lx
NEP	Noise equivalent power	V_R = 20V		3.3×10^{-14}		W/√Hz

Figure 6 **Polar sensitivity curve**

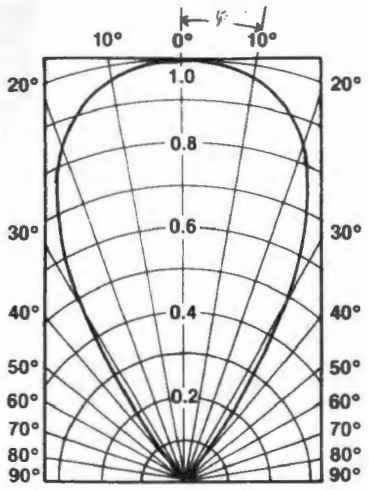


Figure 7 **Variation of diode dark current with reverse voltage**

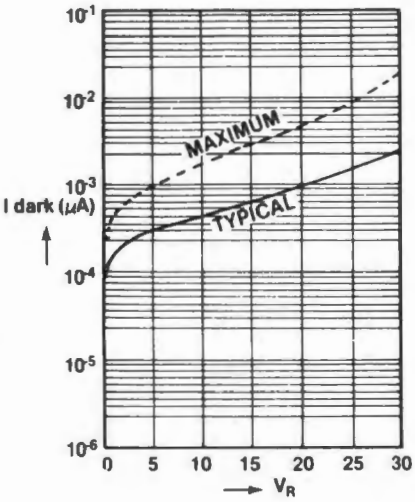
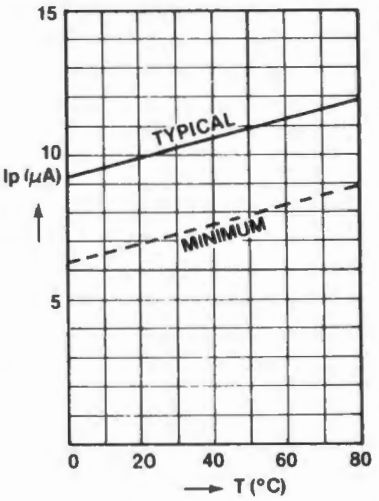


Figure 8 **Variation of output current with temperature**

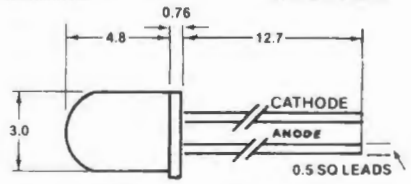


Discrete infra-red pairs

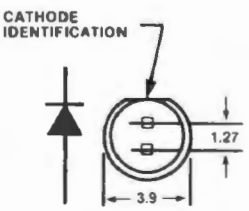
Low power and high power discrete infra-red sources and sensors. The low power versions comprise a solution-grown pn junction Ga As infra-red emitting diode spectrally matched to a silicon passivated NPN planar phototransistor which has exceptionally stable characteristics and high illumination sensitivity. The high power pair consist of a high radiant intensity pn Ga As infra-red emitting diode spectrally matched to a high photo sensitivity silicon PIN photodiode. The high power pair are recommended for use with the RS remote control ic's, see data sheet 3560.

Shape and dimensions

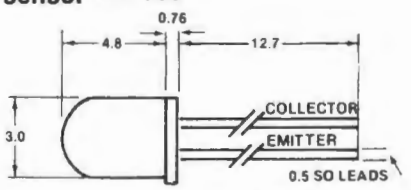
emitter 306-077 **Low Power**



Clear moulded epoxy package

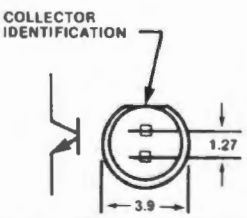


sensor 306-083

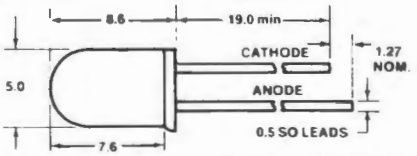


Clear moulded epoxy package

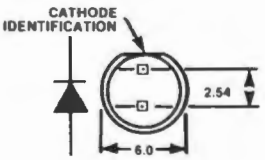
The emitter is distinguished from the sensor by the gold plating near the actual diode chip, visible through the clear housing.



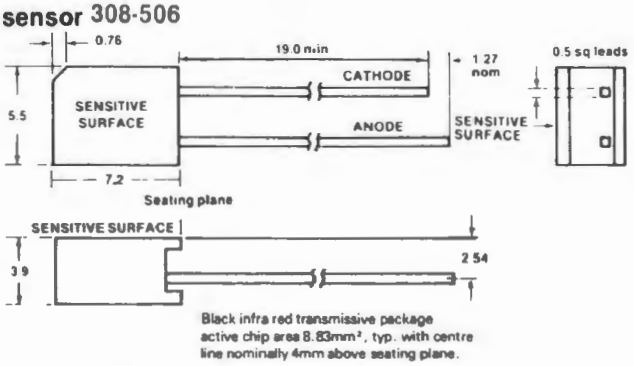
emitter 308-512 **High Power**



Moulded epoxy package



sensor 308-506



Black infra red transmissive package active chip area 8.83mm², typ. with centre line nominally 4mm above seating plane.

Absolute maximum ratings at 25°C (unless stated)

	Low Power		High Power	
	Emitter 306-077	Sensor 306-083	Emitter 308-512	Sensor 308-506
Reverse voltage	2V	–	5V	–
Continuous forward current	40mA	–	150mA	–
Peak forward current p.w. 1μs 300pps p.w. 10μs 1% D.C.	 3A –	 – –	 – 2A	 – –
Collector-emitter voltage	—	30V	–	–
Emitter-collector voltage	–	5V	–	–
Reverse voltage	–	–	–	30V
Power dissipation (cont.)		50mW	–	150mW
Operating temp. range	– 40°C to 85°C	– 40°C to 80°C	– 55°C to 100°C	– 25°C to 100°C
Storage temp. range	– 40°C to 85°C	– 40°C to 100°C	– 55°C to 100°C	– 25°C to 100°C
Lead temperature ($\frac{1}{16}$in from case for 10s)	240°C	260°C	260°C	260°C

Operating characteristics at 25°C

	Emitter Parameters	Low Power 306-077 (I_F = 20mA)			High Power 308-512 (I_F = 100mA)			units
		min	typ	max	min	typ	max	
P_O	Radiant Power Output	0.5	1.2		6	12		mW
λ_P	Wavelength at Peak Emission		940		915	940	975	nm
$\Delta\lambda$	Spectral Bandwidth between Half intensity points	—	—	—		50	75	nm
θ_{HI}	Beam angle — Half intensity points		8°			60°		
V_F	Forward Voltage		1.6			1.4	1.75	V
C	Capacitance (V_F = O, f = 1MHz)	—	—	—		25		pF
t_r	Rise Time I_{FM} = 20mA p.w. = 2μs		600			600		ns
t_f	Fall Time f = 45kHz		350			350		ns

Sensor Parameters		Test Conditions	Low Power 306-083			High Power 308-506			units
			min	typ	max	min	typ	max	
$V_{(BR)}$	Breakdown Voltage	$I_R = 100\mu A$, $E_e = O$				30			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = 100\mu A$, $E_e = O$	30						V
BV_{ECO}	Emitter-Collector Breakdown Voltage	$I_E = 100\mu A$, $E_e = O$	5						V
I_D	Dark Current	$V_R = 10V$, $E_e = O$					5	50	nA
		$V_{CE} = 15V$, $E_e = O$			100				
I_L	Light Current	$V_R = 10V$, $E_e = 2.5\mu W/mm^2$				10	15		μA
		$V_{CE} = 5V$, $E_e = 20mW/cm^2$	1.0	20					mA
		$V_{CE} = 5V$, $E_e = 2mW/cm^2$		2.0					
C_T	Total Capacitance	$V_R = 3V$, $E_e = O$, $f = 1MHz$					30	50	pF
V_{CE}	Collector-Emitter Sat. Voltage	$I_C = 0.5mA$, $E_e = 20mW/cm^2$		0.4					V
t_r	Rise Time	$V_R = 10V$, $R_L = 1k\Omega$					100		ns
		$V_{CC} = 30V$, $I_L = 800\mu A$, $R_L = 1k\Omega$		5					μs
t_f	Fall Time	$V_R = 10V$, $R_L = 1k\Omega$					100		ns
		$V_{CC} = 30V$, $I_L = 800\mu A$, $R_L = 1k\Omega$		5					μs

Typical characteristics

Figure 9 **Collector current vs Irradiance (306-083)**

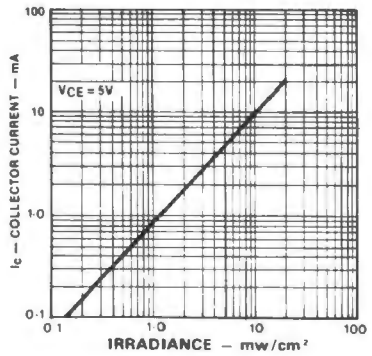


Figure 10 **Reverse current vs Irradiance (308-506)**

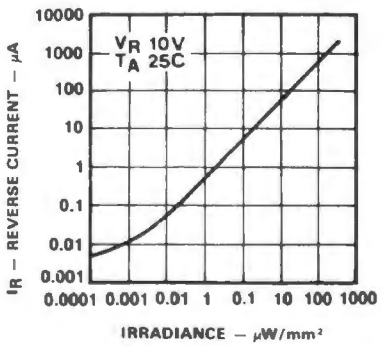
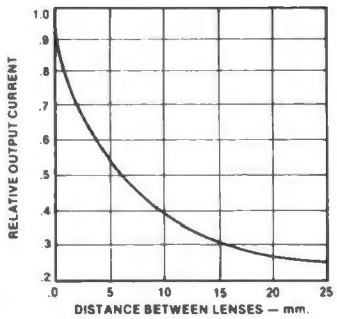


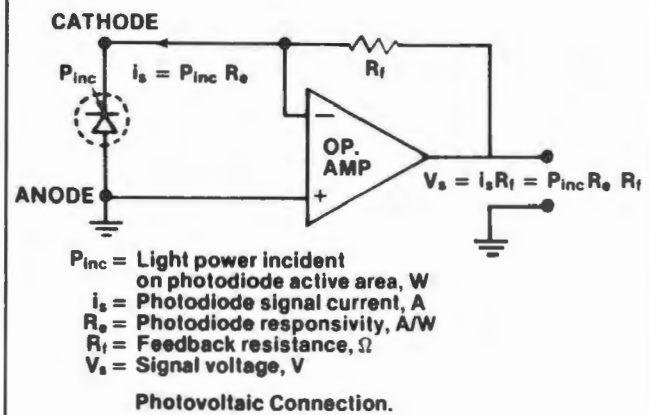
Figure 11 **Coupling characteristics of 306-077 with 306-083**



Large area photodiode

(Stock number 303-674)

A high speed, large area, silicon photovoltaic detector housed in a 26.2mm diameter case. Its large active area, 1cm², and peak spectral response at 900nm makes the device suitable for use as a calibration device in optical instrumentation, and for other optical measurements. Spectral response range (5% points): 350 to 1150nm.



P_{inc} = Light power incident on photodiode active area, W
i_s = Photodiode signal current, A
R_e = Photodiode responsivity, A/W
R_f = Feedback resistance, Ω
V_s = Signal voltage, V

Photovoltaic Connection.

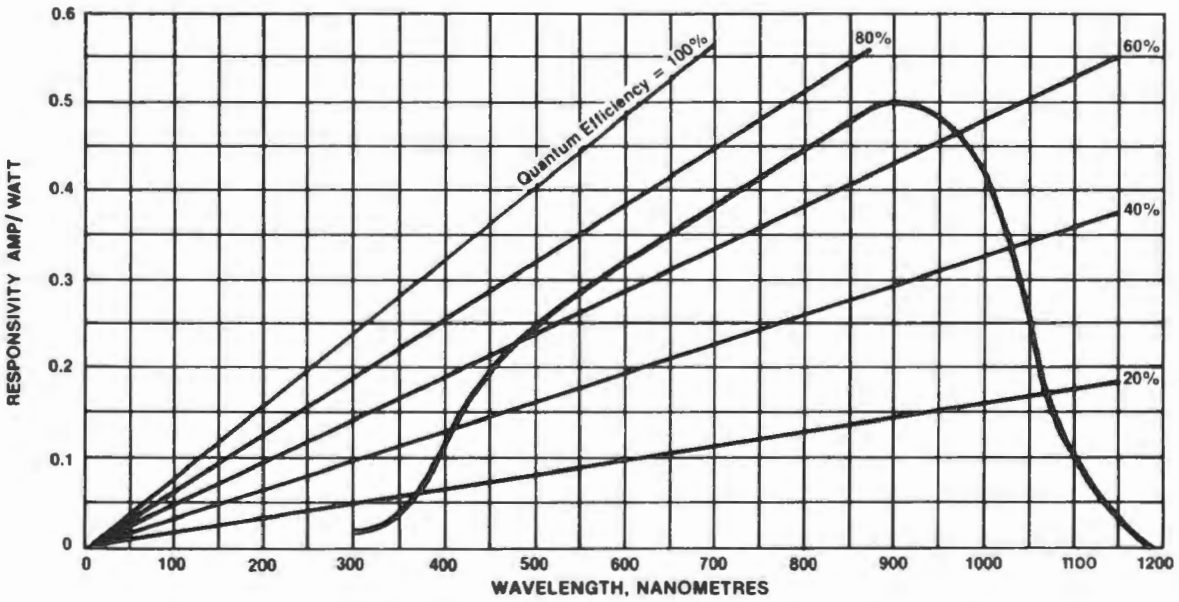
Features

- Photovoltaic operation or low-bias photoconductive operation
- High sensitivity over wide spectral range
- Circular active area (1sq cm)
- Low noise
- Fast response
- Long term stability
- Low capacitance for a photovoltaic detector

Applications

- Optical instrumentation
- Laser detection
- Optical communication

Figure 12 **Typical spectral response.**
Responsivity: 0.2A/W at 450nm., 0.35A/W at 633nm., 0.5A/W at 900nm., 0.15A/W at 1064nm., 7.9mA/lm (2850°K source).



Absolute maximum ratings at 25°C (unless stated)

Reverse voltage V_R ____ 100V
Operating temp. range ____ −55°C to +70°C
Forward current I_F ____ Limited by Pd and bias voltage
Power dissipation (at 25°C) Pd ____ 100mW

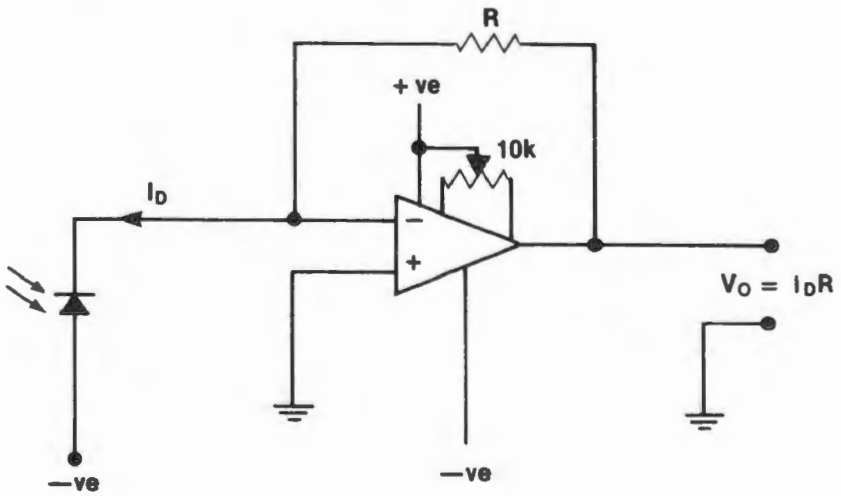
Electrical characteristics at 25°C (unless stated)

	Parameter	Test Conditions	Value min	Value typ	Value max	units
$V_{(BR)}$	Breakdown Voltage	I_D = 100μA	100			V
I_D	Dark Current	Dark, rev. bias 10V		0.5	1.5	μA
R_e	Responsitivity @ 450nm			0.2	0.22	A/W
	633nm			0.35	0.4	A/W
	900nm			0.5	0.55	A/W
	1064nm			0.15	0.16	A/W
C	Capacitance	at 0V		1500		pF
		at 10V rev. bias		350		pF
t_r	Response Time (10% to 90%)	at 0V R_L50Ω		0.5		μs
		at 10V R_L50Ω, λ<910nm		50		ns
R_s	Shunt resistance	at 0V ±0.1V		5		MΩ
I_n	Noise Current	at 0V f = 1kHz		0.1		pA(rms)
		at 10V rev. bias f = 1kHz		0.4		√Hz
NEP	Noise equiv. Power (at f = 1kHz) 450nm	at 0V		0.5		pW
		at 10V rev. bias		2		√Hz
	900nm	at 0V		0.2		pW
		at 10V rev. bias		0.8		√Hz

Applications

General purpose photodiode

Figure 13 **Linear photometer circuit using fet op. amp 307-058. Diode current I_D varies with light level from 1nA to 1mA typ. Resistor R is chosen to give required output, typ. value 1MΩ.**

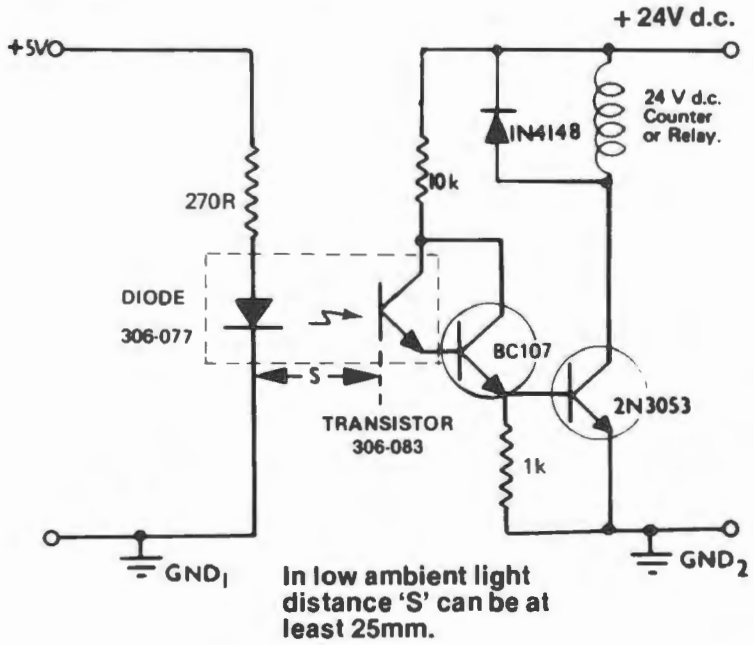


RS data

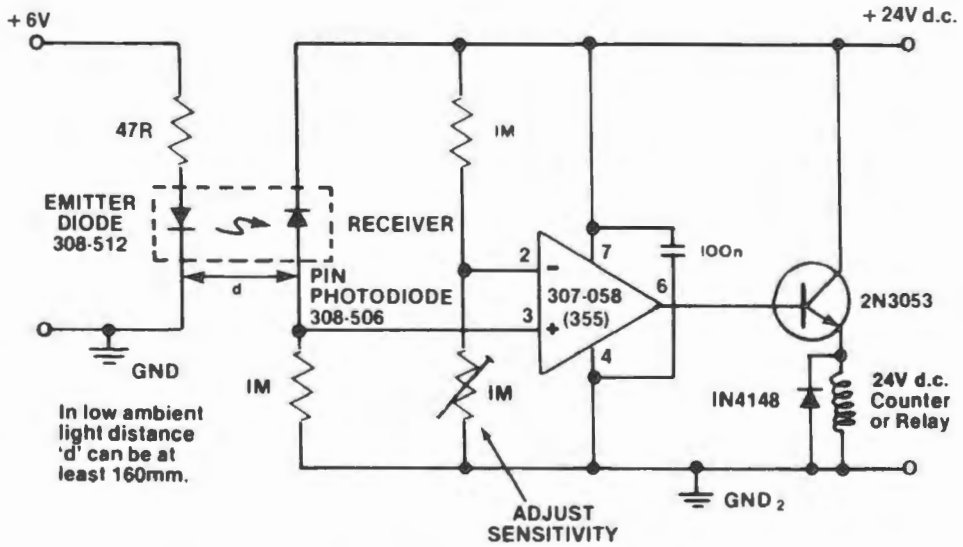
Applications

Discrete infra-red pairs

Figures 14 and 15 **Event counting or limit switching**



In low ambient light distance 'S' can be at least 25mm.



Note: With no illumination from the emitter adjust the IM trimmer, whilst the receiver is in ambient light, until the relay energises. Then reverse adjustment until the relay just de-energises. This compensates for the ambient light level.

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RS data

Waveform generators RS8038

Stock numbers 305 – 844 & 306–314

These Waveform Generators are monolithic integrated circuits capable of producing SINE, SQUARE, TRIANGULAR SAWTOOTH, RAMP and PULSE waveforms of high accuracy. The frequency can be selected externally over a range from less than 0.001 Hz to 100 kHz and is highly stable over a wide range of temperature and supply voltage.

Frequency modulation and sweeping can be accomplished with an external voltage. Two versions are available having different frequency drifts with temperature but otherwise identical specifications.

The wave form generators are suitable for audio oscillators, F.M. waveform generators, simple electronic tone generators etc.

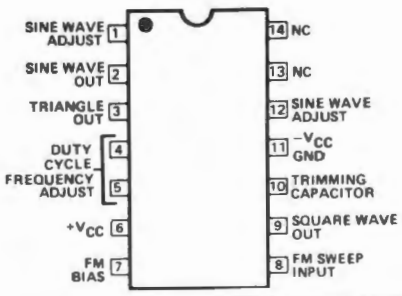
Absolute maximum ratings

Supply voltage ± 18V or 36V total
Power dissipation (see note 4) 750mW
Input voltage (any pin) not to exceed supply voltages
Input current (pins 4 and 5) 25mA
Output sink current (pins 3 and 9) 25mA
Storage temperature range – 65° to + 125°C
Operating temperature range 0°C to + 70°C

Features

- Simultaneous outputs SINE, SQUARE, TRIANGLE
- Wide frequency range 0.001 Hz to 100 kHz
- Low distortion 1 %
- Variable duty cycle 2 % to 98 %

Top view

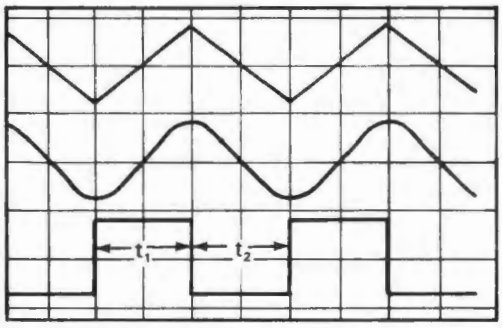


Electrical characteristics $V_S = \pm 10V$ or $+ 20V$, $T_A = 25°C$, $R_L = 10k\Omega$,

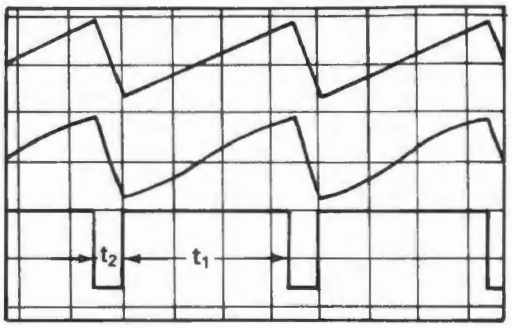
Parameter		Conditions	Min	Typ	Max	Units
Supply voltage	single supply		+10		+30	V
	dual supplies		±5		±15	V
Supply current		$V_S = \pm 10V$, Note 1		12	20	mA
Maximum oscillation frequency			100			kHz
Sweep frequency of FM				10		kHz
Sweep FM range		Note 2		40:1		
Frequency drift with temperature	305-844	Note 5		50		ppm/°C
	306-314			50	100	ppm/°C
Frequency drift with supply voltage		Over supply range		0.05		%/Vs
Recommended programme resistor		R_A and R_B	10^3		10^6	Ω
SQUARE WAVE OUTPUT	Leakage current	$V_9 = 30V$			1	μA
	Saturation voltage	$I_{SINK} = 2mA$		0.2	0.5	V
	Rise time	$R_L = 4k7$		100		ns
	Fall time	$R_L = 4k7$		40		ns
	Duty Cycle adjust		2		98	%
TRIANGLE SAWTOOTH/RAMP OUTPUTS						
	Amplitude	$R_L = 100k$	0.30	0.33		xVs
	Linearity			0.1		%
	Output Impedance	$1_{OUT} = 5mA$		200		Ω
SINE WAVE OUTPUT	Amplitude	$R_L = 100k$	0.2	0.22		xVs
	THD	$R_L = 1M$. Note 3		0.8	5	%
	THD adjusted	Use Fig. 8		0.5		%

Note 1: R_A and R_B collection currents not included.
Note 2: $V_S = 20V$; R_A and $R_B = 10k\Omega$, f = 9kHz; can be extended to 1000:1 See Figure 8.
Note 3: 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B)
Note 4: Derate at 12.5mW/°C for ambient temperatures above 100°C.
Note 5: Over operating temperature range, Fig. 1a pins 7 and 8 connected, $V_S = \pm 10V$.

Phase relationships of waveforms
Duty cycle 50 %



Duty cycle 80 %



Waveform timing

The symmetry of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 1. Best results are obtainable by keeping the timing resistors R_A and R_B separate as shown in Fig 1(a). R_A controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at $1/3\,V_{CC}$: therefore the rising portion of the triangle is,

$$t_1 = 5/3 \times CR_A$$

The falling portion of the triangle and sine-wave and the O state of the square-wave is:

$$t_2 = 5/3 \times \frac{R_A R_B C}{2R_A - R_B}$$

Thus a 50 % duty cycle is achieved when $R_A = R_B$.

If the duty cycle is to be varied over a small range about 50% only, the connection shown in Figure 1(b) is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorter together; as shown in Figure 1(c). This connection, however, carries an inherently larger variation of the duty-cycle.

Using two separate timing resistors of equal value, (Figure 1a) the frequency is given by

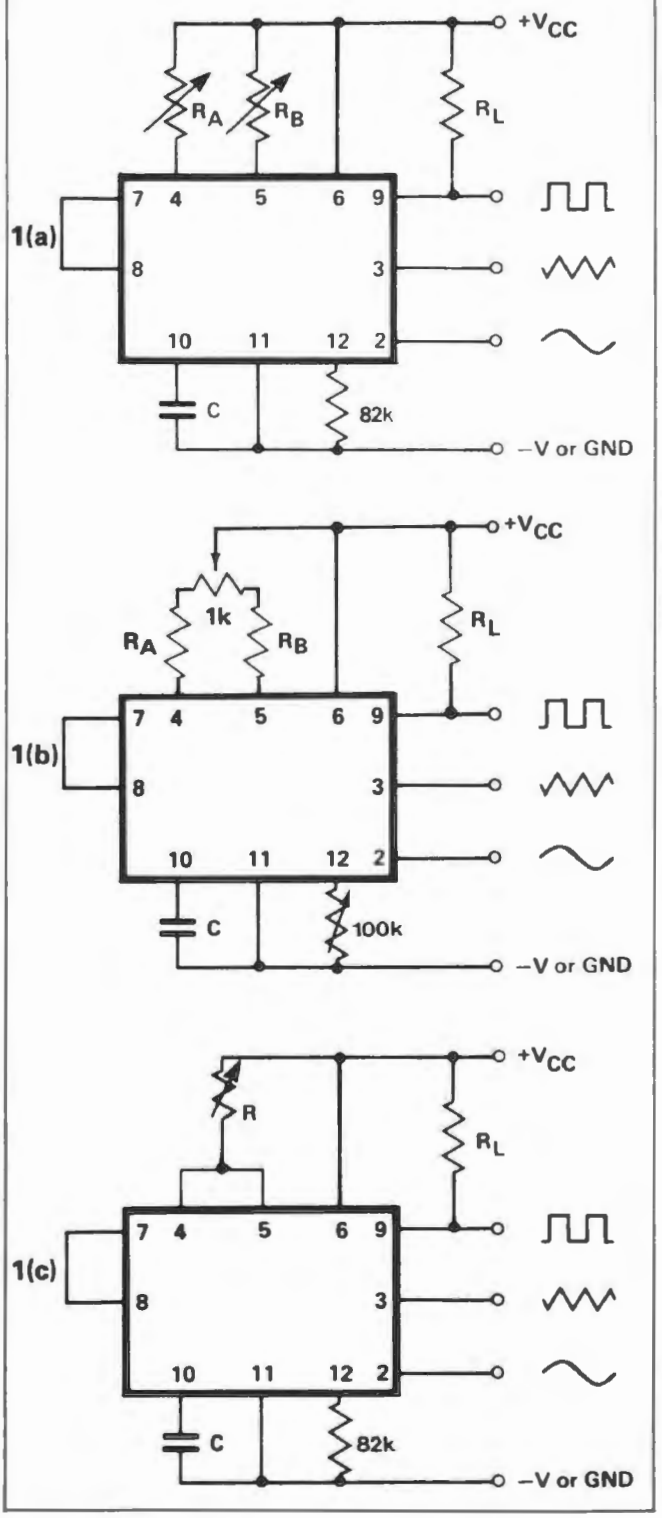
$$f = \frac{0.3}{RC} \qquad (R = R_A = R_B)$$

If a single timing resistor is used (Figure 1(c), the frequency is

$$f = \frac{0.15}{RC}$$

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that currents and thresholds are both direct linear functions of the supply voltage and thus their effects cancel.

Figure 1 **External timing resistor connections**



Selecting R_A, R_B and C

For any given output frequency, there is a wide range of RC combinations that will work. However certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less that 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher current (I > 5 mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will be obtained for charging currents of 10 μA to 1 mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{V_{CC}}{5R_A} \quad (R = R_A \text{ or } R_B)$$

For optimum stability capacitor C should be a low temp. coefficient type, e.g. silvered mica, polystyrene, etc.

Note: Pins 7 and 8 are susceptible to pick-up, therefore a 100 nF capacitor connected from + V_{CC} to pin 8 is often advisable.

Waveform level and power supplies

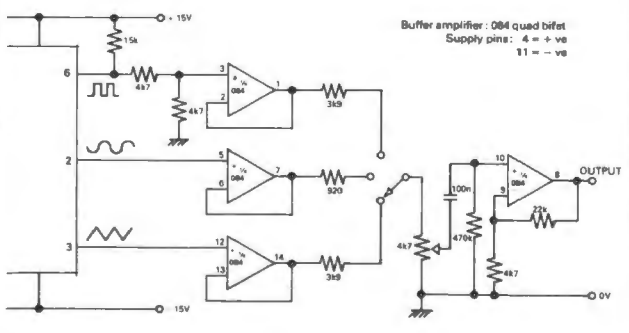
The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (± 5 to ± 15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between +V and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output pin 9 is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30 V). In this way the square-wave output may be made TTL compatible (load resistor connection to + 5 Volts) while the waveform generator itself is powered from a higher voltage.

Output buffering

To prevent overload, with resultant waveform distortion and to provide maximum amplitude the output should not be connected to a load of less than 100kΩ. In some applications an output buffer may therefore be required. Fig. 2 shows a comprehensive buffer circuit allowing amplitude adjustment and waveform selection. Using the component values indicated the selected waveforms will have nominally the same output amplitude.

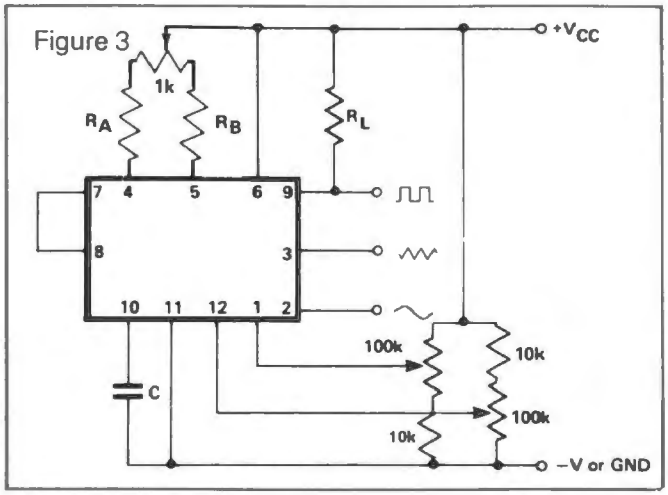
Figure 2



Sine wave distorton

To minimize sine-wave distortion the 82kΩ resistor between pins 11 and 12 is best made a variable one. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 3. This configuration allows a reduction of sine-wave distortion close to 0.5%.

Figure 3



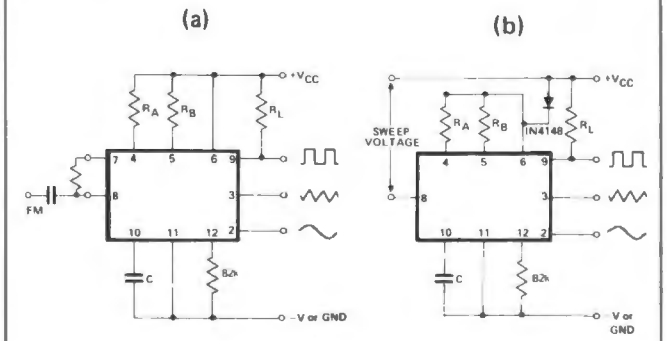
Frequency modulation and sweeping

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from + V_{CC}). By altering this voltage, frequency modulation is performed.

For small deviations (e.g. ± 10%) the modulating signal can be applied directly to pin 8, merely providing dc decoupling with a capacitor, as shown in Figure 4(a). An external resistor between pins 7 and 8 is not necessary, but can be used to increase input impedance. Without it (i.e. terminals 7 and 8 connected together), the input impedance is 8kΩ; with it, this impedance increases to (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 4b). In this way the entire bias for the current sources is created by the modulating signal and a very large (e.g. 1000:1) sweep range is created (f=0 at V_{sweep} = 0). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept from V_{CC} to (2/3 V_{CC} + 2V).

Figure 4



Typical application circuits

Audio oscillator

A versatile audio oscillator giving selectable sine, square and triangular outputs from 20Hz to 18kHz without the need to switch range. This wide range of adjustment is achieved by connecting the F.M. sweep input to the 'Frequency' setting potentiometer which adjusts a d.c. control voltage. To ensure good waveform purity and provide nominally the same output amplitude for each waveform this circuit features a comprehensive buffer circuit using the superior a.c. performance of a quad op-amp.

A suitable p.c.b. is available, (Stock No. 435-226), when combined with an appropriate power supply this may be used to produce a general purpose instrument for use where either fixed or variable frequency waveforms are required.

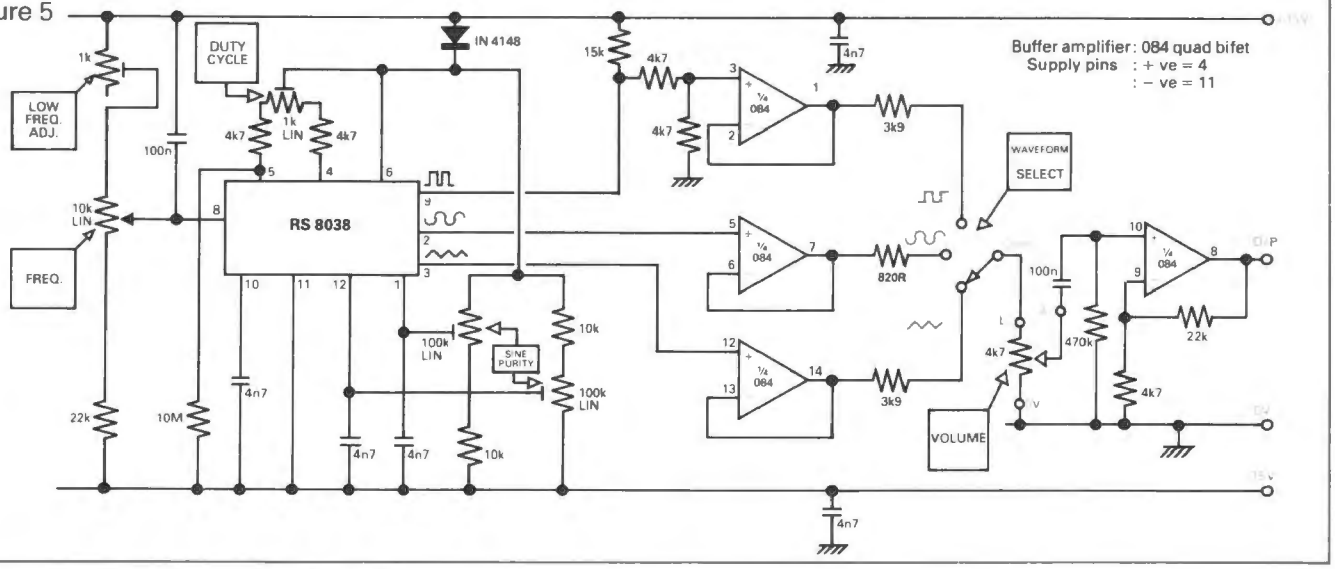
Setting Up Procedure

With a frequency of approximately 1kHz selected adjust the 'Duty Cycle' for equal mark/space ratio on a square wave output displayed on an oscilloscope and then adjust the 'Sine Purity' controls for minimum distortion of a sine wave output.

Adjust 'Low Frequency' preset so that with the 'Frequency' potentiometer set for minimum, frequency output is at 20Hz.

Note: Some deviation from 50% duty cycle will occur at low frequencies using this circuit.

Figure 5



Audio oscillator parts list

Device Type	Stock No.	Quantity
Semiconductors		
8038BC	306-314	1*
8038CC	305-844	1*
084 Quad bifet	304-201	1
IN4148	271-606	1
Resistors		
4k7 metal film	148-663	5
10k metal film	148-736	2
22k metal film	148-815	2
3k9 metal film	148-641	2
15k metal film	148-770	1
470k metal film	149-149	1
820R metal film	148-483	1
10M high stability carbon film 0.5W	133-330	1
Capacitors		
4n7 monolithic ceramic	125-761	4
100n monolithic ceramic	125-806	2
4n7 polystyrene	113-364	1
Trimmers		
1k 3/8" square cermet	186-716	2
100k 3/8" square cermet	186-772	2
10k 3/8" cermet multiturn	186-520	1
Miscellaneous		
14 pin, turned pin dil socket	402-305	2
Vertical P.C. terminal block	423-762	3
Printed Circuit Board	435-226	1
4k7 Potentiometer (Volume control mounted off board)		1
3-way switch (Waveform select mounted off board)		1

*Temperature coeff. 50ppm/°C typ. for both types. 8038BC type has guaranteed max. temperature coeff. of 100ppm/°C.

Simple tone generator

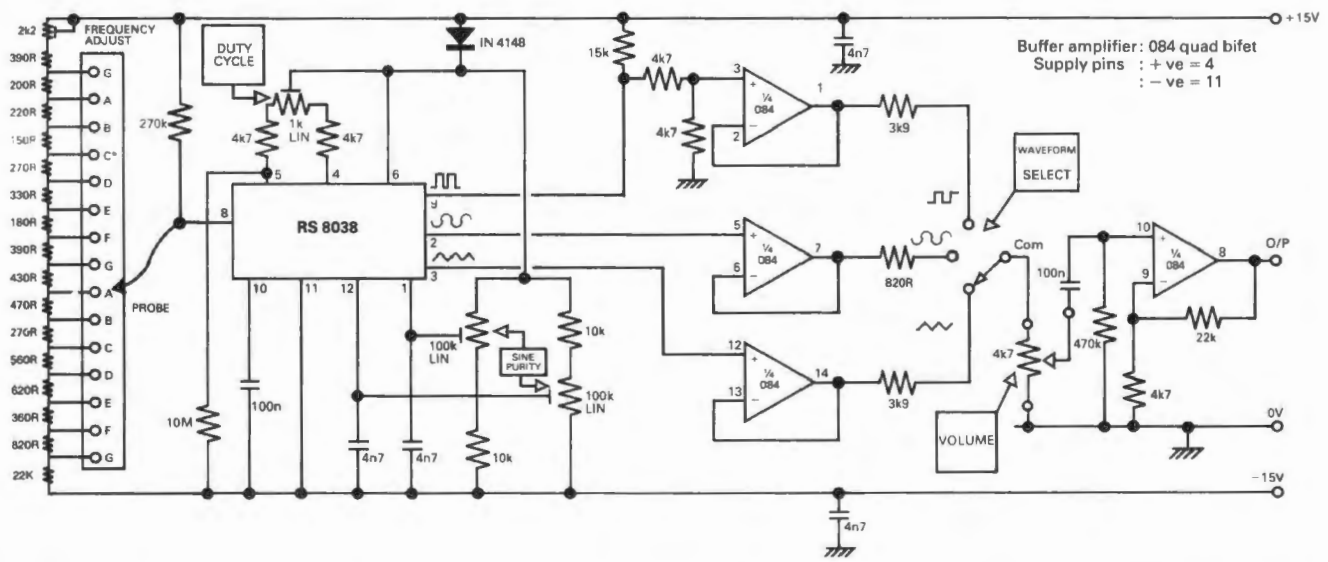
A development of the Audio Oscillator circuit above; this tone generator when used in conjunction with an audio amplifier and loudspeaker makes an effective instrument, even in this simple form.

Setting up procedure

Connect the 'Probe' to A° above middle C and adjust 2.2kΩ frequency adjust to give output frequency of 440Hz. (If frequency counter not available adjust A note against a Piano 'by ear'.) With A note selected adjust the 'Duty Cycle' on the square wave for equal mark/space ratio on the square wave output displayed on a scope and then adjust the 'sine purity' controls for minimum distortion of the sine wave displayed on a scope.

[Note: Values of resistance used are nearest preferred values]

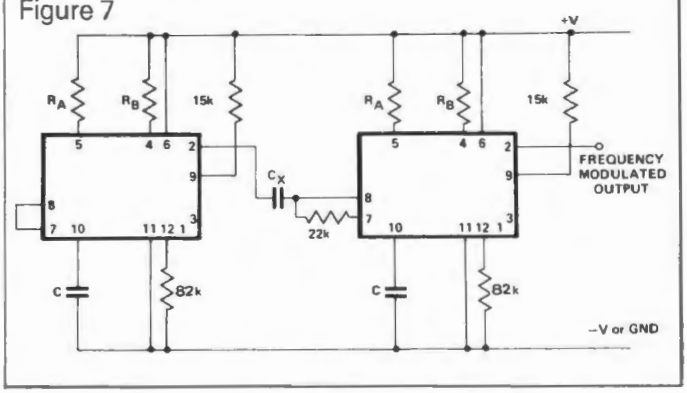
Figure 6



Frequency modulation

The circuit opposite illustrates the basic method whereby two Waveform Generator I.C's can be used to achieve a frequency modulated Waveform. In this mode the first I.C. produces a sine-wave which is coupled via C_X to the second I.C. where it modulates its set frequency by up to 10 per cent as desired. The value of C_X should be chosen to suit the modulating frequency. Refer to previous information to determine values of R_A, R_B, C to set the frequency of each oscillator.

Figure 7



RS data

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RS data

19″ Sub-rack system

Please read this Data sheet in full before proceeding to assemble a Sub-rack

The RS 19″ Sub-rack system is a versatile method of accommodating modules and/or printed circuit boards. The system is 3 Units (5¼″) high and will accommodate boards up to 203mm in length. When used as a card only system it can be adjusted to accept RS stripboards or other standard cards between 95mm and 114mm in height.

Before assembling a 19″ Sub-rack, all system requirements should be considered, and the final form decided upon.

Card system only

The spacing between cards is the first consideration. This system offers the option of a 0.2″ or 0.5″ pitch. The final choice will be dependant on the number of cards to be accommodated and the final width of the card when components are mounted. The appropriate Guide Location Strips may then be selected. If it is also intended to use edge connectors, then Tapped Strips of the same pitch as the Guide Location strips will be required.

The front of the Sub-rack may be covered, either with an overall hinged panel, or by fitting Card Fronts to each card.

Module/Card front system

As an alternative to the card only system, Modules, or a mixture of Modules and cards with Card Fronts can be accommodated in the Sub-rack. For this system 0.5″ pitch Guide Location Strips must be used.

This 19″ Sub-rack is an extremely flexible system with many assembly variations. The final system should be carefully considered and planned, to help ensure that the correct components are obtained, in the correct quantity.

If Tapped Strips ⑦ or ⑧ and Guide Location Strips ⑨ or ⑩ are required, they must be inserted into the rail extrusions before the Sub-rack is assembled.

Guide Location Strips are fitted into all four guide mounting rails as shown. Two Tapped Strips (which must be of the same pitch as the Guide Location Strips) are inserted into the Connector Mounting Rails to retain the edge connectors. Two more Tapped Strips may also be inserted into the Front Guide Mounting Rails to retain Modules and/or Card Fronts.

The Ident Strips may be inserted into the Front Guide Mounting Rails, if Modules or Card Fronts are not used. They may then be marked to identify board positions.

Having inserted the appropriate items, the rails can then be fixed to the end plates and end plate angles using the Pozidrive™ self-tapping screws provided. (A No. 2 point Pozidrive™ screwdriver is recommended.) Lubricating the threads will aid the self-tapping action. The rails should be spaced apart front and rear to suit the card guides and board used. The vertical rail separation can be adjusted to suit the board height. It is recommended that the lower rails are left at their lowest position and the top rails lowered to the desired height.

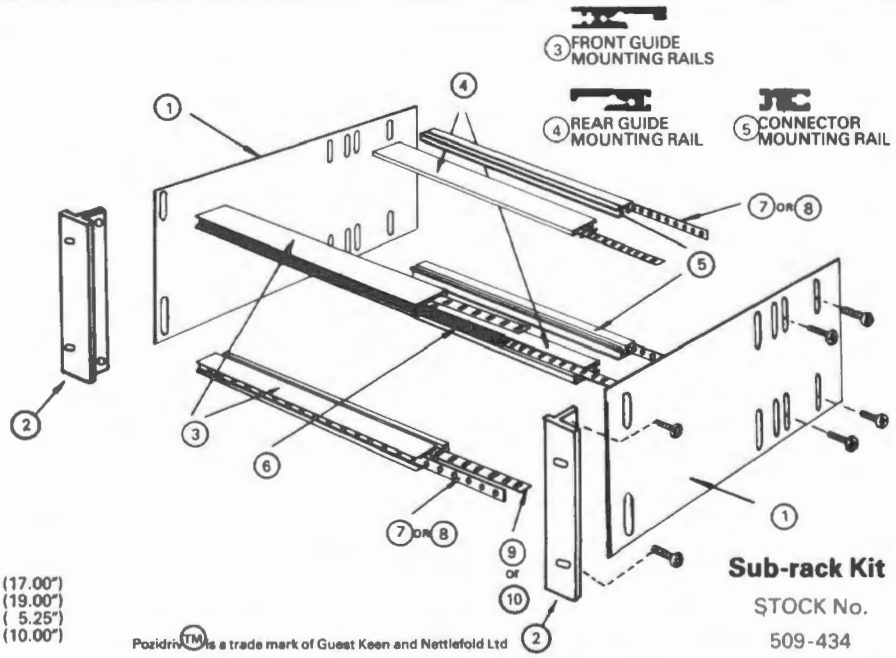
The basic Sub-rack is now ready to accept single cards and connectors, as desired. Instructions for fitting these and other items can be found under the appropriate section of this data sheet.

Sub-rack assembly instructions

Sub-rack kit consists of:

① 2-End Plates
② 2-End Plate Angles
③ 2-Guide mounting rails (front)
④ 2-Guide mounting rails (rear)
⑤ 2-Connector mounting rails
⑥ 2-Ident strips

14-Pozidrive™ self-tapping screws (two spares)



Sub-rack: Standard 19″ Fixings	
Lengths of Rails	431.80mm (17.00″)
Overall Length	482.60mm (19.00″)
Height (3U)	133.35mm (5.25″)
Depth	254.00mm (10.00″)

Sub-rack Kit
STOCK No.
509-434

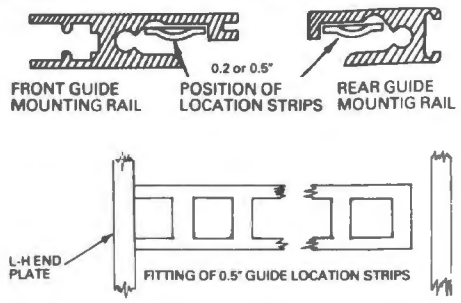
Pozidriv™ is a trade mark of Guest Keen and Nettlefold Ltd

Guide location strips

The Guide Location Strips should be fitted into the Front Guide Mounting Rails and the Rear Guide Mounting Rails as shown. The pitch of the Tapped Strips should be chosen to match the pitch of the Guide Location Strips.

When housing Modules or Modules and Card Fronts, 0.5" Guide Location Strips are used.

The 0.2" Guide Location Strip is symmetrical and may be inserted either end first, the 0.5" type must be inserted as shown with the open end adjacent to the left-hand end plate.



	Stock number
0.2" Guide Location Strips	509-440
0.5" Guide Location Strips	509-456

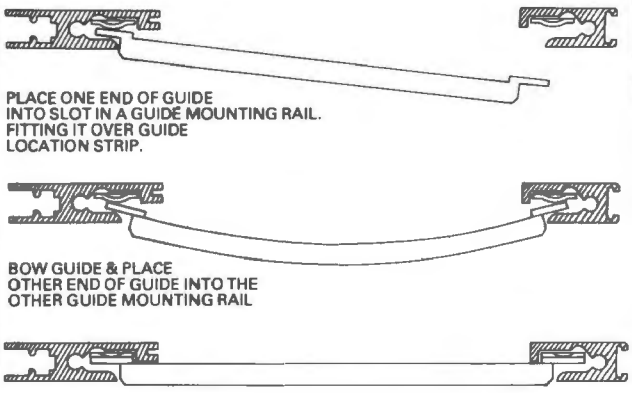
4 per pk.

Card guides

Card Guides may be clipped into the Sub-rack provided the appropriate Guide Location Strips have been fitted to the Guide Mounting Rails. With 0.2" Guide Location Strips fitted, board spacings with multiples of 0.2" may be obtained. 0.4" being the minimum board spacing. With 0.5" Guide Location Strips fitted, card spacing on multiples of 0.5" may be obtained, 0.5" also being the minimum spacing.

When housing Modules or Modules and Card Fronts, guides are used on a 0.5" pitch. Two guides per card and four guides per module are required. Care should be taken to see that when the guides are clipped on the rails they are at 90° to the rails and that they line up with the appropriate connectors mounted on the Connector Mounting Rails. Using an actual board will help to ensure that the guides and connectors are correctly aligned.

Method of clipping card guides to guide mounting rails



	Stock number
Card Guides	509-507

10 per pk.

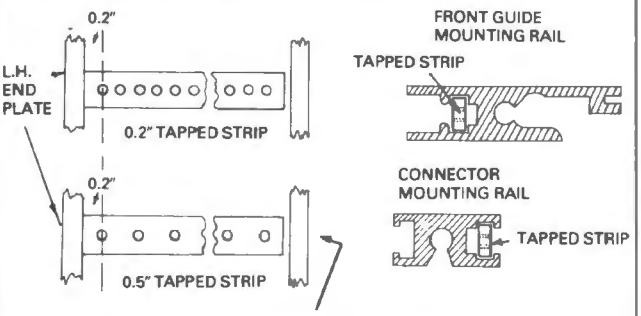
Tapped strips

Tapped Strips may be fitted into the Connector Mounting Rail to retain connectors.

The first available card position is 0.2" from an end plate, and the Tapped Strips must be inserted so this can be achieved as shown in the diagram.

0.5" pitch Tapped Strips may also be inserted into the Front Guide Mounting Rail to retain Modules and Card Fronts.

Fitting of tapped strips



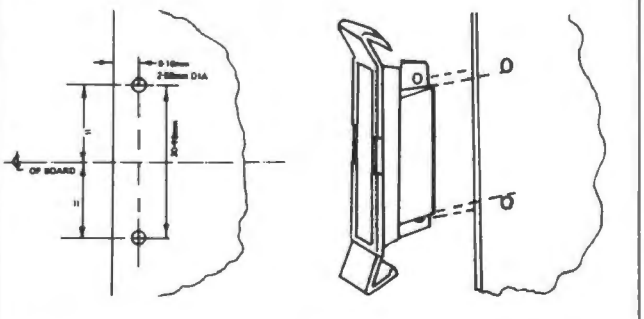
	Stock number
0.2" Tapped Strips	509-462
0.5" Tapped Strips	509-478

2 per pk.

Card handles

The Card Handles may be clipped on to the front edge of stripboards to aid removal. The Hinged Front Panel (Stock No. 508-891) may be used to cover up the cards and handles if desired.

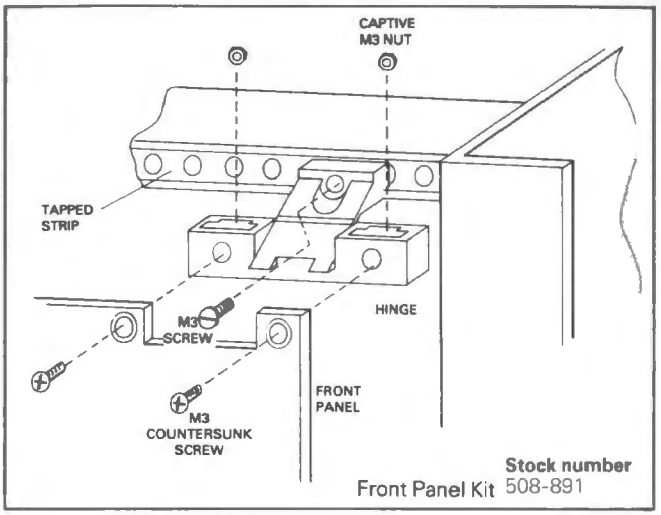
Card Handles



	Stock number
Card Handles	509-513

Hinged front panel kit

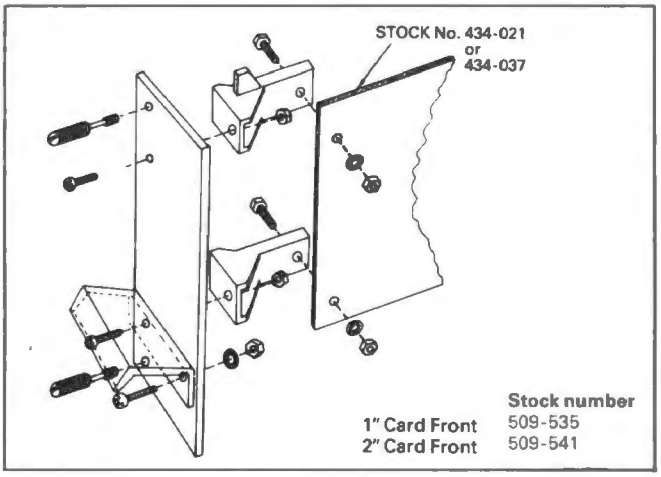
The Front Panel kit may be used to cover the front of the Sub-rack. It cannot be used when Modules or Card Fronts are fitted in the Sub-rack. The front panel should be assembled to the Sub-rack frame using the two plastic hinges and screws as shown. It may be mounted to hinge from either the top or the bottom of the Sub-rack.



Stock number
Front Panel Kit 508-891

1" and 2" Card Fronts

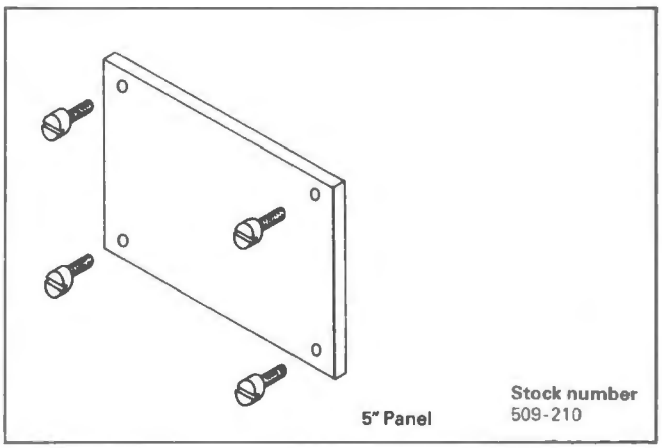
The Card Fronts may be used as a system in their own right, or mixed in a system with Modules. Please Note: Card Fronts are only suitable for use with 114 × 203mm stripboards fitted into Card Guides on a 0.5" pitch. The front panel is retained in the Sub-rack using two knurled screws, which engage in the 0.5" Tapped Strips fitted in the front guide mounting rails of the Sub-rack. Assemble Card Front as shown in the diagram.



Stock number
1" Card Front 509-535
2" Card Front 509-541

5" Front panel

This Card Front may be used to mount meters and controls. It is retained in the Sub-rack by 4 screws which engage in the 0.5" Tapped Strips fitted in the front guide mounting rails of the Sub-rack. Note: This card front is not drilled to accept cards and has no handle.



Stock number
5" Panel 509-210

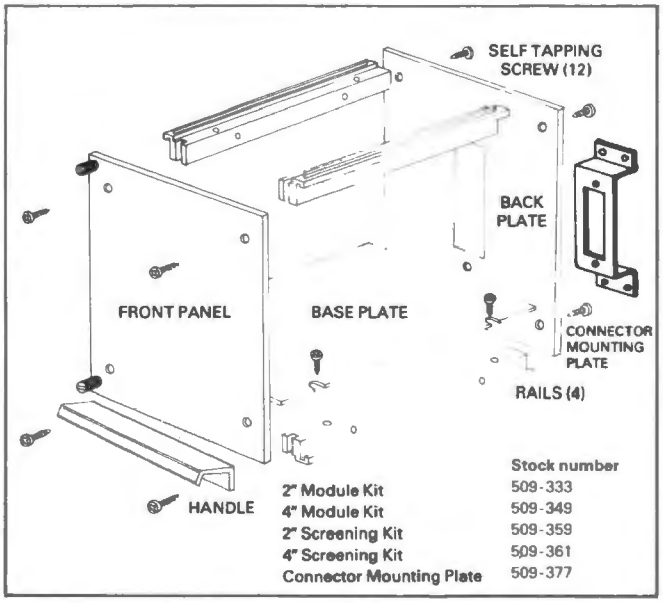
2" and 4" modules

May be used in an all module system, or mixed in a system with Card Fronts mounted on cards. Modules are used with Card Guides on a pitch of 0.5". The front panel is retained in the Sub-rack using knurled screws, which engage in the 0.5". Tapped Strips fitted in the front guide mounting rails of the Sub-rack. Assemble modules as shown in the diagram.

The back plate of the module is pre-cut to accept a 24 way plug (467-009). The Connector Mounting Plate accepts mating 24 way socket (467-015).

Modules are supplied with a baseplate which can be used for transformer mounting etc. Separate screening kits, consisting of a top and two side plates, are available. In addition to screening they provide useful surfaces onto which circuit boards may be mounted.

Note. A maximum of 16" of the 17" rack width available can be fitted with 2" and 4" modules. The remaining 1" may be filled with a 1" Card Front used either with, or without a card.



	Stock number
2" Module Kit	509-333
4" Module Kit	509-349
2" Screening Kit	509-359
4" Screening Kit	509-361
Connector Mounting Plate	509-377

RS data

Connector mounting

Method A

Connectors or module Connector Mounting Plates may be mounted by using the appropriate Tapped Strips in the Connector Mounting Rails and then inserting screws through the end feet and into the Tapped Strips.

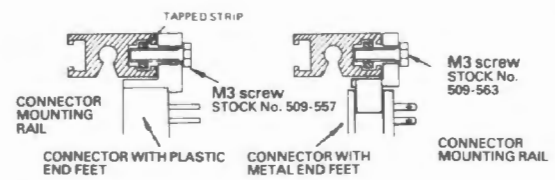
The first available card position is 0.2" from an end plate, and the Tapped Strip must be inserted so this can be achieved.

Module/Stripboard Type	Suitable Connector	Suitable Screws
2 or 4in Module	467 015 (mounted in 509-377)	509-563
114 × 203mm single-sided board	466-999 or 467-043 wirewrap	509-563 509-563
114 × 203mm double-sided board	467-021 or 467-059 wirewrap	509-563 509-563
95.5mm *high single-sided board	466-551 or 467-037 wirewrap	509-557 509-563

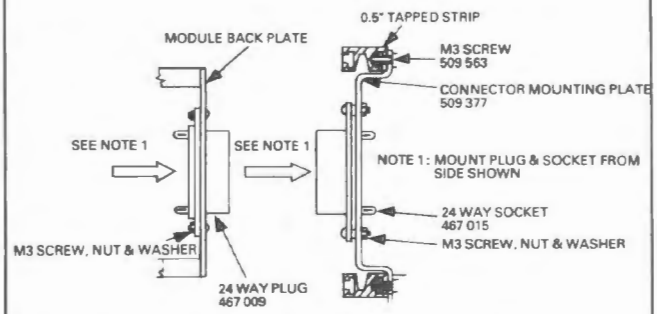
* not suitable for card fronts

Note · Two screws per edge connector and four per Connector Mounting Plate are required

Method A



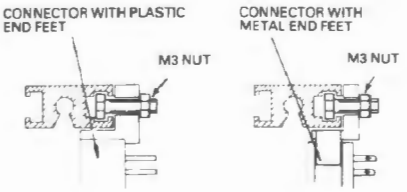
Module Connector Mounting using Method 'A'



Method B

Alternatively, connectors can be mounted without using Tapped Strips, by inserting the head of the screw into the slot normally occupied by the Tapped Strip (see Drawing). This means that each connector must be individually positioned. It is usually more convenient to insert a card into the guide to ensure correct alignment of card and edge connector.

Method B



System selection guide

This chart indicates some of the assembly possibilities and the components needed. For suitable Stripboards and connectors refer to catalogue.

	Stock No.	0.2in pitch Connector Mounting Method A Card Handles Guides	0.2in pitch Connector Mounting Method B Card Handles Guides	0.5in pitch Connector Mounting Method A Card Handles Guides	0.5in pitch Connector Mounting Method A Modules/ Card Fronts Guides	0.5in pitch Connector Mounting Method B Card Handles Guides	0.5in pitch Connector Mounting Method B Modules/ Card Fronts Guides
Sub-Rack	509-434	1	1	1	1	1	1
0.2in Tapped Strip	509-462	1 pk					
0.5in Tapped Strip	509-478			1 pk	2 pk		1 pk
0.2in Guide Location Strips	509-440	1 pk	1 pk				
0.5in Guide Location Strips	509-456			1 pk	1 pk	1 pk	1 pk
Guides	509-507	*	*	*	*	*	*
Card Handles	509-513	*	*	*		*	
Hinged Panel (if required)	509-891	1	1	1		1	
Instrument Case (if required)	508-778	1	1	1	1	1	1
Card Fronts 1in	509-535				*		*
Card Fronts 2in	509-541				*		*
Modules 2in	509-333				*		*
Modules 4in	509-349				*		*
5in Front Panel	509-210				*		*
Screening Kit 2in	509-355				*		*
Screening Kit 4in	509-361				*		*
Connector Mounting Plate	509-377				*		*
M3 Screws	See Chart Above	1 pk	1 pk	1 pk	1 pk	1 pk	1 pk
M3 Nuts	522-421		1 pk			1 pk	1 pk

* Quantity as required

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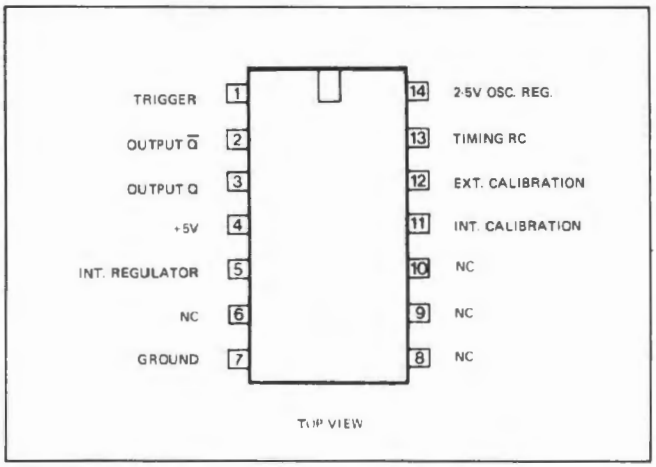
Precision timer i.c. ZN1034

Stock number 305-850

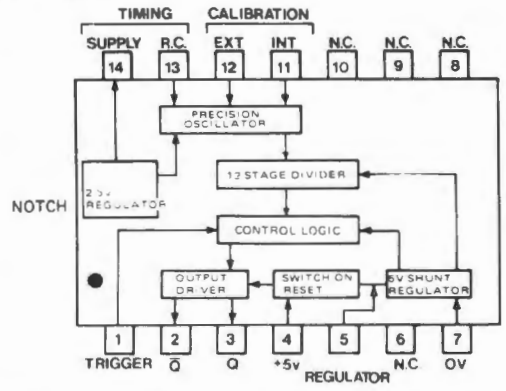
A digital i.c. in a 14 lead DIL package equivalent to ZN1034, providing precise timing intervals from 50ms up to several days. The frequency of an "on-chip" oscillator is determined by an externally connected capacitor and resistor. Additional trimming over a 3:1 range may be achieved by connection of a calibration potentiometer. Pulses from this oscillator are fed through a 12 stage binary divider which changes the state of the outputs after 4095 counts.

Features

- Temperature stability 0.01%/°C
- Repeat timing accuracy 0.01%
- Low current consumption 5mA
- Internal supply voltage regulator
- Complementary TTL compatible outputs
- Single, repetition or cascade operation
- Output current up to 25mA



Block diagram



Electrical characteristics (T_A = 25°C and I supply = 5mA unless otherwise specified)

Operating temperature range 0°C to 70°C

Parameter	Comments	Min.	Typ.	Max.	Units
TTL Positive Supply	See Section 2	4.75	5.00	5.25	Vd.c.
Unregulated Supply	See Section 2	6	–	450	Vd.c.
Supply Current	See Section 2	–	5	50	mA
5V Regulator Quiescent Current	See Section 2	–	2	–	mA
Timing Capacitor C_T	See Note 1	3300	–	–	pF
Timing Resistor R_T		5K	–	5M	Ω
Calibration Resistor R_{CAL}	See Section 1	45	150	300	kΩ
Time Period Temperature Coefficient (Not including external components)					
Internal Calibration		–	±0.01	–	%/°C
External Calibration	See Section 1	–	±0.1	–	%/°C
Repetitive Timing Accuracy	With temp. voltage and timing comps. unchanged.	–	±0.01	–	%
Time Period T	See Section 1	–	–	–	–
Trigger Input High	Open Circuit permissible. See Section 3. Minimum external sink current 70µA.	2.2	–	2.5	V
Low		0	–	1.0	V
Complementary Outputs (Pins 2 and 3)					
High	See Section 4.	2.5	3	–	V
Low	Sink 25mA, Source 25mA	–	0.2	0.4	V
Propagation Delay from $V_{trigger}$ low to V_{out} high		–	2	–	µS
Output Current	See Section 4	–	–	25	mA

1) Timing period

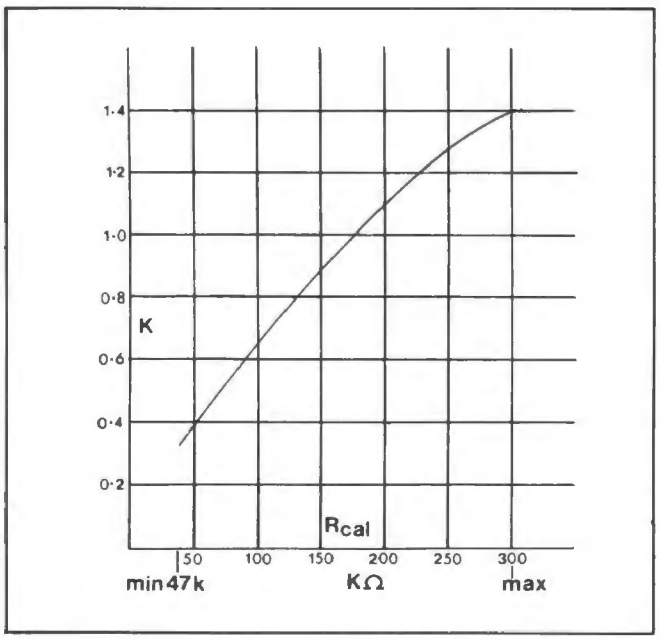
The final period, T is directly related to the oscillator period set by an external resistor R_t and capacitor C_t. This relationship can be shown as

$T = K.4095. R_t. C_t.$

where T in seconds; C in farads

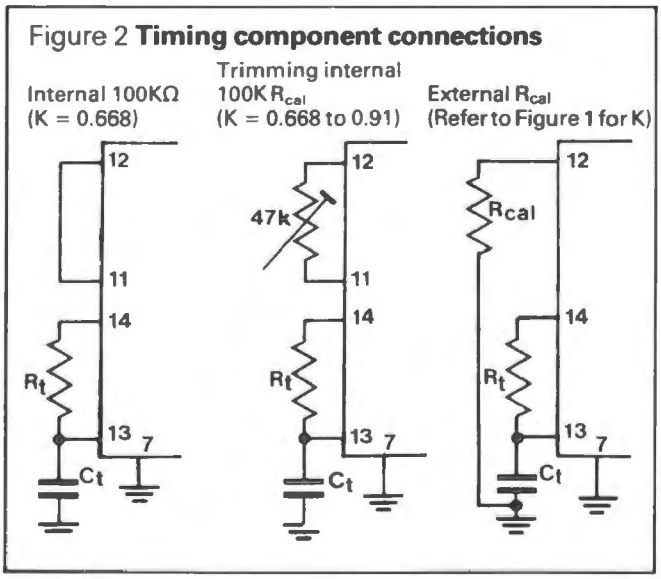
R_t in ohms; K is constant (see below)

The magnitude of the constant K is determined by the value of calibration resistance, R_{cal}. Figure 1 shows the change in K versus R_{cal}.



The internal calibration resistor, value 100K, should be used for the best temperature stability, but external resistors may be used. These options are shown in Figure 2.

Figure 2 **Timing component connections**



Approximate values of C_t and R_t for selected time periods, T are shown in Table 2 (below).

C_t	R_t	R_{cal} = 100KΩ	R_{cal} = 300KΩ
0.01μF	39K	1 sec	2.9 sec
0.1μF	220K	1 min	2.7 min
1μF	100K	5 min	12.5 min
1μF	1.2M	1 hr	2.5 hrs
10μF	3.3M	1 day	2.7 days
100μF	2.2M	1 week	2.7 weeks

2) Power supply connections

The timer may be operated directly from a 5V d.c. supply as shown in Figure 3 or by incorporating the internal regulator a smooth d.c. supply from 6 to 450 volts may be used as shown in Figure 4.

Figure 3

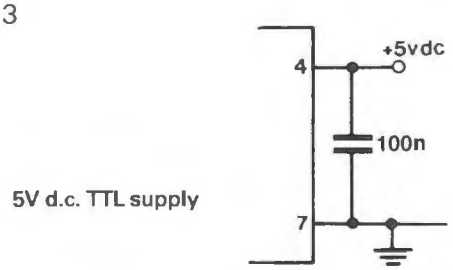
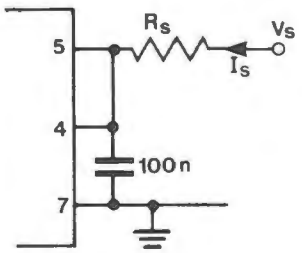


Figure 4



The value of R_s in kΩ may be determined by the following formulae

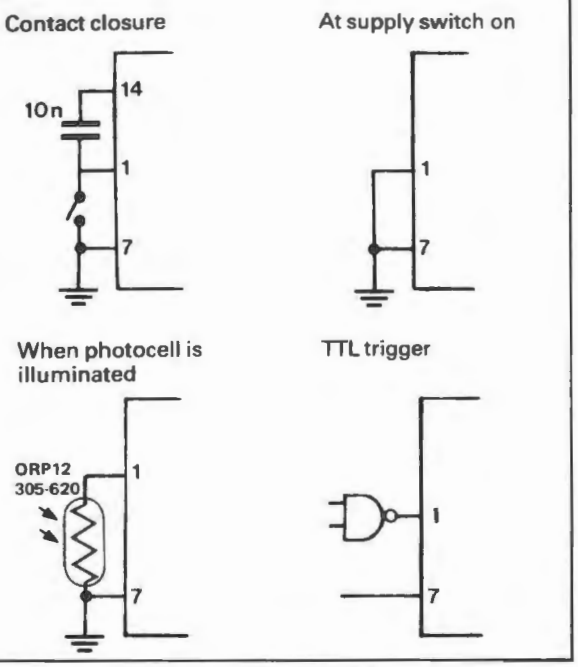
$$R_s = \frac{V_s - 5}{I_s}$$

The value of I_s is calculated by adding the device quiescent current of 7mA to the required on state output current. I_s should be limited to a maximum of 50mA.

3) Trigger options

A negative going edge on pin 1 initiates the timing cycle. Methods of triggering the timer are shown in Figure 5.

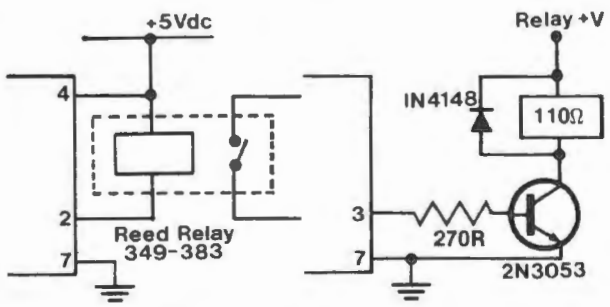
Figure 5



4) Outputs

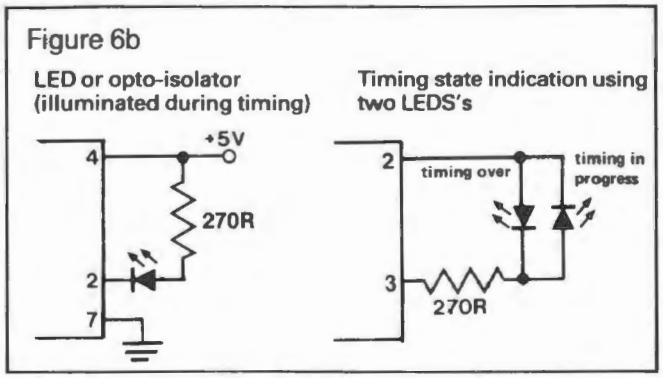
The two complementary outputs pins 2 and 3 may drive various loads, both outputs being capable of supplying 25mA (source or sink). Various output connections are shown in Figure 6. If the opposite mode of operation is required connect the load to the other output.

Figure 6a



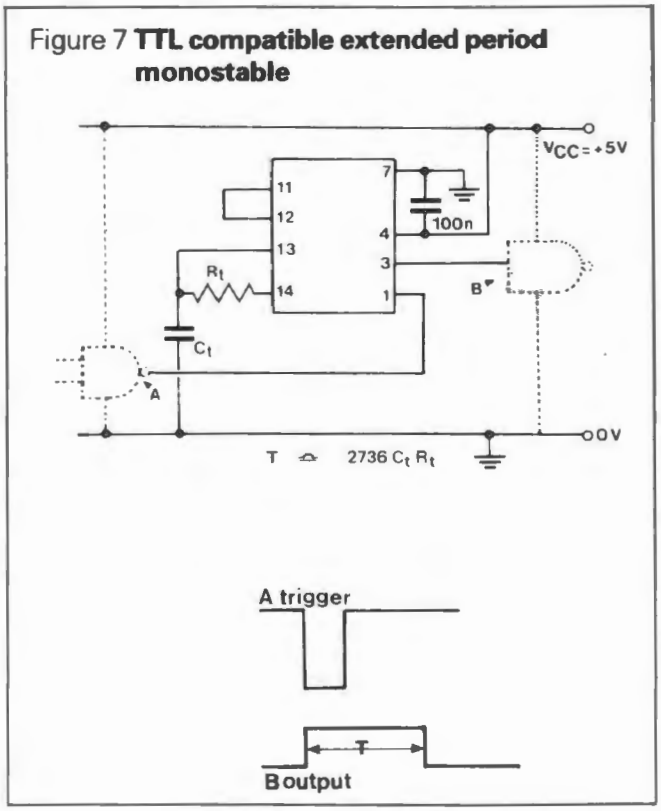
Relays energised during timing

Figure 6b



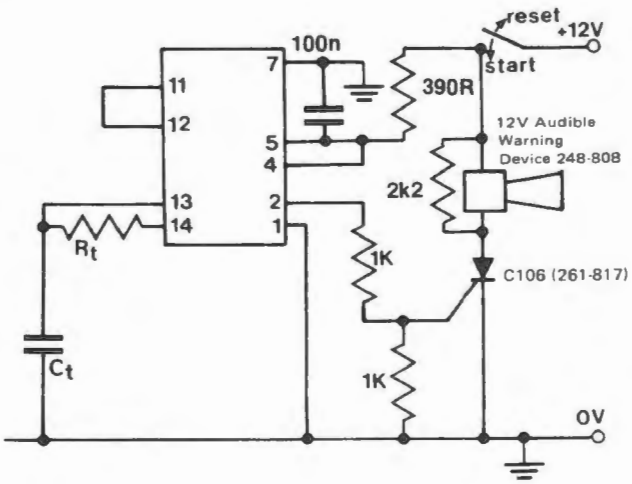
Typical applications

Figure 7 **TTL compatible extended period monostable**



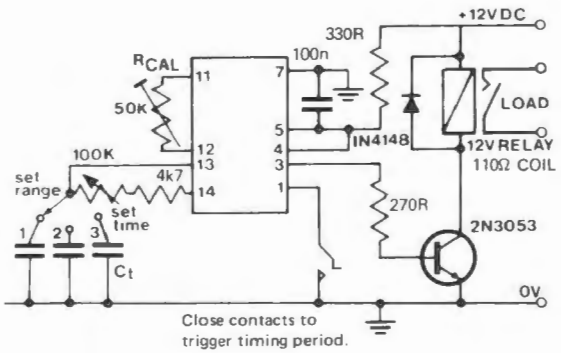
RS data

Figure 8 **Timer with audible alarm**



Alarm sounds after preset delay time which is triggered by "start" contacts closing. Alarm continues until "reset" is operated.

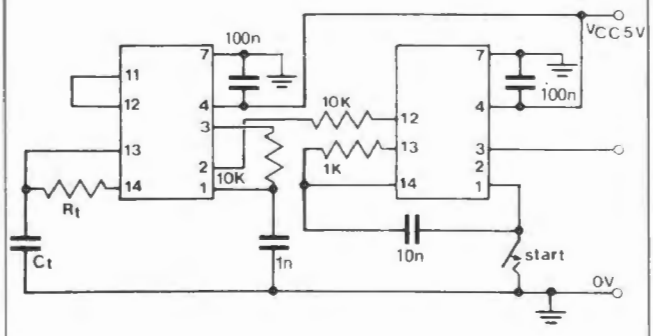
Figure 9 **Multi-range timer**



Range	C_T
0.5 – 10 sec	0.047uF
5 – 100 sec	0.47uF
50 – 1000 sec	4.7uF

Relay is energised during timing period

Figure 10 **Cascade operation**



First timer is arranged in the repetitive operating mode and its output is further divided down in the second timer.

$$T \simeq 11 \times 10^6 C_t R_t$$

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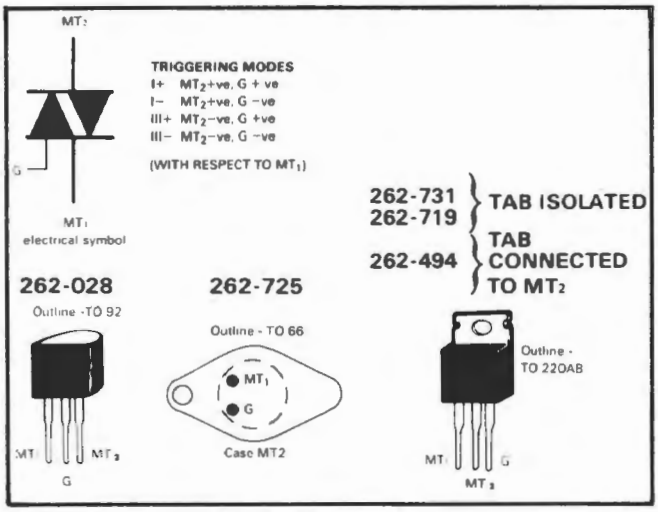
RS data

Triacs

A range of triacs suitable for use in power control, lamp dimming and heater control circuits. T0-92, T0-66, tab mounting and stud mounting versions available.



Features

- T0-92 plastic: 400 V
- T0-66 outline: 400 V
- tab mounting: 400/800 V
- stud mounting:400/1200 V

List of near equivalents	
Old types	New types
261-340 (TRI 400-6)	262-725 (T2700D)
261-801 (TRI 400-8)	262-719 (T2850D)
262-220 (TRI 800-8)	262-731 (TRI 800-8)
261-968 (TRI 500-40)	262-703 (2N5446)

Absolute maximum ratings Note 1: V_{DRM} at T_j Max

	262-028	262-725	262-719	262-731	262-494
V_{DRM}[1]	±400V	±400V	±400V	±800V	±600V
$I_{T\,(RMS)}$	($T_A \leq 45°C$) 350mA	($T_C \leq 75°C$) 6A	($T_C = 80°C$) 8A	($T_C \leq 57°C$) 8A	($T_{mb} \leq 97°C$) 15A
I_{TSM}	($T_J \leq 125°C$) 6A	($T_C = 75°C$) 85A	($T_C = 80°C$) 85A	70A	($T_{mb} \leq 82°C$) 115A
$dI/_{dt}$	50A/µs	100A/µs	70A/µs	100A/µs	30A/µs
I_{GTM}	2A	4A	4A	2A	—
P_{GM}	1W	16W	16W	5W	5W
$P_{G(AV)}$	0.1W	0.2W	0.325W	0.5W	0.5W
T_{stg}	−40°C to +150°C	−65°C to +150°C	−65°C to +150°C	−40°C to +125°C	−40°C to +125°C
T_J	−40°C to +125°C	−65°C to +100°C	−65°C to +100°C	−40°C to +125°C	−40°C to +110°C

Electrical characteristics At T_C = 25°C unless otherwise stated

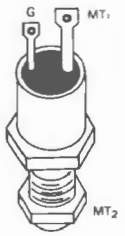
Stock No.	262-028	262-725	262-719	262-731	262-494	
	min. typ. max.	min. typ. max.	min. typ. max.	min. typ. max.	min. typ. max.	
V_{TM}	I_T = 1 Apk — 1.4 1.7	I_T = 30Apk — — 2 25	I_T = 30Apk — 1 7 2	I_T = 15Apk — — 1.55	I_T = 20 Apk — — 1.6	V
dV/dt	T_j = 125°C 20 — —	T_C = 100°C — 100 —	T_C = 100 C 75 250 —	T_J = 105 C 500 — —	T_j = 110 C — — 50	V/µS
dV/dt (COMM)	T_C = 65°C I_T = 0.6Apk 1.5 — —	T_C = 75 C — 10 —	T_C = 80 C 4 10 —	T_C = 85 C 5 — —	T_{mb} = 95 C — — 4	V/µS
I_H	— — 10	— — 30	15 30	— — 50	— — 30	mA
I_{DRM}	$T_C \leq 125°C$ — — 0.05	T_J = 100°C — — 4	T_J = 100 C — 0 1 2	T_J = 105 C — — 1.5	T_j = 85 C — — 0.5	mA
I_{GT}I+	— — 5	— — 25	— 10 25	— — 50	35 — —	mA
I−	— — 10	— — 40	— 20 60	— — 50	35 — —	mA
III+	— — 10	— — 40	— 30 60	— — 50	50 — —	mA
III−	— — 5	— — 25	— 15 25	— — 50	35 — —	mA
V_{GT}	— — 2	— — 2 2	— 1.25 2.5	— — 2.5	1.5 — —	V
θ_{jc}	100	— — 4	— — 3.1	— — 5	0.75	°C/W
Style	TO-92	TO-66	TO220 ISO-TAB	TO-220 ISO-TAB	TO-220 Tab —	

RS data

Absolute maximum ratings

Stock	261-558	262-242	262-703	262-545
V_{DRM}	($T_J \leq 100°C$) ±400V	($T_J \leq 100°C$) ±600V	($T_C \leq 100°C$) ±600V	($T_C \leq 100°C$) ±600V
$I_{T(RMS)}$	($T_C \leq 80°C$) 15A	($T_C \leq 80°C$) 15A	($T_C \leq 70°C$) 40A	($T_C \leq 60°C$) 30A
I_{TSM}	($T_C \leq 80°C$) 85A	($T_C \leq 80°C$) 85A	($T_C \leq 70°C$) 265A	($T_C \leq 100°C$) 265A
$dI/_{dt}$	150A/µs	150A/µs	100A/µs	100A/µs
I_{GTM}	4A	4A	12A	12A
P_{GM}	16W	16W	40W	40W
$P_{G(AV)}$	0.5W	0.5W	0.75W	0.75W
T_{stg}	−65°C to +150°C	−65°C to +125°C	−65°C to +150°C	−65°C to +150°C
T_J	−65°C to +100°C	−65°C to +100°C	−65°C to +110°C	−65°C to +100°C

OUTLINE

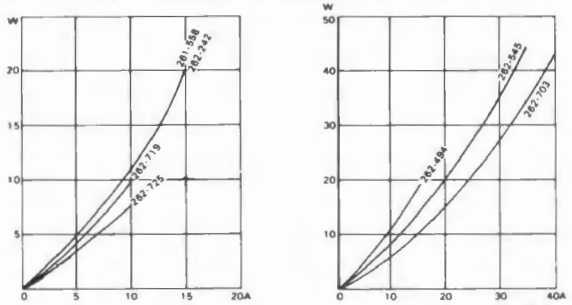


Stud 0 25-28UNF

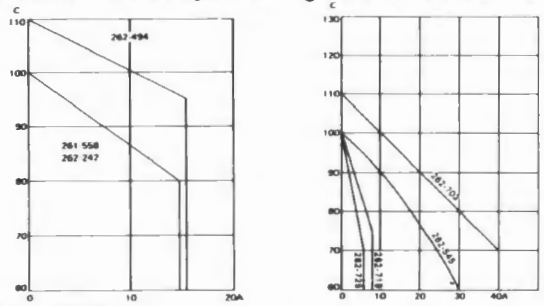
Electrical characteristics At T_C = 25°C unless otherwise stated

Stock No.	261-558			262-242			262-703			262-545			
	min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	
V_{TM}	I_T = 21 Apk	—	1.4	1.8	I_T = 21Apk	—	1.4	1.8	I_T = 56Apk	—	—	1.5	I_T = 100Apk	2.1	2.5	V
$dV/_{dt}$	T_C = 100°C	20	100	—	T_C = 100°C	—	75	—	T_C = 110°C	—	100	—	T_C = 100°C	150		V/µS
$dV/_{dt}$ (COMM)	T_C = 80°C	2	10	—	T_C = 80°C	—	10	—	T_C = 60°C	3	20	—	T_C = 60°C. $I_{T(RMS)}$ = 30A	3	20	V/µS
I_H		—	20	75		—	20	75	T_C = 25°C	—	—	60		25	60	mA
I_{DRM}	T_j=100°C	—	0.1	2		—	1.4	1.8	T_J = 100°C	—	—	4	T_j = 100°C	0.2	4	mA
I_{GT} I+		—	20	50		—	20	50		—	—	50		15	50	mA
I−		—	35	80		—	35	80		—	—	80		30	80	mA
III+		—	35	80		—	35	80		—	—	80		40	80	mA
III−		—	20	50		—	20	50		—	—	50		20	50	mA
V_{GT}		—	1	2.5		—	1	2.5		—	—	2.5		1.35	2.5	V
θ_{jc}			1				1					0.9		0.9		°C/W

Average power dissipation V_S RMS ON-state current



Maximum Case Temperature V_S RMS ON-state current



(conduction angle = **360°**)

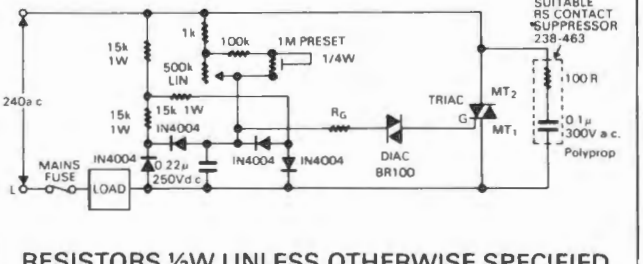
Application

A.C. Power control circuit using a triac

This circuit gives excellent power control from virtually zero to full power with hysteresis free characteristics. It is thus suitable for domestic lamp dimming and simple heater control. As it has no feedback characteristics it does not give good speed control on motors subject to varying load conditions.

Setting up procedure

With 500 kΩ linear potentiometer fully anti-clockwise (max. resistance) adjust 1 MΩ preset for min. load current.



RESISTORS ½W UNLESS OTHERWISE SPECIFIED

Ratings at Ta≤35°C				
Max Resistive/ Inductive load Current	Max. Lamp Load	Triac Type	Heatsink	R_G
25A	4000W	40A,600V (262-703)	1.1°C/W (401-807)	10Ω
13A	1000W	2N5574 (261-558)	2.1°C/W (401-403)	33Ω
8A	1000W	8A 400V (262-719)	4°C/W (401-497)	33Ω
6A	540W	6A 400V (262-725)	4°C/W (401-497)	47Ω

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RS data

Diacs and unijunctions transistors

A Diac is a silicon bi-directional trigger device for suitable firing triacs.
2N2646 unijunctions transistor is suitable for SCR/ triac firing, timer and oscillator circuits.

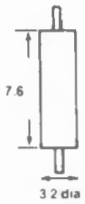
BRY 39 is a silicon planar pnpn device which may be used as a silicon controlled switch or as a programmable unijunction transistor.

Features

DIACS			Unijunction			
				2N2646 294–031	BRY 39 294–176	
	261–334	BRI00 261–930	V_{BB}	35V		
			I_E(pk)	2A	$V_D = V_R$	70V
V_{BD}	32V	32V	I_E	50mA	I_T	250mA
I_{pk}	1A	2A	η	0.56–0.75	I_{TSM}	3A
			P_{TOT}	300mW		

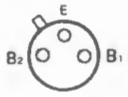
Mechanical details:

Diac symbol



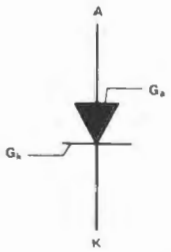
Unijunction symbol

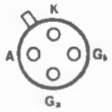
2N2646 Bottom view



Case size TO-18

BRY 39 Bottom view





(G_a connected to case) Case size TO-72

Absolute maximum ratings at T_{amb} = 25°C

Diacs		Unijunction			BRY 39	
	261–334			2N2646	$V_D = V_R$	*70V
P_{TOT} (T_{amb} = 40°C)	150mW	P_{TOT}		300mW	$V_{DRM} = V_{RRM}$	*70V
I_{pk} for 20μs (max) (T_{amb} = 25°C)	1A	V_{BB}		35V	$V_{DSM} = V_{RSM}$	*70V
		I_E		50mA	I_T T_{amb} = 25°C	175mA
					I_T T_{case} = 85°C	250mA
T_{stg}	(−40° to +150°C)	$I_{E(pk)}$	Firing cap ≤10μF V_{BB} ≤30V	2A	I_{TRM} t = 10μs,d = 0.01	2.5A
$T_{j\,max}$	100°C	V_{B_2}	− E	30V	I_{TSM} t = 10μs,T_j = 150°C	3A
					$dI_{T/dt}$	20A/μs
	261–930 BR 100	T_{stg}		−65° to +150°C	V_{GKM}	5V
		T_j		−65° to +125°C	I_{GKM}	100mA
P_{TOT} (T_{amb} = 40°C	150mW				V_{GaM}	70V
I_{pk} for 20μs (max) (T_{amb} = 25°C)	2A				I_{GaM}	100mA
T_{stg}	(−55°C to +125°C)				T_{stg}	−65° to +200°C
$T_{j\,max}$	100°C				T_j	+150°C

* These ratings apply for zero or negative bias on cathode gate w.r.t. cathode when $R_{GK} \leq 10K$

RS data

Electrical characteristics

Diacs				Unijunction					BRY 39		
	261–344					2N2646					
	min.	typ.	max.			min.	typ.	max.			
V_{BO}	28	32	36 V	η	V_{BB} = 10V	0.56	0.65	0.75		V_T	I_T = 100mA 1.4V (max.)
V_{BO} (symmetry)	–	–	3 V	r_{bb}	V_{BB} = 3V I_E = 0	4.7	7.0	9.1	kΩ	I_{RM}	V_{RM} = 70V *100nA (max.)
ΔV (at 10mA)	5	–	– V	I_p	V_{BB} = 25V	–	0.4	5	μA	I_{DM}	V_{DM} = 70V† 2μA (max.)
I_{BO}	–	300	— μA	I_V	V_{BB} = 20V R_{B2} = 100	4	6	–	mA	I_M	R_{GkK} = 10k R_{GaA} = 220k 250μA (max.)
	BR 100 261–930			I_{EB_2O}	$V_{B_2}E$ = 30V, I_{B_1} = 0	–	0.05	12	nA	V_{GKT}	V_D = 6V 0.5V (min.)
	min.	typ.	max.							I_{GKT}	V_D = 6V 1.0μA (min.)
V_{BO}	28	32	36 V	I_{B_2} (mod)	V_{BB} = 10V, I_E = 50mA	–	12	–	mA	V_{GaT}	V_D = 6V 1V (min.)
V_{BO} (symmetry)	–	–	3 V	V_{EB} (sat)	V_{BB} = 10V, I_E = 50mA	–	2	–	V	I_{GaT}	V_D = 6V R_{GK} = 10k 100μA (min.)
ΔV (at 10mA)	5	–	– V							t_{on}	V_D 15V I_T 150mA R_{GkK} = 10k 300nS (max.)
I_{BO}	–	—	100 μA	V_{OB_1}	see oscillator circuit	–	8	–	V	t_{off}	V_D = V_R = 15V I_T = 150mA R_{GaK} = 10kΩ 3μS (max.)

† T_j = 150°C * 1nA (typ.)

Fig 1: **Diac characteristics**

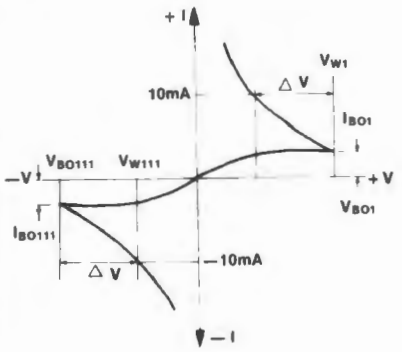
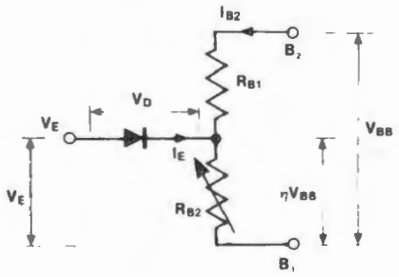


Fig 2: **2N2646 characteristics**

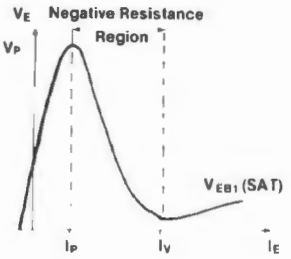


Simple equivalent circuit for unijunctions transistor

$V_P = V_{BB} + V_D$

V_D = 0.5V (approx.)

Fig 3: **Emitter base 1 characteristics**



Thermal characteristics

Diacs			2N2646	BRY 39	
	261–334	261–930 BR 100			
$R_{th\ (j-amb)}$	200°C/W	300°C/W	Derate P_{TOT} by 3mW°/C above 25°C	$R_{th\ (j-amb)}$	450°C/W
Derate P_{TOT} by 2.5mW/°C	2.5mW/°C above 40°C	5mW/°C above 70°C		$R_{th\ (j-case)}$	150°C/W

Applications

Fig 4: **2N2646 in relaxation oscillator circuit**

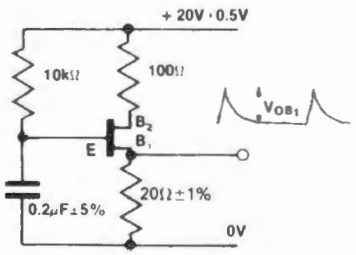
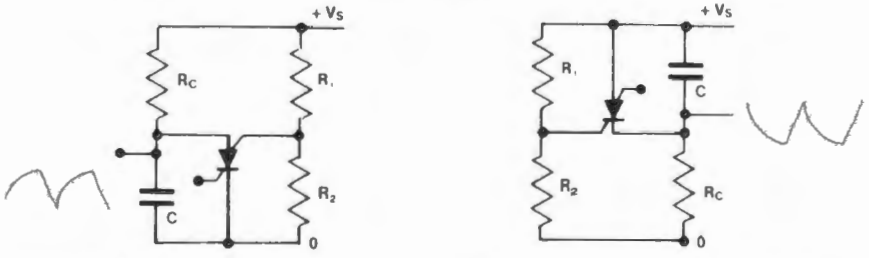


Fig 5: **BRY 39 in relaxation oscillator circuit in two modes:.**



Common cathode arrangement (i.e. used as a P.U.T.)

Common anode arrangement (i.e. used as a silicon controlled switch)

©RS Components Ltd. 1982

RS data

Count display i.c. ZN1040E

Stock number 306-285

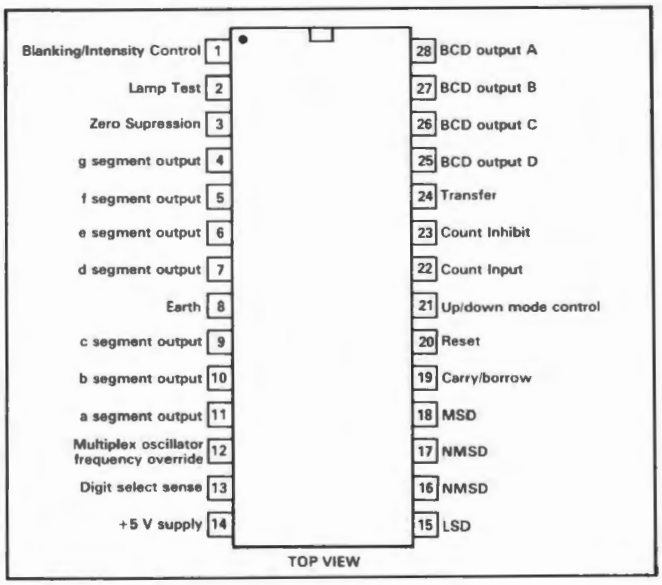
The ZN1040 is designed to satisfy the need for a universal count/display circuit suitable for the widest possible range of applications. The bipolar device allows fast count rates and high output currents to drive seven-segment LED displays, whilst BCD outputs allow interfacing to decoders for other types of display. Contained in a 28 dual-in-line package it requires a supply of 5 volts and consumes an internal current of 90mA typical.

Absolute maximum ratings

Supply voltage	5.5 Volts
Segment output currents	100mA
Other output currents	25mA
Operating temperature range	–20°C to 70°C
Storage temperature range	–55°C to 125°C

Features

- 4 decade synchronous up/down counter with memory
- Carry/borrow output for direct synchronous cascading
- BCD and seven-segment outputs
- Segment outputs can drive LED displays directly
- Schmitt trigger on count input for slow input waveforms
- Count inhibit gating
- Full 5V compatibility, both on supply and TTL compatible interface



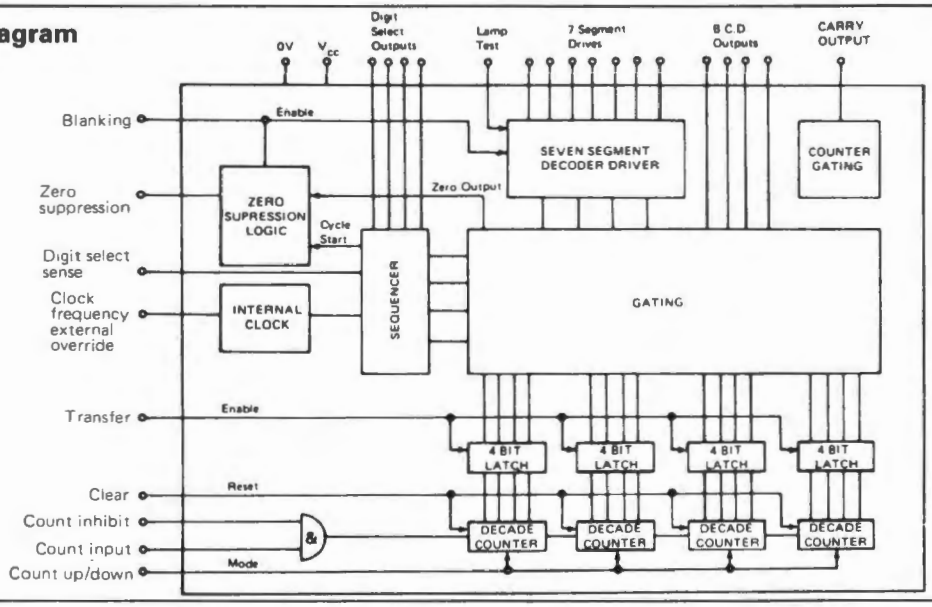
Electrical characteristics (at 25°C).

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Count input positive going threshold	V_T+	–	1.5	–	V	
Count input negative going threshold	V_T-	–	1	–	V	
Input logic 1	V_{IH}	2	–	–	V	
Input logic 0	V_{IL}	–	–	0.8	V	
High level input current	I_{IH}	–	–	20	μA	
Low level input current	I_{IL}	–	–	–600	μA	
Carry and BCD output logic 1		2.4	3.3	–	V	I_{Load} = 0.4mA
Digit select output logic 1	V_{OH}	2.4	3.3	–	V	I_{Load} = –0.4mA
Output logic 0 (except segments)		–	0.25	0.5	V	I_{Load} = 16mA
Segment output logic 0		–	0.3	0.6	V	I_{Load} = 50mA
Maximum count rate		5	8	–	MHz	
Transfer pulse width		50	–	–	ns	
Clear pulse width		100	–	–	ns	
Supply voltage	V_{CC}	4.75	–	5.25	V	
Supply current	I_s	–	90	–	mA	

Notes

1. Digit select outputs may be made to operate in either direction. If the digit select sense terminal is at logic 1, the digit select outputs go high to access and vice versa.
2. Inputs source 0.6mA maximum when at logic 0 and sink 20μA maximum when at logic 1.
3. The count input feeds into a Schmitt trigger possessing approximately 0.6 volt hysteresis. The inhibit control must not be altered while the count is at logic 1. The up/down control may, however, be altered asynchronously from count due to internal latching, but this only changes the mode when the count input is at logic 1.
4. When zero suppression (pin 3) is tied to ground the zero blanking function is disabled; i.e. zero's in MSD's will be displayed.
5. The clock terminal frequency is normally left open circuit, free running at about 500kHz. Alteration of the frequency is affected by adding an external capacitor between the clock frequency terminal and earth (pins 12 and 8). The rate may also be determined externally by overriding the internal clock with a TTL drive onto the clock frequency terminal.
6. Output logic 0 (not segments) is normally under 0.4V as for TTL and only rises when segments and other outputs are loaded with worst case conditions.
7. Unused inputs should be connected via a 1kΩ resistor to supply, in conformity with standard TTL practice.
8. A common anode LED display may show slight 'ghosting' due to the turn-off time of the PNP anode access transistors. This can be virtually eliminated by slowing down the scan rate with a suitable external capacitor from pin 12 to ground such as a 1000pF or 0.01μF.
9. The inhibit and count inputs must not be tied together when using more than four digits.

Figure 1 **System diagram**



Pinning details

Pin No.	Logic level to operate	Function	Pin No.	Logic level to operate	Function
1	0 to blank	Blanking/intensity control	15		*LSD – Digit select output
2	0	Lamp test	16		*NMSD – Digit select output
3	1	Zero suppression	17		
4	0	g segment output	18		
5	0	f segment output	19	1 when 9999 and up, or when 0000 and down and when count at 0	Carry/borrow
6	0	e segment output	20	'0' to reset	Reset
7	0	d segment output	21	1 'up' 0 'down'	Up/down mode control
8	N/A	Earth	22	0 to 1 transition	Count input
9	0	c segment output	23	'0' to inhibit	Count inhibit
10	0	b segment output	24	'0' to hold	Transfer
11	0	a segment output	25	TTL levels	BCD output D
12	TTL drive pulses	Multiplex oscillator frequency override	26	TTL levels	BCD output C
13	1 (+ve pulses) 0 (–ve pulses)	Digit select sense	27	TTL levels	BCD output B
14	N/A	+ 5 volts supply	28	TTL levels	BCD output A

*LSD – Least significant digit
NMSD – Next most significant digit

Operating notes

Section 1: Counter

Counter operation

The counter section of the ZN1040E is a synchronous four decade BCD counter. Each decade consists of four flip-flops which are clocked simultaneously on the positive going edge of the count input pulse. Suitable steering logic ensures that the 16 flip-flops count in a four decade BCD sequence. The BCD outputs of the counter are connected to data latches in which the count may be stored for subsequent decoding and display.

The counter and count control circuitry are shown in Figure 2 whilst the input and inhibit input circuits are shown in more detail in Figure 3.

Figure 2 **Count system functional diagram**

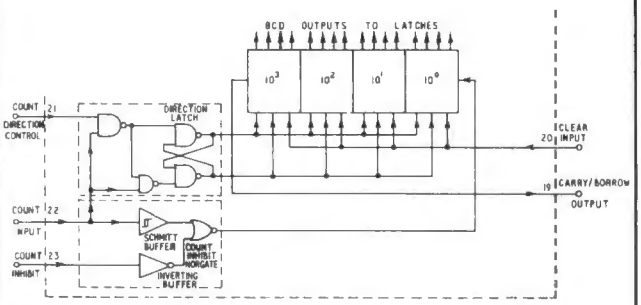
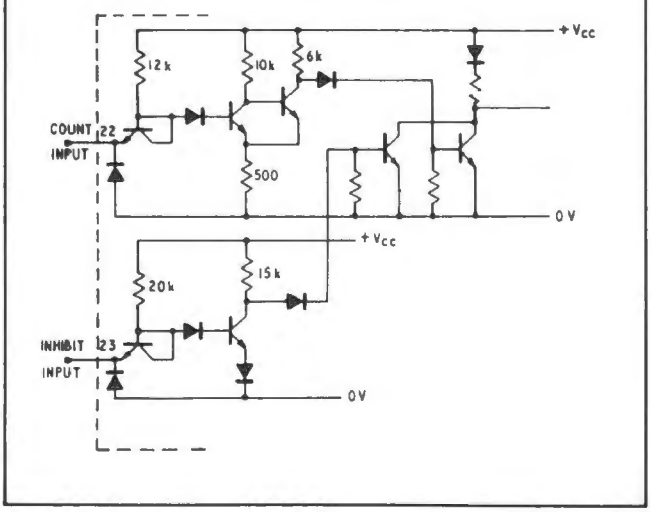


Figure 3 **Count input and inhibit circuit**

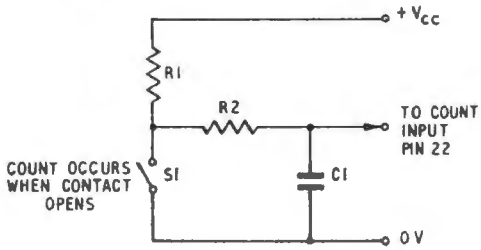


Counting occurs on the positive going edge of the count input pulse.

The counter input consists of a Schmitt trigger which allows the counter to operate reliably from input waveforms with very slow edges. It also allows a very simple anti-bounce circuit to be used when the count input is taken from a mechanical contact as shown in Figure 4.

Bounce occurs mainly on contact closure. R_2 is made very much smaller than R_1 so that when the contact closes C_1 discharges rapidly to below the lower threshold of the Schmitt trigger. However, if the contact subsequently opens due to bounce, the time constant $(R_1 + R_2)\,C_1$ is of sufficient length so that C_1 does not charge to the upper threshold of the Schmitt trigger. When the contact genuinely opens then C_1 will charge and the counter will be clocked. The values of R_1, R_2 and C_1 will depend on the contact characteristics and the maximum count rate.

Figure 4 **Anti bounce circuit**



Inhibit input

The inhibit input is used to gate the count input pulses. When the inhibit input is high then the second input of the inhibit NOR gate is low and count pulses are allowed through. However, when the inhibit input is taken low, the second input of the inhibit NOR gate is taken high. This holds the output low so that the count pulses are blocked. Correct timing of the inhibit control is important. If the inhibit control is taken low when the count input is low then an extra positive going edge will be fed through the inhibit NOR gate and an extra count will result as shown in Figure 5a. The inhibit input should thus be operated when the count input is already high as shown in Figure 5b. If the count input waveform has a duty cycle which is not 50% then it is advisable to arrange that it is normally high, as in Figure 5b, since this makes operation of the inhibit control simpler.

Figure 5a **Incorrect inhibit operation**

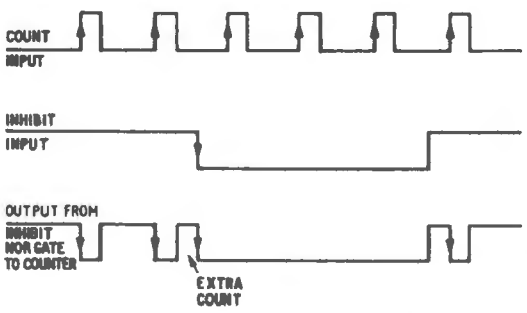
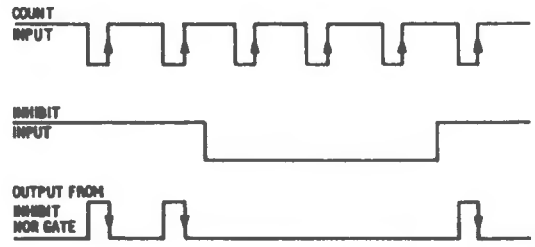


Figure 5b **Correct inhibit operation**



Direction control

Count direction is controlled by a 'D' latch (see counter operation) which can be set, for counting up, by taking the mode input high and reset, for counting down, by taking the mode input low. The clock input of this latch is connected to the count input and the state of the latch may therefore be changed only when the count input is high. If the count direction is to be reversed at a particular count then the state of the direction latch must be changed immediately that count is reached, whilst the count input is still high. Waiting until the count input has gone low again will result in the count direction not being reversed until the count input has gone high again, by which time an additional count will have been made in the original direction. Incorrect and correct operation of the direction control is illustrated in Figures 6a and 6b.

Figure 6a **Incorrect operation of direction control**

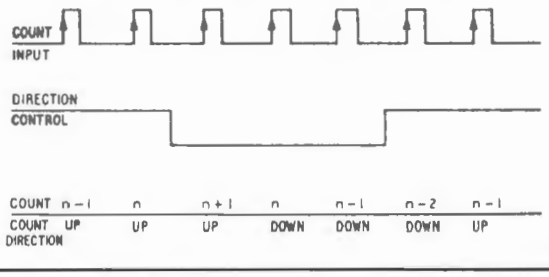
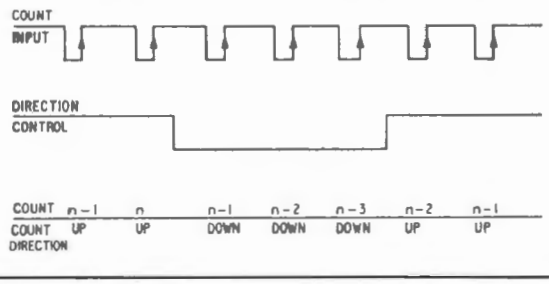


Figure 6b **Correct operation of direction control**



Counter reset

The counter may be reset to zero at any time by taking the clear input low. The counter will remain reset until the clear input is taken high again.

Care must be taken to set the direction latch to the correct state immediately after switch-on, otherwise the initial count may be made in the wrong direction. This may occur if the count input is low at switch-on since the direction latch may then set in either state. It is therefore advisable to ensure that the count input is normally high so that the direction latch will be set to the correct state at switch-on by the count direction control.

Carry/Borrow output

The carry/borrow output (pin 19) may be used as an overflow indicator or to facilitate direct cascading of ZN1040Es. When the count direction is UP then the carry output will go high on the next low-going edge of the count input after a count of 9999 is reached. The carry output will go low again on the next high-going edge at the count input, when the count changes to 0000.

When the ZN1040E is in the count DOWN mode then the carry output will go high on the next low-going edge at the count input after the counter reaches 0000. The carry output will go low again on the next high-going edge at the count input, when the count changes to 9999. In either case the carry output is subject to a propagation delay, t_c of typically 75ns, relative to the count input edges.

Carry output timing for both up and down counting is shown in Figures 7a and 7b.

Figure 7a **Carry output timing for up count**

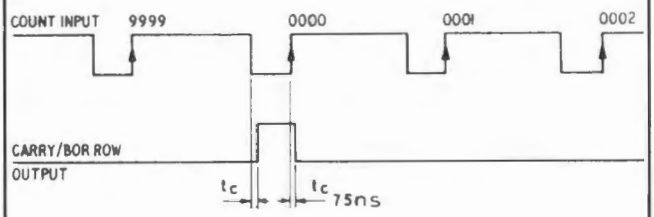
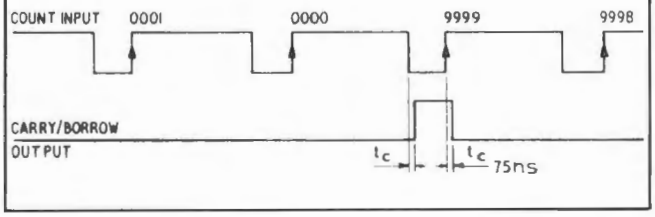


Figure 7b **Carry output timing for down count**



Count memory

Display latch

Each of the decade counters in the ZN1040E produces a binary coded decimal (BCD) number synchronous with the count input. The counter outputs are connected to the inputs of data latches which can store the counter outputs for subsequent display. Whilst the transfer input (pin 24) is high the latches are transparent, and their outputs will follow the data present at the inputs. When the transfer input is taken low the input data present at that instant will be held in the latches and will be unaffected by subsequent changes in the counter outputs.

Display multiplexing

Multiplex system

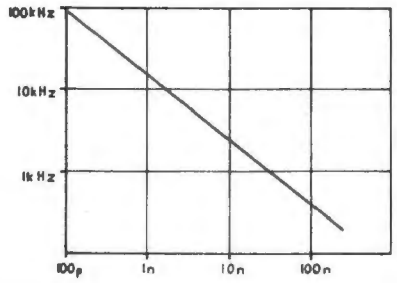
In order to economise on pin connections to the ZN1040E, and to simplify connection to displays the outputs of the ZN1040E are multiplexed, i.e. the four BCD output digits from the data latches are connected, one at a time, to a common data bus. The multiplexed BCD data is connected to four output pins directly and also via a BCD seven-segment decoder driver so that multiplexed seven-segment outputs are also available. Four digit select outputs indicate which digit is present on the BCD or 7-segment outputs at a particular time.

Internal multiplex oscillator

Clock pulses for the multiplex sequence are gener-

ated by an internal oscillator circuit. A capacitor of nominally 5pF is charged via a nominal 700k resistor to the upper threshold voltage of the Schmitt trigger. The nominal frequency of the multiplex oscillator is 500kHz but this can be altered by adding an external capacitor between pin 12 and ground (see Figure 8).

Figure 8 **Nominal MPX oscillator frequency v. external capacitance**



External MPX oscillator

Since the Schmitt trigger input of the MPX oscillator is only coupled to three fairly high impedances (10k and 700k resistors, and a 5pF capacitor) it is a simple matter to override the oscillator action by driving pin 12 from a low impedance external source such as a normal TTL output. Taking pin 12 high will hold the MPX oscillator output high, whilst taking pin 12 low will hold the output low. In this way the multiplexed BCD outputs of the ZN1040E can be synchronised to an external clock. This can be useful if, for example, the BCD output data is to be compared, digit by digit, with some preset limit. In this case the MPX frequency must at least be four times the input frequency to ensure that each digit has been compared before the next input pulse arrives.

The MPX input can be overdriven at frequencies up to 1 MHz which means that the BCD outputs can be compared at count frequencies up to 250 kHz.

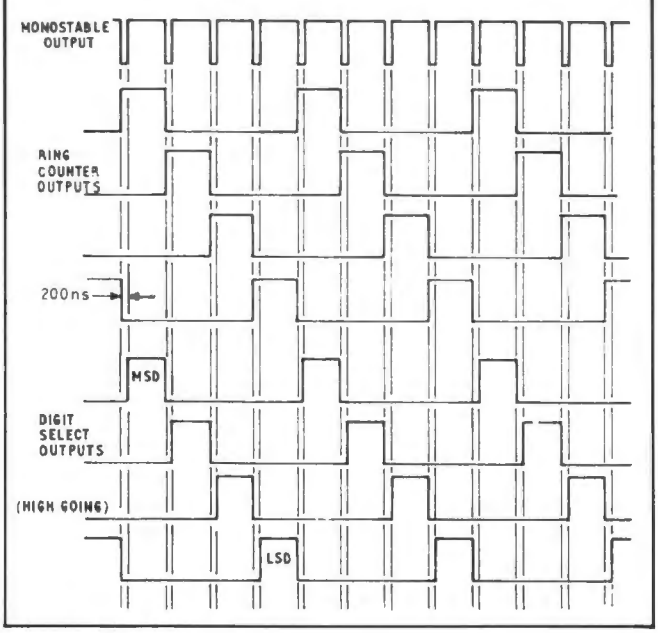
Multiplex sequence generation

The output of the MPX oscillator is connected to the clock input of a sequence generator which is essentially a four-stage ring counter. This produces a sequence of four output pulses which are used to gate the BCD outputs, in sequence, on to four output lines.

Digit select output circuit

Gating allows the selection of either high-going or low-going digit select pulses, thus allowing either common-anode or common-cathode displays to be driven using simple circuits. When the digit select sense input (pin 13) is high then the digit select pulses are high-going, when this input (pin 13) is low the digit select pulses are low-going. A timing diagram for high-going digit select pulses is given in Figure 9. For low-going pulses the digit select waveforms are simply inverted.

Figure 9 **Digit select output circuit**



Seven-segment outputs

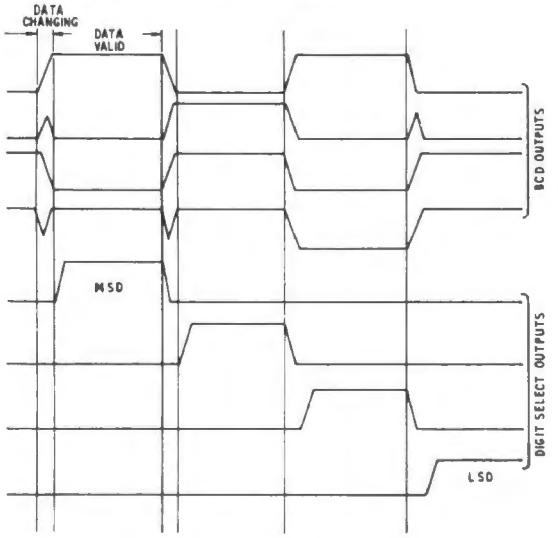
The seven segment outputs (pins 4-7, 9-11) are active low and can sink at least 50mA. The segment cathodes of common-anode displays may thus be driven directly.

BCD outputs

The BCD output for each digit appears on the BCD output lines synchronous with the appropriate digit select pulse. However, since the MPX sequence gating is driven directly from the ring counter outputs, there is no inter-digit gap between one set of BCD data and the next. During the transition between digits the BCD data must therefore be considered invalid. If the BCD data is to be utilised (e.g. stored in an external latch or compared) then the simplest way to overcome this problem is to make use of the leading edge of the digit select pulse to indicate when the data is valid. This is illustrated in Figure 10.

Similar comments also apply to the seven-segment outputs, but since these are normally used only for display driving, the problem does not usually arise.

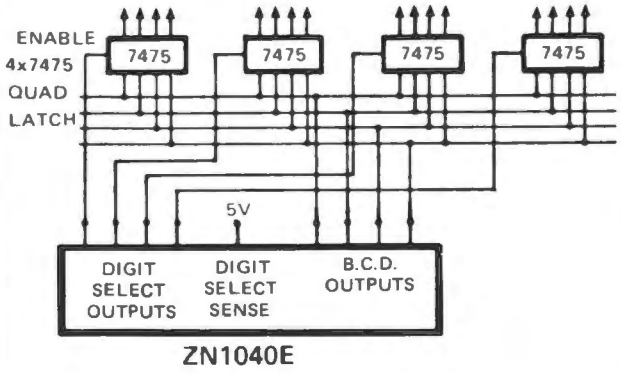
Figure 10 **BCD output timing**



Providing parallel BCD outputs

If outputs are required in parallel form rather than series parallel form the arrangement of Figure 11 may be used. A 7475 may be used as the digit select outputs are arranged to occur only while BCD outputs of the ZN1040E are stationary.

Figure 11 **ZN1040E providing parallel BCD outputs**



Zero suppression, blanking, decimal point and lamp test

The ZN1040E provides automatic blanking of leading zeros in the display, thus improving readability. A decimal point input is also provided which allows leading zeros to be displayed where these occur after the decimal point. A blanking input is provided to inhibit the display together with a lamp test input to check the operation of all display segments.

Blanking

Operation of the blanking input is extremely simple. When this input is high the seven-segment decoder functions normally and when this input is taken low the output of AND gate N6 goes low and the seven segment transistors are all turned off, blanking the display.

Zero blanking

Zero blanking operates on the principle of leaving the display blanked until non-zero data is detected at the outputs of the digit select gates. The trailing edge of the LSD output of the ring counter triggers a monostable which sets flip-flop N4/N5. The output of N4 holds one input of N6 low and the display is therefore blanked. It remains blanked until a non-zero digit appears on the BCD data bus, thus taking one or more of the inputs of NOR gate N3 high. The output of N3 then goes low resetting flip-flop N4/N5 so that the leading non-zero digit and all subsequent digits are displayed.

Should all four digits be zero then the flip-flop will be reset when the LSD output of the ring counter goes high and the output of N1 goes low. This ensures that the right hand digit (LSD) is always displayed, even if zero.

DP input

If not used, the decimal point input is normally held high. If a decimal point is used in the display then the DP input can be utilised to prevent the possibility of a blanked digit appearing after the decimal point. This is achieved by feeding a low-going pulse into the DP input synchronously with the digit select pulse for the digit where the decimal point is to appear. This resets flip-flops N4/N5 so that the display is unblanked for this digit and all subsequent digits even if there are leading zeros after the decimal point. Depending on whether the display has left or right-hand decimal points the display will be of the form .0 —— or 0.——. If there is to be a decimal point before the MSD then left-hand point displays must obviously be used. If no leading zero blanking is required then the DP input is simply grounded, when all digits will be displayed.

A timing diagram for the DP input is shown in Figure 9. It should be pointed out that the ZN1040E does not produce an output to drive the decimal point of a display, this must be done externally.

Lamp test

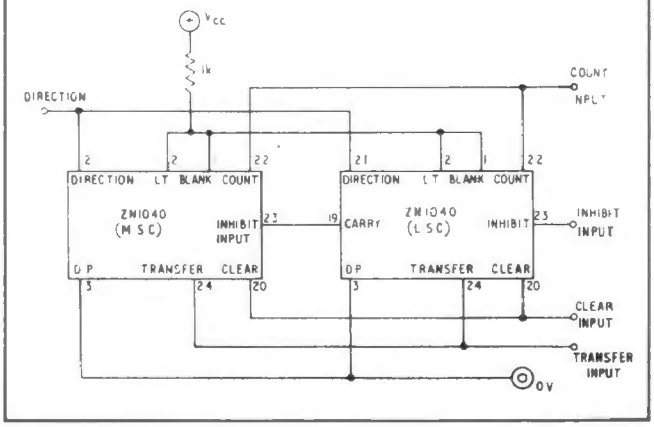
Operation of the lamp test function is quite simple. Taking the lamp test input low applies the BCD code 1000 (8) to the inputs of the BCD seven-segment decoder/driver. Simultaneously flip-flop N4/N5 is reset via N2 and N3, the output of N6 goes high, the display is unblanked and displays 8888. The blanking input must be high for lamp test to operate as a low blanking input will override the lamp test input and blank the display.

Applications information

Cascading the ZN1040E

If a count greater than 4 digits is required then two ZN1040Es may be cascaded using the carry/borrow output; or additional TTL decade counters may be added. To cascade two ZN1040s the carry/borrow output of the less significant counter is connected to the inhibit input of the more significant counter and the count inputs are linked as shown in Figure 12. The MSC is thus inhibited until after the 9999th clock pulse when the inhibit input will be taken high by the carry output of the LSC. On the leading edge of the 1000th clock pulse the MSC count will increase by 1 whilst the LSC count will go to zero. After the carry propagation delay the carry output of the LSC will go low and the MSC will again be inhibited. A timing diagram for this sequence of events is shown in Figure 13.

Figure 12 **Cascading ZN1040Es without leading zero blanking**



The leading zero blanking facility of the ZN1040E cannot be used directly in this application since the blanking circuits would operate independently for each device, leading to gaps in the display when the count was 999 or less, e.g.---- 0-456.

This problem can be overcome by grounding the DP inputs of both counters this inhibiting the zero blanking, or alternatively the DP input of the LSC may be grounded giving zero blanking only on the first three digits of the MSC.

When ZN1040Es are cascaded then separate display interfacing will be used for each set of four digits.

Figure 13 **Timing diagram for cascaded ZN1040Es**

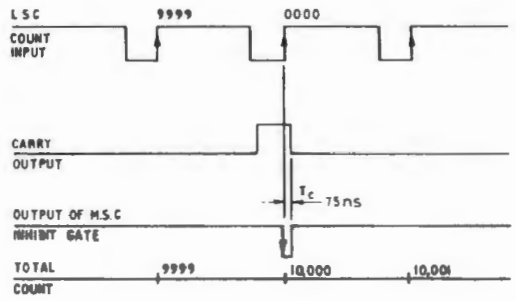
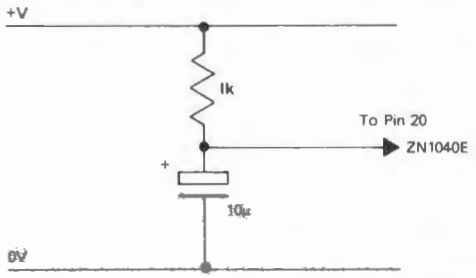


Figure 14 **Power on reset circuit if required**



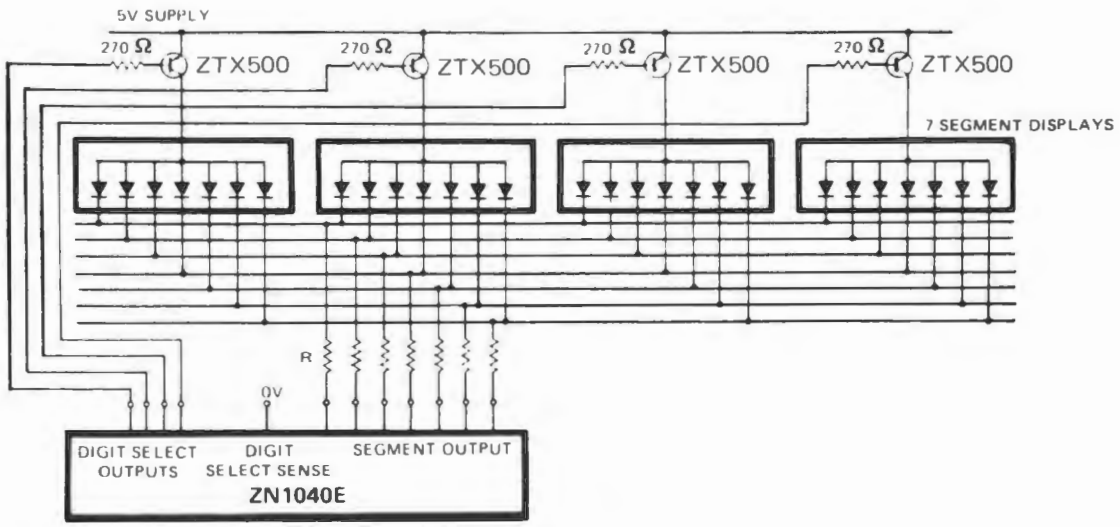
Display interfacing

The ZN1040E is versatile and able to drive virtually any display with minimal buffering. The detailed circuitry for popular types of display is described below. Good supply decoupling close to the IC is recommended, together with extra capacitance to slow down the scan rate to 10kHz or less. An internal 'pull up' resistor on the chip obviates the use of an external resistor when driving into displays requiring PNP transistors.

(a) Common anode LED displays

The circuit shown below, contains 4 low power PNP transistors and 11 resistors. As a guide, for 0.3in displays, Resistor 'R' should be approximately 100Ω.

Figure 15 **ZN1040E driving common anode LED displays**



(b) Common cathode LED displays

For common cathode use, 11 transistors and 18 resistors are required. The value of 'R' remains as shown in Figure 15.

Figure 16 **ZN1040E driving common cathode LED displays**

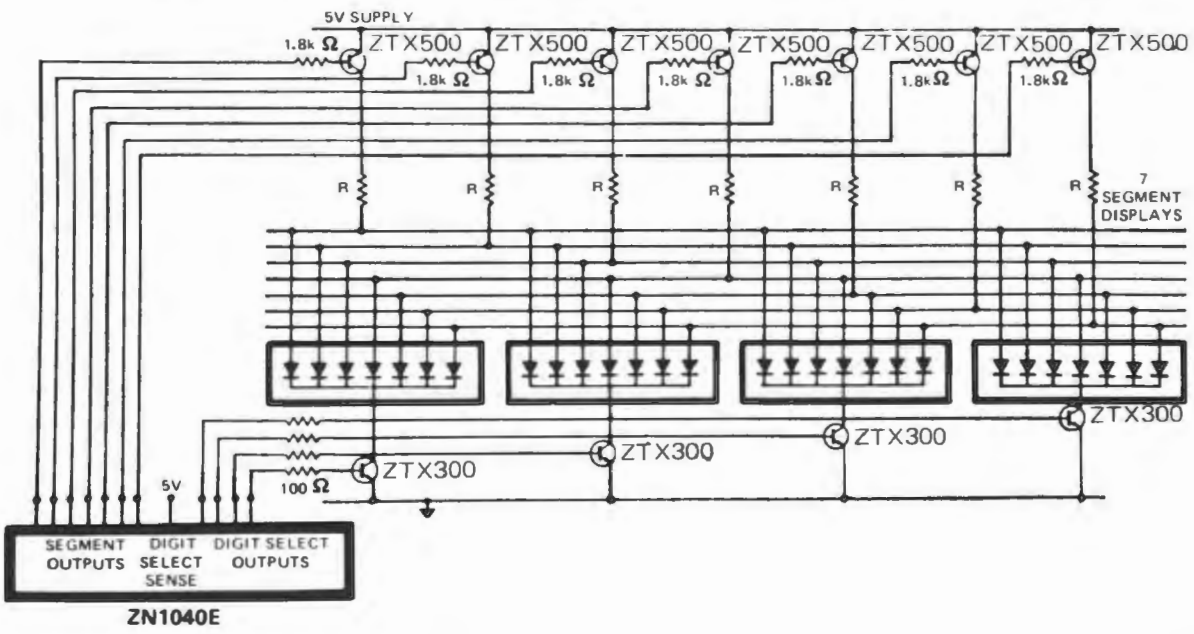
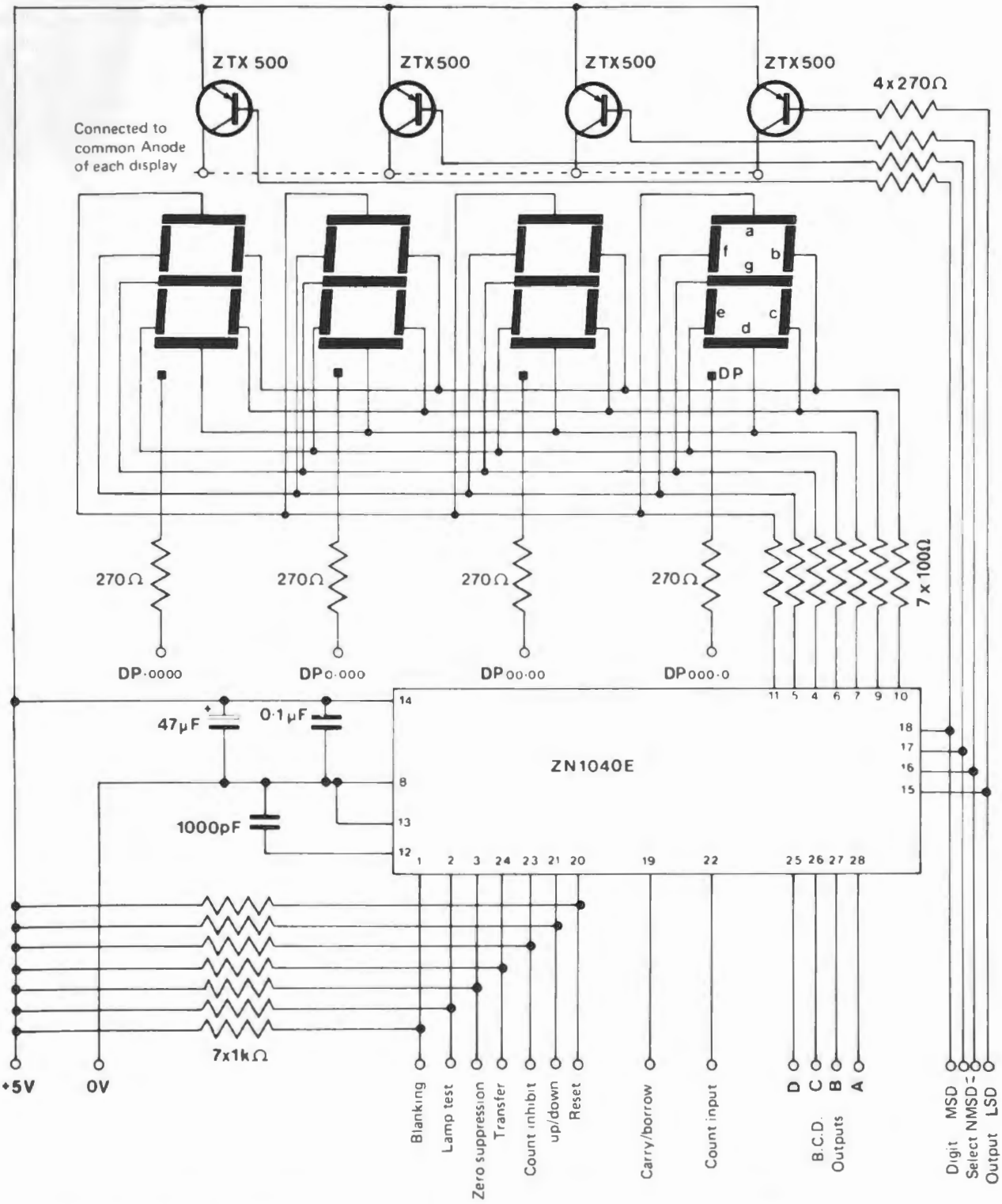


Figure 17 **Full circuit driving four common anode displays**



Printed circuit board 434-239 available.
Recommended components:
47µF 16v Tantalum 102-724
0.1µF 30v Disc ceramic 124-178
1000pF 100v Monolithic ceramic 125-676

All resistors 0.25W high stability carbon film.
7 segment display 0.3in 587-894 (Red) or 587-901 (Green).

RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

8 Bit D to A/A to D converter i.c.

The ZN425E is an 8 bit dual mode analogue to digital/digital to analogue converter. It contains an 8 bit D to A converter using an advance design of R-2R ladder network and an array of precision bipolar switches plus an 8 bit binary counter and a 2.5 volt precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8 bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

By including on the chip an 8 bit binary counter, analogue to digital conversion can be obtained simply by adding an external comparator (531) and clock inhibit gating (7400).

By simply clocking the counter the ZN425E can be used as a self-contained precision staircase ramp generator.

A logic input select switch is incorporated which determines whether the precision switches accept the outputs from the binary counter or external digital inputs depending upon whether the control signal is respectively high or low.

Features

- Dual mode, digital to analogue/analogue to digital.
- On-chip precision voltage reference.
- Includes 8 bit binary counter.
- Will function as precision staircase ramp generator.
- TTL and CMOS compatible.
- Direct voltage output.
- 16 pin D.I.L. package.

Pin connections (Top view)

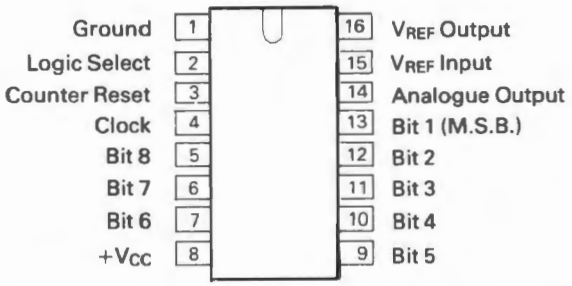
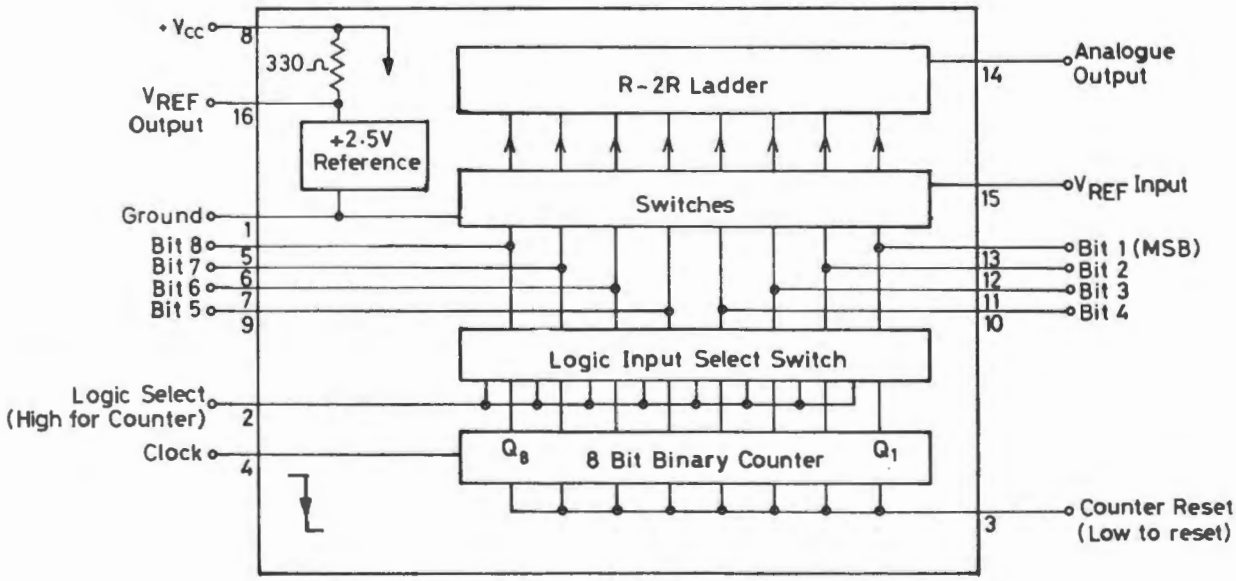


Figure 1: **Block diagram**



Absolute maximum ratings

Supply voltage V_{CC} ——— +7.0 volts
Max. voltage, logic and V_{REF} inputs ——— +5.5 volts

Operating temperature range ——— 0 to +70°C
Storage temperature range ——— −55 to +125°C

Characteristics At T_{amb} = 25°C and V_{CC} = +5 volts unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply voltage	V_{CC}		4.5	—	5.5	volts
Supply current	I_s		—	30	40	mA
High level input voltage	V_{IH}	See notes 1 and 2	2.0	—	—	volts
Low level input voltage	V_{IL}		—	—	0.7	volts
High level input current	I_{IH}	V_{CC} = max., V_I = 2.4V V_{CC} = max., V_I = 5.5V	— —	— —	10 100	μA μA
Low level input current	I_{IL}	V_{CC} = max., V_I = 0.3V	—	—	−0.68	mA
High level output current	I_{OH}		—	—	−40	μA
Low level output current	I_{OL}		—	—	1.6	mA
High level output voltage	V_{OH}	V_{CC} = min., Q = 1, I_{load} = −40μA	2.4	—	—	volts
Low level output voltage	V_{OL}	V_{CC} = min., Q = 0, I_{load} = 1.6 mA	—	—	0.4	volts

8 Bit D to A converter

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Lineraity error			—	—	±0.5	L.S.B.
Settling time		1 L.S.B. step	—	1.0	—	μs
Settling time to 0.5 L.S.B.		All bits ON to OFF or OFF to ON	—	2.0	—	μs
Offset voltage	V_{OS}	All bits OFF	—	3.0	—	mV
V_{OS} temperature coefficient			—	5	—	μV/°C
F.S.R. temperature coefficient		Ext. V_{REF} = 2.5V	—	3	—	ppm/°C
Linearity error temperature coefficient		Relative to F.S.R	—	7.5	—	ppm/°C
Analogue output resistance	R_o		—	10	—	k ohm
External reference voltage			0	—	3.0	volts

Internal voltage reference

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output voltage	V_{REF}	I = 7.5 mA (internal)	—	2.55	—	volts
Slope resistance	R_s	I = 7.5 mA (internal)	—	2	—	ohms
V_{REF} temperature coefficient		I = 7.5 mA (internal)	—	40	—	ppm/°C

Notes:

1. The logic select pin (2) must be held low when the bit pins (5, 6, 7, 9, 10, 11, 12 and 13) are driven externally.
2. To obtain counter outputs on bit pins the logic select pin (2) should be taken to +V_{CC} via a 1 kΩ resistor.
3. The internal reference requires a 0.22 μF stabilising capacitor between pins 1 and 16.

Applications

8 bit D to A converter

The ZN425E gives an analogue voltage output directly from pin 14 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature co-efficient of the Analogue Output Resistance R will be less than 0.004% per °C (or 1 L.S.B./100°C) if R is chosen to be ≥650kΩ.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig 2 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ.

The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{out} = 0.000V.

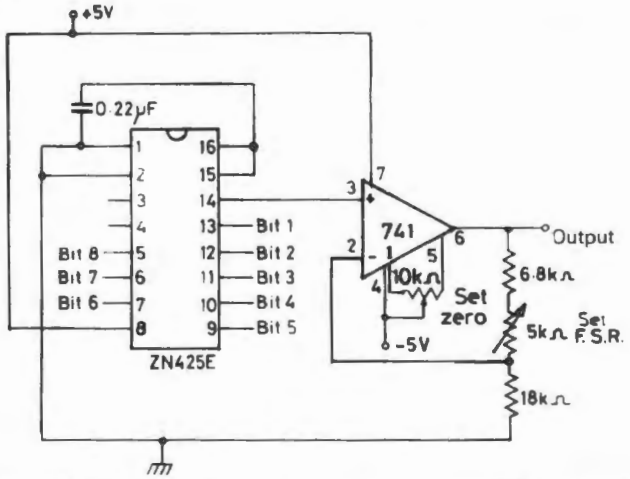
ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading −1 L.S.B.

iii. Repeat i. and ii.

e.g. Set F.S.R. to +3.840 volts −1 L.S.B.
= 3.825 volts

(1 L.S.B. = $\frac{3.84}{256}$ = 15.0 millivolts.)

Figure 2: **8 bit digital to analogue converter**



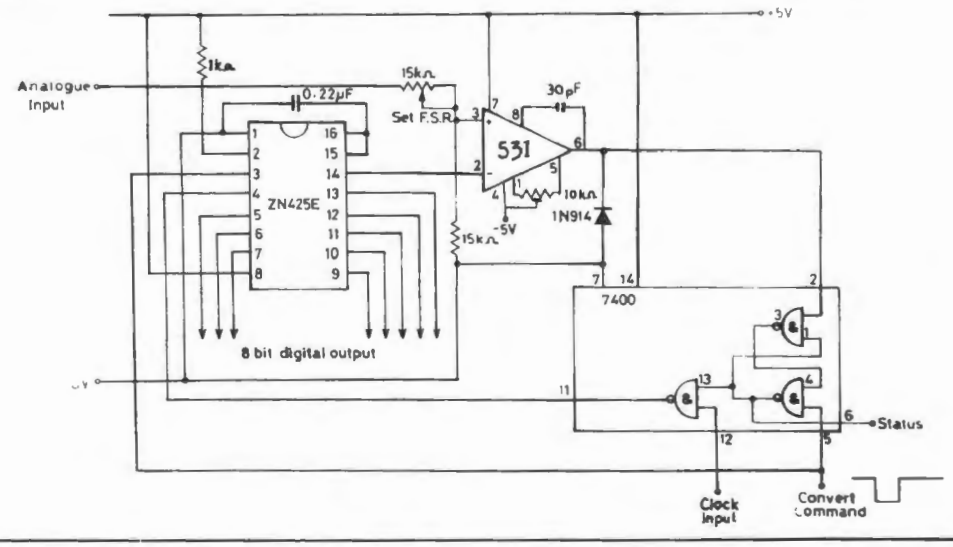
8 bit analogue to digital converter

A counter type analogue to digital converter can be constructed by adding a voltage comparator as in Fig 3. On the negative edge of the CONVERT COMMAND Pulse the counter is set to zero and the STATUS output to logical 1. On the positive edge the counter starts to count up from zero. The analogue output ramps until it equals the analogue voltage applied to the other input of the comparator. At this point, any further clock pulses are inhibited and STATUS goes low to indicate that the output data is valid.

The conversion time depends upon the value of the analogue input and for full scale reading is given by the clock frequency divided into the maximum number of counts.

For example if F_{clock} = 256K
conversion for (F.S.R.) = $\frac{2^8}{256{,}000}$ seconds
= 1 millisecond

Figure 3: **8 bit analogue to digital converter**

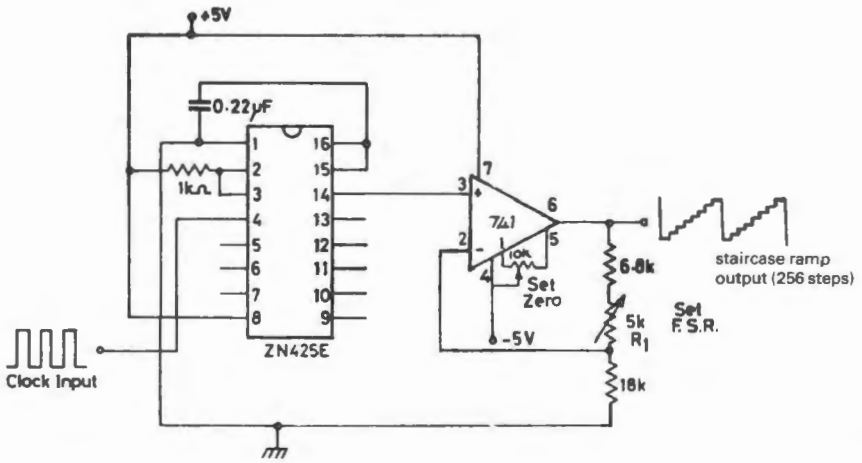


RS data

Precision staircase ramp generator

The inclusion of an 8 bit binary counter on the chip gives the ZN425E a useful staircase ramp generator function. The circuit, Fig 4 uses the same buffer stage as the D to A converter. The calibration procedure is also the same. Holding pin 2 low will set all bits to ON and if RESET is taken low with pin 2 high all the bits are turned to OFF. If the end voltages of the ramp are not required to be set accurately then the buffer stage could be omitted and the voltage ramp will appear directly at pin 14. (N.B. Resetting of the output may take place at any point of the waveform by taking pin 3 [reset] low.)

Figure 4: **Precision staircase ramp generator**



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RS data

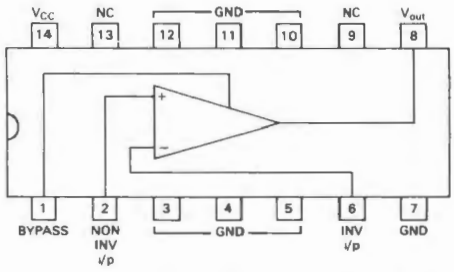
Audio power amplifiers

LM380	**Stock number 306-819**
TBA820M	**Stock number 302-491**
TDA2030	**Stock number 307-424**
TDA2004	**Stock number 309-543**

A range of audio power amplifiers with output powers from 2W to 9W. These versatile devices form the basic building blocks for constructing high quality amplifiers using a minimum of additional components.

LM380

An audio power amplifier with a fixed gain of 50 (34dB). The input stage allows inputs to be ground referenced or A.C. coupled as required and the output is automatically centred at one half of the supply voltage. The device is protected with both current limiting and thermal shutdown circuitry and is housed in a 14 pin D.I.L. package.



NOTE: Non-inv i/p is connected internally to GND via 150 kΩ resistor.

Maximum ratings

Supply voltage	22V
Peak current	1.3A
Package dissipation (internally limited)	10W
Input voltage	±0.5V
Max. junction temperature	150°C
Operating temperature range	0 to 70°C

Typical electrical characteristics

Fixed loop gain	50 (34dB)
Input sensitivity	150mV r.m.s.
Input resistance	150kΩ
Supply voltage range	8 to 22V max.
Bandwidth	100kHz
Quiescent current	7mA

Thermal data

Thermal resistance: in free air above 25°C	100°C/W
with 4 sq. in heatsink (p.c.b.)	50°C/W

Applications

Single ended output amplifier

A simple amplifier can be constructed using only a few external components (P_{out} = 2W V_{CC} = 20V) as shown in Figure 1. The input may be from crystal or ceramic pick-ups, cartridge or microphone, or may be from the LM381.

Bridge amplifier

For an increase in output, two amplifiers may be connected in the configuration shown below. This provides twice the voltage swing across the load for a given supply. A 15Ω load is necessary due to current limitations and therefore the overall output power is increased by a factor of two over the single amplifier.

Figure 1

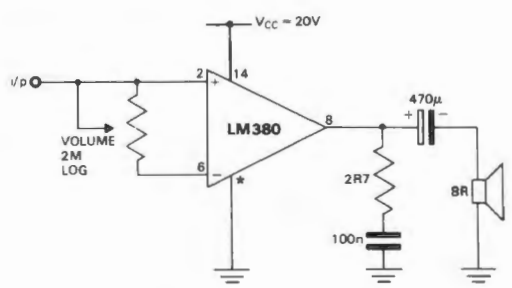
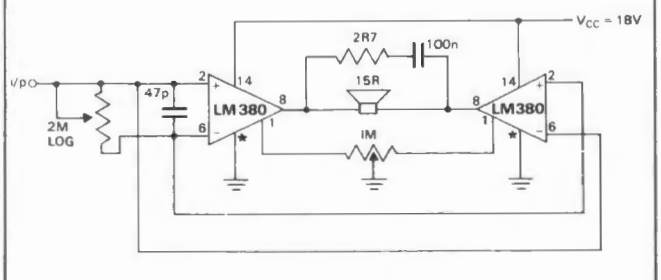


Figure 2

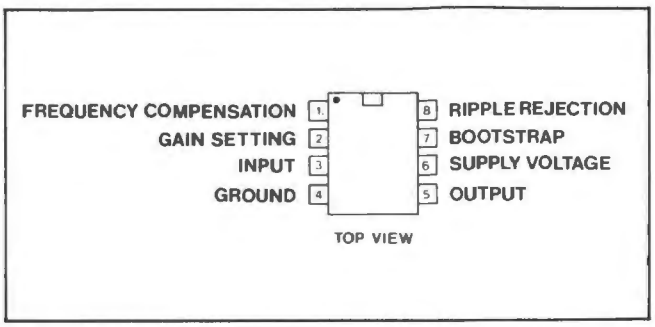


Notes

*Pins 3, 4, 5, and 10, 11, 12 (output ground and Pin 7 (input ground) should all be connected to supply ground. Two square inches of P.C.B. copper or metal strip connected to the central output ground pins of the I.C. will provide sufficient heatsinking to enable a 2 Watt output to be obtained at V_{CC} = 20V, Z_o = 8Ω.

TBA 820M

The RS TBA 820M is a monolithic integrated audio amplifier in an 8 pin dual-in-line plastic package. Featuring a wide supply voltage range of 3 to 16V, low quiescent current and good ripple rejection, this I.C. is ideally suited for use in battery powered equipment. Maximum output power is 2W into 8Ω at a supply voltage of 12V.



Absolute maximum ratings

Supply voltage	V_s	16V
Output peak current	I_o	1.5A
Power dissipation at $T_{amb} = 50°C$	P_{tot}	1W
Storage and junction temperature	T_{stg}, T_j	–40 to 150°C

Thermal data

Thermal resistance junction-ambient $R_{th\,j\text{-}amb}$ 100°C/W max.

Electrical characteristics $V_s = 9V$, $T_{amb} = 25°C$ unless otherwise specified.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply voltage	V_s			3		16	V
Quiescent output voltage (Pin 5)	V_o			4	4.5 (Vs/2)	5	V
Quiescent drain current	I_d				4	12	mA
Bias current (Pin 3)	I_b				0.1		μA
Output power	P_o	d = 10% $R_f = 120Ω$ $V_s = 12V$ $V_s = 9V$ $V_s = 9V$ $V_s = 6V$ $V_s = 3.5V$ $V_s = 3V$	f = 1kHz $R_L = 8Ω$ $R_L = 4Ω$ $R_L = 8Ω$ $R_L = 4Ω$ $R_L = 4Ω$ $R_L = 4Ω$	0.9	 2 1.6 1.2 0.75 0.25 0.20		 W W W W W W
Input sensitivity	$V_{i(rms)}$	$P_o = 1.2W$ $R_L = 8Ω$ f = 1kHz	$R_f = 33Ω$		16		mV
			$R_f = 120Ω$		60		
		$P_o = 50mW$ $R_L = 8Ω$ f = 1kHz	$R_f = 33Ω$		3.5		mV
			$R_f = 120Ω$		12		
Input resistance (Pin 3)	R_i	f = 1kHz			5		MΩ
Frequency response (–3dB)	B	$R_L = 8Ω$	$C_B = 680pF$	25 to 7,000			Hz
		$R_f = 120Ω$	$C_B = 220pF$	25 to 20,000			
Distortion	d	$P_o = 500mW$ $R_L = 8Ω$ f = 1kHz	$R_f = 33Ω$		0.8		%
			$R_f = 120Ω$		0.4		
Voltage gain (open loop)	G_v	f = 1kHz	$R_L = 8Ω$		75		dB
Voltage gain (closed loop)	G_v	$R_L = 8Ω$	$R_f = 33Ω$		45		dB
		f = 1kHz	$R_f = 120Ω$		34		
Input noise voltage (*)	e_N				3		μV
Input noise current (*)	I_N				0.4		nA
Signal to noise ratio (*)	$\frac{S+N}{N}$	$P_o = 1.2W$ $R_L = 8Ω$ $G_v = 34dB$	R1 = 10KΩ		80		dB
			R1 = 50kΩ		70		
Supply voltage rejection	SVR	$R_L = 8Ω$ $f_{(ripple)} = 100Hz$ $C6 = 47μF$ $R_f = 120Ω$			42		dB

(*) B = 22Hz to 22kHz.

Figure 3 **Output power vs. supply voltage**

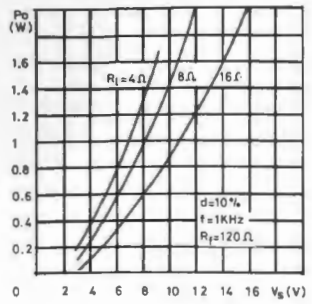


Figure 4 **Suggested value of C_B vs. R_f**

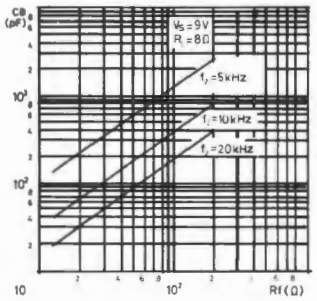


Figure 5 **Frequency response**

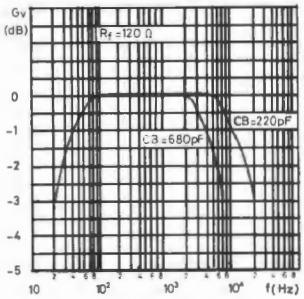


Figure 6 **Voltage gain (closed loop) vs R_F**

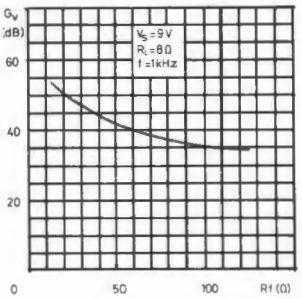
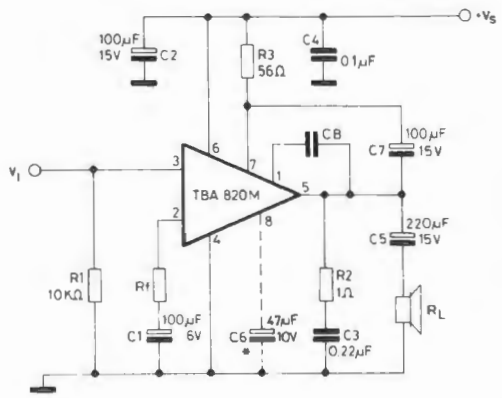
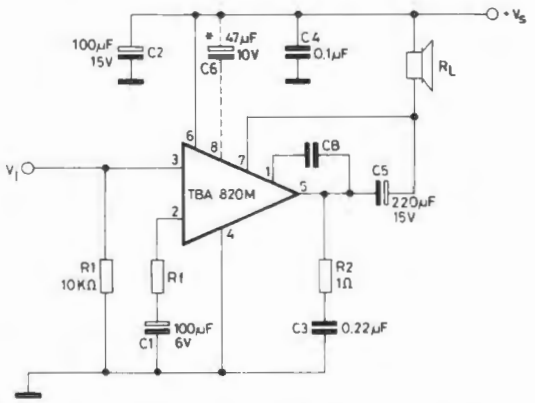


Figure 7 **Circuit diagram with load connected to ground**



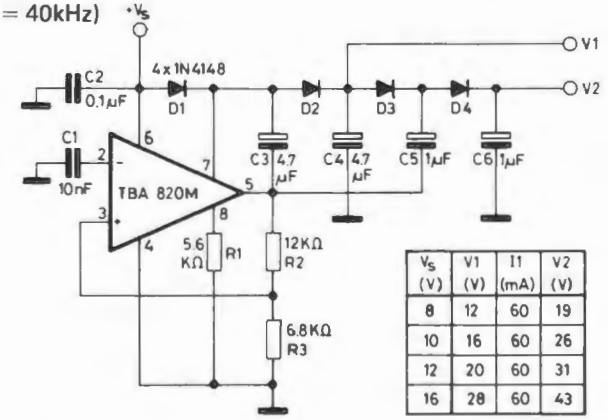
* Capacitor C6 must be used when high ripple rejection is required

Figure 8 **Circuit diagram with load connected to the supply voltage**



* Capacitor C6 must be used when high ripple rejection is required

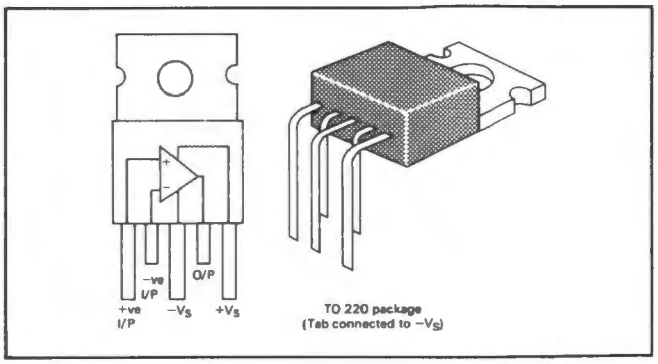
Figure 9 **1.5W D.C./D.C. converter (f = 40kHz)**



V_S (V)	V1 (V)	I1 (mA)	V2 (V)
8	12	60	19
10	16	60	26
12	20	60	31
16	28	60	43

2927
TDA 2030

The RS TDA 2030 is a high quality monolithic audio amplifer i.c. capable of producing an output power of up to 21W maximum into a 4Ω load. The device has a very low harmonic and crossover distortion. The THD is approx. 0.1% with output powers from 0.1 to 8W (8Ω load). The TDA 2030 features built in short circuit protection, thermal shut down and safe operating area protection.



Maximum ratings

Supply voltage V_S ——— ±18V
Input voltage V_{in} ——— V_S
Differential i/p voltage V_{diff} ——— ±15V
Output peak current (internally limited) ——— 3.5A
Power dissipation at T_{case} = 60°C P_D ——— 20W
Storage and junction temperature T_j ——— -40 to +150°C

Thermal data

Thermal resistance junction to case ——— 3°C/W max.

Electrical Characteristics T_{amb} = 25°C, V_S = ± 14V unless otherwise specified

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply voltage V_S		±6(+12)		±18(+ 36)	V
Input offset voltage V_{in} (offset)	V_S = ± 18V		± 2	± 20	mV
Quiescent drain current I_d	V_S = ± 18V		40	60	mA
Input bias current I_b	V_S = ± 18V		0.2	2	μA
Input offset current I_{in} (offset)	V_S = ± 18V		± 20	± 200	nA
Output power P_O	d = 13% V_S = 30V f = lkHz Z_O = 4Ω G_V = 30dB		17	21	W
Input resistance R_{in}	+ ve I/P	0.5	5		MΩ
Voltage gain G_V	Open Loop		90		dB
Input noise voltage e_n	BW (−3dB) = 22 Hz to 22k Hz		3	10	μV
Supply voltage rejection ratio	R_L = 4Ω Z_o = 4Ω G_V = 30 dB f_{ripple} = 100Hz	40	50		dB

Figures in brackets refer to operating limits

Figure 10 **Typical distortion vs output power**

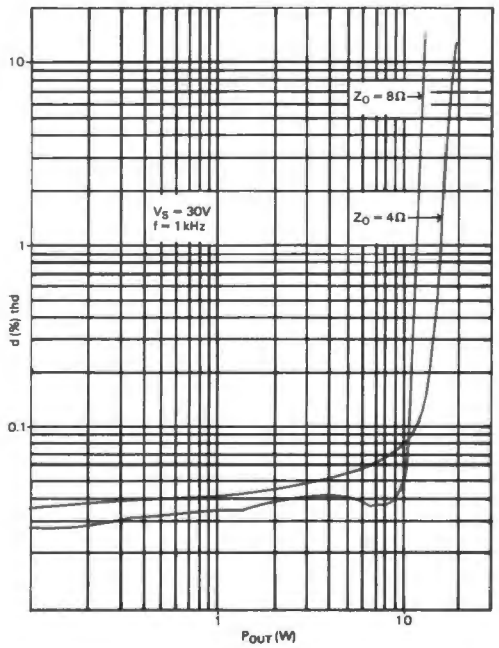
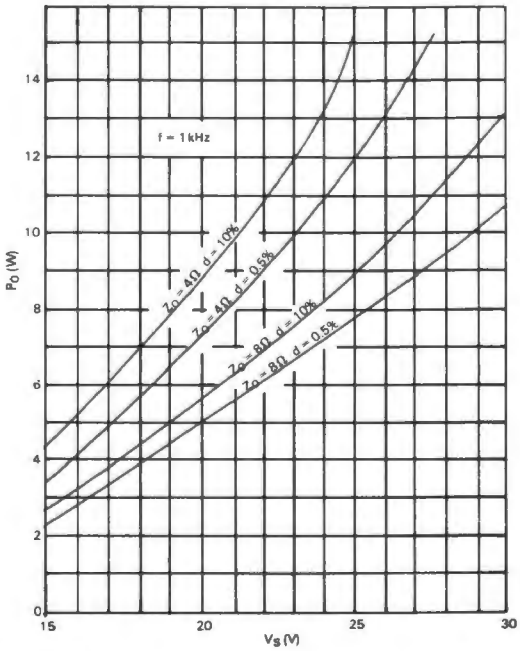


Figure 11 **Typical output power vs supply voltage**



Applications

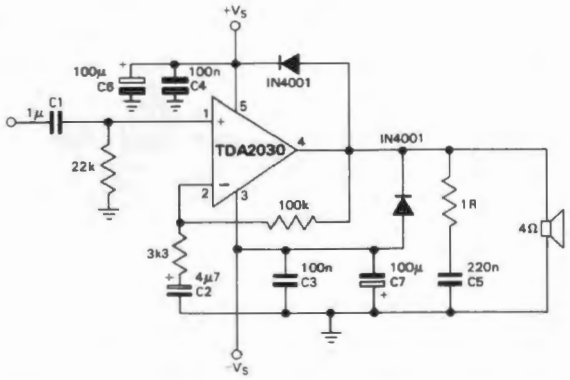
Power amplifier — dual supply rail

The circuit shown in Figure 12 will deliver up to 13W into a load impedance of 4Ω or 10W into a load impedance of 8Ω with distortion approx. 0.1%. A suitable preamplifier is the LM381. A printed circuit board is available Stock number 434-576. Suitable heatsink 401-497 (per stereo pair). Suitable power supply Figure 14.

Power amplifier — single supply rail

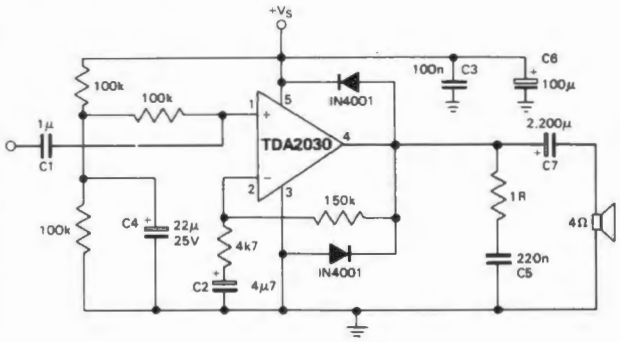
The circuit shown in Figure 13 gives a similar performance to the dual supply rail version. A suitable regulator for a power supply is the RS 317K (306-976) or High Power Regulator 308-152. The printed circuit board Stock number 434-576 will accommodate single or dual rail amplifier circuits.

Figure 12 **Dual supply rail amplifier**



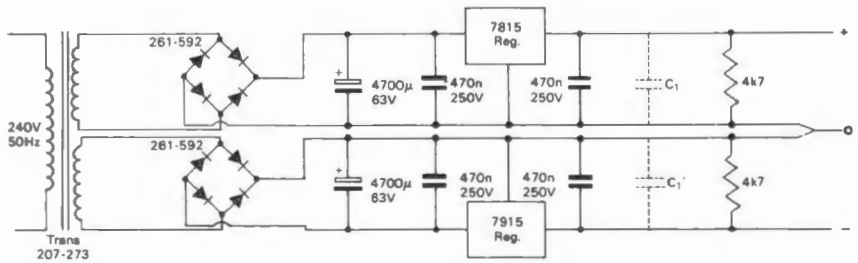
Decoupling capacitors C3, C4, C6 & C7 should be mounted as close as possible to the integrated circuit to minimise the effect of lead lengths.

Figure 13 **Single supply rail amplifier**



All resistors 0.5W
C7 is an off-board component.
Decoupling capacitors C3 and C6 should be mounted as close as possible to the integrated circuit to minimise the effect of lead lengths.

Figure 14 **Power supply for dual supply rail amplifier**

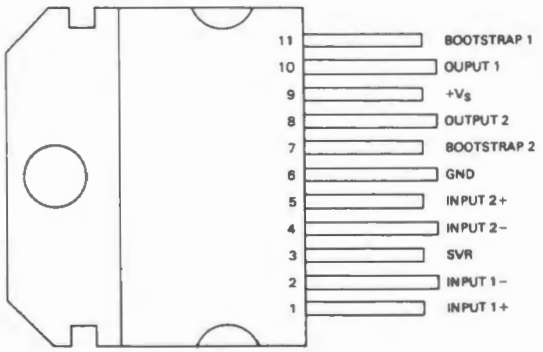


A power supply printed circuit board is available, Stock No. 434-289 (two boards required for dual supply). The 4700µF 63v capacitor 103-064 may be mounted using clip 543-383. C_1 and C_1' (100nF disc ceramic capacitors, Stock No. 124-178) may be added to improve stability. Suitable heatsink for both regulators 401-497 P.S.U leads should be kept short to prevent instability.

TDA 2004

The RS TDA 2004 is a Class B, dual, audio power amplifier in an 11 lead tab mounting plastic package. Each amplifier is capable of delivering up to 9W into a 4Ω load (17V supply, T.H.D. 10%). The two amplifiers may be operated as a stereo pair or connected in a bridge connection to increase power output to four times the power available in a single ended mode. Built-in short circuit protection, thermal shut down and safe operating area limiting are included to increase device reliability. A ready made p.c. board is available under Stock number 434-598 which can accommodate either the stereo amplifier circuit or bridge amplifier as shown in Figures 18 and 19 respectively.

Heatsink tab connected to GND (Pin 6)



Absolute maximum ratings

Supply voltage V_S ____ 18V
Peak supply voltage (for 50ms) ____ 40V
Output peak current (repetitive f≥10Hz) ____ 3.5A
Power dissipation at T_{case} = 90°C ____ 30W
Storage and junction temperature ____ −40 to +150°C
Output peak current (non repetitive t = 0.1ms) ____ 4.5A

Thermal data

Thermal resistance junction to case (θjc) ____ 3°C/W max.
Thermal shutdown case temperature ____ 135°C typ

Electrical Characteristics T_{amb} = 25°C, G_V = 50dB

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply voltage V_S		6		18	V
Quiescent output voltage V_O	V_S = 14.4V	6.6	7.2	7.8	V
	V_S = 13.2V	6.0	6.6	7.2	V
Quiescent drain current Id	V_S = 14.4V		50	120	mA
	V_S = 13.2V		50	120	mA
Output power (each channel) P_O	f = 1kHz T.H.D. = 10% V_S = 14.4V				
	R_L = 4Ω	6	6.5		W
	R_L = 3.2Ω	7.5	8		W
	R_L = 2Ω	9	10		W
	R_L = 1.6Ω	10	11		W
Distortion (each channel)	f = 1kHz V_S = 14.4V R_L = 4Ω				
	0.05W ≤ P_O ≤ 4W		0.2	1	%
Cross talk	V_S = 14.4V V_O = 4V r.m.s. R_L = ∞				
	f = 1kHz	50	60		dB
	f = 10kHz	40	45		dB
Input resistance	f = 1kHz + input	70	200		kΩ
	− input		10		kΩ
Voltage gain G_V	Open loop at 1kHz		90		dB
Bandwidth	R_L = 4Ω (−3dB)	35		15k	Hz
Input noise voltage	R_S = 10kΩ B.W. 25kHz		1.5	5	μV
Supply Voltage Rejection S.V.R.	f_{ripple} = 100Hz C = 10μF	35	45		dB

Figure 15 **Output power vs R_L**

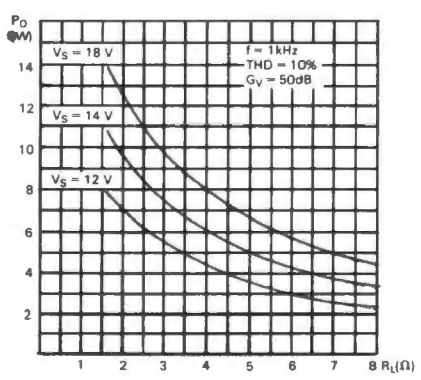


Figure 16 **Distortion vs output power**

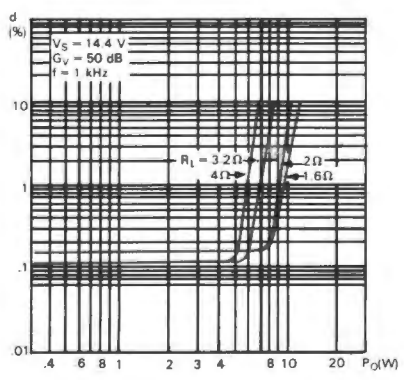
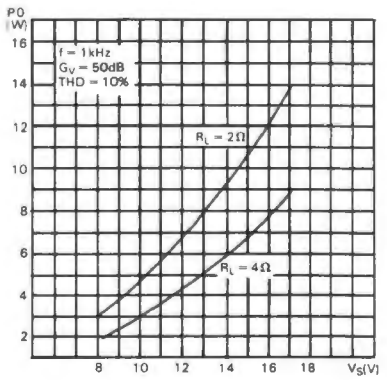
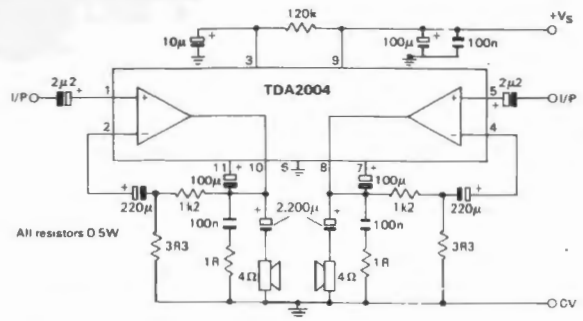


Figure 17 **Output power vs V_S**



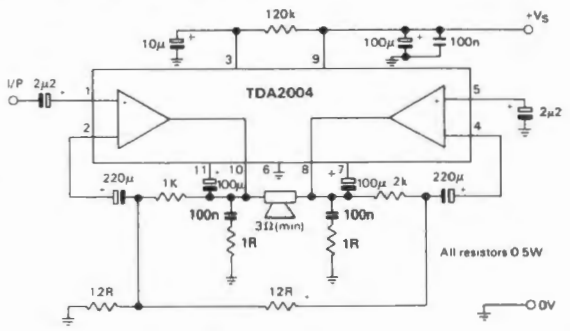
Applications (Ready made p.c.b. Stock number 434-598, is suitable for both stereo and bridge amplifiers.)

Figure 18 **Stereo Amplifier**



The above circuit is a stereo amplifier capable of delivering 4W/channel into 4Ω loads at a T.H.D. of 0.2% for a V_S of 15V and an output signal of 12mV r.m.s. The LM381 can be employed as a preamplifier. Suitable heatsink for the RS TDA2004 is available under Stock No. 401-497 (4° C/W). Decouple the power supply as close to the i.c. as possible.

Figure 19 **Bridge Amplifier**



The TDA 2004 can be connected as a bridge amplifier as shown above. This arrangement can produce four times the power output of a single ended design. In order to operate within maximum output current limits the minimum load impedance is limited to 3Ω. The maximum output power into a 3Ω load at 15V supply is approximately 20W. A suitable heatsink is available under Stock No. 401-497 (4° C/W). Decouple the power supply as close to the i.c. as possible.

TBA2004 Stereo amplifier parts list

Device type	Stock No.	Quantity
Semiconductor		
TDA 2004	309-543	1
Resistors		
3R3 thick film	145-620	2
1R thick film	145-563	2
1k 2 metal film	148-528	2
120k metal film	148-994	1
Capacitors		
2.2µF, 63V electrolytic	104-590	2
10µF, 25V electrolytic	103-553	1
220µF, 16V electrolytic	104-483	2
100µF, 16V electrolytic	104-477	2
100nF, disc ceramic	124-178	3
2200µF, 16V electrolytic	104-512	2
100µF, 25V electrolytic	103-581	1
Miscellaneous		
Printed circuit board	434-598	1
Loudspeaker, 4Ω	*	2
Heatsink 4°C/W	401-497	1
Heatsink compound	554-311	Tube
M3 x 12 Bolt, nut and washers	*	

*See current RS catalogue

TBA2004 Bridge amplifier parts list

Device type	Stock No.	Quantity
Semiconductor		
TDA 2004	309-543	1
Resistors		
120k metal film	148-994	1
1kO metal film	148-506	1
1R thick film	145-563	2
2kO metal film	148-578	1
12R metal film	148-039	2
Capacitors		
2.2µF, 63V electrolytic	104-590	2
10µF, 25V electrolytic	103-553	1
220µF, 16V electrolytic	104-483	2
100µF, 16V electrolytic	104-477	2
100nF, disc ceramic	124-178	3
100µF, 25V electrolytic	103-581	1
Miscellaneous		
Printed circuit board	434-598	1
Loudspeaker, 3Ωmin	*	1
Heatsink 4°C/W	401-497	1
Heatsink compound	554-311	Tube
M3 x 12 Bolt, nut and washers	*	

*See current RS catalogue

RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

C-MOS 4000B series pin connections

The 4000B series of C-MOS integrated circuits all feature buffered ('B' specification) outputs which improve both the output drive and switching speed capabilities.

C-MOS circuitry offers very low power consumption at low switching speeds together with high noise immunity typically 45% of supply voltage making them ideal for battery powered equipment.

All devices operate from a supply voltage between 3 to 18V d.c.

Guaranteed Logic input thresholds for C-MOS are:—

'High' Logic 1	0.7 V_{DD} to V_{DD}
'Low' Logic 0	V_{SS} to 0.3 V_{DD}

Tie unused inputs to V_{DD} or V_{SS} as necessary.

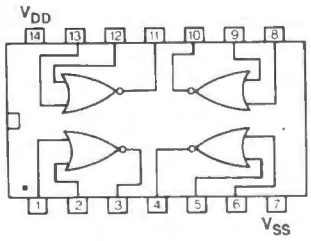
Connections shown are top view

A 'negation' circle at any output or input within the schematic indicates that the terminal is active low or at clocking inputs the device is negative edge triggered.

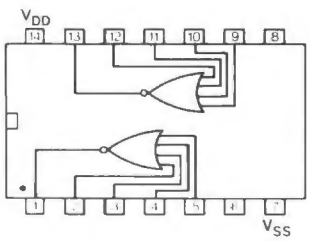
Abbreviations used through this data sheet

A,B,C,etc	Data Inputs	**R**	Reset
a,b,c,etc	Segment outputs (decoder / drivers)	**RBI**	Ripple blanking input
		RBO	Ripple blanking output
B.C.D.	Binary coded decimal	**S**	Preset
BI	Blanking input	**S1,2,etc**	Sum outputs
CE	Clock enable	**S_{in}**	Serial input of shift registers
CF	Cascade feedback		
CK	Clock input	**S_{out}**	Serial output of shift registers
CI	Carry input		
CY	Carry output	**SF**	Source follower output
D,JK	Data inputs to flip-flops	**ST**	Strobe
		T	Trigger
DIS	Disable tri-state output	**U/D**	Up Down mode Control '1'
EN	Enable	**VCO**	Voltage controlled oscillator
F	Function outputs		
INC	Increment	**VI**	Input to VCO
INH	Inhibit	**VO**	VCO output
LE	Latch enable	**V_{CC}**	+ Supply for buffers
LT	Lamp test	**V_{DD}**	+ Supply
MR	Master reset	**V_{EE}**	– Supply
OF	Overflow	**V_{SS}**	OV
PE	Preset Enable	**W**	User-selected + Ve or – Ve Logic
PH	Phase input for Liquid crystals		
P/S	Parallel — Serial Mode control	**WE**	Write enable
		X	Data inputs to selector
Q,$\overline{Q}$	Output and complement	⊓	Schmitt Device or function
QP	Phase Pulse Output		

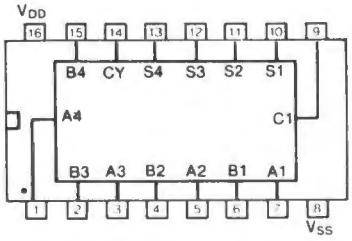
4001B Quad 2 input NOR



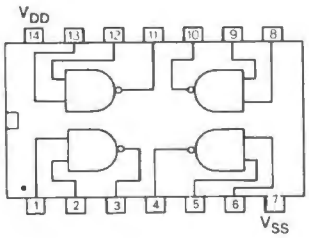
4002B Dual 4 input NOR



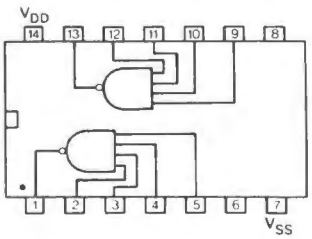
4008B 4 bit full adder



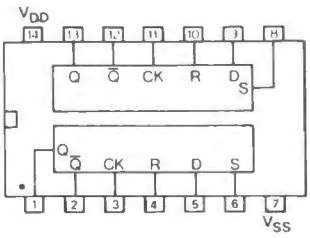
4011B Quad 2 input NAND



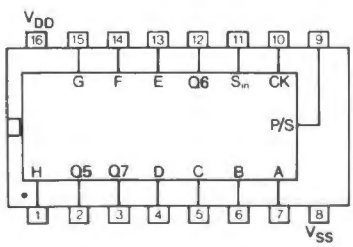
4012B Dual 4 input NAND



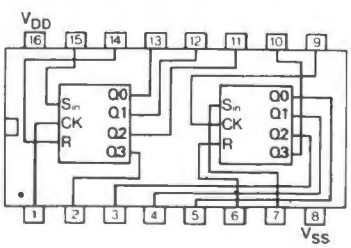
4013B Dual D-type flip-flop



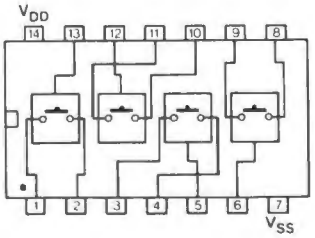
4014B 8 bit shift register



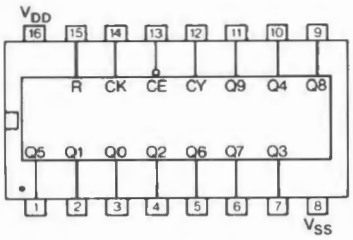
4015B Dual 4 bit shift register



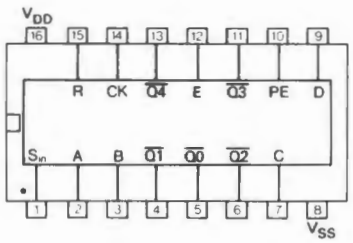
4016B Quad analogue switch



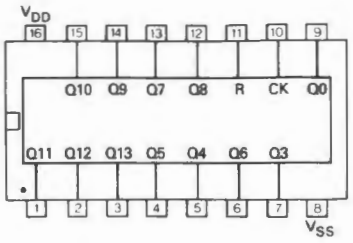
4017B Decade counter divider



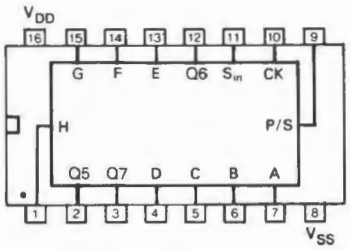
4018B ÷ by N counter



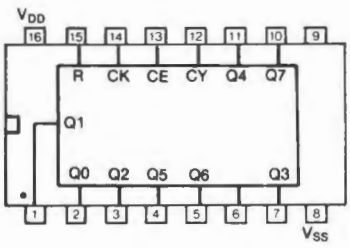
4020B 14 bit binary counter



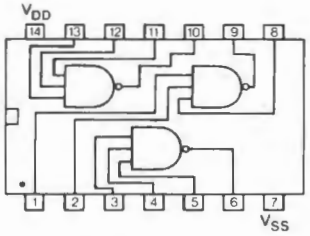
4021B 8 bit shift register



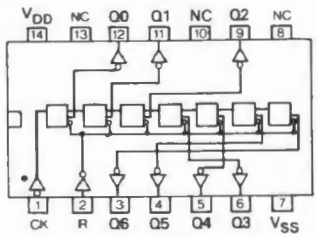
4022B Octal counter/divider



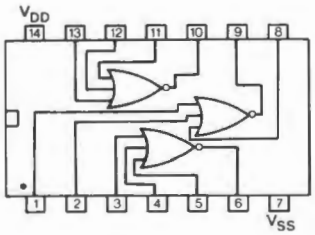
4023B Triple 3 input NAND



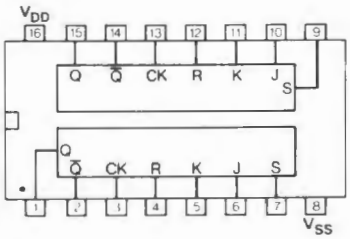
4024B Seven stage ripple counter



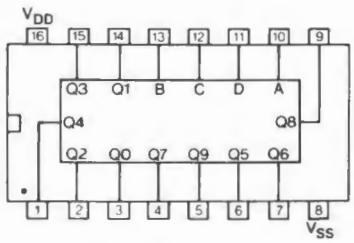
4025B Triple 3 input NOR



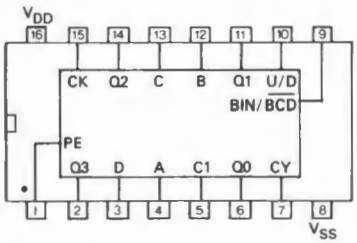
4027B Dual J.K. flip-flop



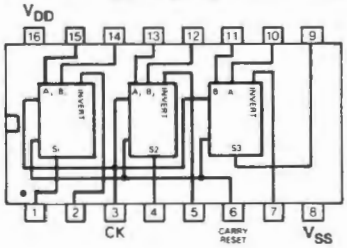
4028B BCD — decimal/binary-octal decoder



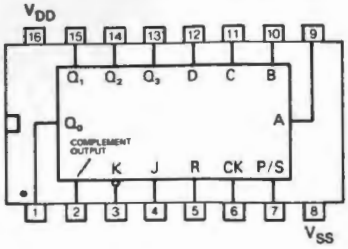
4029B Presettable binary/BCD up/down counter



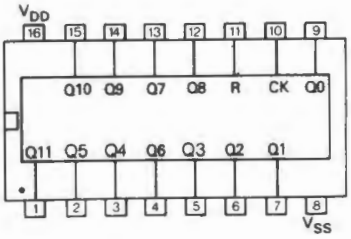
4032B Triple serial adder (carry is added on positive-going clock transition)
4038B Triple serial adder (carry is added on negative-going clock transition)



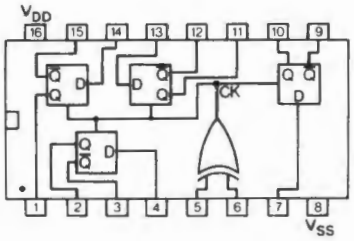
4035B 4 bit parallel — in/parallel — out shift register



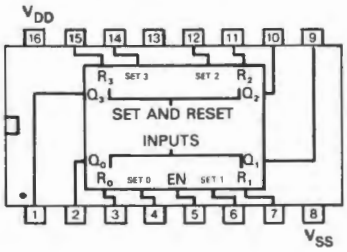
4040B 12 bit binary counter



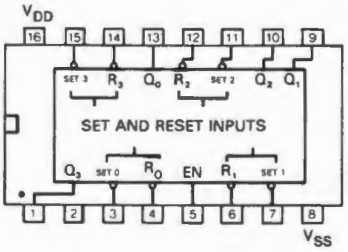
4042B Quad 'D' latch



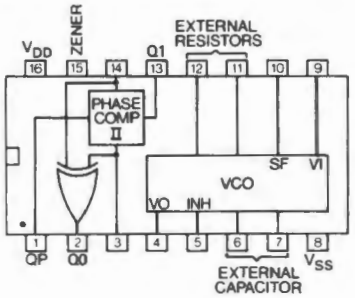
4043B Quad R/S latch with 3-state outputs "NOR"



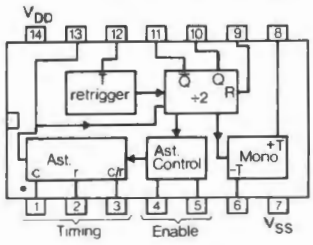
4044B Quad R/S latch with 3-state outputs "NAND"



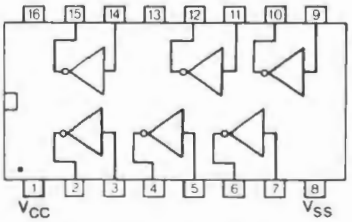
4046B Phase locked — loop



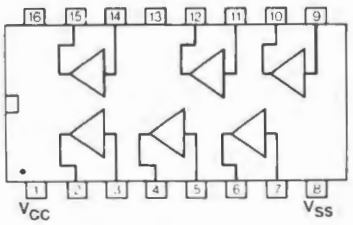
4047B Monostable/Astable multivibrator



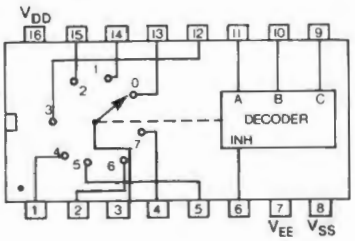
4049UB Hex inverter — buffer



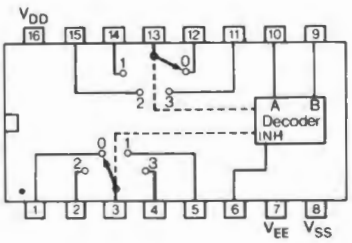
4050B Hex buffer



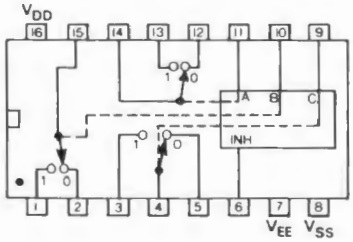
4051B 8 input analogue multiplexer



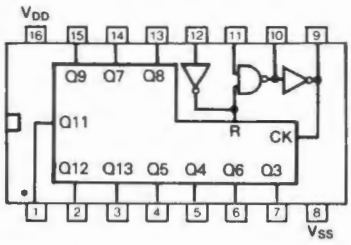
4052B Dual 4 input analogue multiplexer



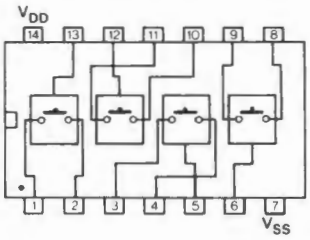
4053B Triple 2 input analogue multiplexer



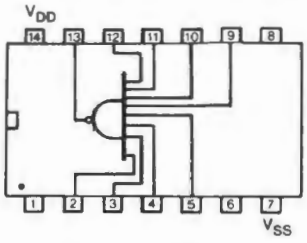
4060B 14 bit binary counter



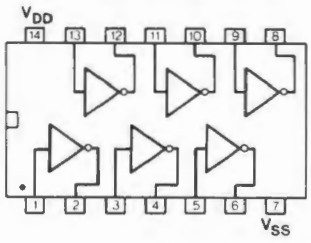
4066B Quad analogue switch



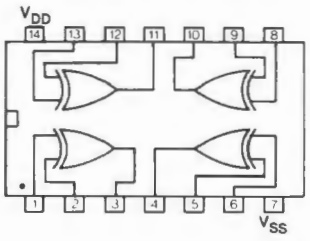
4068B 8-input NAND gate



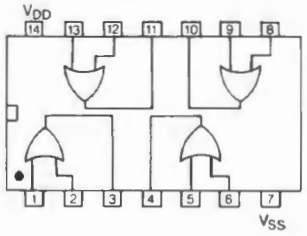
4069UB Hex inverter



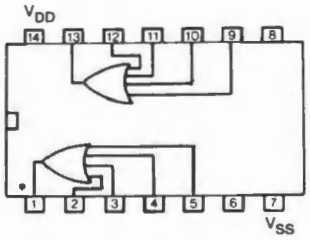
4070B Quad exclusive OR



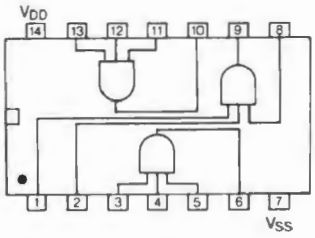
4071B Quad 2 input OR



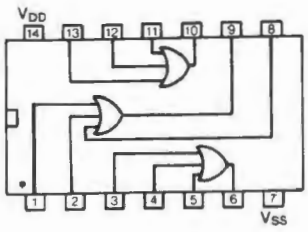
4072B Dual 4-input OR gate



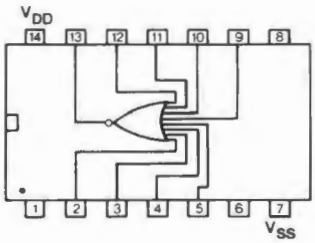
4073B Triple 3 input AND



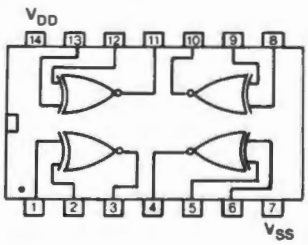
4075B Triple 3 input OR



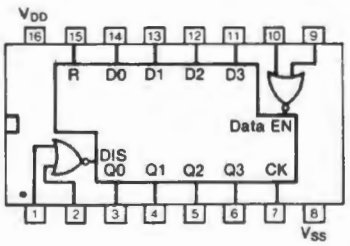
4078B 8 input NOR



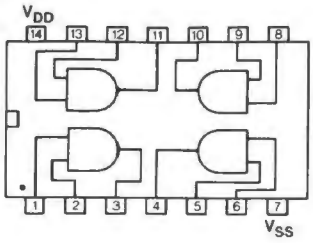
4077B Quad 2 input Exclusive "NOR" gate



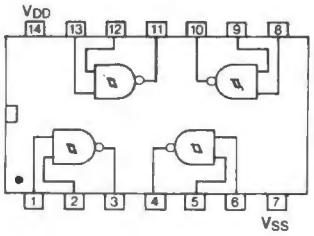
4076B Quad D type register



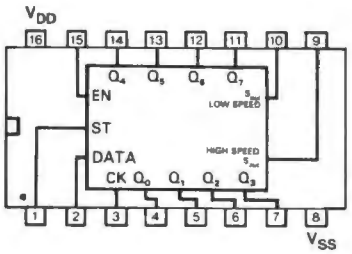
4081B Quad 2 input AND



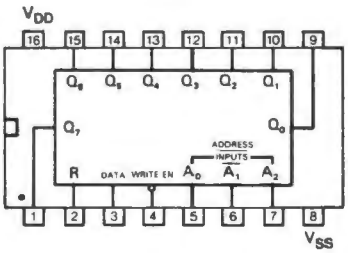
4093B Quad 2 input NAND schmitt



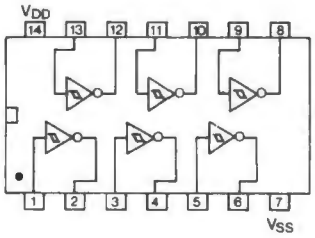
4094B 8-stage shift/store register with three-state outputs



4099B 8 bit addressable latch



40106B Hex inverting schmitt

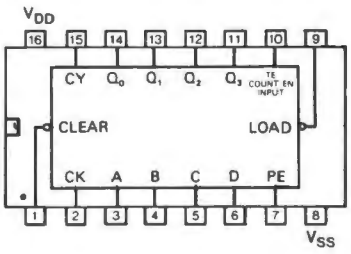


4160B Synchronous programmable 4 bit decade counter with asynchronous clear

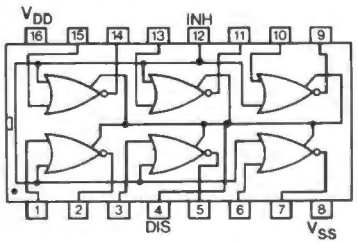
4161B Synchronous programmable 4 bit binary counter with asynchronous clear

4162B Synchronous programmable 4 bit decade counter with synchronous clear

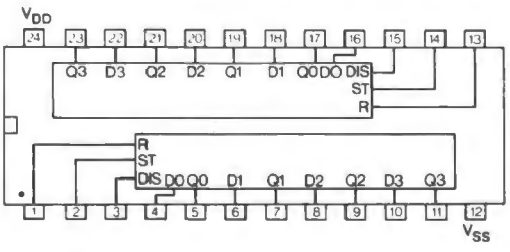
4163B Synchronous programmable 4 bit binary counter with synchronous clear



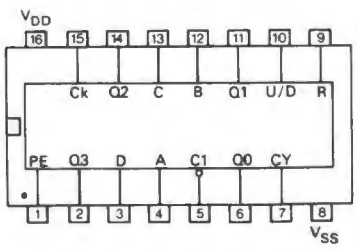
4502B Strobed Hex inverter/buffer



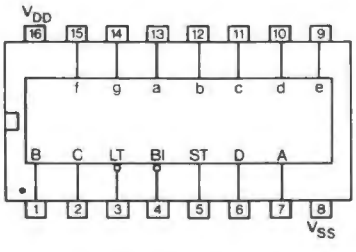
4508B Dual 4 Bit latch with tri-state outputs



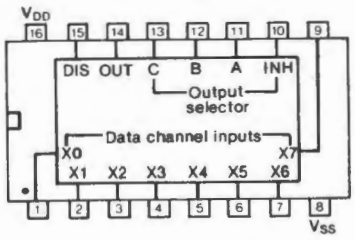
4510B BCD up/down counter



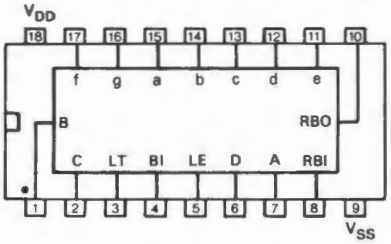
4511B BCD - 7 segment latch/ decoder/driver



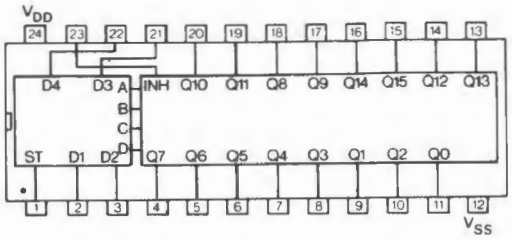
4512B 8 channel data selector



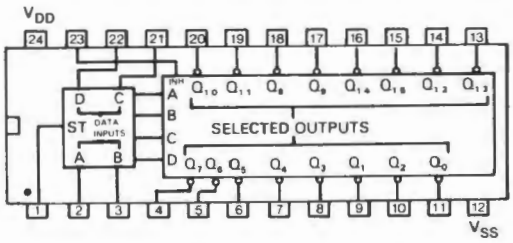
4513B BCD to seven segment latch/ decoder/driver



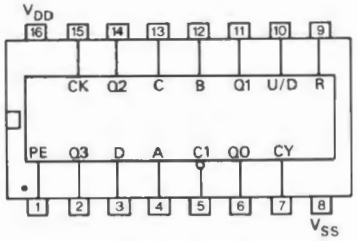
4514B 4 Bit latch to 1 of 16 decoder



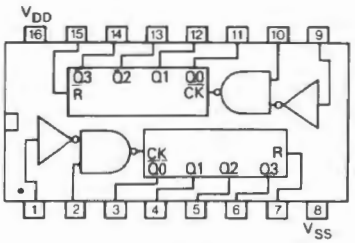
4515B 4 bit latch/4 to 16 line decoder



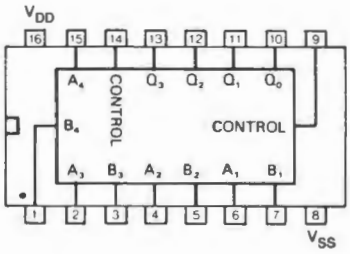
4516B Binary up/down counter



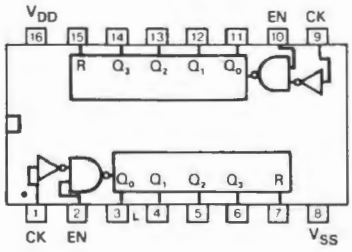
4518B Dual BCD up-counter



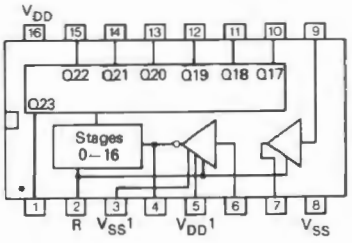
4519B Quad 2 input multiplexer



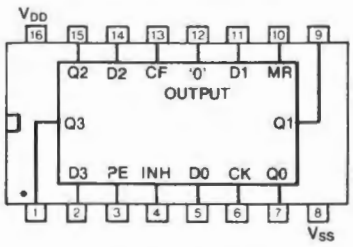
4520B Dual 4 bit binary counter



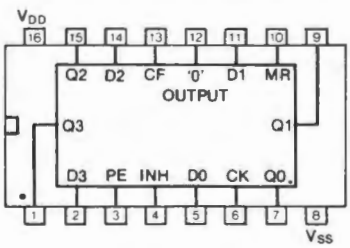
4521B 24 stage frequency divider



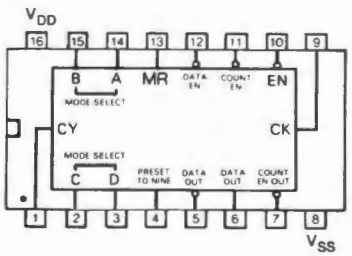
4522B BCD — programmable divide by N



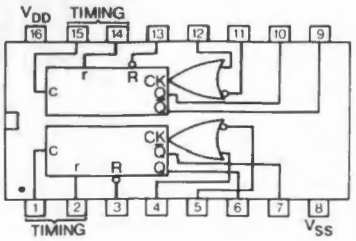
4526B Binary programmable divide by N



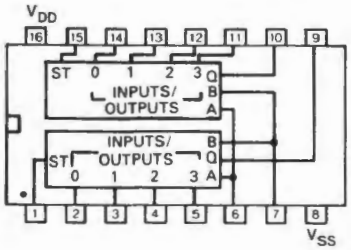
4527B BCD Rate multiplier



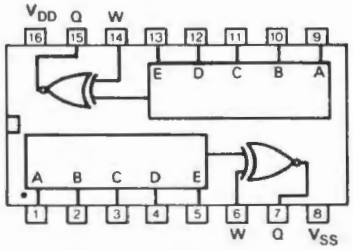
4528B Dual resettable monostable



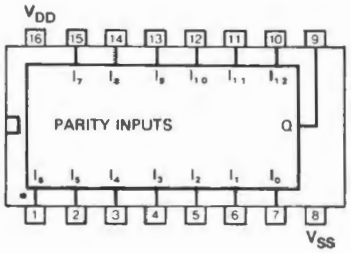
4529B Dual 4-channel analog data selector three state outputs



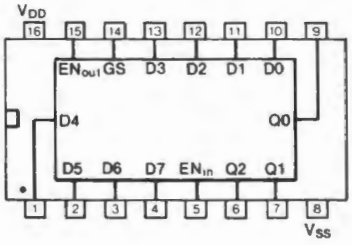
4530B Dual 5 input majority logic gate



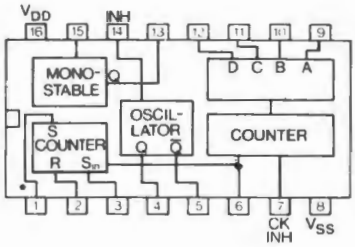
4531B 12 bit parity tree



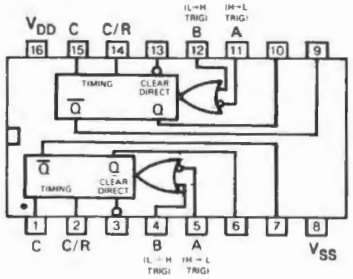
4532B 8 bit priority encoder



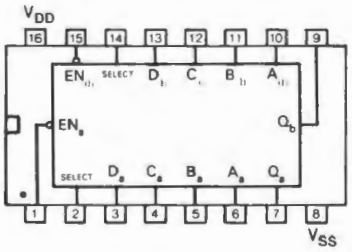
4536B Programmable timer



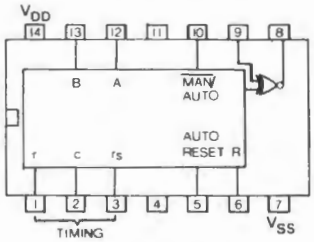
4538B Dual precision retriggerable/ resettable monostable multivibrator



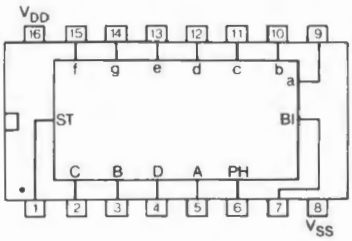
4539B Dual 4 channel data selector/ multiplexer



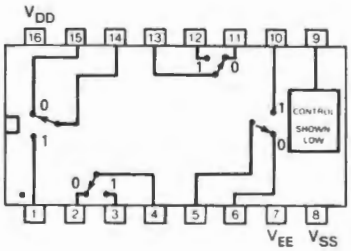
4541B Programmable timer



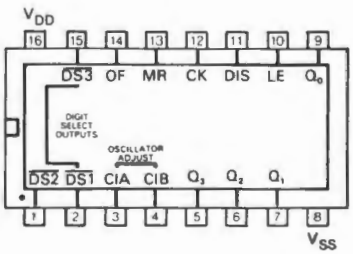
4543B BCD-to-seven segment latch/decoder/driver



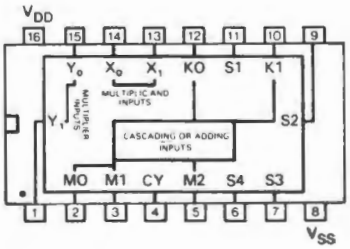
4551B Quad 2-input analog multiplexer/ demultiplexer



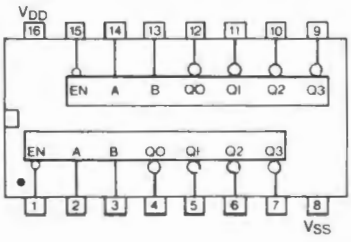
4553B Three-digit BCD counter



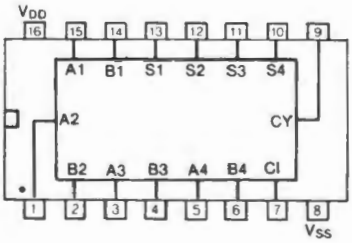
4554B 2 bit by 2 bit parallel binary multiplier



4556B Dual binary to 1 of 4 decoder

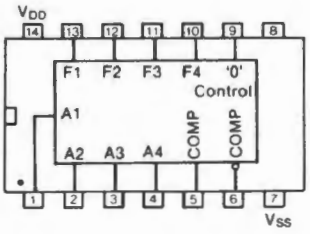


4560B Natural BCD adder

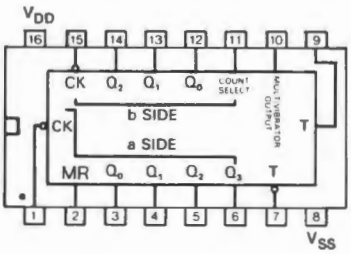


RS data

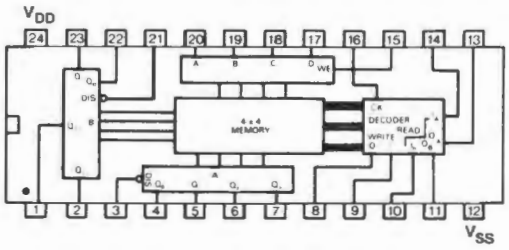
4561B 9's Complementer



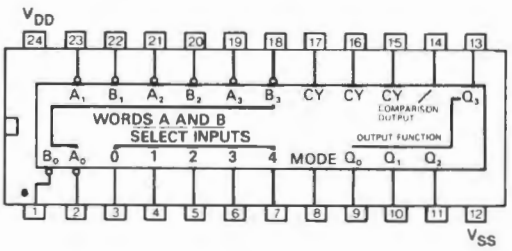
4566B Industrial time base generator



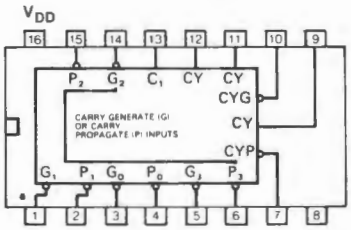
4580B 4 x 4 Multiport register



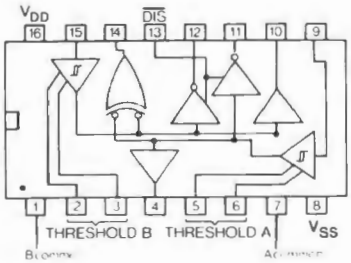
4581B 4 bit Arithmetic logic unit



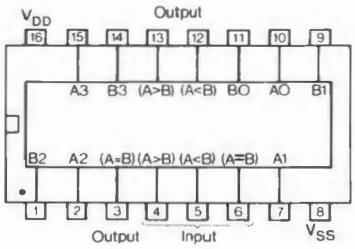
4582B Look-ahead carry block



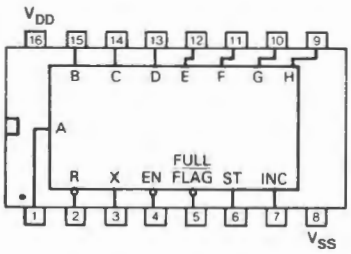
4583B Dual schmitt trigger



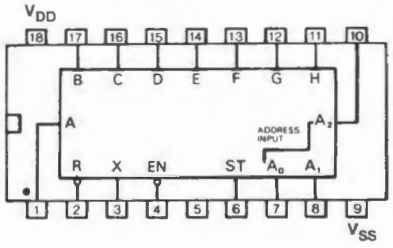
4585B 4 bit magnitude comparator



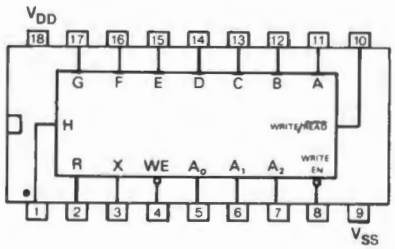
4597B 8 bit bus-compatible latches



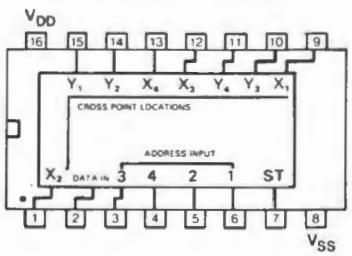
4598B 8 bit bus-compatible latches



4599B 8 bit addressable latch



45100UB 4 x 4 Crosspoint switch with control memory



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RS data

Electronic displays

Three types of display are available: each have differences as far as the display appearance, operation and electrical characteristics are concerned. Section I describes each device type, section II contains details of suitable decoder/drivers with circuit applications. Separate data sheets are available on the following products:

3835 LED Driver i.c.'s and bargraph modules
3964 LCD Decoder drivers RS7211 and 7211B
4197 Alphanumeric displays RS 1414 and 2416
4709 Display driver, serial data input RS5450
4787 Triplex LCD driver RS7231A
5370 LED Display with integral counter

For information on counter/driver i.c.'s consult the semiconductor section of the current catalogue.

Section I — Types of display

Incandescent (filament)

Incandescent displays consist of a number of filaments housed within an evacuated glass envelope. The filaments being arranged in the standard 7-segment format and can display all numbers 0 to 9. A D.I.L. version is available which also has a R.H. decimal point. The main advantages of filament displays are direct T.T.L. compatibility without the need of limiting resistors, white light output allowing a number of coloured filters to be used and high brightness.

L.E.D.

A range of solid state semiconductor displays having the advantages of mechanical ruggedness, long life and easy interface with semiconductor circuitry.

- **Display bezels** are available to accommodate the majority of the L.E.D. displays:
- **Discrete L.E.D. displays** in a range of character heights; 0.3, 0.43, 0.5, 0.56, 0.8 & 1 in. Certain types have segment colours available in Red, Green, and Yellow, with common anode or common cathode connections and dual format i.e. 7-segment or ±1, thus providing many possible multidigit displays.
- **0.5 inch multiplexed displays** in two and four digit formats in either common anode or common cathode versions. Displays may be edge stacked to give increased number of digits. Multiplexing reduces the number of decoders and drivers and requires less power than d.c. drive to achieve the same display intensity.
- **0.11 inch 4 digit multiplexed display** housed in a 14 pin dual in line clear moulded package incorporating magnifier lens. Device may be end stacked for longer displays and is typical of the types used in desktop calculators, hand-held instruments, metering devices and various consumer products, where low power consumption and battery supplies are required.
- **0.27 inch discrete displays with logic.** Two different displays are available with integrated logic chip. One version offers a hexadecimal display with T.T.L. compatible 4-bit latch and decoder/driver, whilst the other offers a 7-segment display with B.C.D. counter, 4-bit latch and decoder/driver.
- **L.E.D. Bar arrays in 10 and 30 segments.** The 10 bar types, red and green versions, are in a 20 pin D.I.L. package which may be end stacked as desired. The Red 30 segment array is housed in an attractive black display bezel which may be panel or surface mounted making it ideal for many applications including analogue meters, bargraphs, level and trend indicators.

Suitable drivers for both types are the **3914** and **3915** devices, stock no's 308-174 and 308-865 (see semiconductor section of the catalogue.

Liquid crystal

Unlike all other types of displays these do not emit light but reflect incident or transmit back light. Power consumption is extremely low making them ideally suited for battery powered equipment. The types available are field effect devices with either 3½, 4, 4½, 6 or 8 digit, 7-segment format. Operation is from an a.c. supply, typically 5V r.m.s. For this reason special forms of decoding are necessary; this is further explained in section I I. Panel mounting bezels are available to accommodate L.C.D displays.

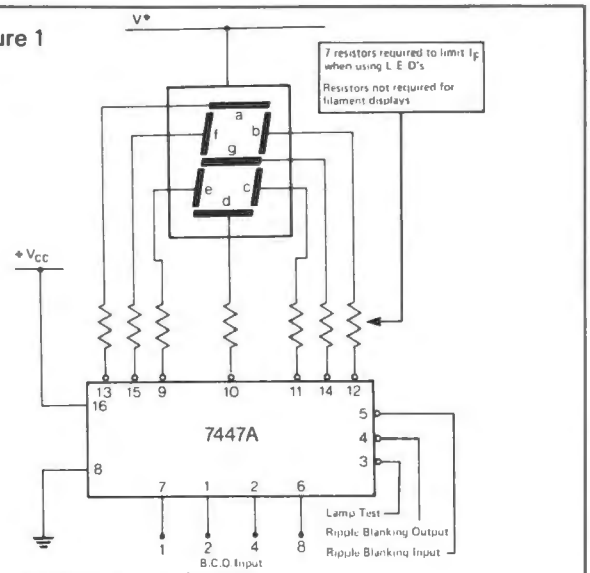
NOTE: The maximum d.c. component allowed to appear across the device is 25 mV.

Section II Decoders/Drivers

7447A

B.C.D. to 7-segment T.T.L. decoder/driver for use with filament or L.E.D. displays. Incorporating open collector output transistors capable of sinking 40 mA. Figure 1 gives details of interconnecting filament and common anode L.E.D. displays with the 7447A.

Figure 1



To determine value of resistors for L.E.D's use the following formula:

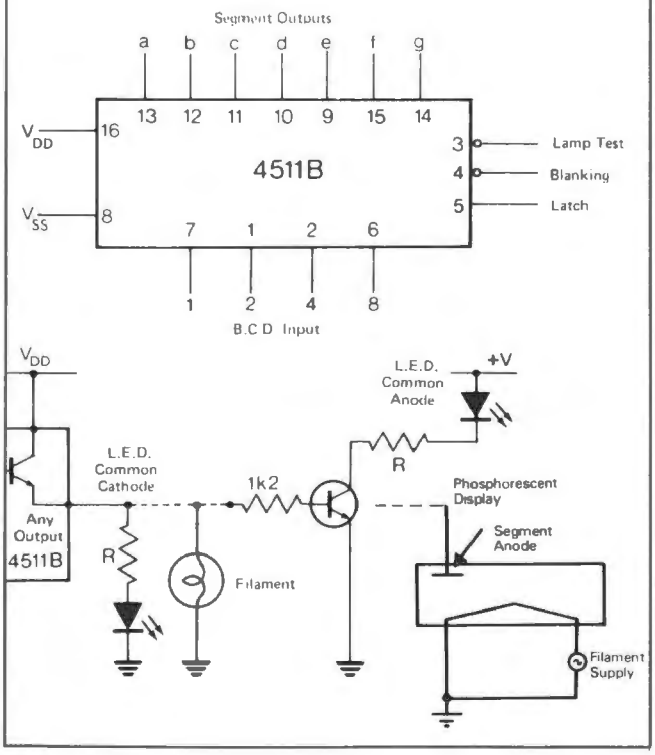
$$R = \frac{V^{+} - V_F - V_{OL}}{I_F}$$

Where V^{+} = Supply Voltage
V_F = Voltage drop across L.E.D.
V_{OL} = 7447A low output voltage (typ. 0.27V)
I_F = Required segment current

4511B

B.C.D. to 7-segment C-MOS decoder/driver with integral latch. Active pull up output capable of sourcing 25 mA. Will drive a filament, common cathode L.E.D. or phosphorescent display directly. Figure 2 shows methods of driving various displays.

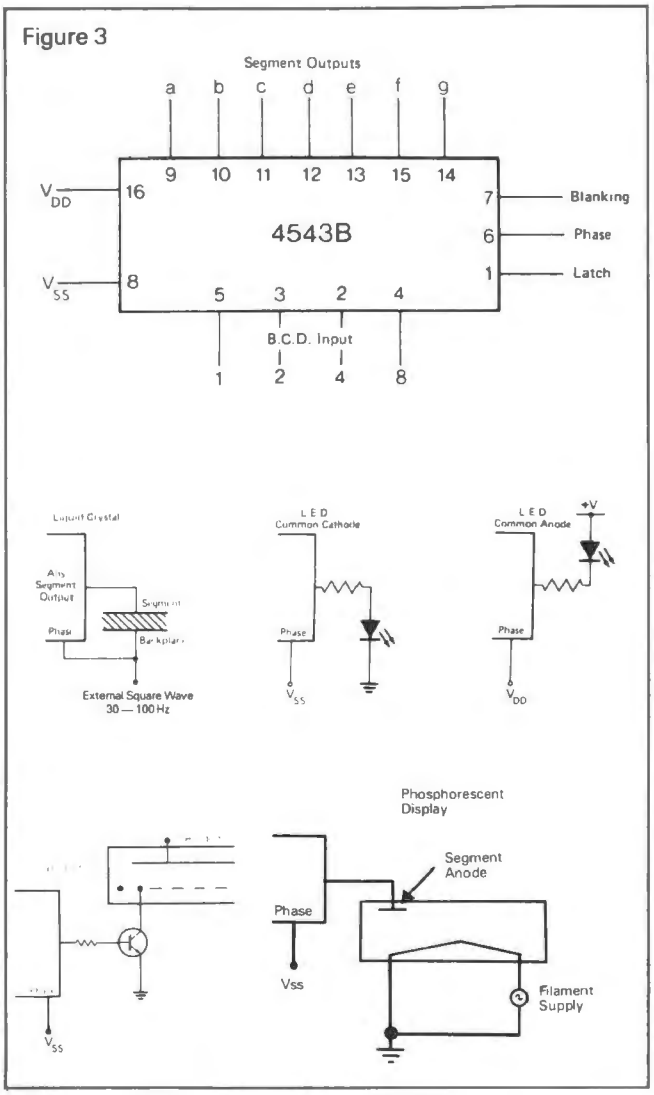
Figure 2



4543B

Similar to the 4511B but designed specifically for Liquid Crystal displays although the phase input may be tied 'high' or 'low' enabling other types of display driving. Source or sink current 10 mA maximum. Figure 3 shows various output connections.

Figure 3

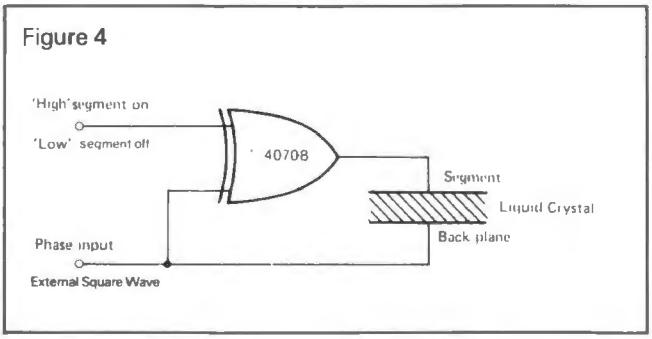


4070B

Not strictly a decoder the 4070B C-MOS quad exclusive OR gates are used for single segment driving of Liquid Crystal displays, Figure 4 shows the interconnections required.

NOTE: The use of 4543B and 4070B C-MOS drivers with Liquid Crystal displays produces an artificial a.c. drive by applying a square wave to the phase input.

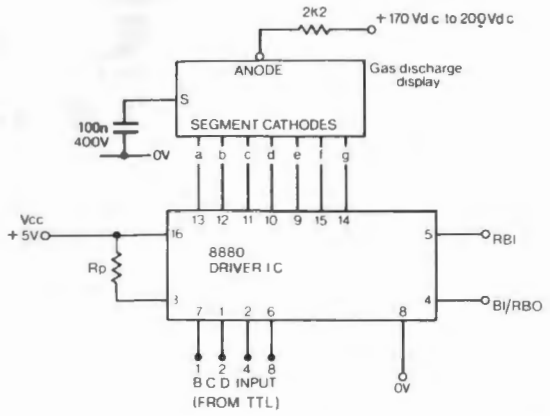
Figure 4



8880

A high voltage 7-segment decoder/driver designed to decode B.C.D. and drive gas filled 7-segment display tubes. See Figure 5.

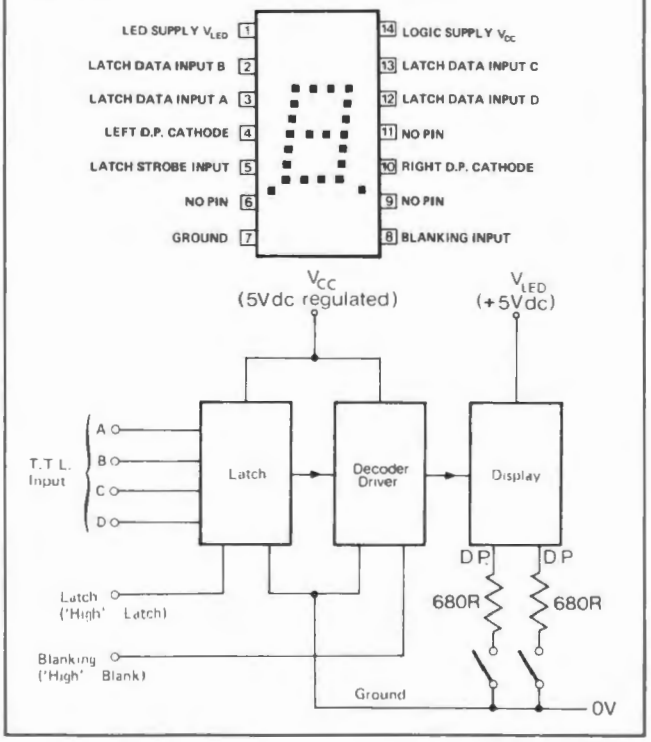
Figure 5



0.27 in with Logic (hexadecimal TIL 311)

Full hexadecimal decoding with integral latch, blanking and constant current drive to L.E.D. display. The two decimal points require external limiting resistors. See Figure 6.

Figure 6



0.27 in with Logic (7-segment TIL 306)

7-segment decoder/driver with integral B.C.D. counter and four bit latch. Features allow high speed fully synchronous multidigit counter-systems to be realised without resort to external logic. See Figure 7.

Figure 7a

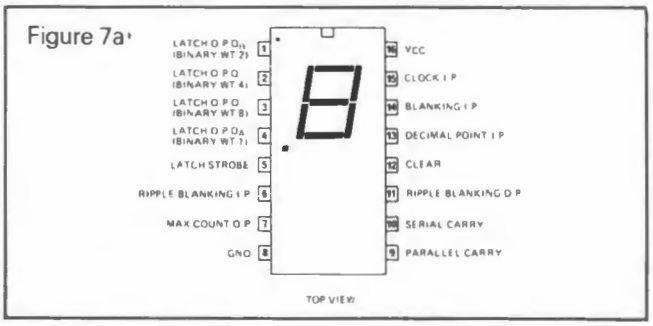
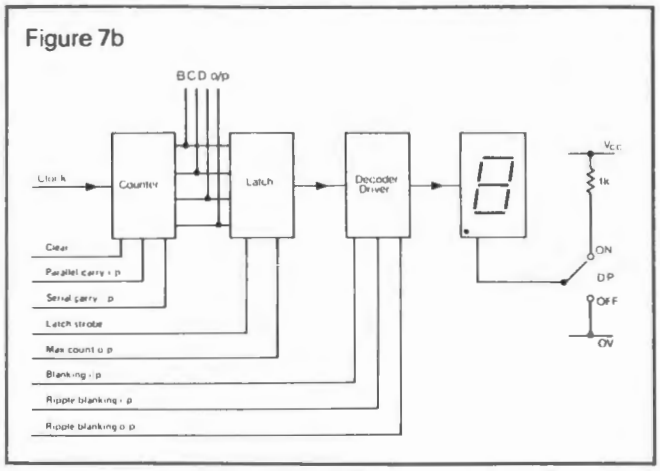


Figure 7b



Additional information

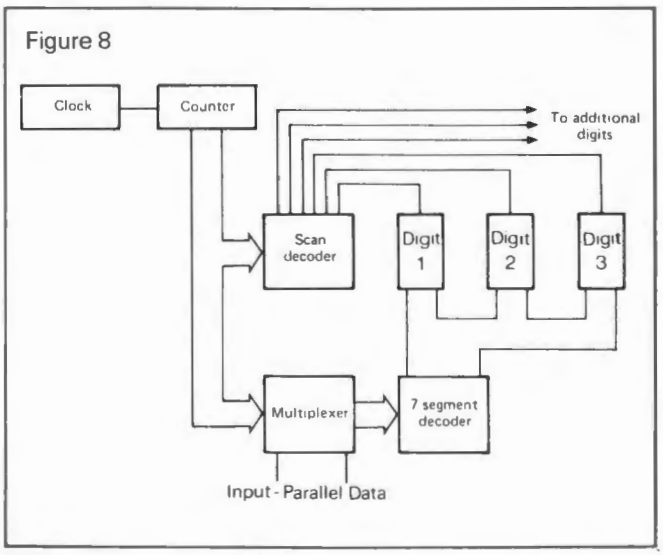
Multidigit displays

The simplest method of direct driving multidigit displays is to use a decoder/driver for each digit and operate each independently, however, various facilities may be required necessitating interconnections between each decoder. (See multiplexing).

Multiplexing

Time division multiplexing can reduce the number of decoders required together with a reduction in the number of interconnections between display and driver circuitry. This form is particularly suited for remote displays. Multiplexing is already incorporated in some multidigit drivers when the number of output pins is limited, such devices as the ZN1040E and the 7217 have full multiplexing over four digits. The basic operation for this method of driving is shown in Figure 8.

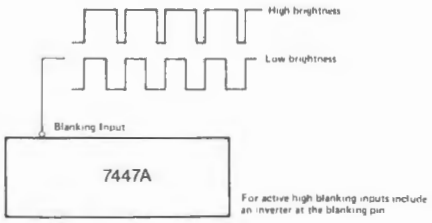
Figure 8



RS data

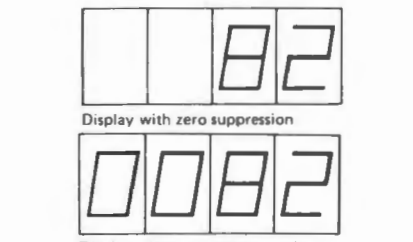
Intensity control
Adjustment of the light output of L.E.D. and filament displays may be achieved by pulse width modulating the Blanking Input of the decoder. Refer to Figure 9. The frequency of this modulation should be high enough to prevent display flicker at short duty cycles.
The 7447A decoder does not have Blanking Inputs but the Ripple Blanking Output may be used. In this case commoning more than one input may only be done when each RBO pin is individually buffered thereby preventing interaction. Intensity control cannot be incorporated into Liquid Crystal Displays.

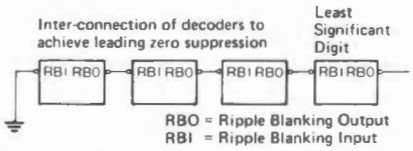
Figure 9



Zero suppression
Leading or trailing zero suppression, often termed Ripple Blanking, is a means by which unnecessary zero's in the display are blanked. The connections required are shown in Figure 10.

Figure 10





The 7447A incorporates Ripple Blanking Input and Output connections whilst the 4511B and 4543B do not, however, by using external gating the Blanking Input may be incorporated to achieve this facility.

Storage
A storage or latching operating i.e. once 'latched' further changes in the B.C.D. input information do not affect the display, may be achieved using the internal latches of the 4511B or 4543B or separate latches such as the 7475 Quad bi-stable latch in conjunction with the 7447A. Multidigit drivers incorporate latching facilities.

Lamp test
A lamp test facility is incorporated in some of these decoders. When operated all segments of the display are illuminated regardless of the input data.

Display/Decoder selection
Table 1

Decoder/Driver	7447A	4511B	4543B	4070B	ZN1040E	7217
Display Type: Common Anode L.E.D. Common Cathode L.E.D.	√	 √	√ √		√* √*	√
Multi-Digit Multiplexed – Common Anode Filament	 √	 √			√*	√
Liquid Crystal Gas Discharge Phosphorescent		 √	√ √* √	√	 √*	
0.27 Hexadecimal 0.27 7-Segment	INTEGRAL LOGIC					

* requires buffer transistors

NOTE: Apart from the display/decoder pairs shown in Table 1 additional forms of display driving may be achieved using external buffer or inverting stages.

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RS data

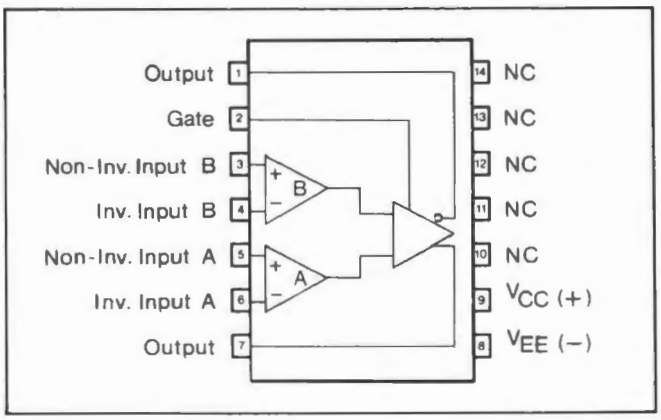
Gated wideband amplifier

Stock number 306-982

The RS Gated wideband amplifier is a monolithic integrated circuit housed in a 14 pin D.I.L. package and designed for wideband video amplifier use. Because of its gated, two-channel, differential design, a number of other applications are possible including video amplifier with AGC, amplitude modulator, balanced modulator, pulse-width modulator, frequency shift keyer, and others.

Maximum ratings $T_A = +25°C$

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+12 −12	V_{dc}
Input Differential Range	V_{IDR}	± 15.0	Volts
Load Current	I_L	25	mA
Power Dissipation Derate above $T_A = +25°C$	P_D	625 5.0	mW mW/°C
Operating Ambient Temperature	T_A	0 to +75	°C
Storage Temperature	T_{STG}	−65 to +150	°C



Electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Single ended voltage gain	A_{VS}	16	19.5	23	dB
Bandwidth	BW		50	-	MHz
Input impedance (f = 50 kHz)	Z_i	3.0	10	-	k Ω
Output impedance (f = 50 kHz)	Z_0		25	-	Ω
Output differential voltage (R_L = 10 kΩ, f = 50 kHz)	V_{ODR}	1.5	2.5		V p-p
Input bias current	I_{IB}		15	30	μ A dc
Input offset current	I_{10}		2.0		μ A dc
Input offset voltage	V_{10}			7.5	m V dc
Quiescent output dc level	V_0		0.2		V dc
Output dc level change (Gate input voltage change + 5 to OV)	$\triangle V_0$		±15		m V
Common mode rejection ratio (f = 50 kHz)	CMRR		85		dB
Input common mode voltage range	V_{ICR}		± 2.5		V_p
Gate characteristics (see note 1) Gate input voltage - low	$V_{IL(G)}$	0.2	0.4		Vdc
Gate input voltage - high	$V_{IH(G)}$		1.3	3.0	
Gate input current - low	$I_{IL(G)}$			4.0	mA
Gate input current - high	$I_{IH(G)}$			4.0	μ A
Step response (e in = 20mv)	t_{PLH} t_{PHL} t_{TLH} t_{THL}		6.5 6.3 6.5 7.0		nS .. .. ..
Wideband input noise (5.0 Hz to 10 M Hz, R_S = 50/Ω/)	e_n		25		μV (r.m.s.)
D.C. power consumption	P_C		70	150	mW

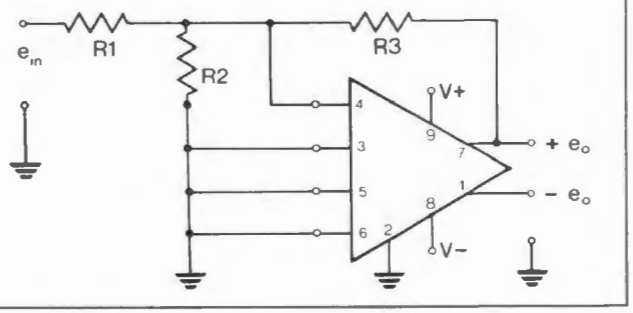
NOTE: $V_{IL(G)}$ is the gate voltage when Channel A gain ≤1 and B ≥16 dB.
$V_{IH(G)}$ is the gate voltage when Channel B gain ≤1 and A≥16 dB.

Video switch, open and closed loop conditions

The basic configuration for this device used as a two-channel wideband amplifier or video switch is shown in Figure 3A. The single-ended gain, as specified on this data sheet, in this configuration is 18dB. Small signal frequency response is shown as the upper curve in Figure 2 illustrating the wide bandwidth capability.

In some applications a closed loop configuration might be considered to obtain differential gain ratios or bandwidth characteristics. A general circuit is given in Figure 1 for one channel operation.

Figure 1: **Closed loop configuration**



$$Acl = -\frac{R3}{R1}\left(\frac{10}{11 + \frac{R3}{R1} + \frac{R3}{R2}}\right)$$

The usual approximation for closed loop gain Acl = –R3/R1, cannot be used with this device due to the small open loop gain. (18dB)

typical values: R1 = 1KΩ R2 = 10KΩ

The small signal response of a closed loop gain of 0dB is shown in Figure 2.

Gated video switch

Figure 3A shows the amplifier connected as a gated analog switch. It should be pointed out here that the number of external components required for this application is very minimal. This particular usage requires only one resistor. In this application, a signal (analog or digital) is appied to the amplifier at pin 3. With the logic signal at pin 2 at a logic 1 state (positive voltage) the input signal is amplified and passed through the amplifier. However, if the logic signal at pin 2 is at a logic 0 state, the amplifier is turned off and no signal will pass through the device. If it were required that the opposite logic levels pass or block the signal, the input signal can just as easily be applied to pin 4 or 6 with pins 3 and 5 grounded. In this case, a high logic level would block transmission and a low logic level would pass the signal, making use of inverters unnecessary. Taking "channel select time" as the time delay from the 50% point of the gate pulse to the 50% point of the full output swing, it is observed to be approximately 20 ns. During the time that the gating logic is in the low state, the circuit which gates the amplifier must sink a maximum of 2.5mA, which most forms of saturated logic can do easily. When the gating logic is in the high state, the circuit that gates the amplifier must source only the leakage current of a reverse biased diode, which is 2μ A maximum. These requirements are quite similar to the output of a standard TTL logic gate or C-MOS buffer.

Figure 2: **Single ended voltage gain versus frequency**

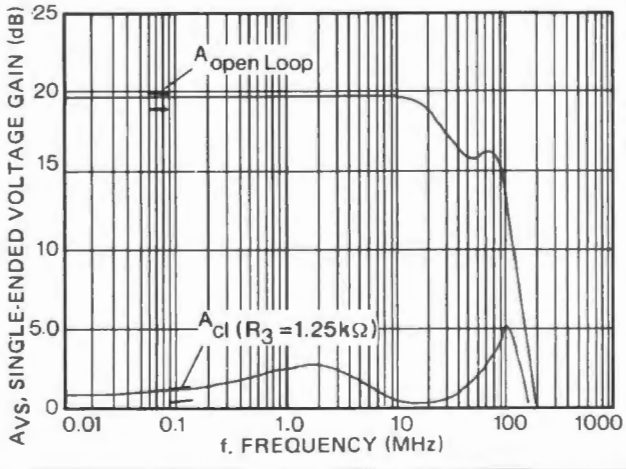
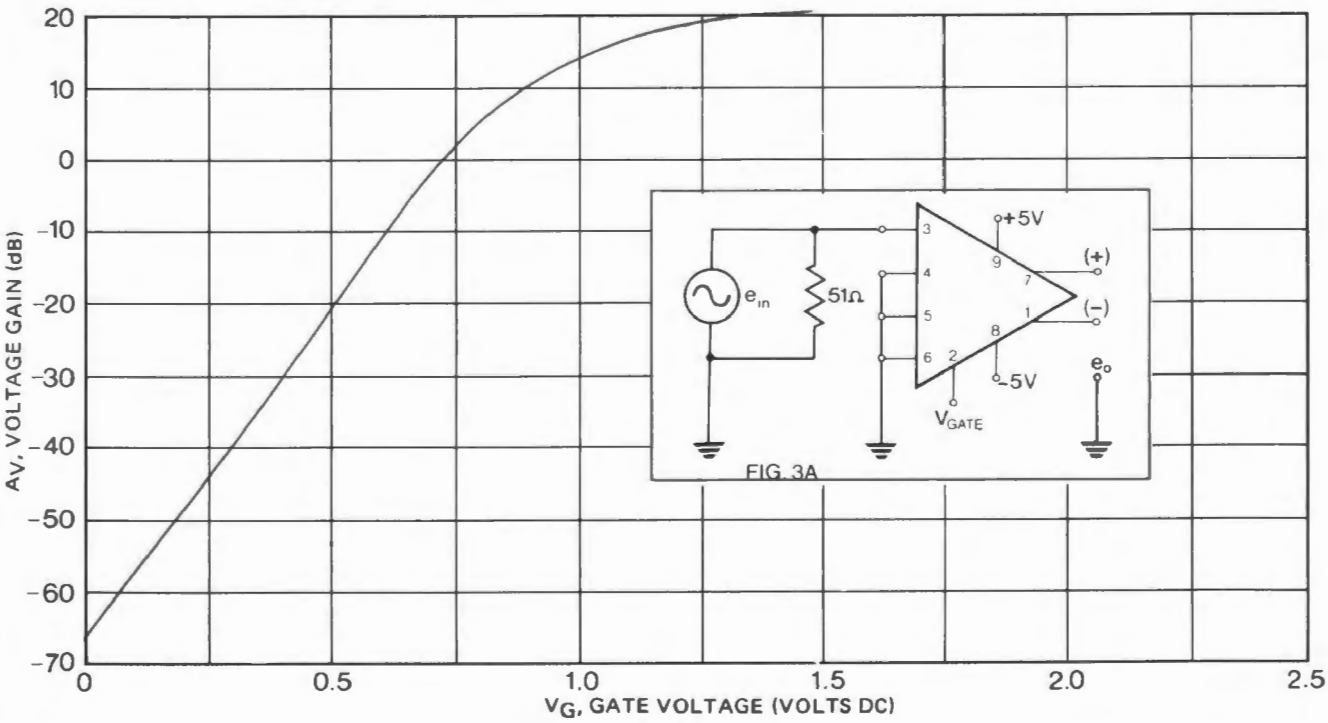


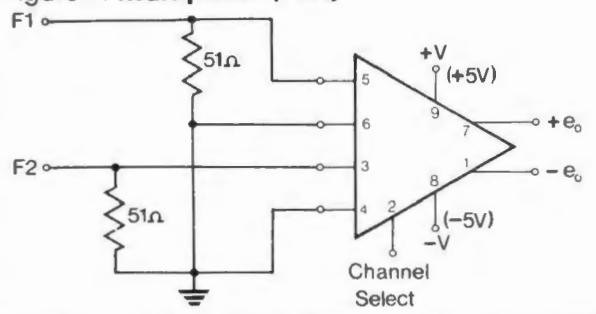
Figure 3: **Voltage gain versus gate voltage**



Frequency Shift Keyer (FSK)

Rather than grounding pins 3 and 5 it is possible to apply a second frequency to these input pins and select which of the two frequencies, either F1 or F2, will be passed through the amplifier. This is illustrated in Figure 4. As the circuit is shown frequency F2 will be passed when the voltage at pin 2 is greater than +1.5 volts F1 will be passed when the voltage at pin 2 is approximately zero volts.

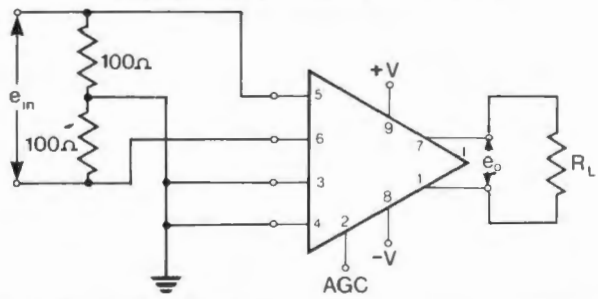
Figure 4: **Multiplexer (FSK)**



Wideband differential amplifier with AGC

The gate characteristics of the device, as shown in Figure 3, also make it useful as an AGC amplifier. With a dc voltage applied to the gate pin, as much as 100 dB of AGC can be obtained. Since there is essentially no dc level shift with AGC, the output waveform will collapse symmetrically about zero with little or no waveform distortion. This application is shown in Figure 5.

Figure 5: **Wideband amplifier with AGC**



Amplitude modulator

The gate characteristics of the amplifier also makes it useful as an amplitude modulator. Shown in Figure 6 and Table 1.

Table 1. Amplitude modulation characteristics

Limits			
$f_{carrier}$	$f_{modulation}$	M_U	M_D
To 100 MHz	To 1 MHz	0.62 Over Entire Range	0.66 Over Entire Range

V_{out} Quiescent — 700 mV (p-p)

$$M_D = \frac{E - E_{min}}{E} \quad \text{(down modulation)}$$

$$M_U = \frac{E_{max} - E}{E} \quad \text{(upward modulation)}$$

where:

E = peak amplitude of the unmodulated carrier

E_{max} = maximum amplitude attained by the modulated carrier envelope

E_{min} = minimum amplitude of the modulated carrier envelope

Amplitude modulated waveform

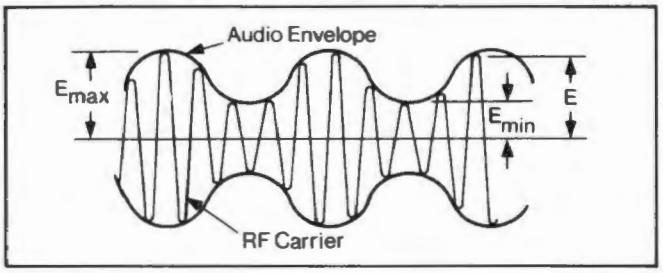
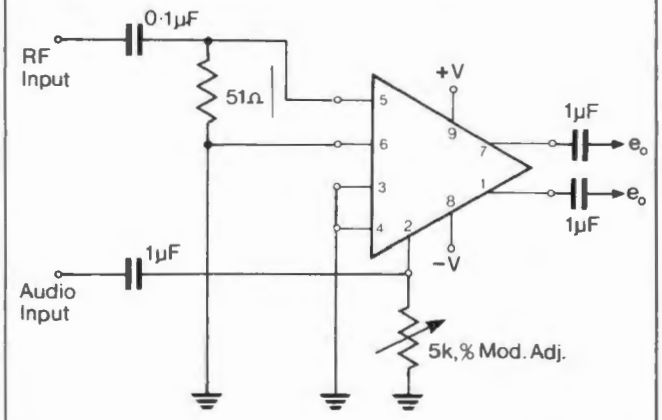


Figure 6: **Amplitude modulator**



Balanced modulator

The amplifier can be connected as shown in Figure 7 to function as a balanced modulator.

The output is composed of only the sum and difference frequencies (sidebands), and the carrier is suppressed. Table II gives the characteristics for this configuration.

Figure 7: **Balanced modulator**

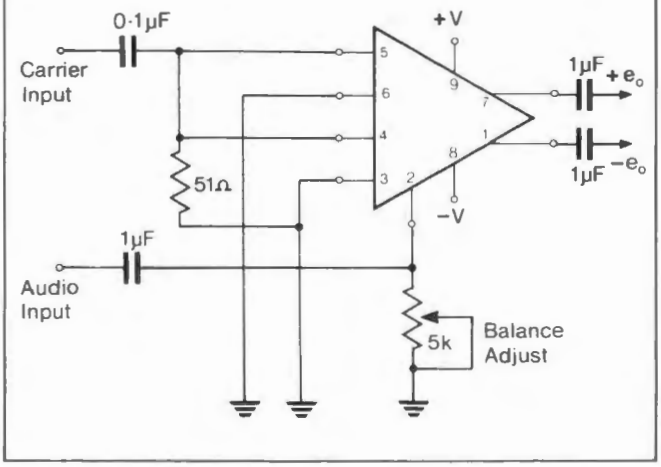


Table II — Balanced modulator characteristics

Hz $f_{carrier}$	Hz $f_{modulation}$	Carrier Rejection (dB)
15 k	3 k	65
100 k	3 k	57
455 k	1-5 k	45
1 m	1 k	38
2 m	1 k	30
10 m	1-5 k	25-30
30 m	10 k	22

RS data

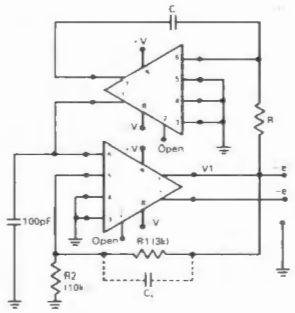
Gated astable multivibrator

Using two amplifiers connected as in Figure 8 results in a rate-controllable square wave output.

$$T = \frac{2\,RCR2}{R1 + R2} \text{ and frequency } f = \frac{1}{2T}$$

As the waveform from the astable is self-generating the rise and fall times are not the maximum available from the device. This astable was used at frequencies to 2 MHz with rise and fall times as indicated in Table III, including the effects of a speed-up capacitor.

Figure 8. **Astable multivibrator**



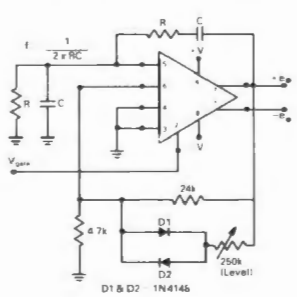
Gated oscillator with level control

Figure 9 shows the amplifier used as a gated oscillator with an adjustable level control.

Table III — Gated astable response (at 250 kHz)

V_{CC}	C_S	tr (ns)	t^f (ns)	V_O (p-p)
6.0	0	25	45	2.1
6.0	100pF	22	30	2.1
5.0	0	25	45	1.75
5.0	100pF	13	45	1.75

Figure 9: **Gated oscillator**



Rise times of this oscillator are dependent on the RC network, varying from 1 to several cycles of the oscillation frequency. At 160 kHz, t_{rise} was $< 30\ \mu$ s and at 8 MHz, t_{rise} was < 100 ns. Fall time is the channel select time, equal to 20 ns.

Useful frequency range with this passive network was from below 1 kHz to 10 MHz.

Single supply operation

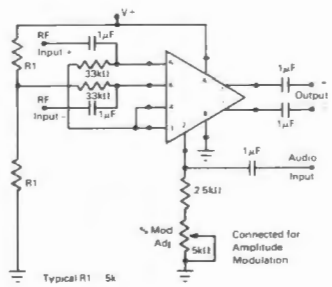
All of the previous applications discussed have considered the use of symmetrical biasing supplies for operation. As it may be necessary under some conditions to use a single supply an alternating biasing circuit must be used. This is done by establishing an artificial ground for the amplifier at one-half the value of the single supply. Figure 10 illustrates this method for the amplitude modulator.

The resistors designated R1 are used to establish a voltage level at $V_{supply}/2$. The current through these resistors is not critical but should be much larger than the bias current of 15 μA. To provide dc returns for the differential amplifier pair and still maintain reasonable input impedance, 33 kΩ resistors are specified from the bases of the differential pair transistors to the artificial ground. The typical value for bias current is 15μ A which places a common mode voltage on the differential amplifier of 0.5 V above the artificial ground. As all signals must be ac coupled in any case and the common mode limit is 2.5 V, this 0.5 V level is acceptable. All signals must be ac coupled to prevent the application of excessive common mode voltage to the amplifier.

Care should be also taken at the gate input to prevent excessive current drain while in the low state. The connection of 2.5kΩ resistor in series with the gate input will establish a similar artificial ground when the gate is taken to the actual ground.

This circuit can then be utilized to obtain the circuits discussed for symmetrical supplies.

Figure 10: **Single supply operation**



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RS data

Electronic attenuator

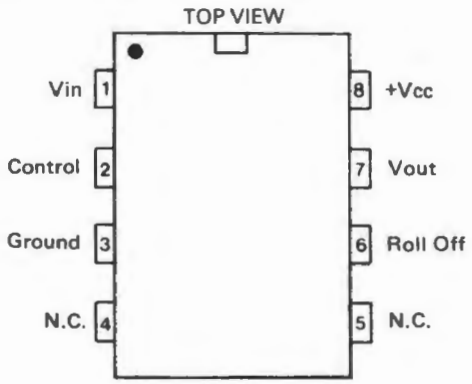
Stock number 306-803

A silicon monolithic gain controlled A.C. amplifier programmed by an external D.C. voltage or resistor. Applications include remote volume controls, speech compressor and expander circuits. The device is housed in an 8 pin D.I.L. plastic package suitable for use over the operating temperature range of 0°C to 75°C

Absolute maximum ratings $T_A = 25°C$

Supply voltage	20V d.c.
Power dissipation	1.2 Watts
Derate above 25°C	10mW/°C
Operating ambient temperature range	0 to +75°C.

Pin connections



Electrical characteristics

e_{in} = 100mV (r.m.s.), f = 1 kHz,
$R_{control}$ = 0, V_{cc} = 16V

Operating supply voltage	9-18V d.c.
Control sink current (e_{in} = 0)	2mA d.c. (max)
Input voltage	0.5V (r.m.s.) max
Input resistance	17 kΩ (typ)

Figure 1 **Attenuation versus D.C. control voltage**

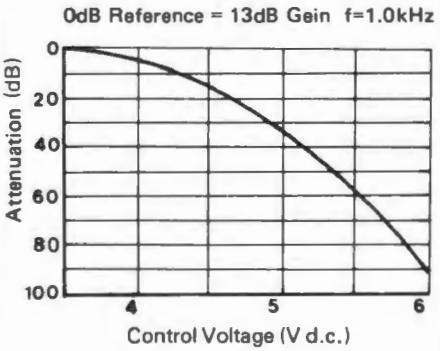


Figure 2 **T.H.D.**

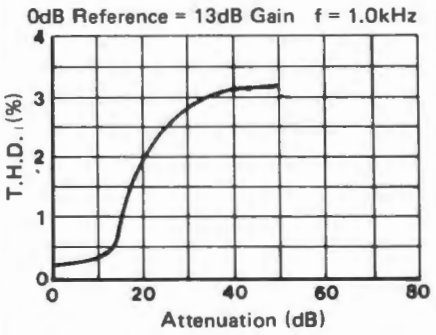


Figure 3 **Attenuation versus control resistor**

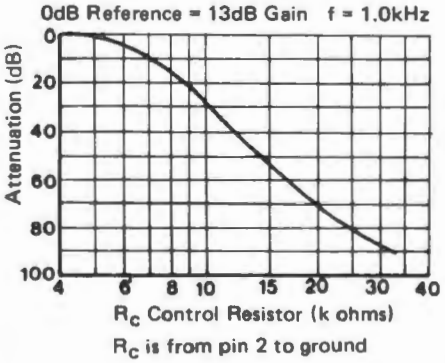


Figure 4 **Frequency response**

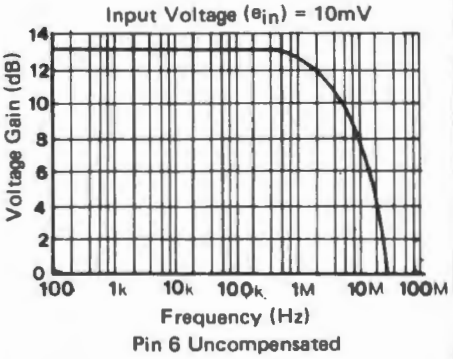
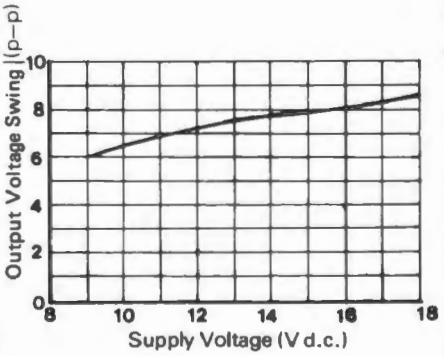


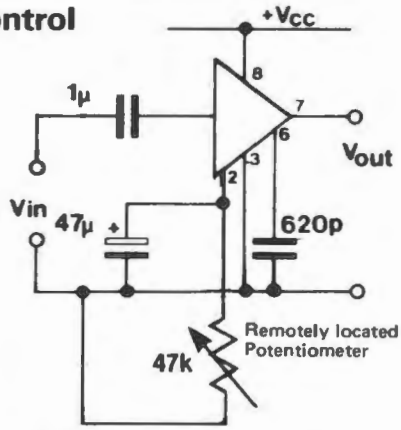
Figure 5 **Output voltage**



RS data

Applications

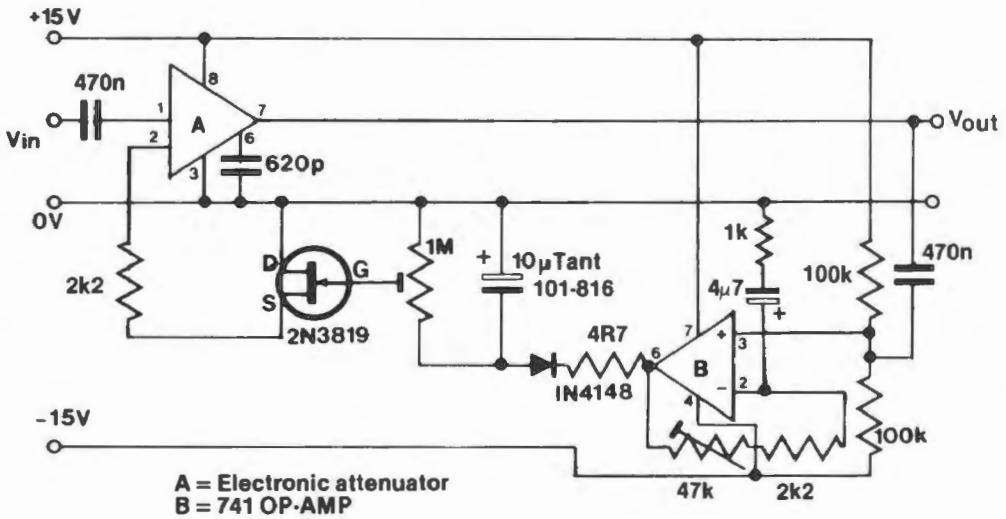
Remote volume control



A typical application where a remotely controlled amplifier is required. The potentiometer may be replaced by a D.C. voltage of 3.5 to 6V (maximum voltage or resistance gives the maximum attenuation). Useful frequency range 50 Hz to 100 kHz.

Note: The electronic attenuator can only be used to control A.C. voltages.

Audio compressor



Specification

Input signal compression range	13mV to 400mV r.m.s.
Output signal (2kΩ source)	60mV to 1.3 r.m.s. ± 1db over input range
Bandwidth	50 Hz to 20 kHz
Distortion	< 1% over input range
Attack time	approx. 50µs
Decay time	> 0.5s

The circuit is powered by a ± 15V d.c. supply which may consist of RS Regulator 305-636, the attenuation of input voltage, V_{in} is controlled by the effective drain - source resistance of the 2N3819 field effect transistor. The output of the attenuator (A) is fed back via amplifier (B) the gain of which may be adjusted by the 47kΩ preset. The output of amplifier (B) is rectified and a negative bias is applied to the gate of the 2N3819 field effect transistor.

Circuit adjustment

1) Set the gain of amplifier, (B) to its maximum value (47kΩ preset adjusted to maximum value)

2) Apply the maximum input voltage to be tolerated (within range 13mV to 400 r.m.s.)

3) Adjust the 1MΩ preset until Vout is approximately 60mV r.m.s.

4) Increase Vout by reducing the gain of the amplifier B until Vout is approximately 4 x V_{in}

The attenuator will now compress voltages in excess of V_{in}.

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For technical enquiries ring: 01-202 8252 or 0536-201234
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RS data

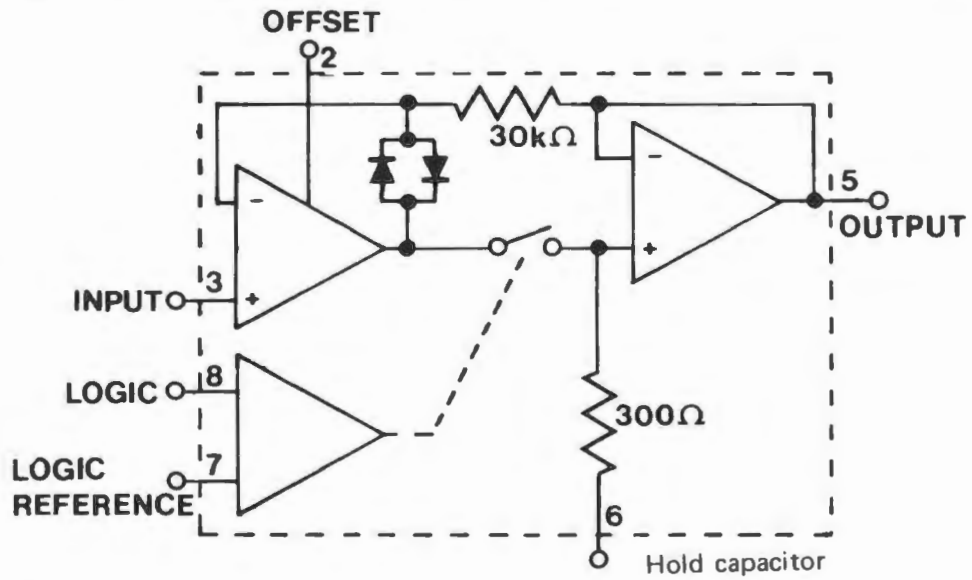
Monolithic sample and hold circuit

Stock number 307-086

This monolithic sample and hold circuit utilizes BI-FET technology to obtain high d.c. accuracy with fast acquisition of signal and low droop rate. A wide bandwidth allows the i.c. to be included within the feedback loop of 1 MHz op-amps without causing instability. Logic inputs on the device are fully differential with low input current, allowing direct connection to TTL, PMOS and CMOS. The 'sample and hold' operates from ±5 V to ±18 V supplies and is housed in an 8-lead T0-5 package. Equivalent to LF398.

Features

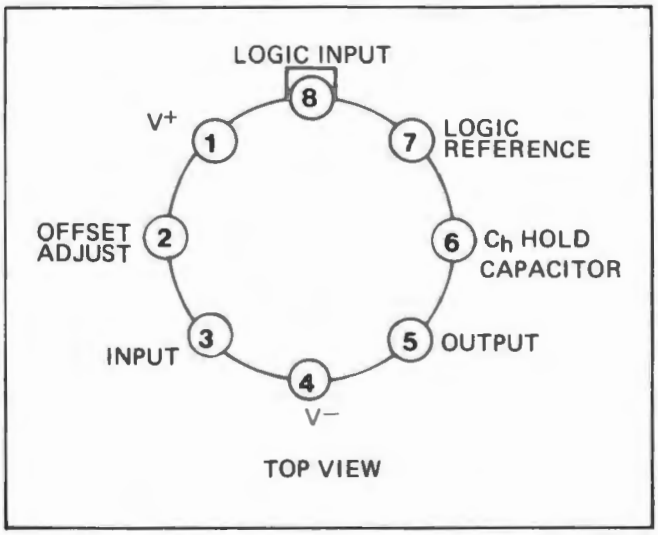
- Operation from ±5 V to ±18 V supplies
- Less than 10 μs acquisition time
- TTL, PMOS, CMOS compatible logic inputs
- 0.5 mV typical hold step C_h = 0.01 μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- Low droop rate (can be 5 mV/min with C_h = 1μF)



Maximum ratings

Supply Voltage	±18 V
Power dissipation*	500 mW
Operating ambient temp. range	0°C to 70°C
Storage temp. range	−65°C to +150°C
Input voltage	Equal to supply voltage
Logic to Logic reference differential voltage	+7 V, −30 V
Output short circuit duration	Indefinite
Hold capacitor short circuit duration	10 sec.

*The maximum junction temperature is 100°C. When operating at elevated ambient temperature, the T0-5 package must be derated based on a thermal resistance (ΘjA) of 150°C/W.



Electrical characteristics

	Conditions	Min	Typ	Max	Units
Input Offset Voltage V_{IO}	Tj = 25°C Full Temp. range		2	7 10	mV mV
Input Bias Current I_{IB}	Tj = 25°C Full Temp. range		10	50 100	nA nA
Input Impedance Z_i	Tj = 25°C		10^{10}		Ω
Gain Error *	Tj = 25°C R_L = 10 K Full Temp. range		0.004	0.01 0.02	% %
Feedthrough Attenuation Ratio at 1 kHz	Tj = 25°C, Ch = 0.01μF	80	90		dB
Output Impedance Zo	Tj = 25°C, 'HOLD' mode Full Temp. range		0.5	4 6	Ω Ω
Hold Step *	Tj = 25°C Ch = 0.01 μF, V_{out} = 0 V		1.0	2.5	mV
Supply Current	Tj ≥ 25°C		4.5	6.5	mA
Logic and Logic reference Input current	Tj = 25°C		2	10	μA
Leakage Current into Hold Capacitor	Tj = 25°C (see Note) Hold mode		30	200	pA
Acquisition Time to 0.1% *	ΔV_{out} = 10 V, C_h = 1000 pF C_h = 0.01 μF		4 20		μS μS
Hold Capacitor Charging Current	$V_{IN} - V_{OUT}$ = 2 V		5		mA
Supply Voltage rejection Ratio	V_{OUT} = 0	80	110		dB
Differential Logic Threshold	Tj = 25°C	0.8	1.4	2.4	V

Note: Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Typical performance characteristics * See definitions on page 4.

Figure 1:
Acquisition time

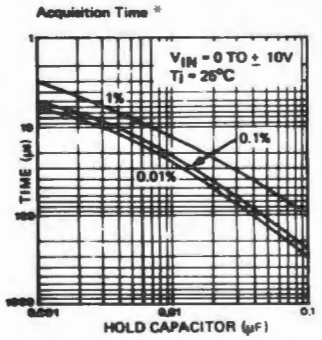


Figure 2:
Aperture time

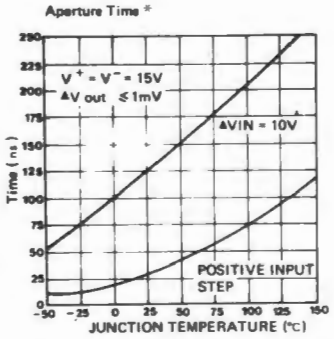


Figure 3:
'Hold' settling time

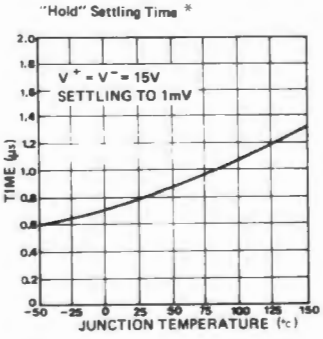


Figure 4:
Dynamic sampling error

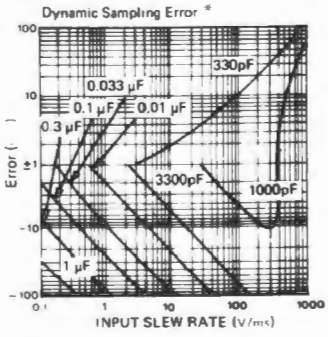


Figure 5:
Hold step

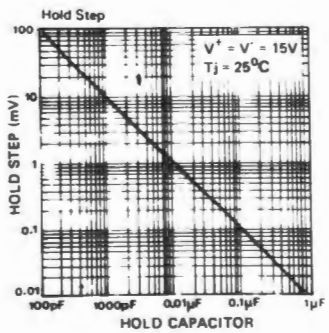


Figure 6:
Output droop rate

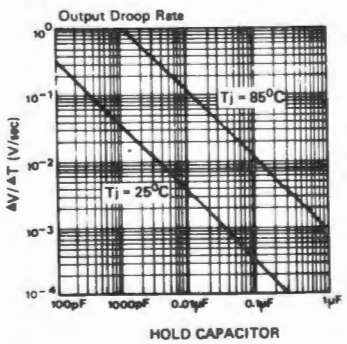
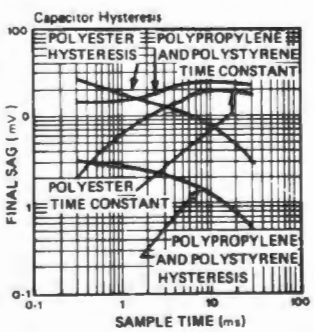


Figure 7:
Capacitor hysteresis



Technical hints

Hold capacitor

Hold step, acquisition time, and droop rate are the major considerations in the selection of a hold capacitor value. To select a reasonable value of capacitance the graphs on the previous page should be consulted. Bear in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the i.c.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A polyester capacitor, for instance, may 'sag back' up to 0.2% after a quick change in voltage. A long 'soak' time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene and polypropylene. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with > 1% hysteresis.

For more exact data, see the curve labelled capacitor hysteresis.

The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the device is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10–50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

d.c. and a.c. zeroing

d.c. zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give approximately 0.6 mA through the 1 k potentiometer. (See Fig. 8.)

a.c. zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01 μF hold capacitor and 5 V logic supply. For larger swings, a smaller capacitor (<10 pF) may be used.

Sampling dynamic signals

Sample error due to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to 300 Ω series resistor on the chip. This means that at the moment the 'hold' command arrives, the hold capacitor voltage may be somewhat different than the actual analogue input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analogue input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analogue phase delay and 100 ns logic delay, one could expect up to (0.1μs) (0.6 V/μs) = 60 mV error if the 'hold' signal arrived near maximum dV/dt of the input. A positive going input would give a ±60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analogue loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analogue delay will be (0.16 μs) (0.6 V/μs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analogue) for a total of −36 mV. To add to the confusion, analogue delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labelled Aperture Time has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the 'hold' command. This curve is based on a 1 mV error fed into the output.

A second curve, Hold Settling Time, indicates the time required for the output to settle to 1 mV after the 'hold' command.

Logic rise time

For proper operation, logic signals into the sample and hold must have a minimum dV/dt of 0.2 V/μs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for the signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 0.2 V/μs.

Digital feedthrough

Fast rise time logic can cause hold errors by feeding externally into the analogue input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analogue input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5 V will also help. (See Fig. 9.)

Figure 8: **d.c. zeroing**

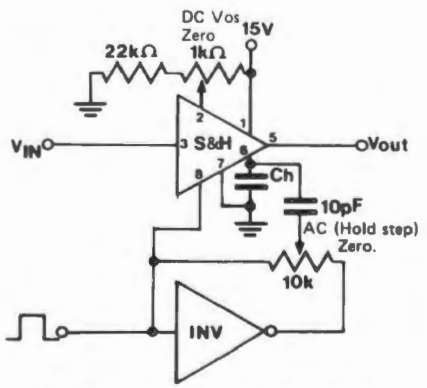
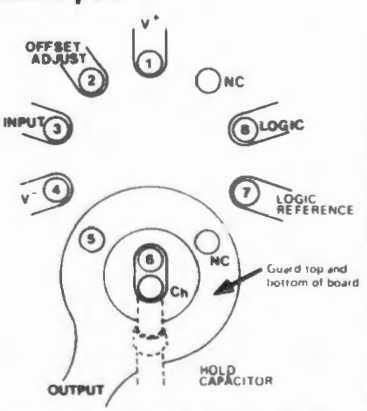


Figure 9: **Guarding techniques**



Use 10 pin layout.
Guard around
C_h is tied to output.

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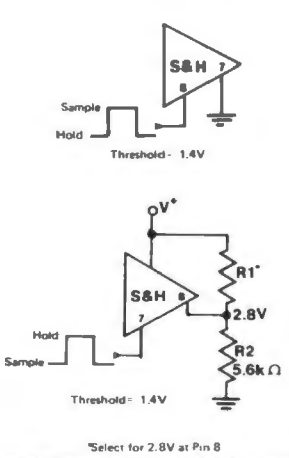
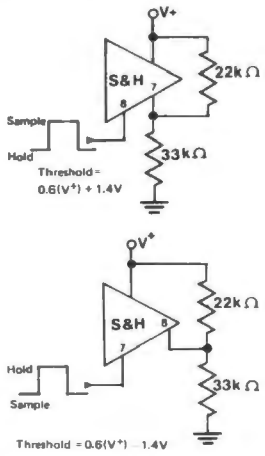
Figure 10: **Logic input configurations**

(a) TTL & CMOS
3 V≤V_L (Hi state) ≤7 V



(b) CMOS
7 V≤V_L (Hi state) = 15 V



(c) Op Amp Drive

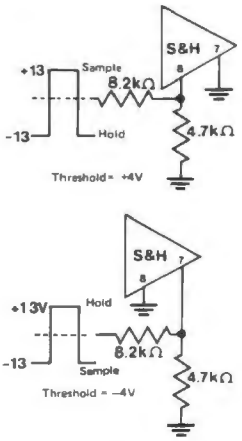
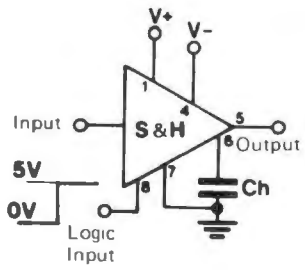
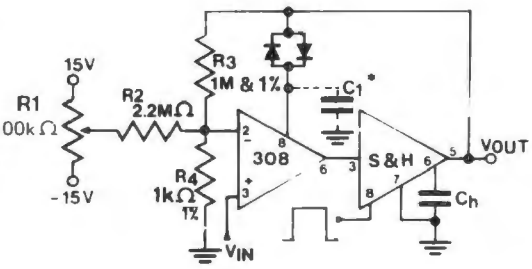


Figure 11: **Typical applications**

(a) Typical Connection

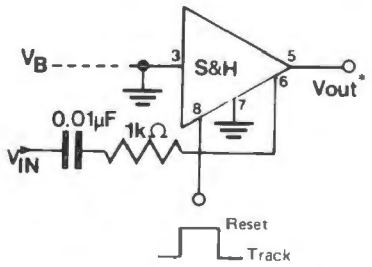


(b) × 1000 Sample & Hold



*For lower gains, the 308 must be frequency compensated. Use = $\frac{100}{A_V}$ pF from pin 8 to ground

(c) Sample and Difference Circuit
(Output follows input on Hold Mode)



* $V_{OUT} = V_B + \Delta V_{IN}$ (HOLD MODE)

Definitions

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (d.c.) analog input voltage. Logic swing is 5 V. Hold Step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. Magnitude of hold step is inversely proportional to hold capacitor value.

Acquisition Time: The time required to acquire a new analogue input voltage with an output step of 10 V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the 'hold' logic command.

Dynamic Sampling Error: The error introduced into the held output due to a changing analogue input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Aperture Time: The delay required between 'Hold' command and an input analogue transition so that the transition does not affect the held output.

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RS data

Digital clock timer i.c.

Stock number 307-115

The RS digital clock/timer i.c. 5387 AA incorporates all the logic circuitry required to act as the central controller in industrial clock timers. The device may be operated with a 12 or 24 hour display format, an AM/PM indicator output is available in the 12 hour mode. An internal comparator and override circuit allows the device to be used as a preselected interval timer. Four 7 segment L.E.D. indicators interface directly with the i.c. The functions displayed are selected via internal anti-bounce circuitry allowing S.P.S.T. switches to be used.

Features

- 50 or 60Hz reference input
- Direct L.E.D. drive
- AM/PM or 24 hour output
- Power failure indication
- Clock input noise rejection circuitry
- Presettable 59 minute countdown timer

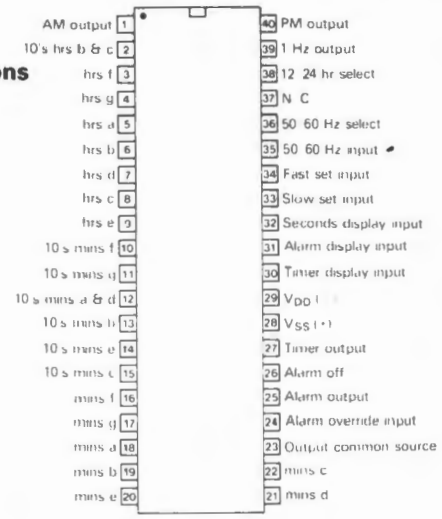
Absolute maximum ratings

Voltage at any Pin
(except segment outputs) — V_{SS} +0.3 to V_{SS} −30 V
Voltage at segment outputs — V_{SS} +0.3 to V_{SS} −15V
Storage temperature — −65 to +150°C
Lead temperature (soldering 10 sec) — 300°C

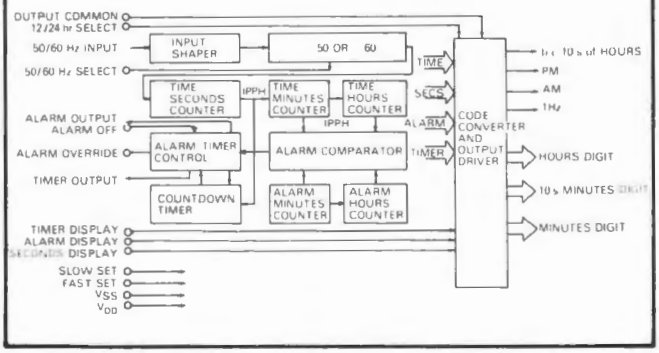
Operating conditions

Power supply voltage, V_{SS} — 8 to 26 V
V_{DD} — 0 V
Logical HIGH input — (V_{SS} −1) to V_{SS}
Logical LOW input, pin 35 — V_{DD} to (V_{DD} +2)
all other input pins — V_{DD} to (V_{SS} −6)
Operating temperature — −25 to +70°C
Operating frequency — 0 to 10 KHz

Pin Connections



Block diagram



Electrical characteristics V_{SS} = 24 to 26 V, f = 50/60 Hz, T_A = −25 to +70°C, unless specified

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supply Current	V_{SS} = 8V, no load			4	mA
	V_{SS} = 26V, no load			5	mA
Input leakage, pin 35				100	μA
Power Failure Detect Voltage	Note 1	1		7.5	V
Count Operating Voltage		8		26	V
Hold Count Voltage	Note 1			26	V

Note 1. The power-fail detect voltage is 0.5 V or more above the hold count voltage. The power-fail latch trips into power-fail mode at least 0.5 V above the voltage at which data stored in the time latch is lost.

Table 1. **Output current levels.** V_{SS} = 24 to 26 V, Output Common = V_{SS}

Parameter	Pin Nos.	Test Conditions	Min.	Max.	Units
Logical HIGH level, Source Current	2, 12	V_{OH} = (V_{SS} −4) V	16		mA
	39	V_{OH} = (V_{SS} −4) V	24		mA
	25, 27	V_{OH} = (V_{SS} −2) V V_{SS} = 24V	500		µA
	All others	V_{OH} = (V_{SS} −4) V	8	(Note 2)	mA
Logical LOW level, Leakage Current	2, 12	V_{OL} = (V_{SS} −14) V		10	µA
	39	V_{OL} = (V_{SS} −14) V		10	µA
	25, 27	V_{OL} = (V_{SS} −12) V	1		µA
	All others	V_{OL} = (V_{SS} −14) V		10	µA

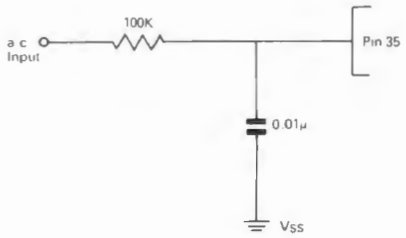
Note 2. Segment output current must be limited to 11 mA maximum by the user; power dissipation 1.2 W at 25°C. Derate by 6.6 mW/°C above 25°C.

Functional description

The block diagram of the clock/timer is shown on page 1. The various display control and setting functions are shown in tables 2 and 3.

50 or 60 Hz input. Pin 35 is the main clock time keeping input. This input is a schmitt trigger with approximately 6 V of hysteresis, allowing the input signal to be a filtered sinewave. Such a filter is shown in figure 1. This simple RC network should be used to remove possible line voltage transients that could cause the clock to gain time or damage the device. The internal prescaler, allowing the clock input to be a 50 or 60 Hz signal, is programmed via Pin 36. Left unconnected, an internal pull-down resistor holds the input a V_{DD}, the prescaler being set for 60 Hz operation. Tying pin 36 to V_{SS} selects 50 Hz operation.

Figure 1 **Input filter**

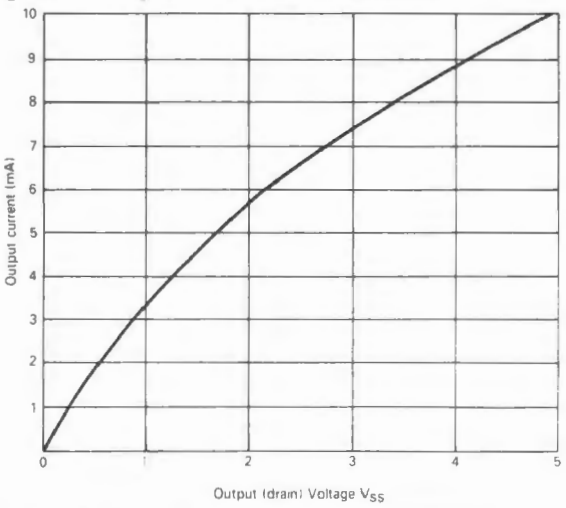


Display mode select. Pins 30, 31 and 32 select the desired display information. Refer to table 2 for the necessary connections. Single pole switches may be used to select the appropriate functions by connecting the input to V_{SS}. Once again internal pull-down resistors tie the input to V_{DD} when unconnected.

Output common source, Pin 23. All display output drivers are open drain devices with all sources commoned. The common source should be connected to V_{SS}.

Typical output Drive currents are shown in figure 2.

Figure 2 **Output current characteristics**



12 or 24 hour select. Pin 38: leaving this pin unconnected the clock is set to provide a 12 hour format; tying the input to V_{SS} selects the 24 hour mode of operation.

Power fail indication. If the power to the integrated circuit drops, indicating a momentary a.c. power failure and possible loss of clock, all "ON" segments will flash at a 1 Hz rate. A fast or slow set input resets the power failure latch and returns the display to normal.

Comparator (alarm) operation. The comparator senses coincidence between the alarm setting and time counters. At coincidence an internal latch enables the externally connected circuit. This latch remains set for 59 minutes, during which time the alarm output (Pin 25) remains "ON" unless it is temporarily inhibited by the override circuit or reset by the alarm "OFF" input. Figure 3 shows the output circuit for the alarm output.

Override alarm input, Pin 24: this input temporarily inhibits the alarm once latched for 8 to 9 minutes, after which time the alarm output becomes enabled again. This override feature may be used repeatedly throughout the 59 minute period in which the alarm output is "ON".

Alarm off input, Pin 26: momentarily connecting this input to V_{SS} resets the alarm. The alarm will become active again in 24 hours or at a new alarm setting. If it is desired to disable the alarm indefinitely, then Pin 26 should be tied permanently to V_{SS}.

Countdown timer output

The countdown timer (sleep control) output, Pin 27, can be used to turn "OFF" an external circuit after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode (table 2) and seting the desired time interval (table 3). The output then turns "ON" and only when the countdown timer reaches '00' minutes does the output revert to the "OFF" state. However, the output may be reset by momentarily connecting the Override Alarm input, Pin 24, to V_{SS}. The output circuit for Pin 27 is shown in figure 3.

Figure 3 **Alarm and countdown outputs**

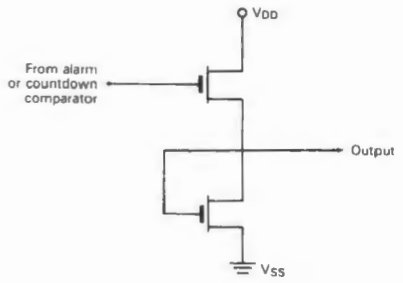


Table 2. **Display modes**

*Selected Display Mode	Digit No. 1	Digit No. 2	Digit No. 3	Digit No. 4
Time Display	10's of Hours & AM PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM PM	Hours	10's of Minutes	Minutes
Timer Display	Blanked	Blanked	10's of Minutes	Minutes

***If more than one display mode input is applied, the display priorities are in the order of Countdown Timer (overrides all others), Alarm, Seconds, Time (No other mode selected).**

Table 3. **Setting control functions**

Selected Display Mode	Control Input	Control Function
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 50 Hz Rate
	Both	Minutes Advance at 50 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 50 Hz Rate
	Both	Alarm Resets to 12:00 AM (12-hour format)
	Both	Alarm Resets to 0:00 (24-hour format)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (12-hour format)
	Both	Time Resets to 0:00:00 (24-hour format)
Timer	Slow	Subtracts Count at 2 Hz
	Fast	Subtracts Count at 50 Hz
	Both	Subtracts Count at 50 Hz

***When setting time, timer minutes will decrement at rate of time counter, until the 59 min timer counter reaches 00 minutes (59 min timer counter will nokt recycle).**

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Applications

Typical application for 12 and 24 hour mode operation is shown in figures 4 and 5. For preference, use individual LED's for AM and PM for clarity reasons; unused segments of 4th display may, however, be used. Central decimal point can be used instead of colon.

Ganged switching of Pins 23 and 30 (figure 5) is necessary to prevent erroneous readings. Connect pin 38 to V_{SS}. (The three individual LED's for AM, PM and colon are not used in 24 hour mode).

Figure 4 **12 hour mode**

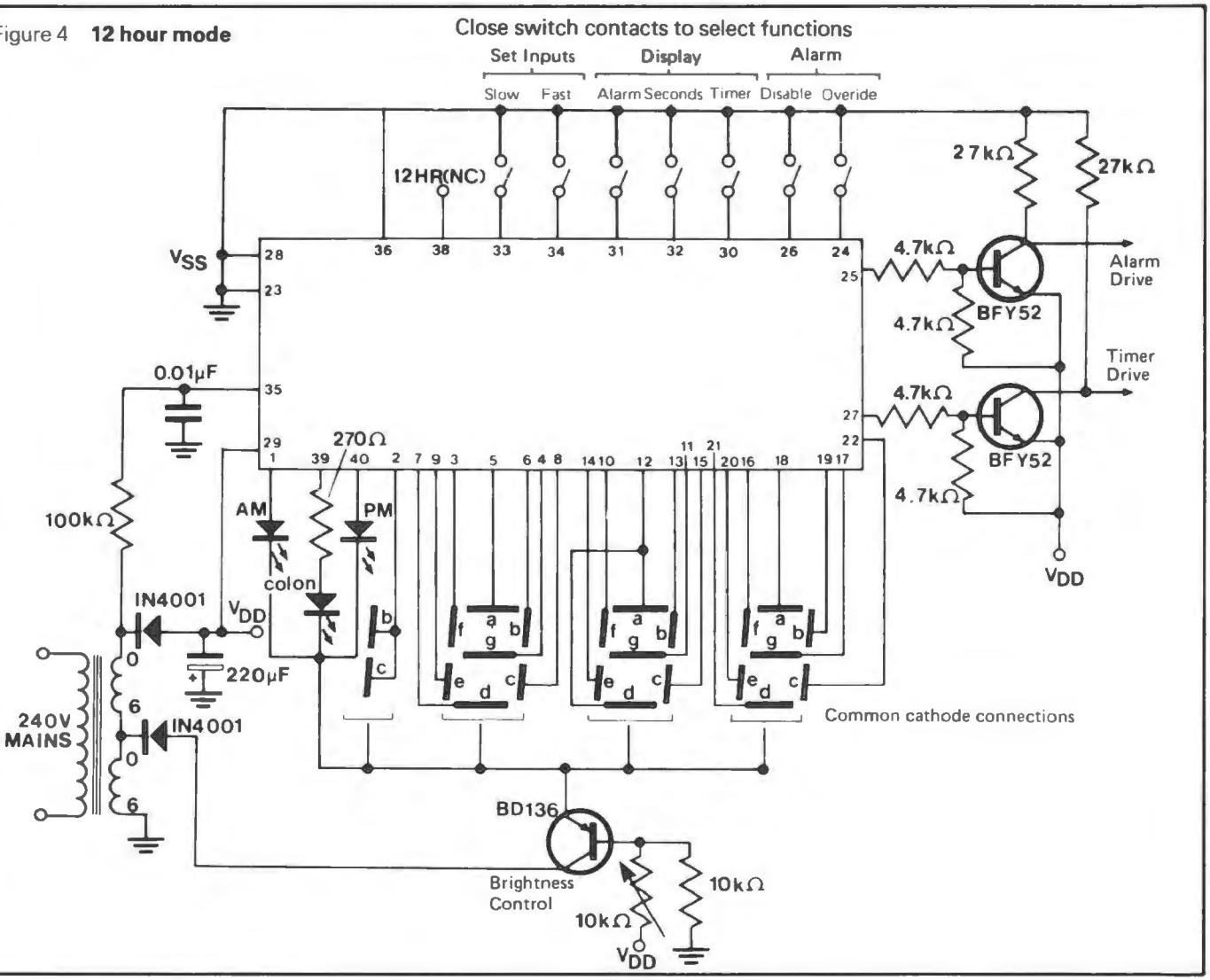
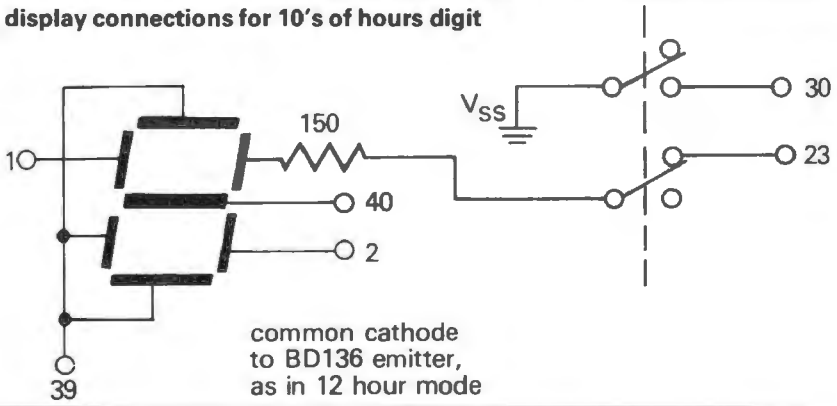


Figure 5 **24 hour mode: display connections for 10's of hours digit**



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RS data

DPM I.C's RS 7106, 7126, 7107

Stock numbers 307-862,303-652, 307-143

The RS digital panel meter i.c.'s incorporate all the analogue and digital active circuitry to enable 3½ digit panel meters with auto-polarity and auto-zero to be constructed. The devices also include display decoder/drivers, thus allowing direct interface with 7-segment common anode L.E.D. displays (7107) or a 3½ digit liquid crystal display (7106 & 7126).

The i.c.'s utilise the dual ramp principle which is a technique where the unknown input voltage is used to charge a capacitor for a fixed time. Then, with the unknown disconnected, a reference voltage is used to discharge the capacitor. The time taken to discharge the capacitor is a measure of the unknown voltage. To ensure that the charge and discharge are linear an integrator is used.

Figure 1 **Simplified schematic**

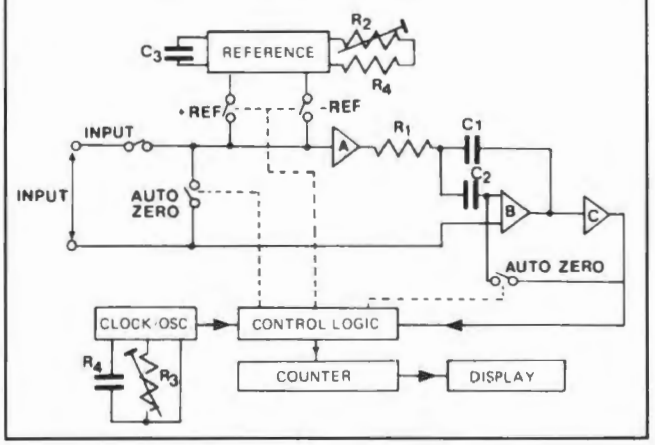


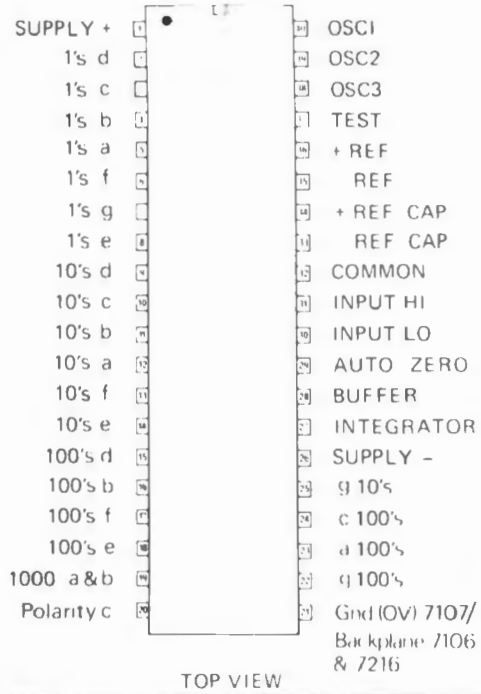
Table 1—Electronic switch positions

State / Switch	1	2	3
INPUT	Closed	Open	Open
+REF	Open	*	Open
−REF	Open	*	Open
AUTO-ZERO	Open	Open	Closed

*+ REF closed for − ve inputs − REF closed for + ve inputs

Initially the control logic sets the electronic switches as shown in table 1, in this mode the unknown input is applied to the integrator, comprising amplifier (B), R1 and C1, via buffer amplifier (A). The integrator output therefore ramps positively or negatively, depending on the input polarity, for a period set by the internal clock oscillator. At the end of this period, state 2 in table 1 is selected, here the input is disconnected and the positive or negative reference connected to the integrator which subsequently begins to ramp towards zero. The comparator (C) determines, during the initial ramp, which reference is selected and also detects that state of zero integrator output. During state 2 the counter

Figure 2 **Pin connections**



accumulates clock pulses until the integrator reaches zero, i.e. comparator (C) changes state. At this point state 3 is selected, here the accumulated count and polarity are displayed giving the unknown input value and the auto-zero mode is selected, this mode short circuits the input and connects capacitor C2 between the buffer amplifier (A) output and short circuited integrator and comparator. Auto-zero capacitor C2 thus charges to a value determined by the offsets appearing at the amplifier outputs and the period of the auto-zero mode; this timing is once again determined by the clock oscillator. Upon completion of auto-zero, state 1 is re-selected thus the whole cycle is repeated. However, the charge on the auto-zero capacitor C2 is subtracted or added to the input voltage thereby correcting any drift in circuit performance. In the event of an input not being applied the auto-zero mode maintains a zero reading by continuous compensation of amplifier drift.

3015

The frequency of the clock oscillator is independent of overall circuit accuracy, however, by selecting a clock frequency such that the initial ramp period is equivalent to or a multiple of the mains period maximum rejection of series mode interference is obtained (see "System Timing" section under Operating Modes).

Absolute maximum ratings

7106 and 7126

Supply voltage (V + to V –) 15V
Analogue input voltage (either input) (Note 1) ..... V + to V –
Reference input voltage (either input) ..... V + to V –
Clock input ..... Test to V +
Power dissipation (Note 2) 800mW
Operating temperature ..... 0°C to + 70°C
Storage temperature ..... – 65°C to + 160°C
Lead temperature (Soldering, 60 sec) ..... 300°C

7107

Supply voltage V + ... + 6V
V – ..... – 9V
Analogue input voltage (either input) (Note 1) ..... V + to V –
Reference input voltage (either input) ..... V + to V –
Clock input ..... Gnd to V +
Power dissipation (Note 2) 800mW
Operating temperature ..... 0°C to + 70°C
Storage temperature ..... – 65°C to + 160°C
Lead temperature (Soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Note 3: Unless otherwise noted specifications apply to both the 7106, 7126 and 7107 at T_A = 25°C, f_{clock} = 48 kHz, 7106 and 7126 are tested in the circuit of figure 10 using the 200mV version. The 7107 is tested using the 200mV version with external precision voltage reference as figure 9 and figure 3.

Note 4: Refer to "Differential Input" section under Operating Modes.

Note 5: Back plane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate.

Note 6: Does not include LED current for 7107.

Electrical characteristics (Note 3)

Characteristics	Conditions	Min	Typ	Max	Units
Zero input reading	V_{in} = 0.0V Full scale = 200.0 mV	–000.0	±000.0	+000.0	Digital Reading
Ratiometric reading	$V_{in} = V_{ref}$ V_{ref} = 100 mV	999	999/1000	1000	Digital Reading
Rollover error (Difference in reading for equal positive and negative reading near full scale)	$-V_{in} = +V_{in}$ = 200.0mV	– 1	±.2	+ 1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	– 1	±.2	+ 1	Counts
Common mode rejection ratio (Note 4)	V_{cm} = ±1V, V_{in} = 0V. Full scale = 200.0mV		50		μV/V
Noise (pk-Pk value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV		15		μV
Leakage current @ input	V_{in} = 0V		1	10	pA
Zero reading drift	V_{in} = 0 0°<T_A<70°C		0.2	1	μV/°C
Scale factor temperature /Coefficient	V_{in} = 199.0mV 0<T_A<70°C (Ext. Ref. Oppm/°C		1	5	ppm/°C
Supply current 7106 & 7107 7216	V_{in} = 0 (Note 6) V_{in} = 0		0.8 50	1.8 100	mA μA
Analogue common voltage (with respect to pos. supply)	25kΩ between common & pos. supply (7216 250K)	2.4	2.8	3.2	Volts
Temp. coeff. of analogue common (with respect to pos. Supply)	25kΩ between common & pos. supply (7216 250K)		80		ppm/°C
7106 and 7216 Pk-Pk segment drive voltage (Note 5)	V supply = 9V	4	5	6	Volts
7106 and 7216 Pk-Pk backplane drive voltage (Note 5)	V supply = 9V	4	5	6	Volts
7107 ONLY Segment sinking current (Except Pin 19)	+ supply = 5.0V Segment voltage = 3V	5	8.0		mA
7107 ONLY Segment sinking current (Pin 19 only)	+ supply = 5.0V Segment voltage = 3V	10	16		mA

Operating modes

Auto-zero

With the inputs shorted, the display should read zero. The negative sign being displayed about 50% of the time.

Differential input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Differential reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worse case condition. (See "Component Value Selection").

Analogue common

This pin is included primarily to set the common mode voltage for battery operation (7106 and 7126) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analogue common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

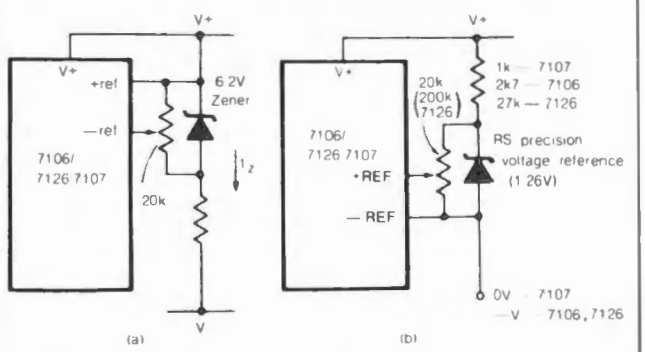
Over-range

Inputs greater than full scale will cause suppression of the three least significant digits, i.e. only 1 or −1 will be displayed.

Polarity

The absence of a polarity sign indicates a positive input reading. A negative input is indicated by a negative sign.

Figure 3 **Using an external reference.**



The limitations of the on-chip reference should also be recognised, however. With the 7107, the internal heating which results from the L.E.D. drivers can cause some degradation in performance. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80 μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106 and 7126 with negligible dissipation, suffer from none of these problems. In all cases, an external reference can easily be added, as shown in figure 3.

(N.B. When an external bandgap reference (1.26V) is used with the 7107, Input − (pin 30) is tied to Analogue common (pin 32) thus establishing the correct common mode voltage. If Analogue common is not shorted to Digital ground (pin 21), the input voltage may float with respect to the power supply if Analogue common is shorted to ground, the input is single ended (referred to supply ground).

Analogue common is also the voltage the input returns to during auto-zero and de-integrate. If signal low is different from analogue common, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications input low will be set at a fixed known voltage (power supply common for instance). In this application, analogue common should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analogue common, it should be since this removes the common mode voltage from the reference system.

(N.B. When using the internal reference analogue common must not be connected to 0_V or ground)

Within the i.c., analogue common is tied to an N channel FET that can sink 30mA (100μA 7126) or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA (1μA 7126) of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The test pin serves two functions. On the 7106 and 7126, it is coupled to the internally generated digital ground through a 500Ω resistor (digital ground is set at approximately 5V below +V). Thus, when operated from a single battery supply, test can be used as the 0v rail for externally generated segment drivers, such as decimal points (or any other presentation the user may want to include on the LCD display), or it may be used as a common mode reference level to ensure compatibility with most op amps. Figure 8 shows such an application.

When the 7106 is operated from a ±5V supply and external digital circuitry is required, the test pin should be connected to 0v. (N.B. the test function can only be implemented in this case by use of a S.P.D.T. switch). The second function is a "lamp test". When test is pulled high (to + supply) all segments will be turned on and the display should read −1888. Caution: on the 7106 and 7126, in the lamp-test mode, the segments have a constant d.c. voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.

System timing

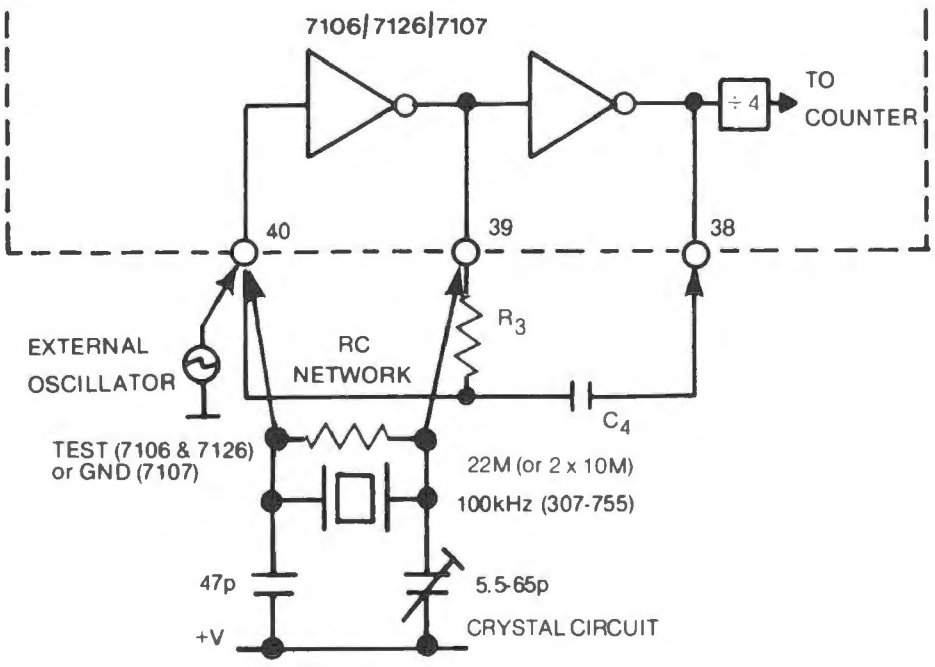
Figure 4 shows the clocking arrangements used in the 7106, 7126 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal circuit between pins 39 and 40.
3. An R.C. oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 50 Hz pickup, the signal integrate cycle should be a multiple of 20 ms. Oscillator frequencies of 200kHz, 100kHz, 66⅔ kHz, 50kHz, 40kHz etc would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Figure 4 **Clock circuits**



Component value selection

(7126 values shown in brackets).

Integrating resistor (R_1)

Both the buffer amplifier and the integrator have a class A output stage with 100μA (6μA) of quiescent current. They can supply 20μA (1μA) of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470k (IM8) is near optimum and similarly a 47k (180k) for a 200.0 mV scale.

Integrating capacitor (C_2)

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). When the analogue common is used as a reference, nominal ±2 volt full scale integrator swing is fine. For the 7107 with ±5 volt supplies and analogue common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings second (50kHz clock), nominal values for C_1 are 220n 7106, 100n 7107 and 47n 7126. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is to have low dielectric absorption to prevent roll-over errors. Polypropylene and polycarbonate capacitors are suitable for this application.

Auto-zero capacitor (C_2)

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise is very important, a 470n (330n) capacitor is recommended. On the 2 volt scale, a 47n (22n) capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference capacitor (C_3)

A 100n capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the reference low is not at analogue common) and a 200 mV scale is used, a larger value is required to prevent roll-over error. Generally 1μ will hold the roll-over error to 0.5 count in this instance.

Oscillator components (R_3 & C_4)

For all ranges of frequency a 100k (200k) resistor is recommended and the capacitor is selected from the equation $f = \frac{0.45}{R_3C_4}$). For 48kHz clock (3 readings/second), $C_4 \simeq$ 100p (50p).

Reference voltage

The analogue input required to generate full-scale output (2000 counts) is: $V_{in} = 2V_{ref}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{ref} should equal 100.0mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V_{ref} = 0.341V. Suitable values for integrating resistor and capacitor would be 120k and 220n 7106, 120k and 100n 7107, 330k and 47n 7126. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for Vin ≠ 0. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between input high and common and the variable (or fixed) offset voltage between common and input low.

7107 Power supplies

The 7107 is designed to work from ±5 volt supplies. (N.B. It is recommended to decouple the supplies with two 10μ capacitors).

However, if a negative supply is not available, it can be generated from the clock output as shown in figure 5.

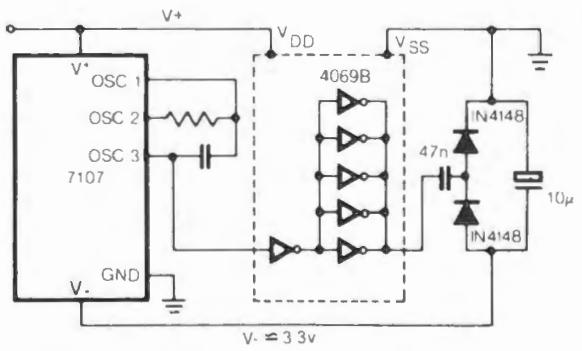
In fact, in selected applications no negative supply is required. The conditions to use a single + 5V supply are:

1. The input signal can be referenced to the centre of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

7106 and 7126 Supplies

The 7106 and 7126 may be operated from either a battery source, or from a mains system derived supply. The latter should be ±5V. The 0v may be connected to the test pin, if external circuitry is required, and also be used as a ground reference for the input. (See Test and Analogue sections).

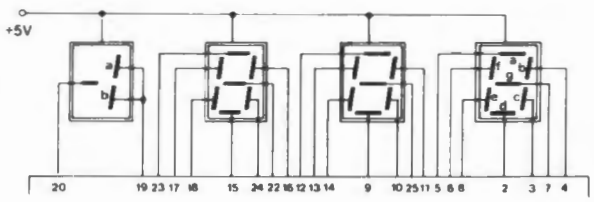
Figure 5 **Generating negative supply from + 5v**



Displays

7107: Common Anode to +5V
7106 and 7126 Backplane to Pin 21

Figure 6 **Display connections 7107**



Note 0.3 in. Common Anode L.E.D. displays are available for direct driving from the 7107 and 3½ digit L.C.D. displays for use with the 7106 and 7126. Please refer to current catalogue. (See figure 8 for method of driving L.C.D. decimal points).

Figure 7 **Display buffering for increased drive current. Requires four RS 7407 hex buffers. Each buffer is capable of 40 mA max.**

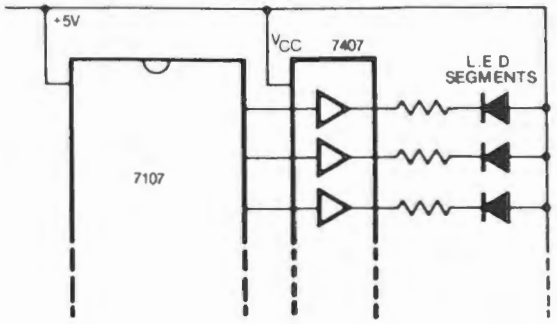
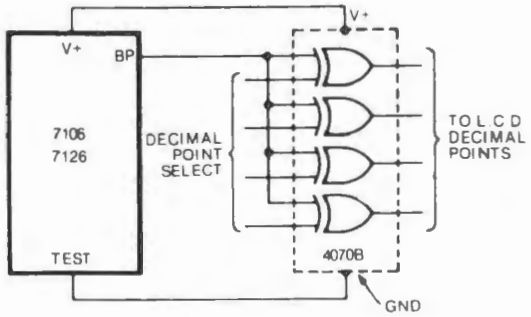


Figure 8 **Exclusive "OR" gate for decimal point drive of liquid crystal display. (See test function)**



External components

Figure 9 **7107 using the internal reference. INPUT — may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See "Analogue Common section under operating modes).**

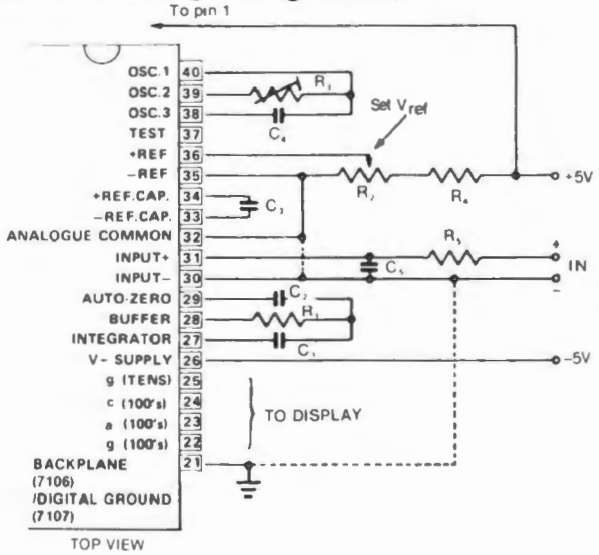
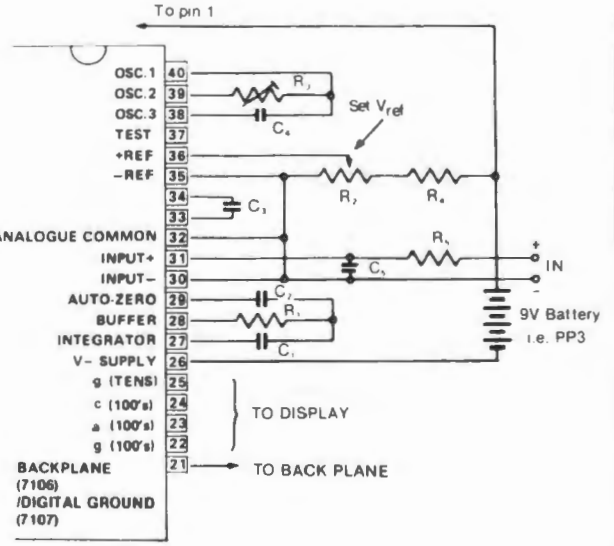


Figure 10 **7106/7126 using the internal reference and a floating supply voltage (9V battery).**



Component values

	7106 and 7107		7126	
	200 mV F.S.R.	2V F.S.R.	200 mV F.S.R.	2V F.S.R.
R_1	47K	470K	180K	IM8
R_2	1K	20K	10K	250K
R_3	100K preset	100K preset	200K	200K
R_4	22K	22K	240K	240K
R_5	1M	1M	1M	1M
C_1	220n 7106, 100n 7107	220n 7106, 100n 7107	47n	47n
C_2	470n	47n	330n	22n
C_3	100n	100n	100n	100n
C_4	100p	100p	50p	50p
C_5	10n	10n	10n	10n

Use 2% 0.5W metal oxide resistors and cermet presets. Capacitors should ideally be 160V polyarbonate except C_4 which should be silvered mica.

Input filters

Due to the extremely low input leakage current, typically 1pA at 25°C, the errors caused by high impedance passive filters on the input are minimal. The simple R.C. filter consisting of R5(IM) and C5(10n) introduces a negligible 1μV error.

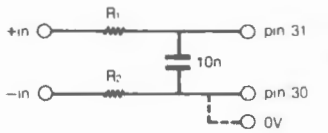
Input protection

As stated in note 1 in the maximum ratings section, the input voltage may exceed the supply voltages providing that the input current to the IC is limited to ±100μA. If the D.V.M. IC is used in the single ended input mode, the 1M ohm input filter resistor is sufficient to give protection up to at least ±100V. If the device is to be used in the differential input mode the 1M ohm resistor in the non-inverting input line should be changed to 470K and another 470K added to the inverting input line, this will then give protection to at least ±100V as before. In some cases an input attenuator, if used, may form part of the input protection.

A.C. Voltage measurements

Measuring A.C. voltages requires the voltage to be first rectified before applying to the D.P.M. To achieve this a precision rectifier is used as shown in figure 12. Here the use of an operational amplifier gives a D.C. voltage proportional to the R.M.S. value of the A.C. input. This is only true for sinewaves as any harmonic content will introduce significant errors.
Apply the output to the D.P.M. differential inputs pins 30 and 31.

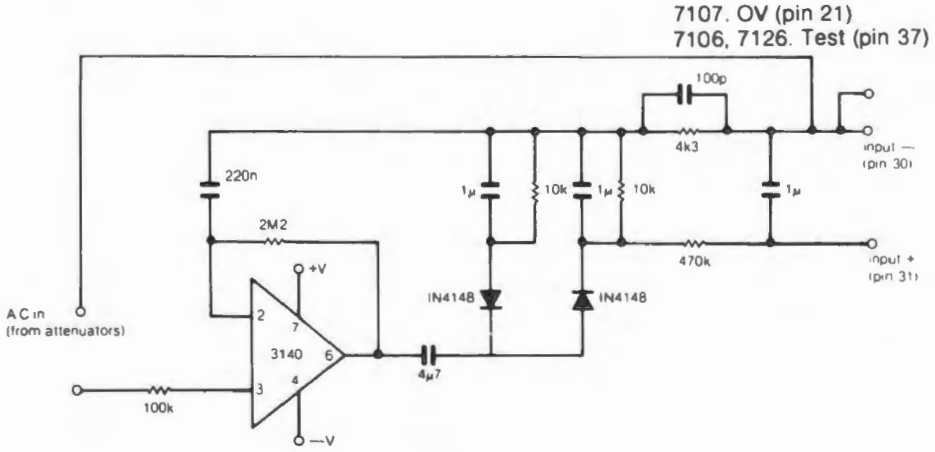
Figure 11 **Input protection**



	Single ended input*	Differential input
R_1	1M	470k
R_2	0	470k

*−in (pin 30) connected to 0V

Figure 12 **A.C. Rectifier**



N.B. DPM 200mV range.
Analogue common not connected to input−
Test decoupled to supplies by 10μF capacitors

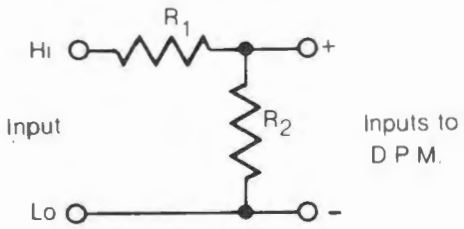
RS data

Input attenuators

When it is required to measure voltages in excess of the maximum, i.e. 2V F.S.D. the input voltage must first be attenuated. In this instance a reduction in input resistance should be expected.

To maintain a reasonably constant attenuation, without serious loss in reading accuracy due to loading effects, the attenuator input resistance is usually selected to lie between 1M and 10M. Figure 13 shows the method of calculating resistor values and figure 14 gives suggested component values.

Figure 13 **Input attenuators**

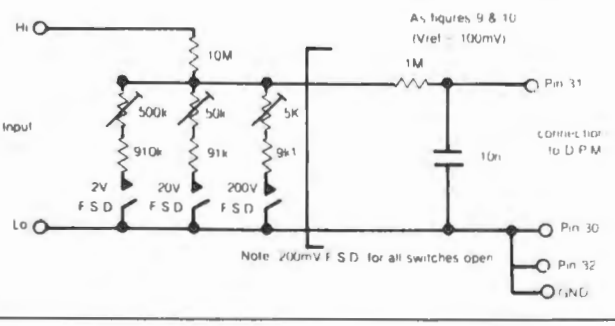


$\frac{R2}{R1 + R2}$ = Attenuation ratio

for 10.1	for 100:1	for 1000:1
$R2 = \frac{R1}{9}$	$R2 = \frac{R1}{99}$	$R2 = \frac{R1}{999}$

Input resistance = $R_1 + R_2$

Figure 14 **Input attenuation – suggested values**



Current measurements

Measurement of A.C. or D.C. current can be achieved by measuring the voltage drop across a known resistor which is placed in series with the circuit under test. Depending on the range selected, i.e. 200mV or 2V the voltage drop across the resistor can be determined by Ohms law:

V drop = I.R. where R = known resistor value
I = current to be measured
V drop = subsequent voltage drop

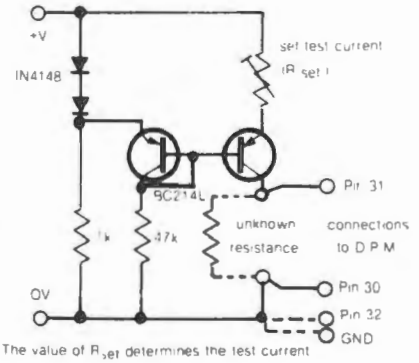
Take care not to exceed the power dissipation of the resistor.

Resistance measurements

To measure the unknown value of a resistor a defined current is passed through the resistor and the resultant potential difference is measured. The current is obtained from a constant current source. A typical circuit to achieve this is shown in figure 15. The approximate values of Rset are shown in the table.

Figure 15 **Resistance converter — set D.P.M. to 2V (F.S.D.) (For use with dual rail supplies)**

I test	R_{set}	Meter F S D
10mA	200R	200R
1mA	2k	2k
100µA	20k	20k
10µA	200k	200k



The value of R_{set} determines the test current

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RS data

Voltage to frequency and frequency to voltage converter

Stock number 307-070

The RS voltage to frequency converter combines both bipolar and C-Mos technology on a single chip. The converter accepts a variable analog input signal and generates an output pulse train whose frequency is linearly proportional to the input voltage. The device may also be used as a highly accurate Frequency to Voltage converter, accepting virtually any input frequency and providing a linearly proportional voltage output. In addition the device operates on single or split supply voltages.

V/F applications

- Temperature sensing and control
- μP data acquisition
- Instrumentation
- 13 bit A/D converters
- Digital panel meters
- Analogue data transmission and recording
- Transducer encoding

F/V applications

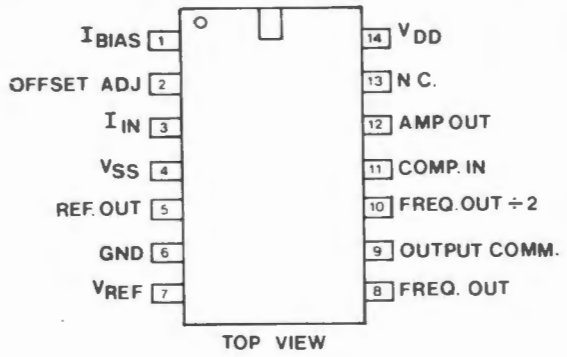
- Frequency meters/tachometers
- Speedometers
- Analogue data transmission and recording
- Motor control
- F.M. demodulation
- Frequency multiplier/divider
- Flow measurement and control

Electrical characteristics

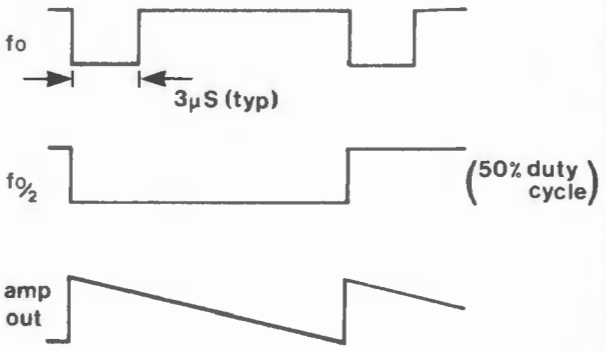
V_{DD} = 5V, V_{SS} = V_{ref} = –5V, R_{bias} = 100kΩ, T_A = 25°C, Full scale 10kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Conversion accuracy					
Linearity (10kHz)		–	0.01	0.05	% FS
Linearity (100kHz)		–	0.1	0.25	% FS
Gain drift	0°C to 70°C	–	±25	±40	ppm/°C FS
Supply rejection	Vss ±1V, V_{DD} ±1V	–	0.025	0.1	%/V
Gain variance		–	±10	–	% of nom
Input amplifier					
Offset voltage	I_{IN} = 0, 0°C to 70°C	–	±10	±50	mV
Offset voltage drift	0°C to 70°C	–	±25	±50	μV/°C
I_{IN} full scale		–	10 μA	–	μA
I_{IN} over range		–	–	50	μA
Logic outputs					
V_{SAT}	I_o = 10 mA (Sink)	–	–	0.4	V
V_{OUT} max to V_{out} common	I_o = 10μA	–	–	18.0	V
V_{out}		V_{SS}	–	V_{DD} – 1	V
Supply					
I_{DD} (Quiescent)	V_{IN} = –0.1V	–	2.0	4.0	mA
I_{SS} (Quiescent)	V_{IN} = –0.1V	–	–1.5	–4.0	mA
V_{DD}		4.0	–	7.5	V
V_{SS}		–4.0	–	–7.5	V
Reference					
Vref – Vss		–1.0	–	+1.0	V
Response time					
Settling time to 0.01% FS		–	–	2	Cycles

Figure 1 **Pin layout**



Output waveforms



Absolute maximum ratings

$V_{DD} - V_{SS}$	18 volts
I_{in}	±10mA
I_{ref}	±10mA
Vo max – Vo com	18 volts
V_{ref} to V_{SS}	1.5 volts
Operating temperature	0°C to +70°C
Maximum dissipation	500mW

Figure 2 shows the schematic for Voltage to Frequency conversion to which the following formulae may be applied:

$$f_{out} = \frac{V_{in}}{R_{in}} \times \frac{1}{V_{ref} \times C_{ref}}$$

$$R_{in} = \frac{V_{in}\,max}{10} \quad M\Omega$$

$$82k\Omega \leq R_{bias} \leq 120k\Omega$$

$$3C_{ref} \leq C_{int} \leq 5C_{ref}$$

For optimum stability: $C_{int} \geq 4\,C_{ref}$

Circuit adjustments

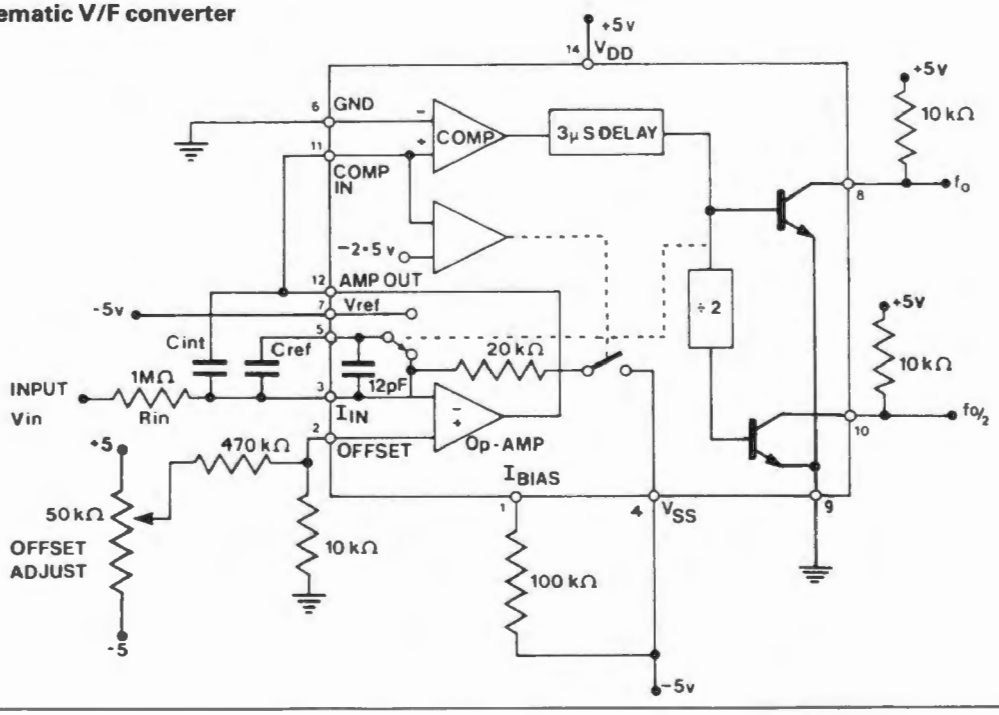
1. To set f_{min}, set V_{in} = 10mV and adjust the 50kΩ OFFSET ADJUST for 10Hz output.
2. To set f_{max} set V_{in} = 10V and adjust R_{IN} or V_{ref} for 10kHz output.
3. Refer to Table 1 for 100kHz operation.
4. For best performance use high stability components for R_{IN}, C_{int} and C_{ref} (Metal oxide resistors and polystyrene or silvered mica capacitors.) Also separate the output ground (Pin 9) from the input ground (Pin 6).

Table 1 Typical values

f_{max} (kHz)	10	100
C_{int} (pF)	600*	82
C_{ref} (pF)	150	22
R_{in}	1MΩ	

*Use 560 pF and 39 pF in parallel.

Figure 2 **Schematic V/F converter**



Fixed supply voltage

Figure 3 shows the external component connections when the device is operated on a fixed voltage single supply rail. Table 2 gives the value of R1 and R2 for various supply voltages.

Figure 3 **Single supply V/F converter**

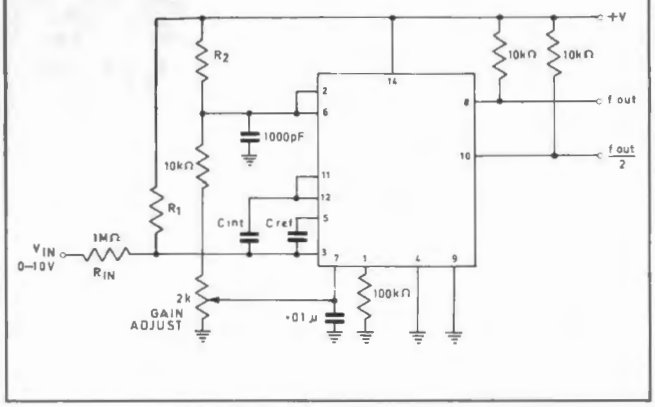


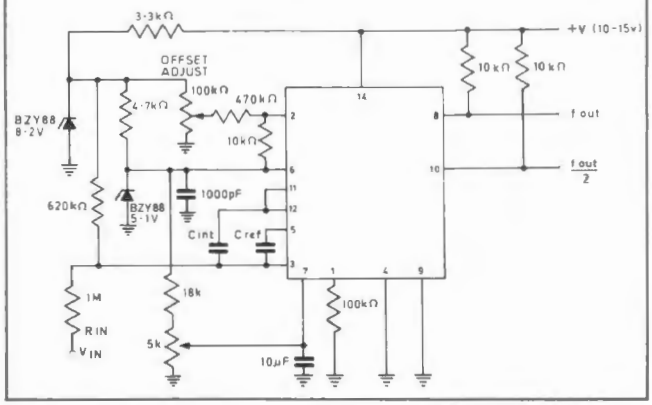
Table 2

V_s	R_1	R_2
10	1MΩ	10kΩ
12	1.5MΩ	15kΩ
15	3.3MΩ	22kΩ

Variable supply with offset adjust and gain adjust

For operation from a variable supply, i.e. battery operation the circuit shown in Figure 4 should be used. The OFFSET ADJUST control operates in a similar manner to that described for Figure 2.

Figure 4 **Variable supply voltage (e.g. a battery)**



Frequency to voltage conversion

The schematic for Frequency to Voltage (F/V) operation is shown in Figure 8 (see page 4). The following equations and performance data refer to this mode of operation:

Input

Frequency:	10Hz to 100kHz
Voltage:	min –0.4, +0.4 max –2, $+V_{DD}$
Waveform:	Sine, Triangular, Square or Pulse
Duty cycle:	0.5 μs min negative pulse width 5.0 μs min positive pulse width
Impedance:	10MΩ (FET Input)

Output

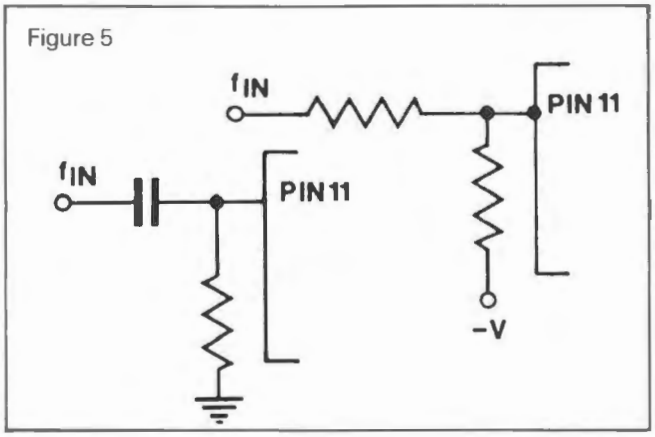
V_{out} range:	0 to 4V (V_{DD} –1)
V_{out}:	f_{IN} (V_{ref} $C_{ref}R_{int}$)
Response time:	R_{int} x C_{int}
Ripple:	Inversely proportional to f_{IN} and C_{int}

Overall accuracy: Better than 0.1% Full Scale.

Input signal conditioning

1. If only a unipolar input signal (f_{IN}) is available it is recommended that either an offset circuit using resistors be used or that the signal be coupled in via a capacitor (refer to Figure 5).

Figure 5



The output voltage of the Op-Amp is referenced to Pin 6 (GND). Therefore if Pin 6 is used to determine the comparator threshold the Op-Amp output reference will also be shifted.

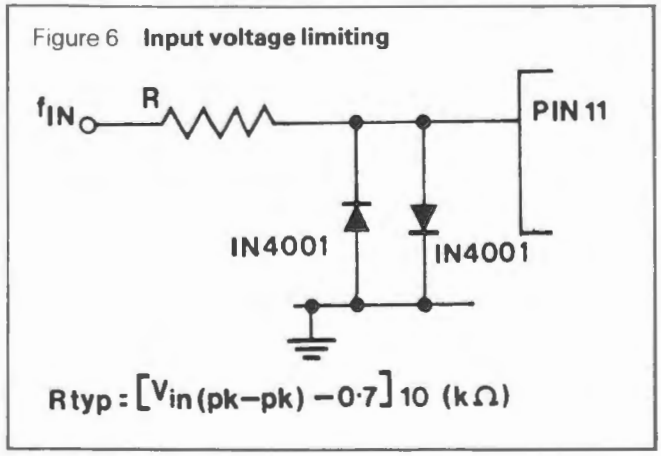
2. For 100kHz max input R_{int} should be decreased to 100kΩ.

3. fo and $fo/_2$ are not used in the F/V mode. However, these outputs may be useful in some applications, such as a buffer to feed additional circuitry. fo will then follow the input frequency waveform: except that fo will go high 3μS after f_{IN} goes high. $fo/_2$ will be square wave with a frequency of one half fo.

4. The input signal must cross zero in order to trip the comparator; if it does not refer to Note 1 above. In order to overcome hysteresis the amplitude must be greater than ±200mV. If the input voltage exceeds –2.5V then the OpAmp output will go to its maximum voltage in a latch-up condition. To overcome this one may incorporate a pair of back to back diodes and series resistor to limit the voltage to ± 0.7V. Refer to Figure 6.

5. At power up it is essential that the input signal is set at a level above zero, failure to comply may result in a latch-up condition.

Figure 6 **Input voltage limiting**



RS data

Single supply F/V conversion

1. The circuit shown in Figure 7 operates from a single supply rail. The input is now referenced to 5.1V (Pin 6). The input signal must therefore be restricted to be greater than 3 volts (Pin 6 minus 2 volts) and less than V_{DD}.
2. If the signal is A.C. coupled then a resistor (100k to 10M) must be placed between the input (Pin 11) and Pin 6 as indicated in Figure 7.
3. The output will now be referenced to Pin 6 which is at 5.1V. For frequency meter applications a 1mA meter with a series scaling resistor can be placed across Pin 6 and 12.

Figure 7 **Single supply F/V converter**

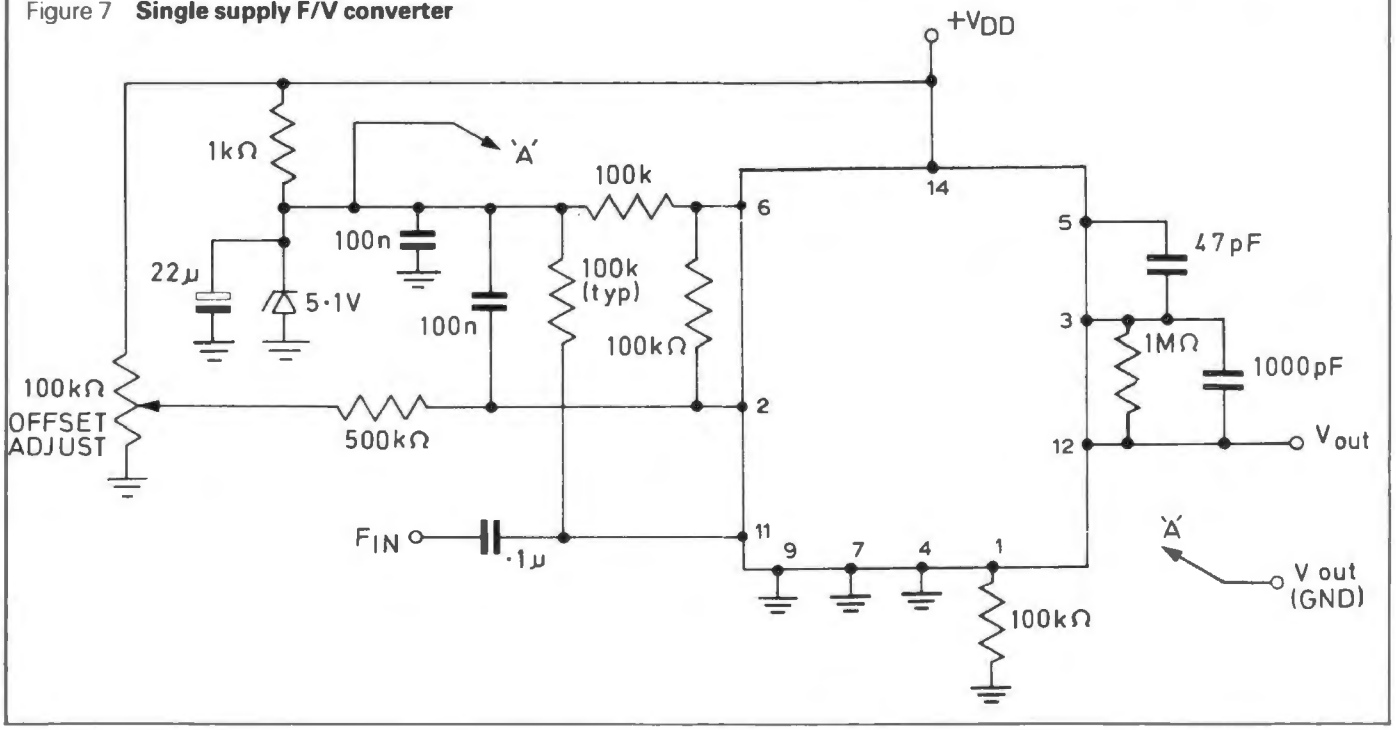
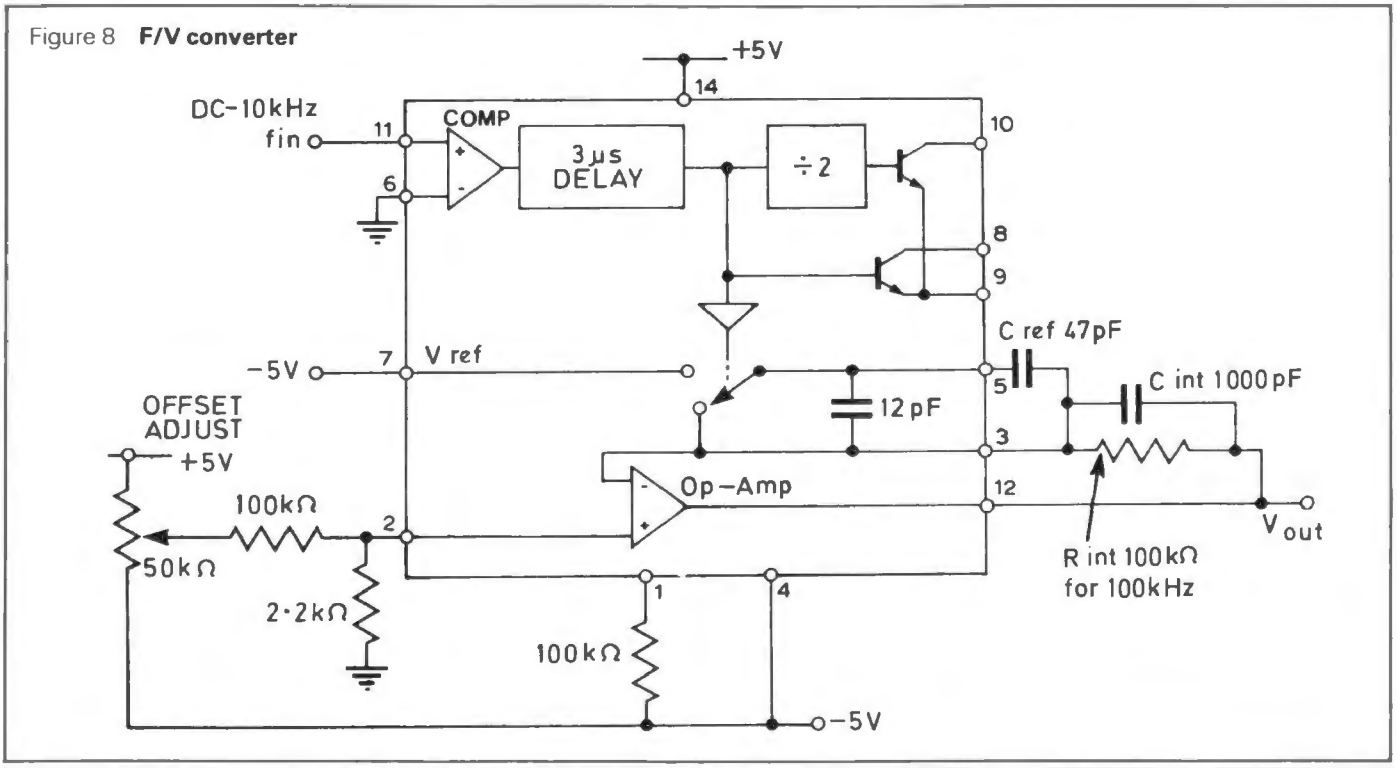


Figure 8 **F/V converter**



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RS data

Type K thermocouples and accessories

General specification for nickel chromium/ nickel aluminium thermocouples (Type K)

Wire identification

Brown sleeve (positive): Nickel chromium
Blue sleeve (negative): Nickel aluminium

Tolerance

±3°C in the range 0°C, to +400°C ±0.75% in the range +400°C to +1000°C.

Sensitivity

40μV per °C over the range 0°C to +1000°C. Temperatures below 0°C must be calibrated as required. For measurements below 0°C British Standards recommend a calibration at the boiling point of Oxygen (–183°C at S.T.P.).

Voltage reference complies with BS4937, Part 4; March 1973. Materials comply with BS1041, Part 4; 1966.

Type K thermocouple products

Wire	151-192
Probe	151-186
Surface probe	158-395
Air temperature probe	158-525
Temperature controller relay	348-144
Digital temperature indicator (type K)	258-108
Digital temperature indicator (type K, T and J)	258-192
Selector switch	332-969
Connector	467-829
Extension wire	151-209
Thermocouple amplifier AD595AD	301-779

Thermocouple 151-192

Features

- Thermocouple junction welded in Argon, resists oxidation
- 400°C maximum working temperature
- Small welded junction minimises thermal heat sinking and provides fast thermal response
- Fibre glass insulation

Specification

Dimensions

Thermocouple wire	1/0.315mm
Overall length	2 metres (min)
Insulation diameter	1.5mm

Materials

Thermocouple wire	Nickel chromium/ Nickel aluminium
Insulation	Fibre glass
Working temperature range	–50°C to +400°C

Thermocouple probe 151-186

Features

- Stainless steel sheath
- Thermocouple electrically insulated from the sheath
- Probe may be bent (only once)
- 250°C maximum working temperature
- Small contact surface area minimises heat sinking effect

Specification

Dimensions

Thermocouple wire	7/0.2mm
Sheath	152mm long, dia. 3.2mm
Handle	90mm long, dia. 10mm
Sleeve	2 metres (min) long, dia. 3mm

Materials

Thermocouple wire	Nickel chromium/ Nickel aluminium
Sheath	Stainless steel (18.8)
Handle	Hardwood (sleeved in PVC)
Sleeve wire insulation	PTFE, overall insulation PVC

Electrical

Probe temperature range	–200°C to +250°C
Minimum insulation resistance between wire and sheath	$>10^4$MΩ
Voltage proof	1000Vd.c.

Thermocouple surface probe 158-395

Features

- Stainless steel, splayed tripod end
- Thermocouple is attached to a thin 4mm dia metallic disc which is sprung to ensure constant pressure during measurements. The sprung action also reduces the risk of damage to the tip should excessive forces be applied in use
- Maximum permissible temperature of tip +750°C
- Insulated handle
  Note. Tip is not isolated from the thermocouple junction

Specification

Dimensions

Thermocouple wire	7/0.2mm dia
Sheath length	92mm
Sheath diameter	5mm widening to 7mm at tripod end
Handle length	104mm
Sleeve length	approx. 1m

Materials

Thermocouple wire	Nickel chromium/ Nickel aluminium
Sheath	Stainless steel
Handle	Nylon grade 6.6

Electrical

Probe temperature range	−100°C to +750°C

Thermocouple air temperature probe 158-525

Features

- Stainless steel sheath
- 750°C maximum working temperature
- Thermocouple electrically insulated from sheath

Specification

Dimensions

Sheath	90mm long, dia 5mm
Handle	76mm long, dia 13mm
Lead length	1m

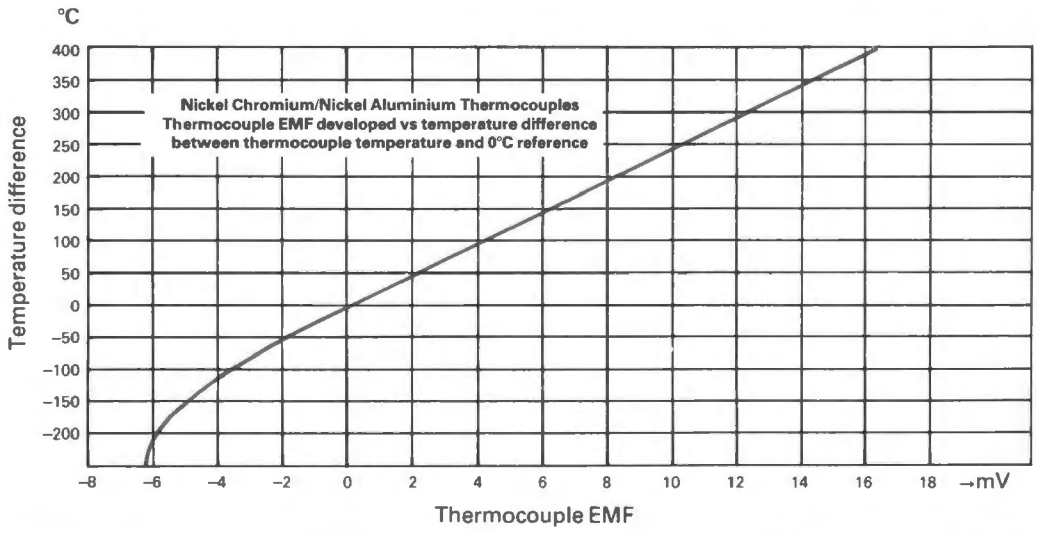
Materials

Thermocouple wire	Nickel chromium/ Nickel aluminium
Sheath	Stainless steel
Handle	Nylon grade 6.6

Electrical

Probe temperature range	−100°C to +750°C

Figure 1 **Typical temperature gradient for type K thermocouples**



Temperature controller relay 348-144

Features

- Panel or chassis mounting (via 11 pin base)
- Supply and status indication
- Failsafe protection
- 48 x 48 DIN standard case
- 110V or 240V a.c. operation

Specification

Supply voltage	110V a.c. or 240V a.c. 50Hz ± 10%
Power consumption	Less than 4VA
Scale range	0°C to 400°C
Scale calibration	1% of FSD at 25°C amb.
Repeatability of set point	0.5% of FSD at 25°C amb.
Set point hysteresis	±2% of FSD
Cold junction compensation	±0.2°C/°C
Ambient temperature range	−10°C to +50°C
Output relay contact (SPDT) rated	240V a.c. 5A resistive
Input sensor	NiCr/NiAl (BS4937-K)

Panel mounting digital temperature indicator 258-108

Features

- Automatic cold junction compensation
- Built in linearity circuit
- ±1°C resolution
- −25°C to +999°C temperature range

Specification

Supply voltage	5 to 8V d.c. 150mA max
Ambient temperature range	+5°C to +45°C
Input range	NiCr/NiAl (BS4937-K)
Temperature range	−25°C to +999°C
Resolution	±1°C
Accuracy at 25°C Note: this does not include sensor errors	±3% ±1 digit
Input impedance	30MΩ typical
Display type	0.3in 7-segment LED

Panel mounting digital temperature indicator 258-186

Features

- Suitable for types K, T and J thermocouples
- Automatic cold junction compensation
- 1°C resolution
- 11.2mm 3½ digit LED display

Specification

Supply voltage	115V a.c. or 240V a.c. or 8-15V a.c. or 8-15V d.c.
Ambient temperature range	0 to +50°C
Input sensor	Internally switchable K, T or J
Temperature range	Type K – 50°C to +1000°C Type T – 100°C to +325°C Type J – 25°C to +625°C
Resolution	1°C
Accuracy at 25°C	0.3%
Note: this does not include sensor errors	
Input impedance	30MΩ typical
Display type	11.2mm 7-segment LED

12-way selector switch

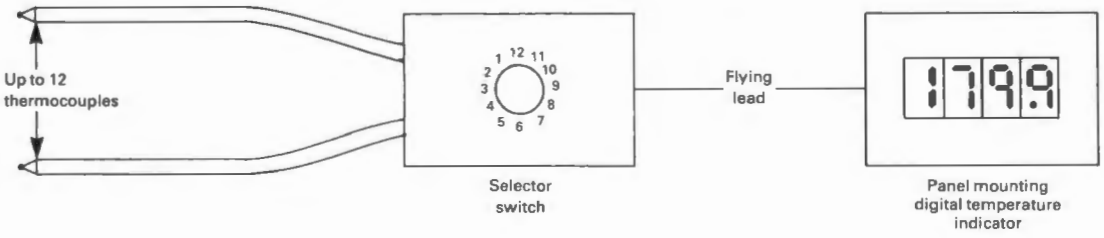
Features

- Allows one of up to 12 thermocouples to be selected
- Gold plated contacts
- Standard 90 x 42 DIN size panel mounting
- Connections via terminal strip
- Complete with 1 m of compensating cable and terminals

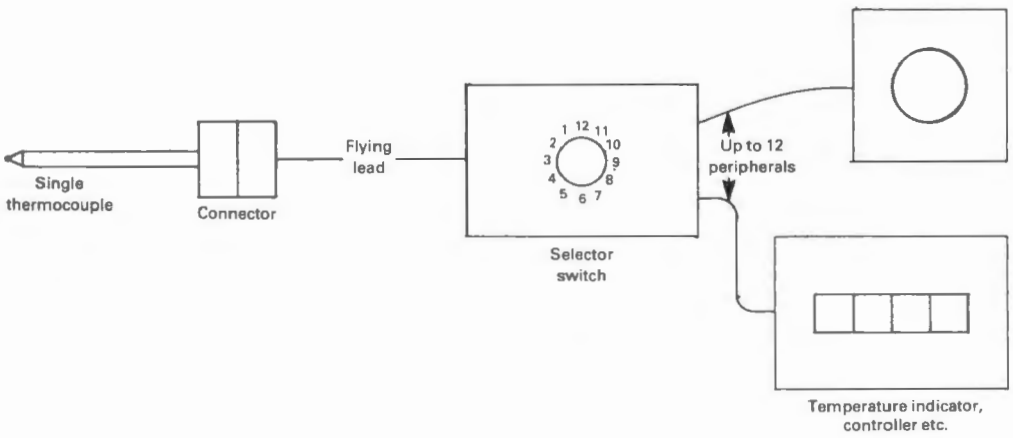
Typical applications

Figure 2 **Typical interconnections**

2a 12 to 1 configuration



2b 1 to 12 configuration

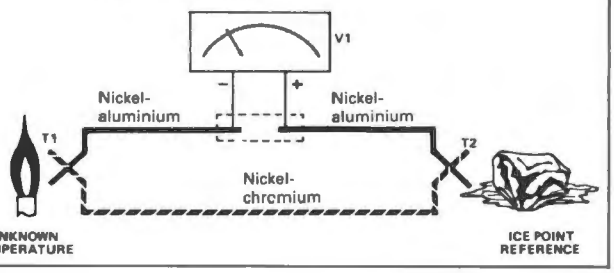


Thermocouple basics

Thermocouples are economical and rugged; they have reasonably good long-term stability. Because of their small size, they respond quickly and are good choices where fast response is important. They function over temperature ranges from cryogenics to jet-engine exhaust and have reasonable linearity and accuracy.

Because the number of free electrons in a piece of metal depends on both temperature and composition of the metal, two pieces of dissimilar metal in isothermal contact will exhibit a potential difference that is a repeatable function of temperature, as shown in Figure 3. The resulting voltage depends on the temperatures, T1 and T2, in a repeatable way.

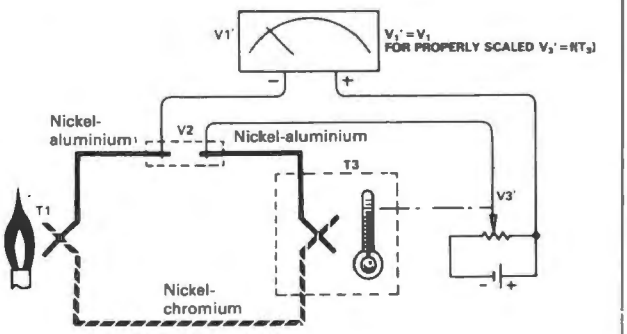
Figure 3 **Thermocouple voltage with 0°C reference**



Since the thermocouple is basically a differential rather than absolute measuring device, a known reference temperature is required for one of the junctions if the temperature of the other is to be inferred from the output voltage. Thermocouples made of specially selected materials have been exhaustively characterized in terms of voltage versus temperature compared to primary temperature standards. Most notably the water-ice point of 0°C is used for tables of standard thermocouple performance.

An alternative measurement technique, illustrated in Figure 4, is used in most practical applications where accuracy requirements do not warrant maintenance of primary standards. The reference junction temperature is allowed to change with the environment of the measurement system, but it is carefully measured by some type of absolute thermometer. A measurement of the thermocouple voltage combined with a knowledge of the reference temperature can be used to calculate the measurement junction temperature. Usual practice, however, is to use a convenient thermoelectric method to measure the reference temperature and to arrange its output voltage so that it corresponds to a thermocouple referred to 0°C. This voltage is simply added to the thermocouple voltage and the sum then corresponds to the standard voltage tabulated for an ice-point referenced thermocouple.

Figure 4 **Substitution of measured reference temperature for ice point reference**



Typical temperature measurement circuit

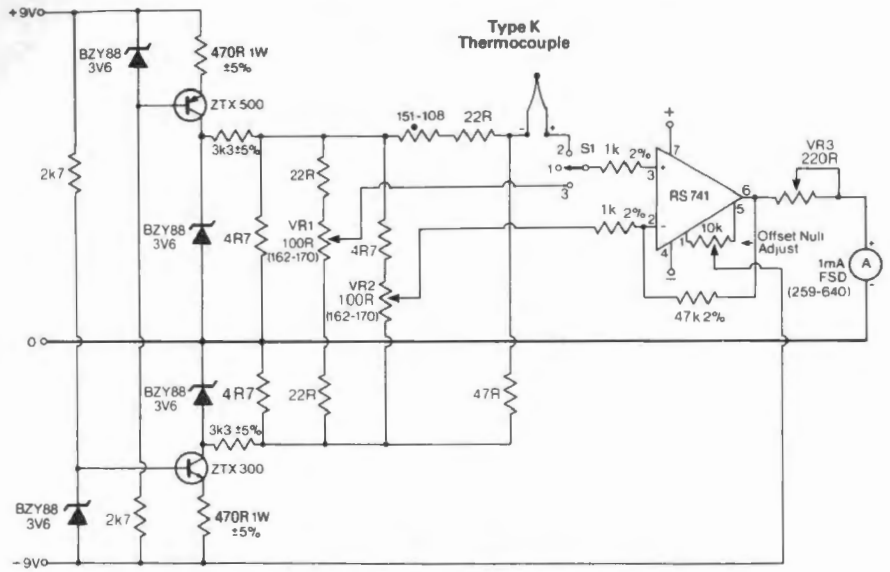
The circuit shown in Figure 5 may be used in conjunction with our thermocouples to measure temperature in the range 0 to 100°C.

The supply rails need to be delivered from a low noise supply (eg. Two PP3 batteries).

Setting up procedure

1. Adjust the value of VR3 to approximately 80ohm.
2. Set S1 to position 1 and with the amplifier inputs shorted together and connected to zero volt rail, adjust offset null so that meter reads zero.
3. Switch S1 to position 2 adjust VR2 so that meter reads ambient temperature on 0-10 scale (eg. with thermocouple junction at T_{amb} = 22°C pointer on meter scale reads 2.2, where 1 minor div = 2°C).
4. Switch S1 to position 3 and adjust VR1 so that meter reads zero.
5. Switch S1 back to position 2 and increase thermocouple junction temperature at 100°C. Adjust VR3 so that meter reads full scale ie. 100 divisions.
6. Some light readjustment of VR2 and VR3 may be necessary with thermocouple junction at ambient temperature and 100°C so that scale reading is linear. During this final adjustment ensure that meter reads zero with S1 in position 3 by adjusting VR1. (VR1 is now permanently set as a zero reference.)
7. During use the circuit may be occasionally readjusted for zero reference by switching S1 to position 3 and adjusting VR1.

Figure 5 **Measurement circuit**



All resistors are ½ watt ± 10% tol. unless otherwise stated.

Thermocouple amplifier (301-779)

The AD595AD is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone Celsius transducer with a low-impedance voltage output.

The AD595AD includes a thermocouple failure alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.

The AD595AD can be powered from a single ended supply (including +5V) and by including a negative supply temperatures below 0°C can be measured. To minimise self-heating, an unloaded AD595AD will typically operate with a total supply current of 160μA, but is also capable of delivering in excess of ±5mA to a load.

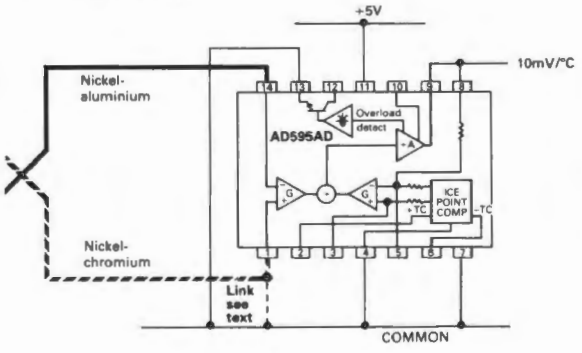
The AD595AD is laser trimmed for type K (nickel-aluminium and nickel-chromium) inputs. The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of two or three resistors.

Single and dual supply connections

The AD595AD is a completely self-contained thermocouple conditioner. Using a single +5V supply the interconnections shown in Figure 6 will provide a direct output from a type K thermocouple measuring from 0 to +300°C.

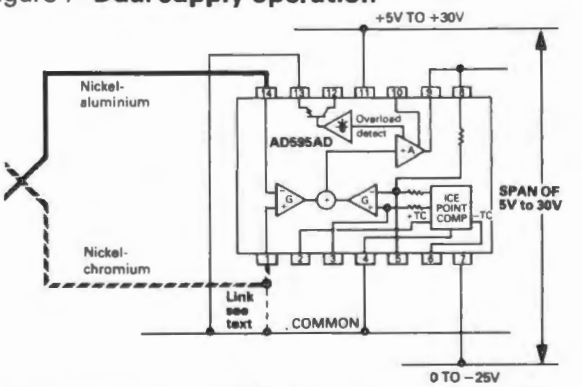
Any convenient supply voltage from +5V to +30V may be used, with self-heating errors being minimised at lower supply levels. In the single supply configuration the +5V supply connects to pin 11 with the V– connection at pin 7 strapped to power and signal common at pin 4. The thermocouple wire inputs connect to pins 1 and 14 either directly from the measuring point or through intervening connections of similar thermocouple wire type. When the alarm output at pin 13 is not used it should be connected to common or –V. The precalibrated feedback network at pin 8 is tied to the output at pin 9 to provide a 10mV/°C nominal temperature transfer characteristic.

Figure 6 **Basic connection, single supply operation**



By using a wider ranging dual supply, as shown in Figure 7 the AD595AD can be interfaced to thermocouples measuring both negative and extended positive temperatures.

Figure 7 **Dual supply operation**



With a negative supply the output can indicate negative temperatures and drive grounded loads or loads returned to positive voltages. Increasing the positive supply from 5V to 15V extends the output voltage range well beyond the +1100°C temperature limit recommended for type K thermocouples.

The common-mode voltage on the thermocouple inputs must remain within the common-mode range of the AD595AD, and a return path provided for the bias currents. **If the thermocouple is not remotely grounded, then the dotted line connection in Figures 6 and 7 must be made.**

A low value resistor may be needed in this connection to ensure that common mode voltages induced in the thermocouple loop are not converted to normal mode.

For comprehensive information on the AD595AD thermocouple amplifier please refer to Data Sheet 5055.

Type K thermocouple reference table

(with reference junctions at 0°C).

Deg. C.	0	1	2	3	4	5	6	7	8	9
				THERMOELECTRIC VOLTAGE IN ABSOLUTE MICROVOLTS						
−270	−6458									
−260	−6441	−6444	−6446	−6448	−6450	−6452	−6453	−6455	−6456	−6457
−250	−6404	−6408	−6413	−6417	−6421	−6425	−6429	−6432	−6435	−6438
−240	−6344	−6351	−6358	−6364	−6371	−6377	−6382	−6388	−6394	−6399
−230	−6262	−6271	−6280	−6289	−6297	−6306	−6314	−6322	−6329	−6337
−220	−6158	−6170	−6181	−6192	−6202	−6213	−6223	−6233	−6243	−6253
−210	−6035	−6048	−6061	−6074	−6087	−6099	−6111	−6123	−6135	−6147
−200	−5891	−5907	−5922	−5936	−5951	−5965	−5980	−5994	−6007	−6021
−190	−5730	−5747	−5763	−5780	−5796	−5813	−5829	−5845	−5860	−5876
−180	−5550	−5569	−5587	−5606	−5624	−5642	−5660	−5678	−5695	−5712
−170	−5354	−5374	−5394	−5414	−5434	−5454	−5474	−5493	−5512	−5531
−160	−5141	−5163	−5185	−5207	−5228	−5249	−5271	−5292	−5313	−5333
−150	−4912	−4936	−4959	−4983	−5006	−5029	−5051	−5074	−5097	−5119
−140	−4669	−4694	−4719	−4743	−4768	−4792	−4817	−4841	−4865	−4889
−130	−4410	−4437	−4463	−4489	−4515	−4541	−4567	−4593	−4618	−4644
−120	−4138	−4166	−4193	−4221	−4248	−4276	−4303	−4330	−4357	−4384
−110	−3852	−3881	−3910	−3939	−3968	−3997	−4025	−4053	−4082	−4110
−100	−3553	−3584	−3614	−3644	−3674	−3704	−3734	−3764	−3793	−3823
−90	−3242	−3274	−3305	−3337	−3368	−3399	−3430	−3461	−3492	−3523
−80	−2920	−2953	−2985	−3018	−3050	−3082	−3115	−3147	−3179	−3211
−70	−2586	−2620	−2654	−2687	−2721	−2754	−2788	−2821	−2854	−2887
−60	−2243	−2277	−2312	−2347	−2381	−2416	−2450	−2484	−2518	−2552
−50	−1889	−1925	−1961	−1996	−2032	−2067	−2102	−2137	−2173	−2208
−40	−1527	−1563	−1600	−1636	−1673	−1709	−1745	−1781	−1817	−1853
−30	−1156	−1193	−1231	−1268	−1305	−1342	−1379	−1416	−1453	−1490
−20	−777	−816	−854	−892	−930	−968	−1005	−1043	−1081	−1118
−10	−392	−431	−469	−508	−547	−585	−624	−662	−701	−739
0	0	−39	−79	−118	−157	−197	−236	−275	−314	−353
0	0	39	79	119	158	198	238	277	317	357
10	397	437	477	517	557	597	637	677	718	758
20	798	838	879	919	960	1000	1041	1081	1122	1162
30	1203	1244	1285	1325	1366	1407	1448	1489	1529	1570
40	1611	1652	1693	1734	1776	1817	1858	1899	1940	1981
50	2022	2064	2105	2146	2188	2229	2270	2312	2353	2394
60	2436	2477	2519	2560	2601	2643	2684	2726	2767	2809
70	2850	2892	2933	2975	3016	3058	3100	3141	3183	3224
80	3266	3307	3349	3390	3432	3473	3515	3556	3598	3639
90	3681	3722	3764	3805	3847	3888	3930	3971	4012	4054
100	4095	4137	4178	4219	4261	4302	4343	4384	4426	4467
110	4508	4549	4590	4632	4673	4714	4755	4796	4837	4878
120	4919	4960	5001	5042	5083	5124	5164	5205	5246	5287
130	5327	5368	5409	5450	5490	5531	5571	5612	5652	5693
140	5733	5774	5814	5855	5895	5936	5976	6016	6057	6097
150	6137	6177	6218	6258	6298	6338	6378	6419	6459	6499
160	6539	6579	6619	6659	6699	6739	6779	6819	6859	6899
170	6939	6979	7019	7059	7099	7139	7179	7219	7259	7299
180	7338	7378	7418	7458	7498	7538	7578	7618	7658	7697
190	7737	7777	7817	7857	7897	7937	7977	8017	8057	8097
200	8137	8177	8216	8256	8296	8336	8376	8416	8456	8497
210	8537	8577	8617	8657	8697	8737	8777	8817	8857	8898
220	8938	8978	9018	9058	9099	9139	9179	9220	9260	9300
230	9341	9381	9421	9462	9502	9543	9583	9624	9664	9705
240	9745	9786	9826	9867	9907	9948	9989	10029	10070	10111
250	10151	10192	10233	10274	10315	10355	10396	10437	10478	10519
260	10560	10600	10641	10682	10723	10764	10805	10846	10887	10928
270	10969	11010	11051	11093	11134	11175	11216	11257	11298	11339
280	11381	11422	11463	11504	11546	11587	11628	11669	11711	11752
290	11793	11835	11876	11918	11959	12000	12042	12083	12125	12166
300	12207	12249	12290	12332	12373	12415	12456	12498	12539	12581
310	12623	12664	12706	12747	12789	12831	12872	12914	12955	12997
320	13039	13080	13122	13164	13205	13247	13289	13331	13372	13414
330	13456	13497	13539	13581	13623	13665	13706	13748	13790	13832
340	13874	13915	13957	13999	14041	14083	14125	14167	14208	14250

Type K thermocouple reference table (cont)

(with reference junctions at 0°C).

Deg. C.	0	1	2	3	4	5	6	7	8	9
	THERMOELECTRIC VOLTAGE IN ABSOLUTE MICROVOLTS									
350	14292	14334	14376	14418	14460	14502	14544	14586	14628	14670
360	14712	14754	14796	14838	14880	14922	14964	15006	15048	15090
370	15132	15174	15216	15258	15300	15342	15384	15426	15468	15510
380	15552	15594	15636	15679	15721	15763	15805	15847	15889	15931
390	15974	16016	16058	16100	16142	16184	16227	16269	16311	16353
400	16395	16438	16480	16522	16564	16607	16649	16691	16733	16776
410	16818	16860	16902	16945	16987	17029	17072	17114	17156	17199
420	17241	17283	17326	17368	17410	17453	17495	17537	17580	17622
430	17664	17707	17749	17792	17834	17876	17919	17961	18004	18046
440	18088	18131	18173	18216	18258	18301	18343	18385	18428	18470
450	18513	18555	18598	18640	18683	18725	18768	18810	18853	18895
460	18938	18980	19023	19065	19108	19150	19193	19235	19278	19320
470	19363	19405	19448	19490	19533	19576	19618	19661	19703	19746
480	19788	19831	19873	19916	19959	20001	20044	20086	20129	20172
490	20214	20257	20299	20342	20385	20427	20470	20512	20555	20598
500	20640	20683	20725	20768	20811	20853	20896	20938	20981	21024
510	21066	21109	21152	21194	21237	21280	21322	21365	21407	21450
520	21493	21535	21578	21621	21663	21706	21749	21791	21834	21876
530	21919	21962	22004	22047	22090	22132	22175	22218	22260	22303
540	22346	22388	22431	22473	22516	22559	22601	22644	22687	22729
550	22772	22815	22857	22900	22942	22985	23028	23070	23113	23156
560	23198	23241	23284	23326	23369	23411	23454	23497	23539	23582
570	23624	23667	23710	23752	23795	23837	23880	23923	23965	24008
580	24050	24093	24136	24178	24221	24263	24306	24348	24391	24434
590	24476	24519	24561	24604	24646	24689	24731	24774	24817	24859
600	24902	24944	24987	25029	25072	25114	25157	25199	25242	25284
610	25327	25369	25412	25454	25497	25539	25582	25624	25666	25709
620	25751	25794	25836	25879	25921	25964	26006	26048	26091	26133
630	26176	26218	26260	26303	26345	26387	26430	26472	26515	26557
640	26599	26642	26684	26726	26769	26811	26853	26896	26938	26980
650	27022	27065	27107	27149	27192	27234	27276	27318	27361	27403
660	27445	27487	27529	27572	27614	27656	27698	27740	27783	27825
670	27867	27909	27951	27993	28035	28078	28120	28162	28204	28246
680	28288	28330	28372	28414	28456	28498	28540	28583	28625	28667
690	28709	28751	28793	28835	28877	28919	28961	29002	29044	29086
700	29128	29170	29212	29254	29296	29338	29380	29422	29464	29505
710	29547	29589	29631	29673	29715	29756	29798	29840	29882	29924
720	29965	30007	30049	30091	30132	30174	30216	30257	30299	30341
730	30383	30424	30466	30508	30549	30591	30632	30674	30716	30757
740	30799	30840	30882	30924	30965	31007	31048	31090	31131	31173
750	31214	31256	31297	31339	31380	31422	31463	31504	31546	31587
760	31629	31670	31712	31753	31794	31836	31877	31918	31960	32001
770	32042	32084	32125	32166	32207	32249	32290	32331	32372	32414
780	32455	32496	32537	32578	32619	32661	32702	32743	32784	32825
790	32866	32907	32948	32990	33031	33072	33133	33154	33195	33236
800	33277	33318	33359	33400	33441	33482	33523	33564	33604	33645
810	33686	33727	33768	33809	33850	33891	33931	33972	34013	34054
820	34095	34136	34176	34217	34258	34299	34339	34380	34421	34461
830	34502	34543	34583	34624	34665	34705	34746	34787	34827	34868
840	34909	34949	34990	35030	35071	35111	35152	35192	35233	35273
850	35314	35354	35395	35435	35476	35516	35557	35597	35637	35678
860	35718	35758	35799	35839	35880	35920	35960	36000	36041	36081
870	36121	36162	36202	36242	36282	36323	36363	36403	36443	36483
880	36524	36564	36604	36644	36684	36724	36764	36804	36844	36885
890	36925	36965	37005	37045	37085	37125	37165	37205	37245	37285
900	37325	37365	37405	37445	37484	37524	37564	37604	37644	37684
910	37724	37764	37803	37843	37883	37923	37963	38002	38042	38082
920	38122	38162	38201	38241	38281	38320	38360	38400	38439	38479
930	38519	38558	38598	38638	38677	38717	38756	38796	38836	38875
940	38915	38954	38994	39033	39073	39112	39152	39191	39231	39270
950	39310	39349	39388	39428	39467	39507	39546	39585	39625	39664
960	39703	39743	39782	39821	39861	39900	39939	39979	40018	40057
970	40096	40136	40175	40214	40253	40292	40332	40371	40410	40449
980	40488	40527	40566	40605	40645	40684	40723	40762	40801	40840
990	40879	40918	40957	40996	41035	41074	41113	41152	41191	41230
1000	41269	41308	41347	41385	41424	41463	41502	41541	41580	41619
1010	41657	41696	41735	41774	41813	41851	41890	41929	41968	42006
1020	42045	42084	42123	42161	42200	42239	42277	42316	42355	42393
1030	42432	42470	42509	42548	42586	42625	42663	42702	42740	42779
1040	42817	42856	42894	42933	42971	43010	43048	43087	43125	43164
1050	43202	43240	43279	43317	43356	43394	43432	43471	43509	43547
1060	43585	43624	43662	43700	43739	43777	43815	43853	43891	43930
1070	43968	44006	44044	44082	44121	44159	44197	44235	44273	44311
1080	44349	44387	44425	44463	44501	44539	44577	44615	44653	44691
1090	44729	44767	44805	44843	44881	44919	44957	44995	45033	45070

RS data

Type K thermocouple reference table (cont)

(with reference junctions at 0°C).

Deg. C.	0	1	2	3	4	5	6	7	8	9
	THERMOELECTRIC VOLTAGE IN ABSOLUTE MICROVOLTS									
1100	45108	45146	45184	45222	45260	45297	45335	45373	45411	45448
1110	45486	45524	45561	45599	45637	45675	45712	45750	45787	45825
1120	45863	45900	45938	45975	46013	46051	46088	46126	46163	46201
1130	46238	46275	46313	46350	46388	46425	46463	46500	46537	46575
1140	46612	46649	46687	46724	46761	46799	46836	46873	46910	46948
1150	46985	47022	47059	47096	47134	47171	47208	47245	47282	47319
1160	47356	47393	47430	47468	47505	47542	47579	47616	47653	47689
1170	47726	47763	47800	47837	47874	47911	47948	47985	48021	48058
1180	48095	48132	48169	48205	48242	48279	48316	48352	48389	48426
1190	48462	48499	48536	48572	48609	48645	48682	48718	48755	48792
1200	48828	48865	48901	48937	48974	49010	49047	49083	49120	49156
1210	49192	49229	49265	49301	49338	49374	49410	49446	49483	49519
1220	49555	49591	49627	49663	49700	49736	49772	49808	49844	49880
1230	49916	49952	49988	50024	50060	50096	50132	50168	50204	50240
1240	50276	50311	50347	50383	50419	50455	50491	50526	50562	50598
1250	50633	50669	50705	50741	50776	50812	50847	50883	50919	50954
1260	50990	51025	51061	51096	51132	51167	51203	51238	51274	51309
1270	51344	51380	51415	51450	51486	51521	51556	51592	51627	51662
1280	51697	51733	51768	51803	51838	51873	51908	51943	51979	52014
1290	52049	52084	52119	52154	52189	52224	52259	52294	52329	52364
1300	52398	52433	52468	52503	52538	52573	52608	52642	52677	52712
1310	52747	52781	52816	52851	52886	52920	52955	52989	53024	53059
1320	53093	53128	53162	53197	53232	53266	53301	53335	53370	53404
1330	53439	53473	53507	53542	53576	53611	53645	53679	53714	53748
1340	53782	53817	53851	53885	53920	53954	53988	54022	54057	54091
1350	54125	54159	54193	54228	54262	54296	54330	54364	54398	54432
1360	54466	54501	54535	54569	54603	54637	54671	54705	54739	54773
1370	54807	54841	54875							

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RS data

150 MHz ÷100 prescaler i.c.

Stock number 307-474

The 8269 is a fixed ratio ECL ÷ 100 Counter with a minimum guaranteed toggle frequency of 150MHz over a –30°C to + 70°C temperature range. The device can operate in the single-ended or differential input mode, and is typically capacitively coupled the single source. An input amplifier is included to allow use of extremely small amplitude high frequency signals. The output of the device is similar to Low Power Schottky TTL and produces a square wave of frequency $f_{out} = f_{in}/100$.

Features

- Low power 170mW typical
- High Frequency, DC to 150MHz, Small input amplitude
- Sine wave input 10MHz<fin<150MHz
- TTL compatible output
- May be used with TTL input
- Single supply operation 5.2V ± 10%
- Single ended or differential input modes
- Positive or negative edge triggered
- Count down sequence avoids FM IF harmonics
- ECL dividers reduce switching transients
- On-chip zener diode gives simple external regulator

Figure 1 **Pin connections**

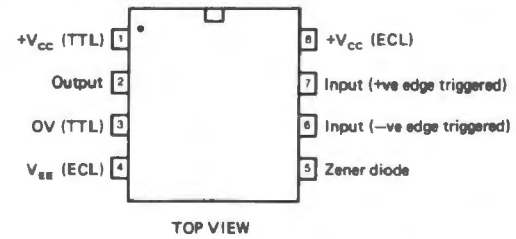


Figure 2 **Logic diagram**

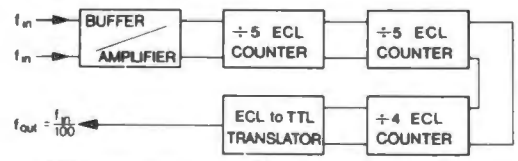
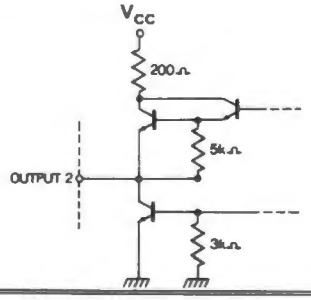


Figure 7 **Output circuit diagram**



Typical applications

Figure 3 **High frequency, single-ended input**

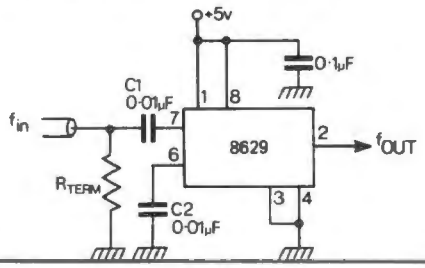


Figure 4 **TTL input (DC<f_{in}<f_{max})**

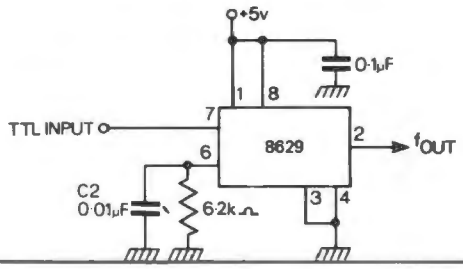


Figure 5 **Voltage regulator**

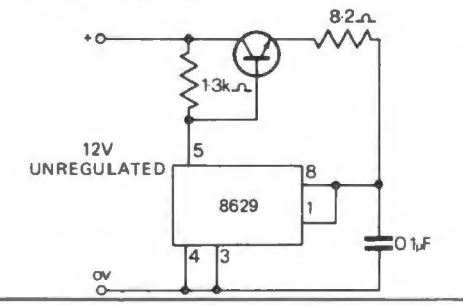
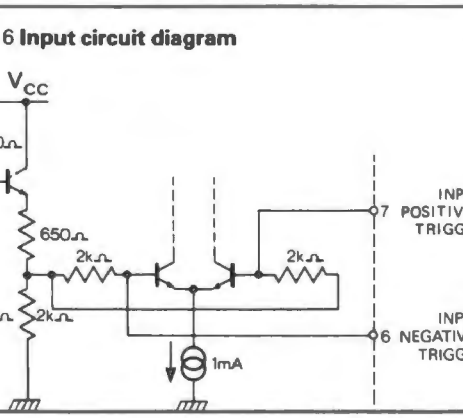


Figure 6 **Input circuit diagram**



N.B. recommended capacitors:
0.01μF sub min. ceramic 124-257
0.1μF low voltage disc ceramic 124-178

RS data

Operating conditions

Supply voltage: V_{CC} = + 5.2V ± 0.52V
Temperature range: –30°C to + 70°C

Electrical characteristics

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = + 5.2V ±0.52V, T_{amb} = 25°C

Notes

1. All currents into device pins shown as positive, out of device pins negative, all voltages referenced to ground unless otherwise stated. All values shown as max or min on absolute value basis.
2. The current supplied to the zener should not exceed 10mA.

Absolute maximum ratings

Power Supply Voltage ——— 8V
Input Voltage V_{IN}(DC) ——— not greater than supply voltage
Output voltage V_{OUT} ——— 5.5V
Output current I_I ——— 40mA
Zener current I_Z ——— 20mA
Operating junction temperature ——— 150°C
Storage temperature range —— –55°C to + 150°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Maximum input frequency	f_{max}	150	200		MHz	V_{CC} = 5.2V, V_{IN} = 600mVp–p, single ended
Input voltage	V_{IN}(p–p)	200		1000	mVp–p	V_{CC} = 5.2V, single ended
Input voltage	V_{IN}(p–p)	100		1000	mVp–p	V_{CC}5.2V, differential
Minimum input frequency with sine wave	f_{sine}	10			MHz	V_{CC} = 5.2V, V_{IN} = 600m Vp–p
Minimum slew rate of square wave input	dv/dt			50	V/μs	V_{CC} = 5.2V, V_{IN} = 600m Vp–p
Logic 1 output voltage	V_{OH}	2.4 2.0			V V	V_{CC} = Min, I_{OH} = –400μA V_{CC} = Min, I_{OH} = –1.6mA
Output short circuit current	I_{OS}	–10		–40	mA	V_{CC} = Max
Logic O output voltage	V_{OL}			0.5	V	v_{CC} = Min, I_{OL} = 8mA
Supply current	I_{CC}		33	45	mA	V_{CC} = Max
Zener voltage, pin 5	V_Z		6.3		V	I_Z = 5mA (see note 2)

Operating notes

Two ground and two V_{CC} connections and are provided, separating the ECL stages from the TTL section, isolating the noise transients inherent in the TTL structure. In most cases, shorting the two grounds to a good ground plane and the V_{CC}'s to a wide V_{CC} bus will provide sufficient isolation. All components used in the circuit layout should be suitable for the frequencies involved and leads should be kept short to minimise stray inductance.

The signal source is usually capacitively coupled to the input as shown in Fig. 3. In the single-ended mode a capacitor of 0.01μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be increased at lower frequencies. If the input is likely to be interrupted, it may be desirable to connect a 100k Ω resistor between an input and ground. In the single ended mode it is preferable to connect the resistor to the unused input. The addition of the 100k Ω resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions.

The input waveform will normally be sinusoidal but below 10MHz correct operation depends on the slew rate of the input signal. A slew rate of 50V/μs will enable the device to operate down to DC. The device will operate with a TTL input signal as shown in Fig. 4 and is DC coupled to the input.

A digital frequency display system can be derived separately or in conjunction with a phase locked loop, and it can extend the useful range of many inexpensive frequency counters to, typically, 200MHz.

The on-chip zener diode allows a simple stabilised power supply to be constructed with the addition of a few extra external components as shown in Fig. 5.

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RS data

Ultrasonic transducers

A range of two transducers operating at 40kHz approximately and designed for ultrasonic transmission and reception. The ultrasonic transmitter, 307-351 is capable of emitting 106dB (0dB = 2 x $10^{-4}\mu$bar) and the receiver 307-367 has a sensitivity of −65dB (0dB = 1/μbar/V/metre).

These units can be used for the transmission of continuous wave ultrasonic sound or for pulsed sound applications.

Characteristics

Item		Unit	307-351	307-367
Transmitting sensitivity	Sv	dB*1	106	–
Receiving sensitivity	Mv	dB*2	–	−65
Resonant frequency (transmitting)	Frsv	kHz*3	40±1	–
Resonant frequency (receiving)	Frmv	kHz*4	–	40±1
Directional angle	θ½	o	Approx. 30	
Maximum input voltage		Vrms	20	–
Impedance		Ω	Approx. 500	Approx. 30k
Capacitance		pF	1100±20%	
Pulse rise time		msec.	2.0	0.5
Maximum input voltage for pulse operation		Vp.p	60	–
Temperature range		°C	−20 to +60	
Transmitting selectivity	Qsv		Approx. 70	–
Receiving selectivity	Qmv			Approx. 60

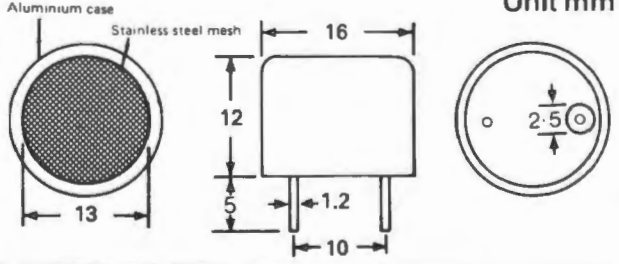
*1 0dB = 2 x $10^{-4}\mu$bar
*2 0dB = 1V/μbar
*3 Frequency where transmitting sensitivity is maximum
*4 Frequency where receiving sensitivity is maximum

Applications

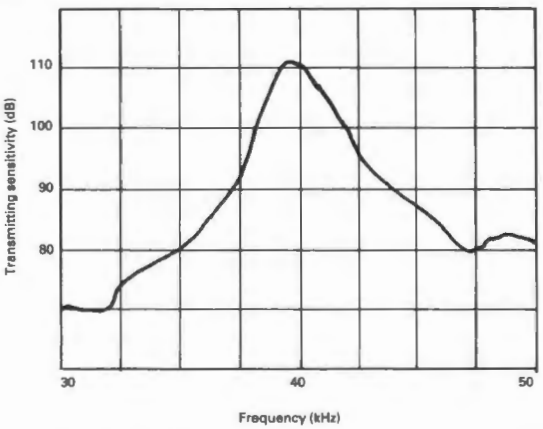
Burglar alarm systems
Proximity switches
Liquid level meters
Anti-collision devices
Counters for moving objects
TV remote control systems

Shape and dimensions

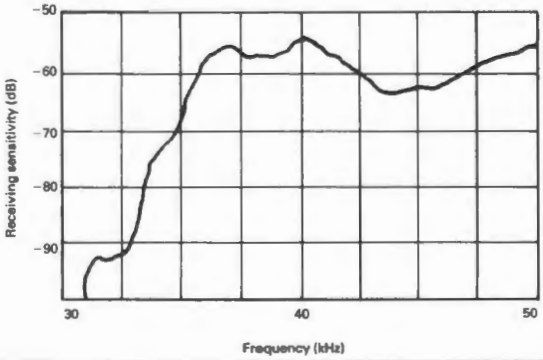
Unit mm



Frequency response (transmitting)

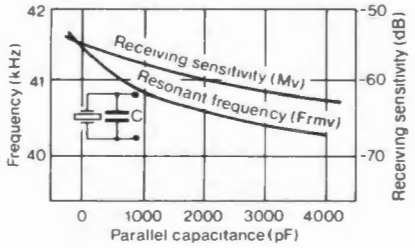


Frequency response (receiving)

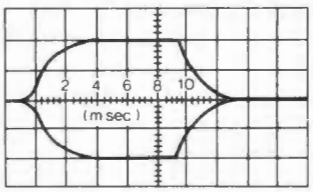


RS data

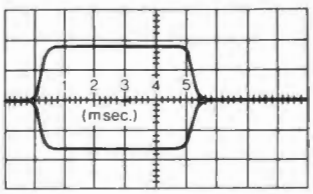
Effect of parallel capacitance



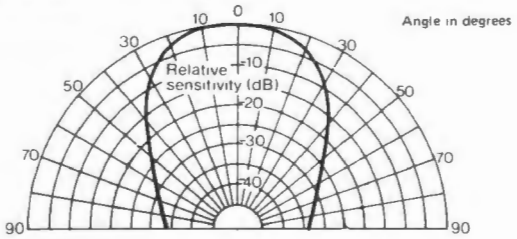
Pulse response (transmitting)



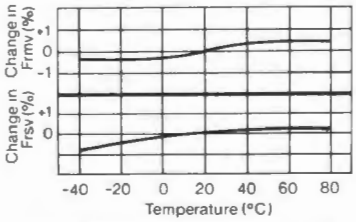
Pulse response (receiving)



Directional radiation pattern



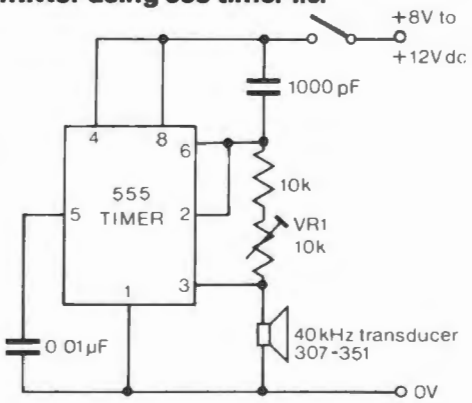
Temperature characteristics TRANSMITTER & RECEIVER



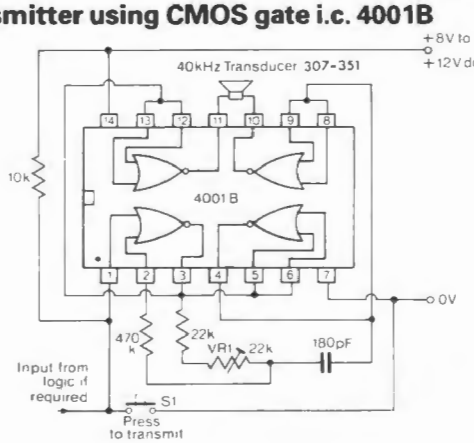
The following circuits show how the transducers may be used in remote control applications. Either of the transmitter circuits may be used with the receiver. The frequency of oscillation is adjusted by means of VR1 for maximum sensitivity. The CMOS circuit allows direct interfacing with logic circuitry. In the receiver VR2 is adjusted for maximum sensitivity.

Note: The relay energises when a signal is received from the transmitter.

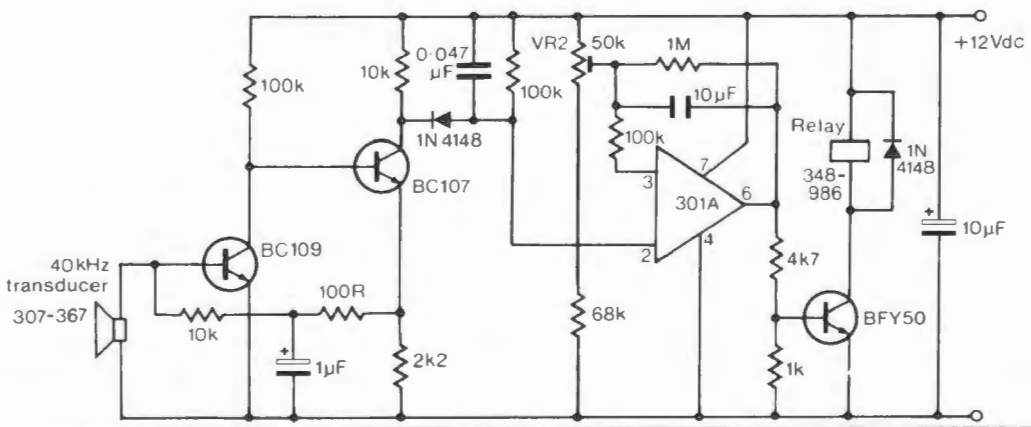
Transmitter using 555 timer i.c.



Transmitter using CMOS gate i.c. 4001B



Receiver



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RS data

Clock module

Stock number 307-402

The RS Clock Module consists of a ready assembled printed circuit board incorporating the logic chip, display L.E.D.'s and additional components which together with a separate transformer 207-920 and setting switches allows a complete full function time clock to be constructed.

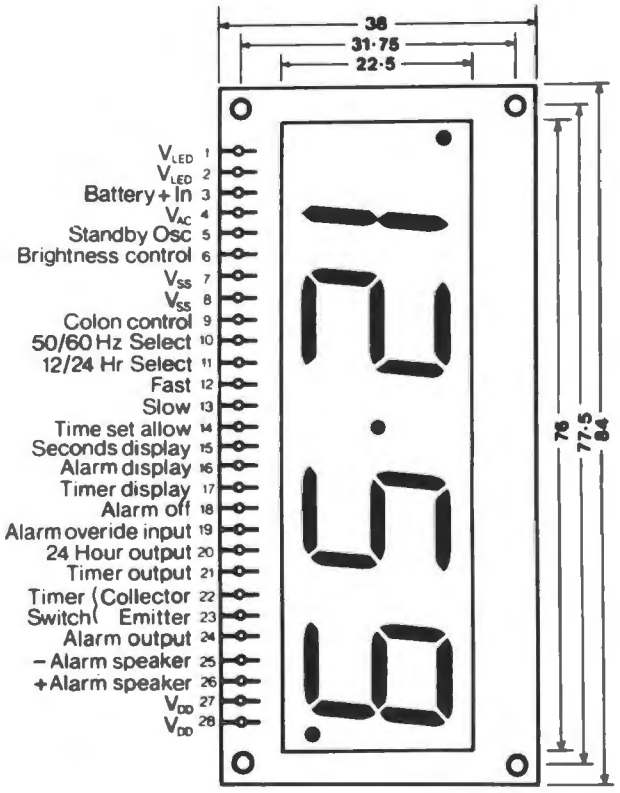
The Module display serves to indicate time, alarm or timer settings, alarm on and P.M. In addition the module has an uncommitted (emitter - collector) PNP transistor for external switching and an output capable of driving an 8 Ω loudspeaker for use as an alarm sounder.

Features

- 0.7 inch high LED display
- 12/24 hour display format
- Battery powered back-up oscillator
- 24 hour alarm comparator
- Seconds display mode
- Power failure indication
- Display brightness control
- Lamp test facility
- 50/60 Hz input
- Simple fast/slow setting controls

Dimensions and connections

All dimensions in mm
Fixing holes 2.8 mm dia.
Connections on 0.1" pitch
0.040" dia.



Absolute maximum ratings

Voltage at all pins except 1 and 2 ____ V_{SS} — 0.3V to V_{SS} + 12V
Voltage at pins 1 and 2 ____ V_{SS} — 3V to V_{SS} + 6V

Operating temperature range ____ 0°C to + 70°C
Storage temperature range ____ −20°C to + 70°C
Terminal temperature (soldering 5 seconds) ____ 230°C

Electrical characteristics

Unless otherwise specified: $T_A = 25°C$, $V_{AC} = 7.75V_{RMS} = V_{SS} = 0V$, $V_{LED} = 3.5V_{RMS}$.

Notes

1. The power fail detect voltage is 0.25V or more above the voltage at which time keeping data will be lost.
2. Does not include tolerances of components external to NMOS Clock IC.

Parameter	Conditions	Min	Typ	Max	Units
V_{AC}, MOS Supply Voltage	Fully Operational Clock Power Fail Detect (See Note 1)	6.5	7.75 3	9.0 6	V_{RMS} V_{RMS}
I_{AC}, MOS Supply Current			5	10	mA_{AVG}
V_{LED}, LED Supply Voltage		3.0	3.5	4.0	$V_{RMS} \times 2$
I_{LED}, LED Supply Current	Lamp Test, Pin 6 Open (Bright)		315		mA_{AVG}
V_{BATT}, MOS Supply Voltage	$V_{AC} = 0V$, $V_{LED} = 0V$, Timekeeping Maintained only	7.5	9.0	12.0	V_{DC}
I_{BATT}, MOS Supply Current	$V_{BATT} = 9V_{DC}$		5	10	mA_{DC}
Control Input Voltages (Pins 9-19) Logical Low Level Logical High Level	 $V_{DD} \approx (V_{AC} \times 1.4) - 1.8V$	 V_{SS} $V_{DD} - 3$		 $V_{SS} + 0.5$ V_{DD}	 V V
Control Input Current	Internal Resistance to V_{DD}, $V_{IN} = 0V$			-10	μA
Alarm/Timer-Output Current (Pins 21 and 24) Alarm/Timer On Sink Current Alarm/Timer Off Source Current	 $V_{OL} = V_{SS} + 2V$ $V_{OH} = V_{DD} - 0.25V$	 5		 -40	 mA μA
24-Hour Output Current AM On, Sink Current PM Off, Source Current	 $V_{OL} = V_{SS} + 2V$ $V_{OH} = V_{DD} - 0.25V$	 400		 -100	 μA μA
Alarm Output Frequency	$T_A = 0°C$ to $70°C$, $V_{AC} = 6.5$ to $9.0 V_{RMS}$		800		Hz
Timer Switch Input Current				200	mA
Speaker Output Current	$R_L = 8\Omega$, 50% Duty Cycle	200			mApk
Alarm Oscillator Frequency Tolerance	$T_A = 0°C$ to $70°C$, $V_{AC} = 6.5$ to $9.0 V_{RMS}$ (See Note 2)			± 20	%
Standby Oscillator Frequency Tolerance	$T_A = 0°C$ to $70°C$, $V_{BATT} = 7.5$ to $10.5 V_{DC}$, $V_{AC} = 0V$, $V_{LED} = 0V$ (See Note 2)			± 20	%

Operating modes

The time, alarm, seconds and timer settings are all achieved by first selecting the display option (press to display) and then activating the fast set and/or slow set switches. The following tables give the setting control functions and display modes.

To prevent inadvertent setting of time the module is fitted with a time set allow input which must be connected to V_{SS} to allow the setting of the time counters. On applying a.c. power to the module without battery back-up the display will flash indicating the operation of the power failure detector. Setting the time will reset the detector.

Display modes

Selected display mode	Digit No. 1	Digit No. 2	Digit No. 3	Digit No. 4
Time	10's of hours.	Hours	10's of minutes	Minutes
Seconds	Blanked	Minutes	10's of seconds	Seconds
Alarm	10's of hours	Hours	10's of minutes	Minutes
Timer	Blanked	Blanked	10's of minutes	Minutes
Alarm and Timer	Lamp test – all segments illuminated			

Setting control functions

Selected display mode	Set Input	Function
*Time or Seconds and Time set allow	Slow	Minutes advance at 2Hz rate
	Fast	Minutes advance at 50Hz rate
	Both (12 hour)	Reset to 12.00 PM (midnight)
	Both (24 hour)	Reset to 0.00.00
Alarm	Slow	Alarm minutes advance at 2Hz rate
	Fast	Alarm minutes advance at 50Hz rate
	Both (12 hour)	Alarm resets to 12.00 PM (midnight)
	Both (24 hours)	Alarm resets to 0.00.00
Timer	Slow	Subtracts at 2HZ rate
	Fast	Subtracts at 10Hz rate
	Both	Timer resets to 59 minutes

*Time setting is only activated when the time set allow switch is closed. When setting time, timer minutes will decrement at the rate of the time counter until the timer counter reaches '00' minutes (timer counter will not re-cycle)

Battery back-up

The module incorporates an RC back-up oscillator which is automatically activated when mains failure occurs. The RC oscillator is powered by a 9V battery (PP3 or similar) which is normally inactive. However, owing to its wide frequency tolerance (±20%) this timekeeping facility is suitable for temporary mains failure only. The oscillator is adjusted externally with a 4.7MΩ potentiometer to give 20Hz on pin 5. In the back-up mode, timekeeping, alarm output and timer output are preserved. Setting facilities, speaker output and the display, however, will only function when the AC mains is restored. For momentary viewing of the display in battery back-up mode connect a 3V battery (2 alkaline cells 591-231 in series) across pin 26 and pin 7 as shown in figure 4.

Note: The transformer must always remain in circuit for the module to operate correctly when in the battery back-up mode.

Brightness control

Two options are available for the display brightness control, either a single pole on/off switch for bright/dim control or a single variable resistor to give continuously variable control. In the event that brightness control is not required pin 6 should be left unconnected.

Colon control

Either a flashing or static colon can be accommodated. Connecting pin 9 to V_{SS} will cause the colon to remain permanently on; unconnected, the colon will flash.

50/60Hz select

The module derives its timekeeping clock input (except in battery back-up mode) from the mains supply frequency; pin 10 allows the user to select 50 or 60Hz input frequencies. Connecting pin 10 to V_{SS} programs the unit for 50Hz operation; left unconnected the 60Hz mode of operation is effected.

12/24 hour select

Pin 11 controls the display mode. For a 24 hour display connect this pin to V_{SS}. When pin 11 is left unconnected the display is in the 12 hour format, and the top left hand corner L.E.D. will light, when appropriate, indicating PM.

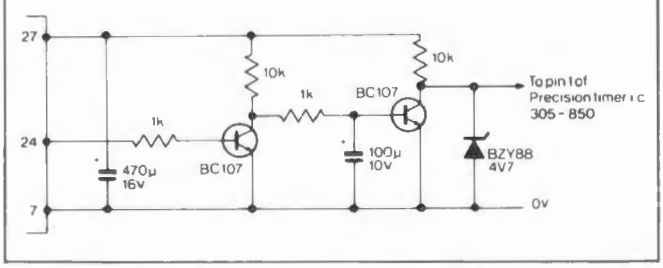
Alarm output

Provides an output of approximately 800Hz modulated at 2Hz for a period of one hour. May be disabled for 8 minutes by the alarm override.

When it is desired to switch an appliance on at a preset time, the alarm output may be utilised together with the circuit shown in figure 1.

The "on" period will commence at the preset alarm time setting and the duration of the period is determined by the precision timer i.c. (305-580). For more information on the precision timer i.c. refer to data sheet 2466, available on request.

Figure 1 **Interfacing precision timer i.c.**



Alarm off

This input (pin 18) resets the alarm once activated (momentary connection to V_{SS}) or disables the alarm function (continuously connected to V_{SS}). The L.E.D. in the bottom right corner of the module illuminates when the alarm mode is enabled (pin 18 left unconnected).

Alarm overide input

Once the alarm has sounded momentarily connecting pin 19 to V_{SS} will turn the alarm off for 8 minutes after which time the alarm will resound. This temporary disabling of the alarm is possible for a full one hour after the initial start of the alarm. After one hour the alarm will turn off whether disabled or not.

24 hour output

Pin 20 produces a changing pulse at 00.00.00. hours (24 hour mode) or 12.00.00 AM (12 hour mode). This output may be used for days counting or feeding into calendar logic circuitry. This is a square wave pulse of 24 hour duration, consisting of 12 hours 'on', 12 hours 'off'

RS data

Figure 2 **Output driving a relay**

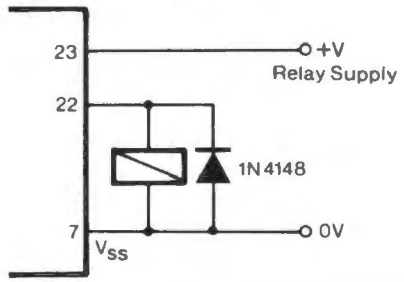
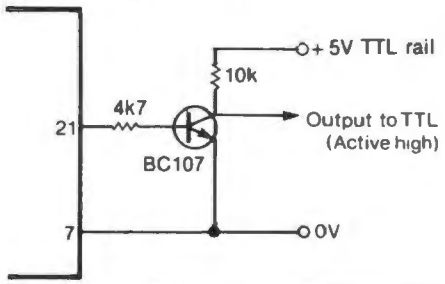


Figure 3 **Interfacing with TTL**



Timer switch

Consisting of an uncommitted PNP transistor this output can be used to switch external circuitry. The output is switched 'on' for a period up to 59 minutes and is activated by selecting the timer display mode. The length of the 'on' time is determined by using the set inputs. The timer output is also activated when the alarm is triggered. Disabling the alarm resets the timer to 59 minutes. The output is active low. The timer counter counts down from 59 or the selected timer interval towards 00, at which time the output turns off. The circuits above show how this output may be committed to different applications.

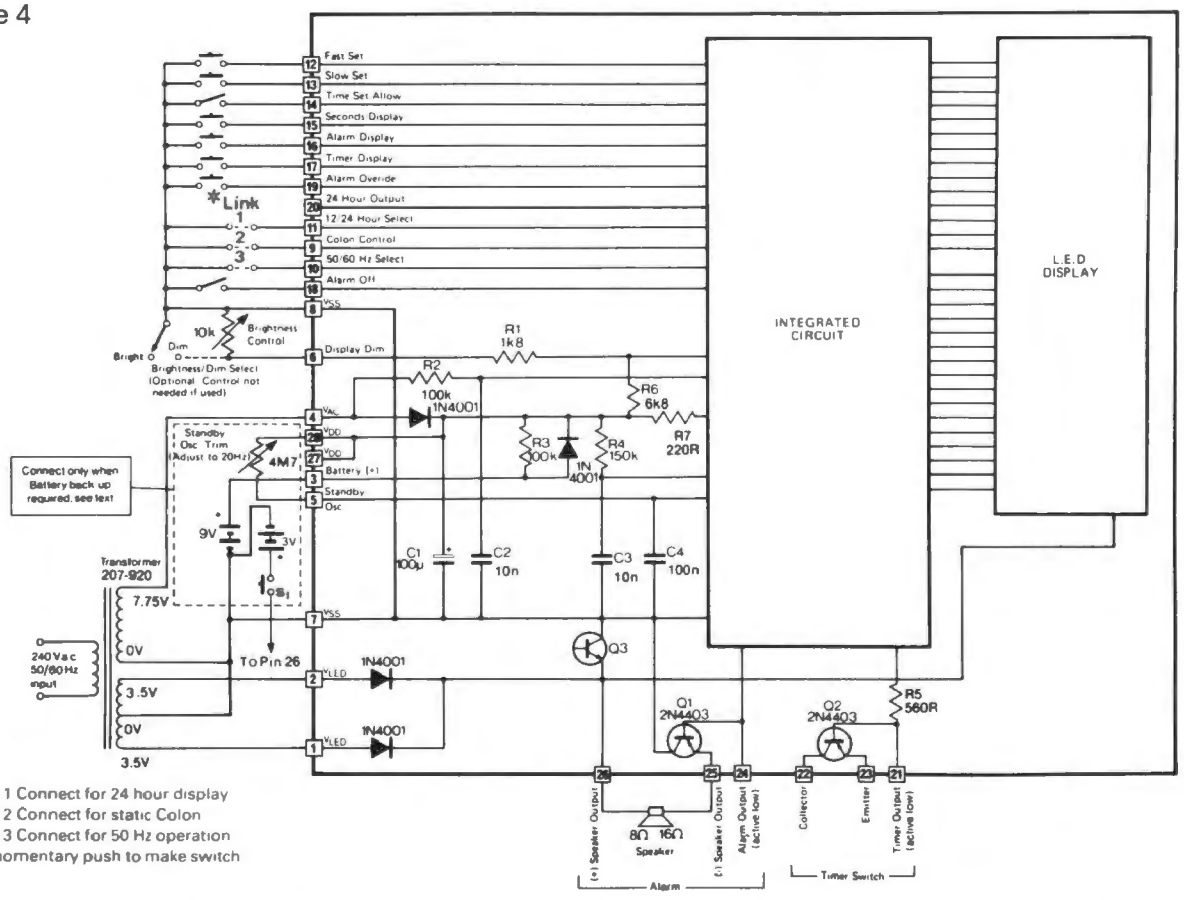
The output may be permanently turned 'on' by connecting pin 21 to V_{SS} via a 560 ohm resistor.
The output transistor used has the following characteristics:-

$V_{cbo} = 45V$ $V_{ceo} = 45V$ $I_C = 100mA$

Full function clock

The circuit shown below gives all necessary connections to build a full function clock unit. For clarity some of the module's internal circuitry is also shown.

Figure 4



* Link 1 Connect for 24 hour display
Link 2 Connect for static Colon
Link 3 Connect for 50 Hz operation
S_1 momentary push to make switch

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RS data

Gas sensor

Stock number 307-733

The RS Gas Sensor is designed to detect Methane, Iso-butane, Propane, Natural gas, etc. before hazardous conditions are created. The device utilises the pellistor principle and is stable against ambient temperature and humidity changes. The sensor is not suitable for the detection of Carbon Monoxide (CO), and should not be mounted in a position where contamination by silicone compounds or salt spray is likely (see Precautions).

Electrical characteristics

Supply voltage	3V ± 10%
Supply current	184mA ± 10%
Operating temperature	–10°C +50°C
Warm-up time	Less than 10 seconds
Response time	Less than 10 seconds

Stability

A warm-up time of 10 seconds from switch-on must be allowed to ensure output stability for accurate readings. The sensor is also position sensitive and should be mounted so that the elements receive equal amounts of gas when subjected to draught.

Construction

The RS gas sensor consists of two heated platinum-wire elements. One is coated by special materials for sensing gas and the other compensates for changes in ambient temperature and humidity. Both elements are housed in double wire-netting for preventing explosions which may otherwise result from the internally heated platinum wires.

A special method of coating the platinum wires with catalytic materials is employed to improve the vibration and mechanical shock handling capabilities of the sensing elements.

Precautions

Although the gas sensor is suitable for a wide range of environments, silicone based products e.g. silicone grease, silicone polish will permanently affect the performance. Long term exposure to salt laden atmospheres will also adversely affect the sensor.

Very high concentrations of gases should be avoided as the elements may be damaged (e.g. permanent damage occurs when the gas sensor is held in the gas stream of an unlit gas burner or lighter).

Features

- Monitoring hazardous areas
- Storage depots and factories
- Boat bilges and cars (LPG)
- Natural gas detection

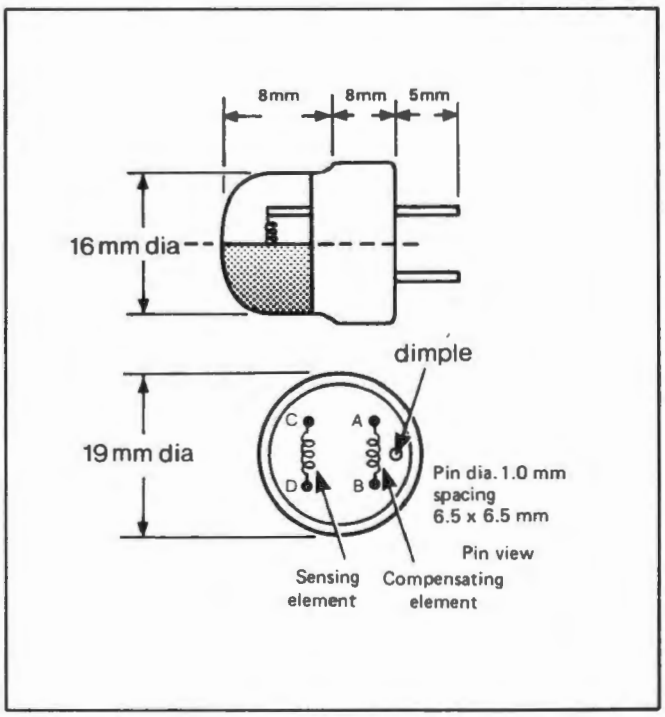
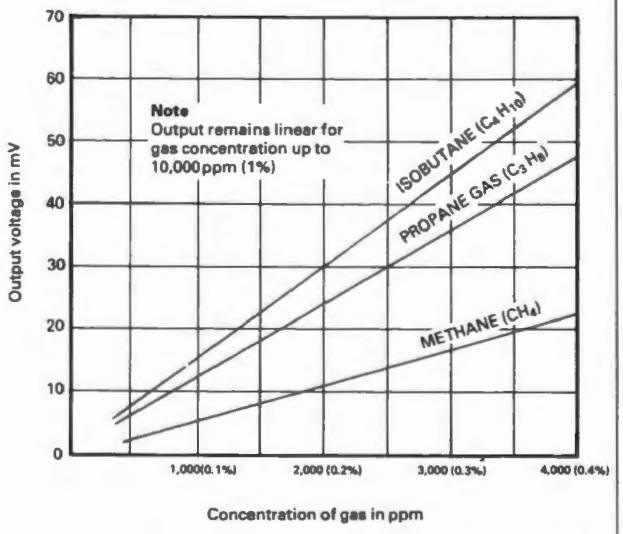


Figure 1. **Sensitivity for various gases**



RS data

Applications

When positioning the RS Sensor it must be remembered that Butane and Propane are heavier than air and leaking gas will sink to the lowest part of the area. The Sensor therefore must be positioned near the floor level (or in the bilges of boats) if these gases are to be detected. When detecting gases in a storage depot several sensors should be used.

Table 1. **Combustion levels**

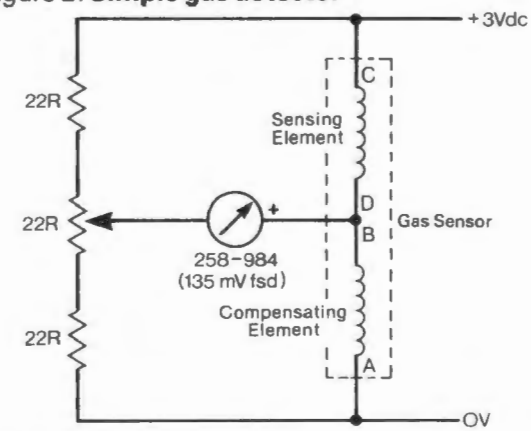
Propane	2.2 to 9.5%
Butane	1.9 to 8.5%
Methane	5.3 to 14.0%

It is recommended that the alarm level be set to 10% or less of the minimum combustion level specified.

Simple gas detector

Figure 2 shows a simple gas detection circuit. The potentiometer should be adjusted to give zero reading initially. The meter output is proportional to gas concentrations as shown previously in figure 1.

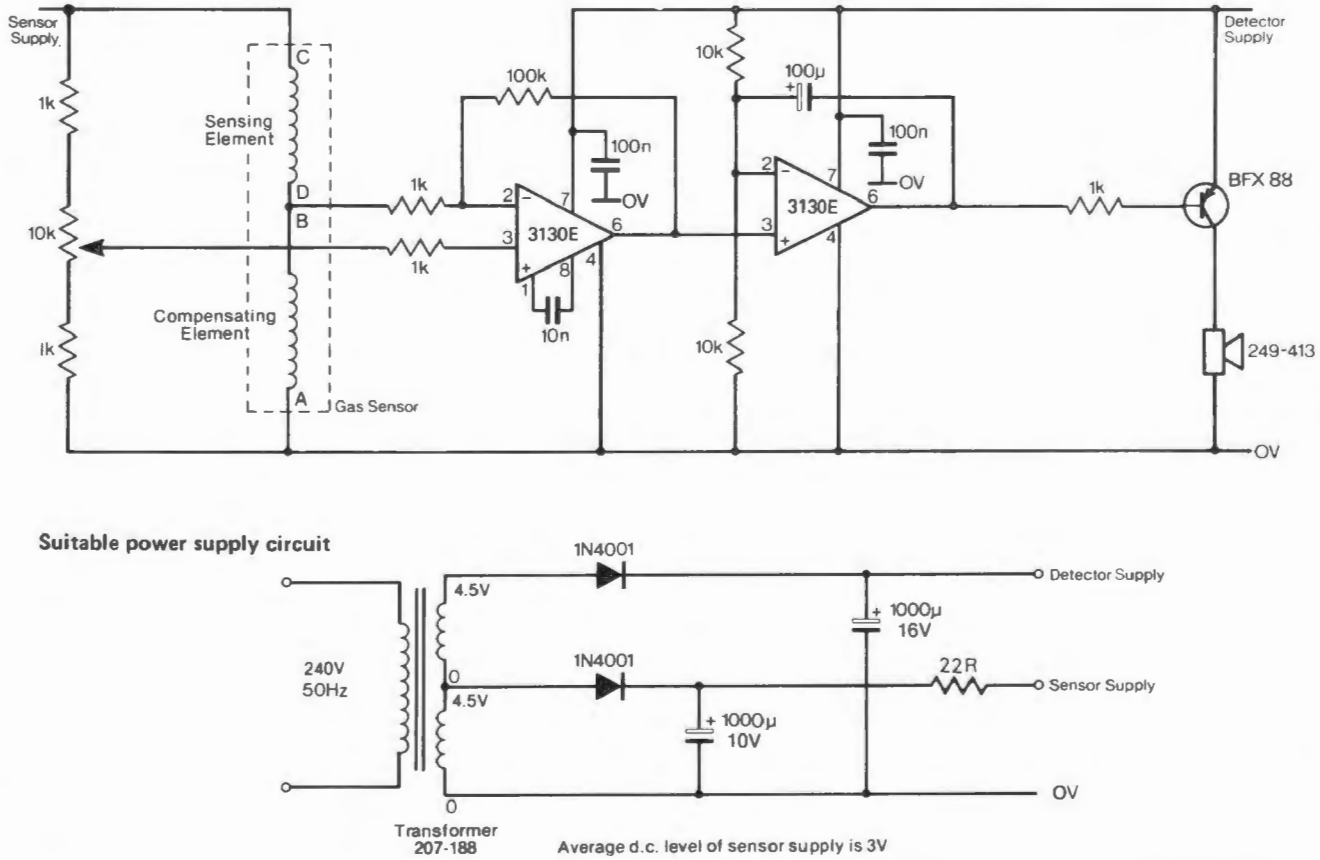
Figure 2: **Simple gas detector**



Simple gas alarm

A simple gas alarm system may be constructed from the circuit shown below. The sensitivity is varied by means of the 10kΩ potentiometer. In order to accurately determine a particular gas alarm level an external reference should be used. When no reference gas concentration is available adjust the potentiometer until the audible alarm is just disabled.

Figure 3: **Simple gas alarm circuit**



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RS data

C-MOS 4 Decade counter driver i.c. 7217

Stock number 307-749

The 7217 C-MOS counter is a four digit, presettable up/down counter with an on board presettable register continuously compared to the counter. The 7217 is intended for use in hardwired applications where thumbwheel switches are used for loading data and single pole switches used for chip control.

The circuit provides a multiplexed 7 segment L.E.D. display output, with common anode configuration. Digit and segment drivers are provided to directly drive displays of up to 0.6in character height at a 25% duty cycle.

The frequency of the onboard oscillator (and thus the multiplex frequency) may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeroes are blanked, and the display drivers may be disabled allowing the display to be used for other purposes. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the store pin. In addition to the display and BCD outputs the circuit provides 3 main outputs; a CARRY/BORROW output which allows for direct cascading of counters, a ZERO output which indicates when the count is zero, and an EQUAL output which indicates when the count is equal to the value contained in the register.

Data is multiplexed into and out of the device by means of a tri-state BCD input/output (I/0) port, which acts as a high impedance input when loading, and provides a multiplexed BCD output. The CARRY/BORROW, ZERO and EQUAL outputs, and the BCD port functioning as an output, will each drive one standard TTL load.

In order to permit operation in noisy environment and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

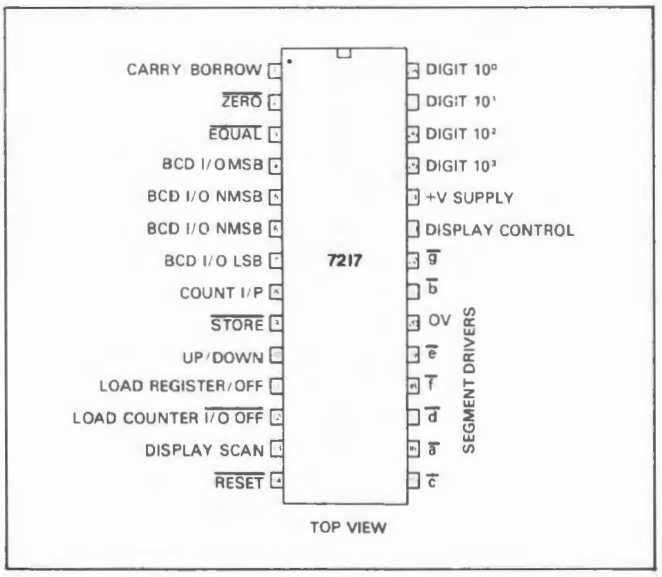
A pair of suitably pre-prepared p.c. boards (R.S. Stock No. 434-403) are available for the 7217 and four seven segment common anode L.E.D. displays (0.3 in or 0.43 in only). The Master board accepts all associated components to drive the 7217 as described later in this data sheet. An instruction leaflet is supplied with the boards giving a complete circuit diagram and wiring details.

Features

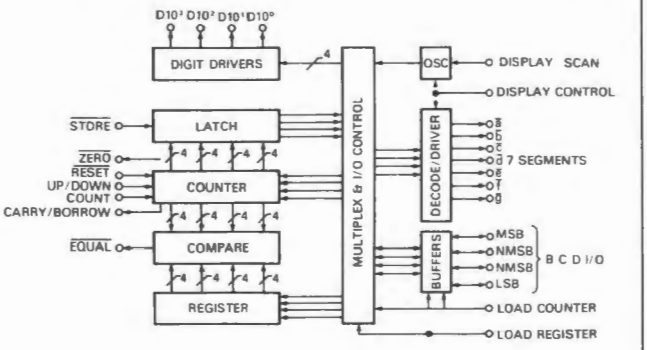
- Four decade, presettable up/down counter with parallel zero detect.
- Settable register with contents continuously compared to counter.
- Directly drives multiplexed 7 segment common anode LED displays.
- On-board multiplexed scan oscillator.
- TTL compatible BCD I/0 port, CARRY/BORROW, EQUAL, and ZERO outputs.
- Display blank control for low power operation; quiescent power dissipation <5mW.
- Low voltage C-MOS process; single 5V (±10%) supply Schmitt trigger on counter input.

Absolute maximum ratings

Power dissipation[1] ——— 1 watt
Supply voltage (V max) ——— 6 volts
Input Voltage (any terminal)[2] — V_{DD} +0.3 to OV −0.3
Operating temperature range ——— −20°C to +70°C
Storage temperature range ——— −55°C to + 125°C



Simplified schematic



Note 1. This limit refers to the package and will not be obtained during normal operation.

Note 2. Due to the SCR structure inherent in the C-MOS process used to fabricate this device, connecting any terminal to a voltage greater than V_{DD} or less than OV may cause destructive latch up. For this reason it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established and that in multiple supply systems the supply to the 7217 be turned on first.

Note 3. In the 7217 the UP/DOWN, STORE, RESET and the BCD I/O as inputs have pull up devices which consume power when connected to OV supply. When all these terminals are connected to OV, with the display off, the device will consume typically 750 μA.

Note 4. These voltages are adjusted to allow the use of thembwheel switches with the 7217.

Note 5. Typical running frequency can be as high as 5 MHz but guarantee input frequency is only 2 MHz.

Electrical characteristics $V_{DD} = 5V$, $T_A = 25°C$, display diode drop 1.7V, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply current (see note 3) (lowest power mode)	I_{min}	DISPLAY off, LC, DC, UP/DOWN $\overline{ST}$, $\overline{RS}$, BCD I/0 Floating or V_{DD}		350	500	μA
Supply current Supply Voltage	I_{OP}, 8's V_{DD}	Display on all '8's	175 4.5	200 5.0	 5.5	mA V
Digit driver output current Segment driver output current	I_{digit} $I_{segment}$	$V_{out} = V_{DD} - 2.2V$ $V_{out} = 1.3V$	175 −25	200 −40		mA mA
ST, RS, UP/DOWN input pull up current. (See note 3) 3 level input impedance	I_p	$V_{out} = V_{DD} - 2.0V$	5	25 100		μA kΩ
BCD I/0 input: HIGH voltage : LOW voltage	V_{BIH} V_{BIL}	(see note 4) (see note 4)		1.3	 0.8	V V
BCD I/0 input pull-up current BCD I/0, CARRY/BORROW, $\overline{ZERO}$, EQUAL output : HIGH current : LOW current	I_{BPU} I_{BOH} I_{BOL}	$V_{in} = V_{DD} - 2V$ (see note 3) $V_{OH} = V_{DD} - 1.5V$ $V_{OL} = 0.4V$	5 100 −2	25		μA μA mA
COUNT input frequency (See Note 5)	f_{in}	50% duty cycle $V_{DD} = 5V \pm 10\%$, −20°C to 70°C	0	5	2	MHz
COUNT input threshold	V_{TC}	$V_{DD} = 5V$		2		V
COUNT input hysteresis	V_{HC}	$V_{DD} = 5V$		0.5		V
DISPLAY SCAN oscillator frequency	f_{ds}	Free running, pin 13 open circuit		10		kHz

Table 1: Pin function details

Pin No.	Function	Logic Level	Condition
1	CARRY/BORROW	0→1	9999→0000 (up) 0000→9999 (down)
2	$\overline{\text{ZERO}}$	0	Count equals zero
3	$\overline{\text{EQUAL}}$	0	Count equals register
4	BCD I/O 2^3 MSB	N/A	depends on state of Load counter or Load register controls
5	BCD I/O 2^2	N/A	
6	BCD I/O 2^1	N/A	
7	BCD I/O 2^0 LSB	N/A	
8	COUNT INPUT	0→1	
9	$\overline{\text{STORE}}$	1	O/P latches NOT updated
		0	O/P latches updated
10	UP/DOWN	1	Counter counts up
		0	Counter counts down
11	LOAD REGISTER/ OFF	1	Register loaded via BCD I/0
		Floating	Normal operation
		0	Device inactive (Display drivers disabled)
12	LOAD COUNTER/ $\overline{\text{I/0 OFF}}$	1	Counter loaded via BCD I/0
		Floating	Normal Operation
		0	BCD port disabled
13	SCAN	N/A	May be overriden by external oscillator (Fig 6) or capacitor (Table 1)
14	$\overline{\text{RESET}}$	1	Normal operation
		0	Counter reset

Pin No.	Function	Logic Level	Condition
28	Digit 10^0	1	LSD digit select O/P
27	Digit 10^1	1	NMSD
26	Digit 10^2	1	NMSD
25	Digit 10^3	1	MSD
24	+V	–	–
23	Display Control	1	Segment drivers disabled
		Floating	Normal operation
		0	Leading zero blanking inhibited
22	$\overline{\text{g}}$	0	g segment O/P
21	$\overline{\text{b}}$	0	b segment O/P
20	OV	–	–
19	$\overline{\text{e}}$	0	e segment O/P
18	$\overline{\text{f}}$	0	f segment O/P
17	$\overline{\text{d}}$	0	d segment O/P
16	$\overline{\text{a}}$	0	a segment O/P
15	$\overline{\text{c}}$	0	c segment O/P

Description of operation

Outputs

The CARRY/BORROW output is a positive signal occurring typically 500ns after the positive going edge of the count input advancing the counter from 9999 to 0000 counting up and from 0000 to 9999 counting down. This output alows direct cascading of counters.

The $\overline{\text{EQUAL}}$ output assumes a low level when the contents of the counter and register are equal (i.e., for the duration of one period of the count input until the count is changed by a positive going edge on the count input).

The $\overline{\text{ZERO}}$ ouput assumes a low level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{\text{EQUAL}}$, and $\overline{\text{ZERO}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 2mA at 0.4V (on resistance 200 ohms), and for a logic one, the output sources >60μA.

The DIGIT and SEGMENT DRIVERS provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/seg. This corresponds to average currents of 10mA/seg with the 25% multiplex duty cycle. The DISPLAY CONTROL PIN controls the display output using three level logic. The pin is self-biased to a voltage approximately ½ V_{DD} which corresponds to normal operation. When this pin is connected to V_{DD}, the segments are inhibited, thus disabling the display and reducing power. When this pin is connected to 0V, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch as in the test circuits.

The BCD INPUT/OUTPUT PORT provides a means of transferring data into and out of the device in BCD format. The 7217 self-multiplexes data into the counter or register via thumbwheel switches in response to inputs at the LOAD COUNTER or LOAD REGISTER pins. When functioning as outputs, the BCD 1/0 pins will also drive one standard TTL load.

The onboard multiplex SCAN OSCILLATOR has a nominal free-running frequency of 10kHz. This may be reduced by the addition of a single capacitor between the scan pin and 0V, or the oscillator may be directly overdriven to about 20kHz. Capacitor values and corresponding nominal oscillators frequencies, digit repetition rates, are shown in Table 2.

The internal oscillator output has a duty cycle of typically 20:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks a four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, providing interdigit blanking (which prevents ghosting) and decoding and leading zero blanking decision time. The digits are scanned from MSD (10^3) to LSD (10^0).
See Fig. (1) for the display digit multiplex timing.

Figure 1 **Multiplex Timing**

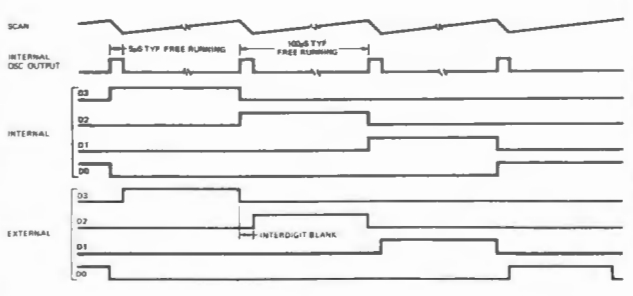


Table 2: Scan oscillator

Scan Capacitor	Nominal Oscillator Frequency	Digit Repetition Rate	Scan Cycle Time
None	10 kHz	2.5 kHz	400 μs
20 pF	5 kHz	1.2 kHz	800 μs
90 pF	1 kHz	250 Hz	4 ms

Table 3: Control input definitions

Input	Terminal	Voltage	Function
$\overline{\text{STORE (ST)}}$	9	V_{DD} (or floating) 0V	Output latches not updated Output latches updated
UP/DOWN (U/D)	10	V_{DD} (or floating) 0V	Counter counts up Counter counts down
$\overline{\text{RESET (RS)}}$	14	V_{DD} (or floating) 0V	Normal Operation Counter Reset
LOAD COUNTER	12	V_{DD} Floating 0V	Counter loaded with BCD data Normal operation BCD port forced to high impedance
LOAD REGISTER	11	V_{DD} Floating 0V	Register loaded with BCD data Normal operation Display drivers disabled, BCD port forced to high impedance, multiplex counter reset to $D10^3$, multiplex oscillator inhibited
DISPLAY CONTROL (DC)	23	V_{DD} Floating 0V	Segment drivers disabled Normal operation Leading zero blanking inhibited

Control

With the UP/DOWN pin at V_{DD}, the counter is incremented on the rising edge of the signal at the count input and with the up/down pin at OV, the counter is decremented on the rising edge of the count. A Schmitt trigger on the count input provides hysteresis to prevent double triggering on slow rising edges and to allow operation in noisy environments.

The $\overline{\text{STORE}}$ pin controls the internal latches and consequently the signals apearing at the 7 segment and BCD outputs. Bringing the store pin to 0V transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{\text{RESET}}$ pin to 0V. The COUNT INPUT is inhibited during reset and load counter operations. The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$ and UP/DOWN pins are provided with pullup resistors of approximately 75K.

The BCD I/O pins and the LOAD COUNTER (LC) & LOAD REGISTER (LR) pins combine to provide presetting & compare functions. LC and LR are three-level negative edge triggered inputs, being self-biased at approximately 1/2 V_{DD} for normal operation. If externally triggered, these inputs will initiate a full thumbwheel switch scan when pulsed HIGH for 500 ns. With both LC and LR open (self-biased) the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD with the display multiplex. In this mode of operation, the BCD pins will drive one TTL load (sink 2mA at 0.4V for logic low level). When either or both of the LC or LR pins is connected to V_{DD}, the TTL driver devices are turned off and the BCD pins become high-impedance inputs. When LC is connected to V_{DD}, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V_{DD} the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V_{DD}, the count is inhibited and both register and counter are preset. When LR is connected to 0V, the circuit powers down; the oscillator is inhibited, the BCD I/0 pins go to the high impedance state, and the segment state, and the segment and digit drivers are turned off, This allows the display to be used for other purposes and minimizes power consumption. In this powered down state, the circuit will continue to count, and the CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$, UP/DOWN, $\overline{\text{RESET}}$ and $\overline{\text{STORE}}$ functions operate as normal. When LC is connected to OV, the BCD 1/0 pins are forced to the high impedance state without disturbing the counter or register. See "Control Section" for a cataloguing of the pins that function as three-state self-biased inputs and their respective operations.

Output and input restrictions

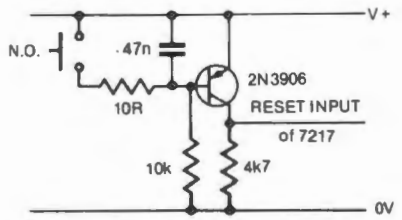
The CARRY/BORROW output is not valid during load counter and reset operations.

The $\overline{\text{EQUAL}}$ output is not valid during load counter or load register operations.

The $\overline{\text{ZERO}}$ output is not valid during a load counter operation.

The $\overline{\text{RESET}}$ input may prove to be susceptible to noise if its input rise time (coming out of reset) is more than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or C-MOS LOGIC) but in hardwired systems adding virtually any capacitance to the $\overline{\text{RESET}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{RESET}}$ input is shown below in Fig. 2.

Figure 2 **Reset Function**



Thumbwheel switches & multiplexing

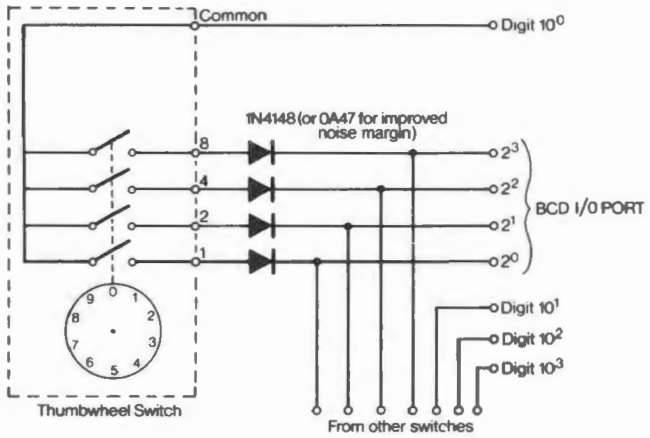
The correct type of thumbwheel switch to use with these circuits is a TRUE BCD coded switch, i.e. all switches open corresponds to 0000.

Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits and to ensure correct operation. See Figure 3.

In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops. Connection schematics for these diodes are shown in Fig. 3.

During load counter and load register operations the multiplex oscillator, is disconnected from the scan input and is allowed to free-run for the load operation. Under all other conditions the oscillator may be overdriven directly. When overdriving the oscillator, be aware that the internal oscillator output will be of the same duty cycle and phase as the overdriving signal and that the digits are blanked during the time the internal oscillator output is at a positive level. The blanking time should not be less than about 2μs to ensure proper leading zero blanking. By varying the duty cycle of the overdriving signal, the brightness of the display may be varied. The oscillator should not be overdriven at less than about 200Hz to prevent flickering of the display.

Figure 3 **Thumbwheel switch/diode configuration**



Displays

The RS 0.3 in, 0.43 in and 0.6 in common anode LED displays are all suitable for use with the 7217, whilst the four digit 0.5 in multiplexed display is perhaps the most convenient method due to the ease of connection. The brightness of the display may be altered by over-driving the multiplex oscillator using. the circuit shown in Fig. 4. (The inverters may be any C-MOS 4000B type e.g. 4001B).

Decimal points

A fixed decimal point may be implemented by connecting the d.p. segment pin from the appropriate digit to OV via a 39Ω resistor. In order to display leading zeroes after a fixed decimal point the circuit shown in Fig. 5. should be used, taking the control signal from the driver of the digit containing the d.p. for lefthand d.p. displays or from the next least significant digit for right hand d.p. displays.

Figure 4

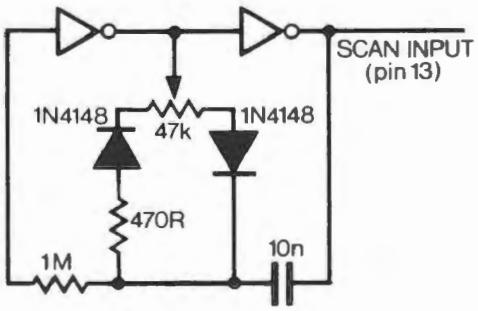
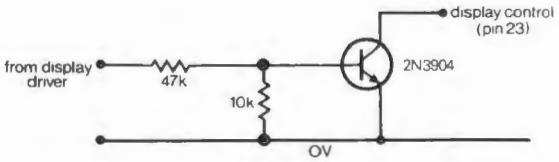


Figure 5

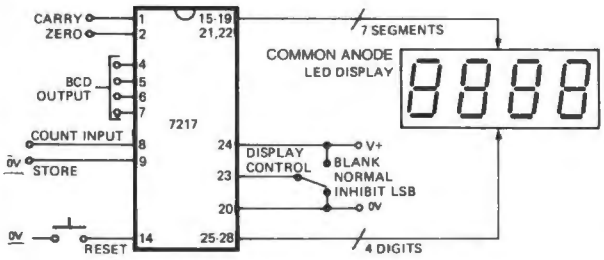


Applications

Unit counter with BCD output

The simplest application of the 7217 is as a 4 digit unit counter. All that is required is a 7217, a power supply and a 4 digit display. Add a momentary switch for reset and an SPDT centre-off switch to blank the display or view leading zeroes. One more SPDT switch gives up/down counting. (see Figure 6).

Figure 6 **Unit counter**

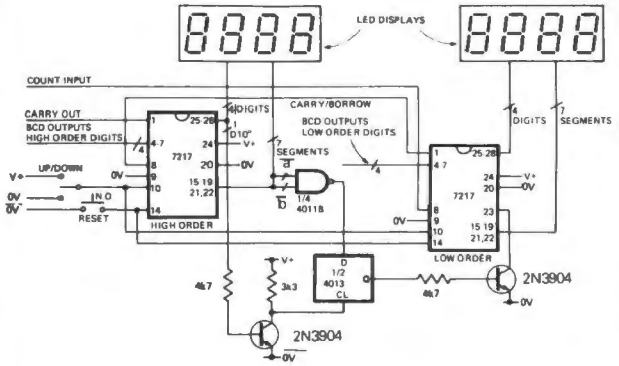


8-digit up/down counter

Figure 7 circuit shows how to cascade counters and retain correct leading zero blanking. The NAND Gate detects whether a digit is active since one of the two segments $\bar{a}$ or $\bar{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, so if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, inhibiting leading zero blanking on the low order counter.

The two devices can be equipped with separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize.

Figure 7 **Up/down counter**



Frequency counter/tachometer

The circuit figure 8 uses a 556 dual timer circuit to generate the gating, store and reset signals. One timer is configured as an astable multivibrator using RA, RB & C to provide an output (556 pin 5) that is high for approximately 1 second and low for approximately 300 —500μs to serve as a gating signal. The gating high time is given by GH = 0.7 (RA + RB) C while the gating low time is GL = 0.7 RBC. The system is calibrated by using a 4M7 potentiometer for RA as a "coarse" control and a 1k potentiometer for RB as a monostable triggered by the negative edge of the gating. This monostable output (556 pin 9) is gated with the astable output to give a short positive pulse at the store input, updating the display, followed by a short negative pusle at the reset input, resetting the counter in preparation for the next gate period. Note that the monostable period must always be at least 1.5 x the astable low time.

Figure 8
Frequency counter/tachometer

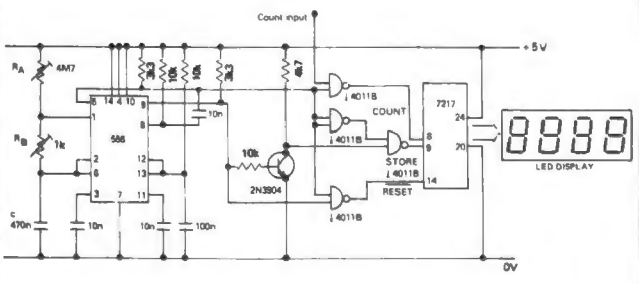
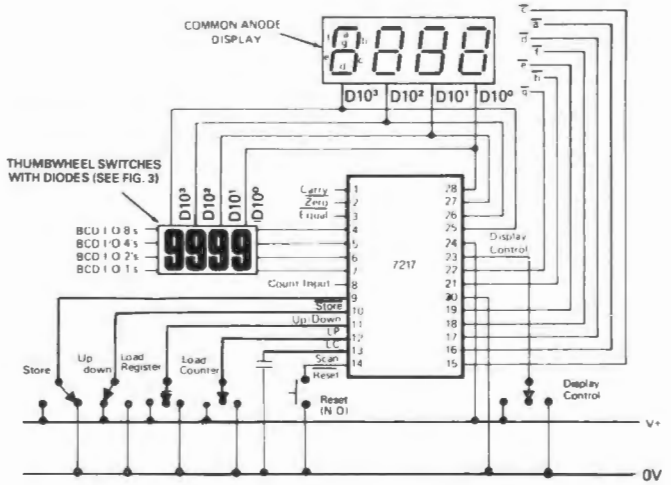


Figure 9 **Test circuit**



Note:
switches shown in normally biased conditions.

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RS data

Eurocard sub-rack systems

Please read this data sheet in full before assembling a sub-rack system.

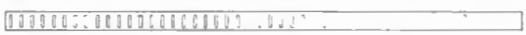
A versatile eurocard racking system in piece part form which is easy to assemble and simple to use. Two system sizes are available — 3U (5¼") high and 6U (10½") high. These are designed to house eurocards of dimensions 100 × 160mm, 100 × 220mm, 233.4 × 160mm and 233.4 × 220mm. Card front panels and modules may also be incorporated as required. The front and rear mounting rails are printed with location numbers 1 to 84 and the maximum usable width for both systems is 16.8 inches which corresponds to 84E (E = 0.2 inches, the basic pitch for eurocard systems).

Sub-rack kit 3U Stock number 508-879

Front mounting rails **Section**

Rear mounting rails **Section**

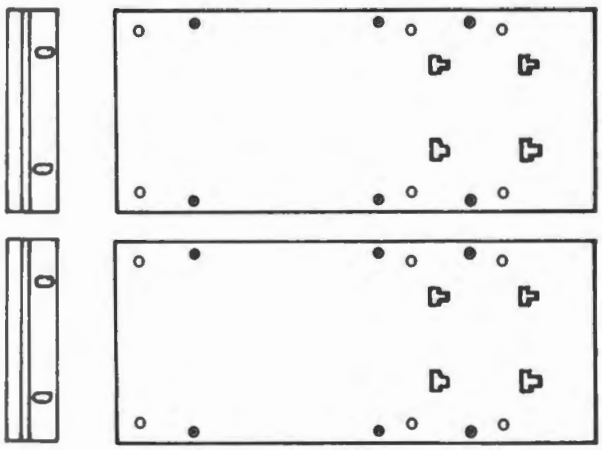
Guide location strips (Four supplied)



8 Posidriv (TM) self tapping screws

Tapped strips (Two supplied)

End plate angles **End plates**



Locking strips (Two supplied)

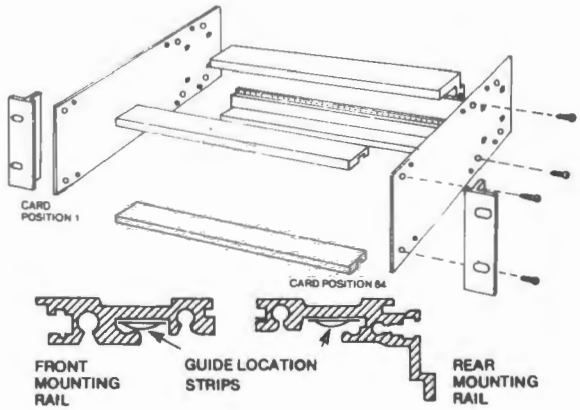
8 Posidriv (TM) self tapping screws

Assembly instructions

Attach the front mounting rails to one end plate and end plate angle with the self-tapping screws ensuring that the locating pips are correctly fitted into the rail extrusions. A no. 2 Supadriv| |screwdriver should be used and the tapping action will be aided by lubricating the threads. The two rear mounting rails are similarly attached using the front set of holes for 160mm length cards and the rearmost set for 220mm length cards. Slide the two locking strips into the front mounting rails, ensuring that the recessed channel is to the rear. Assemble the other end plate and angle to the rails. Place the four guide location strips into the front and rear mounting rails ensuring that the ends marked with black paint on one edge are all towards card position 1 (left hand side).

Note that 160mm and 220mm eurocards can be fixed in the same system (using 220mm. guides) but the front of the 160mm cards will be considerably recessed from the sub-rack face and therefore card fronts cannot be fitted. Modules may be used in a sub-rack system fitted with 220mm guides, but neither the 24 way plug and socket nor the indirect edge connector (for a card fitted into the side of a module) can be used.

Supadriv (TM) and posidriv etc.



Sub-rack kit 6U

Stock number 508-447

Front mounting rails

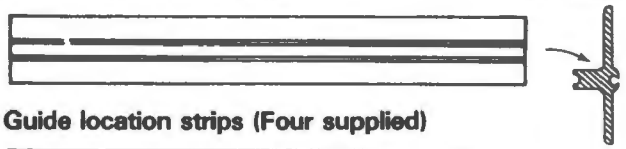
Section

Rear mounting rails

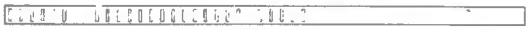
Section

Centre rear mounting rail

Section



Guide location strips (Four supplied)



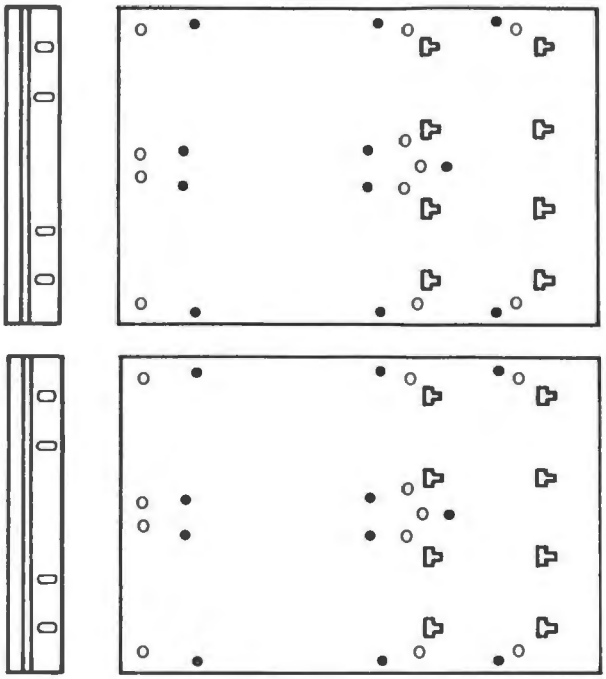
Tapped strips (Four supplied)

Locking strips (Two supplied)

10 Supadriv ⓣ self tapping screws

End plate angles

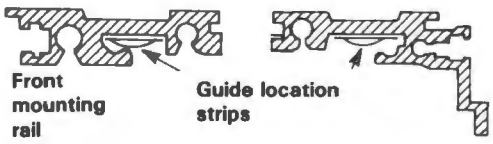
End plates

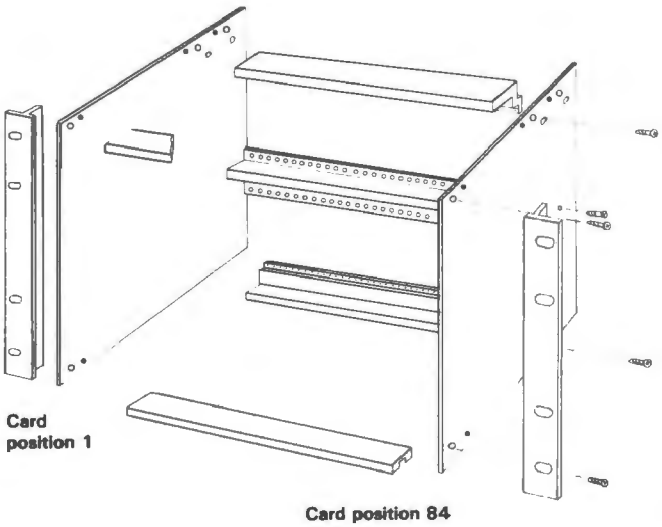


Assembly instructions

Attach the front mounting rails to one end plate and end plate angle with the self-tapping screws ensuring that the locating pips are correctly fitted into the rail extrusions. A no. 2 Supadriv ⓣ screwdriver should be used and the tapping action will be aided by lubricating the threads. The two rear mounting rails and centre rear rail are similarly attached using the front set of holes for 160mm length cards and the rearmost set for 220mm length cards. Slide the two locking strips into the front mounting rails, ensuring that the recessed channel is to the rear. Assemble the other end plate and angle to the rails. Place the four guide location strips into the front and rear mounting rails ensuring that the ends marked with black paint on one edge are all towards card position 1 (left hand side).

Note that 160mm. and 220mm eurocards can be fixed in the same system (using 220mm. guides) but the front of the 160mm cards will be considerably recessed from the sub-rack face and therefore card fronts cannot be fitted. Modules may be used in a sub-rack system fitted with 220mm guides, but neither the 24 way plug and socket nor the indirect edge connector (for a card fitted into the side of a module) can be used.





Guides

Module guides Stock number 508-857

Card guides '160mm' Stock number 508-863

Card guides '220mm' Stock number 508-734

The position and type of guide used depends on the number of cards, front panels and/or modules to be accommodated. If using cards only (without front panels) then a maximum of 28 can be fitted (with 64 way indirect edge connectors). This will give a clearance between cards of approximately 13mm for components. Allow two guides per eurocard and four guides per module.

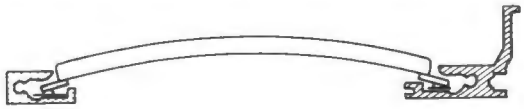
Cards use stepped guides

Modules use standard guides

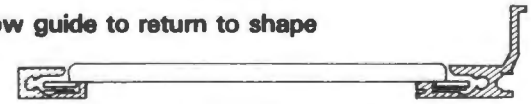
Guides are fitted to mounting rails as shown

Place one end into slot in mounting rail

Bow guide and insert other end into mounting rail



Allow guide to return to shape



Connector assembly instructions

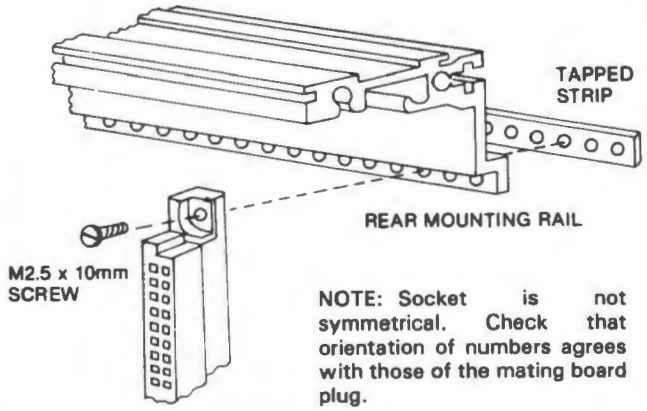
Indirect edge connectors (socket half) are inserted into the frame from the front so that they rest against the series of holes in the rear mounting rails, and an M2.5 × 10mm screw is threaded through the connector into the tapped strip as shown.

When fitting guides and connectors it is advisable to use an actual board with connector fitted, as the indirect edge connector fixing holes are offset from the centre line of the board guides.

Connector mounting screws

Used to mount indirect edge connector plugs and sockets and the mounting plate for module connectors.

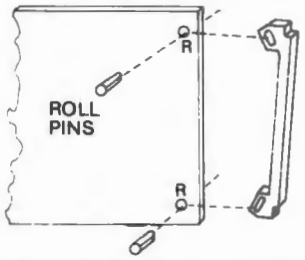
M2.5 screws 50 per pack. **Stock number 508-756**



NOTE: Socket is not symmetrical. Check that orientation of numbers agrees with those of the mating board plug.

Card handles **Stock number 508-762**

Drill two 1.5mm diameter holes in positions marked 'R' on the eurocard, place the handle over the card end and drive in two roll pins as shown.

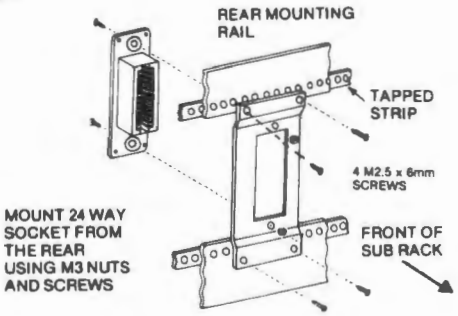


Modules 3U and 6U

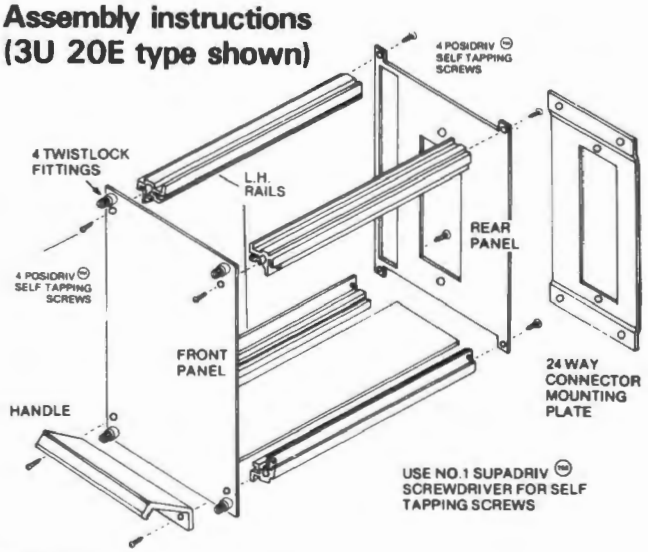
3U 10E Module	**Stock number 508-807**
3U 20E Module	**Stock number 508-813**
6U 10E Module	**Stock number 508-425**
6U 20E Module	**Stock number 508-431**

Available in 10E and 20E widths. The 20E rear panel is cut to accommodate a 24 way plug (467-009) and an indirect edge connector plug (mounted on a 160mm eurocard which slots into the left hand rails). The 10E width has a cut-out for an indirect edge connector only. The eurocard is held in place by threading the M2.5 × 12mm edge connector mounting screws through spacers into the rail extrusion tapped holes (screws and spacers supplied).

Note that 6U eurocards may be fitted with two additional plastic spacers (held with nylon screws) to prevent the card touching screening panel at the centre — spacers and screws supplied with screening kits, see below.



Assembly instructions (3U 20E type shown)



Note: Mount 24-way plug with flange inside module.

Centre handle for 6U modules is attached to the front panel with pan head M2.5 screws, nuts and washers.

24 way connector and mounting plate are fitted to the rear mounting rails as shown. Note that cut-out for 24 way plug is in lower half of 6U module.

Module screening kits

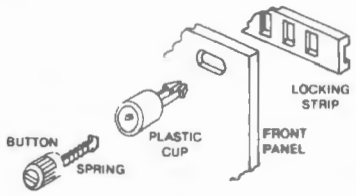
3U 10E Screening kit	**Stock number 508-784**
3U 20E Screening kit	**Stock number 508-790**
6U 10E Screening kit	**Stock number 508-403**
6U 20E Screening kit	**Stock number 508-419**

These consist of two side screens and a top screen which slide into the rail extrusions, the two side screens being retained by M2.5 screws (supplied) 6U kits also contain 2 plastic distance pieces and 4 nylon M3 screws.

RS data

Twist lock

Card fronts and modules are retained in the sub-rack by twistlock fittings. To assemble the fittings position the plastic cup with the internal peg towards card position 1 and push into the front panel from the front. Slide the spring over the metal shaft and push the button assembly (with rectangular bar vertical) through the cup and front panel ensuring that the peg locates in the button cut-out.

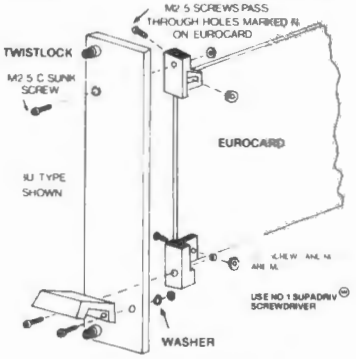


To lock front panels in place push the button in, rotate clockwise through 90° and release.

Card fronts 3U and 6U

3U 4E Card front	**Stock number 508-835**
3U 10E Card front	**Stock number 508-841**
6U 4E Card front	**Stock number 508-469**
6U 10E Card front	**Stock number 508-453**

Available in 4E and 10E widths. Assemble as shown. 6U types have additional centre handle.



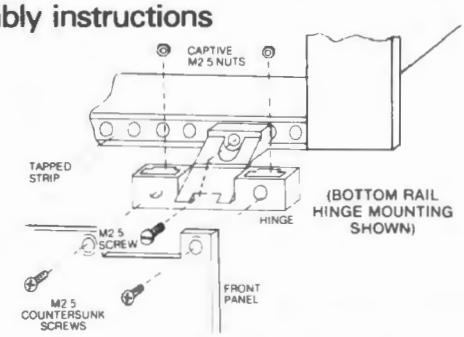
Hinged front panel 3U

Stock number 508-829

This front panel may be used to cover the front of a 3U sub-rack. It cannot be used where modules or card fronts are fitted. The front panel should be assembled to the sub-rack frame using the two plastic hinges and tapped strip sections provided and may be mounted to hinge from either the top or bottom mounting rails. Slide the tapped strip sections into the front mounting rails.

Note:
Only one locking strip is fitted into the appropriate mounting rails when using this panel.

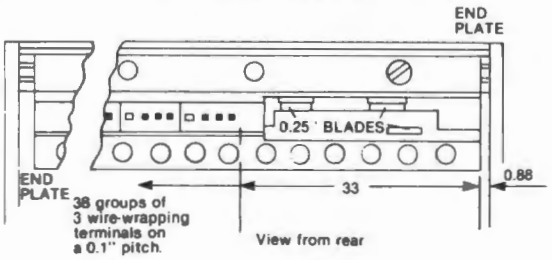
Assembly instructions

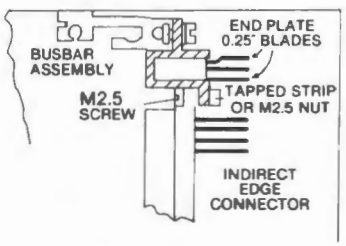


Busbar assembly

Stock number 508-627

The 3-rail busbar assembly may be incorporated in either eurocard sub-rack system by attaching to the rear mounting rail with M2.5 screws and nuts. End plate fixing and connector attachment is as shown in "Connector Assembly Instructions". Power input connections are 0.25" blade, output terminals are 0.6mm square wire-wrapping terminals.





Vertical distance from busbar wire-wrapping terminal to first connector terminal is 12.7mm. Suitable receptacles for the 0.25" blades RS Stock number 532-850, (250 (¼") receptacles).

R.S. Components Ltd. 13-17 Epworth Street, London, EC2P 2HA Telephone: 01-253 1222 or 01-250 4000
An Electrocomponents Group Company

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RS data

Universal counter i.c. 7216A

Stock number 307-941

The RS7216A Universal Counter IC is a fully integrated 8 digit universal counter, which combines a high frequency oscillator, a decade timebase counter, an eight decade data counter and latches, a seven segment decoder, digit multiplexers and eight segment and eight digit drivers which can directly drive large LED displays (e.g. 0·5'' multiplexed displays 587-024). The counter inputs have a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. However, the maximum frequency may be extended by use of prescaling techniques e.g. to increase the range to 50MHz a 74LS90 decade counter (307-610) may be used or to increase the range to at least 100MHz the RS÷100 Prescaler IC (307-474) may be employed. Both the inputs are digital inputs, and therefore in many applications the input signals will need amplification and level shifting to give the correct digital signals.

The RS7216A can function as a frequency counter, period counter, frequency ratio (F_A/F_B) counter, time interval counter or as a totalising counter. The counter normally uses a 10MHz quartz crystal timebase (but a 1MHz quartz crystal timebase is possible), in addition the timebase may be driven from an external oscillator. For period and time interval measurement, the 10MHz timebase gives a 0·1μ sec resolution. In period average and time interval average the resolution can be in the nano-second range. In the frequency mode, the user can select accumulation times of 0·01 sec, 0·1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to an accuracy of 0·1Hz in the least significant digit. There is 0·2 sec between measurements in all ranges.

The RS7216A incorporates leading zero blanking and automatic decimal point setting as the range is changed. The reading displayed is in kilohertz in the frequency modes and micro-seconds for the time measurement modes. The display is multiplexed at 500Hz with a 12·5% duty cycle for each digit with a typical peak segment current of 25mA. In the display off mode, both digit drivers and segment drivers are turned off allowing the display to be used for other functions if required.

A ready made p.c.b. (434-548) is available facilitating construction of a complete universal counter, including provision for ÷100 prescalers, time interval circuitry and p.c.b. rotary switches.

In addition a display p.c.b. (434-532) is available designed to accept eight 0·5'' seven segment LED displays and one 0·2'' discrete LED for overflow indication.

Features

- Functions as a frequency counter, period counter, unit counter, frequency ratio counter or time interval counter
- Four internal gate times: 0·01 sec, 0·1 sec. 1 sec, 10 sec in frequency counter mode
- 1 cycle, 10 cycles, 100 cycles, 1000 cycles in period, frequency ratio and time interval modes
- Measures period from 0·5μ sec to 10 sec
- Output drivers will directly drive both digits and segments of large LED displays
- Single nominal 5V supply required
- Stable high frequency oscillator, uses either 1MHz or 10MHz crystal
- Internally generated multiplex timing with interdigit blanking, leading zero blanking and overflow indication
- Decimal point and leading zero blanking controlled directly by the chip
- Display off mode turns off display and puts chip into low power mode
- Hold and reset inputs for additional flexibility
- All terminals protected against static discharge

Figure 1: **Pin connections**

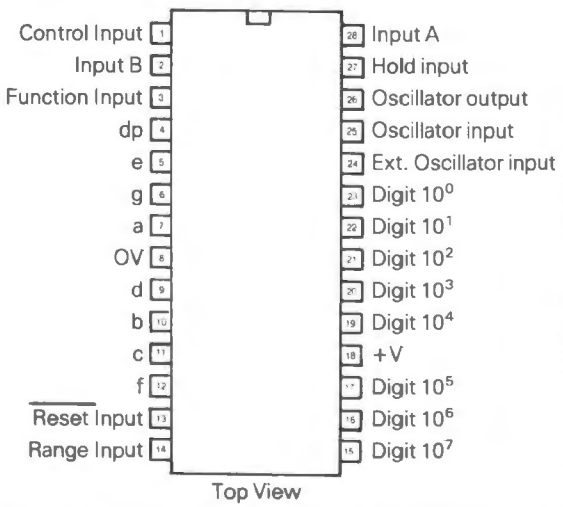
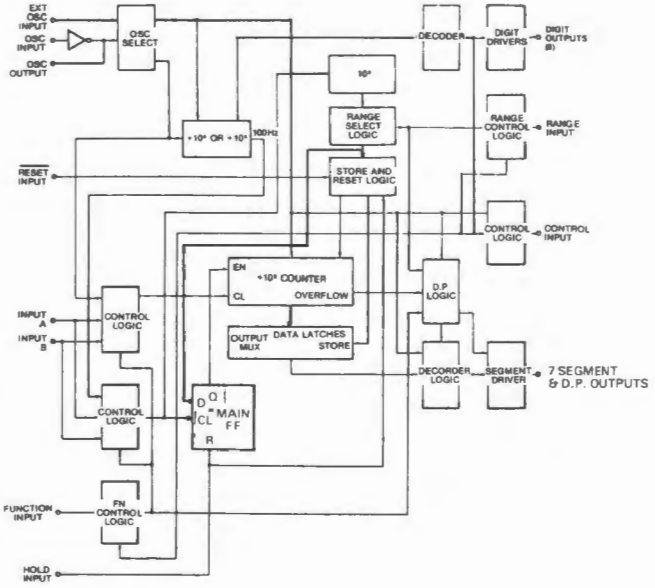


Figure 2: **Block diagram**



Absolute maximum ratings

Maximum supply voltage (+V) _____ 6.5V
Maximum digit output current _____ 400mA
Maximum segment output current _____ 60mA
Voltage on any input or output terminal [1] _____ +V+0·3V to —0·3V
Maximum operating temperature range _____ —20°C to +70°C
Maximum storage temperature range _____ —55°C to +125°C

Notes:

1. The RS7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding +V by more than 0·3V.

Figure 3: **Waveform for guaranteed minimum $F_{A\,MAX}$ function =frequency, frequency ratio, unit counter.**

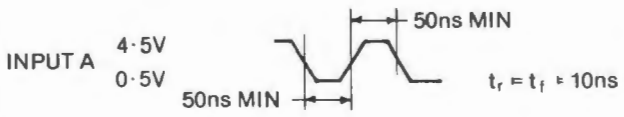


Figure 4: **Waveform for guaranteed minimum $F_{B\,MAX}$ and $F_{A\,MAX}$ for function = period and time interval.**

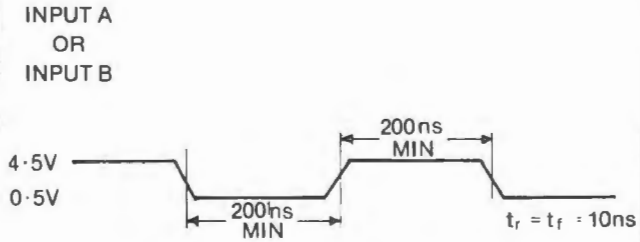
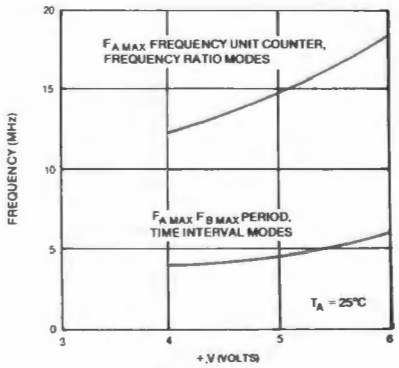


Figure 5: **Typical operating characteristics**



$F_{A\,MAX}$, $F_{B\,MAX}$ as a Function of +V

Electrical characteristics

Test conditions: +V=5·0V, Test Circuit, TA=25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Operating Supply Current	I_{DD}	Display Off, Unused Inputs to 0V		2	5	mA
Supply Voltage Range		$-20°C < T_A < +70°C$, Input A, Input B Frequency at F_{MAX}	4·75		6·0	V
Maximum Frequency Input A, Pin 28	F_A MAX	$-20°C < T_A < +70°C$ $4.75 < +V \leqslant 6·0V$, Figure 5 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2·5			 MHz MHz
Maximum Frequency Input B, Pin 2	F_B MAX	$-20°C < T_A < +70°C$ $4·75V < +V \leqslant 6·0V$ Figure 3	 2.5			 MHz
Minimum Separation Input A to Input B Time Interval Function		$-20°C < T_A < 70°C$ $4·75V < +V \leqslant 6·0V$ Figure 4	 250			 ns
Maximum Osc. Freq. and Ext. Osc. Frequency		$-20°C < T_A < +70°C$ $4·75 < +V \leqslant 6·0V$	 10			 MHz
Minimum Ext. Osc. Freq.					100	KHz
Multiplex Frequency	f_{max}	f_{OSC} = 10MHz		500		Hz
Time Between Measurements		f_{OSC} = 10MHz		200		ms
Input Voltages: Pins 2, 13, 25, 27, 28 Input Low Voltage	V_{IL}	$-20°C < T_A < +70°C$			1·0	V
Input High Voltage	V_{IH}		3·5			V
Input Resistance to +V Pins 13, 24	R	V_{IN} = +V -1·0V	100	400		kΩ
Input Leakage Pin 2,27,28	I_L				20	μA
Digit Driver: Pins 15, 16, 17, 19, 20, 21, 22, 23 High Output Current Low Output Current	I_{OH} I_{OL}	V_{OUT} = +V -2·0V V_{OUT} = +1·0V	—140	—180 +0·3		mA mA
Segment Driver: Pins 4, 5, 6, 7, 9, 10, 11, 12 Low Output Current High Output Current	I_{OL} I_{OH}	V_{OUT} = +1·5V V_{OUT} = +V -2·5V	25	35 -100		mA μA
Multiplex Inputs: Pins 1, 3, 14 Input Low Voltage Input High Voltage Input Resistance to +V	V_{IL} V_{IH} R	 V_{IN} = +1·0V	 +2·0 50	 100	0·8	V V kΩ

Applications notes

General

Inputs A and B

Inputs A and B are digital inputs with a typical switching threshold of 2·0V at +V=5·0V. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centred about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transition at both inputs.

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed inputs

The function, range and control inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The function, range and control inputs must be stable during the last half of each digit output (typically 125μsec). The multiplex inputs are active high for a common anode display. Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a

10kΩ resistor should be placed in series with the multiplex inputs and a 68pF capacitor to decouple the inputs to 0V as shown in figure 13.
Table 1 shows the functions selected by each digit for these inputs.

Control input functions
Display Test — All segments are enabled continuously, giving display of all 8's with decimal points. The display will be blanked if Display Off is selected at the same time.

Display Off — to enable the Display Off mode it is necessary to connect $D10^3$ to the control input and have the HOLD input at +V. The chip will remain in the Display Off mode until HOLD is switched back to 0V. While in the Display Off mode, the segment and digit driver outputs are open. During Display Off the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to 0V.

1 MHz Enable — The 1 MHz enable mode allows use of 1 MHz crystal with the same digit multiplex rate and time between measurements as with a 10 MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in μsec increments rather than 0·1 μsec increments.

External Oscillator Enable — In this mode the external oscillator input is used instead of the on-chip oscillator for Timebase input and Main Counter input in Period and Time interval modes. The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100 kHz or the chip will reset itself to enable the on-chip oscillator (The RS 10MHz crystal oscillator is ideally suited as an external oscillator).

Range Input — The range input selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter. In all functional modes except Unit Counter a change in the range input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Range Input is changed. (N.B. Readings displayed in kilohertz or microseconds)
Function Input — The six functions that can be selected are:
Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency.

These functions select which signal is counted into the Main Counter and which signal is counted by the reference counter as shown in Table 2. In Time Interval a flip flop is toggled first by a 1-0 transition of Input A then by a 1-0 transition of Input B. The oscillator is gated into the Main Counter from the time Input A toggles the flip flop until Input B gates the flip flop. (For complete description of workings of Time Interval see later section figure 18). A change in the function input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Function Input is changed.

Table 1

	Function	Digit
Function Input Pin 3	Frequency	$D10^0$
	Period	$D10^7$
	Frequency Ratio	$D10^1$
	Time Interval	$D10^4$
	Unit Counter	$D10^3$
	Oscillator Frequency	$D10^2$
Range Input Pin 14	·01 sec/1 hertz	$D10^0$
	0.1 sec/10 hertz	$D10^1$
	1 sec/100 hertz	$D10^2$
	10 sec/1k hertz	$D10^3$
Control Input Pin 1	Blank Display	$D10^3$ and Hold
	Display Test	$D10^7$
	1 MHz Enable	$D10^1$
	External Oscillator Enable	$D10^0$

Table 2

Description	Main Counter	Reference Counter
Frequency (FA)	Input A	100 Hz (Oscillator ÷ 10^5 or 10^4)
Period (TA)	Oscillator	Input A
Ratio (FA/FB)	Input A	Input B
Time Interval (A — B)	Osc (Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{OSC})	Oscillator	100 Hz (Oscillator ÷10^5 or 10^4)

Hold Input — When the Hold Input is at +V, any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. When Hold is changed to OV, a new measurement is initiated.
$\overline{\text{Reset}}$ Input — The $\overline{\text{Reset}}$ Input is the same as a Hold Input, except the latches for the Main Counter are enabled, resulting in an output of all zeros.

Display considerations

The display is multiplexed at a 500 Hz rate with a digit time of 244 μsec. An interdigit blanking time of 6 μsec is used to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays. Any zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the Main Counter overflows.

The RS7216 is designed to drive common anode LED displays at peak current of 25mA/segment, using displays with V_F=1·8V at 25mA. The average DC current will be over 3mA under these conditions. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 6, 7 and 8 show the digit and segment currents as a function of output voltage. (V_{OUT} referred to OV).

To obtain additional brightness from the displays, +V may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

Figure 6: **Typical I_{DIG} VS.**

+V—V_{OUT} (4·5V < +V < 6·0V)

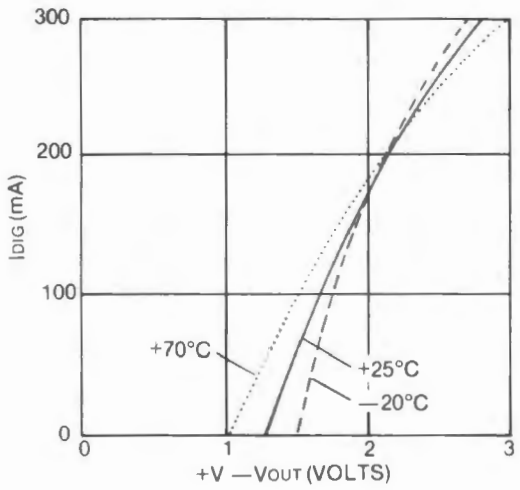


Figure 7: **Typical I_{SEG} VSV_{OUT} (+V varied)**

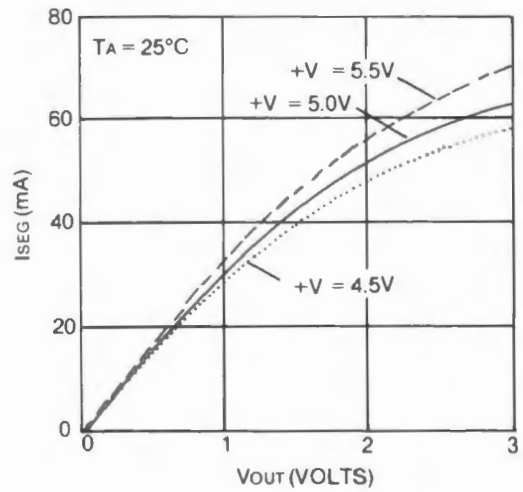
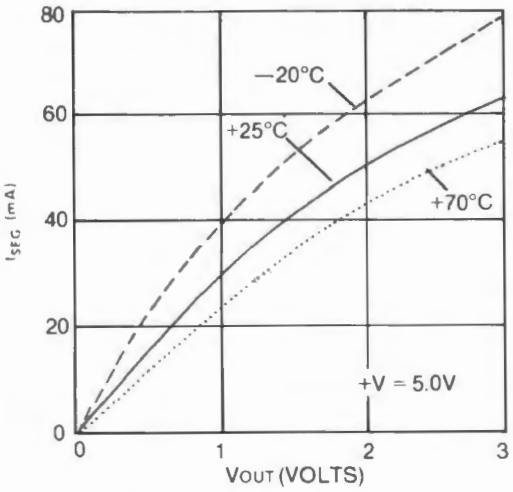
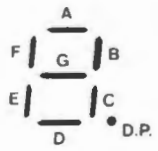


Figure 8: **Typical I_{SEG} VS.V_{OUT} (temperature varied)**



The segment and digit outputs in the RS7216 are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

Segment Identification:



N.B. The correct display to use with this device is a common anode with right hand decimal point e.g. RS multiplexed seven segment display Stock No 587-024.

Accuracy

In a Universal Counter crystal drift and quantization errors cause errors. In Frequency, Period and Time Interval modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the Frequency mode the maximum accuracy is obtained with high frequency inputs and in Period mode maximum accuracy is obtained with low frequency inputs. As can be seen in figure 9, the least accuracy will be obtained at 10 kHz. In Time Interval measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in figure 10. In Frequency Ratio measurement can be more accurately obtained by averaging over more cycles of Input B as shown in figure 11.

Figure 9: **Maximum accuracy of frequency and period measurements due to limitations of quantization errors**

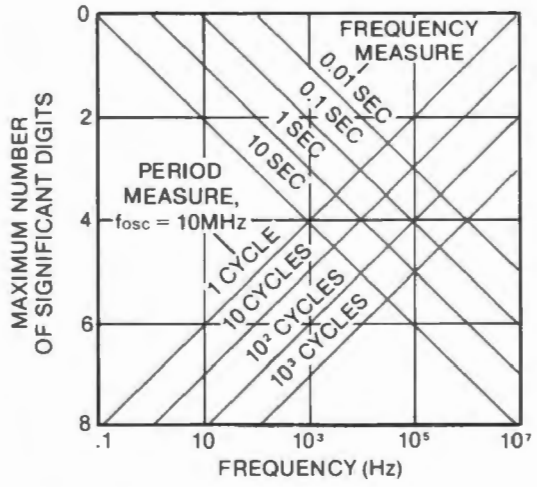


Figure 10: **Maximum accuracy of time interval measurement due to limitations of quantization errors**

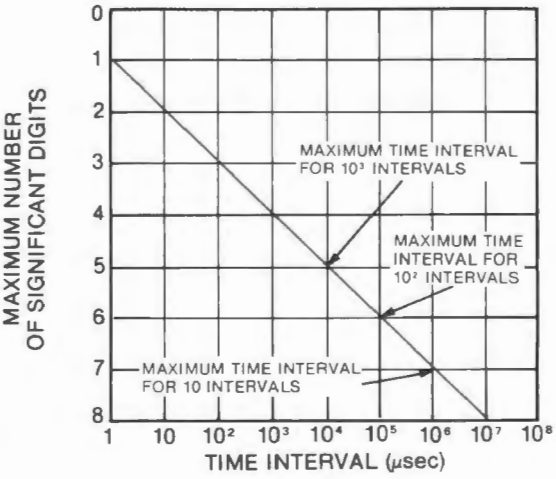
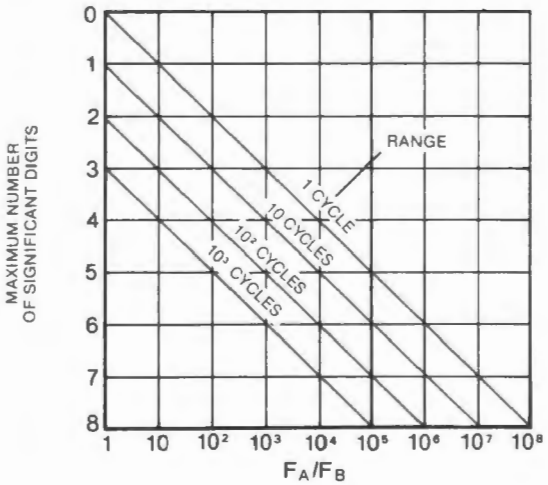


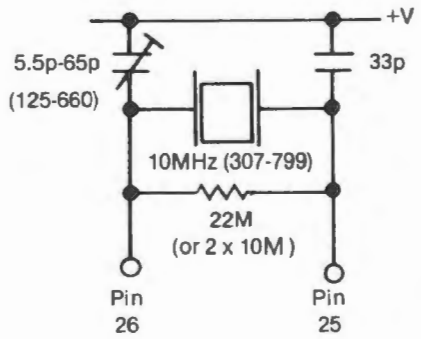
Figure 11: **Maximum accuracy for frequency ratio measurement due to limitation of quantization errors**



Oscillator considerations

The easiest way of implementing the timebase oscillator is to use a 10MHz crystal (307-799) and associated circuitry as shown in figure 12.

Figure 12: **Crystal oscillator circuit**



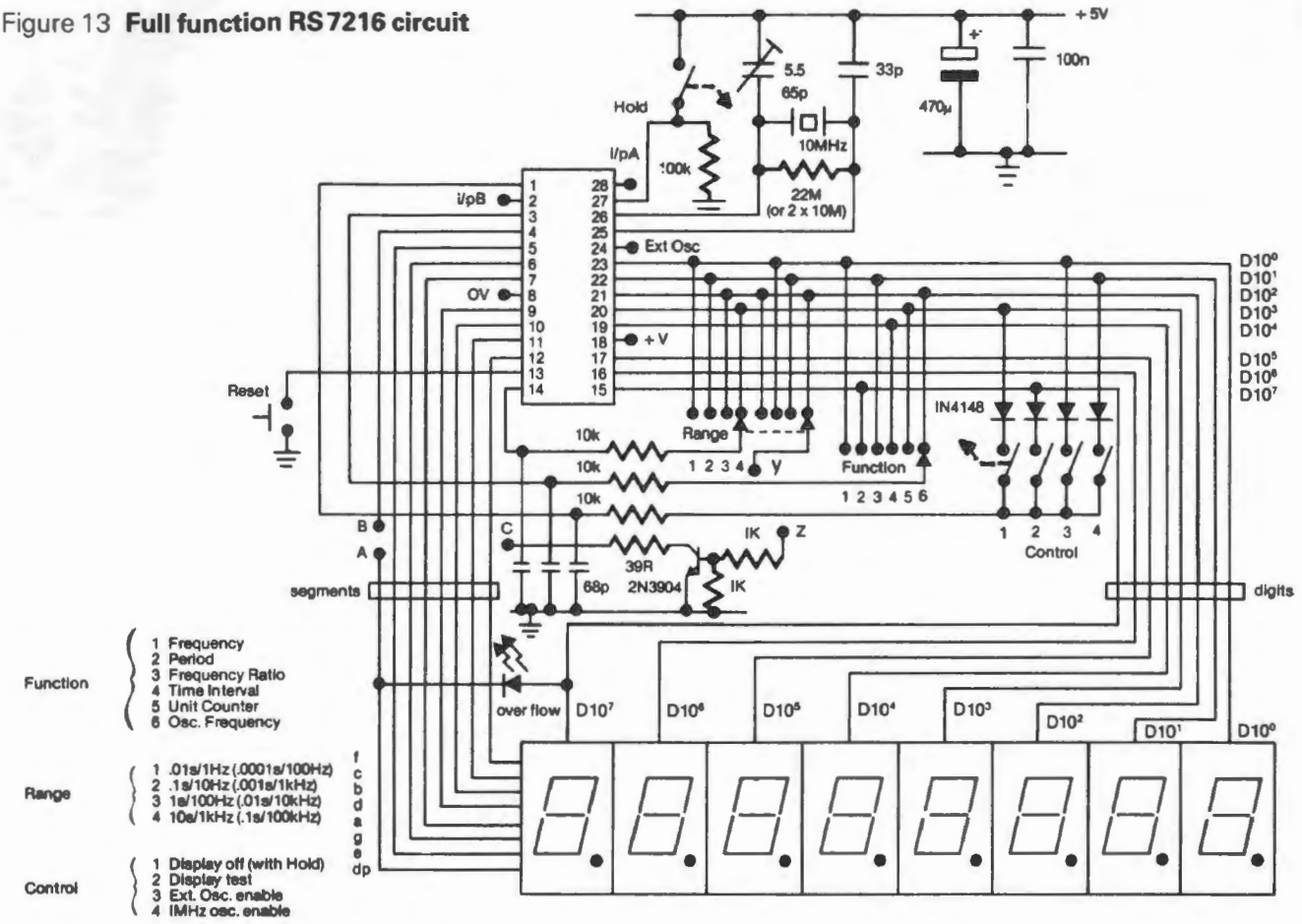
If the 1MHz enable option is to be used, this may be implemented simply by substituting a 1MHz crystal (307-761) for the 10MHz crystal in figure 12 and connecting the 1MHz enable control circuitry.

An external oscillator, e.g. the RS10MHz Crystal Oscillator may be used by connecting the oscillator output to pin 24 and connecting the external oscillator, enables control circuitry. (N.B. oscillator output must be input voltage criteria as detailed in maximum ratings and electrical characteristics sections.)

Circuit applications

The RS7216 has been designed for use in a wide range of Universal Counter applications. In many cases, prescalers will be required to reduce the input frequencies to under 10 MHz. Because Input A and Input B are digital inputs, additional circuitry will often be required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal. The complexity for doing this can vary widely depending on the sensitivity and maximum frequency required.

Figure 13 **Full function RS7216 circuit**



The display may be made up using two multiplexed displays (587-024)

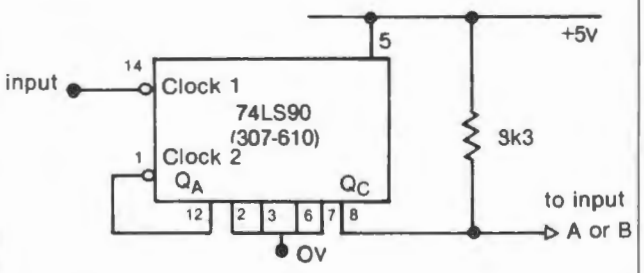
Prescaler techniques

For a full function Universal Counter two of these prescaler circuits will be required. Note that the input to the 74LS90 must be a digital circuit. If decimal point position correction is required see following section.

Note: The output from the 74LS90 comes from the Q_C rather than Q_D to obtain an input duty cycle of 40%. If the signals of inputs A or B have very low cycles it may be necessary to use a monostable (74LS123 or similar) to stretch the pulse width to guarantee a 50ns minimum pulse width.

Figure 14: **Divide by ten prescaler**

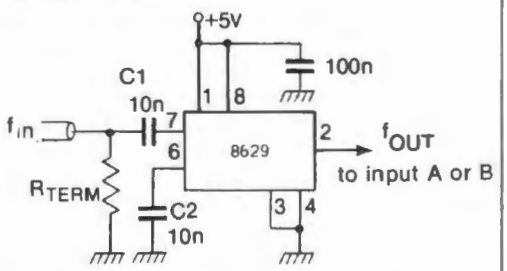
Prescaler ÷ 10 up to 50 MHz



Two circuits required for full functional counter.

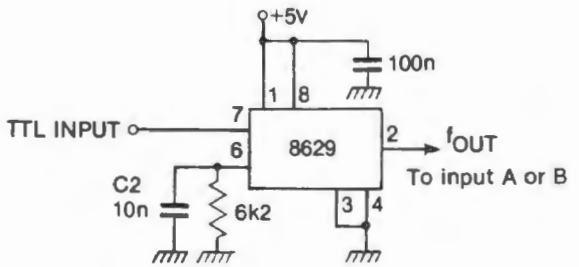
Figure 15: **Divide by 100 high frequency, single-ended input**

Prescaler ÷ 100 up to 150 MHz



Two circuits required for full functional counter.

Figure 16: **Divide by 100 TTL input ($DC < f_{in} < f_{max}$)**



Two circuits required for full functional counter.

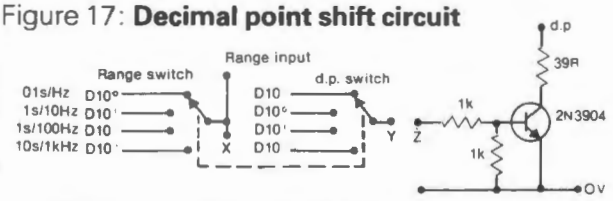
For further details of the RS8629, Stock No 307-474, see data sheet 3059.

RS data

Decimal point shift facility

When a prescaler is used, or for any other reason, it may be desirable to shift the decimal point. If a ÷10 prescaler is used, the decimal point should be moved one place to the right, and if a ÷100 prescaler is used, it would be moved two places to the right. This is to enable the display to remain reading in kilohertz or microseconds. The circuit below shows a method for achieving this function (N.B. the zero blanking cannot be changed and so one or two zeroes will appear to the left of the decimal point. Also when using the ÷100 prescaler on the 0·01 sec/1 hertz range, it is best to shift the decimal point one place to the left giving measurements in MHz and milliseconds but there may be a blanked digit to the right of the decimal point).

Figure 17: **Decimal point shift circuit**



÷ 10 prescaler : join X + Z; d.p. switch not required

÷ 100 prescaler : join Y + Z; d.p. switch ganged with range switch

Parts list for full function counter incorporating divide by 100 TTL inputs

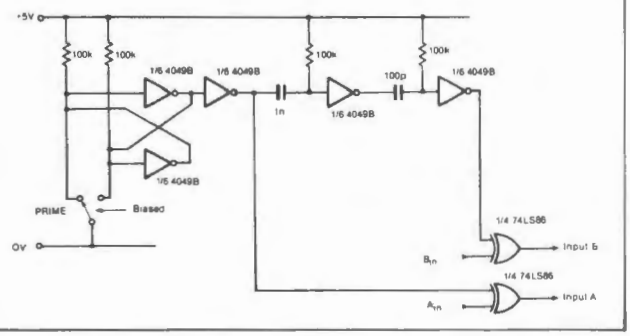
Device Type	Stock No.	Qty.
Semi-conductors		
7216A Counter	307-941	1
8629 Prescaler	307-474	2
74LS86 Input gate	307-604	1
4049B Shift register	306-667	1
IN4148 Diode	271-606	4
L.E.D.	587-822	1
7-segment display 0.5"	587-320	8
2N3904 Transistor	294-312	1
Crystal 10Mhz	307-799	1
Resistors		
39R metal film	148-152	1
1k metal film	148-506	2
6k2 metal film	148-685	2
10k metal film	148-736	3
100k metal film	148-972	5
22M thick film	158-171	1*
* May be replaced with 2 x 10M 133-330		
Capacitors		
5.5-65p trimmer	125-660	1
33p sub. min. plate ceramic	126-130	1
68p sub. min. plate ceramic	126-152	3
100p sub. min. plate ceramic	126-168	1
1n epoxy cased	125-676	1
10n epoxy cased	125-705	2
100n miniature layer	114-402	5
470μ 10V electrolytic	103-519	1

Time interval mode

The principal of operation of the time interval measurement is that the counter is started by channel A going negative and after the selected number of periods is stopped by channel B going negative. However the first pair of negative edges steers the circuit into this mode of operation and therefore when single shot measurements are to be made it is necessary to "prime" the circuit by a negative going A input followed by a negative going B input (separated by at least 250ns and complying with the specified input characteristics as shown in figure 4).

This priming procedure may be accomplished using the circuit shown in figure 18, but not that it may be necessary to reset the counter before priming. After 'priming', the circuit will count the selected number of periods and display the result as an 'Average'. This priming circuit has no effect on the operation of the universal counter in other modes and may therefore be left permanently connected. (N.B. 'Priming' is not necessary if a repetitive measurement is to be made.)

Figure 18: **Priming circuit for single shot operation time interval mode**



Device Type	Stock No.	Qty.
Miscellaneous		
Priming switch	317-027	1
Reset switch	336-747	1
Hold switch	316-989	1
Range switch – mechanism	327-686	1
– 2 pole, 6 way wafer	327-709	1
– spacer	327-715	1
Function switch – mechanism	327-686	1
– 1 pole, 12 way wafer	327-692	1
– spacer	327-715	1
Control switches	316-973	3
BNC socket-printed circuit	456-093	4
4 way p.c.b. straight plug	467-560	6
5 way p.c.b. straight plug	467-576	1
4 way cable shell	467-611	10
5 way cable shell	467-627	1
4 way angled plug	468-080	1
8 pin D.I.L. socket	402-298	2
14 pin D.I.L. socket	402-305	1
16 pin D.I.L. socket	402-311	1
28 pin D.I.L. socket	402-333	1
Printed circuit board – control	434-484	1
Printed circuit board – display	434-532	1

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RS data

Keyboard-switch encoder I.C. RS 74C922

Stock number 307-907

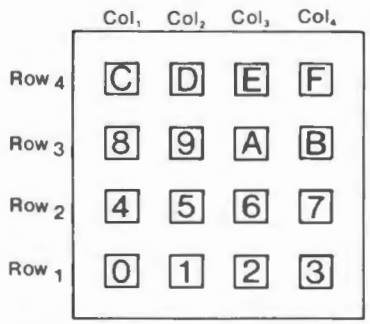
The RS 74C922 Keyboard Encoder I.C. provides all the necessary logic to fully encode an array of 16 SPST switches into binary. The keyboard scan may be implemented by the internal clock by use of an external capacitor, or may be overdriven by an external clock. An on-chip pull-up device permits switches with up to 50kΩ 'on'-resistance to be used. No diodes are needed to eliminate ghosting and an internal debounce circuit is incorporated which needs only a single capacitor to function (this facility may be disabled by omitting the capacitor). The Data Available output goes high when a keyboard entry is made and returns to a low when the key is released, even if another key is depressed. The Data Available output will return to a high to indicate acceptance of the new key after a normal debounce period; this two key rollover is provided between any two switches. An internal register stores the last key pressed even after the key is released. The tri-state outputs provide for easy expansion and bus operation and are Low Power Schottky TTL compatible (i.e. they will each drive one LPSTTL input).

Features

- 50 kΩ maximum switch 'on' resistance
- On or off chip clock
- On-chip row pull up devices
- 2 key roll over
- Keybounce elimination with single capacitor
- Last key register at outputs
- Tri-state outputs LPSTTL compatible
- Wide supply range (3V to 15V)
- Low power consumption

A suitable low profile keyboard is available, RS stock No. 337-100, see figure 1 below.

Figure 1 **Connection to RS low profile keyboard (337-100)**



Connections

	Switch Pin No.	RS74C 922 Pin No.
Row4	1	4
Column 1	2	11
Column 2	3	10
Row 1	4	1
—	5	—
Row 2	6	2
Column 3	7	8
Column 4	8	7
Row 3	9	3

Typical applications

Figure 2 **Synchronous Handshake**

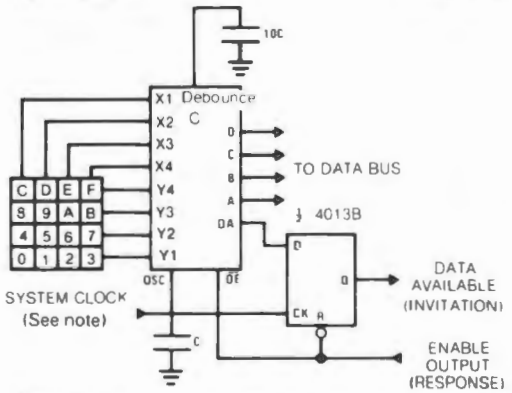
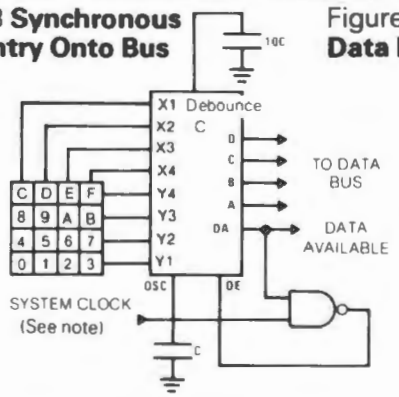
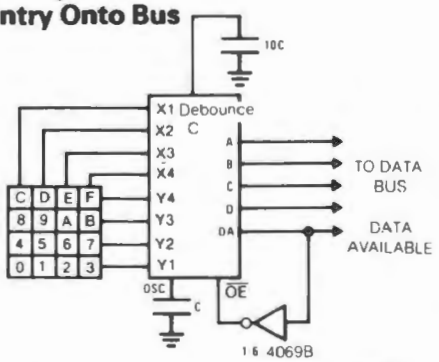


Figure 3 **Synchronous Data Entry Onto Bus**



Outputs are enabled when valid entry is made and go high impedance when keys released

Figure 4 **Asynchronous Data Entry Onto Bus**



Outputs are high impedance until key is pressed then data is placed on bus
When key is released outputs return to high impedance

Note 3: The keyboard may be synchronously scanned by omitting the capacitor at osc, and driving osc. directly, if the system clock rate is lower than 10 kHz.

Figure 5 **Pin connections**

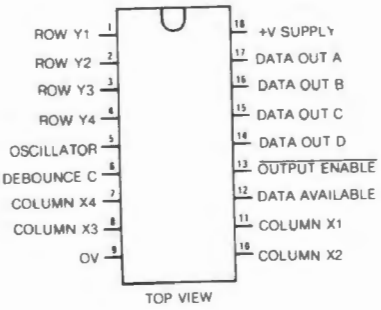
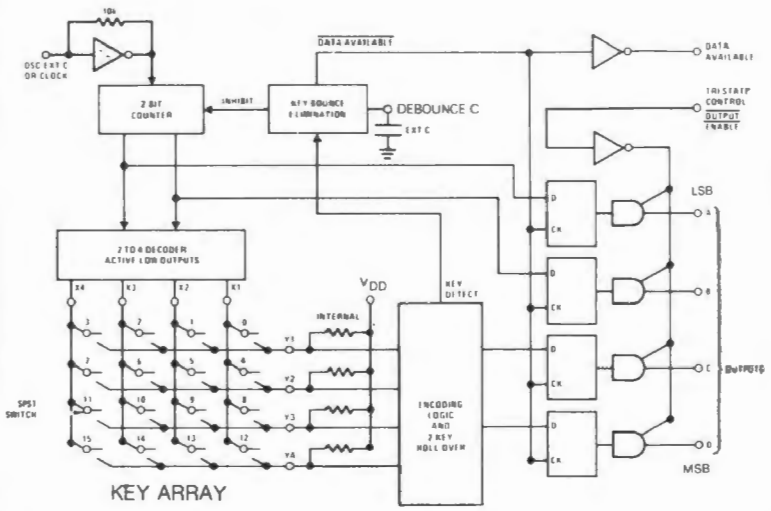


Figure 6 **Block diagram**

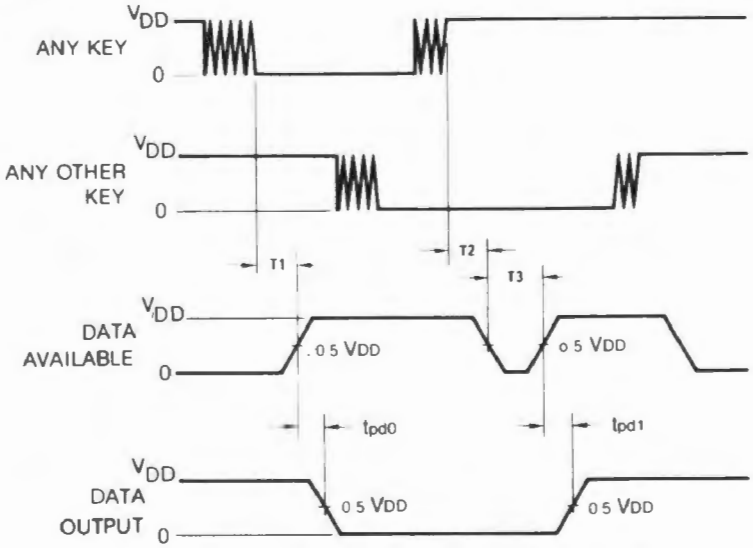


Truth table

SWITCH POSITION	0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4
DATA OUT A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
DATA OUT B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
DATA OUT C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
DATA OUT D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

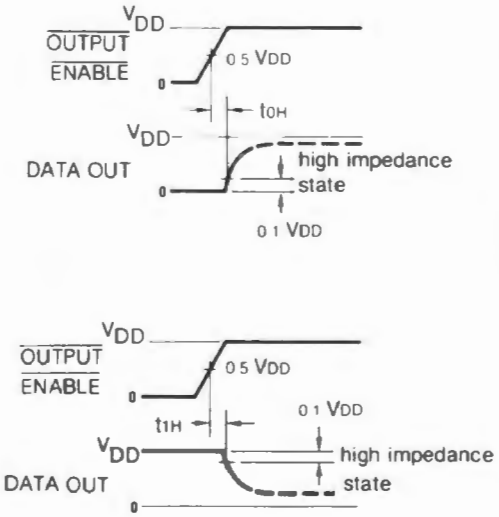
Switching time waveforms

Figure 7



T1 ≈ T2 ≈ RC, T3 ≈ 0.7 RC where R = 10kΩ and C is external capacitor at debounce input.

Figure 8



Absolute maximum ratings

Voltage at Any Pin —V_{DD}—0.3V to V_{DD} +0.3V
Operating Temperature Range —40°C to +85°C
Storage Temperature Range —65°C to +150°C
Package Dissipation 500 mW
Operating V_{DD} Range (+V supply) 3V to 15V
V_{DD} max 18V
Lead Temperature (Soldering, 10 seconds) 300°C

DC Electrical characteristics

Min/max limits apply across temperature range unless otherwise noted

Parameter		Conditions	Min	Typ	Max	Units
CMOS to CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and Debounce inputs	V_{DD} = 5V, $I_{IN} \geq$0 7mA V_{DD} = 10V, $I_{IN} \geq$1 4mA V_{DD} = 15V, $I_{IN} \geq$2 1mA	3 6 9	3 6 6 8 10	4 3 8 6 12 9	V V V
V_{T-}	Negative-Going Threshold Voltage at Osc and Debounce inputs	V_{DD} = 5V, $I_{IN} \geq$0.7mA V_{DD} = 10V, $I_{IN} \geq$1 4mA V_{DD} = 15V, $I_{IN} \geq$2 1mA	0 7 1 4 2 1	1 4 3 2 5	2 4 6	V V V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and Debounce inputs	V_{DD} = 5V, V_{DD} = 10V, V_{DD} = 15V,	3 5 8 12 5	4 5 9 13 5		V V V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and Debounce inputs	V_{DD} = 5V, V_{DD} = 10V, V_{DD} = 15V,		0 5 1 1 5	1 5 2 2 5	V V V
I_{rp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 inputs	V_{DD} = 5V, V_{IN} = 0 1 V_{DD} V_{DD} = 10V V_{DD} = 15V,		—2 —10 —22	—5 —20 —45	µA µA µA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{DD} = 5V, I_O = —10µA V_{DD} = 10V, I_O = —10µA V_{DD} = 15V, I_O = —10µA	4 5 9 13 5			V V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{DD} = 5V, I_O = 10µA V_{DD} = 10V, I_O = 10µA V_{DD} = 15V, I_O = 10µA			0.5 1 1 5	V V V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{DD} = 5V, V_O = 0 5V V_{DD} = 10V, V_O = 1V V_{DD} = 15V, V_O = 1 5V		500 300 200	1400 700 500	Ω Ω Ω
I_{DD}	Supply Current	V_{DD} = 5V, Osc at 0V V_{DD} = 10V V_{DD} = 15V		0 55 1 1 1 7	1 1 1 9 2 6	mA mA mA
$I_{IN(1)}$	Logical "1" Input Current at Output Enable	V_{DD} = 15V, V_{IN} = 15V		0 005	1 0	µA
$I_{IN(0)}$	Logical "0" Input Current at Output Enable	V_{DD} = 15V, V_{IN} = 0V	—1 0	—0 005		µA
CMOS/LPSTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and Debounce inputs	V_{DD} = 4 75V	V_{DD} —1 5			V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and Debounce inputs	V_{DD} = 4 75V			0 8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{DD} = 4 75V, I_O = 360µA	2 4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{DD} = 4 75V, I_O = 360µA			0 4	V
I_{SOURCE}	Output Source Current (P-Channel)	V_{DD} = 5V, V_{OUT} = 0V, T_A = 25°C	—1 75	—3 3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{DD} = 10V, V_{OUT} = 0V, T_A = 25°C	—8	—15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{DD} = 5V, V_{OUT} = V_{DD} T_A = 25°C	1 75	3 6		mA
I_{SINK}	Output Sink Channel (N-Channel)	V_{DD} = 10V, V_{OUT} = V_{DD}, T_A = 25°C	8	16		mA

AC Electrical characteristics TA = 25°C

Parameter		Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1},	Propagation Delay Time to Logical "0" or Logical "1" from D.A.	C_L = 50 pF (*Figure 7*) V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		 60 35 25	 150 80 60	 ns ns ns
t_{0H}, t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	R_L = 10kΩ, C_L = 5 pF, (*Figure 8*) V_{DD} = 5V R_L = 10k V_{DD} = 10V C_L = 10 pF V_{DD} = 15V		 80 65 50	 200 150 110	 ns ns ns
t_{H0}, t_{H1}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	R_L = 10kΩ, C_L = 50 pF, (*Figure 8*) V_{DD} = 5V R_L = 10k V_{DD} = 10V C_L = 50 pF V_{DD} = 15V		 100 55 40	 250 125 90	 ns ns ns
C_{IN} C_{OUT}	Input Capacitance Tri-state Output Capacitance	Any Input, (Note 2) Any Output, (Note 2)		5 10	7.5	pF pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

RS data

Typical performance characteristics

Figure 9 **Typical Irp vs V_{IN} at any Y input**

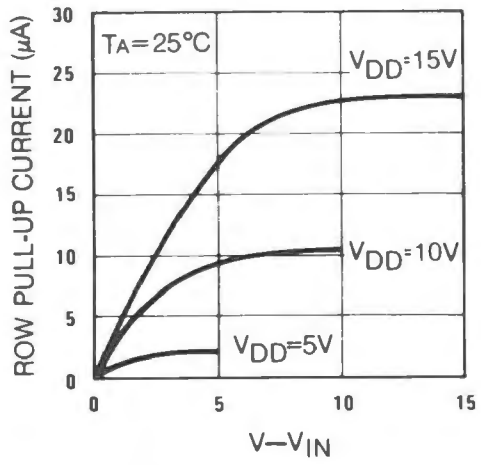


Figure 10 **Typical F_{SCAN} vs C_{OSC}**

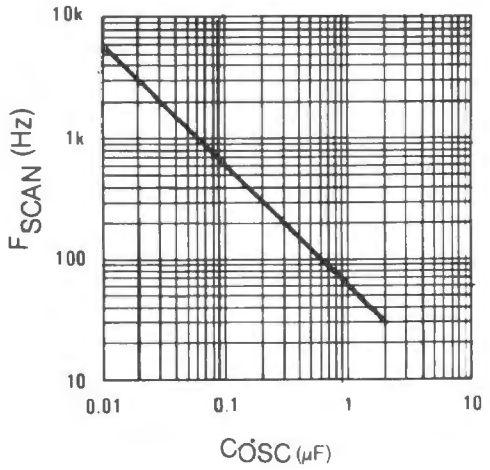


Figure 11 **Typical R_{on} vs V_{OUT} at any X output**

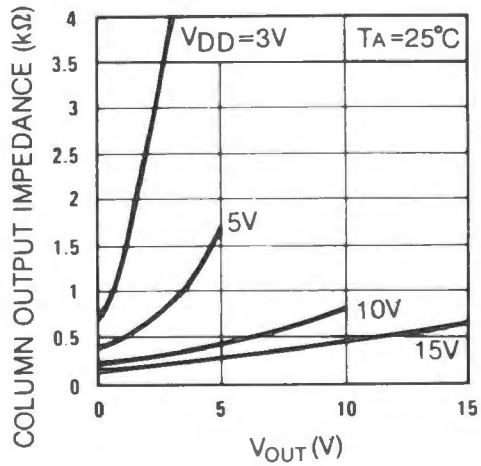
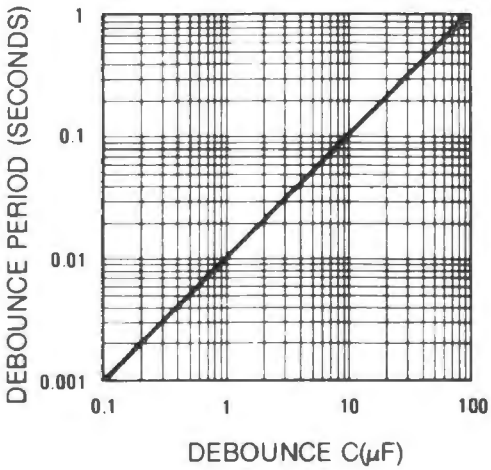


Figure 12 **Typical Debounce Period vs Debounce C**



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RS data

Thermal sensors

Stock numbers 307-929 and 935

Two solid state thermal sensors, having very sensitive active areas of metal oxide material produced by thin film techniques. They exhibit a high negative temperature coefficient of resistance within a narrow temperature band called the transition temperature region and a relatively small resistance change outside the region. Each sensor, encapsulated in a T092 plastic package with an isolated mounting tab, will quickly change resistance from approximately 100 kΩ down to approximately 100 Ω when heated through its specified transition temperature region. A similar characteristic is followed when cooling, but with a rapidly increasing resistance. Suitably applied, these devices are ideal for many temperature and power control applications.

Features

- High sensitivity
- High off/on impedance ratio
- Low noise (no mechanical contacts)
- Low shunt capacitance
- Small physical size
- Excellent reliability

Absolute maximum ratings

Working temperature range ——— 0°C to 120°C

Continuous current ——— See below† (Junction temperature)

Power dissipation (T_{case} = 25°C) ——— 310 mW*

Voltage proof lead to tab ——— 1500 V d.c.

* Derate linearly to zero power at 120°C.

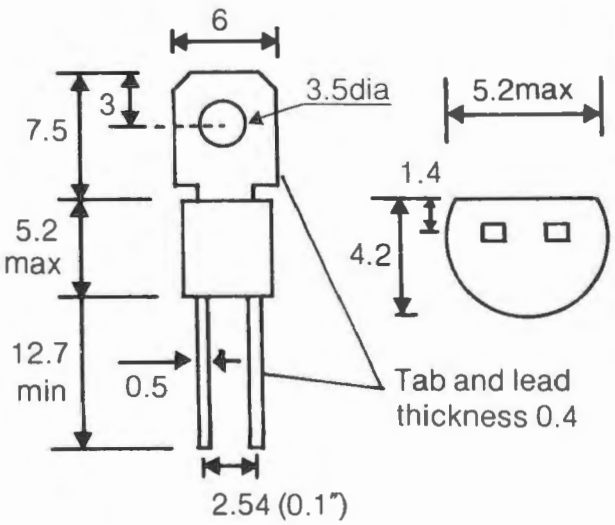
† Maximum continuous operating current is limited by several factors defined in the basic formula:

$T_{junction} = (P_D \times 180) + T_{case}$

where $T_{junction}$ n is the junction temperature.
P_D is the I^2R power dissipated by the device.
T_{case} is the device case temperature.

Note: $T_{junction}$ must NOT exceed 120°C.

Dimensions



Thermal characteristics

		T57 (307-929)	T75 (307-935)
Transition temperature		57°C	75°C
Typical temperature coefficient (% per °C).	pre-transition	−2	−3.5
	transition	−100	−70
	post-transition	−0.25	−1

General characteristics

Type	Parameter	Temp °C	Min	Typ	Max	Units
T57 (307-929)	Resistance	35	35	85	230	kΩ
	Resistance	57		1.0		kΩ
	Resistance	75	15	45	100	Ω
	Latching current*		0.6	1.8	3.2	mA
	Sensitivity	57	40	100		%/°C
T75 (307-935)	Resistance	55	40	80	300	kΩ
	Resistance	75		3.0		kΩ
	Resistance	95	20	115	200	Ω
	Latching current*		0.7	1.9	3.1	mA
	Sensitivity	75	50	70		%/°C
T57 AND T75	Thermal Resistance					
	Die to tab			170		°C/W
	Tab to air			150		°C/W
	Time Constant					
	Air to tab			35		s
	Tab to die			0.5		s
	Shunt Capacitance					
	Lead to lead			0.2		pF
	Lead to tab			0.8		pF

*See circuit considerations.

Figure 1: **Resistance – temperature characteristics**

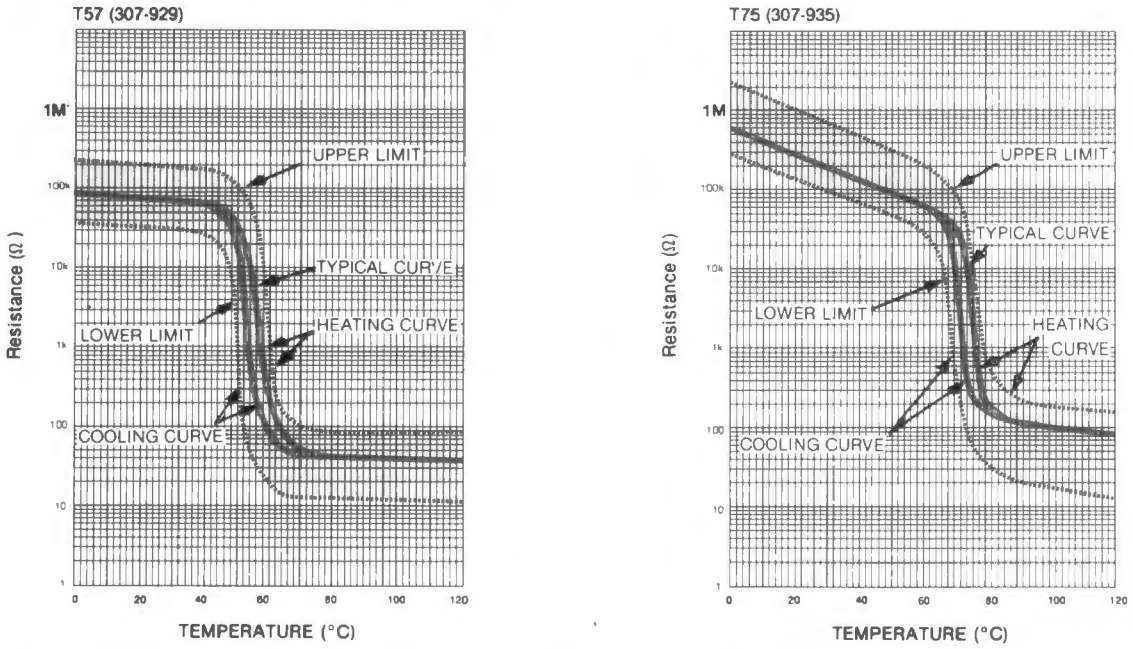
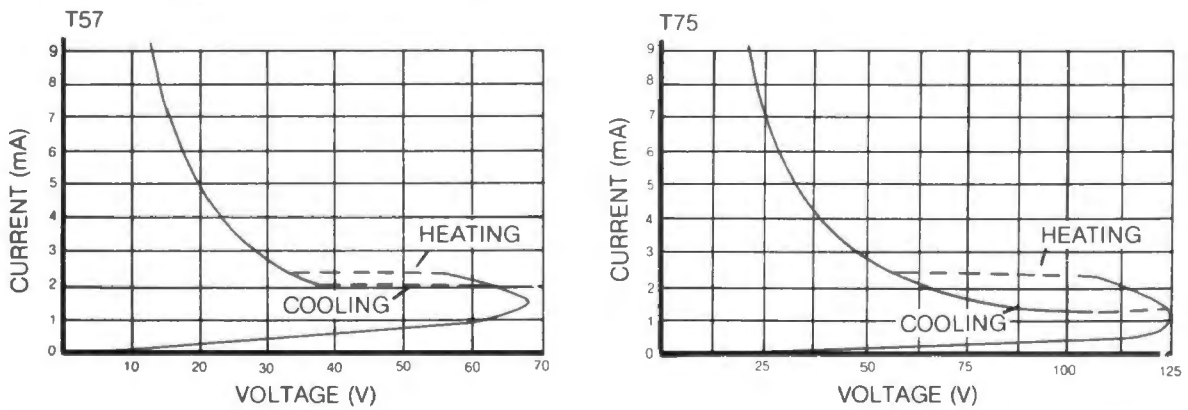


Figure 2: **Typical voltage – current characteristics**



Design considerations

The four most important factors in a design using these sensors are: (not necessarily in order of importance).

1. Temperature of operation
2. Physical mounting procedure
3. Circuit considerations
4. Mode of operation.

Temperature of operation

Below its transition temperature a sensor has very little effect on normal circuit operation owing to its high impedance, and being purely resistive in nature it exhibits negligible reactive effects. As the device approaches the temperature at which it becomes active it begins to respond with increasing sensitivity. Resistance changes rapidly with temperature when either heating or cooling. There is an inherent hysteresis, which means that the device will require a slightly higher temperature (4–6°C depending on type) to reach a given resistance level on heating than when it is cooled. This is seen on the response characteristics shown on Page 2 which demonstrates the resistance level for a variety of heating and cooling cycles. Calibration is not required because the transition temperature is an inherent material characteristic. A rearrangement of the crystal structure in the material always occurs at the same temperature for any given piece of material.

Physical mounting procedure

In order to provide reliable and predictable temperature sensing a low thermal resistance path between sensor and sensing point is essential. The use of silicone based compound (RS Stock number 554-311 is recommended.)

Circuit considerations

Since the sensor is a solid state active device whose characteristics change dramatically with temperature it is important to consider and determine the current flow through the device under all conditions. The most critical is the magnitude of voltage across the device and current through it after it passes through transition. Care should be taken not to exceed maximum power dissipation, or minimum latching current under normal operation as specified in general characteristics. The minimum latching current is the smallest current that will cause the sensor to make step changes in resistance when following the normal cooling characteristic.

The device may also latch or stay in its low resistance state due to self heating caused by high current and will switch to its high resistance state only after significant cooling has occurred. However, latching may be a desirable feature in certain applications, such as the shutting down of equipment until it has cooled to a safe operating temperature.

Latching must be considered in conjunction with the basic formula for junction temperature Page 1.

A further factor to be considered is that since these are low current devices, they may be damaged by fast surge current pulses. A small capacitance across the device represented by long lead lengths could be discharged into the device in its low resistance state resulting in device failure. It is recommended therefore that a series resistance of between 300 and 500 ohms be fitted, should long lead lengths be necessary.

Mode of operation

There are two common modes of operation:

1. Normal mode in which a sensor will follow its resistance temperature characteristics (see Page 2) unaffected by circuit operation.
2. Latching mode in which a circuit is designed to pass a current through a sensor in its low resistance state such that the power dissipation in the sensor causes self heating sufficient to maintain the low resistance state.

Applications

The most common method of using these sensors is in circuits designed to minimise the power applied to a service or load so that the high sensitivity of the sensor can be used to change circuit state at or below a critical temperature. The large resistance change in the transition region may be used to actuate other electronic circuitry, to sound an alarm, cut back power or heat generation, to control temperature etc. Some common applications are power transistor protection in amplifiers and power supplies, triac and SCR protection in power switching applications and temperature control in ovens.

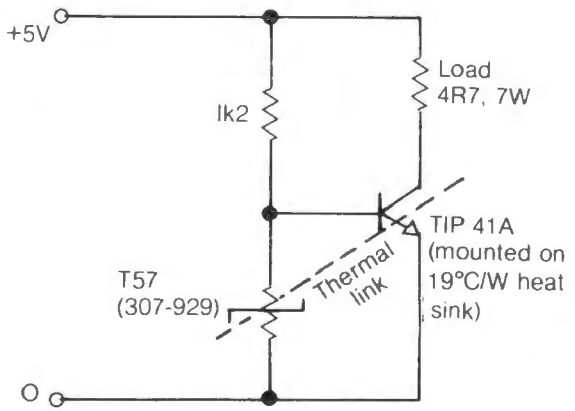
The following circuits show how these sensors can be used and may be taken as a guide to typical applications.

RS data

Transistor protection

In Fig. 3 the circuit is constructed so that the T57 sensor is mounted on the tab of a TIP41A transistor. Under normal conditions the temperature reached by the transistor will not exceed the switching temperature of the sensor and the load will remain fully energised. Should load current and/or transistor temperature increase, causing the sensor to reach 57°C, it will change to its low resistance state, turning the transistor off and limiting load current. Heat sink temperature will be limited to approximately 60°C and the transistor will be protected from thermal runaway and possible breakdown. The circuit has been arranged so that the sensor will work in its normal mode and will therefore return to its normal state when the transistor has cooled down.

Figure 3.

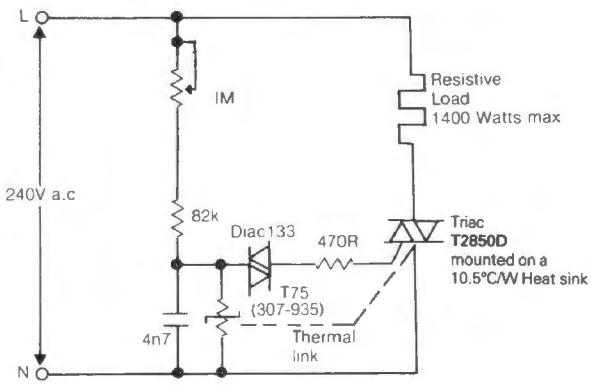


Triac protection

Fig. 4 shows the T75 thermally linked to a triac T2850D.

Under normal conditions the sensor will remain in its high resistance state and the firing circuit will trigger the triac whilst the temperature is below 60°C. Should load current increase, a temperature rise on the triac will be detected by the sensor which changing to its low resistance state will cut out the firing circuit. The triac will therefore be protected from overheating and possible failure.

Figure 4.

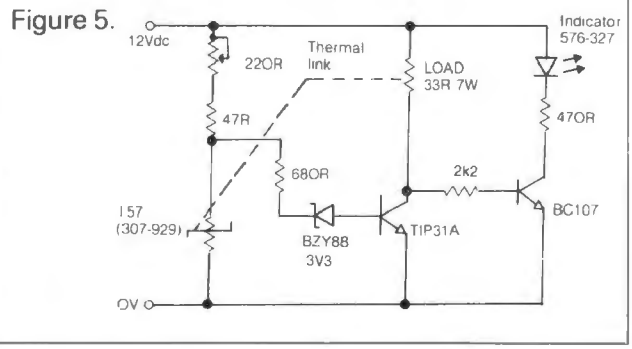


Overloading limitation and indication

Fig. 5 shows a circuit where the sensor T57 is used in a latching mode. The sensor is thermally linked to the load resistor. With a 12V d.c. supply a 33Ω, 7W load resistor will generate sufficient power to heat the sensor up to and beyond 60°C. At the switching temperature the sensor will change to its low resistance state and hold the transistor off, which in turn allows the LED to turn on indicating overload. The 220Ω variable resistor may be adjusted so that the current passing through the sensor in its low resistance state will self heat the sensor to maintain the low resistance state until the supply is removed. The continuous current through the sensor should not exceed the maximum value defined in the basic formula for junction temperature on Page 1.

Should the load resistance be increased thus reducing power to a point where the stabilised load temperature is below the switching temperature of the sensor, the circuit will not latch off and the indicator will remain off. A circuit designer may therefore select a margin of temperature rise between normal stabilised load temperature and sensor switching temperature. Should that margin be exceeded, the power in the load will be automatically limited and the indicator will record the overload.

Figure 5.



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RS data

Overvoltage protector 3423

Stock number 307 — 890

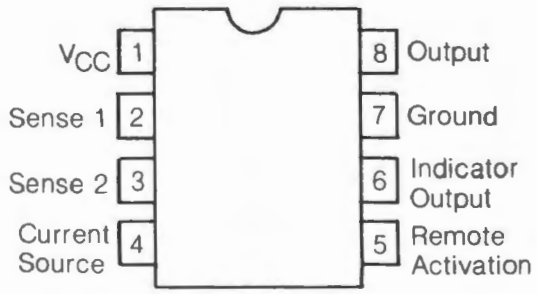
This overvoltage protection circuit (O.V.P.) protects sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" S.C.R. The device senses the overvoltage condition and quickly "crowbars" or short circuits the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

The protection voltage threshold is adjustable and the RS 3423 can be programmed for minimum duration of overvoltage condition before tripping, thus ensuring noise immunity.

Maximum Ratings

Rating	Symbol	Value	Unit
Differential Power Supply Voltage	V_{CC}—V_{EE}	45	Vdc
Sense Voltage (1)	$V_{SENSE\,1}$	6.8	Vdc
Sense Voltage (2)	$V_{SENSE\,2}$	6.8	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperture Range	T_A	0 to +70	°C
Operating Junction Temperature	T_j	150	°C

Pin Connections



(Top View)

Electrical Characteristics ($V_{CC} - V_{EE} = 5.0V$, $T_{LOW} < T_j < T_{high}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}	4.5	—	36	Vdc
Output Voltage	V_O	—	3.0	—	Vdc
Indication Output Current ($V_{OL} = 0.4\,V$)	$I_{o\,(Ind)}$	—	10	—	mA
Reference Voltage ($T_A = 25\,°C$)	V_{ref}	—	2.6	—	Vdc
Temperature Coefficient of Reference Voltage	TCV_{ref}	—	0.08	—	%/°C
Remote Activation Input Current ($V_{IH} = 2.0\,V$)	$I_{in(Ind)}$	—	0.1	—	mA
Source Current	I_{source}	—	0.22	—	mA
Output Current Risetime ($T_A = 25°C$)	t_r	—	400	—	mA/μs
Propogation Delay ($T_A = 25°C$)	t_{pd}	—	0.5	—	μs
Supply Current	I_D	—	5.0	—	mA

Applications

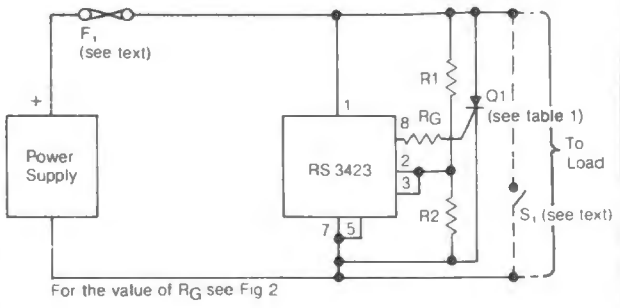
Standard circuit

The basic circuit configuration of the O.V.P. is shown in Fig. 1 and operates for trip voltages in excess of 2.6V. In this circuit, the voltage sensing inputs of both internal amplifiers are tied together for sensing the overvoltage condition. The shortest possible propagation delay is obtained with this configuration. The threshold or trip voltage at which the RS 3423 will trigger and supply gate drive to the crowbar S.C.R., Q1, is given by the equation:

$$V_{trip} = V_{ref}\left(1 + \frac{R1}{R2}\right) \approx 2.6\left(1 + \frac{R1}{R2}\right)$$

R1 and R2 should be selected to give the required trip voltage. (R2 < 10k Ω for minimum drift).

Figure 1a **Supply voltages 4.5V to 36V**



Minimum value for R_G

The minimum value of the gate current limiting resistor, R_G, is given in Fig. 2. Using this value of R_G, the S.C.R., Q1, will receive the greatest gate current possible without damaging the RS 3423. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Fig. 1 may be used to reset the S.C.R. crowbar, but only in conjunction with current limited supplies. Otherwise, the power supply, across which the S.C.R. is connected, must be switched off to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F_1, should be added to protect the S.C.R. and/or the load. The switch S_1 must then be omitted.

Figure 1b **Supply voltages greater than 36V**

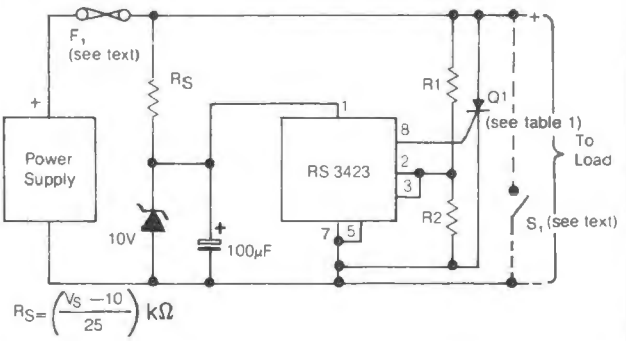
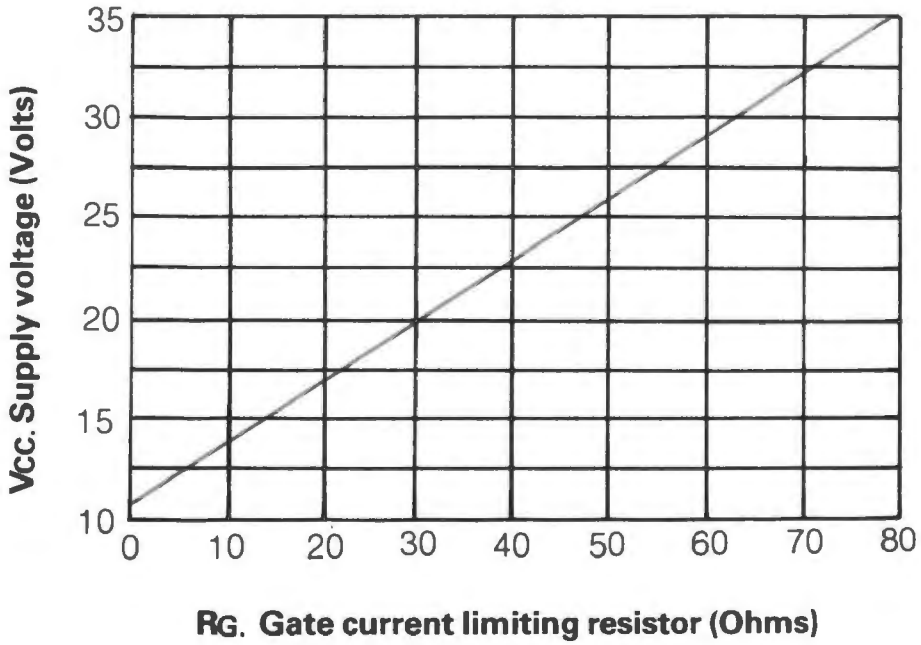


Figure 2 **Minimum R_G versus supply voltage**



When the RS3423 is connected to supply voltages in excess of 36V R_G can be ignored.
Supply on Pin 1 is provided by 10V Zener circuit.

Q1 Thyristor Choice

RS thyristors may be used, the individual choice depending on trip current (fusing current) and operating voltage required. A list of some suitable types given in Table 1.

For further information on the RS range of thyristors see data sheet 1693.

Table 1 **Thyristor list**

Device	V_{RRM} (V)	$I_{T(AVE)}$ max (A)	Turn on time μs	RS Stock No
BTX18-400	400	1.0	0.65	262-012
BT106	700	1.0	1.0	261-249
C106	400	2.5	1.2	261-817
2N 4443	400	5.0	1.0	261-946
2N 4444	600	5.0	1.0	262-034
BTY79-400R	400	6.4	0.85	261-255
THY 500-12	500	12	1.4	261-514
THY 500-26	500	26	1.4	261-520
THY 500-40	500	40	1.4	261-889

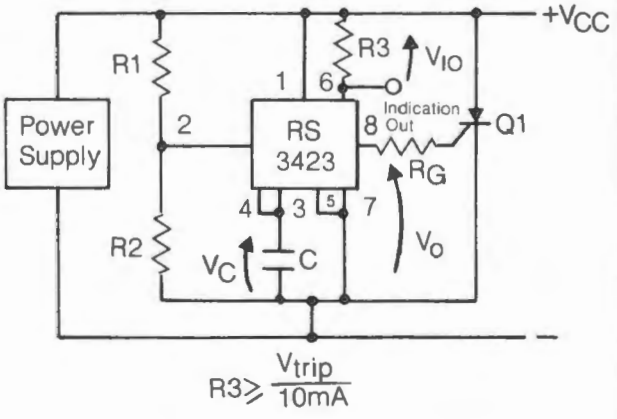
Operation in electrically noisy environments

Configuration for programming minimum duration of overvoltage condition before tripping.

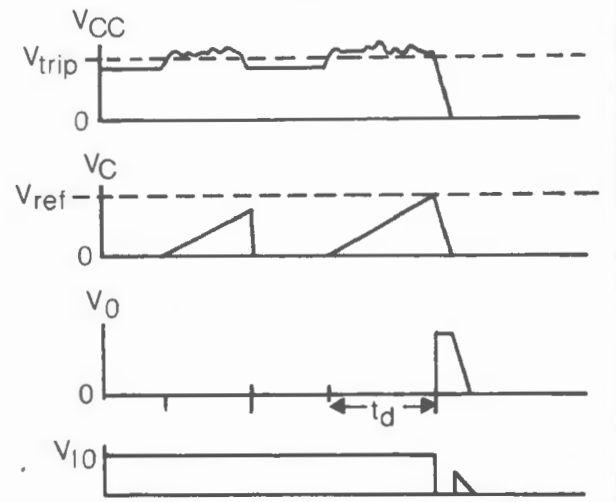
In many instances the RS 3423 will be used in a noisy environment. To prevent false tripping of the O.V.P. circuit by noise which would not normally harm the load, the device has a programmable delay feature. To implement this feature, the circuit shown in Fig. 3 is used. In this configuration, a capacitor is connected from Pin 3 to the — ve rail (V_{EE}). The value of this capacitor determines the minimum duration of the overvoltage condition which will trip the O.V.P.

The value of C can be found from Fig. 4. (see over). The circuit operates in the following manner: when V_{CC} rises above the trip point set by R1 and R2, an internal current source begins charging the capacitor, C, connected to Pin 3. If the overvoltage condition remains present long enough for the capacitor voltage V_C, to reach V_{ref}, the output is activated. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate approximately equal to 10 times the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Figure 3 **Basic configuration for programmable duration of overvoltage condition before trip**



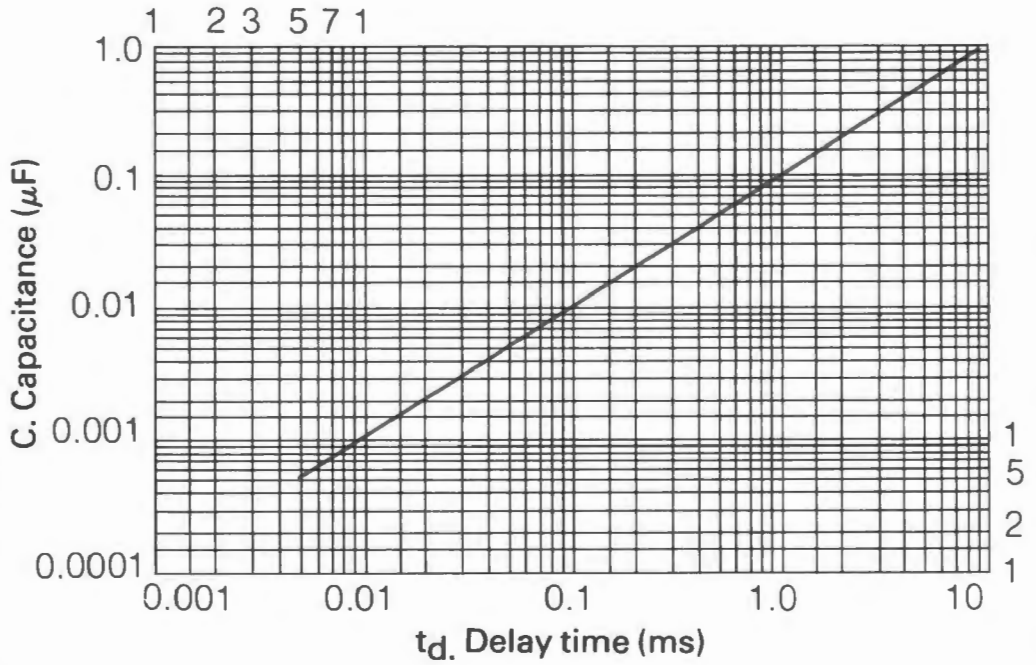
$R3 \geq \frac{V_{trip}}{10mA}$



$t_d = \frac{V_{ref}}{I_{source}} \times C \approx [1.3 \times 10]\ C$ (see figure 4)

RS data

Figure 4 **Capacitance versus minimum overvoltage duration**



Additional features

Activation Indication Output

Fig 3 shows an additional output (for use as an indicator of O.V.P. activation) provided on Pin 6. This output is an open collector transistor which saturates when the O.V.P. is activated. It will remain in a saturated state until the S.C.R. crowbar pulls the supply voltage, VCC, below 4.5V. This output can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the O.V.P. trips. This reduces or eliminates the heatsinking requirements for the crowbar S.C.R.

Remote Activation Input

Another feature of the RS 3423 is its remote activation input, Pin 5. If the voltage on this CMOS/T.T.L. compatible input is held below 0.7V, the RS 3423 operates normally. However, if it is raised to a voltage above 2.0V, the O.V.P. output is activated independent of whether or not an over-voltage condition is present. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one O.V.P. can be used to activate another O.V.P. if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input.

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RS data

Silicon Photodiode with integrated amplifier

Stock number 308-067

The 308-067 consists of a high silicon photodiode combined with a high gain low noise amplifier in a T05 package. It is designed particularly for use where accurate measurements are needed of low light levels, and medium speed variation in such light levels. Its small size and excellent temperature coefficients make it ideally suited for use under adverse conditions. The 308-067 is blue sensitivity optimised and is therefore ideal for general purpose visible light detection.

Any supply voltage between ± 2.5V and ± 18V may be used. A single output line gives a voltage with respect to earth (Pin 1) proportional to the input light level, up to a maximum only slightly less than the power rail. Correction for dark level output is not normally required due to its extremely low value. The output may be short circuited to ground or either power rail without risk of damage. Changes in ambient temperature also cause only minimal variation in signal level, typically 150μV/°C.

Absolute maximum ratings

Supply voltage	±18V
Output short circuit Duration	Indefinite
Storage temperature	—65°C to 100°C
Operating temperature	0°C to 70°C

Connecting details

1. **Earth**
2. **Output**
3. **V+**
4. **V- (Connected to can)**

T05 can with 4 leads	
Gold-plated leads:	12.7mm length
Active light sensitive area:	5mm²

Features

- Very high responsivity
- Linear response
- Low output impedance
- Low noise
- Rugged construction
- Excellent temperature characteristics
- Short circuit proof
- Excellent power supply noise rejection
- TTL compatible
- Simple to use

Applications include

- Light intensity measurements
- Light fluctuation detection
- Optical spectroscopy
- Pollution monitoring
- Alarm systems
- Optical shaft encoders
- Automated inspection and control
- Flow monitoring

CONNECTION DETAILS

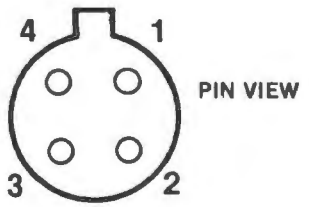
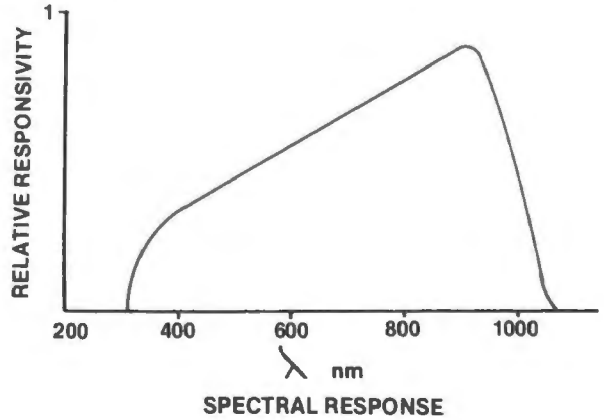
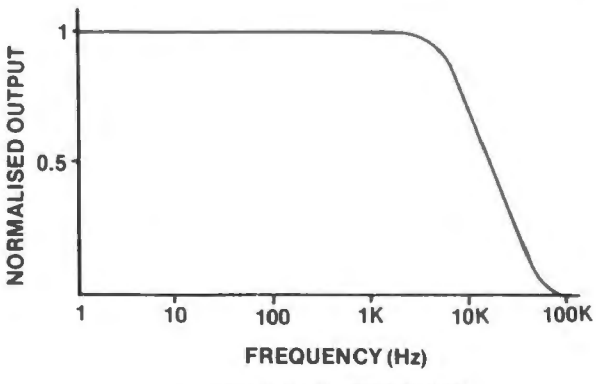


Figure 1: **Spectral and frequency response**





RS data

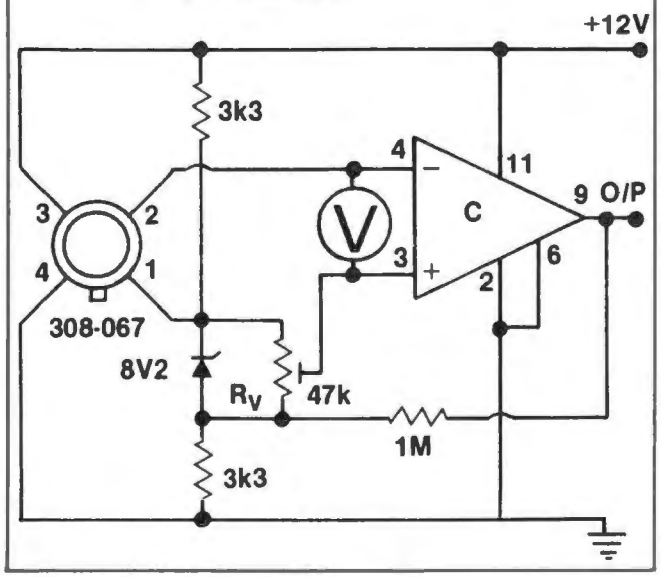
Electrical specification – All at V_S ± 15V and 25°C unless otherwise stated.

Parameter	Conditions	Min.	Typ.	Max.	Units
O/P dark level			+20	+60	mV
O/P saturation level	$R_L \geq 2k\Omega$	–9	–12		V
O/P resistance[1]			75		Ω
O/P short circuit current			6		mA
O/P noise voltage			1	3	mV rms
Responsivity		30	60		$mV/\mu W^{-1}cm^2$
Supply voltage (V+)		2.5	15	18	V
Supply voltage (V–)		–2.5	–15	–18	V
Supply current	$R_L = \infty$		0.5	1.3	mA
Supply voltage rejection ratio		150	50		μV/V
Bandwidth	Upper 3dB point	3	5		kHz
Rise time[2]	$C_L = 0$		30	50	μs
Fall time[2]	$C_L = 0$		30	50	μs
Dark level temperature coefficient	$20°C \leq T_A \leq 50°C$		150	500	μV/°C

Notes:
1. At 5kHz. Drops to 0.01 at d.c.
2. Time for output signal to reach 90% of true reading after application of a step change in light intensity.

Application examples

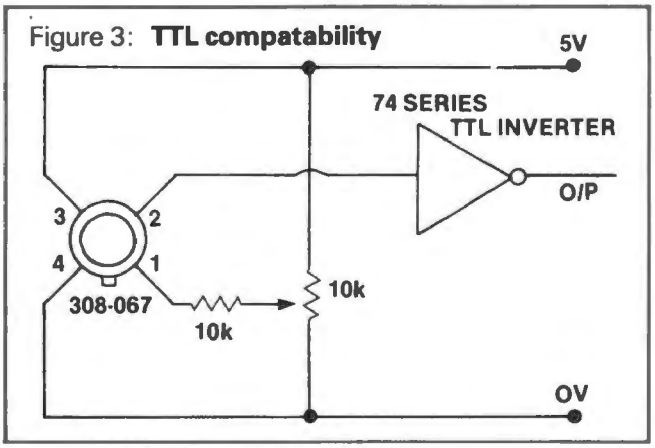
Figure 2: **Light activated switch with "error" monitor**



Linear interfacing
In Figure 2, the comparator (e.g. RS Stock No. 305-260) will switch its output state when the light intensity increases above a pre-set level, determined by R_V. The centre zero voltmeter registers the difference between the switching threshold intensity and the actual intensity received by the 308-067. Since the threshold is determined with respect to pin 1 of the 308-067 supply voltage variations have no effect on the operation of the circuit.

Note:- Centre zero voltmeter (RS Stock No. 259-628) requires two resistors (RS Stock No. 259-369) wired in series.

Figure 3: **TTL compatability**



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RS data

Precision timer/ stopwatch i.c.

Stock number 307-991

The RS 7045 Stopwatch/Timer i.c. is a fully integrated C-MOS digital timer, stopwatch or 24 hour clock circuit. The oscillator, frequency divider, multiplexer, decoder, segment and digit output buffers are all included on chip. The circuit is designed to interface directly either with eight discrete common cathode seven segment LED's (e.g. 8 off 587-917) or with fully multiplexed multi-digit common cathode displays (e.g. 2 off 587-096). The nominal supply voltage is 3.6V, equivalent to a stack of three nickel- cadmium button cells. The only external components required for a complete stopwatch, in addition to the display and the batteries, are a 6.5536MHz crystal (308-051), a trimming capacitor (125-654) and four switches (which ideally should be gold contact types).

The RS 7045 takes the oscillator frequency and divides it in sixteen binary stages to a frequency of 100Hz. Some of these divider outputs are used to generate the multiplex waveforms at a 12.5% duty cycle/800Hz rate. The 100Hz signal is then processed in the counters which feed into latches, which in turn are multiplexed into the decoder. The counter section spans the range of 1/100 sec. to 24 hours, which can be simultaneously displayed on the eight digits available. The digit drivers (cathodes) are connected to the multiplex lines through zero suppression logic, while the segment drivers (anodes) are directly connected to the decoder outputs.

Features

- Versatility of applications: precision timer, 4 stopwatch modes, 24-hour clock.
- Simple to use:
  - 4 controls (stopwatch and timer): 1. Function, 2. Start/Stop, 3. Reset, 4. Display
  - 24-hour clock: 5. Rapid Minute Advance, 6. Rapid Hour Advance
- Total integration: includes oscillator, divider, decoder driver on chip.
- Wide operating supply range: 2.5V $\leq V_{DD} \leq$4.5V.
- Low operating power consumption: display off typ. 0.9mW at 3.6V supply.
- High precision – high frequency operation: quartz crystal oscillator at 6.5536MHz.
- High output current drive: 15mA peak current per segment, with 12.5% duty cycle
- Leading zero suppression: timer stopwatch applications.
- Fractional second suppression: 24-hour clock application.
- Short duration short circuit protection on all inputs and outputs at 3.6V supply (Note 2).
- All terminals protected against static charges.
- Wide operating temperature range: –20°C to + 70°C

Figure 1 **Block diagram**

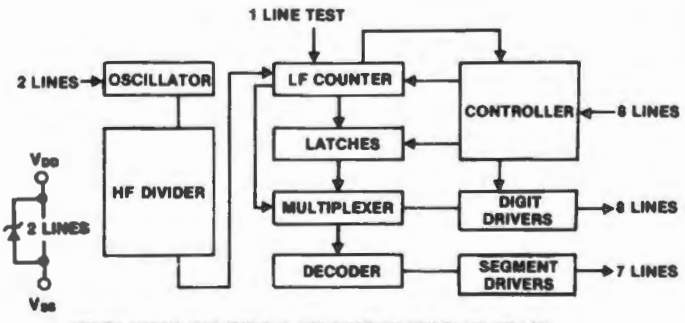
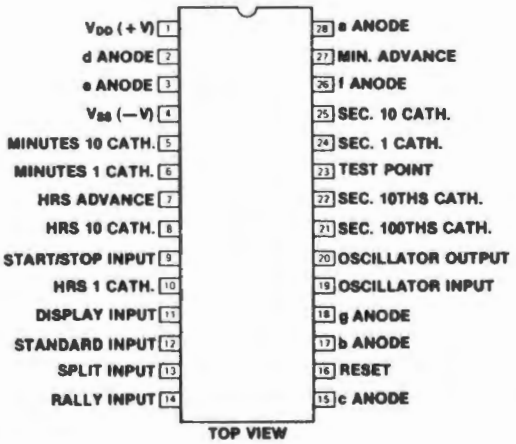


Figure 2 **Pin connections**



Absolute maximum ratings

Power dissipation (Notes 1 and 2) 1W
Supply voltage +5.5V
Input voltage Equal to, but never in excess of the supply voltages
Output voltage Equal to, but never in excess of the supply voltages
Storage temperature −55°C to +125°C
Operating temperature −20°C to +70°C

Typical operating characteristics

$|V_{DD}| - |V_{SS}| = 3.6V$, $T_A = 25°C$, $f_{osc} = 6.5536MHz$, test circuit 1 unless otherwise stated.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply current	I_{DD1}	Display off		180	2000	μA
Instantaneous supply current	I_{DD2}	7 segments lit 1.8V dropped across display	70	105		mA
Instantaneous supply current	I_{DD3}	2 segments lit 1.8V dropped across display	28	42		mA
Operating voltage	V_{DD}	−20°C < T_A < 70°C 7 segments lit	2.5		4.5	V
Segment current drive		1.8V dropped across display, 12.5% duty cycle				
Instantaneous			10	15		mA
Average			1.25	1.875		mA
Segment current drive		2 segments lit, 1.8V dropped across display, 12.5% duty cycle				
Instantaneous	I_{S2}		14	21		mA
Average	I_{S11}		1.75	2.625		mA
Min. switch actuation Current any switch	I_{SW}		50			μA
Digit driver leakage current	I_{LD}				200	μA
Segment driver leakage current	I_{LS}				200	μA
Typical Oscillator Stability	f_{STAB}	$3V \leq V_{DD} \leq 4V$, $C_{TUNING} = 15pF$		1.0		ppm
Max time for oscillator to Start	t	$V_{DD} = 3.6V$			0.1	sec
		$V_{DD} = 2.5V$			1.0	sec
Oscillator input Capacitance	C_{IN}			17		pF

Note 1: This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

Note 2: Short circuit and high output drive considerations:
The RS 7045 has been designed such that the maximum digit output drive current will not exceed 150 mA when used with any conventional LED displays and a fully charged stack of three nickel-cadmium cells. If the 150 mA is exceeded for any extended duration of time, damage may result to the device.
It is, therefore, recommended that if the RS 7045 is to be used under conditions where the digit output drive could exceed 150 mA – high voltage operation at 5V for example – that additional external current limiting resistors be included in series with the LED display (segment lines).
If the digit outputs are short circuited to the positive supply (3.6V) the short circuit current will be approximately 300 mA. This will not damage the device momentarily. Unless this short circuit condition is immediately removed probable device failure will occur from extended time periods of short circuit operation.

Typical performance curves

Figure 3 **Oscillator stability as a function of supply voltage**

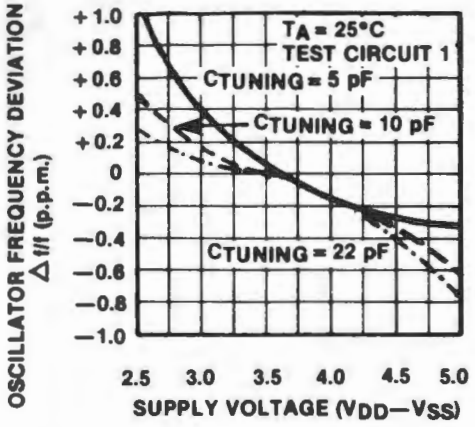


Figure 4 **Peak segment current drive as a function of display voltage drop**

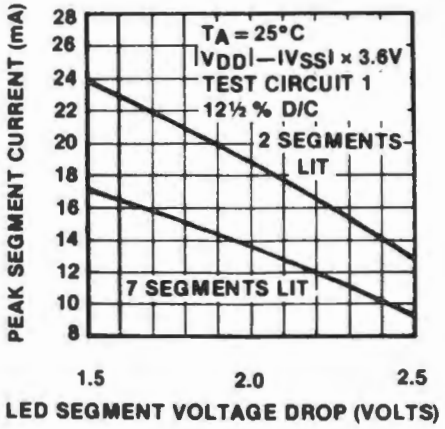


Figure 5 **Peak segment current as a function of supply voltage**

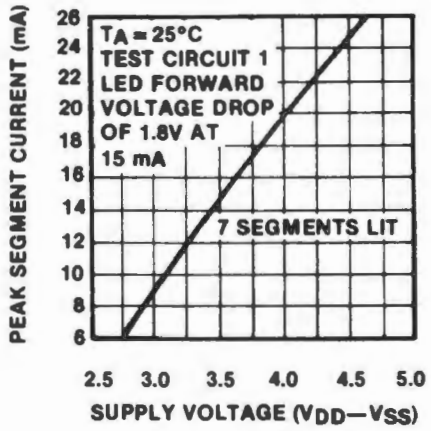
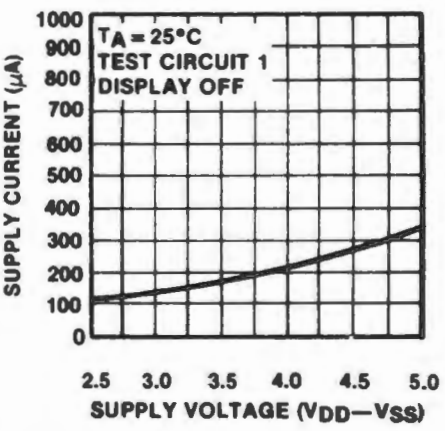


Figure 6 **Supply current as a function of supply voltage**



Functional operation

Stopwatch/timer operation

The control inputs used in the complete stopwatch application are: (refer to test circuit 1 for a schematic diagram).

START/STOP	RESET	SPLIT
DISPLAY	STANDARD	RALLY

START/STOP and DISPLAY are designed for connection to single pole double throw switches to ensure operation free of contact bounce.

The switch connected to RESET can be a normally open single pole single throw. STANDARD, SPLIT and RALLY are control points with internal pull down resistors to V_{SS}. These are designed to be connected to a rotary function switch which will connect no more than one of these points to V_{DD}. If STANDARD (SPLIT, RALLY) is connected to V_{DD}, the stopwatch is said to be in the STANDARD (SPLIT, RALLY) mode. If all three are left open, the stopwatch is in the SEQUENTIAL mode.

Reset function

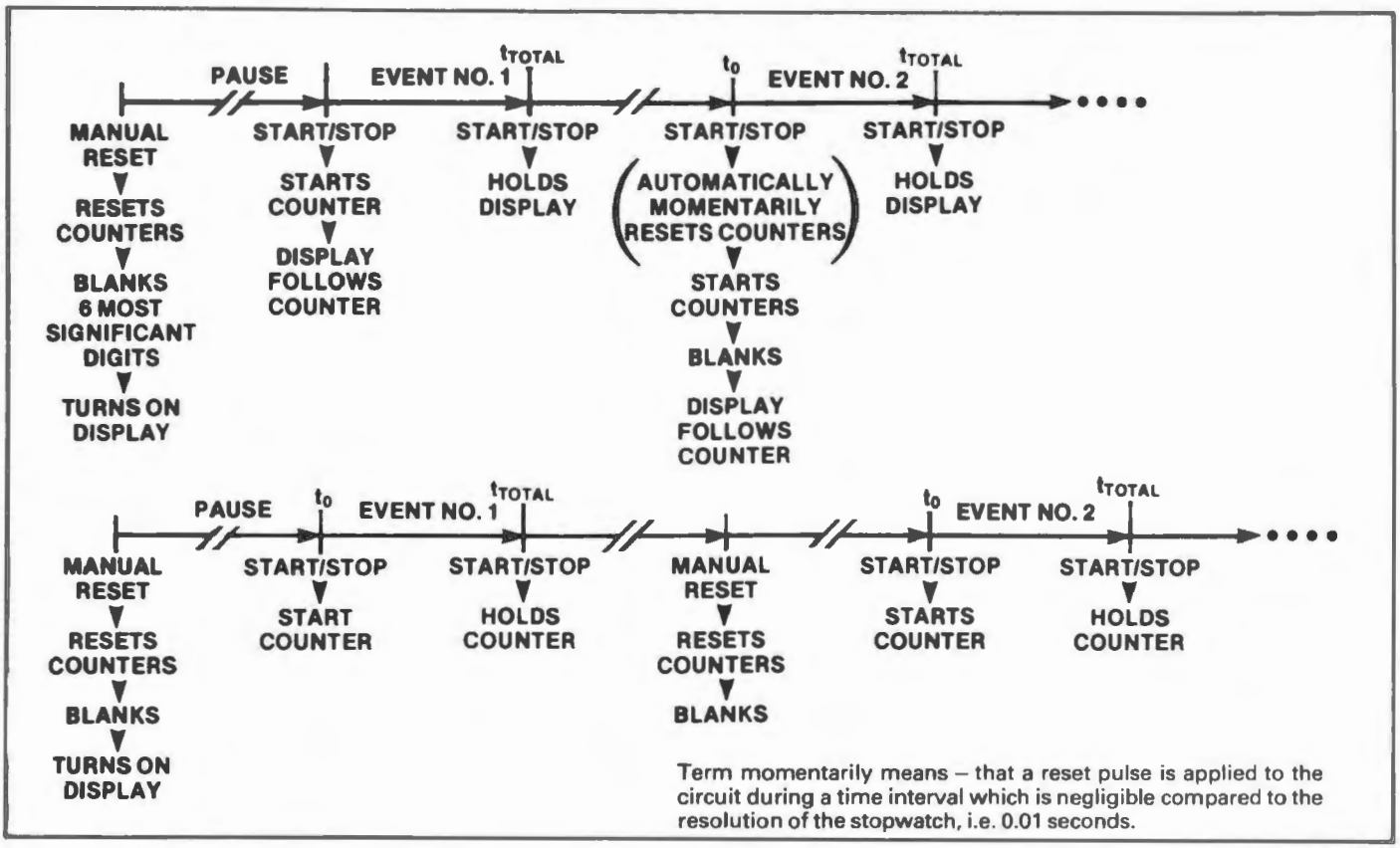
When the stopwatch is turned on, the RESET will normally be activated. This puts the stopwatch in a ready condition by:

1. Resetting all circuitry.
2. Blanking seconds, minutes, hours.
3. Showing 00 in the fractional seconds position.
4. Turning on the display if it was previously turned off.

The display of just two zeros in the fractional seconds positions gives the complete assurance that the stopwatch is "ready to go".

Standard mode

If the STANDARD mode, after a reset has taken place, START/STOP is activated at time t_0. The clock and display are moving simultaneously. A second activation of START/STOP stops the clock and holds the display at time t_{TOTAL}. This completes an event. For timing a second event there are two options. One is to activate START/STOP at the start of the second event. This will momentarily reset the counter and display so that the timing of the second event proceeds from zero. Another activation of START/STOP stops the counter and display at time t_{TOTAL} to end the second event. The other option is to activate RESET after the first event is over. Then, the second event proceeds similarly to the first event. As is clear from this description, RESET can be used at any time to reset the stopwatch, including when a timing is in progress. The DISPLAY input can be activated to turn the display off and on. If the display is off when RESET is activated, it will reset and turn on. Turning off the display for timing long events will result in a very substantial power saving.



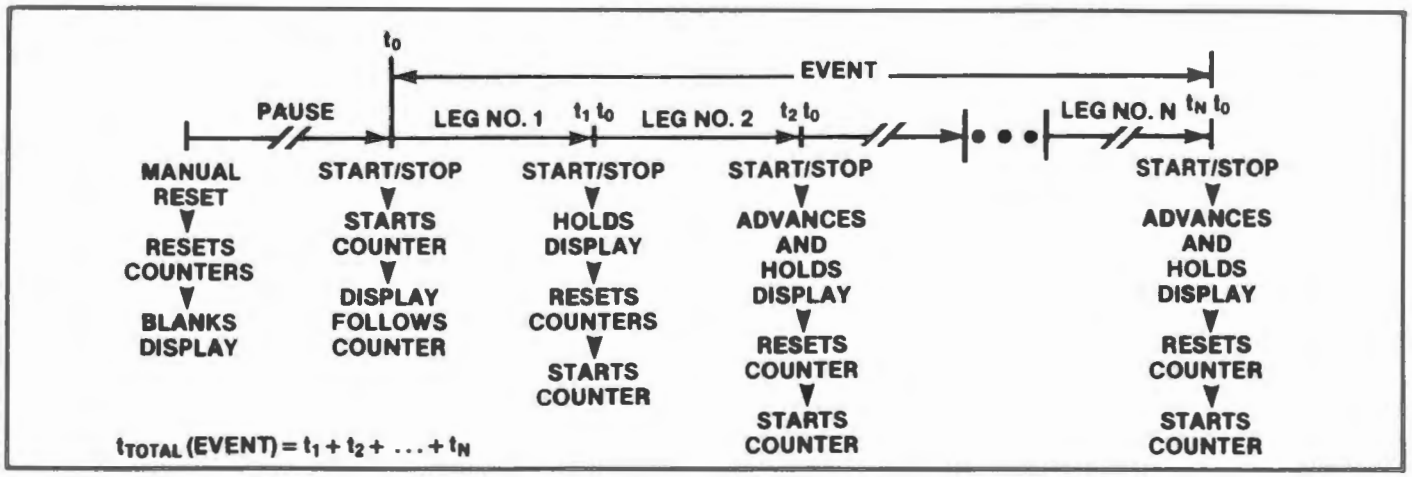
Term momentarily means – that a reset pulse is applied to the circuit during a time interval which is negligible compared to the resolution of the stopwatch, i.e. 0.01 seconds.

Sequential mode

The sequential mode of the stopwatch is designed for timing events consisting of more than one leg (such as relays, multilap races, etc.). After the inital reset the START/STOP is activated at t_0 to start the event. A second activation of START/STOP at time t_1 stops the display to allow t_1 to be read out, while the clock resets and starts counting again instantaneously. At time t_2 an activation of START/STOP enters t_2 (the time of leg no. 2) into the display. This sequence can continue indefinitely. Assuming the total event has N legs, the total elapsed time is then equal to the sum of the N times read out:

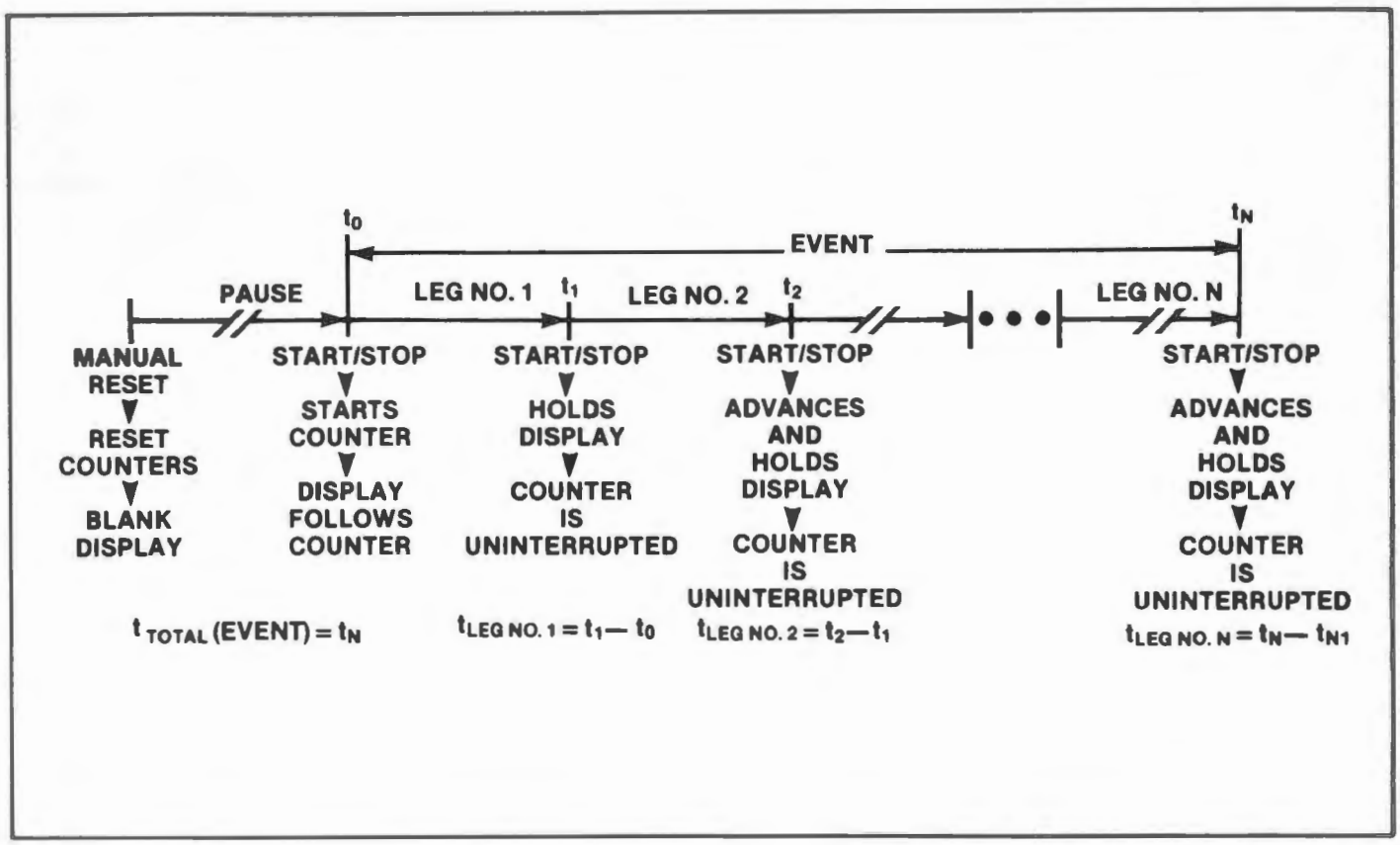
$$t_{TOTAL} = t_1 + t_2 \ldots + t_N$$

If it is desired to see the moving clock after a time has been recorded, the DISPLAY switch can be activated to release the display hold and catch up with the moving clock. The display cannot be turned off in the sequential mode. Reset can be activated at any time to reset clock and display.



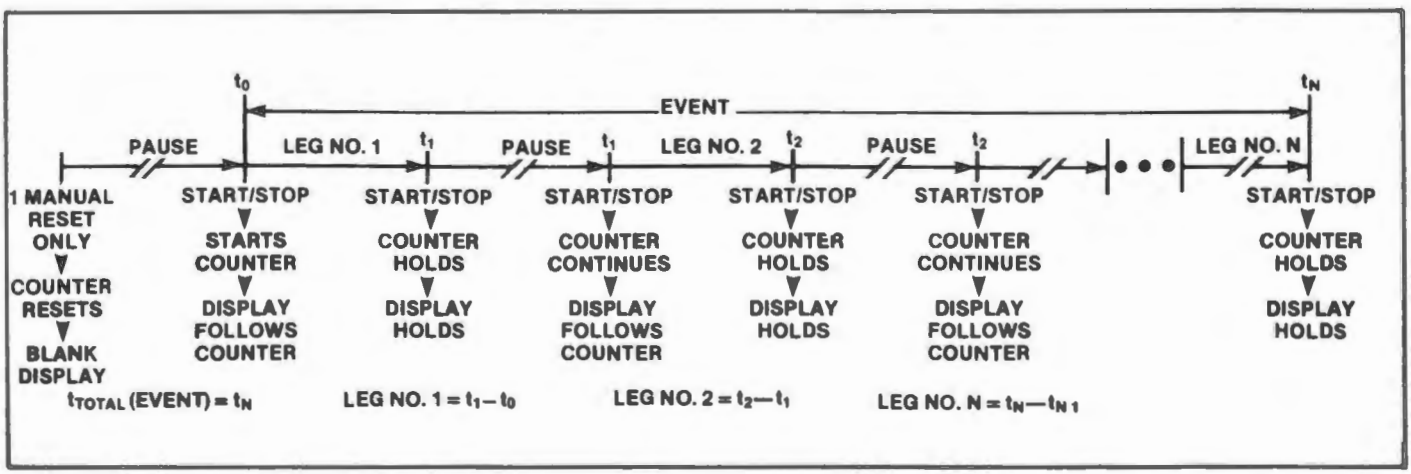
Split mode

The split mode is another mode for timing multileg events. In contrast to the sequential mode, the timing in the split mode is cumulative. From a reset condition, the START/STOP switch is activated at t_0 to start the counter and display running. A second activation at t_1 stops the display so t_1 can be read out while the counter continues timing. A third activation at t_2 advances the display with the total elapsed time from t_0 to t_2 showing. Finally, at time t_N the total elapsed time of the event is entered in the display. The time of one leg of the event can be obtained by subtraction. The display can be synchronized to the counter (catch-up function) at any time by activating the display switch. To reset the timer, activate reset. The display cannot be turned off in the SPLIT mode.



Rally mode

The rally mode is designed for timing of events with interruptions. Consider an N leg event where the legs may be separated by intervals which should not be timed. The rally mode starts with a RESET. At time t_0 the stopwatch is started by activating START/STOP. After this point the RESET function is disabled to prevent accidental resets during long timing intervals. At time t_1 a START/STOP pulse stops counter and display. From here on each leg time is added to the total by a START/STOP pulse at the beginning of the leg and at the end. The individual leg times are determined by subtraction. The display can be turned on and off with the display switch.



Clock operation

The control inputs used in a possible 24-hour clock configuration are (refer to test circuit no. 2):

START/STOP
MINUTES ADVANCE
HOURS ADVANCE
RALLY

START/STOP, MINUTES ADVANCE and HOURS ADVANCE are designed for connection to single pole double throw switches; this assures contact bounce elimination on these inputs. To avoid an additional switch for the DISPLAY input, the RALLY input should be connected to V_{DD} through a 22k resistor and to V_{SS} through a 100n capacitor. These components ensure that the display is on when power is applied to the circuit. The most convenient setting procedure is:

1. If clock is not running when power is applied activate START/STOP switch.
2. Depress MINUTES ADVANCE switch to obtain correct minutes setting, one minute count per activation.
3. Depress HOURS ADVANCE switch to obtain correct HOURS setting, one hour count per activation.

It is possible to set the clock more accurately or to correct small time errors by using START/STOP in combination with MINUTES ADVANCE. If the clock is, for instance, 20 seconds slow, activate the MINUTES ADVANCE once, then activate the START/STOP, wait 40 seconds and activate the START/STOP again. If the clock is 20 seconds fast, the START/STOP switch should be activated to stop the clock, then after 20 seconds activated again to restart the clock. Other clock configurations are possible (see Application notes).

Figure 7 **Test circuit 1. Stopwatch mode**

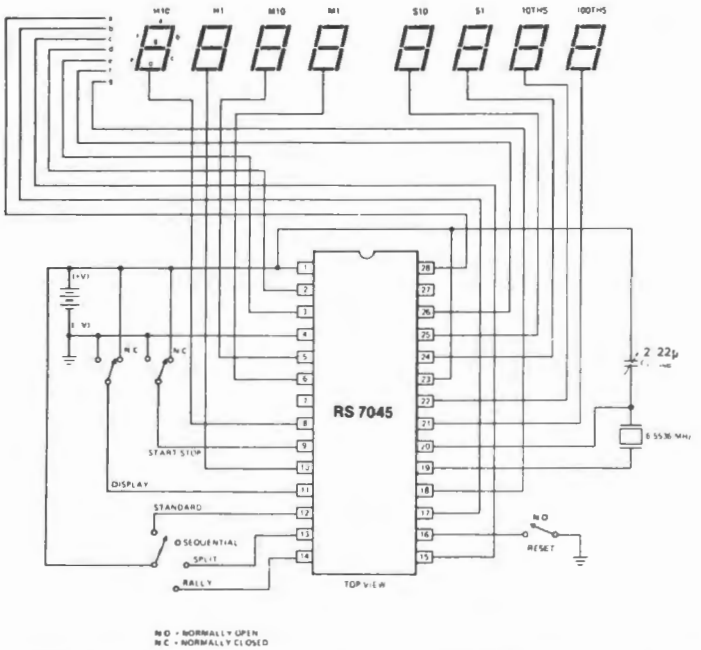
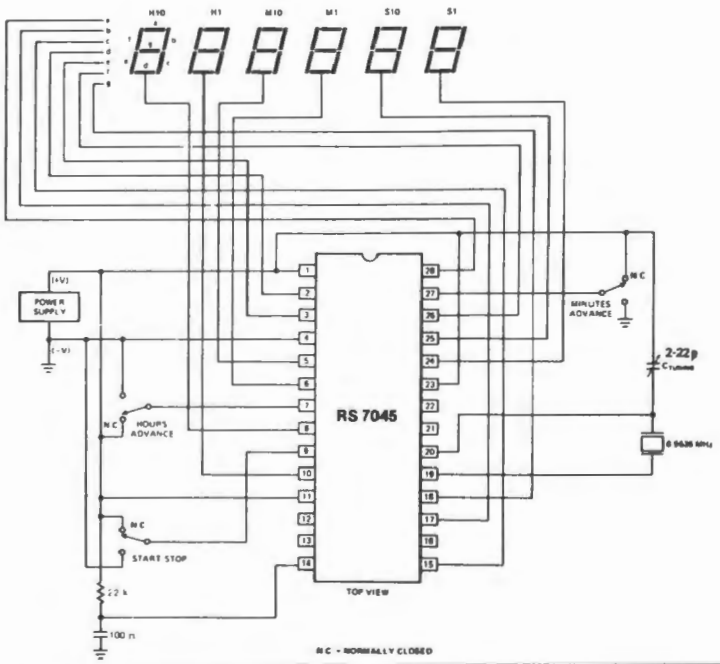


Figure 8 **Test circuit 2. Clock mode**



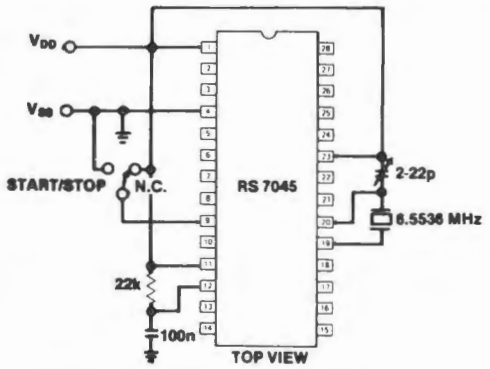
Application notes

The RS 7045 has been designed with versatility of applications in the digital timer/stopwatch/24-hour clock field as the major objective. The simplicity of operating modes designed for an extremely practical, easy to use stopwatch, at the same time allow the design of a variety of simpler elapse timer, stopwatch and clock circuits; a few of these will be shown and discussed briefly here:

Timer circuit I

This simple circuit (display connections not shown) allows interval timing up to 24 hours with a resolution of 0.01 seconds. Each interval is timed by one start and one stop pulse on the start/stop line. The start pulse for the next interval to be timed automatically resets the timer. Leading zero suppression is automatic.

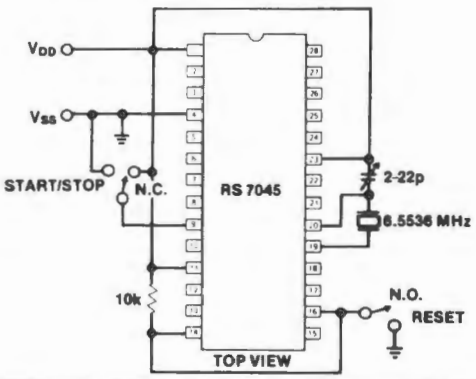
Figure 9 **24 hour timer**



Timer circuit II

This circuit allows cumulative timing of intervals. Each interval is timed by one start and one stop pulse on the start/stop line. Each subsequent interval timed adds to the total line displayed. The reset switch allows the timer to be reset to zero to start another sequence of intervals. Note that the time between the end of one interval and the start of the reset is not recorded or added to the total.

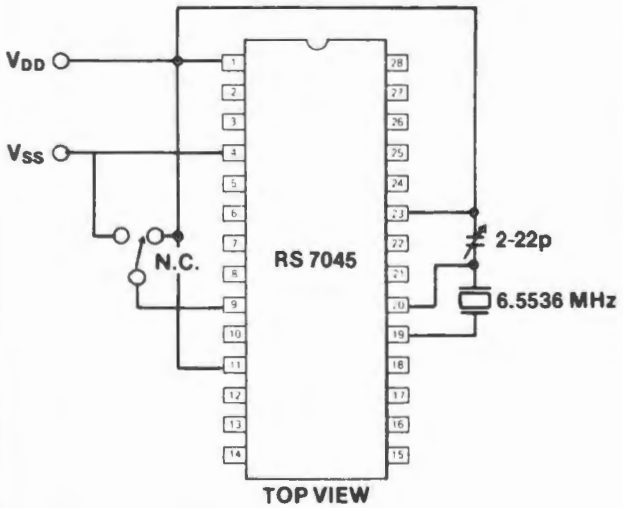
Figure 10 **Cumulative Timer**



Timer circuit III

This circuit allows interval timing with a single pulse on the start/stop line. Each pulse enters the time elapsed since the previous pulse into the display, resets the timer and starts the timer for the next interval.

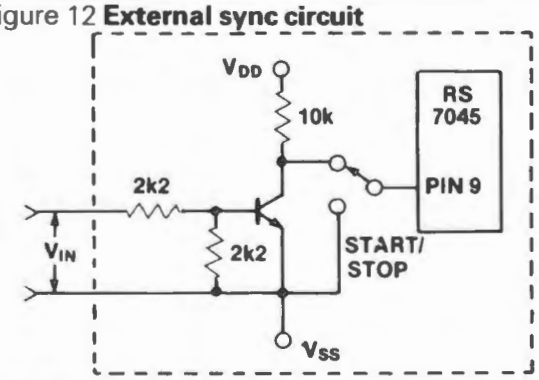
Figure 11 **Interval timer**



Stopwatch external sync circuit

If the stopwatch is connected as shown in test circuit 1, a few additional components will allow external synchronization of the stopwatch in any mode:

Figure 12 **External sync circuit**



Note: Be sure to minimize the distance between the transistor and the RS 7045 to prevent noise from being generated along this connection, which could damage the device. *Refer to absolute maximum ratings. Noise spikes absolutely must not exceed the supply voltages.*

The external sync signal source has to supply a positive pulse to activate the START/STOP input. The minimum voltage of this pulse is about 1.2V in the circuit as shown, but the triggering level can be changed by modifying the input resistor ratio. The output impedance of the external sync signal source should be no greater than 4k ohms.

RS data

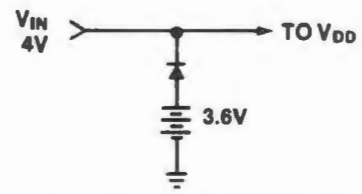
Clock circuit I

The basic clock circuit is shown in test circuit 2. The clock accuracy with a stable voltage supply will depend mostly on the temperature and ageing characteristics of the crystal.

The power supply can be modified to give battery standby power.

The standby circuit should be designed to provide the specified minimum voltage to the RS 7045.

Figure 13 **Battery back-up circuit**



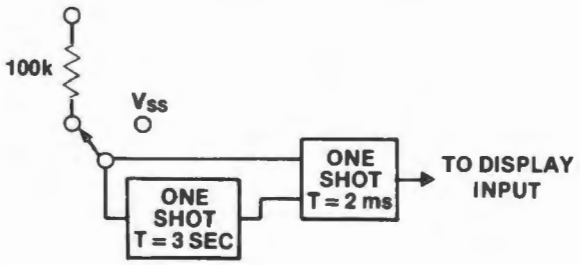
Other clock circuits

The basic clock circuit can be modified for various special applications. If it is desired to turn the display on and off, then connect the display input to an additional SPDT switch, while omitting the capacitor/resistor combination on the rally input.

This 24-hour clock version might be applicable to vehicles, boats, etc. where a battery is available to supply the display off clock current, while the display can be turned on with the ignition. Another possible configuration would connect a special circuit to the DISPLAY input which generates a double pulse about 3 seconds apart:

This means depressing the switch will turn on the clock's display for 3 seconds. This allows design of a battery operated "on demand" digital 24-hour clock.

Figure 14 **Momentary display circuit**



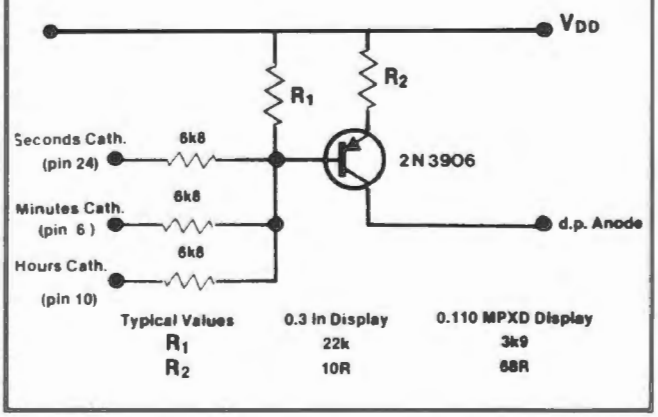
Oscillator calibration

A convenient method of tuning the oscillator is to connect a 10k pull up resistor to the fractional seconds cathode (pin 21) and then use this point to measure the multiplex frequency. This should then be tuned to 800Hz (1.25ms) using the oscillator trim capacitor. (Obviously if an attempt is made to measure the oscillator frequency directly, oscillator frequency may change due to the extra capacitive load.)

Decimal point driving

The RS 7045 may drive decimal points as required using the circuit shown (Figure 15).

Figure 15 **Decimal point driver circuit**



Typical Values	0.3 In Display	0.110 MPXD Display
R_1	22k	3k9
R_2	10R	68R

R.S. Components Ltd. 13-17 Epworth Street, London, EC2P 2HA Telephone: 01-250 4000
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C-MOS A/D Converter

RS data

Stock Number 308-045

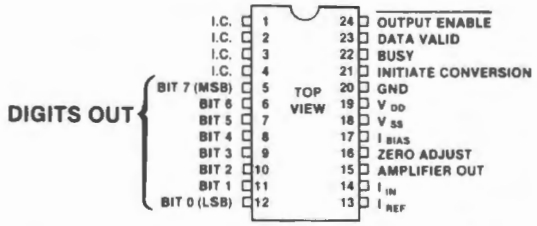
The RS 8703 is an 8 bit monolithic C-MOS analogue-to-digital converter. Fully self-contained in a single 24-pin dual-in-line package requiring only passive support components, voltage or current reference and power supply.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analogue current and pulses of a reference current and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs as an 8 bit binary word. The OUTPUT ENABLE control switches the outputs to a high impedance or off state when held high. The off state allows bus organised output connections.

The RS 8703 is a C-MOS device and must be handled correctly to prevent damage. Store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under 'power on' conditions, as high transients may cause permanent damage.

Absolute maximum ratings

Storage temperature	−65°C to +150°C
Operating temperature range	0°C to +70°C
$V_{DD} - V_{SS}$	18 V
I_{IN}	±10 mA
I_{REF}	±10 mA
Digital input voltage	−0.3 to V_{DD} +0.3 V
Operating V_{DD} and V_{SS} range	3.5 V to 7 V
Package dissipation	500 mW
Lead temperature (soldering, 10 seconds)	300°C



Do not make connections to pins 1, 2, 3 or 4. These pins are internally connected.

Electrical characteristics

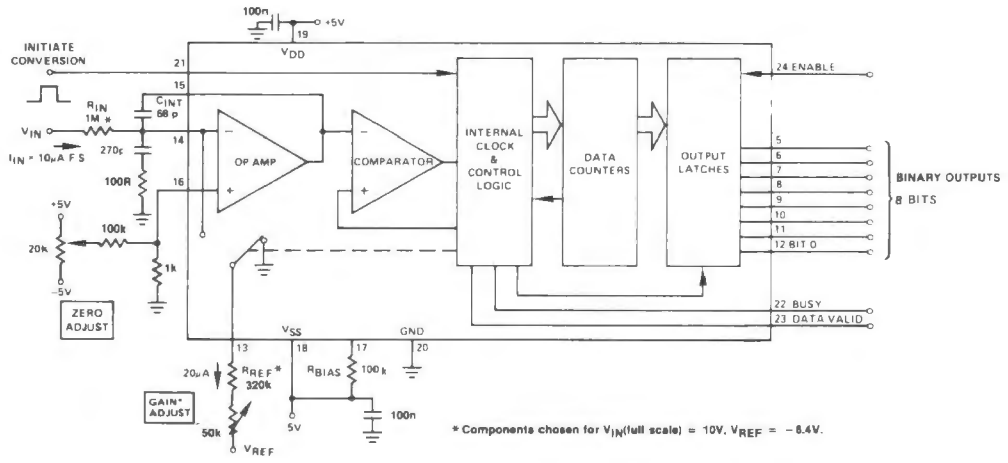
Unless otherwise specified, V_{DD} = +5V, V_{SS} = −5V, V_{GND} = 0, V_{REF} = −6.4V, R_{BIAS} = 100kΩ, test circuit shown. T_A = 25°C unless Full Temperature Range is specified (0°C to +70°C).

Parameter	Definition	Conditions	Min	Typ	Max	Units
Accuracy Resolution Accuracy	Binary word length of digital output		8			Bits
Relative Accuracy	Output deviation from straight line between normalized zero and full scale input				±½	LSB
Differential Non-Linearity	Deviation from 1 LSB between transition points			±¼	±½	LSB
Differential Non-Linearity Temperature Drift	Variation in Differential Non-Linearity due to temperature change	Full Temp Range		±2.5	±5	ppm/°C
Gain Variance	Variation from exact A (compensate by trimming R_{IN} or R_{REF})	Nominal A = 528		±2	+5 −3	% of Nominal
Gain Variance Drift	Variation in A due to temperature change	Full Temperature Range		±25	±75	ppm/°C
Zero Offset	Correction at zero adjust to give zero output when input is zero	I_{IN} = 0		±10	±50	mV
Zero Temperature Drift	Variation in zero offset due to temperature change	Full Temperature Range		±30	±50	V/°C
Analogue Inputs I_{IN} Full Scale	Full Scale analogue input current to achieve specified accuracy			10		μA
I_{REF} (Note 1)	Reference current input to achieve specified accuracy			−20		μA

Parameter	Definition	Conditions	Min	Typ	Max	Units
Digital Inputs V_{IN} (1)	Logical '1' input threshold for Output Enable and Initiate Conversion Input	Full Temperature Range	3.5			V
V_{IN} (0)	Logical '0' input threshold for Output Enable and Initiate Conversion Input	Full Temperature Range			1.5	V
Propagation Delay Output Enable	T_{PLH} T_{PHL}	$C_L = 100pF$, $R_L = 1k\Omega$		500		ns
Digital Output $I_{O(OFF)}$	Off-state output current	$\overline{OE} = 3.5V, 0.4V < V_C < 2.4$		0.1	±10	μA
V_{OUT}(1)	Logical '1' output voltage for Digits Out. Busy and Data Valid Outputs	Full Temperature Range $I_{OUT} = -10\mu A$ $I_{OUT} = -360\mu A$	 4.5 2.4			 V V
V_{OUT}(0)	Logical '0' output voltage for Digits Out. Busy and Data Valid Outputs	Full Temperature Range $V_{DD} = 4.75V$ $I_{OUT} = 360\mu A$			 0.4	 V
Dynamic Conversion Time	Time required to perform one complete A/D conversion	Full Temperature Range		1.25	1.8	ms
Conversion Rate in Free-Run Mode		$V_{INIT\,CONV} = +5V$	555	800		Conversions per Second
Minimum Pulse Width for Initiate Conversion		Full Temperature Range	500			ns
Supply Current I_{DD} Quiescent	Current required from positive supply during operation	Full Temperature Range $V_{INIT\,CONV} = 0V$		 1.4	 5.0	 mA
I_{SS} Quiescent	Current required from negative supply during operation	Full Temperature Range $V_{INIT\,CONV} = 0V$		 −1.6	 −5.0	 mA
Supply Sensitivity	Change in full scale gain vs supply voltage change Change in full scale gain vs supply voltage change for tracking supplies	$V_{DD} \pm 1V, V_{SS} \pm 1V$ $\lvert V_{DD} \rvert = \lvert V_{SS} \rvert = 5V \pm 1V$		±0.5 ±0.05	±1.0 ±0.1	%/V %/V

Note 1: I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

Test circuits



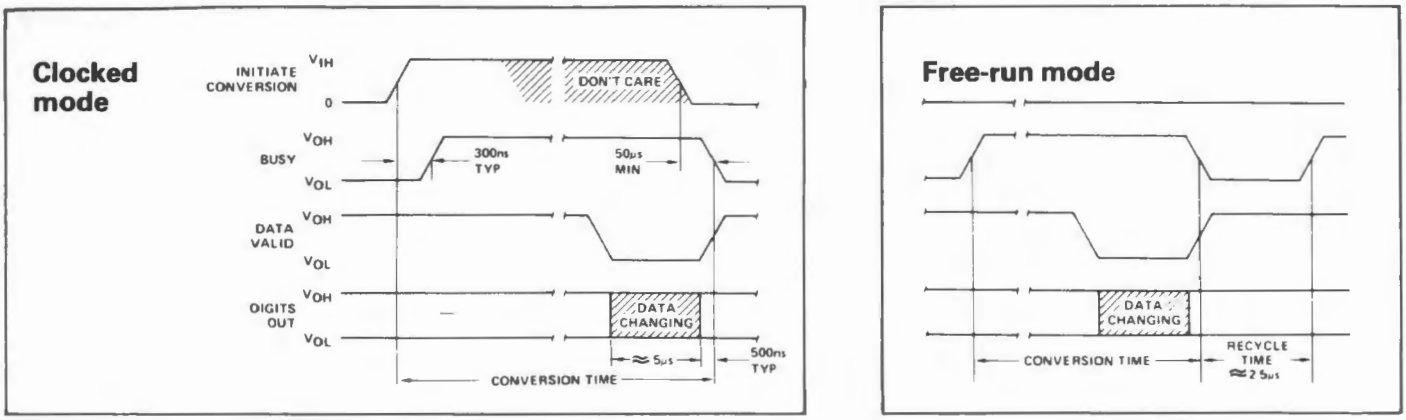
Circuit description

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analogue input voltage; I_{REF} is proportional to the reference voltage and is of opposite sign to I_{IN}. I_{REF} is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in binary) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Timing diagrams (Rise, fall times = 200ns typ., C_L = 50pF)



Pin functions

Initiate Conversion Input — Accepts C-MOS and most 5V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output — A digital status output which is compatible with C-MOS logic and low power TTL (can sink and source 360μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output — A digital status which is compatible with C-MOS logic and low power TTL (can sink and source 360μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5μs before the completion of a conversion cycle. During this 5μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out (Bit 0, Bit 1, etc.) — The binary digit outputs which are the result of the A/D conversion. These outputs are C-MOS logic and low power TTL compatible.

Applications information

Input/Output Relationships — The analogue input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{DIGITAL COUNTS} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

$$A = 528$$

where DIGITAL COUNTS is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analogue input	Digital MSB ... LSB
$V_{IN} \geq$ Full Scale	1 . . . 111 . . . 1
= Full Scale — 1 LSB	1 . . . 111 . . . 1
= 1 LSB	0 . . . 000 . . . 1
$\leq$ 0	0 . . . 000 . . . 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection — Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{EF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 100nF or larger right at the device pins.

R_{DAMP} — Exact value not critical but should have a nominal value of 100 Ω ±10%. Locate close to pin 14, and away from noisy lines.

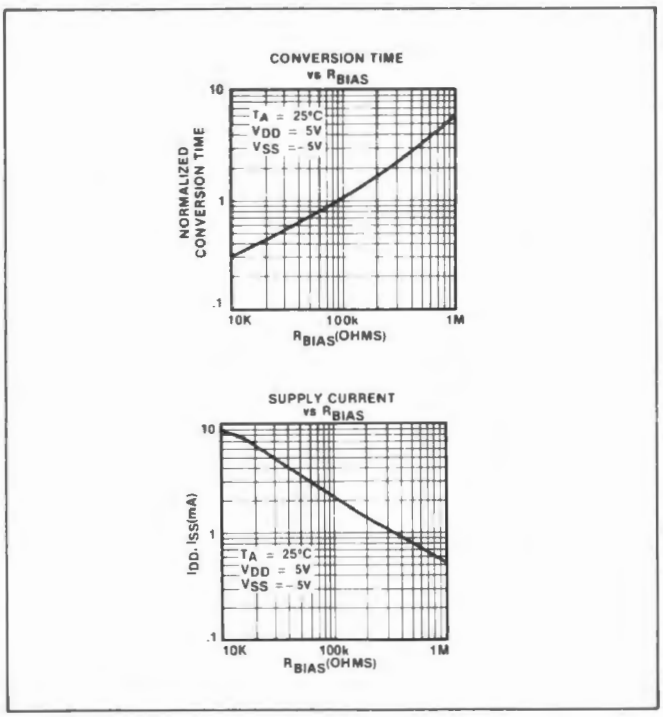
C_{DAMP} — Exact value not critical but should have a nominal value of 270pF ±20%. Locate close to pin 14, and away from noisy lines.

C_{INT} — Exact value not critical but should have a nominal value of 68pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15.

V_{REF} — A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS} — Power supplies of ±5V are recommended, with 0.05% line and load regulation and 100nF decoupling capacitors.

R_{BIAS} — Specifications for the RS 8703 are based on R_{BIAS} = 100k Ω ±10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. The graphs below show the variation in conversion time and supply current with R_{BIAS}.



R_{IN}, R_{REF} — Values of these components are chosen to give a full scale input current of approximately 10μA and a reference current of approximately −20μA.

$$R_{IN} \cong \frac{V_{IN\ FULL\ SCALE}}{10\mu A} \quad R_{REF} \cong \frac{V_{REF}}{-20\mu A}$$

Examples

$$R_{IN} \cong \frac{10V}{10\mu A} = 1M\Omega \quad R_{REF} \cong \frac{-6.4V}{-20\mu A} = 320k\Omega$$

Note: that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the gain adjust to obtain full scale output of $V_{IN\ FULL\ SCALE}$ (see adjustment procedure). Thick film resistors with 2% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

Adjustment procedure — The test circuit diagram shows optional circuits for trimming the zero location and full scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full scale), it is recommended that transition points be used in setting the zero and full scale values. Recommended procedure is as follows:

1. Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
2. Set V_{IN} to + ½ LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
3. For full scale adjustment, set V_{IN} to the full scale value less 1½ LSB and trim the gain adjust. circuit for a 111 . . . 110 to 111 . . . 111 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

Technical hints

Proper design procedures are necessary to obtain best accuracy from the A/D converter.

a. Do not route logic signals under the RS 8703 or near any of the three analogue terminals I_{IN}, I_{REF}, and Zero Adjust (pins 13, 14, 15, 16).
b. Plan the grounding. Keep the analogue ground isolated from the logic ground by making the two electrically common only at the system ground.
c. Filter the supply voltage by using bypass capacitors of value 100nF or greater connected in shunt between the supply line and the logic ground (pin 20). Locate the capacitors as close to the I.C. as practical.
d. Provide a reference as stable as the conversion accuracy to be expected.
The conversion accuracy is a direct function of the V_{REF}. In terms of V_{REF} voltage regulation, the RS 8703 requires ±.04%, to introduce less than 1/10 LSB error.
e. Choose a full scale voltage range as large as possible; this will minimize the effect of zero drift and input noise. For example, a 100μV zero drift or noise voltage on the 8703 (8-bit) will produce a ±½ LSB error at 50mV full scale, but only ±1/40 LSB at 10V full scale.

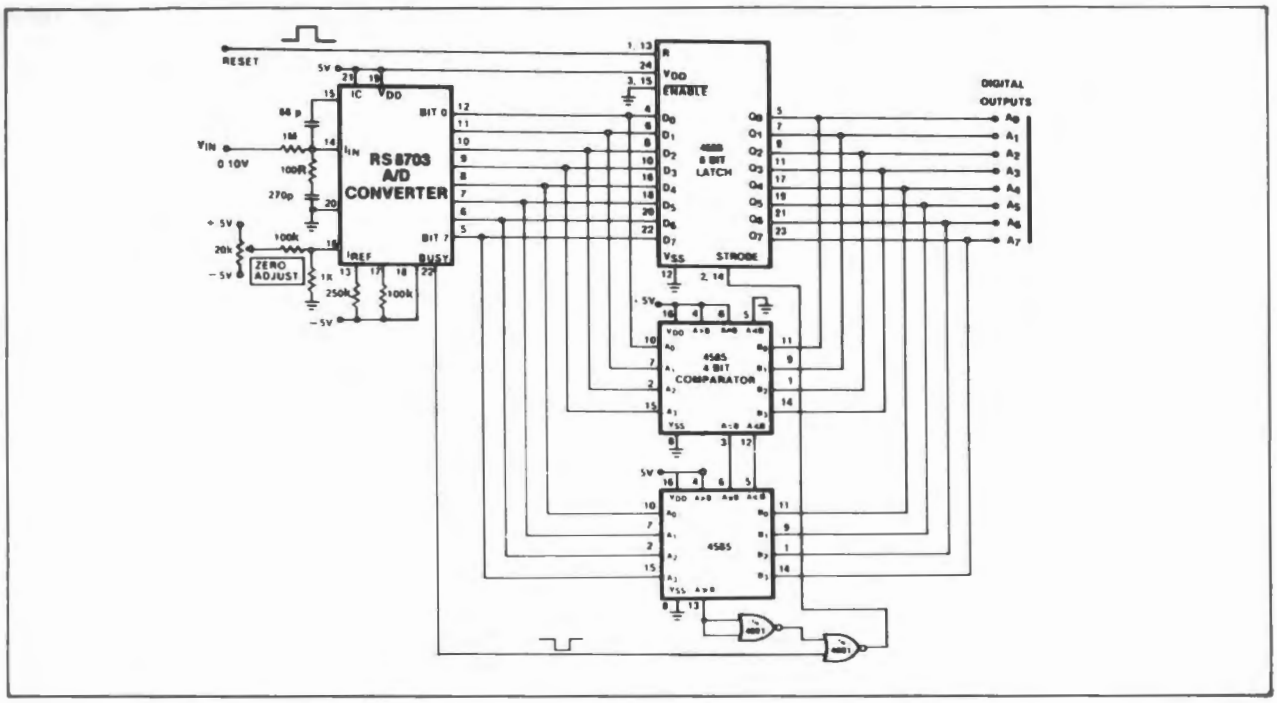
CAUTION: WHEN USING ZENERS, OP AMPS AND VOLTAGE REGULATORS.

These devices are often used as input amplifiers, voltage references and power supplies for A/D converters. It is worth noting that these devices can generate considerable "High Frequency" noise. Normally, this noise does not interfere with the operation of the A/D converter. However, excessive noise from zeners, used as voltage references for example, have been found to be the cause of strange counting sequences and non-linear A/D operation. It should therefore be standard practice to bypass all zeners and voltage regulators with at least 100nF capacitors. (If the zener is exceptionally noisy, 1 to 10μF capacitors may be required. Remember that zeners are often used as white noise sources in noise generators.)

If erratic operation is still observed, then either the op amp's feedback resistor or the output should be bypassed. Note also that the noise level of zeners, op amps and voltage regulators varies from batch to batch. Bypassing these devices during the design state will prevent the noise level variation from becoming a possible problem.

Analogue peak detection is accomplished by repeatedly measuring the input signal with an A/D converter and comparing the current reading with the previous reading. If the current reading is larger than the previous, the current reading is stored in the latch and becomes the new peak value. Since the peak is stored in a C-MOS latch, the peak can be stored indefinitely.

The RS 8703 A/D converter measures the analogue input at a 1kHz rate and computes the binary value of the input. After each 1ms measurement, the binary value is latched in the output of the A/D. This value is then presented to both the 4585 comparators and the 4508 8-bit latch. If the A/D's value is greater than that of the 4508 memory, pin 13 (A > B) of the 4585 goes high. This allows the strobe pulse to go through the 4001 NOR gate to the 4508 memory. The new value is then stored and becomes the reference for subsequent readings. Each time the A/D has a value greater than that stored in the latch, the latch is updated with the larger peak. The system is reset by pulsing the 4508 reset pin high, causing the output to go to 0000 0000.

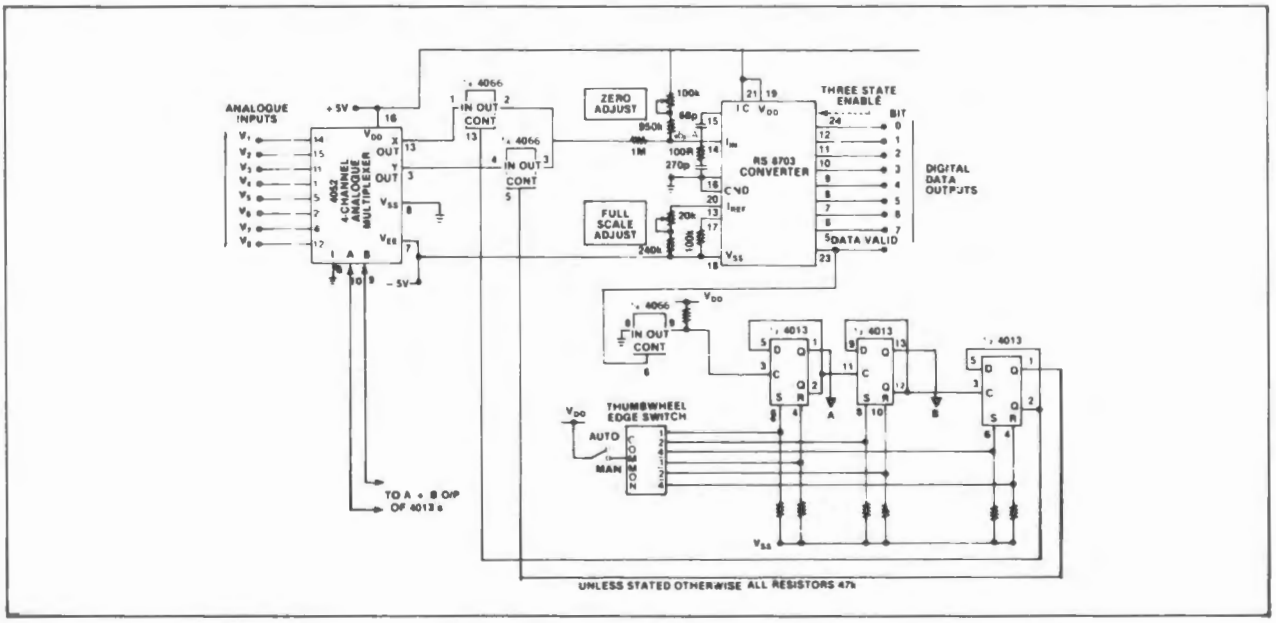


A low-cost data acquisition system with 8 inputs and 8 bits (0.4%) of resolution at the output can be built by using the RS 8703 C-MOS A/D converter and adding the 4052 channel C-MOS multiplexer and the 4013 binary counter circuit.

Each input is measured for 1ms, then the digital value is placed in the output latch and remains for 1ms while the next input is being measured. After each 1ms measurement (conversion), the data valid line goes low for 5μs to indicate that the output latch is being updated. (The data must not be read during this period.) The negative edge of the data valid pulse is used to advance the binary counter by one. So after each conversion the 4052 via the 4013's, automatically advances to the next input. The sampling sequence is therefore V_1, V_2, . . . V_7, V_0 and then back to V_1. The RS 8703 resets itself for 2.5μs after the data valid pulse so the analogue switch has a total of 7.5μs to settle down. This is more than adequate to assure that the A/D will ignore any switching transients.

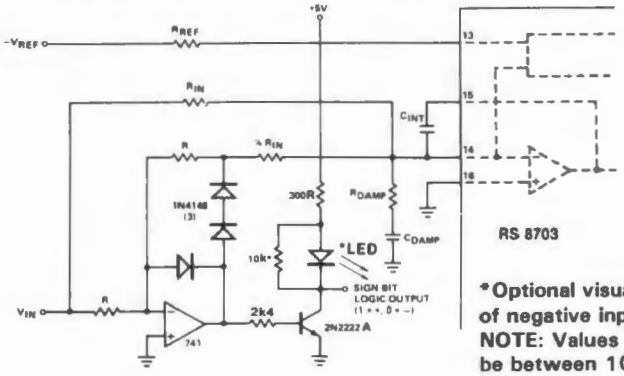
For the circuit shown, the input voltage range is limited by the 4052 to ±5 volts (V_{DD}, V_{EE}). If more input voltage range is needed, the V_{SS} and V_{EE} can be increased or the 1MΩ resistor can be replaced by individual resistors in front of each analogue input. The exact value of each resistor is determined by dividing the maximum input voltage by 5μA. ($R_{IN} = V_{max} \div 5\mu A$).

The 950kΩ and 100kΩ resistors are used to provide an offset current of 5μA, allowing the analogue input voltage to be negative as well as positive. If the input voltage does not go negative, then these two resistors can be deleted.



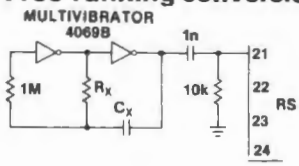
RS data

Bipolar operation (+ and – inputs) with sign indication



*Optional visual indication of negative input
NOTE: Values for R should be between 10k and 100k

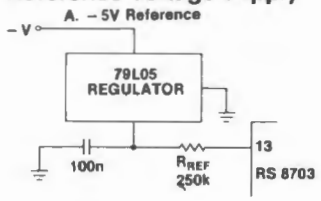
Free-running conversion rate control



Multivibrator circuit at Pin 21 (Initiate Conversion) strobes converter at rates slower than the normal free-run mode. ($T = R_xC_x$)

Reference voltage supply

A. – 5V Reference



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RS data

Remote control i.c.'s

A range of remote control i.c.'s consisting of one transmitter (308-073), an infra-red pre-amplifier (301-527) and five receivers, (303-826, 308-089, 309-981, 309-997 and 305-248) with individual characteristics to suit many control requirements.

The system is based on the transmission of coded P.P.M. (Pulse Position Modulation) signals over a wide variety of transmission media e.g. sound, ultrasonics, infra-red, fibre optics, cable links. Provision is made for carrier frequency generation where required to suit the medium employed. Processing of the received P.P.M. signal is performed by a discrete amplifier or for infra-red an i.c. is available. The restored signal is passed to one, or a combination, of the five receiver i.c.'s where an error checking system inspects the P.P.M. data before activating the appropriate output. The output functions available include parallel 4-bit binary, in either latched or momentary forms, analogue output controls and discrete outputs.

The ability of one transmitter to control a combination of different receivers enables this system to satisfy the majority of remote control applications including sound systems, light displays, machine control, security devices etc.

Printed circuit boards to suit an infra-red link are available (434-807/813/835/891).

Remote control transmitter RS490 (308-073)

The RS490 is a remote control transmitter i.c. which produces a binary coded pulse position modulated (P.P.M.) waveform. The code generated is dependent on the operation of any one single pole switch from a matrix of up to 32 switches and the device will produce a corresponding number of different P.P.M. codewords.

A feature of the i.c. is its ability to generate, if required, a carrier frequency over the range 0 to 200kHz which may be subsequently modulated by the P.P.M. codeword, thereby enabling modulated carriers to be directly produced. The P.P.M. rate can also be adjusted over a wide range to suit transducer response times.

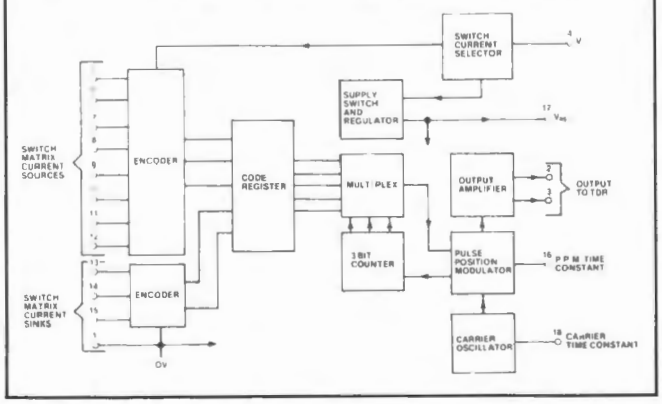
Absolute maximum ratings

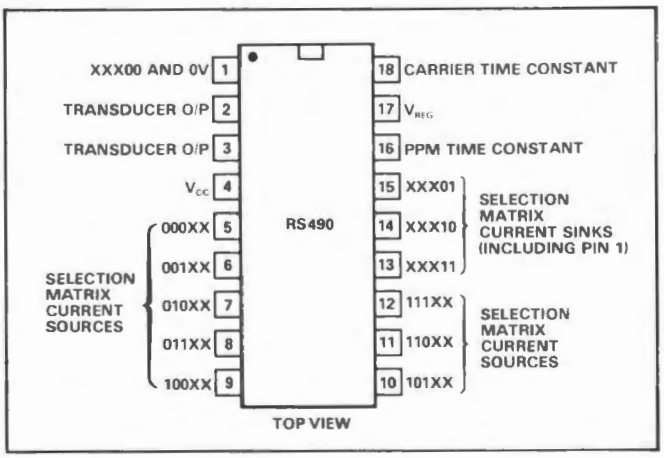
Max. supply voltage	9.5V
Operating voltage range, V_{CC}	7V to 9.5V
Maximum power dissipation	600mW
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

Features

- Ultrasonic or infra-red transmission
- Direct drive for ultrasonic transducer
- Direct drive of visible LED when using infra-red
- Lower power consumption
- Pulse position modulation gives excellent immunity from noise and multipath reflections
- Switch resistance up to 5kΩ tolerated

Figure 1 **RS 490 Transmitter block diagram**





Electrical characteristics

Test conditions (unless otherwise stated): T_{amb} = 25°C $V_{CC} \triangleq$ +7V to +10.5V

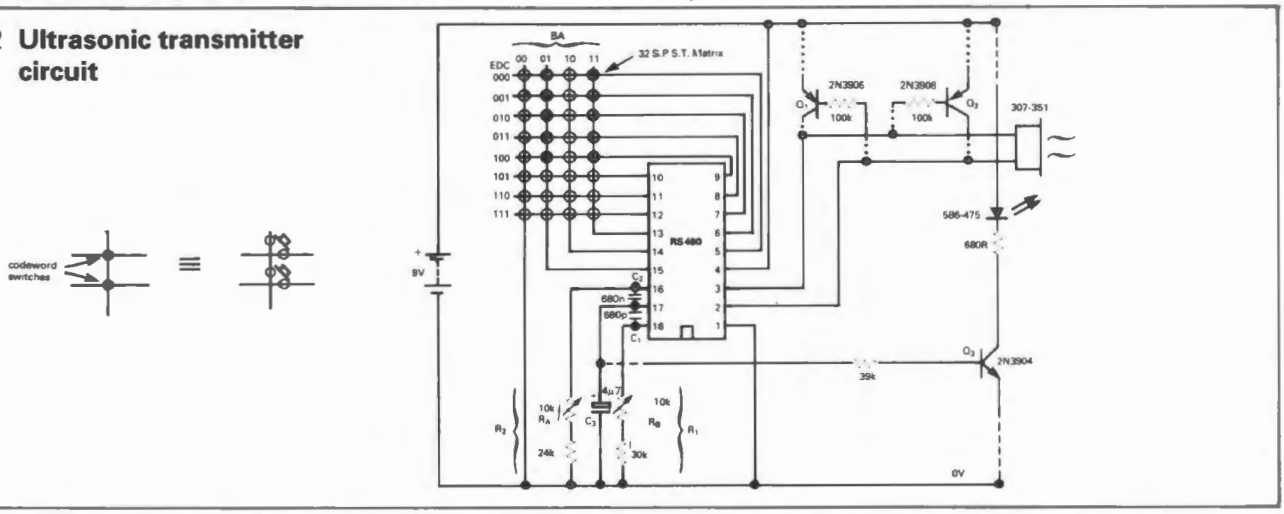
Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply current	4		9.5	16	mA	V_{CC} = 9.5V
Standby supply current	4			10	μA	
Stabilized voltage	17	4.1		4.9	V	
Output current available from stabilized supply	17			1	mA	
Output voltage swing	2, 3	V_{CC}-1			V	Unloaded
Output voltage	2			1	V	I_2 + 10mA, I_3 = 5mA; Peak value < 1ms
Output voltage	3			1	V	
External switch resistance	5-15			5	kΩ	
External carrier resistor R_1	18	20	40	80	kΩ	C2 = 680pF fc = 40kHz
t_1 deviation from calculated value using fixed timing components	2,3			±10	%	$t_1 = 0.95\ C_2R_2$
PPM resistor	16	15	30	60	Ω	
Variation of t_1 and t_0 with V_{CC} t_1 with V_{CC} = 7V/t_1 with V_{CC} = 10.5V	2,3			±4	%	
t_0 with V_{CC} = 7V/t_0 with V_{CC} = 10.5V	2,3			±4	%	
Ratio t_0/t_1	2,3	1.4		1.6		
Pulse width t_0	2,3	0.11±t_1		0.22±t_2		
Interword gap	2,3		3			The interword gap is 3 times t_1 derived by counting

Typical applications

RS490 Transmitter (ultrasonic)

The internal structure of the RS490 remote control i.c. is illustrated in Figure 1 and Figure 2 shows the complete circuit of an ultrasonic transmitter.

Figure 2 **Ultrasonic transmitter circuit**



Thirty-two momentary switches are used to programme the transmitter into producing a pulse position coded signal. The components R_1 and C_1 define the carrier frequency according to Eqt. 1.

$$f \approx \frac{1}{C_1R_1}\text{Hz} \ldots \text{Eqt. 1} \qquad \begin{matrix} C_1 \text{ in F} \\ R_1 \text{ in } \Omega \end{matrix} \qquad \begin{matrix} 0 \leq f \leq 200\text{kHz} \\ 20\text{k}\Omega \leq R_1 \leq 80\text{k}\Omega \end{matrix}$$

The components employed in Figure 2 allow adjustment of the carrier frequency about 40kHz which is the approximate resonant frequency of the RS ultrasonic transducer 307-351.

R_2 and C_2 select the modulation rate according to Eqt. 2.

$t_0 \approx 1.4c_2R_2$ sec . . . Eqt. 2

t_0 = time for '0' interval (see later)

R_2 in Ω 15kΩ≤R_2≤100kΩ

C_2 in F

1 bit/sec ≤ t_0 rate ≤ 10kbit/sec

The capacitor C_3 is a decoupling capacitor for the internal voltage used to provide a constant voltage for the two CR networks. The regulator voltage on pin 17 is not established until a codeword switch has been closed.

The RS 490 is capable of driving the RS ultrasonic transmitter directly from pins 2 and 3 providing an effective range of ≈8m. An increase in range up to ≈ 10m is possible by employing active pull ups Q_1 and Q_2 shown with dotted connections in Figure 2.

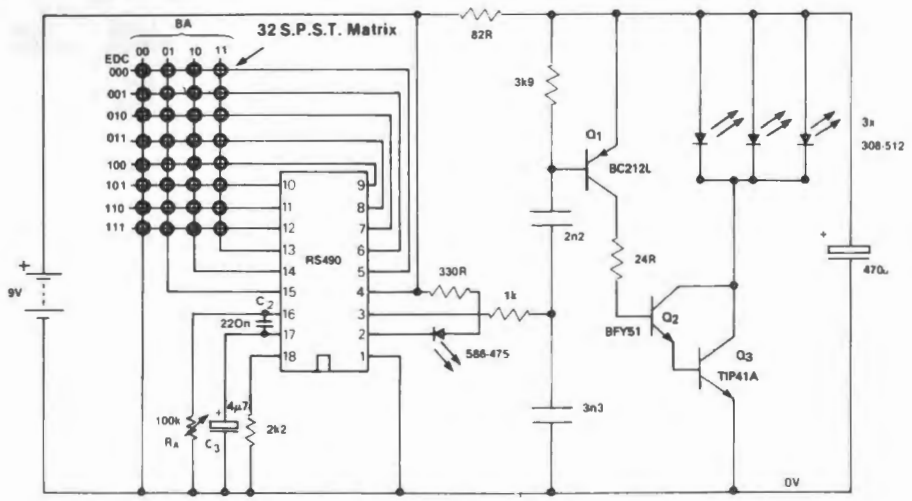
To indicate transmitter operation the voltage appearing on pin 17 at switch closure can be used to drive an NPN transistor feeding an L.E.D. and this modification is shown with dashed connections in Figure 2.

Because the standby current of the RS490 is very low (≈6μA) rising to about 8mA when transmitting, the power requirements can be satisfied by a PP3 battery. Using the L.E.D. indicator modification shown the operating current will be approximately 20mA.

RS490 Transmitter (infra-red)

Operating a remote control system on an infra-red link offers some advantages over the previously discussed ultrasonic mode. The important gains are less multipath interference, lower spurious radiation, a higher modulation rate capability and more robust transducers. Figure 3 shows the complete circuit of an infra-red transmitter.
The modulation rate formula by Eqt. 2 is applicable to the infra-red transmitter circuit. A visual indication of transmitter operation can be provided by employing the unused output on pin 2 to drive an L.E.D. via a pull up resistor as shown in Figure 3.
The programming of the infra-red transmitter is identical to the ultrasonic system in employing 32 S.P.S.T. switches to produce a pulse position coded signal. No carrier frequency is required by the infra-red transducers hence C_1 is omitted and a 2.2kΩ resistor substituted for R_1.

Figure 3 **Infra-red transmitter circuit**



The positive pulses appearing on pin 3 are amplified by Q_1, Q_2 and Q_3 to provide high current pulses to supply 3 RS infra-red sources, 308-512.
All wiring to the transmitters should be short with thick conductors and the 470µF electrolytic mounted close to minimise lead inductance.
A suitable p.c.b. (434-807) is available (see current RS catalogue for details).

RS 490 Output and coding

Figure 4a shows the output voltage waveforms from pins 2 and 3 with respect to 0V. A carrier wave is shown as it depicts a typical output for the ultrasonic system. The carrier wave frequency is shown lower than normal for clarity. The RS 490 transmits a codeword as a group of 6 carrier or d.c. pulses (depending on the system being used) continuously for as long as a programme switch is operated. The minimum switch closing time is 6ms and the transmitter will transmit until the end of a codeword even if the switch is released during a word. On completion of the word the device reverts to standby mode. Each of the five intervals between the start of these pulses may take up 2 possible values, a short interval corresponding to a '1' or a long interval corresponding to a '0'. Figure 4b shows the timing relationship between the carrier pulses '1' and '0'. At the end of each word a synchronising interval 'S' is generated to define a codeword ending. The transmitter maintains a fixed relationship between the '1', '0' and 'S' intervals of 2:3:6. Also the width of the carrier pulse is approximately 1/6th of a '1' interval or 1/3:2 on the above ratio scale. From the possible combinations of the 5 bit codeword up to 2^5 or 32 different words can be generated.
A carrier burst of 3ms duration is shown in Figure 4b as an example of the timing relationships.

Figure 4a **P.P.M. output showing ultrasonic carrier frequency**

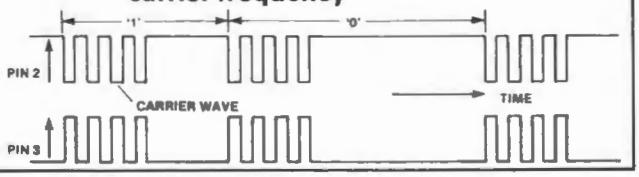
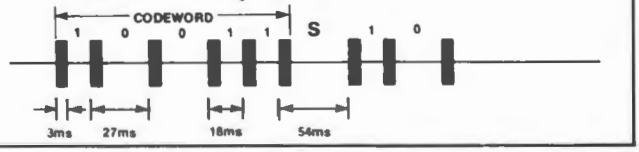


Figure 4b **Ultrasonic transmitter output (for a '1' period of 18ms)**



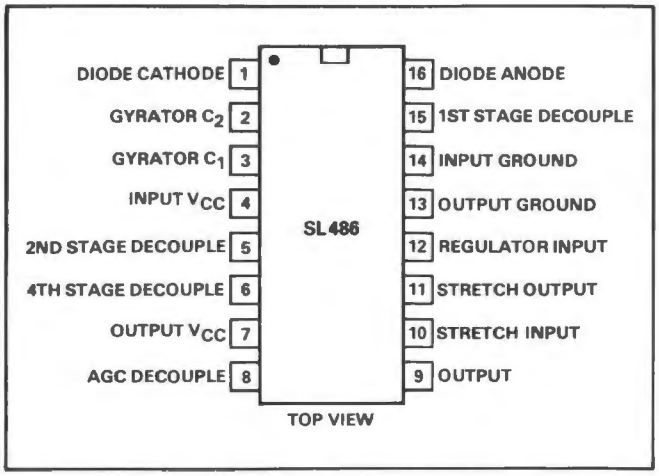
Infra-red pre-amplifier RS 486 (301-527)

A high gain pre-amplifier designed to form an interface between an infra-red receiving diode (308-506) and the digital input of remote control receiving circuits. This i.c. features a fast acting A.G.C. circuit which together with the differential inputs reduce noise pick-up and hence improve performance in noisy environments. An on-chip gyrator circuit allows operation with high brightness background light levels. The device contains two other circuit elements, one to provide a stretched output pulse facility and a voltage regulator to allow operation from a wide range of supplies. 16-pin d.i.l. plastic package.

A suitable p.c.b. (434-891) is available (see current RS catalogue for details).

Features

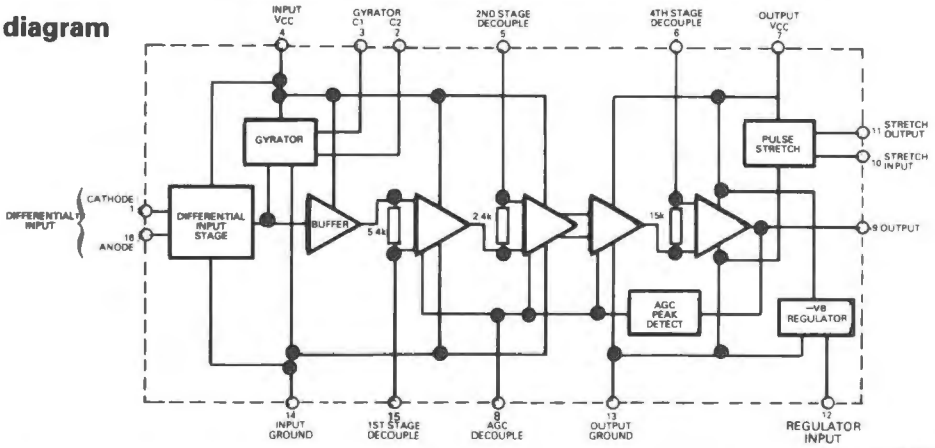
- Fast acting AGC reduces effects of noise
- Differential inputs reduce noise pick-up and improve stability
- Output pulse stretcher for use with microprocessor decoders
- On chip stabiliser
- Low noise input



Absolute maximum ratings

Supply voltage (V Pins 4 and 7)
+10V wrt V Pins 13 and 14
Regulator input voltage (V Pin 12) —20V wrt Pin 7
Output current 5mA
Stretch output current 5mA
Operating temperature range 0°C to +70°C
Storage temperature −55°C to +125°C

Figure 5 **Block diagram**



Electrical characteristics

Test conditions (unless otherwise stated): T_{amb} = 25°C, V_{CC} = 4.5V to 7.0V

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply current	4,7 4		6.0 5.0 +3 I_D	10.0	mA mA	V_{CC} = 5.0V, I_{DIODE} = 1.0μA V_{CC} = 4.5V, I_{DIODE} = 1.5mA
Low voltage supply (external)	4,7(+ve), 13, 14(-ve)	4.5		9.0	V	Input and output V_{CC} commoned input and output ground commoned
High voltage supply (external)	4,7(+ve), 12(-ve)	9.0		18.0	V	Input and output V_{CC} commoned, input and output ground at internal regulated voltage
Internal regulated voltage	13(wrt 7)		−6.4		V	V Pin 7 (+) to V Pin 12(-) = +16V
Voltage between input and output V_{CC}	4,7			1.5	V	At room temperature
Minimum sensitivity of differential input	1,16		5.0		nA	For 4V output pulse, I_{DIODE} = 1.0μA
Common mode rejection	1,16		35.0		dB	
Maximum signal input	1,16		4.0		mA(peak)	
AGC range			68.0		dB	
Output and stretch output pull-up resistance (internal)	9,11		55.0		kΩ	At 25°C

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Stretch output pulse width (T_p) T coefficient on Rx	11		2.4 0.7		ms %/°C	Capacitance Pin 9 to Pin 10 = 10nF ; $T_p \simeq -Rx\ C \ln \frac{1.5}{V_{CC}}$ where Rx = 200kΩ±25% (internal resistance)
Output low	9			Output ground +0.5	V	Output open circuit
Output high	9	Output V_{CC} –0.5			V	Output open circuit
Stretch output low	11			Output ground +0.5	V	Output open circuit
Stretch output high	11	Output V_{CC} –0.5			V	Output open circuit
Sink current stretch output	11			1.8	mA	Low state
Supply rejection, input V_{CC}	4		1.5 0.8		V(peak) V(peak)	Ripple amplitude at 100Hz, Pin 12 ground Ripple amplitude at 100Hz, Pins 13 & 14 ground

Application notes (see Figure 6)

Diode anode and cathode (pins 1 and 16) The infra-red receiving diode is connected between pins 1 and 16. The input circuit is configured so as to reject signals common to both pins. This improves the stability of the device, and greatly reduces the sensitivity to radiated electrical noise. The diode is reverse biased by a nominal 0.65V.

Gyrator C2 and C1 (pins 2 and 3) The decoupling, provided by gyrator C2 and C1, rolls off the gain of the feedback loop which balances the d.c. component of the infra-red diode current. The values of C2 and C1 are chosen to produce a low frequency cut-off characteristic below a nominal 2kHz. Hence, the gyrator produces approximately 20dB rejection at 100Hz.

The gyrator consists of two feedback loops operating in tandem. Only one feedback path is functional when the d.c. component of the diode current is less than 200μA. This loop is decoupled by gyrator C2. For diode currents between 200μA and 1.5mA the second control loop is operative, and this is decoupled by gyrator C1.

The decoupling capacitors, gyrator C2 and C1, must be connected between pins 2 and 3, to pin 4. The series impedance of C2 and C1 should be kept to a minimum.

First stage decouple (pin 15) The capacitor on pin 15 decouples the signal from the non-inverting input of the first difference amplifier (see also Figure 5). The capacitance of 15nF is chosen to produce a 2kHz low frequency roll-off.

The capacitor must be connected between pins 15 and 14 (the input ground).

Second stage decouple (pin 5) The capacitor on pin 5 decouples the signal from the non-inverting input of the second difference amplifier. The capacitance of 33nF is chosen to produce a 2kHz low frequency roll-off. The capacitor must be connected between pins 5 and 4 (the input V_{CC}).

Fourth stage decouple (pin 6) The capacitor on pin 6 decouples the signal from the non-inverting input of the fourth difference amplifier. The capacitance of 4.7nF is chosen to produce a 2kHz low frequency roll-off. The capacitor must be connected between pins 6 and 7 (the output V_{CC}).

A.G.C. decouple/delay adjust (pin 8) The output of the fourth difference amplifier is followed by a peak detector, which is used to provide an A.G.C. control level. This produces a current source which is limited to 10mA at pin 8. The A.G.C. decouple capacitor (C5 normally 150nF) filters the pulsed input, and the resultant level controls the gain of the first three difference amplifiers.

The A.G.C. control level exhibits a fast attack/slow decay characteristic. Immediately infra-red pulses are detected, the gain will be reduced, so that any weaker noise pulses that are also received will not be seen at the output. Thus, provided the infra-red pulses are the most intense, it is possible to receive data in noisy environments. The slow decay keeps the A.G.C. level intact during data reception, and produces a delay before any received noise may become present at the output, when transmission ceases.

Output (pin 9) The output will be low, pulsing high with a source impedance of a nominal 55kΩ, for a received infra-red pulse. It is a linear amplification of the input and swings between output ground and output V_{CC}.

Stretch input and stretch output (pins 10 and 11) A typical infra-red P.P.M. system transmits very narrow pulses. The duration of these pulses is typically 15μs, so in order to utilise a microprocessor based decoder system it is necessary to lengthen the received pulse. This stretched output can be obtained from pin 11 when a capacitor is connected between pins 9 and 10.

The width of the pulse is determined by the value of this coupling capacitor (C8 in Figure 7) and is given by:

$$T_p = -Rx\ C_8 \ln \frac{1.5}{(V_4 - V_{13})}$$

where Tp = pulse width in ms
Rx = 200kΩ (see electrical characteristics)
C_8 = coupling capacitance
and $(V_4 - V_{13})$ = potential between input V_{CC} and ground (pins 4 and 13)

The stretch output is normally high pulsing low for a received infra-red pulse, and swings between output V_{CC} and output ground.

Regulator input (pin 12) The device can be operated with supplies of between 4.5V and 9.0V connected between input/output ground (pins 14 and 13) and input and output V_{CC} (pins 4 and 7) as shown in Figure 6.

The device can be operated with supplies in excess of 9.0V by utilising the on-chip regulator. In this case connections are made between output V_{CC} (pin 7) and the regulator input (pin 12) as shown in Figure 5. A supply voltage of between 9.0V and 18V will then cause the output ground to be regulated at a level nominally 6.4V below the output V_{CC} (pin 7).

The regulator will, however, lose control with a potential difference of less than 9.0V. Below this level the voltage on pin 13 will track nominally 1.5V below the output V_{CC} (pin 12).

When the regulator is not used (low voltage operation), pin 12 must be shorted to output ground (pin 13).

Operational notes (see Figures 6 and 7)

Gyrator C1 (pin 3) If the environment in which the device is operating, limits the background light such that the d.c. component of the diode current has a maximum of 200μA, it may be desirable to omit (see Figure 6) the more bulky and costly 68μF capacitor, gyrator C1 shown in Figure 7. In this case pin 3 can be left open circuit. The resultant application will then have a characteristic of greatly reduced gain when the ambient light causes the d.c. current to rise above this threshold.

The 68μF capacitor can alternatively be replaced by a resistor. The outcome of this is to further reduce the gain in ambient light levels above the 200μA threshold. Below this threshold the overall gain is slightly enhanced as the light level approaches the threshold value. If chosen this resistance should lie between 10kΩ and 200kΩ.

Noise immunity The stretch output can also be used as a means of improving performance relating to a receiver system, over and above its main purpose of providing a stretched output facility. Including C8 (Figure 7) causes the output pulses (from pin 9) to be subjected to the stretch input threshold. Thus any noise pulses from pin 9 that are below this threshold will not be seen at the stretch output (pin 11).

A further improvement can be made, utilising this stretch input threshold by including some additional filtering of the output (C10 in Figure 7). This can be adjusted in value (typically 100pF) to reduce some of the noise pulses that otherwise cross the threshold, to a level below the threshold.

It must be noted that the stretch output logic sense is inverse (for microprocessor applications) from that of the output (pin 9), and the cost of re-inversion may be deemed uneconomical for the improvements gained.

Screening Use of screening for the device, and associated components, improves the performance and immunity to externally radiated noise. The screening method used must protect the sensitive front-end of the device; provided that the diode, pin 1, pin 16, C2 (pin 2) and the first stage decouple (pin 15) are screened, it may be found that for the application considered, the remaining circuitry need not be so protected.

In applications where externally radiated noise is minimal, it may be possible to reduce any screening to pins 1 and 16, and the diode connections, only. In some instances, no screening may be necessary, but this largely depends on the level of radiated noise, the decoupling/filtering employed and the receivers decoding technique.

Decoupling Typical decoupling arrangements for use with or without the regulator, are given in Figures 6 and 7 respectively. When using the

Figure 6 **Circuit diagram of minimum component application (showing low voltage operation)**

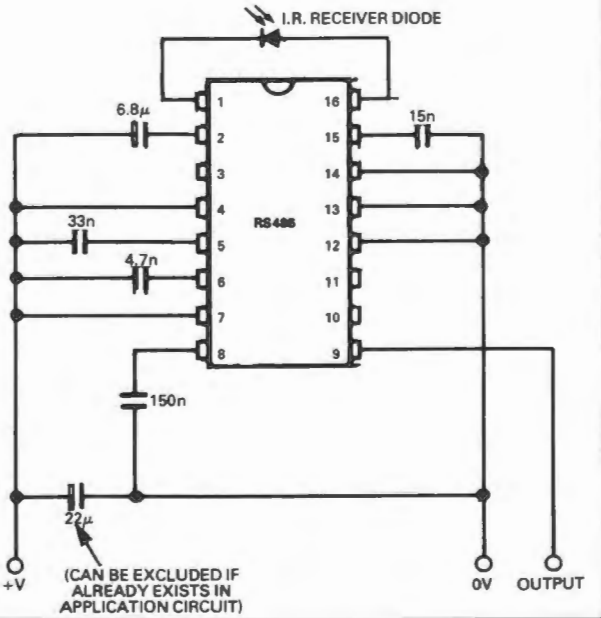
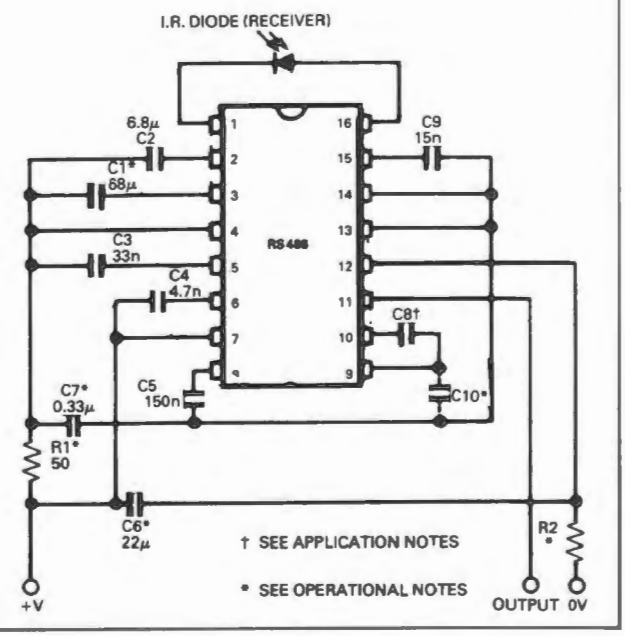
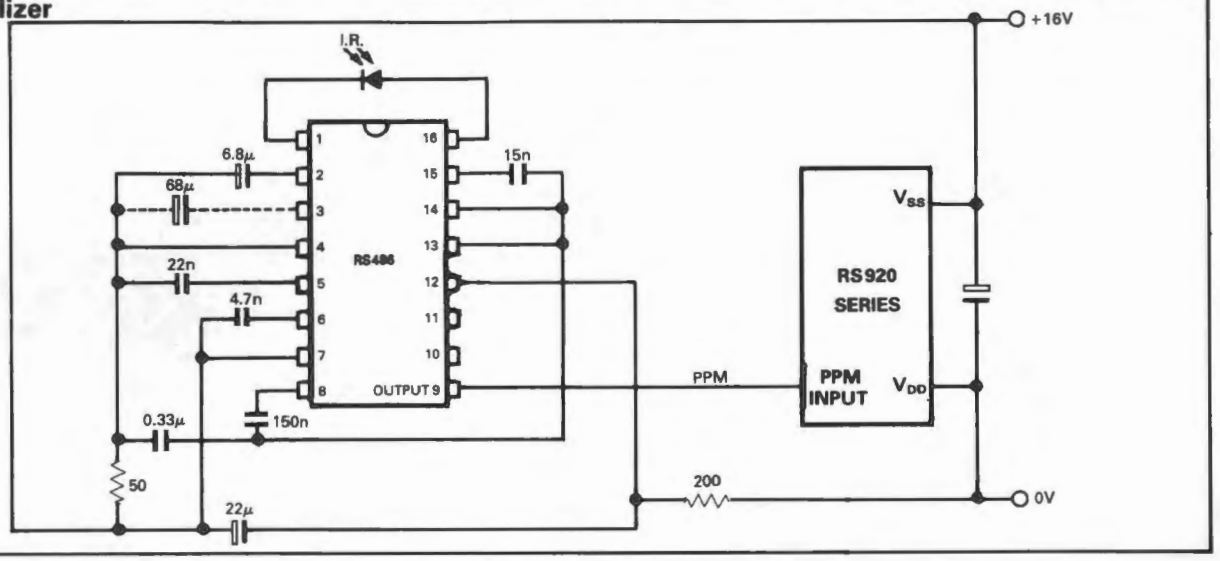


Figure 7 **RS 486 application diagram showing all optional circuitry**
(Note: Supply decoupling and connections for use of voltage regulator; also pulse stretched output)



regulator, further improvements in high frequency supply rejection are possible by the inclusion of R2. The value can be chosen so as to keep the pin 12 end of R2 within the –9.0 to –18V (w.r.t. pin 7) specified voltage range. For example if using the 920 series remote control receivers, on a supply of 16V, a typical value for R2 would be 200Ω.
Note that the regulator is a low impedance point between pins 12 and 13. C7 thus maintains a low impedance path between pins 4 and 12 at high frequencies.

Figure 8 **Application diagram for use with RS920 series remote control receivers, utilising on-chip supply stabilizer**



Remote control receivers: introduction

All of the five remote control receiver i.c.'s have similar signal reception and decoding circuits. The receiver differences are fundamentally confined to the number of P.P.M. codewords to which each responds and the different output functions available.
A general discussion of the circuit operation common to all receivers is given below and each receiver's capabilities are covered later.

Receiver oscillator

After processing by the receiver amplifier the processed P.P.M. signal is transferred to the P.P.M. input of the remote control receiver i.c.
An internal oscillator uses the external components R_1 R_2 and C_1 (see Figures 11 and 13) to generate a frequency in accordance with Eqt. 3.

$$f_{osc} = \frac{1}{0.15\ C_1 R_T} \text{ Hz} \quad \text{Eqt. 3}$$

C_1 in F

$25k\Omega \leq R_1 \leq 200k\Omega$ R_T is the total resistance of R_1 and R_2 in Ω

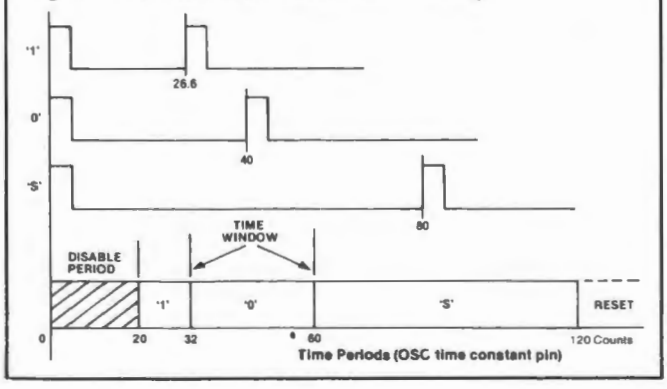
The set frequency of this oscillator is dependent on the received P.P.M. rate from the RS490 transmitter. The importance of this setting is apparent when the internal operation of the receiver is considered.

Internal operation

Whenever a P.P.M. pulse is received by the receiver an internal counter is reset. This counter defines timing windows for the following pulses as shown in Figure 9.

After receipt of the first P.P.M. pulse the counter is reset and disabled for 20 periods of the internal oscillator frequency. This is to reduce the possibility of pulse echoes from multipath reflections between the transmitter and receiver upsetting the correct transmission. If a pulse is received after the counter reaches 20 periods the internal logic examines the spacing or time interval between the receipt of the first pulse and the second and depending on this interval assigns the value '0' or '1' to the pulse spacing. This second pulse again resets the counter and disables it for 20 periods before repeating the above process with the next pulse. In this way the receiver reconstructs the transmitted P.P.M. code, the receipt of an 'S' interval defining the end of the codeword. On receipt of 'S' the receiver verifies that 6 pulses have been received before accepting the code.
The receiver stores this code while receiving another set of P.P.M. pulses. At the end of the second codeword a comparison is made; if the codewords are the same the data is accepted and passed on to a decoder to produce the output function defined by the code; if they are different the first codeword is rejected and the second code used as a reference for comparison with the next code received and no change in an output function occurs. This sequential codeword comparison coupled with P.P.M. and time window checking provides the system with a high degree of noise immunity against producing an incorrect output.
As can be seen from Figure 9 for correct interpretation of the transmitted code each pulse interval for a '0' or '1' must lie within the timing windows defined. This is achieved by setting the 'on chip' oscillator so that 40 periods at the oscillator time constant pin are equal to a '0' interval received at the P.P.M. input. This places a '0' interval at approx-

Figure 9 **P.P.M. Demodulator timing**



imately the centre of the '0' time window hence providing some allowance for oscillator drift both in the transmitter and receiver.

P.P.M. rate selection

The minimum time taken for any receiver to respond to a transmitter command is twice the time to transmit the appropriate codeword, because of the error checking logic. This delay is dependent on the P.P.M. rate chosen at the transmitter and in the example shown in Figure 4b the receiver will respond to the code 10011 in a minimum time of 324 milliseconds. For the discrete outputs this delay is usually of little significance, however, for each step of an analogue output two codewords have to be received. Taking the 'analogue 1+' command 10100 and using the P.P.M. rate shown in Figure 4b one word is 171ms long. The minimum time for the receiver to respond is 342ms. To complete all the 32 steps of 'analogue 1–' would take approximately 11 secs. Hence the P.P.M. rate at the transmitter end of the ultrasonic link should be chosen to provide the desired full range analogue output sweep time.

Using the RS ultrasonic transducers the P.P.M. rate is limited by the rise time of the transmitter (tr ≈ 2ms).

The recommended P.P.M. rate is 37 bit/sec corresponding to a t_0 time of 27ms as shown in Figure 4b. This rate can be increased to approximately 74bit/sec, by using a t_0 time of 13ms, with some loss of range caused by the transducer rise time limitation. The spread in the characteristics of the transducers may increase or reduce this figure.

The infra-red system can be operated up to the maximum P.P.M. rate of the transmitter i.e. 10kbit/sec.

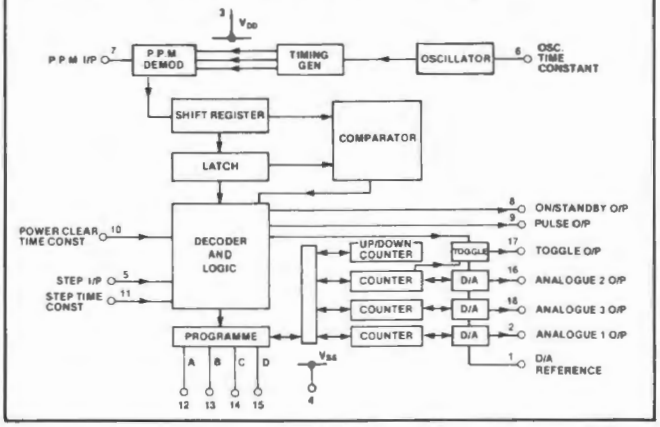
Each receiver i.c. responds to a specific set of codewords from the RS490 transmitter. A description of each receiver type follows.

Remote control receiver RS922 (308-089)

The RS922 is the remote control receiver i.c. for use with the RS490 transmitter.

The P.P.M. codewords transmitted by the 490 are interpreted by the 922 receiver and double checked for timing or codeword errors before being translated into particular control functions. These functions include latched 4-bit B.C.D. outputs (permitting up to 10 switched outputs), 3 indepedent static D/A converters to provide 32 steps of analogue control and 3 other digital control outputs. All digital outputs are C-MOS compatible.

Figure 10 **RS922 Receiver block diagram**



Absolute maximum ratings (V_{DD} = 0V)

Supply voltage V_{SS} ——— +0.3V to –25V
Voltage at any input ——— +0.3V to –25V
Maximum power dissipation ——— 600mW
Operating temperature range ——— –10°C to +65°C
Storage temperature range ——— –55°C to +125°C

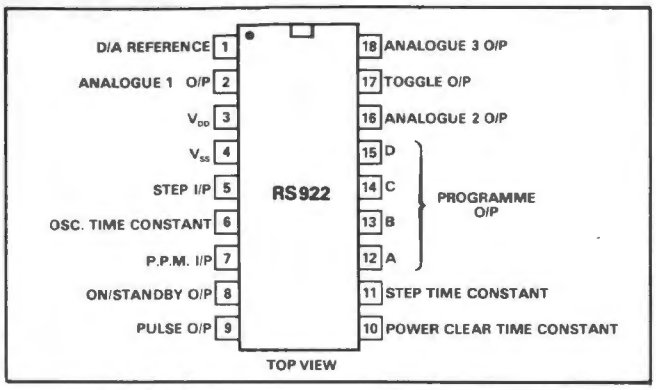
Electrical characteristics

T_{amb} = 25°C, V_{DD} = 0V, V_{SS} = +16V

Characteristic	Pin	Value				Conditions
		Min.	Typ.	Max.	Units	
Operating voltage	4	–14		–18	V	
Supply current	3		8	14	mA	
Input logic level '0'	5	15		16	V	
'1'		0		3.5	V	
Output logic level '0'	8, 9, 12, 15, 17	15		16	V	50k to V_{DD}
'1'		V_{DD}		0.5	V	50k to V_{DD}
Analogue outputs current range	2, 16, 18	0		$\frac{31}{8}$	I_{ref}	3k9 to V_{DD}
Analogue step size	2, 16, 18	0	1/8	1/4	I_{ref}	V_{out}<(V_{SS}–5) V
D/A reference, I_{ref}	1	–250	–345	–455	μA	33k to V_{DD}
Oscillator timing	6		1.6		kHz	C = 82n, R = 50k
Power clear time constant	10		400		ms	C = 4μ7 R = 100k
Step time constant	11		2		s	C = 470n R = 3M3
PPM input logic level high	7	15		16	V	
PPM input logic level low	7	0		10	V	
PPM input pulse width	7	1		$22T_{OSC}$	μs	

Features

- Accepts 5 bit P.P.M.
- All timing from on-chip oscillator
- Suitable for ultrasonic or infra-red systems
- Up to 10 programmes with latched binary outputs
- Incorporates error protection
- Negative logic



This receiver accepts 21 of the transmitted codewords. The command set and output functions for each pin are given in Tables 1 and 2 respectively. The RS922 receiver features a parallel 4-bit latched binary output with 10 output codes, 3 independent analogue outputs and 3 other digital outputs.

Table 1 **Basic 21 command set for RS922 receiver**

Transmitter code	Function	Programme O/P's D C B A
EDCBA		
0000X	Programme 1	0 0 0 0
0001X	Programme 2	0 0 0 1
0010X	Programme 3	0 0 1 0
0011X	Programme 4	0 0 1 1
0100X	Programme 5	0 1 0 0
0101X	Programme 6	0 1 0 1
0110X	Programme 7	0 1 1 0
0111X	Programme 8	0 1 1 1
1000X	Programme 9	1 0 0 0
1001X	Programme 10	1 0 0 1
10100	Analogue 1 +	
10101	Programme Step +	
10110	Analogue 2 +	x = Don't care digit
10111	Analogue 3 +	
11000	Standby	
11001	Toggle O/P (Analogue 2)	
11011	Normalise	i.e. 00110 and 00111 both produce programme 4
11100	Analogue 1 −	
11101	Programme Step −	
11110	Analogue 2 −	
11111	Analogue 3 −	

N.B. LOGIC CONVENTION RS922
Logic '0' – output transistor ON - pulls output to V_{SS}
Logic '1' – output transistor OFF i.e.: NEGATIVE LOGIC

The 'Initial' condition

This describes the state of the outputs of the RS922 receiver every time power is applied and no P.P.M. data has been received.

Programme O/P's – ABCD 0000
Analogue O/P's – All at 12/8 I_{ref}
On/Standby O/P – Logic 0
Pulse O/P – Logic 0
Toggle O/P – Logic 1

Note: Logic '0' is ≈ +14 to +15V
Logic '1' is 0 to +0.5V
measured w.r.t. V_{DD} (0V)

The 'Normalised' condition

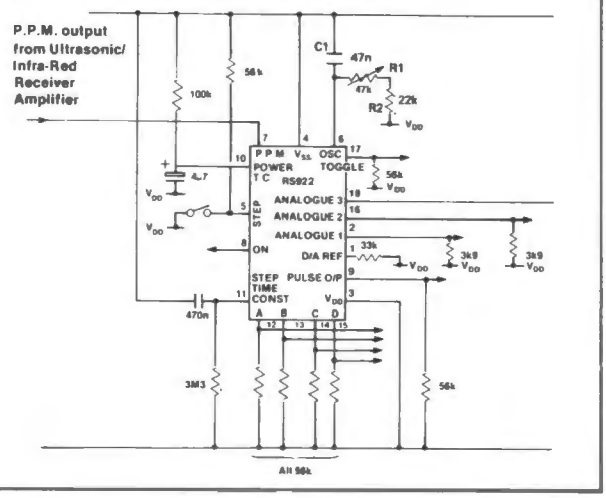
Reception of the 'Normalise' command 11011 affects the following outputs only:

Analogue O/P's – Taken to 12/8 I_{ref}
Toggle O/P – Taken to 1 or 0 (see Table 2)

Table 2 **Pin functions of RS922**

Pin No.	Name	Function
1	D/A Reference	A current drain I_{ref} set by a single external resistor which fixes the nominal step of the analogue O/P's to $I_{ref}/8$.
2, 16, 18	Analogue O/P's 1, 2, 3	These 3 outputs are from three static 5 bit current mirror converters. They are referenced to the current drawn from pin 1, I_{ref} and provide 32 steps, $I_{ref}/8$ from 0 to 31/8 I_{ref} The 'initial' and normalised' condition is 12/8 I_{ref}.
5	Step I/P	Connecting this pin to V_{DD} causes the programme outputs to step up by 1. The time period between steps is defined by the RC network connected to pin 11. The programme output will continue to step for as long as Step I/P is held at V_{DD}, continually cycling.
6	Osc. time	An RC time constant connected to this pin defines the internal oscillator frequency. This frequency controls the timing windows for the incoming P.P.M. pulses from the RS490 transmitter.
7	P.P.M. I/P	The output of the receiver amplifier provides positive P.P.M. pulses which supply the data input to this pin. With no signal this I/P is held low.
8	On/Standby O/P	An open drain O/P with an initial condition of logic 0. This output remains at this level until a programme codeword or programme step is received whereupon it changes to a logic 1. The 'standby' codeword 11000 returns the output to logic 0 until a programme change is commanded. No other codes affect this output.
9	Pulse O/P	This is an open drain O/P with an initial condition of logic 0. A logic 1 pulse is produced on receipt of a programme codeword or programme step command. The width of the 1 pulse is equal to the periodic time of the internal oscillator which can be monitored on pin 6. This pulse is repeated as long as the programme codeword or programme step command is activated. The repetition period is equal to the time taken to transmit the appropriate programme codeword or step command.
10	Power Clear Time Constant	A single RC network connected to this pin defines the time delay before the 'initial' conditions are established, nominally set to 2 sec. by the components indicated in Figure 4.
11	Step Time Constant	An RC network connected to this pin defines the time period between increments of the channel number when the programme step codewords are transmitted.
12, 13, 14, 15	Programme O/P's	These are latched 4 bit binary outputs which respond to the programme transmitter codes and the programme codes. When power is first applied to the receiver programme 1 is established ie. ABCD outputs are all at logic 0 corresponding to programme 1.
17	Toggle O/P	This pin has an 'initial' condition of logic 1 and the only changes to logic 0 when Analogue 2 O/P is at the zero level. Transmission of the 'toggle' command 11001 changes this output to 0 or 1 for each separate transmission of toggle, provided Analogue 2 O/P is not at the zero level.

Figure 11 **RS922 Receiver circuit**



RS922 Analogue O/P's

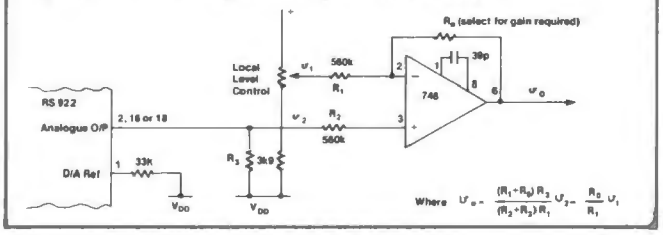
Analogue 1, 2, 3 '+' transmitter codes cause the respective analogue outputs to step up for as long as the transmitter code is being received until the maximum value of I_{ref} is reached at which point continued receipt of the analogue '+' codes have no effect. Similarly the analogue '–' transmitter codes cause the respective output to step down until I_{ref} reaches zero where it remains even under further transmitter command.

The step for the analogue outputs is typically 1/8 I_{ref} and the analogue output current range is 0 to 31/8 I_{ref} hence 32 discrete levels (typically 0 to 1.3mA) are possible from each analogue output.

The analogue outputs are current sources and should normally feed 3.9kΩ sink resistors connected to the V_{DD} and 0V rail. Greatest linearity is obtained if the current sink resistors do not exceed 3.9kΩ giving a 0 to 5V D/A output control range. However a 0 to 10V range may be obtained with higher resistor values if some reduction in linearity of step size can be tolerated. The simplest form of local adjustment of analogue control levels is to make the current sink resistors variable. An analogue output interface circuit is shown below which increases the analogue O/P current and voltage capability without loss of linearity.

A suitable p.c.b. (434-813) is available.

Figure 12 **Analogue output interface**



Remote control receivers RS928 and 929 (309-997 and 305-248)

The RS928 and RS929 are general purpose remote control receiver i.c.'s which function in a similar way to the RS922 device. They each respond to 16 of the possible 32 p.p.m. codewords transmitted by the 490 transmitter i.c. to provide 16 latched, 4-bit binary outputs.

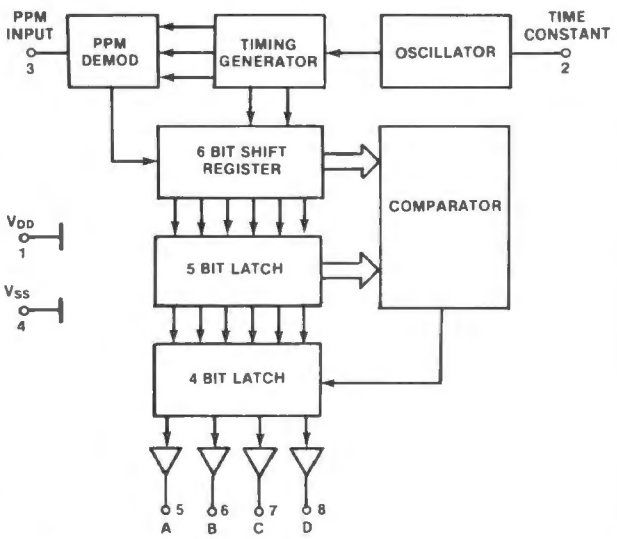
Each i.c. responds exclusively to only 16 of the 32 codewords, the 928 accepting 00000 to 01111 and 929 accepting 10000 to 11111.

8-pin d.i.l. plastic package.

Absolute maximum ratings

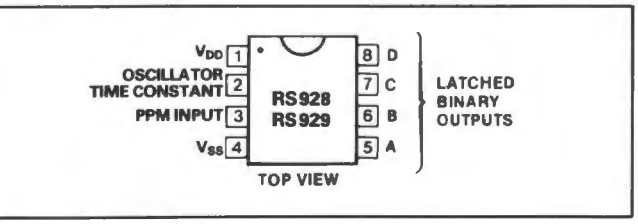
V_{SS} supply and inputs w.r.t. V_{DD} ——— –0.3V to +25V
Storage temperature ——— –55°C to +125°C
Operating temperature ambient ——— –10°C to +65°C

Figure 13 **RS928 and 929 block diagram**



Features

- Accepts 5 bit P.P.M.
- On chip oscillator
- Four high drive outputs
- 16 latched stages
- Negative logic



Electrical characteristics

Test conditions (unless otherwise stated):
V_{SS} = 0V
V_{DD} = −16V
T_{amb} = +25°C

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Current Consumption V_{DD}	1	3	4	5	mA	
Supply voltage	1	−12		−18	V	
PPM input	3					
Logic '0' level		−1		0	V	
Logic '1' level		V_{DD}		−6	V	
Input pulse width		1		$22T_{OSC}$	μs	$T_{OSC} = \frac{1}{f_{OSC}}$
Oscillator timing	2					
Frequency		15		150k	Hz	
			3k		Hz	Typical TC: 22nF to V_{SS}, 100kΩ to V_{DD}
Variation w.r.t. V_{DD}			1		%/V	
Latched binary output	5, 6, 7, 8					
Logic '0' output voltage		−1.5		0V	V	RL = 3.0k to VDD
Output leakage in logic '1' state				1	μA	

Note 1: R_{OSC} (pin 2) is 56k-156k Ω. $f_{OSC} \simeq \frac{1}{0.15CR}$ ±20%.

Remote control receivers RS926 and 927 (309-981 and 303-826)

The RS926 and RS927 are remote control receiver i.c.'s which each respond to 15 of the 32 p.p.m. codewords from the 490 transmitter to provide 15 unlatched, 4-bit binary outputs. The outputs remain in an activated state for as long as a valid code is being received and are switched off when no valid code is detected. Codeword response: 00001 to 01111 (926), 10001 to 11111 (927).

8-pin d.i.l. plastic package.

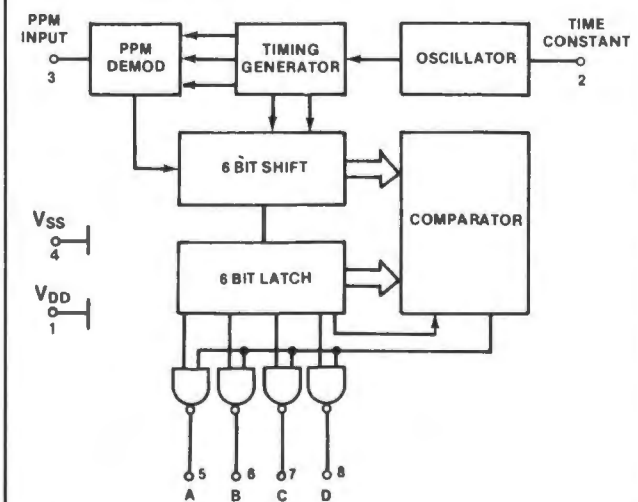
Absolute maximum ratings

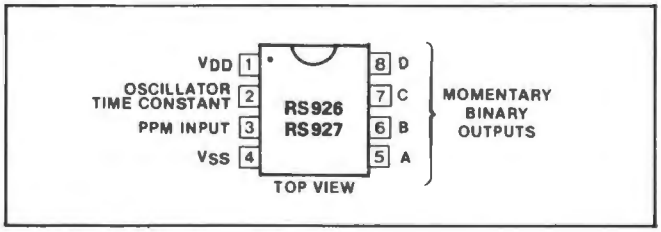
V_{SS} supply and inputs w.r.t. V_{DD} ..... +0.3V to −25V
Storage temperature ..... −55°C to +125°C
Operating temperature ambient ..... −10°C to +65°C

Features

- Accepts 5 bit P.P.M.
- Four outputs indicate in binary the code currently being received, and are switched off when no valid code is detected
- On chip oscillator
- High power, free drain, output buffers
- Positive logic

Figure 14 **RS926 and 927 block diagram**





Electrical characteristics

Test conditions (unless otherwise stated):
$V_{SS} = 0V$
$V_{DD} = -16V$
$T_{amb} = +25°C$

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Operating supply voltage range		−12	−14	−18	V	
Current consumption	1	2	3	4	mA	
PPM input						
Input level high	3	−1		0	V	
Input level low	3	V_{DD}		−6	V	
Input pulse width	3	1		$22T_{OSC}$	μsec	$T = \frac{1}{f_{OSC}}$
Oscillator time constant See Note 1						
Oscillator frequency	2	15		150k	Hz	
			3k		Hz	Typical TC: 22nF to V_{SS} 100k to V_{DD}
Variation wrt V_{DD}			1		%/V	
Output voltage high	5-8	−1.5		0	V	R_L = 3.0k to VDD
Output device leakage (Output OFF)	5-8			1	μA	

Note 1: R_{OSC} (pin 2) is 56k-156k Ω. $f_{OSC} \simeq \frac{1}{0.15CR} \pm 20\%$.

RS 928, 926, 927 and 929 receivers

The RS928 and 929 have parallel 4-bit binary latched open drain outputs only and respond to 16 codewords each. They are identical in circuit operation and application and differ only in their command sets, as shown in Table 3.

The RS926 and 927 respond to 15 codewords each as shown in Table 3. The circuit applications for the RS928 and 929 are equally applicable to the RS926 and 927. The outputs of the 926 and 927 differ from the 928 and 929 by being 4-bit parallel momentary outputs and not latched and are of opposite logic convention. The outputs are activated for as long as a valid code is being received and return to their inactive 'off' state under no signal conditions.

A typical basic circuit application is given in Figure 15. The outputs are capable of driving visible L.E.D.'s, opto-coupled thyristors/triacs or alternatively the 4-bit binary outputs can be decoded using a 4028B CMOS logic i.c. to provide up to 10 outputs or a 4514B to produce the full 16 outputs.

Figure 15 **RS928/9 and 926/7 circuit**

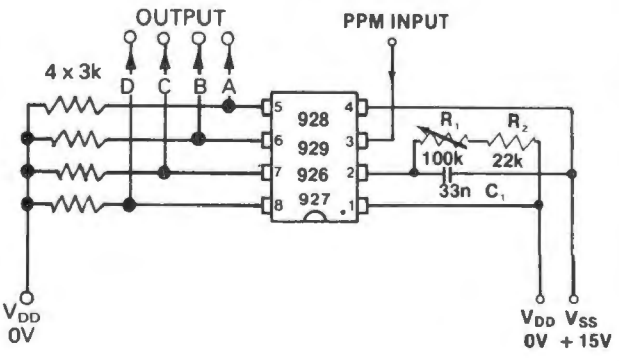


Table 3 **Command set 928/9 & 926/7**

RS490 Transmitter Code	RS928/8	RS927/9
E D C B A	D C B A	D C B A
0 0 0 0 0	0 0 0 0	
0 0 0 0 1	0 0 0 1	
0 0 0 1 0	0 0 1 0	
0 0 0 1 1	0 0 1 1	
0 0 1 0 0	0 1 0 0	
0 0 1 0 1	0 1 0 1	
0 0 1 1 0	0 1 1 0	
0 0 1 1 1	0 1 1 1	
0 1 0 0 0	1 0 0 0	
0 1 0 0 1	1 0 0 1	No change
0 1 0 1 0	1 0 1 0	
0 1 0 1 1	1 0 1 1	
0 1 1 0 0	1 1 0 0	
0 1 1 0 1	1 1 0 1	
0 1 1 1 0	1 1 1 0	
0 1 1 1 1	1 1 1 1	
1 0 0 0 0		0 0 0 0
1 0 0 0 1		0 0 0 1
1 0 0 1 0		0 0 1 0
1 0 0 1 1		0 0 1 1
1 0 1 0 0		0 1 0 0
1 0 1 0 1		0 1 0 1
1 0 1 1 0		0 1 1 0
1 1 1 1 1		0 1 1 1
1 1 0 0 0	No change	1 0 0 0
1 1 0 0 1		1 0 0 1
1 1 0 1 0		1 0 1 0
1 1 0 1 1		1 0 1 1
1 1 1 0 0		1 1 0 0
1 1 1 0 1		1 1 0 1
1 1 1 1 0		1 1 1 0
1 1 1 1 1		1 1 1 1

N.B. LOGIC CONVENTION
RS928 & RS929 (Latching output)
Logic '0' – output transistor ON
– pulls output to V_{SS}
Logic '1' – output transistor OFF
ie: **NEGATIVE LOGIC**
RS926 & RS927 (Momentary outputs)
Logic '0' – output transistor OFF
Logic '1' – output transistor ON
– pulls output to V_{SS}
ie: **POSITIVE LOGIC**

Applications

Ultrasonic control system

Setting up procedure

Transmitter

The potentiometers R_A and R_B in the transmitter circuit shown in Figure 2 require adjustment to define the carrier frequency and P.P.M. rate required.

Activate the switch controlling transmitter code

0000X and monitor the output waveform of the transmitter i.c. appearing at pins 2 and 3. Expanding one of the pulses displayed, adjust R_B to produce a carrier period of approximately 24.5μs corresponding to a frequency of 40.8kHz. Display several pulses of the transmitter code and by adjusting R_A alter the time interval for a '0' to provide the required P.P.M. rate (see Figure 4b).

Receiver

A)
Position the transmitter and receiver transducers 3m apart. Activate the transmitter to produce the codeword 0000X continuously and monitor the P.P.M. I/P pin on the receiver i.c.

B)
Re-adjust R_B controlling the carrier frequency on the transmitter circuit to provide a maximum signal at the P.P.M.. I/P of the receiver i.c. Finally monitor the oscillator waveform on the oscillator time constant pin of the receiver i.c. and adjust R_1 so that the periodic time is 1/40th of the time of a '0' interval on the received P.P.M.

Infra-red control system

Setting up procedure

Transmitter

The potentiometer R_A shown in Figure 3 should be adjusted for the required P.P.M. rate, following the same procedure outlined for the ultrasonic system.

Receiver

Follow part A of the setting up procedure for the ultrasonic system. Monitor the oscillator waveform on the osc time constant pin of the receiver i.c. and adjust R_1, so that the periodic time is 1/40th of the time of a '0' interval on the received P.P.M. of the appropriate input pin.

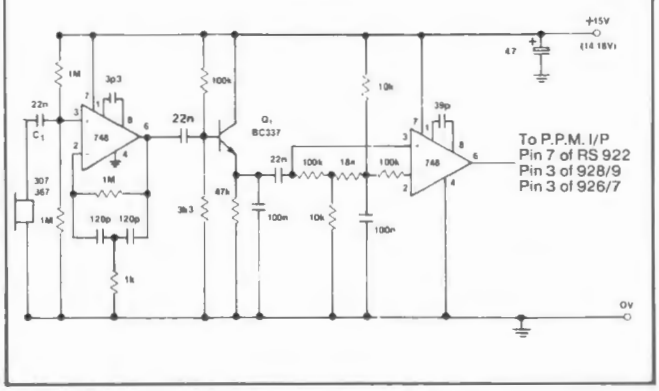
Additional circuits

Receiver amplifier (ultrasonic)

At the receiving end of the ultrasonic link a gain and bandwidth defining system will be required before the incoming signal is suitable for reception by the remote control receivers.

Figure 16 shows a suitable two stage amplifier designed for receiving signals from the RS ultrasonic transducer, 307-367.

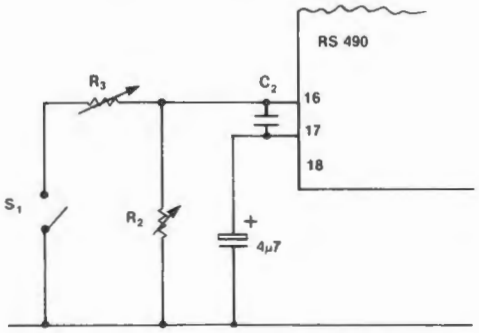
Figure 16 **Ultrasonic receiver amplifier**



Transmitter control for 2 receivers

Figure 17 illustrates a method of employing one RS490 transmitter to control two independent receivers. The P.P.M. rate for one receiver is selected by the potentiometer R_2. The second receiver should be adjusted to receive the P.P.M. rate defined by the parallel combination of R_2 and R_3. The two different P.P.M. rates can be chosen such that data accepted by one receiver is outside the timing windows defined by the oscillator time constant of the other. The P.P.M. rates should be within the limitations of the transducer, only one receiver amplifier being required to directly feed the P.P.M. inputs on the two receivers.

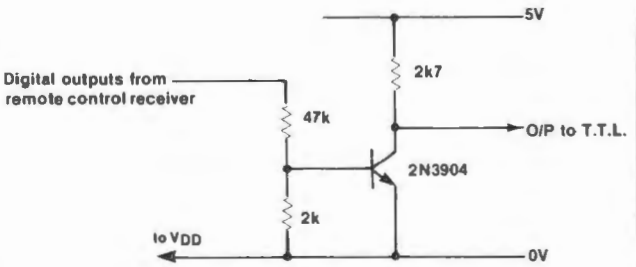
Figure 17 **Transmitter modification for controlling two receivers**



T.T.L. interface

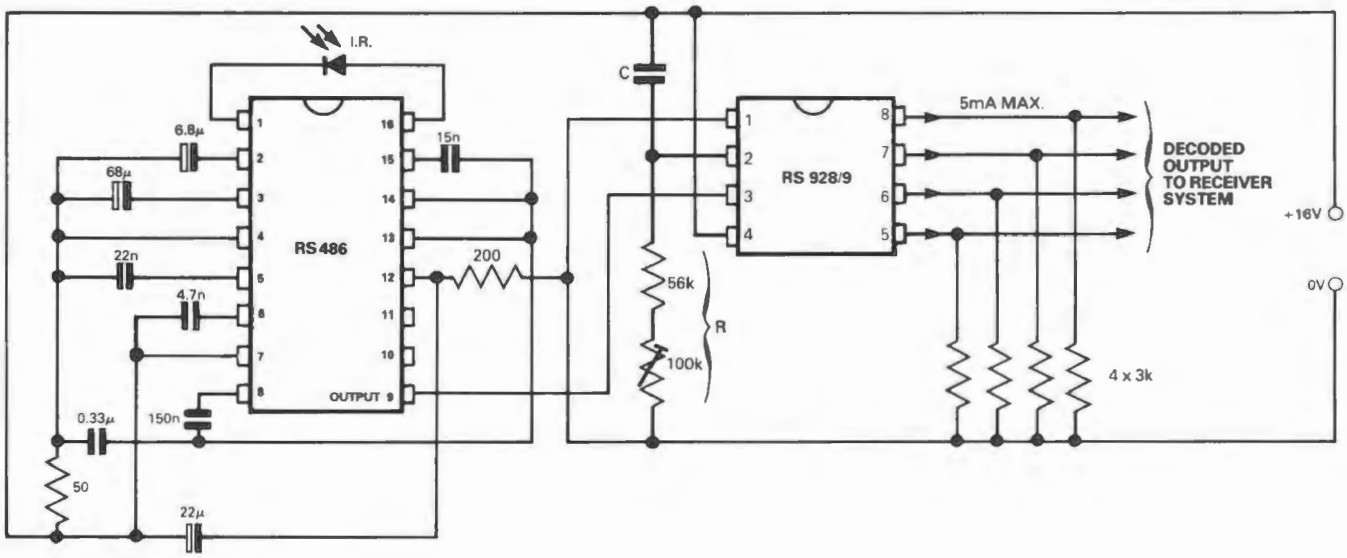
Figure 18 shows a simple interface between logic level outputs of the remote control receiver i.c.'s, to standard T.T.L. inputs. This circuit also inverts the logic levels, a logic 1 from the receiver producing a logic 0 T.T.L. output.

Figure 18 **T.T.L. interface**



RS data

Figure 19 **Typical application circuit**



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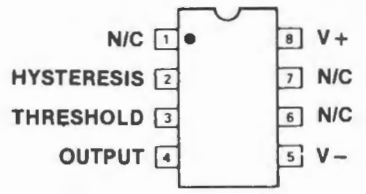
RS data

Micropower voltage detector

Stock number 283-249

The RS 8211 is a bipolar micropower voltage detector/indicator I.C. containing an accurate voltage reference, comparator and a pair of output buffer/drivers. This device provides a 7mA current limited output sink when the voltage applied to the 'Threshold' terminal is less than 1.5 volts (the internal reference). This I.C. also has a low current output (hysteresis output) which is switched on for input voltages in excess of 1.15V. The hysteresis output may be used to provide positive and noise free output switching using a simple feedback network.

CONNECTION DIAGRAM



TOP VIEW

Typical applications for the device are low battery indicators (portable systems), power supply malfunction detectors for volatile memory systems, etc.

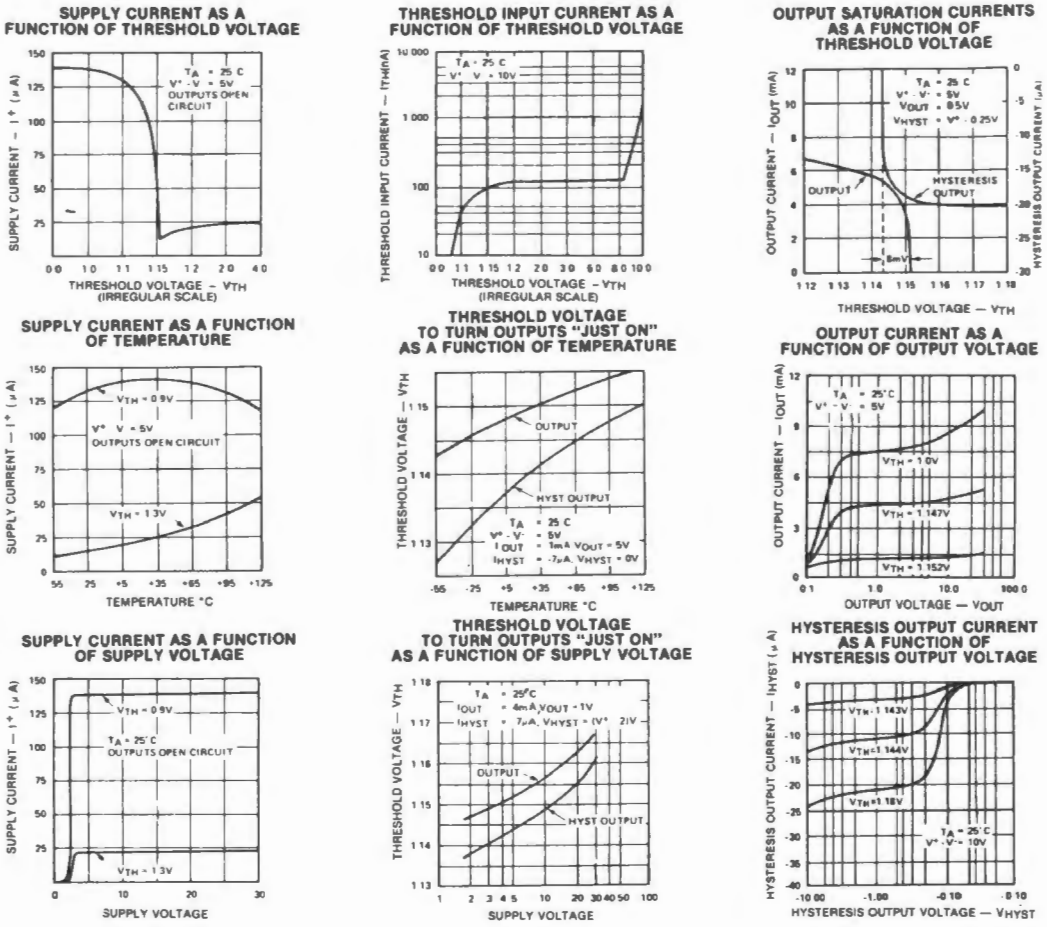
Absolute maximum ratings (Note 1)

Supply Voltage ($V+ - V-$) ——— −0.5 to +30 volts
Output Voltage
−0.5 to +30 volts with respect to V−
Hysteresis Voltage
+0.5 to −10 volts with respect to V−
Threshold Input Voltage
+30 to −5 volts with respect to V−
and +0 to −30 volts with respect to V+
Current into Any Terminal ——— ±50mA
Power Dissipation (Note 2) ——— 300mW
Operating Temperature Range ——— 0 to +70°C
Storage Temperature Range ——— −55°C to +125°C

NOTE 1: Absolute maximum ratings define parameter limits that if exceeded may permanently damage or change the device.
NOTE 2: Derate linearly above 50°C by — 10m W/°C.
NOTE 3: The maximum output current of the RS8211 is limited by design to 12 mA under any operating condition. The output voltage may be sustained at any voltage up to + 30 with respect to V− as long as the maximum power dissipation of the device is not exceeded.

Typical operating characteristics $V+ - V- = 5V$, $T_A = 25°C$ unless otherwise specified

Parameter	Symbol	Conditions	RS 8211 Min.	RS 8211 Typ.	RS 8211 Max.	Units
Supply Current	$I+$	$2.0 < V+ - V- < 30$ $V_T = 1.3V$ $V_T = 0.9V$	 10 50	 22 140	 40 250	 μA μA
Threshold Trip Voltage	$V_{TH\ (TRIP)}$	$I_{OUT} = 4mA$ $V+ - V- = 5V$ $V_{OUT} = 2V$ $V+ - V- = 2V$ $V+ - V- = 30V$	0.98 0.98 1.00	1.15 1.145 1.165	1.19 1.19 1.20	V V V
Threshold Voltage Disparity Between Output and Hysteresis Output		$I_{OUT} = 4mA$ $V_{OUT} = 2V$ $I_{HYST} = 7\mu A$ $V_{HYST} = 3V$		−8.0		mV
Guaranteed Operating Supply Voltage Range		+25°C 0 to +70°C	2.0 2.2		30 30	V V
Threshold Trip Voltage Temperature Coefficient		$I_{OUT} = 4mA$ $V_{OUT} = 2V$		+200		ppm/°C
Variation of Threshold Trip Voltage with Supply Voltage		$\Delta(V+ - V-) = 10\%$ at $V+ - V- = 5V$		1.0		mV
Threshold Input Current	I_{TH}	$V_{TH} = 1.15V$ $V_{TH} = 1.00V$		100 5	250	nA nA
Output Leakage Current		$V_{OUT} = 5V$ $V_{TH} = 1.3V$ $V_{OUT} = 30V$ $V_{TH} = 1.3V$			1 10	μA μA
Output Saturation Voltage	$V_{OUT\ (SAT)}$	$I_{OUT} = 4mA$ $V_{TH} = 1.0V$		0.17	0.4	V
Max Available Output Current	$I_{OUT\ (MAX)}$	(Note 3) $V_{TH} = 1.0V$ $V_{OUT} = 5V$	4	7.0	12	mA
Hysteresis Leakage Current		$V+ - V- = 10V$ $V_{TH} = 1.0V$ $V_{HYST} = V-$			0.1	μA
Hysteresis Sat. Voltage	$V_{HYST\ (SAT)}$	$I_{HYST} = -7\mu A$ $V_{TH} = 1.3V$ measured with respect to V+		−0.1	−0.2	V
Max Available Hysteresis Current	$I_{HYST\ (MAX)}$	$V_{TH} = 1.3V$	−15	−21		μA



General information

Threshold input considerations

Any voltage may be applied to the THRESHOLD terminal (pin 3), having a value between — 5 volts with respect to V— to a maximum of V+, as long as the absolute value of the peak to peak input does not exceed 30 volts. It is recommended however, that the THRESHOLD voltage does not exceed about + 6 volts with respect to V— since above that voltage the threshold input current increases sharply (see above graph).

The outputs change state with an input THRESHOLD voltage of approximately 1.15 volts. Input and output wave forms are shown in Figure 1 for a simple 1.15 volt level detector.

The HYSTERESIS output (pin 2) is a low current output complementary to OUTPUT (pin 4) and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that the output currents be limited to 10μA or less.

The OUTPUT terminal of the RS 8211 may be used to drive most of the common logic families such as TTL or C-MOS using a single pull-up resistor. The guaranteed TTL fanout for the RS8211 is 2.

Figure 1. **Voltage level detection**

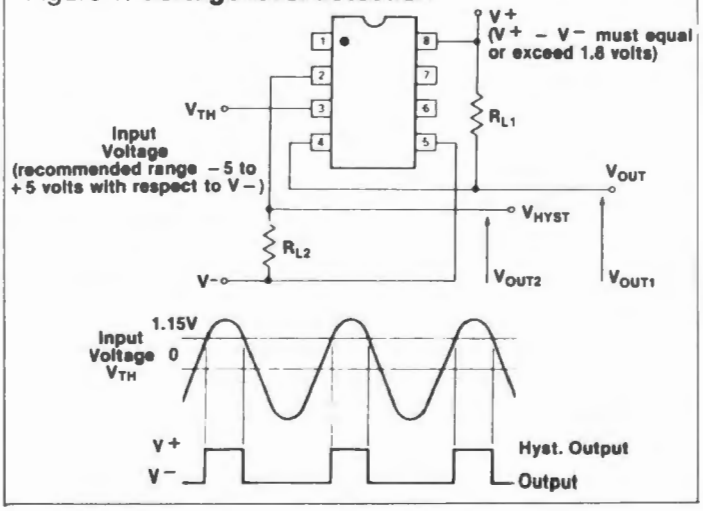
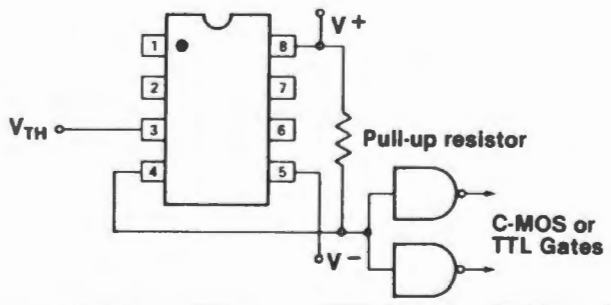


Figure 2. **Output logic interface**



A principal application of the RS8211 is voltage level detection and for that reason the OUTPUT current has been limited to typically 7mA to permit direct drive to an l.e.d. lamp connected to the positive supply V+ without a series current limiting resistor.

In many applications an input resistor divider network will be used. It is recommended that the current in this resistor network necessary to produce 1.15 volts be as follows:

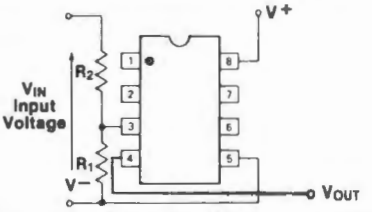
Where the current is a concern (e.g. battery operated systems) a current of 6 to 8μA represents a good compromise between accuracy and low power. Lower currents than 6μ A are usable if accuracy is not important. The inaccuracy at lower currents is due to the input current of the device becoming a significant percentage of the current flowing in the resistor network. If the current in this network is of no concern, a current of 50μ A may be used.

Setup procedures for voltage level detection

Case 1. Simple voltage detection—no hysteresis.

Unless an input voltage of approximately 1.15 volts is to be detected resistor networks will be used to divide the unknown voltage to be sensed. Figure 3 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity with respect to the negative supply V—.

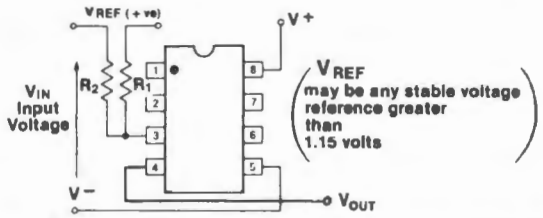
Figure 3. **Input resistor network setup procedures**



a) Range of input voltage greater than +1·5 volts with respect to V−.

Input voltage to change the output states (V_T)

$$= \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts} \quad (V_{OUT} \text{ low for } V_{IN} < V_T)$$



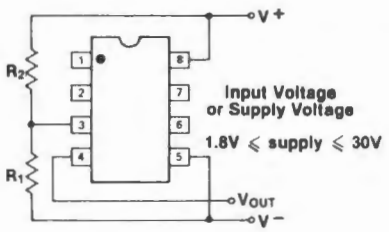
b) Range of input voltage less than +1.15 volts with respect to V−

Input voltage to change the output states (V_T)

$$= \frac{(R_1 + R_2) \times 1.15}{R_1} - \frac{R_2 \times V_{REF}}{R_1} \quad (V_{OUT} \text{ high for } V_{IN} < V_T)$$

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 4.

Figure 4. **Combined input and supply voltages**



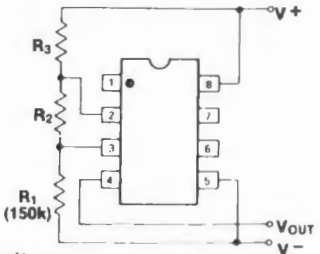
Case 2. Use of the HYSTERESIS function.

The disadvantage of the simple detection circuits is that there is a small but infinite input range whereby the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and to turn the ouputs OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection, (refer to practical applications section).

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figures 5a and 5b.

Figure 5a, 5b. **Two alternative voltage detection circuits employing hysteresis to provide pairs of well defined trip voltages**

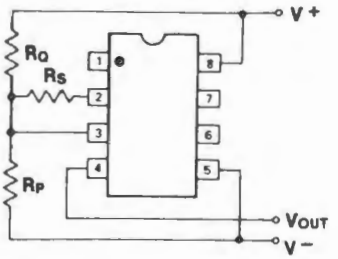


(5a) Low trip voltage

$$V_T1 = \left[\frac{(R_1 + R_2) \times 1.15}{R_1}\right] + 0.1 \text{ volts}$$

High trip voltage

$$V_T2 = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15 \text{ volts}$$

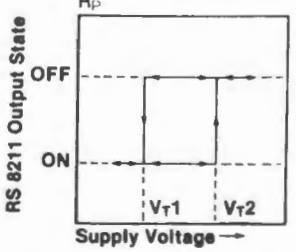


(5b) Low trip voltage

$$V_T1 = \left[\frac{R_O R_S}{(R_O + R_S)} + R_P\right] \times \frac{1}{R_P} \times 1.15 \text{ volts}$$

High trip voltage

$$V_T2 = \frac{(R_P + R_O)}{R_P} \times 1.15 \text{ volts}$$

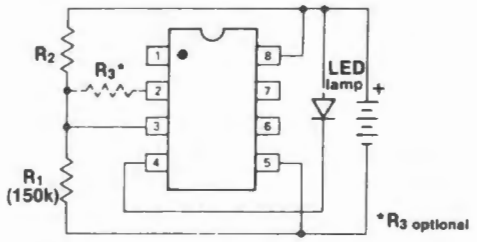


Circuit (5a) requires that the full current flowing in the resistor network ($R_1 + R_2$) be sourced by the HYSTERESIS output whereas for circuit (5b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis circuit (5b) is to be preferred due to the offset voltage of the hysteresis output transistor.

Practical applications

a) Low voltage battery indicator

Figure 6. **Low voltage battery indicator**

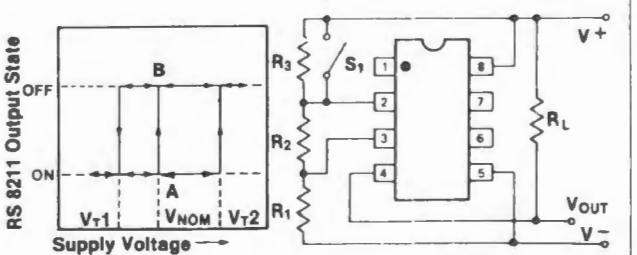


This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35μA which will increase to 7mA when the lamp is turned on. R_3 will provide hysteresis if required.

b) Non-volatile Low voltage detector

In this application the high trip voltage V_T2 is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing

Figure 7. **Low voltage detector and memory**



switch S_1 the operating point changes to B and will remain at B until the supply voltage drops below V_T1 when the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V_T1 (even to zero volts) and then raised back to V_{NOM}.

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RS data

Switching regulator 78S40

Stock number 308-095

The RS 78S40 is a Monolithic Switching Regulator ic consisting of all the active building blocks necessary for switching regulator systems. The device can be used for step down, step up or inverting regulators as well as for series pass regulators. It features wide supply voltage range, low standby power dissipation, high efficiency and low drift. It is useful for any stand-alone, low part-count switching system and works extremely well in battery operated systems.

Absolute maximum ratings

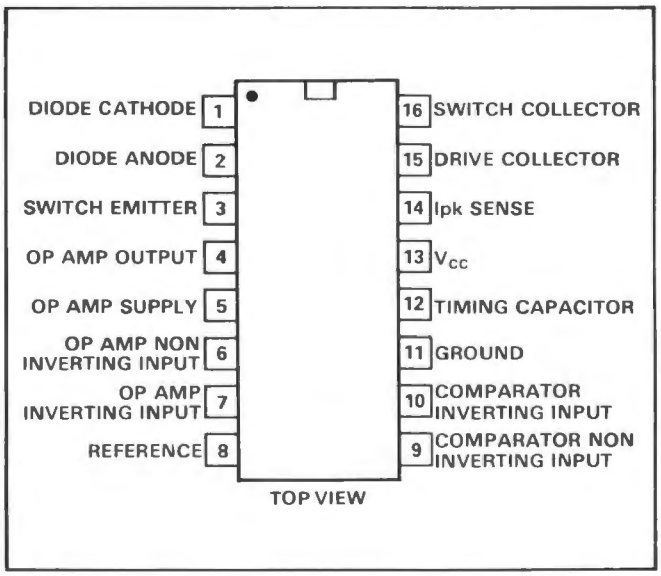
Input voltage from V+ to V–	40V
Input voltage from V+ op amp to V–	40V
Common mode input range (error amplifier and op amp)	–0.3 to V+
Differential input voltage (Note 1)	±30V
Output short circuit duration (op amp)	continuous
Current from V_{REF}	10mA
Voltage from switch collectors to GND	40V
Voltage from switch emitters to GND	40V
Voltage from switch collectors to emitter	40V
Voltage from power diode to GND	40V
Reverse power diode voltage	40V
Current through power switch	1.5A
Current through power diode	1.5a
Internal power dissipation (Note 2)	1500mW
Storage temperature range	–65°C to +150°C
Operating temperature range	0°C to +70°C
Lead temperature (soldering, 10 s)	+260°C

Notes:

1. For supply voltages less than 30V, the absolute maximum voltage is equal to the supply voltage.
2. Rating applies to +25°C. Above +25°C ambient, derate at 14mW/°C.

Features

- Step-down, step-up or inverting switching regulator
- Output adjustable from 1.3 to 40V
- Peak currents to 1.5A without external transistors
- Low standby current drain
- 80dB line and load regulation
- High gain, high current, independent op-amp
- Pulse width modulation with no double pulsing



Electrical characteristics V_{IN} = 5.0V, $V_{Op\ Amp}$ = 5.0V, T_A = +25°C unless otherwise specified.

Characteristics	Conditions	Min	Typ	Max	Units
General					
Supply voltage		2.5		40	V
Supply current (op amp disconnected)	V_{IN} = 5.0V V_{IN} = 40V		1.8 2.3	3.5 5.0	mA mA
Supply current op amp	V_{IN} = 5.0V V_{IN} = 40V			4.0 5.5	mA mA
Reference section					
Reference voltage	I_{REF} = 1.0mA (0<T_A<70°C)	1.180	1.245	1.310	V
Reference voltage temperature coefficient	I_{REF} = 1.0mA		100		ppm/°C
Reference voltage line regulation	V_{IN} = 3.0V to V_{IN} = 40V, I_{REF} = 1.0mA		0.04	0.2	mV/V
Reference voltage load regulation	I_{REF} = 1.0mA to I_{REF} = 10mA		0.2	0.5	mV/mA
Oscillator section					
Charging current	V_{IN} = 5.0V	20		50	μA
Charging current	V_{IN} = 40V	20		70	μA
Discharge current	V_{IN} = 5.0V	150		250	μA
Discharge current	V_{IN} = 40V	150		350	μA
Oscillator voltage swing t_{on}/t_{off}			0.5 6.0		V μs/μs
Current limit section					
Current limit sense voltage		250		350	mV
Output switch section					
Output saturation voltage Q_2	I_{SW} = 1.0A (Darlington configuration)		1.1	1.3	V
Output saturation voltage Q_1	I_{SW} = 1.0A (Q_1 only)		0.45	0.7	V
Output transistor h_{FE}	I_C = 1.0A, V_{CE} = 5.0V		70		
Output leakage current	V_{OUT} = 40V		10		nA
Power diode					
Forward voltage drop	I_D = 1.0A		1.25	1.5	V
Diode leakage current	V_D = 40V		10		nA
Comparator					
Input offset voltage	V_{CM} = V_{REF}		1.5	15	mV
Input bias current	V_{CM} = V_{REF}		35	200	nA
Input offset current	V_{CM} = V_{REF}		5.0	75	nA
Common mode voltage range		0		V^+ –2	V
Power supply rejection ratio	V_{IN} = 3.0V to 40V	70	96		dB
Output operational amplifier					
Input offset voltage	V_{CM} = 2.5V		4.0	15	mV
Input bias current	V_{CM} = 2.5V		30	200	nA
Input offset current	V_{CM} = 2.5V		5.0	75	nA
Voltage gain +	R_L = 2.0k to GND; V_O = 1.0 to 2.5V	25k	250k		V/V
Voltage gain –	R_L = 2.0k to V^+ op amp; V_O = 1.0 to 2.5V	25k	250k		V/V
Common mode voltage range		0		V^+ –2	V
Common mode rejection ratio	V_{CM} = 0 to 3.0V	76	100		dB
Power supply rejection ratio	V^+ op amp = 3.0 to 40V	76	100		dB
Output source current		75	150		mA
Output sink current		10	35		mA
Slew rate			0.6		V/μs
Output voltage LOW	I_L = –5.0mA			1.0	V
Output voltage HIGH	I_L = 50mA	V^+ op amp –3.0V			V

Figure 1 **C_T as a function of t_{off}**

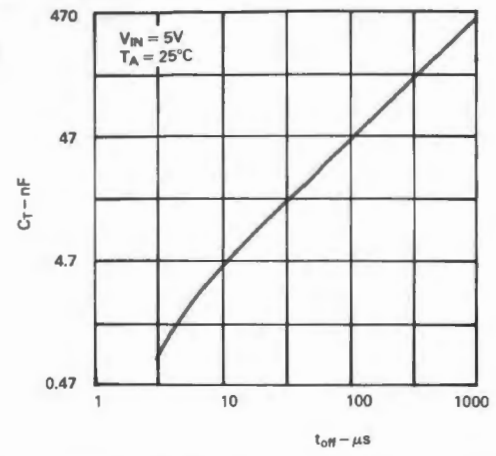


Figure 2 **V_{REF} as a function of T_J**

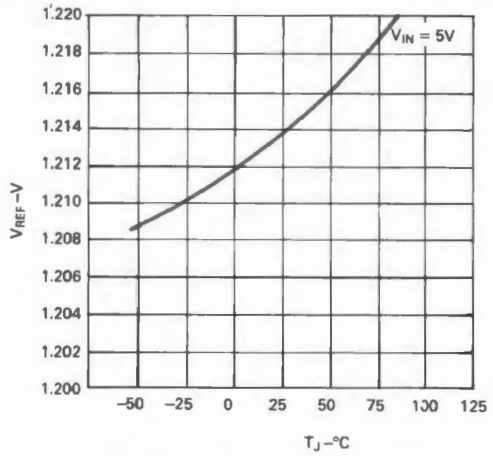


Figure 3 **$I_{discharge}$ as a function of V_{IN}**

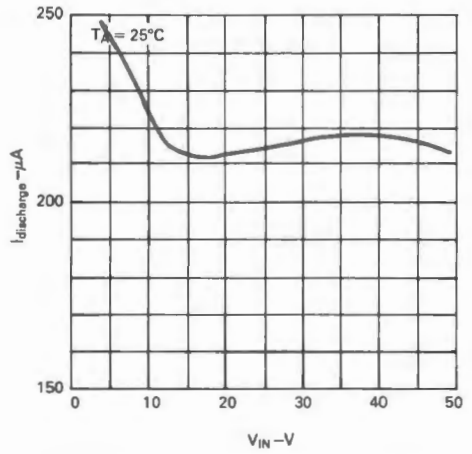
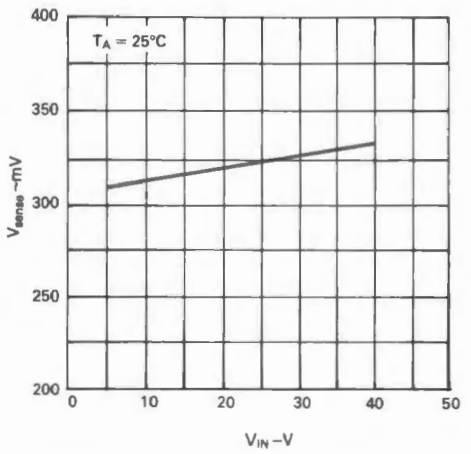


Figure 4 **V_{Sense} as a function of V_{IN}**



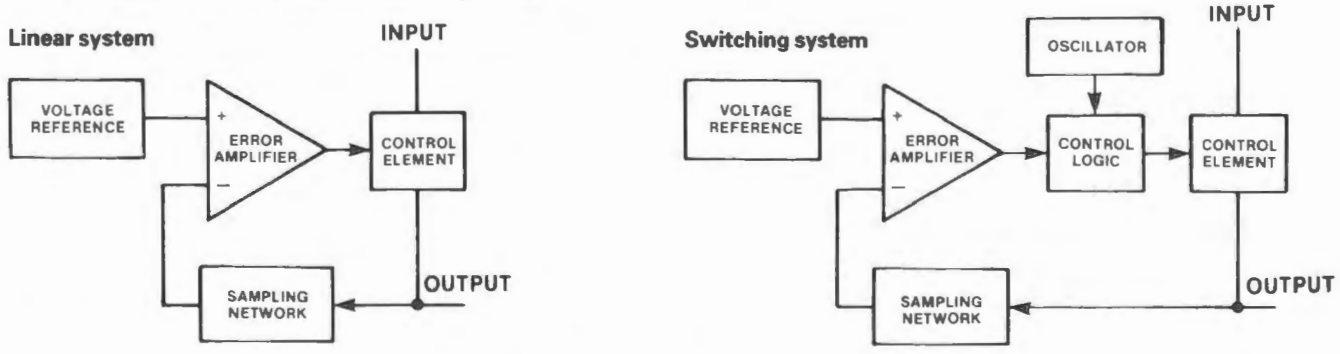
Principle of operation

A DC power supply is usually regulated by some type of feedback circuit that senses any change in the DC output and develops a control signal to compensate for this change. This feedback maintains an essentially constant output.

In a monolithic regulator, the output voltage is sampled and a high-gain differential amplifier compares a portion of this voltage with a reference voltage. The output of the amplifier is then used to modulate the control element, a transistor, by varying its operating point within the linear region or between the two operating extremes, cut-off and saturation. When the pass transistor is operated at a point between cut-off and saturation, the regulator circuit is referred to as a *linear* voltage regulator. When the pass transistor is operated only at cut-off or at saturation, the circuit is referred to as a *switching* regulator.

The advantage of the switching regulator over the more conventional linear regulator is greater efficiency, since cut-off and saturation modes are the two most efficient modes of operation. In the cut-off mode, there is a large voltage across the transistor but little current through it; in the saturation mode, the transistor has little voltage across it but carries a large amount of current. In either case, little power is wasted, most of the input power is transferred to the output, and efficiency is high. Regulation is achieved by varying the duty cycle that controls the average current transferred to the load. As long as this average current is equal to the current required by the load, regulation is maintained.

Figure 5 **Regulator system block diagrams**



Architecture

Each of the fundamental operating modes is built from the same set of function blocks (Figure 6). Additional functions are required for control and protection, but again, these functional blocks are common to each of the operational modes. The different modes are obtained by proper arrangement of these basic blocks.

For maximum design flexibility and minimum external part count, the RS78S40 was designed to include all of the fundamental building blocks in an uncommitted arrangement. This provides for a simple, cost-effective design of any switching regulator mode.

The functional blocks of the regulator, illustrated in Figure 6, are:

- Current-controlled oscillator
- Temperature-compensated current-limiting circuit
- Temperature-compensated voltage reference
- High-gain differential comparator
- Power switching circuit
- High-gain amplifier

The current-controlled oscillator generates the gating signals used to control the on/off condition of the transistor power switch. The oscillator frequency is set by a single external capacitor and may be varied over a range of 100Hz to 100kHz. Most applications require an oscillator frequency from 200 to 30kHz. The oscillator duty cycle (t_{on}/t_{off}) is internally fixed at 6:1, but may be modified by the current-limiting circuit.

The temperature-compensated, current-limiting circuitry senses the switching transistor current across an external resistor and may modify the oscillator on-time, which in turn limits the peak current. This provides protection for the switching transistor and power diode. The nominal activation voltage is 300mV, and the peak current can be programmed by a single resistor R_{SC}.

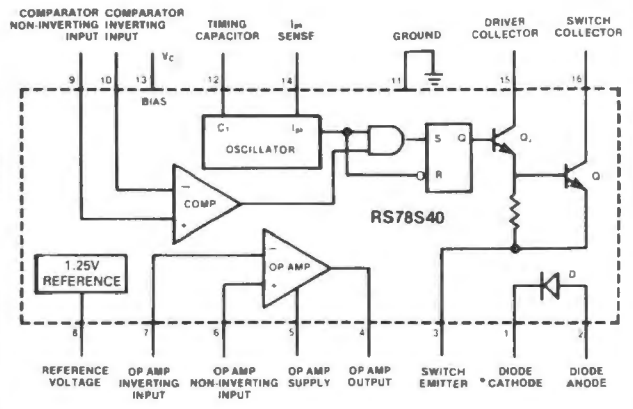
A 1.25V temperature-compensated, band-gap voltage source provides a stable reference to which the sampled portion of the output is compared. The reference is capable of providing up to 10mA of current without an external pass transistor.

A high-gain differential comparator with a common mode input range extending from ground to 1.5V less than V_{CC} is used to inhibit the basic gating signal generated by the oscillator turning on the transistor switch when the output voltage is too high.

The transistor switch, in a Darlington configuration with the collectors and emitter brought out externally for maximum design flexibility, is capable of handling up to 1.5A peak current up to 40V collector-emitter voltage, and switching times that are normally 300-500ns.

Although not required by the basic operating modes, an independent operational amplifier has been included to increase flexibility. The characteristics of this amplifier are similar to the 741, except that a power output stage has been provided, capable of sourcing up to 150mA and sinking 35mA. The input has also been modified to include ground as part of the common-mode range. This amplifier may be connected to provide series pass regulation or a second output voltage, or configured to provide special functions for some of the more advanced applications.

Figure 6



Operation of the comparator, operational amplifier, and reference regulator are essentially identical to individual integrated circuits performing these same functions. However, some precautions should be noted in the case of the on-chip diode. Because of the fact that the integrated circuit substrate is normally at ground potential, the cathode of diode must not be operated at negative voltage; this precludes its use in step down and inverting configurations. The internal construction of the diode also results in a flow of current from the anode to the *substrate* amounting to approximately 10% of the normal anode/cathode current. Because of the usual high voltage between anode and ground, dissipation limits the diode's usefulness in step-up applications. The diode is useful as reverse protection for the switch transistor and is shown connected in manner in the accompanying drawings.

Where applications specify an external Schottky diode (262-466) the use of a silicon fast recovery diode may be considered as a more cost effective alternative. In some applications conventional silicon diodes such as 1N4001 or 1N5401 etc. may be substituted although some loss of efficiency will be encountered.

The switching regulator can be operated over a wide range of power conditions, from battery power to high-voltage, high-current supplies. Low voltage operation down to 2.4V and low standby current, less than 2.5mA at 5V, make it ideal for battery-powered systems.

Besides high efficiency operation, another advantage of the switching regulator is increased application flexibility offered by output voltages that are less than, greater than, or of opposite polarity to the input voltage.

Figure 7 lists the design formulae used to derive the values of the external components required for specific outputs in the three modes of operation. Design examples for step down, step up and inversion operation are given on pages 5-8.

Figure 7 **RS78S40 Design formulae**

Characteristic	Step down	Step up	Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} - V_{OUT}}$	$\frac{V_{OUT} + V_D - V_{IN}}{V_{IN} - V_{SAT}}$	$\frac{\lvert V_{OUT}\rvert + V_D}{V_{IN} - V_{SAT}}$
$(t_{on} + t_{off})_{(max)}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$	$4 \times 10^{-5}\, t_{on}$
I_{pk}	$2\, I_{OUT\,(max)}$	$2\, I_{OUT\,(max)} \times \frac{t_{on} + t_{off}}{t_{off}}$	$2\, I_{OUT\,(max)} \times \frac{t_{on} + t_{off}}{t_{off}}$
$L_{(min)}$	$\left(\frac{V_{IN} - V_{SAT} - V_{OUT}}{I_{pk}}\right) t_{on\,(max)}$	$\left(\frac{V_{IN} - V_{SAT}}{I_{pk}}\right) t_{on\,(max)}$	$\left(\frac{V_{IN} - V_{SAT}}{I_{pk}}\right) t_{on\,(max)}$
R_{SC}	$0.33/I_{pk}$	$0.33/I_{pk}$	$0.33/I_{pk}$
C_O	$\frac{I_{pk}\,(t_{on} + t_{off})}{8\, V_{RIPPLE}}$	$\approx \frac{I_{out}}{V_{RIPPLE}} \times t_{on}$	$\approx \frac{I_{out}}{V_{RIPPLE}} \times t_{on}$

Note:
V_{SAT} – Saturation voltage of the switching element V_D – Forward voltage of the flyback diode.

Design example – Step down regulator

Given the conditions: V_{in} = 25V, V_{out} = 5V, I_{out} (max) = .5A, V_{ripple} = 1%, we can design a step-down switching regulator as depicted schematically in Figure 8.

First, determine the ratio of switch conduction verses diode conduction times:

$$\left(\frac{t_{on}}{t_{off}}\right):$$

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_D}{V_{in} - V_{sat} - V_{out}} \qquad \text{(from table 1)}$$

$$= \frac{5 + 0.7}{25 - 1.1 - 5} \qquad = \frac{5.7}{18.9} = .30$$

Now, we add the requirement that in the continuous conduction mode (coil current never goes to zero) we want the minimum frequency to be above the audio range:

$$f_{min} \geq 5\text{kHz}$$

therefore, $$\frac{1}{t_{on} + t_{off}} \geq 5000\ \text{sec}^{-1}$$

$$\text{or } (t_{on} + t_{off})_{max} = 200\ \mu\text{sec}$$

Algebraic manipulation of the previously obtained value of t_{on}/t_{off} will give us t_{off} as a function of $(t_{off} + t_{on})$ and (t_{on}/t_{off}) which have been determined.

$$\frac{t_{on}}{t_{off}} + 1 = \frac{t_{on} + t_{off}}{t_{off}}$$

$$t_{off} = \frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1} = \frac{200}{1.30} \text{ microseconds}$$

$$t_{off} = 154 \text{ microseconds}$$

$$t_{on}\ max = 46 \text{ microseconds}$$

Note that the variable of interest is t_{on}, the switch conduction time, which is the *only* variable under control of the RS78S40.

The *maximum* value of t_{on} is important because it allows us to set the current limit to the appropriate level and to select inductors with adequate peak current ratings.

The required timing capacitor value may now be determined by using the minimum oscillator charging current and the typical value for oscillator voltage swing:

$$C_T = (I_{ch})\frac{t}{v} = \left(\frac{20 \times 10^{-6}}{.5}\right) t_{on} = (4 \times 10^{-5})\, t_{on}$$

$$C_T = (4 \times 10^{-5})\,(46 \times 10^{-6})$$

$$C_T = 1800\,\text{pF}$$

Of course, the typical charging current is higher than 20 microamps, so the typical operating frequency will be greater than 5kHz.

The *minimum* inductance value may now be obtained by reference to the maximum on time and the desired value of maximum load current.

$$I_{peak} = 2\, I_{out\,(max)}$$
$$= (2)\,(.5A)$$
$$= 1.0A$$

$$L_{(min)} = (V_{in} - V_{sat} - V_{out})\frac{t_{on}\,(max)}{I_{peak}}$$

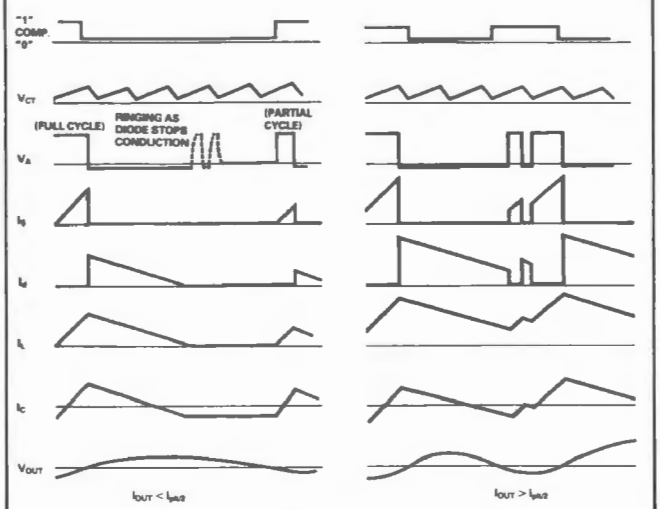
$$L_{(min)} = (18.9)\,\frac{46 \times 10^{-6}}{1.0}$$

$$L_{(min)} = 869\ \mu\text{H}$$

This minimum value of inductance was determined by assuming the onset of continuous conduction operation at the maximum value of load current for a minimum charge current oscillator. As mentioned previously, actual operating frequencies will

typically be higher, resulting in current waveforms more like Figure 7c at full load. Larger than minimum values of inductance reduce the value of load current at which continuous conduction occurs as well as effect a reduction in the peak to average switch current.

Figure 7 **Step-down regulator waveforms**



For this design, then, let's use an inductance value well above the minimum; say 1500 micro Henries.

The reduced peak to average values of switch current allow us to set the current limit threshold at two times the maximum load current or 1.0A

$$R_{sc} = \frac{.33V}{1.0A} = .33\Omega$$

The inductor must be specified to allow non-saturated operation up to this peak current of 1.0 Amperes.

The actual output voltage waveform in Figures 7a, b, c is extremely complex. An RMS value would be very difficult to obtain analytically because of the presence of partial cycles. An *approximation* of the peak-to-peak ripple can be obtained from the formula:

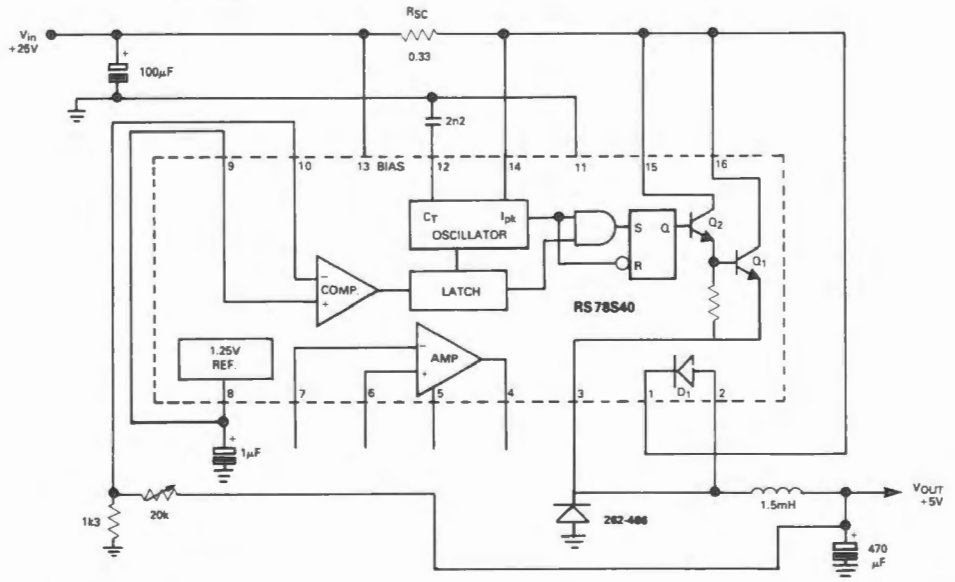
$$V_{p\text{-}p} = (I_{peak}) \frac{(t_{on} + t_{off})}{8\, C_O}$$

For 1% ripple (peak to peak) on the 5 volt output:

$$C_O = \frac{(1.0)\,(200\ 10^{-6})}{(8)\,(.05)}$$

$$C_O = 500\mu F$$

Figure 8 **Step-down voltage regulator**



Design example – step-up regulator

$V_{in} = 12V$, $V_{out} = 28V$, $I_{out} = 0.1A$

$V_{ripple} = 1\%$

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_d - V_{in}}{V_{in} - V_{sat}} = \frac{28 + 0.7 - 12}{12 - 0.5}$$

$$= \frac{15.3}{11.5} = 1.33$$

choose: $f_{min} = 10kHz$

$$(t_{on} + t_{off})_{(max)} = \frac{1}{f_{min}} = 100\ \mu sec$$

$$t_{off} = \frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1} = \frac{100}{2.33} = 43\ \mu sec_{(max)}$$

$$t_{on} = 1.33\, t_{off} = 57\ \mu sec_{(max)}$$

$$C_T = (40.10^{-6})\, t_{on} = 2283 pf.$$

$$I_{peak} = 2\, I_{out(max)} \frac{t_{on} + t_{off}}{t_{off}}$$

$$I_{peak} = (2)\,(0.1)\,\frac{(100)}{(93)} = 0.46A$$

$$L_{(min)} = \frac{V_{in} - V_{sat}}{I_{peak}}\, t_{on(max)} = \frac{12 - 0.5}{0.27}\,(57 \times 10^{-6})$$

$$= 2.43 mH$$

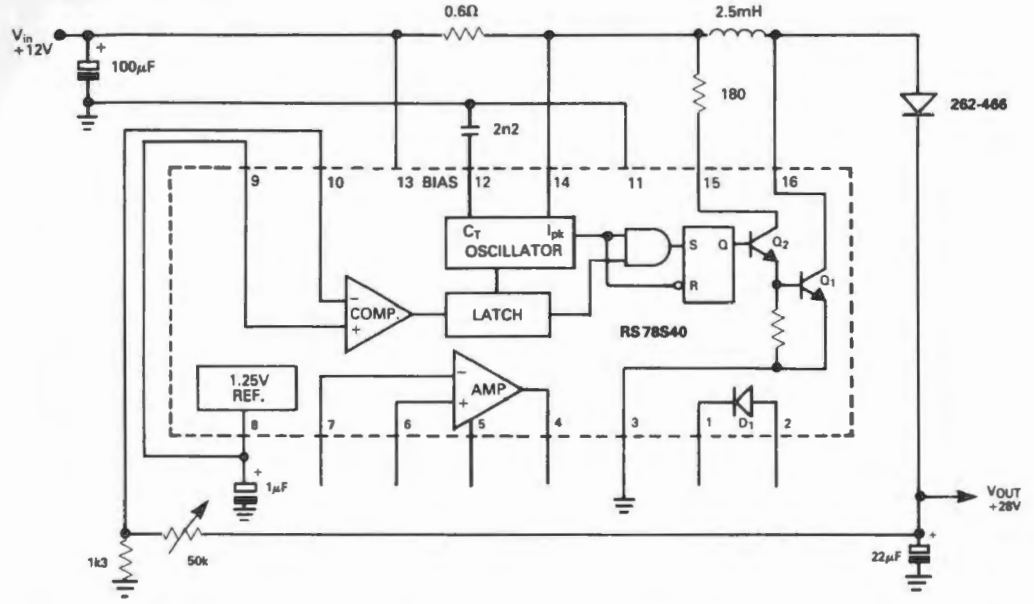
$$R_{SC} = \frac{0.33}{(1.2)\, I_{peak}} = \frac{0.33}{(1.2)\, I_{peak}} = 0.6 \text{ ohms}$$

$$C_O \approx \frac{I_{out}}{V_{ripple}} \bullet ton$$

$$= \frac{0.1}{0.28}\, 57.10^{-6}$$

$$= 20\ \mu F$$

Figure 9 **Step-up voltage regulator**



Design example – inverting regulator

A schematic of the basic inverting regulator is shown in Figure 10.

Conditions

$V_{IN} = 12V$ $I_{out\ (max)} = 500mA$

$V_{OUT} = -15V$ $V_{RIPPLE} \leqslant 1\%$ (peak to peak)

Calculations

An external PNP switching transistor is necessary for the inverting regulator configuration because of polarity limitations.

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_d}{V_{in} - V_{sat}} = \frac{15 + 0.7}{12 - 0.5} = 1.365$$

Let $f_{min} = 8kHz$

$$(t_{on} + t_{off})_{(max)} = \frac{1}{f_{min}} = 125\,\mu s$$

$$t_{on} = \frac{t_{on} + t_{off}}{\frac{t_{off}}{t_{on}} + 1} = \frac{125}{1.365 + 1} = \frac{125}{2.365} = 55.4\mu s$$

$$\therefore t_{off} = 69.6\mu s$$

$$C_T = (4 \times 10^{-5})\, t_{on} = 2784pF$$

make $C_T = 2700pF$ (2n7).

$$I_{peak} = \left(2 \times I_{out(max)}\right) \frac{t_{on} + t_{off}}{t_{off}}$$

$$= (2 \times 0.5)\, \frac{125}{69.6} = 1.796A$$

$$L_{(min)} = \frac{V_{in} - V_{sat}}{I_{peak}}\, t_{on(max)} = \frac{12 - 0.5}{1.796)}\, (55.4 \times 10^{-6})$$

$$= 355\mu H$$

$$R_{SC} = \frac{0.33}{(1.2)\, I_{peak}} = \frac{0.33}{(1.2 \times 1.796} = 0.15 \text{ ohms}$$

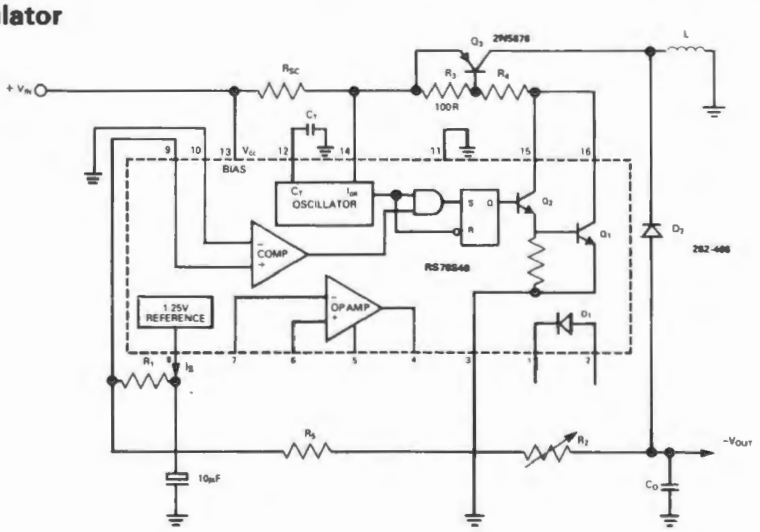
$$C_O = \frac{I_{out}}{V_{ripple}} \times ton$$

$$= \frac{0.5}{0.15}\, 55.4 \times 10^{-6}$$

$$= 184\mu F$$

Make $C_O = 220\mu F$

Figure 10 **Inverting regulator**



The sampling network, R_1 and R_2, can easily be calculated. Assuming the sampling network current I_S is 1mA:

$$R_1 = \frac{V_{REF}}{I_S} \approx 1.3k\Omega$$

$$R_2 = \frac{-V_{OUT}}{I_S} = 15k\Omega$$

Set R_1 = 1.3kΩ and use a 20kΩ pot for R_2 so that output voltage can be adjusted. R_5 should be ≈ 5kΩ to protect V_{REF}, limiting I_S to ≈ 2.6mA.

This application requires an external diode and transistor since the substrate of the regulator is referenced to ground and a negative voltage is present on the output. The external diode and transistor prevent the substrate diodes from a forward-biased condition.

R_3 is provided for quick turn-off of the external transistor and is usually in the range of 100Ω to 300Ω. R_4 can be calculated as follows:

$$R_4 = \frac{V_{IN} - V_{SAT} - V_T - V_{BE}}{I_{pk}/ß}$$

where

V_T = threshold voltage = 300mV

V_{BE} = base emitter drop across the external transistor

ß = ¼ h_{FE} of the external transistor

If the 2N5876 is used, the value for R_4 is:

$$R_4 = \frac{12 - 0.4 - 0.3 - 2.5}{(2.34/10)} \approx 39\Omega$$

Again, capacitors can be placed at the input to reduce transients.

Pulse width modulation

An alternative to the previously described mode of operation is the configuration shown in Figure 11. In this circuit the RS78S40 operates as a pulse-width modulator in which the duty cycle of the constant frequency switching waveform is varied to control the output voltage. The oscillator ramp voltage appearing at pin 12 (C_T) is fed to the non-inverting comparator input. The output voltage is attenuated and subtracted from the reference voltage in the on-chip operational amplifier and the resulting error signal is fed to the inverting input of the comparator.

The intersection of the ramp voltage on the non-inverting input of the comparator with the error voltage on the inverting input, modulates the turn-on point of the output switch transistor during the positive-going ramp of the oscillator. Turn-off, as always, takes place at the onset of the negative-going oscillator ramp.

Because of the fast response of the pulse width modulator to variations in output voltage, increased attention must be paid to loop stability.

The pulse-width modulator, shown in Figure 11 uses a simple, dominant pole technique to provide stable operation with relatively slow response time.

Figure 12 **Pulse width modulator waveforms**

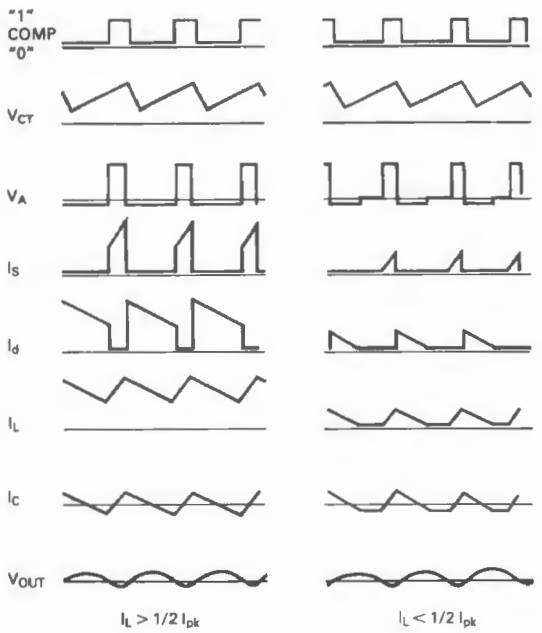
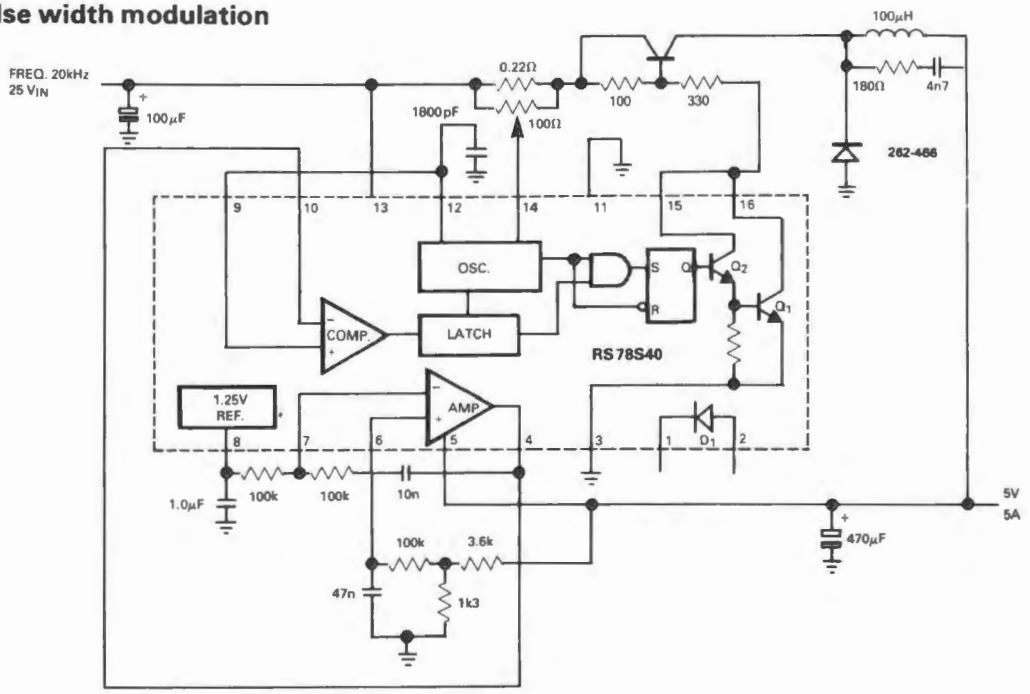


Figure 11 **Pulse width modulation**

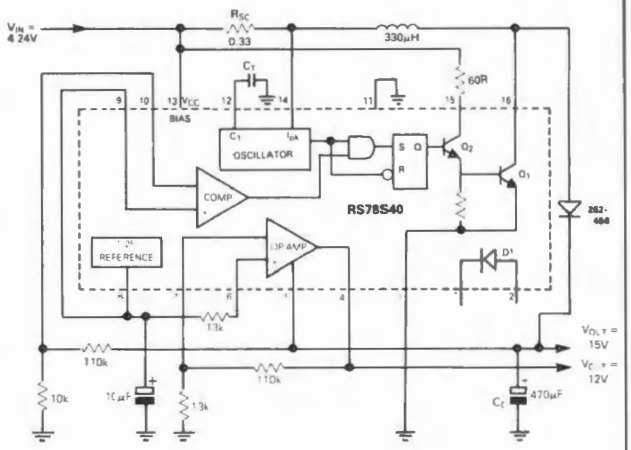


Additional circuits

Constant output voltage regulator

A useful variation is the use of the universal regulator to provide a constant output for voltage inputs that are both higher and lower than the output, see Figure 13. In this case, 12V at 100mA is provided at the output for input voltages over a 4V to 24V range. This is achieved by using a step-up mode similar to the version shown in Figure 9 to provide a 15V output and then using the internal op amp as a series-pass regulator to reduce the output to 12V. When the input voltage exceeds 16V, the step-up regulator circuit follows the input at approximately the input voltage minus 1V, but the series-pass output remains constant at 12V. The op amp exhibits excellent noise rejection, so output ripple is virtually non-existent at the 12V output. Regulator efficiency is about 50% for the upper and lower limits of the input range (4V and 24V) and increases to a maximum of about 75% for intermediate voltages.

Figure 13 **Constant output voltage regulator over 4-24V input range**

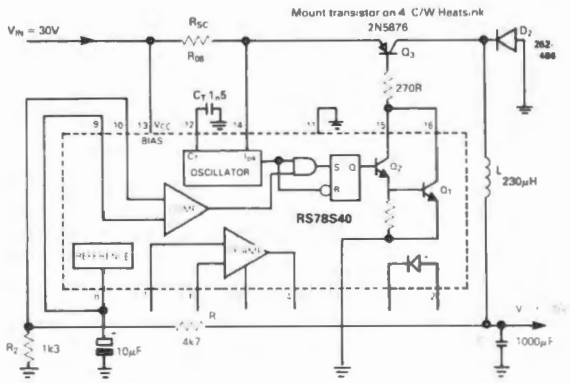


High current step-down regulator

Another variation involves the addition of an external pnp transistor and an external catch diode to the step-down regulator, see Figure 14. The transistor (Q_3) increases output current capability by a factor of 4 and also improves switching efficiency because the switching voltage drops from 1.6V to 0.4V. The npn Darlington pair switch is connected to provide the base drive for Q_3, with a 270Ω resistor limiting the base drive to 100mA. A peak input current of 4A (plus the 80mA typ base drive) with an input voltage of 30V provides a 5V, 2A output.

In this case the off-time/on-time ratio is about 4.6:1 with the off-time at 160µs and on-time at 38µs. Output capacitance of 1000µF keeps output ripple to within 100mV. The external diode (D_2) is required to handle the 4A switching current.

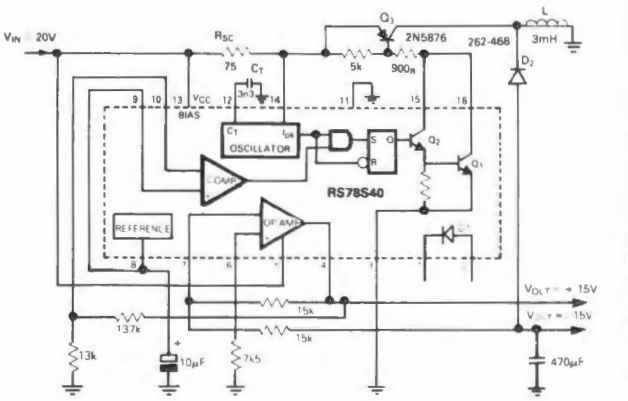
Figure 14 **A 5V 2A step-down regulator**



Dual tracking regulator

Figure 15 illustrates a dual-tracking regulator that provides both +15V and −15V outputs from a single +20V input. The negative output voltage is generated with an inverter circuit similar to the circuit of Figure 10, but the op amp is connected in a unity gain configuration with its output divided down and compared to the 1.25V reference voltage. As shown, this regulator provides ±15V at 100mA with 80% efficiency – 75% positive voltage, 85% negative voltage – with output ripple limited to 30mV.

Figure 15 **± 15V Dual tracking regular**



RS data

Inductor design

The inductors required for the switching regulator circuits can be wound on the RM series of ferrite cores (see current catalogue).

The procedure for designing the inductor is as follows:

1. Calculate the value of inductance required from the formula given for the type of circuit being designed.
2. Calculate LI^2_{pk} in mJ.
3. Consult the catalogue to obtain a core which has an LI^2_{sat} value equal to or greater than LI^2_{pk}

   $LI^2_{sat} \geq LI^2_{pk}$

To keep DC losses to a minimum, employ a core with a large inductance factor, if possible, to reduce the number of turns required for the inductance.

4. Calculate the number of turns required to obtain the required inductance.

$$\text{No. of turns} = \sqrt{\frac{L}{A_L}}$$

Where L is in nH

A_L is the inductance factor

5. Select the largest diameter wire governed by the maximum number of turns accommodated on the bobbin size employed.

As an example of the above procedure, consider the step-up regulator circuit shown in Figure 9.

$L = 2.5\text{mH}\ I_{pk} = 0.46\text{A}$

$\therefore LI^2_{pk} = 0.529\text{mJ}$

From the catalogue the smallest core size which can be employed is the RM10.

(LI^2_{sat} = 1.731 or 1.082mJ. To reduce DC losses, select the RM10 core with the highest inductance factor ie. 400 (nH/turn^2).

$$\text{Turns required} = \sqrt{\frac{L}{A_L}}$$

$$\sqrt{\frac{2.5 \times 10^6}{400}} = 79.06 \text{ turns}$$

Use 79 turns.

The maximum wire diameter which the RM10 core can accommodate for 79 turns is 0.2mm.

Hence wind 79 turns of 0.2mm dia. insulated copper wire onto the bobbin of an RM10 core with an inductance factor of 400nH/turns^2.

Electro-magnetic interference (EMI)

Due to the wiring inductance in a circuit, rapid changes in current generate voltage transients. These voltage spikes are proportional to both the wiring inductance and the rate at which the current changes:

$$V = L\frac{di}{dt}$$

The energy of the voltage spike is proportional to the wiring inductance and the square of the current:

$$E = \frac{1}{2}LI^2$$

Interference and voltage spiking are easier to filter if the energy in the spikes is low and the components predominantly high frequency.

The following precautions will reduce EMI:

- Keep loop inductance to a minimum by utilising appropriate layout and interconnect geometry.
- Keep loop area as small as possible and lead lengths short and, in step-down mode, return the input capacitor directly to the diode to reduce EMI and ground-loop noise.

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RS data

Doppler module

Stock number 308-017

The RS 8960 is an X-band Doppler radar module intended for indoor applications and designed specifically for detecting movement of a remote target by detecting Doppler-shift in reflected microwave radiation.

The module contains a Gunn device (oscillator), which produces the energy to be radiated, and a mixer diode which combines the reflected microwaves with a sample of the oscillator signal.

The unit is self contained requiring only a power supply and amplifier to provide the Doppler output.

Applications include intruder alarms, speed measurement, vibration measurement, proximity switch for automatic operation of doors etc.

Table 1. Operating conditions, ratings, and characteristics

Operating Conditions:					
Supply voltage to Gunn device	+7.0 ±0.2				
Supply current to Gunn device (see note 6)	130mA typ.				
D.C. mixer bias (into O/P terminal w.r.t. 0V)	30μA to 35μA (The mixer diode will be damaged by forward current in excess of 10mA.)				
O/P load	10k Ω (see text)				
Ratings (Absolute maximum system):					
Temperature, storage	−10°C to +70°C				
operating	0°C to +40°C (−5°C to +40°C over which				
Supply voltage max. d.c.	+7.5V				characteristics apply)
Supply voltage transients (1ms max.)	9.0V				
Characteristics at 25°C:					
Centre frequency	10.69GHz				
	Min.	**Typ.**	**Max.**	**Units**	**See notes**
Output voltage for input power 100dB down on output power (at 18dB min.)					4,5
(S + N)/N ratio	20	40		μV	Fig. 7
Power output at 7.0V		10		mW	
Frequency fixed	10.675	10.687	10.700	GHz	
Frequency temperature coefficient		−0.25	−0.4	MHz/degC	
Frequency pushing		4.0		MHz/V	
Out of band radiation		−40		dBm	
Gunn device current		130	165	mA	6
Antenna gain		5		dB	
Material	Mazak (Passivated)				

Operating notes

1 The Gunn device will be damaged if the supply is reversed.

2 The mixer diode has a low junction capacitance and may be damaged by voltage transients of very short duration. It is therefore recommended that soldering appliances should be isolated from the supply and handling precautions applicable to C-MOS devices observed.
The module is despatched with back-to-back protection diodes and a 10nF capacitor connected between the mixer 'O/P' and 0V terminals, and these should be left connected.

3 The operating conditions listed in table 1 apply when operated into the antenna supplied with the RS 8960 module. See Fig. 2 for antenna polar diagram.

4 A return signal 100dB down on radiated power will be achieved from a man-target of radar cross-section $1m^2$ at a range of 15m, when operating with the antenna supplied (antenna gain typically 5dB).
Extended range can be obtained for a reduced (S + N)/N ratio.
For example, 110dB path loss is obtained from a man-target at 25m and the (S + N)/N ratio is reduced to 15dB with output voltage 16μV min. (See text.)

5 Noise measured in a 1Hz to 1kHz bandwidth.

6 The Gunn device has a voltage-current characteristic depicted in Fig. 3. Power supplies should have low source impedance and be capable of supplying up to 250mA at approximately 3V, during the voltage rise from switch on.

Figure 1 **Physical dimensions**

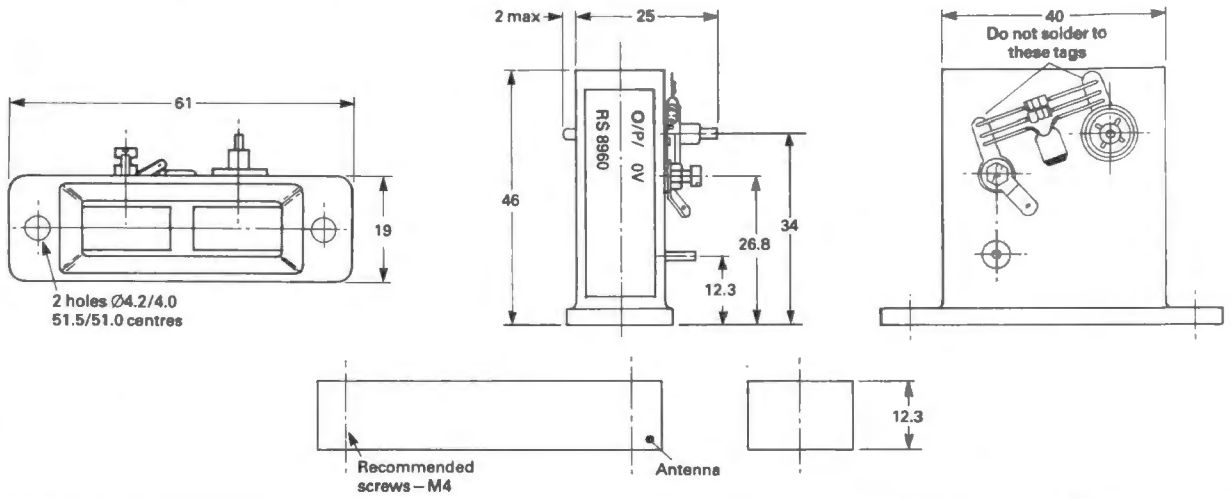
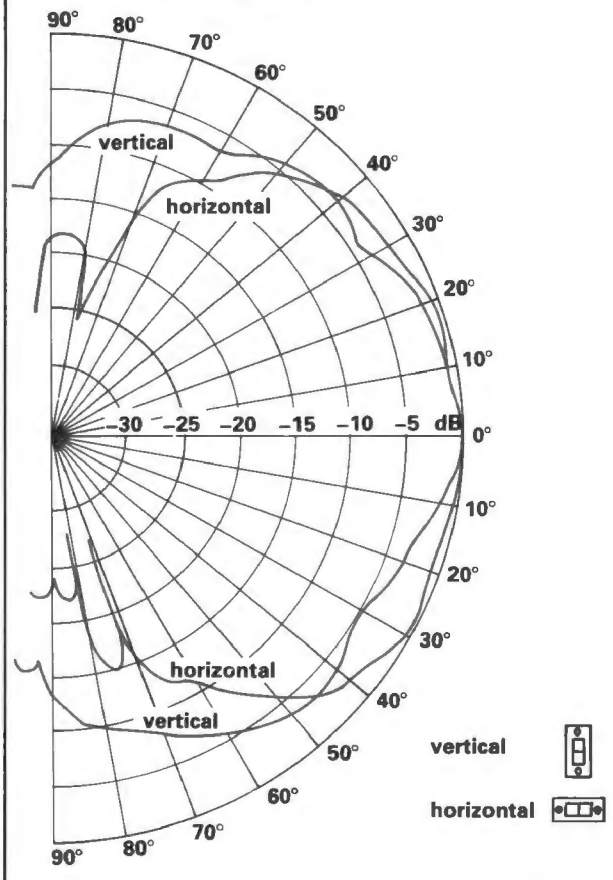


Figure 2 **Polar diagram of RS 8960 with 5dB antenna**



Antenna pattern

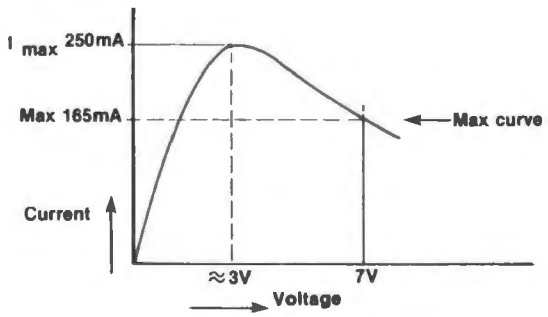
The antenna supplied with the module has the free space radiation pattern shown in Fig. 2.

This pattern may be distorted in practice, by reflections from surrounding surfaces, and care should be taken in the location of the module to avoid close proximity with reflecting surfaces.

D.C. mixer bias

This current should be $\simeq 35\mu A$ with the Gunn device disconnected, and approximately $42\mu A$ with the Gunn device operational and the composite unit operating into free space.

Figure 3 **Characteristic of Gunn device**



Principle of doppler detection

The diagram in Fig. 4 illustrates the basic operation of a microwave doppler detector. The Gunn device generates microwave power in the waveguide and feeds horn H_1 which radiates the resultant electromagnetic field in a beam. (See Fig. 2 for polar diagram.) On encountering a target X a proportion of the microwave power (W_1) is reflected and received by the horn H_2 and transferred via the waveguide to the mixer diode D_1.

Adding mixer r.f. bias to obtain a doppler output

To obtain a doppler signal from D_1, rather than just the detected W_1 signal, the diode must be supplied with some microwave power directly from the Gunn device.

A drilling between the connected waveguides allows local oscillator power (W_2) to be transferred from the Gunn device to the mixer diode. Diode D_1 receives the two signals W_1 and W_2 which are summed to produce an output voltage which is dependent on the relative phases and frequencies of W_1 and W_2. If the target X is stationary W_1 and W_2 are of the same frequency but may differ in phase hence the output voltage from D_1 will be d.c. If the target is moving then both phase and frequency of W_1 and W_2 will differ and the resultant output voltage will be alternating. It is this alternating voltage which is transferred to the amplifier A_1 via capacitor C_2.

Calculation of doppler frequency

The frequency of this alternating voltage is dependent on the velocity of the moving target. Assuming the target is distant from the doppler module then angle 0 is approximately zero.

For a target velocity 'v' the doppler frequency is given by the expression:

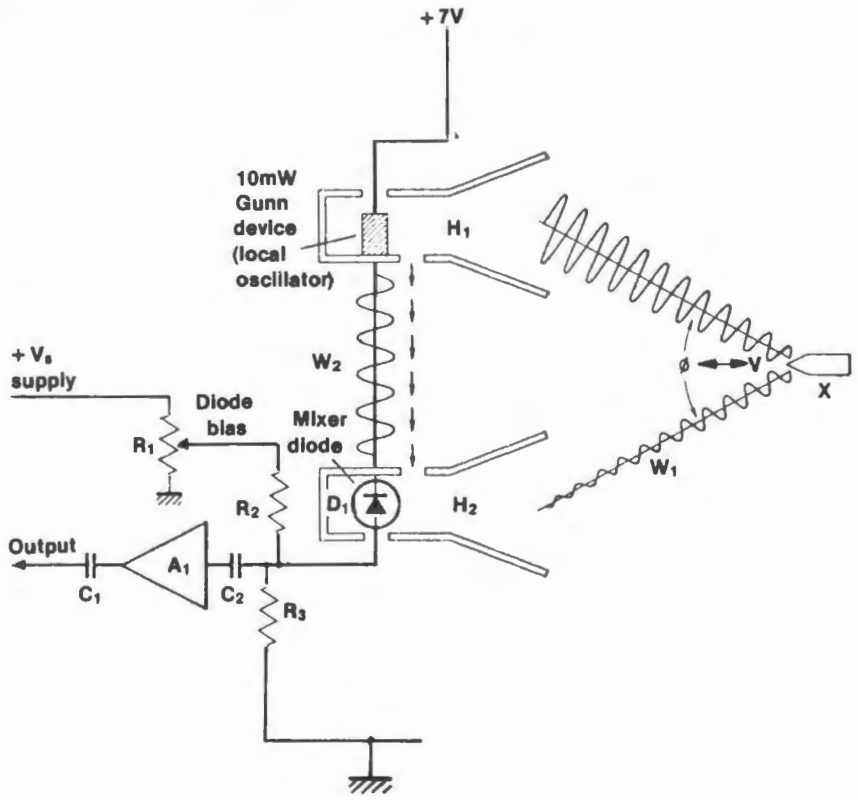
$$f = 2v/\lambda Hz$$

Since the propagation speed of electromagnetic waves is 3×10^8 metres per second, λ becomes $3 \times 10^8/F$, where F is the microwave frequency. Thus the doppler frequency f is given by

$$f = 2vF/(3 \times 10^8)\ Hz$$

With the RS 8960 module, frequency F = 10.69GHz, and a target speed of 1mph (0.45 metres per second) gives the doppler frequency f as 31.8Hz.

Figure 4 **Schematic representation of microwave doppler detector**



Range equation

The power received by the RS 8960 module in free space may be calculated from Eq. 1.

$$P_o + 2.G_{ant} + G_T - a_s = P_{in}. \quad . \quad . \quad . \quad (1)$$

Where P_o = radiated power (dBm)
G_{ant} = antenna gain (dB)
G_T = target gain (dB)
a_s = two-way free space path loss (dB)
P_{in} = received power (dBm)

For the RS 8960 standard antenna supplied, the gain is approximately 5.0dB. Equivalent target gain is plotted against radar cross-section in Fig. 5, and the two-way path loss is shown in Fig. 6.

The target gain G_T of an object is defined by:

$$G_T = 10 \log_{10} \left(\frac{4\pi\sigma}{\lambda_2}\right) dB, \quad . \quad . \quad . \quad . \quad (2)$$

where σ, the radar cross-section (m^2) is approximately frequency-independent provided that the target is large compared with the wavelength λ(m). Eq. 2 is plotted for X-band frequencies in Fig. 5, and it can be seen that the radar cross-section of a man target is taken as approximately $1m^2$, which corresponds with a target gain of 42dB. It has been found, however, that the actual radar cross-sections of persons vary between 0.1 and $2m^2$; from Fig 5, therefore, the equivalent X-band target gain can vary between 32 and 45dB.

The two-way free-space path loss is given by

$$a_s = 40 \log_{10} \left(\frac{4\pi D}{\lambda}\right) .dB, \quad . \quad . \quad . \quad . \quad (3)$$

where D is the range (m) and λ the wavelength (m). This equation is plotted for a free-space wavelength corresponding to a frequency of 10.7GHz in Fig. 6.

Example

Find the minimum output to be expected from a man-target at 10 feet (3.05 metres).

From Fig. 5, the target gain, G_T = 42dB
From Fig. 6, a_s = 120dB
Antenna gain G_{ant} = 5dB

Therefore

$$P_o - P_{in} = a_s - G_T - 2.G_{ant}$$
$$= 120 - 42 - 10$$
$$P_o - P_{in} = 68dB = \text{path loss}. \quad . \quad . \quad . \quad . \quad (4)$$

Figure 5 **Target gain versus target size**

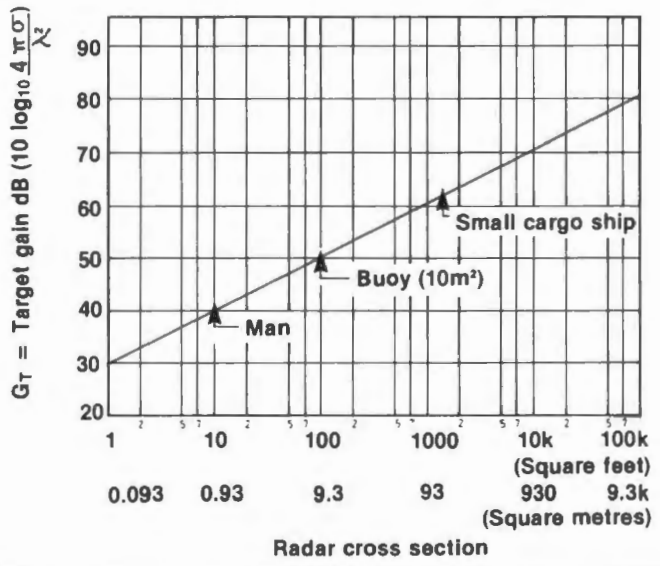
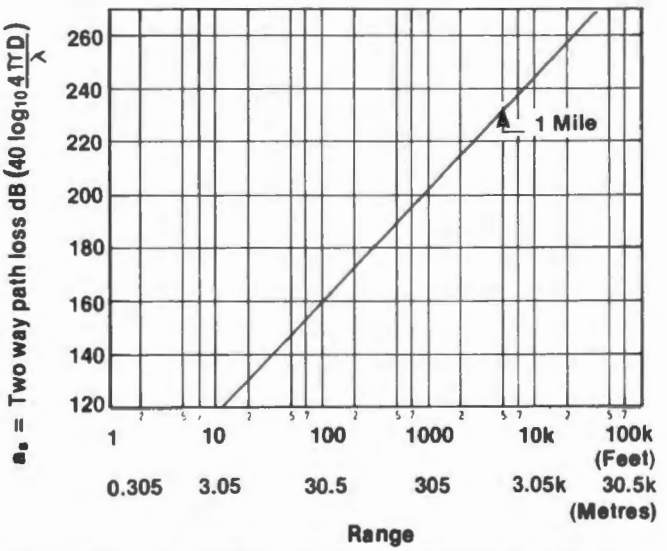


Figure 6 **Two-way path loss**



Now if 100dB path loss gives 20μV min. output signal (see Table 1), then 68dB path loss will give 20μV + 32dB = 20μV × 40 = 800μV min.

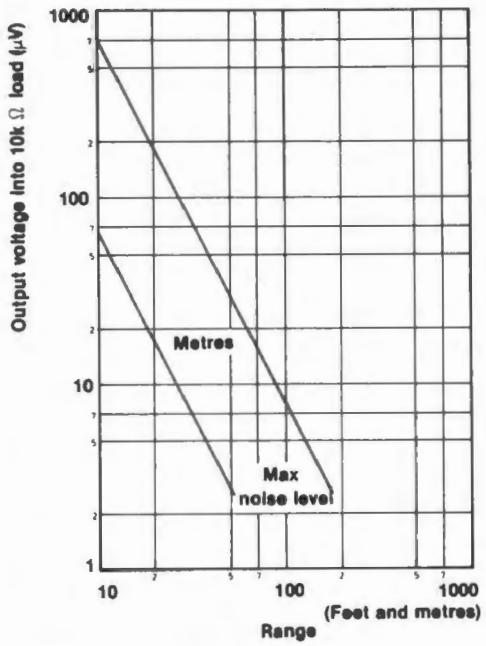
Fig. 7 shows the minimum output voltage versus range for a typical man-target. The most important parameter in a receiver system is the signal-to-noise ratio. In this example the signal-to-noise ratio may be derived as follows:

The date (Table 1) specifies a minimum S/N ratio of 18dB for input power 100dB down on output power. Thus for input power 68dB down on output power, the S/N ratio will be improved by (100−68)dB = 32dB. The S/N ratio for a man-target at 10 feet is then (18 + 32)dB = 50dB.

Care should be taken in the design of bias and amplifying circuitry to prevent degradation of this performance in the complete system.

Modulation or transients in the supply voltage to the Gunn device, will be converted to a.m. noise in the local oscillator coupled power, and may appear in the passband of the following amplifier. The amplifier should be designed with low noise characteristics.

Figure 7 **Min. output for man-target**



Mixer bias and following amplifier

The optimum signal-to-noise performance of the RS 8960, is obtained by operating the mixer diode under total bias of 42μA, which is the sum of d.c. applied bias (35μA), and the bias from the coupled local oscillator supply (7μA).

The correct value of L.O. (local oscillator) power is obtained when operating the antenna into free space. The effect on performance for increased levels of L.O. power is discussed later.

A circuit design shown in Fig. 8 will provide the optimum mixer d.c. bias; it has low noise characteristics, a suitable frequency response, adequate gain, and it is simple to construct. The circuit has an input impedence of approximately 600 Ω, which is a near-match to the diode impedance, and provides satisfactory signal-to-noise ratio. Because of the variation in diode impedance, the overall gain will vary over a range of RS 8960 modules, but may be preset by potentiometer R_3 which should be adjusted to set the amplifier output in routine setting up procedures.

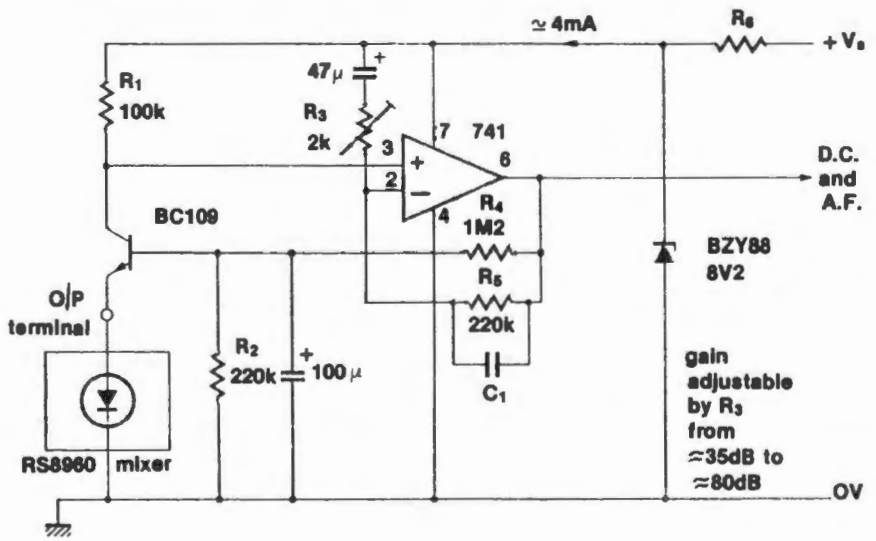
The value of R_6 is dependent on the supply voltage V_s and can be calculated from Eq. 5.

$$R_6 = (V_s - 8.2)\ 100\ \Omega \quad \ldots . \ (5)$$

hence for a supply of 12V

R_6 = 380 Ω nearest preferred value is 390 Ω

Figure 8 **Low impedance amplifier for use with RS 8960**



Modification to the circuitry to provide frequency cut-off for frequencies in excess of 200Hz may be desirable for certain applications to avoid unnecessary degradation of the signal-to-noise performance. This may be achieved by selecting an appropriate value for C_1 from Eq. 6.

$$C_1 = \frac{1}{2\pi\ fc\ R_5} F \quad \ldots . \ (6)$$

where fc = 3dB cut off frequency in Hz

for fc = 200Hz

C_1 = 3.6nF

It is important that supplies to the amplifier and those used to supply the Gunn device and mixer diode bias, are stabilised to a level compatible with the module noise level (that is, less than 2μV). Instability of the Gunn supply will result in a.m. and f.m. noise on the L.O. and subsequent degradation of the module signal-to-noise ratio.

It is recommended that the Gunn device supply voltage is derived from a low impedance source capable of supplying up to 250mA to allow for starting current (see Fig. 3). The supply should be free of transients in excess of 9.0V and the miniature 10nF capacitor, wired directly between the earth tag and the Gunn device terminal to prevent parasitic low frequency oscillations in the supply circuit, must be left connected.

For optimum signal to noise ratio the mixer diode should feed into an impedance of ≈600 Ω.

Externally-generated noise

Noise from external electromagnetic radiation can be minimised by enclosing the module in a metal housing.

The module will respond to fluorescent a.c. lighting in the target area, because the ionised gas acts as a modulated reflecting target during discharge, and so a signal at twice the mains frequency appears at the detector.

Other possible causes of external noise, and therefore false alarms, are: vibration due to heavy vehicles which can cause the rigidly-mounted intruder alarm to move relatively to other reflecting surfaces in the room; air turbulence in plastic water-pipes; movement of suspended objects, etc.

Bandwith

Most of the noise sources outlined above give a broad noise spectrum, and their effects can be significantly reduced by the introduction of filters to limit the amplifier bandwidth. As stated earlier, the frequency of the doppler output is approximately 31Hz per mph of target speed.

On first consideration, a processing circuitry passband centred on 120Hz might be thought desirable, as this would give a maximum response at medium walking pace. However, the majority of existing alarm systems use amplifiers with a peak response at about 20Hz, the signal being attenuated at frequencies above 40Hz and below 5Hz.

The reason for this choice of passband is the fact that both hesitant movement, and the limb and torso movements associated with regular walking, produce velocity variations which pass through zero. Thus, doppler frequencies from zero upwards are produced. It has been found that a man target moving at slow walking pace axially towards or away from the microwave radiating antenna generates a doppler frequency spectrum centred at about 50Hz. Similar movement at right angles to the antenna axis produces a spectrum from about 5 to 15Hz.

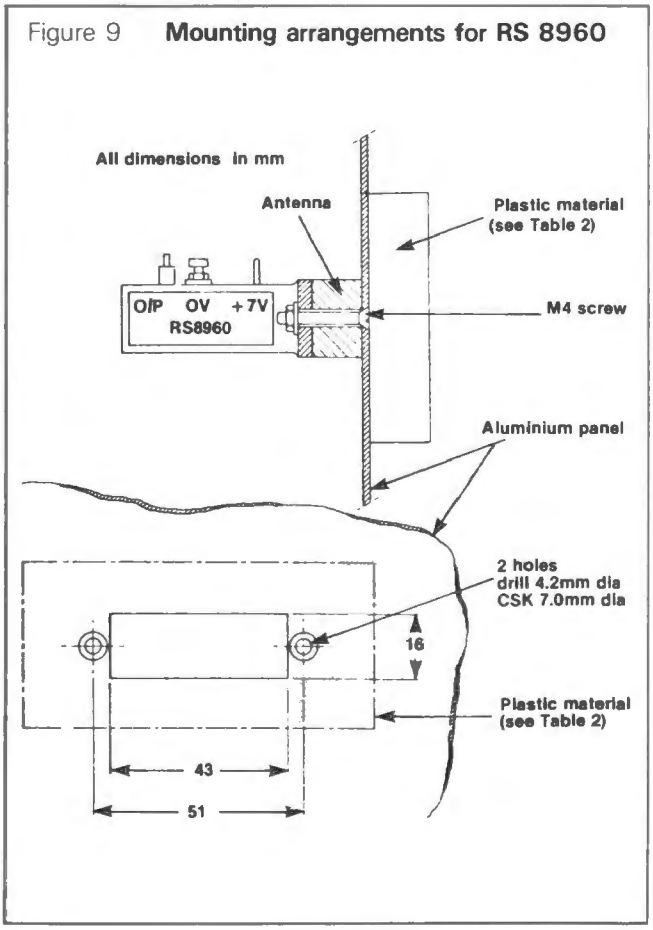
Module mounting configuration

For optimum signal-to-noise ratio, it is recommended that the module and antenna are mounted using M4 screws, to a 14-18 s.w.g. thick metal plate with aperture dimensions as in Fig. 9. In this configuration, the metal plate forms the front panel of the equipment, and the antenna radiates into free space. If the equipment-housing is all metal, any back radiation will be totally contained.

As outlined earlier, the total mixer bias under the optimum operating conditions is approximately 42μA. (35μA d.c. bias + 7μA from −19dBm of coupled L.O. power.)

If however, for environmental reasons, it is considered desirable to cover the antenna aperture, then it is recommended that a plastic material (approx. 10-20mm thick) is fixed to the metal plate with adhesive. A suitable plastic material is expanded polythene or polystyrene, see Table 2. In this case, the L.O. power coupled to the mixer will be −15dBm, and the total mixer bias current will now be approximately 50μA.

Figure 9 **Mounting arrangements for RS 8960**



The increase in L.O. power will, in general, give rise to an increase in a.f. output voltage for a given target, but this will be accompanied by a degradation in signal-to-noise ratio. For −15dBm of L.O. power, the degradation in signal-to-noise ratio should be acceptable for most applications.

However, further increase in the level of coupled L.O. power arising from the use of thick or 'microwave' reflective covering materials, will:

1 continue to increase the a.f. output voltage from the mixer (note that, the increase will not be the same for all modules) but at the same time, degrade the signal-to-noise ratio;

2 present a mismatch to the Gunn device which may impair the switching and running performance, and may 'pull' the frequency outside the allocated operating frequency band.

Table 2 compares the L.O. coupling level obtained for different covering materials at the antenna.

Table 2. Comparison of different covering materials

L.O. Coupling (dBm)	Mixer total bias (μA)	Antenna covering material
—	35 (d.c. only)	—
−19	42	No covering
−15	50	10 to 20mm expanded polythene or polystyrene

Applications

The circuit shown in Fig. 10 is a complete Doppler radar system suitable for detecting most moving targets, including people.

Power for the Gunn device, mixer diode and A.F. amplifiers is supplied by the regulator, shown in Fig. 11, which provides an output voltage of +7V w.r.t. 0V.

A ready made p.c. board is available under Stock No. 434-582 which can accommodate the circuits of Figs. 10 and 11.

Figure 11 **7V Regulator**

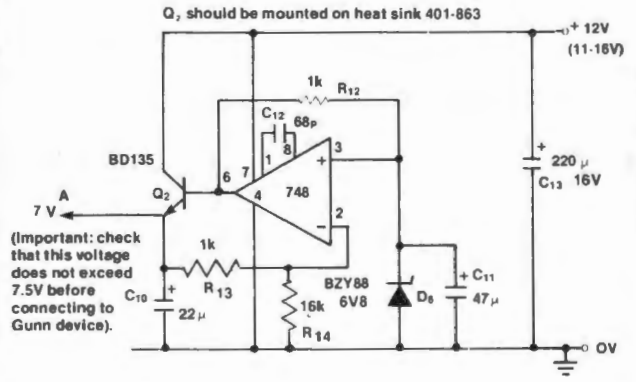
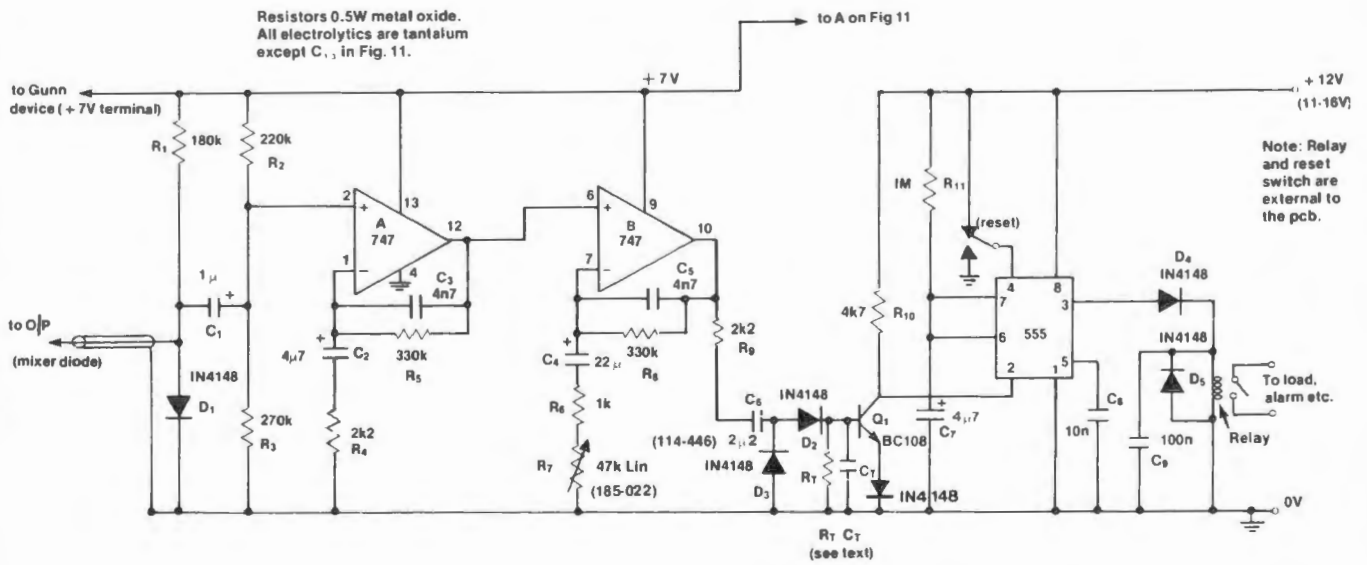


Figure 10 **Doppler detection system**

Licensing reference number: R/3598CD



The output from the mixer diode is a.c. coupled via C_1 to the first half of the 747 OP-AMP. This amplifier has a voltage gain of approximately 44dB and is 3dB down at 100Hz. The output of the first stage is directly coupled to the second half of the 747 which has an adjustable gain from 17dB to 50dB controlled by the 47k log. pot., R_7. The output of the second stage is fed via R_9 and C_6 to the diode D_2. This diode feeds positive charge pulses to the capacitor C_T which causes its voltage to rise. Connected across C_T is the bleed resistor R_T which causes the capacitor to discharge exponentially with time. The R_T and C_T network therefore provides the system with a level of noise immunity, as the charge on C_T generated by random external noise 'leaks' through R_T preventing the voltage on C_T rising enough to switch on Q_1. The appearance of a moving target in the radar range generates pulses which charges C_T at a faster rate than it discharges, hence, C_T voltage rises and Q_1 switches on. As Q_1 saturates, the trigger input to the 555 timer is pulled down to V_{CE} (sat) causing the output on pin 3 to go high activating the relay for a time governed by R_{11} and C_7. Using the values shown the relay is activated for approximately 5 sec.

R_T can be 150k Ω and C_T a 47μF tantalum capacitor but these values may be altered to suit individual conditions. Altering the R_T C_T time constant by increasing R_T will reduce C_T discharge rate and hence lower the level of noise immunity. Increasing C_T will increase the discharge rate but will also increase the amount of charge required to raise its voltage to switch on Q_1, hence, a higher level of noise immunity is achieved.

The 555 timer 'on' time can be adjusted by altering the values of C_7 and R_{11} according to the equation below.

$T = 1.1\ C_7\ R_{11}$ where T in sec.
C_7 in F
R_{11} in Ω

For further information on the 555 timer see Data Sheet 2113.

For low internal noise the fixed resistors R_1 to R_9 should be low noise types i.e. thick film. However, metal oxide can be used throughout the internal noise accommodated by adjusting R_T and C_T.

C_1, C_2, C_4 should be low leakage capacitors such as tantalum. C_6 and C_T should ideally be very low leakage and polyester or polycarbonate types are recommended. A tantalum capacitor may be employed for C_T in most applications.

The circuit should be contained in an earthed all metal box to provide screening from electrical interference. Ideally the supply to the system should be derived from a 12V battery, and not from a mains power supply. This is because the very high voltage gain available from the A.F. amplifiers around 50 to 100Hz could result in mains noise being amplified by induction pickup in the signal leads thereby causing a false alarm. Single point earthing should be employed to prevent earth loops and the signal connections from the O/P terminal on the module to the input of the amplifier should be via a screened lead, earthed at one end only.

Licence requirements

In order to operate this device legally, it is necessary to possess a Telapproach System Licence as defined in the Wireless Telegraphy Act 1949.

Packaged with the RS 8960 is the necessary Department of Trade and Industry Application Form for the Licence which has a validity period of 5 years. This form should be completed and posted with the appropriate fee to:

The Cashier
Department of Trade and Industry
Accounts Branch
24-26 Newport Road
Cardiff, CF2 1SY

This licence is only valid when the design is to the circuit as given in Figure 10 of this Data Sheet.

Please state the reference number of this circuit, R/3598 CD, in section 3 of the Application Form when applying for a licence.

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RS data

Strain gauges and amplifier

Four foil type strain gauges encapsulated in a polyester film. All strain gauges have integral 30mm leads, to alleviate damage to the gauges due to excess heat being applied during soldering and installation. Self adhesive terminal pads are supplied with each gauge which are used as an interface between the gauge leads and connecting leads to peripheral measuring circuitry.

Types 308-118 and 304-374 are temperature compensated to match aluminium (coefficient of expansion 23.4 × 10^{-6}/°C) and are indicated by blue colour coding of the polyester backing material.

Specification

Gauge length	8mm
Measurable strain	3 to 4% max
Temperature range	−30°C to +80°C
Gauge resistance	120Ω ±0.5%
Gauge factor	approx 2.1
Gauge factor tolerance	within ±1%
Fatigue life	more than 10^6 reversals at 1000 × 10^{-6} strain.
Foil material	Cu Ni Alloy
Backing material	polyester sheet

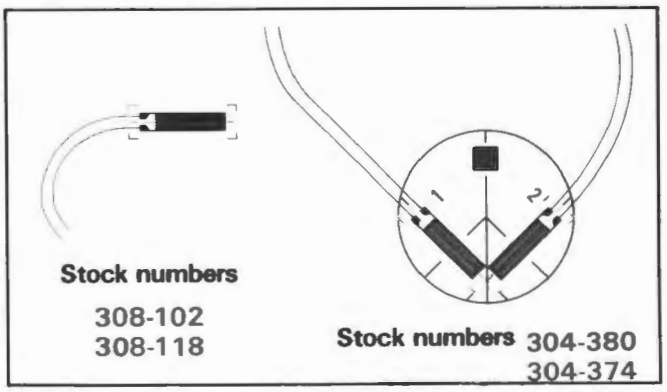
Construction and principle of operation

The strain gauge measuring grid is manufactured from a copper nickel alloy which has a low and controllable temperature coefficient. The actual form of the grid is accurately produced by photo-etching techniques. Polyester film is used to encapsulate the grid, which helps to protect the gauge from mechanical and environmental damage and also acts as a medium to transmit the strain from the test object to the gauge material.

The principle of operation of this device is based on the fact that the resistance of an electrical conductor changes with a ratio of $\Delta R/R$ if a stress is applied such that its length changes by a factor $\Delta L/L$. Where ΔR is change in resistance from unstressed value, and ΔL is change in length from original unstressed length.

Types 308-102 and 304-380 are self temperature compensated to match mild steel (coefficient of expansion 10.8 × 10^{-6}/°C) and are indicated by red colour coding of backing.

Types 308-102 and 308-118 are intended for uniaxial strain measurement only while types 304-380 and 304-374 are ideal for biaxial measurement, having 2 strain gauges mounted at right angles to each other on the same plane. Included on the backing material are gauge axis lines, to enable accurate alignment of gauges along principal strain lines.



The change in resistance is brought about mainly by the physical size of the conductor changing and an alteration of the conductivity of the material, due to changes in the materials structure.

Copper nickel alloy is commonly used in strain gauge construction because the resistance change of the foil is virtually proportional to the applied strain. i.e.

$\Delta R/R = K.E$

where K is a constant known as the gauge factor, $= \frac{\Delta R/R}{\Delta L/L}$

and E = strain = $\Delta L/L$ $\therefore K = \frac{\Delta R/R}{E}$

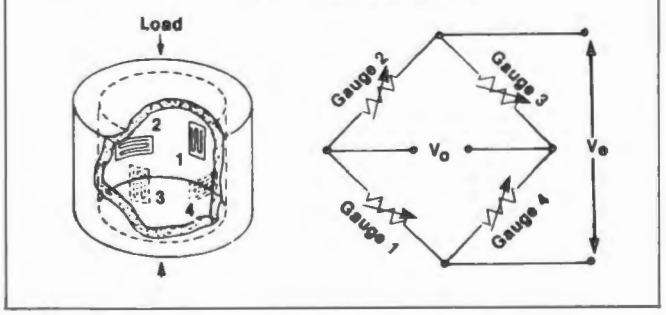
The change in resistance of the strain gauge can therefore be utilised to measure strain accurately when connected to an appropriate measuring and indicating circuit e.g. RS Strain Gauge Amplifier 308-815 detailed at the rear of this data sheet.

Application

When strain gauges are used in compressive load transducer applications, which normally require more stringent accuracy requirements, a full bridge circuit is used with active gauges in all four arms of the bridge, see Figure 1:—

The load transducer shown in Fig. 1 utilises four strain gauges attached to the cylinder. The gauges are connected into the bridge circuitry in such a manner as to make use of Poissons ratio i.e. the ratio between the relative expansion in the direction of force applied and the relative contraction perpendicular to the force, to increase the effective gauge factor and thus the sensitivity.

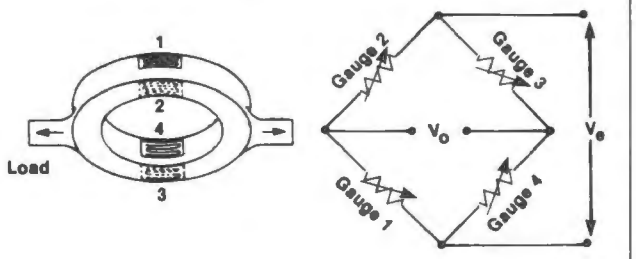
Figure 1 **Compressive load transducer**



To measure tensile loads, a ring with gauges attached as shown in Fig. 2 may be used:—

Under the action of a tensile load, the curvature of the ring in Fig. 2 is deformed such that the inner gauges undergo tension while the outer gauges experience compressive forces.

Figure 2 **Tensile load transducer.**



Instructions for mounting of strain gauges

In order to obtain the best possible results from a strain gauge, it is important to thoroughly prepare the gauge and the surface of the specimen to which the gauge is to be attached, prior to bonding with the adhesives recommended in section 3 below.

1) Specimen surface preparation

An area larger than the installation should be cleared of all paint, rust etc., and finally smoothed with a fine grade emery paper or fine sand blasting to provide a sound bonding surface.

The area should now be degreased with a solvent such as RS P.C.B. Solvent Cleaner, stock no. 555-134, and finally neutralised with a weak detergent solution. Tissues or lint free cloth should be used for this operation, wetting the surface and wiping off with clean tissues or cloth until the final tissue used is stain free. Care must be taken not to wipe grease from a surrounding area onto the prepared area or to touch the surface with the fingers.

This final cleaning should take place immediately prior to installation of the gauge.

2) Strain gauge preparation

By sticking a short length of adhesive tape along the upper face of the gauge it may be picked up from a flat clean surface. Holding both ends of the tape, orientate the gauge in the desired location and stick the end of the tape furthermost from the tags to the specimen. Bend the other end of the tape back on itself thereby exposing the back of the gauge.

3) Adhesives and stain gauge installation

Two basic types of adhesive are recommended: i) RS cyanoacrylate, ii) RS "quick-set" epoxy. When using epoxy adhesive coat the back of the gauge with adhesive and gently push the gauge down into position, at the same time wiping excess adhesive to the two outside edges of the gauge. Stick the whole length of tape to hold the gauge in position. Care should be taken that there is an even layer of adhesive and no air bubbles are left under the grid. Cover the gauge with cellophane or polyethylene etc., and apply a light weight or clamp as required until adhesive has set. Remove tape by slowly and very carefully pulling it back over itself, starting at the end furthermost from the tags. Do not pull upwards.

If cyanoacrylate adhesive is to be used stick one end of the tape down to the specimen completely up to the gauge. Drop a fillit of adhesive in the 'hinge' point formed by the gauge and the specimen. Starting at the fixed end, with one finger push the gauge down at the same time pushing the adhesive along the gauge in a single wiping motion until the whole gauge is stuck down. Apply pressure with one finger over the whole length of the gauge for approximately one minute. Leave for a further three minutes before removing tape.

4) Wiring

The RS Strain Gauges are fitted with 30mm leads to enable the gauge to be soldered to the terminal pads supplied with each gauge, which should be fitted adjacent to the strain gauge. The lead out wires are fragile and should be handled with care. After soldering all traces of flux should be removed.

Installation protection

RS Strain Gauges are encapsulated and therefore are protected from dust and draughts etc. If however, additional protection from humidity, moisture, and mechanical damage etc is required RS Silicone Rubber Compound, stock no. 555-588, may be used. This should be carefully spread over the installation using a spatula.

Connecting to strain gauges

The following bridge circuits are shown with connections referring to the basic amplifier circuit, Fig. 7. All resistors, precision wirewound 0.1% 5ppm. (For RS Precision Resistors see current catalogue).

Note: The expressions are assuming that all gauges are subjected to the same strain. Some configurations produce different strain in different gauges, and allowance must be made.

Figure 3 **Full bridge**

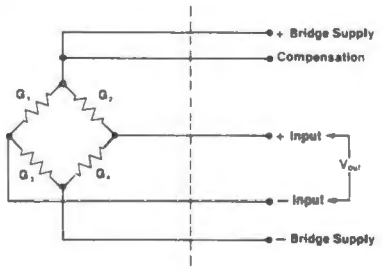


Figure 4 **Half bridge**

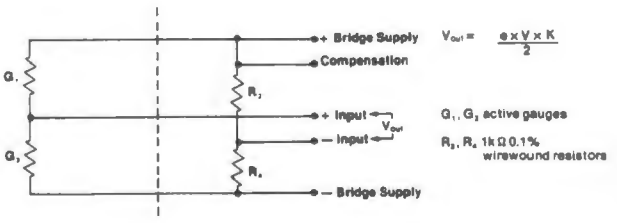


Figure 5 **Quarter bridge (3 wire)**

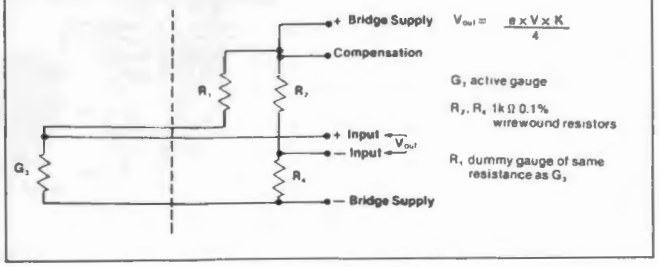
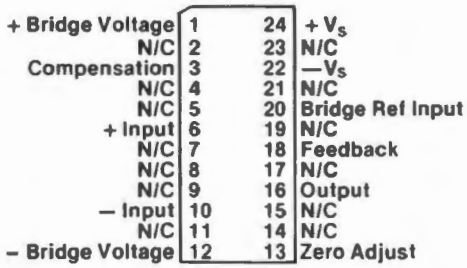


Figure 6 **Pin connections**



Strain gauge amplifier (Stock number. 308-815)

Description & operation

The Strain Gauge Amplifier is a purpose designed hybrid low noise low drift linear D.C. amplifier in a 24 pin D.I.L. package, specifically configured for resistive bridge measurement and in particular Strain Gauges, e.g. RS types 308-102, 308-118, 304-380 and 304-374 detailed earlier in this data sheet.

Foil strain gauges when attached to a specimen, produce very small changes in resistance (typically 0.2mΩ in 120Ω per microstrain), and are thus normally connected in a Wheatstone bridge. Overall outputs of less than 1mV on a common mode voltage of 5 volts may be encountered, requiring exceptional common mode rejection which cannot easily be provided by conventional means.

The Strain Gauge Amplifier overcomes the problem of common mode rejection by removing the common mode voltages. This is achieved by controlling the negative bridge supply voltage in such a manner that the voltage at the negative input terminal is always zero. Thus for a symmetrical bridge, a negative bridge supply is generated equal and opposite to the positive bridge supply, hence zero common mode voltage.

The advantages of such a system are:—

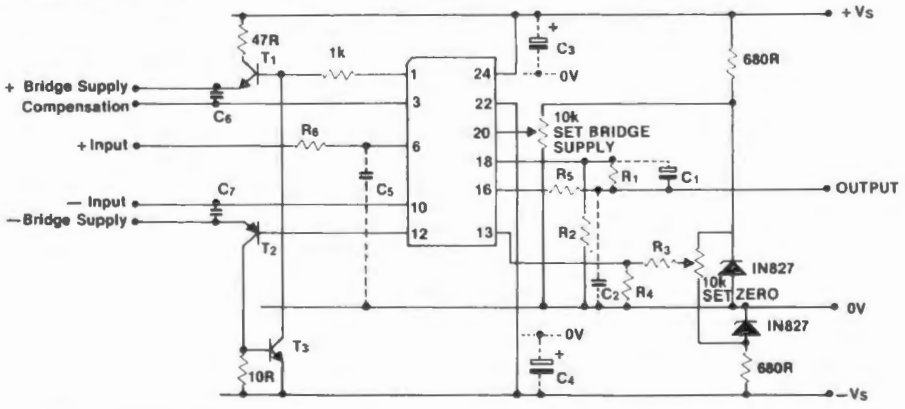
1. No floating power supply needed.
2. Bridge supply easily varied with remote sense if necessary.
3. 5 wire remote sense system.
4. Freedom from common mode effects.
5. Very high stability D.C. amplifier enables numerous configurations to be assembled.
6. Low Noise.
7. High speed (at low gains).

Specification

(At 25°C ambient & ± 12V supply unless otherwise stated.)

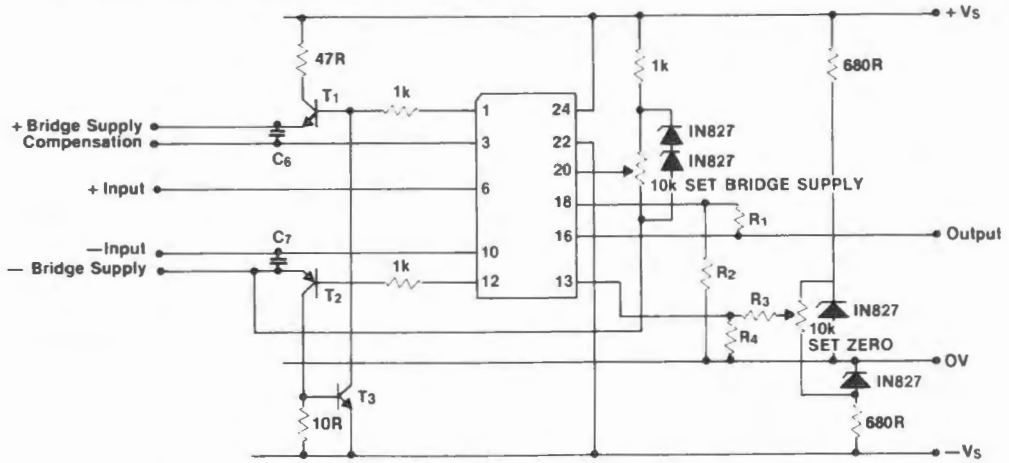
Supply Voltage	±2 to ±20Vd.c.
Input Offset Voltage	1mV max
Input Offset Voltage/Temperature	1μV/°C max
Input Offset Voltage/Supply	5μV/V max
Input Offset Voltage/Time	1μV/month max
Input Impedance	>2.5MΩ min
Input Noise Voltage	1μV p.p max
Band Width (Unity Gain)	400kHz
Output Current	5mA
Output Voltage Span	$\pm V_s$-3V
Closed Loop Gain (Adjustable)	5 to 10,000
Open Loop Gain	>100dB
Common Mode Rejection Ratio	>100dB
Bridge Supply Voltage/Temperature	20μV/°C
Maximum Bridge Supply Current	12mA
Power Dissipation	0.5W
Warm Up Time	5mins
Operating Temperature Range	-25°C to +85°C

Figure 7 **Basic circuit (gain approx. 1000)**



RS data

Figure 8 **Circuit for semiconductor gauges and transducers**



Component values (Figs 7 and 8):

R_1 100k	C_1, C_6, C_7 100n(typ.)
R_2 100R	C_2, C_5 10n(typ.)
R_3 100k*	C_3, C_4 10μ(tant.)
R_4 68R*	T_1 BD135
R_5 10R	T_2 BD136
R_6 100R(typ.)	T_3 BC108

Only typical values are given for certain components, as adjustment of these values may be necessary in specific applications to obtain optimum noise reduction (see Minimisation of Noise, page 4).

*R_3 and R_4 values may be adjusted to alter the zero adjustment range when compensating for bridge imbalance.

Notes:

Gain is defined as $1 + \frac{R_1}{R_2}$

Zero Adjustment Range $\pm 6.2 \times \frac{R_4}{R_3 + R_4}$ Volts

Total Bridge Supply = 2 × Bridge Ref Input (pin 20)

C_5 may be omitted for input lead lengths of less than 10 metres.

T_1 and T_2 provide bridge currents up to 60mA and should be kept away from the amplifier.

T_3 and R_5 provide current limit of approx 60mA.

Where high stability power supplies are being used zero and bridge supply reference may be taken direct from the power rails.

The high output of some semiconductor strain gauges may cause large amounts of asymmetry to the bridge. In correcting for the common mode change, the negative bridge voltage will change, causing a span error. This may be calibrated out or the arrangement above used to eliminate the cause of the error. Some semiconductor strain gauge transducers are temperature compensated by the use of series arm compensation. Thus the common mode voltage changes with temperature, and hence the arrangement above should be used. This operates by referencing the positive bridge supply to the negative supply, thus varying the common mode but not the overall bridge supply.

Minimisation of noise

1. Inherent white/flicker noise in amplifier.

To keep this to a minimum use high quality (metal film) resistors and protect the amplifier from excessively high temperatures. The inherent noise level may be further reduced from its already low value by fitting C_1 and C_2 to reduce the operating bandwidth.

2. Supply frequency (or harmonics) interference.

If at 100Hz then the cause is most likely to be from power supply rails, so use stabilised lines. If at 50Hz then it is generally caused by the location of the supply transformer and/or the wiring. Relocate the supply transformer, screen the input leads to the amplifier, and if possible reduce the operating bandwidth by fitting C_1 and C_2.

3. Power supply transient interference.

It is good practice to decouple the supply lines to the amplifier, by fitting C_3 and C_4, as close to it as possible. If a particular nuisance then fit a mains suppressor, e.g. RS Stock no. 238-407.

4. Electromagnetic interference.

This may be picked up by input leads, output leads, supply leads or direct into the circuit. Minimisation involves a combination of screening, decoupling and reducing operating bandwidth. Screening. The shield should be connected to only one earth potential at the receiving monitoring equipment end. Try not to earth any of the d.c. power lines (e.g. 0V). If the shield at the sensor end is earthed then earth the shield at the receiving end and if possible connect this earth potential to the strain gauge amplifier circuit shield. Decouple the power supply leads by fitting C_3 and C_4, decouple the input leads with R_6 and C_5 (note a similar action on the input is not possible). Remove any pickup from the output leads by fitting R_5 and C_2. Fit C_5 if input leads are more than 10m long and fit C_6 if remote sense is longer than 10m. Reduce the operating bandwidth by fitting C_1 and C_2.

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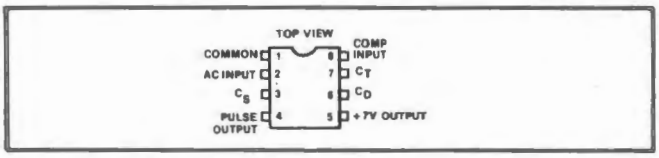
RS data

Zero voltage switch 443A

Stock number 307–985

A zero voltage switch i.c. offering symmetrical burst control of an external triac. Ideal for power control in many heating applications.



Features

- High immunity against spurious triac firing under noisy mains conditions.
- Low external component count.
- Symmetrical burst control with zero voltage switching.
- Firing pulses inhibited before power supply is established.

Absolute maximum ratings (with respect to pin 1)

Voltages

Voltage on pin 8, ——— 10V
Voltage on pin 4, ——— 10V

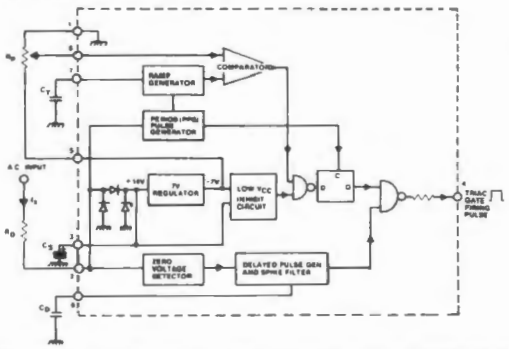
Currents

Supply current, pin 2 peak value ——— ±50mA
Non-repetitive peak current ($t_p \geq 250\mu S$) — ±200mA
Output current, pin 5 ——— Short circuit protected
Output current, pin 4, average value ——— 10mA

Temperatures

Operating ambient temperature ——— −10 to 75°C
Storage temperature ——— −55 to +125°C

Figure 1 **Block diagram**



Electrical characteristics at 25°C unless otherwise stated

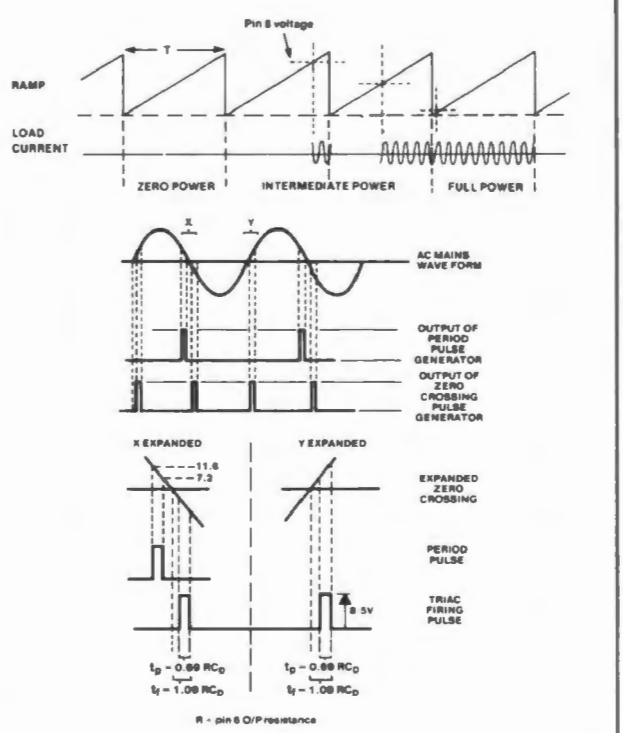
Parameter	Conditions	Min.	Typ.	Max.	Units
Pin 3 voltage	I = 16mA	—	14.7	16	V
Supply current, I_2	Excluding triac trigger pulse and pin 5 output	—	—	7.2	mA
R_p resistance range	total	18	—	140	kΩ
Triac gate drive (pin 4)					
open circuit voltage	ON	—	8.5	—	V
open circuit voltage	OFF	—	—	0.1	V
output current (peak)	Vg = 2V	80	100	—	mA
output current (peak)	Vg = 4V	50	70	—	mA
output current (peak)	short circuit	—	—	200	mA
Pin 8 bias current		—	—	1	μA
Pin 8 offset	w.r.t. ramp voltage	—	—	±20	mV
Ramp period variation	R_p = 100kΩ, C_T = 0.68μF	27	30	33	s
Pin 6 output resistance		21.5	27	32.5	kΩ
Total power dissipation		—	—	250	mW

Operation

The externally current limited AC supply is applied to the device, and rectification followed by shunt regulation provides a 14V DC supply. This is externally smoothed before application to the 7.0V series stabiliser which feeds the control potentiometer. The stabiliser must be within regulation, of operation of the 'Low V_{cc} Inhibit' circuit will result. This circuit overrides all other circuitry and prevents unsuitable firing pulses from being supplied to the triac at 'switch-on'. The current limited AC supply also drives the Period Pulse Generator (PPG) and zero voltage crossing circuits.
The PPG produces a single short duration pulse for each completed mains cycle and serves two purposes. First it is used to clock logic information such that the circuit behaves in a symmetrical manner and only complete mains cycles are applied to the load. Secondly the pulse is used to switch timing components in the ramp generator and this enables long time constants to be achieved without having to resort to the use of electrolytic capacitors.
The zero voltage crossing detector controls a pulse generator that has a delayed output. The delay is necessary since, with loads that are slightly inductive or low power resistive, the triac load current may not reach its required holding level at zero voltage point.
Both delay and pulse duration are defined by an external capacitor and this further serves the purpose of filtering out spikes which occur in the zero crossing region. Automatic rejection takes place of spikes having a duration of up to 50 per cent of the normal width of the triac firing pulse.
The comparator amplifier has differential inputs and these are used to compare the potential appearing on the slider of the control potentiometer with that of the ramp waveform. The output of this amplifier controls the logic circuitry and the potentiometer setting defines the fraction of the ramp period for which the triac is in conduction so controlling the power in the load. See Fig. 2.

RS data

Figure 2



Design Procedure

The ramp period T defines the burst firing repetition rate of the triac supplying the load. For most heating applications 20s ramp periods are adequate. Eqn 1 is used to calculate T.

$T = 2 \times C_T \times R_p \times V_s$ seconds —Eqn 1

Where C_T is in Farads, R_p is in ohms, V_s is in volts r.m.s.

e.g. for $R_p = 100k\Omega$ $C_T \doteq 470nF$ $V_s = 240V$ r.m.s.

$T = 2 \times 470 \times 10^{-9} \times 100 \times 10^3 \times 240 \approx 22.6$ seconds

The other component values required for correct circuit operation should be evaluated as follows.

1) Calculate length of trigger pulse required (t_p)
2) Calculate average gate drive current (I_4AV)
3) Calculate total supply current (I_2)
4) Calculate supply dropper resistance (R_p)

1) Trigger pulse length t_p

The triac cannot latch on until the mains supply voltage exceeds the sum of the triac on-state voltage plus the voltage dropped across the load by the triac holding current. From this voltage requirement the value of t_p can be calculated.

e.g. for triac BT139 (see data sheet 2488)

worst case holding current $I_H = 30mA$
on state voltage $V_{TM} = 1.6V$

Assuming a triac resistance load of 2kW and 240V ±10% supply.

(load) $R_L = \frac{V_s^2}{P}\Omega$ for p in Watts —Eqn 2

then $R_L = \frac{(240 \times 1.1)^2}{2 \times 10^3} = 34.8\Omega$ worst case

Now $V_L \geq V_{TM} + (I_H \times R_L)$ —Eqn 3

Where V_L = supply voltage to latch triac

then $V_L = 1.6 + (30 \times 10^{-3} \times 34.8) = 2.6V$

The trailing edge of the firing pulse is time t_f after the zero crossing point of the supply waveform and t_f must occur no sooner than

$t_f = \frac{V_L}{V_S \times \sqrt{2} \times 2\pi f}$ —Eqn 4

f = supply frequency in Hz

then t_f min $= \frac{2.6}{240 \times 0.9 \times \sqrt{2} \times 2 \times \pi \times 50} = 27.1\mu S$

but from Fig. 2 $t_f = 1.09RC_D$ and $t_p = 0.69RC_D$

where R = pin 6 O/P resistance = 21.5kΩ min

then $C_D = \frac{t_f}{1.09 \times R} = \frac{27.1 \times 10^{-6}}{1.09 \times 21.5 \times 10^3} = 1.16nF$

Nearest preferred value C_D = 1.5nF ±2½% polystyrene

2) Average gate drive current I_4AV

Max. gate drive current into a short circuit = 200mA and as this current occurs $2 \times t_p$ every mains cycle

$I_4AV = 2 \times t_p \times f \times I_4S/C$ A —Eqn 5

but $t_p = 0.69RC_D$ and R typ = 27kΩ

then $I_4AV = 2 \times 0.69 \times 27 \times 10^3 \times 1.5 \times 10^{-9} \times 50 \times 200 \times 10^{-3}$
$= 0.56mA$

3) Total supply current I_2

$I_2 = 7.2 \times 10^{-3} + 1$ pin $5 + I_4AV$ —Eqn 6

where I pin $5 = \frac{7}{R_p}$

then $I_2 = 7.2 \times 10^{-3} + \frac{7}{100 \times 10^3} + 0.56 \times 10^{-3} = 7.83mA$

4) Supply dropper resistance R_D

$R_D = \frac{V_s \text{ peak} - V_3 \text{ max}}{\pi \times I_2}$ —Eqn 7

then $R_D = \frac{(240 \times 0.9 \times \sqrt{2}) - 16}{\pi \times 7.83 \times 10^{-3}} = 11.8k\Omega$

Nearest preferred value = 10kΩ ±5%

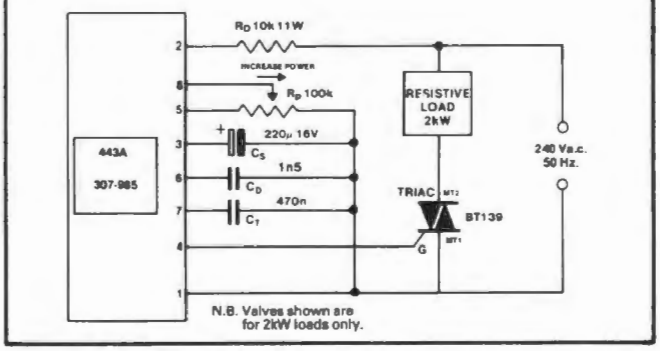
Max. power dissipated by R_p is given by

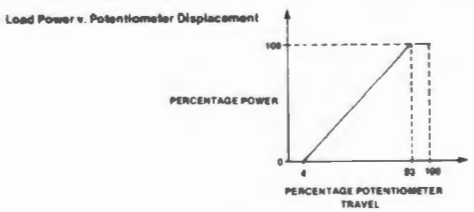
$\frac{V_s^2 \text{ max}}{R_D \text{min}} = \frac{(240 \times 1.1)^2}{9500} = 7.3W$

Hence choose 10kΩ 11W wirewound for R_D

The above design values have been incorporated in Fig. 3 shown below. By following the above procedure the 443A can be adapted to particular application requirements.

Figure 3





This characteristic applies to a linear potentiometer. Different control characteristics are easily obtained by using a non-linear potentiometer and/or offset resistors in the potentiometer circuit.

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RS data

3½ Digit L.C.D. digital panel meter

Stock number 258-827

The RS 3½ digit LCD digital panel meter is housed in a very compact front panel mounting case made of matt black flame retardant ABS which is held in the panel by a simple metal clamp. The meter has a 0.5 inch liquid crystal display, viewed through a clear anti-glare filter, to indicate the maximum count of ± 1999. The decimal points are externally programmed by simply connecting the respective decimal point pin to the 'dp' pin. The meter uses the dual slope integration technique and offers true differential input and reference (for ratiometric measurements), auto-polarity auto-zero and f.s.d. of 199.9 mV.

The low supply current at 9V combined with the small size makes the meter ideally suited for battery powered portable equipment.

Specification

Maximum ratings

Max. supply voltage +V to −V	15V
Max. supply current	2mA
Max. input voltage	+V to −V
Storage temperature range	−20°C to +70°C
Working temperature range	0 to +50°C
Max. analogue common output current	10mA (in addition to supply current)
*See overload Protection	

Overload Protection

Positive supply overload +V to −V	30V max. cont.
(Unit will draw 15mA nom. at 30V	
Max. input voltage with supply overload	15V w.r.t. −V
Reverse polarity protection +V to −V	15V max. cont.
(Unit has series diode)	

Performance

FSD	±199.9mV
Accuracy	±0.1%±1 count
Resolution	100μV
Temperature coefficient	±330ppm/°C max.
Temperature drift of zero	±1 count over range 0 to +50°C
Input impedance	100MΩ min.
Input leakage current	10 pA max.
Common mode rejection	80 dB typ.
Common mode voltage range (+V to −V up to 15V)	+V −0.5V and −V + 1.0V
Common mode voltage range (+V to −V 15 to 30V)	within −V + 14.5 and −V + 1.0
External reference voltage range	within CMVR
Sampling rate	approx. 4 per second
Integration time	60 ms

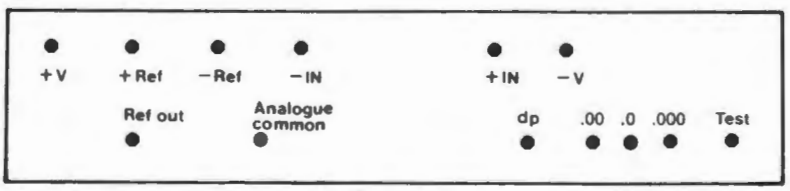
Display

Polarity	shown by minus sign
Over-range	shown by 3 L.S.D.'s blanked
Decimal point	externally programmable
Test facility	test pin to dp pin; all segments displayed

Dimensions

Bezel size	96×56.5mm
Overall depth	23mm
Depth behind panel	21mm
Panel cutout	91×51.5mm
Panel thickness range	1 to 6.3mm

Connections



Rear View

Connections may be made by wire-wrapping or soldering to the terminals.

RS data

Supply

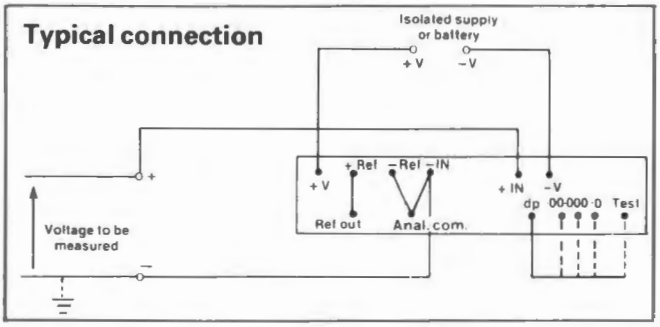
The supply voltage to the meter must be d.c., normally up to a maximum of 15 volts. However, it should be noted that the supply must be either isolated (or derived from a battery) or if an existing system power supply is to be utilised the −V connection must *not* be ground (0V) referenced. In this latter case a dual rail power supply should be used (typically ±5V) with either the 0V left disconnected or connected to −IN if a single ended input is required. −Ref and Analogue common should be connected together, but not to −IN (However a non-zero reading of 1-2 counts may exist due to a common mode error between −Ref and −IN.)

Functions

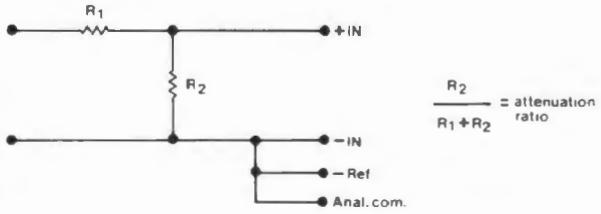
Decimal point: Connect the respective pin to the dp pin (see rear view connections).
Reference: Connect by links as shown in 'typical connection' below and adjust the reference voltage (between +Ref and −Ref) to 100mV by means of the ten-turn pot, accessed through the hole in the underside of the case. (Alternatively apply a known voltage to the inputs (e.g. 199.9mV) and adjust the reference pot to give an identical reading.)
Analogue common: This is to set the common mode voltage and is typically +V − 2.8 V.
Test: This pin performs two purposes; when taken to dp it acts as a display test where all the segments are displayed, and secondly it may be used as a common mode reference level to allow compatibility with most op amps (see application circuits). N.B. When used in the display test mode, a d.c. voltage is applied to the LCD and therefore to prevent "burning" the display, prolonged use must be avoided.

Application circuits

Typical connection

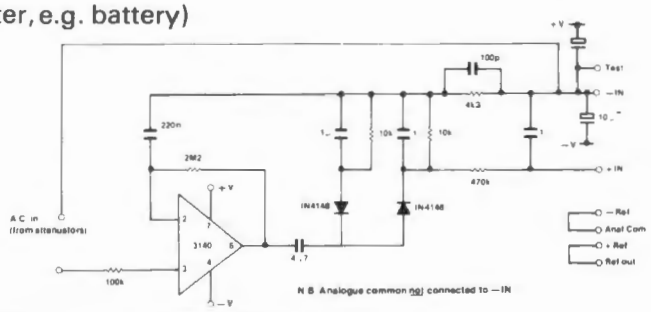


Attenuator



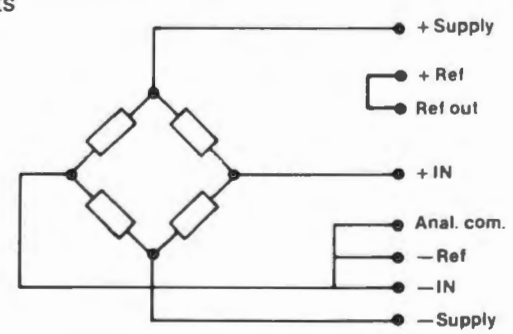
A.C. Rectifier (op amp using same supply as meter, e.g. battery)

This circuit also serves to show how the test pin may be used as a common mode reference voltage when a non-zero referenced supply is used.

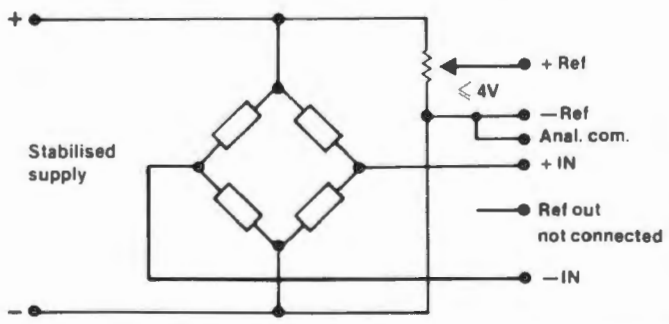


Bridge circuits

Bridge connections for non-ratiometric measurements



Bridge connections for ratiometric measurements



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RS data

3½ Digit L.E.D. digital panel meters

The range of RS 3½ digit L.E.D. digital panel meters includes three supply options, 5V d.c., 110V a.c. and 240V a.c. each available with 200mV, 2V, 20V or 200V d.c. FSD. The meters have a maximum count of ±1999 indicated by four 0.43 inch high red L.E.D. displays viewed through a red antiglare filter. Meters are housed in front panel mounting DIN standard boxes of black flame retardent ABS (which fit both DIN and NEMA standard panel cut-outs) with connections made via a 24 way 0.1 inch edge connector. Features include auto-zero, auto-polarity with externally programmable decimal point. The 200mV and 2V meters have a differential input and reference for ratiometric measurement whilst the 20V and 200V meters are single ended input without external reference connections.

Features

- 3 supply options
- Bright 0.43in display
- Auto polarity
- Internal band-gap reference
- 0.1% accuracy
- 4 FSD versions
- Auto zero
- Programmable decimal points
- DIN standard cut-out

Applications
Simple bridge (for non ratiometric measurements) Ratiometric bridge.

Specification

	Meter supply voltage (nominal) 5V d.c.*	110V a.c.	240V a.c.
Supply voltage range	4.75 to 5.25V	99 to 121V	216 to 264V
Supply current/power	250mA	4.5VA	4.5VA
Supply frequency	d.c. (smooth)	50 to 60Hz	50 to 60Hz
Outputs: +V (typically 5V d.c.)	—	5mA	5mA
: −V (typically −3.6V d.c.)	1mA	1mA	1mA
: Anal. com. (typically +V−2.8V d.c.) †	5mA	5mA	5mA

*Overvoltage and reverse polarity protected. If the meter is connected via a 200mA anti-surge fuse.

† Applies to 200mV and 2V F.S.D. versions only. 20V and 200V F.S.D. meters do not have these outputs.

Performance

	Meter F.S.D. 200mV	2V	20V	200V
Measurement range	±199.9mV	±1.999V	±19.99V	±199.9V
Accuracy	±0.1% ±1 count			
Resolution	100μV	1mV	10mV	100mV
Temperature coefficient typical	±75ppm/°C	±75ppm/°C	±150ppm/°C	±150ppm/°C
maximum	±150ppm/°C	±150ppm/°C	±350ppm/°C	±350ppm/°C
Input impedance	>100MΩ	>100MΩ	11.2MΩ±2%	10.11MΩ±2%
Input leakage current maximum	10pA	10pA		
Input over-voltage	±100V	±100V	±500V	±500V
Common mode rejection ratio (CMRR)	80 dB	80 dB		
Common mode voltage range (CMVR)	within +V−0.5 and −V+1V			
External reference range	within CMVR			
Sampling rate	approx. 3 per second			
Integration time	100ms			
Warm up time	within 10 minutes			
Storage temperature range	−25°C to +85°C			
Working temperature range	0°C to +50°C			

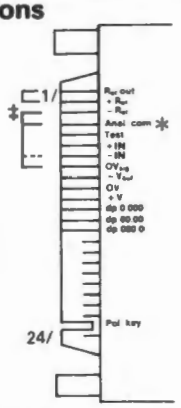
Display – all meters

Polarity: shown by minus sign.
Over-range: shown by the 3 least significant digits blanked.

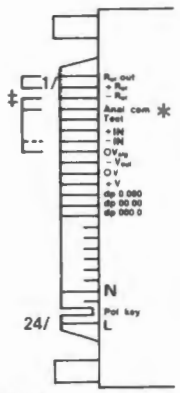
Decimal point: programmable by edge connector. To illuminate a decimal point connect appropriate pin to 0V.
Test facility: connect to +V to display all segments.

RS data

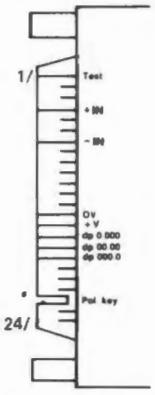
Connections



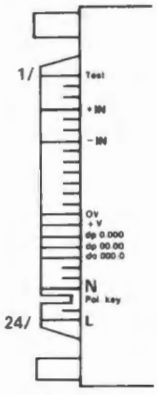
5V d.c. supply versions
200mV and 2V FSD only



110V/240V a.c. supply versions
200mV and 2V FSD only



5V d.c. supply versions
20V and 200V FSD only



110/240V a.c. supply versions
20V and 200V FSD only

‡ Standard connections for differential inputs; for single ended mode also connect −1N to 0V sig.

* In order to improve system linearity it may be necessary to let analogue common float with respect to the other inputs, ie left unconnected, any common mode voltage error thus introduced should be negligible.

Reference

All meters incorporate a highly stable band-gap derived reference which may be adjusted by means of the ten turn pot accessed through the hole in the display circuit board behind the filter. The 200mV and 2V meters may be used with either the internal reference or an external reference. Should the internal reference be used then the standard link connections shown above should be made. With the 20V and 200V meters the internal reference is internally connected and cannot be used with an external reference.

Calibration

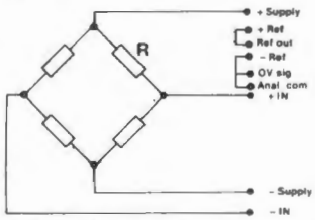
To calibrate the 200mV or 2V meter connect the standard links as shown above and adjust the reference to 100mV (200mV version) or 1.000V (2V version). The reference voltage is measured between the +ref and −ref terminals. Alternatively apply a known voltage to the input (e.g. 199.5mV) and adjust the reference to give the correct reading. The 20V and 200V meters can only be calibrated by applying a known voltage to the inputs and adjusting the reference for the correct reading.

Connections should be made via a 24 way 0.1 inch edge connector, RS466-545, and may be secured to the case by two self tapping screws supplied. (Type AB No. 4 × 12.7mm).

Applications

Bridge circuits – use 200mV or 2V meters

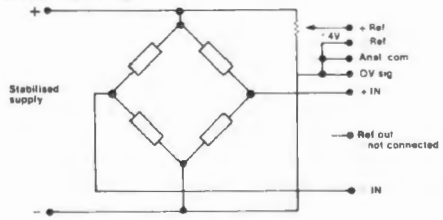
Simple bridge (for non-ratiometric measurements)



The supply to the bridge may be an externally stabilised voltage. Alternatively the analogue commom pin may be used to derive this voltage. In this case +Supply and Anal com. to –Supply (not 0V sig) with the following limitations.

$$I_R \frac{2.8V}{R} \leq 5mA$$

Ratiometric bridge



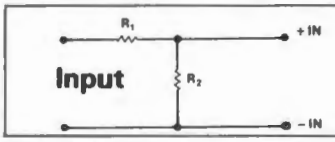
(May be ground referenced if required)

N.B. To avoid common mode errors in all the above circuits ensure that the voltage between − IN and Anal. com. (common mode voltage) does not exceed ±1V.

Attenuators

For applications requiring an f.s.d. greater than the meter's basic movement then the use of an external attenuator may be made. This simply requires two resistors connected as shown below.

The total value of R_1 and R_2 determine the loading on an external circuit connected to the input and should be chosen to reduce this loading to an acceptable level. However, if R_2 is too high then the input impedance of the meter will affect the accuracy. Normally the 200m V and 2V meters do not present a problem as the input impedance is greater than 100 MΩ. The 20V and 200V meters have a lower impedance, as given in the performance table, which may need to be accounted for in the attenuator value calculation.



attenuation ratio

$$= \frac{R_2}{R_1 + R_2}$$

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Telephone: 0536 201234
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RS data

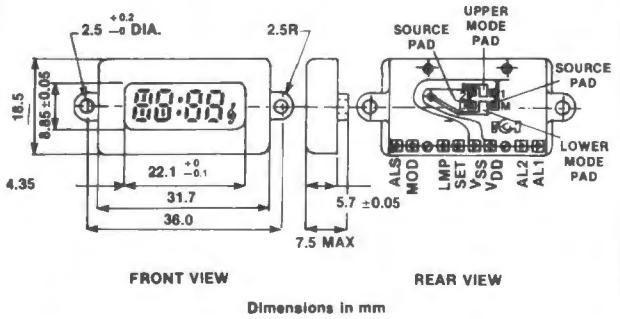
L.C.D. Clock module

Stock number 308–499

The L.C.D. Clock Module is a miniature L.C.D. Clock having 6 time keeping functions, 24 hour alarm output and 4 year calendar with Alpha-numeric day/date. 12 hour or 24 hour and month or date reversal is standard. The character height is 0.25 inches (6.4mm). There is an incandescent back light incorporated in the device.

Connections are made at the back of the module to 8 solder pads.
The unit is compact and the easy mounting design makes it suitable for many instrumentation, timing and general purpose clock applications. The calendar information makes the module particularly useful in monitoring environmental equipment etc.

Clock module dimensions



Electrical characteristics

Absolute maximum ratings

Operating voltage referenced to V_{SS} — +1.3V to +1.6V
Operating temperature — 5°C to 45°C
Storage temperature — −10°C to 60°C

Operating characteristics T_A = 25°C, V_{SS} = 0V

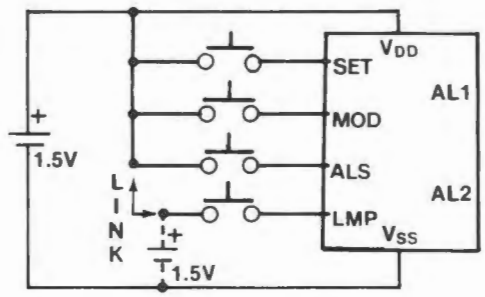
Parameter	Conditions	Min	Typ	Max	Units
Supply current Note (1)	V_{DD} = +1.5V		6		μA
Output current — AL1, AL2 Note (2)	V_{DD} = +1.3V		150		μA
Back light current	V_{DD} = +1.5V		12.5		mA
Crystal frequency			32.768		kHz
Accuracy			±2.5		min/year

Notes (1) With 32.768kHz crystal oscillating and clock not running. Supply current with alarm connected typically 13μA (see Application Circuits).

(2) The alarm signal is an interrupted audio tone. The tone is interrupted at a 1Hz rate with a 25% duty cycle.

External connections

For basic mode of operation



To maintain low current consumption 'LMP' can be powered from a separate battery, shown above by dotted lines after removal of the link. Suitable 'momentary' push to make switches and 1.5V batteries can be found in the current RS catalogue.

Operating mode connections

Operating Mode	Display Digit 1st 2nd : 3rd 4th	*Mode Pad	*Source Pad
European style	Days Months	Lower	D(V_{DD})
American style	Months Days	Lower	M(V_{SS})
24-hours format	Hours : Minutes	Upper	2(V_{DD})
12-hours format	Hours : Minutes	Upper	1(V_{SS})

* Solder appropriate mode and source pads together for desired operation.

Note: For the 12-hours Display Format an 'A' for AM or 'P' for PM appears in 4th digit when setting the hours.

Clock operation and setting

Indicates displays are flashing and settable inside this area

	DISPLAY	SEQUENTIAL SETTING INSTRUCTIONS SET	MOD	ALS	DESCRIPTION
DISPLAY—TIME	1:00	power on			time displayed in 12-hour format
	13 1:00				time displayed in 24-hour format
	13 1:00	press			time is clocking, 24-hour format
TIME SETTING	10:00	press 2nd	1st		set & update hours to desired time via "SET"
	10:25	press 2nd	1st		set & update minutes to desired time via"SET"
	10:25		press		set time is held at beginning of minute
	10:25	press			set time is clocking
CALENDER SETTING	10 8	press 2nd	1st		hold "MOD" about 3 sec until month and date appear then set & update months to desired date via "SET"
	10 1	press 2nd	1st		set & update days to desired date via "SET"
	SA	press 2nd	1st		set & update day-of-week to desired day via "SET"
	10:26		press		circuit returns to normal time display
DISPLAY— ALARM TIME	13 1:00 🔔			press once only	alarm time and " 🔔 " displayed momentarily then
	10:26				display returns to normal time, but alarm symbol is off
	13 1:00 🔔			press and hold on	alarm time and " 🔔 " displayed momentarily then display
	10:26 🔔				returns to normal time, but alarm symbol is on
ALARM TIME SETTING	10:00 🔔	press 2nd		press 1st	press "ALS" twice within 3 secs then set alarm hours to desired time via "SET"
	10:30 🔔	press 2nd		press 1st	set alarm minutes to desired time via "SET"
	10:30 🔔			press once only	circuit returns to normal time display with " 🔔 " to show
	10:27 🔔				alarm signal is on

Notes

Normally hours and minutes are displayed.

Momentarily pressing the "SET" button causes the month and date to appear for one (1) second, followed by the day-of-week for another second, then the display returns automatically to hours and minutes. If "SET" button is held on the display alternates between month and date (1 second) and day-of-week (1 second).

Seconds can be called up by pressing "SET" button twice momentarily within 2 seconds. The display will return to hours-minutes on another momentary press of "SET".

If the alarm circuit has been turned on, the alarm signal is activated when the alarm time matches the normally displayed time. The alarm signal is cut off automatically after 15 seconds, or the user may manually de-activate it by pressing "SET" or "ALS" button. When the alarm is de-activated by pressing and holding the "ALS" button, the alarm circuit and the "𝄞" will turn off.

In order to use the alarm again it must be re-enabled using "ALS" as per setting instructions above.

The incandescent backlighting lamp will be on when "LMP" is pressed. Lamp is designed for momentary contact only.

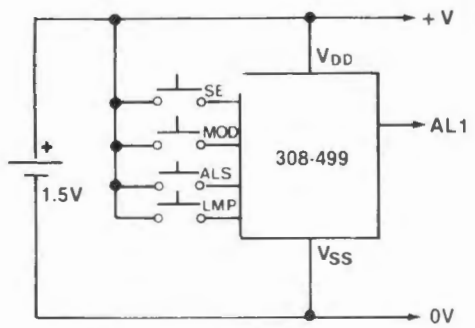
Days of the week display format are as follows:

SU MO TU WE TH FR SA

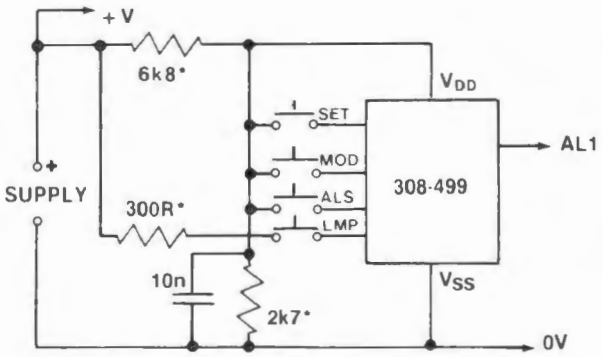
Momentary switches are recommended for all functions.

Applications circuits

1.5V Battery operation

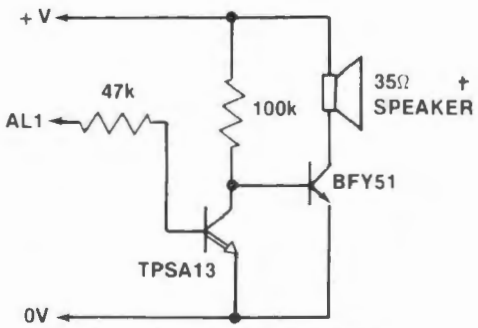


Power supply operation



* Values chosen for a 5V supply and must be altered with other voltages.

Alarm output



† May be replaced by P.C.B. Audible warning Device 249-794 provided supply voltage is between 3V and 15V.

Notes

'Alarm 1' (AL1) is a 'normally high' output which, when activated, gives an audio tone output of 1kHz interrupted at a 1Hz rate with a 25% duty cycle.

'Alarm 2' (AL2) is a 'normally high' output when activated gives a 1Hz signal with a 25% duty cycle.

RS data

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RS data

LED driver i.c.'s & bargraph modules

RS 3914 and RS 3915 i.c.'s are designed to drive 10 external LED's directly in response to an analogue voltage input. The RS 3914 has a linear relationship between the input voltage and number of LED's illuminated whilst the RS 3915 follows a logarithmic law where each LED represents a 3dB change in input voltage level.

3914 and 3915 Bargraph modules house the above i.c.'s in die form on a panel mounting pcb complete with an integral 10 element red LED display. Connections are brought out onto solder pads.

39169 Bargraph module houses an i.c. in die form on a panel mounting pcb with an integral 10 element LED display. The i.c. is designed to drive the LED's in response to an analogue input signal where each LED represents a common **VU** level. The three highest VU levels are represented by **red** LED's all other levels are represented by **green** LED's. Connections are brought out onto solder pads.

Features

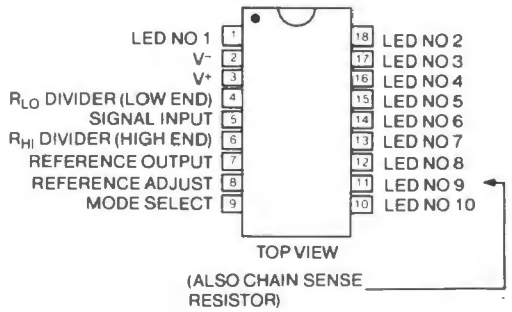
- Bar or dot display externally selectable
- Slow fade on bar or dot display (improves resolution)
- Internal voltage reference from 1.2 V to 12 V
- Operates with single supply of 3 V to 18 V
- Inputs operate down to ground
- LED drive current programmable from 2 to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35 V without damage or false outputs
- LED driver outputs are current regulated, open-collectors (i.c.'s only)
- Outputs can interface with TTL or C-MOS logic (i.c.'s only)

Absolute maximum ratings (notes 5 and 8)

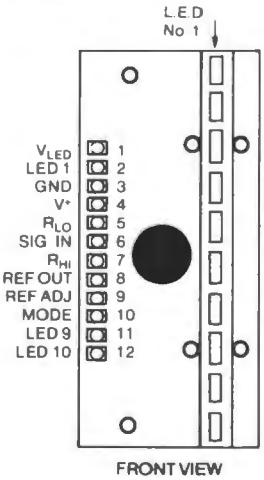
Power dissipation	RS 3914 i.c.	660 mW
	RS 3915 i.c.	625 mW
	3914 module (note 7)	500 mW
	3915 module (note 7)	500 mW
	39169 module (note 7)	500 mW
V^+ voltage	i.c.'s	25 V
	Modules	24 V
LED collector output voltage	i.c.'s only	25 V
	modules	24 V
Voltage on resistor string		−100 mV to V^+
Reference load current		10 mA
Signal input current (with overvoltage applied)		±3 mA
Signal input overvoltage (note 6)		±35 V
Operating temperature range		0°C to +70°C

Figure 1: **Pin connections**

RS 3914 and 3915 i.c.'s



3914, 3915 and 39169 modules



Electrical characteristics

RS 3914 and 3915 i.c. characteristics

Parameter	Conditions	RS 3914 i.c. Min.	RS 3914 i.c. Typ.	RS 3914 i.c. Max.	RS 3915 i.c. Min.	RS 3915 i.c. Typ.	RS 3915 i.c. Max.	Units
COMPARATORS								
Offset Buffer and First Comparator	R_{LO} and R_{HI} at 0V and 12V. (Note 2)		3	10		3	10	mV
Offset Buffer and Any Other Comparator	R_{LO} and R_{HI} at 0V and 12V (Note 2)		5	15		3	15	mV
Turn ON Voltage Change	10% to 90% of a 20mA LED Drive		2	6	—	—	—	mV
Input Bias Current (at Pin 5)			10	50		10	50	nA
Gain ($\Delta_{LED}/\Delta V_{IN}$)	I_{LREF} = 2mA, I_{LED} = 10mA	—	—	—	3	8		mA/mV
COMPARATOR–VOLTAGE–DIVIDER								
Divider Resistance	Total, Pin 6 to 4	6.5	10	15	15	22	30	kΩ
Divider Non-Linearity	Deviation from Straight Line through 1st and Last Threshold Points (Note 3)		0.5	2	—	—	—	%
Relative Accuracy (input change between any two Threshold Points)	(note 4)	—	—	—	2.0	3.0	4.0	dB
Absolute Accuracy at Each Threshold Point	(note 4)							
	V_{IN} = –3, –6dB	—	—	—	–0.5		+0.5	dB
	V_{IN} = –9dB	—	—	—	–0.5		+0.65	dB
	V_{IN} = –12, –15, –18dB	—	—	—	–0.5		+1.0	dB
	V_{IN} = –21, –24, –27dB	—	—	—	–0.5		+1.5	dB
VOLTAGE REFERENCE								
Load Regulations (ΔV_{REF})	I_{LREF} = 0.1mA to 4mA at V^+ = 5V and V_{LED} = 5V			2		0.4	2	%
Line Regulation	3V≤V^+≤18V		0.01	0.03		0.01	0.03	%/V
Output Voltage	1mA Load V^+ = 5V = V_{LED}	1.2	1.25	1.34	1.2	1.25	1.34	V
Output Voltage Change with Temperature	T_A = 0°C to +70°C I_{LREF} = 1mA, V^+ = 5V = V_{LED}		1			1		%
Adjust Pin Current			75	120		75	120	μA
LED CURRENT REGULATION								
LED Current	V^+ and V_{LED} = 5V, I_{LREF} = 1mA	7	10	13	7	10	13	mA
LED Current Difference (Between	V_{LED} = 5V, = I_{LED} = 2mA		0.12	0.4		0.12	0.4	mA
Largest and Smallest LED Currents)	V_{LED}, 5V, I_{LED} = 20mA		1.2	3		1.2	3	mA
Current Change with Supply	I_{LED} = 2mA 2V ≤ V^+_{LED} ≤ 17V		0.1	0.25		0.1	0.25	mA
Voltage (as Measured at LED Cathodes)	I_{LED} = 20mA 2V ≤ V^+_{LED} ≤ 17V		1	3		1	3	mA
Current Regulation – Dropout Voltage (at device pins)	I_{LED} = 20mA at V^+_{LED} = 5V Causing 10% I_{LED} Decrease			1.5			1.5	V
Output Saturation of LED Drive Collectors	I_{LED} = 1.6mA I_{LREF} = 0.32mA		0.25	0.4	—	—	—	V
Ditto	I_{LED} = 2.0mA, I_{LREF} = 0.4mA	—	—	—		0.15	0.4	V

RS 3914, 3915 and 39169 module characteristics

(Other electrical characteristics not stated here are as per the respective i.c. characteristic) (see notes 7 and 9)

Parameter		Conditions	Min.	Typ.	Max.	Units
LED Segment Intensity		V^+ = 12.0V, V_{LED} = 4.5V IL_{REF} = 1.0mA	0.10	0.20		mcd
LED Intensity Matching (All Segments On)		V_{IN} ≥ 10V.V^+ = 12.0V. V_{LED} = 3.0V IL_{REF} = 1.0mA		±33		%
LED Current/Segment		V^+ = 12.0V, V_{LED} = 4.5V IL_{REF} = 1.0mA		10		mA
Peak Wavelength	Red LED			660		nm
	Green LED			565		nm
Voltage Reference Output		0.10mA ≤ IL_{REF} ≤ 4.0mA V^+ = 12.0V, V_{LED} = 4.5V	1.2	1.25	1.34	V
Signal Input Bias Current				10	100	nA
Supply Current (V^+ Lead)		V^+ = 5V to 20V IL_{REF} = 1.0mA		6	10	mA
Absolute Accuracy at Each Threshold Point	3914 module	Deviation from Straight Line through First and Last Threshold Point (Note 3)	–5		5	%
	3915 module	V_{IN} = –3 to –18dB (Note 4)	–1		1.5	dB
		V_{IN} = –21 to –27dB (Note 4)	–2		2	dB
	39169 module	V_{IN} = +3 to –7dB (Note 4)	–1		1.5	dB
		V_{IN} = –10 to –20dB (Note 4)	–2		2	dB

Comparator threshold switching voltages

RS3914 i.c. and module (see note 4)

	VOLTS		
LED output	**Min**	**Typ**	**Max**
1	0.980	1	1.020
2	1.960	2	2.040
3	2.940	3	3.060
4	3.920	4	4.080
5	4.900	5	5.100
6	5.880	6	6.120
7	6.860	7	7.140
8	7.840	8	8.160
9	8.820	9	9.180
10	9.800	10	10.200

RS3915 i.c. and module (see note 4)

		VOLTS		
LED output	**dB**	**Min**	**Typ**	**Max**
1	−27	0.422	0.447	0.531
2	−24	0.596	0.631	0.750
3	−21	0.841	0.891	1.059
4	−18	1.189	1.259	1.413
5	−15	1.679	1.778	1.995
6	−12	2.372	2.512	2.819
7	−9	3.350	3.548	3.825
8	−6	4.732	5.012	5.309
9	−3	6.683	7.079	7.498
10	0	9.985	10	10.015

39169 module (see note 4)

		VOLTS		
LED output	**dB**	**Min**	**Typ**	**Max**
1	−20±1	0.631	0.708	0.794
2	−10±1	1.995	2.239	2.512
3	−7±1	2.818	3.162	3.548
4	−5±½	3.548	3.981	4.467
5	−3±½	4.732	5.012	5.309
6	−1±½	5.957	6.310	6.683
7	0±¼	6.879	7.079	7.286
8	1±¼	7.718	7.943	8.175
9	2±¼	8.660	8.913	9.173
10	3±¼	9.985	10.000	10.015

Typical resistor string values
(See Figs. 2 and 3)

Resistor	NSM3914	NSM3915	NSM3916
R1	1.00 k	1.0 k	0.708 k
R2	1.00 k	0.41 k	1.531 k
R3	1.00 k	0.59 k	0.923 k
R4	1.00 k	0.83 k	0.819 k
R5	1.00 k	1.17 k	1.031 k
R6	1.00 k	1.66 k	1.298 k
R7	1.00 k	2.34 k	0.769 k
R8	1.00 k	3.31 k	0.864 k
R9	1.00 k	4.69 k	0.970 k
R10	1.00 k	6.63 k	1.087 k
Total	10 k	22.6 k	10 k

Notes:

1. Unless otherwise stated, all characteristics apply with the following conditions to RS3914 and RS3915 i.c.'s

$T_A = 25°C$	$-0.15V \leq R_{LO} \leq 12V_{DC}$
$I_{L(REF)} = 0.2$ mA (For higher power conditions, pulse testing is used)	$0V \leq V_{IN} \leq (V^+ - 1.5V)$
	$V_{REF}, V_{RHI}, V_{RLO} \leq (V^+ - 1.5V)$
	$3V_{DC} \leq V^+ \leq 18V_{DC}$ (RS3914)
Pin 9 connected to pin 3 (bar mode)	$3V_{DC} \leq V^+ \leq 20V_{DC}$ (RS3915)
	$3V_{DC} \leq V_{LED} \leq V^+$
	$-0.015 \leq V_{RHI} \leq 12V_{DC}$

2. RS3914 and RS3915 comparator threshold is measured when the first 1 mA flows in the associated LED output pin. When measuring 'overlap' an LED is considered to be extinguishing when its current falls below 1 mA.

3. RS3914 i.c. and module divider non-linearity is measured with R_{LO} at 0.000 V, and R_{HI} at 10.000 V_{DC}. (At lower divider voltages, buffer and comparator offset voltages add significant error.)

4. RS3915 i.c. and module accuracy is measured referred to 0 dB = + 10.000 V_{DC} at signal input, with + 10.000 V_{DC} at R_{HI}, and 0.000 V_{DC} at R_{LO}. (At lower full scale voltages, buffer and comparator offset voltage may add significant error.) See table for threshold voltages.

5. For RS3914 and 3915 i.c.'s only. Although the following situations will not lead to circuit damage, they can result in *incorrect operation:* (a) LED No. 9 (pin 11) collector voltage exceeding V^+ voltage on pin 3, or becoming more than 14 V below applied V^+, (additionally being limited to less than 200 mV below V^-); (b) signal and comparator voltage-divider becoming higher than the limits of note 1, above: (c) reference load capacitance above 47 nF; (d) reference current loading above 5 mA.

6. The addition of a 39 k resistor in series with pin 5 allows ± 100 V signals without damage.

7. Unless otherwise stated these values apply with the following conditions, V^+ (supply) 3 V to 20 V. Input signal range 0.015 V to V^+ −1.5 V with a maximum of 12 V_{DC}. (Comparator divider voltages, same limits.) T_A = 25°C. Reference load current, 80 μA minimum.

8. For RS3914, 3915 and 39169 modules only. Driver dissipation is given by $P_{DR} = (V_{LED} - 1.7V)$ I_{LED} (Total) + ($V^+ \times$ 10 mA), where V_{LED} is the LED supply voltage. 1.7 V is the nominal individual LED voltage drop, and 10 mA is the maximum current of the V^+ supply.

9. The following situations can lead to incorrect operation (a) V_{LED} exceeding V^+ or more than 14 V below V^+; (b) signal and comparator voltage divider becoming higher than the limits of note 8; (c) reference load capacitance above 47 nF; (d) reference current loading above 5 mA.

Functional description

The block diagrams in Figs. 2 and 3 illustrate the simplest circuit configuration for the modules and i.c.'s respectively.

A positive signal applied to the signal input pin is fed to a high input-impedance buffer. The buffer output signal is presented to a series of 10 comparators, each of which is biased to a different threshold voltage level by the resistor divider network R_1 to R_{10}.

Figure 2: **Block diagram of RS 3914, 3915 and 39169 modules**

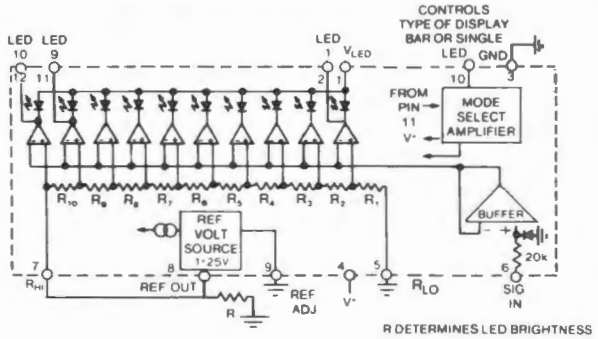
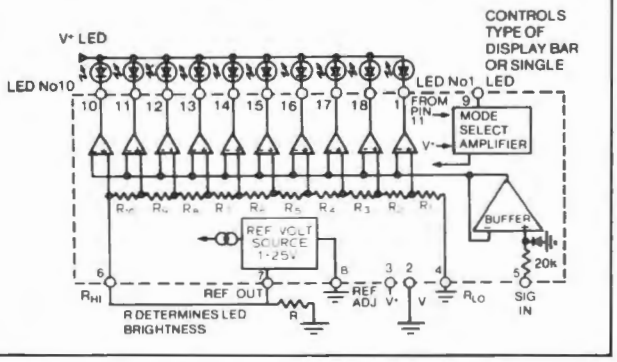


Figure 3: **Block diagram of RS 3914 and RS 3915 i.c.'s**



Resistor divider network

In the block diagrams the high end R_{HI} of the resistor string is connected to the internal 1.25V reference voltage. In the case of the RS 3914, for each 125mV that the input signal increases, a comparator will switch on another indicating LED, similarly for the nonlinear RS 3915 and RS 39169 this resistor divider network can be connected between any 2 voltages, providing that they are 1.5V below V+ and no less than V−.

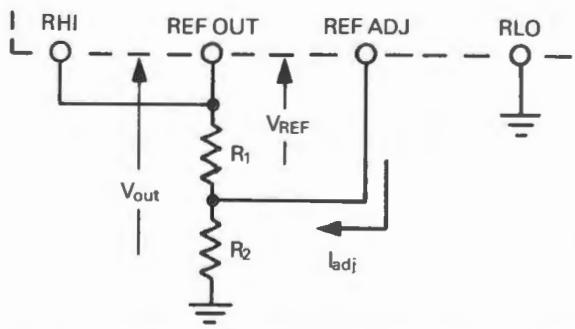
Internal voltage reference

The internal voltage reference may be used to impress a fixed voltage across the resistor divider network.

The reference is designed to be adjustable and develops a nominal 1.25V between REF OUT and REF ADJ. The reference voltage V_{ref} is impressed across programme resistor R_1 and since the voltage is constant, a constant current then flows through the outputs set resistor R_2 giving an output voltage of:

$$V_{OUT} = V_{ref}(1 + R_2/R_1) + I_{adj}R_2$$

Figure 4: **Internal voltage reference**



The 120μA current (max) I_{adj} from the reference adjust pin represents an error term, the reference was designed to minimise changes of this current with V+ and load changes. For correct operation, reference load current should be between 80μA and 5mA. (Load capacitance should be less than 47nF.)

Current programming

A feature not completely illustrated by the schematic diagram is the LED brightness control. The current drawn out of the reference output determines the LED current. Approximately ten times this current will be drawn through each illuminated LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the external current and voltage setting divider, as well as the internal 10-step resistor network, should be included in calculating the LED drive current.

Mode selection

The mode select input pin is used to control the bar and dot modes of operation. It is also employed in display control of multiple chaining of i.c.'s and modules.

Baragraph display

Wire Mode select pin directly to V+ pin. (The bargraph display is selected if Mode Select pin is within 20mV of V+).

Dot display

Leave the mode select pin open circuit.

Dot display, 20 or more LED's

Connect Mode Select pin of the first driver in the series (i.e. the one with the lowest input voltage comparison points) to LED no. 1 of the next highest i.c. or module. Continue connecting the Mode Select pin of the lower input drivers to LED no. 1 of the next highest drivers for 30, 40 or more LED displays. The last bar driver in the chain may have the Mode Select pin connected to pin 11, or left open circuit. All previous drivers should have a 20kΩ resistor in parallel with LED no. 9.

In order for the display to make sense when multiple devices are cascaded in dot mode, special circuitry has been included to shut off LED no. 10 of the first device when LED no. 1 of the second device comes on. The connection for cascading in dot mode is depicted in Fig 8. (shown for 3915 i.c. and module).

As long as the input signal voltage is below the threshold of the second driver i.c. LED no. 11 is off. The Mode Select pin of driver no. 1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED no. 11, the Mode Select pin of driver no. 1 is depressed by one LED voltage drop (1.5V or more) below V_{LED}. This condition is sensed by a comparator referenced 600mV below V_{LED}. This forces the output low, which shuts off the output transistor, extinguishing LED no. 10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100μA) that is diverted from LED no. 9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100μA flowing through LED no. 11 even if the input voltage rises high enough to extinguish the LED. This ensures that the Mode Select pin of driver no. 1 is held low enough to force LED no. 10 off when any higher LED is illuminated. While 100μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LED's in a dark environment. If this is bothersome, the simple cure is to shunt LED no. 11 with a 10k resistor. The 1V drop is more than the 900mV worst case required to hold off LED no.10 yet small enough that LED no. 11 does not conduct significantly.

Application notes

Three of the most commonly needed precautions when using the Dot/Bar driver i.c.'s are shown in the first application drawing (see Fig. 5) showing a 0V to 5V bargraph meter. The most difficult problem occurs when large LED currents are being drawn, especially in bargraph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from the signal source, reference ground and bottom of the resistor string (as illustrated) to a single point close to V^- or GND pin is the best solution.

Long wires from the LED supply to the LED anode common rail (3914 and 3915 i.c.'s) or V_{LED} (3914, 3915 and 39169 modules) can cause oscillations. Depending on the severity of the problem a 47n to 2μ2 decoupling capacitor from the LED anode rail to V^- or GND will damp the circuit.

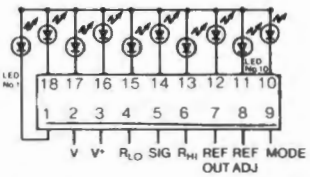
If LED turn-on seems slow (bar mode) or several LED's light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and by-passing fail to stop oscillations, the V^+ voltage is usually below suggested limits (see note 2, Fig. 5). Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be by-passed to V^- or GND with at least a 1n capacitor, or up to 100n in noisy environments.

Power dissipation, especially in the bar mode should be given consideration. For example, with a 5V supply and all LED's programmed to 20mA, the driver will dissipate more than maximum power rating of both devices. In this case a 7R5 resistor in series with the LED supply will cut device heating by half. The negative end of the resistor should be by-passed to V^- or GND by a 2μ2 solid tantalum capacitor.

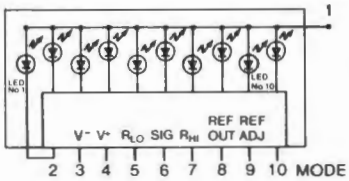
Typical applications

Explanatory note for Figs. 5 to 8

i.c. pin connections in red

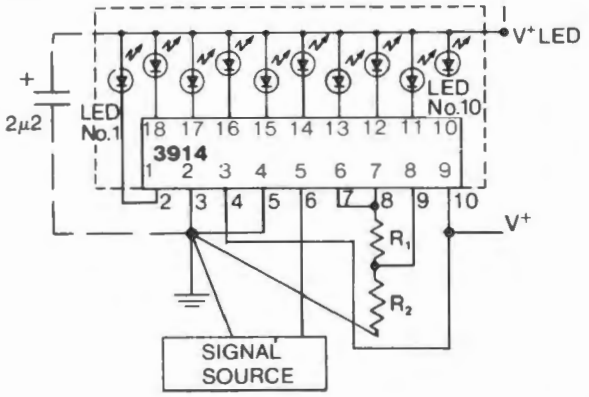


Module pin connections in black



RS 3914 i.c. and module

Figure 5: **0V to 5V bargraph meter**



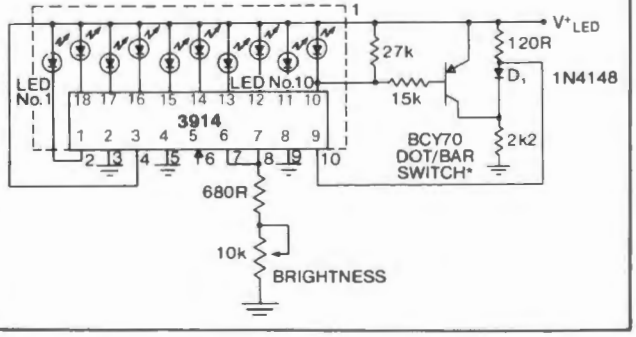
Note 1: Grounding method is typical of *all* uses. The 2μ2 capacitor is needed if leads to the LED supply are 150mm or longer.

Note 2: Supply voltage V^+ is recomended to be 1.8V above high signal input and 1.5V above V_{Out} for correct operation at 25°C.

$$V_{Out} = 1.25 \left[1 + \frac{R_2}{R_1}\right]$$

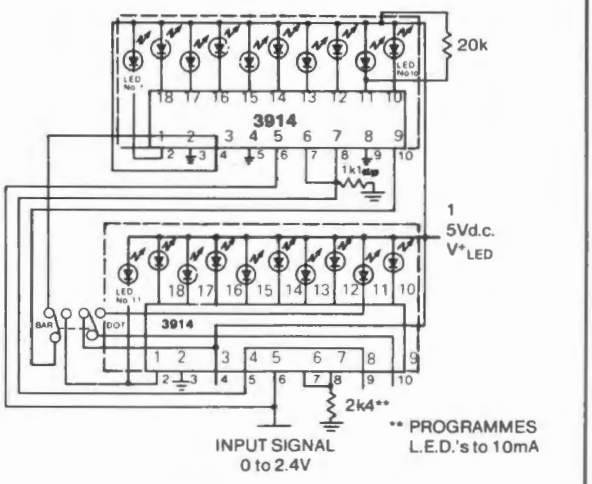
$$I_{LED} \approx \frac{12.5}{R_1}$$

Figure 6: **Indicator and alarm, full scale changes from dot to bar**



*The input to the Dot/Bar switch may be taken from cathodes of other LED's (LED nos. 1, 9 or 10 only on module). Display will change to bar as soon as the LED so selected begins to light.

Figure 7: **Segment meter with mode switch**



The exact wiring arrangement of this schematic shows the need for Mode Select pin to sense the V+ voltage exactly as it appears on V+ pin.

RS 3915 i.c. and module

The device, used in the circuits described previously could be directly substituted by the 3915 i.c. or module to give dB meter indication.

The following circuits are specifically intended for the 3915 type parts.

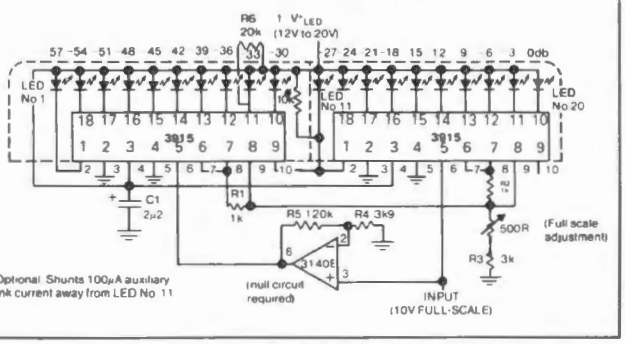
In order to display signals of 60 or 90 dB dynamic range multiple devices can be cascaded.

One approach would be to set the reference voltage of the two drivers 30 dB apart. The disadvantage of this method is that in many applications the threshold level of LED no. 1 could be comparable to the offset voltage of the driver, hence poor accuracy on the lower scale range would result.

A better approach shown in Fig. 8 is to keep the reference at 10 V for both devices and amplify the input signal to the lower device by 30 dB. Since two 2% resistors can set the amplifier gain within 0.35 dB, a gain trim is unnecessary. However, an op amp offset voltage of 5 mV will shift the first LED threshold as much as 4 dB, so that an offset trim may be required. Alternatively, instead of amplifying, input signals of sufficient amplitude can be fed directly to the first i.c. or module and *attenuated* by 30 dB to drive the second device.

To extend this approach to get a 90 dB display, another 30 dB amplification must be placed in the signal path, ahead of the lowest part. Extreme care is required as the lowest driver displays input signals down to 0.5 mV. Several offset nulls may be required. High currents should not share the same path as the low level signal. Also power line wiring should be kept away from signal lines.

Figure 8: **60 dB dot mode display**

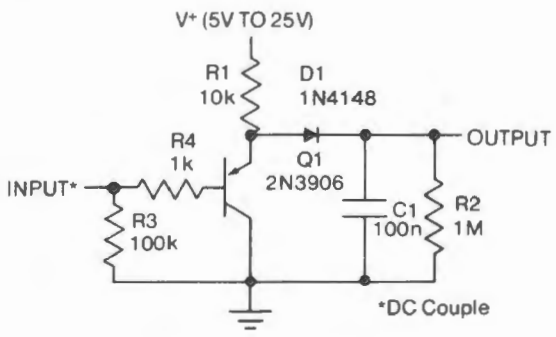


a.c. signal inputs

The simplest way to display an a.c. signal using the 3915 i.c. or module is to apply it directly to the signal input pin unrectified. Since the LED illuminated represents the instantaneous value of the a.c. waveform, one can readily discern both peak and average values of audio signals in this manner. The device will respond to positive half-cycles only but will not be damaged by signals up to ±35 V or up to ±100 V, (if a 39 k resistor is in series with the input). It is recommended to use dot mode and to run the LED's at 30 mA for high enough average intensity.

True average or peak detection requires rectification. If an i.c. or module is set up with 10 V full scale across its voltage divider, the turn-on point for the first LED is only 450 mV. A simple silicon diode rectifier will not work well at the low end due to the 600 mV diode threshold. The half-wave peak detector in Fig. 9 uses a PNP emitter-follower in front of the diode. Now, the transistor's base-emitter voltage cancels out the diode offset, within about 100 mV. This approach is usually satisfactory when a single device is used for a 30 dB display.

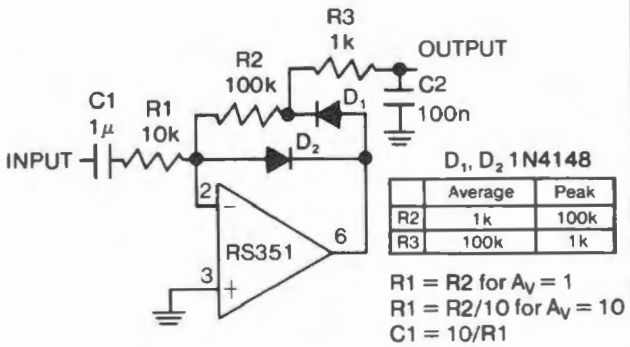
Figure 9: **Half-wave peak detector**



Display circuits using two or more i.c.'s or modules for a dynamic range of 60 dB or greater require more accurate detection. In the precision half-wave rectifier of Fig. 10 the effective diode offset is reduced by a factor equal to the open-loop gain of the op amp. Filter capacitor C2 charges through R3 and discharges through R2 and R3, so that appropriate selection of these values results in either a peak or an average detector. The circuit has a gain equal to R2/R1.

It is best to capacitively couple the input. Audio sources frequently have a small d.c. offset that can cause significant error at the low end of the log display. Op amps that slew quickly, such as the RS 351, or RS 353, are needed to faithfully respond to sudden transients. It may be necessary to trim out the op amp d.c. offset voltage to accurately cover a 60 dB range. Best results are obtained if the circuit is adjusted for the correct output when a low-level a.c. signal (10 to 20 mV) is applied, rather than adjusting for zero output with zero input.

Figure 10: **Precision half-wave rectifier**



For precision full-wave averaging use the circuit in Fig. 11. Using 2% resistors for R1 through R4, gain for positive and negative signal differs by only 1 dB worst case. Substituting 5% resistors increases this to 2 dB worst case. (A 2dB gain difference means that the display may have a ±1dB error when the input is a non-symmetrical transient.) The averaging time constant is R5-C2. A simple modification results in the precision full-wave peak detector of Fig. 12. Since the filter capacitor is not buffered, this circuit can drive only high impedance loads such as the input of a 3915 i.c. or module.

Figure 11: **Precision full-wave average detector**

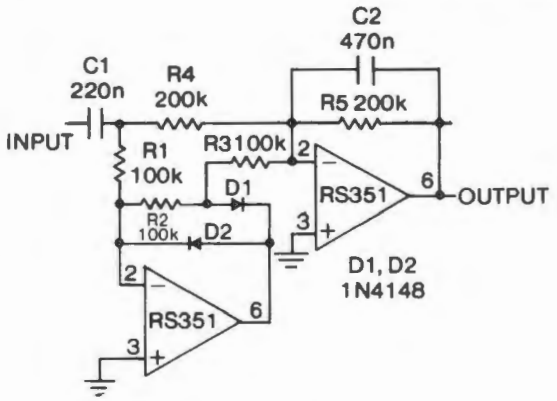


Figure 12: **Precision full-wave peak detector**

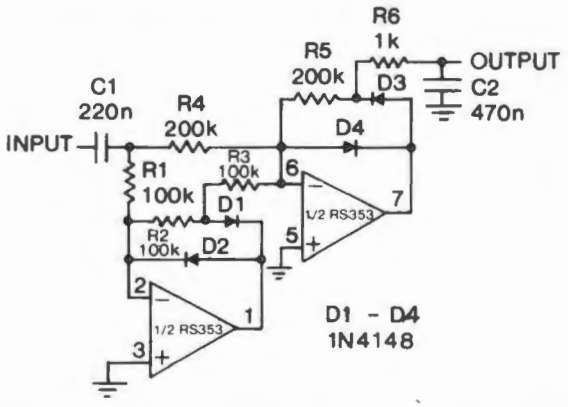


Figure 13: **Audio power meter**

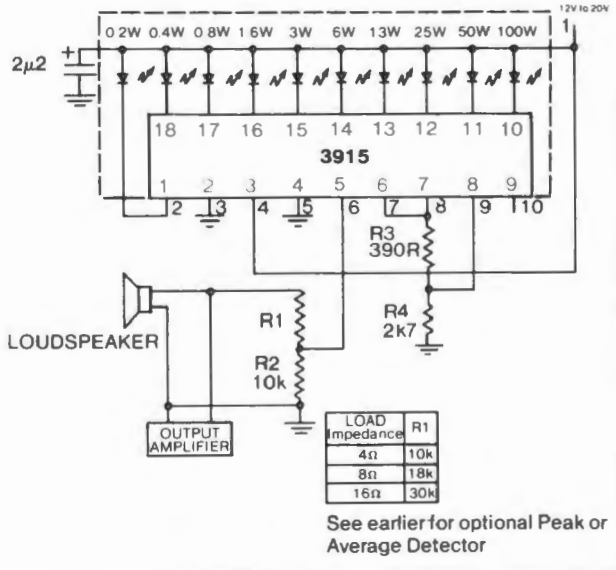


Fig. 13 shows an audio power meter employing either the RS 3915 i.c. or module suitable for power measurement from 0.2 W to 100 W for speaker loads of 4, 8 or 16 Ω.

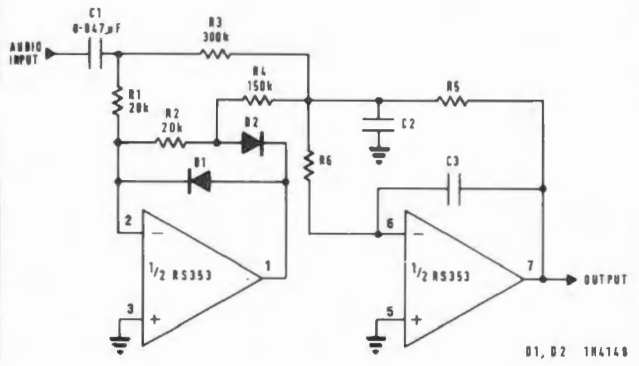
RS data

39169 module

This module is used in audio applications providing a VU or peak program meter display.

The audio level meter most frequently encountered is the **VU meter**. Its characteristics are defined in the ANSI specification C165.

Figure 14: **Full-wave average detector to VU meter specification***



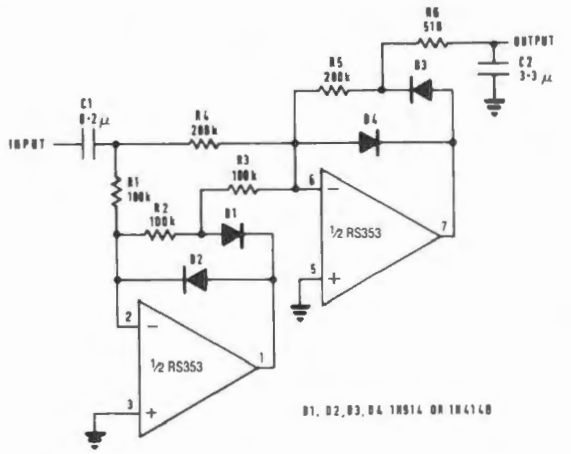
Gain	R5	R6	C2	C3
1	100 k	43 k	2.0	0.56 pF
10	1 M	100 k	1.0	0.056 μF

*Reaches 99% level at 300 ms after applied tone burst and overshoots 1.2%.

The 39169 module outputs correspond to the meter indications specified with the omission of the −2 VU indication. The VU scale divisions differ slightly from a linear scale in order to obtain whole numbers in dB.

Some of the most important specifications for an a.c. meter are its dynamic characteristics. These define how the meter responds to transients and how fast the reading decays. The VU meter is a relatively slow full-wave averaging type, specified to reach 99% deflection in 300 ms and overshoot by 1 to 1.5%. In engineering terms this means a slightly underdamped second order response with a resonant frequency of 2.1Hz and a Q of 0.62 Fig. 14 depicts a simple rectifier/filter circuit that meets these criteria.

Figure 15: **Precision full-wave peak detector**



D1, D2, D3, D4: 1N914 or 1N4148

Attack and decay time to DIN PPM specification. Response down 1 dB for 10 ms tone burst. Decays 20 dB in 1.5 s.

The VU meter, originally intended for signals sent via telephone lines, has shortcomings when used in high fidelity systems. Due to its slow response time, a VU meter will not accurately display transients that can saturate a magnetic tape or drive an amplifier into clipping. The fast-attack **peak program meter** (PPM) which does not have this problem is becoming increasingly popular.

Rather than respond instantaneously to peak, however, PPM specification require a finite 'integration time' so that only peaks wide enough to be audible are displayed. DIN 45406 calls for a response of 1 dB down from steady-state for a 10 ms tone burst and 4 dB down for a 3 ms tone burst. These requirements are consistent with the other frequently encountered specification of 2 dB down for a 5 ms burst and are met by an attack time constant of 1.7 ms.

The specified return time of 1.5 s to −20 dB requires a 650 ms decay time constant. The full-wave peak detector of Fig. 15 satisfies both the attack and decay time criteria.

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RS data

Hybrid r.f. amplifiers

Stock numbers 308-556 and 302-485

Introduction

Two hybrid thick film r.f. amplifiers designed for use in mast-head booster amplifiers, as pre-amplifiers in MATV systems and as general purpose amplifiers for v.h.f. and u.h.f. applications.

The RS OM335 operates from 24 V d.c. and the RS OM361 from 12 V d.c.; however, both amplifiers may be run at reduced supply voltage, the main consequence being a reduction in gain. For example at 12 V the RS OM335 provides a typical gain of 23 dB compared to 27 dB at 24 V d.c. and the output voltage falls from a minimum of 98 dBμV to 92 dBμV. The flatness of the frequency response is little affected and there is no change in noise figure down to a supply voltage of 12 V.

The output voltage is quoted in dBμV, i.e. dB with respect to 1μV. As an aid a conversion table is shown below which shows the output available in mV and in dBm; which is the output with respect to 1 mW into a 75 Ω impedance.

Extended frequency range performance

The recommended frequency range of these amplifiers is 40 to 860 MHz, however, the upper and lower limits can be extended with some reduction in transducer gain to provide 10 MHz to 1.4 GHz coverage. The table below illustrates the performance over the extended range, for the RS OM335.

Conversion table for 75 ohm impedance

dBμV	mV	dBm
90	31,6	−18,75
92	39.8	−16,75
94	50,1	−14,75
96	63,1	−12,75
98	79,4	−10,75
100	100,0	−8,75
102	125,9	−6,75
104	158,5	−4,75
106	199,5	−2,75
108	251,2	−0,75
110	361,2	1,25
112	398,1	3,25
114	501,2	5,25
116	631,0	7,25

Frequency (MHz)	Gain (dB)
10	22,5
20	25,2
30	26,0
40	26,2
50	26,3
800	25,6
1000	27,5
1200	20,5
1300	16,3
1400	13,2

RS OM335
Electrical characteristics

Ratings: Limiting values in accordance with the Absolute Maximum System (IEC 134)

Operating ambient temperature	T_{amb}		−20 to +70°C
Storage temperature	T_{stg}		−40 to +125°C
d.c. supply voltage	V_B	max.	28 V
Peak voltages on pins 1 and 7	V_{1M} , V_{7M}	max.	28 V
	$-V_{1M}$, $-V_{7M}$	max.	10 V
Peak incident powers on pins 1 and 7	P_{i1M} , P_{i7M}	max.	100 mW

Characteristics:

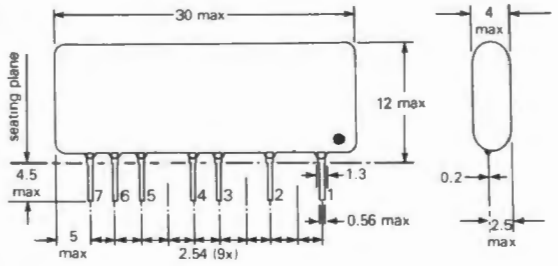
Measuring conditions			
Ambient temperature	T_{amb}	=	25°C
d.c. supply voltage	V_B	=	24 V
Source impedance and load impedance	R_s , R_l	=	75 Ω
Characteristic impedance of h.f. connections	Z_0	=	75 Ω
Frequency range	f	=	40 to 860 MHz

Performance

Supply current	I_B	typ.	35 mA
Transducer gain	$G_{tr} = \lvert s_f \rvert^2$	typ.	23 to 32 dB
		typ.	27 dB
Flatness of frequency response	$\pm\Delta \lvert s_f \rvert^2$	typ.	1,6 dB
Individual maximum v.s.w.r.			
input	$VSWR_{(i)}$	typ.	1,9 (1)
output	$VSWR_{(o)}$	typ.	3, 2 (1)
Back attenuation			
f = 100 MHz	$\lvert s_r \rvert^2$	typ.	46 dB
f = 860 MHz	$\lvert s_r \rvert^2$	typ.	40 dB
Output voltage			
at −60 dB intermodulation distortion		>	98 dBμV
(DIN 45004, par. 6.3: 3-tone)	$V_{o(rms)}$	typ.	101 dBμV
1 dB compression		typ.	115 dBμV (2)
Noise figure	F	typ.	5,5 dB

s-parameters: $s_f = s_{21}$ $s_i = s_{11}$ $s_r = s_{12}$ $s_o = s_{22}$

(1) Highest value, for a sample, occurring in the frequency range.
(2) Measured at saturation for 1 dB gain compression.



Terminal connections

1	= Input
2, 3, 5, 6	= Common
4	= Supply (+)
7	= Output

Package – Phenoformaldehyde based resin

Soldering recommendations
Hand soldering
Maximum contact time for a soldering-iron temperature of 260°C up to seating plane is 5 s

Figure 1: **Circuit diagram of the RS OM335**

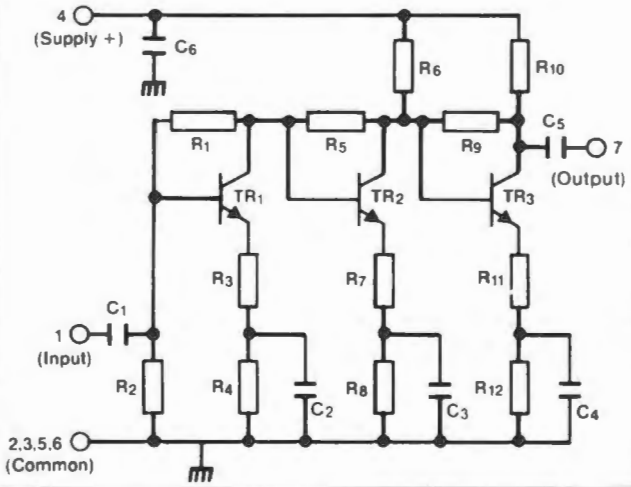


Figure 2: **Mounting recommendations**

The module must be mounted on double-sided printed-circuit board, see the example shown below. Input and output should be connected to 75Ω tracks. The connections to the 'common' pins should be as close to the seating plane as possible and soldered on both sides of the board.

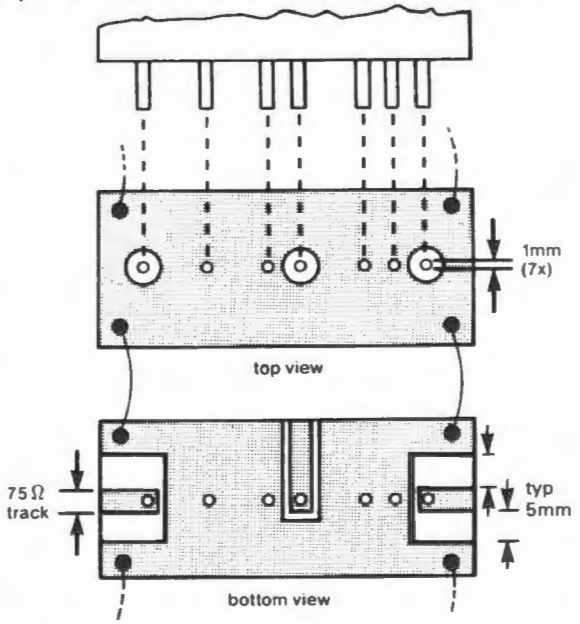


Figure 3: **Frequency response**

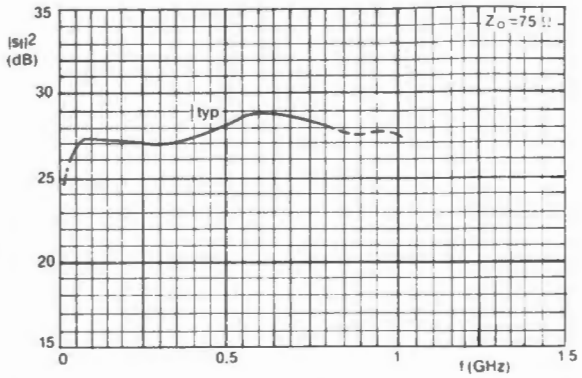


Figure 4: **Input impedance derived from input reflection coefficient s_i, co-ordinates in ohm × 75.**

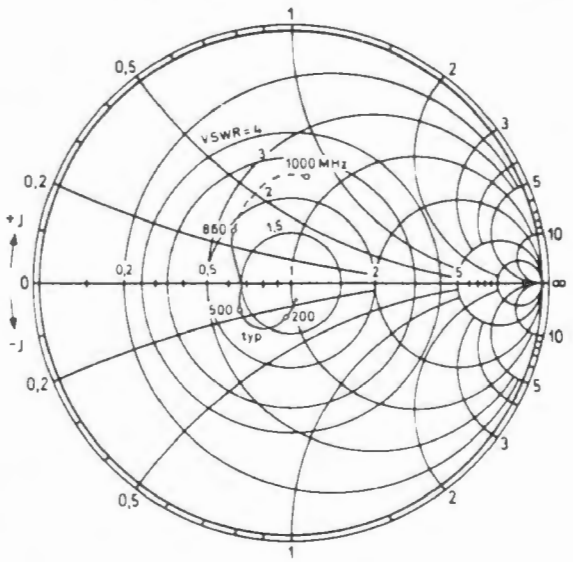
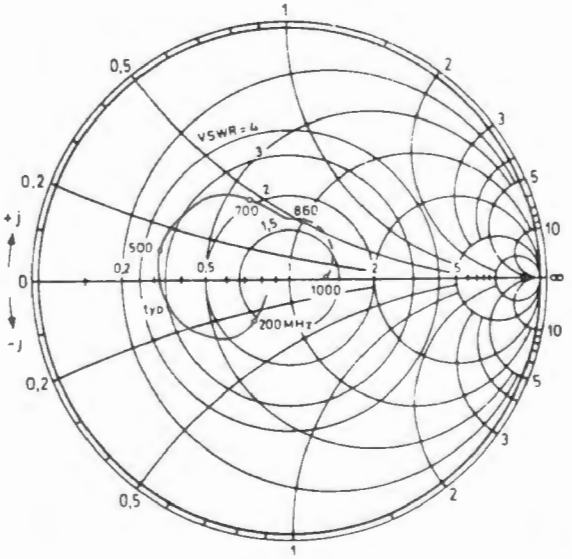


Figure 5: **Output impedance derived from output reflection coefficient s_o, co-ordinates in ohm × 75.**



RS OM361
Electrical characteristics

Ratings: Limiting values in accordance with the Absolute Maximum System (IEC 134)

Operating ambient temperature	T_{amb}		−20 to +70°C
Storage temperature	T_{stg}		−40 to +125°C
d.c. supply voltage	V_B	max.	15 V
Peak incident powers on pins 1 and 8	P_{I1M} , P_{I8M}	max.	100 mW

Characteristics:

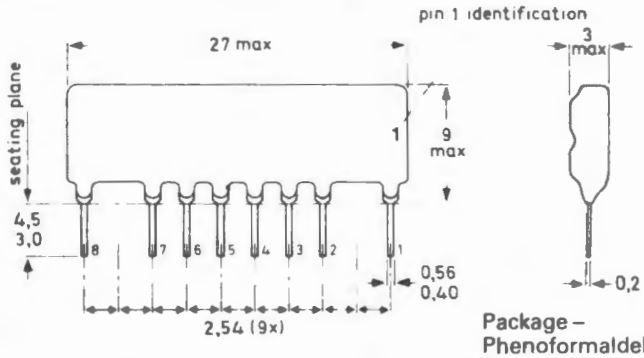
Measuring conditions

Ambient temperature	T_{amb}	=	25°C
d.c. supply voltage	V_B	=	12 V
Source impedance and load impedance	R_s , R_l	=	75 Ω
Characteristic impedance of h.f. connections	Z_0	=	75 Ω
Frequency range	f	=	40 to 860 MHz

Performance

Supply current	I_B	typ.	50 mA
Transducer gain	$G_{tr} = \|s_f\|^2$	typ.	28 dB 26 to 31 dB
Flatness of frequency response	$\pm\Delta\|s_f\|^2$	typ.	1 dB
Individual maximum v.s.w.r.			
input	$VSWR_{(i)}$	typ.	1,5
output	$VSWR_{(o)}$	typ.	1,7
Back attenuation			
f = 100 MHz	$\|s_r\|^2$	typ.	45 dB
f = 860 MHz	$\|s_r\|^2$	typ.	35 dB
Output voltage at −60 dB intermodulation distortion (DIN 45004, par. 6.3 : 3-tone)	$V_{o(rms)}$	> typ.	105 dBμV 107 dBμV
Noise figure	F	typ.	6 dB

s-parameters: $s_f = s_{21}$ $s_i = s_{11}$ $s_r = s_{12}$ $s_o = s_{22}$



Package – Phenoformaldehyde based resin

Terminal connections
1 = input
2, 3, 5, 6, 7 = common
4 = supply (+)
8 = output/supply (+)

Soldering recommendations
Hand soldering
Maximum contact time for a soldering-iron temperature of 260°C up to the seating plane is 5 s.

Figure 6: **Circuit diagram of the RS OM361**

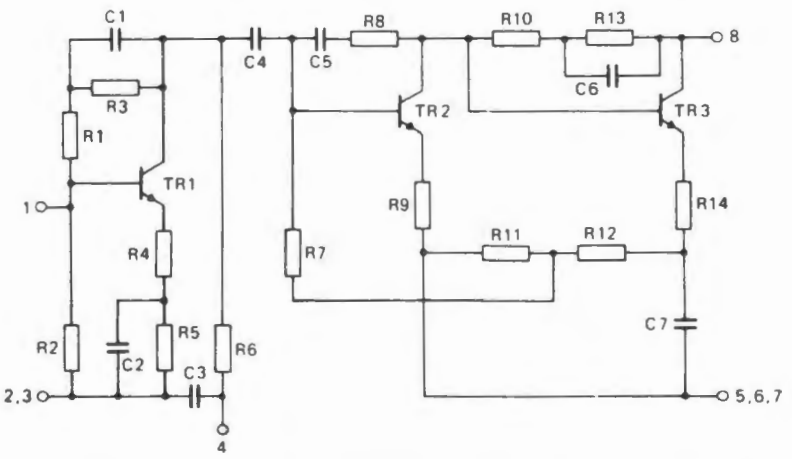
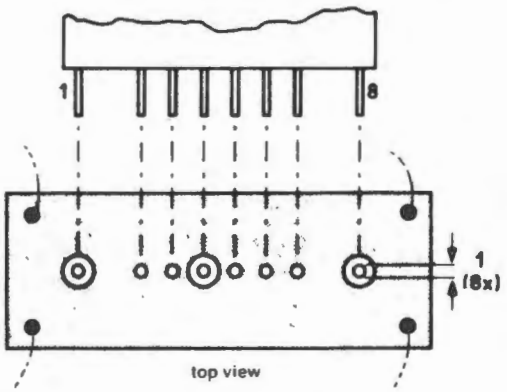


Figure 7: **Mounting recommendations**

The module must be mounted on double-sided printed-circuit board, see the example shown below.
Input and output should be connected to 75Ω tracks.
The connections to the 'common' pins should be as close to the seating plane as possible and soldered on both sides of the board.



Note: L > 5 μH; C > 220 pF ceramic capacitor. All components must be suitable for use in the frequency range 40 to 860MHz.

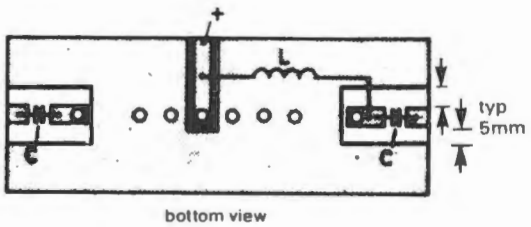


Figure 8: **Frequency response**

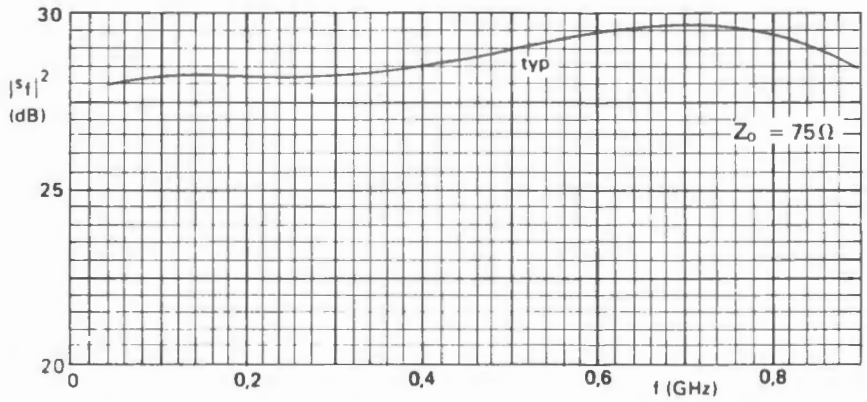


Figure 9: **Input impedance derived from input reflection coefficient s_i, co-ordinates in ohm × 75; typical values.**

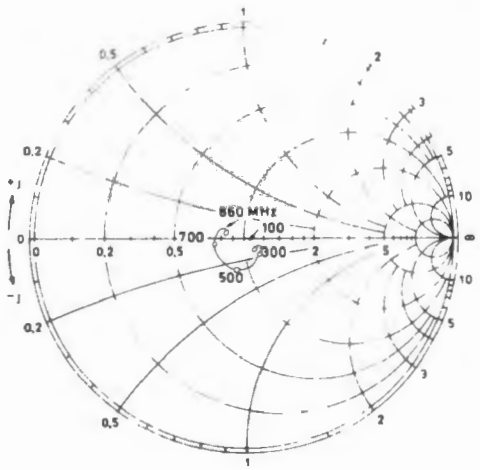
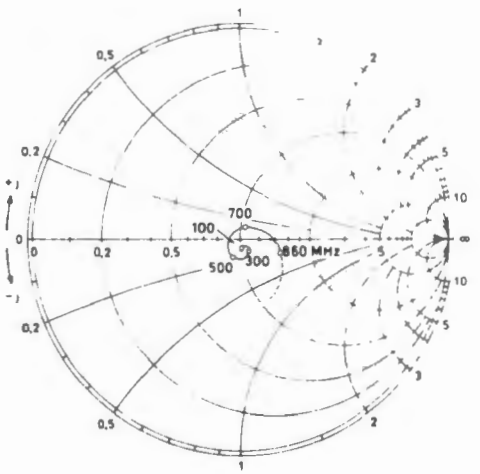


Figure 10: **Output impedance derived from output reflection coefficient s_o, co-ordination in ohm × 75; typical values.**



Design hints for layout of printed circuit boards

Single sided boards

Due to the high gain of the wideband amplifier modules, the use of single-sided printed circuit boards is not recommended. Oscillatory problems, which can easily arise, are extremely difficult to overcome. The use of additional metal screening will help but usually performance is degraded.

Double sided boards

Double sided boards are preferred for module mounting (see Figures 2 and 7). The track width depends on the thickness and material of the printed circuit board used. For a characteristic impedance of Zo = 75Ω, using epoxy glass boards without neighbouring areas of copper, the track should be approximately the same thickness as the thickness of the board. If mass-areas of copper (e.g. ground plane) are closer than 5mm to the 'hot strip' parasitic influences will disturb the characteristic impedance, and hence, the matching. If the lengths of the 75Ω track are smaller than, say 1cm, the width is less critical.

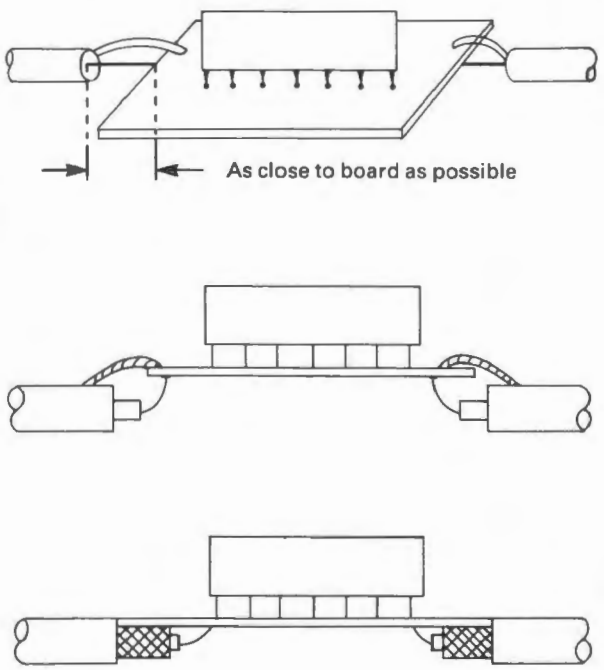
Amplifier cascading

Due to the high gain obtainable from two cascaded wideband amplifiers, the printed circuit board layout must meet very stringent requirements, and unless UHF construction techniques are strictly adhered to, cascading should not be attempted.

Cable connections

Recommendations for the connection of a coaxial cable to the printed circuit board are shown in Figure 11.

Figure 11 **Cable connections**



General

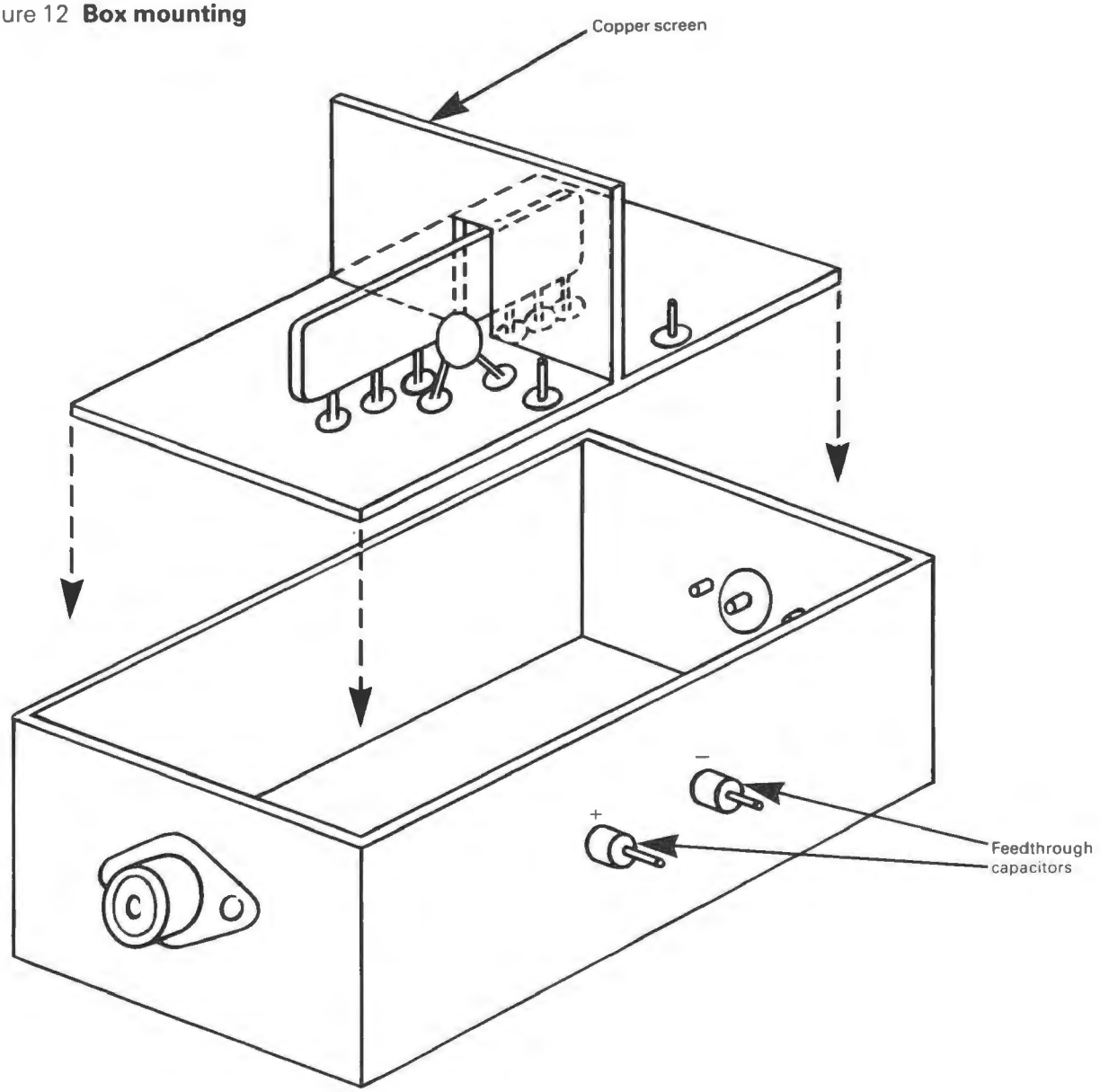
To obtain the best results from these devices it is necessary to have an appreciation of UHF techniques. In particular the following points should be observed:

1. A printed circuit board, preferably double sided, should be used with the track dimensions calculated in accordance with Stripline theory. The layouts shown in Figures 2 and 7 give good gain, however, suitability will depend on the grade of board used and the intended operating frequency.
2. Ideally the printed circuit board should be enclosed in a screened metal box (see Figure 12) with the input and output sockets situated so as to enable short, direct, connections to be made.
3. Power connections are most conveniently made using lead through capacitors, and an additional capacitor of approximately 1000pF should be connected between the module supply pin and the printed circuit board ground plane, as close as possible to the module.
4. If possible, solder a copper screen perpendicular to the module (see Figure 12) and the printed circuit board so that it bridges the module near to the supply pin, thus separating the input and output stages. This will reduce any tendency to oscillate.
5. One technique to reduce parasitic oscillation is to ensure that the mass areas shown hatched in Figures 2 and 7 are interconnected. This can be achieved using 'through board' connections 5mm apart and 5mm from the device forming a 'fence', care must be taken to ensure this does not cause shorting to signal or power tracks.

This device is capable of excellent performance, but great care is necessary in circuit construction to avoid instability. Anyone intending to use these amplifiers with no experience of UHF techniques would be strongly recommended to seek advice from a qualified engineer.

RS data

Figure 12 **Box mounting**



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RS data

Programmable current Source

Stock number 308-540

The RS 334Z is a 3 terminal adjustable current source featuring a 10,000 : 1 range in operating current, excellent regulation and a wide range dynamic voltage range of 1 — 30V. Requiring only one external resistor to set the current, this device can operate as a true floating current source, as no external power supply connections are required. The set current is directly proportional to absolute temperature, but if this facility is not required, simple modification can produce a zero temperature coefficient. Useful applications of the RS 334Z include current source to bias-networks, surge protection, current references, remote temperature sensing, etc.

PIN CONNECTIONS

TO-92
Plastic Package

PIN VIEW

Absolute maximum ratings

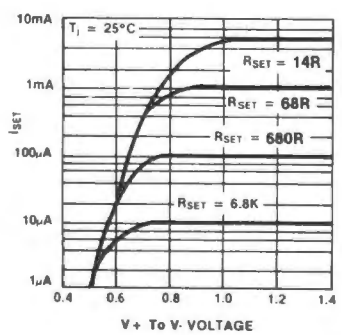
V+ to V− Forward Voltage ____ 30V
V+ to V− Reverse Voltage ____ 20V
R Pin to V- Voltage ____ 5V
Set current ____ 10mA
Power dissipation ____ 200mW
Operating temperature range ____ 0°C to + 70°C
Lead temperature (soldering, 10 seconds) ____ 300°C

Electrical Characteristics

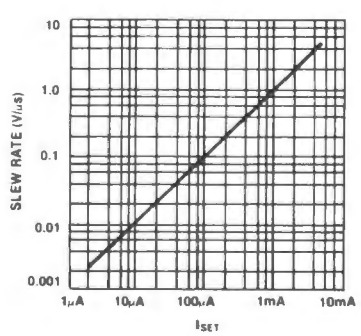
Parameter	Conditions	RS 334Z Min	RS 334Z Typ	RS 334Z Max	Units
Set Current Error, V^+ = 2.5V (see text)	$10\mu A \leqslant I_{set} \leqslant 1mA$			6	%
	$1mA < I_{set} \leqslant 5mA$			8	%
	$2\mu A \leqslant I_{set} < 10\mu A$			8	%
Ratio of Set Current to V⁻Current	$10\mu A \leqslant I_{set} \leqslant 1mA$	14	18	26	
	$1mA \leqslant I_{set} \leqslant 5mA$		14		
Minimum Operating Voltage	$2\mu A \leqslant I_{set} \leqslant 10\mu A$	14	18	26	
	$2\mu A \leqslant I_{set} \leqslant 100\mu A$		0.8		V
	$100\mu A < I_{set} \leqslant 1mA$		0.9		V
	$1mA < I_{set} \leqslant 5mA$		1.0		V
Average Change in Set Current with Input Voltage	$1.5 \leqslant V^+ \leqslant 5V$ $2\mu A \leqslant I_{set} \leqslant 1mA$		0.02	0.1	%/V
	$5V \leqslant V^+ \leqslant 40V$		0.01	0.05	%/V
	$1.5V \leqslant V \leqslant 5V$ $1mA < I_{set} \leqslant 5mA$		0.03		%/V
	$5V \leqslant V \leqslant 40V$		0.02		%/V
Temperature Dependence of Set Current, T (see text)	$25\mu A \leqslant I_{set} \leqslant 1mA$	0.96	1.00	1.04	
Effective Shunt Capacitance			15		pF

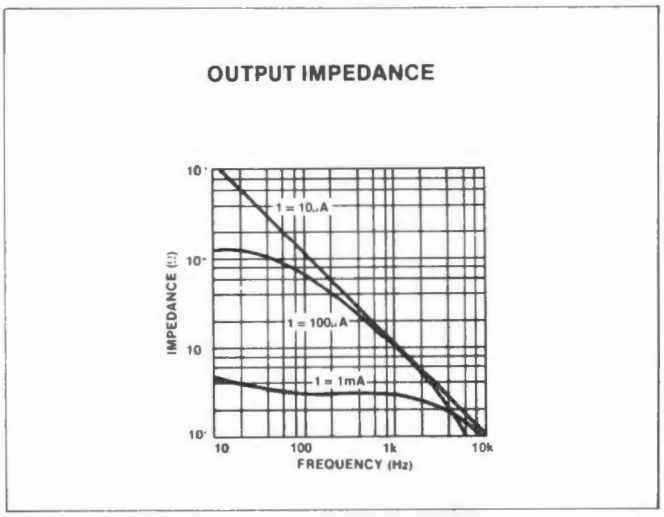
Note 1: Unless otherwise specified, tests are performed at T_j = 25°C with pulse testing so that junction temperature does not change during test.

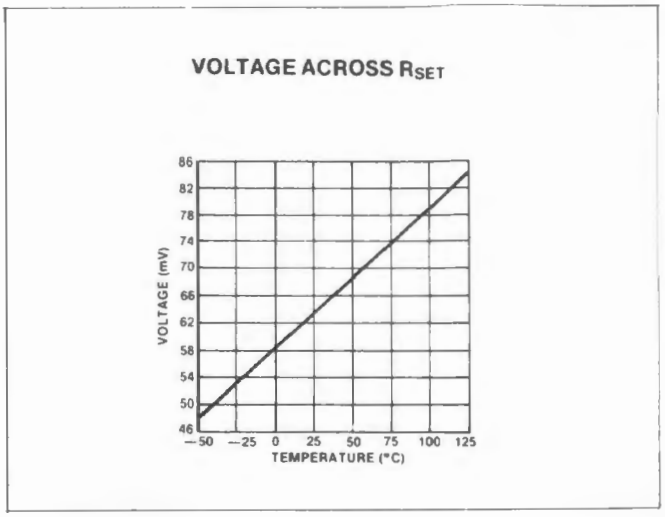
TURN-ON VOLTAGE



MAXIMUM SLEW RATE FOR LINEAR OPERATION







Operating and applications

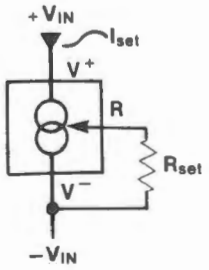
Set current calculation

The circuit shown in Fig. 1 is the basic 2 terminal current source configuration. Here one resistor R_{set} is used to determine the current I_{set} flowing into the V+ pin according to Eqn. 1.

$$I_{set} = \frac{67.7mV}{R_{set}} \quad \text{....Eqn. 1}$$
$$(\text{at } T_j = 25°C)$$

Where I_{set} is in mA
R_{set} is in ohms.

Figure 1. **Basic circuit**



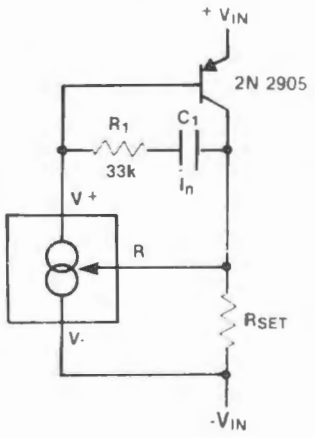
The set current error referred to in the above characteristics table is expressed as a percentage deviation from the calculated value.

The sense voltage developed across R_{set} due to the current flowing out of the R terminal is approximately 64mV at 25°C. By varying R_{set}, the current flowing out of the R terminal will vary in order to maintain the sense voltage at 64mV. This will combine with the current flowing out of the V− terminal to produce the set current I_{set} as calculated from Eqn. 1.

Higher output current

By including an external transistor in the basic circuit of Fig. 1, output currents in excess of 10mA can be achieved. The set current is amplified by the current gain of the tranistor, as shown in Fig. 2.

Figure 2. **Higher output current**



The resistor R_{set} still determines the I_{set} current which now becomes the base drive current for the 2N 2905. Because the output current flows through R_{set}, its power rating should be chosen to reduce the effects of excessive temperature rise in the resistor. The components R_1 and C_1 provide high frequency stability and may require alteration from the values shown, being dependent on circuit parameters.

Temperature sensing

The graph of 'Voltage across R_{set} versus temperature' shown on page 1 is a straight line. The dependence of I_{set} on temperature is also linear in accordance with Eqn. 2.

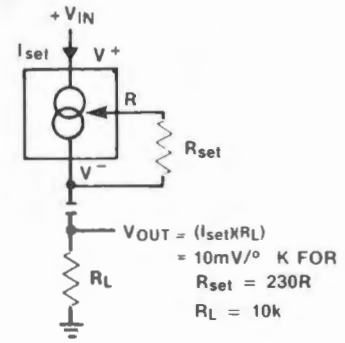
The RS 334Z can be used as a remote temperature sensor because its current mode operation does not lose accuracy over long wire runs.

Sensing is limited to application of slow rates of temperature change due to the high thermal time constant for the plastic package. The resistor R_{set} should be mounted close to the device and as such will experience the temperature being measured. For this reason a low temperature coefficient resistor should be employed for R_{set}.

$$I_{set} = \frac{(227\mu V/°K)\,(T)}{R_{set}} \quad \text{.... Eqn. 2.}$$

The circuit in Fig. 3. is a basic temperature sensor suitable for feeding the high impedance input of an operational amplifier.

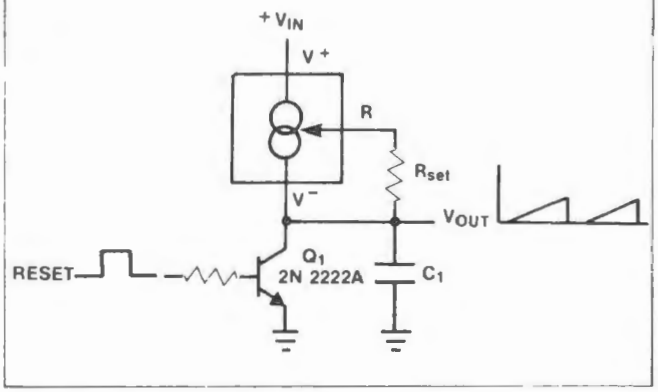
Figure 3. **Temperature sensor**



Ramp generator

By using a constant current to charge a capacitor a linear rate of change of voltage shown in Fig. 4 can be used to generate a ramp. R_{set} controls the constant current fed to the capacitor C_1, the voltage V_{out} rises linearly until the V^+ to V^- voltage falls to the level defined by the turn-on voltage curves shown on page 1.

Figure 4. **Ramp generator**



The transistor Q_1 is the discharge path for C_1 activated by a positive pulse applied to its base. The ramp output voltage is given by Eqn. 3.

$$V_{out} = \frac{I_{set}\, t}{C_1} \quad \text{.... Eqn. 3.}$$

Where V_{out} in volts
I_{set} in amps.
C_1 in Farads.
t in seconds.

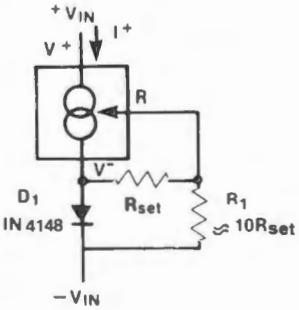
Offsetting temperature drift

To offset the drift of I_{set} with temperature, the circuit shown in Fig. 5 can be employed to provide an approximate zero temperature coefficient current source.

The current I + flowing into the V^+ terminal will be approximately twice the I_{set} value calculated from Eqn. 1 due to the effect of the diode circuit.

R_1 should be approximately 10 R_{set} but the ratio of R_1 to R_{set} will require adjustment to obtain the lowest temperature drift.

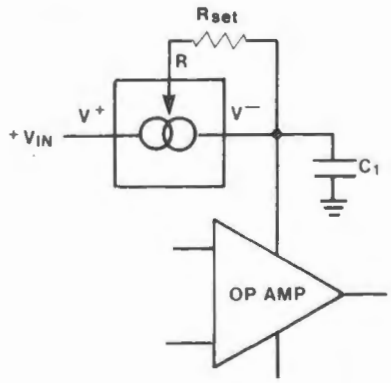
Figure 5. **Low temperature drift**



Current limiting

The RS 334Z can be used as an in-line current limiter for surge protection. A typical application is shown in Fig. 6. The capacitor C_1 should be the minimum value required to ensure stability of the protected device. Too large a value could produce a large inrush current into the device under short circuit conditions.

Figure 6. **Surge protection**

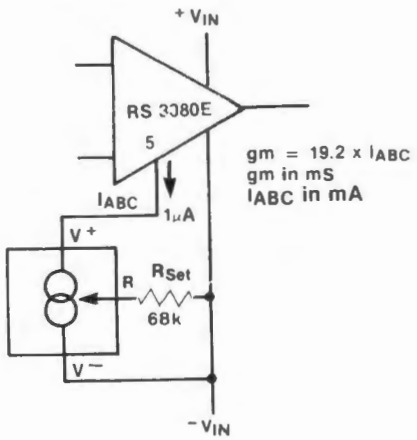


RS data

Amplifier biasing

The RS 3080E operational transconductance amplifier has a programmable transfer characteristic dependent on the current flowing into the amplifier bias input. The RS 334Z can provide a constant bias current for controlled gain requirements as shown in Fig. 7.

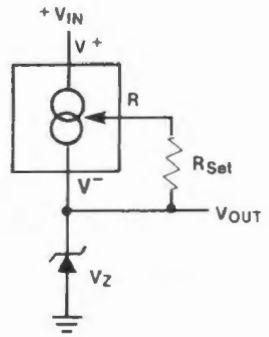
Figure 7. **Amplifier biasing**



Zener biasing

An improvement in the voltage stability of low power zener diodes can be achieved by providing a constant test current. Fig. 8 illustrates a zener biasing circuit limited to zeners requiring I_{test} currents of less than 10mA.

Figure 8. **Zener biasing**



Technical hints

Thermal effects

Internal heating can have a significant effect on current regulation for I_{set} values greater than 100μA. For example, each 1V increase across the RS 334Z at I_{set} = 1 mA will increase junction temperature by 0.4°C in still air. Output current (I_{set}) has a temperature coefficient of ≈ 0.33%/°C, so the change in current due to temperature rise will be 0.4 x 0.33 = 0.132%. This is a 10:1 degradation in regulation compared to true electrical effects. Thermal effects, therefore, must be taken into account when d.c. regulation is critical and I_{set} exceeds 100μA.

Lead resistance

The current setting resistor R_{set} should be connected between the R and V^- terminals using short leads to reduce the effect of lead resistance affecting the set current. Sockets should be avoided as 0.7Ω of contact resistance can reduce the I_{set} current by 1% at the 1mA level.

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RS data

Six decade counter/ driver i.c. RS 50395

Stock number 308–180

The RS 50395 is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with compare-register and storage-latches. The counter as well as the register can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The six-decade register is constantly compared to the state of the six-decade counter and when both the register and the counter have the same content, an EQUAL signal is generated. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7-segment format to the output. The device is capable of driving six seven segment common cathode displays, using external buffers. The seven-segment decoder incorporates a leading-zero blanking circuit which can be disabled by an external signal. The device will interface with standard CMOS logic.

Features

- Single power supply
- Schmitt-Trigger on the count-input
- Six decades of synchronous up/down counting
- Look-ahead carry or borrow
- Loadable counter
- Loadable compare-register with comparator output
- Multiplexed BCD and seven-segment outputs
- Internal scan oscillator
- Direct LED segment drive
- Interfaces directly with CMOS logic
- Leading zero blanking

Figure 1 **Pin connections**

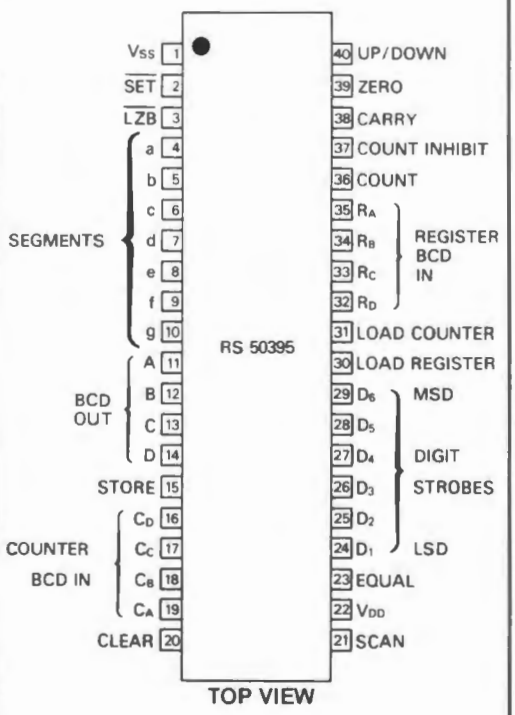
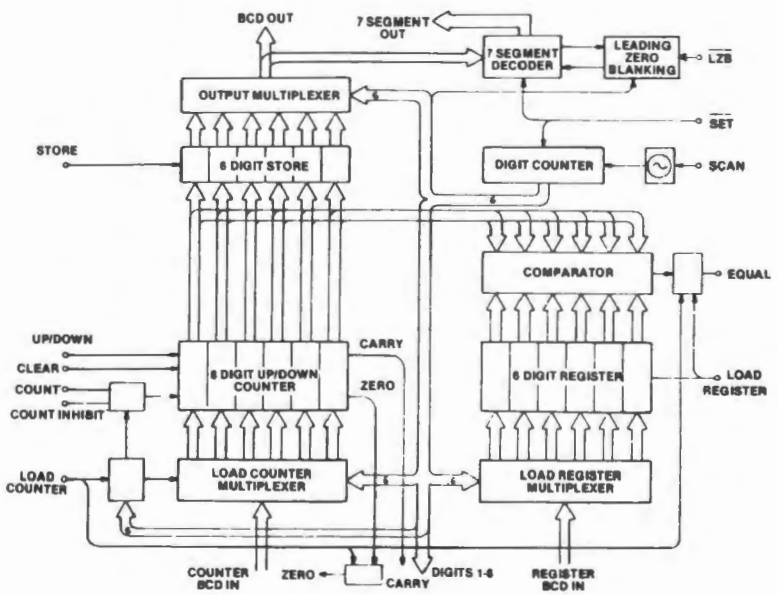


Figure 2 **Functional diagram**



Absolute maximum ratings

Voltage on any terminal relative to V_{DD} _____ −0.3V to +20V
Operating temperature range (ambient) _____ 0°C to +70°C
Storage temperature range (ambient) _____ −40°C to +100°C

Maximum operating conditions

	Parameter	Min	Max	Units	Notes
T_A	Operating temperature	0	70	°C	
V_{SS}	Supply voltage (V_{DD} = 0V)	10	15	V	
I_{SS}	Supply current		30	mA	1
B_V	Breakdown voltage (Segment only at 10μA)		V_{SS} −26	V	
P_D	Power dissipation		670	mW	2

Electrical characteristics

V_{DD} = 0V, V_{SS} = + 10.0V to +15.0V, 0°C ≤ T_A ≤ 70°C

Static operating conditions

	Parameter	Min	Max	Units	Notes
V_{IL}	Input low voltage "0"	V_{DD}	0.2V_{SS}	V	
V_{IH}	Input high voltage "1"	V_{SS} −1	V_{SS}	V	3
V_{OL}	Output voltage "0" at 30μA		0.2V_{SS}	V	4
V_{OH}	Output voltage "1" at 1.5mA	0.8V_{SS}		V	4
I_{OH}	Output current "1" digit strobes segment drivers	 3.0 10.0		 mA mA	 5 6
I_{SCAN}	Scan input pullup current at 0V		5.5	mA	
I_{SCAN}	Scan input pulldown current at 15V	2	40	μA	
$I_{\overline{SET}}$	$\overline{SET}$ input pullup current at 0V	5	60	μA	

Dynamic Operating conditions

	Parameter	Min	Max	Units	Notes
f_{CI}	Count input frequency	0	1.0	MHz	7,8
f_{SI}	Scan input frequency	0	20	kHz	
t_{CPW}	Count pulse width	400		ns	9
t_{SPW}	Store pulse width	2.0		μs	
t_{SS}	Store setup time	0		μs	10
t_{CIS}	Count inhibit setup time	0		μs	10
t_{UDS}	Up/down setup time	−0.75		μs	10
t_{CPW}	Clear pulse width	2.0		μs	10
t_{CS}	Clear setup time	−0.5		μs	10
t_{OA}	Zero access time		3.0	μs	10
t_{OH}	Zero hold time		1.5	μs	10
t_{CA}	Carry access time		1.5	μs	10
t_{CH}	Carry hold time		0.9	μs	11
t_{EA}	Equal access time		2.0	μs	10
t_{EH}	Equal hold time		1.5	μs	10
t_L	Load time	⅛ f_{SI}			

1. I_{SS} with inputs and outputs open at 0°C. 28mA at 25°C and 25mA at 70°C. This does not include segment current. Total power per segment must be limited not to exceed power dissipation of package. (θ_{JA} = 100C/Watt).
2. All outputs loaded.
3. MIN V_{IH} from R_A R_B R_C R_D C_A C_B C_C C_D inputs is V_{SS}−2.5V. Those inputs have internal pulldown resistors to V_{DD}.
4. This applies to the push pull CMOS compatible outputs. Does not include digit or segment drivers.
5. For V_{OUT} = V_{SS} −2.0 volts. Average value over one digit cycle.
6. For V_{OUT} = V_{SS} −3.0 volts. Average value over one digit cycle.
7. Measured at 50% duty cycle.
8. If carry, equal, or zero outputs are used, the count frequency will be limited by their respective output times.
9. The count pulse width must be greater than the carry access time when using the carry output.
10. The positive edge of the count input is the t = 0 reference.
11. Measured from negative edge of count input.

Figure 3 **Timing**

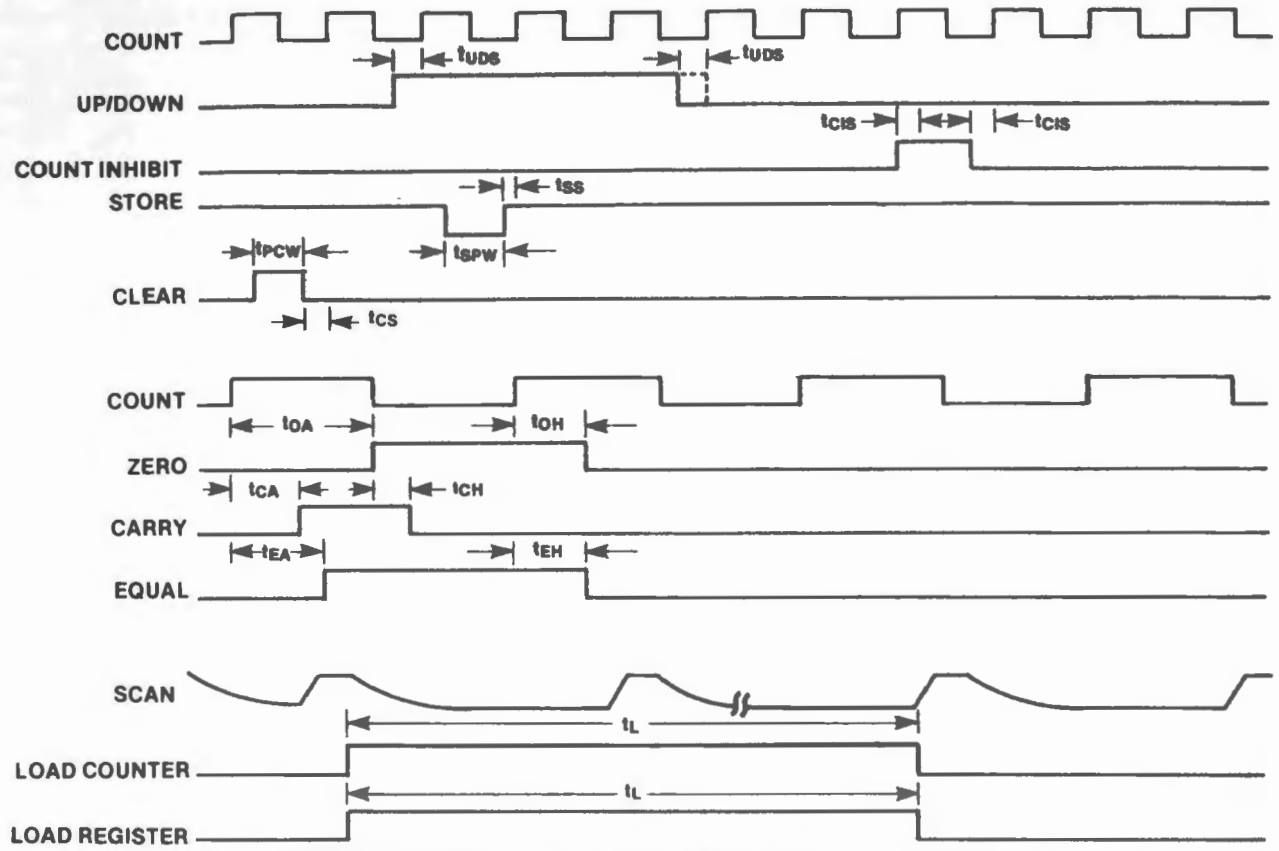
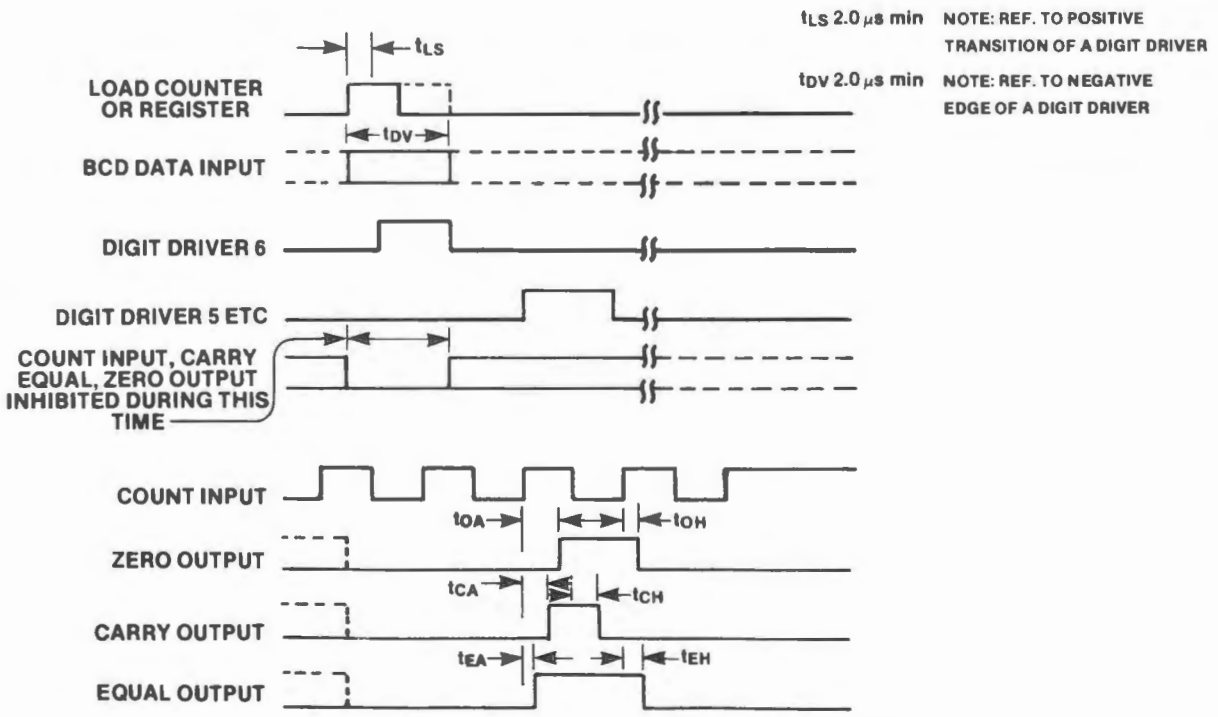


Figure 4 **Loading counter, register (1 digit)**



Note:

The inhibit function of the ZERO or EQUAL outputs does not end when the LOAD COUNTER input goes to a "0" unless that transition occurs during inter-digit blanking period at least 2.0μs prior to a positive transition of a DIGIT DRIVER. This same timing restriction hold for EQUAL and LOAD REGISTER.

Interfacing with the RS 50395

The range of supply voltage, 10.0 to 15.0V, makes the counting system particularly suitable for interfacing with CMOS logic.

A. Segment drivers – these transistors can source 10mA from the V_{SS} supply, there is no internal pull down to V_{DD} when the transistor is turned off. These transistors are capable of driving small LED displays directly via series resistors.

B. Digit drivers – a push pull configuration is used here as the most suitable arrangement for driving both external logic and display drivers (see Figure 5).

When higher power displays are used the segment outputs should be buffered by an emitter follower in order to provide the extra current.

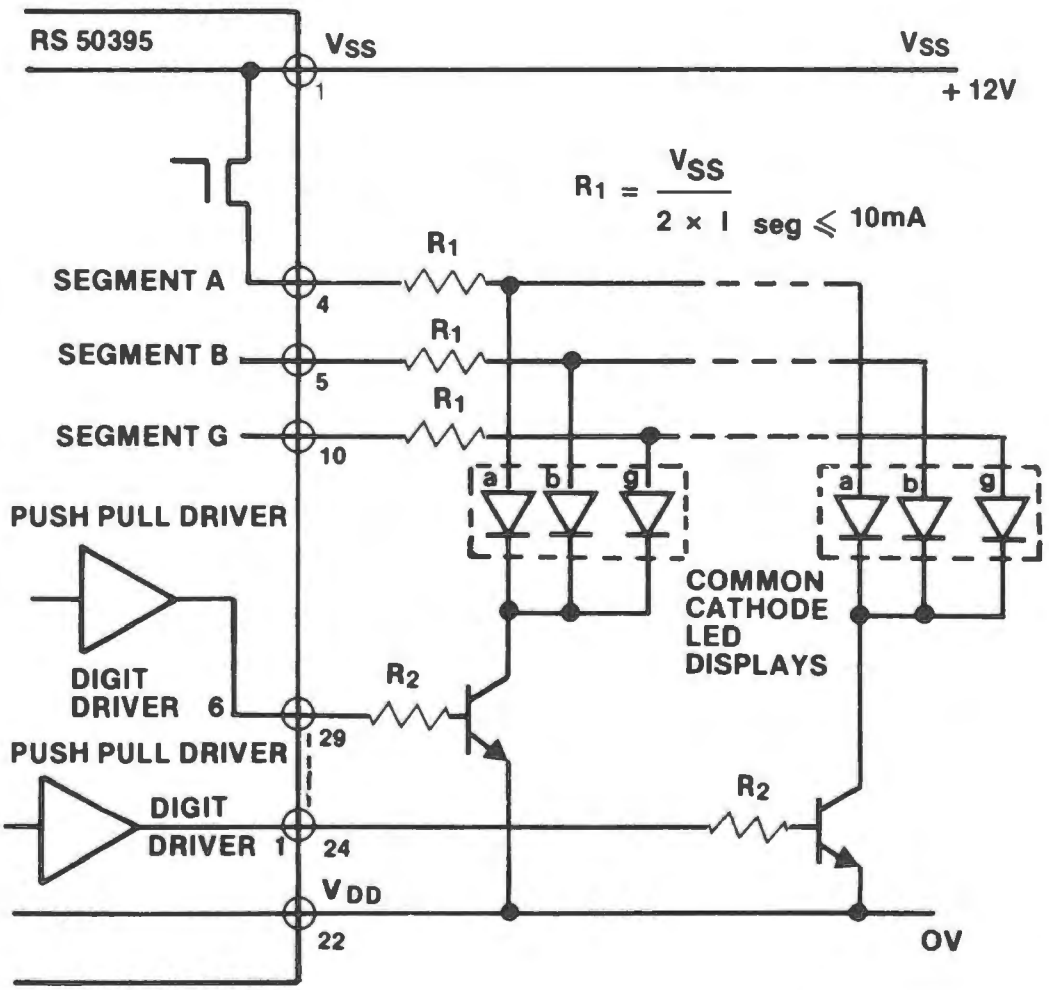
The BCD outputs, EQUAL, ZERO and CARRY are also push pull. Output drive capabilities are listed in the following table:

Table 1

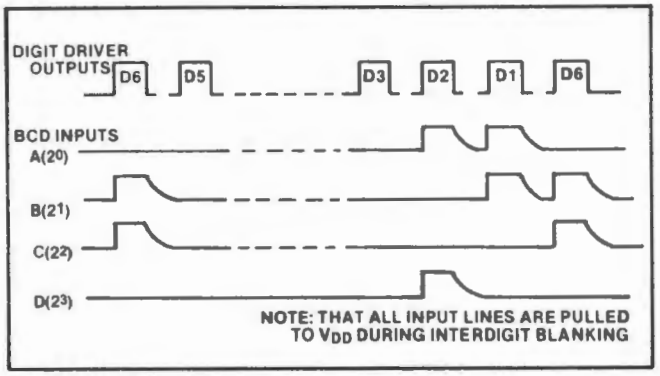
	VOL	VOH
Segment Drivers (Pins 4-10)	N/A (open drain)	V_{SS} –3V at 10mA (average over one digit driver cycle)
Digit Drivers (Pins 24-29)	V_{DD} at no load V_{DD} +4V at 0.2mA	V_{SS} –2V at 3.0mA
Equal/Zero/Carry (Pins 23, 39, 38)	V_{DD} at no load V_{DD} +4V at 0.2mA	V_{SS} –2V at 1.5mA

The following inputs, COUNT, STORE, UP/DOWN, COUNT INHIBIT, CLEAR, $\overline{LZB}$, LOAD REGISTER have no internal current sources and must therefore be driven from sources that give correct logic 1 and 0 levels – open collector circuits, or switches without pull down resistors for example, may not be used. If any of the above functions are not required then those pins should be tied to the appropriate supply, that is to V_{SS} for logic 1 and V_{DD} for logic 0. $\overline{SET}$ has an internal transistor that pulls the pin to V_{SS} if unconnected thus the driving circuit should be able to sink this current, approximately 60 μA, when pulling the input to logic 0. The COUNTER BCD and REGISTER BCD inputs have two internal transistors one static and one switched as a precharge, that pull to V_{DD}. The static current is <350 μA to V_{DD} when the input is taken to V_{SS}, the dynamic current from V_{SS} is 1mA while the transistor is on. The dynamic precharge ensures that even with the large capacitive load and leakage current of a switch matrix at these pins, the correct data will be entered at the maximum digit scan frequency.

Figure 5 **Driving LED displays directly**



An example of a switch matrix input illustrates this operation (see Figure 6). Six binary coded decimal switches are used, one for each decade, the switches being enabled by the corresponding DIGIT DRIVER output, with the paralleled switch outputs connected to the COUNTER (or REGISTER) BCD inputs. The DIGIT DRIVER outputs are separated by the interdigit blanking time and it is only during this time that the precharge transistors at the BCD inputs are all pulled to logic 0 (V_{DD}). After this blanking time the next DIGIT DRIVER output will in its turn switch to logic 1 (only one out of six is ever on) and pull those BCD inputs selected by the switch and diode matrix to logic 1. This value is loaded into the corresponding register or counter stage, i.e. the switch matrix driven by DIGIT DRIVER 6 will be



loaded into MSB of the register or counter. As the DIGIT DRIVER switches back to logic 0 the next interdigit blanking time begins and the inputs are all pulled back to logic 0 again by the internal precharge. It is possible for the DIGIT DRIVER outputs to drive both the switch matrix and a display. If the COUNTER and REGISTER BCD inputs are connected in parallel they may still be driven directly from the DIGIT DRIVER outputs.

Operation

Six decade counter, latch

The six decade counter is synchronously incremented or decremented on the positive edge of the COUNT input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the COUNT input.

The COUNT INHIBIT can be changed in coincidence with the positive transition of the COUNT input; the COUNT input is inhibited when the COUNT INHIBIT is high.

The counter will increment when UP/DOWN input is high (V_{SS}) and will decrement when UP/DOWN input is low. The UP/DOWN input can be changed to 0.75μs prior to the positive transition of the COUNT input.

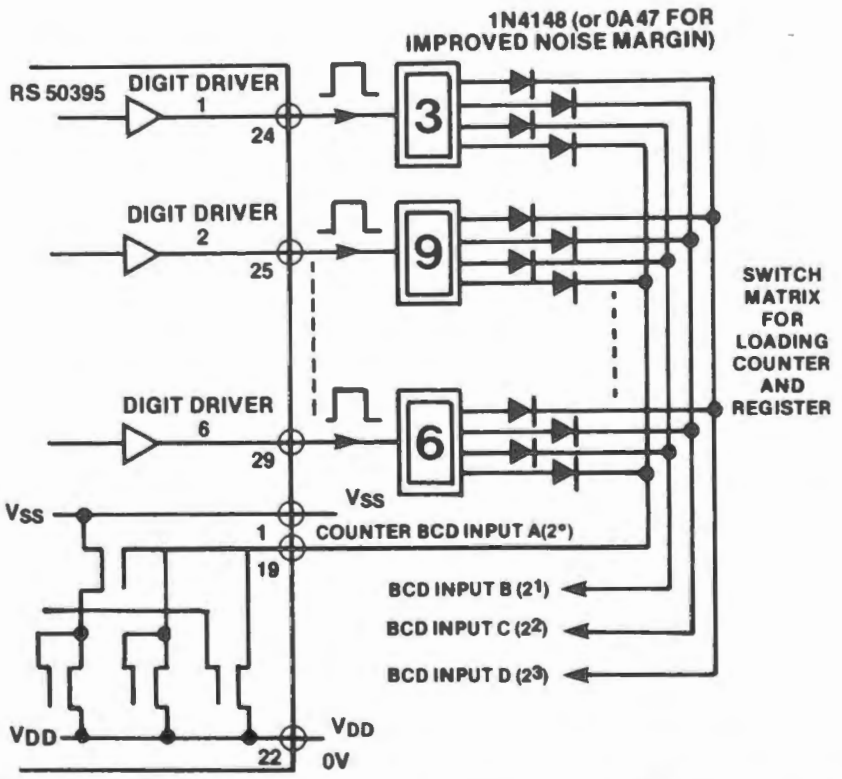
The CLEAR input is asynchronous and will reset all decades to zero when brought high but does not affect the six digit latch or the scan counter.

As long as STORE input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when STORE input is high. STORE can be changed in coincidence with the positive transition of the COUNT input.

The counter is loaded digit by digit corresponding to the DIGIT DRIVER outputs. BCD thumb wheel switches with four diodes per decade connected between the DIGIT DRIVER outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The LOAD COUNTER pulse must be at V_{SS} 2μs prior to the positive transition of the DIGIT output of the digit to be loaded. The LOAD COUNTER pulse may be removed after the positive transition of the DIGIT output since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the DIGIT output.

Figure 6 **BCD switch matrix**



Inputs, outputs

The seven SEGMENT DRIVERS are open drain capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at V_{SS}. The CARRY, EQUAL, ZERO, BCD and DIGIT DRIVER outputs are push pull and are on when at V_{SS}. All inputs except COUNTER BCD, REGISTER BCD, and SCAN inputs are high impedance CMOS compatible.

Three basic outputs originate from the counter: ZERO, EQUAL and CARRY output. Each output goes high on the positive (V_{SS}) going edge of the COUNT input under the following conditions:

ZERO output goes high for one count period when all decades contain zero. During a LOAD COUNTER operation the ZERO output is inhibited.

EQUAL output goes high for one count period when the contents of the counter and compare register are equal. The EQUAL output is inhibited by a LOAD COUNTER or LOAD REGISTER operation, which lasts until the next interdigit blanking period following a negative transition of LOAD COUNTER or LOAD REGISTER.

The CARRY output goes high with the leading edge of the COUNT input at the count of 000000 when counting up or at 999999 when counting down and goes low with the negative going edge of the same COUNT input.

A count frequency of 1MHz can be achieved if the EQUAL, ZERO and CARRY outputs are not used. These outputs do not respond at this frequency due to their output delay as illustrated in the timing diagram (see Figure 3).

Six decade compare register

The register is loaded identically to the LOAD COUNTER as described previously. The register may be loaded independently of the counter, however, the CLEAR input will not remove the register contents. Contents of the register are not displayed by the BCD or seven SEGMENT outputs.

BCD & seven segment outputs

BCD or seven SEGMENT outputs are available. DIGIT DRIVER outputs are decoded internally by a divide by six Johnson counter. This counter scans from MSD to LSD. By bringing the $\overline{SET}$ input low, this counter will be forced to the MSD decade count. During this time the SEGMENT outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when $\overline{SET}$ is low. Applying V_{SS} to $\overline{SET}$ allows normal scan to resume. DIGIT DRIVER 6 output is active (V_{SS}) until the next scan clock pulse brings up DIGIT DRIVER 5 output.

The SEGMENT and DIGIT DRIVER outputs are blanked during the interdigit blanking time. Leading zero blanking affects only the SEGMENT outputs. This option is disabled by bringing the $\overline{LZB}$ input high. Typically the interdigit blanking time is 5 to 25μs when using the internal scan oscillator.

BCD output data changes at the beginning of the interdigit blanking time. Therefore the BCD output data is valid when the positive transition of a DIGIT OUTPUT occurs.

Scan oscillator

The RS 50395 has an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and SCAN input. The waveform present on the scan oscillator input is triangular in the self oscillate mode.

An external oscillator may also be used to drive the SCAN input.

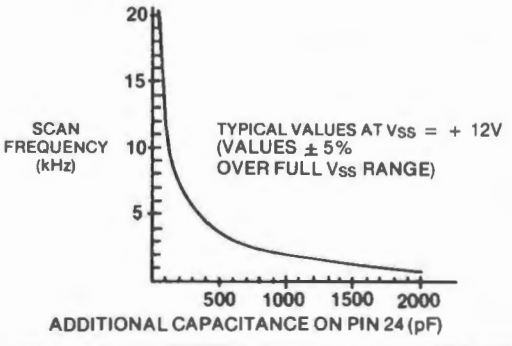
In the internal drive mode, the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self oscillate blanking time. (5 to 25μs). Display brightness can be controlled by the duty cycle of the external scan oscillator.

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor values from V_{SS} to SCAN input:

Table 2

C_{SCAN}	Min (kHz)	Max (kHz)
820pF	1.4	4.8
470pF	2.0	6.8
120pF	7.0	20

Figure 7 **Scan frequency vs external capacitance**



When the scan oscillator is free running the SCAN input may use an external capacitor to set the scanning frequency to a particular value. The signal seen at the pin is a ramp determined by the capacitance, followed by a period clamped at V_{SS}. This period clamped at V_{SS} is determined by the internal oscillator and is the interdigit blanking period. During this time the DIGIT DRIVER outputs are all turned off. When the SCAN input is driven externally this fixed interdigit period remains plus the time at which the synchronizing signal is at logic 0. To make the interdigit blanking time independent of the external synchronizing signal requires only the addition of a resistor and capacitor.

Applications

Figure 8 **6 digit counter**

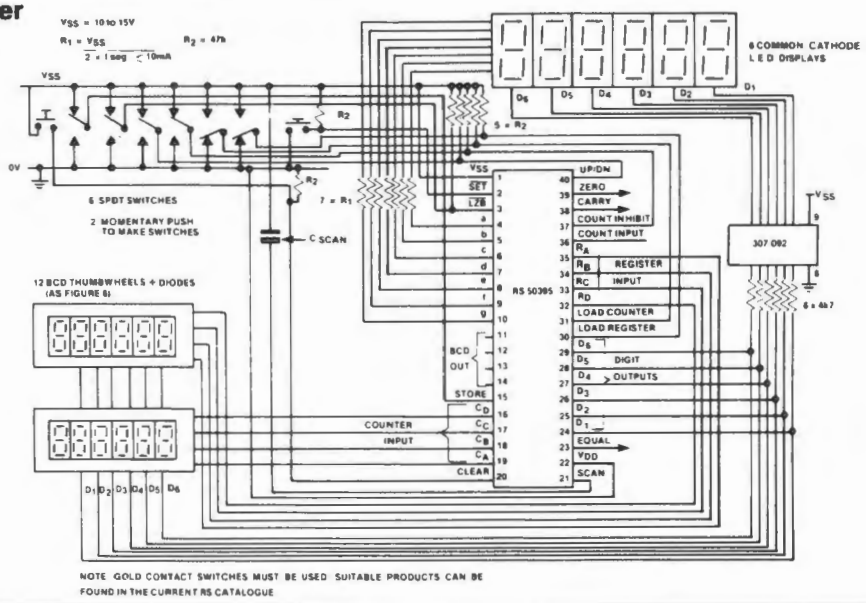
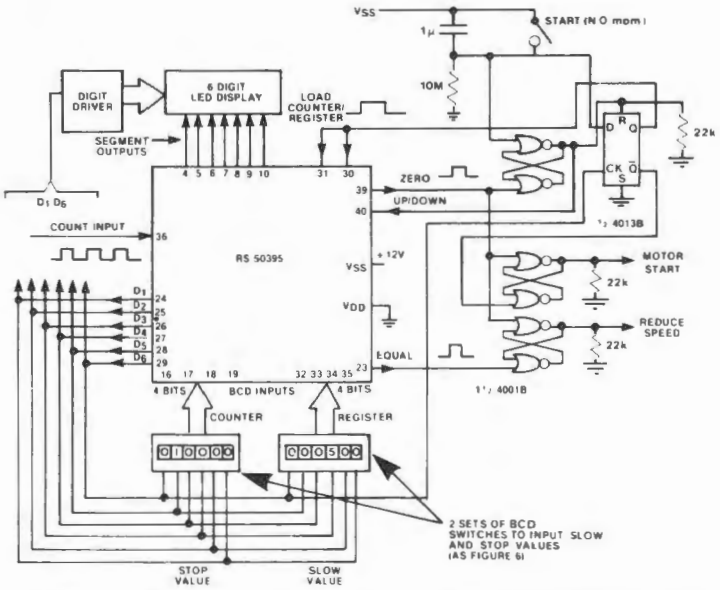


Figure 9 **Batch control**

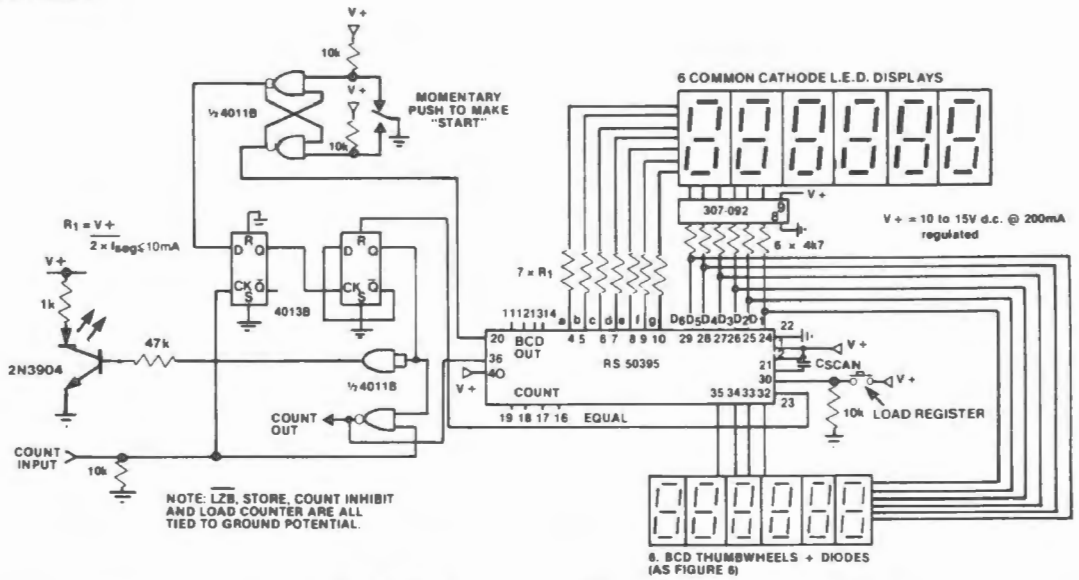


In many situations involving the metering of material, whether as a liquid, individual items or revolutions of a spindle, a two step operation is required for better efficiency. The flow is started at the maximum speed and at a preset point before the end of the operation a signal is required to slow down and eventually stop the equipment. Such applications could be as diverse as filling sacks with cement or controlling the turns on a transformer bobbin. A diagram of such a system is presented (see Figure 9). Pressing the start switch allows the input to the D flip flop to go to logic 1. This is clocked by the DIGIT DRIVER 6 so that a synchronous signal at least one complete scan cycle is obtained. This signal is used as LOAD COUNTER and LOAD REGISTER, the two controls being tied in parallel for simultaneous loading. It does not matter how long the load signal is providing it is at least one scan cycle and changes synchronously with the scan signal. The two values representing total quantity and "slow down" quantity are set on the digit switches and these values are loaded at the beginning of each cycle. Once the counter register loading is complete a start signal is generated to set the equipment in operation. The train of pulses representing the measured quantity is counted, the UP/DOWN control is in the down mode. Thus with two quantities at, let us say, 10 000 and 500 the counter starts off with 10 000 loaded and counts towards zero. When the counter reaches 500 an EQUAL signal is generated and this sets the signal controlling the brake. A further 500 pulses and the counter reaches zero, and output on the ZERO pin resets the start flip flop and the equipment is brought to reset awaiting a new start signal. In such an operation the display outputs would probably not be used.

This application can be extended by using the ZERO output to control the UP/DOWN input. The operation is identical but the start signal also sets a latch into the count down state. As ZERO is detected this latch is reset so that the counter mode is now up. Even with a braking facility there may be an "overrun" and the value now held in the counter and displayed is the extra quantity. The operator may now decide if this extra quantity is within the tolerance allowed for the job and to take whatever action is necessary.

RS data

Figure 10 **N Pulser**



The N Pulser was designed to gate a specific number of pulses, its design uses a minimum of external circuitry.
The number of pulses to be gated are entered into the thumbwheel switches, this value is loaded into the BCD Register with the load register button. When the RS 50395 counter reaches this value the RS 50395 equal output goes high. The pulse string is then interrupted.

To control frequencies above 500kHz a suitable prescaler could be used at the RS 50395 count input, and compensated by the value entered into the RS 50395 BCD Register. Pulses in and pulses out must be CMOS compatible, or suitable level shifters would be required.

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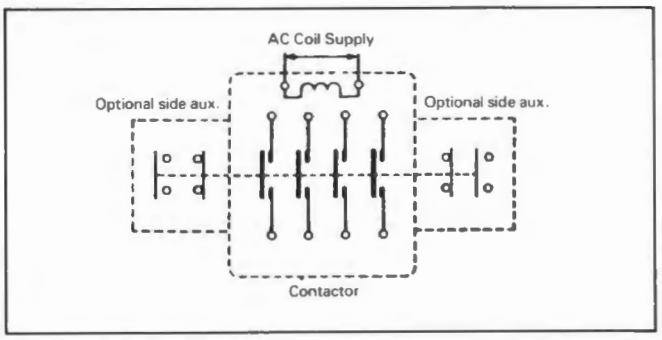
RS data

Contactors and Accessories 30A (AC1)

A range of contactors with accessories which include an enclosure, interlock kit, auxiliary switches and overload relays. The contactors are available with different coil voltages, and the overload relays available in a range of full load currents. The enclosure may be used for housing a contactor with or without an overload relay fitted. The interlock kit is used to mechanically prevent the operation of one contactor whilst another is operating (the most common use being as a motor reversing switch).



Contactor ratings

DC1 rating _____ 30A, 2 poles in series per line
Rating for lighting loads _____ 15A
Mechanical life at class 4 rate
(1200 ops/hour) _____ 5×10^6 operations
Electrical life at full load
current (AC3) _____ 3×10^5 operations
Fault protection max. fuse size class Q1 HRC ___ 30A
Coil pull-in power _____ 54VA
Coil hold-in power _____ 11VA

$110V_{ac}$ 50Hz _____ 348-740
$240V_{ac}$ 50Hz _____ 349-743
$415V_{ac}$ 50Hz _____ 348-734

Contactor specification

Duty	I_{th} (A)	I_e (A)	HP 110/115V	HP 220/240V	HP 415V	HP 600V	kW 110/115V	kW 220V	kW 380V	kW 600V
AC1 resistive loads	30									
3 phase AC2		22		7	15	20		5.5	11	15
3 phase AC3		16		5	10	13.5		4	7.5	10
3 phase AC4		12		4	8	10		3	6	7.5
3 phase Y star-delta		28		10	20	25		7.5	15	18.5
Single phase AC3			1.5	3			1	2.2		

Auxiliary switch specification

	24V	110V	250V	440V	24Vdc
AC3	5	4	4	3	5
AC11	4	3.2	3.2	2.4	4

(Up to two auxiliary switches may be fitted per contactor)

Full load current (FLC) tables (for the selection of overload relays)

3 phase motors						Single phase motors				
Motor rating		F.L.C. @ line volts				Motor rating		F.L.C. @ line volts		
HP	kW	220V	240V	380V	415V	HP	kW	110V	220V	240V
$\frac{1}{8}$	0.1	.68	.62	.39	.36	$\frac{1}{12}$	0.07	2.31	1.16	1.06
$\frac{1}{6}$	0.13	.95	.87	.55	.50	$\frac{1}{8}$	0.1	3.15	1.58	1.44
$\frac{1}{4}$	0.19	1.29	1.19	.75	.68	$\frac{1}{6}$	0.13	4.41	2.21	2.02
$\frac{1}{3}$	0.25	1.64	1.50	.94	.87	$\frac{1}{4}$	0.19	5.88	2.94	2.69
$\frac{1}{2}$	0.37	2.48	2.27	1.43	1.31	$\frac{1}{3}$	0.25	7.77	3.88	3.55
$\frac{3}{4}$	0.56	3.09	2.84	1.78	1.64	$\frac{1}{2}$	0.37	11.1	5.56	5.08
1	0.75	3.5	3.2	2.0	1.8	$\frac{3}{4}$	0.56	13.7	6.82	6.24
$1\frac{1}{2}$	1.1	4.9	4.5	2.8	2.6	1	0.75	18.9	9.44	8.64
2	1.5	6.4	5.8	3.7	3.4	$1\frac{1}{2}$	1.1	24.2	12.1	11.1
3	2.2	9.5	8.7	5.5	5.0	2	1.5	28.9	14.5	13.3
5	3.7	14.6	13.4	8.4	7.7					
$7\frac{1}{2}$	5.6	20.6	18.9	11.8	10.9					

Overload relay specifications

Switch ratings:
500 V 2 A a.c.
250 V 2 A d.c. 20 W max.

Max. fuse ratings (Class Q1)

0.85 – 1.3 A FLC type, 4 A
1.2 – 1.9 A FLC type, 6 A
1.8 – 4.2 A FLC type, 15 A
4.0 – 6.2 A FLC type, 20 A
6.0 – 12.0 A FLC type, 25 A
11.0 – 16.0 A FLC type, 30 A

Time-Current Characteristics

Figure 1 **3 phase connection**

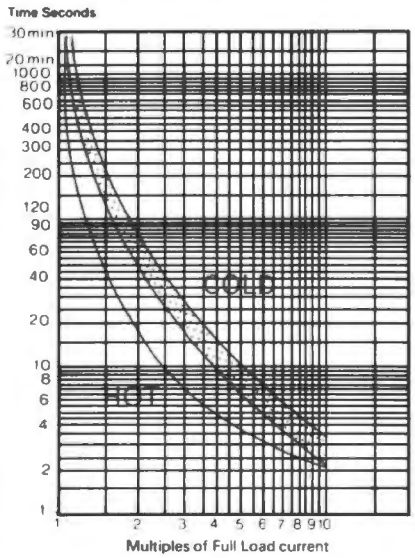
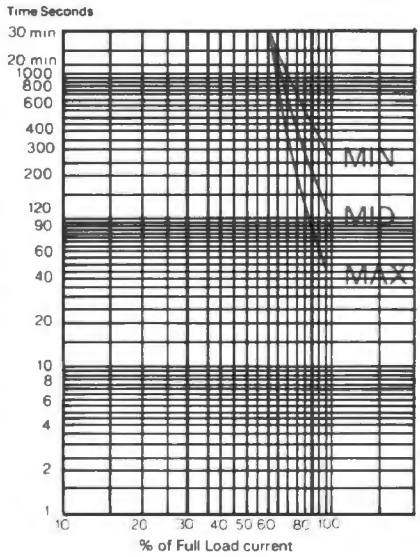


Figure 2 **Single phase connection**

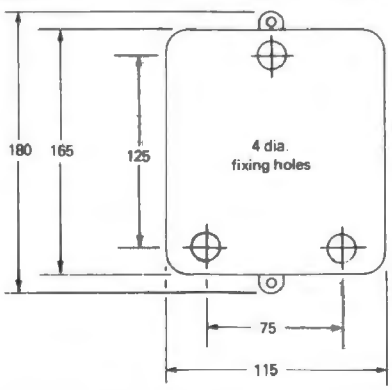


Fitting instructions

Enclosure

An IP55 sealed enclosure is available, stock no. 508-396, for mounting a single contactor plus auxiliary switches and overload relay. The enclosure consists of a black heavy gauge metal base with screw fixed gasketted flame retardent ABS lid. The metal base is fitted with a section of top hat d.i.n. rail to EN50 022, has 2 x 20 mm plugged conduit entries top and bottom and rear fixing holes.

Figure 3 **Enclosure mounting**



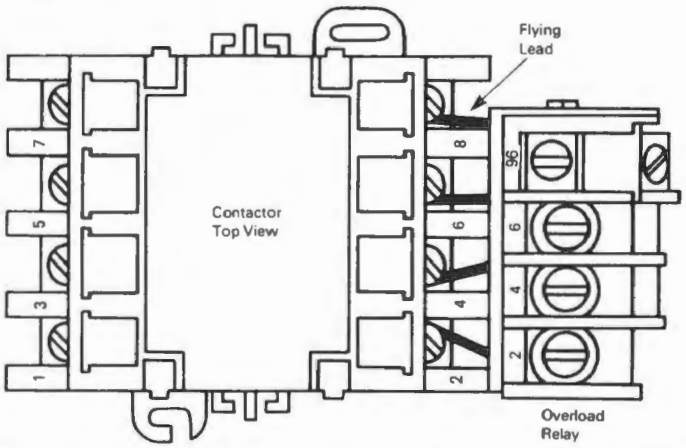
Overload relay

The overload relay should be fitted to the contactor in the position as shown in Figure 4, the flying lead being connected to connection number 8 of the contactor if this contact is to be used as a "hold-on" function (see connection diagrams). Having chosen an overload relay with the correct full load current range (using the FLC tables for common motors if necessary), the final trip current should be selected using the pointer on the side of the relay.

Overload relays

Full load motor current range (A)	Stock Number
0.85 to 1.3	348-172
1.2 to 1.9	348-166
1.8 to 2.8	348-728
2.7 to 4.2	348-712
4.0 to 6.2	348-706
6.0 to 9.2	348-699
8.0 to 12.0	348-683
11.0 to 16.0	348-677

Figure 4 **Overload relay mounting**



Auxiliary switch 337-576

Auxiliary switches may be fitted by removing the two plastic clips holding the contactor lid, placing a switch on the side so that its actuator fits over the moving side-peg and clipping it in place using the two plastic clips supplied. Two auxiliary switches may be fitted to each contactor.

Interlock kit 349-995

Insert the four plastic plungers into the side slots of two contactors from the bottom so that they are positioned as shown in Figures 5 and 6, remove the plastic base plates and mount the contactors onto the metal base plates (already fitted to the interlock kit base) using the captive screws accessed via the holes in the underside of the base.

When the interlock kit is used, overload relays and auxiliary switches may be mounted as normal.

Figure 5

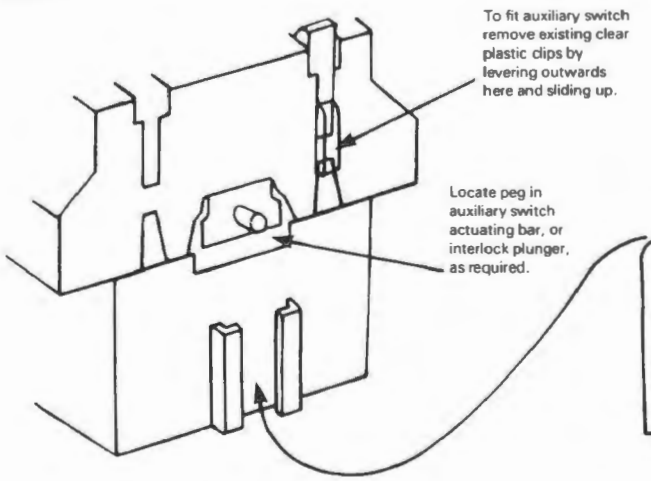
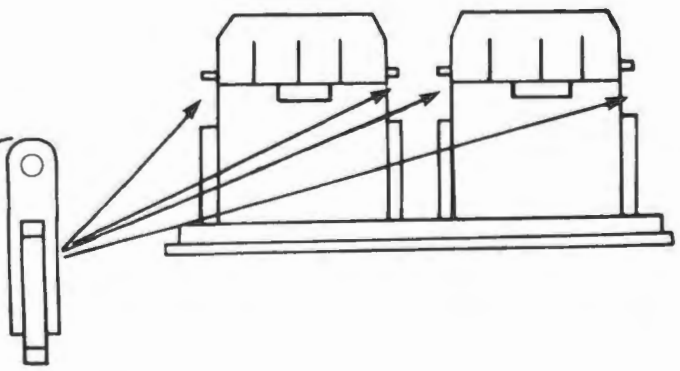


Figure 6



RS data

Typical connection diagrams

Figure 7 **Remote control 3 wire**

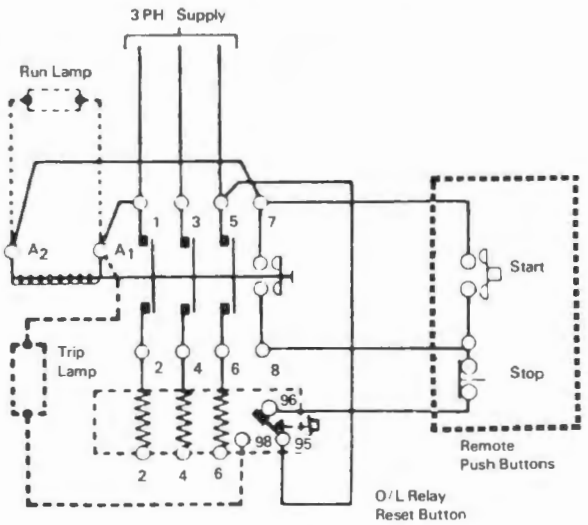


Figure 8 **Remote control 2 wire**

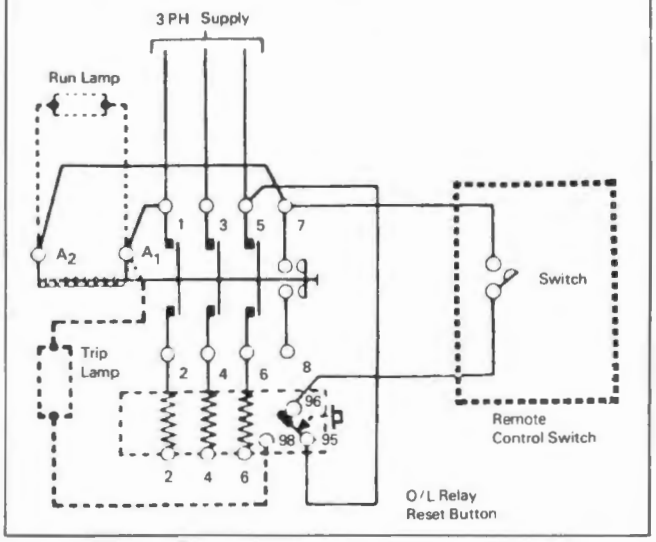
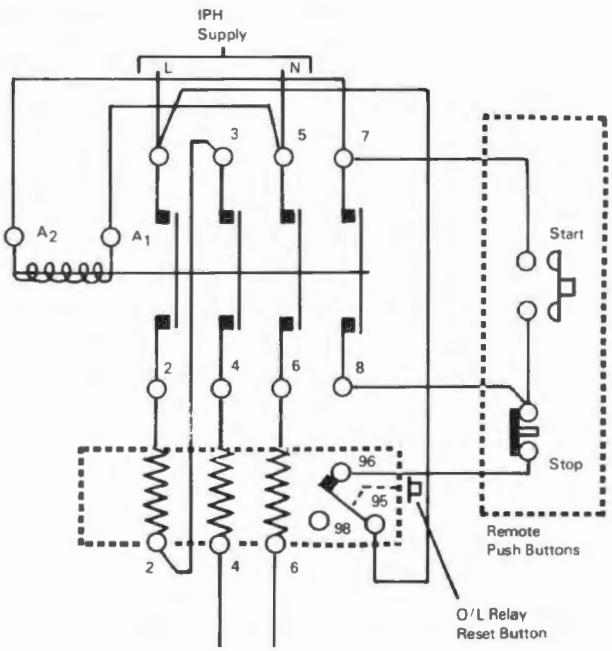


Figure 9 **Connection for single phase motors**



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RS data

Platinum resistance temperature detectors

A range of platinum film resistance temperature detectors. Three types are available as follows:

1. Basic unsheathed element (RS stock number 158-238)
2. Sheathed element (RS stock number 158-244). This comprises a platinum film element encased in a stainless steel sheath. Attached to the sheath is 1m of PTFE covered cable. The base of the sheath extends 15mm each end and may be used for mounting purposes by wrapping. If the tabs are not required, they may be cut off or folded back.
3. Sealed element (RS stock number 158-402) consists of a platinum film resistance element mounted in the end of a sealed stainless steel sheath 150mm long. The end containing the element is flattened to reduce response time. The probe is ideal for insertion into liquids and is fitted with ⅛ BSPF brass compression fitting.

The RS platinum film temperature detector linearliser (stock number 158-418) has been designed specifically for use with RS platinum film detectors and any other platinum temperature sensors which conform to BS 1904 Grade 2. The encapsulated module is suitable for PCB mounting (0.1in grid) and contains circuitry required to produce a linearised 1mV output per degree centigrade in the range −100°C to +500°C at the sensor.

Sensing circuitry is also incorporated in the module which will produce an output suitable to directly drive an LED to indicate low supply volts, i.e. battery 'low' indication. The module therefore provides a simple and cost effective means of accurately measuring a temperature over a wide range without the need of preliminary adjustments. Also specified is the RS platinum film 3½ digit temperature indicator (stock number 258-192) suitable for use with RS and other platinum temperature sensors.

Dimensions (mm)

Figure 1 **Stock number 158-238**

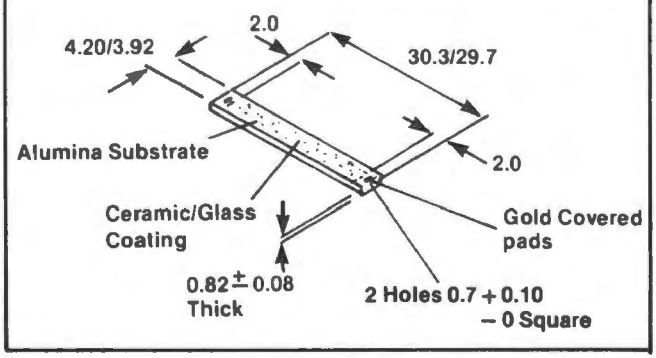
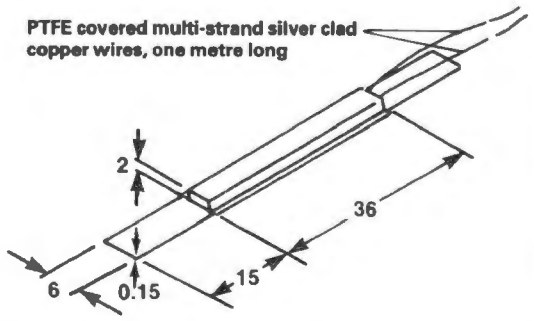


Figure 2 **Stock number 158-244**



4-wire sensor operation

This method of connection obtains maximum accuracy by compensating for any resistance introduced by connecting cables. As a platinum film sensor has a temperature coefficient of 0.385Ω/°C the cable resistance can be significant.

3-wire sensor operation

This method produces medium accuracy and some compensation for connection cable resistance but is more economical in cable costs than the 4-wire system.

2-wire sensor operation

This is a basic general purpose method of connection which will not compensate for connection cable resistance.

Figure 3 **Stock number 158-402**

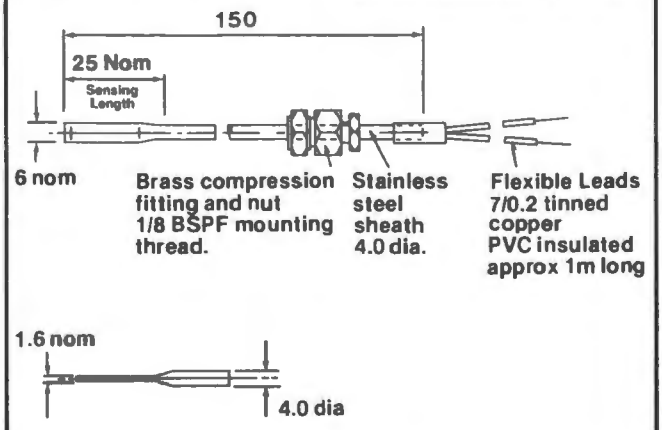
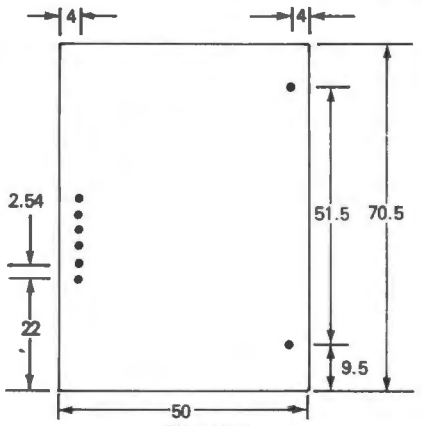


Figure 4 **Stock number 158-418**



Platinum film resistance temperature detectors

Conforms to BS 1904 Grade 2 and DIN 43 760

Specification

Resistance at 0°C	100 ± 0.1Ω
Temperature coefficient	0.385 Ω/°C
Maximum temperature	500°C (156-238) 260°C (158-244) 250°C (158-402)
Minimum temperature	–50°C
Resistance tolerance –100°C	±0.2Ω (±0.5°C)
0°C	±0.1Ω (±0.3°C)
100°C	±0.2Ω (±0.5°C)
200°C	±0.35Ω (±1.0°C)
300°C	±0.5Ω (±1.4°C)
400°C	±0.65Ω (±1.9°C)
500°C	±0.8Ω (±2.4°C)

Resistance/Temperature relationship

(deg.C)	0,0	–2,0	–4,0	–6,0	–8,0
–50,00	80,31				
–40,00	84,27	83,48	82,69	81,89	81,10
–30,00	88,22	87,43	86,64	85,85	85,06
–20,00	92,16	91,37	90,59	89,80	89,01
–10,00	96,09	95,30	94,52	93,73	92,95
–0,00	100,00	99,22	98,44	97,65	96,87
(deg.C)	**0,0**	**+2,0**	**+4,0**	**+6,0**	**+8,0**
0,00	100,00	100,78	101,56	102,34	103,12
10,00	103,90	104,68	105,46	106,24	107,02
20,00	107,79	108,57	109,35	110,12	110,90
30,00	111,67	112,45	113,22	113,99	114,77
40,00	115,54	116,31	117,08	117,85	118,62
50,00	119,39	120,16	120,93	121,70	122,47
60,00	123,24	124,01	124,77	125,54	126,31
70,00	127,07	127,84	128,60	129,37	130,13
80,00	130,89	131,66	132,42	133,18	133,94
90,00	134,70	135,46	136,22	136,98	137,74
100,00	138,50	139,26	140,02	140,77	141,53
110,00	142,29	143,04	143,80	144,55	145,31
120,00	146,06	146,81	147,57	148,32	149,07
130,00	149,82	150,57	151,33	152,08	152,83
140,00	153,57	154,32	155,07	155,82	156,57
150,00	157,31	158,06	158,81	159,55	160,30
160,00	161,04	161,79	162,53	163,27	164,02
170,00	164,76	165,50	166,24	166,98	167,72
180,00	168,46	169,20	169,94	170,68	171,42
190,00	172,16	172,89	173,63	174,37	175,10
200,00	175,84	176,57	177,31	178,04	178,78
210,00	179,51	180,24	180,97	181,71	182,44
220,00	183,17	183,90	184,63	185,36	186,09
230,00	186,81	187,54	188,27	189,00	189,72
240,00	190,45	191,18	191,90	192,63	193,35
250,00	194,07	194,80	195,52	196,24	196,96
260,00	197,69	198,41	199,13	199,85	200,57
270,00	201,29	202,01	202,72	203,44	204,16
280,00	204,88	205,59	206,31	207,02	207,74
290,00	208,45	209,17	209,88	210,59	211,31
300,00	212,02	212,73	213,44	214,15	214,86
310,00	215,57	216,28	216,99	217,70	218,41
320,00	219,11	219,82	220,53	221,23	221,94
330,00	222,65	223,35	224,05	224,76	225,46
340,00	226,17	226,87	227,57	228,27	228,97
350,00	229,67	230,37	231,07	231,77	232,47
360,00	233,17	233,87	234,56	235,26	235,96
370,00	236,65	237,35	238,04	238,74	239,43
380,00	240,13	240,82	241,51	242,20	242,90
390,00	243,59	244,28	244,97	245,66	246,35
400,00	247,04	247,73	248,41	249,10	249,79
410,00	250,48	251,16	251,85	252,53	253,22
420,00	253,90	254,59	255,27	255,95	256,63
430,00	257,32	258,00	258,68	259,36	260,04
440,00	260,72	261,40	262,08	262,76	263,43
450,00	264,11	264,79	265,46	266,14	266,82
460,00	267,49	268,17	268,84	269,51	270,19
470,00	270,86	271,53	272,20	272,88	273,55
480,00	274,22	274,89	275,56	276,23	276,89
490,00	277,56	278,23	278,90	279,56	280,23
500,00	280,90				

Basic resistance bridge networks

Shown below are three basic resistance bridge networks. The output (V_0) for each bridge is 1mV/°C which makes it ideal for direct temperature reading when connected to a DVM or any of the RS DPM's.

Suggested values

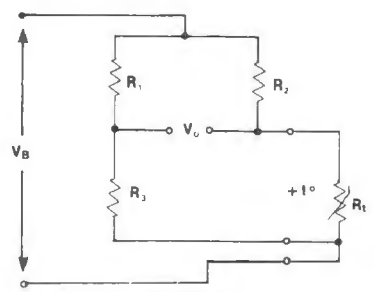
$R_1 = R_2 = 4k$ $V_B = 12V$

$R_3 = 100R$ $V_0 = 1mV/°C$

$R_4 = R_5 = 500R$

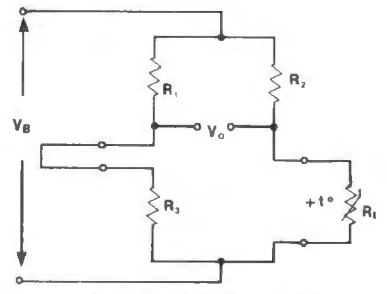
Note: All resistors precision wirewound 0.1%, ±5ppm. (For RS precision resistors see current catalogue.)

Figure 5



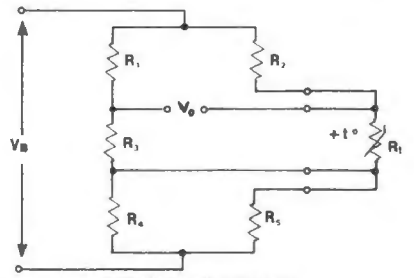
3 WIRE BRIDGE

Figure 6



COMPENSATING LEAD BRIDGE

Figure 7



KELVIN DOUBLE BRIDGE

Applications

Figure 8 **Temperature indicator, using 3½ digit LCD display and RS7106 DPM ic (display range 0-200°C resolution 0.1°C).**

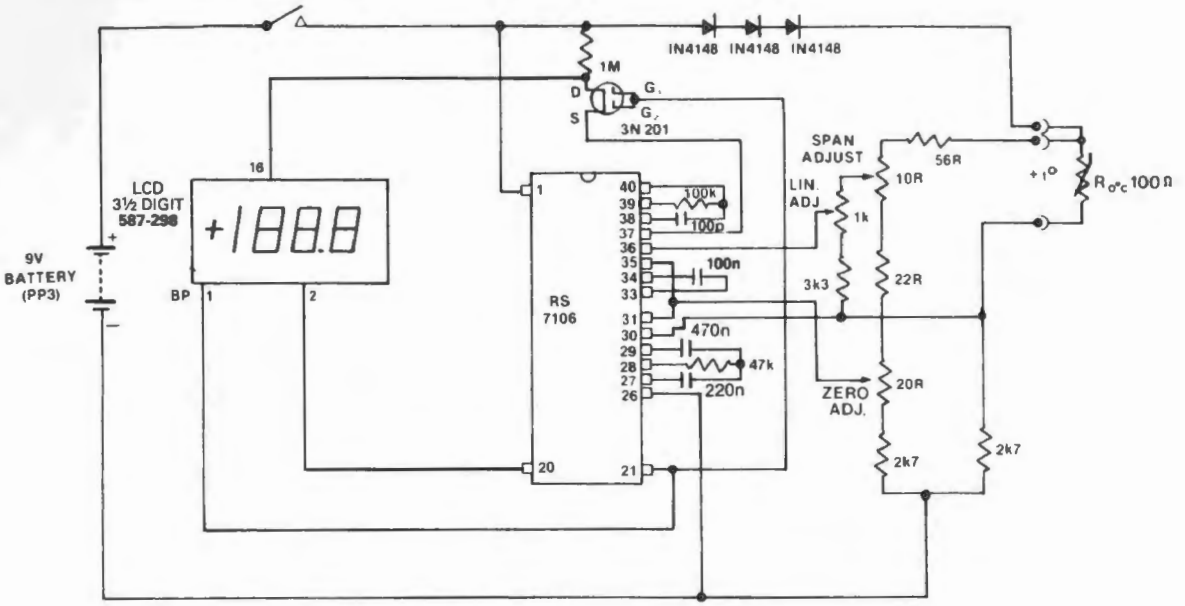
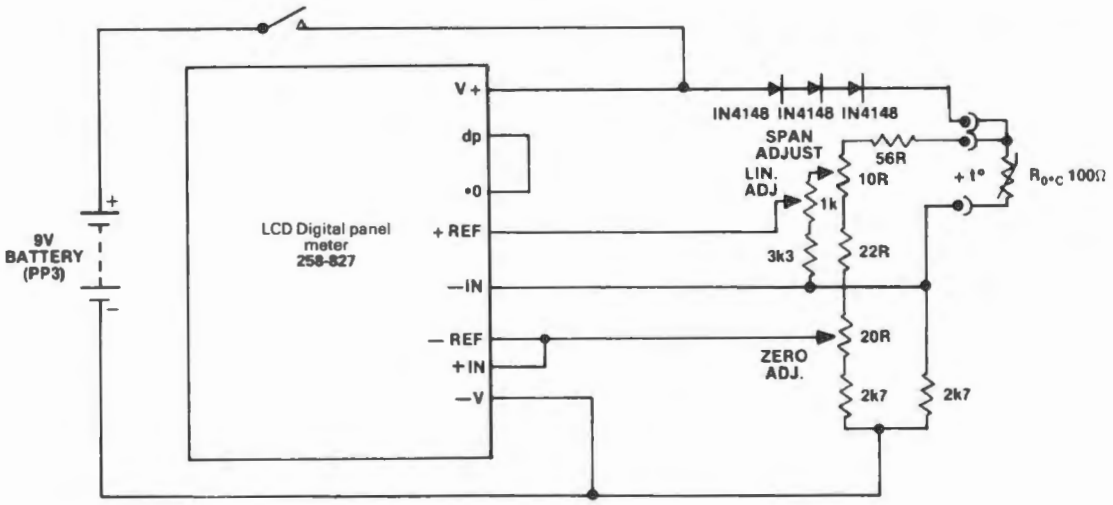


Figure 9 **Temperature indicator, using LCD digital panel meter (display range 0-200°C, resolution 0.1°C).**



Calibration

Before use, the temperature indicator circuits must be calibrated by the following procedure:

Equipment required

Resistance decade box, with a range of at least 199 ohms, resolution 0.01 ohms. (eg RS 610-297).

Calibration procedure:

1. Connect resistance decade box in place of the detector. Set decade box to 100 ohms, adjust zero potentiometer to obtain 000.0°C.
2. Set decade box to 138.50 ohms, adjust span potentiometer to obtain reading of 100.0°C (it may be necessary to alter the linearity potentiometer to obtain this reading in extreme cases).
3. Set decade box to 172.12 ohms, adjust span potentiometer to obtain reading of 190°C.
4. Set decade box to 138.50 ohms, note error reading and adjust linearity potentiometer so the reading moves further away from the correct reading of 100.0°C by an amount similar to the error noted.
5. Set decade box to 172.12 ohms, adjust span potentiometer until a reading of 190°C is obtained.
6. Repeat (4) and (5) until correct.

Recheck:

7. Set decade box to 100.00 ohms, adjust zero potentiometer to obtain 000.0°C.
8. Set decade box to 172.12 ohms, adjust span potentiometer to obtain 190.0°C.
9. Set decade box to 138.50 ohms, check reading in 100.0°C adjust as described in (4) and (5) if incorrect.

Note to Figure 8. The remaining pins on the RS7106, except pin 32, are connected to the LCD.

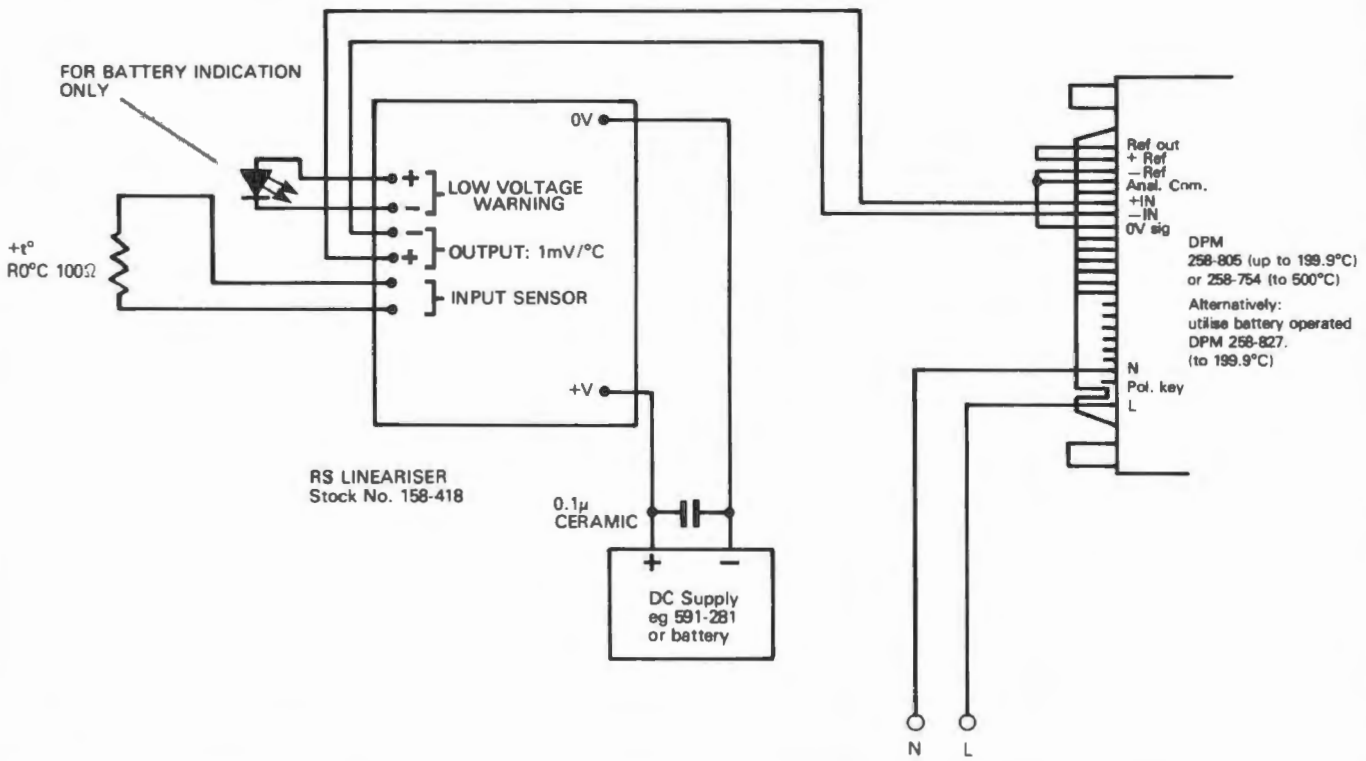
Note to Figures 8 and 9. All resistors 0.5W ±2% thick film metal glaze.

3914
Platinum film temperature detector linearisers

Specification

Power supply voltage	+7V to +15V dc
Power supply current	7mA
Low voltage warning	current limited output, suitable to drive RS LED 576-327 or similar. NB. Inaccurate readings may result if module is used when low voltage warning LED is illuminated.
Input sensor	platinum resistance thermometer element BS 1904:1964
Input temperature range	−100°C to +500°C
Maximum measurement error	±0.2°C over the range −100°C to +350°C, ±1°C from +350°C to +500°C
Ambient temperature range	−10°C to +30°C
Output voltage	1mV per °C
Long term stability	better than 0.1°C per annum
Sensor energising current	2.1mA
Output impedance	<1 ohm

Figure 10 **Connection information**



Notes

The module has been individually calibrated, and care should be taken not to introduce significant input lead resistance error between the sensor and the module, ie avoid long, thin pcb tracks or thin connecting wires.

If the load connected to the output of the module is capacitive (ie a long length of cable) then 100 ohm resistors should be inserted in series with + and − output leads to ensure stability.

When using a lineariser with a mains powered DPM, ensure that the DPM's common mode voltage range is not exceeded. Should this occur, ensure that the lineariser is fed from an isolated supply and connect the DPM in a single ended mode. See Figure 10.

The −ve output sits nominally at 1.2V above the 0V rail, while the +ve output pin varies with temperature.

The lineariser is designed for simple installation and is suitable for remote mounting and requires no compensation loops.

Providing the remote millivolt output is read using a high input impedance instrument, such as a DPM, eg RS 258-827, there is no loss of accuracy – the cable resistance being negligible when compared with the input impedance of the DPM.

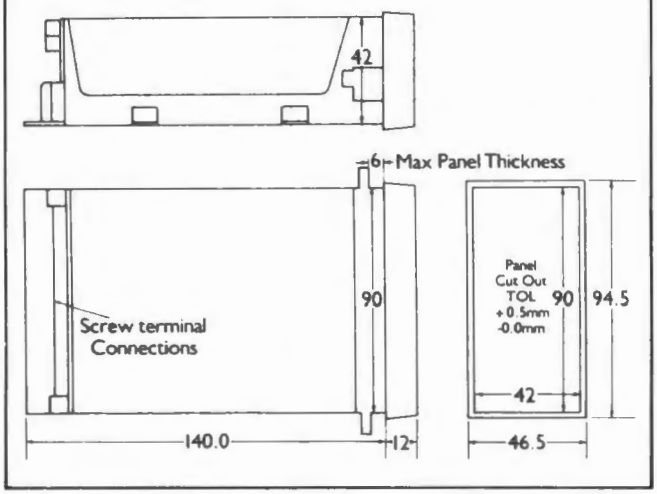
Panel mounting digital temperature indicator

A panel mounting, 3½-digit temperature indicator in a DIN size case suitable for use with RS and other platinum film sensors. The unit features automatic cold junction compensation and automatic zeroing with a 4-wire compensation system used to minimise the effect of lead resistance, maintaining a high overall system accuracy. This enables use with 2-, 3- or 4-wire sensors. The display is autoranging having a resolution of 0.1°C up to +185°C and 1°C for temperatures above. The unit is fitted with a linear analogue output which can be used to drive a chart recorder or form part of an analogue control system. Connections via a terminal strip.

Specifications

Temperature range	−150°C to +800°C
Resolution	0.1°C below +185°C 1°C above +185°C (autorange change at +185°C ±5°C)
Sensor type	PT. 100Ω resistor to BS 1904 DIN 43760
Accuracy at 25°C	±0.2% of reading ±1 digit
Ambient temperature range	0°C to +45°C
Sensor operating mode	4-wire constant current voltage sensing
Analogue output	1mV/°C (2kΩ source)
Display type	3½-digit 11.2mm, 7-seg. LED
Power supply requirements	220/110V, 50 Hz, 10VA

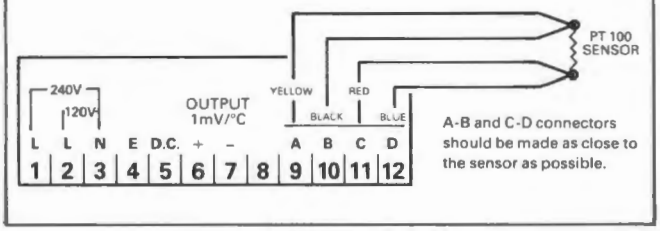
Figure 11 **Dimensions**



4-wire sensor operation

4 core copper cable should be used to connect the sensor to the input terminals as detailed in Figure 12.

Figure 12 **4-wire sensor wiring**



3-wire sensor operation

When using a 3-wire sensor terminals 9 and 10 should be linked together and the sensor connected to terminals 10 (black wire), 11 (red wire) and 12 (blue wire).

2-wire sensor operation

When using a 2-wire sensor terminals 9 and 10 and terminals 11 and 12 should be linked together. The sensor should then be wired to terminals 10 (black wire) and 11 (red wire).

RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

Industrial fuses NS, A1, A2, A3, A4 types.

A range of Industrial Fuselinks which comply with the dimensional requirements and current ratings of BS88: Part 2: 1975. All the fuses except the NS version which is spade connecting, are of the bolted connection, offset tag type (BS88 reference types A1, A2, A3 & A4). Suitable fuse carriers are available to accommodate all fuse types – refer to current catalogue.

Features

- Low power loss – maximum ratings typically 20% below these specified in BS88.
- Fusing factor approx. 1.45 – gives adequate close excess current protection to P.V.C. cables.
- Low total I^2t let-through – reduces thermal stresses.
- Low cut-off currents – reduces electro-thermal stress and damage to contacts.
- High pre-arcing I^2t – made as high as practicable to withstand current surges thus minimising discrimination problems.

All the above features combine to generally enable the safe replacement of fuselinks to BS88: Part 2: 1975 + BS88: Part 1: 1967 by RS Industrial Fuses.

Definitions

Prospective current of a circuit (with respect to a fuse). The current that would flow in a circuit if a fuse situated therein were replaced by a link of negligible impedance.

Prospective breaking current. The prospective current measured at a time corresponding to the instant of the initiation of the arc in a fuse during a breaking operation.

Cut-off current. The maximum instantaneous value reached by the current during the breaking operation of a fuse link when the fuse link operates in such a manner as to prevent the current from reaching the otherwise attainable maximum.

Rated breaking capacity. The maximum prospective breaking current that a fuse is stated to be capable of breaking at a stated recovery voltage under specified conditions.

Fusing factor. The ratio to the rated current of the current co-ordinate on the pre-arcing characteristic corresponding to a stated time.

Pre-arcing time. The time between the commencement of a current large enough to cause the fuse element(s) to melt and the instant when an arc is initiated.

Arcing time. The interval of time between the instant of the initiation of the arc and the instant of final arc extinction.

Operating time. The sum of the pre-arcing time and the arcing time.

I^2t (specific energy or Joule integral). The integral of the square of the instantaneous current (i) over a given time interval ($t_1 - t_0$):

$$I^2t = \int_{t_0}^{t_1} i^2\,dt$$

NOTE. I^2t values usually stated for fuse links are pre-arcing I^2t and operating I^2t extended over the pre-arcing time and the operating time respectively, and measured under specified conditions.

Characteristics

Time/current characteristics

The time/current characteristics (Figures 3 and 4) show the nominal pre-arcing time/current relationship. They are based on tests with the fuselinks mounted in specified test rigs at an ambient temperature between 15°C and 25°C and the tests commencing with the fuselinks at ambient temperature. The tests are based on symmetrical 50 Hz currents to further standardise test procedures.

To comply with the requirements of BS88: Part 2: 1975 the time/current characteristics including manufacturing tolerance, ±10% maximum on current, must lie within specified zones. These zones have the minimum pre-arcing time and maximum total operating time at 415 volts as their limiting values. The concept of virtual time is used for these zones. This has not been common British practice for low voltage fuselinks in the past. However the virtual time is simply related to the more familiar I^2t value. It is the I^2t divided by the square of the r.m.s. prospective breaking current. The published time/current characteristics include virtual pre-arcing times to a limiting value of 0.004 secs. All the RS standard current ratings fall within the limiting values of the time/current zones.

I^2t values

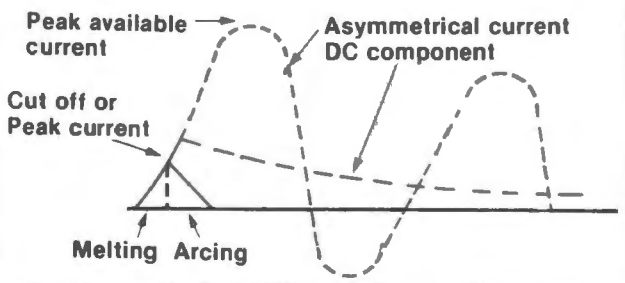
The I^2t values are tabulated and for convenience are included with the time/current characteristics. They show the total operating I^2t and pre-arcing I^2t under onerous condition of maximum arc energy, I_2, to BS88: Part 2: 1975. The total I^2t values are quoted for a rated voltage of 415 volts and, where applicable, higher voltages. These total I^2t values approximate to a virtual operating time of approximately 0.004 secs.

The higher the voltage the more onerous is the duty of the fuselink due to the increase in energy absorbed by the fuselink during the arcing process. Under short circuit conditions this leads to an increase in I^2t let-through with voltage. The pre-arcing I^2t is independent of the applied voltage.

Cut-off characteristics

The current limiting effect of HRC fuselinks is shown diagramatically in Figure 1. Cut-off current characteristics relate to the maximum values of peak fuse current that can be obtained for a given prospective fault current. The characteristics are for a 50 Hz system, power factor between 0.1 and 0.2, and point on wave of initiation of the short circuit chosen to give the maximum value of peak current. The peak currents are plotted against the r.m.s. symmetrical prospective current. The cut-off characteristics refer to all voltages up to 660 volts or where applicable 550 or 415 volts.

Figure 1: **Fuselink operation under 'short circuit' conditions**



Supply frequency

All breaking capacity tests have been performed at 50 Hz but in accordance with BS88: 1975 and IEC 269-2 the RS Industrial range of fuselinks are suitable for operating between 45 Hz and 62 Hz.
For frequencies less than 45 Hz a decrease in voltage rating is required the limiting value being the d.c. voltage rating. The I^2t let-through will decrease with increasing frequency whereas the cut-off current will increase.

De-rating for high ambient temperatures

The recommendations for the maximum current carrying ability of the RS Industrial range of fuselinks are based on three salient factors:
Limiting the temperature of the fuse element.
Limiting the temperature of the fuselink. (For a practical guide the cap temperature is limited to approximately 100°C).
Maintaining a minimum fusing current above 1.25 times its new rating.
From table 1 on page 4 it will be seen that many of the fuselinks can carry rated current at relatively high ambient temperatures since the RS Industrial range have low power dissipation values. The recommendations given in the table relate to the standardised test arrangement in free air. In service the fuselinks are generally mounted within an enclosure which results in an inside temperature higher than the outside ambient. In order to assess the maximum current carrying ability of the fuselink in such applications it is recommended that the inside temperature be related to table 1 and in the absence of details this is normally taken as 15°C above the outside ambient temperature.

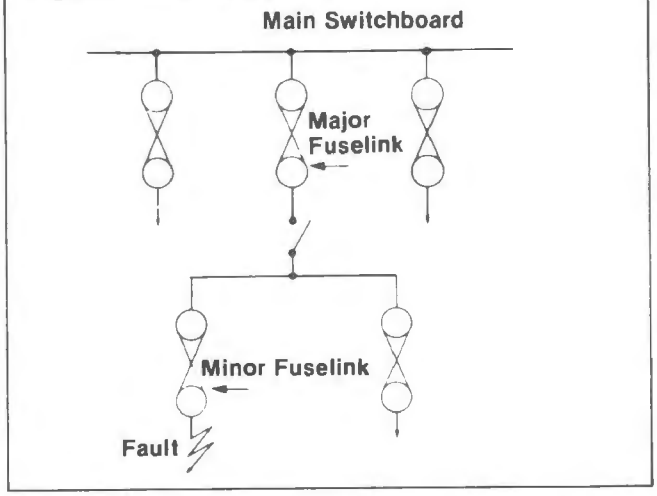
Power dissipation

The thermal interchangeability of fuselinks in associated equipment is assessed by the power dissipation values of fuselinks and power acceptance levels of the equipment. The power acceptance levels of the equipment are determined from temperature rise limits for the materials of its component parts. The quoted power dissipation of fuselinks must be the maximum value i.e. at the extremity of the tags. BS88: Part 2: 1975 specifies the position of measurement and also a standardised test arrangement; the power loss values relate to a maximum test ambient temperature of 25°C.
With general uprating of equipment and increasing use of plastics it is important to keep the power dissipation values of fuselinks as low as possible without adversely affecting other characteristics. The power dissipation values of the RS Industrial range are well below the maximum values permitted in Table 1 of BS88: Part 2: 1975, and are tabulated for convenience with the time/current characteristics.

Discrimination

In determining if discriimination occurs between two fuselinks in a circuit with a fault the minor fuselink should operate and leave the major fuselink unimpaired.
The time/current zones to BS88: Part 2: 1975 ensure that all manufacturers fuselinks which comply with this specification will discriminate on a 2:1 ratio between the major and minor current ratings. This applies for all voltages up to 415 volts a.c. and consequently covers the majority of application requirements. More accurate selection can be made by reference to individual characteristics.

Figure 2: **Discrimination**



For 'Short Circuit' faults, fuse operation in less than ½ cycle, I^2t values should be used to assess discrimination. The total I^2t of the minor fuselink must be less than the pre-arcing I^2t of the major fuselink. For lower values of fault current reference should be made to the time/current characteristics.

Example

Will a 32 A-A2 fuselink discriminate with a 63 A-A3 fuselink at a fault level of 300 Amps? From the curves in Figure 4 it will be seen that the opening times of both fuselinks at 300 amps lie on the time/current characteristics.
The 32A fuse will operate on 0.13 secs and the 63A fuse would operate in 2.7 secs.
Discrimination will therefore be achieved.

Capacitor circuits

For power factor correction capacitors the fuselink should be chosen with a current rating greater than 1.5 times the rated capacitor current. This takes account of the high transient inrush current, circuit harmonics and capacitor tolerances.

Cable protection

Rules for overcurrent protection of conductors are given in chapter 43 of the 15th edition of the IEE wiring regulations for Electrical Installations which is in accordance with IEC publication 364. RS industrial fuselinks to BS88 part 2: 1975 protect associated cables against overcurrents, provided the current rating of the fuselink, I_N, is equal or less than the current carrying capacity of the cable I_z.
In motor circuits the motor starter will provide overload protection of the circuits. The fuselink in such circuits will provide short circuit protection to the cable.

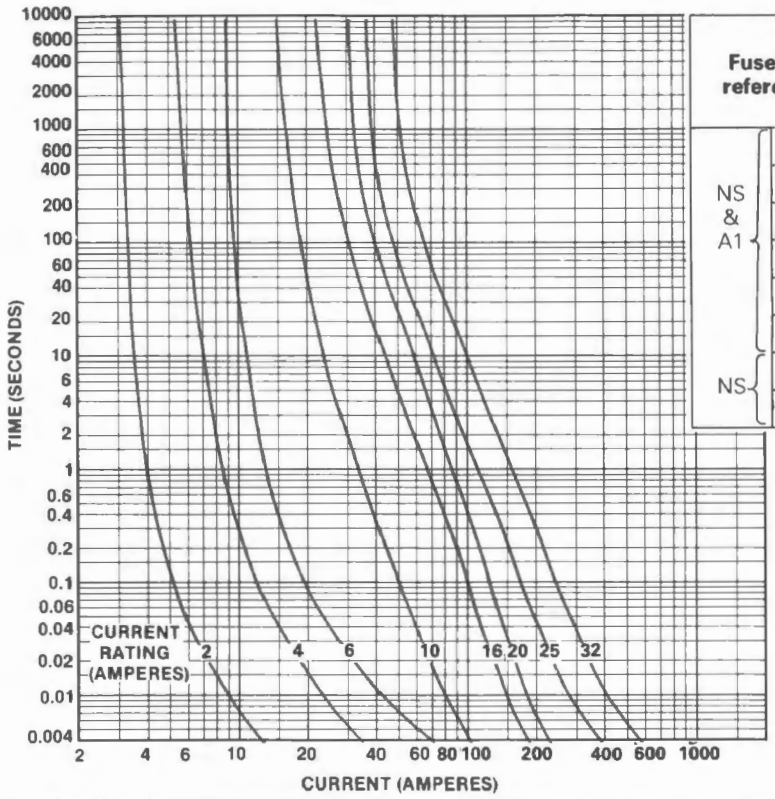
Fluorescent lighting protection

The normal current rating of the fuselink should be at least twice the total normal load current of the maximum number of lights to be switched simultaneously.

Fuselink on the primary side of transformers

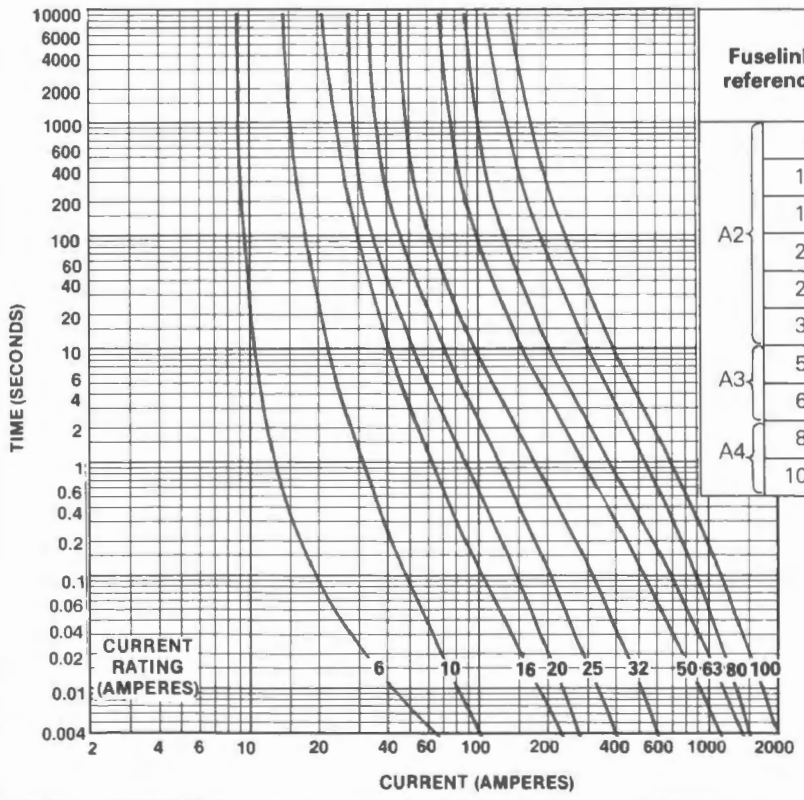
The normal current rating of the fuselink should be at least twice the nominal transformer primary current.

Figure. 3: **Time/current characteristics – fuse types NS & A1**



Fuselink reference		I²t (Amp²secs) Pre arcing	Total at 415V	Total at 550V	Nominal watts loss at full load
NS & A1	2A	0.8	1.6	2.4	1.0
	4A	5	10	15	1.8
	6A	20	40	60	1.8
	10A	44	130	180	1.6
	16A	160	360	480	1.9
	20A	280	640	850	2.5
NS	25A	620	1450	–	2.5
	32A	1400	3200	–	2.7

Figure 4: **Time/current characteristics – fuse types A2, A3 & A4**



Fuselink reference		I²t (Amp²secs) Pre arcing	Total at 415V	Total at 550V	Total at 650V	Nominal watts loss at full load
A2	6A	20	40	60	80	3.3
	10A	44	130	180	220	2.8
	16A	250	765	1000	1200	2.8
	20A	430	900	1300	2500	2.7
	25A	850	1800	2500	4900	3.1
	32A	2100	4400	6100	12000	3.3
A3	50A	6900	14500	20000	40500	4.8
	63A	11500	24500	34000	68000	5.7
A4	80A	13000	23000	32000	63000	7.2
	100A	24000	42000	60000	120000	8.2

RS data

Figure 5 **Cut-off current characteristics**

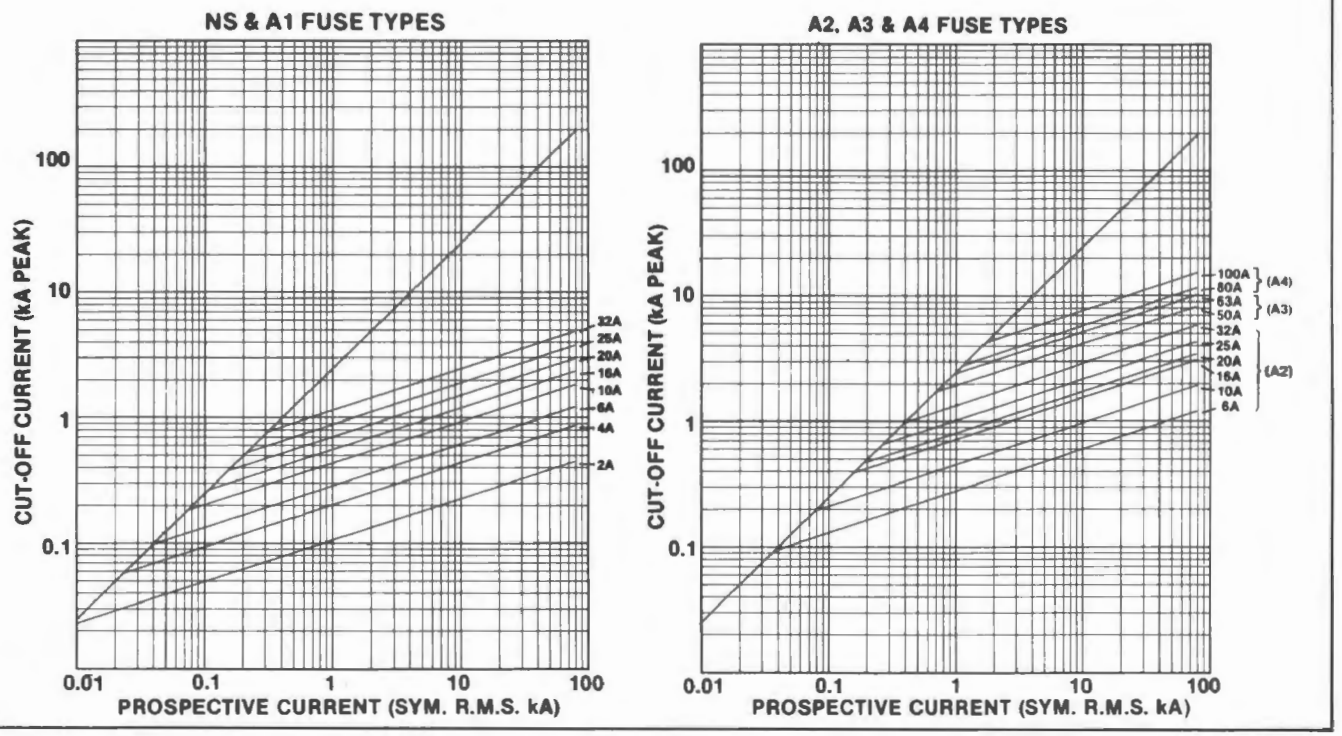


Table 1 **Current carrying ability at high temperatures**

Fuselink reference		Typical current carrying ability at these ambient temperatures – Amps									
		35°C	40°C	45°C	50°C	55°C	60°C	65°C	70°C	75°C	80°C
NS & A1	16A	16	16	16	16	16	16	16	16	14	13
	20A	20	20	20	20	20	20	19	17	16	15
	25A	25	25	24	24	23	22	21	20	18	17
	32A	32	32	32	31	30	28	26	25	23	21
A2	16A	16	16	16	16	16	16	16	16	15	14
	20A	20	20	20	20	20	20	20	20	18	17
	25A	25	25	25	25	25	25	25	22	19	16
	32A	32	32	32	32	32	32	32	32	30	28
A3	50A	50	50	50	50	50	50	50	50	47	44
	63A	63	63	63	63	63	63	63	60	57	54
A4	80A	80	80	80	80	80	80	80	80	76	72
	100A	100	100	100	100	100	100	99	94	89	84

N.B. Ratings below 16 Amps will carry rated circuit up to 80°C

Table 2:

Voltage ratings and breaking capacity

Fuselink reference	Current rating	Voltage rating		Breaking capacity	
		a.c.	d.c.	a.c.	d.c.
NS & A1	2-20A	550V	250V	80kA	40kA
NS & A1	25-32A	415V	250V		
A2	6-32A	660V	250V		
A3	50-63A	660V	250V		
A4	80-100A	660V	400V		

Table 3: **Dimensions (give as maxima as defined by BS88: 1975)**

Fuselink Reference	Fixing Centres (Nominal)		Maximum Bolt Size	Overall Length (Max)		Diameter (Max)		Width of Tag (Max)	
	mm	in		mm	in	mm	in	mm	in
NS	Blade		—	60	2⅜	14.5	9/16	13	½
A1	44.5	1¾	M4	56	2 7/32	14.5	9/16	11.2	7/16
A2	73	2⅞	M5	86	3⅜	24	15/16	9.2	3/8
A3	73	2⅞	M5	91	3 9/16	27	1 1/16	13	½
A4	94	3 11/16	M8	111	4⅜	37	1 7/16	20	¾

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RS data

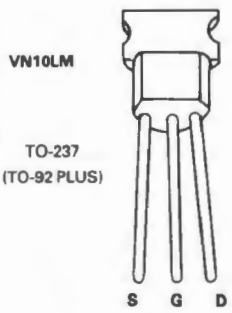
VMOS Power F.E.T.s

VMOS is the generic name for Vertical MOS. Unlike conventional MOS with the source, gate and drain on the surface of the semiconductor chip, VMOS has the source on the top and the drain, like the collector of a bipolar transistor, on the bottom for optimum heat transfer. The control gate lies in a 'V' groove which is etched into the silicon. Current flows vertically from drain to source along both sides of this V-groove 'gate' but only when a potential 'excites' the gate. VMOS is an enhancement mode MOSFET which is effectively 'fail-safe', as no bias means no current flow. This type of construction facilitates production of high voltage, high current F.E.T.s.

A range of four N channel enhancement mode VMOS Power F.E.T.s, in conventional transistor packages, and 14 pin dual-in-line package housing 4 N channel enhancement mode VMOS Power F.E.T.s are available.

WARNING ESD SENSITIVE DEVICES

ESD (Electro-Static-Discharge) sensitive devices. The input gate-source must be protected from voltages that are higher than the permissible limits stated in the data sheet. Users, are therefore cautioned to avoid build-up of electrostatic charge by observing reasonable precautions during handling and installation of devices. Furthermore, during designs of circuits it must be ensured that the devices are never operated with open gate-source connections.



Connections

Absolute maximum ratings

Stock No.	295-141	295-107	295-113	295-129	295-135
Part No.	VQ1000J	VN10LM	VN46AF	VN66AF	VN88AF
Maximum Drain-Source Voltage	60V	60V	40V	60V	80V
Maximum Drain-Gate Voltage	60V	60V	40V	60V	80V
Maximum Continuous Drain Current	0.3A	0.5A	2.0A	2.0A	2.0A
Maximum Pulsed Drain Current	1.0A	1.0A	3.0A	3.0A	3.0A
Maximum Gate-Source Voltage	±30V	±30V	±30V	±30V	±30V
Maximum Dissipation at 25°C Ambient Temperature	1.2W	1W	15W	15W	15W
Linear Derating Factor	9.6mW/°C	8mW/°C	120mW/°C	120mW/°C	120mW/°C
Maximum Operating Temperature Range			−40°C to +150°C		
Maximum Storage Temperature Range			−40°C to +150°C		

Electrical characteristics (25°C unless otherwise noted)

NOTES: 1. Pulse test – 80μs pulse. 1% duty cycle. 2. Sample test.

	Characteristic		Test Conditions	VQ1000J			VN10LM			VN46AF			VN66AF			VN88AF			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
STATIC	BV_{DSS}	Drain Source Breakdown	VGS = 0.VQ 100CJ VN1OLM I_D = 500μA. VN 46.66.88AF I_D = 500μA	60			60			40			60			80			
			V_{GS} = 0.I_D = 2.5mA	–			–			40			60			80			V
	$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}.I_D = 1mA	0.8			0.3		2.5	0.8	1.7		0.8	1.7		0.8	1.7		
	I_{GSS}	Gate Body Leakage	VGS = 10V. V_{DS} = 0			10			10		0.01	10		0.01	10		0.01	10	
			V_{GS} = 10V. V_{DS} = 0.T_A = 125°C (Note 2)			–			–			100			100			100	
			V_{DS} = Max Rating. V_{GS} = 0			100			10			10			10			10	μA
	I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 0.8 Max Rating. V_{GS} = 0. T_A = 125°C (Note 2)			–			–			100			100			100	
			V_{DS} = 25V. V_{GS} = 0			–			–		100			100			100		nA
	$I_{D(on)}$	ON-State Drain Current (Note 1)	V_{DS} = 25V. V_{GS} = 10V	0.5			0.5			1.0	2		1.0	2		1.0	2		A
	$V_{DS(on)}$	Drain-Source Saturation Voltage (Note 1)	V_{GS} = 5V. I_D = 0.1A (VQ 1000CJ: I_D = 0.2A)			1.5			–		0.3			0.3			0.4		
			V_{GS} = 5V. I_D = 0.3A			–			–		1.0	1.5		1.0	1.5		1.4	1.7	V
			V_{GS} = 10V. I_D = 0.5A (VQ 1000 : I_D = 0.3A)			1.65			2.5		1.0			1.0			1.3		
			V_{GS} = 10V. I_D = 1.0A			–			–		2.0	3.0		2.0	3.0		3.0	4.0	
	gm	Forward Transconductance (Note 1)	VN46, 66, 88 V_{DS} = 24V. I_D = 0.5A / VQ1000 VN1OLM V_{DS} = 15V.I_D = 0.5A	100			100	200		150	250		150	250		150	250		mΩ
DYNAMIC	C_{iss}	Input Capacitance (Note 2)	V_{GS} = 0. V_{DS} = 25V. f = 1.0MHz		50			48				50			50			50	
	C_{rss}	Reverse Transfer Capacitance (Note 2)			3			2				10			10			10	pF
	C_{oss}	Common-Source Output Capacitance (Note 2)			20			16				50			50			50	
	$t_{d(on)}$	Turn-ON Delay Time	VN1OLM. VQ 1000 : I_D = 0.3A R_L = 23Ω. R_S = 50Ω VN46, 66, 88AF : I_D = 0.95A R_L = 23Ω. R_S = 50Ω			10		10			2	5		2	5		2	5	
	t_r	Rise Time (Note 2)				–			–		2	5		2	5		2	5	
	$t_{d(off)}$	Turn-OFF Delay Time (Note 2)				10		10			2	5		2	5		2	5	ns
	t_f	Fall Time (Note 2)				–			–		2	5		2	5		2	5	

General information

Of the advantages that VMOS has compared to bipolars, many are well known in small signal applications but many others are apparent only at higher power levels. They include:

1. High input impedance – low drive current (typically less than 100nA). The 'beta' of a VMOS device is therefore over 10^9. Since the resultant drive power is negligible, VMOS will directly interface to medium high impedance drivers such as CMOS logic or opto-isolators.

2. No minority carrier storage time. VMOS is a majority carrier device – its charge carriers are controlled by electric fields, rather than the physical injection and extraction (or recombination) of minority carriers in the active region. The switching delay time is small, several nanoseconds, and is caused primarily by external parasitic elements (series gate inductance).

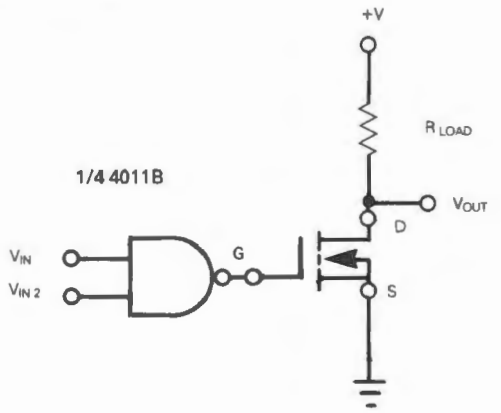
3. No failure from secondary breakdown or current hogging. Since the temperature coefficient of the VMOS drain source ON voltage is positive (a bipolar being negative), VMOS draws less current as the device heats up. If the current density increases at one particular point of the channel, the temperature rises and the current decreases. The current automatically equalises throughout the chip so no hot spots or current crowding which eventually leads to failure in a bipolar, can develop. Similarly, current is automatically shared between paralleled devices so no ballasting resistors are needed.

The high input impedance and high speed of VMOS makes it ideal as a switch – it will interface any driver capable of a 5V-30V swing to nearly any load requiring high current. Furthermore, the lack of failure from secondary breakdown means that it can withstand high voltage and high current simultaneously, so inductive loads are no problem.

Basic switching applications

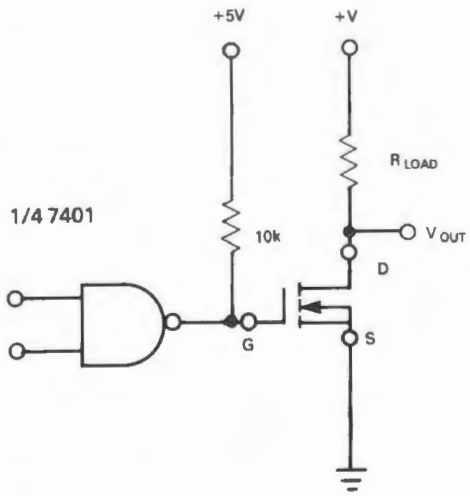
CMOS logic makes an ideal driver for VMOS since no interface components are required (see Figure 1). A logic low to the input of the 4011B turns ON the device while a logic turns the device OFF.

Figure 1 **Basic switch**



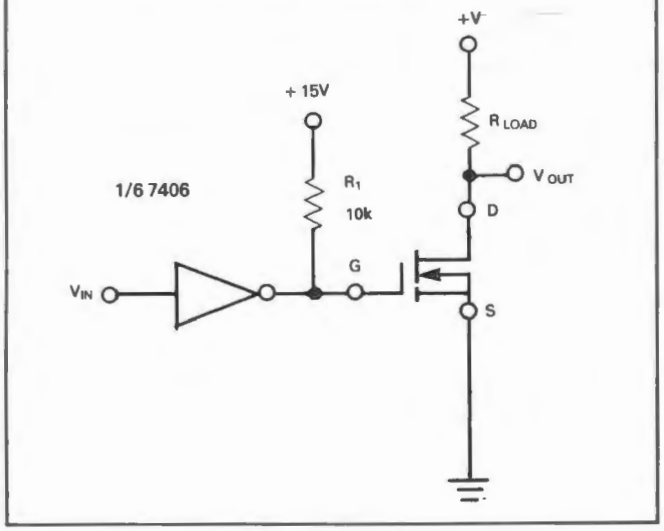
The switching speed is increased when several CMOS gates are paralleled to increase drive current to the VMOS F.E.T. VMOS will also interface to standard TTL, but a pullup resistor is needed to ensure sufficient gate enhancement (see Figure 2). If no pullup resistor is used, the enhancement to the VMOS will be a mere 3V, and the VMOS will conduct only about 200mA (assuming VN66AF is used). On the other hand, with a full 5V of enhancement on the gate of the VMOS, it will conduct approximately 500mA, which is sufficient for many applications.

Figure 2 **Basic switch with increased speed**



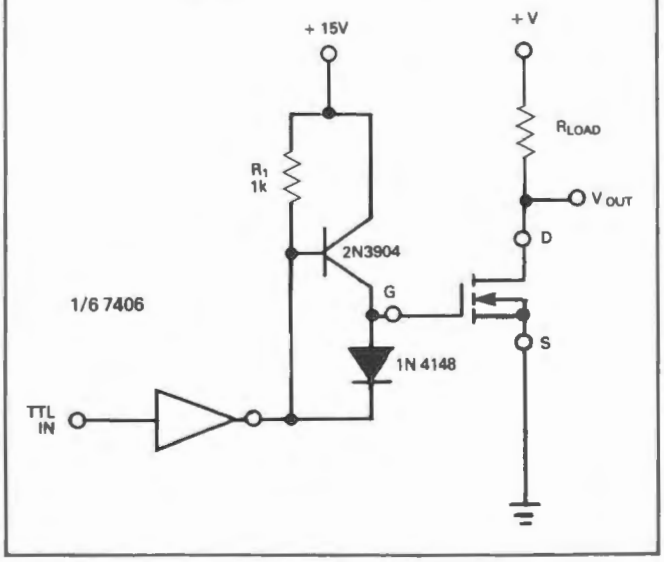
If more current or a lower ON resistance is needed, more drive voltage must be applied to the VMOS. Figure 3 shows how to use open collector TTL with a 10V or 15V supply, although now the turn-ON time will depend heavily on the value of R_1 since only this resistor provides current to charge the input capacitance of the VMOS.

Figure 3 **Open collector TTL for greater enhancement voltage**



If an extremely fast turn-ON time is needed, R_1 must be very small and therefore excessive power will be dissipated when the VMOS is OFF. To solve this problem, use the totem pole drive circuit shown in Figure 4, where the VMOS is driven by an emitter follower, effectively reducing the capacitance that R_1 must charge.

Figure 4 **Totem pole driver for increased speed and reduced dissipation**



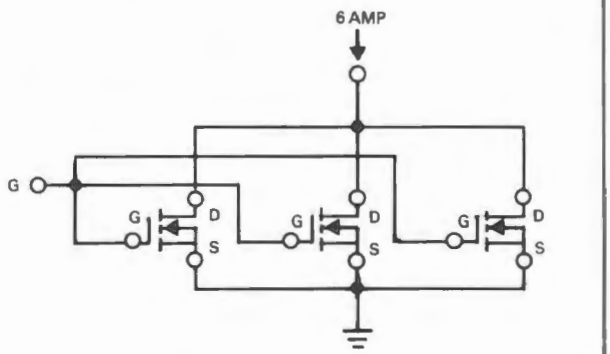
RS data

Parallel and series operation

The current handling capability of VMOS may be increased quite easily by simply paralleling several devices (Figure 5). No ballasting resistors or thermal matching networks are needed because the currents tend to equalise. If a particular device starts to draw more current, it heats up more and conducts less current than it would otherwise.

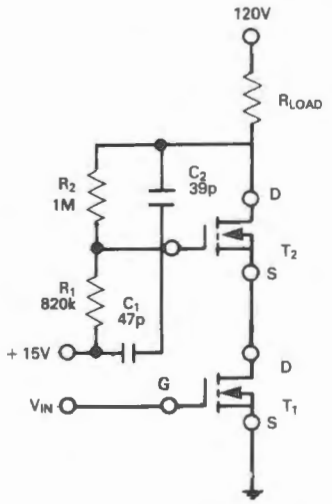
Due to the excellent high frequency response of VMOS, ferrite beads or small valued resistors (≃ 100Ω to 1000Ω) in series with each gate are recommended to suppress spurious high frequency oscillations.

Figure 5 **Parallel operation**



Devices may be connected in series to increase breakdown voltage, as shown in Figure 6. R_1 and R_2 are large because the drive current to the gate of T_2 is small, which C_1 and C_2 form a capacitive divider which dynamically balances the gate drive and also ensures fast switching times by converting charge to the gate of T_2. C_1/C_2 should be approximately equal to R_2/R_1, with allowance for stray capacitance and the enhancement voltage of T_2. The bottom of the divider chain is returned to 15V, rather than ground, to provide sufficient enhancement for T_2 when the devices are ON. By properly selecting resistor and capacitor values, any number of VMOS may be series connected in this manner.

Figure 6 **Series operation for increased breakdown voltage**



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RS data

Programmable timers RS 2240 and RS 7240

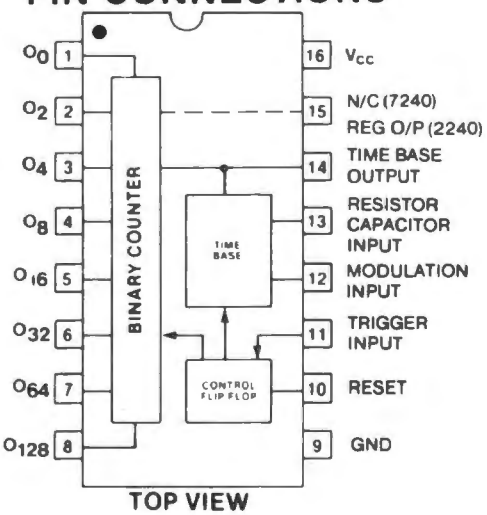
Stock numbers 308-607 & 304-582

The RS 2240 (308-607) & 7240 (304-582) are bipolar and C-MOS versions respectively of a programmable timer/counter I.C. These devices are capable of producing accurate time delays ranging from microseconds to days duration. An external RC network defines an internal timebase frequency. This frequency is fed to an 8 bit counter which can be externally programmed to provide an output in 1 RC steps from 1 RC to 255 RC. Monostable or astable operation is possible allowing 255 frequencies or pulse patterns to be generated. The output can be synchronised to an external signal and a modulation input can be used to generate a frequency modulated output. These versatile devices will find many applications ranging from simple time delay functions to sophisticated sequential timing controllers and bit pattern generators, etc.

Features

- Accurate timing from microseconds to days
- Programmable delays from 1 RC to 255 RC
- TTL DTL and CMOS compatible outputs
- Timing directly proportional to RC time constant
- High accuracy −0.5% (2240); 5% (7240)
- External sync and modulation capability
- Wide supply voltage range
- Cascadeable

PIN CONNECTIONS



TOP VIEW

Absolute maximum ratings[2]

	2240	7240
Supply Voltage	18V	18V
Input Voltage[1]		
Terminals 10, 11, 12, 13, 14,	N/A	GND −0.3V to V⁺ +0.3V
Maximum continuous output current (each output)	10 mA	50 mA
Output Voltage	18V	18V
Regulator Output Current	5 mA	N/A
Power Dissipation at 25°C	650 mW	200 mW
(Derating above 25°C)	(5.3 mW/°C)	(2 mW/°C)
Operating Temperature Range	0°C to 70°C	−20°C to 85°C

NOTES:

1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the 7240 be turned on first.

2. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. Timing error solely introduced by i.c. measured as % of ideal time-base period of T = 1.00 RC.

4. Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

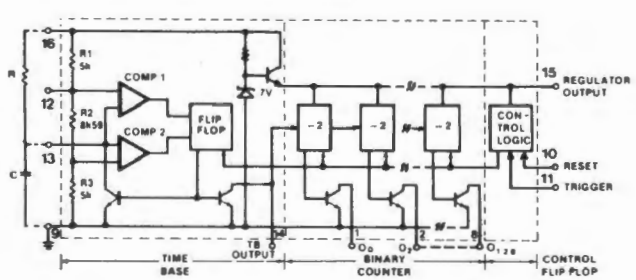
Electrical Characteristics

V & V_{CC} = 5V, T_A = 25°C, R = 10kΩ, C = 100nF, unless otherwise noted

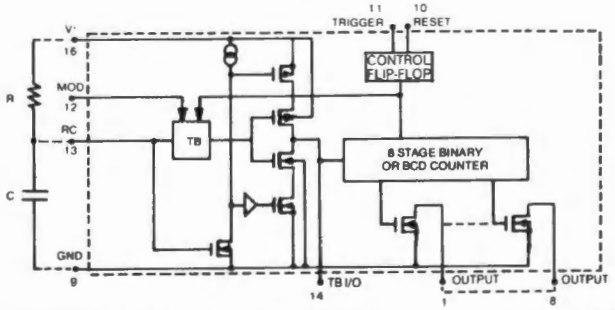
PARAMETER	CONDITIONS	2240 MIN	2240 TYP	2240 MAX	7240 MIN	7240 TYP	7240 MAX	UNITS
General Characteristics								
Supply Voltage V_{CC} & V⁺	For V_{CC} 4.5V, Short Pin 15 to Pin 16 on 2240 only	4		15	2		16	V
Supply Current (7240)	Reset					125		μA
	Operating, R 10KΩ, C 100 nF					300	700	μA
	Operating, R 1MΩ, C 100 nF					120	500	μA
	TB Inhibited, RC Connected to GND					125		μA
Supply Current (2240)	V_{CC} 5V, V_{TR} O, V_{RS} 5V		4	7				mA
Total Circuit	V_{CC} 15V, V_{TR} O, V_{RS} 5V		13	18				mA
Counter only			15					mA
Regulator O/P. V_{REG}	Measured at pin 15, V_{CC} 5V	3.9	4.4					V
	V_{CC} 15V	5.8	6.3	6.8				V
Time Base Section								
Timing Accuracy (note 3)	V_{RS} O, V_{TR} 5V		0.5	5		5		%
Temperature Drift RC Oscillator	V_{CC} 5V, 0°C < T_J < 70°C		200			250		ppm/°C
	V_{CC} 15V, 0°C < T_J < 70°C		80					ppm/°C
Drift with Supply	V_{CC} = 8V see Fig 20		0.08	0.3	see Fig 22			%/V
Max. Frequency	R 1KΩ, C 7nF		130					kHz
Modulation Voltage Level	V_{CC} 5V (measured at pin 12)	2.80	3.50	4.20		3.5		V
	V_{CC} 15V		10.5			11.0		V
Output Voltage	I source = 1 mA				3.5	4.2		V
	I sink = 3.2 mA					0.25	0.6	V
Leakage Current	RC to GND						25	μA
Timing Resistor Range	see Figs 4a & 4b	1K		10M	1K		22M	Ω
Timing Capacitor Range		10n		1,000μ	10p			F
Trigger/Reset Control								
Trigger	Measured at pin 11, V_{RS} O							
Trigger Threshold			1.4	2.0		1.6	2.0	V
	V⁺ 15V					3.5	4.5	V
Trigger Current	V_{RS} O, V_{TR} 2V		10					μA
Impedance			25					kΩ
Response Time (note 4)			0.8					μs
Reset	Measured at pin 10, V_{TR} O							
Reset Threshold			1.4	2.0		1.3	2.0	V
	V⁺ 15V					2.7	4.0	V
Reset Current	V_{TR} O, V_{RS} 2V		10					μA
Impedance			25					kΩ
Response Time (note 4)			0.8					μs
Trigger/Reset Input Resistors (7240)	Pull down					50K		Ω
Counter Section								
Max. Toggle Rate	V_{RS} O, V_{TR} 5V, Measured at pin 14		1.5					MHz
	V⁺ 2V, Counter/Divider Mode					1		MHz
	V⁺ 5V, Counter/Divider Mode				2	6		MHz
	V⁺ 15V, Counter/Divider Mode					13		MHz
	50% Duty Cycle Input with Pk-Pk Voltages Equal to V⁺ & GND							
	Programmed Timer - Divider Mode						100	kHz
Input Impedance			20					kΩ
Input Threshold		1.0	1.4					V
Outputs	Measured at pin 1 - 8							
Rise Time	R_L = 3kΩ, C_L 10pF		180					ns
Fall Time			180					ns
Sink Current	V_{OL} = 0.4V	2	4					mA
Leakage Current	V_{OH} = 15V		0.01	15				μA
	V⁺ 5V, per output						1	μA
Saturation Voltage	All O/P's except TB O/P, V⁺ 5V, I_{OUT} 3.2 mA					0.22	0.4	V

Figure 1a **Block diagrams**

RS2240



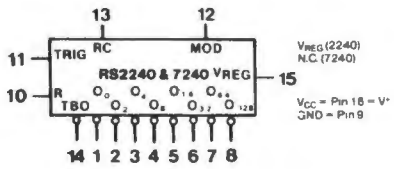
RS7240



Circuit description

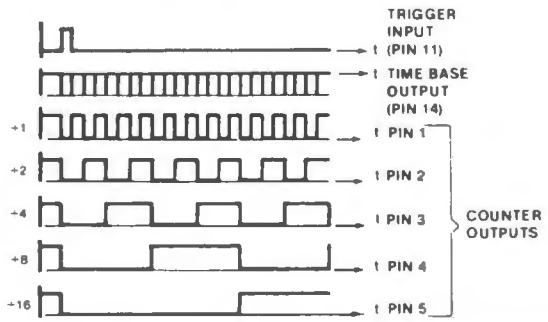
Connection of the supply with no trigger or reset inputs sets the counter outputs O_0 to O_{128} HIGH.

Figure 1b **Circuit symbol**



Application of a positive-going trigger pulse to TRIG, pin 11, initiates the timing cycle. The Trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW.
The time-base oscillator generates timing pulses with a period T=RC where T is in seconds for R in Ohms and C in Farads. These pulses are transferred to the binary counter section.
The timing sequence is completed when a positive going reset pulse is applied to R, pin 10, which disables the time base and counter sections and returns the counter outputs to a HIGH state.
Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.
Figure 2 shows the timing sequence of output waveforms at various terminals of the device subsequent to a trigger input.

Figure 2 **Timing diagram of output waveforms**

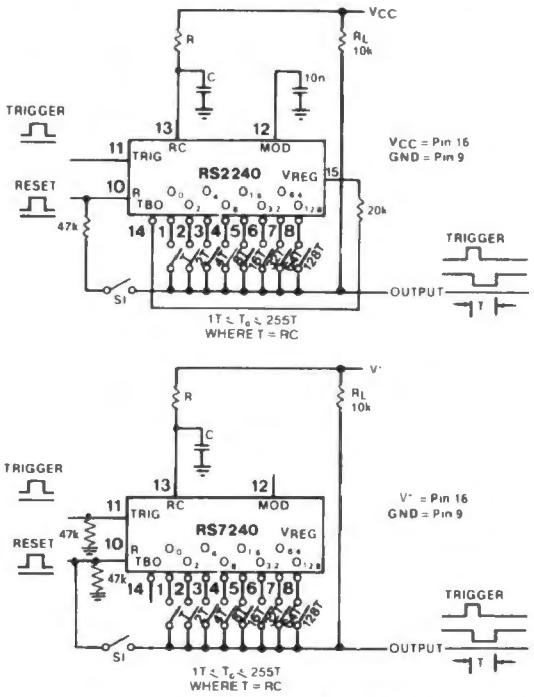


Monostable operation

Precision Timing

In precision timing applications, the timers are used in the monostable or self-resetting mode. Figure 3 shows the basic circuit connection for both types.

Figure 3 **Basic circuit connections for timing applications**
Monostables: S1 closed (Astable: S1 open)



Note: the trigger pulse should be of a shorter duration than the monostable period (2μs. min.)

The output is normally HIGH and goes LOW following a trigger input where it remains LOW for the time duration, T_0 and then returns to the HIGH state. The duration of the timing cycle T_0 is given as:

$$T_0 = NT = NRC \text{ seconds} \qquad \begin{matrix} R \text{ in } \Omega \\ C \text{ in F} \end{matrix}$$

where T=RC is the time-base period as set by the choice of timing components at RC pin 13 (see Figures 4 and 5) and N is an integer in the range of 1 $\leqslant$N. $\leqslant$255 as determined by the combination of counter outputs O_0 . . . O_{128} pin 1 through 8, connected to the output bus.

Figure 4a

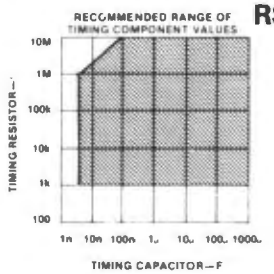


Figure 5a

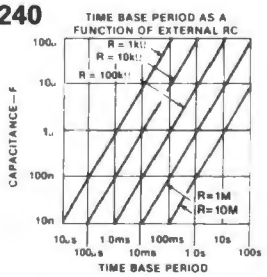


Figure 4b

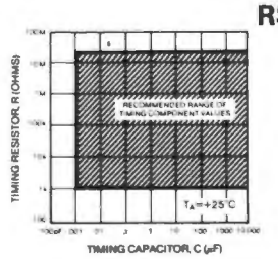
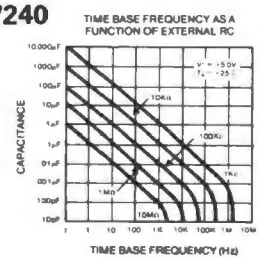


Figure 5b

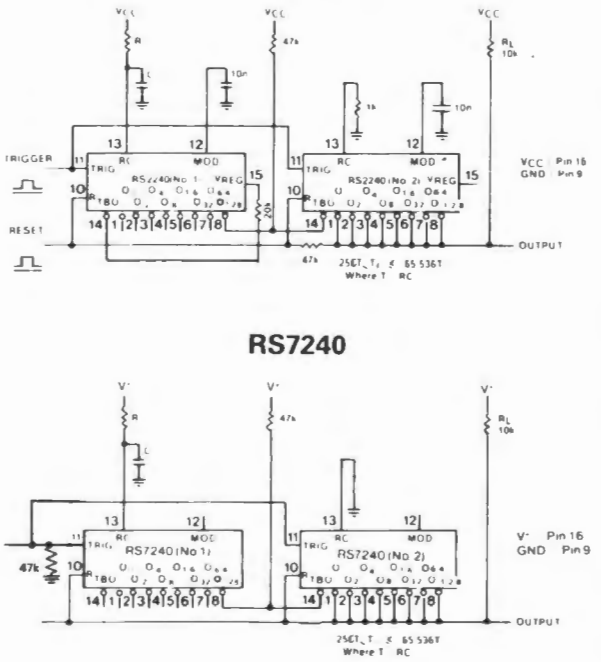


The binary-counter outputs, O_0 ... O_{128}, pins 1 through 8 are open-collector type stages (RS2240) or open drain FETs (RS7240) and can be shorted together to a common pull-up resistor to form a wired-AND connection; the combined output will be LOW as long as any one of the outputs is LOW. The time delays associated with each counter input can be added together. This is done by simply shorting the outputs together to form a common output bus as shown in Figure 3. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_0, is 32 T. Similarly, if pins 1, 5, and 6 are shorted to the output bus, the total time delay is $T_0 = (1 + 16 + 32)$. $T = 49$ T. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1T \leqslant T_0 \leqslant 255$ T.

Ultra-long time delay application

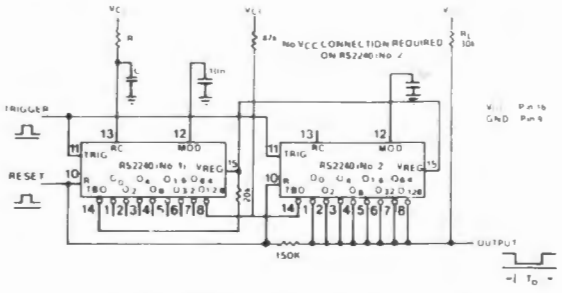
Two timers can be cascaded as shown in Figure 6 to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_0 = 256$ RC to $T_0 = 65{,}536$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the Reset and the Trigger terminals of both units are tied together and the Unit 2 time-base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator.

Figure 6 **Cascaded operation for long delays**



The provision of a regulated output, V_{REG}, on pin 15 of the RS2240 facilitates low power operation in cascaded timer applications. Figure 7 shows the circuit of figure 6, revised to reduce the power dissipation. In this case the V_{CC} terminal of the second RS2240 is unconnected and the first timer powers the second unit by connecting the V_{REG} pins of both devices together.

Figure 7 **Low power operation of cascaded timers**

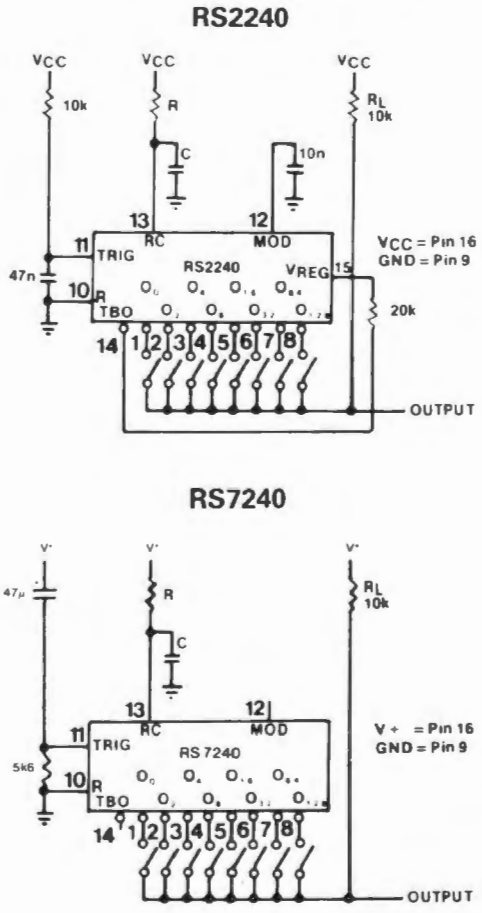


Astable operation

The timers can be operated in their astable or free-running mode by disconnecting the Reset terminal (pin 10) from the counter outputs. Omitting switch S1 in Figure 3 produces astable operation. The timer starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its Reset state.

The circuit of Figure 8 is designed for continuous operation. It self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely. In astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Figure 8 **Free-running or continuous operation**



Binary pattern generation

In astable operation, as shown in Figure 3, the output of the timers appear as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 2 which shows the phase relations between the counter outputs. Figures 9 and 10 show some of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

Figure 9 **Binary pulse patterns obtained by shorting various counter outputs**

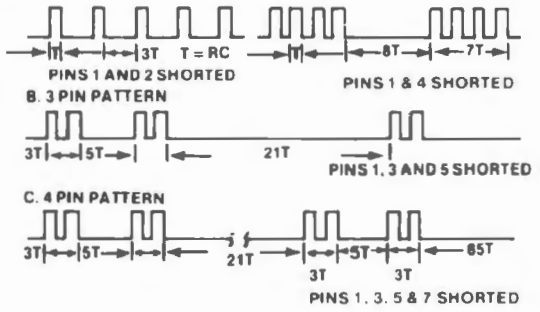
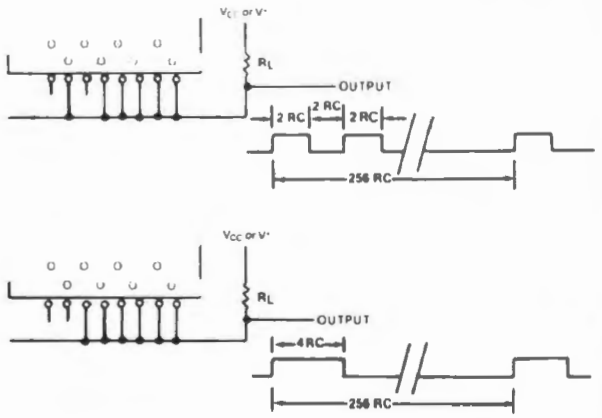


Figure 10 **Continuous free-run operation examples of output**

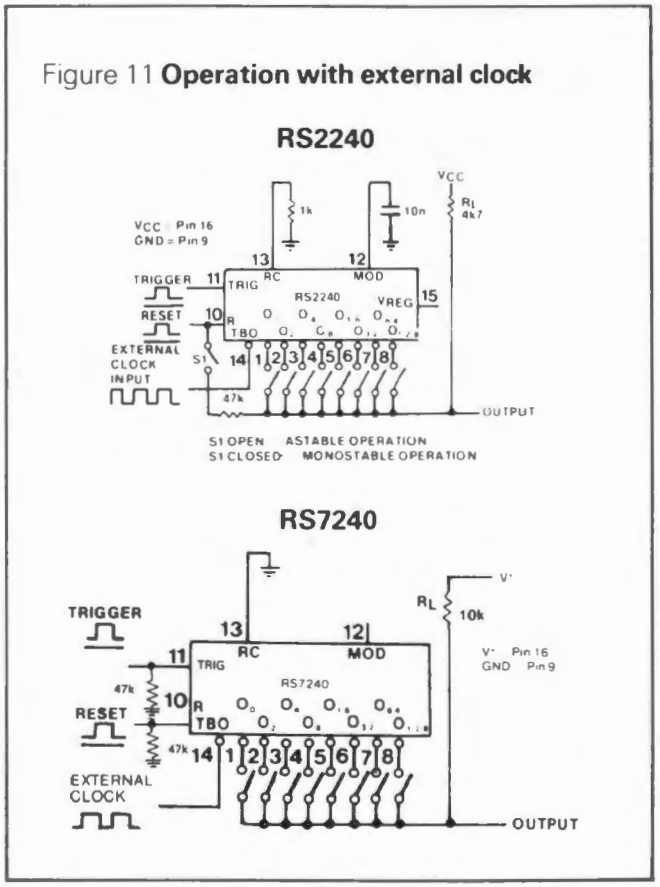


Operation with external clock

The timers can be operated with an external clock or time base by disabling the internal time-base oscillator and applying the external clock input to TBO, pin 14. The recommended circuit connection for this application is shown in Figure 11. The internal time-base is de-activated by connecting a 1 kΩ resistor from RC, pin 13, to ground (2240) or pin 13 directly to ground (7240). The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3V is required. Minimum external clock pulse width must be $\geqslant 1\mu s$ (2240), $\geqslant 10\mu s$ (7240).

For low power operation with supply voltages of 6V or less, the internal time-base section can be powered down by connecting V_{CC} to pin 15 and leaving pin 16 open (2240 only). In this configuration, the internal time-base does not draw any current and the overall current drain is reduced by ≈3mA.

Figure 11 **Operation with external clock**



Used as a straight binary counter the RS7240 is significantly faster than the bipolar RS2240. However, when using this device as a programmable counter the maximum frequency of operation is reduced by more than an order of magnitude. For any division ratio other than 256 the maximum input frequency must be limited to approximately 100 kHz or less (with V⁺ equal to +5 volts). The reason for this is two-fold:

a. Since Ripple counters are used, there is a propagation delay between each individual ÷2 counter, 8 counters in all. Outputs from the individual ÷2 counters are AND'ed together to provide the output signal and the Reset/Trigger signal.

b. There must be a delay of the positive going output to the Reset terminal, (pin 10) and the Trigger terminal (pin 11). The Reset signal must therefore be generated first, and from this signal another signal is obtained through a delay network. The trigger overrides Reset.

The delay between Trigger and Reset is generated by the single RC network consisting of the 56kΩ resistor and the 330pF capacitor.

The delay caused by the counter Ripple delays can be as long as 2μs (5 volt supply), and the delay between Reset and Trigger should be at least 2μs. The sum of these two delays cannot be greater than one-half of the input clock period for reliable operation.

Frequency synthesizer

The programmable counter section of the timers can be used to generate 255 discrete frequencies from a given time-base output setting using the circuit connection of Figure 12. The circuit output is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) T where N is the programmed count in the counter. The modulus N is the total count corresponding to the counter outputs connected to the output bus. For example, if pins 1, 3 and 4 are connected together to the output bus, the total count is N=1 + 4 + 8=13; and the period of the output waveform is equal to (N + 1) T or 14T. In this manner, 255 different frequencies can be synthesized from a given time-base setting.

Synthesis with harmonic locking

The harmonic synchronization feature of the RS2240 & RS7240 time-base can be used to generate a wide number of discrete frequencies from a given input frequency. The circuit connection for this application is shown in Figure 13 (see Figure 14 for external sync waveform and harmonic capture range).

The time-base can be synchronized by setting the time-base period T to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the time components R and C at pin 13 such that:

$$T=RC=(T_S/m)$$

where

m is an integer, $1<m<10$

Figure 14 gives the typical pull-in range for harmonic synchronization for various values of harmonic modulus, m. For $m\leq 10$, typical pull-in range is greater than ±4% of time-base frequency.

The frequency f_O of the output waveform in Figure 13 is related to the input reference frequency f_R by

$$\frac{1}{T_O}=f_O=f_R\cdot\frac{m}{(N+1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1\leq N\leq 255$, the circuit of Figure 13 can produce 2550 different frequencies from a single fixed reference.

Figure 12 **Frequency synthesis from internal time-base**

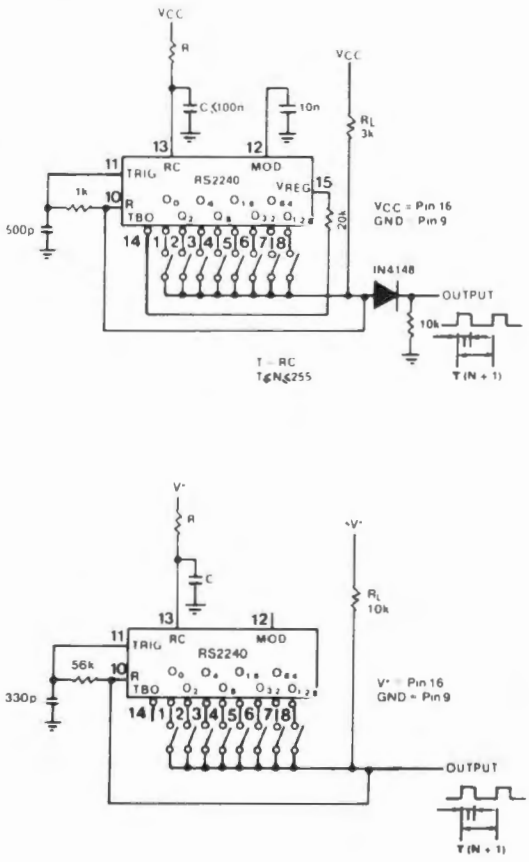
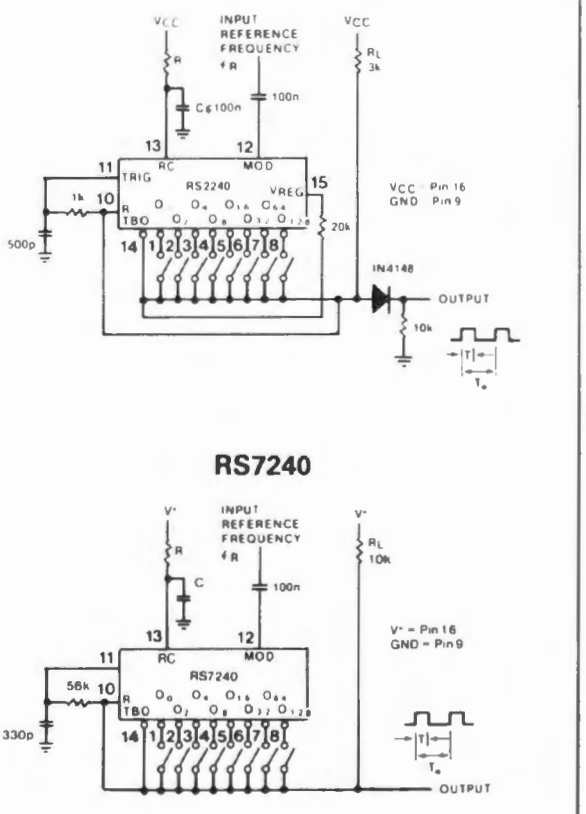


Figure 13 **Frequency synthesis by harmonic locking to an external reference**



The circuit of Figure 13 can be used to generate frequencies which are not harmonically related to a reference input. For example, by selecting the external RC to set m=6 and setting N=4 a 60Hz output frequency synchronized to 50Hz mains frequency can be obtained.

Figure 14 **Typical pull-in range for harmonic synchronization and sync waveform**

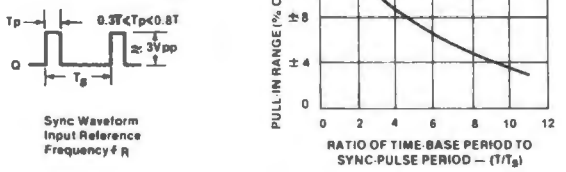
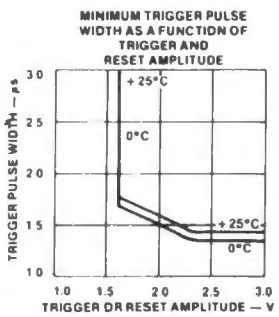


Figure 15 Figure 16

RS2240



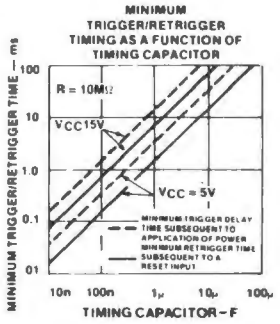
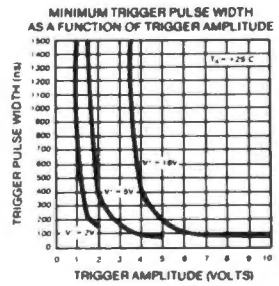
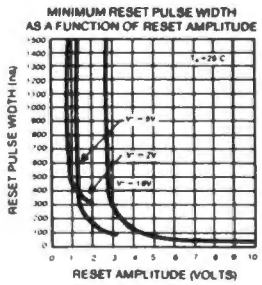


Figure 17 Figure 18

RS7240





Circuit controls

Counter outputs (O_0 . . . O_{128} pins 1 to 8)

The binary counter outputs are buffered open-collector type stages (2240), or open drain FET's (7240), as shown in the block diagram (Figure 1a). Each output is capable of sinking 2 mA at 0.4 V V_{OL} (2240) or 3.2 mA at 0.22 V V_{OL} (7240). In the Reset condition, all the counter outputs are HIGH or in the non-conducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of Figure 2. The counter outputs can be used individually, or can be connected together in a wired-AND configuration, as described in the Monostable Operation section.

Reset and trigger inputs (R and TRIG, pins 10 and 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11 respectively. The threshold level for these contols is approximately two diode drops (≈1.4V) above ground. Minimum pulse widths for the reset and trigger inputs of the 2240 are shown in Figure 15. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.
Figure 16 shows the minimum trigger/retrigger timing for the 2240 in relation to the timing capacitor value. Figures 17 & 18 show minimum trigger pulse width as a function of trigger amplitude and minimum reset pulse width as a function to reset amplitude respectively for the 7240 timer.

Modulation and sync input (MOD, pin 12)

The oscillator time-base period, T, can be modulated by applying a d.c. voltage to MOD, pin 12 (see Figure 19). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, pin 12, as shown in Figure 14. Recommended sync pulse widths and amplitudes are also given.

RC terminal (pin 13)

The time-base period T is determined by the external RC network connected to RC, pin 13. When the time base is triggered, the waveform at pin 13 is an exponential ramp with a period T=1.0 RC.

RS data

Time-base output (TBO, pin 14)
The time-base output of the 2240 is an open-collector type stage as shown in the block diagram (Figure 1a) and requires a 20kΩ pull-up resistor to pin 15 for proper circuit operation. The time-base output of the 7240 is normally left open unless used as an input or output port, it should only be used as an input terminal if pin 13 (RC) is connected to GND (see Figure 11). In the Reset state, the time-base output is HIGH. After triggering, it produces a negative-going pulse train with a period T=RC, as shown in the diagram of Figure 2. The time-base output is internally connected to the binary-counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative-going edge of the timing or clock pulses generated at TBO, pin 14. The trigger threshold for the counter section is ≈ + 1.4V. The counter section can be disabled by clamping the voltage level at pin 14 to ground.
When using high supply voltages (V_{CC}>7V) and a small-value timing capacitor (C<100nF) (2240 only) the pulse width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300pF capacitor from pin 14 to ground.

The variation of time-base period with supply voltage is shown in Figure 20 for the 2240 and the variation of time-base frequency with supply voltage for the 7240 is shown in Figure 22. The maximum divider frequency V_S supply voltage for the 7240 is shown in Figure 21.

Figure 19 Figure 20

RS2240

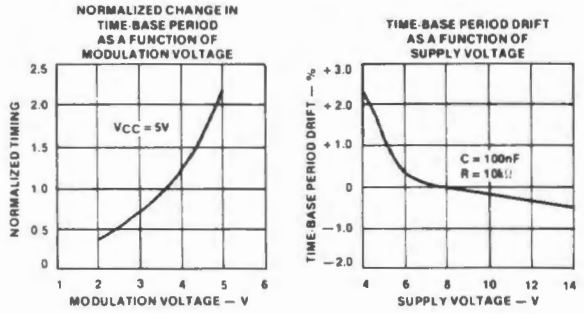
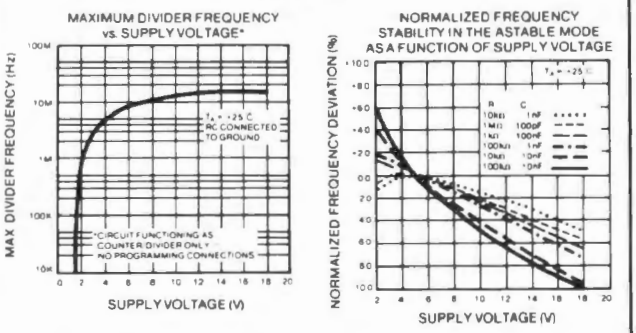


Figure 21 Figure 22

RS7240



Regulator output (V_{REG}, pin 15) (RS2240 only)
The regulator output V_{REG} is used internally to drive the binary counter and the control logic. This terminal can also be used as a supply to additional RS2240 circuits when several timer circuits are cascaded (see Figure 7) to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal to power down the internal time-base and reduce power dissipation. When supply voltages less than 4.5V are used with the internal time-base pin 15 should be shorted to pin 16.

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RS data

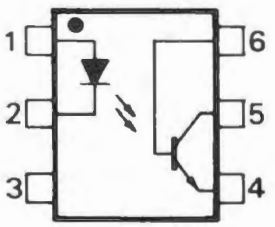
Opto isolators and opto coupled SCR/triacs

Four infra-red light emitting diode and silicon phototransistor couplers consisting of: (1) A single Opto Isolator in dual-in-line package suited for fast signal transfer and offering excellent noise immunity. (2) A single Opto Isolator also in a 6 pin dual-in-line package suited for fast signal transfer and offering a high transfer ratio and a darlington transistor output for greater drive capability which will respond to low power signal sources. (3) A dual Opto Isolator having two isolated light emitting diode-photo transistor couplers in one 8 pin dual-in-line Package. (4) A quad Opto Isolator having 4 isolated light emitting diode-photo transistor couplers in one 16 pin dual-in-line package. These last two items offer space and cost saving when multiple isolation is required. In addition an opto-coupled SCR and two opto-coupled triacs are available in 6-pin DIL packages. See pages 4 and 5. All of these couplers offer high voltage and AC isolation and are suited for interface applications in TTL and analogue circuits.

Phototransistor opto isolators

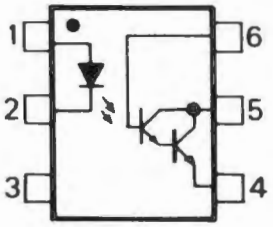
Pin configurations

Single Opto Isolator (307-979)



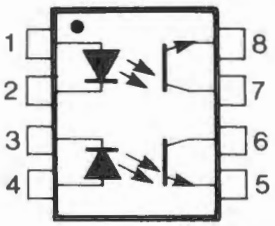
TOP VIEW

Darlington Opto Isolator (307-963)



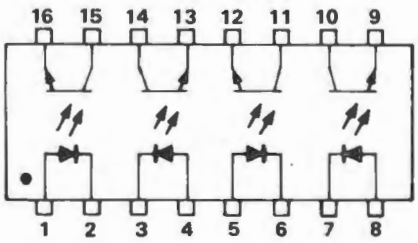
TOP VIEW

Dual Opto Isolator (308-613)



TOP VIEW

Quad Opto Isolator (307-064)



TOP VIEW

Ratings	Single Opto Isolator (307-979)	Darlington Opto Isolator (307-963)	Dual Opto Isolator (308-613)	Quad Opto Isolator (307-064)
Isolation voltage (dc)	±4000V	±4000V	±1500V	±1500V
V_{CE} (max) Transistor (dc)	30V	30V	30V	30V
I_F (max) Diode (dc)	60mA	60mA	60mA	60mA
DC Current transfer Ratio (min)	20%	300%	12.5%	12.5%
	6-pin DIL packages with transistor connection for biasing.		8-pin DIL package	16-pin DIL package

Absolute maximum ratings	Single Opto Isolator (307-979)	Darlington Opto Isolator (307-963)	Dual Opto Isolator (308-613)	Quad Opto Isolator (307-064)	Unit
T_A TEMPERATURE RANGE	−55 to +100	−55 to +100	−55 to +100	−55 to +100	°C
INPUT TO OUTPUT ISOLATION VOLTAGE	±4000	±4000	±1500	±1500	V
INPUT DIODE					
FORWARD DC CURRENT	60	60	60	60	mA
REVERSE DC VOLTAGE	3	3	3	3	V
POWER DISSIPATION					
derate at 1.33W/°C above 25°C	100	100	100	100	mW
OUTPUT TRANSISTOR					
COLLECTOR – EMITTER VOLTAGE	30	33	20	20	V
EMITTER – COLLECTOR VOLTAGE	5	5.2	7	7	V
POWER DISSIPATION					
derate at 2.0W/°C above 25°C	150	150	150	150	mW
TOTAL PACKAGE DISSIPATION					
derate at 5.33W/°C above 25°C	—	—	400	—	mW
derate at 6.67W/°C above 25°C	—	—	—	500	mW

Electrical characteristics Ta = 25°C

Parameter	Test conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
DIODE														
V_F	I_F = 10mA		—				1.5		—			—		V
	I_F = 20mA			1.5		—			—			—		V
	I_F = 60mA		—			—			1.3			1.3		V
I_R	V_R = 3V			10			100		0.1			0.1		μA
TRANSISTOR														
BV_{CEO}	I_C = 1mA	30				—		10			10			V
	I_C = 100μA		—		30				—			—		V
BV_{ECO}	I_E = 10μA	5				—			—			—		V
	I_E = 100μA		—		5				—			—		V
B_{VCBO}	I_C = 10μA	70				30			—			—		V
I_{CEO} DARK CURRENT	V_{CE} = 5V I_F = 0		—			—			5	500		5	500	nA
	V_{CE} = 10V I_F = 0 H = 0		5	50			100		—			—		nA
I_{CBO}	V_{CE} = 10V I_E = 0			20			50		—			—		nA
h_{FE}	V_{CE} = 5V I_C = 100μA	100	200			20k			—			—		
C_{CE}	V_{CE} = 0		8			5			2			2		pF
COUPLED														
I_C/I_F DC CURRENT	I_F = 10mA V_{CE} = 2V	20			300				—			—		%
TRANSFER RATIO	I_F = 16mA V_{CE} = 5V		—			—		12.5	35		12.5	35		%
R_{ISO} ISOLATION RESISTANCE	V = 500V	10^{11}			10^{11}				10^{11}			10^{11}		Ω
$V_{CE(SAT)}$	I_F = 10mA I_C = 10mA		—			1			—			—		V
	I_F = 16mA I_C = 2mA			0.4		—			0.5				0.5	V
C I/O INPUT/OUTPUT CAPACITANCE			2			0.5			0.5			0.5		pF
t_r RISE TIME	V_{CE} = 10V, I_B = O, I_F = 10mA		2			—			—			—		μs
	V_{CE} = 10V, R_L = 100Ω,													
	I_F = 10mA		—			3			—			—		μs
	V_{CE} = 10V, R_L = 100Ω.													
	I_F = 8mA		—			—			2			2		μs
t_f FALL TIME	V_{CE} = 10V, I_B = 0, I_F = 10mA		2			—			—			—		μs
	V_{CE} = 10V, R_L = 100Ω,													
	I_F = 10mA		—			25			—			—		μs
	V_{CE} = 10V, R_L = 100Ω,													
	I_C = 8mA		—			—			2			2		μs

Figure 1

Response time vs base resistance for 307-979

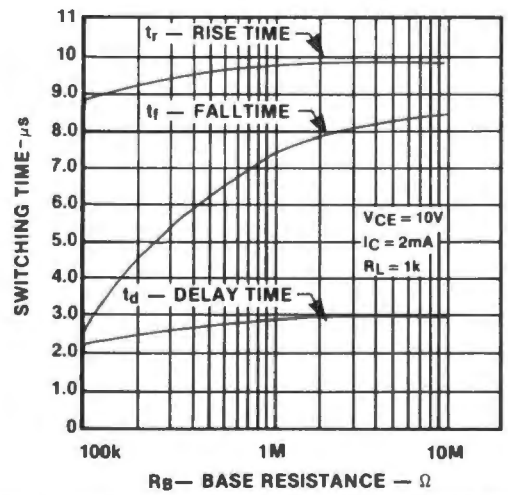


Figure 2

Rise and fall time vs load resistance for 307-979

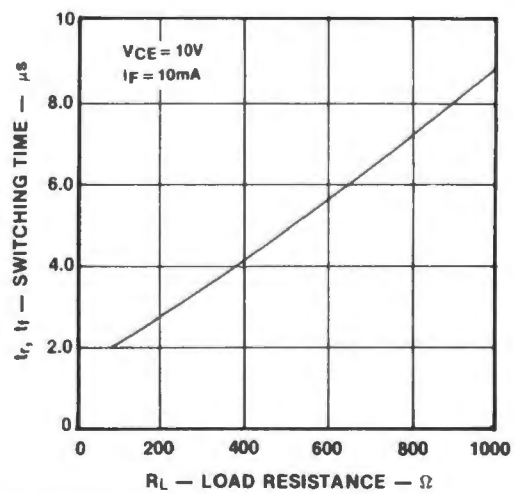
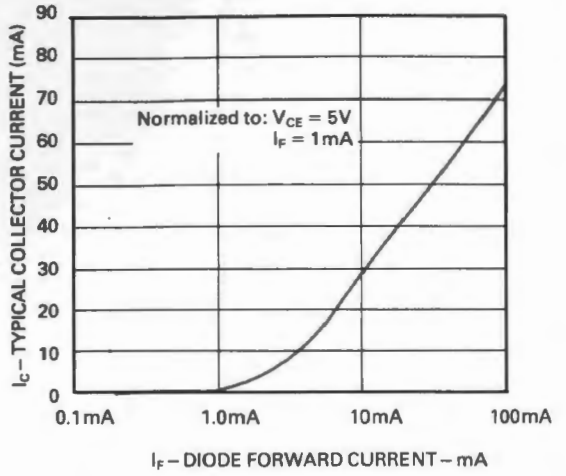
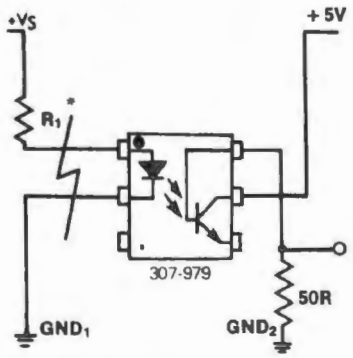


Figure 3 **Typical collector current vs diode forward current for 307-963**



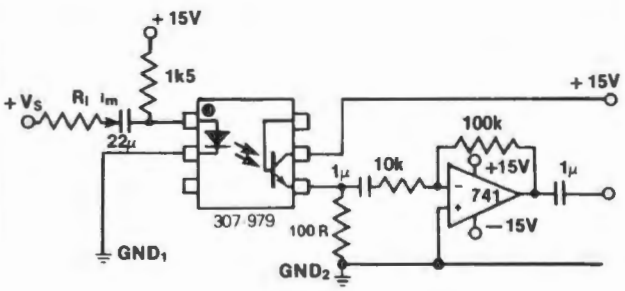
Applications

Figure 4 **Fast pulse transfer**



This mode of operation increases switching speed from about 2μs to about 100ns but reduces current transfer ratio to about 0.2%

Figure 5 **A.C. signal isolation**



Choose R_i, to limit modulating current (i_m) to 5mA max. Useful frequency range in the order of 20Hz to 20kHz

Figure 6 **Light activated solid state relay**

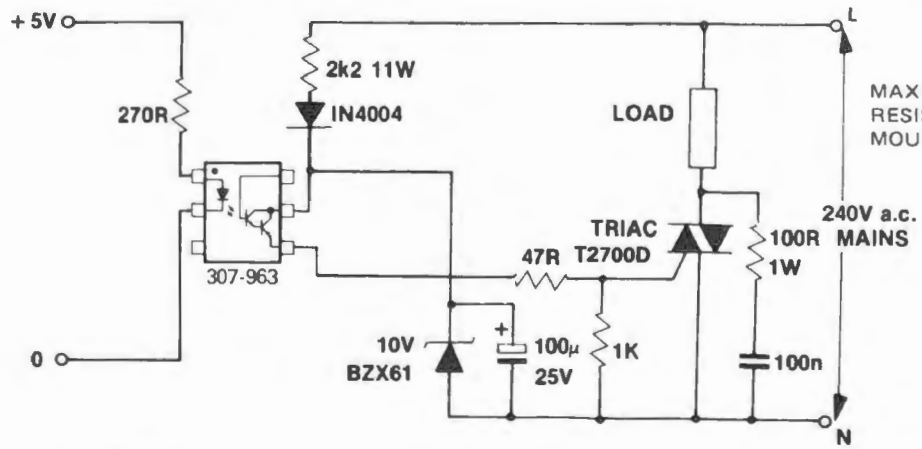
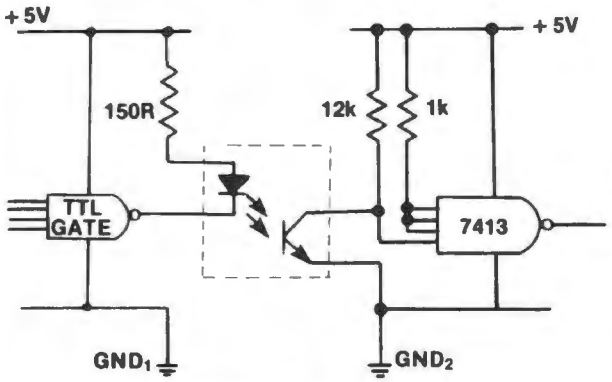
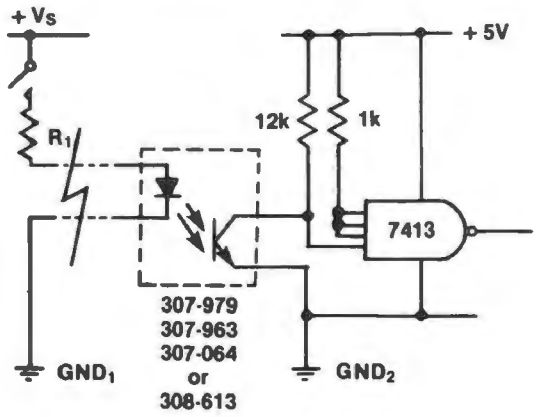


Figure 7 **TTL interface**



RECOMMENDED FOR USE WITH 307-979 or 308-613

Figure 8 **Switched input isolation offering good noise immunity**

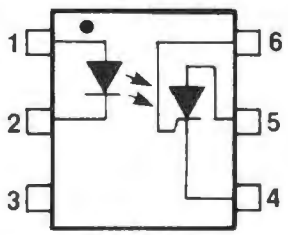


NOTE: *R_1 is chosen to limit I_F, $R_1 = \frac{V_S - V_F}{I_F}$ Where V_F—forward volts drop of diode
I_F—forward diode current
V_S—supply voltage

Opto-coupled SCR and Triacs

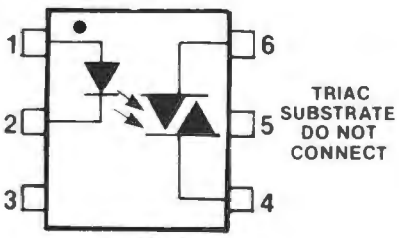
A gallium arsenide infra-red light emitting diode coupled with a light activated silicon controlled rectifier or triac in a 6 pin dual-in-line package.

Opto-Coupled SCR H11C4 (308-001)



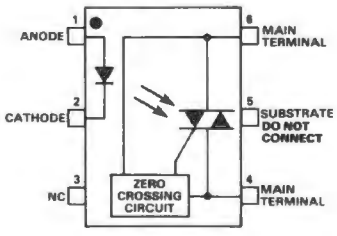
TOP VIEW

Opto-Coupled Triac 3020 (308-196)



TOP VIEW

Zero Voltage Crossing Opto-Coupled Triac 3041 (301-628)



TOP VIEW

Electrical characteristics T_A = 25°C unless otherwise stated

	308-001			308-196			301-628			
LED	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
V_F (at I_F = 10mA)	–	1.2	1.5	–	1.2	1.5	–	1.2	1.5	V
I_R (at V_R = 3V)	–	–	10	–	0.05	100	–	–	100	μA
Output switch (SCR or triac)										
V_{DRM}	400	–	–	400	–	–	400	–	–	V
V_{RRM}	400	–	–	400	–	–	400	–	–	V
V_{TM}	–	1.1 (I_{TM} = 0.3A)	1.3	–	2.5 (I_{TM} = 0.1A)	3.0	–	1.75	3.0	V
I_{DRM} (at 400V V_{DRM})	–	–	150 (T_A = 100°C)	–	0.01	0.1	–	0.01	0.1	μA
I_H	–	100 (R_{GK} = 10kΩ, V_{AK} = 50V)	–	–	100 (V_{AK} = 3V)	–	–	200	–	μA
dV/dt		20 (R_{GK} = 10kΩ)			2		–	100	–	V/μs
Total device										
LED current to latch O/P switch	–	–	20 (V_{AK} = 50V, R_{GK} = 10kΩ)	–	8	15				mA
	–	–	11 (V_{AK} = 100V, R_{GK} = 27kΩ)		(V_{AK} = 3.0V, 10mA LED Drive)					
Isolation					Surge voltage (5s) 7,500V Peak					

Absolute maximum ratings T_A = 25°C unless otherwise stated

L.E.D.	**308-001**	**308-196**	**301-628**
Continuous forward current	60mA	50mA	50mA
Reverse voltage	6V	3V	6V
Output switch (SCR or triac)			
V_{DRM}	400V	400V	400V
V_{RRM}	400V	400V	400V
$I_{T(RMS)}$	300mA	100mA	100mA
I_{TSM}	5A [100μs pulse 1% duty cycle]	1.2A [10μs pulse 10% duty cycle]	1.2A [10ms pulse 10% duty cycle]
P_D	400mW [Derate 5.3 mW/°C above 25°C]	300mW [Derate 4 mW/°C above 25°C]	330mW [Derate 4.4 mW/°C above 25°C]

Figure 9 **On-state current vs maximum allowable temperature**

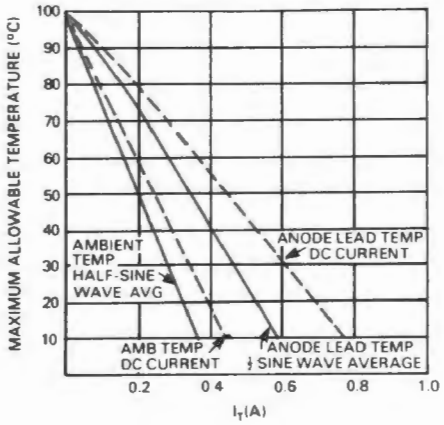
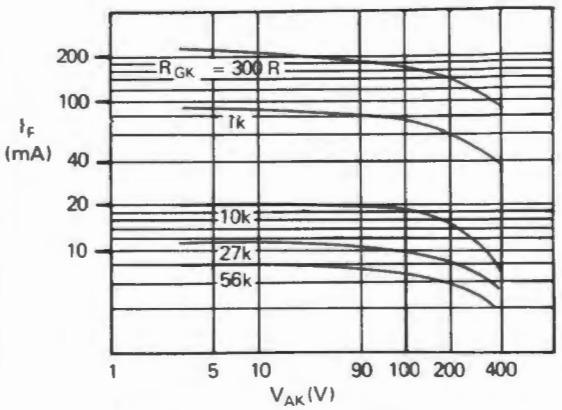


Figure 10 **Input current to trigger vs anode-cathode voltage**



R_{GK} =
GATE — CATHODE RESISTOR

Applications

Figure 11 **Lamp driver with TTL input**

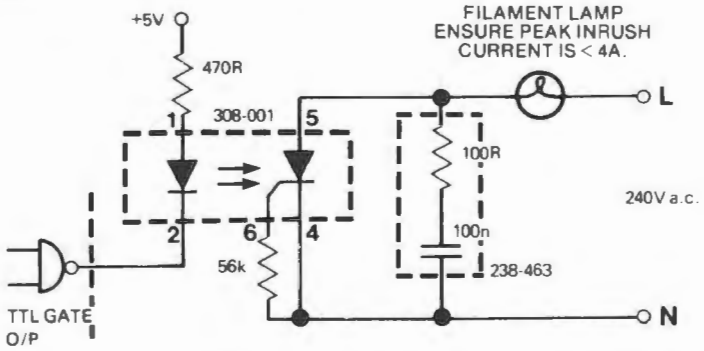
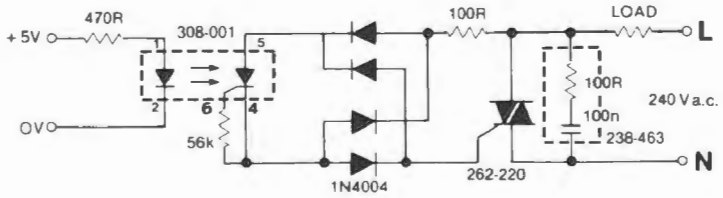


Figure 12 **Solid state relay**



Opto-coupled triac

Figure 13 **On-state characteristics**

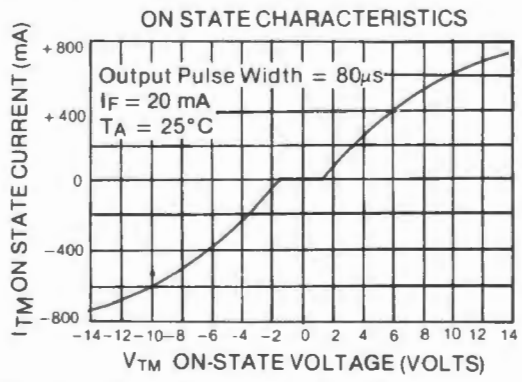
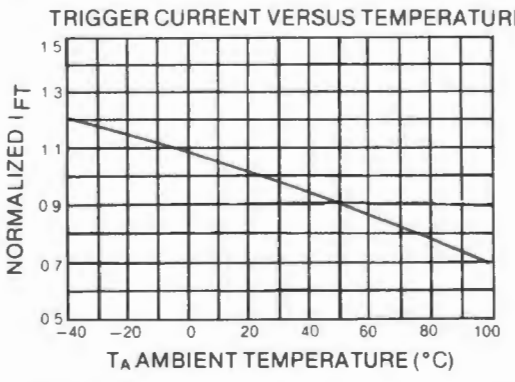


Figure 14 **Trigger current vs temperature**



Applications

Figure 15 **Resistive load with TTL input**

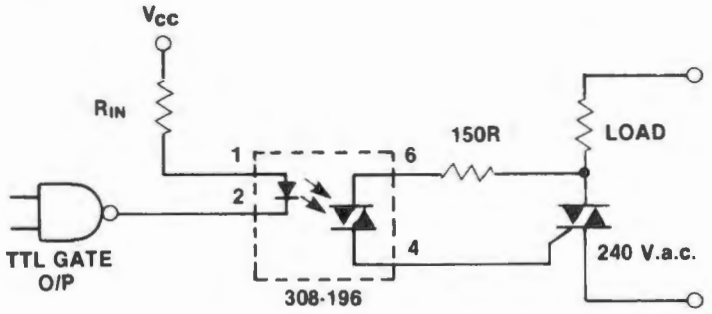
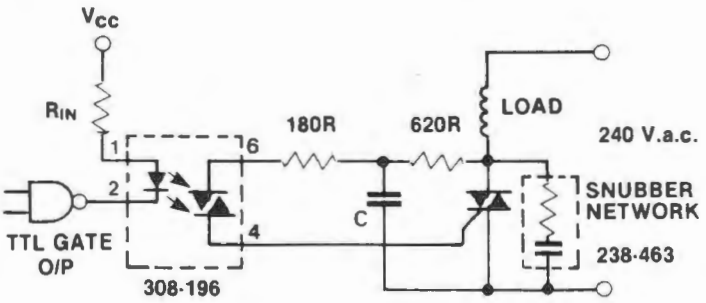
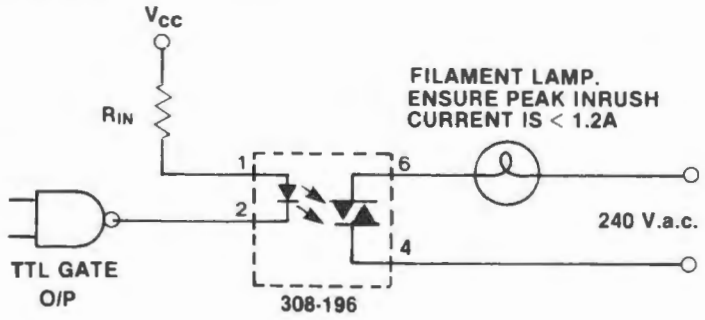


Figure 16 **Inductive load with TTL input**



C	LOAD POWER FACTOR
220n	0.75
330n	0.5

Figure 17 **Low power filament lamp driver with TTL input**



RS data

Zero voltage crossing opto-coupled triac

Figure 18 **Trigger current vs temperature**

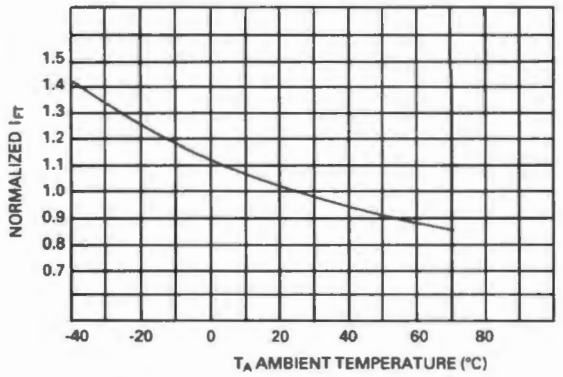
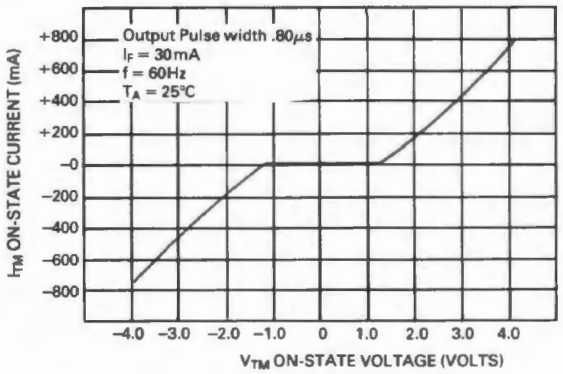


Figure 19 **On-state characteristics**



Applications

Figure 20 **Mains switching**

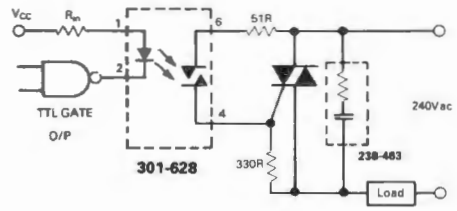
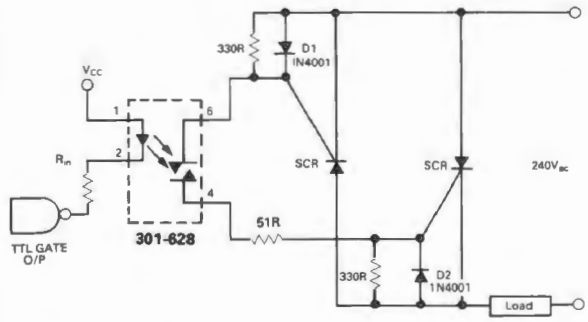


Figure 21 **Inverse – parallel SCR driver circuit**



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L.C.D. Decoder-driver i.c. RS 7211 and RS 7211B

The RS 7211 and 7211B C-MOS decoder-driver i.c.'s are suitable for the direct driving of four digit seven segment liquid crystal displays. Each i.c. provides a complete (no external components necessary) on-board RC oscillator, a divider chain, backplane driver devices and 28 segment outputs. The latter outputs have a zero d.c. component to ensure long display life.

The input to each device is by four data-bit inputs and four digit select inputs allowing for the interface to multiplexed B.C.D. or binary output devices such as the RS 7217, RS 1040E etc. The output codes for the 7211 is the standard seven-segment hexa-decimal 0 to 9, A to F. The 7211B outputs are to the 'B' code which includes all numerals 0 to 9 together with — (dash), E, L, H, P and blank.

The devices may be cascaded to encode more than a single four digit display; up to sixteen 0.5 inch digits may be driven without the use of an external oscillator and is thus suitable for use with any of the RS seven-segment liquid crystal displays.

The use of the RS 7211 and 7211B enables the benefits of L.C.D.'s to be employed, namely good visibility and low power, especially in battery powered equipment.

Equivalent to ICM 7211 IPL and ICM 7211A IPL respectively.

Features

- Four digit non-multiplexed seven segment L.C.D. display outputs with backplane driver, providing a.c. signals for long display life.
- Complete (no external components necessary) on-board RC oscillator to generate backplane frequency.
- Backplane input/output allows simple synchronisation of slave-device segment outputs to a master backplane signal for easy cascading.
- Multiplexed B.C.D. input.
- Binary to hexadecimal decoding (7211).
- Binary to 'B' code (7211B).
- Low voltage C-MOS process-single supply, typically 5V.
- Very low power – ideally suited to battery powered equipment.

Figure 1 **Pin connections**

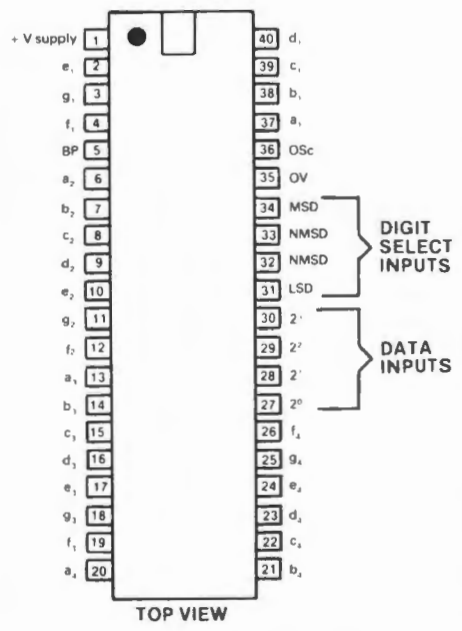
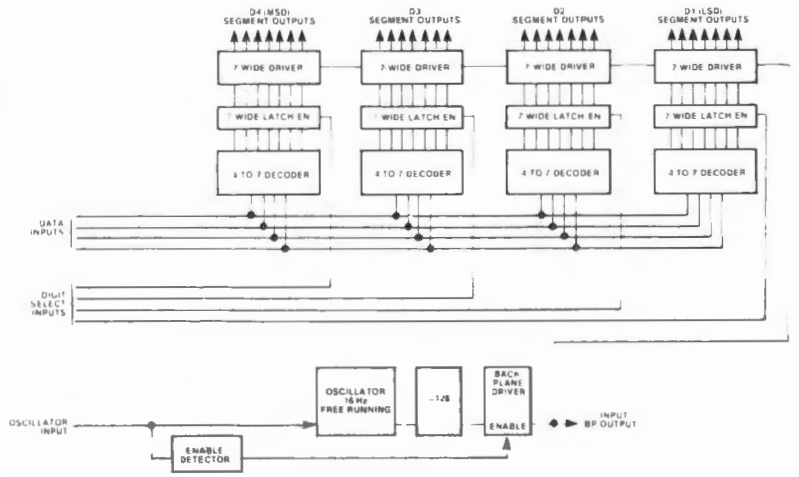


Figure 2 **Block diagram**



Absolute maximum ratings

Power dissipation (Note 1)_____ 0.5W at 70°C
Supply voltage_____6.5V
Input voltage (any terminal) (Note 2) +V +0.3V, −0.3V
Operating temperature range_____ −20°C to 70°C
Storage temperature range_____ −55°C to +125°C

Absolute maximum ratings define stress limitations which, if exceeded, may permanently damage the device. These are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "Operating characteristics".

Note 1: This limit refers to that of the package and will not be obtained during normal operation.

Note 2: Due to the SCR structure inherent in the C-MOS process used to fabricate these devices, connecting any terminal to voltages greater than +V or less than 0V may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply to applied to the device before its supply is established, and that in multiple supply systems, the supply to the RS 7211, 7211B, be turned on first.

Operating characteristics

Table 1. Characteristics All Parameters measured with +V = 5V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating current	I_{op}	Test circuit (Figure 7). Display off		10	50	μA
Operating supply voltage range	+V		3	5	6	V
Oscillator input current	I_{OSL}	Pin 36		±2	±10	μA
Segment rise/fall time	t_{rfs}	C_{load} = 200pF		0.5		μs
Backplane rise/fall time	t_{rfb}	C_{load} = 5000pF		1.5		μs
Oscillator frequency	f_{OSC}	Pin 36 Floating		16		kHz
Backplane frequency	t_{bp}	Pin 36 Floating		125		Hz
Logical "1" Input voltage	V_{IH}	Referred to 0V	3			V
Logical "0" Input voltage	V_{IL}	Referred to 0V			2	V
Input leakage current	I_{DL}	Pins 27–34		±0.1	±1	μA
Input capacitance	C_{IN}	Pins 27–34		5		pF
Backplane input leakage	I_{ILBPI}	Measured at pin 5 with pin 36 at 0V		±.01	±1	μA
Backplane input capacitance	C_{BPI}			200		pF
Digit select active pulse width	t_{sa}	Refer to Timing diagrams	1			μs
Data setup time	t_{ds}		500			ns
Data hold time	t_{dh}		200			ns
Inter-digit select time	t_{IDS}		2			μs

Figure 3 **Operating supply current as a function of supply voltage**

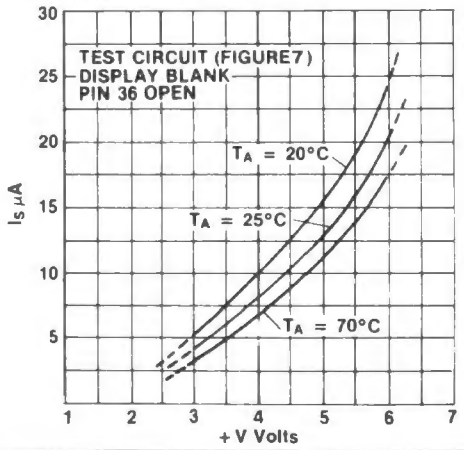


Figure 4 **Backplane frequency as a function of supply voltage**

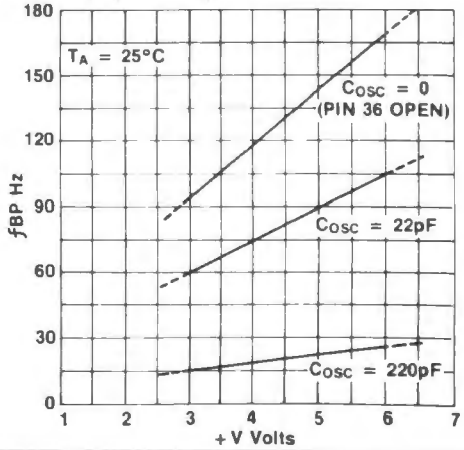


Table 2. Input definitions

In this table, +V and 0V are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 1. For lowest power consumption, input signals should swing over the full supply.

Input	Terminal	Condition	Function	
B0(2^0)	27	+V = Logical One 0V = Logical Zero	Ones (Least significant)	Data Input Bits
B1(2^1)	28	+V = Logical One 0V = Logical Zero	Twos	
B2(2^2)	29	+V = Logical One 0V = Logical Zero	Fours	
B3(2^3)	30	+V = Logical One 0V = Logical Zero	Eights (Most significant)	
OSC	36	Floating or with external capacitor	Oscillator input Disables BP output devices, allowing segments to be synchronised to an external signal input at the BP terminal (Pin 5).	

Multiplexed-binary input configuration

Input	Terminal	Condition	Function
D1	31	+V = Active 0V = Inactive	D1 (Least significant) Digit select
D2	32		D2 Digit select
D3	33		D3 Digit select
D4	34		D4 (Most significant) Digit select

Display driving

The RS I.C.'s provide outputs suitable for driving conventional four digit by seven segment L.C.D. displays, including 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a C-MOS inverter, with the n- and p- channel devices ratioed to provide identical resistances, and thus equal rise and fall times. This eliminates any d.c. component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the oscillator input (pin 36) to the supply. This allows the 28 segment outputs to be synchronised directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200 pF (comparable to one additional segment). The limitation on how many devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimise power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 0.5 inch characters without the rise and fall times exceeding 5μs (i.e. 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all devices be slaved to it.

This external signal should be capable of driving very large capacitive loads with short (1-2 μs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used. Approx. 50 Hz is recommended for RS L.C.D.'s.

The on-board oscillator is designed to free run at approximately 16kHz at microampere supply levels. The oscillator frequency is divided by 128 to provide backplane frequency, which will be approximately 125Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor to the oscillator terminal (pin 36). Refer to Figure 4.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the oscillator input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

Figure 5 **Multiplexed input timing diagram**

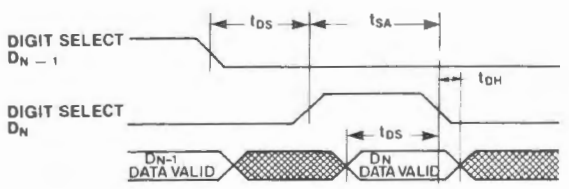
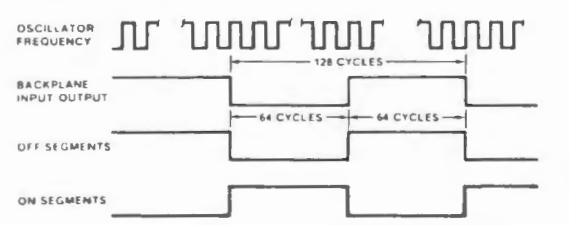


Figure 6 **Display waveforms**



Input configuration and output code

The RS 7211 and 7211B accept a four-bit true binary (i.e. positive level = logical one) input at pins 27 to 30, the least significant bit at pin 27 ascending to the most significant bit at pin 30. This binary input is decoded into seven-segment alpha-numeric hexadecimal or 'B' code outputs as shown in Table 3.

The device is intended to accept data from multiplexed B.C.D. or binary outputs (e.g. from devices such as RS 7217, RS 7216, RS 1040E etc). Four separate digit select lines are provided (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 to 30. More than one digit select may be activated simultaneously (which will write the same character into all selected digits) although the timing requirements shown in Figure 6 and Table 1 for data set-up, hold and interdigit select times must be met to ensure correct output.

Table 3 **Output code & segment assignment**

BINARY				CODE	
2_3	2_2	2_1	2_0	7211	7211B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	R	A
1	0	1	1	b	b
1	1	0	0	C	C
1	1	0	1	d	d
1	1	1	0	E	E
1	1	1	1	F	(Blank)

RS data

Applications

Figure 7 **Test circuit**

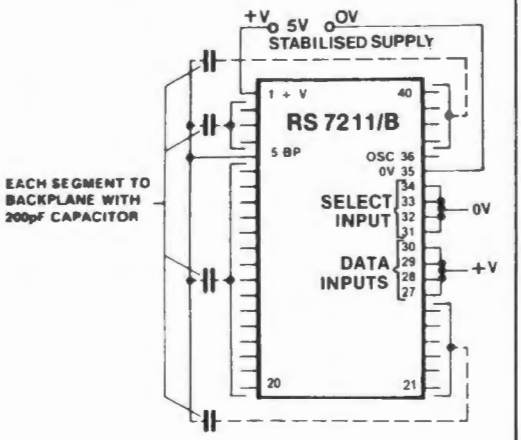


Figure 8 **Cascading two decoders to drive an eight digit display**

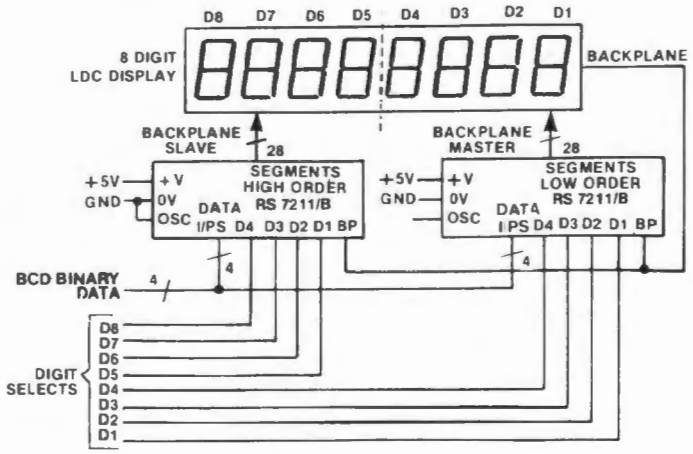


Figure 9 **Decimal point drive using exclusive "OR" gate**

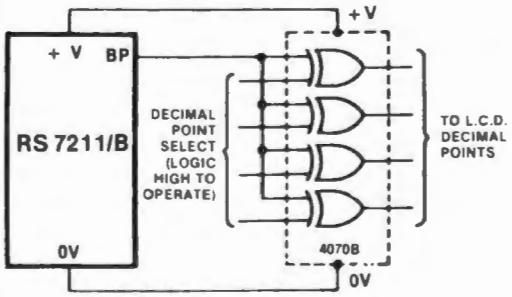
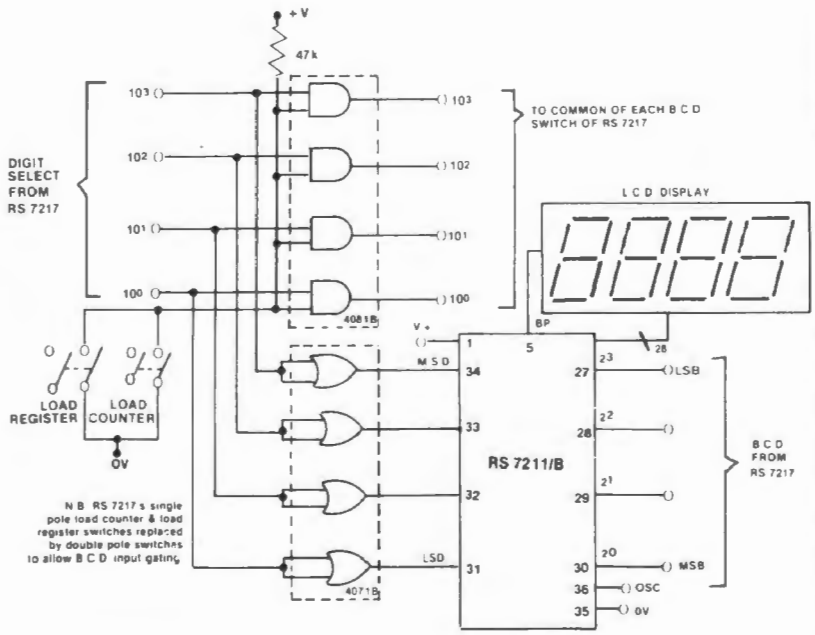


Figure 10 **4 Digit L.C.D. counter using RS 7217 driving RS 7211/B**



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RS data

4½ digit L.C.D. counter/ decoder/driver i.c. RS7224

Stock number 308-562

The RS7224 is a high performance C-MOS 4½ digit L.C.D. counter, including decoders, output latches, display drivers, count inhibit, leading zero blanking and reset circuitry.

The I.C. has a maximum count of 19999 and provides 29 segment outputs and backplane driver output, generating the zero d.c. component signals (for maximum display life) necessary to drive a conventional 4½ digit liquid crystal display. The device also includes a complete RC oscillator and divider chain to generate the backplane frequency and a backplane driver disable control which allows the segments to be slaved to a master backplane signal.

The device is guaranteed to count from d.c. to 15 MHz with a 5 V ±10% supply over the operating temperature range. At normal temperatures the RS7224 can be expected to count at up to 25 MHz. There is a Schmitt trigger on the count input to allow operation in noisy environments and correct counting with slowly changing input waveforms. A true count inhibit is incorporated so that the state of the count input has no effect on the input gating.

The RS7224 also provides several features intended to allow the simple cascading of four-digit blocks. The carry output enables the counter to be cascaded, while the leading zero blanking input and output allows correct leading zero blanking between four-decade blocks. The backplane driver of the L.C.D. devices may be disabled, allowing the segments to be slaved to another backplane signal, which is necessary when using an eight-digit single backplane display. The RS7224 may be used with any of the RS seven segment L.C.D.'s and because of the very low power consumption is ideally suited to battery powered equipment.

Features

- High frequency counting – guaranteed 15 MHz, typically 25 MHz at 5 V
- Less than 100 μW quiescent power
- Direct 4½ digit 7 segment L.C.D. display drive
- Store and Reset inputs permit operation as frequency or period counter
- True count inhibit disables first counter stage
- Carry output for cascading four-digit blocks
- Schmitt-trigger on the count input allows operation in noisy environments or with slowly changing inputs
- Leading zero blanking input and output for correct leading zero blanking with cascaded devices
- Complete onboard oscillator and divider chain to generate backplane frequency, or backplane driver may be disabled allowing segments to be slaved to a master backplane signal
- All inputs fully protected against static discharge – no special handling precautions necessary

Figure 1: **Pin connections**

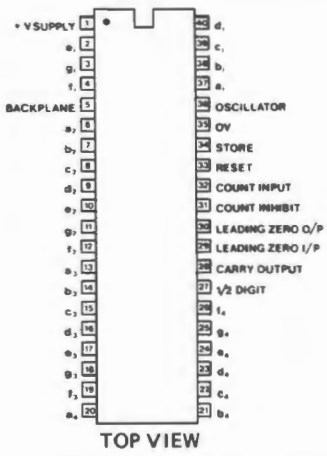
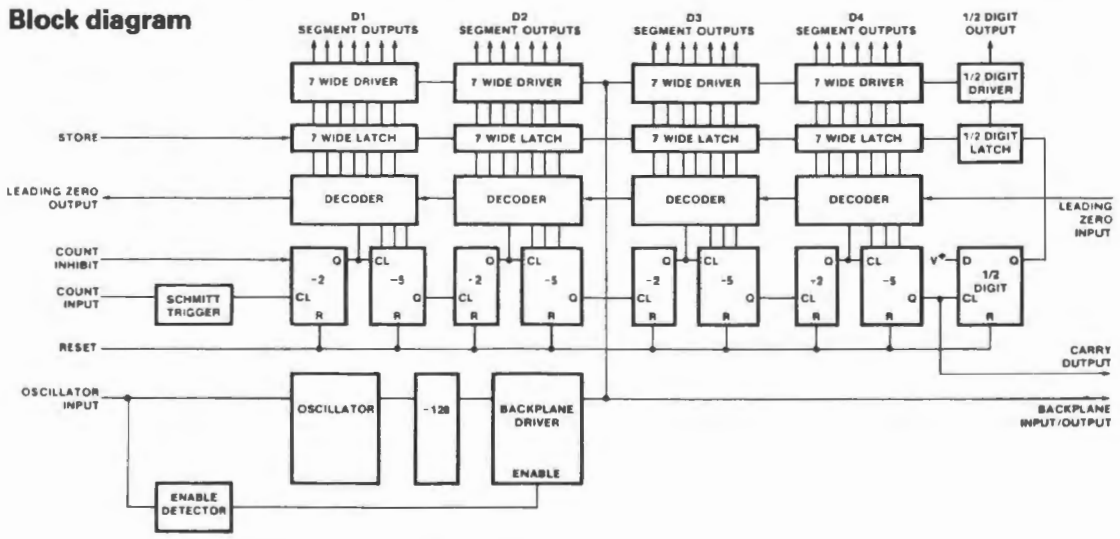


Figure 2: **Block diagram**



Absolute maximum ratings

Power dissipation (Note 1) ..... 0.5W@70°C
Supply voltage (+V) 6.5V
Input voltage (any terminal) (Note 2) ..... +V +0.3V, −0.3V
Operating temperature range ..... −20°C to +70°C
Storage temperature range ..... −55°C to +125°C

Absolute maximum ratings define stress limitations which, if exceeded, may permanently damage the device. These are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under 'Operating characteristics'.

Note 1: This limit refers to that of the package and will not be obtained during normal operation.

Note 2: Due to the SCR structure inherent in the C-MOS process used to fabricate these devices, connecting any terminal to voltages greater than +V or less than 0V may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the RS7224 be turned on first.

Operating characteristics

Table 1: **Characteristics**

All Parameters measured with +V = 5V unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating current	I_{op}	Test circuit (Fig. 8), Display blank		10	50	μA
Operating supply voltage range	+V		3	5	6	V
Oscillator input current	I_{OSC}	Pin 36		±2	±10	μA
Segment rise/fall time	t_{rfs}	C_{load} = 200pF		0.5		μs
Backplane rise/fall time	t_{rfb}	C_{load} = 5000pF		1.5		μs
Oscillator frequency	f_{OSC}	Pin 36 Floating		16		kHz
Backplane frequency	f_{bp}	Pin 36 Floating		125		Hz
Input Pullup currents	I_{PU}	Pins 29, 31, 33, 34 V_{OUT} = +V −3V		10		μA
Input High voltage	V_{IH}	Pins 29, 31, 33, 34	3			V
Input Low voltage	V_{IL}	Pins 29, 31, 33, 34			2	V
Count Input Threshold	V_{CT}			2		V
Count Input Hysteresis	V_{CH}			0.5		V
Output High Current	I_{OH}	Carry Pin 28 Leading Zero Out Pin 30 V_{OUT} = +V −3V	350	500		μA
Output Low Current	I_{DL}	Carry Pin 28 Leading Zero Out Pin 30 V_{OUT} = +3V	350	500		μA
Count frequency	f_{count}	4.5V > (+V) > 6V	0	25	15	MHz
Store, Reset Minimum Pulse Width	t_S, t_R		3			μs

Figure 4: **Backplane frequency as a function of supply voltage**

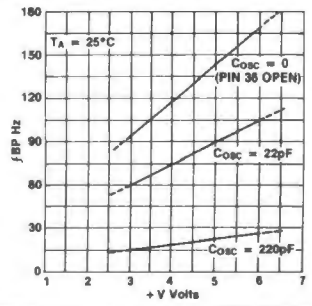


Figure 3: **Operating supply current as a function of supply voltage**

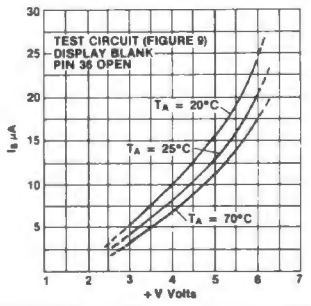


Table 2: **Control input definitions**

In this table +V and 0V are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 1. For lowest power consumption, input signals should swing over the full supply.

Input	Terminal	Voltage	Function
Leading Zero Input	29	+V or Floating 0V	Leading Zero Blanking Enabled Leading Zeroes Displayed
Count Inhibit	31	+V or Floating 0V	Counter Enabled Counter Disabled
Reset	33	+V or Floating 0V	Inactive Counter Reset to 0000
Store	34	+V or Floating 0V	Output Latches not Updated Output Latches Updated

Figure 5: **Maximum count frequency (typical) as a function of supply voltage**

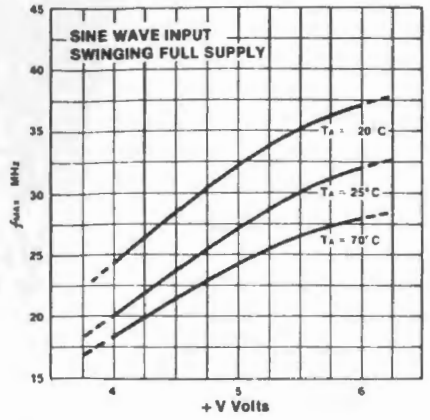


Figure 6: **Supply current as a function of count frequency**

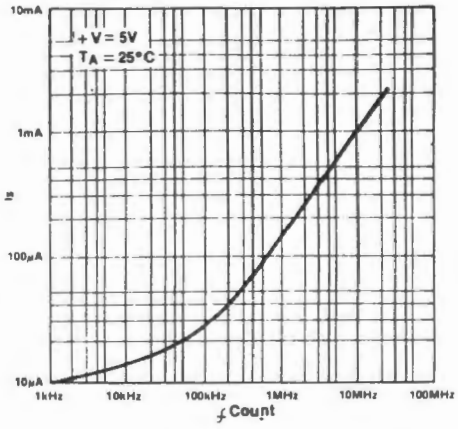
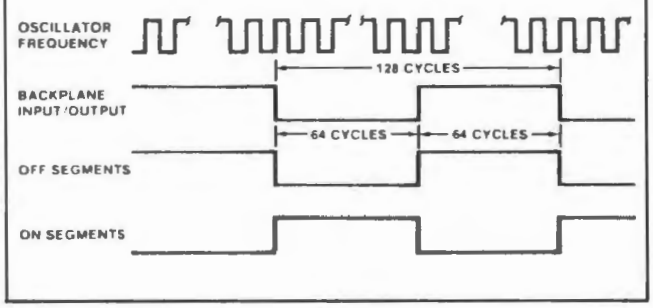


Figure 7: **Display Waveforms**



Description of operation

Display section

The RS7224 provides outputs suitable for driving conventional four-digit by seven-segment L.C.D. displays, including 29 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a C-MOS inverter, with the n- and p- channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any d.c. component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the oscillator input (pin 36) to 0V of the supply. This allows the 29 segment outputs to be synchronised directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200 pF (comparable to one additional segment). The limitation on how many devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimise power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 0.5 inch characters without the rise and fall times exceeding 5μs (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the RS7224 devices be slaved to it.

This external signal should be capable of driving very large capacitive loads with short (1–2μs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 16Hz at microampere supply levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor to the oscillator terminal (pin 36), see Fig. 4. The recommended frequency for RS L.C.D.'s is approximately 50Hz.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the oscillator input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

Counter section

The RS7224 implements a four-digit ripple carry resetable counter, including a Schmitt trigger on the count input and carry output. Also included is an extra D-type flip-flop, clocked by the carry signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will increment on the negative-going edge of the signal at the count input, and the carry output will provide a negative-going edge following the count which indexes the counter from 9999 to 10000. N.B. The carry output goes high at the transition from 5999 to 6000 and remains high until the transition from 9999 to 10000.

Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the Reset terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent carry outputs will not be affected.

A negative level at the Count Inhibit input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true count inhibit which is not sensitive to the state of the count input,

preventing false counts which can result from using a normal logic gate forcing the state of the clock to prevent counting.

Each decade of counter drives directly into a four-to-seven decoder which derives the seven segment output code. Each decoder output corresponds to one segment terminal of the device. The output data is latched at the driver, when the Store pin is at a negative level, these latches are updated, and when the Store pin is left open or at a positive level, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the leading zero input is floating or at a positive level, this circuity is enabled and the device will blank leading zeroes. When the leading zero input is at a negative level, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The leading zero output is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked, which can only occur when the leading zero input is at a positive level and the half-digit is not set.

For example in an eight-decade counter using two RS7224 devices, the leading zero output of the high order digit device would be connected to the leading zero input of the low order digit device. This will assure correct leading zero blanking for all eight digits (see Fig. 10). The Store, Reset, Count Inhibit, and Leading Zero inputs are provided with pull-up devices, so that they may be left open when a positive level is desired. The Carry and Leading Zero outputs are suitable for interfacing to C-MOS logic in general, and are specifically designed to allow cascading of RS7224 devices in four-digit blocks.

Figure 8: **Test circuit**

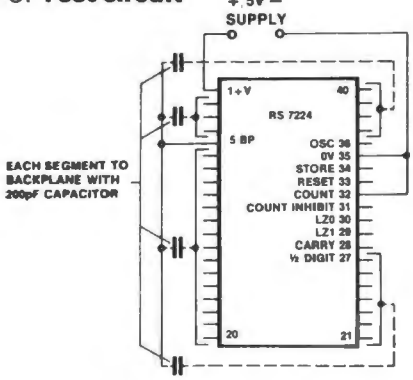


Figure 9: **4½ digit unit counter**

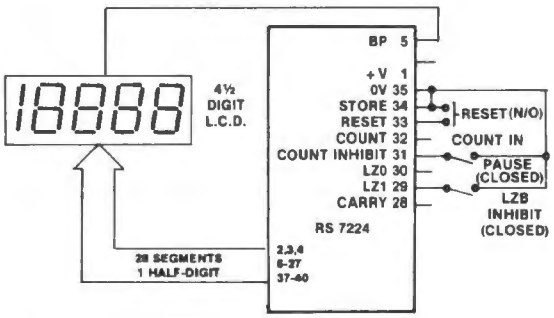


Figure 10: **8 digit unit counter**

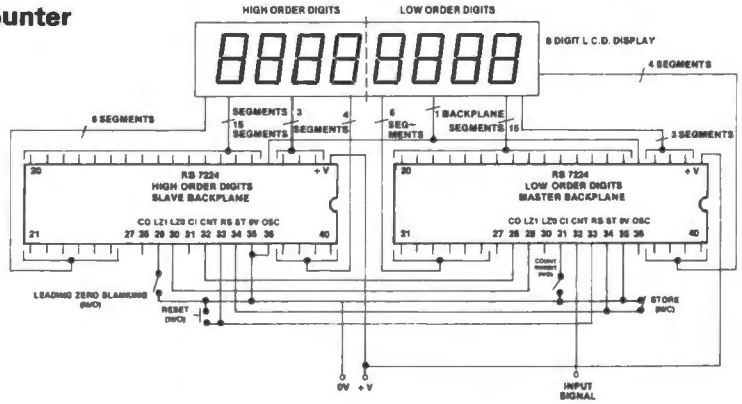
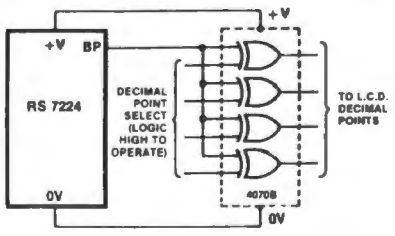


Figure 11: **Decimal point drive using exclusive 'OR' gate**



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RS data

Semiconductor temperature sensor

Stock number 308-809

The RS590 semiconductor temperature sensor is functionally a two terminal I.C. which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V d.c. the device acts as a high impedance constant current regulator passing μA per degree Kelvin. Linearisation circuitry, precision voltage amplifiers, resistance measuring circuitry or cold junction compensation are not required for basic temperature measurement.
The RS590 is ideal in remote sensing applications. The device is virtually insensitive to voltage drops over long lines due to its high impedance current output provided the connection cable used is a twisted pair and well insulated.

Specification

Typical at +25°C (298.2°K) and V_S = 5V unless otherwise stated.

Absolute maximum ratings

Forward voltage (+ to —)	+44V
Reverse voltage (+ to —)	—20V
Breakdown voltage (Case to + or —)	±200V
Rated performance temperature range	—55°C to + 150°C
Storage temperature range	—65°C to + 175°C
Lead temperature (soldering, 10 sec)	+300°C

Power supply

Operating voltage range	+ 4V to + 30V

PIN CONNECTIONS

TO 52 Package

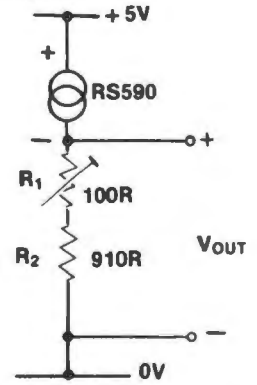
PIN VIEW

Output

Nominal current output	298.2μA
Nominal temperature coefficient	1μA/°C
Calibration error	±2.5°C max
Absolute error[2] (over rated performance temperature range)	
Without external calibration adjustment	±5.5°C max
With + 25°C calibration error set to zero	±2.0°C max
Nonlinearity	±0.8°C max
Repeatability	±0.1°C max
Long term drift[1]	±0.1°C max
Current noise	40pA/$\sqrt{Hz}$
Power supply rejection	
$+4V \leq V_S \leq +5V$	0.5μA/V
$+5V \leq V_S \leq +15V$	0.2μA/V
$+15V \leq V_S \leq +30V$	0.1μA/V
Case isolation to either lead	$10^{10}\Omega$
Effective shunt capacitance	100pF
Electrical Turn-on time[2]	20μs
Reverse bias leakage current[3] (Reverse voltage = 10V)	10pA

1 Conditions: constant + 5V, constant + 125°C
2 Does not include self heating effects
3 Leakage current doubles every 10°C

Figure 1. Calibration Error Trim at Single Point Temperature



To trim the above circuit, the temperature of the RS590 is measured by a reference temperature sensor and R_1 is trimmed so that V_{OUT}=1mV/ °K at that temperature.

Operation

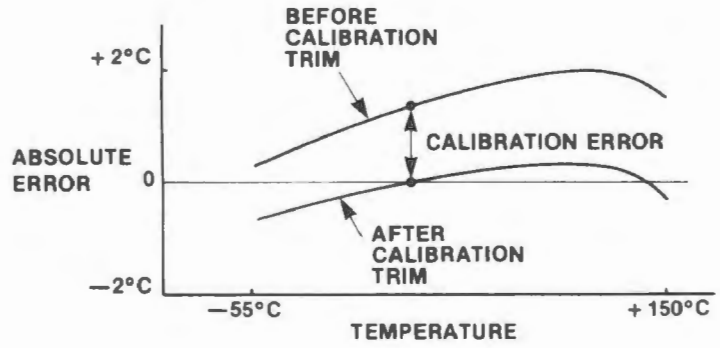
As previously stated the output of the RS590 is basically a proportional to absolute temperature (PTAT) current regulator i.e. the output is equal to a scale factor multiplied by the temperature of the sensor in degrees Kelvin.

Calibration error

The difference between the indicated temperature and actual temperature is called the calibration error. Since this is a scale factor error, it is relatively simple to trim out. Fig. 1 shows the most elementary way of accomplishing this.

Each RS590 is tested for error over the temperature range with callibration error trimmed out.
This error consists of a slope error and some curvature, mostly at the temperature extremes. Fig. 2 shows a typical temperature curve before and after calibration error trimming.

Figure 2: **Effect of calibration error trim on accuracy at single point temperature**



Nonlinearity

Nonlinearity as it applies to the RS590 is the maximum deviation of current over the entire temperature range from a best fit straight line. Fig. 3 shows the nonlinearity of the typical RS590 from Fig. 2.

Figure 3: **Nonlinearity**

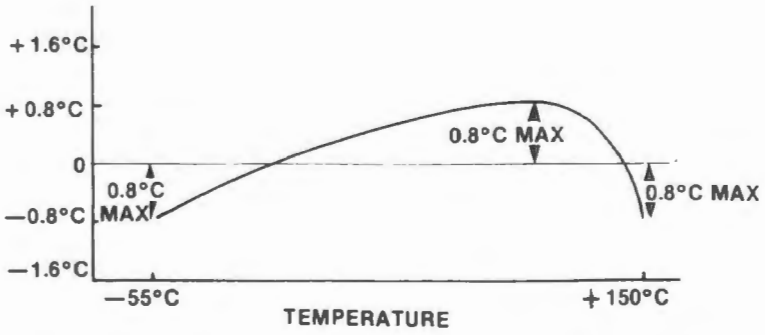


Fig 4A. shows a circuit in which nonlinearity is the major contribution to error over temperature. The circuit is trimmed by adjusting R_1 for a 0V output with RS590 at 0°C. R_2 is then adjusted for 10V out with the sensor at 100°C. Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output (150°C) the V+ supply to the op-amp must be greater than 17V. Also note that V− should be at least −4V: if V− is ground there is no voltage applied across the device.
Note: Resistor values are typical and may need alteration depending upon magnitude of V−.

Figure 4A: **Two point temperature trim**

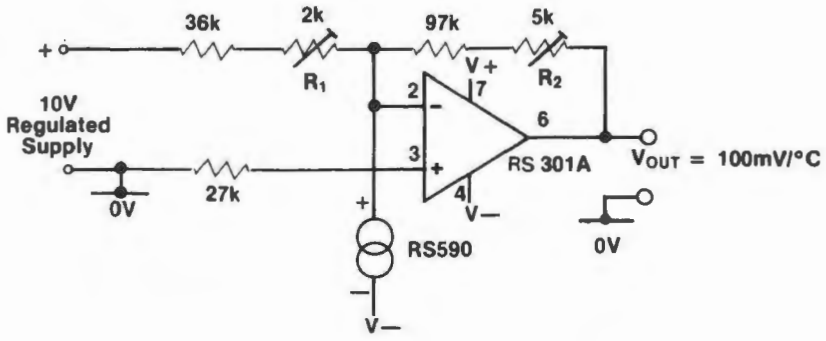
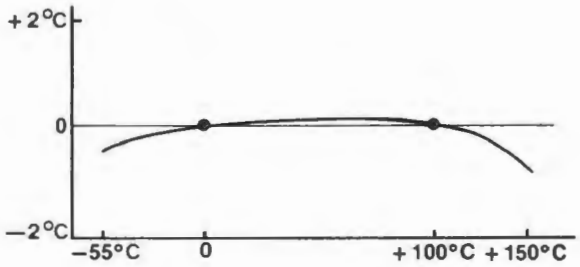


Figure 4B: **Typical two-trim accuracy**



Series/Parallel connection

Several RS590 devices may be connected in series as shown in Fig. 5. This configuration allows the minimum of all the sensed temperatures to be indicated. Connecting the sensors in parallel (Fig. 6) indicates the average of the sensed temperatures.

Figure 5: **Series connection**

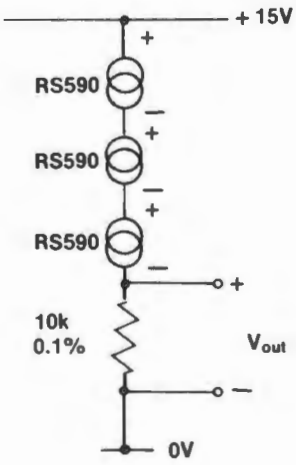
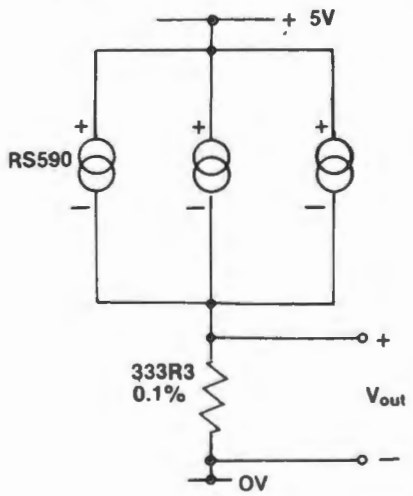


Figure 6: **Parallel connection**



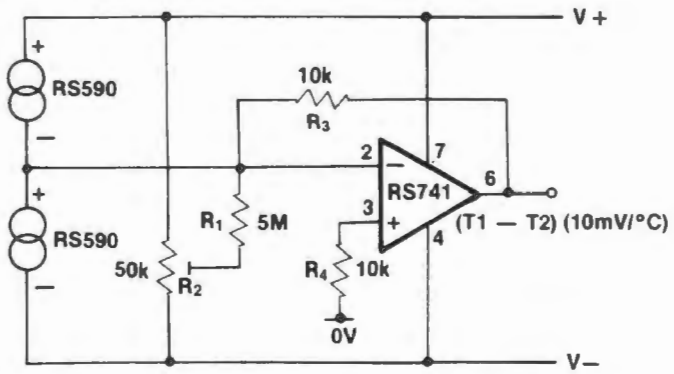
RS data

Differential temperature measurement

Fig. 7 illustrates one method by which differential temperature measurements can be made.

R_1 and R_2 may be used to trim the output of the op-amp to indicate a desired temperature difference.

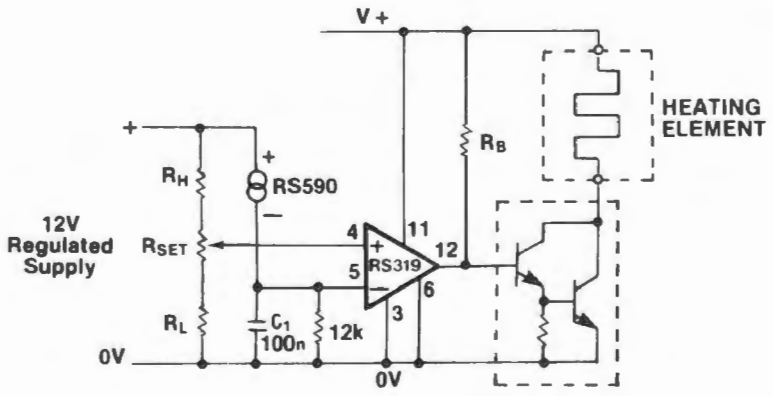
Figure 7: **Differential temperature measurement**



Temperature control

The RS590 may also be used in temperature control circuits (see Fig. 8). R_H and R_L are selected to set the high and low limits for R_{SET}. The RS590 is powered from a 12V stabilised source which isolates it from supply variations while maintaining a reasonable voltage across it. C_1 may be needed to filter extraneous noise. The value of R_B is determined by the ß of the transistor and the current requirements of the load.

Figure 8: **Temperature control**



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RS data

R.M.S. to D.C. converter I.C.'s

Stock numbers 308-786 & 302-665

Two r.m.s. to d.c. converter I.C.'s capable of accurately evaluating the r.m.s. value of a wide range of signal waveforms containing a.c. and/or d.c. components.

The RS AD636JH features a 200mV full scale range making it compatible with many popular display-oriented A to D converters or RS D.P.M.s.

The RS AD536A features a wider full scale range of up to 10V.

The provision of a dB output extends the I.C.'s versatility to audio spectrum measurements and frequencies above. Input signals in excess of the supply voltage can be tolerated without damage. Loss of supply with the input connected will not cause circuit failure.

Principles of Operation

These converter I.C.'s embody an implicit solution of the r.m.s. equation that overcomes the dynamic range as well as other limitations inherent in a straightforward computation of r.m.s. The actual computation performed by the I.C. follows the equation:

$$V_{r.m.s.} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{r.m.s.}}\right]$$

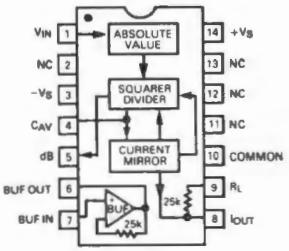
Figure 1 is a simplified schematic of the RS AD536A and the RS AD636JH it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be a.c. or d.c., is converted to a unipopular current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2/I_3$$

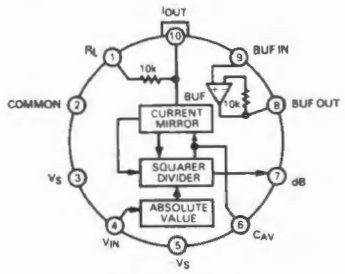
Features

- True r.m.s. to d.c. conversion
- Laser trimmed to high accuracy
- Input protected
- Wide response capability
- Computes r.m.s. of a.c. and d.c. signals
- Low power consumption
- Single or dual supply operation.
- Monolithic integrated circuit.

TOP VIEWS



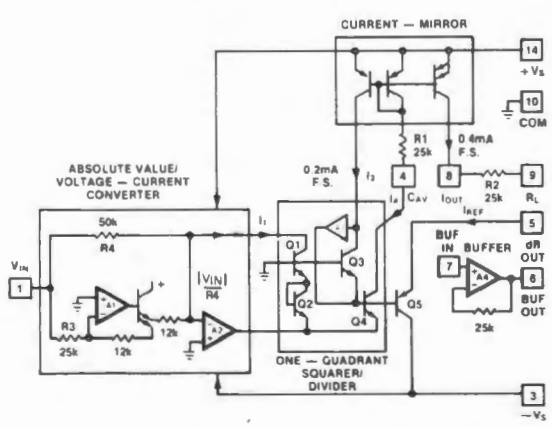
RS AD536A



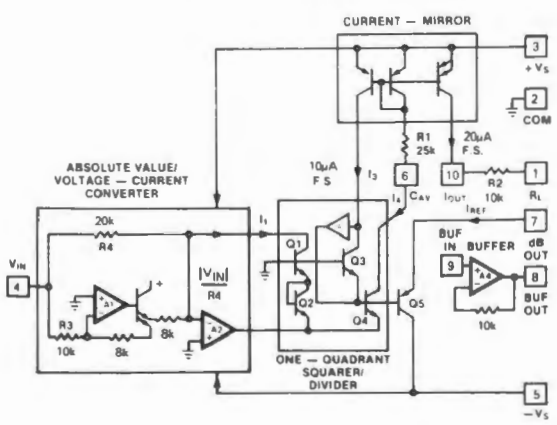
RS AD636JH

Figure 1 **Schematic Diagrams**

RS AD536A (308-786)



RS AD636JH (302-665)



Electrical Characteristics T_{amb} = 25°C unless specified

Parameter	RS AD536A (V_S = ±15V unless specified) Conditions	RS AD536A Value	RS AD636JH (+ V_S = 3V, − V_S = 5V unless specified) Conditions	RS AD636JH Value	Units
Conversion accuracy					
Total error. Internal trim	Fig 2[1]	±5 (±0.5% of reading) max.	Fig. 2[5]	±0.5 (±1% of reading)	mV
Temp. coefficient	0 to 70°C	±0.1 (±0.01% of reading) max.	0 to 70°C	±0.1 (±0.01% of reading)	mV/°C
Supply voltage error		±0.1 (±0.01% of reading)		±0.1 (±0.01% of reading)	V/V
d.c. reversal error		±0.05% of reading		±0.5% of reading	%
External trim error	Fig. 3[1]	±3 (±0.3% of reading)	Fig 3[5]	±0.3 (±0.3% of reading)	mV
Error vs crest factor [2]	CF = 1to 2	Specified Accuracy	CF = 1 to 2	Specified Accuracy	
	CF = 3	−0.1% of reading	CF = 3	−0.2%	
	CF = 7	−1% of reading	CF = 6	−0.5%	
Frequency response [3]			Note 4		
Bandwidth for 1%	10mV < V_{IN} ⩽ 100mV	6	V_{IN} = 10mV	12	kHz
additional error (0.1dB)	100mV < V_{IN} ⩽ IV	40	V_{IN} = 100mV	80	kHz
	IV < V_{IN} ⩽ 7V	100	V_{IN} = 200mV	130	kHz
±3dB bandwidth	10mV < V_{IN} ⩽ 100mV	50		80	kHz
	100mV < V_{IN} ⩽ IV	300		800	kHz
	IV < V_{IN} ⩽ 7V	2		1.3	MHz
Ave time const CAV	Fig. 6	25	Fig. 6	25	ms/µF
Input characteristics					
Signal range		±20		±2.8	V peak
	V_S = ±5V	±5	Vs = ±2.5V	±2	V peak
			Vs = ±5V	±5	V peak
Safe input, all supplies		±25 max.		±12 max.	V
Input resistance		16.7 ±25%		6.7 ±25%	kΩ
Input offset voltage		±2 max.		0.5 max.	mV
Output characteristics			Note 4		
Offset voltage		±2 max.		0.5 max.	mV
vs temperature		±100		±10	µV/°C
vs supply voltage		±0.1		±0.1	mV/V
Voltage swing		0 to +10 min.		0 to 0.3 min. (1 typ.)	V
	V_S = ±5V	0 to + 2 min.	V_S = ±5V	0 to 0.3 min. (1.4 typ.)	V
Output current		+ 5000, − 130 min.			µA
Short circuit current		+ 20			mA
Output resistance		0.5 max.			Ω
dB output					
Error	7mV ⩽ V_{IN} ⩽ 7V rms	±0.5	7mV ⩽ V_{IN} ⩽ 300mV rms	±0.5	dB
Scale factor		−3		−3	mV/dB
S.F. temp. coeff.		−0.03		−0.03	dB/°C
I_{REF}	0dB = 1V rms	5 to 80 (20 typ.)	0dB = 0.1V rms	2 to 8 (4 typ.)	µA
I_{REF} range		1 to 100		1 to 50	µA
I_{OUT} terminal					
Scale factor	rms input	40 ±25%	rms input	100 ±20%	µA/V
Output resistance		10^8		10^8	Ω
Voltage compliance		−Vs to (+ Vs −2.5V)		−Vs to (+ Vs −2V)	V
Buffers amplifier					
I/O voltage range		−Vs to (+ Vs −2.5V) min.		−Vs to (+Vs −2V) min.	V
Input offset voltage	R_S = 25kΩ	±4 max.	Rs = 10kΩ	2 max.	mV
Input current		100 typ. (300 max.)		100 typ. (300 max.)	nA
Input resistance		10^8		10^8	Ω
Output current		+ 5000, −130 min.		+ 5000, −130 min.	µA
Short circuit current		20		20	mA
Small signal bandwidth		1		1	MHz
Slew rate	2kΩ pull down	5	10kΩ pull down	5	V/µs
Power supply					
Voltage range, dual		±3 to ±18		+ 2/ −2.5 to ±12	V
single		+ 5 to + 36		+ 5 to + 24	V
Quiescent current	full V_S, temp range	2 max. (1 typ.)	Buffer I/P at $-V_S$	1 max. (0.8 typ.)	mA
Temperature range					
Operating range		0 to + 70		0 to + 70	°C
Storage range		−55 to + 150		−55 to + 150	°C

The output current I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a curent I_3, which equals Avg. (I_4), back to the squarer/divider to complete the implicit r.m.s. computation. Thus:

$$I_4 = \text{Avg.}\ (I_1^2/I_4) = I_1\ \text{r.m.s.}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used direcly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the RS AD536A thus results:

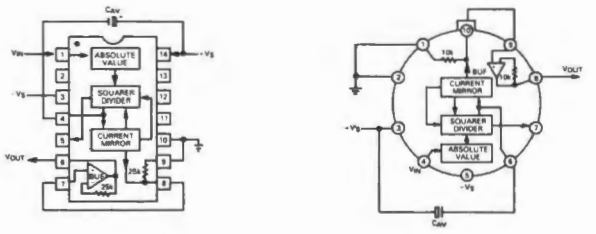
$$V_{OUT} = 2R_2 I_{1\text{r.m.s.}} = V_{IN}\ \text{r.m.s.}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to $-\log_{10} V_{IN}$. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

Standard Connection

Either converter I.C. is simple to connect for the majority of high accuracy r.m.s. measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 2.
In this configuration, the unit will measure the r.m.s. of the a.c. and d.c. level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 6. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be

Figure 2 **Standard connections**



RS AD536A **RS AD636JH**

1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the d.c. input, a capacitor is added in series with the input, as shown in Figure 4, the capacitor must be nonpolarised. If the converter is driven from power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 100nF disc ceramics as near to the device as possible.

The input and output signal ranges are a function of the supply voltages as detailed in the specifications. These devices can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the internal resistor R2. The buffer amplifier can then be used for other purposes. In addition these I.C.s can be used in a current output mode by disconnecting R2 from ground. The output current is available at the I_{OUT} pin with a nominal scale of 40μA per volt r.m.s. input, positive out, for the RS AD536A and 100μA per volt r.m.s. input, positive output for the RS AD636JH.

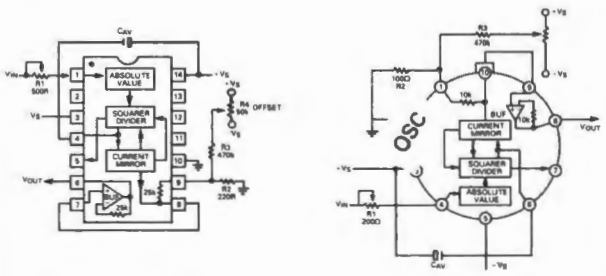
Optional External Trims for High Accuracy

If it is desired to improve the accuracy the external trims shown in Figure 3 can be added. R_4 is used to trim the offset. Note that the offset trim circuit adds resistance in series with the internal resistor R2. This will cause an increase in scale factor, which is trimmed out by using R_1 as shown. The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output at 'V_{OUT}'. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.

2. Connect the desired full scale input level to V_{IN}, either d.c. or a calibrated a.c. signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from the buffer output pin. i.e., 200mV d.c. input should give 200mV d.c. output. A ± 200mV peak-to-peak sinewave should give a 141.4mV d.c. output. The remaining errors, as given in the specifications, are due to device nonlinearity. The major advantage of external trimming is to optimise device performance for a reduced signal range.

Figure 3 **Optional External Gain and Output Offset Trims**

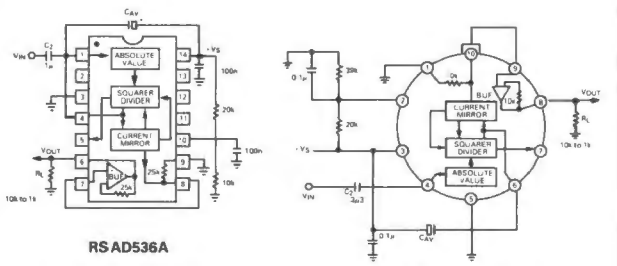


RS AD536A **RS AD636JH**

Single Supply Connection

The applications in Figure 2 and 3 require the use of approximately symmetrical dual supplies. Both i.c.'s can also be used with only a single positive supply down to + 5 volts, as shown in Figure 4. The major limitation of this connection is that only a.c. signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at the common pin; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between + Vs and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 microamps of current flows into the common pin (1μA for the RSAD 636JH). AC input coupling requires only capacitor C_2 as shown; a d.c. return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The load resistor, R_L, is necessary to provide output sink current.

Figure 4 **Single Supply Connection**



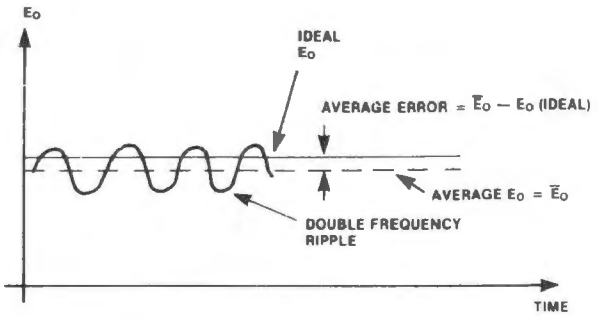
RSAD536A **RSAD636JH**

Circuit Performance Considerations

These devices will compute the r.m.s. of both a.c. and d.c. signals. If the input is a slowly-varying d.c., the output of the device will track the input exactly. At higher frequencies, the average output will approach the r.m.s. value of the input signal. The actual output will differ from the ideal output by an average (or d.c.) error and some amount of ripple, as demonstrated in Figure 5.

The d.c. error is dependent on the input signal frequency and the value of C_{AV}. Figure 6 can be used to determine the minimum value of C_{AV} which will yield 1% or 0.1% d.c. error above a given frequency. For example, if a 60Hz waveform is to be measured with a d.c. error of less than 0.1%, C_{AV} must be greater than 0.65μF. If a 1% error can be tolerated, the minimum value of C_{AV} is 0.22μF.

Figure 5 **Typical Output Waveform for Sinusoidal Input**



The a.c. component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

The primary disadvantages in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 6 shows that the relationship between C_{AV} and settling time is 100 milliseconds for each microfarad of C_{AV}.
The settling time is twice as great for decreasing signal amplitudes as for increasing signals (the values in Figure 6 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 7.

Figure 6 **Lower Frequency for Stated % of Reading Error and Settling Time for Circuit Shown in Figure 2**

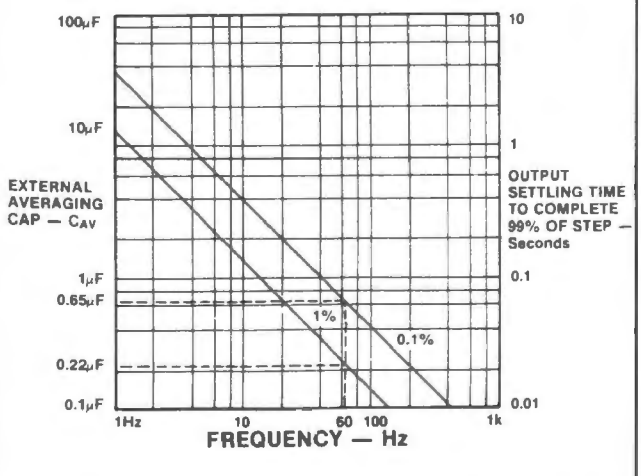


Figure 7 **Settling Time vs. Input Level**

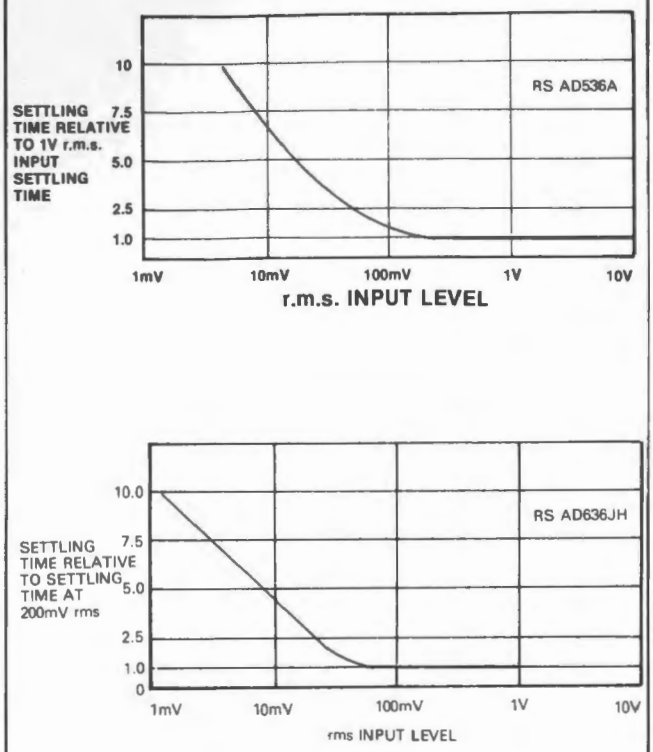
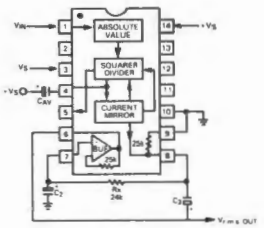
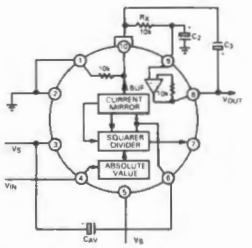


Figure 8 **2 Pole "Post" Filter**



RSAD536A



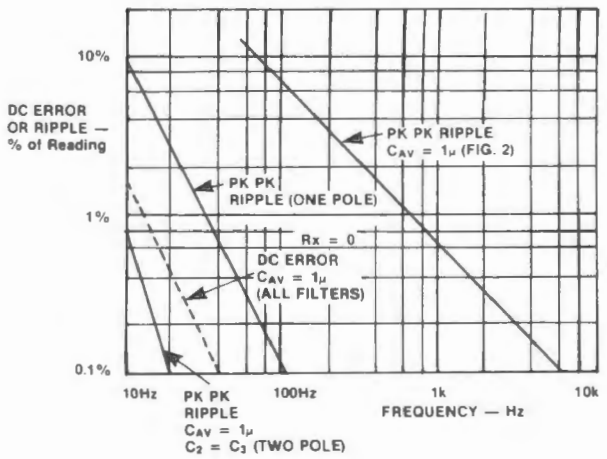
RSAD636JH

Note: For single pole, short Rx, remove C_3

A better method of reducing output ripple is the use of a "post-filter". Figure 8 shows a suggested circuit. If a single-pole filter is used (C_3 removed, Rx shorted), and C_2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 9, and settling time is increased. For example, with C_{AV} = 1μF and C_2 = 2.2μF (4.7μF for the RS AD 636JH) the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the d.c. error is dependent upon this value and is independent of the post filter.

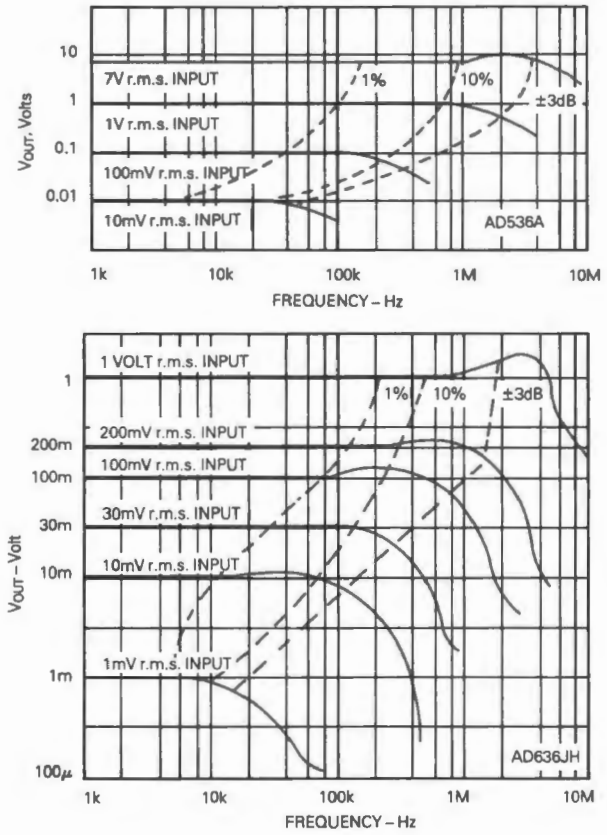
Figure 9 **Performance Features of Various Filter Types**



Frequency Response

These devices utilise a logarithmic circuit in performing the implicit r.m.s. computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below (Figure 10) represents the frequency response of the i.c. The dashed lines indicate the upper frequency limits for 1%, 10% and 3dB of reading additional error.

Figure 10 **High Frequency Response**



AC Measurement Accuracy and Crest Factor

Crest factor is often overlooked in determining the accuracy of an a.c. measurement. Crest factor is defined as the ratio of the peak signal amplitude to the r.m.s. value of the signal (C.F. = $V_{p}/r.m.s.$). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$), where η is duty cycle. Figure 11 is a curve of reading error for the RS AD536A for a 1 volt r.m.s. input signal with crest factors from 1 to 10. A rectangular pulse train (pulse width 100μs) was used for this test since it is the worst-case waveform for r.m.s. measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt r.m.s. input amplitude.

Figure 12 is a similar curve for the RS AD636JH for a 200mV rms input signal, crest factors from 1 to 7 and a pulse width of 200μS.

Figure 11 **Error vs. Crest Factor for the AD536A**

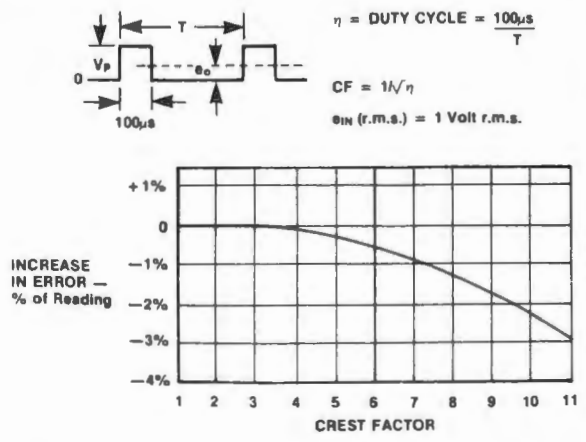
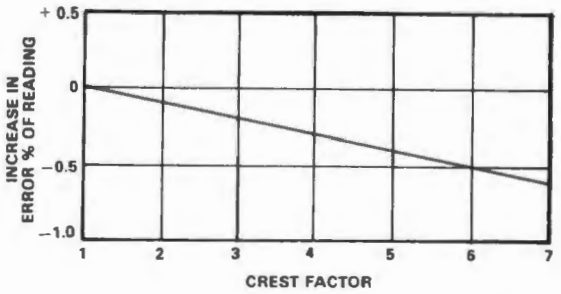


Figure 12 **Error vs. Crest Factor for the AD636JH**



RS data

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Telephone: 0536 201234
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RS data

Frequency counter i.c. RS7216C

Stock number 308-837

The RS7216C Frequency Counter i.c. is a fully integrated 8 digit frequency counter, which combines a high frequency oscillator, a decade timebase counter, an eight decade data counter and latches, a seven segment decoder, digit multiplexers and eight segment and eight drivers which can directly drive large LED displays (e.g. 0.5'' multiplexed displays 587-024).

The counter input has a maximum frequency of 10 MHz. However, the maximum frequency may be extended by use of prescaling techniques e.g. to increase the range to 50 MHz a 74LS90 decade counter (307-610) may be used or to increase the range to at least 100 MHz the RS ÷ 100 Prescaler i.c. (307-474) may be employed. The input is a digital input, and therefore in many applications the input signal will need amplification and level shifting to give the correct digital signal.

The counter normally uses a 10 MHz quartz crystal timebase (but a 1 MHz quartz crystal timebase is possible), in addition the timebase may be driven from an external oscillator. The user can select accumulation times of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to an accuracy of 0.1 Hz in the least significant digit. there is 0.2 sec between measurements in all ranges.

The RS7216C incorporates leading zero blanking and automatic decimal point setting as the range is changed, but this may be overridden using the external decimal point control when required. The reading is displayed in kilohertz in the frequency mode. The display is multiplexed at 500 Hz with a 12.5% duty cycle for each digit with a typical peak segment current of 25 mA. In the display mode, both digit drivers and segment drivers are turned off allowing the display off to be used for other functions if required.

Features

- Functions as a frequency counter, measures from d.c. to 10 MHz
- Four internal gate times: 0.01 sec, 0.1 sec, 1 sec and 10 sec
- Decimal point and leading zero blanking may be externally selected
- Measurement in progress output
- Eight digit multiplexed LED outputs
- Output drivers will directly drive both digits and segments of large LED displays
- Single nominal 5 V supply required
- Stable high frequency oscillator, uses either 1 MHz or 10 MHz crystal
- Internally generated multiplex timing with inter-digit blanking, leading zero blanking and overflow indication.
- Decimal point and leading zero blanking controlled directly by the chip
- Display off mode turns off display and puts chip into low power mode
- Hold and reset inputs for additional flexibility
- All terminals protected against static discharge

Figure 1: **Pin connections**

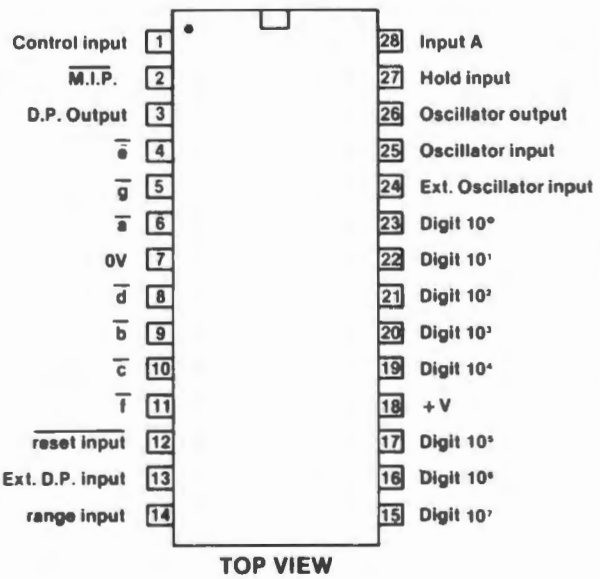
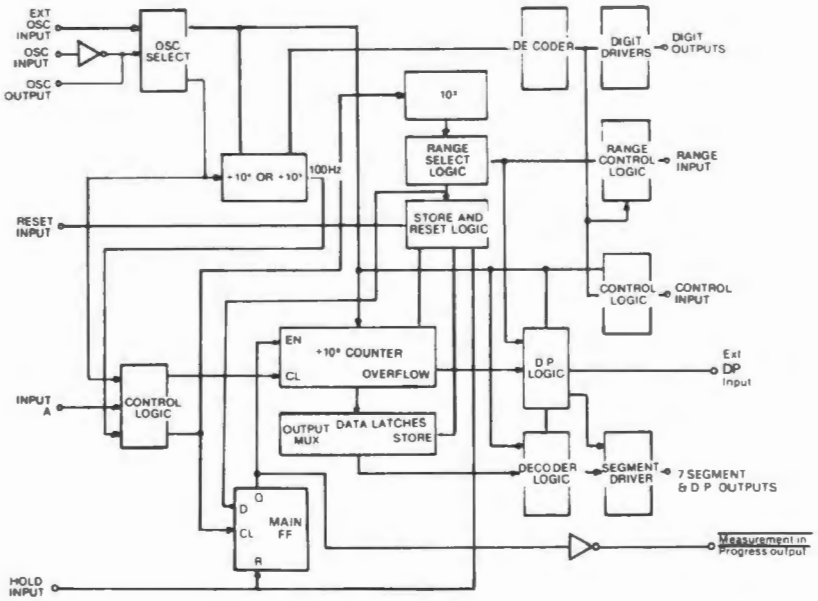


Figure 2: **Block diagram**



Absolute maximum ratings

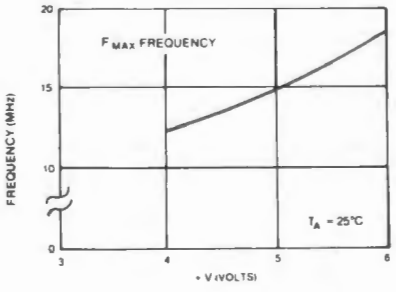
Maximum supply voltage (+V)	6.5V
Maximum digit output current	400mA
Maximum segment output current	60mA
Voltage on any input or output terminal[1]	+V + 0.3V to − 0.3V
Maximum power dissipation at 70°C	1.0W
Maximum operating temperature range	−20°C to + 70°C
Maximum storage temperature range	− 55°C to + 125°C

Notes:

1. The RS7216C may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if inputs or outputs are forced to voltages exceeding +V by more than 0.3V.

Figure 3: **Waveform for guaranteed minimum F**

Figure 4: **Typical operating characteristics**



F MAX, as a Function of +V

Electrical characteristics

Test conditions $+V = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
Operating Supply Current	I_{DD}	Display Off, Unused Inputs to 0V		2	5	mA
Supply Voltage Range	$+V$	$-20°C < T_A < +70°C$, Input A, Frequency at F_{MAX}	4·75		6·0	V
Maximum Frequency Input A, Pin 28	F_{MAX}	$-20°C < T_A < +70°C$ $4.75 < +V < 6·0V$, Figure 3	10			MHz
Maximum Osc. Freq. and Ext. Osc. Frequency		$-20°C < T_A < +70°C$ $4·75 < +V < 6·0V$	10			MHz
Minimum Ext. Osc. Freq.					100	kHz
Oscillator Transconductance	gm	$+V = 4.75V, T_A = +70°C$	2000			μmhos
Multiplex Frequency	f_{mux}	$f_{OSC} = 10MHz$		500		Hz
Time Between Measurements		$f_{OSC} = 10MHz$		200		ms
Input Voltages: Pins 12,27,28 Input Low Voltage Input High Voltage	 V_{IL} V_{IH}	$-20°C < T_A < +70°C$	 3·5		1·0	 V V
Input Resistance to +V Pins 12,24	R	$V_{IN} = +V-1·0V$	100	400		kΩ
Input Leakage Pin 27, Pin 28	I_L				10	μA
Output Current Pin 2	I_{OL}	$V_{OL} = 0.4V$	0.36			mA
	I_{OH}	$V_{OH} = +V-0.8V$	265			μA
Digit Driver: Pins 15, 16, 17, 19, 20, 21, 22, 23 High Output Current Low Output Current	 I_{OH} I_{OL}	 $V_{OUT} = +V-2·0V$ $V_{OUT} = +1\ 0V$	 −150	 −180 +0.3		 mA mA
Segment Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	 I_{OL} I_{OH}	 $V_{OUT} = +1\ 5V$ $V_{OUT} = +V-2·5V$	 25	 30 −100		 mA μA
Multiplex Inputs: Pins 1, 3, 14 Input Low Voltage Input High Voltage Input Resistance to 0V	 V_{IL} V_{IH} R	 $V_{IN} = +1\ 0V$	 +2·0 50	 100	0·8	 V V kΩ

Applications notes

General

Input A

Input A is a digital input with a typical switching threshold of 2.0V at $+V = 5.0V$. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centred about the switching voltage. When the input is being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed inputs

The range, control and external decimal point inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The range and control inputs must be stable during the last half of each digit output, (typically 125 μs). The multiplex inputs are active high for a common anode display.

Noise on the multiplex inputs can cause improper operation. For maximum noise immunity, a 10 kΩ resistor should be placed in series with the multiplex inputs and a 68 pF decoupling capacitor between the multiplex input and 0 V, as shown in figure 9.

Table 1 shows the functions selected by each digit for these inputs.

Control input functions

Display test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Display Off is selected at the same time.

Display Off – To enable the Display Off mode it is necessary to connect $D10^3$ to the control input and have the HOLD input at + V. The chip will remain in the Display Off mode, until HOLD is switched back to 0 V. While in the Display Off mode, the segment and digit driver outputs are open. During Display Off the oscillator continues to run with a typical supply current of 1.5 mA with a 10 MHz crystal and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to 0V.

1 MHz select – The 1 MHz enable mode allows use of a 1 MHz crystal with the same digit multiplex rate and time between measurements as with a 10 MHz crystal.

External oscillator enable – In this mode the external oscillator input is used instead of the on-chip oscillator for the timebase input. The on-chip oscillator will continued to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100 kHz or the chip will reset itself to enable the on-chip oscillator. (The RS 10 MHz crystal oscillator is ideally suited as an external oscillator.)

Range input – The range input selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter. A change in the range input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the range input is changed.

External decimal point enable – When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to the external decimal point is active (except MSD). Leading Zero Blanking will be disabled for all digits following the decimal point.

Hold input – When the hold input is at + V, any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. When hold is changed to 0V, a new meseasurement is initiated.

$\overline{\text{Reset}}$ input – The $\overline{\text{Reset}}$ Input is the same as a Hold Input, except the latches for the main counter are enabled, resulting in an output of all zeros.

Display considerations

The display is multiplexed at a 500 Hz rate with a digit time of 244 μs. An interdigit blanking time of 6 μs is used to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays. Any zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the main counter overflows.

Table 1

	FUNCTION	DIGIT CONNECTION
Range Input Pin 14	1 hertz	$D10^0$
	10 hertz	$D10^1$
	100 hertz	$D10^2$
	1000 hertz	$D10^3$
Control Input Pin 1	Blank Display	$D10^3$ and Hold
	Display Test	$D10^7$
	1 MHz Enable	$D10^1$
	External Oscillator Enable	$D10^0$
	External Decimal Point Enable	$D10^2$
External Decimal Point Input Pin 13.	Decimal point is output for same digit that is connected to this input (except $D10^7$).	

The RS7216C is designed to drive common anode LED displays at peak current of 25mA/segment, using displays with $V_F = 1.8V$ at 25mA. The average DC current will be over 3mA under these conditions.

Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 5, 6 and 7 show the digit and segment currents as a function of output voltage (V_{out} referred to OV).

To obtain additional brightness from the displays, +V may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

Figure 5: **Typical I_{DIG} VS. $+V - V_{OUT}$ (4.5V < +V < 6.0V)**

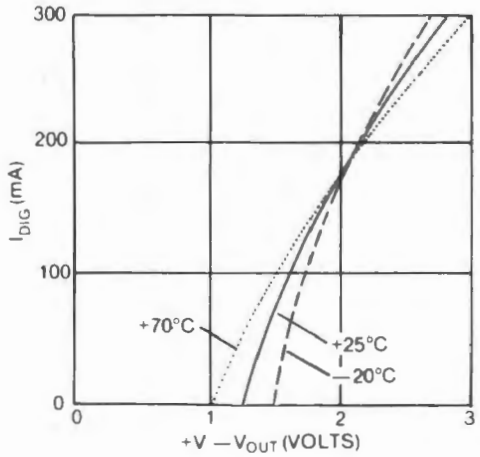


Figure 6: **Typical I_{SEG} VS. V_{OUT} (+V Varied)**

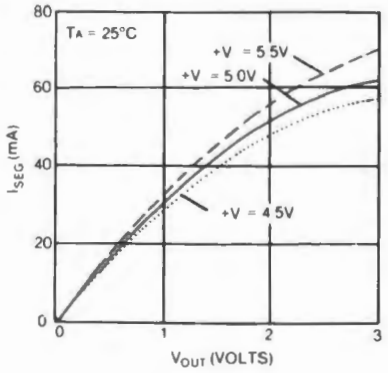
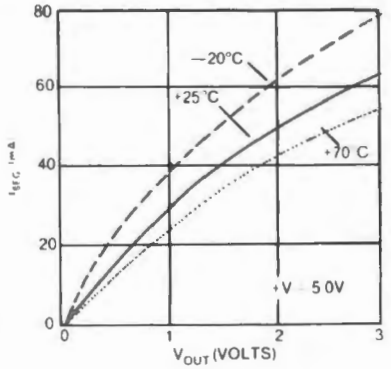
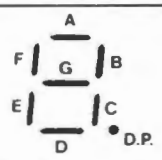


Figure 7: **Typical I_{SEG} VS. V_{OUT} (Temperature varied)**



The segment and digit outputs in the RS7216C are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

Segment identification:



N.B. The correct display to use with this device is a common anode with right hand decimal point e.g. RS multiplexed seven segment display Stock No. 587-024.

Accuracy

In a frequency counter crystal drift and quantization errors cause measurement errors. When measuring frequency a signal derived from the oscillator is used in the reference counter, therefore, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficent of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. With frequency measurement obviously the maximum accuracy is obtained with high frequency inputs.

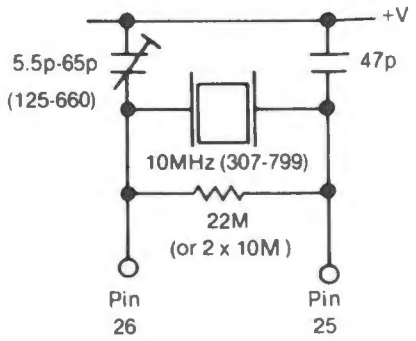
Oscillator considerations

The easiest way of implementing the timebase oscillator is to use a 10 MHz crystal (307-799) and associated circuitry as shown in Figure 8.

If the 1 MHz enable option is to be used, this may be implemented simply by substituting a 1 MHz crystal (307-761) for the 10 MHz crystal in Figure 8 and connecting the 1 MHz enable control circuitry.

An external oscillator, e.g. the RS 10 MHz crystal oscillator may be used by connecting the oscillator output to pin 24 and connecting the external oscillator enable control circuitry. (N.B. oscillator output must meet input voltage criteria as detailed in maximum ratings and electrical characteristics sections.)

Figure 8: **Crystal oscillator circuit**



Circuit applications

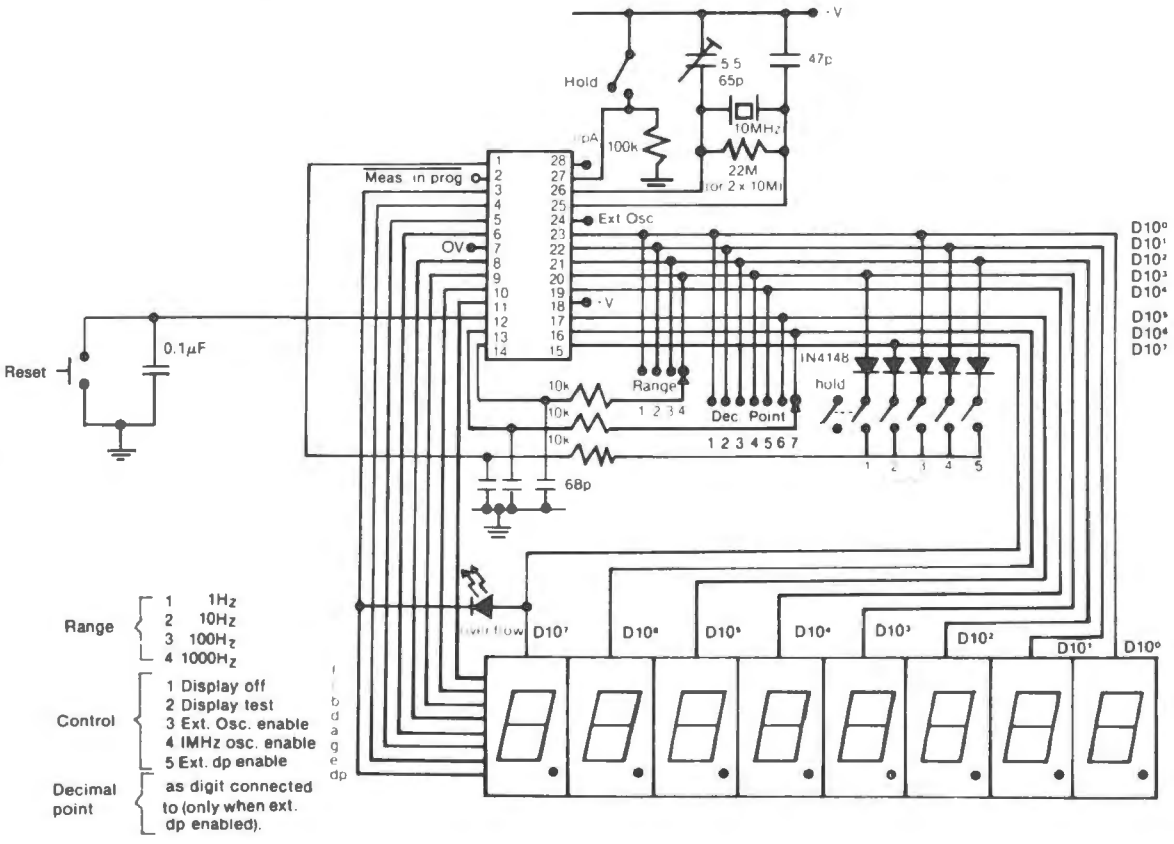
General notes

The range and function input switches should be break before make types. The control, hold and reset switches, being individual switches may be miniature toggle, slide or pushbutton types, as required. (N.B. all switches, however, should have gold contacts.)

The display may be made up using two multiplexed displays (587-024), or eight 0.5in individual displays (588-320).

The recommended supply decoupling is a 220μ electrolytic capacitor and a 100 n disc ceramic (124-178), as close to the device supply pins as possible.

Figure 9: **Full RS7216C test circuit**

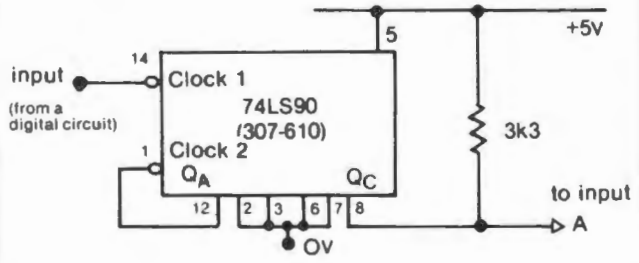


The RS7216C has been designed for use in a wide variety of frequency counter applications. In many cases, prescalers will be required to reduce the input frequencies to under 10 MHz. Because input A is a digital input, additional circuitry will often be required for input buffering, amplification, hysteresis, and level shifting to obtain a good digital signal. The complexity for doing this can vary widely depending on the sensitivity and maximum frequency required.

Prescaler techniques

Figure 10: **Divide by ten prescaler**

Prescaler ÷ 10 up to 50 MHz



Note: The output from the 74LS90 comes from Q_C rather than Q_D to obtain an input duty cycle of 40% for the RS7216C. If the signal at input A has a very low duty cycle it may be necessary to use a monostable (74LS123 or similar) to stretch the pulse width to guarantee a 50 ns minimum pulse width.

For further details of the RS8629, Stock No. 307-474, see data sheet 3059.

The use of the external decimal point control allows the correct positioning of the decimal point (and zero blanking) when prescalers are used – see page 4.

Figure 11: **Divide by 100 high frequency single ended input**

Prescaler ÷ 100 up to 150 MHz

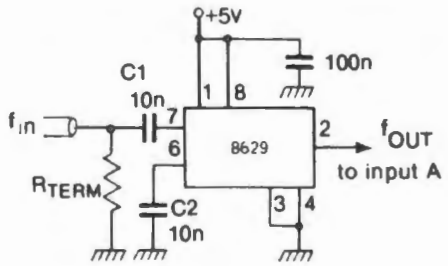
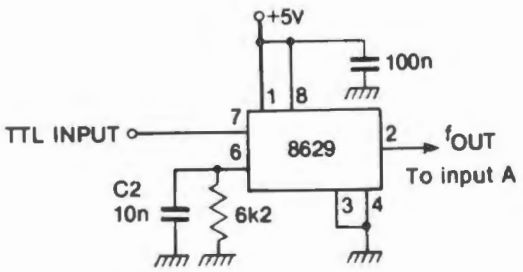


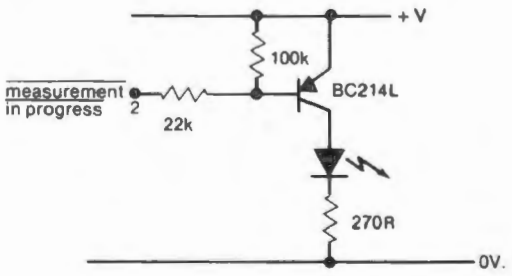
Figure 12: **Divide by 100 TTL input ($DC<f_{in}<f_{max}$)**



Measurement in progress output

The most simple use this output may be put to is to enable a visual indication of measurement in progress to be displayed (see Figure 13). In more sophisticated systems, however, this output may be used to control any function which needs to be synchronised with the start of the measurement cycle (e.g. prescalers etc).

Figure 13: **Measurement in progress display**



RS data

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RS data

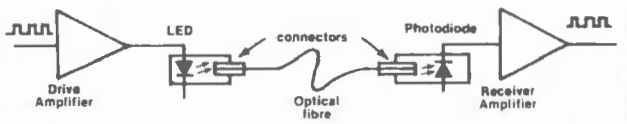
Fibre Optics

This data sheet discusses Fibre Optics in general terms and gives details of some of the basic RS products. For more detailed information the following data sheets should be consulted:

4361	Fibre Optic Transmitter and Receiver Modules
4557	'Sweet Spot' Fibre Optic Devices
4563	Optical Communication Receiver I.C.
5134	'Sweet Spot' Visible Emitter

Fibre Optics can offer solutions to many of the problems associated with traditional electrical hard wired transmission systems.

Figure 1 **Basic fibre optic link**



Fibre Optics vs Copper Wire

In an optical system, see Fig. 1, signals are transmitted in the form of photons (light) which have no electrical charge and, therefore, cannot be affected by the electric fields as experienced in high voltage environments or during a lightning discharge. Similarly, high magnetic fields from motors, machinery, transformers etc., have no affect on optical transmission. There are no crosstalk problems as the small leakage of flux which may occur at the fibre boundary interface is retained by the opaque primary jacket ensuring that optical signals cannot interfere with each other when fibres are in close proximity. This factor also guarantees security of transmission, for the signal is unable to be externally detected throughout the length of the fibre.

Features

- Freedom from electro-magnetic interference.
- Freedom from crosstalk.
- Security of transmission.
- Elimination of sparking and fire hazards.
- Electrical isolation.
- Absence of ground loops.
- Low weight coupled with high strength.
- Increased bandwidth and lower transmission losses than in coaxial cables at high frequencies.

Generally in data communication, fibres carry signals which are of μW levels. Consequently if a fibre is broken or damaged, the escaping flux is harmless, whereas a spark from an electrical cable may prove fatal in explosive atmospheres or in flammable environments.

The inert nature of optical fibres means they can tolerate most kinds of weather and be immersed in many fluids. Their low weight and small size is useful in many applications. Complete electrical isolation is a distinct benefit, giving more freedom in the design of the transmitter and receiver and ensuring the elimination of ground loop problems. However, by far the major advantage is in bandwidth. In either coaxial or parallel-wire cable the bandwidth varies inversely as the square of the length, while in fibre optic cables it varies inversely as the length, only.

Fibre Optics Theory

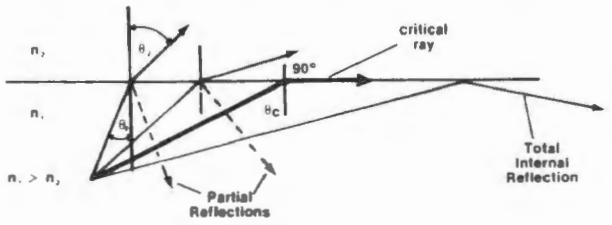
Total Internal Reflection TIR

Optical fibres transmit light by the phenomenon of total internal reflection. Light rays passing between the boundaries of two optically transparent media of different densities will experience refraction and change direction according to Snells Law:—

$$n_1 \text{ Sin } \theta_1 = n_2 \text{ Sin } \theta_2 \qquad \text{Snells Law}$$

where n_1 and n_2 are the indices of refraction of the two media.

Figure 2 **Principles of Internal Reflection**



If rays pass from a dense to a less dense medium (i.e. $n_1 > n_2$) then at a certain value of θ_1 the resultant θ_2 will be 90°. This value θ_1 is known as the critical angle and is denoted θC, See fig. 2.

$$\text{so,} \quad n_1 \text{ Sin } \theta C = n_2 \text{ Sin } 90°.$$

$$\text{Sin } \theta C = \frac{n_2}{n_1}$$

Numerical Aperture

In a fibre, rays which are internally reflected rebound along the length of the fibre and only exit at the far end. Partially reflected rays lose power at each rebound and consequently die away rapidly.

Figure 3 **Step index fibre propagation modes**

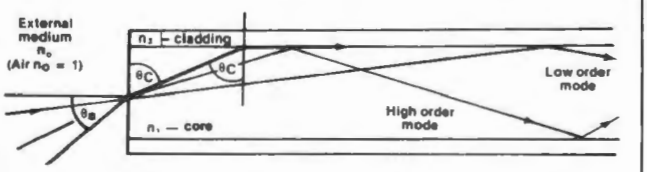


Fig. 3 shows the air/fibre interface. The angle θ_a is the maximum angle at which a ray incident to this interface can enter the core and experience total internal reflection. θ_a is called the Acceptance Angle and sin θ_a is known as the Numerical Aperture (NA).

Numerical Aperture = Sin θ_a.

From Snells Law:

$$n_o \text{ Sin } \theta_a = n_1 \text{ Sin } (90° - \theta_c)$$
$$= n_1 \text{ Cos } \theta_c$$
$$= n_1 \sqrt{1 - \text{Sin}^2 \theta_c}$$
$$= n_1 \sqrt{1 - (n_2/n_1)^2}$$

When $n_0 = 1$ (i.e. air)

$$\text{Sin } \theta_a = \sqrt{n_1^2 - n_2^2}$$

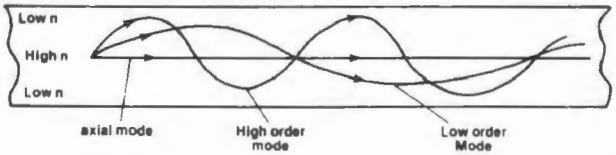
Propagation modes

Light rays in a fibre may be classified as meridional and skew. Meridional rays are those that pass through the axis of a fibre after each rebound, while skew rays never intersect the fibre axis. There are also parallel rays which travel directly down the fibre, never being reflected. Basic fibre theory is concerned with meridional rays. These fall into two categories, low order modes and high order modes (see fig. 3). Low order modes are those rays launched at small angles within the acceptance angle, while high order modes occur when rays are launched at large angles. Single-Mode fibres result when the core area and the NA are so small that only one mode can propagate. Other modes of propagation do exist but these disappear or do not affect the basic theory.

Fibre construction

Two types of fibre construction are commonly in use. A **step-index** fibre which consists of a cylindrical core of glass, silica or plastic of refractive index n_1, covered by a thin cladding of a lower refractive index n_2. The second type is a **graded index** fibre whose refractive index changes gradually from a high refractive index at the centre to a lower index towards the perimeter. This causes the rays to propagate as in fig. 4.

Figure 4 **Graded index fibre propagation modes**



Dispersion

Two types of dispersion are encountered in fibres which limit bandwidth. **Material** dispersion and **Modal** dispersion. Material dispersion results from the fact that different wavelengths travel at different velocities in the same medium. Consequently, the various wavelengths launched simultaneously within the flux will not arrive at the receiver simultaneously but will suffer time dispersion due to differences in travel time. This effect can be reduced by using an emitter with a narrow spectrum of emission (e.g. laser).

Modal dispersion is caused by the difference in path lengths between low order modes and high order modes. As can be seen in fig. 3 and fig. 4 the high order modes have a longer travel time than the lower order modes and simultaneously launched rays will suffer dispersion on arrival. Modal dispersion can be reduced in step-index fibres by decreasing the NA to allow only the lower modes to

propagate. In graded-index fibres the effect is compensated for by the high order modes travelling faster in the lower-index regions, so the time differential between high and low order modes is not as large in graded-index fibres as it is in step-index fibres.

Dispersion is generally only a problem in long distance communications and consequently graded-index fibres, although more costly than step-index fibres, are used in these applications in conjunction with lasers. For shorter distances (< 500m) and/or lower bandwidth step-index fibres are favoured for lower costs and easier coupling methods.

Transmission loss
There are four main causes of transmission loss in optical fibres:—

i) Material absorption
ii) Material scattering
iii) Scattering due to irregularities at the core/cladding interface
iv) Radiation due to curvature.

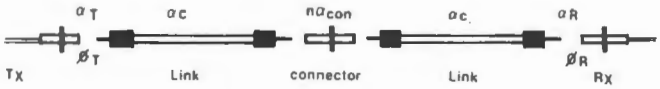
Material absorption is caused by molecular impurities within the core of the fibre which absorb certain wavelengths. High purification processes during manufacture limit the problem — but are costly. Alternatively, a suitable emitter is chosen whose peak wavelength corresponds approximately to the spectral region of maximum transmission of the fibre. Plastic fibres, for example generally have minimum absorption between 630 and 670nm and are therefore recommended to be used with visible red emitters.

Material scattering is caused by particle impurities and by fluctuations in temperature and composition (Rayleigh scattering) which interrupts the reflection paths of the light rays.
Further scattering is caused by **irregularities** at the core/cladding interface which results in transmission into the cladding and subsequent loss of energy on reflection.

Curvature of the fibre may also cause losses. If the curvature is too great some rays will strike the boundary at angles less than the critical angle and partial transmission into the cladding will occur, with a resultant loss of reflection.
The first three conditions contribute to the overall attenuation of the fibre given in dB/km.

Coupling losses
In addition to the losses inherent in a fibre, coupling losses must be considered when designing a fibre optic link. The three main loss mechanisms are, fibre to fibre (in-line), fibre to fibre (bulkhead) and fibre to emitter/detector unit. In the case of the RS plastic and glass systems a maximum figure is quoted for each coupling in dB. The loss is due to a number of factors but in particular, reflections at the mating faces, slight misalignment due to manufacturing tolerances and separation between the mating faces. The latter is deliberately engineered to prevent scratch damage to the fibre faces when the coupling is made.

Attenuation calculations



$$\text{Overall attenuation} = 10 \log_{10} \frac{\varnothing_T}{\varnothing_R}$$
$$= \alpha_T + \alpha_{C_1} + n\alpha_{con} + \alpha_{C_2} + \alpha_R$$

where $\varnothing_T$ and $\varnothing_R$ is the power in μW transmitted and received respectively.
α_T and α_R are the coupling losses between the fibre and transmitter and receiver respectively.
$n\alpha_{con}$ is the total insertion loss due to 'n' number of coupling connectors (i.e.) in-line or bulkhead).
α_{C_1} and α_{C_2} are the attenuation figures of the individual lengths of cable involved in the link.

The above equation applies to the RS fibre-optic systems. The attenuation figures for each part of the link can be found in the specification sections of this data sheet.

N.B. It is important for system performance to keep connections to a minimum. It may be advantageous in certain instances to use a longer length of cable rather than incur coupling losses, by using in-line connectors to join shorter lengths in order to make up the desired distance.

Generally in designing a system, the flux which the transmitter produces and the length over which the data is to be transmitted is known. From the above attenuation equation, the flux appearing at the fibre/receiver interface can be calculated and a suitable circuit designed to amplify the received signal.

Typical calculation (glass system)

For the infra-red emitter the maximum power $\varnothing_T$ which can be injected into the fibre is 20μW (I_F = 100mA), see specification section. Assuming a 10m length of cable joins the emitter and detector with no in-line or bulkhead connectors present we have for a glass link:–

$\alpha_T = \alpha_R = 0.5$dB, $\alpha C = 1.3$dB } See glass system specification

$$10 \log (\varnothing_T/\varnothing_R) = \alpha_T + \alpha_C + \alpha_R = 2.3$$

$$\log (\varnothing_T/\varnothing_R) = 0.23$$

$$\varnothing_T/\varnothing_R = 1.7$$

$$\varnothing_R = 20/1.7\mu W$$

$$= 11.7\mu W$$

The spectral sensitivity of the detector S = 0.53 A/W.

$$\therefore \text{Detector current} = 0.53\ \varnothing_R$$
$$= 6.2\mu A.$$

Specification — Polymer System

Polymer Cable (368-047)

Core material	Polymethyl methacrylate
Cladding material	fluorinated polymer
Sheath material	black polyethylene
Core/cladding diameter	1.00mm
Overall diameter	2.25mm
Optical construction	step index
Numerical aperture	0.47
Attenuation at 600nm	150dB/km (max)
Minimum bend radius	15mm
Tensile strength	5kg
Operating temp range	–30° to +85°C
Maximum temperature	100°C

End-Termination (456-396)

Ferrule material	nickel-silver
Coupling nut material	nickel plated brass
Heatshrink sleeving	polyolefin with inner adhesive lining
Coupling loss per connector	2dB (max)

Bulkhead Connector (456-403)

Material	nickel plated brass
Insertion loss	2.5dB (max) per coupling

Emitter (309-290)

Absolute max. ratings of L.E.D.

Reverse voltage V_R	3.0 V
Forward current I_F	100 mA

Peak current (100μs pulse width 1% duty cycle) I_F = 1.0A

Power dissipation (T_A = 25°C) P_{TOT} : 200mW, derate linearly from T_A = 25°C at 2.6mW/°C

Operating temperature —55°C to + 100°C

Electrical characteristics (T_A = 25°C)

	Min.	Typ.	Max.	Units
Forward voltage (I_F = 100mA) V_F	—	2.0	2.5	V
Reverse breakdown voltage (I_R = 10μA) BV_R	3.0	8.0	—	V

Optoelectronic characteristics (I_F = 100mA, T_A = 25°C)

Axial luminous intensity I_L	150 mcd typ. (50 mcd min).
Axial radiometric intensity I	4.0 mW/sr typ.
Peak spectral wavelength λpk	670 nm typ.
Spectral bandwidth $\Delta\lambda$	20 nm typ.
Light o/p rise and fall times (t_r and t_f) †	10ns typ.
Capacitance (V_R = O, f = 1 MHz) Co	100 pf typ.

†time for a 10%-90% change in intensity with step change in current.

Figure 5 **Emission Spectrum**

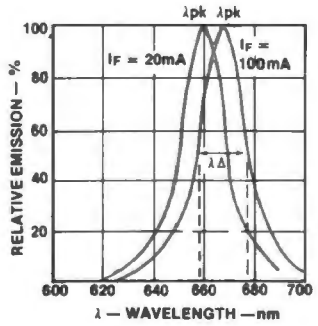
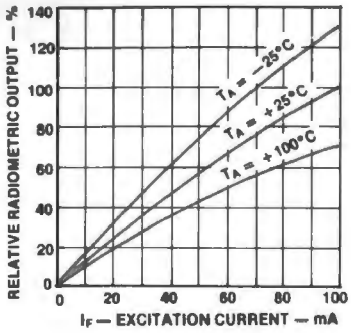


Figure 6 **Relative radiometric o/p vs I_F**

NB. Normalisation: LED Intensity ≙4mW/sr (Sensor 1mm² area).



Detector (309-307)

Absolute max. ratings of PIN photodiode

Reverse voltage V_R : 50V
Power dissipation (T_A = 25°C) P_{TOT} : 250 mW,
derate linearly from T_A = 25°C at 2.5 mW/°C
Junction temperature θj : 125°C
Operating temperature −55°C to + 100°C

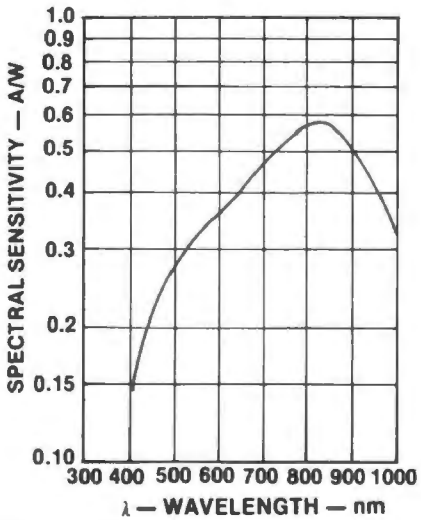
Optoelectronic characteristics (T_A = 25°C)

Peak spectral wavelength λpk 850 nm
Spectral sensitivity S 0.44 A/W (670nm)

Rise time of photocurrent
R_L = 50Ω, V_R = 20V, λ = 900nm) t_r 1ns typ., 5ns max.
Capacitance V_R = 0V 15 pF
V_R = 1V 12 pF
V_R = 20V 3.5 pF

Cut off frequency
R_L = 50Ω, V_R = 20V, λ = 900nm) 500 MHz
Dark current (V_R = 20, E = O) ≤5 nA
Noise equivalent power
(V_R = 20V) 3.3×10^{-14} W/√Hz

Figure 7 **Spectral sensitivity as a function of light wavelength**



Construction – Emitter and Detector

Both the L.E.D. and PIN photodiode are housed in nickel-plated brass bodies designed for bulkhead mounting. The devices are optically aligned prior to potting to give maximum output.

Coding: Black sleeved lead – emitter – L.E.D. cathode
Red sleeved lead – detector – photodiode anode.

Specification – Glass System

Optical Leads – Cable

Core/cladding material glass
Pre-sheath material polypropylene
Core diameter 100μm
Cladding diameter 140μm
Optical construction Step index
Numerical aperture 0.26
Attenuation at 840nm 5dB/km (typ).
(N.B. Lead attenuations quoted below)
Bandwidth (1km) >100MHz
Outer sheath material polyurethane
Strength members fibreglass
Overall diameter 4.5mm
Tensile strength 30kg
Resistance to radial pressure 15 bars
Minimum bend radius 80mm
Operatating temp. range –40°C to +90°C (cable + fibre)

Optical Leads – Connector

Type SMA (U.S. MIL Std.)
Material bronze-beryllium
Connector mating torque 80-100 Newtons
Insertion loss per connector 0.5dB typ.

Optical Leads – Attenuation

Length	Stock No.	α at 840nm (max.)
2m	368-069	1.0dB
5m	368-075	1.1dB
10m	368-081	1.2dB
20m	368-097	1.5dB
25m	368-104	1.6dB
50m	368-110	1.8dB
100m	368-126	2.0dB

In-Line Connector (456-419)

Type SMA screw thread
Material bronze-beryllium
Separation, fibre/fibre 0.3mm max.
Insertion loss 1dB typ.

Bulkhead Connector (456-425)

Type	SMA screw thread four hole flange for panel mounting
Material	bronze-beryllium
Separation, fibre/fibre	0.3mm max.
Insertion loss	1dB typ.

Emitter (309-515)

Absolute maximum ratings of LED

Reverse voltage V_R	1.0V
Forward current I_F	100mA
Operating temperature	−40°C to +100°C

Electrical characteristics (T_A = 25°C)

Forward voltage (I_F = 100mA) V_F	1.6V typ., 2.0V max
Series resistance R_S	1.6 Ω typ.
Device capacitance C_T	800pF typ.

Opto electronic characteristics (T_A = 25°C)

Power output (I_F = 100mA) P_O	500μW typ.
Response time (IV dc bias, I_{PEAK} = 100mA)	12ns typ.
Peak emission wavelength (I_F = 50mA) λp	820nm typ.
Spectral bandwidth △λ	35nm typ.

Figure 8 **Emission Spectrum**

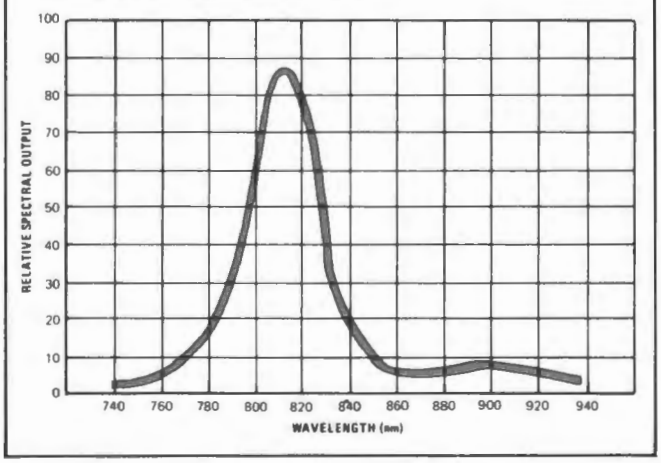
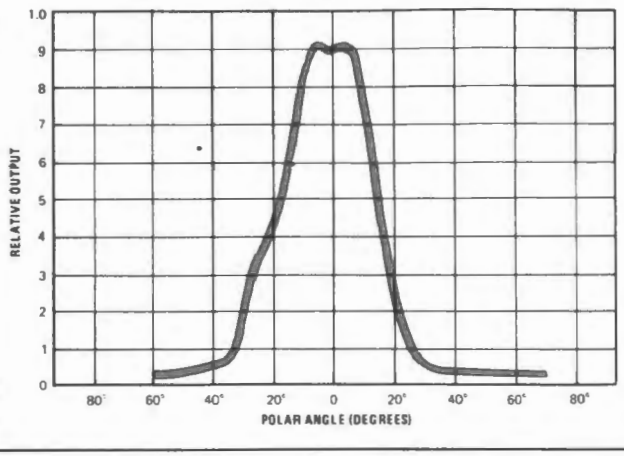


Figure 9 **Radiant intensity**



Detector (309-521)

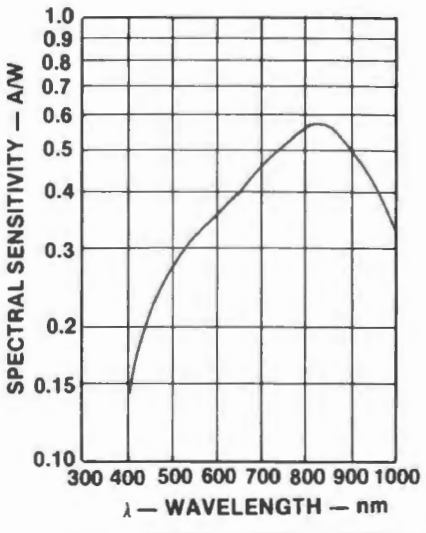
Absolute max. ratings of PIN photodiode

Reverse voltage V_R	50V
Power dissipation (T_A = 25°C) P_{TOT}	250mW
derate linearily from T_A = 25°C at	2.5mW/°C
Junction temperature θ_j	125°C
Operating temperature	− 55°C to + 100°C

Optoelectronic Characteristics (T_A = 25°C)

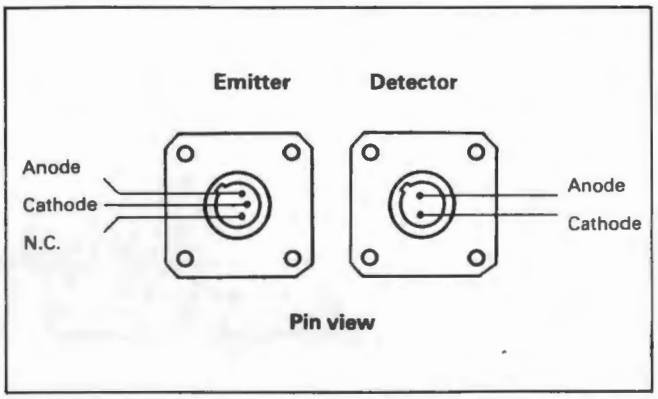
Peak spectral wavelength λmax	850nm
Spectral sensitivity S	0.53 A/W (890nm)
Rise time of photocurrent (R_L = 50Ω, V_R = 20V, λ = 900nm) t_r	1ns typ., 5ns max.
Capacitance V_R = 0V	15pF
V_R = 1V	12pF
V_R = 20V	3.5pF
Cut off frequency (R_L = 50Ω, V_R = 20V, λ = 900nm)	500MHz
Dark current (V_R = 20V E = O)	≤5 nA
Noise equivalent power (V_R = 20V)	3.3×10^{-14} W/√Hz

Figure 10 **Spectral sensitivity as a function of light wavelength**



Construction – Emitter and Detector

Both the LED and PIN photodiode are housed in SMA styled bulkhead mounting bases. The devices are optically aligned prior to potting to give maximum output.



Applications

General Illumination

The polymer cable can be used in its own right to illuminate inaccessible areas. Using only one filament lamp or light source many independent items can be illuminated, thereby improving reliability and decreasing servicing time in terms of bulb failure. Such applications include illumination in mimic displays, teaching aids e.g. maps, plans etc, panel instruments e.g. meters, switches, dials etc. Other applications include illumination of microscopes, tool tips, proximity sensing and remote sensing of light sources.

Data Transmission

Figure 11 **Transmitter — TTL interface**

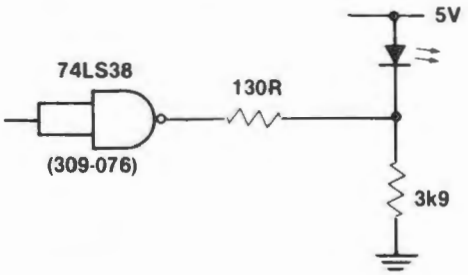
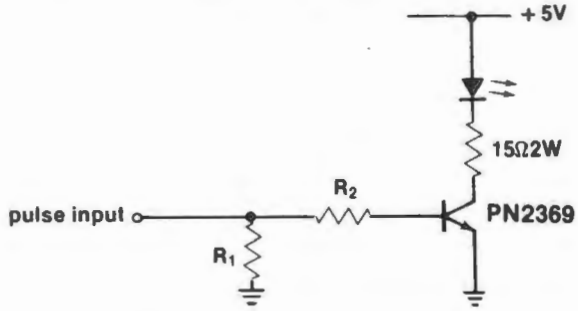
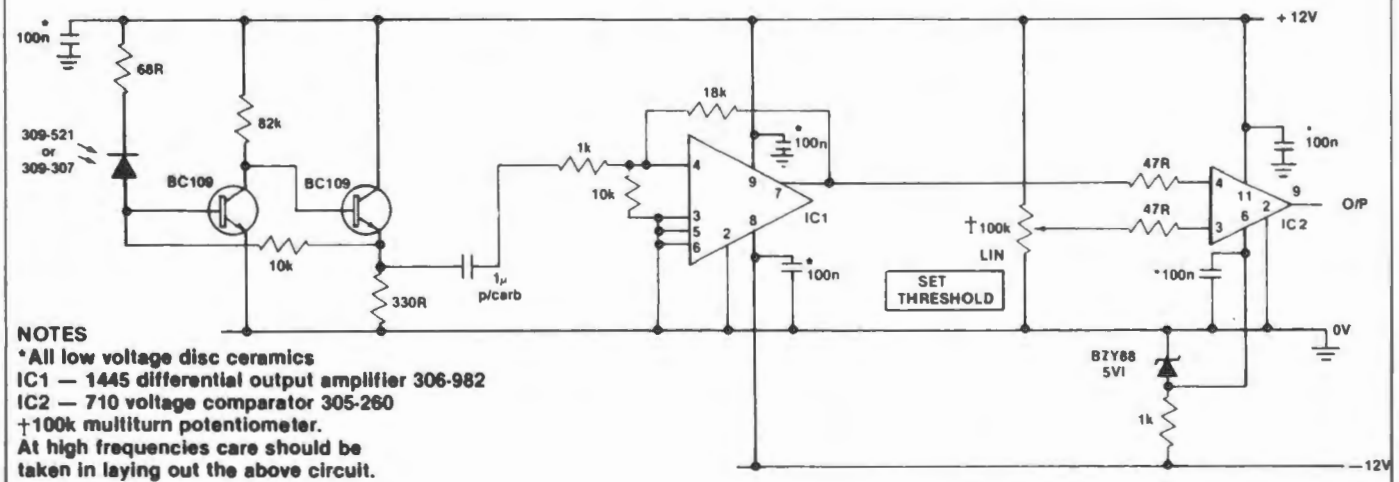


Figure 12 **Transmitter — general interface**



R_1 and R_2 should be chosen to match pulse source to base of PN2369.

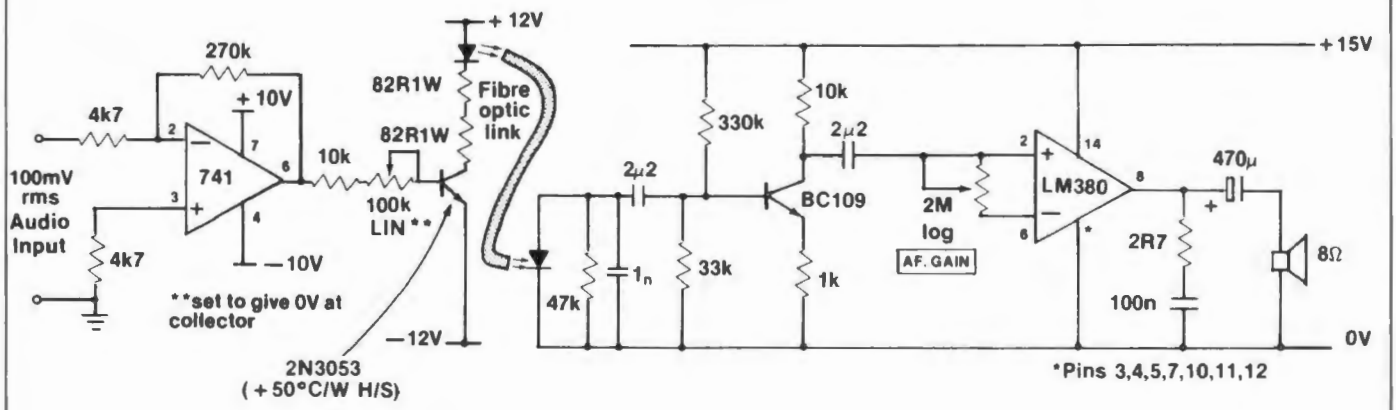
Figure 13 **Receiver — high speed 5M Bits/Sec**



NOTES
***All low voltage disc ceramics**
IC1 — 1445 differential output amplifier 306-982
IC2 — 710 voltage comparator 305-260
†100k multiturn potentiometer.
At high frequencies care should be taken in laying out the above circuit.

RS data

Figure 14 **Audio demonstration link**



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RS data

Universal asynchronous receiver transmitter 6402 and 6402-1

Stock numbers 309-284 and 304-144

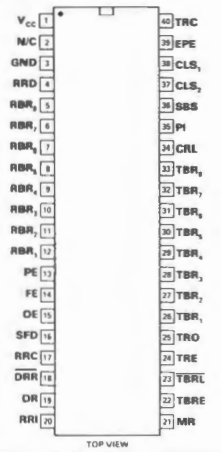
The RS Universal asynchronous receiver transmitters, UARTS are designed for interfacing an asynchronous serial data channel and a parallel data channel. The devices can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems.

The transmitter converts parallel data into serial form and automatically adds start, parity and stop bits. The receiver converts serial start, data parity and stop bits to parallel data verifying proper code transmission, parity and stop bits. Utilising CMOS – LSI technology the devices operate at low power levels and can be clocked at frequencies up to 1 MHz (6402) or 2 MHz (6402-1). Several status output flags are provided thereby increasing flexibility and simplifying the user interface.

Features

- Two speed options up to 1 MHz 6402 or 2 MHz 6402-1
- Low power – less than 10 mW at 2 MHz
- Programmable word length, stop bits and parity
- Automatic data formatting and status generation
- CMOS and LS TTL compatible.

PIN CONNECTIONS



Absolute maximum ratings

Operating temperature range ——— −40°C to +85°C
Storage temperature ——— −65°C to +150°C
Supply voltage ——— +7.0 V d.c.
Voltage on any input or output pin ——— −0.3 V to V_{CC}+0.3 V

d.c. characteristics

Test conditions: V_{CC} = 5 V d.c. ±5%, T_{amb} = 25°C 6402-1 characteristics in ( ) where different.

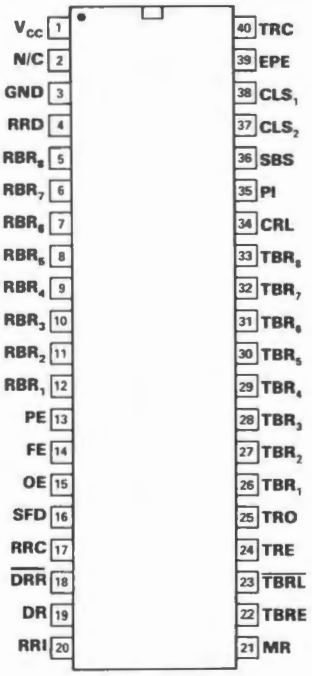
Parameter	Condition	Min.	Typ.	Max.	Unit
Input voltage High V_{IH}		V_{CC} − 2.0			V
Input voltage Low V_{IL}				0.8	V
Input leakage I_{IL}	$G_{nd} \leq V_{IN} \leq V_{CC}$	−5.0 (−1)		5.0 (1)	μA
Output voltage High V_{OH}	I_{OH} = −0.2 mA	2.4			V
Output voltage Low V_{OL}	I_{OL} = 1.6 mA			0.45	V
Output leakage I_{OL}	$G_{nd} \leq V_{OUT} \leq V_{CC}$	−5.0 (−1)		5.0 (1)	μA
Power supply current I_{CC}	$V_{IN} = G_{nd}$ or V_{CC}		1.0	800 (100)	μA
Input capacitance C_{IN}			7.0	8.0	pF
Output capacitance C_O			8.0	10.0	pF

a.c. characteristics

Test conditions : V_{CC} = 5 V d.c. ±5%, T_{amb} = 25°C 6402-1 characteristics in ( ) where different.

Parameter	Condition	Min.	Typ.	Max.	Unit
Clock frequency f_c		d.c.		1.0 (2.0)	MHz
Power supply current I_{CC}	f_c = 500 kHz			1.2 (1.9)	mA
Pulse widths t_{pw}	see timing diagrams	225 (150)	50		ns
Pulse width t_{MR}	see timing diagrams	600 (400)	200		ns
Input data setup time t_{DS}	see timing diagrams	75 (50)	20		ns
Input data hold time t_{DH}	see timing diagrams	90 (60)	40		ns
Output enable time t_{EN}	see timing diagrams		80	190 (160)	ns

Pin connections



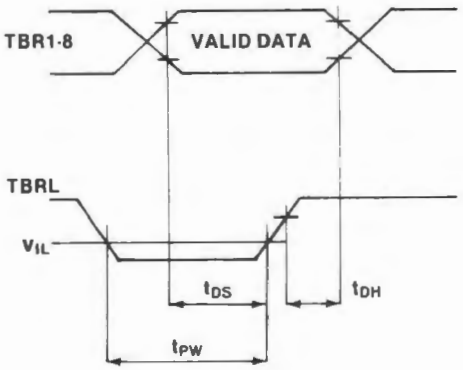
TOP VIEW

Pin definition

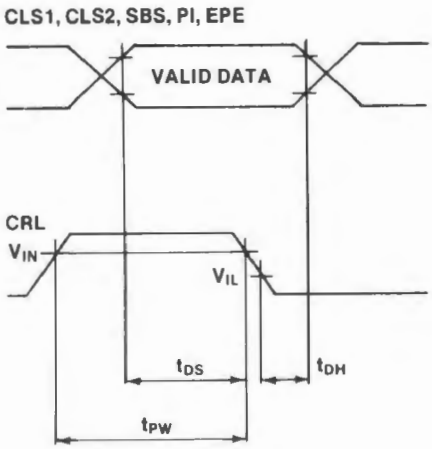
V_{CC}	+V supply
N/C	No Connection
GND	GROUND
RRD	RECEIVER REGISTER DISABLE
$RBR_{1.8}$	RECEIVER BUFFER REGISTER OUTPUTS
PE	PARITY ERROR
FE	FRAMING ERROR
OE	OVERRUN ERROR
SFD	STATUS FLAGS DISABLE
RRC	RECEIVER REGISTER CLOCK
$\overline{DRR}$	DATA RECEIVED RESET
DR	DATA RECEIVED
RRI	RECEIVER REGISTER INPUT
MR	MASTER RESET
$\overline{TBRE}$	TRANSMITTER BUFFER REGISTER EMPTY
$\overline{TBRL}$	TRANSMITTER BUFFER REGISTER LOAD
TRE	TRANSMITTER REGISTER EMPTY
TRO	TRANSMITTER REGISTER OUTPUT
$TBR_{1.8}$	TRANSMITTER BUFFER REGISTER INPUTS
CRL	CONTROL REGISTER LOAD
PI	PARITY INHIBIT
SBS	STOP BIT SELECT
$CLS_{1.2}$	CHARACTER LENGTH SELECT
EPE	EVEN PARITY ENABLE
TRC	TRANSMITTER REGISTER CLOCK

Timing diagrams

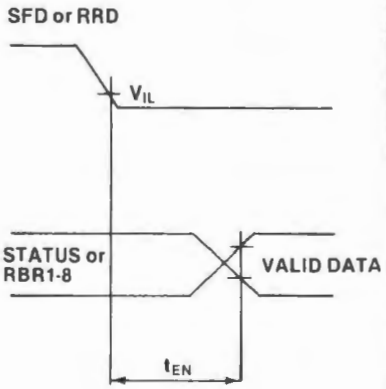
Data input cycle



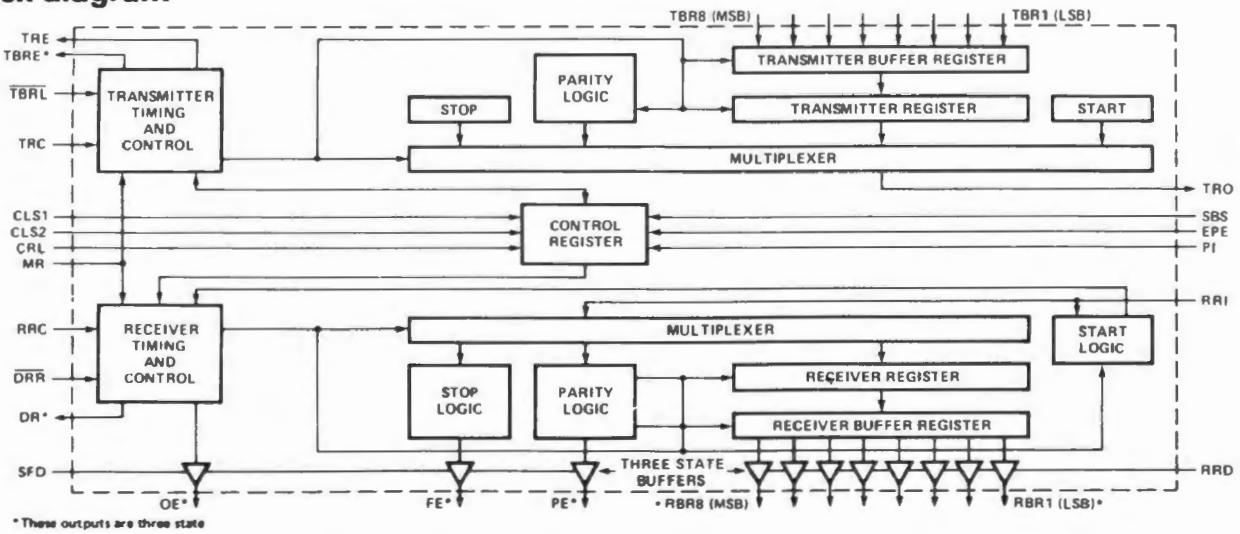
Control register load cycle



Status flag enable time or Data Output enable time



Block diagram



Control inputs

RRD – Receiver register disable – a high level on this input forces the receiver holding register outputs RBR1 – RBR8 to a high impedance state thus allowing direct connection in data bus applications.

SFD – Status flag disable – a high level forces the outputs PE, FE, OE, DR, and TBRE (see status flag description) to a high impedance state.

$\overline{\text{DRR}}$ – Data received reset – a low level on this input clears Data received output (DR) to a low level thereby permitting the next character to be received without an overrun error.

MR – Master reset – a high level clears the PE, FE, OE, DR, and TRE status flags and sets the TBRE and TRO outputs high. Eighteen clock periods after MR goes low, TRE returns high. Note: MR does not clear the receiver buffer register.

CRL – Control register load – a high level loads the control register with the character length, parity and stop bit length. See control register description below.

$\overline{\text{TBRL}}$ – Transmitter buffer register load – a low level transfers data from the inputs TBR1 to TBR8 into the transmitter buffer register. A low to high transition on this input requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed until the current transmission is completed at this point the next character is loaded and transmission of that character commences so that the two characters are transmitted end to end.

Control register – The following inputs are used to set the control register status when the CRL input goes high.

CLS1, CLS2 – Character length select – these two inputs select the character length according to the following table.

Character length (bits)	5	6	7	8
CLS1	L	H	L	H
CLS2	L	L	H	H

PI – Parity inhibit – a high level inhibits parity generation, parity checking and forces the PE status flag output low. This input overrides the EPE input.

EPE – Even parity enable – when the PI is set low a high level on the EPE input generates and checks even parity conversely a low level selects odd parity.

SBS – Stop bit select – this input selects the number of stop bits. The number of stop bits added to the transmitted character also depends on the character length selected by the CLS1 and CLS2 inputs. The following table lists the number of stop bits selected versus the character length and state of the SBS input.

	Character length selected		
SBS input	5 bits	6, 7 or 8 bits	
L	1	1	Stop bits
H	1½	2	

Status flags

TBRE* – Transmitter buffer register empty – a high level on this output indicates that the transmitter buffer register has transferred its contents to the transmitter register and is ready to accept new data.

TRE – Transmitter register empty – a logic high level indicates the transmission is completed including stop bits.

PE* – Parity error – a high level on parity error indicates that the received parity does not match the parity programmed by the control register bits. When parity is inhibited (refer to PI control input) the output is forced low.

FE* – Framing error – a high level indicates the first stop bit is invalid.

OE* – Overrun error – a high level indicates the data received flag was not cleared before the last character was transferred to the receiver register buffer.

DR* – Data received – a high level indicates a character has been correctly received and transferred to the receiver buffer register – this output must be reset before a new character can be received (refer to $\overline{\text{DRR}}$ control input).

* Status flags are three state and can be disabled (high impedance state) by using the status flags disable input (SFD) – refer to control input description.

Data inputs and outputs

RBR1 to RBR8 – The contents of the receiver buffer register appears on these outputs. Word formats less than 8 bits are right justified to RBR1. The outputs are forced to a high impedance state by applying a logic high to the RRD input.

RRI – Receiver register input – serial data on this input is clocked into the receiver register.

TBR1 to TBR8 – Character data is loaded into the transmitter buffer register via these inputs in conjunction with the $\overline{\text{TBRL}}$ input. For character formats of less than 8 bits, the TBR8, 7 or 6 inputs are ignored corresponding to the programmed character length.

TRO – Transmitter register output – character data, start, stop and parity bits appear serially at this output.

RS data

Clock inputs

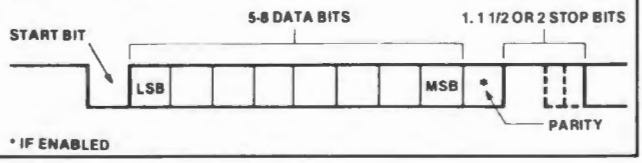
RRC – Receiver register clock – this input determines the rate at which the received data is clocked into the receiver register. The actual clock frequency should be 16 times the required data rate.

TRC – Transmitter register clock – this input sets the transmitted data rate. The frequency of the clock should be 16 times the required data rate.

Transmitter operation

The transmitter section accepts parallel data, formats and transmits in serial form adding start, parity (if selected) and stop bits as shown in Fig. 1.

Figure 1: **Word format**



The sequence of events prior to and following the transmission of the data is described below together with the aid of the timing diagram shown in Fig. 2.

Ⓐ Data is loaded into the TBR from the inputs TR1 to TBR8 by a logic low on $\overline{TBRL}$. Valid data must be present t_{DS} prior to the low to high transition of $\overline{TBRL}$ and remain valid at t_{DH} after this transition. If the data is less than 8 bits only the least significant bits are accepted. Following the transition of $\overline{TBRL}$ from low to high TBRE goes low indicating the TRB is not empty. If the transmitter register TR, is empty indicated by the TRE status output being high the data is transferred to the TR and transmission commences Ⓑ between 0 to 1 clock periods later. Should $\overline{TBRL}$ go low again during the transmission shown at Ⓒ in Fig. 2 the data is loaded into the TBR as before and the TBRE status goes low following the $\overline{TBRL}$ low to high transition however the data is not immediately loaded into the TR, due to the transmission in progress, instead the data remains in the TBR until the last stop bit of the current transmission has been transmitted.

At Ⓓ the data-in the TBR is automatically transferred into the TR and transmission of that character commences.

Receiver operation – refer to Fig. 3.

Data is received in serial form at the RR1 input, when no data is being received this input must remain high, the data is clocked into the RR at the clock rate which should be 16 times the required data rate. A low level on the $\overline{DRR}$ clears the DR line and during the first stop bit data is transferred from the RR to the RBR. If the word length is less than 8 bits the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1.

A logic high on the OE status output indicates an overrun which occurs when the DR line has not been cleared before the present character was transferred to the RBR. A logic high on PE indicates a parity error.

One half clock cycle after the data is transferred to the RBR the DR line is set high and FE is evaluated. A logic high on the FE output indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a correct stop bit is received.

Figure 2: **Transmitter timing**

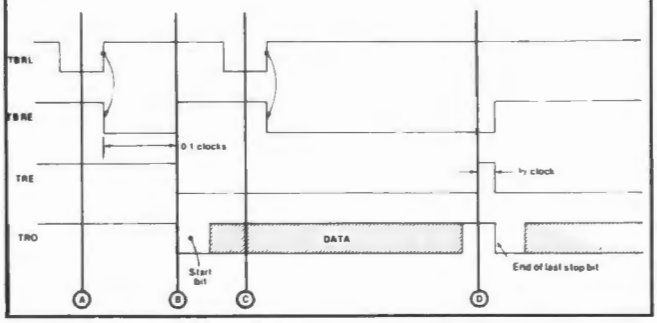
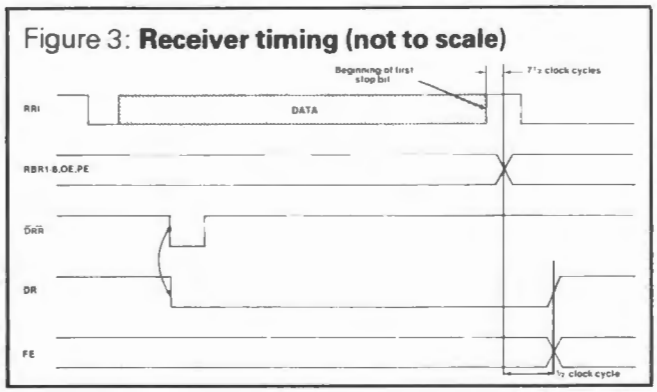


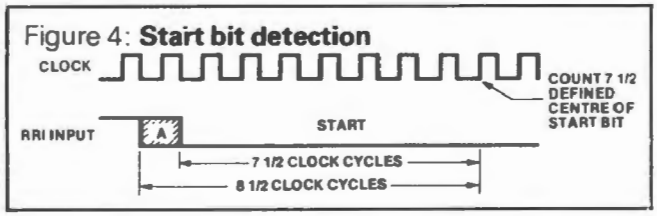
Figure 3: **Receiver timing (not to scale)**



Start bit detection

The receiver uses a 16 times clock for timing. The start bit Ⓐ in Fig. 4 could have occurred as much as one clock cycle before it was detected, as indicated by the crosshatched section. The centre of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the centre of the start bit will be located within ±½ clock cycles, ±1/32 bit or 3.125%. The receiver begins searching for the next start bit at the centre of the first stop bit.

Figure 4: **Start bit detection**



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RS data

A/D Converter i.c.

Stock number 309–464

The RS427 is an 8-bit bipolar successive approximation A to D converter I.C. This versatile device incorporates tri-state output buffers to permit bussing on common data lines, a voltage switching D to A converter, a 2.5V precision reference, a fast comparator and approximation logic. Operation is from a +5V and −3 to −30V supplies and the data outputs are TTL compatible.

The use of the internal reference is optional to retain flexibility, permitting an external reference to be employed.

Just 3 resistors and 1 capacitor are required to construct an accurate high speed A/D converter circuit suitable for many applications.

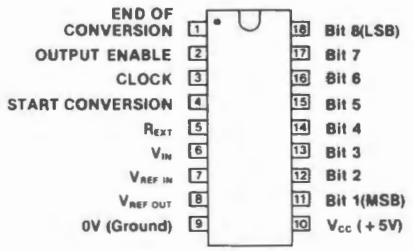
Absolute maximum ratings

Supply voltage V_{cc} ..... +7.0V
Max. voltage, logic and V_{REF} INPUTS ..... V_{CC}
Operating temperature range ..... 0°C to + 70°C
Storage temperature range ..... −55°C to +125°C

Features

- Fast; 15μs conversion time guaranteed
- 3-state outputs, TTL compatible
- Internal or external reference
- No missing codes over operating temperature range
- Unipolar and bipolar input ranges
- Ratiometric conversion
- +5V and −3V to −30V supplies
- Microprocessor compatible.

Pin connections



TOP VIEW

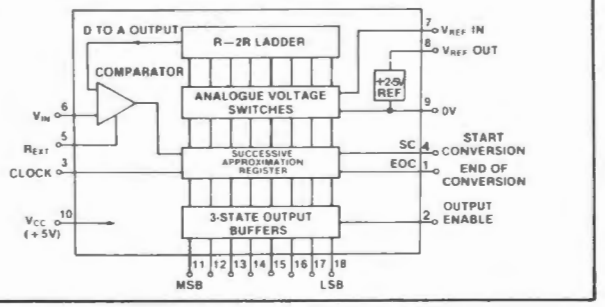
Electrical characteristics V_{CC} = 5V, T_{amb} = 25°C unless otherwise specified.

	Conditions	Min.	Typ.	Max.	Units
Internal Voltage Reference					
Output Voltage	R_{REF} = 390Ω, C_{REF} = 1µF	2.475	2.550	2.625	V
Slope Resistance			0.5	2	Ω
V_{REF} Temperature Coefficient			50		ppm/°C
Reference Current	See REFERENCE Page 2	4		15	mA
Comparator					
Input Current	V_{IN} = 3V, R_{EXT} = 82kΩ, V− = −5V		1		µA
Input Impedance			100		kΩ
Tail Current, I_{EXT}		25		150	µA
Negative Supply, V−	See COMPARATOR Page 2	−3.0		−30.0	V
Input Voltage		−0.5		3.5	V
Converter					
Linearity Error				±0.5	LSB
Differential Non-Linearity			±0.5		LSB
Linearity Error T.C.			±3		ppm/°C
Differential Non-Linearity T.C.			±6		ppm/°C
Full Scale (Gain) T.C.	External Ref. 2.5V		±2.5		ppm/°C
Zero T.C.			±8		µV/°C
Zero Transition (00000000→00000001)	$V_{REF\ IN}$ = 2.560V	12	15	18	mV
F.S. Transition (11111110→11111111)	$V_{REF\ IN}$ = 2.560V	2.545	2.550	2.555	V
Conversion Time			10	15	µs
External Reference Voltage		1.5		3.0	V
Supply Voltage (V_{CC})		4.5		5.5	V
Supply Current			25	40	mA
Power Consumption			125		mW
Logic (over operating temp.)					
High Level Input Voltage		2			V
Low Level Input Voltage				0.8	V
High Level Input Current	V_{IN} = 5.5V, V_{CC} = max.			50	µA
	V_{IN} = 2.4V, V_{CC} = max.			15	µA
High Level Input Current Clock Input	V_{IN} = 5.5V, V_{CC} = max.			100	µA
	V_{IN} = 2.4V, V_{CC} = max.			30	µA
Low Level Input Current	V_{IN} = 0.4V, V_{CC} = max.			−5	µA
High Level Output Current I_{OH}				−100	µA
Low Level Output Current I_{OL}				1.6	mA
High Level Output Voltage	I_{OH} = max., V_{CC} = min.	2.4			V
Low Level Output Voltage	I_{OL} = max., V_{CC} = min.			0.4	V
Disabled Output Leakage	V_O = 2.4V			2	µA
Max. Clock Frequency	Note below	600	900		kHz
Clock Pulse Width		500			ns
Enable/Disable Delay Time	See Fig. 5			500	ns
Duration of Start Conversion (SC) Pulse		500			ns
Input Clamp Diode Voltage	I_{IN} = −8mA			−1.5	V

Note: 600 kHz clock corresponds to a conversion time of 15μs (nine clock periods).

The internal block diagram of the RS427 is shown in Fig. 1. The operation of the converter is detailed below followed by a consideration of relevant sections of the device.

Figure 1 **RS427 Block diagram**

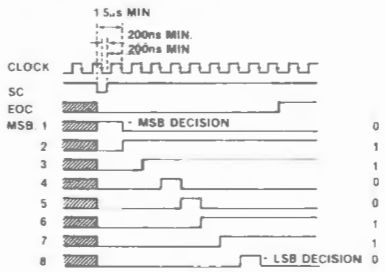


Operation

At the start of conversion the MSB is set to a 1 and all the other bits are set to 0. This produces a voltage output from the D to A converter of $\frac{1}{2}(V_{REF\ IN})$. This value is compared with the input voltage, V_{IN} and a decision is made on the first (negative) clock edge to set the MSB to 0 if $\frac{1}{2}(V_{REF\ IN}) > V_{IN}$ or retain a 1. Bit 2 is switched to a 1 on the same clock edge and on the next edge a decision is made regarding Bit 2, again by comparing the D to A output with V_{IN}. This process is repeated for all eight bits so that when the End of Conversion (EOC) output goes HIGH the digital output from the converter is a valid representation of V_{IN}. The binary output data is latched until the next Start Conversion (SC) pulse.
Detailed waveforms are shown in the Timing diagram (Fig. 2).

Conversion timing details

Figure 2 **Timing diagram**



Notes on timing diagram

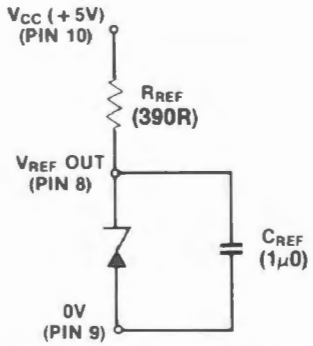
1. Conversion is initiated by a Start Conversion (SC) pulse which sets the MSB to 1 and all other bits to 0.
2. To allow for MSB settling, the first active (negative going) edge of Clock pulse after the SC pulse should not occur until at least 1.5μs after the negative edge of the SC pulse.
3. The positive edge of the SC pulse should not occur within 200 ns of an active clock edge.
4. As a special case of conditions (2) and (3) the SC pulse may be coincident with and of the same duration as a negative going clock pulse.
5. Cross hatching indicates a 'don't care' condition.
6. The output data is valid when End of Conversion (EOC) goes HIGH and remains latched until the next SC pulse.
7. The conversion sequence shown is for the digital word 01100110. For clarity the digital outputs are shown enabled during the conversion. Normally the outputs will be disabled during conversion and enabled after EOC goes HIGH.

Reference

(a) Internal reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 3). A resistor (R_{REF}) should be connected between Pins 8 and 10. The recommended value of 390Ω will supply a nominal reference current of (5.0 – 2.5)/ 0.39 = 6.4 mA. A stabilising/decoupling capacitor, C_{REF} (1μF), is required between Pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (Pin 8) is connected to $V_{REF\ IN}$ (Pin 7).
Up to five RS427s may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Figure 3 **Internal voltage reference**



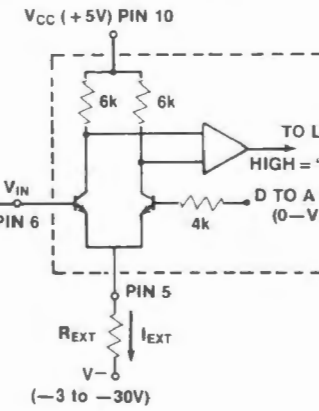
(b) External reference

If required an external reference voltage in the range +1.5 to +3.0V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

Comparator

The RS427 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 4.

Figure 4 **Comparator equivalent circuit**



The comparator derives the tail current, I_{EXT}, for its first stage from an external resistor, R_{EXT}, which is taken to a negative supply V–.
This arrangement allows the RS427 to work with any negative supply in the range –3 to –30V. The RS427 is designed to be insensitive to changes in I_{EXT} from 25μA to 150μA. The suggested nominal value of I_{EXT} is 65μA and a suitable value for R_{EXT} is given by $R_{EXT} = |V-|\ 15k\Omega$.

V− Volts	R_{EXT} (±10%)
−3	47kΩ
−5	82kΩ
−10	150kΩ
−12	180kΩ
−15	220kΩ
−20	330kΩ
−25	390kΩ
−30	470kΩ

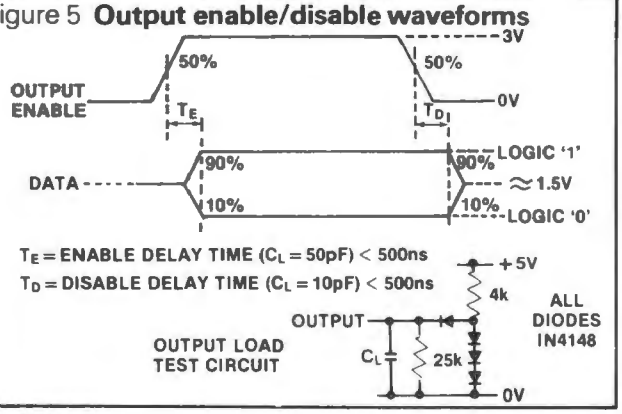
Typical preferred values of R_{EXT} for various levels of V−

The output from the D to A converter is connected through the 4kΩ ladder resistance to one side of the comparator. The analogue input to be converted could be connected directly to the other comparator input (V_{IN}. Pin 6) but for optimum stability with temperature the analogue input should be applied through a source resistance (R_{IN} = 3.9kΩ) to match the ladder resistance.

Logic outputs

The 3-state data outputs are OFF (high impedance) when Output Enable pin 2 is LOW. If EOC pin 1 is connected to pin 2 the data outputs will automatically be enabled when valid.
The output enabled/disable timing is shown in Fig. 5.

Figure 5 **Output enable/disable waveforms**

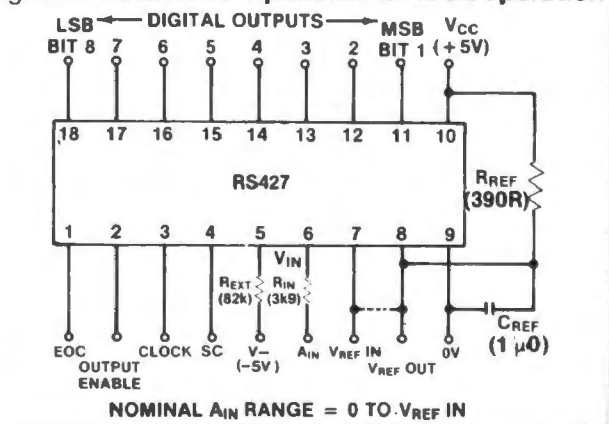


Applications

1. Unipolar Operation

The basic connection of the RS427 (Fig. 6) will accept an input signal from 0 to $V_{REF\,IN}$ which in some applications can be made directly available from previous conditioning/scaling amplifiers.

Figure 6 **External components for basic operation**



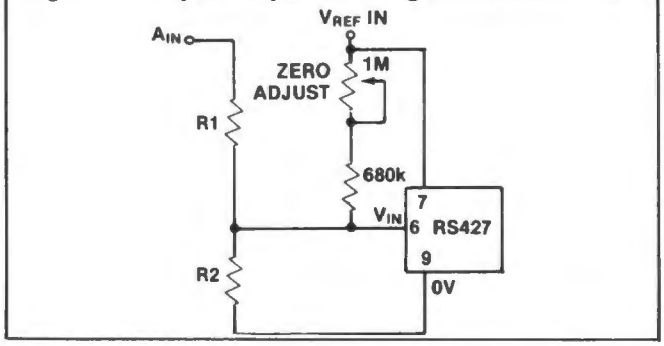
Other input ranges can be obtained by connecting a simple resistor network to V_{IN} (Pin 6) as shown in Fig. 7. The values of R_1 and R_2 are chosen so that V_{IN} = $V_{REF\,IN}$ when the Analogue Input (A_{IN}) is at full scale.

The resulting full scale range is given by

$$A_{IN}\,FS = \left(1 + \frac{R1}{R2}\right).V_{REF\,IN} = G.\,V_{REF\,IN}$$

To match the ladder resistance $R_1//R_2$ ($\approx R_{IN}$) = 4kΩ (3.9kΩ nearest preferred value).
The required nominal values of R_1 and R_2 are given by $R_1 = 4G\,k\Omega$, $R_2 = \frac{4G}{G-1}\,k\Omega$

Figure 7 **Unipolar operation – general connection**

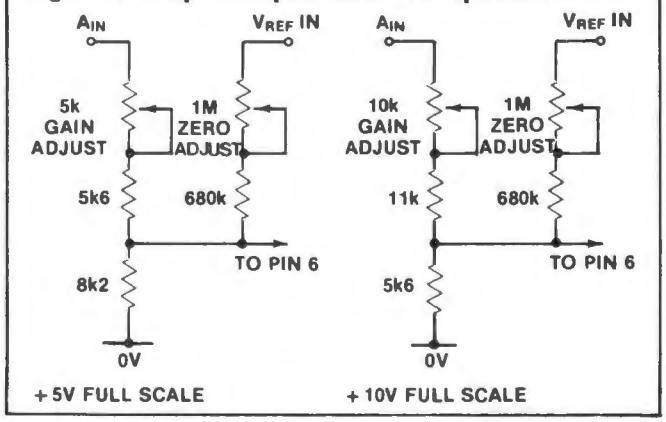


Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\,IN}$ = 2.5V.

Input Range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value.
Components for zero adjust are as shown (G≥1.5).
Practical circuit realisations for +5V and +10V input ranges are given in Fig. 8.

Figure 8 **Unipolar operation – component values**



Unipolar adjustment Procedure

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.
(ii) Apply full scale minus 1½ LSB to A_{IN} and adjust gain until Bit 8 (LSB) output just alternates between 0 and 1 with all other bits at 1.
(iii) Apply ½ LSB to A_{IN} and adjust zero until Bit 8 just alternates between 0 and 1 with all other bits at 0.

Unipolar setting-up points

Input Range, +FS	½ LSB	FS − 1½ LSB
+5V	9.8mV	4.9707 volts
+10V	19.5mV	9.9414 volts

$$1\ \text{LSB} = \frac{FS}{256}$$

RS data

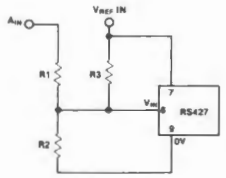
Unipolar logic coding

Analogue Input (A_{IN}) (Nominal code centre value)	Output Code (Binary)
FS −1 LSB	11111111
FS −2 LSB	11111110
¾ FS	11000000
½ FS +1 LSB	10000001
½ FS	10000000
½ FS −1 LSB	01111111
¼ FS	01000000
1 LSB	00000001
0	00000000

2. Bipolar Operation

For bipolar operation the input to the RS427 is offset by half full scale by connecting a resistor R_3 between $V_{REF\,IN}$ and V_{IN} (Fig. 9).

Figure 9 **Bipolar operation – general connection**

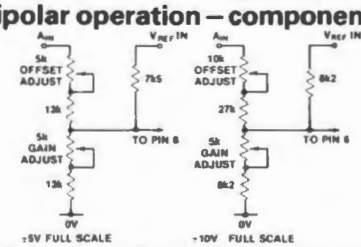


When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.
When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\,IN}$.
If the full scale range is $\pm G.V_{REF\,IN}$ then $R_1 = (G-1).R_2$ and $R_1 = G.R_3$ fulfil the required conditions.
To match the ladder resistance $R_1//R_2//R_3$ ($= R_{IN}$) = 4kΩ.
Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8Gk\Omega$, $R_2 = 8G/(G-1)k\Omega$, $R_3 = 8k\Omega$.
A bipolar input range of $\pm V_{REF\,IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\,IN}$) results if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$
Assuming that $V_{REF\,IN} = 2.5$ volts the nominal values of resistors for ±5V and ±10V input ranges are given in the following table.

Input Range	G	R_1	R_2	R_3
±5V	2	16kΩ	16kΩ	8kΩ
±10V	4	32kΩ	10.66kΩ	8kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.
Practical circuit realisations are given in Fig. 10.

Figure 10 **Bipolar operation – component values**



Note that in the ±5V case R_3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to obtain a more symmetrical range of adjustment using standard potentiometers.

Bipolar adjustment procedure

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.
(ii) Apply −(FS −½ LSB) to A_{IN} and adjust offset until the Bit 8 (LSB) output just alternates between 0 and 1 with all other bits at 0.
(iii) Apply +(FS −1½ LSB) to A_{IN} and adjust gain until Bit 8 just alternates between 0 and 1 with all other bits at 1.
(iv) Repeat Step (ii).

Bipolar setting-up points

Input Range, ±FS	−(FS −½ LSB)	+(FS −1½ LSB)
±5V	−4.9805V	+4.9414V
±10V	−9.9609V	+9.8828V

$1\,LSB = \frac{2FS}{256}$

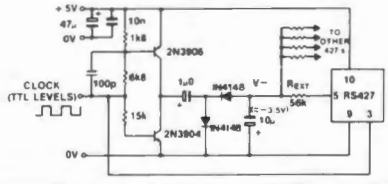
Bipolar logic coding

Analogue Input (A_{IN}) (Nominal code centre value)	Output Code (Offset Binary)
+(FS −1 LSB)	11111111
+(FS −2 LSB)	11111110
+½ FS	11000000
+1 LSB	10000001
0	10000000
−1 LSB	01111111
−½ FS	01000000
−(FS −1 LSB)	00000001
−FS	00000000

3. Single 5V supply rail operation

The RS427 takes very little power from the negative rail and so a suitable negative supply can be generated very easily using a 'diode pump' circuit. The circuit shown in Fig. 11 works with any clock frequency from 10kHz to 1 MHz and can supply up to five RS427s.

Figure 11 **Single 5V supply operation**



4. Ratiometric operation.

If the output from a transducer varies with its supply then an external reference for the RS 427 should be derived from the same supply. The external reference can vary from +1.5V to +3.0V. The RS427 will still operate if $V_{REF\,IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

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RS data

D to A converter

Stock numbers 309–458

The RS DAC0800 is an 8 bit high speed current output D to A converter featuring 100ns typical setting times coupled with monotonic performance over a 40 to 1 reference current range when used as a multiplying DAC. The high compliance complementary output currents allow differential output voltages of 20V peak to peak using simple resistor loads. Reference-to-full scale current matching of better than ±1 LSB can eliminate the need for full scale trim in most applications.
The digital inputs are directly TTL compatible but simple circuitry will enable the device to interface with most common logic families. The performance and characteristics are essentially stable over the full operating voltage range of ±4.5V to ±18V and power dissipation is only 33mW at ±5V.

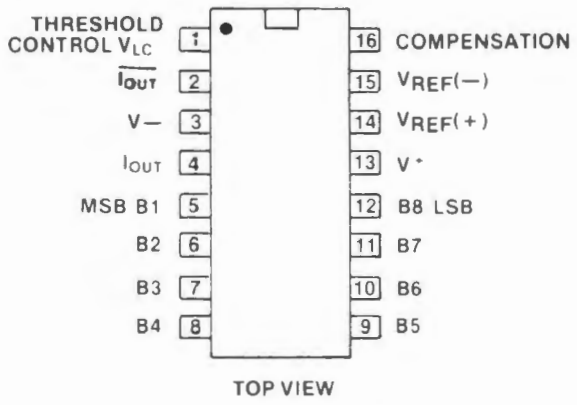
Features

- Fast settling output current 100ns
- Full scale error ±1 LSB
- Nonlinearity over temperature ±0.1%
- Full scale current drift ±10 ppm/°C
- High output compliance −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range ±4.5V to +18V
- Low power consumption 33mW at ±5V

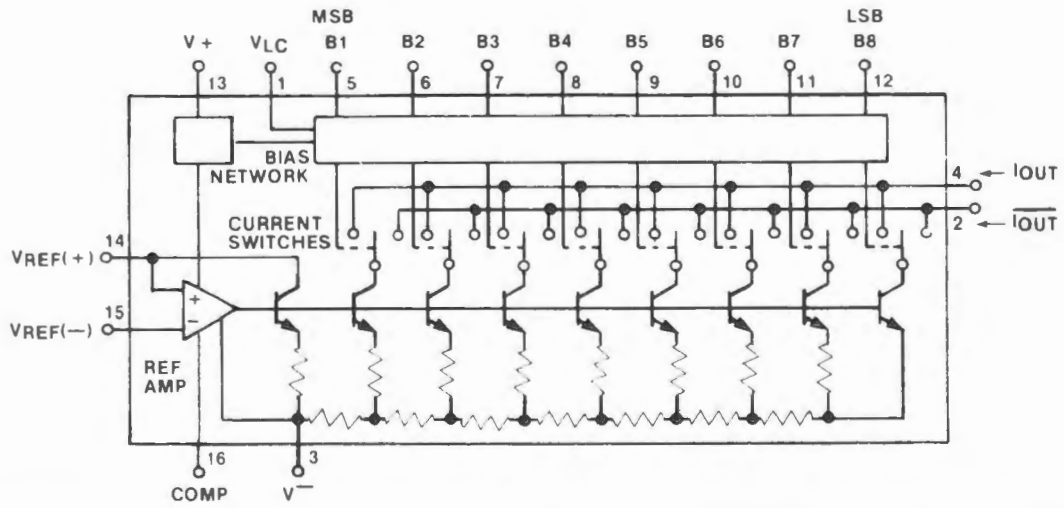
Absolute maximum ratings

Supply voltage ±18V or 36V
Power dissipation 500mW
Reference input differential voltage V^- to V^+ (V14 to V15)
Reference input common-mode range V to V^+ (V14, V15)
Reference input current 5mA
Logic inputs V^- to V^- plus 36V
Analogue current outputs Figure 9
Storage temperature −65°C to +150°C
Lead temperature (soldering, 10 seconds) 300°C
Operating temperature 0°C to +70°C

Pin connections



Block diagram



Electrical characteristics $V_S = \pm 15V$, $I_{REF} = 2mA$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$

	Parameter	Conditions	RS DAC0800 Min	RS DAC0800 Typ	RS DAC0800 Max	Units
	Resolution		8	8	8	Bits
	Monotonicity		8	8	8	Bits
	Nonlinearity				±0.19	% FS
t_S	Settling time	To ± 1/2 LSB. All bits switched		100	150	ns
		"ON" or "OFF", $T_A = 25°C$				
t_{PLH}, t_{PHL}	Propagation delay	$T_A = 25°C$				
	Each bit			35	60	ns
	All bits switched			35	60	ns
TCI_{FS}	Full scale temp. coeff.			±10	±50	ppm/°C
V_{OC}	Output voltage compliance	Full scale current change	−10		18	V
		< 1/2 LSB, R_{OUT} >20MΩ Typ				
I_{FS4}	Full scale current	$V_{REF} = 10V$, $R_{14} = 5k\Omega$	1.94	1.99	2.04	mA
		$R_{15} = 5k\Omega$, $T_A = 25°C$				
I_{FSS}	Full scale symmetry	$I_{FS4} - -I_{FS2}$		±1	±8.0	μA
I_{ZS}	Zero scale current			0.2	2.0	μA
I_{FSR}	Output current range	V = −5V	0	2.0	2.1	mA
		V = −7V to −18V	0	2.0	4.2	mA
	Logic input levels					
V_{IL}	Logic "0"	$V_{LC} = 0V$			0.8	V
V_{IH}	Logic "1"		2.0			V
	Logic input current	$V_{LC} = 0V$				
I_{IL}	Logic "0"	$-10V \leq V_{IN} \leq +0.8V$		−2.0	−10	μA
I_{IH}	Logic "1"	$2V \leq V_{IN} \leq +18V$		0.002	10	μA
V_{IS}	Logic input swing	V = −15V	−10		18	V
V_{THR}	Logic threshold range	$V_S = \pm 15V$	−10		13.5	V
I_{15}	Reference bias current			−1.0	−3.0	μA
dI/dt	Reference input slew rate			8.0		mA/μs
$PSSI_{FS+}$	Power supply sensitivity	$4.5V \leq V^+ \leq 18V$		0.0001	0.01	%/%
$PSSI_{FS-}$		$-4.5V \leq V \leq 18V$		0.0001	0.01	%/%
		$I_{REF} = 1mA$				
	Power supply current	$V_S = \pm 5V$, $I_{REF} = 1mA$				
I+				2.3	3.8	mA
I−				−4.3	−5.8	mA
		$V_S = 5V, -15V$, $I_{REF} = 2mA$				
I+				2.4	3.8	mA
I−				−6.4	−7.8	mA
		$V_S = \pm 15V$, $I_{REF} = 2mA$				
I+				2.5	3.8	mA
I−				−6.5	−7.8	mA
P_D	Power dissipation	±5V, $I_{REF} = 1mA$		33	48	mW
		5V, −15V, $I_{REF} = 2mA$		108	136	mW
		±15V, $I_{REF} = 2mA$		135	174	mW

Basic circuit

Figure 1 **±20 Vp-p output digital-to-analogue converter**

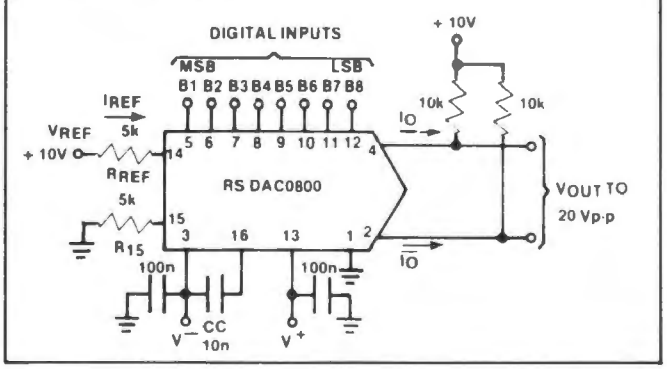


Fig 1. shows the RS DAC0800 employed as a basic positive reference, TTL compatible D/A converter.

Reference amplifier

The relationship between the output currents and related circuit variables is given below.

$I_0 + \overline{I_0} = I_{FS}$

(this equation is true for any logic input state)

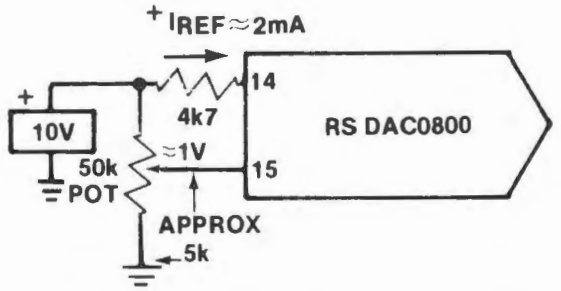
$$I_{FS} \approx + \frac{V_{REF}}{R_{REF}} \times \frac{255}{256} mA = I_{REF} \times \frac{255}{256} mA$$

Where I_0 $\overline{I_0}$ = complementary output currents
I_{FS} = full scale current in mA
V_{REF} = reference voltage in volts
R_{REF} = reference resistor in kΩ
I_{REF} = reference current in mA
$R_{15} = R_{REF}$ R_{15} provides bias current cancellation and may be eliminated if a small loss of accuracy and temperature drift can be tolerated.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R_{REF} should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 100nF to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

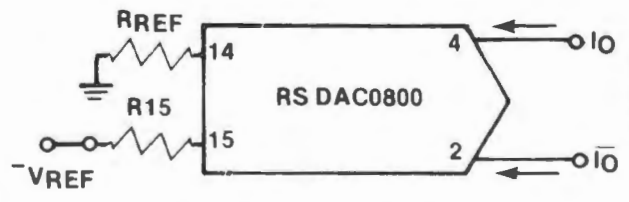
In most applications, the reference to full scale current matching (±1 LSB) will be sufficiently accurate. For systems requiring closer matching the circuit shown in Fig. 2 can be employed.

Figure 2 **Full scale adjustment circuit**



The RS DAC0800 can be used with a negative reference as shown in Fig. 3. The reference amplifier input current, I_{REF}, must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

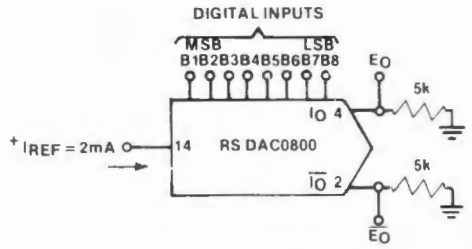
Figure 3 **Basic negative reference operation**



$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$ Note. R_{REF} sets I_{FS}; R_{15} is for bias current cancellation

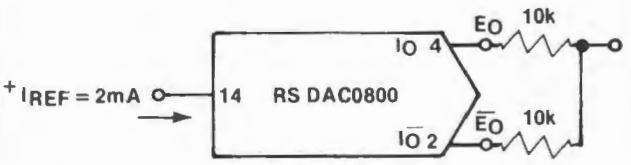
The circuits and associated tables shown in Figs. 4–6 illustrate unipolar, bipolar and symmetrical offset binary operation respectively. The digital inputs and decoupling components have been removed for clarity.

Figure 4 **Basic unipolar negative operation**



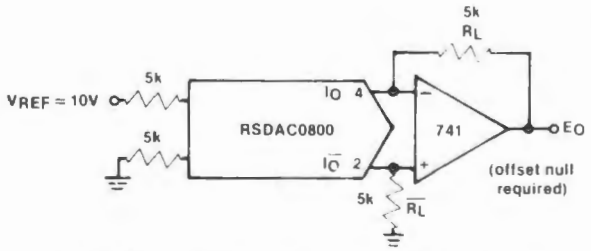
	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$\overline{I_O}$mA	E_O	E_O
Full scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full scale −LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half scale +LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half scale −LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero scale +LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero scale	0	0	0	0	0	0	0	0	0.000	1.992	−0.000	−9.960

Figure 5 **Basic bipolar output operation**



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos. full scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. full scale −LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero scale +LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero scale −LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. full scale +LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. full scale	0	0	0	0	0	0	0	0	+10.000	−9.920

Figure 6 **Symmetrical offset binary operation**



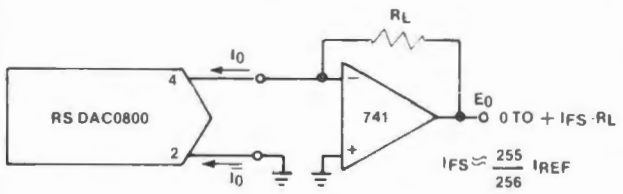
If $R_L = R_L$ within ·0.05%, output is symmetrical about ground

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. full scale	1	1	1	1	1	1	1	1	+9.920
Pos. full scale −LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero scale	0	1	1	1	1	1	1	1	−0.040
Neg. full scale +LSB	0	0	0	0	0	0	0	1	−9.840
Neg. full scale	0	0	0	0	0	0	0	0	−9.920

RS data

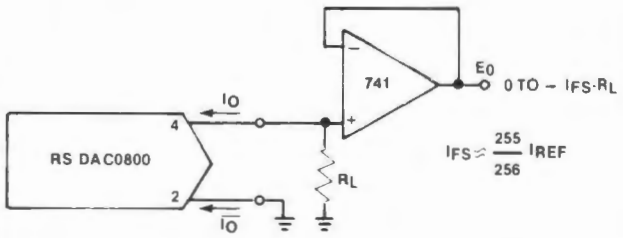
The addition of an operational amplifier to the output of the RS DAC0800 is a simple and effective means of providing a low impedance analogue output. Apart from providing a buffer stage for the analogue output, the output voltage swing can also be adjusted via R_L to suit individual requirements.
An offset null circuit should be employed for the OP-AMP and it should be adjusted to provide zero output for all bits at '0' input.
Figs. 7 & 8 show alternative connections for producing positive or negative outputs.

Figure 7 **Positive low impedance output operation**



For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_0}$ (pin 2), connect I_0 (pin 4) to ground.

Figure 8 **Negative low impedance output operation**

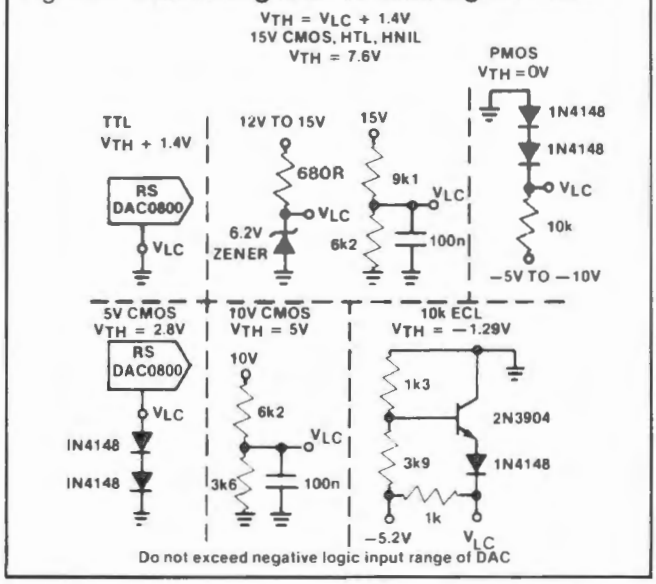


For complementary output (operation as a negative logic DAC) connect non-inverting input of op amp to $\overline{I_0}$ (pin 2); connect I_0 (pin 4) to ground.

Logic interfaces

The logic threshold voltage V_{TH} is typically 1.4V and by superimposing a voltage on pin 1 (V_{LC}) variation in V_{TH} is possible to suit the logic employed.
Fig. 9 illustrates the simple circuits required.

Figure 9 **Interfacing with various logic families**



Do not exceed negative logic input range of DAC

Figure 10
Output current vs output voltage (output voltage compliance)

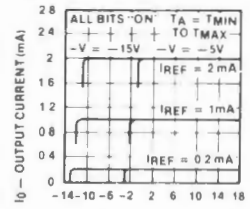


Figure 11
Output voltage compliance vs temperature

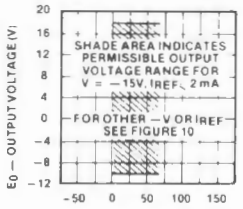


Figure 12
Power supply current vs V⁺

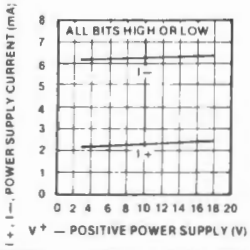


Figure 13
Power supply current vs V⁻

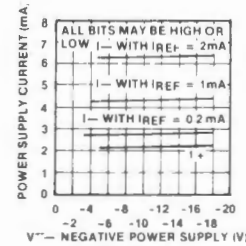
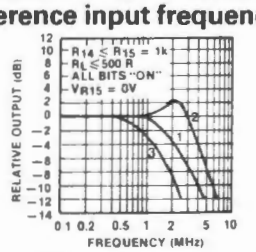


Figure 14 **Reference input frequency response**



Curve 1: CC = 15 pF, VIN = 2 Vp-p centered at 1V.
Curve 2: CC = 15 pF, VIN = 50 mVp-p centered at 200 mV.
Curve 3. CC = 0 pF, VIN = 100 mVp-p centered at 0V and applied through 50 Ω connected to pin 14. 2V applied to RREF

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RS data

Keyboard encoder i.c. 309-509

The RS2376 Keyboard Encoder I.C. is a fully integrated P-MOS keyswitch encoding circuit, suitable for encoding a keyboard with up to 88 switches, plus shift and control, into a useable 9 bit data code, i.e. the standard 8 bit ASC II data code + one parity bit.

The RS2376 offers the facilities of two key roll-over operation with N-key lockout and has user-selectable odd or even parity and output polarity. A self contained oscillator and debounce circuit are incorporated in the device, requiring only the addition of a resistor and capacitor for each function. The outputs are directly TTL/MOS logic compatible.

The RS 76 key Keyboard (336-703) is designed to accept the RS2376 Keyboard Encoder I.C., enabling a full ASCII code keyboard to be easily constructed.

Features

- One integrated circuit required for complete keyboard assembly.
- Outputs directly compatible with TTL or MOS logic arrays.
- External control provided for output polarity selection.
- External control provided for selection of odd or even parity.
- Two key roll-over operation.
- N-key lockout.
- Self-contained oscillator circuit.
- Externally controlled delay network provided to eliminate the effect of contact bounce.
- Static charge protection on all input and output terminals.

Figure 1 **Pin connections**

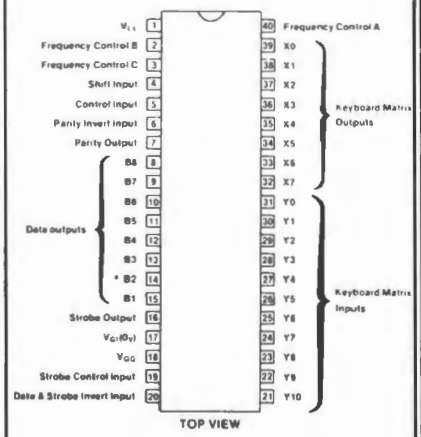
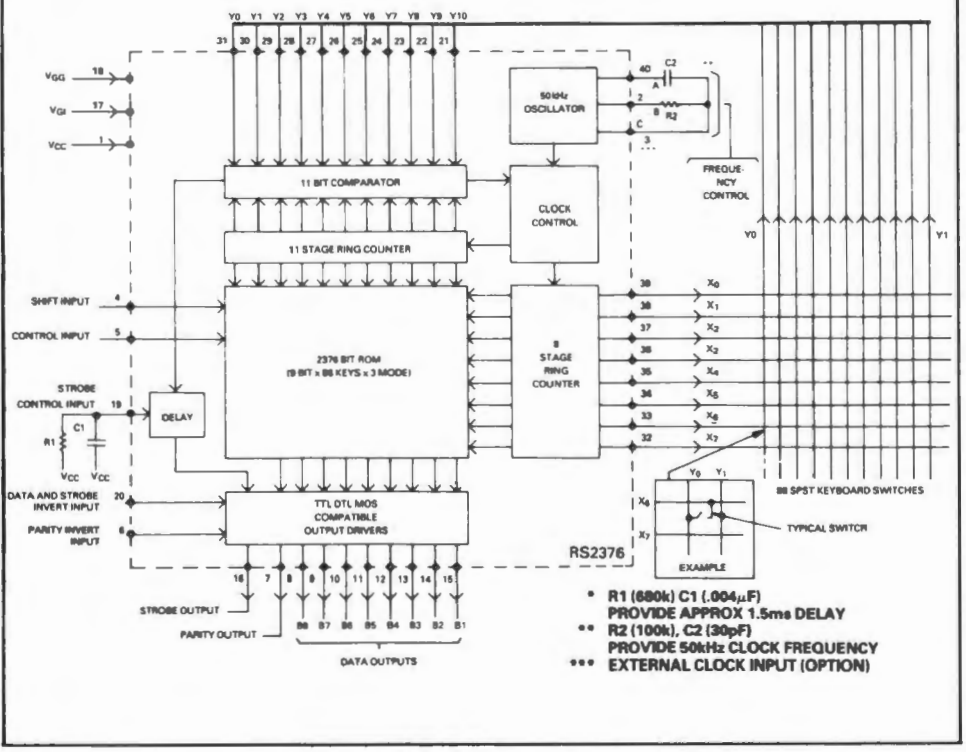


Figure 2 **Block diagram**



4080
Electrical characteristics

Maximum ratings

V_{GI} and V_{GG} (with respect to V_{CC}) ——— −20V to +0.3 V
Logic input voltages (with respect to V_{CC}) ——— −20 V to 0.3 V
Storage Temperature ——— −65°C to +150°C
Operating Temperature Range ——— 0°C to +70°C

Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC}=5 Volts ± 0.5 Volts, (V_{cc}=Substrate Voltage)
V_{GG}=−12 Volts ± 1.0 Volts, V_{GI}=OV
Operating Temperature (TA)=0°C to +70°C

Characteristics	Conditions	Symbol	Min	Typ*	Max	Units
Clock Frequency	See Block diagram (Figure 2) footnote for typical R — C values	f	10	50	100	kHz
Data Input (Shift, Control, Parity invert, data & strobe invert).						
Logic "0" Level		V_{10}	V_{GG}	—	+0.8	V
Logic "1" Level		V_{11}	V_{CC}−1.5	—	V_{CC}+0.3	V
Shift & Control Input Current	V_I = +5V	$I_{INS.C}$	15	36	60	μA
	V_I = 0V		8	16	30	μA
Data, Parity Invert Input Current	V_I = −5V to +5V	$I_{IND.P}$	—	.01	1	μA
X Output (X_0-X_7) Logic "1" Output Current	V_{OUT} = V_{CC}	I_{XI}	—	0	—	μA
	V_{OUT} = V_{CC}−1.3V		80	150	400	μA
	V_{OUT} = V_{CC}−2.0V		140	300	800	μA
	V_{OUT} = V_{CC}−5V		250	700	1500	μA
	V_{OUT} = V_{CC}−10V		500	1500	3000	μA
Logic "0" Output Current	V_{OUT} = V_{CC}	I_{XO}	15	30	80	μA
	V_{OUT} = V_{CC}−1.3V		13	27	65	μA
	V_{OUT} = V_{CC}−2.0V		12	25	60	μA
	V_{OUT} = V_{CC}−5V		5	10	40	μA
	V_{OUT} = V_{CC}−10V		—	1	20	μA
Y Input (Y_0-Y_{10}) Trip Level	Y Input Going Positive	V_Y	V_{CC}−5	V_{CC}−3	V_{CC}−2	V
Hysteresis	Note 1	ΔV_Y	0.5	0.9	1.4	V
	Note 2					
Selected Y Input Current	V_{IN} = V_{CC}	I_{YS}	30	60	160	μA
	V_{IN} = V_{CC}−1.3V		26	54	130	μA
	V_{IN} = V_{CC}−2.0V		24	50	120	μA
	V_{IN} = V_{CC}−5V		10	20	80	μA
	V_{IN} = V_{CC}−10V		—	2	20	μA
Unselected Y Input Current	V_{IN} = V_{CC}	I_{YU}	15	30	80	μA
	V_{IN} = V_{CC}−1.3V		13	27	65	μA
	V_{IN} = V_{CC}−2.0V		12	25	60	μA
	V_{IN} = V_{CC}−10		5	10	40	μA
Input Capacitance	at 0V	C_{IN}	—	3	10	pF
Switch Characteristics Minimum Switch Closure	See Timing Diagram (Figure 3)	—	—	—	—	—
Contact Closure Resistance		Z_{CC}	—	—	300	Ω
		Z_{CO}	10^7	—	—	Ω
Strobe Delay Trip Level (Pin 19)		V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V
Hysteresis	See Note 1	V_{SD}	0.5	0.9	1.4	V
Quiescent Voltage (Pin 19)	With 680kΩ to V_{CC}		−3	−5	−8	V
Data Output (B_1-B_9) Logic "O"	I_{OL} = 1.6mA	—	—	—	0.4	V
Logic "1"	I_{OH} =-100μA	—	V_{CC}−1	—	—	V
Power I_{CC}	V_{CC} = +5V	—	—	5	10	mA
I_{GG}	V_{GG} = −12V	—	—	5	10	mA

*Typical values at +25°C and nominal voltages.

NOTE 1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Guaranteed number of X & Y loads which may be applied to an X output=eleven.

Operation

The RS2376 contains a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/MOS compatible output drivers.

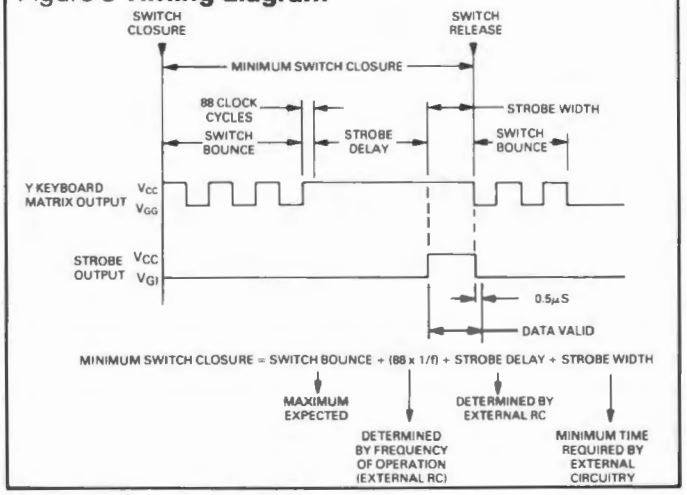
The ROM portion of the chip is a 264 by 9 bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0-X7) and one input of the 11-bit cmparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1-D8 (pins 8-15) and the Strobe Output (pin 16).

Figure 3 **Timing diagram**



Typical characteristic curves

Figure 4 **Strobe delay VS. C1**

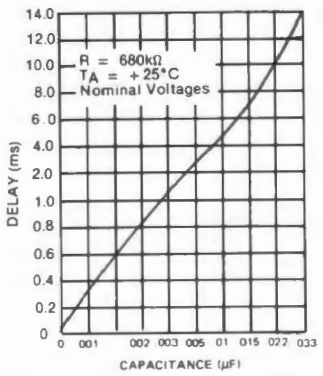


Figure 5 **Oscillator frequency VS. C2**

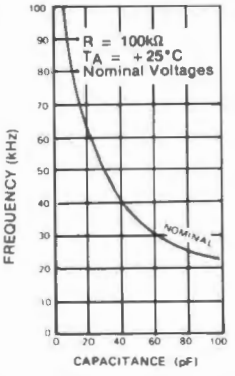


Figure 6 **Typical output on resistance (R_{DON}) VS. Gate bias voltage (V_{GS})**

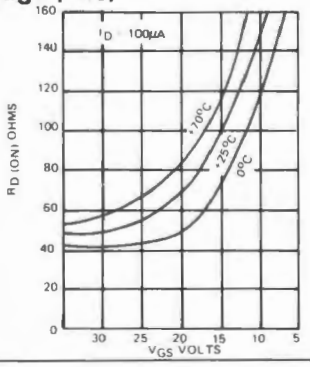


Figure 7 **Typical power consumption (mW) VS. Temp (°C)**

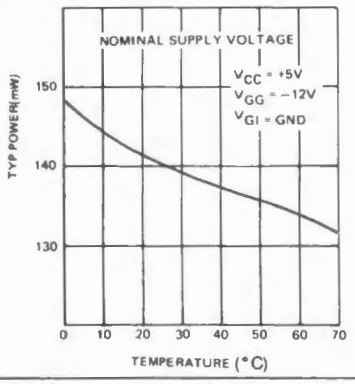
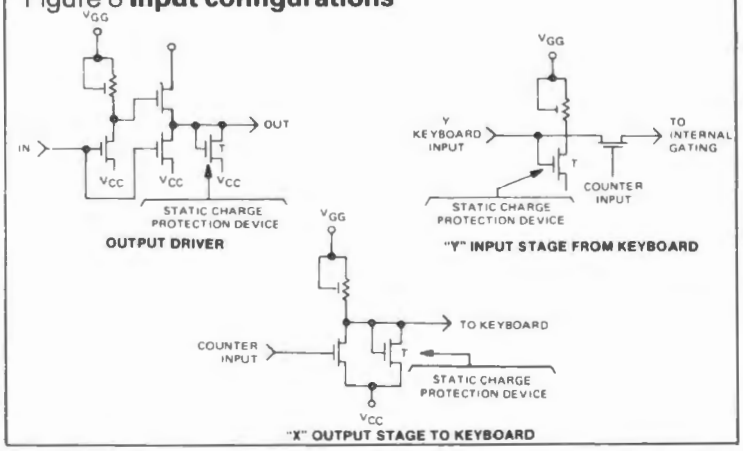


Figure 8 **Input configurations**



Power supply connections

Figure 9 **TTL operation**

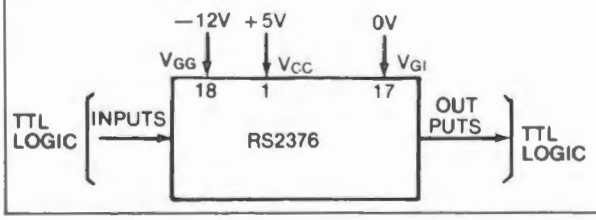
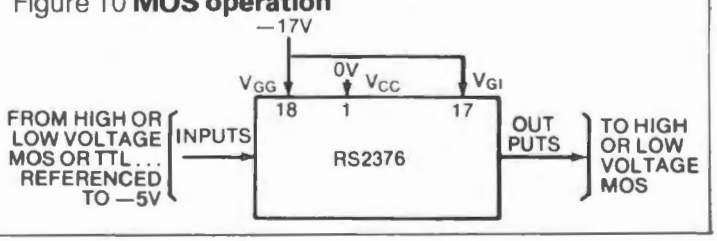


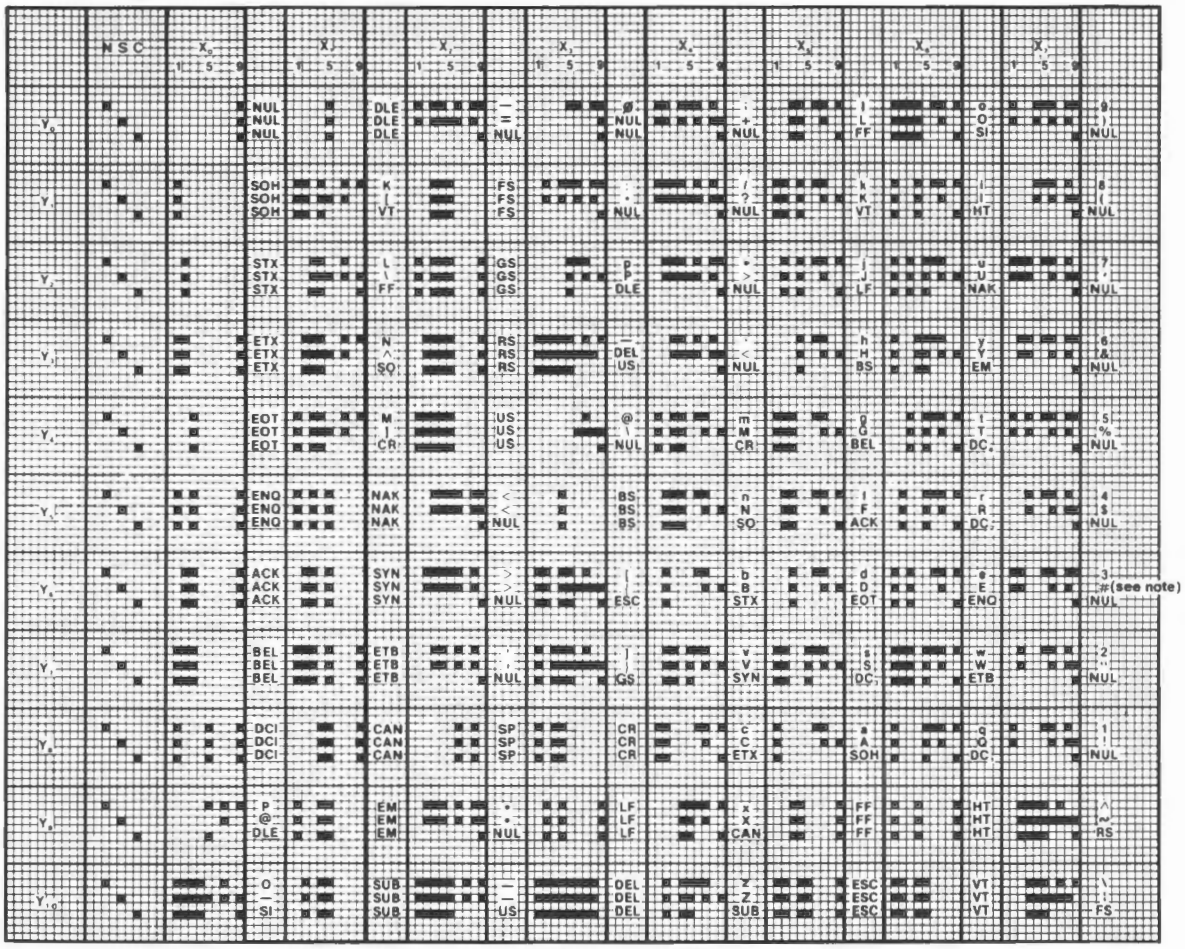
Figure 10 **MOS operation**



RS data

Code assignment chart

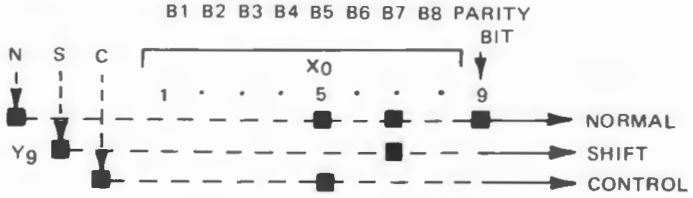
■ represents a Logic "1"



Code Assignment shown with Data and Strobe Invert Input (Pin 20) and the Parity Invert Input (Pin 6) tied to Logic "O". This code is an 8 bit ASCII code (B1-B8). Output B9 is included as an odd parity bit operating on outputs B1-B7.

Note: the # is replaced with the £ sign for many applications.

Example



(CODE REPRESENTATIVE OF KEY DEPRESSION AT LOCATION X_0 — Y_9 AND PROPER MODE SELECTION)

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
■ = OUTPUT LOGIC "1". (SEE DATA B1 – B8)
LOGIC "1" = +5V
LOGIC "0" = 0V

Truth tables

DATA (B1-B8) INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	INTERNAL STROBE	STROBE OUTPUT (PIN 16)
1	1	0
0	0	0
1	0	1
0	1	1

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (PIN 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (PIN 7)
1	1	0
0	1	1
1	0	1
0	0	0

MODE SELECTION

$\overline{S}$ $\overline{C}$ = N
$\overline{S}$ C = S
S $\overline{C}$ = C
S C = C

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RS data

Contactors and accessories (60A and 100A AC1)

A range of contactors and accessories including an interlock kit, main adder poles and auxiliary switches. The contactor design is space saving with right angle action (gravity drop out).
Contacts are of silver cadmium oxide double break type with individual low bounce helical contact springs. The 100A contactor has box clamp terminals for cable sizes up to 50mm^2 whereas the 60A contactor has single screw saddle clamps for cable sizes up to 16mm^2. Terminal marking conforms to CENELEC 50 005.

Features

- Comply with BS5424, IEC158, VDE0660
- 3 main poles with facility to convert to 4 or 5 pole by using main adder poles
- Even when extended to 5 main poles, an additional 1N/O + 1N/C auxiliary switch may be added to either or both sides
- In addition to the add-on facilities, the contactors have, as standard, a start/hold on switch and a 1 N/C auxiliary switch.
- Dual voltage coils

Contactor design

Figure 1 **Basic assembly**

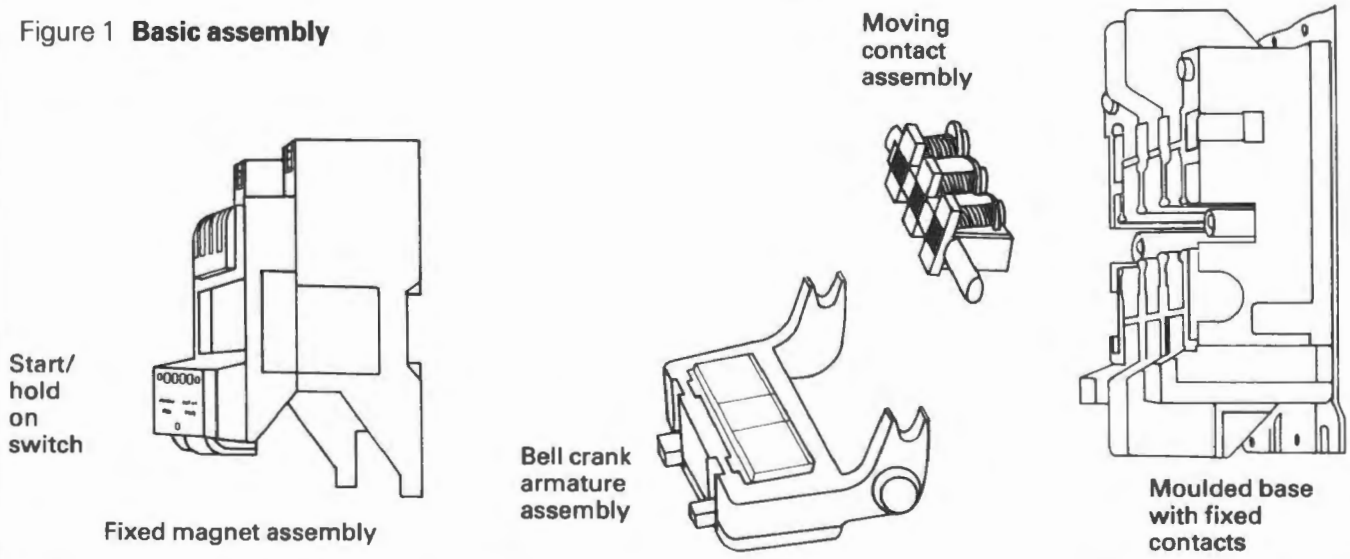
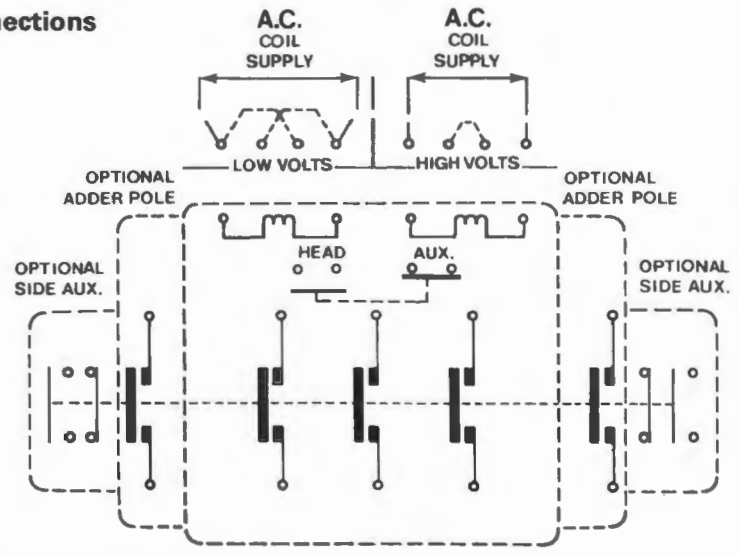


Figure 2 **Electrical connections**



Coil voltages and specifications

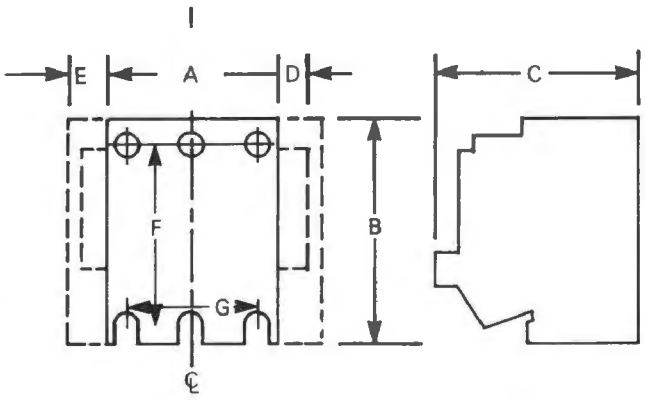
Contactor I(AC1) & Ith	RS stock number	Low volts a.c.	High Volts a.c.	Frequency Hz	Pull-in power VA	Hold-in power VA
60A	348-352	110-120	220-240	50	200	28
60A	348-346	190-210	380-420	50	200	28
100A	346-407	110-120	220-240	50	200	28

Ratings – up to 600 operations per hour

I (AC1) & Ith	3 phase motor utilisation categories	I_e (A)	HP 220/240V	HP 415V	HP 600V	kW 220V	kW 380V	kW 600V	Mechanical life at class 4 rate (600 ops/hr)	Electrical life at full load current (AC3)
60A	AC2	60	22	45	60	15	30	37	5×10^6 ops	3×10^5 ops
	AC3	50	17	35	45	15	25	30		
	AC4	35	13	25	30	10	18.5	22		
	star/delta	87	35	65	75	22	45	55		
100A	AC2	90	25	50	70	18.5	37	55	5×10^6 ops	3×10^5 ops
	AC3	72	25	50	70	18.5	37	55		
	AC4	55	15	35	40	11.0	22	35		
	star/delta	125	20	100	130	37.0	75	120		

I (AC1) & Ith	Lighting load	DC1 220V with 2 poles in series in positive line	Transformer loads Limited to 20.I inrush	Capacitors	Fault protection : max fuse size class Q1 HRC
60A	30A	60A	15A	30A	80A
100A	60A	100A	30A	50A	125A

Figure 3 **Contactor dimensions**



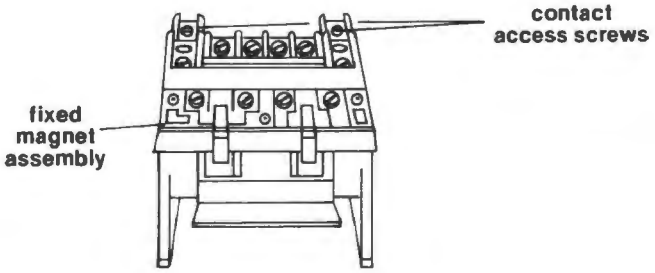
Contactor	Overall dimensions mm					Fixing holes mm	
Ith AMP	A	B	C	D	E	F	G
60	83	132	105	15	20	114.3	63.5
100	83	174	105	15	20	114.3	63.5

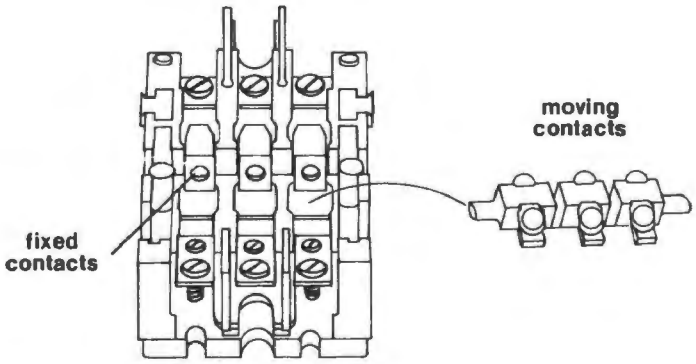
Dimension B is an overall dimension which includes the phase barriers.

Dimensions D and E relate to auxiliary switches and main adder poles respectively.

Figure 4 **Main contact inspection**

To inspect the fixed and moving contacts loosen the two captive contact access screws and remove the fixed magnet assembly.





Auxiliary switch

Auxiliary switches (348-330) may be fitted to either side of the contactors. Terminals are marked to conform to CENELEC 50-005. To fit auxiliary switch release the two captive coil access screws and remove the head auxiliary switch assembly (see fig. 5). Slide auxiliary switch into dovetail recess (see fig. 6) and re-fit head auxiliary switch assembly.

Figure 5

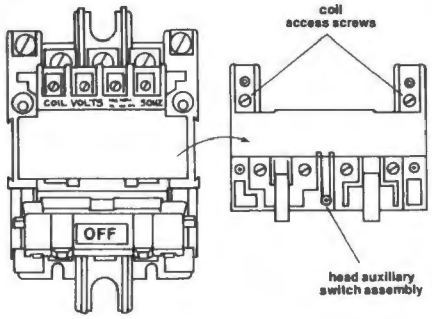
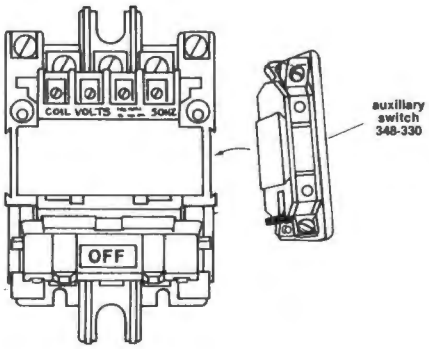


Figure 6



Auxiliary switch specification

	24V ac	110V ac	250V ac	440V ac	24V dc
AC3	5A	4A	4A	3A	5A
AC11	4A	3.2A	3.2A	2.4A	4A

Main adder poles

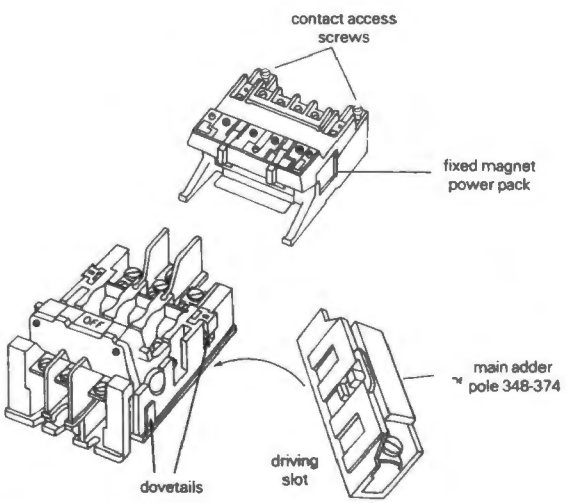
Main adder poles can be fitted to either or both sides.

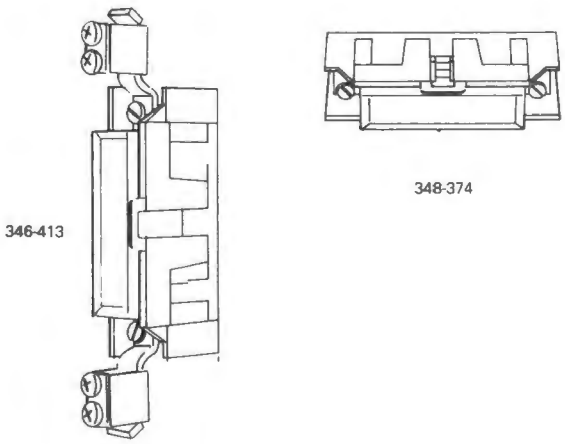
The 100A version (346-413) and the 60A version (348-374) differ only in size of contacts and cable terminals; both types have similar cable terminals to their equivalent contactors.

Contactors and main adder poles are interchangeable eg. A 60A main adder pole will fit a 100A contactor.

To fit a main adder pole, release the two captive contact access screws (see fig. 7) and remove the fixed magnet assembly, bell crank armature assembly and moving contact bar (see fig. 1). Slide the main adder pole into the two dovetail recesses, together with the moving contact bar assembly, ensuring that the end of the contact carrier engages with the driving slot in the adder pole. Re-assemble the remaining components.

Figure 7





RS data

Interlock kit

Stock number 348-368

To assemble an interlocked pair of contactors first remove the metal plate and square insulating plate from the base of the contactors (see fig. 8). Locate the contactors over the square pegs of the interlock kit (see fig. 9) and secure with the screws supplied. Finally check for correct operation.

Figure 8 **Base view of contactor with metal plate removed**

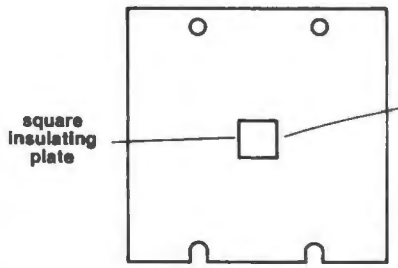


Figure 9 **Interlock kit**

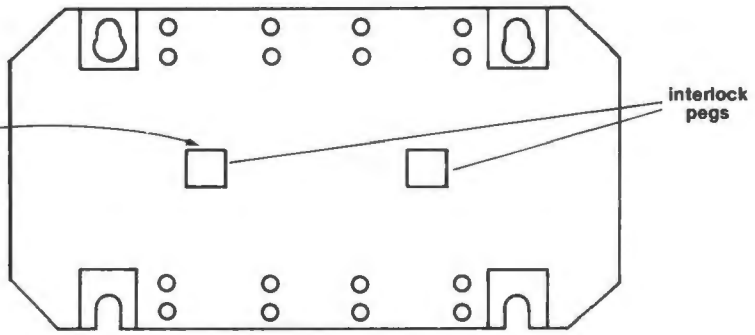
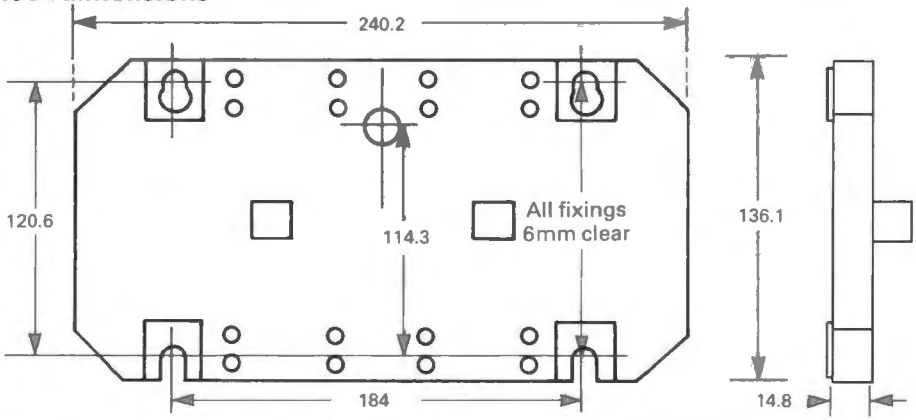


Figure 10 **Interlock dimensions**



Enclosures

Suitable enclosures with protection up to IP67 are available for mounting the RS 60A and 100A contactors; see below. Refer to figs. 3 and 10 for fixing and dimensional details of contactor and interlock kit.

Clear (IP66)	Opaque, grey (IP67)	Size H	W	D	contactors accommodated
508-330	508-009	300	185	175	Single contactor plus accessories
508-324	507-999	300	300	175	Interlocked pair of contactors plus accessories

Further details of the above enclosures can be found in the current RS catalogue.

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RS data

Alpha-numeric keyboard

Stock number 336-703

The RS76 key alpha-numeric keyboard consists of a main 60 key-QWERTY-plus array with a 16 key numeric and cursor control side pad. The keyboard layout is designed to conform to the requirements of ECMA 23 and BS4822 and is supplied in sloped form with two shot moulded charcoal grey keycaps with white lettering. The switches used in the keyboard are a mechanical type, of the same design as RS P.C.B. mounting keyboard switches. They are mounted on a double sided, through-hole plated glass fibre P.C.B., complete with aluminium support and mounting frame. This keyboard may be fitted into RS keyboard case (507-416) which has a suitable cut-out.

The keyboard circuit layout is designed to allow access to the switch matrix, via two 16 pin DIL sockets, for direct memory mapping into a computer or microprocessor system. Alternatively by the addition of the 88 key encoder i.c. (309-509) and four other LSTTL i.c.'s a very powerful encoded keyboard may be built, offering the following extra features: alternate action caps lock, side pad shift inhibit, repeat function, encoded cursor controls in the side pad and user selectable odd or even parity and output polarity.

The complete encoded keyboard generates the full ASCII character set in 8 bit data code (+ 1 parity bit operating on the first seven bits) making it ideal for use in modern small system designs.

The keyboard P.C.B. is supplied complete with DIL sockets fitted for all i.c.'s plus two 16 pin DIL sockets for the matrix outputs, and a 16 pin DIL socket for the coded outputs and the power supply inputs. Inter connection may be made using either 16 pin 'Speedbloc' DIL connectors or 16 pin DIL modules and ribbon cable.

Life	20×10^6 ops/switch
Operating temp. range	0°C to 65°C
Supply (encoded)	+5V, −12V
Encoded outputs	TTL, MOS compatible

Figure 1 **Keyboard layout**

Figure 2 **Keyboard dimensions**

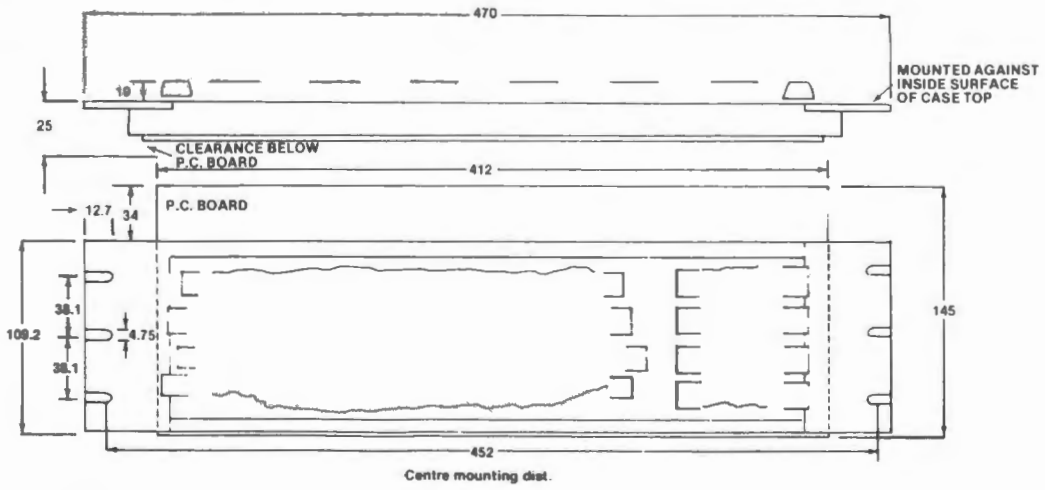


Figure 3 **Suggested panel cut out in mm (inches)**

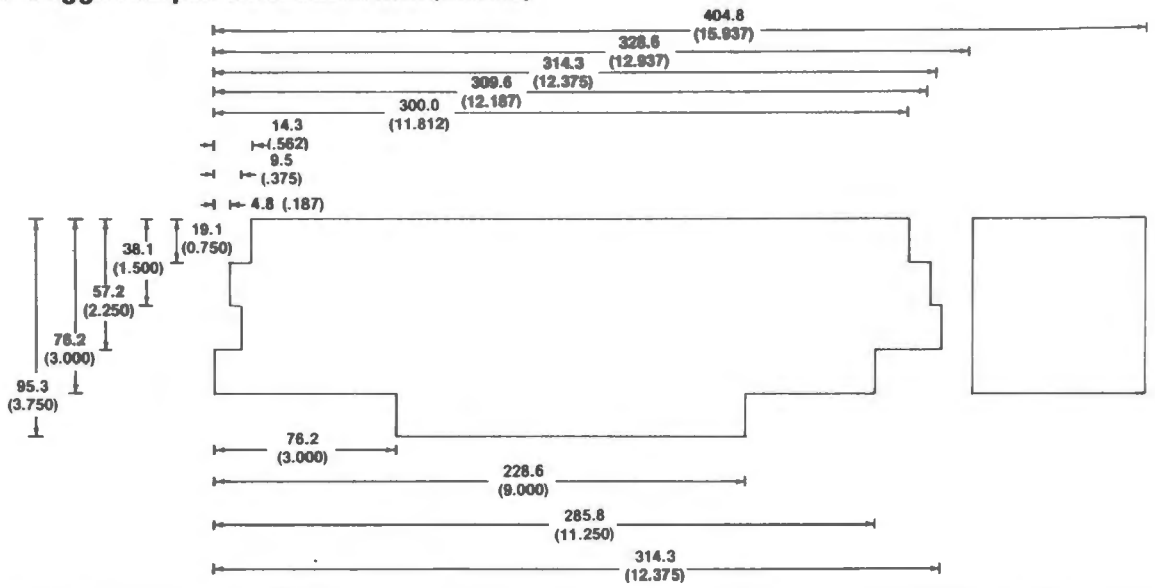
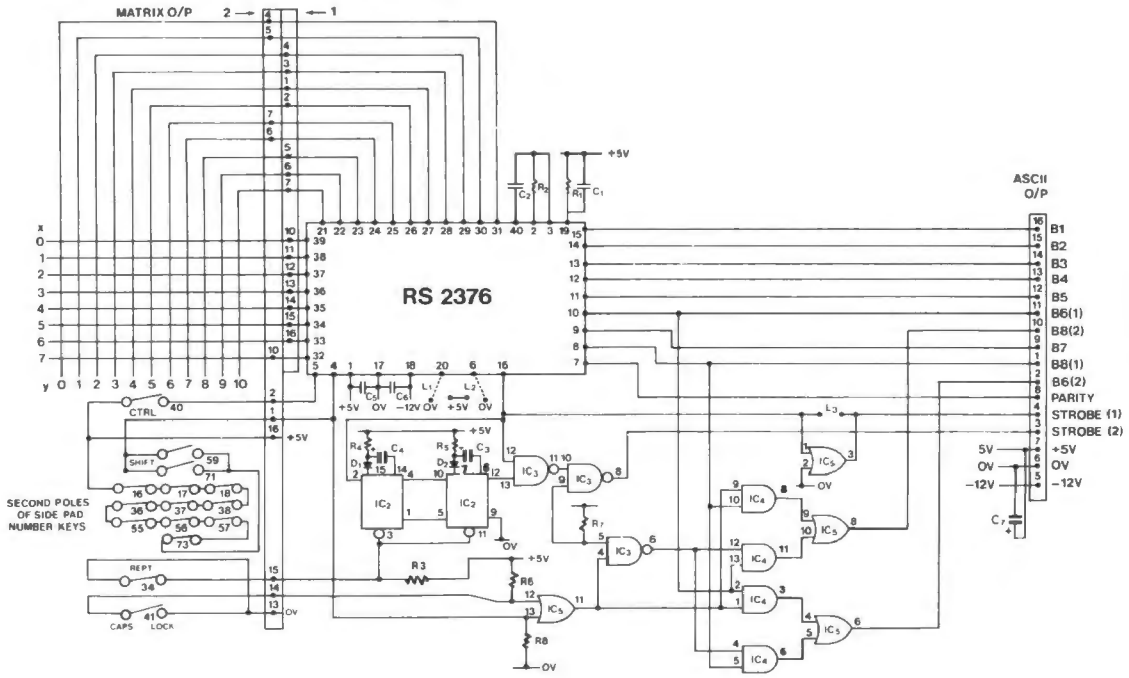


Figure 4 **Circuit diagram of complete encoded keyboard**



Components

R_1 680k	C_1 4n7 } oscillator + debounce components		
R_2 100k	C_2 33p }		
R_3 4k7	C_3* 4μ7 tantalum	IC_1	RS2376
R_4* 18k (33k)	C_4* 4μ 7 tantalum	IC_2	74LS123
R_5* 12k (22k)	C_5 100n disc	IC_3	74LS00
R_6 4k7	C_6 100n disc	IC_4	74LS08
R_7 1k5	C_7 47μ 10V electrolytic	IC_5	74LS32
R_8 1k	Links at D_1 and D_2		

Note: A 74123 may be used in place of a 74LS123 but links at D_1 and D_2 should be replaced by 1N4148 diodes and timing resistors R_4 and R_5 with 33k and 22k value resistors respectively.

The keyboard is supplied fitted with these components.

Links - to be made as required

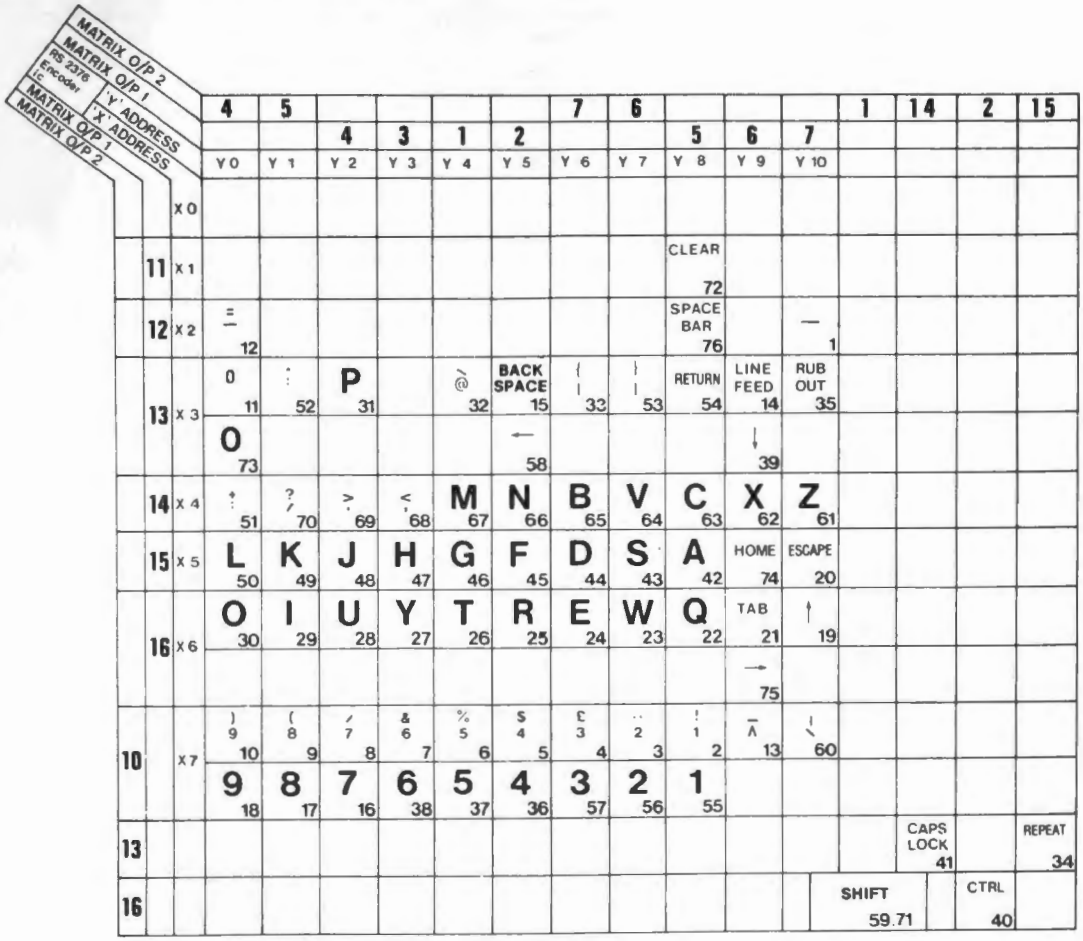
L_1 Output strobe polarity — L_1 to +5V inverted outputs; L_1 to 0V non-inverted outputs

L_2 Parity odd or even — L_2 to +5V even parity; L_2 to 0V odd parity

L_3 only used if output buffering not required.

* To give repetition rate of approx. 15Hz

Figure 5 **Matrix outputs and X-Y addresses**



Output coding of complete encoded keyboard

Key number	Character	9 Bit output code LSB MSB	Hex code from first 7 bits
1	—	N 111110101	5F
		S 111110101	5F
		C 111110000	1F
2	! 1	N 100011010	31
		S 100001011	21
		C 000000001	00
3	" 2	N 010011010	32
		S 010001011	22
		C 000000001	00
4	£ 3	N 110011011	33
		S 110001010	23
		C 000000001	00
5	$ 4	N 001011010	34
		S 001001011	24
		C 000000001	00
6	% 5	N 101011011	35
		S 101001010	25
		C 000000001	00
7	& 6	N 011011011	36
		S 011001010	26
		C 000000001	00
8	/ 7	N 111011010	37
		S 111001011	27
		C 000000001	00
9	(8	N 000111010	38
		S 000101011	28
		C 000000001	00
10	) 9	N 100111011	39
		S 100101010	29
		C 000000001	00
11		N 000011011	30
		S 000000001	00
		C 000000001	00
12	= —	N 101101011	2D
		S 101111010	3D
		C 000000001	00
13	–	N 011110100	5E
		S 011111111	7E
		C 011110001	1E
14	LINE FEED	N 010100001	0A
		S 010100001	0A
		C 010100001	0A
15	BACK SPACE	N 000100000	08
		S 000100000	08
		C 000100000	08
16	7	N 111011010	37
		S 111011010	37
		C 000000001	00
17	8	N 000111010	38
		S 000111010	38
		C 000000001	00
18	9	N 100111011	39
		S 100111011	39
		C 000000001	00
19	↑	N 110100000	0B
		S 110100000	0B
		C 110100000	0B
20	ESC	N 110110001	1B
		S 110110001	1B
		C 110110001	1B
21	TAB	N 100100001	09
		S 100100001	09
		C 100100001	09
22	Q	N 100011101	71
		S 100010100	51
		C 100010001	11
23	W	N 111011101	77
		S 111010100	57
		C 111010001	17
24	E	N 101001101	65
		S 101000100	45
		C 101000001	05
25	R	N 010011101	72
		S 010010100	52
		C 010010001	12
26	T	N 001011101	74
		S 001010100	54
		C 001010001	14
27	Y	N 100111100	79
		S 100110101	59
		C 100110000	19
28	U	N 101011100	75
		S 101010101	55
		C 101010000	15
29	I	N 100101101	69
		S 100100100	49
		C 100100001	09
30	O	N 111101101	6F
		S 111100100	4F
		C 111100001	0F

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE

RS data

Output coding of complete encoded keyboard (continued)

Key number	Character	9 Bit output code LSB MSB	Hex code from first 7 bits
31	P	N 000011100	70
		S 000010101	50
		C 000010000	10
32		N 000000100	40
		S 000001111	60
		C 000000001	00
33	{ [	N 110110100	5B
		S 110111111	7B
		C 110110001	1B
34	REPEAT	NO CODE	
35	RUB OUT	N 111111110	7F
		S 111111110	7F
		C 111111110	7F
36	4	N 001011010	34
		S 001011010	34
		C 000000001	00
37	5	N 101011011	35
		S 101011011	35
		C 000000001	00
38	6	N 011011011	36
		S 011011011	36
		C 000000001	00
39	↓ 2	N 010100001	0A
		S 010100001	0A
		C 010100001	0A
40	CONTROL	NO CODE	
41	CAPS LOCK	NO CODE	
42	A	N 100001100	61
		S 100000101	41
		C 100000000	01
43	S	N 110011100	73
		S 110010101	53
		C 110010000	13
44	D	N 001001100	64
		S 001000101	44
		C 001000000	04
45	F	N 011001101	66
		S 011000100	46
		C 011000001	06
46	G	N 111001100	67
		S 111000101	47
		C 111000000	07
47	H	N 000101100	68
		S 000100101	48
		C 000100000	08
48	J	N 010101101	6A
		S 010100100	4A
		C 010100001	0A
49	K	N 110101100	6B
		S 110100101	4B
		C 110100000	0B
50	L	N 001101101	6C
		S 001100100	4C
		C 001100001	0C
51	+ ;	N 110111010	3B
		S 110101011	2B
		C 000000001	00
52	* :	N 010111011	3A
		S 010101010	2A
		C 000000001	00
53	}]	N 101110100	5D
		S 101111111	7D
		C 101110001	1D
54	RETURN	N 101100000	0D
		S 101100000	0D
		C 101100000	0D
55	1	N 100011010	31
		S 100011010	31
		C 000000001	00
56	2	N 010011010	32
		S 010011010	32
		C 000000001	00
57	3	N 110011011	33
		S 110011011	33
		C 000000001	00
58	← 3	N 000100000	08
		S 000100000	08
		C 000100000	08
59	SHIFT	NO CODE	
60	↑	N 001110101	5C
		S 001111110	7C
		C 001110000	1C
61	Z	N 010111100	7A
		S 010110101	5A
		C 010110000	1A
62	X	N 000111101	78
		S 000110100	58
		C 000110001	18
63	C	N 110001101	63
		S 110000100	43
		C 110000001	03
64	V	N 011011100	76
		S 011010101	56
		C 011010000	16
65	B	N 010001100	62
		S 010000101	42
		C 010000000	02
66	N	N 011101100	6E
		S 011100101	4E
		C 011100000	0E
67	M	N 101101100	6D
		S 101100101	4D
		C 101100000	0D
68	<	N 001101010	2C
		S 001111011	3C
		C 000000001	00
69	>	N 011101011	2E
		S 011111010	3E
		C 000000001	00
70	? /	N 111101010	2F
		S 111111011	3F
		C 000000001	00
71	SHIFT	NO CODE	
72	CLEAR 4	N 000110001	18
		S 000110001	18
		C 000110001	18
73	O	N 000011011	30
		S 000011011	30
		C 000000001	00
74	HOME 5	N 001100001	0C
		S 001100001	0C
		C 001100001	0C
75	→ 6	N 100100001	09
		S 100100001	09
		C 100100001	09
76	SPACE BAR	N 000001010	20
		S 000001010	20
		C 000001010	20

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE

All codes shown above with Links L_1 & L_2, connected to 0V.
Cursor control standard ASCII characters.

1. ↑ VT — Vertical tab
2. ↓ LF — Line feed
3. ← BS — Back space
4. CLEAR CAN — Cancel
5. HOME FF — Form feed
6. → HT — Horizontal tab

For further details regarding the RS 2376 encoder i.c. see Data sheet 4080.

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RS data

Synchronous motor and gearboxes

Synchronous motor 332-802

A synchronous motor having two separately wound phases red to grey and blue to grey, which depending on the way they are connected (see Figure 1), will allow the motor to be operated from either 240 Vac or 110 Vac. The phases are wound symmetrically around 12 pairs of poles in the motor such that given a constant supply frequency 50 Hz or 60 Hz, a rotating magnetic field will be developed which will drive the central permanent magnet rotor (mounted on the output spindle) at a speed which is directly proportional to the frequency.

The motor is supplied with two capacitors of specific value and voltage rating which when connected as shown in Figure 1 will determine the direction and phasing of the current through the windings such that the resultant rotating magnetic field will change direction at the flick of a switch S. If only one direction is required then the appropriate capacitor should be permanently connected.
Figure 2 gives the motor dimensional details.

Features

- Accurate output shaft speeds
- High torque with small physical size
- Smooth running
- Dual voltage input
- Forward and reverse output drive
- Quiet operation

Note: It is important that these capacitor values are adhered to as they are chosen for correct current phasing. Deviations of greater than ±10% of these values may result in motor instability.

Figure 1 **Rate contacts of a switch S at 250 Vac minimum**

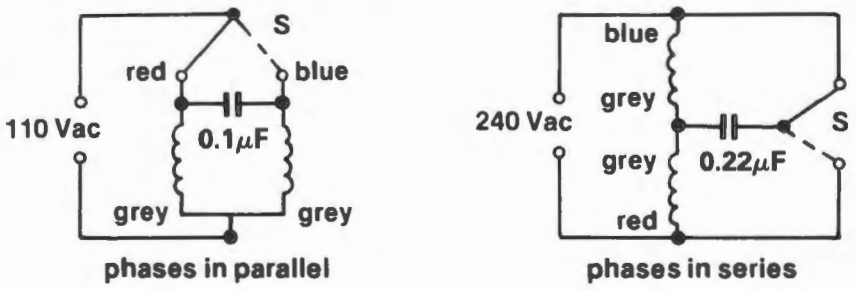
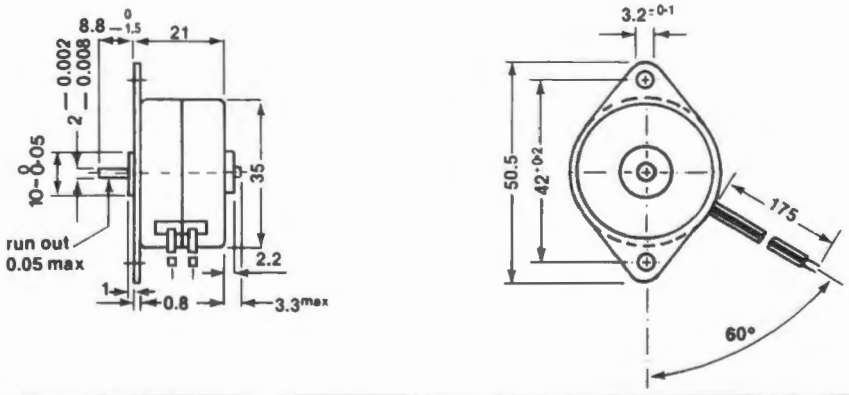


Figure 2 **Dimensions**



Motor characteristics figures are typical at T_{amb} = 25°C unless otherwise stated

Parameter	Phases in parallel	Phases in series	Unit
Nominal input voltage	110	240	V(ac)
Input voltage tolerance	±10	±10	%
Frequency	50/60	50/60	Hz
Output speed	250/300	250/300	rpm
Running current	8	8	mA
Input power	0.8	1.7	W
Starting torque (max)	4	7	mNm
Working torque (max)	4	7	mNm
Torque derating	0.4*	0.4*	% per °C
Temperature increase of motor	30	50	°C
Required phasing capacitor	0.1	0.22	μF
Ambient temperature range	−20 to +60		°C
Insulation test voltage	1500		V
Radial force (max)	2.5		N
Axial force (max)	0.75		N
Mass	80		g
Moment of inertia	2.6		gm cm^2
Case	Zinc plated pressed steel		
Bearings	Sintered bronze (slide)		

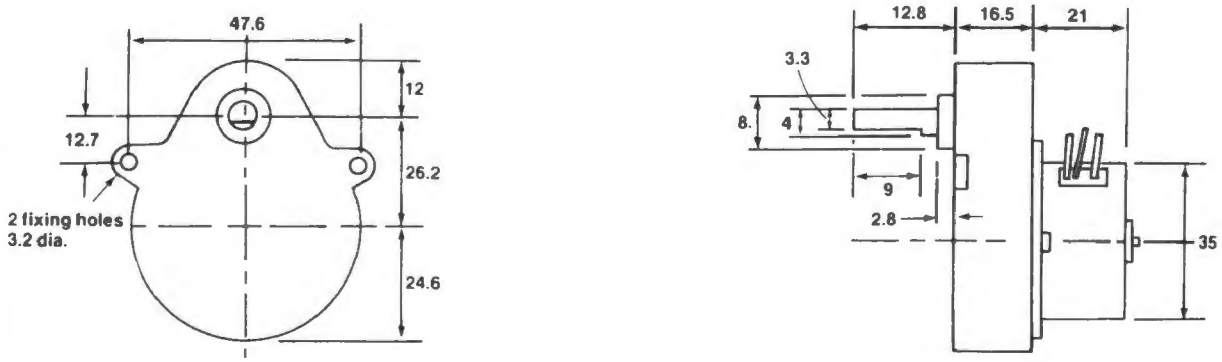
*Derate torque by 0.4% per °C ambient temperature rise above 25°C, e.g. maximum derating at T_{amb} = 60°C is (60 − 25) × 0.4 = 14%

Gearboxes

A range of ovoid shaped gearboxes, for use with RS synchronous motor 332-802. Gears are fixed (reversible) i.e. output shaft will *not* slip in either direction. Their rugged construction consists of cogs mounted between passivated steel side plates with beryllium copper intermediate support bearings and a self-lubricating bronze output bearing. The output shaft is stainless steel and incorporates a flat for ease of load coupling. The high material and constructional quality provides for a very efficient transmission of torque with speed reduction.

These advantages coupled with a gearhead fixture which is based on commonly-used ovoid standards renders this range suitable for reliable, long life performance in many industrial and instrument applications. Figure 3 gives dimensional detail including a motor/gearbox assembly profile.

Figure 3 **Dimensions**



Gearbox parameters coupled with synchronous motor 336-393 at 50 Hz

Stock no.	332-868	336-450	336-444	336-438	336-422	336-416	336-400†
Synchronous output speed (50Hz)	60 rpm	20 rpm	10rpm	5 rpm	2 rpm	1 rpm	1 rph
Gear ratio	25 :6	25 :2	25:1	50:1	125:1	250:1	15,000:1
Maximum output torque *240V i/p	21mNm	62mNm	121mMm	233mMm	560mNm	800mNm**	800mNm**
110V i/p	12mNm	35mNm	69mNm	133mNm	320mNm	576mNm	800mNm**
Maximum radial load	40N (8mm from mtg. face)						
Maximum axial load	20N						
Maximum shaft run out	± 0.13mm						
Maximum backlash	±1°						

*@T_{amb} = 25°C **Absolute maximum torque for any gearbox
†Direction of rotation of output shaft is clockwise when the motor rotation is anticlockwise looking in the same direction.

Assembly detail

Each gearbox is provided with a pinion which is the appropriate link between the motor and the first cog of the gearbox. With the aid of a spacer tool (also provided) and a little RS high strength adhesive retainer 556-014, the pinion may be securely fitted to the motor spindle. Detail assembly instructions are supplied with each gearbox.

Load considerations

Torque

The gearbox should not be subjected to load torques in excess of the maximum output values stated. Should a mechanical stop be applied or the load system is inadvertently jammed, the motor is stall proof and will run with the output shaft locked. (Do not apply a stop to gearbox 336-400 as the mechanical advantage of the gear ratio far exceeds the maximum torque of 800mNm.) As with any gearbox these conditions are not recommended and where necessary loads should be controlled by overtravel cut out mechanisms linked to the motor supply or reversing switch S (Figure 1).

Care should also be taken when increasing the output shaft synchronous speed, by means of additional pulleys and gears, as the maximum available output torque will be proportionally reduced by the ratio of the increased speed and the efficiency of the additional pulley/gear system.

Example

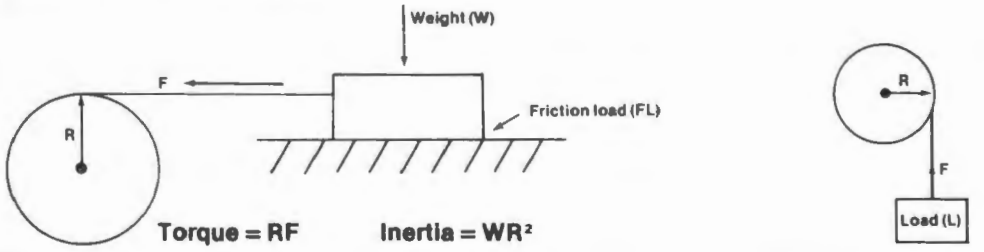
Using gearbox 336-444 at 240 V i/p with required final output speed of 15 rpm and an additional gear efficiency of 80%.

Final available output torque

$$= 121 \times \frac{10}{15} \times 0.8 = 64.5\,\text{mNm}$$

It will also follow that available output torque will increase proportionally with a required reduction in output speed. But in all cases, available torque will decrease with gear efficiency.

Figure 4 **Load torque and moment of inertia**



Torque is the force (F) applied at a radius (R) to lift a Load (L) or overcome Friction (FL). Inertia is the tendency of a body weight (W) to preserve its state of rest or uniform motion in a straight line.

In the case of RS synchronous motors and gearboxes, the motor equivalent moment of inertia (J) at the gearbox output should be equal to or greater than the equivalent load inertia at the same point. This will ensure that load starting and stopping will not override the positional and timing control of the motor. A table of (J) is given for each gearbox fitted with motor 336-393.

Gearbox stock no.	332-868	336-450	336-444	336-438	336-422	336-416	336-400
J (kg cm²)	0.022	0.2	0.8	3.2	20	80	144×10^{3}

Depending on the state of the motor at rest (i.e. the relative position between the rotor and the initiated magnetic field), under adverse conditions a starting time of up to 80 mS should be allowed before synchronous speed is reached.

RS data

Torque conversion factors

Read down

Units to be converted ▼	Imperial			Metric			International system – S.I.		
	0zf-in	lbf-in	lbf-ft	gf·cm	kgf·cm	kgf·m	mN·m	cN·m	N.m
1 oz·in =	1	0.0625	0.005	72	0.072	0.0007	7.062	0.706	0.007
1 lbf·in =	16	1	0.083	1152.1	1.152	0.0115	113	11.3	0.113
1 lbf·ft =	192	12	1	13825	13.825	0.13825	1356	135.6	1.356
1 gf·cm =	0.014	0.0009	0.000 07	1	0.001	0.000 01	0.098	0.01	0.001
1 kgf·cm =	13.89	0.868	0.072	1000	1	0.01	98.07	9.807	0.098
1 kgf·m =	1389	86.8	7.233	100 000	100	1	9807	980.7	9.807
1 mN·m =	0.1416	0.009	0.0007	10.2	0.01	0.0001	1	0.1	0.001
1 cN·m =	1.416	0.088	0.007	102	0.102	0.00102	10	1	0.01
1 N·m =	141.6	8.851	0.738	10.197	10.197	0.10197	1000	100	1

Example 1

Convert 10 lbf·ft into cN·m

lbf·ft → 135.6 (cN·m)

10 x 135.6 = 1356 cN·m

Example 2

Convert 14 kgf·m into lbf·ft

kgf·m → 7.233 (lbf·ft)

14 x 7.233 = 101.26 lbf·ft

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RS data

Commutating auto-zero operational amplifier RS7600

Stock number 309-537

The RS7600 Commutating Auto-Zero (CAZ) operational amplifier, is an ultra low offset, low frequency operational amplifier. The key feature of the CAZ amplifier is automatic compensation for long term drift phenomena and temperature effects. Two internal operational amplifiers are connected so that when one amplifier is processing an input signal the other is maintained in an auto-zero mode.

The RS7600 contains all the circuitry required for system operation, including an oscillator, a counter, level transistors, analogue switches and operational amplifiers. Only two external gain setting resistors and two auto-zero capacitors are needed for complete amplifier function. Control of the oscillator and counter section is provided through the OSC and DR (Division Ratio) terminals. Internal biasing of the two on-chip operational amplifiers is programmable through a three-voltage-level terminal, designated BIAS. The operational amplifier is internally compensated and is primarily intended for applications which require voltage gains from unity through 100.

Absolute maximum ratings

Total supply voltage (V+ to V—) 18 V
Positive supply voltage (GND to V^+) 18 V
Negative supply voltage (GND to V—) 18V
DR Input Voltage $V^+ + 0.3$ to $V^+ - 8$V
Input voltage (C_1, C_2, + Input, — Input, BIAS, OSC) $V^+ + 0.3$ to $V^- - 0.3$ V
Differential input voltage $V^+ + 0.3$ to $V^- - 0.3$ V
Duration of output short circuit Unlimited
Continuous total power dissipation 375 mW
(at or below +25°C free air temp.)

Note:
For operation above 25°C free air temperature, derate 3 mW/°C from 375 mW

Features

- Exceptionally low input offset voltage.
- Constructed using C-MOS technology.
- Low long term input offset voltage drift.
- Low input offset voltage temperature drift.
- Low D.C. input bias current.
- Housed in a 14 pin D.I.L. plastic package.
- Wide common mode and differential input voltage range.

Since the device will auto-zero its internal offset error, no adjustment is required other than that of gain, which is established by the external resistors.

Pin connections top view

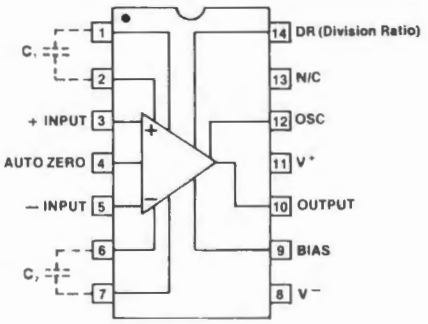
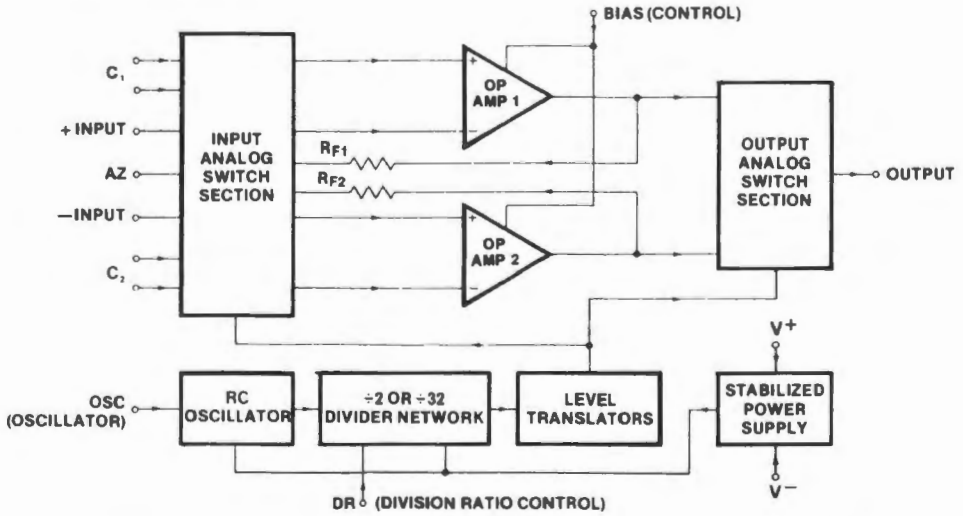


Figure 1 **Block diagram**



Operating characteristics

Test Conditions $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} = 160$ Hz) $C_1 = C_2 = 1\mu F$,

Figure 2 test circuit unless otherwise specified.
Note: f_{COM} is commutation frequency.

Parameter	Symbol	Conditions		Value Min	Value Typ	Value Max	Unit
Input Offset Voltage	V_{OS}	$R_S \leq 1k\Omega$ $C_1 = C_2 = 1\mu F$	Low Bias Setting Med Bias Setting High Bias Setting		±2 ±2 ±7	 ±5 	μV μV μV
Long Term Input Offset Voltage Stability	$V_{OS/TIME}$	Low or med Bias Settings			0.2		μV/year
Average Input Offset Voltage Temperature Coefficient	TCV_{OS}	Low or Med Bias Settings	$-55°C<T_A<+25°C$ $+25°C<T_A<85°C$		0.005 0.01	0.1 0.1	μV/°C μV/°C
Noise Voltage (RMS)	e_n	Band Width 0.1 to 10Hz $R_S \leq 1k\Omega$	Low Bias Med Bias High Bias		0.8 0.8 1.0		μV μV μV
Equivalent Input Noise Voltage Peak-to-peak	$e_{np\text{-}p}$	Band Width 0.1 to 10Hz $R_S \leq 1k\Omega$	Low Bias Med Bias High Bias		4.0 4.0 5.0		μV μV μV
Spot equivalent Noise voltage	e_{n10}	f = 10Hz Band Width 1Hz				700	nV/√Hz
Spot equivalent Noise Current	i_{n10}	f = 10Hz Band Width 1Hz				0.1	pA/√Hz
Differential Input Voltage Range	DIF V_{IN}			$V^--0.3$	to	$V^+ + 0.3$	V
Common Mode Input Range	CMVR	Low Bias Med Bias High Bias		-4.2 -4.0 -3.5		$+4.2$ $+4.0$ $+3.5$	V V V
Common Mode Rejection Ratio	CMRR	Any Bias Setting			88		dB
Power Supply Rejection Ratio	PSRR	Any Bias Setting			110		dB
Non Inverting Input Bias Current	I_{NIB}	Any Bias Setting (Includes charge injection currents)			0.3	3	nA
Inverting Input Bias Current	I_{IB}	Any Bias Setting (Includes charge injection currents)			0.150	1.5	nA
Voltage Gain	A_V	$R_L = 100k\Omega$	Low Bias Med Bias High Bias	90 90 80	105 105 100		dB dB dB
Maximum Output Voltage Swing	V_{OUT}	$R_L = M\Omega$ $R_L = 100k\Omega$ $R_L = 10k\Omega$	 Positive Swing Negative Swing	 +4.4	±4.9 ±4.8 	 -4.5	V V V V
Large Signal Slew Rate	SR	Unity Gain	High Bias Setting Med Bias Setting Low Bias Setting		1.8 0.5 0.2		V/μs V/μs V/μs
Unity Gain Band Width	GBW	See figure 3	High Bias Setting Med Bias Setting Low Bias Setting		1.2 0.3 0.12		MHz MHz MHz
BIAS Terminal Input Current	I_{BIAS}	$V^- - 0.3 \leq V_{BIAS} \leq V^+ + 0.3$ V			±30		pA
BIAS Voltage to Define Current Modes	V_{BH} V_{BM} V_{BL}	Low Bias Setting Med Bias Setting High Bias Setting		$V^+-0.3$ $V^+ + 1.4$ $V^-_{-0.3}$		$V^+ + 0.3$ $V^+ - 1.4$ $V^- + 0.3$	V V V
DR (Division Ratio) Input Current	I_{DR}	$V^+ - 8.0V \leq V_{DR} \leq V^+ + 0.3V$			±30		pA
DR Voltage to define oscillator division ratio	V_{DRH} V_{DRL}	Internal oscillator division ratio 32 Internal oscillator division ratio 2		$V^+-0.3$ V^+-8		$V^+ + 0.3$ $V^+ - 1.4$	V V
Nominal Commutation Frequency	f_{COM}	$C_{OSC} = 0$ pF	DR Connected to V^+ DR Connected to GND		160 2560		Hz Hz
Supply Current	I_S	High Bias Setting Medium Bias Setting Low Bias Setting		4 0.6 0.25	7 1.7 0.6	15 5 1.5	mA mA mA
Operating Supply Voltage Range	$V^+ - V^-$	High Bias Setting Medium or Low Bias Setting		5 4		16 16	V V

Figure 2 **Test circuit: Voltage gain = 1000**

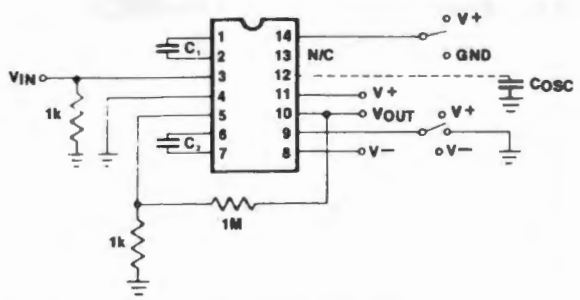
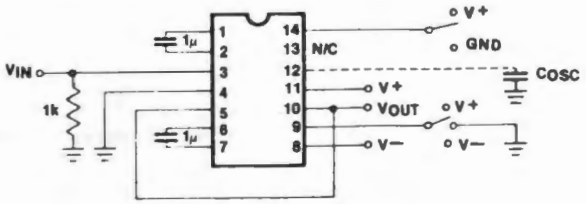


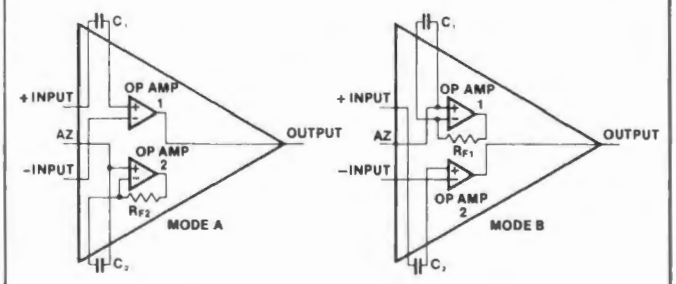
Figure 3 **Test circuit: Unity voltage gain**



Operation

Operation of the RS7600, CAZ operational amplifier is demonstrated in Figure 4. The basic amplifier configuration represented by the large triangles has one more input than does a regular op amp — the AZ, or auto-zero input. The voltage at the AZ input is that voltage to which each of the internal op amps must be auto-zeroed. In mode A, op amp 2 is connected into a unity gain mode through on-chip analogue switches, and charges the external capacitor C_2 to a voltage equal to the DC offset voltage of that amplifier, in addition to the instantaneous low frequency noise voltage. A short time later, the analogue switches reconnect to the on-chip op amps in the configuration shown in Mode B. In this mode, op amp 2 has capacitor C_2 (which was charged to a voltage equal to its offset and noise voltage) connected in series to its non-inverting (+) input and nulls out the input offset and noise voltage of the amplifier. While one of the op amps is processing the input signal, the other is placed in an auto-zero mode and charges a capacitor to a voltage equal to its equivalent DC and low-frequency error voltage. The internal op amps are connected (at a rate designated as the commutation frequency, f_{COM}) so that at all times one or the other of the op amps is processing the input signal, while the voltages on capacitors C_1 and C_2 are being updated regularly to compensate for variables such as low-frequency noise voltage and input offset voltages due to drift with temperature, time, or supply voltage.

Figure 4 **Diagramatic representation of the 2 half cycles of operation of the CAZ operational amplifier**



Bias Control

The on-chip op amps consume over 90% of the power required for the RS7600. Three externally-programmable bias levels are provided. These levels are set by connecting the BIAS terminal to V^+, GND or V^-. The difference between each bias setting is approximately a factor of three, which allows a 9:1 ratio between supply current and the bias setting. The reason for this current programmability is to provide the user with a choice of device power dissipation levels, slew rate values (the higher the slew rate the better the recovery from commutation spikes), and offset errors due to chip "Voltage drop" and thermoelectric effects (the higher the power dissipation the higher the input offset error). In most cases, the medium (MED BIAS) setting will be the best choice.

Output Loading (Resistive)

With a 10 kΩ load the output swing can cover nearly the entire supply voltage range, and the device can be used with loads as low as 2 kΩ. However, with loads of less than 50 kΩ, the on-chip op amps become transconductance amplifiers, since their output impedances are about 50 kΩ each. Thus the open-loop gain is 20 dB less with a 2 kΩ load than it would be with a 20 kΩ load. For high gain configurations requiring high accuracy, output loads of 100 kΩ or more are suggested.

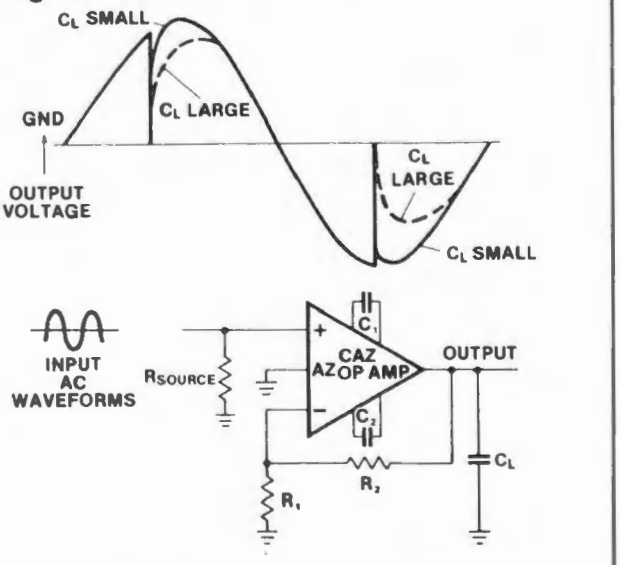
Another consideration which must not be overlooked is the additional power dissipation of the chip which results from a large output swing into a low value load. This added variable can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output to reduce high-frequency noise outside the signal passband of interest. With conventional op amps, the obvious solution would be to place a capacitor across the external feedback resistor to provide the low pass filter.

However, with the CAZ op amp, this is not feasible because of the nature of commutation voltage spikes. The voltage spikes show a low impedance characteristic in the direction of the auto-zero voltage, and a high impedance on the recovery edge, as shown in Figure 5. It can be seen that the effect of a large load capacitor is to produce an area error in the output waveform, and hence an effective gain error. The output low pass filter must be a high impedance type to avoid output voltage area errors. For example, a 1.5 Hz filter should use a 100 kΩ resistor and a 1.0 μF capacitor, or a 1.0 MΩ resistor and an 0.1 μF capacitor.

Figure 5 **Effect of a load capacitor on output voltage waveforms**



RS data

Oscillator and Digital Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open-circuited. If the full divider network is used, this will result in a commutation frequency of about 160 Hz nominal. The commutation frequency is the frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents approximately the optimum frequency at which the input offset voltage is close to minimum, where the low-frequency noise is acceptable, and where errors derived from noise spikes will be low. Other commutation frequencies may provide optimization of other parameters, but always to the detriment of major characteristics.

The oscillator is of a high impedance type, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the desired frequency of the oscillation is 5.2 kHz, the terminal should be left unattached and open. In other instances, it may be desirable to lock the oscillator to a clock or to run it at another frequency. The RS7600, provides two degrees of flexibility. First, the DR (division ratio) terminal permits the user to choose between dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND), to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and V^+, or system ground terminals. For situations which require the commutation frequency to be locked onto a master clock, the OSC terminal can be driven from TTL logic (with resistive pull-up) or from CMOS logic, provided that the V^+ supply (with respect to ground) is + 5V (±10%) and the logic driver also operates from a similar supply voltage. This is because the logic section, including the oscillator, operates from an internal —5V supply referenced to V^+, generated on-chip, and is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-precision DC amplifiers are due to thermoelectric, Peltier or thermocouple effects within junctions consisting of various metals, alloys, silicon, etc. Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1 μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can provide, it is essential to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces.

In addition, the supply voltages and power dissipation should be kept to a minimum. Use the medium bias mode as well as a high impedance load, and keep well away from heat dissipated by surrounding equipment.

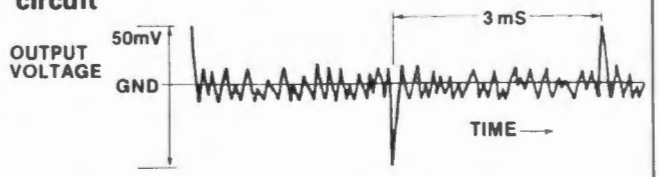
Commutating Voltage Transient Effects

While in most respects the CAZ op amp behaves like a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 100 Hz. This is because of the finite switching transients which occur in the input and output terminals due to commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and include all of the higher harmonics. If the commutation frequency is higher than the highest in-band frequency, these transients can be effectively blanked with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage equal to the input offset voltage (about 5-10 mV), which usually occurs during the transition from the signal processing mode to the auto-zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must be at least 10,000 x 10 pF, or 0.1μF each.

The charge which is injected into the op amp when it is switched into the signal-processing mode produces a rapidly-decaying voltage spike at the input, in addition to an equivalent DC bias current averaged over a full cycle.

Figure 6 **Output waveform from** Figure 2 **test circuit**



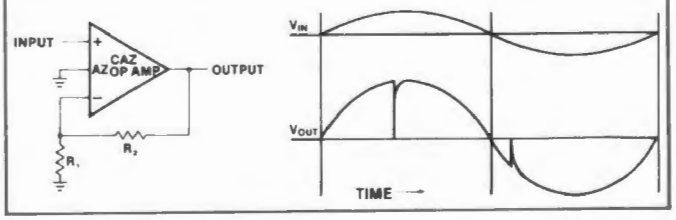
This bias current is directly proportional to the commutation frequency and in most instances will greatly exceed the inherent leakage currents of the input analogue switches, which are typically about 1.0 pA at ambient temperatures of 25°C.

The output waveform shown in test circuit Figure 2 (with no input) is treated in Figure 6. Note that the equivalent noise voltage shown is amplified 1000 times, and that because of the finite slew rate of the on-chip op amps the 7 mV input transients are not amplified by 1000.

The output transient voltage effects (as distinct from the input effects which are propogated through the on-chip op amps) will occur if there is a difference in the output voltage of the internal op amps between the auto-zero modes and the signal-processing modes. The output stage of the on-chip op amp must slew from its auto-zero output voltage to the desired signal-processing output voltage. This is shown in Figure 7, where the system is auto-zeroed to ground.

The duration of the output transients is greatly affected by the gain configuration and the bias setting, since these two parameters have an effect on system slew rate. At low gains and high bias settings, the output transient durations are very short.

Figure 7 **Simple CAZ OP AMP circuit and the output voltage waveform**



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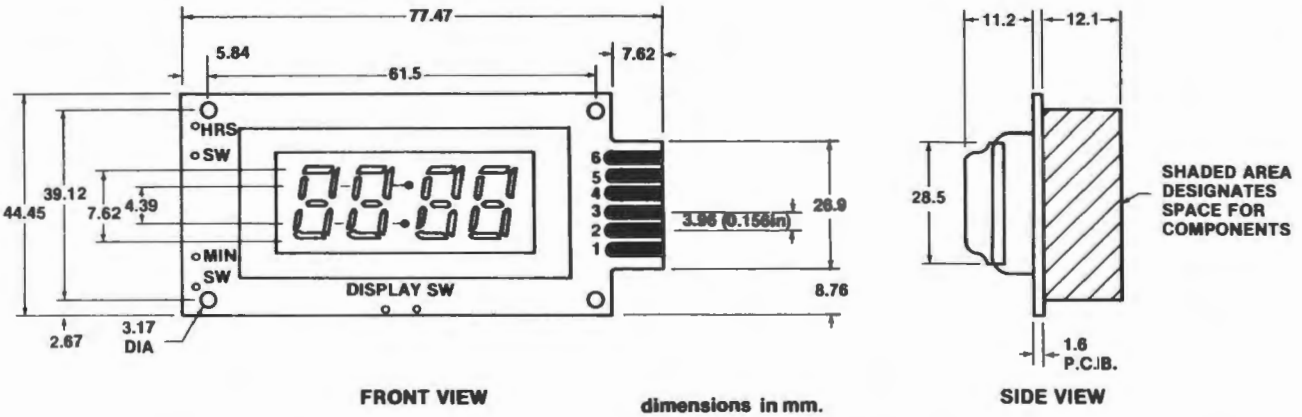
RS data

Fluorescent clock module

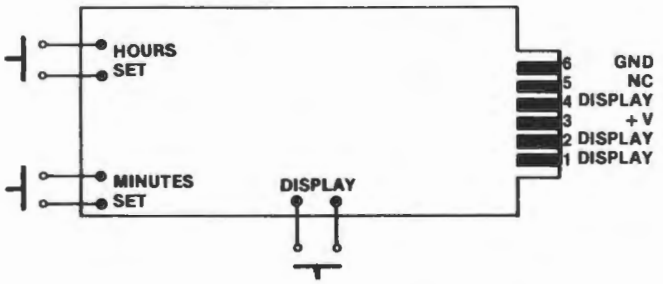
Stock number 304–829

The fluorescent clock module is a miniature 4 digit 12 hour clock with 0.3" green vacuum fluorescent display. It incorporates a 2.097 MHz crystal timebase and is protected against voltage transients and polarity reversal. Time-keeping is maintained down to 9Vdc supply voltage.
The display has leading zero blanking, a flashing central colon, and may be controlled to give 100%, 33% or 0% brightness with variable dimming (between 0% and 33%) achieved via connections to a six way edge connector. Time setting is achieved with HOURS SET and MINUTES SET switches which are disabled when the display is blanked to prevent accidental operation or tampering. By closing the DISPLAY switch the display blanking may be overuled (useful in battery powered portable equipment).
Supply voltage is nominally 12-14Vdc making the clock ideal for automotive applications.

Physical dimensions



External connections



Absolute maximum ratings

Pins 1, 2, 3, 4 w. r.t. pin 6 ——— −24 to +24Vdc continuous
+40Vpk transient for 50ms
+80Vpk transient for 5ms
−200Vpk transient for 1ms

Operating temperature ——— −40°C to +85°C
Storage temperature ——— −65°C to +150°C
Pad temperature during soldering (10 seconds) ——— +300°C

RS data

Electrical characteristics

T_{AMB} = 25°C, V pin 3 = 14Vdc, Display at 10:08 unless otherwise specified.

	Conditions	Min.	Typ.	Max.	Units
Power Supply Voltage	Timekeeping Maintained Time Memory Maintained	9 6	14 14		Vdc Vdc
Power Supply Current	Display Blanked 100% Brightness 33% Brightness 0% Brightness		2 83 97 104	5 95 110 120	mA mA mA mA
Timing Accuracy	T_{AMB} = 25°C T_{AMB} = —25°C to +65°C		±0.5 ±2	±2 ±5	sec/day sec/day
Optical characteristics					
Display Brightness	100% Brightness	700	1400		cdm^{-2}

Note: Display is colour filterable to shades of blue, blue green, green and yellow.

Display brightness controls

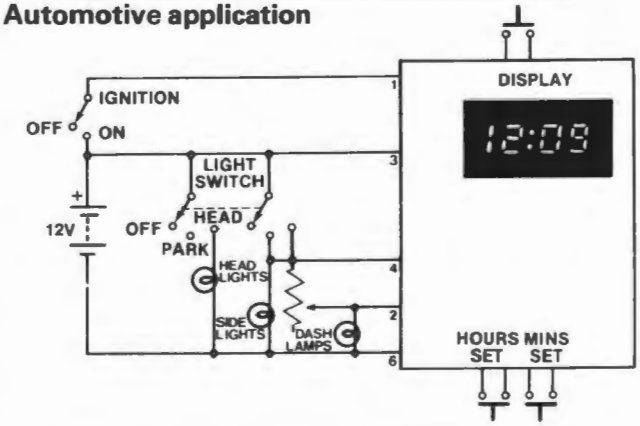
Truth Table

Display Brightness	Input pin connections		
	Pin 1	Pin 4	Pin 2
Blanked	L OR OPEN*	L OR OPEN*	X
100% Brightness	H	L	X
33% Brightness	X	H	H OR OPEN*
0% Brightness	X	H	L

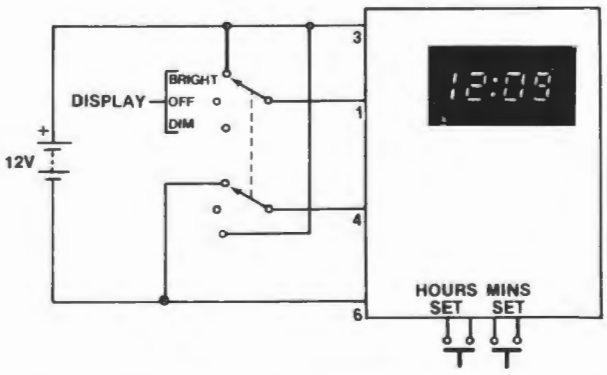
*Pin left open circuit
X Don't care condition
H Connection to supply positive (pin 3)
L Connection to gnd (pin 6)

Applications

Automotive application



Battery powered instrument application



Colon: Central colon display flashes at 0.5Hz rate normally. When setting minutes, colon will flash at 1Hz rate.

Note: Edge connector inputs are protected from voltage transients. Hours set, minutes set and display switch inputs are unprotected and normal handling and soldering precautions for MOS devices should be observed.

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
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Telephone: 0536 201234
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RS data

L.C.D. Clock module

Stock number 304-841

The RS 12.7mm L.C.D. Clock Module consists of a ready assembled printed circuit incorporating a logic chip and L.C.D. display with 12.7mm high digits. An attractive black display bezel is also included with the appropriate fixings and screws.

This module may be used for various timing applications. In addition to its use as a standard alarm clock, the module can be used to trigger external circuits and switch equipment on for pre-set periods (16, 32, 64 or 128 minutes).

Low power consumption makes the module ideal for use in portable or battery-powered equipments.

Absolute Maximum Ratings

Operating voltage, referred to VDD ——— –3V
Operating temperature ——— 0°C to + 50°C
Storage temperature ——— –10°C to + 60°C

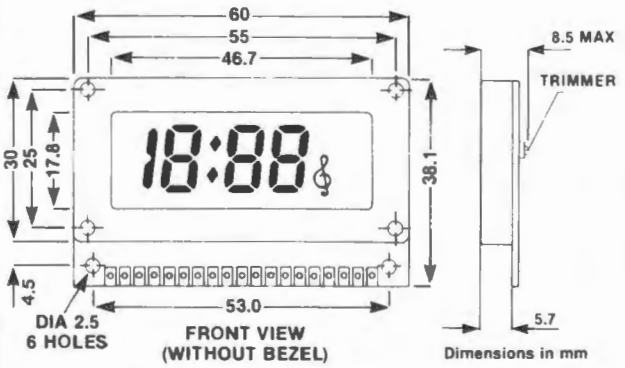
Features

- Time display in 24 hour format
- 12.7mm digit height
- Dual time facility
- 4 minute alarm output
- 4 minute alarm suppression
- 24 minute stopwatch
- 16, 32, 64 or 128 minute interval timer
- Interval timer started manually or from alarm trigger
- Backlit display
- Black bezel for panel mounting

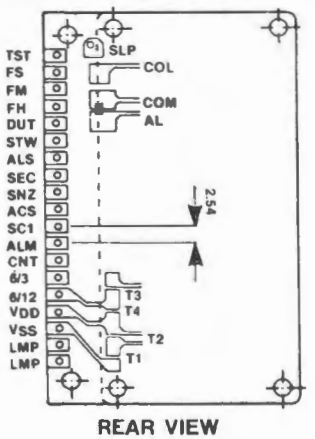
Mode	Display	Terminal To V_{DD}	Terminals for setting
Standard clock hours/minutes	hrs min 22 ✳ 53 ✳	—	FH FM
Standard clock minutes/seconds	min sec 3 ✳ 26 ✳	SEC	FS
Alarm	hrs min 14 : 30	ALS	FH FM
Dual time	hrs min 14 ✳ 30	DUT ALS	FH FM
Stopwatch	min sec 0 : 00	STW ALS	FH FM

✳ Alarm enable ✳ Colon flashing

Dimensions



(Cut out dimensions for Bezel 62.3 × 32.3)



REAR VIEW

Note: The module is supplied with a solder bridge between AL and COM. This disables the alarm sign (𝄞).

Electrical characteristics Tamb = 25°C

Characteristics	Min	Typ	Max	Unit
Supply voltage, (V_{SS}) Referred to V_{DD}	–1.2	–1.5	–1.9	V
Current consumption		6	10	μA
Alarm/control/SLP output current	100			μA
Time accuracy (f = 32.768 kHz)	–30		+30	Sec/Month

Operational description

1. Standard clock

This uses the module's primary counter to display decades of hours, hours, decades of minutes and minutes OR minutes, decades of seconds and seconds.

Terminals FH and FM advance hours and minutes respectively. If connected to V_{DD} continuously, the figures advance once per second. Alternatively the figures will advance once per V_{DD} pulse. The hours and minutes are advanced totally independently. While terminal SEC is connected to V_{DD} the minutes and seconds will be displayed. Terminal SEC is only operative while the standard clock is being displayed.

A V_{DD} pulse on terminal FS will zero seconds of the standard clock. If at this zero pulse, the seconds display is less than 30 then the seconds will zero independently. However if the seconds display is greater than or equal to 30 then the seconds will zero and advance the minutes by 1. Terminal FS is operative while the standard clock is being displayed and is independent of the state of terminal SEC.

2. Dual time

The module incorporates a secondary counter which can be used as a secondary clock recording a different time. It is driven in parallel from the minute pulse of the standard clock.

To operate this dual time facility terminal DUT must be continuously connected to V_{DD}.

To set the time of the secondary clock terminals FH and FM must be connected to V_{DD} in the usual way.

It should be noted that in this dual time mode the secondary clock will not display minutes with seconds.

3. Stopwatch

The secondary counter can also be used as a stopwatch. To activate this facility, terminals STW and ALS must be continuously connected to V_{DD}. The stopwatch will count minutes and seconds up to 24 minutes, with leading zero blanking.

In this state terminals FH and FM act as follows:

Terminal FH:	Pulse to stop count Pulse to start count
Terminal FM:	Pulse to stop and clear

N.B. As only one 4 digit secondary counter is available, the stopwatch and dual time facilities cannot be used in parallel.

4. Alarm

The alarm time is loaded into the secondary counter using terminals FH and FM (as for the standard clock) with ALS connected to V_{DD}.

The secondary counter is used here as memory, hence neither dual time nor stopwatch can be used if the alarm facility is required.

The alarm will sound as soon as the contents of the primary and secondary counters are equal, regardless of which counter is currently being displayed.

The alarm once started, may be manually cancelled by a V_{DD} pulse to terminal ACS or it will sound for four minutes and then automatically self cancel.

If alarm/override (terminal SNZ) is connected to V_{DD} momentarily, then the alarm will cancel and sound again after three to four minutes of silence.

The alarm is pulse triggered. Hence even if dual time is selected when the alarm sounds, the alarm will still automatically cancel after four minutes.

The alarm will also be cancelled if either the standard clock or the alarm time is altered.

The alarm will not go off if the period timer is in operation or if terminal ACS is connected to V_{DD}.

5. Control timer

Terminal CNT can be used to switch external equipment in conjunction with the alarm facility. Terminal CNT goes to V_{DD} when the alarm sounds, and will stay at V_{DD} for a period pre-set by the states of terminals 6/12 and 6/3 (i.e. 16, 32, 64 or 128 minutes).

The CNT output may be manually activated by a V_{DD} pulse to terminal SCI and manually cancelled by a V_{DD} pulse to terminal ACS.

The output will also cancel if either the standard clock or the alarm is altered.

6. Period timer

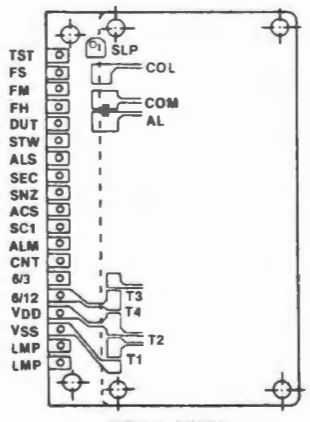
Terminal SLP can be used to switch external equipment.

This is an independent timing facility and is neither activated nor de-activated at the alarm time.

Terminal SLP goes to V_{DD} for a duration pre-set by the states of terminals 6/12 and 6/3 (i.e. 16, 32, 64 or 128 minutes) after a V_{DD} pulse to terminal SCI.

The period timer can be de-activated manually by an earth pulse to terminal ACS.

Terminal function



REAR VIEW

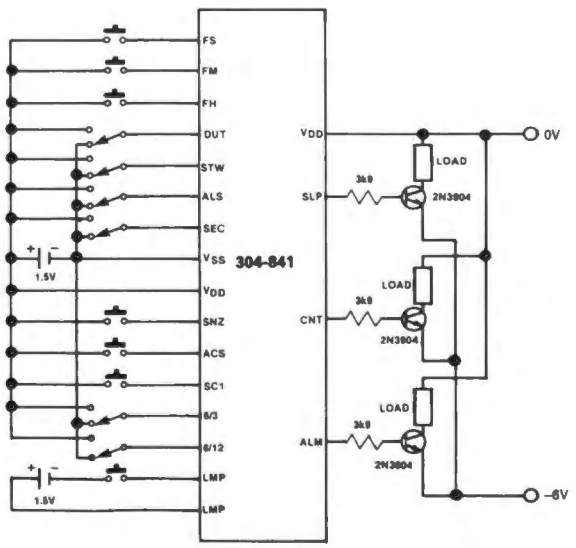
Note: T1, T2, T3, T4 are junctions for linking by solder bridge

Terminal	Voltage Applied	
TST	V_{DD}	Allows high speed testing of the clock module:
		1. With FH connected to V_{DD}, hours and minutes advance fast.
	V_{DD}	2. With SEC and FM connected to V_{DD}, minutes and seconds advance fast.
FS	V_{DD}	1. In STANDARD CLOCK mode, resets seconds to '00'.
	V_{DD}	2. In ALARM or DUAL TIME mode, will enable FM to advance the tens of minutes.
FM	V_{DD}	1. Increments minutes by one per second (or by one per pulse if a pulsed V_{DD} is applied).
	V_{DD}	2. In STOPWATCH mode, resets counters to 0 min 00 sec.
	V_{DD}	3. In ALARM or DUAL TIME mode, increments tens of minutes (in conjunction with FS).
FH	V_{DD}	1. Increments hours by one per second (or by one per pulse if a pulsed V_{DD} is applied).
	V_{DD}	2. In STOPWATCH mode, causes counter to start and stop alternately.
DUT	V_{DD}	DUAL TIME is displayed when DUT and ALS are connected to V_{DD}.
STW	V_{DD}	STOPWATCH is displayed when STW and ALS are connected to V_{DD}.
ALS	V_{SS}	1. STANDARD CLOCK is displayed.
	V_{DD}	2. ALARM is displayed.
	V_{DD}	3. DUAL TIME is displayed in conjunction with DUT.
	V_{DD}	4. STOPWATCH is displayed in conjunction with STW.
SEC	V_{SS}	1. Normally connected to V_{SS} to display hours and minutes.
	V_{DD}	2. In STANDARD clock mode only, minutes and seconds (but not tens of minutes) are displayed when connected to V_{DD}.
SNZ	V_{DD}	This overide control will stop the ALARM for between 3 and 4 minutes when momentarily connected to V_{DD}.

Terminal	Voltage Applied	
ACS	V_{DD}	Cancels PERIOD TIMER output, CONTROL TIMER output and ALARM output when momentarily connected to V_{DD}.
SCI	V_{DD}	Starts PERIOD and CONTROL timers when momentarily set to V_{DD}.
ALM	—	Modulated ALARM output. Activated for max. period of 4 mins .
CNT	—	CONTROL timer output — goes to V_{DD} level (for a period set by 6/3 and 6/12 in conjunction with SCI or after ALARM output is activated.
6/3 and 6/12	V_{DD}/V_{SS}	Selects duration of PERIOD TIMER and CONTROL TIMER. PERIOD REQUIRED 16 minutes: 6/3 and 6/12 to V_{DD} (or bridge T2 and T4 solder links) 32 minutes: 6/3 to V_{DD} and 6/12 to V_{SS} (or bridge T2 and T3 solder links). 64 minutes: 6/3 and 6/12 to V_{SS} (or bridge T1 and T3 solder links). 128 minutes: 6/3 to V_{SS} and 6/12 to V_{DD} (or bridge T1 and T4 solder links).
V_{DD}	—	Positive supply terminal.
V_{SS}	—	Negative supply terminal.
LMP	—	These two terminals should be connected to 1.5V for backlit display.
SLP	—	This output goes to V_{DD} level for a period set by 6/3 and 6/12 after SCI has been connected to V_{DD}.
COL	—	Colon output signal.
COM	—	Display common point.
AL	—	Controls " 🔔 " sign (used as an alarm active sign).
		1. When connected to COL, sign will flash when colon flashes in STANDARD CLOCK and DUAL TIME modes. In other modes sign will be displayed continuously.
		2. Connect to COM when the sign is not required.
		N.B. This terminal affects the display only and cannot be used to enable/disable the alarm output.

Application circuits

Figure 1: **Alarm clock with period timer, alarm override, stopwatch, control, dual time functions, operated by individual switches.**



RS data

Figure 2: **Alarm clock with period timer, alarm override, stopwatch, dual time functions, operated by rotary switches.**

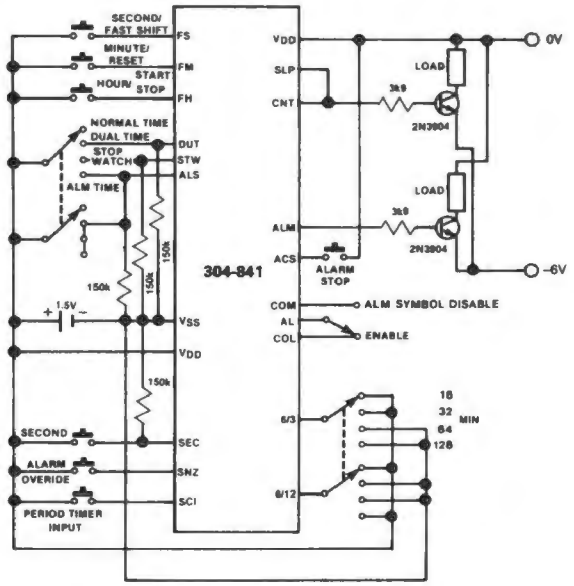
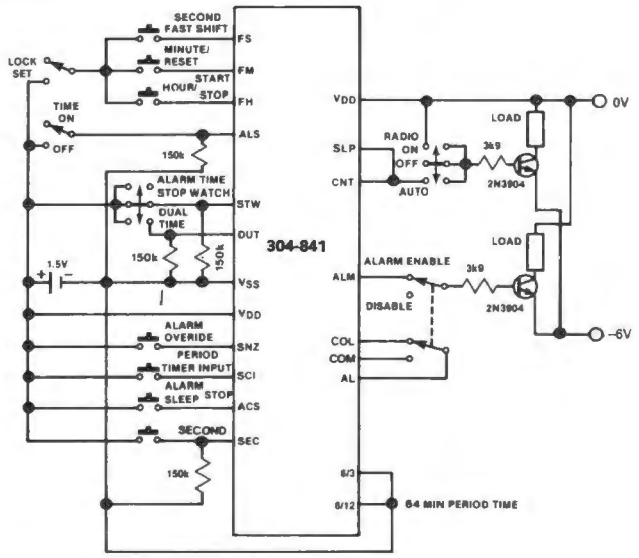


Figure 3: **Alarm clock with period timer, alarm override, stopwatch, dual time functions, operated by slide switches.**



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RS data

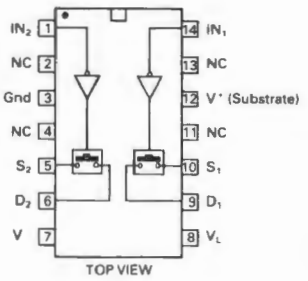
Analogue switch i.c.'s

A comprehensive range of analogue switches suitable for use in a wide range of applications including analogue signal multiplexing and switching, data acquisition systems and high frequency switching, i.e. video signals. The switches exhibit a low on resistance which is virtually constant over the entire analogue signal range and a high OFF resistance and low transient switching essential in sample and hold circuits. Input signal range ±V supply, operating temperature range 0°C to +70°C. TTL, DTL and CMOS compatible, except DG308 which is only CMOS compatible.

HI 200 309-559

Dual monolithic SPST CMOS Analogue Switch

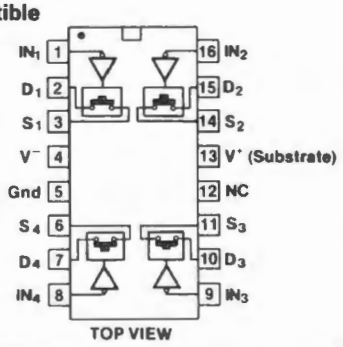
IN LOGIC	SWITCH
0	ON
1	OFF



DG 308 303-551

Quad SPST CMOS Compatible Analogue Switch

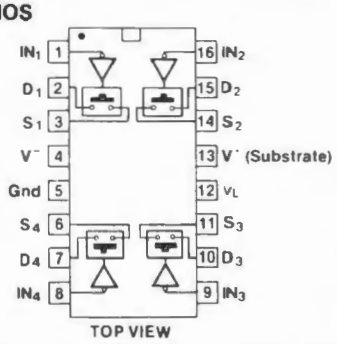
IN LOGIC	SWITCH
0	OFF
1	ON



HI 201 309-565

Quad monolithic SPST CMOS Analogue Switch

IN LOGIC	SWITCH
0	ON
1	OFF

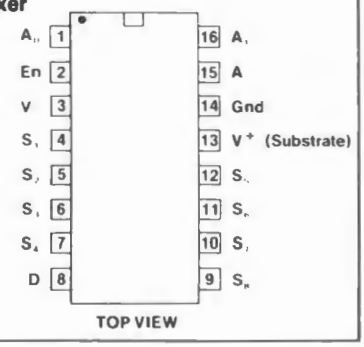


DG 508 309-571

8-Channel CMOS Multiplexer

TRUTH TABLE

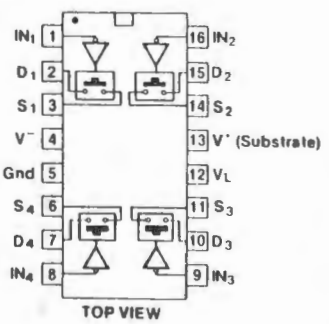
A_2	A_1	A_0	EN	SWITCH ON
X	X	X	0	NONE
0	0	0	1	S_1
0	0	1	1	S_2
0	1	0	1	S_3
0	1	1	1	S_4
1	0	0	1	S_5
1	0	1	1	S_6
1	1	0	1	S_7
1	1	1	1	S_8



DG 211 303-573

Quad SPST Analogue Switch

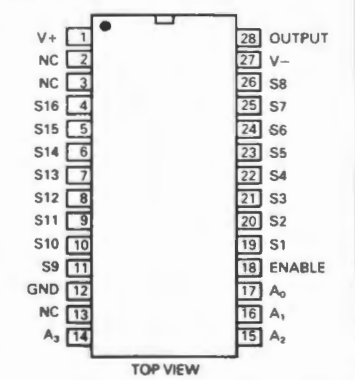
IN LOGIC	SWITCH
0	ON
1	OFF



HI 506 301-814

16-Channel CMOS Multiplexer

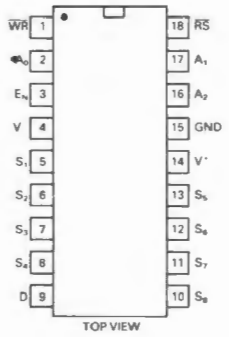
A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16



DG 528 300-467

8-Channel Multiplexer with Data Input Latches

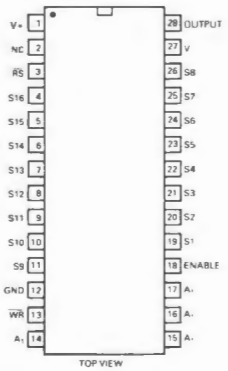
A_2	A_1	A_0	En	$\overline{WR}$	$\overline{RS}$	
X	X	X	X	↓	1	Maintains previous switch condition
X	X	X	X	X	0	NONE (latches cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8



DG 526 300-451

16-Channel Multiplexer with Data Input Latches

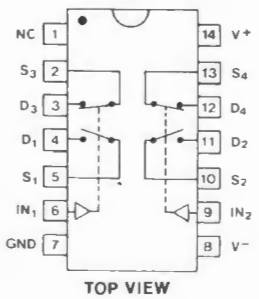
	A_3	A_2	A_1	A_0	E_n	$\overline{WR}$	$\overline{RS}$	On Switch
Latching	X	X	X	X	X	↓	1	Maintains previous switch state
Reset	X	X	X	X	X	X	0	None (latches cleared)
Transparent Operation	X	X	X	X	0	0	1	None
	0	0	0	0	1	0	1	1
	0	0	0	1	1	0	1	2
	0	0	1	0	1	0	1	3
	0	0	1	1	1	0	1	4
	0	1	0	0	1	0	1	5
	0	1	0	1	1	0	1	6
	0	1	1	0	1	0	1	7
	0	1	1	1	1	0	1	8
	1	0	0	0	1	0	1	9
	1	0	0	1	1	0	1	10
	1	0	1	0	1	0	1	11
	1	0	1	1	1	0	1	12
	1	1	0	0	1	0	1	13
	1	1	0	1	1	0	1	14
	1	1	1	0	1	0	1	15
	1	1	1	1	1	0	1	16



DG 303 303-567

Dual SPDT Analogue Switch

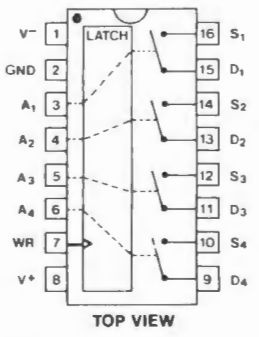
In Logic	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF



AD 7590 303-595

Quad SPST Analogue Switch with Data Latch

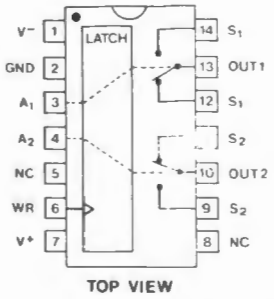
Address	WR	Switch
0	0	OFF
1	0	ON
X	1	Latched in previous state



AD 7592 303-589

Dual SP Changeover Analogue Switch with Data Latch

Address	WR	Switch Output
0	0	Pin 12 and Pin 11
1	0	Pin 14 and Pin 9
X	1	Latched in previous state



Electrical characteristics

$T_A = 25°C$, $V+ = 15V$, $V- = -15V$, $GND = 0$

Parameter	Symbol	Conditions	HI 200		HI 201		Units
			Typ.	Max.	Typ.	Max.	
Drain-Source ON resistance	r_{DSON}[1]	$V_D = 10V$, $V_{IN} = 0.8V$ $V_D = -10V$, $V_{IN} = 0.8V$	55 55	80 80	65 65	100 100	Ω Ω
Source OFF leakage current	I_{SOFF}	$V_D = \pm 14V$	1	500	2	250	nA
Drain OFF leakage current	I_{DOFF}	$V_S = \pm 14V$	1	500	2	250	nA
Channel ON leakage current	I_{DON}[2]	$V_D = V_S \pm 14V$	0.02	500	2	250	nA
Input-transition voltage	V_T[3]		0.8/3.0		0.8/3.0		V
Input (address) current (Input voltage high)	$I_{INH}(I_{AH})$	$V_{IN} = 2.4V$ $V_{IN} = 15V$	0.001 0.001	1 1	0.001 0.001	1 1	μA μA
Peak input (address) current for transition	I_{IN} PEAK ($I_{A\ PEAK}$)	$V_{IN} = 1.45V$ ± 10%	—	1	—	1	μA
Input (address) current (Input voltage low)	I_{INL} (I_L)	$V_{IN} = 0V$	—	1	—	1	μA
Turn ON time (EN)	t_{ON} (EN)		0.24	—	0.185	—	μs
Turn OFF time (EN)	t_{OFF} (EN)		0.5	—	0.22	—	μs
Source OFF capacitance	C_{SOFF}	$V_S = 0$ $V_{IN} = 5V$	5.5	—	5.5	—	pF
Drain OFF capacitance	C_{DOFF}	$V_D = 0$ $V_{IN} = 5V$	5.5	—	5.5	—	pF
Channel ON capacitance	$C_{DON} + C_{SON}$	$V_D = V_S = V_{IN} = 0$	11	—	11	—	pF
OFF isolation			70	—	80	—	dB
Multiplexer switching time	$t_{transition}$		—	—	—	—	μs
Break before Make time	t_{open}		—	—	—	—	μs
Operational supply current	$I_{operational}$	$V_{IN} = 0$	±0.5	±2.0	±0.5	±2.0	mA
Standby supply current	$I_{standby}$	All channels OFF $V_{IN} = 5V$	—	—	—	—	mA

Notes: 1 r_{DSON} is quoted at $I_D = 1mA$.
2 Leakage from driver into ON switch.
3 Where two values are quoted, these are the input Low and High threshold levels.

Absolute maximum ratings

Parameter	Units	HI200	HI201
Power dissipation (Package)[1]	mW	450	750
Supply voltage	V	±20	±20
V_S or V_D Positive	V	$V^+ + 2V$	$V^+ + 2V$
V_S or V_D Negative	V	$V^- - 2V$	$V^- - 2V$
V_{IN}, V_{REF}, A or EN to Gnd	V	$V^- - 4V$ to $V^+ + 4V$ (–5 to + 20V) (3)	$V^- - 4V$ to $V^+ + 4V$ (–5 to + 20V) (3)
Current any terminal except S or D	mA	—	—
Continuous current S or D	mA	—	—
Peak current S or D[2]	mA	80	80
Operating Temperature	°C	0 to +75	0 to +75
Storage Temperature	°C	–65 to +150	–65 to +150

Notes: 1. IC soldered into PCB, DG Types derate by 6.5mW/°C above 25°C.
2. Pulsed 1mS, 10% duty cycle maximum.
3. Figures in brackets refer to V_{REF} parameter only.

Electrical characteristics

T_A = 25°C, V+ = 15V, V– = –15V, GND = 0 (Conditions in brackets are for DG 508 only)

Parameter	Symbol	Conditions	DG 211		DG 308		DG 508	
			Typ.	Max.	Typ.	Max.	Typ.	Max.
Drain-Source ON resistance	r_{DSON}[1]	V_D = 10V, V_{IN} = 0.8V V_D = –10V, V_{IN} = 0.8V	125 115	175 175	70 60	100 100	270 230	450 450
Source OFF leakage current	I_{SOFF}	V_D = ± 14V (± 10V)	±0.01	±5	±0.1	±5	±0.005	±5
Drain OFF leakage current	I_{DOFF}	V_S = ± 14V (± 10V)	±0.02	±5	±0.1	±5	±0.015	±20
Channel ON leakage current	I_{DON}[2]	V_D = V_S ± 14V ± 10V)	±0.15	±5	±0.1	±5	±0.03	±20
Input-transition voltage	V_T[3]		1.5	—	Mid-supply		1.45	
Input (address) current (Input voltage high)	$I_{INH}(I_{AH})$	V_{IN} = 2.4V (V_A = 2.4V) V_{IN} = 15V (V_A = 15V)	–0.0004 0.003	–1 1	— 0.001	— 1	–0.02 0.006	–10 10
Peak input (address) current for transition	I_{IN} PEAK ($I_{A\ PEAK}$)	V_{IN} = 1.45V (V_A = 1.45V) ± 10%	—	—	—	—	–75	—
Input (address) current (Input voltage low)	I_{INL} (I_L)	V_{IN} = 0V (V_{EN} = 0V)	–0.0004	–1	–0.001	–1	–0.002	–10
Turn ON time (EN)	t_{ON} (EN)		0.46	—	0.13	0.2	1.0	—
Turn OFF time (EN)	t_{OFF} (EN)		0.45	—	0.09	0.15	0.4	—
Source OFF capacitance	C_{SOFF}	V_S = 0 V_{IN} = 5V	7	—	7	—	6.0	—
Drain OFF capacitance	C_{DOFF}	V_D = 0 V_{IN} = 5V	7	—	7	—	25	
Channel ON capacitance	C_{DON} + C_{SON}	V_D = V_S = V_{IN} = 0	20	—	20	—	—	—
OFF isolation			70	—	>50	—	68	—
Multiplexer switching time	$t_{transition}$		—	—	—	—	0.6	—
Break before Make time	t_{open}		—	—	—	—	0.2	—
Operational supply current	$I_{operational}$	V_{IN} = 0 (V_A = 0, V_{EN} = 5V)	±0.25	±0.4	—	±0.1	+1.3 –0.7	+2.4 –1.5
Standby supply current	$I_{standby}$	All channels OFF V_{IN} = 5V (V_A = 0, V_{EN} = 0V)	—	—	—	—	+1.3 –0.7	+2.4 –1.5

Notes: 1 r_{DSON} is quoted at I_D = 1mA except for DE 508 = 200μA and DG 303 = 10mA
2 Leakage from driver into ON switch.
3 Where two values are quoted, these are the input Low and High threshold levels.

Absolute maximum ratings

Parameter	Units	DG211	DG308	DG508
Power dissipation (Package)[1]	mW	470	470	470
Supply voltage	V	±16	±20	±20
V_S or V_D Positive	V	V^- +40V	V^+ +2V or V^- –2V 20mA	V^+ +2V or V^- – 2V 20mA
V_S or V_D Negative	V	V^+ –40V		
V_{IN}, V_{REF}, A or EN to Gnd	V	–0.3 to V^+	–0.3 to V^+	–0.3 to V^+
Current any terminal except S or D	mA	30	30	30
Continuous current S or D	mA	20	20	20
Peak current S or D[2]	mA	70	100	40
Operating Temperature	°C	0 to +70	0 to +70	0 to +70
Storage Temperature	°C	–65 to +125	–65 to +125	–65 to +125

Notes: 1. IC soldered into PCB, DG Types derate by 6.5mW/°C above 25°C. HI 506, derate by 8mW/°C above 25°C.
2. Pulsed 1mS, 10% duty cycle maximum.
3. Figures in brackets refer to V_{REF} parameter only.

HI 506		DG 528		DG 526		DG 303		AD 7590		AD 7592		Units
Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
270 270	400 400	270 230	450 450	250 250	400 400	30 30	50 50	60 60	90 90	60 60	90 90	Ω Ω
0.03	—	±0.005	±5	0.02	1	±0.1	±5	±0.5	±5	±0.5	±5	nA
1.0	—	±0.015	±20	0.2	10	±0.1	±5	±0.5	±5	±0.5	±5	nA
1.0	—	±0.03	±20	0.2	10	±0.1	±5	±0.5	±5	±0.5	±5	nA
0.8/2.4		0.8/2.4		0.8/2.4		0.8/4.0		0.8/2.4		0.8/2.4		V
— 0.001	— 5	–0.002	–10	0.02 0.02	10 10	–0.001 —	–1 —	0.01 0.01	1 1	0.01 0.01	1 1	μA μA
—	—	—	—	—	—	—	—	—	1	—	1	μA
0.001	5	–0.002	–10	0.01	10	–0.001	–1	—	1	—	1	μA
0.3	—	1.0	—	0.7	1.5	0.15	—	0.17	0.34	0.3	0.6	μs
0.3	—	0.4	—	0.4	1	0.13	—	0.3	0.6	0.3	0.6	μs
4	—	5	—	10	—	14	—	10	—	10	—	pF
44	—	25	—	35	—	14	—	10	—	10	—	pF
—	—	—	—	—	—	40	—	60	—	60	—	pF
75	—	68	—	55	—	63	—	>85	—	>85	—	dB
0.3	—	0.6	1	0.65	1	—	—	—	—	—	—	μs
0.08	—	0.2	—	—	—	—	—	—	—	—	—	μs
+3.4 –0.8	+5.0 –2.0	— —	+2.5 –1.5	—	+2.5 –1.5	0.23 –0.001	1 –0.1	—	±1	—	±1	mA
+3.4 –0.8	+5.0 –2.0	—	—	—	—	—	—	—	—	—	—	mA

HI 506	DG 528	DG 526	DG303	DG 7590	AD 7592
1200	470	625	470	670	670
±20	±20	±20	±20	±17	±17
V^+ +2V	V^+ + 2V or V^- –2V 20mA	V^+ + 2V or V^- –2V 20mA	V^+ +2V or V^- –2V 20mA	V^+ + 25V	V^+ +25V
V^- +2V				V^- –25V	V^- –25V
V^- 4V to V^+ + 4V	V^+ + 2V or V^- –2V 20mA	V^+ + 2V or V^- –2V 20mA	–0.3 to V^+	–0.3 to V^+ +0.3	–0.3 to V^+ + 0.3
—	30	30	30	—	—
—	20	20	20	50	50
50	40	40	100	150	150
0 to 75	0 to 70	0 to 70	0 to 70	0 to 70	0 to 70
–65 to +150	–65 to +125	–65 to +125	–65 to +125	–65 to +150	–65 to +150

4175

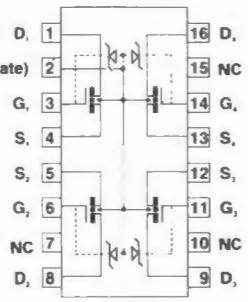
Quad D-MOS switch array

SD 5001 **301-808**

Quad D – MOS analogue switch array featuring insulated gate FET transistors.

(Substr (Substrate)

In Logic	FET
0	OFF
1	ON



TOP VIEW

SD 5001 specification

Absolute maximum ratings $T_A = 25°C$

PARAMETER		SD5001	UNITS
V_{DS} Drain-to-source		+10	Vdc
V_{SD} Source-to-drain 1		+10	
V_{DB} Drain-to-substrate		+15	
V_{SB} Source-to-substrate		+15	
V_{GS} Gate-to-source		+25	
		−15	
V_{GB} Gate-to-substrate		+25	
		−0.3	
V_{GD} Gate-to-drain		+25	
		−15	
I_D Drain current		50	mA
Ambient temperature range	Storage	−55 to +150	°C
	Operating	0 to +85	
Power Dissipation	Total package dissipation[2]	640	mW
	Individual transistor dissipation	300	

NOTES:
1. Refer to test conditions specified in Electrical Characteristics Table.
2. Derated 5mW per degree centigrade.

Electrical characteristics $T_A = 25°C$

PARAMETER		TEST CONDITIONS	SD5001 Min	SD5001 Typ	SD5001 Max	UNIT
BREAKDOWN VOLTAGE BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	10	25		V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$	10			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source Open $I_D = 10nA$	15			V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain Open $I_S = 10\mu A$	15			V
LEAKAGE CURRENT $I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$, $V_{DS} = +10V$		1	10	nA
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$, $V_{SD} = +10V$		1	10	nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$, $V_{GB} = 25V$			1	μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.1	1.0	2.0	V
$r_{DS}(On)$	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +5V$		50	70	Ω
		$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +10V$		30		
		$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +15V$		23		
		$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +20V$		19		
$r_{DS}(On)$	Resistance match (Note 1)	$I_D = 1.0mA$, $V_{SB} = 0$ $V_{GS} +5V$		1	5	Ω

NOTE:
1. This untested parameter is guaranteed by design.

A.C. electrical characteristics

PARAMETER		TEST CONDITIONS	SD5001 Min	SD5001 Typ	SD5001 Max	UNIT
gfs	Forward transconductance	$V_{DS} = 10V$, $V_{SB} = 0V$ $I_D = 20mA$, f = 1kHz	10	15		mmhos
$C(_{GS} + _{GD} + _{GB})$	Gate node capacitances	$V_{DS} = 10V$, f = 1MHz $V_{GS} = V_{BS} = -15V$		2.4	3.5	pf
$C(_{GD} + _{DB})$	Drain node capacitances			1.3	1.5	
$C(_{GS} + _{SB})$	Source node capacitances			3.5	4.0	
C_{DG}	Reverse transfer capacitances			0.3	0.5	
C_T	Cross talk			−107		dB

Switching characteristics

V_{DD}	R_L	$t_{d(ON)}$(ns) TYP	$t_{d(ON)}$(ns) MAX	t_r(ns) TYP	t_r(ns) MAX	*t_{OFF}(ns) TYP	*t_{OFF}(ns) MAX
5	680	0.6	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	

*t_{OFF} is dependent on R_L and does not depend on the device characteristics.

HI 506 characteristics

Figure 1 **Logic threshold vs. power supply voltage**

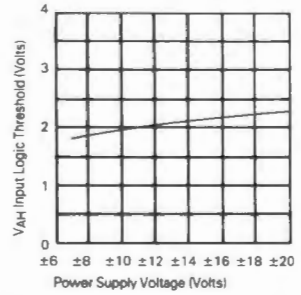


Figure 2 **On channel current vs. voltage**

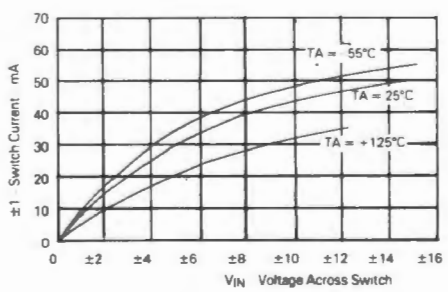
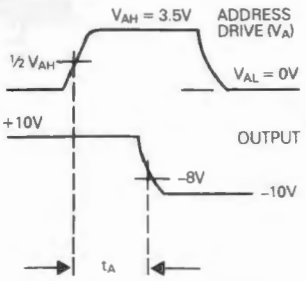


Figure 3 **Switching waveforms**



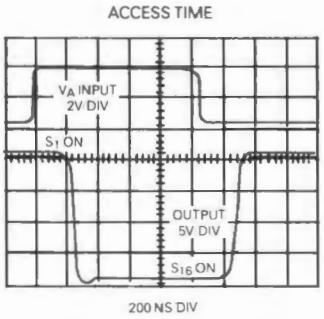


Figure 4 **Address decoder**

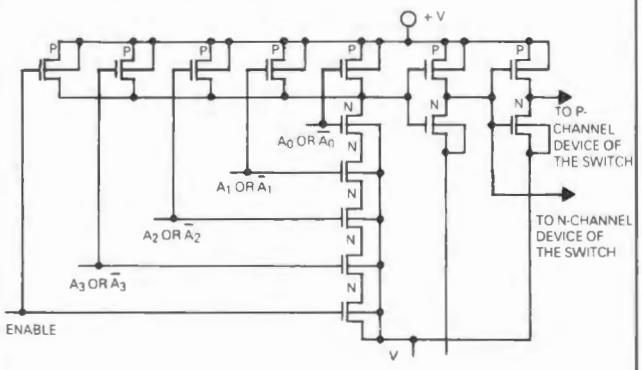
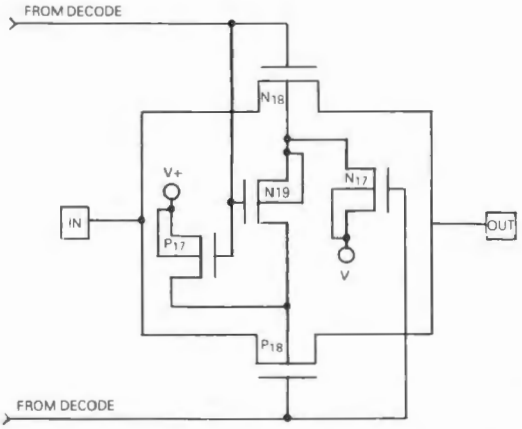


Figure 5 **Multiplex switch**



Switching characteristics

Switch Logic Thresholds

DG211

V_L = +5V for TTL input threshold i.e. 1.6V
V_L = GND Input threshold set at 0V ±500mV
V_L = V_{DD} for CMOS input threshold

V_L Voltage	Logic Threshold
0	0
5	1.5
10	3
15	4.5
20	6

HI200 and HI201

V_L open circuit for TTL compatible inputs
V_L connected to V_{DD} for CMOS compatible inputs where V_{DD} > +5.5V

Figure 6 **Timing sequence for AD7590 and AD7592**

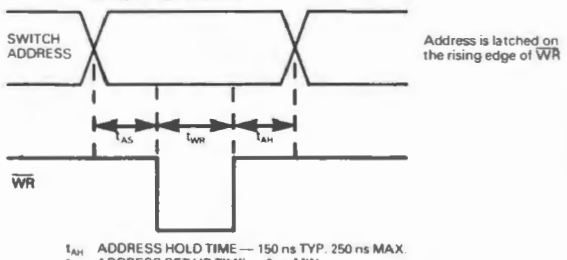
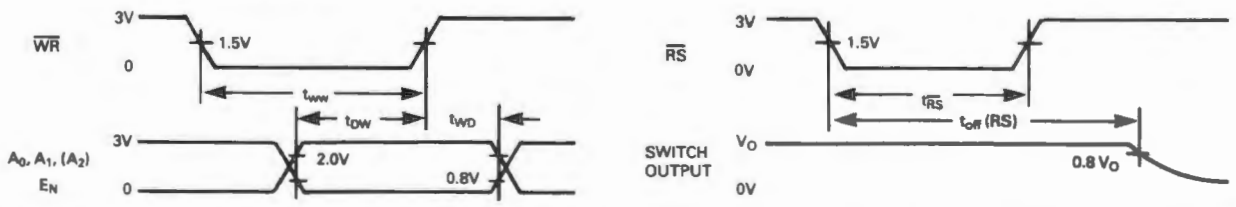


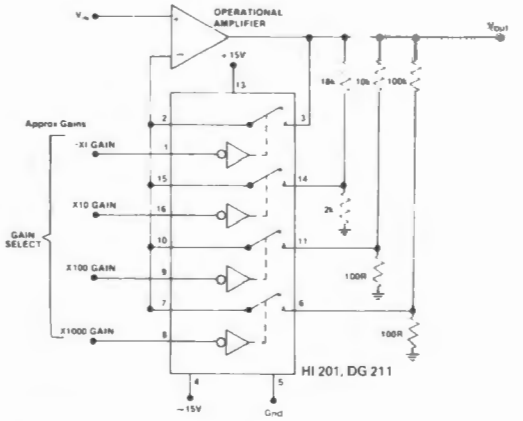
Figure 7 **Timing sequence for DG528 & DG526**



RS data

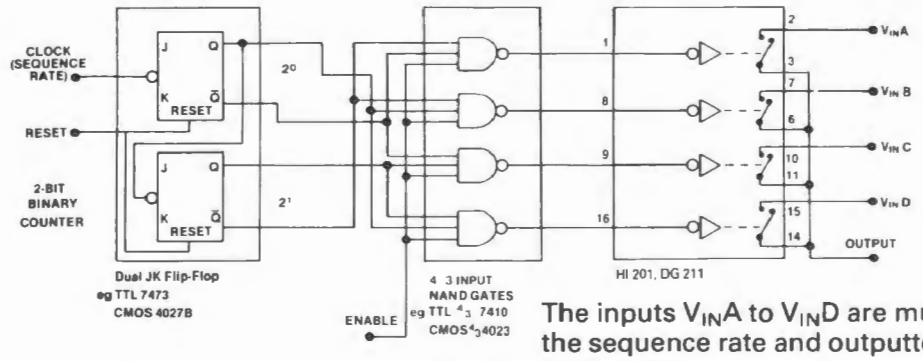
Applications using HI201 and DG211

Figure 8 **Gain programmable amplifier**



The desired gain is selected by taking the required gain select pin from logic 1 to logic 0. All other gain select pins being tied to logic 1. (V_{REF} open circuit.)

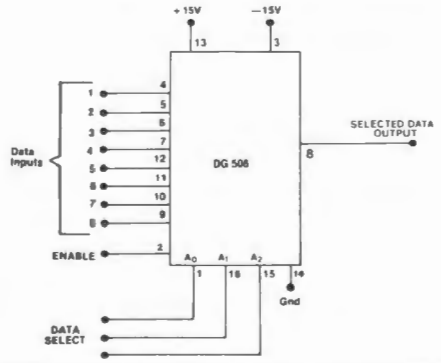
Figure 9 **4-channel sequencing multiplexer**



The inputs $V_{IN}A$ to $V_{IN}D$ are multiplexed together at the sequence rate and outputted on the commoned output pins.

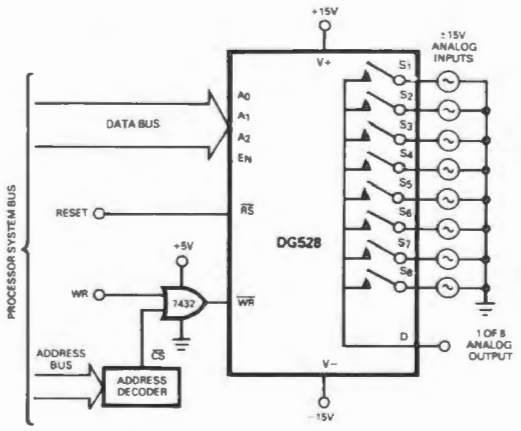
Applications using DG528 and DG508

Figure 10 **A one from eight data selector**



This selector can be used to select specific inputs for various data processing circuits etc.

Figure 11 **Microprocessor interface using DG528**



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RS data

Alphanumeric displays

The RS1414 and 2416 are 4-digit alphanumeric **display modules complete with built-in CMOS** driving circuitry. The on-board integrated circuit contains an ASC II decoder, multiplexer, memory and LED driver. Inputs are TTL compatible. Each digit consists of 16 bar-segments plus a decimal point segment for enhanced punctuation. A single 5V supply is the only power required by the modules. The devices are end-stackable enabling a display system to be built using any number of units, since each character in any device can be addressed independently and will continue to display the character last written until it is replaced by another.

The 1414 has a character height of 2.84mm and is ideal for hand held and portable instrumentation. The 2416 has a larger character height, 4.06mm, with additional blanking and cursor editing facilities.

Note: These devices are manufactured using C-MOS technology and should not be subjected to excessive levels of static charge in storage, handling or use, otherwise device failure is likely to occur. Please read this data sheet carefully particularly the section dealing with 'System design' and 'Handling' considerations.

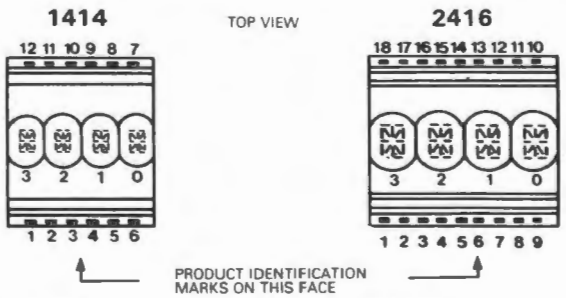
Features

- Wide viewing angles: 1414, ±40°; 2416, ±50°.
- Close vertical row spacing: 20.3mm (0.8in)
- Rugged solid plastic encapsulated packages.
- Fast access time: 450ns (1414); 500ns (2416)
- Built in memory
- Built in character generator
- Built in multiplex and LED drive circuitry
- Direct access to each digit independently and asynchronously
- TTL logic levels, 5V power
- End stackable packages

Absolute maximum ratings

Voltage, (any pin with respect to ground) ——— −0.5 to +6Vd.c.
Operating temp. range ——— −20° to +65°C.
Storage temp. range ——— −20° to +70°C.

Input voltage (any pin) under all conditions ——— $V_{IN} \leq V_{CC}$*
Relative humidity (non condensing) at 65°C —— 85%
Soldering temp ——— 260°C for 3 seconds
*See section on 'System design' considerations.



Pin function

1	D5 Data input
2	D4 Data input
3	$\overline{WR}$ Write
4	A1 Digit select
5	A0 Digit select
6	V_{CC}
7	Gnd
8	D0 Data input (LSB)
9	D1 Data input
10	D2 Data input
11	D3 Data input
12	D6 Data input (MSB)

Pin function

1	$\overline{CE1}$ Chip enable
2	$\overline{CE2}$ Chip enable
3	$\overline{CLR}$ Clear
4	CUE Cursor enable
5	$\overline{CU}$ Cursor select
6	$\overline{WR}$ Write
7	A1 Digit select
8	A0 Digit select
9	V_{CC}
10	Gnd
11	D0 Data input (LSB)
12	D1 Data input
13	D2 Data input
14	D3 Data input
15	D6 Data input (MSB)
16	D5 Data input
17	D4 Data input
18	$\overline{BL}$ Display blank

2.84mm CHARACTERS ACTUAL SIZE:
ALPHANUMERIC

4.06mm CHARACTERS ACTUAL SIZE:
ALPHANUMERIC

Electrical and optical characteristics at 25°C

	Parameter	Conditions	Units	1414			2416		
				min	typ.	max.	min	typ.	max.
V_{CC}	Supply Voltage		V	4.5	5.0	5.5	4.5	5.0	5.5
I_{CC}	Supply Current	All digits on (10 segs/dig.) V_{CC} = 5V	mA			90			125
		Display blank V_{in} = 0, V_{CC} = 5V, $\overline{WR}$ = 5V	mA		1.5	2.7		1.8	3.7
		Cursor (60 sec. max duration)	mA						140
V_{IL}	Input Voltage – Low (any input)	V_{CC} = 5V	V			0.8			
V_{IH}	Input Voltage – High (any input)	V_{CC} = 5V	V	3.0		*	3.0		*
I_{IL}	Input Current – Low (any input)	V_{IN} = 0.8V, V_{CC} = 5V	μA			160			160
	Luminous Intensity	8 segments at 5V	mcd		0.5			0.5	
λpk	Spectral peak wavelength		nm		660			660	
θ	Off axis viewing angle	See note 1.	degrees		±40°			±50°	

NOTE1: "Off Axis Viewing Angle" is here defined as: "The minimum angle in any direction from the normal to the display surface at which part any part of any segment in the display is not visible".

*See Absolute Maximum Ratings

WARNING! ESD SENSITIVE DEVICE

Caution: ESD (Electro-Static-Discharge) sensitive device. This CMOS device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that all input voltages be constrained to the range $V- \leq V_{in} \leq V+$, **particularly during power up conditions.**
Unused inputs must be tied to an appropriate logic voltage level (either V+ or V–).

Figure 1: **Dimensional details**

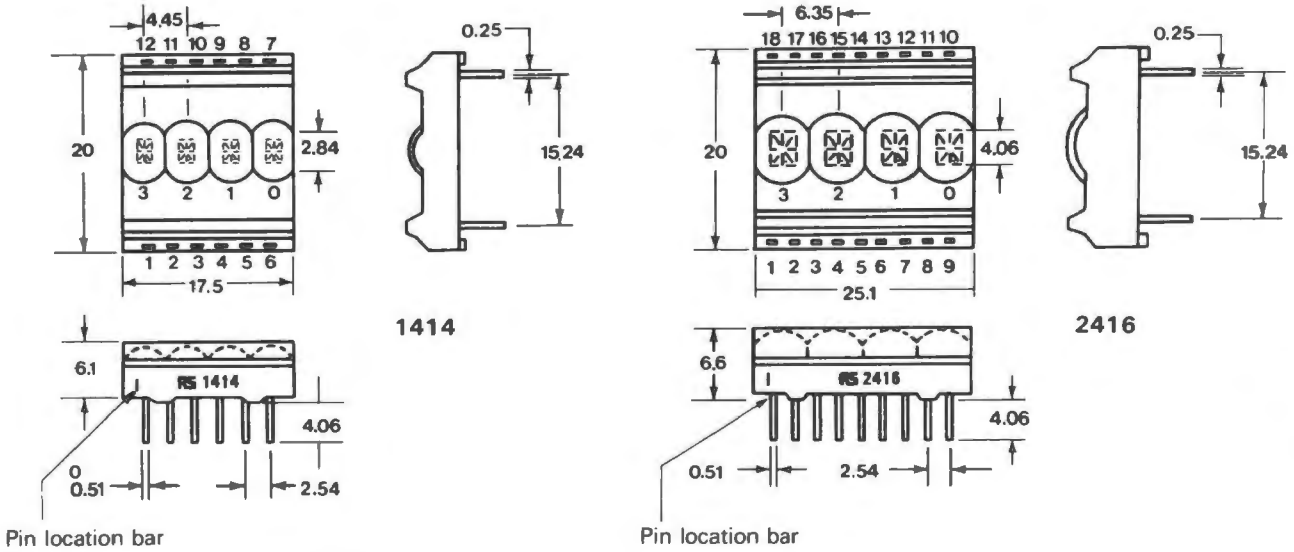


Figure 2: **Block diagram**

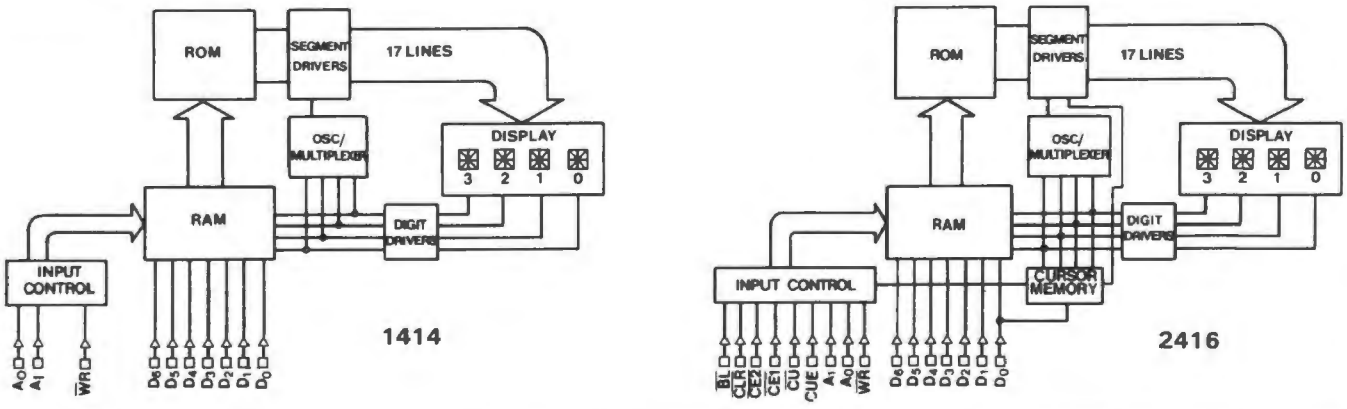
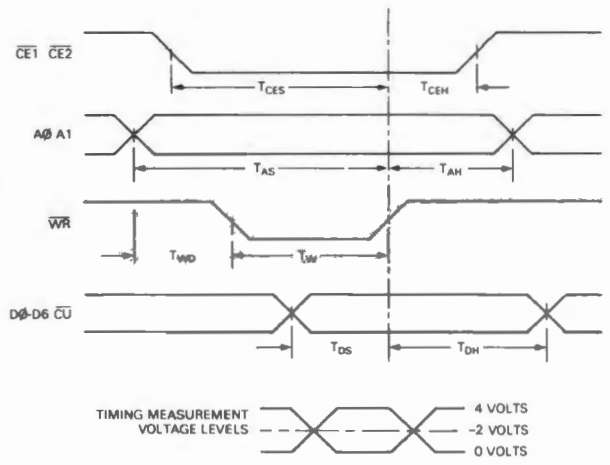


Table 1: **Timing characteristic at 25°C**

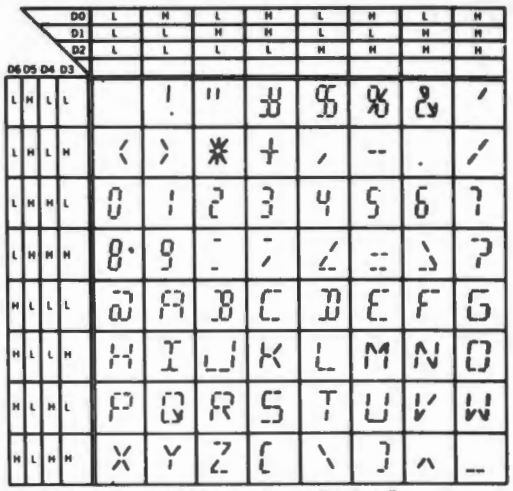
	Parameter	Device 1414	Device 2416	Units
t_W	Write Pulse	325	300	ns
t_{WD}	Write Delay	75	150	ns
t_{DS}	Data Set-up Time	250	250	ns
t_{DH}	Data Hold Time	50	50	ns
t_{AS}	Address Set-up Time	400	450	ns
t_{AH}	Address Hold Time	50	50	ns
t_{CLR}	Clear Time (see text)	-	15	ms
t_{CES}	Chip enable set up	-	450	ns
t_{CEH}	Chip enable hold	-	50	ns

Figure 3: **Timing characteristics/write cycle waveforms**



Note: $\overline{CE1}$, $\overline{CE2}$ waveform refers to 2416 only.

Figure 4: **Character set**



ALL OTHER INPUT CODES DISPLAY "BLANK"

Figure 5: **Digital address table**

A_1	$A\phi$	Digit
L	L	ϕ (Right)
L	H	1
H	L	2
H	H	3 (Left)

Electrical and mechanical description

General

The internal electronics on the RS intelligent displays eliminate all the traditional difficulties of using multi-digit light emitting displays (segment decoding, drivers and multiplexing). The intelligent display also provides internal memory for the four digits. This approach allows the user to asynchronously address one of four digits, and load new data without regard to the LED multiplex timing.

Figure 2 gives the block diagrams of the 1414 and 2416 displays. The units consist of four 17 segment monolithic LED die and a single CMOS integrated circuit chip. The LED die are magnified to a height of 2.84mm (1414) and 4.06mm (2416) by built-in lenses. The IC chip contains 17 segment drivers, four digit drivers, 64 character ROM, four word × 7 bit Random Access Memory, oscillator for multiplexing, multiplex counter/decoder, address decoder, and Miscellaneous Control logic. In addition, the 2416 incorporates a cursor memory.

Packaging

Packaging consists of a plastic lens which also serves as an "encapsulation shell" since it covers five of the six "faces". The assembled and tested substrate (ceramic or "PTF" multilayer) is placed within the shell and the entire assembly is then filled with a water-clear IC grade epoxy.

This yields a very rugged part which is quite impervious to moisture, shock and vibration. Although not "hermetic", the device will easily withstand total immersion in water/detergent solutions. Note: solvents containing alcohol should not be used.

Electrical inputs 1414 and 2416

V_{CC} Positive supply + 5 volts

Gnd Ground

D_0-D_6 Data lines
The seven data input lines are designed to accept the first 64 ASC11 characters. See Figure 4 for character set. (The 2416 interprets all undefined codes as blank.)

A_0, A_1 Address lines
The address determines the digit position to which the data will be written. Address order is right to left for positive-true logic.

$\overline{WR}$ Write (active low)
Data and address to be loaded must be present and stable before and after the trailing edge of write (see Figure 3 for timing information).

In addition, the 2416 features:

$\overline{CE1}$, $\overline{CE2}$ Chip enable (active low)
This determines which device in an array will actually accept data. When either or both chip enable is in the high state, all inputs are inhibited.

$\overline{CLR}$ Clear (active low)
When held low for 15ms the data RAM will be cleared.

CUE Cursor enable. Activates cursor function. Cursor will not be displayed regardless of cursor memory contents when CUE is low.

$\overline{CU}$ Cursor select (active low)
This input must be held high to store data in data memory and low to store data into the cursor memory.

$\overline{BL}$ Display blank (active low)
Blanking the entire display may be accomplished by holding the BL input low. This is not a stored function, however. When BL is released, the stored characters are again displayed.

Operation

Multiplexed display systems sequentially read and display data from a memory device. In synchronous systems, control circuitry must compare the location of data to be read to the location or position of new data to be stored or displayed, i.e. synchronize before a write can be done. This can be slow and cumbersome.

Data entry in "intelligent display" is asynchronous and may be done in any random order. Loading data is similar to writing into a RAM. Each digit has its own memory location and will display until replaced by another code.

The waveforms of Figure 3 demonstrate the relationships of the signals required to generate a write cycle. As can be seen from the waveforms, all signals are referenced from the rising or trailing edge of wire.

Data loading

Loading data into the displays is straightforward. The desired data code (D_0-D_6) and digit address (A_0, A_1) are presented in parallel and held stable during a 'write' cycle. Data entry may be asynchronous and random (Digit 0 is defined as right hand digit with $A_1 = A_0 = 0$). In the case of the 2416, setting the chip enables $\overline{CE1}$, $\overline{CE2}$ to their true state will enable data loading.

System interconnection

System interconnection is also straightforward. The least significant two address bits (A_0A_1) are normally connected to the like named inputs of all displays in the system. Data lines are connected to all displays directly and in parallel as is the write line (WR) for the 2416 which will then behave as a write only memory. For multiple 1414 systems an external 'one of N' decoder chip is usually used and the 'write' pulse connected to the enable of the decoder (see Figure 6). A 3-to-8 line decoder multiplexer (74138) or a 4-to-16 line decoder/ multiplexer (74154) are possible choices. All higher-order address bits (above A_1) become inputs to the decoder. For multiple 2416 systems the two chip enables $\overline{CE1}$ and $\overline{CE2}$ allow four 2416's (16 characters) to be easily interconnected without a decoder (see Figure 7). Alternatively, 'one of N' decoder i.c.'s can be used to extend the address for larger displays.

Figure 6: **Typical interconnection for 32 digit system**

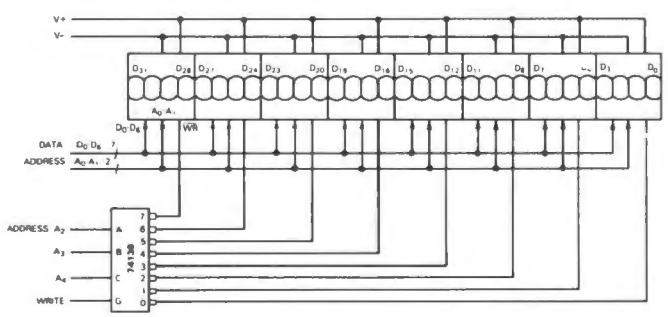
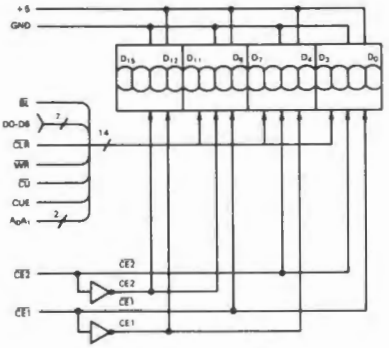


Figure 7: **Typical interconnection for 16 digit system**



Clear memory (2416 only)
Clearing of the entire internal four-digit memory may be accomplished by holding the clear line $\overline{CLR}$ low for one complete internal display multiplex cycle, 15ms minimum; less time may leave some data uncleared. $\overline{CLR}$ does not clear the cursor memory.

Display blanking (2416 only)
Blanking the display may be accomplished by loading a blank, or space into each digit of the display or by using the $\overline{BL}$ display blank input. Setting the $\overline{BL}$ input low does not affect the contents of either data or cursor memory. A flashing display can be realized by pulsing $\overline{BL}$.

Cursor (2416 only)
The cursor function causes all segments of a digit position to illuminate. The cursor is *not* a character, however, and upon removal the previously displayed character will re-appear. A cursor should not be lit for more than 60 seconds due to the limit on localised power dissipation.

$\overline{CU}$, cursor select, controls the writing of signals into the cursor memory.

CUE, cursor enable, determines the choice of display of ASC11 characters or cursor(s).

Setting the chip enables $\overline{CE1}$, $\overline{CE2}$ and cursor select $\overline{CU}$ to their true state will enable cursor loading. A write $\overline{WR}$ pulse will now store or remove a cursor into the digit location addressed by A_0, A_1;
as defined in data entry. A cursor will be stored if DO = 1; and will be removed if DO = 0. Cursor will not be cleared by the $\overline{CLR}$ signal. The cursor $\overline{CU}$, pulse width should not be less than the write $\overline{WR}$ pulse or erroneous data may appear in the display.

For those users not requiring the cursor, the cursor enable signal CUE may be tied low to disable display of the cursor function. A flashing cursor can be realized by simply pulsing CUE. If cursor has been loaded to any or all positions in the display, then CUE will control whether the cursor(s) or the characters appear. CUE does not affect the contents of cursor memory.

A "display test" or "lamp test" function can be realized by simply storing a cursor into all digits. Because of the random state of the cursor RAM after power up, if the cursor function is to be used, it will be necessary to clear cursors initially to ensure that all cursor memories contain its zero state.

Data Loading Tables
The following tables illustrate the operation of the above control functions. They are not 'truth tables' in that any one horizontal line is dependent on the preceding line. This is true of the 2416 cursor loading i.e. it is dependent on the preceding loading data lines.

Table 2: **1414 Loading data**

$\overline{WR}$	Address A_1	Address A_0	Data Input D6	D5	D4	D3	D2	D1	D0	Digit 3	Digit 2	Digit 1	Digit 0
H	X	X	X	X	X	X	X	X	X	No Change	No Change	No Change	No Change
L	L	L	H	L	L	L	L	L	H	No Change	No Change	No Change	A
L	L	H	H	L	L	L	L	H	L	No Change	No Change	B	A
L	H	L	H	L	L	L	L	H	H	No Change	C	B	A
L	H	H	H	L	L	L	H	L	L	D	C	B	A
L	L	L	H	L	L	L	H	L	H	D	C	B	E
L	H	L	H	L	L	H	L	H	H	D	K	B	E
L	–	–	–	–	–	–	–	–	–	See Character Set, Figure 4			

X = Don't Care

Table 3: **2416 loading data**

$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A_1	A_0	D6	D5	D4	D3	D2	D1	D0	Digit 3	Digit 2	Digit 1	Digit 0
L	X	X	X	X	H	H	X	X	X	X	X	X	X	X	X	Blank			
H	H	X	L	X	X	H	X	X	X	X	X	X	X	X	X	Previous display			
H	X	H	L	X	X	H	X	X	X	X	X	X	X	X	X	NC	NC	NC	NC
H	X	X	L	X	H	H	X	X	X	X	X	X	X	X	X	NC	NC	NC	NC
H	L	L	L	H	L	H	L	L	H	L	L	L	L	L	H	NC	NC	NC	A
H	L	L	L	H	L	H	L	H	H	L	L	L	L	H	L	NC	NC	B	A
H	L	L	L	H	L	H	H	L	H	L	L	L	L	H	H	NC	C	B	A
H	L	L	L	H	L	H	H	H	H	L	L	L	H	L	L	D	C	B	A
H	L	L	L	H	L	H	L	L	H	L	L	L	H	L	H	D	C	B	E
H	L	L	L	H	L	H	H	L	H	L	L	H	L	H	H	D	K	B	E
H	L	L	L	H	L	H	-	-	-	-	-	-	-	-	-	See character set Figure 4			

Loading Cursor

H	L	L	L	H	L	H	X	X	X	X	X	X	X	X	X	Normal Data Entry			
H	L	L	H	X	H	H	X	X	X	X	X	X	X	X	X	Enable Previous Stored Cursors			
H	L	L	H	L	L	H	L	L	X	X	X	X	X	X	H	NC	NC	NC	▩
H	L	L	H	L	L	H	L	H	X	X	X	X	X	X	H	NC	NC	▩	▩
H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	H	NC	▩	▩	▩
H	L	L	H	L	L	H	H	H	X	X	X	X	X	X	H	▩	▩	▩	▩
H	L	L	L	X	H	H	X	X	X	X	X	X	X	X	X	D	K	B	E
H	L	L	L	L	L	H	L	L	X	X	X	X	X	X	L	D	K	B	E
H	L	L	H	X	H	H	X	X	X	X	X	X	X	X	X	▩	▩	▩	E

X = Don't Care
NC = No change from previously displayed characters

System design and construction

System design considerations

The practical circuit design (i.e. design of PCB, etc.) should be such that the voltage to any input must never exceed the power supply inputs (i.e. $Gnd < V_{in} < V_{cc}$). If these conditions are not met, then malfunction or at worst, device destruction can occur. The most common cause of this condition is circuit noise due to noise on the input leads and transient power supply changes.

Good circuit layout The principles of good circuit layout are those for all logic circuitry, but the tolerance of MOS circuitry for deviations is much less than that of bipolar logic. The most important principle is to keep the lead length from the output of one device to the input of another as short as possible. This is to reduce the coupling effect between input signals.

Buffering The second most common deviation from good design practice is the use of parallel tracking. Avoid PCB design which allow an interconnection track to run parallel to another. This is particularly true if one of the tracks is a power bus when the fluctuations of power supply current can cause inductively coupled changes in the input track. Possibly the worst example of parallel tracking is the ribbon cable: it is physically neat and convenient, but can be electrically destructive for the MOS circuits.

It is often necessary, because of the very nature of the intelligent display, to use ribbon cable from the CPU board to the display assembly board. In those circumstances for cables over 30 cm (12 inches), use a TTL buffer for each used input. This is especially true for noisy systems which have motors, relays etc. The buffers must be on the display end of the cable, thus maintaining a minimum distance between their outputs and the display inputs. Long cables can be a poor transmission line for speed pulses. Line drivers, line receivers, or schmidt trigger gates may be required to shape pulses.

Voltage transients It has become common practice to provide 0.01 μF bypass capacitors liberally in digital systems. For intelligent displays, the emphasis is on adequate decoupling. Like other CMOS circuitry, the intelligent display controller chip has very low power consumption and the usual 0.01 μF would be adequate were it not for the LEDs. The module itself can, in some conditions, use up to 100 mA (multiplexed). In order to prevent power supply transients, capacitors with low inductance and high capacitance at high frequencies are required. This suggests a solid tantalum or ceramic disc for high frequency bypass. For larger displays, distribute the bypass capacitors evenly, keeping capacitors as close to the power pins as possible. Do not rely on existing on-board decoupling: use a 10 μF and 0.01 μF for every 3 or 4 intelligent displays to decouple the displays themselves, at the displays.

Functional limitations Several parameters in this data sheet which may affect your design will be emphasized again. While these may not be destructive, they may affect reliability and/or functional operation.

1. The length of time all cursors may be lit should be 1 minute maximum.
2. The timing parameters for 25°C will increase with increased temperature.
3. The timing parameters will increase with increased V_{CC}.

Handling considerations

Handling The static voltages generated by friction with modern synthetic materials (i.e. carpets, clothing, device carriers etc.) are often measured in thousands of volts. Although there is usually little energy in these static charges to MOS circuitry that energy is sufficient to cause destruction if applied between circuit inputs. Input protection diodes can minimize the vulnerability of the circuits, but there is a limit to their protection capabilities. Under certain conditions, static charges can exceed that limit. The most effective protection is to avoid the generation of static charges. When they are inevitable, the charges must be prevented from coming in contact with the device pins.

1. Avoid touching the pins; handle the body only.
2. Keep the devices in anti-static tubes or conductive material when transporting.
3. Use conductive and grounded working area (conductive flooring, conductive work benches, individual wrist straps etc.).

Soldering Because of the plastic housing of the intelligent displays, it is necessary to control the solder temperature, soldering time and solder distance. A maximum of 260°C for 3 seconds at a distance of greater than 1/16 inch is required. An additional requirement for wave soldering is the intelligent display package cannot exceed 70°C.

Cleaning The cleaning process for the intelligent displays is crucial to maintain the optical performance of the plastic housing. The solvent that *cannot* be used on the intelligent display product is alcohol. Alcohol will attack the lens material causing cracking, crazing and destruction of the clear optical properties of the lens.

In the suggested category are the chlorinated hydrocarbons (Acetone, 1.1.1. Trichloroethane, etc.) or Trichlorotrifluoroethane or warm deionised water. One note of caution: do not specify a solvent without first finding the chemical composition. Some manufacturers use some form of alcohol as an additive, so beware.

Interfacing the 1414 and 2416

The general and straightforward interface circuits shown in Figures 6 and 7 can easily interface to microprocessor systems or any other systems which can provide the seven data lines, appropriate address and control lines.

The 1414 does not have a chip enable input. Therefore, each 1414 in a system requires its write pulse to be gated with appropriate address signals. Figure 8a shows the use of a 74154 decoder (4 line to 16 line) for up to a 64 character display. Using the G1 input for display select (address select in a memory mapped system) and the G2 input to gate the write signal. Another approach (Figure 8b and 8c), which minimises logic for a 16 or 32 digit display takes advantage of decoding scheme of the 7442 decoder.

Figure 8: **Gating the write impulse**

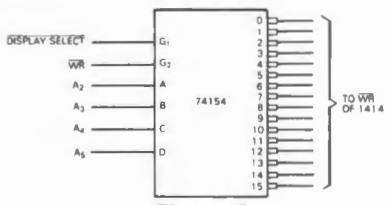


Figure 8a

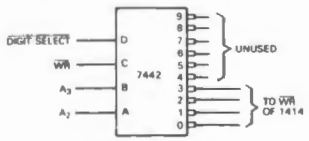


Figure 8b

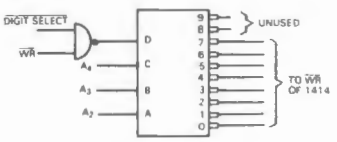


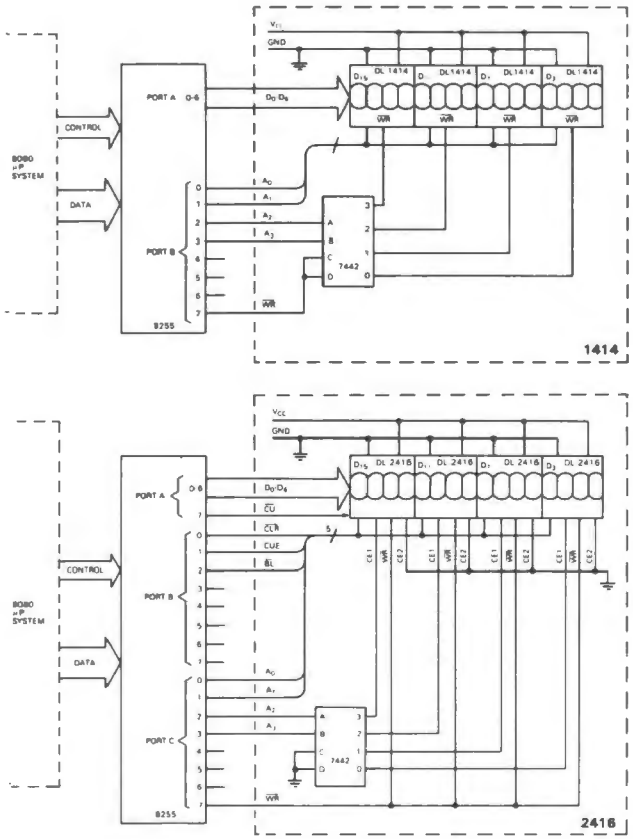
Figure 8c

RS data

Parallel I/O

The parallel I/O device of a microprocessor can easily be connected to either of the circuits in Figure 9. One eight bit output port can provide the seven input data bits also the cursor $\overline{CU}$ required by the 2416. Another eight bit output port can contain the address and control signals required by either display and the chip enable information necessary for the 2416.

Figure 9: **16 digit parallel I/O system**



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RS data

Servo control i.c. RS ZN409

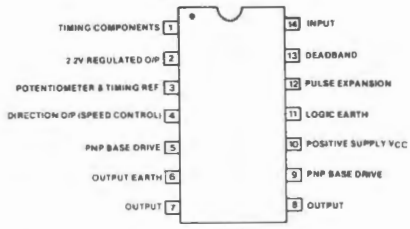
Stock number 304-813

The RS ZN409 is a precision monolithic integrated circuit designed particularly for pulse-width position servo mechanisms used in many types of control applications. The low number of components required with the device, together with its reduced length and low power consumption, make this integrated circuit ideal for use in compact servo applications where space, weight and battery life are at a premium. The amplifier will operate over a wide range of repetition rates and pulse widths and is therefore suitable for the majority of systems. The RS ZN409 can also be used in motor speed control circuits.

Features

- Low external component count
- Low quiescent current (7mA typical at 4.8V)
- Excellent voltage and temperature stability
- High output drive capability
- Consistent and repeatable performance
- Precision internal voltage stabilisation
- Time shared error pulse expansion
- Balanced deadband control
- Schmitt trigger input shaping
- Reversing relay output (D.C. motor speed control)

PIN CONNECTIONS



Absolute maximum ratings

Supply voltage ..... 6.5 Volts
Package dissipation ..... 300 Milliwatts
Operating temperature range ..... –20°C to +65°C
Storage temperature range ..... –65°C to 150°C

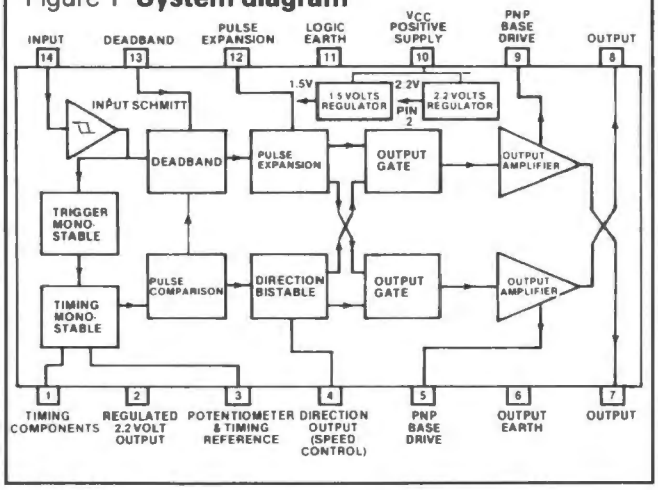
Characteristics

V_{CC} = 5V. At 25°C ambient temperature unless otherwise stated.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Input threshold (lower)	1.15	1.25	1.35	V	Pin 14
Input threshold (upper)	1.4	1.5	1.6	V	Pin 14
Ratio upper/lower threshold	1.1	1.2	1.3		–10 to +65°C
Input resistance	20	27	35	kΩ	$V_{in} \leq 2V$ (Pin 14)
Input current	350	500	650	μA	$V_{in} \geq 2V$ (Pin 14)
Regulator voltage	2.1	2.2	2.3	V	–10 to +65°C, 1.3mA load current
Regulator supply voltage rejection ratio	200	300	–		V_{CC} = 3.5 to 6.5V $RSRR = \frac{dV_{in}}{dV_{out}}$
Monostable linearity for ±45° pot rotation	–	3.5	4.0	%	R_p = 1.5kΩ R_1 = 12kΩ
Monostable period temperature coefficient	–	±0.01	–	%/°C	Excluding R_T, C_T. R_p = 1.5kΩ, R_1 = 12kΩ (potentiometer slider set mid-way)
Output Schmitt deadband	±1	±1.5	±3	μs	C_E = 0.47μF
Minimum output pulse	2.5	3.5	4.5	ms	C_E = 0.47μF, R_E = 180kΩ
Error pulse for full drive	70	100	130	μs	15 ms repetition rate C_E = 0.47μF, R_E = 180kΩ
Total deadband	±3.5	±5	±6.5	μs	C_D = 1000pF
P.N.P. drive	40 35	55 50	70 65	mA mA	T = 25°C T = –10°C
Output saturation voltage	–	300	400	mV	I_L = 400mA
Direction bistable output	2	2.8	3.6	mA	V_{CC} = 5V max.
Supply voltage range	3.5	5	6.5	V	
Supply current	4.6	6.7	10	mA	Quiescent
Total external current from regulator	1.3	–	–	mA	V_{CC} = 3.5V
Peak voltage $V_{C\ EXT}$ (with respect to 2V regulated voltage)	– –	0.7 0.5	– –	V V	T = 25°C T = –10°C

Circuit operation

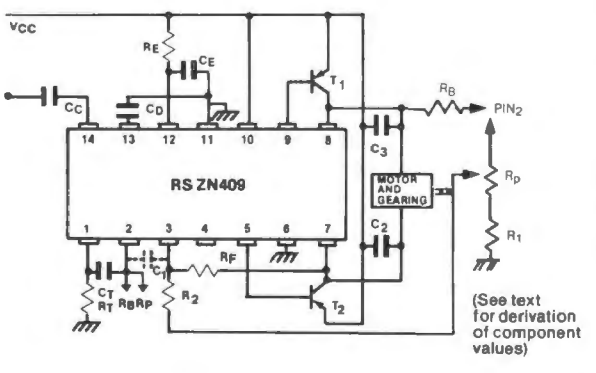
Figure 1 **System diagram**



The system diagram in Fig. 1 illustrates the internal structure of the RS ZN409 servo control I.C.

In the standard servo application the displacement of a potentiometer control varies the pulse width of a timing circuit. The signal produced provides the control input for the servo I.C. The servo shown in Fig. 2 consists of the RS ZN409 integrated circuit, several external components, a power amplifier consisting of two external PNP transistors and two on-chip NPN transistors which form a bridge circuit to drive the d.c. motor. The motor drives a reduction gear box which has a potentiometer attached to the output shaft. The RS precision d.c. servo system components are ideally suited for this application and the 6V motor should be used. This potentiometer in association with R_1 and the timing components C_T and R_T controls the pulse width of the timing monostable. The input pulse is compared with the monostable pulse in a comparison circuit and one output is used to enable the correct phase of an on-chip power amplifier. The other output from the pulse comparison circuit drives the pulse expansion circuit (C_E, R_E) via the deadband circuit (C_D). Thus any difference between the input and monostable pulses is expanded and used to drive the motor in such a direction as to reduce this difference so that the servo takes up a position which corresponds to the position of the control potentiometer.

Figure 2 **Servo system using the RS ZN409**



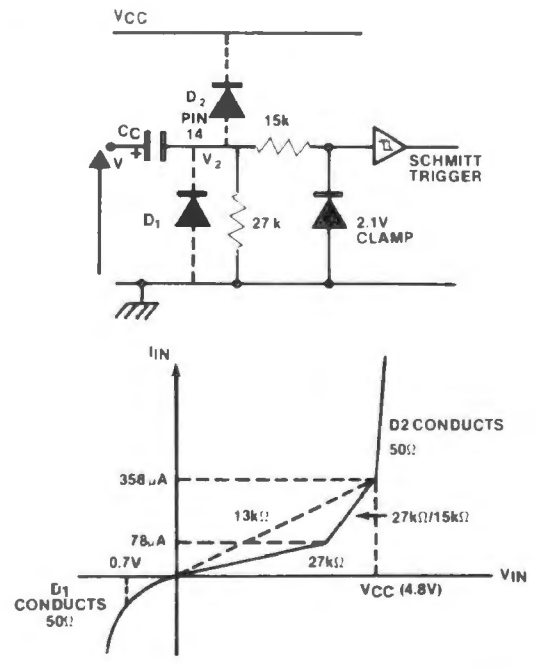
Component function	Circuit reference	Value
Monostable timing components	R_T	100kΩ
	C_T	0.1μF
Potentiometer and timing reference components	Rp	2kΩ
	R_1	6.2kΩ
Pulse expansion	C_E	0.47μF
	R_E	180kΩ
Deadband	C_D	2200pF
Dynamic feedback	R_F	300kΩ
	R_B	300kΩ
	R_2	1.2kΩ
Input coupling	C_C	2.2μF
Motor decoupling	C_2	0.1μF
	C_3	0.1μF
R.F. decoupling (see text)	C_1	0.1μF
Drive transistors	T_1, T_2	BC461

Input circuit

The RS ZN409 operates with positive going input pulses which can be coupled either directly or via a capacitor to pin 14. The advantage of a.c. coupling is that should a fault occur which causes the input signal to become a continuous positive level, the servo will remain in its last quiescent position, whereas with direct coupling the servo output arm will rotate continuously. A nominal 27kΩ on-chip resistor is shunted across the input to provide d.c. restoration of the input signal when a.c. coupling is used. The active input circuit is a Schmitt trigger which allows the servo to operate consistently with slow input edges and supplies the fast edge required by the trigger monostable independent of input edge speed.

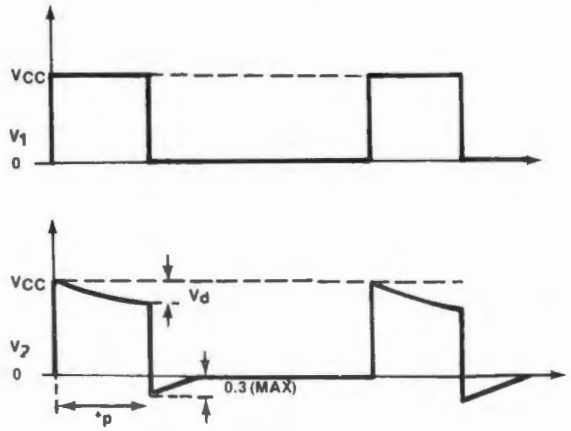
Figure 3

Input circuit **Input characteristics**



The input circuit and its V/I characteristic are shown above. D_1 and D_2 are the parasitic substrate and isolation diodes associated with the input resistors. It is advisable that the pulse input amplitude should not fall below 0V nor exceed the supply voltage V_{CC} in order to prevent these diodes from conducting, although a small amount of conduction will not cause the circuit to malfunction. When a.c. coupling is used the value of C_C should be chosen to give a pulse droop not exceeding 0.3 volts.

Figure 4 **Input waveforms**



Assuming that the input signal swings between 0V and V_{CC} and taking the input chord resistance R_{IN} of 13kΩ the droop for a pulse of duration msec will be:

$$V_d = \frac{V_{CC} t_p}{C_C . R_{IN}} \text{ volts} \quad \begin{matrix} t_p \text{ (msec)} \\ C_C \text{ (}\mu\text{F)} \\ R_{IN} \text{ (k}\Omega\text{)} \end{matrix}$$

For a nominal pulse width of 1.5msec and V_d equal to 0.3 volts the required minimum value of C_C can be found to be 1.85μF and a nominal value of 2.2μF is chosen. (Nearest preferred value).

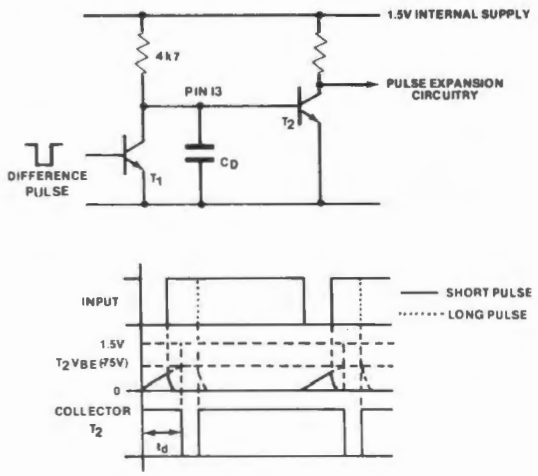
$$C_C = \frac{4.8 \times 1.5}{0.3 \times 13} = 1.85\mu F$$

If it is required to operate the servo with reduced input pulse amplitude the input pulse should exceed the upper Schmitt threshold voltage of 1.5 volts by a reasonable margin and a minimum input pulse amplitude of 2.4 volts is recommended.

Deadband circuit

The function of the deadband circuit is to provide a small range of output shaft positions about the quiescent position where the difference pulse does not drive the motor. This is necessary to eliminate hunting around the quiescent position caused by servo inertia and overshoot. The minimum deadband required is also a function of the pulse expansion characteristics and dynamic feedback component values.

Figure 5 **Deadband circuit and waveforms**



When the difference pulse is applied T_1 turns off and the base of T_2 rises on an exponential waveform with a time constant of 4.7 kΩ × C_D. If the difference pulse is small the potential reached on the base of T_2 is insufficient to turn T_2 on and no output results.

The pulse expansion circuit has a built in deadband of 1.5μsec with C_E = 0.47μF and this must be added to the deadband caused by C_D to obtain the total T_d.

$$T_d = 1.5 + t_d \mu\text{sec}$$
$$\text{and } t_d = 3.3\, C_D \mu\text{sec } (C_D \text{ in nF})$$
(Taking V_1 = 1.5 volts and V_{be} = 0.75 volts)
Thus with C_D equal to 2200pF (2n2)
t_d = 7.26μsec and T_d = 8.76μsec.

The mechanical deadband Ød depends on the chosen sensitivity S_1 of the servo and in a typical application at ±500μsec input pulse variation causes ±50° rotation, i.e. S_1 = 10μsec per degree.

Thus $\text{Ød} = \frac{2.T_d}{S_1}$ degrees (T_d in μsec. S_1 in μsec per degree).

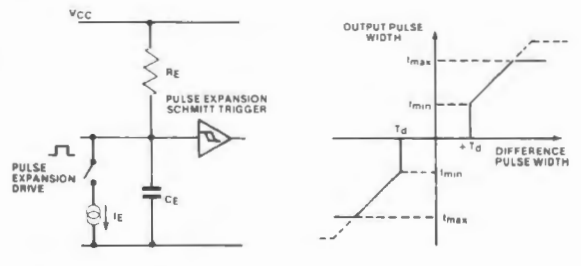
Thus a value for T_d of 8.76μsec provides a mechanical deadband Ød of 1.8°.

And generally:

$$\text{Ød} = \frac{3 + 6.6\, C_D}{S_1} \text{ degrees} \quad \begin{matrix} C_D \text{ in nF.} \\ S_1 \text{ in μsec per degree.} \end{matrix}$$

Pulse expansion

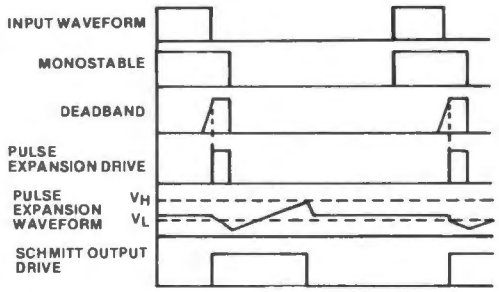
Figure 6
Pulse expansion circuit and characteristics



A schematic of the pulse expansion circuit is shown in Fig. 6. In the quiescent state with no drive the Schmitt trigger input is biased via R_E and takes up a level just above the lower threshold V_L.

A drive pulse causes a current I_E to be switched on for the duration of the pulse and this discharges C_E linearly with time. Thus, at the end of the pulse the voltage on C_E depends on the duration of the pulse. If the pulse is narrow and just causes the potential on C_E to fall to V_L the Schmitt trigger will switch to the upper threshold V_H and at the end of the drive pulse C_E will start to charge to V_H with a time constant C_ER_E. When the potential on C_E reaches V_H the Schmitt will switch to V_L and C_E will discharge to the quiescent level. The output drive is taken from the Schmitt output.

Figure 7 **Pulse expansion timing diagram**



D.C. motors need a certain amount of drive to overcome static friction and the minimum output pulse obtained from this form of pulse expansion characteristic is chosen to ensure that the motor will rotate when driven.

The value of t_{min} is determined by the Schmitt trigger hysteresis and the exponential waveform on C_E because V_H is small the following linear relationship is sufficiently accurate.

$$V_H = \frac{(V_{CC}-V_L)}{C_ER_E} \times t_{min}$$

For nominal operation $V_{CC} = 4.8V$; $V_L = 1.5V$; $V_H = 0.12V$ and:

$$t_{min} \simeq \frac{C_ER_E}{30}\ \text{msec} \begin{cases} C_E \text{ in } \mu F \\ R_E \text{ in } k\mu \end{cases}$$

and for $C_E = 0.47\mu F$ and $R_E = 180k\Omega$, $t_{min} = 3.5$msec.

It can be seen from the simple equation that t_{min} is dependent on V_{CC}, and t_{min} will increase with reducing V_{CC}. This variation is put to good use to maintain the initial motor drive, $V_{CC} \times t_{min}$ reasonably constant over the operating voltage range of 3.5 to 6.5 volts.

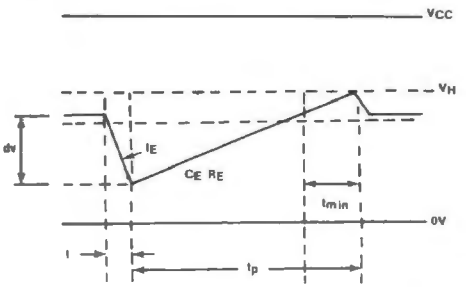
When the pulse expansion drive is increased above the minimum value the output pulse increases from t_{min} almost linearly until full pulse expansion is reached, i.e. when the output pulse width equals the input pulse repetition rate. The pulse expansion will be almost linear provided that the current source I_E does not saturate, i.e. provided that C_E is not discharged to almost zero volts. Ideally the current source should saturate when full motor drive is obtained but due to component tolerances it is usual to allow some margin to ensure that full motor drive can be obtained. If a margin is allowed, an extended pulse expansion characteristic results (shown dotted in Fig. 6) and if this is excessive it can lead to the servo exhibiting an underdamped characteristic causing jittering or hunting. Thus for full pulse expansion the voltage on C_E should discharge from its quiescent value of 1.5V to 0.75 volts. Thus with $I_E = 3$mA for the current source:

$$\frac{1.5-0.75}{t_e} = \frac{I_E}{C_E}$$

$$\therefore C_E = 4.\ t_e\ \mu F \quad (t_e \text{ in msec})$$

For $t_e = 0.1$ msec, a value of $0.47\mu F$ was chosen for C_E.

Figure 8 **Pulse expansion waveform**



If t_p is the maximum motor drive pulse length required, i.e. equal to the input pulse repetition period for full pulse expansion, and the mean value of the potential on C_E is taken as 1.2 volts, then:

$$dv = \frac{(t_p-t_{min})}{C_ER_E} \times (V_{CC}-1.2)$$

And for the discharge period t_e:

$$dv = \frac{I_E\ t_e}{C_E}$$

$$\therefore R_E = \frac{(t_p-t_{min})}{I_E\ t_e} \times (V_{CC}-1.2)$$

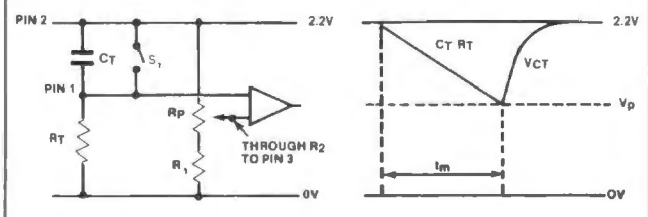
For nominal values of $V_{CC} = 4.8V$ and $I_E = 3$mA

$$R_E = 1.2\ \frac{(t_p-t_{min})}{t_e}\ k\Omega$$

and for $t_p = 20$msec, $t_{min} = 3.5$msec, $t_e = 0.1$msec, $R_E = 180k\Omega$. (Nearest preferred value).

Monostable timing

Figure 9
Monostable timing circuit and waveform



The leading edge of the input waveform triggers the timing monostable by opening switch S_1. C_T then charges until the differential amplifier detects that the timing waveform potential has fallen to V_p, the potential on the potentiometer wiper and switch S_1 is closed to terminate the timing pulse. Thus the monostable period is determined by the setting of the potentiometer wiper. In the standard

application the servo centre position pulse width is 1.5 msec with a range of ±50° rotation at 10 μsec per degree. Thus the 2.0 msec maximum monostable period t_{mono} (max) corresponds to a potentiometer setting of 200° (for a linear relationship) and since the potentiometer has a total rotation of approximately 270° and the maximum allowable swing on pin 3 is specified as 0.5 volt, the value of C_TR_T can be calculated as follows:

$$\frac{0.5}{t_{mono\ (MAX)}} \simeq \frac{2}{C_TR_T}$$

$$\therefore C_TR_T = 4\,t_{mono\ (max)}$$

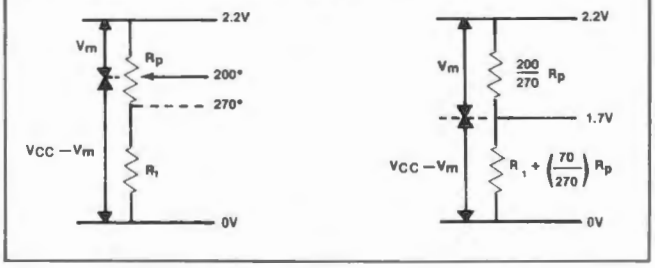
Thus if $t_{mono\ (max)} = 2$ msec, $C_TR_T = 8$msec.

The optimum value of R_T is 100kΩ due to the design of the on-chip monostable circuit giving $C_T = 0.1\mu F$ (nearest preferred value).

$R_T = 100k\Omega \qquad C_T = 0.1\mu F$

The value of R_1 can now be calculated from the actual voltage swing with a potentiometer setting of Øp = 200° and Ømax = 270°.

Figure 10
Potentiometer set at 200°C **Equivalent circuit**



Thus from the equivalent circuit:

$$\frac{Vm}{\frac{200}{270}\ R_p} = \frac{(V_{CC} - V_m)}{R_1 + \frac{70}{270}\ R_p}$$

where V_m is calculated from the actual values of C_T and R_T chosen using the relationship:

$$V_m = \frac{2.0.\ t_{mono\ (max)}}{C_TR_T}$$

since $C_T = 0.1\mu F$ (nearest preferred value) was chosen with $R_T = 100k\Omega$, $V_m = 0.4V$ and hence: $R_1 = 3.1\ R_p$. If $R_p = 2k\Omega$ then $R_1 = 6.2k\Omega$.

Dynamic feedback

Without dynamic feedback in the standard application the inertia of the motor and gearbox causes the servo output shaft to overshoot the set position which results in the servo 'hunting'. If the deadband was widened to stop this effect an unacceptably large deadband would result and the servo would still be underdamped. The dynamic feedback circuit utilises the motor back emf (which is proportional to motor speed) and feeds back a proportion of this signal to the wiper of the potentiometer. The phase of the feedback signal is chosen to modify the potential on the wiper so that the monostable period is dynamically varied to reduce the motor drive as the servo output shaft approaches the set position and the values of the feedback resistors are chosen to achieve optimum setting characteristics.

The value for R_F and R_B of 330kΩ will suit the normal type of servo mechanism, however if the servo is fairly fast this can be decreased to 300 kΩ to minimise any tendency to overshoot. Where the servo is slow R_F and R_B can be increased to 360kΩ or 390kΩ.

RF Decoupling

C_1 (typical value 0.1μF) is only necessary where strong RF fields may affect the operation of the circuit.

Transistors T1 and T2

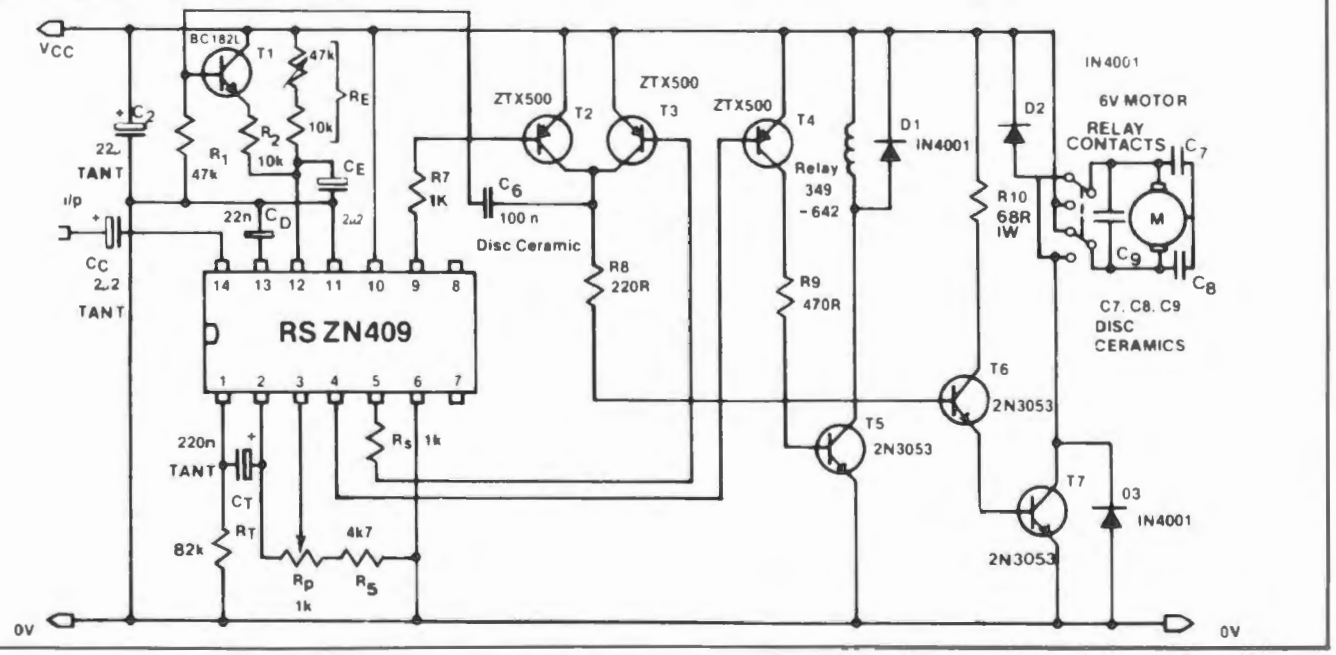
The external PNP transistors are usually selected for a low V_{CE}(sat) to obtain maximum output drive. The recommended type is BC461.

Motor speed control

Introduction

In the motor speed control application the

Figure 11
Proportional motor speed control circuit



RS data

RSZN409 is used as a linear pulse width amplifier. The d.c. motor is driven via a power amplifier with a train of pulses whose mark/space ratio can vary between zero and one to control the motor speed from zero to maximum. The device operates with fixed timing components and a fixed resistor replaces the position feedback potentiometer. The nominal monostable period represents zero motor speed and input pulses less than or greater than nominal drive the motor in the forward and reverse direction respectively. The motor direction is usually controlled by a relay operated from pin 4, the direction output. Pulse expansion components C_E and R_E are chosen to obtain the required relation between control potentiometer and motor speed and it is usual to operate with a much larger deadband than that used in the servo application.

The outputs from pins 9 and 5 of the RSZN409 integrated circuit are combined using two ZTX500 PNP transistors to provide a pulsed output whose mark/space ratio varies from 0 to 1 depending on the deflection of the control potentiometer.

This signal is then used to drive the motor via the power amplifier.

The RSZN409 has additional circuitry which performs the motor reversing function by taking the output from the direction bistable and provides either zero current or approximately 3mA sink current at pin 4, depending on the state of the direction bistable. This current is amplified and used to drive the relay coil (100mA) via the 2N3053 transistor thus controlling the motor direction via the relay changeover contacts.

It is usual to have a relatively wide deadband and C_D = 22nF provides a deadband of about 14% (± 7 degrees).

A 1kΩ potentiometer (R_p) can be used to set up the zero output condition with the control pot in its central position.

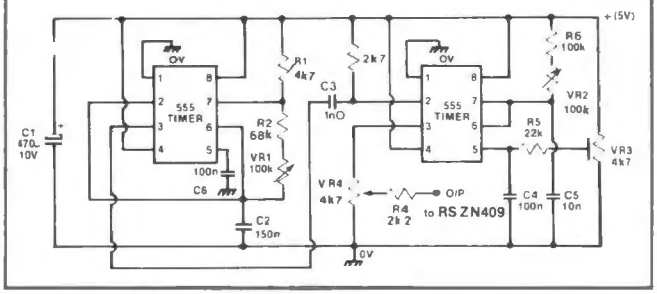
Pulse width generator

A pulse width generator circuit is shown in Figure 12 suitable for driving the RSZN409 in servo or motor speed applications.

The frame rate is generated by the first timer and the frequency is adjusted by VR1 so that the time between pulses is 18mS. VR2 is then used to control the output pulse width over the range 1–2mS. VR3 is set so that the midpoint of VR2 corresponds to an output pulse of 1.5mS.

VR4 can be included should an output amplitude control be required.

Figure 12 **Pulse width generator**



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RS data

General purpose d.c. motors

A range of small d.c. motors with integral gearboxes for reliable yet economic usage in model systems, rotating displays, warning indicators, aerial drives and many other general purpose applications where rotational drive is required.

The motor consists of a permanent magnet stator with a three pole laminated iron rotor. A flat copper commutator has carbon brush contacts with a voltage dependent resistor, disc spark suppressor mounted between commutator and coils. This provides interference suppression and considerably increases brush life.

A steel ring completes the magnetic circuit and also provides a foundation for the plastic housing. Bearings are self-lubricating bronze and both reduction gears and housing are of tough polyacetal resin, which is highly resistant to chemicals and corrosion. Electrical connections are made via two solder tags on the motor body. Figure 1 gives motor dimensions.

Features

- Combined motor-gearbox
- Integral interference suppressor
- Tough, corrosion-resistant housing
- Economic and versatile in application

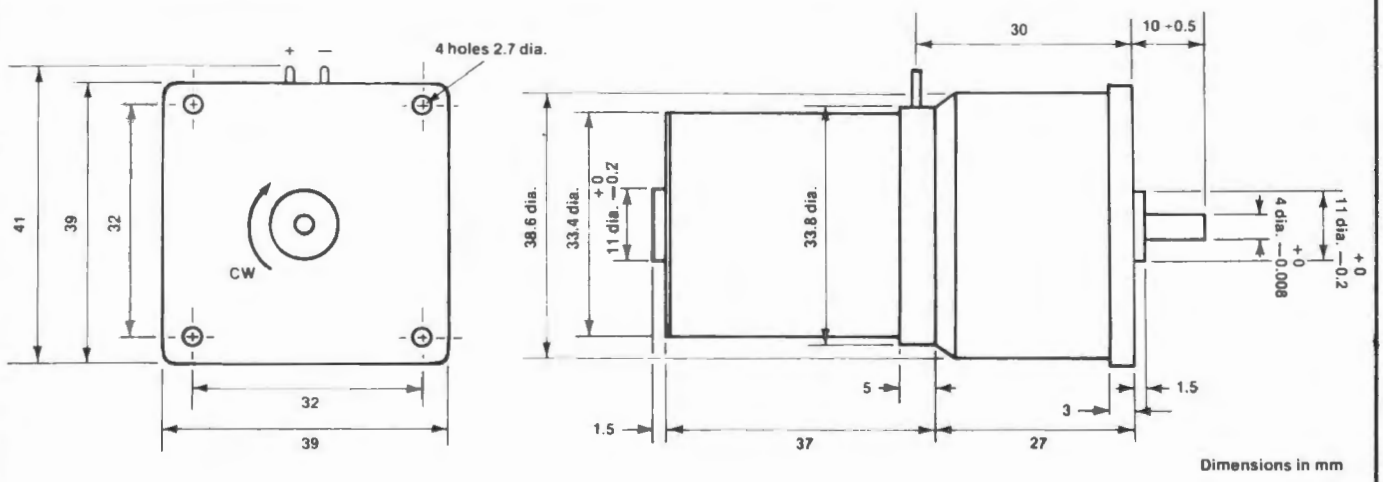
Quick reference table

RS stock no.	336-315	336-321	336-337	336-343	symbol
nominal supply voltage	12	12	6	6	V d.c.
reduction ratio	50:1	9:1	50:1	9:1	
output speed	60	330	60	330	r.p.m.
output torque	125	25	125	25	mNm

note: 1mNm = Nm x 10^{-3}≙10gcm

Dimensional details

Figure 1



The direction of rotation is given with polarity as shown.

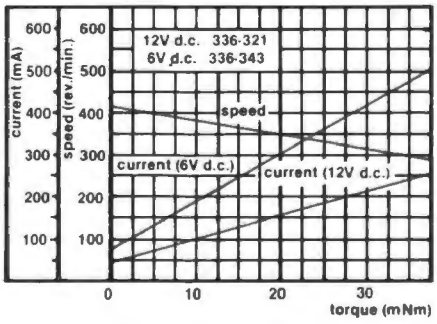
RS data

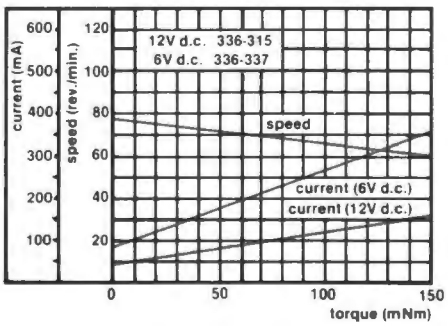
Typical motor characteristics values apply to an ambient temperature of 22±5°C

RS stock no.	336-315	336-321	336-337	336-343	symbol
nominal voltage	12	12	6	6	V d.c.
torque	125	25	125	25	mNm
speed at nominal load	60	330	60	330	r.p.m.
at no load	78	415	78	415	r.p.m.
current at nominal load	185	185	360	360	mA
at no load	45	45	80	80	mA
input power	2.2	2.2	2.1	2.1	W
Ambient temperature range	–20 to +60				°C
maximum axial play	0.5				mm

Limiting conditions					
max. input voltage	18	18	9	9	V d.c.
max. load	150	37.5	150	37.5	mNm
max. radial force on bearings	6	2	6	2	N
max. axial force	6	2	6	2	N

Typical curves





Absolute maximum values should never be exceeded.

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RS data

Precision d.c. motors, gearboxes and servo mounting kit

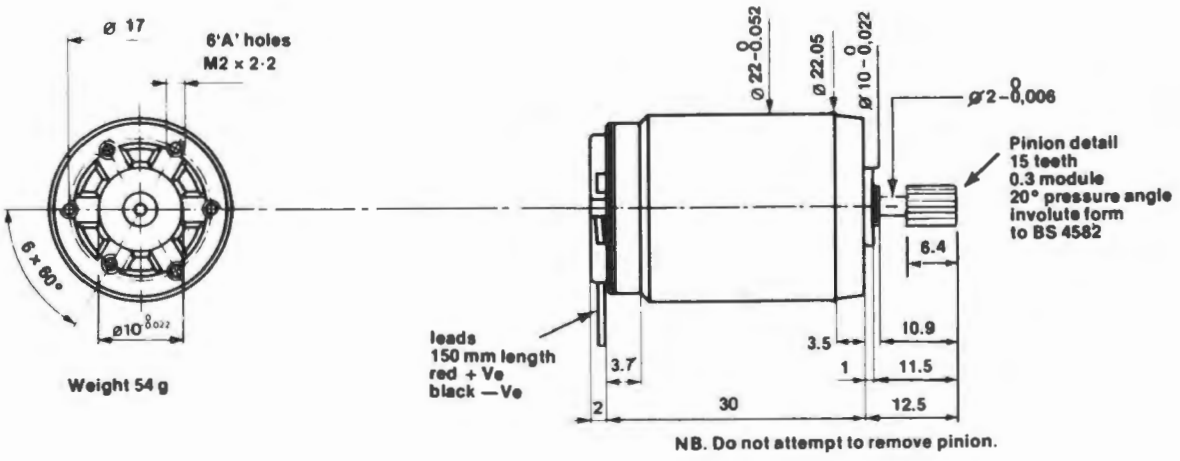
High quality d.c. motors ideally suited for driving a wide range of industrial and laboratory equipment in both open ended and servo controlled modes. They incorporate a self supporting cylindrical rotor coil that is wound in a unique skew fashion and fixed to the central shaft at the commutator end by means of a moulded plastic disc. The ironless rotor (rotates around a central double pole permanent magnet) has a very low inertial mass, which gives a fast and smooth response characteristic of output torque versus speed (see figs. 7 & 8). Because there is no iron in the rotor its angular orientation with the central magnet is unbiased and there will be no inherent 'cogging'. The motor will therefore start, run and stop smoothly in any position.

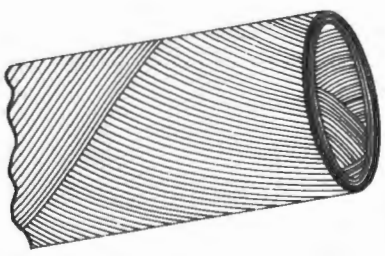
The silver alloy commutator with gold alloy brush contacts present a negligible series resistance to the motor coil which improves overall efficiency and enables the motor to be started at much lower voltages than larger, carbon brush d.c motors. In this instance, low voltage battery operation (perhaps in portable equipment) would be a very appropriate application. The coil and commutator assembly are mounted on self lubricating sintered bronze bearings and housed in a rugged nickel plated steel case. The excellent constructional and material quality of these motors coupled with the advantages described go together to ensure high reliability and maintenance-free operation. Dimensional details are given in fig. 1. Electrical and mechanical characteristics, see page 2.

Features

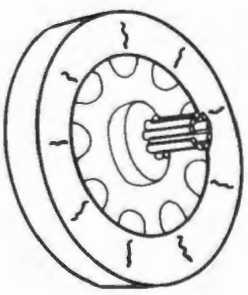
- low inertia ironless rotor
- precious metal commutator and brush contacts
- self lubricating bearings
- non preferred armature position
- low electrical and mechanical losses
- smoothness of torque
- rapid response
- high power to volume ratio

Figure 1.





section of rotor showing skew winding



commutator detail

Typical motor characteristics (T_{amb} = 22°C unless otherwise stated)

No.	Characteristic	Symbol	Motor Stock Number		Tolerance	Units
			336-292	336-309		
1	Input voltage (maximum recommended)	$V_{IN}(max)$	12	6		Volts
2	No-load speed	ω_o	7400	6000	±8%	r.p.m.
3	Stall torque (starting torque)	M_d	88	102		Nm x 10^{-4}
4	Power output at input voltage (max)	$P_{OUT}(max)$	1.7	1.6		Watts
5	Average no-load current	I_0	8	16		mA
6	Back-EMF constant	K_e	1.6	1	±8%	V/10^3 r.p.m.
7	Rotor inductance		0.9	0.4		mH
8	Motor regulation		88.9	60.6		10^3/Nms
9	Terminal resistance	$R_{m(22)}$	20.8	5.7	±8%	Ω
10	Torque constant	K_t	153	97	±8%	Nm x 10^{-4}/A
11	Rotor moment of inertia	J_m	2.1	3.46		kgm² x 10^{-7}
12	Mechanical time constant	τ_m	19	21		ms
13	Thermal time constant (rotor) (stator)		7 550	11 550		s s
14	Thermal resistance (rotor-body) (body-amb)	θrb θba	9 26	9 26		°C/W °C/W
15	Guaranteed starting voltage		0.15	0.1		Volts
16	Working temperature range (ambient)		−30 to +65			°C
17	Maximum armature temperature		100			°C

Mechanical data

18	End play		100 to 150		μm
19	Radial play		5 to 15		μm
20	Max. side load (5mm from bearing)		1.5		N

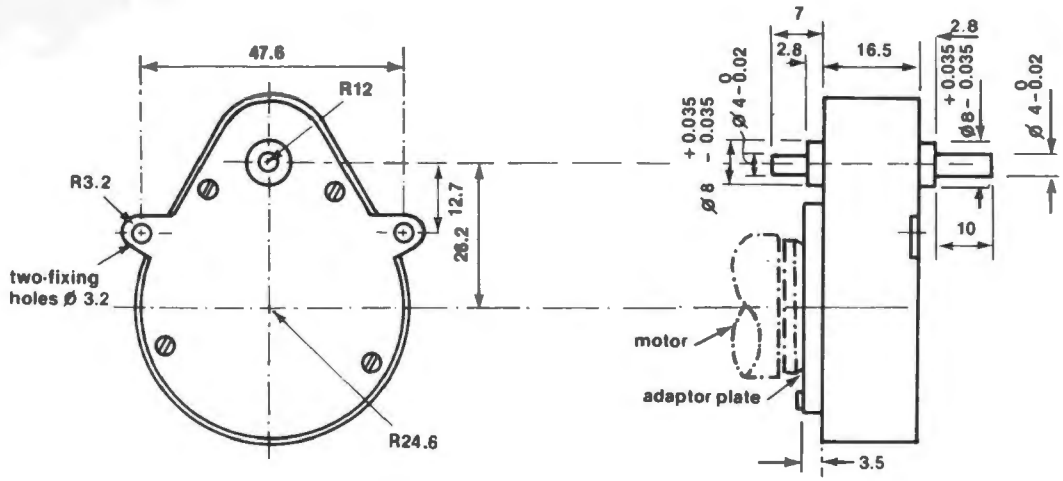
Note. In all cases take into account the heating effect in the motor armature (I^2R losses). The armature temperature should never exceed 100°C.

Definition of characteristics 1 to 15

1. Input voltage (max.). Voltage at which characteristics 2 to 5 are defined. All these values are dependent on supply voltage. (Direction of the motor may be changed by reversing the supply voltage).
2. No-load speed: Speed reached by the motor at no-load and input voltage (max.). Varies linearly with the supply voltage.
3. Stall torque: Torque developed at start when applying input voltage (max.) Varies with rising armature temperature, resistance increases at a rate of 0.4% per °C and stall torque decreases proportionally.
4. Power output: Mechanical peak power at input voltage (max.).
5. No-load current: Measured on the unloaded motor at no-load speed. The tolerances are relatively large (about −30% to +50%) and depend to a large extent on temperature. At −30°C it could increase to several times the indicated value, due to increased viscosity of bearing lubricant.
6. Back-EMF constant: The generated motor voltage for every 1000 r.p.m. of rotor speed. This constant equates with the torque constant (see 10).
7. Rotor Inductance: Value measured at terminals at a frequency of 1kHz, with motor stalled.
8. Motor regulation: Value obtained by dividing the no-load speed (radians per second) by the stall torque (Newton metres) or by dividing the motor resistance by the square of the torque constant. This represents the slope of the speed/torque characteristic (see Figs. 7 and 8), and indicates the efficiency of a motor for a given speed/torque condition. The lower the regulation value the lower the dissipated power for a given condition.
9. Terminal resistance: The total resistance of the motor at 22°C. Terminal resistance can, in most cases, be equated with armature resistance, since the contact resistance of the commutator/brushes is negligible by comparison. Note: resistance increases as in 3.
10. Torque constant: Also known as motor constant; indicates the torque developed for a current of 1Amp. Also equates to the EMF induced at an angular speed of 1 radian per second (back-EMF constant expressed in terms of V/rad/s =|Vs). The motor constant decreases by less than 0.02% for every 1°C rise in temperature. (Temperature coefficient of magnet).
11. Moment of inertia of the rotor: In the International System of Units it is expressed in kgm² (10^{-7}kgm²= 1gcm²)
12. Mechanical time constant: The time taken for the motor to achieve 63% of its no-load speed or its final speed under the set operating conditions, if these include only friction load with no inertial load.
13. Thermal time constant: The time taken by the armature (rotor) or stator (motor body) to attain 63% of the temperature rise corresponding to a given constant dissipated power.
14. Thermal resistances: Will give the armature temperature rise of the rotor and the temperature rise of the motor body per dissipated watt (I_2R). They are measured under unfavourable conditions, with the motor lying on a thermally insulated board, and without cooling. With large temperature differences, a rotor turning at high speed, forced air cooling or heat sink, it is possible to establish smaller values.
15. Guaranteed starting voltage. The average voltage where a motor will start at no load, is usually half the guaranteed value.

Gearboxes

Figure 2.



High quality ovoid gearboxes for use with RS d.c. precision motors. They have an inherently rugged construction enabling them to be used in a wide variety of d.c. drive applications including instrumentation and servo control. Gears are fixed (reversible) and mounted between steel plates on individual bearings. There is a double ended 4mm dia output shaft supported by self lubricating sintered bearings. The shaft is set at 12.7mm(½in) from the mounting centres of the gearbox. This is a commonly used, internationally recognised mounting configuration. The shorter end of the shaft is for coupling into RS mounting kit 336-214 (assembly instructions on page 4). If the kit is not required this end may be used as an additional load drive.

Each gearbox is supplied with an adaptor plate and mounting screws for assembling a motor to a gearbox (assembly shown fig. 2). Instructions are given on page 4. A range of gear ratios is offered giving the user the option to drive a variety of loads at reduced speeds. D.C. precision motors are fitted with a common pinion, which will mesh with any RS d.c. gearbox. The mechanical advantage of each gearbox will provide a considerable torque at the output shaft and the maximum starting torque available can be calculated by multiplying the starting torque of the motor (under given input voltage conditions) by the gear ratio and efficiency of the gearbox. Note that with larger gearbox ratios, this calculated torque may be far in excess of the maximum allowable stall torque of the gearbox — 0.8Nm. Care should be taken therefore, that the load torque does not exceed this value.

Inertial loads will alter the time constant of the drive (see motor equations). The equivalent moment of inertia at the motor shaft can be calculated by dividing the load moment by the square of the gearbox ratio.

Gearbox characteristics

Gearbox stock no.	336-220	336-236	336-242	336-258	336-264	336-270	336-286
gear ratio	5:1	15:1	40:1	160:1	640:1	1250:1	2560:1
approximate efficiency	81%	73%	73%	66%	59%	59%	53%
output direction with respect to input	=	≠	≠	=	≠	≠	=

= direction the same
≠ direction reversed.

Mechanical details applying to all gearboxes:

Maximum output torque: 0.4 Nm at 25 rpm, 0.05 Nm at 300 rpm
Maximum stall torque: 0.8 Nm
Average backlash: 1.5° at no-load
3° at 0.3 Nm
Radial shaft play: 25μm
Shaft end play: 250μm
Maximum side load: 40N (at 8mm from mounting face)
Maximum axial load: 20N
Maximum static axial force for press fit: 150N
Weight: 72g max.

Motor/gearbox mounting instructions

Figure 3.

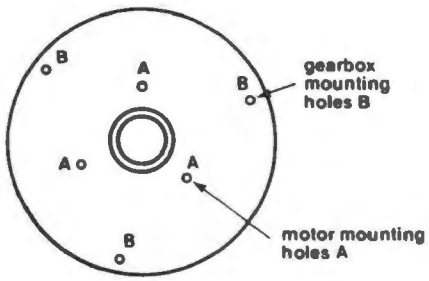
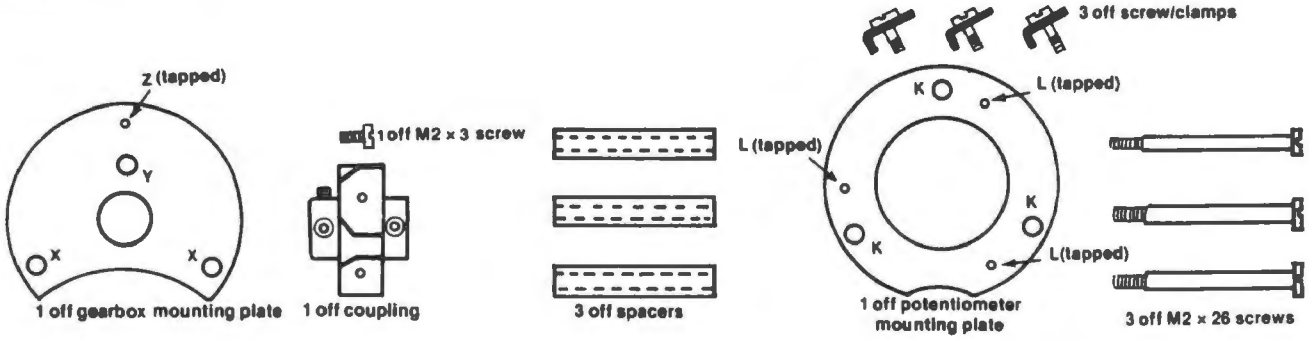


Fig. 3 shows the plastic adaptor plate provided with each gearbox (motor mounting side shown).
Screw adaptor plate to motor using 3 off M2 x 4 screws in holes A (use any 3 of 6 'A' holes in fig. 1). Fasten motor/adaptor plate assembly to gearbox (see fig. 2) using 3 off M2 x 5 screws in holes B.

Servo mounting kit 336-214

Figure 4.



A mounting kit specially designed to mechanically couple RS d.c. precision motor/gearbox assemblies, to RS conductive plastic servo potentiometers. The completed assembly provides a rugged and compact structure for servo control. Fig. 4 describes the parts supplied with each kit. Mounting plates are plated steel, spacers are plated brass and screws are plated steel. All kit parts are precision engineered to give good mechanical support to the potentiometer coupling and fine shaft alignment. The coupling is for 4mm to ⅛ in dia shafts and will adequately accommodate any slight shaft parallel or radial alignment discrepancy due to tolerance of parts or kit assembly.

Kit assembly instructions

Figure 5.

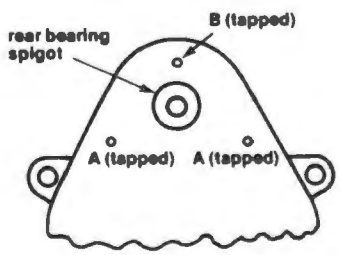


Fig. 5 shows the view of the gearbox before assembly of the mounting kit. Parts refer to fig. 4.

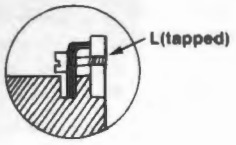
1. Locate the gearbox mounting plate over the rear bearing spigot and tighten M2×3 screw through hole Y into tapped hole B of the gearbox.

2. Assemble potentiometer mounting plate with 3 off spacers and 3 off screws M2×26. Pass each screw through a K hole and through a spacer. Pass two of the screws through holes X of gearbox mounting plate and tighten into tapped holes A of the gearbox. Tighten one screw directly into tapped hole Z of the gearbox mounting plate.

3. Fit coupling to gearbox shaft, ensuring that there is a 1mm clearance between the rear bearing spigot and the coupling. Do not lock the coupling at this point.

4. Locate potentiometer spindle into the coupling and spigot into the central hole of potentiometer mounting plate. Fit 3 off potentiometer screw/clamps into tapped holes L as shown in

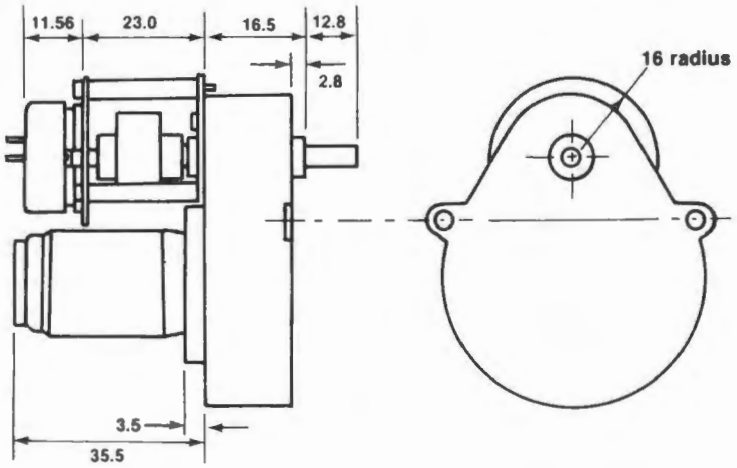
figs. 4 & 6. Adjust position of potentiometer body as required and tighten clamps.



5. Lock coupling to potentiometer spindle and with the aid of resistance meter, set the angular position of the spindle to give the required resistance. Whilst holding the coupling in position, adjust the load to its required angular position and then lock coupling to gearbox shaft.

6. It is recommended that the initial set position lies within the desired angular range of the intended servo mechanism. Date sheet R/4024 gives details of a circuit using RS servo i.c. 304-813.

Figure 6. Dimensional assembly of the servo mounting kit to gearbox, including potentiometer and motor.



Physical properties of motor and applications

Scope

Primarily d.c. precision motors are dynamically efficient. That is to say because of the low rotor inertia and minimal frictional losses, their response is fast and output torque will be uniform and will change smoothly in response to electrical input. One of their main features is to accelerate a load quickly, maintain constant speed to within reasonable limits then decelerate to rest, usually in small angular motions. Such characteristics render them very suited for servo applications.

A second advantage lies with the defined motor characteristics, which may be consulted when using a motor in an open ended mode. With load torque and speed known the most suitable motor/gearbox choice can be made and input voltage, power and efficiency simply calculated. It should be noted that the speed of these motors cannot be defined absolutely, unless some form of speed encoding with feedback control is used. For most open ended applications a range of velocities can be predicted to tolerances of 5 to 10% providing certain influence factors are taken into consideration. Better tolerances may be achieved with one set speed. The main factors influencing speed are torque, input power, winding temperature and overall motor tolerances (see definition of characteristics page 2).

The curves shown on page 5 (figs. 7 & 8) give motor performance at maximum recommended input voltage. Lower input voltages will give similar curves which may be derived from the motor characteristics on page 2 and motor equations page 7. Maximum output power is limited to approximately 1.5 watts. Output power can be translated into a variety of torque/speed configurations with different gearboxes (figs. 9 to 12). Careful selection using these parameters will enable the user to choose an optimum drive performance.

Figure 7.

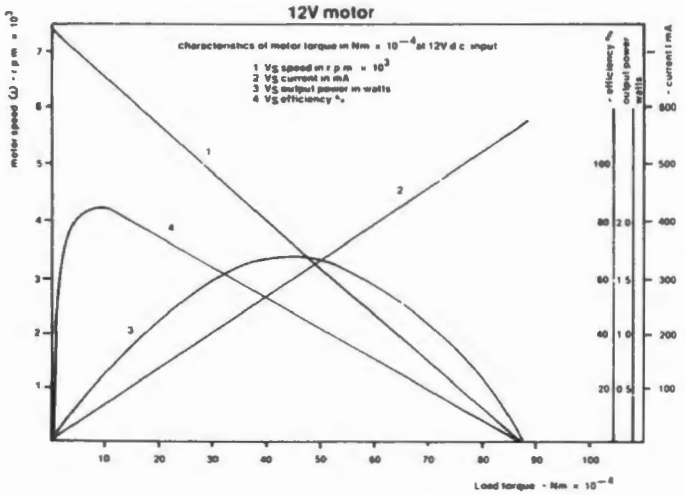
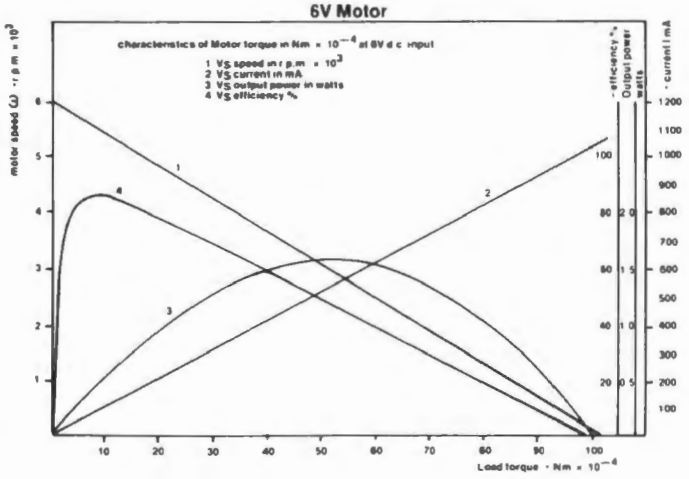


Figure 8.



Torque versus speed characteristics for motor/gearbox combinations at maximum input voltage

Figure 9.

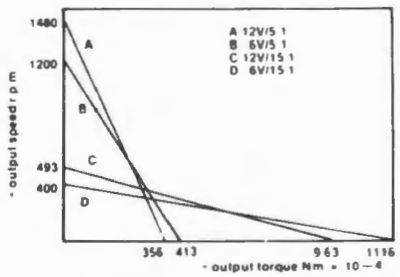


Figure 10.

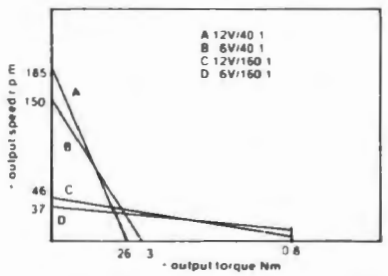


Figure 11

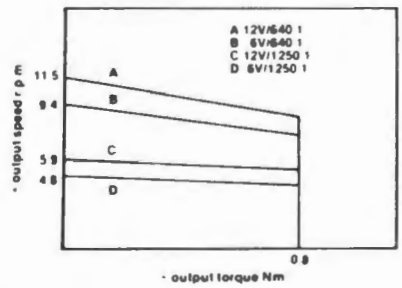
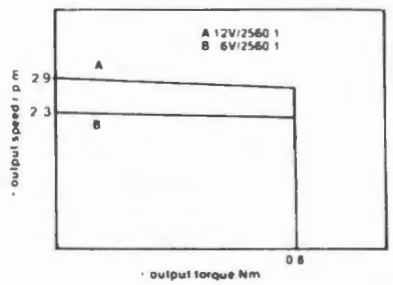


Figure 12.



Motor Equations

see page 2 for definition of motor symbols

Figure 13.

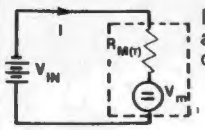


Fig. 13 gives the equivalent electrical circuit for a d.c. motor. The basic equations below will derive the curves shown in figs. 7 & 8.

Input voltage V_{IN}

$$V_{IN} = IR_{m(T)} + V_m \quad \text{——— 1}$$
$$V_m = K_e \omega \quad \text{——— 2}$$

Basic motor equation

$$V_{IN} = IR_{m(T)} + K_t \omega \quad \text{——— 3}$$

where $R_{m(T)}$ is terminal resistance at T°C (see equation 13), and ω is motor speed in radians /sec. $K_e = K_t$.

Input current I

$$I = M/K_t \quad \text{——— 4}$$

where M is the sum of load torque M_L and motor frictional torque M_f. Under normal conditions $M_f << M_L \therefore M \simeq M_L$.
Where equation 4 gives the current/torque characteristic.

Input power P_{IN}

$$P_{IN} = P_{OUT} + P_d \quad \text{——— 5}$$

Dissipated power P_d

$$P_d = I^2 \ R_{m(T)} \quad \text{——— 6}$$

Output power P_{OUT}

$$P_{OUT} = M\omega \quad \text{——— 7}$$

where M is in Nm and ω is in radians/sec. Equation 7 gives the output power/torque characteristic.

Temperature rise ΔT

$$\Delta T = \theta ra \ P_d \quad \text{——— 8}$$

Temperature rise can be estimated by taking the thermal resistance between rotor and ambient θ_{ra} (worst case: see definition of characteristics no. 14 page 2).

Where $\theta_{ra} = \theta_{rb} + \theta_{ba}$ ——— 9

Rotor temperature T

$$T = T_i + \Delta T \quad \text{——— 10}$$

where T_i is the initial rotor temperature.

NB. Care should be taken when starting and running a motor (particularly at high torques) that the heating effect in the winding does not cause its continuous running temperature to exceed 100°C.

Starting current I_d

$$I_d = V_{IN}/R_{m(T)} \quad \text{——— 11}$$

Starting torque M_d

$$M_d = K_t(I_d - I_O) \quad \text{——— 12}$$

Terminal resistance $R_{m(T)}$

$$R_{m(T)} = R_{m(Ti)}(1 + \gamma \Delta T) \quad \text{——— 13}$$

where the temperature coefficient of copper γ = 0.004 per °C.

Efficiency η

$$\eta = 1 + {}^{I_O}/_{I_d} - {}^{I_O}/_{I} - {}^{I}/_{I_d} \quad \text{——— 14}$$

Equation 14 derives an estimated efficiency characteristic, see figs. 7 & 8. Actual measured currents will give a more realistic efficiency value. Another approximation for efficiency $\eta = P_{OUT}/P_{IN}$.

Motor time constant τm

$$\tau_m = (R_{m(T)}/K_t^2)Jm \quad \text{——— 15}$$

Equation 15 is for an unloaded motor.

Loaded time constant τ

$$\tau = \tau_m(1 + {}^{J_L}/_{J_M}) \quad \text{——— 16}$$

where J_L is the equivalent moment of inertia of the load at the motor shaft, τ is the time taken for an inertial load J_L to reach 63% of its final speed.

Motor speed ω

$$\omega = \omega_1(1 - e^{-t/\tau}) \quad \text{——— 17}$$

where ω_1, is the final speed attained by the motor with load J_L, and t is the time to reach ω from rest.

Angular acceleration α

$$\alpha = K_t(I_d - I_O)/Jm \quad \text{——— 18}$$

where α is the acceleration at motor start, and starting torque $M_d = J_m\alpha$

RS data

Worked example (refers to motor equations page 7)

To calculate the working parameters of a particular application it is useful to get an early approximation of the mechanical output power required (see equation 7) where in most cases the required output speed, load torque and available supply voltage is known. Taking two examples as follows:-

Case A Output speed 20 r.p.m.
Output torque 1000 gcm
Case B Output speed 1000 r.p.m.
Output torque 20 gcm

Available supply 6V
In both cases

$$P_{OUT} = \frac{1000 \times 2\pi}{60} \times 20 \times 10^{-4}$$
$$= 0.21 \text{ watts}$$

where 1Nm = 10^4 gcm

$$1 \text{ r.p.m.} = \frac{2\pi}{60} \text{ radians/sec}$$

Therefore the load is well within the output power capability of the 6V motor.
As a general rule of thumb, when the load torque exceeds half the motor starting torque Md than a gearbox should be considered. If load torque <½ Md then the motor may be considered on its own. Although in A and B the same output power is required, they will need different drive configurations.

Case A Load torque >> Md: therefore a gearbox must be used. Looking at the motor/gearbox characteristics fig. 10 we could select either a 40:1 or a 160:1 gearbox because the operating point falls within both characteristics for the 6V motor.
In general, the higher the gearbox ratio the lower the required motor output torque. Looking at fig. 8 efficiency will increase between Md and 1/10 Md. Therefore in case A the 160:1 gearbox will give a better efficiency.

Case B Load torque <½ Md: therefore we could consider a 5:1 gearbox or the motor on its own.

Question What is the supply voltage, current, power and efficiency for case A at 22°C?

Assuming the 160:1 gearbox is used, then:

Motor speed ω = gearbox ratio x output speed
= 160 x 20
= 3,200 r.p.m. = 335 rad/sec.

Input voltage $V_{IN} = IR_m + K_t$
$$= \frac{9.5 \times 5.7}{97} + 335 \times 97 \times 10^{-4}$$
$$= 3.81 \text{ volts}$$

Power dissipated Pd = $0.098^2 \times 5.7$ = 55mW

Estimated temperature rise ΔT
= $35 \times 55 \times 10^{-3}$ = 1.9°C

$$\text{Load torque } M_L \times = \frac{\text{Output torque}}{\text{gearbox ratio x gearbox effy.}}$$
$$= \frac{1000}{160 \times .0.66} = 9.5\text{gcm}$$

$$\text{Running current} = M_L/K_t = \frac{9.5}{97} = 0.098\text{A}$$

Input power P_{IN} = 0.21 + 0.055 = 0.265 watts

We can see that rotor resistance will have a negligible change and the motor will run within its power and temperature limits. However, if ΔT substantially affects motor resistance Rm (T) then V_{IN} and Pd must be reassessed accordingly.
In some cases we may need to examine the situation where the motor is stalled or when it does not start under load.

Stall current Id = $\frac{3.81}{5.7}$ = 0.67A (assuming a power supply voltage of 3.81 volts).

Power dissipated at stall = $0.66^2 \times 5.7$ = 2.5 watts
Estimated temperature rise at stall ΔT
= 2.5 x 35 = 89°C
At 22°C ambient, rotor temperature
= 89 + 22 = 111°C
Therefore precautions should be taken to prohibit motor stall and/or a current limit should be incorporated.

Estimated motor efficiency =

$$1 + \frac{6}{670} - \frac{6}{98} - \frac{98}{670} \doteqdot 80\%$$

Overall efficiency = motor effy x gearbox effy = 80% x 66% = 53%.

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RS data

DIN Rail miniature circuit breakers

A range of single pole and triple pole d.i.n. rail mounting miniature circuit breakers, conforming to VDE 0641, BS 3871 part 1, CEE 19 and DIN 43234, having the capability of safely carrying their normal stated operating current but reliably interrupting dangerous over-currents, thereby protecting the insulation of cables against over heating.

Features

RS d.i.n. rail miniature circuit breakers are current limiters and have the following features:

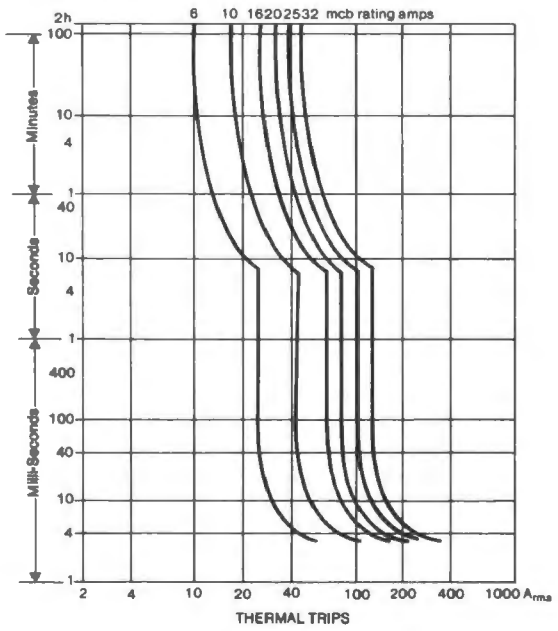
- High switching capacity (6 kA at cos $\varnothing$=0.6)
- Low let-through energy
- Full selectivity with back-up fuses (selectivity class S3)

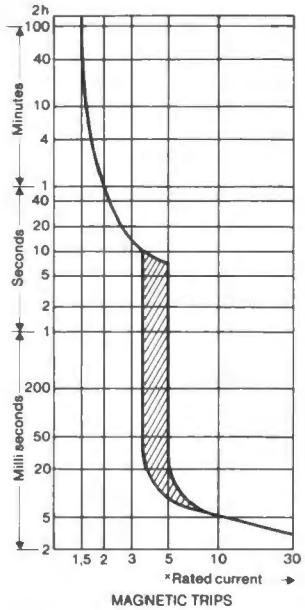
Specification

Mechanical life span Breaker life span at rated current	}	20,000 operations = 40,000 movements
Ambient temperature	open	max/min + 50°C/−25°C
	enclosed	max/min +40°C/−25°C
Rated insulation voltage		440V
Heat loss at continuous current Ith 2		3.5W
Switching capacity 220/415V 50 Hz		6000A
Selectivity with fuses 100A		35 kA
80A		45 kA
63A		55 kA

Tripping characteristics

Figure 1 **Tripping characteristics**





As shown in Figure 1 the magnetic trips operate at 3.5 to 5 times the rated current. The advantage of this is that the current peaks which occur when switching on filament lamp circuits, will not then cause the circuit breaker to trip.

The characteristics for the thermal trips indicate the mean value of the tolerance band at 20°C ambient starting from the cold state. The response time of the bimetal trips from the warm state is approximately 25% of that shown.

RS data

Application: Miniature circuit breakers for lighting installations

		Fluorescent lamps 220-240V								Filament bulbs 220-240V						
		Non-compensated				Individually compensated										
rating W		40	100	65	120	40	100	65	120	40	60	75	100	200	300	500
current A		0.43	1.5	0.7	1.6	0.3	0.7	0.45	0.8	0.18	0.27	0.34	0.45	0.9	1.36	2.27
capacitor μF		—	—	—	—	4.5	18	7	18	—	—	—	—	—	—	—
length cm		120	120	150	150	120	120	150	150	—	—	—	—	—	—	—
stock nos.	rating per pole	Maximum number of lamps per pole when switched simultaneously.														
		No. of fluorescent lamps								No. of filament bulbs						
335-924 / 334-779	6A	12	3	7	3	9	4	6	3	18	12	10	8	4	2	1
335-918 / 334-763	10A	21	6	12	5	18	7	12	6	36	24	19	15	7	4	2
335-902 / 334 757	16A	33	9	20	9	30	11	19	9	57	38	30	23	11	7	4
335-895 / 334 741	20A	42	12	25	11	37	14	24	12	72	48	38	30	14	9	5
335-889 / 334-735	25A	52	15	32	14	47	18	30	15	90	60	48	38	18	12	7
335-873 / 334 729	32A	67	19	41	18	60	22	38	18	114	76	60	46	22	14	8

Full rated current can be utilized for switching individual lamps

Selectivity

In domestic and commercial premises a fuse is in most cases fitted into the supply line to the distribution board in which the miniature circuit breakers are housed. This can be either the sealed service line fuse or the fuse in the consumer box.

It is required that:

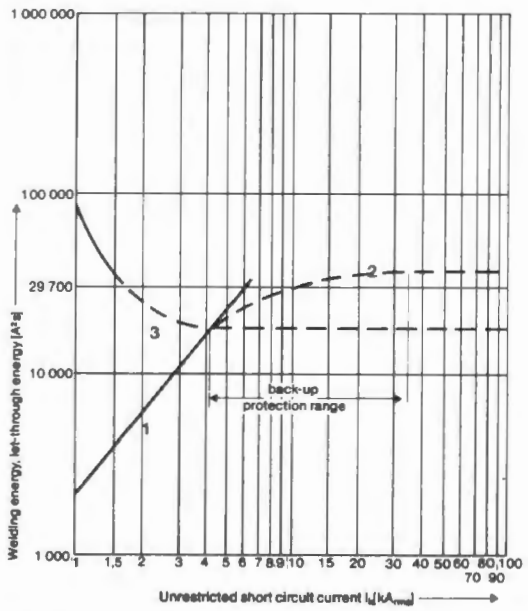
1. The installation should not be interrupted during faultless operation.
2. In a fault situation only the affected mains section should be disconnected.
3. Upon failure of an overcurrent protective device, the next element on the line side should reliably effect disconnection.

The selectivity of miniature circuit breakers is judged by their let-through energy. As shown in Figure 2 the characteristic curve for the RS d.i.n. rail miniature circuit breakers cut the line of the lowest welding energy of a 100 amp fuse at 4200 amp. These are the highest permissible fault current values for full selectivity of such a switching combination.

The I.E.E. regulations demand that the switching capacity of protective devices must at least be sufficient to control the prospective fault current at the point of installation. However, this demand need not be met where an additional protective element is connected on the line side.

An RS d.i.n. rail miniature circuit breaker in combination with a 100 amp fuse offers short circuit protection up to 35 kA.

Figure 2 **Back-up protection with RS miniature circuit breakers and 100 amp fuse.**



1. Maximum let-through energy of miniature circuit breaker.
2. Maximum let-through energy of miniature circuit breaker and 100 amp fuse.
3. Minimum welding energy of 100 amp fuse.

R.S. Components Ltd. 13-17 Epworth Street, London. EC2P 2HA Telephone: 01-253-1222 01-250-4000
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RS data

Voltage converter i.c.'s RS7660 and AD7560

Stock numbers 304-598 and 300-445

RS7660

The RS7660 i.c. is a power supply circuit designed to perform supply voltage conversion from positive to negative, ie. for an input range of +1.5V dc to +10.0V dc complementary output voltages of –1.5V dc to –10.0V dc are produced. In most applications the device requires just two non-critical external capacitors to function, an additional diode being required only for supply voltages in excess of 6.5V dc.

Typical applications include data acquisition systems requiring dual rail supplies for analogue functions derived from the single rail logic supply, microprocessor negative rails, –5V substrate bias for dynamic rams, –5V rail for 7107 dpm i.c.s. etc.

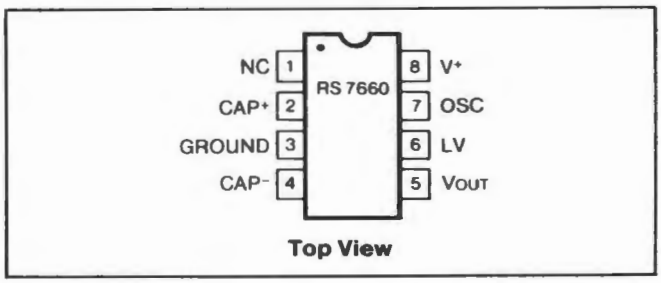
Absolute maximum ratings

Supply voltage ____ 10.5V
Oscillator input voltage (Note 1) ____
0.3V to (V^+ +0.3V) for V^+ <5.5V
(V^+ –5.5V) to (V^+ +0.3V) for V^+ >5.5V
–0.3V to (V^+ +0.3V) for V^+ <3.5V
LV (Note 1) ____ No connection for V^+ >3.5V
Output short duration (V_{SUPPLY} ≤5.5V) Continuous
Operating temp range ____ –20°C to +70°C

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Features

- Simple conversion of +5V logic supply to ±5V supplies
- Simple voltage multiplication ($V_{OUT} = (-) nV_{IN}$)
- 99.9% typical open circuit voltage conversion efficiency
- 98% typical power efficiency
- Wide operating voltage range 1.5V to 10.0V
- Easy to use – requires only 2 external non-critical passive components



Top View

Note 1. Connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to 'power up' of the RS7660.

Note 2. Derate linearly above 50°C by 5.5mW/°C.

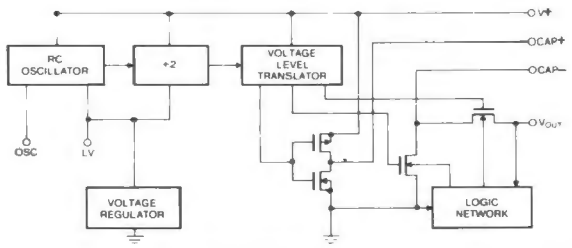
Operating characteristics $V^+ = 5V$, $T_A = 25°C$, $C_{OSC} = 0$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Limits Min.	Typ.	Max.	Unit
I^+	Supply Current	$R_L = \infty$		170	500	μA
V^+_{H1}	Supply Voltage Range – Hi (D_X out of circuit)	0°C ≤ T_A ≤ 70°C, R_L = 10kΩ, LV = No Connection	3.0		6.5	
V^+_{L1}	Supply Voltage Range – Lo (D_X out of circuit)	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = Ground	1.5		3.5	V
V^+_{H2}	Supply Voltage Range – Hi (D_X in circuit)	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = No Connection	3.0		10.0	V
V^+_{L2}	Supply Voltage Range – Lo (D_X in circuit)	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = Ground	1.5		3.5	V
R_{OUT}	Output Source Resistance	I_{OUT} = 20mA, T_A = 25°C		55	100	Ω
		I_{OUT} = 20mA, –20°C ≤ T_A ≤ +70°C			120	Ω
		V^+ = 2V, I_{OUT} = 3mA, LV = Ground, –20°C ≤ T_A ≤ +70°C			300	Ω
f_{OSC}	Oscillator Frequency			10		kHz
P_{Ef}	Power Efficiency	R_L = 5kΩ	95	98		%
V_{OUTEf}	Voltage Conversion Efficiency	$R_L = \infty$	97	99.9		%
Z_{OSC}	Oscillator Impedance	V^+ = 2 Volts		10		MΩ
		V^+ = 5 Volts		100		kΩ

Circuit operation

Contained on chip are series dc voltage regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic network which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latchup free operation.

Figure 1 **Block diagram of RS 7660**

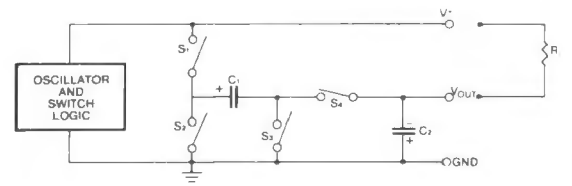


The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the 'OSC' terminal, or the oscillator may be overdriven by an external clock.

The 'LV' terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

The mode of operation of the device may be best understood by considering Figure 2, which shows an idealized voltage doubler.

Figure 2 **Idealized voltage doubler**



Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: switches S_2 and S_4 are open during the half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The RS7660 approaches this ideal situation more closely than existing non-mechanical circuits.

The four switches in Figure 2 are MOS power switches; S_1 is a P-channel device and S_2, S_3 and S_4 are N-channel devices. A common difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their 'ON' resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probably device latchup.

This problem is eliminated in the RS7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias

The voltage regulator portion of the device is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the 'LV' pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal **must** be left open to ensure latchup proof operation, and prevent device damage.

Typical performance characteristics

Output voltage as a function of output current

Figure 3

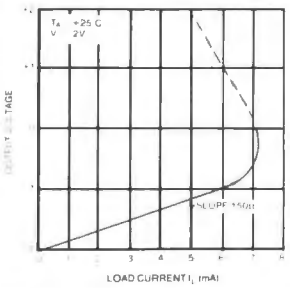
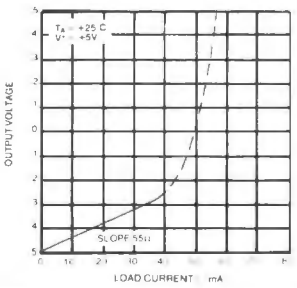


Figure 4



Supply current and power conversion efficiency as a function of load current

Figure 5

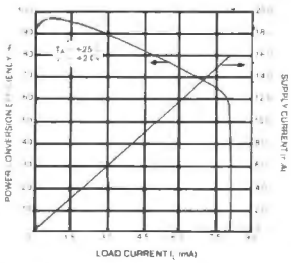
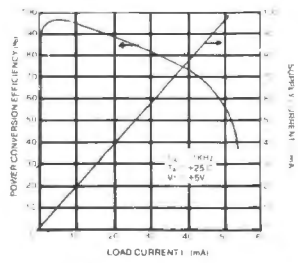


Figure 6



Output source resistance as a function of supply voltage and temperature

Figure 7

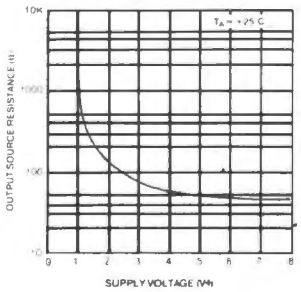
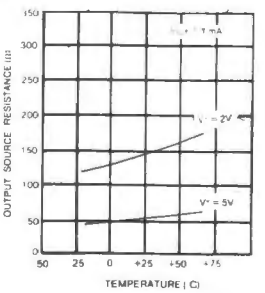


Figure 8



Frequency of oscillation as a function of temperature and external oscillator capacitance

Figure 9

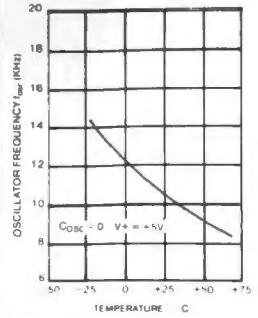


Figure 10

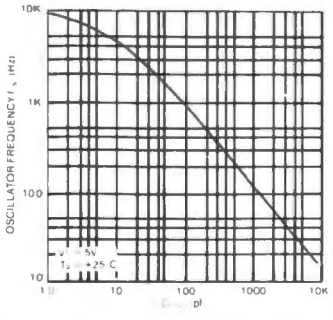


Figure 11

Power conversion efficiency as a function of osc frequency

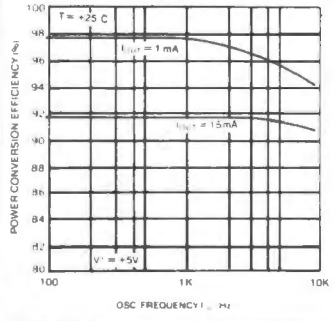
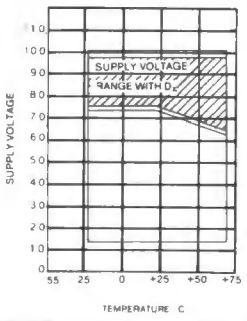


Figure 12

Operating voltage as a function of temperature



Typical applications

Simple negative voltage converter.

The majority of applications will undoubtedly utilize the RS7660 for generation of negative supply voltages. Figure 13 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of + 1.5V to +10.0 volts, keeping in mind that pin 6 (LV) is tied to the supply negative GND only for supply voltages below 3.5 volts, and that diode D_X **must** be included for proper operation at higher voltages and/or elevated temperatures.

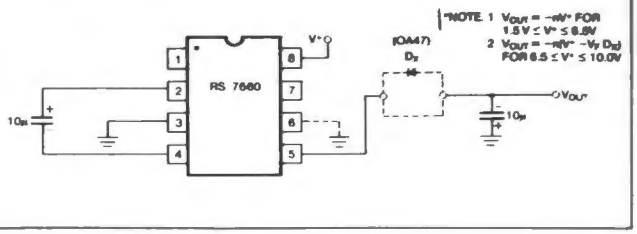
The output characteristics of the circuit in Figure 13 are those of a nearly ideal voltage source in series with 70 ohms. Thus for a load current of –10mA and a supply voltage of +5 volts, the output voltage will be –4.3 volts. The dynamic output impedance due to the capacitor impedances is $1/\omega C$ where

$$C = C_1 = C_2$$

$$\text{giving } \frac{1}{\omega C} = \frac{1}{2\pi f_{osc} \times 10^{-5}} \simeq 3 \text{ ohms}$$

for $C = 10\mu F$ and $f_{osc} = 5kHz$
(½ of oscillator frequency)

Figure 13 **Simple negative converter**

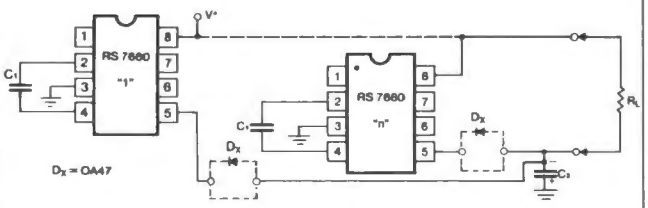


Paralleling devices

Any number of RS7660 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2 serves all devices while each device requires its own pump capacitor. The resultant output resistance would be approximately.

$$R_{OUT} = \frac{R_{OUT} \text{ (of RS7660)}}{n \text{ (number of devices)}}$$

Figure 14 **Paralleling devices**



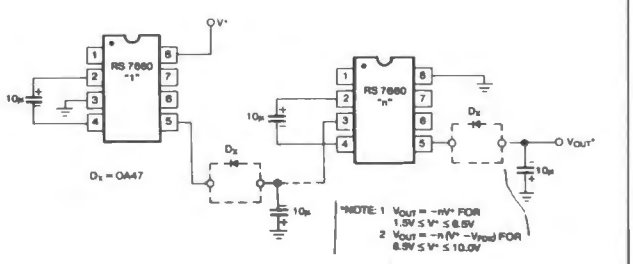
Cascading devices

The RS7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage, however, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the sum of the individual RS7660 R_{OUT}'s.

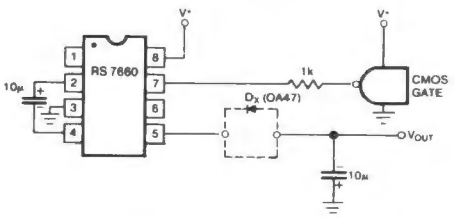
Figure 15 **Cascading devices for increased output voltage**



Changing the RS7660 oscillator frequency

It may be desirable in some applications, due to noise or other considerations, to change the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 16. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be ½ of the clock frequency.

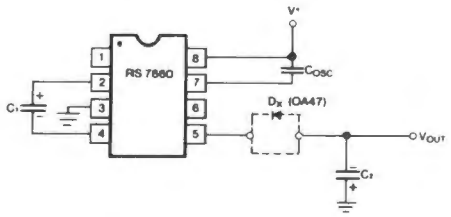
Figure 16 **External clocking**



It is also possible to maximise the conversion efficiency of the RS7660 by lowering the oscillator frequency. This is achieved by connecting an additional capacitor C_{OSC} as shown in Figure 17.

Reducing the oscillator frequency will necessitate an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10μF to 100μF).

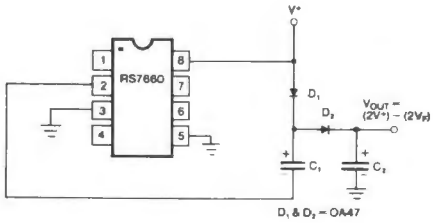
Figure 17 **Reducing oscillator frequency**



Positive voltage multiplication

The RS7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 18. In this application, the pump inverter switches of the RS7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

Figure 18 **Positive voltage multiplier**

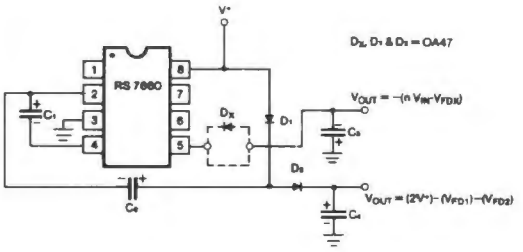


The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.

Combined negative voltage conversion and positive supply multiplication.

Figure 19 combines the functions shown in Figures 13 and 18 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9 volts and –5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

Figure 19 **Combined negative converter and positive multiplier**



AD7560

The AD7560 is a monolithic CMOS voltage converter plus voltage reference circuit. It performs both voltage inversion and subsequent voltage multiplication of the incoming positive supply voltage. It contains two converter circuits, A and B, in series to provide two negative output voltages of approximately $-V_{DD}$ and $-3V_{DD}$ from the $+V_{DD}$ input. The unregulated $-3V_{DD}$ output from converter B is used to generate an internal reference voltage of –5V. This is buffered and amplified to provide a temperature compensated – 10V output (V_{REF}, pin 9) which can sink over 1.0mA. In applications where the reference output is not required this section can be powered down via the reference inhibit input $\overline{INH}$, pin 1.

An on-chip oscillator is provided to drive the converters. The oscillator frequency is determined by the addition of an external capacitor. Additionally, if converter synchronization to an external clock source is required, the clock input can be driven directly from a 5V CMOS compatible clock source.

Absolute maximum ratings*

V_{DD} to DGND	–0.3V, +8V
V_{DD} to V_{C2}	–0.3V, +16V
V_{DD} to V_{C4}	–0.3V, +32V
V_{DD} to V_{SS}	–0.3V. +32V
V_{C2}, – C1, (DGND = 0V)	V_{DD}, –8V
V_{C4}, – C3, (DGND = 0V)	V_{DD}, –24V
+C1 (DGND = 0V)	–0.3V, V_{DD}
+C3 (DGND = 0V)	V_{C2}, V_{DD}
AGND to DGND	V_{SS}, V_{DD}
CLK, $\overline{INH}$, (DGND = 0V)	V_{DD}, –5V
V_{REF}	V_{DD}, V_{SS}
R_{IN}, R_{FB} (AGND = 0V)	±15V
I_{DD}	100mA dc
I_{REF} Short circuit duration to V_{DD}	Continuous
I_{C2} Short circuit duration to DGND	Continuous
I_{C4} Short circuit duration to DGND	Continuous
Operating temperature range	–25°C to +70°C
Storage temperature	–65°C to +150°C
Lead temperature (soldering, 10 secs)	+300°C
Power dissipation (package) to + 50°C	450mW
Derate above +50°C by	6mW/°C

*Stresses above those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational selections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Features

- Efficient series stacked dc/dc converters which provide multiple outputs from a single +5V supply (–5V, –10V, –15V, +10V, +15V)
- On-chip –10V reference voltage output
- High reference voltage power supply rejection
- Minimum circuit requires only two low cost capacitors

Applications

- Negative reference voltage generation for data acquisition systems, from a single +5V supply
- Op-amp supply generation; ±5V, ±15V
- Low power, high efficiency voltage converter for single battery operation

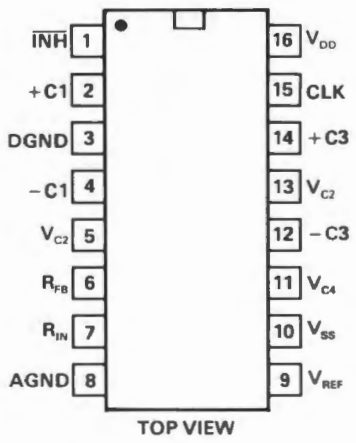
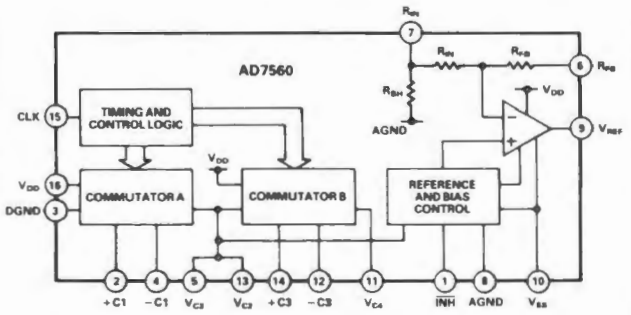


Figure 20 **Block diagram of AD7560**



Electrical characteristics using internal voltage reference

V_{DD} = +5V, F_{CLK} = 6kHz external clock, 0 ≤ I_{REF} ≤ 1mA. All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	Test conditions	Limits			Unit
		Min.	Typ.	Max.	
Converter A (Pins 5 and 13)					
Voltage conversion factor, $\propto_A$					
T_A = +25°C	$I_{C2} = I_{C4}$ = 0mA	0.90	0.95		
T_{min}, T_{max}		0.85	0.90		
V_{C2} Output source resistances					
T_A = + 25°C	I_{C2} = 5mA, I_{C4} = 0mA		12	160	Ω
T_{min}, T_{max}				200	Ω
V_{C2} Short circuit current	Short circuit to DGND		30		mA
Converter B (Pin 11)					
Voltage conversion factor, $\propto_B$					
T_A = +25°C	$I_{C2} = I_{C4}$ = 0mA	2.80	2.90		
T_{min}, T_{max}		2.75	2.85		
V_{C4} Output source resistance					
T_A = +25°C	I_{C2} = 0mA, I_{C4} = 2.5mA		750	900	Ω
T_{min}, T_{max}				1200	Ω
V_{C4} Short circuit current	Short circuit to DGND		20		mA
Voltage reference (Pin 9)					
Reference output resistance			20		kΩ
Reference short circuit current	Short circuit to AGND			0.4	mA
Buffer amplifier resistor values		30	50	75	kΩ
Input shunt resistance, R_{SH}			75		kΩ
Digital inputs					
INH (Pin 1)					
V_{IH} Input high voltage		+3.0			V
V_{IL} Input low voltage				+0.8	V
I_{IN} Input current	V_{IN} = 0V or V_{DD}			±10	μA
C_{IN} Input capacitance				7	pF
CLK (Pin 15)					
V_{IH} Input high voltage		+3.0			V
V_{IL} Input low voltage				+0.8	V
I_{IN} input current	V_{IN} = 0V or V_{DD}		±15	±25	μA
Power requirements					
V_{DD} Operating range		+4.5	+5.0	+5.5	V
Power supply current	$I_{C2} = I_{C4}$ = 0mA		3	6	mA
	I_{C2} = 0mA, I_{C4} = 2.5mA		12	16	mA

Electrical characteristics using external voltage reference

V_{DD} = +5V, F_{CLK} = 6kHz external clock, 0 ≤ I_{REF} ≤ 1mA. All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	Test conditions	Limits			Unit
		Min.	Typ.	Max.	
Converter A (Pins 5 and 13)					
Voltage conversion factor, $\propto_A$					
T_A = +25°C	$I_{C2} = I_{C4}$ = 0mA	0.68	0.80		
T_{min}, T_{max}		0.65	0.70		
V_{C2} Output source resistance					
T_A = + 25°C	I_{C2} = 1mA, I_{C4} = 0mA, 0≤ I_{REF} ≤0.25mA		120	160	Ω
T_{min}, T_{max}				200	Ω
V_{C2} Short circuit current	Short circuit to DGND		30		mA
Converter B (Pin 11)					
Voltage conversion factor, $\propto_B$					
T_A = +25°C	$I_{C2} = I_{C4}$ = 0mA	2.35	2.45		
T_{min}, T_{max}		2.30	2.35		
V_{C4} Output source resistance					
T_A = +25°C	I_{C2} = 0mA, I_{C4} = 0.25mA, 0≤I_{REF} ≤0.25mA		750	900	Ω
T_{min}, T_{max}				1200	Ω
V_{C4} Short circuit current	Short circuit to DGND		20		mA
Voltage reference (Pin 9)					
Reference voltage output			–10.00		V
Reference voltage accuracy				±500	mV
Reference temperature coefficient				±200	ppm/°C
Reference voltage drift	1000 hours, +70°C		±60		mV
Reference sink current			1.0	1.5	mA
Reference output resistance			1	3	Ω
Reference short circuit current	Short circuit to AGND			5	mA
Power supply rejection	V_{REF}/V_{DD}		±6	±12	mV/V
Buffer amplifier resistor values		30	50	75	kΩ
Input shunt resistance, R_{SH}			75		kΩ
Digital inputs					
INH (Pin 1)					
V_{IH} Input high voltage		+3.0			V
V_{IL} Input low voltage				+0.8	V
I_{IN} Input current	V_{IN} = 0V or V_{DD}			±10.0	μA
C_{IN} Input capacitance				7	pF
CLK (Pin 15)					
V_{IH} Input high voltage		+3.0			V
V_{IL} Input low voltage				+0.8	V
I_{IN} Input current	V_{IN} = 0V or V_{DD}		±15	±25	μA
Power requirements					
V_{DD} Operating range		+4.75	+5.0	+5.5	V
Power supply current	$I_{C2} = I_{C4}$ = 0mA		15	22	mA

Test circuits

Figure 21 **Test circuit for dc-dc converter only, $\overline{INH}$ = 0V**

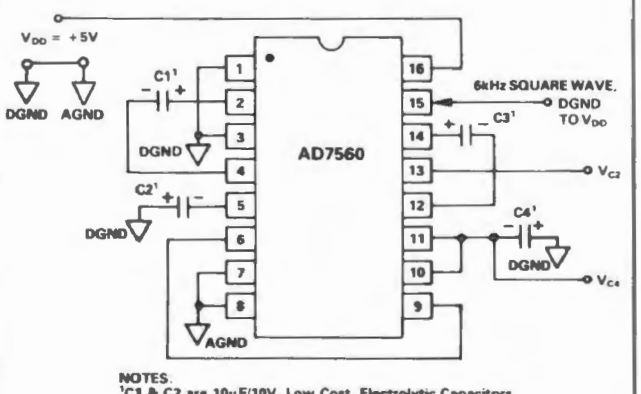
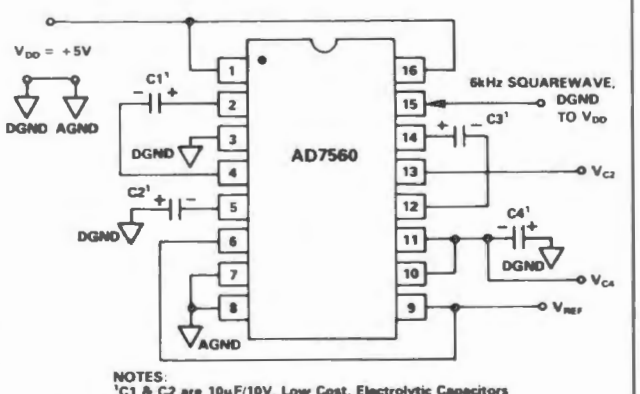


Figure 22 **Test circuit for dc/dc converter and voltage reference, $\overline{INH}$ = V_{DD}**



Typical performance characteristics

Figure 23 **V_{C2} output voltages vs. I_{C2} output current for different values of I_{C4}** (see Figure 21)

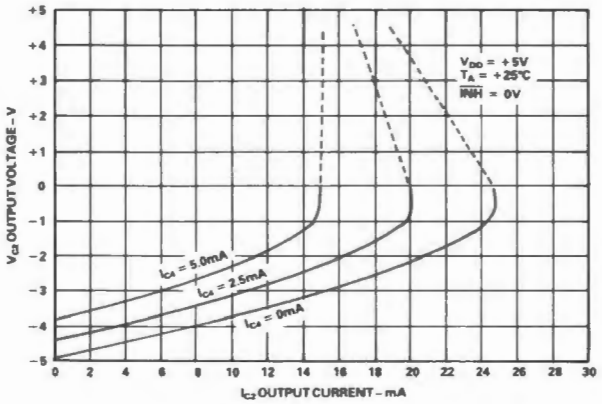


Figure 24 **V_{C4} Output voltage vs. I_{C4} output current for different values of I_{C2}** (see Figure 21)

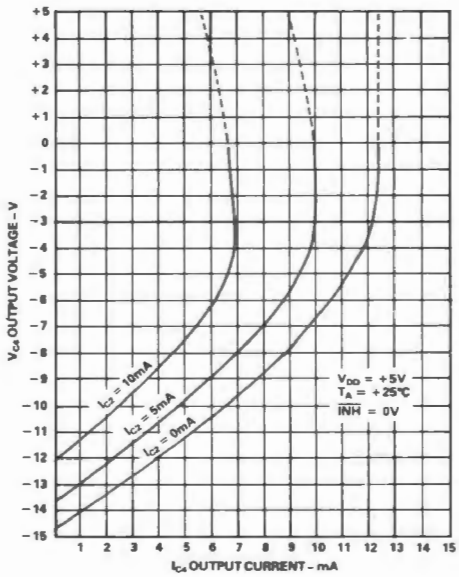


Figure 25 **V_{REF}, V_{C2} and V_{C4} output voltage levels vs. reference sink current I_{REF}** (see Figure 22)

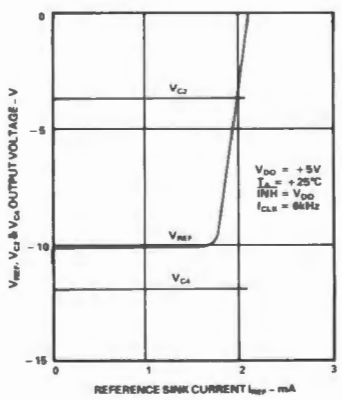


Figure 26 **Output reference voltage V_{REF} vs. I_{C2} and I_{C4} load currents** (see Figure 22)

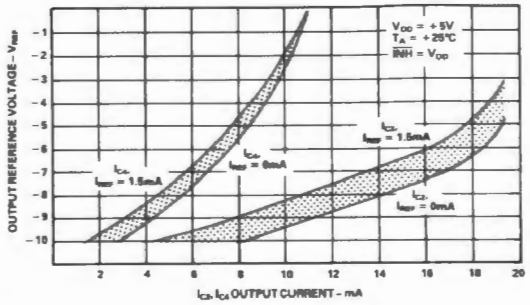


Figure 27. **I_{C2} vs. operating area (shaded) for V_{REF} = –10V** (see Figure 22)

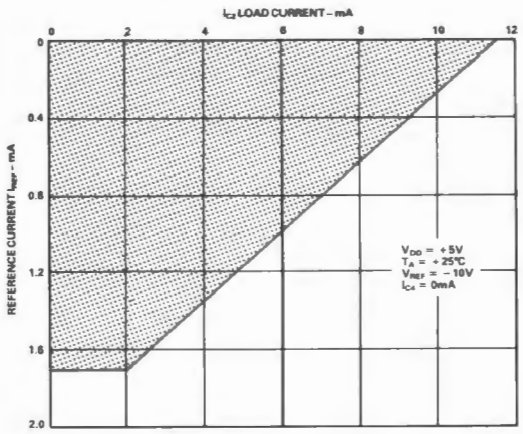


Figure 28 **I_{C4} vs. I_{REF} operating area (shaded) for V_{REF} = –10V** (see Figure 22)

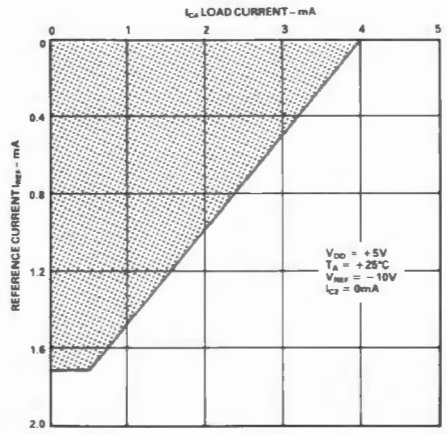


Figure 29 **V_{C4} output voltage vs. V_{C2} output voltage i.e., V_{C4} output voltage as a function of current loading on V_{C2}** (see Figure 21)

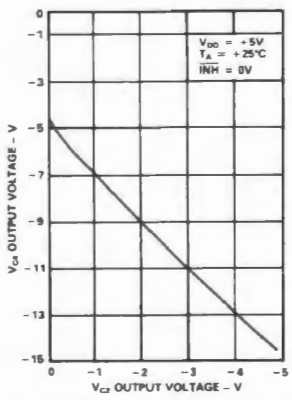


Figure 30 **Effect of INHIBIT input ($\overline{INH}$, pin 1) on converter efficiency**

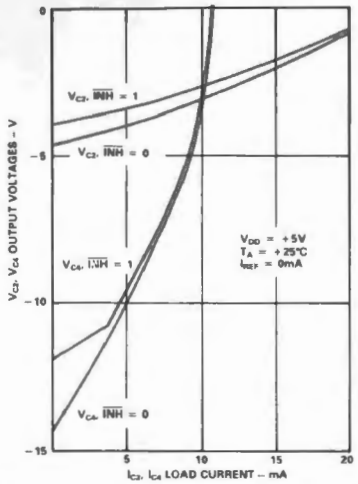


Figure 31 **Typical clock frequency vs. clock capacitance**

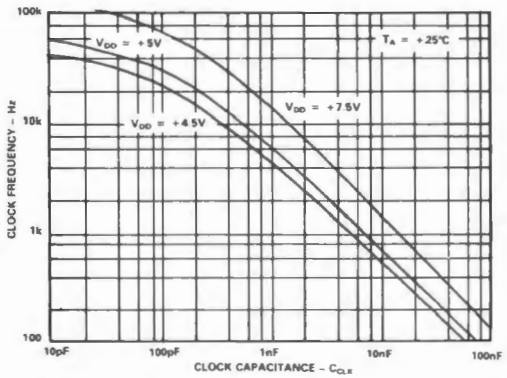


Figure 32. **V_{C2}, V_{C4} and V_{REF} output voltages vs. clock frequency**

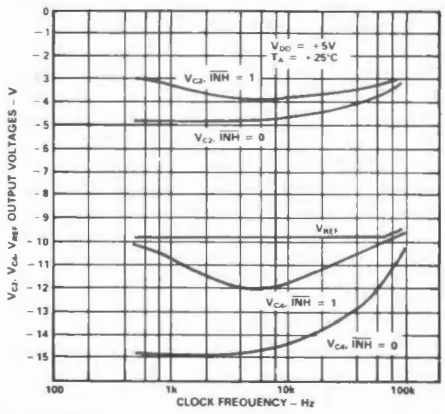


Figure 33. **Power supply current vs. power supply voltage for different values of C_{CLK}**

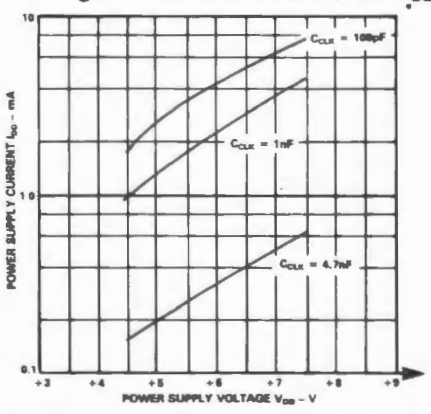


Figure 34 **Power supply current I_{DD} vs. I_{C2}, I_4 and I_{REF} load currents**

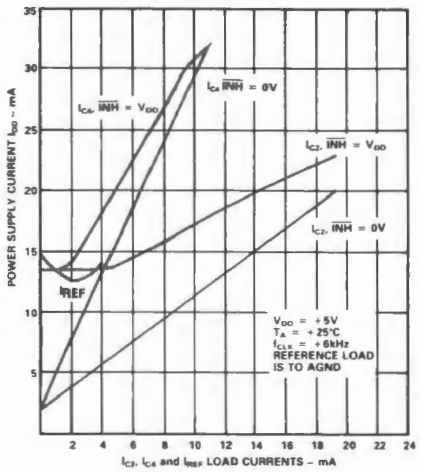
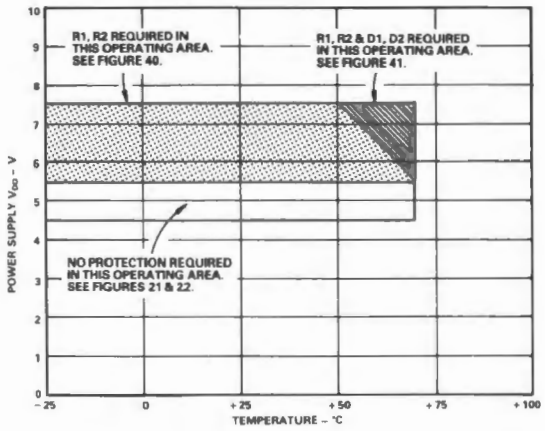


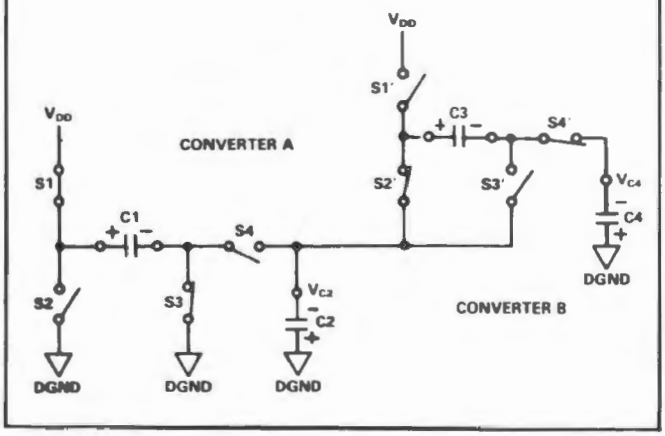
Figure 35 **Operating areas as a function of supply voltage and temperature**



Circuit description

The AD7560 consists of two separate dc-to-dc converters which are driven in series plus a precision voltage reference with buffer amplifier. The voltage conversion circuitry of the AD7560 may be best understood by referring to Figure 36. This shows the two converters A, and B, each comprising four switches and two external capacitors.

Figure 36 **Converter circuitry with external capacitors included**



Consider initially converter A, switches S1 through S4, and capacitors C1 and C2. The oscillator and voltage-level translator sections provide the control signals to the four switches. During the charge phase, capacitor C1 is charged through S1 and S3 (S2 and S4 open) to a voltage equal to the supply voltage V_{DD}. In the pump phase, S2 and S4 are closed (S1 and S3 open) and the charge is pumped or transferred from capacitor C1 to C2. The voltage on C2 (V_{C2}, pins 5 and 13) is equal in value and opposite in polarity to $+V_{DD}$ with respect to DGND (assuming ideal switches and no load on C2). Since a finite time is required after power-on for the voltage to build up across C2 this discussion has assumed that steady state conditions have been reached.

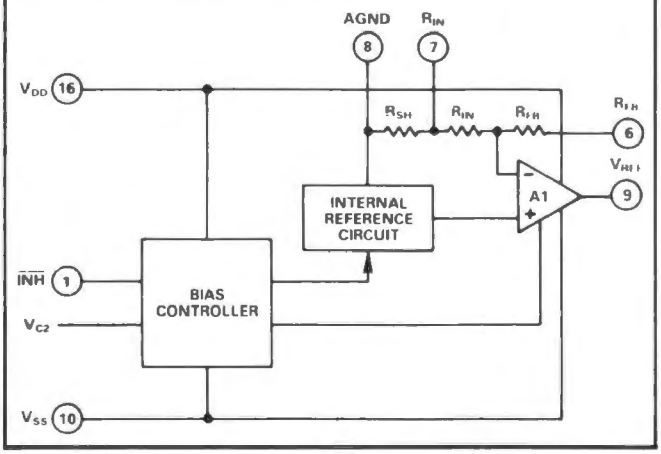
Operation of the second converter is identical with the first except that capacitor C3 is now charged between $+V_{DD}$ and $-V_{DD}$.

This means that during the charge phase capacitor C3 will charge to $(+V_{DD}) - (-V_{DD})$ or $+2V_{DD}$. This voltage is then pumped to capacitor C4. The subsequent voltage on C4 (V_{C4}, pin 11) is ideally $3V_{DD}$ and is negative with respect to DGND. When the first converter is in the charge phase, the second is in the pump phase and vice versa. Converter timing is derived from an on-chip oscillator which can be free-running or synchronized with an externally applied clock.

Figures 23 and 24 in the Typical Performance section show output voltage vs. load current characteristics for converter A (V_{C2}) and converter B (V_{C4}) outputs respectively.

The reference portion of the AD7560 consists of an internal reference voltage circuit and an output buffer amplifier (see Figure 37). Both the reference circuit and the amplifier obtain their bias conditions from a bias controller which is powered by V_{C2} (converter A output) via an internal connection and from an externally applied negative voltage to V_{SS} (pin 10). The amplifier operating current is supplied from V_{DD} and V_{SS}. Normally the voltage output V_{C4} available on C4 (converter B output) is used as the V_{SS} supply. The reference voltage circuit, which is referenced to analogue ground (AGND, pin 8), provides a stable temperature compensated – 5V reference voltage at the non-inverting input of the buffer amplifier A1. R_{IN} and R_{FB} are two thin film resistors with nominal value of 50kΩ each. With R_{IN} (pin 7) tied to AGND and R_{FB} (pin 6) tied to the amplifier output V_{REF} (pin 9), the amplier provides a non-inverting gain of 2 for the internal reference. The amplifier thus supplies a precision reference voltage output of – 10V with a current sink capability of over 1.0mA. The R_{IN} pin is internally tied to AGND via shunt resistor R_{SH} which is approximately equal to 1.5 R_{FB}.

Figure 37 **Reference voltage circuitry**

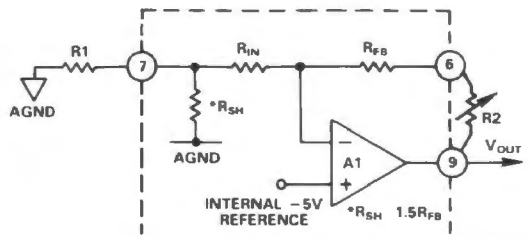


The entire reference voltage circuitry can be powered down via the INHIBIT input (INH, pin 1). This reduces current loading on V_{C2} and V_{C4} and results in increased conversion efficiency of both dc-to-dc converters. See Figure 30 under Typical Performance Characteristics.

Trim techniques

Normal lot-to-lot variations in fabrication will produce devices whose output reference voltages will be distributed symmetrically around – 10.00V. With the addition of one fixed resistor and a potentiometer it is possible to adjust every device to provide a – 10.00V output (see Figure 38).

Figure 38 **Trim resistors for reference circuit**



Trim resistor	AD7560
R1 (Fixed)	10kΩ
R2 (Variable)	20kΩ

R1: thick film metal glaze, tolerance ±2%, TC ±100ppm/°C
R2: 20 turn cermet trimmer, tolerance ± 10%, TC ± 100ppm/C

Table I **Recommended trim resistor values**

The fixed resistor R1 must be sufficiently large (when R2 = 0Ω) to ensure that the output reference voltage of any device is less than –10.00V. Potentiometer R2 is then increased from 0Ω until the reference voltage equals –10.00V. Worst case values of R1 and R2 are indicated in Table I and, therefore, represent the minimum values required which will ensure all devices can be properly trimmed.

In the absence of external gain trim components the output reference voltage is expressed as:

$$V_{REF} = -5 \times \left(1 + \frac{R_{FB}}{R_{IN}}\right) \text{Volts}$$

This reference voltage has a typical temperature coefficient (TC) of 40ppm/°C. The internal thin-film resistors R_{IN} and R_{FB} (and R_{SH}) have typical TCs of –300ppm/°C. However, their matching and tracking is so tight as to produce no appreciable effect on the output TC.

The inclusion of external gain trim components R1 and R2 (as shown in Figure 38) modifies the overall reference performance since these external trim resistors will have different TCs from the internal thin-film resistors. The lowest values possible for R1 and R2 should be chosen in order to minimise their effect on the overall reference TC. To obtain the lowest possible reference TC the most suitable technique for reference trimming is a 'select on test' approach to choosing R1 and/or R2 as opposed to potentiometer trimming.

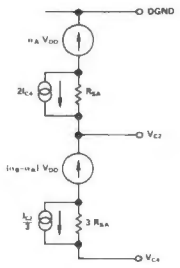
Referring to Figure 38, if pins 6, 7 and 9 are connected together – omitting R1 and R2 – ampli-

fier A1 is configured as a unity gain buffer amplifier making the internal –5V reference available externally. However, the current loading capability of the V_{C4} output is not appreciably increased over normal –10V reference conditions.

Output voltage calculation

Since the two converters (A and B), are driven in series, current loading on either of the two storage capacitors will reduce both output voltages, V_{C2} and V_{C4}, as well as the overall converter efficiency. An approximate equivalent circuit for the converter outputs is shown in Figure 39.

Figure 39 **Equivalent circuit for V_{C2}, V_{C4} outputs** (see Figure 21)



The output voltages using this equivalent circuit and under moderate current loads can be calculated as follows:

$$V_{C2} = -\alpha_A V_{DD} + I_{C2} R_{SA} + 2 I_{C4} R_{SA}$$

$$V_{C4} = -\alpha_B V_{DD} + 2 I_{C2} R_{SA} + 6 I_{C4} R_{SA}$$

Where: α_A is converter A conversion factor, typically $\alpha_A = 0.95$

$$\alpha_A = \frac{|V_{C2}|}{V_{DD}}$$

α_B is converter B conversion factor, typically $\alpha_B = 2.90$

$$\alpha_B = \frac{|V_{C4}|}{V_{DD}}$$

I_{C2} = External current load on C2

I_{C4} = External current load on C4

R_{SA} = Converter A output source resistance $R_{SA} = 120\Omega$ typically.

If only converter B output is loaded the previous expression simplies to:

$$V_{C4} = -\alpha_B V_{DD} + 6 I_{C4} R_{SA}$$

which is the analysis of a voltage source, $\alpha_B V_{DD}$, with an output impedance of $6R_{SA}$. Refer to the relevant current-voltage characteristics shown under Typical Performance Characteristics.

Voltage conversion efficiency

The efficiency of the dc-to-dc converters depends upon the switching transient losses which occur during the conversion cycles. These losses increase with increasing supply voltage V_{DD} and with increasing oscillator frequency f_{CLK}. Figure 33 shows typical power supply current I_{DD} vs. power supply voltage V_{DD} for different values of clock capacitor. The choice of values for the pump and reservoir capacitors for both converters depends primarily on the required output current loading and the peak-to-peak output voltage ripple. The AD7560 is specified with C1 = C2 = C3 = C4 = 10μF and a clock frequency of 6kHz as per the test circuit of Figure 21. The efficiency is relatively constant and optimal over a clock frequency range from 2kHz to 20kHz as indicated in Figure 32 which shows the converter output voltages as a function of clock frequency with fixed values for C1 to C4. If maximum efficiency is required at clock frequencies other than 6kHz, then the value of the pump and storage capacitors must be changed to ensure that the capacitive load impedances remain constant, ie, if the clock frequency is reduced from 6kHz to 600Hz (a reduction of 10) then C1 to C4 values should be increased by 10 (from 10μF to 100μF). Note that the pump frequency is always one half the clock frequency at pin 15.

Clock frequency control

The conversion cycle time (charge and pump phases) of the dc-to-dc converters may be derived from the on-chip oscillator or else controlled by an externally applied clock signal.

1. External clock capacitor: when the clock input (CLK, pin 15) of the AD7560 is left open circuit, the internal oscillator runs at a typical rate of 50kHz. This frequency is lowered by connecting an external capacitor between CLK and V_{DD} or between CLK and DGND.

2. External clock signal: the internal oscillator can be overridden by an externally applied clock signal. The clock input of the AD7560 is 5V CMOS compatible and sources or sinks typically 15μA of input current. The mark/space ratio of the external clock can be highly asymmetric; minimum clock HIGH level (or LOW level) requirement is 5μs. The conversion phases change state on the negative going edge of the clock signal.

Inhibit input

As mentioned in the circuit description section, the reference and amplifier circuitry of the AD7560 obtains bias and operating current from the converter outputs – internally from converter A and externally (via V_{SS}) from converter B. This total current load is constant and is typically 3.5mA. Note that this 3.5mA includes any reference current that the reference amplifier sinks. In applications where the reference output voltage is not required, this current load can be reduced to negligible values by applying a logic LOW to the inhibit input ($\overline{INH}$, pin 1). The effect of the inhibit control on voltage conversion efficiency is evident from the performance characteristics as shown in Figure 30.

Internal circuit protection

Referring to Figure 36, the MOS switches of both converters S3, S4 and S3', S4' are N-channel devices. During normal charge and pump cycles and also during power-up and output short circuit conditions (see following section), the voltages on the sources and drains of these output transistors vary in amplitude and polarity. To ensure optimum transistor performance (ie., low R_{ON} and substrate reverse biased with respect to source) under any condition, their substrates must be tied to the most suitable negative potential available. To achieve this, a section of the internal control logic is devoted to sensing the voltages on the transistor sources and drains, and ensuring that their substrates are always correctly biased. This technique prevents the AD7560 from latching up during power-up and overload conditions, and also ensures optimum efficiency of both dc-to-dc converters.

Operation at high voltages and elevated temperatures

Under normal specified conditions, the AD7560 operates efficiently over its full temperature and supply voltage ranges. If any one of the external capacitors short circuits or if the V_{C2} or V_{C4} output is shorted to any low impedance point (eg., V_{DD} or DGND) the AD7560 internal protection circuitry mentioned previously acts to prevent SCR action and to avoid device destruction. If the AD7560 is to operate under a combination of temperature/supply voltage conditions, as shown in the shaded areas of Figure 35, then external protection circuitry is required both to ensure device operation and, in the event of a short circuit occuring, to preclude device destruction.

Figure 40 shows the protection circuitry required when operating in the dotted area of Figure 35. Due to the inclusion of R1 in series with the V_{C2} output on pin 5, the V_{C2} output on pin 13 should not be used.

Figure 40 **Location of protection components R1, R2 required for operation in dotted area of Figure 35**

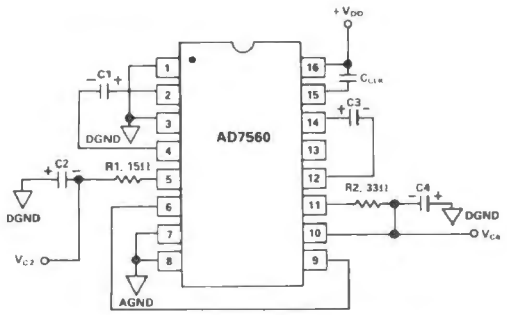
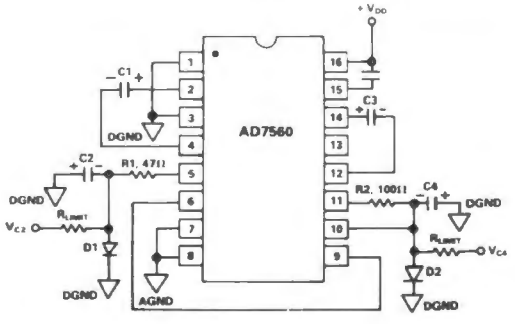


Figure 41 shows the protection circuitry required when operating in the lined area of Figure 35. Under these conditions of high temperature/high voltage, if the V_{C2} or V_{C4} output is shorted to V_{DD}, the internal parasitic transistors may be turned on leading to SCR action and possible device destruction. Diodes D1 and D2 ensure that the V_{C2} and V_{C4} outputs are never pulled higher than a diode drop above DGND. Note that these diodes will require current limiting protection via the R_{LIMIT} series resistors.

Figure 41 **Location of protection components R1, R2 and D1, D2 required for operation in lined area of Figure 35**



Note that none of the above external protection is required when operating the AD7560 within specified limits of $+4.5 \leq V_{DD} \leq +5.5V$ at any temperature over its $-25°C$ to $+70°C$ range.

Applications information

The AD7560 can be used in a multitude of configurations to suit different requirements and applications. Table II outlines some of these operating configurations.

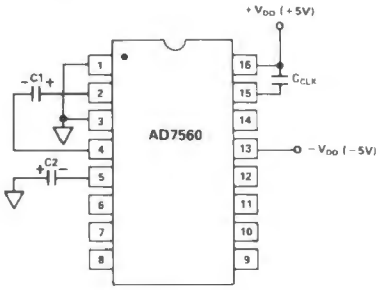
Figure	Input voltage	Nominal output voltages
42	+5V	−5V
43	+5V	−5V, −15V
44	+5V	−5V, −15V, −10V Reference
45	+5V	−5V, +10V
46	+5V	−5V, +15V
47	+5V	−5V, −15V, +10V
48	+5V	−5V, −15V, +15V
49	+5V	−5V, −15V, −10V, −10V Reference
50	+5V	−5V, −15V, +15V, −10V Reference

Table II. **Typical AD7560 operating configurations**

+ V_{DD} In, $-V_{DD}$ Out (Figure 42)

Figure 42 shows the circuitry required for single voltage conversion. C1 and C2 are standard 10μF/10V electrolytic capacitors. See Figure 23 for typical performance characteristics.

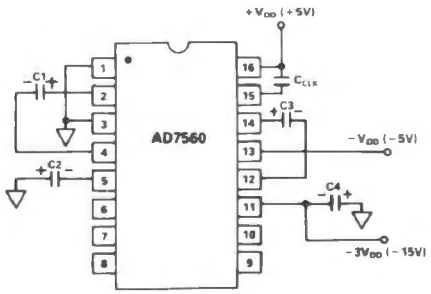
Figure 42 **+V_{DD} to −V_{DD}**



+V_{DD} In, $-V_{DD}$ and $-3V_{DD}$ Out (Figure 43)

Figure 43 shows the circuitry required for voltage conversion and negative voltage multiplication. Capacitors C1 and C2 are 10μF/10V, capacitors C3 and C4 are 10μF/25V. All are standard low cost electrolytic types. Typical performance characteristics are shown in Figure 24.

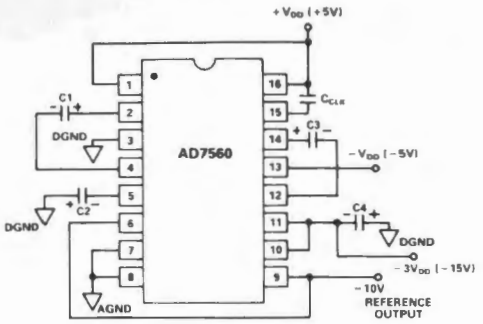
Figure 43 **+V_{DD} to −V_{DD} and −3V_{DD}**



+V_{DD} In, $-V_{DD}$, $-3V_{DD}$ and −10V Reference Out (Figure 44)

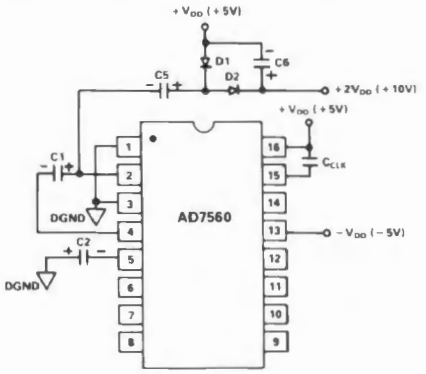
To allow the voltage reference circuit to operate, the inhibit input ($\overline{INH}$, pin 1) is tied to V_{DD}. The feedback loop of the internal buffer amplifier is closed by typing R_{FB} (pin 6) to V_{REF} (pin 9). The amplifier input resistance R_{IN} (pin 7) is tied to AGND (pin 8) to provide a gain of +2 for the internal −5V reference (see Figure 44).

Figure 44 $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $-10V$ reference output



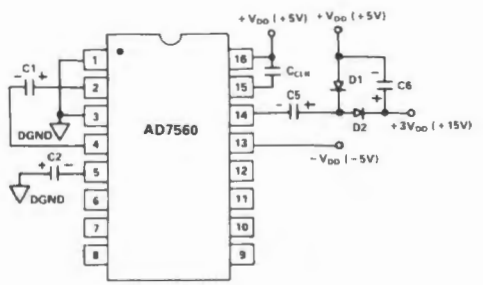
$+V_{DD}$ In, $-V_{DD}$, $+2V_{DD}$ Out (Figure 45)
Positive voltage multiplication is possible using a diode pump scheme as shown in Figure 45. In this configuration, the input capacitor (C5) of the diode pump is switched between $+V_{DD}$ and DGND by the action of converter A. During its pump phase (pin 2 at AGND) C5 is charged to $+V_{DD} - V_F$ (where V_F is the forward diode drop of D1). During the charge phase (pin 2 at $+V_{DD}$) the voltage on C5 plus the supply voltage is applied through D2 to capacitor C6. Thus the output voltage on C6 is $+2V_{DD} - 2V_F$.

Figure 45 $+V_{DD}$ to $-V_{DD}$ and $+2V_{DD}$



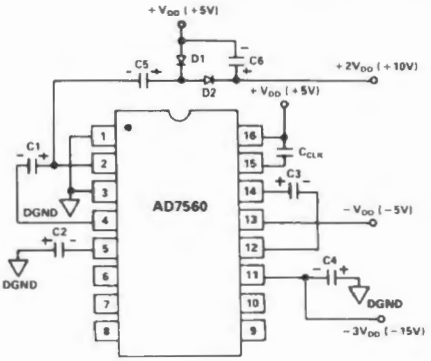
$+V_{DD}$ In, $-V_{DD}$, $+3V_{DD}$ Out (Figure 46)
In this configuration, multiplication of $+V_{DD}$ to $+3V_{DD}$ is achieved by switching the input of the diode pump capacitor (C5) between $+V_{DD}$ and V_{C2}. During the pump phase of converter B capacitor C5 is charged to $+V_{DD} + V_{C2} - V_F$ (where V_F is the forward diode drop of D1). During the charge phase the voltage on C5 plus the supply voltage is applied through diode D2 to capacitor C6. The output voltage on C6 is thus $2V_{DD} + V_{C2} - 2V_F$. Capacitors C5 and C6 are $10\mu F/25V$.

Figure 46 $+V_{DD}$ to $-V_{DD}$ and $+3V_{DD}$



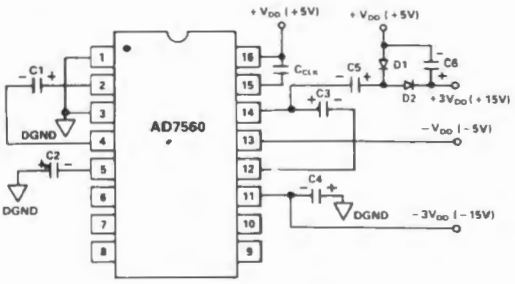
$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$ and $+2V_{DD}$ Out (Figure 47)
This configuration uses both converters and a diode pump. Driving the diode pump input capacitor from +C1 (pin 2) provides positive voltage doubling as explained in conjunction with Figure 45.

Figure 47 $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$, and $+2V_{DD}$



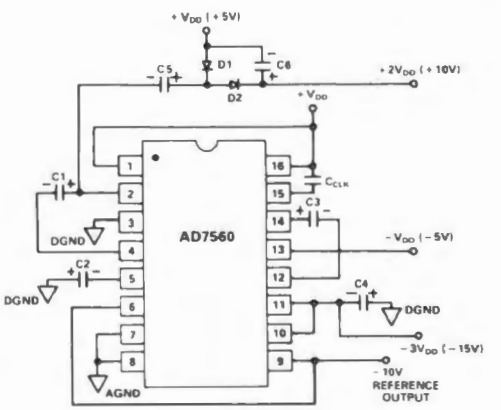
$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$ Out (Figure 48)
This circuit is similar to Figure 47 except that the diode pump is now driven from +C3 (pin 14). This provides voltage trebling as explained in conjunction with Figure 46.

Figure 48 $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$



$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$, $+2V_{DD}$ and $-10V$ Reference Out (Figure 49)
The configuration shown in Figure 49 uses both converters, reference circuit and diode pump to provide multiple analogue outputs.

Figure 49 $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+2V_{DD}$ and $-10V$ Reference Output

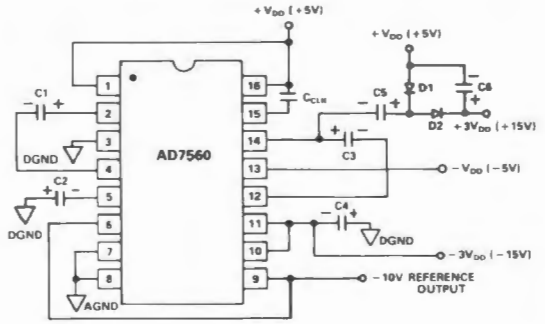


RS data

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$, $+3V_{DD}$ and $-10V$ Reference Out (Figure 50)

This circuit is similar to Figure 49 except that the diode pump is now driven from +C3 (pin 14) to provide positive voltage trebling (see Figure 50).

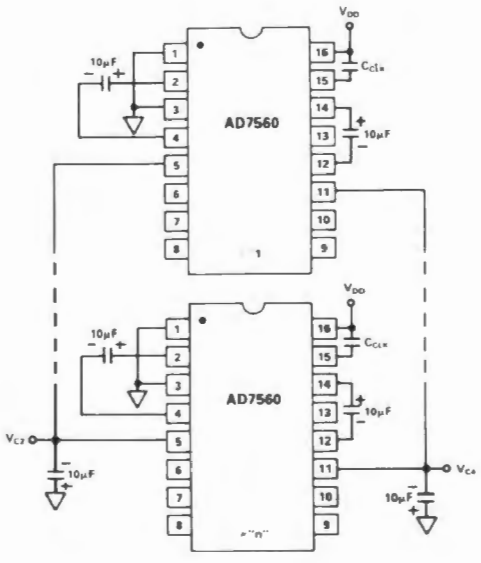
Figure 50 **$+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$ and $-10V$ Reference Output**



Increasing output current capability

It is possible to run two or more AD7560s in parallel to reduce the output resistance of both V_{C2} and V_{C4}. Figure 51 shows the circuit connections. Each converter has its own pump capacitor while the respective storage capacitors are common. The resultant output resistance of either converter A or converter B is approximately equal to that of a single device divided by the number of devices paralleled.

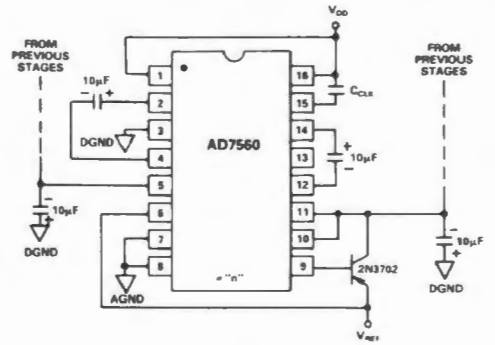
Figure 51 **Paralleling devices to increase output current capability**



Each AD7560 in Figure 51 is shown with an individual clock capacitor. Thus each device runs independently at a different conversion frequency leading to increased noise in the reference voltage output. To reduce the generated noise to a minimum drive all CLK inputs in parallel from a common clock signal.

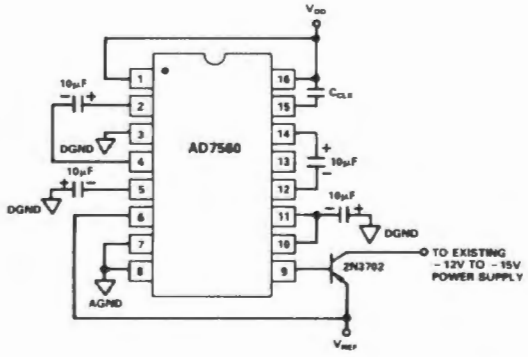
The reference voltage output can also benefit from the paralleling of devices. Figure 52 shows how the final AD7560 (eg., device # "n" in Figure 51) should be connected to boost the available reference current. For example, with two devices in parallel the typical reference current is increased to over 5mA.

Figure 52 **Reference current boosting**



Note that this reference current boosting technique may also be used with existing –12V to –15V power supplies. Using the single general purpose PNP transistor as indicated in Figure 52 and an existing –12V power supply, one AD7560 can control up to 200mA of reference current (see Figure 53).

Figure 53 **Reference current boosting using existing –12V to –15V power supply**



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Issued July 1985 4254

RS data

Programmable clock/ timer i.c. TMS 1601A

Stock number 308-821

The RS programmable clock/timer i.c. is a dedicated mask programmed microcomputer which has been designed as the basis of a versatile timing unit. In the normal mode the unit is a 24 hour 7 day timer; however use of the reset function allows any period cycle up to one week to be followed. Four independent switch outputs are available which can be used to control a wide range of peripherals with the correct interface circuitry.

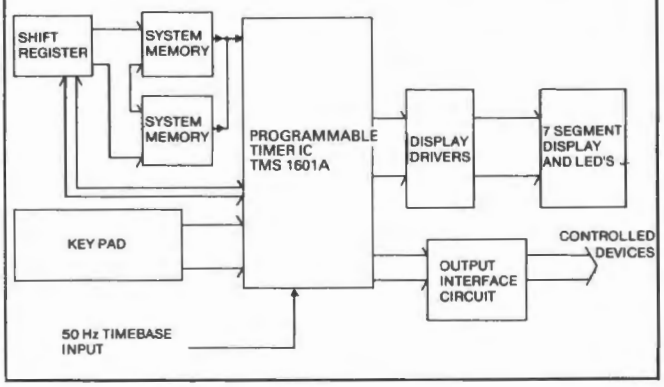
Absolute maximum ratings

Supply voltage, V_{DD} ——— −15V to 0.3V
Data input ——— −15V to 0.3V
Indicator outputs to buffers
average output current ——— −24mA
Indicator outputs to buffers
peak output current ——— −48mA
Row outputs average output current ——— −14mA
Row outputs peak output current ——— −28mA
Switch outputs average output current ——— −14mA
Switch outputs peak output current ——— −28mA
Continuous power dissipation ——— −600mW
Operating temperature range
(in free air) ——— 0°C to 70°C
Storage temperature range ——— −55°C to 150°C
(All voltages with respect to V_{SS})

Features

- 112 Daily switching functions
- 112 Weekly switching functions
- 4 switch outputs interface to thyristor, triac drives etc
- 4 digit 7 segment display to indicate real time, turn on-off times and reset times
- Individual outputs to drive day of week, switch and status LED's
- Reset function allows continual or manually initiated time looping from minutes up to one week
- Period feature to calculate and enter turn off time when an on period is entered
- Memory view facility
- Memory clear allowing total or specific switch deletions for correcting errors etc
- Data entry from a matrix keypad
- Manual control of any output

Block diagram of programmable timer system

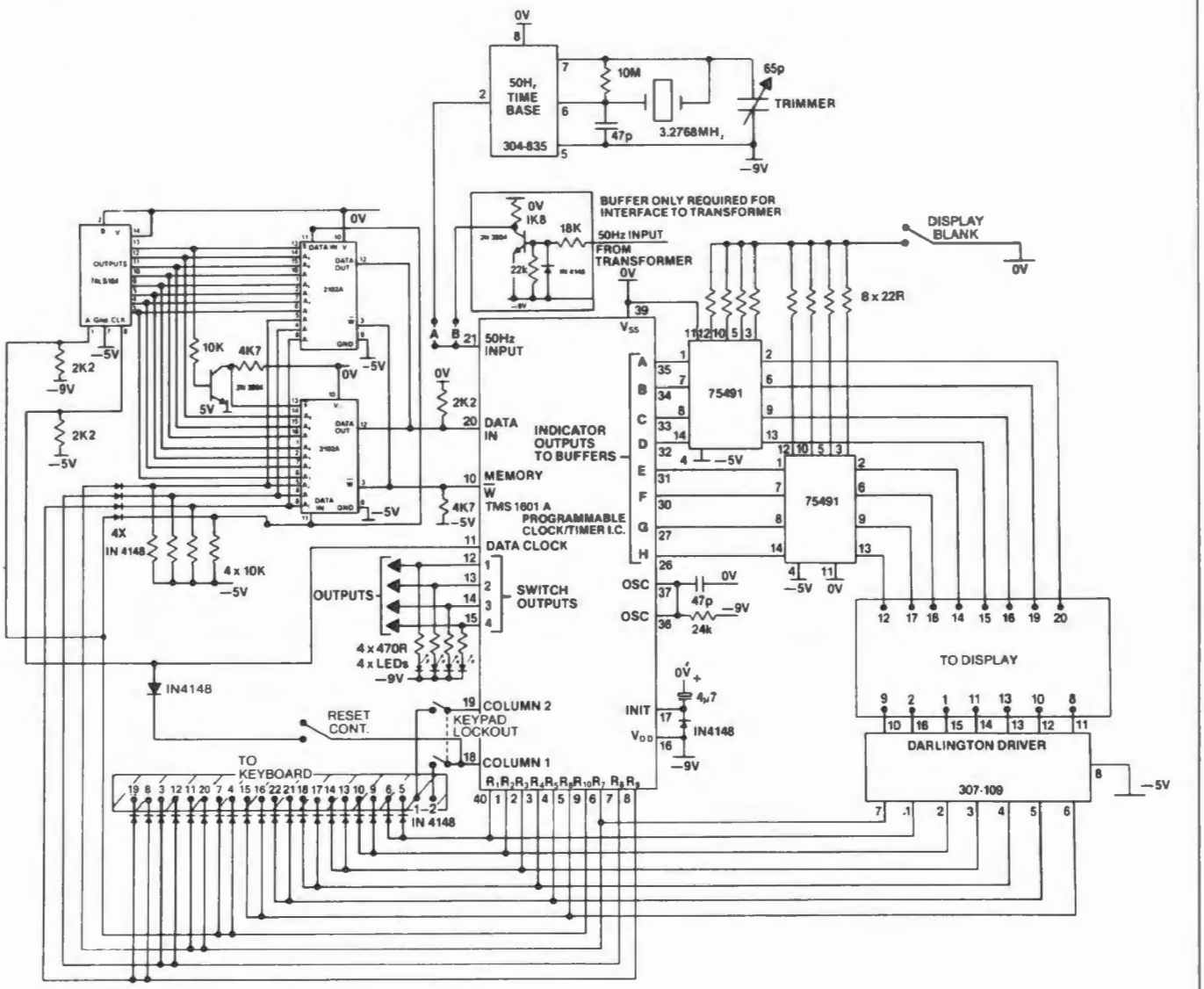


Electrical characteristics $T_A = 25°C$ $V_{DD} = -9V$

* Indicator outputs

Parameter	Conditions	Min	Typ	Max	Units
Supply voltage, V_{DD}		−7.5	−9	−10.5	V
Input current (COLUMN, DATA IN, 50Hz IN)	$V_I = 0V$	70	180	400	μA
High level output voltage	$I_O = -5mA$	−1.7			V
Low level output current	$V_{OL} = V_{DD}$		300 (900)		μA
Average supply current from V_{DD}			17		mA
Average power dissipation			153		mW
Internal oscillator frequency		500		550	kHz
Small signal input capacitance (COLUMN, DATA IN, 50Hz IN)	$V_I = 0V$ f = 1KHz		10		pF

Figure 1 **Main board**



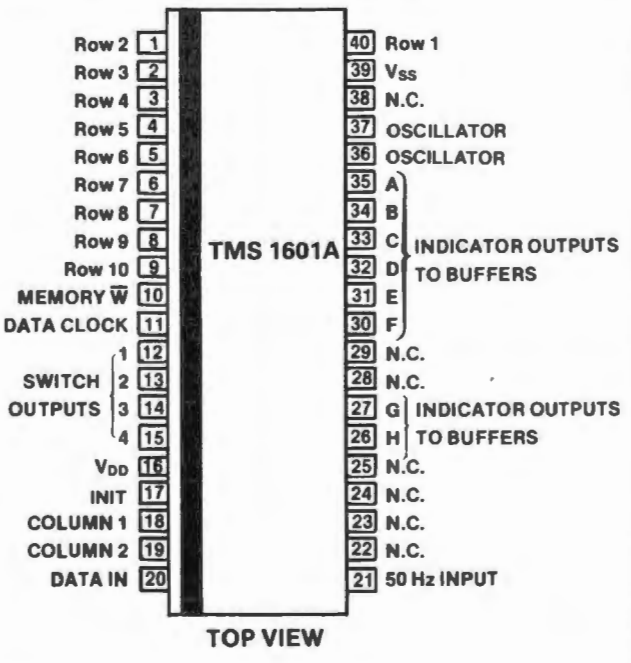


Figure 2 **Keyboard**

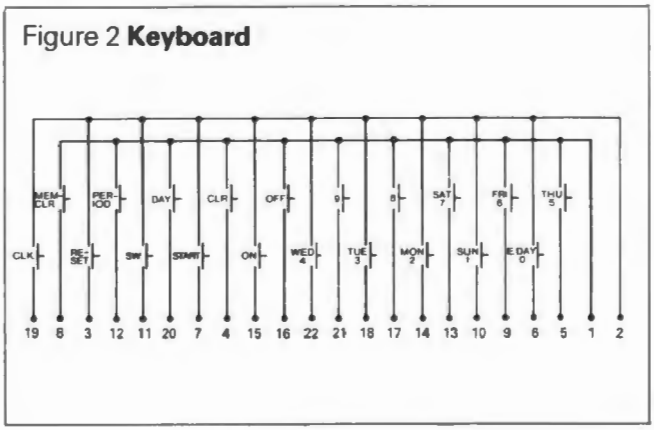
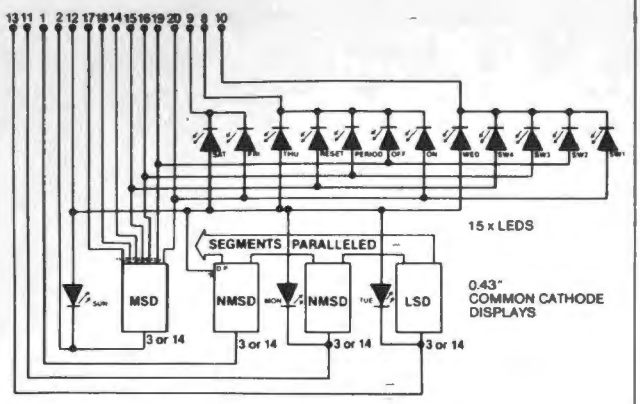


Figure 3 **Display**



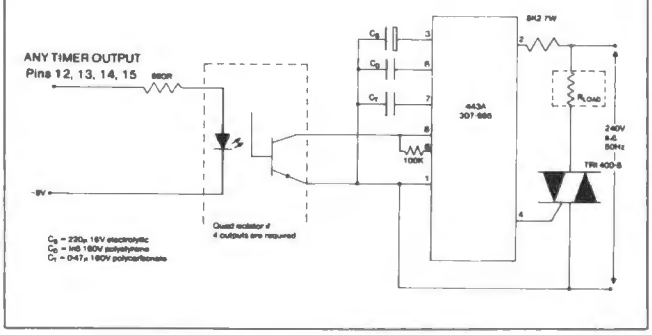
Interface circuits

The following circuits interface between the programmable timer i.c. and the controlled device(s). The circuit chosen will be dependent on the type of load being driven.

Zero voltage switching using ZVS i.c.

This zero voltage switching circuit can be used in applications requiring a minimum of interference which may be caused by firing the triac at points away from the zero voltage switching point. See data sheet 3611 for further details.

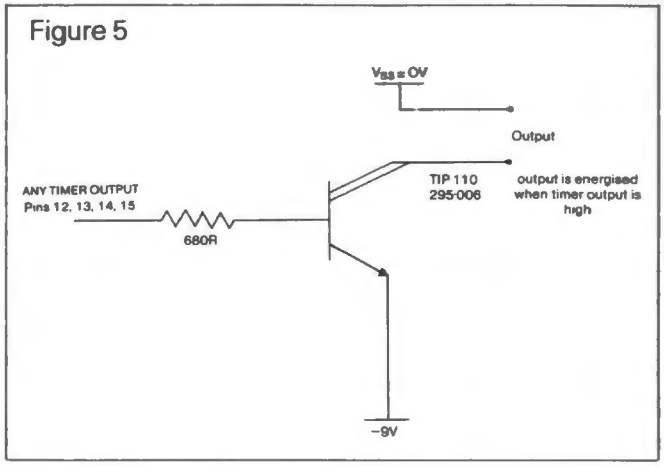
Figure 4



Output switching using a darlington transistor

Simple low voltage switching without isolation may be achieved using a darlington transistor.

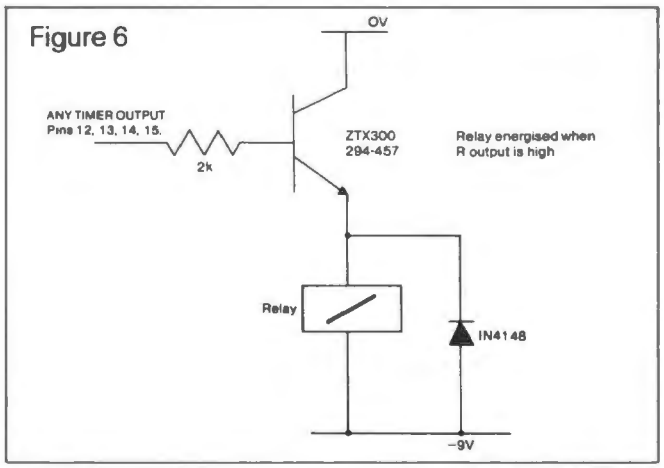
Figure 5



Relay driving circuit

The following circuit uses a relay as the isolating and switching unit.

Figure 6

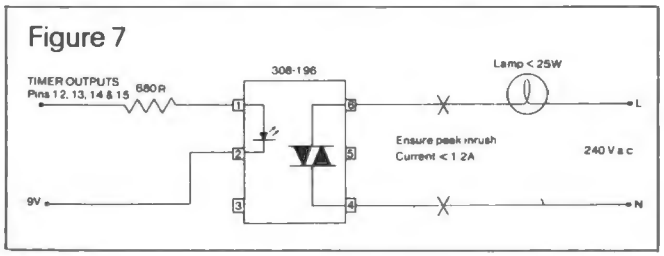


General interface circuits

These circuits form triac interfaces with optical isolation of the load from the timer circuit.

Opto-coupled triac (see data sheet 3958) for direct low power switching.

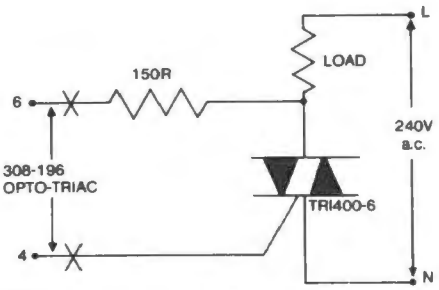
Figure 7



If larger load currents are required, use one of the following two circuits at points X–X.

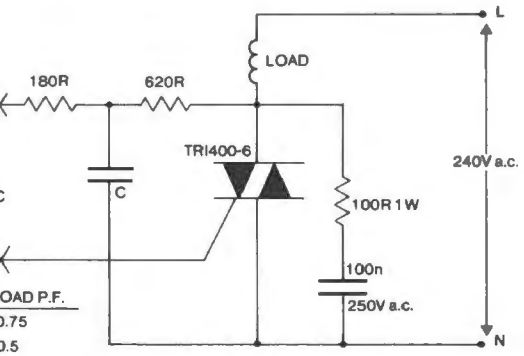
Resistive load

Figure 8



Inductive load

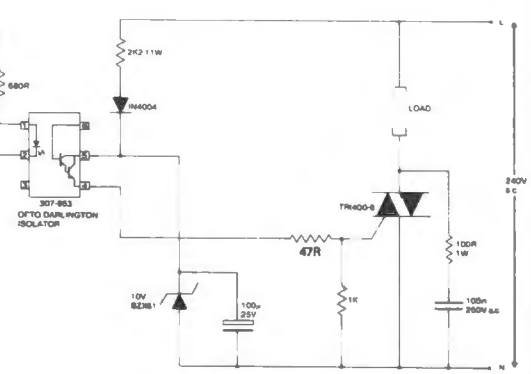
Figure 9



C	LOAD P.F.
220n	0.75
330n	0.5

Additional triac interface circuit

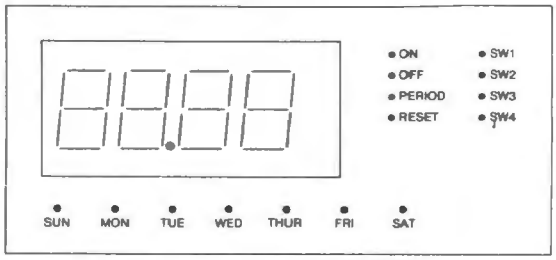
Figure 10



Programming guide

The following display layout is recommended and will be used throughout this data sheet.

Figure 11



The following symbols will be used

● = LED illuminated ☼ = LED flashing

Data entry	Key operation	Resultant display
Clock setting		**Eg. set clock to Monday 9.30**
On initial power up the display flashes up 8's and the Friday LED is illuminated. The clock key is depressed which sets the timer into the default mode of Sunday 00.00, all switches are in the off state. Depressing the day key starts the day LED's flashing. Day and time is then entered.	Apply power	☼☼☼☼ ● FRI
	Clock	0 0 0 0 ● SUN
	Day	☼ ☼ ☼ ☼ ☼ ☼ ☼ SUN MON TUE WED THU FRI SAT
	Monday	0 0 0 0 ● MON
	9	0 0 0 9 ● MON
	3	0 0 9 3 ● MON
	0	0 9 3 0 ● MON
When the clock key is depressed this causes the clock to start counting and is signified by the colon flashing at ½Hz, thus allowing synchronisation to a time signal reference.	Clock	0 9 ☼ 3 0 ● MON

Setting switching times

The timer has four independent switches which can be controlled by settings stored in the system memory or by manual instructions. Each switch can have up to 28 on/off times for operation on a weekly basis and 4 which occur every day.

Selects day entry mode and shows which days can be entered by flashing LED's

Enters day

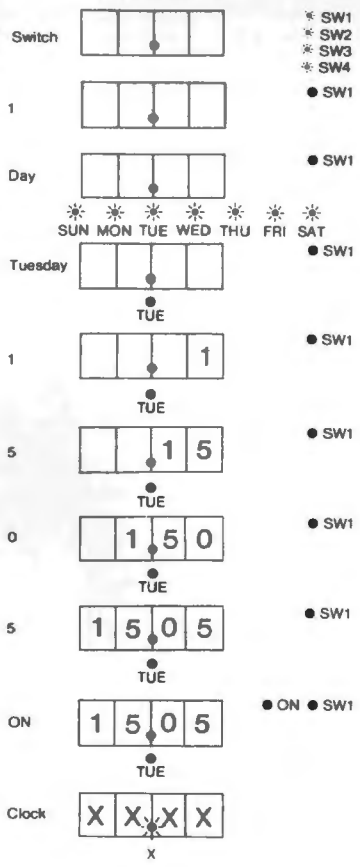
Time entry
(Unlike in the clock mode, leading zero blanking occurs when entering switching times.)

On or off command

Reverts back to real time clock with time and day displayed.

Eg. set switch 1 on at 15.05 Tuesday

Initially in clock mode.



To turn a switch off the same sequence is followed except an off is entered instead of an on.

Selects day entry mode and shows which days can be entered by flashing LED's.

Enters day

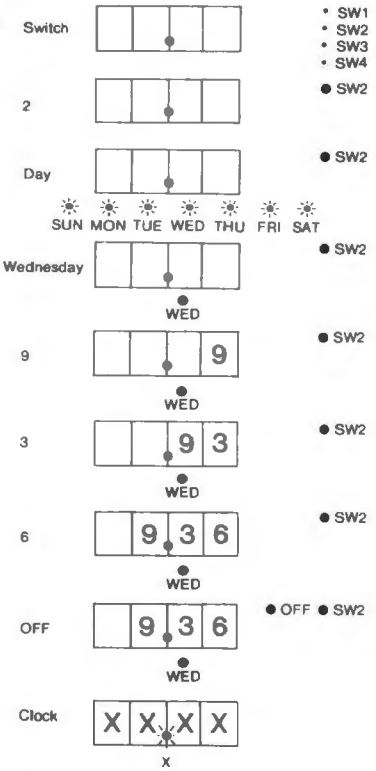
Time entry

On or off command

Display reverts back to a real time clock showing time and day.

Eg. set switch 2 off at 9.36 Wednesday

Initially in clock mode



Direct ON and OFF

Should any of the switchs require direct operation the following method can be used.

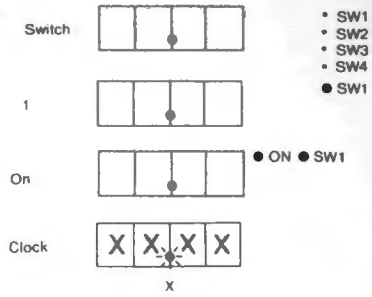
This procedure will directly turn a switch on or off.

On or off entry

Reverts display back to clock and day

Eg. To turn switch 1 on directly

Initially in clock mode



Using Everyday Key To Set Times

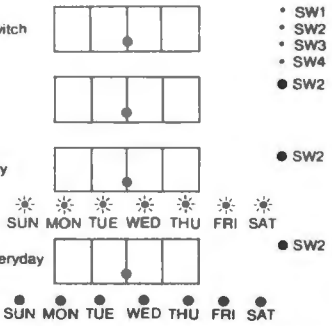
If it is required that a switch operation occurs everyday then use of the everyday key instead of a specific day key should be made.

Selects day entry mode and shows which days can be entered by flashing LED's.

Enters everyday for the operation.

Eg. Operate switch 2 everyday at 8.20

Initially in clock mode



Time entry and on or off is identical to all previous entries.

Multiple entries for one switch on the same day

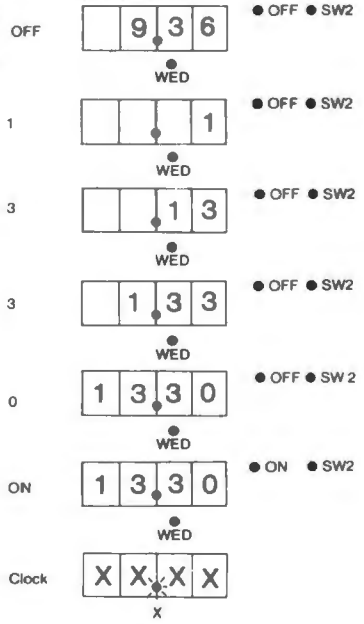
Enter the first setting as previously described but do not revert back to the clock display. Enter next setting time following by on or off command. This may continue until all the required settings have been entered or all of the available memory has been filled. (See note below)

Further entries may now be made.

Reverts back to clock and day display.

Eg. also turn switch 2 ON at 13.30 Wednesday etc.

From above OFF operation



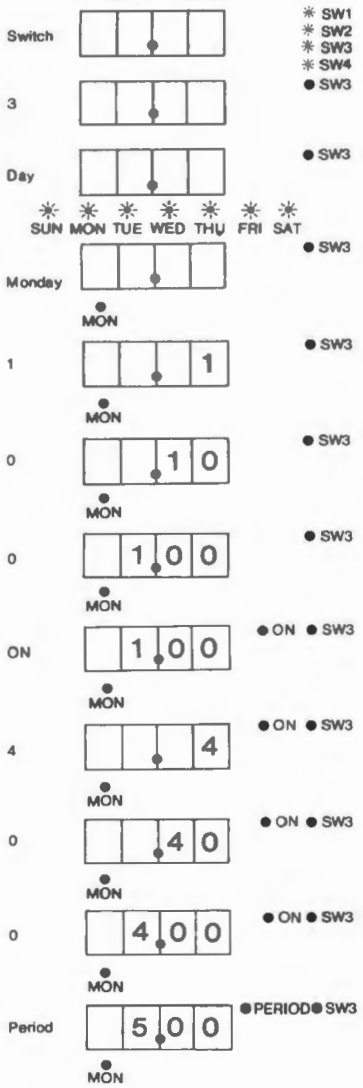
4254

Period setting

Eg. To turn switch 3 on at 1.00 Monday for a period of 4 hours

Initially in clock mode

As an alternative way of entering off times this function may be used. It must occur directly after an on entry where the desired on period is entered. On pressing the period key the correct off time is displayed and stored in the system memory. The maximum period length allowed is 23 hours 59 mins.



Reset setting

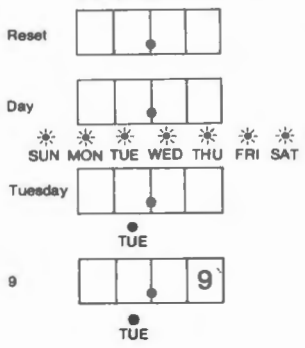
Eg. Set reset time to Tuesday 9.40

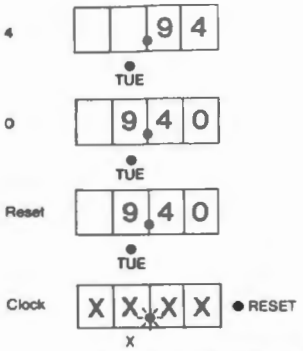
Initially in clock mode

Using the reset setting puts the unit into the timer mode where it will run up to the reset time then either automatically reset to Sunday 00.00 and commence counting again or wait for a start input depending which mode is selected. A reset time from Sunday 00.01 to Saturday 23.59 may be programmed allowing a looping period from 1 min up to 7 days in which all the switches may be used. When a looping period is required enter reset point to give required loop length. Set clock to Sunday 00.00 and start clock when period is required to commence. The reset mode is set with the reset/continuous toggle switch.

Reset continuous (automatic) is effected when the RESET CONT. switch is closed: when open, resetting is effected manually through the RESET key.

Note: all programming features are available during a time loop.





Reverts back to clock and day. Reset LED illuminated, stays illuminated until reset is cleared.

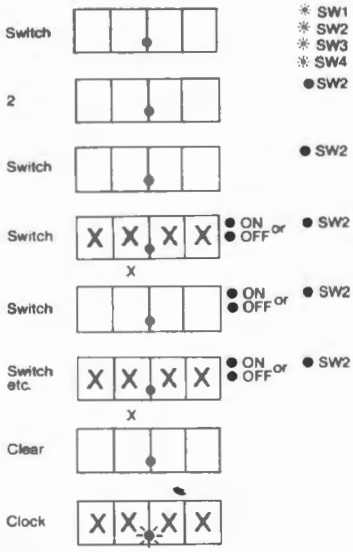
The clock will run until Tuesday 9.40 where it will reset. If continuous reset is selected it will automatically reset to Sunday 00.00 and start counting again. If non-continuous reset is selected it will reset to Sunday 00.00 with the display flashing up zeros and wait there until a start command is given. On pressing the start key the clock will commence counting from Sunday 00.00 until the reset point is reached again.

Memory display

Eg. To display the memory contents of switch 2

Initially in clock mode

To display the memory contents of any of the switches it is necessary to enter into the specific switch mode. Its contents may then be viewed chronologically from Sunday to Saturday by depressing the switch select key. The contents are displayed numerically on every double depression with the single day entries followed by the everyday ones. If no single day entries are present the everyday entries will be shown first. Should no entries be present the display will show 88.88 and all the day LED's will be illuminated.



Reverts back to clock and day.

Clear single memory entries

Enter the memory display mode, obtain the setting to be deleted and press memory clear. The entry will be removed and further sequential viewing and deletions may then be performed.

Note: If only one switching time is stored this cannot be deleted by the above method and must be removed by "clear memory for a specific switch" as shown below or the "clear all memory" operation.

Clear memory for a specific switch

Eg. Clear switch 2 entry

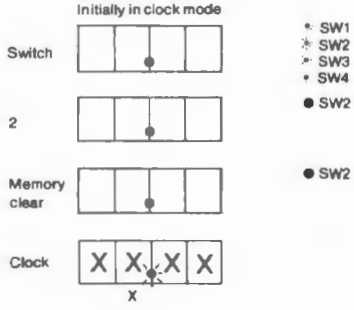
Initially in clock mode

This operation will delete all the entries for a selected switch.

Select switch for which entries need to be cleared.

Clears entries

Reverts back to clock and day.



Clear all memory

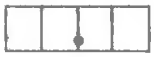
Pressing Memory Clear switch twice clears all the switch on and off times stored in the system memory.

Initially in clock mode

Memory clear

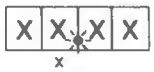
Clear system memory

Memory clear



Reverts back to clock and day

Clock

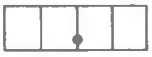


Clear clock

This operation clears the clock setting allowing a new day and time to be entered.

Initially in clock mode

Clear



Press day key followed by day and time as for setting clock.

Display of reset time

To display the reset time it is necessary to enter a double reset with the display initially in the clock mode. The reset time and day will then be displayed. To revert back to the clock press clock once.

Clear reset time

With the timer initially in clock mode the reset time may be deleted by keying reset followed by memory clear. This clears the point where the clock was due to reset to Sunday 00.00 and thus puts the timer into the real time clock condition. A new reset may now be entered if required.

Correction for miss-operation

Should an incorrect data entry be made it is possible to re-write the data before pressing clock, period, reset, ON or OFF.

Errors

Clock setting error

Entry of a clock setting greater than 23.59 will not allow the clock to run when the clock key is pressed. Re-entry of a time less than 24.00 followed by clock will start the timer running.

Memory time setting errors

The timer has provision for 28 on and off times on a weekly basis and 4 on an everyday operation for each switch. If entry of more data is attempted the display will show 88.88 as an overload indication, to revert back to the clock display requires the pressing of clear followed by clock. If a period of greater than 24 hours is entered using the period key the display will show 88.88. It is necessary to enter clear clock and re-enter the data within the restraints given.

Overlapping times

If any switch is instructed to turn on and off at the same time the following priority will take place.
(a) If the switch is already ON then it will turn OFF
(b) If the switch is already OFF then it will turn ON
Should any switch be operating in the period mode and an OFF time is programmed which conflicts with the period ON time, the OFF time will override the period mode making the period shorter. However the period OFF time will still be present in the system memory.

General operating notes

Multiple switching times entry

When entering switching times for the same day one week hence, it may be necessary to safeguard against inadvertently switching the outputs of the *current* day (which will be the *same* day as far as the counter is concerned). To avoid the switches turning on and off as subsequent times are entered, it is necessary to enter times which occur *before* the actual time shown on the clock in reverse order i.e. working backwards to 00.01 hours from the actual clock time. Switching times *beyond* the actual clock time and for other days of the week should be entered in chronological order.

Everyday switch operations

When everyday switch operations are being used and the clock setting is altered to a time earlier in the current week, correct switch operations may not occur until the next day commences.

Display blanking

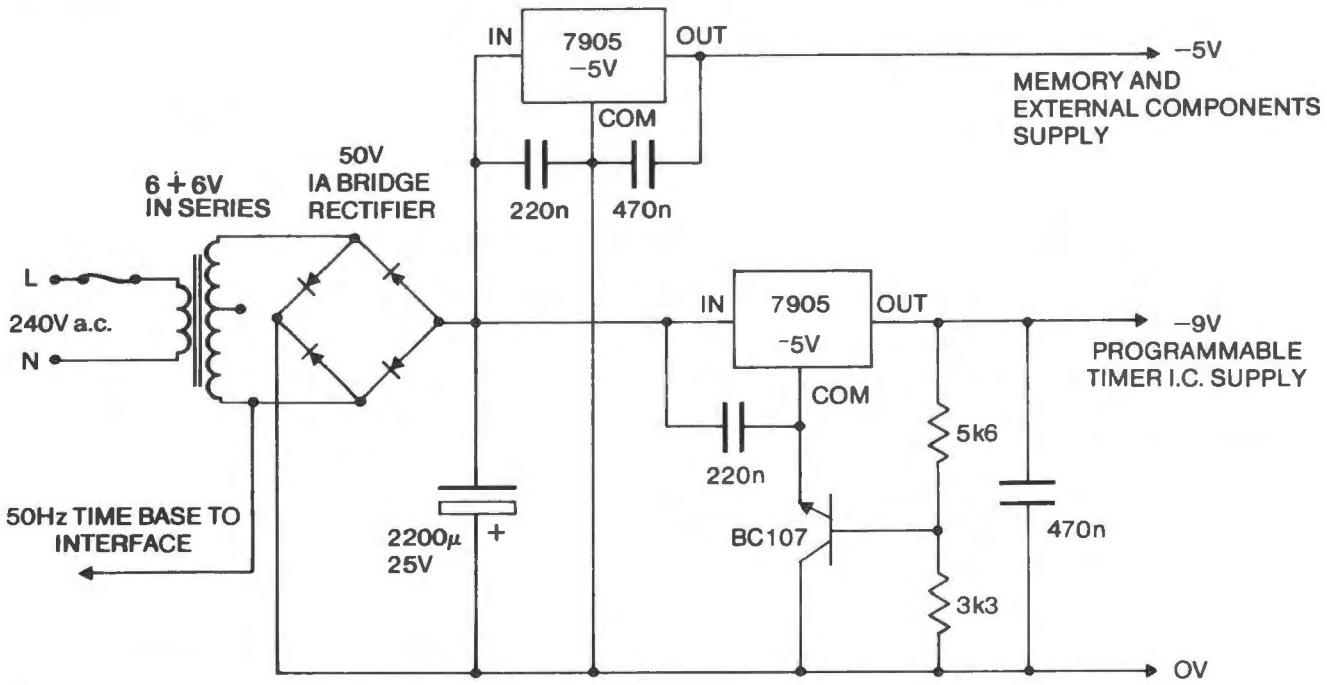
Display blanking for conserving power during battery backup operation may be achieved by inserting a switch in the 0V line to the display current limiting resistors. On opening the switch the display is blanked (see main circuit diagram).

Keypad lockout

Should the entry of data need prohibiting at any time for reasons of security a single pole double throw key switch can be inserted in the column connections as shown on the main circuit diagram. With this switch in the open position the keyboard will be locked out preventing further data entries etc which would alter the timer settings.

RS data

Figure 12 **Power supply for use with programmable timer**



Note: Supply line ripple must not exceed 0.2V peak to peak in the operating frequency range.

List of components

2x	20 way speedbloc Pcb right angle plugs and cable to suit		467-346
2x	20 way speedbloc sockets		467-289
1x	Pcb plug 5 way		467-576
1x	Pcb socket 5 way		467-627
	Crimp terminals		467-598
1x	10 way speedbloc Pcb right angle plug	(optional)	467-330
1x	10 way speedbloc socket	(optional)	467-273
1	Keyboard and connectors		335-182
15x	0.2" LED's High intensity types		587-822
4x	0.43" Common cathode 7 segment displays		587-383
1x	Display bezel 4 digit		587-204
4x	Subminiature LEDs	(optional)	587-721
27x	1N4148 diodes		271-606
2x	2N3904 transistors	(1 optional)	294-312
1x	BC107 transistor		293-527
1x	Darlington driver		307-109
2x	Display drivers 75491		303-157
2x	2102A memories		308-663
1x	50Hz time base i.c.	(optional)	304-835
1x	74LS 164		305-018
1x	TMS 1601A		308-821
1x	1A 50V Bridge rectifier		262-141
1x	3.2768MHz crystal		307-777
2x	7905 −5V regulators		306-049
2x	Heat sinks		401-863
8x	22R high stability carbon film		131-053
4x	470R high stability carbon film	(optional)	131-211
1x	1K8 high stability carbon film		131-283
3x	2K2 high stability carbon film		131-299
1x	3K3 high stability carbon film		131-312
2x	4K7 high stability carbon film		131-334
1x	5K6 high stability carbon film		131-340
5x	10K high stability carbon film		131-378
1x	18K high stability carbon film		131-407
1x	22K high stability carbon film		131-413
1x	24K 0.4W metal film		148-821
1x	10M 0.5W carbon film	(optional)	133-330
1x	65p Trimmer	(optional)	125-660
2x	47p polystyrene	(1 optional)	113-241
2x	220n polyester film		115-118
2x	470n polyester film		115-130
1x	4μ7 35V tantalum		101-793
1x	2200μ 25V elect		105-010
1x	40-pin DIL socket		
3x	18-pin DIL socket		
3x	16-pin DIL socket		
1x	8-pin DIL socket		
1x	Mains transformer		207-633

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RS data

Miniature elapsed time indicator

Stock number 258-164

The RS miniature elapsed time indicator is a small and inexpensive, low power consumption device which is essentially a small sealed mercury electrolysis unit. It consists of a short length of capillary tube with two columns of mercury separated by a droplet of electrolyte. Positioned in the electrolyte is a solid index which ensures mechanical separation of the two columns of mercury when subjected to shock or vibration. Electrical connection to the mercury is made by electrodes mounted on to end caps of a standard 1¼'' glass cartridge fuse case in which the capillary tube is mounted. The device is ideal for mounting into RS fuse holder 412-675, or direct mounting to p.c.b's utilising leads attached to the end caps.

Specification

Maximum d.c. current 85μA
Minimum d.c. current 0.6μA
Maximum full scale time range .....10000hrs.
Minimum full scale time range .....100hrs.
Reading accuracy .....±5%

Operation

When a d.c. potential is connected across the device, current flows through the product and electrochemically transfers mercury from the anode to the cathode. The rate at which mercury is transferred is proportional to the amount of current flowing through the device. Hence, the anode will shorten and the cathode will lengthen, moving the index along the length of tube. If a constant current is used, the amount of mercury electrochemically transferred from anode to cathode is proportional to the length of time the current is applied. Full scale times of 100-10000hrs. may be selected, simply by connecting an appropriate series resistor to limit the current through the device.

Device consumption for 1000hr. full scale travel 2mW.
Device current (d.c.) for a full scale travel of 1000hrs. 6.77μA.
Device current (I_t) for other full scale times is given by:

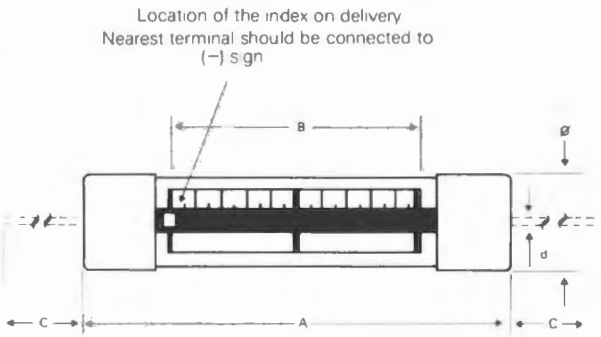
$$I_t = 6.77 \times \frac{1000\mu A}{T} \qquad \text{Eq. 1}$$

where T=required full scale time.

Features

- Low cost
- Reversible
- Low power consumption
- Very small size
- Convenient 1¼'' glass cartridge fuse type package

Dimensions



A ± 1	B ± 0.1	C min.	Ø ± 1	d ± 0.1
32	16.5	40	6.35	0.8

Resetting

To reset the device to zero, apply a reverse polarity current of 85μA.

N.B.
The electrolyte droplet should always be kept within the scale of the device. If the device is allowed to considerably over run the scale range, bringing the electrolyte in contact with one electrode i.e. all of the mercury in one column is transferred to the other, the device will permanently cease to function. However, the devise is normally resettable simply by reversing the polarity of the supply.

RS data

Applications

The device has many uses, some of which are listed below:—

M.T.B.F./reliability measurement

Because of the low cost and small size of these devices, they will find uses where the traditional methods of time recording make the costs uneconomical or overall size/power consumption too high. Thus, it is possible to gain more information concerning life times of individual components or assemblies.

Warranty by actual hours of use

By mounting the product inside a piece of equipment, the device will provide a visual record of actual hours of use. Warranty periods may then by stated realistically in hours of use.

Calibration scheduling and preventive maintenance

Equipment calibration, servicing and preventive parts replacement within specified periods is essential to ensure that the equipment remains within specification during use. Indeed, catastrophic failure of some equipment can result from components being used beyond their normal life expectancy. In some instances, periodic preventive maintenance may be unnecessary when based on calendar days, if the equipment has not been used at times during that period. Therefore, RS miniature elapsed time indicators may be used to accurately determine optimum maintenance periods.

Charge and discharge monitoring

The device operates according to the quantity of electricity passing through the mercury. The increase in length of the mercury column may be defined as follows:

$L = K.C$

where C is in coulombs, and

$K = 1.477$ C/mm.

Repetitive pulse counter

Because the device is essentially a current/time integrator, it may also be used as a pulse counter (provided the pulse width is ≥ 1 mS). The number of pulses per mm travel of the index is given by the ratio $\frac{K}{C}$

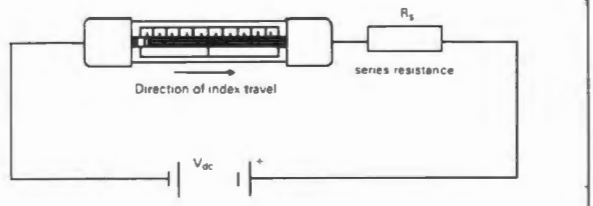
where $K = 1.447$ C/mm and

C is in coulombs

Connection to device

Typical connection:

Figure 1



Series resistor

Example of calculation of series resistor required for full scale time of 2000hrs. and Vd.c. 12 V. From Eq. 1,

$$I_t = 6.77 \times \frac{1000}{2000} = 3.385\mu A$$

$$\therefore R_s = \frac{12}{3.385 \times 10^{-6}} = 3.55\ M\Omega$$

N.B.

Care should be taken not to apply excessive heat to the device when soldering direct to a p.c.b. as damage to the device may occur. If the device is required to operate from an a.c. voltage, a diode should be connected in series with R_s and calculations should be made using the mean value.

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RS data

Reflective and slotted opto switches 2601

Gallium Arsenide infra-red emitting diodes and spectrally matched detectors housed in moulded packages mechanically designed to enable sensing in a variety of applications, i.e. limit switching, paper/tape sensing and optical encoding.

Reflective opto switch
Stock number 307-913

Comprises a Ga As infra-red emitting diode with a silicon phototransistor in a moulded rugged package. The sensor responds to the emitted radiation from the infra-red source only when a reflective object is within the field of view of the sensor. The device is ideal for such applications as end of tape detection, mark sensing, etc. An infra-red transmitting filter eliminates ambient illumination problems.

Absolute maximum ratings at 25°C (unless stated)

Operating temp range	−40°C to +80°C
Storage temp range	−40°C to +80°C
Lead soldering temperature (5 sec)	260°C

Input diode

Forward d.c. current	40mA*
Reverse d.c. voltage	2V
Power dissipation	50mW**

Output sensor

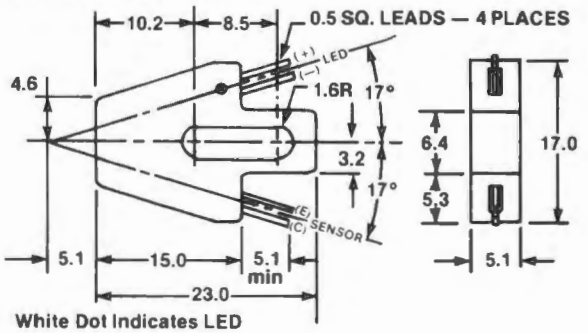
Collector – emitter voltage	15V
Emitter – collector voltage	5V
Power dissipation	50mW**

*Derate linearly 0.73mA/°C above 25°C
**Derate linearly 0.91mW/°C above 25°C

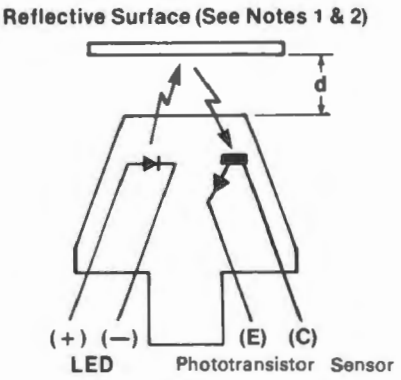
Applications

- Limit switch
- Paper sensor
- Counter
- Chopper
- Coin sensor
- Optical sensor
- Position sensor
- Level indicator

Mechanical details



Electrical details



Electrical characteristics

at 25°C (unless stated)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Input Diode						
V_F	Forward Voltage	—	—	1.8	V	I_F = 40mA
I_R	Reverse Current	—	—	100	μA	V_R = 2V
P_O	Radiant Power	0.5	1.5	—	mW	I_F = 20mA
Output Sensor						
BV_{CEO}	Collector-Emitter Breakdown Voltage	15	—	—	V	I_{CE} = 100μA
BV_{ECO}	Emitter-Collector Breakdown Voltage	5	—	—	V	I_{BC} = 100μA
Coupled						
I_C	Photocurrent (see note 1)	200	—	—	μA	I_F = 40mA, V_{CF} = 5V
I_{CX}	Photocurrent (see note 2)	—	—	20	μA	d = 5mm (see fig. 2)

Typical characteristics

Figure 1 **Output current vs input current**

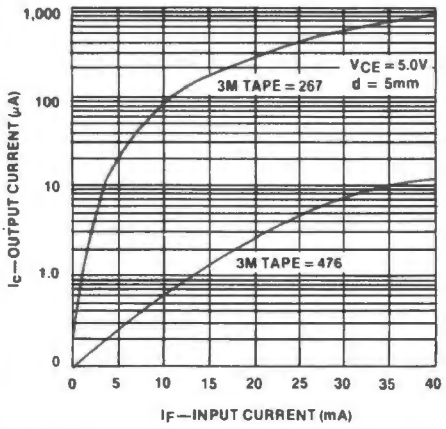


Figure 2 **Output current vs reflective object distance**

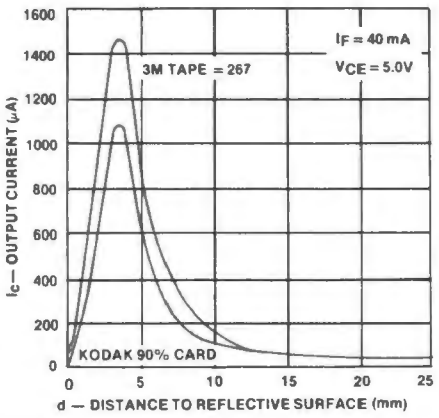
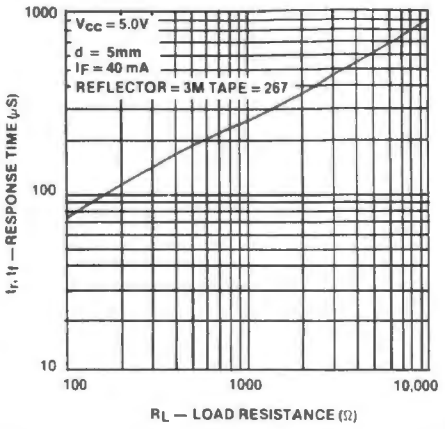


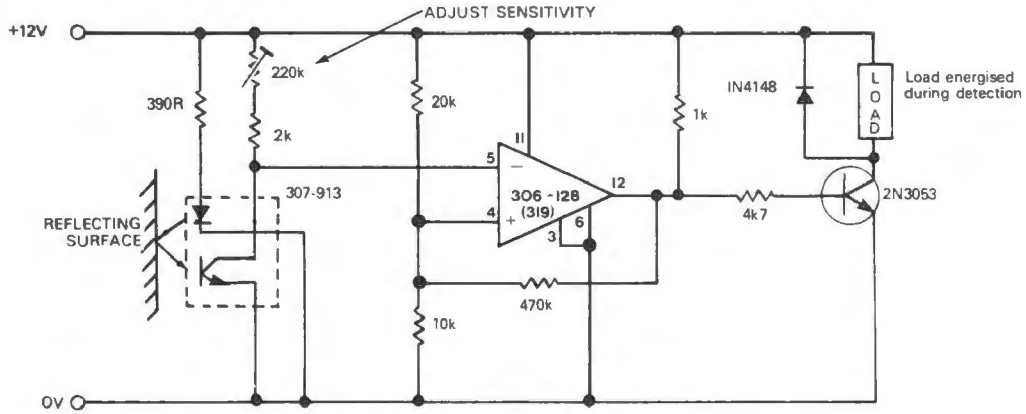
Figure 3 **Nonsaturated switching time vs load resistance**



Note 1: Photocurrent (I_C) is measured using 3M tape = 267 for a reflecting surface. The reflective qualities of 3M tape = 267 are very similar to an Eastman Kodak neutral white test card having 90% diffuse reflectance.

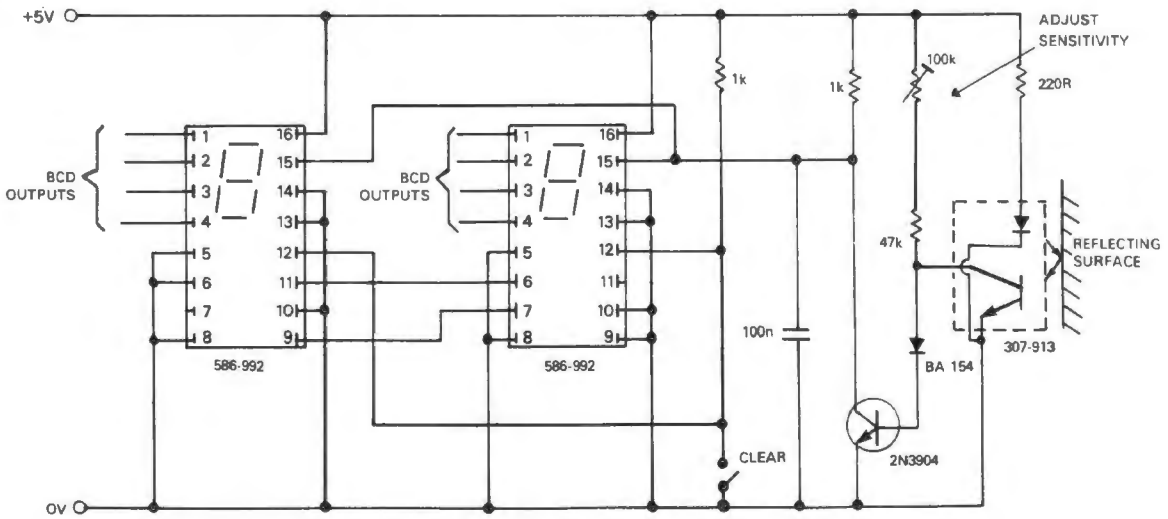
Note 2: Photocurrent (I_{CX}) is measured using 3M tape = 476 for a reflecting surface. 3M tape = 476 has a very black dull surface with optical reflectance qualities comparable to a surface coated with carbon black printers ink.

Figure 4 **Reflective object detection**



Applications

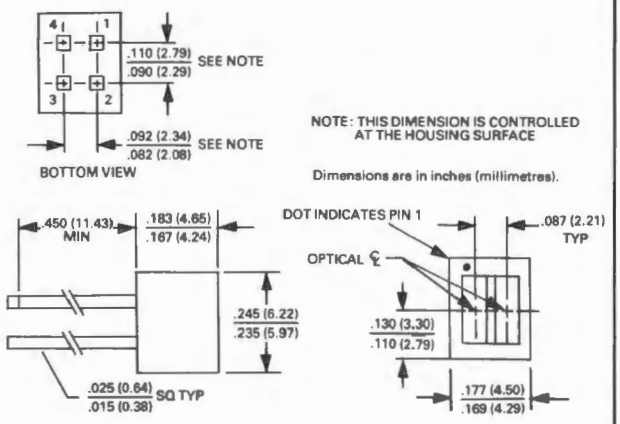
Figure 5 **Reflective object counter**



Miniature reflective opto-switch
Stock number 301-606

Comprises a Ga As infra-red emitting diode and an npn silicon phototransistor mounted side by side on parallel axes and housed in a black plastic moulding to reduce ambient light noise. The photosensor responds to radiation only when a reflective object passes within its field of view.

Figure 6 **Mechanical details**

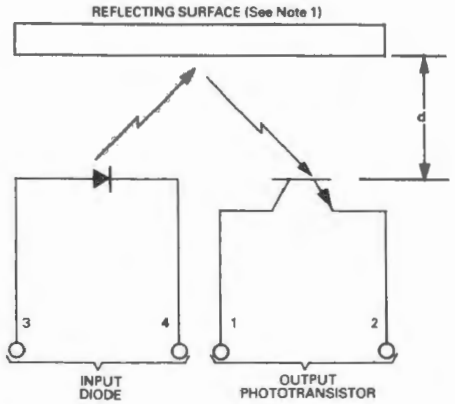


* Cathode lead. Other leads are .06 (1.52) nom. longer.

Applications

- B.O.T. – E.O.T. Sensors
- Line finders
- Batch counters
- Object sensors
- Level indicators

Figure 7 **Electrical details**



Note 1: Photocurrent is measured using an Eastman Kodak neutral white test card having 90% diffuse reflectance as a reflective surface.

Absolute maximum ratings

at 25°C (unless stated)

Operating temp. range	−55°C to + 80°C
Storage temp. range	−55°C to +80°C
Lead soldering temperature (3 secs)	240°C

Input diode

Forward d.c. current	50mA
Peak forward current (pulse width = 1μS, 300p.p.s.)	3A
Reverse d.c. voltage	3V
Power dissipation	75mW*

Phototransistor

Collector-emitter voltage	30V
Emitter-collector voltage	5V
Collector d.c. current	25mA
Power dissipation	75mW*

*derate linearly 1.36mW/°C above 25°C

Electrical characteristics at 25°C (unless stated)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Input Diode						
V_F	Forward Voltage	—	—	1.7	V	$I_F = 20mA$
I_R	Reverse Current	—	—	100	μA	$V_R = 3V$
Photo Transistor						
$V(BR)_{CEO}$	Collector-Emitter Breakdown Voltage	30	—	—	V	$I_C = 100\mu A$
$V(BR)_{ECO}$	Emitter-Collector Breakdown Voltage	5	—	—	V	$I_E = 100\mu A$
I_{CEO}	Collector Dark Current	—	—	100	nA	$V_{CE} = 5$ $I_F = 0$
Coupled						
$I_C(On)$	On-State Collector Current	350	700	—	μA	$I_F = 20mA$ $V_{CE} = 5V$ d = 1.27mm (see Note 2)
I_{CX}	Photocurrent (see Note 3)	—	—	0.20	μA	$I_F = 20mA$ $V_{CE} = 5V$ No reflecting surface

Note 2 d is the distance in mm from the assembly face to the reflective surface.

Note 3 Photocurrent (I_{CX}) is the collector current measured with the indicated current in the input diode and no reflecting surface.

Typical characteristics

Figure 8

Collector Current vs. Diode Forward Current

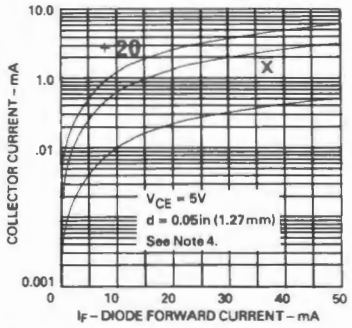


Figure 9

Rise and Fall Time vs. Load Resistance

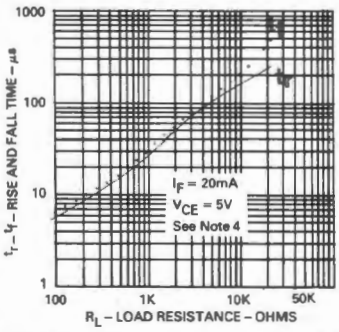
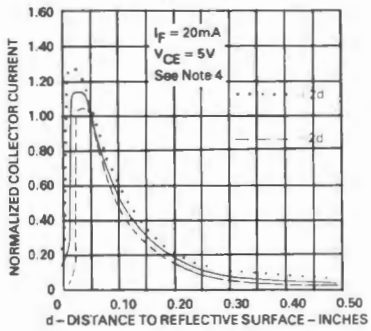


Figure 10

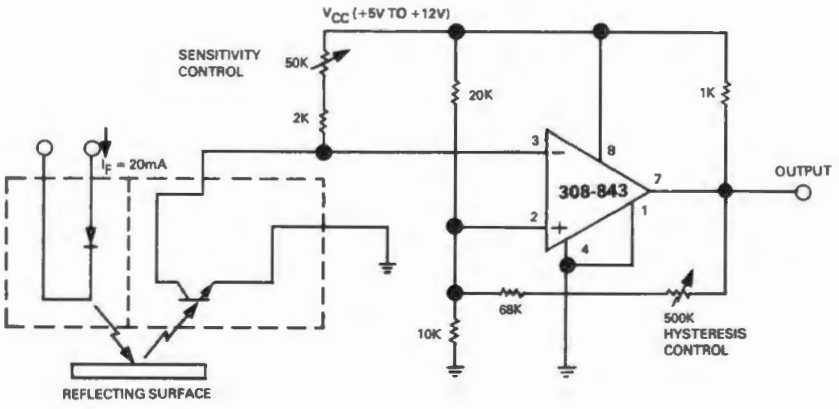
Normalized Collector Current vs. Object Distance



Note: 4 Photocurrent is measured using an Eastman Kodak neutral white test card having 90% diffuse reflectance as a reflecting surface.

Applications

Figure 11



Slotted opto switches (Stock numbers 306-061, 304-560)

Two versions are available. 306-061 comprises a Ga As infra-red LED coupled with an npn silicon photo-transistor housed in a plastic package with infra-red transmitting filter for high ambient light application and dust protection. 304-560 is a similar device but the detector is an integrated circuit consisting of a Schmitt trigger, voltage regulator, differential amplifier and photodiode. The on-chip voltage regulator gives a wide operating voltage range and ensures output compatibility with TTL/LSTTL/CMOS logic.

Figure 12 **Mechanical details** **306-061** **304-560**

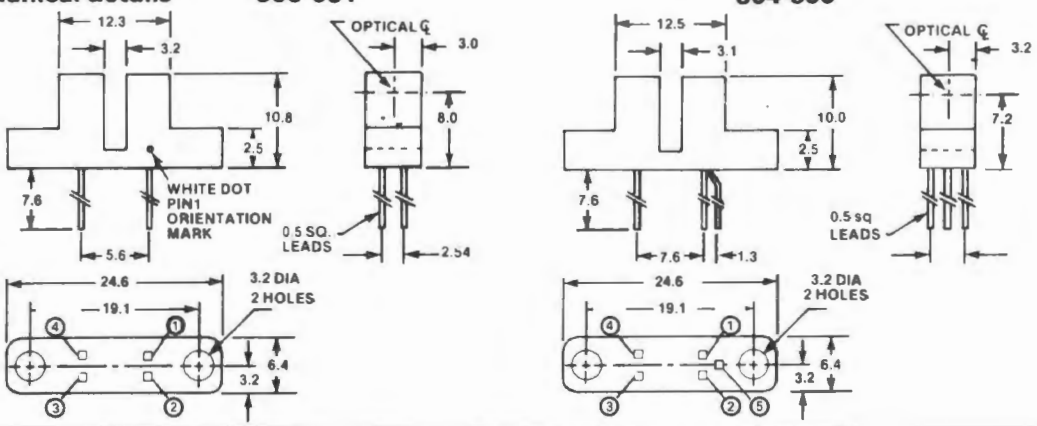
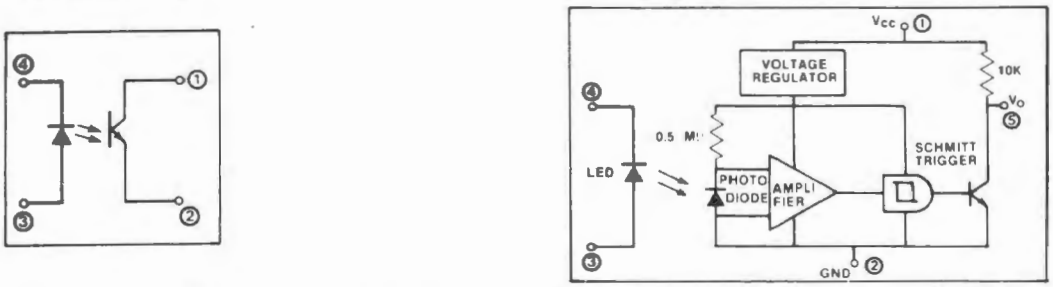


Figure 13 **Electrical details**



Absolute maximum ratings at 25°C (unless stated)

	306-061	304-560
Operating temperature range	−55°C to 100°C	−40°C to 100°C
Storage temperature range	−55°C to 125°C	−55°C to 115°C
Lead soldering temperature (10s)	260°C	260°C

Input diode (306-061 and 304-560)

Forward d.c. current	50mA
Peak forward current (1μs p.w. 300pps)	3A
Reverse d.c. voltage	3V
Power dissipation	100mW

*Derate linearly 1.33mW/°C above 25°C

Output sensors	**306-061**	**304-560**
Collector – emitter voltage	30V	—
Emitter – collector voltage	5V	—
Max allowable V_{CC}	—	20V
Collector d.c. current	30mA	50mA
Power dissipation	150mW**	250mW

**Derate linearly 3.3mW/°C above 25°C

Electrical characteristics at 25°C (unless stated)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Input Diode						
V_F	Forward Voltage	—	1.2	1.7	V	I_F = 20mA
I_R	Reverse Current	—	—	100	μA	V_R = 3V
Output Sensor						
BV_{CEO}	Collector-Emitter Breakdown Voltage	30	60	—	V	I_C = 1.0mA
BV_{ECO}	Emitter-Collector Breakdown Voltage	5	8	—	V	I_E = 100μA
I_D	Collector Dark Current	—	10	100	nA	V_{CE} = 10V, I_F = O, H = O
Coupled						
$V_{CE(SAT)}$	Collector-Emitter Sat. Voltage	—	0.2	0.4	V	I_F = 10mA, I_C = 250μA
$I_{C(ON)}$	On-state Collector Current	1000	3000	—	μA	I_F = 10mA, V_{CE} = 5V
t_R	Response Time	—	5	—	μS	

RS data

Figure 14 **On-state collector current vis input diode forward current**

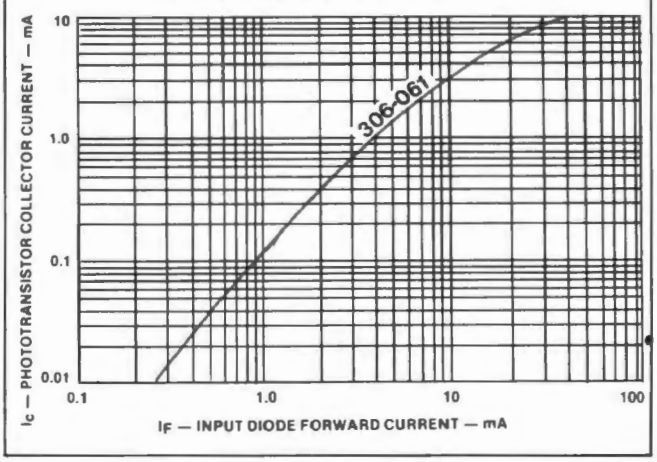
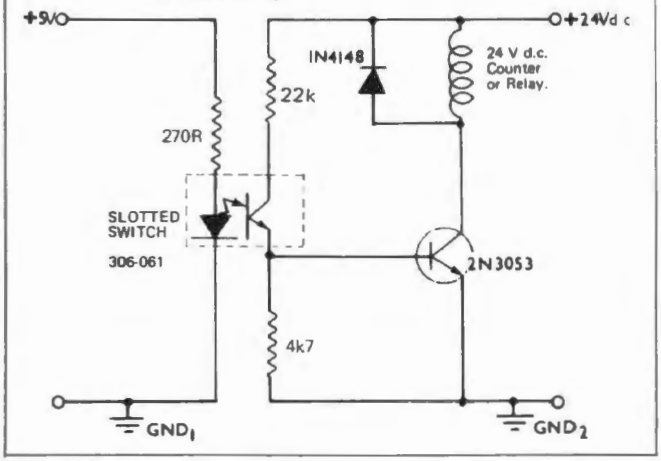


Figure 15 **Application: Event counting or limit switching**



Opto Schmitt switch (Stock number 304-560)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Input Diode						
V_F	Forward Voltage	—	—	1.5	V	I_F = 20mA
I_R	Reverse Current	—	—	10	μA	V_R = 3V
Output Sensor						
V_{CC}	Operating Supply Voltage Range	4.5	—	16	V	
	Output Voltage (Low)	—	—	0.4	V	−40°C<T_A<100°C. I_O = 16mA
	Output Voltage (High)	—	V_{CC}	—	—	NB. Output tied to V_{CC} through 10K resistor
I_{CC}	Operating Current	—	—	15	mA	V_{CC} = 16V
t_p	Propagation Delay Time	1	—	5	μS	I_F = 10mA
t_r	Output Rise Time	—	150	180	nS	C_L = 50pF R_L = 390R V_{CC} = 5V
t_f	Output Fall Time	—	23	50	nS	C_L = 50pF, R_L = 390R- V_{CC} = 5V
	Hysteresis	10	—	30	%	Note 2
I_{FT}	Required LED Current	—	—	10	mA	Note 1. −40°C<T_A<75°C
f_{max}	Maximum Operating Frequency	—	—	100	kHz	C_L = 50pF, R_L = 390R V_{CC} = 5V

Note 1: Required LED current is the minimum forward LED current required to trigger the detector output from LOW to HIGH. Higher LED current may be required for application where optical transmission is reduced.

Note 2: Hysteresis is defined in terms of irradiance (mW/cm²) transmitted to the detector and is equal to the difference in the threshold point (min. irradiance to switch the output high) to the release point (reduced amount of irradiance to switch the output back low) divided by the threshold point.

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RS data

10V and 10.24V reference i.c.'s

Stock number 283-299 and 283-306

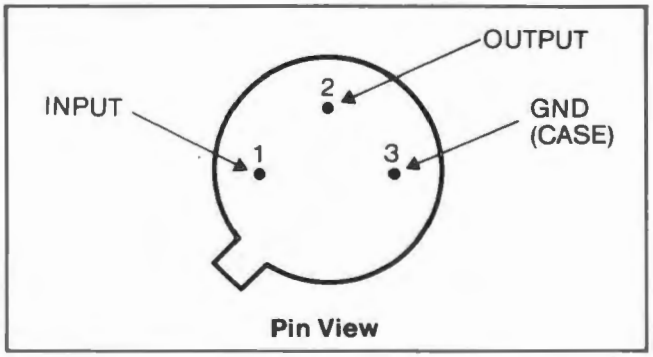
Two precision, 3 terminal voltage reference I.C.'s of 10.000V and 10.240V nominal outputs. Ideal for enabling conveniently equal step sizes for BCD and binary applications respectively in precision D to A and A to D systems.

Absolute maximum ratings

Supply voltage	40V
Power dissipation (see curve)	600 mW
Short circuit duration	continuous
Output current	±20 mA
Operating temperature range	–55°C to +125°C
Storage temperature range	–65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C

Features

- Accurate output voltage
  - 283-299 — 10V±0.03%
  - 283-306 — 10.24V±0.03%
- Single supply operation — 12.5V to 40V
- Low output impedance — 0.2Ω
- Excellent line regulation — 0.2mV/V
- Low zener noise — 20μVp-p
- 3-lead TO-39 metal can
- Short circuit proof
- Low standby current — 3 mA



Pin View

Electrical characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Output voltage	$T_A = 25°C$				
283-299			10.000		V
283-306			10.240		V
Output accuracy	$T_A = 25°C$		±0.03	±0.1	%
Output accuracy				±0.3	%
Output voltage change with temperature	(Note 2)			±0.2	%
Line regulation	$13 \leq V_{IN} \leq 33V$, $T_C = 25°C$		0.02	0.1	%
Input voltage range		12.5		40	V
Load regulation	$0\ ma \leq I_{OUT} \leq 5\ mA$		0.01	0.03	%
Quiescent current	$13V \leq V_{IN} \leq 33V$, $I_{OUT} = 0\ mA$	2	3	5	mA
Change in quiescent current	$\Delta V_{IN} = 20V$ From 13V To 33V		0.75	1.5	mA
Output noise voltage	BW = 0.1Hz To 10 Hz, $T_A = 25°C$		20		μVp-p
Ripple rejection	f = 120 Hz		0.01		%/Vp-p
Output resistance			0.2	1	Ω
Long term stability	$T_A = 25°C$, (Note 3)			±0.2	%/yr.

Note 1: Unless otherwise specified, these specifications apply for $V_{IN} = 15.0V$, $R_L = 10\ k\Omega$, and over the temperature range of $-55°C \leq T_A \leq +125°C$.

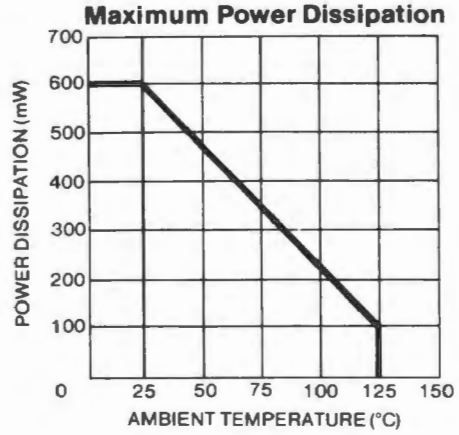
Note 2: This specification is the difference in output voltage measured at $T_A = 85°C$ and $T_A = 25°C$ or $T_A = 25°C$ and $T_A = -25°C$ with readings taken after test chamber and device-under-test stabilization at temperature using a suitable precision voltmeter.

Note 3: This parameter is guaranteed by design and not tested.

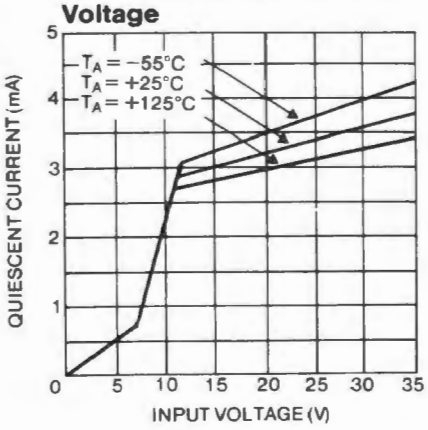
RS data

Performance graphs

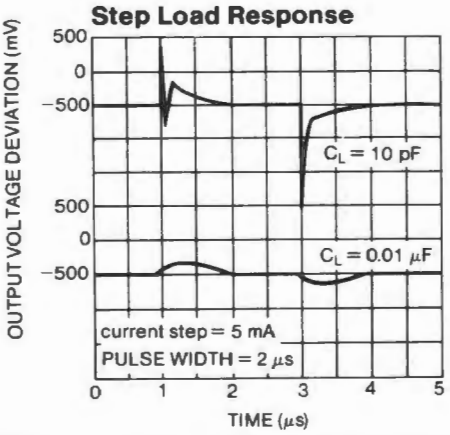
Maximum Power Dissipation



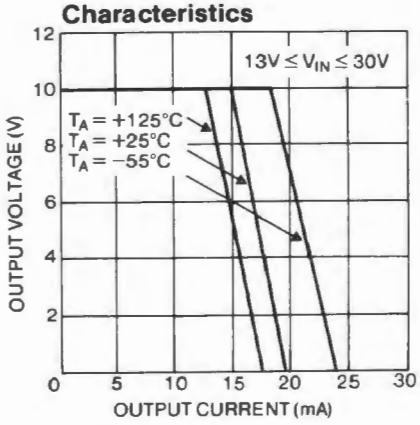
Quiescent Current vs Input Voltage



Step Load Response



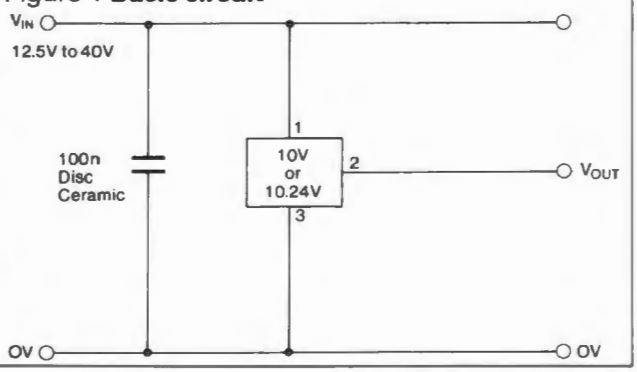
Output Short Circuit Characteristics



Typical applications

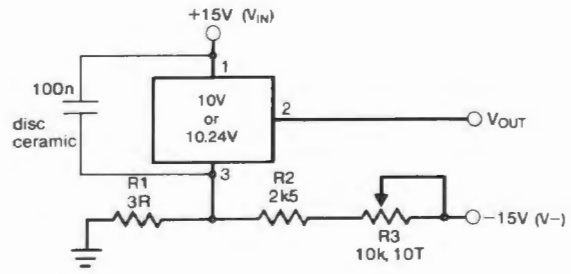
The basic circuit for applying the 10V & 10.24V reference I.C.'s is shown here in Figure 1.

Figure 1 **Basic circuit**



The output of the 10V and 10.24V references may be adjusted to a precise voltage by using the circuit shown in Figure 2, since the supply current of the devices is relatively small and constant with temperature and input voltage. For the circuit shown, supply sensitivities are degraded slightly to

Figure 2 **Output voltage fine adjustment**



0.01%/V change in V_{OUT} for changes in V_{IN} and V−.

An additional temperature drift of 0.0001%/°C is added due to the variation of supply current with temperature. Sensitivity to the value of R1, R2 and R3 is less than 0.001%/%

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RS data

Real time clock i.c.

Stock number 304-548

The RS 58174 is a metal gate CMOS circuit that functions as a real time clock and calendar in bus-orientated microprocessor systems. An interrupt timer is included, which can be programmed to have one of three times. The time base is obtained from a RS 32.768 kHz crystal with time keeping down to 2.2V for low power standby operation from batteries.

Features

- Microprocessor compatible.
- Tenths, units and tens of seconds, units and tens of minutes, units and tens of hours, day of week, units and tens of days, units and tens of months, independent registers.
- Automatic leap year calculation.
- Internal data save pull-up resistors.
- Protection for read during data changing.
- 500 ns fast access time.
- Independent interrupt system.
- TTL compatible.
- Low power standby operation.

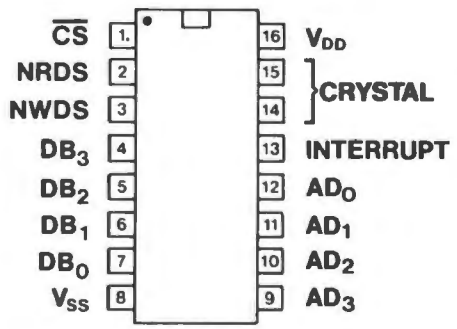
Absolute maximum ratings

Voltage at all inputs and outputs
V_{DD} +0.3 to V_{SS} − 0.3V
Operating temperature ——— 0°C to +70°C
Storage temperature ——— − 65°C to + 150°C
$V_{DD} - V_{SS}$ ——— 6.5V
Lead temperature (soldering 10 seconds) ——— 300°C

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Pin Connections



TOP VIEW

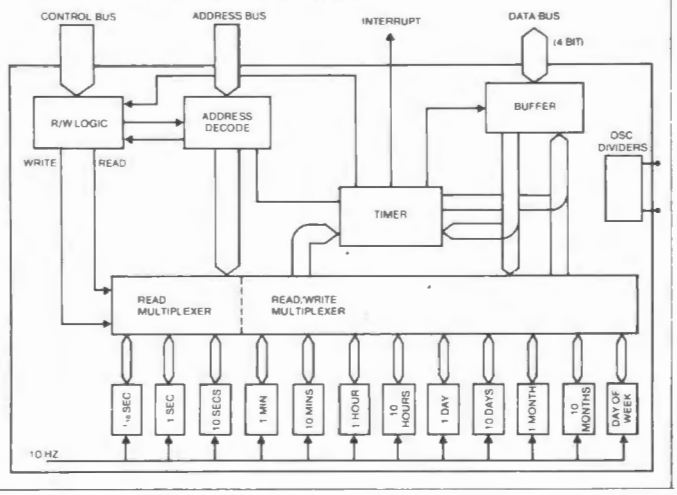
NRDS = Not read data strobe
NWDS = Not write data strobe

Electrical characteristics $T_A = 0$ to + 70°C $V_{SS} = OV$

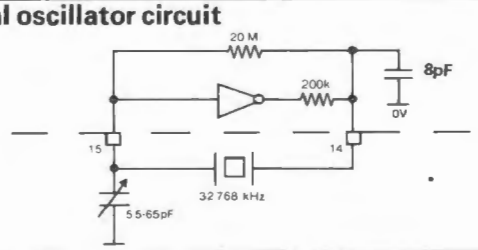
Parameter	Terminals	Conditions	Min.	Typ.	Max.	Units
V_{DD} (supply voltage)	16	Standby mode (no READ or WRITE instructions)	2.2			V
		Operational mode	4.0		5.5	V
I_{DD} (Supply current)	16	$V_{DD} = 2.5V$		4	10	μA
		$V_{DD} = 5.0V$			1	mA
Logic 1 input	1 to 7 and 9 to 12	$V_{DD} = 5V$	2.0			V
Logic 0 input					0.8	V
Input capacitance					10	pF
Input current to V_{SS}	2, 4 to 7 and 9 to 12	$V_{DD} = 5V$, $V_{in} = V_{DD}$			30	μA
Internal resistor to V_{DD}	1 and 3		30	100		kΩ
Logic 1 output	4 to 7	$I_{OH} = 0.1$ mA	2.4			V
Logic 0 ouput		$I_{OL} = 1.6$ mA			0.4	V
Logic 0 output	13	$I_{DS} = 5$ mA			1.0	V
Off leakage		$V_{OUT} = 5$ V			5	μA

The internal counters are arranged as bytes of four bits each. When a byte is addressed it will appear on the data I/O bus enabling independent access. For bytes which do not contain 4 bits (e.g. week days use only 3 bits) the unused bits are not recognised during a write operation and tied to V_{SS} during a read operation. The addressable reset latch holds tenths, units and tens of seconds in a reset condition. If a register is updated during a read operation the I/O data is prevented from updating and a subsequent read will return the illegal b.c.d. code 1111. This allows detection that the previous data had changed and is now incorrect. The interrupt timer can be programmed for 0.5,5 or 60 second intervals and may be coded for single or repeated operation. The open drain interrupt output is pulled to V_{SS} when the timer times out and reading the interrupt register provides the status and internal selected information.

Internal circuit block diagram



Crystal oscillator circuit



The oscillator is formed by the on chip inverter/amplifier with bias resistors and capacitors. A 5.5—65 pF trimmer is used to fine tune the oscillator. The oscillator output is blocked by the start/stop flip-flop.

Circuit Description

non-integer divider

This divides the incoming 32.768 kHz frequency by 15/16 giving an output of 30.720 kHz.

fixed divider (512)

This is a standard 9 stage binary ripple counter with an output frequency of 60 Hz. This counter is reset to zero by the start/stop flip-flop.

fixed divider 6

This three stage Johnson counter gives an output of 10 Hz. This counter is also reset to zero by the start/stop flip-flop.

synchronization stage

This section is fed with 10Hz and 32.768 kHz clock signals and generates a pulse of 15.25μs width on the rising edge of each 10Hz pulse. This pulse is used to increment all the seconds, minutes, hours, days, months and year counters. It is also used to set the data changed flip-flop.

Standby mode

This is automatically selected when the supply voltage falls to the standby level. (2.2V minimum) with no read or write strobes.

Table 1 Interrupt read back status
Address 15 Read Mode

Interrupt status	DB3	DB2	DB1	DB0
Reset	0	0	0	0
60 sec. signal	0/1	1	0	0
5.0 sec. signal	0/1	0	1	0
0.5 sec. signal	0/1	0	0	1

DB3 = 0, no interrupt DB3 = 1, interrupt from timer

Table 2 Years status register
Address 13 Write Mode

	DB3	DB2	DB1	DB0
Leap year	1	0	0	0
Leap year +1	0	1	0	0
Leap year +2	0	0	1	0
Leap year +3	0	0	0	1

Data changed flip-flop

This indicates that the clock value has changed since the last read operation and is set by the rising edge of each 10Hz pulse. The flip-flop sets all data bus bits to a 1 during NRDS time indicating that a register has been updated and is reset by any clock read command.

seconds counters

a) tenths of seconds
b) units of seconds
c) tens of seconds

The outputs of all three counters may be separately multiplexed on to the command 4 bit output bus. All three counters are reset to zero by the start/stop flip-flop.

minutes counters

a) units of minutes
b) tens of minutes

Both these counters are parallel loaded with data from the 4 bit bus when correctly addressed by the microprocesor and a write data strobe pulse is given. The output of both counters can be read separately on the common 4 bit output bus when correctly addressed and a read data strobe pulse is given.

hours counters

a) units of hours
b) tens of hours

Both count in a 24 hour mode and have identical parallel load and read multiplex features as the minutes counters.

days counters

The two days counters are
a) units of days
b) tens of days

These counters count up to 28, 29, 30 or 31 days depending on months counters and year status register states. The days counters have parallel load and read multiplex capabilities.

months counters

The two months counters are
a) units of months
b) tens of months

These have parallel load and read multiplex capabilities.

Years status register
This is a four bit shift register. It is shifted every year on the 31st December. The status register must be set in accordance with year status register requirement. See table 2. No readout capability is available.

Chip select ($\overline{CS}$)
This external chip select is provided and is active low,

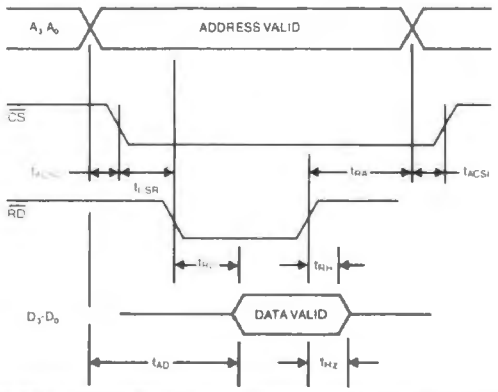
Counter and register selection
The address line codings for AD0-AD3 which select the registers for either parallel loading or reading on the output bus, can be seen in table 5.

Interrrupt output
An exclusive address (15) selects the interrupt latches. These enable the interrupt and dictate its frequency see Table 1. The interrupt output flip flop is reset by reading the interrupt register. At chip address 15 writing a 1 on DB3 selects repeated interrupt, a 0 selects single interrupts. To ensure correct operation the interrupt should be serviced within 16.6ms.
The interrupt register contents are read onto the data bus by reading the interrupt status of the circuit, a high on DB3 indicates that an interrupt has occurred. The trailing edge of the NRDS pulse that reads the interrupt status automatically resets DB3 to zero. The next system NRDS following an interrupt status read pulse automatically restarts the interrupt timer if in continuous mode.
With DB3 set to zero at chip address 15 the timer is reset at the completion of the selected timing period and must be set by software if a subsequent interrupt is required. Setting DB3 to 1 allows automatic repeated timer inputs, starting after the next system NRDS pulse following an interrrupt status read pulse. Interrupt should be initialised by applying the reset condition and reading 3 times at address 15.

Stop/start
A logic 1 on DB0 at chip address 14 starts the clock running, a logic 0 stops the clock, This allows time data to be loaded and the clock then to be started precisely.

Test mode
This mode is used in production testing of the circuit. For normal operation the circuit must be in non-test mode and set as part of the system initialisation. Non test mode is set by writing a logic 0 to DB3 at AD0.

Read cycle waveforms



Data transfer timing

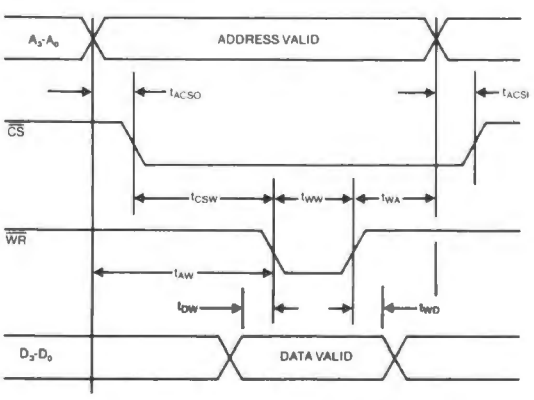
Table 3 Data from peripheral to microprocessor timing

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Address bus valid to chip select ON ($\overline{CS}$=0)	t_{ACSO}	V_{DD} = 5V		40		ns
$\overline{CS}$ ON to read strobe	t_{CSR}		70			ns
Read cycle access time from read strobe to data bus valid	t_{RD}	C_L = 100pF		450	500	ns
Data hold from trailing edge of read strobe	t_{RH}		0		250	ns
Address bus hold time from trailing edge of read strobe	t_{RA}		50	500		ns
Address change to chip select OFF	t_{ACSI}			40		ns
Address bus valid to data valid	t_{AD}	C_L = 100pF		850	1200	ns
Time from trailing edge of read strobe until interface device bus drivers are in tri-state mode	t_{HZ}		0		250	ns

Table 4 Data from microprocessor to periphal timing

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Address bus valid to chip select ON ($\overline{CS}$=0)	t_{ACSO}	V_{DD} = 5V		40		ns
Chip select ON to write strobe	t_{CSW}		310	450		ns
Address bus valid to write strobe	t_{AW}		350			ns
Write strobe width	t_{WW}		430			ns
Data bus valid before write strobe	t_{DW}		50			ns
Address bus hold time following write strobe	t_{WA}		100			ns
Data bus hold time following write strobe	t_{WD}		50			ns
Address change to chip select OFF ($\overline{CS}$=1)	t_{ACSI}			40		ns

Write cycle waveforms



Note: All times are measured from, or to, logic 1 level = 2.0V or logic 0 level = 0.8V.

RS data

Application

When the system is powered up it is necessary to enter the correct data into the device registers and start the clock running. The seconds, minutes, hours, days and months counters are all parallel loaded with data from the 4 bit data bus when correctly addressed, $\overline{CS}$ is low and a write data strobe pulse is given. Data to be entered is set up on the 4 bit data bus; the address from Table 5 for the required register is set on the 4 bit address bus and a write data strobe pulse is sent. Chip select must be low during write and read operations. All information is entered in the same way with the relevant address. To start the clock running at the required instant a logic 1 is written to DB0 at address 14, likewise writing a 0 stops the clock. Data can be read from a register by using the required address as in Table 5 and applying a read strobe pulse. The data becomes available on the 4 bit data bus: chip select must be low for this read operation.

Table 5 Address decoding for internal registers

Selected counter	Address bits				Mode
	AD3	AD2	AD1	AD0	
0 Test only	0	0	0	0	Write only
1 Tenths of sec.	0	0	0	1	Read only
2 Units of secs.	0	0	1	0	Read only
3 Tens of secs.	0	0	1	1	Read only
4 Units of mins.	0	1	0	0	Read or Write
5 Tens of mins.	0	1	0	1	Read or Write
6 Units of hours	0	1	1	0	Read or Write
7 Tens of hours	0	1	1	1	Read or Write
8 Units of days	1	0	0	0	Read or Write
9 Tens of days	1	0	0	1	Read or Write
10 Day of week	1	0	1	0	Read or Write
11 Units of months	1	0	1	1	Read or Write
12 Tens of months	1	1	0	0	Read or Write
13 Years	1	1	0	1	Write only
14 Stop/Start	1	1	1	0	Write only
15 Interrupt and status	1	1	1	1	Read or Write

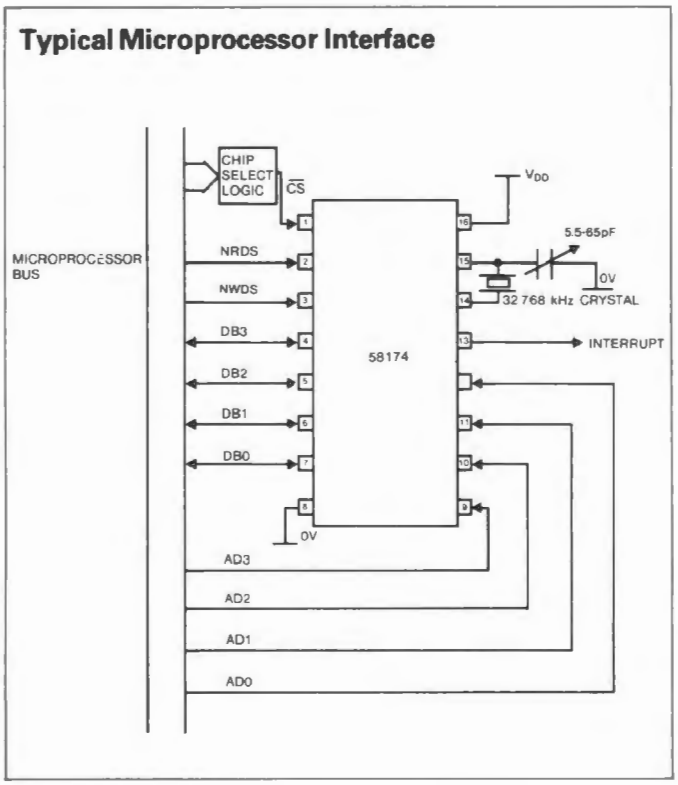
Table 6 Interrupt selection data

Address 15 Write Mode

Function	DB3	DB2	DB1	DB0
No Interrupt	X	0	0	0
Interrupt at 60sec intervals*	0/1	1	0	0
Interrupt at 5.0sec intervals*	0/1	0	1	0
Interrupt at 0.5sec intervals*	0/1	0	0	1

*+16.6 ms
DB3 = 0, single interrupt DB3 = 1, repeated interrupt

Typical Microprocessor Interface



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RS data

Keyless lock i.c. RS 7225

Stock number 304-554

The RS 7225 is a monolithic ion implanted PMOS 4 input Keyless Lock I.C. The circuit has sequential logic for interpretation of correct inputs, a momentary and static lock control output, out-of-sequence detection circuitry and an output for wrong entries.

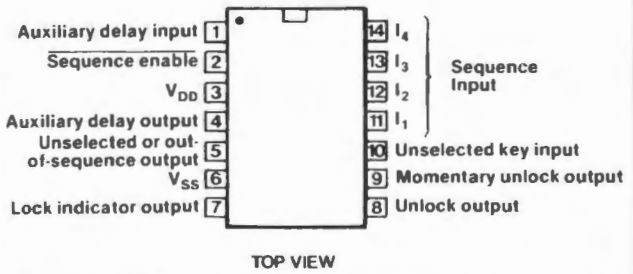
Features

- Stand alone lock logic.
- Out-of-sequence detection.
- Unselected/Out-of-sequence output and sequence input.
- Direct LED and lock relay drive.
- Externally controlled combination delay.
- Internal pull down resistors on all inputs.
- Low current consumption & high noise immunity.
- Single power supply operation.
- Auxiliary delay circuit.

Absolute maximum ratings (Voltages w.r.t. V_{DD})

Supply voltage	18 Vd.c.
All inputs	18 Vd.c.
Operating temperature range	— 25 to + 70°C
Storage temperature range	— 65 to + 150°C

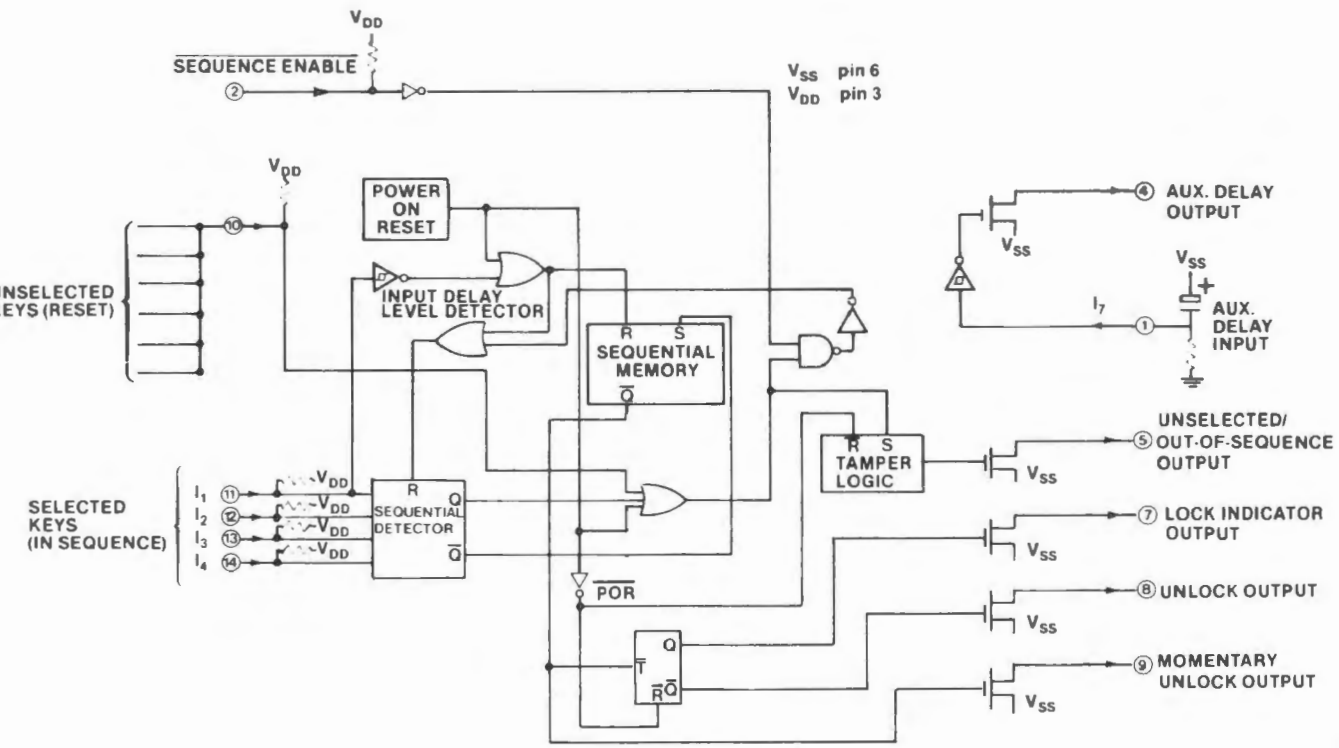
Pin Connections



Electrical characteristics $T_A = 25°C$ $V_{DD} = 0$ V

Parameter	Conditions	Min.	Typ.	Max.	Units
Logic 1 output currents — pins 8 and 9	V_{SS} = 5V V_{SS} = 12V — Vout = V_{SS} − 2	2.15 9.00	3.06 11.64	4.10 14.40	mA mA
— pin 5	V_{SS} = 5V V_{SS} = 12V — Vout = V_{SS} − 2	0.48 2.00	0.68 2.60	0.92 3.23	mA mA
— pin 1	V_{SS} = 5V V_{SS} = 12V — Vout = V_{SS} − 2	0.40 1.84	0.62 2.37	0.84 3.00	mA mA
Lock indicator output	V_{SS} = 5V V_{SS} = 12V — Vout internally clamped to 1.7V	0.64 6.55	1.00 8.68	1.37 11.00	mA mA
Input logic 0, pin 11	V_{SS} = 5V V_{SS} = 12V	0 0		V_{SS} − 3 V_{SS} − 8	V V
All other inputs logic 0	V_{SS} = 4 to 18V	0		V_{SS} − 3	V
Input logic 1, pin 11	V_{SS} = 5V V_{SS} = 12V	V_{SS} − 1.5 V_{SS} − 5.5		V_{SS} V_{SS}	V V
All other inputs logic 1	V_{SS} = 4 to 18V	V_{SS} − 1		V_{SS}	V
Quiescent supply current (all inputs & outputs open)	V_{SS} = 5V V_{SS} = 12V			20 40	μA μA
Input load current	V_{IN} = V_{DD}, V_{SS} = 12V		6		μA

Figure 1 **RS7225 Block diagram**



Circuit description

Sequential inputs and combination delay

The sequential memory is set by the correct sequence of logical 1's on the inputs I_1, I_2, I_3 and I_4. This causes the Unlock output to go high, the momentary Unlock output to go high and the Lock Indicator to turn OFF. An external capacitor at input I_1, determines the amount of time allowed to enter the input sequence. This time period is a function of the external capacitance and the supply voltage. See figure 2 for characteristic graph.

Unselected keys

Should a logic 1 appear at this input the sequential input detector will be reset and a pulse will be transmitted on the unselected key output.

Unlock output

This output will change state when the sequential memory is set. Its output state will be a logic 1 or open circuit.

Lock indicator

This output drives and LED directly and is the complement of the Unlock output, i.e. logic 1 indicates 'locked'.

Momentary unlock

This output goes to a logical 1 when the sequential memory is set. It goes open when input I_1 to the level detector changes from logic 1 to logic 0.

Unselected out-of-sequence output

This output gives a 15μS pulse when I_3 or I_4 receives an Out-of-sequence input or if the Out-of-sequence input receives a logic 1. This output is normally open. An output is inhibited between power on and the first logic 1 input to pin 11.

Sequence enable

A logic 1 at this input disables the "Sequential Detector" disallowing any sequential input. This input is intended to be used in conjunction with the Unselected/Out-of-sequence output.

Power-ON-reset

A power on reset circuit resets the device to the locked condition when the circuit is powered up.

Power supplies

The circuit is designed to operate over a supply voltage range from +4 to +18 Volts.

System timing

(Input capacitance = 10pF)

Parameter	Min.	Typ.	Max.	Units
Convenience delay set-up time t_S	6	8	10	μsec
Hold time t_H	14	16	20	μsec
Input lock control output delay t_{LC}	10	13	15	μsec
Input pulse width t_{iw}	22	25		μsec
Unselected/Out-of-sequence output pulse width t_w			15	μsec
Combination delay Rise time t_r	C + 70			n sec
Combination delay fall time t_f	C + 60			n sec

Figure 2 **Typical delay hold time against V_{SS} (with 1μF combination delay capacitor)**

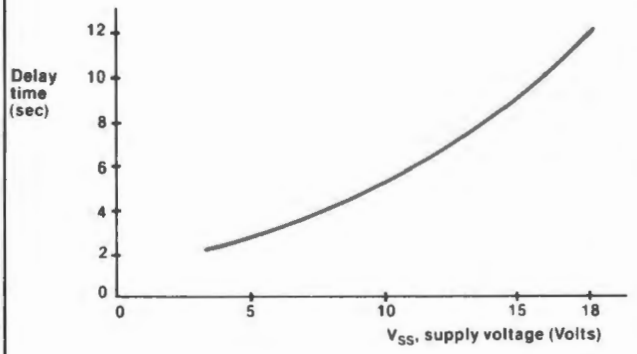
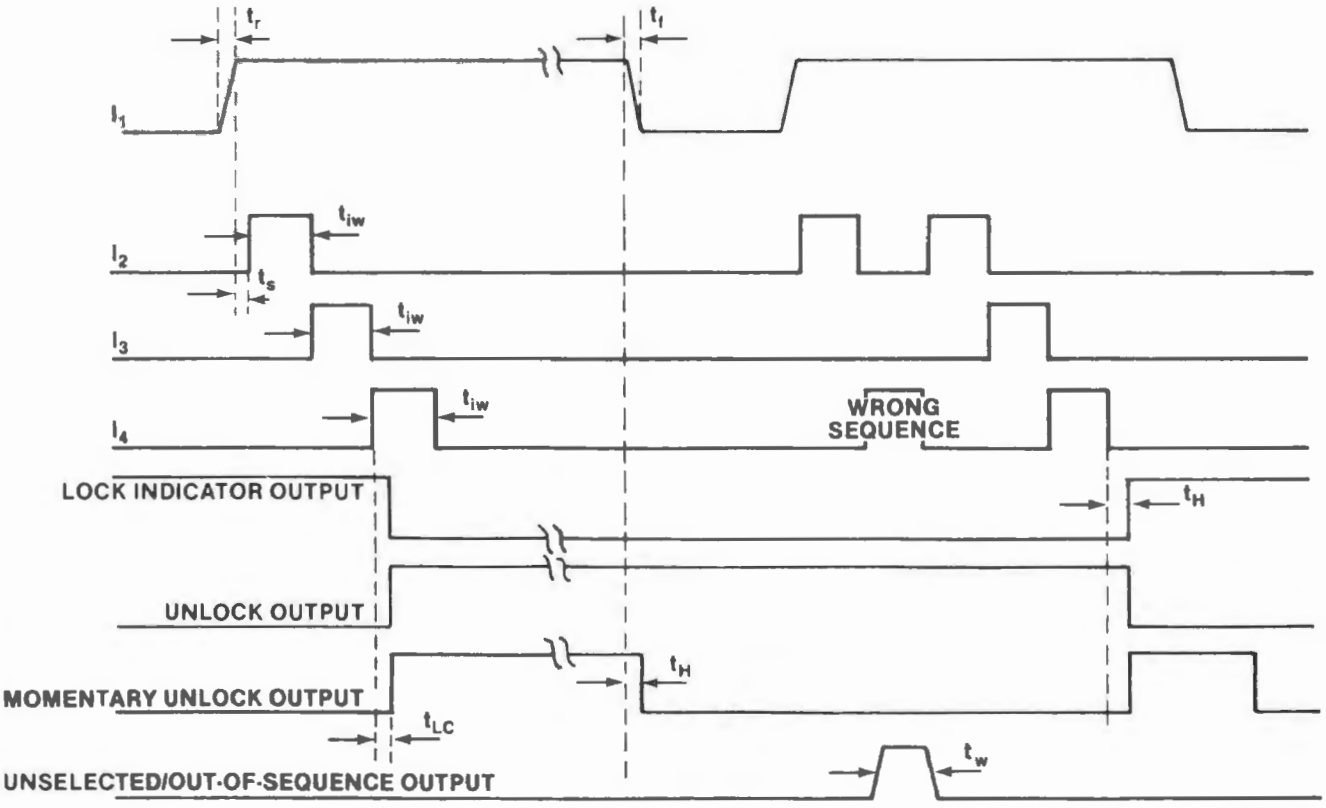


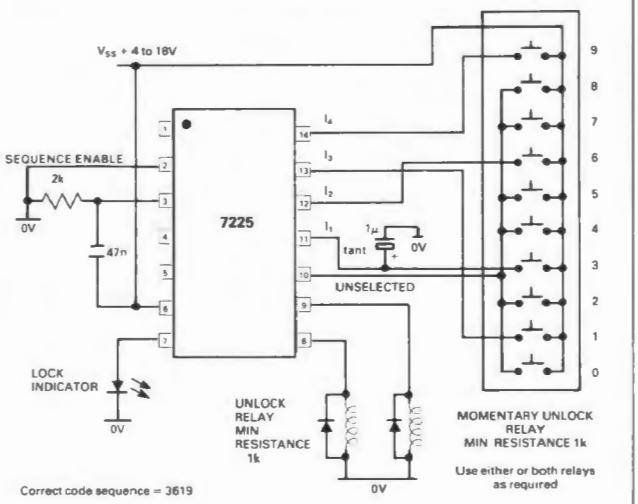
Figure 3 **Timing diagram**



RS data

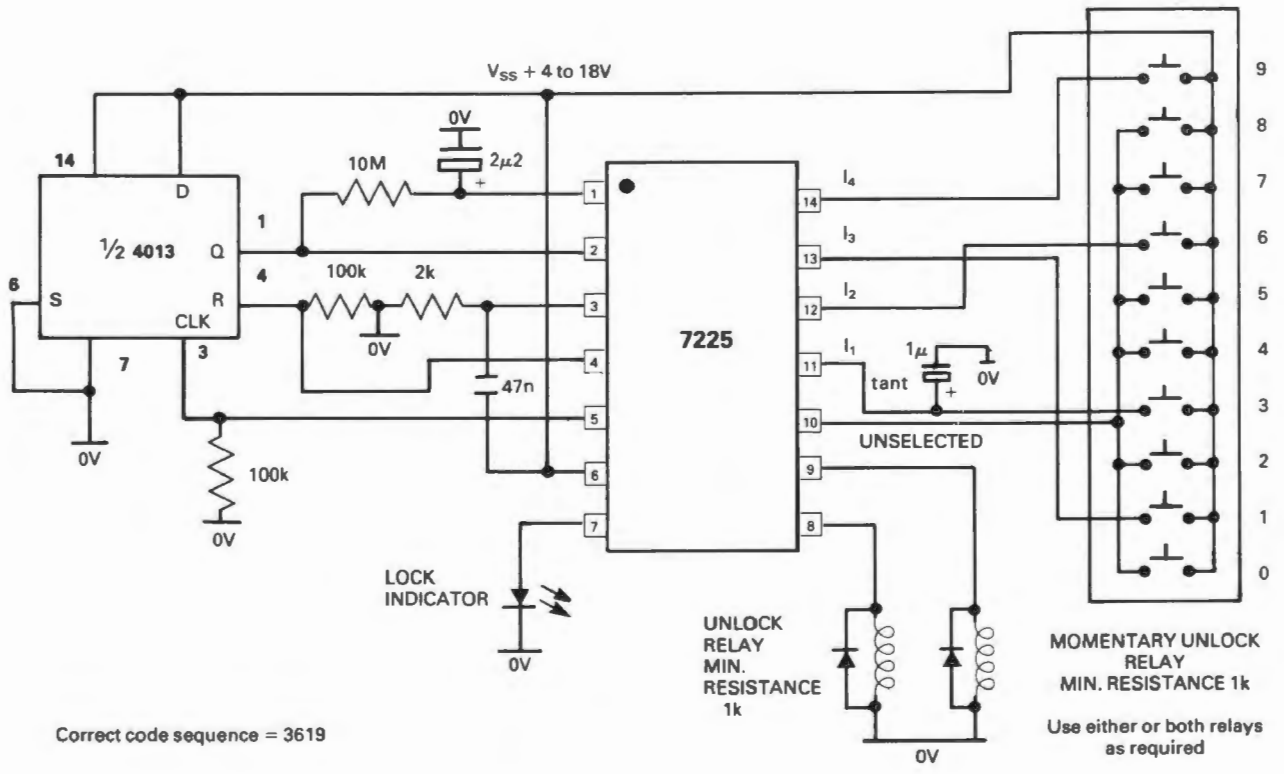
Applications

Figure 4 **Typical application in lock circuit**



When input I_1 is taken high the circuit will accept the unlocking input sequence, I_2 I_3 I_4. After a correct sequence the Unlock output will go high and the Momentary Unlock control output will also go high until input I returns to a low level. The Lock Indicator output will go low, turning the lock indicator OFF thus showing the circuit is in the unlocked condition. If the input sequence is incorrect the internal "sequence detector" will be reset and the entire input sequence must be repeated. The Unlock output is turned OFF by repeating the input sequence: this also turns the Lock Indicator ON again. The Momentary Unlock output goes high each time the correct sequence is entered.

Figure 5 **Application using internal delay circuitry to disable the sequence detector and stay locked for approximately 20 seconds if an incorrect entry is made**



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RS data

European 'D' Fuses

Stock Nos: 413–620 thru 686
413–743 thru 765

A range of DII and DIII delayed-acting type European industrial H.R.C fuselinks which comply with the dimensional requirements and current ratings of DIN 49515, VDE 0636.

Features

- Low internal wattage
- Non ageing continuous load capacity
- High breaking capacity, in excess of 70 kA
- Visual indication as to state of fuse element via coloured disc in end cap

All the above features combine to generally enable the safe replacement of fuselinks in equipment where DII and DIII type fuses marked with the symbol or 'gL' are used.

Cable protection

RS DII and DIII delayed-acting type industrial fuse-links with fusing factor of 1.5 allow for close excess current protection of P.V.C. insulated cables. In motor circuits the starter will provide overload protection for the motor and the fuselink will provide short circuit protection for the cable.

Ratings

Prospective short-circuit currents* at point of installation of D fuse cartridges (500 Volts.)

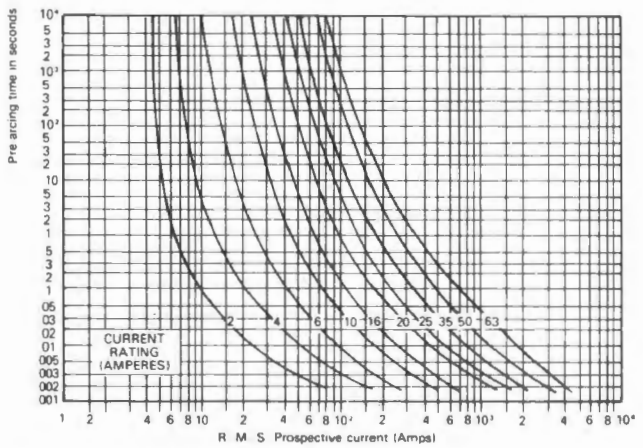
Rated current A	Permissible short-circuit current at 220 V~ 220 V– kA	380 V~ 440 V– kA	500 V~ 500 V– kA
2 4 6 10 16 20 25	unlimited	unlimited	unlimited
35 50 63	80	70	70

*A.C. kA (r.m.s.) $\cos\varphi = 0, 1 - 1$
D.C. non-inductive

Non-ageing continuous, load capacity of D fuse-links

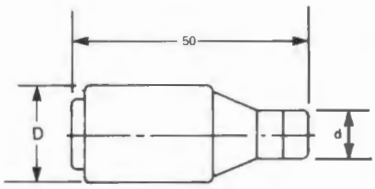
2	4	6	10	16	20	25	35	50	63	Fuse current rating A
3	6	9	14	20	26	30	43	60	70	Permiss. contin. current A

Mean time/current characteristics-delayed acting in accordance with VDE 0635 and VDE 0636/3.



RS data

Dimensions



Rated current (A)	d (mm)	D (mm)
2	6	22
4	6	22
6	6	22
10	8	22
16	10	22
20	12	22
25	14	22
35	16	29
50	18	29
63	20	29

Health and Safety at Work Act

The fuses referred to in this data sheet are manufactured and tested to the specifications indicated, but must be correctly installed by competent personnel to provide protection within the capability of the stated ratings and related performance characteristics.

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RS data

Manual motor starters and accessories

A range of manual motor starters and accessories conforming to VDE 0660 pt. 1, IEC 157-1 and BS 4752, which provides a compact and economical method of starting squirrel cage motors or switching distribution circuits.

Specification

Max. switching frequency ——— 40 operations per hour.
Mechanical life span ——— 5 x 10^5 operations.
Contact life span to AC3 at max. rating operating current ——— 10^5 operations.
Breaking capacity 220/240V ——— 1.7 kA rms.
380/415V ——— 1.5 kA rms.
500V ——— 1.3 kA rms.
600V ——— 1.0 kA rms.
Bimetal trips with T11 characteristics to VDE 0660

Safety applications

The starter when fitted with an undervoltage trip can be switched off remotely using emergency pushbuttons, level switches, positive break door interlocks or guard switches, magnetic safety switches, limit switches and similar devices. The low-volt release feature is useful on appliances or machines that would present a danger if an interrupted mains supply was suddenly restored causing them to restart without warning e.g. Kitchen equipment such as potato peelers, bacon slicers etc.

Features

- Isolating characteristics, positive operation and terminal shrouds = Ideal main switch to IEC 204.
- Overcurrent protection — adjustable bimetal and instantaneous magnetic trips.
- Remote stopping possible by using voltage trips.
- High impact thermoplastic enclosures.
- Water and dust protection to IP55 possible by using enclosures or mounting frames (see appropriate sub heading p.3)

Basic starter

The basic starter (fig. 1) which forms the nucleus of the system is a triple pole manually operated starter which affords overcurrent protection via adjustable bimetallic trips, temperature compensated for 20 and 40°C, and short circuit protection via instantaneous magnetic trips. Connections by single screw saddle clamps accepting cables up to 6mm².

Adjustment of Bimetal Trips

To adjust the bimetal trips insert a small screwdriver at 'x', see figs 1 and 2. Turn clockwise to increase current, anti-clockwise to decrease current.

Adjustment of temperature compensation

Prior to adjustment, totally isolate from mains. Remove the front cover from the starter, unclipping from base at points 'A', see figs. 1 and 2. While holding red current disc insert small screwdriver at 'x' and turn. Clockwise 20°C ambient, anti-clockwise 40°C ambient.

Figure 1 **Basic starter**

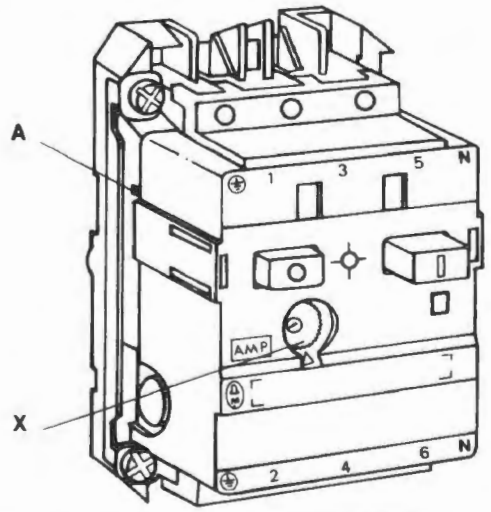
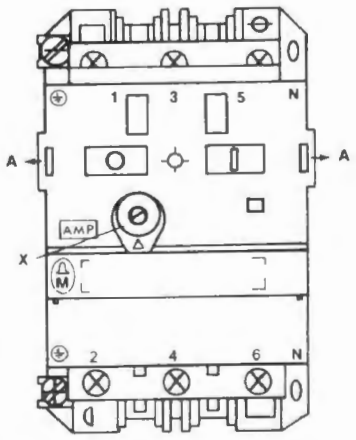


Figure 2 **Front view of Starter**



Back up fuses

The basic starter is inherently short circuit proof in the two lower current ratings, and therefore back up fuses are not required. In the higher current rated devices (>1.6A) back up fuses are required to protect the starter and associated cabling from possible short circuit currents. The rating of the fuse should be taken from the table below.

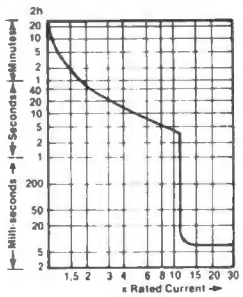
STOCK NO.	SETTING RANGE OF BIMETAL TRIPS	FIXED MAGNETIC TRIP SETTING	MAX. BACK UP FUSES REQUIRED WHEN FAULT LEVEL EXCEEDS BREAKING CAPACITY OF STARTER 220/240V	308/415V	500V	600V
348-043	0.6 - 1.0A	11A	No back up fuse required, short circuit proof up to highest fault currents.			
348-037	1.0 - 1.6A	16A				
348-021	1.6 - 2.4A	26A			25	25
348-015	2.4 - 4.0A	44A		50	35	35
348-009	4.0 -6.0A	70A	50	50	35	35
347-999	6.0 - 10.0A	110A	50	50	50	50
347-983	10.0 - 16.0A	180A	50	50	50	50

Tripping characteristics

Figure 3 shows the tripping characteristics of the basic starters, at 20°C ambient temperature with the bimetal trips at their initial cold state, (i.e. at initial switch-on).

The tripping time of the bimetal trips at their normal working temperature (i.e. after switch-on and they have been passing current) is approx. 25% of that shown.

Figure 3
Time/current characteristics



Auxiliary Switch

Two auxiliary switches (348-100) are available as a set which when fitted to the basic starter will extend the switching capability to 3 main poles + 2 auxiliary switches.

Note:- Switches may be fitted either in normally open N/O or normally closed N/C configuration.

Rated operating current:

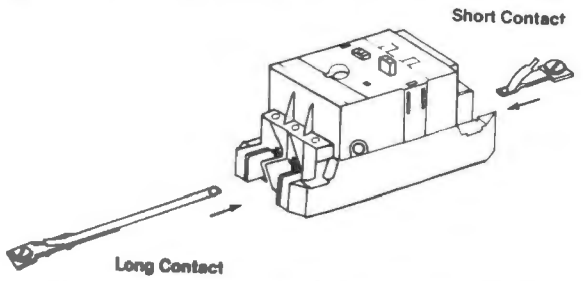
AC11	240V — 6A	DC11	60V — 1.5A
	415V — 3A		110V — 1.0A
	500V — 1.5A		220V — 0.5A

Assembly

N/C Switch:— Press start (O) button and insert the long contact into the ⊏shaped hole under the main terminals. (Note correct orientation of starter as in figure 4.) Press start (I) button and insert the short contact into the ⊏shaped hole directly opposite. If only one N/C switch is required, identification plate 11/12 should be used in order to follow the CENELEC numbering system.

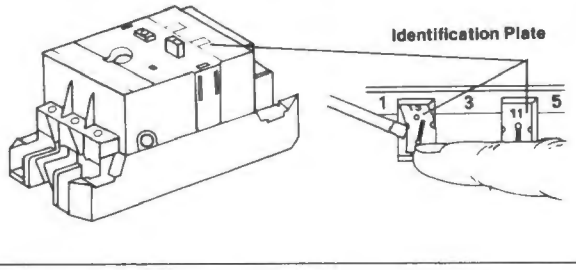
N/O Switch:— Press start (I) button and insert the long contact into the⊏ shaped hole under the main terminals. (Note correct orientation of starter as in figure 4.) Press stop (O) button and insert the short contact into the ⊏shaped hole directly opposite. If only one N/O switch is required, identification plate 13/14 should be used in order to follow the CENELEC numbering system.

Figure 4 **Assembly of auxiliary switch**



Identificaton plates:- Fit the appropriate switch identification plates into the holders as detailed in fig. 5, for clarification of switching mode.

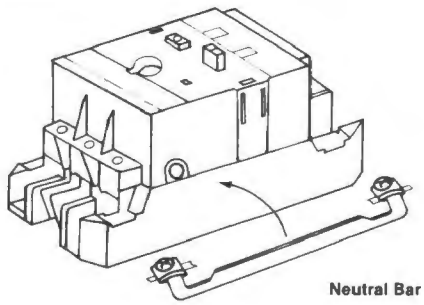
Figure 5 **Fitting of switch identification plates**



Neutral bar

A neutral bar (348-093) may be attached to the basic starter, as shown in fig. 6. for use when phase to neutral supplies are required either for voltage trips or for control and indication lights mounted adjacent to a motor.

Figure 6 **Fitting of neutral bar**



Voltage trips

An **undervoltage** or a **shunt trip** may be fitted to the basic starter to provide remote switching, interlocking or voltage monitoring. (See typical connection diagrams p. 4 and safety applications p. 1).

Undervoltage trip is designed to trip the starter out should the supply voltage drop to between 70 and 30% of its rated value. The coil is continuously rated and has a pick up voltage of approx. 80% of rated voltage. Coil rating (VA/W): 3/2, 100% relative duty cycle.

Shunt trip is designed to trip the starter out when a voltage ⩾50% rated voltage, is applied to it. Used for remote switching, interlocking between starters. Used in preference to the undervoltage trip where the motor starter should not switch off upon loss of voltage. Coil rating (VA/W): 3/2, 40% relative duty cycle.

Assembly

Both undervoltage and shunt trips are fitted to the basic starter in exactly the same manner. Remove the front cover from the starter by unclipping from base at points 'A', see figs 1 and 2. Press the start (I) button and fit the required voltage trip from the right, see fig. 7, ensuring the armature is held closed. Secure the voltage trip with the 2 self-tapping screws provided. The leads from the shunt coil may be passed through the front cover at point A (start button side). See figs 1 and 2.

Figure 7

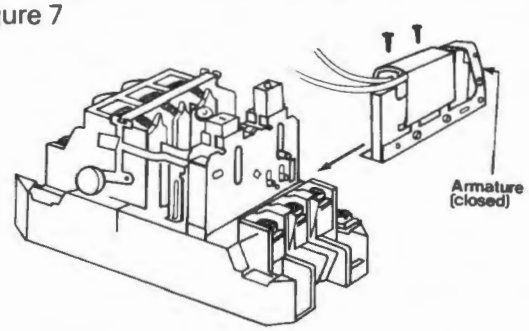
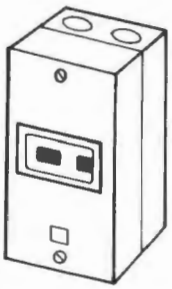


Figure 8 **Surface enclosure**



Enclosures and mounting frames

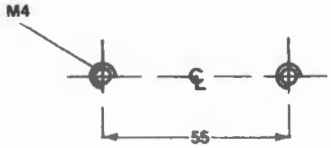
A range of high impact thermo plastic enclosures and mounting frames that permit the basic starters, including accessories, to be surface, flush or rear mounted. Push button apertures are fitted with a diaphragm to give sealed protection to IP55. Thus the surface enclosure gives IP55 protection to both the pushbuttons and the terminals whereas the flush and rear mounting versions are subject to the IP rating of their associated equipment.

Assembly

Surface enclosure

Two part enclosure having 4xPG16 (23.5mm dia.) knock outs. See Cables/Cable Accessories section of current catalogue for PG16/M20 adaptor, and integral retaining pegs to which a starter is clipped. The enclosure is fitted to a flat surface utilising the two internal M4 screw receptacles, see fig. 9 for mounting details.

Figure 9 **Mounting details**



Flush mounting frame

Two part frame consisting of four panel retaining clamps, front cover sealing ring and integral retaining pegs to which a starter is clipped. The base frame is fitted into the panel cut-out, see fig. 11, and secured using the four retaining clamps. The sealing ring is then fitted over the flange to prevent ingress of dust or moisture when the front cover is replaced.

Figure 10
Flush mounting frame

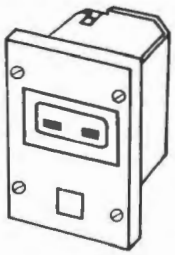
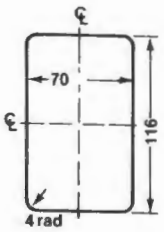


Figure 11
Panel cut-out



Rear mounting frame

A mounting kit consisting of front frame, mounting ring and two adjustable depth supports. As can be seen in fig. 12 the starter can be base mounted, panel depth 71mm, or mounted using the adjustable depth supports, panel depth 115-132mm. The front frame requires a 74.5mm dia. hole for mounting and is secured to the panel using the mounting ring and screws supplied, see figs. 12 and 14. When using the adjustable depth supports the lower sections are secured to the base plate, (see fig. 13, for mounting details) and the top sections are loosely fitted to the starter. The starter assembly is then fitted to the lower supports ensuring a clearance of 0.6 to 1.0mm between front frame and starter when secured.

Figure 12
Side view of rear mounting frame assembly

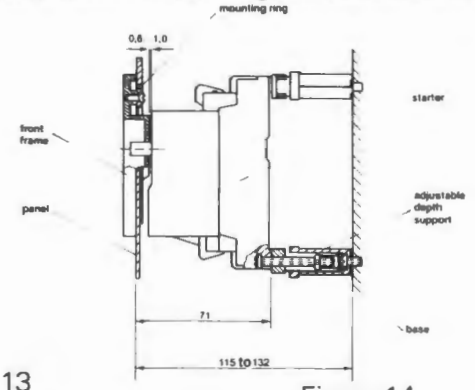
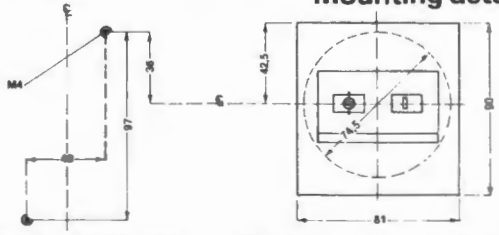


Figure 13
Base plate mounting details

Figure 14
Front frame mounting details



RS data

Operating accessories

Padlocking attachment (347-949) and emergency stop push button attachment (347-933) may be fitted to the aforementioned enclosure and mounting frames. The attachments directly replace the standard push button diaphragms, see figs. 15 and 16, maintaining protection to IP55.

Figure 15 **Padlocking attachment**

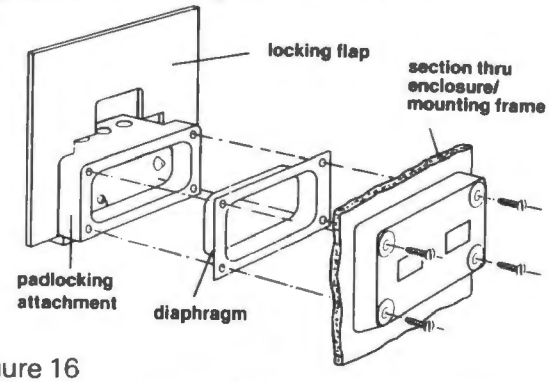


Figure 16
Emergency stop push-button attachment

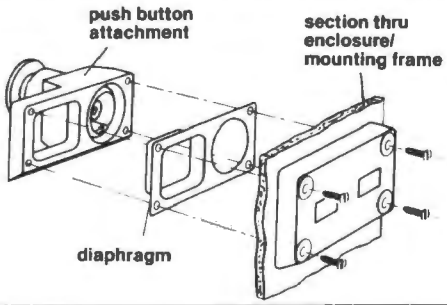
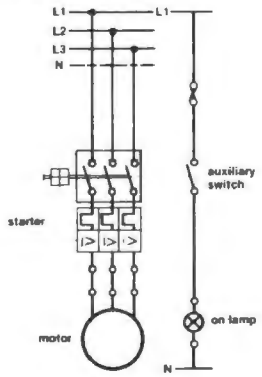


Figure 17 **Visual operational indication by using a manual motor starter with auxiliary make contact**



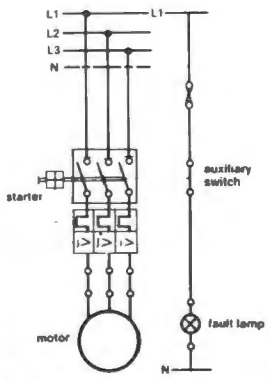


Figure 18 **Visual fault indication by using a manual motor starter with auxiliary break contact**

Figure 19 **Two motors interlocked against each other by means of a shunt trip and auxiliary contact of the manual motor starter**

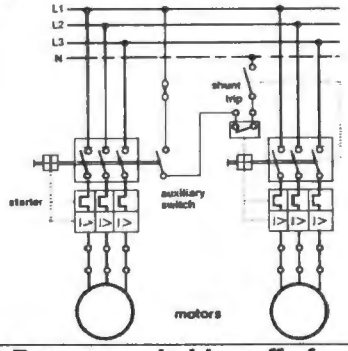


Figure 20 **Remote switching off of a manual motor starter by means of a shunt trip**

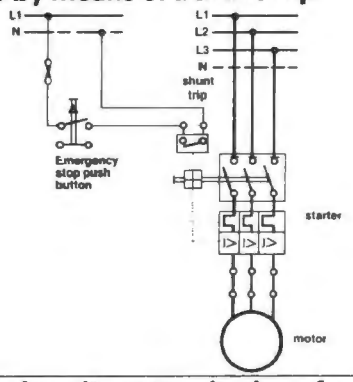
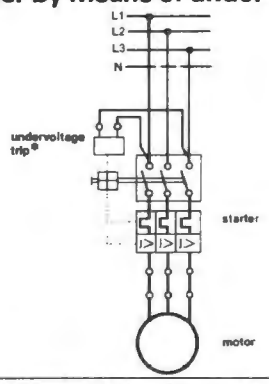
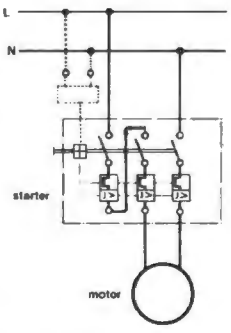


Figure 21 **Supply voltage monitoring of a manual motor starter by means of under-voltage trip**



*RS Stock No. 348-071 shown connected across phases. RS Stock No. 348-087 may be used connected any phase to neutral.

Figure 22 **Connections for Single phase motors**



Undervoltage trip RS Stock No. 348-087 may be connected across L and N if required (see safety applications).

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RS data

High speed opto-isolators 6N137 and Dual 6N137

Stock numbers 304 – 273 and 302 – 104

The 6N137 consists of a Ga As P input diode optically coupled to a unique integrated detector comprising a photodiode, high gain linear amplifier and Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.
The internal isolator design provides maximum DC and AC circuit isolation between input and output whilst achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt V_{cc} applied to the detector. The isolation and coupling is achieved with a typical propagation delay of 45ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a propagation delay of 25ns typical (single version only).
The 6N137 can be used in high speed digital interfacing applications where common mode signals must be rejected, such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished in system interfaces such as between a computer and a peripheral memory, printer, controller, etc.
The Dual 6N137 is equivalent to the HCPL-2630.

Features

- LSTTL/TTL compatible: 5V supply
- Ultra high speed typically 10M bit/s (NRZ)
- Low input current required
- High common mode rejection
- Guaranteed performance over temperature range
- 3000 Vdc withstand test voltage
- Enable input available (single type only)

Absolute maximum ratings

(No derating required up to 70°C). Where two figures are given (e.g. 20/15) the first is for single version, the second for dual version.

Operating Voltage Range — 4.5 to 5.5V (7V 1 Minute Maximum)
Storage Temperature — −55°C to + 125°C
Operating Temperature — 0°C to + 70°C
Lead Solder Temperature — 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current — 40/30mA (≤ 1msec duration)
Average Forward Input Current — 20/15mA
Reverse Input Voltage — 5V
Enable Input Voltage — 5.5V (Not to exceed V_{cc} by more than 500mV)
Output Current — 50/16mA
Output Collector Power Dissipation — 85/60mW
Output Voltage — 7V

Electrical characteristics T_A = 0 to + 70°C, V_{cc} = 4.5 to 5.5V unless otherwise stated

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Note
Input Current, Low Level	I_{FL}		0	—	250	μA	
Input Current, High Level	I_{FH}		6.3	—	15	mA	5
High Level Output Current	I_{OH}	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250μA, V_E = 2.0V		50	250	μA	
Low Level Output Voltage	V_{OL}	V_{CC} = 5.5V, I_F = 5mA, V_{EH} = 2.0V, I_{OL}(Sinking) = 13mA		0.5	0.6	V	
High Level Enable Voltage	V_{EH}		2.0		V_{CC}	V	
High Level Enable Current	I_{EH}	V_{CC} = 5.5V, V_E = 2.0V		−1.0		mA	
Low Level Enable Voltage (Output High)	V_{EL}		0		0.8	V	
Low Level Enable Current	I_{EL}	V_{CC} = 5.5V, V_E = 0.5V		−1.6	−2.0	mA	
High Level Supply Current (per channel)	I_{CCH}	V_{CC} = 5.5V, I_F = 0, V_E = 0.5V		7	15	mA	
Low Level Supply Current (per channel)	I_{CCL}	V_{CC} = 5.5V, I_F = 10mA, V_E = 0.5V		13	18	mA	
Input-Output Insulation Leakage Current	I_{I-O}	Relative Humidity = 45%, T_A = 25°C, t = 5s, V_{I-O} = 3000Vdc			1.0	μA	1
Resistance (Input-Output)	R_{I-O}	V_{I-O} = 500V, T_A = 25°C		10^{12}		Ω	1
Capacitance (Input-Output)	C_{I-O}	f = 1MHz, T_A = 25°C		0.6		pF	1
Input Forward Voltage	V_F	I_F = 10mA, T_A = 25°C		1.5	1.75	V	2
Input Reverse Breakdown Voltage	BV_R	I_R = 10μA, T_A = 25°C	5			V	
Input Capacitance	C_{IN}	V_F = 0, f = 1MHz		60		pF	
Current Transfer Ratio	CTR	I_F = 5.0mA, R_L = 100Ω		700		%	3
Fan Out (TTL Load)	N	V_{CC} = 5.5V			8		

**All typical values are at V_{cc} = 5V, T_A = 25°C

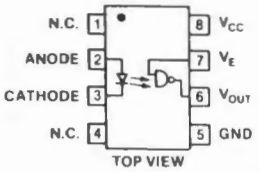
Switching characteristics at $T_A = 25°C$, $V_{CC} = 5V$

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Note
Propagation Delay Time to High Output Level	t_{PLH}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$		45	75	ns	
Propagation Delay Time to Low Output Level	t_{PHL}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$		45	75	ns	
Output Rise-Fall Time (10-90%)	t_r, t_f	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$		25		ns	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$, $V_{EH} = 3.0V$, $V_{EL} = 0.5V$		25		ns	
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$, $V_{EH} = 3.0V$, $V_{EL} = 0.5V$		15		ns	
Common Mode Transient Immunity at Logic High Output Level	CM_H	$V_{CM} = 10V$, $R_L = 350\Omega$, $V_O(min.) = 2V$, $I_F = 0mA$,		50		V/μs	4
Common Mode Transient Immunity at Logic Low Output Level	CM_L	$V_{CM} = 10V$, $R_L = 350\Omega$, $V_O(max.) = 0.8V$, $I_F = 5mA$,		−150		V/μs	4

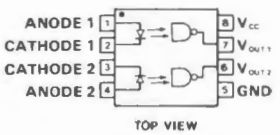
NOTES:

1. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5,6,7 and 8 shorted together.
2. At 10mA V_F decreases with increasing temperature at the rate of 1.6mV/°C.
3. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
4. Common mode transient immunity in Logic High Level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low Level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$).
5. 6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Figure 1
Pin connections

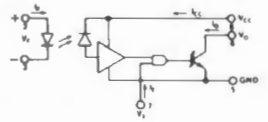


(a) 6N137



(b) Dual 6N137

Figure 2
Internal schematic



NOTE:
A 0.01 to 0.1uF bypass capacitor must be connected between pins 8 and 5.

TRUTH TABLE
(Positive Logic)

Input V_F	Enable V_E	Output V_O
H	H	L
L	H	H
H	L	H
L	L	H

Typical Characteristics

Figure 3
Opto-isolator Collector characteristics

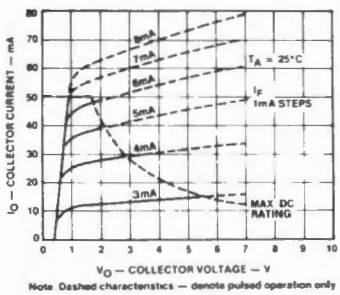


Figure 4
Input Diode Forward characteristics

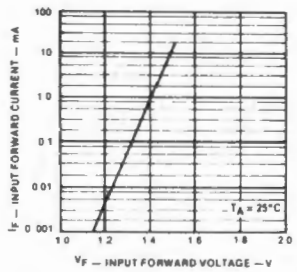


Figure 5
Output Current, I_{OH} vs. Temperature

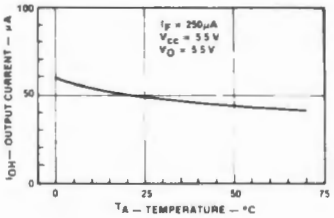


Figure 6 **Input-Output characteristics**

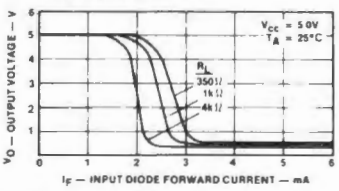


Figure 7 **Output Voltage, V_{OL} vs. Temperature and Fan-Out.**

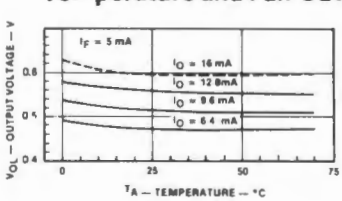
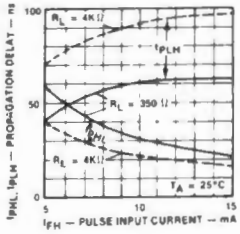


Figure 8 **Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.**



Definitions

Logic Convention. The 6N137 is defined in terms of positive logic.

Bypassing. A ceramic capacitor (.01 to 0.1μF) should be connected from pin 8 to pin 5 (Figure 15). Its purpose is to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 20mm.

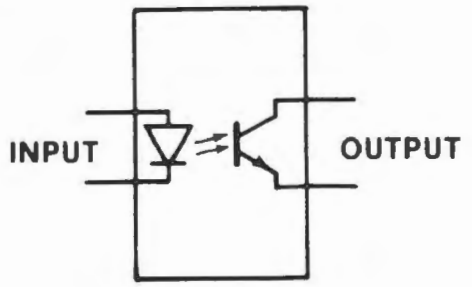
Polarities. All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

Enable Input. No external pull-up required for a logic 1, i.e., can be open circuit.

Phototransistor vs Integrated Detector

A common type of optically coupled isolator (Figure 9) uses a phototransistor for a detector where the transistor provides the gain necessary to interface with logic circuits. The major problem with this phototransistor isolator is bandwidth. This is due to the fact that both the detection of the photons and the amplification of the resulting photo current occur in the same physical structure in the phototransistor. The large feedback capacitance between the collector and the base is what essentially limits the phototransistor bandwidth.

Figure 9 **Phototransistor isolator**



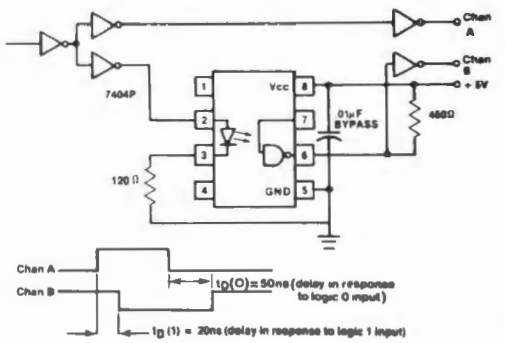
The 6N137 design greatly reduces this bandwidth limitation by proper optimization of the detector. The detector element is a monolithic structure, consisting of a photodiode, which collects the light; and a linear high speed amplifier (Fig. 2), which amplifies the resultant photo current. Functional separation of the photodiode from the amplifier reduces feedback capacitance to less than 1pF, thus making possible bandwidths up to 20MHz. The device, in detail, consists of a gallium arsenide phosphide input diode and a monolithically integrated detector at the output. The detector comprises a photodiode followed by a linear amplifier which drives a Schottky clamped output transistor. This output circuit is temperature, voltage, and current compensated to be truly compatible with standard TTL and DTL circuits. It also has a DTL/TTL compatible strobing input; with logic '0' at the strobe input, the output is held at logic '1', regardless of input conditions at the gallium arsenide phosphide diode. The basic features of the 6N137 are compared to phototransistor types in Table 1.

TABLE 1			
Isolator Types	**Bandwidth BW**	**Propagation Delay**	**Common Mode Rejection**
6N137 (IC Compatible Optical Isolated Gate)	20 MHz (Data Rate)	60ns	10V/10MHz
Phototransistor Types	100 kHz	6μs	3V/1MHz

TTL interfacing

The 6N137 is TTL (also DTL) compatible at both input and output requiring only 5mA input current to sink 13mA at the output — that is, it has 8-gate fan-out capability at 5mA input. The device interfacing with TTL inverters is demonstrated in Figure 10, the circuit for testing response delays. The inverting mode achieves the best speed performance, with typical delays of 20ns and 50ns. The current limiting resistor in series with the input diode is 120Ω, allowing approximately 10 mA of current to flow in on the 'on' state. The output load resistor is only 450Ω– due to the greater sinking capability of the output transistor.

Figure 10 **Response delay between TTL gates**



The input diode turn-on delay time of the 6N137 is a function of the input charging time. This delay time is most easily improved by simply adding a capacitor in parallel with the input current limiting resistor and operating from a low impedance source. In general, the capacitor should be a low inductance type with a value for a time constant of 15 to 30ns with the current limiting resistor. If the current limiting resistor is 100Ω, the capacitor should be 150 to 300pF.

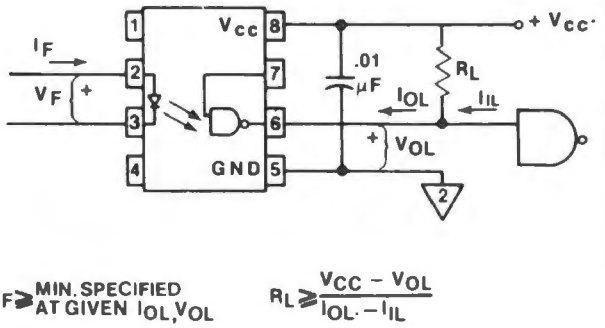
On the output side of the isolator, speed is enhanced by using the lowest possible value of pull-up resistance which is consistent with the current sinking capability of the isolator collector. The stray capacitance to ground should also be minimized. An output pull-up resistor is recommended to improve noise immunity and speed of response in moving to logic '1' output.

Line receivers

When digital data is transmitted over an appreciable length of transmission line (even less than a metre), there arises a possibility of ground shift, ground looping, etc. Opto-isolators can reduce the amount of ground loop current and the effects of the resulting common mode voltage. They are, therefore, very useful as line receivers.

Most line drivers are capable of sourcing a line voltage higher than the minimum ($\approx$ 1.5V) needed to turn "on" an opto-isolator. They usually also deliver a line current greater than the value of I_F as determined with reference to Figure 11. It is possible, of course, to design a line driver that will source the proper current and no more, but that is usually not good practice. Good practice is to drive the line with all the voltage and current available, then deal with the excess in the design of the termination of the line.

Figure 11 **Input and output considerations**



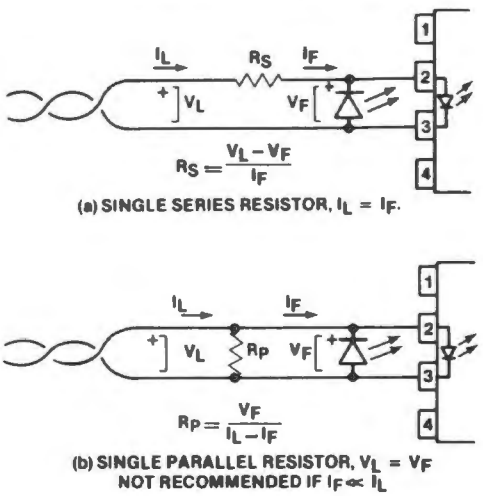
In the design of the termination, the "off" state is usually ignored unless pre-bias is used. There are usually three objectives in the design of the termination:

(A) proper "on" state I_F
(B) threshold level, I_{Fth} (to switch the output)
(C) reflections due to impedance mismatch.

Resistive Terminations

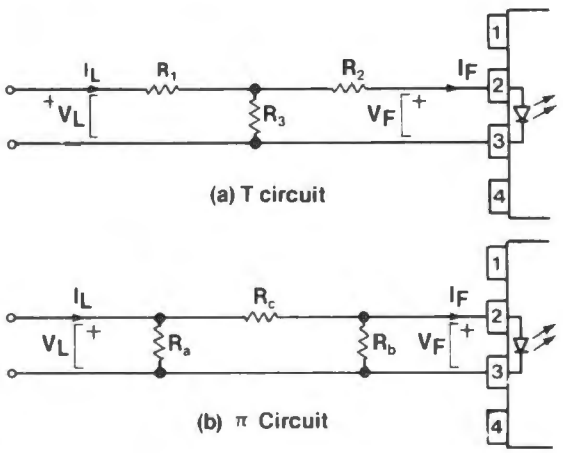
Objective (A) is mandatory; objectives (B) and (C) are discretionary. If discretion allows (B) and (C) to be neglected, the termination may be as simple as in Figure 12 requiring only a single resistor. In most cases, the series resistor termination of Figure 12 (a) would be used because it will accomodate a broader range of driver and line resistance variables. It is slower than the single parallel resistor termination of figure 12 (b) because the input diode is driven from a higher impedance. Slowness can be remedied with a peaking capacitor in parallel with R_S as previously explained; if peaking capacitance is applied, the anti-parallel diode should be used (even if the driver is polarity *non*-reversing) to allow the peaking capacitor to charge and discharge the maximum amount.

Figure 12 **Single–resistor terminations using opto-isolators as line receivers**



When, in addition to proper I_F, consideration must be given to either threshold current. I_{Fth}, or to line reflections, an additional resistor provides one additional degree of freedom. A two-resistor termination can accommodate the additional objective of either setting the I_{Fth} level or of approximate impedance matching but not both. To satisfy all three of the design objectives requires a three resistor termination in either "π" or "T" configuration.

Figure 13 **T and π circuits**

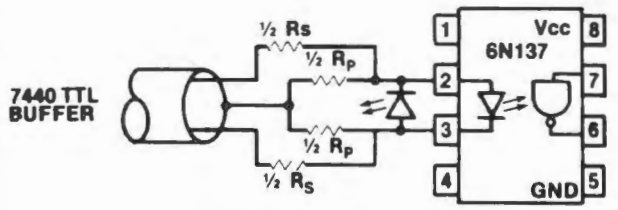


The 6N137 may be used as line receivers in either single-ended or balanced line applications. The turn-on voltage of the input diode establishes a threshold for the flow of current, thereby making the noise immunity higher than it would be for a linear line receiver. In many applications, this noise immunity is high enough that only a single-ended transmission line is required. For transmission over long distances or in very noisy environments, a balanced system should be used.

Figure 14 – demonstrates the use of the 6N137 as a balanced line receiver, using 7440 line driver. The resistor values are chosen in each case to match the line driver to the isolator line receiver. The line driver should be designed to supply more current

than the isolator input diode requires; this permits the use of a shunt resistor at the receiving end for better impedance matching and improved noise immunity. To maintain a reasonable impedance match during the negative excursion when the isolator input diode is reversed biased, a diode having about the same turn-on voltage as the input diode should be connected in reverse polarity across the input diode. For this purpose two silicon diodes in series could be used, or one LED, such as the RS standard red 0.2in LED.

Figure 14 **Typical line driver/receiver system**



Formulas for the terminating resistances are given below.

TABLE 2

	Basically	Given R_O, I_L	Given R_O, V_L	For best CMR
R_P	$\frac{V_D}{I_L - I_D}$	$\frac{V_D}{I_L - I_D}$	$R_O\left(\frac{V_D}{V_L - I_D R_O}\right)$	Connect ½ R_P from each side of isolator input to cable shield.
R_S	$\frac{V_L - V_D}{I_L}$	$R_O - \frac{V_D}{I_L}$	$R_O\left(1 - \frac{V_D}{V_L}\right)$	Connect ½ R_S in series from each line to input terminal of isolator.

Where:

R_O – Line-to-line terminating resistor which gives least reflection.

V_L, I_L – line-to-line voltage and line current with R_O connected.

V_D, I_D – isolator input diode forward voltage and current.

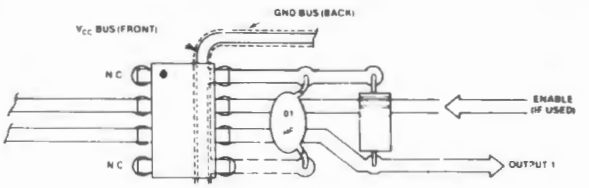
Circuit board layout

Careful attention is required for the 6N137 circuit layout due to the high gain employed in its internal amplifier. Power Supply lead lengths (Pins 5 and 8) are particularly important as their inductance provides an impedance across which a positive feedback signal may appear. A socket may be used, but it should be of a type having very short lead lengths. Proper bypassing is also essential. A total of at least 1μF of capacitance from V_{CC} to ground should be used on the board. Part of this 1μF may come from other bypasses installed to serve other circuits on the same board. In addition to the 1μF total, a bypass capacitor of 0.01μF should be connected directly from Pin 8 to Pin 5 of each 6N137 used on the board. These individual bypass capacitors must be low inductance disc ceramic. It is also important to have adequate bypassing for those circuits whose response is related to the signals produced in regenerative phase (circuit feedback) with variations in the V_{CC} line voltage. If the common practice of having 1μF for each two circuits is adopted, there should be no problem, and much less bypassing will ordinarily suffice.

Common mode decoupling

Common mode decoupling can be significantly enhanced by running a ground trace midway between the rows of isolator terminals. This trace is, of course, connected to the output ground (Pin 5) of the 6N137 (see Figure 15). Its purpose is to cause electric potential at the input side to be coupled to ground at the output, rather than to some signal amplifying terminal. If no socket or if in-the-board socket pins are used, this ground lead may be simply a printed trace, but if a socket is used, the ground trace should be paralleled by a piece of grounded wire running up over the socket. When the common mode voltage is very high (>1000V) the ground wire should be insulated to prevent electric discharge from the ground wire to the input terminals.

Figure 15 **Typical printed circuit board layout**



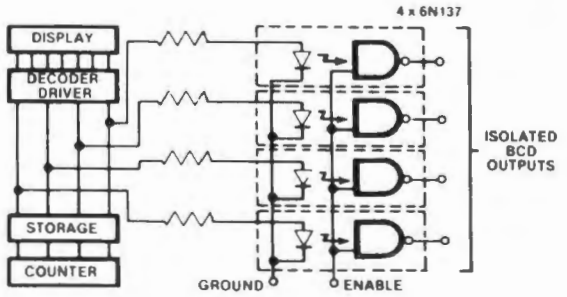
RS data

Typical applications

Ground loops involving peripheral equipment are effectively prevented by the use of optically coupled isolators. A typical situation is shown in Figure 16 in which the information on a set of BDC lines is made available at the electrically isolated outputs of the optically coupled isolators.

Although the use of the enable feature of the 6N137 is not always required, strobing of the enable inputs improves propagation delay times and helps to eliminate the change-of-state glitches that are sometimes present on BCD and other word lines. When the enable inputs are held at logic '0' (low) the outputs will all be at logic '1' (high). When the enable inputs are high, the outputs will be low on only those isolators whose **isolated** input is at the logic '1' state; the other outputs will remain high.

Figure 16 **Strobed optically coupled isolators**



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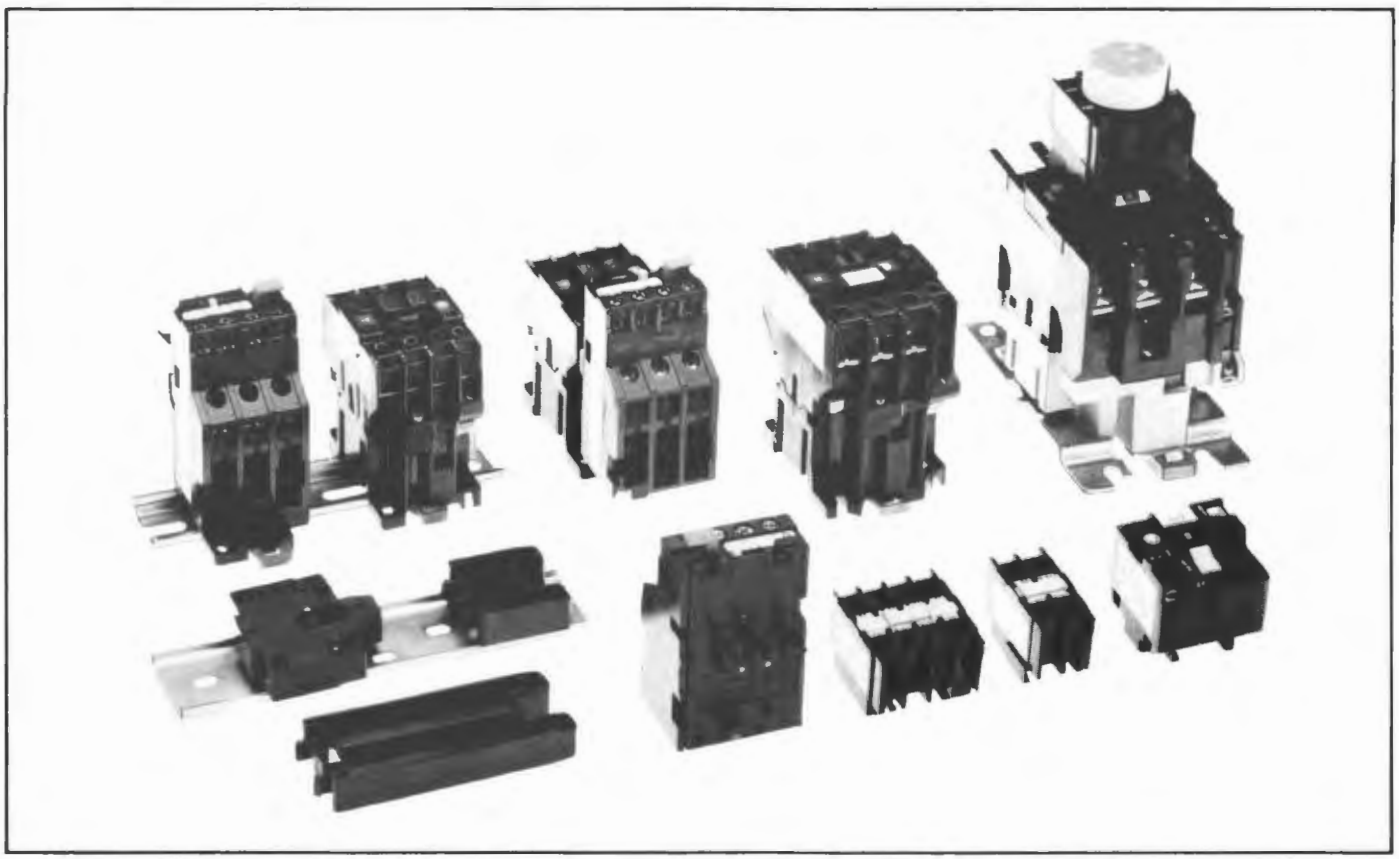
RS data

Control gear components 'd' range

The RS 'd' range of contactors, control relays and accessories is designed to provide a versatile and comprehensive motor control gear system comprising high quality, easily maintained components of proven reliability.

Features

- All contactors in this range are for use with ac control. The control voltage for both 50Hz and 60Hz is clearly marked on a tag attached to the coil. This may be seen, on the outside of the contactor, when the coil is fitted.
- Contactor main poles have double break, silver cadmium oxide contacts. The moving contacts have lateral guiding to ensure central positioning and even wear. Shock absorbers limit contact bounce and the resulting wear caused by arcing.
- Control relays have wiping contacts and serrated surfaces to give good performance even for low power switching (of associated electronic equipment, for example). Minimum switching level: 0.6VA with minimum values of 6V and 10mA.
- Control relay mouldings are designed to ensure that if a N/O contact welds accidentally, the N/C contacts will not close on de-energisation or if a N/C contact welds accidentally, the N/O contacts will not close on energisation.
- Control relays and contactors up to 32A are dual mounting, ie. they will either snap-fit onto a symmetric mounting rail, top hat profile to BS5584:1978 (RS stock no. 606-838), or they may be fitted to a flat surface via 2 × M4 screws.
- The 40A and 63A versions may be fitted to a flat surface via 3 × M6 screws. Alternatively, the contactors can be straddled across two parallel support rails, 'C' profile (RS stock no. 606-844).
- A range of accessories is available which includes:
  Thermal overload relays with phase failure protection and electrically separate contacts.
  An adaptor to convert the overload relays, up to 25A, to free standing units.
  Mechanical interlock kits, clip-on auxiliary contact blocks in instantaneous and time delayed versions and mechanical latching blocks.
- Coils are available separately for replacement purposes.



Dimension information

Contactors and control relays	RS stock nos. for each unit listed under control voltages			Depth on rail dimensions[1]				
	110V	240V	415V	Fig	C	C_1	C_2	C_3
Contactor 9A-4kW	347-618	347-624	347-602	1	79	109	121	131
Contactor 12A-5.5kW	347-589	347-595	347-573	1	79	109	121	131
Contactor 16A-9kW	345-454	345-460	345-476	1	84	114	163	136
Contactor 25A-11kW	347-523	347-539	347-517	2	94	124	133	146
Contactor 32A-15kW	345-482	345-498	345-505	2	99	129	138	151
Contactor 40A-22kW	347-494	347-501	347-488	3	112	142	–	164
Contactor 63A-37kW	347-466	347-472	347-450	3	112	142	–	164
Control relay 2 N/O + 2 N/C	346-457	346-441	–	1	79	109	121	131
Control relay 13 N/O + 1 N/C	346-435	346-429	–	1	79	109	121	131

Notes: [1]the dimensions are shown against each figure reference and include:
The basic unit (c), the unit with clip-on auxiliary blocks – instantaneous (C_1) latching (C_2) and time delayed (C_3).

Figure 1 **Size 1 contactor and control relay dimensions**

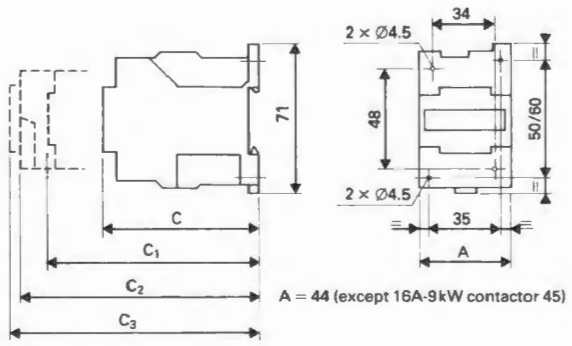


Figure 2 **Size 2 contactor dimensions**

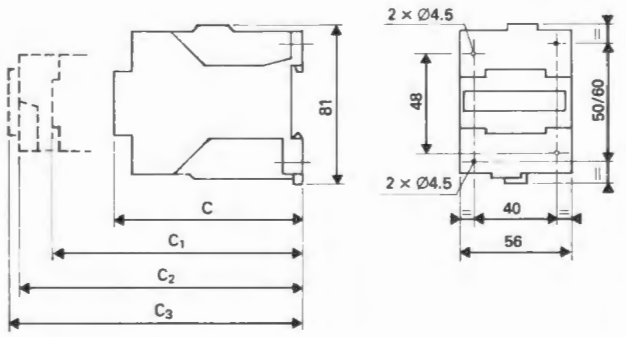
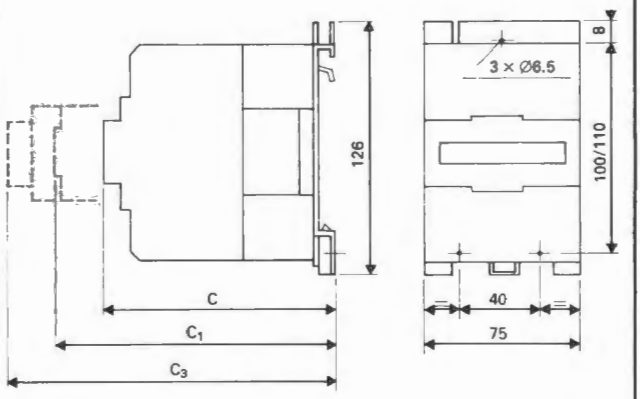


Figure 3 **Size 3 contactor dimensions**



Conformity to standards

Control relays: IEC 158-1, 337-1 and 255, NFC 63-110, 63-140 and 45-250, VDE 0660, BS775, CE1, NBN, NEN, SABS, GOST. Terminal markings to BS5583 (EN 50 011E).

Contactors: IEC 158-1, NFC 63-110, VDE 0660, BS5424, JEM 1038, terminal markings to BS5472 (EN 50 005).

Overload relays: IEC 292-2, NFC 63-650, VDE 0660 terminal markings to BS5472 (EN 50 005).

Approvals

Control relays: CSA, ASE, NEMKO, DEMKO, BV, GL, USSR, LROS.

Contactors: as control relays plus UL (except 40A version) RINA. Approvals for 16A and 32A pending.

Overload relays: CSA, ASE, BV, GL, USSR, LROS, , RINA, NEMKO, DEMKO.

Electrical ratings and dimensions contactors

Contactor rating			9A-4kW	12A-5.5kW	16A-9kW	25A-11kW	32A-15kW	40A-22kW	63A-37kW
Composition			3 pole + 1 N/O aux.					3 pole + 1 N/O + 1 N/C aux. 1	
Armature colour			brown	red	green	red	green	brown	red
Maximum dimensions when mounted in a panel	h.		71	71	71	81	81	126	126
	w.		44	44	45	56	56	75	75
	d.		79	79	84	94	99	112	112
Cabling max. CSA flexible (mm²)			2 × 4	2 × 4	2 × 6	2 × 6	2 × 10	2 × 10	2 × 16
Operating position Maximum deviation from vertical without derating			±30°						
Rated insulation voltage conforming to IEC 158-1			660V						
Frequency limits			25 to 400Hz						
Maximum permanent current Ith AC1 duty conforming to IEC 158-1, O ≤40°			25A	25A	32A	40A	50A	60A	80A
Making capacity I rms conforming to IEC 158-1			250A	250A	250A	450A	480A	800A	1000A
Breaking capacity conforming to IEC 158-1	220-380-415-440V		250A	250A	250A	450A	480A	800A	1000A
	500V		175A	175A	175A	400A	400A	800A	1000A
	660V		85A	85A	85A	180A	180A	400A	630A
Short time rating provided no current flows for 15 minutes before the overload. Ambient temperature ≤40°C	Duration:	1 sec	225A	225A	225A	360A	450A	720A	900A
		5 sec	130A	130A	155A	220A	270A	430A	600A
		10 sec	105A	105A	130A	200A	260A	320A	504A
		30 sec	70A	70A	90A	120A	180A	200A	230A
		1 min	56A	56A	70A	100A	140A	170A	200A
		3 min	35A	35A	50A	60A	80A	110A	125A
		15 min	30A	30A	40A	50A	60A	80A	90A
Short circuit protection Maximum fuse rating to BS88			25A	32A	40A	50A	63A	80A	125A
Impedance per pole			2.5mΩ	2.5mΩ	2.5mΩ	2mΩ	2mΩ	1.5Ω	1mΩ
Heat dissipation per pole at rated current	AC1 duty		1.56W	1.56W	2.5W	3.2W	5W	5.4W	6.4W
	AC3 duty		0.20W	0.36W	0.6W	1.25W	2W	2.4W	3.9W
Motor control *Rated current ie.* AC2, starting slip ring motors; AC3, starting squirrel cage motors; AC4, starting plugging, including squirrel cage motors			9A	12A	16A	25A	32A	40A	63A
⅄ △ star delta*			–	20A	–	40A	–	65A	107A
Power rating AC2, AC3, AC4	220/240V	kW	2.2	3	4	5.5	7.5	11	18.5
		hp	3	4	5.5	7.5	10	15	25
	380V	kW	4	5.5	7.5	11	15	18.5	30
		hp	5.5	7.5	10	15	20	25	40
	415V	kW	4	5.5	9	11	15	22	33
		hp	5.5	7.5	12.5	15	20	30	44
	440V	kW	4	5.5	9	11	15	22	33
		hp	5.5	7.5	12.5	15	20	30	44
	660V	kW	5.5	7.5	7.5	15	18.5	30	37
		hp	7.5	10	10	20	25	40	50
⅄ △ star delta*	220/240V	kW	–	5.5	–	11	–	18.5	30
		hp	–	7.5	–	15	–	25	40
	380V	kW	–	10	–	13.5	–	30	55
		hp	–	13.5	–	25	–	40	75
	415/440V	kW	–	10	–	22	–	37	59
		hp	–	13.5	–	30	–	50	80

Mechanical life –20 × 10^6 operations
Electrical life at full load current (AC3) –2.5 × 10^6 operations.

*Where no values are shown the contactor has not been tested for this application (ratings pending 16A and 32A types).

Coils

The following information is for coils available separately or as fitted into the contactors and control relays when first supplied. The chart provides an easy reference guide for coil replacement.

RS stock no. for Coil only	Nominal control Voltage Un (50Hz)	Min/Max coil voltage[2] and frequency				As used in:	Coil size reference
		U min. 50Hz	U max.	U min. 60Hz	U max.		
347-220	110V	102	117	110	130	9A, 12A, 16A contactors and control relays	1
347-236	240V	231	251	245	266		1
347-214	415V	398	442	440	481		1
347-191	110V	105	112	109	122	16A[1] old type 25A and 32A contactors	2
347-208	240V	233	258	254	279		2
347-185	415V	415	440	440	480		2
347-163	110V	110	124	130	147	40A and 63A contactors	3
347-179	240V	235	249	277	294		3
347-157	415V	407	440	481	519		3

Notes

[1]The 16A contactors (frame size 2) as previously supplied by RS under stock nos. 347-551 (110V coil) 347-567 (240V coil) 347-545 (415V coil) may be fitted with replacement coil from this range.

[2]The operating limits are listed in the following table:

Coil size	Operating limits		Average consumption (ac supply)		Average operating time[3]		Heat dissipation (sealed)
	pull-in %Un	drop-out %Un	50Hz inrush/sealed	60Hz inrush/sealed	closing	opening	
1	85-110%	30-55%	70VA/8VA	80VA/8VA	12 to 22ms	4-12ms	1.8 to 2.7W
2	85-110%	30-55%	100VA/9VA	100VA/9VA	15 to 25ms	7-15ms	2.5 to 3.5W
3	85-110%	30-60%	200VA/20VA	200VA/20VA	20 to 26ms	8-12ms	6 to 10W

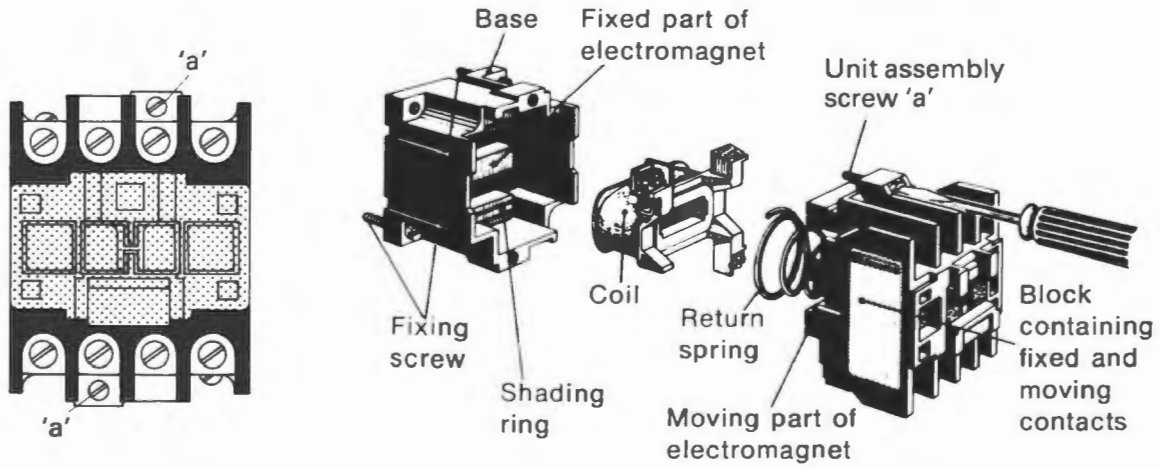
Notes:

[3] Maximum operating rate (at ambient temperature ≤ 55°C) = 3600 ops/hr.
The average operating time is based on the nominal voltage (Un). The closing time is measured from the moment the control supply is switched on to the time that contact is just made by the power poles. The opening time is measured from the moment the coil supply is switched off to the separation of the of the power poles.
Arcing time is dependent upon the circuit being controlled by the poles. For three phase current, arcing time is normally less than 10ms. The load is isolated from the supply after a time equal to the sum of the opening time and the arcing time.

Coil changing

To change a coil undo unit assembly screws 'a', see Figure 4, remove the upper housing of the contactor and lift out the coil. Note: after separation of the contactor the return spring should not be tampered with. To fit the replacement coil follow above instructions in the reverse procedure.

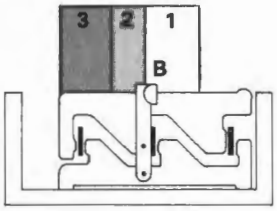
Figure 4



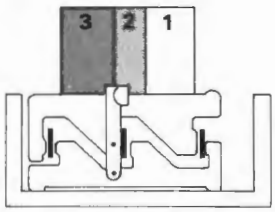
Thermal overload relays

The 'd' range is designed for use on both ac or dc supplies. They are *ambient temperature compensated* which means they are unaffected by ambient temperature variations within the limits –40°C to +60°C. Phase failure protection is effected via a *differential* tripping operation.

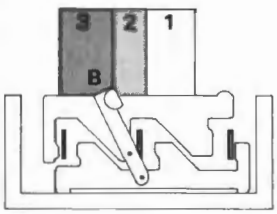
Figure 5 **Differential operation**



Cold position The lever arm (B) of the differential mechanism is in the 'rest' position, corresponding to the cold state of the bimetals.



Balanced operation In the hot state the lever arm (B) of the differential mechanism remains in zone 2 for normal operation. In the event of overload the lever moves into zone 3 and the protection relay trips.



Unbalanced operation In the event of single phasing the corresponding bimetal (in this case the one on the right) remains in the cold position and inhibits the displacement of the lower carrier. This amplifies the movement of lever arm (B) towards the trip zone so that the trip mechanism operates at current values well below full load.

□1. Cold state
□2. Normal operating zone
□3. Tripping zone

Relay contacts (see Standard terminal markings).

The contacts are *electrically separated* to permit two circuits to be controlled. For example the alarm circuit may be at a much lower control voltage than that which operates the contactor coil.

The contacts are rated at 10A thermal. Terminal capacity for the relay contacts is 2 × 2.5mm² flexible conductor maximum.

A manual reset button and a full load current (flc) adjustment are also incorporated. The relays should be set at *full load current* and not at trip current.

Overload relay range

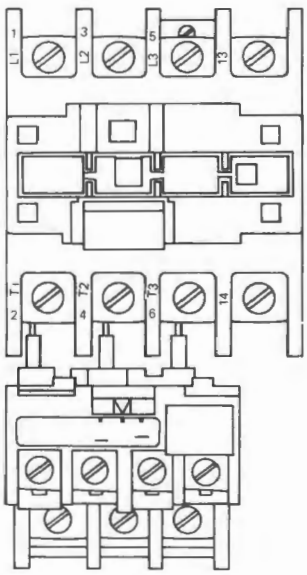
RS stock no.	Motor flc range A	For contactor size
347-444 347-438 347-422 347-416 347-400 347-393 347-387	0.63-1.0 1.0-1.6 1.6-2.5 2.5-4.0 4.0-6.0 5.5-8.0 7-10	9A-4kW
347-371	10-13	12A-5.5kW
347-365	13-18	16A-9kW
347-359	18-25	25A-11kW
345-511 345-527	23-32 28-40	32A- 15kW
347-343 347-337	23-32 30-40	40A- 22kW
347-321 347-315 347-309	38-50 48-57 57-66	63A- 37kW

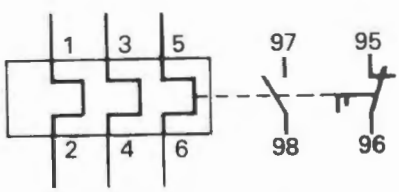
Fitting instructions for direct mounting of overload relays

Thermal overload relays should be fitted to contactors in the position as shown in Figure 6.

Having chosen an overload relay with the correct full load current (using the flc tables or motor manufacturer's data), the final trip current should be set using the pointer on top of the relay.

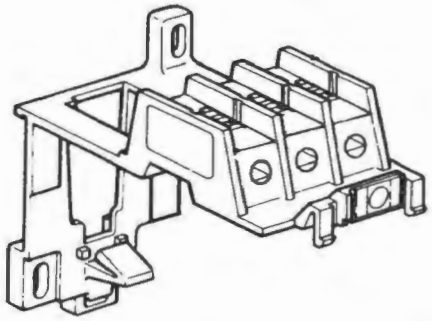
Figure 6 **Overload relay mounting**





Free standing adaptor (346-019)

Figure 7 **Free standing adaptor**



An adaptor for converting the RS 'd' range overload relays into free standing units. After conversion, the relays may be snap-fitted to symmetric DIN rail (RS stock nos. 424-131 or 606-838) or fixed to a flat surface using two M4 screws. The relays suitable for conversion are the ones designed to fit directly onto the 9A, 12A, 16A and 25A contactors.

Applications for free standing overload relays include:

Hard wiring of contactor to one overload where the plug-in pin spacings are not compatible, or where there is insufficient room under the contactor for direct mounting.

Hard wiring of a contactor to several overloads.

Figure 8 **Dimensions when fitted to the relay and DIN rail mounted**

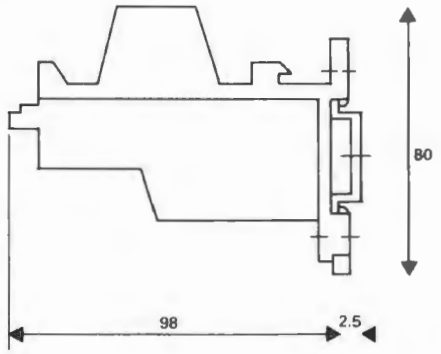


Figure 9 **Mounting details for direct-to-panel fixing**

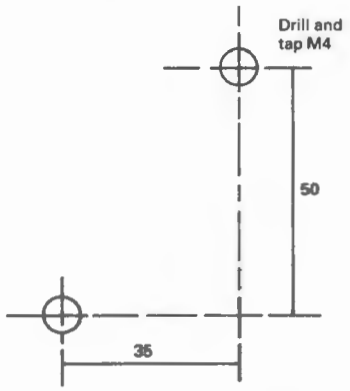
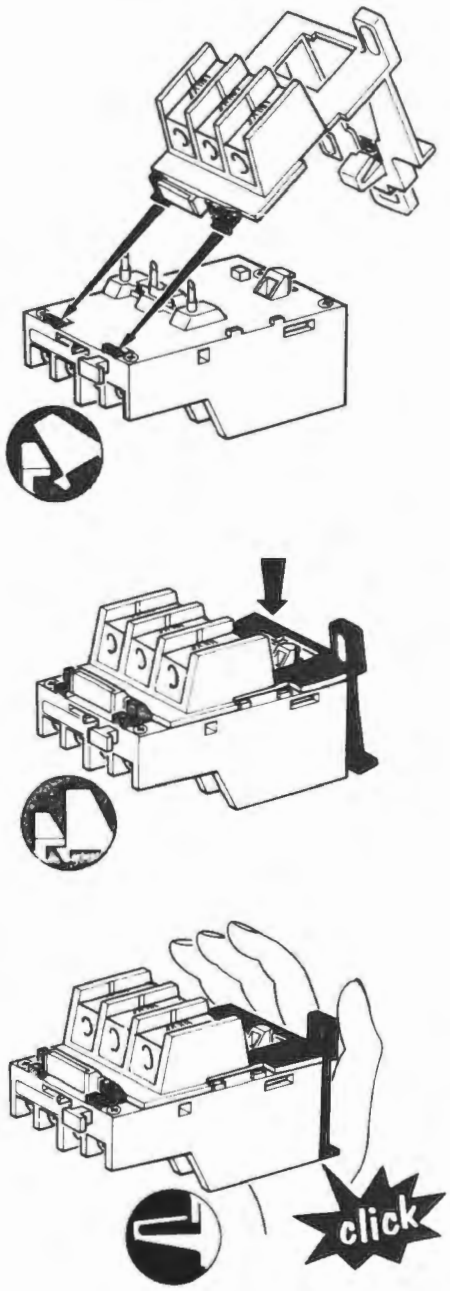


Figure 10 **Assembly instructions**



Mounting Alternatives

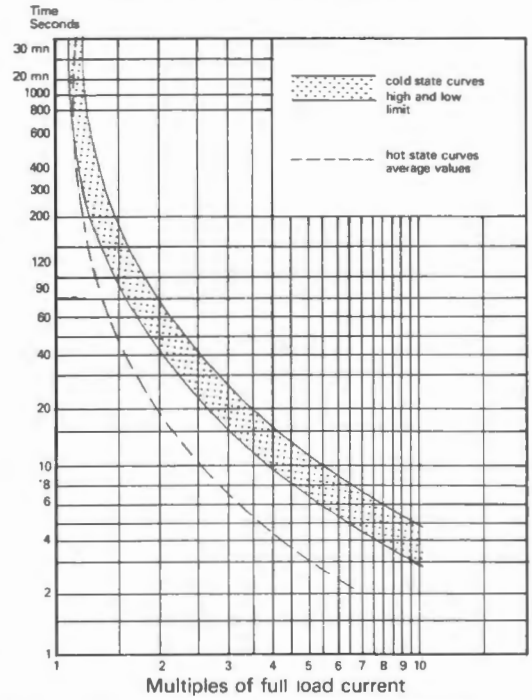
1. Onto symmetric DIN rail, top hat profile to BS5584: 1978 (EN50022, DIN 46277-3). This is the same style of mounting rail that is used for mounting contactors and control relays ('d' range and similar).
2. Onto a flat surface, such as a chassis plate. (See Figure 9 for mounting details).

Recommended BS88 fuses

For the short circuit protection of cables in motor starter applications.

Overload relay flc	BS88 fuse (A)
0.63-1.0	4
1.0-1.6	6
1.6-2.5	10
2.5-4.0	16
4.0-6.0	16
5.5-8.0	20
7-10	25
10-13	32
13-18	40
18-25	50
23-32	63
28-40	80
38-50	100
48-57	100
57-66	125

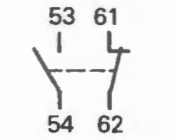
Figure 11 **Tripping curves – overload relays Time current characteristics**



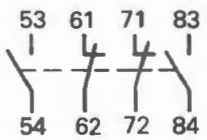
Clip-on auxiliary blocks

These clip-on accessories are for top fitting. The resulting increased dimensions are tabulated on page 2.

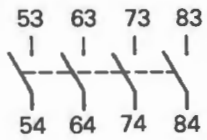
Instantaneous contacts



1 N/O + 1 N/C
347-292



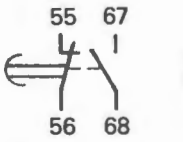
2 N/O + 1 N/C
347-286



4 N/O
347-270

Time delayed contacts

The time delay is effected pneumatically. It is thus unaffected by electrical interference or variations in the supply voltage.

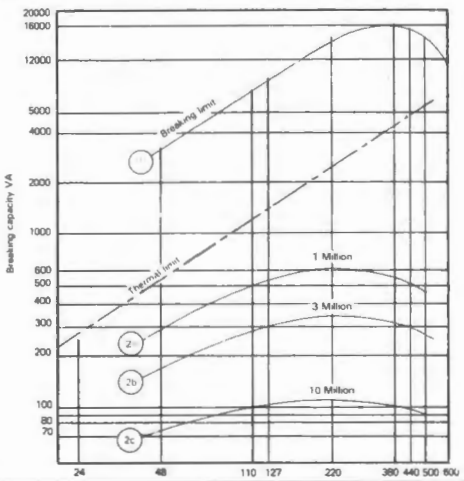


1 N/O + 1 N/C

Contact ratings for clip-on auxiliary blocks

The contacts have a thermal rating of 10A and are made from silver cadmium oxide (not to the same proportions as the contactors). They have a wiping action and serrated surfaces. They are ideally suited for applications such as series switching of dc control currents, low voltages (12-24V) and low power switching (minimum switching level 0.6VA with V min 6V and I min 10mA.

Figure 12 **ac rating of auxiliary contacts**

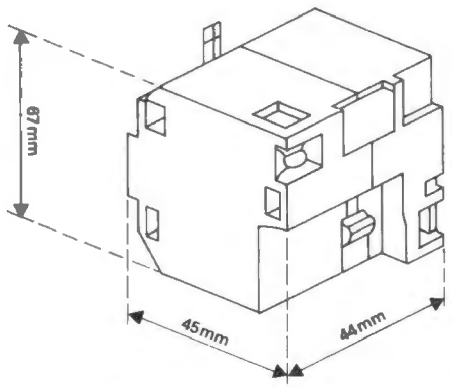


Control relays, overload relays and auxiliary contact blocks

Electric life:
(Inductive – 3,600 operations per hour).
1. Breaking limit of contacts.
2. Contact life.
(a) 1 million operations, relays and instantaneous/ time delay aux. contact blocks.
(b) 3 million operations, relays and instantaneous/ time delay aux. contact blocks.
(c) 10 million operations, relays and instantaneous contact blocks.

Latching clip-on block
(345-533 110V and 345-549 240V)

Figure 13 **Latching clip-on block**



The latch adder block is a clip-on device which is fixed, and operated in the same manner as all the other 'd' range adder blocks. The latch contains a mechanical latching mechanism which operates when the component armature closes, and the delatch coil which releases the mechanism. The latch mechanism is self-compensating thus keeping maximum pressure on the component poles for its mechanical life of 5 million operations. Its block construction does not affect the overall length or width of the component it is attached to; only the depth which is increased by 45mm.

The latch adder can be used on any 'd' range relays or the 9A to 32A contactors. It must be stressed that precautions should be taken to ensure that the delatch coil and the component coil are **never energised simultaneously.**

Although the delatch coil is only short-time rated a cut throat contact within the latch adder ensures the voltage remains on the delatch coil for less than 15ms, this is guaranteed even if the supply falls to 40% of the nominal voltage. However, a pulse of at least 10ms is required to ensure operation, and the latch is limited to 1800 ops/hour.

The delatch coil can be operated in two ways. Firstly a button on the front allows the block and the component to be delatched manually. Secondly the delatch coil can be operated through a local or remote contact using a control voltage of 110V or 240V.

Fitting instructions
Instantaneous and time delayed auxiliary contact blocks and latching blocks

The blocks can be fitted to contactors and control relays in one simple movement, see Figure 14, and are positively held in position by a spring operated latch.

For removal, the latch is raised and the block is slid off see Figure 15.

Figure 14 **Fitting auxiliary contact blocks**

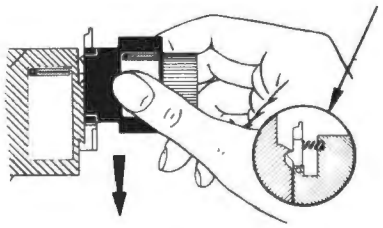
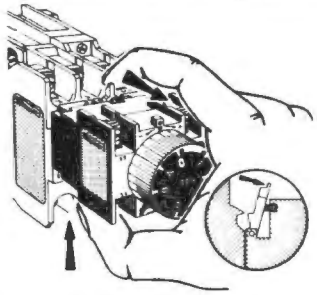


Figure 15 **Removal of auxiliary contact blocks**



Mechanical interlock kits

A mechanical interlock kit is designed to fit between two contactors allowing only one to be operative at any one time. Two kits are available, one to interlock any combination of any two contactors between 9 to 25A, ie. two 9A types or a 16A and 25A type, etc, the other one for similarly interlocking combinations of the 40 and 63A contactors. To mechanically interlock a pair of contactors the interlock mechanism is sandwiched in between the contactors, see Figure 16. Holding the interlocked pair together the bridge is inserted into the base to lock the contactors together (see Figure 17).

Figure 16

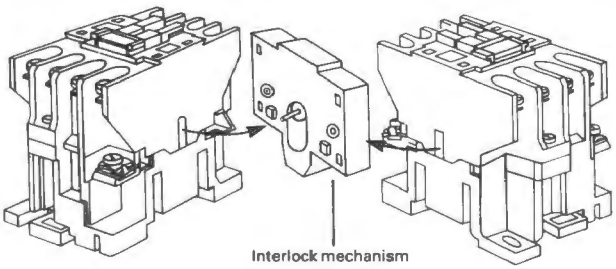
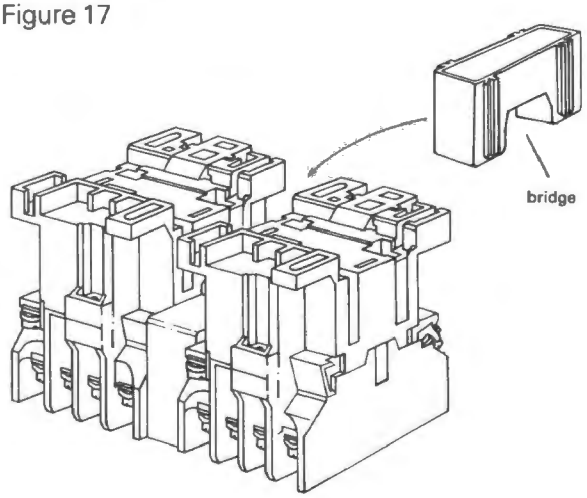


Figure 17



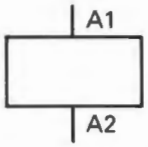
Enclosures

For suitable enclosures please see current RS catalogue. Two sizes from the industrial cases to IP54 range in steel have been introduced, suitable for contactors up to 35A. Suitable symmetric DIN rail is also available from RS.

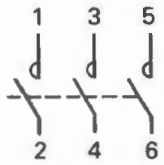
Standard terminal markings EN50005 (BS5472: 1977)

The RS range of control gear is marked according to this European Specification. A new standard for control relays, EN50011 (BS5583:1978), incorporates the same standard terminal markings here described.

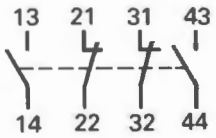
Coils
Marking: alpha-numeric
Odd number – incoming terminal
Even number – outgoing terminal



Main contacts
Marking: single numbers
Odd number – incoming terminal
Next even number – corresponding outgoing terminal



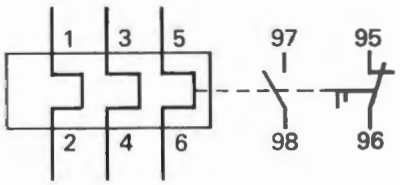
Auxiliary contacts
Marking: two numbers
First number – sequential
Second number – functional
ie. 1-2 N/C contacts
3-4 N/O contacts
1-2-4 changeover contacts



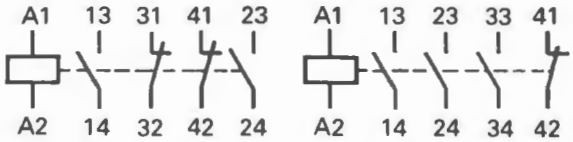
(contact sequence in accordance with EN 50 011 reference 22E)

Auxiliary contacts (special function)
Marking: two numbers
First number – sequential
Second number – functional
ie. 5-6 N/C contacts
7-8 N/O contacts

Overload relays
Marking: main circuit – as main contacts
auxiliary contacts: two numbers.
First number – normally 9.
Second number – functional.
ie. 5-6 N/C contacts
7-8 N/O contacts
5-6-8 changeover contacts.



Control relays
Marking: as auxiliary contacts.
Contact sequence, as shown, is in accordance with EN 50 011 designated by the distinctive letter E.



RS data

Full load current (flc) tables

3 phase motors							Single phase motors				
Motor rating		flc at line volts					Motor rating		flc at line volts		
hp	kW	220V	240V	380V	415V	500V	hp	kW	110V	220V	240V
¼	0.19	1.29	1.19	.75	.68	.5	1/12	0.07	2.31	1.16	1.06
½	0.37	2.48	2.27	1.43	1.31	1.0	⅛	0.1	3.15	1.58	1.44
¾	0.56	3.09	2.84	1.78	1.64	1.3	⅙	0.13	4.41	2.21	2.02
1	0.75	3.5	3.2.	2.0	1.8	1.5	¼	0.19	5.88	2.94	2.69
1½	1.1	4.9	4.5	2.8	2.6	2.2	⅓	0.25	7.77	3.88	3.55
2	1.5	6.4	5.8	3.7	3.4	2.8	½	0.37	11.1	5.56	5.08
3	2.2	9.5	8.7	5.5	5.0	3.9	¾	0.56	13.7	6.82	6.24
5	3.7	14.6	13.4	8.4	7.7	6.5	1	0.75	18.9	9.44	8.64
7½	5.6	20.6	18.9	11.8	10.9	10.	1½	1.1	24.2	12.1	11.1
10	7.5	27.5	25.	15.5	14.	12.5	2	1.5	28.9	14.5	13.3
12½	9.3	34.5	31.5	20.	18.	15.5					
15	11.2	41.	37.	22.5	21.	18.5					
20	15.	54.	50.	30.	28.	24.					
25	18.6	65.	61.	38.	35.	30.					
30	22.4	76.	70.	43.	40.	34.					
40	30.	99.	91.	57.	53.	45.					
50	37.	120.	107.	72.	66.	57.					

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Telephone: 0536 201234
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RS data

Fibre optic transmitter and receiver modules

Stock numbers 303–680, 303–696

High quality potted and sealed modules for p.c.b. mounting, specifically designed to ease the task of implementing fibre optic communication into system design. For use with RS terminated optical leads or any leads terminated in SMA connectors with a penetration not exceeding 9.8mm. Only a minimum number of external components are required to realise a complete working system. Particularly suited to data transfer applications in base-band modems, computer-peripheral circuits and other areas employing low data rates.
For general information on Fibre Optics see RS Data Sheet 4030.

Absolute maximum ratings

Transmitter supply voltage	+ 7 V max.
Receiver supply voltages	± 15 V max.
Operating temperature	0°C to 60°C
Storage temperature	− 25° to + 75°C
Pin soldering temperature	250°C for 8 secs max.

Note on RS-232-C

RS-232-C is an internationally accepted interface standard defining voltage levels, data rates, polarities, terminating impedances and other important parameters for data terminal to data communication equipment links. It is issued by the EIA (Electronic Industries Association) in the U.S.A. and is *not* connected in any way with RS Components Ltd. Many microprocessor-based and other computer systems use this interface standard. The RS Fibre Optic Modules are ideal for converting RS-232-C wired interfaces to optically isolated interfaces.

General application of modules

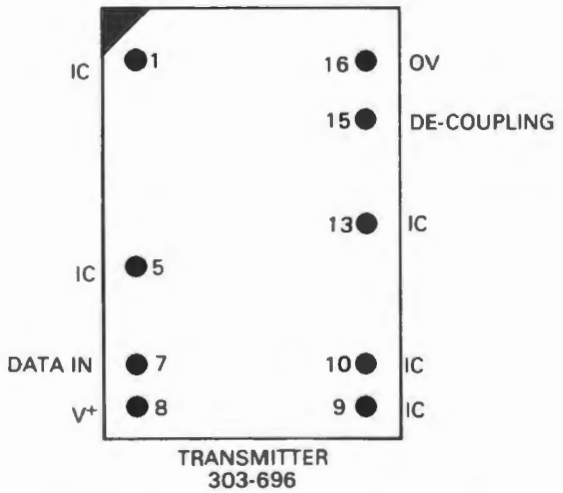
The RS Fibre Optic Transmitter and Receiver Modules are designed to simplify the integration of a fibre optic link into both new and existing systems, where their many advantages over traditional wire systems are desired or required. Problem areas solved by fibre optic links include:

earth loops
radio frequency interference
crosstalk
voltage isolation
isolation in medical equipment
data security
tranmission in hazardous areas

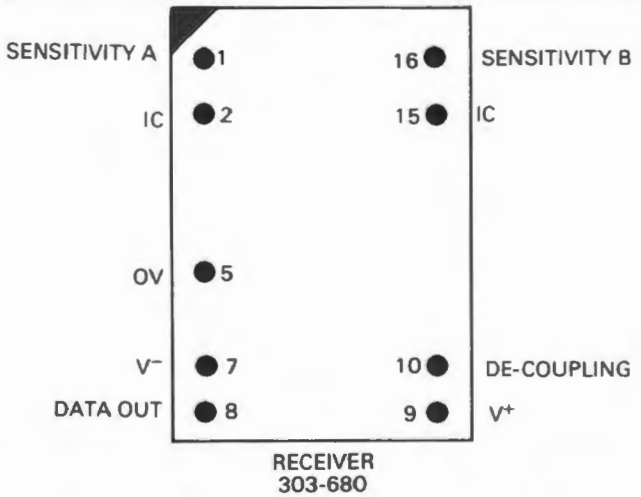
Features

- Very simple system implementation
- Interface directly to RS-232-C systems
- Will accommodate true d.c. levels
- Guaranteed to operate 20 kbits/s min.
- Efficient infra-red transmission

Pin connections (top view)



TRANSMITTER
303-696



RECEIVER
303-680

Pins marked IC are 'internally connected' and external connections must not be made to these.

RS data

Optical power calculations

Electrical and optical characteristics quoted on page two refer to measurements at 25°C. At temperatures much above this, an additional margin should be allowed in assessing the loss permissible between the transmitter and the receiver. Typically 3 dB would be an adequate extra margin. Note also that the optical characteristics are referred to 200 μm core fibre optic cable. (The RS terminated (glass) leads are 200 μm.) For other sizes of core different amounts of energy may be coupled to (or extracted from) the fibre cable. Such additional losses are generally proportional to the area of the core and can thus easily be determined by knowing the core diameter.

If a core size (D) of less than 200 μm is being used this *mismatch* loss at the transmitter end of the system will be

$$\left(\frac{D}{200}\right)^2$$

i.e. for 150 μm the additional loss will be

$$\left(\frac{150}{200}\right)^2 = 0.56$$

Expressed in dB:

$L_m = 10 \log_{10} 0.56 = 2.5$ dB loss

If a core size greater than 200 μm is being used there is no additional loss.

With core sizes less than 200 μm there is no additional loss at the receiver end. For cores greater than 200 μm there may (theoretically) be a loss at the receiver, but in practice this would normally be negligible.

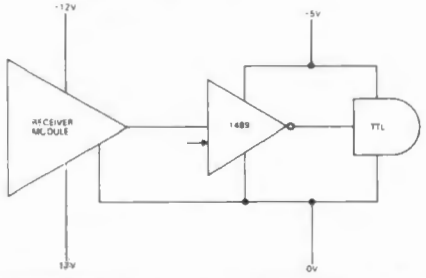
TTL compatibility

Although specifically designed to solve problems associated with RS-232-C interfaces, the modules may be used for TTL, with appropriate circuit changes.

At the transmitter end, simple removal of the 2k7 input resistor to pin 7 achieves TTL compatibility.

The receiver requires an RS-232-C – to – TTL interface circuit. The 1489 line receiver i.c. (RS stock number 309-593) is suitable for this purpose. The method of connection is shown in figure 5. (Note that the 3.3 kΩ resistor is omitted.)

Figure 5 **TTL Receiver**



CMOS compatibility

The same circuit as is used for TTL is applicable to CMOS. However, normal CMOS voltages are used in place of the 5V rail.

Design examples

(1) *The RS transmitter/receiver modules are being used with RS terminated glass leads. The ambient temperature is around 25° C. What is the greatest fibre length which may be used?*

Assume the worst case for the transmitter and say the optical output power s only 5 μW. Similarly, say we require 0.5 μW input power to the receiver. No temperature or core size mismatch losses are applicable. Therefore maximum optical attenuation allowable

$$= 10 \log_{10} \frac{5}{0.5} \qquad = 10 \text{ dB}$$

It is always advisable to allow a 3 dB margin for extraneous losses such as those associated with connectors which may not be dirt-free, bending of fibres, component ageing etc., just to make sure that the system continues to work for an extended lifetime. This leaves 7 dB for the fibre and in-line connectors. This could be two 50 m leads plus one in-line connector, giving a 100 m run.

Note that if worst case figures are not assumed, it may be possible to, say, double this to 200 m, although such a system may not be repeatable with other components.

Note also that although the transmitter emission peaks at 940 nm and the receiver sensitivity peaks at 900 nm, there is no great loss penalty incurred in practice. Similarly, RS glass leads are characterised at 840 nm. However, the extra attenuation at 940 nm amounts to only an additional 0.3 to 0.4 dB on a 50 m length.

(2) *Suppose a 3.1 dB/km, 200 μm cable is available in 1 km lengths. What is the longest possible transmission path length which may be set up?*

It is not unusual for the transmitter module emitter to give 15 μW output. Ignoring temperature losses and since there are no mismatch losses, the maximum attenuation is

$$10 \log_{10} \frac{15}{0.5} \qquad = 15 \text{ dB}$$

Without allowing for any extraneous losses, but taking 1 dB as a typical in-line connector loss, 4 km could be achieved. Working on worst case figures and allowing for extraneous losses, 2 km is realistic.

(3) *A 50 m link is required using 300 μm cable, exhibiting a loss of 10 dB/km. Is this feasible? The temperature range may extend to 50° C.*

Temperature loss = 3 dB (say)
Mismatch loss at transmitter = 0 dB
Mismatch loss at receiver = 0 dB (approx.)
Extraneous losses = 3 dB (say)
Cable loss = 0.5 dB
Total loss = 3 + 3 + 0.5
= 6.5 dB

Reference to example (1) shows that this system is feasible, as the maximum optical attenuation allowable is 10 dB.

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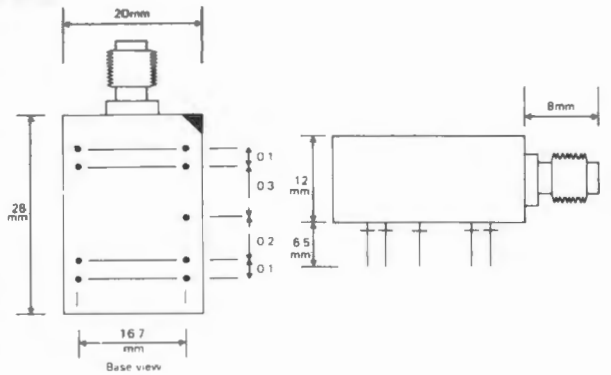
Figure 3 **Receiver dimensional details**



(4) Do not connect unassigned pins (those designated 'IC') to any other point, including the ground plane.
(5) All external components should be mounted with the minimum possible lead lengths. This especially applies to potentiometers, which should preferably be p.c.b. mounting types.
(6) Do not plug the modules in or out of circuit with the power connected, if socket strip mounting is used.
(7) For very short links, of the order of a few metres only, a 100Ω potentiometer, connected as a variable resistor, should be connected in series with the 27Ω resistor shown in the transmitter circuit, to limit the emitter current.

Circuit design notes

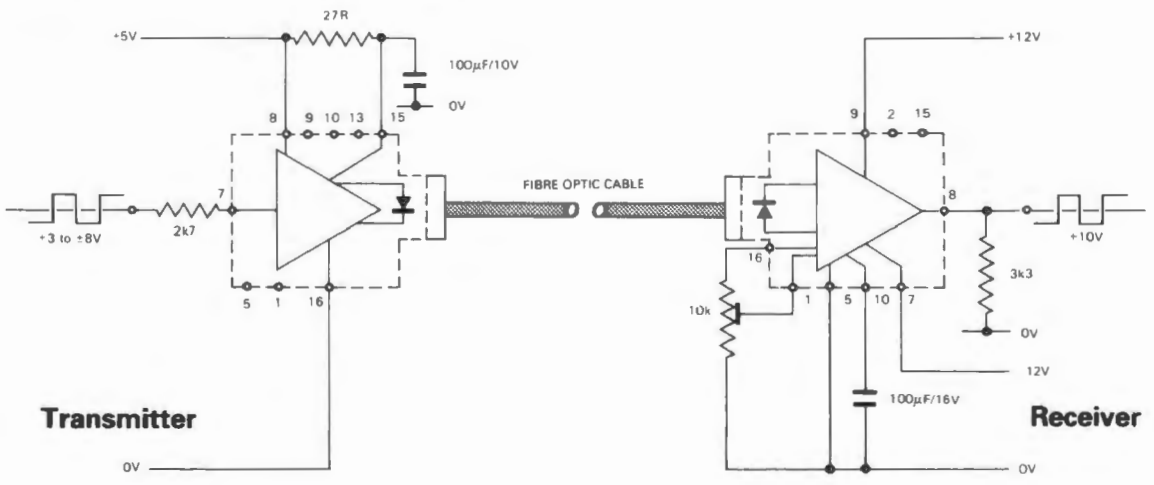
The basic mode of operating the transmitter and receiver modules is shown in the circuit diagram in figure 4. As can be seen, very few external components are required to realise a full, working system. It is, however, worth noting the following points in order to ensure trouble-free operation.

(1) If a p.c.b. is designed, preserve the maximum possible ground-plane material.
(2) Soldering is the preferred method of mounting the modules on the circuit board.
(3) Keep soldering time short and temperature low, consistent with acceptable joint quality, to avoid heat damage – see 'Absolute maxmum ratings'.

Operation

(1) Set up and check the circuit.
(2) Connect power to the transmitter and receiver.
(3) Connect an oscilloscope to pin 8 of the receiver.
(4) Adjust the 10kΩ receiver potentiometer for a 1:1 mark/space ratio of the received signal. (For short links the transmitter 100Ω variable resistor will require adjustment too.)

Figure 4 **Simplex interface link (for replacement of 'RS-232-C' cable link)**



IMPORTANT
- Check circuits thoroughly before connecting power
- Ensure optical connectors are secure but do not overtighten
- Do not exceed ± 8V at the transmitter data input

Electrical characteristics $T_A = 25°C$

	Parameter	Conditions	Min	Typ	Max	Units
Transmitter	Supply voltage		+4	+5	+6	V
	Quiescent current			+6		mA
	Peak current			+90		mA
	Input impedance			30		kΩ
	Data input levels		±3		±8	V
Receiver	Supply voltages		+11, −11	+12, −12	+13, −13	V
	Quiescent currents			+7.5, −0.08		mA
	Peak currents			+9.5, −6		mA
	Output impedance			3.3		kΩ
	Data output levels	±12V supply		±10		V
Data Rate			d.c.		20	kbits/s

Optical characteristics $T_A = 25°C$ (see also **Optical Power Calculations** on page 4)

	Parameter	Min	Typ	Max	Units
Transmitter	Power output	5	10		μW
	Peak emission wavelength		940		nm
Receiver	Power input required	0.5			μW
	Peak detection wavelength		900		nm

Module construction

The electronic circuits in each module are fabricated using thick-film technology and are interfaced to an opto-electronic emitter in the transmitter and an opto-electronic detector in the receiver. The modules are potted for ruggedness and then sealed. Optical connections are via SMA-type sockets and will accept RS 'glass' terminated leads, or any SMA fibre optic connector with a penetration not exceeding 9.8mm – see figure 1.

Figure 1 **Acceptable SMA plug-end profile**

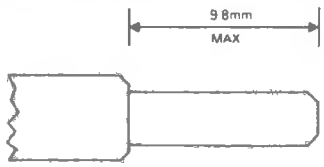
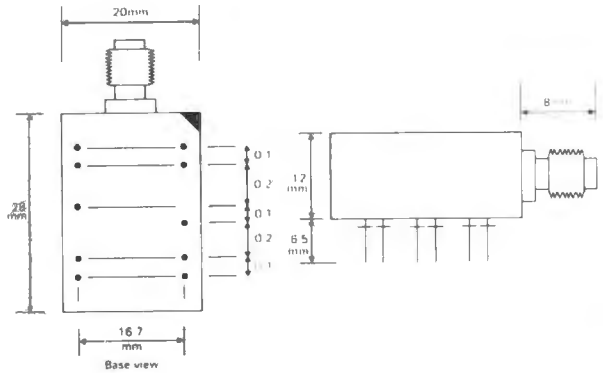


Figure 2 **Transmitter dimensional details**



The two *rows* of pins on each module are pitched at 0.1 inches. Note, however, that due to production constraints the pitching *between* rows is *not* 0.1 inches.

Exact dimensional information is shown in figure 2 and figure 3, and should be carefully studied prior to printed circuit board layout. Mounting into 'stripboards' and 'socket strips' is possible, but care should be exercised to avoid undue strain on the pins.

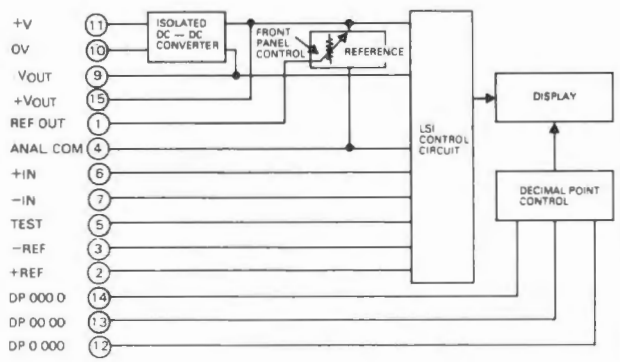
RS data

3½ digit L C D digital panel meter

Stock number 258-170

The RS 3½ digit LCD digital panel meter combines the low power requirements of a liquid crystal display and LSI semiconductor technology to provide a high performance digital panel meter within a DIN/NEMA standard case. Connections to the meter are made via a 24 way 0.1 in. gold plated edge socket, Stock No. 466-545.

Meter schematic diagram



Features

- Auto polarity
- Internal band gap reference
- 0.1% accuracy
- 0.5 in. high LCD display
- Automatic zero
- Isolated supply input
- Programmable decimal points
- DIN standard cut-out of 92×45 mm
- Reverse polarity protected*
- Over-voltage protected*
- Low power less than 10 mA at 5 V supply

Display

Polarity: Shown by minus sign for negative inputs.

Over-range: Shown by three least significant digits blanked.

Decimal points: Programmable at edge connector. To display decimal point, connect appropriate pin to $+V_{OUT}$, leave unconnected if decimal point not required.

Test facility: Connect test pin to $+V_{OUT}$ momentarily to turn on all display segments – prolonged use will 'burn' the display.

* With fuse fitted — see "connections" over.

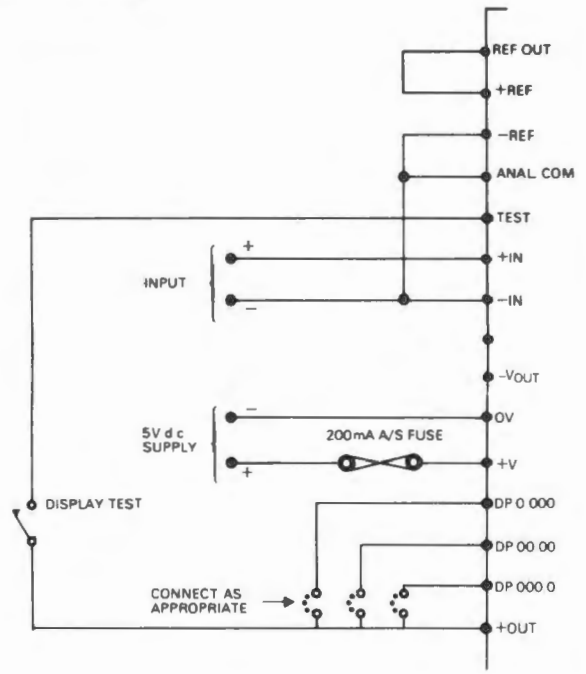
Electrical characteristics

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	+V	4.75	5	5.25	V d.c.
Supply current			8	10	mA
Output analogue common (See Note 1)			+V −2.8		V d.c.
Measurement range	V_{IN}	−199.9		+199.9	mV d.c.
Temp. Coeff.			±75	±150	ppm/°C
Input impedance		100			MΩ
Input over-voltage		−100		+100	V
Common mode rejection ratio	CMRR		80		dB
Common mode voltage range	CMVR	− OUT+1		+ OUT−0.5	V
Voltage OUT	+ OUT to − OUT		9		V
Integration time			100		ms
Sampling rate			3		per second
External ref. range		− OUT+1		+ OUT−0.5	V
Warm-up time				10	minutes
Storage temperature		−20		+60	°C
Operating temperature		0		+50	°C

Note 1: Maximum current 5 mA.

RS data

Connections



Note:
Input + or − may be connected to either 0V or +V supply pins and therefore ground references are possible with no adverse effects.

Reference

The meter incorporates a highly stable band-gap derived reference which may be adjusted by means of the ten turn potentiometer (trimmer) accessed through the hole in the display circuit board behind the filter. The meter may be used with either the internal reference or an external reference. Should the internal reference be used then the standard connections are shown above.

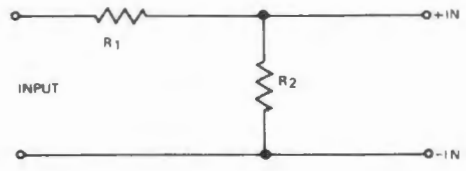
Calibration

To calibrate the meter, connect the meter as per the standard connection and adjust the reference to 100 mV. The reference voltage is measured between the + ref and − ref terminals. Alternatively apply a known voltage to the input (e.g. 199.5 mV) and adjust the reference to give the correct reading.

Attenuators

For applications requiring an f.s.d. greater than the meter's basic movement then the use of an external attenuator may be made.

The total value of R_1 and R_2 determines the load on an external circuit connected to the input and should be chosen to reduce this loading to an acceptable level.

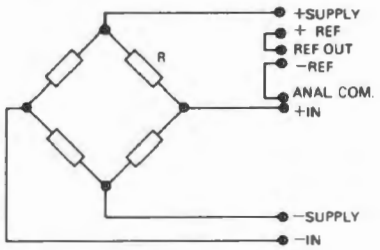


$$\text{attenuation ratio} = \frac{R_2}{R_1 + R_2}$$

Applications

Bridge circuits

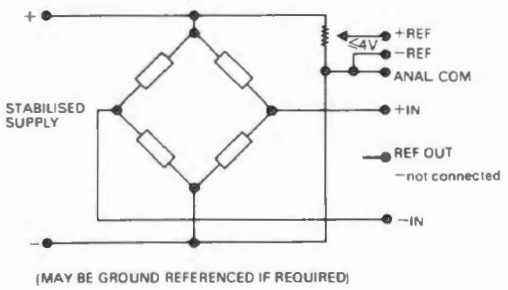
Simple bridge (for non-ratiometric measurements)



The supply to the bridge may be an externally stabilised voltage. Alternatively the analogue common pin may be used to derive this voltage. In this case +V is connected to +Supply and Anal. com. to −Supply with the following limitations.

$$I_R = \frac{2.8\,V}{R} \leq 5\,mA$$

Ratiometric bridge



N.B. To avoid common mode errors in all the above circuits, ensure that the voltage between −IN and Anal. com. (common mode voltage) does not exceed ±1 V.

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Telephone: 0536 201234
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RS data

12 Bit A to D Converter I.C.

Stock number 303–725

The RS574 is a complete 12-bit successive approximation analogue to digital converter with 3-state output buffer circuitry for direct interface to an 8, 12 or 16-bit microprocessor bus. The design is implemented using two LSI chips each containing both analogue and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost.

One chip contains the high speed current output switching circuitry, laser-trimmed thin film resistor network, low temperature coefficient buried zener reference and the precision input scaling and bipolar offset resistors. This chip is laser-trimmed at the wafer stage to adjust ladder network linearity, voltage reference tolerance, temperature coefficient and the calibration accuracy of input scaling and bipolar offset resistors.

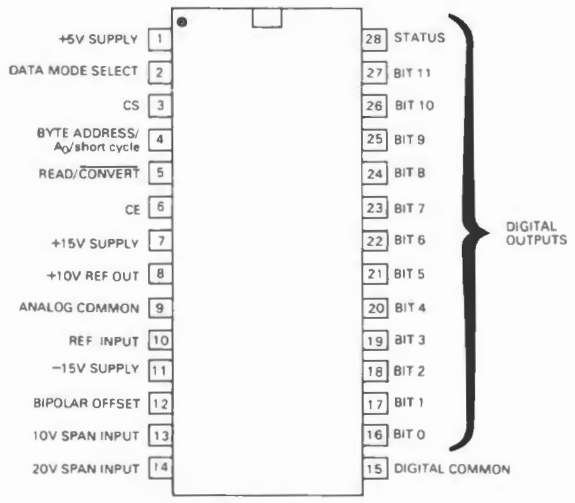
The second chip uses an LCI (linear-compatible integrated injection logic) process to provide the low power I^2L successive-approximation register, converter control circuitry, clock, bus interface and the high performance latching comparator. The precision, low-drift comparator is adjusted for initial input offset error at the wafer stage by the 'Zener Zap' technique which trims the comparator input stage to 1/10 LSB typical error.

Features

- Complete 12-bit analogue to digital converter
- Internal buried zener reference and clock
- Full 8, 12 or 16-bit microprocessor bus interface
- Fast successive approximation conversion – 25 μS
- Long-term stability of reference with low temperature coefficient
- Low power consumption
- Multiple-mode three-state output buffers connect directly to the data bus

Absolute maximum ratings

V_{CC} to Digital common	0 to 16.5 V
V_{DD} to Digital common	0 to −16.5 V
V_{LOGIC} to Digital common	0 to 7 V
Analogue common to Digital common differential	1 V
Control inputs (pins 2, 3, 4, 5, 6) to Digital common	−0.5 to V_{LOGIC} +0.5 V
Analogue inputs (pins 10, 12, 13) to Analogue common	±16.5 V
20 V span input to Analogue common	±24 V
Reference output	Indefinite short to common Momentary short to V_{CC}
Chip temperature	100 °C
Power dissipation	1 W
Lead temperature soldering 10 s	300 °C
Storage temperature	−65° to +150 °C
Thermal resistance	60 °C/W
Operating temperature	0 to +70 °C



CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Electrical Characteristics $T_A = 25°C$, $V_{CC} = 15V$, $V_{DD} = -15V$, $V_{LOGIC} = 5V$

Parameter	Conditions	Min.	Typ.	Max.	Units
Resolution				12	bits
Non linearity error	0 to 70°C	−1		1	LSB
Differential linearity error (minimum resolution with no missing codes)	0 to 70°C	11			bits
Unipolar offset	(Adjustable to Zero)	−2		2	LSB
Bipolar offset	(Adjustable to Zero)	−10		10	LSB
Full scale calibration error	50Ω REF OUT to REF IN				
— adjustable to zero				0.3	%FS
— without initial adjustment	0 to 70°C			0 5	%FS
— with initial adjustment	0 to 70°C			0.22	%FS
Temperature coefficient	0 to 70°C				
— unipolar offset output		−2		2	LSB
— bipolar offset output		−2		2	LSB
— full scale calibration		−9		9	LSB
Power supply rejection	$13.5 \leqslant V_{CC} \leqslant 16.5V$	−2		2	LSB
	$4.5 \leqslant V_{LOGIC} \leqslant 5.5V$	−½		½	LSB
	$-16.5 \leqslant V_{DD} \leqslant -13.5V$	−2		2	LSB
Analogue input range	Bipolar 10V span	−5		+5	V
	Bipolar 20V span	−10		10	V
	Unipolar 10V span	0		10	V
	Unipolar 20V span	0		20	V
Input impedance	10V span	3	5	7	KΩ
	20V span	6	10	14	KΩ
V_{LOGIC}		4.5	5	5.5	V
V_{CC}		13.5	15	16	V
V_{DD}		−13.5	−15	−16	V
I_{LOGIC}			30	40	mA
I_{CC}			2	5	mA
I_{DD}			18	30	mA
Power dissipation			450	725	mW
Internal V_{REF}		9.9	10.0	10.1	V
Output current V_{REF}	(external load should not change during conversion)			1.5	mA

Introductory explanation of converter characteristics

Nonlinearity error
This refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs ½ LSB before the first code transition (all zero's to only the LSB ON). Full scale is defined as a level 1½ LSB beyond the last code transition to all (ones). The deviation of a code from the true straight line is measured from the middle of each particular code. The RS574 is guaranteed to ±1 LSB maximum error over a 0°C to +70°C temperature range.

Differential linearity error
This is the error introduced by the digital output coding not progressing in the ideal sequential manner with a change in analogue input voltage. The RS574 is guaranteed to have no missing codes to 11-bit resolution over the operating temperature range. This means that all of the upper 11bits must be present and in practice very few of the 12-bit codes are missing.

Unipolar offset
The first transition should occur at a level ½ LSB above analogue common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed later. The unipolar offset temperature coefficient specifies the maximum change of the transition point over the temperature range, with or without external adjustment.

Bipolar offset
In a similar manner to that used in the unipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analogue value ½ LSB below analogue common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over the temperature range.

Full scale calibration error
The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analogue value 1½ LSB below the nominal full scale (i.e. 9.9963V for 10.0V full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error can be trimmed out as shown in Fig. 3. The full scale calibration error over temperature is shown in the electrical characteristics with and without the initial error trimmed out. The temperature coefficients indicate the maximum change in the full scale gain from the initial value using the internal 10V reference.

Power supply rejection
The RS574 uses a +5V and ± 15V supplies. The only effect of power supply error on performance of the device will be a small change in the full scale calibration. This will result in a linear change in all low order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

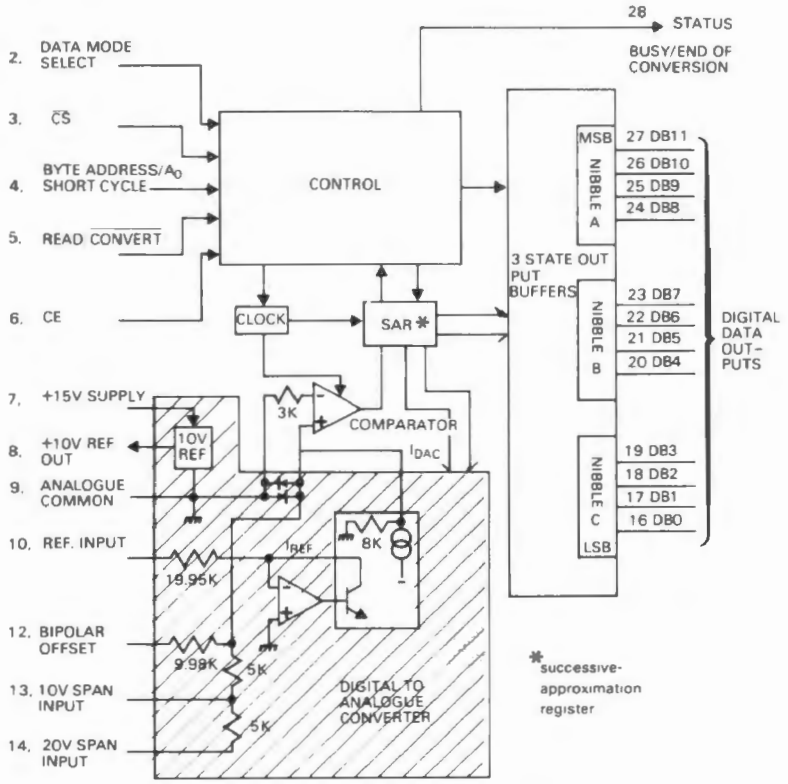
Code width
This is a fundamental quantity for analogue to digital converter specifications and is defined as the range of analogue input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit of the full scale range 2.44mV of 10V for this 12-bit device.

Table 1 **Digital specifications**

Logic Input Characteristics	Conditions	Min	Typ	Max	Units
except mode select which must be hardwired to either V_{LOGIC} or Digital common					
Logic 0				0.8	V
Logic 1		2.0			V
Input current logic 0	t_{MIN} to t_{MAX}			±50	μA
Input current logic 1	t_{MIN} to t_{MAX}			±50	μA
Logic outputs					
Bit outputs and status	output sink V_O = 0.4V	1.6			mA
Bit outputs and status	output source V_O = 2.4V	0.5			mA
Output leakage high impedance state				±40	μA
Conversion time		15	25	25	μS
Minimum pulse widths					
At CE		300			nS
At $\overline{CS}$		500			nS
At R/$\overline{C}$		400			nS

Circuit operation
As can be seen from Fig. 1 the RS574 is a complete 12-bit analogue converter which requires no external components to provide a complete successive approximation conversion function.
When the control section is commanded to initiate a conversion (see further on) it then enables the clock and resets the successive-approximation register to all zeros. (Once a conversion cycle has been started it cannot be stopped or re-started and data is not available from the output buffers.) The successive-approximation register, timed by the clock, will then sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.
During the conversion cycle, the internal 12-bit current output digital to analogue converter is sequenced by the successive approximation register from the most significant bit to the least significant bit to provide an output current which accurately balances the input signal current through the 5kΩ or 10kΩ input resistor. The comparator

Figure 1 **RS574 block diagram**



determines whether the addition of each successively-weighted bit current causes the digital to analogue converter current sum to be greater or less than the input current. If the sum is less, the bit is left on, if more, the bit is turned off. After testing all the bits the successive-approximation register contains a 12-bit binary code which accurately represents the input signal.
The temperature compensated buried zener reference provides the primary voltage reference for the converter and guarantees excellent stability with both time and temperature. The reference is trimmed to 10 V ±1%, it is buffered and can supply up to 1.5 mA to an external load in addition to the internal requirements. The thin film application resistors are trimmed to match the full scale output current of the digital to analogue converter. There are two 5kΩ input scaling resistors to allow either 10V or 20V input span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10V reference for bipolar.

Table 2 **Timing specifications – full control mode**

t_{DSC}	300 ns max
t_{HEC}	300 ns min
t_{SSC}	300 ns min
t_{HSC}	200 ns min
t_{SRC}	200 ns min
t_{HRC}	200 ns min
t_{SAC}	0 min
t_{HAC}	300 ns min
t_C(12-bit convert)	15–35 μs
t_C(8-bit convert)	10–20 μs
t_{DD}	400 ns max
t_{HD}	100 ns min
t_{SSR}	350 ns min
t_{SRR}	0 min
t_{SAR}	200 ns min
t_{HSR}	100 ns min
t_{HRR}	0 min
t_{HAR}	100 ns min
t_{HL}	600 ns max

Control functions
There are two sets of control pins on the 574, the general control inputs (CE, $\overline{CS}$, and READ/$\overline{CONVERT}$) and the internal register control inputs (DATA MODE SELECT and Ao). The general control pins function similarly to those on most analogue to digital converters, performing device timing, addressing, cycle initiation and read enable functions. The internal register control inputs, which are not found on most analogue to digital converters, select output data format and conversion cycle length.

The two major control functions, convert start and read enable, are controlled by CE, $\overline{CS}$, READ/$\overline{CONVERT}$. Although all three inputs must be in the correct state (for convert start, CE = 1, $\overline{CS}$ = 0, READ/$\overline{CONVERT}$ = 0 and for read enable, CE = 1, $\overline{CS}$ = 0, READ/$\overline{CONVERT}$ = 1) to perform the function, the sequence does not matter. For typical microprocessor controlled applications the procedure for a conversion start would be to first set

READ/$\overline{\text{CONVERT}}$ = 0 (from the R/W line), address the chip with $\overline{\text{CS}}$ = 0, then apply a positive start pulse to CE. A read would be performed similarly but with READ/$\overline{\text{CONVERT}}$ = 1.

A much simpler stand alone operation can be implemented with, CE wired high, $\overline{\text{CS}}$ wired low, and READ/$\overline{\text{CONVERT}}$ toggled as needed to initiate a conversion, the data will automatically appear at the end of the conversion.

Alternatively, the READ/$\overline{\text{CONVERT}}$ input can be brought low to start conversion, then brought high at any time later, (after completion of conversation) to enable the data output lines. Many combinations of the above can be implemented by proper manipulation of the three control lines. See Figs. 4 and 5 for control line timing.

The Ao (byte select) and DATA MODE SELECT inputs work together to control the output data and conversion cycle. In almost all situations mode select is hard-wired high or low to +5 or digital common. If it is wired high, all 12 data lines will be enabled when the read function is called by the general control inputs. For an 8-bit bus interface DATA MODE SELECT will be wired low. In this mode only the 8 upper bits or the 4 lower bits can be enabled at once, as addressed by Ao. For these applications the 4 LSB's (pins 16–19) should be hard wired to the 4 MSB's (pins 24–27). Thus during a read, when Ao is low the upper 8 bits are enabled and present data on pins 20 through 27. When Ao goes high, the upper 8 data bits are disabled, the 4 LSB's then present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 and 23.

The Ao input performs an additional function of controlling conversion length. If Ao is held low prior to cycle initiation, a full 12-bit cycle in about 25 μs will result, if Ao is held high prior to cycle initiation a shortened 8-bit cycle in about 16 μs will result. The Ao line must be set prior to cycle initiation and held in the desired position at least until status goes high. Thus, for microprocessor interface applications, the Ao line must be properly controlled during both the CONVERSION START and READ functions. The status line goes high at the initiation of the conversion cycle and will go low when the cycle is complete.

Applications

Unipolar range operation

The 574 contains all the active components required to perform a complete 12-bit analogue to digital conversion. Thus for most situations all that is necessary is connection of the power supplies (+5, +15 and −15V), the analogue input and conversion initiation command as described later. The unipolar operation connections are shown in figure 2. The thin film resistor network is trimmed for absolute calibration so in many applications no calibration trimming is required. If the offset trim is not required, pin 12 can be directly connected to pin 9, the two resistors and trimmer for pin 12 are then not required. If the full scale trim is not needed, a 50Ω ±1% resistor should be connected between pins 8 and 10.

The analogue input is connected between pins 13 and 9 for a 0 to +10V input range or between pins 14 and 9 for a 0 to +20V input range. For the 10V span input the LSB has a nominal value of 2.44mV and 4.88mV for the 20V span input. If a 10.24V range is desired (nominally 2.5mV/bit) the gain trimmer R2 should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analogue input to pin 13. For a full scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14. The gain trim would now be performed with these trimmers.

Unipolar calibration

The 574 is intended to have a nominal ½ LSB offset so that the exact analogue input for a given code will be in the middle of the code. (Halfway between the transitions to the codes above and below it.) So when properly calibrated the first transition from 0000 0000 0000 to 0000 0000 0001), will occur for an input level of +½ LSB (1.22mV for 10V range). If pins 12 and 9 are connected together the unit will typically behave in this manner as per the specification. If the offset trim R1 is used it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±15mV of offset trim range. The full scale trim is performed by applying a signal 1½ LSB below the nominal full scale (9.9963V for 10V range) and adjusting R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

Figure 2 **Unipolar input connections**

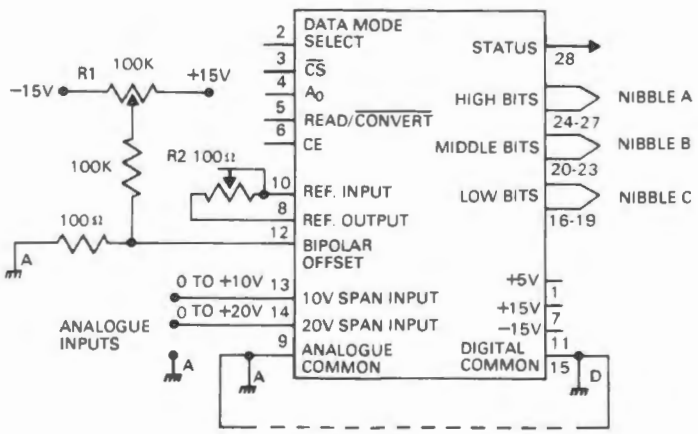
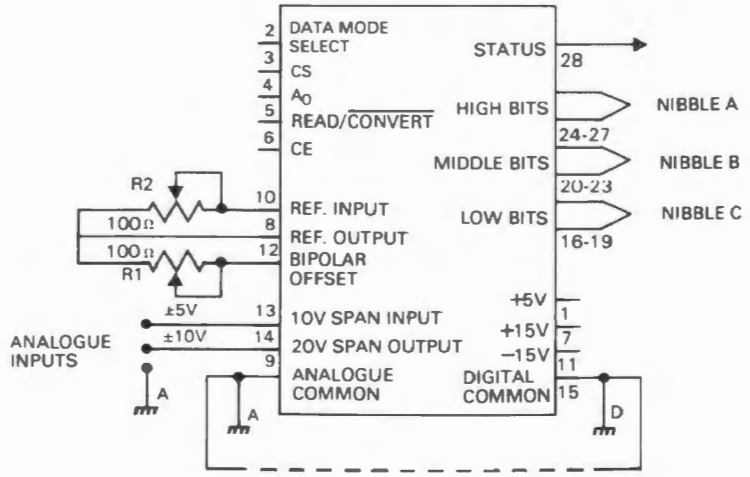


Figure 3 **Bipolar input connections**



Bipolar operation

The bipolar connections are shown in Fig. 3. As for the unipolar ranges if the offset and gain specifications quoted are sufficient, one or both of the trimmers shown can be replaced by a 50Ω ±1% fixed resistor. The analogue input is applied as for the Unipolar ranges.

Bipolar calibration is similar to Unipolar calibration, first a signal ½ LSB above negative full scale (−4.9988 V for the ±5 V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1½ LSB below positive full scale (+4.9963 V for the ±5 V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

Grounding considerations

The analogue common at pin 9 is the ground reference point for the internal reference and should be a 'high quality' ground. It should be connected directly to the analogue reference point of the system. In order to achieve all of the high accuracy performance available from the 574 in an environment of high digital noise content it is recommended that the analogue and digital commons be connected together at the package. In some situations the digital common at pin 15 can be connected to the most convenient ground reference point, analogue power return being preferred. If the digital common contains high frequency noise beyond 200 mV, this noise may feed through the converter so some caution should be observed.

Full control interface

The 574 has a versatile set of control functions which allows interface to a wide variety of microprocessors as well as much simpler data acquisition systems including stand-alone operation.

It is impossible to cover all of the potential control interface situations but discussion of two possible extreme situations and their timing will allow extension of the control concepts to most other applications.

Standard full control interface

The timing for this interface can be seen in Fig. 4. In this operating mode $\overline{CS}$ is used as the address input which will select the particular device. READ/$\overline{CONVERT}$ selects between the read data and start conversion functions and CE is used to time the actual functions.

The left side of Fig. 4 shows the conversion start control. $\overline{CS}$ and READ/$\overline{CONVERT}$ are brought low (their sequence does not matter) then the start pulse is applied to CE. The timing diagram shows a time delay for $\overline{CS}$ and READ/$\overline{CONVERT}$ prior to the start pulse at CE. If less time than this is allowed, the conversion will still be started, but an appropriately longer pulse will be needed at CE. However, if the hold times for $\overline{CS}$ and READ/$\overline{CONVERT}$ after the rising edge of the start pulse at CE are not followed, the conversion may not be initiated.

The Ao line determines the conversion cycle length and must be selected prior to conversion initiation. If Ao is low, a 12-bit cycle results, if Ao is high an 8-bit short cycle occurs.

Minimum set-up and hold times are shown. The status line goes high to indicate conversion in progress. The analogue input signal is allowed to vary until the status output goes high. It must then be held steady until the status output returns to a low at the end of conversion.

Figure 4 **System timing, full control applications**

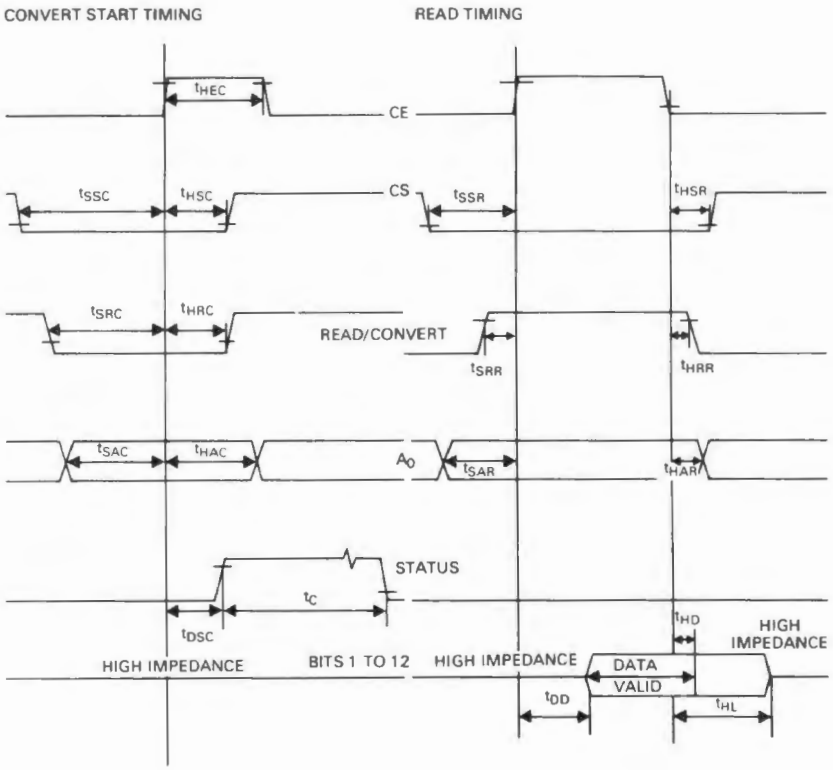
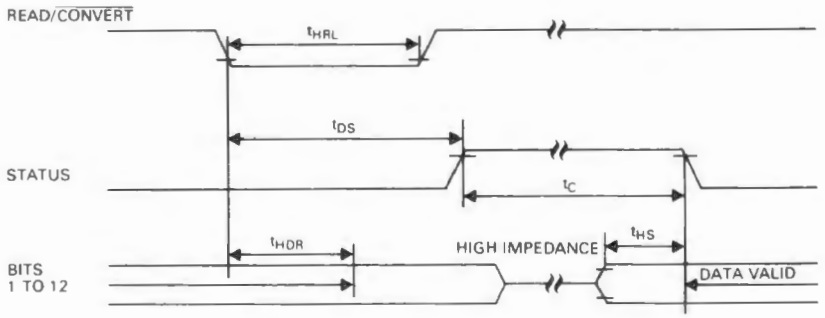
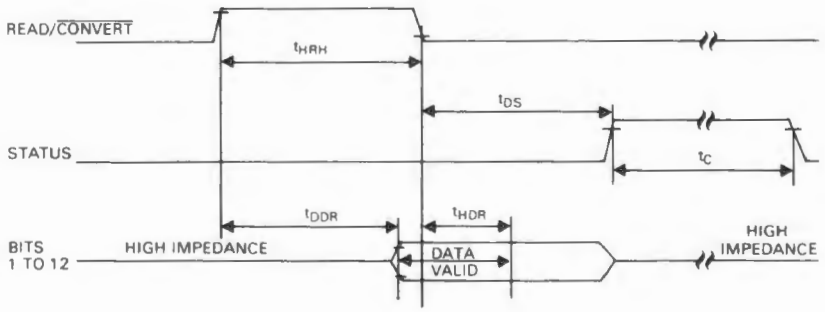


Figure 5 **Timing for stand alone operation**

*) SHORT LOW READ $\overline{\text{CONVERT}}$ PULSE (OUTPUTS COME ON AFTER CONVERSION)



. SHORT HIGH READ $\overline{\text{CONVERT}}$ PULSE (OUTPUTS SYNCHRONISED TO RISING EDGE)



RS data

The DATA READ function operates in a similar fashion except that READ/$\overline{\text{CONVERT}}$ is now held high. The data is held in the output register and can be recalled at will until a new conversion cycle is commanded. In addition if the converter is in the 8-bit mode the Ao line functions as the byte select address with set-up and hold times as shown in Fig. 4. With Ao low, pins 20 to 27 come out of high impedance state and present data. With Ao high, pins 16 to 19 come out of the high impedance mode and present data, and pins 20 to 23 present active trailing zeros. In the 8-bit mode pins 16 to 19 will be hard wired directly to pins 24 to 27 for direct two byte loading onto an 8-bit bus. There are two delay times for the data lines after CE is brought low, t_{HD} is the delay until data is no longer valid, t_{HL} is the delay until the outputs are fully into the high impedance state.

Stand alone operation

For simpler operation the 574 can be controlled with just the READ/$\overline{\text{CONVERT}}$ input. For this CE is wired high, $\overline{\text{CS}}$ low.

DATA MODE SELECT high and Ao low. There are two ways of cycling the device in this set up as shown in Fig. 5. If a negative pulse is used to initiate conversion the converter will automatically bring the 12 data lines out of the high impedance state at the end of the conversion. The data will remain valid on the output lines until another pulse is applied.

If the conversion is initiated by a high pulse, the data lines are held in a high impedance state at the end of conversion until the READ/CONVERT is brought high. The next conversion cycle is initiated when READ/CONVERT goes low, the data from the previous cycle will remain valid for the time t_{HDR}. An alternative is to toggle READ/CONVERT as needed to initiate a new cycle on read data. Data will appear when READ/CONVERT is brought high and a new cycle is initiated when READ/CONVERT is taken low.

Table 3 **Timing specifications – stand alone mode**

t_{HRL}	400 ns min
t_{DS}	500 ns max
t_{HDR}	300 ns max
t_{HS}	−100 ns min +200 ns max
t_{HRH}	150 ns min
t_{DDR}	350 ns min
t_C	15–35 μs (12-bit convert)
t_C	10–20 μs (8-bit convert)

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RS data

12 bit D to A converter i.c

Stock number 303-731

The RS 7542 is a precision 12-bit CMOS multiplying digital to analogue converter designed for direct interface to microprocessors. The device consists of three 4-bit data registers, a 12-bit DAC register, address decoding logic and a 12-bit CMOS multiplying DAC.

Data is loaded into the registers in three 4-bit nibbles, and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the write cycle of a static RAM. A clear register allows the DAC register to be cleared during power up.

Absolute maximum ratings

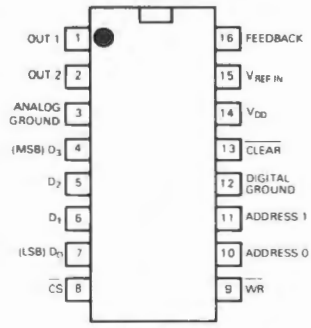
V_{DD} to analogue or digital ground ——— 0V to +7V
Analogue ground to digital ground differential — V_{DD}
Pins 4 to 11 and 13 to digital ground — −0.3 to +15V
Pins 1, 2 to analogue ground ——— −0.3 to +15V
V_{REF} and $V_{Feedback}$ to analogue ground ——— ±25V
Power dissipation (derating by 8.3mW/°C above 70°C) ——— 670mW
Operating temperature range ——— 0°C to +70°C
Storage temperature range ——— −65°C to +150°C
Lead temperature 10s soldering ——— +300°C

Electrical characteristics

V_{DD} = +5V, V_{REF} = +10V
T_A = +25°C, V_{OUT1} = V_{OUT2} = 0V unless otherwise stated

Features

- 12-bits resolution
- ±½ LSB non linearity over operating temperature range
- Low gain drift
- Microprocessor compatible
- Full 4 quadrant multiplication
- Low multiplying feedthrough error
- Low power dissipation
- Latch free operation (protection Shottky diode not required)

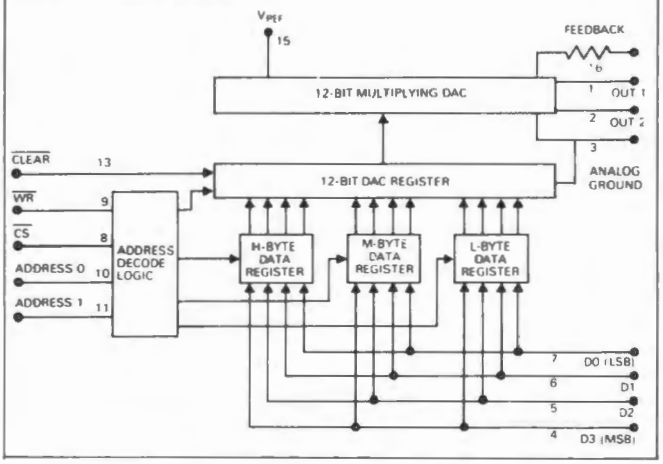


TOP VIEW

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply voltage	V_{DD}	For specified performance	4.75	5	5.25	V
Supply current	I_{DD}	Digital inputs = V_{INH} or V_{INL}			8	mA
Resolution				12		bits
Nonlinearity			−½		+½	LSB
Differential nonlinearity			−1		+1	LSB
Gain error		Using R Feedback	−0.3		+0.3	%FSR
Gain change		+25°C to T_{MIN} or T_{MAX}	−0.03		+0.03	%FSR
D.C. supply rejection		V_{DD} = 4.5 to 5.0V, Δ gain for Δ V_{DD}	−0.005		+0.005	% per %
Output leakage current pin 1 pin 2		Pin 1 DAC register loaded all 0's Pin 2 DAC register loaded all 1's	−50 −50		+50 +50	nA nA
Current settling time		Output 1 to ½ LSB load = 100Ω from ↓ WR			2.0	μS
Multiplying feed-through error		V_{REF} = ±10V			2.5	mV p-p
Pin 15 input resistance			8	15	25	KΩ
O/P capacitance pin 1 pin 2 pin 1 pin 2		{DAC register loaded to all 0's} {DAC register loaded to all 1's}			75 260 260 75	pF pF pF pF
High level input voltage	V_{INH}		+0.3			V
Low level input voltage	V_{INL}				+0.8	V
Input current	I_{IN}				1	μA
Input capacitance					8	pF

Figure 1 **Block diagram**



Switching characteristics

Address valid-to-WRITE setup time (loading 4 bit data registers)	t_{AWS1}	200 ns min.
Address valid-to-WRITE setup time (loading 12 bit DAC register)	t_{AWS2}	120 ns min.
Address-to-WRITE hold time	t_{AWH}	50 ns min.
CHIP SELECT-to-WRITE setup time (loading 4-bit data registers)	t_{CWS1}	180 ns min.
CHIP SELECT-to-WRITE setup time (loading 12-bit DAC register)	t_{CWS2}	60 ns min.
CHIP SELECT-to-WRITE hold time	t_{CWH}	50 ns min.
WRITE pulse width	t_{WR}	120 ns min.
Data setup time (loading 4-bit data registers)	t_{DS}	50 ns min.
Data hold time (loading 4-bit data registers)	t_{DH}	50 ns min.
Minimum CLEAR pulse width	t_{CLR}	200 ns min.

Description of terms used in conjunction with converters

Nonlinearity

This is error contributed by the digital to analogue converter transfer function deviating from a best straight line

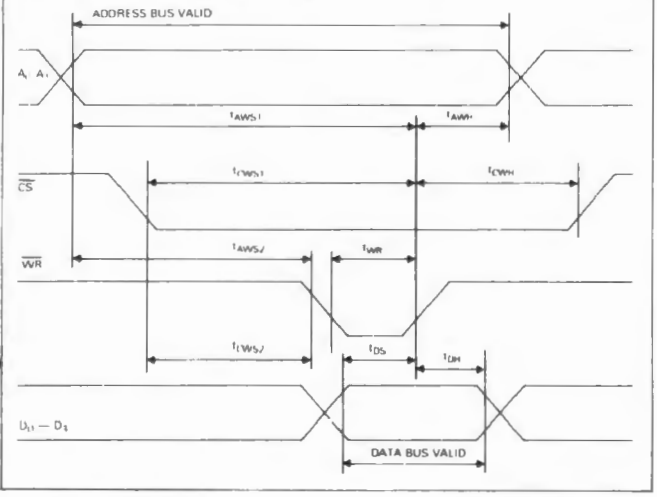
Differential nonlinearity

Differential nonlinearity is the difference between the measured change and ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum over the operating temperature range ensures monotonicity.

Gain error

Gain is defined as the ratio of the digital to analogue converters full scale output to its reference input voltage.

Figure 2 **Write cycle timing**



An ideal 7542 would exhibit a gain of −4095/4096. Gain error is adjustable using external presets as shown in figures 7 and 8.

Output leakage current

This is current which appears at the OUT 1 terminal with the digital to analogue converter register loaded to all 1's.

Multiplying feedthrough error

This is AC error due to capacitive feedthrough from the V_{REF} terminal to the OUT 1 terminal with the digital to analogue register loaded to all 0's.

Table 1 **7542 truth table**

RS7542 Control Inputs					7542 Operation	
A_1	A_0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$		
X	X	X	X	0	Resets DAC 12-bit register to code 0000 0000 0000	
X	X	1	1	1	No operation device not selected	
0	0	↓	0	1	Load low byte data register on edges as shown below	Load applicable data register with data at D_0 - D_3
0	0	0	↓	1		
0	1	↓	0	1	Load middle byte data register on edges as shown below	
0	1	0	↓	1		
1	0	↓	0	1	Load high byte data register on edges as shown below	
1	0	0	↓	1		
1	1	0	0	1	Load 12-bit DAC register with data in low byte, middle byte and high byte data registers	
1	1	0	0	1		

Notes to table 1

MSB → XXXX (high byte) XXXX (middle byte) XXXX (low byte) ← LSB

Although positive-going edges of either $\overline{CS}$ or $\overline{WR}$ will load the data register, timing is optimised by using $\overline{WR}$ to latch the data and using $\overline{CS}$ as a device enable.

General introduction

The RS 7542 is designed to interface as a memory-mapped output device, with the $\overline{CS}$ pin enabled by the decoded device address being derived from decoding the higher order address bits. A_0 and A_1 are the operation address bits for the 7542 and are decoded internally to point to the desired loading operation (i.e. load high byte, middle byte, low byte or DAC register). Table 1 shows the truth table for the 7542. All data loading operations are identical to the write cycle of a static RAM.

An additional feature is the CLEAR input which allows the DAC register to be cleared asynchronously to 0000 0000 0000. When the device is operated in a Unipolar mode, see Figure 7, a CLEAR causes the DAC output to assume 0V. In the bipolar mode, see Figure 8, a CLEAR causes the DAC output to go to $-V_{REF}$.

Summary

A) The 7542 DAC register can be asynchronously cleared with the $\overline{CLEAR}$ input.
B) Each 7542 requires 4 locations in memory.
C) Performing any of the four basic loading operations (load low byte data register, middle byte data register, high byte data register or 12-bit DAC register) is accomplished by executing a memory WRITE operation to the applicable address location for the required DAC operation.

The 7542 converter uses a 12-bit multiplying D/A conversion technique with a highly stable thin film R/2R ladder and twelve N-channel current switches on a monolithic chip. The only additions required for most applications are, a voltage reference and an output operational amplifier.

The simplified digital to analogue circuit is shown in Figure 3. An inverted R/2R ladder structure is used where the binary weighted currents are switched between the OUT 1 and OUT 2 bus lines, maintaining a constant current in each ladder leg independent of the switch state. See Figure 4 for the type of current switches used. The input resistance at V_{REF} is always equal to R_{LDR} (where R_{LDR} is the R/2R ladder characteristic resistance and is equal to the value R). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or current a.c. or d.c., of positive or negative polarity. If a current source is used, a low temperature coefficient external feedback resistor R_{FB} is recommended to define the scale factor.

Figure 3 **Functional diagram**

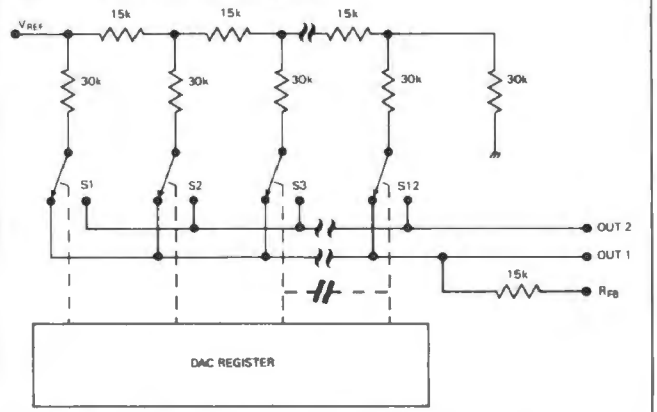
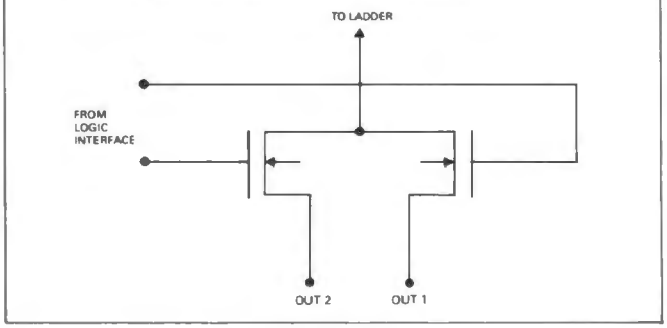


Figure 4 **N-channel current steering switch**



Equivalent circuit analysis

Figures 5 and 6 show equivalent circuits for the digital inputs of the 7542. With all the inputs low the reference current is switched to OUT 2.

The leakage current source I_L is composed of surface and junction leakages to the substrate, while the I/4096 current source represents a constant 1-bit current drain through the termination resistor on the R/2R ladder. The "ON" capacitance of the output N-channel switch is 260pF, as shown on the OUT 2 terminal. The "OFF" switch capacitance is 75pF, as shown on the OUT 1 terminal.

Analysis of the circuit for all digital inputs high is similar to that with all the digital inputs low, however the "ON" switches are now on terminal OUT 1, hence the 260pF at this terminal.

Figure 5 **7542 equivalent circuit all inputs low**

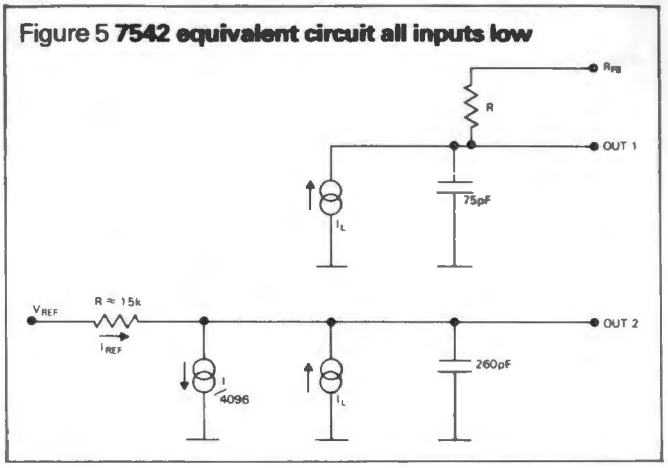
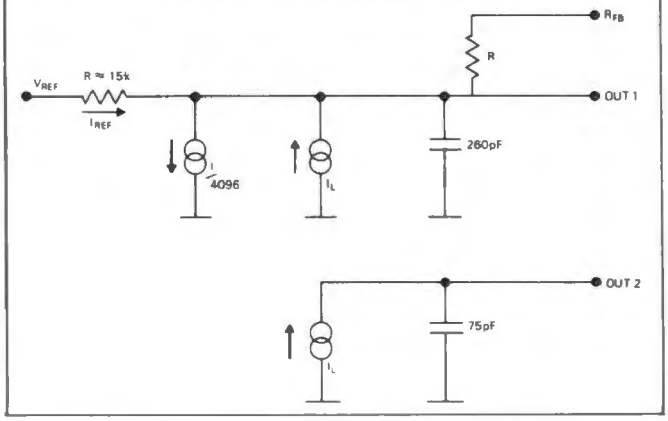


Figure 6 **7542 equivalent circuit all inputs high**



Applications

Unipolar binary operation (2 quadrant multiplication)

Figure 7 shows the analogue circuit connections required for unipolar binary operation. With a d.c. reference voltage or current (positive or negative polarity) applied to pin 15, the circuit is a unipolar digital to analogue converter. With an a.c. reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 2.

R1 provides full scale trim capability (i.e. load the DAC register to 1111 1111 1111, and adjust R_1 for $V_{OUT} = -V_{REF}$ (4095/4096). Alternatively, full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

A phase compensation capacitor between the inverting input and output of the output amplifier may be required for stability when using high speed amplifiers. This capacitor is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT 1. The amplifier should be trimmed to provide an offset voltage $\leq$10% of the voltage resolution at V_{OUT}, additionally the amplifier should exhibit a bias current which is low over the temperature range being encountered.

RS data

Figure 7 **Unipolar binary operation, 2-quadrant multiplication**

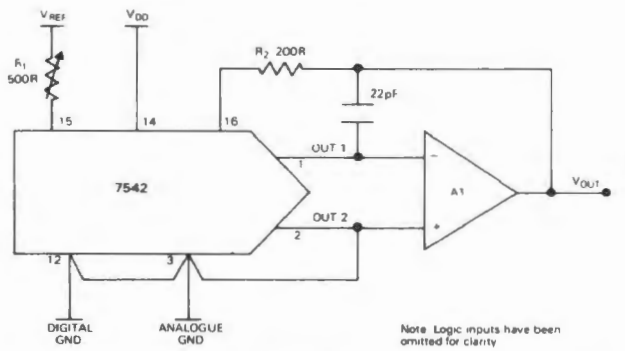


Table 2 **Unipolar binary operation, 2-quadrant multiplication code**

Binary number in DAC register MSB LSB	Analogue output, V_{OUT}		
1111 1111 1111	$-V_{REF}$	$\left(\frac{4095}{4096}\right)$	
1000 0000 0000	$-V_{REF}$	$\left(\frac{2048}{4096}\right)$	$= -\frac{1}{2} V_{REF}$
0000 0000 0001	$-V_{REF}$	$\left(\frac{1}{4096}\right)$	
0000 0000 0000	0V		

Bipolar operation 4 quadrant multiplication

Figure 8 shows the circuitry for bipolar operation with Table 3 giving the code relationship. With a d.c. reference (positive or negative polarity) the circuit provides offset binary operation. With an a.c. reference, the eleven LSB's provide digitally controlled attenuation of the a.c. reference while the MSB provides polarity control. With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ alternatively R_1 and R_2 may be omitted and the ratio of R_3 to R_4 adjusted to give $V_{OUT} = 0V$.

Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R_5.

As in the Unipolar mode of operation, A_1 must be chosen for low offset voltage and bias current. R_3, R_4 and R_5 must be selected for matching and tracking. Mismatch of $2R_3$ to R_4 causes both offset and full scale error. Mismatch of R_5 to R_4 or $2R_3$ causes full scale error. A phase compensation capacitor (10 to 25pF) may be required for stability as shown.

Figure 8 **Bipolar operation 4-quadrant operation**

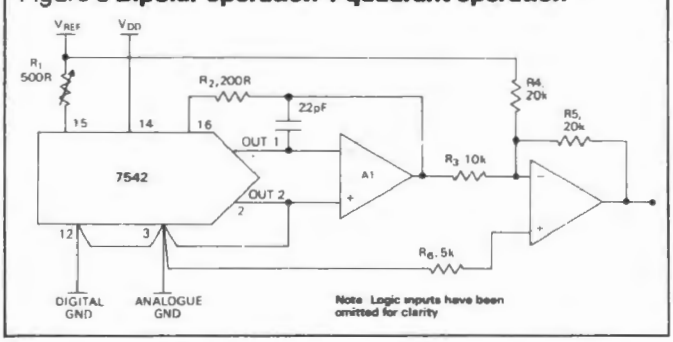
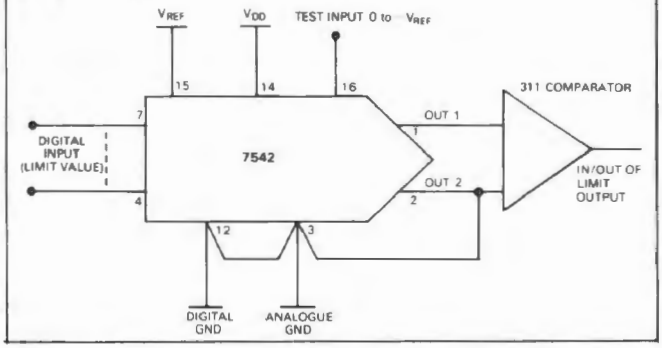


Table 3 **Bipolar operation 4-quadrant multiplication code**

Binary number in DAC register MSB LSB	Analogue output, V_{OUT}	
1111 1111 1111	$+V_{REF}$	$\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}$	$\left(\frac{1}{2048}\right)$
1000 0000 0000	0V	
0111 1111 1111	$-V_{REF}$	$\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}$	$\left(\frac{2048}{2048}\right)$

Figure 9 **Digitally programmable limit detector**
The circuit forms a simple detector whose switching threshold can be set by the digital input. The 311 comparator should be connected to give the required output form.



Operational notes

The 7542 is a precision 12-bit multiplying digital to analogue converter designed for system interface to obtain performance consistent with the specifications. The following points should be observed.

Ground management

Voltage difference between the digital and analogue grounds causes loss of accuracy (a d.c. potential between the grounds introduces gain error. A.C. or transient voltages cause noise injection into the analogue output). The simplest method of reducing ground differential voltages is to tie the analogue and digital ground pins together at the 7542. In more complex systems where the analogue and digital grounds are interconnected on board planes, it is recommended to connect diodes (IN4148 types) back to back between the 7542 analogue and digital ground pins.

Output amplifier offset

CMOS digital to analogue converters exhibit a code-dependant output resistance which in turn causes a code-dependant amplifier noise gain. The effect is a differential nonlinearity at the amplifier output of magnitude $0.67V_{OS}$ (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, the amplifier V_{OS} should be adjusted to less than 10% of the converter's output resolution, i.e. V_{REF} (2^{-n}) where n is the number of bits being used.

High frequency considerations

The 7542 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

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RS data

A to D Converter i.c. 507C

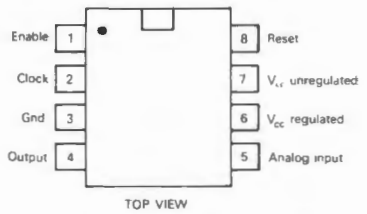
Stock number 304-150

The RS 507C is a single slope analogue to digital converter designed for use in a wide range of applications including interface to microprocessors, where an extremely cost effective solution is required.

Absolute maximum ratings

Supply voltage regulated input	6.5 V
Supply voltage unregulated input	20 V
Analogue input voltage	6.5 V
Enable, clock and reset input voltage	±20 V
On state output voltage	6 V
Off state output voltage	20 V
Continuous dissipation	1000 mW
Operating free air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature (soldering 10s 1.6mm from case)	260°C

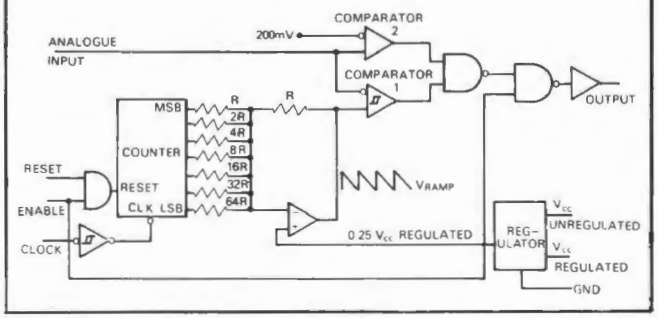
Pin connections



Features

- 7-Bit resolution
- Guaranteed monotonicity
- 1 ms conversion speed
- Ratiometric conversion
- Single supply operation
- Low power consumption

Figure 1 **Block diagram**



Electrical characteristics T_A = 25°C, V_{CC} Regulated = V_{CC} Unregulated = 5V

Parameter	Terminals	Conditions	Min.	Typ.	Max	Units
Supply voltage regulated	6		3.5	5	6	V
Supply voltage unregulated	7		8	15	18	V
Analogue input voltage	5		0		5.5	V
Input voltage	1,2,8				±18	V
On-state output					5.5	V
Off-state output					18	V
Clock frequency				125	150	kHz
Regulator output	6	Unregulated input =12 to 18V 0 to −1 mA output current	5	5.6	6	V
Supply current	6	regulated input = 5V, unregulated o/c.		5	8	mA
Supply current	7	Unregulated input = 15V, regulated o/c.		7	10	mA
High level input	1, 8		2			V
Low level input	1, 8				0.8	V
Positive going threshold	2		2.5	3.5	4.5	V
Negative going threshold	2		0.4	0.9	1.2	V
Hysteresis	2		2	2.6	4	V
Input current high	1, 2, 8	V_{in} = 2.4V		17	35	µA
Input current high	1, 2, 8	V_{in} = 18V	130	220	320	µA
Input current low	1, 2, 8	V_{in} = 0			±10	µA
Input current analogue	5	V_{in} = 4V		10	300	nA
High level output current		V_{out} = 18V		0.1	100	µA
Low level output current		V_{out} = 5.5V	5	10	15	mA
Low level output voltage		I_{out} = 1.6 mA		80	400	mV
Resolution			7			bits
Overall error					±80	mV
Differential nonlinernity					±1	L.S.B
Zero error		Binary count = 0			±80	mV
Scale error		Binary count = 127			±80	mV
Propagation delay		From reset or enable		2		µs

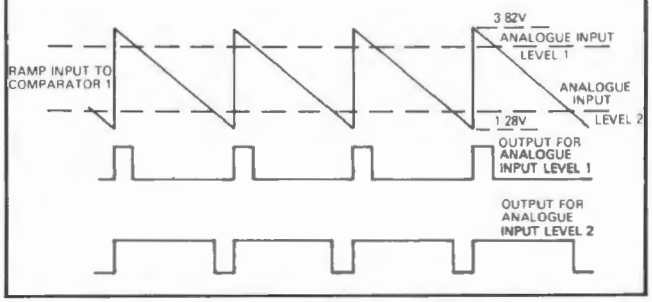
RS data

Table 1 Truth table

Analogue input Condition	Enable	Output
X	L	H
$V_{IN} < 200mV$	H	L
$V_{RAMP} > V_{IN} > 200mV$	H	H
$V_{IN} > V_{RAMP}$	H	L

Notes Low level on enable also inhibits the reset function V_{RAMP} = 25 to 75% of V_{CC} Regulated (internally generated)

Figure 2 **Output signal duty cycle for two different analogue input levels.**



Circuit operation

The RS 507C being a single slope converter provides a voltage-to-time conversion. An external clock signal is applied through a buffer to a negative-edge-triggered synchronous counter. Binary-weighted resistors from the counter are connected to an operational amplifier which is used as an adder. This operational amplifier generates a signal that ramps down from 0.75 Vcc regulated to 0.25 Vcc regulated. Comparator 1 compares this ramp signal to the analogue input signal. Comparator 2 functions as a fault detector and disables the output should the analogue input fall below 200 mV. With the analogue input voltage in the range 0.25V regulated to 0.75V regulated, the duty cycle of the output signal is determined by the unknown analogue input as shown in Figure 2 and Table 1.

The voltage regulator section allows operation from either an unregulated 8 to 18V source or a regulated 3.5 to 6V source. Whichever external power source is used the internal circuitry operates at the regulatd voltage value.

When operating from an external regulated supply the Vcc unregulated pin 7 may be connected to the Vcc regulated pin 6 or left open circuit. When operating from an unregulated supply the Vcc regulated pin 6 can be used as a reference voltage output within the output current constraint.

Figure 3 **Input and output circuits (all values shown are nominal.)**

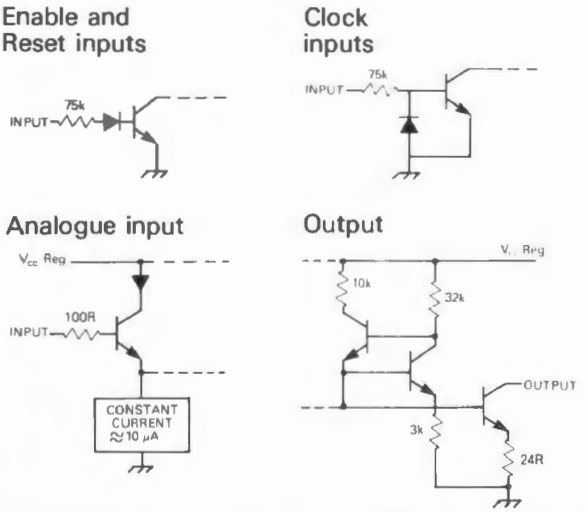
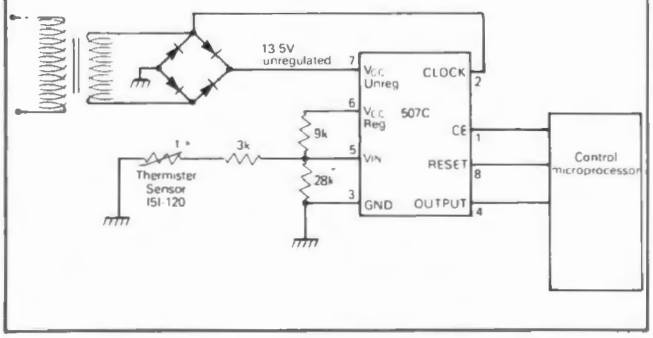


Figure 4 **Typical interface connections to a microprocessor system for temperature monitoring.**



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RS data

Universal counter i.c. 7226A

Stock number 304-138

The RS 7226A universal counter i.c. is a fully integrated 8-digit universal counter with the same features as the RS 7216A. In addition multiplexed BCD outputs and control signals to aid transfer of measured information to other devices are included. Contained in the device is a high frequency oscillator, decade timebase counter, an 8-decade data counter with latches and a 7-segment decoder and digit multiplexer with segment and digit drivers to directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other (period, frequency ratio and time interval) modes. Both inputs have digital input characteristics.

Absolute maximum ratings

Maximum supply voltage (V^+)	6.5V
Maximum digit output current	400mA
Maximum segment output current	−60mA
Voltage on any input or output terminal (1)	V^+ +0.3V to −0.3V
Maximum power dissipation at 70°C	1.0W
Maximum operating temperature range	−20°C to +70°C
Maximum storage temperature range	−55°C to +125°C

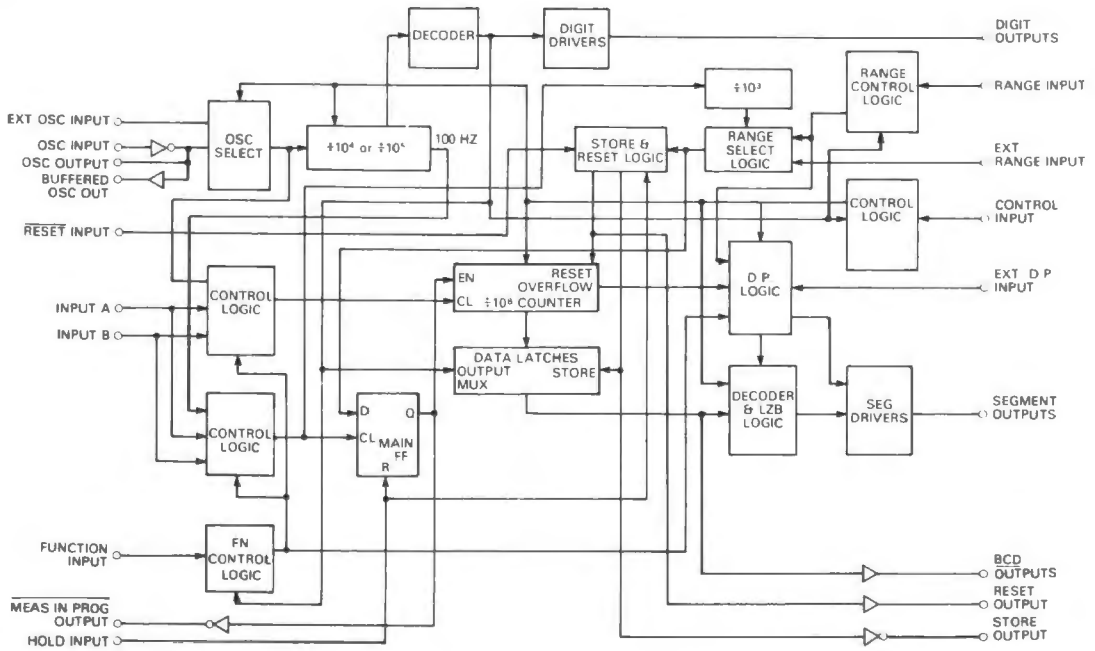
Features

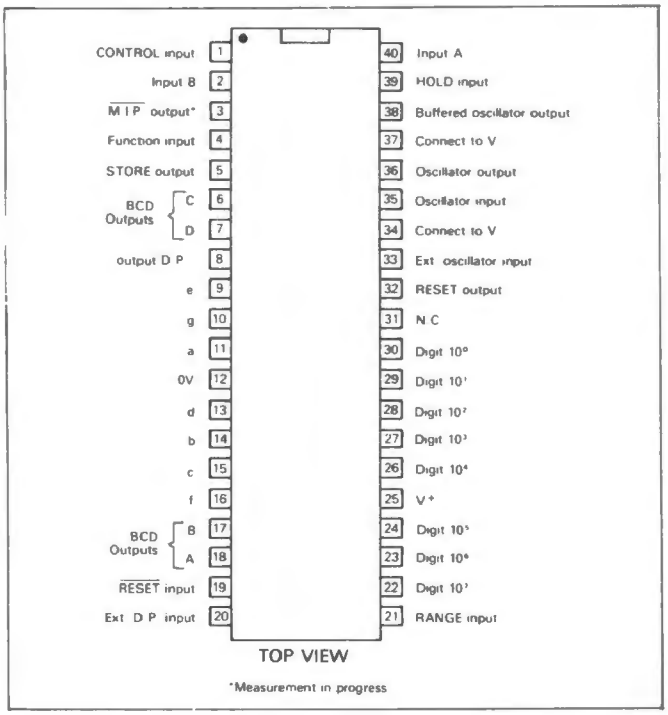
- Four internal gate times: 0.01 sec, 0.1 sec, 1 sec, 10 sec in frequency counter mode
- 1 cycle, 10 cycles, 100 cycles, 1000 cycles in period, frequency ratio and time interval modes
- Measures frequencies from d.c. to 10MHz
- Measures period from 0.5μ sec to 10 sec
- Eight digit multiplexed LED outputs
- Multiplexed BCD outputs
- Control signals to aid data transfer
- Output drivers will directly drive both digits and segments of large LED displays
- Stable high frequency oscillator, uses either 1MHz or 10MHz crystal
- Internally generates multiplex timing with inter-digit blanking, leading zero blanking and overflow indication
- Decimal point and leading zero blanking controlled directly by the chip
- All terminals protected against static discharge

NOTE

1. The RS 7226A may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V^+ by more than 0.3V.

Figure 1 **Block diagram**





General notes

Inputs A & B

Inputs A and B are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centred about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transition at both inputs.

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed inputs

The function, range and control inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The function, range and control inputs must be stable during the last half of each digit output (typically 125μsec). The multiplex inputs are active high for a common anode display.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED's to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs and a 68pF capacitor to decouple the inputs to 0V as shown in Figure 10.

Table 1 shows the functions selected by each digit for these inputs.

Control input functions

Display test – All segments are enabled continuously giving a display of all 8's with decimal points. The display will be blanked if display off is selected at the same time.

Display off – To enable the display off mode it is necessary to connect $D10^3$ to the control input and have the HOLD input at V^+. The chip will remain in the display off mode until HOLD is switched back to 0V. While in the display off mode, the segment and digit driver outputs are open. During display off the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to 0V.

1MHz enable – The 1MHz enable mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as with a 10MHz crystal. The decimal point is also shifted one digit to the right in period and time interval, since the least significant digit will be in μsec increments rather than 0.1μsec increments.

External oscillator enable – In this mode the external oscillator input is used instead of the on-chip oscillator for timebase input and main counter input in period and time interval modes. The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself to enable the on-chip oscillator. (The RS 10MHz crystal oscillator is ideally suited as an external oscillator.)

Table 1

	Function	Digit
FUNCTION INPUT Pin 4	Frequency	$D10^0$
	Period	$D10^7$
	Frequency Ratio	$D10^1$
	Time Interval	$D10^4$
	Unit Counter	$D10^3$
	Oscillator Frequency	$D10^2$
RANGE INPUT Pin 21	.01 sec/1 hertz	$D10^0$
	0.1 sec/10 hertz	$D10^1$
	1 sec/100 hertz	$D10^2$
	10 sec/1k hertz	$D10^3$
CONTROL INPUT Pin 1	Blank Display	$D10^3$ and HOLD
	Display Test	$D10^7$
	1 MHz Enable	$D10^1$
	External Oscillator	$D10^0$
	External D.P. Enable	$D10^2$
EXTERNAL DECIMAL POINT INPUT Pin 20	Decimal Point is output for same digit that is connected to this input.	

Electrical characteristics $T_A = 25°C$, $V^+ = 5.0V$, unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Current	I_{DD}	Display Off, Unused Inputs to 0V		2	5	mA
Supply Voltage Range		$-20°C < T_A < +70°C$. Input A, Input B frequency at F_{MAX}	4.75		6.0	V
Maximum Frequency Input A, Pin 40	$F_{A\ MAX}$	$-20°C < T_A < +70°C$ $4.75 < V^+ < 6.0V$, Figure 2 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	10 2.5			MHz MHz
Maximum Frequency Input B, Pin 2	$F_{B\ MAX}$	$-20°C < T_A < +70°C$ $4.75V < V^+ < 6.0V$ Figure 16	2.5			MHz
Minimum Separation Input A to Input B Time Inteval Function		$-20°C < T_A < 70°C$ $4.75V < V^+ < 6.0V$ Figure 16	250			ns
Maximum Osc. Freq. and Ext. Osc. Frequency		$-20°C < T_A < +70°C$ $4.75 < V^+ < 6.0V$	10			MHz
Minimum Ext. Osc. Freq.					100	KHz
Multiplex Frequency	f_{max}	f_{osc} = 10MHz		500		Hz
Time Between Measurements		f_{osc} = 10MHz		200		ms
Input Voltages: Pins 2, 19, 33, 39 40 Input Low Voltage Input High Voltage	 V_{IL} V_{IH}	$-20°C < T_A < +70°C$	 3.5		1.0	 V V
Input Resistance to V^+ Pins 19, 33	R	$V_{IN} = V^+ - 1.0V$	100	400		kΩ
Input Leakage Pins 2, 39, 40	I_L				2.0	μA
Digit Driver: Pins 22, 23, 24, 26, 27, 28, 29, 30 High Output Current Low Output Current	 I_{OH} I_{OL}	 $V_{OUT} = V^+ - 2.0V$ $V_{OUT} = +1.0V$	 150	 180 −0.3		 mA mA
Segment Driver: Pins 8, 9, 10, 11, 13, 14, 15, 16 Low Output Current High Output Current	 I_{OL} I_{OH}	 $V_{OUT} = +1.5V$ $V_{OUT} = V^+ - 2.5V$	 25	 35 100		 mA μA
Multiplex Inputs: Pins 1, 4, 20, 21 Input Low Voltage Input High Voltage Input Resistance to 0V	 V_{IL} V_{IH} R	 $V_{IN} = +1.0V$	 2.0 50	 100	 0.8	 V V kΩ

Range input – The range input selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter. In all functional modes except unit counter a change in the range input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the range input is changed. (N.B. Readings displayed in kilohertz or microseconds.)

Function input – The six functions that can be selected are:

Frequency, period, time interval, unit counter, frequency ratio and oscillator frequency. These functions select which signal is counted into the main counter and which signal is counted by the reference counter as shown in Table 2. In time interval a flip flop is toggled first by a 1-0 transition of input A then by a 1-0 transition of input B. The oscillator is gated into the main counter from the time input A toggles the flip flop until input B gates the flip flop. (For complete descriptions of workings of time interval see later section Figure 14.) A change in the function input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the function input is changed.

Table 2

Description	Main Counter	Reference Counter
Frequency (F_A)	Input A	100 Hz (Oscillator $\div 10^5$ or 10^4)
Period (T_A)	Oscillator	Input A
Ratio (F_A/F_B)	Input A	Input B
Time Interval (A – B)	Osc (Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (fosc)	Oscillator	100 Hz (Oscillator $\div 10^5$ or 10^4)

Figure 3 **Reset, store and measurement in progress outputs between measurements**

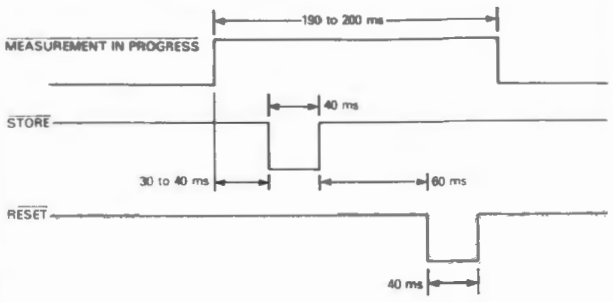
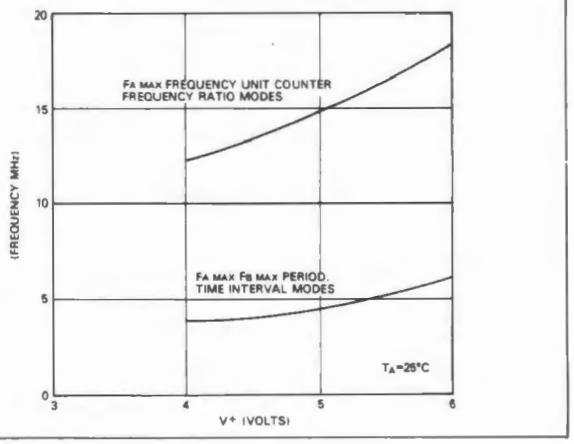


Figure 2 **Typical operating characteristics $F_{A\,MAX}$, $F_{B\,MAX}$ Vs. V^+**



Hold input – Except in the unit counter mode when the hold input is at V^+ any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. In unit counter mode when the hold input is V^+ the counter is stopped but not reset. When HOLD is changed to 0V, a new measurement is initiated.

Reset input – The RESET is the same as the hold input, except the latches for the main counter are enabled, resulting in an output of all zeros.

Measurement in progress, store and reset outputs – These outputs are provided to aid data transfer. Figure 3 shows the relationship between these signals during the time between measurements. All three can drive a low power schottky TTL load. The measurement in progress output can directly drive an ECL load if the two devices are on the same power supply.

BCD outputs – The BCD representation of each digit output is present on the BCD outputs. Each BCD output will drive one low power schottky TTL load. The truth table for the BCD outputs is shown in Table 3.

Table 3 Truth Table BCD Outputs

Number	D Pin 7	C Pin 6	B Pin 17	A Pin 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Buffered oscillator output – The buffered oscillator output has been provided to enable use of the on-chip oscillator signal without loading the oscillator itself. This output will drive one low power schottky TTL load. Care should be taken to minimise capacitive loading on this pin.

Display considerations

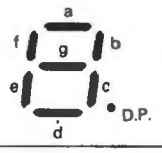
The display is multiplexed at a 500Hz rate with a digit time of 244μsec. An interdigit blanking time of 6μsec is used to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays. Any zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the main counter overflows.

The RS 7226A is designed to drive common anode LED displays at peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average d.c. current will be over 3mA under these conditions. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 4 and 5 show the digit and segment currents as a function of output voltage. (V_{out} referred to 0V.)

To obtain additional brightness from the displays V^+ may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

The segment and digit outputs in the RS 7226A are not directly compatible with either TTL or CMOS logic. Should logic signals be required, the BCD outputs are available.

Segment identification:



N.B. The correct display to use with this device is a common anode with right hand decimal point e.g. RS multiplexed seven segment display stock number 587-024.

Figure 4 **Typical I_{DIG} Vs. $V^+ - V_{OUT}$ (4.5V $<V^+<$ 6.0V)**

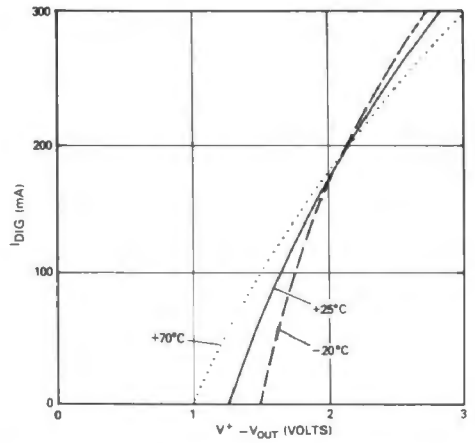


Figure 5 **Typical I_{SEG} Vs. V_{OUT} (V^+ varied)**

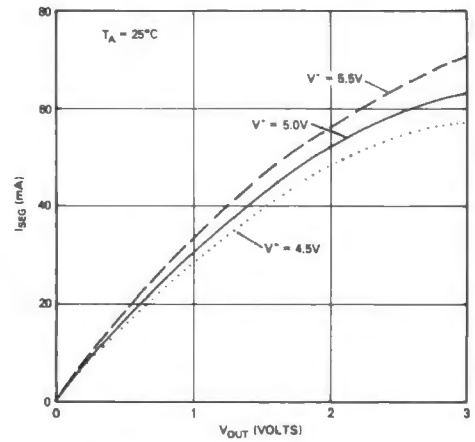
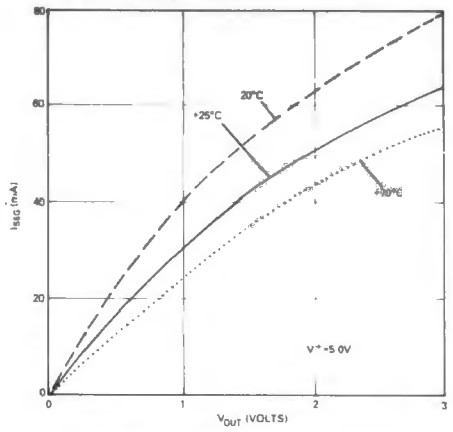


Figure 6 **Typical I_{SEG} Vs. V_{OUT} (temperature varied)**



Accuracy

In a universal counter crystal drift and quantization errors cause errors. In frequency, period and time interval modes, a signal derived from the oscillator is used in either the reference counter or main counter.

Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the frequency mode the maximum accuracy is obtained with high frequency inputs and in period mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 7 the least accuracy will be obtained at 10kHz. In time interval measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 8. A frequency ratio measurement can be more accurately obtained by averaging over more cycles of input B as shown in Figure 9.

Figure 7 **Maximum accuracy of frequency and period measurements due to limitations of quantization errors**

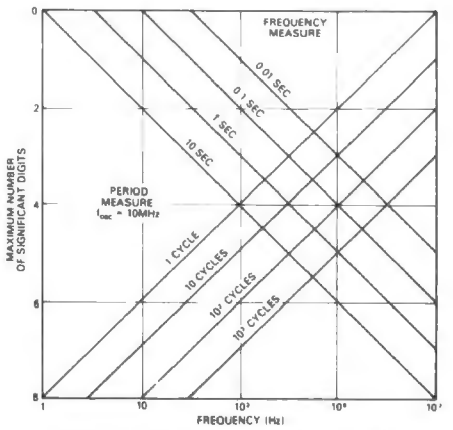


Figure 8 **Maximum accuracy of time interval measurement due to limitations of quantization errors**

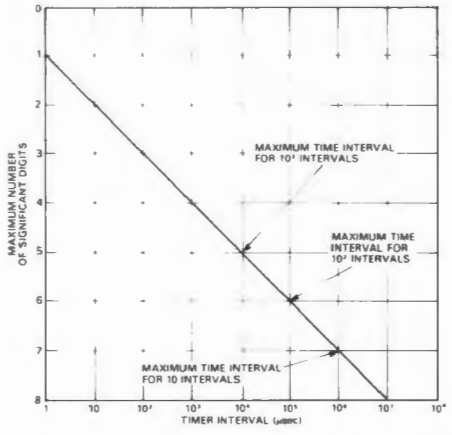
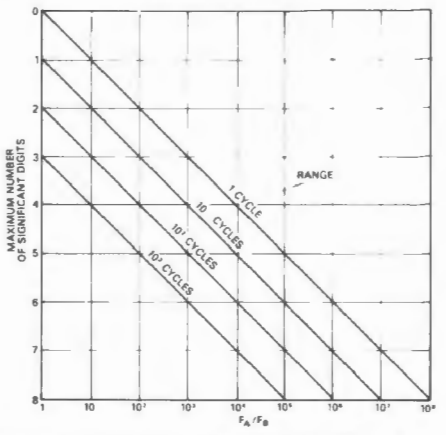
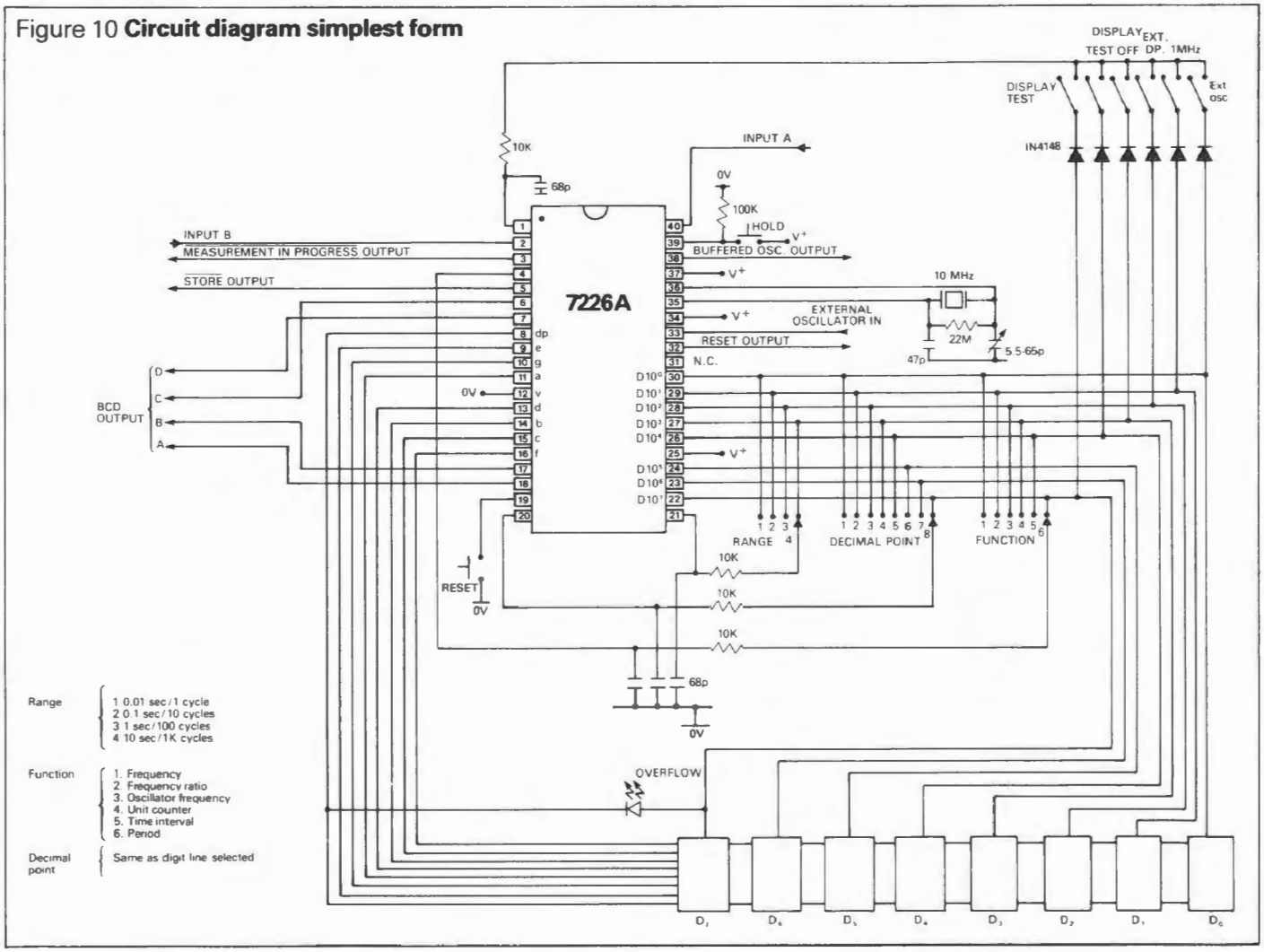


Figure 9 **Maximum accuracy for frequency ratio measurement due to limitation of quantization errors**



Circuit applications

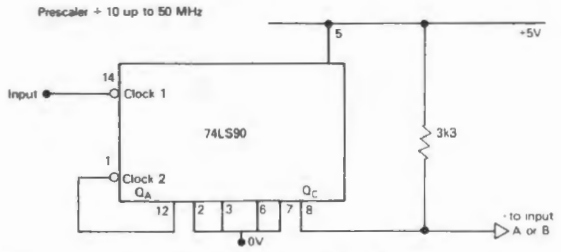
Figure 10 **Circuit diagram simplest form**



The RS 7226A has been designed for use in a wide range of universal counter applications. In many cases, prescalers will be required to reduce the input frequencies to under 10MHz. Because input A and B are digital inputs, additional circuitry will often be required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal. The complexity for doing this can vary widely depending on the sensitivity and maximum frequency required.

Prescaler techniques

Figure 11 **Divide by ten prescaler**



For a full function universal counter two of these prescaler circuits will be required. Note that the input to the 74LS90 must be a digital circuit. If decimal point position correction is required see following section.

Note. The output from the 74LS90 comes from Q_C rather than Q_D to obtain an input duty cycle of 40%. If the signals at inputs A or B have very low duty cycles it may be necessary to use a monostable (74LS123 or similar) to stretch the pulse width to guarantee a 50ns minimum pulse width.

Figure 12 **Divide by 100 high frequency, single-ended input**

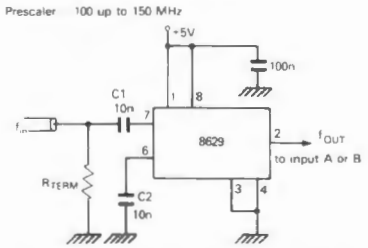
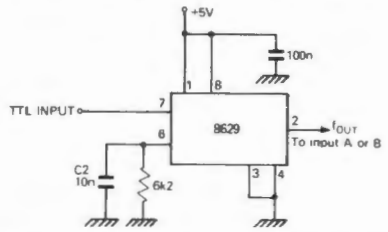


Figure 13 **Divide by 100 TTL input (d.c.<f_{in}<f_{max})**



As with the ÷10 circuit above, two of these +100 prescaler circuits will be required for a full function counter.

For further details of the RS 8629 see data sheet 3059.

External decimal point input

The external decimal point input is active when the control input (pin 1) is connected to the $D10^2$ digit line (pin 28). The decimal point input is then used to select the required decimal point position by connecting the digit strobe line for the required position to this input. The $D10^7$ (pin 22) should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point. This feature is extremely useful when prescalers are used and a different decimal point position is required.

Time interval mode

The principal of operation of the time interval measurement is that the counter is started by channel A going negative and after the selected number of periods is stopped by channel B going negative. However the first pair of negative edges steers the circuit into this mode of operation and therefore when single shot measurements are to be made it is necessary to "prime" the circuit by a negative going A input followed by a negative going B input (separated by at least 250ns and complying with the specified input characteristics as shown in Figure 16).

This priming procedure may be accomplished using the circuit shown in Figure 14, but note that it may be necessary to reset the counter before priming. After "priming", the circuit will count the selected number of periods and display the result as an "average". This priming circuit has no effect on the operation of the universal counter in other modes and may therefore be left permanently connected. (N.B. "Priming" is not necessary if a repetitive measurement is to be made.) Accurate resolution for time interval measurement is 100ns with a maximum time between the two events of ten seconds.

For operation in the time interval mode, range 1 (0.01 sec/1 cycle) must be selected.

RS data

Figure 14 **Priming circuit for single shot operation time interval mode**

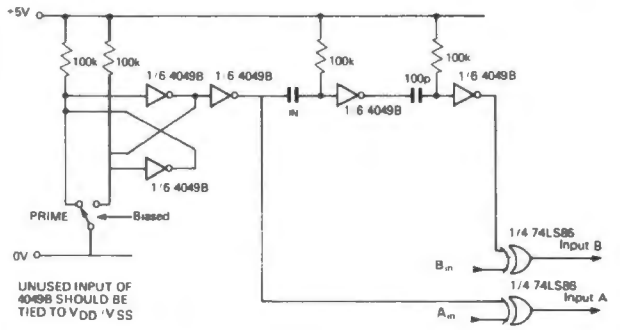


Figure 15 **Waveform for guaranteed minimum $F_{A\,MAX}$ function = frequency, frequency ratio, unit counter**

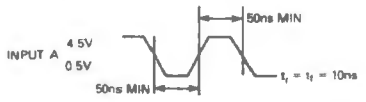
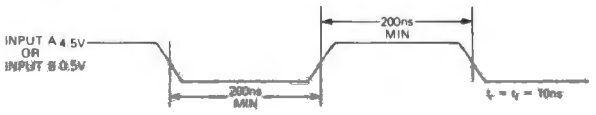


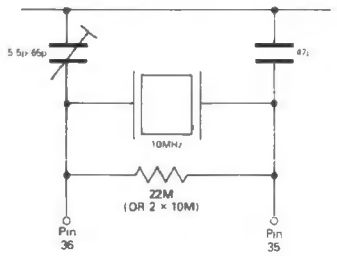
Figure 16 **Waveform for guaranteed minimum $F_{B\,MAX}$ and $F_{A\,MAX}$ for function = period and time interval**



Oscillator considerations

The easiest way of implementing the timebase oscillator is to use a 10MHz crystal (307-799) and associated circuitry as shown in Figure 17.

Figure 17 **Crystal oscillator circuit**



If the 1MHz enable option is to be used, this may be implemented simply by substituting a 1MHz crystal for the 10MHz crystal in Figure 17 and connecting the 1MHz enable control circuitry.

An external oscillator, e.g. the RS 10MHz crystal oscillator may be used by connecting the oscillator output to pin 24 and connecting the external oscillator enable control circuitry. (N.B. oscillator output must meet input voltage criteria as detailed in maximum ratings and electrical characteristics sections.)

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RS data

Digitally controlled audio attenuator i.c.

Stock number 303-747

The RS 7110 is a C-MOS digitally controlled audio attenuator i.c.

The addition of one external operational amplifier enables an audio signal to be attenuated in 1.5 dB steps over the range 0 to 88.5 dB via a 6 bit binary input code.

Full muting is provided (for input codes 11 11 XX where X is a 1 or 0).

On chip switches enable loudness compensation to provide bass boost at high attenuation settings.

Absolute maximum ratings $T_A = +25°C$

* V_{DD} (to GND)	+14V
* V_{BB} (to GND)	−14V
Voltage (pins 11, 12, 13) to GND	V_{BB}, +14V
V_{IN} (to GND)	±35V
Digital input voltage to GND	−0.3 to V_{DD}
Output voltage (pin 1) to GND	−100mV to V_{DD}
Power dissipation (package)	670mW
Operating temperature	0 to +70°C
Storage temperature	−65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

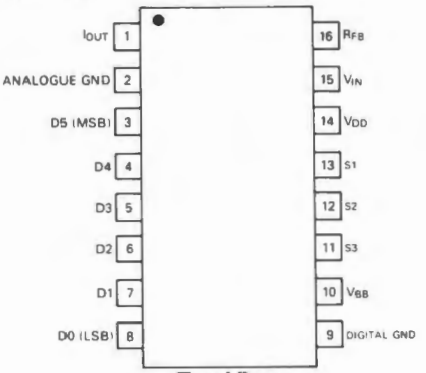
CAUTION:
ESD (electro-static-discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

Electrical characteristics $V_{DD} = +5$ to $+12V$, $V_{BB} = 0$ to $-12V$, pins 11-13 open, $T_A = 0$ to $+50°C$ unless otherwise noted

Features

- Attenuation range: 0 to 88.5dB plus full muting
- Resolution: 1.5dB
- Low distortion: THD better than −98dB
  IMD better than −92dB
- Includes switches for loudness compensation
- Low power consumption
- Excellent S/N ratio: 100dB (20Hz – 20kHz)
- Complies with DIN 45403 and DIN 45405
- Latch proof operation

Pin Connections



Top View

NOTES
1. Output amplifier (and, amplifier supplies) must be capable of 30V peak output.
2. Output noise voltage density includes op amp noise.
3. The RS 7110 is guaranteed monotonic for all attenuation settings between 0 and 88.5dB.
4. Input resistance for a given unit is constant for all input conditions.
5. Feedthrough is primarily dependent upon printed circuit board layout.

* If loudness compensation switches (S1, S2, S3) are not used, the negative power supply may be omitted and V_{BB} (pin 10) connected instead to DGND (pin 9). In this case the absolute maximum rating of V_{DD} is +17V.

Parameter	Test Conditions	RS 7110 With "Ideal OP-AMP"	RS 7110 with RS 071 OP-AMP (Fig 1)	Units
Attenuation Range	V_{IN} = 10V rms @ 1kHz	0 to −88.5	0 to −88.5	dB
Resolution	Frequency Range 20Hz to 20 kHz	1.5 max	1.5 max	dB
Attenuation Accuracy(Absolute) 0dB to − 48dB −48dB to −88.5dB	(Note 3)	 ±0.7 max Monotonic	 ±0.7 max Monotonic	dB
Total Harmonic Distortion (THD)	per DIN 45403, BLATT 2 (with input level of 1V rms)	−98 max	−85 typ	dB
Intermodulation Distortion (IMD)	per DIN 45403, BLATT 4	−92 max	−79 typ	dB
V_{IN}	for <1% (max) THD (Note 1)	30 max	10 max	V peak
Feedthrough Error	1 KHz (Note 5)	−85	−85	dB
Output Noise Voltage Density	20Hz to 20kHz (Note 2)	30 max	70 typ	$nV/\sqrt{Hz}$
Bandwidth	0dB Attenuation	D.C. to 150 min	D. C. to 250 typ	kHz

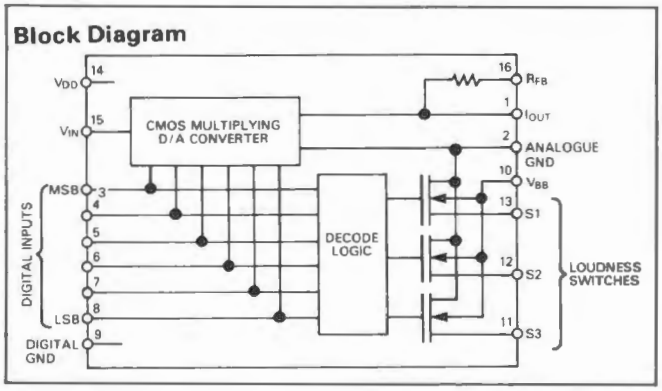
See page 2 for notes

Audio characteristics $V_{DD} = +12V$, $V_{BB} = -12V$, $V_{IN} = -10V$, pins 11-13 open, $T_A = 0$ to $+50°C$ unless otherwise noted

Parameter	Test Conditions	Limit
ANALOG INPUT		
Input Resistance of V_{IN} (pin 15)	V_{OUT} = 0V (Note 4)	9kΩ min 18kΩ max
LOUDNESS SWITCHES		
Switch ON Resistance R_{ON}	Switch Current = 1mA	600Ω max
Switch OFF Leakage Current	V_{switch} = +12V	1μA max
Switch Coding		See Table 1
DIGITAL INPUTS		
V_{INH}		11.5V min
V_{INL}		0.5V max
I_{NH}		1μA max
I_{NL}		1μA max
C_{IN}		5pF typ
POWER REQUIREMENTS		
V_{DD}		+12V nom
V_{BB}		−12V nom
I_{DD}	Digital Inputs = V_{INL} or V_{INH}	1mA max
I_{BB}		100μA max
Total Power Dissipation		5mW typ

NOTES
1. Output amplifier (and, amplifier supplies) must be capable of 30V peak output.
2. Output noise voltage density includes op amp noise.
3. The RS 7110 is guaranteed monotonic for all attenuation settings between 0 and 88.5dB.
4. Input resistance for a given unit is constant for all input conditions.
5. Feedthrough is primarily dependent upon printed circuit board layout.

Block Diagram



Circuit description

The block diagram above illustrates the internal structure of the RS 7110. The input signal is applied to pin 15 which is the input to a 6 bit multiplying digital to analogue converter. This D/A converter operates as an accurate digitally controlled attenuator, the attenuation being controlled by a 6 bit digital input code applied to pins 3 through to 8. The attenuated output is a current which is converted to a voltage via an external operational amplifier. An internal decoder controls 3 FET switches which can be used for loudness compensation.

Analogue circuit performance:

Table 1 gives the nominal attenuation in dB for the RS 7110 for all digital input codes. It also shows the loudness switch states and the nominal output voltage when using an external operational amplifier (as shown in Figure 1) and a fixed −10 volt reference applied to V_{IN} (pin 15). It may be seen that the transfer function for the circuit of Figure 1 is given by

$$V_{OUT} = -V_{IN} .10^{-\left(\frac{1.5N}{20}\right)}$$

where N is the binary input for values 0 to 59. For N = 60 through 63 the input is fully muted, that is, the attenuation is infinite.

Figure 1 **Basic circuit**

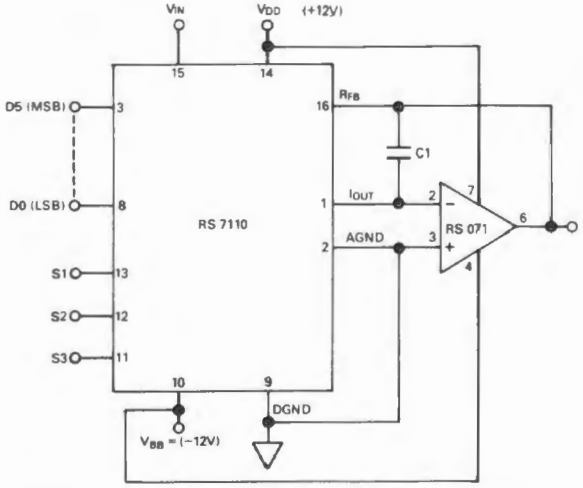
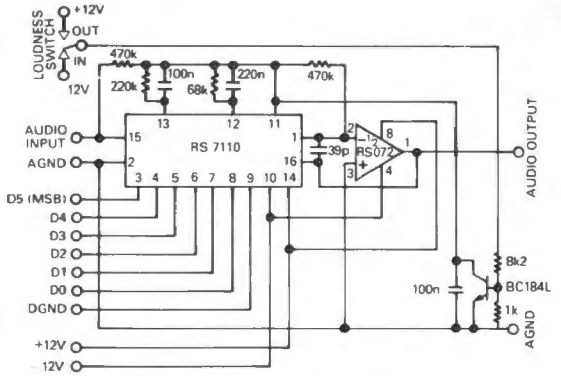


Table 1 Performance

N	Digital Input D5 D0	Attenuation dB	[1] Switches S1	S2	S3	[2] VOUT
0	00 00 00	0.0				10.000
1	00 00 01	1.5				8.414
2	00 00 10	3.0				7.079
3	00 00 11	4.5				5.597
4	00 01 00	6.0				5.012
5	00 01 01	7.5				4.217
6	00 01 10	9.0				3.548
7	00 01 11	10.5				2.985
8	00 10 00	12.0				2.512
9	00 10 01	13.5				2.113
10	00 10 10	15.0				1.778
11	00 10 11	16.5				1.496
12	00 11 00	18.0				1.259
13	00 11 01	19.5				1.059
14	00 11 10	21.0				0.891
15	00 11 11	22.5				0.750
16	01 00 00	24.0				0.631
17	01 00 01	25.5				0.531
18	01 00 10	27.0				0.447
19	01 00 11	28.5				0.376
20	01 01 00	30.0				0.316
21	01 01 01	31.5				0.266
22	01 01 10	33.0				0.224
23	01 01 11	34.5				0.188
24	01 10 00	36.0				0.158
25	01 10 01	37.5				0.133
26	01 10 10	39.0				0.112
27	01 10 11	40.5				0.0944
28	01 11 00	42.0				0.0794
29	01 11 01	43.5				0.0668
30	01 11 10	45.0				0.0562
31	01 11 11	46.5				0.0473
32	10 00 00	48.0	■			0.0398
33	10 00 01	49.5	■			0.0335
34	10 00 10	51.0	■			0.0282
35	10 00 11	52.5	■			0.0237
36	10 01 00	54.0	■			0.0200
37	10 01 01	55.5	■			0.0168
38	10 01 10	57.0	■			0.0141
39	10 01 11	58.5	■			0.0119
40	10 10 00	60.0		■		0.0100
41	10 10 01	61.5		■		0.00841
42	10 10 10	63.0		■		0.00708
43	10 10 11	64.5		■		0.00596
44	10 11 00	66.0		■		0.00501
45	10 11 01	67.5		■		0.00422
46	10 11 10	69.0		■		0.00355
47	10 11 11	70.5		■		0.00299
48	11 00 00	72.0		■		0.00251
49	11 00 01	73.5		■		0.00211
50	11 00 10	75.0		■	■	0.00178
51	11 00 11	76.5		■	■	0.00150
52	11 01 00	78.0		■	■	0.00126
53	11 01 01	79.5		■	■	0.00106
54	11 01 10	81.0		■	■	0.000891
55	11 01 11	82.5		■	■	0.000750
56	11 10 00	84.0		■	■	0.000631
57	11 10 01	85.5		■	■	0.000531
58	11 10 10	87.0		■	■	0.000447
59	11 10 11	88.5		■	■	0.000376
60	11 11 XX[3]	∞				

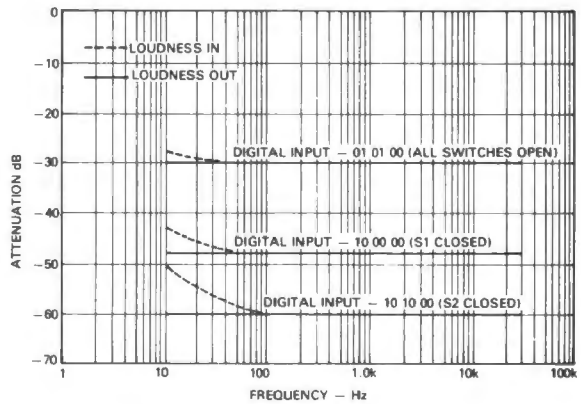
NOTES:
[1] Switch closed in shaded area
[2] VIN = −10V dc
[3] X = 1 or 0 Output is fully muted for N>60.

Figure 2 **Single channel audio attenuator with loudness compensation**



The circuit shown in Figure 2 is a single channel attenuator with loudness compensation. Figure 3 shows the attenuation vs. frequency for two digital input codes at which the loudness compensation switches S1 & S2 are activated. If the loudness compensation switches S1, S2 & S3 are not required the negative supply for the RS 7110 may be omitted and V_{BB} (pin 10) connected instead to DIGITAL GND (pin 9).

Figure 3 **Attenuation vs. frequency**



High frequency amplifiers

R_{FB} and the output capacitance of the AD7110 create a phase lag in the output amplifier's feedback circuit. This phase lag, in conjunction with the amplifier's phase lag, may cause ringing or oscillation. When using a high speed amplifier, shunting the amplifier input to output with 30-50pF of feedback capacitance (C1) ensures stability.

RS data

Figure 4 **Digital threshold voltage vs. power supply voltage**

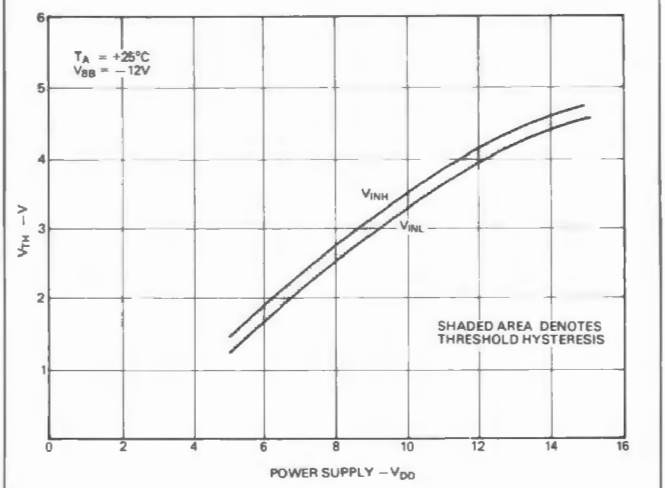
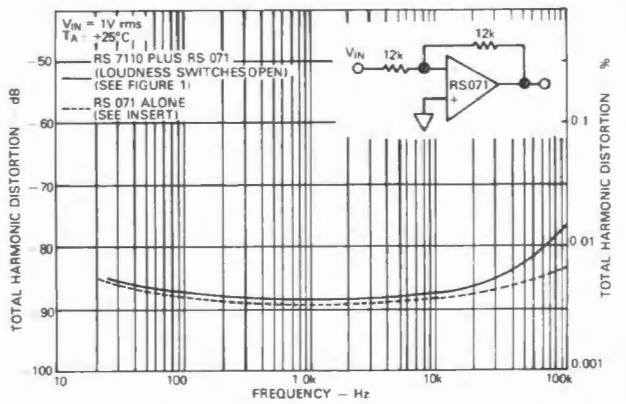


Figure 5 **Total harmonic distortion vs. frequency**



Circuit precautions

To realise the full attenuation range of the RS 7110 particular attention should be given to circuit layout and supply decoupling.

Input and output connections should be kept separate on the p.c.b. Short connections are advised, where possible, to avoid pick-up. Adequate supply decoupling is essential, 100nF disc ceramics or greater may be employed between the supply rails and their associated grounds, mounted close to the device pins.

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RS data

Chopper stabilized operational amplifiers RS7650 and 7652

Stock numbers 303-854 and 630-667

Two chopper stabilized CMOS operational amplifiers featuring extremely low input offset voltage, excellent time and temperature drift characteristics, very high gain, common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), low intermodulation effects and high bandwidth.

Both amplifiers employ circuitry that is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes and over-range lock-up.

They achieve their low offset voltage by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases.

Two external capacitors store the correcting potentials on the two amplifier nulling inputs which are then used to reduce the offset voltage of the complete amplifier.

These operational amplifiers can be configured in all normal op-amp application circuits providing a significant improvement in circuit performance over conventional amplifiers.

The RS7652 is similar to the RS7650 but offers improved noise performance and a wider common-mode input voltage range. The bandwidth and slew rate are reduced slightly.

Absolute maximum ratings

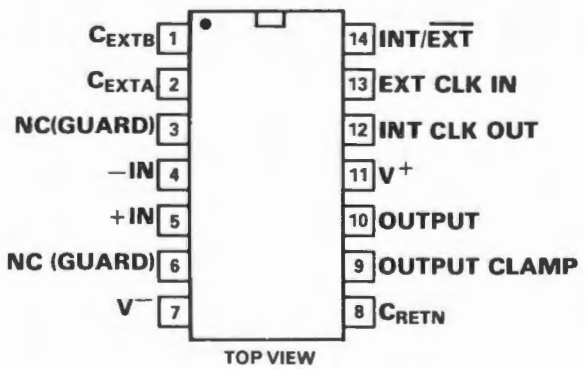
Total supply voltage (V^+ to V^-) _____ 18 volts
Input voltage _____ (V^+ +0.3) to (V^- –0.3) volts
except EXT CLOCK IN: (V^+ +0.3) to (V^+ –6.0) volts*
Storage temp. range _____ –55°C to 150°C
Operating temp. range _____ 0°C to +70°C
Lead temperature (soldering, 10 sec) _____ 300°C
Voltage on control pins _____ V^+ to V^-
Duration of output short circuit _____ Indefinite
Current into any pin _____ 10mA
– while operating _____ 100μA
Cont. total power diss. (T_A = 25°C) _____ 375mW

*RS7650 only.

Features

- Extremely low input offset voltage – 1μV over temperature range
- Low long term and temperature drift of input offset voltage
- Low dc input bias current; 10pA 7650 (15pA 7652)
- Extremely high gain, CMRR and PSRR; 120dB 7650 (110dB 7652)
- High slew rate; 2.5V/μs 7650 (0.5V/μs 7652)
- Wide bandwidth; 2MHz 7650 (0.45MHz 7652) GBW product
- Internally compensated for unity gain operation
- Very low intermodulation effects (phase shift <10°)
- Clamp circuit to avoid overload recovery problems, allow comparator use
- Extremely low chopping spikes at input and output

Pin connections RS7650 and 7652



TOP VIEW

ATTENTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

Electrical characteristics: Test conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$ (unless otherwise stated)

Parameter	Symbol	Test conditions	Limits			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{OS}	$T_A = +25°C$ Over Operating Temperature Range		±0.7 ±1.0	±5	μV
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$			0.01	0.05	μV/°C
Input Bias Current (doubles every 10°C above about 60°C)	I_{BIAS}	$T_A = +25°C$ $0°C < T_A < +70°C$		1.5 (15) 35	10 (30)	pA
Input Offset Current	I_{OS}	$T_A = +25°C$		0.5 (25)	(60)	pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	$R_L = 10kΩ$, $V_{OUT} = ±4V$	120	150		dB
Output Voltage Swing (Note 3)	V_{OUT}	$R_L = 10kΩ$ $R_L = 100kΩ$	±4.7	±4.85 ±4.95		V
Common-Mode Voltage Range	CMVR		–5.0 (–4.3)	–5.2 to +2.0 (–4.8 to +4.0)	1.6 (3.5)	V
Common-Mode Rejection Ratio	CMRR	CMVR = –4.3V to 3.5V	110	120 (130)		dB
Power Supply Rejection Ratio	PSRR	± 3V to ±8V	120 (110)	130		dB
Input Noise Voltage	e_{np-p}	$R_S = 100Ω$, DC to 1Hz DC to 10Hz		(0.2) 2 (0.7)		μVp-p
Input Noise Current	i_n	f = 10Hz		0.01		pA/√Hz
Unity-Gain Bandwith	GBW			2.0 (0.45)		MHz
Slew Rate	SR	$C_L = 50pF$, $R_L = 10kΩ$		2.5 (0.5)		V/μs
Rise Time	t_r			0.2 (0.8)		μs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		4.5 (5.0)		16	V
Supply Current	I_{supp}	No Load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open	120	200 (400)	375	Hz
Clamp ON Current (Note 2)		$R_L = 100kΩ$	25	70 (100)	200	μA
Clamp OFF Current (Note 2)		$–4.0V < V_{OUT} < +4.0V$		1		pA
Offset Voltage vs Time				100		nV/√month

Figures in brackets relate to RS7652.

Typical operating characteristics RS7650

Figure 1 **Maximum output current as a function of supply voltage**

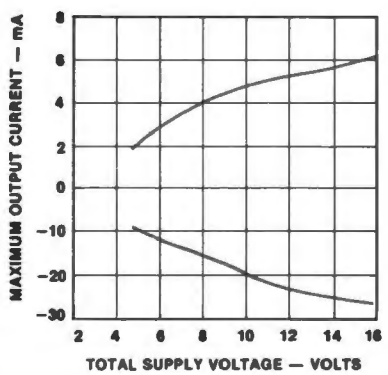


Figure 2 **Common-mode input-voltage range as a function of supply voltage**

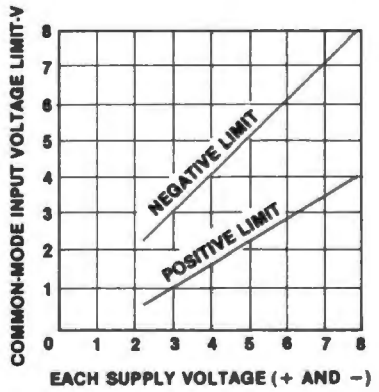


Figure 3 **Clock ripple referenced to the input as a function of temperature**

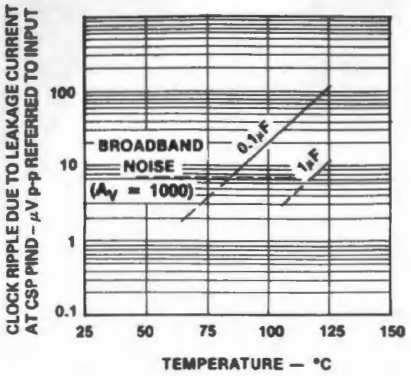


Figure 4 **10Hz p-p noise voltage as a function of chopping frequency**

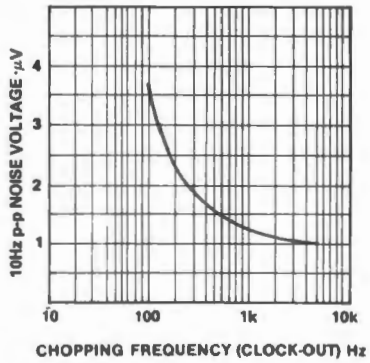


Figure 5 **Input offset voltage change as a function of supply voltage**

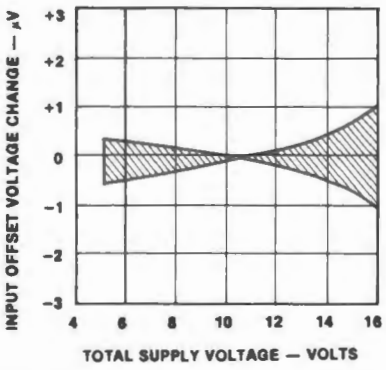


Figure 6 **Input offset voltage as a function of chopping frequency**

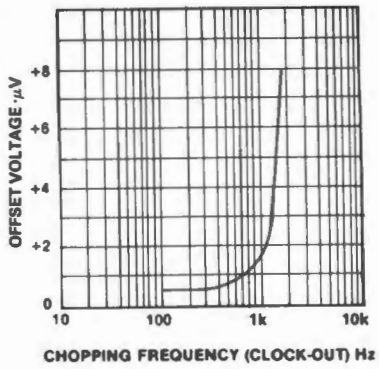


Figure 7 **Output with zero input; gain = 1000, balanced source impedance = 10kΩ**

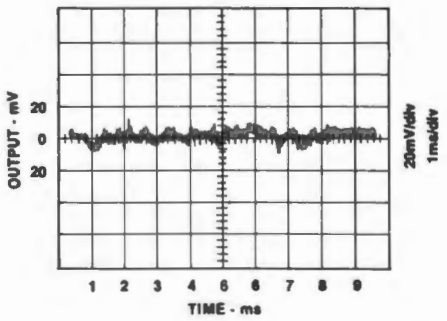
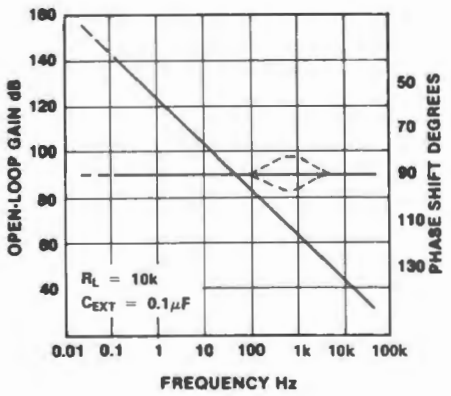


Figure 8 **Open loop gain and phase shift as a function of frequency**



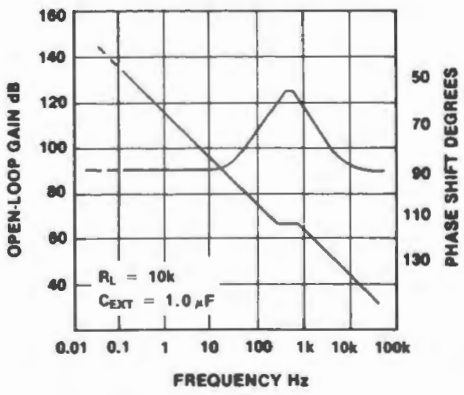


Figure 9 **Voltage follower large signal pulse response**

Note: the two different responses correspond to the two phases of the clock.

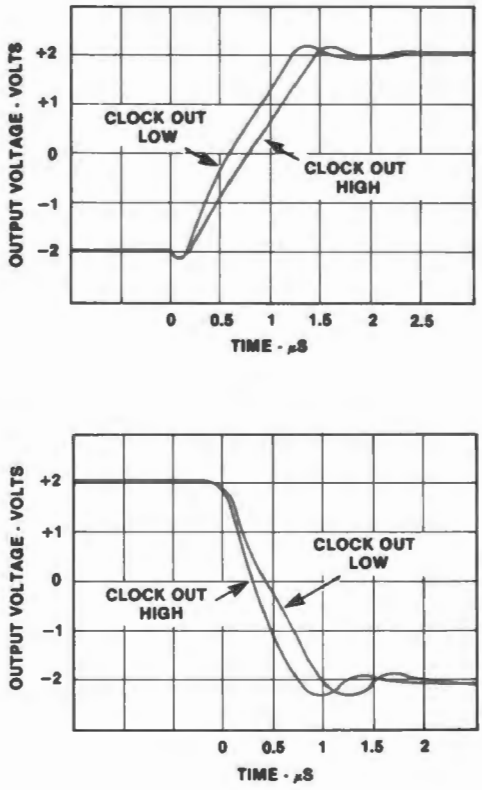


Figure 10 **N-Channel clamp current as a function of output voltage**

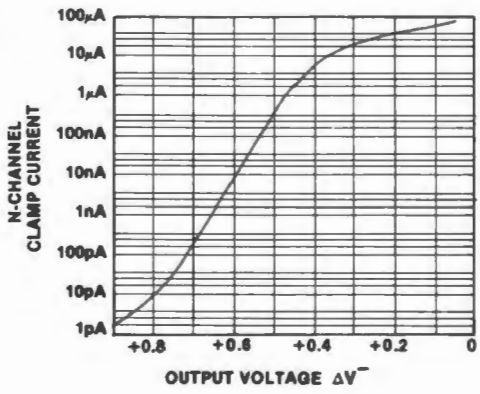
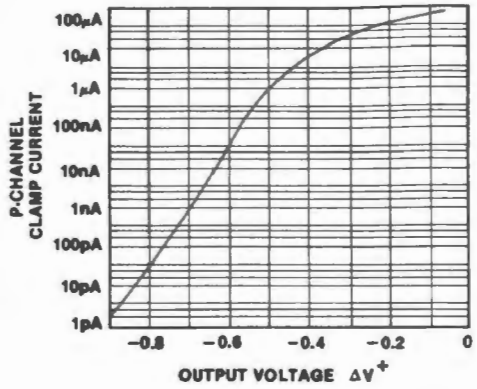


Figure 11 **P-Channel clamp current as a function of output voltage**



Typical operating characteristics (RS7652)

Figure 12 **Maximum output current as a function of supply voltage**

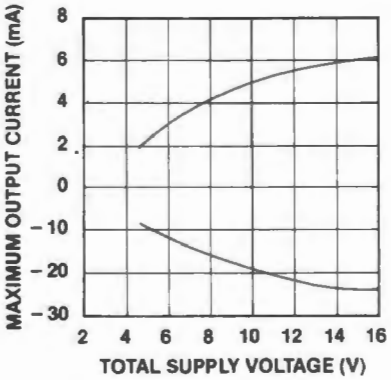


Figure 13 **Common mode input voltage range as a function of supply voltage**

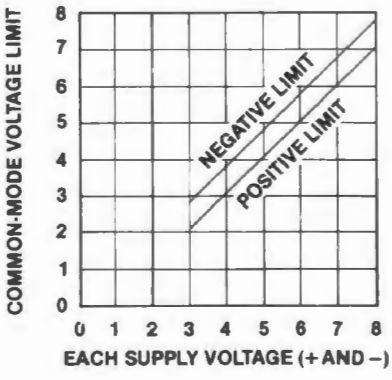
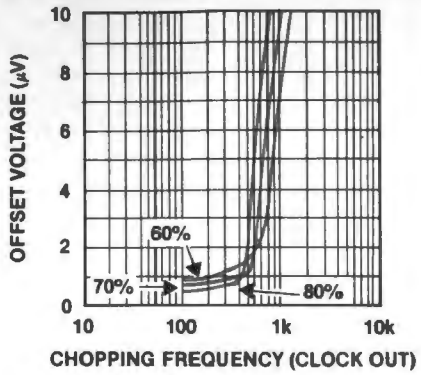


Figure 14 **Input offset voltage as a function of chopping frequency**



% parameter is EXT CLK in duty cycle

Figure 15 **10Hz p-p noise voltage as a function of chopping frequency**

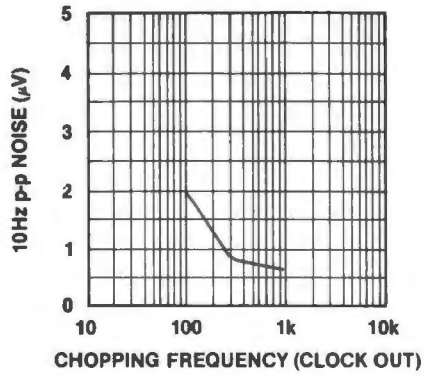


Figure 16 **Clock ripple referenced to the input as a function of temperature**

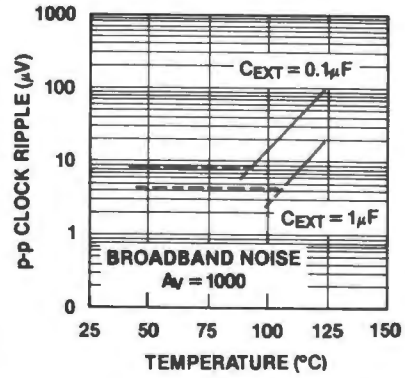


Figure 17 **Broadband noise, source impedance = 1kΩ, gain = 1000, C_{EXT} = 0.1μF**

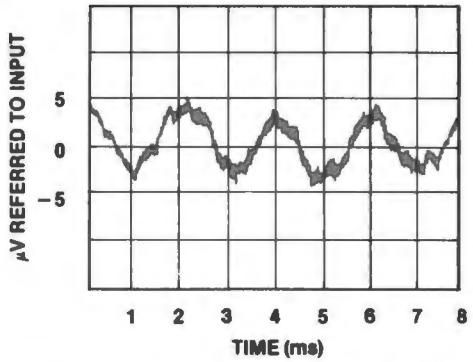


Figure 18 **Broadband noise, source impedance = 1kΩ, gain = 1000, C_{EXT} = 1.0μF**

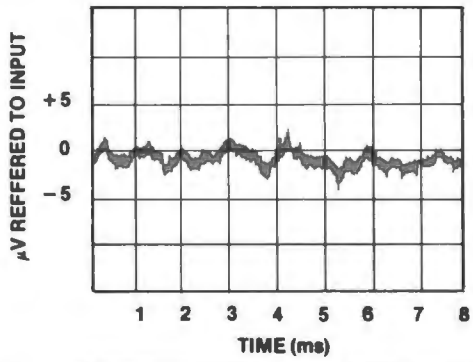
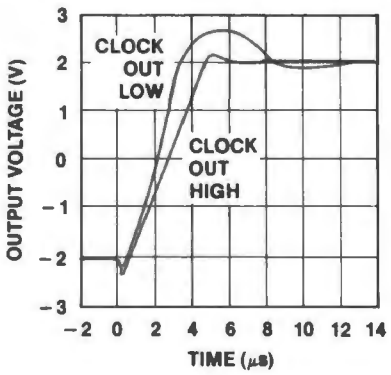


Figure 19 **Voltage follower large signal pulse response**

Note: the two different responses correspond to the two phases of the clock.



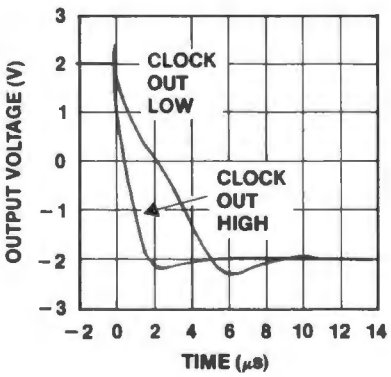


Figure 20 **Open-loop gain and phase shift as a function of frequency**

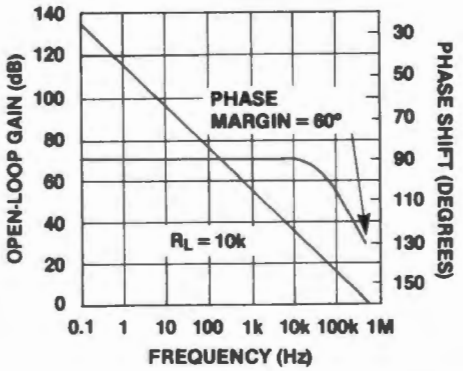


Figure 21 **N-Channel clamp current as a function of output voltage**

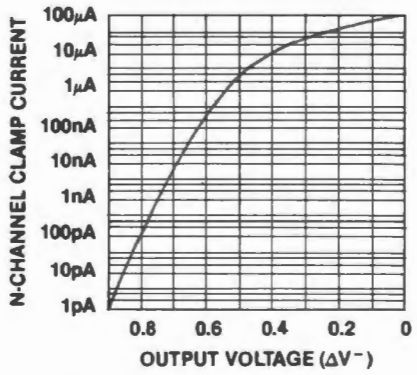


Figure 22 **P-Channel clamp current as a function of output voltage**

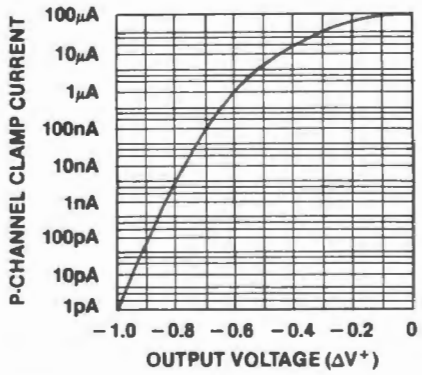
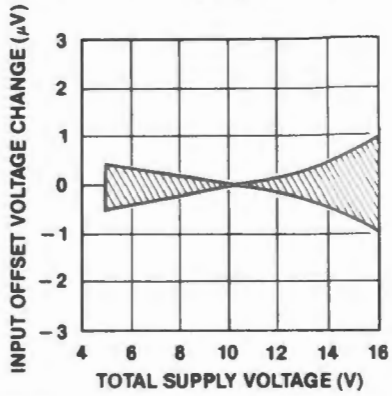


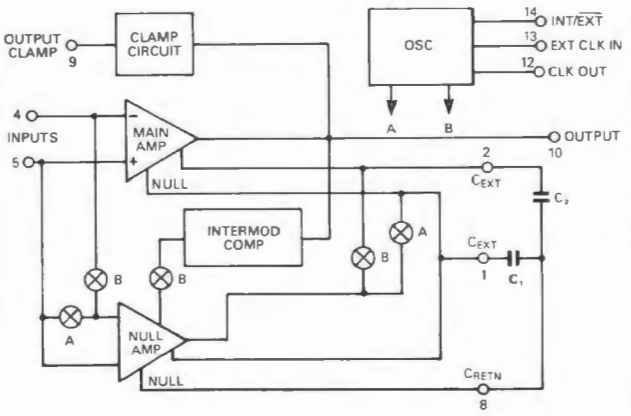
Figure 23 **Input offset voltage change as a function of supply voltage**



Circuit description

The RS7650 and 7652 circuit (Figure 24) consists of a main dc amplifier, a nulling dc amplifier, an output clamp, a compensation circuit that minimises the intermodulation between applied signals and the chopping frequency, and switches controlled by a two-phase oscillator. These switches are actuated on alternate half-cycles of the chopping frequency.

Figure 24 **RS7650 and 7652 block diagram**



During one clock half-cycle of the oscillator, the A switches close and the B switches open, driving the nulling amplifier to a null. A fraction of the voltage on capacitor C_1 is then added algebraically to the input of the nulling amplifier, so as to null the input-voltage offset error of this amplifier.

In the other clock half-cycle of the oscillator, the B switches close and the A switches open, driving the main amplifier to a null. During this clock interval, capacitor C_1 holds the nulling amplifier in its nulled state, while the main amplifier is being nulled. Capacitor C_2 maintains the main amplifier in its nulled state. The null sequence continually repeats, to produce a very low offset voltage.

The amplifiers minimise intermodulation effects by generating a compensating dynamic offset in the nulling amplifier when the B switches are closed. Therefore, the nulling amplifier does not see the main amplifier input signal as an offset error. Although the correction is not total, the intermodulation terms are reduced to such a low level that the ac and dynamic signals scarcely disturb the

nulling system. The results are minimum phase error and a clean gain-frequency curve.

The very effective approach prevents input overloads – a clamp in the feedback network reduces the closed-loop gain of the main amplifier just before the circuit reaches its maximum output level. The clamp consists of a pair of low-leakage n and p-channel MOSFETs that turn on shortly before the output limits. The clamp network is brought out to an external pin. Tying this pin to the chip's inverting input implements the clamping automatically. The clamping action does not disturb the null network and has negligible effect on the device's input bias current in the active region.

Clock oscillator

The amplifiers have an internal oscillator giving a chopping frequency of 200Hz 7650 and 400Hz 7652, available at the CLOCK OUT pin. Provision has also been made for the use of an external clock. The INT/EXT pin has an internal pull-up and may be left open for normal operation, but to utilise an external clock this pin must be tied to V– to disable the internal clock. The external clock signal may then be applied to the EXT, CLOCK IN pin. At low frequencies the duty cycle of the external clock is not critical, since an internal divide-by-two provides the desired 50% switching duty cycle. However, since the capacitors are charged only when EXT CLK IN is HIGH, a 50-80% positive duty cycle is favoured for frequencies above 500Hz 7650 and 800Hz 7652 to ensure that any transients have time to settle before the capacitors are turned OFF. The external clock should swing between V+ and GROUND for power supplies up to ±6V, and between V+ and V+ –6V for higher supply voltages. Note that a signal of about 400Hz 7650 and 800Hz 7652 will be present at the EXT CLK IN pin with INT/EXT high or open. This is the internal clock signal before the divider.

In those applications where a probe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a STROBE signal is connected to EXT CLK IN during the time that the unknown signal is applied to the amplifier, neither capacitor will be charged as long as STROBE is low. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10μV/sec, and relatively long measurements can be made with little change in offset.

Applications

The amplifiers can be employed in any conventional op-amp configuration yielding significant improvements in circuit performance by reduction of input offset voltage and bias current. The basic inverting and non-inverting amplifier circuits are shown in Figures 25 and 26. The use of the output clamping circuit is optional and if used the overload recovery performance will be improved.

Figure 25 **Non inverting amplifier with (optional) clamp**

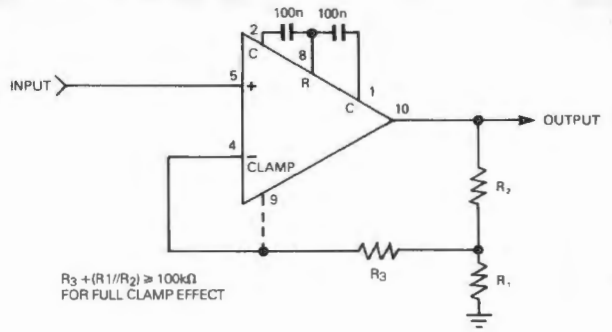
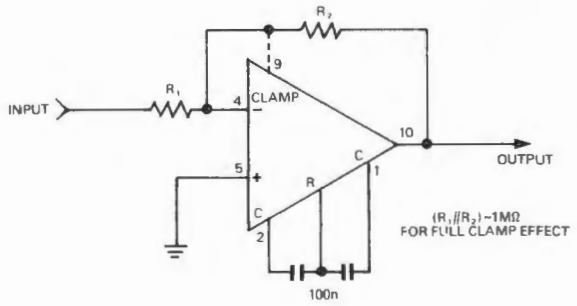
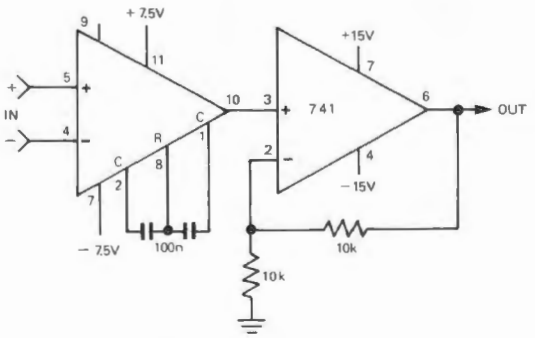


Figure 26 **Inverting amplifier with (optional) clamp**



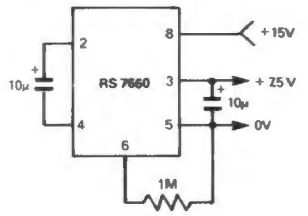
In some applications the output drive capability of the amplifiers may be insufficient. This limitation can be overcome by using a 741 or any other suitable op-amp to boost the output. A suggested circuit is shown in Figure 27.

Figure 27 **Using 741 to boost output drive capability**



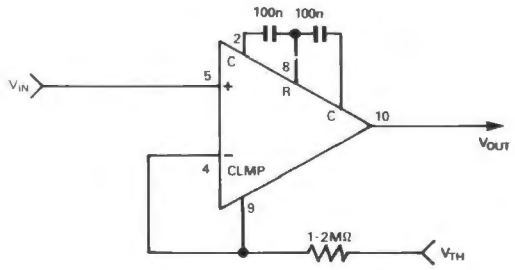
The amplifiers operate on ±8V max supply rails unlike the majority of conventional amplifiers which frequently operate on ±15V. Combining the amplifiers with standard op-amps can be easily implemented using a standard zener divider on the ±15V rails. An efficient, alternative approach is to employ the RS 7660 voltage converter i.c. (304-598) as shown in Figure 28 to split each rail. This configuration results in a voltage conversion efficiency of approximately 95%.

Figure 28 **Splitting +15V with RS 7660 Same for −15V. >95% efficient**



The output clamp circuit can be used to advantage in the zero offset comparator circuit shown in Figure 29. Conventional chopper stabilized amplifiers suffer from slow overload recovery, the clamp circuit prevents this by forcing the inverting input to follow the input signal just before an overload condition occurs. The threshold input signal source must tolerate the output clamp current (V_{IN}/R) without disturbance.

Figure 29 **Low offset comparator**



Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the amplifiers. Boards must be thoroughly cleaned with RS solvent cleaner or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or RS silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials.

This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used.

Figure 30 illustrates the use of the guard pins in three popular amplifier circuits.

Static protection

All device pins are static protected by the use of input diodes. However strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input leakage currents.

Figure 30 **Input guard connections**

Figure 30a **Inverting amplifier**

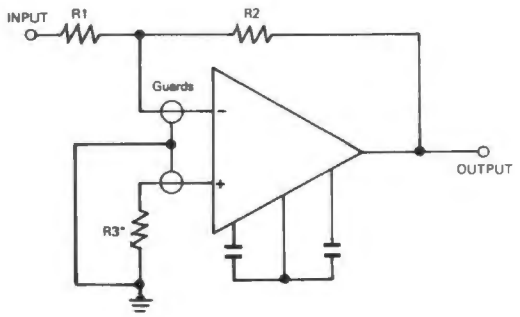


Figure 30b **Follower**

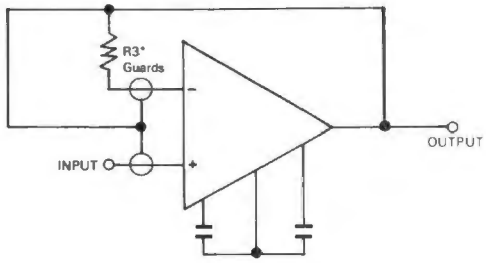
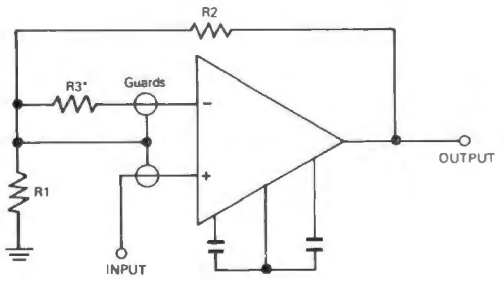


Figure 30c **Non-inverting amplifier**



*R3 is used to compensate for large source resistances

NOTE $\frac{R1\,R2}{R1+R2}$ MUST BE LOW IMPEDANCE

Latch-up avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latch-up, even under fault conditions.

Output stage/load driving

The output circuit is a high-impedance stage (approximately 18kΩ), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open loop gain is proportional to load resistance. For example the open loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for dc, this lower gain is of little consequence, since the dc gain is typically greater than 120dB even with a 1kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10kΩ or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° 7650 and 2° 7652 in the transition region where the main amplifier takes over from the null amplifier.

Thermo-electric effects

The ultimate limitations to ultra-high precision dc amplifiers are the thermo-electric or Peltier effects arising in thermo-couple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realise the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermo-electric coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Component selection

The two required capacitors, C_{EXTA} and C_{EXTB} have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 100nF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion. A high quality film type capacitor such as polycarbonate is preferred, although a ceramic or other lower grade capacitor may prove suitable in many applications.

RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

Fans and accessories

A range of dc and ac fans for equipment cooling with air flows from 46 to 350 cubic metres per hour. Appropriate filters, guards and supply leads are also described.

80 and 120 mm dc axial fans

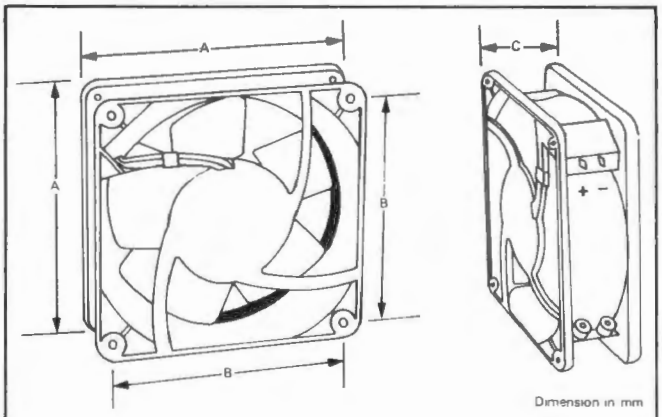
This RS range of brushless dc fans is specially suited for low power, portable or mobile equipment and standby facilities. The low power consumption reduces heat rise in the windings thereby prolonging life. Reliable all-metal construction designed for blowing or extracting as for conventional axial mains fans. Built-in solid state components use the Hall effect principle to achieve brushless commutation, thus eliminating electrical and reducing acoustic noise. Accessories include finger guards, filters and supply leads.

Absolute maximum ratings

Nominal working voltage, V_S ——— 12/24V dc
Maximum continuous over-voltage ——— 16/32V dc
Maximum peak voltage (1 ms) ——— 20/40V dc
Operating temperature range ——— –30 to +70°C
Maximum short-term operating temp ——— +85°C
Storage temperature range ——— –55 to +90°C
Humidity rating at 95% RH, +40°C ——— 30 days
Life expectancy at V_S, –30 to +70°C ——— 20,000 hrs

Features

- Standard fixing centres
- Two sizes and two voltages
- Solid state commutation
- No external components required
- Low electrical noise
- Low power consumption
- Stall current protected
- Class B insulation
- Ball bearings
- VDE 0730 and CSA approved
- Vertical or horizontal mounting
- Black die cast frame



Dimension in mm

Stock Nos.	508-021 508-037	508-043 508-059
Dimensions A	80	120
B	71.5	105
C	38	38
Terminations	Flying leads 300 mm long	110 'spade' solder terminals accepting plug and lead accessory

Characteristics T_{amb} = 25°C, V_S = nominal, free air operation

Parameter	508-021	508-037	508-043	508-059	Units
Frame size	80	80	120	120	mm
Nominal working voltage	12	24	12	24	V dc
Operating voltage range	9.5 to 14	19 to 28	9.5 to 14	19 to 28	V dc
Running current	240	120	400	200	mA
Air flow (note 1)	60		160		m³/h
Power consumption	3		5		W
Current when stalled	35		35		mA
Acoustic noise at 1 m	38		47		dB(A)
Nominal speed	330		2800		rpm

Note 1. See page 6 for conversion chart of air flow in other units, and page 4 for typical operating characteristics.

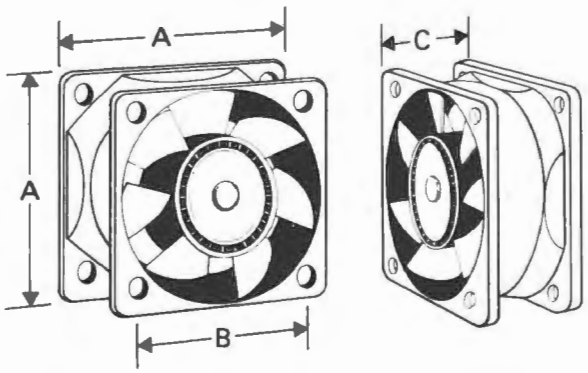
62mm Slimline dc axial fans

A pair of compact axial flow fans operating from 12 or 24V. The high efficiency fans have over-temperature and over-current protection and can be reverse mounted for blowing or extraction. The fans are protected against reverse polarity and feature brushless motors to minimise the effect of interference on nearby equipment. The low power consumption makes them ideal for battery powered operation.

Features

- 12V and 24V versions available
- Meets VDE 0730
- No external components required
- Frame thickness 25mm (1in)
- Electronically commutated motor
- Low power consumption
- Maintenance free

62mm Slimline



Stock Nos.	501-913 501-929
Dimensions A	62
B	50
C	25.4
Terminations	Flying leads 310mm long

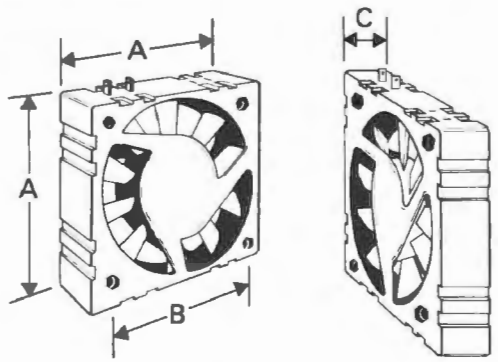
62mm Ultraslim dc axial fans

A range of three extremely low profile axial fans operating from 5, 12 or 24V supplies. The fans are polarity protected and can be reverse mounted for blowing or extraction. The 14mm casing depth allows for vertical mounting in modern racking systems adjacent to 'hot spots' on printed circuit boards. Accessories include finger guards, filters and supply leads.

Features

- Frame thickness 14mm
- 5V, 12V and 24V versions available
- Reverse polarity protected
- Brushless motor
- Sleeve bearings
- Maintenance free
- Vertical or horizontal mounting

62mm Ultraslim



Stock Nos.	501-884 501-890 501-907
Dimensions A	62
B	50
C	14
Terminations	110 'spade' solder terminals accepting plug and lead accessory

Characteristics T_{amb} = 25°C, V_S = nominal, free air operation

	Slimline		Ultraslim			Units
Stock number	**501-913**	**501-929**	**501-907**	**501-890**	**501-884**	
Nominal working voltage	12	24	5	12	24	V dc
Operating voltage range	6 to 15	12 to 30	3.5 to 7.5	8.5 to 18	17 to 36	V dc
Running current	125	125	250	110	45	mA
Air flow (note 2)	40	40	20	20	20	m^3/h
Power consumption	3	3	1.3	1.3	1.1	W
Current when stalled	100	50	250	110	45	mA
Acoustic noise at 1m	40	40	32	32	32	dB(A)
Nominal speed	5300	5300	3400	3400	3400	rpm

Note 2. See page 6 for conversion chart of air flow in other units, and page 4 for typical operating characteristics.

ac axial fans

Standard axial fans

A range of six ac mains fans designed for cooling electrical and electronic equipment. All-metal construction designed for mounting either way round for extraction or blowing. Sizes 80 and 120mm utilise sleeve bearings: size 160mm has ball bearings. Accessories include finger guards, filters and supply leads.

Features

- 46, 160 or 350m³/h airflow
- No external components required
- Impedance protected*
- Meets VDE 0730
- Vertical or horizontal mounting
- Black die cast frame
- Class B insulation
- Three standard sizes
- 240V and 110V ac versions

*160mm version incorporates thermal cut-out.

Low noise axial fans

A pair of ac mains fans for use in equipment where ambient noise is low and undue acoustic noise caused by the fan would be noticeable and undesirable. Particularly recommended in confined areas or office and computer room environments. Low noise figures are achieved at the expense of airflow.

Features

- 28dB(A) noise level
- Impedance protected
- Class B insulation
- 240V and 110V versions
- Meets VDE 0730
- Standard 120 × 38mm 'box' frame
- Sleeve bearings
- 110 'spade' solder terminals
- Accepts RS guard, filter and lead
- Black die cast frame
- Vertical or horizontal mounting

Slimline axial fans

A pair of ac mains fans with a frame width of only 25mm, particularly recommended where equipment space is limited. Metal frame with plastic impeller can be reverse mounted for extraction or blowing. Accessories include finger guards, filters and supply leads. Compactness is achieved at the expense of airflow.

Features

- Frame thickness 25mm (1 in)
- Standard fixing centres
- Vertical or horizontal mounting
- 240V and 115V ac versions
- Black die cast frame
- Sleeve bearings
- No external components required
- Shaded pole motor
- 110 'spade' solder terminals
- Class B insulation
- UL and CSA approved

Earthing

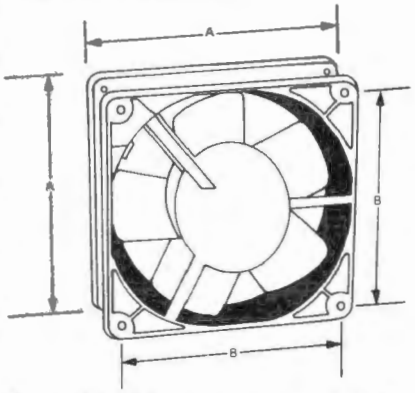
All ac axial fans have 2 pole terminations or flying leads. An earth connection must be run separately to the frame of the fan and secured by a 5mm M4 screw in the threaded hole provided. (Some fans have an M4 screw already fitted.) Ensure paint has been removed from the earth hole to give good earth contact.

Characteristics T_{amb} = 25°C, V_S = nominal; f = 50Hz, free air

	Standard Fans						Low noise		Slimline		Units
Stock No.	**509-046**	**509-030**	**509-068**	**509-226**	**508-065**	**508-071**	**507-400**	**507-393**	**507-236**	**507-220**	
Frame size (Dimension A)	80	80	120	120	160	160	120	120	120	120	mm
Nominal working voltage	110	240	110	240	110	240	110	240	115	240	V ac
Operating voltage range	99-121	216-264	99-121	216-264	99-121	215-264	99-121	216-264	103-127	208-264	V ac
Running current	115	70	240	120	500	250	120	60	135	80	mA
Stall current	210	100	375	170	750	400	130	65	200	100	mA
Air flow (note 3)	46		160		350		83		108		m³/h
Power consumption	12		23		40		11		14		W
Acoustic noise at 1m	34		44		49		29		44		dB(A)
Nominal speed	2650		2650		2760		1600		2500		rpm
Operating temperature range	–10 to +70		–10 to +50		–30 to +65		–10 to +60		–10 to +55		°C
Life expectancy (over temp. range)	15,000		15,000		20,000		30,000		25,000		hrs

Note 3. See page 6 for conversion chart of air flow in other units and page 5 for typical operating characteristics.

160mm versions

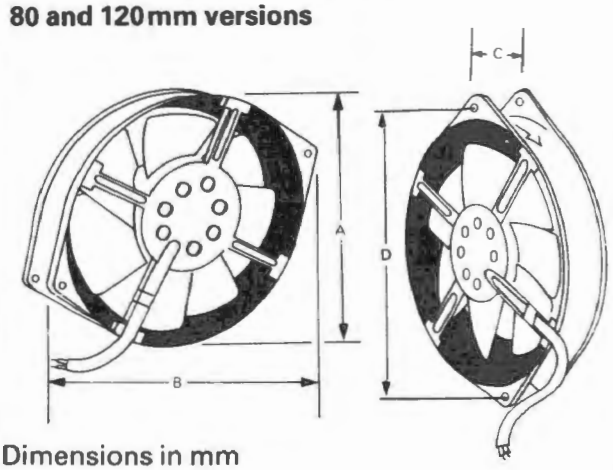


See table 1 for mounting details

Dimensions in mm

Stock Nos.	509-406 509-030	509-068 509-226	507-400 507-393	507-236 507-220
Dimensions A	80	120		
B	71.5	105		
C	38	38 (25 for slimline version)		
Terminations	Flying leads 300mm long	110 'spade' solder terminals accepting plug and lead accessory		

80 and 120mm versions



Dimensions in mm

See table 1 for mounting details

Stock Nos.	508-065 508-071
Dimensions A	150
B	172
C	55
D	162
Terminations	Flying leads 300mm long

Operating characteristics (without filter)

Figure 1: **80mm d.c. fans**

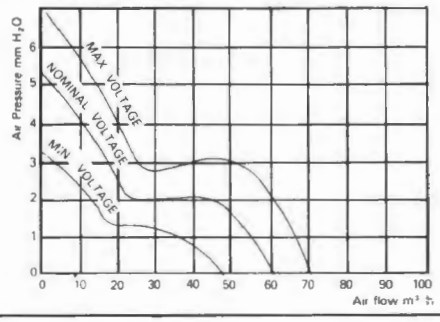


Figure 2: **120mm d.c. fans**

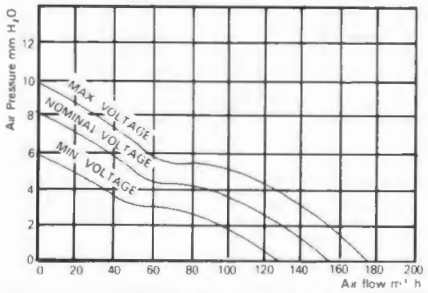


Figure 3 **62mm Slimline dc fans**

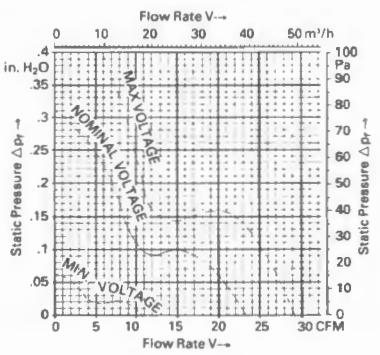


Figure 4 **62mm Ultraslim dc fans**

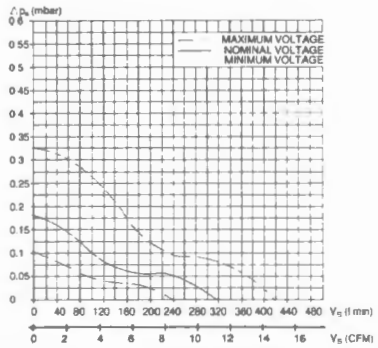


Figure 5 **80mm ac fans**

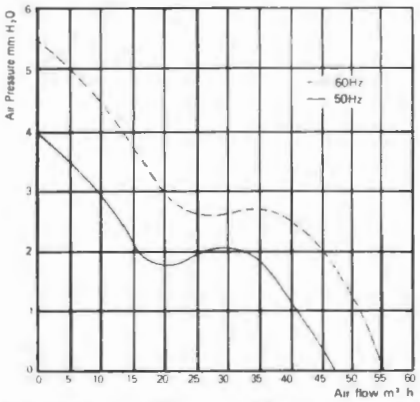


Figure 6 **120mm ac fans**

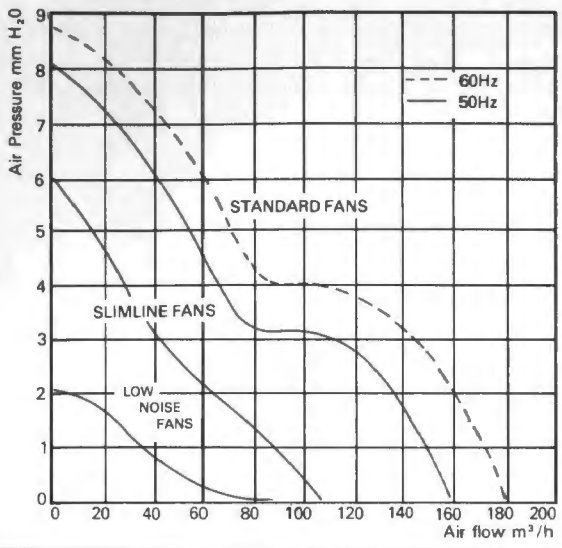
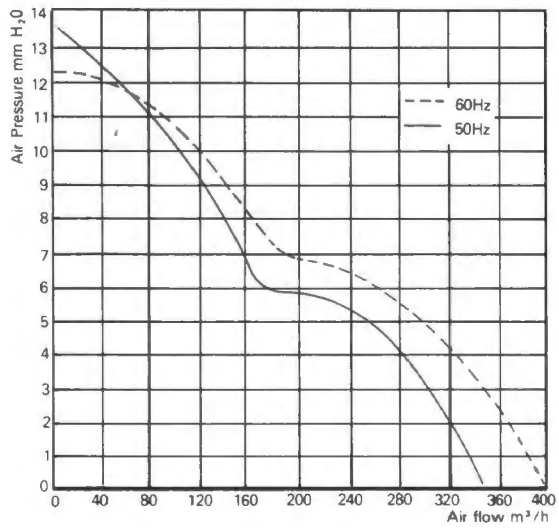
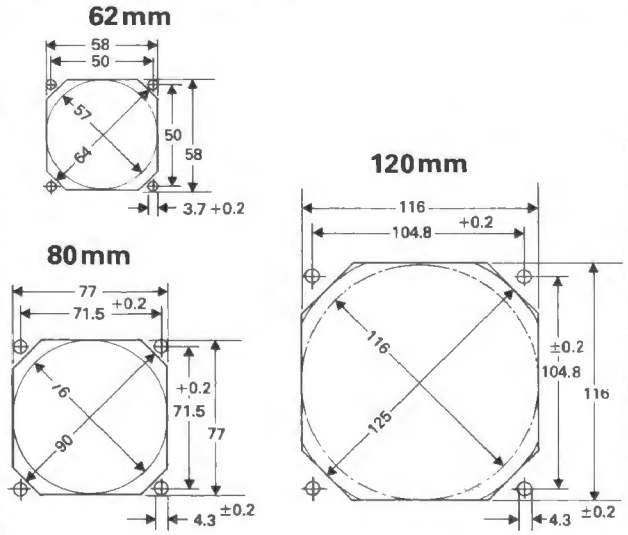


Figure 7 **160mm ac fans**



Panel cut-outs and mounting holes

Figure 8 **Panel cut outs**



Note. Fan efficiency is reduced if simplified circular cut-out is used: for optimum efficiency, shape cut-out as shown to fit fan venturi.

Table 1 **Panel fixing for ac fans**

Fan size	80mm	120mm	160mm
Cut-out diameter	76	116	144
Fixing centres	71.5	105	162
P.C.D.	101	149	229
Mounting holes, dia.	4 × 4.5	4 × 4.5	2 × 4.5

Fan accessories

Table 2 **List of accessories**

Description	Size mm	Stock No.
Fan filter unit	62	**501-941**
	80	**507-911**
	120	**507-905**
	160	**507-898**
Replacement filters (packs of 3)	62	**501-957**
	80	**507-882**
	120	**507-876**
	160	**507-860**
Plug and lead	62 and 120	**507-450**
Finger guards	62	**501-935**
	80	**509-052**
	120	**509-232**
	160	**507-961**

Filter units

Four sizes of filters are designed for use with the entire range of ac and dc axial fans (see Figure 10).

The filter front grille, made from matt black ABS plastic, is secured to the filter back plate using two quick-release screws (supplied) to facilitate filter changing. Dimensions are given in Figure 9.

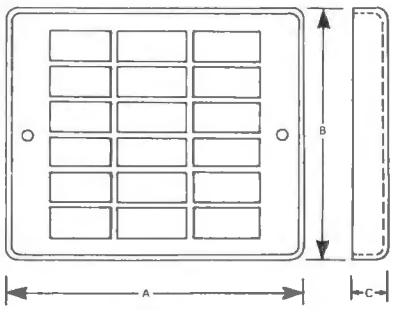
The back plate, made from zinc plated black passivated mild steel, is mounted on the same fixing centres as the corresponding fan, but on the opposite side of the mounting panel to the fan. The front grille completely obscures the back plate when assembled. See Figure 9 for overall dimensions.

The filter pad housed between the front grille and back plate is made of synthetic material which will withstand temperatures up to 100°C and is flame resistant to BS2963. It gives a 75% retention by weight of dust particles down to 5 microns. Depending on the type of dust, filters may be cleaned by shaking out the dust (but do not use compressed air lines) or by washing in warm water with a mild detergent. (Do not wring.) Replacement filters are available in packs of three.

Finger guards

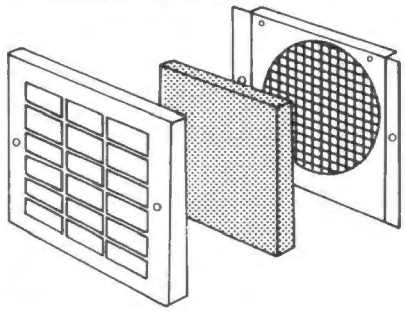
A range of bright zinc-plated steel finger guards for all RS axial fans is available. Fixing centres correspond to the fan mounting holes given in Figure 8 and Table 1.

Figure 9 **Filter front grille**



Fan size	62mm	80mm	120mm	160mm
Dimensions A	64	125	162	226
B	64	105	136	190
C	14	17	17.5	18

Figure 10 **Typical filter unit**



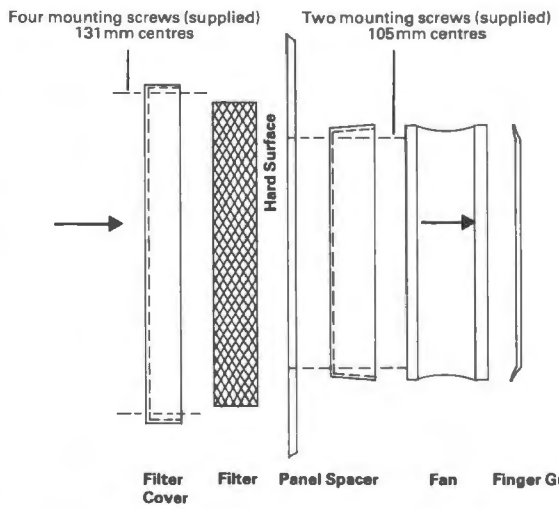
Note. Fixing centres correspond to fan fixing centres.

Additional fan filter unit 508-510

An earlier design of fan filter unit with washable filter, for use with 120mm ac axial fans only. Replacement filters are NOT available.

Manufactured from gloss black ABS thermoplastic. The particular filter supplied is unidirectional. Full instructions for assembly and fitting as supplied with the product.

Figure 11 **Additional fan filter 508-510**



Plug and lead assembly

For RS Components 120mm axial and 62mm 'Ultraslim' fans, an integral moulded plug and 600mm lead is available. The twin lead is double insulated and the plug conforms to creepage, clearance and breakdown requirements of BS415. Fits all two terminal fans with 0.110in (2.8mm) solder terminals spaced 0.3in (8mm).

Figure 12 **Fan plug and lead**

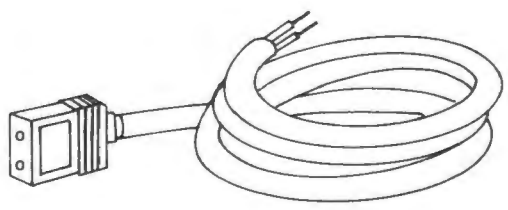
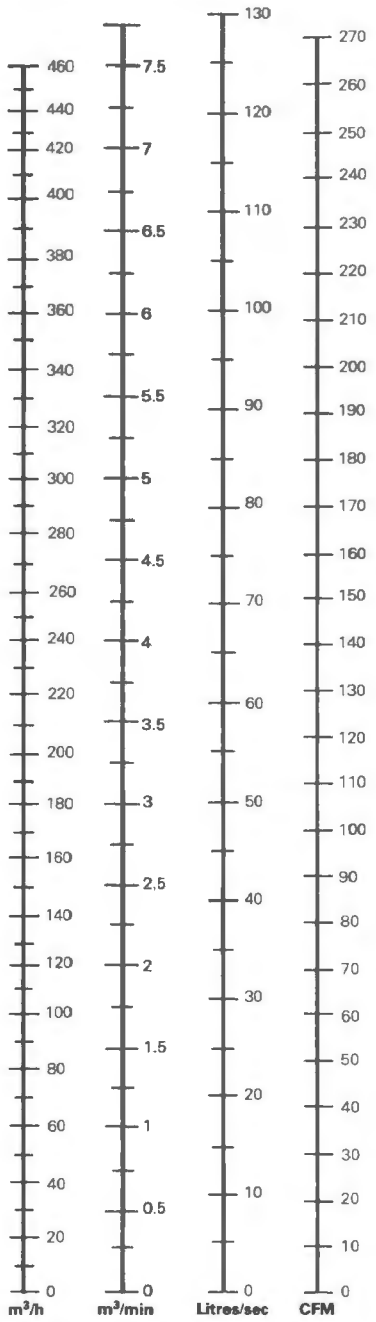


Figure 13 **Air flow conversion chart**



Air flow calculations (axial fans)

The reduction of air flow when a filter is fitted to a fan varies between 15 and 20%. This loss will increase as dirt is collected in the filter pad, so regular inspection and replacement is recommended. Other factors which affect air flow are the losses due to resistance caused by ducting, louvres, and turbulence casued by the shape and position of the items being cooled.

In a resistance-free situation, the air flow required to maintain a certain peak temperature in an object dissipating P watts of energy can be expressed in its simplest form as:

$$\frac{2.6 \times P}{\triangle t} \text{ m}^3/\text{h}$$

where $\triangle t$ is the permissible temperature rise above ambient in °C. (See Figure 13 for conversion chart to other units.)

In practice, however, the air flow must be increased considerably to compensate for various losses. Multiply the airflow required by some or all of the following typical resistance factors.

Filter resistance, Rf = 1.2 for new filters or 1.8 or higher for used filters.

Ducting resistance, Rd = 1.3 for straight ducting of the same diameter as the fan, and 1.7 or higher for ducting bent through 90°C.

Louvre resistance, R1. Allow up to 2.5 for inlet louvres of the same diameter as the fan, with 50% free area. For fine mesh air inlet grilles this factor may be as high as 4.

Baffle resistance, Rb, a variable depending on the turbulence and baffling effect caused by internal equipment layout. Allow at least a factor of 2.

Cut-out resistance, Rc, a factor dependent on the accuracy of the panel cut-out with respect to the fan venturi dimensions. (See Figure 8 note.)

Allow up to 1.25 for the turbulence created by mismatch of the cut-out to the fan venturi.

Applications

Fan failure monitor (dc axial)

Many designers require a fail-safe system to safeguard expensive equipment which might be harmed by heat rise in the event of fan failure due to a blocked rotor. A useful feature of the dc range of fans permits a simple monitoring circuit to be installed for detecting and displaying such an event. This is achieved by inserting a low value resistor in the supply line to the fan and monitoring its volt drop caused by the supply current. If the rotor is blocked the motor switches off automatically and the supply current drops away to below 50 mA. The change in volt drop can be detected by a simple voltage comparator circuit incorporated into the customer's design.

An alternative to this analogue technique is a digital system which relies on the fact that the Hall effect commutation system creates a low level ripple at twice the rpm.

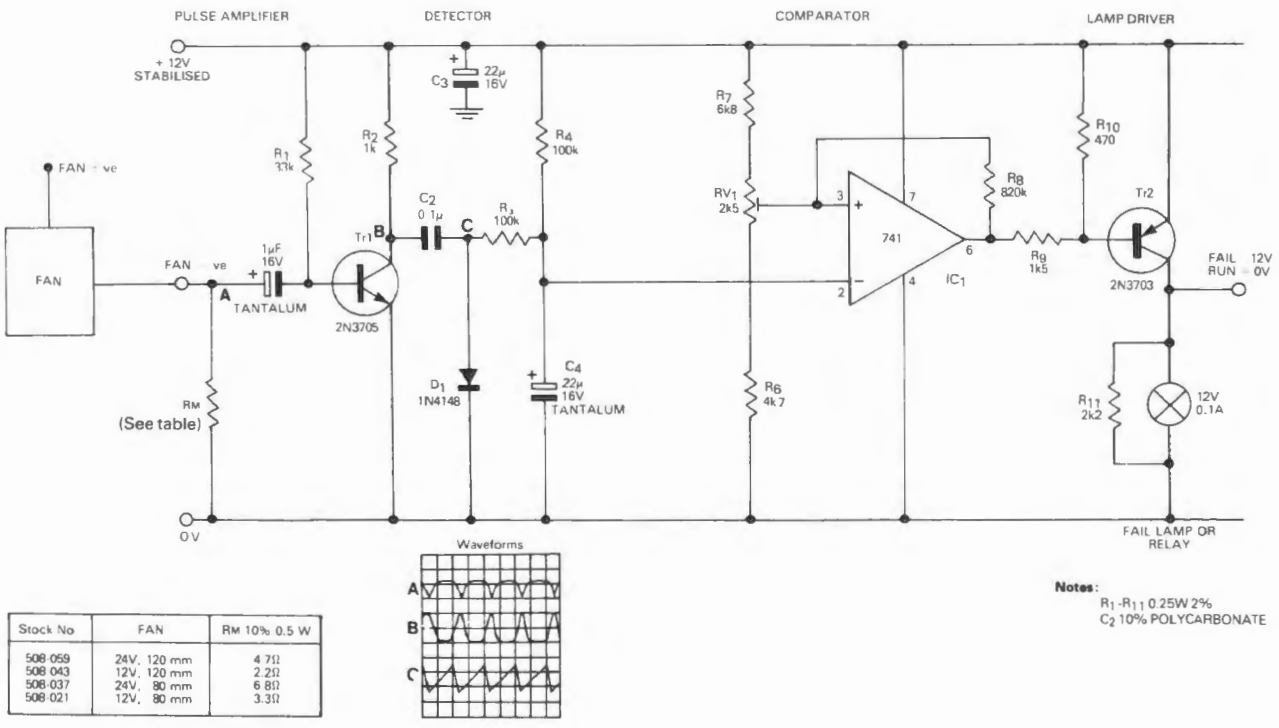
A pulse amplifier and detector across a series resistor can be used to drive a fault lamp or relay. (See Figure 14).

A voltage proportional to the fan current is picked off by the series resistor R_m and is applied to the pulse amplification stage. This stage, which is normally saturated is held 'on' by R_1. The notch pulses turn off the transistor and a limited narrow pulse is developed across R_2. At the end of each pulse the transistor turns on and connects the now charged capacitor C_2 across D_1. The result is an exponentially decaying voltage with a mean value directly proportional to fan speed. This is integrated by R_3 and C_4 to produce a ripple-free dc voltage which forms one input to a voltage comparator. The comparator compares the output of the detector(s) with the reference voltage set by RV_1 and IC_1 output switches should an out of limits condition occur. TR_2 provides a higher current switched output should this be needed in a particular application.

Fan assisted heatsink cooling

Considerable cost savings on semiconductor components can be achieved by using a suitable heatsink designed for fan cooling such as the RS heatsink 402-383. Higher power output and improved performance are a direct result of fan assisted cooling. (See Data Sheet 4484, Encapsulated thyristor and diode packs.)

Figure 14 **dc fan failure monitor circuit**

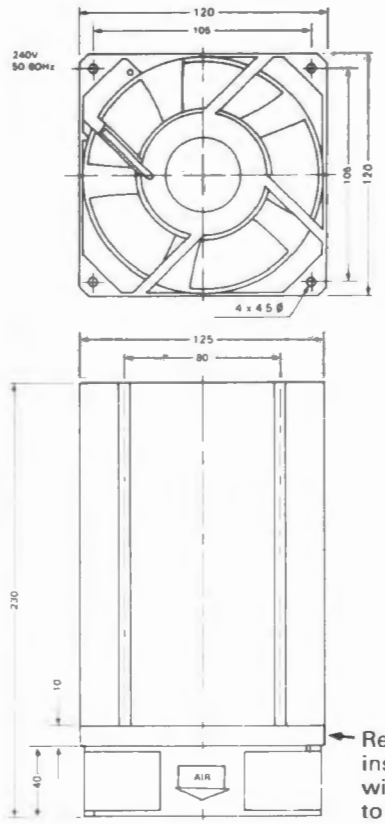


Stock No	FAN	RM 10% 0.5 W
508-059	24V, 120 mm	4.7Ω
508-043	12V, 120 mm	2.2Ω
508-037	24V, 80 mm	6.8Ω
508-021	12V, 80 mm	3.3Ω

Notes:
R_1-R_{11} 0.25W 2%
C_2 10% POLYCARBONATE

Figure 15 **Heatsink with 120mm axial fan**

To obtain correct cooling, 3 aluminium sheets 180 × 100 × 2mm must be inserted into the slots provided, to close off the fins and ensure proper air-flow. Also a 10mm spacer should be used between fan and heatsink to isolate the fan from the heat source.



ac cross flow fan

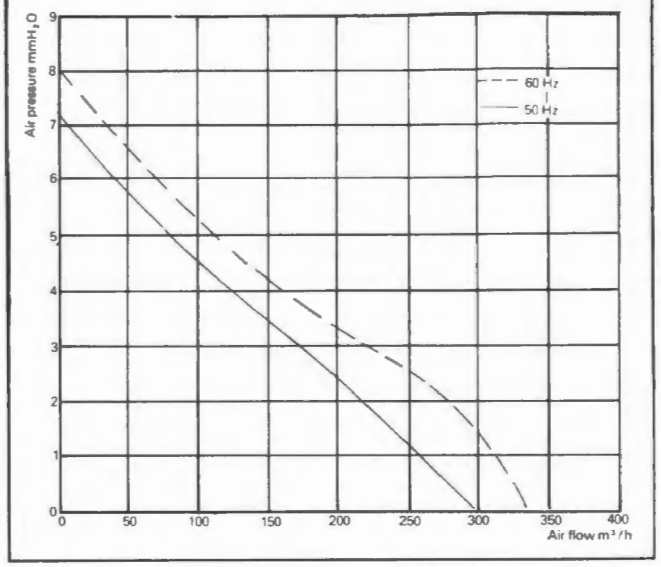
A powerful but compact cross-flow (tangential) fan or blower in accordance with DIN 41494 for 19in racking systems. Designed for air to be pulled into a system through a filter, then rotated upwards through 90°C passing through the component racks then discharged at the top.

Specification V_S = 240V, f = 50Hz

Supply voltage	240V
Voltage range	±10%
Frequency range	50/60Hz
Air flow	300m³/h
Power consumption	35W
Running current	150mA
Stall current	260mA
Speed	2650 rpm
Built-in capacitor	1μF
Noise level	54dB(A)
Temperature range	–25 to +70°C
Life expectancy	30,000 hrs
Termination	terminal block
Finish	zinc galvanised steel
Grille finish	black anodized aluminium
Impeller dimensions	380 × 65mm

Operating characteristics (Filter fitted)

Figure 16 **Operating characteristics (filter fitted)**



Features

- High efficiency
- Standard 19in rack fitting
- Equal air distribution over 380 × 60mm outlet
- Long life
- Attractive black anodized grille
- Fitted with ball bearings

Accessories

The fan is supplied complete with filter and grille. The fan is designed to work at peak efficiency with the filter fitted, and should not be run without. Replacement filters in packs of 3 are available (Stock No. 507-652). Filtration efficiency at 5μ is 55% to BS2831, when clean. Instructions for assembling and changing the filter are supplied with the fan. Filter size 390 × 85mm.

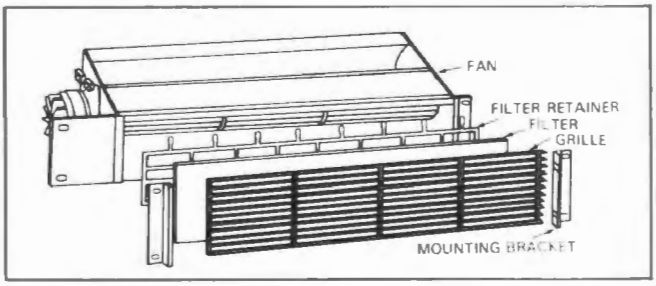


Figure 17 **Typical mounting configurations**

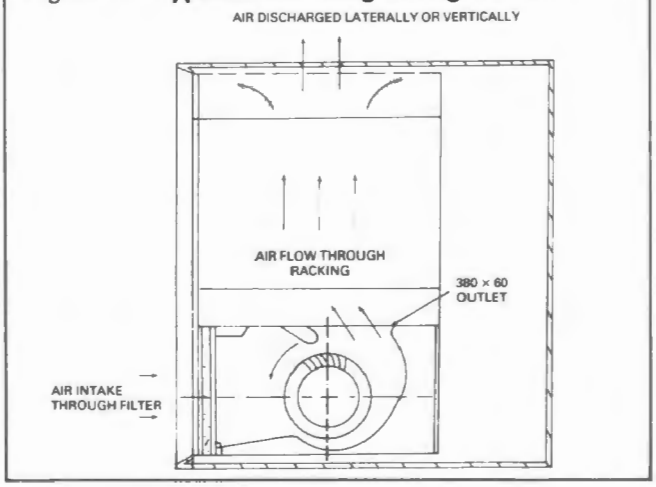
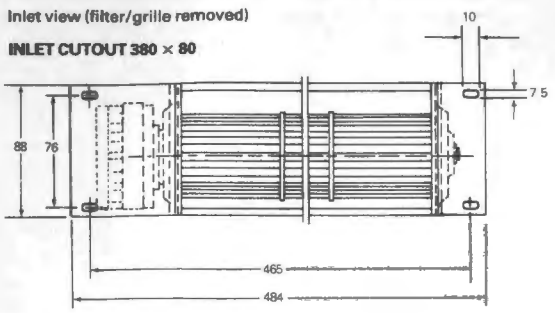
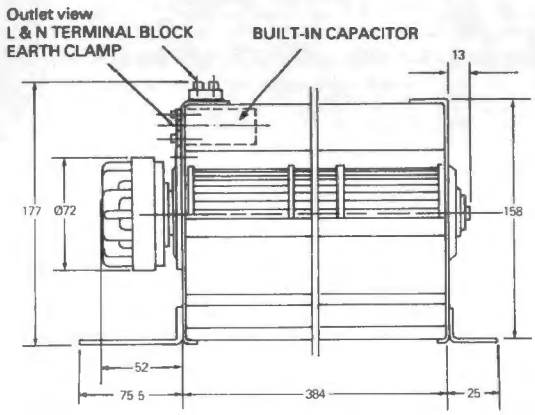


Figure 18 **Major dimensions**





Fan comparison charts Performance (ac fans quoted at 50Hz)

size mm	type	stock no.	nominal voltage V	voltage range	air flow m³/h	power W	running current mA	stall current mA	acoustic noise dB(A)	speed rpm	temp. range °C	life* (typ) × 10³ hrs
62	dc slimline axial	501-913	12	±25%	40	3	250	100	40	5300	–10/65	25
		501-929	24	±25%	40	3	125	50	40	5300	–10/65	25
	dc ultraslim axial	501-907	5	±25%	20	1.3	250	250	32	3400	–20/55	15
		501-890	12	±25%	20	1.3	110	110	32	3400	–20/55	15
		501-884	24	±25%	20	1.1	45	45	32	3400	–20/55	15
80	ac standard axial	509-046	110	±10%	46	12	115	210	34	2650	–10/70	15
		509-030	240	±10%	46	12	70	100	34	2650	–10/70	15
	dc axial	508-021	12	9.5/14	60	3	240	35‡	38	3300	–30/70	20
		508-037	24	19/28	60	3	120	35‡	38	3300	–30/70	20
120	ac standard axial	509-068	110	±10%	160	23	240	375	44	2650	–10/50	15
		509-226	240	±10%	160	23	120	130	44	2650	–10/50	15
	ac low noise axial	507-400	110	±10%	82	11.5	120	150	29	1450	–10/60	30
		507-393	240	±10%	82	11.5	60	75	29	1450	–10/60	30
	ac slimline axial	507-236	115	±10%	108	13	135	200	41	2500	–10/55	25
		507-220	240	±10%	108	15	80	100	44	2500	–10/55	25
	dc axial	508-043	12	9.5/14	160	5	400	35‡	47	2800	–30/70	20
		508-059	24	19/28	160	5	200	25‡	47	2800	–30/70	20
160	ac axial	508-065	110	±10%	350	40	500	750	49	2760	–30/65	20
		508-071	240	±10%	350	40	250	400	49	2750	–30/65	20
19in	ac rack	508-576	240	±10%	300	35	150	260	54	2650	–25/70	30

Physical properties

size mm	type	stock no.	weight kg	power lead type	panel cut-out mm	mtg holes mm	FC mm
62	dc slimline axial	501-913	0.80	B	57 dia†	4 × 3.7	50 × 50 (70 PCD)
		501-929	0.80	B			
	dc ultraslim axial	501-907	0.45	C	57 dia†		
		501-890	0.45	C			
		501-884	0.45	C			
80	ac standard axial	509-046	0.42	A	76 dia.	4 × 4.5	71.5 × 71.5 (101 PCD)
		509-030					
	dc axial	508-021	0.52		76 dia. †		
		508-037					
120	ac standard axial	509-068	0.60	C	116 dia.	4 × 4.5	105 × 105 (145 PCD)
		509-226					
	ac low noise axial	507-400	0.79				
		507-393					
	ac slimline axial	507-236	0.465				
		507-220					
	dc axial	508-043	0.55		116 dia. †		
		508-059					
160	ac standard axial	508-065	1.2	A	144 dia.	2 × 4.5	162
		508-071					
19in	ac rack	508-576	1.6	D	80 x 380	4 × 6.0	76 × 465

Notes. †Fan efficiency can be improved by shaping the cut-out to fit the exact dimensions of the fan venturi outlet or inlet.
‡Cut-out protects against full stall current. *Over full temperature range at nominal voltage.
A = flying leads. 300mm long. B = flying leads. 310mm long. C = solderable 110 spade terminals accepting RS plug and socket 507-450.
D = terminal block fitted: no lead supplied.

RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

Servo control module

Stock number 591-663

The RS servo control module is designed to power the 12V d.c. precision motor (Stock number 336-292) and gearbox combination in either positional or velocity control modes.

The unit is designed for incorporation into equipment and is capable of being mounted on a 10E 3U-height Eurocard for system applications.

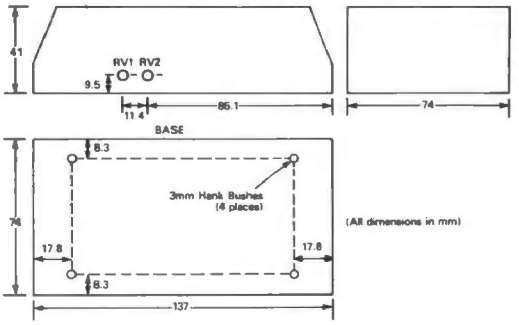
Features

- 100-120V or 200-240V a.c. 50/60Hz operation
- Adjustable output current limit
- ±5.1V short circuit protected references
- Adjustable positive feedback for armature resistance compensation (negative output resistance)
- Velocity or positional control
- Adjustable scaling between control potentiometer rotation and motor rotation.

Ratings

Mains supply frequency range _____ 50 to 60Hz
Mains supply voltage range (110V) 100 to 120V a.c.
(220V) 200 to 240V a.c.
Ambient temperature range _____ 0 to +50°C
a.c. supply loading (full load) _____ 18VA (typ.)

Module dimensions and mounting details



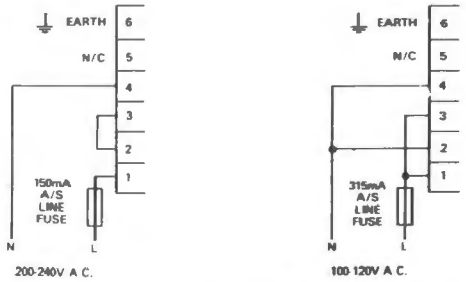
Electrical characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
Motor driver section					
Output voltage				±12	V d.c.
Output current	(Adjustable via external resistor)	0.03		0.38	A
Voltage gain	Less positive feedback effect	2.85	3	3.15	
Input offset voltage				40	mV
Input bias current				250	μA
Negative output resistance	(Adjustable via RV2)	−3		−20	Ω
Reference supply section					
Positive reference voltage (V_{ref})		4.7	5.1	5.5	V d.c.
Negative reference voltage ($-V_{ref}$)		within ±0.15V of positive ref. voltage			V d.c.
Output current	(Short circuit protected)			7.5	mA
Preamplifier section					
Output voltage			±4		V d.c.
Voltage gain	(adjustable by RV1)	15		140	
Input offset voltage				25	mV
Input offset current				200	nA
Input bias current				500	nA
Common mode range	Pin 8 open circuit		±12		V
Common mode rejection	Pin 8 open circuit		50		dB

Supply connections & fusing

The servo control module is capable of operation from 200-240V or 100-120V a.c. 50/60Hz supplies. The connection diagram for 200-240V operation is shown on the label fixed to the unit and is reproduced below, together with the revised connections required for 100-120V operation.

Figure 1



IMPORTANT: THE UNIT MUST BE EARTHED. INCORRECT SUPPLY CONNECTION WILL RESULT IN UNIT DAMAGE.

Motor & gearbox considerations

Reference has been made to Data Sheet 4226 'Precision D.C. Motors, Gearboxes and Servo Mounting Kit' for relevant characteristics and motor equations.

Two factors govern the maximum current which a motor/gearbox combination can sustain without damage.

1) Motor armature temperature
2) Gearbox torque limit

1) Motor armature temperature

The maximum armature temperature for the RS 12V precision motor (336-292) is 100°C

Now $R_{m(T)} = R_{m(22)}\,(1 + \alpha\,[T - 22])$ **Eqtn. 1**

where $R_{m(T)}$ = armature resistance in ohms at temperature T°C

and α = temperature coefficient of resistance of winding copper = 0.004/°C

$R_{m(22)} = 20.8\Omega \pm 8\% = 22.5\Omega$ max

$\therefore\ R_{m(100)} = 22.5\,(1 + 78 \times 0.004) = 29.5\Omega$ max

Thermal resistance armature to ambient = 35°C/watt = θ_{ra}

but $P_D = I^2\,R_{m(T)}$ or $I = \sqrt{\dfrac{P_D}{R_{m(T)}}}$ **Eqtn. 2**

and $P_D = \dfrac{\Delta T}{\theta_{ra}}$ or $I = \sqrt{\dfrac{\Delta T}{\theta_{ra}\,R_{m(T)}}}$ **Eqtn. 3**

$\therefore\ I = \sqrt{\dfrac{100\text{-}22}{35 \times 29.5}} = 0.275\text{A}$ max at 22°C ambient

i.e. max. motor current at 22°C ambient = 0.275A

Now the maximum output current delivered to the motor from the servo control module can be limited by an external resistor R_{CL} connected between terminal 10 & 12 (See figures 1 and 2).

$$R_{CL} \simeq \frac{40\text{-}105.I_{max}}{50.I_{max} - 1.45} \qquad \textbf{Eqtn. 4}$$

and $$I_{max} \simeq \frac{40 + 1.45.R_{CL}}{105 + 50.R_{CL}}$$

Applying the above approximate formula for I_{max} = 0.275A

$$R_{CL} \simeq \frac{40\text{-}105\,(0.275)}{50\,(0.275) - 1.45} = 0.904\Omega$$

$\therefore$ nearest preferred value for R_{CL} = $2 \times 1.8\Omega$ ½W resistors in parallel.

I_{max} can be adjusted nominally between 0.03A ($R_{CL\infty}$) and 0.38A (R_{CL} 0)

The precise value for R_{CL} in critical applications should be determined by selecting on test. The approximate formulae should be adequate for most applications. Table 1 indicates suitable values of R_{CL} for various ambient temperatures.

Table 1. Values of current limit resistance R_{CL}

Ambient Temperature °C	Max. Allowable Motor Current mA	Calculated R_{CL} Value Ω	Practical R_{CL} Value Ω
15	287	0.765	2 × 1.5 in //
25	270	0.967	2 × 0.47 in ser
35	251	1.230	1.2
45	231	1.560	1.5
55	209	2.01	2 × 1.0 in ser
65	184	2.67	2.7

2) Gearbox torque limit

When using high ratio gearboxes high, possibly damaging, torques may be developed at the output shafts. All RS ovoid gearboxes have a maximum permissible stall torque of 0.8Nm and typical efficiencies as quoted on data sheet 4226. Current limiting of the motor supply provides a convenient method of controlling output torque to the permitted maximum.

Gearboxes (5:1), (15:1), (40:1) and (160:1) will sustain continuous stall without damage at the maximum output current of the RS Servo Control Module. Higher ratio gearboxes may need a current limit lower than that calculated on the basis of rotor temperature. Table 2 shows the amended values of motor current and R_{CL}.

Table 2. Values of R_{CL} for high ratio gearboxes

RS Gearboxes	Max. Allowable Motor Current mA	Calculated R_{CL} Valve Ω	Practical R_{CL} Valve Ω
640:1	140	4.56	4.7
1250:1	70	15.9	18
2560:1	40	65.1	68

Speed control mode

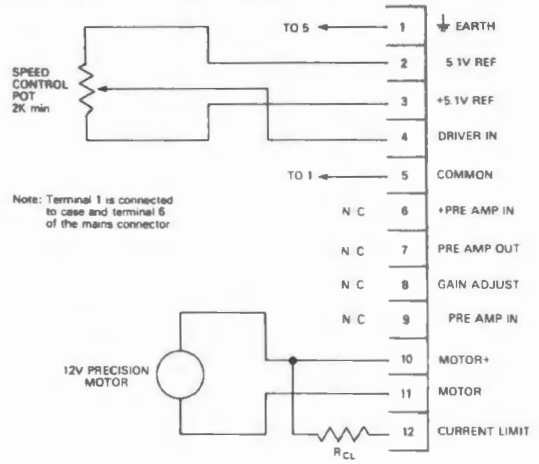
Ensure mains supply is off and make connections as Figure 2. A voltage of ±4.0V at terminal 4 with respect to terminal 5 will give ±12V at the motor to produce full speed in either direction. This can be obtained by connecting a potentiometer (minimum value 2K ohms) between +5.1V and −5.1V with wiper to terminal 4. For speed control using an externally derived voltage at terminal 4 with respect to terminal 5 problems due to 'multiple grounds' can be avoided by deleting the connection between terminals 1 and 5. In that case terminal 5 MUST be connected via the external equipment to a good safety ground.

After checking connections apply the mains supply with RV2 fully anti-clockwise. (Located on side of case and used to adjust resistance of output section.) Set the input voltage in the range 1 to 2 volts (3 to 6 volts at motor) so that the motor runs at ¼ to ½ full speed. Advance RV2 clockwise until instability of motor speed is noticed: very likely a 'ticking' will be heard from the motor at that point. Retard RV2 anti-clockwise slightly to remove the instability.

By adjusting RV2 in this way the negative output resistance of the amplifier has been made nearly equal to the positive resistance of the rotor of the motor and the voltage applied to the motor by the servo amplifier increases as the mechanical loading increases.

RV2 adjustment should be checked following a change of motor. Need for adjustment is indicated if the motor 'ticks' or if speed is unstable.

Figure 2 **Speed control connections**



Positional servo mode

Ensure mains supply is off and make connections as Figure 3. Master and slave potentiometers should be connected to the same reference supply which conveniently but not necessarily may be the ±5.1V supplies at terminals 3 and 2. Because the same reference supply is used for both potentiometers its value affects only the mechanical gain (restoring force per unit mis-alignment) of the servo and not the absolute accuracy, but note that voltage applied to pins 6 or 9 must be within the common mode range of ±12 volts.

Generally pins 5 and 1 will be connected together, but if an external reference supply is employed it may be preferable to delete the connection. In that case terminal 5 MUST be connected via the external equipment to a good safety ground.

After checking connections apply the mains supply with RV1 (located on side of case and used to adjust preamplifier gain) and RV2 both fully anti-clockwise and with the MASTER potentiometer near its mid position. The servo should stabilise with the SLAVE potentiometer also near its mid position, if not reverse the connections to the motor.

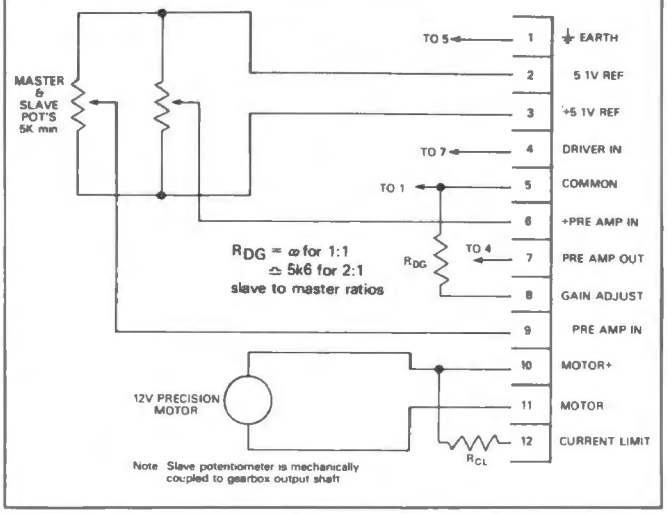
Advance RV1 clockwise until the desired response to movement of the MASTER potentiometer is obtained. With RV1 too far clockwise the SLAVE potentiometer will hunt repetitively either side of the correct position. With RV1 too far anti-clockwise the SLAVE potentiometer may be sluggish when approaching the correct position. Optimum adjustment is generally obtained when the SLAVE potentiometer overshoots the desired position and then stabilises without undershoot.

Advance RV2 clockwise to minimise the overshoot without introducing instability or 'ticking' from the motor, then back off anti-clockwise slightly.

A suitable joystick potentiometer (Stock number 162-732) is available.

RS data

Figure 3 **Positional servo connections**



Note: To prevent gearbox damage do not employ mechanical stops on gearbox output shaft.

To reverse servo rotational sense

Either reverse the reference supply connections to the MASTER potentiometer or reverse the reference supply connection to the SLAVE potentiometer and the connections to the motor.

To adjust differential gain

The user may wish the SLAVE potentiometer to travel through a smaller or larger arc than the MASTER potentiometer, e.g. RS joystick potentiometer having a sweep angle of ±25° might need to produce a larger sweep angle from the SLAVE.

The potentiometer wiper having the smaller sweep angle should be connected to terminal 9. The potentiometer wiper having the larger sweep angle should be connected to terminal 6. The reference supplies should be the ±5.1V supplies of the servo amplifier.

Before adjusting RV1 or RV2 select by experiment the resistor R_{DG} which when connected between terminals 5 and 8 gives correct sweep angle of the SLAVE. Then adjust RV1 and RV2 as described above.

To cure continuous rotation

Because the torque available from the motor is insufficient to bring the servo to rest instantaneously and because there is no true 'velocity feedback' there is generally overshoot with a correctly adjusted servo using the RS servo control module. Should the MASTER command a position of the SLAVE close to its stated 340° ±4° electrical rotations the overshoot may cause the SLAVE potentiometer wiper to become open circuit momentarily and the servo may rotate continuously.

Although the effect depends in a complex manner upon friction, gear ratio, moment of inertia of load and upon current limit, the user will normally expect to be able to achieve the SLAVE rotation angles of table 3.

Table 3. SLAVE potentiometer rotation angles

RS Gearbox	Motor Current in mA	Practical R_{CL} Valve Ω	Permissible SLAVE rotation
5:1	287	2 × 1.5 in //	±92 degrees
	184	2.7	±88 degrees
15:1	287	2 × 1.5 in //	±128 degrees
	184	2.7	±116 degrees
40:1	287	2 × 1.5 in //	±160 degrees
	184	2.7	±154 degrees
All others	Dependant on Gearbox see Table 2	See Table 2	±162 degrees

Optimum gearbox choice for positional servo

In many applications it will be required to combine the maximum possible stall torque with the greatest possible slewing rate. The RS 160:1 gearbox is recommended in most instances.

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RS data

Eye response photodiode BPW21

Stock number 303-719

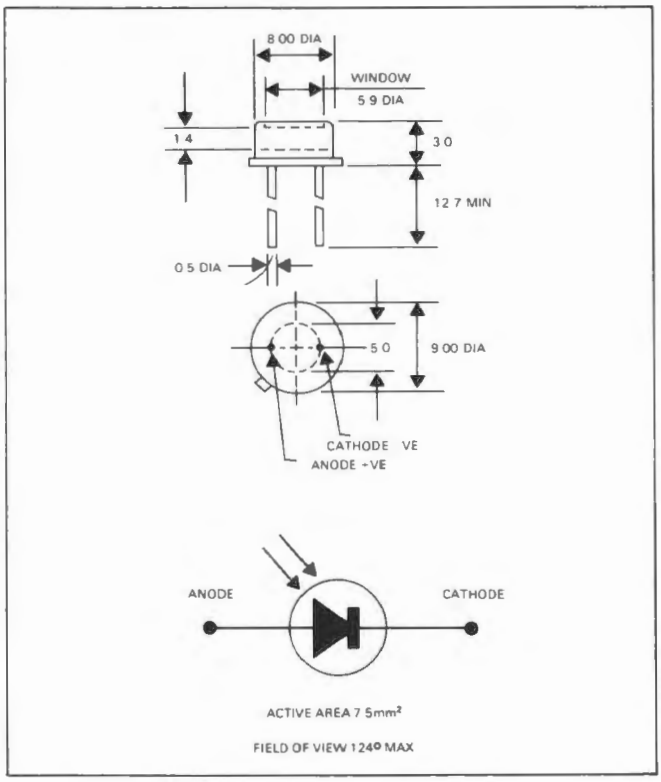
A silicon photodiode housed in an hermetically sealed case with a flat window incorporating built-in colour correction. Sensitivity approximating the human eye response. Linear current (short circuit) versus illumination. Log. voltage versus illumination. This photodiode is designed for use in the photovoltaic mode and is ideally suited for use in light monitoring and control, optical instrumentation and camera control.

Features

- Response approximating to the human eye
- Photovoltaic cell operation
- Linear output current versus illumination
- Hermetically sealed TO5 case

Absolute maximum ratings

Ambient temperature range —— −25°C to +100°C
Reverse voltage, V_R —— 10V
Open circuit voltage —— 650mV
Power dissipation (at 25°C), Pd —— 250mW
Illuminance, E —— 10^5 lux



Electrical characteristics at 25°C

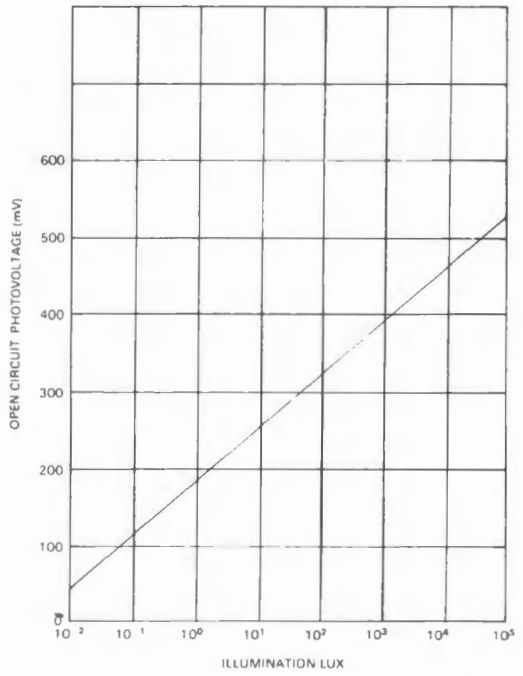
* The illuminance indicated refers to unfiltered radiation of a tungsten filament lamp at a colour temperature of 2856°K (standard Light A in accordance with DIN 5033 and IEC publ. 306-1).

Parameter		Conditions	Min	Typ	Max	Unit
S_k	Sensitivity (short circuit)	$R_L = 100\Omega$. $E_A = 10^{-2}$ to 10^5 lux*	4.5	7		nA/Lux
V_{ph}	Photovoltage (open circuit)	$E_A = 1$ Lux*		250	350	mV
$T_k I_{sc}$	Temp. Coeff. of short circuit current	$E_A = 1K$ Lux*		−0.05		%/°C
$T_k V_{ph}$	Temp. Coeff. of open circuit voltage	$R_L = 100\Omega$. $E_A = 1K$ Lux*		−2		mV/°C
λ_p	Peak wavelength sensitivity			560		nm
	Spectral bandwidth	50% sensitivity upper limit		680		nm
		50% sensitivity lower limit		440		nm
	Junction capacitance	$V_R = 0V$		490		pF
t_r	Rise time	$R_L = 1K\Omega$. $V_R = 5V$		1.0		µS
I_D	Dark current	$R_L = 1K\Omega$. $V_R = 5V$		2	30	nA
NEP	Noise equivalent power	$V_R = 5V$		1.4×10^{-5}		Lux/√Hz

RS data

Typical characteristics

Figure 1 **Photovoltage vs illumination**



(for standard illuminant A, 1000 Lux = 4.75 mW/cm²)

Figure 2 **Photocurrent vs illumination**

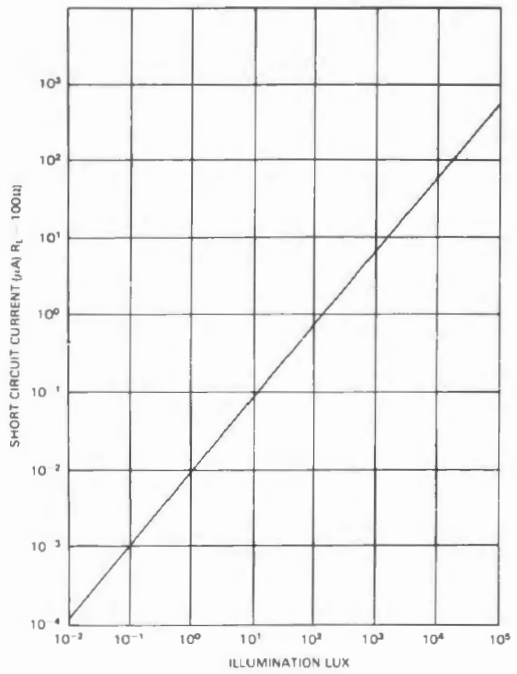
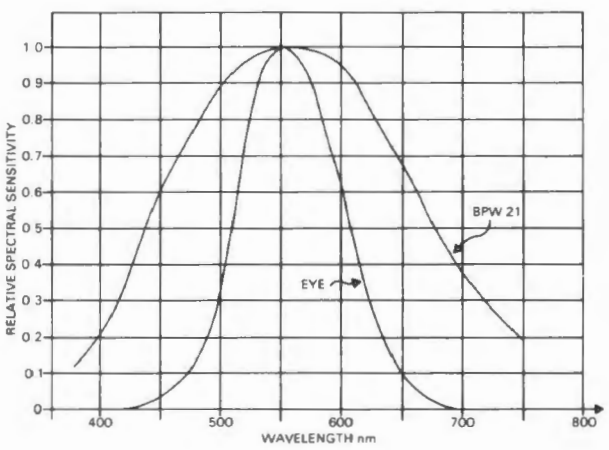
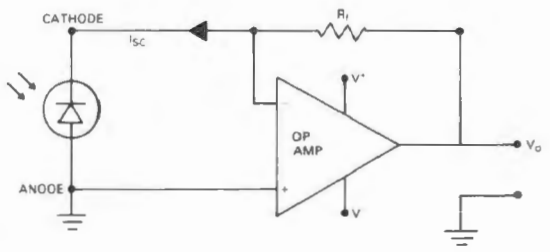


Figure 3 **BPW21 and human eye spectral sensitivity**



Typical photovoltaic connection

Figure 4



$V_O = R_f . I_{SC}$
$I_{SC} = E_V . S_k$
$V_O = R_f . E_V . S_k$

where
V_O = signal output voltage. V
R_f = feedback resistance. Ω
I_{SC} = Photodiode short circuit current. A
E_V = insident illumination. Lux
S_k = Photodiode sensitivity. A/Lux

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RS data

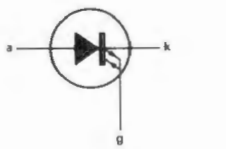
Gate turn-off thyristor BTW58-1300R

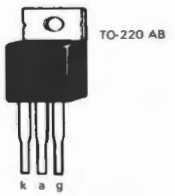
Stock number 262-753

The gate turn-off switch (G.T.O.) combines the high current, high blocking voltage characteristics of a conventional thyristor with the fast and ease-of-driving characteristics of a transistor or darlington. The result is a fast and very effective solid state switch. The switch latches 'ON' when a positive supply is applied to its gate (1.5V, 100mA, for $<10\mu s$) and is turned 'OFF' when a negative supply is applied ($-5V$ for $1\mu s$) with respect to the cathode. Because the G.T.O. switch is a member of the thyristor family, overvoltage transients tend to switch it harmlessly into conduction rather than punching through insulating layers. Consequently, the G.T.O. has a much higher overload capability than a transistor and can be protected by a fuse.

Features

- Capability of turning 'ON' and 'OFF' via the gate
- Blocking voltage of 1500V max
- Low drive power
- High current capability
- Fast turn-off time
- TO-200 AB package





Note: The exposed metal mounting base is directly connected to the anode.

Absolute maximum ratings

Repetitive peak off-state voltage (1)	V_{DRM} 1300V
Continuous off-state voltage (1)	V_D 750V
Max RMS ON-state current	$I_{T(RMS)}$ 7.5A
Max average ON-state current	$I_{T(AV)}$ 6.5A
Max controllable anode current	I_{TCRM} 25A
Max fall time	t_f 250 ns
Storage temperature range	T_{stg} −40 to +150°C
Maximum junction temperature	T_j 120°C

Electrical characteristics

T_j = 120°C unless otherwise stated

Note 1: Measured with gate and cathode connected together.

Parameter	Conditions	Symbol	Max	Units
ANODE TO CATHODE				
Transient OFF-State Voltage	(1)	V_{DSM}	1500	V
Repetitive peak OFF-State Voltage	(1)	V_{DRM}	1300	V
Working OFF-State Voltage	(1)	V_{DW}	1200	V
Continuous OFF-State Voltage	(1)	V_D	750	V
Average ON-State Current	t=20ms	$I_{T(AV)}$	6.5	A
RMS ON-State Current		$I_{T(RMS)}$	7.5	A
Controllable anode current		I_{TCRM}	25	A
Non-repetitive peak ON Current	t=10ms	I_{TSM}	50	A
i^2t	t=10ms	i^2t	12.5	A^2s
Total dissipation	T_{mb} = 25°C	P_{tot}	65	W
GATE TO CATHODE				
Repetitive peak ON-state current				
g-c forward	t=10ms	I_{GFM}	25	A
g-c reverse	t=20μs	I_{GRM}	25	A
Average power dissipation		$P_{G(AV)}$	2.5	W
Thermal Resistance:				
Junction/mountbase		$R_{thj\text{-}mb}$	1.5	°C/W
Mountbase/heatsink (with heatsink compound)		$R_{thmb\text{-}h}$	0.3	°C/W

Secondary characteristics $T_j = 120°C$ unless otherwise stated

Parameter	Conditions	Symbol	Min	Max	Units
ANODE TO CATHODE					
ON-state voltage	$I_T = 5A$, $I_G = 0.2A$	V_T	-	3.0	V
Rate of rise of OFF-state voltage that will not trigger any OFF-state device: exponential method	VD = 2/3 $V_D$max; $V_{GR} = 5V$	dV_D/dt	-	10	kV/μs
Rate of rise of OFF-state voltage that will not trigger device after conduction: linear method	$I_T = 5A$, $V_D = V_D$ max, $V_{GR} = 10V$	dV_D/dt	-	1.0	kV/μs
OFF-state current	$V_D = V_D$max	I_D	-	3.0	mA
Latching current (below which, device behaves like a transistor: see figure 7)	$T_j = 25°C$	I_L	-	1.5	A
GATE TO CATHODE					
Gate turn-off voltage	(see figure 17)	V_{GR}	-3	-10	V
Trigger voltage	$V_D = 12V$, $T_j = 25°C$	V_{GT}	1.5	-	V
Trigger current	$V_D = 12V$, $T_j = 25°C$	I_{GT}	200	-	mA
Max reverse leakage current	$V_{GRM} = 10V$	I_{GRM}	-	1.0	mA
SWITCHING CHARACTERISTICS					
Turn on when switched to $I_T = 5A$ from $V_D = 250V$	$I_{GF} = 500mA$				
Delay		t_d	-	0.25	μs
Rise		t_r	-	1.0	μs
Turn off when switched to $V_D = 250V$ from $I_T = 5A$	$V_{GG} = -10V$, $L_G = 0.8\mu H$				
Storage		t_s	-	0.5	μs
Fall		t_f	-	0.25	μs

Switching characteristics test circuit and waveform

Figure 1 **Waveform**

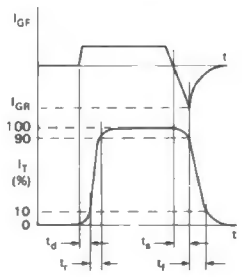


Figure 2 **Test circuit**

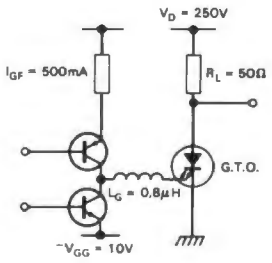
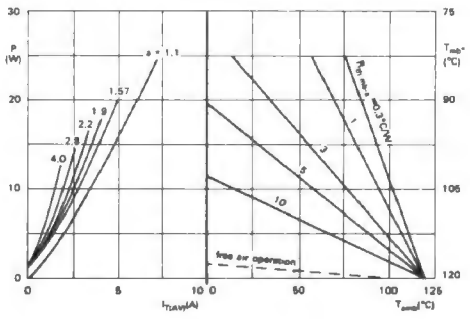


Figure 3 **The right hand part shows the interrelationship between the power (derived from the left hand part) and the maximum permissible temperatures**



$$a = \text{form factor} = \frac{I_{T(RMS)}}{I_{T(AV)}}$$

* T_{mb} scale is for comparison purposes and is correct only for $R_{th\ mb-a} < 9.6°C/W$

Figure 4 **Minimum gate voltage that will trigger all devices as a function of junction temperature**

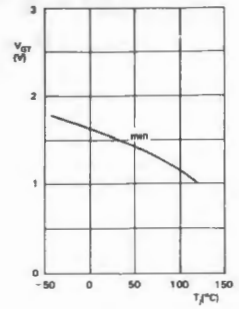


Figure 5 **Minimum gate current that will trigger all devices as a function of junction temperature**

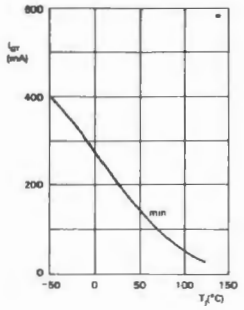


Figure 6 **Maximum V_T versus I_T**

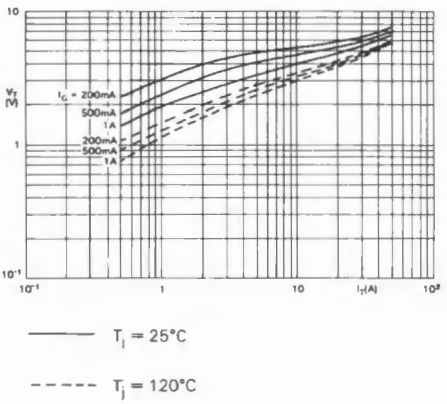


Figure 7 **Typical latching behaviour**

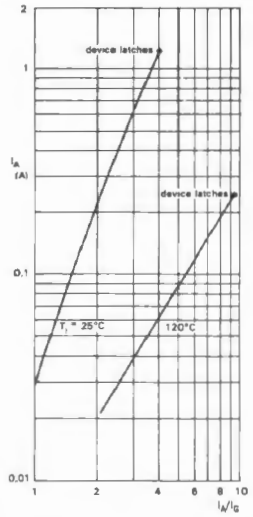


Figure 8 **Reverse gate current, storage time and fall time versus series gate resistance**

resistive load: I_T = 5A; V_{GR} = 10V; T_{mb} = 25°C. Maximum values

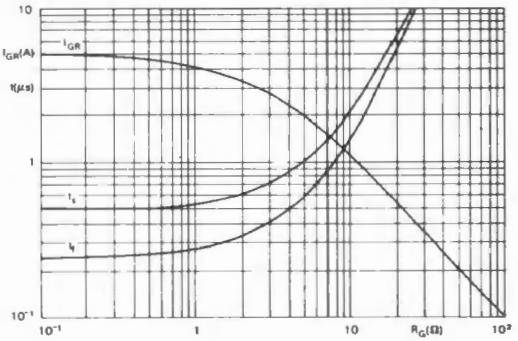


Figure 9 **Delay time, rise time, storage time and fall times as a function of temperature**

resistive load: I_T = 5A; V_{GR} = 10V; R_G = 0Ω; L_G = 0.8μH. Maximum values

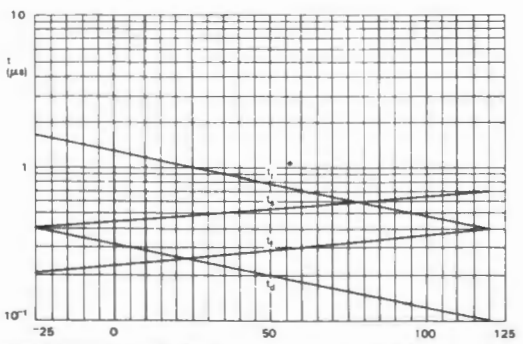
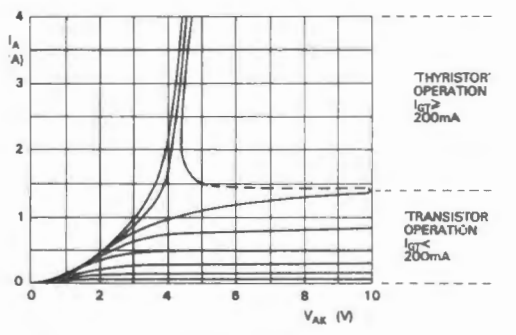


Figure 10 **ON-state current as a function of ON-stage voltage**

with gate current as a parameter for the GTO



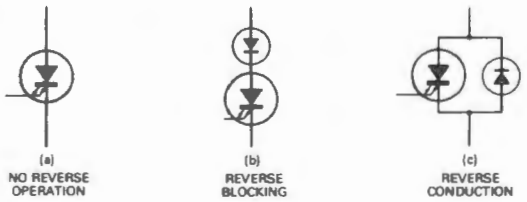
Forward characteristics of the GTO

Figure 10 continues the thyristor/transistor analogy for the GTO by showing that, when the anode current is less than the latching current I_L, the GTO behaves like high-voltage transistor with a gate to anode current amplification factor I_A/I_G which increases with increasing anode current as shown in Figure 7. If the gate current is less than that required for triggering (I_{GT}), the GTO is in the off-state with a low leakage current flowing between the anode and cathode. If the gate current is greater than, or equal to I_{GT}, the GTO is in the on-state with a small potential difference between anode and cathode. As long as the anode current remains below the latching level however, the GTO may return to the off state if the gate current falls below I_{GT}. If the anode current is greater than the latching level, the GTO, like a thyristor, will remain latched in the on-state, even if the flow of gate current ceases. Unlike the thyristor however, the GTO can be turned off again by reversing the polarity of the gate drive voltage.

Reverse characteristics of the GTO

The reverse characteristic of the GTO is equivalent to that of a resistance which is incapable of blocking voltage or conducting significant current. For d.c. switching, this does not present any problems. If reverse voltage blocking is required for a.c. switching, a diode must be connected in series with the GTO as shown in Figure 11. If reverse current must be allowed to flow, a diode must be connected in anti-parallel with the GTO. An 800V 6A minimum $I_{T(AV)}$ diode should be used. See current catalogue for suitable device.

Figure 11 **Changing the reverse characteristics of a GTO circuit with additional diodes**



Turn-on behaviour

Precautions during pulse or capacitor discharge drive

During turn-on, care should be taken to ensure that adequate gate current is available whenever the anode current is likely to be less than the latching level. For example, Figure 12 shows that, if turn-on is achieved by discharging a capacitor into the gate of a GTO with an inductive load, too brief a time-constant may cause the gate-current to fall below I_{GT} before sufficient time has elapsed for the anode current to rise above the latching level. This could cause uncertain triggering. Uncertain triggering could also be caused by some types of anode load which vary considerably both during switch-on and during idling.

It has also been observed that, if the anode current is only slightly higher than the latching level, a steep trailing edge of a positive gate pulse may cause the GTO to unlatch as shown in Figure 13. The fall time of the gate drive pulses should therefore be prolonged.

The disadvantage of having to take the foregoing precautions during turn-on is far outweighed by the triggering sensitivity of the GTO (I_{GT} min. = 200 mA).

Figure 12 **To ensure good triggering**
the anode current must rise above the latching level before the gate current falls below the minimum level required to ensure triggering

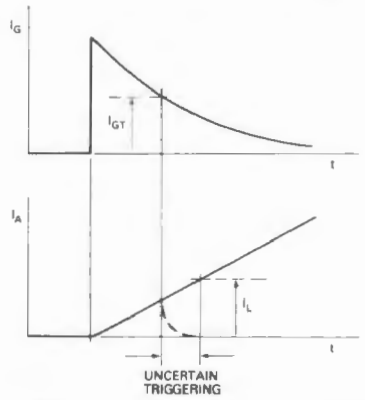
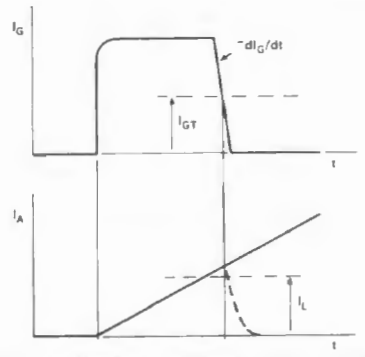


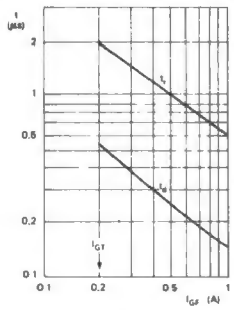
Figure 13 **Unlatching can occur**
if the anode current is only slightly higher than the latching level during a rapid positive to negative transition of the gate current



Minimizing switching losses

To minimize losses during fast switching, it is essential to minimize the turn-on time of the GTO. As shown in Figure 14, both components of the turn-on time (delay time t_d and rise time t_r) reduce with increasing forward gate current. The ideal waveform for the gate drive circuit is shown in Figure 1 where it rapidly rises to a level much higher than the minimum value required to ensure triggering (I_{GT}), and does not reduce to I_{GT} until the anode current has stabilized at a value much higher than the latching level (I_L). In conventional thyristors, a rapidly rising anode current would cause a high level of localized dissipation in the crystal during turn-on. The interdigitated construction of the GTO gate increases its ability to withstand the stresses caused by fast turn-on.

Figure 14 **Components of the turn-on time as functions of forward gate current**



Advantages of d.c. gate drive

Like a transistor, the GTO can also be turned-on by applying a direct gate current of greater than I_{GT}. As shown in Figure 6, this mode of operation has the additional advantage of reducing the voltage drop across the GTO whilst it is conducting, even if the anode current is very much higher than the latching level.

Turn-off behaviour

To understand the turn-off process, it is helpful to have some understanding of the solid-state conduction through the GTO crystal. Figure 15 shows a cross-section through the crystal whilst conduction is taking place between the anode and the cathode. During this on-state, the central region of the crystal is filled with a hole-electron plasma which enables the GTO to conduct a high current with very little potential difference between anode and cathode. To turn-off the GTO this plasma must be interrupted by applying a negative voltage bias to the gate. This causes the plasma to be squeezed to a narrow filament as shown in Figure 16. The period up to the breaking of the plasma filament is the storage phase of the turn-off time. For it to be short, a reasonably strong voltage (−5V to −10V) should be applied between the gate and the cathode. The gate region is so designed that it can withstand short periods (~20μs) of operation whilst in reverse avalanche breakdown. The application of a reverse bias voltage which exceeds the reverse breakdown level does not however further assist the turn-off process. The relationship between applied reverse gate voltage and the two components of the turn-off delay of a GTO is shown in Figure 17.

Figure 15 **Cross-section of the GTO crystal**
during the start of turn-off (storage time t_s) when gate current extraction commences

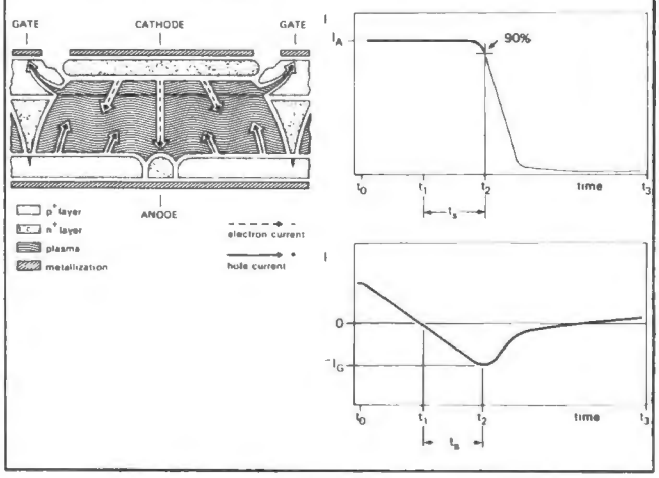
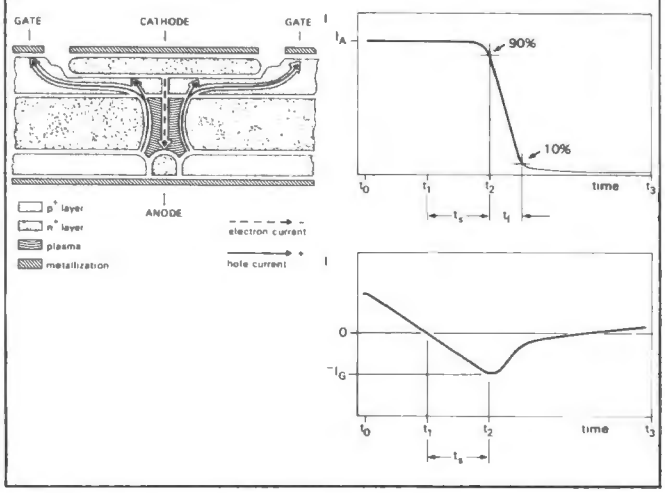
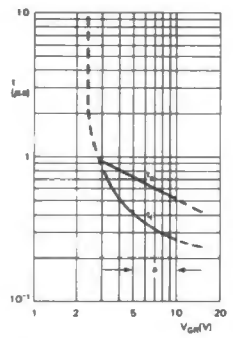


Figure 16 **Cross-section of the GTO crystal**
during the next phase of turn-off which is the fall time t_f during which the conduction is squeezed into a narrow filament which finally breaks



When the plasma filament shown in Figure 16 is broken, the anode current falls and the anode voltage rises at a rate dependent on the load. The anode current fall-time depends on the current extracted from the gate as shown in Figure 8. For example, if an anode current of 5A is switched off by extracting 1A of gate current, the storage and fall times may be as long as 2.5μs and 2μs respectively. Alternatively, if 5A is extracted from the gate to switch off the same 5A load, the storage and fall times are reduced to 0.5μs and 0.25μs respectively. The ability to withstand the high peak level of reverse gate current which is necessary to ensure fast turn-off is ensured by using a shorted anode structure and a low-impedance base region beneath the cathode. These features are made possible by careful control of the diffusion. Localised hot-spots during turn-off are prevented by using long, narrow cathode fingers (interdigitated construction).

Figure 17 **The influence of negative gate voltage** on the two components of the turn-off time



As shown by Figure 18, the final stage of turn-off consists of a small tail of anode current due to charge trapped in the remoter regions of the crystal. Gold doping has been used to ensure that this charge rapidly recombines so that it does not normally have any appreciable influence on the turn-off dissipation.

Maximum controllable anode current

Although the GTO crystal is quite small, it is capable of conducting and switching-off currents well in excess of its average anode current rating. For example, the 6.5A 262-618 can switch off 25A pulses of anode current. The only condition is that the rate of rise of the voltage between anode and cathode must be limited as shown in Figure 20 for inductive loads. The higher the current that must be switched off, the lower the allowable dV/dt. Figure 20 shows that, as might be expected, for a given dV/dt, the level of current that can be switched off increases with increasing negative bias applied to the gate. In applications where Figure 20 indicates that a slow rise circuit is required, one of the two circuits shown in Figure 19 can be used. Figure 19a is suitable for use in circuits with a single GTO controlling load currents up to 25A. Figure 19b is for GTO bridge circuits for controlling load currents up to 6A.

Safe operating area (SOAR)

Since the GTO is a switch with two stable states, it cannot remain in a quasi-saturated condition during turn-on or turn-off. There is not therefore a SOAR limitation while the GTO is forward biased. The SOAR for a reverse biased GTO is a simple rectangle as shown in Figure 21.

Drive circuits

The GTO operates with very short switching times for both turn-on and turn-off, less than 0.5μs for the 262-618. However, to achieve this performance in practice, it is essential that the device is driven correctly. Figure 22 shows the basic method of drive.

To turn the GTO on, a positive current must be injected into the gate for the duration of the time necessary for turn-on. This continuous drive reduces the forward voltage drop at low anode currents (below about 2A for 262-618) and thus minimises losses.

Turn-off is achieved by drawing from the gate a current pulse of between 20 and 100% of the anode current for a few hundred nanoseconds. This is done by applying a negative voltage of between −5 and −10V directly between gate and cathode.

If the impedance of the gate turn-off circuit is sufficiently low, unity turn-off gain is achieved. Under these conditions, all the anode current is diverted into the gate, turning off the cathode before the anode voltage has started to rise. With unity turn-off gain, the slow-rise circuit indicated in Figure 22 is not required and circuit dissipation is reduced.

Figure 18 **Cross-section of the GTO crystal** during the final phase of turn-off (tail time) during which a depletion layer is formed and the charge recombines in the remote n-base

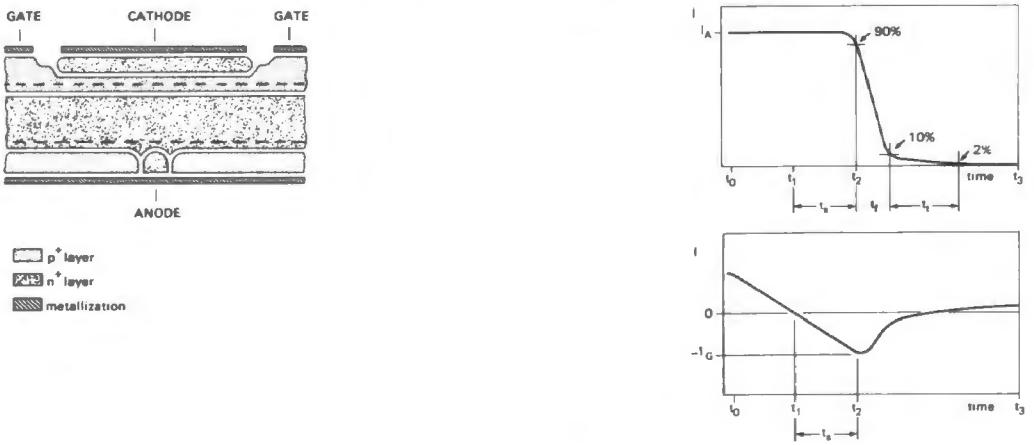


Figure 19 **Slow rise circuits**

$C_s = I_{TC}/(dV/dt)$
where C is in μF, I_{TC} is in A and rise time is in V/μS

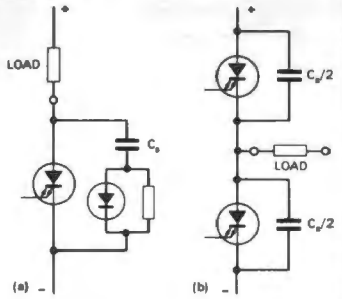


Figure 22 **Basic drive circuit**

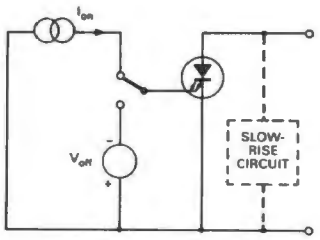
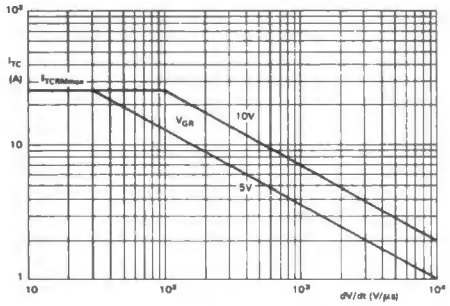


Figure 20 **Permitted anode voltage rise time**
as a function of controllable anode current with reverse bias voltage on the gate as a parameter



Two practical drive circuits for the GTO based on the turn-off circuit in Figure 22 are shown in Figures 23 and 24. In both the negative turn-off voltage is switched from a capacitor charged during the on-time of GTO to a level set by a voltage regulator diode.

Figure 23 shows a simple direct gate-drive circuit. With TR_2 turned off, positive gate drive current flows from the d.c. supply rail to the GTO via the emitter follower TR_1. When TR_2 is turned on, TR_1 turns off and a negative voltage of about 10V, set by D_2, is applied to the gate of the GTO. As long as TR_2 is on, the gate voltage will remain negative because the reverse gate resistance of the GTO in the non-conducting state is high and C_1 will therefore only discharge slowly. A GTO anode current of up to about 10A can be turned off with this circuit; for lower currents, a lower value voltage regulator diode can be used.

Figure 21 **Reverse biased SOAR**

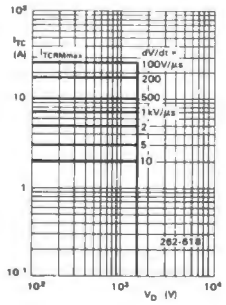
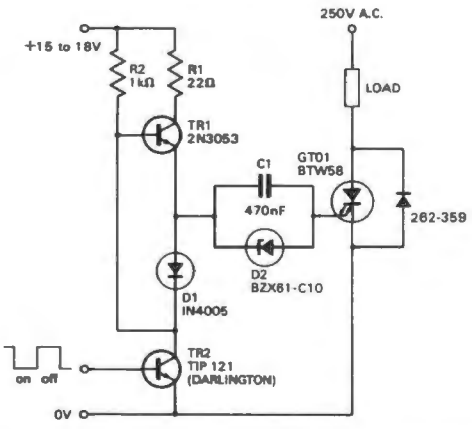


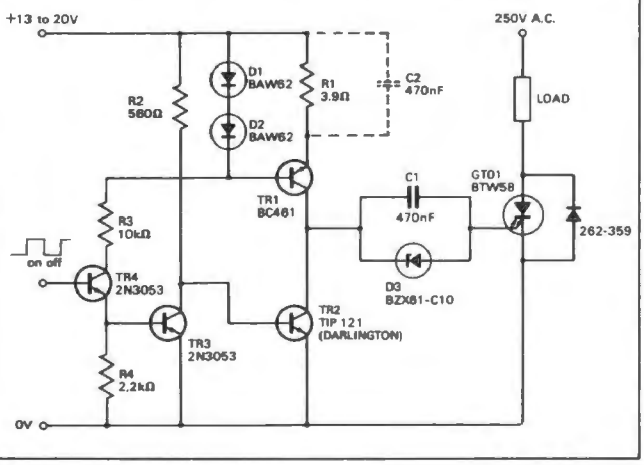
Figure 23 **Simple direct gate drive circuit**



The main drawback of this simple circuit is that the positive turn-on current is dependent on the supply voltage. A modified circuit in which this dependency is reduced is shown in Figure 24. In this circuit, TR_1 is a current source which gives the required positive gate drive. Diode D_1 in Figure 23 is now omitted and consequently the impedance in the negative gate path is reduced, making the circuit better suited to operation with unity turn-off gain.

If the anode di/dt is high, capacitor C_2 should be included to ensure that the initial gate current is large hence reducing turn-on loss.

Figure 24 **Modified simple direct gate drive circuit**



D.C. motor control

Figure 25 shows the basic configuration for the PWM control of a d.c. motor; no commutation circuit is required. The switching frequency is chosen so that the switching period is much less than the L/R time-constant of the motor to ensure that the motor current is continuous. The slow-rise circuit may not always be needed, depending on the drive circuit used.

Figure 25 **D.C. motor chopper control**

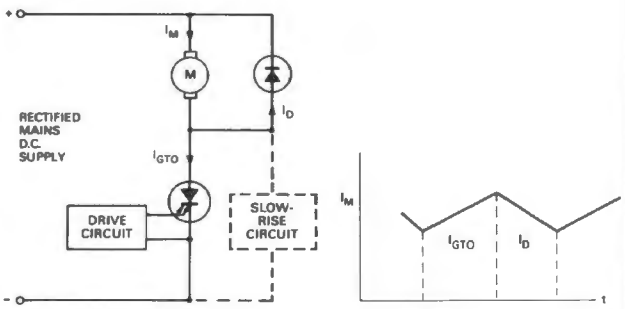
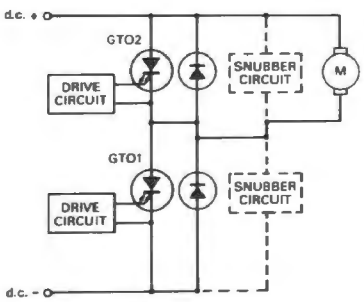


Figure 26 shows a d.c. motor controller which uses a second GTO and allows regenerative braking. When GTO2 is turned on for a short time, the back e.m.f. of the motor transfers energy into the motor inductance. When GTO2 is turned off, this energy is returned to the supply.

Figure 26 **D.C. motor chopper control with regenerative braking**



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RS data

Encapsulated thyristor and diode packs

A range of encapsulated modules, either thyristor or diode, available in two voltage ratings 800V_{RRM} and 1200V_{RRM} for 250V_{rms} and 440V_{rms} respectively. The thyristor module is available in three current ratings; the diode module has a single current rating. The concept of the package has revolutionised certain areas of application which hitherto required large numbers of discrete devices mounted on separate heatsinks. As all packages have isolated bases, complex electrical circuits may be mounted on the same heatsink giving savings in production time. Applications include: fully controlled single and three phase bridges, fully controlled single and three phase a.c. switches, motor control, dimmers, battery chargers, primary control of battery chargers, furnace control, etc.

A phase angle trigger module is also available, stock number 301-678. Featuring encapsulated construction with identical fixing centres as the thyristor and diode modules. The module contains all the timing, buffering and thyristor drive circuits necessary to provide reliable and accurate phase control for any of the thyristor modules from a 0 to 5V control signal.

Thyristor pack

Diode pack

Features

- Isolation voltage 2500V
- Packs comprise either two thyristors or two diodes
- On thyristor modules gates taken to one end of package
- Busbars and heatsinks available for increased current ratings

Absolute maximum ratings

Thyristor module

Stock No.	I/V	V_{RRM}	V_{RSM}	I_{RRM}	I_{TRMS}	T_{stg}, T_{vj}
262-551	18/800	800V	900V	8mA	40A	–40/125°C
262-567	18/1200	1200V	1300V	8mA	40A	–40/125°C
262-573	25/800	800V	900V	8mA	50A	–40/125°C
262-589	25/1200	1200V	1300V	8mA	50A	–40/125°C
262-595	40/800	800V	900V	12mA	75A	–40/125°C
262-602	40/1200	1200V	1300V	12mA	75A	–40/125°C

Diode module

Stock No.	I/V	V_{RRM}	V_{RSM}	I_{RRM}	I_{TRMS}	T_{stg}, T_{vj}
262-769	45/800	800V	900V	12mA	90A	–40/125°C
262-775	45/1200	1200V	1300V	12mA	90A	–40/125°C

Electrical characteristics (See table 1 for full definition of parameter symbols) T_j = 25°C unless specified.

		Diode		Thyristor			
Symbol	**Parameter**	**45A Packs**	**18A Packs**	**25A Packs**	**40A Packs**	**Units**	**Conditions**
I_{TAV}	Mean On state current	59 45	25 18	32 25	48 40	A A	T_C = 60°C T_C = 85°C
I_{TSM}	Surge ON state current	700 600	320 280	470 400	1000 850	A A	T_j = 125°C
i^2t	Fusing current	2450 1800	500 390	1100 800	5000 3600	A^2s A^2s	T_j = 125°C
di/dt_{cr}	Critical rate of rise, i	—	100	100	100	A/μs	T_j = 125°C
dV/dt_{cr}	Min. critical rate of rise, V	—	500	500	500	V/μs	T_j = 125°C
T_q	Turn-off time (typ)	—	80	80	80	μs	T_j = 125°C
I_H	Holding current	—	100/200	100/200	150/250	mA	(typ/max)
I_L	Latching current	—	250/400	250/400	300/600	mA	R_G = 33Ω (typ/max)
V_T	Max ON state voltage	1.4	2.3	1.8	1.95(1)	V	I_T = 75A
$V_{T(TO)}$	Threshold voltage	0.85	1.0	0.9	1.0	V	T_j = 125°C
V_{GT}	Max. trigger voltage, d.c.	—	3	3	3	V	
I_{GT}	Max. trigger current, d.c.	—	150	150	150	mA	
V_{GD}	Max. non-trigger voltage, d.c.	—	0.25	0.25	0.25	V	T_j = 125°C
I_{GD}	Max. non-trigger current, d.c.	—	5	5	6	mA	T_j = 125°C

(1) At I_T=200A

Secondary characteristics

		Diode		Thyristor			
Symbol	**Parameter**	**45A Packs**	**18A Packs**	**25A Packs**	**40A Packs**	**Units**	**Conditions**
r_T	ON state slope resistance	5	16	12	4.5	mΩ	T_j = 125°C
$R_{thj\text{-}c}$	Therm. Res. junction/case	0.6	1.2/1.3/1.35	0.9/0.95/1.0	0.65/0.69/0.73	°C/W	Cont./sin. 180/rect. 120
$R_{thc\text{-}h}$	Therm. Res. case/heatsink	0.2	0.2	0.2	0.2	°C/W	
V_{isol}	Insulation test voltage	2500	2500	2500	2500	V	r.m.s.

Table 1: Full definitions of parameter symbols

Note: Parameter values stated on page 1 refer to one arm only of the circuit. See Table 2 for other circuit configurations.

V_{RRM}	Repetitive peak off-state and reverse voltage
V_{RSM}	Non-repetitive peak reverse voltage
I_{RRM}	Repetitive peak off-state and reverse current
I_{TRMS}	RMS on-state current
I_{TAV}	Mean on-state current (half sinewaves)
I_{TSM}	Surge on-state current (10ms half sinewave)
i^2t	i^2t value for fusing (8 to 10ms)
$(di/dt)_{cr}$	Critical rate of rise of on-state current (p.r.f.s. 50 to 60Hz)
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage
t_q	Circuit commutated turn-off time (typ.)
I_H	Holding current
I_L	Latching current at specified R_G (GATE circuit resistance
V_T	ON-state voltage for the specified current I_T
$V_{T(TO)}$	Threshold voltage
r_T	ON-state slope resistance
	See note below
V_{GT}	Gate trigger voltage
I_{GT}	Gate trigger current
V_{GD}	Minimum gate non-trigger voltage
I_{GD}	Maximum gate non-trigger current
$R_{thj\text{-}c}$	Thermal resistance junction to case Cont.: Pure d.c. for a Sin. 180: Half sinewaves single Rec. 120: Rectangular pulses 120° arm
$R_{thc\text{-}h}$	Contact thermal resistance case to heatsink
V_{ISOL}	Insulation test voltage (r.m.s.)
T_{stg}	Storage temperature range
T_{vj}, T_j	Working temperature range (virtual junction temperature)
T_c	Case temperature
T_{amb}	Ambient temperature
Note:	Maximum values used for the calculation of maximum on-state power loss.

Table 2 **Circuit configurations**

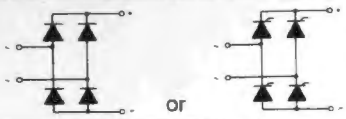
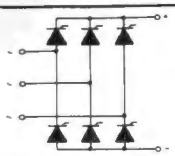
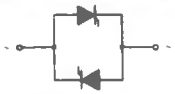
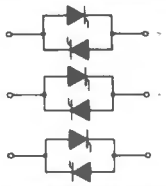
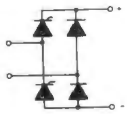
Configuration	Principal circuit	Description
B2		Full controlled single phase bridge
B6		Full controlled three phase bridge
W1		Full controlled single phase A/C switch
W3		Full controlled three phase A/C switch
B2Hz		Half controlled single phase bridge with flywheel path

Table 3 **RC network protection**

The semiconductor modules require the same protection as normal thyristors and diodes. The table shows the recommended RC networks, care must be taken to use capacitors with the required voltage and pulse conditions, the ratings for the resistors coincide with the line frequency.

	$V_{RMS} \leq 250V$		$V_{RMS} \leq 380V$		$V_{RMS} \leq 500V$	
	C	R	C	R	C	R
18/25/40A	0.22μF	68Ω 6W	0.22μF	68Ω 6W	0.1μF	100Ω 10W

Assembly instructions

Table 4 **Mounting torques 402-383**

M1	Torque for mounting module to heatsink	4.5 min 5.5 max Nm
M2	Torque for mounting busbars	2.5 min 3.5 max Nm
Note: 1Nm~0.1mkp~9lb in.		

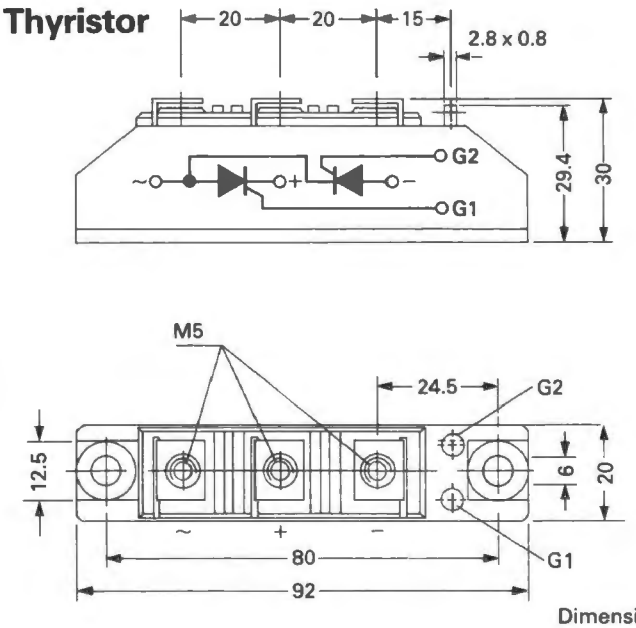
Before mounting on 402-383 surfaces should be coated with RS heatsink compound, 554-311.

In all cases a flat washer and a crinkle or spring washer should be used.

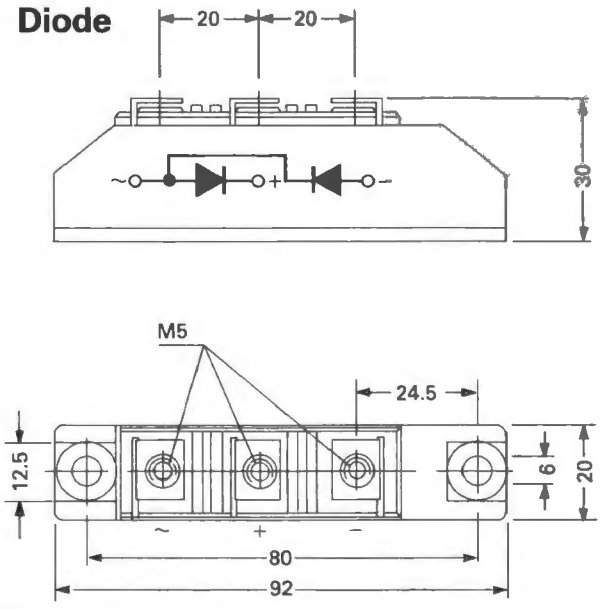
Screws are supplied with the modules for mounting onto the heatsink. Care must be taken that the busbar screws penetrate sufficiently into their tapped hole to give a secure fixing, and also that the screws do not bottom on this blind tapped hole such that the busbars are not held tightly.

After a period of three hours the screws should again be tightened up to the specified torque as the thermal compound spreads out under the mounting pressure.

Thyristor

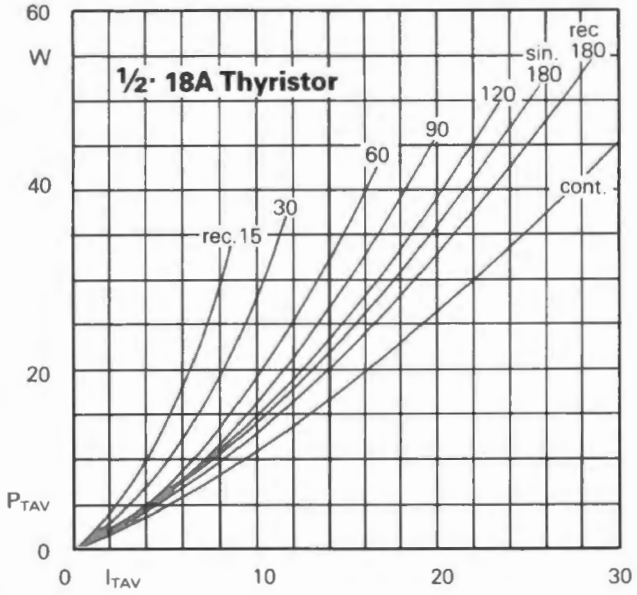


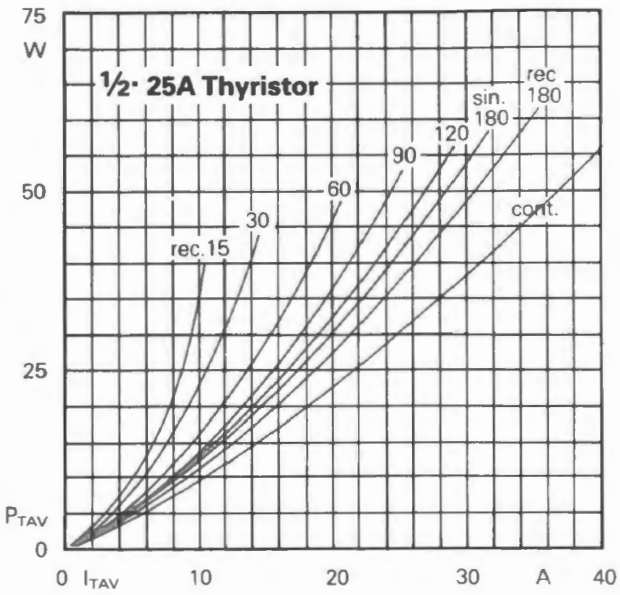
Diode

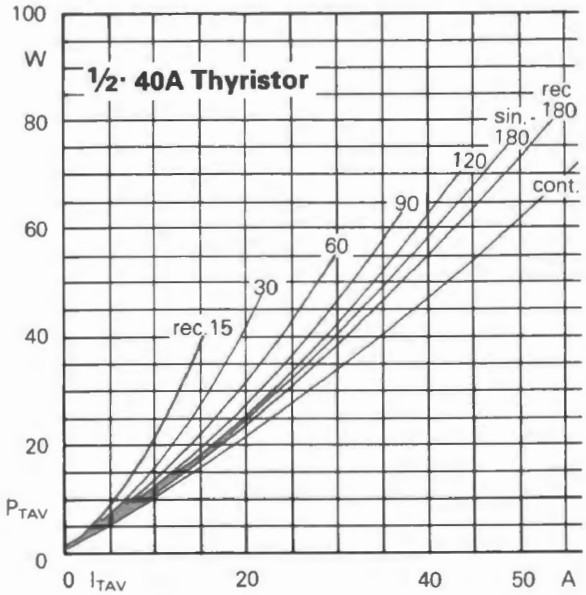


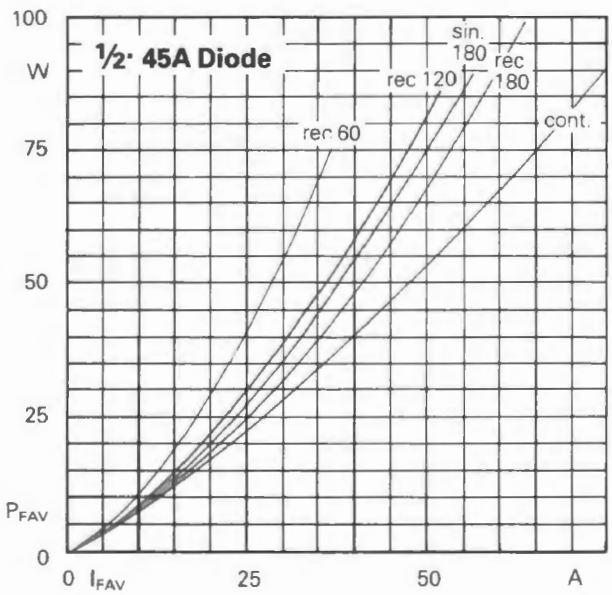
Dimensions in mm

Figure 1



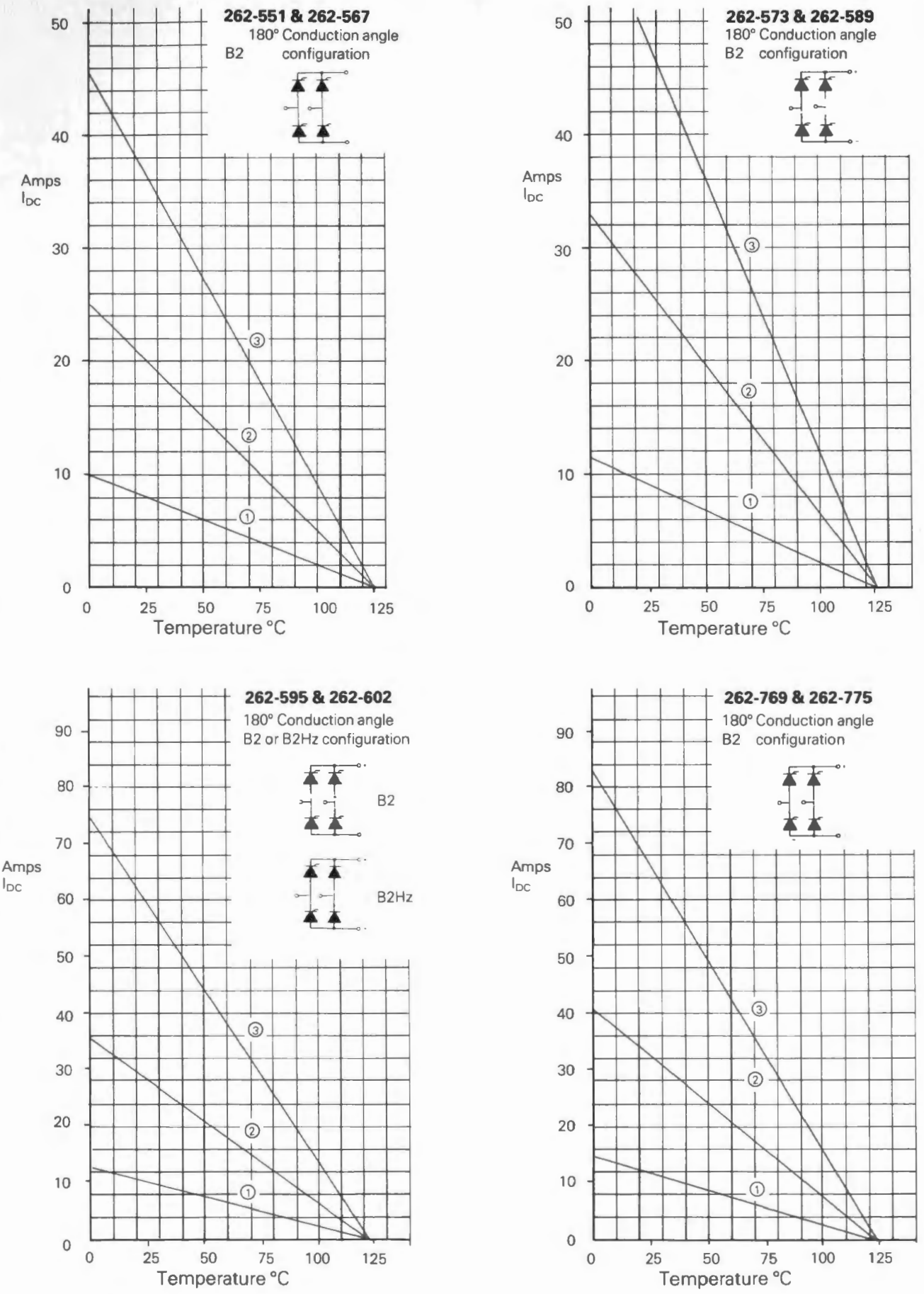






Mean power loss P_{TAV} against mean on-state current I_{TAV} for various conduction angles for a single component.

Figure 2 **Output current I_{DC} against temperature for heatsink mounting.**



① Chassis: 2mm gauge aluminium; 150mm x150mm square.
② Heatsink 402-945.
③ Heatsink 402-383.

Heatsink data

Figure 3 **Heatsink dimensions 402-383**

'X' indicates fixing points required to accommodate 120mm axial fan (4 x M4 screws on 105 centres – see figure 4).

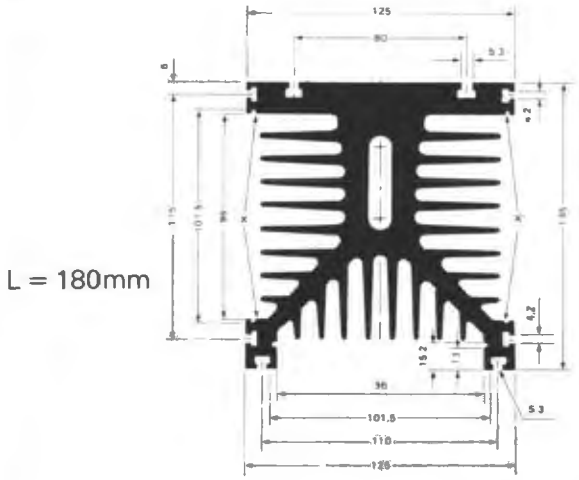
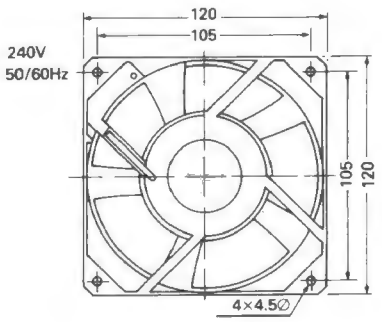
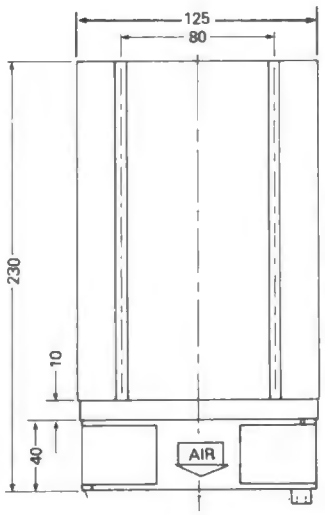


Figure 4 **Heatsink with 120mm axial fan**

To obtain correct cooling, 3 aluminium sheets 180 x 100 x 2mm must be inserted into the slots provided, to close off the fins and ensure proper air-flow. Also a 10mm spacer should be used between fan and heatsink. (Remove burrs from spacer and heatsink assembly.)





Resin bonded insulating spacer with suitable cutout to match fan (see Data Sheet 4440).

Figure 5 **Heatsink dimensions 402-945**

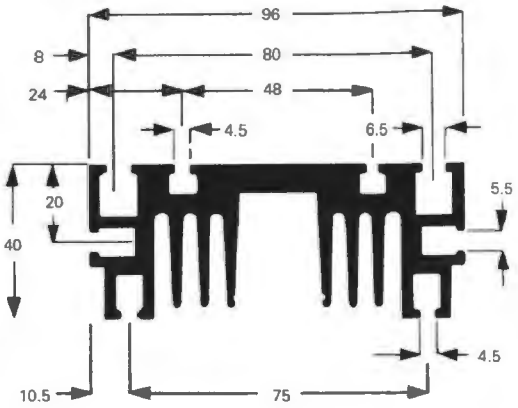


Figure 6 **402-945 Naturally cooled**

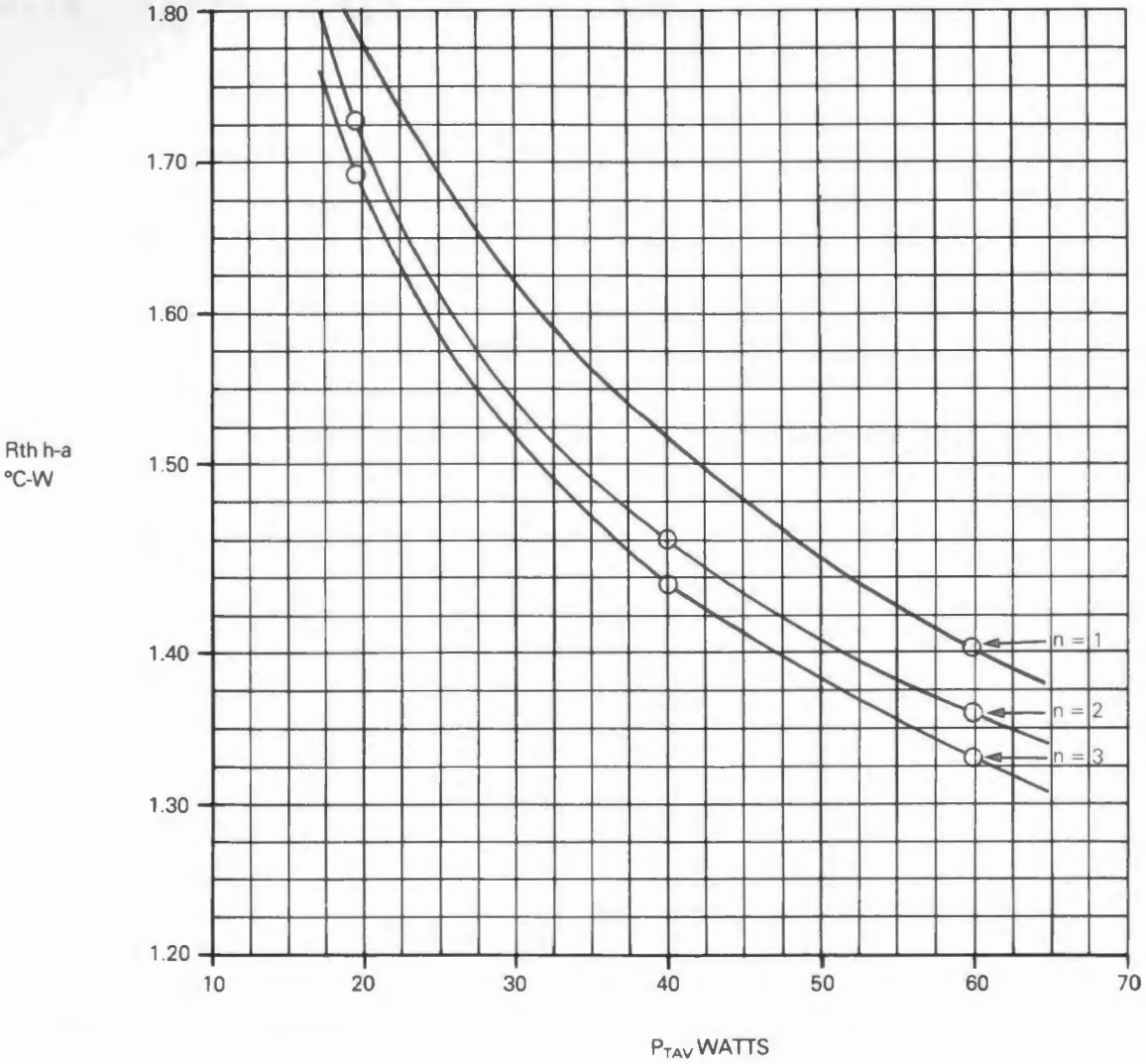
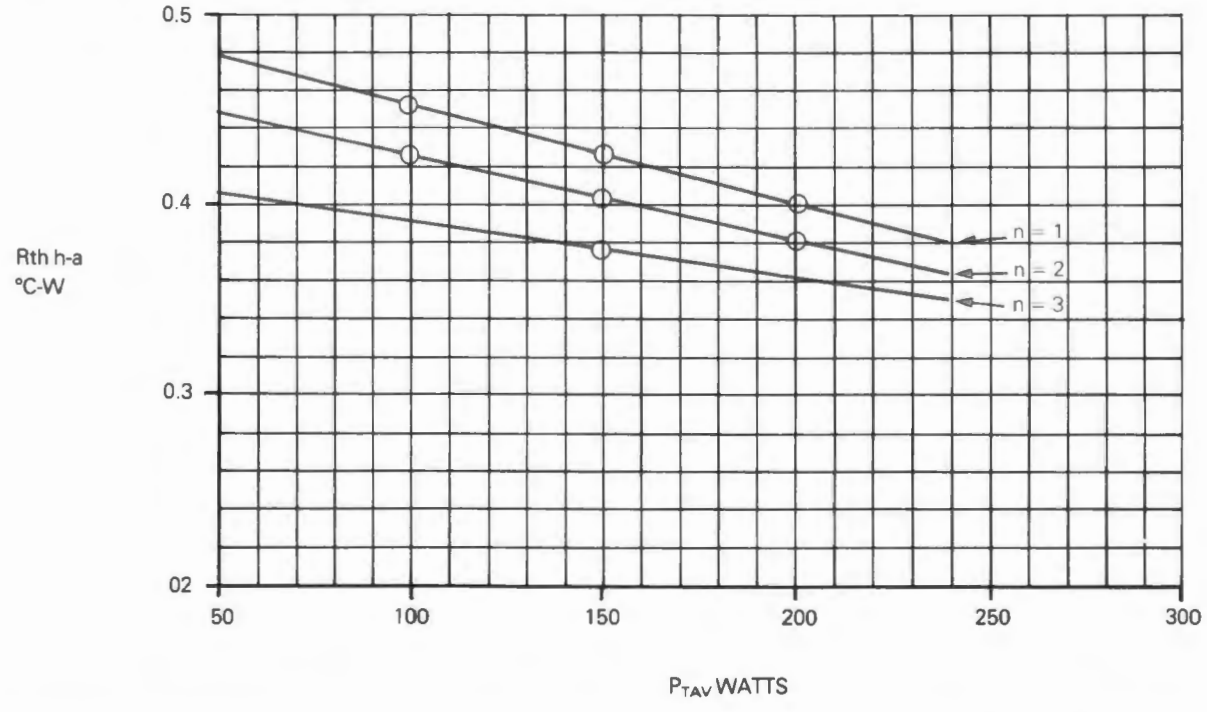


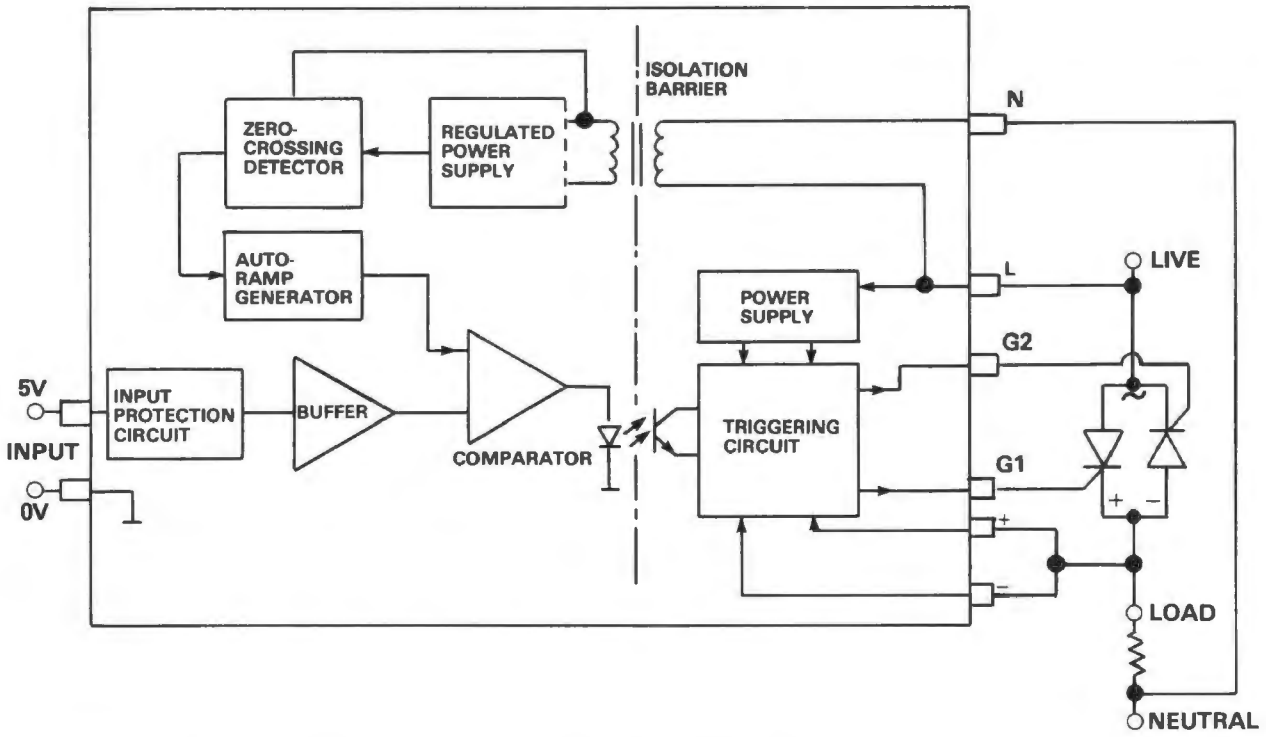
Figure 7 **402-383 Naturally cooled**



Thermal resistance of heatsinks against total dissipation of modules where n = 1, 2 or 3 modules mounted on the heatsink.

RS data

Figure 8 **Phase angle controller**



For further details of phase angle trigger module, see Data Sheet 5162.

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RS data

L.C.D. Panel meter module with annunciators

Stock number 257 — 846

A low profile digital panel meter module with a 3½ digit liquid crystal display incorporating a wide range of commonly employed symbols. A high-contrast display combined with a wide viewing angle results in excellent clarity. Very low current consumption allows long battery life to be obtained: especially useful in portable equipment. Typical applications include digital thermometers, pH meters, and multimeters. Supplied complete with mounting clips.

Absolute maximum ratings

Supply voltage ——— +15V d.c. max
Operating temperature ——— 0°C to +50°C
Storage temperature ——— −20°C to +60°C
Pin soldering temperature ——— 250°C for 8 secs max

Module operation

The L.C.D. panel meter module is centred around the 7126 integrated circuit which is a complete dual-slope-integration analogue-digital convertor which consumes typically only 50μA and drives the custom L.C.D. direct. The circuit diagram of the module is shown in Figure 1.

Components R3, R4 and C1 determine the integrator time constant and C2 reduces the susceptibility to noise of the auto-zero-circuitry. The display is guaranteed to read zero when the analogue input is zero volts.

An input filter is formed by R5 and C3 and assists with overload protection of the 7126. The input voltage may exceed the supply voltage provided the input current does not exceed 100μA.

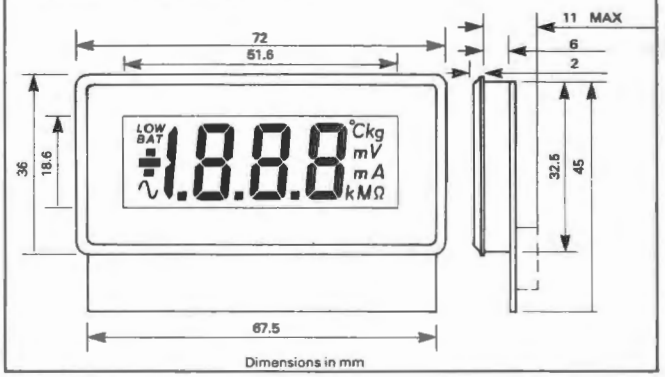
The frequency of the internal oscillator is determined by C5 and R6 and provides typically three samples per second.

As supplied the module is calibrated by means of VR1 for a full scale reading of 200mV with link L1 in circuit and resistor R2 omitted. Figure 2 shows how the input sensitivity may be altered and how the module may be converted for current measurement.

Features

- 15mm high digits
- Auto-zero and auto-polarity
- Programmable decimal points
- 200mV 'full-scale deflection'
- Accuracy is 0.05% of reading (± 1 digit)
- Current consumption typically 100μA at 9V
- Variable threshold low battery warning indicator
- Internal bandgap reference for excellent stability.

Panel cut-out: 68 × 33



Handling precautions

The DPM module contains CMOS devices and must be handled correctly to prevent damage. Input pins should be shorted with conductive foil. Do not make any circuit changes under 'Power On' conditions as high transients may cause permanent damage.

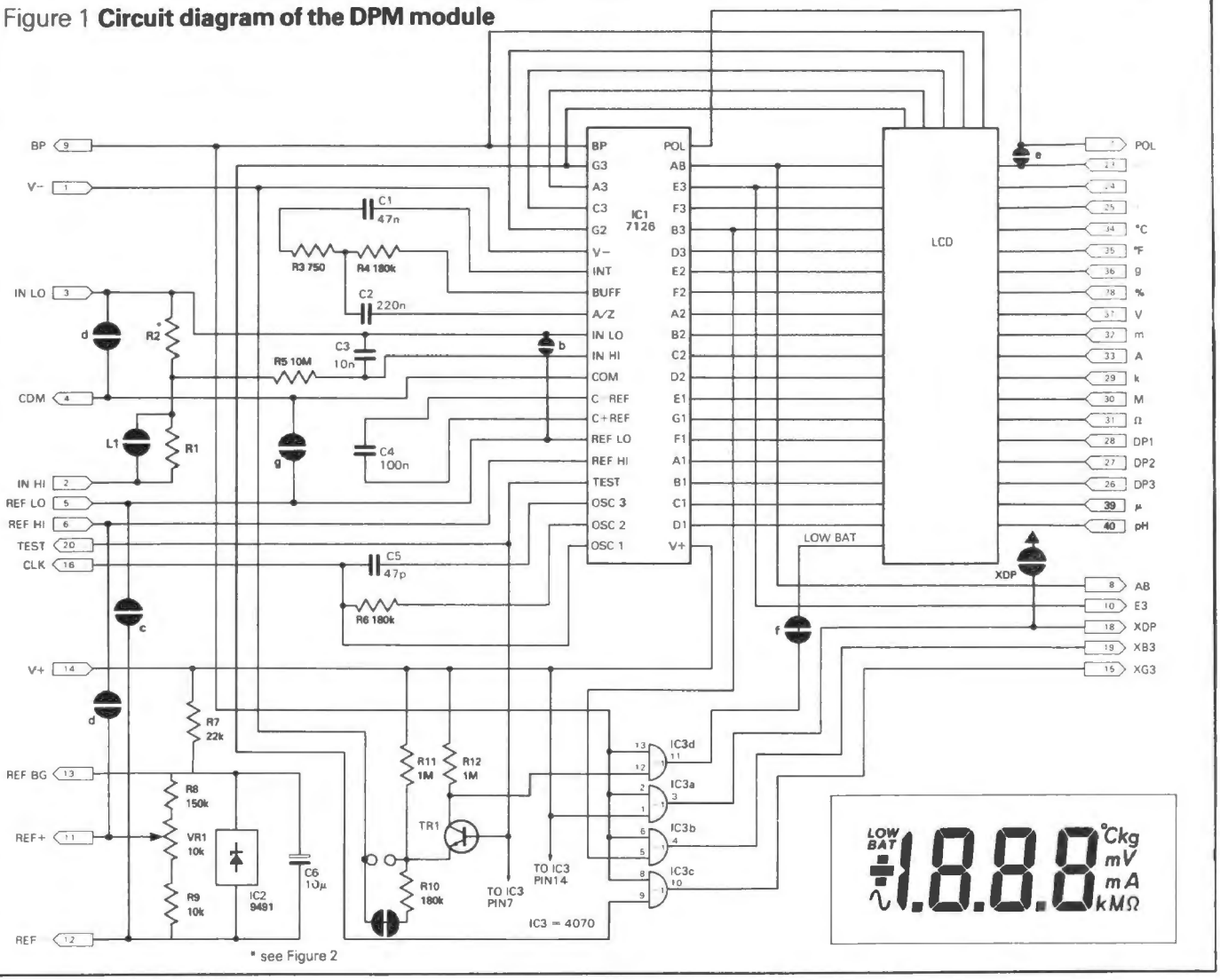
The 7126 has its own internal voltage reference in so far as common is maintained at approximately 2.8V below the positive supply with a temperature coefficient of typically 80ppm/°C. A potential divider could be formed across the internal reference in order to derive the voltage required for the convertor reference input. The convertor operates in ratiometric mode such that the digital display is 1000 V_{IN}/V_{ref} and V_{ref} is normally 100mV.

Electrical characteristics $T_A = 25°C$

Note 1: Accuracy is 0.05% of reading ±1 digit.
Note 2: Also see text 'Module operation'.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply voltage	V_{CC}		5	9	15	V dc
Input impedance	R_{in}		100			MΩ
Accuracy		dc voltage: see note 1	0.05			%
Current consumption	I_{CC}	See note 2		100		μA
Sample rate					3	s^{-1}
Reading stability				50		ppm/°C
Low battery warning threshold				6.4		V dc
Battery life		PP3 battery		2000		hours

Figure 1 **Circuit diagram of the DPM module**



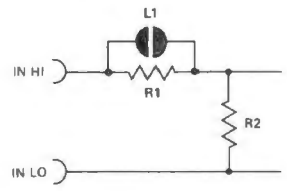
* see Figure 2

In order to obtain higher stability of reading a bandgap reference integrated circuit (IC2) type 9491 is used which relies upon the bulk properties and doping levels of the silicon. The bandgap reference does however require at least 50µA additional current to remain correctly biased. If minimum module consumption is the main requirement the i.c. reference should be used and R7 should be removed to isolate the bandgap reference from the supply. A potential divider across IC2 produces a 100mV output at REF+.

When using the i.c. reference the module may be operated down to 7 volts, whereas when the bandgap reference is used operation down to 5 volts is possible.

A low-battery detection circuit is included in the module to provide advance warning of battery failure directly on the display. A potential divider is formed across the supply by R11 and R10 and when the voltage falls below the threshold set by R10, the collector TR1 changes to a high level. Exclusive - OR gate IC3d then acts as an inverter to provide an output in anti-phase to the backplane input and so provide the required L.C.D. drive signal for the LOW BAT warning. The 180k value fitted for R10 provides advance battery low warning at typically 6.4V. The value of R10 may be altered, if required, by adding a resistor at the rear of the p.c.b. and splitting pad h to isolate the internal resistor. Resistors in the range 100k to 200k are usually required.

Figure 2 **Method of altering the full scale reading of the DPM module**



Required Full Scale	L1/R1	R2
2V	10M	1M
20V	10M	100k
200V	10M	10k
2000V	10M	1k
200µA	LINK	1k
2mA	LINK	100Ω
20mA	LINK	10Ω
200mA	LINK	1Ω

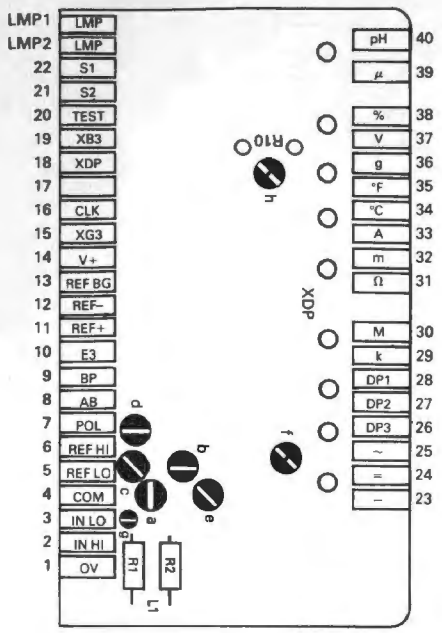
Exclusive −OR gate IC3a inverts the backplane signal and may be used to activate any multiple of the auxiliary L.C.D. symbols or decimal points by direct connection to those required. Gates IC3b and IC3c provide outputs which are useful in auto-ranging applications.

Connection notes

The pin connection diagram for the p.c.b. is shown in Figure 3. The analogue inputs are truly differential and may be operated to within 0.5V below the positive supply and 1V above the negative supply. Common mode rejection ratio within this range is typically 86dB. The COM (common) pin is a convenient method of establishing the correct common mode voltage since it is set approximately 2.8V below the positive supply.

Reference inputs are differential and may be anywhere within the power supply voltage range of the module.

Figure 3 **P.c.b. pin connection diagram**



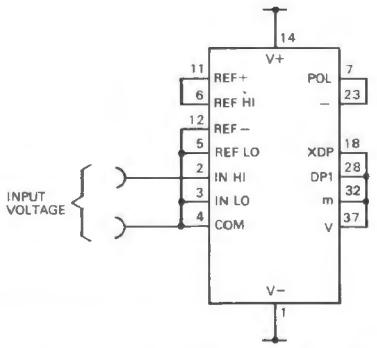
The Polarity output is a square wave in-phase with the backplane signal when the analogue input has positive polarity and in anti-phase when the input has negative polarity.

Four outputs are provided for use in auto-ranging applications, these are AB, E3, XG3 and XB3 – see Figure 4d.

Output REF+ is 100mV with respect to REF– when the latter is correctly terminated. REF BG is 1.2V with respect to REF–.

Figure 4a **Module connections for measuring a floating voltage source with 200mV full scale.**

Autopolarity indication is implemented together with the decimal point and 'mV' annunciation.



Note that the linking is achieved by the use of the solder pads, not wire links.

The Clock output may be used for systems timing or as an input to over-ride the internal oscillator and control the sample rate. If CLK is connected to V+ (or TEST) the display may be held at a particular value, but this should not be connected for extended periods as the steady d.c. potential applied to the L.C.D. may cause the segments to 'burn'.

The TEST output may be used as a negative supply for external integrated circuits with a maximum load of 1mA. If TEST is connected to V+ the L.C.D. segments will be turned on and the display will read as shown in Figure 5. (This mode should not be used for extended periods, to avoid damage to the L.C.D.) Note that – 1888 is not precisely indicated, two segments being 'missing'. This occurs as an unavoidable consequence of using the B3 and G3 outputs to feed IC3 – see Figure 2.

Figure 4b **Basic arrangement for measuring the ratio of two voltages.**

The display = 1000 V2/V1. Maximum input voltage is ± 2V with a 9V supply.

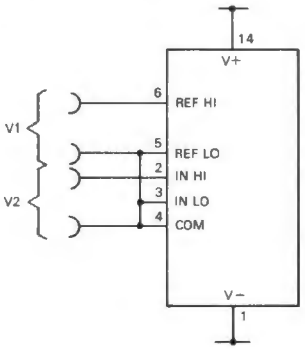


Figure 4c

If a zero display is required when the applied input is not zero volts the offset voltage should be connected between the IN LO and COM, while the input voltage is connected between the COM and IN HI.

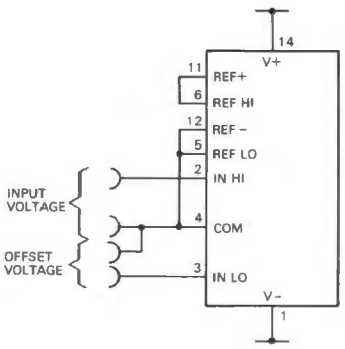


Figure 4d **Generation of signals for use in auto-ranging applications**

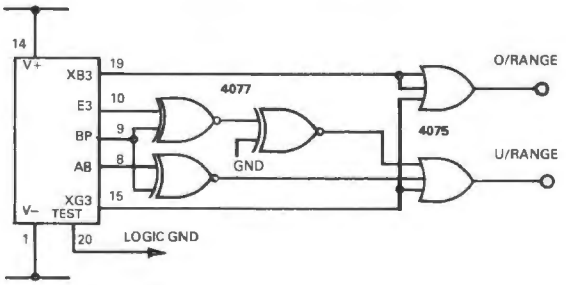


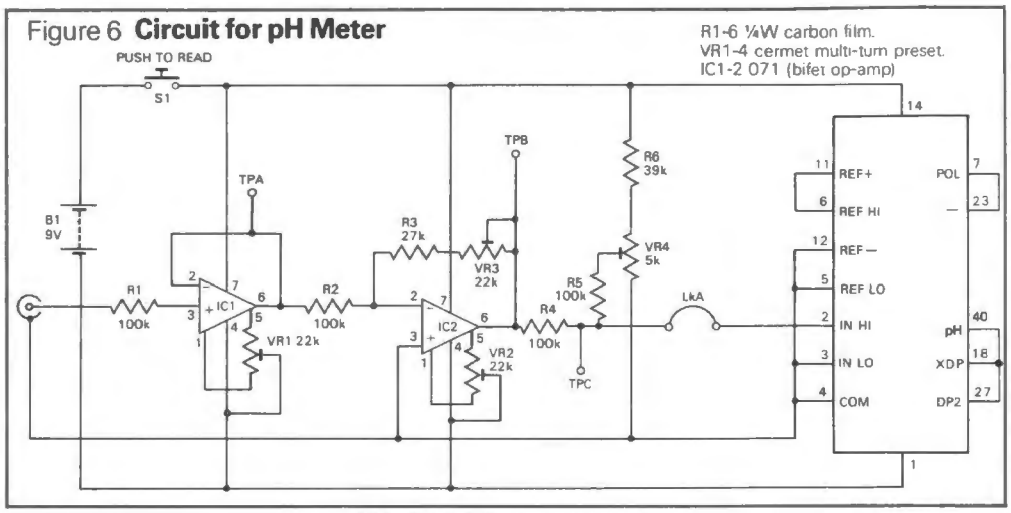
Figure 5 **Display in 'TEST' condition.**

RS data

Applications

The L.C.D. DPM may form the basis of many instruments. The circuits on page 3 give the basic connection data, along with the Figure 2 on page 2. Further circuits are suggested here, although some experimentation may be required to optimise these for particular applications.

Figure 6 **Circuit for pH Meter**



pH Meter

'pH' is essentially a measure of the acidity of a solution and as such is useful in many industrial and organic processes. The value is in fact defined as:

$$pH = \log_{10}(1 \div [H+])$$

A 'neutral' solution (e.g. pure water) has a pH of 7. Acidity is indicated by values between 0 and 7, and alkalinity by values between 7 and 14.

pH probes produce very small voltages and required amplification by high impedance amplifiers to drive a suitable meter. Figure 6 shows a suitable circuit.

Operational amplifier IC1 forms a unity-gain voltage follower, with a very high input impedance. Amplification is provided by IC2 and is set by VR3. A reference voltage is adjusted by VR4, such that with zero input from the probe a reading of 7.00 is obtained on the panel meter.

Calibration

1. Remove link LK A.
2. Connect battery.
3. Connect 150mm of wire (insulated) to the meter side of LK A position. Bare the other end – this acts as a 'test prod'.
4. Touch 'prod' on the 'earthy' side of the coaxial input socket. A reading of 0.00 should be obtained.
5. Connect a shorting link to the coaxial socket and touch the 'prod' on TP A. Adjust VR1 for a zero reading.
6. Touch 'prod' on TP B and adjust VR2 for zero reading.
7. Touch 'prod' on TP C and adjust VR4 for a reading of 7.00.
8. Remove the lead and insert LK A. Remove the socket link and insert the pH probe.
9. Place the pH probe into distilled water (pH 7) and adjust VR1 for a reading of 7.00.
10. Place the probe into an acid solution of pH 4. Adjust VR3 for a reading of 4.00. Calibration is now complete.

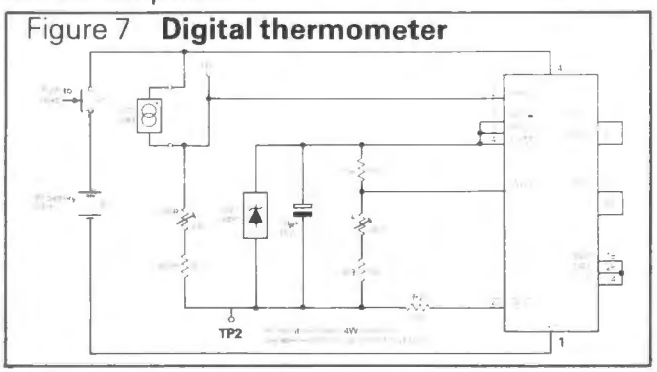
Digital Thermometer

The circuit of a digital thermometer is shown in Figure 7. This has been designed to operate with the **590** type of temperature sensor (RS Stock No. 308-809).

Calibration of the circuit is easily performed with the aid of a digital voltmeter. Connect the voltmeter across TP1 and TP2 and, with the 590 sensor at 0°C, adjust VR1 for a voltmeter reading of 273mV. With the 590 sensor still held at 0°C, adjust VR2 for a digital display of 0.0°C.

Calibration can be effected at ambient temperature if a calibrated thermometer is available. VR1 may be adjusted so that the voltage across TP1 and TP2, equals 1mV/°K at that temperature. VR2 can then be adjusted until the digital display indicates the correct temperature.

Figure 7 **Digital thermometer**



Multi-meter circuits

The meter module is ideally suited as a basis of a high grade multi-meter. Figure 2 outlines the method of use for d.c. voltage and current ranges. For a.c. a precision rectifier, using an operational amplifier, can be located after the attenuator stages. Resistance ranges are fairly readily incorporated in the normal manner. Input protection can also be arranged in a conventional way. Since, however, some specialized components (close tolerance resistors) are required, an actual circuit is not offered.

Telephone: 0536 201234
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RS data

8 Channel, 8 bit A to D converter i.c.'s 7581JN and 7581LN

Stock numbers 303-545 and 301-612

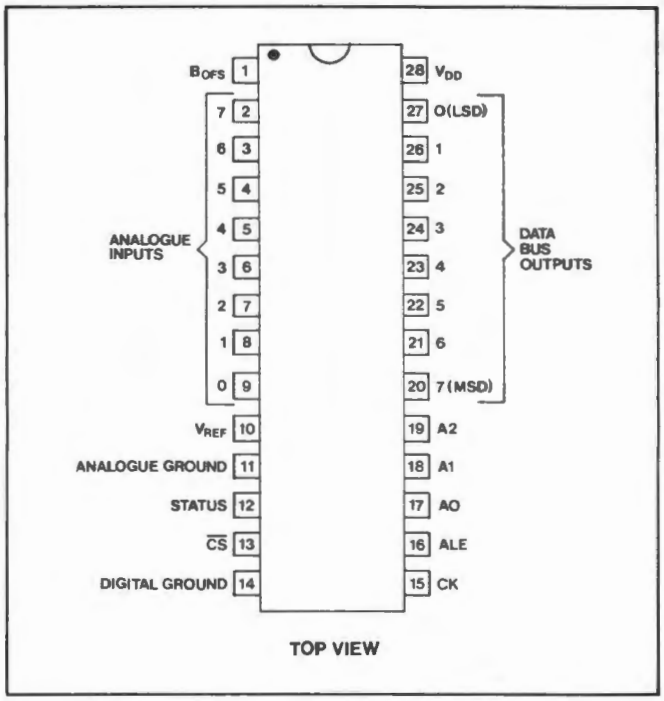
The RS7581's are microprocessor compatible 8-bit, 8-channel monolithic memory buffered data acquisition systems. The devices contain an 8-bit successive approximation analogue to digital converter, an 8-channel input multiplexer, 8 x 8 dual port ram, three state data drivers, address latches and microprocessor compatible control logic. Two converter types are available the 7581JN with ±1⅞ LSB relative accuracy and ±1⅞ LSB differential non-linearity, or the high performance 7581LN. This grade features a ±½ LSB relative accuracy and ±¾ LSB differential non-linearity, making it ideal for use in applications where higher accuracy is required.

Absolute maximum ratings

V_{DD} to analogue ground	0 to 7V
V_{DD} to digital ground	0 to 7V
Analogue ground to digital ground	−0.3 to V_{DD}
Digital input to digital ground	15V
Digital output voltage to digital ground	−0.3 to V_{DD}
CK input to digital ground	15V
V_{REF} to analogue ground	±25V
B_{OFS} to analogue ground	±17V
Analogue inputs pins 2-9	±17V
Power dissipation	1.2W
Lead temperature soldering 10s	+300°C
Storage temperature	−65°C to 150°C
Operating temperature	0°C to 70°C

Features

- 8-bit resolution
- On chip 8 x 8 memory
- Direct microprocessor interface
- CMOS and TTL digital inputs
- Single 5V supply
- Fast conversion
- Conversion process totally transparent to μP.



WARNING!

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Electrical characteristics V_{DD} = +5V, V_{REF} = −10V, T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Resolution				8	8	bits
Relative Accuracy				±1⅞ (±½)	±1⅞(±½)	LSB
Differential Nonlinearity				±1⅞ (±¾)	±1⅞ (±¾)	LSB
Offset error		Note 1		200 (50)	200 (50)	mV
Worst channel gain error				±3 (±1)	±6 (±2)	LSB
Gain match between channels				2 (1)	3 (1)	LSB
B_{OFS} Gain error		Note 2		−2½	–	LSB
Input resistance V_{REF}	RV_{REF}		10	20	30	kΩ
Input resistance B_{OFS}	RB_{OFS}	Note 3	10	20	30	kΩ
Any analogue input (pins 2-9)			10	20	30	kΩ
Reference for specified perf.	V_{REF}			−10		V
Reference Range	V_{REF}	Note 4	−5		−15	V
Analogue input range Unipolar				0 to $+V_{REF}$ and 0 to $-V_{REF}$		V
Analogue input range Bipolar			$-VB_{OFS}$		$\lvert V_{REF}\rvert - VB_{OFS}$	V
Digital inputs, pins 13 & 15-19						
High input voltage	V_{INH}			2.2		V
Low input voltage	V_{INL}			0.4		V
Input current	I_{IN}			0.01		μA
Input capacitance	C_{IN}			4		pF
Digital outputs, pins 12 & 20-27						
Output high voltage	V_{OH}	40μA I source		4.8		V
Output low voltage	V_{OL}	16mA I sink		0.4		V
DB_7 to DB_0 leakage	I_{LKG}			0.3		μA
Output capacitance		Floating output		5		pF
Supply voltage	V_{DD}			5		V
Supply current static	I_{DD}			3	5	mA
Supply current dynamic	I_{DD}	f_{CK} = 1 MHz		3	8	mA

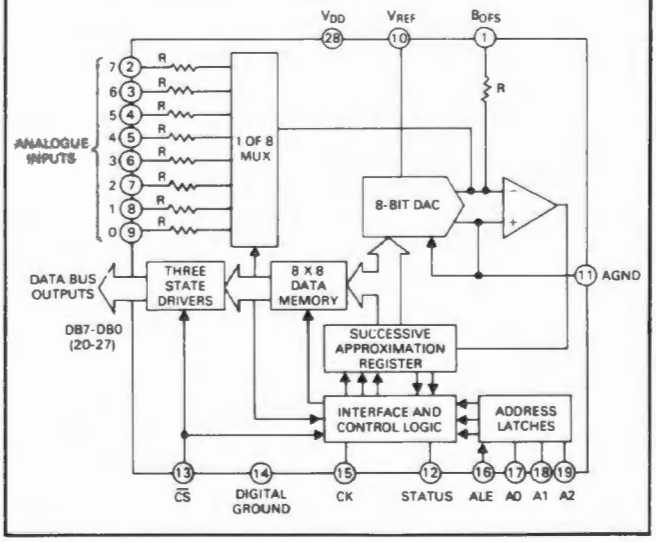
Figures in brackets are for 7581LN high performance device

Notes
1) Typ. offset temperature coefficient is ± 150μV/°C.
2) Typ. change in B_{OFS} gain from +25°C to 0°C to +70°C is ±2 LSB's.
3) R_{BOFS}/R_{AIN} (0-7) mismatch causes transfer function rotation about positive full scale.
4) Typical range, not guaranteed or subject to test.

General information

The RS7581 accepts eight analogue inputs and sequentially converts each input into an eight-bit binary word using the successive approximation technique. Results from the conversions are stored in the internal 8 x 8 dual-port RAM. The device will run either directly from the microprocessor clock in 6800 type systems or from other suitable signals (eg. ALE etc). Start-up logic is included on the chip to establish correct power-up. A maximum of 800 clock pulses are required for start-up. See Figure 1 for functional diagram.

Figure 1 **Functional diagram**



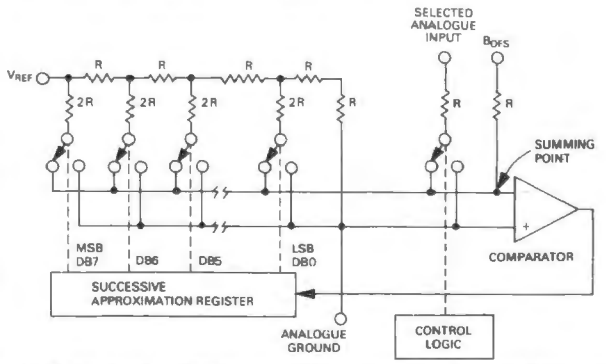
Conversion of a single channel takes 80 clock periods with a complete scan through all eight channels taking 640 input clock periods. When a channel conversion is complete, the successive approximation register contents are loaded into the proper channel location of the 8 x 8 dual port RAM. At this instant the status signal output gives a short (8 clock periods) negative pulse. This negative pulse is extended to 72 clock periods when channel 1 conversion is complete. This status output can be used to generate conversion related timing signals for microprocessor interrupts. Simultaneously with the status output going low the multiplexer address is decremented. Eight clock periods later the next conversion is started.

Automatic interleaved DMA (direct memory access) is provided by on-chip logic to ensure memory updates only occur when the microprocessor is not addressing the converter memory. A_0, A_1 and A_2 are used to address the memory locations: this address may be latched by ALE for systems which feature a multiplexed address/data bus. For systems with separate address and data busses, the address latches can be made transparent by tying ALE (pin 16) high. CS (pin 13) activates the three-state buffers to place addressed data on the DB_0 to DB_7 data outputs.

Converter details

The functional diagram of the converter shows the internal structure. The current weighted D to A converter is a precision multiplying type. Figure 2 shows the circuit used. It consists of a precision silicon chromium thin film R/2R ladder network and eight N-channel MOS FET switches operated in a single pole double throw mode. The currents in

Figure 2 **Internal converter circuit**



each 2R shunt arm are binary weighted, ie. the current in the MSB arm is V_{REF} divided by 2R, in the second arm is V_{REF} divided by 4R, etc. Depending on the digital output of the successive approximation register, the current in the individual shunt arms is steered either to analogue ground or to the comparator summing point.

Table 1 **Timing specifications Unipolar operation** $V_{DD} = +5V, V_{REF} = -10V, C_L = 100pF$

Parameter	Symbol	Typ at 25°C	Limit over temperature range	Units
ALE pulse width	t_H	50	80 min	ns
Address valid to latch set-up	t_{ALS}	45	70 min	ns
Address valid to latch hold	t_{ALH}	10	20 min	ns
Address latch to CS set-up	t_{LCS}	10	20 min	ns
CS to output propagation delay	t_{ACC}	200	250 max	ns
CS pulse width	t_{CW}	250	280 min	ns
CS to output tri-state propagation delay	t_{CF}	50	80 max	ns
CS to low impedance bus	t_{CLZ}	100	150 max	ns
Clock frequency stated accuracy	f_{CLK}	1600	1200 max*	kHz

*Guaranteed conversion time of 66.6μs/channel with 1200kHz clock.

Channel selection and identification

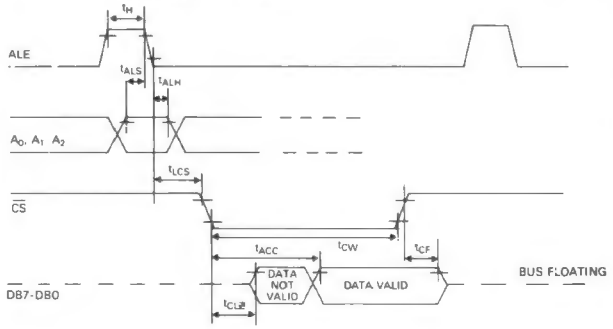
Table 2 shows the required address inputs for the appropriate channel output required. The input address is latched when ALE goes low. When ALE is high the address input latch is transparent. A typical timing diagram is shown in Figure 3.

Table 2 **Channel selection**

Channel data to be read	ALE	A2	A1	A0
0	1	0	0	0
1	1	0	0	1
2	1	0	1	0
3	1	0	1	1
4	1	1	0	0
5	1	1	0	1
6	1	1	1	0
7	1	1	1	1

The input address is latched when ALE goes low.
The address input latch is transparent when ALE is high.

Figure 3 **Timing diagram**

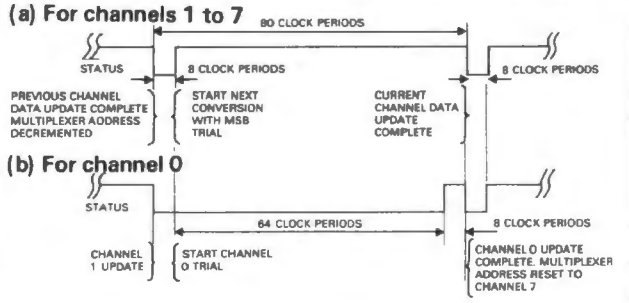


t_H: ALE pulse width requirement.
t_{ALH}: Address valid to latch hold time.
t_{ALS}: Address valid to latch set-up time.
t_{LCS}: Address latch to chip select set-up time.
t_{CW}: Chip select pulse width requirement.
t_{ACC}: Chip select to valid data propagation delay.
t_{CF}: Chip select to output data tri-state propagation delay.
t_{CLZ}: Chip select to low impedance data bus.

Channel identification

In some real-time applications, it may be necessary to provide an interrupt signal when a particular channel receives updated data. To achieve this, it is necessary to identify which channel is currently under conversion. The status output provides an identifying signal by staying low for an additional 64 clock periods over the normal 8 periods when channel 0 is active. This is illustrated in Figure 4. Memory update takes place on the rising edge of a clock pulse. This occurs 6 clock periods before status goes low. The microprocessor may also be used to interrogate the status output and hence determine channel identity.

Figure 4 **Status output for channel identification**



Applications

Unipolar binary operation

Figures 5 and 6 show the analogue circuit connections and typical transfer characteristic for unipolar operation (0V to +10V).

Calibration, (device clocked ie. continuous conversions), comparator offset

This is trimmed out using the bipolar offset pin B_{OFS} using the potential divider and buffer amplifier.

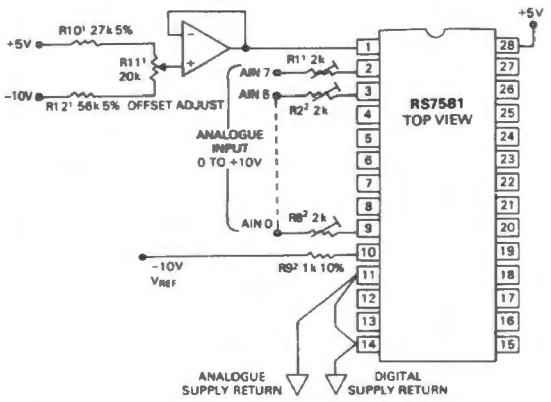
1) As the comparator offset is the same regardless of which channel is active. A_0, A_1 and A_2 are taken low and ALE is used to latch this address.
2) With the analogue input 0 = 19.5mV (½LSB) R11 is adjusted altering the offset voltage on B_{OFS}, until DB_7-DB_1 are low and DB_0 (the LSB) flickers.

Gain adjustment (full scale)

In many applications gain adjustment is not required, this removes the need for trimmers in the analogue input channels. If gain adjustment is required the following procedure is recommended.

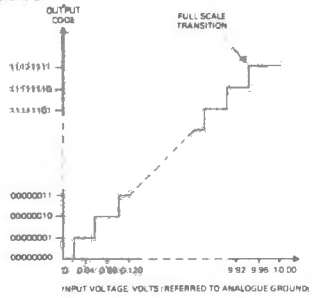
1) Offset adjustment should be performed as before.
2) Apply +9.941V (FS−1½ LSB) to all input channels 0-7.
3) Select required channel n via A_0, A_1 and A_2, latch this using ALE.
4) Adjust the trimmer in the selected channel until DB_7-DB_1 are high and DB_0 (the LSB) flickers.
5) Select next channel requiring adjustment and repeat 3 and 4.

Figure 5 **RS7581 unipolar (0V to +10V) operation (output code is straight binary)**



NOTES
1 R10, R11, R12 AND BUFFER AMPLIFIER CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED. B_{OFS} CAN BE TIED TO A_{GND}.
2 R1-R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.

Figure 6 **Transfer characteristic for unipolar circuit**



NOTE: APPROXIMATE BIT WEIGHTS ARE SHOWN FOR ILLUSTRATION.
BIT WEIGHT FOR A −10V REFERENCE IS ≈39.1mV.

Unipolar (complementary binary) operation

Figures 7 and 8 show the analogue circuit connections and typical transfer characteristic for unipolar (complementary binary) operation.

Calibration (continuous conversions) offset

Comparator offset is trimmed out at the B_{OFS} pin.

1) As the comparator offset is the same regardless of which channel is active, A_0, A_1 and A_2 are taken low and ALE is used to latch this address.
2) With analogue input 0 = −9.998V (−FS + ½ LSB)

adjust R11 altering the offset voltage on B_{OFS}, until DB_7-DB_1 are low and DB_0 (the LSB) flickers.

Gain adjustment (full scale)

In many applications gain adjustment is not required, this removes the need for trimmers in the analogue input channels. If gain adjustment is required the following procedure is recommended.

1) Offset adjustment should be performed as before.
2) Apply −58.6mV (1½ LSB) to all input channels 0-7.
3) Select required channel n via A_0, A_1 and A_2, latch this using ALE.
4) Adjust the trimmer in the selected channel until DB_7-DB_1 are high and DB_0 (the LSB) flickers.
5) Select next channel requiring adjustment and repeat 3 and 4.

Figure 7 **RS7581 (−10V to 0V) operation (output code is complementary binary)**

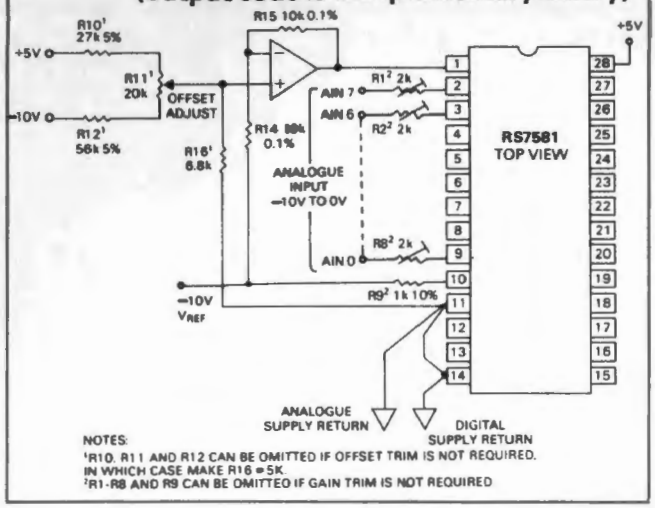
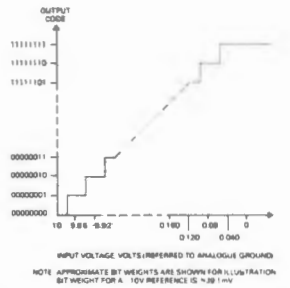


Figure 8 **Transfer characteristic for unipolar circuit**



Bipolar (offset binary) operation

Figures 9 and 10 illustrate the analogue circuitry and transfer characteristic for ±5V bipolar operation, output coding is offset binary. Comparator offset correction is again applied to the B_{OFS} pin as before.

Calibration (continuous conversions) offset

1) Apply −4.980V (−FS + 4 LSB) to all input channels 0-7.
2) R11 of the comparator offset circuit is trimmed until DB_7-DB_1 are low and the LSB (DB_0) flickers.

Gain (full scale)

1) Apply +4.984V (+FS −4 LSB) to all input channels 0-7).
2) Select required channel n via A_0, A_1 and A_2, latch this using ALE.
3) Adjust the trimmer in the selected channel until DB_7-DB_1 are high and DB_0 (the LSB) flickers.
4) Select the next channel requiring gain trim and repeat steps 2 and 3.
5) Apply 0V to each gain-trimmed channel. If the output code does not flicker between 01111111 and 10000000 repeat the calibration procedure.

Figure 9 **RS7581 bipolar (−5V to +5V) operation (output code is offset binary)**

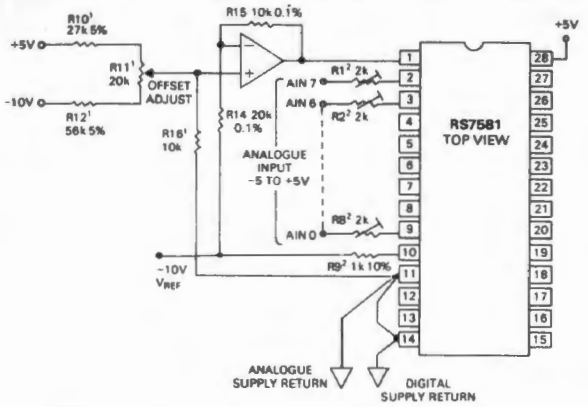
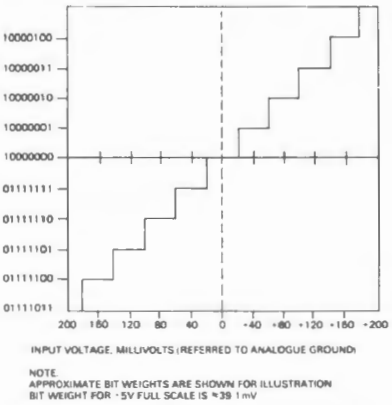


Figure 10 **Transfer characteristic around major carry for bipolar circuit**



RS data

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RS data

Universal Guard Safety Switch

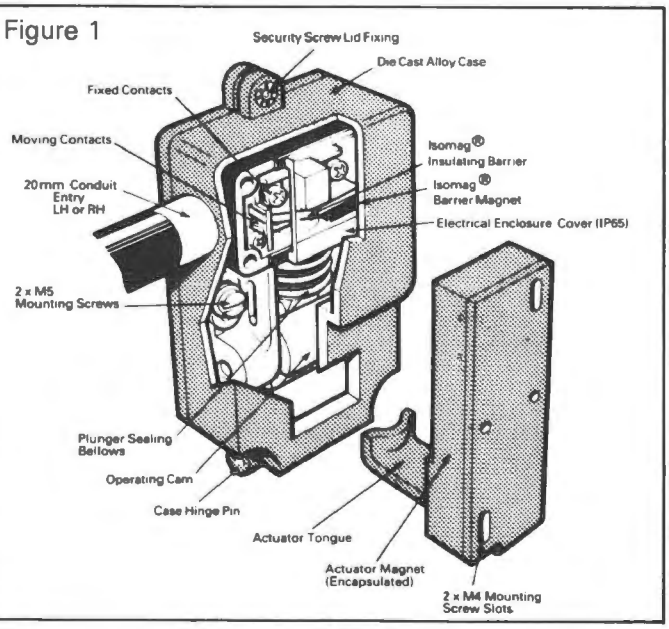
Stock Number 334-971

A universal guard safety switch which fulfils the requirements covering machine safety as detailed in BS 5304 "Safeguarding of Machinery – Codes of Practice". The switch is operative in any position and offers equal protection to hinged, sliding or lift-off guards. Its advantages over other guard safety switches include forced disconnection of contacts, sealing to IP65 allowing the unit to be hosed down, fail safe design and high degree of tamper resistance.

Electrical Data

Contacts: 1 pair N/O
Rating: 10A 500V a.c.
Conduit entry: M20 (1 gland supplied for either RH or LH entry)

Figure 1



Construction details

Switch case: heavy duty die cast alloy.
Actuator: reinforced polycarbonate case, steel tongue.
Switch interior: reinforced polycarbonate.
Mounting: any position.
Mounting screws: switch M5 x 19 (not supplied)
actuator M4 x 19 (not supplied)
Switch cover screw: M4 with special security head (screw driver bit supplied).
Mounting clearance: 3mm min – 6mm max (between guard and actuator)

Features

- Forced mechanical disconnection
- Unique Isomag isolation system
- Suitable for hinged sliding or removeable guards,
- Highly tamper-resistant, rugged construction
- Simple to install
- Dust proof and Hose proof to IP65 in any position

Requirements for a guard safety switch

Very few industrial establishments are exempt from the legislation and recommendations covering Machine Safety, similar to those illustrated is BS 5304 "Safeguarding of Machinery – Codes of Practice".
Basic requirements include forced disconnection in the event of contact weld and a fail-safe design in case of component failure (e.g. return spring). In addition, a high degree of tamper resistance together with ease of installation and tha ability to meet a wide range of applications.

The RS Guard Safety Switch – advantages

(a) No operating cams required, the switch is complete and ready for immediate installation (see Installation Details). It is operative in any position, accepts considerale guard wear (adjustment via slotted mounting holes in switch and actuator housing), and is unaffected by vibration.
(b) Fits almost any type of guard. The safety switch offers forced disconnection protection equally to hinged, sliding and lift-off guards. A guard movement of only 6mm is sufficient to effectively isolate the machine and ensure forced disconnection. In addition, existing guards can be easily and inexpensively be updated due to the simplicity of the basic switch design.
(c) Has a high level of electrical protection. The magnetically-actuated insulated barrier isolates the moving contacts at all times, ensuring that deliberate or accidental operation of the machine is virtually impossible when the guard is open.
(d) It is extremely tamper-resistant. The combination of the magnetically-actuated barrier, the design of the mechanically-operated switch and the use of tamper-resistant security screws ensures a high level of all-round personnel and machinery protection.
(e) The die cast case affords authorised personnel quick and easy access to the IP65 protected internal switch unit which can be thoroughly hosed down and cleansed.

®Isomag is a registered mark of EJA Engineering Ltd.

How the switch works

The switch, fully detailed in Figure 1, is mounted on the fixed portion of the guard while the actuator is mounted on the moving guard (sliding, hinged or lift-off pattern). Closing the guard causes the actuator tongue to enter the switch through the cover aperture and operate the integral cam. This drives the moving contacts to the closed position and simultaneously removes the insulating barrier from the fixed contacts by the action of the encapsulated actuator magnet. Opening the guard automatically replaces the barrier in position and insulates the electrical contacts. Compared with standard limit switches the RS Guard Safety Switch offers a high degree of safety and tamper resistance. In addition, because of its flexibility, complete standardisation is possible with attendant cost savings.

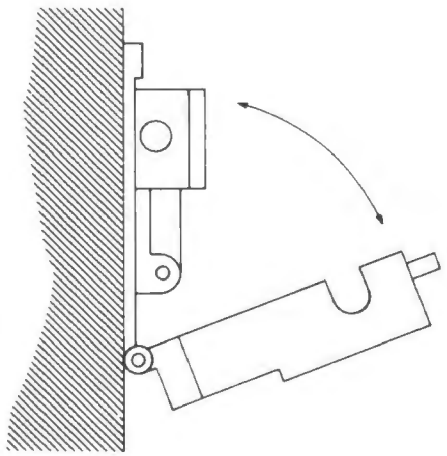
When installed the rugged design and simple electro-mechanical device combine to provide a switch which is easy to service and maintain.

Easy to hose down

The lid of the case can easily be swung open to allow the unit to be regularly hosed down, as is imperative in the Food Industry (see Figure 2). The switch components are sealed to IP65 environmental protection in any position.

The switch cannot be actuated with the lid open.

Figure 2



Installation details

1. Mount the switch on the fixed part of the guard (see Figures 3 & 4)

Figure 3: **Case details**

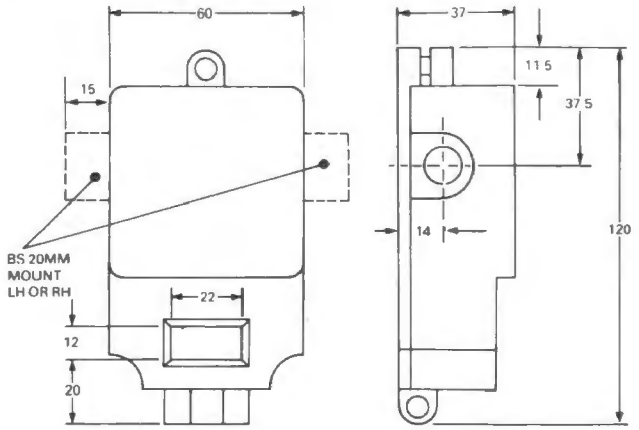
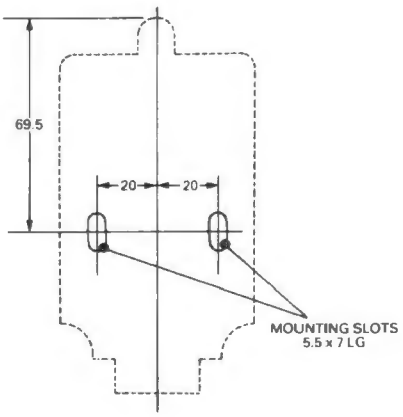
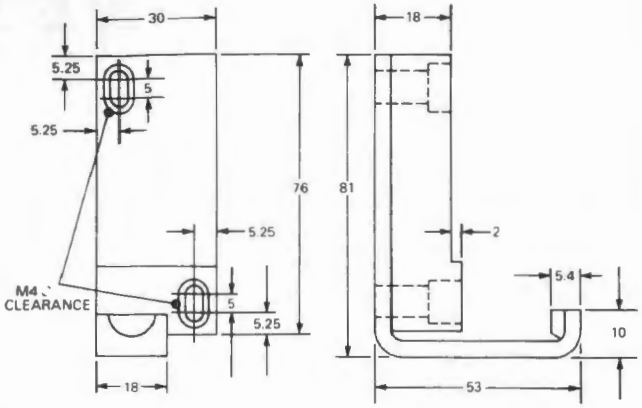


Figure 4: **Mounting details**



2. Mount the actuator on the moving part of the guard with the tongue centrally opposite the switch entry (see figure 5).

Figure 5: **Actuator details**



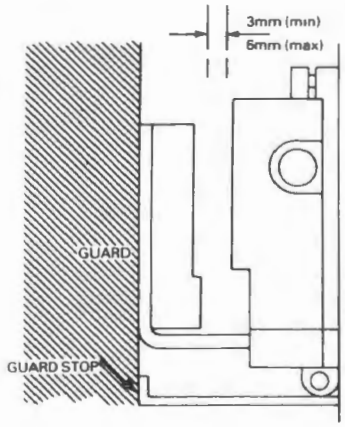
3. Ensure the bottom of the actuator tongue clears the bottom of the switch entry by 1mm (.040") using feeler gauge. Tighten actuator screws.

Important notes

(a) The switch will accomodate inaccuracies in guard or door. The tongue of the actuator should not be used as a guide to align the guard.

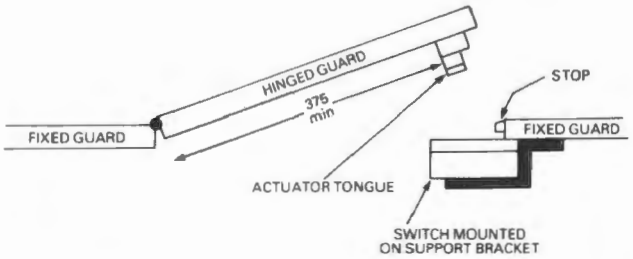
(b) It is essential that the switch is not used as a guard stop. All guards or doors should be fitted with stops (see Figure 6). A gap (3mm min-6mm max) should be allowed between the front of the switch and the magnetic actuator.

Figure 6



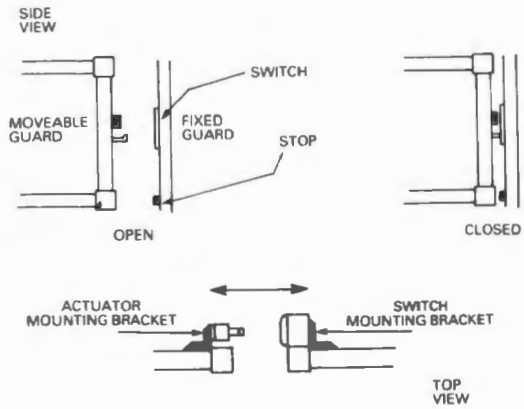
(c) When used on a hinged guard, the switch should be mounted as near as possible to the camb. Minimum mounting distance from the hinge should be 375mm (see Figure 7).

Figure 7



(d) To ensure moveable guards, when closed, are located as close as possible to the fixed guard, the switch should be mounted in a similar manner to that shown in figure 8. i.e. virtually flush with the mounting faces of the guard.

Figure 8



RS data

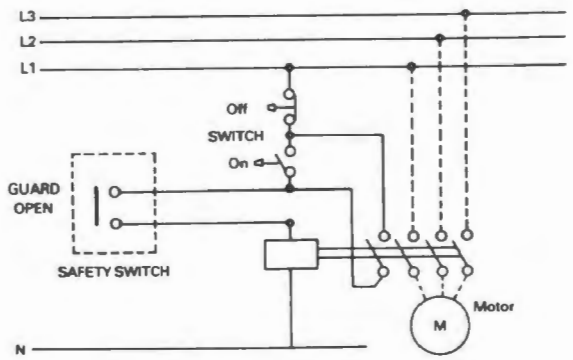
Electrical Installation

After mounting the switch and prior to the installation of the conduit fittings:-

1. Select whether LH or RH cable entry is required.
2. Screw brass bush into selected entry hole and tighten until knockout plate is ejected into switch interior.
3. Remove ejected plate, fit conduit and complete connections (see Figure 9 for typical connection diagram).
4. Replace transparent cover and die cast cover, ensuring that special lid screw is fully tightened.

Note: Should the incorrect knockout be selected and ejected, the nylon blanking plug supplied should be used to re-seal the switch conduit entry.

Figure 9



For alarm contacts: Add interposing fail-safe relay operating auxiliary contacts in alarm circuit.

Maintenance details

The switch requires no regular maintenance, but an occasional application of silicone grease, available from RS, to the operating cam and a periodic inspection of the moving components is recommended.
Cleaning:- The switch may be steam cleaned or pressure hosed with or without the die cast cover open.

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RS data

Pressure transducers

Stock numbers 303-343, 303-337

The RS pressure transducers are gauge type transducers, available in two pressure ranges (0-15 and 0-30 p.s.i.). Suitable for general purpose pressure sensing and measurement. The sensing element in each transducer is a 0.1'' square silicon chip with integral sensing diaphragm and four piezo resistors. When pressure is applied to the diaphragm it causes it to flex, changing the resistance, which results in an output voltage proportional to pressure when a suitable excitation voltage is applied to the device. The sensing resistors are connected as a four active element bridge for best linearity and sensitivity. The linear outputs are complimentary (i.e. as input pressure increases, output A increases and output B decreases).

Features

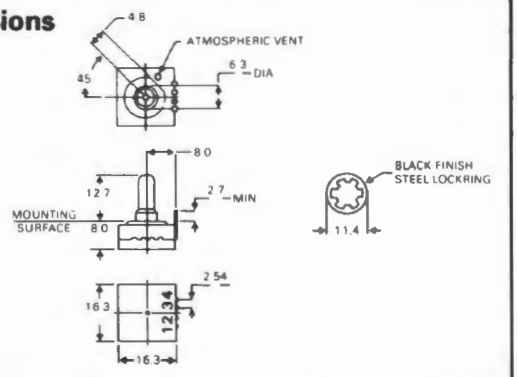
- Miniature package.
- Low cost.
- Low null shift, high sensitivity.
- Linear output proportional to pressure.
- Temperature compensated.
- Low hysteresis.

Absolute maximum ratings

Maximum pressure: 303-343	45 p.s.i.
303-337	60 p.s.i.
Maximum voltage	20V d.c.
Operating temperature range	−55 to +125°C
Soldering temperature, 10 secs	315°C
Mechanical shock	tested to 150g
Vibration, 0 to 2kHz	tested to 20g

Measurand: input media are limited to those which will not attack polyester, silicon, or silicone based adhesives.

Dimensions

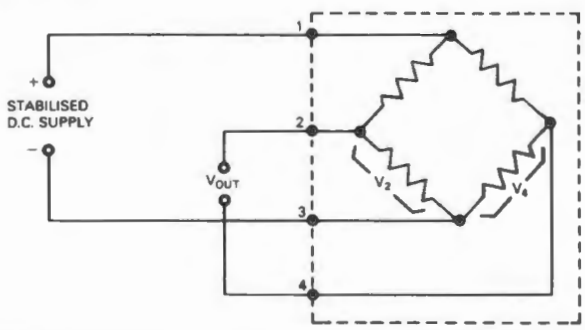


Terminals

1	V_{SS}
2	Output A
3	Ground
4	Output B

Pins have 0.63 square cross section to facilitate wire wrap or solder connections, on 2.54 centres

Electrical connections



$V_{OUT} = V_2 - V_4$
V_{OUT} increases with increase in pressure.

RS data

Electrical characteristics Supply voltage 10.0 ± 0.01 Vd.c. Tamb = 25°C

	303-343			303-337			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Pressure range		0-15			0-30		p.s.i.
F.S.O. (Full scale output)	98.5	100	101.5	75	79	83	mV
Null offset	–1	0	+1	–1	0	+1	mV
Sensitivity		6.67			2.63		mV/p.s.i.
Overpressure			45			60	p.s.i.
Response time			1			1	ms
Recommended excitation voltage		10	16		10	16	Vdc
Linearity (Best fit straight line) Greatest pressure at vent Greatest pressure at port		 ±0.5% ±1.0%			 +0.3% ±0.5%		 F.S.O. F.S.O.
Temperature error 0°C to +50°C Sensitivity shift Null shift		 ±1.5% ±2			 ±1.5% ±2		 F.S.O. mV
Repeatability and hysteresis		0.15%			0.15%		F.S.O.
Stability over 3 years		1.5%			1.5%		F.S.O.
Input resistance		8K			8K		ohms

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RS data

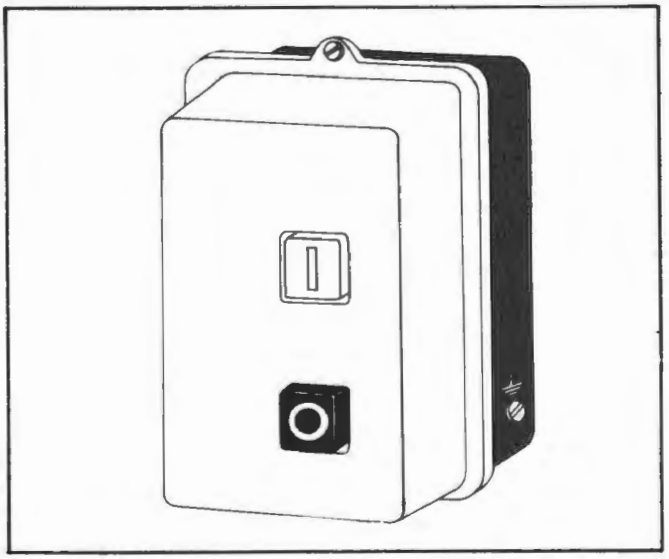
Direct on line (D.O.L.) starter 10 HP 415V. a.c.

Dust and damp protection to IP 55

3 pole direct on line a.c. starters, conforming to BS 4941, IEC 292-1 and VDE 0660, housed in compact enclosures having a high degree of protection to IP55. The starters are available with either 220-250V 50Hz or 380-440V 50Hz operating coils and are supplied with all necessary interconnection links. Overload relays are available separately, and should be selected according to the motor full load current (refer to table below).

Features

- Dust and damp protection to IP55.
- Easily fixed and wired.
- Generous space for connections.
- Heavy gauge steel base.
- Flame retardant A.B.S. lid.
- Wide range operating coils.



Ratings

Max rating — 3 phase connected. 10HP (7.5KW)
single phase connected. 3HP (2.2KW)

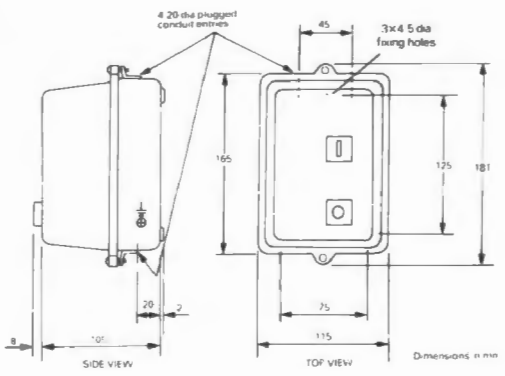
Coil ratings — (stock number **347-028**) 220-250V 50Hz
(stock number **347-012**) 380-440V 50Hz

Full load current table

3 phase		Single phase		Full load current overload relay	Overload relay
415V HP	380V KW	240V HP	220V KW	Min-Max	RS Stock number
0.5	0.37	—	—	0.85-1.3	348-172
0.75	0.55	—	—	1.2-1.9	348-166
1.00	0.75	0.25 0.33	0.18 0.25	1.8-2.8	348-728
1.5 2.0	1.1 1.5	— 0.5	— 0.37	2.7-4.2	348-712
3.0	2.2	0.75	0.55	4.0-6.2	348-706
4.0 5.5	3.0 4.0	1.0	0.75	6.0-9.2	348-699
7.5	5.5	1.5	1.10	8.0-12.0	348-683
10.0	7.5	2.0 3.0	1.50 2.20	11.0-16.0	348-677

RS data

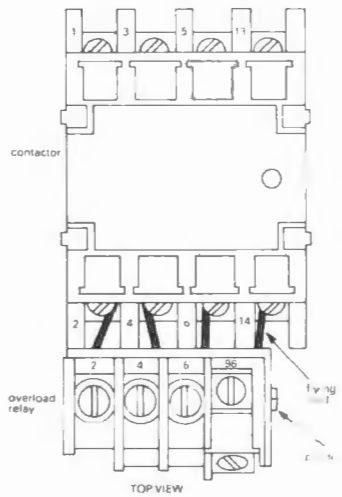
Figure 1 **Dimensions**



Overload relay

The overload relay should be fitted to the contactor in the position as shown in figure 2, the flying lead being connected to terminal number 14 of the contactor. Having chosen an overload relay (using the Full Load Current Table if necessary), the final trip current should be set to the motor full load current using the pointer on the side of the relay.

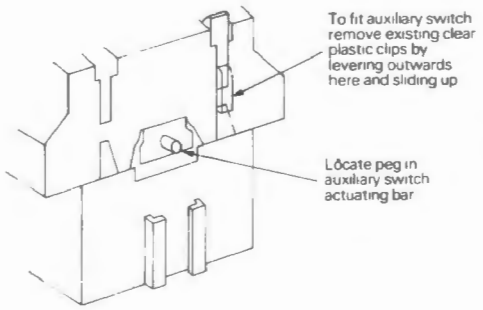
Figure 2 **Overload relay mounting**



Auxiliary switch

Auxiliary switches (337-576) may be fitted by removing the two plastic clips holding the contactor lid, placing a switch on the side so that its actuator fits over the moving side-peg and clipping it in place using the two plastics clips supplied. Two auxiliary switches may be fitted to each contactor. Refer to figure 3.

Figure 3



Connection diagrams

Interconnection links A and B are provided wired to the contactor and should be connected to the overload relay terminals 95 and 96 respectively as shown below.

Figure 4 **Local control 3 phase supply**

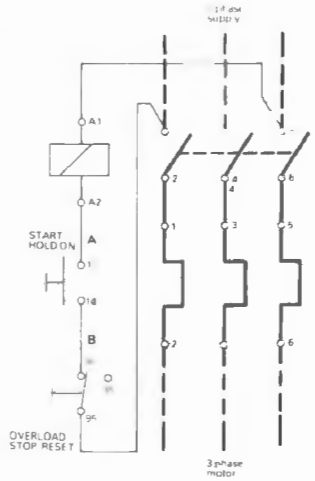
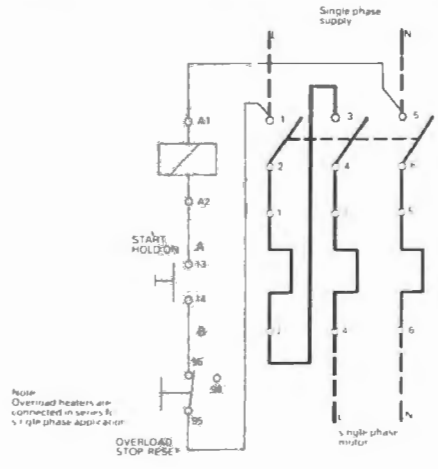


Figure 5 **Local control single phase supply**



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For technical enquiries ring: 01-202 8252 or 0536-201234
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RS data

'Sweet spot'™ fibre optic devices

Stock numbers 303-270, 303-292, 303-309

The RS 'Sweet Spot' opto-electronic components are a range of devices suited to many applications in light sensing and infra-red especially for fibre optics. The unique form of construction uses a glass focusing bead and a clear lens cap to focus or project a narrow beam of radiation which can be easily and efficiently coupled to a wide range of optical fibres.

Absolute maximum ratings

Operating temperature	0°C to + 70°C
Storage temperature	0°C to + 85°C
Pin soldering temperature	240°C for 5 secs max

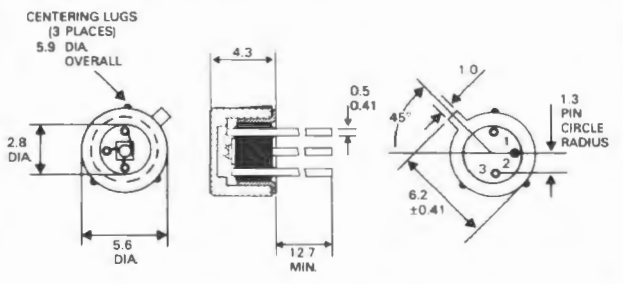
	303-270
Supply voltage	16V
Continuous dissipation	50mW

	303-309	303-292
Forward current	100mA	—
Reverse voltage	1v	50V

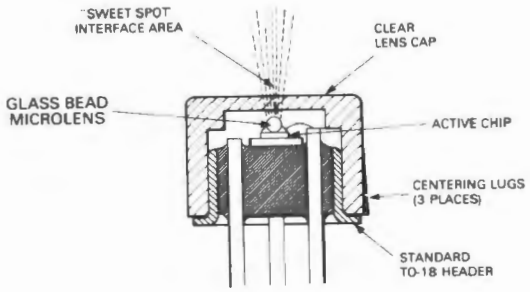
Features

- Low cost solution for fibre optic links
- Plastic cap designed for easy press-fit installation
- Emitter – high radiance, good linearity and fast response
- PIN Photodiode – large active area and wide field of view
- Schmitt Receiver – photodiode integrated with a complete receiver

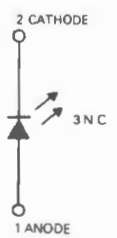
Dimensional information



Cross section through device

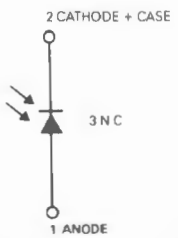


Emitter 303-309



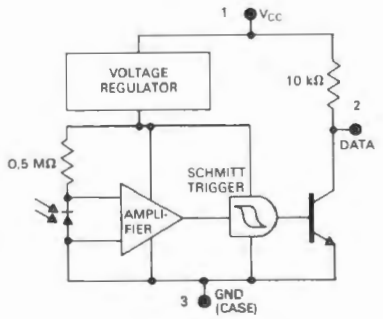
Black spot on can

PIN Photodiode 303-292



White spot on can

Schmitt receiver 303-270



Yellow spot on can

Electro-optical characteristics $T_A = 25°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Emitter 303-309						
Forward voltage drop	V_F	$I_F = 50mA$		1.6	2.0	V
Equivalent series resistance	R_S			1.6		Ω
Device capacitance	C_T	$V_R = 1V$		800		pF
Power output	P_O	$I_F = 50mA$	200	400		μW
Response time	t_r	1V d.c. bias, $I_{PK} = 100mA$		12	20	ns
Peak output wavelength	λ_{PK}	$I_F = 50mA$		820		nm
Spectral bandwidth	$\Delta\lambda$	$I_F = 50mA$		35		nm
Temperature coefficient of V_F	$\Delta V_F/\Delta T$			−1.7		mV/°V
Temperature coefficient of P_O	$\Delta P_O/\Delta T$	$I_F = 50mA$		−0.12		dB/°C
Temperature coefficient of λ	$\Delta\lambda/\Delta T$			0.35		nm/°C
Thermal resistance	θ			500		°c/w
Projected radiation (I.R.) beam		At device window		400		μm
PIN Photodiode 303-292						
Peak response wavelength	λ_{PK}			850		nm
Responsivity		X_{PK} IN = 820nm	0.35	0.45		A/W
Dark current	I_{DK}	$V_R = 5V$		0.1	5	nA
Response Time	t_r	$V_R = 5V$ $V_R = 15V$		30 15		ns ns
Device capacitance	C_T	$V_R = 15V$		3.7		pF
Field-of-View	FoV	3dB points		80		degrees
Temperature coefficient of I_D	$\frac{\Delta I_D}{I_D}/\Delta T$			10		%/°C
Bandwidth					50	MHz
Schmitt Receiver 303-270						
Supply voltage	V_{CC}		4.5		16	V
Data rate			0		200	kbit/s
Input sensitivity		λ_{PK} IN = 820nm		2	5	μW
Field-of-View	F_OV			40		degrees
High level logic output voltage	V_{OH}	$P_{IN} = 10\mu W$, $I_{OL} \geqslant 100\mu A$, $V_{CC} = 5V$	2.4			V
Low level logic output voltage	V_{OL}	$P_{IN} < 0.5\mu W$, $I_{OL} = -16mA$, $V_{CC} = 5V$			0.4	V
Logic output propagation delay time Low-to-High High-to-Low	 $t_{D(L-H)}$ $t_{D(H-L)}$	$V_{CC} = 5V$, $R_L = 390\Omega$		 1.1 3.0		 μs μs
Logic output transition time Low-to-High High-to-Low	 t_r t_f			 80 10		 ns ns
Supply Current	I_{CC}			14		mA

Typical performance curves

Emitter 303-309

Figure 1 **Power output vs d.c. forward current**

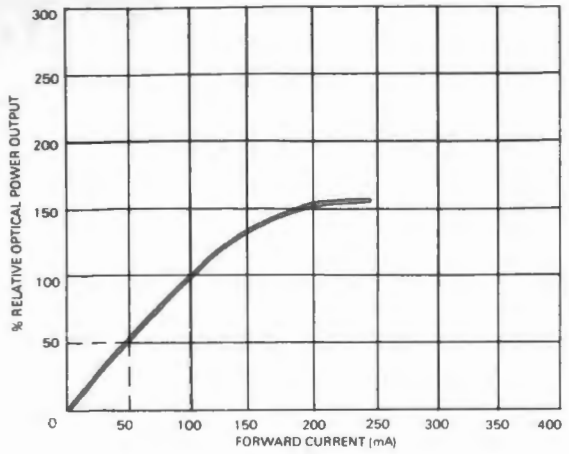


Figure 2 **Forward current V_S forward voltage**

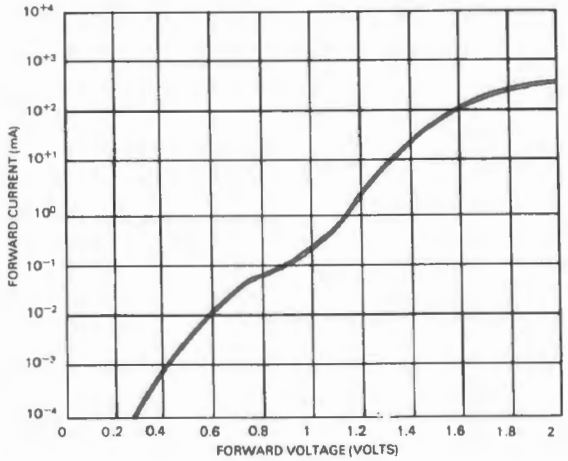


Figure 3 **Radiant intensity vs Polar angle**

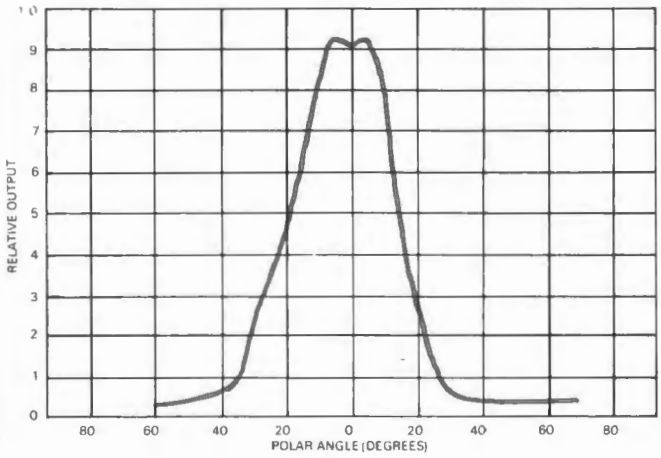
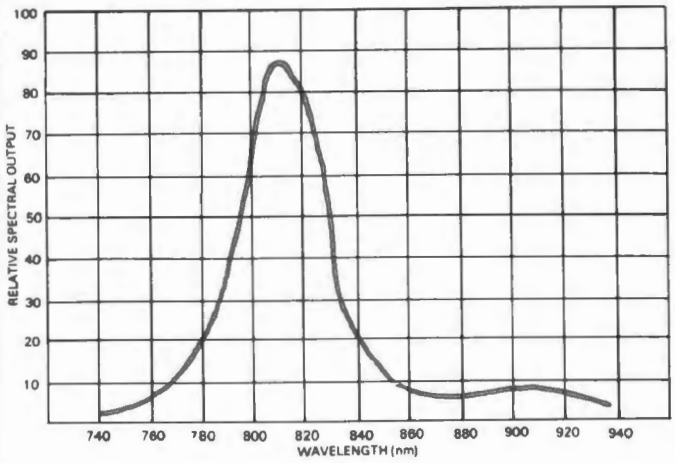


Figure 4 **Spectral output vs wavelength**



PIN Photodiode 303-292

Figure 5 **Typical rise/fall time vs bias voltage**

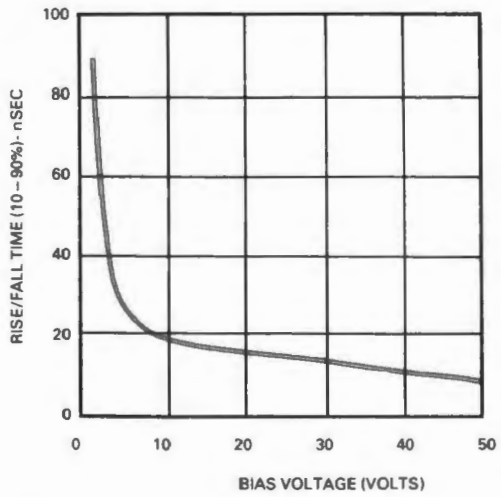
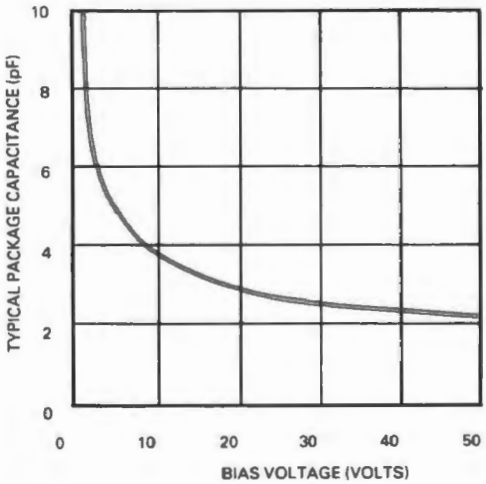


Figure 6 **Typical package capacitance vs bias voltage**



RS data

PIN Photodiode 303-292

Figure 7 **Relative spectral responsivity**

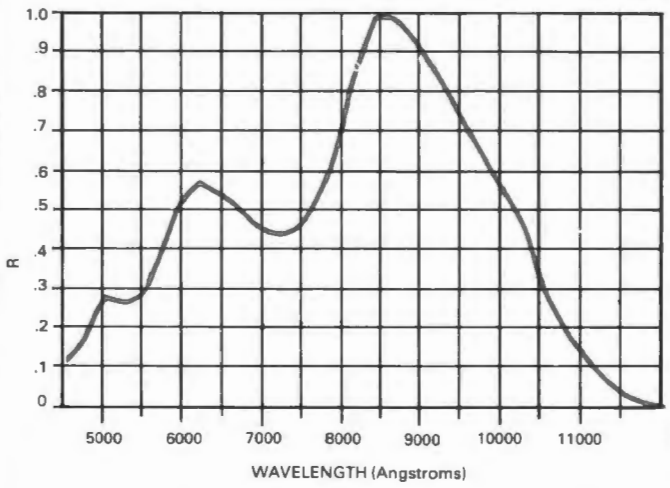
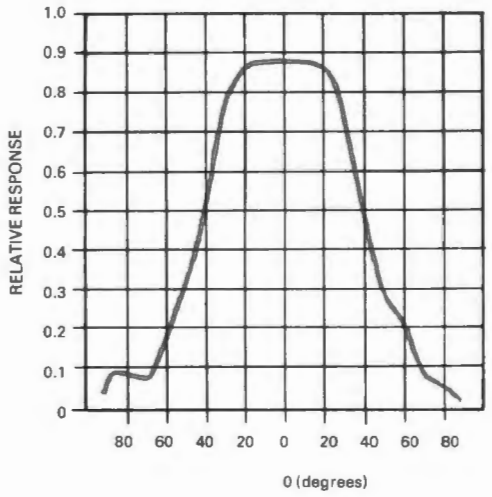


Figure 8 **Typical augular response**



Schmitt receiver 303-270

Figure 9 **Transition/delay times test circuit**

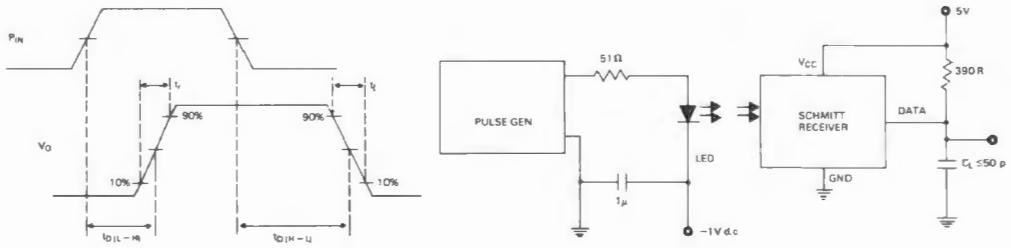


Figure 10 **Directional responsivity**

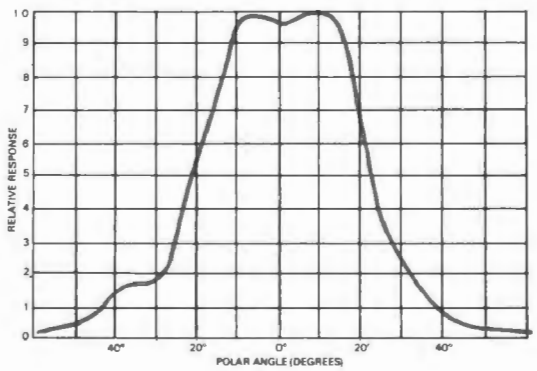
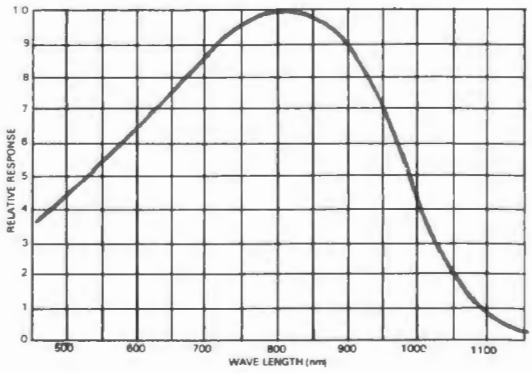


Figure 11 **Spectral responsivity**



R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
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Telephone: 0536 201234
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RS data

Optical communication receiver i.c.

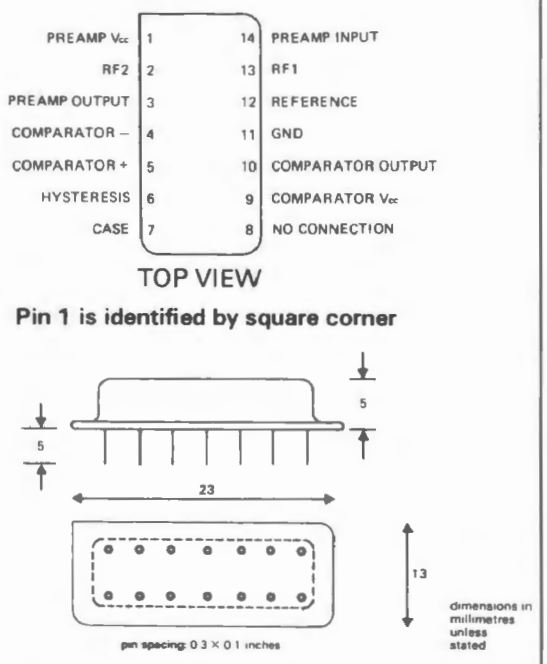
Stock number 303-668

A high-speed transimpedance amplifier and comparator stage on a thick film circuit configured in a 14 pin glass-sealed metal package. The large gain-bandwidth product of the amplifier allows fast response, even with high capacitance photodiodes. The analogue output permits reception of 20 MHz signals, whilst the internal comparator allows 15 Mbit/s NRZ data to be received and converted for C-MOS/TTL compatibility. Equivalent to NS LH0082 CD.

Caution: All handling should be carried out under ANTI-STATIC conditions.

Absolute maximum ratings

Supply voltage	+15 V
Power dissipation, T_A = 25°C	0.5 W
Junction temperature	150°C
Storage temperature	−65°C to +150°C
Operating temperature range	−25°C to 85°C
Lead temperature (soldering, 20 seconds)	300°C
Input current	±10 mA



CAUTION:
ESD (Electro-Static-Discharge) sensitive device

Features

- Ideal for low noise fibre optic links
- Easily integrated into systems design
- 2 GHz gain-bandwidth FET-input amplifier
- Internal voltage reference incorporated
- Internal comparator has 'built-in' hysteresis
- All feedback and coupling components incorporated
- 50 Mbit/s data rate possible with external comparator
- Single 5 V supply operation
- Pin selectable sensitivity and 80 dB dynamic range

Introduction

Before proceeding to a discussion of the Receiver i.c., it is very useful to first of all consider the general design criteria for optical communication receivers.

Optical sensors

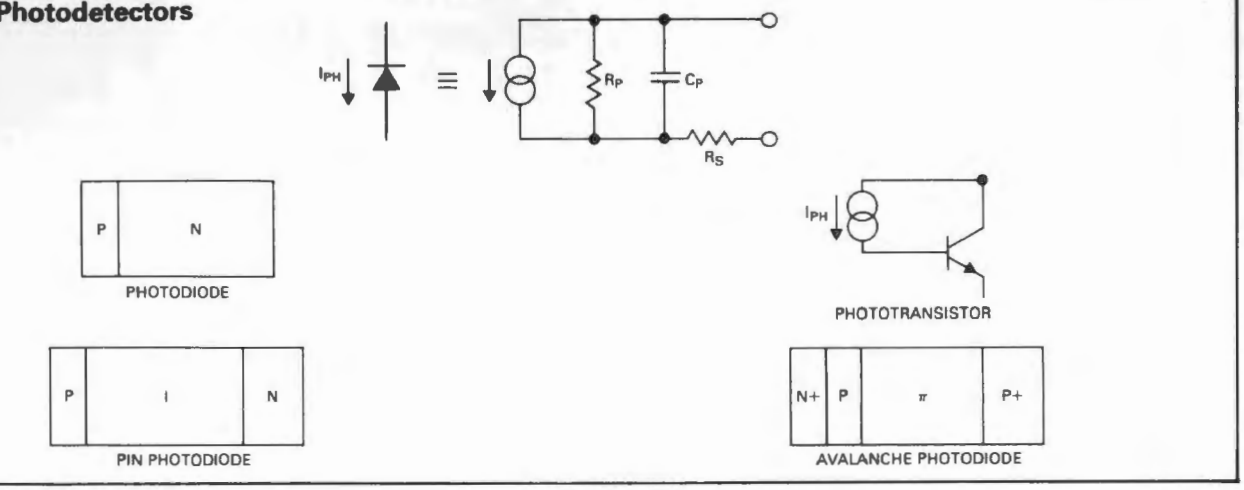
The design of receiver circuitry for fibre optic transmission is an involved topic. First, we will discuss the basic characteristics of the most commonly used photodetectors.

The four most popular photosensors are shown in Fig. 1. The photodiode, phototransistor, PIN photodiode and avalanche photodiode all operate on the same basic principle. An incident photon creates a hole-electron pair near or within the depletion region. The electrical field separates the pair and causes current to flow in an external circuit. Fig. 1 also shows an equivalent circuit for a photodiode. R_S is usually of the order of 10 to 100 ohms, R_p is 10^9 to 10^{10} ohms typically, and C_p is the photodiode's capacitance, dependent upon processing and area. Note the direction of photo-induced current flow, as conventional current is sourced by the anode. This is not the same mode typically used for solar cell operation – the photovoltaic mode. In this mode, a portion of the photocurrent flows through the photodiode itself, producing a voltage from anode to cathode. The photocurrent mode, however, is superior to the photovoltaic mode in linearity, speed of response, stability and temperature coefficient. Thus, we will limit our circuitry discussion to using the photodiode in the photocurrent mode alone.

Electrical characteristics $V_{CC} = 5V$ $T_A = 25°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Preamplifier						
Input bias current	I_B				200	pA
Input capacitance	C_{IN}				5	pF
Voltage gain	A_V		70	90		V/V
−3dB frequency	f_{3dB}			18		MHz
Output quiescent voltage	V_O		2.0	2.1	2.5	V
Temperature drift of V_O	$\Delta V_O/\Delta T$			−6		mV/°C
Output impedance	R_O			15		Ω
Output noise		10 Hz to 10 MHz		300		μV rms
Output swing	V_O	No load	3.5	4.0		V
Transimpedance		Low sensitivity	90	100	110	kΩ
Transimpedance		High sensitivity	0.9	1.0	1.1	MΩ
Supply current	I_S		10	22	30	mA
Comparator reference						
Typical fibre optic receiver						
Comparator input resistance	R_{IN}		0.95	1.00	1.05	kΩ
Hysteresis voltage			7	9	11	mV
Output pull-up resistor	R_O		0.95	1.00	1.05	kΩ
Reference voltage	V_R		2.2	2.4	2.6	V
Temperature drift of V_R	$\Delta V_R/\Delta T$			−2		mV/°C
Reference voltage output impedance	R_O (V_{REF})			15		Ω
Low level output voltage	V_{OL}	$I_{OL} = 3.2$ mA		0.3	0.5	V
High level output voltage	V_{OH}	$I_{OH} = -1$ mA	3.8	4		V
Propagation delay time	T_{PD}	$V_{IN} = 30$ mV		160		ns
Rise time	T_R			80		ns
Fall time	T_F			60		ns
Supply current	I_S	Output high	4.5	8	17	mA
Supply current	I_S	Output low	9.5	13	22	mA
Typical fibre optic receiver		Photodiode: responsivity = 0.5 A/W. bias = −2.5 V, C = 3pF				
Input power for 10^{-9}BER	P_{IN}	500 kbit/s NRZ, $R_F = 1$ MΩ		30		nW
		2 Mbit/s NRZ, $R = 100$ kΩ		300		nW
Analogue output: rise or fall time	t_r, t_f	$R_F = 1$ MΩ		1.5		μs
		$R_F = 100$ kΩ		50		ns
Maximum date rate (NRZ)		$R_F = 1$ MΩ		650		kbit/s
		$R_F = 100$ kΩ		5		Mbit/s
Noise equivalent power	P_N	$R_F = 1$ MΩ		1		nW
		$R_F = 100$ kΩ		10		nW
Equivalent input noise current	i_N	10 Hz to 10 MHz, $R_F = 1$ MΩ		300		pA rms
		10 Hz to 10 MHz, $R_F = 100$ kΩ		3		nA rms
Total supply current	I_S			35		mA

Figure 1: **Photodetectors**



Phototransistor

The phototransistor can be modelled by a photo-induced current source between the collector and the base. Beta multiplication produces a much larger photocurrent at the emitter or collector; however, this is at the expense of speed of response. The small photocurrent must charge the base-emitter capacitance, producing slow rise and fall times. Gain-bandwidth is typically 200 MHz. The uncertainty in sensitivity due to beta variations, and the slow response relegate the phototransister to relatively low performance fibre optic receivers.

PIN photodiode

The PIN photodiode enhances the conventional photodiode's utility by producing the same amount of photocurrent from a lower capacitance source, thus giving higher speed operation. In normal operation, the entire intrinsic region is depleted, thus spreading apart the 'plates' of the capacitor. Frequency response is typically to 1 GHz.

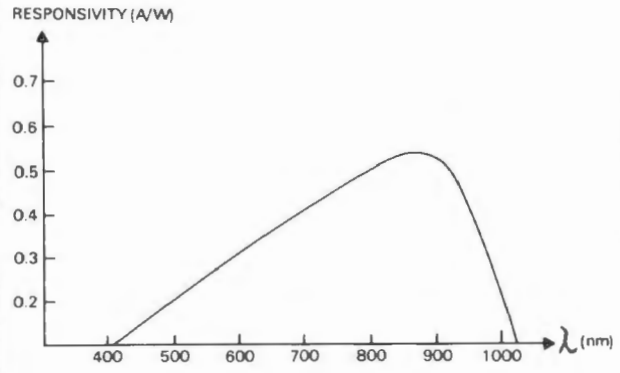
Avalanche photodiode

The avalanche photodiode requires 150 to 300 volts of reverse bias to operate. Photo-induced carriers are swept into a high field region where avalanche multiplication takes place. This produces front-end signal gain (50–500) without paying a speed penalty. Gain-bandwidth product of an avalanche photodiode is in the neighbourhood of 100 GHz. The drawbacks to avalanche photodiodes are the high bias voltage needed, and the temperature compensation necessary for stable operation.

Responsivity

A photodiode's most fundamental characteristic is its responsivity, i.e., the amount of current it will produce in response to the incident light power. Responsivity is given in amperes per watt. Fig. 2 illustrates a typical responsivity versus wavelength for a silicon photodiode. The responsivity drops below 900 nm due to absorption, and above 900 nm due to the band gap of silicon (1.2 eV). A similar graph could be shown for a phototransistor or an avalanche photodiode. The y-axis would simply be multiplied by beta or the avalanche gain respectively. Note that when the incident light is measured in watts, the area of the detector does not play a part in the quantity of current produced. A photodiode whose responsivity at a given wavelength is 0.5 will produce 1 μA in response to an incident light power of 2 μW as long as all of the light falls on the photodiode's sensitive area.

Figure 2: **Typical photodiode responsivity**



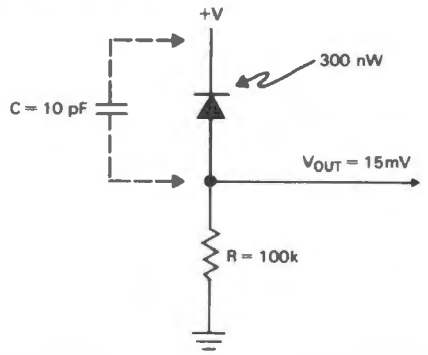
Receiver circuitry

The most challenging aspect of many fibre optic links is the design of the receiver. The receiver must convert the low level current output of a photodiode to a high level analogue or digital signal with accuracy and speed.

Fig. 3 illustrates the simplest of fibre optic receivers. The photodiode is back biased with a resistor to convert the photo-induced current to a voltage. Let us assume that we want to convert an input light power of 300 nW to a 15 mV signal. If the photodiode's responsivity is 0.5 A/W, then the photodiode will produce 150 nA, and for a 15 mV signal level, the resistor must be 100 k. If the capacitance of the photodiode is 10 pF, then the rise time of the voltage output in response to a step light input will be approximately 2.2 μs (t_r = 2.2 RC). This also implies that our analogue bandwidth is limited to a −3 dB frequency of 159 kHz. (Since ω = 1/(RC), where $\omega = 2\pi f$.)

How is it possible to obtain higher frequency performance at the same sensitivity without sacrificing signal-to-noise ratio? Decreasing the size of the resistor and using voltage amplifiers can achieve the same responsivity at a higher speed but it will sacrifice signal-to-noise ratio since a resistor's noise current contribution increases as the value of the resistor decreases. (This is because $i_n = \sqrt{4KTB/R}$). As we will see later, signal-to-noise is not only important for analogue communication, but also sets the limiting bit error rate for digital signalling.

Figure 3: **Simple receiver**



A single circuit topology can be practically applied in two ways to help us out. Fig. 4 illustrates the general topology, with the first of the two specific implementations shown below. This is known as the bootstrap configuration as the function of the amplifier is to chase the voltage developed by the photocurrent flowing through the resistor, and to apply this voltage to the opposite end of the photodiode. By keeping the voltage change across the photodiode's capacitance small, the effect of this reactance is reduced, and the circuit will respond faster. By rearranging the general topology once again, we arrive at the second implementation, known as the transimpedance approach as shown in Fig. 5. Since the negative input of the amplifier can be considered a virtual ground, the voltage change across the photodiode's capacitance is kept small and thus its effect is reduced. The choice between either of the two approaches is left to the designer; however, the constraints placed on either of the amplifiers are the same when speed of response is used as the criterion.

To give us an idea of how fast an amplifier we need to produce the desired speed of response, we will analyze the transimpedance circuit of Fig. 6. We first define a time constant t that is equal to the product of the feedback resistor and lumped circuit capacitance C. C is the sum of stray capacitance, amplifier input capacitance and photodiode capacitance. The only other parameter to define is t_A, the inverse of the gain-bandwidth product of the amplifier. When we solve this simple circuit analysis problem we find that the rise time of V_{OUT} is:

$$t_R = \pi \sqrt{t \cdot t_A}$$

$$t = RC,\ t_A = \frac{1}{2\pi(GBW)}$$

Rise time is chosen as the prime indicator of circuit speed performance as it allows us to make rapid calculations of the maximum bit rate for a digital communications link. The equation given above is an approximation as it assumes that the open loop gain of the amplifier is greater than 10 and $t < 2A_O t_A$, where A_O is the open loop gain of the amplifier.

Returning to our original problem, how fast must our amplifier be to produce the desired overall fibre optic receiver speed? Let us use a specific example to determine the required amplifier speed. Suppose that we want to receive a 5 Mbit NRZ signal, our feedback resistor is 100k, and the circuit capacitance is 5.5pF. From the data rate, we know that the rise time of the receiver must be 100ns or less. Rearranging the above equation, we obtain:

$$\frac{1}{t_A} = \frac{\pi^2 t}{t_r^2}$$

Figure 4: **Bootstrapped amplifier**

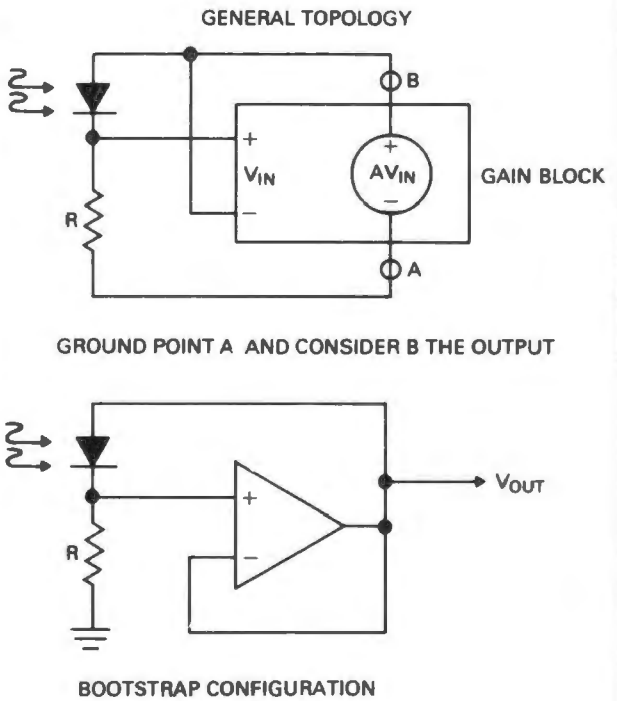


Figure 5: **Transimpedance amplifier**

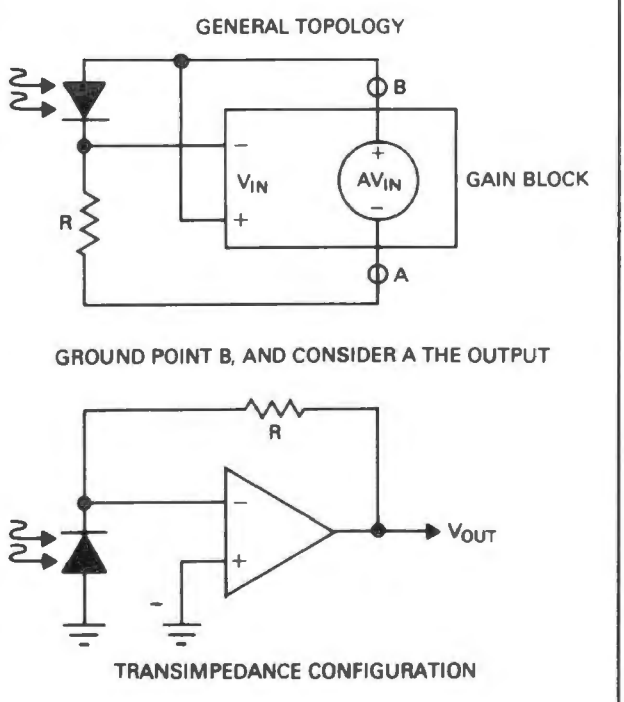
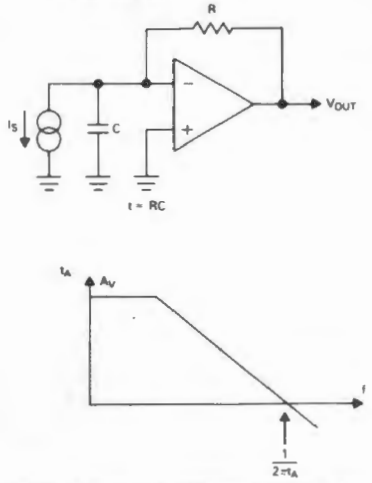


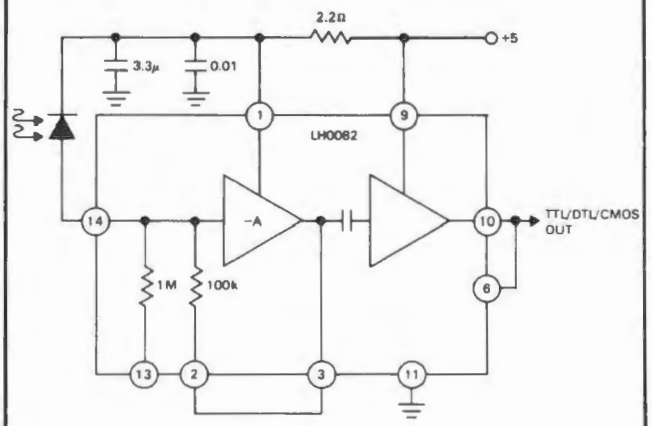
Figure 6: **Equivalent circuit and amplifier characteristic**



When we plug in the numbers, we find that the gain-bandwidth of the amplifier must be 86 MHz! It's obvious that a 741-type amplifier with a gain-bandwidth of 1 MHz will not even come close to providing the speed we need. Fortunately, the LH0082 fibre optic receiver contains a preamp with a gain-bandwidth product of nearly 2 GHz. The LH0082 will provide the sensitivity and speed necessary for the example application, and it also includes a comparator for providing a TTL/DTL/C-MOS compatible output. Fig. 7 is a block diagram of the LH0082. Two internal feedback resistors are included for use with the preamp to set sensitivity. External resistors can also be used. The output of the preamp is a.c. coupled to a comparator that can be connected as an edge triggered flip-flop. In this mode, the bit error rate can be set by the amount of hysteresis applied to the comparator. Using the internal hysteresis resistor, the bit error rate is better than 10^{-10}. The entire circuit operates from a single 4.5 to 5.5 volt power supply, although the preamp can be operated to 10 volts, and the comparator to 15 volts.

Fig. 8 shows how to use the LH0082 as a 5Mbit/s, 300 nW sensitivity fibre optic receiver. The only external components needed are the photodiode, a power supply decoupling resistor and two bypass capacitors.

Figure 8: **LH0082 basic operating circuit – 300 nW, 5 Mbit/s**



Bit error rate

The bit error rate (BER) is a very important consideration in any digital communications system: fibre optic data links are no exception. A BER of 10^{-10} means that one bit of 10 billion will be a bad bit. Obviously, the smaller the BER, the better off we are. There is a very simple relationship between the signal-to-noise ratio and the bit error rate. Given δ as the RMS noise voltage, A as the peak-to-peak signal level, and we determine the presence of one or a zero with a threshold of A/2, then the BER is:

$$BER = \tfrac{1}{2}\left(1 - \text{erf}\,\frac{A}{2\sqrt{2}\,\delta}\right)$$

$$\text{Where: erf}\,(x) = \frac{2}{\sqrt{\pi}}\int_0^x e^{-y^2}dy$$

Fig. 9 is a plot of this somewhat obtuse function. Note that we are guaranteed a BER of 10^{-10} with only 22 dB of signal-to-noise ratio. Thus, if we have a comparator threshold of 10 mV a peak signal level of 20 mV, then the RMS noise must be less than 1.6 mV to give us 10^{-10} BER.

Figure 7: **LH0082 circuit diagram**

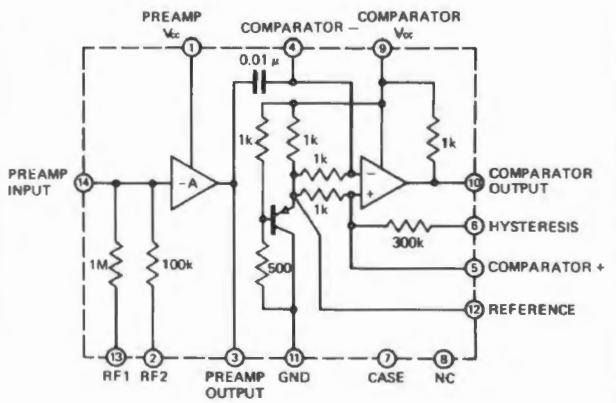
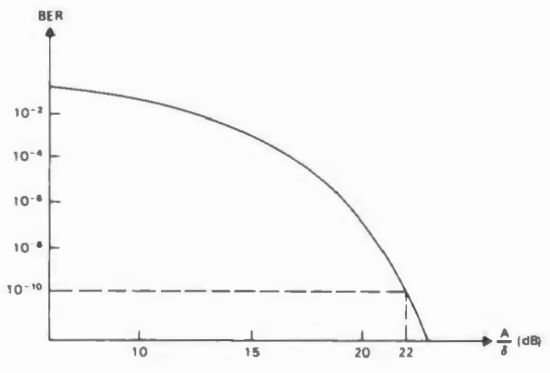


Figure 9: **Bit error vs. signal-to-noise ratio**



Stray signal pick-up problems

Although communication via fibre optic cable provides freedom from the effects of radio frequency interference, the circuitry at the receiver is not so fortunate. Let's take the example of the basic LH0082 300 nW sensitivity receiver. Assuming a 0.5 A/W photodiode, the LH0082 requires only 150 nA at its input to cause the comparator to switch states. Suppose that the output of a TTL gate is nearby and at that point the voltage can traverse 3 V in as little as 5 ns. How much stray capacitance from this TTL output to the input of the LH0082 is needed to equal the signal level generated by the photodiode?

$$\text{Since } I = C\frac{dv}{dt}$$

$$\text{Then } C = \frac{I}{dv/dt}$$

$$\text{i.e. } C = \frac{(150\,\text{nA})\,(5\,\text{ns})}{3\text{V}}$$

$$\text{Thus } C = 2.5 \times 10^{-16}\,\text{F or .00025 pF!!!}$$

Although this may seem like an impossibly small amount of capacitance to live without, straightforward printed circuit board layout techniques can provide trouble-free operation.

A complete link

Putting together a total link is not so difficult as much literature would have you believe. We can be almost careless in our handling of the transmitter circuitry, light coupling to transducers, and connecting the cable. The expense is a little care at the receiver end.

Fig. 10 gives a sample application ideally suited to fibre optics. A data entry room is located 300 metres from a computer facility, separated by a manufacturing area containing arc welders, punch presses and so on. One-way communication from the three data entry terminals to the computer is required at 19.2 kbit/s. Let us assume that we will multiplex the three data channels with one sync. channel and send the signal through one fibre optic cable, and demultiplex the signal at the computer end. We will sample each of the three data channels and the sync. channel at 5 times the data rate or $4 \times 19.200 \times 5 = 384$ kbit/s data rate. We will select an inexpensive red indicator LED whose total output power is only 30 μW or −15 dBm. We must now account for all of the losses involved in transferring this light to the photodiode at the receiving end:

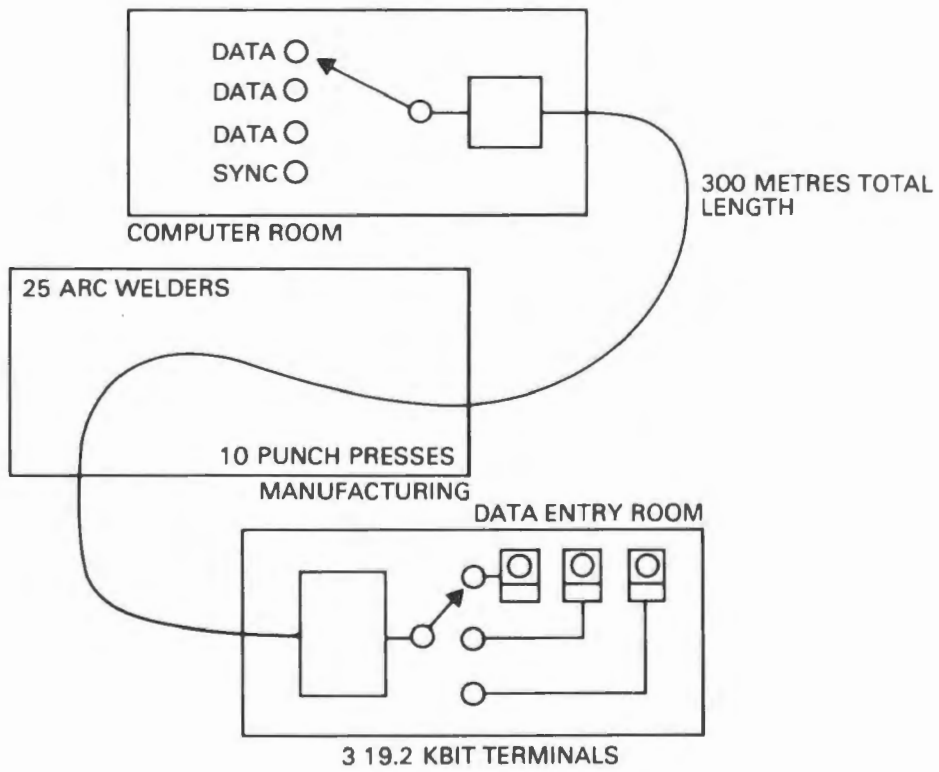
LED-transmitter connector:	−10 dB
receiver connector:	−3 dB
$300 \times \frac{40}{1000}$ dB (cable):	−12 dB
'Safety' factor:	−3 dB
Total loss =	−28 dB

Thus, the power at the receiver is:

$$-15\,\text{dBm} - 28\,\text{dB} = -43\,\text{dBm}\ (50\,\text{nW})$$

The LH0082 in the high sensitivity mode ($R_F = 1$M) has a 30 nW sensitivity with a 0.5 A/W photodiode and can provide a maximum data rate of 650 kbit/s. The use of low cost connectors, poor coupling of light to the transmitter end, and inexpensive moderate loss cable (40 dB/km) does not prohibit a high performance data link when used with a versatile receiver such as the LH0082.

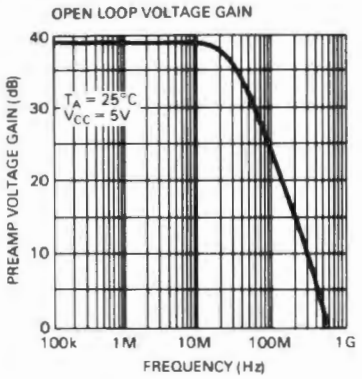
Figure 10: **Typical system**

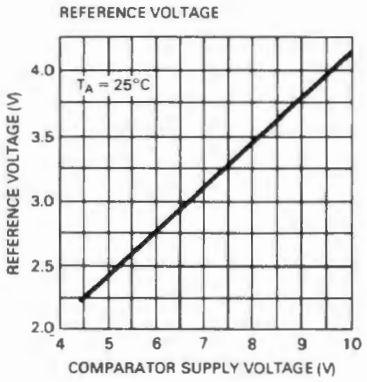


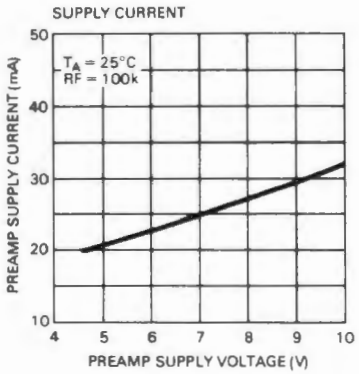
Additional device data

These graphs give additional data to enable designers to optimise their circuits.

Figure 11a: **Additional characteristics**







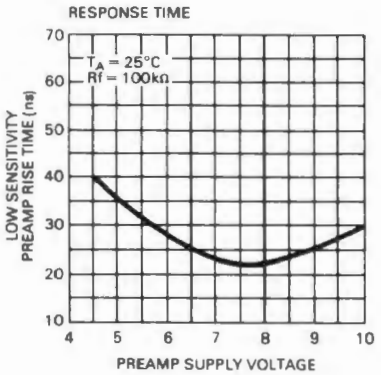
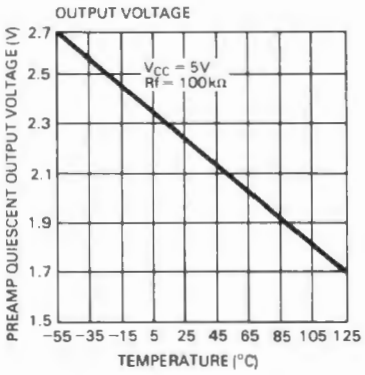
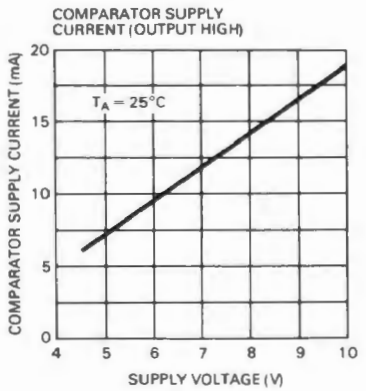
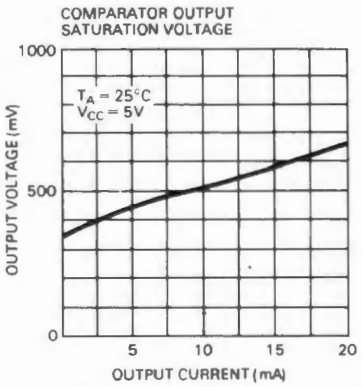
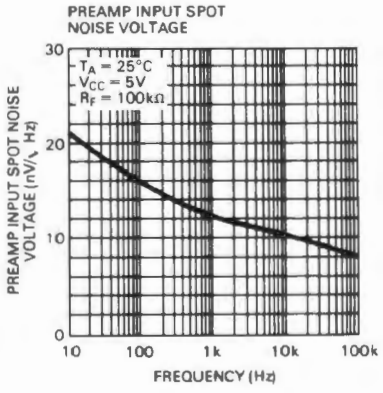


Figure 11b: **Additional characteristics**









RS data

Applications circuits

The following circuits show how the LH0082 may be used to achieve various design objectives

Figure 12: **Fibre optic receiver basic high sensitivity: 30 nW, 650 kbps**

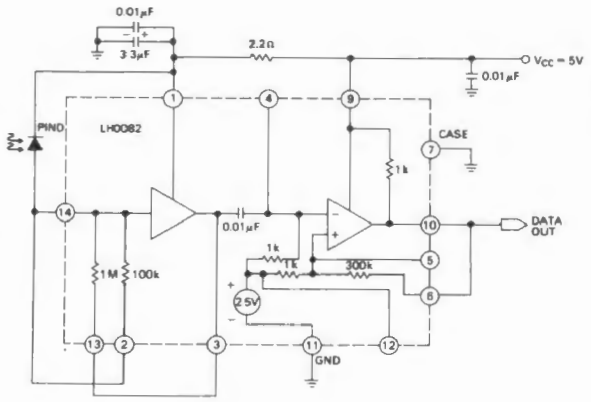


Figure 13: **Fibre optic receiver basic low sensitivity: 300 nW, 5 Mbit**

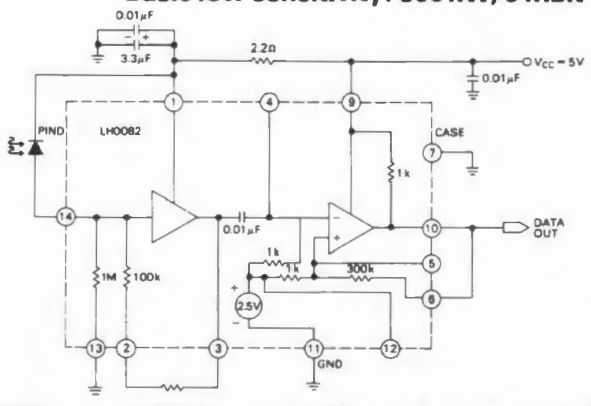


Figure 14: **Phototransistor connections**

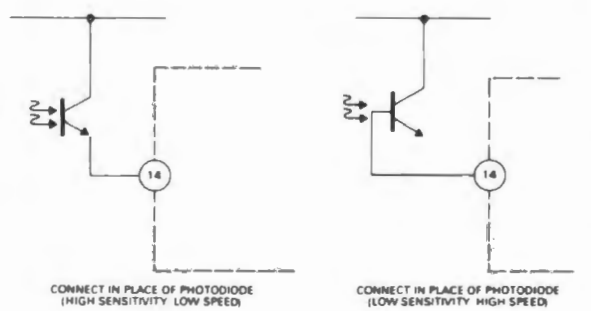


Figure 15: **Fibre optic receiver very high sensitivity – low speed: 3 nW, 100 kbit/s**

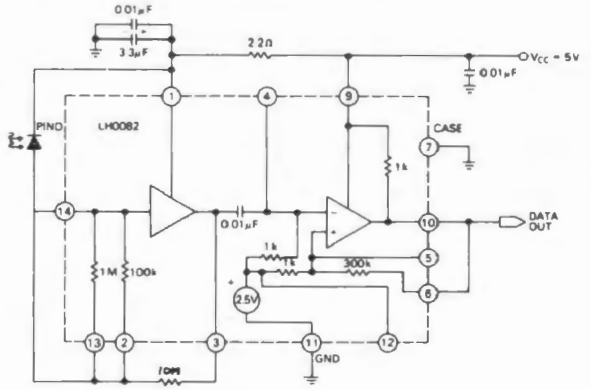


Figure 16: **Fibre optic receiver high sensitivity – improved speed**

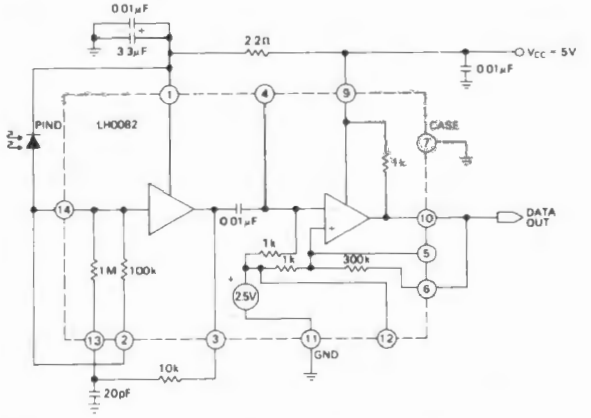
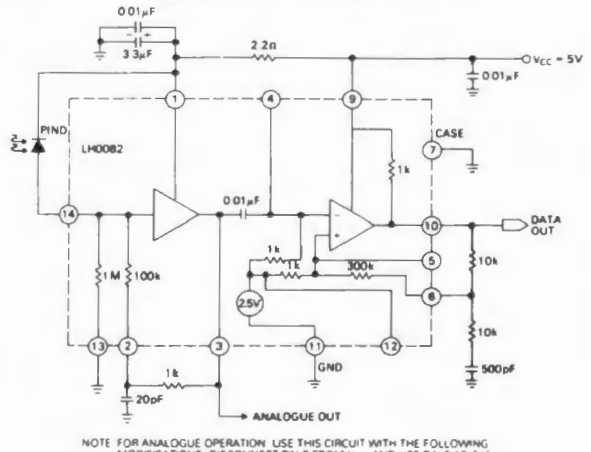


Figure 17: **300 nW sensitivity, 15 Mbit**



NOTE FOR ANALOGUE OPERATION USE THIS CIRCUIT WITH THE FOLLOWING MODIFICATIONS. DISCONNECT PIN 9 FROM V+ AND USE PIN 3 AS THE OUTPUT. BANDWIDTH FOR THE CONFIGURATION IS APPROXIMATELY 20MHz. ANALOGUE RESPONSIVITY IS 50mV µW. DYNAMIC RANGE >= 18

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Compander i.c. RS571

RS data

Stock number 303-242

The RS571 is a versatile dual channel gain control circuit in which either channel may be used as a dynamic range compressor or expander. Each channel has a full wave rectifier to detect the average value of the signal, a linearised, temperature-compensated, variable gain cell, and an operational amplifier. Applications include high level limiters, low level expanders (noise gates), dynamic noise reduction systems, voltage controlled amplifiers, dynamic filters, etc.

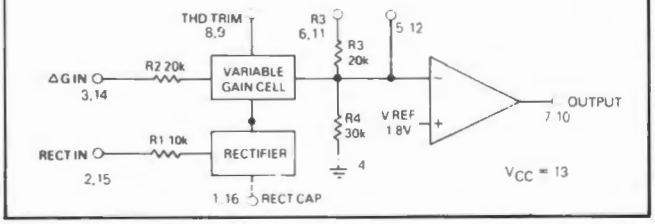
Features

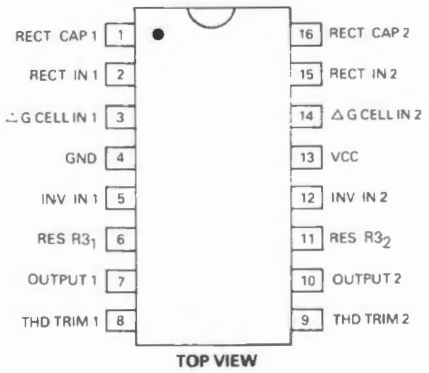
- Completed compressor and expander in one integrated circuit.
- Temperature compensated.
- Greater than 110dB dynamic range.
- Operates down to 6Vdc.
- System levels adjustable with external components.
- Distortion may be trimmed out.

Absolute maximum ratings

Positive supply ——— 18 Vdc
Operating temperature range ——— −40 to +70°C
Power dissipation ——— 400 mW

Block diagram (one half)





Electrical characteristics (T_A=25°C, V_{CC}=15 V)

Parameter	Test Conditions	Min	Typ	Max	Unit
Supply voltage V_{CC}		6		18	V
Supply current I_{CC}	No signal		3.2	4.0	mA
Output current capability		±20			mA
Output slew rate			±0.5		V/µs
Gain cell distortion	Untrimmed		0.5	2.0	%
	Trimmed		0.1		%
Resistor tolerance			±5	±15	%
Internal reference voltage		1.65	1.8	1.95	V
Output dc shift[2]	Untrimmed		±30	±100	mV
Expander output noise	No signal, 20Hz-20kHz		20		µV
Unity gain level		−1.5	0	1.5	dBm
Gain change[1,3]	−40°C<T<70°C		±0.1	±0.5	dB
	0°C<T<70°C		±0.1	±0.4	dB
Reference drift[3]	−40°C<T<70°C		+2, −25	+20, −50	mV
	0°C<T<70°C		±5	±20	mV
Resistor drift[3]	−40°C<T<70°C		+8, −0		%
	0°C<T<70°C		+1, −0		%
Tracking error[4]	Rectifier input=				
	+6dBm		±0.2		dB
	−10dBm		+0.2	−0.2, +0.5	dB
	−20dBm		+0.2	−0.4, +0.7	dB
	−30dBm		+0.2	−1, +1.5	dB
	−40dBm		+0.2, −0.4		dB

Notes
1. Measured at 0dBm 2. Expander ac input change from no signal to 0dBm 3. Relative to value at T_A=25°C 4. Relative to 0dBm

Circuit description

The RS571 compander building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system.

Full wave rectifier

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|ave}{R_1}$$

or for capactively coupled voltage inputs

$$G \propto \frac{|V_{IN}|ave}{R_1}$$

The speed with which the gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})e^{-t/\tau} + G_{final}$$

where $\tau = 10k \times C_{RECT}$

Variable gain cell

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the △G input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op. amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2}$$

or for capacitively coupled circuits

$$I_{IN} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the △G cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

Operational amplifier

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the △G cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expander gain to be determined only by internal components. The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load.

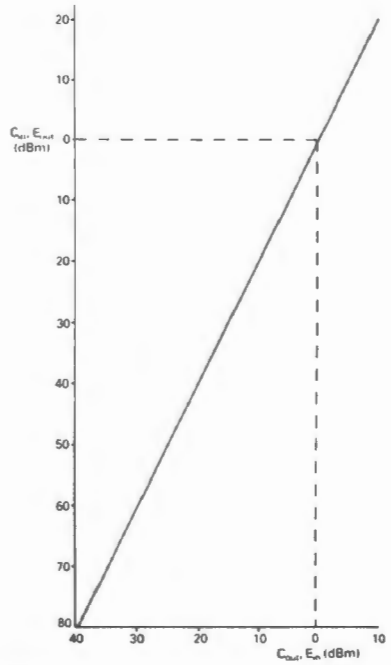
Band gap reference

A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and △G cell, and a bias current for the △G cell. The low temperature coefficient of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.

Figure 1: **Compression/expansion characteristic of the RS571**

Compressor input levels along the vertical axis correspond to output levels along the horizontal axis; expander input levels along the horizontal axis correspond to output levels along the vertical axis.

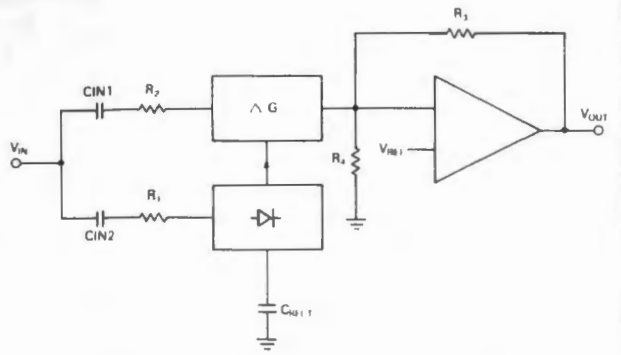


Applications

Basic expander

Figure 2 shows how the circuit would be connected for use as an expander.

Figure 2: **Basic expander**



Both the rectifier and the △G cell inputs are tied to V_{IN} so that the gain is proportional to the average value of V_{IN}. Thus when V_{IN} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the expander gain is

$$G_{exp}=\frac{2R_3V_{IN}ave}{R_1R_2I_B}$$

where I_B=140μA, the bias current derived from the band gap voltage reference.

The maximum input that can be handled by the circuit in Figure 2 is a peak of 2V. The rectifier input current can be as large as $I=2V/R_1=2V/10k\Omega=$ 200μA. The △G cell input current should be limited to $I=2V/R_2=2V/20k\Omega=100\mu A$. If it is necessary to handle larger input voltages than 0 to ±2V peak, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

If low-level tracking accuracy is not important, it is not necessary to use both of the input capacitors shown in Figure 2. If R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the △G cell summing node and the rectifier summing node because of offset voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

The output of the expander is biased up to 3V by the dc gain provided by R_3, R_4. The output will bias up to

$$V_{OUT\ dc}=\left(1+\frac{R_3}{R_4}\right)V_{REF}$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to $\frac{1}{2}V_{CC}$.

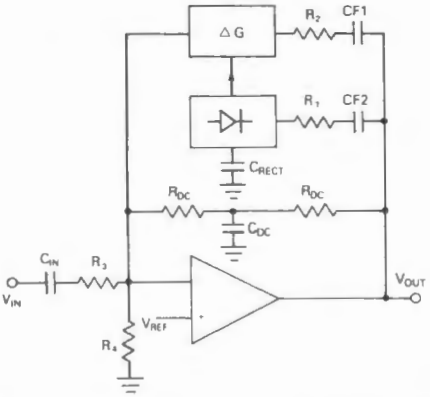
Note that it is possible externally to increase R_1, R_2 and R_3 and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased.

To obtain the largest dynamic range from this circuit, the rectifier input should always be as large as possible (subject to the ±200μA peak current restriction).

Basic compressor

Figure 3 shows how to use the RS571 as a compressor.

Figure 3: **Basic compressor**



It is just an expander in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. This is so because the 3dB increase in output level produces a 3dB increase in gain in the △G cell, yielding a 6dB increase in feedback current to the summing node. The exact expression for gain is

$$G_{comp}=\left(\frac{R_1R_2I_B}{2R_3V_{IN}ave}\right)^{1/2}$$

The same restrictions as to rectifier and △G cell maximum input current still hold, which places a limit on the maximum compressor output. As in the expander, the rectifier and △G cell inputs could be made common to save a capacitor, but low-level tracking accuracy would suffer. Since there is no dc feedback path around the op amp through the △G cell, one is provided by the pair of resistors R_{dc}. The op amp output will bias up to

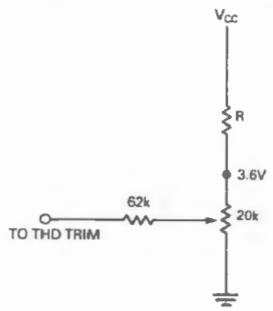
$$V_{OUT\ dc}=\left(1=\frac{2R_{dc}}{R_4}\right)V_{REF}$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the ±200µA peak-current restriction). If the input signal is small, a large output can be produced by reducing R_3, with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

Distortion trim

Distortion can be produced by voltage offsets in the △G cell. The distortion is mainly even harmonics, and drops with decreasing input signal (input signal meaning the current into the △G cell). The THD trim terminal provides a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 4 is suitable, as would be any other capable of delivering ±30µA into a 100Ω resistor tied to 1.8V.

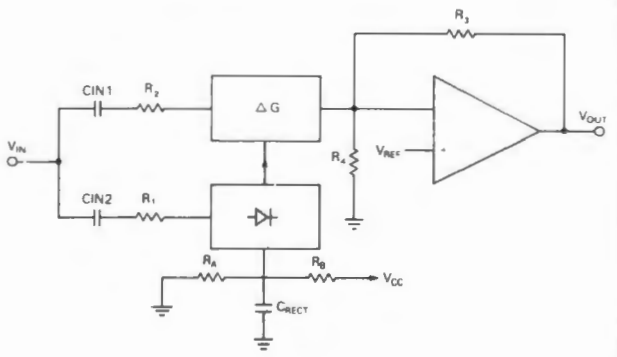
Figure 4: **Offset voltage compensation network for trimming out harmonic distortion.**



Low-level tracking

The expander will follow a 2:1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias <100nA that produces errors at low levels. The magnitude of the error can be estimated. For a full scale rectifier input signal of ±200µA, the average intput current will be 127µA. When the input signal level drops to a 1µA average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

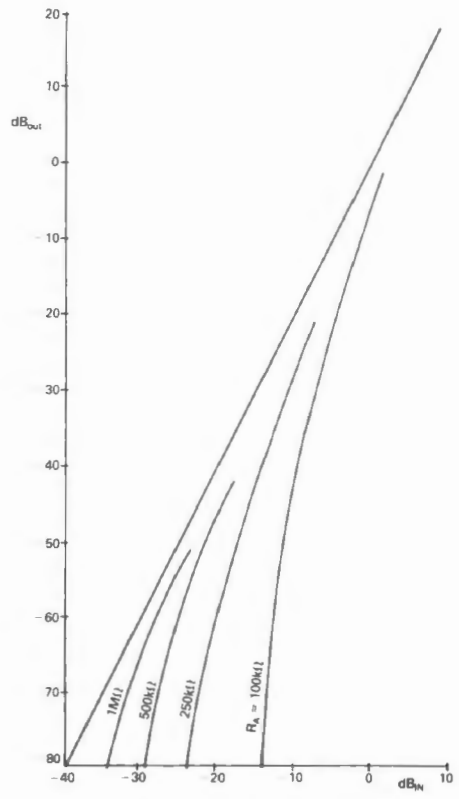
Figure 5: **Alternative resistors R_A, R_B for modifying low-level tracking.**



It is possible to deviate from the 2:1 transfer characteristic at low levels as shown in the circuit of Figure 5. Either R_A or R_B (but not both) is required. The voltage on C_{RECT} is 2 x V_{BE} plus V_{IN} ave. For low-level inputs V_{IN} ave is negligible, so we can assume 1.3V as the bias on C_{RECT}. If R_A is connected from C_{RECT} to earth, it will bleed off a current $I=1.3V/R_A$. If the rectifier average input current is less than this, there will be no gain-control to the △G cell, so its gain will be zero and the expander output will be zero. As the input level is raised, the input current will exceed $1.3V/R_A$ and the expander output will become active. For large input signals, R_A will have little effect, but the 2:1 expansion ratio present at high levels will increase to an infinite ratio at low levels where the output shuts off completely.

Figure 6 shows some examples of tracking curves that can be obtained.

Figure 6: **Effect of resistor R_A on low-level tracking of an expander.**

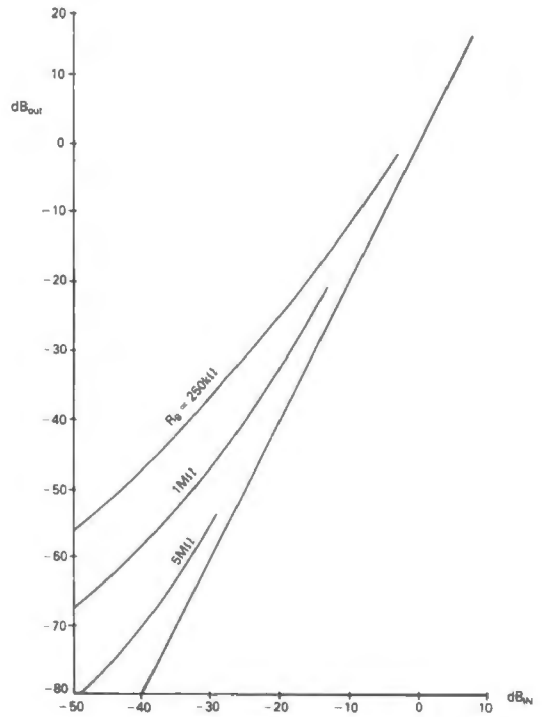


Complementary curves would be obtained for a compressor, where at low signal levels the result would be infinite compression. The bleed current through R_A will be a function of temperature because of the two V_{be} drops, so the low-level tracking will drift with temperature. If a negative supply is available, it would be desirable to tie R_A to that, rather than earth, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{be} temperature drift.

The alternative resistor R_B will supply an extra current to the rectifier equal to $(V_{CC}-1.3V)/R_B$. In this case, the expander transfer characteristic will deviate towards 1:1 at low levels so that the gain will flatten out and expansion will cease. (In a compressor there would be a lack of compression at low levels.)

Figure 7 shows some typical transfer curves.

Figure 7: **Effect of resistor R_B on low-level tracking of an expander.**



Attack and decay times

The attack and decay times of the compander are determined by the rectifier filter time-constant R_1C_{RECT}. Figure 8 shows how the gain changes when the input signal undergoes a 10, 20 or 30dB change in level. The attack is much faster than the decay, which is desirable in most applications.

Figure 8: **Gain change as a function of time (normalized with respect to rectifier time-constant) for input signal level changes of 10, 20 and 30dB.**

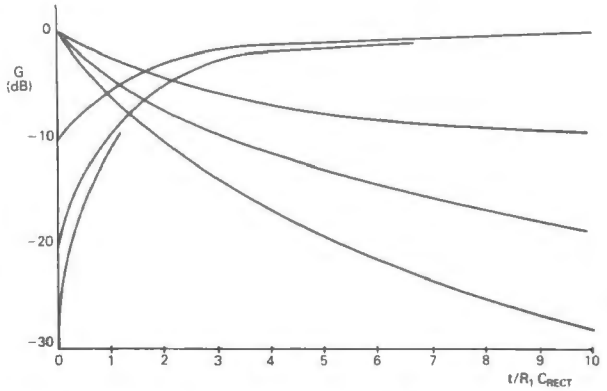


Figure 9 shows the compressor attack envelope for a +12dB step in input level. The output immediately rises to four times then declines towards a final value of twice the initial level.

Figure 9: **Compressor attack envelope for +12dB input step.**
Vertical axis, relative output signal amplitude.

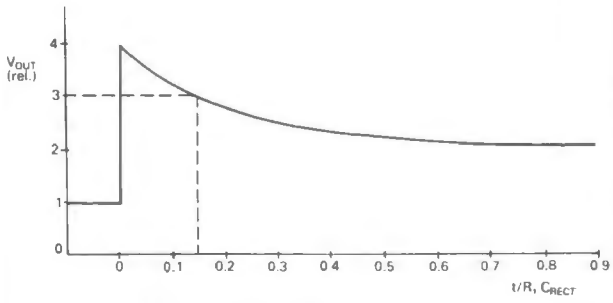
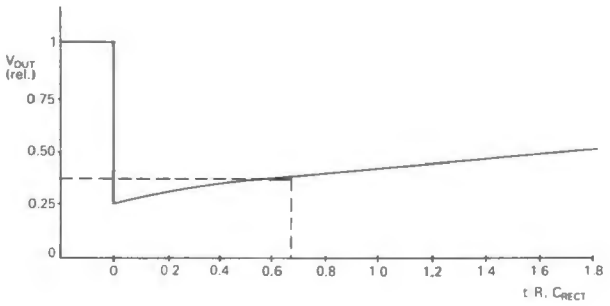


Figure10 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output drops to a quarter then rises to a final value of half the initial level.

Figure 10: **Compressor release envelope for −12dB input step.**



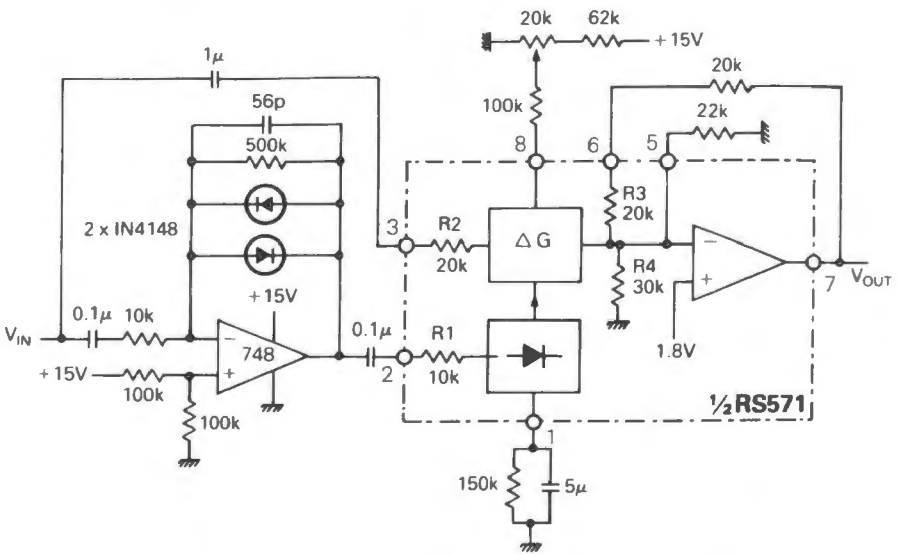
There is, of course, a trade-off between fast response and low distortion. If a small C_{RECT} is used to get very fast attack and decay, some ripple will appear on the gain control line and produce distortion. As a rule of thumb, a C_{RECT} of 1µF will produce 0.2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. It is interesting to note that the low-frequency distortion generated by a compressor would be cancelled by an expander, provided they had the same value of C_{RECT}.

Circuits

Noise gate

Figure 11 illustrates the use of the RS571 as a noise gate which will mute the output when the input signal drops below −60dBm. Such a circuit would be useful at the output of a tape recorder where the output noise would be eliminated in the absence of an output signal. The rectifier input is taken from the op amp, the output of which will be a 1.2V peak-to-peak square wave for signals larger than −4dBm. The overall gain will stay constant until the input drops below this level. At lower input levels the op amp output will start dropping and the circuit will start a 2:1 expansion.

Figure 11: **Noise gate, low-level expander**

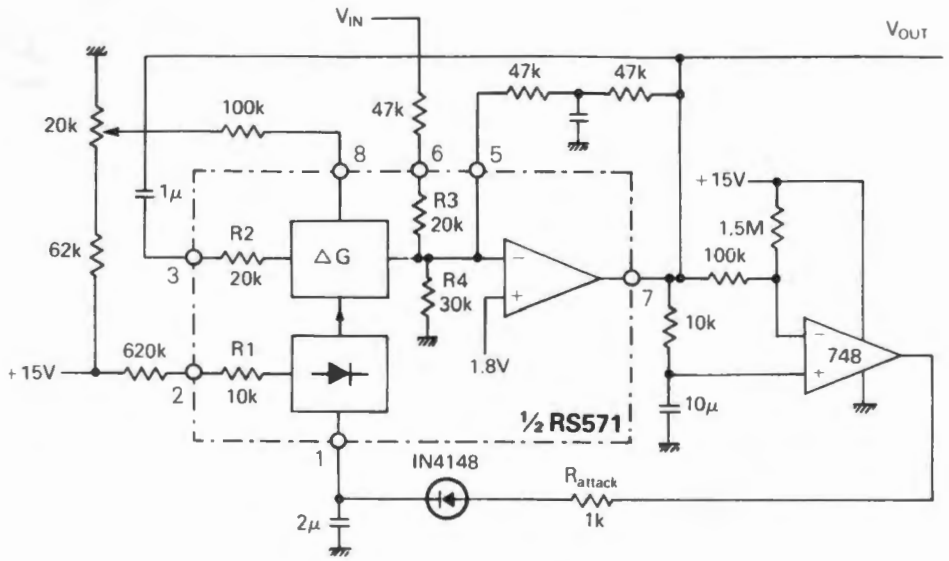


As the input approaches −60dBm the presence of the 150kΩ resistor across C_{RECT} will cause the expansion ratio to increase, until the gain drops to zero at −60dBm (see Figure 6). The external amplifier has its bandwidth limited to 200 to 6000Hz so that the gain will be controlled only by the important audio information. The external 20kΩ resistor around the op amp of the RS571 adjusts it to unity gain for large signals, and the 22kΩ resistor from the summing node to earth biases the output to 7.5V. A trimming network is included for low-distortion operation.

Limiter

Figure 12 illustrates the use of the RS571 as a fast-attack limiter.

Figure 12: **Fast-attack limiter**



For small signals, the 748 (or comparator) output is low and C_{RECT} is charged only by the current from the external 620kΩ resistor tied to V_{CC}. The gain is thus constant, and is set to unity by the 47kΩ resistor in series with R_3. When an input signal exceeds 0dBm, a −1V peak will cause the 748 output to go high and C_{RECT} will be rapidly charged. This will increase the gain of the ΔG cell, producing more feedback current around the op amp so that the circuit gain will drop. The output is thus limited to 0dBm no matter how high the input. Practically though, the circuit will limit input signals up to about +20dBm. This limit is due to the rectifier, which is biased ON with 20μA and has a maximum input of 200μA. There is a factor of 10 or 20dB of gain reduction available.

RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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R.F. Amplifier i.c. RS560C

RS data

Stock number 303- 214

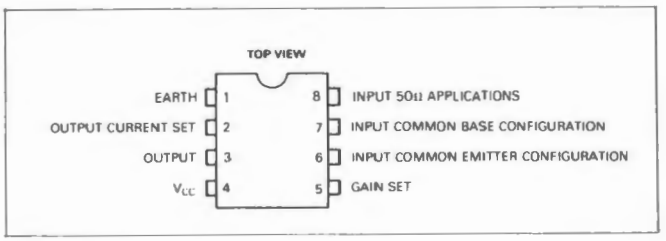
A high performance low noise R.F. amplifier I.C. in an 8 pin D.I.L. package. The large number of circuit nodes accessible from the outside of the package affords great flexibility, enabling the operating currents and circuit configuration to be optimised for many applications. A particular feature is the option of connecting the input transistor in either common emitter or common base.

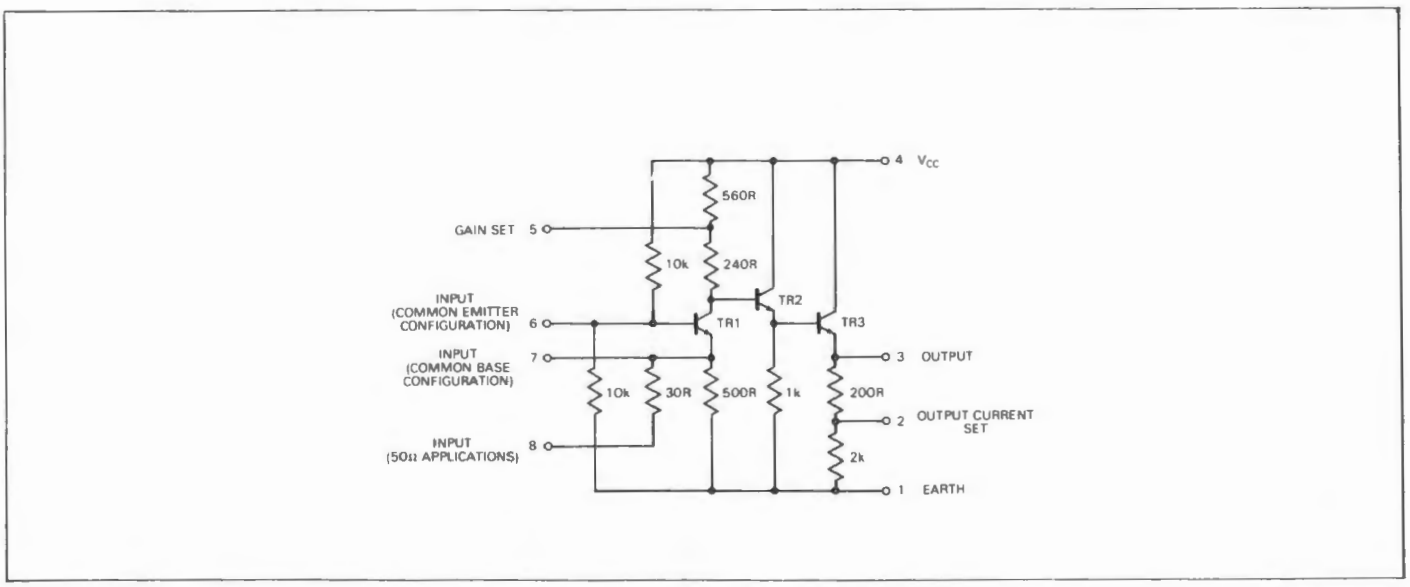
Features

- Gain up to 40dB.
- Noise figure less than 2dB (R_S 200 ohm)
- Bandwidth 300 MHz
- Supply voltage 2-15V (depending on configuration)
- Low power consumption

Absolute Maximum Ratings

Supply voltage V_{cc} ——— +15 V
Storage Temperature ——— −55 °C to +125 °C
Junction Temperature ——— +125 °C
Operating Temperature Range@ 100mW —— −5 °C to +100 °C





Electrical Characteristics V_{CC} = 6V, T_A = 25°C, f = 30 MHz, R_S = R_L = 50Ω, Test Circuit Figure 11.

Parameter	Conditions	Min.	Typ.	Max.	Units
Small signal voltage gain Gain flatness	 10 MHz - 220 MHz	11	14 ±1.5	17	dB dB
Upper cut-off frequency			250		MHz
Output swing	V_{cc} = 6V V_{cc} = 9V	+5	+7 +11		dBm dBm
Noise figure (common emitter)	R_s = 200Ω		1.8		dB
	R_s = 50Ω		3.5		dB
Supply current			20	30	mA

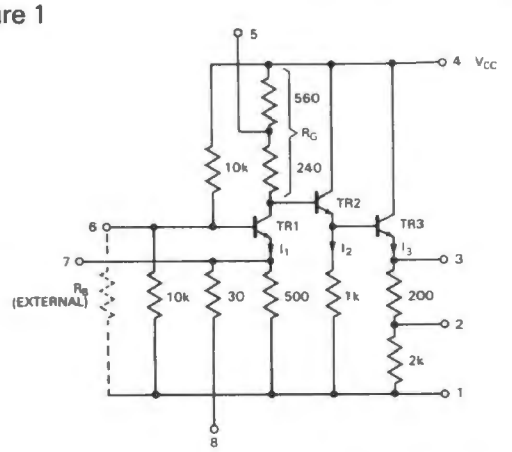
Design Information

Input and Gain Considerations

The input stage can be operated in a common base or common emitter configuration. Common emitter gives a high input impedance, the lowest posible noise figure and the highest gain. Common base gives a low input impedance which can be made equal to 50 ohms.

Two gain ranges are available in each configuration and these can be selected by shorting pin 5 to pin 4 or by leaving it open circuit. With pin 5 open circuit R_G equals 800 ohms (see Figure 1) and the highest gain is obtained. When pin 5 is connected to pin 4 R_G is reduced to 240 ohms and the gain is reduced by 10dB.

Figure 1



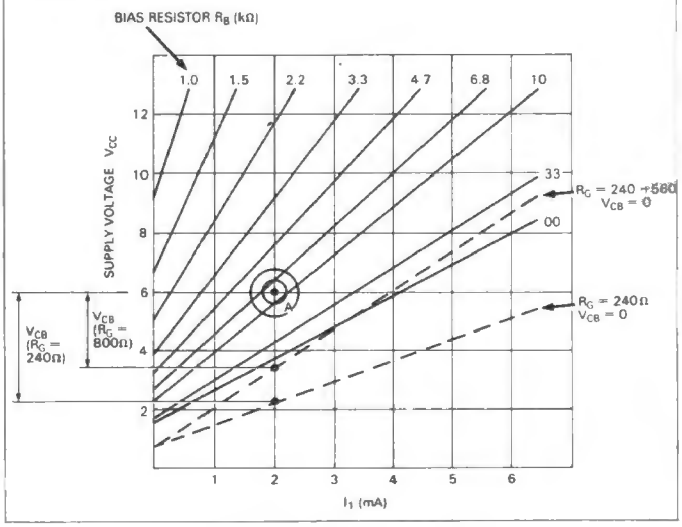
Biasing

The internal biasing components are designed for operation with low supply voltages and low currents. Without using any external resistors the first stage current will be approximately 4mA at 6V, 2.3mA at 4V and 0.5mA at 2V.

Operation at supply voltages greater than 6V requires the addition of an external resistor (R_B) from pin 6 to ground, to set I_1 to the desired value. Figure 2 can be used to find an appropriate value for R_B.

As example assume a value for I_1 of 2mA is required at a supply voltage of 6V.

Figure 2

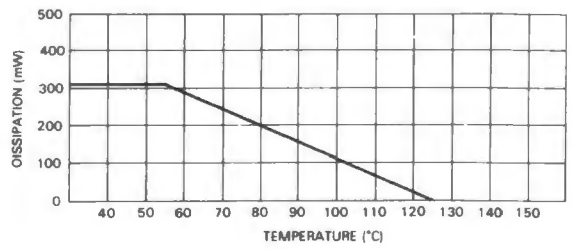


The point 2mA is found on the graph (point A, Figure 2) and since this point is closest to the line corresponding to a bias resistor value of 6.8k then this value should be used.

It is important when setting the bias to ensure that TR1 does not saturate. The collector-base voltage of TR1 can also be found from Figure 2. The two dotted lines labelled $V_{CB} = 0$ are used to find this voltage The vertical distance from the bias point to the appropriate $V_{CB} = 0$ line gives the operating collector-base voltage, which should always be greater than the required peak output voltage. In the example under consideration the collector-base voltage if $R_G = 800$ ohms is 2.5V and if $R_G = 240$ ohms it is 3.8V.

Once the first stage current has been set the currents in the second and third stages I_2 and I_3 (see Figure 1) can be calculated. The voltage on TR1 emitter will be approximately 0.75V less than its base. Hence the current is determined by this voltage divided by the value of the emitter resistor (1k ohms). Similarly the voltage on the emitter of TR3 will be $V_{CC} - I_1 R_G - (2 \times 0.75)$ and the current I_3 can be obtained in the same way.

Figure 3. **Max. power dissipation at various ambient operating temperatures**



Power dissipation

It is important at this stage to check the total power dissipation of the device to ensure that it is within the limits given in Figure 3. If the dissipation is too high there are several options. A heat sink could be added to the package to reduce the thermal resistance, or the supply voltage or current could be reduced. In some circumstances an external resistor can be used to remove some power dissipation from the package. (see later).

Output power

The output power of the RS560C can be controlled at three main points in the i.c. The first is the output emitter follower stage.

The maximum voltage that this can deliver into a load resistance of R_L is $2I_3R_L$ volts peak-to-peak. To increase I_3 (within the power dissipation limits), an external resistor can be used from pin 3 to ground.

The second point which can limit the output swing is saturation at the collector of the first stage. Correct biasing and the use of a high supply voltage should eliminate this difficulty.

The third and most fundamental limit concerns the distortion at the input base emitter junction. Unless an emitter resistor is used, the maximum input signal which can be handled with reasonable linearity is about 20mV peak-to-peak. Adding an emitter resistance increases this $2I_1R_e$ volts peak-to-peak. The internal 30 ohm resistor can be used to increase the input signal handling, and is brought into operation by decoupling pin 8 instead of pin 7.

Voltage gain

The voltage gain as a function of I_1 is shown in **Figure 4.**

This is the gain in common emitter without any emitter resistance. If the 30 ohm resistor is used to improve the input signal handling then the gain will be reduced. The theoretical expression is:

$$\text{Gain (dB)} = 20 \log_{10} \frac{R_G}{R_E + 25/I_1}$$

Where R_E and R_G are in ohms. I_1 mA.

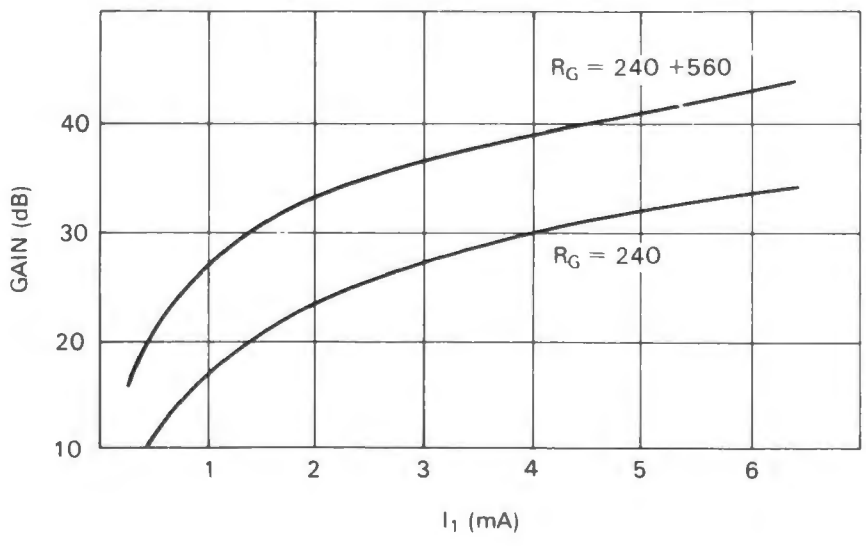
The above expression is a close approximation to the gain achieved in practice. Losses in the emitter follower stages account for 1 or 2dB, hence with R_E = 30 ohms, I_1 = 1mA and R_G = 240 ohms the theoretical gain is approximately 13dB, in practice the gain is 11dB.

Input and output impedance

The input impedance of the RS560C in the common emitter configuration (pins 7 or 8 decoupled) is much greater than 50 ohms. Its value depends on the exact circuit but it will normally be greater than 500 ohms. The input capacitance is 15pf when pin 7 is decoupled and is reduced by adding emitter resistance (decoupling pin 8).

In the common base connection (pin 6 decoupled) the input impedance is given by $25/I_1$ ohms where I_1 is the first stage current in milliamps. An input impedance of 5 ohms or less can be obtained.

Figure 4. **Design graph**



A 50 ohm input impedance can be obtained in two ways. The internal 30 ohm resistor can be used in series with the input and the first stage operated in common base. The other way is to operate the first stage in common emitter and add a 50 ohm resistor across the input.

The RS560C has a low impedance voltage output. At low frequencies the output impedance is $25/I_3$ ohms where I_3 is in milliamps. At high frequencies series inductance becomes increasingly significant, This output inductance (25nH) can give resonance problems when driving capacitive loads at frequencies over 200MHz. It is advisable in this case to isolate the RS560C from the load with a series 30 ohm resistor.

Low noise operation
The RS560C can be treated as a conventional transistor amplifier in evaluating its noise performance. For calculating noise figures the typical hfe and base resistance of the input transistor TR1 are 80 and 17 ohms respectively.

The optimum noise figure is achieved when the first stage current conforms to the equation.

$$I_1 = \frac{225}{R_S}$$

Where I_1 = first stage current in mA.
R_S = source resistance seen by input of RS560C in ohms.

The section on biasing details the procedure for obtaining this optimum current.

Design examples

A selection of design examples follows illustrating the design techniques discussed in the previous sections.

High power 50 ohm amplifier with a 9V supply rail

Step 1. Set bias
As high output power is required the first stage current I_1 is set at 5mA and the internal 30 ohm resistor R_E employed to linearise the input. Referring to Figure 1 operation at 5mA and 9V requires a bias resistor of R_B of approximately 22k ohms.

Step 2 - Check V_{CB}.
From Figure 2, the operating point (9V, 5mA) is 1.7V above the $V_{CB} = 0$ line for $R_G = 240 + 560$. This is too low for a high powered amp so employ $R_G = 240$ ohms. In this case $V_{CB} = 4.5V$.

Step 3 - Calculate Gain
From the full expression for gain

$$\text{Gain} = 20 \log_{10} \frac{240}{30+25/5} = 16.7 \text{ db}$$

This will be reduced by the emitter followers but a gain of about 15dB can be expected.

Step 4 - Set output stage current
Since the output is a 50 ohm load the high output stage current is obtained by shortening pin 2 to ground.

Step 5 - Check dissipation
The current and voltage in the circuit calculated using preceeding section will be as shown in Figure 5. Thus the power dissipation in each stage will be:

1st stage:	5mA at 9V =	45mW
2nd stage:	7mA at 9V =	63mW
3rd stage:	32mA at 9V =	288mW
		396mW

This exceeds the rating of the RS560C.

The dissipation can be reduced by using an external resistor to set the output instead of the on chip 200 ohm. If 300 ohms external is used the power dissipation becomes

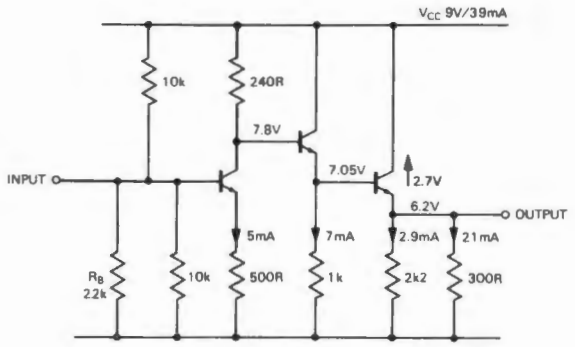
1st stage:	5mA at 9V =	45mW
2nd stage:	7mA at 9V =	63mW
3rd stage:	24mA at 2.7V =	65mW
	2.9mA at 6.3V =	18mW
		191mW

This lower dissipation allows the RS560C to be used to +82°C

An example of a 50 ohm low power amplifier, where the 50 ohm output impedance is obtained by connecting pin 2 to ground, is shown later.

Step 6 - Calculate output voltage swing
The output stage current has been set to 24mA so the maximum output voltage into a 50 ohm load will be 2 x 50 x 0.024 = 2.4 volts peak-to-peak. Since we have arranged the V_{CB} of the first stage to be 4.5V there will be no problem with saturation of TR1. The maximum input signal will be 2 x 0.005 x 30 = 300mV peak-to-peak, since the gain gives 1.7V peak-to-peak output.

Figure 5. **Bias circuit diagram for high power 50 ohm amplifier**



Hence the maximum output voltage will be 1.7V peak-to-peak, limited to this value by the value of emitter resistance used with TR1.

The final circuit diagram is shown in Figure 6. The frequency response of the circuit is shown in Figure 7. The circuit takes a supply current of 39mA and delivers the design output swing of 1.7V peak-to-peak up to 100MHz. At 150MHz the output swing reduces to 1.5V peak-to-peak.

Figure 6. **Practical circuit for 50 ohm amplifier**

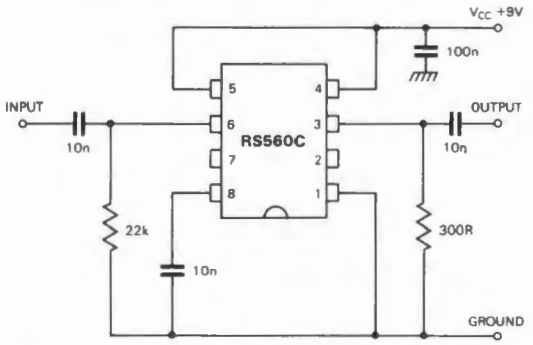
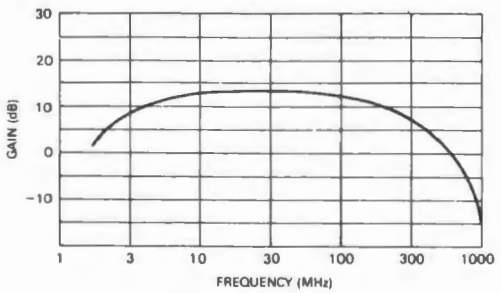


Figure 7. **Frequency response of high powered amplifier**



Low noise amplifier for 50 ohm source system

Step 1 - Set bias

The prime design consideration in this example is low noise figure, consequently the first stage current I_1 is calculated for optimum noise.

$$I_1 = \frac{225}{R_s} \text{ for optimum noise}$$

$$= \frac{225}{50} = 4.5\text{mA}$$

Using a 9V supply and 4.5mA first stage current reference to Figure 2 gives the necessary bias resistor R_B of 10k ohms.

Step 2 - Check V_{CB}

Figure 2 gives a V_{CB} of 2.5V if the high gain option is used. ($R_G = 800\Omega$)

Step 3 - Calculate gain

Figure 2 also gives the gain approximately 40dB. No emitter resistor will be used since minimum noise is required.

Step 4 - Set output stage current

There is no requirement for output swing in this case so the low output stage current can be used. Pin 2 is thus left open-circuit.

Step 5 - Check dissipation

The currents and voltages in the circuit so far are shown in Figure 8. The power dissipation is therefore well within the device specifications.

The final circuit diagram is shown in Figure 9.

The measured frequency response is shown in Figure 10. The measured noise figure with a 50 ohm source impedance is 3.4dB.

Figure 8. **Bias circuit for low noise amplifier**

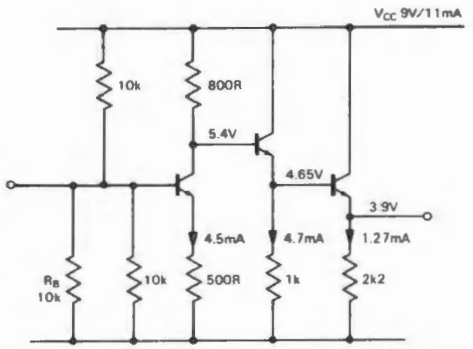


Figure 9. **Practical circuit for low noise amplifier**

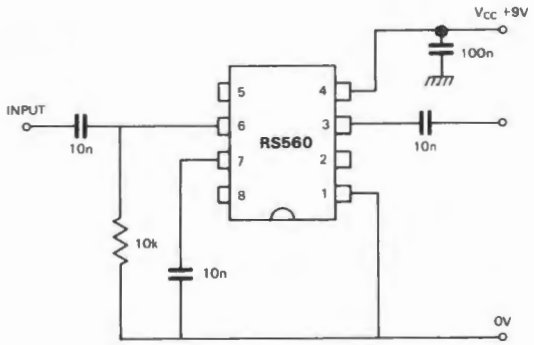
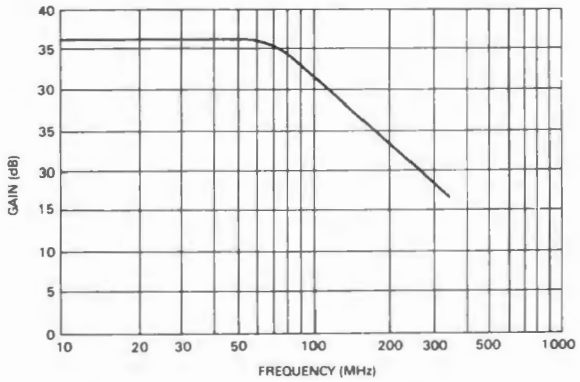


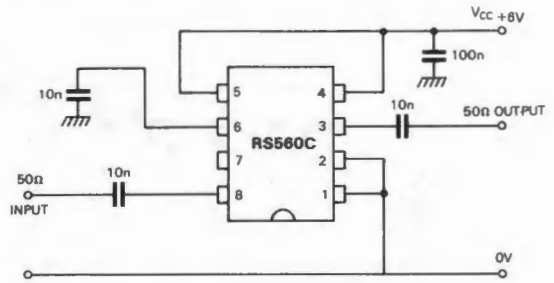
Figure 10. **Frequency response of low noise amplifier**



Circuit applications

The following circuit diagrams and associated response curves illustrate the versatility of this amplifier.

Figure 11. **50Ω line driver. The response of this configuration is shown in Figure 13**



Gain 14dB
Bandwidth 220 MHz (P_{out} = 1mW, 50Ω)
200 MHz (P_{out} = 5mW, 50Ω)
Input SWR 1.5:1

Figure 12. **Input standing wave ratio plot of circuit shown in Figure 11.**

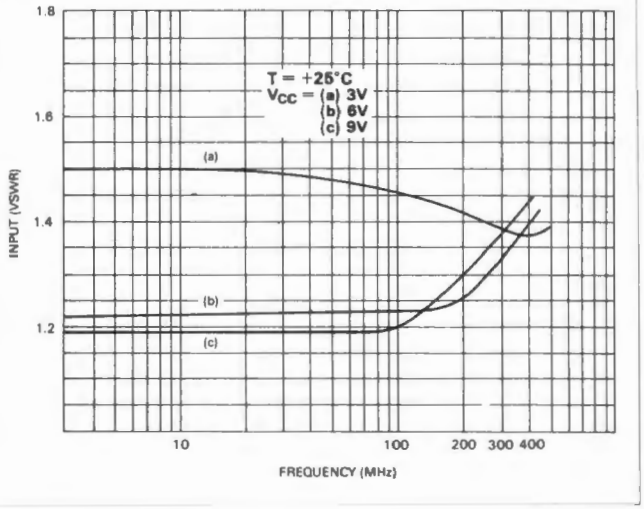


Figure 13. **Frequency response, small signal gain**

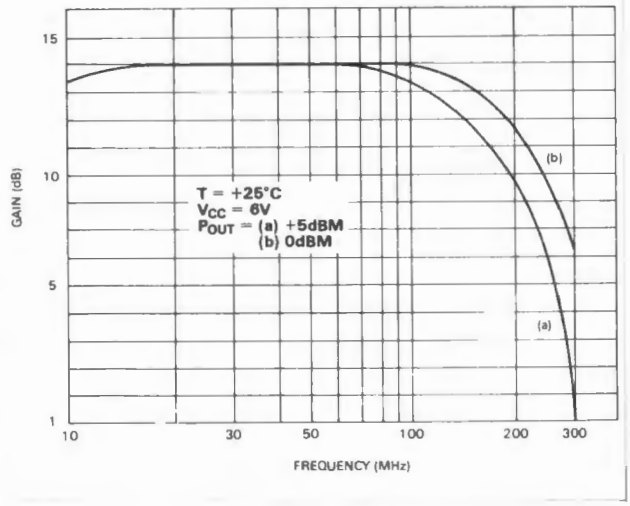
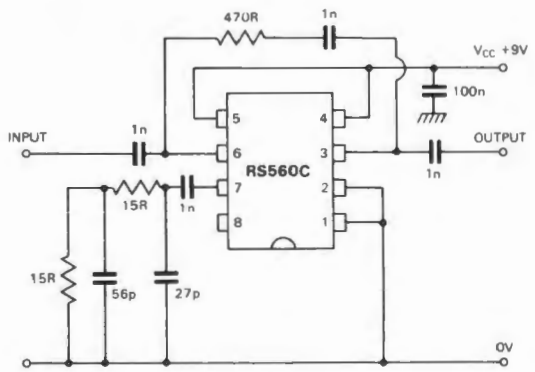


figure 14. **Wide bandwidth amplifier**



Gain 13dB at V = 9V
– 1dB at 6 MHz and 300 MHz

Figure 15. **Frequency response of circuit shown in 14**

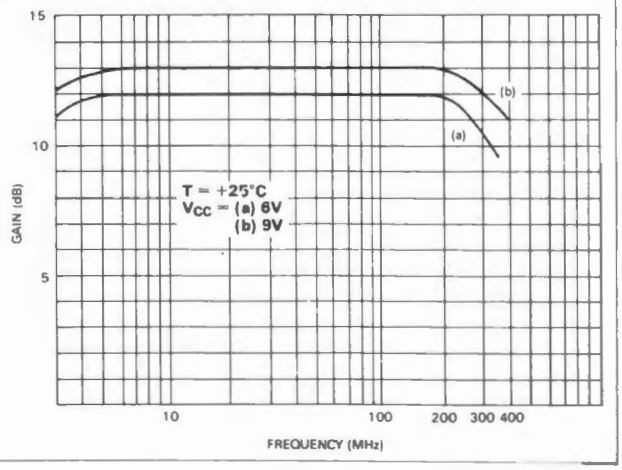


Figure 16. **Three stage directly-coupled high gain low noise amplifier**

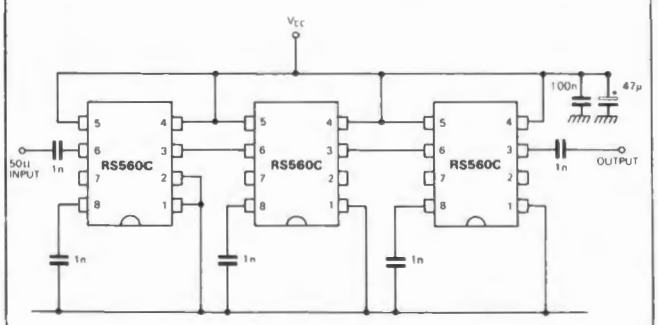


Figure 17. **Frequency response of circuit shown in 16**

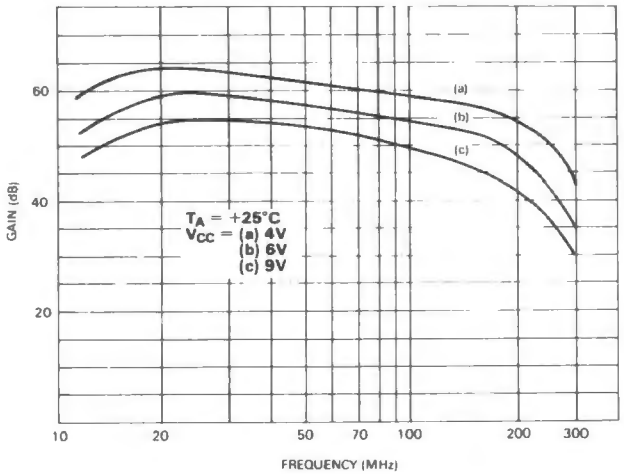
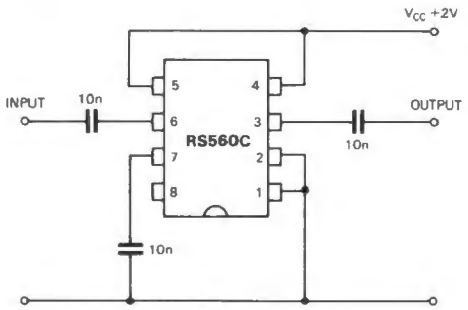


Figure 18. **Low power consumption amplifier**



Gain 13dB
Power supply current 3mA
Bandwidth 125 MHz
Noise figure 2.5dB (R_S = 200Ω)

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RS data

Phase control i.c. RS2085A

Stock number 303-220

The RS2085A is a bipolar i.c. designed for use in closed or open loop a.c. phase control circuits with resistive or inductive loads. Closed loop systems can employ either voltage or tachogenerator frequency feedback for maximum versatility. Ideal for motor speed control in power drills, machines etc.

Absolute maximum ratings

Triac gate voltage pin 2	4V
Repetitive peak input current pin 4	80mA
Non repetitive peak input current pin 4 (tp<250μs)	200mA
Peak input current pin 5 positive half cycle	2mA
Repetitive peak input current pin 5 negative half cycle	80mA
Non repetitive peak input current pin 5 negative half cycle (tp<250μs)	200mA
Peak input current (1_{SYNC}) pin 6	±3mA
Peak input current (V_{SYNC}) pin 7	±3mA
Inhibit input voltage pin 8	V_{reg} V
−5V regulator current pin 11	10mA
Control amp input voltage pin 13	V_{reg} V
Tacho input current pin 15	±10mA
Operating ambient temperature	0 to +85°C
Storage temperature	−55 to +125°C

Features

- Powered direct from AC mains or DC line.
- 5V supply available for ancillary circuitry.
- Low supply current consumption.
- Average or peak load current limiting.
- Ramp generator to provide controlled acceleration.
- Negative Triac firing pulse.
- Warning LED drive circuit.
- Actual speed derived from tachogenerator frequency or analogue feedback.
- Well defined control voltage/phase angle.
- Inhibit input for use with Thermistor Temperature Sensors.

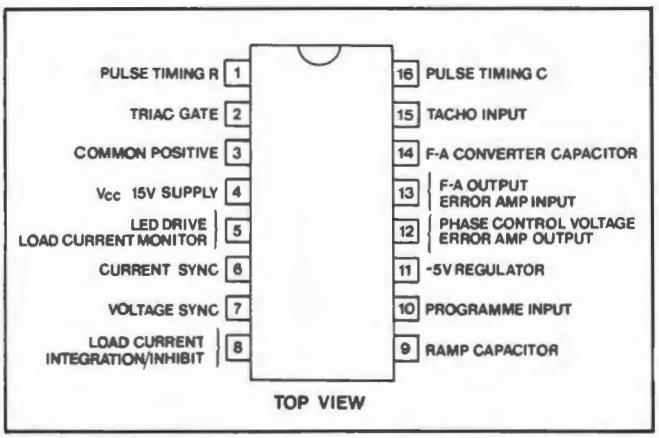
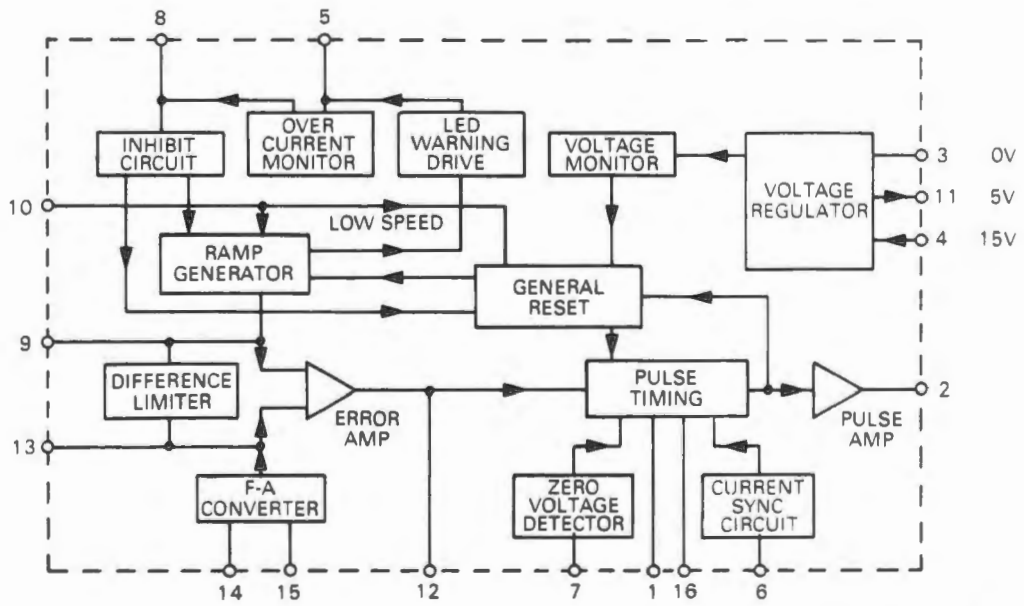


Figure 1 **Block diagram**



Electrical characteristics measured with respect to pin 3. T_a = 25°C

Parameter	Pin No.	Notes	Min.	Typ.	Max.	Units
Operating current	4	1		2.8	3.8	mA
Shunt voltage regulator						
Regulating voltage	4	2	−15	−14	−13	V
Voltage monitor enable level			−11		−9	V
Series regulator						
Regulating voltage (V_{reg})	11	3	−5.35	−5V	−4.65	V
Temperature coefficient					±1	mV/°C
External load					10	mA
Regulation		4	−75		+75	mV
Ramp generator						
Capacitor charging current	9		25	30	35	μA
Capacitor discharge current		5		25		μA
Capacitor discharge current		6		10		mA
Capacitor to actual speed voltage clamp			−0.8		+0.8	V
Speed programme circuit						
Input voltage range	10		V_{reg} −0.5		0	V
Input bias current					1	μA
Zero power demand voltage			−100	−75	−50	mV
Frequency to analogue converter						
Tacho input voltage	15	7	350			mV
Hysteresis	15		125	175	225	mV
Bias current	15				10	μA
Conversion factor	15 to 14	8		0.5		mV/rpm
Conversion gain	15 to 14			1		
Error amplifier						
Input voltage range	9 and 13		V_{reg}		0	V
Input bias current	9 and 13				0.5	μA
Input offset voltage	9, 13 and 12	9			±10	mV
Trans conductance	9, 13 and 12		80	100	120	μA/V
Output current drive	12		±20	±25	±30	μA
Firing pulse timing						
Voltage SYNC trip level	7		±35	±50	±65	μA
Current SYNC trip level	6		±35	±50	±65	μA
Phase control voltage swing	12		V_{reg}		0	V
Firing pulse width	13	10		50		μs
Pulse repetition time	13	11		100		μs
Firing pulse output						
Drive current	2	12	50	75	100	mA
Leakage current	2	13			10	μA
Load current limiting						
Offset voltage	5				±20	mV
Current gain	5 and 8	14	0.475	0.5	0.525	
Voltage for load current limit	8	15		−1		V
Voltage for load current inhibit	8	16		−1.5		V

Notes:

1. Pin 4 voltage = 13.0V including triac gate drive traffic.
2. 0 to +85°C.
3. 1mA external load.
4. For 0-5mA external load change.
5. Load current limit in operation.
6. Load current inhibit in operation: 5V on ramp capacitor.
7. Peak value.
8. Typical application : C pin 14 = 10nF, R pin 13 = 150kΩ, 8 pole tacho 10,000rpm max.
9. V9-V13 to give I_{12} = 0
10. C pin 16 = 47nF
11. C pin 16 = 47nF, R pin 1 = 200kΩ
12. Pin 2 = −3V
13. Pin 2 = 0V
14. Pin 5 = 100μA
15. 0.2V reg
16. 0.3V reg

Circuit description

The RS2085A incorporates a shunt stabilizer which enables it to be powered from the mains, via current limiting components, or from a DC supply. In addition, an on-chip series regulator provides a −5V supply which powers various internal circuits, the speed programming potentiometer and other ancillary components. Up to 5mA is available from this supply for powering additional external circuitry. A supply voltage monitor circuit prevents triac firing pulses from being generated until an adequate supply voltage is established and by discharging the ramp capacitor, ensures a soft start when the supply returns to normal after a short interruption. Motor acceleration is controlled by a ramp generator to a maximum determined by the speed program input. Grounding the speed program input will cause a general reset and inhibit the triac pulses. The ramp generator rise time and therefore the motor acceleration is determined by a fixed

internal changing current and an external capacitor. For use in closed loop systems a frequency to analogue (F-A) converter provides a DC voltage proportional to motor speed, sensed at the tacho input. The conversion is made by transferring a pulse of charge from the F-A converter capacitor to an RC filter on the F-A output pin. Hysteresis on the tacho input prevents noise from giving a false indication of motor speed.

The error amplifier has differential inputs that compare the ramp generator voltage with the actual speed voltage from the F-A converter. A clamp circuit across the amplifier inputs prevents the differential input voltages exceeding about ±0.5V. The output from this amplifier is a bidirectional current of limited amplitude which is integrated to limit the maximum rate of charge of triac firing pulse angle. For use in open loop systems the amplifier is connected as a voltage follower and acts as a buffer between the ramp generator and pulse timing circuit. Triac firing pulse synchronisation is achieved by delaying the pulse with reference to the zero crossing voltage points of the mains cycle as determined by the zero voltage detection circuit. With inductive loads, the load current will phase lag the mains voltage, and under these conditions the triac firing pulse must be delayed until the load current from the previous half cycle has ceased. The current synchronisation circuit satisfies this requirement by preventing firing pulses until a voltage drop appears across the triac. If the triac fails to latch, repeated firing pulses will be supplied. The firing pulse width and the spacing of repeated pulses are controlled by a single capacitor.

An average load current limit circuit which works on positive mains halfcycles only is used to protect the triac and motor under stall conditions. External resistors determine the trip point which operates at two levels: the first under moderate overload conditions, discharges the soft start capacitor with a constant current until a safe load current is reached whilst the second initiates a general reset and rapid discharge of the soft start capacitor.

A warning LED may be connected in series with the −15V supply to give an indication of an overload condition or the programming of zero speed/power. The diode is extinguished by shunting the supply current to −15V during −ve mains half cycles by internal circuitry on the load current monitor pin.

Features description

Low supply current consumption

Due to the low current consumption of the device the power dissipation in the mains dropper resistor may be as low as one watt on a 220V AC supply (0.5W on 100V).

By incorporating both a shunt and a series voltage regulator in the IC design, a high ripple voltage can be accommodated on the supply smoothing capacitor. The combination of the above two features results in reduced size and a minimum count of components used in the power supply circuitry.

Powered direct from AC mains or DC line

This device incorporates a shunt regulator (−15V) such that it may be powered from an AC or DC supply via current limiting components or the device may be powered direct from a −12V DC supply.

−5V supply available for ancillary circuitry

A −5V series regulator is incorporated to provide a smooth supply for the internal analogue control functions. This supply may be used externally to power ancillary circuitry such as timing circuits and other logic control circuits etc, as well as driving potentiometers for the analogue control inputs. Due to this supply technique, greater symmetry between positive and negative half cycle firing phase angle will result.

Low supply inhibit circuit

Timing functions and triac gate drive pulses are inhibited until there is sufficient supply voltage across the device to guarantee complete gate drive pulses.

This ensures that bulk conduction is established in the triac and correct linear operation of the control system is maintained.

Negative triac gate firing pulses

Since the device works with the positive supply as common, the triac gate pulses are negative going. This is an advantage when selecting a suitable triac since most triac manufacturers prefer this drive polarity.

The device is designed to give a triac pulse that is greater than 50mA for a period fo 50 microseconds with standard pulse timing components (47nF, pin 16). Repeated triac gate pulses are given if the triac fails to latch or becomes unlatched due to motor brush bounce.

Well-defined control voltage/phase angle (open loop)

An internal 5V stabilizer circuit is used as the charging voltage for the pulse timing ramp capacitor and as the reference voltage for the speed input potentiometer. This ensures that maximum phase angle can be obtained by adjusting the resistor or capacitor on the pulse timing circuit, without affecting the maximum setting.

Average or peak load current limiting

The load current is normally sensed in the positive mains cycle by means of a low impedance resistor in series with the triac and the load. The voltage drop across this resistor is converted back into a low current source by a second resistor and fed into the load current sensing input (pin 5) of the IC. In high load current applications where the power dissipated in a series sensing resistor would be unacceptable, a current transformer may be utilised.

The current fed into the sensing input (pin 5) is mirrored by the IC and fed to the inhibit input (pin 8). Peak current limiting can be provided at this point by inserting a resistor between pin 8 and common (pin 3), whereas average current limiting requires the addition of an integrating capacitor.

When average current limiting is used the double action of the inhibit circuit is utilised. This has two trip points such that when the first trip point (−1V) is reached the power to the load will be gradually reduced by decreasing the voltage on the ramp capacitor, (the discharge rate being equal but opposite to the soft start), hence reducing the power and providing a constant current drive (producing constant torque) to the motor. When the second trip point (−1.5V) is reached a general reset of all timing functions occurs at a fast rate, hence if a gross overload was suddenly applied to the

motor, a rapid reduction in power supplied would result. Since it is not possible to turn the triac off during a cycle, the triac and motor should be chosen to be capable of withstanding one complete mains cycle under the worst overload condition.

Peak load current limiting tends to produce a fold back action (of motor speed and torque) at large conduction phase angle. This is due to the peak current initially increasing when the phase conduction angle is reduced at constant load torque.

Ramp generator to provide controlled acceleration
The ramp generator is a follower integrator design which can be used to control the acceleration rate up to the programmed speed. This can also be used to control the rate of phase angle increase in open loop control systems.

The ramp is defined by an internal current source (25 microamps) and the capacitor connected to pin 9.

Warning LED drive circuit
The LED drive circuit is designed to drive an LED in series with the device such that the overall consumption is minimised by utilising the IC drive current to power the LED. Due to the multiplexing technique on pin 5, some additional current will be required when the circuit is used to provide both load current limit and LED drive (this will normally be about 0.5 microamps).

The LED will illuminate under one of the following two conditions:

1. The program speed (or phase in open loop systems) is set for zero.
2. The running speed is less than that programmed. Hence, indication will be given when the system is powered up but zero power determined, or when the machine cannot maintain the set operating speed due to the load current circuit operating. The LED will also be illuminated while the soft start function is in operation ie., the LED will turn off only when the set speed has been reached.

Actual speed derived from tacho generator frequency or analogue feedback
Tacho frequency or analogue feedback may be used with this device. When frequency feedback is used, the frequency to analogue (F-A) conversion circuit is used. This circuit is extremely linear and tracks the regulated (−5V) supply.

Frequency feedback has the advantage of not being dependent on mechanical clearance, magnetic strength, etc, and since conversion rate is defined by two external components, accurate speed programming can be obtained without the need for calibration.

Tacho input drive
The RS2085A requires less than 10μA (pk) to drive the tacho input (pin 15) and has bidirectional clamping. This makes it possible to connect a tacho pick up coil directly to the device hence minimising component count.

A motor may fail to start up if a signal is picked up by a sensitive tacho due to vibration in the rotor caused by 'elastic sticktion' when power is initially applied. This can be easily overcome by incorporating a filtering capacitor across the tacho input.

Tacho fail safe operation
The RS2085A will command maximum power when an open circuit tacho is detected. This may be a safer situation in the case of hand operated tools.

Inhibit input for use with thermistor temperature sensors
A thermistor may be connected to pin 8, the load current integration pin. This is to ensure that the circuit shuts down if the maximum load temperature is exceeded. The input may also be used as an interface 5V control logic.

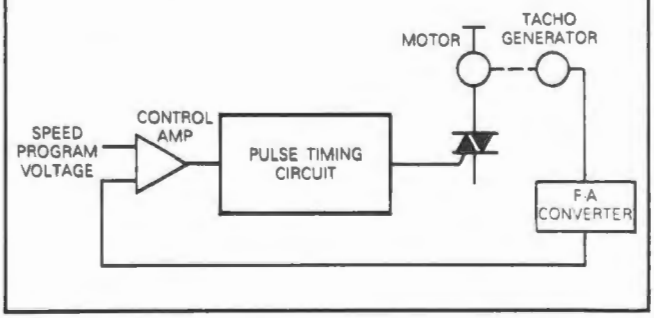
System design
Throughout this section, component references are those shown on the Reference System Circuit Diagram, Figure 3.

Open loop operation
The simplest method of motor speed control using electronics is an open loop system. In an open loop system, the phase angle of the triac firing pulse is determined by the program input voltage on pin 10. The RS2085 is particularly useful in open loop applications due to the well-defined control voltage/phase angle relationship. In this mode, changes in motor loading will cause corresponding variations in motor speed but regulation will be a considerable improvement over that achieved when motor speed regulation is obtained by a conventional series dropper resistor.

Closed loop control
A block diagram of a basic closed loop speed control system is shown in Figure 2. In this case, a voltage proportional to motor speed is compared by the amplifier with the speed program voltage and any difference will cause an appropriate change in firing pulse angle and hence motor speed. In this way automatic compensation for changing motor loads can be made.

In addition to the basic speed control functions mentioned above, additional circuitry is provided to allow control of motor acceleration and reduction of firing pulse phase angle in case of motor overload.

Figure 2 **Basic closed loop control system**



Feedback voltage
An analogue feedback voltage of 0V to −5V, obtained by rectifying and smoothing the output from a tacho generator, may be applied to pin 13. If analogue feedback is used, the frequency to analogue converter circuitry must be made inoperative by connecting pin 15 to ground and leaving pin 14 open circuit.

In most motor control applications digital feedback is recommended as this method has the advantage of inherent stability against tacho ageing and

temperature drift whilst requiring no speed calibration.

When digital feedback is used, it is possible by selecting the appropriate 'A' or 'B' circuit variant to produce a system which fails in the case of an open circuit tacho connection to either full speed ('A' variant) or zero speed ('B' variant), the 'A' variant being safer in the case of say a portable hand tool where an intermittent tacho connection could cause the machine to suddenly start up whilst being examined.

The method of tacho connection to pin 15 differs between the two circuit variants. On the 'A' variant direct connection with possibly a small capacitor to ground to reject noise is sufficent, as signal amplitude is unimportant, provided the minimum value is greater than about 350mV peak which is necessary to overcome hysteresis plus input offset voltage.

On the 'B' variant, an internally generated 25μA bias current is applied to pin 15 which is normally shunted to ground by the tacho coil.

An open circuit tacho will allow the tacho input to be pulled negative by the bias current until a general reset is initiated at a trip level of about −5.5V. In order to prevent a reset condition during normal operation it is necessary to limit the tacho signal to a value significantly less than the trip level, this being achieved by the capacitor C10 and resistor R6, which are chosen to give a substantially constant input voltage at all speeds.

Frequency to analogue converter

The frequency to analogue converter is used with digital feedback to convert the frequency of the tacho input to an analogue voltage suitable for application to the control amplifier.

During negative half cycles at the tacho input, C4 is charged by an internally generated current of nominally 100μA until −5.5V is reached, at which point the capacitor is rapidly discharged. Each time C4 is charged a pulse of current equal to and designed to track with that at pin 14 is integrated at pin 13 by C6, producing a DC voltage proportional to motor speed.

By choosing a suitable conversion factor for the frequency to analogue converter it is possible to design a system to run at any given speed within the 0V to −5V control voltage range at pin 10.

Example: A motor fitted with an 8 pole tacho is required to run at 5000rev/min with a control voltage at pin 10 of 2.5V. Calculate the values of C4 and R3 required.

Since at steady speed the control voltage at pin 10 and the F-A output voltage at pin 13 must balance, C4 and R3 must be chosen to give 2.5V at pin 13 at a motor speed of 5000rev/min.

The analogue feedback voltage (Vf) generated by the converter circuit is given by

$$Vf = Kft \times 10^{-3}\ \text{Volts} \qquad \ldots 1$$

where K is the conversion factor given by

$$K = \frac{C4 \times R3}{200}\ \text{mV/Hz} \qquad \ldots 2$$

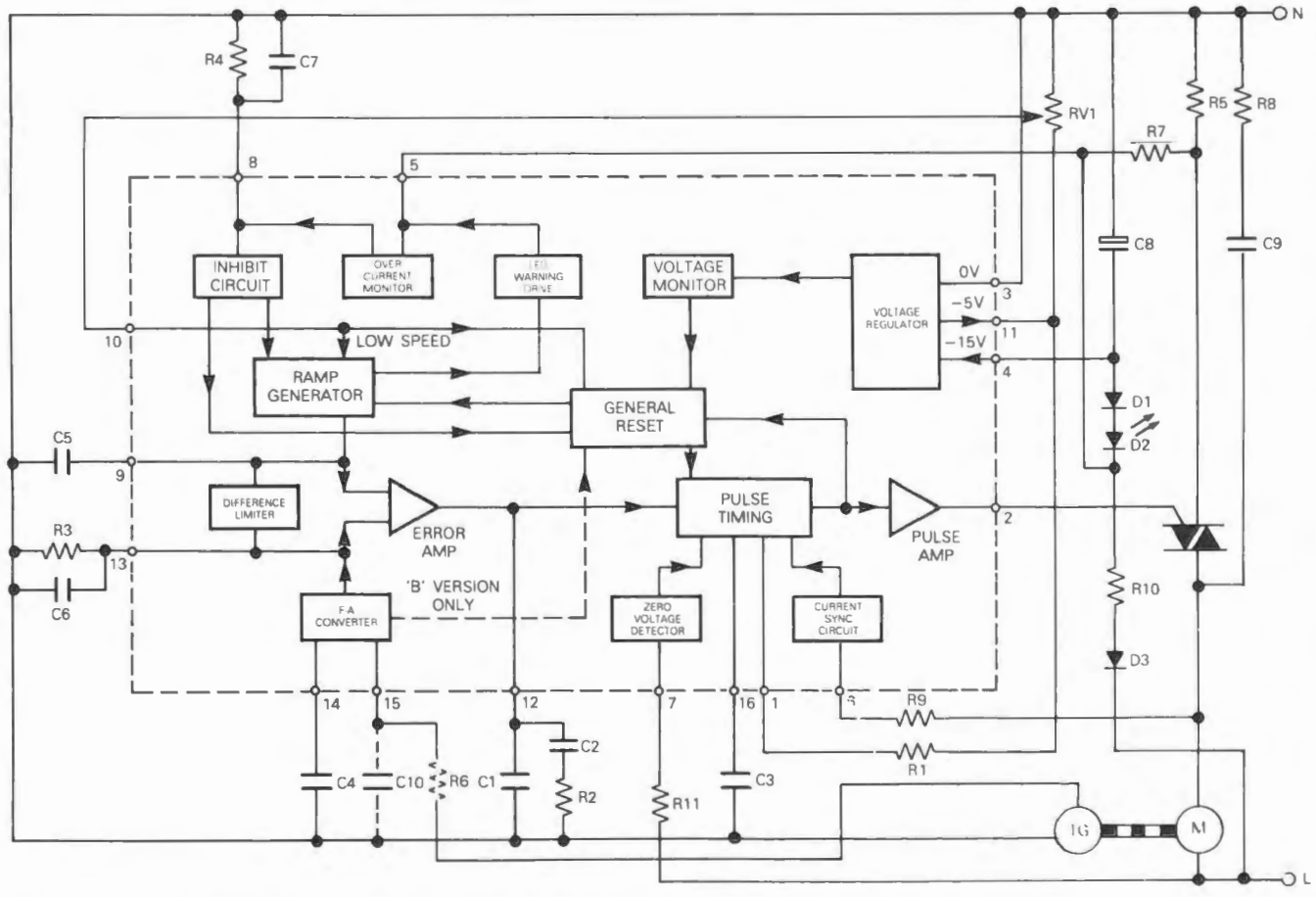
and ft is the tacho frequency given by

$$ft = \frac{SN}{120}\ \text{Hz} \qquad \ldots 3$$

using 1 and 3 above

$$K = \frac{2.5V}{0.333} = 7.5\text{mV/Hz}$$

Figure 3 **Reference system circuit diagram**



choosing R3 = 150kΩ in the range 100kΩ to 470kΩ and using above

$$C4 = \frac{7.5 \times 200}{150k} = 10nF$$

Provided close tolerance components are used for C4 and R3, most systems should not need calibration, but if required R3 can be replaced by a series resistor/potentiometer combination to give precise speed adjustment.

The value of capacitor C6 on pin 13 is a compromise between F-A converter response time and ripple voltage at the control amplifier input. In most systems a value of 1 μF will be sufficient.

Under some conditions noise introduced into the tacho coil by vibration of the stationary motor armature when power is first applied, or by electromagnetic induction can produce sufficient feedback to prevent motor start up, the phase control system using the tacho noise as evidence that the motor is running. This condition is most likely with the RS2085A where the tacho is connected directly to pin 15 without a capacitor to ground. A cure can usually be found by connecting a capacitor to ground or in difficult cases a series resistor as well.

Ramp generator

The ramp generator limits the rate of change of speed reference voltage (Vs) applied to the control amplifier and therefore controls the rate of acceleration of the motor. The ramp rate Vr is set by an internally generated 30 μA current source Ir and the capacitor C5 on pin 9, the rate being given by

$$Vr = \frac{Ir \times 10^{-6}}{C10} V/s \qquad ...4$$

Using the previous example where the control voltage is increased from zero to −2.5V and C5 = 10 μF the ramp rate (Vr) will be

$$\frac{30 \times 10^{-6}}{10 \times 10^{-6}} = 3.0V/s$$

and the acceleration time $= \frac{2.5V}{3.0V/s} = 0.83$ seconds

The final ramp voltage on pin 9 is 2Vbe below the control voltage on pin 10.

Speed program voltage

The speed program voltage (V10) on pin 10 has a working range from the zero power demand level at −75mV and Vreg. Levels above 75mV on pin 10 will cause the ramp capacitor to remain discharged and the triac drive pulse will be inhibited. The LED on pin 5 will also remain lit.

In most applications pin 10 voltage will be derived from a potentiometer connected between Vreg and ground.

The control amplifier

In closed loop applications, the control amplifier is used to compare the analogue feedback voltage (Vf) at pin 13 with the speed reference voltage on pin 10 and to produce a phase control voltage Vp on pin 12. The amplifier has a transconductance gain of 100 μA/V with a limited bidirectional ouput drive capability of ±25 μA. Proportional control therefore occurs for differential input errors between ±250mV.

The gain and phase compensation for closed loop control systems are determined by C1, C2 and R2 on pin 12. These components are best chosen empirically to achieve a compromise in terms of speed overshoot and response time in the actual system.

For open loop control, the control amplifier may be used as a buffer by connecting pin 12 to pin 13 and disabling the F-A converter by grounding pin 15. Use may still be made of the ramp generator to control the maximum rate of phase angle increase.

If required the maximum phase angle can be controlled by a clamp voltage applied to pin 12 but care must be taken to ensure a sharp turn-on knee.

Zero voltage detector

The zero voltage detector resets the pulse timing circuit ramp generator at the zero points of each mains cycle. The mains voltage is applied via a high value current limiting resistor R11 to pin 7 and a reset pulse is generated whenever the input current is between ±50 μA.

The circuit is designed to give symmetrical switching about the zero voltage points ensuring symmetrical triac firing in positive and negative mains half cycles.

The value of R11 should be chosen to limit the peak current in pin 7 to less than ±1mA.

Current sync circuit

The current sync circuit operates in conjunction with the pulse timing circuit by supplying an enable signal dependent on the conduction state of the triac. The enable signal is generated if the voltage across the triac is sufficient to produce an input current to pin 6 via R9 greater than ±50 μA.

Peak current to pin 6 should be limited to below ±1mA.

Pulse timing circuit

The function of the pulse timing circuit is to control the delay and duration of the triac firing pulse. A ramp voltage is produced on the pulse timing capacitor C3 on pin 16 which is charged by a constant current determined by R1 on pin 1. The ramp is reset by the voltage sync circuit at each mains zero crossing. A triac firing pulse is produced when the ramp voltage reaches a level determined by the control amplifier output on pin 12 unless further delayed by the current sync input pin 6.

Full power may be supplied to inductive loads since, when maximum conduction is demanded, the triac pulse is delayed until the lagging load current from the previous half cycle has reduced to zero. At this point the triac will cease to conduct and the supply voltage will appear across it, which when detected by the current sync input, initiates the next triac pulse.

At high motor speeds brush bounce may become severe, causing interruptions in motor supply current and unlatching of the triac. Under these conditions the current sync circuit will initiate a retriggering pulse to the triac.

The ramp waveform is generated by rapidly charging C3 on pin 16 to a Vbe more negative than Vreg at the mains zero voltage crossing. After the zero voltage point, C3 is discharged in a linear fashion by a current (Id) defined externally on pin 1 by R1. When the voltage on C3 reaches a value determined by the control amplifier on pin 12 a triac gate pulse is initiated. The dynamic working range of the ramp generator is approximately equal to Vreg.

The triac pulse duration is determined by recharging C3 to nominally 50mV above the original trip voltage.

If retriggering occurs the delay will be determined by the time taken for the current Id to discharge C3 back to the original trip voltage.

Triac pulse timing equations

Ramp discharge current

$$Id = \frac{(Vreg - Vbe)}{R1} \times 10^6 \mu A \quad ...5$$

Dynamic ramp voltage on pin 16

$$Vrp = \frac{Id \times 10^{-6}}{2 \times fm \times C3} \ V \quad ...6$$

For full phase control the calculated value of Vrp must be less than Vreg.

In most applications standard values can be used for C3 and R1. These are:

For 50 Hz supply

C3 = 47nf ± 10%
R1 = 200kΩ ± 5%

For 60 Hz supply

C3 = 47nF ± 10%
R1 = 160kΩ ± 5%

With the above components the triac pulse width will be approximately 70μs and the retriggering time 100μs.

Triac gate drive

The triac gate pulse is negative going, this being preferred by triac manufacturers and in most cases it will be found that the triggering current requirement is less for negative pulses. Internal current limiting is provided, the current being largely independent of the triac gate voltage although a series resistor can be used to reduce overall power consumption if required.

When a series resistor is used the approximate gate drive current may be calculated from

$$Itg = \frac{V4 - 1 - Vtg}{Rg} \times 10^3 mA \quad ...7$$

provided the series resistor is sufficient to reduce the gate current below the internally limited value.

Triac latching

As mentioned before, it is necessary to trigger the triac when conditions are right for a latching current to be established within the period of the gate pulse.

When switching on an inductive load the initial current will increase from zero at a rate dependent on the voltage across and the inductance of the load (the minimum voltage being determined by the load current detector). To help with latching, additional triac load current for a short duration can be provided if required by means of a series RC network in parallel with the triac. C9 and R8 provide this function as well as offering some protection from dv/dt triggering of the triac due to noise spikes on the mains.

Load current limiting

The purpose of motor current limitation is more to protect the triac than the motor itself. Since the stall current is generally much higher than that required for maximum working torque, a limitation can be set at a lower value thus guaranteeing safe operation of the triac under all load conditions.

The load current is normally sensed in the positive mains half cycle by means of a low value resistor R5 in series with the triac and load. This voltage drop is converted back into a low current source by R7 in series with pin 5 and is mirrored internally with a ratio of 2:1 into pin 8. Peak current limiting can be provided at this point by inserting a resistor between pin 8 and common whereas average current limiting requires the addition of an integrating capacitor.

When average current limiting is used the double action of the inhibit circuits on pin 8 is utilised. This has two trip points at −1V (load current limit) and −1.5V (load current inhibit). When the first trip point (−1V) is reached the power to the load will be gradually reduced by decreasing the voltage on the ramp capacitor, (the discharge rate being equal but opposite to the soft start), hence reducing the power and providing a constant current drive (producing constant torque) to the motor. When the second trip point (−1.5V) is reached a general reset of all timing functions occurs at a fast rate, hence if a gross overload was suddenly applied to the motor, a rapid reduction in power supplied would result. Since it is not possible to turn the triac off during a cycle, the triac and motor should be chosen to be capable of withstanding one complete mains cycle under the worst overload condition.

The value of R5 can be calculated from

For load current limit

$$\frac{\frac{1}{R4} \times R7}{\text{Average load current} \times 0.25} \quad ...8$$

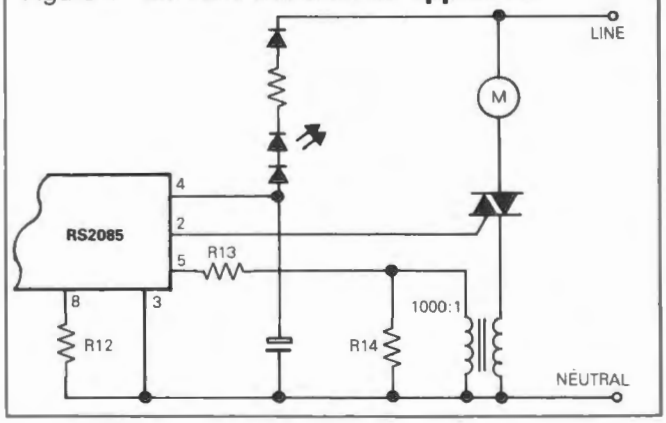
For load current inhibit

$$\frac{\frac{1.5}{R4} \times R7}{\text{Average load current} \times 0.25} \quad ...9$$

The value of R4 can vary between 100kΩ and 470kΩ, the lower value being preferred in order to reduce offset voltages produced by pin 8 bias current. When the LED drive capability of pin 5 is used the overload current level will be increased by about 20%.

In high current applications where the power dissipated in a series sensing resistor would be unacceptable, a current transformer may be used as shown in Figure 4.

Figure 4 **Current transformer application**



With a 1000:1 current transformer the average overload current can be calculated from

For load current limit

$$\frac{4 \times 1000 \times R13}{R14 \times R12} \quad ...10$$

For load current inhibit

$$\frac{4 \times 1.5 \times 1000 \times R13}{R14 \times R12} \quad ...11$$

Suitable values for R12 and R13 are 100kΩ and 5.6kΩ.

Peak load current limiting tends to produce a foldback action (of motor speed and torque) at large conduction phase angles. This is due to the peak current initially increasing when the phase conduction angle is reduced at constant load torque. If peak current limiting is adequate, capacitor C7 can be removed and the peak overload current calculated from

$$\frac{R7 \times 1.5}{R5 \times R4 \times 0.5} \quad \ldots 12$$

Inhibit circuit

As previously stated the inhibit circuit has two trip levels normally used in load current limiting but if required a general reset can be initiated by the application of a voltage between −1.5 and −Vreg to pin 8. This feature allows on/off control by external control circuitry or the fitting of a PTC thermistor to sense motor winding temperature as shown in Figure 6. At normal temperatures pin 8 is held close to the 0V rail as the thermistor resistance is low, but as the thermistor critical temperature is approached, the resistance increases rapidly until pin 8 voltage falls below −1.5V when the power to the load is removed.

LED drive circuit

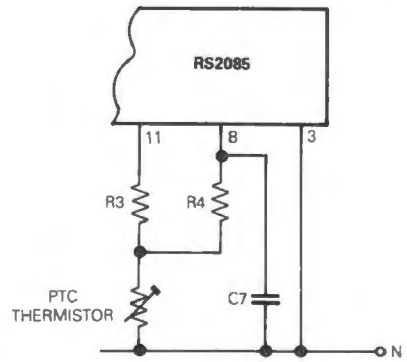
The LED drive circuit is designed to drive an LED in series with the device such that the IC supply current is used to drive the LED thereby minimising overall power consumption.

In order to turn the LED off an internal circuit with a voltage drop lower than the LED plus its associated silicon diode is used to shunt current from the LED.

Due to the multiplexing technique used on pin 5 whereby IC supply current is provided during negative half cycles and load current monitoring during positive half cycles some additional current, usually amounting to about 0.5mA will be required when the LED drive facility is used.

Due to SCR latching associated with the LED drive circuit it is not possible to use the LED feature with or without load current limiting if the circuit is powered from DC supplies.

Figure 5 **Over-temperature shut-down**



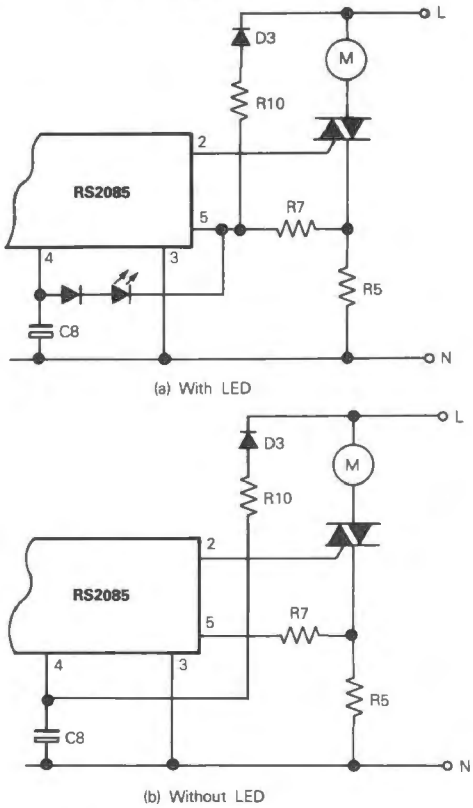
AC supply circuits

The RS2085 circuit has been designed for very low power consumption, this parameter being particularly important when operating from mains voltages via a dropper resistor.

When calculating the value of dropper resistor required additional currents such as those required by the control potentiometer on pin 10 or any other ancillary circuitry powered from the −5V or −15V supplies must be added to the IC supply current.

The circuit design whereby all critical control circuitry is powered from a −5V series stabilized supply ensures that the circuit is insensitive to ripple on the −15V line, thus enabling a single dropper resistor and capacitor to be used as shown in Figure 6.

Figure 6 **Mains supply circuits**



Component values can be calculated from

$$C8 = \frac{Is}{Vcr \times fm} \times 10^3 \mu F \quad \ldots 13$$

$$R10 = \frac{\sqrt{2}/\pi\, Vac - Vcc}{Is\ (mA)} \times 10^3 \Omega \quad \ldots 14$$

$$Pdr = \frac{(\sqrt{2}\, Vac - Vcc)^2}{4R10} \ W \quad \ldots 15$$

The low current requirement of the RS2085 reduces the power dissipation in the mains dropper resistor to below 2W, but in some cases even this level of power can be undesirable. By using a reactive feed arrangement the power loss in the dropper resistor is eliminated, but due to the phase shift introduced by the reactive feed capacitor, the multiplexing of current overload and LED drive on pin 5 will not function.

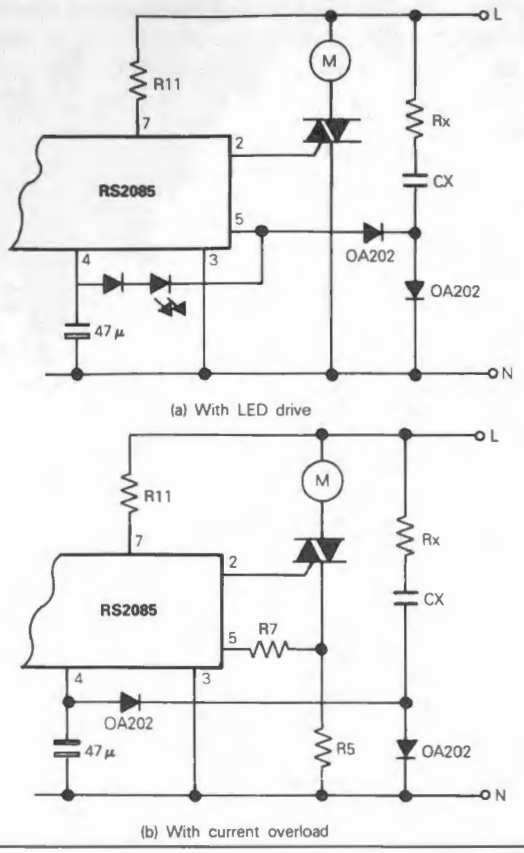
Figure 7a shows a reactive feed using the LED drive feature, and Figure 7b reactive feed with current overload.

The value of Cx can be calculated from

$$Cx = \frac{Is\ (mA)}{fm\ (2\sqrt{2}\, Vac - Vcc)} \times 10^3 \mu F \quad \ldots 16$$

Resistor Rx is included to limit current due to noise spikes on the supply, a value of 330Ω being suitable.

Figure 7 **Reactive feed circuits**



Operation from DC supplies

Operation from stabilized or unstabilized DC supplies is possible provided a signal in phase with the mains is available to drive the voltage sync input on pin 7.

If a stabilized supply is used, the voltage must always be set between the maximum shunt stabilizer voltage on pin 4 and the minimum voltage monitor enable level. Supplies outside these limits will prevent circuit operation or cause damage to the chip through excessive power dissipation.

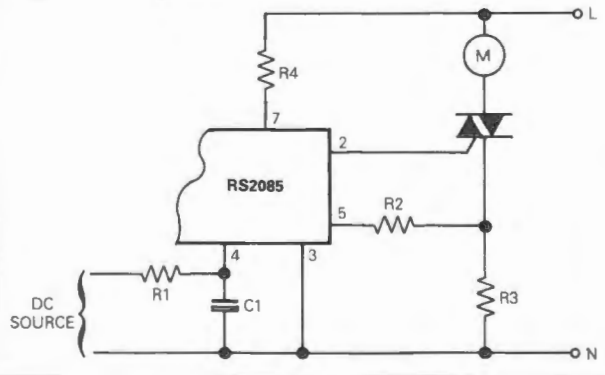
When operation from an unstabilized DC supply is required, the circuit shown in Figure 7 should be used, R1 value being calculated from

$$\frac{Vss - Vcc}{Is\ (mA)} \times 10^3\Omega \qquad ...17$$

To ensure a relatively constant current through R1 the unstabilized DC supply should be considerably higher than the shunt stabilizer voltage.

NB Worst case conditions should be used in the above equations.

Figure 8 **Operation from unstabilized DC**



Symbols used in text

Symbol	Function	Units
fm	Mains frequency	Hz
ft	Tacho frequency	Hz
Id	Pulse ramp discharge current	μA
Ir	Ramp current	μA
Is	Supply current	mA
Itg	Triac gate drive current	mA
K	Tacho conversion factor	mV/Hz
N	Number of tacho poles	–
Rg	Series triac gate resistor	Ohms
S	Motor speed	rpm
Vac	AC supply voltage (RMS)	V
Vbe	Transistor base emitter voltage	V
Vcc	Negative rail voltage pin 4	V
Vcr	Supply ripple voltage	V
Vf	Analogue feedback voltage	V
Vp	Phase control voltage	V
Vr	Ramp rate	V/s
Vreg	−5V series stabiliser voltage (pin 11)	V
Vrp	Dynamic ramp voltage	V
Vs	Internal speed reference voltage	V
Vss	Unstabilized DC supply voltage	V
Vtg	Triac gate voltage	V
V10	Speed program voltage on pin 10	V

Applications information

Universal motor applications

Figure 9 shows a typical universal motor closed loop speed control circuit suitable for use in domestic appliances such as food mixers or in electric drills. The circuit is basically that in the reference system diagram with the addition of component values which, with an 8 pole tacho give a speed range from zero to 15,000 rev/min.

Open loop control

Where an existing tapped resistor speed control is being updated or where speed regulation is relatively unimportant, an open loop control system may be adequate and provide a lower cost solution. A basic open loop system is shown in Figure 10, but if required, the LED and current overload circuits shown in Figure 9 may be added.

Current feedback

Another method of speed control possible with the universal motor is to use the increased motor current produced by loading to automatically increase the conduction angle of the control triac thus maintaining motor speed. A circuit designed to achieve this type of control using the RS2085 is shown in Figure 11. In this case, the normal average load current limiting voltage appearing at pin 8 is connected directly to the program input pin 10, providing a feedback signal of correct polairty. Since load current limiting starts when pin 8 voltage reaches −1V, the full range of phase control must be achieved within this limit. The dynamic working range of the error amplifier is 5V and to satisfy the 1V maximum limit on pin 8, the error amplifier is connected to have a gain of 5.7 using the resistors R5 and R4 between pins 12 and 13. Potentiometer VR1 provides the speed control sig-

nal but again the dynamic range must be limited to less than 1V, the resistors R1 and R2 giving a suitable reduction. The potentiometer VR2 is used to set the feedback level but in most cases a fixed resistor will suffice when a suitable level has been determined.

When considering this system of speed control it is most important to remember that the regulation is not as good as a true closed loop system and that the low speed range is limited.

Optical feedback

Most applications utilise a feedback signal derived from a tacho generator but there is no reason why other systems cannot be used. Figure 12 shows how a slotted optical coupler can be interfaced with few additional components. The feedback signal is produced by interrupting the light from the LED using a perforated disc attached to the motor shaft. By connecting the LED in series with the IC, sufficient current for operation is available without increasing dissipation in the mains dropper resistor. The capacitor and resistor associated with the LED are required to provide a smooth DC supply.

Current foldback

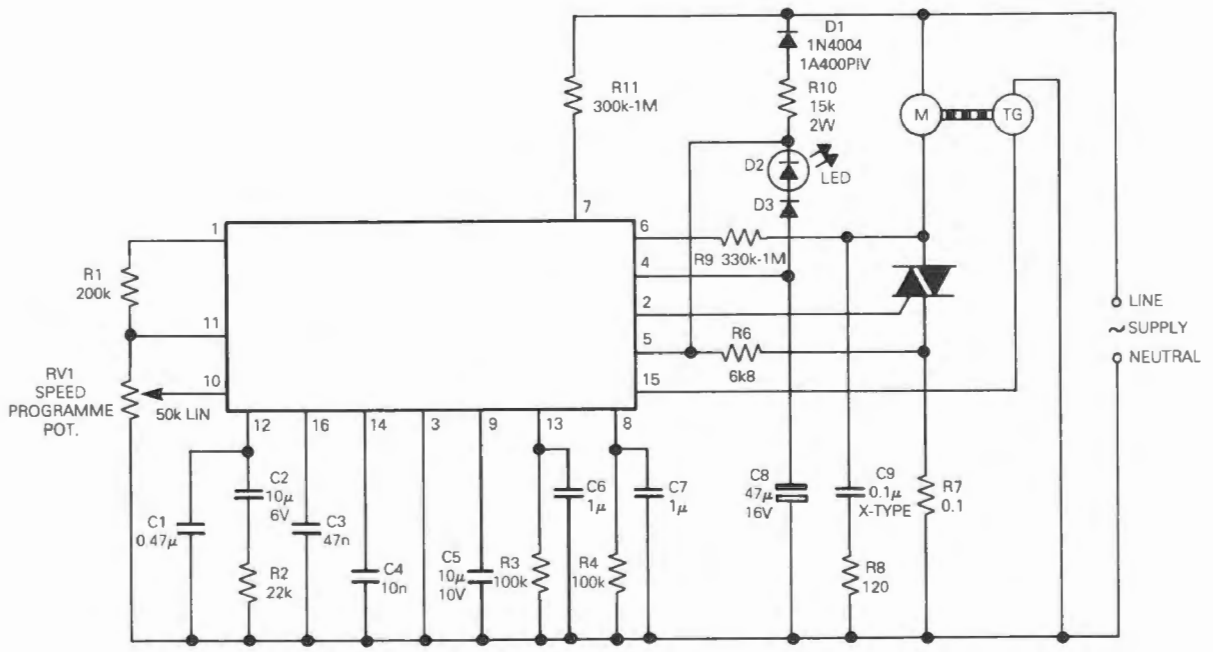
In some applications it is desirable to reduce the current overload point as the motor's speed is reduced, preventing the possibility of the motor overheating due to reduced fan cooling. Figures 13 and 14 show two possible methods of achieving foldback operation, together with graphs indicating the degree of overload current reduction for various component values.

Both circuits give similar results with the exception that the version shown in Figure 14 produces a fixed current overload point at settings close to maximum phase angle. This constant overload point will extend over about 15% of the control range.

Systems interfacing

The 5V stabilized supply available from the RS2085 allows standard CMOS logic elements to be powered directly thus enabling easy interface to a logic control system. Figure 15 shows a method of providing 16 speeds controlled by a 4 bit binary input from an isolated digital system. Digital information is transmitted via opto isolators to a single CMOS circuit powered from the RS2085, any 4 bit binary counter or latch being suitable. A simple D-A converter using a CA3046 transistor array produces a 16 step analogue output suitable for direct connection to the RS2085 control input. Where only on/off control is required, this can be accomplished by connecting pin 8 to −5V by using a transistor or relay contacts as shown in Figure 16a if the current limit on pin 5 is being used or by direct connection of a CMOS gate as in Figure 16b if current limiting is not employed. This method of control discharges the ramp capacitor at switch off, allowing controlled acceleration when power is again demanded.

Figure 9 **Universal motor application**



NOTE: A small capacitor may be required across the tacho coil to filter tacho noise at start-up.

Control of temperature

Although the RS2085 is primarily designed for speed control of electric motors, other types of load such as heating elements or lighting may also be controlled. Figure 17 shows a circuit for temperature control where the voltage on pin 13 set by a fixed resistor and NTC thermistor is compared with the reference voltage on pin 10. The value of Rt should be chosen to give equal voltages at pins 10 and 13 when the thermistor is at the required temperature.

Figure 10 **Open loop application, 240V**

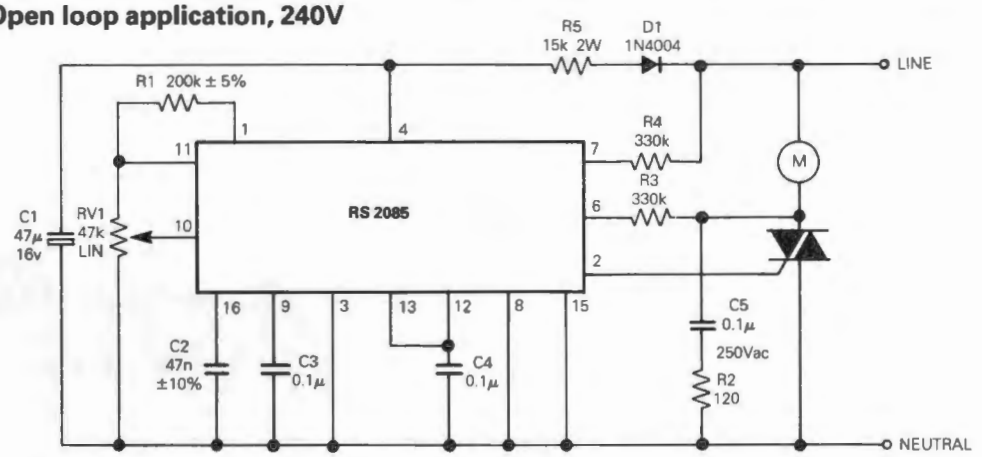


Figure 11 **Current feedback application**

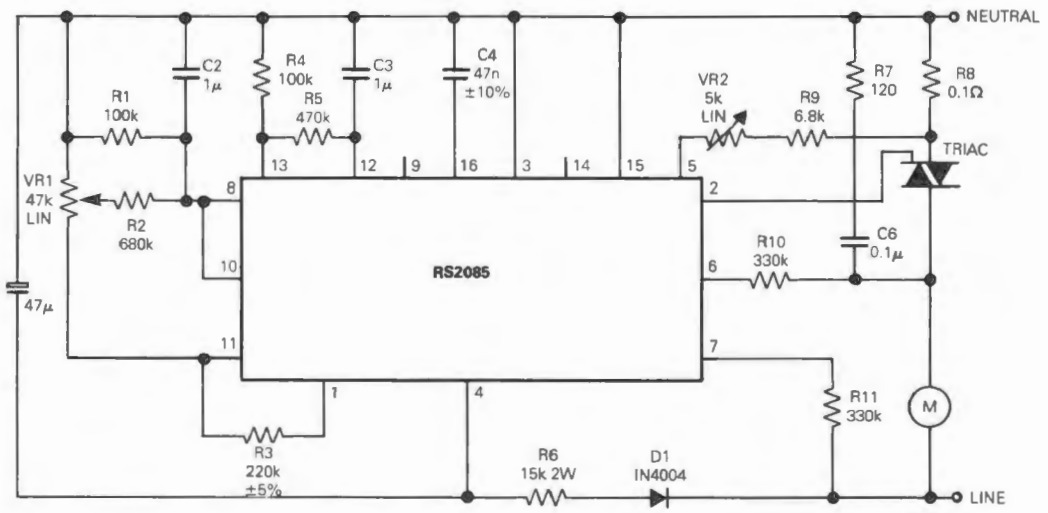


Figure 12 **Optical feedback application**

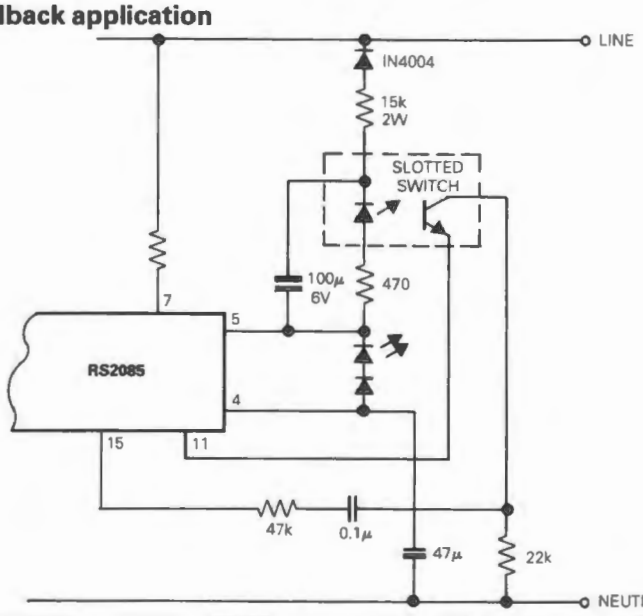


Figure 13 **Current limit foldback, method 1**

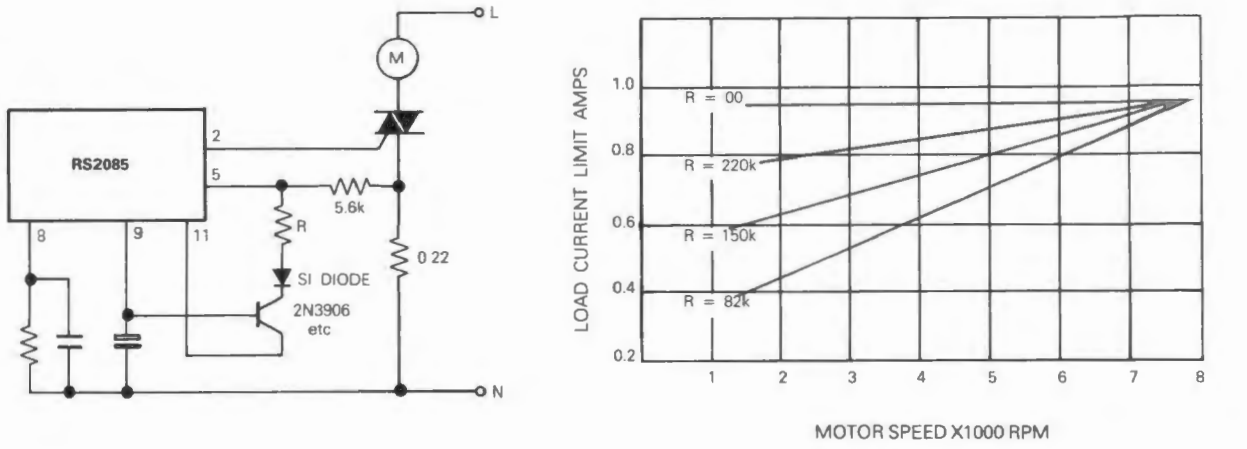


Figure 14 **Current limit foldback, method 2**

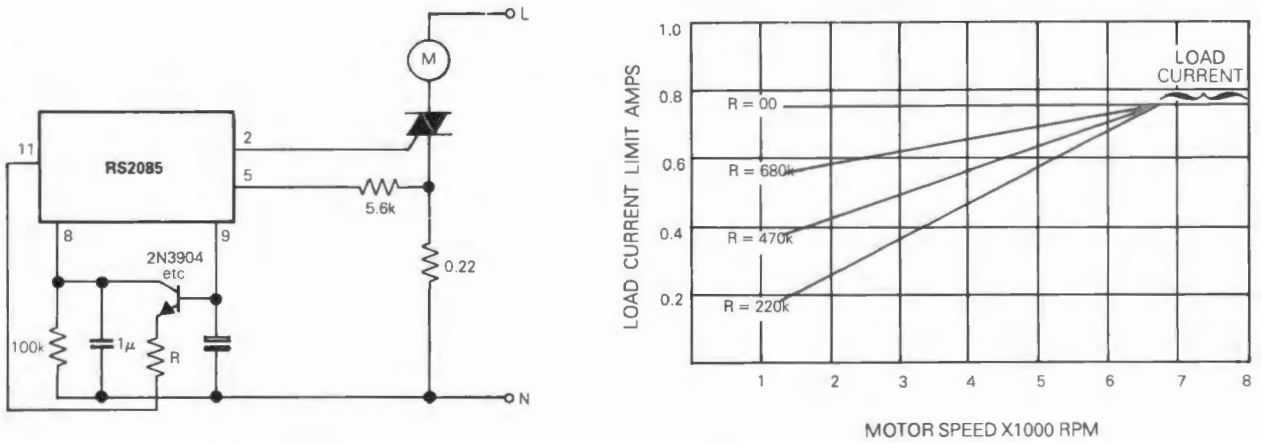


Figure 15 **Interface to digital system**

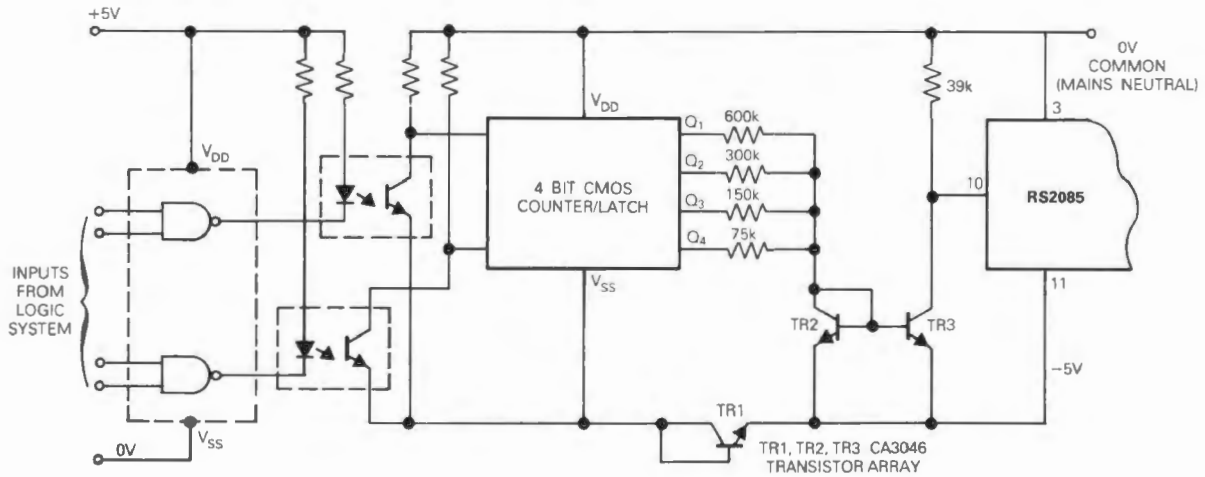


Figure 16 **On/Off control**

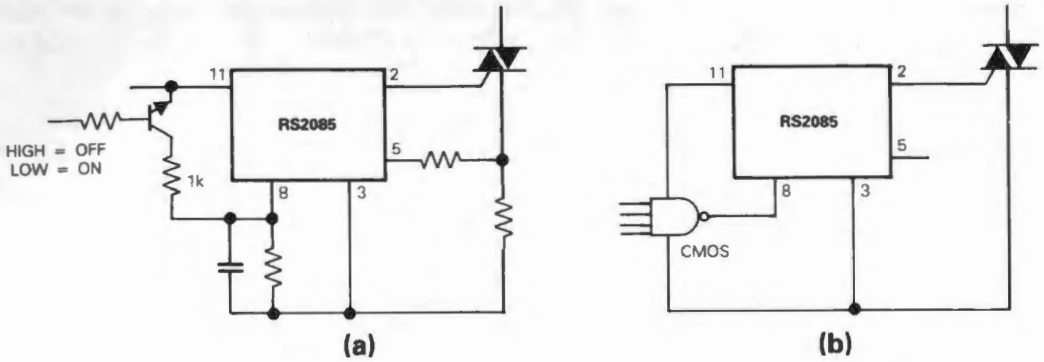
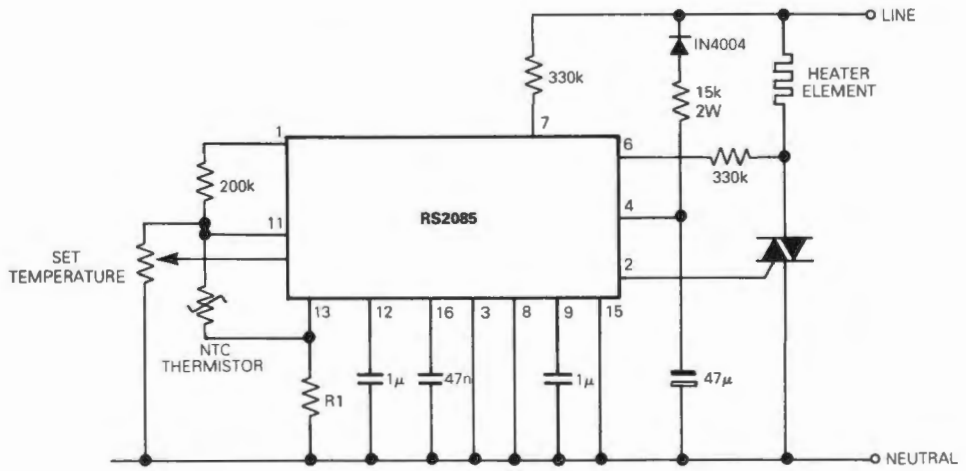


Figure 17 **Temperature control application**



Motor reversing

When the RS2085 is used in electric drills it is sometimes a requirement to reverse the direction of rotation. Unless some kind of interlock between the reversing switch and the on/off control is fitted, it is possible to damage the motor by operating the reversing switch whilst the motor is still running. To overcome this problem, it is necessary to remove power from the motor automatically when the reversing switch is operated.

It is not possible to give a precise method of achieving this as the best method depends on the design of the drill and the number of spare contacts available on the reversing switch. However in general the requirement is to rapidly discharge the soft start capacitor allowing the motor to come to rest and then to accelerate gently in the new direction.

Two methods of discharging the soft start capacitor are recommended.

1. Momentarily take pin 10 to within 50mV of the 0V rail (pin 3).
2. Momentarily take pin 8 more negative than the load current inhibit voltage with respect to pin 3. This is typically 1.5V.

RS data

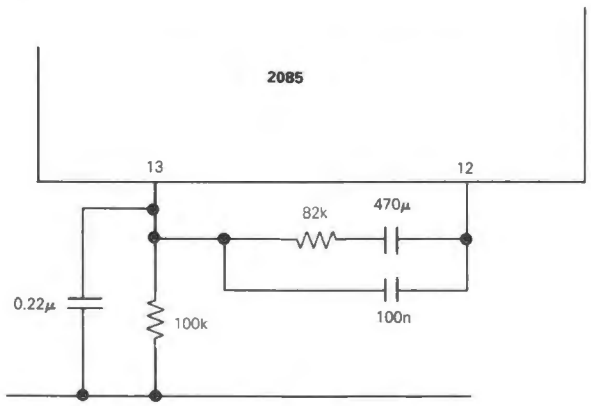
Start up delay

Problems may arise due to the finite time delay between the application of power to the tool and the motor starting to run. The problem is usually seen in closed loop applications and seems to affect some motors more than others.

There is no wholly satisfactory solution to this problem which is basically caused by the fact that many universal motors do not begin to turn until the applied voltage is as much as 30% of their full working voltage. At switch-on, the soft start and compensation circuit capacitors are all discharged; these capacitors must reach such a charge that the output of the error amp is about 1.5V before the motor will begin to rotate – this is the source of the time delay. Obviously, motors with large mechanical time constants (low -3dB frequency on their Bode Plot) will require heavy compensation and thus will be slow to start.

The problem can be alleviated by using an alternative compensation circuit. This circuit applies negative feedback around the error amplifier to generate the roll-off at HF, rather than slew-limiting the output as does the present circuit. The component values shown are typical for a large (700W) electric drill. With this circuit it was found that a satisfactory soft start was obtained without having to have a large capacitor on pin 9. The additional advantage of this technique is that no electrolytic capacitors are needed, apart from the main smoothing capacitor.

Figure 18 **Alternative compensation circuit**



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RS data

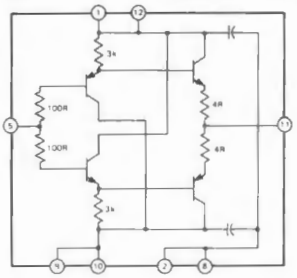
High speed buffer amplifier RS HOS 100

Stock number 303-264

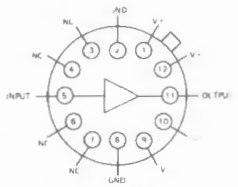
The RS HOS-100 high speed, bipolar, voltage follower/buffer amplifier is designed to provide high current drive at frequencies from D.C. to 125MHz. Featuring a slew rate of 1400V/μs, output drive of ±10mA into 1kΩ loads, excellent phase linearity (2°) and low distortion (<0.1%).

Ideal for wide range for buffer applications including high impedance input buffers for fast A to D convertors and comparators, coaxial cable drivers, yoke drivers in high resolution CRT displays etc.

Internal schematic



Top view



Applications

- Current boosters
- High speed A/D input buffers
- Coaxial cable drive
- High speed line drivers
- Video impedance transformation

Features

- Wide bandwidth - d.c. to 125MHz
- High slew rate - 1400V/μs
- Operating temperature range –25°C to +85°C
- High output drive ±10V with 100Ω load

Absolute maximum ratings

Supply voltage (V+ to V–) ——— 40V
Maximum power dissipation ——— 1.5W
Input voltage ——— Equal to supply voltage
Maximum continuous output current ——— ±100mA
Maximum peak output current ——— ±250mA
Operating temperature range (case) ——— 25°C to +85°C
Storage temperature ——— –65°C to +150°C
Lead temperature (soldering 10 sec) ——— +300°C
Maximum junction temperature ——— +175°C

Electrical characteristics

V_S = ±15V, R_L = 1kΩ, T_C = 25°C

*Applies over full temperature range –25°C to +85°C

Parameters	Conditions	Min	Typ	Max	Units
Input bias current Input impedance	 V_{IN} = 1V rms, f = 1kHz	 100	5 200	25	μA kΩ
Voltage gain	V_{IN} = 1V rms, f = 1kHz	0.94	0.96	1.0	V/V
Output offset voltage	R_S = 50Ω		10	25	mV
Output offset voltage T_C	R_S = 50Ω		25	75*	μV/°C
Output impedance	V_{IN} = 1V rms, f = 1kHz, R_S = 500Ω		8	12*	Ω
Output voltage swing	R_S = 50Ω V_S = ±5V	±12*	±13 6		V
Supply current	V_{IN} = OV, V_S = ±15, V_S = ±5		15 10	20	mA mA
Power consumption	V_{IN} = 0V		450	600	mW
Slew rate	V_{IN} = ±10V, R_S = 50Ω	1000	1400		V/μs
Bandwidth	V_{IN} = 1V rms, R_S = 50Ω	100	125		MHz
Rise time	ΔV_{IN} = 0.5V, R_S = 50Ω		2		ns
Propogation delay	ΔV_{IN} = 0.5V, R_S = 50Ω		1.5		ns
Phase nonlinearity	BW = 1 to 20MHz, R_S = 50Ω		2		Degrees
Harmonic Distortion	f>1kHz, R_S = 50Ω		<0.1		%

RS data

Typical performance curves

Figure 1 **Frequency response**

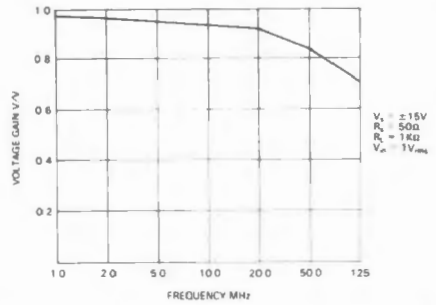


Figure 2 **Negative/positive pulse responses**

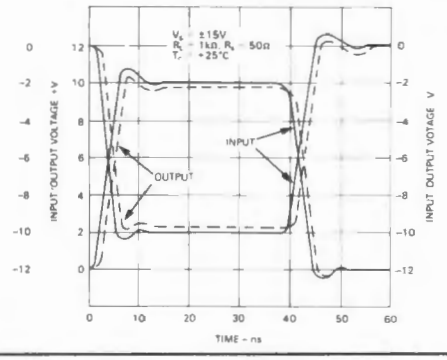


Figure 3 **Output offset voltage vs temperature**

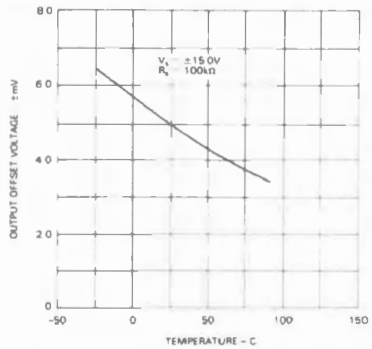
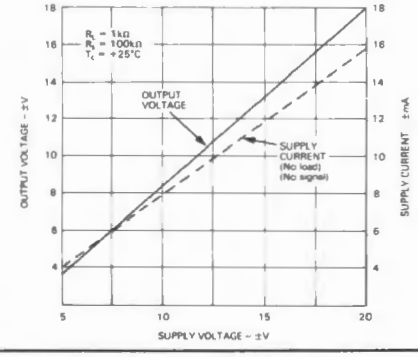


Figure 4 **Output voltage vs supply voltage**
Supply current vs supply voltage



Applications

Layout Considerations

As is the case with any high-speed design, proper layout is critical to avoid the introduction of unnecessary errors due to high-frequency coupling, stray capacitance, and the like.

Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as shielding the effects of high-frequency coupling. Sockets should be avoided, as the increased inter-lead capacitance can degrade bandwidth. Input and output connections should be kept as short as practical.

Capacitive Loading

The RS HOS-100 has been designed to drive capacitive loads of several thousand picofarads (such as coaxial cable) without oscillation. In these applications, peak current resulting from (C × dv/dt) should be limited below the absolute maximum peak current rating of ±250mA.

Also, power dissipation due to driving capacitive loads plus standby power should be kept below the total power rating of 1.5W.

Typical Applications

Figure 5 **Current booster**

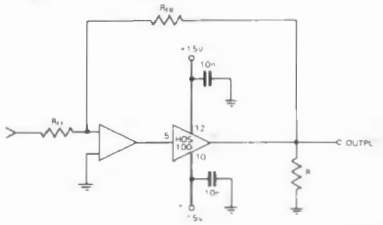


Figure 6 **Coaxial cable driver**

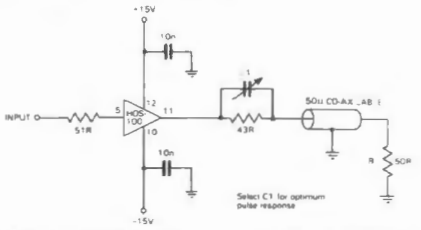
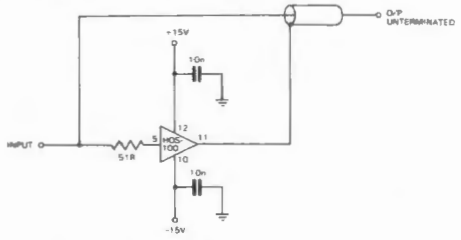


Figure 7 **High speed shield/line driver**



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An Electrocomponents Group Company

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RS data

Direct on line (D.O.L.) starter 5.5 H.P. 415V. a.c.

3 pole direct on line a.c. starters, conforming to BS 4941, IEC 292-1 and VDE 0660, housed in compact double insulated enclosures having a degree of protection to IP42. The starters are available with either 240V 50Hz or 415V 50Hz operating coils and are supplied with all necessary interconnection links. Overload relays are available separately, and should be selected according to the motor full load current (refer to table below).

Features

- Environmental Protection to IP42.
- Easily fixed and wired.
- Double insulated Makrolon® enclosure.
- Compact design.
- Generous space for connections.
- Auxiliary IN/O – IN/C contact block can be added.

(see over)

Ratings

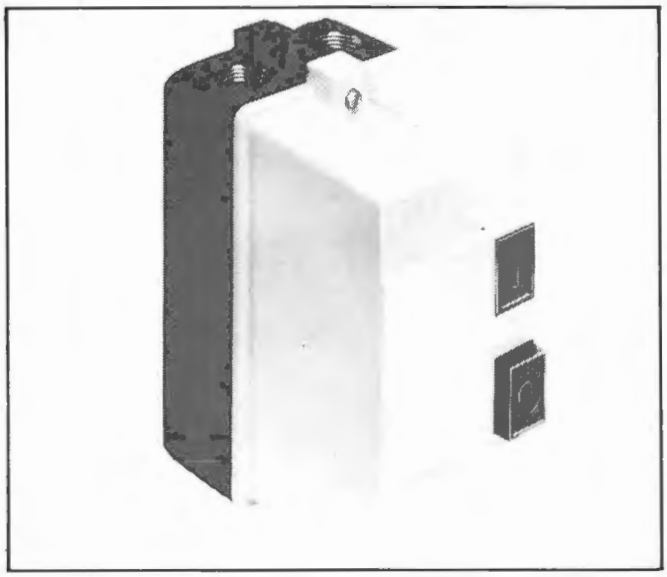
Max. rating 3 phase connected ——— 5.5hp (4.0kW)
Max. rating single phase connected – 1.5hp (1.1kW)

Coil data

240V 50Hz as in RS stock number 348–481
(Spare coil – RS stock number 347–624)
415V 50Hz as in RS stock number 348–497
(Spare coil – RS stock number 347–602)

Cable entry

Four PG 13.5 threaded but sealed cable entries are provided (two top, two bottom) For 20mm conduit entry, just knock out the seal at desired entry point/s and use PG 13.5/M20 conduit adaptors (RS stock number 547–420).



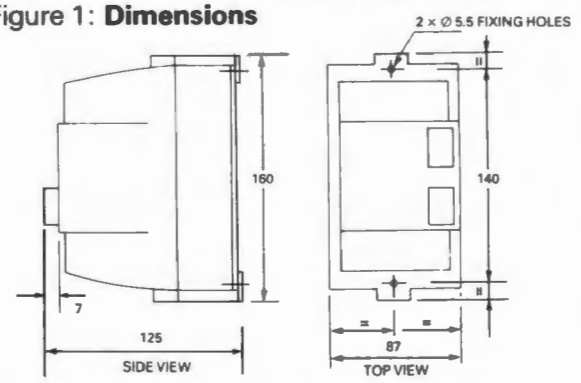
Approximate full load current for AC motors (Amps)

kW	hp	Three phase 50Hz 380V	Three phase 50Hz 415V	Single phase 50Hz 220V	Single phase 50Hz 240V
0.18	0.25	0.72	0.62	2.2	2.0
0.37	0.50	1.15	1.05	3.88	3.56
0.55	0.75	1.58	1.44	5.20	4.77
0.75	1.00	2.02	1.85	6.59	6.04
1.1	1.5	2.99	2.74	9.60	8.80
1.5	2.0	3.94	3.60	—	—
2.2	3.0	5.78	5.29	—	—
3.0	4.0	7.50	6.87	—	—
4.0	5.5	9.16	8.39	—	—

Overload relay selection guide	
FLC Range (Amps)	O/L Relay RS stock number
0.63–1.00	347–444
1.00–1.60	347–438
1.60–2.50	347–422
2.50–4.00	347–416
4.00–6.00	347–400
5.50–8.00	347–393
7.00–10.00	347–387

RS data

Figure 1: **Dimensions**

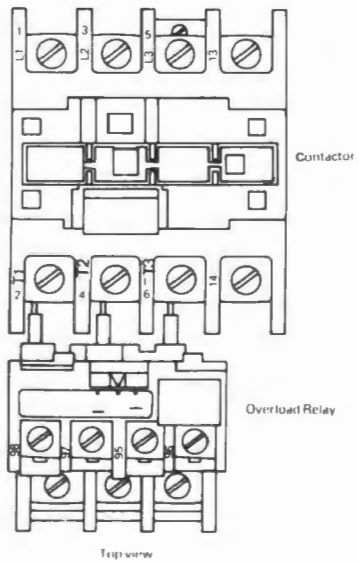


Overload relay

Thermal overload relays should be fitted to contactors in the position shown in Figure 2.

Having chosen an overload relay with the correct full load current (using the FLC table or motor manufacturers data), the final trip current should be set using the pointer on top of the relay.

Figure 2: **Overload relay mounting**



Instantaneous auxiliary contact block

An IN/O–IN/C instantaneous contact block (347–292) can be fitted by clipping the block onto the contactor as detailed in Figure 3.

For removal, the latch is raised and the block is slid off, see Figure 4.

Figure 3: **Fitting auxiliary contact blocks**

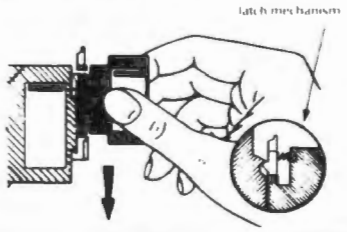
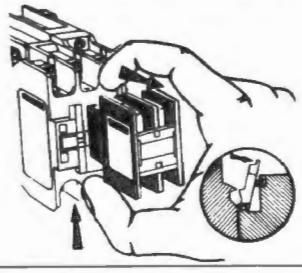


Figure 4: **Removal of auxiliary contact blocks**



Connection diagrams

Interconnection links Ⓐ and Ⓑ are provided wired to the contactor and should be connected to the overload relay terminals 95 and 96 respectively as shown below.

Figure 5: **Local control 3 phase supply**

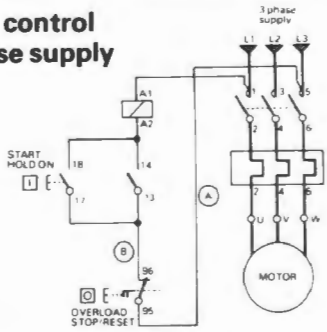
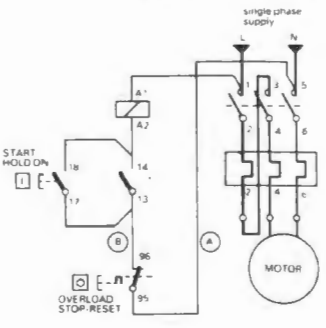


Figure 6: **Local control single phase supply**



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Telephone: 0536 201234
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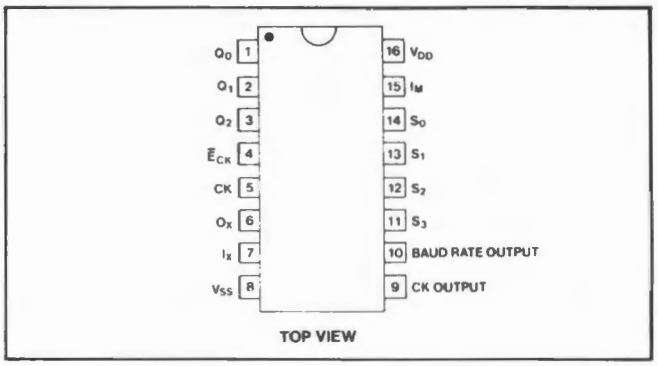
RS data

Baud rate generator i.c. 4702B

Stock Number 303-517

The 4702B baud rate generator i.c. provides clock signals for digital data transmission systems such as universal asynchronous receiver and transmitter circuits. Any of the 14 commonly used baud rates may be generated from an external clock source or by using the on-chip crystal oscillator circuit. Multi-channel operation is also possible where different output frequencies are available simultaneously.



Features

- Provides 14 commonly used baud rates
- Uses standard 2.4576 Mhz crystal
- On-chip pull-up circuits
- TTL compatible outputs
- Low power operation

Absolute Maximum Ratings

Supply Voltage V_{DD} ——— −0.5 to +5.5V
Data Input Voltage ——— −0.5 to (V_{DD} +0.5)V
Operating Temperature Range ——— −40°C to +85°C
Storage Temperature Range ——— −65°C to +150°C

Electrical Characteristics T_A = 25°C V_{DD} = 5V, V_{SS} = OV

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply voltage	V_{DD}		4.5	5	5.5	V
Input high voltage	V_{IH}		3.5			V
Input low voltage	V_{IL}				1.5	V
Output high voltage	V_{OH}	$I_{OH} < 1\mu A$ Inputs at 1.5 or 3.5V	4.5			V
Output low voltage	V_{OH}	$I_{OL} < 1\mu A$ Inputs at 1.5 or 3.5V			0.5	V
Input low current — Ix	I_{OL}	Input under test at OV, all other			1	μA
— all other inputs		inputs at 5V	−15	−30	−100	μA
Input high current all inputs	I_{IH}	All other inputs at OV			1	μA
Output high current — Ox	I_{OH}	V_{OUT} = 4.5V	−0.1			mA
— all other outputs		V_{OUT} = 4.5V	−0.3			mA
Output low current — Ox	I_{OL} =	0.4V	0.1			mA
— all other outputs		V_{OUT} = 0.4V	1.6			mA
Quiescent power supply current	I_{DD}	E_{CK} = V_{DD} CK = OV			1	mA
		All other inputs at OV or V_{DD}			1	mA

A.C. Characteristics $T_A = 25°C$, $V_{DD} = 5V$, $V_{SS} = OV$, $C_L = 50pF$, $R_L = 200\ K\Omega$, Input transition time $< 20ns$, $C_L < 7pF$ on O_X.

Parameter	Symbol	Min	Typ	Max	Units
Propagation delay Ix to CK output	t_{PLH}		175	350	ns
	t_{PHL}		135	275	ns
Propagation delay CK to CK output	t_{PLH}		130	260	ns
	t_{PLH}		110	220	ns
Propagation delay CK output to Qn	t_{PLH}		53	367	ns
	t_{PLH}		45	367	ns
Propagation delay CK to baud rate output	t_{PLH}		37	85	ns
	t_{PHL}		32	75	ns
Output transition Time (except Ox)	t_{TLH}		80	160	ns
	t_{THL}		35	75	ns
Set up time select to CK output	t_s	350	185		ns
Hold time select to CK output	t_h		−182		ns
Set up time I_M to CK output	t_s	350	190		ns
Hold time I_M to CK output	t_h	0	+182		ns
Minimum clock pulse width low	$t_{wCK(L)}$	120	60		ns
high	$t_{wCK(H)}$	120	60		ns
Minimum Ix pulse width low	$t_{wIx(L)}$	160	75		ns
high	$t_{wIx(H)}$	160	75		ns

Description

The 4702B baud rate generator provides a wide range of output frequencies ranging from 50 baud for interfacing with electromechanical devices to 9600 baud for high speed modems. The circuit contains the following five functional subsystems.

Oscillator

This circuit generates 16 output clock pulses per bit period from an input clock frequency of 2.4576Mhz. Standard UART circuits use a clock that is 16 times the transmitted baud rate. It may be driven from two alternative clock sources. 1, with E_{CK} at a logic low level the CK input is the clock source. 2, when the E_{CK} input is high a crystal connected between 1_X and O_X is the input clock source.

Scan counter

The clock frequency is output on the CK output pin. This is internally applied to a ÷ 8 prescaler with buffered outputs Q_0, Q_1 and Q_2. This allows simple multichannel operation as shown in figure 3.

Counter network

The scan counter output Q_2 is a square wave of 1/8 the input frequency and drives the frequency counter network which generates the 13 output baud rates. See figure 1. The 134.5 baud rate has a frequency error of −0.87% and the 110 baud rate a frequency error of −0.83%. The division of 16/3 is performed by alternating the divide ratio between 5 twice and 6 once. The result is an exact average output frequency with some frequency modulation. When the divide by 16 feature of the UART is considered the resulting distortion in output frequency is less than 0.78%. All the output signals have a 50% cycle except for the 1800 baud output.

Output multiplexer

The outputs from the counter network (figure 1) are fed to a 16-input multiplexer, which is controlled by the rate select inputs (S_0 to S_3). The multiplexer output is resynchronized with the incoming clock in order to cancel all cumulative delays and present an output signal that is synchronous with the scan counter outputs (Q_0 to Q_2). The output baud rate for each select code is shown in table 1. Note two codes select an I_M input allowing a zero baud or special rate to be fed to the output from this input.

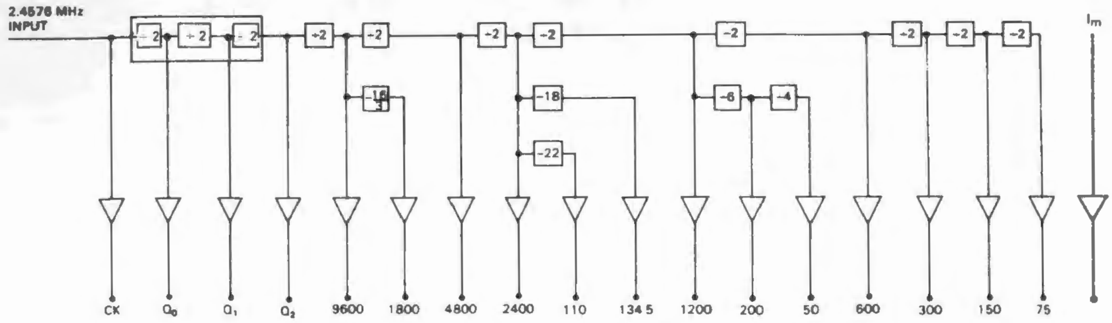
Initialization Reset

This circuit generates a common master reset signal for all the internal flip-flops. This signal is derived from a digital differentiator that senses the first high level on the CK input after E_{CK} goes low. When E_{CK} is high, selecting the crystal input, CK must be low. A high level on CK would apply a continuous reset.

Table 1 Truth table for baud rate select inputs

S_3	S_2	S_1	S_0	Baud rate output	Actual output frequency (H_z)
L	L	L	L	Multiplexed input (I_m)	
L	L	L	H	Multiplexed input (I_m)	
L	L	H	L	50	800
L	L	H	H	75	1200
L	H	L	L	134.5	2152
L	H	L	H	200	3200
L	H	H	L	600	9600
L	H	H	H	2400	38400
H	L	L	L	9600	153600
H	L	L	H	4800	76800
H	L	H	L	1800	2880
H	L	H	H	1200	19200
H	H	L	L	2400	38400
H	H	L	H	300	4800
H	H	H	L	150	2400
H	H	H	H	110	1760

Figure 1: **Figure 1:**



OUTPUTS TO OUTPUT MULTIPLEXER

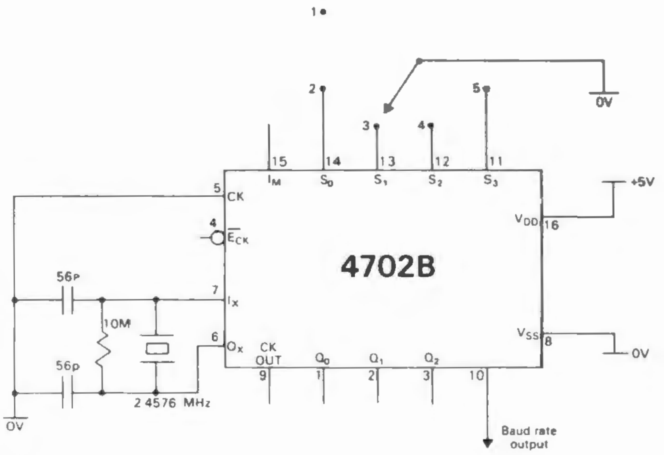
Applications

Single channel baud rate generator

Figure 2 shows a simple single channel application. This circuit generates one of five common bit rates with a single pole five position switch. The output drives one standard LSTTL load and for many applications these five standard rates are adequate.

Figure 2: **Switch selectable baud rate generator**

Switch position	Baud rate
1	110
2	150
3	300
4	1200
5	2400

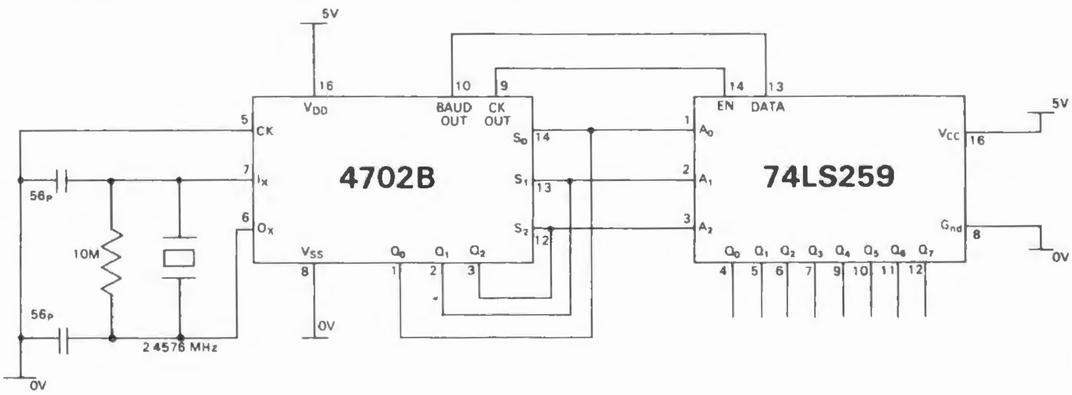


Multichannel baud rate generator

Figure 3 shows a simple circuit which generates eight baud rates on eight output lines with the use of a 74LS259 addressable latch. This circuit uses the scan counter outputs which go through a complete sequence of eight states for every half period of the highest output frequency (9600 baud). Feeding these scan counter outputs back to the select inputs of the multiplexer causes the 4702B to interrogate sequentially the state of eight different frequency signals. The addressable latch also addressed by the scan counter reconverts the multiplexed signal output into eitght parallel output frequency signals.

Figure 3: **This circuit simultaneously produces eight different output baud rates.**

74LS259 output	Baud rate
Q_0	110
Q_1	9600
Q_2	4800
Q_3	1800
Q_4	1200
Q_5	2400
Q_6	300
Q_7	150



Additional features

19200 baud operation is possible by connecting Q_2 output to I_M on the 4702B. A select code of 0 or 1 then gives this baud output. One 4702B can control up to eight parallel output channels. Additional devices can be run from one crystal controlled 4702B by using the clock as a master clock generator.

RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

8 Bit D to A Converter I.C. ZN 428

Stock number 303-523

The ZN428 is a Monolithic 8 bit D to A converter with input latches to facilitate up-dating from a data bus. The latch is transparent when ENABLE is LOW and the data is held when ENABLE is taken HIGH. The ZN428 also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

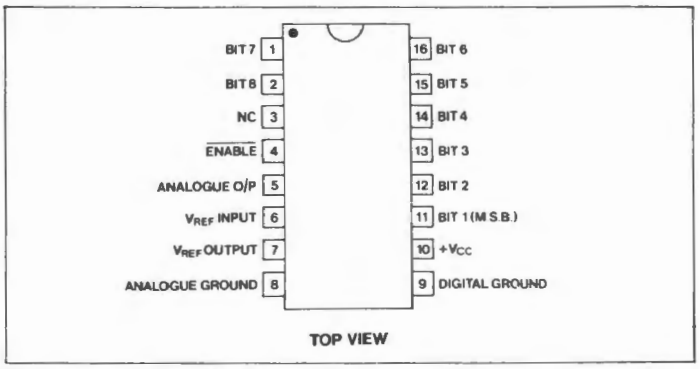
Absolute maximum ratings

Supply voltage V_{CC} ——— +7.0 volts
Max. voltage, logic and V_{REF} input ——— $+V_{CC}$
Operating temperature range ——— 0°C to +70°C
Storage temperature range ——— −55°C to +125°C
Analogue ground to digital ground ——— ±200mV

Notes
1. See reference section
2. $R_L = 10M\Omega$, $C_L = 10pF$
3. All inputs HIGH ($V_{IH} = 3.5$ volts).
4. Set up time before $\overline{\text{ENABLE}}$ goes high.
5. Hold time after $\overline{\text{ENABLE}}$ goes high.

Features

- Contains DAC with data latch and on-clip reference.
- Guaranteed monotonic over the full operating temperature range.
- Single +5V supply.
- TTL and 5V CMOS compatible.
- 800ns settling time.
- Microprocessor compatible.
- Complementary to ZN427 A to D series.

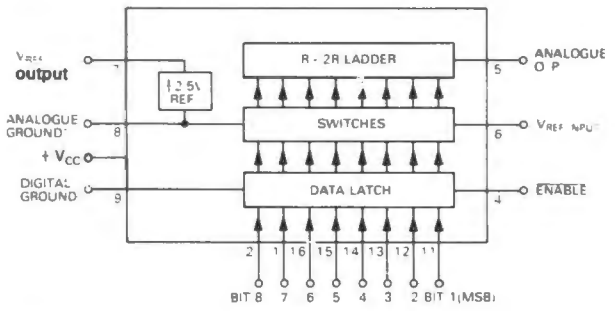


TOP VIEW

Electrical Characteristics $V_{CC} = +5$ volts, $T_{amb} = 25°C$ unless otherwise specified.

Parameter	Conditions	Min	Typ.	Max.	Units
Supply voltage (V_{cc})		4.5	5.0	5.5	volts
Supply current	Note 3		20	30	mA
Power consumption			100		mW
INTERNAL VOLTAGE REFERENCE					
Output voltage	$R_{REF} = 390\Omega$	2.475	2.550	2.625	volts
Slope resistance	$C_{REF} = 1\mu F$		0.5	2	Ω
$V_{REF\ OUT}$ T.C.			50		ppm/°C
Reference current	Note 1	4		15	mA
D TO A CONVERTER					
Linearity error	$2.0V \leq V_{REF\ IN} \leq 3.0V$			±0.5	LSB
Differential non-linearity			±0.5		LSB
Linearity error T.C.			±3		ppm/°C
Differential non-linearity T.C.			±6		ppm/°C
Offset voltage	All bits OFF		2	5	mV
Offset voltage T.C.			±6		µV/°C
Full scale output	External reference $V_{REF\ IN} = 2.560$ volt	2.545	2.550	2.555	
Full scale output T.C.	all bits ON		2		ppm/°C
Analogue output resistance			4		kΩ
External reference voltage		0		3.0	volts
Settling time to 0.5 LSB	1 LSB Major Transition (Note 2)		800		ns
	All bits ON to OFF or OFF to ON (Note 2)		1.25		µs
High level input voltage		2.0			V
Low level input voltage				0.8	V
High level input current	$V_{IN} = 5.5V$, V_{CC} = Max.			60	µA
	$V_{IN} = 2.4V$, V_{CC} = Max.			20	µA
Low level input current	$V_{IN} = 0.4V$, V_{CC} = Max.			−5	µA
$\overline{\text{ENABLE}}$ pulse width		100			ns
Data set-up time	Note 4	150			ns
Data hold time	Note 5	10			ns

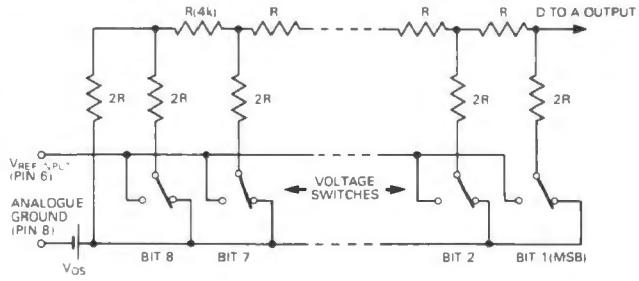
Figure 1. **System diagram**



D to A converter

The converter is one of the voltage switching type and uses an R-2R ladder network as shown in Figure 2. Each 2R element is connected to OV or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-R2 ladder.

Figure 2. **The R-2R Ladder network**



$$\text{Analogue Output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the data latch.

V_{OS} is a small voltage produced by the D to A switch currents flowing through the packaged lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see APPLICATIONS) and because the offset temperature coefficient is low ($\pm 6\mu V/°C$) the effect on accuracy is negligible.

Figure 3 **Analogue output equivalent circuit**

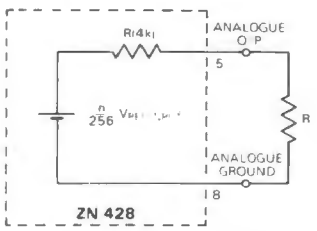


Figure 3 shows an equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per°C.

The gain drift to this is $\frac{0.2R}{R+R_L}$ % per °C

RL should be chosen to be as large as possible to make the gain drift small. As an example if R_L = 400kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN428 can be buffered by an amplifier.

Voltage reference

Internal reference

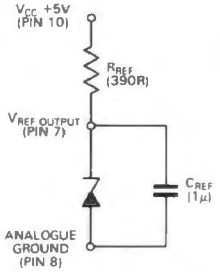
The internal reference is an active band gap circuit which is equivalent to a 2.5 volt Zener diode with a very low slope impedance (Figure 4). A resistor (R_{REF}), should be conncted between $+V_{CC}$ (pin 10) and pin 7. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor, C_{REF} = 1μF is required between pins 7 and 8 for internal reference operation, $V_{REF\ OUTPUT}$ (pin 7) being connected to $V_{REF\ INPUT}$ (pin 6).

Up to five ZN428's may be driven from one internal reference (there is no need to reduce R_{REF}). This useful feature saves power and gives excellent gain tracking between the converters.

External reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than 2.5/n Ω, where n is the number of converters supplied. $V_{REF\ IN}$ can be varied from 0 to + 3 volts for ratiometric operation. The ZN428 is guaranteed monotonic for $V_{REF\ IN}$ above 2 volts.

Figure 4 **Internal voltage reference**



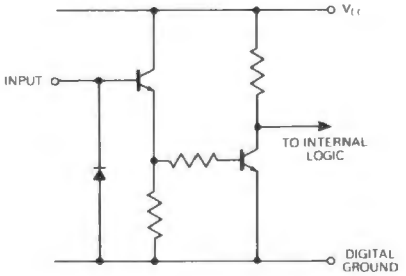
Data inputs

INPUT coding is binary for unipolar operation and offset binary for bipolar operation. When the $\overline{\text{ENABLE}}$ input is low the data inputs drive the D to A directly. When $\overline{\text{ENABLE}}$ goes high the input data word is held in the data latch.

The equivalent circuit for the data and $\overline{\text{ENABLE}}$ inputs is shown in Figure 5.

The ZN428 is provided with separate analogue and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

Figure 5. **Equivalent circuit of all digital inputs**



Applications

Unipolar D to A converter

The nominal output range of the ZN428 is 0 to $V_{REF\ INPUT}$ through a 4kΩ resistance. Other output ranges

can readily be obtained by using an external amplifier.

The general scheme (Figure 6) is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full scale range is given by

$$V_{OUT}\,FS = \left(\frac{1 + R_1}{R2}\right) V_{REF\,IN} = G.\,V_{REF\,IN}$$

The impedance at the inverting input is R_1/R_2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4kΩ). The required nominal values of R_1 and R_2 are given by R1 = 4G kΩ and R2 = 4G/(G-1)kΩ.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\,INPUT}$ = 2.5V

Table 1. Nominal values of R_1 and R_2

Output range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

For gain setting, R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5V and +10V output ranges are also shown (Figures 7 and 8). Settling time for a major transition is 1.5μs typical.

Figure 6 **Unipolar operation — basic circuit**

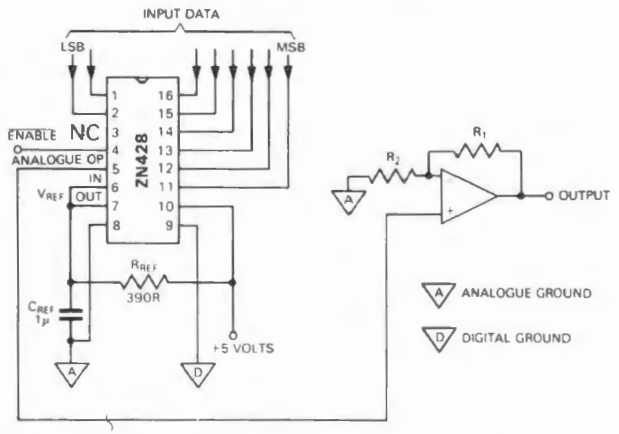
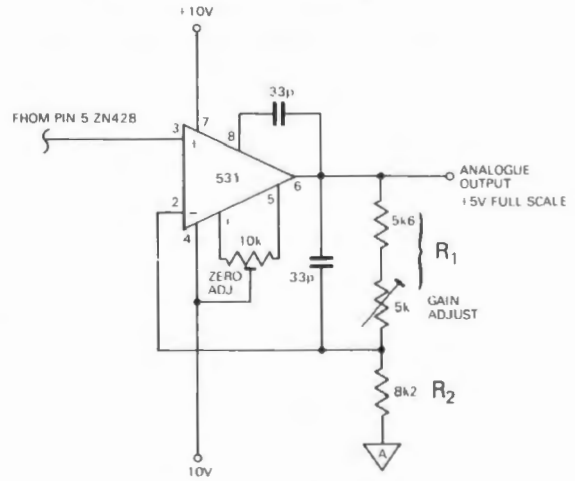


Figure 7 **+5V Full scale actual circuit**



Unipolar adjustment procedure

(i) Set all bits to OFF with ENABLE low and adjust zero until V_{OUTPUT} = 0.0000V.

(ii) Set all bits ON (high) and adjust gain until V_{OUTPUT} = FS-1 LSB.

Table 2. Unipolar setting up points

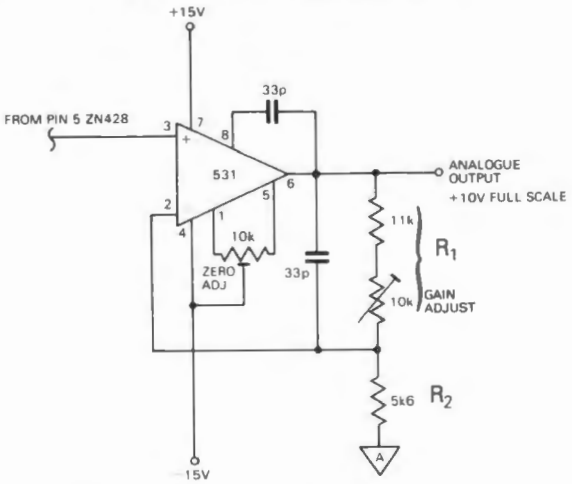
Output range, +FS	LSB	FS − 1LSB
+5V	19.5 mV	4.9805V
+10V	39.1 mV	9.9609V

Note:
1 LSB = $\frac{FS}{256}$

Table 3. Unipolar logic coding

Input Code (Binary)	Analogue Ouput (Nominal value)
11111111	FS − 1 LSB
11111110	FS − 2 LSB
11000000	¾FS
10000001	½FS + 1 LSB
10000000	½FS
01111111	½FS − 1 LSB
01000000	¼FS
00000001	1 LSB
00000000	0

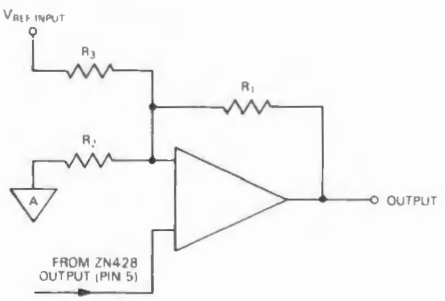
Figure 8 **+10V Full scale actual ciruit**



Bipolar D to A converter

For bipolar operation the output from the ZN428 is offset by half full scale by connecting a resistor R_3 between $V_{REF\,INPUT}$ and the inverting input of the buffer amplifier (Figure 9).

Figure 9: **Bipolar operation — basic circuit**



RS data

Figure 10. **±5V Full Scale actual circuit**

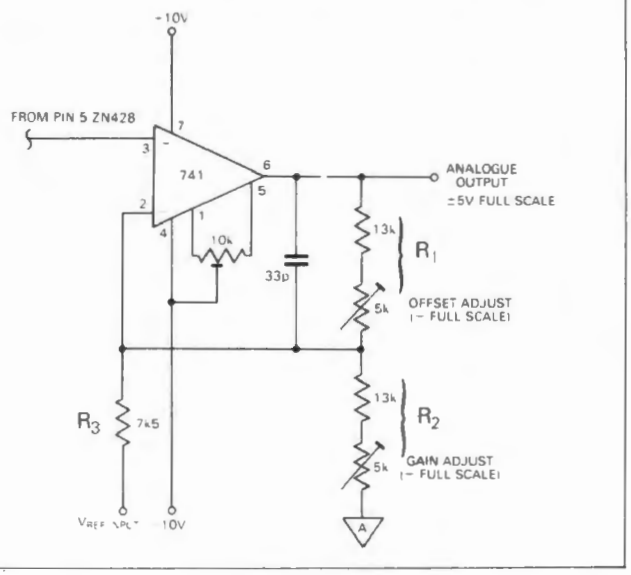
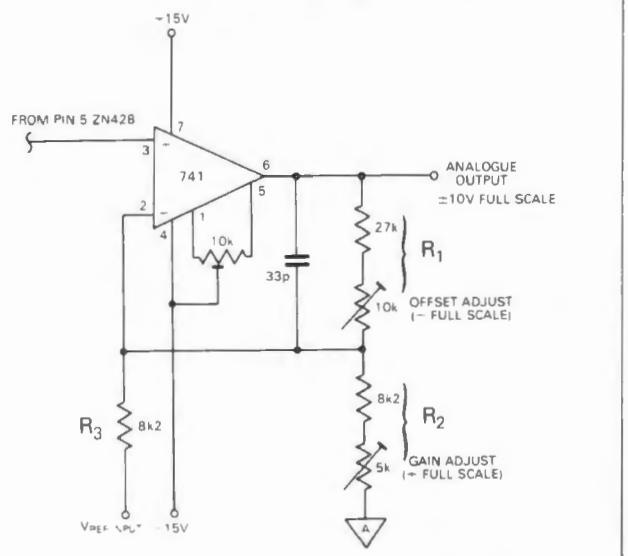


Figure 11. **±10V Full Scale actual circuit.**



When the digital input to the ZN428 is zero the analogue output is zero and the amplifier output should be -Full scale. An input of all ones to the D to A will give a ZN428 output of $V_{REF\ INPUT}$ and the amplifier output required is +Full scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 4kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by R_1 = 8G kΩ, R_2 = 8G/(G-1) kΩ and R_3 = 8kΩ
where the resultant output range is ±G $V_{REF\ INPUT}$.

A bipolar output range of ± $V_{REF\ INPUT}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ INPUT}$) is obtained if R_1 = R_3 = 8kΩ and R_2 = ∞.

Assuming the $V_{REF\ INOUT}$ = 2.5 volts the nominal values of resistors for ±5V and ±10V output ranges are given in the following table:

Table 4. Nominal values of R_1, R_2 and R_3

Output range	G	R_1	R_2	R_3
±5V	2	16kΩ	16kΩ	8kΩ
±10V	4	32kΩ	10.66kΩ	8kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are also shown (Figures 10 and 11). Note that in the ±5V case R_3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5μs typical.

Bipolar adjustment procedure

(1) Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust offset until the amplifier output reads — Full Scale.
(2) Set all bits ON (high) and adjust gain until the amplifier output reads +(Full Scale -1 LSB).

Table 5. Bipolar setting up points

Input range, ±FS	LSB	−FS	+(FS − 1 LSB)
±5V	39.1 mV	−5.0000V	+4.9609V
±10V	78.1 mV	−10.0000V	−9.9219V

Note:
1 LSB = $\frac{2FS}{256}$

Table 6. Bipolar logic coding

Input Code (Offset Binary)	Analogue Ouput (Nominal Value)
11111111	+ (FS − 1 LSB)
11111110	+ (FS − 2 LSB)
11000000	+ ½FS
10000001	+ 1 LSB
10000000	0
01111111	− 1 LSB
01000000	− ½FS
00000001	− (FS − 1 LSB)
00000000	− FS

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RS data

R.F./I.F. Amplifier i.c. RS1612C

Stock number 303–208

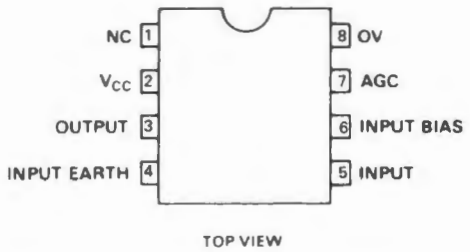
A versatile R.F./I.F. amplifier i.c. in an 8 pin D.I.L. plastic package. Featuring low power consumption, 15MHz bandwith, high voltage gain and 70dB AGC range.

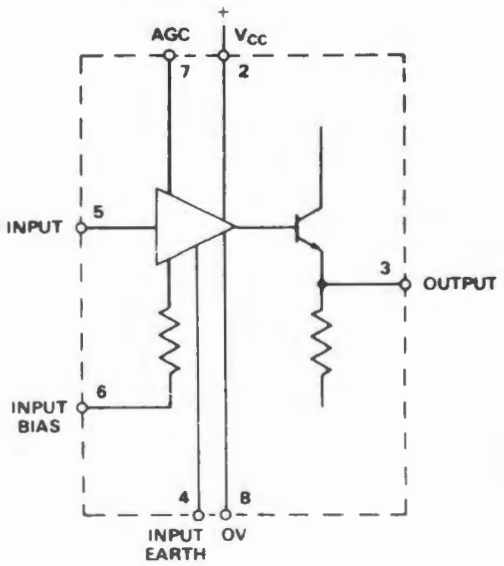
Absolute maximum ratings

Supply voltage ——— +12V d.c.
Storage temperature ——— –55°C to 125°C

Features

- Wide AGC range 70dB typ.
- Integral R.F. power supply decoupling.
- 15MHz 3dB bandwidth
- Low current consumption 3.3mA typ.
- High voltage gain 34dB typ.





Electrical characteristics (V_{CC} = 6V, T_A = –30 to +70°C, f = 1.75MHz)

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply current	No signal, pin 3 open circuit		3.3	6	mA
Voltage gain	R_S = 50Ω, R_L = 500Ω, T_{amb} = 22°C	31	34	38	dB
Cut-off frequency (–3dB)			15		MHz
Noise figure	R_S = 800Ω		3		dB
Max output signal (max AGC) Max input signal (max AGC)	R_L = 1.2kΩ		1.0 250		V_{rms} mV_{rms}
AGC range	Pin 7 = 0V to 5.1V	60	70		dB
AGC current	Current into pin 7 at 5.1V		0.15	0.6	mA

AGC and earthing

There are seven connections to the RS 1612C, an input, an input bias point, an AGC input, the output, the positive supply pin and two earths – for input and output respectively.

The positive supply should be 6V, but the devices will function at supplies of up to 9V. Since internal HF supply decoupling is incorporated a certain amount of HF ripple can be tolerated in the supply. LF ripple should be kept down as it can cause intermodulation – especially at large HF signal levels – and 10mV rms of LF ripple should be considered maximum.

The AGC characteristic is shown in Figure 1a. It is temperature dependent, so that while a potentiometer may be used to provide a gain control voltage the gain so defined will not be temperature stable to better than ±2dB. The AGC terminal will normally draw about 150 microamps at 5V. Figure 1b shows the frequency response of the RS 1612C.

There are two earth connections: pin 4 is the input earth and pin 8 the output earth. When several devices are cascaded pin 8 of one stage and pin 4 of the next should have a common earth point – also high common earth impedances to pin 4 and pin 8 of the same device should be avoided. Figure 2a shows a circuit where common earth impedance could cause instability and Figure 2b shows one where the input and output signals have correct point earthing. If extra supply decoupling is used the capacitor should ground to the output earth point.

The input bias point (pin 6) is normally connected directly to the input (pin 5) and the signal applied through a capacitor but occasionally, when the signal is obtained from a tap on a coil, the arrangement in Figure 2b may be used to give slightly improved noise performance. C_D is a decoupling capacitor.

Figure 1a **AGC characteristics**

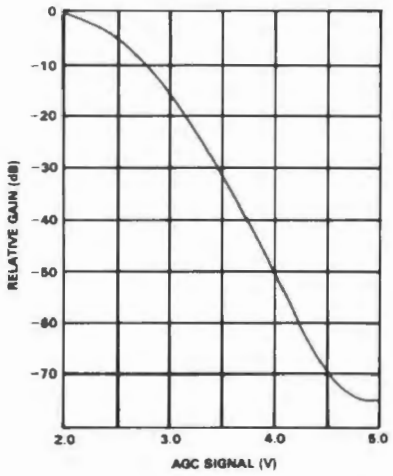


Figure 1b **Typical voltage gain ($R_S = 50\Omega$)**

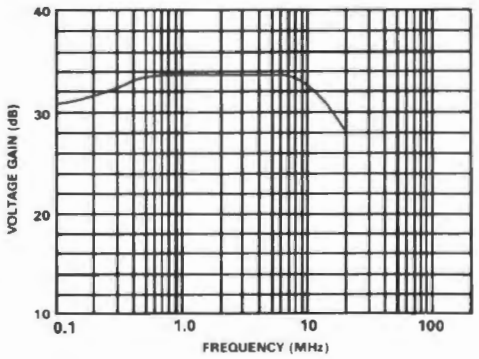


Figure 2a **Incorrect connection of earths**

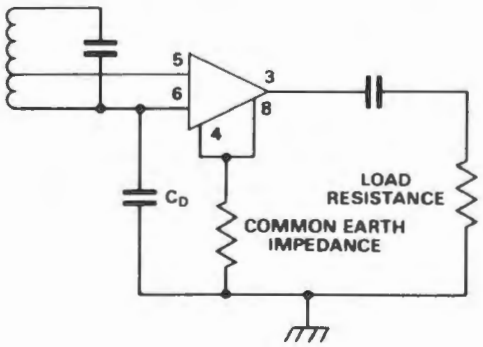
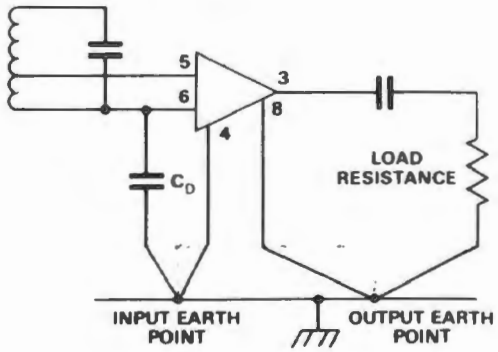


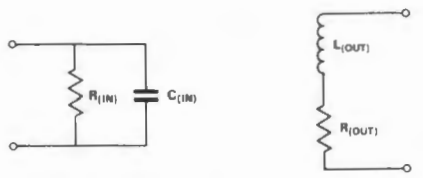
Figure 2b **Correct connection of earths**



Input and output impedances

The equivalent circuits of input and output respectively are shown in Figures 3a and 3b and the values of R_{in}, R_{out}, C_{in} and L_{out} may be determined for any particular frequency from the graphs Figures 4 and 5.

Figure 3 **Equivalent circuits**



(a) input circuit **(b) output circuit**

For the RS 1612C, R_{in} is not negative and R_{out} is negative only below 700kHz.

If a capacitor C1 in series with a resistance R2 is connected across the output oscillation will occur if, at the resonant frequency of L_{out} and C1, R_{out} has a negative resistance greater than the positive resistance R2. Where the load is capacitive, 47 ohms should be placed in series with the output.

Suitable input arrangements for the amplifiers are shown in Figure 2b and Figure 6. The method shown in Figure 6a is representative of all inputs – the input and bias points are directly-connected and the signal is coupled via a capacitor. If a crystal filter is used it should be correctly terminated, allowing for the impedance of the IC, and coupling made via a capacitor.

The output is a voltage source, with the impedance characteristics mentioned above. Output coupling is via a capacitor, with a series resistor if necessary to preserve stability (Figure 6b). If a current output to a tuned circuit is required the arrangement in Figure 6c is suitable, using almost any small signal NPN transistor with an f_T of over 300MHz and low C_{OB}. To drive particularly low impedance e.g. a 50 ohm coaxial cable, this impedance should be increased somewhat by a series output resistor (say, 100 ohms) as if the output is loaded directly by low impedance, most of the negative feedback will be removed – with consequently poor linearity and constancy of gain. Examples of the use of these amplifiers are shown in Figure 7.

Figure 4 **Input admittance with o/c output (G_{11})**

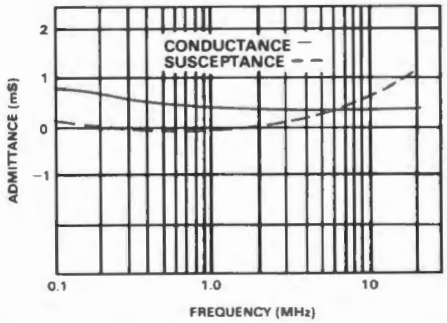


Figure 5 **Output impedance with s/c input (G_{22})**

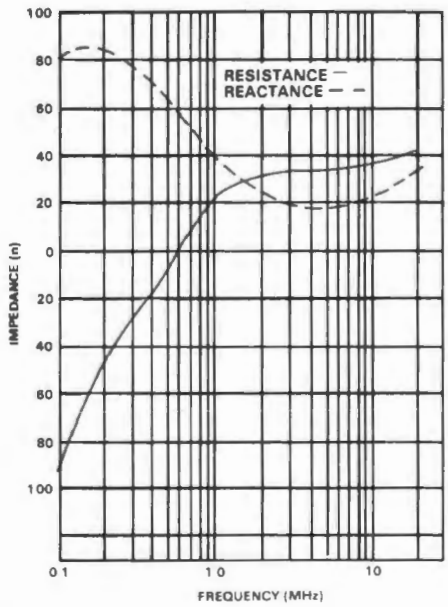
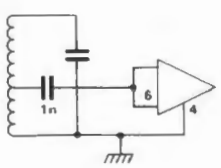
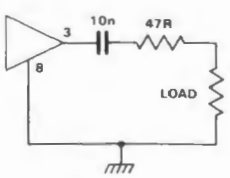


Figure 6 **Input and output circuits**

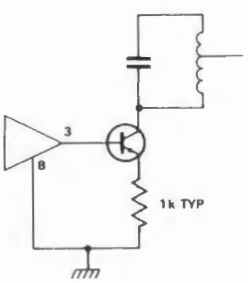
(a) Tuned circuit



(b) Normal output circuit



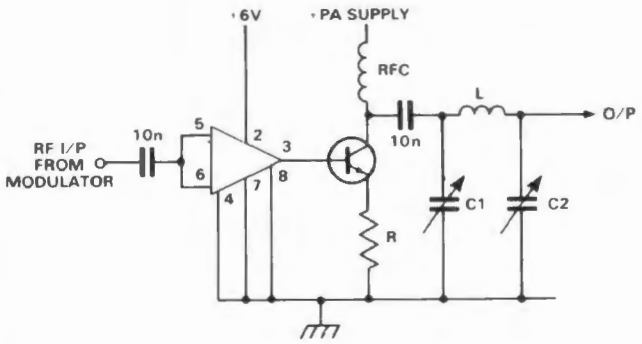
(c) Current drive into inductance



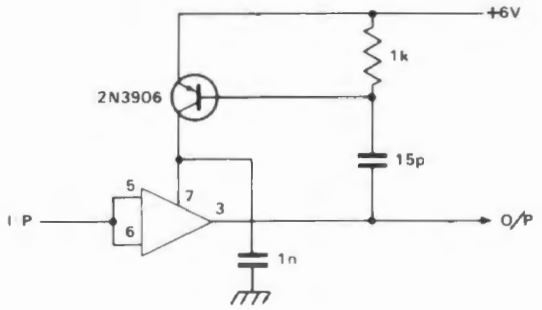
RS data

Figure 7 **Typical application**

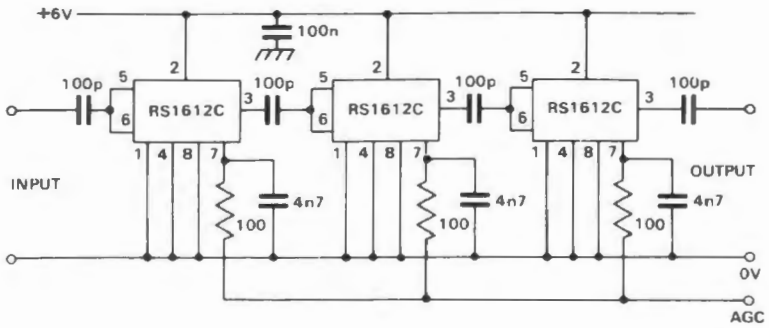
(a) Linear power amplifier for low power SSB transceivers. L, C1 and C2 form the output tank circuit. The values of PA supply and R should be chosen to suit the transistor used. C_{OB} should be as low as possible.



(b) Constant level RF amplifier stabilising at approximately 500mV rms output over a range of inputs greater than 20dB. With tuned feedback, this circuit makes an excellent constant level oscillator.



(c) I.F. section of simple S.S.B. transceiver. At 9MHz gain is approximately 100dB.



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RS data

Audio preamplifiers LM381, HA12017 and 6270

Stock numbers 306-825, 304-576, 302-132

Two high quality audio preamplifier i.c.s. suitable for magnetic cartridge amplification using RIAA equalisation, or microphone amplification using a "flat" characteristic. Also a microphone preamplifier incorporating a Voice Operated Gain Adjusting Device (V.O.G.A.D.).

LM381

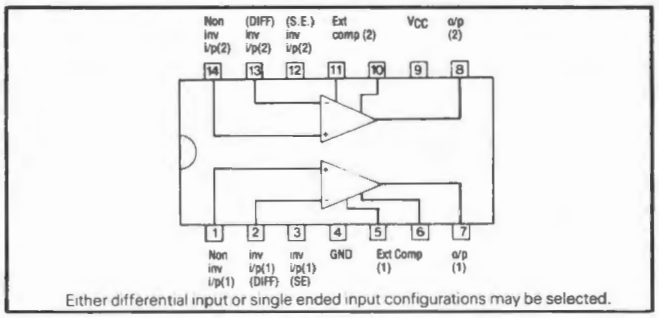
A dual preamplifier specially designed to meet the requirements of amplifying low level signals in low noise applications. Each amplifier contains an internal power supply decoupler-regulator, providing 120dB supply rejection and 60dB channel separation. Other features include high gain, large output voltage swing and a wide power bandwidth. Operation is from a single supply in the range 9 to 40V and the device is internally compensated and short-circuit protected.

Maximum ratings

Supply voltage	40V
Dissipation	715mW
Operating temperature range	0 to 70°C
Input voltage for linear swing	300mV rms

Typical electrical characteristics

Voltage gain open loop single ended	320,000 (110dB)
Voltage gain open loop single differential	160,000 (104dB)
Total supply current ($R_L = \infty$)	10mA
Input resistance	100kΩ
Open loop output resistance	150Ω
Voltage swing	$V_{CC} - 2V$
Full power bandwidth	75kHz
Channel separation	60dB
Harmonic distortion at 60dB gain	0.1% at 1kHz



Either differential input or single ended input configurations may be selected.

NOTES
A ready made pc board RS stock number 434-396 is available to accommodate the LM 381 and associated components (including the tone and volume controls) for a stereo pre-amplifier giving RIAA flat characteristics.

Applications

Figure 1 **Magnetic cartridge amplifier to the RIAA characteristic**

An amplifier to RIAA characteristics for use with dynamic cartridges with a standard load of 50kΩ. When a crystal or ceramic cartridge is used the LM380 "single ended amplifier" circuit may be connected directly. Gain $\simeq \frac{30,000}{Re\Omega}$

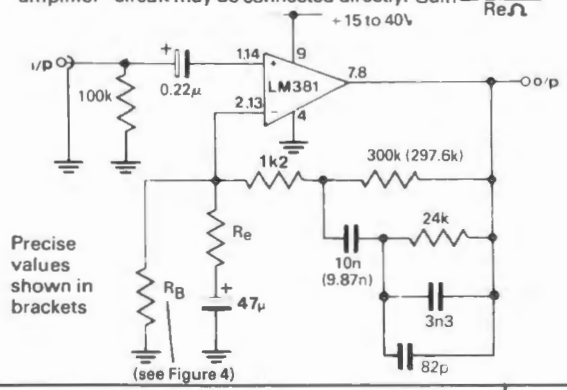
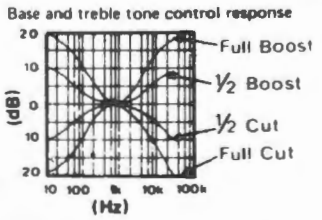
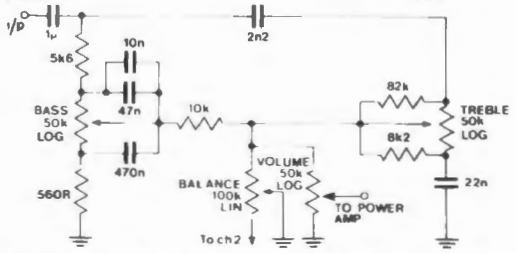


Figure 2 **Tone control stage**

Some audio applications require bass and treble tone controls. Normally two preamplifiers are required to compensate for the insertion loss of the controls. However, due to the excellent gain and large output of the LM381, only a single preamplifier is needed.





The i/p of the tone control stage can be put in series with any preamplifier circuit.

Figure 3 **Audio mixer**

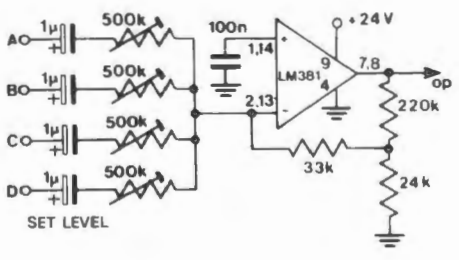
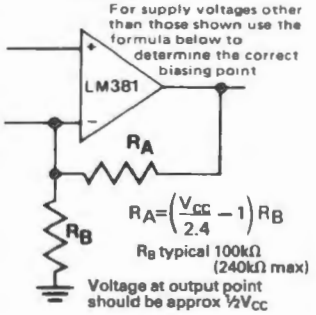


Figure 4 **Biasing**

For supply voltages other than those shown use the formula below to determine the correct biasing point

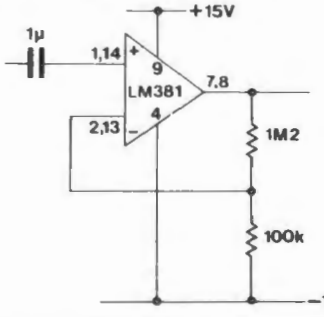


$R_A = \left(\frac{V_{CC}}{2.4} - 1\right) R_B$

R_B typical 100kΩ (240kΩ max)

Voltage at output point should be approx ½V_{CC}

Figure 5 **Biasing – split supply**



HA12017

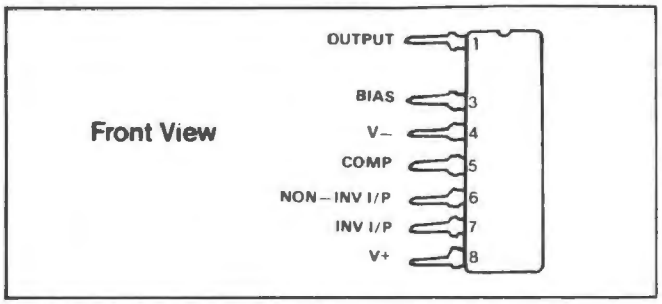
A low noise, very low distortion pre-amplifier i.c. designed for high quality magnetic cartridge amplification using RIAA equalisation.

Absolute maximum ratings

Supply voltage V_{CC} ——— ±26.5V
Power dissipation (T_A 25°C) P_T ——— 500mW
Storage temperature range T_{stg} ——— −55 to +125°C

Recommended operating conditions

Power supply voltage V_{CC} ——— ±24V
Minimum power supply voltage ——— ±6V
Operating temperature range ——— −30 to +75°C



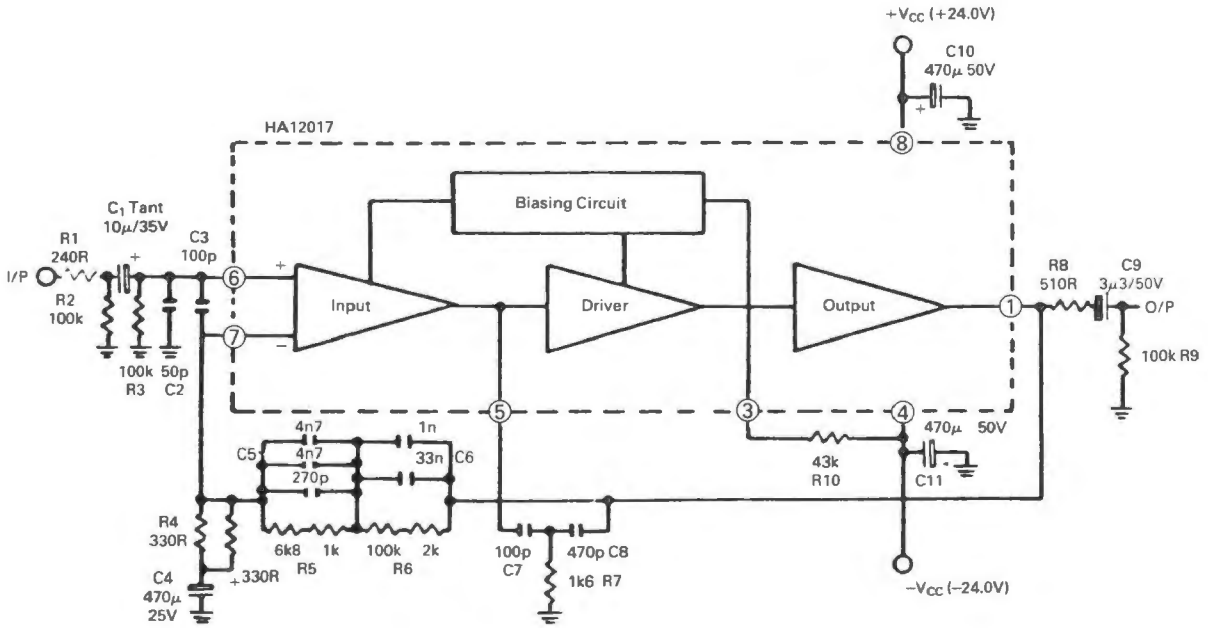
Electrical characteristics

(V_{CC} = ±24V, T_A = 25°C)

Parameter	Symbol	Test Conditions	min.	typ.	max.	unit
Quiescent Current	Iq	no input signal		4.0	6.0	mA
Open Loop Voltage Gain	$G_{V(OL)}$	f = 1kHz	95	105	—	dB
Total Harmonic Distortion	THD	f = 1kHz, V_{out} = 10V	—	0.002	0.01	%
Output Voltage	V_{out}	f = 1kHz,THD = 0.1%	13.5	14.7	—	V
Overload Margin	—	f = 1kHz, THD = 0.1% G_v = 35.9dB		235		mV
Supply Ripple Rejection	SVR+	f = 100Hz Rg = 43Ω		56		dB
	SVR−	f = 100Hz Rg = 43Ω		45		dB
Output Noise Voltage 1	V_{n1}	R_k = 43Ω, IHF-A Network	—	11.5	15.6	μV
Output Noise Voltage 2	V_{n2}	R_k = 3.3kΩ, BW −20Hz to 20kHz	—	53	90	μV

NOTES: All the parameters except $G_{V(OL)}$ are tested with RIAA curve and G_V = 35.9dB. (Av = 62)

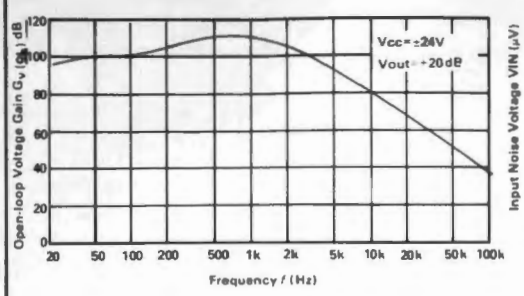
Figure 6 **RIAA pre-amplifier**



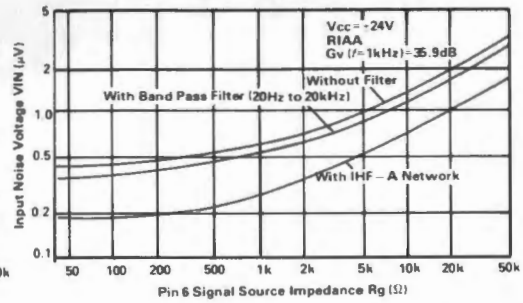
The RIAA pre-amplifier circuit is designed to accurately follow the RIAA playback curve, consequently some of the components in the feedback circuit consist of combinations of standard value capacitors and resistors in order to achieve an accurate response (e.g. 4n7 + 4n7 +270p). For less demanding applications standard preferred value components may be substituted in place of these networks. Input impedance of the amplifier circuit is approximately 50kΩ in order to match the load impedance requirements of the popular dynamic cartridges.

Figure 7

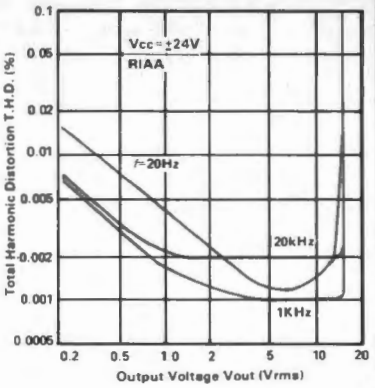
Open loop voltage gain V frequency



Input noise voltage V source impedance



THD V output voltage

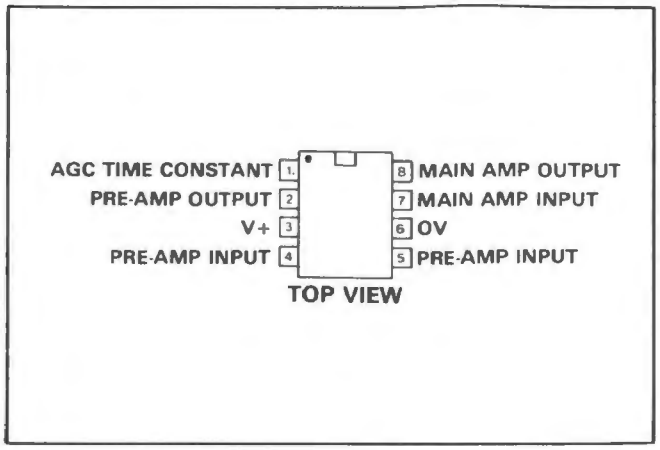


RIAA Pre-amplifier external component functions

Component	Recommended Value	Function
R1	240Ω	Protects the i.c. from abnormal input voltage. Prevents parasitic oscillation caused by signal-source impedance. Decreases high-frequency disturbance.
R2	100kΩ	Passes the electric charge of C1. Decides Rin (input resistance) Rin – R1 + (R2/R3)
R3	100kΩ	Supplies DC bias to pin-6 (input pin). Decides input resistance.
R4	165Ω	Decides voltage gain as feedback resistance.
R5	7.8kΩ	Decides RIAA characteristics, in pairs with C5 and C6.
R6	102kΩ	
R7	1.6kΩ	In a pair with C8, decides the frequency at which Gv (OL) characteristic changes from –12dB/oct to –6dB/oct.
R8	510Ω	Prevents parasitic oscillation caused by capacitive load.
R9	100kΩ	Keeps the voltage of output terminals at DC standard level. Prevents shock noise caused by function-switching.
R10	43kΩ	Decides basic bias current R10 – (+V_{CC}– (–V_{CC}) –5) kΩ
C1	10uF	Input coupling.
C2	50pF	In combination with C3, increases stability of large-amplitude operation in high frequency range.
C3	100pF	In strong field, prevents detection of TV, FM and AM signals.
C4	470uF	Supplies full DC-feedback. Decides roll off frequency (f_L) in low frequency range. F_L = 3Hz (Typical application) $F_L = \frac{1}{2\pi C4.R4}$
C5	9670pF	Decides RIAA characteristics in pairs with R5 and R6.
C6	34000pF	
C7	100pF	Supplies phase-compensation.
C8	470pF	In a pair with R7, decides the frequency at which Gv (OL) characteristic changes from –12dB/oct to –6dB/oct.
C9	3.3uF	Output-coupling.
C10	470uF	Removes ripple on V_{CC} line.
C11	470uF	

6270

An integrated circuit combining the functions of audio amplifier and Voice Operated Gain Adjusting Device (V.O.G.A.D.), designed to accept signals from a low output microphone and to provide an essentially constant output signal of 90mV for a 60dB range of input. The dynamic range, attack and decay times are controlled by external components. Typical applications include audio A.G.C. systems, transmitter overmodulation protection, tape recorders, etc.



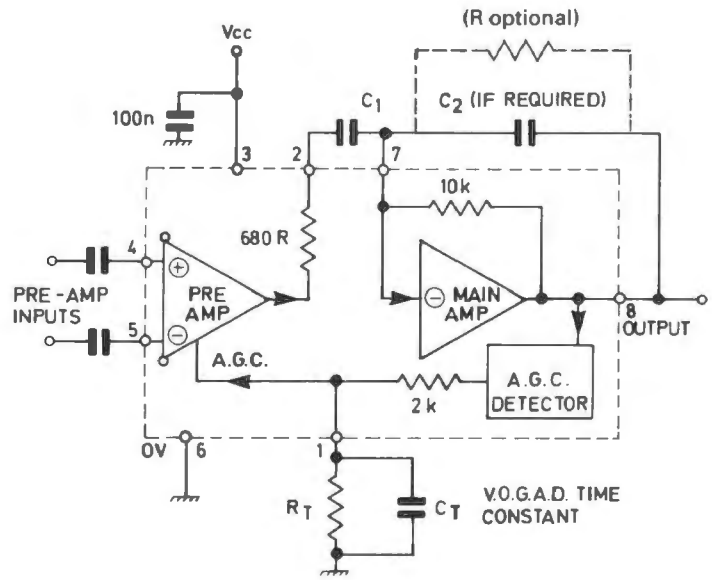
Absolute Maximum Ratings

Supply voltage V_{CC} ——— +12V
Storage temperature range T_{stg} ——— −55 to +125°C

Electrical characteristics

Parameter	Symbol	Test Conditions	min.	typ.	max.	units
Supply voltage	V_{CC}		4.5	6	10	V
Supply current	I_Q		—	5	10	mA
Input impedance	$Z_{IN(S)}$	Single ended, pin 4 or pin 5	—	150	—	Ω
Differential input impedance	$Z_{IN(D)}$	Input between pins 4 & 5	—	300	—	Ω
Voltage gain	G_V	72μV rms input pin 4	40	52	—	dB
Output level	V_{OUT}	4mV rms input pin 4	55	90	140	mV rms
Total harmonic distortion	T.H.D.	90mV input pin 4	—	2	5	%
Operating temperature range	T_{AMB}		−30		+85	°C

Figure 8



Circuit description

The principal elements of the device are shown in figure 8. The differential input preamplifier is A.G.C. controlled. The output from this stage is a.c. coupled via a capacitor to the second stage which is gain programmable by a single resistor to enable the overall sensitivity to be set. Adding a capacitor in parallel with this resistor permits the H.F. response to be tailored, if required. The output from the second stage provides the main audio output from the device, and also drives the A.G.C. detector. The detected output, which is input level dependent, is applied to the time constant circuit and the A.G.C. controlled first stage. The second stage is run in inverting mode.

Determination of gain, bandwidth, attack and decay times

The mid band gain of the second stage, which is run in parallel feedback configuration, is determined by the ratio of the 10k internal feedback resistor and the 680R resistor in series with the output of the first stage. This gain may be reduced by wiring an external feedback resistor, R_{ext}, between pins 7 and 8. The gain will then be given by the expression:

$$G = \frac{R_{ext} \times 10{,}000}{(R_{ext} + 10{,}000) \times 680} \qquad (R_{ext} \text{ in ohms})$$

The minimum permissible value for R_{ext} is 680R. The threshold point, i.e. the input level at which A.G.C. action commences, is approximately 1mV for $R_{ext} = \infty$ and approximately 8mV for $R_{ext} = 1k$.

The low frequency −3dB point is determined by the series combination of the internal 680R resistor and C_1. The high frequency −3dB point is determined by the parallel combination of the internal 10k gain-setting resistor, any external resistor R_{ext}, and C_2. Using the typical values $C_1 = 1\mu$, $C_2 = 4n7$, and $R_{ext} = \infty$, the −3dB points will occur at 234Hz and 3386Hz.

Normally the 6270 device is required to respond quickly by holding the output level almost constant as the input is increased. This "attack time", i.e. the time taken for the output to return to within 10% of the original level following a 20dB increase in the input level, will be approximately 20ms with the circuit in figure 10. It is determined by the value of C_T and can be calculated approximately by the formula:

$$\text{Attack time} \simeq 0.4\text{ms}/\mu\text{F}$$

The decay time is determined by the discharge rate of the capacitor, this being dependent on the values of R_T and C_T. For $R_T = 1M$ and $C_T = 47\mu$ the decay time is approximately 20dB/second. Other values of R_T may be used to vary the decay time for specific applications.

Figure 9(a) **Voltage gain (single ended input) – typical**

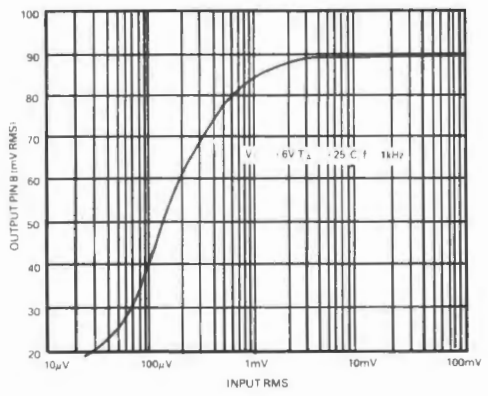
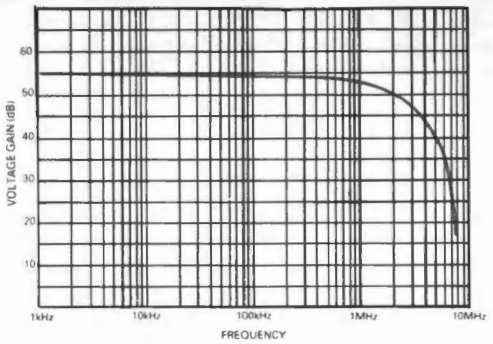


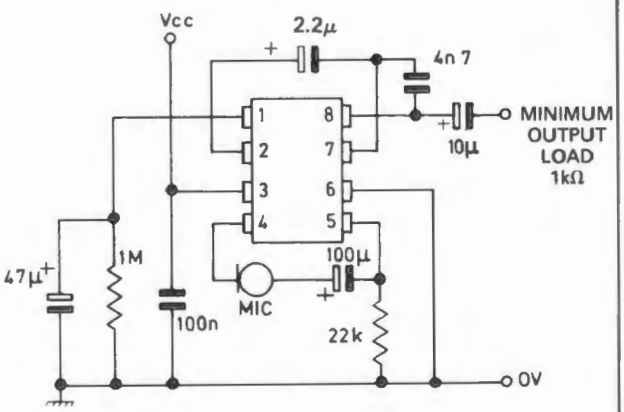
Figure 9(b) **Open loop frequency response (typical)**



Typical application

Figure 10 shows a typical application with the 6270 used as preamplifier for a 300Ω microphone. The bandwidth is approximately from 230Hz to 3,400Hz (−3dB). The input should normally be a.c. coupled, but if for any reason the coupling capacitor is omitted, the d.c. resistance between pins 4 and 5 should be less than 10 ohms. The 22k resistor

Figure 10



between pin 5 and ground is necessary to ensure that the offsets in the device at the onset of A.G.C. are of such polarity as to inhibit oscillation. If it is required to use the device with an unbalanced source, then the input may be A.C. coupled to pin 4 or pin 5, the unused input remaining floating. Any tendency to pick up noise when used in this mode may be inhibited by decoupling the unused input to ground by a 1000p capacitor. **The inputs must not be D.C. grounded.**

Bandwidth, gain, attack and decay times may be altered in accordance with the information given above to suit the differing requirements of specific applications.

RS data

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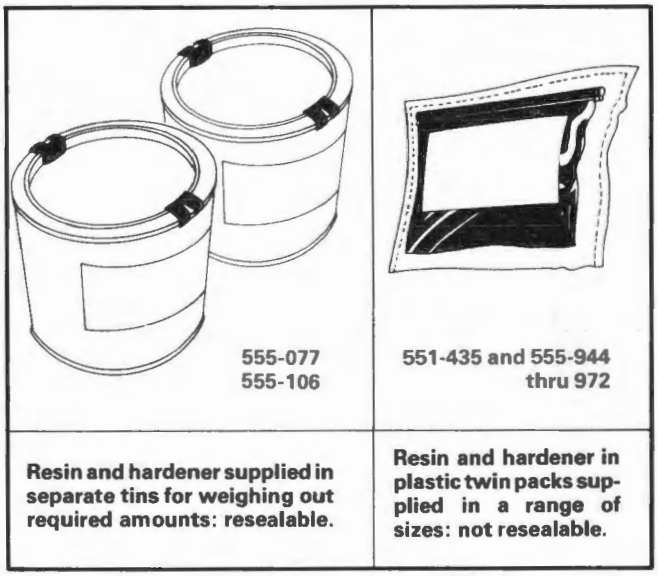
RS data

Potting Compounds

A range of potting compounds for encapsulation of electronic components and sub-assemblies, for use in laboratories or in manufacturing. Each potting compound is supplied in two parts (resin and hardener/catalyst) which require mixing and using within the specified time (pot life). The mixed compounds cure (harden) at room temperature and this process can be speeded up by curing in a low temperature oven. Good electrical and thermal characteristics are guaranteed which give long term stability of breakdown voltage, leakage currents and heat dissipation whilst providing environmental protection in industrial, humid or salt atmospheres. The physical properties of these potting compounds provide protection against mechanical and thermal shock and vibration effects, enabling components or assemblies to be handled and transported without risk of deterioration. A further feature of some compounds permit their use as an adhesive or jointing medium for bonding dissimilar materials. Recommended for use with RS potting boxes (intended for permanent potting). As a mould release when making your own moulds, use RS silicone oil or grease aerosols. For cleaning off surplus material use RS solvent 556-648 (aerosol) or 555-134 (tin).

Stock No. 555-077 General purpose epoxy, translucent yellow, supplied in two tins.
Stock No. 555-106 General purpose polyurethane, amber, supplied in two tins.
Stock No. 551-435 and 555-944 thru 972 Flame retardent epoxy, jet black, supplied in "mix-in-the-bag" twin packs.

NOTE:
Certain resins or hardeners in the RS range have a tendency to crystalise out if stored for long periods at low temperatures. The contents can easily be liquified before mixing by warming in an oven at 50°C for a short period without harming the physical properties. Avoid mixing the components until the contents have cooled down again to room temperatures or rapid curing will result.



555-077 555-106	551-435 and 555-944 thru 972
Resin and hardener supplied in separate tins for weighing out required amounts: resealable.	**Resin and hardener in plastic twin packs supplied in a range of sizes: not resealable.**

Absolute maximum ratings

(Unmixed component parts)
Continuous storage temperature ——— +5 to +30°C
Short term storage temperature ——— 0 to +50°C
Shelf life at 25°C ——— 6 months
(Shelf life will be longer for lower storage temperatures down to 5°C see warning below.)

WARNING:
Care must be exercised when mixing component parts which have been stored at temperatures below ambient : to avoid condensation and absorption of moisture which would occur with a cold mixture, the containers must be allowed to warm up to room temperature (preferably overnight) before opening/mixing. (This will also make for easier mixing since the contents will be less viscous.)

Major characteristics

Parameter	555-077	555-106	551-435 and 557-944 to 557-972	Units
colour	clear yellow	amber	jet black	
mix ratio (by weight)	1 : 1 (Note 2)	2.6 : 1	8.6 : 1	
density	1.4	1.3	1.8	g/cm³
pot life at 25°	150	40	60	mins
cure time at 25°C	8/24 (Note 1)	24	8/24 (Note 1)	hrs
cure time at 100°C	½	4	½	hrs
operating temperature range	−45 to +120	−70 to +150	−40 to +120	°C
hardness	Shore D 80	Shore A 70	Shore D 90	
compressive strength	550		800	kg/cm²
tensile strength		245	600	kg/cm²
adhesive shear strength	170			kg/cm²
flexural strength	580		500	kg/cm²
thermal conductivity	9×10^{-4}	6.4×10^{-4}	9×10^{-4}	cal cm/sec cm² °C
dielectric strength	18.5	12.5	10	kV/mm
dielectric constant	3.1	5.8	4	(at 10^4 Hz)
dissipation factor (tan δ)	0.04	0.15	0.04	(at 10^4 Hz)
thermal expansion	80×10^{-6}	170×10^{-6}	50×10^{-6}	%/°C
volume resistivity	10^{13}	5×10^{12}	10^{15}	Ωcm

1. Compound can be handled after 8 hours but full properties are developed after 24 hours.

2. Mix ratio may be varied to suit application: parameter values quoted are for a 1 : 1 mix.

General purpose epoxy 555-077

A versatile compound which offers the ability to vary the rigidity of the cured part from hard to flexible. In addition to its importance in encapsulating electronic sub-assemblies, it is useful for jointing materials of different composition and varying thermal coefficients of expansion. Simply varying the mix ratio from 1 : 1 to 3 : 1 (by adding more catalyst/hardener) gives greater flexibility with improved ability to withstand thermal and vibration stresses whilst giving increased adhesion without impairing the electrical properties.
The more flexible mixes will be found to be more suited as adhesives with higher peel strengths and also for jointing materials of widely different composition and TCE's (thermal coefficient of expansion).
Based on specification R45/H15.

Features

- Adjustable flexiblity
- Semi-clear
- Room or oven cure
- May be used as an adhesive
- Suitable on glass, metal, ceramic and plastic
- Accommodates differing TCE's
- Good vibration damper
- Withstands high g forces
- Class E insulation

Absolute maximum ratings

(Mixed compound)

Dielectric strength ——— 18.5 kV/mm
Operating temperature range ——— –45 to +120°C
Pot life at 25°C ——— 2 to 3 hours

Instructions

1. Clean thoroughly surfaces to be bonded using abrasives and/or RS solvents such as 555-134 (tin) 556-648 (aerosol) for electromechanical components or 556-654 (tin) 554-838 (aerosol) for electronic components and delicate thermoplastics.
2. Weigh out the required amount of resin. Add an equivalent weight of hardener if a 1 : 1 mixture is required or *more* hardener if a flexible formulation is required.

Formulation	Parts by weight Resin : Hardener
Rigid	100 : 100
Semi rigid	100 : 200
Flexible	100 : 300

3. Mix the two components thoroughly but carefully avoid trapping air in the mixture. Thorough mixing is essential to achieve full specified properties but in so doing if air bubbles have been trapped, then allow to stand for ½ hour before using.

4. The freshly mixed compound has a pot life of 2-3 hours at normal room temperatures; avoid leaving the mixture near a heat source until it has been used for potting or bonding.

5. Apply the mixture by pouring into a suitable mould prepared with RS aerosol silicone oil or grease as a mould release agent. For permanent potting use RS potting boxes which are made from black ABS plastic and offer a range of sizes. Application when used as an adhesive may be made by brush, roller or scraper.

6. Cure takes place in approximately 8 hours at room temperature and full properties are developed after 24 hours. A more rapid cure can be achieved with full specified properties by warming in an oven as follows:
at 70°C curing takes 45 mins.
at 100°C curing takes 15 min.

7. During mixing and handling of the resin and hardener normal precautions should be taken to avoid ingestion, inhalation, prolonged skin contact, eye splashes, etc. Wear protective gloves and goggles and use in a well ventilated area. Wash off splashes in soap and water NOT solvent.

General purpose polyurethane 555-106

A tough but flexible potting compound based on polyurethane resin. Suitable for electrical and electronic components and assemblies including cables and connectors. Must be used promptly after mixing.
Pot life at room temperature is 30-40 minutes. Mix ratio cannot be varied. Based on specification CPC 19.

Features

- Flexible
- Semi-clear
- Room or oven cure
- Suitable on a wide range of materials
- Extremely wear resistant
- Suitable for outdoor use
- Class F insulation

Absolute maximum ratings

(Mixed compound)

Dielectric strength ——— 12.5 kV mm
Operating temperature range ——— –70 to +150°C
Pot life at 25°C ——— 40 mins

Instructions

1. All parts to be encapsulated should be clean and free of grease, dirt and other chemical contaminants.
Use abrasives where possible and RS solvents for cleaning such as 556-648 (aerosol) 555-134 (tin) for electro-mechanical components or 554-838 (aerosol) 556-654 (tin) for delicate electronic components and thermoplastics.

2. Stir the resin and hardener thoroughly before mixing to achieve uniform consistency.

3. Weigh out the required amounts of resin and hardener in the exact ratio 100 to 38 (2.6 : 1). Mix the two parts together thoroughly for best results. Inadequate mixing is a primary cause of failure: use a flat not round, stirring device to minimise entrapped air.

4. If entrapped air is a problem, the mixture can be evacuated prior to use at a pressure of 1-5 mm. mercury. This will cause foaming which will rise three to four times the mixture height before subsiding. Continue evacuation until most of the bubbling has ceased.

5. Pot life is dependent upon mass and ambient temperature. A 30 minute pot life can be relied upon for a 100 gram mass at 25°C.

6. Pour into mould and allow to stand at a constant room temperature for up to 24 hours when the moulding can be handled. Full specified properties are developed after a further 24 hours. For permanent potting use RS potting boxes. (If the temperature is allowed to drop during curing, condensation may be absorbed.)

7. Accelerated cures are possible by heating in an oven, e.g.
at 70°C, curing takes 12 hours
at 100°C, curing takes 4 hours

8. Observe the normal precautions for handling urethane systems. Pouring and mixing should be carried out in a fume cupboard or well ventilated area. Wear protective gloves and goggles. Avoid ingestion, inhalation, prolonged skin contact and eye splashes. In the case of the eye contact, irrigate eyes immediately with copious amounts of water and obtain immediate medical attention. Wash other areas of the body exposed to the urethane mixture thoroughly in hot soapy water.

9. Replace lids firmly on tins immediately after use to prevent moisture absorption: the resin is hygroscopic.

Flame retardant black epoxy

Two part potting compound for encapsulating p.c.b.'s and components and large scale moulding.

50g pack size, stock no. **557-944**
100g pack size, stock no. **557-950**
250g pack size, stock no. **557-966**
500g pack size, stock no. **557-972**
1000g pack size, stock no. **551-435**

A room curing epoxy with excellent electrical and physical properties with several advantages over conventional epoxies. The high gloss finish in the cured compound is pleasing in appearance. It has a dense black pigmentation which fully conceals the encapsulated parts and renders tampering and repairing impossible. Although the surface finish is 'hard' in the normal sense of the word, a slight flexibility in the compound permits the encapsulation of delicate electronic components and allows for thermal expansion. As well as providing class E insulation, it is flame retardent. The "mix-in-the-bag" system of packaging permits mixing and pouring without mess and is an ideal method of achieving a thorough mix without trapping in air. The choice of pack sizes makes this ideal for both development work and volume production. The component parts are not hygroscopic so that mixing and pouring can be conducted under cold and damp conditions.

Features

- High gloss, jet black finish
- Room or oven cure
- Meets BS415 and UL492
- Low exothermic heat rise
- Class E insulation
- UL94-VO approved
- Pre-evacuated twin packs
- Easy mixing and pouring
- Choice of pack sizes
- High consistency between packs
- Pre-determined mix ratio
- Low toxicity products of decomposition

Absolute maximum ratings

(Mixed compound)

Dielectric strength	10 kV mm
Operating temperature range	–40 to +120°C
Pot life at 25°C	60 mins

Instructions

1. Clean components to be encapsulated by washing in RS solvents 556-648 (aerosol) 555-134 (tin) or for more delicate components and thermoplastics wash in 554-838 (aerosol) 556-654 (tin).

2. Cut and remove outer wrapper with care: do not damage inner pack. (Figure 1).

3. Remove the dividing clip which separates the two parts (resin and hardener) by pulling the two parts away from each other, thereby forming one complete bag. (Figure 2).

4. Hand mix the two parts whilst still in the bag. Force the contents from one end of the bag to the other to make a thorough mix of the resin and hardener. (Figure 3). Exert pressure during mixing with thumbs and finger tips using both hands, but do not squeeze excessively into the palm of the hand to avoid undue pressure on the bag.

5. Using thumb and finger, squeeze contents away from the corners to ensure thorough mixing of all material.

6. Full mixing can be achieved within one minute by using the correct technique, but until experience is gained, or when using larger packs, continue mixing for three minutes to safeguard against incomplete mixing.*

7. Carefully cut off the pointed end of the bag which will act as a dispensing nozzle. The size of your cut will determine the rate of flow. (Figure 4).

8. Lay the bag across the palm of one hand whilst squeezing the resin out with the other hand, starting at the back. (Figure 5). To stop the flow, remove hand pressure and invert the bag.

9. Use within 60 minutes of mixing, keeping bag contents away from heat source. Cure time: 24 hours at room temperature to attain full electrical and physical properties. Can be handled after 5 to 8 hours depending on ambient temperature.

10. Curing may be accelerated by raising ambient temperature. (typical cure time at 100 °C = 30 mins or 90 mins at 70°C.)

*Note: Incomplete mixing will be characterised by a tacky surface in the cured component.

Figure 1

Figure 2

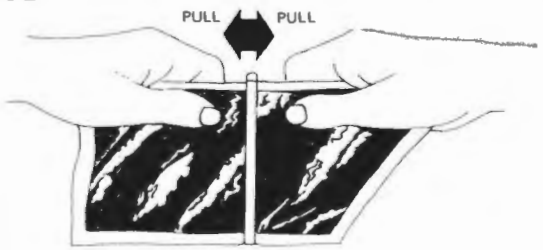


Figure 3

Figure 4

Figure 5

RS data

APPLICATIONS

Epoxies in general

Rigid epoxies such as the RS 555-077 (1:1mix) and the RS Black Epoxy are particularly suited to give the best performance under high conditions of electrical stress with high humidity and temperature. Many varied applications have been found, limited only by the users imagination, in electro-mechanical and electronics assemblies, components and inter-connections. Also many non-electrical applications as a bonding medium have been found. Hard epoxies are very resistant to mould growth, also chemicals including solvents, oils and sea water. UV or sunglare can cause surface 'chalking'. Some known and proven applications are given below:

Printed circuit boards and modules
Piezoelectric spark ignition system
Memory modules
Transistorised transformer unit
Thermal switches in aircraft
Capacitor encapsulation/filling
Electrical connectors in washing machinery
Mounting precision mirrors
Encapsulating reed switches
Transformers
Small components for ease of handling
Chokes
Small ferrites (unsuitable for large-ferrites)
Small electrical joints
Dusty environments (low tracking risk)
Voltage multipliers
Brake control circuits
Mould making
Proximity switch
Thick film circuits
High voltage circuits
Automotive circuits
Aerial loops
Photocopier circuits (H.V.)
R.F. interference suppression
Rotating machinery
Rotor arm circuits

RS Epoxy 555-077

By varying the mix ratio of this potting compound its various attributes can be used in a wider range of applications. Advantage can be taken of the more flexible compound (by mixing in the ratios given on page 2) to provide greater ability to absorb mechanical and thermal shocks in combination with dissimilar materials. Known and proven applications are given below. Note that flexible epoxies lose some of their chemical resistance properties.

Vibration damping
High g applications
Items experiencing rapid temperature change
Bonding materials with dissimilar thermal coefficient of expansion
Jointing glass, metal, ceramic or plastics together
May be applied as an adhesive
Sealing neoprene heater cables
Sealing neoprene gaskets to phenolic housing
Sealing polycarbonate to brass
Sealing the lens of an infrared camera
Hammer head to GRP handle
Glass bulbs to shells
Phenolic switch housing to zinc coated steel
Aluminium to iron
Steel to brake lining
Magnets to copper

RS Black epoxy, 551-435 and 557-944 thru 972

The features of this particular epoxy opens up the following additional areas of application to those given under 'Epoxies in general'.

Attractive jet black gloss finish (selling feature).
Fully obscures contents (commercial security).
Prevents tampering.
Flame retardent — safe in hazard areas under fault conditions (mines, tunnels, chemical processing).
Pre-measured packs suitable for field use.
Products of decomposition are of low toxicity — safe fumes if exposed to fire.
Very low exothermic heat rise — will not over-heat during curing of thick cross-sections — suitable for very large encapsulation.
Reproducible finish and characteristics due to accurate mix ratio and ability to mix thoroughly.
Easy to use in volume production even with changes of operators.

RS Polyurethane potting compound 555-106

This product combines toughness with flexibility and excellent abrasion resistance and shock protection. Compared to epoxies, polyurethanes in general offer inferior chemical resistance, humidity performance (long term), thermal conductivity, dissipation factors and thermal expansion. Care must also be adopted in use against toxic fumes, a shorter pot life and condensation. Avoid high temperature with high humidity.
Unaffected by UV or sunlight.
Many of the applications listed for the flexible version of RS epoxy 555-077 are suitable. Additional known and proven applications are as follows:

Modules and p.c.b.'s with ferrites, glass or ceramic discs, etc.
Large ferrites.
Large transformers.
Anti-shock encapsulation.
Rollers.
Noise damping.
Impact pads.
Anti-vibration pads.
Sealing strips.
Hybrid ceramic circuit encapsulation.
Cable jointing.
Flexible connectors.
Repairable — servicing feature.

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RS data

3½ Digit BCD potentiometer i.c.

Stock number 303-040

The RS 7525 is a monolithic CMOS 3½ digit BCD digitally controlled potentiometer design for precision incremental voltage-divider applications, with control from 0 to 1.999 V_{IN} increments.

Absolute maximum ratings

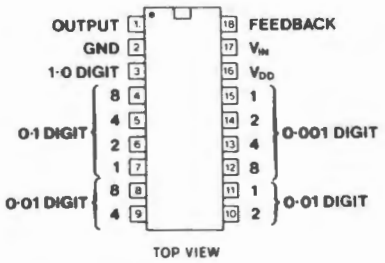
V_{DD} to GND	−0.3 V to +17 V
V_{IN} and feedback to GND	±25 V
Digital input to GND	−0.3 V to V_{DD}
Output pin to GND	−0.3 V to V_{DD}
Power dissipation	670 mW
Operating temperature	0 to +70°C
Storage temperature	−65 to +150°C

Notes

1 Sample tested over temperature
2 Nonlinearity measured against best straight line. Monotonicity is guaranteed over temperature range.
3 Measured using internal feedback resistor FS is BCD=1.999
4 AC parameter, sample tested
5 Thin film resistor temperature coefficient≈ −300ppm/°C

Features

- 3½ BCD digits resolution (1999 bits)
- ±½ LSB nonlinearity
- ±0.05% full scale gain error
- Excellent repeatability



CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Electrical characteristics T_A=25°C, V_{DD}=15V, V_{IN}=+10V, OUTPUT=0V

Parameter	Conditions	Min.	Typ.	Max.	Units
Resolution	Note 1			1 in 2000	
Non linearity error	BCD 0.000 to 1.999 Note 2			±½	LSB
Gain error	BCD=1.999 Note 3		±0.05		%
Gain temperature coefficient	BCD=1.999			±25	ppm/°C
Output leakage current	BCD=0.000			100	nA
Switching time 10% to 90%	V_{IN}=+5V, R_{OUT}=100Ω, Digital inputs V_{IL} or V_{IH} Note 4			1	µs
Feed through error	V_{IN}=±10V 20kHz Sinewave			±0.05	%V_{IN}
Analogue input resistance	Note 5	2		10	kΩ
V_{IN} range				±10	V
Output capacitance	BCD=0000 BCD=1999			60 200	pF pF
Feedback resistance to output	Note 5	8		40	kΩ
Digital input HIGH voltage Digital input LOW voltage Digital input leakage current Digital input capacitance		+14.5		 +0.5 ±1 5	V V µA pF
V_{DD} V_{DD} range (functional, but performance unspecified)		14.25 +5	15	15.75 +17	V V
I_{DD}				500	µA

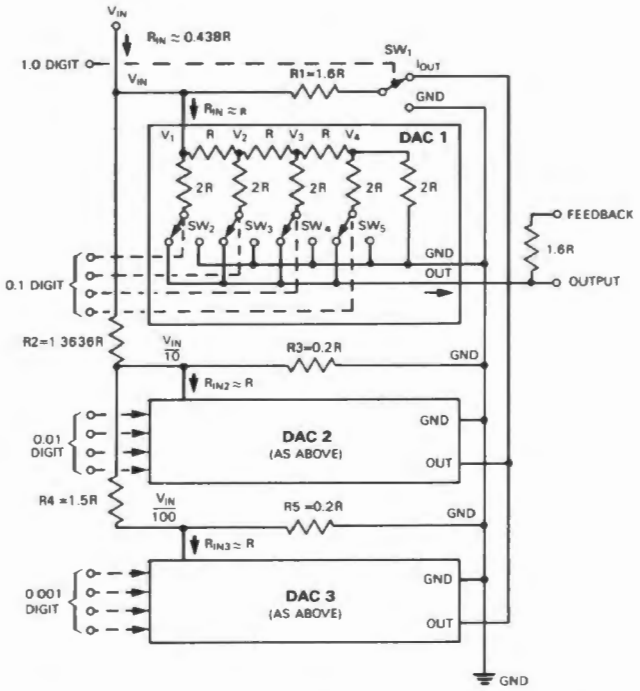
Converter characteristics

Switching time
In a D to A converter the switching time is the time taken for an analogue switch to change to a new state from the previous one. It includes delay time and rise time from 10% to 90%, but does not include settling time as this is a function of the output amplifier used.

Output capacitance
This is the capacitance between the output terminal and ground.

Feedthrough error
This is the error caused by capacitive coupling from the V_{IN} terminal to the output terminal.

Figure 1: **Internal circuit diagram**



Operation

The RS7525 consists of a 3½ digit BCD digital to analogue converter comprising of a thin-film R/2R resistor ladder, interquad voltage dividers and 13 N-channel MOS SPDT current steering switches. Figure 1 shows the converter circuit and it can be seen that the 1.0 digit consists of a 1-bit multiplying DAC (SW 1 & R_1) while the 0.1, 0.01 and 0.001 digits are 4-bit multiplying digital to analogue converters (DAC 1, DAC 2 and DAC 3). These converters are connected by two 10:1 dividers R_{IN2}, R_2, R_3 and R_{IN3}, R_4, R_5. DAC 1 shows the R/2R ladder and switch network as also used in DAC 2 and DAC 3. With an input voltage $V_{IN}/2R$, $V_{IN}/4R$, $V_{IN}/8R$ and $V_{IN}/16R$.

A logic ONE applied to a digital input steers that arm's current to the output, while a logic ZERO steers the current to GND.

Table 1: **Analogue output for different digital inputs**

BCD INPUT					ANALOGUE OUTPUT	
Digital input				Equivalent Decimal Input	V_O/V_{IN}	V_O
1.0	0.1	0.01	0.001			
1	1001	1001	1001	1.999	−1.999	$-1.999V_{IN}$
1	0000	0000	0001	1.001	−1.001	$-1.001V_{IN}$
1	0000	0000	0000	1.000	−1.000	$-1.000V_{IN}$
0	1001	1001	1001	0.999	−0.999	$-0.999V_{IN}$
0	0101	0000	0000	0.500	−0.500	$-0.500V_{IN}$
0	0000	0000	0000	0.000	0	0

Note
For proper BCD coding the 0.1, 0.01 and 0.001 digit inputs must not exceed BCD 9 (1001).

Equivalent circuit

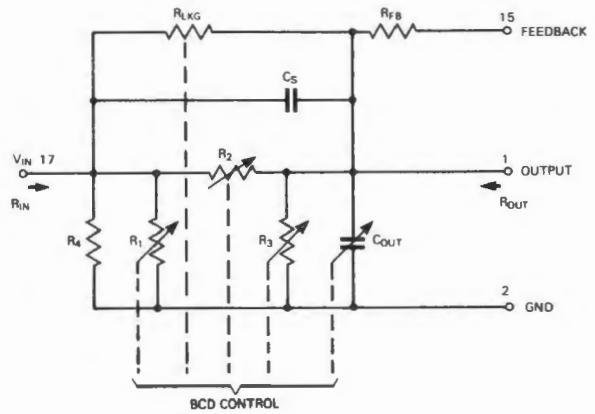
The equivalent circuit can be seen in figure 2 and is basically a digitally controlled π attenuator network with a signal input V_{IN}, signal output and a signal ground. The attenuation is varied under control of the BCD digital input.

With the output terminated at an operational amplifier virtual ground and the feedback pin connected to the operational amplifier output, the nominal transfer equation is:

$V_{OUT} = -V_{IN}$ B.C.D., where $0.000 \leq BCD \leq 1.999$

Table 1 shows the analogue output for various BCD inputs.

Figure 2: **Equivalent circuit**



Applications

AC or DC input voltages up to ±10V may be applied to the device for attenuation. This provides high flexibility in fields such as instrumentation and audio gain control. The digital control with excellent repeatability and 0.2% accuracy makes this device an ideal replacement for multi-turn potentiometers.

Output amplifier offset

The output resistance at the output pin is code dependant varying between ∞ and 0.35 R_{LDR}. For a fixed feedback resistor of value $1.6R_{LDR}$ the output error for a fixed amplifier offset V_{OS} is (see figure 3):

$$V_{ERROR} = (1 + \frac{R_{FB}}{R_{out}})\ V_{OS}$$

With $R_{OUT} = \infty$

$$V_{ERROR} = (1 + \frac{R_{FB}}{\infty})\ V_{OS}$$

$$= V_{OS}$$

or with $R_{OUT} = 0.35\ R_{LDR}$

$$V_{ERROR} = (1 + \frac{1.6R_{LDR}}{0.35R_{LDR}})\ V_{OS}$$

$$= (1 + 4.6)\ V_{OS} = 5.6\ V_{OS}$$

Both these cases show that amplifier offset in conjunction with a changing output resistance at the output pin create nonlinearity error in addition to a simple offset term.

For optimum operation the output amplifier initial offset should be adjusted to less than 100μV (as measured between the amplifier input terminals). The offset voltage over the operating temperature range should not exceed 250μV.

With high frequency amplifiers R_{FB} and C_{OUT} create a phase lag, which may cause ringing or oscillation. When using a high speed amplifier a feedback shunt capacitor C_1 of approximately 5 to 20 pF will ensure stability.

If an output voltage range of ±19.99 volts is required (i.e. ±10.0 Volts input), a high voltage output amplifier with appropriate supply voltages must be used.

To keep circuit linearity the output operational amplifier offset voltage should not exceed 2% of the circuit resolution. (Circuit resolution= $\frac{V_{IN}}{1000}$).

RS data

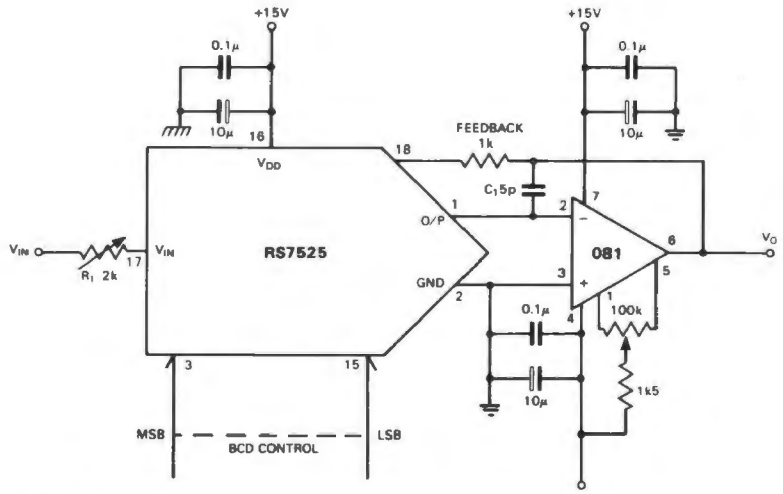
Calibration procedure

Offset adjustment
Apply BCD 0.000 to the 7525 digital inputs. Use a high resolution high impedence voltmeter between 7525 output and GND. Adjust the amplifier's input offset voltage to achieve an input differential of less than 100μV.

Gain adjustment
Apply BCD code 1.000 to the 7525 digital input. With +10V applied to the V_{IN} terminal. Using a high resolution voltmeter between the output amplifier output and the ground pin of the 7525 adjust the 2KΩinput resistor R_1 until the voltmeter reads the output voltage as −V.

The digital BCD code input may be a direct digital signal or alternatively it can be derived from switches, DIL switches or jumper links, etc, where a more permanent setting is required. Note the BCD control inputs are CMOS and will require usual pull-up resistors when single pole input selection is used, the DIL 13–commoned resistor networks are ideal for this application.

Figure 3: **Typical application circuit**



NOTE:
Supply decoupling capacitors should be as close to the device supply pins as possible. The output pin 1 should not be allowed to exceed −300mV as catastrophic substrate currents will flow under such conditions.

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RS data

6 word 12-bit D to A converter i.c.

Stock number 303–034

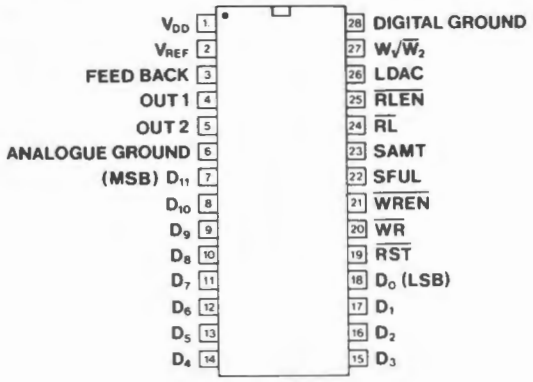
The RS 7544 is a 12-bit monolithic multiplying digital to analogue converter which incorporates a 6-word deep, 12-bit wide, First-In, First Out (FIFO) stack register which acts as a buffer store for the digital information. Two status flags, stack full (SFUL) and stack almost empty (SAMT) are included. Write ($\overline{WR}$), write enable ($\overline{WREN}$), Roll ($\overline{RL}$) and Roll enable ($\overline{RLEN}$) control inputs are also featured. The 12-bit digital to analogue converter has a load control and select input allowing the contents of either of the bottom two stack registers to be converted. A system reset $\overline{RST}$ loads the digital to analogue converter with all 0's and resets the FIFO stack.

Features

- 12-bit resolution
- Monotonic to 12-bits over temperature range
- 6-word deep, 12-bit wide first-in, first-out (FIFO) buffer memory
- FIFO status flags for Input/Output handshaking
- Directly interfaces with microprocessors
- Low gain drift
- ±1 LSB max. gain error
- Single +5V supply

Absolute maximum ratings

V_{DD} to analogue or digital ground ..... 0V to +7V
Analogue ground to digital ground differential ..... V_{DD}
Digital input and output voltages to digital ground pins 7 to 27 ..... –0.3 to +15V
V_{REF} and feedback to analogue ground ..... ±25V
Operating temperature range ..... 0°C to +70°C
Storage temperature range ..... –65°C to +150°C
Lead temperature 10s soldering ..... +300°C
Power dissipation (derate by 12mW/°C above +50°C) 1200mW



Top View

Caution:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conjunctive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Electrical characteristics

T_A = 25°C, V_{DD} = +5V, V_{REF} = +10V, OUT 1 = OUT 2 = 0V

Parameter	Conditions	Min.	Typ.	Max.	Units
Resolution				12	Bits
Relative accuracy				±½	LSB
Differential nonlinearity	Monotonic to 12-bits over temp. range			±1	LSB
Gain error				±12.3	LSB
Gain temp. coefficient			2	5	ppm/°C
Power supply rejection (Δ gain for Δ V_{DD})	V_{DD} = 4.75 to 5.25V			0.002	% per %
Leakage Current OUT 1	DAC register loaded all 0'S			1	nA
OUT 2	DAC register loaded all 1'S			1	nA
Pin 2 input resistance		7	12	20	KΩ
Input resistance temp. coefficient			−300		ppm/°C
O/P capacitance Pin 4	DAC register loaded to all 0's			75	pF
Pin 5				260	pF
Pin 4	DAC register loaded to all 1's			260	pF
Pin 5				75	pF

characteristics (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
High level input voltage		3			V
Low level input voltage				0.8	V
Input current			0.001	1	μA
Input capacitance				8	pF
High level output voltage	I source = −40μA	4			V
Low level output voltage	I sink = 1.6 mA			0.6	V
Supply voltage V_{DD}			5		V
Supply current I_{DD}	Digital inputs = V_{IH} or V_{IL}			2	mA
	Digital inputs = 0V or V_{DD}			100	μA

Dynamic characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
Propagation delay		Full-scale change to 90% 100Ω 13pF load			185	ns
Stack propagation delay		Full-scale change to 90% 100Ω 13pF load			1.26	μs
Output glitch energy		Design guidance only		700		nVsec
Multiplying feed through error		V_{REF} = ±10V 10KHz Sine Wave			2.5	mVp-p
t_{WR}	Write pulse width		75			ns
t_{WRS}	Write enable setup		0			ns
t_{WRH}	Write enable hold time		0			ns
t_{WDS}	Write to data setup time				220	ns
t_{WDH}	Write to data hold time		270			ns
t_{WMT}	Stack almost empty flag LOW response				400	ns
t_{WFL}	Stack full flag HIGH response				320	ns
t_{RL}	Roll pulse width		75			ns
t_{RLS}	Roll enable setup time		0			ns
t_{RLH}	Roll enable hold time		0			ns
t_{RFL}	Stack full flag LOW response				1.1	μs
t_{RMT}	Stack almost empty flag HIGH response				380	ns
t_{LDAC}	Load DAC pulse width		120			ns
t_{WSS}	Word select setup time		135			ns
t_{WSH}	Word select hold time		0			ns
t_{RST}	Reset pulse width		75			ns

Table 1: **Pin functions**

Pin No.	Name	Function	Pin No.	Name	Function
1	V_{DD}	+5V Supply	20	$\overline{WR}$	Write, with $\overline{WREN}$ low, the trailing edge of $\overline{WR}$ loads data into the lowest available empty register of the stack.
2	V_{REF}	±20V Reference Voltage			
3	Feedback	DAC Feedback Resistor			
4	OUT1	Output from R-2R Ladder	21	$\overline{WREN}$	Write Enable.
5	OUT2	Output from R-2R Ladder	22	SFUL	Stack Full Flag. When HIGH, indicates stack is full. When LOW, indicates less than six words remain in the stack.
6	Analogue ground	—			
7	D11	Data Input (MSB)	23	SAMT	Stack Almost Empty Flag. When HIGH, indicates one word or less remains in the stack. When LOW, indicates more than one word contained in the stack.
8	D10	Data Input			
9	D9	Data Input			
10	D8	Data Input	24	$\overline{RL}$	Roll, with $\overline{RLEN}$ low the trailing edge of $\overline{RL}$ rolls information down the FIFO stack past the register data-selector.
11	D7	Data Input			
12	D6	Data Input			
13	D5	Data Input	25	$\overline{RLEN}$	Roll Enable.
14	D4	Data Input	26	LDAC	Load DAC. Loads information from one of two stack registers (1 or 2) into the DAC register
15	D3	Data Input	27	$W_1/\overline{W_2}$	WORD1/$\overline{WORD2}$. A HIGH enables WORD 1 through the data-selector, a LOW enables WORD 2.
16	D2	Data Input			
17	D1	Data Input			
18	D0	Data Input (LSB)	28	Digital ground	—
19	$\overline{RST}$	Reset, when low resets DAC Register and stack control flip-flops to zero.			

Terminology

Relative accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed as a percentage of fullscale range.

Differential nonlinearity
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max. over the operating temperature range ensures monotonicity.

Gain error
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the 7544, ideal full-scale output is V_{REF} −1 LSB. Gain error is adjustable to zero.

Glitch energy
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA secs or nV secs depending upon whether the glitch is measured with the reference input of the DAC connected to ground.

Propagation delay
This is a measure of the internal delays of the circuit and is defined as the time from LDAC going high to the analog output current reaching 90% of its final value for a full-scale change.

FSR
This is an abbreviation for Full Scale Range. For a 12-bit converter with a reference input of 10V the FSR is 10 × (4095/4096) Volts.

Output leakage current
Current which appears at OUT1 with DAC Register loaded to all 0s or at OUT2 with DAC Register loaded to all 1s.

Multiplying feedthrough error
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

Circuit operation

The 7544 stack consists of six 12-bit data registers as shown in figure 1. Internally a stack register is considered to be empty if the output from its control flip-flop (FF1-FF6) is LOW. After a reset signal $\overline{RST}$, all control flip-flops are reset LOW and the DAC register is loaded with all 0's. Twelve-bit data is written into the stack under control of $\overline{WR}$ and $\overline{WREN}$. Initially this data is latched into register 6, the top register of the stack, and the output of the FF6 control flip-flop momentarily goes HIGH. (As at this instant the output of FF5 is LOW) FF6 subsequently returns LOW. FF6 returning LOW sets the output of FF5 momentarily HIGH and in doing so

Figure 1: **Timing diagram for write operations**

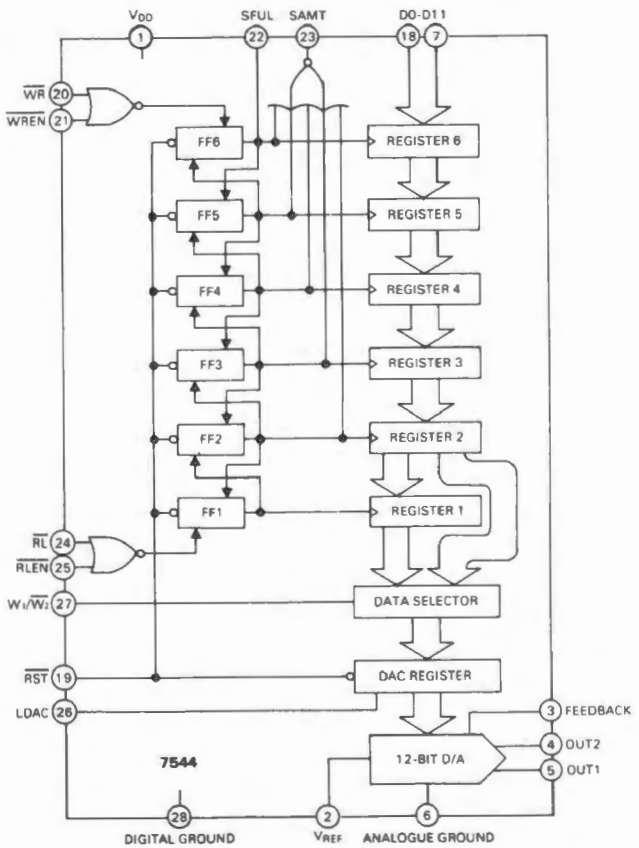
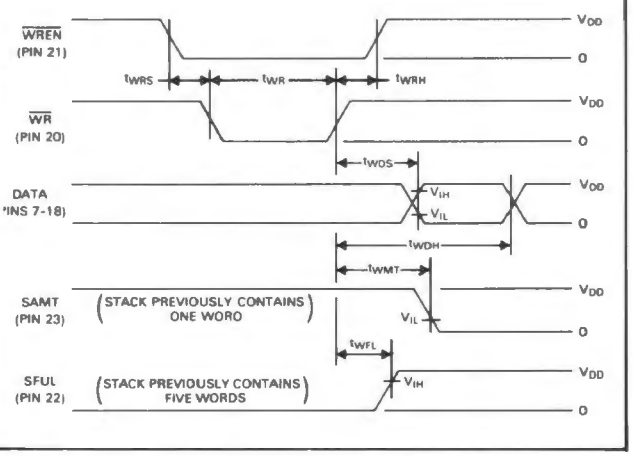


Figure 2: **Block diagram**



loads data from register 6 into register 5. The process is repeated down the stack until the input data reaches register 1 with FF1 going High and remaining High. Note that the SAMT flag, which was set HIGH after the reset $\overline{RST}$ is still unchanged. Register 1 is now no longer affected by subsequent write operations. Although all the other stack registers have the data as in register 1 in them, their control flip-flops are LOW so this data can be overwritten. The next write operation initiates a similar sequence of events but this time the data will fall through to register 2. The SAMT flag now goes LOW. After four further write cycles the SFUL flag is set HIGH indicating the stack is full. See figure 1 and table 2.

A stack roll operation may be initiated using the $\overline{RLEN}$ and $\overline{RL}$ inputs. This causes the output of the FF1 to reset LOW, register 1 then appears empty and a roll-down sequence similar to that described above is automatically initiated. The data originally in register 1 is lost and the SFUL flag is reset LOW if the stack was initially full. See table 3 and figure 1. Any arbitrary sequence of stack write and roll operations are permissible.

Data can be selected from register 1 or register 2 using the $W_1/\overline{W}_2$ control input. This data is loaded into the 12-bit DAC register using the LDAC signal. See table 4 and figure 4. An LDAC operation does not alter word positions in the stack hence SFUL and SAMT will remain unchanged. Note LDAC is a level triggered control signal.

Write data timing

The ripple-through nature of the stack leads to an apparent time skew (or delay) between the write signals and valid input data. This delay means that input data need not be valid on the trailing edge of $\overline{WR}$ which is the normal constraint, but must be valid some time latter, t_{WDS}, as can be seen in figure 1. Input data must remain valid for some time after t_{WDS} max. to allow the input data latches to settle with the correct data. The minimum data hold time is t_{WDH} min. and is specified from the falling edge of $\overline{WR}$. This time incorporates the delay time caused by skewing.

Stack almost empty (SAMT) flag timing

Referring to the functional diagram figure 1 it can be seen that the SAMT flag is derived from a five-input NOR gate monitoring the control flip-flops FF2 to FF6 outputs. After a RST signal all the control flip-flop outputs are reset LOW and the SAMT flag is set HIGH. When the first 12-bit word is written to the top of the stack, register 6 control flip-flop (FF6) momentarily goes HIGH as explained previously. The SAMT flag will go LOW and remain LOW while the word passes down the stack. When the input data is finally latched in the register 1 position, flip-flops FF2 to FF6 are again LOW and the SAMT flag will return HIGH. When the second word is written to the top of the stack, SAMT goes LOW and remains LOW since this word will fall-through the stack to register 2 with FF2 going HIGH and remaining HIGH. As the SAMT flag behaviour is dependant on the input data write frequency if the time between write cycles is less than the stack propogation delay (typically 2μs) then the SAMT flag will go LOW after the first write signal and remain LOW since the next word will start falling through the stack before the first word has reached register 1. If the SAMT flag is used as an interrupt for the system microprocessor (positive edge triggered), the interrupt input should be masked during data writing to avoid an erroneous interupt. During roll operations there is no possibility of glitches on the flag output.

Stack full (SFULL) flag

This stack status flag is set HIGH when the stack is full. When LOW it indicates less than six words are in the stack and subsequent write operations may occur.

Figure 3: **Timing diagram for stack roll operations**

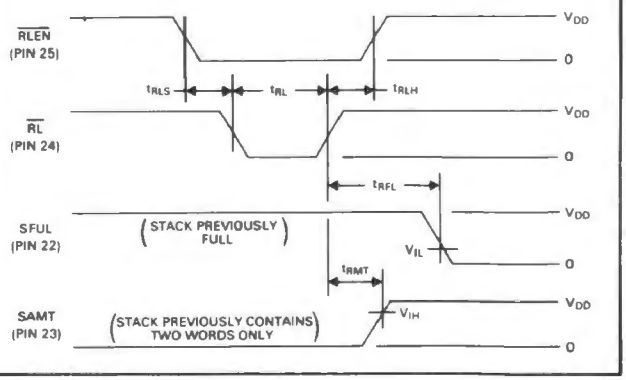


Table 2: **Truth table for stack write operations**

	FIFO stack control inputs					Data input	Resulting stack register contents						Output flags	
Operation	$\overline{\text{RLEN}}$	$\overline{\text{RL}}$	$\overline{\text{WREN}}$	$\overline{\text{WR}}$	$\overline{\text{RST}}$	**D0-D11**	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**SFUL**	**SAMT**
Clear DAC Latch, Reset Stack F/Fs	X	X	X	X	0	X	(X)	(X)	(X)	(X)	(X)	(X)	0	1
Write Word A into Stack	1	X	0	↑	1	A	(A)	(A)	(A)	(A)	(A)	A	0	1
Write Word B into Stack	1	X	0	↑	1	B	(B)	(B)	(B)	(B)	B	A	0	↓
Write Word C into Stack	1	X	0	↑	1	C	(C)	(C)	(C)	C	B	A	0	0
Write Word D into Stack	1	X	0	↑	1	D	(D)	(D)	D	C	B	A	0	0
Write Word E into Stack	1	X	0	↑	1	E	(E)	E	D	C	B	A	0	0
Write Word F into Stack	1	X	0	↑	1	F	F	E	D	C	B	A	↑	0
Write Word G into Stack	1	X	0	↑	1	G	F	E	D	C	B	A	1	0

Notes:

1 indicates logic HIGH — (X), (A), (B) etc. indicates data which can be overwritten

0 indicates logic LOW — ↑ indicates LOW to HIGH transition

X indicates "don't care" — ↓ indicates HIGH to LOW transition

Table 3: **Truth table for stack roll operations**

	FIFO stack control inputs					Data input	Resulting stack register contents						Output flags	
Operation	$\overline{\text{RLEN}}$	$\overline{\text{RL}}$	$\overline{\text{WREN}}$	$\overline{\text{WR}}$	$\overline{\text{RST}}$	**D0-D11**	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**SFUL**	**SAMT**
Roll Down[1]	0	↑	1	X	1	X	(F)	F	E	D	C	B	↓	0
Roll Down	0	↑	1	X	1	X	(F)	(F)	F	E	D	C	0	0
Roll Down	0	↑	1	X	1	X	(F)	(F)	(F)	F	E	D	0	0
Roll Down	0	↑	1	X	1	X	(F)	(F)	(F)	(F)	F	E	0	0
Roll Down	0	↑	1	X	1	X	(F)	(F)	(F)	(F)	(F)	F	0	↑
Roll Down	0	↑	1	X	1	X	(F)	(F)	(F)	(F)	(F)	(F)	0	1
Roll Down	0	↑	1	X	1	X	(F)	(F)	(F)	(F)	(F)	(F)	0	1

Notes:

[1]Initially stack registers R1 to R6 contain words A to F respectively.

1 indicates logic HIGH — (X)(A)(B) etc. indicates data which can be overwritten

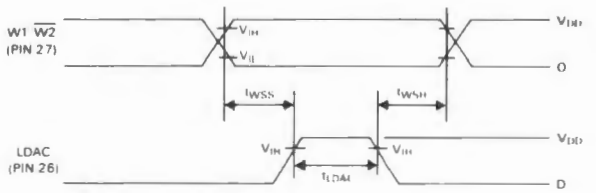
0 indicates logic LOW — ↑ indicates LOW to HIGH transition

X indicates "don't care" — ↓ indicates HIGH to LOW transition

Table 4: **Truth table for DAC register loading**

DAC Control Inputs				
Operation	W1/$\overline{W2}$	LDAC	$\overline{RST}$	DAC Output
Load DAC Register with all "0"s	X	X	0	Unipolar Mode: Output Assumes 0V Bipolar Mode: Output Assumes $-V_{REF}$
Load DAC Register from Word 1 Register	1	↑	1	DAC Converts Word 1
Load DAC Register from Word 2 Register	0	1	1	DAC Converts Word 2

Figure 4:
Timing diagram for DAC register loading



Applications

Unipolar binary operation (2 quadrant multiplication)

Figure 5 shows the analogue circuit required for unipolar operation with table 5 giving the input/output relationship. With a d.c. reference voltage or current (positive or negative) the circuit is a unipolar digital to analogue converter. With an a.c. reference voltage or current, the circuit provides 2 quadrant multiplication.

R1 allows full scale trimming, this is performed by loading the DAC register to 11111111 1111 and adjusting R1 until $V_{OUT} = -V_{REF}\left(\frac{4095}{4096}\right)$. Alternatively this adjustment may be performed by omitting R1 and R2 and trimming the reference voltage magnitude.

A phase compensation capacitor C1 (10 to 25pF) may be required for stability when high speed amplifiers are used. This capacitor cancels the pole formed by the DAC internal feedback resistance and output capacitance at OUT1. Amplifier A1 should be trimmed or selected to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT} (eg 0.24 mV with a 10V reference). Additionally the amplifier should have a low bias current over the temperature range being encountered. Bias current causes an output offset at V_{OUT} equal to Bias Current multiplied by the DAC feedback resistance which is nominally 15K.

Table 5: **Unipolar binary code table for circuit of Figure 5**

Binary number in DAC register MSB LSB	Analog output, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Bipolar Operation (4 quadrant multiplication)

Figure 6 shows the analogue circuitry with table 6 giving the code relationship for bipolar operation. With a d.c. reference (positive or negative) the circuit provides offset binary operation. When an a.c. reference is used the eleven LSB's provide digitally controlled attenuation of the reference with the twelfth MSB providing polarity control. The output should be set-up with the DAC register loaded to 1000 0000 0000 and R1 adjusted for V_{OUT} = 0V. Alternatively this adjustment may be performed by omitting R1 and R2 and adjustment of the ratio of R3 and R4 to obtain V_{OUT} =0V. Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5. As in the unipolar operation mode A1 must be chosen or trimmed for low V_{OS} and bias current. R3, R4 and R5 must be selected for matching and tracking. Mismatch of

Figure 5: **Unipolar binary operation (2-quadrant multiplication)**

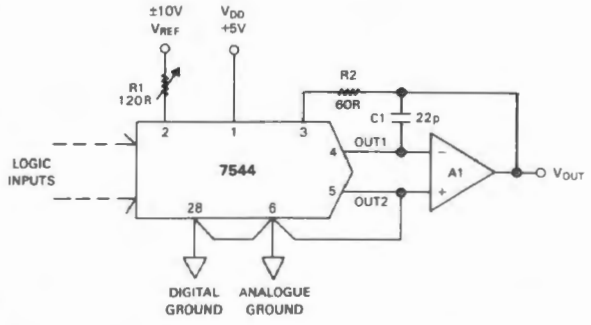
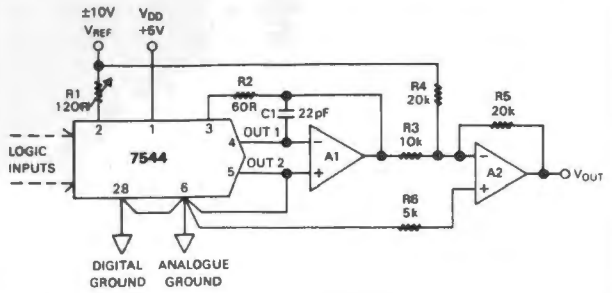


Figure 6:
Bipolar operation (4-quadrant multiplication)



2R3 or R4 causes both offset and full scale error. Mismatch of R5 and R4 and 2R3 causes full scale error. A phase compensation capacitor C1 (~ 10 to 25pF) may be required for stability.

Application guidelines

Grounding considerations

Voltage differences between the analogue and digital ground cause a loss of accuracy (d.c. voltage difference between the grounds introduces gain error; a.c. or transient voltages cause noise injection into the analogue output). The simplest solution is to tie the digital and analogue grounds together at the device terminals. In more complex systems where the two grounds intertie on the backplane it is recommended that diodes be connected back to back between the analogue and digital ground pins on the 7544 (IN4148 types).

Output amplifier offset

CMOS digital to analogue converters exhibit a code-dependant output resistance which in turn causes a code-dependant amplifier noise gain. The effect is a differential nonlinearity term at the amplifier's output of magnitude $0.67V_{OS}$ (amplifier input offset voltage). This differential nonlinearity adds to the R/2R differential nonlinearity. To keep monotonic operation it is recommended the amplifier offset voltage is adjusted to less than 10% of the converter's output resolution over the temperature range encountered.

Output resolution = $V_{REF}\,(2^{-n})$ where n = number of bits exercised.

Table 6: **Bipolar Code Table for offset binary circuit of Figure 6**

Binary number DAC register MSB LSB	Analog output, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Gain temperature coefficients

This has a maximum value of 5ppm/°C and a typical value of 2ppm/°C which corresponds to gain shifts of 1.4 LSB's and 0.57 LSB's over a 70°C range. When resistors are used to adjust the full-scale range as shown in figures 5 and 6 the temperature coefficients of R1 and R2 should be taken into account. It can be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:—

$$\text{Temp. Coefficient due to R1} = \frac{R1\,(\partial_1 + 300)}{-R_{IN}}$$

$$\text{Temp. Coefficient due to R2} = \frac{R2\,(\partial_2 + 300)}{+R_{IN}}$$

∂_1 = temp coefficient of R_1 in ppm/°C
∂_2 – temp coefficient of R_2 in ppm/°C
R_{IN} = DAC resistance at V_{REF} pin typ. 12kΩ/7kΩ min.

For high quality resistors ∂ is of the order of 50 ppm/°C and if R1 and R2 are small compared to R_{IN} their contribution to the overall gain temperature coefficient will be small.

With R1 = 120Ω and R2 = 60Ω and ∂_1 and ∂_2 = 50 the overall gain error temperature coefficient would be

$$5 + \frac{0.06}{7}(50 + 300) = 8\text{ppm/°C}.$$

RS data

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RS data

Display driver i.c. serial data input

Stock number 303-056

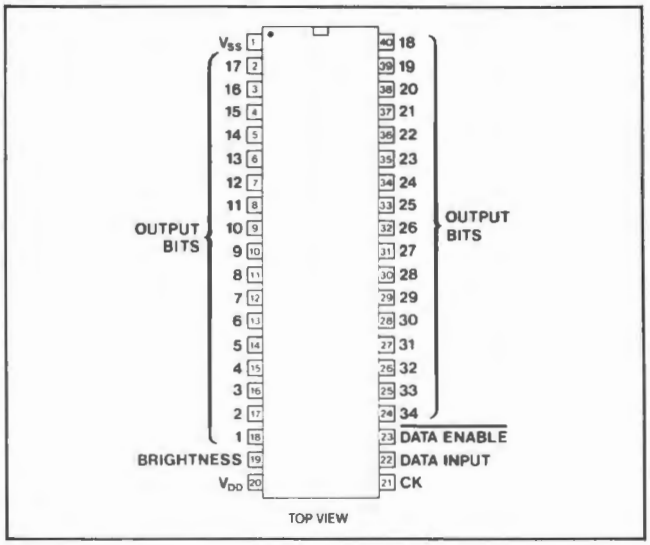
The RS 5450 is a universal monolithic MOS LED display driver with up to 15mA output current sink capability on each of the 34 outputs. Data is input in a serial form with a leading 1 start bit, followed by the serial data bits. This form of data entry is ideal for interfacing between serial data systems and 7-segment, alphanumeric or custom display panels. The 5450 internal data latches relieve the host system from display memory and control duties except for specific display updates.

Absolute Maximum Ratings

Supply voltage ____ 12V
Voltage at any pin ____ V_{SS} to (V_{SS} + 12)
Power dissipation 560 mW at + 85°C 1W at + 25°C
Junction temperature ____ 150°C
Lead temperature soldering 10S ____ 300°C
Operating temperature ____ −25°C to + 85°C
Storage temperature ____ −65° to + 150°C

Features

- Serial data input
- Wide supply voltage operation
- TTL Compatibility
- Brightness Control
- 34 Outputs for Universal display format



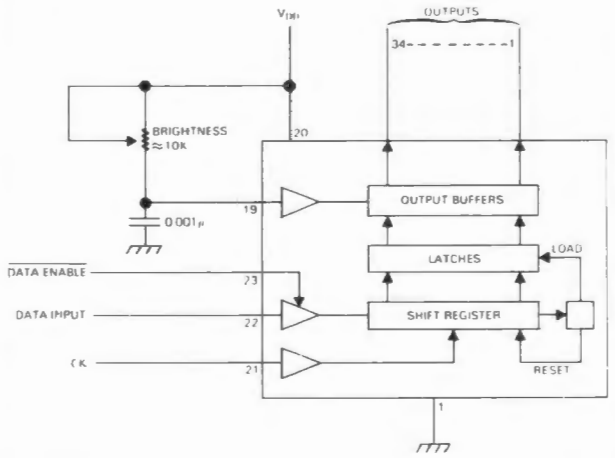
Electrical Characteristics T_A = −25 to + 85°C. V_{DD} = 4.5 to 11V, V_{SS} = OV

Parameter	Conditions		Min	Typ	Max	Units
Supply Voltage			4.75		11	V
Power supply current					7	mA
Input logic HIGH	4.75 ≤ V_{DD} ≥ 5.25		2.2		V_{DD}	V
	V_{DD} > 5.25		V_{DD} −2		V_{DD}	V
Input logic LOW	± 10μA Input bias		−0.3		0.8	V
Brightness input			0		0.75	mA
Output sink current						
Segment off	V_{OUT} = 3V				10	μA
Segment on (Note 1)	V_{OUT}=1V	Brightness input = OμA	0		10	μA
		Brightness input = 100μA	2.0	2.7	4	mA
		Brightness input = 750μA	15		25	mA
Brightness input voltage	Input current = 750μA		3.0		4.3	V
Clock frequency			0		0.5	MHz
Duty cycle			40	50	60	%
Output matching					±20	%

Note 1
V_{OUT} voltage is set by the user (see figure 4 for allowable operation). When a fixed resistor is used on the brightness input some variation in brightness **may** occur from one device to another.

RS data

Figure 1: **Block diagram**



Data input

The 5450 is designed to operate a variety of LED displays with minimal interface between the display and data source. Serial data transfer from the data source to the display is accomplished with 2 signals, serial data and clock. See figures 2 and 3.

A logic '1' at the input will turn on the appropriate LED.

Figure 2: **Input data timing**

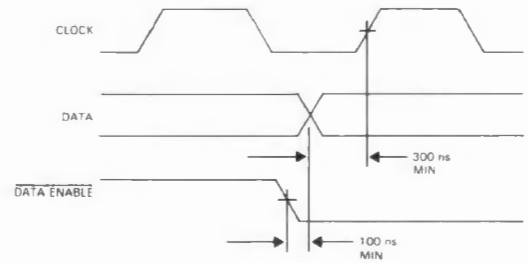
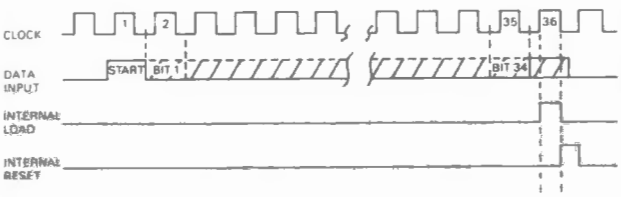


Figure 3: **Input data format**



Note Data input is in a don't care condition during 36th clock cycle. Data output is updated on the rising edge of the 36th clock pulse.

Applications

The display output current is approximately 20 times greater than the current into the brightness input pin 19, and is set using an external resistor to V_{DD}. See figure 1. An internal current limiting resistor normally 400Ω is present at this point. A 1nF capacitor should be connected between the brightness input and V_{SS} to prevent possible oscillations.

The output drivers are capable of sinking up to 15mA at 1.0V output voltage over the full operating temperature range. This may be adjusted provided the maximum chip power dissipation is not exceeded. See output characteristic graphs and the following equation.

Junction temperature=(V_{OUT}) X ($^{1}_{LED}$) X (No of outputs used) X (Thermal Coefficent of device package) $+T_A$

Eg.

At an ambient temperature $T_A = 25°C$, temperature coefficient 124°C/W. $I_{LED} = 10mA$, 34 outputs used, maximum junction temperature 150°C, then

$$V_{OUT} = \frac{150 - 25}{10 \times 10^{-3} \times 34 \times 124} \qquad V_{OUT} = 2.96V$$

So with a standard 0.2in LED the LED supply should be 2.96 plus the forward voltage drop of the LED at the typical current i.e. 2V, so the LED supply voltage would be 5V.

Figure 4: **Output characteristic graphs**

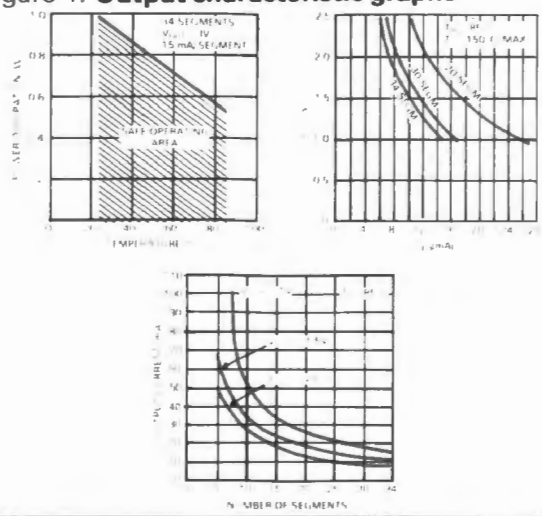
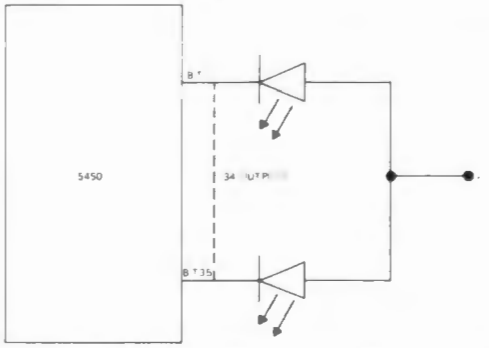


Figure 5: **Typical Display Connections**



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RS data

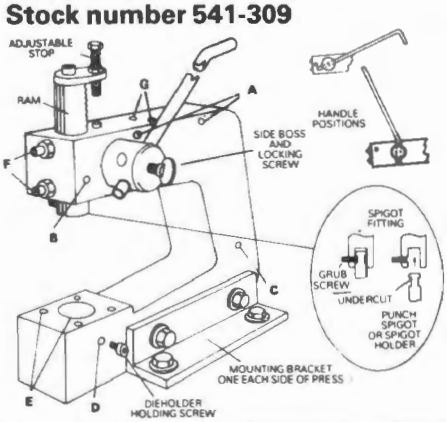
Rack and pinion lever press and accessories

A bench mounting, hand operated rack and pinion lever press offered with punching, cutting and forming accessories (separately available) to provide an invaluable service for sheet material working in workshop and production environments. The press has a high quality carbon steel frame capable of applying a constant pressure of up to 3,000 lbf max. (1360kgf) over the full stroke. The press and accessories are very straightforward to set up and operate, this data sheet describes their range of suitable functions with sufficient detail for the user to adapt the press to his own custom design tooling if required.

Basic dimensions (mm)

Frame size L x W x H	270 x 48 x 190
Overall width (including mounting brackets)	165
Maximum height (excluding handle)	335
Handle length	560
Bench mounting holes (4 x 10 clear)	150 x 94 centres

Figure 1 **Rack and pinion lever press Stock number 541-309**



Key to Figure 1.

- **A** Two mounting holes for the crop and shear tool 541-387
- **B** Two mounting holes (one each side of press) for stripper 541-573
- **C** Two mounting holes (one each side of press) for back stop 541-551
- **D** Two mounting holes (one each side of press) for side stop 541-567 and the holding screw for dieholder 541-719
- **E** Five base mounting holes to accept and locate RS dieholders and tool accessories
- **F** Ram set screws. These have been set for correct ram alignment. No further adjustment is required.
- **G** Two mounting holes for the handle clamp block, circle cutting attachment 607-623.

Features

- High strength frame
- Compact size
- Easily bench mounted
- Straightforward tool setting procedures
- Versatile range of accessories
- Adaptable for custom tooling
- Constant pressure over full stroke

Specification

Ram diameter	31.57
Maximum pressure at ram	1360kg
Depth of throat	150
Throat clearance (daylight)	83
Stroke length (stop fitted)	6 to 60
Max stroke length (stop removed)	76
Punch and die fittings	
Ram spigot hole 22mm deep x 18± ⅛ dia.	
Central die hole (through) 38.03± ⅛ dia.	
Dieholder fixing holes (4 x M8)	55 x 35 centres
Weight (nett)	14.2kg

Maximum allowable sheet material thicknesses for RS accessories unless otherwise specified

Fibreglass board	2
S.R.B.P. board	3.2
Aluminium	2.5
Mild steel (16 s.w.g. – 28 tons/in^2 u.t.s.)	1.62

Index to accessories

Press assembly and operation

The press is supplied with a handle, 2 bench mounting brackets (with mounting hardware), an adjustable stop screw, nut and washer, a dieholder holding screw, a grub screw, plus a set of hexagon keys for all fittings.

Bench mounting

Mount the press on a rigid, stable surface, taking into account the overall weight, handle length and pressure specified. Typical mounting surfaces would include mechanical engineering benches and heavy woodworking style benches. Use RS work bench 607-320. Bolt the brackets, one each side of the press, as shown with two bolts M10 x 80mm long. Drill the bench with 4 holes M10 clearance 150 x 94mm centres. Ensure that the central die hole in the press base overlaps the edge of the bench to permit metal cut-outs and offcuts (also tools, etc.) to pass through. (Alternatively drill a hole greater than 38mm diameter through the bench.) Secure the press to the mounting surface with four bolts M10 x 100mm long.

Handle and adjustable stop

The handle may be fitted into the side boss in the various positions as shown in Figure 1. Orientate the handle so that its movement is *easily controlled* and *safe* to operate.

Always lock the handle with the screw provided to prevent accidental slippage.

IMPORTANT: Fit the adjustable stop screw, locknut and washer as shown, using the stop to limit ram downward movement. Uncontrolled over-reach of the ram may cause injury, damage to tools and working materials.

Set the handle movement and adjustable stop so that the ram downward stroke gives full closure of any punch and die fitted. Also ensure that there is sufficient clearance (with the ram in the up position) for material feeding, punch adjustment and tool dismantling.

When the press is operated initially there will be a degree of resistance to ram movement due to the lubricant grease in the rack and pinion mechanism. This is quite normal and the ram will run more easily with use.

Spigot fitting

The spigots on all RS punches and spigot holders have an undercut as shown in Figure 1 under 'spigot fitting'. Fix the punch into the ram by locating the locking grub screw into the undercut of the spigot. This gives a positive hold on the punch during operation and also prevents damage to the spigot/ ram mating surfaces during the life of the punch.

General points of safety and information

When operating the press always hold the handle so that ram movement is controlled at all times. Ensure tool punches and dies are aligned correctly, otherwise they may be damaged, considerably shortening life.

Lubrication

Use RS multipurpose oil 555-689 or RS multipurpose grease 556-446 to lubricate and protect all running surfaces of the press.

For easier punching, shearing and forming use a light smearing of RS multipurpose oil 555-689 or RS multi-purpose grease 556-446 on cutting and folding edges of tools.

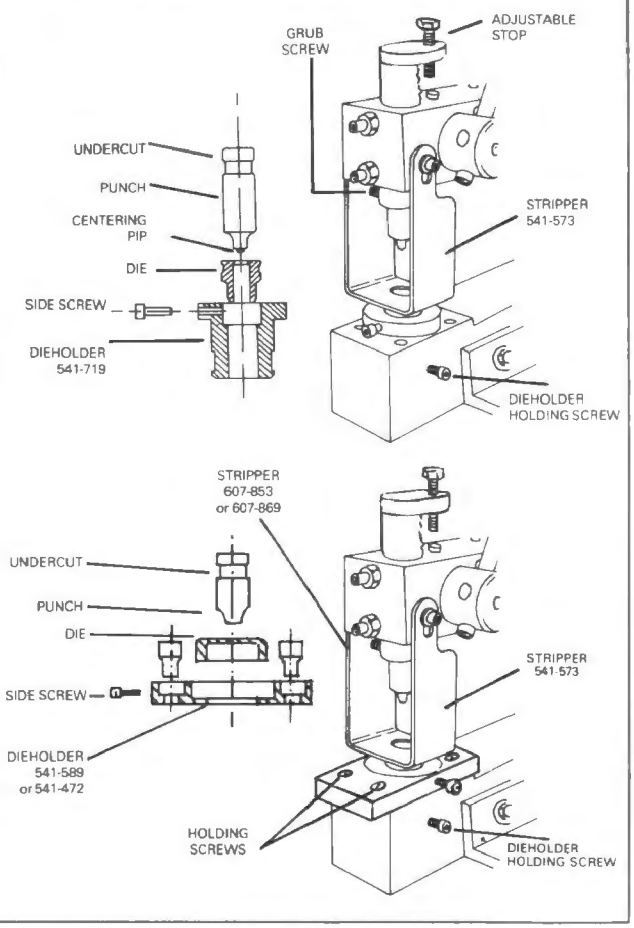
Circular, nibbling, keyhole and component hole punching

Accessories required

Punch and die types	Stock Nos.	Use stripper	Use dieholder
Circular 3mm to 12mm	541-804 to 541-927	541-573	
Circular 1/8in to 7/16in	541-724 to 541-775	541-573	541-719
Nibbling	541-371, 607-639		
Indent	607-645, 606-816	541-573	
Keyhole	607-651, 607-667, 607-689 and 607-695	607-853	
Keyhole	607-673	607-869	
Component	607-702 to 607-730, 607-752 to 607-803 and 607-847	607-853	541-589
Component	607-819 to 607-831	607-869	
T03	606-822	*	541-472

*Special stripper provided with the tool.

Figure 2 **Settings for circular, nibbling, keyhole and component punches and dies**



Setting procedure

When setting punches and dies in the press, it is essential to follow the procedure below so that punch and die alignment is true, otherwise tools may be permanently damaged. The essence of setting is to tighten down, punch – die – dieholder in that order. Use the hexagon keys provided with the press.

1 Raise the ram to the 'up' position.
2 Fit the punch into the ram, locating the grub screw in the undercut.

3 Locate the appropriate dieholder into the base mounting holes of the press, using the holding screw(s) provided, and drop the die into the dieholder. Follow the relevant setting Figure 2.

4 Bring the punch slowly down into the die, orientating their position as required.

5 With the punch in the die, lock the punch in the ram and the die in the dieholder using the side screw.

6 Lock the dieholder with the holding screw(s).

7 Raise and lower the punch in the die several times to ensure that they align and do not foul each other.

8 Make sure all locking screws are tightened firmly. Do not overtighten.

9 Set the adjustable stop on the press to limit ram throw.

It is recommended that punches enter the die by 1/16in (1.6mm) approximately.

Note: for the T03 tool, as hole piercing is a two stage operation, the two shorter punches should enter the die by 1.6mm.

Punching and stripping

10 Feed the working material under the punch, aligning the punch centering pip* against the workpiece in the required position. Use a reference mark on the workpiece or side and back stops (541-567 and 541-551).

11 For a stripping operation fit a stripper as shown in Figure 2 so that the hole(s) in the stripper allow(s) full closure of the punch and die yet gives sufficient clearance for material to feed freely between die and stripper.

12 Pull the handle down firmly to pierce the material then raise the punch.

13 The stripper will hold the material down as the punch is raised thus automatically separating the material from the punch.

14 Repeated punching can now be made in rapid succession.

* Nibbling tools do not have a centering pip. Use the side and back stops for references.

Points of caution and information

15 Use materials up to the thickness specified for the press.

16 Dies are counterbored to prevent material build up, allowing natural fall away of cut-outs.

17 When cutting edges wear with use, punches may be ground down.

18 For easier material punching, larger punches have a special profile *(manufacturer's patent pending)*.

19 Protect the punch and die surfaces and edges from damage by storing safely. Use RS storage boxes 607-594 and 607-601.

Punching large circular holes

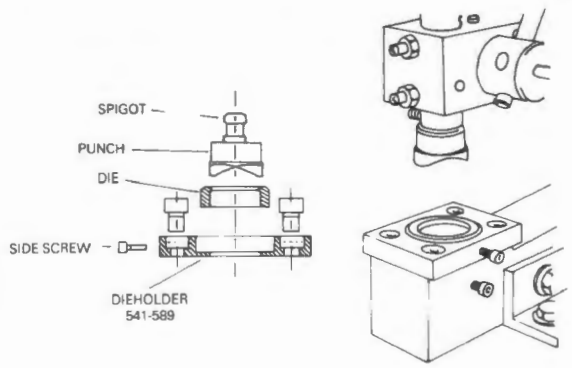
Accessories required:

Metric punches and dies 20mm to 27.5mm dia.
Imperial punches and dies 3/4in to 1in dia.
Dieholder 541-589.

Setting procedure

Following the setting procedure as described for small punches and dies with the exceptions as below. Items **1** and **2** as page 2.

Figure 3 **Setting for large circular punches**



3 Locate and retain dieholder 541-589 using the four dieholder mounting screws provided Figure 3. Drop the die into the die holder but do not tighten locking screws at this point.

Items **4** to **5** as page 3.

Punching procedure

These punches do not require a stripper and should be used as follows.

10 Feed the working material under the punch and centralise by marker or by using the end and back stops as described on page 11.

11 Pull the handle down firmly to pierce the material.

12 Loosen the locking screw in the ram and pass the punch through the workpiece, die and through the base of the press.

13 Before punching the next hole raise the ram and refit the punch (see spigot fitting) and bring it down into the die to ensure correct alignment.

14 Lock the punch and repeat the punching procedure.

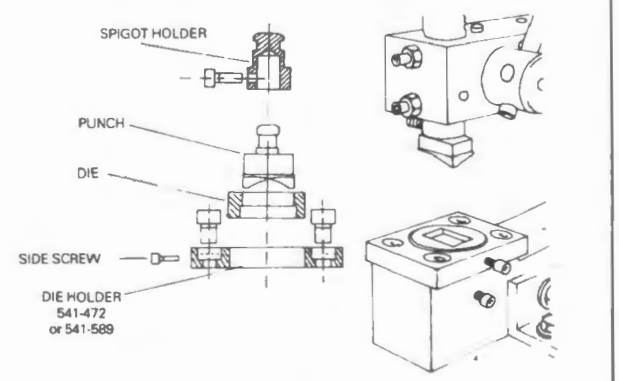
Note the points of caution and information items on this page 15, 16, 18 and 19.

Punching rectangular holes (also medium sized circular holes)

Accessories required:

Rectangular punches and dies.
Circular punches and dies 12.5mm to 16.5mm dia.
Circular punches and dies 1/2in and 5/8in dia.
Dieholders 541-472, 541-589.

Figure 4 **Setting for rectangular punches and medium sized circular holes**



Setting procedure

1 Raise the ram to the 'up' position.
2 Fit spigot holder into ram and secure as under spigot fitting – page 1.
3 Fit and retain the punch lightly in the spigot holder.
4 Locate and retain dieholder using the four dieholder holes and screws provided Figure 4. Drop the die into the dieholder but do not tighten locking screws at this point.
5 Ensure that die orientation is correctly positioned for location on the workpiece. If necessary use the back and end stops page 11 as references.
6 Bring the punch slowly down to give correct alignment and clearance when in the die.
7 In this set position, lock the punch in the spigot holder, lock the die in the dieholder and secure the dieholder with the four screws.
8 Raise and lower the punch in the die several times to ensure that they align and do not foul each other.
9 Make sure all locking screws are tightened firmly. Do not overtighten.
10 Set adjustable stop (see Figure 1) to limit ram throw.

Punching procedure

Follow items **10** and **11** under 'large circular holes' then:

11 After the punch has pierced the workpiece, loosen the locking screw in the spigot holder to release the punch.
12 Pass the punch through the workpiece, die and through the base of the press. Leave the spigot holder in the ram.
13 Before punching the next hole raise the ram and refit the punch into the spigot holder.
14 Re-align punch in the die and lock, repeating the punching procedure.

Note the points of caution and information items **15, 16, 18** and **19** on page 3.

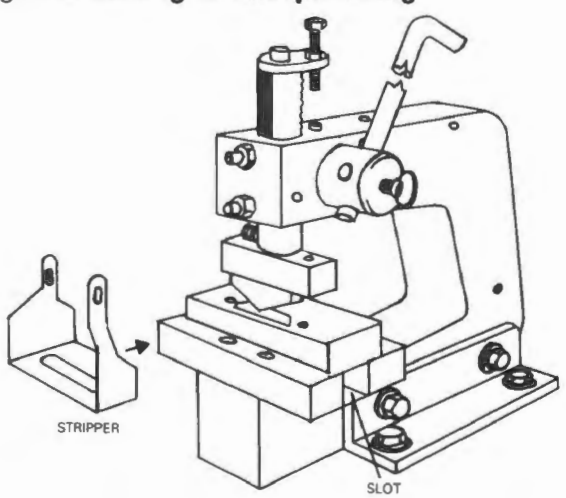
'D' hole punching

Accessories required

'D' punches and dies 607-415 to 607-522.

Strippers 607-516 and 607-522.

Figure 5 **Setting 'D' hole punching**



Used in conjunction with RS press 541-309 these punches and dies will cut the complete range of panel cut-outs for standard 'D' connectors. Both component and fixing screw holes are punched in one operation.

It is essential that a stripper is used with these tools. See page 1 for maximum material thicknesses.

For 9-way and 15-way 'D' hole punches use stripper 607-516. For all other sizes use stripper 607-522.

Setting and punching procedure

1 Fit the punch in the die, raise the ram to the 'up' position and place the die on the press base.
2 Lower the ram so that the punch spigot runs into the ram hole. Retain the die in the press base with the four screws provided, but do not lock at this point.
3 Turn the ram locking screw so that it holds the punch spigot at the undercut.
4 Raise and lower the punch in the die, making suitable adjustments to ensure free alignment.
5 Lower the punch into the die, lock the punch in the ram and the die to the base.
6 Raise the punch and fit the stripper (see Figure 5) so that the hole in the stripper allows full closure of the punch and die (without fouling) yet gives sufficient clearance for material to feed freely between die and stripper.
7 Set the adjustable stop to limit ram throw.
8 Feed the workpiece under the stripper and align using centre lines on the workpiece with the bottom of the 'V' shape of the punch which will be the centre of the punched hole.
9 Pull the handle down to pierce the workpiece then raise the punch.
10 The stripper will hold material down as the punch is raised.

Points of caution and information

11 Use materials up to the maximum thicknesses as specified on page 1.
12 To prevent material build-up ensure that the slot (see Figure 5) does not get jammed with cut-outs.
13 Always ensure that tools are free of waste material and are lightly oiled before storage.
14 Protect the tool surfaces and edges from damage by storing in the packaging supplied.

Internal circle cutting

Accessories required:

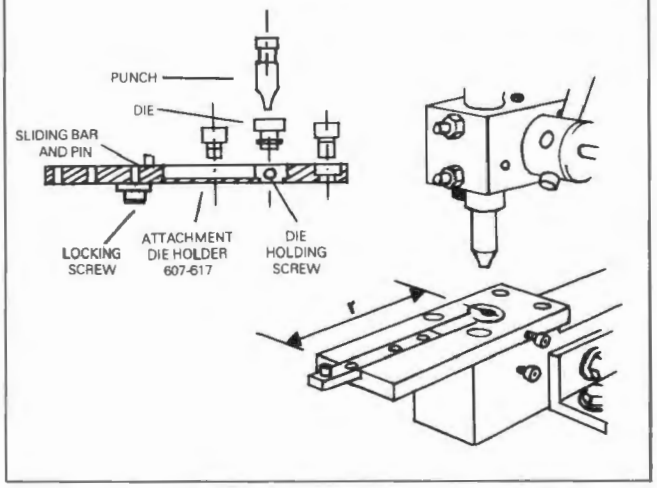
Radius nibbling attachment/dieholder 607-617.

Elliptical nibbling punch and die 607-645.

Circular hole punches, metric 3mm to 12mm, ⅛in to 7/16in (see item 15).

Stripper 541-573.

Figure 6 **Setting for radius nibbling attachment dieholder, punch and die**



A nibbling attachment/dieholder which in conjunction with elliptical punch and die 607-645 can be used to cut internal circles between 30mm and 140mm dia.

Punch, die, attachment/dieholder setting procedure

1 Raise the ram to the 'up' position.

2 Fit the punch into the ram, locating the grub screw in the undercut.

3 Set the attachment/dieholder 607-617 down onto the press base and retain with the four screws provided. Do not lock at this point.

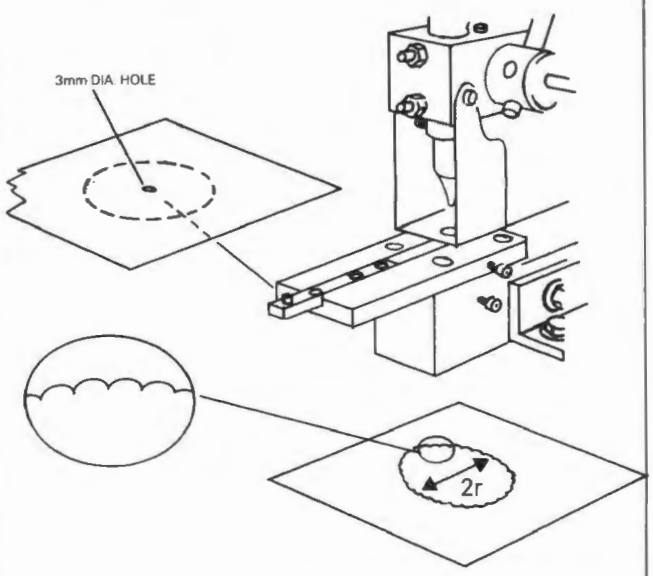
4 Lower the punch into the die, orientating their position so that the ellipse shape will cut the closest approximation to a circle.

5 With the punch in the die, lock the punch in the ram, the die in the attachment/dieholder, then secure the dieholder firmly to the press frame.

6 Raise and lower the punch in the die several times to ensure that they align and do not foul each other. Make sure all screws are tightened firmly, but not overtightened.

7 Set the adjustable stop (see Figure 1) to limit ram throw. It is recommended that the punch enters the die 1/16in (1.6mm) approx.

Figure 7 **Radius nibbling and internal circle cutting**



Radius nibbling and circle cutting with stripping action

8 The attachment has a sliding bar and pin which can be positioned and locked in the attachment/dieholder so that the pin is set at a distance r between the pin centre and the back edge of the elliptical die shape, see Figure 6. Where 2r is the diameter of the completed hole, see Figure 7.

9 Note that the sliding bar has three tapped holes, which will accept the locking screw, see Figure 6. By using the appropriate tapped hole, the pin can be locked in any position with r ranging from 15mm to 70mm.

10 Drill or punch a 3mm dia. hole in the workpiece, and locate the pin through the hole, see Figure 7, so that it acts as a centre fulcrum about which the workpiece can revolve. Note that turning may be limited by the throat depth of the press.

11 Fit stripper 541-573 as shown Figure 7 for repetitive punching. Set the stripper position so that the hole in the stripper allows full closure of the punch and die but with sufficient clearance for material to feed between the die and stripper.

12 Commence nibbling by pulling the press handle down firmly to pierce the material, then raising the punch to give stripping action.

13 Turn the workpiece on the pin fulcrum and continue to nibble until a hole 2r diameter is cut out.

14 As the elliptical punch produces a ripple effect along the cutting edge (see inset Figure 7), smooth down with a file if necessary.

15 Accurate and repeatable 5 hole punching, see Figure 8, can be achieved using circular hole punches.

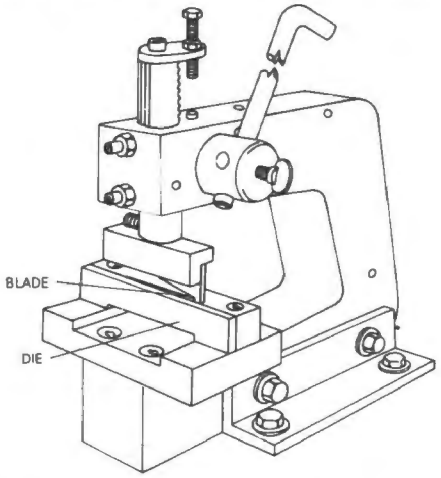
Figure 8

16 Note the points of caution and information given under points 15 to 17 and 19 (page 3).

Cutting and slotting

Accessory required:
Cutting tool 541-400.

Figure 9 **Setting for cutting tool 541-400**



Used in conjunction with RS press 541-309 this guillotine style tool has a 3.18mm (⅛in) width blade with toe for accurate cutting alignment (overall length 70mm).

The blade cuts a 63.5mm length by ⅛in width slot with every full stroke. Will give a cutting and slotting action in sheet materials (see page 1 for maximum thicknesses) without material distortion. Features optimum usage with minimum wastage. Can also be used for trimming corners.

Setting procedure

1 Raise the ram to the 'up' position.
2 Set the die down on the press base and retain with the four screws provided. Do not lock at this point.
3 Fit the blade into the ram as shown in Figure 9 ensuring that the locking screw in the ram holds the blade spigot at the undercut. Do not lock at this point.
4 Bring the ram slowly down and locate the complete length of the blade into the die slot.
5 Lock the blade in the ram and then the die down to the base.
6 Raise the ram up and down several times to ensure free alignment of blade and slot.
7 Set the adjustable stop (see Figure 1) to limit ram throw. It is recommended that the stop is set so that the blade enters the slot along its full length during operation but does not 'bottom' onto the die body.

Figure 10a

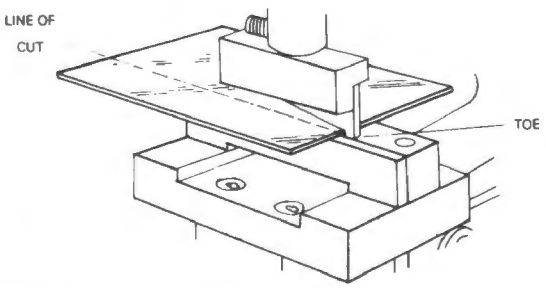


Figure 10b

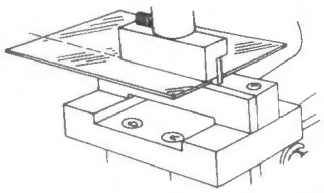
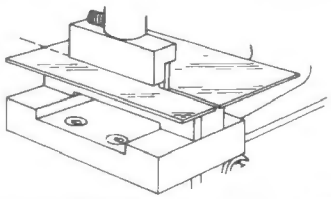


Figure 10c



Operating procedure

8 Lower the blade so that the toe just enters the slot, then feed the workpiece (flat against the die face) up to the position as shown in Figure 10a.
9 Holding the workpiece steady, pull the handle down firmly following the line of cut with the blade edge to the position as shown in Figure 10b.
10 Raise the blade, feeding the workpiece along, keeping the toe in the slot as shown in Figure 10c.
11 With the workpiece flat on the die face repeat as in **9** and **10** until the line of cut is complete.

The tool may also be used to crop edges and corners.

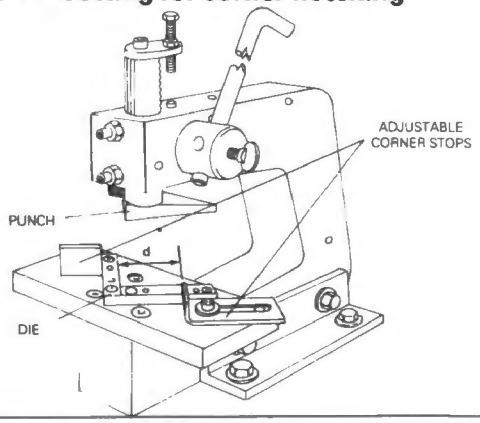
Points of caution and information

12 Use materials up to the max. thicknesses as specified on page 1.
13 To prevent material build up ensure that the slot does not get jammed with cut-outs.
14 Always ensure that the tool is free of waste material and is lightly oiled before storage.
15 Protect the tool surfaces and edges from damage by storing in the packaging supplied.
16 Do not use the toe for punching or cutting.

Corner notching

Accessory required:
Notching tool 541-416.

Figure 11 **Setting for corner notching**



A corner notching tool used in conjunction with RS press 541-309 having a 90° Corner punch with 53mm length cutting edges (tapered for easier cutting) and a compatible die base with adjustable corner stops to set corner lengths independently between 0 and 65mm.

Setting instructions

1 Raise the ram to the 'up' position.
2 Set the die down onto the base as shown in Figure 11. Retain with the four screws provided but do not lock at this point.
3 Place the punch in the die.
4 Slowly lower the ram, locating the hole in the ram onto the punch spigot.
5 Using the adjustable stop (see Figure 1) to hold the ram in position, set the 90° corner of the punch squarely in the 'V' of the die, locking the punch in the ram at the spigot undercut.
6 Raise and lower the punch in the die so that there is a clearance between cutting edges.
7 Lower the punch into the die and lock the die base.
8 Raise and lower the punch again to ensure free movement in the die.
9 Set the adjustable stop (Figure 1) to limit ram throw.

Figure 12a

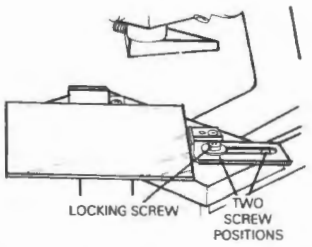
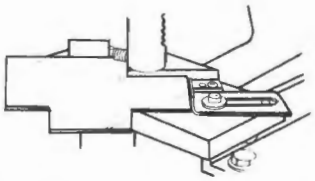


Figure 12b



Adjustable corner stops

10 Two stops Figure 11 have slots for adjusting their position with respect to the die cutting edges.
11 Set distance 'd' see Figure 11 to give a repeatable corner notch of that dimension. Lock the stop.
12 Locking screws can be used in two positions see Figure 12a to give set corner dimensions infinitely adjustable up to 65mm.
13 Note that the punch sides are 53mm length, being the maximum corner which can be cut at one stroke.
14 The stops may be removed completely for larger notching.

Operating procedure

15 It is important to note that the workpiece reference edges should be at 90° so that true right angle corners can be cut by the tool.
16 Set the stops to the required distance.
17 Offer the workpiece up against the stops and flat against the die face, see Figure 12a.
18 Holding the workpiece, pull the handle firmly down in one stroke, to punch a corner notch as shown in Figure 12b.
19 For corners in excess of 53mm per side use the punch to nibble away smaller corner pieces until the full corner has been cut.

Points of caution and information

Follow the points as described under cutting and slotting (cutting tool 541-400).

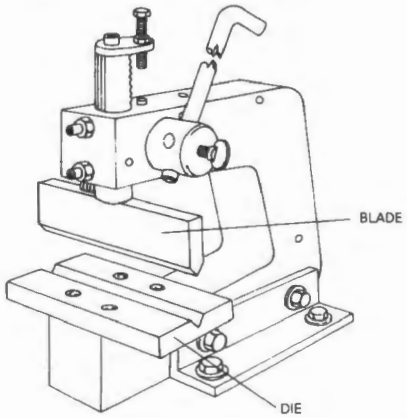
Bending and box forming

Accessories required:

'V' bending tool 541-422.
Corner notching tool 541-416.

A 'V' bending tool for forming up to 90° bends, comprising a 160mm 'V' groove die and 5 blades 50, 75, 100, 125 and 150mm length. Blades are not hardened so that they can be cut (with H.S.S. hacksaw) or machined to required length. Use in conjunction with RS corner notching tool 541-416 to form small boxes as described in this instruction.

Figure 13 **Setting for metal bending**



Setting procedure

1 Raise the ram to the up position.
2 Set the die down onto the base and retain by the four screws provided. Do not lock at this point.
3 Fit the appropriate blade to the ram, see Figure 13, ensuring that the locking screw in the ram holds the blade spigot at the undercut. Do not lock at this point.
4 Lower the ram slowly and locate the 'V' of the blade into 'V' groove of the blade.
5 In this position, lock the blade in the ram and the die to the press base.
6 Raise and lower the blade ensuring that it seats fully and squarely into the groove.

Figure 14a

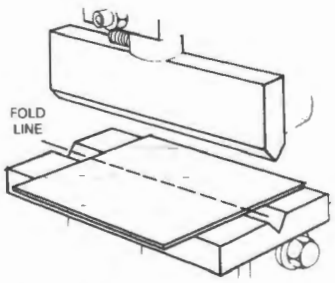
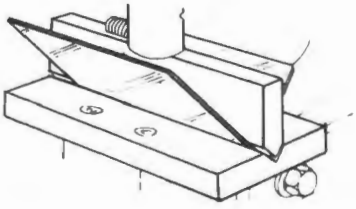


Figure 14b



Bending procedure

7 For good forming, the length of fold should be no more than 5mm longer than the blade.

8 After marking the material with a fold line, place the workpiece flat on the die face centrally under the blade, Figure 14a.

9 Lower the blade slowly and align it centrally on the fold line.

10 Pull the handle down firmly in one stroke, to form a bend up to 90°.

11 With the blade pressed fully home, a 90° bend is formed as shown in Figure 14b see note †.

12 Raise the blade and extract the workpiece clear of the press.

Note †. For softer materials an overbend >90° may be obtained. Adjustment to 90° may be made using the adjustable stop, see Figure 1, to limit blade throw.

Box making

Please note the limitations on box size given in Table 1.

13 Preparation will require sheet material cut as shown in Figure 15.

14 For depth of box 'D' cut corner notches as described under corner notching.

15 The width 'W' and length 'L' of the box will determine blade lengths. Naturally, for a square box only one blade is needed.

16 For good forming the blade length should be slightly shorter than the length of fold, but NOT more than 5mm shorter.

17 With all fold lines clearly marked as shown in Figure 15, follow items **7** to **11** for each of the four box sides, Figure 15.

18 To attain the box sizes listed in Table 1 always bend with the main body of the box away from the press.

Figure 15 **Box formation**

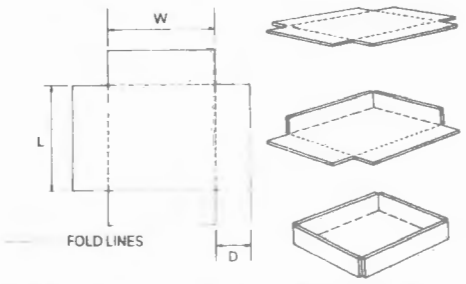


Table 1 **Range of possible box sizes**

For Lengths 'L' or widths 'W' between:	maximum depth of box 'D' is:
20 and 30mm 30 and 45mm	10mm to 20mm increasing pro rata 20mm
45 and 75mm 75 and 90mm	20mm to 50mm increasing pro rata 50mm
90 and 95mm 95 and 105mm 105 and 110mm	50mm to 60mm increasing pro rata 60mm to 70mm increasing pro rata 70mm
110 and 115mm 115 and 119mm	70mm to 75mm increasing pro rata 75mm
120 and 135mm 135 and 155mm	100mm to 110mm increasing pro rata 110mm to 130mm increasing pro rata
Note: for rectangular shaped boxes, depth should be determined by the shortest side dimension L or W.	

Points of caution and information

19 Use materials up to the max. thickness as specified on page 1.

20 When cutting blades to required length ensure that the spigot remains at the centre line of the blade length.
(Note, the maximum and minimum blade lengths are 150mm and 19mm respectively.)

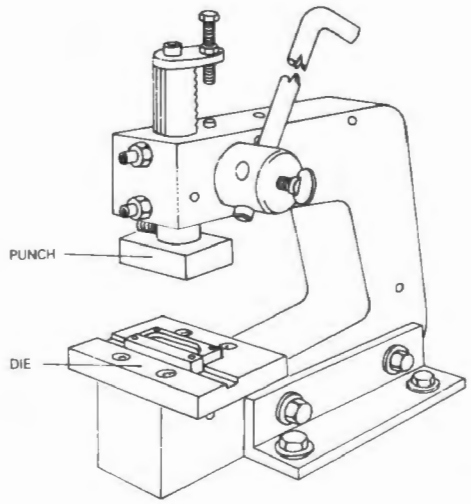
21 When bending always place the workpiece centrally under the blade.

22 Protect the tool surfaces and edges from damage by safe storage.

Louvre forming

Accessory required:
Louvre tool 541-393.

Figure 16 **Setting for louvre forming**



A louvre forming tool 44.4mm length by 10mm width to form ventilation apertures. Minimum spacing between adjacent louvres 5.5mm, see Figure 17b.

Setting procedure

1 Raise the ram to the 'up' position.

2 Set the die down on the press base with the 'D' shape of the louvre facing either inwards or outwards as required. Figure 16 shows the 'D' facing inwards.

3 Retain the die with four screws provided but do not lock at this point.

4 Fit the punch into the ram and hold with the locking screw in the undercut of the spigot.

5 Lower the punch, slowly locating it into the die.

6 With the punch set fully into the die, lock the punch in the ram, then the die to the base.

7 Raise and lower the punch in the die to ensure free movement and no fouling.

Figure 17a

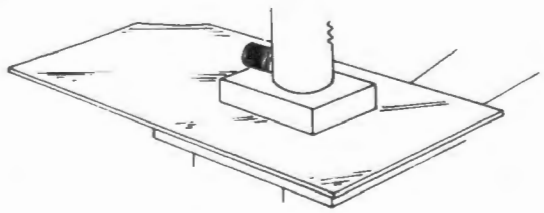
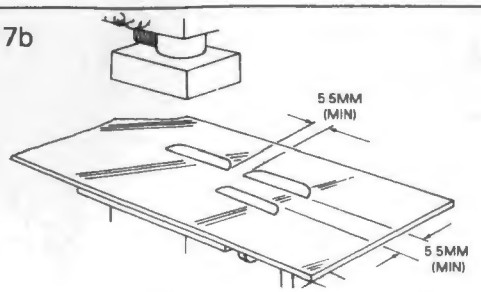


Figure 17b



Louvre forming procedure

8 With the ram raised, place the workpiece flat on the dieface.

9 Lower the ram, aligning the punch against the workpiece in the required position. Use a reference line on the workpiece or the end and back stops as described on page 11.

10 Holding the workpiece, pull the handle down firmly in one stroke until the punch pierces the material and seats fully into the die, see Figure 17a.

11 Raise the ram and re-position the workpiece ready for the next louvre, Figure 17b.

12 Spacing between louvres is limited to 5.5mm (min.) top to bottom and side to side.

Points of caution and information

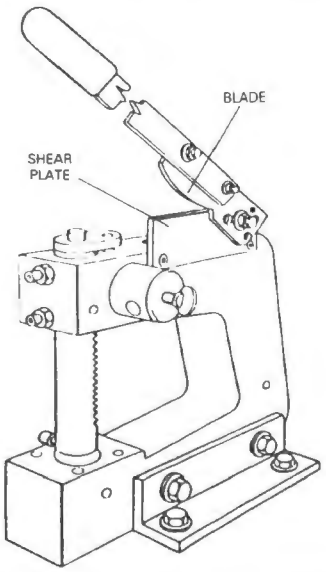
13 Use materials up to the max. thickness as specified on page 1.

14 Protect the tool surfaces and edges from damage by safe storage.

Cropping and shearing

Accessory required:
Crop and shear tool 541-837

Figure 18 **Setting for cropping and shearing**



A tool for shearing sheet material and cropping rod, which can be mounted to RS press 541-309, see Figure 18, or independently mounted using the bracket supplied with the tool, see Figure 20. Lever length is 560mm, Blade length 75mm.

Setting up procedures

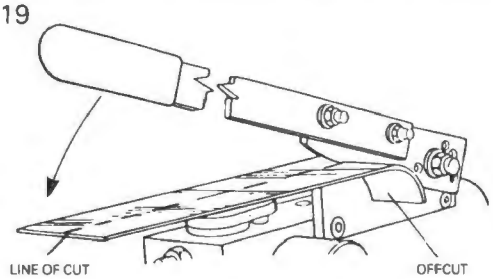
1 When using RS press 541-309, ensure that it is securely mounted to a rigid surface (see Bench mounting, page 2).

2 Remove the adjustable stop from the press, lower the ram, then remove the handle.

3 Mount the shear plate, using the two countersunk head screws provided, as shown in Figure 18 (see also mounting holes B, Figure 1, page 1).

4 For independent mounting, bolt the 'L' shaped bracket, supplied with the tool, to a suitably rigid bench surface (2 mtg. holes M10 clear, 150mm centres), then mount the tool to the bracket using the two countersunk head screws provided as shown in Figure 20.

Figure 19



Sheet material cutting procedure

5 Use sheet material to the maximum thickness as given in Table 2.

6 With the blade up, slide the workpiece horizontally up to the blade.

7 With forward pressure on the workpiece, pull the lever down so that the blade bites into and shears along the line of cut, Figure 19.

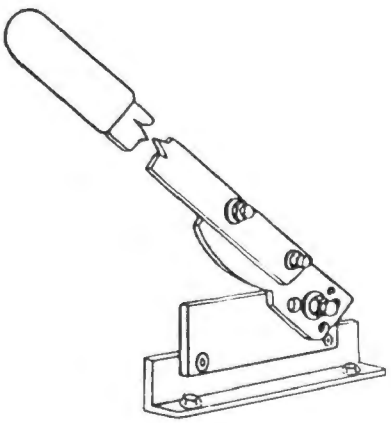
8 Continue to feed the material, cutting with a scissor action.

9 Note that the offcut as indicated in Figure 19 will bend naturally during cutting.

Table 2 **Maximum thickness of sheet material**

Material	Max thickness
aluminium	14swg (2mm)
mild steel	18swg (1.2mm)
fibreglass and paper pcb's	1.6mm

Figure 20 **Bench mounting**



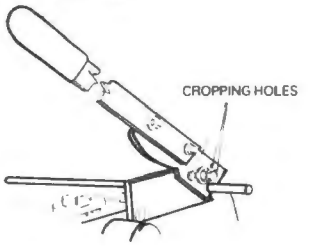
Rod cropping

This tool is also capable of cropping brass, copper and mild steel rod and studding. The tool has 4 cropping holes – diameters 3, 4, 5 and 6mm clear.

10 Mount the tool as described under items 1 to 4. Position the lever so that the cropping holes in the blade align with those in the shear plate.

11 Insert a rod of the appropriate diameter as shown in Figure 21 and holding it steady, bring the lever down, cropping to the required length.

Figure 21 **Rod cropping**



Points of caution and information

12 When handling smaller size materials, keep hands well clear of the cutting edges, by gripping the material with pliers.

13 Lightly oil the cutting and cropping edges for easier shearing and longer blade life.

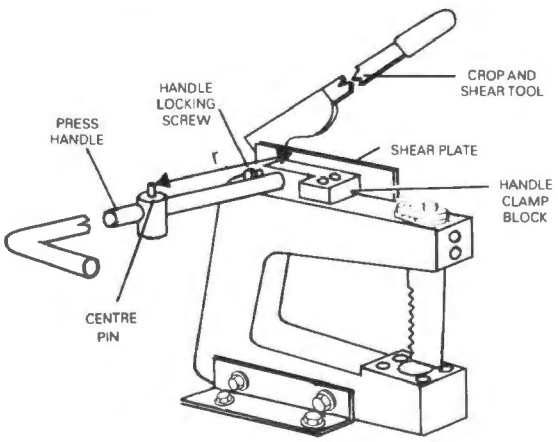
14 Store the tool with the blade closed protecting the cutting edges from damage.

Circle cutting (external)

Accessories required:

Attachment 607-623
Crop and shear tool 541-837

Figure 22 **Setting for circle cutting**



An attachment which when fitted to the top of the press in conjunction with the press handle and crop and shear tool 541-837 will enable the user to cut external radii and circles.

Setting procedure and cutting

1 Follow the setting up procedure points **1** to **3** for crop and shear tool 541-837 (page 9).

2 Mount the handle clamp block to the top of the press at holes G, (see Figure 1, page 1).

3 Slide the centre pin over the press handle then fit and lock the handle into the clamp.

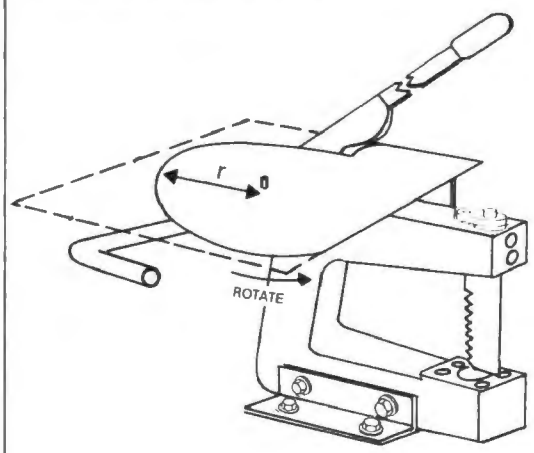
4 Move the centre pin along the press handle to a set distance r between the pin and the cutting edge of the shear plate (see Figure 22).

5 With a 3mm hole punched or drilled in the workpiece, locate onto the centre pin (see Figure 23).

6 Commence shearing in the same manner as points **5** to **9** of crop and shear tool (page 9).

7 Revolve the workpiece around the centre pin, continuing to cut until the required length of radius or circle is complete.

Figure 23 **Circle cutting**



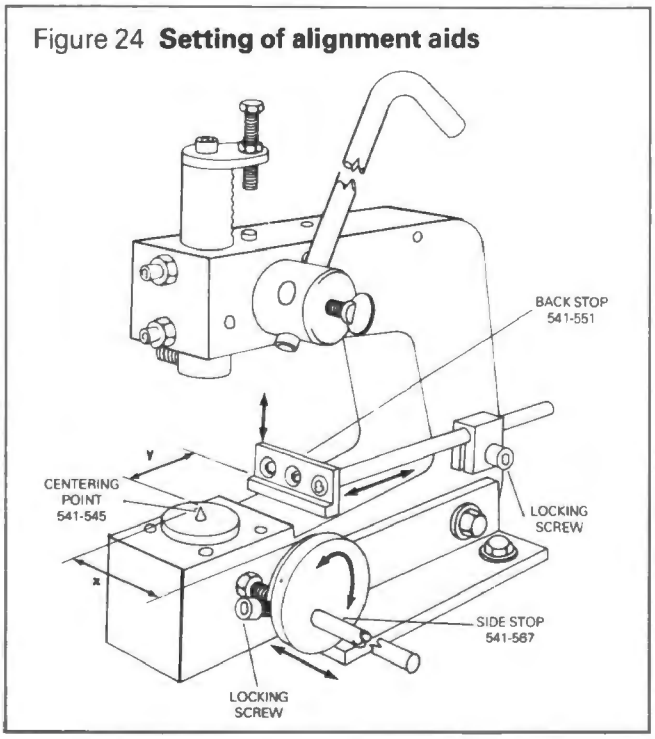
Job alignment aids

Accessories required:

Side stop 541-567
Back stop 541-551
Centering point 541-545

Three alignment accessories for use in conjunction with RS press 541-309 for accurate and repeatable dimensional reference.

Figure 24 **Setting of alignment aids**



Side stop 541-567

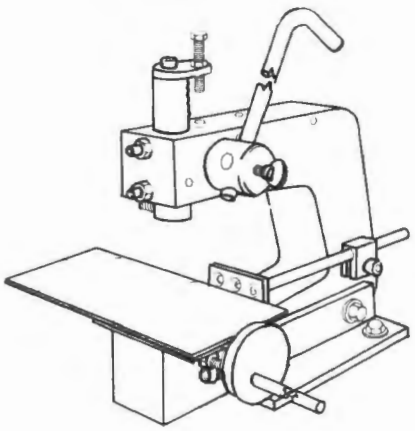
1 Side stop 541-567 can be fitted on either side of the press frame at holes D, see Figure 1, page 1.

2 Consists of a circular shaped stop (with a step rest) mounted 'off centre' to a bar which screws into the press frame with a locknut.

3 The stop slides along the bar to give side reference dimension 'x', see Figure 24, and also revolves on the bar in a cam fashion giving variation in rest height.

4 Fit the stop as shown, tightening the bar locking nut and locking the stop with screw indicated.

Figure 25 **Alignment of workpiece against stops**



5 Maximum range of adjustment from ram centre 41 to 220mm.

6 Maximum vertical adjustment 20mm above the dieholding face.

Back stop 541-551

7 Back stop 541-551 can be fitted to either side of the press frame at holes C, see Figure 1, page 1.

8 Consists of a bar clamp with an 'L' shaped rest.

9 The bar slides in the clamp until it is tightened to give back reference dimension 'y', see Figure 24.

10 The stop can also be moved up and down to give a degree of vertical adjustment.

11 The rest can be screwed to the end of the bar in three positions.

12 Maximum adjustment from ram centre 150mm.

13 With both the stops fitted and set for correct distance and height, sheet material can be positioned for repeated accurate centering. See Figure 25.

Centering point 541-545

14 Consists of a circular plug which fits into the central hole of the press base, having a centre point, which represents the centre line of the ram.

RS data

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An Electrocomponents Group Company
Telephone: 0536 201234
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RS data

Power supply supervisor RS 3543

Stock number 302-687

The RS 3543 is a power supply supervisory i.c. that contains circuits for full monitoring and shutdown control of a single rail supply. Equally suitable for controlling both linear and switch mode power supplies this device can provide valuable protection for both the equipment and power supply. Over-voltage and undervoltage circuits are programmable for minimum fault duration before operation.

Features

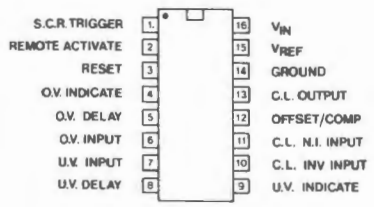
- Over-voltage, under-voltage, and current sensing circuits.
- Voltage reference trimmed to 1% accuracy.
- S.C.R. drive of 300 mA suitable for "Crowbar" operation.
- Programmable time delays.
- Open collector outputs.
- Standby current less than 10 mA.

Absolute maximum ratings

Input supply voltage, V_{IN}	40 V
Sense inputs	V_{IN}
SCR Trigger current	300 mA*
Indicator output voltage	40 V
Indicator output sink current	50 mA
Power dissipation (package limitation)	1000 mW
Derate above 25°C	8.0 mW °C
Operating temperature range	0°C to +70°C
Storage temperature range	–65°C to +150°C

At higher input voltages, a dissipation limiting resistor, R_G is required.

Pin connections



TOP VIEW

Electrical characteristics T_A = 0 to 70°C V_{IN} = 10V unless specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Range	T_J = 25°C to T_{max}	4.5	–	40	V
Input Voltage Range	T_{min} to T_{max}	4.7	–	40	V
Supply Current	T_J = 25°C, V_{IN} = 40V	–	7	10	mA
REFERENCE SECTION (Pins 15,16)					
Output Voltage	T_J = 25°C	2.45	2.50	2.55	V
Output Voltage	Over Temp Range	2.40	–	2.60	V
Line Regulation	V_{IN} = 5 to 30V	–	1	5	mV
Load Regulation	I_{REF} = 0 to 10mA	–	1	10	mV
Short Circuit Current	V_{REF} = 0	12	15	25	mA
Temperature Stability		–	50	–	ppm/°C
SCR TRIGGER SECTION (Pins 1,2,3)					
Peak Output Current	V_{IN} = 5V, R_G = 0, V_O = 0	100	200	400	mA
Peak Output Voltage	V_{IN} = 15V, I_O = 100mA	12	13	–	V
Output Off Voltage	V_{IN} = 40V	–	0	0.1	V
Remote Activate Current	Pin 2 = Gnd	–	0.4	0.8	mA
Remote Activate Voltage	Pin 2 open	–	2	6	V
Reset Current	Pin 3 = Gnd, Pin 2 = Gnd	–	0.4	0.8	mA
Reset Voltage	Pin 3 open, Pin 2 = Gnd	–	2	6	V
COMPARATOR SECTIONS (Pins 4 to 9)					
Input Threshold (Input voltage rising on Pin 6 and falling on Pin 7)	T_J = 25°C	2.40	2.50	2.60	V
	Over Temp. Range	2.35	–	2.65	V
Input Hysteresis		–	25	–	mV
Input Bias Current	Sense input = 0V	–	0.3	1.0	µA
Delay Saturation		–	0.2	0.5	V
Delay High Level		–	6	7	V
Delay Charging Current	V_D = 0V	200	250	300	µA
Indicate Saturation	I_L = –10mA	–	0.2	0.5	V
Indicate Leakage	V_{IND} = 40V	–	0.01	1.0	µA
CURRENT LIMIT SECTION (Pins 10 to 13)					
Input Voltage Range		0	–	(V_{IN} –3V)	V
Input Bias Current	Pin 12 open, V_{CM} = 0V	–	0.3	1.0	µA
Input Offset Voltage	Pin 12 open, V_{CM} = 0V	–	0	15	mV
Input Offset Voltage	10kΩ from Pin 12 to Gnd	70	100	130	mV
CMRR	$0 \leq V_{CM} \leq 12V$, V_{IN} = 15V	60	70	–	dB
AVOL	Pin 12 open, V_{CM} = 0V	72	80	–	dB
Output Saturation	I_L = –10mA	–	0.2	0.5	V
Output Leakage	V_{IND} = 40V	–	0.01	1.0	µA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C	–	5	–	MHz

Figure 1 **Block diagram**

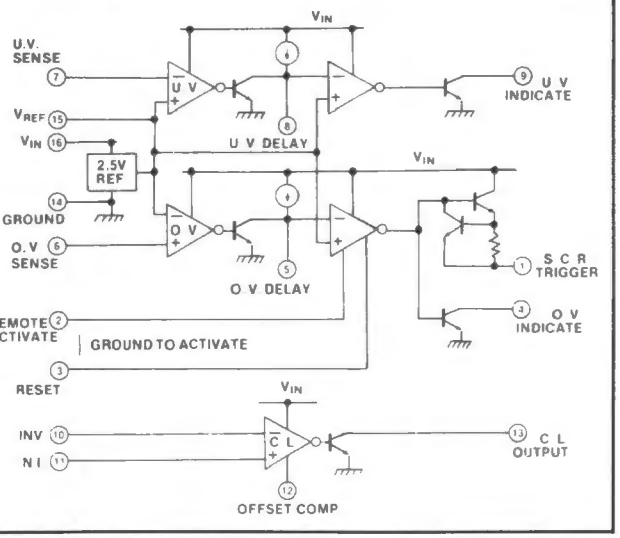


Table 1. **Switching characteristics**

Parameter	Conditions	Typ	Units
SCR TRIGGER SECTION (Pins 1,2,3)			
Output Current Rise Time	R_L =50Ω, T_J =25°C, C_D =0, Pin 2 =0.4V, Pin 6 =2.7V	400	mA μs
Propagation delay, pin 2		300	ns
Propagation delay, pin 6		500	ns
COMPARATOR SECTIONS (Pins 4 to 9)			
Propagation delay	Pin 6 =2.7V, Pin 7 =2.3V, T_J =25°C, C_D =0	400	ns
	C_D =1μ	10	ms
CURRENT LIMIT SECTION (Pins 10 to 13)			
Propagation delay	$V_{overdrive}$ = 100mV, T = 25°C	200	ns

Circuit description

The RS 3543 contains all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown, an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage, and third op amp comparator usable for current sensing (C.I.) are all included in this IC, together with an independent, accurate reference generator.

Both over- and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and reset capability.

The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

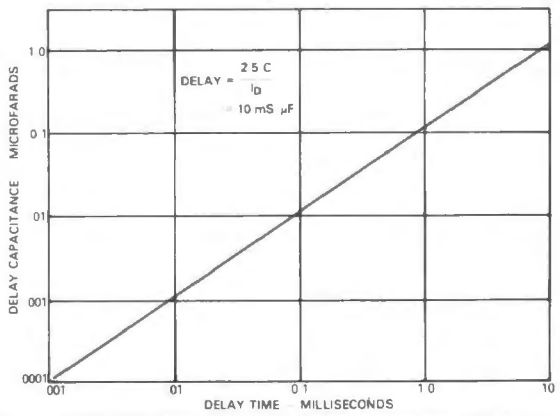
The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

Voltage reference circuit

The 2.50 V reference in the RS 3543 is based on the well-known band gap reference which has the capability of providing a very stable output voltage. The output is nominally set at 2.50 V, but in addition, is trimmed to remove effects of production manufacturing tolerances giving an output voltage accuracy of 1%. Additionally this also trims the temperature coefficient of output voltage to better than 50 parts per million per degree centigrade.

The output of this reference circuit is current limited for protection and will provide up to 10 milliamps of current for use as a reference for other functions that may be required along with the RS 3543. In addition to stable temperature performance, this regulator also maintains its output voltage to within 10mV for all line and load voltages. Additional benefits of the band gap reference circuit include low noise performance, instant turn on and a high degree of long term stabilty.

Figure 2 **Activation delays vs capacitor value**



Comparator section

The over and under-voltage sensing circuits are identical with only the input polarity changed between them. This configuration is made up of two comparators in series, each referenced to 2.50 volts, with the delay terminal at their juncture. Upon sensing an out of tolerance condition the first comparator activates a constant current source of 250μA that charges an externally selected capacitor to provide a delay. The second comparator then activates the output indicating circuit. The overall time delay from input sense to output indicate, with no external capacitor, is approximately 0.5μs. By adding a capacitor this delay is increased by approximately 10 ms per 1μF of capacitance as shown in Figure 2. Since the comparator can discharge in excess of 10 mA, the capacitor is reset in a fraction of its charge time. To eliminate the tendency to oscillate at threshold, a hysteresis of approximately 25 mV is built into the input comparator.

The output indicating transistor is designed to sink 10 mA of current with a saturation voltage of less than 0.4 volt. Its open collector allows several outputs to be connected together to provide a single indicating signal.

SCR Trigger section

While the under-voltage sensing circuit has only the 10 mA, or low current, open collector output, the over-voltage section contains additionally, an SCR crowbar triggering circuit suitable for 300 mA. Since in many cases it is desirable to activate this crowbar during other than over-voltage conditions a remote activation circuit is also included, together with associated reset terminal, which activates the output circuitry in the same manner as the over-voltage comparator.

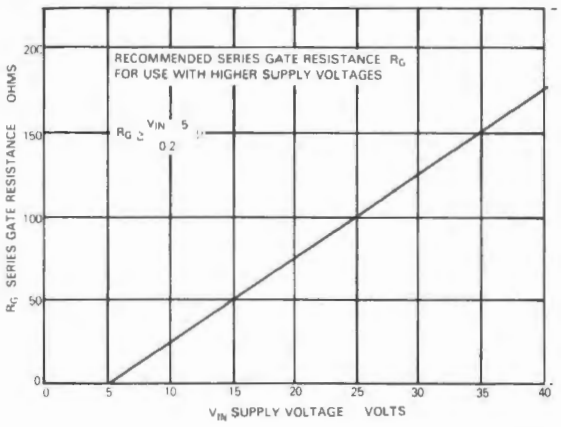
An additional function of this circuit is to provide the capability to latch the outputs on after a fault is sensed, by

externally connecting the over-voltage indicating terminal, pin 4, to the remote activation terminal pin 2. With this configuration, a over-voltage condition will pull pin 4 to ground and hence provide a remote activate signal to pin 2, which, in turn, holds the circuit in the on condition until the reset terminal is externally grounded, removing the latch and turning off the output.

Thresholds for both remote activation and reset terminals are approximately 1.2 volts.

Note. At higher input voltages, a dissipation limiting resistor, RG, is required in series with the SCR gate. The value of RG may be found from Figure 3.

Figure 3 **SCR Trigger power limiting**



Current sensing amplifiers

The amplifier in the RS 3543 designated for current sensing actually has much wider application. It is basically a high-gain, non-compensated operational amplifier with an open collector output, i.e. pull-up on the output must be provided externally. A wide common-mode range extending from slightly below ground to within 2 volts of the supply voltage is made possible by the PNP front end.

With a pull-up resistor of 2 kΩ, the open loop voltage gain is greater than 72 dB with a unity gain bandwidth beyond 5MHz. When used as a comparator, the response time is less than 200 ns, and if linear amplification is required, external compensation may be added for stable performance over a wide frequency range or a unique frequency response.

The input to this amplifier is balanced for zero offset voltage but a fixed offset or threshold of up to 200 mV may be incorporated by adding a resistor, RT, from pin 12 to ground as shown in Figure 5.

Reducing the impedance at pin 12 also lowers the gain of the amplifier as shown in Figure 6. This fact allows pin 12 to do double duty as a point to apply frequency compensation as well with either C1 to the output or C2 to ground.

Figure 4 **Current limit input threshold**

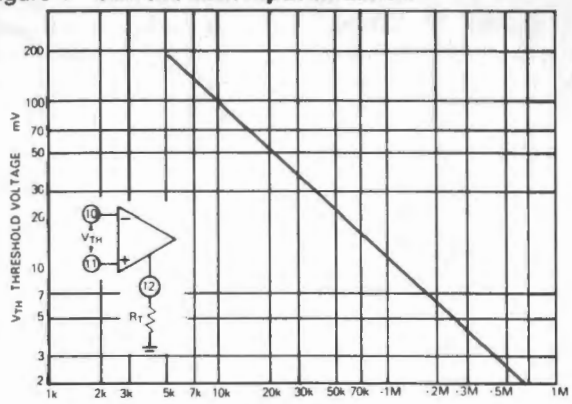


Figure 5 **Current sense compensation**

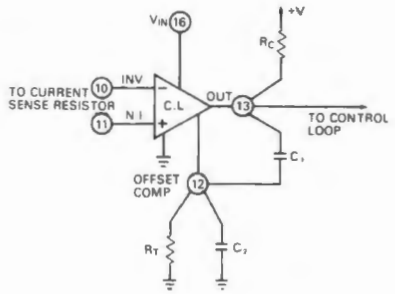


Figure 6 **Current limit amplifier gain**

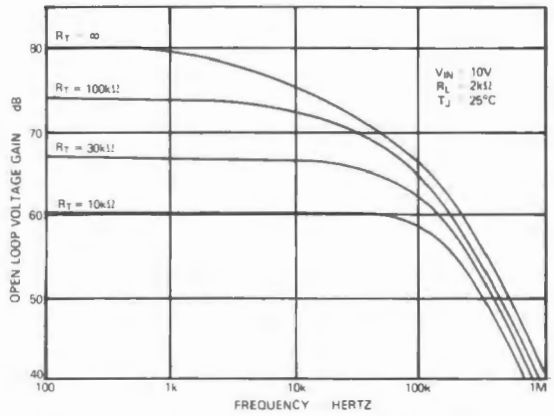
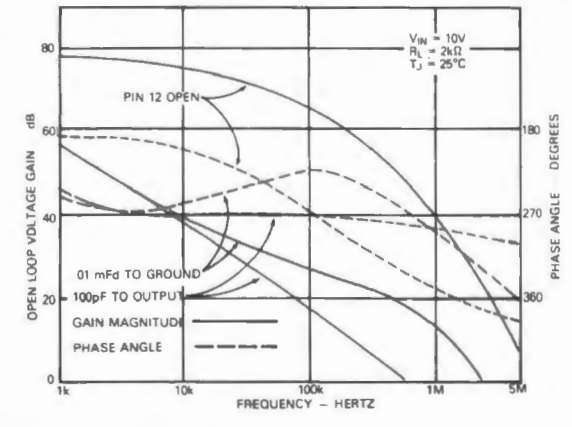


Figure 7 **Current limit amplifier frequency response**

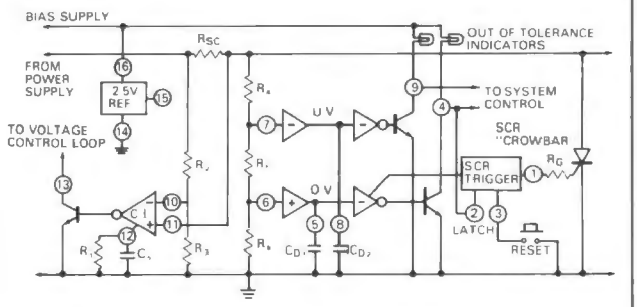


RS data

Typical appplications

Figure 8 shows a typical application of the RS 3543 as used to monitor a single power supply output voltage for both high and low voltage operation as well as current limiting. The data accompanying Figure 8 indicates how the values for the external bias supply which must provide a standby current of 10 mA maximum plus the activation current for the SCR trigger. The application in Figure 8 shows a single resistor divider string, R4, R5 and R6, which sets the thresholds for both the under and over-voltage activating levels. The external capacitors CD1 and CD2 are used to

Figure 8 **Typical monitoring applications**
This typical application for the RS 3543 provides linear foldback current limiting as will as over and under-voltage protection.



provide time delays before activation of the output circuitry. The output of the comparators can be used for many different functions; in this case, they are shown driving indicators. They can also provide signals to the system under power to give information that an out-of-tolerance condition exists. Additionally, by the external connection between pin 2 and pin 4, a latch has been provided such that an over-voltage condition will activate and hold that control signal until positive reset action at pin 3 is performed.

In firing an SCR with supply voltages above 5 volts an external resistor, RG, is used on pin 1 to provide power dissipation limiting for the RS 3543. While the RS 3543 will provide up to 300 mA of trigger current, the power limitation of the 16-pin dual-in-line package should be held to less than one watt.

In this application, current limiting is performed by sensing the current in the positive supply line with fold-back provided by the action of R2 and R3. A fixed threshold for the amplifier is set by R1 which is connected between pin 12 and ground.

Although the RS 3543 could have been driven from the output voltage to be monitored, it would lose control when that output voltage fell to approximately 3 V. This would, of course, preclude the use of the current limit function where short circuit protection must be provided.

The values for the external components used in conjunction with the RS 3543 application of Figure 8 are determined as follows:

Current limit input threshold, $Vth \approx \frac{1000}{R1}$

Cs is determined by the current loop dynamics

Peak current to load, $Ip \cong \frac{Vth}{Rsc} + \frac{Vo}{Rsc}\left(\frac{R2}{R2+R3}\right)$

Short circuit current, $Isc = \frac{Vth}{Rsc}$

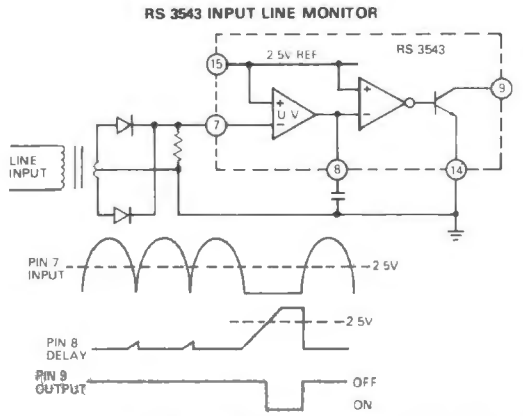
Low output voltage limit, $Vo\ (Low) = \frac{2.5\,(R4+R5+R6)}{R5+R6}$

High output voltage limit, $Vo\ (High) = \frac{2.5\,(R4+R5+R6)}{R6}$

Voltage sensing delay, td = 10,000 Cd

SCR trigger limiting resistor, $Rg > \frac{Vin-5}{0.2}$

Figure 9 **Using the under-voltage sensing circuit**
The under-voltage sensing circuit can be used to monitor the AC input voltage and provide a power failure signal before the power supply output voltage begins to fall.



As shown in Figure 9, the under-voltage circuit can be used to monitor the AC input voltage to a power supply. An isolation transformer and rectifier are used to provide a rectified AC signal to the input of the under-voltage comparator. The signal is compared with the 2.50 V reference, activating the first stage of the comparator with each transition toward zero. With proper selection of the delay capacitor, no output is provided unless some number of input pulses are missing at which time the first comparator allows the charging of the capacitor to 2.50 volts which activates the output circuit. In this way, the under-voltage circuit provides an immediate indication of failure, even for one or two cycles. This provides an early warning indication that the power supply output voltage is going to drop while taking advantage of the holdup capability provided by normal electrolytic capacitor storage within the power supply system.

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RS data

pH Probe and pH buffer powders

Stock numbers 424–557 and 557–045

A standard combination-type pH electrode for general use in determining the acidity or alkalinity of chemical solutions. The design is of the type where the reference electrode is incorporated in the same probe as the main electrode. An electrical output proportional to pH allows its use with an amplifier/meter to form an accurate pH measuring instrument.

A hand held, digital pH meter, suitable for the probe is available, stock number 610-540.

Probe Characteristics

pH range	0 to 14pH
Response time (depending on pH)	Up to 1½ mins
Temperature range	−5 to + 100°C
Lead termination	50Ω b.n.c.
Output voltage (at 7pH)	0mV ± 18mV

IMPORTANT! The probe is despatched with a protective teat, containing 3.8M KCl solution, fitted over the glass membrane and ceramic junction, and a sleeve, sealing the filling aperture. Remove the teat prior to use, and gently shake to allow air bubbles to rise to the top of the probe. Pierce a hole in the sleeve through to the filling aperture. Always store the probe upright in a pH7 buffer solution. **NEVER** allow the ceramic junction to dry out.

pH Measurement

Next to temperature measurement, pH measurement is one of the most widely used in many areas of science. Essentially pH is a measure of the concentration of hydrogen ions in a solution and is effectively a measure of acidity. Absolute measurement of pH and the monitoring of its rate of change are important in chemistry, but pH measurement is also of importance to the food and drink industries, to aquarists, to prolong the life of tropical fish, and to gardeners, where lime is used to control soil acidity and improve plant growth.

pH measurement is also of value in many industrial processes and is also beginning to gain prominence in such areas as colour photography processing.

The value of pH is defined as:

$$pH = \log \frac{1}{[H^+]}$$

$[H^+]$ is the hydrogen ion concentration in the solution.

At ordinary temperatures pure water will slightly dissociate into hydrogen ions and hydroxyl ions:

$$H_2O = H^+ + OH^-$$

Now, the concentration of each type of ion is 10^{-7} gram-molecules per litre, and hence the pH value of pure water is:

$$pH = \log \frac{1}{10^{-7}} = 7$$

This figure is conventionally taken to represent neutrality on the pH scale.

Applications

- Scientific laboratories
- Educational establishments
- Processed food industry
- Drinks industry
- Aquarium monitoring and control
- Agriculture and gardening
- Colour photography processing

If acid is added to water its hydrogen ion concentration increases, and therefore its pH value decreases. Acidity is indicated by pH values below 7, alkalinity by values above 7.

Acid has the effect of liberating hydrogen ions in solution and one of the traditional tests is the use of litmus paper. Acids react with litmus to turn it red, alkalis turn it blue. However, for more accurate measurements, although more precise direct chemical indicators are available, electronic methods are now the accepted norm.

The RS pH meter, stock number 610-540, enables measurement of pH to be made to an accuracy of ±0.03pH. For those wishing to construct their own pH meter, the following circuit is offered. Please note that the following circuit is not that of the RS pH meter, neither is the calibration procedure the same.

Application

A pH probe consists of two electrodes between which a potential difference is generated when they are immersed in the solution under test. The output voltage is, however, quite small, and processing by high impedance amplifiers is necessary. The circuit given is suitable for most applications.

Operational amplifier IC1 forms a unity-gain voltage follower, with a very high input impedance. Amplification is provided by IC2 and is set by VR3. A reference voltage is adjusted by VR4, such that with zero input from the probe a reading of 7.00 is obtained on the panel meter.

Figure 1: **Probe Schematic**

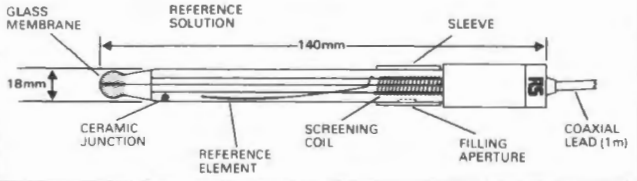
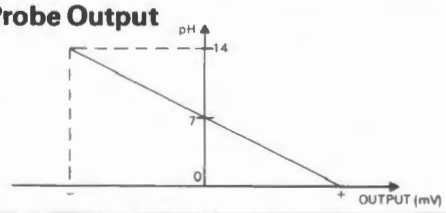


Figure 2: **Probe Output**



RS data

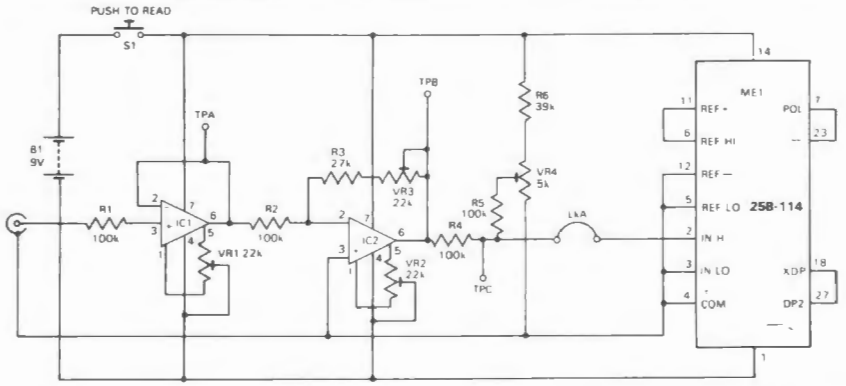
Calibrate as follows:

1. Remove link Lk A.
2. Connect battery.
3. Connect 150mm of wire (insulated) to the meter side of Lk A position. Bare the other end — this acts as a "test prod".
4. Touch "prod" on the "earthy" side of the coaxial input socket. A reading of 0.00 should be obtained.
5. Connect a shorting link to the coaxial socket and touch the "prod" on TP A. Adjust VR1 for a zero reading.
6. Touch "prod" on TP B and adjust VR2 for zero reading.
7. Touch "prod" on TP C and adjust VR4 for a reading of 7.00.
8. Remove the lead and insert Lk A. Remove the socket link and insert the pH probe.
9. Place the pH probe into a neutral solution of pH 7 and adjust VR1 for a reading of 7.00.
10. Place the probe into an acid solution of pH 4. Adjust VR3 for a reading of 4.00. Calibration is now complete.
11. Repeat 9 and 10 as necessary.

NOTE:

The chemicals contained within the probe present no specific hazard, but should not be allowed to come into contact with the mouth or food should the probe be broken or its contents become spilled.

Figure 3: **Circuit for pH Meter**



Note: this is not the circuit of the RS pH meter 610-540 – see text.

R1-6 ¼W carbon film
VR1-4 cermet multi-turn preset
IC1-2 071 (bifet op-amp)

pH Buffer Powders

These Buffer Powders represent an important advance in the preparation of standard solutions since they are accurate and dissolve easily. The pure dry chemicals used are sealed into a laminate of polythene and aluminium foil, which keeps out moisture and gases that can cause deterioration of the buffer powder. For best results a fresh buffer solution should be made up on the day of use.

Directions:

Before opening, the powder must be shaken down to the bottom of the sachet. This may be done conveniently by holding the sachet upright and tapping the bottom edge on a hard surface, i.e., a bench top. Alternatively, the sachet may be held upright and the top flicked with a finger nail. The corner of the sachet should then be cut off and the contents emptied into the vessel used for dissolving the powder. The sachet should be tapped to loosen any powder adhering to the inside. The water should be freshly distilled or demineralised. Distillate from hard water may be heavily contamined with carbon dioxide, which should be removed by aeration or boiling prior to use. An accuracy of 2% in the volume of water used is sufficient.

4pH type (acidic)

Each sachet makes 100 ml. of solution. The pH value is in accordance with NBS specifications i.e. 4.01 ± 0.02 pH at 25°C. pH values at other temperatures are:

°C	0	10	20	25	30	40	50
pH	4.00	4.00	4.00	4.01	4.02	4.04	4.06

°C	60	70	80	90			
pH	4.09	4.13	4.16	4.21			

The solution may be kept for up 2 weeks in a stoppered bottle.

7pH type (neutral)

Each sachet makes 200 ml of solution. The pH value is 7.00± 0.04pH at 25°C pH values at other temperatures.

°C	0	10	20	25	30	40	50
pH	7.11	7.06	7.01	7.00	6.98	6.97	6.97

°C	60	70	80	90			
pH	6.97	6.99	7.03	7.08			

The solution should not be used for calibration after the day on which it is made up, but it may still be used for probe storage.

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Telephone: 0536 201234
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Pyroelectric detectors

Stock numbers 302-592/609/615

The ceramic pyroelectric detectors available in the R5 range (see below) are suitable for many applications, some of which are described in this Data Sheet. Each detector consists of an infrared-sensitive element, a low-noise electrical impedance-matching circuit, and an infrared window, all contained within a TO-5 encapsulation.

The sensitive element is an electrically-polarised ceramic slice, with metallic electrodes deposited on opposite faces. As a result of the pyroelectric nature of the ceramic, an electrical signal is obtained from the electrodes in response to changes in temperature.

Features

Sensitive to changes in 'target' temperature (in field of view).
Can be used in Intruder Alarms
Diverse applications in pyrometry in general.
Industrial uses, including conveyor sorting.
Scientific and Development possibilities embrace spectral analysis and tool control (interference fringe detection).

Absolute maximum ratings

	RPY 89	RPY 95	RPY 96
Storage temperature (°C)	—40 to +50	—20 to +50	—40 to +70
Operating temperature (°C)	—40 to +100	—20 to +50	—40 to +60
Operating voltage (Vdc)	30	30	30

Note: The case potential must not be allowed to become positive with respect to the other two terminals.

Figure 1: **RPY89/RPY96**

RPY89
RPY96

Figure 2: **RPY95**

RPY95

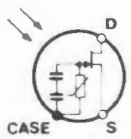
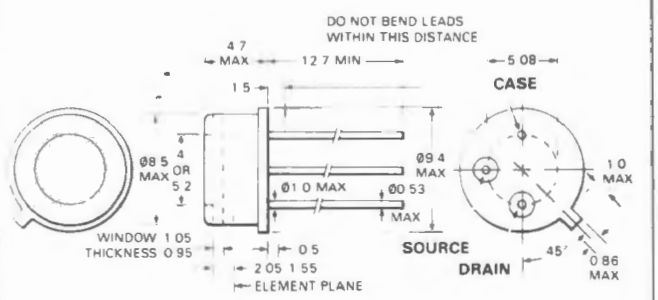


Figure 3: **Outline details**



Dimensions in mm

Product Selection Guide

RS Stock No.	Pro Electron Designation	Number of Elements	Element Spacing (mm)	Element Dimensions (mm)	Spectral Response (μm)	Window Diameter (mm)	Application
302-615	RPY89	1	–	2 x 2	1.0 x 15 (Silicon window)	5.2	General purpose
302-609	RPY95	2	1.0	2 x 1	6.5 to 14 (Daylight filter)	4.0	Intruder alarms
302-592	RPY96	1	–	2 x 1	6.5 to 14 (Daylight filter)	4.0	Intruder detection

Characteristics $T_A = 25°C$

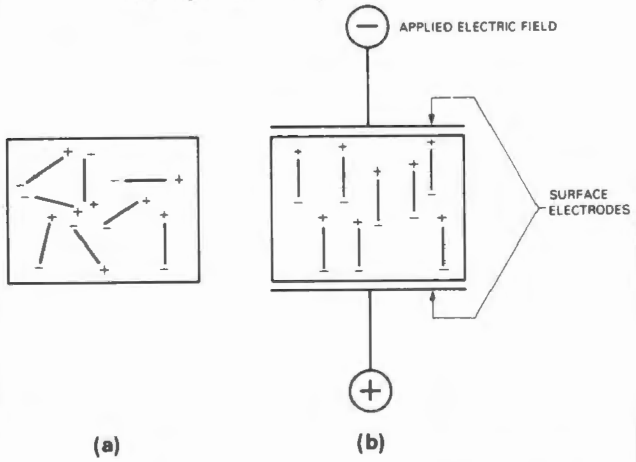
Parameter	RPY89			RPY95			RPY96			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Spectral response	1		15	6.5		14	6.5		14	μm
Responsitivity	188	250		250	450			130		V/W
Noise Equivalent Power (NEP)		2×10^{-9}	3×10^{-9}		2.1×10^{-9}	6×10^{-9}		3.5×10^{-9}	9×10^{-9}	W/Hz
Field of View (FOV)		112			110			105		Degrees
Operating Voltage	8	9	10	8	9	10	8	9	10	V
Frequency Range	01		1000	0.1		1000	0.1		1000	Hz

Pyroelectricity

An explanation of pyroelectricity is given here as a fore-runner to the Design Notes and Applications information.

A pyroelectric ceramic is composed of a mass of minute crystallites, each of which behaves as a small electric dipole. Above a certain temperature, known as the Curie temperature, the crystallites have no dipole moment. Below the Curie temperature, in freshly manufactured material, the electric dipole in each crystallite is oriented randomly with respect to the dipoles in other crystallites (see Figure 4a). If the material is heated to just below the Curie temperature and an electric field is applied to it, the dipoles tend to line up with the applied field (see Figure 4b). After the material has cooled and the applied field has been removed, the dipoles remain in the 'poled' position giving rise to a remanent polarisation of the ceramic. (This is a somewhat simplified explanation that ignores the effect of domains in the crystallites.) To perform the poling process, electrodes are deposited on opposite faces of the material. The charge on the

Figure 4: **Orientation of electric dipoles a) unpoled b) poled**



surface of the ceramic is captive within the lattice structure of the crystallites, but the equal and opposite induced charge on the electrodes is free to move. Thus the electrode which was positive during the poling process acquires a positive charge.

The magnitude of the charge appearing at the surface is related to the internal charges by the 'dipole moment'; that is, the product of charge and separation, as shown in Figure 5. The dipole moment M of the bulk is given by:

$$M = PAd.$$

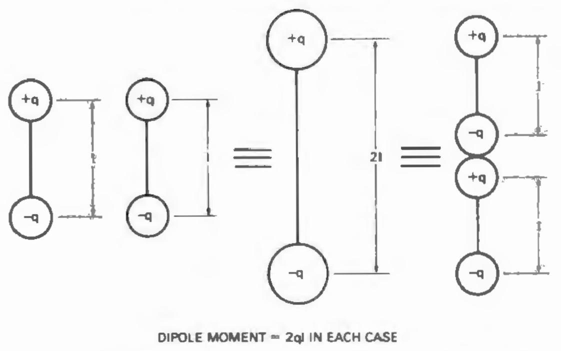
where P is the dipole moment per unit volume, A is the area of an electrode, and d is the separation of the electrodes.

he charge at the surface Q_s has a dipole moment of $Q_s d$. This must equal the total dipole moment, so that:

$$Q_s = PA.$$

The pyroelectric effect arises because of a charge in polarisation with temperature and may occur in several ways. For example, the individual dipoles may shorten with increasing temperature, or the total dipole moment may be reduced by an increase in the randomness of the orientation of the dipoles due to thermal agitation. Thus, when the temperature of the material increases, the captive surface charge is reduced. This leaves a surfeit of induced charge on the electrodes, so that electric potential across the devices rises according to Q = CV (where Q is charge, C is the capacitance, and V is the potential). The excess charge gradually leaks away through the circuit to which the pyroelectric element is connected.

Figure 5: **The same dipole moment resulting from three possible arrangements of dipoles**



The magnitude of the excess charge is related to the pyroelectric coefficient λ which is the rate of charge of polarisation with temperature. As Figure 6 shows, λ is a function of temperature.

For a small temperature change δT, the excess charge δQ is given by:

$$\delta Q = \lambda A \delta T.$$

The charge will give rise to a potential change δV, given by:

$$\delta V = \frac{\delta Q}{C_E} = \frac{\lambda A \delta T}{C_E}$$

where C_E is the electrical capacitance between the surface electrodes.

To maximise the pyroelectric effect in an infrared detector, the sensitive element is made thin. This results in a larger temperature change for the same incident radiation.

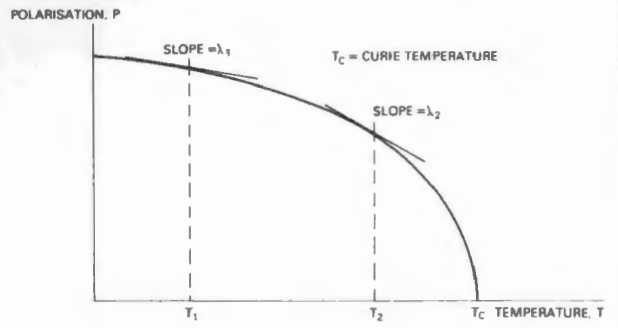
Consider an infrared signal of intensity W watts r.m.s. per unit area whose amplitude varies

sinusoidally at a radial frequency ω. If the thermal capacitance of the sensitive element is C_{th} (JK^{-1}), then, by analogy with electrical theory, the temperature signal δT is given by:

$$\delta T = \frac{WA}{j\omega C_{th}}$$

for all values of $\omega C_{th} R_{th}$ greater than unity, where R_{th} is the thermal resistance. (The value of ω that

Figure 6: **Variation of polarisation with temperature**



equals $1/C_{th}R_{th}$ is termed the thermal break frequency. For the detectors described in this publication $\omega \simeq 1$ Hz.) The temperature signal will give rise to an electrical signal δV given by:

$$\delta V = \frac{\lambda A \delta T}{C_E} = \frac{\lambda A^2 W}{j\omega C_{th} C_E}$$

It can be seen, therefore that the voltage developed decreases as the frequency of the radiation signal increases. Also, the voltage lags the radiation signal by 90° (above the thermal break frequency). The signal current i available into a short-circuit is given by:

$$i = \delta V j\omega C_E, \quad = \frac{\lambda W A^2}{C_{th}}$$

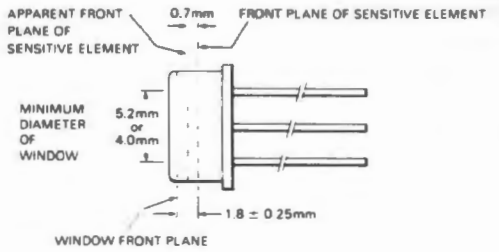
which is independent of frequency and in phase with the incident radiation. The pyroelectric element is of necessity a high-resistivity insulator, so that the dominant noise source at low noise frequencies is the current noise of the amplifier. Therefore, the ratio of signal current to noise current is independent of frequency until the point at which other noise mechanisms predominate.

Device construction

The encapsulation is a low-profile T0-5 type fitted with an infrared window as shown in Figure 7. Two types of window are available: either silicon, with a substantially flat transmission over the wavelength range from 1 μm to beyond 15 μm; or a 'daylight' filter, which transmits in the narrower range 6.5. μm to greater than 14 μm (thereby making the device insensitive to short-wavelength infrared, as emitted by the sun). A practical point to note is that because the window material has a high refractive index, the apparent position of the front plane of the sensitive element is moved 0.7 mm towards the window front plane (as shown in Figure 7).

The detectors contain either a single or dual pyroelectric element, and electrically each device can be represented by one or two capacitors, an

Figure 7: **Section through a ceramic pyroelectric detector**



n-channel FET, and a non-linear network, connected as shown in Figures 1 and 2. The non-linear network contributes greatly to the usefulness of the detectors: it protects the gate of the FET (which forms part of the impedance-matching circuit) from excessive negative voltages, and progressively limits the pyroelectric voltage resulting from large changes in the ambient temperature. Thus, signals may be obtained under conditions which would otherwise either overload the preamplifier or require it to have a very large dynamic range.

The dual-element devices have two differentially-connected sensitive areas with a single impedance-converting amplifier to provide immunity from common mode signals such as those generated by variations in ambient temperature, background radiation, and acoustic noise.

The pyroelectric ceramic material, a lead zirconate titanate, is doped so as to optimise the properties required for infrared detectors. It is insensitive to water and is extremely rugged. Thus it can be handled by mass-production techniques similar to those used in the manufacture of conventional semiconductor devices.

Design notes

Preamplifier

Each detector includes a low-noise FET with its source and drain brought out to external connections (Figures 1 and 2). This allows a great deal of freedom in the design of the preamplifier to match the sensitive element to subsequent amplifiers.

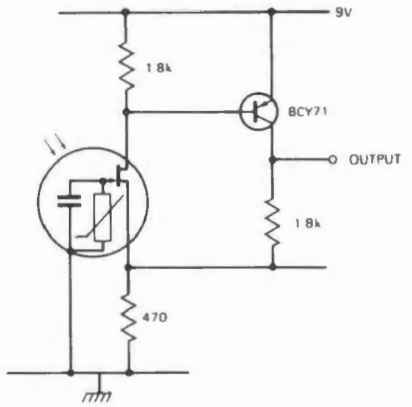
The recommended preamplifier (shown in Figure 8) is the configuration which is the least dependent on the FET characteristics. It has a gain of 4.8, set by the 1.8 kΩ and 470Ω resistors connected to the source. The noise level at the output is typically 250nVHz$^{1/2}$ at 10 Hz and the output impedance is approximately 200 Ω. The d.c. output, with zero input, will lie between 2 and 7 V. This spread is the main reason for limiting the gain, although higher gains can be achieved if the resistors are selected to match each FET. The gain provided by this amplifier is important where low noise is necessary, since the noise introduced by subsequent standard operational amplifiers would otherwise prove obtrusive.

Amplifier

If the amplifier stages subsequent to the preamplifier are to increase the noise level by less than one-third of the preamplifier output noise; that is, their input noise should be less than 80 nVHz$^{-1/2}$ (approximately one-third of 250 n VHz$^{-1/2}$) at 10 Hz.

Various operational amplifiers may be employed. In fact the ubiquitous 741 op amp typically has a noise level of 70VHz$^{-½}$. Depending on the particular circuit requirements an amplifier with or without external compensation may be chosen.

Figure 8: **Recommended preamplifier**



If the system design can tolerate some degradation in the overall signal-to-noise ratio, a wide range of operational amplifiers can be considered. A particularly useful device is the 324, a quad operational amplifier, which is ideally suited to single-supply operation.
The typical voltage noise for the 324 is 170 n VHz$^{-½}$ at 10Hz. With four independent amplifiers in a single package, this device provides a compact and economical solution to a variety of application problems. The use of the RS 741N (low noise version of the 741) should also be considered.
However, it should not be forgotten that the input bias current should preferably be as low as possible, say less than 100nA. Also, it must be kept in mind that, since time-constants for the circuits are generally large, low-leakage capacitors must be employed.

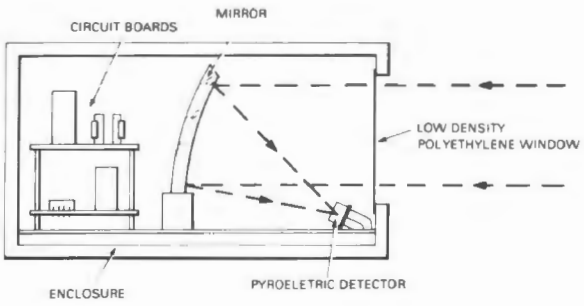
Applications.

The pyroelectric element will only produce an output signal if the flux of infrared radiation incident on it changes. This may be achieved either by moving the object of interest into and out of the field of view, or by interrupting the radiation incident on the detector. Both methods are used in the following applications.

Intruder alarm

To detect an intruder within the area protected by the field of view of the alarm, use is made of the intruder's movement to cause a change in the radiation reaching the detector. The circuit is designed so as to require two or more signals to exceed a preset threshold within a defined time, thus reducing the possibility of false alarms.
One arrangement of an alarm is shown in Figure 9. Infrared lenses tend to be expensive, and as a consequence the alarm employs a relatively inexpensive moulded plastic mirror. However, the surface quality of the mirror is important, especially for dual-element detectors which require a well-focused image to achieve maximum sensitivity. A horizontal section through the mirror is shown in Figure 10. The mirror is constructed from five segments, each being an off-axis section from a sphere of radius 80 mm. The segments are mounted on a circle of radius 40 mm so that their foci are coincident. With this type of off-axis design, the detector can be mounted at the focus without obscuring the field of view. Five images of the detector are projected on to the protected area, ensuring the necessary multiple triggering of the alarm. It is possible to increase the number of facets up to twenty in any one plane (the limit being set by the detector field of view of 112° for a 5.2 mm aperture window) and rows could be added above and below to increase coverage in the vertical direction.
The recommended detectors are those which do not respond to wavelengths below μm. Therefore, the major part of the radiation from the sun is not sensed so that an intermittently illuminated background will not trigger the alarm. The dual-element type RPY95 has been designed specifically for intruder alarm applications, the differential connections of the elements minimising the risk of false alarms caused by environmental effects.

Figure 9: **Prototype intruder alarm**

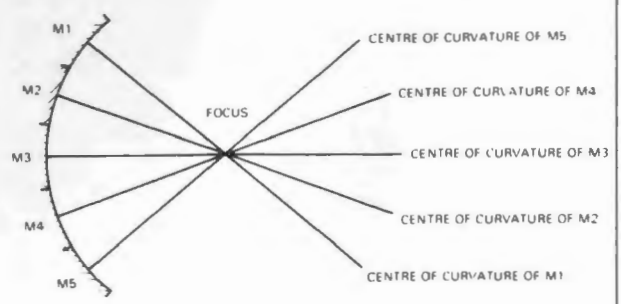


The detector and mirror are housed in an enclosure that has an infrared window made from low-density polyethylene sheeting, which transmits 95% of the radiation in the range of interest. (Plastic 'bin liner' material is often a good substitute.) False triggering effects caused by the thermally-induced motion of the atmosphere are thus minimised.
If, for example, a man in shirt sleeves enters the field of view up to 30 m from the detector, this combination of optics and detector is sufficiently sensative to trigger the alarm circuit.

Practical alarm circuit

The alarm circuit shown in Figure 11 utilises a simple single-shot threshold detector as a trigger.

Figure 10: **Section through multi-faceted mirror**



Some adjustment of sensitivity can be achieved by varying R_{13}. The use of a dual-element detector provides some degree of false alarm immunity; however, this could be further improved by adopting a more sophisticated double-pulse triggering technique. Note, however, that the circuit will work with the single-element devices.

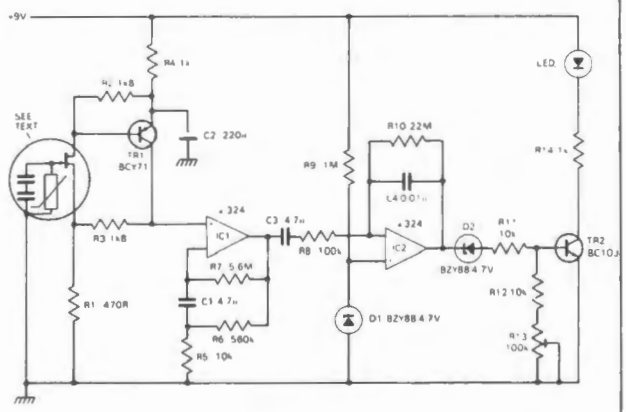
Further application ideas

These ideas are given as a guide to the general possibilities of pyroelectric detectors, circuits or guarantees that they will prove satisfactory cannot be supplied.

Staircase light-switch

The alarm circuit described above can be used to sense the presence of someone in a dark corridor or staircase, and then to switch on the lighting. The circuitry can be simplified, if required, as the possibility of false triggering is normally unimportant. The addition of a light-level sensor and a delay switch will provide a fully automatic system. The same principle may be applied to switch off lighting, heating, etc. when a room (e.g. in a hotel) is unoccupied.

Figure 11: **Circuit of low-cost intruder alarm**



NOTE. R4 may be shorted out in some applications and R2 may be selected around 1k8 for optimum performance

Fire alarm

The detectors can also find application in fire alarm systems. The flickering nature of a flame and hot gases provide the necessary modulation of the infrared radiation received by the detector. Since flames are copius sources of infrared energy, the use of collecting optics is unnecessary.
The false immunity of such detector systems can be greatly improved by using a window with a narrow bandpass characteristic which restricts incoming radiation to a specific wavelength.

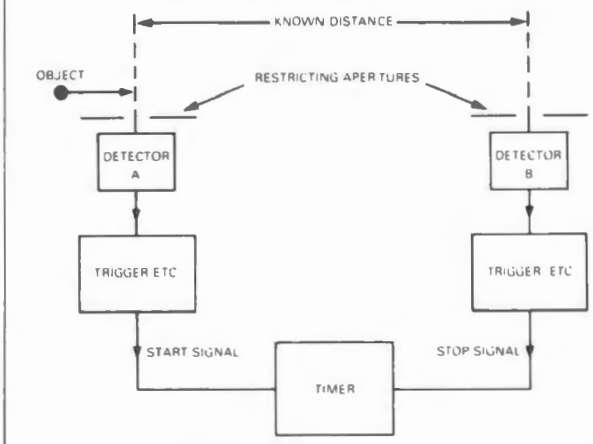
Speed indicator

The detectors can be used for speed measurement. Two detectors are separated by a known distance and each is connected to a circuit consisting of preamplifier, amplifier, and trigger (see Figure 12). The speed of an object moving past the detectors is measured by determining the time between signals from two circuits. (As an alternative to the use of two detectors, a single detector may be used in conjunction with a beam splitter.)

Sorter

The detectors can be employed to sort objects with different temperatures, emissivities, thermal conductivities, or radiation transmission. For example, identical objects on a conveyor belt can be made to pass across the field of view of a detector. The magnitude of the output signal from the detector will be a measure of the temperature of each object with respect to the background. The output signal can control an accept/reject mechanism. A similar technique can be used to mark material in a continuous strip process.

Figure 12: **Speed measurement with two detectors**



Simple radiometer

A simple radiometer may be constructed by placing a mechanical chopper in front of the detector and defining the field of view with an aperture. The signal S from the detector is given by:

$$S = ß\,(e_2T_2^4 - e_1T_1^4),$$

where e_1 is the emissivity of the chopper blade, T_1 is its temperature (in kelvin), e_2 is the emissivity of the target, T_2 is the temperature of the target, and ß is a constant. Variations in T_1 can be compensated by using a linear temperature transducer. A calibrated gain control can be used to allow for variations in emissivity of the target.

Radiometer with compensation for target emissivity
A radiometer that eliminates errors due to variations in target emissivity can be constructed. The target radiation is split into two spectral regions using filters and the radiation from each spectral region is allowed to fall alternatively on to the detector. The ratio of the two output signals from the detector depends only on the temperature of the target. The radiation from the target must be chopped prior to filtering in order that the radiation emitted by the filter can be eliminated as a source of error.

Simple switch
A circuit may be constructed to detect, for example, the presence of a human hand nearby, and thus be used as a proximity switch.

Applications using choppers with collecting optics

Radiometer
The use of collecting optics will increase the radiation energy incident on a detector, in the ratio of the area of the collecting aperture to the area of the sensitive element in the detector. As a result, the temperatures of areas of a remote control radiant object can be measured (if its emissivity is known). The area of the distant object observed is defined by the image of the sensitive element in the collecting optics.

Level sensor
A dual-element detector can be used with a chopper and focused optical system to form a level sensor capable of the remote detection of small temperature discontinuities. A practical application for such an instrument is in the detection of solid or liquid levels in vertical storage tanks and silos. In containers of this type, there is usually a temperature difference between the full and empty parts of the tank. By employing a dual-element detector (elements in series opposition) and a chopper blade which simultaneously masks and exposes both elements; a difference signal is produced. The instrument can thus be used to scan a field of view and produce a maximum difference signal at the level discontinuity.

Spectral analysis
The ceramic pyroelectric detectors may be used in infrared spectrometers. However, the noise equivalent power is a factor of ten higher than that of a Golay cell. Therefore, the bandwidth of the instrument would need to be reduced by 100 times to achieve the same resolution. Some bandwidth, and hence speed, can be recovered by controlling the charts speed so that the writing speed is maintained constant. The lower resolution and speed would, however, probably be acceptable in spectrometers intended for teaching applications.

Gas analysis
The presence of some gases can be detected by the amount of infrared radiation that they absorb at characteristic wavelengths. To detect a particular gas, infrared radiation at the characteristic absorption wavelength of that gas (the radiation is selected by narrowband filters) is passed through a reference chamber, which does not contain the gas, and a sample chamber. The relative transmission of infrared radiation through the two chambers is a measure of the amount of the sought-after gas. The absorption of the gas is likely to be small, so that a long radiation path-length will be needed for a high sensitivity. The long path-length can be accommodated in a small space by the use of multiple reflection between mirrors. This type of system can be used to detect alcohol in the breath ('breathalyser'), and to analyse industrial pollution and car exhaust gases.

Machine tool control
These detectors are sufficiently rugged to allow them to be used in the control of machine tools. A control system might use a detector to count the passage of inteference fringes that are made to move as the work piece or tool is moved. The distance travelled by the work piece or tool is related to the fringe count and the wavelength of the infrared radiation.

General recommendations for the use of Ceramic Pyroelectric Infrared Detectors

1) Care should be taken to avoid damage to or contamination of the window. Finger grease in particular is very difficult to remove and will adversely affect the transmission properties. Solvents other than water should not be used for cleaning windows.

2) The printed circuit board and socket in the neighbourhood of the preamplifier and detector should be thoroughly cleaned. Also, all components should be low-noise or low-leakage types to ensure the best possible performance.

3) The material is inherently piezoelectric as well as pyroelectric. That is, it will produce an electrical output if it is stressed, for example by vibration (mechanical microphony). However, this effect is likely to be small compared with the output signal produced by the variations in the incident radiation flux if the detector vibrates in a non-uniform radiation field (optical microphony). It is therefore important that the detector should be securely mounted, preferably in a standard TO-5 socket.

4) If the detector is to be soldered directly on to a printed circuit board, the leads should not be bent within 1.5mm of the header. This will prevent damage to the glass-to-metal seals in the header. The use of a heat-shunt is recommended during soldering.

5) The case must never be positive with respect to the source or drain terminals, since this is likely to damage the FET.

6) The detector is quite capable of operating at audio frequencies. Although the voltage signal decreases as frequency increases, the noise also decreases (but at a slower rate). The detector may work at higher frequencies still if the radiation is very intense. One obvious precaution is never to operate at mains related frequencies, unless special screening techniques are used.

7) For frequencies greater than the thermal break frequency (1Hz) the output waveform will be triangular for an incident squarewave radiation signal. If necessary, the squareness may be restored by differentiation.

8) The radiation from chopper blades must be subtracted when determining the temperature of a target in the field of view of a pyrometer. This is most important when there is little difference between the chopper and target temperatures.

9) The radiation from the background within the spectral range of the detector should not change within the electrical passband of the system.

10) The 'daylight' filter, fitted to the RPY95 and RPY96, prevents the passage of most of the radiation from a black-body source with its peak emission in the visible region. It blocks visible and short-wavelength infrared radiation but allows the majority of long-wavelength infrared radiation to pass.
The silicon window, fitted to the RPY89, prevents the passage of visible radiation but not short or long wavelength infrared radiation.

11) It is inadvisable to chop radiation on the detector side of the restricting aperture because this will cause an unwanted, modulated signal due to hot-spots within the detector field of view.

12) In a system operating at very low frequencies, air movement in the line of sight of a detector can cause unwanted signals. If the detector is enclosed in a box with an infrared window, air movement close to the detector is reduced. As a result the effect is much diminished.

Typical performance curves

Figure 13: **Responsivity vs. Frequency**

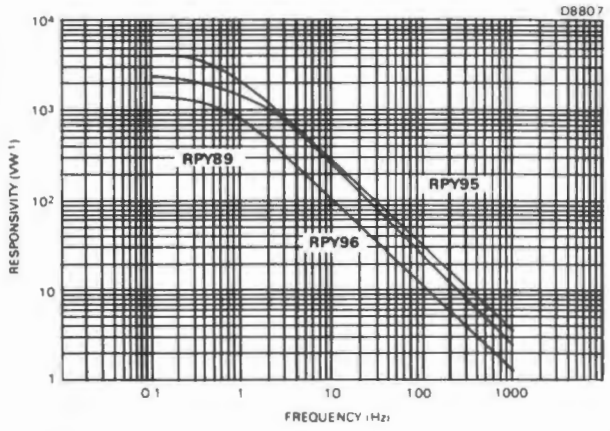


Figure 14: **N.E.P. vs. Frequency**

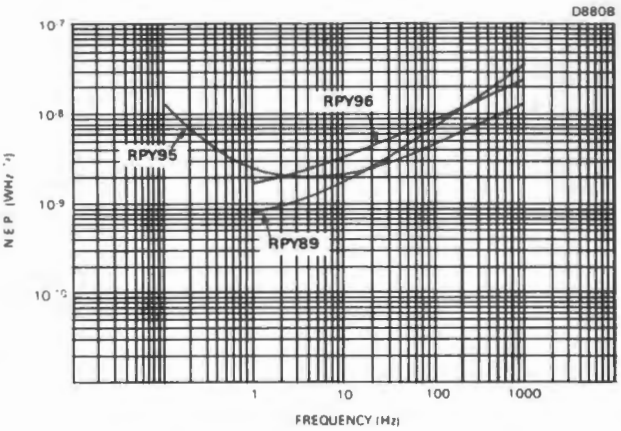
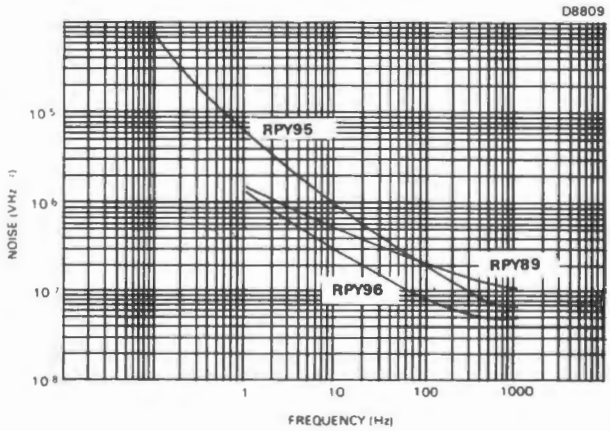


Figure 15: **Noise vs. Frequency**



RS data

Figure 16: **Responsivity vs. Temperature**

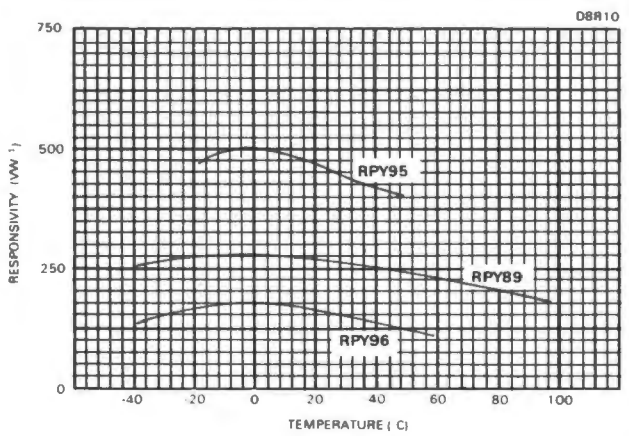


Figure 17: **N.E.P. vs. Temperature**

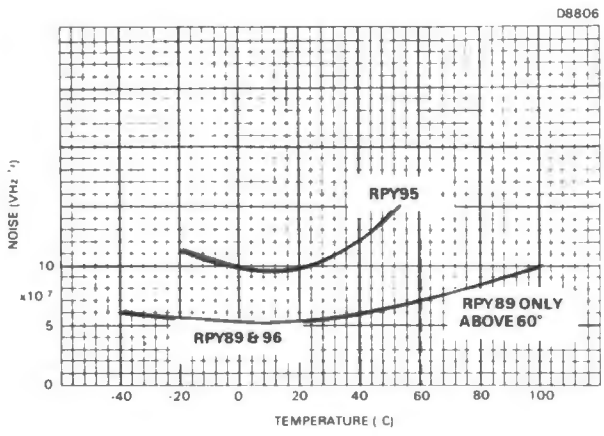


Figure 18: **Noise vs. Temperature**

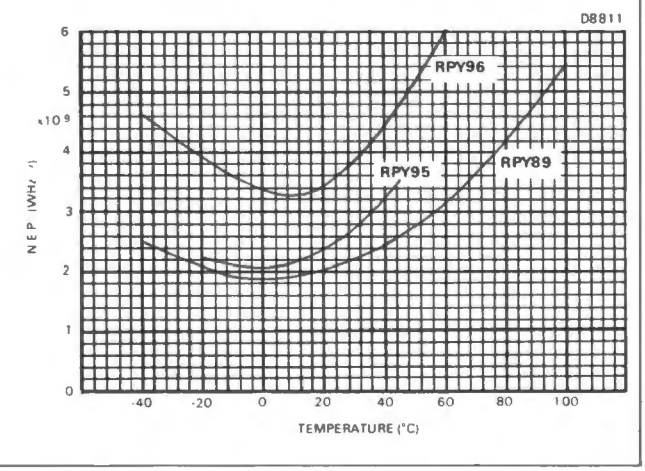
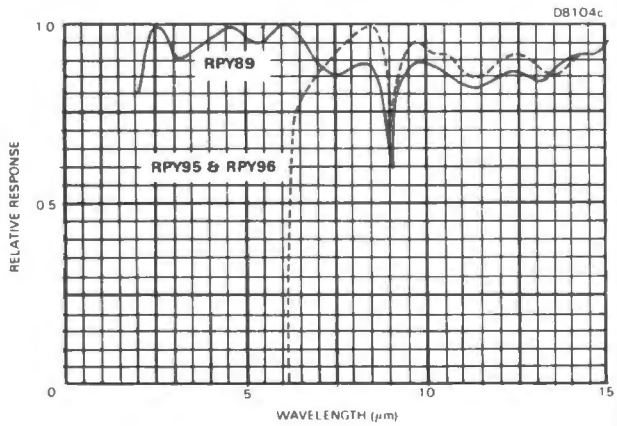


Figure 19: **Typical window transmission characteristics**



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Telephone: 01-250 4000

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RS data

Opto-isolators 6N136, Dual 6N136, 6N139, Dual 6N139, HCPL 3700, HCPL 2601

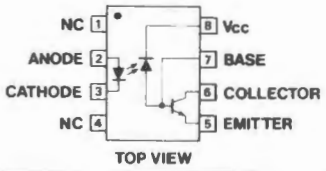
Stock numbers 303-141, 302-097, 303-135, 302-110, 303-113/129

Each of the opto-isolators described in this Data Sheet are recognised 'industry-standard' devices, and each type has its own place in circuit design for achieving solutions in the fields of isolation and coupling. All types come in the popular 8-pin dual-in-line pack and have the advantage of a 3000 V d.c. Withstand Test Voltage.

Pin-out diagrams

6N136

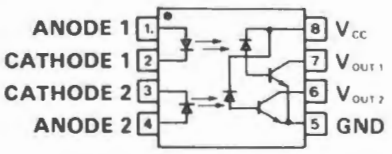
303-141



TOP VIEW

Dual 6N136 (HCPL 2531)

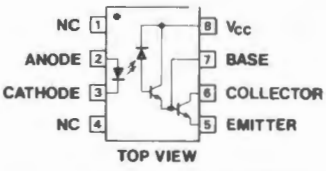
302-097



TOP VIEW

6N139

303-135



TOP VIEW

Features

6N136 type
- General use
- Medium speed (1 Mbit/s NRZ)

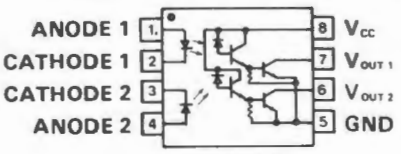
6N139 type
- High sensitivity (0.5 mA)
- High transfer ratio (400%)
- 300 kbit/s data rate (NRZ)

HCPL 3700
- a.c. type
- 'μP' interfaces

HCPL 2601
- Shielded construction
- High common mode transient rejection
- 700% transfer ratio
- 10 Mbit/s data rate (NRZ)

Dual 6N139 (HCPL 2731)

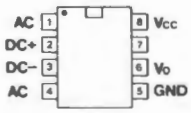
302-110



TOP VIEW

HCPL 3700

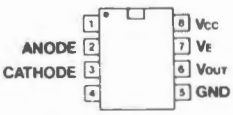
303-113



TOP VIEW

HCPL 2601

303-129



TOP VIEW

Absolute maximum ratings

Parameter	6N136	Dual 6N136	6N139	Dual 6N139	HCPL3700	HCPL2601	Units
Storage temperature	–55 to + 125	–55 to + 125	–55 to + 125	–55 to + 125	–55 to + 125	–55 to + 125	°C
Operating temperature	–55 to + 100	–55 to + 100	0 to + 70	–40 to + 85	–25 to + 85	0 to + 70	°C
Lead solder temperature	260 (10 secs)	260 (10 secs)	260 (10 secs)	260 (10 secs)	260 (10 secs)	260 (10 secs)	°C
Diode maximum forward current	25 (note 1)	25 (note 1)	20 (note 4)	20 (note 13)	50 (note 8)	20	mA
Diode maximum reverse voltage	5	5	5	5	–	5	V
Output circuit: Max. V_{CC}	15	15	18	18	20	7	V
Input power dissipation	45 (note 2)	45 (note 12)	35 (note 5)	35 (note 14)	230 (note 9)		mW
Output power dissipation	100 (note 3)	35 (note 12)	100 (note 6)	100 (note 15)	210 (note 10)	40	mW
Maximum output current	8	8	60 (note 7)	60 (note 16)	30 (note 11)	25	mA

Notes: (see page 1)

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.
4. Derate linearly above 50°C free-air temperature at a rate of 0.4 mA/°C.
5. Derate linearly above 50°C free-air temperature at a rate of 0.7 mW/°C.
6. Derate linearly above 25°C free-air temperature at a rate of 2.0 mW/°C.
7. Derate linearly above 25°C free-air temperature at a rate of 0.7 mA/°C.
8. Measured at a point 1.6 mm below seating plane.
9. Derate linearly above 70°C free-air temperature at a rate of 4.1 mW/°C.
   Maximum input power dissipation of 230 mW allows an input IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA} = 240° C/W. Excessive P_{IN} and T_J may result in IC chip degradation.
10. Derate linearly above 70°C free-air temperature at a rate of 3.9 mW/°C. Maximum output power dissipation of 210 mW allows an output IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA_0} = 265° C/W. Total package dissipation should not exceed 305 mW
11. Derate linearly above 70°C free-air temperature at a rate of 0.6 mA/°C.
12. Derate linearly above 70°C free-air temperature at a rate of 1.0 mW/°C.
13. Derate linearly above 50°C free-air temperature at a rate of 0.5 mA/°C.
14. Derate linearly above 50°C free-air temperature at a rate of 0.9 mW/°C.
15. Derate linearly above 35°C free-air temperature at a rate of 1.7 mW/°C.
16. Derate linearly above 35°C free-air temperature at a rate of 0.6 mA/°C.

Electrical characteristics: 6N136 type T_A = 0 to 70°C (Typical values at 25°C) unless specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Current Transfer Ratio	CTR	I_F = 16mA, V_O = 0.4V, V_{CC} = 4.5V, T_A = 25°C	19	24		%	1
		I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V	15	21		%	
Logic Low Output Current	V_{OL}	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V		0.1	0.4	V	
Logic High Output Current	I_{OH}	I_F = 0mA, V_O = V_{CC} = 5.5V, T_A = 25°C		3	500	nA	
		I_F = 0mA, V_O = V_{CC} = 15V, T_A = 25°C		0.01		μA	
		I_F = 0mA, V_O = V_{CC} = 15V			50	μA	
Logic Low Supply Current	I_{CCL}	I_F = 16mA, V_O = Open, V_{CC} = 15V		60		μA	
Logic High Supply Current	I_{CCH}	I_F = 0mA, V_O = Open, V_{CC} = 15V, T_A = 25°C		0.02	1	μA	
		I_F = 0mA, V_O = Open, V_{CC} = 15V			4	μA	
Input Forward Voltage	V_F	I_F = 16mA, T_A = 25°C		1.5	1.7	V	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	I_F = 16mA		−1.6		mV/°C	
Input Reverse Breakdown Voltage	BV_R	I_R = 10μA, T_A = 25°C	5			V	
Input Capacitance	C_{IN}	f = 1MHz, V_F = 0		60		pF	
Input-Output Insulation Leakage Current	I_{I-O}	45% Relative Humidity, t = 5s, V_{I-O} = 3000Vdc, T_A = 25°C			1.0	μA	2
Resistance (Input-Output)	R_{I-O}	V_{I-O} = 500V dc		10^{12}		Ω	2
Capacitance (Input-Output)	C_{I-O}	f = 1MHz		0.6		pF	2
Transistor DC Current Gain	h_{FE}	V_O = 5V, I_O = 3mA		175		—	

Switching characteristics: 6N136 type T_A = 25°C, V_{CC} = 5V, I_F = 16mA, unless specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Propagation Delay Time to Logic Low at Output	t_{PHL}	R_L = 1.9kΩ		0.2	0.8	μs	4,5
Propagation Delay Time to Logic High at Output	t_{PLH}	R_L = 1.9kΩ		0.3	0.8	μs	4,5
Common Mode Transient Immunity at Logic High Level Output	CM_H	I_F = 0mA, V_{CM} = $10V_{p-p}$, R_L = 1.9kΩ		1000		V/μs	3, 4, 5
Common Mode Transient Immunity at Logic Low Level Output	CM_L	V_{CM} = $10V_{p-p}$, R_L = 1.9kΩ		−1000		V/μs	3, 4, 5
Bandwidth	BW	R_L = 100Ω		2		MHz	6

Notes: 6N136

1. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.
3. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
4. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
5. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
6. The frequency at which the a.c. output voltage is 3 dB below the low frequency asymptote.

Electrical characteristics: 6N139 type T_A = 0 to 70°C (Typical values at 25°C) unless specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Current Transfer Ratio	CTR	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	400 500	900 1000		%	1,2
Logic Low Output Voltage	V_{OL}	I_F = 1.6mA, I_O = 6.4mA, V_{CC} = 4.5V I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V		0.1 0.1 0.2	0.4 0.4 0.4	V	2
Logic High Output Current	I_{OH}	I_F = 0mA, V_O = V_{CC} = 18V		0.05	100	μA	2
Logic Low Supply Current	I_{CCL}	I_F = 1.6mA, V_O = Open, V_{CC} = 5V		0.2		mA	2
Logic High Supply Current	I_{CCH}	I_F = 0mA, V_O = Open, V_{CC} = 5V		10		nA	2
Input Forward Voltage Input Reverse Breakdown Voltage	V_F B_{VR}	I_F = 1.6mA, T_A = 25°C I_R = 10μA, T_A = 25°C	 5	1.4	1.7	V V	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	I_F = 1.6mA		−1.8		mV/°C	
Input Capacitance	C_{IN}	f = 1 MHz, V_F = 0		60		pF	
Input-Output Insulation Leakage Current	I_{I-O}	45% Relative Humidity, T_A = 25°C t = 5 s, V_{I-O} = 3000Vdc			1.0	μA	3
Resistance (Input-Output)	R_{I-O}	V_{I-O} = 500Vdc		10^{12}		Ω	3
Capacitance (Input-Output)	C_{I-O}	f = 1MHz		0.6		pF	3

Switching characteristics: 6N139 type T_A = 25°C

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Propagation Delay Time To Logic Low at Output	t_{PHL}	I_F = 0.5mA, R_L = 4.7kΩ I_F = 12mA, R_L = 270Ω			100 2	μs	2,4
Propagation Delay Time To Logic High at Output	t_{PLH}	I_F = 0.5mA, R_L = 4.7kμ I_F = 12mA, R_L = 270Ω		1	60 10	μs	2,4
Common Mode Transient Immunity at Logic High Level Output	CM_H	I_F = 0mA, R_L = 2.2kΩ, R_{CC} = 0 $\lvert V_{cm} \rvert$ = $10V_{p-p}$		500		V/μs	5,6
Common Mode Transient Immunity at Logic Low Level Output	CM_L	I_F = 1.6mA, R_L = 2.2kΩ, R_{CC} = 0 $\lvert V_{cm} \rvert$ = $10V_{p-p}$		−500		V/μs	5,6

Notes: 6N139 type

1. D.C. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. 'Base' not connected.
3. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.
4. Use of a resistor between Pin 5 and 7 will decrease gain and delay time for the 6N139.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
6. In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is:

$$R_{CC} \approx \frac{1\,V}{0.15\,I_F\,(mA)}\ k\Omega.$$

WARNING!

ESD SENSITIVE DEVICE

Caution: Types 6N136 and 6N139 (and dual version)

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Electrical characteristics: HCPL 3700 T_A = 0 to 70°C (unless specified.[2])

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Input Threshold Current	I_{TH+}	$V_{IN} = V_{TH+}$; V_{CC} = 4.5V; V_O + 0.4V; $I_O \geq$ 4.2mA	1.96	2.5	3.11	mA	7
	I_{TH-}	$V_{IN} = V_{TH-}$; V_{CC} = 4.5V; V_O = 2.4V; $I_{OH} \leq$ 100 µA	1.00	1.3	1.62	mA	7
Input Threshold Voltage DC (Pins 2, 3)	V_{TH+}	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open; V_{CC} = 4.5V; V_O = 0.4V; $I_O \geq$ 4.2mA	3.35	3.8	4.05	V	7
	V_{TH-}	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open; V_{CC} = 4.5V; V_O = 2.4V; $I_O \leq$ 100µA	2.01	2.6	2.86	V	7
AC (Pins 1, 4)	V_{TH+}	$V_{IN} = V_1 - V_4$; Pins 2 & 3 Open; V_{CC} = 4.5V; V_O = 0.4mA; $I_O \geq$ 4.2mA					
	V_{TH-}	$V_{IN} = V_1 - V_4$; Pins 2 & 3 Open; V_{CC} = 4.5V; V_O = 2.4V; $I_O \leq$ 100 µA	2.87	3.8	4.24	V	7,8
Hysteresis	I_{HYS}	$I_{HYS} = I_{TH+} - I_{TH-}$		1.2		mA	
	V_{HYS}	$V_{HYS} = V_{TH+} - V_{TH-}$		1.2		V	
Input Clamp Voltage	V_{IHC1}	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10mA; Pin 1 & 4 Connected to Pin 3	5.4	6.0	6.6	V	
	V_{IHC2}	$V_{IHC2} = V_1 - V_4$; I_{IN} = 10mA; Pins 2 & 3 Open	6.1	6.7	7.3	V	
	V_{ILC3}	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 15mA; Pins 1 & 4 Open		12.0	13.4	V	
	V_{ILC}	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = – 10mA		–0.76		V	
Input Current	I_{IN}	$V_{IN} = V_2 - V_3$ = 5.0V; Pins 1 & 4 Open	3.0	3.7	4.4	mA	
Bridge Diode Forward Voltage	$V_{D1,2}$	I_{IN} = 3mA (see schematic)		0.59		V	
	$V_{D3,4}$			0.74		V	
Logic Low Output Voltage	V_{OL}	V_{CC} = 4.5V; I_{OL} = 4.2mA		0.1	0.4	V	7
Logic High Output Current	I_{OH}	$V_{OH} = V_{CC}$ = 18V			100	µA	7
		$V_2 - V_3$ = 5.0V; V_O = Open					
Logic Low Supply Current	I_{CCL}	V_{CC} = 5.0V		1.0	4	mA	
Logic High Supply Current	I_{CCH}	V_{CC} = 18V; V_O = Open		2		nA	7
Input-Output Insulation Leakage Current	I_{I-O}	Relative Humidity = 45% T_A = 25°C, V_{I-O} = 3000Vdc; t = 5 sec.			1	µA	9
	R_{I-O}						
Input-Output Resistance	C_{I-O}	V_{I-O} = 500Vdc		10_{12}		Ω	9
Input-Output Capacitance	C_{IN}	f= 1MHz, V_{I-O} = 0Vdc				pF	9
Input Capacitance		f = 1MHz; V_{IN} = 0V, Pins 2 & 3, Pins 1 & 4 Open		50		pF	

Parameter	Symbol	Min.	Max.	Units	Notes
Supply Voltage	V_{CC}	4.5	18	V	
Operating Temperature	T_A	0	70	°C	
Operating Frequency	f	0	4	kHz	1

Switching characteristics: HCPL 3700 $T_A = 25°C$, $V_{CC} = 5.0V$

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Notes
Propagation Delay Time to Logic Low Output Level	t_{PHL}	$R_L = 4.7K\Omega$, $C_L = 30pF$		4.0	15	μs	3
Propagation Delay Time to Logic High Output Level	t_{PLH}	$R_L = 4.7k\Omega$, $C_L = 30pF$		10.0	40	μs	4
Common Mode Transient Immunity at Logic Low Output Level	CM_L	$I_{IN} = 3.11mA$, $R_L = 4.7k\Omega$ $V_{O\,max} = 0.8V$, $V_{CM_L} = 140V$		600		$V/\mu s$	5,6
Common Mode Transient Immunity at Logic High	CM_H	$I_{IN} = 0mA$, $R_L = 4.7k\Omega$		4000		$V/\mu s$	5,6
Output Level Output Rise Time (10-90%) Output Fall Time (90-19%	 t_r t_f	$V_O^{min} = 2.0V$, $V_{CM_H} = 1400V$ $R_L = 4.7k\Omega$, $C_L = 30pF$ $R_L = 4.7k\Omega$, $C_L = 30pF$		 20 0.3		 μs μs	

Notes: HCPL 3700

1. Maximum operating frequency is defined when output waveform (Pin 6) obtains only 90% of V_{CC} with $R_L = 4.7k\Omega$, $C_L = 30$ pF using a 5 V square wave input signal.
2. All typical values are at $T_A = 25°C$, $V_{CC} = 5.0V$ unless otherwise stated.
3. The t_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 μs rise time) to the 1.5 V level on the leading edge of the output pulse (see Fig. 3).
4. The t_{PLH} propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 μs fall time) to the 1.5 V level on the trailing edge of the output pulse (see Fig. 3).
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) $dV_{CM/dt}$ on the leading edge of the common mode pulse, V_{CM}, to insure that the output will remain in a Logic High state (i.e., $V_O > 2.0V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) $dV_{CM/dt}$ on the trailing edge of the common mode pulse signal, V_{CM}, to insure that the output will remain in a Logic Low state (i.e., $V_O < 0.8V$) see Fig. 4.
6. In applications where $dV_{CM/dt}$ may exceed 50,000 V/μs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge current. The recommended value for R_{CC} is 240 Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240 Ω.
7. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH-}$ once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
8. a.c. voltage is instantaneous voltage.
   Device considered a two terminal device: Pins 1, 2, 3 and 4 connected together, and Pins 5, 6, 7 and 8 connected together.

Electrical characteristics: HCPL 2601 $T_A = 0$ to 70°C unless specified (typical values at $T_A = 25°C$, $V_{CC} = 5V$)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
High Level Output Current	I_{OH}	$V_{CC} = 5.5V$, $V_O = 5.5V$, $I_F = 250\mu A$, $V_E = 2.0V$		7	250	μA	
Low Level Output Voltage	V_{OL}	$V_{CC} = 5.5V$, $I_F = 5mA$ $V_E = 2.0V$, I_{OL} (Sinking) = 13mA		0.4	0.6	V	
High Level Supply Current	I_{CCH}	$V_{CC} = 5.5V$, $I_F = 0$, $V_E = 0.5V$		10	15	mA	
Low Level Supply Current	I_{CCL}	$V_{CC} = 5.5V$, $I_F = 10mA$ $V_E = 0.5V$		15	19	mA	
Low Level Enable Current	I_{EL}	$V_{CC} = 5.5V$, $V_E = 0.5V$		−1.6	−2.0	mA	
High Level Enable Current	I_{EH}	$V_{CC} = 5.5V$, $V_E = 2.0V$		−1.0		mA	
High Level Enable Voltage	V_{EH}		2.0			V	11
Low Level Enable Voltage	V_{EL}				0.8	V	
Input Forward Voltage	V_F	$I_F = 10mA$, $T_A = 25°C$		1.5	1.75	V	
Input Reverse Breakdown Voltage	BV_R	$I_R = 10\mu A$, $T_A = 25°C$	5			V	
Input Capacitance	C_{IN}	$V_F = 0$, f = 1 MHz		60		pF	
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	$I_F = 10mA$		−1.6		mV/°C	
Input-Output Insulation Leakage Current	I_{I-O}	Relative Humidity = 45% $T_A = 25°C$, t = 5 s, $V_{I-O} = 3000Vdc$			1	μA	3
Resistance (Input-Output)	R_{I-O}	$V_{I-O} = 500V$		10^{12}		Ω	3
Capacitance (Input-Output)	C_{I-O}	f = 1 MHz		0.6		pF	3

Switching characteristics: HCPL 2601 $T_A = 0\ 25°C$, $V_{CC} = 5V$)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Propagation Delay Time to High Output Level	t_{PLH}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$		35	75	ns	4
Propagation Delay Time to Low Output Level	t_{PHL}			35	75	ns	5
Output Rise Time (10-90%)	t_r			25		ns	
Output Fall Time (90-10%)	t_f			15		ns	
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$, $V_{EH} = 3V$, $V_{EL} = 0V$		25		ns	6
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	$R_L = 350\Omega$, $C_L = 15pF$, $I_F = 7.5mA$, $V_{EH} = 3V$, $V_{EL} = 0V$		15		ns	7
Common Mode Transient Immunity at High Output Level	CM_H	$V_{CM} = 50V$ (peak), V_O (min.) = 2V, $R_L = 350\Omega$, $I_F = 0mA$	1000	10,000		V/μs	8,10
Common Mode Transient Immunity at Low Output Level	CM_L	$V_{CM} = 50V$ (peak), V_O(max.) = 0.8V, $R_L = 350\ \Omega$, $I_F = 7.5mA$	-1000	-10,000		V/μs	9,10

Notes: HCPL 2601

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Fig. 5. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., $V_{OUT} > 2.0V$).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., $V_{OUT} < 0.8V$).
10. For sinusoidal voltages,
$$\left(\frac{dv_{CM}}{dt}\right)_{max} = \pi f_{CM} V_{CM}\ (p\text{-}p)$$
11. No external pull-up is required for a high logic state on the enable input.

Applications Data – HCPL 3700

General description

The HCPL 3700 is a voltage/current threshold detection optocoupler. The optocoupler uses an internal Light Emitting Diode (LED), a threshold sensing input buffer IC, and a high gain photon detector to provide an optocoupler which permits adjustable external threshold levels. The input buffer circuit has a nominal turn on threshold of 2.5 mA (I_{TH+}) and 3.8 volts (V_{TH+}). The addition of one or more external attenuation resistors permits the use of this device over a wide range of input voltages and currents. Threshold sensing prior to the LED and detector elements minimizes effects of different optical gain and LED variations over operating life (CTR degradation). Hysteresis is also provided in the buffer for extra noise immunity and switching stability.

The buffer circuit is designed with internal clamping diodes to protect the circuitry and LED from a wide range of over-voltage and over-current transients while the diode bridge enables easy use with a.c. voltage input.

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and C-MOS compatible breakdown voltages.

The HCPL 3700, by combining several unique functions in a single package, provides the user with an ideal component for industrial control computer input boards and other applications where a predetermined input threshold optocoupler level is desirable.

Design considerations

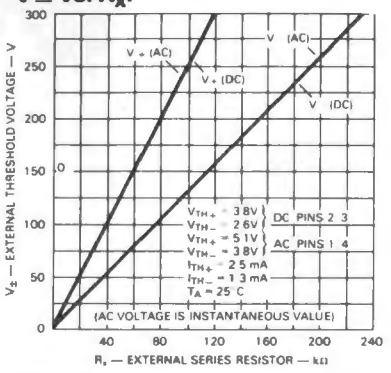
The HCPL 3700 optocoupler has internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_x, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of R_x can be obtained from Fig. 1. Specific calculation of R_x can be obtained from Equation (1). Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_x and R_p as shown in Fig. 2 and determined by Equations (2) and (3).

R_x can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts of a relay or switch, the HCPL 3700 in combination with R_x and R_p can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

In applications where $dV_{CM/dt}$ may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See note 6 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 μF be placed between Pins 8 and 5 to reduce the effect of power supply noise.

For interfacing a.c. signals to TTL systems, output low pass filtering can be performed with a pull-up resistor of 1.5 kΩ and 20 μF capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For a.c. input applications, a filter capacitor can be placed across the d.c. input terminals for either signal or transient filtering.

Figure 1: **Typical threshold characteristics, $V\pm$ vs. R_x.**



Either a.c. (Pins 1, 4) or d.c. (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_x can be determined without use of R_p via

$$R_x = \frac{V_{+\,(-)} - V_{TH+\,(-)}}{I_{TH+\,(-)}} \qquad (1)$$

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_x and R_p will permit this selection via equations (2), (3) provided the following conditions are met. If the denominator of equation (2) is positive, then

$$\frac{V_+}{V_-} \geqslant \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

Conversely, if the denominator of equation (2) is negative, then

$$\frac{V_+}{V_-} \leqslant \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}}$$

$$R_x = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \qquad (2)$$

$$R_p = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_-) - (V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \qquad (3)$$

Figure 2: **External threshold voltage level selection.**

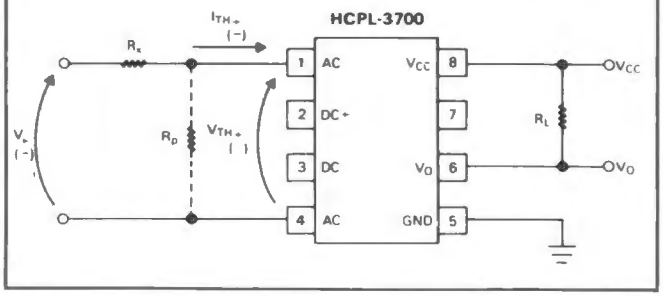


Figure 3: **Typical input characteristics, I_{IN} vs. V_{IN} (a.c. voltage is instantaneous value.)**

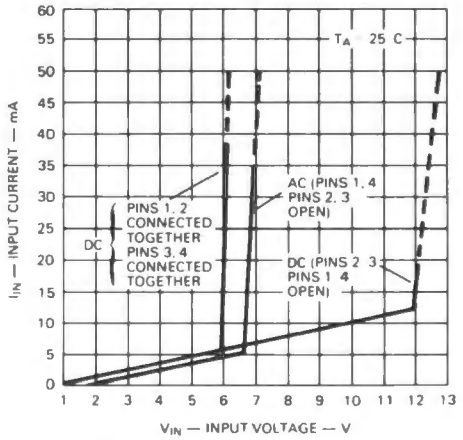
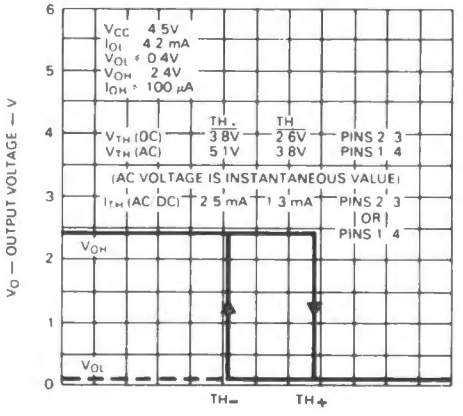
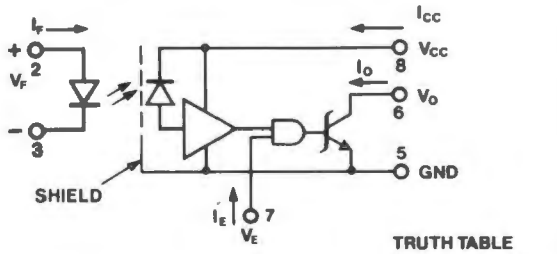


Figure 4: **Typical transfer characteristics. (a.c. voltage is instantaneous value.)**



RS data

Applications data – HCPL 2601



A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 & 5

TRUTH TABLE (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

General Description

The HCPL 2601 optically coupled gate combines a GaAsP light emitting diode and an integrated high gain photon detector. An enable input allows the detector to be strobed. The output of the detector i.c. is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 1000 volts/μsec., equivalent to rejecting a 300 volt P-P sinusoid at 1 MHz.

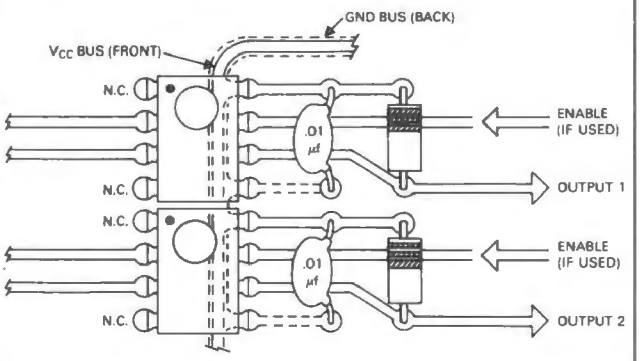
This unique design provides maximum d.c. and a.c. circuit isolation while achieving TTL compatibility. The isolator d.c. operational parameters are guaranteed from 0°C to 70°C allowing troublefree system performance. This isolation is achieved with a typical propagation delay of 35 nsec.

The HCPL 2601's are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Design considerations

Optimum performance can be achieved by using some care at the layout stage – see Fig. 5.

Figure 5: **Recommended printed circuit board layout.**



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Telephone: 01-250 4000
For technical enquiries ring: 01-202 8252 or 0536-201234
An Electrocomponents Group Company

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RS data

8-digit triplexed LCD driver i.c. 7231A

Stock number 302-514

The RS 7231 is a complete single chip triplexed LCD driver i.c. for use with 8-digit LCD displays. Display interconnections are reduced when compared with conventional direct drive techniques as the triplexed drive format is featured.

Features

- Single chip 8-digit driver
- Two independent annunciators per digit (decimal point and arrow)
- Triplexed operation reduces display connection wires
- Parallel address and data inputs
- On-chip oscillator
- Directly interfaces to microprocessors

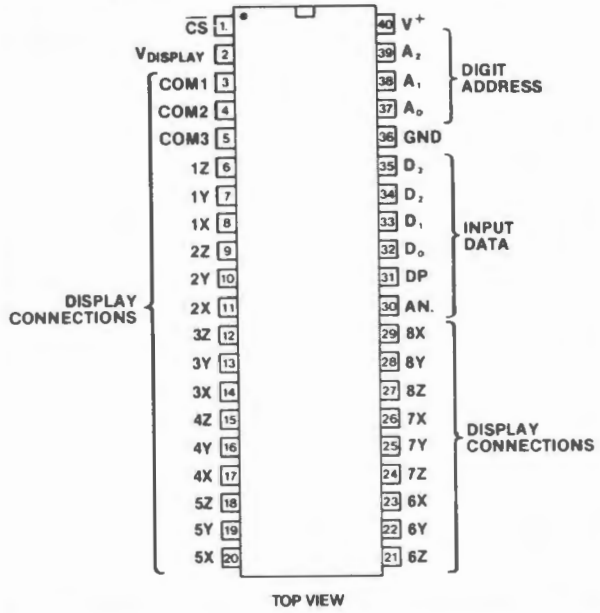
Absolute maximum ratings

Supply voltage V^+	6.5 V
Input voltage	$-0.3 \leq V_{IN} \leq 6.5$ V
Display voltage	$-0.3 \leq V_{DISP} \leq +0.3$ V
Power dissipation	0.5 W at 70°C
Operating temperature range	−20°C to +85°C
Storage temperature range	−55°C to +125°C

WARNING!

CAUTION:
ESD (Electro-Static Discharge) sensitive device. The data control inputs are diode protected, however permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Pin connections



Electrical characteristics $V^+ = 5V \pm 10\%$, $T_A = -20$ to $+85$°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power supply voltage	V^+		4.5	5	5.5	V
Data retention supply voltage	V^+	Guaranteed retention at 2 V	1.6	2		V
Logic supply current excluding display	I^+	Current from V^+ to GND $V_{DISP}=2$ V		30	100	μA
Shutdown total current	I_S	V_{DISP} pin 2 open circuit		1	10	μA
Display voltage range	V_{DISP}	$GND \leq V_{DISP} \leq V^+$	0		V^+	V
Display voltage setup current	I_{DISP}	$V_{DISP}=2$ V current from V^+ to V_{DISP} on-chip		15	25	μA
Display voltage setup resistor value	R_{DISP}	One of three identical resistors in string	40	75		kΩ
DC component of display signals		(sample test only)		¼	1	%($V^+ - V_{DISP}$)
Display frame rate	f_{DISP}		60	90	120	Hz
Input low level	V_{IL}	Pins 30-35,37-39 and 1.			0.8	V
Input high level	V_{IH}		2.0			V
Input leakage	I_{ILK}			0.1	1	μA
Input capacitance	C_{IN}			5		pF
Operating temperature range			−20		+85	°C

Figure 1 **Block diagram**

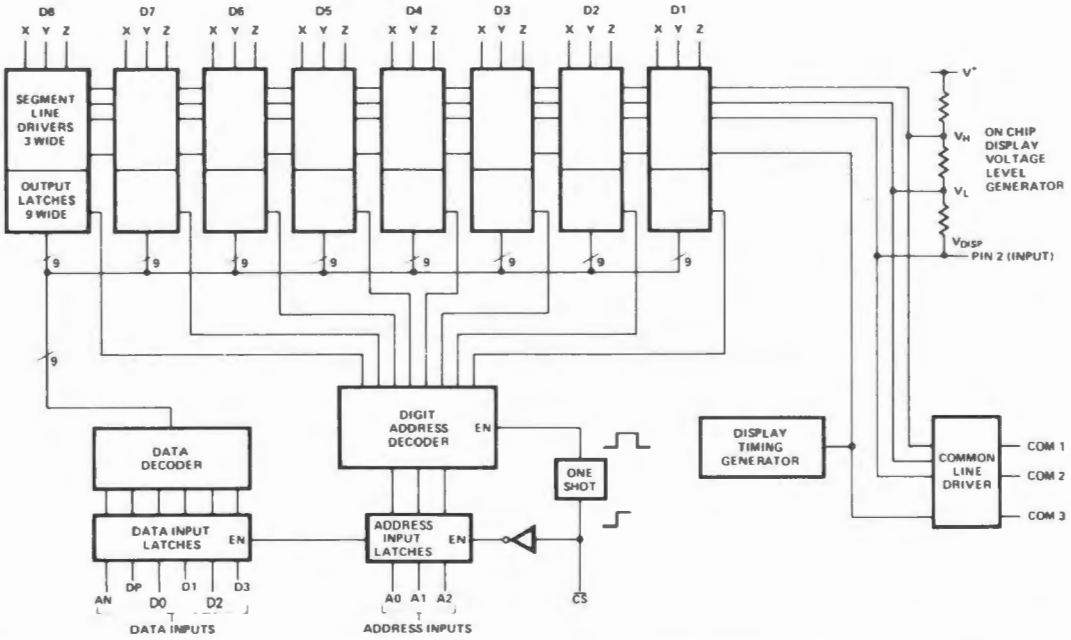


Table 1 **AC characteristics**
$V^+ = 5\,V \pm 10\%$, $T_A = -20$ to $+85°C$

Parameter	Symbol	Min	Typ	Max	Units
$\overline{CS}$ Pulse width	t_{cs}	500	350		ns
Address/Data setup time	t_{ds}	200			ns
Address/Data hold time	t_{dh}	0	−20		ns
Inter-chip select time	t_{ics}	3			μs

Terminal descriptions

Table 2

Terminal	Pin No.	Description	Function
AN	30	Annunciator control bit	High = ON
DP	31	Annunciator control bit	Low = OFF
D0	32	LSB 4-bit binary data input see table 5	High = logic 1 Low = logic 0
D1	33		
D2	34		
D3	35	MSB	
A0	37	LSB 3-bit digit address input	
A1	38		
A2	39	MSB see table 4	
$\overline{CS}$	1	Data input strobe/ chip select	Trailing (positive going) edge latches data, causes data input to be decoded and sent out to addressed digit
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display shutdown input.	Display voltage control. When open (or less than 1 V from V^+) chip is shutdown, oscillator stops and all display pins go to V^+.
Common line driver outputs	3, 4, 5		Drive display commons or rows.
Segment line driver outputs	6-29		Drive display commons or rows.
V^+	40	Positive supply	
GND	36	Ground.	

Operation

The 7231 i.c. generates the voltage levels and switching waveforms required to drive triplexed liquid crystal displays. A mask programmed ROM is featured which decodes the six bits of input data into 64 combinations of output segments to form the selected display.

The input format to the driver is six parallel data bits with a three bit parallel digit select address. Data is input under control of the chip select input (see figure 2 for timing diagram). The parallel data bits are subdivided into four binary code bits and two annunciator control bits. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string and display timing is derived from the self-contained oscillator.

Table 3 **Binary data decoding**

Code input				Display output HEX
D3	D2	D1	D0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	b
1	1	0	0	C
1	1	0	1	d
1	1	1	0	E
1	1	1	1	F

Figure 2 **Input timing diagram**

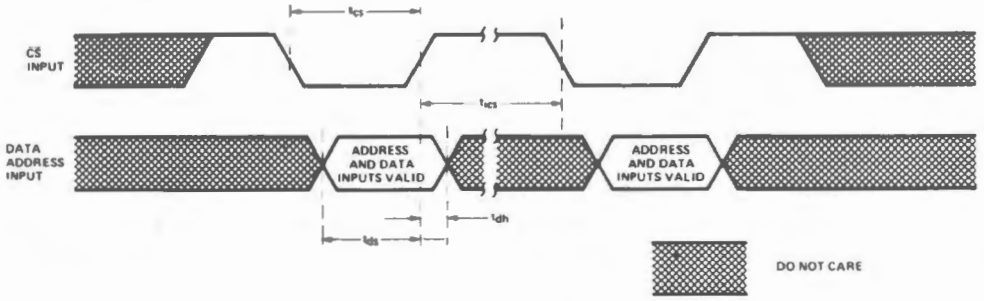
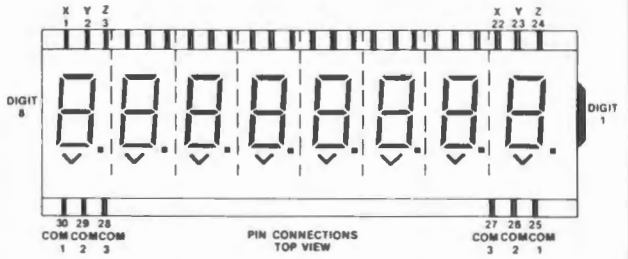


Table 4 **Address decoding**

Code input			Display output digit selected
A2	A1	A0	
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5
1	0	1	D6
1	1	0	D7
1	1	1	D8

Figure 4 **RS Triplexed display connections**



Input data format

The parallel input structure is organised to allow direct microprocessor interfacing (see figure 1). Address and data inputs are written into the input latches on the rising edge of the chip select input. The rising edge also triggers an on-chip pulse which enables the address decoder and latches the decoded data into the digit/character outputs.

Triplex operation for liquid crystal displays

Figure 3 shows the connection for a 7-segment display font with two annunciators. The voltage waveforms for the common lines and one segment line can be seen in figure 6. For simplicity just the Y segment line is shown. This line intersects with COM1 to form the "a" segment, COM2 to form the "g" segment and COM3 to form the "d" segment. Four different waveforms on the Y segment line are also shown for ON/OFF combinations of the "a", "g" and "d" segments. Each intersection acts as a capacitance from the segment line to the common line. This is shown schematically in figure 5.
Figure 8 shows the voltage across the "g" segment for the same four ON/OFF combinations in figure 6.

The degree of polarization of the liquid crystal material and thus the contrast of any segment depends on the RMS voltage across the intersection capacitance. Note that the RMS OFF voltage is always Vp/3, and the RMS on voltage is always 1.92 Vp/3.

An internal resistor string of three equal value resistors is used to generate the display drive voltages. One end of the resistor string is connected to V^+ on the chip and the other end is present at pin 2. This allows the display voltage to be optimised for the liquid crystal display being used. It is important that pin 2 never be driven below ground as this will cause device latchup and destruction of the chip.

Figure 3 **Connections for a typical digit**

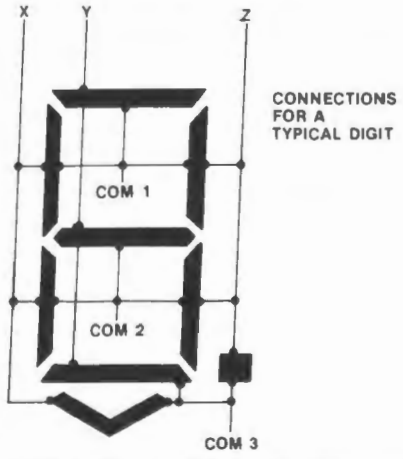
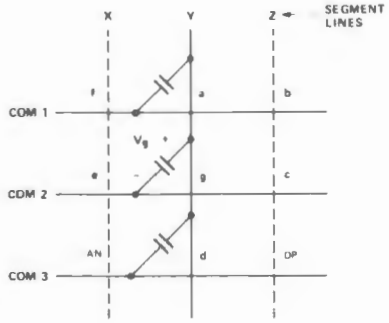


Figure 5 **Display schematic**



RS data

Figure 6 **Display voltage waveforms**

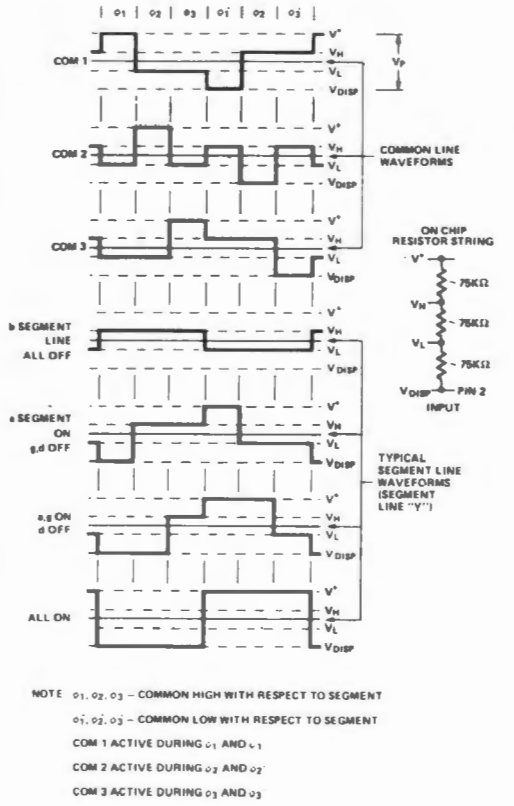
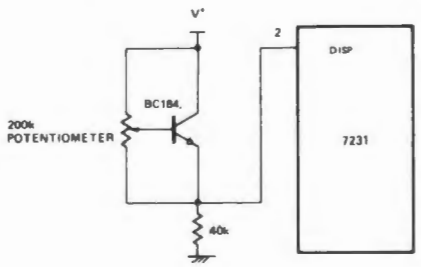


Figure 7 **Transistor multiplier for temperature compensation**



Temperature effects and compensation

With a variation in temperature on a liquid crystal display the threshold voltage will change. Typically the display peak volage has a temperature coefficient of –0.7% per °C. This means that as the temperature rises the threshold voltage goes down. Assuming a fixed value for Vp when the threshold voltage drops below Vp/3 OFF segments begin to be visible.

For applications where the display temperature does not vary widely, Vp may be set at a fixed voltage using a 200 kΩ potentiometer connected to ground. This method should be used in applications where the temperature variation of the chip and display is within ±5°C.

For applications where a larger temperature variation is expected temperature compensation for the display voltage is required. Figure 7 shows a suitable circuit which includes a transistor with a base-emitter junction temperature coefficient which is multiplied and compensates for the liquid crystal display temperature coefficient.

Figure 8 **Voltage waveforms on segment g (V_g)**

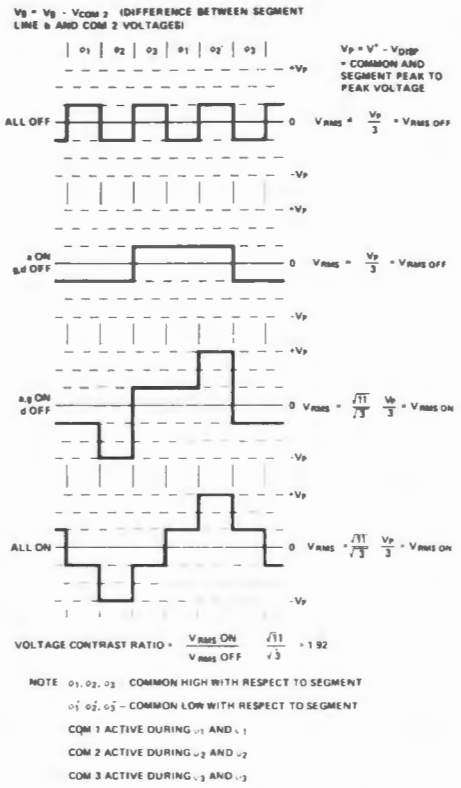
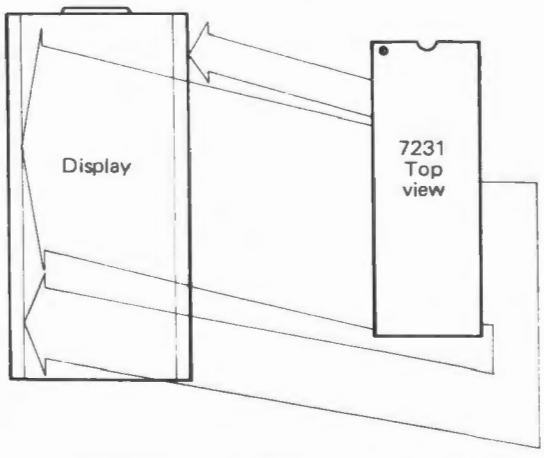


Figure 9 **Typical display connection layout**



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RS data

Instrumentation amplifier RS AD524AD

Stock number 302-463

The RS AD524AD is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. Featuring a combination of high linearity, high common mode rejection, low offset voltage drift and low noise, this i.c. is suitable for use in many data acquisition systems.

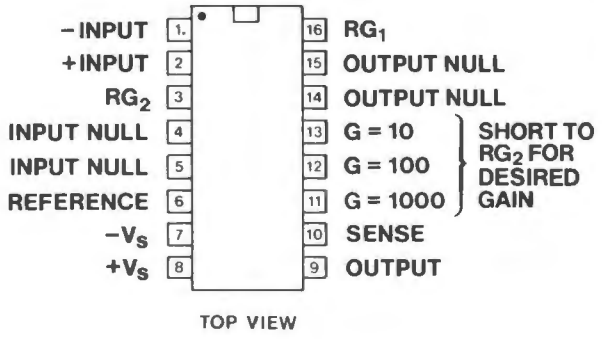
The precision of an instrumentation amplifier is provided at the expense of flexibility. Integration, differentiation, rectification, or any other non-voltage gain functions are best realised with operational amplifiers.

Instrumentation amplifiers are almost by definition used in situations where an over-voltage may be applied to their inputs. The input protection circuit of the RS AD524AD uses a unique junction FET to provide 36V of protection.

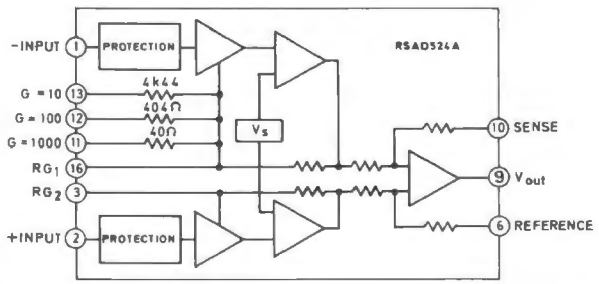
As a complete amplifier the RS AD524AD does not require any external components for fixed gains of 1, 10, 100 or 1000. For other settings between 1 and 1000 only a single resistor is required.

Features

- Low nonlinearity: 0.005% (G = 1)
- High CMRR: 130dB (G = 1000)
- Low offset voltage: 50μV
- Low offset voltage drift: 2μV/°C (G = 1000)
- Gain bandwidth product: 25MHz
- Pin programmable gain of 1, 10, 100, 1000
- Complete input protection, power on – power off
- No external components required
- Internally compensated



Basic circuit diagram



Electrical characteristics typical @ $V_S = \pm 15$V, $R_L = 2k\Omega$ and $T_A = +25$°C unless specified

Parameter

Gain

Gain equation

$$\text{Gain} = \left[\frac{40{,}000}{R_G} + 1\right] \pm 20\%$$

(Where RG is the external gain programming resistor connected between RG_1 and RG_2.)

Gain Range (pin programmable) — 1 to 1000

Gain error, max

G = 1	±0.05%
G = 10	±0.25%
G = 100	±0.5%
G = 1000	±2%

Nonlinearity, max

G = 1	±0.01%
G = 10	±0.01%
G = 100	±0.01%
G = 1000	±0.01%

Gain vs. Temperature, max

G = 1	5ppm/°C
G = 10	15ppm/°C
G = 100	35ppm/°C
G = 1000	100ppm/°C

Voltage offset (may be nulled)

Input offset voltage, max	250μV
vs. temperature, max	2μV/°C
Output offset voltage, max	5mV
vs. temperature, max	100μV/°C

Offset referred to the input vs. supply

G = 1	70dB
G = 10	85dB
G = 100	95dB
G = 1000	100dB

Input current
- Input bias current, max — ±50 nA
  - vs. temperature — ±100 pA/°C
- Input offset current, max — ±35 nA
  - vs. temperature — ±100 pA/°C

Input
- Input impedance
  - Differential resistance — $10^9\,\Omega$
  - Differential capacitance — 10 pF
  - Common mode resistance — $10^9\,\Omega$
  - Common mode capacitance — 10 pF
- Input voltage range
  - Max differ. input linear — ±10 V
  - Max common mode linear — ±10 V
- Common mode rejection d.c. to 60 Hz with 1 kΩ source imbalance, min
  - G = 1 — 70 dB
  - G = 10 — 90 dB
  - G = 100 — 100 dB
  - G = 1000 — 110 dB

Output rating — ±10 V @ 5 mA

Dynamic response
- Small signal – 3 dB
  - G = 1 — 1 MHz
  - G = 10 — 400 kHz
  - G = 100 — 150 kHz
  - G = 1000 — 25 kHz
- Slew rate
  - G = 1 to 100 — 5.0 V/μs
- Settling time to 0.01%, 20 V step
  - G = 1 to 100 — 15 μs
  - G = 1000 — 75 μs

Noise
- Voltage noise, 1 kHz
  - R.T.I — 7 nV/√Hz
  - R.T.O. — 90 nV/√Hz
- R.T.I., 0.1 to 10 Hz
  - G = 1 — 15 μV p-p
  - G = 10 — 2 μV p-p
  - G = 100 — 0.3 μV p-p
  - G = 1000 — 0.3 μV p-p
- Current noise
  - 0.1 to 10 Hz — 60 pA p-p

Sense input
- R_{IN} — 20 kΩ ±20%
- I_{IN} — 15 μA
- Voltage range — ±10 V min
- Gain to output — 1

Reference input
- R_{IN} — 40 kΩ ±20%
- I_{IN} — 15 μA
- Voltage range — ±10 V min
- Gain to output — 1

Temperature range
- Specified performance — −25°C to +85°C
- Storage — −65°C to +150°C

Power supply
- Power supply range — ±6 V to ±18 V
- Quiescent current — 3.5 mA (5 mA max)

Input offset and output offset

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors.

Voltage offset and drift comprise two components each; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G =1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (R.T.I.) which is to say that the effect on the output is 'G' times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also R.T.I.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total error R.T.I. = input error + (output error/gain)

Total error R.T.O. = (gain × input error) + output error

As an illustration, a typical RS AD524AD might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100 (−50μV) = −4.75mV.

The RS AD524AD provides for both input and output offset adjustment. This simplifies very high precision applications and minimizes offset voltage charges in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

Figure 1: **Offset null circuits**

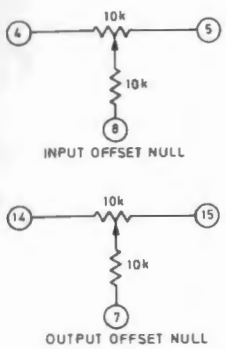


Figure 2: **CMRR vs. frequency R.T.I. zero to 1k source imbalance**

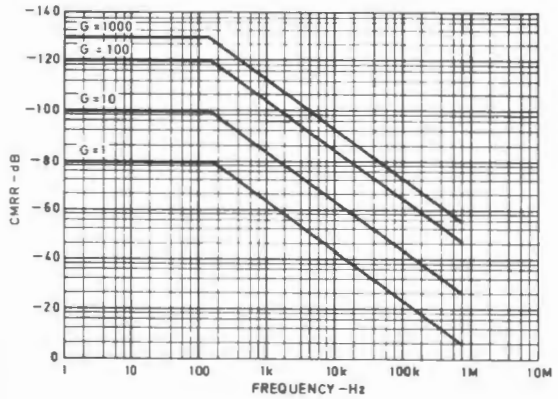


Figure 3: **PSRR vs. frequency**

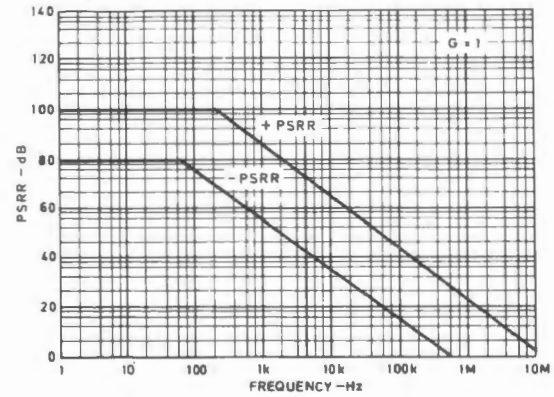


Figure 4: **Gain vs. frequency**

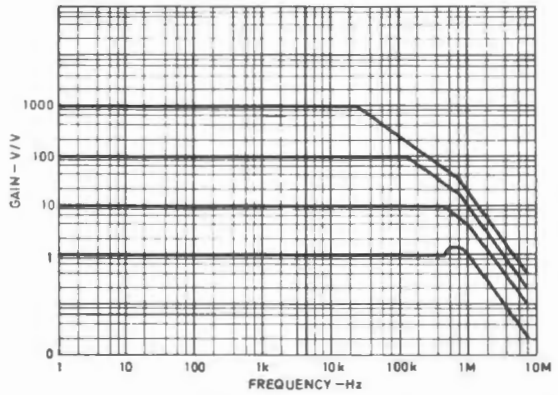
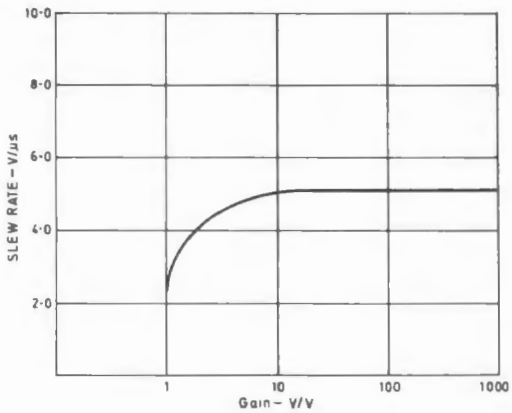


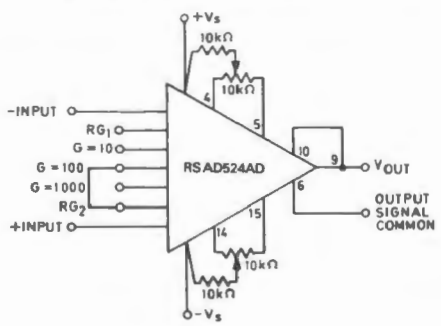
Figure 5: **Slew rate vs. gain**



Application notes on the RS AD524AD

The RS AD524AD has internal high accuracy pre-trimmed resistors for pin programmable gains of 1, 10, 100 and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG_2 together.
(No connection gives G = 1)

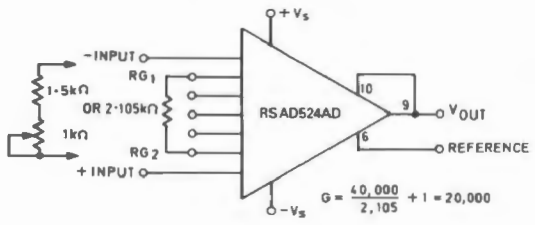
Figure 6: **Operating connections for G = 100**



RS data

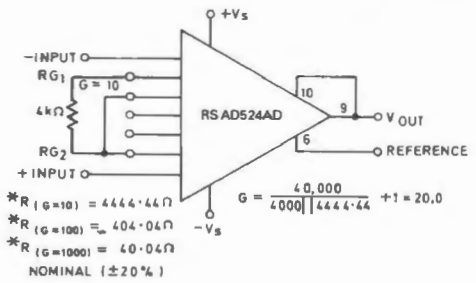
The RS AD524AD can be configured for gains other than those that are internally preset. There are two methods to do this. The first shown in Fig. 7 uses just an external resistor to program the gain.

Figure 7: **Operating connections for G = 20**



The second technique uses the internal resistors in parallel with an external resistor Fig. 8. This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

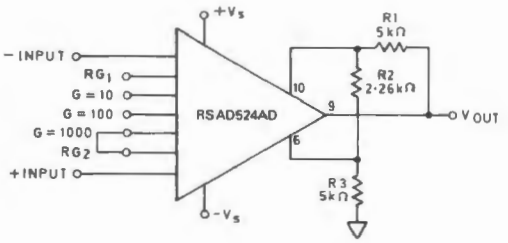
Figure 8: **Operating connections for G = 20**



The RS AD524AD may also be configured to provide gain in the output stage. Fig. 9 shows an H pad attenuator connected to the reference and sense lines of the RS AD524AD. R1, R2 and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

Sense and reference terminals allow remote sensing of output voltage so that effects of IR drops and ground drops may be minimized. For low current non-remote loads, the sense terminal may be tied directly to the output while the reference terminal may be tied to power supply common.

Figure 9: **Gain of 2000**



Output gain resistor values

Output Gain	R1, R3	R2	Nominal Gain
2	5kΩ	2.26kΩ	2.02
5	2.05kΩ	1.05kΩ	5.01
10	1kΩ	4.42kΩ	10.1

To minimize noise, shielding should be provided for the inputs.

R.S. Components Ltd. 13-17 Epworth Street, London, EC2P 2HA Telephone: 01-250 4000
For technical enquiries ring: 01-202 8252 or 0536-201234
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RS data

Digital panel meter i.c. 4½ digit BCD output 7135

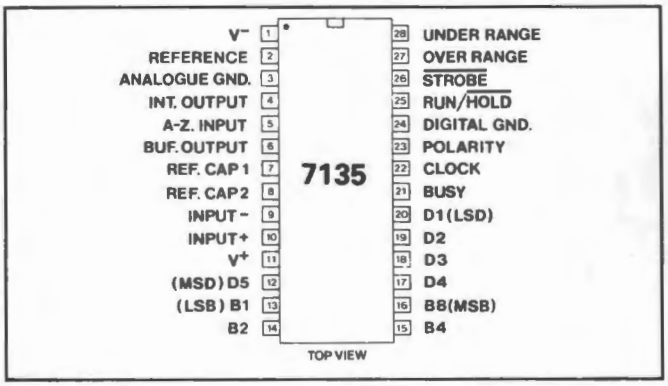
Stock number 302-261

The RS 7135 is a precision 4½ digit analogue to digital converter with BCD and digit strobe outputs. Dual slope conversion is used with an accuracy of ±1 count in 20,000. Applications include custom DVMs offering high resolution or direct interface to microprocessor or digital systems.

Under-range and over-range outputs are included to allow auto-ranging circuitry to be easily connected. A run/hold input is also featured which allows output data to be held until required.

Features

- Accuracy guaranteed to ±1 count over full range
- Guaranteed zero reading for 0V input
- 1 pA typical input current
- True differential input
- Over-range and under-range signals available for auto-ranging
- Blinking display for over-range indication
- Six auxiliary inputs/outputs are present for interfacing to microprocessors and other digital systems
- Multiplexed BCD data outputs



Absolute maximum ratings

Supply voltage V^+	+6V
Supply voltage V^-	−9V
Analogue and reference input voltage	V^+ to V^-
Clock input voltage	Gnd to V^+
Power dissipation	800 mW
Operating temperature range	0°C to +70°C
Storage temperature range	−65°C to +160°C

WARNING!

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Electrical characteristics $V^+ = 5V, V^- = -5V, T_A = 25°C$, 3 readings/sec

Parameter	Conditions	Min	Typ	Max	Units
Zero input reading	Vin = 0V, Full scale = 2V	−0.0000	±0.0000	+0.0000	Digital reading
Ratiometric reading	Vin = Vref, Full scale = 2V	+0.9998	+0.9999	+1.0000	Digital reading
Linearity over ± full scale	$-2V \leq V_{IN} \leq +2V$		0.5	1	Digital count error
Differential linearity	$-2V \leq V_{IN} + 2V$		0.01		LSB
Rollover error	$-V_{IN} = V_{IN} = 2V$		0.5	1	Digital count error
Noise	$V_{IN} = 0V$, Full scale = 2.000V		15		μV
Input leakage current	$V_{IN} = 0V$		1	10	pA
Zero reading drift	$V_{IN} = 0V$ 0°C ≤ T_A ≤ 70°C		0.5	2	μV/°C
Scale factor temperature coefficient	$V_{IN} = +2V$ 0°C ≤ T_A ≤ 70°C (ext. ref. 0ppm/°C)		2	5	ppm/°C
+5V supply range		+4	+5	+6	V
−5V supply range		−3	−5	−8	V
+5V supply current	fc = 0		1.1	3.0	mA
−5V supply current	fc = 0		0.8	3.0	mA
Power dissipation capacitance	Vs clock frequency		40		pF
Clock frequency		DC		1200	kHz

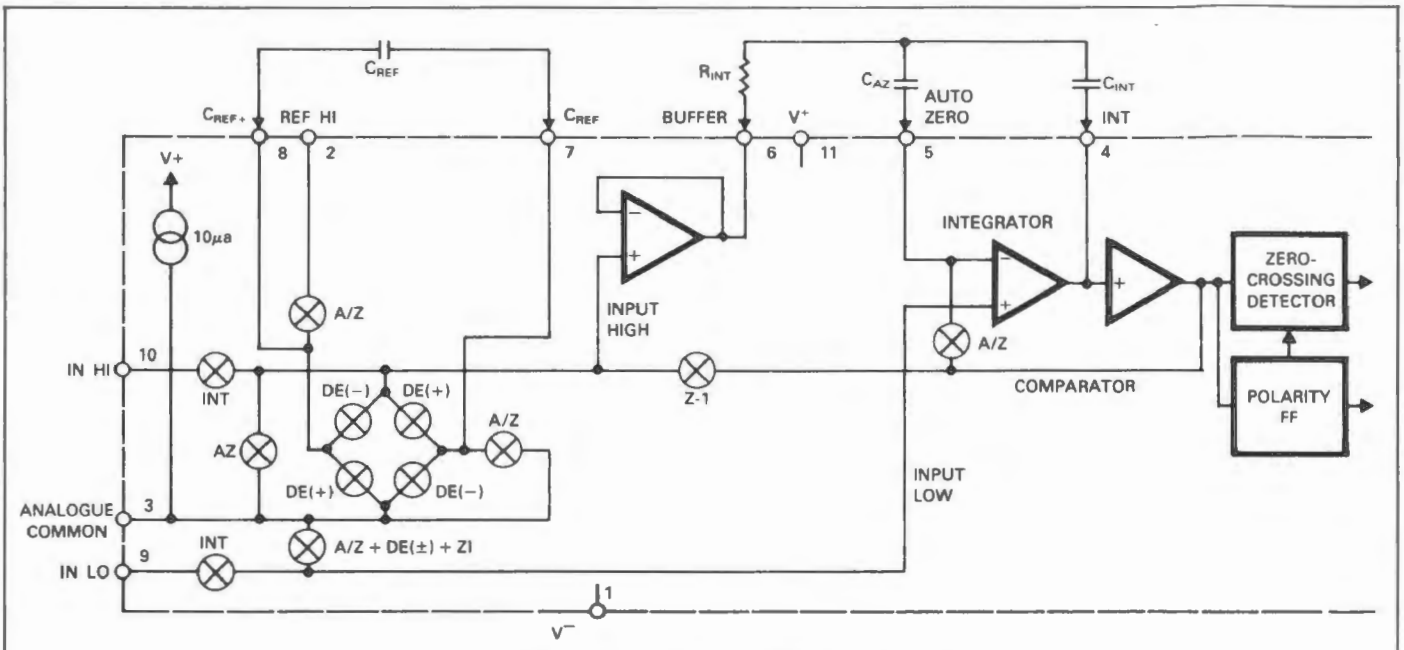


Figure 1 **Analogue Section of 7135**

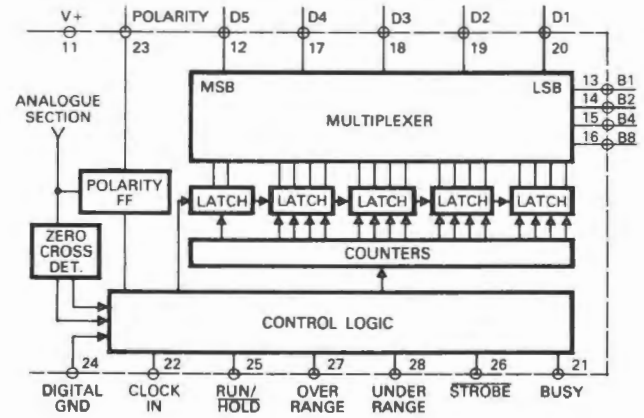


Figure 2 **Digital Section 7135**

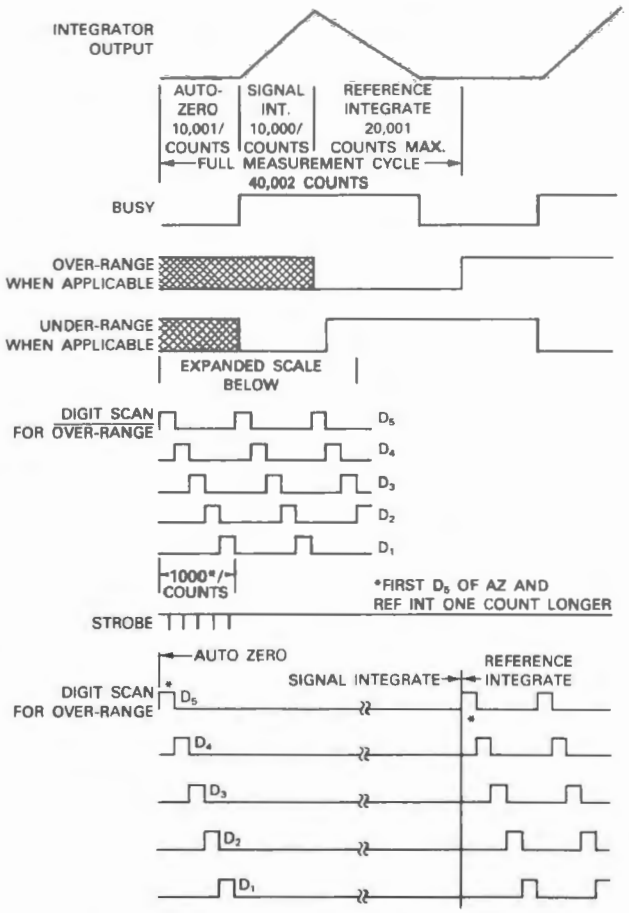


Figure 3 **Timing Diagram for Outputs**

Description of operation

The basic measurement cycle used can be divided into four operating phases.

1. auto-zero
2. signal integrate
3. de-integrate
4. zero integrator

1. Auto-zero

During this phase three operations occur. Firstly input high + and input low − are disconnected from the input pins and internally shorted to analogue common. Secondly the reference capacitor is charged up to the reference voltage. Thirdly a feedback loop is closed around the system to charge the auto-zero capacitor to compensate for offset voltages in the buffer amplifier, integrator and comparator. Since the comparator is included in the loop the auto-zero accuracy is limited only by the noise in the system. In any case the offset referred to the input is less than 10μV.

2. Signal integrate

During signal integrate the auto-zero loop is opened, the integral short removed and the internal input high + and low − are connected to the external input pins. The differential voltage present between input high + and low − is integrated for a fixed time. This differential voltage

can be within a wide common mode range, within one volt of either supply. If the input signal has no return with respect to the converter power supply, the low – input can be connected to analogue common to establish the correct common mode voltage. At the end of this phase the polarity of the integrated signal is latched into the polarity flip flop.

3. De-integrate or reference integrate
In this phase the low – input is internally connected to analogue common and the input high + is connected across the previously charged reference capacitor. Internal circuitry ensures the capacitor is connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $10000\left(\frac{V_{IN}}{V_{REF}}\right)$

4. Zero integrator
This final phase shorts the input low – to analogue common. The next step is to close a feedback loop around the system to cause the integrator output to return to zero. Under normal conditions this phase lasts for between 100 and 200 clock periods, but after an over-range it lasts for 6200 clock periods.

Table 1 **Digital input/output characteristics**

Parameter	Pin Nos	Conditions	Min	Typ	Max	Units
V_{INH}	22,25		2.8	2.2		V
V_{INL}				1.6	0.8	V
I_{INL}		$V_{IN} = 0V$		0.02	0.1	mA
I_{INH}		$V_{IN} = +5V$		0.1	10	μA
V_{OL}	All outputs	$I_{OL} = 1.6mA$		0.25	0.40	V
V_{OH}	B and D outputs	$I_{OH} = -1mA$	2.4	4.2		V
V_{OH}	21, 23, 26, 27, 28	$I_{OH} = -10\mu A$	4.9	4.99		V

Input characteristics

Differential input
The input can accept differential voltages anywhere within the common mode range of the input amplifier, ie from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a common mode rejection ratio of 86dB typ. However since the integrator also swings with the common mode voltage care must be observed so that the integrator output does not saturate. The worst case condition is with a large positive common mode voltage with a near full scale negative differential input voltage. Here the negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For such critical applications the integrator swing may be reduced to less than the usual recommended 4V swing at full scale with some loss in accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity.

Analogue common
This is used as the input low return during the auto zero and de-integrate phases. If the low – input is at a different potential to analogue common a common mode voltage exists in the system and will be taken care of by the common mode rejection ratio of the converter. In most applications the low – input will be set at a fixed known voltage, eg power supply common. Where this is the circuit used, analogue common should also be connected to this point which will remove the common mode voltage from the converter. The reference voltage should be referred to analogue common.

Voltage reference
The reference voltage must be positive with respect to analogue common and may be ideally derived from a 1.2V band gap reference, see figure 7.

Run/$\overline{\text{hold}}$ input pin 25
With this input open circuit or high the analogue to digital converter will free run giving output measurements every 40002 clock pulses. If taken low the converter will continue its current full measurement cycle and then hold this reading at the output until Run/$\overline{\text{hold}}$ is taken high or open circuit. After a hold operation a positive pulse on Run/$\overline{\text{hold}}$ longer than 300ns will initiate a new measurement cycle to take place, this will begin with between 9002 and 10001 counts of auto zero. If this pulse occurs before the full 40002 count measurement cycle has been completed it will be ignored and the converter will only finish its current measurement cycle. An indication that a full measurement cycle has been completed is that the first strobe pulse will occur 101 counts after the end of this cycle. Thus if Run/$\overline{\text{hold}}$ is low and has been low for at least 101 counts the converter is holding and a new measurement may be started if required.

Strobe pin 26
This is a negative going output pulse that is used to synchronise data transfer to external latches, UARTS, microprocessor systems etc. There are five negative going strobe pulses which occur only once in each measurement cycle, they occur in the centre of each of the respective digit drive pulses. They commence 101 pulses after the end of the full measurement cycle. Digit 5 the MSD goes high at the end of the measurement cycle and stays on for 201 counts. In the centre of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first strobe pulse goes negative for ½ clock pulse width. Similarly after digit 5, digit 4 drive goes high for 100 clock pulses, and 100 pulses later (at digit pulse centre) the strobe line goes negative again for ½ clock pulse width. This continues with digit 3, 2 and 1 where the fifth and last strobe pulse is present. The digit drivers continue to scan (unless the previous signal was over-range) but no additional strobe pulses will be sent until a new measurement is available.

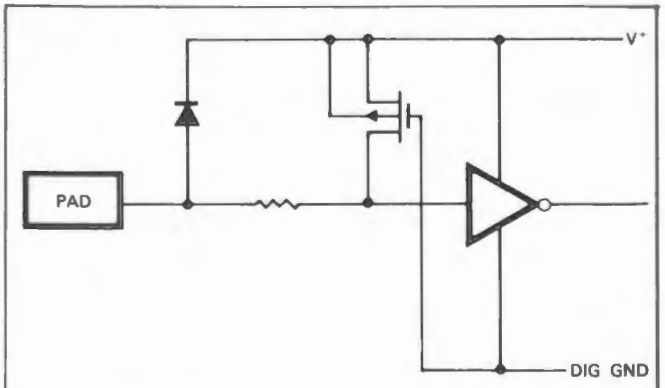


Figure 4 **7135 Digital Logic Input**

Busy pin 21
Busy output goes high at the beginning of signal integrate and stays high until the first clock pulse after zero crossing (or after the end of measurement in the case of over-range). The internal latches are enabled and loaded during the first clock pulse after a busy output and are latched at the end of this clock pulse. The circuit reverts to the auto-zero phase when the busy ouput goes low as it may also be considered as a $(\overline{ZI} + AZ)$ signal. A simple way for transmitting the data down a single wire pair from a remote location would be to AND the busy output with the clock and subtract 10001 counts from the number of pulses received. Note there is one no count pulse in each reference integrate cycle.

Over-range pin 27
This ouput goes high when the input signal exceeds the range of the converter (20000 counts). The output flip-flop is set after the corresponding busy output and is reset to zero at the beginning of reference integrate in the next measurement cycle.

Under-range pin 28
This output goes high when the reading is below 9% of the range. The output flip-flop is set after the corresponding busy output and is reset at the beginning of the signal integrate of the next reading.

Polarity pin 23
This output is high for a postive input signal and is valid even for a zero reading ie +0000 means the input signal is positive but less than the least significant bit. The converter may be used as a null detector by forcing equal frequency of + and − readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of the reference integrate phase and remains correct until it is updated for the next measurement.

Digit drive pulses pins 12, 17, 18, 19 and 20
Each digit drive pulse is a positive going signal that lasts for 200 clock pulses. The sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are continuously scanned unless an over-range occurs. If an over-range occurs all digit drives are turned off from the end of the strobe sequence until the beginning of the reference integrate phase when the digit scan will start again commencing with D_5. This will give a flashing display to give a visual indication of over-range.

BCD output pins 13, 14, 15 and 16
The binary coded decimal ouput is a positive logic output that occurs simultaneously with the digit drive signals.

Component selection

For optimum performance of the analogue circuitry care must be taken in selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage and conversion rate. These values must be chosen to suit the particular application.

Integrating resistor
This resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifer and integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. Values of 5 to 40μA give good results and a nominal value of 20μA should be chosen. The exact value of the integrating resistor may be chosen using the following formula.

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating capacitor
The product of the integrating resistor and capacitor should be selected to give a maximum voltage swing which ensures the tolerance build-up does not saturate the integrator swing (approximately 0.3volt from either supply rail). For ± supplies and analogue common tied to the power supply ground, a ± 3.5 to ± 4 volt full scale integrator swing is ideal and 0.4μF would be a nominal value. In general the value of C_{INT} can be chosen with the following equations.

$$C_{INT} = \frac{(10000 \times \text{clock period}) \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$C_{INT} = \frac{(10000)\,(\text{clock period})\,(20\mu A)}{\text{Integrator output voltage swing}}$$

An important characteristic of the integrating capacitor is low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input connected to the reference. This ratiometric condition should read half scale ie 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. In less critical applications polystyrene and polycarbonate capacitors may also be used.

Auto-zero and reference capacitors
The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible. The dielectric absorption of the reference and auto-zero capacitor is only important at power on or when the circuit is recovering from an overload condition. This means less expensive capacitors may be used if accurate readings are not required for the first few seconds of recovery.

Reference voltage
The analogue input voltage required to generate a full scale output is equal to 2X V_{REF}. The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason it is recommended that a high quantity reference is used where high accuracy absolute measurements are required. The 1.2V gap reference is ideal.

Rollover resistor and diode
A small rollover error occurs in the 7135 but this can be easily corrected by adding a diode and resistor in series between the integrator output and analogue common. The values shown in the application circuits are optimum for the recommended conditions. If integrator swing or clock frequency is modified adjustment may be needed. If rollover error is not important these can be eliminated.

Maximum clock frequency

The comparator in this circuit follows the integrator ramp with a 3μs delay, and at a clock frequency of 160kHz (6μs period) half of the first reference integrate clock period is lost in delay. This means that the output will change from 0 to 1 with a 50μV input, 1 to 2 with 150μV, 2 to 3 at 250μV etc. This transition at mid point is considered desirable in most applications. However if the clock frequency is increased appreciably above 160kHz the instrument will flash "1" on noise peaks. For many dedicated applications where the input signal is always of one polarity the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to 1MHz may be used. For a fixed clock frequency the extra count or counts caused by comparator delay will be constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the integrate phase. By careful selection of the ratio between this resistor and the integrating resistor the comparator delay can be compensated and the maximum clock frequency extended. At higher frequencies, ringing will cause significant non-linearities in the first few counts of the device.

The maximum clock frequency is established by leakage on the auto-zero and reference capacitors. With most devices measurement cycles as long as 10 seconds give no measureable leakage error. To achieve maximum rejection of 50Hz mains interference oscillator frequencies of 250kHz, 166 2/3kHz, 125kHz etc would be suitable. Note 100kHz (2.5 reading per second) will reject both 50 and 60Hz. The clock used should be free from significant phase or frequency variations, see applications circuits figures 5 and 6. As the device features a multiplexed output and may be used to indirectly drive display devices good power supply decoupling should be used.

Zero crossing flip-flop

This flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half clock pulse have died down. False zero-crossings caused by clock pulses are not recognised. The flip-flop delays the true zero-crossing by up to one count in every instance and if a correction was not made the reading would always be one count too high. To correct this the counter is disabled for one clock pulse at the beginning of phase 3 similarly a delay of 1 count at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2 so that true ratiometric readings occur.

Noise

The peak to peak noise around zero is approximately 15μV. Near full scale this value increases to approximately 30μV. Much of the noise originates in the auto-zero loop and is proportional to the ratio of the input signal to the reference.

Analogue and digital ground

Care must be taken to avoid ground loops and it is important that digital return currents are not fed into the analogue ground.

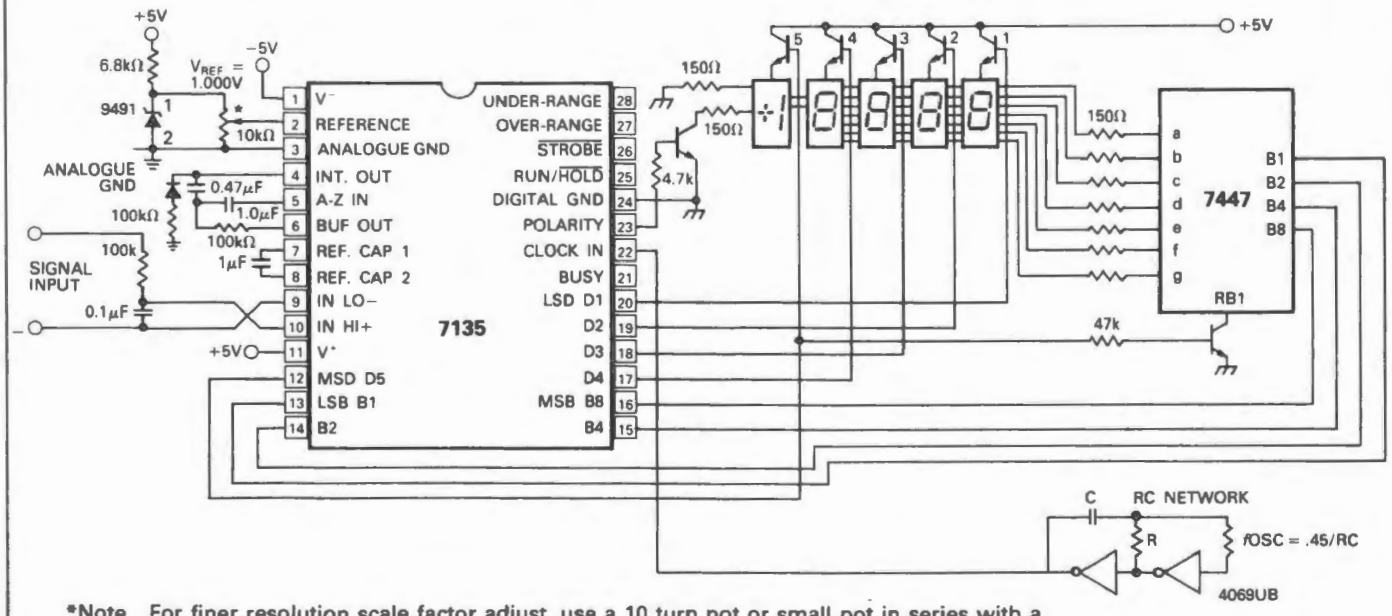
Power supplies

The 7135 is designed to operate from ± 5V supplies. With the following constraints the device will function from a single + 5V supply.

1. The input signal is referenced to the centre of the common mode range of the converter.

AND

2. The input signal is less than ± 1.5 volts in magnitude.



*Note For finer resolution scale factor adjust, use a 10 turn pot or small pot in series with a fixed resistor.

Figure 5 **4½ Digit A-D Converter with a multiplexed common anode LED display**

Applications

The application circuits show a variety of possibilities and the versatility of this converter. Figure 5 shows a complete circuit to interface with a 4½ digit common anode LED display. Note a typical R – C input filter is incorporated. The ½ digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder. The 2 gate clock circuit should use CMOS gates to maintain good power supply rejection. Figure 6 is similar except the output drives a multiplexed common cathode LED display. Both versions of the circuit will give a blinking display as a visual indication of over-range. A clock oscillator circuit using the low power 555 timer is shown.

LCD displays can be interfaced to the 7135 using an LCD display driver like the 7211, this can be seen in figure 9. A standard 4054 circuit is used for displaying the ½ digit, polarity and an over-range flag. Similarly a phosphorescent or other display type may be driven with the appropriate circuitry.

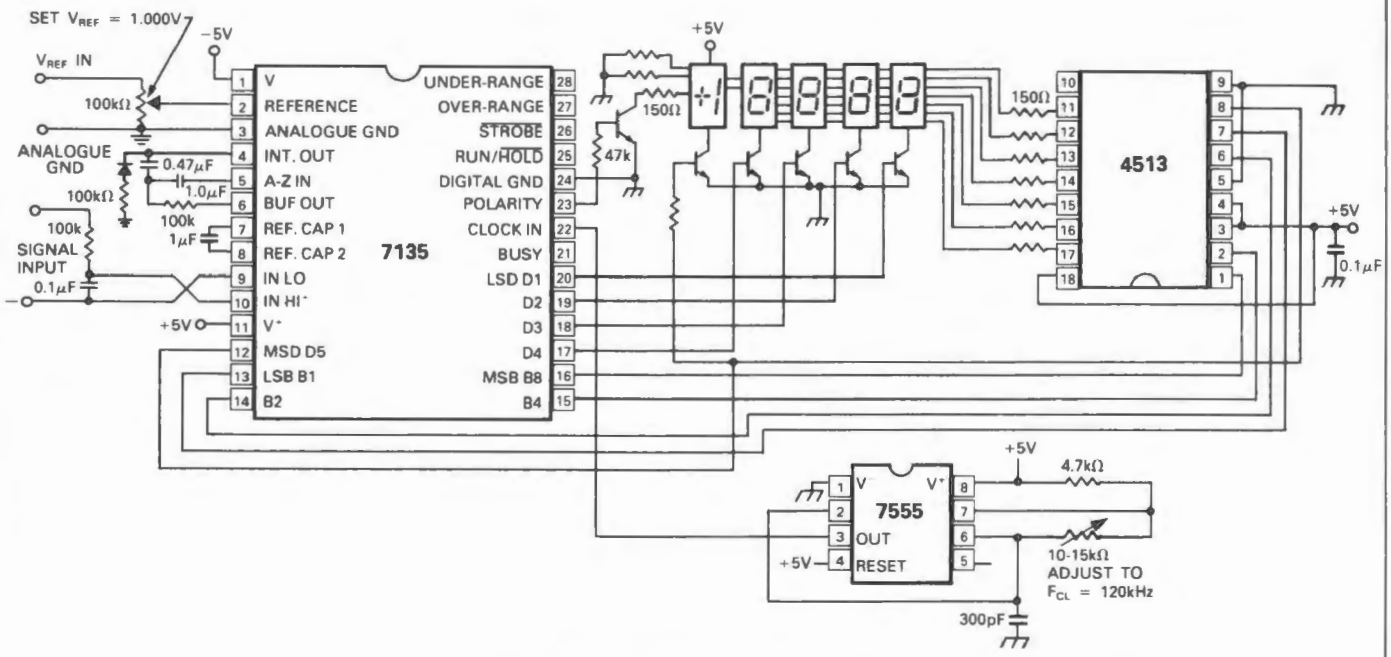


Figure 6 **Driving multiplexed common cathode LED displays**

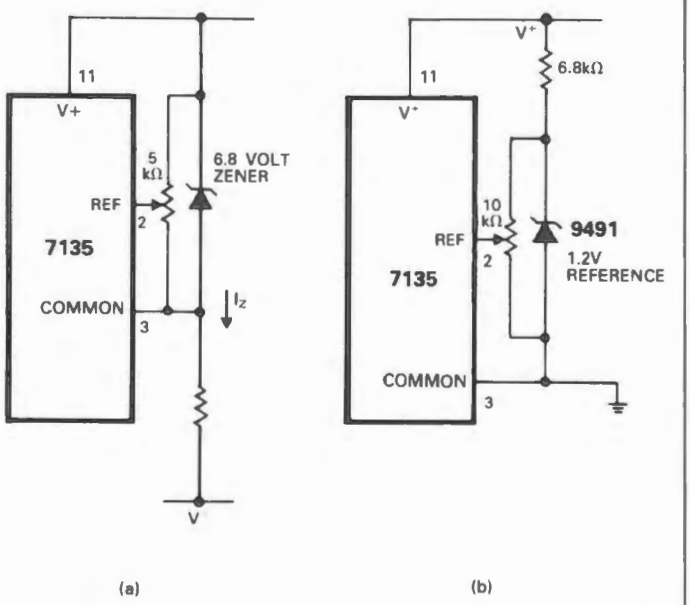


Figure 7 **Using an External Reference**

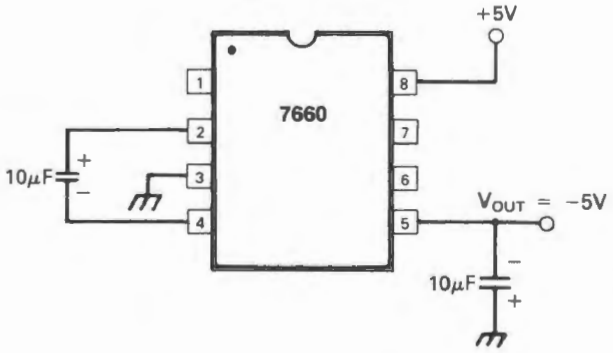


Figure 8 **Generating Negative Supply from +5V**

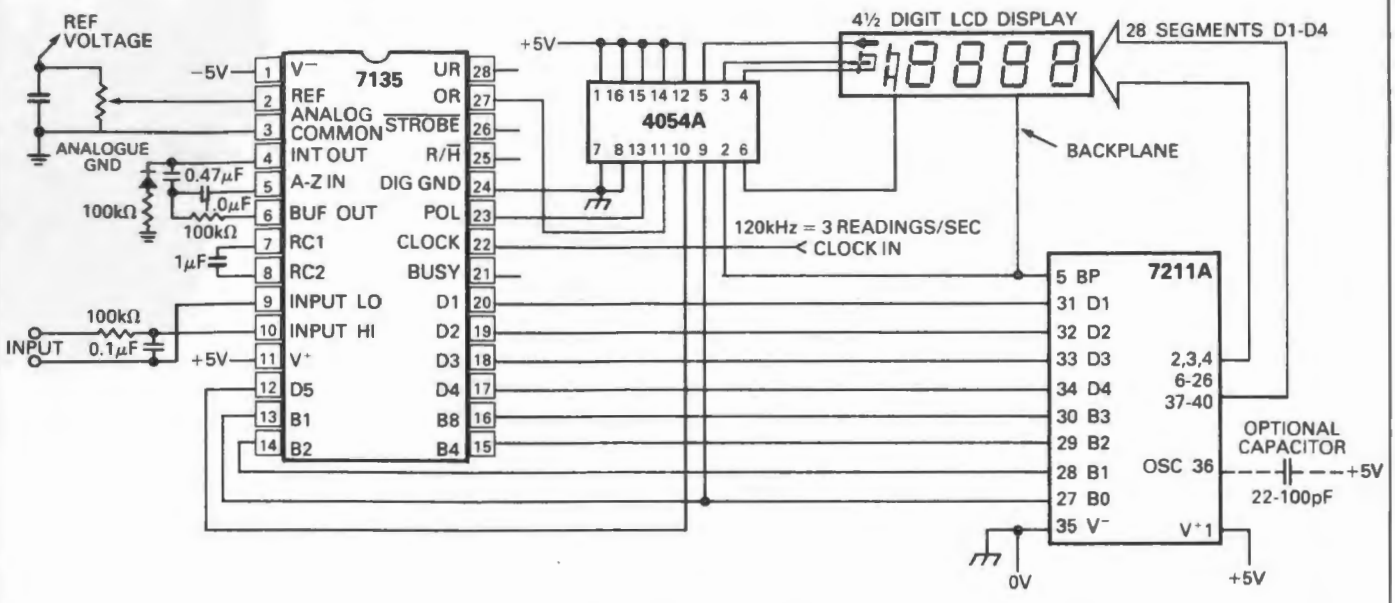


Figure 9 **Driving LCD Displays**

RS data

R.S. Components Ltd. 13-17 Epworth Street, London, EC2P 2HA
Telephone: 01-250 4000
For technical enquiries ring: 01-202 8252 or 0536-201234
An Electrocomponents Group Company

©RS Components Ltd. 1982, 1983

RS data

Speech Synthesis System

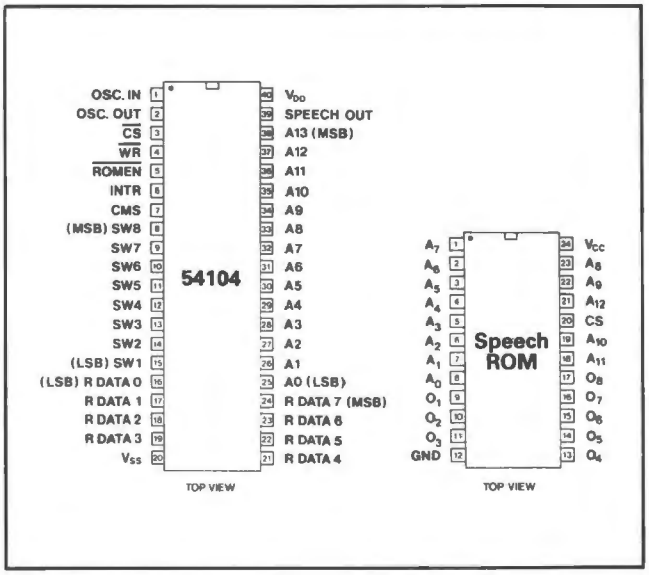
Stock numbers 303-365 thru 303-416

The RS speech synthesis system has been designed for easy interface to digital systems and produces good quality spoken English from its comprehensive vocabulary.

A minimum number of external components is required to produce a working speech synthesizer which can be easily expanded to future requirements using any of the five speech ROMs available. The RS ready made PCB simplifies construction and allows expansion up to a system incorporating eight ROMs.

Features

- Standard 8-bit bus interface to microprocessors and digital systems
- Comprehensive vocabulary, 5 dedicated ROMs available
- Good quality plain English
- Natural inflection and emphasis as in original speech
- TTL compatible
- On chip switch debounce for interfacing to manual switches
- Interrupt operation for cascading words
- Crystal controlled oscillator



Absolute maximum ratings

SPC (speech processor chip)

Supply voltage ____ +12V
Voltage on any pin ____ +12V
Operating temperature range ____ 0°C to +70°C
Storage temperature range ____ −65°C to +150°C

ROMs (speech library chips)

Supply voltage ____ +6.5V
Voltage on any pin ____ −0.5V to V supply
Power dissipation ____ 1W
Operating temperature range ____ 0°C to +70°C
Storage temperature range ____ −65°C to +150°C

SPC Electrical characteristics V supply = 7 to 11V, T_A = 0°C to + 70°C

Parameter	Conditions	Min	Typ	Max	Units
Power supply voltage		7		11	V
Power supply current				45	mA
Input low voltage		−0.3		0.8	V
Input high voltage		0.2		V_{DD}	V
Output low voltage	Output current = 1.6mA			0.4	V
Output high voltage	Output current = 100μA	2.4		5.0	V
Clock input low voltage		−0.3		1.2	V
Clock input high voltage		5.5		V_{DD}	V
Clock output low voltage				1.2	V
Clock output high voltage		5.5		V_{DD}	V
Input leakage				±10	μA
Clock input leakage				±10	μA
Silence voltage			0.45V_{DD}		V
Peak to peak speech output	V_{DD} = 11V		2.0		V
External load on speech output	R_{EXT} connected between speech output and V_{SS}	50			kΩ

ROMs Electrical characteristics V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C

Parameter	Conditions	Min	Typ	Max	Units
Power supply voltage		4.5	5.0	5.5	V
Power supply current	All inputs = 5.25V, data output open		100	130	mA
Logic 1 input voltage		2.2		V_{CC} + 1.0	V
Logic 0 input voltage		−0.5		0.6	V
Logic 1 output voltage	Output current = −200μA	2.4			V
Logic 0 output voltage	Output current = 3.2mA			0.4	V
Output leakage current	V_{OUT} = 4V chip deselected			10	μA
Output leakage current	V_{OUT} = 0.45V chip deselected			−20	μA

Table 1 **Word list in address order for complete ROM set**

Library Address	ROM 1: Number & Letters	ROM 2: Metering	ROM 3: Process Control	ROM 4: Clock Calendar	ROM 5: Warnings & Alarm
0	ONE	AMP	ADJUST	FIRST	ALARM
1	TWO	AND	AND	SECOND	ALERT
2	THREE	ANGLE	ANTI	THIRD	ALL
3	FOUR	CALIBRATE	AUTOMATIC	FOURTH	AND
4	FIVE	CENTIGRADE	AVERAGE	FIFTH	AREA
5	SIX	CYCLE	CANCEL	SIXTH	AT
6	SEVEN	DEGREE	CHANGE	SEVENTH	ATTENTION
7	EIGHT	'ES	CLOCKWISE	EIGHTH	CALL
8	NINE	FARAD	CLOSE	NINTH	CAUTION
9	TEN	FAHRENHEIT	COMPLETE	TENTH	CHECK
10	ELEVEN	FEET	CONTROL	ELEVENTH	CLEAR
11	TWELVE	FREQUENCY	COOLANT	TWELFTH	DANGER
12	THIRTEEN	GALLON	DATA	THIRTEENTH	DO
13	FOURTEEN	GRAM	DEVICE	FOURTEENTH	DOOR
14	FIFTEEN	HENRY	DOWN	FIFTEENTH	ELECTRICAL
15	SIXTEEN	HERTZ	ERROR	SIXTEENTH	EMERGENCY
16	SEVENTEEN	HIGH	FAST	SEVENTEENTH	ENTER
17	EIGHTEEN	HIGHER	FLOW	EIGHTEENTH	ESCAPE
18	NINETEEN	INCH	FORWARD	NINETEENTH	EVACUATE
19	TWENTY	IS	GUARD	TWENTY	EXPLOSION
20	THIRTY	KELVIN	HEAT	THIRTY	FAIL
21	FORTY	LIMIT	IN	'ITH	FAILURE
22	FIFTY	LITRE	ING	MONDAY	FIRE
23	SIXTY	LOAD	INSERT	TUESDAY	FLOOD
24	SEVENTY	LOW	LIMIT	WEDNESDAY	FROM
25	EIGHTY	LOWER	MACHINE	THURSDAY	GAS
26	NINETY	MEASURE	MOVE	FRIDAY	GO
27	HUNDRED	METRE	OFF	SATURDAY	HAZARD
28	THOUSAND	MINUS	ON	SUNDAY	HIGH
29	MILLION	MINUTE	OPEN	JANUARY	HOT
30	ZERO	NEGATIVE	OPERATE	FEBRUARY	INTRUDER
31	A	NOT	OUT	MARCH	IS
32	B	OFF	PRESS	APRIL	LEAKAGE
33	C	OHM	PUT	MAY	LEVEL
34	D	ON	RATE	JUNE	LOCK
35	E	OUNCE	RE	JULY	LOW
36	F	OVER	READY	AUGUST	NO
37	G	PENCE'	REPEAT	SEPTEMBER	NOT
38	H	PER	REVERSE	OCTOBER	OVER
39	I	POSITIVE	ROTATE	NOVEMBER	PASS
40	J	POUND	SELECT	DECEMBER	PRIORITY
41	K	POWER	SET	ALARM	REPLACE
42	L	PRESSURE	SHUT	AT	SAFE
43	M	RADIAN	SLOW	CLOCK	SMOKE
44	N	RANGE	START	DATE	STAY

45	O	RE	STEP	DAY	THE
46	P	SECOND	STOP	HOUR	TOXIC
47	Q	SPEED	SWITCH	IS	WARNING
48	R	'SS	TURN	MINUTE	WATER
49	S	TEMPERATURE	UP	MONTH	Low Tone 80Hz
50	T	THE	VALVE	OF	High Tone 400Hz
51	U	TOLERANCE		O'	
52	V	TON		SET	
53	W	VALUE		'SS	
54	X	VOLT		THEE	
55	Y	WATT		TIME	
56	Z	WEIGHT		YEAR	
57	'SS	20ms SILENCE			
58	COMMA	40ms SILENCE			
59	EQUAL	80ms SILENCE			
60	KILO	160ms SILENCE			
61	MEGA	320ms SILENCE			
62	MICRO				
63	MILLI				
64	NANO				
65	NUMBER				
66	PERCENT				
67	PICO				
68	POINT				
69	AM				
70	PM				
71	20ms SILENCE				

Overview

The speech synthesis system functions around a speech compression technique which reduces the amount of memory needed to store electronic speech by removing the excess or redundant data from the speech signal. The four main techniques involved are:

1. Elimination of redundant pitch periods.
2. Adaptive delta modulation coding to minimise bandwidth and memory requirements.
3. Phase angle adjustments to create mirror image symmetry.
4. Replacing the low level portion of a pitch period with silence (half period zeroing).

The above operations are performed on high quality speech, which yields a natural synthesised speech incorporating the tones, emphasis and inflection originally present.

Table 2 **A.C. Switching characteristics** V_{DD} = 7 to 11V, T_A = 0 to 70°C

SPC

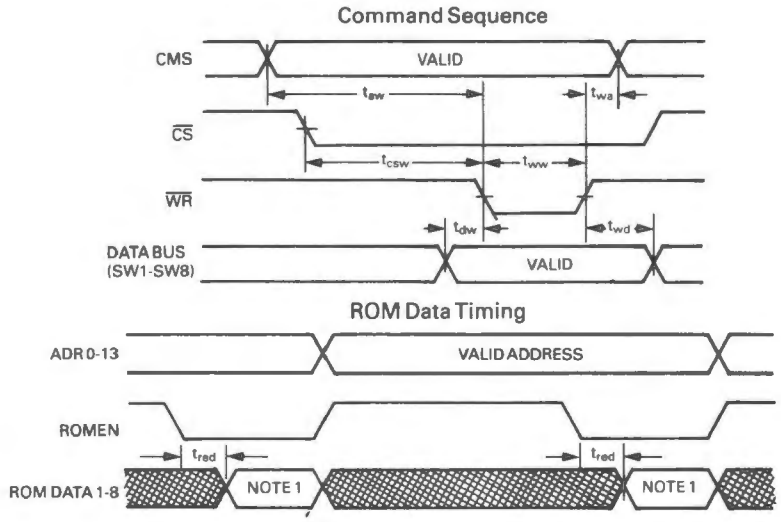
Symbol	Parameter	Min	Max	Units
t_{AW}	CMS valid to write strobe	350		ns
t_{CSW}	CS on to write strobe	310		ns
t_{DW}	Data bus valid to write strobe	50		ns
t_{WA}	CMS hold time after write strobe	50		ns
t_{WD}	Data bus hold time after write strobe	100		ns
t_{WW}	Write strobe width (50%)	430		ns
t_{RED}	$\overline{\text{ROMEN}}$ on to valid ROM data		2	μs
t_{WSS}	Write strobe to speech output delay		410	μs
I_F	External clock frequency	3.92	4.08	MHz
t_{SU}	Data bus valid to ROM select clock	25		ns
t_W	ROM select clock width	20		ns
t_H	Data bus hold time after ROM select clock	5		ns

Table 3 **A.C. switching characteristics** V_{CC} = 5V ± 10% T_A = 25°C

ROMS

Parameter	Conditions	Min	Max	Units
Chip select access time t_{AC}	All times to 1.5V level except t_{OFF}		120	ns
Output turn off delay t_{OFF}	tr & ts of input 20ns t_{OFF} tri-state		100	ns
Address access time t_A	output to less than 20μA output current		450	ns
Input capacitance C_{IN}	V_{IN} = 0V, f = 1MHz		7.5	pF
Output capacitance C_{OUT}	V_{OUT} = 0V, f = 1MHz		15	pF

Figure 1 **Timing diagram**



Note: ROM data 1-8 go valid any time after ADR 0-13 changes; however it must be valid within the t_{RED} specifications and remain valid until $\overline{ROMEN}$ goes high.

Functional Description

The following section describes the input and output functions associated with the speech processor i.c. A low represents a logic 0 (0.4V nominal) and a high represents a logic 1 (2.4V nominal).

Inputs

$\overline{CS}$ Chip Select

The speech processor is selected with $\overline{CS}$ low. It is only necessary to have $\overline{CS}$ low during a command to the speech processor and is not necessary for the duration of the speech data.

SW 1-8 data bus

This is an 8-bit parallel data bus which contains the starting address of the speech data.

Data bus inputs SW1-8 accept an 8-bit binary address which is the address of the word to be 'spoken' (see table 1), the word list for complete ROM set giving a listing of the words and their respective address for the five word ROMs.

CMS Command Select

This line specifies the two control commands to the speech processor:

CMS	Function
0	Reset interrupt and start speech sequence
1	Reset interrupt only

$\overline{WR}$ Write strobe

The write strobe line latches the starting address (SW1-SW8) into an internal register. On the rising edge of $\overline{WR}$ the speech processor starts execution of the command specified by CMS. The command sequence is shown in the timing waveform figure 1. If a command to start a new speech sequence is issued during a speech sequence, the new speech will be started immediately. When connecting $\overline{WR}$ to a switch it must be a single pole two position type.

R data 1-8 ROM data

This is the 8-bit parallel data bus which conveys the speech data from the speech ROMs.

Outputs

INTR Interrupt

This signal goes high at the completion of any speech sequence and is reset by the next valid command or at power up.

A0-A13 ROM address

This is the 14-bit parallel bus that supplies the address of the speech data to the speech ROM.

$\overline{ROMEN}$ ROM enable

For low power applications this line is used to drive transistors which switch the supply to the static speech ROMs.

Speech out

This is the analogue output that represents the speech data.

Input/Output signals

OSC-IN, OSC-OUT, Clock input/output

These two terminals are used to connect the main timing reference (crystal) to the speech processor, see figure 3.

Figure 2 **Speech processor block diagram**

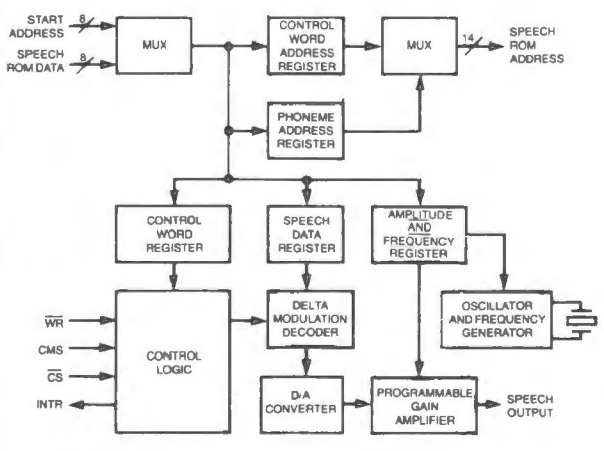
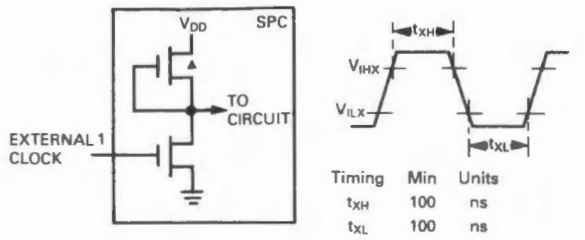


Figure 3 **External Clock Input (4.0MHz)**



Timing	Min	Units
t_{XH}	100	ns
t_{XL}	100	ns

Operation

The unsynthesised waveform for typical voice pitched period might look like the signal shown in figure 4a. In the process of converting this signal to a synthetic form, several operations are performed.

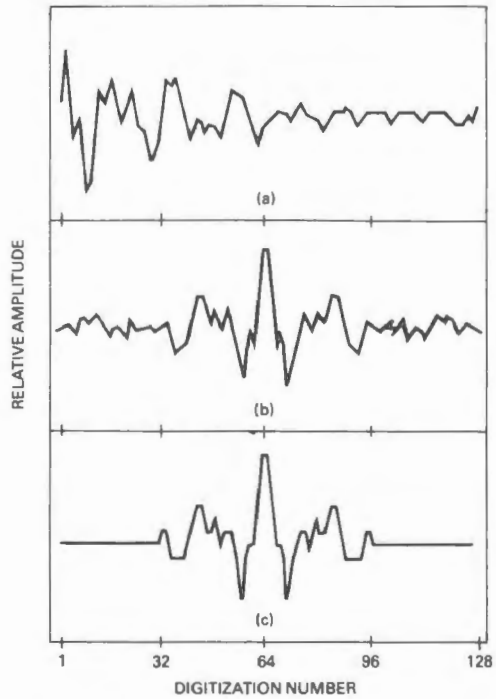
First the phase delay of the signal can be adjusted to create a symmetrical waveform about the centre of the pitch period as shown in figure 4b.

The next operation is to replace the low level beginning and ending quarters of the waveform with silence. The result is a compression factor of 4 to 1 on the original data. Finally delta modulation is applied and the results can be seen in figure 4c.

When the $\overline{WR}$ goes high, the start address code, is loaded into the control word address register. The speech processor uses this control address to fetch the first block of speech data. The control word contains waveform information, repeat information and address of the speech data. This address is loaded into the phoneme address register and is used to fetch the speech data used to recreate the speech waveform.

Synthesis of the waveform starts with a period of silence (no speech required) a quarter period of adaptive delta modulation generated speech followed by the same speech data selected in reverse. Finally the speech processor will finish the last quarter cycle of the speech block period with silence. This resulting phase modified speech data sounds the same as the original speech. At the end of a waveform or speech block the speech processor makes a decision about repeating the sequence. Each waveform of a typical voiced signal may be repeated an average of 3 or 4 times. The typical unvoiced waveform may be repeated approximately 7 to 8 times. Once the proper number of repeats has been generated the speech processor will begin a new speech block sequence. This operation continues until the speech processor has executed all control words associated with the original eight bit start address code.

Figure 4 **Speech compression**



(a) Original Speech Waveform
(b) Phase Angle Adjusted to Create Mirror Symmetry
(c) Half-Period Zeroed and Delta Modulated

The encoding technique stores the speech signals as adaptive delta modulation data which exploits the relatively predictable and slowly changing characteristics of voiced speech. Because of the small differential between successive speech samples, a delta value rather than an absolute value can be used to determine the actual speech signal. Addition of the delta value to the previously accumulated values results in a new output waveform signal level. An adaptive technique is used so that the delta step size can change in response to slope variations. This technique uses multiple delta modulation step sizes to obtain a more accurate resolution and yet the required amount of stored data remains lower than the information required for a more conventional encoding scheme.

Forming sentences

In normal human speech, the brain puts durations of silence between the words to make the phrases flow smoothly. Various silence durations are included in the speech ROMs which allow the actual quality of any phrase to be significantly improved. The most natural response will result if the actual spoken phrase is studied and the closest duration of silence is chosen from the word list. A rough guide to use is the words beginning with the letters K, T, P, B, D or G insert approximately 80ms silence prior to the words and for those ending in the same letters as above, approximately 40ms silence following the word is recommended. For other words a delay of appoximately 20ms should be used.

Ready made speech synthesis printed circuit board system operation.

The ready made printed circuit board allows a complete speech synthesis system to be quickly assembled. All connections are made through a 64 way a/c indirect edge connector see table 6 for connection details. The board operates from a single +9V supply and features an audio output for an 8Ω loudspeaker, VR1 may be used to select the required output volume. The input data format consists of an initial 3-bit ROM select address on SW1 to SW3 which is latched in with a ROM select clock pulse, this operation selects the required ROM and only needs repeating when a different ROM is required. If the SW4 line is held high during a ROM select clock pulse the audio output will be muted.

Word selection is achieved by setting up the required word address on SW1 to 8 the data bus input. CMS and $\overline{CS}$ are set up and the word is output when a $\overline{WR}$ strobe is issued. An interrupt

output becomes active when the word has been spoken. This enables the control system to set the CMS line if required and initialise the next word selection sequence see table 2 and figures 1 and 5 for timing details.

Table 4 **Speech synthesis PCB component list**

RESISTORS			CAPACITORS		
R_1	470R	131-211	C_1	10μ	104-449
R_2	470R	131-211	C_2	22n	125-783
R_3	56K	131-463	C_3	470p	125-862
R_4	47K	131-457	C_4	470p	125-862
R_5	47K	131-457	C_5	100n	125-806
R_6	100R	131-132	C_6	10μ	104-449
R_7	2K2	131-299	C_7	10n	125-777
R_8	2K2	131-299	C_8	10n	125-777
R_9	8K2	131-362	C_9	4n7	125-761
R_{10}	8K2	131-362	C_{10}	100n	125-806
R_{11}	8K2	131-362	C_{11}	100n	125-806
R_{12}	100K	131-491	C_{12}	2μ2	114-446
R_{13}	47K	131-457	C_{13}	22p	125-828
R_{14}	6K8	131-356	C_{14}	470μ	104-499
R_{15}	2R2	145-608	C_{15}	100n	125-806
R_{16}	4K7	131-334	C_{16}	4μ7	103-985
R_{17}	1K5	131-277	C_{17}	100n	125-806
R_{18}	1M	131-615	C_{18}	470μ	104-499
R_{19}	1K	131-255	C_{19}	220n	114-418
R_{20}	1K	131-255	C_{20}	220n	114-418
R_{21}-R_{28}	820R	131-249	C_{21}	56p	114-676
			C_{22}	27p	114-654
			C_{23}-C_{31}	100n	125-806
			C_{32}	220μ	104-483

SEMICONDUCTORS		
TR_1	2N3706	294-356
TR_2	2N3703	294-334
TR_3-TR_{10}	ZTX 751	295-523
IC_1	324	307-884
IC_2	LM380	306-819
IC_3	MM54104	303-416
IC_4	74LS175	307-698
IC_5	74LS138	307-648
IC_6 & IC_7	74LS32	307-569
IC_8 to IC_{15}	64K Speech ROMs	
Reg 1	7805	305-888

OTHER DEVICES	
Crystal 4MHz	304-633
Potentiometer 1M	185-498
DIN 41612 connector	468-119
IC sockets where required	

Table 5 **ROM selection data**

ROM Selected	Data Bus		
	SW3	SW2	SW1
IC_8	0	0	0
IC_9	0	0	1
IC_{10}	0	1	0
IC_{11}	0	1	1
IC_{12}	1	0	0
IC_{13}	1	0	1
IC_{14}	1	1	0
IC_{15}	1	1	1

A high on SW4 line during ROM selection causes the audio output to be muted.

Figure 5 **ROM Select sequence**

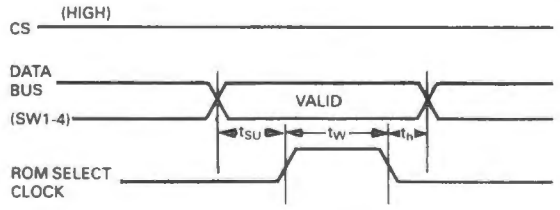
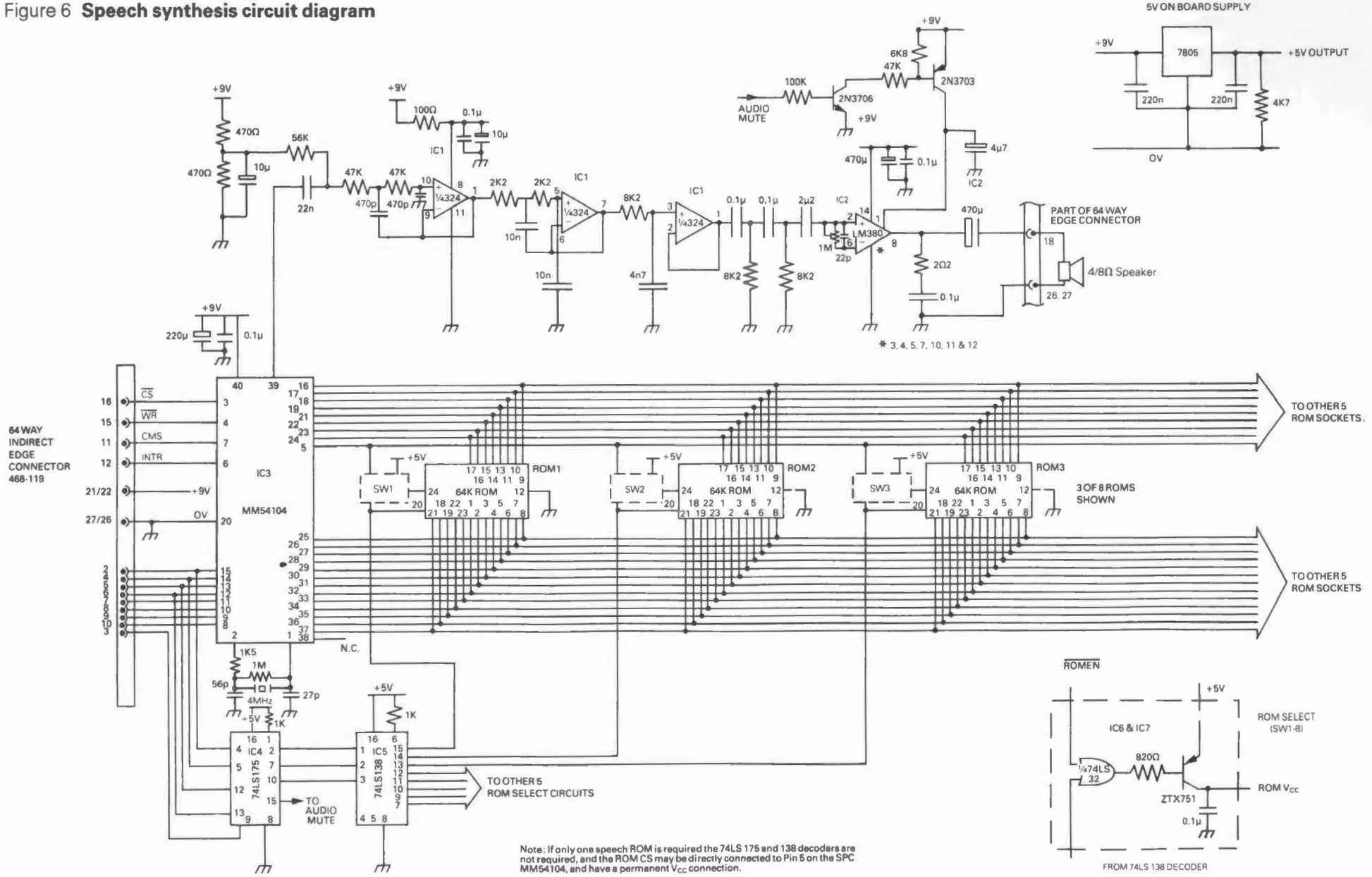


Table 6 **Speech synthesis PCB connections: Indirect edge connector 468-119**

Pin No.	Rows a & c commoned
2	SW1
3	ROM select clock
4	SW2
5	SW3
6	SW4
7	SW5
8	SW6
9	SW7
10	SW8
11	CMS
12	INTR
15	$\overline{WR}$
16	$\overline{CS}$
18	Audio output
21 & 22	+9V supply
26 & 27	Gnd

Figure 6 **Speech synthesis circuit diagram**



Note: If only one speech ROM is required the 74LS 175 and 138 decoders are not required, and the ROM CS may be directly connected to Pin 5 on the SPC MM54104, and have a permanent V_{CC} connection.

RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company
Telephone: 0536 201234
©RS Components Ltd. 1984

RS data

Precision Analogue Multiplier i.c. RS AD534

Stock number 302-154

The RS AD534 is a four quadrant multiplier and can be used in a wide range of applications. The multiplier can be considered as a basic building block for use in voltage controlled oscillators and filters, analogue signal processing.

Features

- Low four quadrant error
- Low wideband noise
- High Z monolithic differential inputs
- Excellent long term stability
- TO-100 package

Absolute maximum ratings

Supply voltage	±18V
Internal power dissipation	500mW
Output short circuit to ground	Indefinite
Input voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$
Rated operating temperature range	0 to +70°C
Storage temperature range	−65 to +150°C
Lead temperature, 60s soldering	+300°C

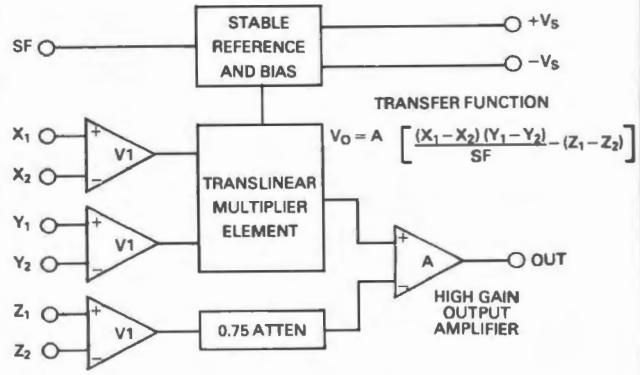


Figure 1 **RS AD534 functional block diagram**

Electrical characteristics (T amb at +25°C, with $\pm V_S$ = 15V, $R_L \geq$ 2k, unless stated)

Parameter	Condition	Typ
MULTIPLIER PERFORMANCE		
Transfer Function		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z_2$
Total Error[1]	−10V ≤ X, Y ≤ +10V	±1.0% max
	T_A = min to max	
	V_S = ±14V to ±16V	±1.5%
vs Temperature		±0.022%/°C
Scale Factor Error	SF = 10.00 nominal[2]	±0.25%
Temperature-Coefficient of Scaling-Voltage	T_A = min to max	±0.02%/°C
Supply Rejection	$\pm V_S$ = (15V) ±1V	±0.01%
Nonlinearity, X	X = 20V pk-pk	
	Y = ±10V	±0.4%
Nonlinearity, Y	Y = 20V pk-pk	
	X = ±10V	±0.01%
Feedthrough[3], X	Y nulled	
	X = 20V pk-pk 50Hz	±0.3%
Feedthrough[3], Y	X nulled	
	Y = 20V pk-pk 50Hz	±0.01%
Output Offset Voltage,		±5mV (±30mV max)
Drift	T_A = min to max	200μV/°C

DYNAMICS		
Small-Signal BW	V_{OUT} = 0.1V rms	1MHz
1% Amplitude Error	C_{LOAD} = 1000pF	50kHz
Slew Rate	V_{OUT} 20V pk-pk	20V/μs
Settling Time to ±1%	$\triangle V_{OUT}$ = 20V	2μs
NOISE		
Noise Spectral-Density	SF = 10	0.8μV/$\sqrt{Hz}$
	SF = 3 (Note 4)	0.4μV/$\sqrt{Hz}$
Wideband Noise	f = 10Hz to 5MHz	1mV rms
	f = 10Hz to 10kHz	90μV rms
	f = 10Hz to 10kHz, SF = 3 (Note 4)	60μV rms
OUTPUT		
Output Voltage Swing	T_A = min to max	±11V min
Output Impedance	Unity-Gain, f ≤ 1kHz	0.1Ω
Maximum Output Current	R_L = 0, T_A = min to max	30mA
Amplifier Open-Loop Gain	f = 50Hz	70dB
INPUT AMPLIFIERS (X, Y and Z)[5]		
Signal Voltage Range	Rated Accuracy (Diff. or CM)	±10V
	Operating (Diff.)	±12V
Offset Voltage, X Y		±5mV (±20mV max)
Drift	T_A = min to max	100μV/°C
Offset Voltage, Z		+5mV (±30mV max)
Drift	T_A = min to max	200μV/°C
CMRR (X, Y, Z)	50Hz, 20V pk-pk	80dB (60dB min)
Bias Current	Diff. Input = 0	0.8μA (2μA max)
Offset Current	Diff. Input = 0	0.1μA
Differential Resistance		10MΩ
DIVIDER PERFORMANCE		
Transfer Function	$X_1 > X_2$	$10\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$
Total Error[1]	X = 10V, −10V ≤ Z ≤ +10V	± 0.75%
	X = 1V, −1V ≤ Z ≤ +1V	± 2.0%
	0.1V ≤ X ≤ 10V, −10V ≤ Z ≤ + 10V (Note 6)	± 2.5%
SQUARER PERFORMANCE		
Transfer Function		$\frac{(X_1 - X_2)}{10} + Z_2$
Total Error[1]	−10V ≤ X ≤ + 10V	± 0.6%
SQUARE-ROOTER PERFORMANCE		
Transfer Function	$Z_1 \leq Z_2$	$\sqrt{10(Z_2 - Z_1)} + X_2$
Total Error[1]	1V ≤ Z ≤ 10V	±1.0%
POWER SUPPLY SPECIFICATIONS		
Supply Voltage	Rated Performance	± 15V
	Operating	± 8V to ± 13V
Supply Current	Quiescent	4mA (6mA max)

Functional description

The functional block diagram of the RS AD534 can be found in figure 1.

The input voltages are converted to differential currents by three identical voltage to current converters, each trimmed for *low* offset. The product of X and Y currents is generated by a multiplier cell using the translinear technique. An on-chip buried zener provides the stable reference. This internal reference source is laser trimmed for a scale factor (SF) of 10.000V.

The difference between XY/SF and Z is then applied to the output amplifier. This allows various closed loop configurations and therefore can reduce non-linearities due to the input amplifiers.

Non-linearity for signals applied to the X input are due almost entirely to the multiplier element and are of a parabolic form.

The generalised transfer function for the RS AD534 is:

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$$

Where A = 70dB typical open loop gain d.c.
X, Y, Z = Input voltages
(Full scale = ± SF, Peak = ± 1.25 SF)

Scale factor is pre-trimmed to 10.00 but is adjustable down to 3.

In most cases the open loop can be regarded as infinite, and the scale factor as 10. The operation performed by the RS AD534 will be of the form of the equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10(Z_1 - Z_2)$$

The scale factor can be adjusted within the range of 10 down to 3 by use of a series resistor/potentiometer network. A tolerance of ± 25% can be expected in R_{SF} due to device tolerances.

$$R_{SF} = 5.4K\,\frac{SF'}{10 - SF'}$$

where SF' is scale factor required.

Reduction in bias currents, noise and drift can be attained by decreasing scale factor. This has the overall effect of increasing signal gain without the usual increase in noise or offset.

N.B. The peak input signal = 1.25 x SF. Therefore peak input = ± 5V for SF = 4. Small signal performance is improved by a lower SF since the dynamic range of the inputs is fully utilised.

Supply voltages of ±15 are assumed, but satisfactory operation is possible down to ± 8V (see figure 11). Attenuation of the input must be employed for signals greater than ± 12 higher supply assumed.

The multiplier

In its simplest form the multiplier is a three terminal device (figure 2.)

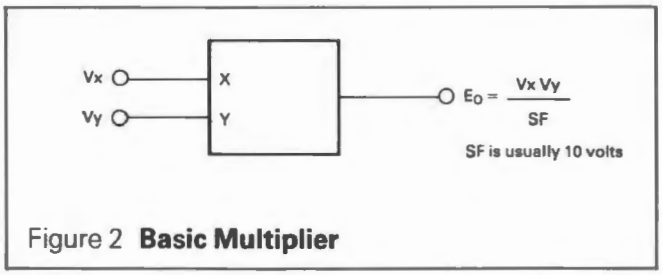


Figure 2 **Basic Multiplier**

A common input to both X and Y will yield a squared term at the output thus:

$V_X = V_Y = V_{IN}$
$\therefore V_O = V_{IN}^2/SF$

Figure 3 shows the RS AD534 being used as a multiplier.

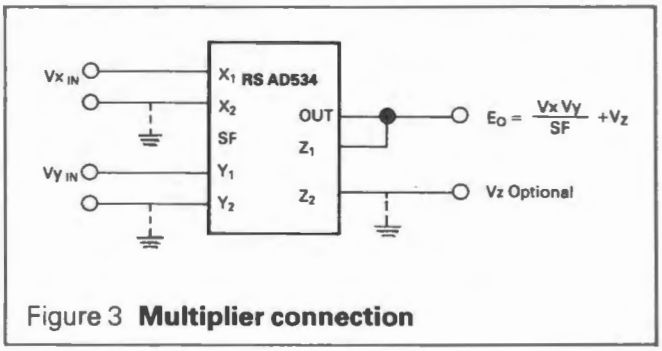


Figure 3 **Multiplier connection**

$$(X_1 - X_2)(Y_1 - Y_2) = 10V\,(Z_1 - Z_2)$$

No other external components are required for this practical multiplier and it is an improvement on the simple multiplier due to the differential inputs (including the feedback circuit) and the good common mode rejection ratio. In some applications such as suppressed carrier modulation, ac feedthrough can be reduced by use of the optional trim circuit shown in figure 4 (see also figure 14).

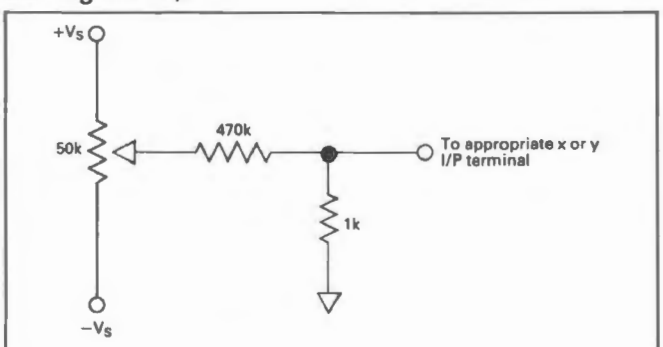


Figure 4 **Optional trimming circuit**

The high impedance terminal (Z_2) may be used to sum an additional signal into the output. In this mode the output amplifier may be considered as a voltage follower with a typical small signal bandwidth of 1MHz and 20V/μs slew rate. The ground should be referenced to the driven system and the differential inputs returned to their respective ground potentials. This is utilising the maximum accuracy of RS AD534.

Notes: [1]Figures given are percent of full-scale. ± 10V (i.e. 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3.
[5]See Functional Block Diagram, Figure 1, for definition of sections.
[6]With external Z-offset adjustment, Z ≤ ± X.

Scaling

The RS AD534 has a scale factor range of 10V down to 3V. Much lower scaling voltages can be achieved without any reduction of input signal range using a feed-back attenuator as in figure 5. This example shows a scale factor of unity such that $V_{OUT} = X, Y$.

Thus $V_O = \frac{R_1}{R_1 + R_2} E_C E_{IN}$

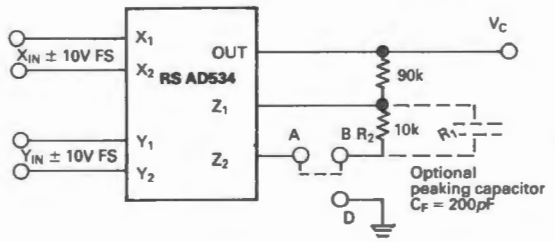


Figure 5 **Scale factor of unity**

$R_1 = 90k, R_2 = 10k$ = Unity scale factor

Note: This mode of operation lowers the bandwidth to less than 80kHz without the peaking capacitor. There is also an increased offset voltage.

$$V_{OFS} = \left(\frac{R_1 + R_2}{R_2}\right) I_{OF}$$

Feedback attenuation also retains the ability for adding a signal to the output via a signal applied to the high impedance terminal (Z_2).

By shorting B, D, in figure 5 and applying a signal between A and D, a gain of +10 can be obtained. With A and D shorted and the signal applied to D, B, a gain of −9 is obtained, and a voltage follower is produced by shorting A to B and the input to B, D.

Figure 6 shows an application as a current converter.

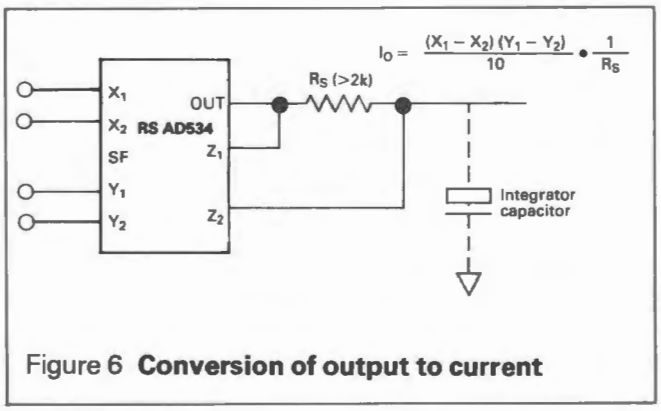


Figure 6 **Conversion of output to current**

A useful technique in voltage controlled systems such as the voltage to frequency converter is shown in Figure 7.

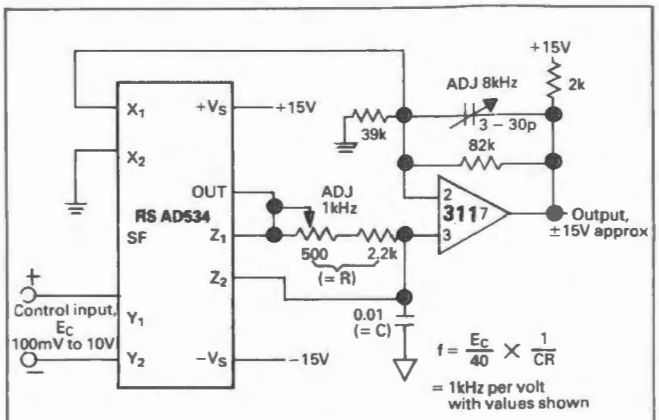


Figure 7 **Differential-input voltage-to-frequency converter**

Calibration procedure (See figure 7)
With E_C = 1.0V, adjust pot to set f = 1.000kHz. With E_C = 8.0V, adjust trimmer capacitor to set f = 8.000kHz. Linearity will typically be within ± 0.1% of FS for any other input.

Due to delays in the comparator this technique is not suitable for maximum frequencies above 10kHz.

A triangle-wave of ±5V pk appears across the 0.01μF capacitor; if used as an output, a voltage-follower should be interposed.

Divider

Figure 8 shows the RS AD534 connected as a basic divider.

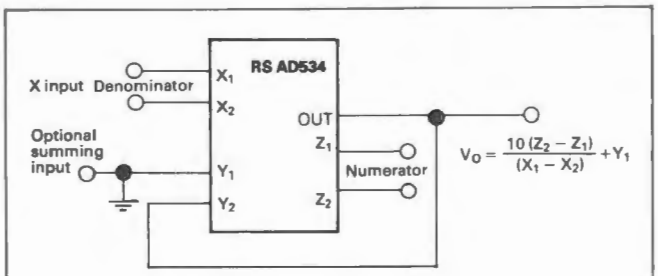


Figure 8 **Basic divider connection**

The differential operation on both numerator and denominator allows the ratio of two floating variables to be generated. The Y_1 input is a high impedance summing input that may be used for summing. Note that the bandwidth is proportional to the magnitude of the denominator as shown in figure 18.

The RS AD534 will maintain an accuracy of 1.5% over a range of 10V to 1V denominator range. This range may be extended to 100:1 by reducing the X offset with an externally generated trim voltage (± 7.5mV is required), applied to the unused X input. To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_2 (if X_2 is used for offset, otherwise reverse the signal polarity). Monitor the output via a blocking capacitor for this adjustment and trim for minimum output.

Reduction in bandwidth and increase in noise precludes operation beyond 100:1.

The overall gain can be reduced by attenuation as with the multiplier see figure 9.

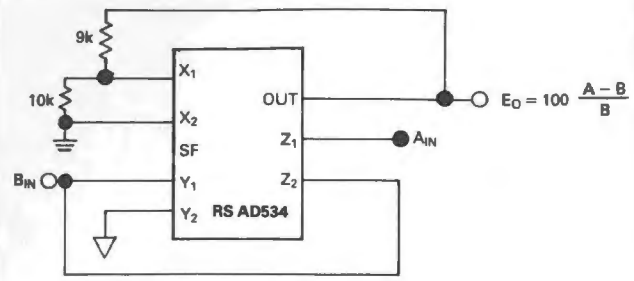


Figure 9 **Percentage computer**

Operation as a square rooter

The operation of the RS AD534 in the square root mode is shown in figure 10. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realised, but operation is restricted to the one quadrant associated with each combination of inputs.

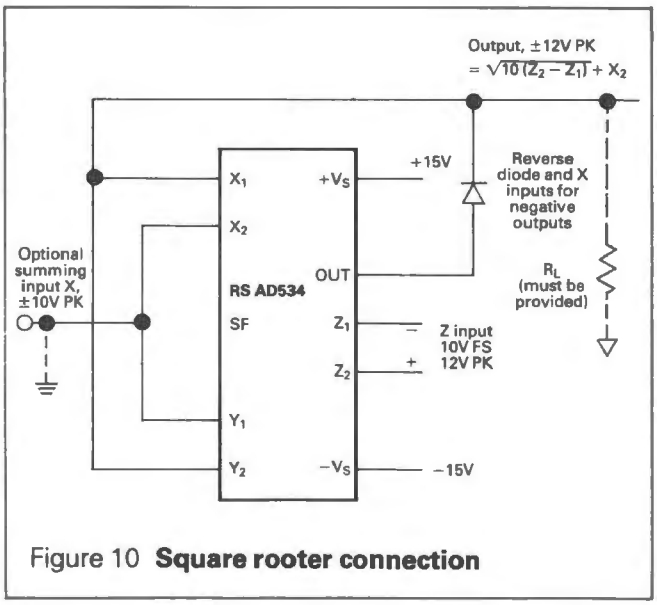


Figure 10 **Square rooter connection**

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the RS AD534 is stable with all loads up to at least 1000pF. For critical applications, a small adjustment to the Z input offset (see Optional Trimming Configuration, page 3) will improve accuracy for inputs below 1V.

Typical Performance Curves (typical at + 25°C, with $V_S = \pm 15V$ dc, unless otherwise stated)

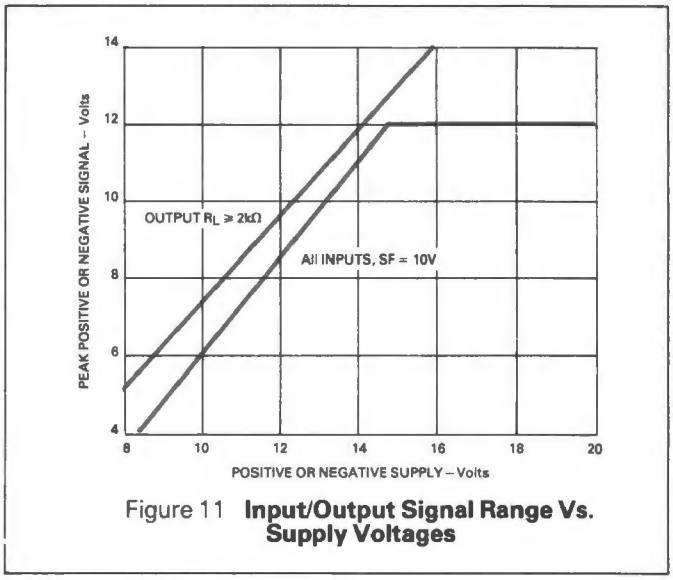


Figure 11 **Input/Output Signal Range Vs. Supply Voltages**

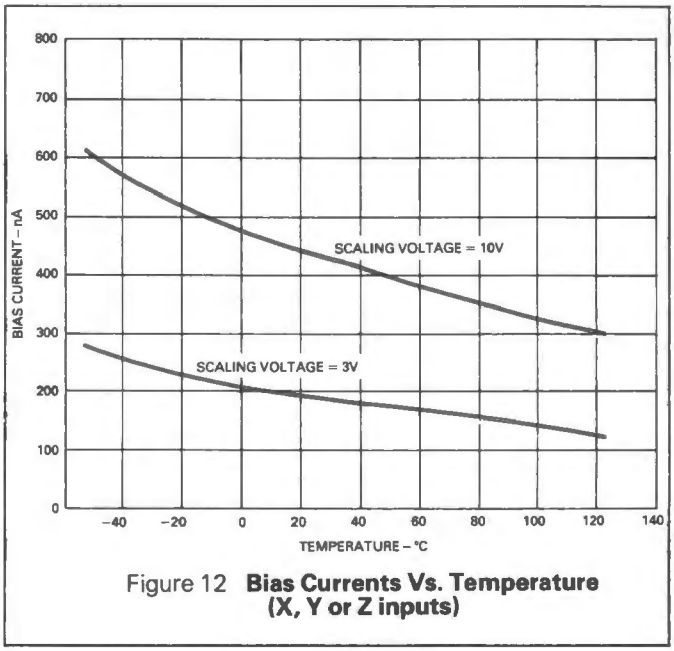


Figure 12 **Bias Currents Vs. Temperature (X, Y or Z inputs)**

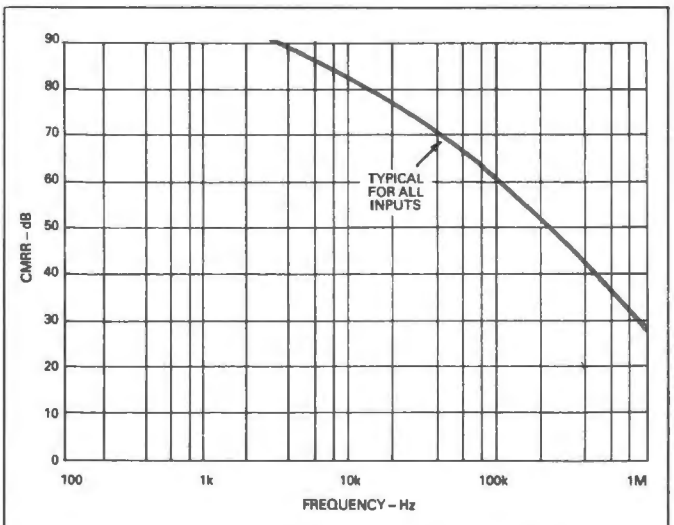


Figure 13 **Common-Mode-Rejection-Ratio Vs. Frequency**

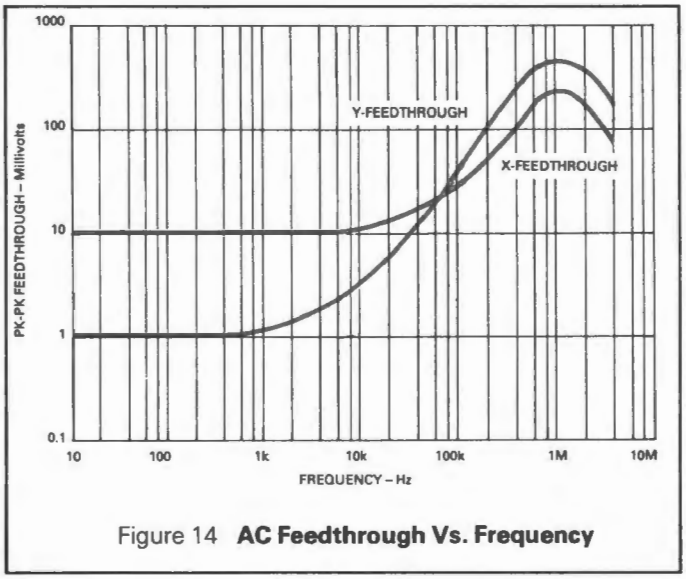


Figure 14 **AC Feedthrough Vs. Frequency**

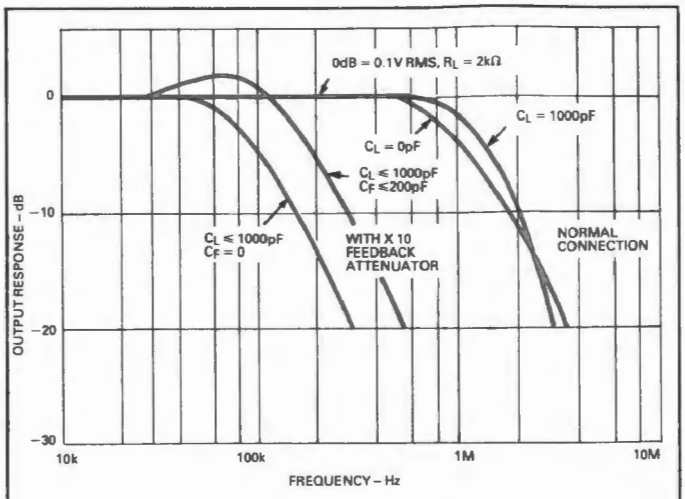


Figure 17 **Frequency Response as a Miltiplier**

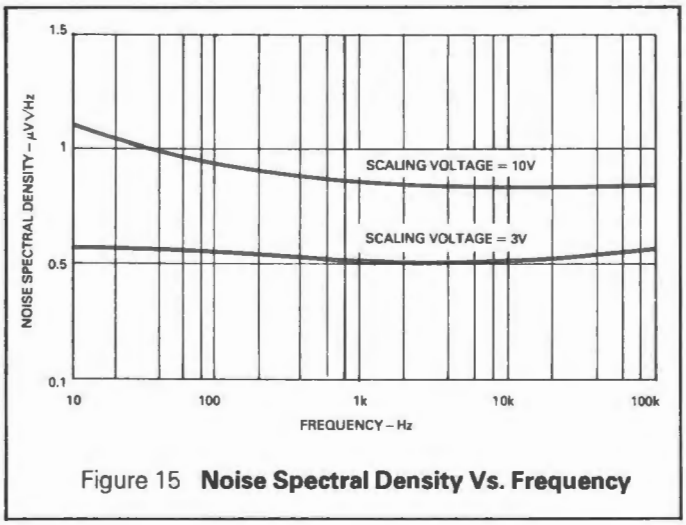


Figure 15 **Noise Spectral Density Vs. Frequency**

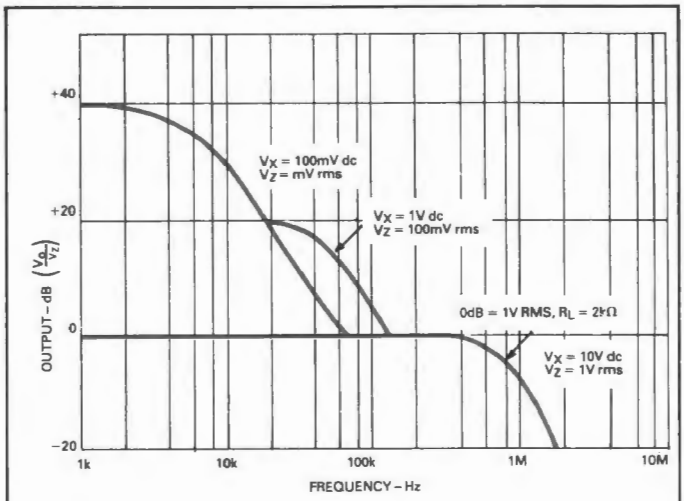


Figure 18 **Frequency Response Vs. Divider Denominator Input Voltage**

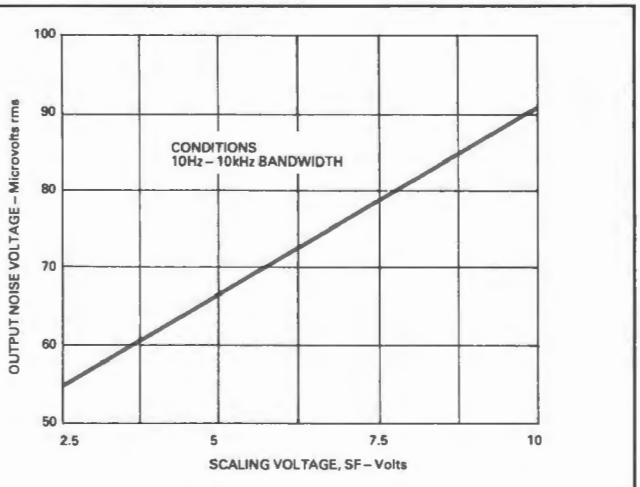


Figure 16 **Wideband Noise Vs. Scaling Voltage**

Applications

Wattmeter

Multipliers are well suited for wattmeter designs. Figure 19 shows a simple arrangement that measures the power output of an audio amplifier into a load. The 18kΩ-10kΩ divider scales the amplifier's output voltage swing to a maximum of 10V (from a maximum of 28V, representing about 100W peak power), well within the RS AD534's input range. The voltage is measured across the load, with the tap of the divider connected to X_1 and the lower end of the load to X_2. The power dissipated in the divider is negligible (1/3500 of the power in the load).

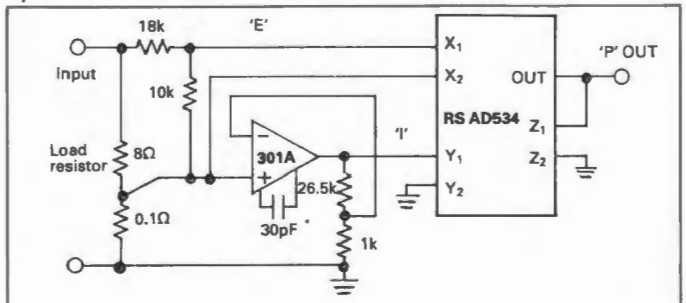


Figure 19 **Wattmeter measures audio-amplifier output power into dummy load**

Current is measured with a 4-terminal, 0.1Ω shunt. The 0.1Ω 'steals' only about 1/80 of the voltage coming out of the amplifier, but the differential voltage measurement ensures that even this small difference between the amplifier output and the load voltage does not affect the measurement of the power dissipated in the load. The RS301A op amp is used to amplify the signal up to manageable levels and to present it to the multiplier's Y input. The output of the multiplier is $(X_1 - X_2)(Y)/10$, which is proportional to the product of load voltage and current, hence the power dissipated in the load.

In practice, the output of the amplifier under test should be connected to the input of the circuit through heavy gauge wire. Connections should be made with soldered lugs to minimise contact resistance, and the load should be a high-wattage-capacity, non-reactive 8Ω resistor. An 8Ω loudspeaker could be used as a load, but the cost of the necessary anechoic chamber or concert hall (to avoid loss of friends in the laboratory – or one's hearing) should be considered. This system can be used to test instantaneous amplifier power into a resistive load as a function of frequency and waveform. With an averaging output, it will test average power. With a loudspeaker, it will determine how much power is delivered to a real load.

Frequency doubling

By use of trigonometric identities that can be found in any mathematical formulary, circuits can be assembled that accept sinusoidal inputs and generate outputs at two, three, four, and five-or-more times the input frequency.

Frequency doubling, in its simplest form, makes use of the identity,

$$\cos 2\theta = 1 - \sin^2\theta$$

Since, for a sine wave, $\theta = \omega t$,

$$\cos 2\omega t = 1 - \sin^2 \omega t$$

If an input E sin ωt, is applied to a multiplier, connected as a squarer, the output will be

$$E_O = 1/20\, E^2 (1 - \cos 2\omega t)$$

The dc term may be eliminated from the output by capacitive coupling, or by applying a bias voltage (which can be done conveniently with the RS AD534). Figure 20 shows a circuit which accepts a sinusoidal signal with a 10V amplitude and produces a double-frequency signal also having a 10V amplitude with no dc offset.

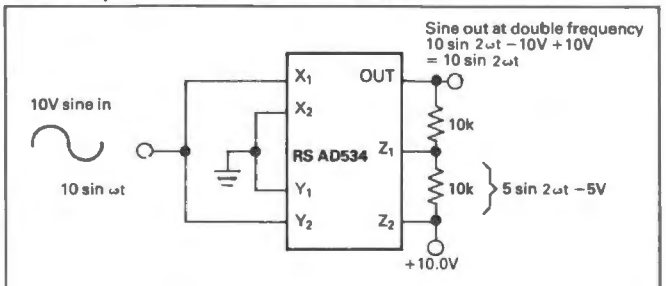


Figure 20 **Frequency doubler**

An obvious problem is that variations of input amplitude result in dc errors at the output. If the output is ac-coupled, abrupt changes of input level cause the output to bounce, which in some applications is troublesome. Figure 21 shows a circuit, using a different trigonometric identity, which produces frequency doubling, at a given frequency, with no dc offset, hence no bounce. It uses the identity:

$$\cos \omega t \sin \omega t = \tfrac{1}{2}\sin 2\omega t$$

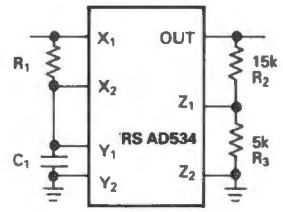


Figure 21 **'No-bounce' frequency doubler**

Bridge linearization

If one arm of Wheatstone bridge varies from its nominal value by a factor, (1 + 2w), the voltage or current output of the bridge will be (with appropriate polarities and scale factors):

$$y = \frac{w}{1+w}$$

Linear response requires very small values of w (to make the denominator essentially independent of w) and, as a consequence, preamplification.

The circuit shown in Figure 22 enables large-deviation bridges to be used without losing linearity or resorting to high attenuation. The circuit computes the inverse of the bridge function, ie:

$$w = \frac{y}{1-y}$$

Depending on which arm of the bridge varies, it may be necessary to reverse the polarity of the X connections.

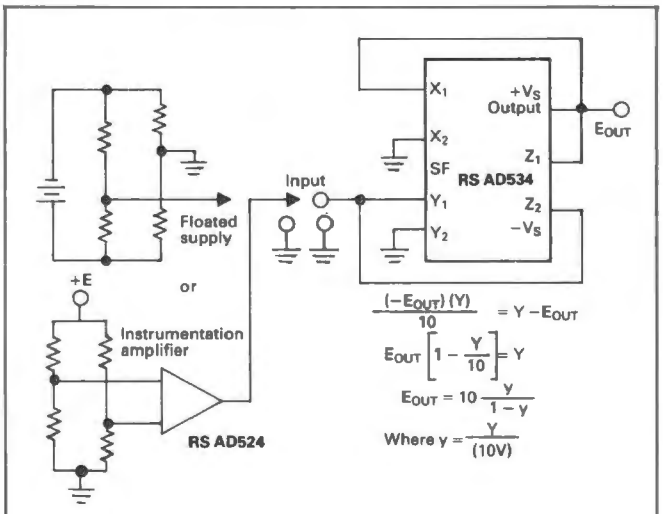


Figure 22 **Bridge-linearization circuit**

Since the input to this circuit is single-ended, the bridge must either float with respect to ground, or the RS AD524AD instrumentation amplifier may be used to translate the bridge output to the RS AD534's common. Any resistive, linearly responding transducer (ie, one or more legs of the bridge proportional to the phenomenon being measured) may profit from the application of this circuit. Examples include position servos, linear thermistors, platinum-resistance-wire sensors (nearly linear over wide ranges), pressure transducers, strain gauges, etc.

RS data

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An Electrocomponents Group Company
Telephone: 0536 201234
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RS data

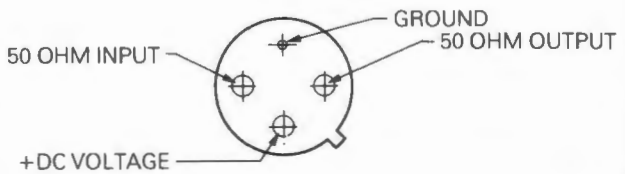
Cascadable r.f. amplifier RS EA5

Stock number 302-435

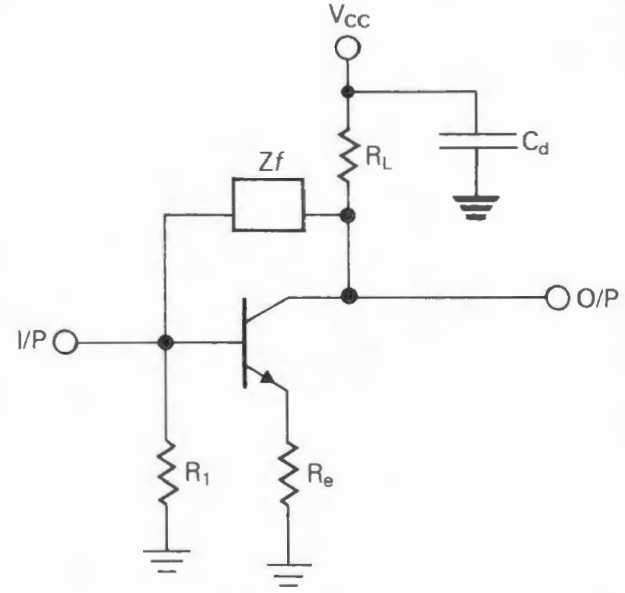
The RS EA5 is designed to bring the repeatability, stability and ease of use of thin film processing to an RF amplifier application. Each amplifier can be thought of as a gain block which the designer can employ in a system approach to amplifier design. Since these units are unconditionally stable, exceptionally flat and provide a good 50 ohm interface, they may be easily cascaded in a 50 ohm microstrip circuit without loss of gain, power output or bandwidth.

Features

- Versatile
- Medium output level (+7dBm typ)
- Small size
- 50 ohm
- Cascadable
- Broad band
- 13dB gain



Pin connection diagram



Internal circuit representation

Absolute maximum ratings

Ambient operating temperature	−54°C to +100°C
Storage temperature	−62°C to +125°C
Maximum case temperature	125°C
Maximum dc voltage	+17 Volts
Maximum cw input power	+50 Milliwatts
Maximum peak power	0.5 Watt (3μsec max)

Electrical characteristics (Measured in a 50 ohm system)

Characteristic	0-50°C	Typ.	−54°C to +85°C	Units
Frequency	5-400 (Min.)		5-400 (Min.)	MHz
Small Signal Gain	13.0 (Min.)		12.5 (Min.)	dB
Gain Flatness	<±0.3 (Typ.)			dB
Noise Figure	5.7 (Typ.)			dB
Power Output at 1 dB Compression	+9 (Typ.) +6.5 (Min.)		+6.0 (Min.)	dBm
VSWR Input/Output	<1.8:1 (Typ.)			
Second Order Harmonic Intercept Point		+33		dBm
Second Order Two Tone Intercept Point		+28		dBm
Third Order Two Tone Intercept Point		+21		dBm
DC Volts (nominal)		15		V
DC Current at 15V		24		mA

Introduction

Each RS EA5 is a complete cascadable amplifier including stable biasing circuitry and an internal RC filter network to provide power supply decoupling. Designed to work from a 15 volt supply, these modules offer stable and repeatable performance over a very broad range of frequencies enabling the designer to concentrate on the complexities of the system without worrying about the intricacies of the RF transistor amplifier design.

Performance Parameters – Cascading Rules

The following are a few simple rules to use when cascading these amplifiers.

Gain

The typical cascaded gain will be the sum of the individual unit typical gains. The overall gain specification should not exceed the sum of the minimum gains as specified for each unit.

Frequency Response

Each cascadable amplifier is flat across the frequency band specified to within ± 0.3 dB. The cascaded frequency response for up to 4 units will be typically less than ± 1.0 dB. However, for a conservative specification, ± 1.5 dB should be used when the full band width is required.

Additionally as no input or output coupling capacitors are included internal to the device the low frequency response may be extended. Figure 1 shows the frequency response for one amplifier obtained when 50nF coupling capacitors are used.

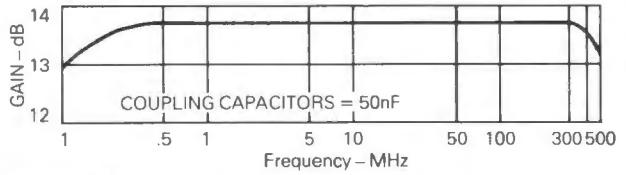


Figure 1 **Frequency response**

Cascaded Noise Figure

The overall noise figure measured at the input amplifier of a cascade will increase due to the second stage contribution. The overall noise figure of a cascade can be calculated using the following equation:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \ldots\ldots\ldots \frac{F_n - 1}{G_1 G_2 \ldots\ldots\ldots G_{n-1}}$$

Where Fn is the noise figure of the nth stage and Gn is the gain of the nth stage. (All terms are numeric ratios and not in units of dB.)

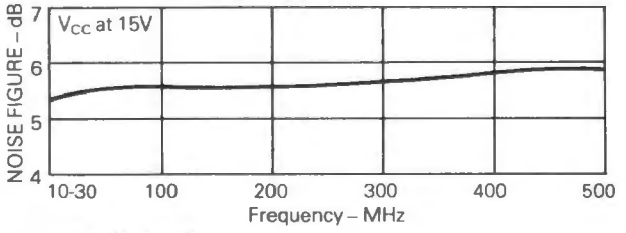


Figure 2 **Noise Figure**

Figure 2 shows how the noise figure varies across the band for one individual amplifier.

Impedance

The RS EA5 cascadable amplifier is designed for 50 ohm input and output by using internal collector base and emitter resistive feedback. In addition, LC matching and reactive feedback compensation are used to obtain matching at the high end of the band. The impedance is between 40 and 60 ohms and is essentially resistive below 1½ octaves from the high end of the band.

Voltage Standing Wave Ratio

The VSWR is specified at a maximum of 2.0:1. The cascaded VSWR will be typically less than 2.0:1 across the entire band but can be greater than 2.0:1 in certain cases. About 1½ octaves below the high end of the band there is virtually no degradation when cascading, and the 2.0:1 cascading specification is easily achieved. Across the band VSWR for a single device is shown in figure 3.

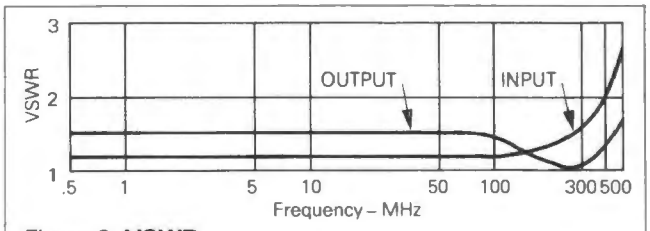


Figure 3 **VSWR**

Output Power

When cascading these amplifiers there is no degradation in output power of the last stage provided, of course, the driver stage supplies sufficient power.

The output power of a single amplifier is measured using a 50 ohm source and a 50 ohm load and is shown in figure 4. The output power of a driving stage can be affected by the load impedance (input impedance of the next stage). This can cause some minor differences to occur that are not fully explained by considering compression alone. In general, if the effective load presented to the driver stage is greater than 50 ohms, then more output power can be obtained from the driver stage. Conversely, if the load presented is less than 50 ohms, then a reduction may result.

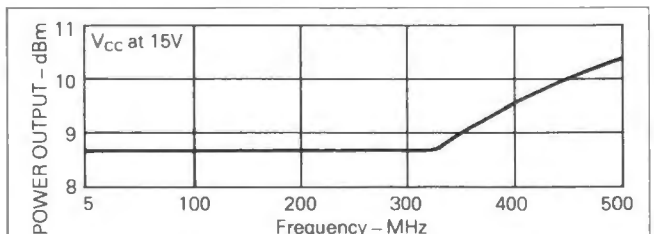


Figure 4 **Power Output at 1 dB Gain Compression**

Phase Linearity and Group Delay

The RS EA5 cascadable amplifier offers excellent linearity and relatively constant group delay because of the thin film integrated construction. Phase linearity is the best fit straight line to the phase response curve and is expressed in degrees deviation. Tables of deviation from linear phase, gain and group delay are shown in table 1.

Freq MHz	Mag	S11 Ang	Mag	S21 Ang	Mag	S12 Ang	Mag	S22 Ang
100	.10	−85.5	4.84	−166.9	.08	37.1	.21	13.9
200	.15	−77.9	4.86	−154.0	.09	67.1	.12	46.7
300	.23	−45.5	4.86	−142.4	.10	96.6	.03	74.0
400	.40	−37.1	4.73	−133.7	.11	121.9	.14	−93.8
500	.48	−17.8	4.52	−121.9	.11	147.1	.26	−86.6
600	.58	6.8	4.06	−110.4	.11	171.8	.31	−87.9

Table 1 **Deviation from Linear Phase, Gain and Group Delay**

The cascaded phase linearity will be equal to or less than the sum of the individual stage linearity. The group delay is defined as the rate of change of phase shift versus frequency $\frac{(d\theta)}{(d\omega)}$

The group delay is calculated by taking the phase difference over a given frequency band and then dividing by that frequency band. Both the phase and frequency are in radians. The group delay can be expressed in units of time by the mathematical relationship:

$$t_d \text{ (seconds)} = \frac{\text{Phase (degrees)}}{\text{Frequency } (H_z) \times 360^\circ}$$

Mounting Instructions

In common with normal r.f. practice this amplifier must be used in conjunction with a microstrip circuit board using 50 ohm input and output connections together with a good r.f. ground plane.

To achieve maximum cascaded gain, gain flatness and to realise the inherent stability provided in each unit, it is very important to assure good rf grounding between the case and the ground plane.

The case should make intimate contact with the ground plane prior to soldering the pins. For greater assurance in making ground contact each RS EA5 is supplied with an accessory kit that should be assembled as shown in figure 6.

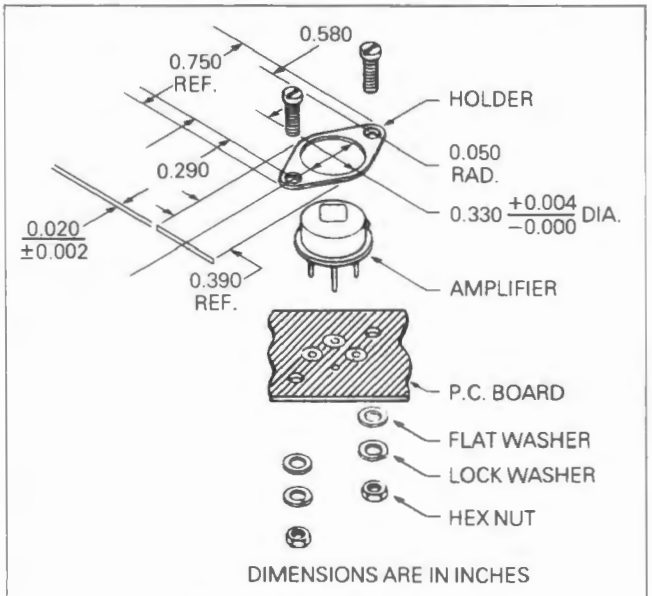


Figure 6 **Mounting instructions**

RS data

R.S. Components Ltd. 13-17 Epworth Street, London, EC2P 2HA Telephone: 01-253 1222 or 01-250 4000
An Electrocomponents Group Company

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RS data

Dual Switched Capacitor Filter I.C.

Stock number 302-407

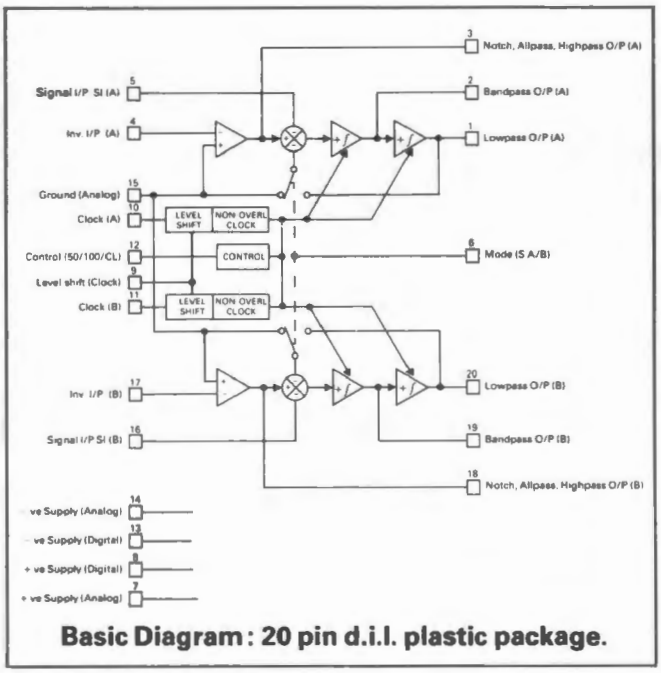
The RS MF10 consists of two independent general purpose active filter building blocks fabricated in CMOS technology.
Using switched capacitor techniques this integrated circuit can produce various second order filter functions using only three or four resistors and an external clock. Alternatively the two halves can be combined in cascade to provide third and fourth order functions and functions of order greater than four may be obtained by cascading several MF10 packages.

Features

- Easy to use
- Functions set by only three to four resistors and an external clock
- Operation up to 20kHz
- Filter cut-off frequency stability directly dependent on the external clock quality
- Low sensitivity to component variations
- Separate high pass (or notch or allpass), bandpass, lowpass outputs
- $f_o \times Q$ range up to 200kHz
- Cascadable for higher order filters

Absolute maximum ratings

Supply voltage ..... ± 7V
Power dissipation ..... 500 mW
Operating temperature ..... 0°C to 70°C
Storage temperature ..... 150°C
Lead temperature (soldering, 10 seconds) ..... 300°C



Basic Diagram: 20 pin d.i.l. plastic package.

Electrical characteristics (Complete filter) $V_S = \pm 5V$, $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Frequency range	$f_o \times Q < 200$kHz	20	30		kHz
Clock to centre frequency ratio, f_{CLK}/f_o	Pin 12 high, $Q = 10$, $f_o \times Q <$ 50kHz, Mode 1		49.94 ± 0.2%	±1.5%	
	Pin 12 at mid supplies $Q = 10$, $f_o \times Q <$ 50kHz, Mode 1		99.35 ± 0.2%	±1.5%	
Q accuracy (Q deviation from an ideal continuous filter)	Pin 12 high, Mode 1, $f_o \times Q <$ 100kHz, $f_o <$ 5kHz		± 2	± 6	%
	Pin 12 at mid supplies $f_o \times Q <$ 100kHz, $f_o <$ 5kHz, Mode 1		± 2	± 6	%
f_o Temperature coefficient	Pin 12 high (~50:1)		± 10		ppm/°C
	Pin 12 mid supplies (~100:1) $f_o \times Q <$ 100 kHz, Mode 1		± 100		ppm/°C
	External clock temperature independent				

(continued from previous page)

Q Temperature coefficient	$f_o \times Q < 100$ kHz, Q setting Resistors temperature independent		±500		ppm/°C
DC Low Pass Gain Accuracy	Mode 1, R1 = R2 = 10k			±2	%
Crosstalk			50		dB
Clock Feedthrough			10		mV
Maximum Clock Frequency		1	1.5		MHz
Power Supply Current			8	10	mA

Electrical characteristics (Internal Op Amps) $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Supply voltage		±4	±5		V
Voltage Swing (Pins 1, 2, 9, 20)	$V_S = \pm 5V$, $R_L = 5k$	±3.2	±3.7		V
Voltage Swing (Pins 3 and 18)	$V_S = \pm 5V$, $R_L = 3.5k$	±3.2	±3.7		V
Output Short Circuit Current	$V_S = \pm 5V$				
Source			3		mA
Sink			1.5		mA
Op Amp Gain BW Product			2.5		MHz
Op Amp Slew Rate			7		V/μs

Introduction to the switched capacitor

Consider the basic switched capacitor circuit shown in Figure 1.

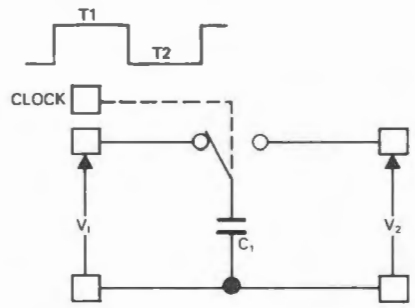


Figure 1 **A basic switched capacitor circuit.**

During time T_1 capacitor C_1 charges to V_1. In the next part of the clock cycle the switch changes over causing capacitor C_1 to discharge to V_2. The total charge transferred in one complete clock cycle ($T_1 + T_2$) is:

$$Q = C_1 (V_1 - V_2)$$

This process continues with a repetition time of $T_1 + T_2$ causing an average current (i) of:

$$i = \frac{Q}{T_1 + T_2} = \frac{C_1 (V_2 - V_1)}{(T_1 + T_2)}$$

By using Ohm's law. Where $i = \frac{v}{r}$

$$\frac{i}{(V_2 - V_1)} = \frac{I}{r} = \frac{C_1}{(T_1 + T_2)}$$

$$r = \frac{T_1 + T_2}{C_1} = \frac{1}{C_1 \times f\,clk}$$

i.e. r appears as a resistance between input and output of value that is tunable by the clock frequency.

A switched capacitor integrator

A simple linear integrator circuit is shown in Figure 2 with the associated output waveform following application of an input step voltage. The time constant is given by:

$$\tau = R_1 C_2$$

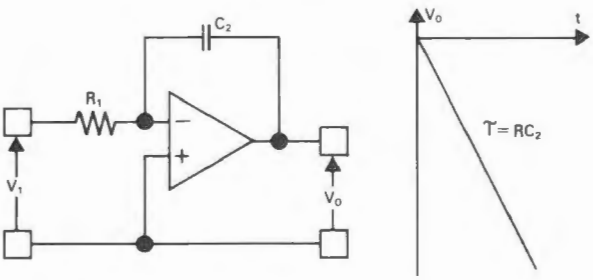


Figure 2 **A simple linear integrator.**

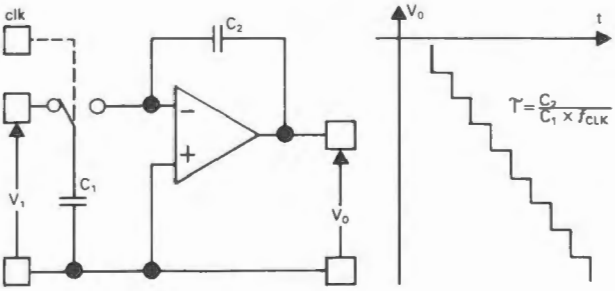


Figure 3 **A switched capacitor integrator.**

If a switched capacitor circuit is used in place of R_1 as shown in Figure 3 an integrator with time constant proportional to the capacitor ratio $\left(\frac{C_2}{C_1}\right)$ and inversely proportional to the clock frequency is produced.

$$\tau = \frac{C_2}{C_1} \times \frac{1}{f\,clk.}$$

The MF10 dual switched capacitor filter IC

The MF10 uses two non-inverting switched capacitor integrators in each channel together with all of the necessary active and reactive components to construct two complete 2nd order state variable type active filters. This enables the centre or break frequency together with the Q and gain to be set using an external clock and three to four resistors.

To keep the device as universal as possible, the outputs of each section of each filter are brought out. This allows designs for all five filtering functions: lowpass, bandpass, highpass, allpass and band reject or notch filters. With two independent 2nd order sections in one package, cascading to achieve 4th order responses can easily be accomplished. Additionally, any of the classical filter response types such as Butterworth, Chebyshev, Bessel and Cauer can be implemented.

A clock with close to 50% duty cycle is required to control the resonant frequency of the filter. Either TTL or CMOS logic compatible clocks can be accommodated, whether the MF10 is powered from split supplies or a single supply, by simply grounding the level shift (L Sh) control pin.

The resonant frequency of each filter is directly controlled by its clock. A tri-level control pin sets the ratio of the clock frequency to the centre frequency (the 50/100/CL pin) for both halves. When this pin is tied to V^+ the centre frequency will be 1/50 of the clock frequency. When tied to mid-supply potential (i.e., ground, when biased from split supplies) provides 100 to 1 clock to centre frequency operation. When this pin is tied to V^- a power saving supply current limiter shuts down operation and rolls back the supply current by 70%.

Filter centre frequency accuracy and stability are only as good as the clock provided. Standard crystal oscillators, combined with digital counters, can provide very stable clocks for specific filter frequencies.

The MF10 is intended for use with centre frequencies up to 20kHz, and is guaranteed to operate with clocks up to 1MHz. This means that for centre frequencies greater than 10kHz, the 50 to 1 clock control should be used. The effect of using 100 to 1 or 50 to 1 clock to centre frequency ratio manifests itself in the number of 'stair-steps' apparent in the output waveform. The MF10 closely approximates the time and frequency domain response of continuous filters (RC active filters, for example) but does so using sampling techniques. The clock to centre frequency control determines the number of samples taken (1 per clock cycle) in one cycle of the centre frequency. For most audio applications, the audible effects of these step edges and the clock frequency component in the output are negligible as they are beyond 20kHz. To obtain a cleaner output waveform, a simple passive RC lowpass can be added to the output to serve as a smoothing filter without affecting the MF10 filtering action.

Several of the modes of operation (discussed in a later section) allow altering of the clock to centre frequency ratio by an external resistor ratio. This can be used to obtain centre frequencies of values other than 1/50 or 1/100 of the clock frequency. In multiple stage, staggered tuned filters, the centre frequency of each stage can be set independently with resistors to allow the overall filter to be controlled by just one clock frequency.

All of the rules of sampling theory apply when using the MF10. The sampling rate, or clock frequency, should be at least twice the maximum input frequency to produce the best equivalent to a continuous time filter. High frequency components in the input signal that approach the clock frequency will generate beat frequency signals which appear at the output of the lower frequency filter and are indistinguishable from valid passband signals. Bandlimiting the input signal to attenuate these potential beat frequencies is the best preventive measure. In most applications, beat frequencies will not be a problem as the clock frequency is much higher than the passband of interest. In the event that a much higher clock frequency is required, the modes of operation which utilize external resistor ratios to increase the clock to centre frequency ratio can extend the clock frequency to greater than 100 times the centre frequency. By using a higher clock frequency, the beat frequencies are correspondingly higher. The limiting factor, with regard to increasing the clock to centre frequency ratio, has to do with increased DC offsets at the various outputs.

The basic filter configurations

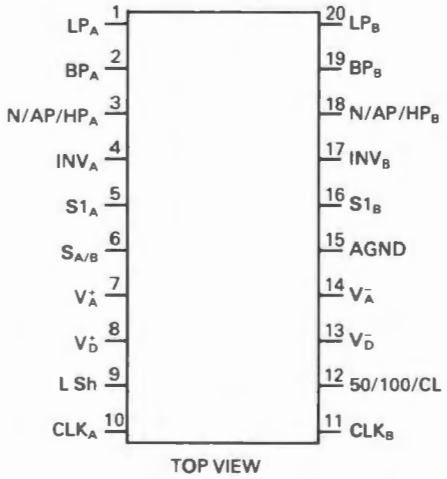
There are six basic configurations (or modes of operation) for the 2nd order sections in the MF10 to realise a wide variety of filter responses. In all cases, no external capacitors are required. Design is a simple matter of establishing a few resistor ratios to set the desired passband gain and Q and generating a clock for the proper resonant frequency. Each 2nd order section can be treated in a modular fashion, with regard to individual centre frequency, Q and gain, when cascading either the two sections within a package or several packages for very high order filters. This individuality of sections is important in implementing the various response characteristics such as Butterworth, Chebyshev, etc.

The following is a general summary of design hints common to all modes of operation.

1) The maximum supply voltage for the MF10 is ± 7V or just $+14$V for single supply operation. The minimum supply to properly bias the device is $+8$V (± 4V).
2) The maximum swing at any of the outputs is typically within 1V of either supply rail.
3) The internal op amps can source 3mA and sink 1.5mA. This is an important criterion when selecting a minimum resistor value.
4) The maximum clock frequency is typically 1.5MHz.
5) To insure the proper filter response, the $f_o \times Q$ product of each stage must be realisable by the MF10. For centre frequencies less than 5kHz, the $f_o \times Q$ product can be as high as 300kHz (Q must be less than or equal to 150). A 3kHz bandpass filter, for example, could have a Q as high as 100 with just one section. For centre frequencies less than 20kHz, the allowable $f_o \times Q$ product is limited to 200kHz. A 10kHz bandpass design using a single section should have a Q no larger than 20.

6) Centre frequency matching from part to part for a given clock frequency is typically ±0.2%. Centre frequency drift with temperature (excluding any clock frequency drift) is typically ±10ppm/°C with 50:1 switching and ±100ppm/°C for 100:1.
7) Q accuracy from part to part is typically ±2% with a temperature coefficient of ±500ppm/°C.
8) The expressions for circuit dynamics given with each of the modes are important. They determine the voltage swing at each output as a function of the circuit Q. A high Q bandpass design can generate a significant peak in the response at the lowpass output at the centre frequency.
9) Both sides of the MF10 are independent, except for supply voltages, analogue ground, clock to centre frequency ratio setting and internal switch setting for the three input summing stage.

Connection diagram



TOP VIEW

Pin description

LP, BP, N/AP/HP — These are the lowpass, bandpass, notch or allpass or highpass outputs of each 2nd order section. The LP and BP outputs can sink typically 1mA and source 3mA. The N/AP/HP output can typically sink and source 1.5mA and 3mA, respectively.

INV — This is the inverting input of the summing op amp of each filter. The pin has static discharge protection.

S1 — S1 is a signal input pin used in the allpass filter configurations (see modes of operation 4 and 5). The pin should be driven with a source impedance of less than 1kΩ.

$S_{A/B}$ — It activates a switch connecting one of the inputs of the filter's 2nd summer either to analog ground ($S_{A/B}$ low to V_A^-) or to the lowpass output of the circuit ($S_{A/B}$ high to V_A^+). This allows flexibility in the various modes of operation of the IC. $S_{A/B}$ is protected against static discharge.

V_A^+, V_D^+ — Analog positive supply and digital positive supply. These pins are internally connected through the IC substrate and therefore V_A^+ and V_D^+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.

V_A^-, V_D^- — Analog and digital negative supply respectively. The same comments as for V_A^+ and V_D^+ apply here.

L Sh — Level shift pin; it accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the MF10 can be driven with CMOS clock levels (±5V) and the L Sh pin should be tied either to the system ground or to the negative supply pin. If the same supplies as above are used but TTL clock levels, derived from 0V to 5V supply, are only available, the L Sh pin should be tied to the system ground. For single supply operation (0V and 10V) the V_D^-, V_A^- pins should be connected to the system ground, the AGND pin should be biased at 5V and the L Sh pin should also be tied to the system ground. This will accommodate both CMOS and TTL clock levels.

CLK (A or B) — Clock inputs for each switched capacitor filter building block. They should both be of the same level (TTL or CMOS). The level shift (L Sh) pin description discusses how to accommodate their levels. The duty cycle of the clock should preferably be close to 50% especially when clock frequencies above 200kHz are used. This allows the maximum time for the op amps to settle which yields optimum filter operation.

50/100/CL — By tying the pin high a 50:1 clock to filter centre frequency operation is obtained. Tying the pin at mid supplies (i.e., analog ground with dual supplies) allows the filter to operate at a 100:1 clock to centre frequency ratio. When the pin is tied low, a simple current limiting circuitry is triggered to limit the overall supply of current down to about 2.5mA. The filtering action is then aborted.

AGND — Analog ground pin; it should be connected to the system ground for dual supply operation or biased at mid supply for single supply operation. The positive inputs of the filter op amps are connected to the AGND pin so 'clean' ground is mandatory. The AGND pin is protected against static discharge.

Definition of terms

f_{CLK}: the switched capacitor filter external clock frequency.

f_o: centre of frequency of the second order function complex pole pair. f_o is measured at the bandpass output of each 1/2 MF10, and it is the frequency of the bandpass peak occurrence (Figure 4).

Q: quality factor of the 2nd order function complex pole pair. Q is also measured at the bandpass output of each 1/2 MF10 and it is the ratio of f_o over the −3dB bandwidth of the 2nd order bandpass filter, Figure 4. The value of Q is not measured at the lowpass or highpass outputs of the filter, but its value relates to the possible amplitude peaking at the above outputs.

H_{OBP}: the gain in (V/V) of the bandpass output at f = f_o.

H_{OLP}: the gain in (V/V) of the lowpass output of each 1/2 MF10 at f → 0Hz, Figure 5.

H_{OHP}: the gain in (V/V) of the highpass output of each 1/2 MF10 as f → $f_{CLK}/2$, Figure 6.

Q_z: the quality factor of the 2nd order function complex zero pair, if any. (Q_z is a parameter used when an allpass output is sought and unlike Q it cannot be directly measured.)

f_z: the centre frequency of the 2nd order function complex zero pair, if any. If f_z is different from f_o, and if the Q_z is quite high it can be observed as a notch frequency at the allpass output.

f_{notch}: the notch frequency observed at the notch output(s) of the MF10.

H_{ON_1}: the notch output gain as f → 0Hz.

H_{ON_2}: the notch output gain as f → $f_{CLK}/2$.

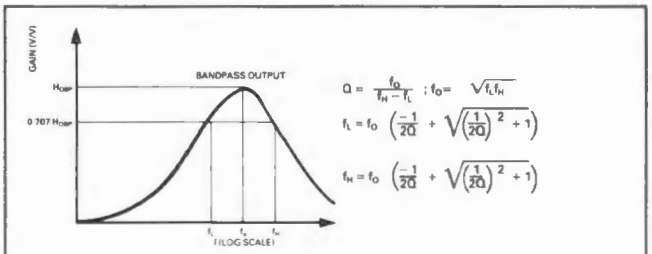


Figure 4

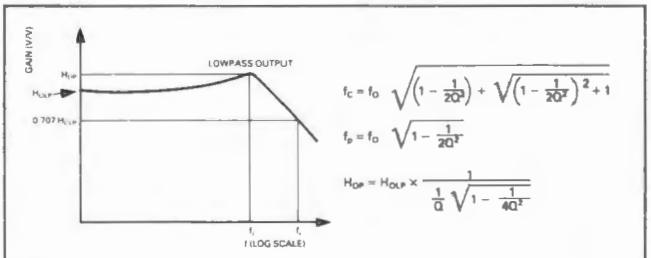


Figure 5

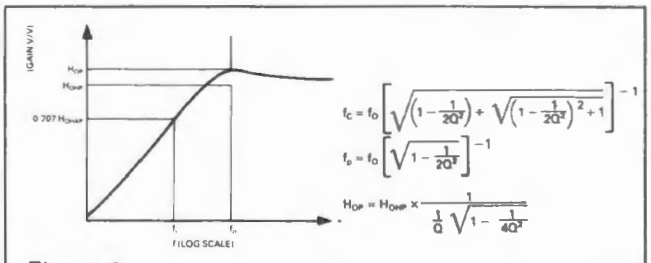


Figure 6

Mode 1a

A configuration that gives good output dynamics together with the provision for high Q in bandpass designs. The notch output features equal gain above and below the notch frequency.

Design equations

Outputs — Notch
Bandpass
Lowpass

f_o = centre frequency of the complex pole pair

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

f_{notch} = centre frequency of the imaginary zero pair

$= f_o$.

H_{OLP} = Lowpass gain (as f → 0) $= -\frac{R_2}{R_1}$

H_{OBP} = Bandpass gain (at f = f_o) $= -\frac{R_3}{R_1}$

$H_{ON_1} = H_{ON_2} = -\frac{R_2}{R_1}$

$Q = f_o/BW = \frac{R_3}{R_2}$

Circuit dynamics

$H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q$

$H_{OLP\ (Peak)} = Q \times H_{OLP}$ (If the DC gain of LP output is too high, a high Q value could cause clipping at the lowpass output resulting in gain non-linearity and distortion at the bandpass output.)

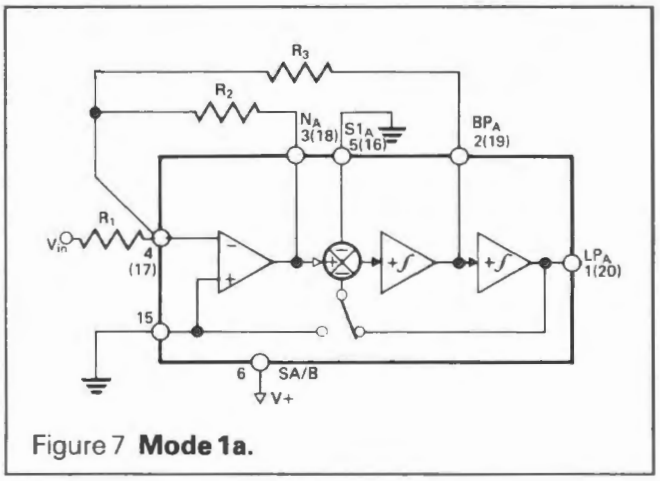


Figure 7 **Mode 1a.**

Mode 1b

A variation of Mode 1a in which the notch output is replaced by a second (non-inverting) bandpass output. This is a minimum external component configuration (only 2 resistors) useful for low Q lowpass and bandpass applications. The non-inverting bandpass output is necessary for minimum phase filter designs.

Design Equations

Outputs — Bandpass (non-inv)
Bandpass
Lowpass

$f_o = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

$Q = \frac{R_3}{R_2}$

$H_{OLP} = -1$

$H_{OPB_1} = -\frac{R_3}{R_2}$

H_{OBP_2} = 1 (non-inverting)

Circuit dynamics

$H_{OBP_1} = Q$ (This is the reason for the low Q recommendation)

$H_{OLP\ (Peak)} \simeq Q \times H_{OLP}$ (For high Qs)

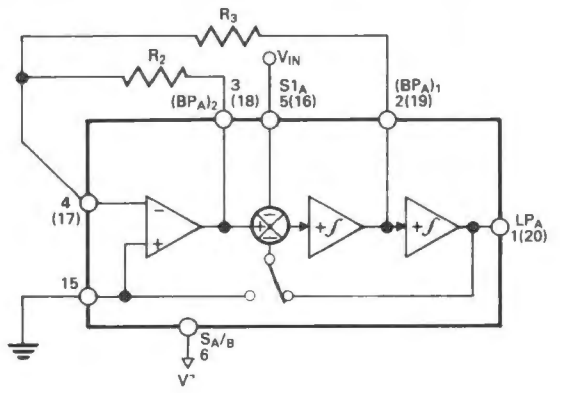


Figure 8 **Mode 1b.**

Mode 2

This mode allows tuning of the clock frequency to centre frequency ratio to be values greater than 100:1 or 50:1. The notch output is useful for designing elliptic highpass filters because the frequency of the required complex zeros (f notch) is less than the frequency of the complex poles (f_o).

Design Equations

Outputs — Notch
Bandpass
Lowpass

(N.B. Notch frequency is lower than the bandpass centre frequency.)

f_o = centre frequency

$$= \frac{f_{CLK}}{100}\sqrt{\frac{R_2}{R_4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_2}{R_4}+1}$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R_2/R_4+1}{R_2/R_3}}$$

H_{OLP} = Lowpass output gain (as $f \rightarrow 0$)

$$= -\frac{R_2/R_1}{R_2/R_4+1}$$

H_{OBP} = Bandpass output gain (at $f = f_o$) $= -R_3/R_1$

H_{ON_1} = Notch output gain (as $f \rightarrow 0$)

$$= -\frac{R_2/R_1}{R_2/R_4+1}$$

H_{ON2} = Notch output gain as $f \rightarrow \frac{f_{CLK}}{2} = -\frac{R_2}{R_1}$

Circuit dynamics

$$H_{OBP} = Q\sqrt{H_{OLP} \times H_{ON_2}} = Q\sqrt{H_{ON1} \times H_{ON2}}$$

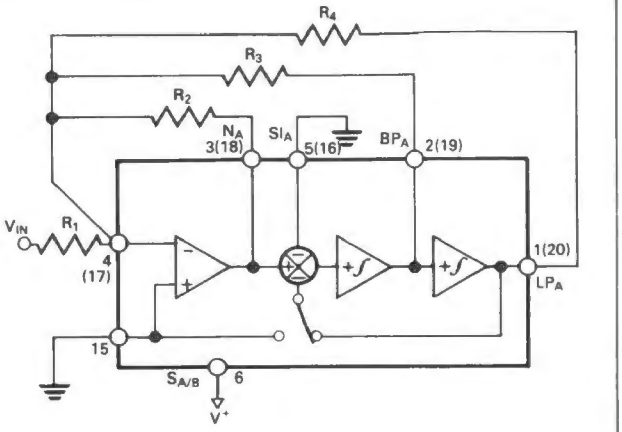


Figure 9 **Mode 2.**

Mode 3a

The most versatile mode of operation, this configuration is the classical state variable filter implemented with only 4 external resistors.

Clock to centre frequency ratio can be externally tuned either above or below the 100:1 or 50:1 values and thus make it suitable for multiple stage Chebyshev filters controlled by a single clock.

Design Equations

Outputs — Highpass
Bandpass
Lowpass

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R_2}{R_4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R_2}{R_4}}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R_2}{R_4}} \times \frac{R_3}{R_2}$$

$$H_{OHP} = \text{Highpass gain as} \left(f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R_2}{R_1}$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_o) = -\frac{R_3}{R_1}$$

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\frac{R_4}{R_1}$$

Circuit dynamics

$$\frac{R_2}{R_4} = \frac{H_{OHP}}{H_{OLP}}$$

$$H_{OBP} = Q \times \sqrt{H_{OHP} \times H_{OLP}}$$

$H_{OLP\ (peak)} = Q \times H_{OLP}$ (for high Qs)

$H_{OHP\ (peak)} = Q \times H_{OHP}$ (for high Qs)

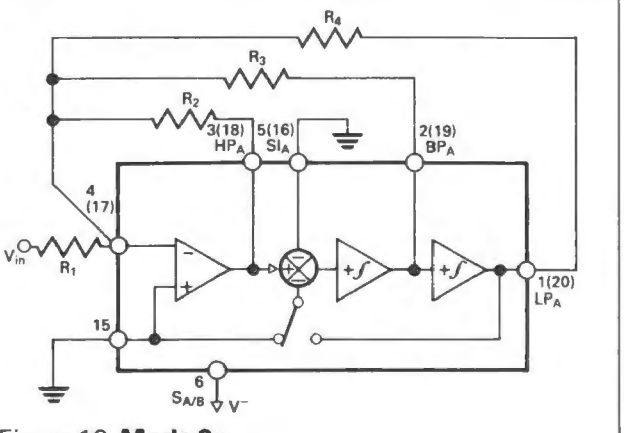


Figure 10 **Mode 3a.**

Mode 3b

Similar to mode 3a; however a notch output is created by summing the highpass and lowpass outputs with an external op-amp. The ratio of the summing resistors R_h and R_i adjusts the notch frequency independent of the centre frequency. For elliptic filter designs, each stage combines a complex pole pair (at f_o) with a complex zero pair (at f notch) and this configuration provides easy tuning of each of these frequencies for any response type.

When cascading several stages of the MF10 the external op-amp is only needed at the final output stage. The summing junction for the intermediate stages can be the inverting input of the MF10 internal op-amp.

Design Equations

Outputs — Highpass
Bandpass
Lowpass
Notch (With External Op-Amp)

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R_2}{R_4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R_2}{R_4}}$$

$$Q = \sqrt{\frac{R_2}{R_4}} \times \frac{R_3}{R_2}$$

$$H_{OHP} = -\frac{R_2}{R_1}$$

$$H_{OBP} = -\frac{R_3}{R_1}$$

$$H_{OLP} = -\frac{R_4}{R_1}$$

$$f_n = \text{notch frequency} = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_i}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_i}}$$

$$H_{ON} = \text{gain of notch at } f = f_o = \left| Q\left(\frac{R_g}{R_i} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)\right|$$

$$H_{ONi} = \text{gain of notch (as } f \to 0) = \frac{R_g}{R_i} \times H_{OLP}$$

$$H_{ONh} = \text{gain of notch as } f \to \frac{f_{CLK}}{2} = \frac{R_g}{R_h} \times H_{OHP}$$

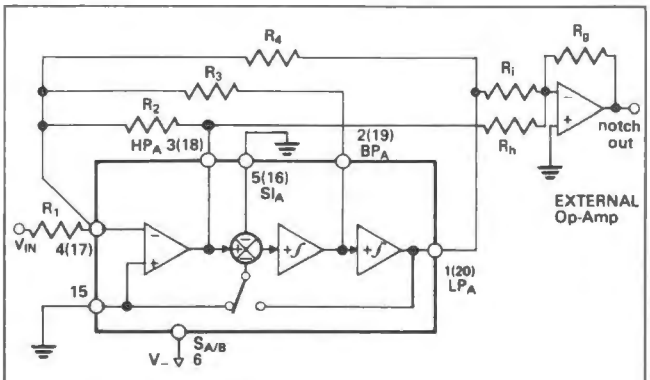


Figure 11 **Mode 3b.**

Mode 4

Utilising the SI_A (SI_B) terminal as a signal input an allpass function can be obtained. An allpass can provide a linear phase change with frequency which results in a constant time delay. This configuration restricts the gain at the allpass output to unity but exhibits slight peaking around f_o.

Design Equations

Outputs — Allpass
Bandpass
Lowpass

f_o = centre frequency

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50};$$

f_z^* = centre frequency of the complex zero pair $\simeq f_o$

$$Q = \frac{f_o}{BW} = \frac{R_3}{R_2};$$

Q_z = quality factor of complex zero pair $= \frac{R_3}{R_1}$

For AP output make $R_1 = R_2$

$$H_{OAP} = \text{Allpass gain}\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R_2}{R_1} = -1$$

$$H_{OLP} = \text{Lowpass gain (as } f \to 0) = -\left(\frac{R_2}{R_1} + 1\right) = -2$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_o) = -\frac{R_3}{R_2}\left(1 + \frac{R_2}{R_1}\right) = -\left(2\frac{R_3}{R_2}\right)$$

Circuit dynamics

$$H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)\, Q$$

* Due to the sampled data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4 dB peaking around f_o of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

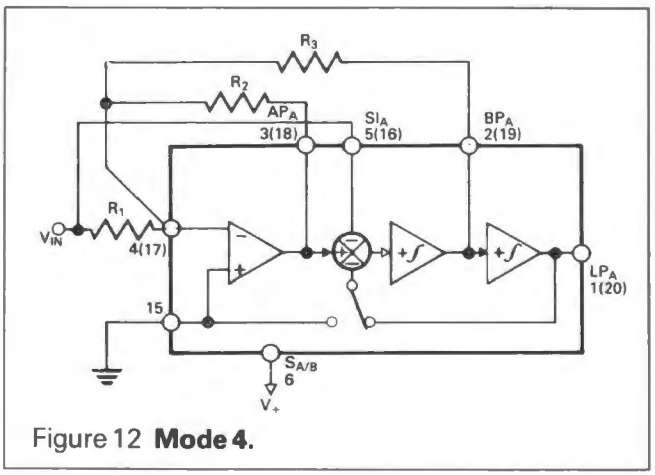


Figure 12 **Mode 4.**

Mode 5

Featuring an improved allpass design over that of Mode 4 this configuration maintains a more constant amplitude with frequency at the complex zeros (C_z) output. The frequencies of the pole pair and zero pair are resistor tunable.

Design Equations

Outputs — Allpass
Bandpass
Lowpass

$$f_o = \sqrt{1 + \frac{R_2}{R_4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 + \frac{R_2}{R_4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1 - \frac{R_1}{R_4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 - \frac{R_1}{R_4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1 + R_2/R_4} \times \frac{R_3}{R_2}$$

$$Q_z = \sqrt{1 - R_1/R_4} \times \frac{R_3}{R_1}$$

$$H_{0_{cz1}} = \text{gain at Cz output (as } f \rightarrow 0 \text{ Hz)} = \frac{R_2 (R_4 - R_1)}{R_1 (R_2 + R_4)}$$

$$H_{0_{cz2}} = \text{gain at Cz output } \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{R_2}{R_1}$$

$$H_{OBP} = \left(\frac{R_2}{R_1} + 1\right) \times \frac{R_3}{R_2}$$

$$H_{OLP} = \left(\frac{R_2 + R_1}{R_2 + R_4}\right) \times \frac{R_4}{R_1}$$

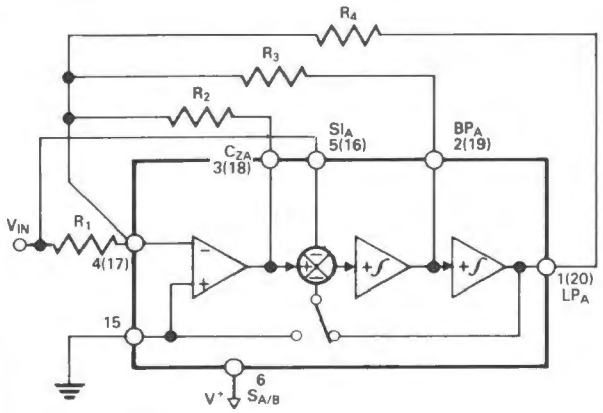


Figure 13 **Mode 5.**

Mode 6A

By using only one of the internal integrators a single pole filter is formed. This mode is useful for creating odd-ordered cascaded filter responses by providing a real pole that is clock tunable to track the resonant frequency of other 2nd order MF10 sections. The corner frequency is resistor tunable.

Design Equations

Outputs — High Pass, Lowpass } Single Pole

f_o = cutoff frequency of LP or HP output

$$= \frac{R_2}{R_3} \frac{f_{CLK}}{100} \text{ or } \frac{R_2}{R_3} \frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R_3}{R_1}$$

$$H_{OHP} = -\frac{R_2}{R_1}$$

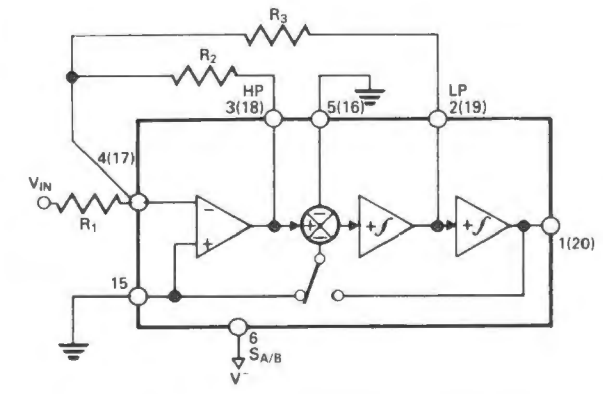


Figure 14 **Mode 6a.**

Mode 6B

This mode utilises only one of the integrators for a single pole lowpass and the input op-amp as an inverting amplifier to provide a non-inverting lowpass output.

Design Equations

f_c = cutoff frequency of LP outputs

$$= \frac{R_2}{R_3} \frac{f_{CLK}}{100} \text{ or } \frac{R_2}{R_3} \frac{f_{CLK}}{50}$$

$$H_{OLP_1} = 1 \text{ (non-inverting)}$$

$$H_{OLP_2} = -\frac{R_3}{R_2}$$

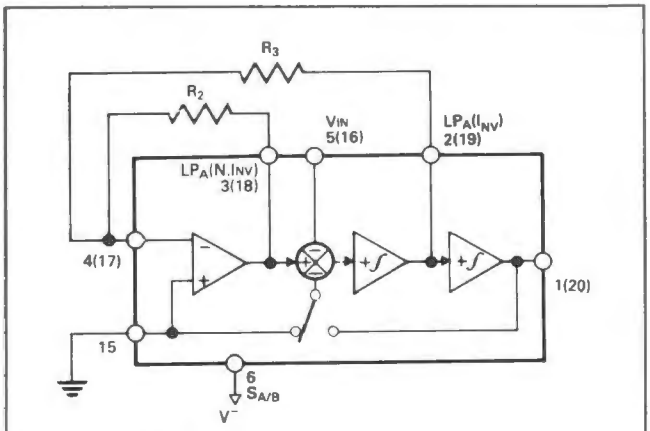


Figure 15 **Mode 6b.**

Applications

For single-supply operation, it is important for several terminals to be biased to half supply. A single-supply design for a 4th order 1kHz Butterworth lowpass (24dB/octave or 80dB/decade rolloff) is shown using Mode 1 in Figure 16. Note that the analogue ground terminal (pin 15), the summer inputs $S1_A$ and $S1_B$ (pins 5 and 16) and the clock switching control pin (pin 12) are all biased to $V_{CC}/2$. For symmetrical split supply operation these pins would be grounded. An input coupling capacitor is optional, as it is needed only if the input signal is not also biased to $V_{CC}/2$. For a two-stage Butterworth response, both stages have the same corner frequency, hence the common

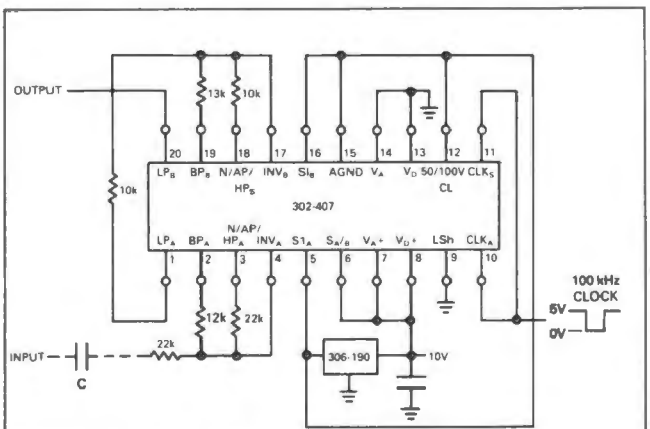


Figure 16 **4th order, 1kHz Butterworth lowpass filter.**
Only 6 resistors are required: this example also illustrates single supply biasing.

clock for both sides. The resistor values shown are the nearest 5% tolerance values used to set the overall gain of the filter to unity and to set the required Q of the first stage (side A) to 0.504 and the second stage (side B) Q to 1.306 for a flat passband response.

A unique advantage of the switched capacitor design of the MF10 is illustrated in Figure 17. Here the MF10 serves double duty in a data acquisition system as an input filter for simple bandlimiting and, as a sample and hold to allow larger amplitude, higher frequency input signals. By gating OFF the applied clock, the switched capacitor integrators will hold the last sampled voltage value. The droop rate of the output voltage during the hold time is approximately 0.1mV per ms.

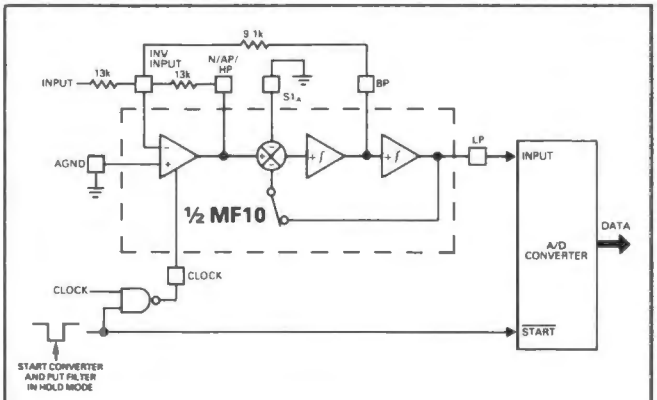


Figure 17 **An MF10 as an Input Filter and Sample/Hold**

A useful non-filtering application of the MF10 is shown in Figure 18. In this circuit, the MF10, together with an RS 311 comparator, are used as a resonator to generate stable amplitude sine and cosine outputs without using AGC circuitry. The MF10 operates as a Q of 10 bandpass filter which will ring at its resonant frequency in response to a step input change. The ringing signal is fed to the RS 311 which creates a square wave input signal to the bandpass to regenerate the oscillation. The bandpass output is the filtered fundamental frequency of a 50% duty cycle square wave. A 90° phase shifted signal of the same amplitude is available at the lowpass output through the second integrator in the MF10. The frequency of oscillation is set by the centre frequency of the filter as controlled by the clock and the 50:1/100:1 control pin. The output amplitude is set by the peak to peak swing of the square wave input, which in this circuit is defined by the back to back diode clamps at the RS 311 output.

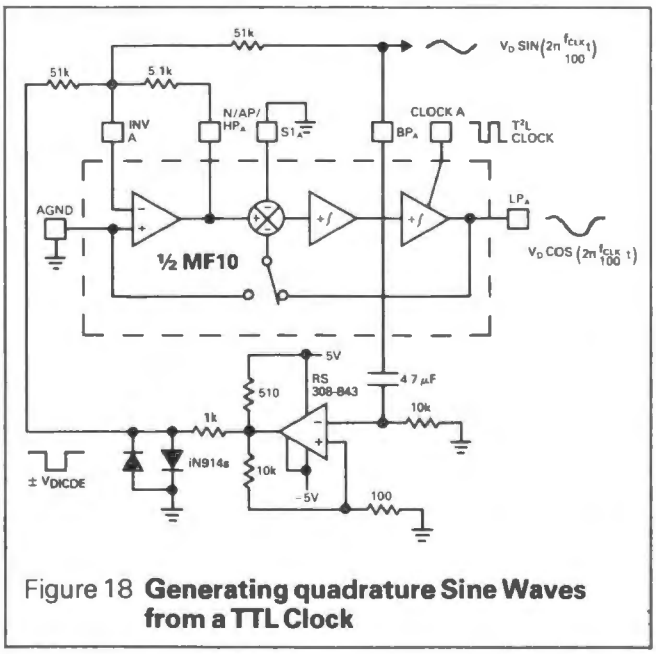


Figure 18 **Generating quadrature Sine Waves from a TTL Clock**

Finally, as a graphic illustration of the simplicity of filter implementation using the MF10, Figure 19 is a complete 300 baud, full-duplex modem filter. The filter is an 8th order, 1dB ripple Chebyshev bandpass which functions as both an 1170Hz originate filter and a 2125Hz answer filter. Control of answer or originate operation is set by the logic level at the 50/100/CL input so that only one clock frequency is required. The overall filter gain is 22dB.

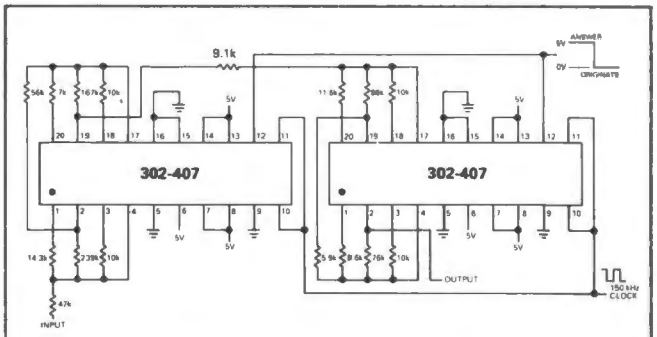


Figure 19 **A Complete Full-Duplex 300 Baud Modem Filter**

RS data

R.S. Components Ltd. 13-17 Epworth Street, London, EC2P 2HA Telephone: 01-253 1222 or 01-250 4000
An Electrocomponents Group Company

©RS Components Ltd. 1983

RS data

High Voltage Opto-isolator

Stock number 302-148

The RS OPL1264A opto-isolator consists of a GaAsP light emitting diode optically coupled to an NPN silicon phototransistor. The form of construction provides **10kV isolation** between input and output, with a minimum current transfer ratio of 25%. This device has **BASEEFA approval,** thus extending its area of application wider than that covered by most conventional types.

Features

- High isolation : 10kV input to output
- Simple to use and interface
- Good current transfer ratio: 25% minimum
- BASEEFA approved

Absolute maximum ratings (at 25°C unless stated)

Storage temperature — −40 to +85°C
Operating temperature — −40 to +85°C
Soldering temperature — 240°C (5 secs)

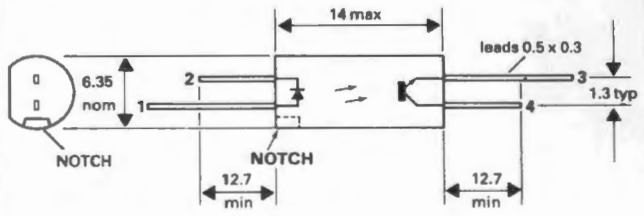
Input Diode

Power dissipation — 50mW*
Forward d.c. current — 40mA**
Reverse d.c. voltage — 3V

Output Transistor

Power dissipation — 100mW*
Collector – Emitter voltage — 32V
Emitter – Collector voltage — 5V

* Derate linearly at 1.82mW/°C above 25°C
** Derate linearly at 0.73mA/°C above 25°C



All dimensions in mm

Package details

Electro-optical characteristics (at 25°C)

	Parameter	Conditions	Min	Typ	Max	Units
Input Diode	Forward voltage	I_F = 20mA			1.5	V
	Reverse current	V_R = 3V			100	μA
Output Transistor	Collector – emitter breakdown voltage	I_C = 1mA	32			V
	Emitter – collector breakdown voltage	I_E = 100μA	5			V
	Collector – emitter dark current	V_{CE} = 20V			200	nA
	Collector – emitter dark current	V_{CE} = 10V, T_A = 70°C			100	μA
Coupled characteristics	d.c. current transfer ratio	I_F = 10mA, V_{CE} = 5V	25			%
	Isolation voltage	Input leads shorted and output leads shorted	10			kV
	Collector – emitter saturation voltage	I_F = 10mA, I_C = 1.6mA			0.4	V
	Input – output capacitance	Input leads shorted and output leads shorted		0.06		pF
	Turn-on time	I_C = 2mA, V_{CC} = 10V, R_L = 100Ω		4		μs
	Turn-off time	I_C = 2mA, V_{CC} = 10V, R_L = 100Ω		3		μs

RS data

Notes on BASEEFA Approval

The BASEEFA (British Approvals Service for Electrical Equipment in Flammable Atmospheres) Approval number is:

BAS Ex 812252U Code EEx ia IIc

This confirms that the component has successfully met the examination and test requirements and has been found to comply with harmonised standards:

BS 5501 : Part 1 : 1977 EN 50 014
BS 5501 : Part 7 : 1977 EN 50 020

In particular compliance has been met in respect of clearances, creepage distances and distances through the casting compound for a maximum peak voltage of 375V.

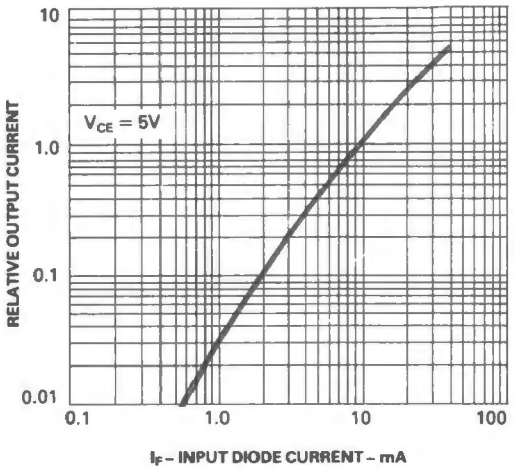


Figure 2 **Relative output current vs input current**

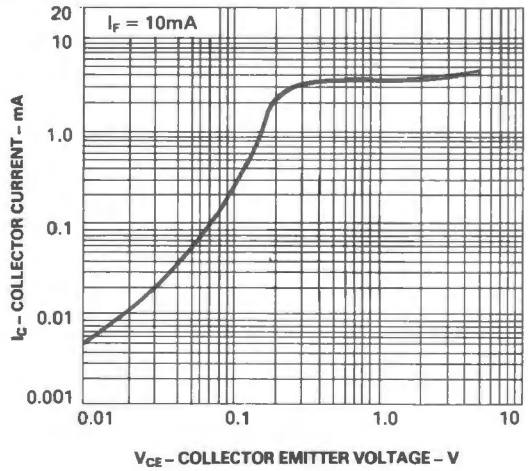


Figure 1 **Collector current vs collector emitter voltage**

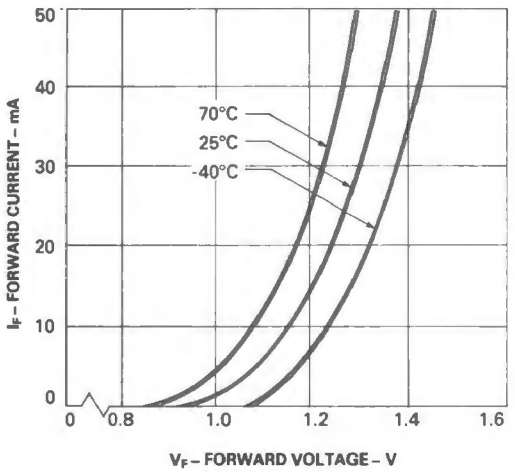


Figure 3 **Forward current vs forward voltage**

©RS Components Ltd. 1984

RS data

Dual 6N138 Opto-isolator

Stock number 302-126

The RS Dual 6N138 opto-isolator is equivalent to the HCPL-2730.

This isolator contains a pair of GaAsP light emitting diodes optically coupled to a pair of integrated high gain photon detectors. Each channel has an extremely high current transfer ratio, 3000V dc isolation and excellent input-output common mode transient immunity. In addition the photodiodes and first-stage transistors have a separate connection pin (V_{CC}). This permits lower output saturation voltage and higher speed operation than is possible with conventional photodarlington type isolators. The V_{CC} pin may be strobed low as an 'output disable'. V_{CC} can be as low as 1.6V without adversely affecting performance.

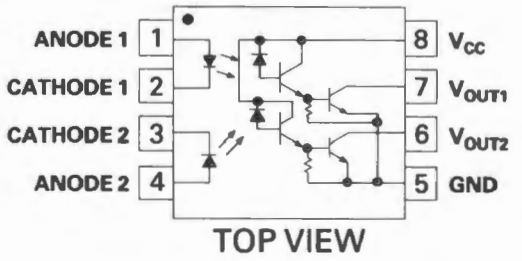
Features

- High current transfer ratio: 1000% typical
- Low input current requirement: 1.6mA typical
- Low output saturation voltage: 1V typical
- 3000V dc withstand test voltage
- Performance guaranteed over 0 to 70°C temperature range
- High common mode rejection
- Data rates up to 300kbit/s

Absolute maximum ratings

Storage temperature ——— −55°C to +125°C
Operating temperature ——— −40°C to +85°C
Lead solder temperature ——— 260°C for 10 sec (1.6mm below seating plane)
Average input current — I_F (each channel) ——— 20mA[1]
Peak input current — I_F (each channel) ——— 40mA (50% duty cycle, 1ms pulse width)
Reverse input voltage — V_R (each channel) ——— 5V
Input power dissipation (each channel) ——— 35mW[2]
Output current — I_O (each channel) ——— 60mA[3]
Supply and output voltage – V_{CC} (Pin 8-5). V_O (Pin 7, 6-5)[4]
HCPL-2730 ——— −0.5 to 7V
HCPL-2731 ——— −0.5 to 18V
Output power dissipation (each channel) ——— 100mW[5]

Figure 1 **Schematic**



(8 pin Dual-in-Line package)

CAUTION: ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

NOTES

1. Derate linearly above 50°C free-air temperature at a rate of 0.5mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.9mW/°C.
3. Derate linearly above 35°C free-air temperature at a rate of 0.6mA/°C.
4. Pin 5 should be the most negative voltage at the detector side.
5. Derate linearly above 35°C free-air temperature at a rate of 1.7mW/°C. Output power is collector output power plus supply power.

Electrical characteristics

(Over recommended temperature T_A = 0°C to 70°C, unless otherwise specified)

Parameter	Symbol	Min	Typ*	Max	Units	Test conditions	Fig	Notes
Current transfer ratio	CTR	300	1000		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	3	6, 7
Logic low Output voltage	V_{OL}		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		6
Logic high Output current	I_{OH}		0.01	250	μA	I_F = 0mA, V_O = V_{CC} = 7V		6
Logic low Supply current	I_{CCL}		0.9		mA	I_{F1} = I_{F2} = 1.6mA V_{O1} = V_{O2} = Open V_{CC} = 7V		
Logic high Supply current	I_{CCH}		4		nA	I_{F1} = I_{F2} = 0mA V_{O1} = V_{O2} = Open V_{CC} = 7V		
Input forward voltage	V_F		1.4	1.7	V	I_F = 1.6mA, T_A = 25°C	5	6
Input reverse breakdown voltage	BV_R	5			V	I_R = 10μA, T_A = 25°C		
Temperature coefficient of forward voltage	$\frac{\Delta V_F}{\Delta T_A}$		−1.8		mV/°C	I_F = 1.6mA		6
Input capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0		6
Input-output insulation leakage current	I_{I-O}			1.0	μA	45% relative humidity, T_A = 25°C t = 5s, V_{I-O} = 3000 Vdc		8
Resistance (input-output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		8
Capacitance (input-output)	C_{I-O}		0.6		pF	f = 1 MHz		8
Input-input insulation leakage current	I_{I-I}		0.005		μA	45% relative humidity, t = 5s V_H = 500 Vdc		9
Resistance (input-input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 Vdc		9
Capacitance (input-input)	C_{I-I}		0.25		pF	f = 1 MHz		9

*All typicals at T_A = 25°C (See below for notes)

Switching Characteristics (at T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Units	Test conditions	Fig	Notes
Propagation Delay Time To Logic Low at Output	t_{PHL}		5 0.5	20 2	μs	I_F = 1.6mA, R_L = 2.2kΩ I_F = 12mA, R_L = 270Ω	10	
Propagation Delay Time To Logic High at Output	t_{PLH}		10 1	35 10	μs	I_F = 1.6mA, R_L = 2.2kΩ I_F = 12mA, R_L = 270Ω	10	
Common Mode Transient Immunity at Logic High Level Output	CM_H		500		V/μs	I_F = 0mA, R_L = 2.2kΩ $\|V_{CM}\|$ = 10V_{p-p}	11	10,11
Common Mode Transient Immunity at Logic Low Level Output	CM_L		−500		V/μs	I_F = 1.6mA, R_L = 2.2kΩ $\|V_{CM}\|$ = 10V_{p-p}	11	10,11

NOTES

6. Each channel.
7. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
8. Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.
9. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
10. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in Logic High state (i.e. V_O >2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e. V_O <0.8V).
11. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is

$$R_{CC} = \frac{1V}{0.3\,I_F\,(mA)}\,k\Omega$$

Major Characteristics

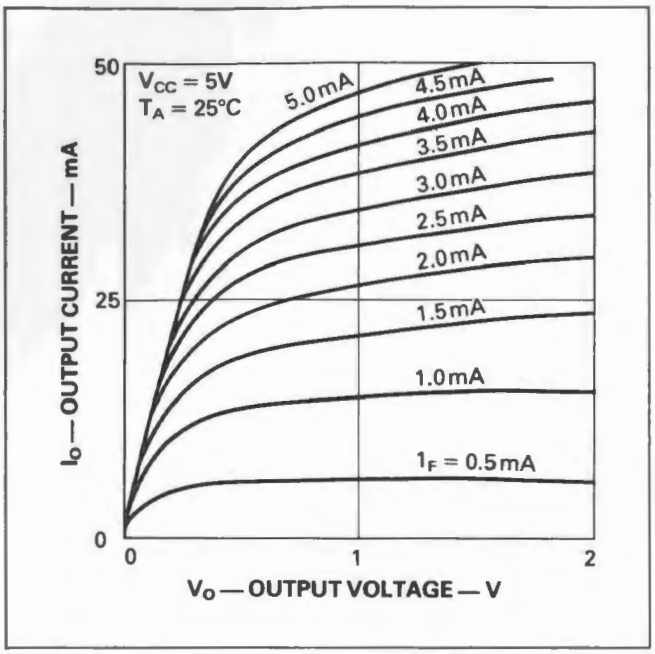


Figure 2 **DC Transfer Characteristics**

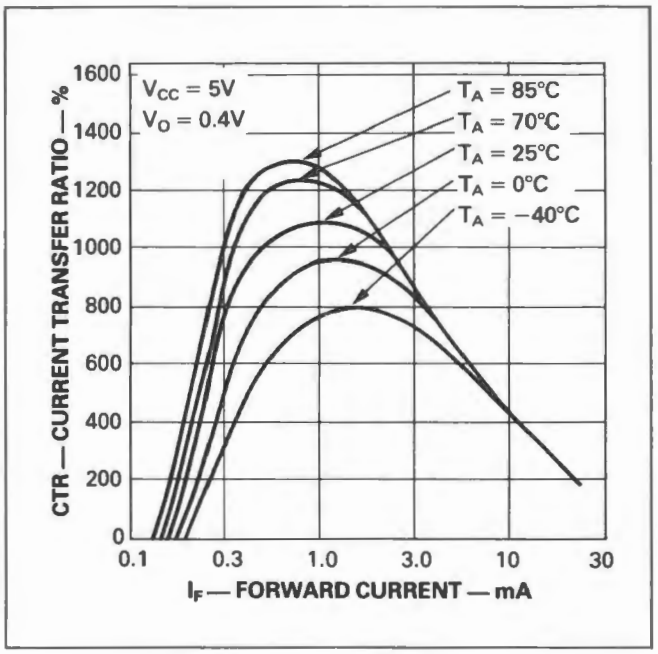


Figure 3 **Current Transfer Ratio vs. Forward Current**

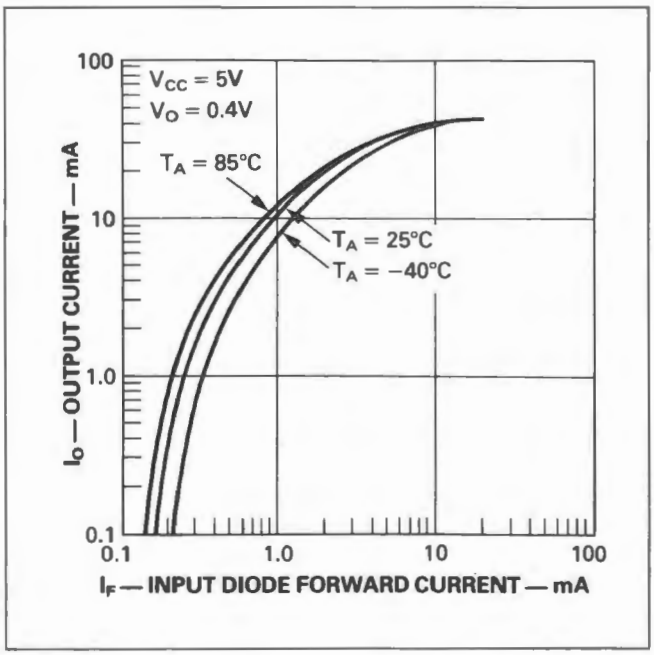


Figure 4 **Output Current vs. Input Diode Forward Current**

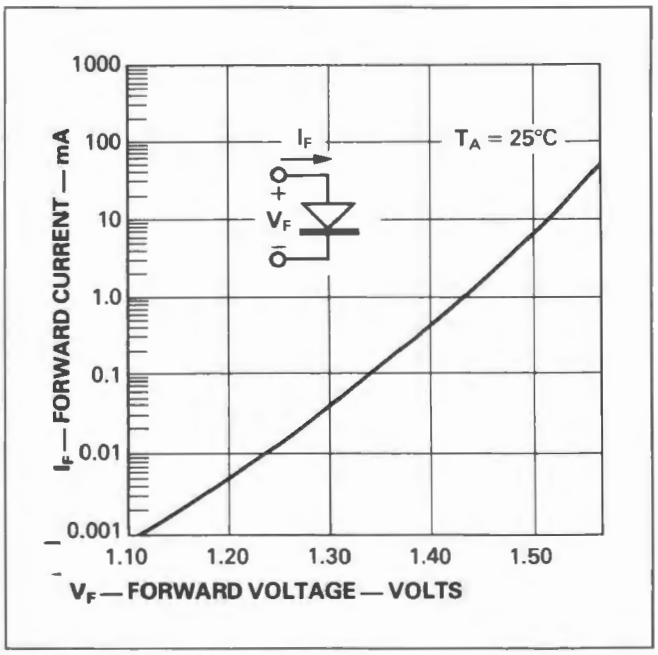


Figure 5 **Input Diode Forward Current vs. Forward Voltage**

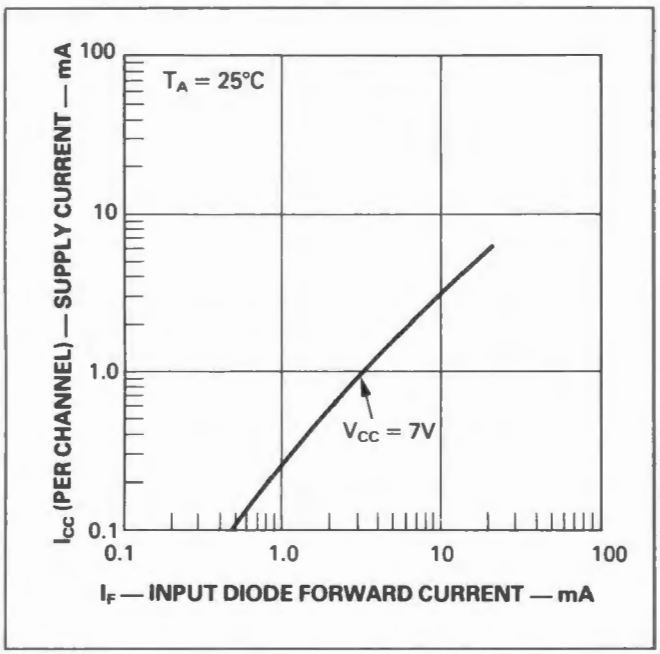


Figure 6 **Supply Current Per Channel vs. Input Diode Forward Current**

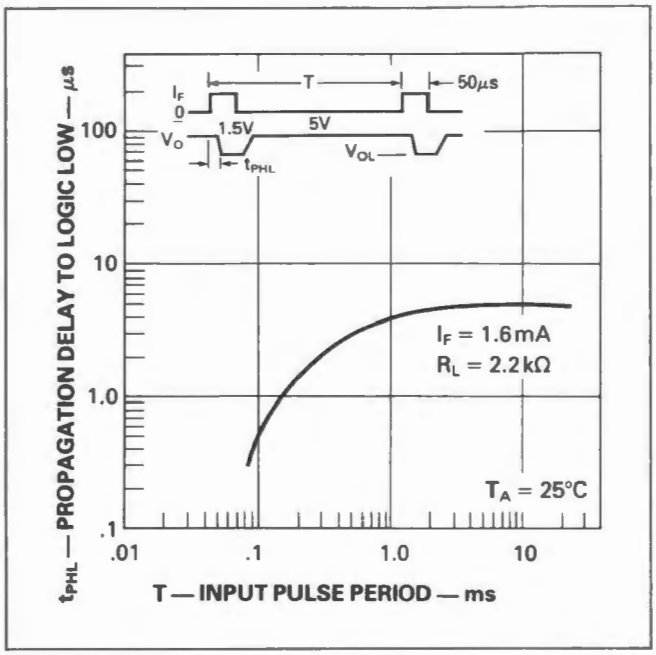


Figure 7 **Propagation Delay To Logic Low vs. Pulse Period**

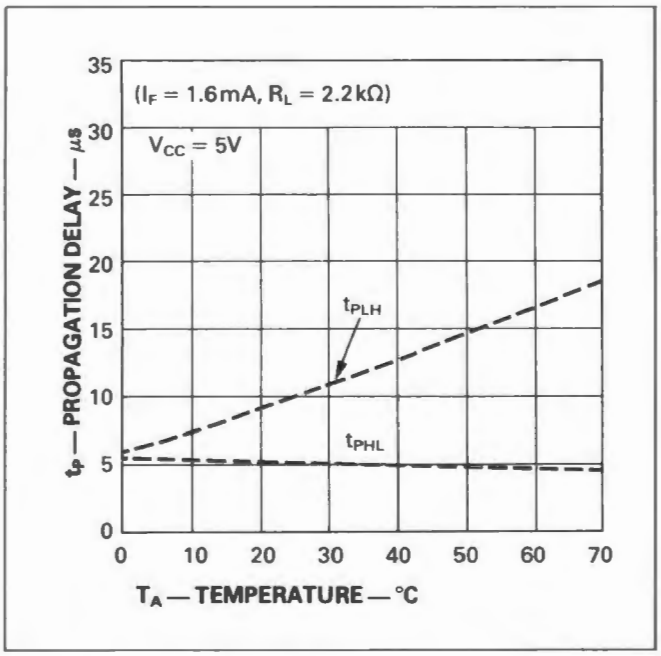


Figure 8 **Propagation Delay vs. Temperature**

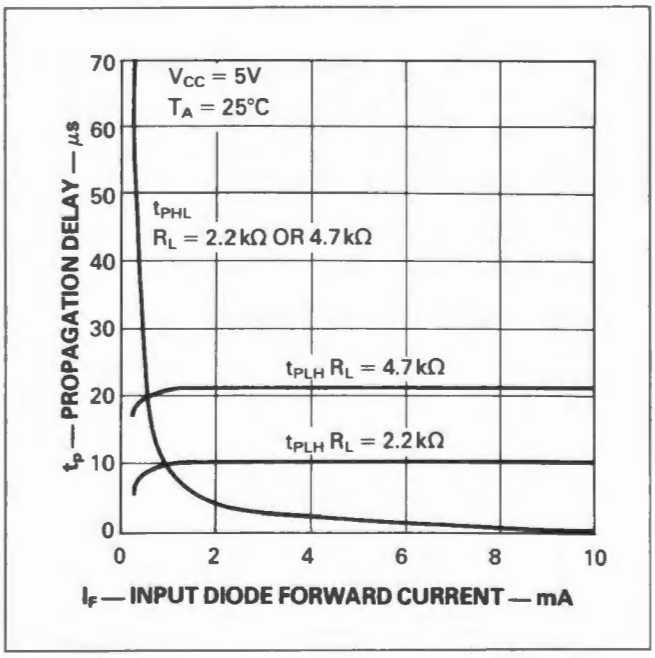


Figure 9 **Propagation Delay vs. Input Diode Forward Current**

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RS data

Frequency Meter Module

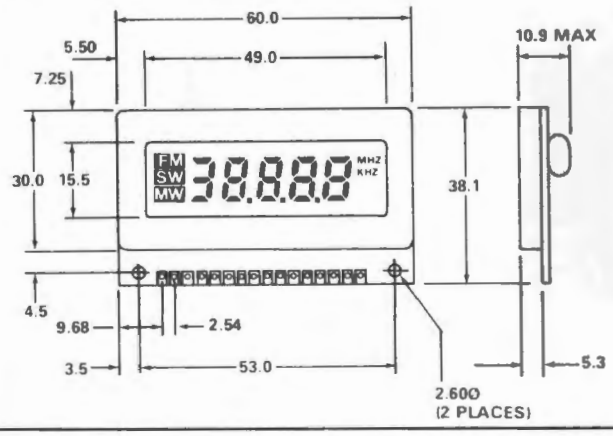
Stock number 258-063

A self-contained module which reads and displays frequencies up to 3999.9 kHz directly. The small size and low current consumption of this unit, with its liquid crystal display, makes the device ideal for incorporation into a wide variety of equipments, especially battery operated ones. The offset facility enables standard radio intermediate frequencies to be added to or subtracted from the display, making the module of direct interest to communications designers.

Features

- Easily fitted to panels
- 4¾ digit display
- 9 mm high clear digits
- May be pre-scaled for higher frequencies
- 26 I.F. offsets available
- 4.75 V to 7 V operating voltage
- Selectable display annunciators

Figure 1 **Dimensions (in mm)**



Absolute maximum ratings

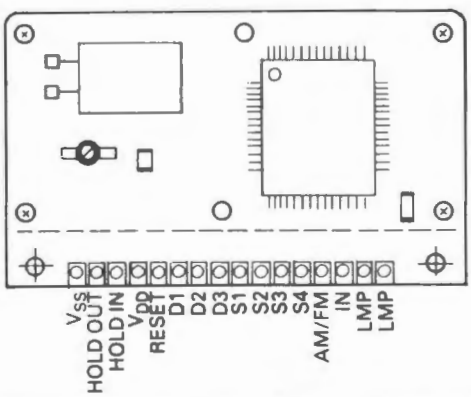
Power supply voltage (V_{DD}) ——— = 0.3 to + 7 V (@ 25°C)

Input voltage (V_I) ——— = 0.3 to V_{DD} (@ 25°C)

Storage temperature (T_{stg}) ——— = −10 to + 60°C

Operating temperature (T_{op}) ——— 0 to + 50°C

Figure 2 **Connections**



Electrical characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power supply voltage	V_{DD}		4.75	5	7	V
Current consumption	I_{DD}	No load			4	mA
Input voltage – high	V_{IH}		3.6			V
Input voltage – low	V_{IL}				0.8	V
Hold output voltage – high	V_{OH}	$I_O = -40\mu A$	4.2			V
Hold output voltage – low	V_{OL}	$I_O = 1.6$ mA			0.4	V
Hold output current – high	I_{OH}	$V_O = 2.5$ V	−0.2			mA
Hold output current – low	I_{OL}	$V_O = 0.4$ V	1.6			mA
Maximum input frequency*	f_{IN}	$V_I = 1$ Vp-p (Capacitor coupled)	5	7		MHz

*For frequencies greater than 3.9999 MHz the display reads $f_{in} - 4$ MHz

Table 1 **Display format**

Display range	Example of digital display	Select inputs AM/FM	S1	S2	S3	S4	IF offset value	Units
0.0-3999.9	MW 1222.5 KHZ	H	L	L	L	L	−455	kHz
		H	L	H	L	L	−260	
		H	L	L	H	L	−450	
		H	L	H	H	L	−261	
		H	L	L	L	H	−468	
		H	L	H	L	H	−470	
0.00-399.99 (See note 1)	SW 12.555 MHZ	H	H	L	L	L	−0.455	MHz
		H	H	H	L	L	−0.468	
		H	H	L	H	L	−2.0	
		H	H	H	H	L	−10.7	
00.000-39.999 (See note 1)	FM 92.88 MHZ	L	L	L	L	L	+10.7	MHz
		L	H	L	L	L	+10.63	
		L	L	H	L	L	−10.7	
		L	H	H	L	L	+10.66	
		L	L	L	H	L	+10.74	
		L	H	L	H	L	+10.77	
		L	L	H	H	L	−10.63	
		L	H	H	H	L	−10.65	
		L	L	L	L	H	−10.66	
		L	H	L	L	H	−10.67	
		L	L	H	L	H	−10.68	
		L	H	H	L	H	−10.71	
		L	L	L	H	H	−10.74	
		L	H	L	H	H	−10.75	
		L	L	H	H	H	−10.77	
		L	H	H	H	H	−10.78	
Frequency meter 0.0-3999.9 (See note 1)	MW 1222.2 KHZ	H	L	L	H	H	Nil	kHz

Note 1 Due to the maximum input frequency considerations of the frequency meter module, input frequencies from 4MHz to 40MHz require a ÷ 10 prescaler to be used before the module input, and frequencies from 40MHz to 400MHz require a ÷ 100 prescaler to be used.

H = 'High level' (V_{DD}) L = 'Low level' (V_{SS})

Designation and definition of inputs and outputs

V_{DD} Positive voltage to module (H).

V_{SS} Negative voltage to module (L).

IN Input (See note 2).

AM/FM, S1, S2, S3, S4 (Internal resistor pulldown to V_{SS})
Inputs for selecting the operating mode and IF offset, see Table 1.

D1, D2, D3 (Internal resistor pulldown to V_{SS})
Inputs for selecting the display format, see Table 2.

HOLD IN (Internal resistor pulldown to V_{SS})
When at V_{SS} or open, the display follows the INput. When connected to V_{DD}, the display is fixed within 300ms and ignores the INput.

HOLD OUT This output is used to reduce power consumption of a prescaler. HOLD OUT goes from V_{DD} to V_{SS} within 300ms after HOLD IN has gone from V_{SS} to V_{DD}.

RESET (Internal resistor pulldown to V_{SS})
When in AM, FM or SW mode, connection to V_{DD} displays the contents of the IF offset ROM (read only memory).
When in the frequency counter or event counter mode, connection to V_{DD} resets the counter.

LMP Two inputs are provided to power the 5 volt back light lamp (20mA typ).

Note 2 The high input impedance of the frequency meter module necessitates correct termination of the input in order to reduce the possibility of spurious triggering of the frequency meter.

Table 2 **Display format selection**

Select terminals			Display contents
D1	D2	D3	
L	L	L	Normal display
H	L	L	1) 0 displayed in the last two digits in MW/SW mode 2) 2nd last digit displays 1, 3, 5, 7 and 9 with the last digit displaying 0 in FM mode
L	H	L	The last digit displays 0

Applications

Connected to local oscillator circuit

When used in radio receiver applications it is often very convenient to display the frequency tuned to by connecting the module to the local oscillator and offsetting the display by an amount equal to the intermediate frequency. An example is shown in figure 3 in block diagram form.

Figure 3 **Module connected to L.O.**

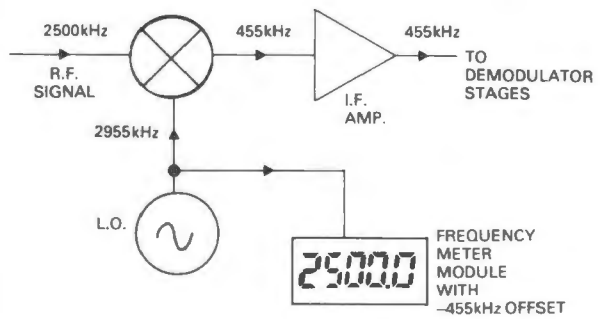
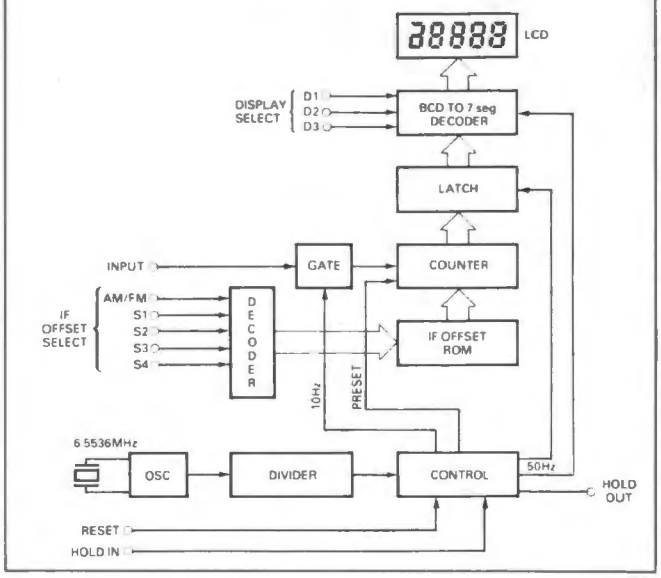
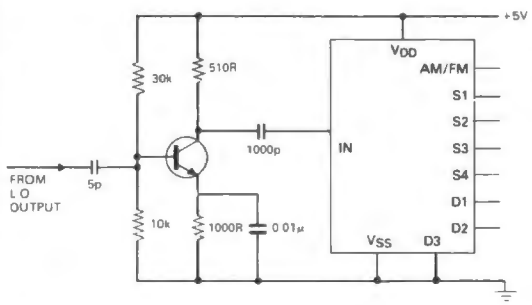


Figure 4 **Block diagram**



A typical interfacing circuit that may be used is shown in figure 5.

Figure 5 **Module interfaced to L.O.**

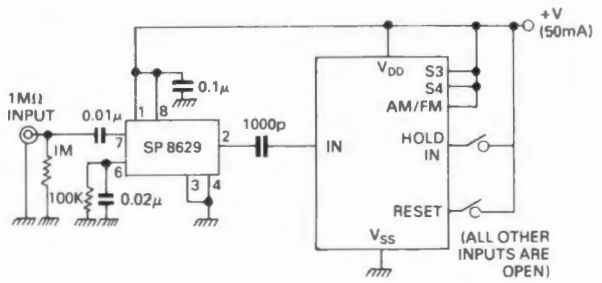


See Tables 1 and 2 for conditions of inputs AM/FM, S1-4 and D1-3.

RS data

High frequency applications
For high frequency applications the frequency meter module may be used in conjunction with the RS 150MHz ÷ 100 prescaler i.c. SP8629 (stock no. 307-474). Details of this i.c. are given on Data Sheet 3059. A typical circuit is shown in figure 6.

Figure 6 **150MHz frequency meter**



Careful layout as per standard VHF practice is essential for good results. The p.c.b. for the SP8629 should be of double-side design, where the top (component) side is used as a ground plane. All tracks should be as wide as possible, especially the prescaler 5V line. Both resistors should be 0.5W thick film types. The 0.1μF capacitor and 0.01μF capacitors should be disc ceramic types. (Note that the capacitor connected to pin 7 of the SP8629 and the 1MΩ resistor limit the working voltage that the 1MΩ input can be connected to.) When HOLD IN is closed the display is frozen. The RESET switch resets the display to zero. At frequencies below 10MHz the prescaler may give problems due to insufficent slew rate – see Data Sheet 3059 for further details.

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RS data

Tachometer i.c. 2917

Stock number 302—047

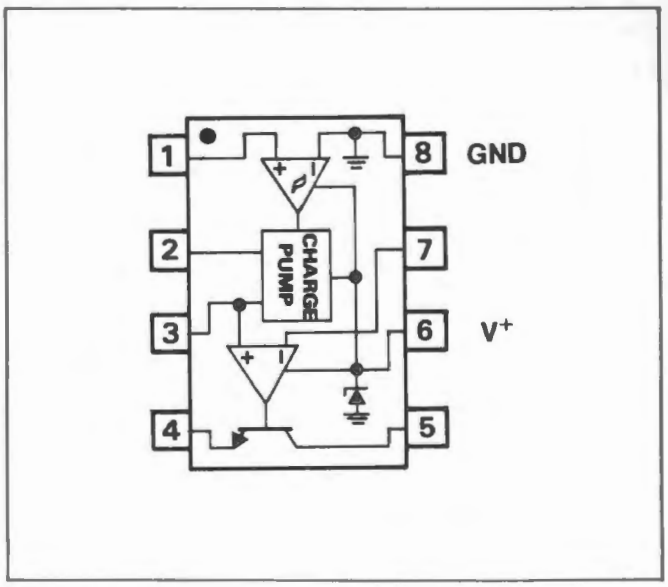
The RS·Tachometer i.c. is a monolithic frequency to voltage converter; featuring a ground referenced, protected input stage with built in hysteresis making it ideally suited for use with magnetic pick ups (stock number 304-166) or it may simply be adapted for use with many other sensors with pulse rate outputs.
This tachometer i.c. uses a charge pump technique and offers frequency doubling for low ripple. Its output swings to ground for a zero frequency input and the integral regulator clamps the supply to provide stable frequency to voltage or current operation.
Additionally this device contains an op-amp/comparitor together with a floating transistor that may be configured to provide either a proportional output or a speed switched output that will directly drive meters, relays, solenoids, lamps etc.

Features

- Built-in hysteresis with ground referenced fully protected input
- Interfaces directly with RS magnetic pick-up
- Built in zener
- Floating transistor output will source or sink 50mA to operate relays, solenoids, meters etc
- Frequency doubling for low ripple
- 0.3% typical linearity

Absolute maximum ratings (Note 1)

Supply voltage	28V
Supply current	25mA
Collector voltage	28V
Differential input voltage	
Tachometer	28V
Op-amp/Comparator	28V
Input voltage range	
Tachometer	±28V
Op-amp/Comparator	0.0V to +28V
Power dissipation	500mW
Operating temperature range	–40°C to +85°C
Storage temperature range	–65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C



Electrical characteristics $V_{CC} = 12V_{DC}$, $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
TACHOMETER					
Input thresholds	V_{IN} = 250mVp-p @ 1kHZ (Note 2)	±10	±15	±40	mV
Hysteresis	V_{IN} = 250mVp-p @ 1kHz (Note 2)		30		mV
Offset voltage	V_{IN} = 250mVp-p @ 1kHz (Note 2)		3.5	10	mV
Input bias current	$V_{IN} = \pm 50mV_{DC}$		0.1	1	µA
V_{OH} } Pin 2	$V_{IN} = +125mV_{DC}$ (Note 3)		8.3		V
V_{OL} } Pin 2	$V_{IN} = -125mV_{DC}$ (Note 3)		2.3		V
Output current: I_2, I_3	V2 = V3 = 6.0V (Note 4)	140	180	240	µA
Leakage current: I_3	I_2 = 0, V3 = 0			0.1	µA
Gain constant, K	(note 3)	0.9	1.0	1.1	
Linearity	f_{IN} = 1kHz, 5kHz, 10kHz, (Note 5)	–1.0	0.3	+1.0	%

Parameter	Conditions	Min	Typ	Max	Units
OP/AMP COMPARATOR					
V_{OS}	V_{IN} = 6.0V		3	10	mV
I_{BIAS}	V_{IN} = 6.0V		50	500	nA
Input common-mode voltage		0		V_{CC} –1.5V	V
Voltage gain			200		V/mV
Output sink current	V_C = 1.0	40	50		mA
Output source current	$V_E = V_{CC}$ –2.0		10		mA
Saturation voltage	I_{SINK} = 5mA		0.1	0.5	V
	I_{SINK} = 20mA			1.0	V
	I_{SINK} = 50mA		1.0	1.5	V
ZENER REGULATOR					
Zener voltage (Pin 6)	R_{DROP} = 470Ω		7.56		V
Series resistance			10.5	15	Ω
Temperature stability			+1		mV/°C
TOTAL SUPPLY CURRENT			3.8	6	mA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 187° C/W junction to ambient.

Note 2: Hysteresis is the sum $+V_{TH} - (-V_{TH})$, offset voltage is their difference.

Note 3: V_{OH} is equal to 3/4 x V_{CC} –1 V_{BE}, V_{OL} is equal to 1/4 x V_{CC} – 1 V_{BE} therefore $V_{OH} - V_{OL} = V_{CC}/2$. The difference, $V_{OH} - V_{OL}$, and the mirror gain, I_2/I_3, are the two factors that cause the tachometer gain constant to vary from 1.0.

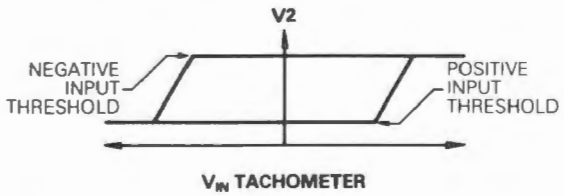
Note 4: Be sure when choosing the time constant R1 x C1 that R1 is such that the maximum anticipated output voltage at pin 3 can be reached with I_3 x R1. The maximum value for R1 is limited by the output resistance of pin 3 which is greater than 10MΩ typically.

Note 5: Nonlinearity is defined as the deviation of V_{OUT} (@ pin 3) for f_{IN} = 5kHz from a straight line defined by the V_{OUT} @ 1 kHz and V_{OUT} @ 10kHz. C1 = 1000pF, R1 = 68k and C2 = 0.22μFd.

Design considerations

The first stage is a differential amplifier driving a positive feedback flip flop circuit. The input threshold voltage is the amount of differential input voltage at which the output of this stage changes state. One input is internally grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This makes the device ideally suited for use with magnetic variable reluctance pickups which typically provide a single-ended output. This single ended input is also fully protected against voltage swings to +28V, which may be attained with these types of pickups.

Tachometer Input Threshold Measurement



Following the input stage is the charge pump where the input frequency is converted to a d.c. voltage. To do this requires one timing capacitor, one output resistor and one integrating or filter capacitor. When the input stage changes state, due to a zero crossing, the capacitor is either charged or discharged linearily between two voltages whose difference is half the regulator voltage (Vz). So in one half cycle of the input frequency the change in charge on the timing capacitor is equal to Vz/2 x C1. The average amount of current pumped into or out of the capacitor then is:

$$i_{C(AVG)} = \frac{\triangle Q}{T} = C1 \times \frac{V_z}{2} \times (2 f_{IN})$$
$$= V_z \times f_{IN} \times C_1$$

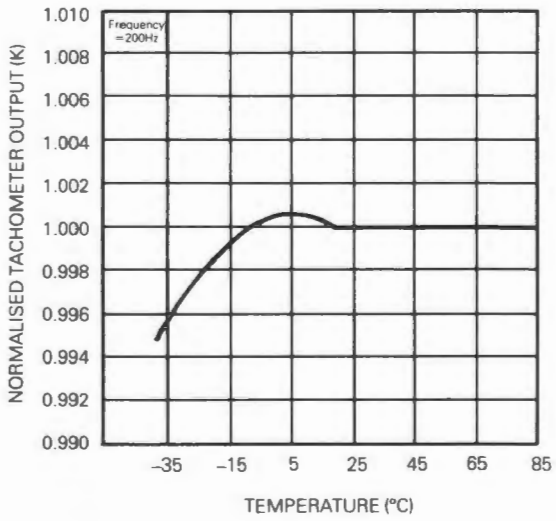
The output circuit mirrors this current very accurately into the load resistor R1, connected to ground, such that if the pulses of current are integrated with a filter capacitor then:

$$V_0 = i_c \times R1$$
$$= V_z \times f_{IN} \times C1 \times R1 \times K$$

(Where K is the gain constant – typically 1.0).

The size of C2 is dependent only on the amount of ripple voltage allowable and the required response time.

Normalised Tachometer Output vs Temperature



Choosing R1 and C1

There are some limitations on the choice of R1 and C1 which should be considered for optimum performance. The timing capacitor also provides internal compensation for the charge pump and

should be kept larger than 100 pF for very accurate operation. Smaller values can cause an error current on R1, especially at low temperatures. Several considerations must be met when choosing R1. The output current at pin 3 is internally fixed and therefore $V_O/R1$ must be less than or equal to this value. If R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Also output ripple voltage must be considered and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1, C2 combination is:

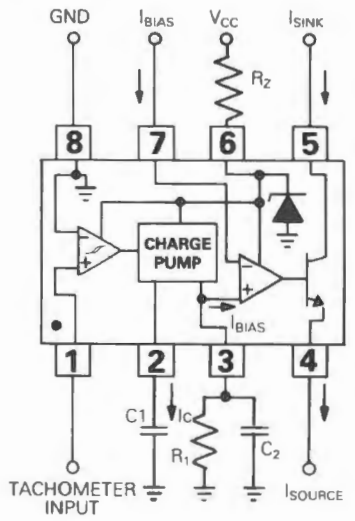
$$V_{RIPPLE} = \frac{V_Z}{2} \times \frac{C1}{C2} \times \left(1 - \frac{V_Z \times f_{IN} \times C1}{I_2}\right) \text{pk–pk}$$

It appears R1 can be chosen independent of ripple, however response time, or the time it takes V_{OUT} to stabilize at a new voltage increases as the size of C2 increases so a compromise between ripple, response time, and linearity must be chosen carefully.

As a final consideration, the maximum attainable input frequency is determined by V_Z, C1 and I_2:

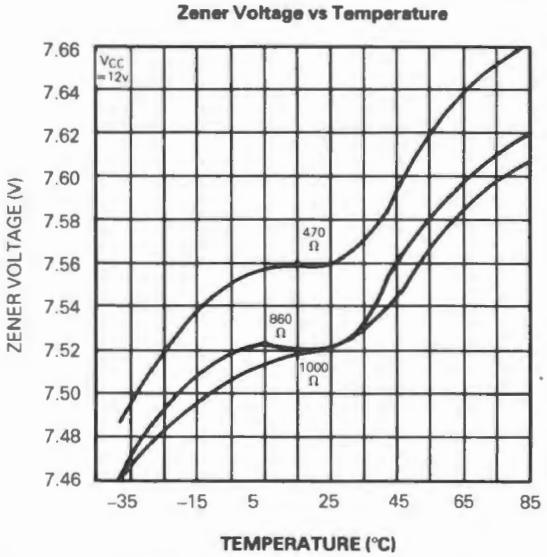
$$f_{MAX} = \frac{I_2}{C1 \times V_Z}$$

Figure 1



Choosing R_z

The most important consideration in choosing a dropping resistor from the unregulated supply to the device is that the tachometer and op-amp circuitry alone require about 3mA at the voltage level provided by the zener. At low supply voltages there must be some current flowing in the resistor above the 3mA circuit current to operate the regulator. As an example, if the raw supply varies from 9 to 16V, a resistance of 470Ω will minimise the zener voltage variation to 160mV. If the resistance goes under 400Ω or over 600Ω the zener variation quickly rises above 200mV for the same input variation.



Typical applications

Figure 2 **Minimum component tachometer**

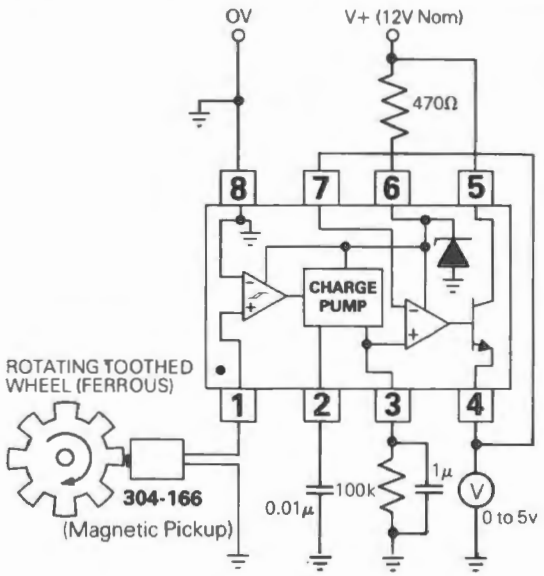
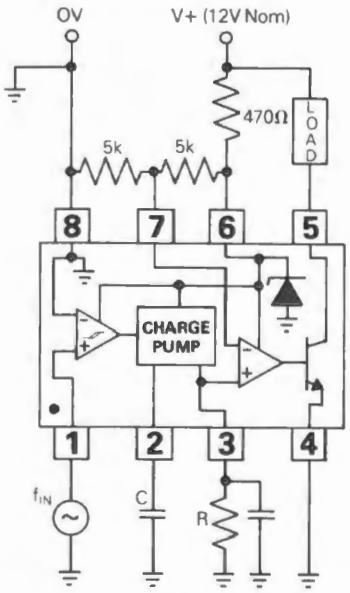


Figure 3 **Speed switch**

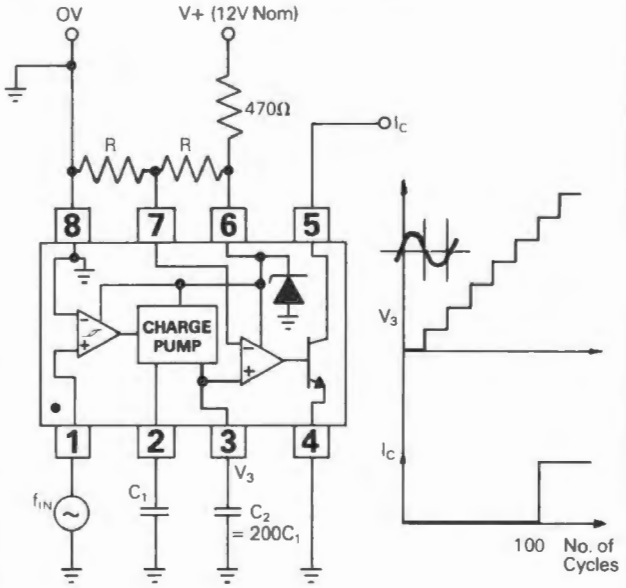


Load is energised when:

$$f_{IN} \geq \frac{1}{2RC}$$

RS data

Figure 4 **100 Cycle delay switch**



V_3 steps up in voltage by the amount

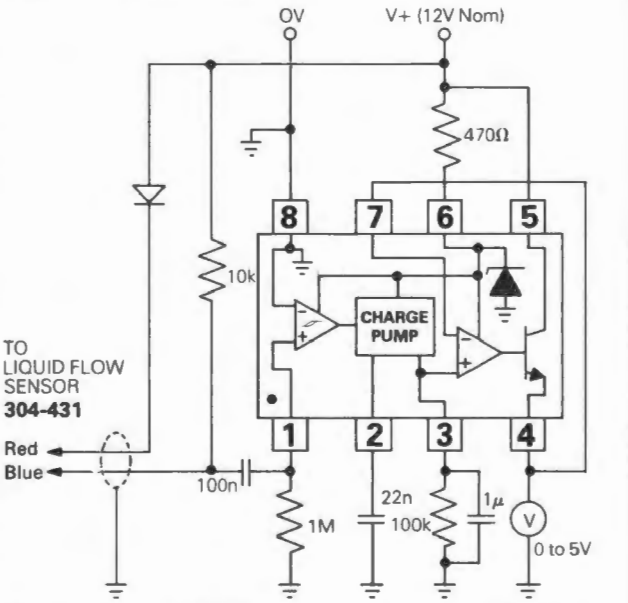
$\frac{V_{CC} \times C1}{C2}$ for each complete cycle

(2 zero crossings).

e.g. If C2 = 200 C1 after 100 consecutive input cycles.

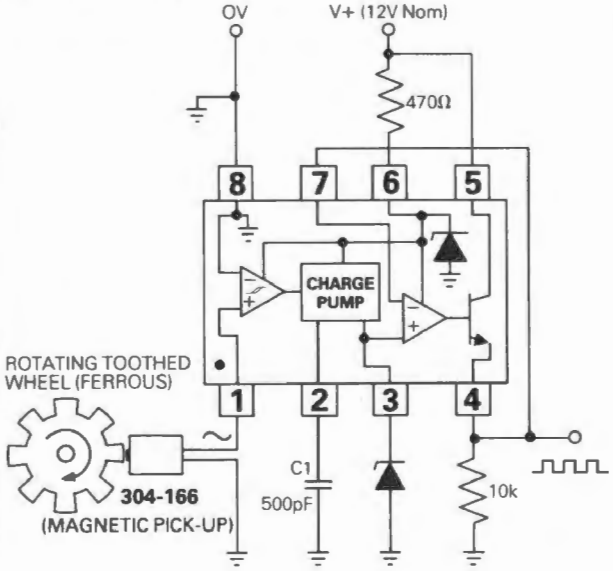
$V3 = 1/2\ V_z$ (V_Z = zener volts)

Figure 5 **Flow meter**



Note: Flow sensor output is decoupled to provide a signal that is symmetrical about OV.

Figure 6 **Frequency doubler**

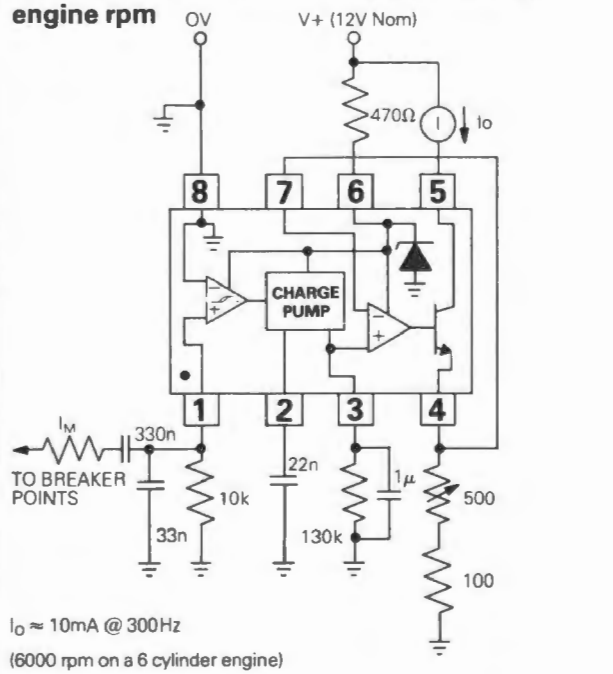


Precision two-shot output frequency equals twice input frequency.

$$\text{Pulse width} = \frac{V_z}{2} \times \frac{C_1}{I_2}$$

Pulse height = V_{ZENER} (external zener) pin 3

Figure 7 **Current driven meter indicating engine rpm**



$I_O \approx 10mA$ @ 300Hz

(6000 rpm on a 6 cylinder engine)

©RS Components Ltd. 1984

RS data

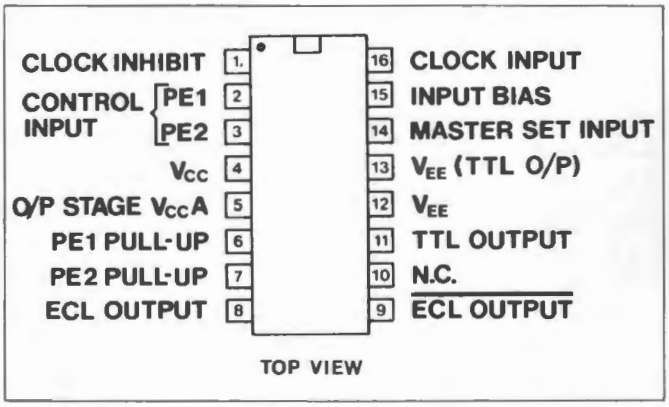
575 MHz ÷ 10/11 Prescaler i.c.

Stock number 302—378

The 8680 is an ECL (emitter coupled logic) prescaling counter with both ECL 10K and TTL compatible outputs. The circuit will operate from either ECL or TTL power supplies as required. The division ratio is set by two inputs PE1 and PE2. Division by 10 is undertaken when either control input is in the high state or by 11 when both control inputs are low. The counter can also be set to the eleventh state by applying a high level to the master set input.

Features

- High speed operation DC to 575 MHz
- Divide by 10 or 11 selectable
- ECL and TTL compatible outputs
- Asynchronous master set



Absolute maximum ratings

Supply voltage	8V
ECL output source current	50mA
TTL output sink current	30mA
Maximum clock input voltage	2.5V peak to peak
Maximum junction temperature	+150°C
Operating temperature range	0° to +70°C
Storage temperature range	− 55°C to +150°C

Electrical characteristics

Supply voltage 4.75 to 5.5V T_A = 25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Maximum input frequency	f max	AC coupled 350mV p-p		650	575	MH_z
Minimum input frequency	f min	AC coupled 600mV p-p	10			MH_z
PE1 and PE2 inputs, high voltage	V_{INH}	Vcc = 5V	3.9			V
PE1 and PE2 inputs, low voltage	V_{INL}	Vcc = 5V			3.5	V
PE1 and PE2 inputs, low current	I_{IL}	Vcc = Vcc max pins 6 & 7 =Vcc, V_{IN} = 0.4V	−4			mA
TTL output high voltage	V_{OH}	Vcc = Vcc min I_{OH} = − 640μA	2.3			V
TTL output low voltage	V_{OL}	Vcc = Vcc max I_{OL} = 20mA			0.5	V
TTL output short circuit current	I_{SC}	Vcc = Vcc max V_{out} = OV Pin 14 = Vcc	−80		−20	mA
Propagation delay CP to TTL output	tp	Vcc = 5V	6		14	ns
Propagation delay MS to TTL output	tp	Vcc = 5V			17	ns
Mode control set-up time	ts	Vcc = 5V	4			ns
Mode control release time	tr	Vcc = 5V	4			ns
TTL output rise time	t_{TLH}	Vcc = 5V			5	ns
TTL output fall time	t_{THL}	Vcc = 5V			5	ns
Power supply current	I_{EE}	Vcc = Vcc max, pins 6, 7 & 13 open			111	mA
Power supply voltage			4.75	5	5.5	V

Figure 1 **Block diagram**

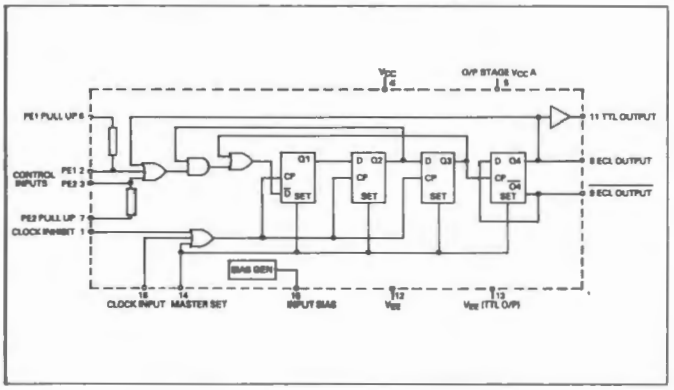


Table 1 **Truth Table**

MS	Clock Inh.	PE1	PE2	Output Response
H	X	X	X	All Outputs Set High
L	H	X	X	Hold
L	L	L	L	÷ 11
L	L	H	L	÷ 10
L	L	L	H	÷ 10
L	L	H	H	÷ 10

X = Don't care condition

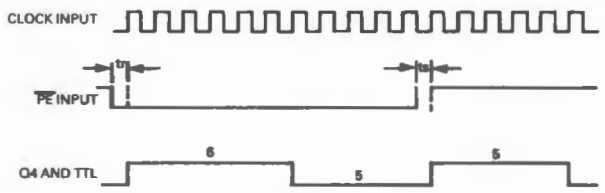
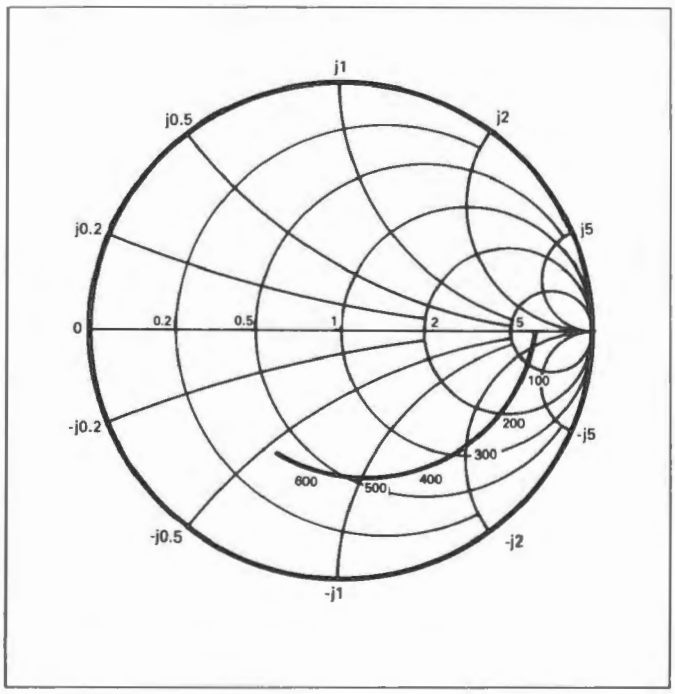


Figure 2 **Input Impedance**



Test conditions: Supply voltage 5V, ambient temperature 25°C, frequencies in MH_z and impedances normalised to 50Ω.

Applications

The clock input to the device is ECL compatible and can also be directly coupled to TTL when connected as shown in figure 3. The clock input can also be capacitively coupled to the signal source as shown in figure 4. When the internally generated bias voltage (pin 15) is connected to the clock input, the clock input becomes centred about the switching threshold see figures 4 and 5.

The two outputs provide complementary signals and are both ECL 10K compatible. Internal pull-down resistors are not included and hence must be added externally to V_{EE}. The outputs will drive a 50Ω load to −2V, the output high level will typically be reduced by 50mV.

The TTL output operates on the same supply and is powered up by connecting the V_{EE} (pin 12) to the TTL V_{EE} (pin 13). When the TTL output is not required pin 13 the TTL V_{EE} pin should be left open circuit reducing the power consumption by 20mW.

Both control inputs (PE1 and PE2) are ECL 10K compatible and each control input is provided with a pull up resistor the remote ends of which are connected to pins 6 and 7. This allows the pull up resistors to be used to interface from TTL or unused if not required. If interfacing to ECL is required then pins 6 and 7 should be left open circuit; alternatively they can be connected to V_{EE} to act as pull-down resistors. The master set input is used to set the counter to the eleventh state, when high it achieves this and is asynchronous and overrides the clock input.

All the inputs have internal 50K pull-down resistors, and operation will occur down to DC provided the input slew rate is better than 20V/μs.

The input impedance of the device is dependent on the input frequency. See the Smith Chart in figure 2.

All components used in the device circuits should be suitable for the frequencies involved and leads should be kept as short as possible to minimise stray inductance.

Figure 3 **TTL input configuration**

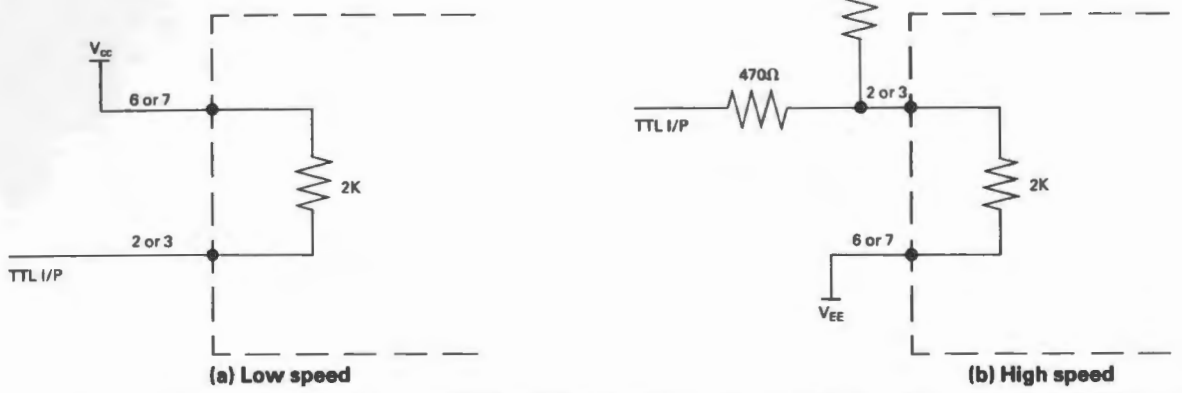


Figure 4 **AC coupled input**

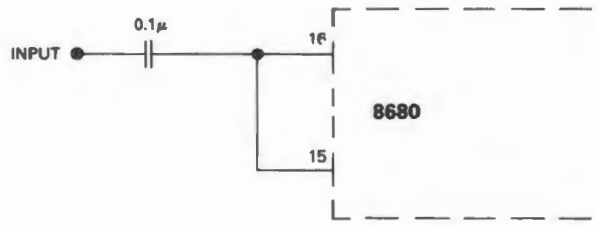
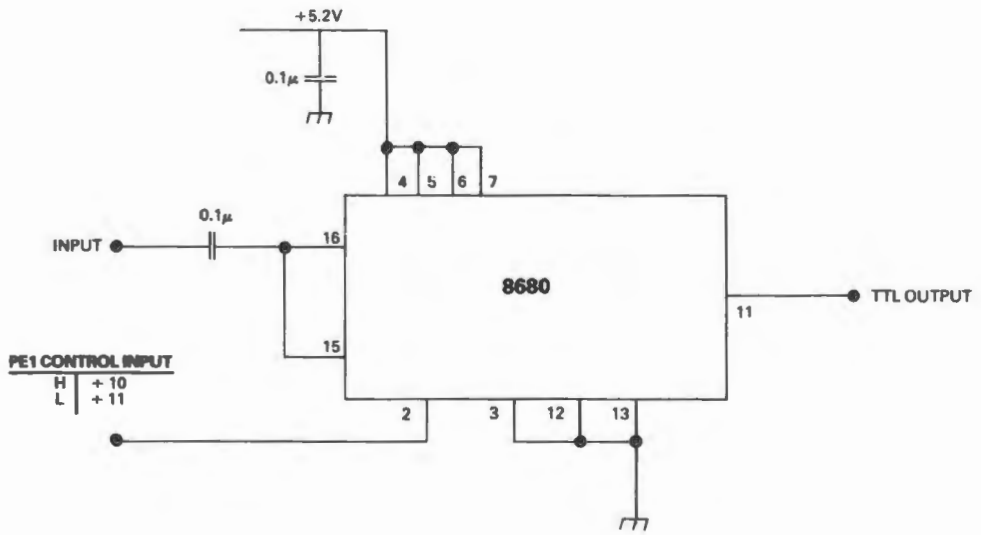


Figure 5 **Typical application circuit**



RS data

R.S. Components Ltd. 13-17 Epworth Street, London, EC2P 2HA
Telephone: 01-250 4000
For technical enquiries ring: 01-202 8252 or 0536-201234
An Electrocomponents Group Company

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RS data

Fast analogue to digital converter i.c. 3300.

Stock number 302—069

The 3300 CMOS fast analogue to digital converter is designed for use in applications requiring high speed and low power consumption. When operating from an 8V supply at a clock frequency of 15MHz the power consumption is less than 150mW. The high conversion rate of the 3300 makes it ideal for digitizing high speed signals. The overflow bit allows two or more 3300s to be connected in series to increase the resolution e.g. a 7-bit converter may be produced with two 3300s. Operation of two units in parallel doubles the conversion speed (e.g. at 8V operation the sampling rate may be increased from 15MHz to 30 MHz).

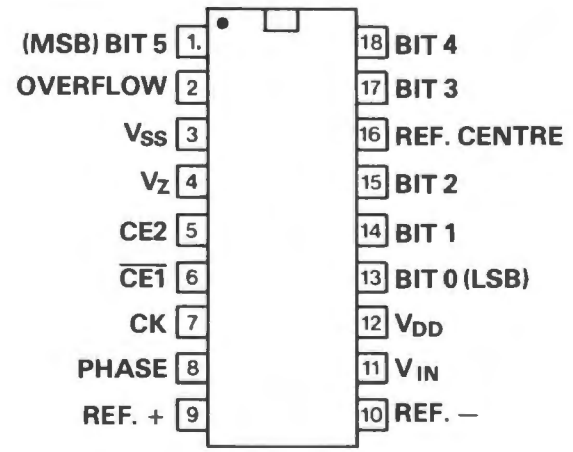
Sixty four paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs and sixty three comparators are used to quantize all input voltage levels with the additional comparator for the overflow bit.

Absolute maximum ratings

Supply voltage V_{DD} —— −0.5 to 10V
Input voltage except zener pin 4 −0.5 to V_{DD} +0.5V
DC input current CLK, PH, CE1, CE2 V_{IN} —— ±10mA
Power dissipation (derate by 3.3mW/°C above 55°C) —— 315mW
Operating temperature range —— −40 to +85°C
Storage temperature range —— −65 to +150°C
Lead temperature soldering 10s max. —— +265°C

Features

- CMOS lower power construction
- Fast parallel conversion technique
- 15MHz sampling rate, 66.6 ns conversion
- 6-bit latched, 3-state outputs with overflow bit
- ±½ LSB accuracy
- Single supply operation (4 to 10V)
- Internal voltage reference
- 2 units may be operated in series to give a 7-bit output
- 2 units may be operated in parallel giving up to 30MHz operation



TOP VIEW

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Electrical characteristics $T_A = -40$ to $+85°C$

Parameter	Conditions	Min.	Typ.	Max.	Units
Resolution				6	Bits
Linearity error	V_{DD}=8V, V_{REF}=7.68V, CLK = 15MHz gain adjusted		±0.5	±0.8	LSB
Differential linearity error	V_{DD} = 8V, V_{REF} = 7.68V CLK = 15MHz		±0.5	±0.8	LSB
Quantizing error		−½		+½	LSB
Gain temperature co-efficient	V_{DD} =8V, CLK = 15MHz		0.016		LSB/°C
Analogue input range	V_{DD}=8V, CLK=15MHz	0 to 2.4		0 to V_{DD} +0.5	V
Input capacitance			50		pF
Input current			600	1000	μA
Reference input		2.5		V_{DD}	V
Digital inputs					
Low voltage	V_{DD}=5V			1.5	V
	V_{DD}=8V			2.5	V
High voltage	V_{DD}=5V	3.5			V
	V_{DD}=8V	5.5			V
Input current	V_{DD}=8V		±1		μA
Digital outputs					
Output low (sink) current	V_{DD}=5V, Vo=0.4V	1.6	10		mA
	V_{DD}=8V, Vo=0.5V	3.2	15		mA
Output high (source) current	V_{DD}=5V, Vo=4.6V	−0.8	6		mA
	V_{DD}=8V, Vo=7.5V	−1.6	9		mA
Maximum conversion speed	V_{DD}=5V		12		M. samples /sec.
	V_{DD}=8V	15	19		
Ladder impedance		1000	1400	1800	
Zener voltage	I_Z=10mA	5.8	6.4	7	V
Zener dynamic impedance	I_Z=10mA		10	30	Ω
Zener temperature coefficient			0.5		mV/°C
Digital output delay	V_{DD}=8V		20		ns
Aperture time	V_{DD}=8V		25		ns
Device current (Excluding I_{REF} & I_Z)	V_{DD}=5V CLK=11MHz		7		mA
	V_{DD}=8V CLK=15MHz		22		mA
	V_{DD}=5V Auto Balance state		6.4	16	mA
	V_{DD}=8V Auto Balance state		24	40	mA
Supply voltage		3		10	V

Operation

A sequential parallel conversion technique is used to obtain high speed operation. The sequence consists of the 'Auto Balance' phase Ø1 and the 'sample unknown' phase Ø2 see block diagram figure 1. Each conversion takes one clock cycle. With the phase control pin 8 low, the 'Auto Balance' phase Ø1 occurs during the high period of the clock cycle, and the 'sample unknown' Ø2 occurs during the low period of the clock cycle.

During the 'Auto Balance' phase a transmission switch is used to connect each of 64 commutating capacitors to their associated ladder reference taps.

The tap voltages will be:

$$V_{tap}(N) = [(V_{REF}/64) \times N] - [V_{REF}/2 \times 64]$$

$$V_{tap}(N) = V_{REF}\left[\frac{(2N-1)}{128}\right]$$

$V_{tap}(N)$ = reference ladder tap voltage at point N

V_{REF} = Voltage across REF + and REF −

N = tap number (1 through 64)

The other side of the capacitor is connected to a single stage amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately:

$$\frac{(V_{DD} - V_{SS})}{2}$$

The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the 'sample unknown' phase, all ladder tap switches are opened the comparator amplifiers are no longer shorted and V_{in} is switched to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators with tap voltages greater than V_{in} will drive the comparator outputs to a low state, all comparators with tap voltages lower than V_{in} will drive the comparator outputs to a high state. The status of all these comparator amplifiers is stored at the end of this Ø2 phase by a secondary latching amplifier stage. Once latched, the status of

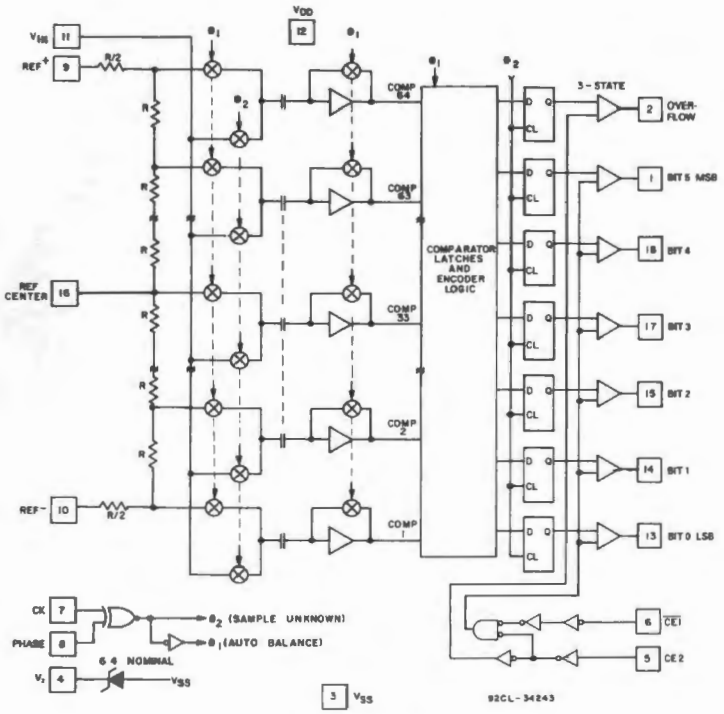


Figure 1 **Block diagram**

the 64 comparators is decoded by a 64 to 7-bit decode array and the results are clocked into a storage register at the rising edge of the next Ø2 phase.

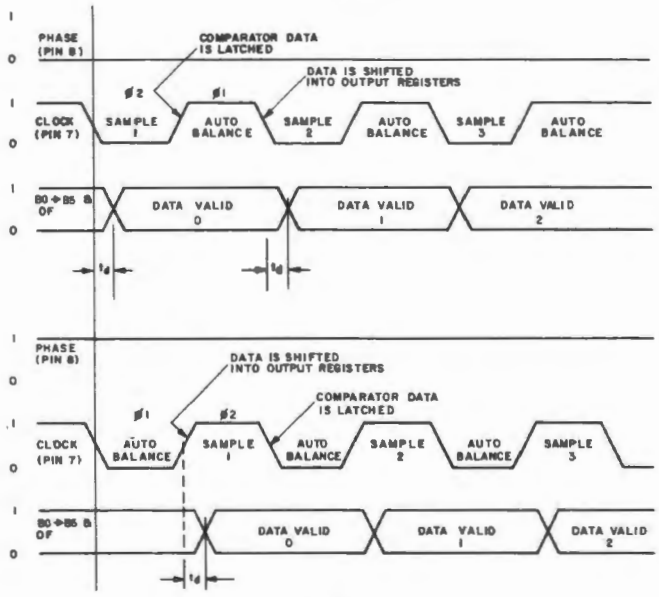
A 3-state buffer is used at the output of the 7 storage registers which are controlled by two chip enable signals. CE1 will independently disable BO through B5 when it is in a high state. CE2 will independently disable BO through B5 and the overflow buffers when it is in the low state.

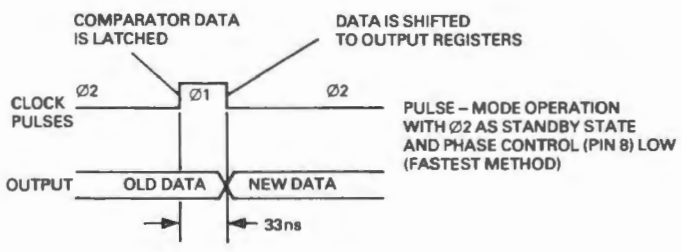
To ease operation a phase control input is provided which can be used to complement the clock as it enters the chip. Also an internal zener is provided for use as a reference.

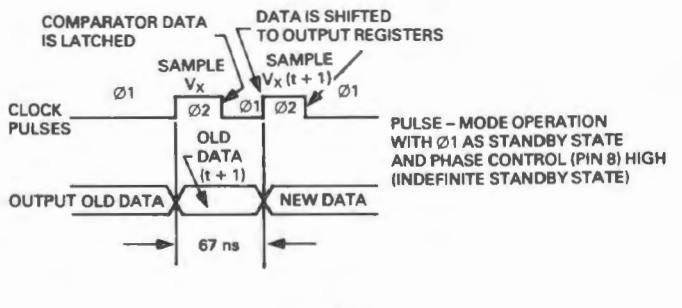
Continuous clock operation

One complete conversion cycle can be traced through the 3300 with the aid of the timing diagram figure 2a. When the phase control input is in the high state the rising edge of the clock input will start a 'sample' phase. During the high state of the clock the 64 comparators will track the input voltage and the 64 latches will follow the comparator outputs. At the falling edge of the clock all the 64 comparator outputs are stored by the latches. This ends the 'sample' phase and starts the 'Auto Balance' phase for the comparators. During this low state of the clock the outputs of the latches propagate through the decode array and a 7-bit code appears at the D inputs of the output registers. On the next rising edge of the clock this 7-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new 'sample' phase thereby repeating the conversion process.

Figure 2 **Timing diagram for the 3300**







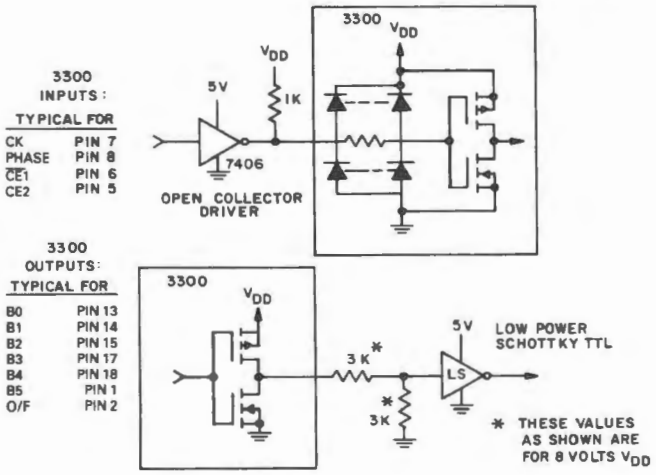
Pulse mode operation

For sampling high speed non-recurrent or transient data the converter may be operated in a pulse mode. The fastest method is to keep the converter in the 'sample unknown' ∅2 phase during the standby state.

The device can now be pulsed through the 'Auto Balance' phase in as little as 33ns. The analogue value is captured on the leading edge of ∅1 and is transferred into the output registers on the trailing edge of ∅1. We are now back in the standby state ∅2 and another conversion can be started within 33 ns, but not later than 10 μs due to the eventual droop of the computing capacitors. The main advantage of this method is that it has the lowest power drain. The larger the time ratio between ∅2 and ∅1 the lower the power consumption see figure 2b.

The second pulse mode method uses the 'Auto Balance' ∅1 phase as the standby state. In this state

Figure 3 **TTL interface circuit for V_{DD} >5.5 volts**



the converter can stay indefinitely waiting to start a conversion. A conversion is initiated by strobing the clock input with two ∅2 pulses. The first pulse starts a 'sample unknown' phase and captures the analogue value in the comparator latches on the trailing edge. A second ∅2 pulse is needed to transfer the data into the output registers, this occurs on the leading edge of the second pulse. The conversion now takes place in 67 ns, but the repetition rate may be as slow as desired. The shortcoming is in the high device power consumption due to the low ratio of ∅2 to ∅1 see figure 2c.

Figure 4 **Typical 6-bit configuration 15-MHz sampling rate**

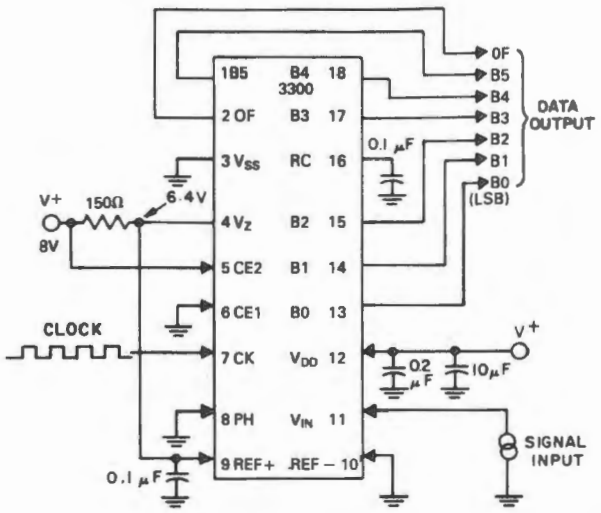


Figure 5 **Typical 6-bit resolution configuration 30-MHz sampling rate.**

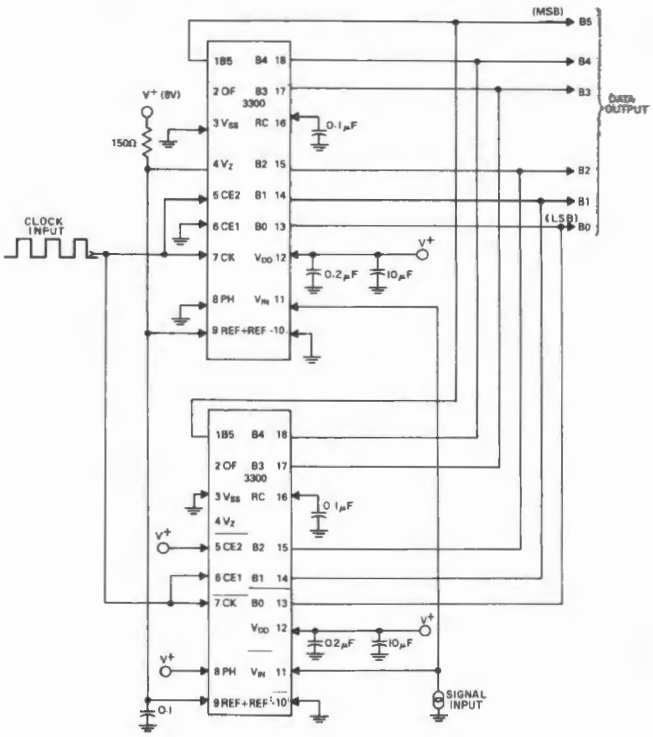


Table 1 **Output coding**

CODE DESCRIPTION	INPUT VOLTAGE* VREF 6.40 (VOLTS)	VREF 3.20 (VOLTS)	BINARY OUTPUT CODE (LSB) 0.F B5 B4 B3 B2 B1 B0	DECIMAL COUNT
ZERO	0.00	0.00	0 0 0 0 0 0 0	0
1 LSB	0.10	0.05	0 0 0 0 0 0 1	1
2 LSB	0.20	0.10	0 0 0 0 0 1 0	2
½ Full Scale – 1 LSB	3.10	1.55	0 0 1 1 1 1 1	31
½ Full Scale	3.20	1.60	0 1 0 0 0 0 0	32
½ Full Scale + 1 LSB	3.30	1.65	0 1 0 0 0 0 1	33
Full Scale – 1 LSB	6.20	3.10	0 1 1 1 1 1 0	62
Full Scale	6.30	3.15	0 1 1 1 1 1 1	63
Overflow	6.40	3.20	1 1 1 1 1 1 1	127

*THE VOLTAGES LISTED BELOW ARE THE IDEAL CENTRES OF EACH OUTPUT CODE SHOWN AS A FUNCTION OF ITS ASSOCIATED REFERENCE VOLTAGE.

Calibration techniques for increased accuracy

In most applications the accuracy of the 3300 should be sufficient without any setting up adjustments. In applications where accuracy is of utmost importance three calibration adjustments can be made to obtain improved accuracy these are offset trim, gain trim and midpoint trim.

Offset Trim

Generally offset correction can be performed in the preamp by introducing a dc shift to V_{in} or by the offset trim of the op amp. When this is not possible the REF − pin 10 input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is ½ LSB i.e.:

V_{in} (first 0 to 1 transition) = ½ LSB ($V_{REF}/64$)

$= V_{REF}/128$

If V_{in} for the first transition is less than the theoretical value then a 50Ω trimmer connected between REF- and ground can be used. Set V_{in} to ½ LSB i.e. $V_{REF}/64$ and trim until the 0 to 1 transition occurs.

If V_{in} for the first transition is greater than the theoretical value then a 50Ω trimmer should be connected between REF − and a negative voltage about 2 LSBs ≈ $V_{REF}/32$) less than the previous voltage. Set V_{in} to ½ LSB and trim for the 0 to 1 transition.

Gain Trim

In general the gain trim can also be performed in the preamp by introducing a gain adjustment for the op amp. When this is not possible then a gain adjustment circuit should be made to adjust the reference voltage. To perform the gain trim set the input voltage V_{in} to ½ LSB less than V_{REF} i.e. 63 to 64 transition = $V_{REF} - V_{REF}/128$ i.e.

$$V_{in} = V_{REF}\frac{127}{128}$$

and adjust V_{REF} until the 63 to overflow 64 transition occurs. Offset trim should be carried out prior to this adjustment.

Midpoint trim

The reference centre pin 16 is available to the user as the approximate midpoint of the resistor ladder. The actual count that is brought out is count 33. Before midpoint trimming offset and gain trims should be done first. The theoretical transition from count 32 to 33 occurs at 33½ LSBs i.e.:

V_{in} (32 to 33 transition) = 32.5 ($V_{REF}/64$).

An adjustable voltage follower can be connected to the reference centre or a 2K preset can be connected between REF + and REF − with the wiper connected to the reference centre. V_{IN} is set to the 32 to 33 transition voltage i.e. 32.5 ($V_{REF}/64$) and the voltage follower output or preset is adjusted until the output transition occurs.

The reference centre point can also be used to create some unique converter transfer characteristics. E.g. if REF − is at ground potential Reference centre is connected to 3.25 volts and REF + is connected to 4.8 volts, then the lower order counts 1 through 33 will have an LSB value of 100mV while the upper counts 34 through overflow will have an LSB value of 50mV. This set up effectively provides twice the sensitivity in the upper counts as compared to the lower counts.

High speed 30MHz operation with two 3300s

A high speed 30MHz 6-bit converter may be configured using two 3300s as shown in figure 5. The phase control signals are set to complement the clock input inside one converter and change the conversion phases between the two devices allowing them to operate alternately. CE2 and CE1 inputs are configured so the outputs provide the digital information alternately giving the system an overall operating speed of up to 30MHz.

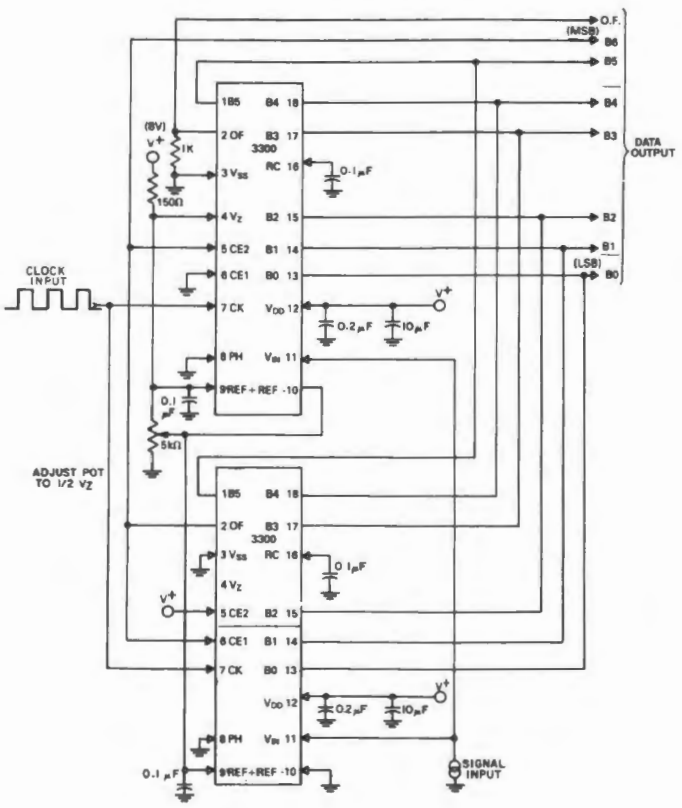
7-bit resolution with two 3300s

The 3300s feature open ended ladder networks and overflow outputs which allow two devices to be operated together to give 7-bit resolution.

For 7-bit operation the resistor ladder networks are connected together as in figure 6, since the absolute resistance value of each ladder may vary external trim of the mid-reference voltage may be required.

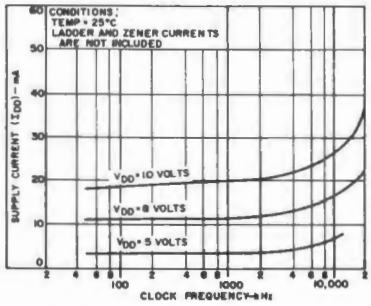
The overflow output of the lower device now becomes the seventh bit. When it goes high all counts come from the upper device, and when it goes low all counts come from the lower device. This is achieved by connecting the lower overflow signal to the CE1 control of the lower *a* to *d* converter and the CE2 control of the upper *a* to *d* converter. The three-state outputs of the two devices (bits 0 through 5) are now connected in parallel to complete the circuitry, see figure 6.

Figure 6 **Typical 7 bit resolution configuration 15-MHz sample rate**

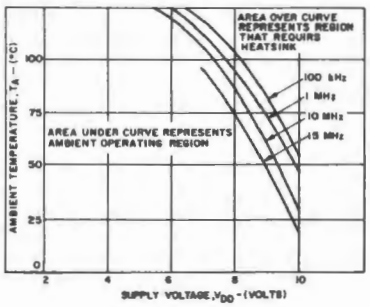


RS data

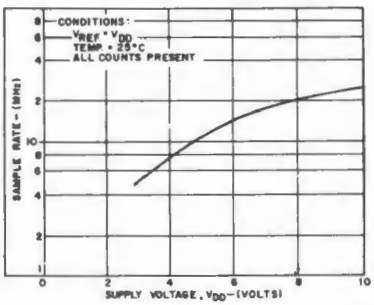
Figure 7 **Characteristic graphs**



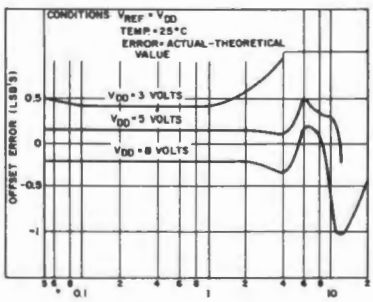
Typical current drain versus sampling rate as a function of supply voltage.



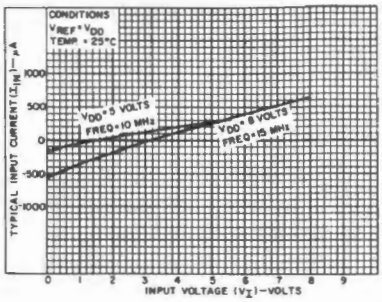
Maximum ambient temperature versus supply voltage. (Above curve includes ladder dissipation but not the zener dissipation.)



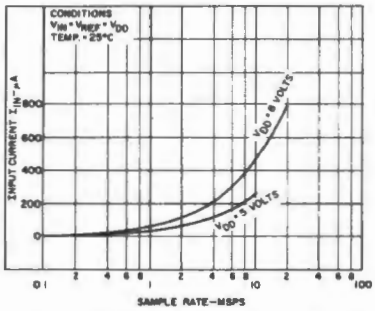
Typical maximum sample rate versus supply voltage.



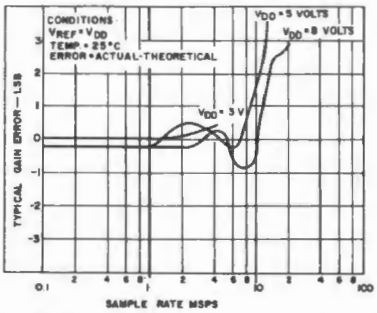
Typical offset error versus sample rate as a function of supply voltage. (See literature for offset trim.)



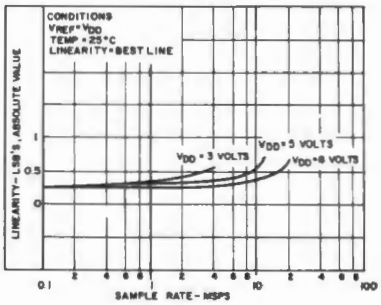
Typical input current versus input voltage as a function of supply voltage.



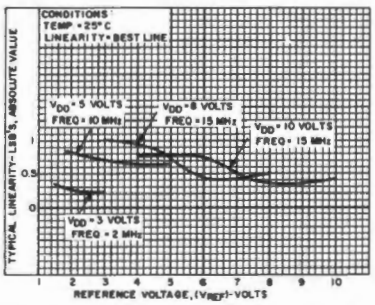
Typical input current versus sample rate as a function of supply voltage.



Typical gain error versus sample rate as a function of supply voltage. (See literature for gain trim.)



Typical linearity versus sample rate as a function of supply voltage.



Typical linearity versus reference voltage as a function of supply voltage.

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RS data

Microprocessor compatible real time clock i.c. 146818

Stock number 302—003

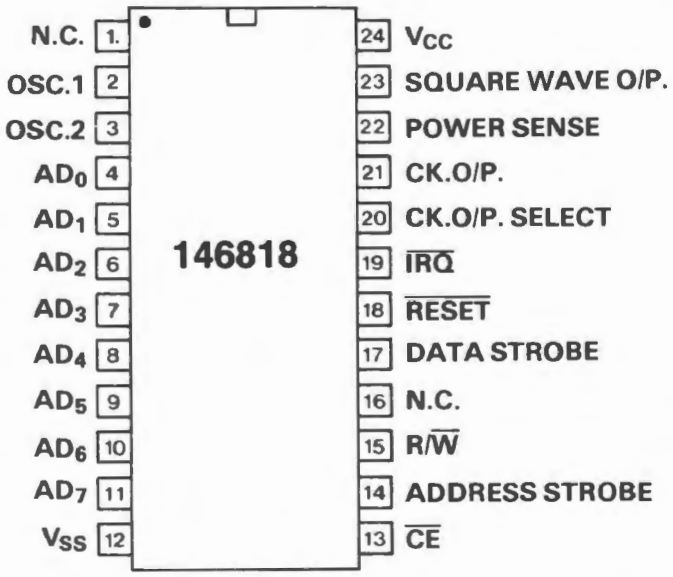
The 146818 is a 6800 peripheral CMOS device which combines three unique features: a complete time-of-day clock with alarm, calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of Low-power static RAM. This device includes 6800 multiplexed bus interface circuit and 8085s multiplexed bus interface as well, so it can be directly connected to 8085 etc.
The Real-Time Clock plus RAM has two distinct uses. First, it is designed as a battery powered CMOS part including all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the 146818 may be used with a CMOS microprocessor to relieve the software of time-keeping work-load and to extend the available RAM of an MPU.

Absolute maximum ratings

Supply voltage V_{CC} ——— −0.3 to +7.0V
Input voltage ——— −0.3 to +7.0V
Operating temperature range ——— 0 to 70°C
Storage temperature range ——— −55 to +150°C

Features

- Time-of-Day Clock and Calendar
  - Counts Seconds, Minutes, and Hours of the Day
  - Counts Days of Week, Date, Month, and Year
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12- or 24 Hour Clock with AM and PM in 12-Hour Mode
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Interfaced with Software as 64 RAM Locations
  - 14 Bytes of Clock and Control Register
  - 50 Bytes of General Purpose RAM
- Three Interrupts are Separately Software Maskable and Testable
  - Time-of-Day Alarm, Once-per-Second to Once-per-Day
  - Periodic Rates from 30.5μs to 500ms
  - End-of-Clock Update Cycle
- Programmable Square-Wave Output Signal
- Three Time Base Input Options
  - 4.194304MHz
  - 1.048576MHz
  - 32.768kHz
- Clock Output may be used as Microprocessor Clock Input
  - At Time Base Frequency ÷ 4 or ÷ 1
- Multiplexed Bus Interface Circuit
- Low-Power, High-Speed, High-Density CMOS



TOP VIEW

Electrical characteristics D.C. (V_{CC} = 5.0V ± 10%, V_{SS} = 0V, Ta = 0 to + 70°C, unless otherwise noted.)

Parameter		Symbol	Test Condition	min	typ	max	Unit
Supply voltage	V_{CC}			4.5	5.0	5.5	V
Input voltage	V_{IL}			−0.3	–	0.7	V
	V_{IH}			V_{CC} −1.0	–	V_{CC}	V
Operating temperature	T_{opr}			0	25	70	°C
Input "High" voltage	$AD_0 \sim AD_7$, $\overline{CE}$, AS, $R/\overline{W}$, DS, CKFS, PS	V_{IH}		V_{CC} −2.0	–	V_{CC}	V
	$\overline{RES}$			V_{CC} −1.0	–	V_{CC}	
	OSC_1			V_{CC} −1.0	–	V_{CC}	

* The time base frequency to be used needs to be chosen in Register A.

Input "Low" voltage	$AD_0 \sim AD_7$, $\overline{CE}$, AS, R/$\overline{W}$, DS, CKFS, PS	V_{IL}		–0.3	–	0.7	V
	$\overline{RES}$			–0.3	–	0.8	
	OSC_1			–0.3	–	0.8	
Input Leakage Current	OSC_1, $\overline{CE}$, AS, R/$\overline{W}$, DS, $\overline{RES}$, CKFS, PS	$\|I_{in}\|$		–	–	2.5	μA
Three-state (off state) Input Current	$AD_0 \sim AD_7$	$\|I_{TSI}\|$		–	–	10	μA
Output Leakage Current	$\overline{IRQ}$	I_{LOH}		–	–	10	μA
Output "High" Voltage	$AD_0 \sim AD_7$	V_{OH}	$I_{OH} = -1.6mA$	4.1	–	–	V
	SQW, CKOUT						
	$AD_0 \sim AD_7$		$I_{OH} < -10\ \mu A$	V_{CC} –0.1	–	–	
	SOW, CKOUT						
Output "Low" Voltage	$AD_0 \sim AD_7$	V_{OL}	$I_{OL} = 1.6mA$	–	–	0.5	V
	CKOUT		$I_{OL} = 1.6mA$				
	$\overline{IRQ}$, SQW		$I_{OL} = 1.6mA$				
Input Capacitance	$AD_0 \sim AD_7$	C_{IN}	$V_{IN} = 0V$ Ta = 25°C f = 1 MHz	–	–	12.5	pF
	All inputs except $AD_0 \sim AD_7$			–	–	12.5	
Output Capacitance	SQW, CKOUT, $\overline{IRQ}$	C_{out}		–	–	12.5	
Supply Current (MPU Read/ Write operating)	Crystal Oscillation f_{OSC} = 4MHz	I_{CC}*	$V_{CC} = 5.0V$ SQW: disable CKOUT = f_{OSC} (No Load) $t_{CYC} = 1\ \mu s$ Circuit: Fig. 10 Parameter: Table 1	–	–	10	mA
	f_{OSC} = 1MHz			–	–	7	
	f_{OSC} = 32kHz			–	–	5	
Supply Current (MPU not operating)	f_{OSC} = 4MHz			–	–	5	
	f_{OSC} = 1MHz			–	–	2	
	f_{OSC} = 32kHz			–	300	500	μA
Supply Current (MPU Read/ Write Operating)	External Clock f_{OSC} = 4MHz	I_{CC}*	$V_{CC} = 5.0V$ SQW: disable CKOUT = f_{OSC} (No Load) OSC_2: open $t_{CYC} = 1\ \mu s$ Circuit: Fig. 15	–	–	10	mA
	f_{OSC} = 1MHz			–	–	7	
	f_{OSC} = 32kHz			–	–	5	
Supply Current (MPU not operating)	f_{OSC} = 4MHz			–	–	4	
	f_{OSC} = 1MHz			–	–	1	
	f_{OSC} = 32kHz				60	100	μA

Electrical characteristics

Low voltage standby operation

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Supply voltage	V_{CCL}		2.7		4.5	V
Supply current	I_{CCL}	V_{CCL} = 3.0V SQW disabled CK OUT = f_{OSC}				
		XTAL 4MHz			600	μA
		XTAL 1MHz			350	μA
		XTAL 32kHz		50	100	μA
		EXTERNAL 4MHz			500	μA
		EXTERNAL 1MHz			150	μA
		EXTERNAL 32kHz		30	70	μA
Set up time to low voltage operation	t_{CE}		0			ns
Set up time to normal voltage operation	t_r		t_{cyc}(953)			ns
Fall time of V_{CC}	t_{pf}		300			μs
Rise time of V_{CC}	t_{pr}		300			μs
Input high level $\overline{CE}$, CKFS		$V_{CC}L$ = 2.7 to 3.5V	0.7 x $V_{CC}L$		$V_{CC}L$	V
PS	V_{ihL}	$V_{CC}L$ = 3.5 to 4.5V	2.5		$V_{CC}L$	V
Input high level $\overline{RES}$			0.8 x $V_{CC}L$		$V_{CC}L$	V
Input high level OSC1			0.8 x $V_{CC}L$		$V_{CC}L$	V
Input low level CKFS, PS	V_{iLL}		–0.3		0.5	V
$\overline{RES}$			–0.3		0.5	V
OSC1			–0.3		0.5	V
Output high level	V_{ohL}	I_{OH} = –800μA/	-0.8 x V_{cc}			
Output low level	V_{oLL}	I_{OL} = –800μA/			0.5	V
SQW, CKOUT, $\overline{IRQ}$						

AC CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, Ta = 0 ~ +70°C, unless otherwise noted.)

Bus Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Cycle Time	t_{cyc}	953	–	–	ns
Pulse Width, AS/ALE "High"	PW_{ASH}	100	–	–	ns
AS Rise Time	t_{ASr}	–	–	30	ns
AS Fall Time	t_{ASf}	–	–	30	ns
Delay Time DS/E to AS/ALE Rise	t_{ASD}	40	–	–	ns
DS Rise Time	t_{DSr}	–	–	30	ns
DS Fall Time	t_{DSf}	–	–	30	ns
Pulse Width, DS/E Low or $\overline{RD}$/$\overline{WR}$ "High"	PW_{DSH}	325	–	–	ns
Pulse Width, DS/E High or $\overline{RD}$/$\overline{WR}$ "Low"	PW_{DSL}	300	–	–	ns
Delay Time, AS/ALE to DS/E Rise	t_{ASDS}	90	–	–	ns
Address Setup Time (R/$\overline{W}$)	t_{AS1}	15	–	–	ns
Address Setup Time ($\overline{CE}$)	T_{AS2}	55	–	–	ns
Address Hold Time (R/$\overline{W}$, $\overline{CE}$)	t_{AH}	10	–	–	ns
Muxed Address Valid Time to AS/ ALE Fall	t_{ASL}	50	–	–	ns
Muxed Address Hold Time	t_{AHL}	20	–	–	ns
Peripheral Data Setup Time	t_{DSW}	195	–	–	ns
Write Data Hold Time	T_{DHW}	0	–	–	ns
Peripheral Output Data Delay Time from DS/E or $\overline{RD}$	t_{DDR}	–	–	220	ns
Read Data Hold Time	t_{DHR}	10	–	–	ns

Control Signal Timing

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Oscillator Startup	1 MHz, 4 MHz	t_{RC}	–	–	100	ms
	32 kHz		–	–	1000	
Reset Pulse Width		t_{RWL}	5.0	–	–	μS
Reset Delay Time		t_{RLH}	5.0	–	–	μS
Power Sense Pulse Width		t_{PWL}	5.0	–	–	μS
Power Sense Delay Time		t_{PLH}	5.0	–	–	μS
$\overline{IRQ}$ Release from DS		t_{IRDS}	–	–	2.0	μS
$\overline{IRQ}$ Release from $\overline{RES}$		t_{IRR}	–	–	2.0	μS
VRT Bit Delay		t_{VRTD}	–	–	2.0	μS

Figure 1 **Bus read, write timing** (6800 family)

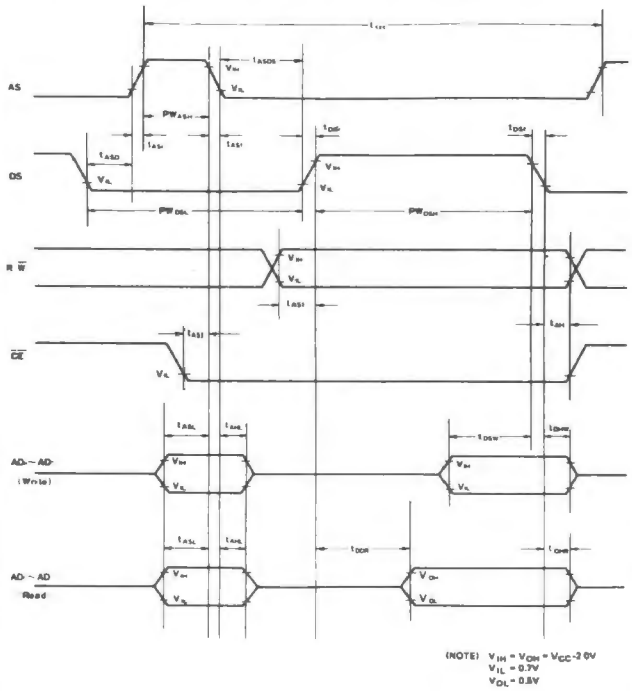


Figure 2 **Read timing** (8085 family)

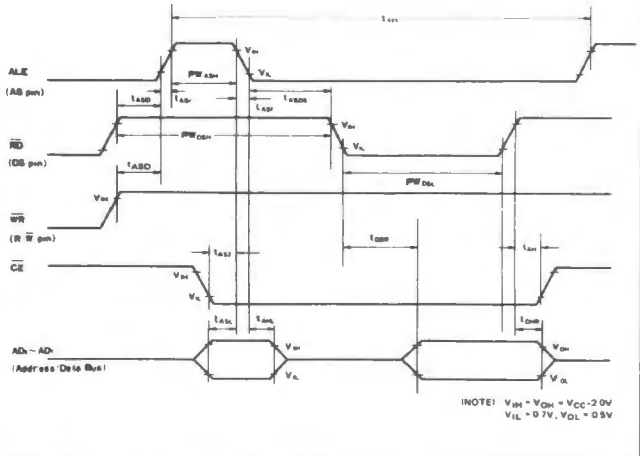


Figure 3 **Write timing** (8085 family)

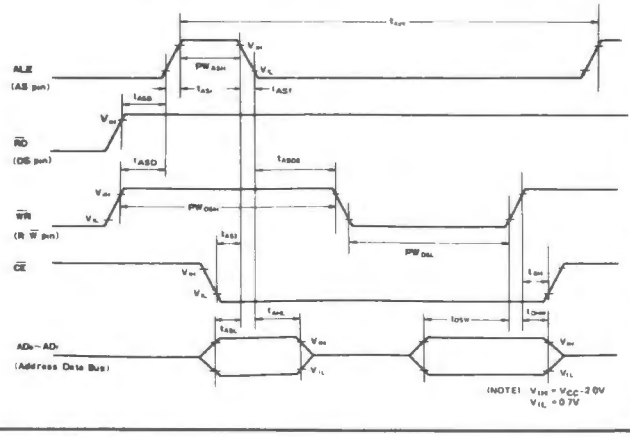


Figure 4 **$\overline{IRQ}$ Release Delay (from DS)**

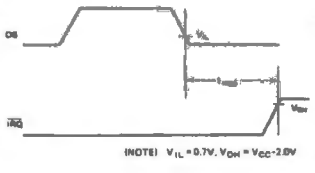


Figure 5 **$\overline{IRQ}$ Release Delay (from RES)**

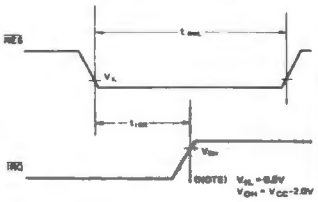
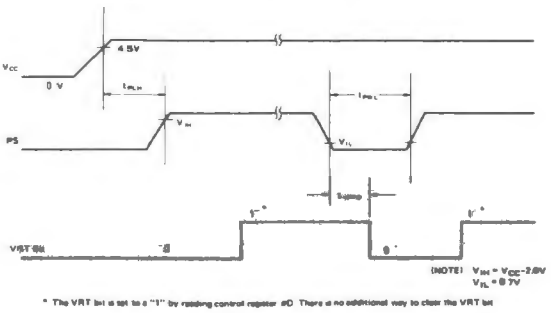


Figure 6 **VRT Bit Clear Timing**



* The VRT bit is set to a "1" by reading control register #0. There is no additional way to clear the VRT bit.

Figure 7 **$\overline{RES}$ Release Delay**

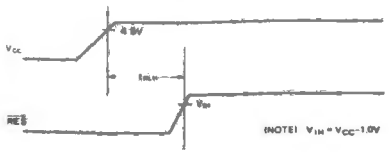


Figure 8 **Test Load**

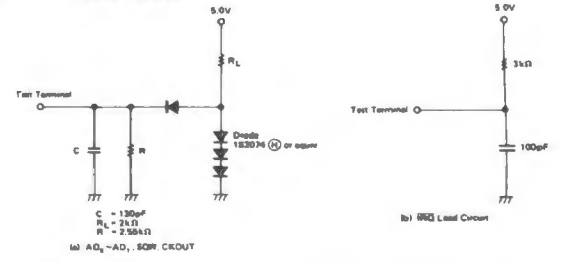
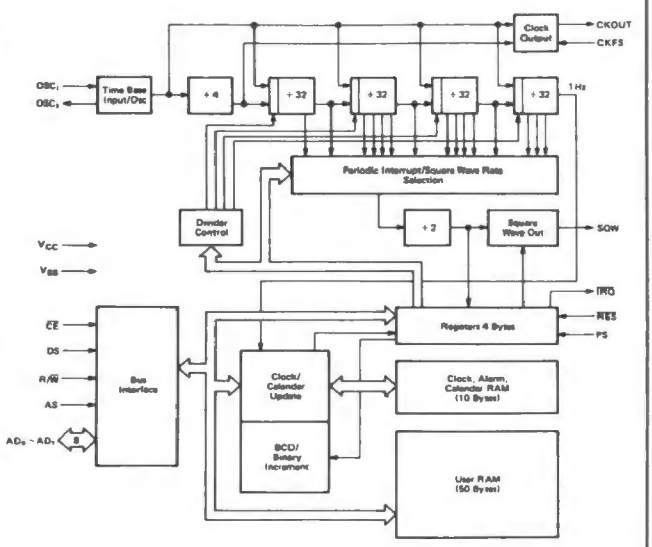


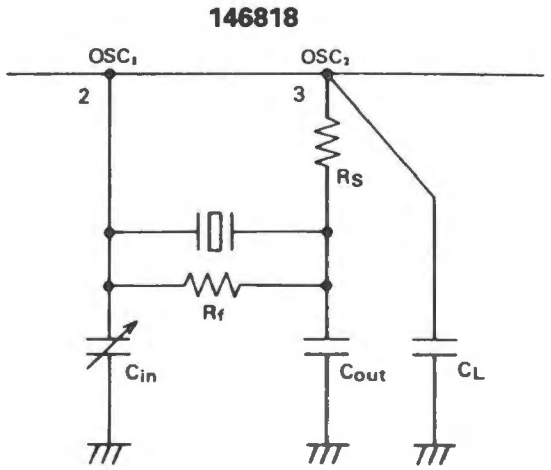
Figure 9 **Block Diagram**



Crystal Oscillation Circuit

The on-chip oscillator is designed for a parallel resonant crystal at 4.194304 MHz or 1.048576MHz or 32.768kHz frequencies. The crystal connections are shown in Figure 10.

Figure 10 **Crystal Oscillator Connection**



Note for Board Design of the Oscillation Circuit

In designing the board, the following notes should be taken when the crystal oscillator is used.

(1) Crystal oscillator, load capacity C_{in}, C_{out}, C_L and R_f, R_S must be placed as near to the 146818 as possible.
(Normal oscillation may be disturbed when external noise is induced to pin 2 and 3.)

(2) Pin 3 signal line should be wired apart from pin 4 signal line as much as possible. Don't wire them in parallel, or normal oscillation may be disturbed when this signal is fed back to OSC_1.

(3) A signal line or a power source line must not cross or go near the oscillation circuit line as shown in the right figure to prevent the induction from these lines and perform the correct oscillation. The resistance between OSC_1, OSC_2 and other pins should be over 10MΩ.

Figure 11 **Note for Board Design of the Oscillation Circuit**

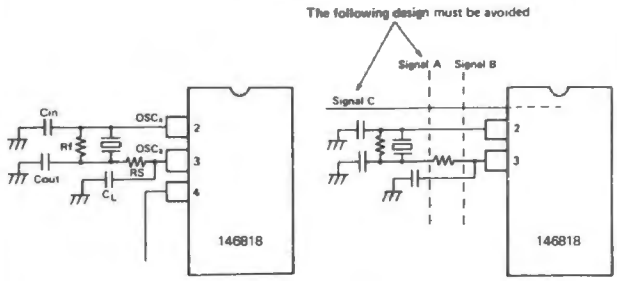


Table 1 **Oscillator Circuit Parameters**

Parameter \ f_{OSC}	4.194304 MHz	1.048576MHz	32.768kHz
R_S	–	–	150kΩ
R_f	150kΩ	150kΩ	5.6MΩ
C_{in}	22pF	33pF	15pF
C_{out}	22pF	33pF	33pF
C_L	–	–	33pF
CI	80Ω (max)	700Ω (max)	40kΩ (max)

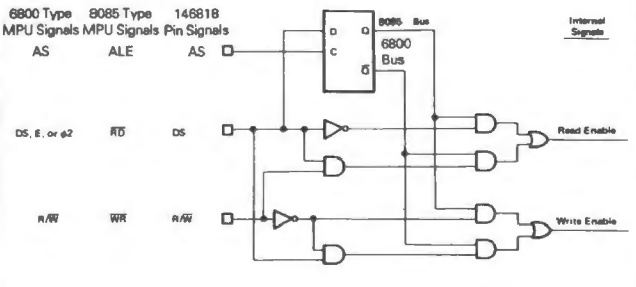
Note:
1. R_S, C_L are used for 32.768 kHz only.
2. Capacitance (C_{in}) should be adjusted to accurate frequency. Parameters listed above are applied to the supply current measurement (see table of DC CHARACTERISTICS).
3. CI: Crystal Impedance.

Interface Circuit for Processors 6800, 8085 etc.

The 146818 has a new interface circuit which permits the 146818 to be directly interfaced with many type of multiplexed bus microprocessors such as 6800 and 8085 etc.

Figure 12 shows the bus control circuit. This circuit automatically selects the processor type by using AS/ASE to latch the state of DS/$\overline{RD}$ pin. Since DS is always "Low" and $\overline{RD}$ is always "High" during AS/ALE, the latch automatically indicates which processor type is connected.

Figure 12 **Functional Diagram of the Bus Control Circuit**



Address Map

Figure 13 shows the address map of the 146818. The memory consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes. All 64 bytes are directly readable and writeable by the processor program except

Registers C and D which are read only. Bit 7 of Register A and the seconds byte are also read only. Bit 7, of the second byte, always reads "0". The contents of the four control and status registers are described in the Register section.

Time, Calendar and Alarm Locations

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm byte may be either binary or binary-coded decimal (BCD).

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

Figure 13 **Address Map**

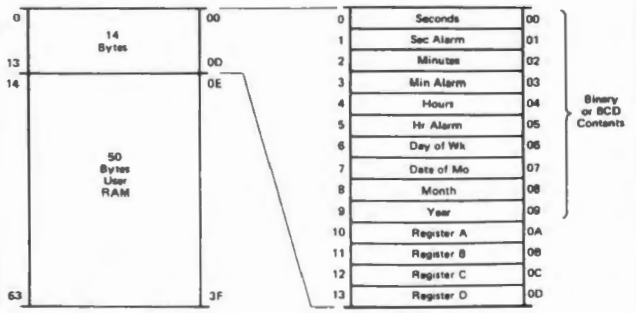


Table 2 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order of the hours byte represents PM when it is a "1".

The time, calendar, and alarm bytes are not always accessible by the processor program. Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 248 μs at the 4.194304MHz and 1.048567MHz time bases and 1948 μs for the 32.768kHz time base. The Update Cycle section shows how to accommodate the update cycle in the processor program.

The three alarm bytes may be used in two ways. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specific time each day if the alarm enable bit is "1". The alternate usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from C0 to FF. That is, the two most-significant bits of each byte, when set to "1", create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Table 2 **Time, Calendar, and Alarm Data Modes**

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0~59	$00~$3B	$00~$59	15	21
1	Seconds Alarm	0~59	$00~$3B	$00~$59	15	21
2	Minutes	0~59	$00~$3B	$00~$59	3A	58
3	Minutes Alarm	0~59	$00~$3B	$00~$59	3A	58
4	Hours (12 Hour Mode)	1~12	$01 ~ $0C (AM) and $81 ~ $8C (PM)	$01 ~ $12 (AM) and $81 ~ $92 (PM)	05	05
	Hours (24 Hour Mode)	0~23	$00~$17	$00~$23	05	05
5	Hours Alarm (12 Hour Mode)	1~12	$01 ~ $0C (AM) and $81 ~ $8C (PM)	$01 ~ $12 (AM) and $81 ~ $92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0~23	$00~$17	$00~$23	05	05
6	Day of the Week Sunday = 1	1~7	$01~$07	$01~$07	05	05
7	Day of the Month	1~31	$01~$1F	$01~$31	0F	15
8	Month	1~12	$01~$0C	$01~$12	02	02
9	Year	0~99	$00~$63	$00~$99	4F	79

*** Example: 5:58:21 Thursday 15th February 1979**

Static CMOS RAM

The 50 general purpose RAM bytes are not dedicated within the 146818. They can be used by the processor program, and are fully available during the update cycle.

When time and calendar information must use battery back-up, very frequently there is other non-volatile data that must be retained when main power is removed. The 50 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program.

The time/calendar functions may be disabled by holding the dividers, in Register A, in the reset state by setting the SET bit in Register B or by removing the oscillator. Holding the dividers in reset prevents interrupts or SQW output from operating while setting the SET bit allows these functions to occur. With the dividers clear, the available user RAM is extended to 59 bytes. Bit 7 of Register A, Registers C and D, and the high-order Bit of the seconds byte cannot effectively be used as general purpose RAM.

Interrupts

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 μs. The update-ended interrupt may be used to indicate to the program that an up-date cycle is completed. Each of these independent interrupt conditions is described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the $\overline{IRQ}$ pin is immediately activated, though the interrupt indicating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit, which the software interrogates, when it wishes. When the software detects that the flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held until after the read cycle. One, two, or three flag bits may be found to be set when Register C is read. The program should inspect all utilised flag bits every time Register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt-flag is set and the corresponding interrupt-enable bit is also set, the $\overline{IRQ}$ pin is asserted "Low". $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a "1" whenever the $\overline{IRQ}$ pin is being driven "Low".

The processor program can determine that the RTC initiated the interrupt by reading Register C. A "1" in bit 7 (IRQF bit) indicates that one of more interrupts have been initiated by the part. The act of reading Register C clears all the then-active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bits set and service each interrupt which is set. Again, more than one interrupt-flag bit may be set.

DIVIDER STAGES

The 146818 has 22 binary-divider stages following the time base as shown in Figure 9. The output of the dividers is a 1Hz signal to the update-cycle logic. The dividers are controlled by three divider bits (DV2, DV1, and DV0) in Register A.

Divider Control

The divider-control bits have three uses, as shown in Table 3. Three usable operating time bases may be selected (4.194304MHz, 1.048576MHz, or 32.768kHz). The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one second later. The divider-control bits are also used to facilitate testing the 146818.

Table 3 **Divider Configurations**

Time Base Frequency	Divider Bits Register A			Operation Mode	Divider Reset	Bypass First N-Divider Bits
	DV2	DV1	DV0			
4.194304MHz	0	0	0	Yes	–	N = 0
1.048576MHz	0	0	1	Yes	–	N = 2
32.768kHz	0	1	0	Yes	–	N = 7
Any	1	1	0	No	Yes	–
Any	1	1	1	No	Yes	–

Note: Other combinations of divider bits are used for test purposes only.

Square-Wave Output Selection

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in Figure 9. The first purpose of selecting a divider tap is to generate a square-wave output signal in the SQW pin. Four bits in Register A establish the square-wave frequency as listed in Table 4. The SQW frequency selection shares the 1-of-15 selector with periodic interrupts.

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave enable (SQWE) bit in Register B. Altering the divider, square-wave output selection bits, or the SQW output-enable bit may generate an asymetrical waveform at the time

of execution. The square-wave output pin has a number of potential uses. For example, it can serve as a frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control.

Periodic Interrupt Selection

The periodic interrupt allows the $\overline{IRQ}$ pin to be triggered from once every 500ms to once every 30.517 μs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Table 4 shows that the periodic interrupt rate is selected with the same Register A bits which select the square-wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit. Similarly the periodic interrupt is enabled by the PIE bit in Register B.

Periodic interrupt is usable by practically all real-time systems. It can be used to scan for all forms of input from contact closures to serial receive bits. It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function.

Table 4 **Periodic Interrupt Rate and Square Wave Output Frequency**

Rate Select Control Register 1				4.194304 or 1.048576MHz Time Base		32.768kHz Time Base	
				Periodic Interrupt Rate t_{PI}	SQW Output Frequency	Periodic Interrupt Rate t_{PI}	SQW Output Frequency
RS3	RS2	RS1	RS0				
0	0	0	0	None	None	None	None
0	0	0	1	30.517μs	32.768kHz	3.90625ms	256Hz
0	0	1	0	61.035μs	16.384kHz	7.8125ms	128Hz
0	0	1	1	122.070μs	8.192kHz	122.070μs	8.192kHz
0	1	0	0	244.141μs	4.096kHz	244.141μs	4.096kHz
0	1	0	1	488.281μs	2.048kHz	488.281μs	2.048kHz
0	1	1	0	976.562μs	1.024kHz	976.562μs	1.024kHz
0	1	1	1	1.953125ms	512Hz	1.953125ms	512Hz
1	0	0	0	3.90625ms	256Hz	3.90625ms	256Hz
1	0	0	1	7.8125ms	128Hz	7.8125ms	128Hz
1	0	1	0	15.625ms	64Hz	15.625ms	64Hz
1	0	1	1	31.25ms	32Hz	31.25ms	32Hz
1	1	0	0	62.5ms	16Hz	62.5ms	16Hz
1	1	0	1	62.5ms	8Hz	125ms	8Hz
1	1	1	0	250ms	4Hz	250ms	4Hz
1	1	1	1	500ms	2Hz	500ms	2Hz

Update Cycle

The 146818 executes an update cycle once-per-second, assuming one of the proper time bases is in place, the divider is not clear, and the SET bit in Register B is clear. The SET bit in the "1" state permits the program to initialize the time and calender bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 4.194304MHz or 1.048576MHz time base the update cycle takes 248 μs while a 32.768kHz time base update cycle takes 1984 μs. During the update cycle, the time, calendar, and alarm bytes are not accessible by the processor program. The 146818 protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update in progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating non-availability during update are usable by the program. In discussing the three methods it is assumed that at random points user programs are able to call a sub-routine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999ms are available to read valid time and data information. During this time a display could be updated or the information could be transferred to continuously available RAM. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update

cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes "1 , the update cycle begins 244 μs later. Therefore, if a "0" is read on the UIP bit, the user has at least 244 μs before the time/calendar data will be changed. If a "1" is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 μs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set "1" between the setting of the PF bit in Register C (see Figure 14) Periodic interrupts that occur at a rate of greater than t_{BUC} + t_{UC} allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within ($t_{PI} \div 2$) + t_{BUC} to insure that data is not read during the update cycle.

Power-down Considerations

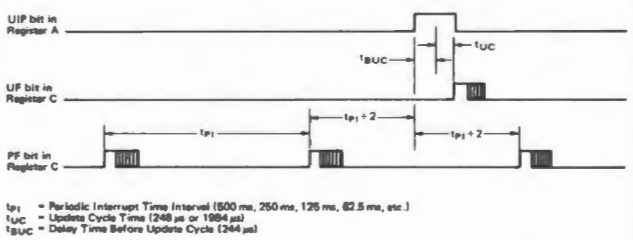
In most systems, the 146818 must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made. During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimise power consumption, and ensure hardware reliability.

The chip enable ($\overline{CE}$) pin controls all bus inputs ($R/\overline{W}$, DS, AS, $AD_0 \sim AD_7$). $\overline{CE}$, when negated, disallows any unintended modification of the RTC data by the bus. $\overline{CE}$ also reduces power consumption by reducing the number of transitions seen internally.

Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the square-wave (SQW) pin.

During and after the power source conversion, the V_{IN} maximum specification must never be exceeded. Failure to meet the V_{IN} maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part.

Figure 14 **Update-Ended and Periodic Interrupt Relationship**



SIGNAL DESCRIPTIONS

The block diagram in Figure 9, shows the pin connection with the major internal functions of the 146818 Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

V_{CC}, V_{SS}

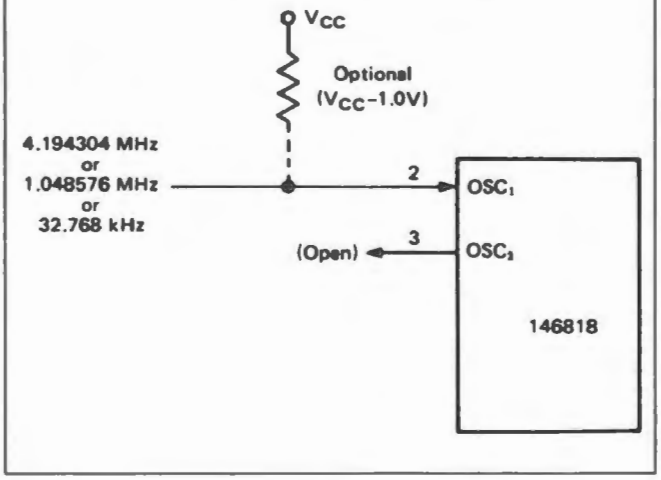
DC power is provided to the part on these two pins, V_{CC} being the most positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

OSC_1, OSC_2 – Time Base (Inputs)

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304MHz, 1.048576MHz, or 32.768kHz maybe connected to OSC_1 as shown in Figure 15. The time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant crystal at 4.194304MHz, 1.048576MHz or 32.768kHz frequencies. The crystal connections are shown in Figure 10.

Figure 15 **External Timebase Operation**



CKOUT – Clock Out (Output)

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 5.

CKFS – Clock Out Frequency Select (Input)

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. CKFS tied to V_{CC} causes CKOUT to be the same frequency as the time base at the OSC_1 pin. When CKFS is at V_{SS}, CKOUT is the OSC_1 time-base frequency divided by four. Table 5 summarizes the effect of CKFS.

Table 5 **Clock Output Frequencies**

Time Base (OSC_1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4.194304MHz	"High"	4.194304MHz
4.194304MHz	"Low"	1.048576MHz
1.048576MHz	"High"	1.048576MHz
1.048576MHz	"Low"	262.144kHz
32.768kHz	"High"	32.768kHz
32.768kHz	"Low"	8.192kHz

SQW – Square-Wave (Output)

The SQW pin can output a signal from one of 15 of the 22 internal-divider stages. The frequency and output enable of the SQW may be altered by programming Register A, as shown in Table 4. The SQW signal may be turned on and off using a bit in Register B.

$AD_0 \sim AD_7$ – Multiplexed Bidirectional Address/ Data Bus
Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the 146818 since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the 146818 latches the address from AD_0 to AD_5. Valid write data must be presented and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle, the 146818 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses, then ceases driving the bus (returns the output drivers to three-state) when DS falls in the 6800 case or $\overline{RD}$ rises in the other case.

AS – Multiplexed Address Strobe (Input)
A positive going multiplexed address strobe pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the address to be latched within the 146818. The bus control circuit in the 146818 also latches the state of the DS pin with the falling edge of AS or ALE.

DS – Data Strobe or Read (Input)
The DS pin has two interpretations via the bus control circuit. When emanating from 6800 family type processor, DS is a positive pulse during the latter portion of the bus cycle, and is called DS (data strobe), E (enable), and $\emptyset_2$ ($\emptyset_2$ clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data.

The second interpretation of DS is that of $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ emanating from the 8085 type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. The interpretation of DS is also the same as an output-enable signal on a typical memory.

The bus control circuit, within the 146818, latches the state of the DS pin on the falling edge of AS/ALE. In 6800 mode, DS must be "Low" during AS/ALE, which is the case with 6800 family multiplexed bus processors. To insure the 8085 mode of this circuit the DS pin must remain "High" during the time AS/ALE is "High".

R/$\overline{W}$ – Read/Write (Input)
The bus control circuit treats the R/$\overline{W}$ pin in one of two ways. When a 6800 family type processor is connected, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with "High" level on R/$\overline{W}$ while DS is "High", whereas a write cycle is a "Low" on R/$\overline{W}$ during DS.

The second interpretation of R/$\overline{W}$ is as a negative write pulse, $\overline{WR}$, $\overline{MEMW}$, and $\overline{I/OW}$ from 8085 type processors. This circuit in this mode gives R/$\overline{W}$ pin the same meaning as the write ($\overline{W}$) pulse on many generic RAMs.

$\overline{CE}$ – Chip Enable (Input)
The chip-enable ($\overline{CE}$) signal must be asserted ("Low") for a bus cycle in which the 146818 is to be accessed. $\overline{CE}$ is not latched and must be stable during DS and AS (in the 6800 case) and during $\overline{RD}$ and $\overline{WR}$ (in the 8085 Case). Bus cycles which take place without asserting $\overline{CE}$ cause no actions to take place within the 146818. When $\overline{CE}$ is "High", the multiplexed bus output is in a high-impedance state.

When $\overline{CE}$ is "High", all address, data, DS, and R/$\overline{W}$ inputs from the processor are disconnected within the 146818.

This permits the 146818 to be isolated from a powered-down processor. When $\overline{CE}$ is held "High", an unpowered device cannot receive power through the input pins from the real-time clock power source. Battery power consumption can thus be reduced by using a pull-up resistor or active clamp on $\overline{CE}$ when the main power is off.

$\overline{IRQ}$ – Interrupt Request (Output)
The $\overline{IRQ}$ pin is an active "Low" output of the 146818 that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains "Low" as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the processor program normally reads Register C. The $\overline{RES}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance state. Multiple interrupting devices may thus be connected to an $\overline{IRQ}$ bus with one pull-up at the processor.

$\overline{RES}$ – Reset (Input)
The $\overline{RES}$ pin does not affect the clock, calendar, or RAM functions. On powerup, the $\overline{RES}$ pin must be held "Low" for the specified time, t_{RLH}, in order to allow the power supply to stabilize. Figure 16 shows a typical representation of the $\overline{RES}$ pin circuit.

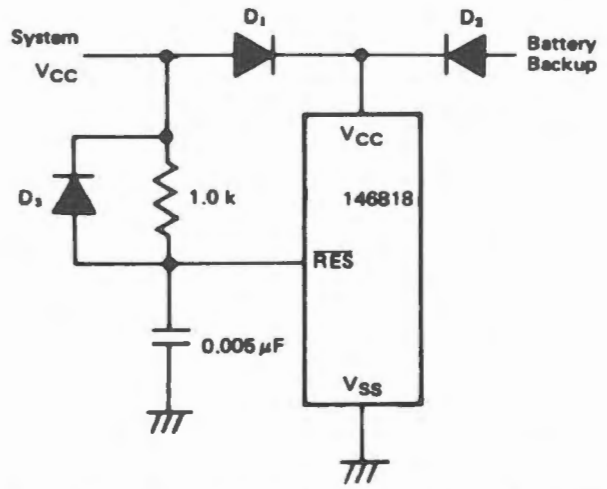
When $\overline{RES}$ is "Low" the following occurs:

a. Periodic Interrupt Enable (PIE) bit is cleared to "0".
b. Alarm Interrupt Enable (AIE) bit is cleared to "0".
c. Update ended interrupt Enable (UIE) bit is cleared to "0".
d. Update ended Interrupt Flag (UF) bit is cleared to "0".
e. Interrupt Request status Flag (IRQF) bit is cleared to "0".
f. Periodic Interrupt Flag (PF) bit is cleared to "0".
g. Alarm Interrupt Flag (AF) bit is cleared to "0".
h. $\overline{IRQ}$ pin is in high-impedance state, and
i. Square-Wave output Enable (SQWE) bit is cleared to "0".

● PS – Power Sense (Input)
The power-sense pin is used in the control of the valid RAM and time (VRT) bit in Register C. When the PS pin is "Low" the VRT bit is cleared to "0".

During powerup, the PS pin must be externally held "Low" for the specified time, t_{PLH}. As power is applied the VRT bit remains "Low" indicating that the contents of the RAM, time registers, and calendar are not guaranteed. When normal operation commences PS should be permitted to go "High". Figure 17 shows a typical circuit connection for the power-sense pin.

Figure 16 **Typical Powerup Delay Circuit for RES**



Note: If the Real time clock is isolated from the MPU power supply by a diode drop (D_1), care must be taken to meet V_{IN} requirements.

REGISTERS

The 146818 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

Register A ($0A)

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0	
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	Read/Write Register except UIP

UIP – The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 µs (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero – it is not in transition. The UIP bit is a read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibit any update cycle and then clear the UIP status bit.

Table 6 **Update Cycle Times**

UIP Bit	Time Base (OSC_1)	Update Cycle Time (t_{UC})	Minimum Time Before Update Cycle (t_{BUC})
1	4.194304MHz	248µs	–
1	1.048576MHz	248µs	–
1	32.768kHz	1984µs	–
0	4.194304MHz	–	244µs
0	1.048576MHz	–	244µs
0	32.768kHz	–	244µs

DV2, DV1, DV0 – Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 3 shows that time bases of 4.194304MHz, 1.048576MHz, and 32.768kHz may be used. The divider selection bits are also used to reset the divider chain. When the time-calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed the first update cycle begins one second later. These three read/write bits are never modified by the RTC and are not affected by $\overline{RES}$.

RS3, RS2, RS1, RS0 – The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate an output square-wave (SQW pin) and/or a periodic interrupt. The program may do one of the following: 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 4 lists the periodic interrupt rates and the square-wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by $\overline{RES}$ and are never changed by the RTC.

Register B ($0B)

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0	
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE	Read/Write Register

SET – When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by $\overline{RES}$ or internal functions of the 146818.

PIE – The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit to cause the $\overline{IRQ}$ pin to be driven "Low". A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Control Register A. A "0" in PIE blocks $\overline{IRQ}$ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still at the periodic rate. PIE is not modified by any internal 146818 functions, but is cleared to "0" by a $\overline{RES}$.

AIE – The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an $\overline{IRQ}$ signal. The $\overline{RES}$ pin clears AIE to "0". The internal functions do not affect the AIE bit.

UIE – The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flag (UF) bit to assert $\overline{IRQ}$. The $\overline{RES}$ pin going "Low" or the SET bit going "1" clears the UIE bit.

SQWE – When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a "0" the SQW pin is held "Low". The state of SQWE is cleared by the $\overline{RES}$ pin. SQWE is a read/write bit.

DM – The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or $\overline{RES}$. A "1" in DM signifies binary data, while a "0" in DM specified binary-coded-decimal (BCD) data.

24/12 – The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by the software.

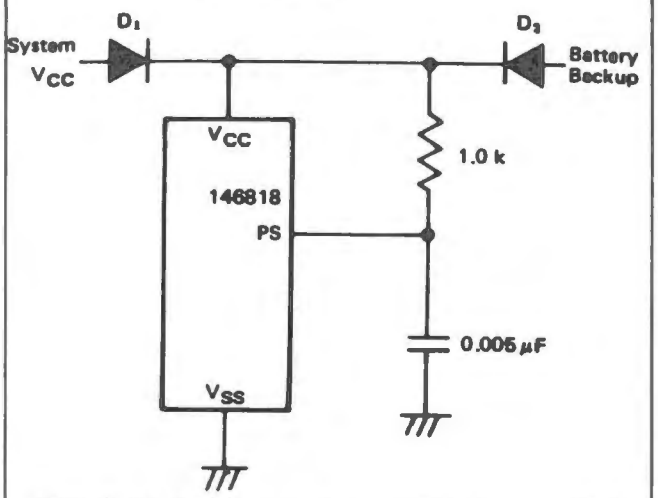
Register C ($0C)

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

Read-Only Register

Figure 17 **Typical Powerup Delay Circuit for Power Sense**



Note: If the Real time clock is isolated from the MPU power supply by a diode drop (D_1), care must be taken to meet V_{IN} requirements.

IRQF – The interrupt request flag (IRQF) is set to a "1" when one or more of the following is true:

PF = PIE = "1"
AF = AIE = "1"
UF = UIE = "1"

i.e., IRQF = PF·PIE + AF·AIE + UF·UIE

Any time the IRQF bit is a "1", the $\overline{IRQ}$ pin is driven "Low". All flag bits are cleared after Register C is read by the program or when the $\overline{RES}$ pin is low. A program write to Register C does not modify any of the flag bits.

PF – The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a paticular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an $\overline{IRQ}$ signal and the IRQF bit when PIE is also a "1". The PF bit is cleared by a RES or a software read of Register C.

AF – A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the $\overline{IRQ}$ pin to go "Low", and a "1" to appear in the IRQF bit, when the AIE bit also is a "1". A $\overline{RES}$ or a read of Register C clears AF.

UF – The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting $\overline{IRQ}$. UF is cleared by a Register C read or a $\overline{RES}$.

b3 to b0 – The unused bits of Status Register C are read as "0s". They can not be written.

Register D ($0D)

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

Read Only Register

VRT – The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is "Low". The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read/only bit which is not modified by the $\overline{RES}$ pin. The VRT bit can only be set by reading the Register D.

b6 to b0 – The remaining bits of Register D are unused. They cannot be written, but are always read as "0s".

RS data

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An Electrocomponents Group Company

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RS data

Miniature dot matrix impact printer system

Stock numbers 301-959, 301-965, 301-971

The RS miniature dot matrix impact printer system consists of a printer unit, control ic and associated pcb. The printer is a dot matrix impact type using plain 57.5mm wide paper and produces a good quality permanent ink printout. Up to 24 columns of 5 x 8 characters can be produced, larger format characters may also be printed. The custom mask programmed control ic is designed specifically for use with the printer mechanism and produces all the signals for the Darlington transistors to drive the printer. Serial or 7-bit parallel ASCII data is accepted by the i.c., a choice of 110, 300, 1200 or 2400 baud is provided and a busy output allows for handshake operation. Upper and lower case characters are printed, lower case being with one dot line descenders to improve the print quality. Control input characters allow operation in various graphics modes including larger formats and inverted printing.

Features

- Compact 24-column mechanism
- High contrast permanent printout
- Dot matrix format allows graphics printing
- Easily replaceable ink ribbon cassette
- Custom control ic with full upper and lower case ASCII character set
- Lower case characters printed with one line descenders where required.

Absolute maximum ratings

Printer Controller PC160-1

Supply voltage	7V
Voltage on any pin with respect to ground	–0.5V to +7V
Power dissipation	1.5W
Operating temperature	0°C to +70C
Storage temperature	–65°C to +150°C

Printer characteristics

Mechanical

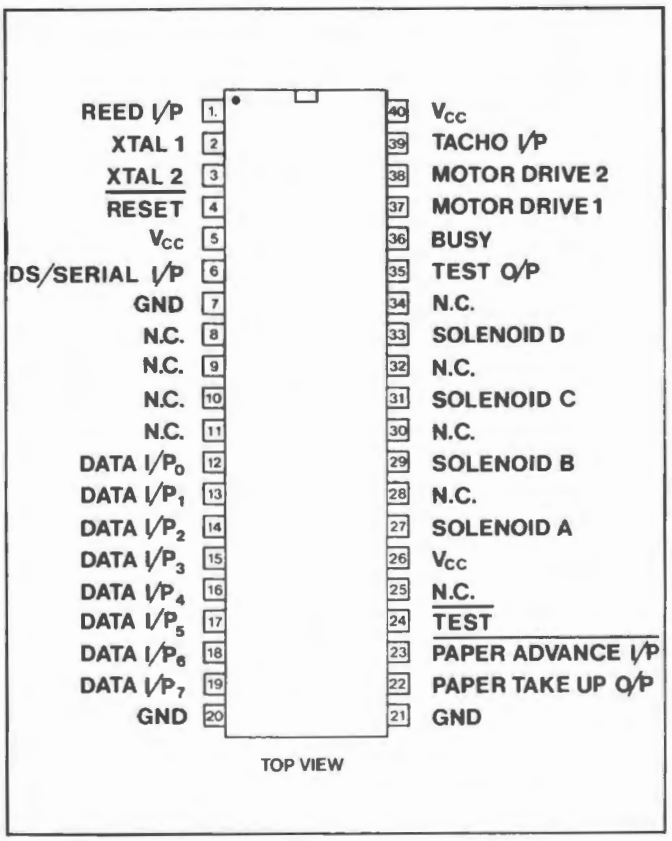
Printing system	Mechanical dot printer (4 print solenoids)

Print format

Maximum number of dots per line	144
Print column capacity	24 columns max (5 x 7 dot matrix character format)
Printing speed one dot line	≈150 ms (continuous printing)
5 x 7 dot matrix	≈0.7 lines/sec. (continuous printing with 3 dot line spacing)

Character formation

Dot spacing	0.33 mm horizontal 0.33 mm vertical
5 x 7 dot – matrix	1.7 mm (width) x 2.4 mm (height)
5 x 8 dot – matrix	1.7 mm (width) x 2.7 mm (height)



TOP VIEW

Paper feeding

The paper is automatically fed dot-line by dot-line in conjunction with the ink ribbon.

Inking

Ribbon cassette with continuous ribbon feeding performed automatically during motor operation.

Service life ≈10,000 lines of print

Paper

Width 57.5 +0.5 mm

Outside diameter of roll 50 mm max.

Thickness 0.07 mm

Printer

Connections PCB solder pads on 2.54 mm pitch

Overall dimensions ≈94 x 42.6 x 12.8 mm

Ribbon cassette dimensions ≈91 x 25 x 7 mm

Reliability (MCBF) 500,000 lines

Operating temperature range 0°C to +50°C

Printer controller pc 160-1

Electrical characteristics

(T_A = 0°C to +70°C. V_{CC} = 4.5 to 5.5V)

Parameter		Conditions	Min	Typ	Max	Units
Supply voltage			4.5	5	5.5	V
Supply current				5	10	mA
Output low voltage	V_{OL}	I_{OL} = 1.6mA			0.45	V
Output high voltage	V_{OH}	I_{OH} = 40μA	2.4			V
Input low voltage	V_{IL}		0		0.8	V
Input high voltage	V_{IH}		2.0		V_{CC}	V
Operating frequency				6.0		MHz

Operating information

The 160-1 controller is a single-chip microcomputer, provided with internal firmware for date interface and mechanism control. A variety of special functions have been provided, selected by the user by sending appropriate control codes.

The following remarks apply to both serial and parallel data modes, unless otherwise specified. Data should be formatted for a 24-character line.

Character set and control codes

The character set is a full ASCII character set (hex) codes 20 to 7F inclusive. A £ sign is provided at code 23. Codes above 7F are invalid. Control codes from 00 to 1F are ignored, with the following exceptions.

(Hex)		
OA	(LF)	initiates print cycle in chosen mode and line feed.
OD	(CR)	exactly as OA. Note that a data stream terminated by CRLF will cause printing plus an extra line feed.
1B	(ESC)	escape sequence: next character defines action taken (see below)

After an escape code, the next character is interpreted as follows:

Codes 00 to 0F determine print mode, in accordance with bit patterns shown:

Bit 0	(lsb)	0 for text mode, 1 for data mode (inverted)
Bit 1		0 for character mode, 1 for graphics mode
Bit 2		0 for single width, 1 for double width
Bit 3		0 for single height, 1 for double height

All sixteen mode combinations are acceptable. Mode zero is assumed at power up or after a software reset, which is also the ESC,00 sequence.

Other codes received after ESC are ignored, and the escape sequence is terminated, with the exception of the escape code itself; the sequence ESC, ESC will initiate the self-test mode, where the character set is printed in all eight character modes, and a graphics pattern is generated.

Printing will be initiated automatically when a full line of data has been received (i.e. 24 characters or graphics codes, or 12 in double width mode).

Character printing

Characters are formed from a 5-wide by 8-high dot matrix, with one dot space between columns. The matrix is doubled in the appropriate dimension by mode control codes. Text mode prints left to right, like a typewriter; data mode prints inverted, and right to left, for panel-mounting applications. The 8th dot row is used for descenders.

Graphics printing

Graphics codes are received as 6-bit groups; input data is assumed to be graphics information following receipt of an ESC, followed by bit 1 set to 1. 24 (12 in double width mode) characters must be received, following which the dot line is printed, and graphics mode automatically cleared. It is therefore essential to transmit an ESC, sequence before every dot line.

The graphics pattern is built up as a succession of horizontal dot lines, each of 144 dots. They may be thought of as 24 x 6-bit codes, with the most significant bit of each code being printed first. Only the least significant six bits of data will be printed, so input codes must be in the range 00 to 3F: codes from 40 to 7F will be treated as 00 to 3F. The mechanism will stop after each dot line to receive more data. 1 is "dot on", 0 is "dot off".

All eight graphics modes are feasible, and may be used to economise on data coding if only a coarse pattern is required. Printing large areas of solid dot patterns is NOT recommended as it may lead to overheating or premature wear. If the graphics mode is to be used extensively, the power supply rating should be studied carefully, as the supply voltage must never be allowed to fall below 4.5V or improper operation and consequential damage may result.

Notes:

1. Data strobe input must be taken low when busy is low and input data are on Data I/P O-7, and held low until busy goes high, acknowledging that data has been read in. In serial mode, DS (Pin 6) is serial data input, positive true, TTL compatible.
2. Reset may be taken low via a 100 ohm resistor to initialise the microprocessor after power-up or to clear a fault condition.

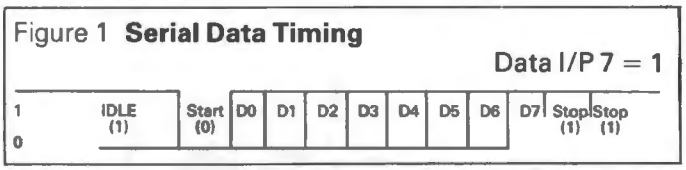
3. +5V supply (tolerance ±10%) must be capable of 1A continuous and 3A peak demand to ensure orderly initialisation. Typical current consumption is 80 mA quiescent and 400 mA printing.
4. Busy output (NB: max 1 TTL load from the control i.c. On the p.c.b. this signal is buffered and will drive 20 LSTTL loads) is high when busy (or reset), low when ready to accept data. Incoming data during busy period will be ignored.
5. Data inputs are 0 (least significant) to 7 (most significant), and have additional functions: D7 must be held low for parallel data input, and held high for serial data input. Data I/P 6 & Data I/P 5 select baud rates in serial mode as follows:

Data I/P 6 (J2)	0 (A)	0 (A)	1 (B)	1 (B)
Data I/P 5 (J3)	0 (A)	1 (B)	0 (A)	1 (A)
Baud Rate	110	300	1200	2400

All data input lines MUST be terminated high or low in ALL modes.

See timing diagrams figures 1 and 2 for more information.

Figure 1 **Serial Data Timing**

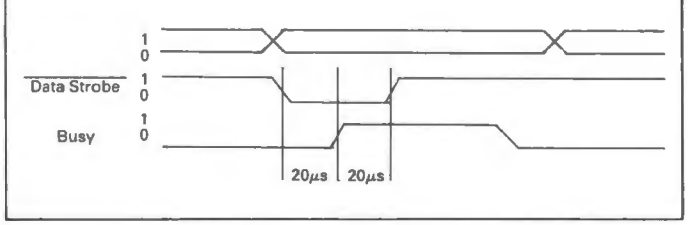


One start bit (always a zero), 8 data bits (D7 ignored). Two or more stop bits (ones).

Baud rates	110	300	1200	2400	Baud
Bit times	9091	3333	833	417	μS

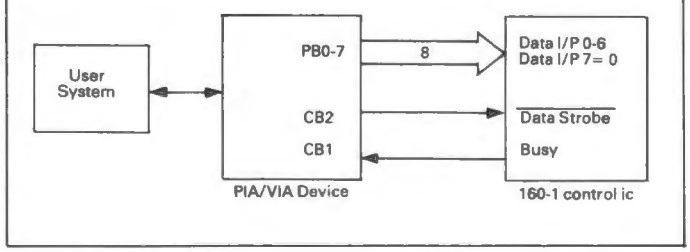
The busy line will go true momentarily after each serial character is received, and will stay true during a print cycle. Data must not be sent during the busy time period.
Baud rate selection is by Data I/P6 & Data I/P5 (see note 5).

Figure 2 **Parallel Data Timing**



Data Inputs are sampled when $\overline{DS}$ is low, and must be held steady until busy goes high. $\overline{DS}$ must be removed immediately to prevent multiple inputs.

Figure 3 **Typical PIA/VIA interface**



Paper loading

Only the correct size and grade of paper should be used. Before loading the paper into the printer cut the edge squarely. Insert into the paper inlet on the printer side and push whilst operating the printer paper feed.

Removal of paper

To remove the paper, feed it out of the printer using the electrical paper feed. Alternatively it may be pulled out by hand but care must be taken to pull it straight out and not obliquely as jamming may occur.

Replacement of the ink ribbon cassette

Once the ink ribbon has reached the end of its useful life after approximately two rolls of printing it should be replaced. The ink ribbon cassette is of the throwaway type and re-inking should not be attempted.
Changing should only be performed when the paper has been removed from the printer and should be carried out in the following manner:
To remove the old cassette push down on the end marked push until the other end of the cassette disengages, then remove the whole ink ribbon assembly.
To replace the cassette first turn button on the cassette in the direction shown until the ribbon becomes taut, place the cassette straight onto the printer, turning the button during this operation facilitates correct engagement.
Finally ensure that the ink ribbon is running freely through the slot in the printer.

Table 1 **ASCII Codes used**

*ASCII CONTROL CODES

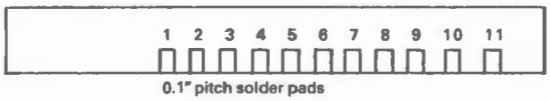
	CONTROL	BINARY CODE	HEXADECIMAL CODE
LF	Line feed	000 1010	0A
CR	Carriage return	000 1101	0D
ESC	Escape	001 1011	1B

*ASCII CHARACTER CODE

Character	Binary Code	Hexadecimal Code	Character	Binary Code	Hexadecimal Code
Space	010 0000	20	P	101 0000	50
!	010 0001	21	Q	101 0001	51
"(dble.quote)	010 0010	22	R	101 0010	52
£	010 0011	23	S	101 0011	53
$	010 0100	24	T	101 0100	54
%	010 0101	25	U	101 0101	55
&	010 0110	26	V	101 0110	56
'(sgl. quote)	010 0111	27	W	101 0111	57
(	010 1000	28	X	101 1000	58
)	010 1001	29	Y	101 1001	59
*(asterisk)	010 1010	2A	Z	101 1010	5A
+	010 1011	2B	[	101 1011	5B
,(comma)	010 1100	2C	\	101 1100	5C
-(minus)	010 1101	2D	]	101 1101	5D
.(period)	010 1110	2E	^	101 1110	5E
/	010 1111	2F	–(underline)	101 1111	5F
0	011 0000	30	`	110 0000	60
1	011 0001	31	a	110 0001	61
2	011 0010	32	b	110 0010	62
3	011 0011	33	c	110 0011	63
4	011 0100	34	d	110 0100	64
5	011 0101	35	e	110 0101	65
6	011 0110	36	f	110 0110	66
7	011 0111	37	g	110 0111	67
8	011 1000	38	h	110 1000	68
9	011 1001	39	i	110 1001	69
:	011 1010	3A	j	110 1010	6A
;	011 1011	3B	k	110 1011	6B
<	011 1100	3C	l	110 1100	6C
=	011 1101	3D	m	110 1101	6D
>	011 1110	3E	n	110 1110	6E
?	011 1111	3F	o	110 1111	6F
@	100 0000	40	p	111 0000	70
A	100 0001	41	q	111 0001	71
B	100 0010	42	r	111 0010	72
C	100 0011	43	s	111 0011	73
D	100 0100	44	t	111 0100	74
E	100 0101	45	u	111 0101	75
F	100 0110	46	v	111 0110	76
G	100 0111	47	w	111 0111	77
H	100 1000	48	x	111 1000	78
I	100 1001	49	y	111 1001	79
J	100 1010	4A	z	111 1010	7A
K	100 1011	4B	{	111 1011	7B
L	100 1100	4C	¦	111 1100	7C
M	100 1101	4D	}	111 1101	7D
N	100 1110	4E	~	111 1110	7E
O	100 1111	4F	■	111 1111	7F

*American Standards Institute Publication X3 4-1968

Figure 4 **Printer Connections**



Pad	
1	Reed switch
2	Reed common
3	Motor –
4	Motor +
5	Solenoid common
6	Solenoid D
7	Solenoid C
8	Solenoid B
9	Solenoid A
10	Tacho common
11	Tacho

Figure 5 **Printer Power Supply**

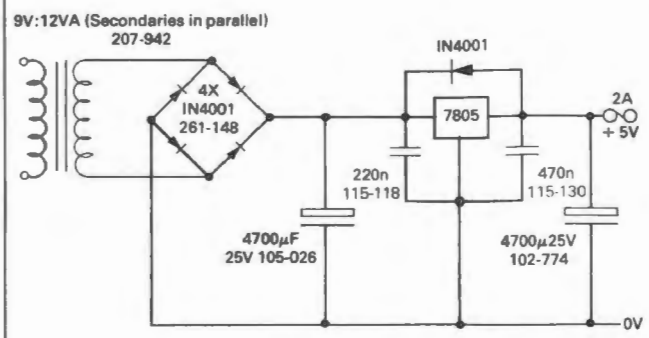
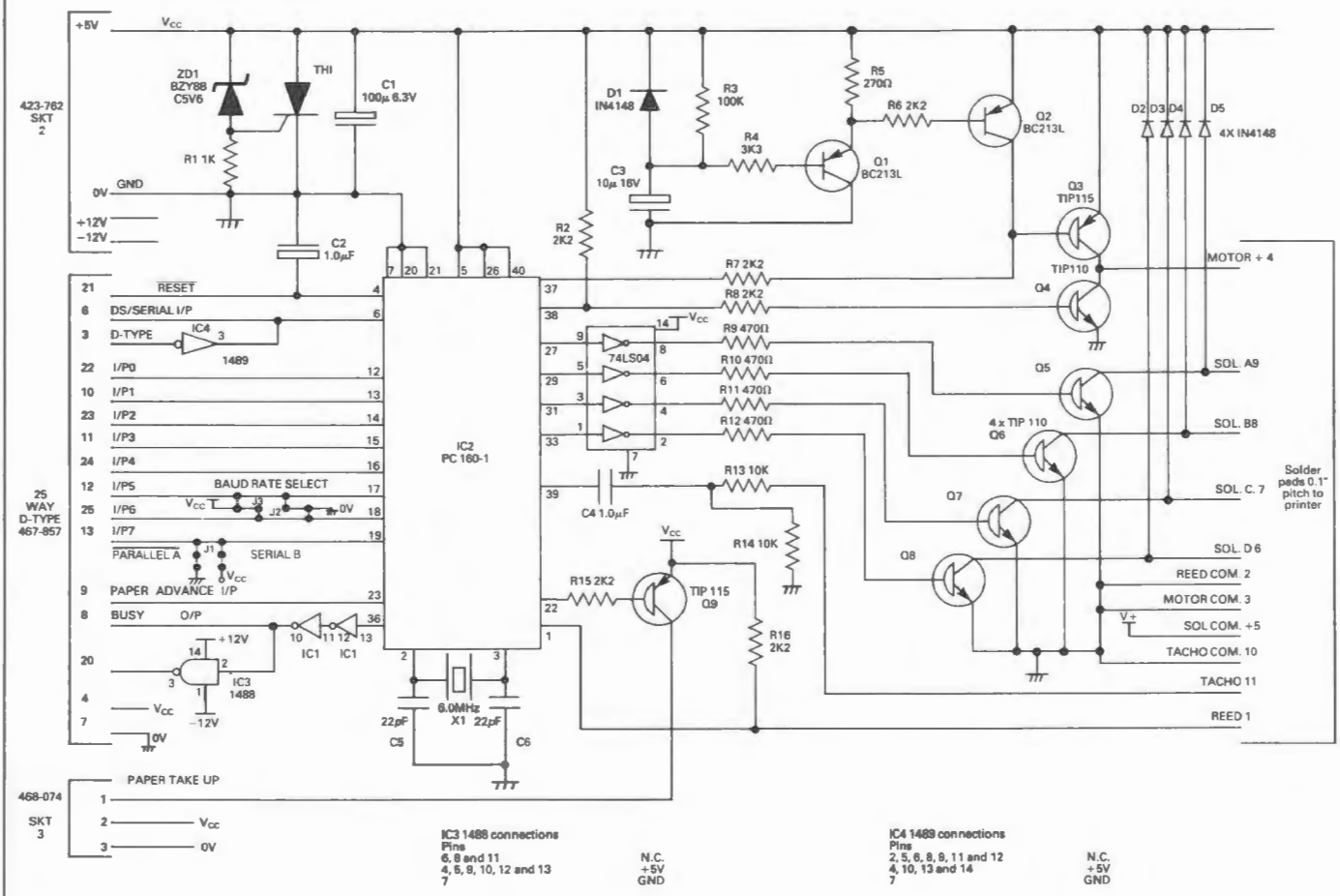


Figure 6 **Circuit diagram**



Component List Printer Controller

R1	1K	
R2	2K2	
R3	100K	
R4	3K3	
R5	270Ω	0.4W metal
R6	2K2	film
R7	2K2	0.25W high stability
R8	2K2	carbon film
R9	470Ω	(0.5W thick film)
R10	470Ω	(metal glaze)
R11	470Ω	
R12	470Ω	
R13	10K	
R14	10K	
R15	2K2	
R16	2K2	

IC1	74LS04	307-503
IC2	PC160-1	301-965
IC3	1488	309-587
IC4	1489	309-593

Q1	BC213L	294-974
Q2	BC213L	294-974
Q3	TIP 115	295-012
Q4	TIP 110	295-006
Q5	TIP 110	295-006
Q6	TIP 110	295-006
Q7	TIP 110	295-006
Q8	TIP 110	295-006
Q9	TIP 115	295-012

C1	100μ6.3V	102-730
C2	1.0μ 35V	101-771
C3	10μ 16V	103-957
C4	1.0μ 100V	114-430
C5	22pF 100V	125-828
C6	22pF 100V	125-828

D1	IN4148	271-606
D2	IN4148	271-606
D3	IN4148	271-606
D4	IN4148	271-606
D5	IN4148	271-606
ZD1	BZY885V6	282-094
TH1		*
X1	6.0 MHz crystal	302-198

Print controller pcb	435-147
Fuse 2A Quick blow type	

SKT1	25 way D type	467-857
SKT2		423-762
SKT3		468-074
J1		334-555
J2		334-555
J3		334-555

IC Sockets

1X	40-pin DIL
3X	14-pin DIL

* Small signal thyristor, C106 can be used if the leads are deformed.

Printer Electrical Specification

Motor:
- Terminal voltage ____ 4.5 (+0.5 –0.7)V
- Mean current ____ ≈0.2A (at 4.5V 25°C)

Print solenoid:
- Terminal voltage ____ 4.0 (+0.5 –1.0)V
- Ohmic resistor ____ 1.5Ω ±0.15Ω (at 25°C)

Timing detector ____ Tachometer directly coupled to the motor

Reset detector ____ Reed switch

Table 2 PCB Data Input/Output

D connector socket

Pin	Serial Mode	Parallel Mode
1	NC	NC
2	NC	NC
3	Serial data in	NC
4	Request to send (+5V)	NC
5	NC	$\overline{\text{NC}}$
6	NC	$\overline{\text{Data strobe}}$
7	Ground	Ground
8	NC	$\overline{\text{Busy}}$
9	NC Note 2	$\overline{\text{Paper advance}}$
10	OV Note 1	D1
11	OV Note 1	D3
12	NC	D5
13	NC	D7 Note 3
14	NC	NC
15	NC	NC
16	NC	NC
17	NC	NC
18	NC	NC
19	NC	NC
20	Date terminal ready	$\overline{\text{NC}}$
21	NC Note 2	$\overline{\text{Reset}}$
22	OV Note 1	D0
23	OV Note 1	D2
24	OV Note 1	D4
25	NC	D6

Notes:
1. These lines must be tied to 0V off board.
2. May be connected by user to give parallel function for these pins.
3. Not normally specified. Selection by on board link J1.

RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
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Telephone: 0536 201234
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RS data

Shaded pole motors

A pair of shaded pole motors, available in either clockwise (334-202) or counter clockwise (334-218) versions which are ideally suited to small loads such as fans, water stirrers etc.

The motors are of a self-starting asynchronous type with impedance protection and no r.f. interference. The bearings are self-aligning, sintered bronze impregnated with synthetic oil. The two pole windings are varnish impregnated to Class 'E' (BS5000 pt 2).

Absolute maximum ratings

Storage temperature range

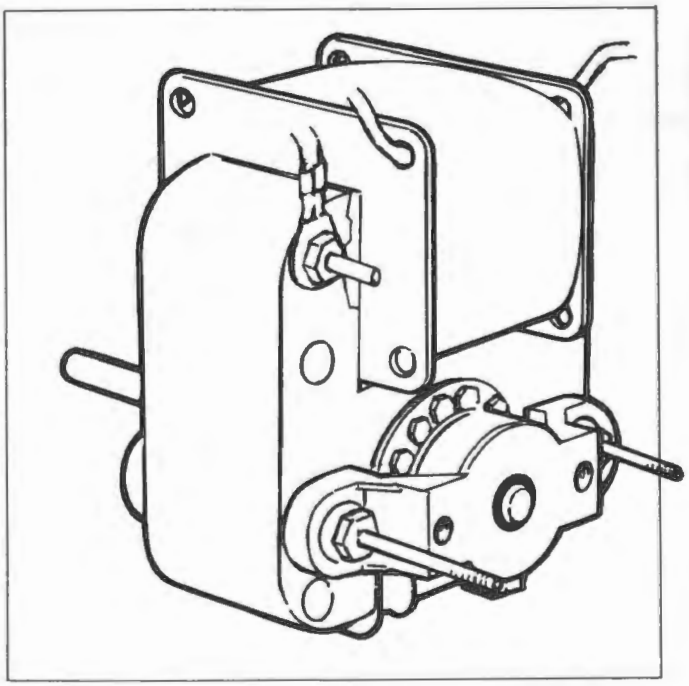
Max. bearing operating temperature ——— + 80°C

Max. coil operating temperature ——— +120°C

Max. supply voltage ——— +260V a.c.

Features

- Non-reversing, self-starting
- Clockwise or counter-clockwise versions available
- Class 'E' insulation
- r.f. interference free
- Sintered bronze bearings
- Continuous or intermittent duty.



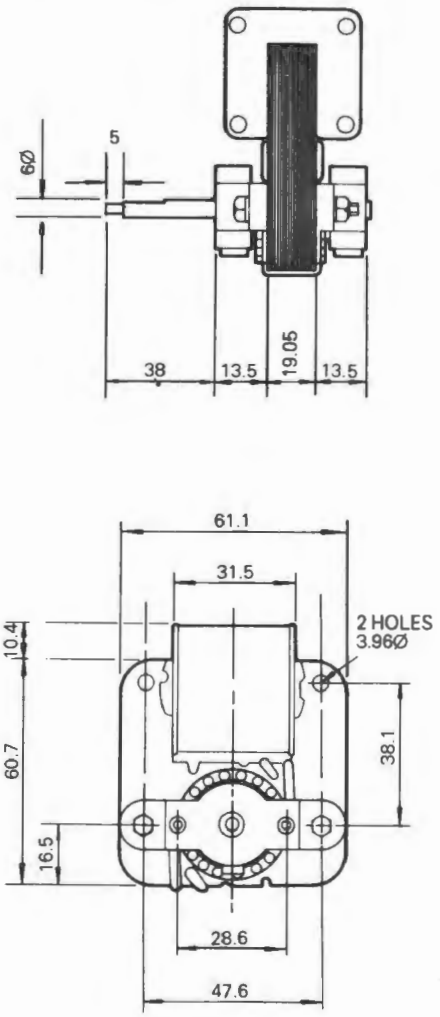
Performance figures

Parameter	Typ.	Unit
Mechanical rating*	160	g/cm
	4.2	Watts
Self-cooled rating*	240	g/cm
	6.3	Watts
Fan rating*	280	g/cm
	7.4	Watts
Voltage range	220/260	V
Frequency range	50/60	Hz
Input power	23	W
Input current (loaded)	180	mA
Starting torque	75	g/cm
No load speed	2750	rpm
Speed loaded	2400	rpm

* At 2550rpm 50Hz supply.

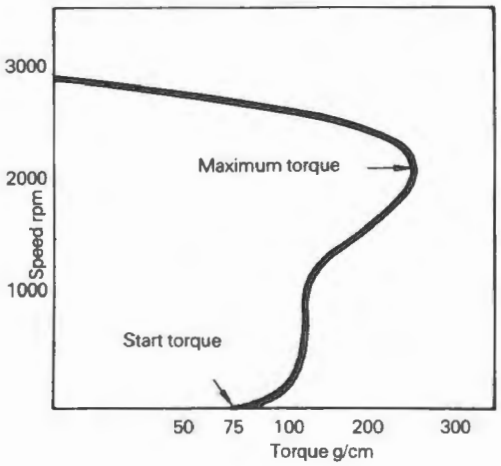
RS data

Figure 1 **Dimension details**



A shaded pole motor is a single phase induction motor that has one or more auxiliary short-circuited windings acting on only a portion of the magnetic circuit. The winding is a closed copper ring imbedded in the face of the pole. The shaded pole provides the required rotating field for starting purposes.

Figure 2 **Typical performance**



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An Electrocomponents Group Company
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RS data

Type T thermocouples and accessories

General specification for Copper/ Copper-nickel Thermocouples

(Copper-nickel is also known as constantan)

Wire identification (to BS1843: 1952)
White sleeve (positive): Copper
Blue sleeve (negative): Copper-nickel
Blue: Outer sleeve
Blue: Connector body

Tolerance (to BS1041 pt 5)

Welded tip thermocouple
−200°C to 0°C *
0°C to 100°C ± 1°C
100°C to 400°C ± 1%

Hypodermic probe
−100°C to 0°C *
0°C to 93°C ± 0.4%
93°C to 250°C ± 0.37%

* BS1041 pt 4 does not specify tolerances for temperatures less than 0°C.

Sensitivity

	−100°C	0°C	100°C	400°C
Approximate e.m.f. (mV)	−3·38	0	4·28	20·87
Sensitivity (μV/degC)	28	38	46	61

Resists oxidizing and reducing atmospheres up to 350°C. Subject to alteration of calibration above 400°C due to oxidation of copper. Requires protection from acid fumes.

Thermocouple – 151-259

Features

- Thermocouple junction welded in Argon, resists oxidation
- 400°C maximum working temperature
- Small welded junction minimises thermal heat sinking and provides fast thermal response
- Glass fibre insulation.

Specifications

Dimensions
Thermocouple wire — 1/0.315mm
Overall length — 1.1mm
Insulation diameter — 1.1 x 1.7mm

Materials
Thermocouple wire — Copper/Copper-nickel
Insulation — Glass fibre
Working temperature range
−200°C to +400°C

Temperatures below 0°C to be calibrated as required. For measurements below 0°C British Standards recommend a calibration at the boiling point of Oxygen (−183°C at S.T.P.).

Voltage reference complies with BS4937; Part 0; March 1973. Materials comply with BS1041: Part 4; 1966.

Hypodermic thermocouple probe 151-271

Features

- Stainless steel sheath
- Thermocouple not electrically insulated from the sheath
- 200°C maximum working temperature.

Specification

Dimensions:
Thermocouple wire — 7/0.2mm
Sheath length — 100mm
Handle length — 40mm
Lead length — 1.5mm

Materials: Thermocouple wire
Copper/Copper-nickel
Sheath — Stainless steel
Load wire insulation — P.T.F.E.
Probe temperature range −100°C to + 250°C

Panel mounting digital temperature indicator 258-186

Features

- Suitable for types K, T and J thermocouples
- Automatic cold junction compensation
- 1°C resolution
- 11.2mm 3½ digit L.E.D. display

Specifications

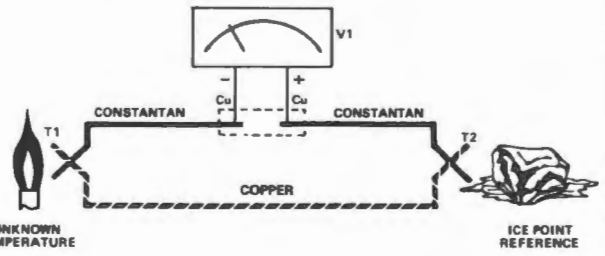
Supply voltage — 115V a.c. or 240V a.c. or 8-15V a.c. or 8-15V d.c.
Ambient temperature range — 0 to +50°C
Input sensor — Internally switchable K, T or J
Temperature range — Type K −50°C to +1000°C
Type T −100°C to +325°C
Type J −25°C to +625°C
Resolution — 1°C
Accuracy at 25°C — 0.3%
Note: this does not include sensor errors
Input impedance — 30MΩ typical
Display type — 11.2mm 7-segment L.E.D.

Thermocouple basics

Thermocouples are economical and rugged; they have reasonably good long-term stability. Because of their small size, they respond quickly and are good choices where fast response is important. They function over temperature ranges from cryogenics to jet-engine exhaust and have reasonable linearity and accuracy.

Because the number of free electrons in a piece of metal depends on both temperature and composition of the metal, two pieces of dissimilar metal in isothermal contact will exhibit a potential difference that is a repeatable function of temperature, as shown in Figure 1. The resulting voltage depends on the temperatures, T1 and T2, in a repeatable way.

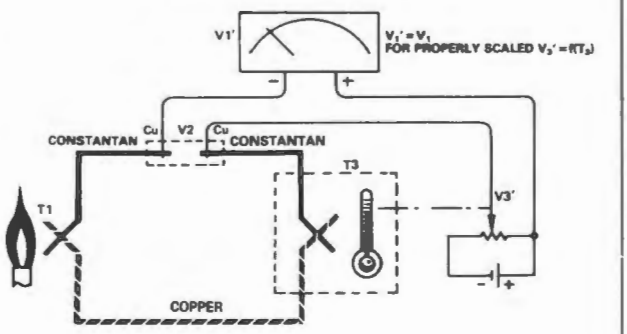
Figure 1 **Thermocouple voltage with 0°C reference**



Since the thermocouple is basically a differential rather than absolute measuring device, a known reference temperature is required for one of the junctions if the temperature of the other is to be inferred from the output voltage. Thermocouples made of specially selected materials have been exhaustively characterized in terms of voltage versus temperature compared to primary temperature standards. Most notably the water-ice point of 0°C is used for tables of standard thermocouple performance.

An alternative measurement technique, illustrated in Figure 2, is used in most practical applications where accuracy requirements do not warrant maintenance of primary standards. The reference junction temperature is allowed to change with the environment of the measurement system, but it is carefully measured by some type of absolute thermometer. A measurement of the thermocouple voltage combined with a knowledge of the reference temperature can be used to calculate the measurement junction temperature. Usual practice, however, is to use a convenient thermoelectric method to measure the reference temperature and to arrange its output voltage so that it corresponds to a thermocouple referred to 0°C. This voltage is simply added to the thermocouple voltage and the sum then corresponds to the standard voltage tabulated for an ice-point referenced thermocouple.

Figure 2 **Substitution of measured reference temperature for ice point reference**



Type T thermocouple reference table

(with reference junctions at 0°C).

Deg. C.	0	1	2	3	4	5	6	7	8	9
					THERMOELECTRIC VOLTAGE IN ABSOLUTE MILLIVOLTS					
−270	−6.258									
−260	−6.232	−6.236	−6.239	−6.242	−6.245	−6.248	−6.251	−6.253	−6.255	−6.256
−250	−6.181	−6.187	−6.193	−6.198	−6.204	−6.209	−6.214	−6.219	−6.224	−6.228
−240	−6.105	−6.114	−6.122	−6.130	−6.138	−6.146	−6.153	−6.160	−6.167	−6.174
−230	−6.007	−6.018	−6.028	−6.039	−6.049	−6.059	−6.068	−6.078	−6.087	−6.096
−220	−5.889	−5.901	−5.914	−5.926	−5.938	−5.950	−5.962	−5.973	−5.985	−5.996
−210	−5.753	−5.767	−5.782	−5.795	−5.809	−5.823	−5.836	−5.850	−5.863	−5.876
−200	−5.603	−5.619	−5.634	−5.650	−5.665	−5.680	−5.695	−5.710	−5.724	−5.739
−190	−5.439	−5.456	−5.473	−5.489	−5.506	−5.522	−5.539	−5.555	−5.571	−5.587
−180	−5.261	−5.279	−5.297	−5.315	−5.333	−5.351	−5.369	−5.387	−5.404	−5.421
−170	−5.069	−5.089	−5.109	−5.128	−5.147	−5.167	−5.186	−5.205	−5.223	−5.242
−160	−4.865	−4.886	−4.907	−4.928	−4.948	−4.969	−4.989	−5.010	−5.030	−5.050
−150	−4.648	−4.670	−4.693	−4.715	−4.737	−4.758	−4.780	−4.801	−4.823	−4.844
−140	−4.419	−4.442	−4.466	−4.489	−4.512	−4.535	−4.558	−4.581	−4.603	−4.626
−130	−4.177	−4.202	−4.226	−4.251	−4.275	−4.299	−4.323	−4.347	−4.371	−4.395
−120	−3.923	−3.949	−3.974	−4.000	−4.026	−4.051	−4.077	−4.102	−4.127	−4.152
−110	−3.656	−3.684	−3.711	−3.737	−3.764	−3.791	−3.818	−3.844	−3.870	−3.897
−100	−3.378	−3.407	−3.435	−3.463	−3.491	−3.519	−3.547	−3.574	−3.602	−3.629
−90	−3.089	−3.118	−3.147	−3.177	−3.206	−3.235	−3.264	−3.293	−3.321	−3.350
−80	−2.788	−2.818	−2.849	−2.879	−2.909	−2.939	−2.970	−2.999	−3.029	−3.059
−70	−2.475	−2.507	−2.539	−2.570	−2.602	−2.633	−2.664	−2.695	−2.726	−2.757
−60	−2.152	−2.185	−2.218	−2.250	−2.283	−2.315	−2.348	−2.380	−2.412	−2.444
−50	−1.819	−1.853	−1.886	−1.920	−1.953	−1.987	−2.020	−2.053	−2.087	−2.120
−40	−1.475	−1.510	−1.544	−1.579	−1.614	−1.648	−1.682	−1.717	−1.751	−1.785
−30	−1.121	−1.157	−1.192	−1.228	−1.263	−1.299	−1.334	−1.370	−1.405	−1.440
−20	−0.757	−0.794	−0.830	−0.867	−0.903	−0.940	−0.976	−1.013	−1.049	−1.085
−10	−0.383	−0.421	−0.458	−0.496	−0.534	−0.571	−0.608	−0.646	−0.683	−0.720
− 0	−0.000	−0.039	−0.077	−0.116	−0.154	−0.193	−0.231	−0.269	−0.307	−0.345
0	0.000	0.039	0.078	0.117	0.156	0.195	0.234	0.273	0.312	0.351
10	0.391	0.430	0.470	0.510	0.549	0.589	0.629	0.669	0.709	0.749
20	0.789	0.830	0.870	0.911	0.951	0.992	1.032	1.073	1.114	1.155
30	1.196	1.237	1.279	1.320	1.361	1.403	1.444	1.486	1.528	1.569
40	1.611	1.653	1.695	1.738	1.780	1.822	1.865	1.907	1.950	1.992
50	2.035	2.078	2.121	2.164	2.207	2.250	2.294	2.337	2.380	2.424
60	2.467	2.511	2.555	2.599	2.643	2.687	2.731	2.775	2.819	2.864
70	2.908	2.953	2.997	3.042	3.087	3.131	3.176	3.221	3.266	3.312
80	3.357	3.402	3.447	3.493	3.538	3.584	3.630	3.676	3.721	3.767
90	3.813	3.859	3.906	3.952	3.998	4.044	4.091	4.137	4.184	4.231
100	4.277	4.324	4.371	4.418	4.465	4.512	4.559	4.607	4.654	4.701
110	4.749	4.796	4.844	4.891	4.939	4.987	5.035	5.083	5.131	5.179
120	5.227	5.275	5.324	5.372	5.420	5.469	5.517	5.566	5.615	5.663
130	5.712	5.761	5.810	5.859	5.908	5.957	6.007	6.056	6.105	6.155
140	6.204	6.254	6.303	6.353	6.403	6.452	6.502	6.552	6.602	6.652
150	6.702	6.753	6.803	6.853	6.903	6.954	7.004	7.055	7.106	7.156
160	7.207	7.258	7.309	7.360	7.411	7.462	7.513	7.564	7.615	7.666
170	7.718	7.769	7.821	7.872	7.924	7.975	8.027	8.079	8.131	8.183
180	8.235	8.287	8.339	8.391	8.443	8.495	8.548	8.600	8.652	8.705
190	8.757	8.810	8.863	8.915	8.968	9.021	9.074	9.127	9.180	9.233
200	9.286	9.339	9.392	9.446	9.499	9.553	9.606	9.659	9.713	9.767
210	9.820	9.874	9.928	9.982	10.036	10.090	10.144	10.198	10.252	10.306
220	10.360	10.414	10.469	10.523	10.576	10.632	10.687	10.741	10.796	10.851
230	10.905	10.960	11.015	11.070	11.125	11.180	11.235	11.290	11.345	11.401
240	11.456	11.511	11.566	11.622	11.677	11.733	11.788	11.844	11.900	11.956
250	12.011	12.067	12.123	12.179	12.235	12.291	12.347	12.403	12.459	12.515
260	12.572	12.628	12.684	12.741	12.797	12.854	12.910	12.967	13.024	13.080
270	13.137	13.194	13.251	13.307	13.364	13.421	13.478	13.535	13.592	13.650
280	13.707	13.764	13.821	13.879	13.936	13.993	14.051	14.108	14.166	14.223
290	14.281	14.339	14.396	14.454	14.512	14.570	14.628	14.686	14.744	14.802
300	14.860	14.918	14.976	15.034	15.092	15.151	15.209	15.267	15.326	15.384
310	15.443	15.501	15.560	15.619	15.677	15.736	15.795	15.853	15.912	15.971
320	16.030	16.089	16.148	16.207	16.266	16.325	16.384	16.444	16.503	16.562
330	16.621	16.681	16.740	16.800	16.859	16.919	16.978	17.038	17.097	17.157
340	17.217	17.277	17.336	17.396	17.456	17.516	17.576	17.636	17.696	17.756
350	17.816	17.877	17.937	17.997	18.057	18.118	18.178	18.238	18.299	18.359
360	18.420	18.480	18.541	18.602	18.662	18.723	18.784	18.845	18.905	18.966
370	19.027	19.088	19.149	19.210	19.271	19.332	19.393	19.455	19.516	19.577
380	19.638	19.699	19.761	19.822	19.883	19.945	20.006	20.068	20.129	20.191
390	20.252	20.314	20.376	20.437	20.499	20.560	20.622	20.684	20.746	20.807
400	20.869									

RS data

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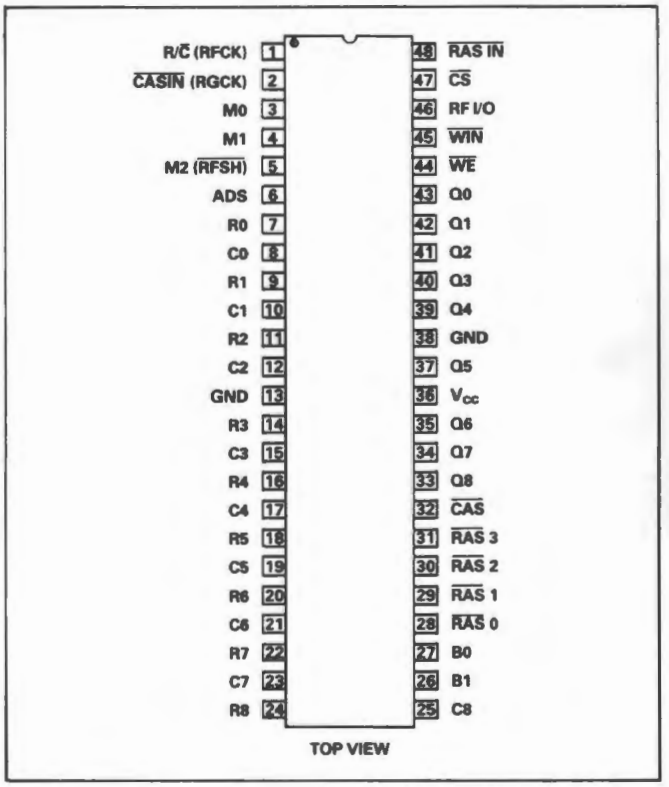
RS data

Dynamic ram controller i.c.

74S409/8409 **Stock number 301-842**

The 74S409 is a complete single chip dynamic memory controller and driver i.c. It will directly drive all 16K, 64K and 256K Drams with an address capability of 64K, 256K or 1M words. All control circuitry including capacitive load drivers to maximise a.c. performance are present, and operation in eight different refresh modes makes the device completely universal. The single +5V supply and 25ns typical propagation delay ease the overall operation of a memory system.



TOP VIEW

Absolute maximum ratings

Supply voltage V_{CC} ——— −0.5V to +7.0Vdc
Input voltage ——— −1.5V to +5.5V
Output current ——— 150mA
Storage temperature range ——— −65°C to +150°C
Lead temperature soldering 10s ——— 300°C

'Absolute maximum ratings' are the values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the device should be operated at these limits.

Main features

- All DRAM drive functions on one chip – minimises skew on outputs, maximises AC performance.
- On-chip capacitive load drivers (specified to drive up to 88 DRAMs).
- Directly drives all 16K, 64K, and 256K DRAMs.
- Capable of addressing 64K, 256K or IM words.
- Propagation delays of 25ns typical at 500pF load.
- 8 modes of operation: 3 access, 3 refresh and 2 set-up.

WARNING!

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Electrical characteristics V_{CC} = 5.0V ±5.0%, 0°C ≤ T_A ≥ 70°C Typicals are for V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Test conditions	Min	Typ	Max	Units
V_{CC}	Supply voltage		4.75		5.25	V
T_A	Ambient temperature		0		+70	°C
V_C	Input clamp voltage	V_{CC} = MIN, I_C = −12mA		−0.8	−1.2	V
I_{IH1}	Input high current for ADS. R/$\overline{C}$ only	V_{IN} = 2.5V		2.0	100	μA
I_{IH2}	Input high current for other input, except RF I/O	V_{IN} = 2.5V		1.0	50	μA
I_IRSI	Output load current RF I/O	V_{IN} = 0.5V, output high		−1.5	−2.5	mAV
I_ICTL	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IN} = 0.5V, chip deselect		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS. R/$\overline{C}$ only	V_{IN} = 0.5V		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	V_{IN} = 0.5V		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0			V
V_{OL1}	Output low voltage, except RF I/O	I_{OL} = 20mA		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	I_{OL} = 10mA		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	V_{OH} = −1mA	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	I_{OH} = −100μA	2.4	3.5		V
I_{1D}	Output high drive current, except RF I/O	V_{OUT} = 0.8V *		−200		mA
I_{0D}	Output low drive current, except RF I/O	V_{OUT} = 2.5V *		200		mA
I_{OZ}	THREE-STATE output current (address outputs)	0.4V ≤ V_{OUT} ≤ 2.7V, CS ≥ 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		250	325	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	T_A = 25°C		8		pF
C_{IN}	Input capacitance all other inputs	T_A = 25°C		5		pF

* This test is provided as a monitor of driver output source and sink current capacity. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

** These are absolute voltage with respect to pins 13 or 38 on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

Switching characteristics

V_{CC} = 5.0V ± 5.0%, 0°C ≤ T_A ≤ 70°C. See Figure 11 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

Symbol	Access Parameter	Test Conditions	Min	Typ	Max	Units
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 8a	95	125	160	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 8a, 8b	80	105	140	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 8a	40	48	60	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 8a, 8b	50	63	80	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 8a		98	125	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 8a, 8b		78	105	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figure 8a		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 8a		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figure 8b	40	54	70	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figure 8a		90	120	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figures 8a, 8b		75	105	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 7a, 7b, 8a, 8b	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 7a, 7b, 8a, 8b	15	23	32	ns
t_{APDL}	Address input to output low delay	Figures 7a, 7b, 8a, 8b		25	40	ns
t_{APDH}	Address input to output low delay	Figures 7a, 7b, 8a, 8b		25	40	ns
t_{SPDL}	Address strobe to address output low	Figures 7a, 7b		40	60	ns
t_{SPDH}	Address strobe to address output high	Figures 7a, 7b		40	60	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 7b	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 7b	15	30	60	ns
t_{CRS}	$\overline{CASIN}$ setup time to $\overline{RASIN}$ high (Mode 6)	Figure 8b	35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (RIC low in Mode 4)	Figure 7b	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 7b	25	39	50	ns
t_{RCC}	Column select to column address valid	Figure 7a		40	58	ns
t_{RCR}	Row select to row address valid	Figures 7a, 7b		40	58	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 2			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figures 2, 9	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figures 2, 9	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	$\overline{CS}$ = X, Figures 2, 3, 4		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figures 2, 3		45	60	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figures 2, 4		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	C_L = 50pF, Figure 2			80	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	C_L = 50pF, Figure 2			80	ns
t_{RGEOB}	$\overline{RGCK}$ low to end-of-burst low	C_L = 50pF, Figure 4			95	ns
t_{MCEOB}	Mode change to end-of-burst high	C_L = 50pF, Figure 4			75	ns

Symbol	Refresh Parameter	Test Conditions	Min	Typ	Max	Units
t_{FRQL}	$\overline{RFCK}$ low to forced $\overline{RFRQ}$ low	C_L = 50pF, Figure 3		20	30	ns
t_{FRQH}	$\overline{RGCK}$ low to force $\overline{RFRQ}$ high	C_L = 50pF, Figure 3		50	75	ns
t_{RGRL}	$\overline{RGCK}$ low to $\overline{RAS}$ low	Figure 3	50	65	95	ns
t_{RGRH}	$\overline{RGCK}$ low to $\overline{RAS}$ high	Figure 3	40	60	85	ns
t_{RFRH}	$\overline{RFSH}$ high to $\overline{RAS}$ high (ending forced RFSH)	See Mode 1 description	55	80	110	ns
t_{CSCT}	$\overline{CS}$ high to $\overline{RFSH}$ counter valid	Figure 9		55	70	ns
t_{RHAV}	$\overline{RASIN}$ high to input address valid	Figure 9		55	95	ns

Symbol	Access 3-State Parameter	Test Conditions	Min	Typ	Max	Units
t_{ZH}	$\overline{CS}$ low to address output high from Hi	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15pF, Figures 9, 12 R2 = 1k, S1 open		20	40	ns
t_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figures 9, 10 R1 = 1k, S2 open		25	50	ns
t_{HZH}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$ RASO-3) high from Hi-Z high	Figures 9, 12 R2 = 750Ω, S1 open		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, RASO-3) Hi-Z high from high	C_L = 15pF R2 = 750Ω, S1 open		40	75	ns
t_{HZL}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, RASO-3) low from Hi-Z high	Figure 12 S1, S2 open *		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, RASO-3) Hi-Z high from low	C_L = 15pF, Figure 12, R2 = 750Ω, S1 open *		40	75	ns

* Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

General notes for test conditions:

1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8, C_L = 500pF; RAS0-RAS3, C_L = 500pF; CAS C_L = 600pF unless otherwise noted.

2: Input pulse 0V to 3.0V, $t_R = t_F$ = 2.5 ns, f = 2.5MHz, t_{PW} = 200ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

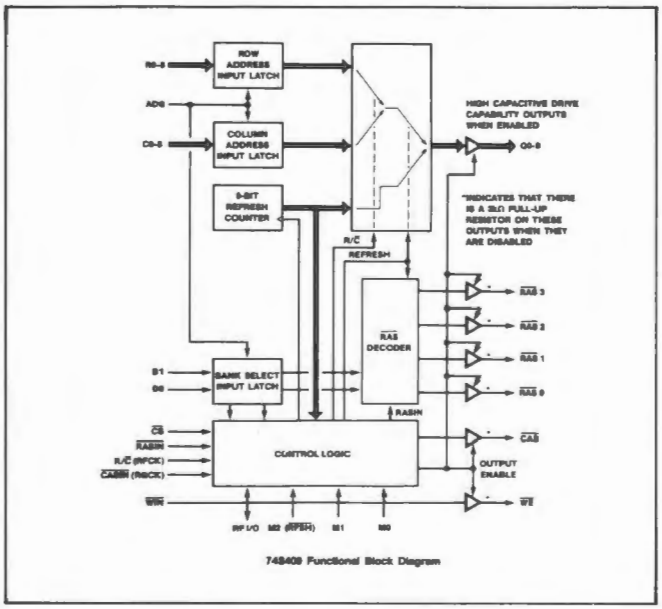
3: The load capacitance on RF/IO should not exceed 50pF.

Operating conditions

Symbol	Parameter	Figure Ref.	Min	Typ	Max	Units
t_{RAH}	Row address hold time (Mode 5)	Figure 8a	30			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 8a, 8b	20			ns
t_{ASC}	Column address setup time (Mode 5)	Figure 8a	8			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 8a, 8b	6			ns
t_{ASA}	Address setup time to ADS	Figures 7a, 7b, 8a, 8b	15			ns
t_{AHA}	Address hold time from ADS	Figures 7a, 7b, 8a, 8b	15			ns
t_{ADS}	Address strobe pulse width	Figures 7a, 7b, 8a, 8b	30			ns
t_{RHA}	Row address held from column select	Figure 7a	10			ns
t_{RC}	Refresh cycle period	Figure 2	100			ns
$t_{RASINLH}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 2	50			ns
t_{RST}	Counter reset pulse width	Figure 2	70			ns
t_{RFCKLH}	Minimum pulse width of $\overline{RFCK}$	Figure 9	100			ns
T	Period of $\overline{RAS}$ generator clock	Figure 3	100			ns
t_{RGCKL}	Minimum pulse width low of $\overline{RGCK}$	Figure 3	35			ns
t_{RGCKH}	Minimum pulse width high of $\overline{RGCK}$	Figure 3	35			ns
t_{CSRL}	$\overline{CS}$ low to access $\overline{RASIN}$ low	See Mode 5 description	10			ns
t_{RFSRG}	$\overline{RFSH}$ low set-up to $\overline{RGCK}$ low (Mode 1)	See Mode 1 description	35			ns
t_{RQHRF}	$\overline{RFSH}$ hold time from $\overline{RFSH}$ $\overline{RQST}$ (RF I/O)	Figure 3	2T			ns

Mode	(RFSH) M2	M1	M0	Mode of Operation	Conditions
0	0	0	0	Externally controlled refresh	RF I/O = $\overline{EOC}$
1	0	0	1	Auto refresh – forced	RF I/O = Refresh request ($\overline{RFRQ}$)
2	0	1	0	Internal auto burst refresh	RF I/O = $\overline{EOC}$
3a	0	1	1	All-RAS auto write	RF I/O = $\overline{EOC}$; all $\overline{RAS}$ active
3b	0	1	1	Externally controlled All-RAS access	All-$\overline{RAS}$ active
4	1	0	0	Externally controlled access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto access, slow t_{RAH}, hidden refresh	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto access, fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set end of count	See Table 3 for Mode 7

Table 1 **74S409 Mode Select Options**



74S409 Functional Block Diagram

Description

Dynamic memory system designs, which formerly required several support chips to drive the memory array, can now be implemented with a single IC... the 74S409 Multi-Mode Dynamic RAM Controller/Driver. The 74S409 is capable of driving all 16k and 64k Dynamic RAMs (DRAMs) as well as 256k DRAMs. Since the 74S409 is a one-chip solution (including capacitive-load drivers), it minimises propagation delay skews, the major performance disadvantage of multiple-chip memory drive and control.

The 74S409's 8 modes of operation offer a wide selection of DRAM control capabilities. Memory access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialisation is both simple and fast.

The 74S409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. All output drivers are capable of driving 500pF loads with propagation delays of 25ns. The 74S409 timing parameters are specified driving the typical load capacitance of 88 DRAMs, including trace capacitance.

The 74S409 has 3 mode-control pins: M2, M1, and M0, where M2 is in general REFRESH. These 3 pins select 8 modes of operation. Inputs B1 and B0 in the memory access modes (M2 = 1), are select inputs which select one of four $\overline{RAS}$ outputs. During normal access, the 9 address outputs can be selected from the Row Address Latch or the Column Address Latch. During refresh, the 9-bit on-chip refresh counter is enabled onto the address bus and in this mode all $\overline{RAS}$ outputs are selected, while $\overline{CAS}$ is inhibited.

The 74S409 can drive up to 4 banks of DRAMs, with each bank comprised of 16k's, 64k's, or 256k's. Control signal outputs $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are provided with the same drive capability. Each $\overline{RAS}$ output drives one bank of DRAMs so that the four $\overline{RAS}$ outputs are used to select the banks, while $\overline{CAS}$, $\overline{WE}$, and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the data outputs in three-state. Only the bank with its associated $\overline{RAS}$ low will be written to or read from.

Pin definitions

V_{CC}, GND, GND, V_{CC} = 5V ± 5%. The three supply pins have been assigned to the centre of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution would be a 1μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

R0-R8: Row Address Inputs.

C0-C8: Column Address Inputs.

Q0-Q8: Multiplexed Address Outputs – Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input – Enables selected $\overline{RAS}_n$ output when M2 ($\overline{RFSH}$) is high, or all $\overline{RAS}_n$ outputs when $\overline{RFSH}$ is low.

R/$\overline{C}$ (RFCK) – In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/Column Select Input: selects either the row or column address input latch onto the output bus.

$\overline{\text{CASIN}}$ (RGCK) – In Auto-Refresh Mode, Auto Burst Mode, and All-$\overline{\text{RAS}}$ Auto-Write Mode, this pin is the $\overline{\text{RAS}}$ Generator Clock input. In all other modes it is $\overline{\text{CASIN}}$ (Column Address Strobe Input), which inhibits $\overline{\text{CAS}}$ output when high in Modes 4 and 3b. In Mode 6 it can be used to prolong $\overline{\text{CAS}}$ output.

ADS: Address (Latch) Strobe Input – Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; Latches on high-to-low transition.

CS: Chip Select Input – Three-states the Address Outputs and puts the control signal into a high-impedance logic '1' state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.

M0, M1, M2: Mode Control Inputs – These 3 control pins determine the 8 major modes of operation of the 74S409 as depicted in Table 1.

RF I/O – The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low in Modes 0 and 2 when the End-of-Count output is at 127, 255, or 511 (see Table 3). In Auto-Refresh Mode it is the Refresh Request output.

$\overline{\text{WIN}}$: Write Enable Input.

$\overline{\text{WE}}$: Write Enable Output – Buffered output from $\overline{\text{WIN}}$.

$\overline{\text{CAS}}$: Column Address Strobe Output – In Modes 3a, 5, and 6, $\overline{\text{CAS}}$ transitions low following valid column address. In Modes 3b and 4, it goes low after R/$\overline{\text{C}}$ goes low, or follows $\overline{\text{CASIN}}$ going low if R/$\overline{\text{C}}$ is already low. $\overline{\text{CAS}}$ is high during refresh.

$\overline{\text{RAS}}$ 0-3: Row Address Strobe Outputs – Selects a memory bank decoded from B1 and B0 (see Table 2), if $\overline{\text{RFSH}}$ is high. If $\overline{\text{RFSH}}$ is low, all banks are selected.

B0, B1: Bank Select Inputs – Strobed by ADS. Decoded to enable one of the $\overline{\text{RAS}}$ outputs when $\overline{\text{RASIN}}$ goes low. Also used to define End-of-Count in Mode 7 (Table 3).

Conditions for all modes

Input addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter.

The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{\text{RASIN}}$ and R/$\overline{\text{C}}$ are initially high. When the address inputs are enabled into the address latches, the row addresses appear on the Q outputs. The address strobe also inputs the bank-select address, (B0 and B1). If $\overline{\text{CS}}$ is low, all outputs are enabled. When $\overline{\text{CS}}$ is transitioned high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S409s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{\text{CS}}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive capability

The 74S409 has timing parameters that are specified with up to 600pF loads. In a typical memory system this is equivalent to about 88, 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 10. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S409 driving any 16k or 64k DRAMs

The 74S409 can drive any 16k or 64k DRAMs. All 16k DRAMs are basically the same configuration, including the newer 5V-only version. Hence, in most applications, different manufacturers' DRAMs are interchangeable (for the same supply-rail chips), and the 74S409 can drive all 16k DRAMs (see Figure 1a).

There are three basic configurations for the 5V-only 64k DRAMs: a 128-row by 512-column array with an on-RAM refresh counter, a 128-row by 512-column array with no on-RAM refresh counter, and a 256-row by 256-column array with no on-RAM refresh counter. The 74S409 can drive all three configurations, and at the same time allows them all to be interchangeable (as shown in Figures 1b and 1c). Since the 9-bit on-chip refresh counter can be used as a 7-bit refresh counter for the 128-row configuration, or as an 8-bit refresh counter for the 256-row configuration, the on-RAM refresh counter (if present) is never used. As long as 128 rows are refreshed every 2ms (i.e. 256 rows in 4ms) all DRAM types are correctly refreshed.

This makes all the 64k DRAM configurations interchangeable when used with the 74S409, allowing maximum flexibility in the choice of DRAMs.

Read, write, and read-modify-write cycles

The output signal, $\overline{\text{WE}}$, determines what type of memory access cycle the memory will perform. If $\overline{\text{WE}}$ is kept high while $\overline{\text{CAS}}$ goes low, a read cycle occurs. If $\overline{\text{WE}}$ goes low before $\overline{\text{CAS}}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{\text{CAS}}$ goes low. If $\overline{\text{WE}}$ goes low later than t_{CWD} after $\overline{\text{CAS}}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{\text{WE}}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{\text{WE}}$, which follows $\overline{\text{WIN}}$.

Power-up initialise

When V_{CC} is first applied to the 74S409, an initialise pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

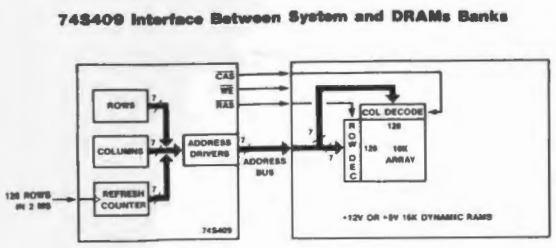


Figure 1a **74S409 with any 16K DRAMs**

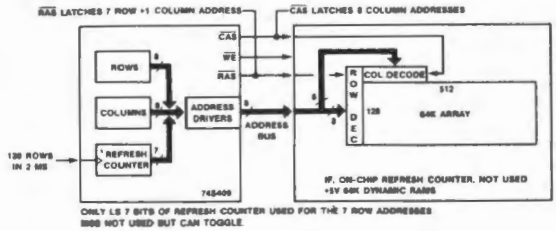


Figure 1b **74S409 with 128 row x 512 column 64K DRAM**

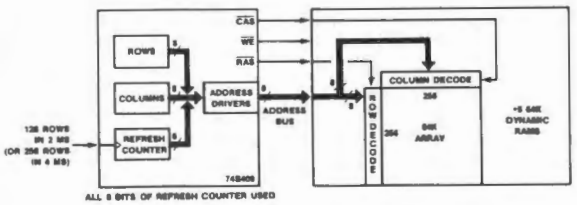


Figure 1c **74S409 with 256 row x 256 column 64k DRAM**

74S409 functional mode descriptions

Mode 0 – externally controlled refresh

Figure 2 is the Externally Controlled Refresh Timing. In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled. When $\overline{RAS}$ occurs, the enabled row in the DRAM is refreshed. In the Externally Controlled Refresh mode, all $\overline{RAS}$ outputs are enabled following $\overline{RASIN}$, and $\overline{CAS}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{RASIN}$ or $\overline{RFSH}$ goes low-to-high while the other is low. RF I/O goes low when the count is 127, 255, or 511, as set by End-of-Count (see Table 3), with $\overline{RASIN}$ and $\overline{RFSH}$ low. To reset the counter to all zeroes, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and $\overline{RFSH}$ can transition low simultaneously because the refresh counter becomes valid on the output bus t_{RFLCT} after $\overline{RFSH}$ goes low, which is a shorter time than t_{RFPDL}. This means the counter address is valid on the Q outputs before $\overline{RAS}$ occurs on all $\overline{RAS}$ outputs, strobing the counter address into that row of all the DRAMs. Refer to Figure 2. To perform externally controlled burst refresh, $\overline{RFSH}$ initially can again have the same edge as $\overline{RASIN}$, but then can maintain a low state, since $\overline{RASIN}$ going low-to-high increments the counter (performing the burst refresh).

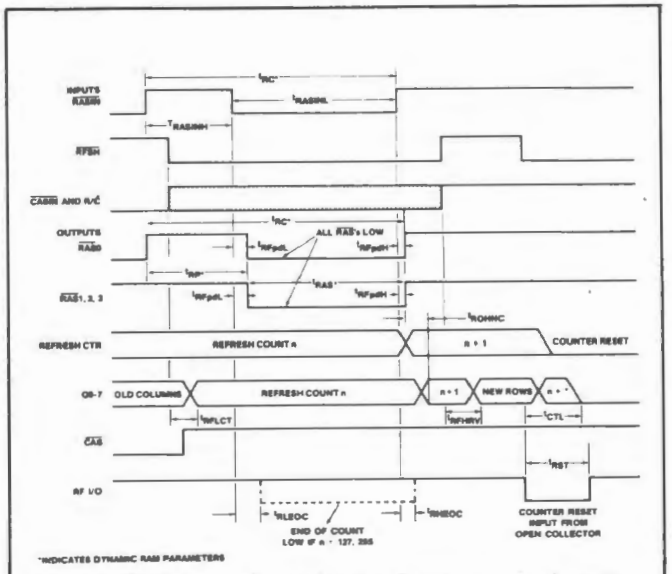


Figure 2 **External control refresh cycle (modes 0, 1, 2)**

Mode 1 – automatic forced refresh

In Mode 1, the R/$\overline{C}$ (RFCK) pin becomes RFCK (refresh cycle clock), instead of R/$\overline{C}$, and $\overline{CAS}$ remains high. If RFCK is kept permanently high, then whenever M2 ($\overline{RFSH}$) goes low, an externally controlled refresh will occur and all $\overline{RAS}$ outputs will follow $\overline{RASIN}$, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but when set low externally through an open-collector driver, the refresh counter resets as normal. This externally controlled method may be preferred when operating in the Automatic Access mode (Mode 5), where hidden or forced refreshing is undesirable, but refreshing is still necessary.

If RFCK is an input clock signal, one (and only one) refresh cycle must take place every RFCK cycle. Refer to Figure 9. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O ($\overline{Refresh\ Request}$) goes low immediately after RFCK goes low, indicating to the system that a forced refresh is requested. The system must allow a forced refresh to take place while RFCK is low (refer to Figure 3). The $\overline{Refresh\ Request}$ signal on RF I/O may be connected to a $\overline{Hold}$ or $\overline{Bus\ Request}$ input to the system. The system acknowledges the $\overline{Hold}$ or $\overline{Bus\ Request}$ when ready, and outputs Hold Acknowledge or $\overline{Bus\ Request\ Acknowledge}$. If this is connected to the M2 ($\overline{RFSH}$) pin, a forced-refresh cycle will be initiated by the 74S409, and $\overline{RAS}$ will be internally generated on all four $\overline{RAS}$ outputs, to strobe the refresh counter contents on the address outputs into all the DRAMs. An external $\overline{RAS}$ Generator Clock (RGCK) is required for this function. It is fed to the $\overline{CASIN}$ (RGCK) pin, and may be up to 10MHz. Whenever M2 goes low (inducing a forced refresh), $\overline{RAS}$ remains high for one to two periods of RGCK, depending on when M2 goes low relative to the high-to-low triggering edge of RGCK; $\overline{RAS}$ then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to $\overline{RAS}$ going low, M2 should go low t_{RFSRG} before the next falling edge of RGCK. The $\overline{Refresh\ Request}$ on RF I/O is terminated as $\overline{RAS}$ begins, so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh $\overline{RAS}$ will have ended, and

normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh $\overline{RAS}$ end in less than 2 periods of RGCK from the time $\overline{RAS}$ went low, then M2 may go high earlier than t_{FRQH} after RF I/O goes high and $\overline{RAS}$ will go high t_{RFRH} after M2.

To allow the forced refresh, the system will have been inactive for about 4 periods of RGCK, which can be as fast as 400ns every RFCK cycle. To guarantee a refresh of 128 rows every 2ms, a period of up to 16μs is required to RFCK. In other words, the system may be down for as little as 400ns every 16μs, or 2.5% of the time. Although this is not excessive, it may be preferable to perform a Hidden Refresh each RFCK cycle, which is allowed while still in the Auto-Access mode, (Mode 5).

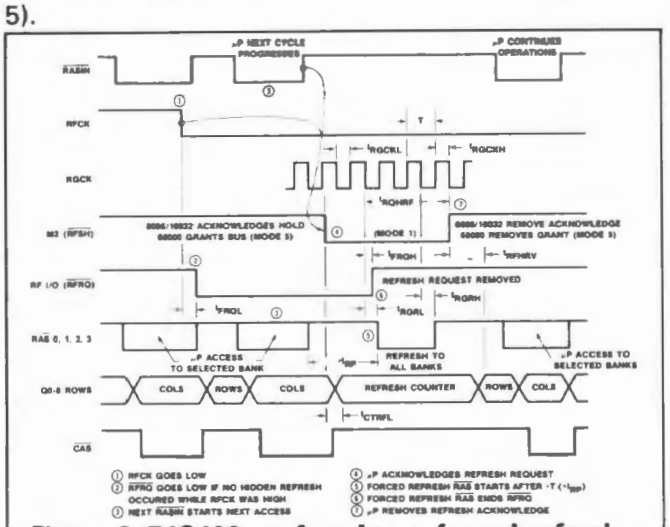


Figure 3 **74S409 performing a forced refresh (mode 5-1-5) with various microprocessors**

Mode 2 – automatic burst refresh

This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2ms (see Figure 4). When the 74S409 enters this mode, $\overline{CASIN}$ (RGCK) becomes the RAS Generator Clock (RGCK), and $\overline{RASIN}$ is disabled. $\overline{CAS}$ remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last $\overline{RAS}$ has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to indicate the End-of-Burst condition.

The signal on all four $\overline{RAS}$ outputs is just a divide-by-four of RGCK; in other words, if RGCK has a 100ns period, $\overline{RAS}$ is high and low for 200ns each cycle. The refresh counter increments at the end of each $\overline{RAS}$, starting from the count it contained when the mode was entered. If this was zero, then for a RGCK with a 100ns period with End-of-Count set to 127, RF I/O will go low after 128 x 0.4μs, or 51.2μs. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins.

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the 74S409 (set to Mode 2), causing it to perform a complete burst refresh. When end-of-burst occurs (after 26μs) power can then be removed from the 74S409 for 2ms, consuming an

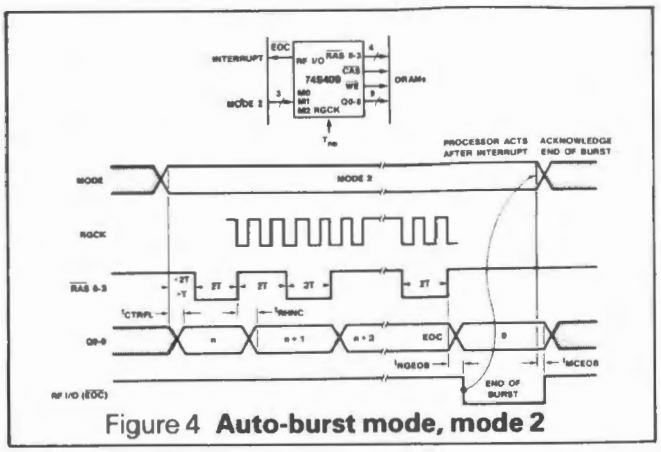


Figure 4 **Auto-burst mode, mode 2**

average power of 1.3% of normal operating power. No control signal glitches occur when switching power to the 74S409.

Mode 3a – all-$\overline{RAS}$ automatic write

Mode 3a is useful at system initialisation, when the memory is being cleared (i.e., with all-zeroes in the data field and the corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All $\overline{RAS}$ outputs are activated, as in refresh, and so are $\overline{CAS}$ and $\overline{WE}$. To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations.

To select this mode, B1 and B0 must have previously been set to 00, 01, or 10 in Mode 7, depending on the DRAM size. For example, for 16k DRAMs, B1 and B0 are 00. For 64k DRAMs, B1 and B0 are 01, so that for the configuration of Figure 1b, the 8 refresh counter bits are strobed by $\overline{RAS}$ into the 7 row addresses and the ninth column address. After this Automatic-Write process, B1 and B0 must be set again in Mode 7 to 00 to set End-of-Count to 127. For the configuration of Figure 1c, B1 and B0 set to 01 will work for Automatic-Write and End-of-Count equals 255.

In this mode, R/C is disabled, $\overline{WE}$ is permanently enabled low, and $\overline{CASIN}$ (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127, 255, or 511 (as set by End-of-Count in Mode 7), and the $\overline{RAS}$ outputs are active.

Referring to Figure 5a, an external 8-bit counter (for 64k DRAMs) with three-state outputs is required and must be connected to the column address inputs. It is enabled only during this mode, and is clocked from RF I/O. The 74S409 refresh counter is used to address the rows, and the column address is supplied by the external counter. Every row for each column address is written to in all four banks. At the End-of-Count RF I/O goes low, which clocks the external counter.

Therefore, for each column address, the refresh counter first outputs row-0 to the address bus and all four $\overline{RAS}$ outputs strobe this row address into the DRAMs (see Figure 5b). A minimum of 30ns after $\overline{RAS}$ goes low (t_{RAH} = 30ns), the refresh counter is disabled and the column address input latch is enabled onto the address bus. About 14ns after the column address is valid, $\overline{CAS}$ goes low, (t_{ASC} = +14ns), strobing the column address into the DRAMs. When $\overline{RAS}$ and $\overline{CAS}$ go high the refresh counter increments to the next row and the cycle repeats. Since $\overline{WE}$ is kept low in this mode, the data at DI (input data) of the DRAMs is written

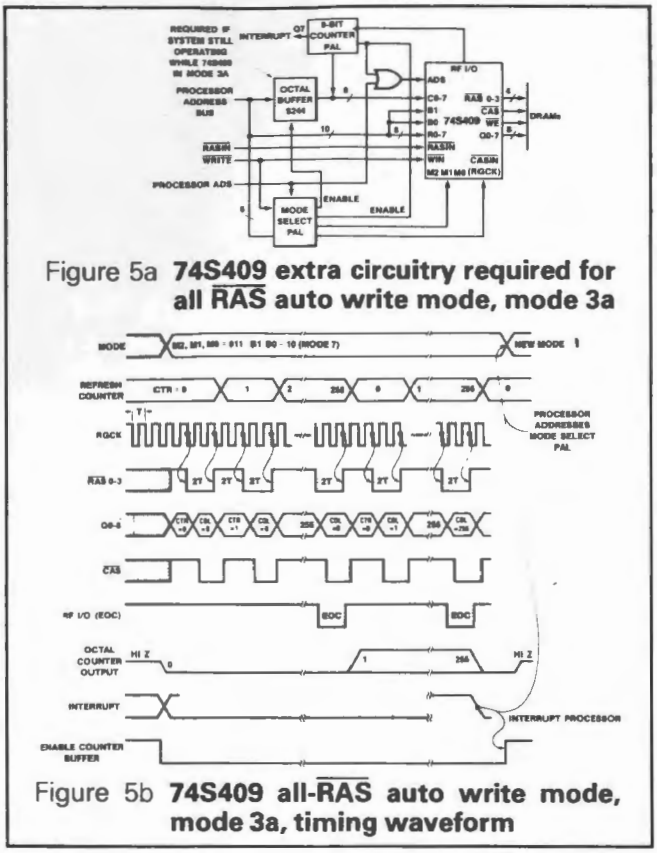


Figure 5a **74S409 extra circuitry required for all $\overline{RAS}$ auto write mode, mode 3a**

Figure 5b **74S409 all-$\overline{RAS}$ auto write mode, mode 3a, timing waveform**

into each row of the latched column. During each cycle $\overline{RAS}$ is high for two periods of RGCK and low for two periods, giving a total write-cycle time of 400 ns minimum, which is adequate for most 16k and 64k DRAMs. On the last row of a column, RF I/O increments the external counter to the next column address.

At the end of the last column address, an interrupt is generated from the external counter to let the system know that initialisation has been completed. During the entire initialisation time, the system can be performing other initialisation functions. This approach to memory initialisation is both automatic and fast. For instance, if four banks of 64k DRAMs are used, and RGCK is 100 ns, a write cycle to the same location in all four banks takes 400 ns, so the total time taken in initialising the 64k DRAMs is 65k x 400 ns or 26 ms. When the system receives the interrupt, the external counter must be

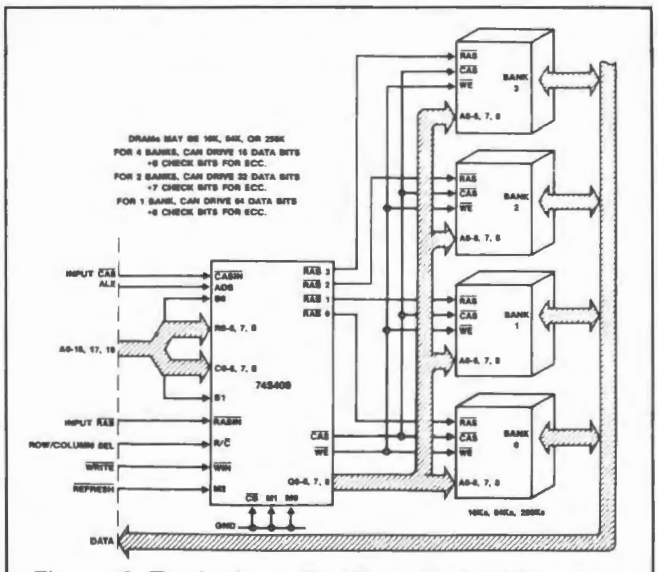


Figure 6 **Typical application of 74S409 using externally controlled access and refresh in modes 0 and 4**

permanently disabled. ADS and $\overline{CS}$ are interfaced by the system, and the 74S409 mode is changed. The interrupt must then be disabled.

Mode 3b – externally controlled all-RAS write

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialisation, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S409 for the next write cycle. This method is slower than Mode 3a since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialisation, and is not free for other initialisation operations. However, initialisation sequence timing is under system control, which may provide some system advantage.

Mode 4 – externally controlled access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in Figure 6.

Output address selection

Refer to Figure 7a. With M2 ($\overline{RFSH}$) and R/$\overline{C}$ high, the row address latch contents are transferred to the multiplexed address bus output Q0-Q8, provided $\overline{CS}$ is set low. The column address latch contents are output after R/$\overline{C}$ goes low. $\overline{RASIN}$ can go low after the row addressers have been set up on Q0-Q8. This selects one of the $\overline{RAS}$ outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 ns later column addresses appear on the Q outputs.

Automatic CAS generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/$\overline{C}$. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time

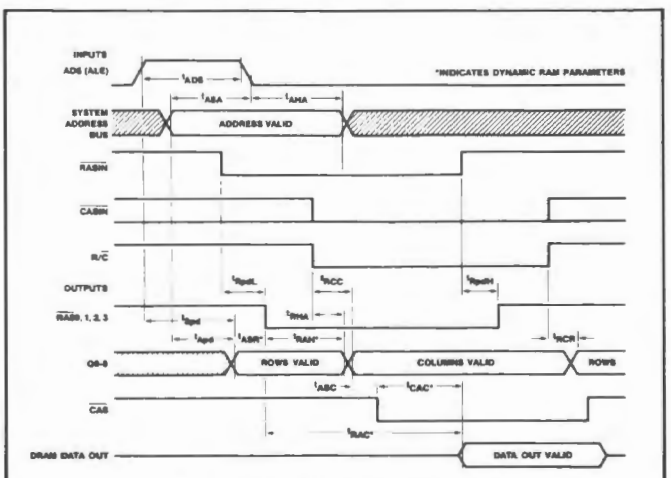


Figure 7a **Read cycle timing (mode 4)**

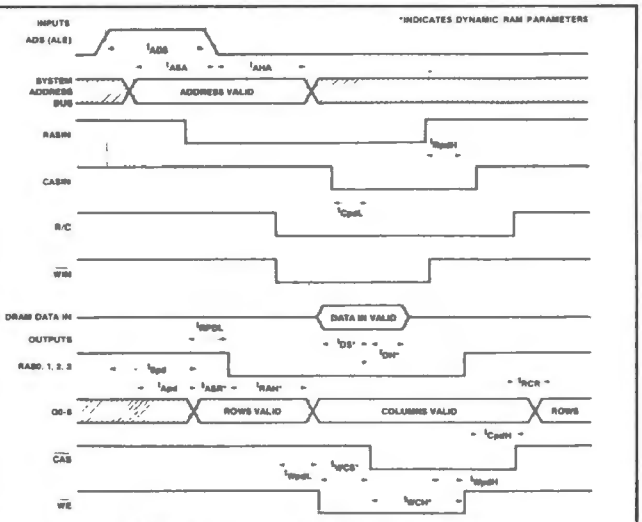


Figure 7b **Write cycle timing (mode 4)**

(see Figure 7b). For maximum system speed, $\overline{CASIN}$ can be kept low, since $\overline{CAS}$ will automatically occur approximately 20ns after the column addresses are valid, or about 60ns after R/$\overline{C}$ goes low (see Figure 7a). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0ns or −10ns. In other words, a t_{ASC} greater than 0ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast memory access

For faster access time, R/$\overline{C}$ can go low a time delay ($t_{RPDL} + t_{RAH} - t_{RHA}$) after $\overline{RASIN}$ goes low, where t_{RAH} is the Row-Address hold-time of the DRAM.

Mode 5 – automatic access with hidden refresh

The Auto Access with Hidden Refresh mode has two advantages over the Externally Controlled Access mode, due to the fact that all outputs except $\overline{WE}$ are initiated from $\overline{RASIN}$. First, inputs R/$\overline{C}$ and $\overline{CASIN}$ are unnecessary and can be used for other functions (see Refreshing, below). Secondly, because the output control signals are derived internally from one input signal ($\overline{RASIN}$), timing-skew problems are reduced, thereby reducing memory access time substantially or allowing use of slower DRAMs. The automatic access features of Mode 5 (and Mode 6) of the 74S409 make DRAM accessing appear essentially 'static'.

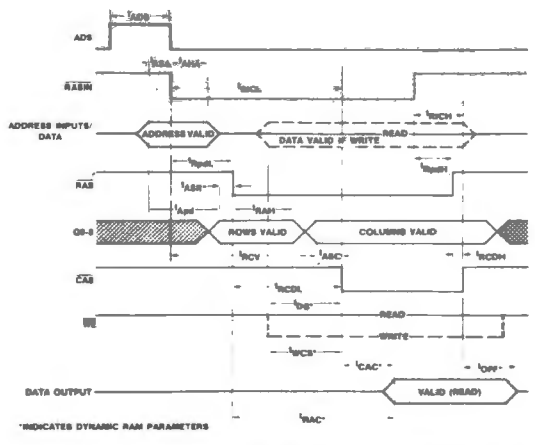


Figure 8a **Modes 5, 6 timing ($\overline{CASIN}$ high in mode 6)**

Automatic access control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{CAS}$ occurs. This is all performed automatically by the 74S409 in this mode.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (t_{ASR}), is 0ns on most DRAMs. The 74S409 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 8a).

Next, the row address is disabled after t_{RAH} (30ns minimum); in most DRAMs, t_{RAH} minimum is less than 30ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15ns); to $\overline{RAS}$ (27ns); to rows held (50ns); to columns valid (25ns); to $\overline{CAS}$ (23ns) = 140ns (that is, 125ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

Refreshing

Because R/$\overline{C}$ and $\overline{CASIN}$ are not used in this mode, R/C becomes RFCK (refresh clock) and $\overline{CASIN}$ becomes RGCK ($\overline{RAS}$ generator clock). With these two signals it is possible to perform refreshing without extra ICs, and without holding up the processor.

One refresh cycle must occur during each refresh clock period and then the refresh address must be incremented to the next refresh cycle. As long as 128 rows are refreshed every 2ms (one row every 16μs), all 16k and 64k DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than 16μs. RFCK going high sets an internal refresh-request flip-flop. First the 74S409 will attempt to perform a hidden refresh so that the system throughput will not be affected. If, during the time RFCK is high, $\overline{CS}$ on the 74S409 goes high and $\overline{RASIN}$ occurs, a hidden refresh will occur. In this case, $\overline{RASIN}$ should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the 74S409 will perform a refresh. The refresh counter is enabled to the address outputs whenever $\overline{CS}$ goes high with RFCK high, and all $\overline{RAS}$ outputs follow $\overline{RASIN}$. If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flip-flop is reset so no further refresh can occur until the next RFCK period starts with the positive-going edge of RFCK. Refer to Figure 9.

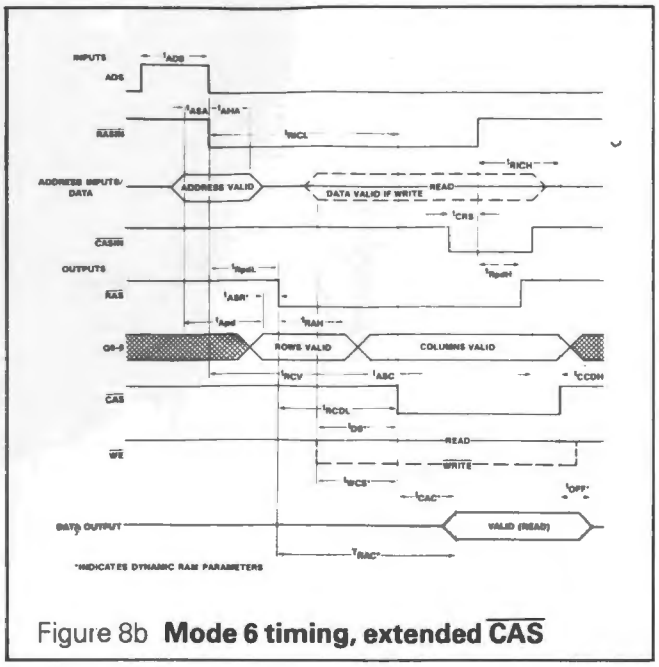


Figure 8b **Mode 6 timing, extended $\overline{CAS}$**

To determine the probability of a Hidden Refresh occurring, assume each system cycle takes 400 ns and RFCK is high for 8 μs, then the system has 20 chances to not select 74S409. If during this time a hidden refresh did not occur, then the 74S409 forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After RFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 ($\overline{RFSH}$) low does the 74S409 initiate a forced refresh (which is performed automatically). Refer to Mode 1, and Figure 3. The internal refresh request flip-flop is then reset.

Figure 9 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and $\overline{CS}$ again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic '1') and the address outputs go three-

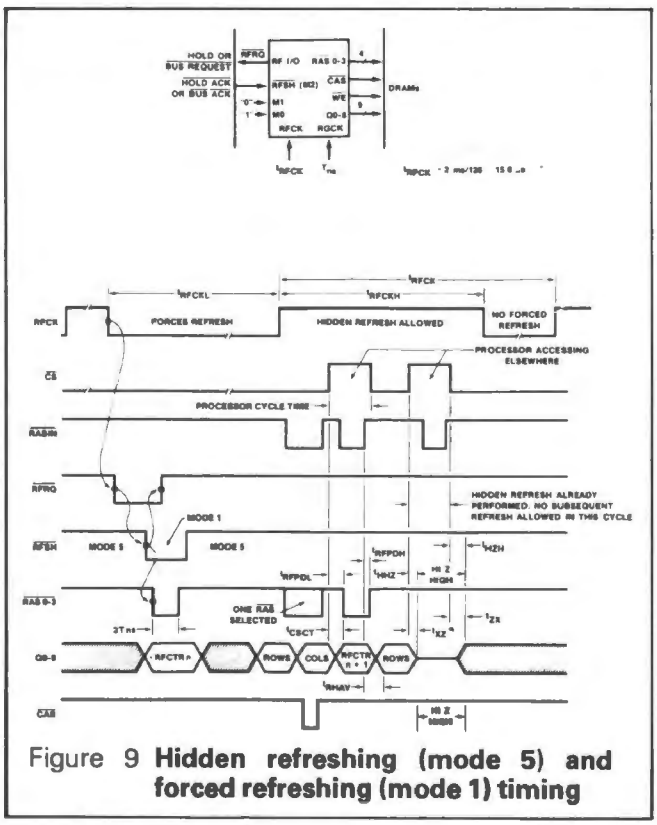


Figure 9 **Hidden refreshing (mode 5) and forced refreshing (mode 1) timing**

Bank Select (strobed by ADS)		Enabled $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Table 2 **Memory bank decode**

state until $\overline{CS}$ again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50 per cent; in fact, the low-time should be designed to be a minimum. This is determined by the worst-case time (required by the system) to respond to the 74S409's forced-refresh request.

Note that $\overline{RASIN}$ going low earlier than t_{CSRL} after $\overline{CS}$ goes low may result in the 74S409 interpreting the $\overline{RASIN}$ as a hidden refresh $\overline{RASIN}$ if no hidden refresh has occurred in the current RFCK cycle. In this case, all $\overline{RAS}$ outputs would go low for a short time. Thus, it is suggested that when using Mode 5, $\overline{RASIN}$ should be held high until t_{CSRL} after $\overline{CS}$ goes low if a refresh is not intended.

Mode 6 – fast automatic access

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20 ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10 ns to 15 ns) in applications requiring fast access times; $\overline{RASIN}$ to $\overline{CAS}$ is typically 105 ns.

In this mode, the R/$\overline{C}$ (RFCK) pin is not used, but $\overline{CASIN}$ (RGCK) is used as $\overline{CASIN}$ to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 8b. This is desirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to

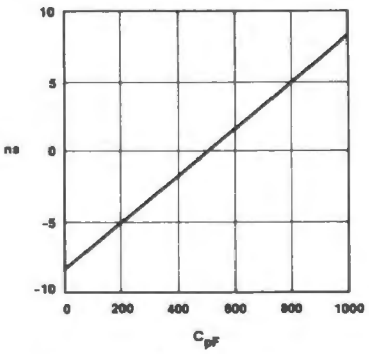


Figure 10 **Change in propagation delay vs loading capacitance relative to a 500pF load**

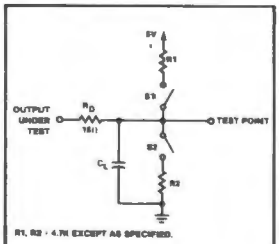


Figure 11 **Standard test load**

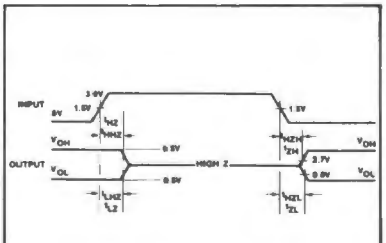


Figure 12 **Waveform**

RS data

meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by $\overline{CASIN}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{CASIN}$ subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, $\overline{CASIN}$ should be set high in Mode 6.

There is no internal refresh-request flip-flop in this mode, so any refreshing required must be done by entering Mode 0 or Mode 2.

Mode 7 – set End-of-Count

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same $\overline{EOC}$ is 127; with B1 = 0 and B0 = 1, $\overline{EOC}$ is 255; and with B1 = 1 and B0 = 0, $\overline{EOC}$ is 511. This selected value of $\overline{EOC}$ will be used until the next Mode 7 selection. At power-up the $\overline{EOC}$ is automatically set to 127 (B1 and B0 set to 11).

Bank Select (Strobed by ADS)		End of Count Selected
B1	B0	
0	0	127
0	1	255
1	0	511
1	1	127

Table 3 **Mode 7**

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RS data

Dual 8-bit D to A converter i.c. 7528

Stock number 301-921

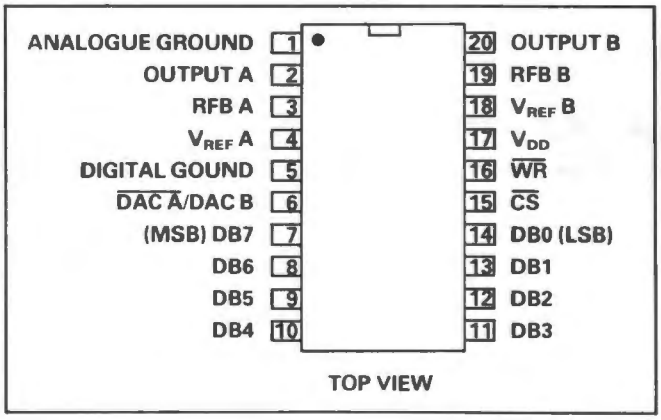
The 7528 is a monolithic dual 8-bit digital to analogue converter i.c. in a compact 20-pin DIL package offering excellent DAC to DAC matching. Separate on chip latches are provided for each DAC allowing easy microprocessor interface. Data is input via a common 8-bit TTL/CMOS compatible input port with the control $\overline{DACA}$/DACB selecting which DAC is loaded. The load cycle is similar to a ram write cycle and is bus compatible with most 8-bit microprocessor systems. Operation is from a single +5V to +15V power supply with low power consumption. Both converters work on a four quadrant multiplication technique with separate reference and feedback connections for each DAC.

Absolute maximum ratings

V_{DD} to analogue or digital ground	0V to +17V
Analogue ground to digital ground differential	V_{DD}
Digital input voltage to digital ground	−0.3V to +15V
Pin 2 and 20 to analogue ground	−0.3V to + 15V
Pin 4 and 18 to analogue ground	±25V
Power dissipation	450mW
Operating temperature range	0°C to +70°C
Storage temperature range	−65°C to +150°C
Lead temperature 10s soldering	+300°C

Features

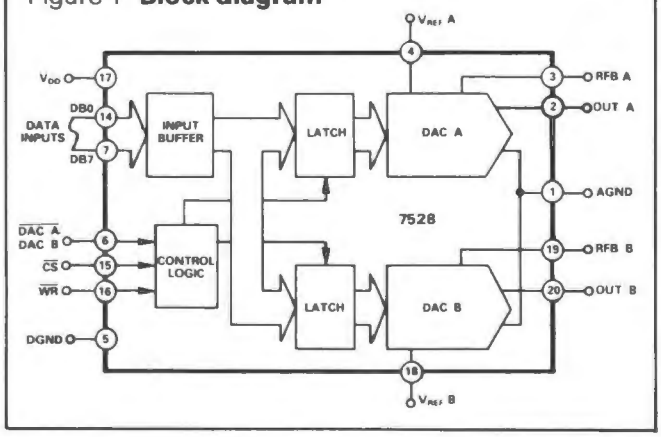
- +5 to +15V operation
- Converters matched to 1%
- TTL and CMOS compatible
- On chip data latches
- Four quadrant multiplication



CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Figure 1 **Block diagram**



Electrical characteristics V_{DD} = +5V, V_{REF} A = V_{REF} B = +10V, Output A = Output B = 0V. T_A = 25°C unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
Supply voltage		5		15	V
Supply current	Digital inputs = V_{INH} or V_{INL}			1	mA
Resolution			8		Bits
Relative accuracy				±½	LSB
Differential nonlinearity				±1	LSB
Gain error	DAC latches 11111111			±2	LSB
Gain temp. coefficient				±0.007	%/°C
Output leakage current	DAC latches 00000000			±50	nA
Input resistance V_{REF}A and V_{REF} B		8	11	15	kΩ
V_{REF} A/V_{REF} B input R match				±1	%
Digital inputs					
Input high voltage		2.4			V
Input low voltage				0.8	V
Input current	V_{IN} = 0V or V_{DD}		±1	±1000	nA
Input capacitance	pins 6 through 16			30	pF

AC characteristics T_A = +25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Chip select to write set up time	t_{CS}	V_{DD} = +5V	200			ns
		V_{DD} = +15V	60			ns
Chip select to write hold time	t_{CH}	V_{DD} = +5V	10			ns
		V_{DD} = +15V	20			ns
DAC select to write set up time	t_{AS}	V_{DD} = +5V	200			ns
		V_{DD} = +15V	60			ns
DAC select to write hold time	t_{AH}	V_{DD} = +5V	10			ns
		V_{DD} = +15V	20			ns
Data valid to write set up time	t_{DS}	V_{DD} = +5V	30			ns
		V_{DD} = +15V	110			ns
Data valid to write hold time	t_{DH}	V_{DD} = +5V	0			ns
		V_{DD} = +15V	0			ns
Write pulse width	t_{WR}	V_{DD} = +5V	60			ns
		V_{DD} = +15V	180			ns
DC supply rejection Δ gain/Δ V_{DD}		V_{DD} = ±5%			0.02	% per %
Propagation delay		V_{DD} = +5V	220			ns
		V_{DD} = +15V	80			ns
Glitch energy for code transition all 0'S to all 1'S		V_{DD} = +5V		160		nVsec
		V_{DD} = +15V		440		nVsec
Output capacitance A & B	C_{out}	DAC latches 00000000			50	pF
Output capacitance A & B	C_{out}	DAC latches 11111111			120	pF
AC feed through V_{REF} to output		V_{REF} = 20V p.p. Sine Wave			−70	dB
Channel to channel isolation				−77		dB
Digital cross talk						
V_{DD} = +5V		00000000 to		30		nVsec
V_{DD} = + 15V		11111111 transition		60		nVsec
Harmonic distortion		V_{IN} = 6V_{rms} 1KH_z		−85		db

Operation information

Converter selection

Both converters share a common 8-bit input port and the control input $\overline{DACA}$/DACB selects which converter accepts data from the input port see table 1.

Mode selection

The $\overline{CS}$ and $\overline{WR}$ control inputs select the operating mode of the selected converter see table 1.

Write mode

When $\overline{CS}$ and $\overline{WR}$ are both low the selected converter is in the write mode. The input data latches of this converter are transparent and its analogue output responds to the digital data on DB0 to DB7.

Hold mode

The selected converter latch retains the data which was present on DB0 to DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analogue outputs remain at the values corresponding to the data in their respective latches.

Figure 2 **Write cycle timing diagram**

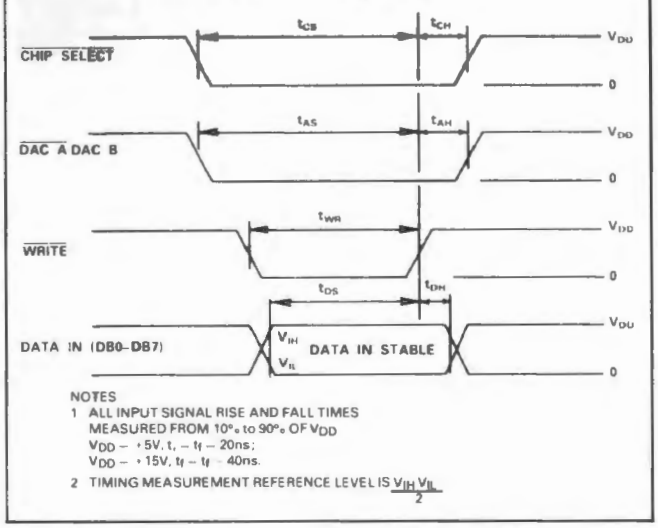


Table 1 **Mode selection**

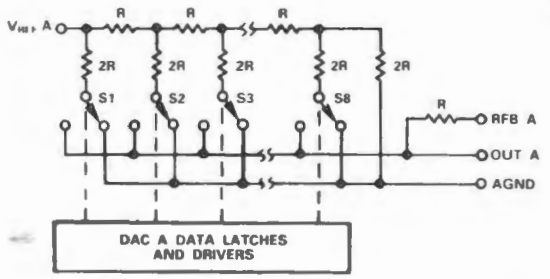
$\overline{DACA}$/ DAC B	$\overline{CS}$	$\overline{WR}$	DACA	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Circuit information

The 7528 contains two identical 8-bit multiplying D to A converters DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D to A converter circuit for DAC A can be seen in Figure 3. An inverted R-2R ladder structure is used i.e. binary weighted currents are switched between the DAC output and analogue ground thus maintaining fixed currents in each ladder leg independent of switch state.

Figure 3 **Simplified functional circuit for DAC A**

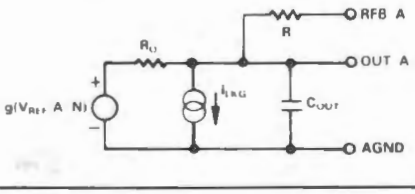


Equivalent circuit

Figure 4 shows an approximate equivalent circuit for one of the converters, note analogue ground is common for both DAC A and DAC B.

The leakage current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices approximately doubles every 10°C. The resistor R_0 as shown in figure 4 is the equivalent output resistance of the device which varies with input code from 0.8R to 2R. R is typically 11K. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50pF to 120pF depending upon the digital input. (g V_{REF} A, N) is the equivalent Thevenin voltage generator due to the reference input voltage V_{REF}A and the transfer function of the R-2R ladder.

Figure 4 **Equivalent analogue output circuit of DACA**

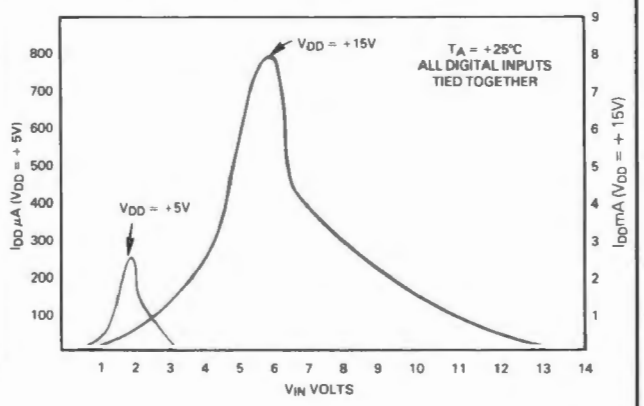


Digital circuitry

The input buffers are CMOS inverters designed so that when the 7528 is operated with V_{DD} = 5V, the buffer converts the TTL input levels (of 2.4 and 0.8V) into CMOS logic levels for the rest of the converter. When V_{IN} is in the region of 2.0 volts to 3.5 volts the buffers operate in their linear region and pass a quiescent current see Figure 5. To minimise power supply currents it is recommended that the digital inputs be as close to the supply rails V_{DD} and digital GND as is possible.

The 7528 may be operated with any supply voltage in the range 5V≤ V_{DD} ≤15V. With V_{DD} = +15V the input logic levels are CMOS compatible only i.e. 1.5V and 13.5V.

Figure 5 **Digital input current vs. input voltage**



Applications information

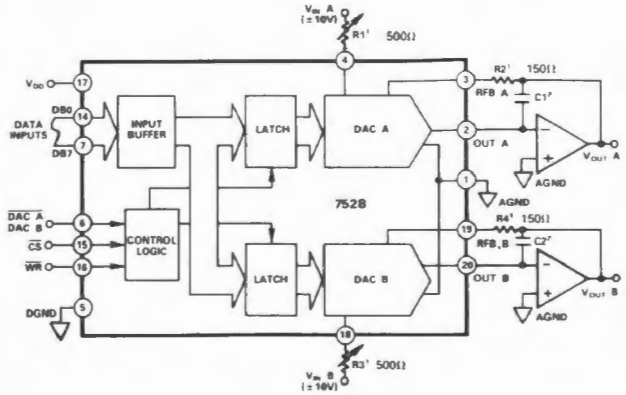
In order to achieve system performance consistent with the device specifications careful attention must be given to the following:

1. Ground Management. AC or transient voltages between Analogue and Digital ground pins can cause noise injection into the analogue output. The simplest cure is to tie analogue and digital ground together at the 7528 pins. In more complex systems where the analogue and digital ground intertie is on the backplane, it is recommended that diodes be connected in inverse parallel between the 7528 analogue and digital ground pins. (IN 4148 or equivalent.)
2. Output Amplifier Offset. CMOS digital to analogue converters exhibit a code-dependent output resistance which in turn causes a code dependent noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output of maximum magnitude $0.67V_{OS}$ (V_{OS} is the amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To obtain monotonic operation it is recommended that the amplifier V_{OS} be no greater than 10% of 1LSB over the temperature range of interest.
3. High Frequency Considerations. The output capacitance of a CMOS converter works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation, but can suitably be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

Dynamic performance

The overall dynamic performance of the two digital to analogue converters in the 7528 will depend upon the gain and phase characteristics of the output amplifiers together with the optimum choice of printed circuit layout and decoupling components. Figure 8 shows the relationship between input frequency and channel to channel isolation.

Figure 6 **Dual DAC unipolar binary operation (2 quadrant multiplication). See Table 2.**



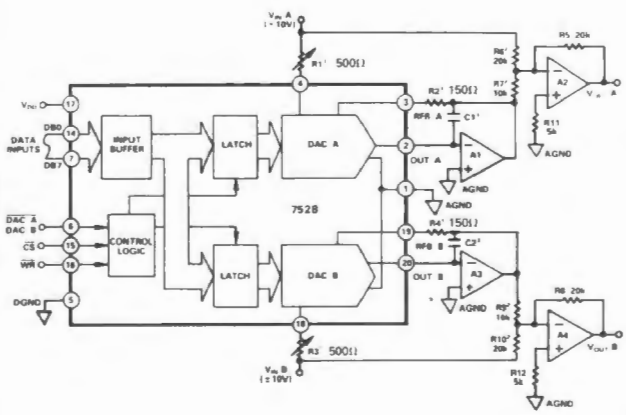
NOTES.
[1]R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
[2]C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

Table 2 **Unipolar Binary Code Table**

DAC Latch Contents MSB LSB	Analogue Output (DAC A or DAC B)
1 1 1 1 1 1 1 1	$-V_{IN}\left\{\frac{255}{256}\right\}$
1 0 0 0 0 0 0 1	$-V_{IN}\left\{\frac{129}{256}\right\}$
1 0 0 0 0 0 0 0	$-V_{IN}\left\{\frac{128}{256}\right\} = -\frac{V_{IN}}{2}$
0 1 1 1 1 1 1 1	$-V_{IN}\left\{\frac{127}{256}\right\}$
0 0 0 0 0 0 0 1	$-V_{IN}\left\{\frac{1}{256}\right\}$
0 0 0 0 0 0 0 0	$-V_{IN}\left\{\frac{0}{256}\right\} = 0$

Note: $1LSB = (2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$

Figure 7 **Dual DAC bipolar operation (4 quadrant multiplication). See Table 3.**



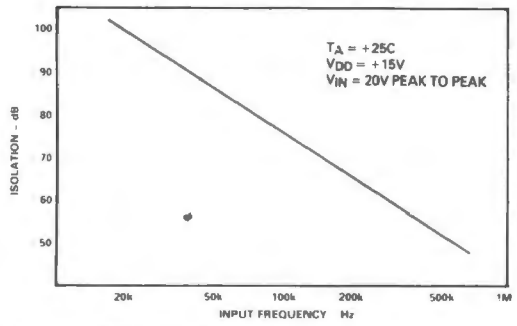
NOTES
[1]R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
ADJUST R1 FOR V_{OUT} A = 0V WITH CODE 10000000 IN DAC A LATCH
ADJUST R3 FOR V_{OUT} B = 0V WITH CODE 10000000 IN DAC B LATCH.
[2]MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10
[3]C1, C2 PHASE COMPENSATION (10pF–15pF) MAY BY REQUIRED IF A1/A3 IS A HIGH-SPEED AMPLIFIER

Table 3 **Bipolar (Offset Binary) Code Table**

DAC Latch Contents MSB LSB	Analogue Output (DAC A or DAC B)
11111111	$+ V_{IN}\{\frac{127}{128}\}$
10000001	$+ V_{IN}\{\frac{1}{128}\}$
10000000	0
01111111	$- V_{IN}\{\frac{1}{128}\}$
00000001	$- V_{IN}\{\frac{127}{128}\}$
00000000	$- V_{IN}\{\frac{128}{128}\}$

Note: $1LSB = (2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

Figure 8 **Channel to channel isolation**

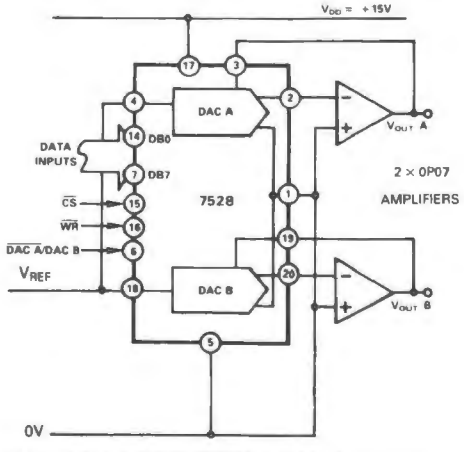


Single supply applications

The 7528 DAC R-2R ladder termination resistors are connected to analogue ground within the device. This arrangement is convenient for single supply operation because analogue ground may be biased at any voltage between Digital ground and V_{DD}.

In the circuit of figure 12 the 7528 is used to implement a programmable window comparator. DACs A and B are loaded with the upper and lower voltage limits required respectively. If the test input is outside the set limits the pass/fail output will go low indicating a fail condition.

Figure 9 **7528 single supply operation**



Microprocessor interfaces

Figure 10 **7528 dual DAC to 6800 CPU interface**

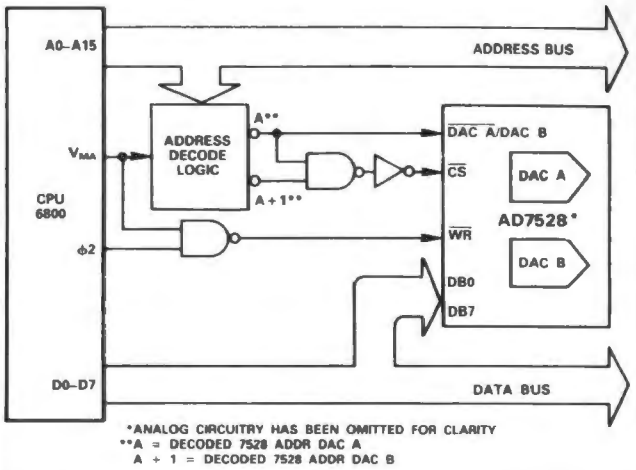
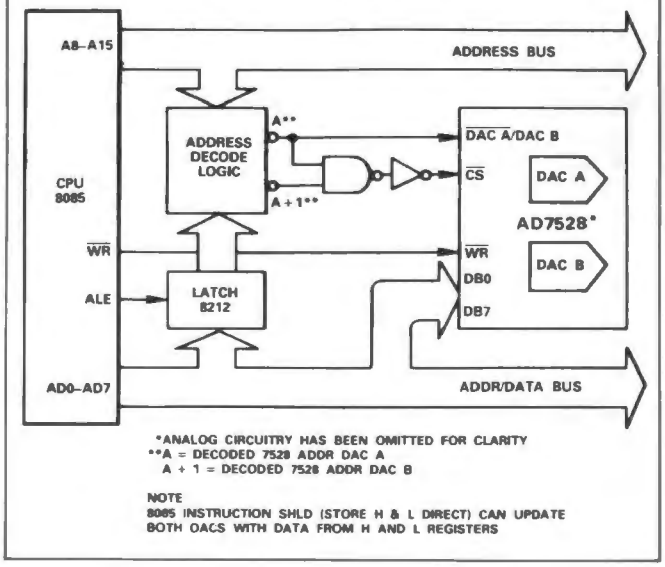
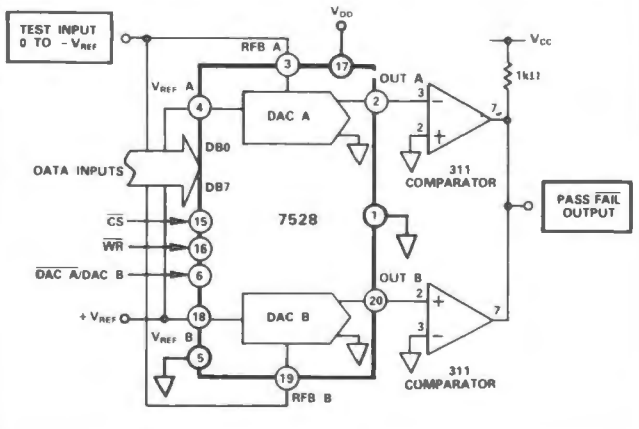


Figure 11 **7528 dual DAC to 8085 CPU interface**



Programmable window comparator

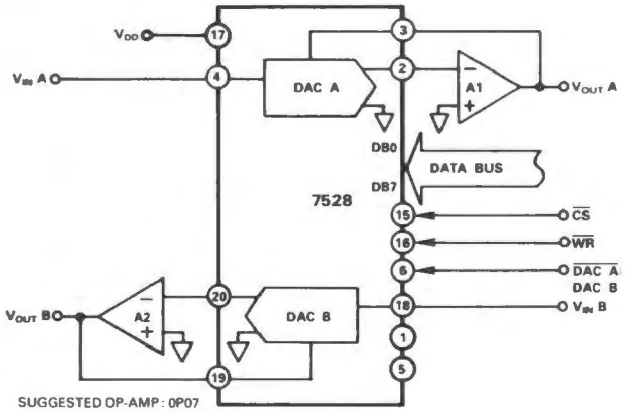
Figure 12 **Digitally programmable window comparator (upper and lower limit detector)**



RS data

Digitally controlled dual attenuator

Figure 13 **Digitally controlled dual attenuator**



In this configuration the 7528 functions as a 2-channel digitally controlled attenuator. Ideal for stereo audio and telephone signal level control applications. Table 4 gives input codes vs. attenuation for a 0 to 15.5dB range.

$$\text{Input code} = 256 \times 10 \exp \left\{ -\frac{\text{Attenuation, dB}}{20} \right\}$$

Table 4 **Attentuation vs. DAC A, DAC B Code for the Circuit of Figure 13.**

Attn. dB	DAC Input Code	Code in Decimal	Attn. dB	DAC Input Code	Code in Decimal
0	1 1 1 1 1 1 1 1	255	8.0	0 1 1 0 0 1 1 0	102
0.5	1 1 1 1 0 0 1 0	242	8.5	0 1 1 0 0 0 0 0	96
1.0	1 1 1 0 0 1 0 0	228	9.0	0 1 0 1 1 0 1 1	91
1.5	1 1 0 1 0 1 1 1	215	9.5	0 1 0 1 0 1 1 0	86
2.0	1 1 0 0 1 0 1 1	203	10.0	0 1 0 1 0 0 0 1	81
2.5	1 1 0 0 0 0 0 0	192	10.5	0 1 0 0 1 1 0 0	76
3.0	1 0 1 1 0 1 0 1	181	11.0	0 1 0 0 1 0 0 0	72
3.5	1 0 1 0 1 0 1 1	171	11.5	0 1 0 0 0 1 0 0	68
4.0	1 0 1 0 0 0 1 0	162	12.0	0 1 0 0 0 0 0 0	64
4.5	1 0 0 1 1 0 0 0	152	12.5	0 0 1 1 1 1 0 1	61
5.0	1 0 0 1 0 0 0 0	144	13.0	0 0 1 1 1 0 0 1	57
5.5	1 0 0 0 1 0 0 0	136	13.5	0 0 1 1 0 1 1 0	54
6.0	1 0 0 0 0 0 0 0	128	14.0	0 0 1 1 0 0 1 1	51
6.5	0 1 1 1 1 0 0 1	121	14.5	0 0 1 1 0 0 0 0	48
7.0	0 1 1 1 0 0 1 0	114	15.0	0 0 1 0 1 1 1 0	46
7.5	0 1 1 0 1 1 0 0	108	15.5	0 0 1 0 1 0 1 1	43

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RS data

12-bit D to A converter i.c. 7545

Stock number 301-886

Introduction

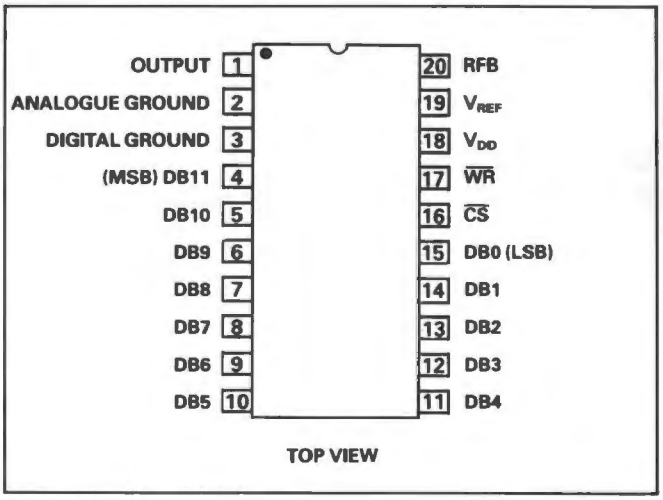
The 7545 is a monolithic 12-bit CMOS multiplying digital to analogue converter incorporating internal data latches. It is loaded by a single 12-bit wide data word and interfaces directly to most bus systems. Under normal operation data is loaded using the $\overline{CS}$ and $\overline{WR}$ control signals alternatively these may be tied low allowing direct unbuffed operation. The 7545 is ideal for use in single supply or battery operated applications with its low power consumption.

Absolute maximum ratings

V_{DD} to digital ground ——— −0.3V to +17V
Digital input voltage
to digital ground ——— −0.3V to V_{DD}
V_{RFB} and V_{REF} to digital ground ——— ±25V
Voltage on pins 1 and 2
to digital ground ——— −0.3V to V_{DD}
Power dissipation ——— 450mW
Operation temperature range ——— 0°C to +70°C
Storage temperature range ——— −65°C to +150°C
Lead temperature IOS soldering ——— +300°C

Features

- 12-bit resolution.
- Low gain temperature coefficient.
- Fast TTL compatible data latches.
- Single +5V to +15V supply operation.
- Compact 20-pin DIL package.
- Ideal for battery operation.



TOP VIEW

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Electrical characteristics

V_{DD} = +5V, V_{REF} = +10V, V_{OUTPUT} = 0V, Analogue Ground = Digital Ground, T_A = +25°C.

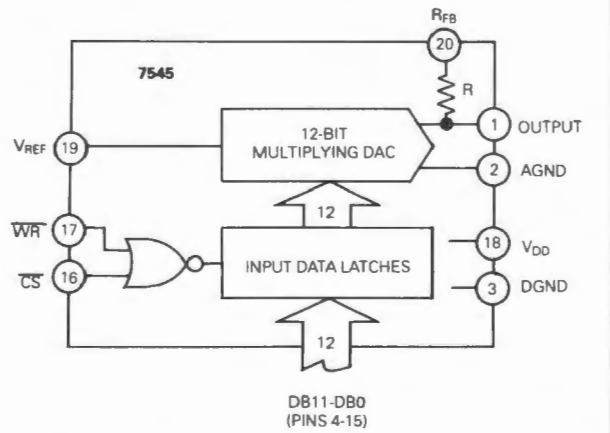
Parameter	Conditions	Min.	Typ.	Max.	Units
Supply voltage		5		15	V
Supply current	Digital inputs = V_{INH} or V_{INL}			2	mA
	Digital inputs = 0V or V_{DD}		10	100	μA
Resolution			12		Bits
Relative accuracy				±1	LSB
Differential nonlinearity	12-bit monotonic T_{MIN} to T_{MAX}			±1	LSB
Gain error (internal RFB)	DAC register 1111 1111 1111			±10	LSB
Gain temperature coefficient	Δ Gain/Δ Temperature		±2	±5	ppm/°C
DC supply rejection	Δ V_{DD} = ±5%			0.015	% per %
Output leakage current OUTPUT	DB0-DB11 = 0V $\overline{WR}$ & $\overline{CS}$ = 0V			10	nA
Reference input resistance	Temperature coefficient = −300ppm/°C max.	7	11	25	kΩ
Output capacitance OUTPUT	DB0-DB11 = 0V, $\overline{WR}$ & $\overline{CS}$ = 0V			70	pF
Output capacitance OUTPUT	DB0-DB11 = V_{DD}, $\overline{WR}$ & $\overline{CS}$ = 0V			200	pF
Input high voltage V_{IH}		2.4			V
Input low voltage V_{IL}				0.8	V
Input current I_{IN}	V_{IN} = 0V or V_{DD}			±1	μA
Input capacitance DB0-DB11	V_{IN} = 0V			5	pF
Input capacitance $\overline{WR}$ and $\overline{CS}$	V_{IN} = 0V			20	pF

Dynamic characteristics

V_{DD} = +5V, V_{REF} = +10V, V_{OUTPUT} = 0V, Analogue Ground = Digital Ground T_A = +25°C

Parameter	Conditions	Min.	Typ.	Max.	Units
Propagation delay (from input change to 90% analogue O/P)	Output load = 100Ω, C_{EXT} = 13pF			300	ns
Glitch energy	V_{REF} = analogue ground		400		nVs
AC feed through at output	V_{REF} = ±10V, 10kHz sinewave		5		mVp-p
Chip select to write setup time t_{CS}		280	200		ns
Chip select to write hold time t_{CH}		0			ns
Write pulse width t_{WR}	$t_{CS} \geq t_{WR} \geq 0$	250	175		ns
Data setup time t_{DS}		140	100		ns
Data hold time t_{DH}		10			ns

Figure 1 **7545 Functional diagram**



Circuit information

Converter section:

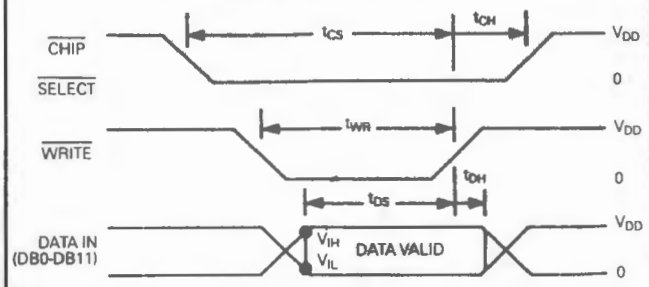
Figure 3 shows a simplified circuit of the digital to analogue converter used in the 7545 and Figure 4 gives the approximate equivalent circuit. Note that the ladder termination resistor is connected to analogue ground and R is typically 11k.

The binary weighted currents are switched between the output bus line and analogue ground by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the output bus line C_{OUT}, is code dependent and varies from 70pF (all switches connected to analogue ground) to 200pF (all switches to output).

A current switch can be seen in Figure 4. The input resistance at V_{REF} figure 3 is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value 'R'). Since R_{IN} at the V_{REF} pin is constant the reference terminal can be driven by a reference voltage or a reference current a.c. or d.c. of positive or negative polarity. If a current source is used a low temperature coefficient external R_{FB} is recommended to define the scale factor.

Figure 2 **Write cycle timing diagram**



MODE SELECTION

WRITE MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0-DB11) inputs.

HOLD MODE:
Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:

$V_{DD} = +15V$; $t_r = t_f = 20ns$

$V_{DD} = +15V$; $t_r = t_f = 40ns$

All input signal rise and fall times measured from 10% to 90% of V_{DD}.

Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$

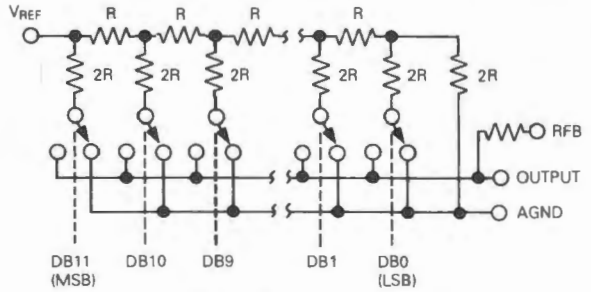


Figure 3 **Simplified D/A circuit of 7545**

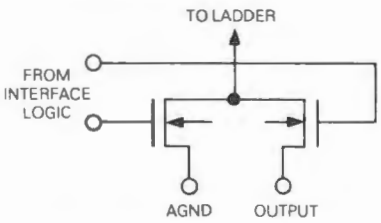


Figure 4 **N-channel current steering switch**

Digital section:

Figure 5 shows the digital input structure for 1 bit. The digital control signals are generated internally from $\overline{CS}$ and $\overline{WR}$.

The input buffers are simple CMOS inverters designed to convert TTL input levels (2.4V and 0.8V) into CMOS logic levels when operated on a 5V supply.

When V_{IN} is in the region of 2.0V to 3.5V the input buffers operate in their linear region and draw current from the power supply. To minimise power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and digital ground) as is practically possible. The 7545 may be operated with any supply voltage in the range $5V < V_{DD} < +15V$. With $V_{DD} = +15V$ the input logic levels are CMOS compatible only (i.e. 1.5V and 13.5V).

Circuit Information

Digital section:

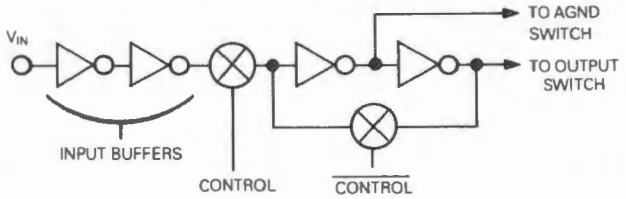


Figure 5 **Digital input structure**

Applications

Figures 6 and 7 show simple unipolar and bipolar circuits, resistor R, is used to trim for full scale. In many applications it should be possible to dispense with gain trim resistors altogether. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing of high speed op-amps. Note all the circuits in Figures 6, 7 and 8 have constant input impedances at the V_{REF} input.

The circuit shown in Figure 6 can either be used as a fixed reference digital to analogue converter so that it provides an analogue output voltage in the range 0 to $-V_{IN}$ (the inversion is introduced by the output op-amp). Or V_{IN} can be an a.c. signal when the circuit behaves as an attenuator (2-quadrant multiplier). V_{IN} can be any voltage in the range $-20 < V_{IN} < +20V$ (provided the op-amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table 1 shows the code relationship for the circuit of Figure 6.

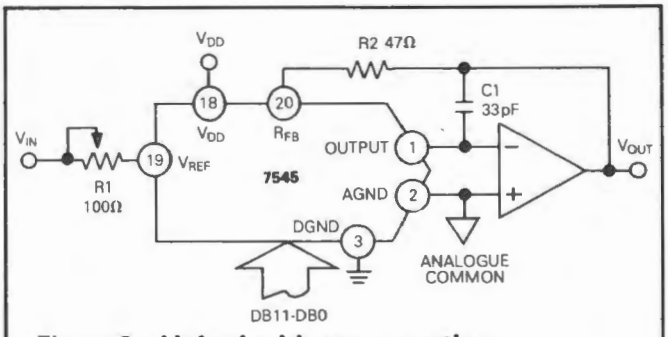


Figure 6 **Unipolar binary operation**

Binary number in DAC register			Analogue output
1111	1111	1111	$-V_{IN} \bullet \left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN} \bullet \left\{\frac{2048}{4096}\right\} = -1/2V_{IN}$
0000	0000	0001	$-V_{IN} \bullet \left\{\frac{1}{4096}\right\}$
0000	0000	0000	0 Volts

Table 1 **Unipolar binary code table for circuit of Figure 6**

A circuit for bipolar operation is shown in Figure 7 with the appropriate codes in Table 2. The digital to analogue function itself uses offset binary code and inverter U, on the MSB line converts the 2s

complement input code to offset binary. If required the inversion function may be performed in software with an exclusive OR instruction. R_3, R_4 and R_5 must be selected to match within 0.01% and should be the same type of resistor so that their temperature coefficients match. Mismatch of R_3 to R_4 causes both offset and full scale error, mismatch of R_5 to R_4 and R_3 causes full scale error.

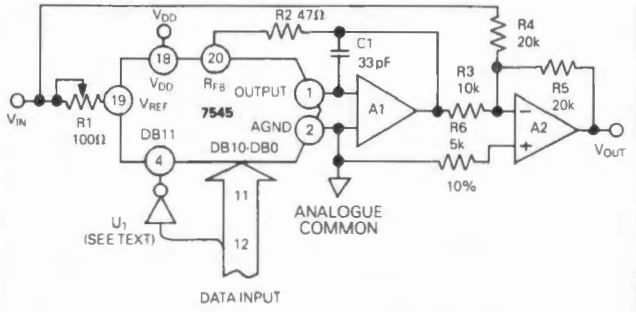


Figure 7 **Bipolar operation (2's complement code)**

Data input			Analogue output
0111	1111	1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

Table 2 **2's complement code table for circuit of Figure 7**

Figure 8 shows an alternative method of achieving a bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for the circuit in Figure 7. The 7592 acts as a change-over switch, R_4 and R_5 should match each other to 0.01% to maintain the overall accuracy. Mismatch between R_4 and R_5 introduces a gain error.

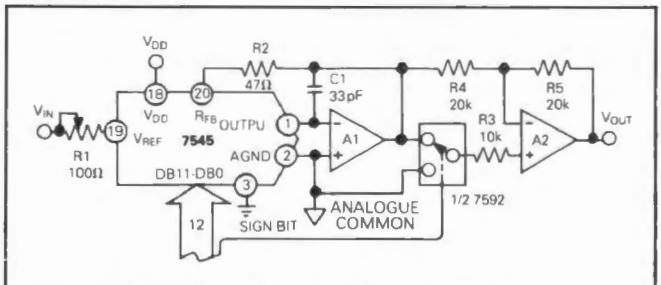


Figure 8 **12-Bit plus sign magnitude D/A converter**

Sign bit	Binary numbers in DAC register			Analogue output
0	1111	1111	1111	$+V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$
0	0000	0000	0000	0 Volts
1	0000	0000	0000	0 Volts
1	1111	1111	1111	$-V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$

Note: Sign bit of '0' connects R3 to GND.

Table 3 **12-Bit plus sign magnitude code table for circuit of Figure 6**

Application notes

Output offset:

CMOS digital to analogue converters exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output amplifier. The maximum amplitude of this offset, which adds to the converter nonlinearity is $0.67V_{OS}$ where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} to be no greater than (25×10^{-6}) V_{REF} over the required temperature range. A suitable op-amp for use with the 7545 is the OP07 and in most applications will not require offset trim.

General ground management:

A.C. or transient voltages between analogue and digital ground can cause noise injection into the analogue output. The simplest method of stopping this is to tie analogue ground to digital ground at the 7545 pins. In more complex systems where the analogue and digital ground intertie is on the backplane and is recommended that two diodes (IN4148 or equivalent) be connected in inverse parallel between the 7545 analogue and digital ground pins.

Digital glitches:

With $\overline{WR}$ and $\overline{CS}$ both low the input latches are transparent and the converter inputs follow the data inputs. In some bus systems data is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output. The solution is to retime the write pulse $\overline{WR}$ so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the output and analogue ground pins. This can be minimised by screening the analogue pins (1, 2, 19 and 20) from the digital pins by a ground track run between pins 2 and 3 and 18 and 19 of the 7545. The analogue pins are at one end of the package and separated from the digital functions by V_{DD} and digital ground to aid screening. On-chip capacitive coupling can also give rise to crosstalk particularly in circuits with high currents and fast rise/fall times. This can be minimised by using $V_{DD} = +5V$ but it should be free from digitally induced noise.

Temperature coefficients:

A maximum value of 5ppm/°C and 2ppm/°C typical will be present. This corresponds to worst case gain shifts of 2 LSBs and 0.8 LSB respectively over a 100°C range. When trim resistors R_1 and R_2

are used to adjust full scale range their temperature coefficients should also be taken into account.

Single supply operation

The ladder termination resistor is connected to analogue ground. This arrangement is particularly suited for single supply operation as the output and analogue ground may be biased at any voltage between digital ground and V_{DD}. The output terminal and analogue ground should never go more than 0.3 volts less than digital ground as damage will occur. The 7545 is protected from latchup phenomenon present in many CMOS devices.

Figure 9 shows the 7545 connected in a voltage switching mode. The output is connected to the reference voltage and analogue ground is connected to digital ground. The converter output voltage is available at the V_{REF} pin and has a constant output impedance equal to R. R_{FB} is not used in the circuit.

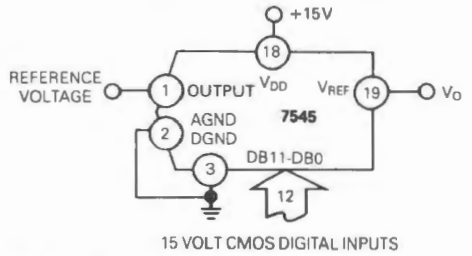


Figure 9 **Single supply operation using voltage switching mode**

The loading on the reference voltage source is code dependent and the response time of the circuit is often set by the behaviour of the reference voltage with changing load conditions. To maintain linearity the voltages at the output and analogue ground should remain within 2.5V of each other for a V_{DD} of 15V. If V_{DD} is reduced or the differential voltage between the output and analogue ground is increased to more than 2.5V the differential nonlinearity of the converter will increase and the linearity degraded. Figures 10 and 11 show typical curves illustrating this effect for different supply and reference voltages. If the output voltage is required to be offset from ground by some value, then the output and analogue ground may be biased up to the required value. The effect on linearity and differential nonlinearity is the same as reducing V_{DD} by the amount of offset. The circuits of figures 6, 7 and 8 can all be converted to single supply operating by biasing analogue ground to some voltage between V_{DD} and digital ground.

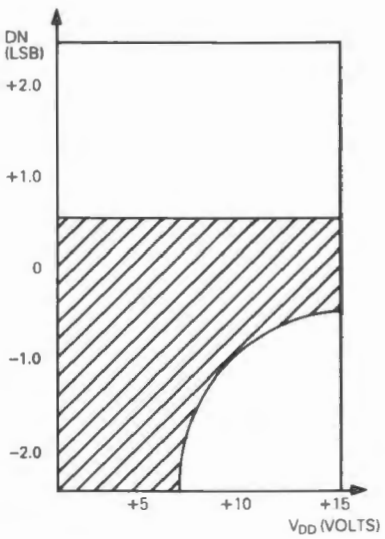


Figure 10 **Differential nonlinearity vs. V_{DD} for Figure 9 circuit. Reference voltage = 2.5V. Shaded area shows range of values of differential nonlinearity that typically occur.**

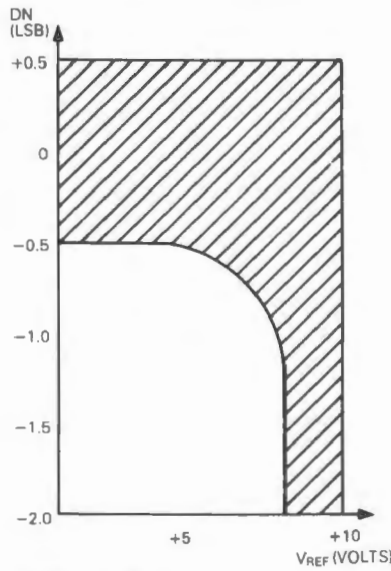


Figure 11 **Differential nonlinearity vs. V_{REF} for Figure 9 circuit. V_{DD} = 15V. Shaded area shows range of values of differential nonlinearity that typically occur.**

Microprocessor interface

The 7545 can interface directly with both 8 and 16-bit microprocessors via its 12-bit-wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown in Figure 12. This uses two memory addresses one for the lower 8-bits of data to the converter and the other for the upper 4-bits via the latch.

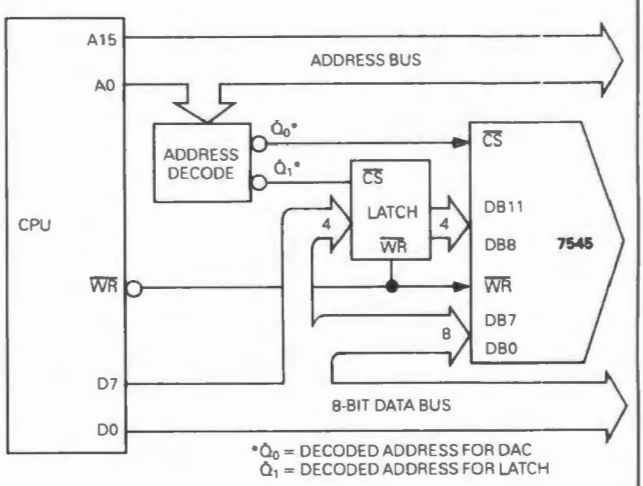


Figure 12 **8-Bit processor to 7545 interface**

Figure 13 shows an alternative circuit for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080 and Z80. This technique uses the 12 lower address lines of the processor address bus to supply data to the converter, thus each 7545 connected in this way uses 4K bytes of address locations. Data is written into the converter using a single memory write instruction. The address field of the instruction is organised so that the lower 12-bits contain the data for the converter and the upper 4-bits contain the address of the 4K block at which the converter resides.

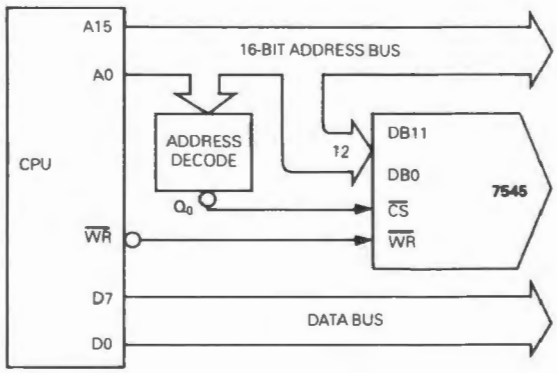


Figure 13 **Connecting the 7545 to 8-bit processors via the address bus**

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RS data

B.T. Telephone type connection system

The comprehensive range of RS connectors and accessories is suitable for the connection of flexible cordage to a wide range of electronic equipment. The range is manufactured to B.T. Spec. D2902, D2931 and CW1311.

Note: British Telecommunications require of any person who connects subscriber's apparatus directly or indirectly to any telecommunication system that it runs to comply with the terms and conditions relating to the attachment of subscriber's apparatus under which service is provided by BT.

Features

- Suitable for:
  - Telephone systems
  - Audio/PA systems
  - Alarms and security systems
  - Computer interface/peripheral equipment.
- Easy to install, service or replace.
- Simple system expansion.
- System expansion by the addition of ancillary equipment is made easy.
- Gives working 'snatch out' facility to ensure safety.
- Plug and socket polarisation prevents incorrect connections.

Performance data

Mechanical	
Durability	1000 engagements min. or 50 engagements min. switching current
Snatch out facility and still retain	10 times
Plug retention in jack	50N
Engagement force	2.5N max. per way
Withstand probe of standard test finger BS 3042, test figure 1 also equivalent European standard.	Yes
Electrical	
Working voltage	200V d.c.
Insulation resistance	100 megohms at 500V d.c.
Circuit resistance (Contact plus bulk resistance of contacts and joint resistance of plug to cord and 75mm of cord)	100 milliohms initial plus 20 milliohms after conditioning
Current rating	250mA d.c. per contact
Environmental climatic	
Dry heat	250 hours at 55°C
Damp heat	10 days
Thermal shock	5 cycles +55°C to −10°C
Domestic	
Resistant to:	
Isopropanol White spirit 5% Domestic bleach Methylated spirit	5 cycles of 5 minutes
Sprayed with:	
Silicone furniture polish	5 applications
Materials	
Contact	Phosphor bronze
Moulding	Thermoplastic polyester to UL94 V-O Colour natural
Contact plating	Gold to meet above conditions

The RS pluggable telephone system

	Description	Stock No.	Page No.
Plugs	431A 4-way line plug	470-229	3
	430A 4-way handset plug	470-235	3
	631A 6-way line plug	470-241	3
	630A 6-way handset plug	470-257	3
Sockets	601A line socket	470-263	3
	602A handset socket	470-279	3
	603A RA line socket	470-285	4
	605A line jack socket	470-291	4
	Panel mounting bracket	470-308	4
Cordsets	4-way line plug cord set	470-493	5
	6-way line plug cord set	470-140	5
	4-way line cord with tags	470-156	5
	6-way line cord with tags	470-162	5
	4-way curly handset cord	470-178	5
Adaptors	6-way plug-screw adaptor	470-314	6
	4-way plug screw adaptor	470-320	6
	LJU10/3A dual outlet	470-336	6
	LJU10/7A break in adaptor	470-342	7
	Extension lead 3m	472-051	7
	Extension lead 6m	472-067	7
	Extension lead 10m	472-073	7
Wall Boxes	**Master**		
	LJU1/1A IDC	472-506	7
	LJU1/1A Screw	472-512	7
	LJU2/1A IDC	472-528	8
	LJU2/1A Screw	472-534	8
	LJU3/1A IDC	472-540	8
	LJU3/1A Screw	472-556	8
	LJU4/1A IDC	472-562	8
	LJU4/1A Screw	472-578	8
	LJU5/1A IDC	472-584	8
	LJU5/1A Screw	472-590	8
	Secondary		
	LJU1/3A IDC	470-358	7
	LJU1/6A Screw	470-364	7
	LJU2/3A IDC	470-370	8
	LJU2/6A Screw	470-386	8
	LJU3/3A IDC	470-392	8
	LJU3/6A Screw	470-409	8
	LJU4/3A IDC	470-976	8
	LJU4/6A Screw	470-960	8
	LJU5/3A IDC	470-998	8
	LJU5/6A Screw	470-982	8
Tooling	IDC Handtool (precision)	470-128	9
	Plastic IDC handtool	470-487	9
	Plug handtool	470-134	9
	Line socket test plug 50mm	471-597	9
	Line socket test plug 1m	471-604	9
Cable	4-way line cord	368-025	10
	6-way line cord	368-031	10
Cable clips	4-way cable clips	470-207	10
	4-way cable clips	470-213	10

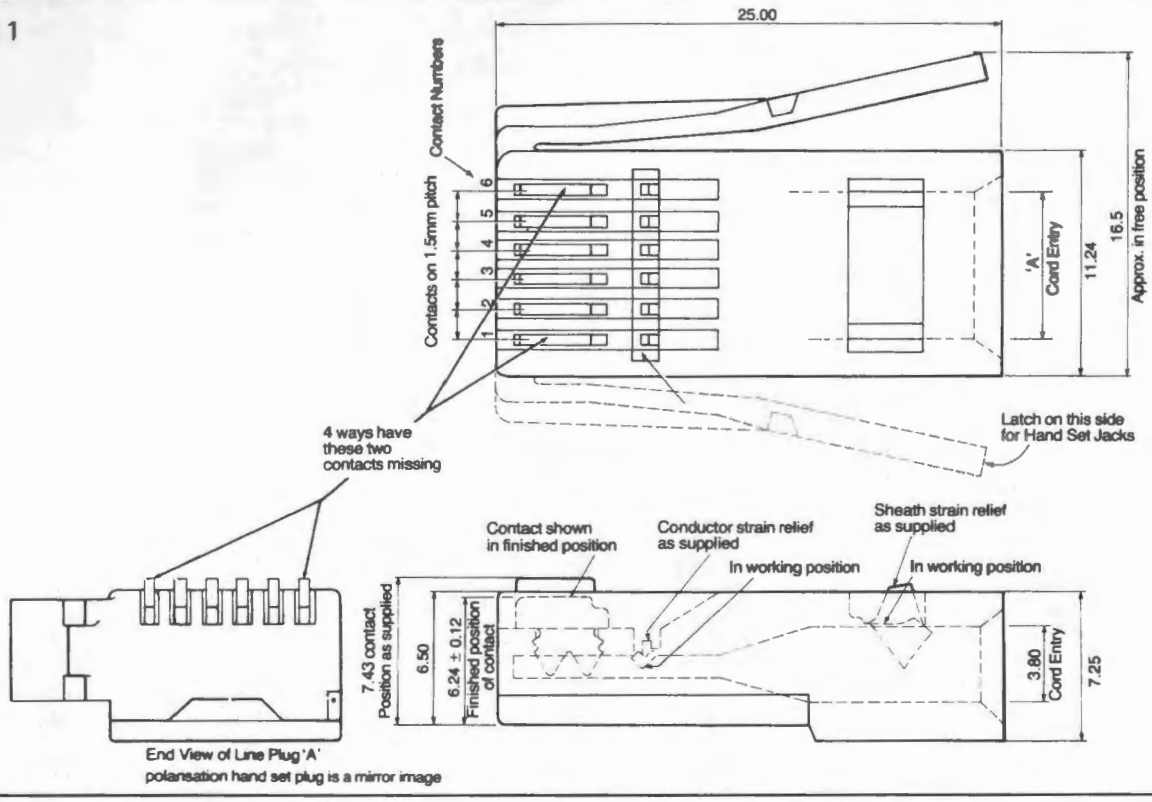
Important: **Line** plugs and sockets are not intermateable with **handset** plugs and sockets.

Plugs with 'A' style polarisation

The RS range of line and handset plugs are designed to fit 'D' shaped cordage (to B.T. specification 1311 types 46CA & CB) using insulation piercing techniques and plastic latch strain reliefs.

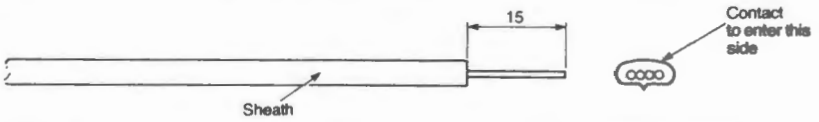
Note: Use RS tool number 470-134 for simultaneous termination of contacts and strain reliefs.

Figure 1



Cord preparation

Figure 2



Sockets with 'A' style polarisation

Straight sockets 470-263 (Line) and 470-279 (Handset)

The RS sockets are designed so that connections can be made into the base of instruments having their PCB on the bottom of the instrument. There are two versions available for both line and handset applications.

Figure 3

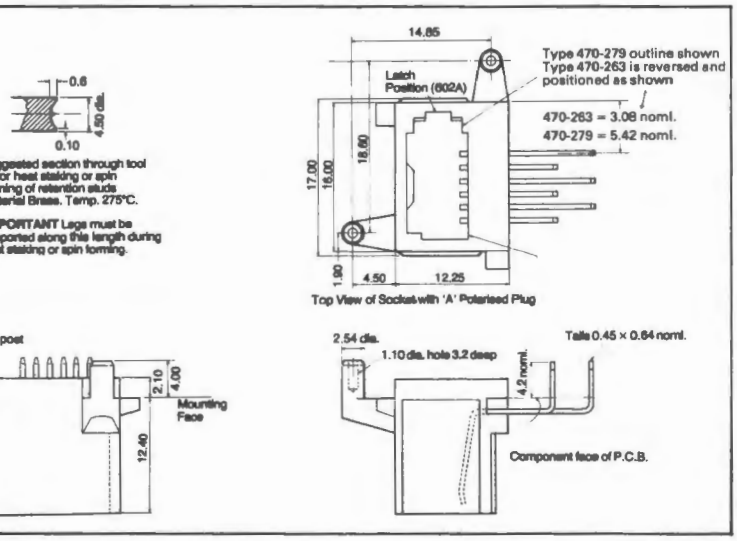
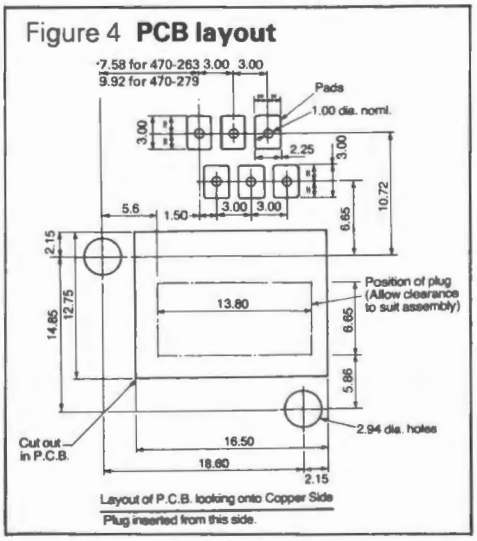


Figure 4 **PCB layout**



Right angle line sockets: 470-285

RS socket 470-285 is designed so that connections can be made to the edge of a PCB and in the same plane. This jack is only available in the line cord version. The socket is useful in equipment with a PCB in the base needing connections to rear, side or front faces. Clips are provided to hold the socket in place while soldering, and the front face has slots for mechanical restraint against snatch out forces.

Figure 5

PCB layout

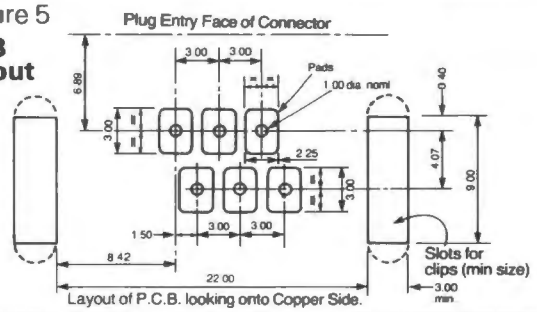
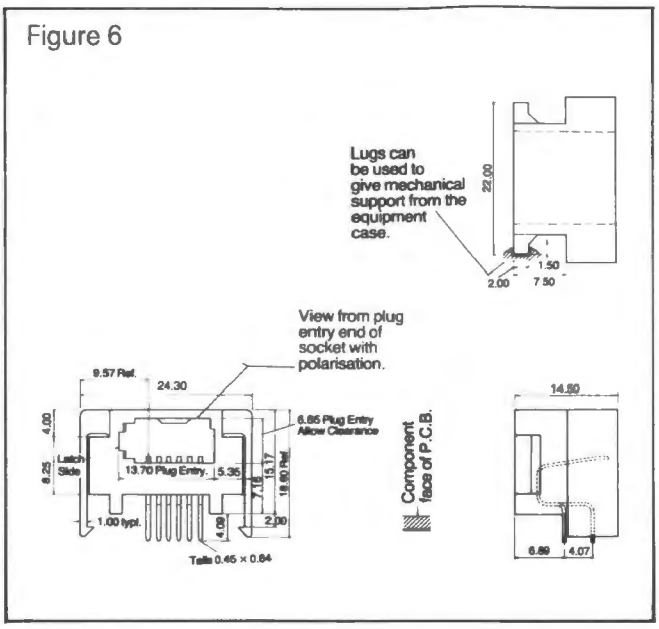


Figure 6



Line jack sockets: 470-291

RS socket 470-291 is designed so that connection can be made to a PCB from the component side. The socket is only available in line cord versions. If full snatch out force is to be applied the socket should be supported on the top face by the equipment shell.

Figure 7

PCB layout

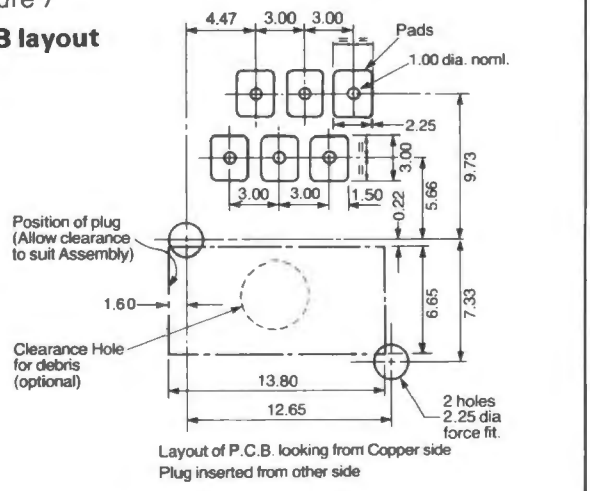
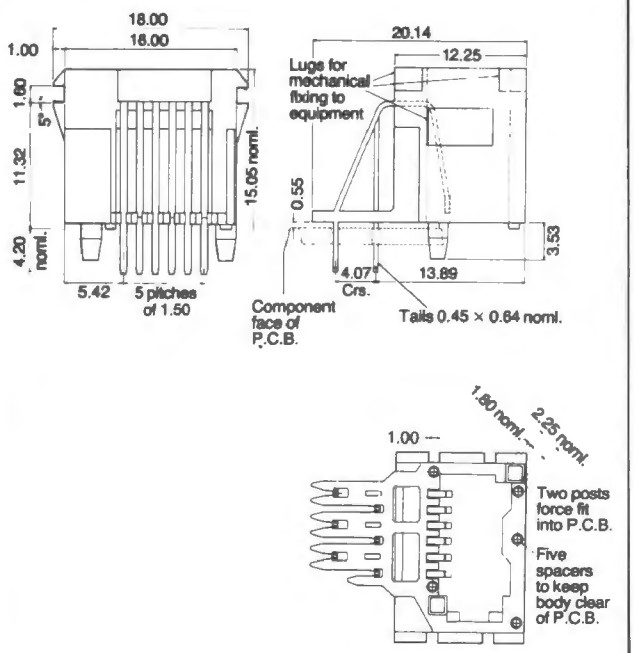


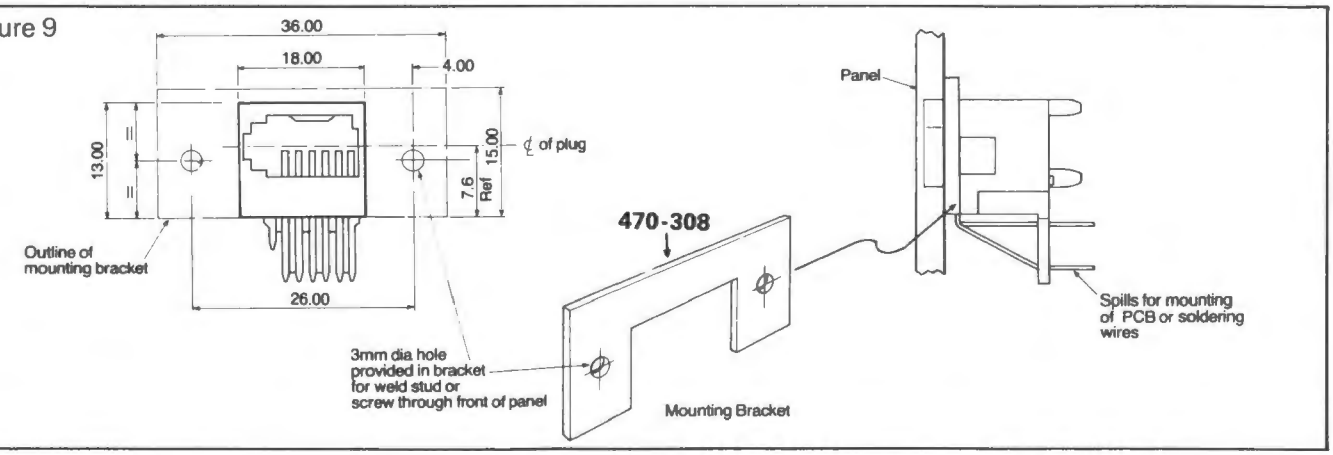
Figure 8



Panel mounting

RS socket 470-291 can be panel mounted using mounting bracket 470-308, fixing is as follows:

Figure 9



Cord sets

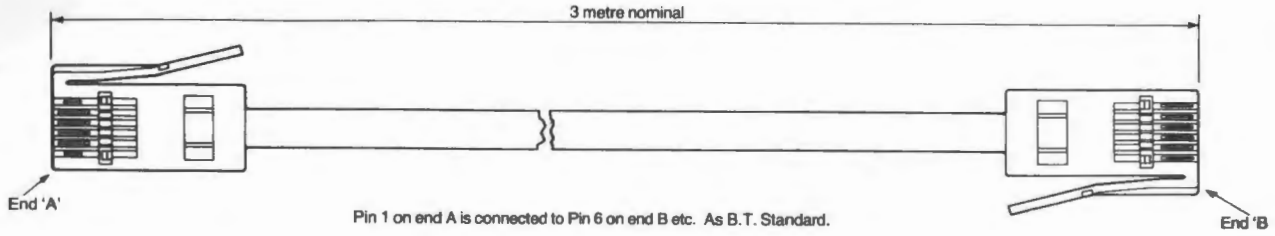
RS Cord sets are available for use when converting existing equipment or designing new equipment.

The cordage used is to B.T. specification CW1311 type 4CA and 6CA in light grey to match the plugs. The conductors are 4 ends Tinsel to give high flexibility and long life. Termination of Tinsel is difficult and purchase of pre-terminated cords avoids these difficulties. The cordage is 'D' shaped with nominal dimensions of 5.5 x 3.5mm for the 4-way and 7.5 x 3.5mm for the 6-way.

Warning: If hazardous voltages are used on double ended line cords, the live end must be fixed under the cover of the equipment or retained by other means. UK Telephone lines must be regarded as hazardous.

RS line cords terminated with plugs both ends

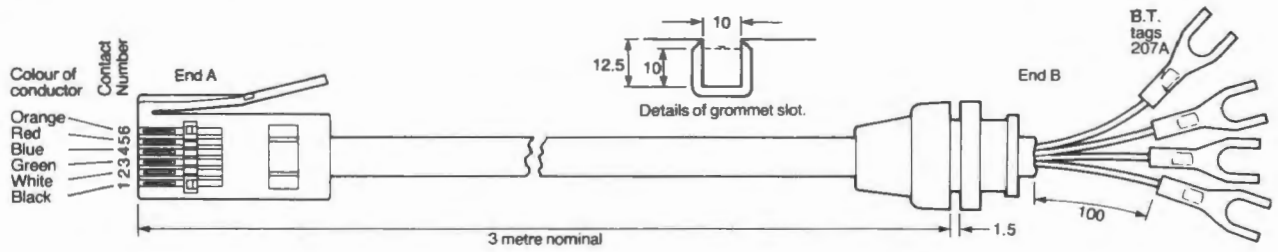
Figure 10



Stock Number	Description	British Telecom No.	End 'A'	End 'B'
470-493	4 way line plug cordset	4/500	431A	431A
470-140	6 way line plug cordset	6/500	631A	631A

RS Line cords terminated with plug one end and spade terminals at the other:

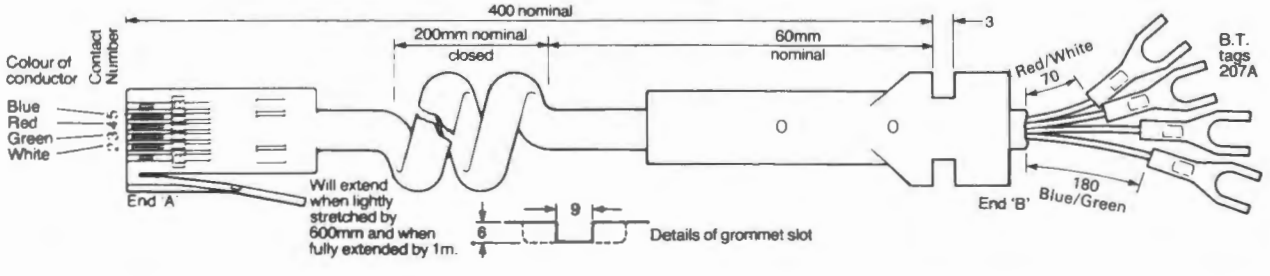
Figure 11



Stock Number	Description	British Telecom No.	End 'A'	End 'B'
470-156	4 way line cord with tags	4/502	431A	Grommet DSL 16 + tags 207A
470-162	6 way line cord with tags	6/502	631A	Grommet DSL 16 + tags 207A

RS Handset cords terminated with handset plug at one end:

Figure 12



Stock Number	Description	British Telecom No.	End 'A'	End 'B'
470-178	4 way curly handset cord	4/503	430A	DSL 44 Grommet + tags 207A

Adaptors

4 and 6-way plug-screw terminal adaptors: 470-320 (4 way) and 470-314 (6 way)

The RS plug can be attached to any equipment wire or cable by the use of a small electrical screwdriver. The terminals are contained in a small box with a lid which is removed using a single screw. The terminals will take a 207A BT tag barrel so that this plug can be attached to existing telephones with round cordage. The plug is supplied with a DSL16 grommet at the cable exit point for neatness and cable protection. This grommet can be removed when used with cords having an attached grommet. A small cable tie is provided with each plug which when applied to the incoming cable inside the box provides strain relief.

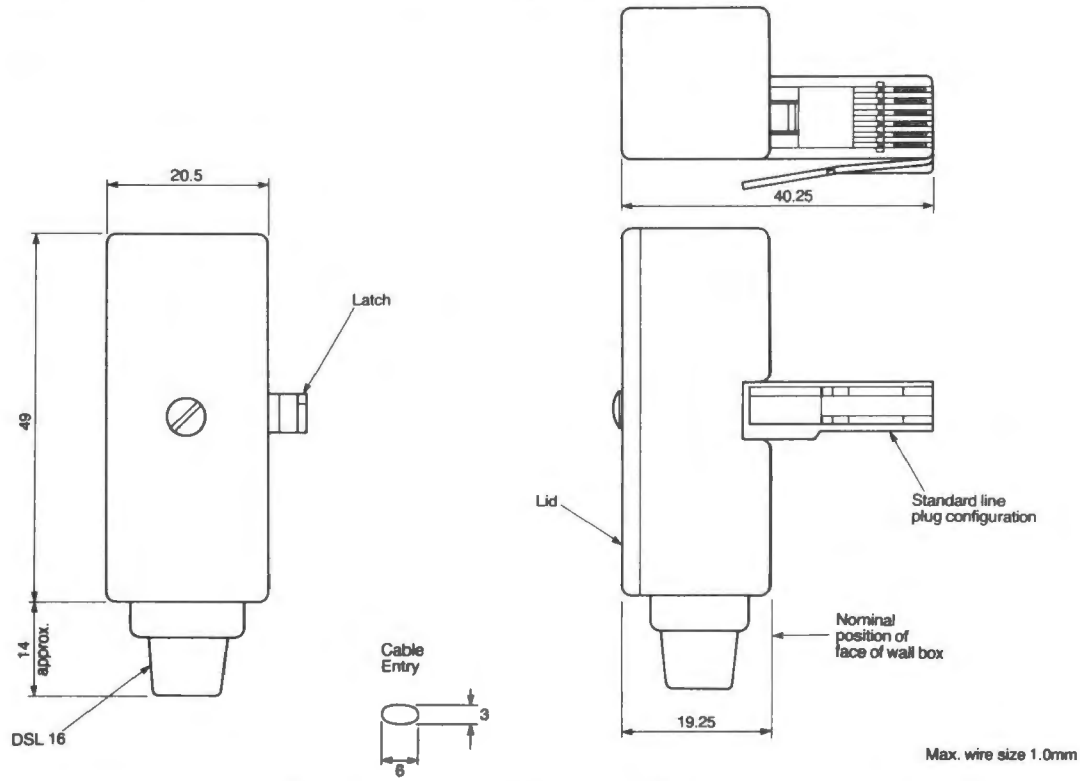
Method of connection

1. Remove the lid.
2. Pass grommet over cord to be connected or discard if grommet is already on the cord.
3. Connect cord to plug using screw terminal blocks provided and in accordance with above table. If tagged cord is being used cut off spades leaving crimp barrel.
4. Fix the end of the cord to the grommet using the cable tie.
5. Push the terminal blocks, grommet and cord loop gently into the box and fix lid.

Colour coding

Contact 1	Black	Used on business telephones (not used on 4-way)
Contact 2	White	Line
Contact 3	Green	Earth (if required, used in recall systems)
Contact 4	Blue	Anti-tinkle (only needed if extension/s connected)
Contact 5	Red	Line
Contact 6	Orange	Used on business telephones (not used on 4-way)

Figure 13



Dual outlet adaptor: 470-336

This adaptor fits any line jack unit or 6-way jack socket with polarisation 'A', converting it to a dual outlet.

Figure 14 **circuit diagram**

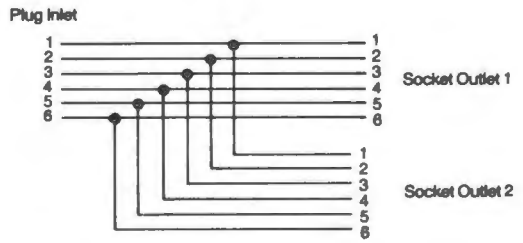
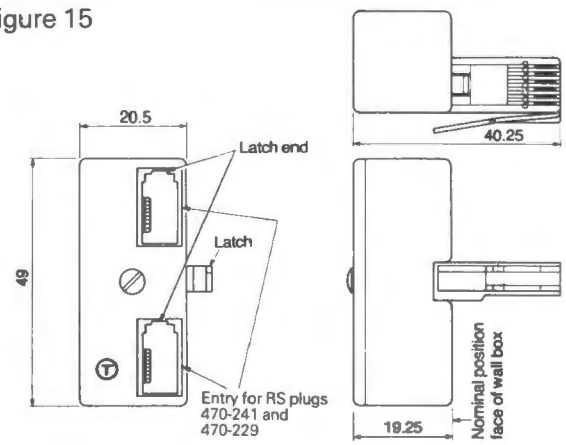


Figure 15



'Break-in' adaptor 470-342
This adaptor allows ancillary equipment to be easily connected to the plugged telephone installation. The adaptor allows the user to 'break in' into two of the parallel circuits.

Figure 16 **circuit diagram**

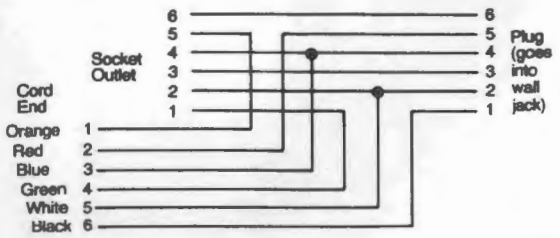
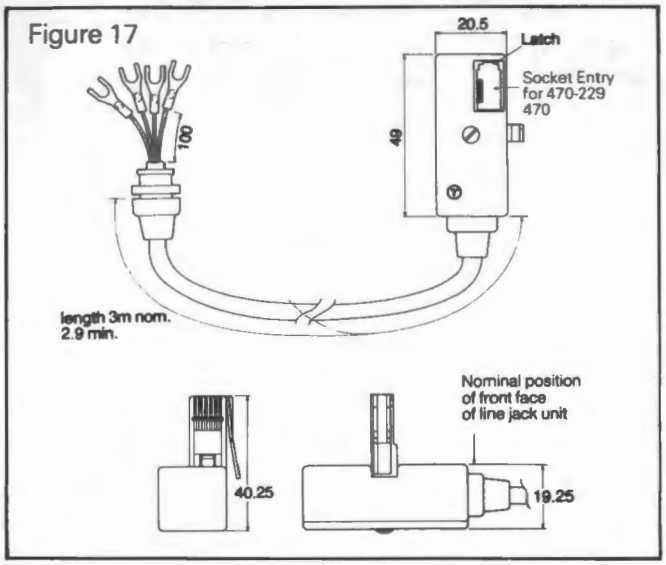
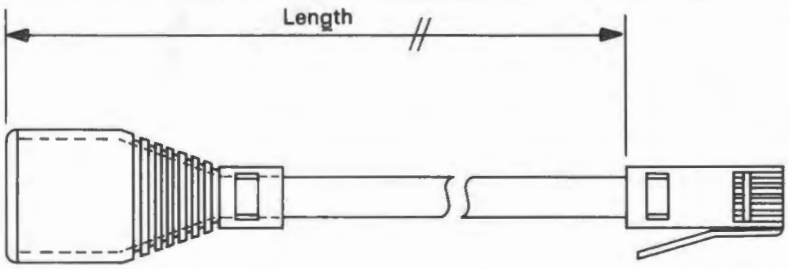


Figure 17



Extension cord 472-051 (3m), 472-067 (6m), 472-073 (10m)
The RS extension cord consists of a 631A line plug and 6 way line socket connected pin to pin by cordage to BT spec. CW1311.

Figure 18

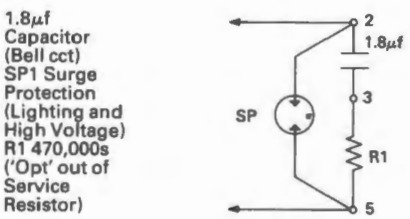


Jack colour
Connection sequence
1. Black
2. White
3. Green
4. Blue
5. Red
6. Orange

Plug colour
Connection sequence
1. Black
2. White
3. Green
4. Blue
5. Red
6. Orange

Line jack units – wall boxes

RS line jack units are for wall mounting. The line jack 1 and 2 units are for surface mounting only. Line jack units 3, 4 and 5 conform to the general outline of electrical switches and sockets to BS 1363-1967 (Standard UK 13A socket outlets). Line jack units are either master or secondary units – the master having bell capacitor, 'opt-out-of' service resistor and surge arrester. Only one master socket should be used in most installations. A master (or primary socket) can be distinguished from an extension socket by the extra components it contains; ie. 1.8μf capacitor, 470k resistor, high voltage/ lighting protection element.

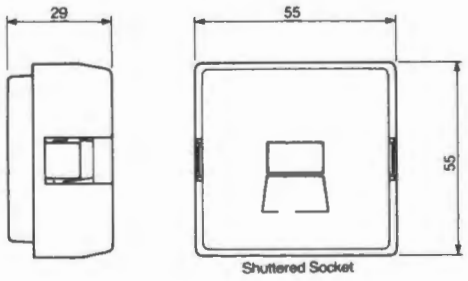


Master unit circuit/component diagram

RS line jack units are available in 2 types:
a) IDC connector types which require single strand 0.5mm connecting wire (2 per terminal) and a special tool.
b) Screw terminal types which need only a small screwdriver and will connect up to 1.00mm wires.

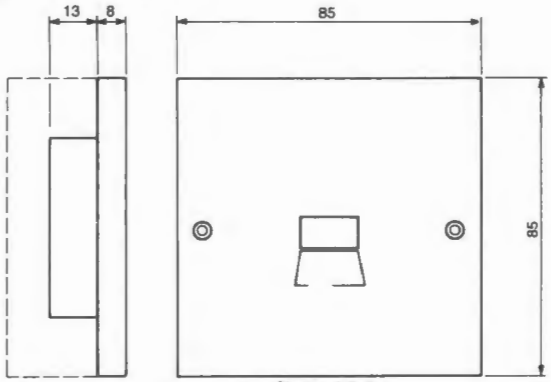
RS Master Jacks Type 472-506 and 472-512
RS Secondary Jacks Type 470-358 and 470-364
This line jack has all the components and connectors on the half that is fixed to the wall. This makes wiring easier.

Figure 19 **LJU1/**



Master Jacks Type 472-540 and 472-556
Secondary Jacks Type 470-392 and 470-409
This line jack has all the components fixed to the rear of the unit.

Figure 20 **LJU3/**



Master Jacks Type 472-528 and 472-534
Secondary Jacks Type 470-370 and 470-386
This line jack unit has all the components fixed to the removable cover.

Figure 21 **LJU2/**

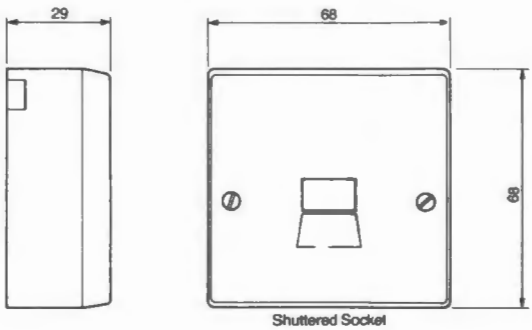
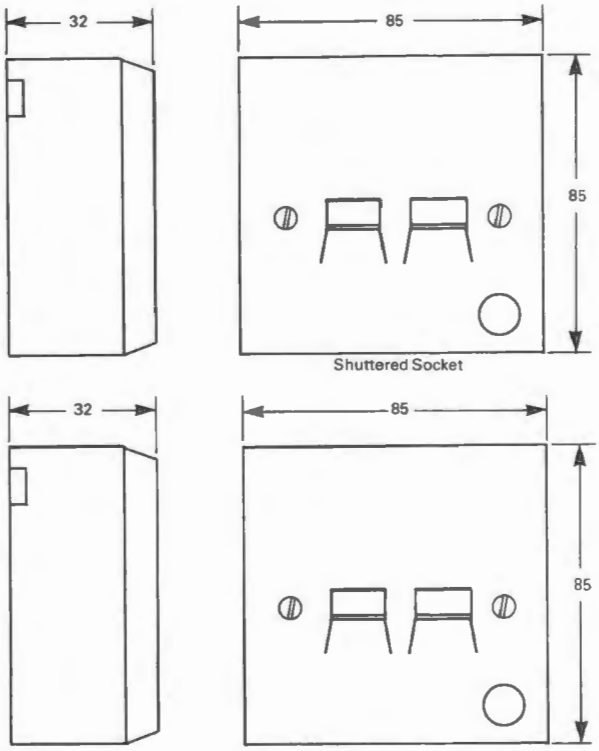


Figure 22 **LJU4 and 5**

Master Jacks Type 472-562 and 472-578
Secondary Jacks Type 470-960 and 470-976
This line jack has all the components fixed to the rear of the unit. The two socket outlets are mounted independently.

Master Jacks Type 472-584 and 472-590
Secondary Jacks Type 470-982 and 470-998
This line jack has all the components fixed to the rear of the unit. The two socket outlets are connected in parallel.



Connection of cordage to insulation displacement terminals

1. Strip outside sheath from cordage (100mm approx).
2. Place the appropriate strand over the terminal slot.
3. Using tool number RS 470-128, place tool over slot and press downwards inserting the strand into the terminal slot as shown in fig. 24.

Figure 23

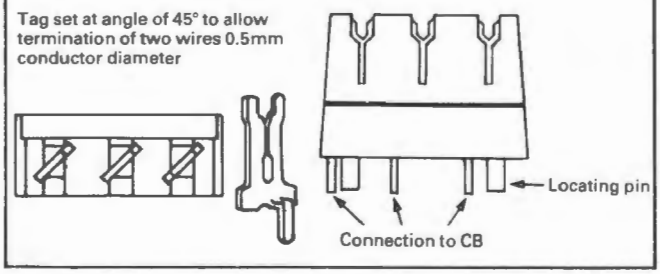
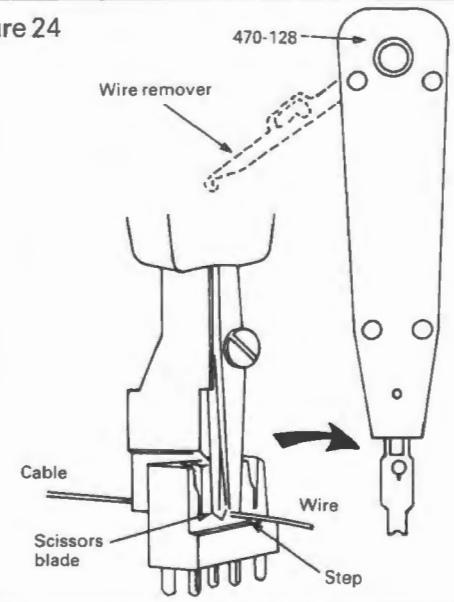


Figure 24



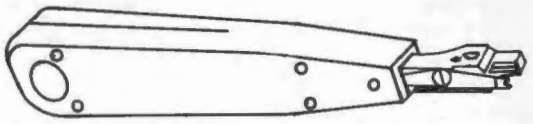
Tooling

IDC handtool (precision) 470-128

For use when terminating cable to IDC contacts within line jacks.

For termination instructions see above

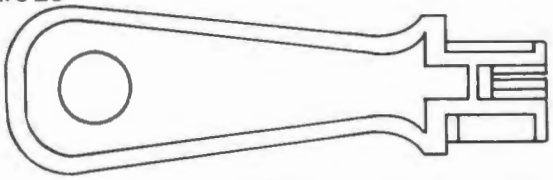
Figure 25



Plastic IDC termination tool 470-487

For use in the same applications as 470-128 (above)

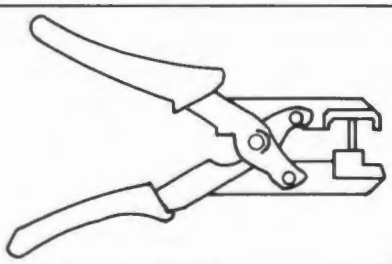
Figure 26



Plug termination hand tool 470-134

This simple lever action handtool will terminate all line and handset plugs to the recommended cable. This tool will perform the following operations simultaneously: press down the insulation displacement contacts onto the wire; enlarge the conductor strain relief; engage the sheath strain relief.

Figure 27



Termination procedure

1. Strip sheath 15mm from end of cable (make sure strands are of equal lengths).
2. Carefully push insulated strands into corresponding holes in the plug.
3. Insert plug and cable into jaw of tool until plug latch operates (Fig. 28).
4. Operate the tool as a normal pair of crimping pliers (Fig. 29).
5. Press latch on plug and withdraw cable and plug assembly.

Figure 28

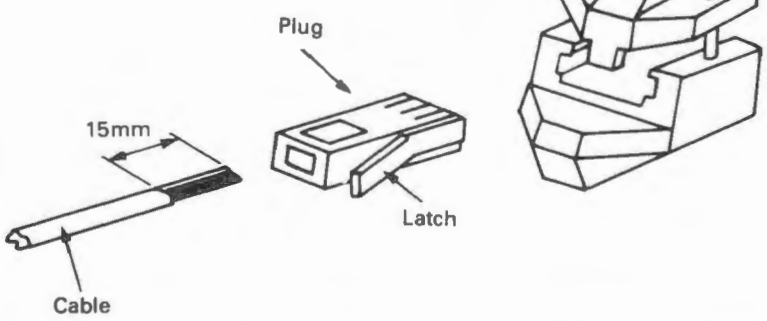
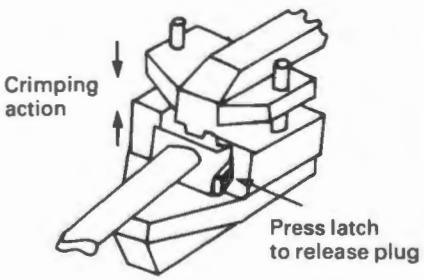


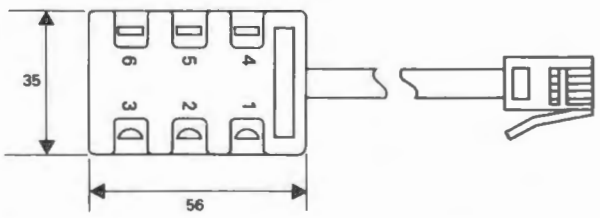
Figure 29



Line Socket Test Plug 471-597 (50mm) and 471-604 (1m)

The RS 'break-out' test plug is an engineer's test tool designed for accessing circuits via RS line jack units and line sockets.

Figure 30

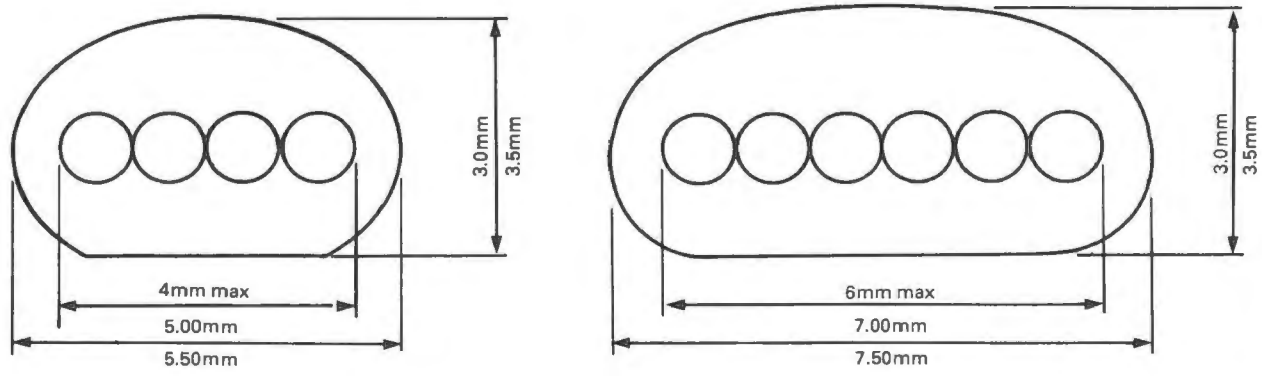


RS data

Cable

The cable is a specially designed 'D' shaped cordage to BT specification CW1311 and is available in 4 and 6 ways on 200m reels.

Figure 31



(a) 4-way 368-025

(b) 6-way 368-031

Cross-section of 4-way and 6-way cordage.

Specification

Conductors	7/0.152 T.A.C.W.
Insulation	PVC 1.00mm diameter (nominal)
Sheathing	PVC (grey)
4-core dimension	5.25 x 3.25mm (nominal)
4-core dimension	7.25 x 3.25mm (nominal)

Cable clips

4 and 6 way cable clips for hanging 'D' shaped cordage to B.T. specification CW1311. Body material is white plastic with hardened steel fixing pins.

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RS data

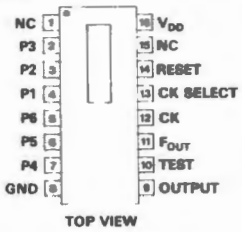
Programmable Crystal Oscillators

Stock numbers 301-858, 301-864

Two programmable crystal oscillators which can be used to generate 57 different output frequencies. The broad range of output frequencies is derived from the internal crystal oscillator. Two different base frequency oscillators of 600kHz and 1MHz are available giving output frequencies from 0.005Hz up to 1MHz. The oscillators are housed in standard 16-pin DIL packages.

Features

- Provide 57 different frequencies from a single internal quartz crystal.
- Frequency range from 0.005Hz to 1MHz.
- Laser trimmed for high accuracy.
- Lower power consumption.
- TTL compatible.



TOP VIEW

Absolute maximum ratings

Supply voltage	−0.3 to +10V
Operating temperature	−10 to +70°C
Storage temperature	−30 to +85°C

Performance specification

Calibration tolerance	±100p.p.m.
Frequency stability	±0.015%
Voltage coefficient	10p.p.m/V typ. 25p.p.m/V max.
Aging	10p.p.m max.

Electrical characteristics T_a=25°C V_{DD}=5V

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	4.0	5.0	6.0	V
I_{OH}	Output current: Hi[1]			−1.0	mA
I_{OL}	Output current: Lo[2]	1.6			mA
V_{IH}	Input voltage: logic 1	V_{DD}−1.0		V_{DD}	V
V_{IL}	Input voltage: logic 0	0.0		1.0	V
I_{IH}	Input current reset: Hi			0.5	μA
I_{IL}	Input current reset: Lo	−15			μA
I_{IH}	Input current Prog 1-6, CSEL, CK, TEST: Hi			15	μA
I_{IL}	Input current Prog 1-6, CSEL, CK, TEST: Lo	−0.5			μA
I_{DD}	Supply current[3]		0.7	1.0	mA

[1]V_{OH} = 4V [2]V_{OL} =0.4V [3]Crystal: 600kHz, OUT: 60kHz

Switching characteristics

Ta =25°C V_{DD}=5V C_L=15pf

Symbol	Parameter	Typ	Max	Unit
t_R	Reset delay time		1.0	μsec
t_E	Timing error after reset released		1.5	μsec
t_r	Rise time	70		nsec
t_f	Fall time	30		nsec
F_{in}	External oscillator operating frequency		1.25	MHz

WARNING!

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Figure 1 **Block diagram**

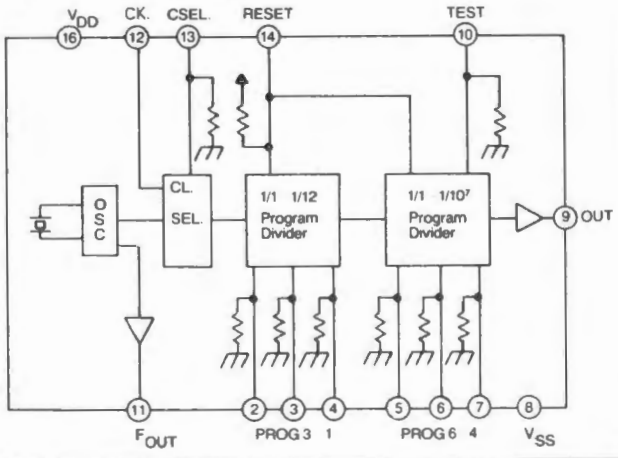
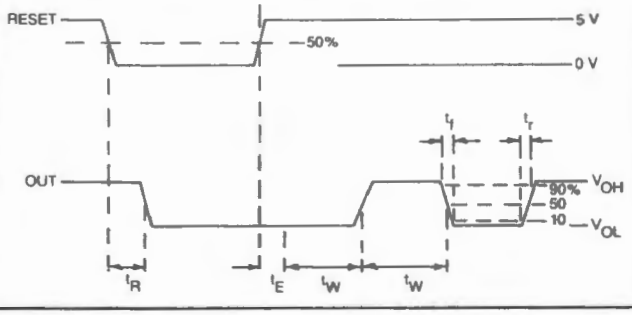


Figure 2 **Timing diagram**



RS data

Pin Functions

Prog 1 through Prog 6 control divide ratio of base frequency.

Prog 1	Prog 2	Prog 3	Dividing ratio	Prog 4	Prog 5	Prog 6	Dividing ratio
0	0	0	1/1	0	0	0	1/1
0	0	1	1/10	0	0	1	1/10
0	1	0	1/2	0	1	0	$1/10^2$
0	1	1	1/3	0	1	1	$1/10^3$
1	0	0	1/4	1	0	0	$1/10^4$
1	0	1	1/5	1	0	1	$1/10^5$
1	1	0	1/6	1	1	0	$1/10^6$
1	1	1	1/12	1	1	1	$1/10^7$

OUT: Supplies programmed output frequency with rectangular pulse shape (50% duty cycle, except as noted).

TEST: Setting this terminal Hi multiplies programmed output frequency by 1,000, except when programmed divide ratio is less than 1/1000.

F_{OUT}: Supplies base frequency of internal crystal oscillator.

CK: External clock input.

CSEL: Clock select. Setting this terminal Hi causes the divider to count the frequency of an external clock instead of the internal clock.

RESET: Setting this terminal Lo resets all counters and sets output to Lo.

(All inputs except CK and RESET have internal pull-down resistors. RESET has an internal pull-up resistor.)

Output frequencies of 600kHz unit (301-858)

UNIT: Hz

Program Pin Settings		P4	0	0	0	0	1	1	1	1
		P5	0	0	1	1	0	0	1	1
		P6	0	1	0	1	0	1	0	1
P1	P2	P3								
0	0	0	600K	60K	6K	600	60	6	0 6	0 06
0	0	1	60K	6K	600	60	6	0 6	0 06	0 006
0	1	0	300K	30K	3K	300	30	3	0 3	0 03
0	1	1	200K	20K	2K	200	20	2	0 2	0 02
1	0	0	150K	15K	1 5K	150	15	1 5	0 15	0 015
1	0	1	120K	12K	1 2K	120	12	1 2	0 12	0 012
1	1	0	100K	10K	1K	100	10	1	0.1	0 01
1	1	1	50K	5K	500	50	5	0 5	0.05	0 005

*33% duty cycle **40%duty cycle

Output frequencies of 1MHz unit (301-864)

UNIT: Hz

Program Pin Settings		P4	0	0	0	0	1	1	1	1
		P5	0	0	1	1	0	0	1	1
		P6	0	1	0	1	0	1	0	1
P1	P2	P3								
0	0	0	1M	100K	10K	1K	100	10	1	0 1
0	0	1	100K	10K	1K	100	10	1	0 1	0 01
0	1	0	500K	50K	5K	500	50	5	0 5	0.05
0	1	1	333.3K	33 3K	3 3K	333.3	33 3	3 3	0 33	0 033
1	0	0	250K	25K	2.5K	250	25	2 5	0 25	0.025
1	0	1	200K	20K	2K	200	20	2	0.2	0.02
1	1	0	166.6K	16.6K	1 6K	166.6	16.6	1 66	0.16	0.016
1	1	1	83.3K	8 3K	833.3	83 3	8 3	0 83	0 083	0 0083

*33% duty cycle **40%duty cycle

Applications

Figure 3 **One shot timer**

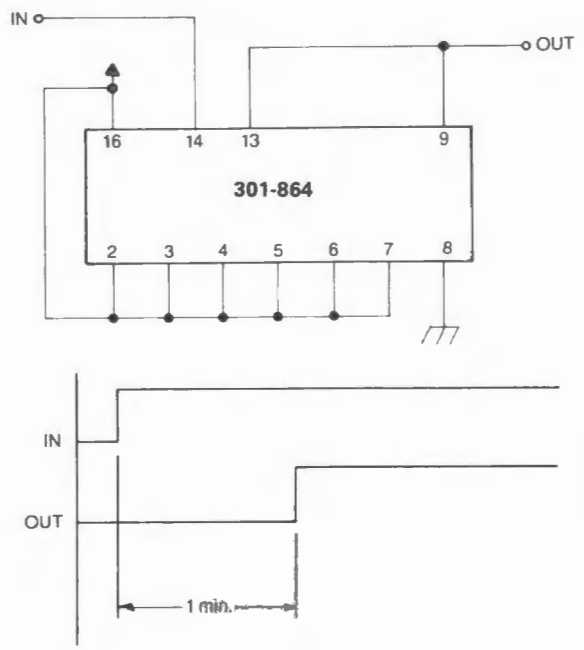
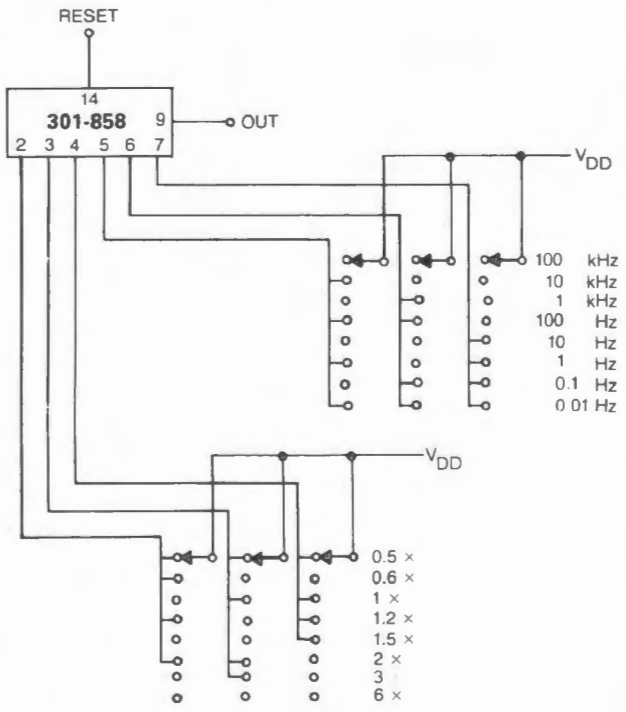


Figure 4 **Square wave generator providing 0.005Hz to 600kHz (for 600kHz oscillator)**



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RS data

Electronic motor protection relay and accessories

Stock numbers 346—249, 255, 261, 277, 283, 299

The three phase, electronic, motor protection relay and accessories make up a system of overload, stalled current and phase failure protection that offer benefits over the conventional bi-metallic (thermal) or solenoid overload devices.

The need for such a product

When a large motor burns out, the cost of repair or replacement, besides the dismantling and re-installation, is high.

Even with small motors, their application may warrant a greater degree of protection. An industrial process may be involved which, if interrupted, would result in spoilage or costly 'down time'.

Indiscriminate repeated starting, or attempts to start a stalled motor is considered to be the biggest cause of electrical failures, whether directly due to overheating or as a result of the mechanical stresses set up in the machine. A severe example is where a motor is working in high ambient temperatures, e.g. near a furnace, hot pipe etc., the motor may not cool down, after an overload trip, as quickly as the overload relay. The motor is restarted causing further overheating until eventual burn out.

Heavy duty starts may cause a conventional overload relay to trip out before the run-up time has expired. It is not good practise to increase the trip current to a level which will prevent this 'nuisance' tripping since this may be well above the rated motor current, thus reducing motor protection.

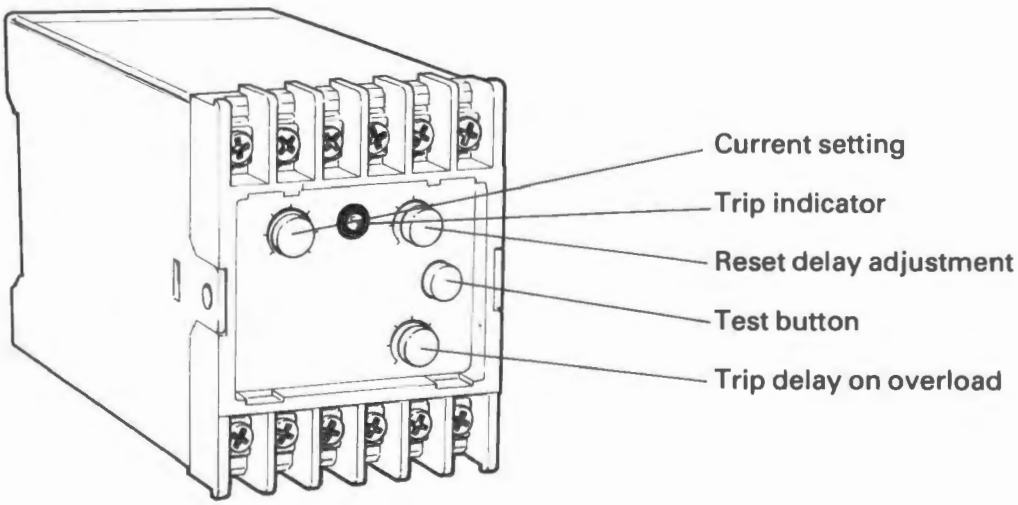
The RS three phase, electronic, motor protection unit is designed to overcome these problems.

Features

- Precise setting of minimum over-load to match actual load conditions.
- Tripping time base on I^2 which gives an inverse time characteristic approximating the thermal behaviour of the load.
- Full load current (f.l.c.) range from 0.65A to 2 times nominal current transformer rating (see selection chart).
- Tripping time adjustable (up to 40 secs. at 6 x f.l.c.) to take into account slow run-up times but can be set as low as 2 seconds.
- Rapid phase failure tripping feature independant of overload trip setting (approximately 2 seconds).
- Constant repeatability (no thermal drift).
- Remote pushbutton reset or auto reset.
- Delay before permissable reset adjustable 1-20 minutes.

Specification

Operating Voltage	240V 50Hz or 415V 50Hz by means of external voltage dropper
Tolerance (basic relay)	–25% +10%
Consumption (operating voltage)	12.5VA
Output Relay	1 NC and 1NO contacts electrically separate rated at 1A (AC11) at 240V AC
Operating temperature	–25°C to +60°C
Storage temperature	–25°C to +85°C



Basic relay (346-249)
The electronic overload relay is mounted in an ABS plastic case and has three customer adjustable settings – trip current, trip delay and reset delay. A l.e.d. trip indicator is mounted on the top face. A test button is also provided.

Adjustments
Trip current setting can be pre-set over a nominal range of 3:1.

Trip delay on overload can be adjusted over a range of approximately 20:1 (refer to trip curves).

Reset delay time selection from a nominal range of 1 to 20 minutes.

Test pushbutton simulates approximately 8 x f.l.c. for manual check of performance.

Hand reset (remote push button) or auto (by wire link). For safety reasons this reset adjustment will not override either the trip or reset delay functions.

Cable terminations (max cable size 2.5mm^2)
11 terminals are utilized in the following manner:

Terminal numbers	Function	
1 & 2	N/O output contact rated 1A (AC11) at 240V a.c.	Relay energises when supply applied and unit reset
3 & 4	N/C output contact rated 1A (AC11) at 240V ac.	
5 & 6(N)	Supply 240V 50/60Hz (line to neutral)	
7, 8 & 9	Input from current transformers 25mA secondary winding	
10 & 11	Remote reset (or link if auto reset is required)	
12	Spare	

Current transformers
A range of current transformers with a 25mA secondary winding, saturating at about 10 x f.l.c. Specially designed for use with the Electronic Motor Protection Relay. The types available from RS are as follows:

Primary/secondary	Stock No.
1A/25mA	346-261
20A/25mA	346-277
50A/25mA	346-283
100A/25mA	346-299

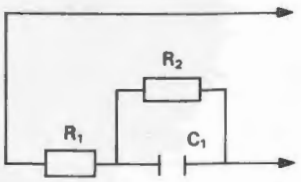
These current transformers are supplied in pairs which is normally sufficient for monitoring three wire connected loads. Three current transformers are essential for four wire connected loads and recommended when current transformers are to be connected in the phases of a delta connected motor (see current transformer selection chart (i)).

Current transformer selection chart

Motor F.L.C. (Amps)	Connected in Supply Lines				(1) Connected in Phases of Y△ status			
	C.T.	Turns Through C.T.	Setting Range (2) Min	Max.	C.T.	Turns Through C.T.	Setting Range (2) Min	Max.
0-0.7								
0.8-1.4	1 Amp: 25mA (346-261)	Direct Conn.	0.65	2.0	1 Amp: 25mA (346-261)	Direct Conn.	1.2	3.4
1.5-1.6								
1.7-3.1	20 Amp: 25mA (346-277)	10	1.3	4.0	20 Amp: 25mA (346-277)	10	2.2	6.9
3.2-3.5								
3.6-5.4		5	2.6	8.0		5	4.5	13.8
5.5-8.5		4	3.3	10		4	5.7	17.3
8.6-15.7		2	6.5	20		2	11.3	34.6
15.8-17.5								
17.6-29.2		1	13	40		1	22.6	69.2
29.3-42.8	50Amp: 25mA (346-283)	2	16.3	50	50Amp: 25mA (346-283)	2	28.2	86.6
42.9-54.3		1	32.5	100		1	56.3	173
54.4-74.2								
74.3-87								
87.1-160	100Amp: 25mA (346-299)	1	65	200	100Amp: 25mA (346-299)	1	113	346
160.1-180								
180.1-257	200Amp: 1 Amp plus 1 Amp: 25mA OR 200 Amp: 5 Amp plus 4 turns through 20 Amp: 25mA	1 THROUGH MAIN CT DIRECT CONN. SECONDARY CT 1 THROUGH MAIN CT 4 THROUGH SECONDARY CT	(3) 135	(3) 400				
257.1-307	300Amp: 1 Amp plus 1 Amp: 25mA OR 300 Amp: 5 Amp plus 4 turns through 20 Amp: 25mA	1 THROUGH MAIN CT DIRECT CONN. SECONDARY CT 1 THROUGH MAIN CT 4 THROUGH SECONDARY CT	(3) 195	(3) 600	200Amp: 1 Amp plus 1 Amp: 25mA OR 200 Amp: 5 Amp plus 4 turns through 20 Amp: 25mA	1 THROUGH MAIN CT DIRECT CONN. SECONDARY CT 1 THROUGH MAIN CT 4 THROUGH SECONDARY CT	(3) 234	(3) 692
307.1-350								
350.1-450	400Amp: 1 Amp plus 1 Amp: 25mA OR 400 Amp: 5 Amp plus 4 turns through 20 Amp: 25mA	1 THROUGH MAIN CT DIRECT CONN. SECONDARY CT 1 THROUGH MAIN CT 4 THROUGH SECONDARY CT	(3) 260	(3) 800	300Amp: 1 Amp plus 1 Amp: 25mA OR 300 Amp: 5 Amp plus 4 turns through 20 Amp: 25mA	1 THROUGH MAIN CT DIRECT CONN. SECONDARY CT 1 THROUGH MAIN CT 4 THROUGH SECONDARY CT	(3) 338	(3) 1039
450.1-550	500Amp: 1 Amp plus 1 Amp: 25mA OR 500 Amp: 5 Amp plus 4 turns through 20 Amp: 25mA	1 THROUGH MAIN CT 4 THROUGH SECONDARY CT 1 THROUGH MAIN CT DIRECT CONN. SECONDARY CT	(3) 325	(3) 1000				

Notes: (1) Connect 1 current transformer per phase (see typical circuit configurations).
(2) Setting range – this is the normal limit of adjustment on the basic relay.
(3) These figures only apply if the main current transformer is linear up to twice normal rating.
The relay is not suitable for single phase loads or single current transformer operation on balanced loads.

Voltage dropper (346-255)
A series wired unit for use with 240V relay on 415V supply.
Power consumption 0.6W.



Voltage dropper circuit

Installation

The basic relay should be mounted onto a vertical and flat surface free from significant vibrations. The unit may be clipped onto 35mm symmetric DIN rail (EN 50 022) RS stock number 424-131. A small section of rail is provided for direct to panel mounting. The two wire controls for remote push-button reset, should be twisted for up to 3 metres but for longer runs it is recommended that the wires should be screened. Terminal 12 on thre basic relay may be used as a connecting point between screen and earth. (See typical circuit configurations).

The current transformers should be wired up as shown in the appropriate diagram under 'typical circuit configurations' however the phase conductors may need to pass through the current transformers several times in order to obtain the desired secondary current for the relay (see current transformer selection chart).

Operation

The measured current from the current transformers is rectified by the basic relay and the resultant output is used to determine:

a) If the current setting is being exceeded. This being the case, then the unit will trip out in accordance with the trip time setting and the percentage overload (see typical trip curves).

b) If the ripple frequency is correct. This frequency alters when a phase is lost. The sensing circuit detects this difference and causes the unit to trip out in approximately 2 seconds.

Resetting the relay, either by remote pushbutton or automatically when a link is in circuit, can only occur after the preset delay period.

The relay is energised in the 'healthy' condition and will fail safe, tripping on the loss of unit supply. There is a short delay (approx. ½ second) before contacts attain the 'healthy' position on initial application of supply to the unit.

Setting Up

1. Initial setting up of unit.

   Two alternative methods are possible, the first of which should prove to be the most accurate.

   a) With both current and trip delay settings at maximum, start motor in normal manner. Reduce current setting until l.e.d. on unit is illuminated then increase setting until l.e.d. is extinguished – unit is now correctly set and will go into overload mode (i.e. l.e.d. illuminated) if current increases by approx. 10%. Trip delay setting and reset time setting should now be adjusted to 'desired values'.

   'Desired value' of trip delay should be just sufficient for motor to run up to speed on maximum load, i.e. a high inertia load will usually require a higher setting than a low inertia load.

   'Desired value' of reset time should be sufficient to allow motor to cool down prior to restart; i.e. a large motor will usually require a longer cooling time than a small motor.

   N.B. This method can only be used if the motor can be run on max. load (even if this does not correspond to max f.l.c.). If motor cannot be fully loaded and is to trip only when current exceeds rated f.l.c. then use method b).

   b) Using the fact that minimum current setting is approximately 0.65 x nominal c.t. rating (maximum being approximately 2 x nominal c.t. rating) then the following calculaton will give approximate angular displacement of current setting potentiometer from the minimum position i.e.:

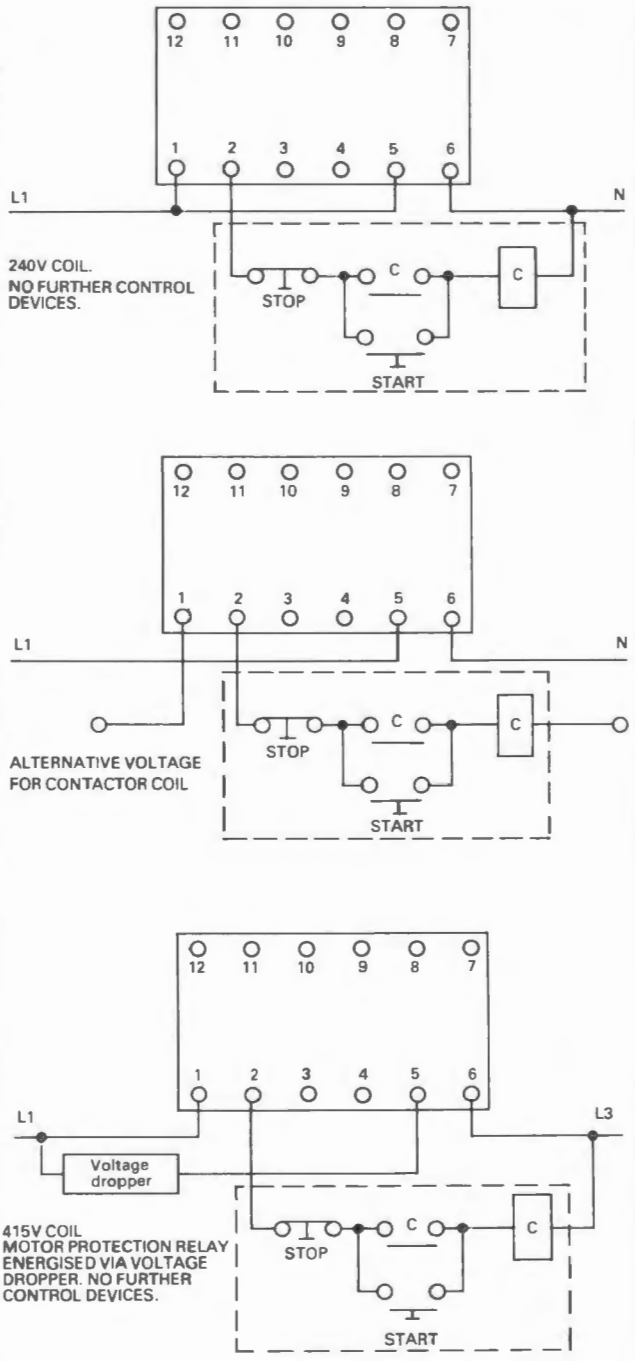
   $$\frac{200 \times \text{f.l.c.}}{\text{c.t. rating}} - 130°$$

   Trip delay and reset time setting should then be adjusted to desired values.

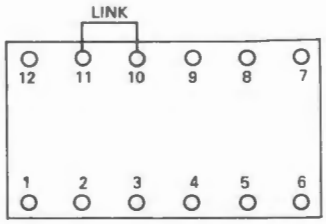
2. After setting up unit, the stalled motor trip delay can be checked by means of the Trip Test button. This will give the approximate delay available for both 'hot' and 'cold' conditions.

Typical circuit configurations

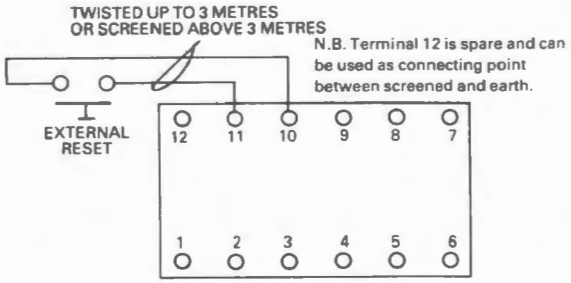
(1) Supply to basic relay and control circuits



(2) Hand or Auto reset

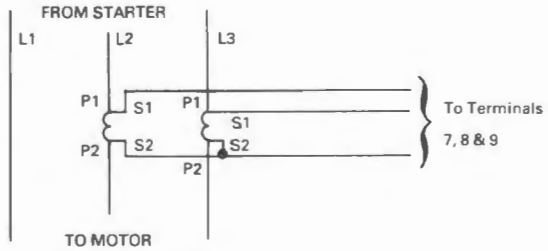


Auto reset if required.
The 'delay before reset' can still be adjusted. This is particularly useful on unattended motors.

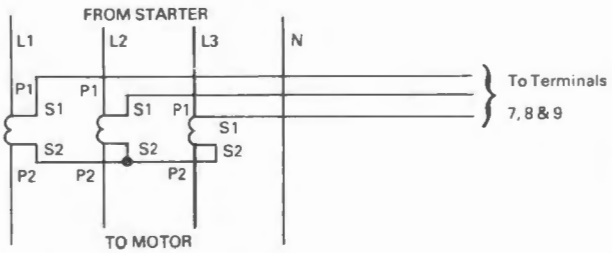


Remote reset (e.g. additional N/O contact block on the stop button of the RS two button station. Stock No. 333-669).

(3) Current transformers

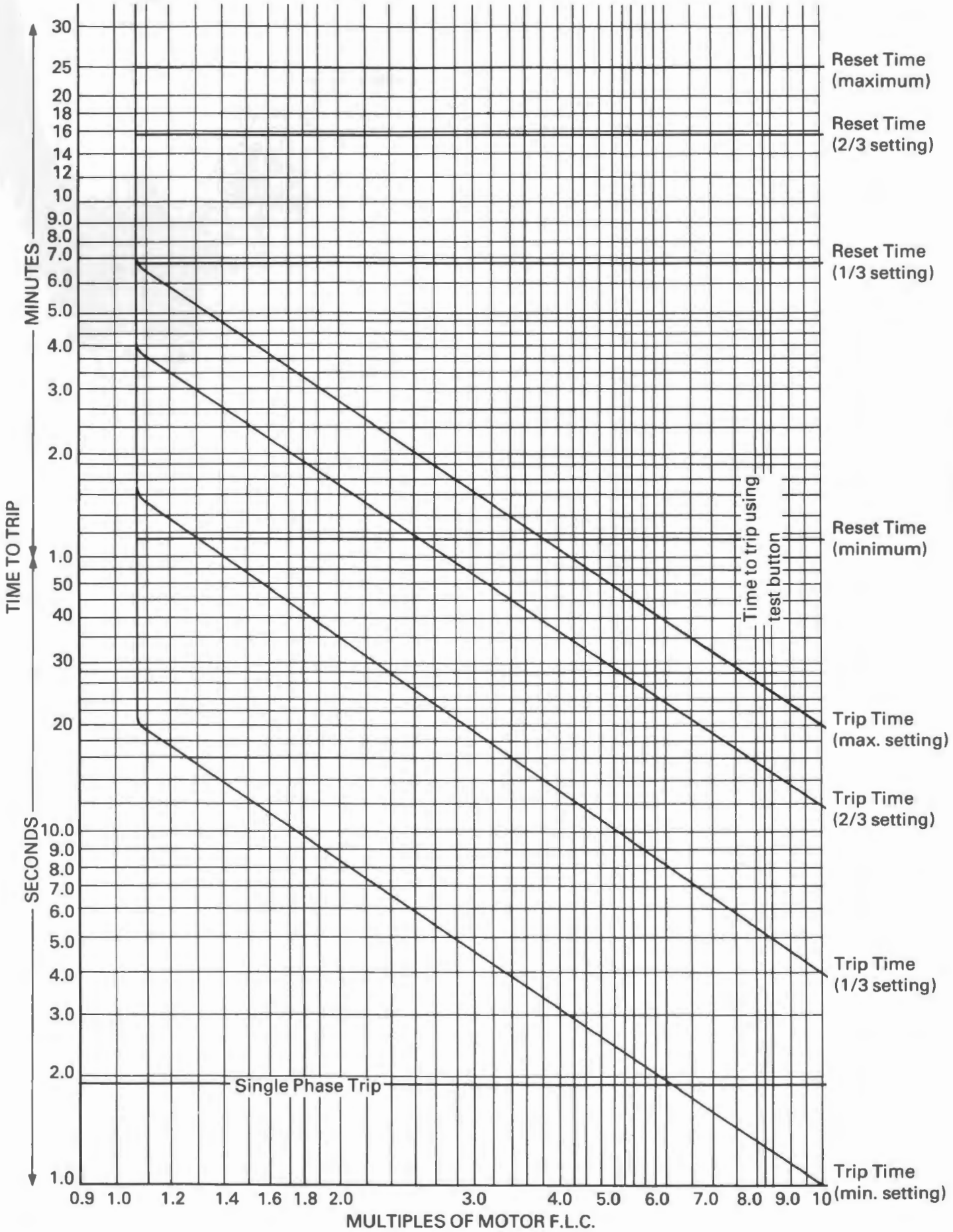


3 Phase 3 wire system



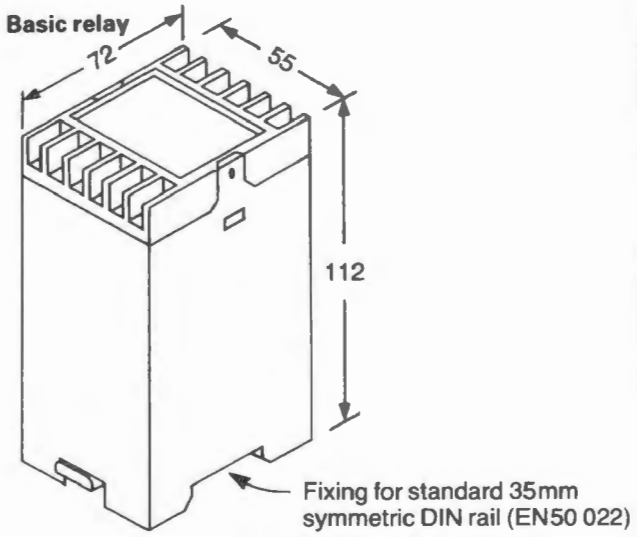
3 Phase 4 wire system

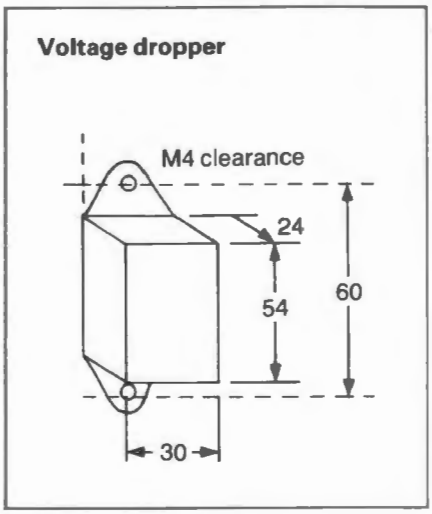
TYPICAL TRIP CURVES



RS data

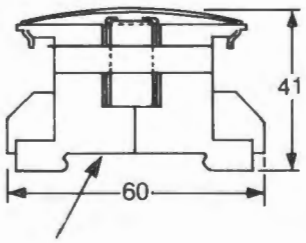
Dimensions



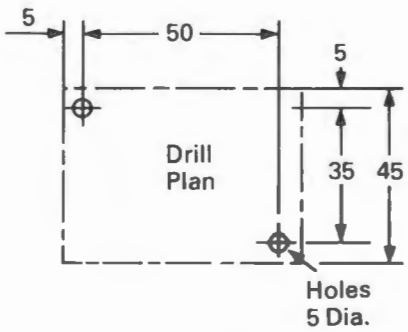


Current transformers

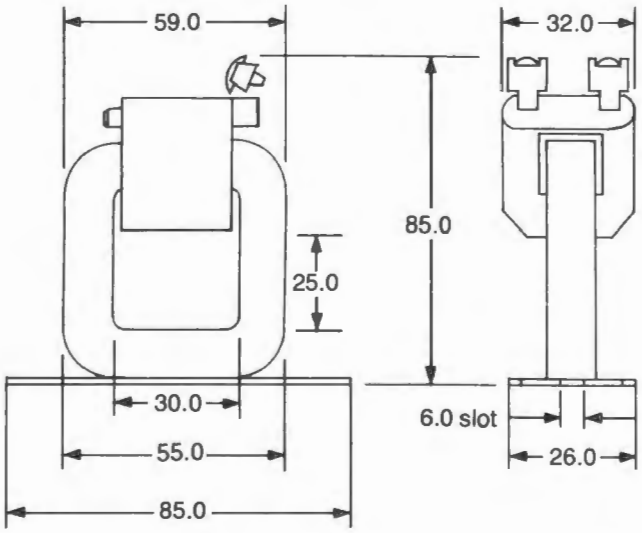
Type 1A/25mA (346-261)



Fixing for standard 35mm
symmetrical DIN rail (EN 50 022)
RS Stock No. 424-131



Types 20A/25mA (346-277), 50A/25mA (346-283)
and 100A/25mA (346-299)



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RS data

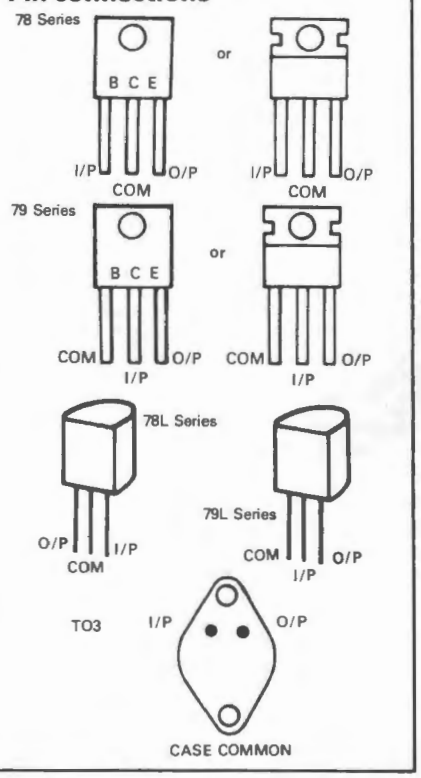
Fixed voltage series regulators

A range of 19 fixed voltage linear regulators with outputs covering a wide range of positive or negative output voltages.

Quick selection table

Description	Output Voltage	Output Current	Case	Stock No.	Suitable Transformer Stock No.	Sec. Voltage	VA
78L05	5V	100mA	T0-92	**306-190**	207-188	9(S)	6
RS309K (LM309K)	5V	1.2A	T03	**305-614**	207-122	9(S)	20
7805	5V	1.2A	T0220	**305-888**	207-122	9(S)	20
78H05	5V	5A	T03	**307-301**	207-239	9(S)	50
78L12	12V	100mA	T0-92	**306-207**	207-217	15(P)	6
7812	12V	1.2A	T0220	**305-894**	207-267	15(P)	50
78H12	12V	5A	T03	**307-317**	207-289	12(S)	100
78L15	15V	100mA	T0-92	**306-213**	207-217	15(P)	6
7815	15V	1.2A	T0220	**305-901**	207-267	15(P)	50
78L24	24	100mA	T0-92	**306-229**	207-201	24(S)	6
7824	24	1.0A	T0220	**305-917**	207-251	24(S)	50
79L05	–5	–100mA	T0-92	**306-235**	207-188	9(S)	6
7905	–5	–1.2A	T0220	**306-049**	207-122	9(S)	20
79L12	–12	–100mA	T0-92	**306-241**	207-217	15(P)	6
7912	–12	–1.2A	T0220	**306-055**	207-267	15(P)	50
79L15	–15	–100mA	T092	**306-251**	207-217	15(P)	6
7915	–15	–1.2A	T0220	**305-923**	207-267	15(P)	50
79L24	–24	–100mA	T092	**306-263**	207-201	24(S)	6
7924	–24	–1.0A	T0220	**306-184**	207-251	24(S)	50

Pin connections



Electrical characteristics – Positive Regulators

Parameter \ Type	78H05	78H12	RS309K	7805	7812	7815	7824	78L05	78L12	78L15	78L24	Units
Voltage output	**5**	**12**	**5**	**5**	**12**	**15**	**24**	**5**	**12**	**15**	**24**	V
Current output	5	5	1.2	1	1	1	1	0.1	0.1	0.1	0.1	A
Input voltage range	8 to 25	15 to 25	7 to 35	7 to 25	14.5 to 30	17.5 to 30	27 to 38	7 to 30	14.5 to 35	17.5 to 35	27 to 35	V
Load regulation	0.5	0.17	1	0.2	0.4	0.5	0.6	0.2	0.2	0.3	0.4	%
Ripple rejection	60	60	70	70	61	60	56	60	55	52	49	dB
Output impedance	2	2	50	30	75	95	150	200	200	200	200	mΩ
Line regulation	0.2	0.17	0.1	0.2	0.2	0.3	0.3	1	1	1.5	1.5	%
Output noise voltage	40	75	40	40	80	90	170	40	60	90	200	μV
Short circuit current	7	7	dependant on V_{IN}	0.75	0.35	0.23	0.15	–	–	–	–	A
Max. operating junction temperature	150	150	125	150	150	150	150	125	125	125	125	°C
Total power dissipation*	50	50	12.75	20	20	20	20	0.9	0.9	0.9	0.9	W
Thermal resistance (junction to case)	2	2	3	4	4	4	4	N/A	N/A	N/A	N/A	°C/W
Thermal resistance (junction to ambient)	33	33	35	50	50	50	50	180	180	180	180	°C/W
Suitable transformer (for max. current)	207-289 sec. in series	207-302 sec. in parallel	207-122 sec. in series	207-122 sec. in series	207-267 sec. in parallel	207-267 sec. in parallel	207-251 sec. in series	– –	– –	– –	– –	

* T case = 25°C (internally limited), derate linearly to 0W at 150°C.

Electrical characteristics – Negative Regulators

Parameter \ Type	7905	7912	7915	7924	79L05	79L12	79L15	79L24	Units
Voltage output	**–5**	**–12**	**–15**	**–24**	**–5**	**–12**	**–15**	**–24**	V
Current output	1	1	1	1	0.1	0.1	0.1	0.1	A
Input voltage range	–7 to –25	–14.5 to –30	–17.5 to –30	–27 to –38	–7 to –25	–14.5 to –35	–17.5 to –35	–27 to –35	V
Load regulation	0.2	0.4	0.5	0.6	0.2	0.2	0.3	0.4	%
Ripple rejection	70	61	60	56	60	55	52	49	dB
Output impedance	30	75	95	150	200	200	200	200	mΩ
Line regulation	0.2	0.2	0.3	0.3	1	1	1.5	1.5	%
Output noise voltage	40	80	90	170	40	60	90	200	μV
Short circuit current	0.75	0.35	0.23	0.15	–	–	–	–	A
Max. operating junction temperature	150	150	150	150	125	125	125	125	°C
Total power dissipation*	20	20	20	20	0.9	0.9	0.9	0.9	W
Thermal resistance (junction to case)	4	4	4	4	N/A	N/A	N/A	N/A	°C/W
Thermal resistance (junction to ambient)	50	50	50	50	180	180	180	180	°C/W
Suitable transformer (for max. current)	207-122 sec. in series	207-267 sec. in parallel	207-267 sec. in parallel	207-251 sec. in series	–	–	–	–	

* T case = 25°C (internally limited), derate linearly to 0W at 150°C.

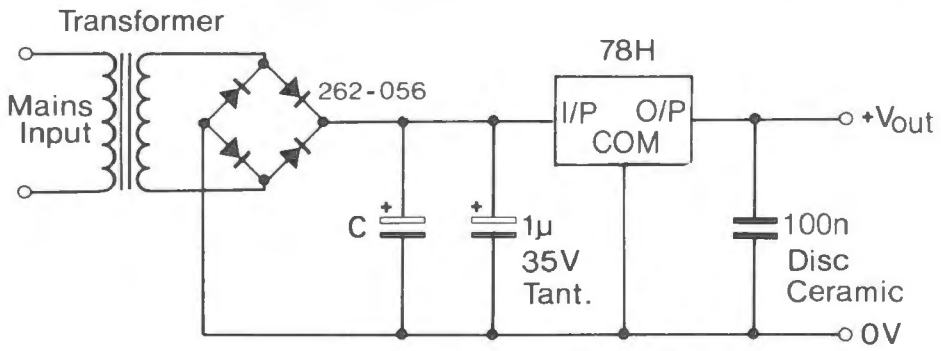
78H05 and 78H12 fixed hybrid regulators

Two fixed voltage hybrid regulators, housed in TO3 style metal cases, capable of supplying output currents up to 5 amps. The internal circuitry limits the junction temperature to a safe value and provides automatic thermal overload protection. Safe operating protection is also incorporated making the regulators virtually damage proof.

In order to achieve maximum performance the internal power dissipation must be kept below 50W. Transformer and heatsink selections are dependent upon the exact application.

78H – Basic circuit, fixed voltage

Figure 1



Regulator	Output Voltage	Transformer	Heatsink	C
78H05	+5V dc	207-239 (S)	401-807, 1.1°c/w	15,000μF 16V
78H12	+12V dc	207-289 (S)	401-403, 2.1°c/w	22,000μ 25V

Fixed voltage monolithic regulators

Figure 2 **Basic circuit – 78 series Positive regulators**

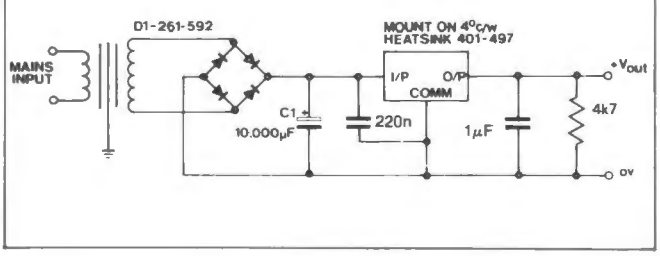
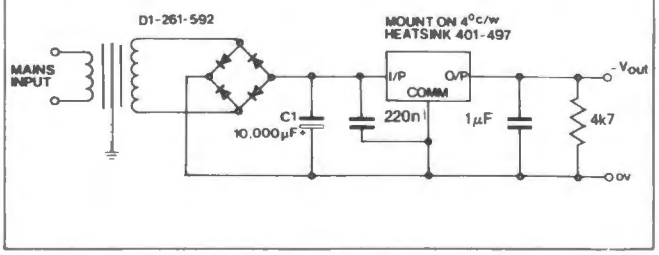
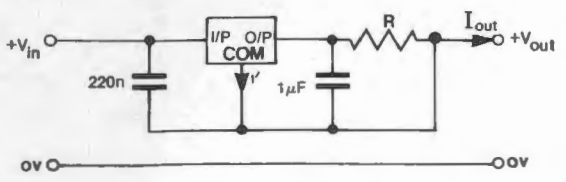


Figure 3 **Basic circuit – 79 series Negative regulators**



Notes: For suitable transformers see table on page 1

Figure 4 **Constant current generator**



For T03 types	1′ = 10mA typ.
For 78/79 series	1′ = 4.5mA typ.
For 78L/79L series	1′ = 3.5mA typ.

Circuit gives constant current through load provided V_{out} does not exceed $V_{in} - (V_R + 2.5)$. Select R to give designed constant current I_{out}

$$I_{out} = \frac{V_R}{R} + 1'$$

Where V_R is the basic regulator voltage.

Increasing basic regulator voltage

The input voltage V_{in} should be derived from a suitable transformer, rectifier and smoothing capacitor circuit. Note V_{in} must be greater (within maximum ratings) than $V_{out} + 2.5V$.

Figure 5 – gives higher output voltage than basic circuit but with reduced regulation.

$$V_{out} = V_R + 1'R$$

where V_R = basic regulator voltage.
1′ = 10mA (T03), 4.5mA (78/79), 3.5mA, (78L/79L) typ.

e.g. For 6V output with 5V regulator (306-190)

$$R = 220\Omega \text{ typ.}$$

Figure 5

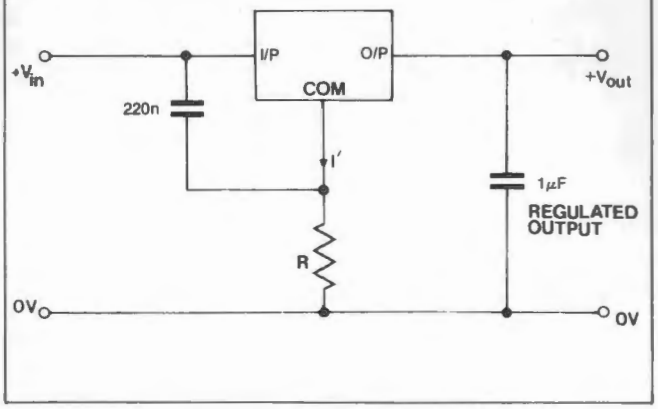


Figure 6 – gives better regulation than Figure 5.

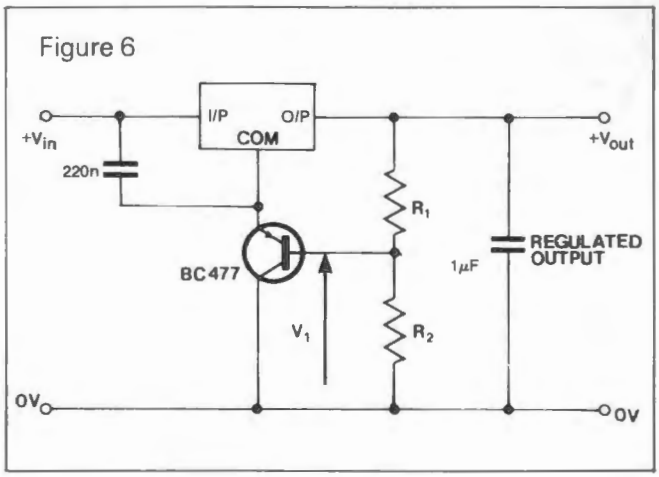
$$V_{out} = V_R + V_1 + 0.6$$

$$\text{where } V_1 = \frac{R_2\, V_{out}}{R_1 + R_2}$$

$$\text{and } \frac{R_1}{R_2} = \frac{V_R + 0.6}{V_{out} - (V_R + 0.6)}$$

e.g. For 9V output with 5V regulator
R1 = 5k6 R2 = 3k3

Figure 6



RS data

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RS data

Thermocouple amplifier AD595AD

Stock number 301-779

The AD595AD is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone Celsius transducer with a low-impedance voltage output.

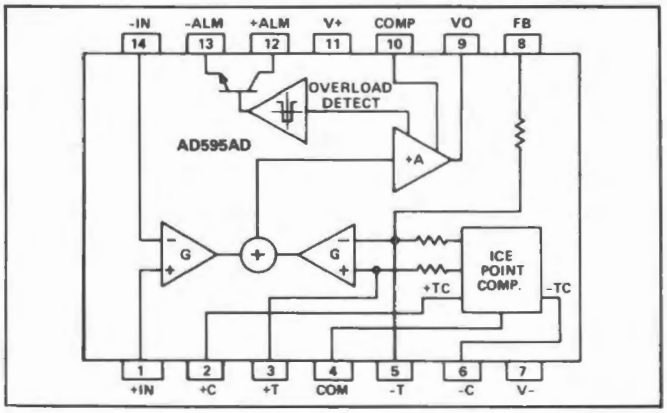
The AD595AD includes a Thermocouple Failure alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.

The AD595AD can be powered from a single ended supply (including +5V) and by including a negative supply temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD595AD will typically operate with a total supply current of 160μA, but is also capable of delivering in excess of ±5mA to a load.

The AD595AD is laser trimmed for type K (nickel-aluminium and nickel-chromium) inputs. The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of two or three resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications.

Features

- Pretrimmed for type K thermocouples
- Can be used with type T thermocouple inputs
- Low impedance voltage output: 10mV/°C
- Built-in ice point compensation
- Wide power supply range: +5V to ±15V
- Low power: <1mW typical
- Thermocouple failure alarm
- Set-point mode operation
- Self contained Celsius thermometer operation
- High impedance differential input



Absolute maximum ratings

$+V_S$ to $-V_S$	36	Volts
Common mode input voltage	$+V_S$ to $(-V_S - 0.15V)$	Volts
Differential input voltage	$\pm V_S$	Volts
Alarm voltages		
+ALM	$-V_S$ to $(-V_S + 36V)$	Volts
-ALM	$\pm V_S$	Volts
Operating temperature range	−55 to +125	°C
Output short circuit to common	Indefinite	

Electrical characteristics – Ta = 25°C; V_S = 5v; Type K thermocouple unless otherwise stated.

Temperature measurement		**Units**
(Specified Temperature Range 0 to + 50°C)		
Calibration error at +25°C[1]	±3	°C max
Stability vs. temperature[2]	±0.05	°C/°C max
Gain error	±1.5	% max
Nominal transfer function	10	mV/°C

Amplifier characteristics		
Closed loop gain[3]	247.3	
Input offset voltage	(temperature in °C) × 40.44μV/°C	μV
Input bias current	0.1	μA
Differential input range	−10 to +50	mV
Common mode range	$+V_S-4$ to $(-V_S-0.15)$	Volts
Common mode sensitivity – RTO	10	mV/V max
Power supply sensitivity – RTO	10	mV/V max
Output voltage range		
Dual supplies	$-V_S+2.5$ to $+V_S-2$	Volts
Single supply	$+V_S-2$ to 0	Volts
Usable output current[4]	±5	mA
3dB bandwidth	15	kHz
Alarm characteristics		
$V_{CE(SAT)}$ at 2mA	0.3	Volts
Leakage current	±1	μA max
Operating voltage at −ALM	$+V_S-4$	Volts max
Short circuit current	20	mA
Power requirements		
Specified performance	$+V_S=5, -V_S=0$	Volts
Operating	$+V_S$ to $-V_S \leq 30$	Volts
Quiescent current (No load)		
$+V_S$	160 typ, 300 max	μA
$-V_S$	100 typ	μA

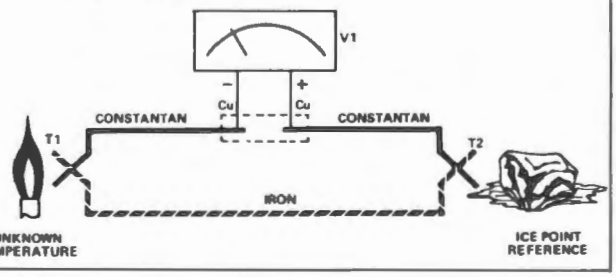
Note: 1 Calibrated for minimum error at +25°C using a thermocouple sensitivity of 40.44μV/°C. Since a type K thermocouple deviates from this straight line approximation, the AD595AD will normally read 2.7mV when the measuring junction is at 0°C.
Note 2: Defined as the slope of the line connecting the AD595AD, errors measured at 0°C and 50°C ambient temperature.
Note 3: Pin 8 shorted to Pin 9.
Note 4: Current sink capability in single supply configuration is limited to current drawn to ground through a 50kΩ resistor at output voltages below 2.5V.

Thermocouple basics

Thermocouples are economical and rugged; they have reasonably good long-term stability. Because of their small size, they respond quickly and are good choices where fast response is important. They function over temperature ranges from cryogenics to jet-engine exhaust and have reasonable linearity and accuracy.

Because the number of free electrons in a piece of metal depends on both temperature and composition of the metal, two pieces of dissimilar metal in isothermal contact will exhibit a potential difference that is a repeatable function of temperature, as shown in Figure 1. The resulting voltage depends on the temperatures, T1 and T2, in a repeatable way.

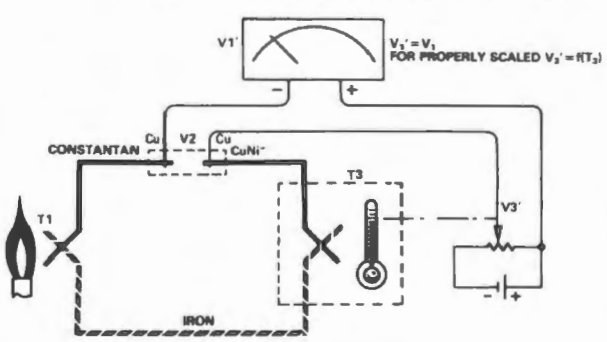
Figure 1 **Thermocouple voltage with 0°C reference**



Since the thermocouple is basically a differential rather than absolute measuring device, a known reference temperature is required for one of the junctions if the temperature of the other is to be inferred from the output voltage. Thermocouples made of specially selected materials have been exhaustively characterized in terms of voltage versus temperature compared to primary temperature standards. Most notably the water-ice point of 0°C is used for tables of standard thermocouple performance.

An alternative measurement technique, illustrated in Figure 2, is used in most practical applications where accuracy requirements do not warrant maintenance of primary standards. The reference junction temperature is allowed to change with the environment of the measurement system, but it is carefully measured by some type of absolute thermometer. A measurement of the thermocouple voltage combined with a knowledge of the reference temperature can be used to calculate the measurement junction temperature. Usual practice, however, is to use a convenient thermoelectric method to measure the reference temperature and to arrange its output voltage so that it corresponds to a thermocouple referred to 0°C. This voltage is

Figure 2 **Substitution of measured reference temperature for ice point reference**



simply added to the thermocouple voltage and the sum then corresponds to the standard voltage tabulated for an ice-point referenced thermocouple.

The temperature sensitivity of silicon integrated circuit transistors is quite predictable and repeatable. This sensitivity is exploited in the AD595AD to produce a temperature related voltage to compensate the reference or 'cold' junction of a thermocouple as shown in Figure 3.

Figure 3 **Connecting isothermal junctions**

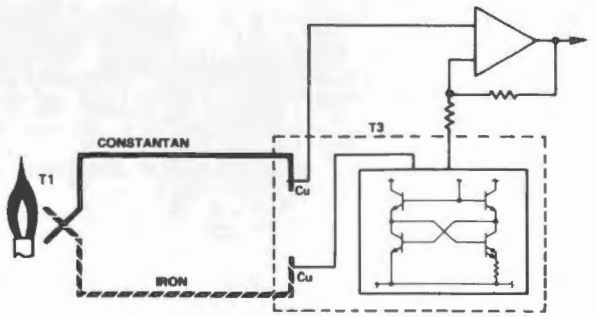


Table 1. **Output voltages v. thermocouple temperature. (Ta = 25°C; V_S = –5V, +15V).**

Thermocouple temperature °C	Type K voltage mV	AD595AD output mV	Thermocouple temperature °C	Type K voltage mV	AD595AD output mV
–200	–5.891	–1454	500	20.640	5107
–180	–5.550	–1370	520	21.493	5318
–160	–5.141	–1269	540	22.346	5529
–140	–4.669	–1152	560	23.198	5740
–120	–4.138	–1021	580	24.050	5950
–100	–3.553	– 876	600	24.902	6161
– 80	–2.920	– 719	620	25.751	6371
– 60	–2.243	– 552	640	26.599	6581
– 40	–1.527	– 375	660	27.445	6790
– 20	– .777	– 189	680	28.288	6998
– 10	– .392	– 94	700	28.128	7206
0	0	2.7	720	29.965	7413
10	.397	101	740	30.799	7619
20	.798	200	750	31.214	7722
25	1.000	250	760	31.629	7825
30	1.203	300	780	32.455	8029
40	1.611	401	800	33.277	8232
50	2.022	503	820	34.095	8434
60	2.436	605	840	34.909	8636
80	3.266	810	860	35.718	8836
100	4.095	1015	880	36.524	9035
120	4.919	1219	900	37.325	9233
140	5.733	1420	920	38.122	9430
160	6.539	1620	940	38.915	9626
180	7.338	1817	960	39.703	9821
200	8.137	2015	980	40.488	10015
220	8.938	2213	1000	41.269	10209
240	9.745	2413	1020	42.045	10400
260	10.560	2614	1040	42.817	10591
280	11.381	2817	1060	43.585	10781
300	12.207	3022	1080	44.349	10970
320	13.039	3327	1100	45.108	11158
340	13.874	3434	1120	45.863	11345
360	14.712	3641	1140	46.612	11530
380	15.552	3849	1160	47.356	11714
400	16.395	4057	1180	48.095	11897
420	17.241	4266	1200	48.828	12078
440	18.088	4476	1220	49.555	12258
460	18.938	4686	1240	50.276	12436
480	19.788	4896	1250	50.633	12524

Since the compensation is at the reference junction temperature, it is often convenient to form the reference 'junction' by connecting directly to the circuit wiring. So long as these connections and the compensation are at the same temperature no error will result.

Interpreting AD595AD output voltages

To achieve a temperature proportional output of 10mV/°C and accurately compensate for the reference junction over the rated operating range of the circuit, the AD595AD is gain trimmed to match the transfer characteristic of K type thermocouples at 25°C. For a type K output in this temperature range the TC is 40.44μV/°C. The resulting gain for the AD595AD is 247.3 (10mV/°C divided by 40.44μV/°C). In addition, an absolute accuracy trim induces an input offset to the output amplifier characteristic of 11μV for the AD595AD. This offset arises because the AD595AD is trimmed for a 250mV output while applying at 25°C thermocouple input.

Because a thermocouple output voltage is non-linear with respect to temperature, and the AD595AD linearly amplifies the compensated signal, the following transfer functions should be used to determine the actual output voltages:

AD595AD output = (Type K voltage + 11μV) × 247.3

or conversely:

Type K voltage = (AD595AD output / 247.3) – 11μV

Table 1 lists the ideal AD595AD output voltages as a function of Celsius temperature for type K British Standard thermocouples, with the package and reference junction at 25°C. As is normally the case, these outputs are subject to calibration, gain and temperature sensitivity errors. Output values for intermediate temperatures can be interpolated, or calculated using the output equations and B.S. thermocouple voltage tables referred to zero degrees Celsius.

Functional description

The AD595AD behaves like two differential amplifiers. The outputs are summed and used to control a high-gain amplifier, as shown in Figure 4.

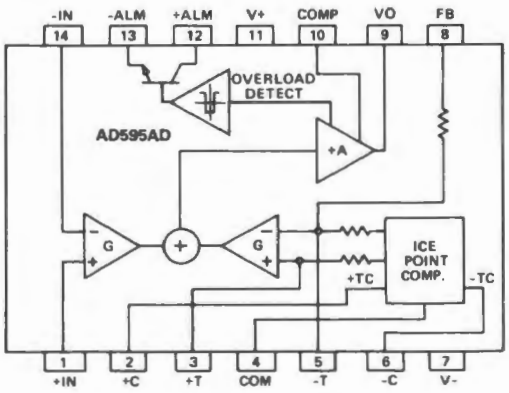


Figure 4 **AD595AD Block diagram**

In normal operation the main amplifier output, at pin 9, is connected to the feedback network, at pin 8. Thermocouple signals applied to the floating input stage, at pins 1 and 14, are amplified by gain G of the differential amplifier and are then further amplified by gain A in the main amplifier. The

output of the main amplifier is fed back to a second differential stage in an inverting connection. The feedback signal is amplified by this stage and is also applied to the main amplifier input through a summing circuit. Because of the inversion, the amplifier causes the feedback to be driven to reduce this difference signal to a small value. The two differential amplifiers are made to match and have identical gains, G. As a result, the feedback signal that must be applied to the right-hand differential amplifier will precisely match the thermocouple input signal when the difference signal has been reduced to zero. The feedback network is trimmed so that the effective gain to the output, at pins 8 and 9, results in a voltage of 10mV/°C of thermocouple excitation.

In addition to the feedback signal, a cold junction compensation voltage is applied to the right-hand differential amplifier. The compensation is a differential voltage proportional to the Celsius temperature of the AD595AD. This signal disturbs the differential input so that the amplifier output must adjust to restore the input to equal the applied thermocouple voltage.

The compensation is applied through the gain scaling resistors so that its effect on the main output is also 10mV/°C. As a result, the compensation voltage adds to the effect of the thermocouple voltage a signal directly proportional to the difference between 0°C and the AD595AD temperature. If the thermocouple reference junction is maintained at the AD595AD temperature, the output of the AD595AD will correspond to the reading that would have been obtained from amplification of a signal from a thermocouple referenced to an ice bath.

The AD595AD also includes an input open circuit detector that switches on an alarm transistor. This transistor is actually a current-limited output buffer, but can be used up to the limit as a switch transistor for either pull-up or pull-down operation of external alarms.

The ice point compensation network has voltages available with positive and negative temperature coefficients. These voltages may be used with external resistors to modify the ice point compensation and recalibrate the AD595AD as described in the next column.

The feedback resistor is separately pinned out so that its value can be padded with a series resistor, or replaced with an external resistor between pins 5 and 9. External availability of the feedback resistor allows gain to be adjusted, and also permits the AD595AD to operate in a switching mode for set-point operation.

CAUTIONS:
The temperature compensation terminals (+ C and −C) at pins 2 and 6 are provided to supply small calibration currents only. The AD595AD may be permanently damaged if they are grounded or connected to a low impedance.

The AD595AD is internally frequency compensated for feedback ratios (corresponding to normal signal gain) of 75 or more. If a lower gain is desired, additional frequency compensation should be added in the form of a 300pF capacitor from pin 10 to the output at pin 9. As shown in Figure 5 an additional 0.01μF capacitor between pins 10 and 11 is recommended.

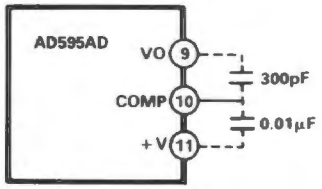


Figure 5 **Low gain frequency compensation**

Recalibration principles and limitations
The ice point compensation network of the AD595AD produces a differential signal which is zero at 0°C and corresponds to the output of an ice referenced thermocouple at the temperature of the chip. The positive TC output of the circuit is proportional to Kelvin temperature and appears as a voltage at +T. It is possible to decrease this signal by loading it with a resistor from +T to COM, or increase it with a pull-up resistor from +T to the larger positive TC voltage at +C. Note that adjustments to +T should be made by measuring the voltage which tracks it at −T. To avoid destabilizing the feedback amplifier the measuring instrument should be isolated by a few thousand ohms in series with the lead connected to −T.

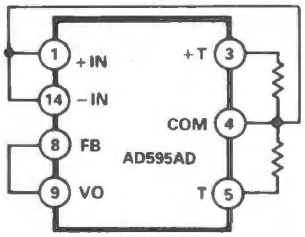


Figure 6 **Decreased sensitivity adjustment**

Changing the positive TC half of the differential output of the compensation scheme shifts the zero point away from 0°C. The zero can be restored by adjusting the current flow into the negative input of the feedback amplifier, the −T pin. A current into this terminal can be produced with a resistor between −C and −T to balance an increase in +T, or a resistor from −T to COM to offset a decrease in +T.

If the compensation is adjusted substantially to accommodate a different thermocouple type, its effect on the final output voltage will increase or decrease in proportion. To restore the nominal output to 10mV/°C the gain may be adjusted to match the new compensation and thermocouple input characteristics. When reducing the compensation the resistance between −T and COM automatically increases the gain to within 0.5% of the correct value. If a smaller gain is required, however, the nominal 47kΩ internal feedback resistor can be paralleled or replaced with an external resistor.

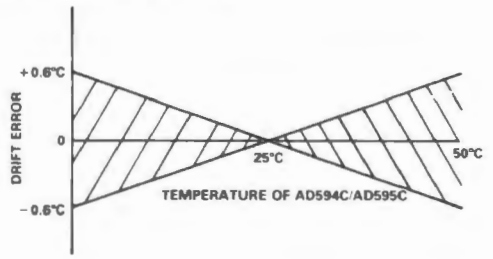
Fine calibration adjustments will require temperature response measurements of individual devices to ensure accuracy. Major reconfigurations for other thermocouple types can be achieved without seriously compromising initial calibration accuracy, so long as the procedure is done at a fixed temperature using the factory calibration as a

reference. It should be noted that intermediate recalibration conditions may require the use of a negative supply.

Using type T thermocouples with the AD595AD
Because of the similarity of thermal EMFs in the 0 to 50°C range between type K and type T thermocouples, the AD595AD can be directly used with both types of inputs. Within this ambient temperature range the AD595AD should exhibit no more than an additional 0.2°C output calibration error when used with type T inputs. The error arises because the ice point compensator is trimmed to type K characteristics at 25°C. To calculate the AD595AD output values over the recommended −200 to 350°C range for type T thermocouples, simply use British Standard thermocouple voltages referred to 0°C and the output equation given on page 3 for the AD595AD. Because of the relatively large non-linearities associated with type T thermocouples the output will deviate widely from the nominal 10mV/°C. However, cold junction compensation over the rated 0 to 50°C ambient will remain accurate.

Stability over temperature
Each AD595AD is tested for error over temperature with the measuring thermocouple at 0°C. The combined effects of cold junction compensation error, amplifier offset drift and gain error determine the stability of the AD595AD output over the rated ambient temperature range. Figure 7 shows an AD595AD drift error envelope. The slope of this figure has units of °C/°C.

Figure 7 **Drift error vs. temperature**

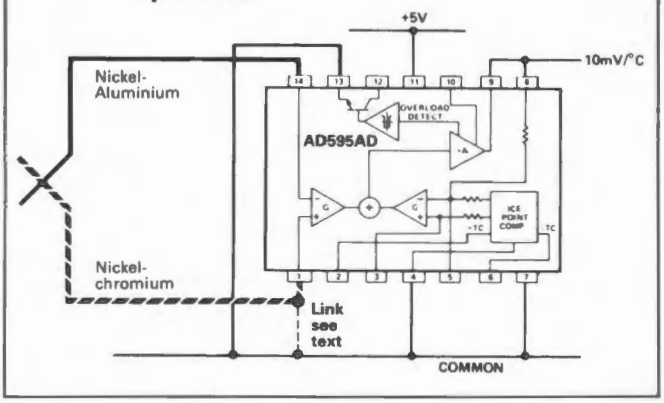


Thermal environment effects
The inherent low power dissipation of the AD595AD and the low thermal resistance of the package make self-heating errors almost negligible. For example, in still air the chip to ambient thermal resistance is about 80°C/Watt. At the nominal dissipation of 800μW the self-heating in free air is less than 0.065°C. Submerged in fluorinert liquid (unstirred) the thermal resistance is about 40°C/Watt, resulting in a self-heating error of about 0.032°C.

Single and dual supply connections
The AD595AD is a completely self-contained thermocouple conditioner. Using a single +5V supply the interconnections shown in Figure 8 will provide a direct output from a type K thermocouple measuring from 0 to +300°C.

Any convenient supply voltage from +5V to +30V may be used, with self-heating errors being minimized at lower supply levels. In the single supply configuration the +5V supply connects to pin 11 with the V– connection at pin 7 strapped to power and signal common at pin 4. The thermocouple

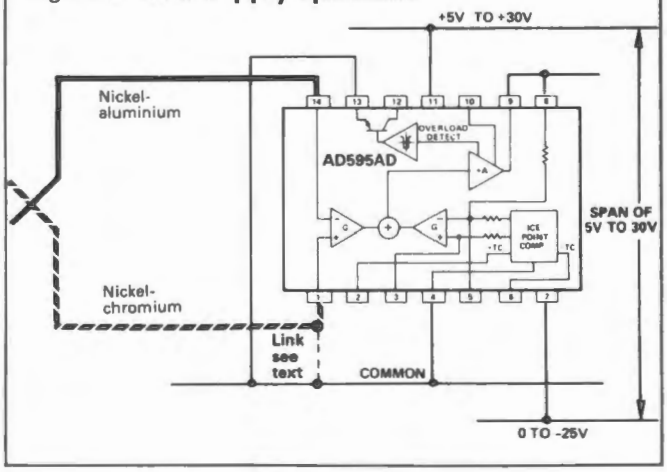
Figure 8 **Basic connection, single supply operation**



wire inputs connect to pins 1 and 14 either directly from the measuring point or through intervening connections of similar thermocouple wire type. When the alarm output at pin 13 is not used it should be connected to common or –V. The precalibrated feedback network at pin 8 is tied to the output at pin 9 to provide a 10mV/°C nominal temperature transfer characteristic.

By using a wider ranging dual supply, as shown in Figure 9 the AD595AD can be interfaced to thermocouples measuring both negative and extended positive temperatures.

Figure 9 **Dual supply operation**



With a negative supply the output can indicate negative temperatures and drive grounded loads or loads returned to positive voltages. Increasing the positive supply from 5V to 15V extends the output voltage range well beyond the +1100°C temperature limit recommended for type K thermocouples.

The common-mode voltage on the thermocouple inputs must remain within the common-mode range of the AD595AD, and a return path provided for the bias currents. **If the thermocouple is not remotely grounded, then the dotted line connection in Figures 8, 9 and 11 must be made.**

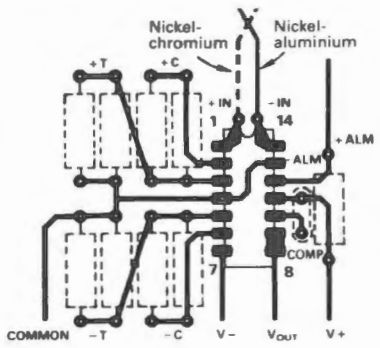
A low value resistor may be needed in this connection to ensure that common mode voltages induced in the thermocouple loop are not converted to normal mode.

Thermocouple connections
The isothermal terminating connections of a pair of thermocouple wires form an effective reference junction. **This junction must be kept at the same**

temperature as the AD595AD for the internal cold junction compensation to be effective.

A method that provides for thermal equilibrium is the printed circuit board connection layout illustrated in Figure 10.

Figure 10 **PCB connections**



Here the AD595AD package temperature and circuit board are thermally contacted in the copper printed circuit board tracks under pins 1 and 14. The reference junction is now composed of a copper-nickel/chromium connection and copper-nickel/aluminium connection, both of which are at the same temperature as the AD595AD.

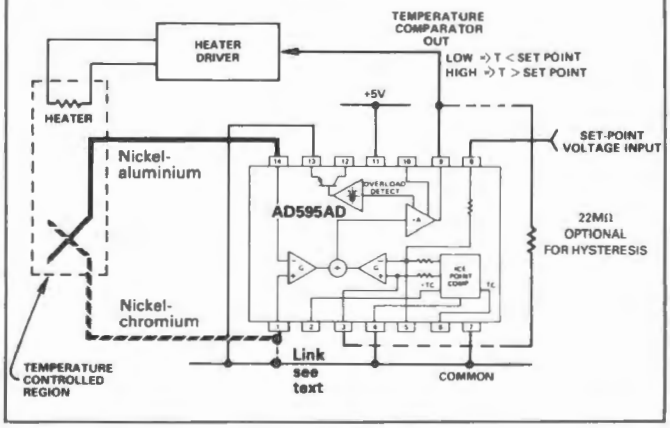
The printed circuit board layout shown also provides for placement of optional alarm load resistors, recalibration resistors and a compensation capacitor to limit bandwidth.

To ensure secure bonding the thermocouple wire should be cleaned to remove oxidation prior to soldering.

Set-point controller

The AD595AD can readily be connected as a set-point controller as shown in Figure 11.

Figure 11 **Set-point controller**



The thermocouple is used to sense the unknown temperature and provide a thermal EMF to the input of the AD595AD. The signal is cold junction compensated, amplified to 10mV/°C and compared to an external set-point voltage applied by the user to the feedback at pin 8. Table 1 lists the correspondence between set-point voltage and temperature, accounting for the nonlinearity of the measurement thermocouple. If the set-point temperature range is within the operating range (–55°C to +125°C) of the AD595AD, the chip can be used as the transducer for the circuit by shorting the inputs together and utilizing the nominal calibration of 10mV/°C. This is the Celsius thermometer configuration as shown in Figure 15.

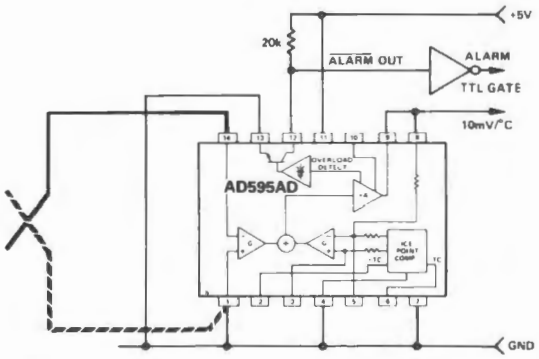
In operation if the set-point voltage is above the voltage corresponding to the temperature being measured the output swings low to approximately zero volts. Conversely, when the temperature rises above the set-point voltage the output switches to the positive limit of about 4 volts with a +5V supply. Figure 11 shows the set-point comparator configuration complete with a heater element driver circuit being controlled by the AD595AD toggled output. Hysteresis can be introduced by injecting a current into the positive input of the feedback amplifier when the output is toggled high.

Alarm circuit

In all applications of the AD595AD the –ALM connection, pin 13, should be constrained so that it is not more positive than (V+) –4V. This can be most easily achieved by connecting pin 13 to either common at pin 4 or V– at pin 7. For most applications that use the alarm signal, pin 13 will be grounded and the signal will be taken from +ALM on pin 12. A typical application is shown in Figure 12.

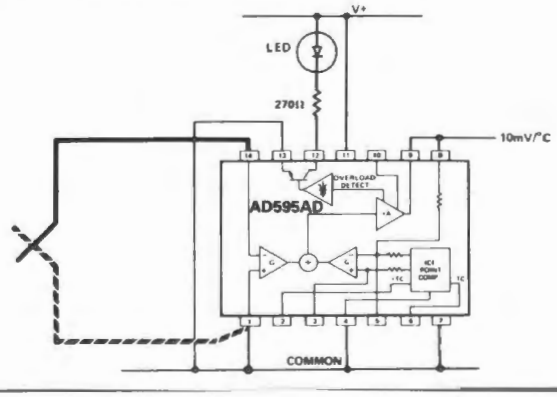
In this configuration the alarm transistor will be off in normal operation and the 20k pull up will cause the +ALM output on pin 12 to go high. If one or both of the thermocouple leads are interrupted, the +ALM pin will be driven low. As shown in Figure 12 of this signal is compatible with the input of a TTL gate which can be used as a buffer and/or inverter.

Figure 12 **Using the alarm to drive a TTL gate ('grounded' emitter configuration)**



Since the alarm is a high level output it may be used to directly drive an LED or other indicator as shown in Figure 13.

Figure 13 **Alarm directly drives LED**



A 270Ω series resistor will limit current in the LED to 10mA, but may be omitted since the alarm output transistor is current limited at about 20mA. The transistor, however, will operate in a high dissipation mode and the temperature of the circuit will rise well above ambient. Note that the cold junction compensation will be affected whenever the alarm circuit is activated. The time required for the chip to return to ambient temperature will depend on the power dissipation of the alarm circuit, the nature of the thermal path to the environment and the alarm duration.

The alarm can be used with both single and dual supplies. It can be operated above or below ground. The collector and emitter of the output transistor can be used in any normal switch configuration. As an example a negative referenced load can be driven from –ALM as shown in Figure 14.

The collector (+ALM) should not be allowed to become more positive than (V–) +36V, however, it may be permitted to be more positive than V+. The emitter voltage (–ALM) should be constrained so that it does not become more positive than 4 volts below the V+ applied to the circuit.

Additionally, the AD595AD can be configured to produce an extreme upscale or downscale output in applications where an extra signal line for an alarm is inappropriate. By tying either of the thermocouple inputs to common most runaway control conditions can be automatically avoided. A +IN to common connection creates a downscale output if the thermocouple opens, while connecting –IN to common provides an upscale output.

Figure 14 **ALM driving a negative referenced load**

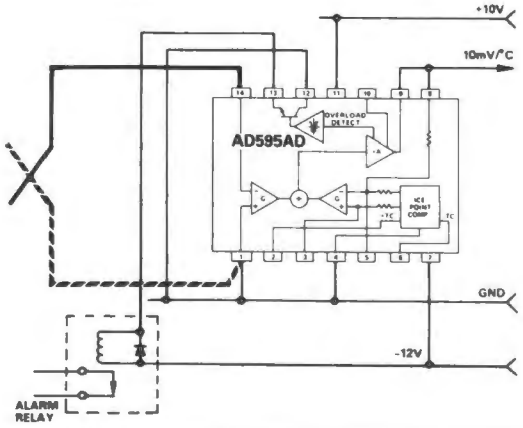
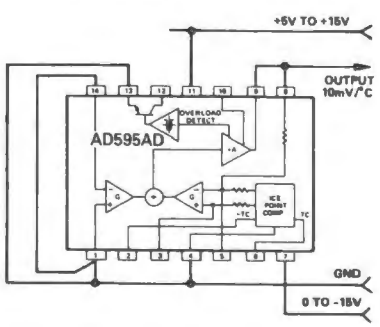


Figure 15 **AD595AD as a stand-alone Celsius thermometer**



Celsius thermometer

The AD595AD may be configured as a stand-alone Celsius thermometer as shown in Figure 15.

Simply omit the thermocouple and connect the inputs (pins 1 and 14) to common. The output now will reflect the compensation voltage and hence will indicate the AD595AD temperature with a scale factor of 10mV/°C. In this three terminal, voltage output, temperature sensing mode, the AD595AD will operate over the full military –55°C to +125°C temperature range.

RS data

R.S. Components Ltd. 13-17 Epworth Street, London, EC2P 2HA
Telephone: 01-250 4000
For technical enquiries ring: 01-202 8252 or 0536-201234
An Electrocomponents Group Company

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RS data

Heating cable

Stock number 378—246

RS Cut to length heat tracing system

The RS Heater Cable enables any industrial user to have simple and effective heat available to him in an extremely flexible form to suit the most simple or the most unusual application.

Although primarily used for pipe tracing the heater cable has innumerable applications, a number of which are detailed in this Data Sheet.

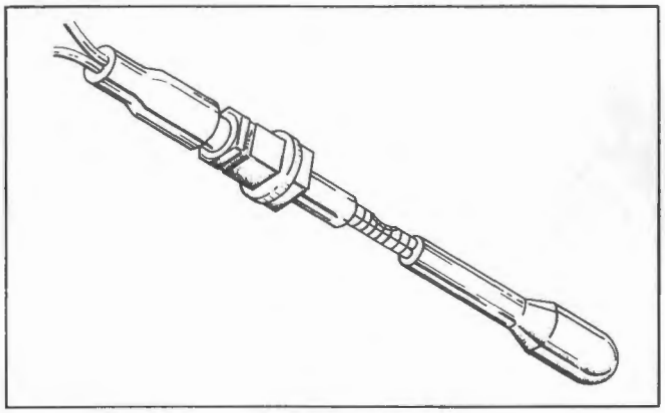
The RS Heater cable enables the user to cut and terminate as simply as any power cable.

In fact, the heater cable is both a power cable and a heating device in one. It is extremely simple to terminate and very flexible with circuit length down to 0.75m, and with suitable series connections in excess of 100m.

The system can be used for both internal and external heating.

Features

- Cut to any length
- Easy to terminate
- Suitable for internal and external heating applications
- Manufactured to BS 6351



Specification

Location	Non hazardous areas

Construction

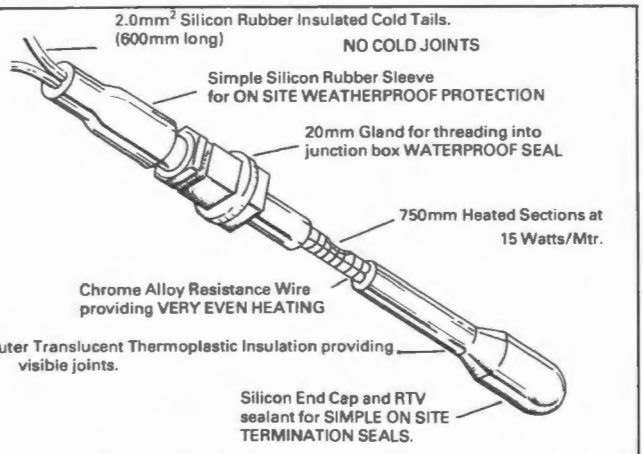
Core	$2mm^2$ copper braid
Electrical Insulation	silicon rubber
Heater element	chrome alloy resistance wire
Outer sheath	PVC extrusion
Dimensions	8mm x 5mm
Bus bar interval	750mm

Terminations

Far End Seal	silicon end cap and sealant
Cold lead end seal	2 separate silicon rubber sleeves and silicon sealant
Cold lead	Up to 700mm silicon insulated
Rating	15 watts/m

Withstand temperature (non-operative)

Maximum	100°C
Minimum	–20°C
Maximum pipe temperature	40°C
Supply voltage as standard	240V



MAX PIPE TEMPERATURE	WITHSTAND TEMPERATURES
40°C – 15 Watts/Mtr.	MAX 100°C MIN –20°C
MAX CIRCUIT LENGTH	
190m	

Fig. 1

Pipe tracing and design

To enable pipes to maintain their required operating temperature, it is not sufficient merely to insulate the pipe through which they flow but the heat loss must be replaced through the pipe surface.

The RS heater cable provides a simple economical means of replacing the heat loss either by straight tracing or by spiralling around the pipe and is suitable at temperatures between –20°C and +80°C, which makes it ideal for freeze protection of water pipes. It is also suitable for use at maintaining pipes at up to 40°C.

Freeze protection

Table 1 provides details of the loadings required to freeze protect pipelines at differing ambient temperatures. By reading off the spiral ratio chart you can determine the exact quantity of thermotape needed to freeze protect the pipe in question, i.e. a 6in bore pipe 13m long has to be frost protected at an ambient temperature of – 10°C. From Table: 21W/m required. Therefore total loading required = 13 x 21 = 273 Watts at 15W/m the length of cable needed = $\frac{273}{15}$ = 18.2m.

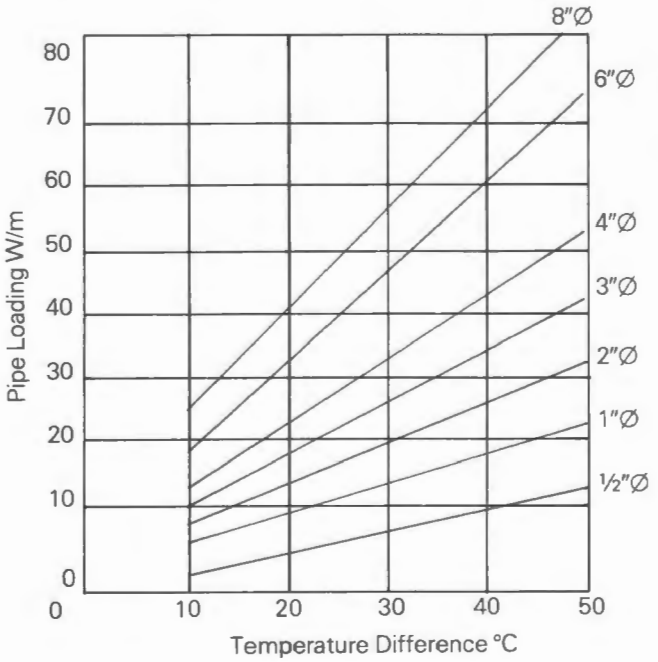
As each Zone is 750mm, length of heater cable will be 18.75m with up to 750mm cold tail.

Maintain duty

The graph below should be used to identify the loading required to maintain the temperature of the process material inside the pipeline. Note the thermotape should only be used to maintain pipe temperatures up to 40°C, i.e. a 4in bore pipe 7m long is to be traced at 25°C with an ambient of –5°C. The temperature difference is 30°C. From the graph: a loading of 36W/m will be required. Thus total loading required is 36 x 7 = 252 Watts. Length of cable needed = $\frac{252}{15}$ = 16.8m.

As each Zone is 750mm, length of heater cable will be 17.25m to be spiralled around the pipe, and up to 750mm cold tail.

Low temperature maintaining duty



The above graph is based upon 1in thermal insulation similar to mineral wool with K factor 0.05W/m°C.

	Pipe Dia	mm	15	25	40	50	75	100	150	200
		ins	½	1	1½	2	3	4	6	8
Ambient –10°C	Loading W/m		5	7	9	10	12	14	21	26
	Spiral Ratio		1:1	1:1	1:1	1:1	1:1	1:1	1.5:1	1.7:1
Ambient –20°C	Loading W/m		7	10	13	15	19	23	33	42
	Spiral Ratio		1:1	1:1	1:1	1:1	1.3:1	1.6:1	2.2:1	2.8:1

Table 1.

For other insulation thicknesses the loading from the graph should be multiplied by the insulation factors below.

Insulation factors

Insulation Thickness	Ins	½	1	1½	2	3
	mm	12	25	35	50	75
Factor x Heat Loss		2	1	0.6	0.5	0.35

Plastic pipes
Note where plastic pipes are to be traced the maximum maintain temperature should be 20°C.

In all cases including freeze protection surface capillary thermostats are to be used (see Control Section).

Installation Section

Terminations (RS533-639)
Each termination kit is supplied with comprehensive instructions.

The heater is cut to the exact length required leaving up to 600mm for the cold tail connection at the one end and a 25mm section at the other end to seal off the cable off. The actual joint can be visibly seen and identified through the translucent outer sheath material.

The heater cable has the same loading along its complete length with a bus bar spaced every 750mm; thus we have equal sectional loadings of approximately 11½W every 750mm.

The heater cable is terminated at its far end with the aid of a silicon rubber mould and a small amount of silicon compound applied over the conductors and slid over the heater cable.

At the mains connection the two bus bar connections are split and two separate silicon rubber tubes are slid over the bus bars and cable, providing a perfect seal in conjunction with a suitable nylon compression gland (RS 542-172).

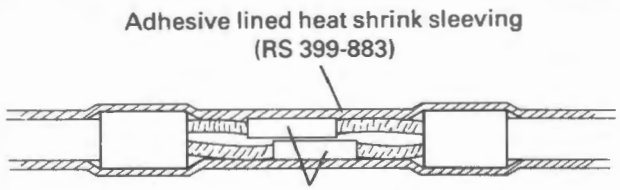


Fig. 2

In line joints
Where the 20m length of heating cable is insufficient to complete the heating cable requirements, two lengths can be joined together. The individual bus bars should be crimped with the aid of the insulated butt crimps (RS 532-945) and then the two sections of cable should be shrunk together with the aid of adhesive lined heat shrink sleeving (RS 399-883) see fig. 2.

Fixing materials
For freeze protection a suitable PVC insulating tape (RS 511-910) should be used to fix the heater cable to the pipe concerned.

For processing temperature applications above 20°C we would recommend the use of aluminium foil fixing tape 2in (50mm) wide fitted along the line of the heater cable itself. This will aid heat transfer and reduce operating temperature of the heater cable.

Straight tracing
The heater cable is fitted to the pipe along its underside, see fig. 3. The fixing tape (RS 511-910) should hold the cable in question against the pipe at ½m intervals.

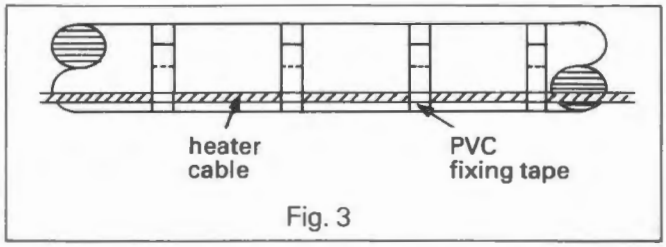


Fig. 3

Spiralling
For spiralling the heater cable on to the pipe ensure that even pitch centres are used (this will be where the length of heater cable is in excess of the length of pipe line), see fig. 4. For freeze protection the spiral pitch centres are shown in Table 1.

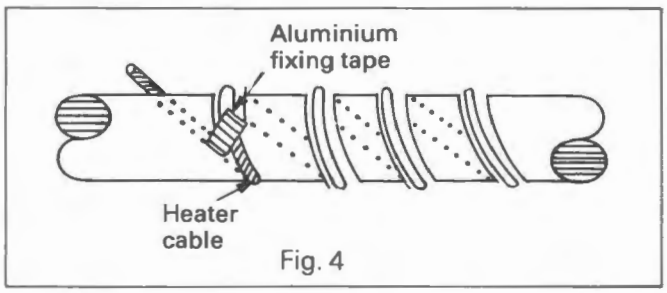


Fig. 4

Mains connection
One of the advantages of the RS heater cable system is that one can connect up to the incoming mains by joining into any part of the heater cable at the bus bars. There is therefore a facility to make T-joints with the aid of a suitable junction box and to make connections at any part of the cable.

Controls
It is essential that the heater cable is provided with suitable temperature controls. This will ensure:

(a) The heater cable is only switched on when required.

(b) Life of the heater cable is prolonged.

(c) That the heater cable does not overheat.

(d) That energy costs are kept to a minimum.

Freeze protection
For freeze protection a straightforward air thermostat is the simplest form of temperature control. Because the heater cable has automatic cold tails, these tails can be wired directly into the thermo-

RS data

stat, or alternatively, the air thermostat is positioned separate from the heater and can be interwired via a junction box back to the heater.

In all cases the thermostat should be positioned in the coldest location. A suitable thermostat would be RS 333-596 (air thermostat in weatherproof housing) but the temperature must be set to 4°C.

In the case of the tracing of plastic pipes, however, air thermostats should not be used even for freeze protection (refer to capillary thermostats).

Process temperatures
Where it is necessary to maintain a product at its correct handling temperature, it is essential that a thermostat sensor is directly fitted to the pipe surface, adjacent to the heater cable for straight tracing and beneath the heater cable for spiralling. A capillary thermostat should preferably have a stainless steel capillary and bulb with the switch mechanism in a housing separated from the pipe by a suitable pipe bracket.

This type of thermostat should also be used whenever plastic pipes have to be traced.

Applications
The number of applications for the heater cable are innumerable. To give an indication of the number of these we are listing below different types of applications within individual industries.

Application – always beneath 40°C maintenance temperature	
Food Processing	Glacial Acetic Acid Caustic Soda Glycerine Vegetable Oils Liquid Glucose
Freeze Protection	Water Lines Sprinkler Systems Hydrant Water Mains Agricultural Lines and Farms Car Wash Plants Industrial Showers Fire Mains
Refrigeration	Cold Room Defrosts Cold Store Doors Defrost Drain Lines
Fuel Oil	High Viscosity Fuel Oils Storage Tanks
General Use	Low Temperature Gas Lines Chemical Lines – 'Glycol' Anti-condensation/prevention
Drink Manufacture	Beer Vats Small Wine Processing
Ancillary Heating	Underfloor Heating Gutter Heating Snow Melting Roof De-icing Seed Propagation Soil Heating Low Temperature Laboratory Projects
Transport	Fuel Lines on Aircraft Diesel Tanker Supply Lines Water Supply Lines on Board Ship.

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RS data

Bucket-brigade delay line TDA 1022

Stock number 302-031

In the electronic production and reproduction of music and speech, artificial delay has many potential applications. In electronic organs, for example, it can be used to introduce vibrato and chorus effects. In playing back recorded music it can be used to simulate reverberation, restoring the spatial presence that is often deliberately avoided in the recording studio. It can improve the intelligibility of announcements broadcast over multiple loudspeakers in large halls or public gathering places. And it can even be used to restore the natural timbre and pitch of speech played back faster or slower than the speed at which it was recorded.

For some applications of artifical delay, various expedients have gained a limited acceptance. These include magnetic discs and loops, tape recorders with multiple heads, and metal springs and plates. In general, though, the best of these are too expensive or too specialized for common use, and the performance of the cheaper and less specialized is too limited.

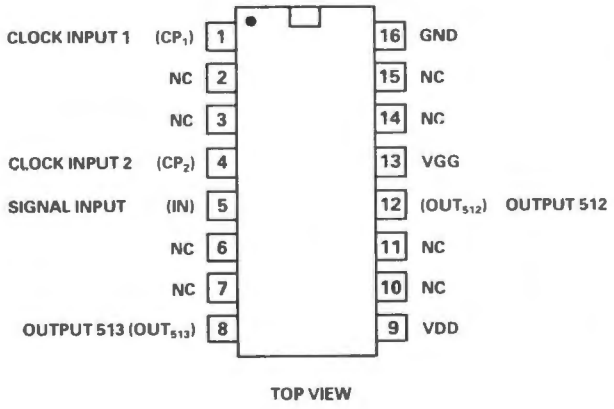
The TDA1022 is a MOS monolithic integrated circuit, generally intended to delay analogue signals. The device contains 512 stages and can provide delays from 51.2 ms to 0.853 ms when used with clock frequencies in the range 5 kHz to 300 kHz (e.g. delay time $512/2f_{CP}$).

Absolute maximum ratings

Voltage range for all pins,
with respect to GND (pin 16) _____ 0 to −20V
Current into any input or output _____ ± 10mA
Operating temperature range _____ −20 to +60°C
Storage temperature range _____ −40 to +150°C

Features

- Analogue delays from 51.2 to 0.512 ms.
- Easily cascadeable for greater delays.
- D.C. to 45 kHz input frequency range.
- 512 stages.
- Ideally suited for generating musical effects.
- More compact than mechanical delay systems.



CAUTION
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Operating conditions $T_{amb} = -20$ to $+60°C$

Parameter	symbol	min.	typ.	max.	unit
Negative supply voltage	$-V_{DD}$	12	–	16	V
Tetrode gate voltage	V_{GG}	–	$V_{DD}+1$	–	V
Clock voltage HIGH	V_{CPH}	0	–	–1,5	V
Clock voltage LOW	V_{CPL}	–	V_{DD}	–	V
Clock input capacitance	C_{CP}	–	–	200	pF
Clock frequency	f_{CP}	5	–	300	kHz
Clock pulse width (see note 1)	t_{CPW}	–	–	$0,5 \times T_{Cp}$	
Clock rise/fall time (see note 1)	t_r, t_f	–	$0,05 \times T_{CP}$	500	ms
Clock cross point	V_x	0	–	–3	V
Signal input frequency	f_{IN}	0	–	$0,32 \times f_{CP}$ or 45	kHz
DC input bias voltage (see note 2)	$-V_{INbias}$	4,5	–	6,5	V
Load resistance (see note 3)	R_L	10	50	–	kΩ

Characteristics

$T_{amb} = 25°C$; $-V_{DD} = -V_{CPL} = 15V$; $V_{CPH} = 0V$; $-V_{GG} = 14V$; $R_L = 50k\Omega$

Parameter	symbol	min.	typ.	max.	unit
Signal input voltage swing (rms value) at $f_{CP} = 40kHz$; $f_{IN} = 1kHz$; total harmonic distortion at output = 2%	V_{IN}(rms)	–	–	2	V
Attenuation from input to output at $f_{CP} = 40kHz$; $f_{IN} = 1kHz$	A	1	3,5	6	dB
Change in attenuation when f_{CP} varies from 5kHz to 100kHz at $f_{IN} = 1kHz$; V_{IN}(rms) = 1V	$\triangle A$	–	0,5	1	dB
change when f_{CP} varies from 100kHz to 300kHz	$\triangle A$	–	0,5	1	dB
DC output voltage shift when f_{CP} caries from 5 to 300kHz	$\triangle V_{OUT}$	–	–	0,5	V
Output noise voltage (rms value) at $f_{CP} = 100kHz$; weighted according to IEC 173 (A-curve)	V_{no}(rms)	–	0,2	0,4	mV
Signal-to-noise ratio at $f_{CP} = 100kHz$; weighted according to IEC 173 (A-curve)	S/N	–	83	–	dB

Note 1: T_{CP} = period time $1/f_{cp}$ (see also Figure 5)

2: Adjust V_{IN} bias for minimum distortion.

3: Attenuation can be reduced to typically 2.5dB, if the load resistor is replaced by a current source of 100 to 400μA.

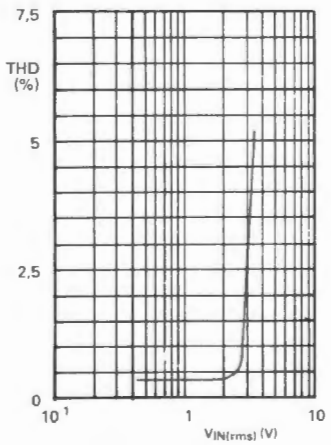


Figure 1. **Total harmonic distortion (THD) as a function of input voltage (rms value) at $-V_{DD} = 15V$; $-V_{GG} = 14V$; $f_{IN} = 1kHz$; $-V_{CP} = 15V$; $t_{CP} = 40kHz$; $R_L = 47k\Omega$; V_{IN} biased at –5,2V dc for class A operation.**

Introduction to the bucket-brigade delay line

To characterise an analogue signal of B hertz completely, at least 2B samples per second are needed. If these are stored in the stages of a kind of shift register then the attractive features of the shift register – especially as a delay line – can be used for analogue signal handling.

Sampled values of the analogue signal are stored in the form of charges on a series of capacitors. Between successive capacitors is a switch that transfers the charge from one capacitor to the next on command of a clock pulse. By analogy with the old fire-fighting method, in which buckets of water were passed along the line from man to man, a delay line of this sort is known as a bucket-brigade.

Since each capacitor cannot take up a new charge until it has passed on its previous one, only half the capacitors carry information and the ones in between are empty. Starting from the condition shown in Figure 2(a), the transfer proceeds in two stages:

in the first, bucket 1 empties into bucket 2, and bucket 3 into bucket 4;

and in the second, bucket 2 empties into bucket 3, and bucket 4 into bucket 5.

Two antiphase clock signals are required; one to govern the emptying of even-numbered, and the other of odd-numbered buckets.

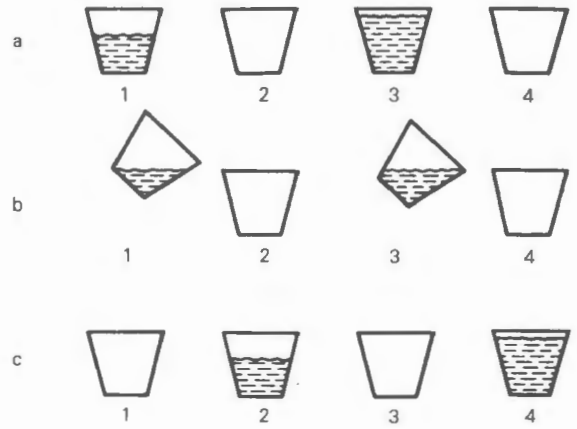


Figure 2 **Sample transfer in a bucket-brigade, simplified scheme. Samples in buckets 1 and 3 (a) are poured into empty buckets 2 and 4 (b); thus, the samples move step by step from left to right (c).**

There is a practical drawback to the scheme illustrated in Figure 2. The buckets in which the samples are stored must empty completely during each transfer. In practice, the buckets are capacitors and the samples are charges on them. Owing to leakage current, complete discharge is difficult to ensure. So instead, the scheme illustrated in Figure 3 is adopted.

Figure 3(a) represents the initial condition; buckets 2 and 4 are full, and samples are stored in buckets 1 and 3. During the first transfer, bucket 2 fills bucket 1, and bucket 4 fills bucket 3. What remains in bucket 2 is then equal to the original contents of bucket 1, and what remains in bucket 4 is equal to the original contents of bucket 3. During the next transfer, bucket 3 fills bucket 2, and bucket 5 fills bucket 4. Thus, as the buckets empty from right to left, the sampled quantities move, as before, from left to right; that is, from input to output. This is the scheme used in a practical bucket-brigade delay line.

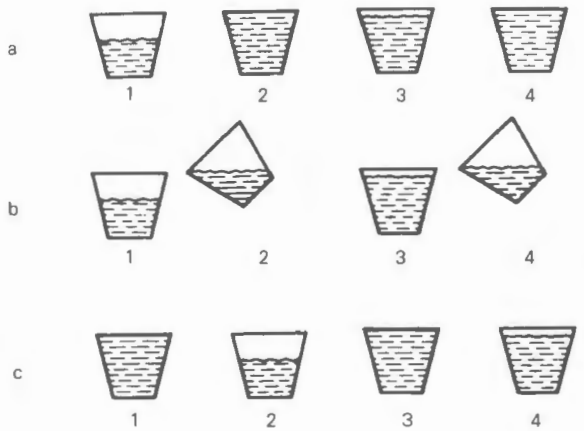


Figure 3 **Sample transfer in a bucket-brigade, practical scheme. Buckets 1 and 3 contain samples (a); when full buckets 2 and 4 are poured into them (b), the sample quantities move, as before, from left to right (c).**

Bucket-brigade delay line as an integrated circuit

A bucket-brigade delay line based on discrete components would be impracticable. Even at the low frequencies encountered in audio applications, the number of storage capacitors and switches needed to give any reasonable delay would be prohibitive. The alternative is therefore integration, and the most advantageous technology is MOS.

Figure 4 shows the circuit of the TDA1022, an integrated bucket-brigade having 512 delay stages. The transistors of which it is made up are p-channel enhancement-mode MOS, which means that the clock signals, CP1 and CP2, must be negative with respect to earth.

When clock signal CP1 goes negative, the input transistor connects the sampling capacitor C_2 to the analogue input signal at pin 5. As long as the transistor conducts, the voltage across the capacitor tracks the voltage at pin 5, so the sample ultimately stored in the capacitor is the signal voltage at the instant when CP1 goes positive and the transistor ceases to conduct. The sample is shifted into the first 'bucket' capacitor, C_1, when CP2 goes negative, and from the first to the second when CP1 again goes negative.

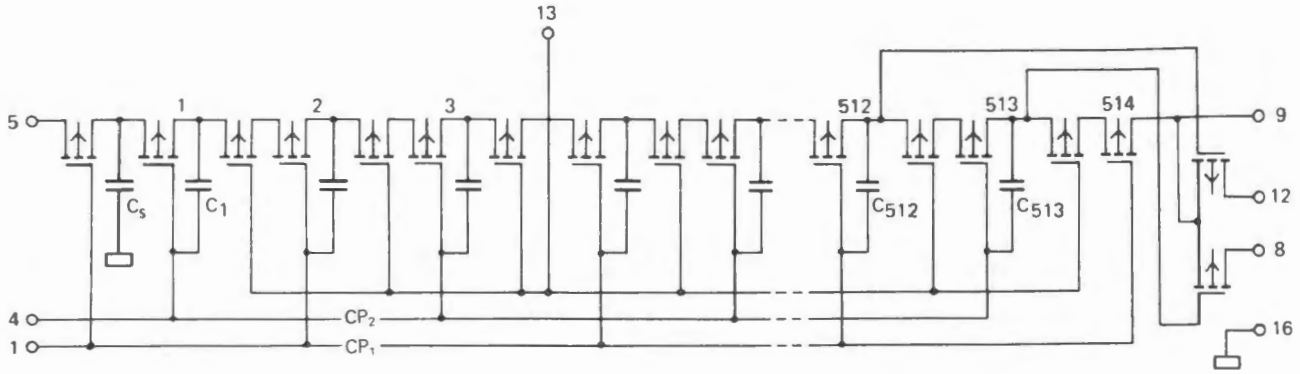


Figure 4 **TDA 1022 integrated bucket-brigade delay line.**

If the output of the delay line were to be taken direct from the 512th stage, its envelope would be as shown in Figure 5(a), where the clock frequency is fully present. Strong low-frequency filtering would be required and the filters would be expensive because their characteristics would have to be very steep-sided to ensure adequate bandwidth. Precautions would also have to be taken about restoring the sampled amplitudes of low-frequency signals, for heavy filtering would distort the higher audio frequencies.

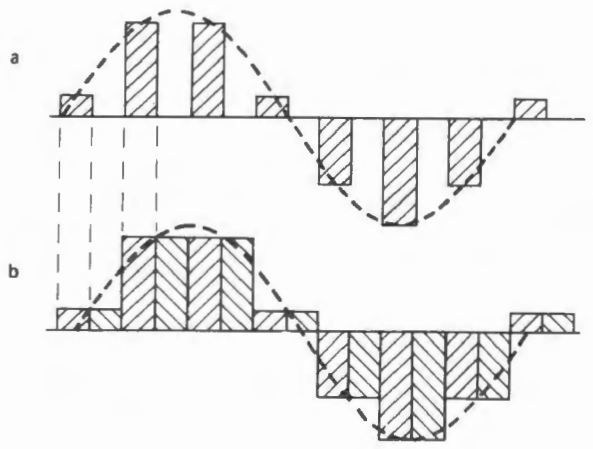


Figure 5 **(a) Envelope of clocked pulse samples requires strong low-pass filtering to suppress clock-frequency. (b) Supplementing main output by half-clock-period delayed pulses restores continuity and simplifies filtering.**

To avoid these problems the TDA 1022 is split into two paths after the 511th stage. One path goes from the 512th stage to the output buffer connected to pin 12 (see Figure 4); and the other goes via a 513th stage, giving an extra half-clock-period delay, to the output buffer connected to pin 8. Summing the outputs at pins 8 and 12 gives the envelope shown in Figure 5(b).

The delay obtainable, t, is given by

$$t = \frac{n}{2f_{\phi}}$$

where n is the number of stages and f_{CP} is the clock frequency ($f_{CP} = f_{CP}1 = f_{CP}2$). Since the TDA 1022 is designed for operation at clock frequencies from 5 kHz to 300 kHz, the delay obtainable from a single device (effectively 512 stages) is 51.2 ms to 0.853 ms.

The timing diagram of the clock pulses is shown in Figure 6. Clock pulse voltage level HIGH is 0 to −1.5 V and LOW is −10 V to −18 V (typ. $-V_{DD}$). Rise and fall times are typically 0.05T, where T is the period, $1/f_{CP}$. The clock pulse width should be equal to or less than 0.5 T.

The TDA 1022 is designed for input signal frequencies from 0 to 0.32 x f_{CP} at levels up to 2 V r.m.s. (5.6 V peak-to-peak). The highest signal frequency to be delayed, f_{max} imposes a further limitation on the delay obtainable. To characterize the signal completely, the sampling rate must be at least $2f_{max}$; however, to avoid sideband interference a higher rate is required, at least $3f_{max}$. Thus, if f_{max} is, say, 10 kHz, the clock frequency must be at least 30 kHz. The maximum delay obtainable from a single TDA 1022 is then

$$t = \frac{512}{2 \times 30 \times 10^3} = 8.53\,\text{ms}.$$

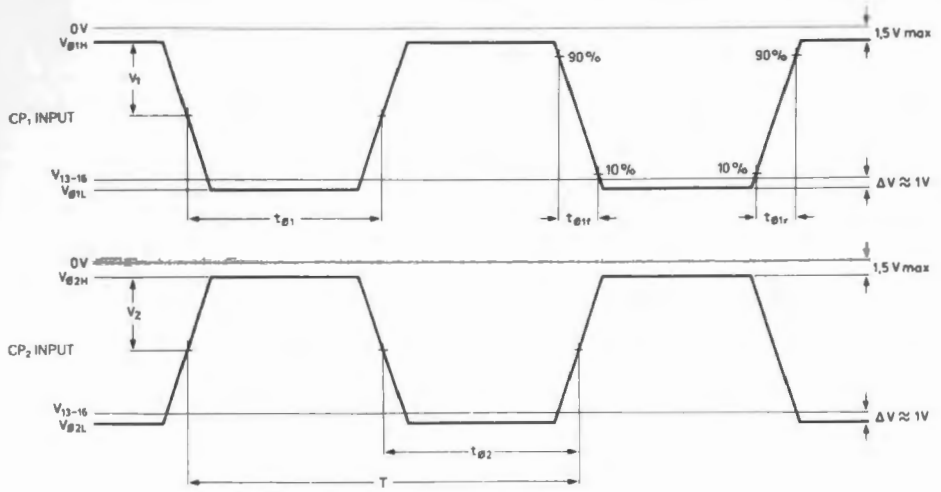


Figure 6 **Clock pulse timing diagram for the TDA 1022.**

For greater delays, additional TDA1022s must be cascaded. However, shorter delays, down to the 0.512ms minimum, can be obtained merely by increasing the clock frequency. The d.c. shift over all stages of the TDA1022 is less than 0.5V as the clock frequency is varied between 5 and 300kHz.

A feature of the TDA1022 is its low attenuation. When a resistive load of 47kΩ is used, the attenuation is typically 4dB; when the load resistor is replaced by a current sink of 100μA to 400μA, it is only 2.5dB, as shown in Figure 7. This makes it possible to connect a number of TDA1022s in cascade without undue losses.

Applications information

Figure 8 shows the TDA1022 used as a simple delay line. The delayed signal is fed to a low pass fitter with a cut-off frequency of 15kHz that is used to remove the sampled nature of the waveform. With a 50kHz clock frequency a delay of 5.12ms is produced. Longer or shorter delays may be generated by altering the clock frequency however to maintain the same degree of filtering the break point of the filter must be changed correspondingly.

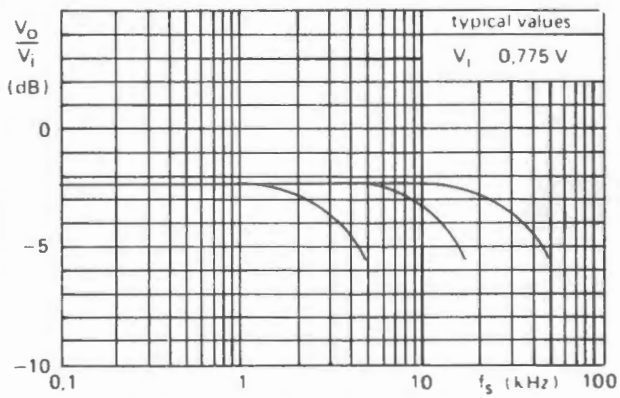
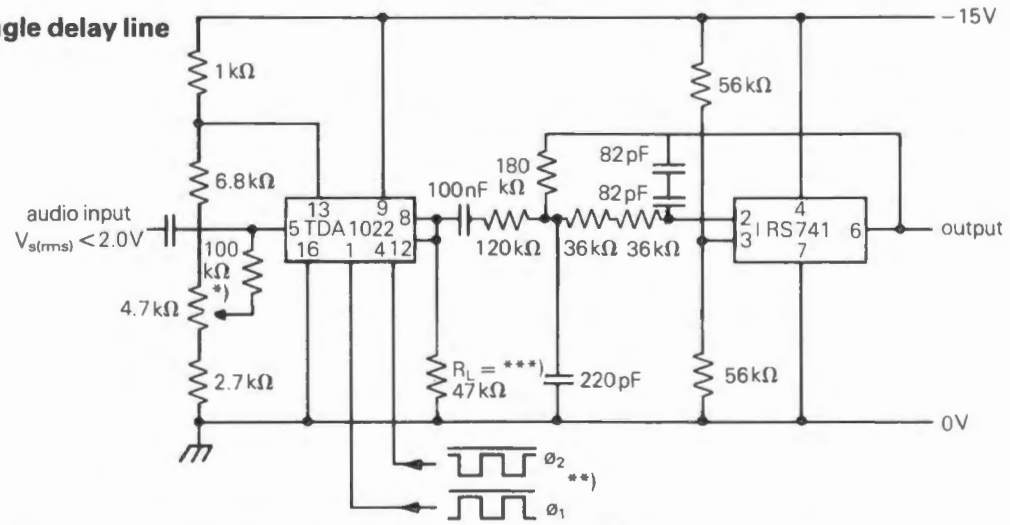


Figure 7 **Attenuation characteristic of the TDA1022 at: $V_{DD} = -15V$, tetrode gate voltage $V_{13-16} = -14V$, $V_ø = -15V$, load resistor replaced by current sink.**

Longer delays may be produced by cascading two or more TDA1022s as shown in Figure 8. Both devices are run from the same clock. To prevent voltage offsets from adding each device is biassed separately with the input a.c. coupled.

Figure 8 **Single delay line**



*) Adjust d.c. voltage for class-A operation (≈ 5V).

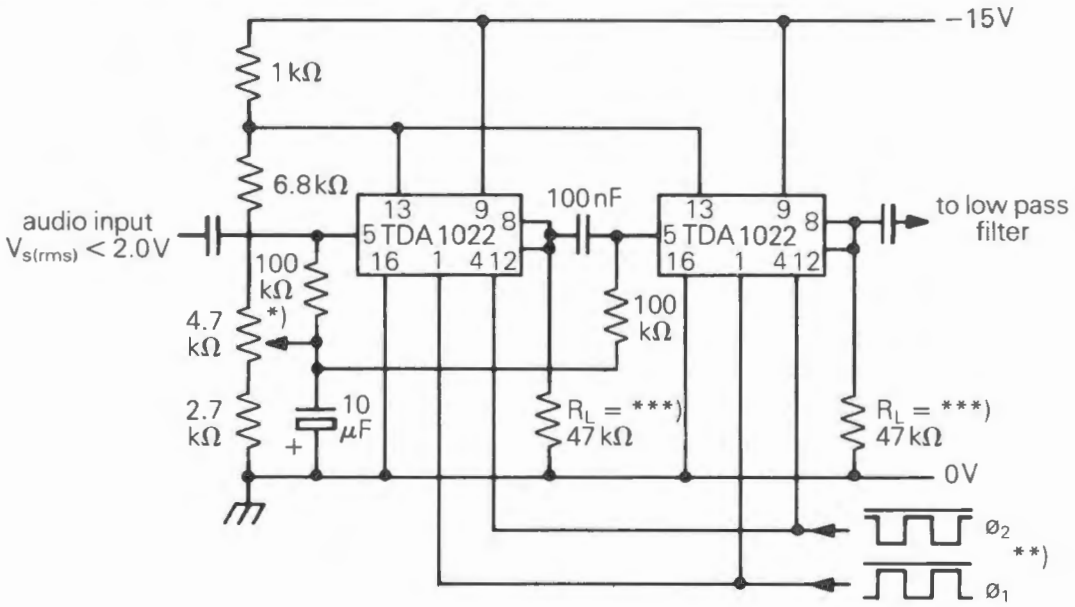
Conditions: low pass filter RS741 (12dB per octave); gain = +3.5dB (compensation for line attenuation); f_{CP} = 50kHz (min.); cut-off frequency = 15kHz.

**) Clock input voltage amplitude: $V_{CL} = -15V$.

***) Can be replaced by a current source of 100 to 400μA (see also note 3 on page 2).

RS data

Figure 9 **Series connection of two delay lines**

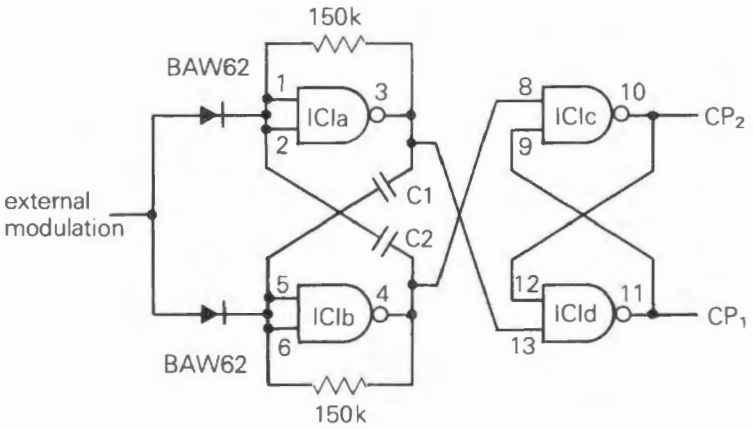


*) Adjust d.c. voltage for class-A operation (≈ 5V).

**) Clock input voltage amplitude: $V_{CL} = -15V$.

***) Can be replaced by a current source of 100 to 400 µA (see also note 3 on page 2).

Longer delays may be produced by cascading two or more TDA1022s as shown in Figure 9. Both devices are run from the same clock. To prevent voltage offsets from adding each device is biassed separately with the input a.c. coupled.



f_{Cp} (kHz)	$C_1 = C_2$ (pF)
15	470
30	220
60	100

Figure 10 **Clock oscillator which can be modulated by external voltages (e.g. for vibrato); using quadruple 2-input NAND gates 4011B (ICIa-d).**

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RS data

Two zone alarm control panel

Stock number 346-586

The RS alarm control panel incorporates all the features required to form the nucleus of a complete security system for all types of premises. The fully auto resetting panel controls a five circuit, two zone (one switchable) system with memory. It includes a 24 hour anti-tamper loop for maximum security, these five circuits are suitable for use with all RS four wire sensors and other security products. The control panel facilities include a personal attack circuit, and a separate entry-exit circuit with independently adjustable exit and entry timers, adjustable bell cut-off timer, internal audible buzzer and full alarm status indication on the front panel.

The control panel meets the requirements of BS4737: Part 1 ('Intruder alarm systems in buildings') and is fitted with an anti-tamper switch, and security key switch supplied with two keys: additional keys are not available for security reasons.

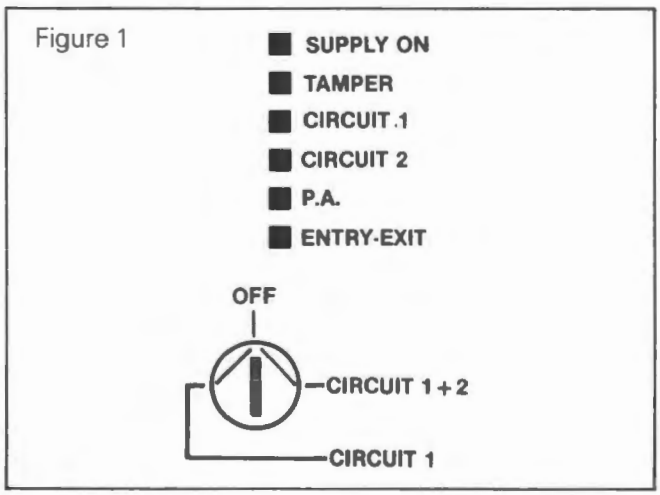
The control panel is totally self-contained, operates from a 240V ac supply and has the facility to charge a 12V sealed lead acid back-up battery such as RS 12V, 3Ah dryfit, 591-938.

Features

- Totally self contained.
- Five circuit, two zone system.
- 24 hour anti-tamper loop.
- Personal attack circuit.
- Separately adjustable entry/exit timers.
- Full status indication on front panel.

Front panel controls

Figure 1



Supply on
The 'supply on' indicator illuminates only when the mains voltage is present.

Tamper
The 'Tamper' indicator illuminates (and latches) whenever the tamper circuit is in Fault/Alarm condition.

Circuit 1
The 'Circuit 1' indicator illuminates whenever Circuit 1 is in Fault/Alarm condition.

Circuit 2
The 'Circuit 2' indicator illuminates whenever Circuit 2 is in Fault/Alarm condition.

P.A. (Personal Attack)
The P.A. indicator illuminates (non-latching) whenever the P.A. is in Fault/Alarm condition.

Entry/Exit
The Entry/Exit indicator illuminates whenever the Entry Circuit is operated, and latches in Alarm condition.

Keyswitch
The Keyswitch is supplied with 2 keys (spare keys are not provided for security reasons). The Keyswitch selects the control function; it does not switch the mains supply or 12V supply to the control board, the keys are removable in all positions.

Guide to installation

Draw a plan of the building to be protected and decide on the location of the control panel, detection devices and bell housing.

The control panel should be sited as near as practicable to the usual point of entry and, if possible, it should not be conspicuous.

Detection devices will vary depending on the layout of the building. However, the most likely point of unauthorised entry (usually at the back of buildings or places of easy access where an intruder can 'work' without being noticed) should be particularly well protected as should areas containing articles of high value. Ideally design your system to detect the intruder as early as possible, on entry rather than after entry. It is also worthwhile to protect internal doors as intruders nearly always move around as soon as they have gained entry. Internal protection devices are especially useful if the layout of the building makes it difficult to protect the exterior thoroughly. All the detection devices on your system can function in any one of three modes, i.e.

1. Entry/Exit.
2. 'Circuit 1 + 2' key position.
3. 'Circuit 1' key position (circuit 2 or Exit/Entry circuit are not on in this position).

Decide in which one of these three modes you want each detection device to work. On setting the control panel there is no delay on any circuit except for the 'Entry/Exit' circuit and therefore the 'Entry/Exit' circuit should include all detectors that could be used during authorised 'Entry/Exit', even if only very occasionally.

The main bell should be mounted outside, where it can be seen and heard. Normally it should be mounted where it is not accessible without a ladder. Also it is good practice to run the cable to the bell straight through the wall at the back of the bell housing so that the cable is not exposed. To comply with BS4737: Part 1 the cabling to the main bell should be monitored for open or short circuit, this can be achieved by using the RS Self Activating Bell Module, 301-577.

The total output current capacity of the RS control panel is 1 amp therefore it is essential that the total load drawn by the complete system, in full alarm condition does not exceed the rating of the power supply. Ideally it should not run at more than 80% of maximum i.e. 800 mA.

Many false alarms are caused by poor joints wrapped in insulation tape. To satisfy the British Standard a tamper-proof junction box or a soldered joint (sleeved with heat shrink sleeving) should be used when making connections to the master detection circuit.

If you use ultrasonics, passive infra red or similar devices, refer to the manufacturer's instructions for wiring. However, in almost all cases, a 12V supply (taken from ±12V terminals) to the unit is required. In this case, in addition to two supply wires, a further 4 wires, (2 tamper wires and two which form the alarm loop) are required. Therefore a six core cable should be used.

Functional description

Figure 2 **P.C.B. layout**

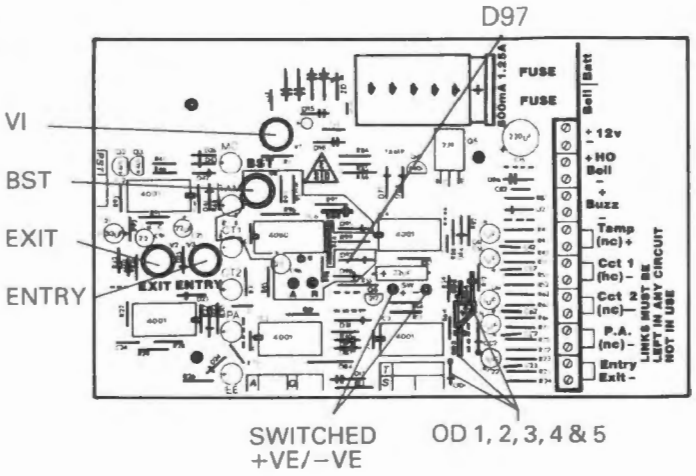


Table 1 **Main terminal block**

12V auxiliary supply	±
Sounders output	+ve (fused 800ma) −ve (switched in alarm)
To buzzer	+ve −ve (switched)
Tamper	+ve N/C detection circuit (operative in all key positions)
Circuit 1	−ve N/C detection circuit (operative in both 'ON' key positions)
Circuit 2	−ve detection circuit (operative in one key position)
P.A.	−ve N/C detection circuit
Entry/Exit	−ve N/C detection circuit (operative in one key position)

Tamper circuit

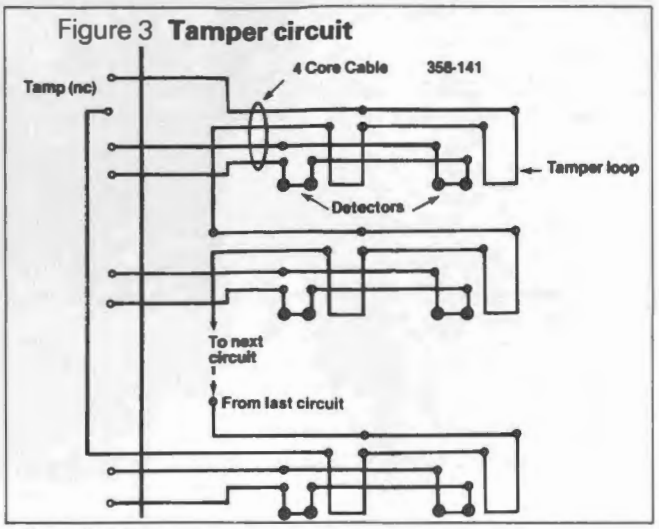
This loop is the 'monitor' circuit to be run with all the other detector circuits. The Tamper Circuit is of positive (+ve) polarity.

Breaking of the Tamper loop results in an 'alarm' condition. This loop is always 'active' irrespective of the key position, but the alarm condition varies according to the key position, i.e.

Circuit 1	Bell alarm and buzzer sounding.
Circuit 1 and 2	
OFF	Buzzer only.

The tamper circuit may be reset and the buzzer silenced by turning the control key on and off again. Remember – all wiring loops going into any one detection circuit must all be wired in series (see Figure 3). The main alarm bell should also be included in the tamper circuit.

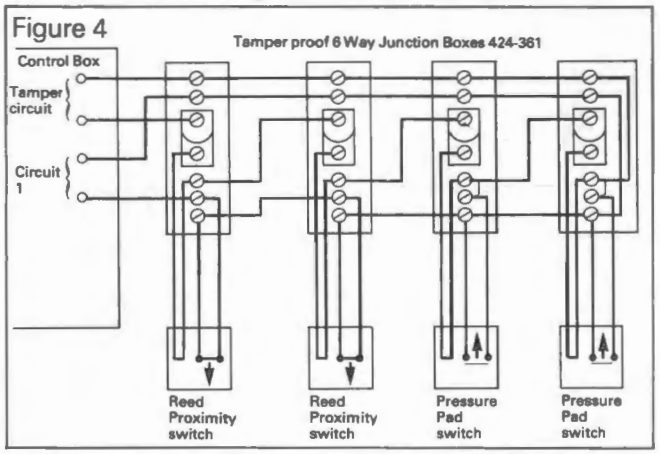
Figure 3 **Tamper circuit**



Circuit 1

The protection of this zone is achieved through two loops; the tamper loop, and a switch loop circuit 1. This four wire zone may be used in conjunction with detection devices such as pressure pad switches, reed proximity switches, etc., in any combination, see Figure 4 for an example.

Figure 4



Note how in the example shown above the tamper circuit is continuous and the normally closed reed switch is connected in the switch loop. The normally open pressure mat switch is connected between the tamper loop and the switch loop circuit 1.

Full alarm condition will result:

1. When an o/c appears in the tamper loop (bell and buzzer sounding)
2. When an o/c appears in the circuit loop (bell only sounding)
3. When an s/c appears between Circuit 1 and tamper (bell only sounding).

Circuit 2

Affords the same protection as Circuit 1 and the same type of detection devices may be used.

Full alarm conditions will result:

1. When an o/c appears in the tamper loop (bell and buzzer sounding)
2. When an o/c appears in the circuit loop (bell only sounding)
3. When an s/c appears between Circuit 2 and tamper (bell only sounding).

Circuit 2 has the extra facility of being front panel switchable, allowing circuit 1 to be operated in isolation.

NB

a) The Key switch only controls the switch loop Circuit 2, it does not switch the tamper circuit which remains active in either position.

b) Memory. The detection circuits have a separate LED indication so that the control panel identifies the first circuit to trip. This valuable feature enables the user to establish which part of the system was activated first. To clear memory turn the control to 'Circuit 1 and 2' then 'OFF' with key.

P.A. (Personal attack)

The protection of this zone differs from all the others in as much as breaking of the P.A. circuit loop will activate the alarm irrespective of the control key position, (even in the 'OFF' position).

The Alarm output, in key-off position, is non-latching, so a latching P.A. switch is recommended. P.A. switches should be N/C and wired in series, like the N/C reed switches. When using a latching P.A. switch the bell is not controlled by the bell stop timer and will therefore ring continuously until the switch is delatched. If the P.A. circuit is activated in either Key-on position using a non-latching switch the bell will ring for the duration set by the bell stop timer and the P.A. circuit will then reset.

Note: After the P.A. circuit has been activated in one of the control on positions the control panel needs to be reset by returning the Key switch to the 'off' position and returning to the desired control setting.

Entry/Exit

The Entry/Exit circuit may be wired in the same manner as Circuit 2 and the same type of detection devices may be used. The variable resistor marked 'Exit' sets the Exit delay. This delay should be set to allow adequate time to leave the premises after arming the alarm. The variable resistor marked 'Entry' sets the Entry delay. This delay should be set to allow adequate time to reach and disarm the panel on an authorised entry. Both delays are adjustable from 0-2 minutes.

Operation: during Exit the buzzer will sound (duration set by 'Exit' variable resistor). When the final exit door is closed and the exit time has expired the buzzer will cease to sound.

Upon entry the buzzer will sound (duration set by 'Entry' variable resistor) until the control panel is turned off. If the panel is not turned off before this period has expired it will sound the full alarm.

The Entry/Exit is not functional in Key position 'Circuit 1' (please refer to Function Options).

All detection circuits

If any N/C detection circuit is not to be used the short circuit link should be left in the terminals.

Stabilized supply

13.5V dc (nominal) is available at the terminals marked ±12V for auxiliary equipment. The total system requirement should not exceed 1 amp. It is important that if a dryfit battery is used an open circuit voltage or 13.65V dc should not be exceeded. When adjustment is required the voltage should be set by variable resistor V1.

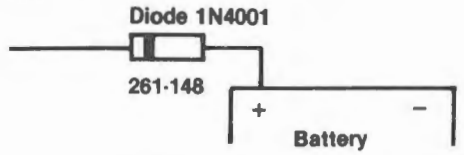
Rechargeable back-up battery

Should be connected to the flying leads provided Red +ve Black −ve. The back-up battery provides for all circuits including the Auxiliary Output in the event of mains failure. The size of battery should be chosen to have sufficient capacity for 8 hours normal operation without external power.

Non-rechargeable back-up battery

A 12V non-rechargeable back-up battery may be used by connecting a 1A diode in series with the positive lead to the battery (see Figure 5). The initial nominal capacity of the primary battery should be sufficient for 36 hours normal operation including 2 hours operation in the alarm condition without external power.

Figure 5



Fuses

Mains	Providing power for the transformer	1A
Bell	Providing power for the bell	800mA
Battery	Providing power for the battery	1.25A

Sounders

Connect the Bells/Sounders to the Bell Terminals. The +ve (HO) Terminal is fused (800ma). The –ve Terminal switches –ve in alarm.

Alarm output duration timer

Adjusting the variable resistor (BST) determines the alarm duration time, once this time has expired the alarm output will shut down and the control panel can only be reset by the key. The time is adjustable from 0 to 45 minutes. One-third adjustment is approximately 20 minutes. Note: visual indication on the front panel remains.

Auto reset (pins A,R)

By linking pins A to R and removing option diodes (OD) 3, 4, and 5 Auto reset will result. After the alarm duration time the control will reset itself and accept another alarm trip, providing all the circuits are closed. If a circuit is open the operation will be as a standard alarm duration timer.

Continuous Bells – Remove D97 and the alarm duration timer will not function.

Self activating bell (S.A.B.)

When using the RS Self Activating Bell Module it should be securely fixed to the interior of the bell box and wired in accordance with Figure 6. The bell and S.A.B. module must be wired with a minimum of five conductors, the RS 6 core signal cable (359-914) is ideal for this purpose. For bell circuits wired without an anti-tamper circuit the S.A.B. module should be wired as shown in Figure 7 which uses the tamper switch to break the 'hold off' signal.

Figure 6

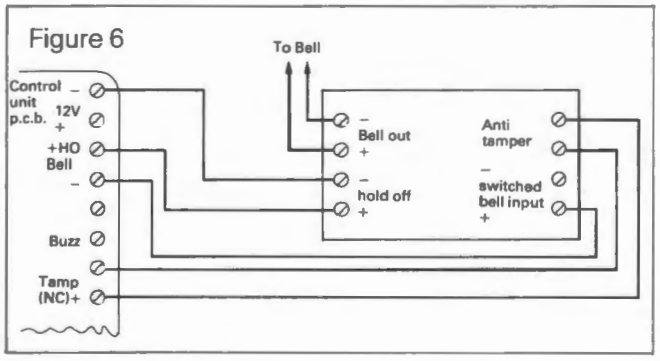
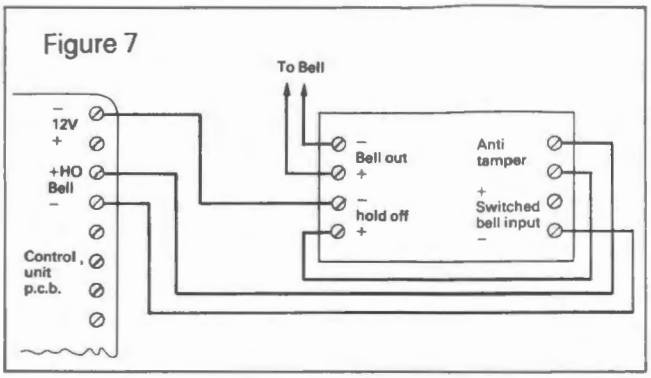


Figure 7



Ultrasonic and passive infra-red detectors

Ultrasonic and passive infra-red detectors are extremely reliable units that operate by safe and well proven techniques. In many cases, especially where there are large doors or windows which can be difficult to protect in other ways, they offer a far greater degree of security than would otherwise be possible and can eliminate a lot of unnecessary wiring.

However the following points should be borne in mind:

a) Whenever you are using volumetric devices ensure the power supply is regulated.

b) When using a latching detector a switched positive or negative is available from the printed circuit board of the control panel. See Figure 2.

c) Remember that ultrasonics are most sensitive to an object moving towards them while passive infra-reds are most sensitive to objects crossing the beam tangentially. Actual range will depend on the unit you are using (see specifications with the unit) but typically a passive infra-red device has an angle of 90° while an ultrasonic has an angle of 120°.

d) Certain types of environment are hostile to ultrasonics. These include any powerful air currents (from ducted air central heating, fans etc.); powerful draughts (strong enough to make curtains sway for example); telephone bells within the range of the sonic; open fires; pets; letters coming through a letter-box etc. Where possible mount ultrasonics so that none of these are present within the range, or at least turn down the sensitivity/environmental control, following closely the instructions supplied with the unit. (RS data sheet 5257.)

e) When using passive infra-reds bear in mind they should not be subjected to bright sunlight or rapid changes in temperatures. Also the ray should not be directed at an open fire.

Function options

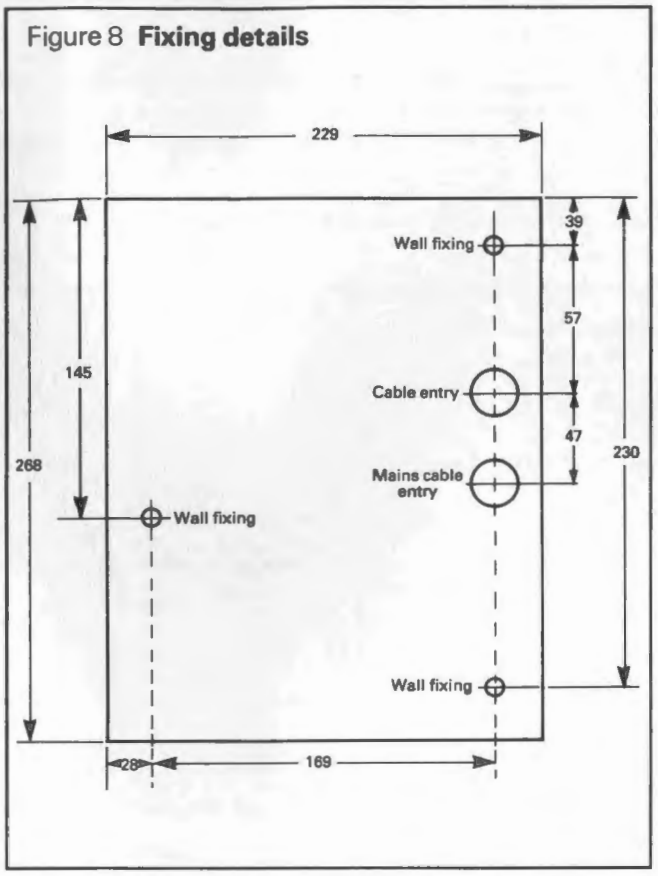
Circuit 2. To have Circuit 2 functional in both 'key on' positions, remove OD2.

Entry/Exit. To have Entry/Exit functional in both 'key on' positions, remove OD1.

Mounting details

The control box should be mounted within the building to be protected (see Figure 8). It is recommended that the control box is mounted on an internal wall close to the point of entry, but not visible from the outside of the building.

Figure 8 **Fixing details**



Testing and maintenance

A programme of routine testing is described in BS4737 Part 1 Section 1.2, and this should be strictly adhered to. The minimum testing and maintenance required is as follows:

Every 12 months or 6 months if primary batteries are used;

1. Check the installation, location and siting of all equipment and devices against the record.
2. Check the satisfactory operation of all detection devices, including deliberately-operated devices.
3. Inspect all flexible connections against the relevant requirements.
4. Check that the normal and stand-by power supplies are functioning and appear to be in order.
5. Check the control equipment and service it in accordance with the alarm company's procedure.
6. Check the satisfactory operation of every audible alarm and warning device.
7. Check that the intruder alarm system is fully operational.

Fault identification/repair service

The electronics of this product have been carefully designed to be contained on a single printed circuit board. If you suspect a fault with the alarm control panel then it should only be necessary to return the P.C.B. assembly to RS for repair/exchange (see the latest RS catalogue for details). Before returning the P.C.B. assembly it is advisable to test the control panel in isolation. This is best done by removing the field wiring and replacing it with wire links to all the detector circuits (see Figure 2). Should it prove to be functioning correctly then each field circuit can be tested by replacing them in succession.

Should the P.C.B. assembly need returning it is easily removed as follows:

a) Isolate mains supply.
b) Remove the mains fuse within the control panel.
c) Disconnect the battery.
d) Remove all field wiring from the terminal block.
e) Remove the transformer secondary from the terminal block.
f) Unplug the key switch.
g) Remove the three screws securing the P.C.B. assembly.

The P.C.B. assembly may now be removed and packed carefully for returning to the RS repair department together with the 'Repair/Exchange' form.

Associated security products

It is recommended that the RS alarm control panel is used in conjunction with products specifically designed for security applications. This data sheet has been written assuming RS security products have been used throughout. A list of suitable security products is given below.

4-core signal cable	358-141
6-core signal cable	359-914
Tamper proof 6 way terminal block	424-361
Flexible jumper loop	424-377
Pressure pad switch	317-140
Flush mounting reed proximity switch	333-158
Flush mounting reed proximity switch	337-396
Surface mounting reed proximity switch	333-192
Surface mounting reed proximity switch	335-536
Roller shutter reed proximity switch	333-170
Window foil	609-994
Window foil make off block	489-330
Surface pass key switch	533-164
Pass key switch	335-952
Security key switch	334-864
Low current A.W.D.	248-404
High output low current A.W.D.	249-924
12-24V dc alarm bell	249-637
Bell enclosure	249-895
Multiple tone siren	249-570
Xenon beacon	565-456
Passive infra-red detector	301-123
Ultrasonic intruder detector	302-479
Rechargeable dryfit battery	591-938
Two tone buzzer	249-429
Self activating bell module	301-577

RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

Digital panel meter module

Stock number 258—041

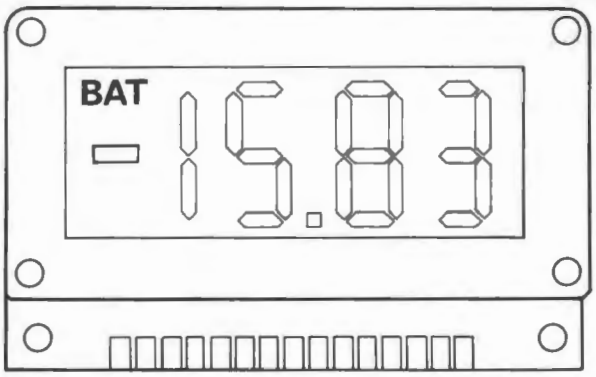
This complete digital panel meter will measure and display up to ±199.9mV directly with an accuracy of ±0.1%. The small size and ultra-low power consumption, with its liquid crystal display makes the module ideal for incorporation into a wide range of equipment, especially battery portable designs.

Features

- Easily fitted to panels
- 3½ digit display
- 12.7mm clear digits
- 7V to 10V operating voltage
- Low battery annuciator
- Optional mounting bezel

Handling precautions

The DPM module contains CMOS devices and must be handled correctly to prevent damage. Input pins should be shorted with conductive foil. Do not make any circuit changes under 'Power On' conditions as high transients may cause permanent damage.



Electrical data

Power supply voltage (V_{DD}, V_{SS})	9V DC nominal (range 7V to 10V)
Supply current (at 9V)	300μA typ, 500μA max
Input sensitivity (RFL, RFH = 100mV)	± 199.9mV full scale
Resolution (RFL, RFH = 100mV)	1 count = 100μV
Accuracy (at 25°C)	± 0.1% of reading ± 1 count
Common mode voltage range (CMVR)	(V_{DD} −1.5V) to (V_{SS} + 1.5V)
Common mode rejection ratio (CMRR)	70dB typ, within CMVR
Maximum input voltage (INLO, INHI)	must not exceed V_{DD} or V_{SS} unless input current is limited to 100μA max
Input impedance	100MΩ
Input leakage current (V_{IN} = 0)	1pA typ, 10pA max
Sampling rate	3 readings per second
Analogue common voltage (COM)	V_{DD} less 2.8V (±0.4V), see CMVR note
Low battery indicator	set to 7.25 ±0.25V
Operating range	0°C to +50°C, R.H. 80% max
Storage range	−20°C to +70°C R.H. 80% max
Temperature coefficient	50ppm per °C typ, 100ppm max

Description

The DVM module is a complete digital panel meter, incorporating the proven 7126 type dual-slope integrating analogue-to-digital converter, with a precision voltage reference and all the necessary circuits to drive the large 3½ digit liquid crystal display. The DVM module also features a battery voltage monitor, which causes a low battery warning (BAT) to be shown on the meter display. This monitor is pre-set to 7.25V but can be adjusted by the single turn control on the back of the meter.

The differential analogue input has a very high impedance and a low leakage current, which gives virtually zero loading on the input signal. Excellent noise performance is provided by the common mode rejection of the A to D converter and the inclusion of an input filter. The input voltage is compared with the high stability internal reference by the A to D converter, and the resulting digital reading is displayed on the LCD display. The internal reference is pre-set to 100mV, which provides a display range of ±199.9mV. A single-turn potentiometer, located on the back of the meter, sets the internal reference voltage.

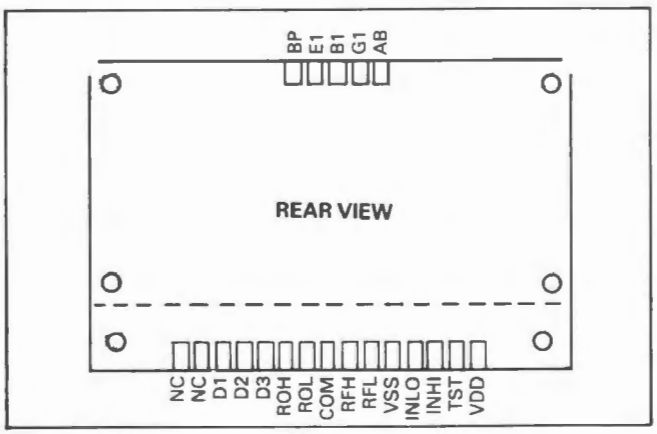
The DPM inputs can be used to measure the ratio between two input voltages connected to INLO, INHI and RFL, RFH. In this mode the internal reference is not required and ROL, ROH are left open. The resultant display reading = (analogue input ÷ reference input voltage) x 1000.

No zero adjustment is required, since the circuit is autozeroing. Input polarity is also automatically detected and displayed. Input over-range is indicated by the blanking of the three right hand digits, giving a display of 1---. Three decimal points are available on the display, and are selectable by making the relevant link connections. An internal oscillator, which controls the A to D functions and the LCD drivers, is preset to give about 3 readings per second for optimum rejection of 50Hz hum pick-up. Outputs are available on the meter for generating, via external logic, the necessary under- and over-range signals for auto-ranging applications.

These meters can be readily mounted behind a panel cut-out using the fixing holes provided. An optional mounting bezel kit is available, where required. All connections are by solder pads, which suit wires or pin connectors.

Connections

V_{DD}, V_{SS}	Power supply: positive to V_{DD}, negative to V_{SS}.
INHI,INLO	Analogue inputs. Display will show negative if INHI is lower potential than INLO. (NB. See note on common mode voltage range.)
ROH, ROL	Internal reference outputs. When ROL is connected to COM, a 100mV reference is available at ROH.
RFH, RFL	Reference inputs. When internal reference is used, link RFH to ROH, and RFL to ROL and COM.
COM	Analogue Common (NB. See note on common mode voltage range.)
D1, D2, D3	Decimal point select. Link relevant pin to V_{DD}; D1 (X.XXX), D2(XX.XX), D3(XXX.X).
TST	Display test. When connected to VDD, reading should be – 1888. **Caution** this will harm display if maintained for more than 30 secs. This pin should also be used as negative supply (1mA max) for external logic gates in auto-ranging applications.
BP, B1 E1, AB, G1	Terminals for generating over-range and under-range outputs.



Mounting Bezel (258-057)

Available as an optional extra, the black ABS moulded bezel with clear acrylic window provides an attractive and convenient mounting method for the digital module.

The bezel is mounted through a single panel cut-out and the DPM module is attached to the bezel by 4 screws through the module mounting holes. Spring clips, retained by the screws, provide firm retention of the bezel/module assembly in the cut-out.

Bezel size	64.5 x 34.5mm
Front projection from panel	6mm max
Panel cut-out	63mm x 32.5mm
Max Panel thickness	3mm

Common Mode Voltage Range (CMVR)

The DVM module is designed to operate from a 9V supply which is normally floating (isolated) with respect to the analogue inputs (INHI & INLO). An analogue common (COM) is provided, which is internally regulated to be about 2.8V (2.4 to 3.2V) below the positive supply. When the inputs are floating, INLO (or INHI) should be linked to this COM reference to set the correct operating conditions for the analogue input amplifier.

Inputs which are not floating with respect to the supply can be accepted *provided* that they are within the CMVR of the input amplifier (that is 1.5V below the positive supply to 1.5V above the negative supply). In this case, COM *must not* be linked to INLO (or INHI), although it should still be connected to ROL if the internal reference is being used. (NB. If either INLO or INHI are taken to V_{DD} or V_{SS}, then the input will be outside its CMVR and the meter may be damaged).

The DVM module can be operated from a 'split power supply' (eg ±5V) which is particularly useful when the analogue input is supplied from an operational amplifier. If this amplifier supply is greater than ±5V, then two 4.7V zener diode networks *must* be used to reduce the meter supply voltage. V_{DD} is taken to the positive supply (+5V max), V_{SS} to the negative (–5V max) and the centre point (0V) should be connected to INLO. The analogue input to INHI is then measured with respect to INLO (0V).

COM *must not* be linked to INLO (or INHI), although it should still be connected to ROL if the internal reference is to be used.

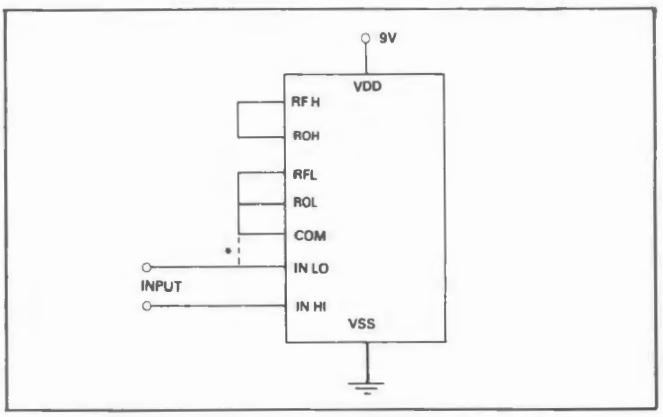
Basic 200mV circuit

Basic connections for a 200mV DVM. When ROL is linked to COM, the 100mV reference voltage is generated between ROL and ROH. This voltage is connected to the reference inputs by linking RFH to ROH, RFL to ROL.

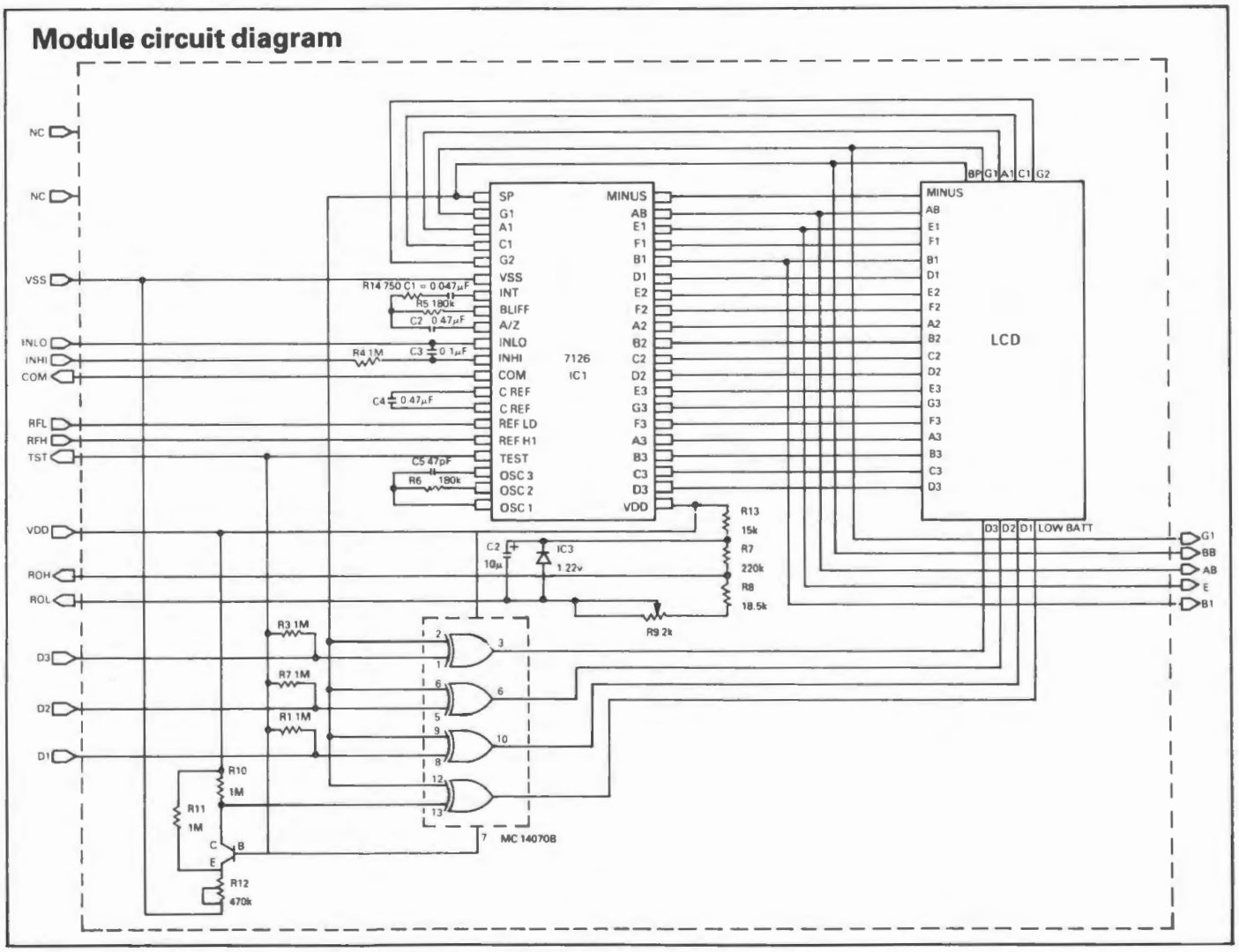
*INLO is linked to COM if the analogue inputs are floating. (NB. See note on common mode voltage range.)

In the application circuits the connections are similar to the 200mV DVM unless otherwise specified.

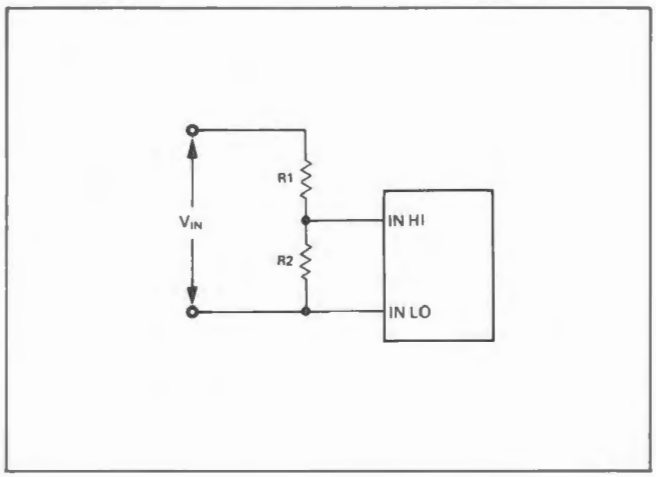
Note that the accuracy and stability of external circuitry, such as attenuators or shunts, will affect the overall meter performance.



Module circuit diagram



Input Attenuator for $V_{IN} > 200mV$



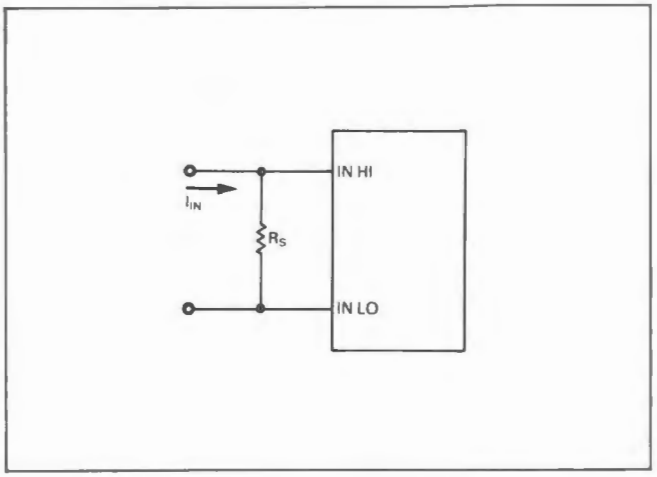
To measure voltages greater than 200mV an input attenuator is required, as shown above. This attenuator can also be used to adjust the meter scale factor. R1 and R2 should be accurate and stable. Good metal film resistors meet these requirements.

$$\text{Meter input} = \left(\frac{R2}{R1 + R2} \right) \times V_{IN}$$

e.g. (i) for V_{IN} = 2V; R1 =9MΩ, if R2 is chosen to be 1MΩ.

e.g. (ii) to display the speed of a shaft rotating up to 1500rpm, using a tachogenerator having an output of 60V DC per 1000rpm: The 90V output at 1500rpm must be reduced to 150mV to give a reading of 1500. If R1 is chosen as 1MΩ, R2 should theoretically be 1.669kΩ.

Current measurement



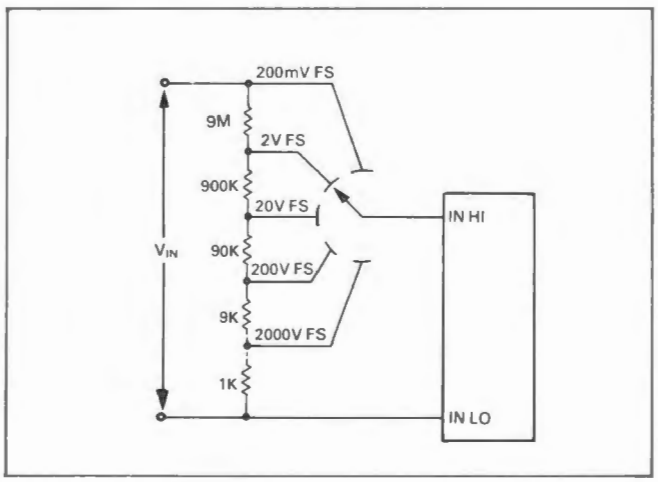
Current measurement requires a shunt resistor (R_S) to convert the input current into a 200mV input voltage as shown above. This shunt can also be used to adjust the meter scale factor.

$$\text{Meter Input} = R_S \times I_{IN}$$

e.g. (i) for I_{IN} = 200mA; R_S = 1Ω. For higher currents (eg. 20A or 200A), special block shunts, having a 200mV output are available.

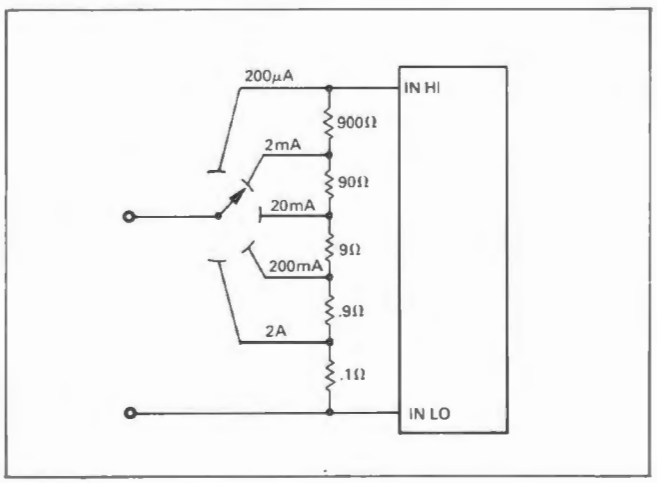
e.g. (ii) to display the level in a tank, as a percentage of its capacity, using a linear sensor having a 0mA output when empty and 5mA when full: Rs should then be 20Ω, which will convert the 0 to 5mA signal into a 0 to 100mV input. By selecting the appropriate decimal point, this can be displayed as 0 to 100.0%.

Multirange voltmeter



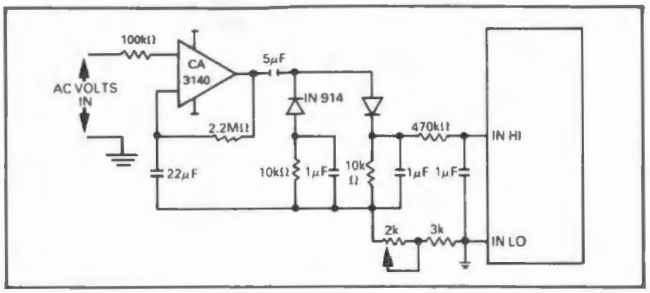
Multirange voltmeters are easy to implement using a rotary or push-button switch system as shown. It is necessary to also switch the decimal point. This can easily be accomplished by connecting the appropriate D1 to D3 terminals with a rotary switch to V_{DD}.

Multirange ammeter



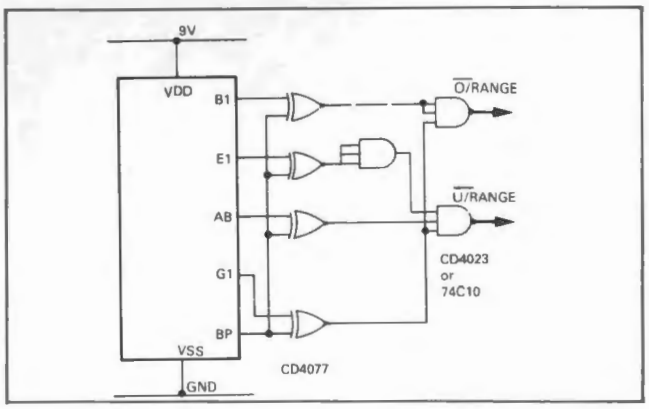
Multirange current meters can be produced using a rotary or push-button switch system as shown.

AC Voltage measurements



The module can only measure DC. To measure AC voltages, an AC to DC convertor needs to be used to condition the waveform.

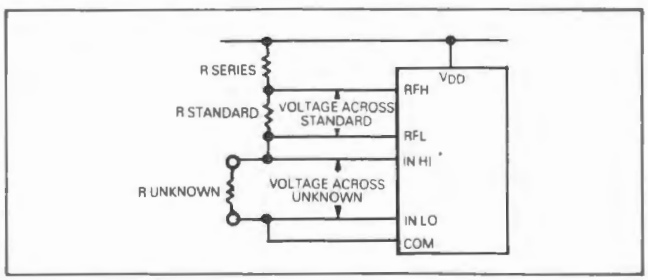
Auto-ranging



Connections for generating the over- and under-range signals for use in auto-ranging applications.

Note: Take power supply for external gates from V_{DD} and TST (not V_{SS}).

Resistance measurements



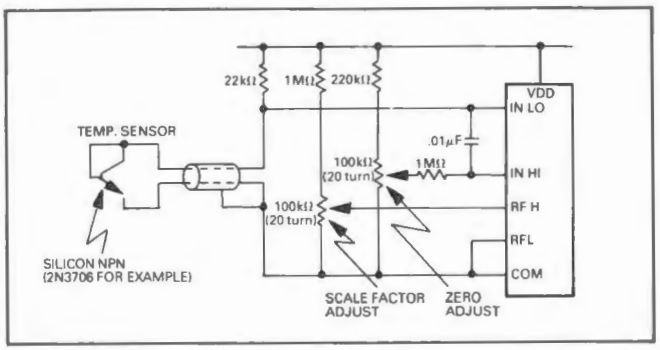
The ratiometric technique is used for resistance measurements. The unknown resistance is placed in series with a known resistor and current is passed through the pair. The voltage developed across the unknown resistor is applied to the input (INHO, INLO). The voltage across the known resistor is applied to the reference inputs RFH and RFL. If the unknown equals the standard, the display will read 1000.

$$\text{Displayed reading} = \frac{R_{unknown}}{R_{standard}} \times 1000$$

Due to the ratiometric technique, no accurately defined reference voltage is required. The module will over-range for $R_{unknown} \geq 2 \times R_{standard}$.

N.B. R_{series} should be nominally 25 times $R_{standard}$ within the limits $33k\Omega \leq R_{series} \leq 270k\Omega$.

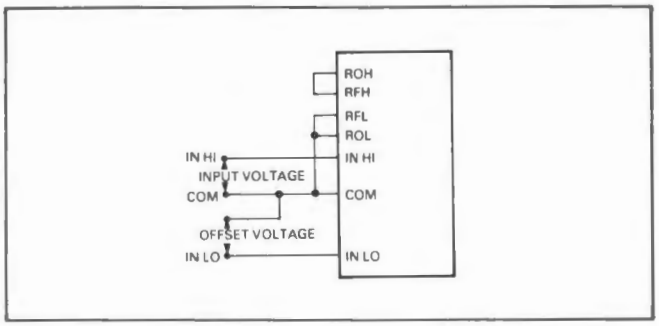
Digital thermometer



The sensing transistor has a temperature coefficient around –2mV/°C. To calibrate, place sensor in iced water (0°C) and adjust zero for a 000.0 reading. Then place sensor in boiling water (100°C) and adjust scale factor for a 100.0 reading. The sensor would normally be built into a protective housing.

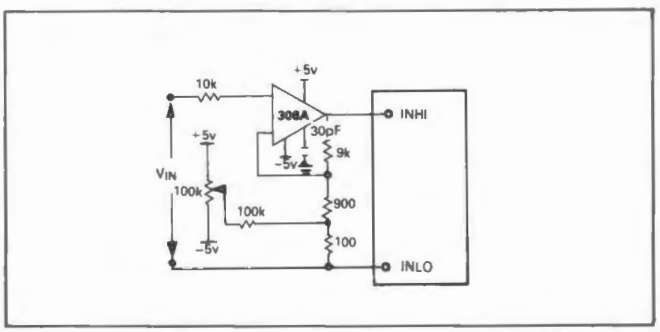
Note) This circuit does not use the internal reference, ROL and ROH should be left open.

Zero display for non-zero input voltage



If a zero display is required when the input voltage level is not zero, the offset voltage should be connected between INLO and COM while the input voltage is connected between COM and INHI.

20mV Full scale



An operational amplifier is used to measure full scale voltages less than 199.9mV. Note that the auto-zero circuitry within the module cannot compensate for the op amp offset or voltage drift.

RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company
Telephone: 0536 201234
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RS data

Pullcap fuses

Stock numbers 413-787 to 850

The pullcap range of fuselinks is ASTA CERTIFIED to BS88 Part 1 1975 for a breaking capacity (or rupturing capacity) of 80kA at 415Vac and 40kA at 250Vdc. This means that it is ideal for applications where high prospective fault currents are likely as frequently found in industrial premises and, although not dimensionally standard they meet the supplementary requirements of BS88 Part 2 for industrial fuselinks.

The time current characteristics, as shown, are the nominal pre-arcing time/current relationships including tolerances, which lie within the appropriate standard zones of BS88 Part 2. The virtual time shown on these graphs (pre-arcing time) is simply related to the more familiar I^2t value. It is this I^2t value divided by the square of the prospective breaking current.

All breaking capacity tests are performed at 50Hz but BS88: Part 1:1975 8.5.2.1 AC tests, states that 'when the rated frequency of the fuse is 50Hz... the tests shall be made at a frequency between 45Hz and 62Hz'. For frequencies less than 45Hz a decrease in voltage rating is required, the limiting value being the d.c. voltage rating. The absence of voltage zeros makes fuse operation more difficult in d.c. circuits hence the de-rating of voltage. For higher frequencies the I^2t let-through will decrease but the cut-off current will increase.

BS88/BS1361 Fuselinks

Because of their higher breaking capacity and greater suitability for industrial use the BS88 cartridge fuselink is more expensive than its BS1361 'Domestic' counterpart. However, the latter type is used in switch fuses and switch splitters commonly found in industrial premises and the 30A size is dimensionally the same as the 'Pullcap' BS88 type. If a smaller rated fused is required in such equipment, then a suitably rated 'pullcap' type may be used. 30A fuses to BS1361 include Reyrolle F192, GEC D3030, Dormain Smith DSD30 and MEM 30LC.

Applications

Cable protection

The pullcap industrial fuselinks to BS88:1975 have a class Q1 fusing factor which does not exceed 1.5. This makes them ideally * suitable for close excess current protection of PVC cables. To comply with the 15th edition of the IEE wiring regulations 1981 section 433-2, the nominal current of the fuse must not exceed the lowest of the current-carrying capacities of any of the conductors of the circuits.

$$*\text{Fusing factor} = \frac{\text{minimum fusing current}}{\text{nominal current rating}}$$

Capacitor circuits

For power factor correction capacitors a current rating of at least 1.5 times the rated capacitor current is advised so as to take into account high inrush currents.

Fluorescent lighting, discharge lighting circuits

The normal current rating of the fuselink should be at least twice the maximum full load current to be switched.

Transformer loads

For fuselink protection on the primary side, the chosen value should be at least twice the nominal transformer primary current.

Motor loads
Direct on line start

max f.l.c. A	recommended rating A	RS Stock No.
0.5	2	413-787
1.0	4	413-793
1.5	5	413-800
3.5	10	413-816
6.0	16	413-822
7.5	20	413-838
10.0	25	413-844
13.0	32	413-850

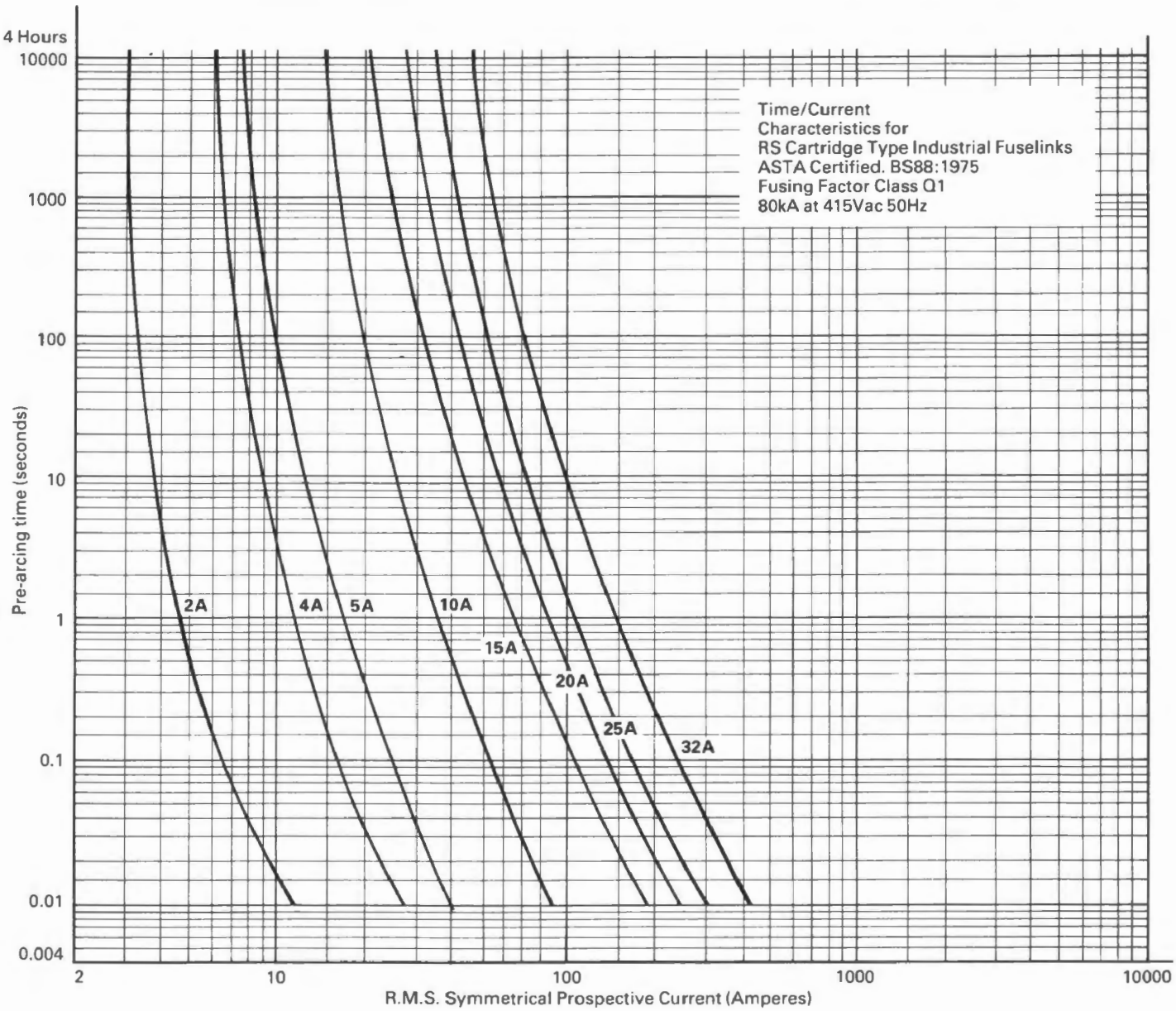
RS data

Star-delta start

max f.l.c. A	recommended rating A	RS Stock No.
1.1	2	413-787
2.0	4	413-793
2.8	5	413-800
6.3	10	413-816
11.0	16	413-822
14.0	20	413-838
18.0	25	413-844
24.0	32	413-850

Fuseholder assemblies

In order to facilitate the use of the pullcap range in motor control circuits, a suitable fuseholder assembly is available from RS (see current catalogue) which will fit on the 35mm wide top hat type DIN rail (RS stock no. 424-131.) which is also popular for mounting motor control gear. This means that the protective fuse assemblies can be mounted alongside the contactors in small enclosures and in motor control centres.



R.S. Components Ltd. 13-17 Epworth Street, London, EC2P 2HA
Telephone: 01-250 4000
For technical enquiries ring: 01-202 8252 or 0536-201234
An Electrocomponents Group Company
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RS data

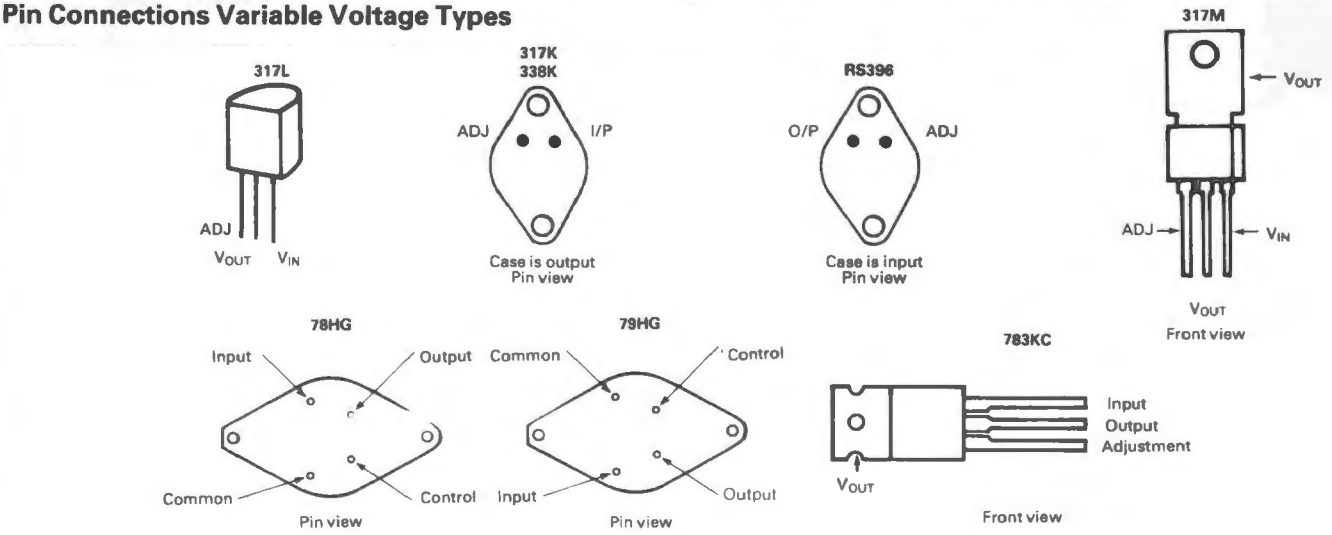
Variable voltage series regulators

A range of eight variable voltage linear regulators with outputs to suit most applications. The low power versions being ideally suited for on board regulators and the high power versions as system regulators. Variable regulators are particularly useful where an adjustable supply is required, or for presetting to a specific output and include a high voltage version.

Quick selection table

Description	Output Voltage	Current	Case	Stock No.
317L	1.2V to 37V	100mA	T092	303-179
317M	1.2V to 37V	500mA	T0202 T0220	303-185
783KC	1.25V to 125V	700mA	T0220	302-255
317K	1.2V to 37V	1.5A	T03	306-976
338K	1.2V to 32V	5A	T03	304-627
78HG	5V to 24V	5A	T03	307-339
79HG	−2.25V to −24V	−5A	T03	307-878
RS396	1.25V to 15V	10A	T03	302-722

Pin Connections Variable Voltage Types



Absolute maximum ratings

Parameter \ Type	317L	317M	317K	338K	78HG	79HG	RS396	Units
Maximum input voltage	–	–	–	–	40	40	–	V
Input-output voltage differential	40	40	40	35	35	35	20	V
Output current	0.1	0.5	1.5	5	5	5	10	A
Power dissipation	0.625	12	20	50	50	50	70	W
Operating temperature	–40 to +125	0 to +125	0 to +125	0 to +125	0 to +150	0 to +150	0 to +125	°C
Storage temperature	–55 to +150	–65 to +150	–65 to +150	–65 to +150	–55 to +150	–55 to +150	–65 to +150	°C
Lead temperature (Soldering 10s)	300	300	300	300	300	300	300	°C

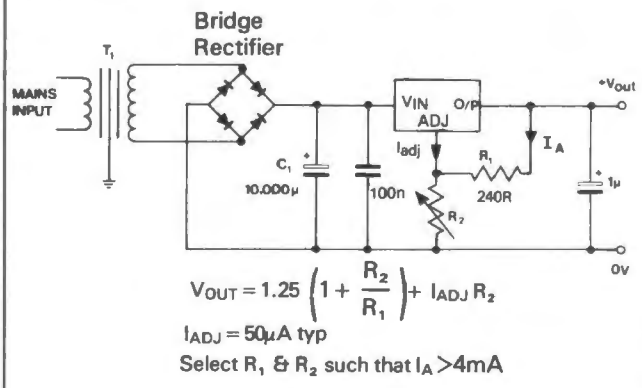
Electrical characteristics

Parameter \ Type	317L	317M	317K	338K	78HG	79HG	RS396	Units
Output voltage range	1.2 to 37	1.2 to 37	1.2 to 37	1.2 to 32	5 to 24	−2.25 to −24	1.25 to 15	V
Typical drop out voltage	1.8	1.8	2.5	2.9	2.3	2.2	2.1	V
Minimum input voltage	–	–	–	–	–	−7	–	V
Load regulation	0.1	0.1	0.1	0.1	0.2	0.7	0.15	%
Line regulation	0.01	0.01	0.01	0.005	0.2	0.4	0.005	$\%/V_{OUT}$
Ripple rejection	65	65	65	60	60	50	74	dB
Output impedance	10	10	10	3	2	—	—	mΩ
Thermal resistance junction to case	160	12	2.3	1	1.8	1.8	1.2	°C/W
Adjustment pin current	50	50	50	45	—	—	100	μA
Case	TO92	TO202	TO3	TO3	TO3	TO3	TO3	

Parameter \ Type	783KC High voltage	Units
Min. output current	15	mA
Max. output current	700	mA
Output voltage range	1.25 to 125	V
Max. input to output voltage differential	**125**	**V**
Operating virtual junction temperature	125	°C
Line regulation	0.001	$\%/V_{OUT}$
Ripple rejection	76	dB
Output regulation typ. (I_O = 15 to 700mA)	75	mV
Output voltage change with temperature	0.4	%
Output voltage long term drift	0.2	%
Output noise voltage	0.003	%
Adjustment-terminal current	83	μA
Reference voltage (output to ADJ)	1.27	V
Max. dissipation @ 25°C case temperature	20	W

Variable voltage monolithic regulators

Figure 1 **Basic circuit: positive voltage types 317L/M/K, 338K**

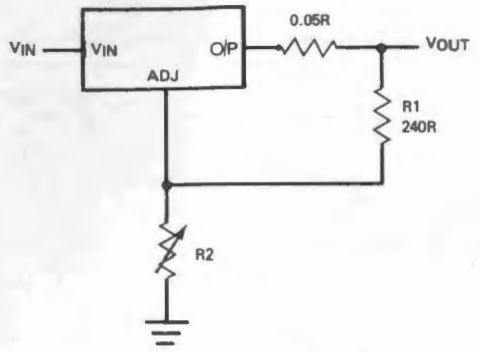


Load regulation

These regulators are capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05Ω x I_L. If the set resistor is connected near the load effective line resistance will be 0.05Ω (1 + R_2/R_1) or in this case, 11.5 times worse.

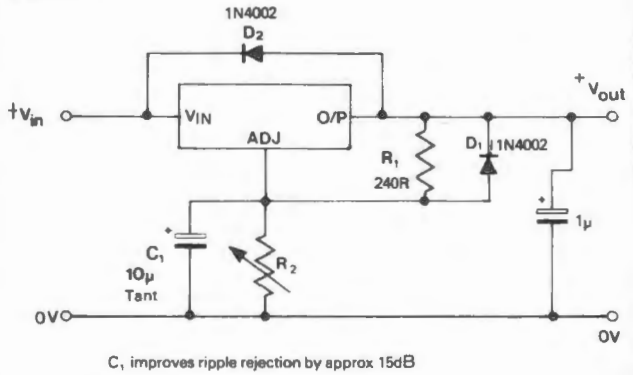
With TO-3 package, it is easy to minimise the resistance from the case to the set resistor, by using 2 separate leads to the case. The ground of R_2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

Figure 2



The circuit shown below incorporates a capacitor C_1 to improve ripple rejection. The two diodes provide protection for the regulator in the event of an input or output short circuit, D_1 provides a discharge path for C_1 under output short circuit conditions while D_2 restricts the output to input reverse voltage across the regulator under input short circuit conditions.

Figure 3



Transformer selection

Selection of a suitable transformer is dependent upon a number of factors as listed below:

1. Output voltage and current required.
2. Maximum input voltage rating of the regulator.
3. Minimum input/output differential voltage rating of the regulator i.e. dropout voltage.
4. a.c. to d.c. voltage conversion (approx. 1.4x).
5. Power dissipation with regulator.
6. Effective VA loading upon transformer.

Example:
Regulated circuit using RS317K to provide 24V d.c. max up to 0.5A.

Maximum d.c. input voltage required (for RS317K) = 40V d.c.

Minimum d.c. input voltage required (V_{in})
= output voltage (max) + dropout voltage
= 24V + 2.5V (for RS317K)
26.5V d.c.

Minimum a.c. secondary voltage required from the transformer:

$$= \frac{V_{in}\text{ (d.c.)}}{\text{voltage conversion}} = \frac{26.5}{1.4} = 19\text{V a.c.}$$

Nearest preferred transformer voltage is 0-12V, 0-12V connected in series to give 24V a.c. This will provide approx. 24V x 1.4 i.e. 34V d.c. and therefore well within minimum and maximum input ratings.

Power dissipation within regulator (20W max. for RS317K) = $(V_{in}\text{(d.c.)} - V_{out}) \times I_{out}$
$= (34 - 24) \times 0.5 = 5W$

Although this dissipation level is well within the 20W limit at lower output voltage settings it will increase, owing to greater voltage drop across the regulator, but not exceed the limit.

VA rating of the transformer can now be determined from the following formula:
VA rating = V_{in} (d.c.) x I_{out} = 34 x 0.5 = 17VA
The nearest transformer rating within our range is 20VA.
RS Stock No of transformer required 207.144.
Note: Circuit losses, mains fluctuations, and regulation have not been taken into account but should be considered in a practical design.

General circuits

Figure 4

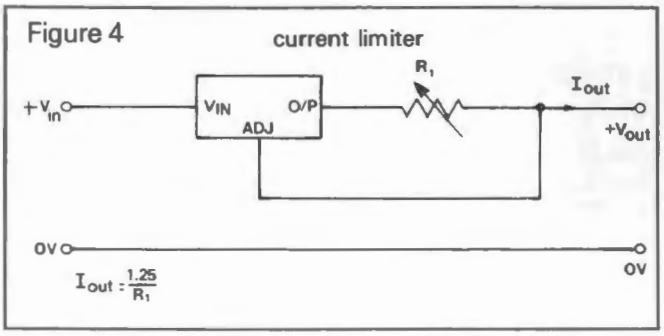
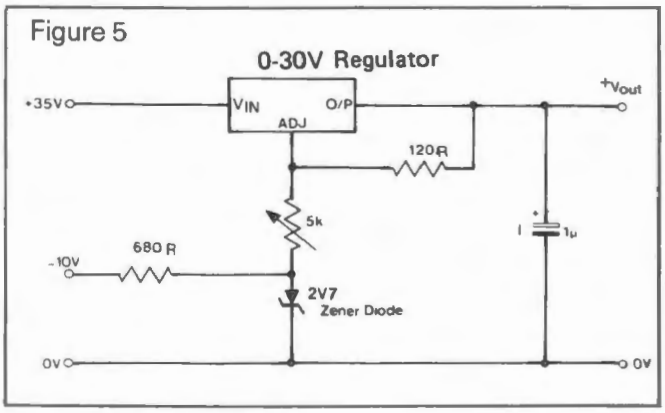


Figure 5



78HG and 79HG hybrid regulators

Two hybrid variable voltage regulators, housed in TO3 style metal cases, capable of supplying output currents up to 5 amps. The internal circuitry limits the junction temperature to a safe value and provides automatic thermal overload protection. Safe operating protection is also incorporated making the regulators virtually damage proof.

In order to achieve maximum performance the internal power dissipation must be kept below 50W. Transformer and heatsink selections are dependent upon the exact application.

Figure 6 **Basic circuit, variable voltage (positive output)**

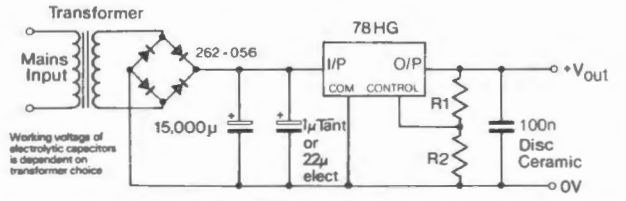
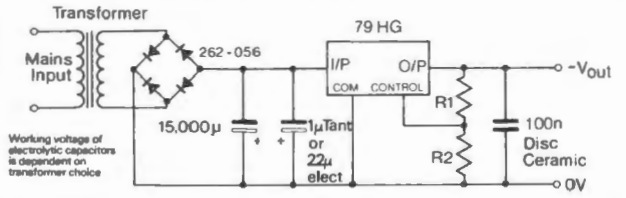


Figure 7 **Basic circuit, variable voltage (negative output)**



Select R_1 and R_2 to give the desired output voltage using the following formula:

$$V_{out} = \frac{R_1 + R_2}{R_2} V_{control}$$

where $V_{control}$ = 5V(78HG), 2.23V (79HG). R_2 current should be 1mA (minimum). The transformer and heatsink requirements are selected depending upon the application. The input/output voltage differential should be greater than 3 volts, and in order to achieve maximum performance in internal power dissipation must be kept below 50 Watts.

Both regulators have a junction to case thermal resistance of 1.8°C/W (max) and a maximum working junction temperature of 150°C.

RS396 10A regulator

The RS396 is a 10 amp regulator, adjustable from 1.25V to 15V incorporating internal current limiting, thermal and safe operating area protection.

Heat sinking

Because of its extremely high power dissipation capability, care must be taken to ensure good heat sinking. The RS396 will dissipate up to 70W continuously, provided, the maximum junction temperature limit is not exceeded. A good heat sink compound (stock number 554-311) must be used when mounting the regulator, especially if an electrical insulator is used to isolate the regulator input from the heat sink.

Filter capacitors

A very important consideration is the size of the filter capacitor in the raw supply. At these high current levels, capacitor size is usually dictated by ripple current ratings rather than just obtaining a certain ripple voltage. Capacitor ripple current (rms) is 2-3 times the d.c. output current of the filter. If the capacitor has just 0.05Ω d.c. resistance, this can cause 30W internal power dissipation at 10A output current. Capacitor life is very sensitive to operating temperature, decreasing by a factor of two for each 15°C rise in internal temperature. Since capacitor life is not all that great to start with, it is obvious that a small capacitor with a large internal temperature rise is inviting very short mean-time-to-failure. A second consideration is the loss of usable input voltage to the regulator. The RS396 requires 2V-2.5V minimum input/output voltage differential to maintain regulation. If the capacitor is small, the large dips in the input voltage may cause the RS396 to drop out of regulation. 2000 µF per ampere of load current is the *minimum* recommended value, yielding about 2.5 Vp-p ripple of 100Hz. Larger values will have longer life and the reduced ripple will allow lower d.c. input voltage to the regulator, with subsequent cost savings in the transformer and heat sink. Sometimes several capacitors in parallel are better to decrease series resistance and increase heat dissipating area.

Ripple rejection

Ripple rejection at the normal ripple frequency of 100Hz is a function of both electrical and thermal effects in the RS396 if the adjustment pin is not bypassed with a capacitor, it is also dependent on output voltage. A 25µF capacitor from the adjustment pin to ground will make ripple rejection independent of output voltage for frequencies above 100Hz. If lower ripple frequencies are encountered, the capacitor should be increased proportionally.

Keep in mind that the bypass capacitor on the adjustment pin will limit the turn-on time of the regulator. A 25µF capacitor, combined with the output divider resistance, will give an extended output voltage settling time following the application of input power.

Load regulation

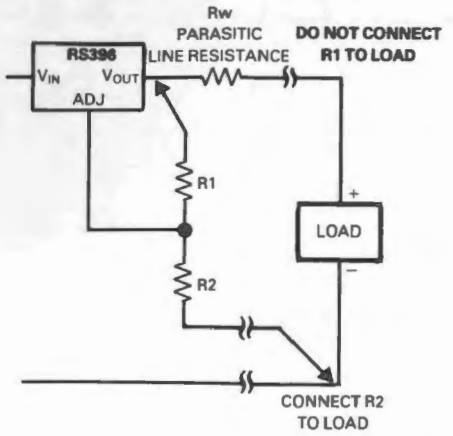
Because the RS396 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the output pin and the wire connecting the regulator to the load. For the data sheet specification, regulation is measured ¼in from the bottom of the package on the output pin. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the divider is connected *directly* to the output pin, *not to the load*. This is illustrated in Figure 8. If R1 were connected to the load, the effective resistance between the regulator and the load would be:

$$(Rw) \times \left(\frac{R2 + R1}{R1}\right)$$

Rw = Line resistance

Connected as shown, Rw is not multiplied by the divider ratio. Rw is about 0.004Ω per foot using 17 gauge wire. This translates to 40mV/ft at 10A load current, so it is important to keep the positive lead between regulator and load as short as possible.

Figure 8 **Proper divider connection**



Thermal. as well as electrical, load regulation must be considered with IC regulators. Electrical load regulation occurs in microseconds, thermal regulation due to die thermal gradients occurs in the 0.2ms-20ms time frame, and regulation due to overall temperature changes in the die occurs over a 20ms to 20 minute period, depending on the time constant of the heat sink used. Gradient induced load regulation is calculated from:

$$\Delta V_{OUT} = (V_{IN} - V_{OUT}) \times (\Delta I_{OUT}) \times (ß)$$

ß = Thermal regulation specified on data sheet.

For V_{IN} = 9V, V_{OUT} = 5V, ΔI_{OUT} = 10A, and ß = 0.005%/W, this yields a 0.2% change in output voltage. Changes in output voltage due to overall temperature rise are calculated from:

$$V_{OUT} = (V_{IN} - V_{OUT}) \times (\Delta I_{OUT}) \times (TC) \times (\theta_{jA})$$

TC = Temperature coefficient of output voltage.
θ_{jA} = Thermal resistance from junction to ambient. θ_{jA} is approximately 0.5°C/W + θ of heat sink.

For the same conditions as before, with TC = 0.003%/°C, and θ_{jA} = 1.5°C/W, the change in output voltage will be 0.18%. Because these two thermal terms can have either polarity, they may subtract from, or add to, electrical load regulation. For worst-case analysis, they must be assumed to add. If the output of the regulator is trimmed under load, only that portion of the load that changes need be used in the previous calculations, significantly improving output accuracy.

Line regulation

Electrical line regulation is very good on the RS396 – typically less than 0.005% change in output voltage for a 1V change in input. This level of regulation is achieved only for very low load currents, however, because of thermal effects. Even with a thermal regulation of 0.003%/W, and a temperature coefficient of 0.003%/°C, d.c. line regulation will be dominated by thermal effects as shown by the following example:

Assume V_{OUT} = 5V, V_{IN} = 9V, I_{OUT} = 8A

Following a 10% change in input voltage (0.9V), the output will change quickly (≤ 100μs), due to electrical effects, by (0.005%V) x (0.9V) = 0.0045%. In the next 20ms, the output will change an additional (0.002%/W) x (8A) x (0.9V) = 0.0144% due to thermal gradients across the die. After a much longer time, determined by the time constant of the heat sink, the output will change an additional (0.003%/°C) x (8A) x (0.9V) x (2°C/W) = 0.043% due to the temperature coefficient of output voltage and the thermal resistance from die to ambient. (2°C/W was chosen for this calculation.) The sign of these last two terms varies from part to part, so no assumptions can be made about any cancelling effects. All three terms must be added for a proper analysis. This yields 0.0045 + 0.0144 = 0.043 = 0.062% using *typical* values for thermal regulation and temperature coefficient.

Paralleling regulators

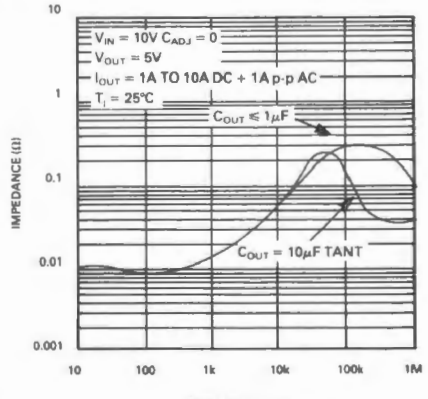
Paralleling regulators are not normally recommended because they do not share currents equally. The regulator with the highest reference voltage will supply all the current to the load until it current limits. With an 18A load, for instance, one regulator might be operating in current limit at 16A while the second device is only carrying 2A. Power dissipation in the high current regulator is extremely high with attendant high junction temperatures. Long term reliability cannot be guaranteed under these conditions.

Quasi-paralleling may be accomplished if load regulation is not critical. The connection shown in Figure 12 will typically share to within 1A, with a worst-case of about 3A. Load regulation is degraded by 150mV at 20A loads. An external op amp may be used as in Figure 13 to improve load regulation.

Input and output capacitors

The RS396 will tolerate a wide range of input and output capacitance, but long wire runs or small values of output capacitance can sometimes cause problems. If an output capacitor is used, it should be 1μF or larger. We suggest 10μF solid tantalum if significant improvements in high frequency output impedance are needed (see Figure 9). This capacitor should be as close to the regulator as possible, with short leads, to reduce the effects of lead inductance. No input capacitor is needed if the regulator is within 6 inches of the power supply filter capacitor, using 19 gauge stranded wire. For longer wire runs, the RS396 input should be bypassed locally with a 4.7μF (or larger) solid tantalum capacitor, or a 100μF (or larger) aluminium electrolytic capacitor.

Figure 9 **Output impedance***



* For output voltages other than 5V, multiply vertical scale readings by V_{OUT}/5

Correcting for line losses

Three-terminal regulators can only provide partial Kelvin load sensing (see Load regulation). Full remote sensing can be added by using an external op amp to cancel the effect of voltage drops in the unsensed positive output lead. In Figure 13 the 301A op amp forces the voltage loss across the unsensed output lead to appear across R3. The current through R3 then flows out of the V^- pin of the op amp through R4. The voltage drop across R4 will raise the output voltage by an amount equal to the line loss, just cancelling the line loss itself. A small ($\simeq$ 40mV) initial output voltage error is created by the quiescent current of the op amp. Cancellation range is limited by the maximum output current of the op amp, about 300mV as shown. This can be raised by increasing R3 or R4 at the expense of more initial output error.

Transformers and diodes

Proper transformer ratings are very important in a high current supply because of the conflicting requirements of efficiency and tolerance to low-line conditions. A transformer with a high secondary voltage will waste power and cause unnecessary heating in the regulator.

Too low a secondary voltage will cause loss of regulation under low-line conditions. The following formulae may be used to calculate the required secondary voltage and current ratings using a full-wave centre tap:

$$V_{rms} = \left(\frac{V_{OUT} + V_{REG} + V_{RECT} + V_{RIPPLE}}{\sqrt{2}}\right)\left(\frac{V_{NOM}}{V_{LOW}}\right)(1.1^*)$$

$$I_{rms} = (I_{OUT})\,(1.2) \qquad \text{(Full-wave centre tap)}$$

where:

V_{OUT} = d.c. regulated output voltage

V_{REG} = Minimum input-output voltage of regulator

V_{RECT} = Rectifier forward voltage drop at three times d.c. output current

V_{RIPPLE} = ½ peak-to-peak capacitor ripple voltage

$$= \frac{(5.3 \times 10^{-3})\,(I_{OUT})}{2C}$$

V_{NOM} = Nominal line voltage a.c. rms

V_{LOW} = Low line voltage a.c. rms

I_{OUT} = d.c. output current

Example: $I_{OUT} = 10A$, $V_{OUT} = 5V$

Assume: $V_{REG} = 2.2V$, $V_{RECT} = 1.2V$

$V_{RIPPLE} = 2\,V_{p\text{-}p}$, $V_{NOM} = 115V$,

$V_{LOW} = 105V$

$$V_{rms} = \left(\frac{5 + 2.2 + 1.2 + 1}{\sqrt{2}}\right)\left(\frac{115}{105}\right)\ 1.1$$

$$= 8.01\,V_{rms}$$

$$\text{Capacitor } C = \frac{(5.3 \times 10^{-3})\,(I_{OUT})}{2 \times V_{RIPPLE}}$$

$$= \frac{(5.3 \times 10^{-3})\,(10)}{2} = 26{,}500\,\mu F$$

* The factor of 1.1 is only an approximate factor accounting for load regulation of the transformer.

The diodes used in a full-wave rectified capacitor input supply must have a d.c. current rating considerably higher than the average current flowing through them. In a 10A supply, for instance, the average current through each diode is only 5A, but the diodes should have a rating of 10A-15A. There are many reasons for this, both thermal and electrical. The diodes conduct current in pulses about 3.5ms wide with a peak value of 5-8 times the average value, and an rms value 1.5-2.0 times the average value. This results in long term diode heating roughly equivalent to 10A d.c. current. The most demanding condition however, may be the one cycle surge through the diode during power turn on. The peak value of the surge is about 10-20 times the d.c. output current of the supply, or 100A-200A for a 10A supply. The diodes must have a one cycle non-repetitive surge rating of 200A or more, and this is usually not found in a diode with less than 10A average current rating. Keep in mind that even though the RS396 may be used at current levels below 10A, the diodes may still have to survive shorted output conditions where average current could rise to 12A-15A. Smaller transformers and filter capacitors used in lower current supplies will reduce surge currents, but unless specific information is available on worst-case surges, it is best not to economise on diodes. Stud-mounted devices in a DO-4 package are recommended. Cathode-to-case types may be bolted directly to the same heat sink as the RS396 because the case of the regulator is its power input. See current RS catalogue for suitable diodes.

Typical applications

Figure 10 **Basic 1.25V to 15V regulator**

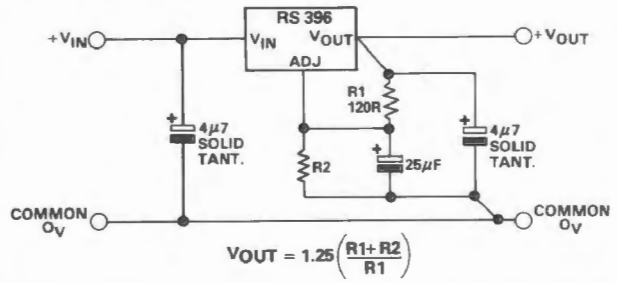
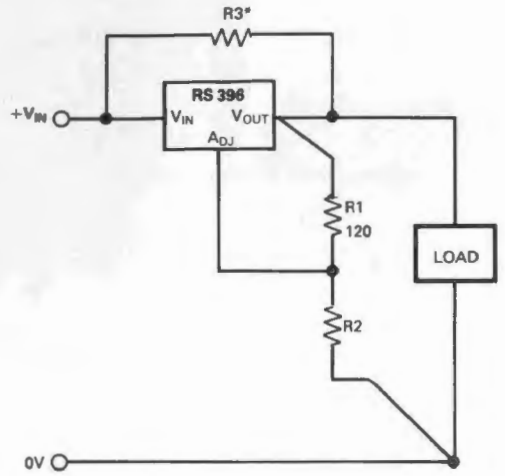


Figure 11 **Reducing regulator power dissipation**



*R3 is selected to supply partial load current. Therefore, a minimum load must always be maintained to prevent the regulated output from rising uncontrolled. R3 must be greater than $(V_{MAX} - V_{OUT})/I_{MIN}$, where V_{MAX} is worst-case high input voltage, and I_{MIN} is the minimum load current. R3 must be rated for at least $(V_{IN} - V_{OUT})^2/R3$ watts. Regulator power dissipation will be reduced by a factor of 2-3 in a typical situation where minimum load current is ½ full load current. Regulator dissipation will peak at:

$$V_{IN} = \frac{(R3)(I_{OUT})}{2} + V_{OUT}$$

and will be equal to:

$$P_{MAX} = \frac{(R3)(I_{OUT})^2}{4} \text{ assuming: } (R3)(I_{OUT}) \leq V_{MAX} - V_{OUT}$$

(1) R3 power rating must be increased to $(V_{MAX})^2/R3$ if continuous output shorts are possible. (2) Under normal load conditions, system power dissipation is not changed, but under short circuit conditions *system* power dissipation increases by $(V_{IN})^2/R3$ watts over the already high power of a shorted regulator. The RS396 will not be harmed and neither will R3 if it is rated properly, but the raw supply components must be able to withstand the overload also. Thermal shutdown of the RS396 will probably occur for sustained shorts, somewhat alleviating the problem.

Figure 12 **Paralleling regulators**

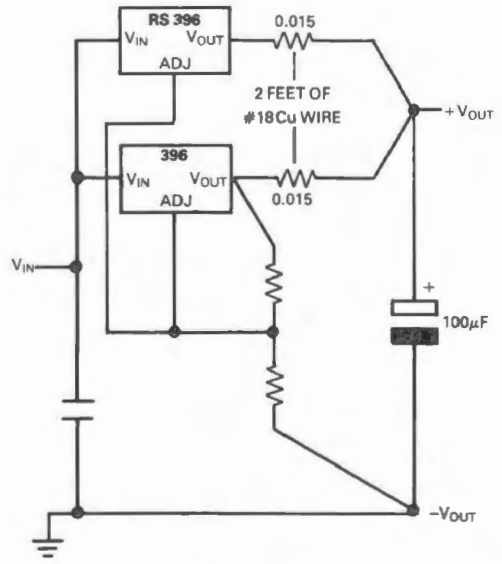
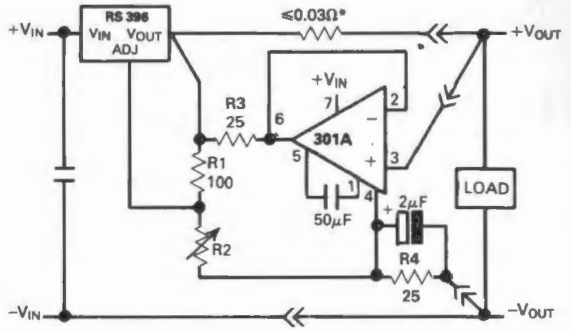


Figure 13 **Correcting for line losses**



* Parasitic line resistance created by wiring, connectors, or parallel ballasting.

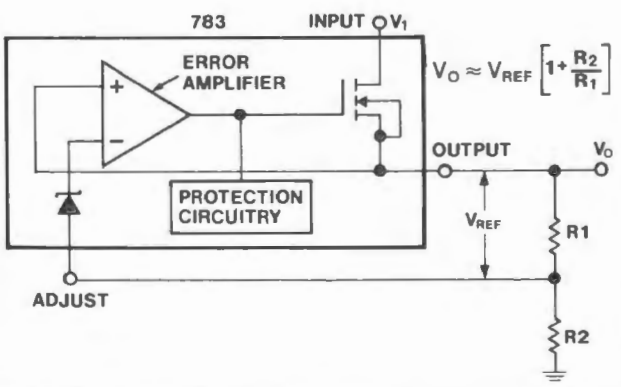
High voltage regulator RS783

The RS783 is an adjustable voltage regulator with an output range of 1.25 to 125V capable of supplying 700mA output current. The device incorporates full short-circuit, safe-operating-area and thermal shutdown protection, together with excellent regulation.

The regulator combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary breakdown and thermal runaway characteristics usually associated with bipolar outputs the RS783 maintains full overload protection while operating at up to 125 volts from input to output.

Only two external resistors are required to programme the output voltage (see Figure 14). An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not necessary, will improve transient response and protection from instantaneous output short circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

Figure 14 **Functional block diagram**



Design considerations

The internal reference is used to generate 1.25 volts nominal (V_{REF}) between the output and adjustment terminals. This voltage is developed across R_1 and causes a constant current to flow through R_1 and the programming resistor R_2, giving an output voltage of:

$$V_O = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + 1_{ADJ}(R_2)$$

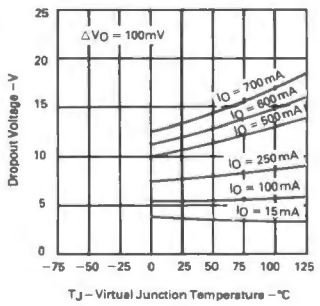
OR

$$V_O \approx V_{REF}\left(1 + \frac{R_2}{R_1}\right)$$

The RS783 was designed to minimise I_{ADJ} and maintain consistency over line and load variations, thereby minimising the I_{ADJ} (R_2) error term.

To maintain I_{ADJ} at a low level, all quiescent operating current is returned to the output terminal. This quiescent current must be sunk by the external load and is the minimum load current necessary to prevent the output from rising. The recommended R_1 value of 82 ohms will provide a minimum load current of 15 milliamperes. Larger values may be used if the input to output differential voltage is less than 125 volts, or if the load will sink some portion of the minimum current.

Dropout voltage vs virtual junction temperature



Bypass capacitors

The RS783 regulator is stable without bypass capacitors; however, any regulator may become unstable with certain values of output capacitance if an input capacitor is not used. Therefore, the use of input bypassing is recommended whenever the regulator is located more than 20cm from the power supply filter capacitor. A 1μF tantalum or electrolytic capacitor is usually sufficient.

Adjustment-terminal capacitors are not recommended for use with the RS783 as they can seriously degrade load transient response as well as create a need for extra protection circuitry. Excellent ripple rejection is presently achieved without this added capacitor.

Due to the relatively low gain of the MOS output stage, output voltage drop may occur under large load transient conditions. Addition of an output bypass capacitor will greatly enhance load transient response as well as prevent drop-out. For most applications it is recommended that an output bypass capacitor be used with a minimum value of:

$$C_{out}(\mu F) = \frac{15}{V_{out}}$$

Larger values will provide proportionally better transient response characteristics.

Protection circuitry

The RS783 regulator includes built-in protection circuitry capable of guarding the device against most overload conditions encountered in normal operation. These protective devices are current limiting, safe-operating-area protection and thermal shutdown. These circuits are meant to protect the device under occasional fault conditions only. Continuous operation in the current limit or thermal shutdown mode is not recommended.

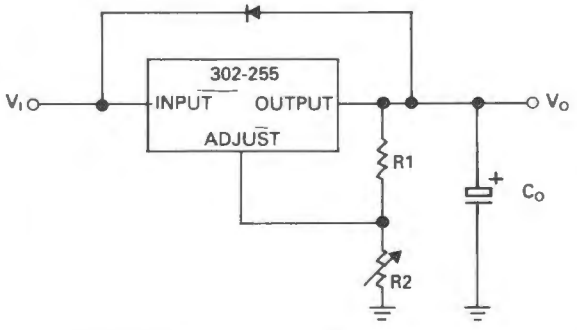
The internal protection circuits of the RS783 will protect the device up to a maximum rated input voltage as long as certain precautions are taken. If the input voltage is instantaneously switched on, transients exceeding maximum input ratings may occur, which may destroy the regulator. In addition, if rise times in excess of 10V per nanosecond are applied to the input, a parasitic n-p-n transistor in parallel with the DMOS output can be tuned on causing failure. If the device is operated over 50 volts and the input is switched on rather than ramped, a low Q capacitor, such as tantalum or electrolytic should be used rather than ceramic, paper or plastic bypass capacitors. A dissipation factor of 0.015 or greater will usually provide adequate damping to suppress ringing. No problems will occur normally if the input voltage ramps through a line rectifier or filter network.

Similarly, if an instantaneous short circuit is applied to the output, both ringing and excessive fall times can result. A tantalum or electrolytic bypass capacitor is recommended to eliminate this problem. However, if a large output capacitor is used and the input is shorted, the addition of a protection diode may be necessary to prevent capacitor discharge through the regulator. The amount of discharge current delivered is dependent on output voltage, size of capacitor and fall time of V_{in}. A protective diode (see Figure 9) is required only for capacitance values greater than:

$$C_O(\mu F) = \frac{3 \times 10^4}{V_{out^2}}$$

Care should be taken to prevent insertion of regulators into a socket with power on. Power must be turned off prior to removing or inserting regulators.

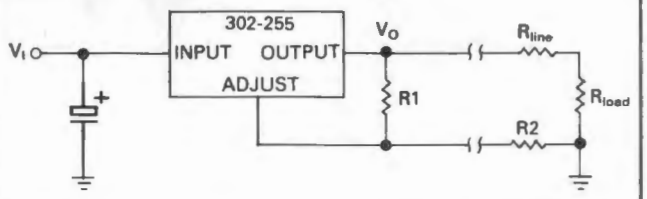
Figure 15 **Regulator with protective diode**



Load regulation

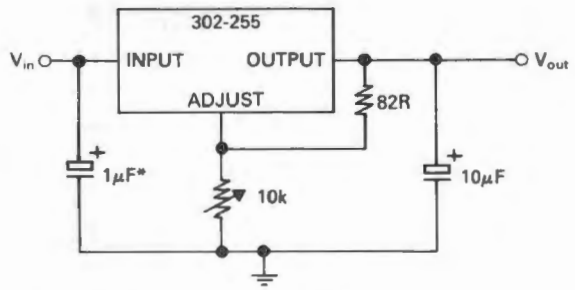
The current set resistor (R_1) should be located close to the regulator output terminal rather than near the load. This eliminates long line drops from being amplified through the action of R_1 and R_2 to degrade load regulation. To provide remote ground sensing R2 should be near the load ground, see Figure 16.

Figure 16 **Regulator with current set resistor**



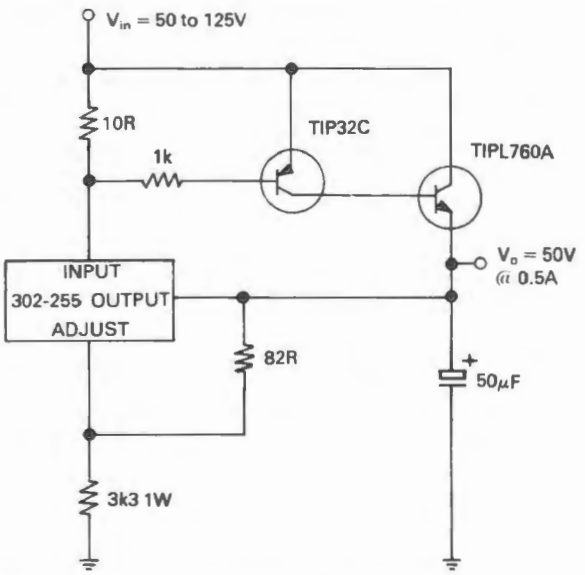
Typical applications

Figure 17 **1.25V to 115V adjustable regulator**



*required if the device is more than 20cm from filter capacitor

Figure 18 **50V regulator with current boost**



TIPL760A must be mounted on suitable heatsink.

RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

'Sweet spot' 'visible' emitter

Stock number 301-915

The RS 'Sweet spot' opto-electronic components are a range of devices suited to many applications in light sensing and especially for fibre optics. The unique form of construction uses a glass focusing bead and a clear lens cap to focus or project a narrow beam of radiation which can be easily and efficiently coupled to a wide range of optical fibres. *Data sheet 4557 details other devices in this range.*

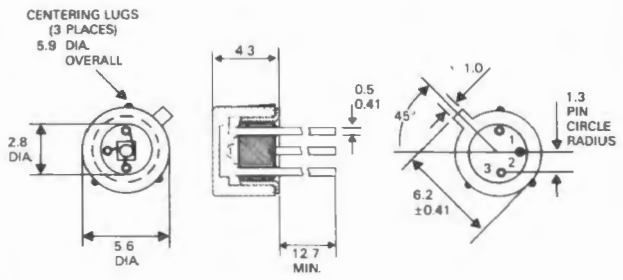
Absolute maximum ratings

Operating temperature	−40°C to +100°C
Storage temperature	−40°C to +100°C
Pin soldering temperature	240°C for 5 secs max
Continuous forward current	50mA
Reverse voltage	5V (10μA)

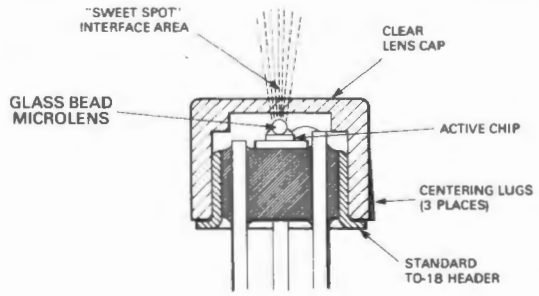
Features

- Low cost solution for fibre optic links.
- Plastic cap designed for easy press-fit installation.
- High radiance.
- Good linearity.
- Optimised for 1 mm core fibre otptic cables.
- Projects a uniform 'sweet spot' of light 400μm in diameter at the window surface.

Dimensional information (mm)



Cross section through device



'Sweet spot' in a trade name of Honeywell Control Systems Ltd.

Emitter 301-915

Light green spot on can

RS data

Electro-optical characteristics $T_A = 25°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Emitter 301-915						
Forward voltage drop	V_F	$I_F = 50mA$		1.9	2.5	V
Equivalent series resistance	R_S			2.5		Ω
Device capacitance	C_T	$V_R = 1V$		100		pF
Power output (see note below)	P_O	$I_F = 50mA$	20	25		μW
Response time	t_r	1V d.c. bias, $I_{PK} = 100mA$		100	150	ns
Peak output wavelength	λPK	$I_F = 50mA$		665		nm
Spectral bandwidth	Δλ	$I_F = 50mA$		22		nm
Temperature coefficient of V_F	$\Delta V_F/\Delta T$			−1.4		mV/°C
Temperature coefficient of P_O	$\Delta P_O/\Delta T$	$I_F = 50mA$		−0.06		dB/°C
Temperature coefficient of	$\Delta\lambda/\Delta T$			0.35		nm/°C
Thermal resistance				500		°C/W
Projected radiation beam		At device window		400		μm

Note: P_O is measured at the end of a 10m length of RS polymer cable.

Typical performance curves

Emitter 301-915

Figure 1 **Power output vs d.c. forward current**

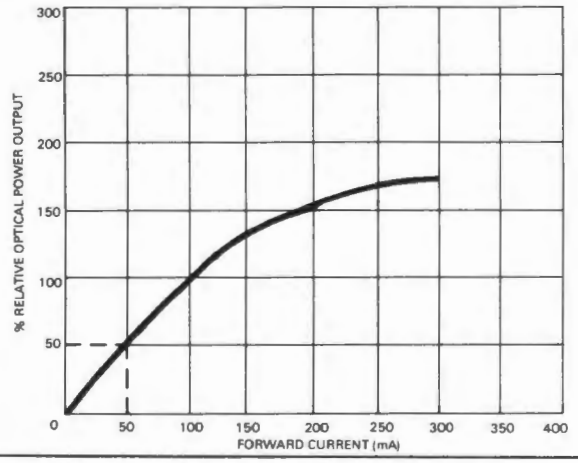


Figure 2 **Radiant intensity vs Polar angle**

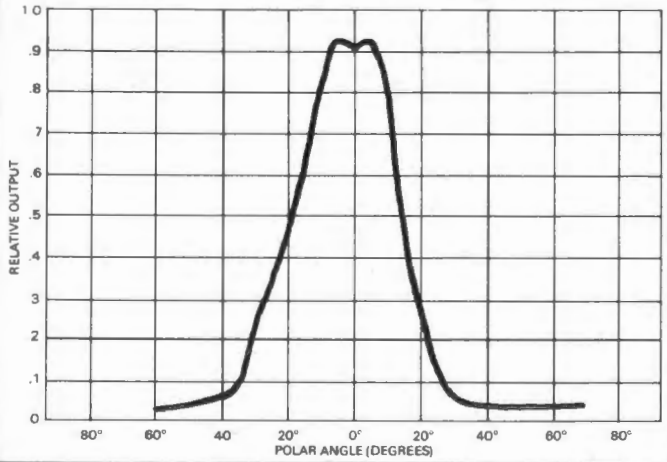
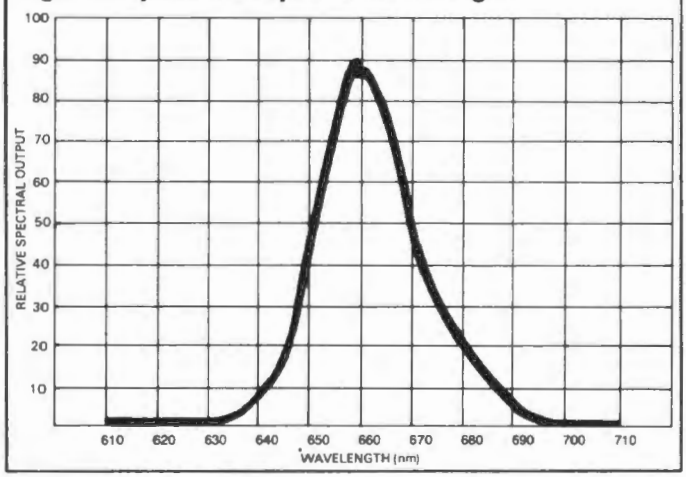


Figure 3 **Spectral output vs wavelength**



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RS data

Intelligent multimeter Thurlby 1905a

Stock number 610-871

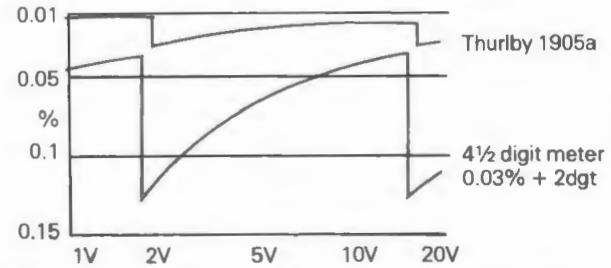
The Thurlby 1905a is a high performance 5½ digit, manual ranging multimeter incorporating dc and ac voltage, dc and ac current, resistance and diode test ranges as standard. It has all the functions and capabilities of a conventional bench multimeter combined with longer scale length, greater sensitivity, higher effective accuracy and powerful computing and data logging capabilities.

Features

- 5½ digits (± 210,000 counts)
- 1μV, 1mΩ, 1nA sensitivity
- 0.015% basic 1 year accuracy
- Null, hold and store functions
- Digital filter with adaptable characteristics
- Wide range of computing functions:
- Ax+B, Hi-Lo-Pass, % deviation Min/Max, Running Average, dB
- 100 reading data logger
- RS 232 interface available

The 1905a has a scale length of ±210,000 counts for dc voltage, current and resistance ranges. Not only does this provide ten times greater resolution compared with 4½ digit meters (the 1905a can measure a 1mV change in a 200 volt signal), but as shown in Figure 1 it also provides a dramatic improvement in effective accuracy.

Figure 1 **Effective Accuracy versus Reading**



With a max. resolution of 1μV, 1mΩ and 1nA, the 1905a is ten times more sensitive than 4½ digit meters. That extra sensitivity enables measurements to be made in areas previously impossible such as thermocouple junctions, switch contact resistance or capacitor leakages.

Industry standard 10MΩ input impedance applies to all dc voltage ranges, but the lower two ranges can also be selected to have greater than 1000MΩ impedance to eliminate errors when measuring high impedance circuitry.

A full set of current ranges allows measurement to 5 amps dc or ac.

The 1905a uses non-linear digital filtering which is highly effective in eliminating unwanted noise but responds rapidly to a change in reading. When working with very noisy or unstable measurements the characteristics of the digital filter can be reprogrammed to suit the particular application.

Press the 'null' key and the present displayed reading is stored and subtracted from all future readings. This powerful feature has a host of uses such as removing test lead resistance, observing deviation levels, or measuring relative to an alternative voltage point without having to move the ground lead connection.

Press the 'hold' key and the display is frozen allowing one time to study or record the result. Alternatively, press the 'store' key and the result is transferred to memory for recall later.

The 1905a has a set of computing functions waiting to transform its capabilities. Voltages can be expressed in dBV, related to any 0dB reference or expressed in dBm for a chosen impedance. Transducer outputs can be scaled, offset and displayed in the required engineering units. Tests can be made against preset limits, percentage deviations from a preset nominal displayed, running averages taken and maximum and minimum values recorded.

A simple and consistent entry sequence combined with clear display prompts and a logical keyboard arrangement make programming quick and simple, and the various computing functions can be operated simultaneously.

The 1905a can store readings for recall later at any required time interval from ⅓ second to 2¾ hours. Up to 100 readings can be stored. Tedious time related measurement sequences can be handled automatically without disrupting work schedules.

One can also capture rapidly changing measurements and read them out at a convenient speed.

DC Voltage	**Accuracy**	**Input Impedance**	**Max. Input**
±210.000mV	±(.025%r+.0015%s+2dgt)*	10MΩ or >1000MΩ	1100V pk 15 secs
±2100.00mV	±(.015%r+.001%s+1dgt)		400V DC or RMS cont.
±21.0000V	±(.020%r+.001%s+1dgt)		
±210.000V	±(.025%r+.001%s+1dgt)	10MΩ	1100V DC or AC pk
±1100.00V			
Resistance	**Accuracy**	**Excitation Current**	**Max. Input**
210.000Ω	±(.05%r+.003%s+2dgt)*	1mA	
2100.00Ω			
21.0000kΩ	±(.04%r+.001%s+2dgt)	100μA	400V DC
210.000kΩ		10μA	or RMS cont.
2100.00kΩ	±(.08%r+.002%s+2dgt)	1μA	
21.000MΩ	±(.25%r+.003%s+2dgt)	.1μA	
DC Current	**Accuracy**	**Voltage Burden**	**Max. Input**
±210.00μA	±(.1%r+.0015%s+2dgt)*	250mV max.	1A, 300V
±2100.00μA			fuse protected
±21.0000mA			
±210.000mA	±(.15%r+.002%s+2dgt)*		
±2100.00mA	±(.25%r+.0015%s+2dgt)*	500mV max.	5A, 300V
±5.0000A	±(.45%r+.0015%s+2dgt)*	1V max.	fuse protected
AC Voltage	**Accuracy 45-65Hz**	**Input Impedance**	**Max. Input**
210.00mV	±(.3%r+.05%s+10dgt)	10MΩ//40pF	1100V pk 15 secs
2100.00mV	±(.2%r+.02%s+4dgt)		400V RMS cont.
21.000V			
210.00V	±(.3%r+.02%s+4dgt)		750V RMS cont.
750.0V			
AC Current	**Accuracy 45Hz-1kHz**	**Voltage Burden**	**Max. Input**
210.00μA	±(.3%r+.05%s+10dgt)	250mV max.	1A, 300V
2100.0μA			fuse protected
21.000mA			
210.00mA			
2100.0mA	±(.45%r+.05%s+10dgt)	500mV max.	5A, 300V
5.000A	±(.65%r+.05%s+10dgt)	1V max.	fuse protected
Diode Test	**Accuracy**	**Excitation Current**	**Max. Input**
2100.00mV	5%r	1mA	400V

r = of reading
s = of scale
*indicates use of 'null' key

Intelligent functions

1. Logger
Stores up to 80 readings automatically at any entered time interval from 1 second to 9999 seconds. A facility exists for storing readings at approximately 3 per second. Alternatively, readings may be entered into store manually by pressing the 'store' key when a reading is required to be stored.

2. Av.Lo.Hi.
Enables the running average, lowest reading and highest reading that occur while the programme is being run to be stored in memory for recall later.

3. Filter
Enables varying amounts of digital filtering to be selected.

4. Dec. Pt.
Enables the decimal point to be repositioned in order to change the engineering units of this display.

5. dB
Enables voltage, current or resistance to be displayed in logarithmic form.

In order to facilitate the display of voltage in decibels, the result of the calculation

$$20 \log_{10} \left(\frac{x}{\sqrt{R_{eff}}} \right)$$

is displayed, where 'x' is in volts. The display can be in dBV (dBs relative to 1V), dBm (dBs relative to 1mW of power into a reference impedance) or dB rel (dBs relative to a measured voltage representing 0dB).

This function can be used to display other logarithmic relationships in addition to dBs.

6. $Ax + B$
Enables a reading x, to be multiplied by a scaling factor 'A' and an offset 'B' to be added. The result of the calculation $Y = Ax + B$ is displayed.

7. $\Delta\%$
Enables the percentage amount that a reading, x, differs from some nominal value (represented by the constant 'n') to be displayed according to the formula:

$$Y = \left(\frac{x-n}{n} \right) \times 100$$

8. Limits
Enables the reading x, to be compared with high and low limit readings set as constants. A 3½ digit reading is displayed along with a two letter code as follows:

	$x <$ low limit –	LO (low)
low limit <	$x <$ high limit –	PA (pass)
	$x >$ high limit –	HI (high)

Simultaneous operation of programmes

Any number of programmes may be operated simultaneously, but the sequence in which data is fed to the various programmes is pre-defined as shown in Figure 2.

Thus if 'Limits' and '$Ax + B$' are run simultaneously, the 'Limits' programme will operate on the output of the '$Ax + B$' programme and never the other way round.

Logarithmic calculations

The 'dB' function can be used to provide a general logarithmic function in addition to dB calculations.

The displayed value represents

$$20 \log_{10} \left(\frac{x}{\sqrt{R_{eff}}} \right)$$

where x is in volts, mA or kΩ and R_{eff} is initialised to 1.

If, for instance, it is required to display $\log_e x$, this can be done by applying the equation:

$$\log_e x = \log_e 10 \times \frac{1}{20} \times 20 \log_{10} x$$

$$= 0.11513 \times 20 \log_{10} x.$$

Thus, by combining the 'dB' programme (Ref = 1.000) with the '$Ax + B$' programme (A=0.11513, B=0), a display representing $\log_e x$ can be achieved.

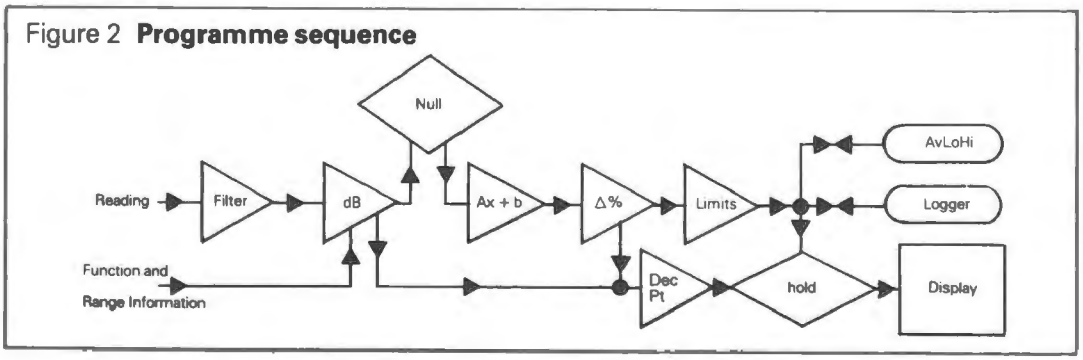
4-20mA current loops
The provision of the '$Ax + B$' function combined with an over-range point of 21mA makes the instrument ideal for use with a 4-20mA current loop system.

For example, a user may wish to monitor a weighing system which outputs 4mA at 0 kilogrammes, and 20mA at 10 kilogrammes. He calculates the values for 'A' and 'B' as follows:

$$A = \frac{10}{20-4} = 0.625 \quad B = -(4 \times 0.625) = -2.5$$

Thus, by measuring the loop output using the 20mA range and running the '$Ax + B$' programme with A = 0.625 and B = -2.5, a direct readout of weight in kilogrammes is obtained.

Figure 2 **Programme sequence**



RS data

RS232 serial data output module

This module fits inside the Thurlby 1905a digital multimeter and outputs serial data, representing the information on display, via a back panel connector.

The serial data is transmitted at RS232 levels, i.e. line high >+3 volts and line low <–3 volts (typically ±8V, Z_{out} = ½k).

The data is made available on a 25 way D connector (male) of which only 3 pins are used. These are:

pin 2: data out
pin 7: data ground
pin 1: protective ground (i.e. mains earth).

The data output is optically isolated from both protective ground and the measurement ground of the 1905 multimeter. The maximum voltage allowable between data ground and protective ground (mains earth), and/or between data ground and measurement ground (the common ground socket) is limited to 500Vpk.

The data transmission rate if fixed at 9.6 kilobaud. The data format is 8 bit ASCII with line low representing a logic 1, the least significant bit is sent first. A start bit (line high) precedes each character and the line is returned to idle (line low) at the end of each character (see Figure 3). A string of 11 characters is transmitted (10 active characters and carriage return), each character commencing 2.5ms after the start of the previous character.

Data is transmitted every conversion (i.e. every 330ms) and starts 290ms after the completion of the signal measurement phase of the multimeter conversion.

The 11 characters are sent as follows:

'M' or 'R' (see Note 1).

9 characters representing the 8 display digits plus the decimal point.

Carriage return.

Thus the display 12.3456 (5½ digit mode) is transmitted as:
R/SP/1/2/./3/4/5/6/SP/CR

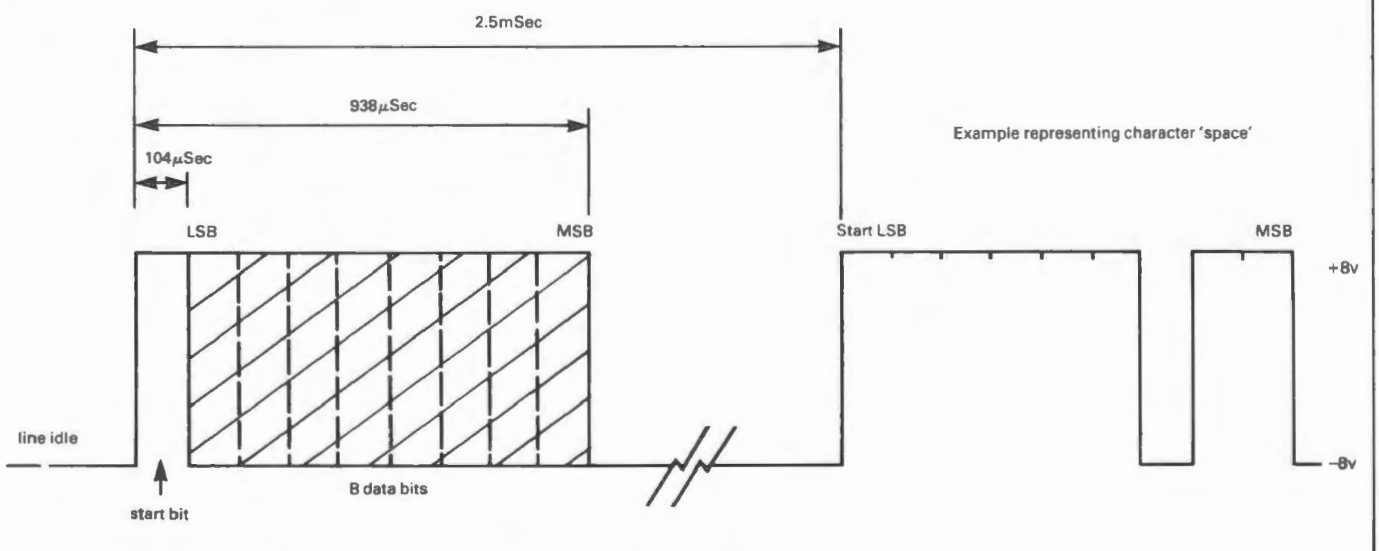
whilst the display – 98.76 (4½ digit mode) is transmitted as:
R/–/SP/9/8/ ./7/6/SP/SP/CR

The letter R indicates that a 'real-time' result is being transmitted i.e. the result of the latest measurement of the DMM input signal. The letter M precedes a message (e.g. ENTER?; RUN?; or FILTER=), or data being recalled from memory in Logger or AvLoHi programs, or as result frozen by the 'hold' key.

When no decimal point appears on the display, an additional space is inserted after the first character to ensure a constant string length.

Note 1: In all cases 11 characters are transmitted (10 + carriage return) so that an INPUT statement from a computer will read a 10 character string. This string is the same as the 1905 display except that all transmitted letters are upper case, and the string commences with either a letter 'R' or a letter 'M'.

Figure 3



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RS data

Dimmer switch i.c. 576B

Stock number 301-713

Functional description

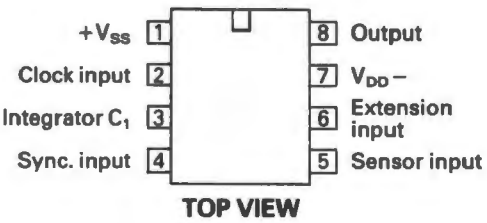
The 576 permits the design of a fully electronic dimmer with phase control of resistive loads and operation from a single touch sensitive sensor input. The circuit is designed for on and off switching with a varied conduction angle which continuously ramps up and down until the sensor input is disconnected.

Features

- Sensor input/extension inputs available
- Brightness controlled with an approximately linear characteristic
- High interference immunity
- Set brightness value remains stored for short supply interruptions of <1s
- Low external component count
- Compact 8-pin D.I.L. package.

Absolute maximum ratings

Supply voltage V_{DD} ——— –20 to +0.3V
Input voltage V_I ——— –20 to +0.3V
Operating temperature range ——— 0°C to +80°C
Storage temperature range ——— –55°C to +125°C



TOP VIEW

Electrical characteristics

T_A = 25°C Voltage ratings are with V_{SS} = OV

Parameter	Symbol	Conditions	Lower Limit	Typ.	Upper Limit	Units
Supply voltage	V_{DD}		–18	–15	–13	V
Supply current	I_{DD}	V_{DD} = –15V		1.0	1.4	mA
Supply current with missing Sync. signal	I_{DD}	V_{DD} = –15V			0.85	mA
Input reverse current	I_I	$V_I = V_{SS}$ –10V		<0.1	3	µA
Input capacitance	C_I	V_I =0V, f = 1MHz			5	pF
Sensor input						
High input voltage	V_{IH}	With series 10MΩ	V_{SS}–2			V
Low input voltage	V_{IL}	resistor from supply			V_{SS}–8	V
Input current	I_{IH}	line			35	µA
High to low transition time	t_{tHL}		line	sine	wave	
Low to high transition time	t_{tLH}		line	sine	wave	
Frequency with active signal	f	Synchronized with 50/60 Hz clock at Sync. input		50/60		Hz
Extension input						
High input voltage	V_{IH}		V_{SS}–2			V
Low input voltage	V_{IL}				V_{SS}–8	V
Input current	I_{IH}				35	µA

Parameter	Symbol	Conditions	Lower Limit	Typ.	Upper Limit	Units
Sync. Input						
High input voltage	V_{IH}	With series	$\frac{1}{2}V_{DD}+2$			V
Low input voltage	V_{IL}	1.5MΩ resistor			$\frac{1}{2}V_{DD}-2$	V
Input current	I_{IH}				240	μA
HL/LH transition			line	sine	wave	
Clock input						
High input voltage	V_{IH}		$V_{SS}-2$		$V_{SS}+0.3$	V
Low input voltage	V_{IL}		V_{DD}		$V_{SS}-8$	V
HL transition	t_{THL}				100	μs
LH transition	t_{TLH}				100	μs
Clock frequency	f_{CLK}		0		500	Hz
Without clock	V_{IO}		V_{SS}		$V_{SS}+0.3$	V
Integrator						
External capacitance	C_I			47		nF
Output						
L output current		$V_{DD} = -15V$, $V_{QL} = -3V$	25			mA
L pulse width				40		μs
H output voltage			V_{SS}		$V_{SS}+0.5$	V
HL transition					20	μs
LH transition					20	μs

Operation

The integrated circuit distinguishes between the turn on/off instruction and dimming by the duration of the control operation.

Turning on/off: A short touch of between 50 to 400ms on the sensor input turns the output on or off depending on its preceding state. The switching process occurs at the end of the touch period.

Setting of phase angle control: If the sensor is touched for a period longer than 400ms the conduction angle is varied continuously. The cycle between minimum and maximum conduction takes about 7 seconds and continues until the end of the touch period.

Table 1 **Control Inputs**

Function	Mains cycle	Sensor input	Extension input
Operated	Positive	L	H
	Negative	X	H
Not operated	Positive	H	L or X
	Negative	X	X or L

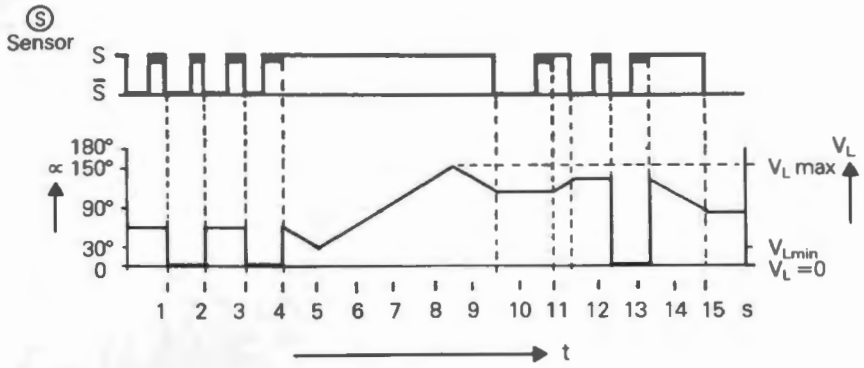
H = V_{IH}, L = V_{IL}

External circuitry

The circuit of Figure 2 shows a typical application as a general purpose phase control circuit for loads of up to 400W. The supply for the 576 is derived via R_1, C_2, D_1, D_2 and C_3. R_2 and C_4 provide the filtered signal for synchronisation of the internal time base with the mains frequency. R_7 sets up the sensitivity of the sensor. R_5 and R_6 limit the current under incorrect polarization conditions on the extension input. Both resistors may be omitted if no extension input is required, then pin 6 must be connected directly to pin 7.

All switching and control functions can also be performed from a switch connected to the extension input. Control for the extension units is identical to the central unit. A digitally determined immunity period of approximately 50ms ensures high interference immunity against electrical variations on the control inputs. In the case of supply interruptions the set switching state will be stored for about 1 second, after this period the circuit will turn into the off state. All stated time specifications are for a mains frequency of 50Hz. If 60Hz supplies are used the periods will be shortened accordingly.

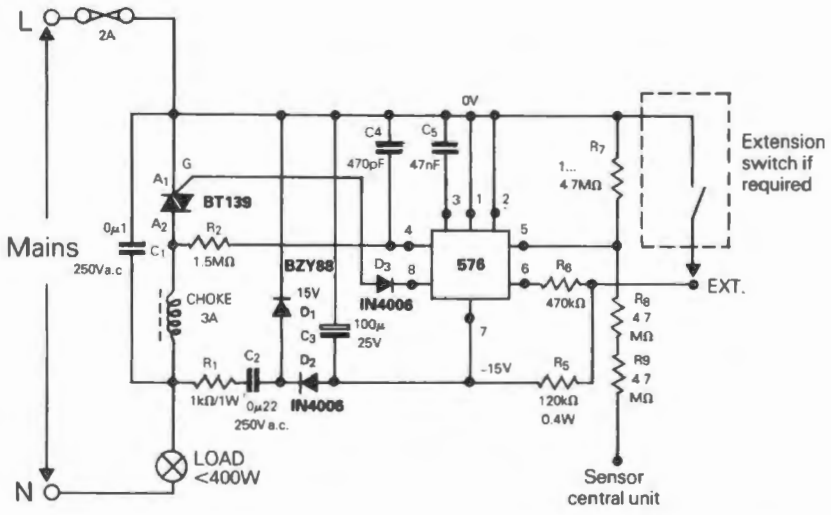
Figure 1 **Control behaviour** (schematic)



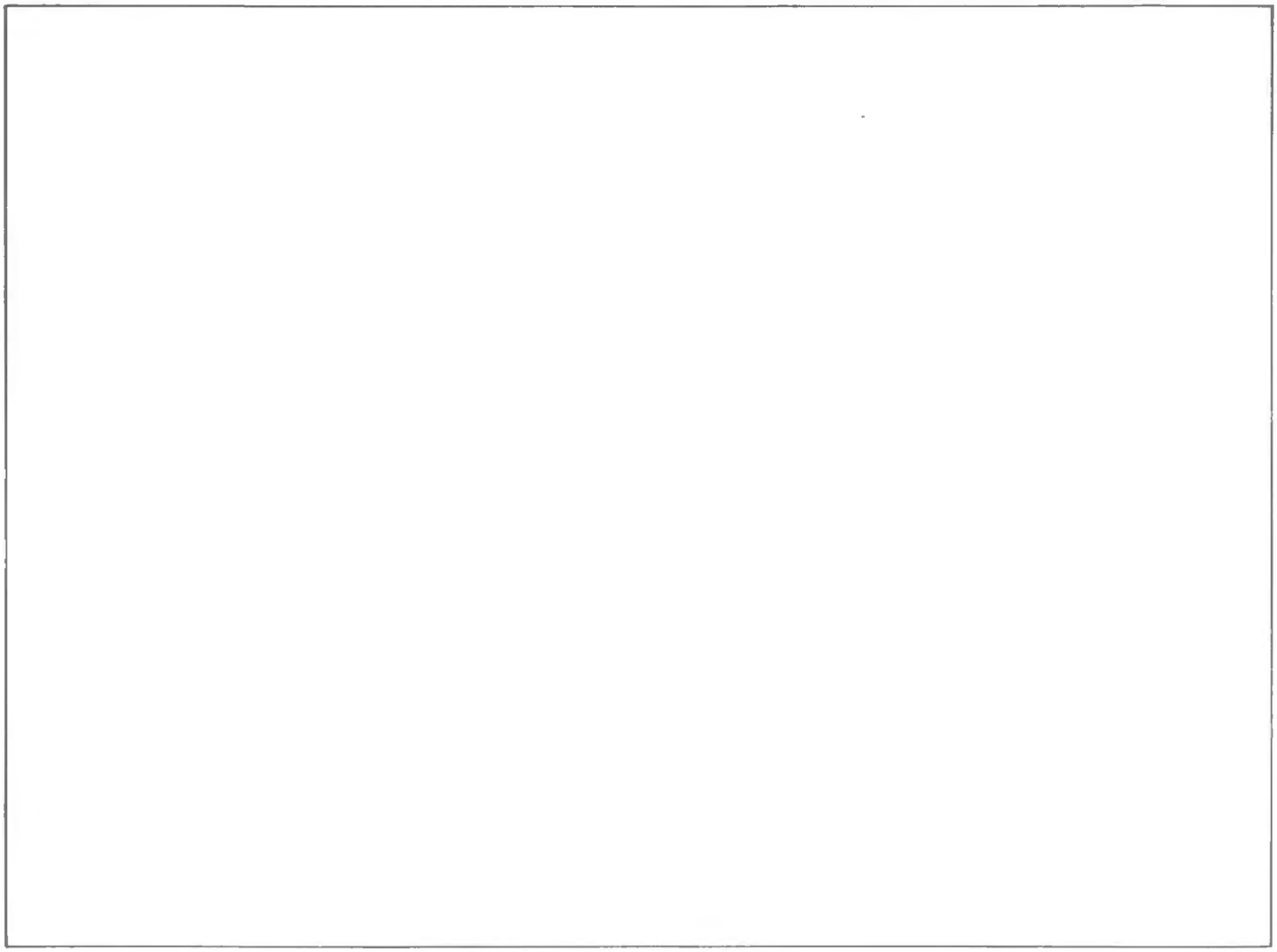
∝ Conduction angle S Control signal: S Senor touched
V_L Lamp voltage (▬<0.4s; —<0.4s)
S̄ Sensor not touched

With turning off, the selected brightness is stored and again set when the switch is turned on. Dimming starts at that stored value and the control direction is reversed with repeated dimming.

Figure 2 **Application circuit**



RS data



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RS data

Phase angle trigger module

Stock number 301-678

A fully isolated phase angle trigger module which will act as a proportional phase control for thyristors in half controlled single phase bridge or inverse pair configurations. The gate output varies depending on load and is always sufficient to ensure that when a trigger command is received, the thyristor will receive sufficient gate current and gate voltage to remain on. This is especially useful for a light load of a few milliamps where the thyristor holding current would want to drop out, under this condition the module will continue to feed gate power into the thyristor provided an input signal is still present.

A range of compatible encapsulated thyristor and diode models is available, full details can be found on Data Sheet 4484.

Absolute maximum ratings

Supply voltage	205-265Vac
Supply frequency	47-53Hz
Operating temperature range	0 to +55°C
Storage temperature range	–20 to +70°C

Electrical specification

Input range	0-5.0Vdc
Input threshold	0.3Vdc
Maximum input	25Vdc
Input impedance	100kΩ min.
Output current	1A peak (each gate)
Off state dv/dt	100V/μs
Fusing (optional)	150mA high speed 412-217 (see connection diagram)
Auxiliary output	5V,4mA dc max. (short circuit protected

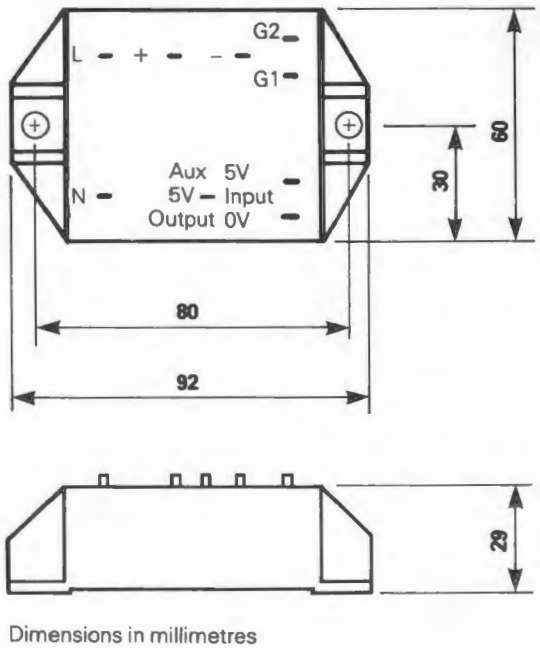
General

Isolation	2500Vrms input/output
Line voltage	240Vac + 10%/ − 15%
Supply frequency	47-53Hz
Operating temperature	0°C to + 55°C
Storage temperature	−20°C to +70°C
Input signal/firing angle	linear

Features

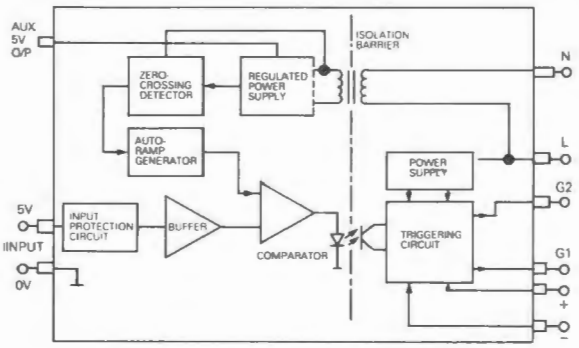
- Fully isolated 2.5kV input to output
- Can be used for ac or dc control
- Identical fixing centres as encapsulated thyristor and diode modules
- Will trigger different current rating thyristors without any modification
- No external components required
- Auxiliary 5V supply.

Dimensions and connections



Dimensions in millimetres

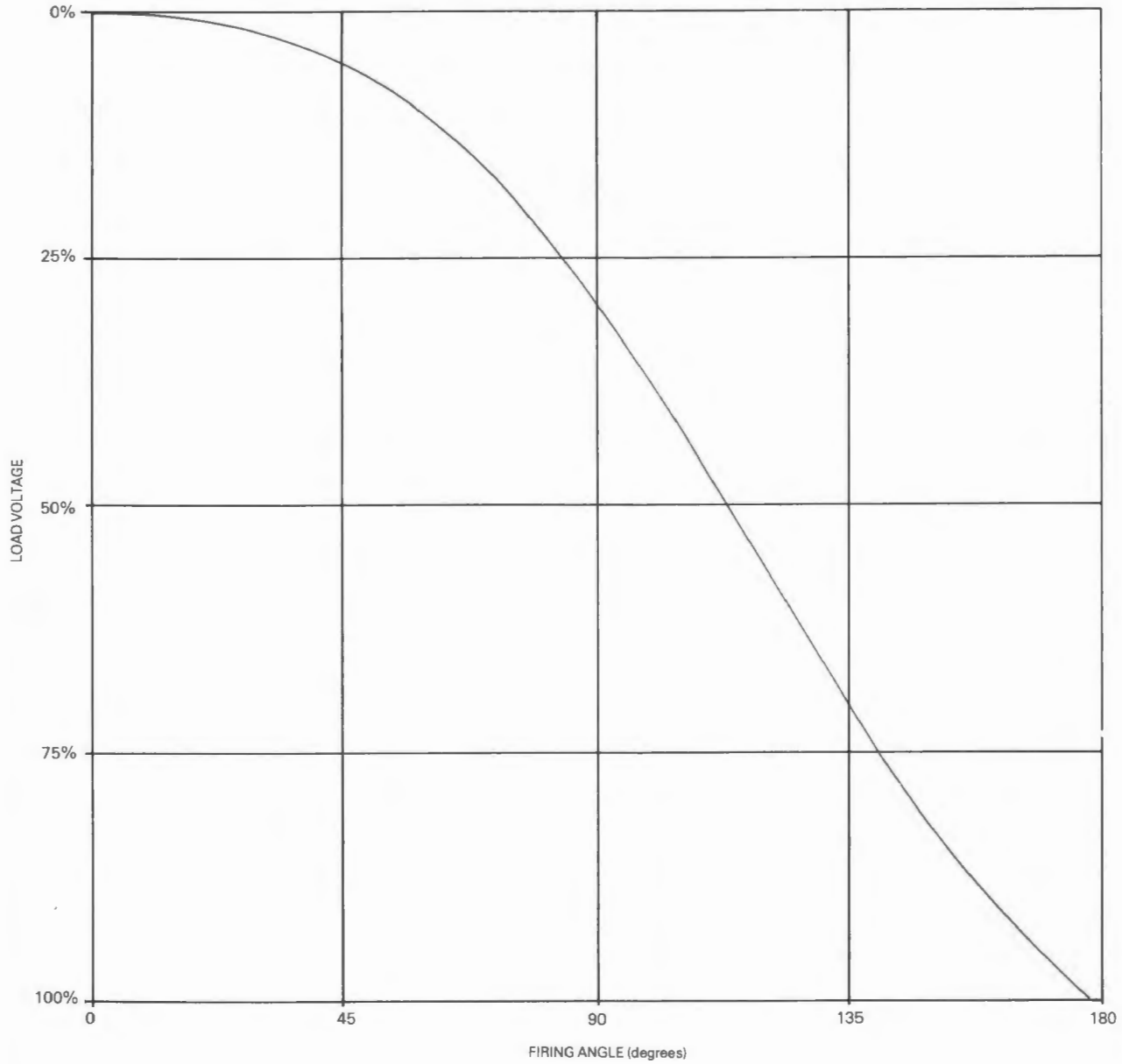
Figure 1 **Phase angle trigger module block diagram**



The phase angle trigger module contains all the synchronizing, timing, driving, buffering and isolating circuitry necessary to drive thyristor pairs in a phase control mode. A block diagram for the unit is shown in Figure 1. The input port is completely isolated from the mains and trigger terminals with an isolation specification of 2500Vac.

A control voltage of 0 to 5Vdc applied to this input port will provide control of the thyristor firing angle from 0 to 180°. The relationship between the control voltage and the thyristor firing angle is linear, however as the firing angle is referred to the control of a sine wave the effective load voltage will vary as indicated in the graph (Figure 2).

Figure 2 **Load voltage versus firing angle**



Applications

A typical arrangement for the control of an ac load is shown in Figure 3. The thyristor ratings should be chosen to be adequate for the load. Generation of radio frequency interference (RFI) is inherent with phase control. A suitable mains filter for loads up to 1kW is available Stock No. 238-479. This circuit arrangement is ideally suited for the control of lighting and motor loads.

DC loads may be controlled using the arrangement shown in Figure 4. This uses a single phase half controlled bridge to provide control of a dc load from an ac mains source.

Dv/Dt protection

The module can stand up to 100 V/μs rate of rise of off state voltage. If the load is resistive, generally there is no need to put a snubber RC network to protect the trigger module. When an inductive load is used, a snubber RC (Rs and Cs) network should be connected as shown in Figure 3 or Figure 4 to protect the trigger module and the thyristors. The value of the RC network is calculated by the equations given below.

The value of the snubber capacitors, Cs is micro Farads

$$Cs = \frac{Irms\ (Vrms + 500)}{5000 \quad (Dv/Dt)^2}$$

where, Irms is the maximum rms load current
Vrms is the rms supply voltage
Dv/Dt (100 V/μs) is the trigger module maximum allowable rate of rise of off stage voltage.

and the value of the snubber resistor, Rs in ohms

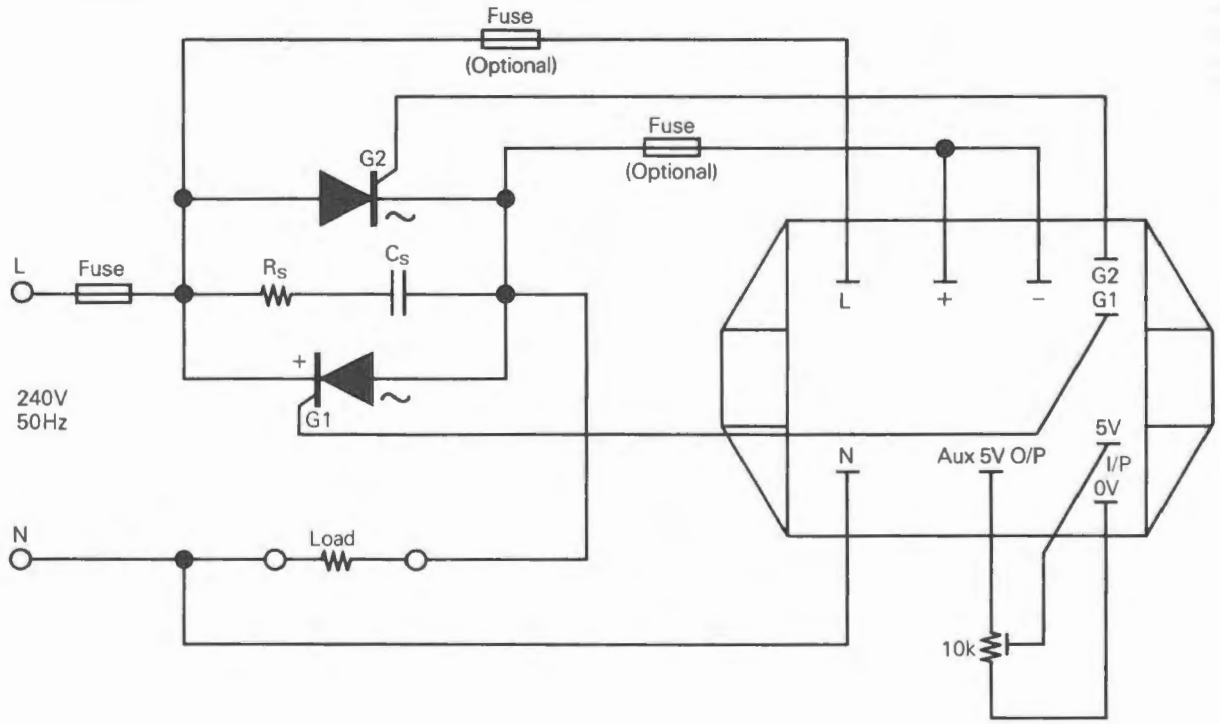
$$Rs = \frac{300}{Cs \times Dv/Dt}$$

with a dissipation (in W) of

$$P = 2 \times 10^{-6} \times Cs \times Vrms^2 \times f$$

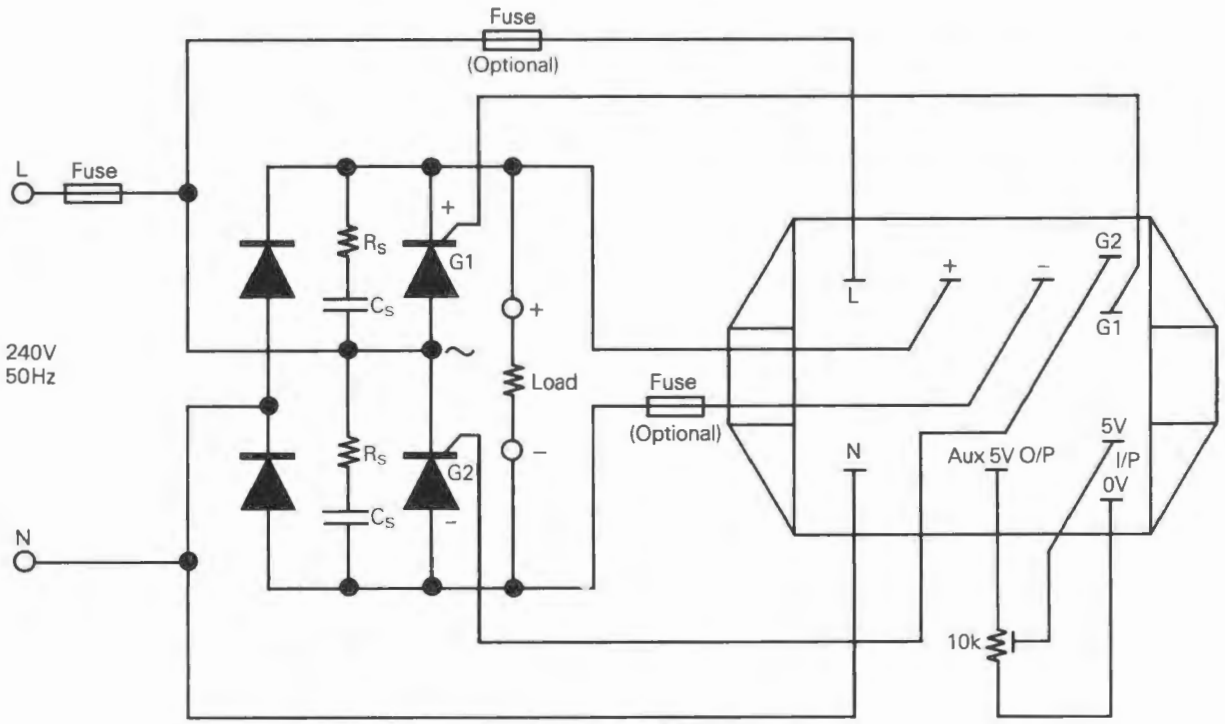
where, f is the operating frequency (in Hz). With ac controllers, f is double the value of the operating frequency.

Figure 3 **Single phase inverse pair WIC configuration (AC-AC control).**



RS data

Figure 4 **Single phase half controlled bridge – B2HZ configuration (AC-DC control).**



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RS data

Hybrid power amplifiers

HY60 Stock number 303-236
MOS 248 Stock number 301-707

Two hybrid audio-power amplifiers with output powers of 30W or 120W. These versatile devices form the basic building blocks for constructing high quality amplifiers using a minimum of additional components.

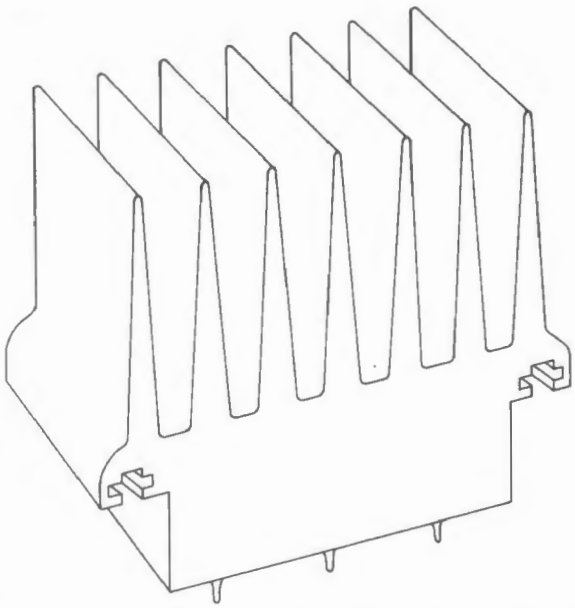
Features

- 30W and 120W versions available
- Fully encapsulated
- Integral heatsinks
- Only five external connections necessary

HY 60

The RS HY 60 is a fully encapsulated high quality power amplifier with integral heatsink capable of delivering 30W continuous power into an 8Ω load. Operating from ±25V (typical) supply rails, the amplifier requires no external passive components, only five connections being necessary; input, output, positive rail, negative rail and ground. 'T' slots in the heatsink facilitate mounting using the M3 nuts and screws supplied.

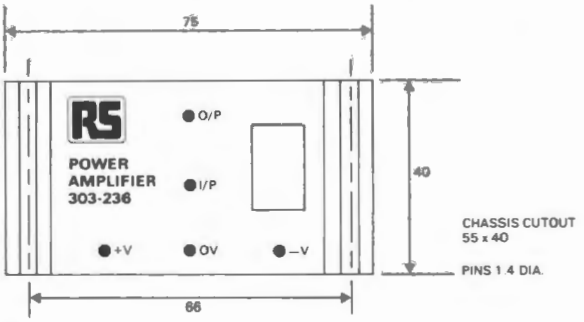
Figure 1



Electrical characteristics

Parameter	Typ.
Output power	30W rms into 8Ω
Frequency response (–3dB)	15Hz-50kHz
Total harmonic distortion (Typical) at 1kHz	0.015%
Intermodulation distortion	<0.006%
Signal to noise ratio (DIN AUDIO)	100dB
Slew rate	15V/μs
Rise time	5μs
Input sensitivity	500mV
Input impedance	100kΩ
Load impedance	4Ω to ∞
Damping factor (8Ω at 100Hz)	>400
Supply voltage	±25V (±30V max) (±15V min with reduced O/P)
Supply current	1A (8Ω load) 2A (4Ω)

Figure 2 **Pin connections (viewed from base)**



PIN 1 — Positive Supply Voltage
PIN 2 — Output
PIN 3 — Input
PIN 4 — 0 Voltage
PIN 5 — Negative Supply Voltage

Figure 3 **THD v. output power at 1kHz**

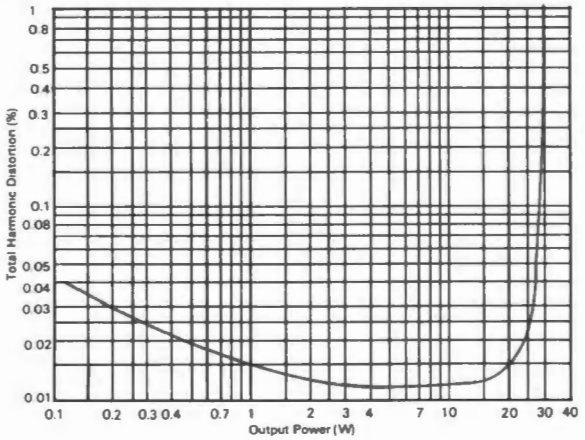
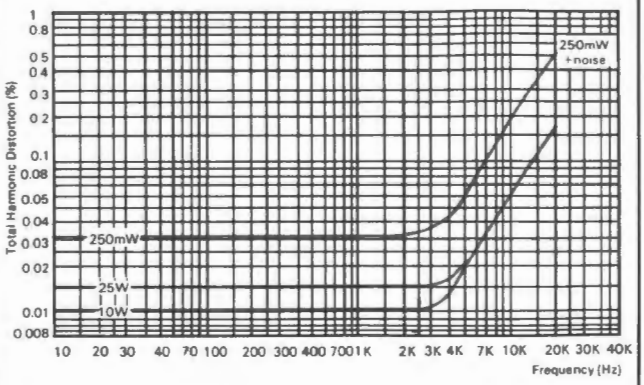


Figure 4 **THD v. frequency**

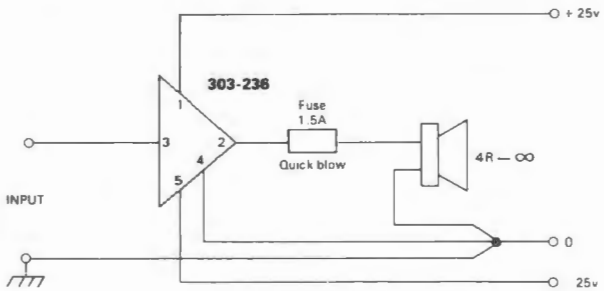


Notes

1. For normal conditions no supplementary heat sink is needed: the amplifier must however, be mounted to allow a vertical flow of air through the fins.
2. The amplifier must be powered from a true split line (symmetrical) supply and under no circumstances should an attempt be made to use a single line.
3. No input capacitor is required as the module incorporates an internal capacitor of 100V working.
4. Internal circuits are designed to protect the amplifier against abnormal loads. Short circuits can be tolerated for ten seconds. However, for loudspeaker protection it is recommended that a 1.5amp quickblow fuse is mounted between the output and the speaker.
5. 'Star earthing' techniques should be observed to avoid hum-loops, i.e. all 0 volt connections, including speaker return leads, should be made at the power supply.

Application

Figure 5 **Application circuit**



6. Long power supply connecting leads may lead to instability of the power amplifier. This will appear as H.F. oscillation at the output and prolonged operation in this condition will cause damage to the modules.

MOS 248

The RS MOS 248 is a fully integrated high quality power amplifier with an integral heat-sink. The module incorporates a VMOS output stage and is capable of delivering 120W continuous power into an 8Ω load. Operating from ±55V (typical) supply rails the amplifier requires only five external connections: input, output, positive rail, negative rail and ground, plus one external resistor. 'T' slots in the heatsink facilitate mounting using the M3 nuts and screws provided.

Figure 6

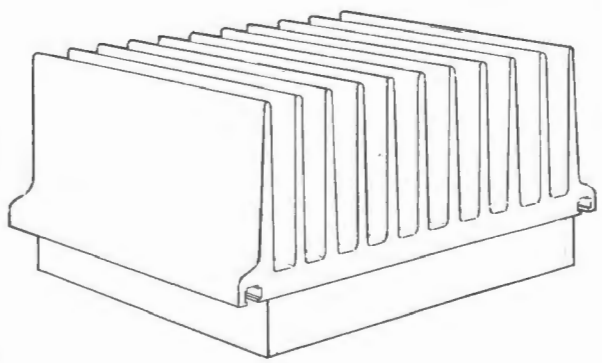
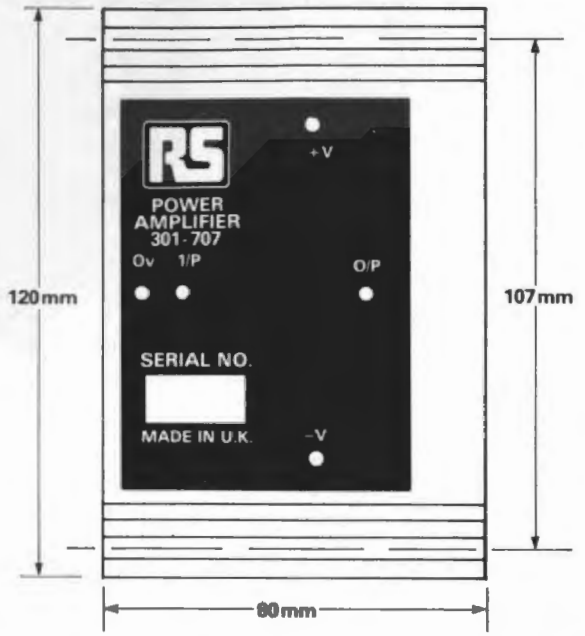


Figure 7 **Pin connections (viewed from base)**



Electrical characteristics

Parameter	Typ.
Output power	120W rms into 8Ω
Frequency response (–3dB)	15Hz-100kHz
Total harmonic distortion (Typical) at 1kHz	0.005%
Intermodulation distortion	<0.006%
Signal to noise ratio (DIN AUDIO)	100dB
Slew rate	20V/μs
Rise time	3μs
Input sensitivity	500mV rms
Input impedance	100kΩ
Load impedance	4Ω to ∞
Damping factor (8Ω at 100Hz)	>400
Supply voltage	±55V (±60V max)
Supply current	1.8A (8Ω load)

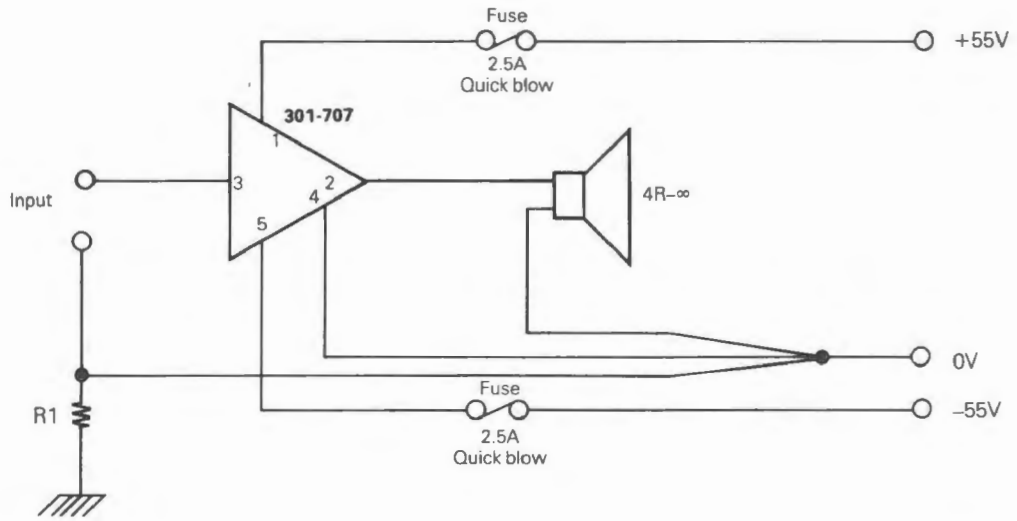
Notes:

1. For normal usage and conditions the amplifier needs no supplementary heatsink; it must however, be mounted to allow a vertical flow of air through the fins.
2. The amplifier must be powered from a true split line (symmetrical) supply and under no circumstances should an attempt be made to use a single line.
3. No input capacitor is required owing to an internal capacitor of 100V working.
4. As the amplifier has no built in protection circuitry, apart from the inherent protection characteristics of MOSFETs themselves, it is advised that a 2.5A quick blow fuse be mounted in the positive **and** the negative supply lines. Fuses in these positions will also give adequate protection for a loudspeaker of nominal impedance, providing the recommended fuse rating is not exceeded.
5. Star earthing techniques should be observed to avoid hum-loops i.e. all 0 volt connections, including speaker return leads, should be made at the power supply.
6. On power leads greater than 2ft long, it is essential that a local decoupling capacitor is fitted between the +V and –V terminals of the amplifier – typical value being 1μF with DC working voltage >120V (114-014).

RS data

Application

Figure 8 **Application circuit**



In order to prevent earth loop problems when a pre-amplifier is connected the fitting of a resistor (R_1) is recommended in the position shown. The value is not critical but should be between 82 and 270Ω 0.25W.

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RS data

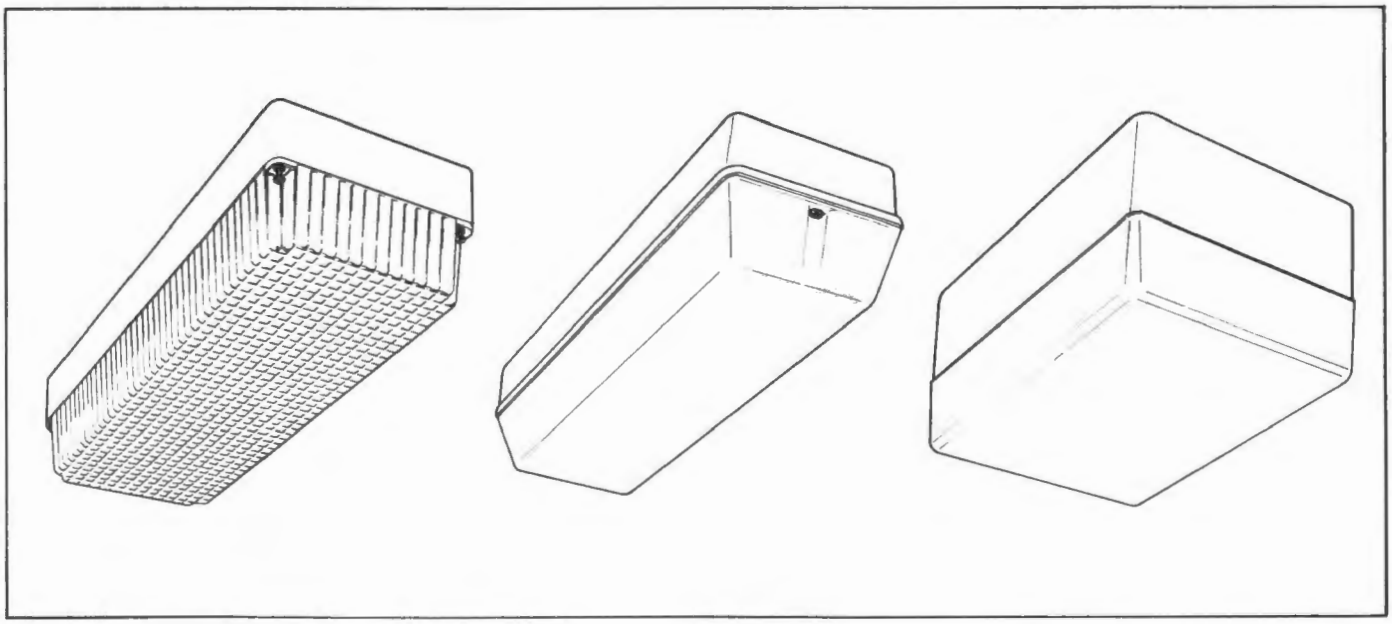
Emergency lighting

A comprehensive range of emergency lighting equipment certified to ICEL 1001.1980. The performance of operation is guaranteed when installed to the requirements of BS5266 Part 1, code of practice for emergency lighting. All luminaries have Greater London Council and Lancashire County Council approval.

A range of 'Exit and Emergency Exit' self-adhesive labels is available. The lettering is matt green and complies with BS5266 Part 1.

Features

- Certified to ICEL 1001.1980
- Comprehensive range
- Totally self contained
- High light output
- Vandal resistant
- Easy installation
- Three hour duration



Stock Number	Type	Light Service	Light Output (Lumens)		Battery	Input Voltage	Recharge Time
			Emergency	Normal			
565-793	8W non-maintained	300mm 8W fluorescent tube	180	–	Nickel-cadmium 4.8V 4Ah	250V 50Hz	24 hrs
565-800	8W maintained	300mm 8W fluorescent tube	180	180	Nickel-cadmium 4.8V 4Ah	250V 50Hz	24 hrs
565-816	6W non-maintained	225mm 6W fluorescent tube	140	–	Nickel-cadmium 3.6V 4Ah	250V 50Hz	24 hrs
565-822	2.4W non-maintained	2 x 1.25W Xenon filled bulbs	20	–	Nickel-cadmium 2.4V 4Ah	250V 50Hz	24 hrs
565-838	8W non-maintained bulkhead	200mm 8W fluorescent tube	180	–	Nickel-cadmium 3.6V 4Ah	250V 50Hz	24 hrs

Why emergency lighting?

Anyone involved in the management of hotels, boarding houses, licensed premises and places of public entertainment has the responsibility of complying with the provisions of the 1971 Fire Precautions Act. In addition the Health and Safety at Work Act 1974 requires that all shops, offices, factories and other places of work must now be brought under the same provisions and infers that emergency lighting is necessary, if employees are likely to be on the premises during the hours of darkness or in areas without sufficient daylight, to ensure that escape routes can be effectively illuminated.

Other statutory documents relating to emergency lighting are:

Fire Certificates (Special Premises) Regulations 1976

Cinematograph Act 1952.

Cinematograph (Safety) Regulations 1955, No. 1129.

The Factories Act 1961.

The Office, Shops and Railway Premises Act 1963 (means of escape against fire in offices, shops, railway premises, Safety Health and Welfare Booklet).

The Theatre Act 1968.

The Private Places of Entertainment (Licensing) Act 1967.

The Gaming Act 1968.

The Manchester Corporation Act of 1965 (Section 18).

Additionally, there is a number of Codes of Practice, specifications and Local Authority Standards which include:

B.S.5266: Part 1 – Code of Practice for Emergency Lighting of Premises 1975.

ICEL: 1003: 1982; Emergency Lighting Applications Guide.

B.S.2560: Exit Signs in Cinemas etc.

The G.L.C. Specification for self-contained Emergency Lighting.

The Lancashire County Council Emergency Lighting Specification.

The Manchester Emergency Lighting Specification.

Applications for emergency lighting

a) escape lighting.
b) safety lighting.
c) standby lighting.

Escape lighting is where the level of illumination needs to be maintained at all times to ensure adequate illuminance throughout all escape routes. The minimum illuminance as recommended by BS5266 Part 1 is 0.2 lux in the most adverse conditions.

Safety lighting is where the level of illumination needs to be maintained at such a level that there is no risk to persons involved in potentially hazardous processes, should the normal lighting fail.

Standby lighting is lighting of sufficient illuminance to carry on normal activities on the failure of main lighting. The required lighting level depends on the activity or process.

Types of emergency lighting

Local authorities and fire brigades will often specify the type of lighting required and should always be consulted when appropriate.

There are two basic types of lighting unit; maintained units which are illuminated at all times and non-maintained units which are only illuminated when a power failure occurs. There are many applications for both but in general EXIT signs require permanent illumination, and maintained fittings should be used. Non-maintained lighting is usually applicable elsewhere. However, this is only a general guidline and advice should be sought if uncertain.

Units can be incandescent or fluorescent; each with its own advantages. Large areas usually require fluorescent lighting for maximum light output and local or smaller areas can often be adequately lit by incandescent units. Remember however, that emergency lighting means lighting to see by in an emergency and lives may depend on good visibility.

It is better, therefore, to use fluorescent units whenever possible to give maximum emergency cover.

Installation guide

All emergency lighting installations should comply with BS5266 Part 1. The British Code of Practice for Emergency Lighting, and there is no substitute for careful study of this standard or other relevant specifications as mentioned previously.

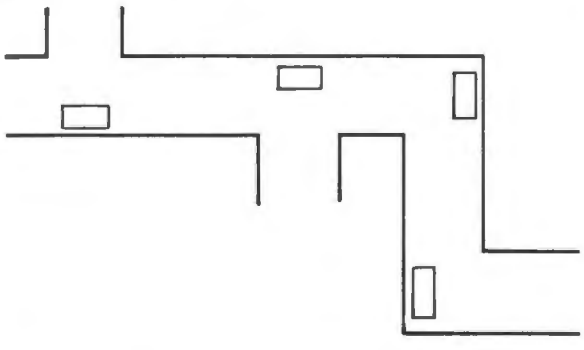
In general BS5266 Part 1 specifies the position of luminaires and a minimum illuminance of 0.2 lux throughout all escape routes. All exit, emergency exit and escape route signs are required to be illuminated at all times.

Careful thought and consideration should be given to the emergency lighting scheme and it is well worth drawing a plan of the escape routes and then the number and spacing of the emergency lights required by using the spacing table.

The positioning of luminaires should be such that all exit doors, inside and out, emergency exits and potential hazards are well illuminated. For example:

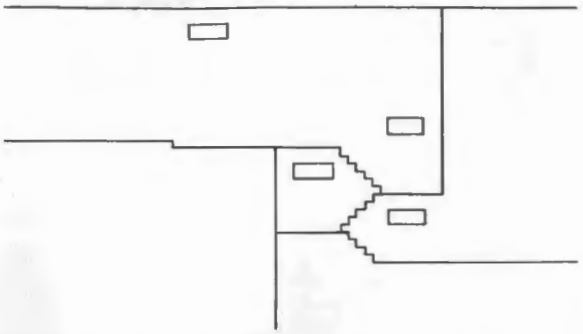
a) Where corridors intersect or change in direction.

Figure 1 **Corridor installation**



b) Near any change in floor level which may constitute a hazard and on staircases so that each flight of stairs receives direct light.

Figure 2 **Staircase installation**



Escape lighting should also be extended to cover the following areas:

a) Covered car park walkways.
b) Toilets and cloakrooms exceeding 8 square metres.
c) Passenger lifts.
d) All fire alarm call points and fire fighting equipment.
e) Plant, switch and control rooms.

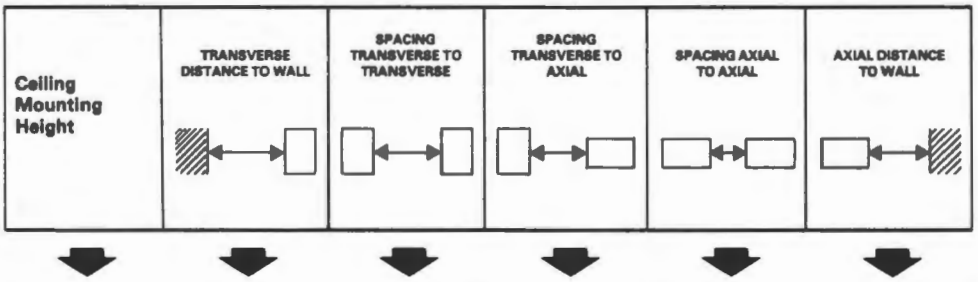
Although 0.2 lux is the recommended minimum, it is often the position of a hazard, not the lighting level, which determines the number of luminaires for large areas or long corridor runs. The spacing table will be of assistance, but two important factors should be borne in mind. Firstly, luminaires must not cause glare or create a difference between the brightest and the darkest areas of more than 40:1 (uniformity ratio). Secondly, it is wise to allow for deterioration due to dust, changes in decor, fall-off in lamp or battery performance and aim for about 0.4 lux as a minimum light level. If the spacing, when installing fluorescent luminaires, is reduced by 25% for wall or ceiling mounting and when installing incandescent luminaires if the spacing is reduced by 25% for ceiling mounting and 35% for wall mounting, then a service factor of 0.5 will be achieved which will allow for deterioration with age. Some allowance has been made in the table by quoting the next lowest whole number.

Consideration must also be given to accessibility for maintenance such as for cleaning of the diffuser and lamp changing. The fittings should also not be sited where their temperature is likely to exceed 25°C or go below 0°C.

Self-contained emergency lighting luminaires may be wired in PVC insulated cable and connected to the lighting sub-circuits so that they are activated in the event of power failure to those circuits.

Spacing tables for ceiling mounting units

Spacing tables based on end discharge voltage, aged lamps, no reflectance and average production units. All measurements in metres to next lowest figure. This guide is for ceiling mounted units.



Model	Metres	Spacing in metres				
8W Fluorescent	2	5	12	10	9	4
	2.5	5	13	11	10	4
	3	5	14	12	11	4
	4	6	15	13	12	4
	5	6	16	14	13	5
	6	6	16	15	14	5

Model	Metres	Spacing in metres				
6W Fluorescent	2	4	11	10	8	4
	2.5	5	12	12	9	4
	3	5	12	12	10	4
	4	5	14	12	11	4
	5	5	14	13	12	4
	6	4	14	13	12	4

Model	Metres	Spacing in metres				
2.5W Incandescent	2	2	5	5	5	1
	2.5	1	5	5	5	1
	3	1	5	5	5	1
	4	–	4	4	4	–
	5	–	2	2	2	–
	6	–	1	1	1	-

Emergency lighting models

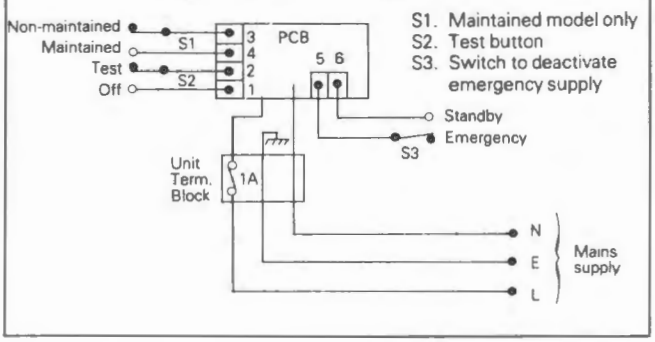
8W maintained

The RS565-800 8W fluorescent, 3 hour, maintained, emergency lamp is housed in a polycarbonate fire resistant case with a clear polycarbonate diffuser. This model has many features making it useful for a wide range of applications as described below.

Maintained/non-maintained operation

This luminaire can be switched from maintained to non-maintained operation whilst still retaining the emergency mode in the event of mains failure. This is easily achieved by removing the link from terminals 3 and 4, on the printed circuit board, and connecting a mains switch in its place (Figure 3).

Figure 3 **Single unit switching**



Up to 10 emergency lighting units may be wired in banks from a single switch by removing the link from terminals 3 and 4, and connecting a second 'live' supply through a 1 amp fused spur and switch to terminal 4 (leave terminal 3 open). Operation of switch 'S1' will convert all units from maintained to non-maintained operation (Figure 4).

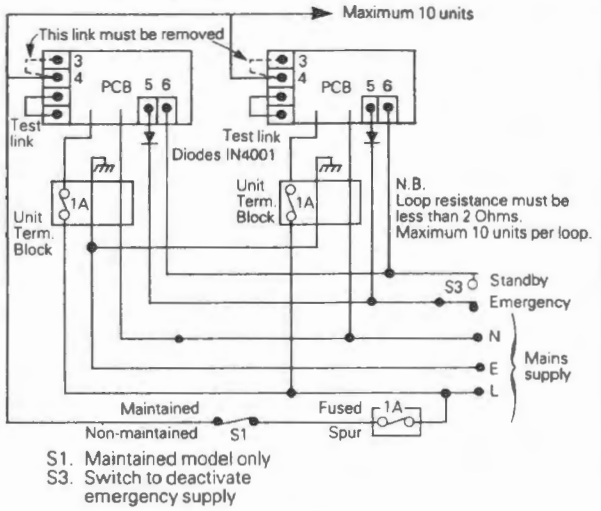
Test switch

The facility is provided to connect a remote test button or test key switch to the luminaire. This must be a 'push to break' and is connected in place of the link across terminals 1 and 2. When operated it disconnects the mains supply from the unit thereby switching over to the Emergency Mode. In this position the red indicator will extinguish and the emergency lamp light.

Note: If fitted this facility must be protected against interference.

WARNING: Isolate the mains supply before connection. This switch and associated wiring carries mains voltage.

Figure 4 Multiple unit switching



Switch to deactivate emergency supply

Where premises are unoccupied for most of the time (e.g. Village Hall with only very occasional occupation) and in the event of a power failure emergency lighting is not required, this can be deactivated by completing a link between terminals 5 and 6. (A key switch is strongly recommended for security reasons.) This must be open for normal operation and closed to deactivate the emergency supply.

This facility can also be remote bank switched by adding a suitable diode in each circuit (Figure 4).

Note: The mains supply must not be removed from the unit even though the premises are unoccupied to ensure that the battery is kept fully charged, also ensure that the luminaire is not in the non-maintained mode.

Ensure that these functions are permitted by your local authority before installation.

8W Non-maintained

The RS565-793 8W fluorescent, 3 hour non-maintained emergency lamp is manufactured to the same design as the 8W maintained model and has the same outward appearance, thus ensuring uniformity in a lighting scheme.

This luminaire is particularly useful where maintained types are not required such as switch rooms of sub-stations etc. When wired in the 'deactivated' mode it gives the facility to be switched on when required providing a full 3 hours illumination for repair or maintenance work. The unit can be wired as the 8W maintained lamp for bank switching (Figures 3 and 4).

8W Non-maintained bulkhead

The RS565-838 8W fluorescent, 3 hour, non-maintained, weatherproof bulkhead, emergency lamp is environmentally protected to IP55. Applications include walkways, car parks and warehouses.

6W Non-maintained

The RS565-816 6W fluorescent, 3 hour, non-maintained emergency lamp is housed in a fire resistant polycarbonate black galley with an opal diffuser. This model is ideal for smaller installations where good illumination is required without the switching facilities of the 8W models.

2.5W Non-maintained

The RS565-822 2.5W incandescent, 3 hour, non-maintained emergency lamp is of similar design to the 6W fluorescent unit and uses the same galley and diffuser. This luminaire is suitable for illuminating narrow corridors, changes in direction, fire fighting appliances and any other area requiring local illumination.

The unit incorporates two 1.25W Xenon filled lamps with a long life. The filaments are constantly monitored by being illuminated at 10% of full brightness in the non-emergency mode.

Legends

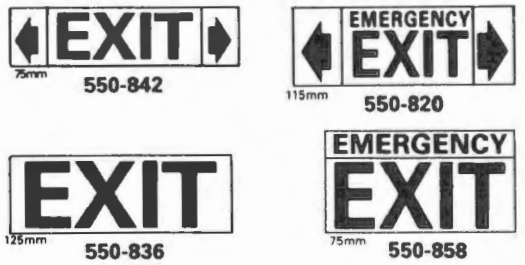
Self adhesive labels are available to convert the RS emergency light fittings into Exit signs.

All legends are self adhesive and provide a permanent bond after 24 hours. Supplied on a suitable backing paper containing the necessary instructions. Letters are matt green and comply with BS5266 Part 1 for the appropriate viewing distance.

Where arrows are provided the legend face is pre-cut allowing these to be discarded if not required. Legend RS550-858 is also pre-cut for either EXIT or EMERGENCY EXIT use. All legend backgrounds are clear for maximum light transmission particularly on incandescent models.

Exit signs should generally be illuminated constantly and the use of maintained luminaires is recommended for this application.

Figure 5 **Exit signs**



Fixing details

Figure 6 **8W Non-maintained and maintained**

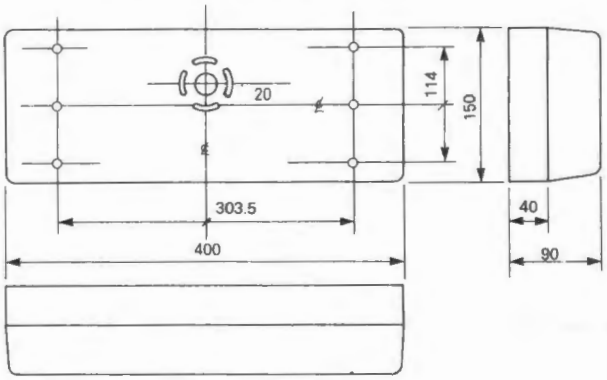


Figure 7 **6W and 2.5W Non-maintained**

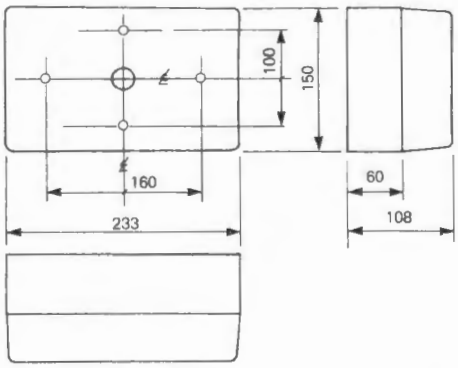
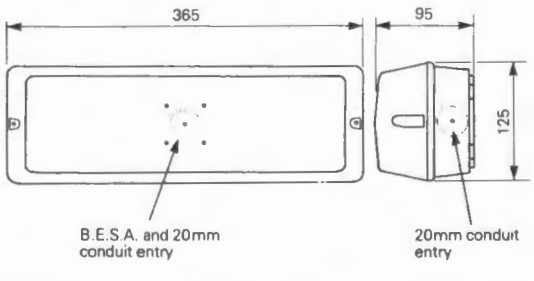


Figure 8 **8W Non-maintained bulkhead**



RS data

Testing and maintenance

A programme of routine testing is described in BS5266 Part 1 and this should be strictly adhered to. The minimum testing and maintenance is as follows:

Tests

1. Every month isolate mains supply and check the emergency lamp lights (or use test button if fitted).

2. Every six months isolate mains supply for at least one hour and check that the emergency lamp remains alight for this period.

3. Biennially isolate mains supply for three hours and check that the emergency lamp remains alight for this period. Ensure that the building will be unoccupied for the following 24 hours to completely recharge the batteries.

Preventative maintenance

Clean the diffuser at regular intervals. Every nine months replace fluorescent lamp on maintained models. Every four years replace battery assembly (or at other intervals if the duration test does not satisfy the 3 hour requirement).

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RS data

3½ digit LCD DPM i.c.

Stock number 301-684

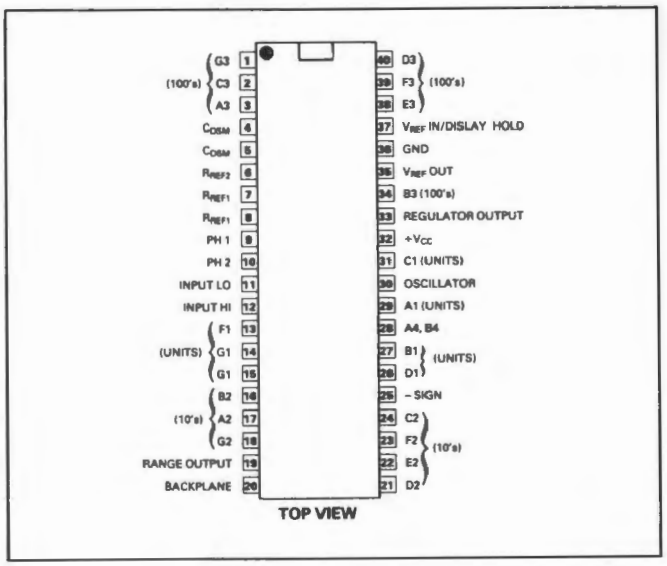
The 451 is a complete monolithic 3½ digit single chip digital voltmeter i.c. The auto-zero function is digital and so does not need a capacitor for storing the error voltage. Output signals for external auto-zero switches are available so that op-amps or other signal conditioning circuits can be included in the auto-zero loop. This allows input impedance modification or input sensitivities of as low as 1.999 mV full-scale to be achieved.

Absolute maximum ratings

Supply voltage V_{CC} ——— –0.5 to +7V
Max. voltage all other inputs ——— –0.5 to V_{CC} +0.5V
Operating temp. range ——— 0°C to +70°C
Storage temp. range ——— –55°C to +125°C

Features

- Access to auto-zero loop allows inclusion of external circuits
- Full scale reading of 1.999mV is possible
- Digital auto zero with guaranteed zero reading for 0V input
- True polarity at zero for null detection
- Direct drive for a liquid crystal display
- On-chip clock and reference
- Underrange and overrange indication
- Single supply rail



Electrical characteristics V_{CC} = +5V T_{AMB} = +25°C

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply voltage	Direct connection Using on chip shunt reg.	4.5 6.0	5.0	5.5	V V
Supply current		—	4	6.5	mA
Shunt regulator Output voltage		4.5	5.0	5.5	V
Sink current		—	—	15	mA
Display O/P peak voltage		—	$\pm V_{CC}$	—	
D.C. component		—	—	±25	mV
Backplane frequency		—	½2000	—	oscillator frequency
Full scale reading		–1999	—	+1999	
Zero reading	V_{IN} = 0, V_{FS} = 200mV	–000.0	±000.0	+0.000	Reading
Rollover error	$-V_{IN} = +V_{IN} = \pm$ 200mA Conversion time ≥0.5s	–2	0	+2	Counts
Linearity	V_{FS} = 200mV, conv. time ≥0.5s	–1	0	+1	Count

Parameter	Conditions	Min.	Typ.	Max.	Units
Common mode range		1.8	—	3.8	V
Common mode rejection		—	120	—	μV/V
Supply rejection		—	100	—	μV/V
Input offset current		—	0.1	1	nA
Input resistance		—	20	—	MΩ
Zero temp. coefficient		—	—	1	μV/°C
Oscillator freq. range		—	—	300	KHz
Conversion time	48000 oscillator periods	250	—	—	ms
Ref. output voltage		1.26	1.3	1.35	V
Temp. coefficient		—	±50	±80	ppm/°C
Knee current		—	—	150	μA
Maximum sink current		1	2	—	mA

Figure 1 **System diagram**

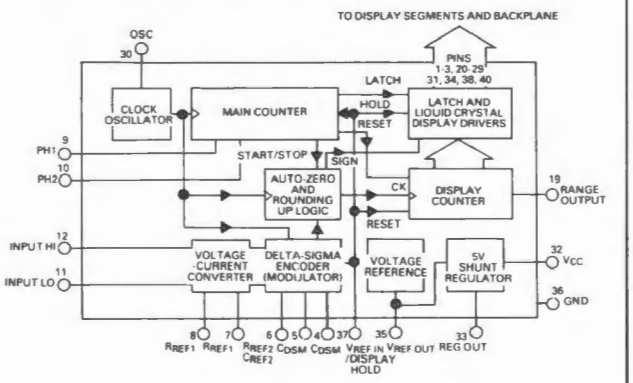
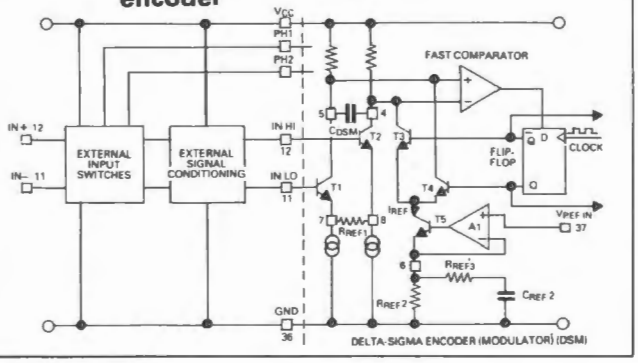


Figure 2 **Input switching and delta-sigma encoder**



General description

The ZN451 utilises a charge-balancing conversion principle, which offers a number of advantages over the more common dual-slope integration method.

These include a fixed conversion time which is independent of the analogue input voltage, completely digital auto-zero and inherently bipolar operation. Linearity is also extremely good over the entire input voltage range, unlike some dual-slope designs where stray capacitance can cause problems around zero.

The auto-zero loop of the ZN451 is external to the device so that op-amps and other signal-conditioning circuits can be included within it and thus have their zero errors removed.

The conversion time of the ZN451 is divided into two periods, Phase 1 and Phase 2, unlike the dual-slope system which has three distinct phases, signal integrate, reference integration and auto-zero.

The heart of the ZN451 is the delta sigma encoder, a simplified circuit of which is shown in Figure 2.

The delta-sigma encoder of the ZN415 consists of a voltage-current converter comprising T_1 and T_2, a reference generator A_1/T_5 and a feedback loop containing a fast comparator, D-type flip-flop and current switches T_3 and T_4. These can switch a current $I_{REF} = V_{REF}/R_{REF2}$ into the collector circuit of either T_1 or T_2, depending on the state of the flip-flop.

The polarity of the voltage across capacitor C_{DSM} is monitored by the comparator, whose output is sampled on every clock pulse by the flip-flop. The outputs of the flip-flop switch I_{REF} into the collector circuit of either T_1 or T_2 so as to oppose the existing voltage on C_{DSM} i.e. to maintain the average charge acquired by D_{DSM} at zero, thus keeping the circuit in equilibrium.

Assuming perfect symmetry in the circuit, with zero volts applied between the bases of T_1 and T_2 their collector currents will be equal, and the only charge acquired by C_{DSM} will be that put on it by I_{REF}. The flip-flop will thus change state on every clock pulse so that C_{DSM} will alternatively acquire charge quanta of $+I_{REF}T_C$ and $-I_{REF}T_C$ (where T_C is the clock period) and the nett charge acquired will be zero. The output of the flip-flop will thus be a square-wave with a 50% duty cycle.

During the measurement the voltage to be measured is applied between the bases of T_1 and T_2 and is converted into a current $I_{IN} = V_{IN}/R_{REF1}$ flowing in R_{REF2}. This produces a different current $2\,I_{IN}$ in the collector currents of T_1 and T_2, so that the charge acquired by C_{DSM} is no longer equal and opposite ($\pm I_{REF}$) but is now $(I_{REF} - 2I_{IN})\,T_C$ when T_4 is turned on and $(-I_{REF} - 2\,I_{IN})\,T_C$ when T_3 is turned on.

In order to maintain equilibrium the flip-flop will now no longer change state on every clock pulse but will remain in one state for a longer period than it remains in the opposite state, i.e. $N_1T_C(I_{REF} - 2I_{IN}) + (N - N_1)\,T_C(-I_{REF} - 2I_{IN}) = 0$ where N_1 is the number of clock pulses for which the flip-flop Q output is a '1' and N is the total number of clock pulses over which the measurement is made and assuming N is so large that quantising error can be ignored.

Thus $N_1(I_{REF} - 2I_{IN}) = (N - N_1)(I_{REF} + 2I_{IN})$

And $\frac{2N_1 - N}{N} = \frac{2I_{IN}}{I_{REF}}$ i.e. $N_1 - \frac{N}{2} = \frac{NI_{IN}}{I_{REF}} = \frac{NV_{IN}R_{REF2}}{R_{REF1}V_{REF}}$

In other words, if a counter is allowed to count N_1 and $N/2$ is subtracted from it by (initially presetting the counter to $-N/2$) then the result is directly proportional to V_{IN}, assuming N, V_{REF1} and R_{REF2} are fixed. With zero input voltage the DSM duty-cycle should be 50%, N_1 should equal $N/2$ and the accumulated count should be zero. In practice, of course, this will not be the case due to offsets and component mismatching in the DSM. Fortunately, an interesting property of the DSM allows the zero error to be removed digitally.

If the DSM output is taken from the $\overline{Q}$ output of the flip-flop instead of the Q output then the number of pulses counted over a period of N clock pulses will be not N_1 but $N\text{-}N_1$. Thus, if the counter is preset to $-N$ instead of $-N/2$ the number accumulated in the counter after N clock pulses will be $-N_1$. In other words, taking the $\overline{Q}$ output of the DSM and presetting the counter to $-N$ gives a result proportional to minus the input voltage. This is what occurs during phase 1.

Clearly, if the input voltage is the same during phase 1 and phase 2 the counter will accumulate a count of $-N_1$ during phase 1 and add a further N_1 pulses during phase 2, giving a total count of zero. If the input voltage is zero during both phases the system will measure minus the zero error during phase 1 and plus the zero error during phase 2, thus giving an automatic zero reading.

Obviously when measuring an actual input voltage the DSM must not see the same voltage during both phases, otherwise a zero reading will always result whatever the input. The input voltage must thus be switched, and this can be achieved in two ways. Most obvious is to disconnect the input voltage during phase 1 and connect it during phase 2, so that the result is proportional to $-V_{OS} + (V_{OS} + V_{IN}) = V_{IN}$. Alternatively the polarity of the input voltage can be reversed during phase 1 so that the result is proportional to $-(V_{OS} - V_{IN}) + (V_{OS} + V_{IN}) = 2V_{IN}$. This of course means that the component values must be calculated for twice the required full-scale reading, i.e. for 200mV full-scale the components would be calculated for 400mV. This can be achieved simply by doubling the value R_{REF1}.

The second method has advantages where a large input overload margin is required before the DSM saturates. This occurs when its duty-cycle is 0% or 100%, i.e. when $I_{IN} = \pm\frac{I_{REF}}{2}$ and N_1 = zero or N. (N = 5000 in the ZV451).

Overrange occurs at a reading of ±2000. The duty cycle of the DSM at this point depends on the input switching method used.

Whatever method is used, with zero input voltage the counter will count 2500 clock pulses during phase 1 and 2500 during phase 2 to give a reading of zero (assuming negligible zero-error). Using the first input switching method the signal is measured only during phase 2, so an additional 2000 clock pulses must be counted during phase 2, i.e. a total of 4500 clock pulses must be counted during phase 2.

Substituting in $I_{IN} = \frac{(N_1 - N/2)I_{REF}}{N}$ to find the required value of I_{IN} for overrange $I_{IN} = 0.4 \times I_{REF}$FS. The overload margin before DSM saturates is thus $1/10 I_{REF}$ or 25% of full-scale.

Using the second input switching method the input signal is measured during both phases, so for a full-scale reading an additional 1000 clock pulses will be counted due to the input voltage in each phase, giving a clock total of 3500 clock pulses in each phase.

Therefore substituting $I_{IN} = \frac{(N_1 - N/2)I_{REF}}{N}$ to find the required I_{IN} for overrange.

$I_{IN} = 0.2\,I_{REF}$.

The overload margin before the DSM saturates is thus $0.3\,I_{REF}$ or 150% of full-scale. i.e. input switching method (b) gives six times the overload margin of method (a).

Input switching method (b) has several other interesting properties, some of which can usefully be exploited.

Figure 3 **Voltage follower input circuit**

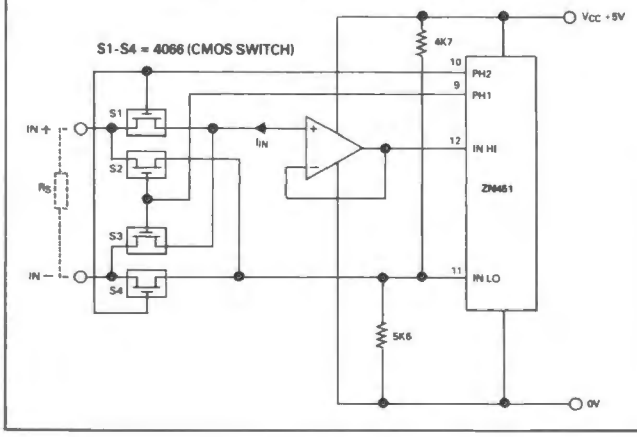
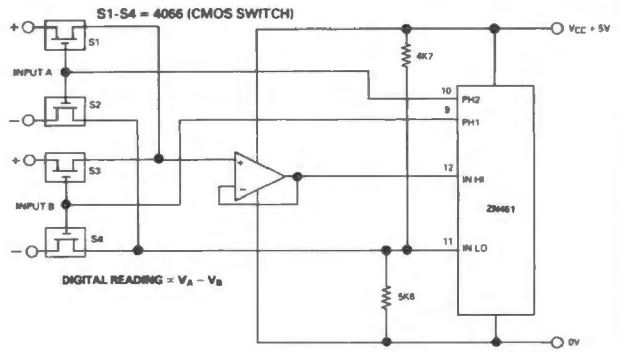


Figure 3 shows the simplest possible configuration using an op-amp as a voltage follower to boost the input resistance. Suppose this is a J-FET op-amp with an input current of around 100pA. Suppose a 10M resistor is connected between input + and input −. The input current of the op-amp will generate a voltage of 1mV across this resistor. However, this will not cause a zero error since the direction of current flow, and hence the polarity of the voltage, is the same during phase 1 and phase 2.

Therefore, using switching method (b), high resistance sources will not cause zero errors, subject to the proviso that the error voltage does not cause saturation of the DSM.

Figure 4 **Sum or difference measurement**



The two measurement phases of the ZN451 can also be used to perform other functions. By re-configuring the input switches to measure one input voltage during phase 1 and a second input voltage during phase 2 it is possible to measure the sum of difference of the two voltages, depending on their relative polarity. This is shown in Figure 4.

Timing diagram

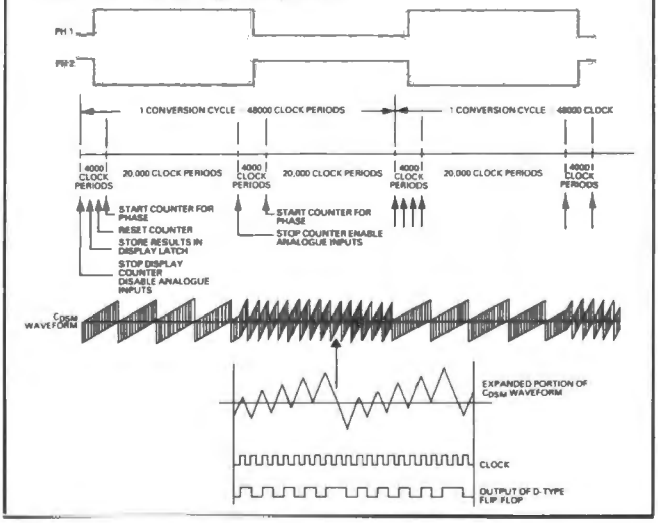
The value of N chosen for the ZN451 is 5000, so each phase of the measurement should take 5000 clock pulses, a total of 10,000 for the whole measurement. However, the display counter of the ZN451 is preceded by a divide-by-four counter which performs several functions.

Firstly it provides two guard bits so that quantising errors between phase 1 and phase 2 measurements do not give rise to spurious zero errors of ± 1, but are confined to the (non-displayed) guard bits.

Secondly, it provides information to the polarity and rounding up logic, which drives the − sign. The divide-by-four stage means that the display counter sees only one-quarter of the pulses from the DSM and each phase must thus run for 20,000 clock pulses. Furthermore, each measurement phase is separated by a pause of 4000 clock periods to allow the input switches to settle. One measurement cycle thus takes a total of 48,000 clock periods.

Figure 5 is a timing diagram of the ZN451 which clearly shows the two measurement phases and the operation of the DSM. Two control signals PH_1 and PH_2 indicate which measurement phase is active. These outputs are CMOS compatible and can be used directly to drive input switches such as the 4066, CMOS switch.

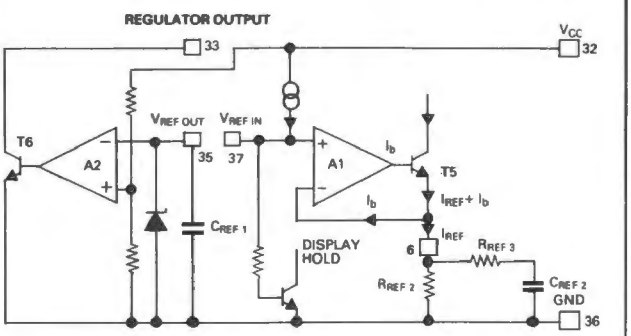
Figure 5 **Timing diagram**



Reference Loop and Supply Shunt Regulator

The reference current defining loop is shown in more detail in Figure 6.

Figure 6 **Reference current loop and supply shunt regulator**



A reference input voltage applied to the non-inverting input of A_1 causes the output of A_1 to bias T_5 such that the inverting input of A_1 assumes the same potential and a current $V_{REF\ IN}/R_{REF2}$ flows R_{REF2}. By making the input bias current A_1 the same as the base current of T_5 this base current flows into the inverting input of A_1 instead of through R_{REF2}. The reference current flowing in the collector of T_5 is therefore almost identical to the current flowing in R_{REF2}. The reference loop is stabilized by C_{REF2} and R_{REF3}.

A highly stable on-chip bandgap reference of approximately 1.28V is provided and this may be used by linking $V_{REF\ OUT}$ to $V_{REF\ IN}$ when the reference will be biased on by the 150μA current source connected to the non-inverting input of A_1. The on-chip reference is stabilized by C_{REF1}. The on-chip reference also provides the reference voltage for the on-chip supply regulator A_2. This compares V_{REF} against $V_{CC}/4$ and controls V_{CC} with transistor T_6 such that the two are kept equal, i.e. V_{CC} = 5V. The supply regulator can be configured as a shunt or series regulator using only a few external components. If $V_{REF\ OUT}$ is not connected to $V_{REF\ IN}$ but supply regulation is still required then the on-chip reference must be biased on by a 22k resistor to V_{CC}.

Supply voltage options

The ZN451 is designed to be extremely flexible with regard to supply voltage and four power supply options are possible allowing operation over a wide range of supply voltages. These options are illustrated in Figure 7.

The first option is to ignore the on-chip regulator and to connect an externally stabilized voltage of 4.5 to 5.5V direct to pin 32, for example a 5V logic supply.

For supply voltages greater than 6V the on-chip shunt regulator (pin 33) may be used by linking pins 32 and 33. When using the shunt regulator an

external resistor must be placed in series with the supply to limit the regulator current as shown in Figure 7(b). The value of this resistor is given by:

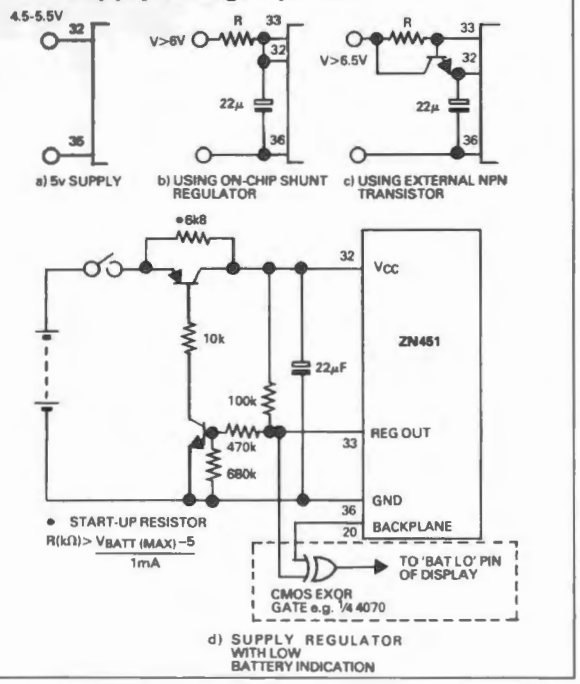
$$R = \frac{V_{supply} - 5 \text{ volts}}{6.5} \left(k\Omega = \frac{V}{mA}\right)$$

which allows for the maximum 6.5mA current consumption of the I.C.

If the supply voltage is unstabilized then R should be calculated using the minimum supply voltage that will be encountered. The current drawn by this configuration increases with supply voltage as the shunt regulator sinks more current in order to maintain V_{CC} at 5V. The maximum allowable supply voltage is thus determined by the 15mA maximum rating of the shunt regulator, assuming very little current is drawn by the DVM circuitry, i.e.

$$V_{max} = 15(mA) \times R(k\Omega) + 5 \text{ volts}$$
$$= (3V_{min} - 10) \text{ volts}$$

Figure 7 **Supply voltage options**



Since the current drawn by the shunt regulator increases with supply voltage this configuration is not recommended for battery operation where long battery life is a prime criterion, as the current drawn from a new battery could be up to 2.3 times the maximum current consumption of the DVM.

For battery operation a series regulator circuit is recommended which can be constructed using one or two external transistors controlled by pin 33. The simplest series regulator, shown in Figure 7(c), uses a single NPN transistor and allows operation down to about 6.5V. Current consumption of this circuit is the normal current consumption of the DVM plus the base current of the transistor.

The base resistor must be chosen such that it can supply sufficient base drive when the supply voltage is a minimum assuming:

a) Maximum DVM current of 6.5mA

(b) Maximum shunt regulator voltage of 5.5V

(c) Minimum gain of the transistor

Now base current I_b (mA) $= \frac{V_{min} - V_{reg} - V_{beT1}}{R_b}$

required base current $= \frac{6.5mA}{h_{fe\ (min)}}$

Therefore R_b (kΩ) $= \frac{(V_{min} - V_{reg} - V_{beT1}) \times h_{fe}}{6.5}$

$$= \frac{(V_{min} - 6) \times h_{fe}}{6.5}$$

Example: The circuit is to operate down to 6.5V with a transistor type whose minimum gain is 80

$$R_b = \frac{(6.5 - 6) \times 80}{6.5}$$

$$= 6.1k$$

Nearest value of 5k6 is used.

Although a great improvement on the shunt regulator, the circuit of Figure 7c still does not achieve maximum battery life since V_{min} must always exceed the regulator voltage by V_{beT1} plus the voltage drop across R_b.

For the ultimate in battery life the circuit of Figure 7d is suggested. This allows operation down to voltages as low as $V_{reg} + V_{CE(sat)T1}$ and, as an added bonus, it automatically detects the end of useful battery life, i.e. the point which the regulator ceases to function.

T_1 is a PNP series regulator transistor controlled by pin 33 via T_2, which provides the required signal inversion. During normal operation the voltage drop across R_1 is small since the base current required by T_2 is only a few hundred nanoamps, and the voltage at pin 33 is not much above the V_{be} of T_2 (about 0.6V).

When the battery voltage drops to $V_{reg} + V_{CE(sat)T1}$ the voltage at the non-inverting input of the regulator amplifier will fall below V_{REF} and the shunt regulator output transistor will turn off causing the voltage at pin 33 to rise to about 80% of supply.

Pin 33 can conveniently be connected to a low battery indicator consisting of a CMOS EXOR gate, as shown in the dotted box. When pin 33 is low the output of the EXOR gate will be in phase with the backplane and the LO BAT indicator will be extinguished. When pin 33 is high the output will be out of phase with the backplane and LO BAT will be visible.

Oscillator options

The on-chip oscillator of the ZN451 may be used with various configurations of external components, as shown in Figure 8. It will operate with only an external capacitor, which may be fixed, or variable to adjust the oscillator frequency. Alternatively the frequency may be adjusted by placing a variable resistor in series with the capacitor. Graphs of oscillator versus capacitor and resistor values are given in Figure 9. if absolute accuracy of the oscillator frequency is required then a crystal or ceramic resonator may be used as the frequency determining element. By making the integration time a whole number of mains cycles a degree of mains interference rejection can be provided. For example a 100kHz crystal gives an integration time of 200ms which is 10 cycles at 50Hz mains frequency or 12 cycles at 60Hz, the total measurement interval being 480ms or just over two conversions/second.

If mains interference is superimposed on the input signal it is important that its peak amplitude should not be large enough to cause saturation of the

DSM. If this is not the case then the ZN451 should be preceded by a lowpass filter to give additional mains rejection.

The final option is to overdrive the oscillator input from a TTL or CMOS gate, as shown in Figure 8d.

In order to maintain an adequate drive to the comparator the value of C_{DSM} must also be changed in proportion to the oscillator period. A table of suitable values is given blow.

Figure 8 **Oscillator options**

Oscillator frequency (kHz)	C_{DSM} Min.	C_{DSM} Max.
50	200n	2μ
100	100n	1μ
150	68n	680n

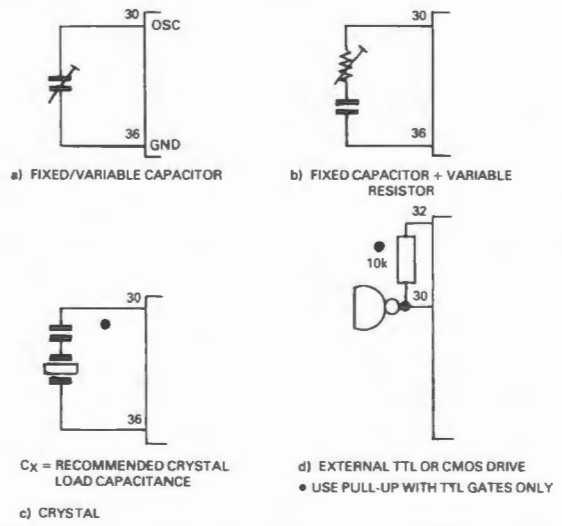
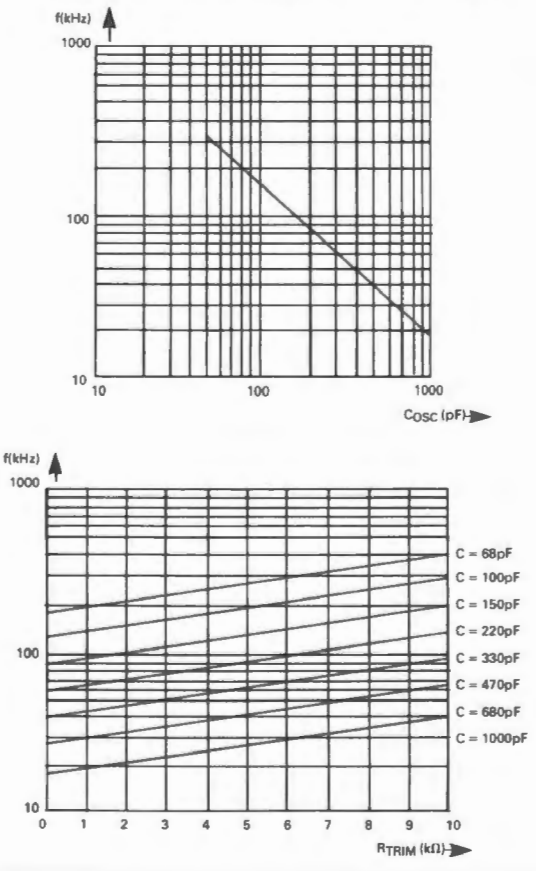


Figure 9 **Oscillator Frequency vs External Capacitor and Resistor**



Range Output

To simplify the design of auto-ranging instruments, underrange and overrange detection circuits are provided in the ZN451. Overrange is indicated when the count exceeds 1999, whilst underrange is indicated for counts less than 150. This provides a degree of hysteresis to prevent the instrument jittering between ranges, which could occur if underrange was indicated at a count of 199 and there was a mismatch in the attenuators or other signal conditioning circuits.

Because the pins of the ZN451 are fully utilised it is not possible to provide separate underrange and overrange pins, so a single three-state output is provided.

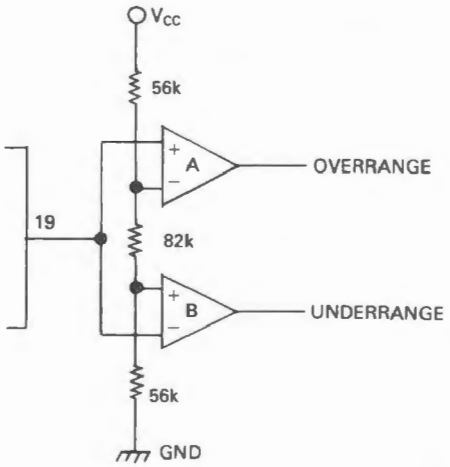
If the measurement is in range then pin 19 will be at $V_{CC}/2 \pm 0.5V$ with a source resistance of approx. 40k.

For an overrange measurement pin 19 will go HIGH for 1000 clock pulses synchronous with the data store pulse at the end of the measurement. For an underrange measurement pin 19 will pulse LOW in a similar manner. In each case the output resistance is approx. 80k.

The range output can be fully decoded using a dual comparator, as shown in Figure 10.

A visual overrange indication is also provided. In this condition the leading digit of the display shows a '1' whilst all other digits are blanked.

Figure 10 **Decoding the range output**



Range Output	Output A	Output B
Underrange (GND)	0	⎍
In Range (½ V_{CC})	0	0
Overrange (V_{CC})	⎍	0

Display Hold

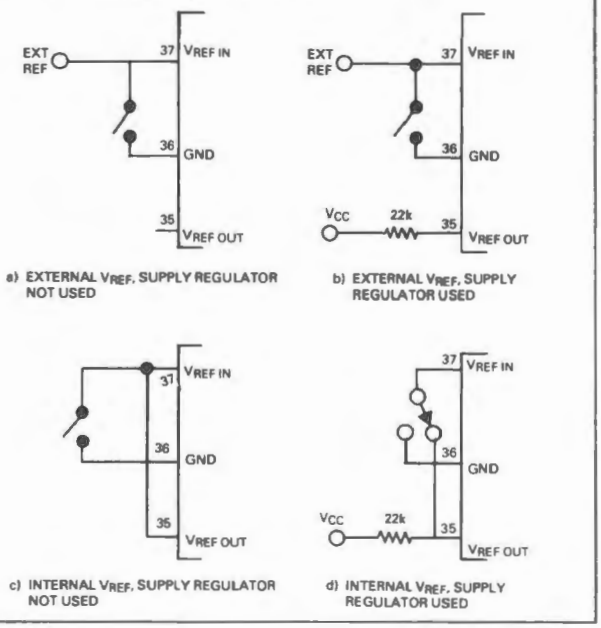
The reference input, pin 37, also doubles as a display hold pin. If this pin is grounded then the display will continue to show the results of the last valid measurement until pin 37 is released. Display hold also resets the system counters and a new measurement begins immediately display hold is released. The method of activating display hold depends on whether or not the on-chip reference and shunt regulator are being utilised.

If an external reference voltage is used (pins 35 and 37 not joined) then display hold can be activated by grounding pin 37 with a single-pole switch, transis-

tor or open-collector logic gate, provided that the external reference is not required to supply other circuits. If the on-chip regulator is to be used then pin 35 must, of course, be biased up with an external 22k resistor so that V_{REF} can supply the reference voltage for the regulator. If the on-chip reference is used but the on-chip regulator is not then display hold can be activated in a similar manner by grounding the junction of pin 35 and pin 37.

However, since the on-chip reference also provides the reference voltage for the on-chip regulator pin 35 must not be grounded if the regulator is in use or the supply voltage will drop to zero. If the on-chip reference and shunt regulator are both used then pin 37 must be disconnected from pin 35 before it grounded to activate display hold. This is illustrated in Figure 11. As pin 37 normally supplies the bias current for the on-chip reference this must be provided by an external 22k resistor when these pins are not linked.

Figure 11 **Display Hold Options**



Backplane Output

The backplane output normally supplies a square-wave of the same frequency as, but 180° out of phase with, the active segment outputs. This provides the necessary a.c. drive to the L.C. display. By grounding the backplane output the a.c. drive to the segments may be inhibited and the segment outputs become normal active low (TRUE = 0) outputs. This facility is useful if the output data is to be used for some purpose other than display driving. An L.C. display should not be connected to the ZN451 in this condition as d.c. drive will eventually damage it.

Decimal Point Drive

The ZN451 provides all the output necessary to drive the segments of a 3½ digit liquid crystal display. However, in order to drive decimal points and annunciators such as low battery indicators, some external components are required. To turn on a decimal point it is necessary to provide it with a drive signal of the same frequency as, but 180° out of phase with, the backplane output. For driving a single, fixed decimal point, the simple inverter circuit of Figure 12a can be used.

If more than one decimal point is to be selected then it is necessary for the unused decimal points to be switched off by arranging their drive waveforms to be in phase with the backplane output. This is simply achieved using exclusive OR gates as shown in Figure 12b.

Figure 12a **Driving a Fixed Decimal Point**

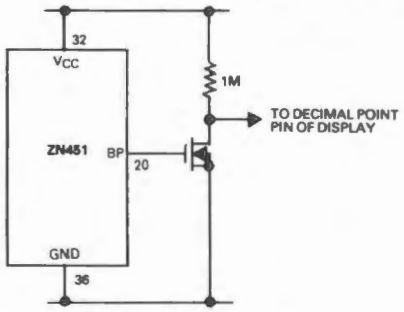
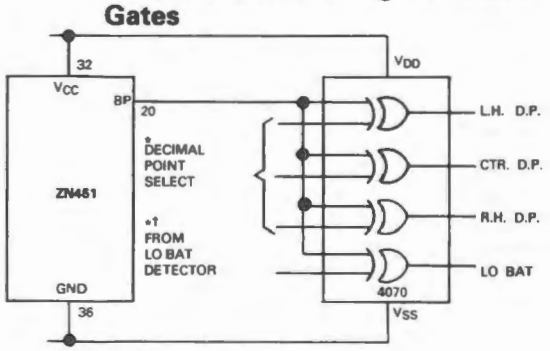


Figure 12b **Decimal Point Select and 'LO BAT' Indicator Drive using Exclusive OR Gates**



A logic '1' on the input causes the output waveform to be out of phase with the backplane and the appropriate decimal point is activated. Conversely a logic '0' causes the output to be in phase with the backplane. A single 4070 CMOS quad-EXOR gate I.C. will provide the drive for the three decimal points of a 3½ digit liquid crystal display plus the drive to a low battery indicator. A suitable low battery detection circuit is shown in Figure 7d.

Calculation of Full-Scale Range

The component values for any full-scale range depend on the input switching method used. Using method (a) the input voltage is measured only during phase 2, so the equation

$$\frac{NV_{IN}R_{REF2}}{V_{REF}R_{REF1}} = N_1 - \frac{N}{2}$$ holds.

Since N = 5000 and full-scale reading = ± 1999 this equation can be rewritten as

$$V_{IN}\text{ (full-scale)} = \frac{\pm 1999\, V_{REF}R_{REF1}}{5000\, R_{REF2}}$$

$$\frac{\pm 0.4\, V_{REF}R_{REF1}}{R_{REF2}}$$

from which required values of R_{REF1} and R_{REF2} can be calculated for any required full-scale input voltage, using either the internal reference of 1.3V or an external reference.

Using input switching method (b) the input voltage is measured during both phases so the displayed count is twice as large for the same input voltage and component values.

The describing equation thus becomes

$$V_{IN}\ (\text{full scale}) = \frac{\pm\ 0.2\ V_{REF}R_{REF1}}{R_{REF2}}$$

Using input switching method (b) the same full-scale range as method (a) can be obtained if the value of R_{REF1} is doubled or the input signal is attenuated by a factor of two.

These equations are in fact not exact since they do not take account of the reference amplifier offset voltage, which is typically ± 5mV. This offset means that I_{REF} is not precisely $V_{REF}/R_{REF2} \cdot r_e$ of T_1 and T_2 in the voltage-current converter also appears in series with R_{REF2} (typically 5k). In practice this is not a problem since the tolerance of the on-chip reference means that a calibration adjustment must be provided anyway. Using the on-chip reference voltage of 1.26- 1.35 volts the recommended component values for a full-scale reading of 199.9mV would be R_{REF1} = 200k or 400k, R_{REF2} = 500k (min), 530k (max.). Allowing for the use of 2% tolerance components for R_{REF1} and R_{REF2} an adequate adjustment range for calibration purposes will be provided if R_{REF2} is made up of a 470k resistor in series with a 100k multiturn trimmer. Full-scale ranges less than 200mV can be accommodated by reducing the value of R_{REF1}, thus producing the same full-scale input current for a smaller input voltage. The limitations on the minimum value of R_{REF1} are caused by non-linearity in the voltage-current converter, offsets in the auto-zero switches, and the fact the r_e becomes a much larger proportion of R_{REF1}. These factors place a practical limit of about 20k on R_{REF1}. As R_{REF1} is reduced, the gain temperature coefficient will also tend to increase.

Similarly full-scale ranges greater than ±200mV can be accommodated by increasing the value of R_{REF1}. The maximum input voltage that can be applied is limited by the common-mode range of the differential inputs.

The full-scale range can also be adjusted by varying R_{REF2} which determines the reference current, and indeed placing a preset in series with R_{REF2} is the recommended method of calibration.

I_{REF} can also be varied by using an adjustable external reference voltage instead of the internal reference, which makes ratiometric operation possible.

The maximum value of I_{REF} is limited to about 3μA since above this value the voltage-current converter becomes non-linear. The minimum value of I_{REF} is not quite so well defined as it is determined by deterioration in the performance of current switches T_3 and T_4 at low collector currents. The minimum useable value of I_{REF} is typically 500nA. This means that the upper and lower limits are $V_{REF}/500nA$ and $V_{REF}/3\mu A$ respectively. The upper and lower limites on V_{REF} itself are determined by the common-mode range of the reference current amplifier A_1 which is 1 to 1.5V. Radiometric operation with a variable V_{REF} within these limits is possible provided that the upper or lower limit of I_{REF} is not exceeded.

Practical Applications and Design Precautions

Since the input switching of the ZN451 is external to the device it is possible to include op-amps and other signal conditioning circuits within the auto-zero loop and thus eliminate their zero errors.

The two methods of input switching are shown in Figures 13a and 13b. In Figure 13a a series switch and shunt switch disconnect the input signal during phase 1. In Figure 13b a switch bridge reverses the polarity of the input signal during phase 1.

Figure 13a **Input switching**

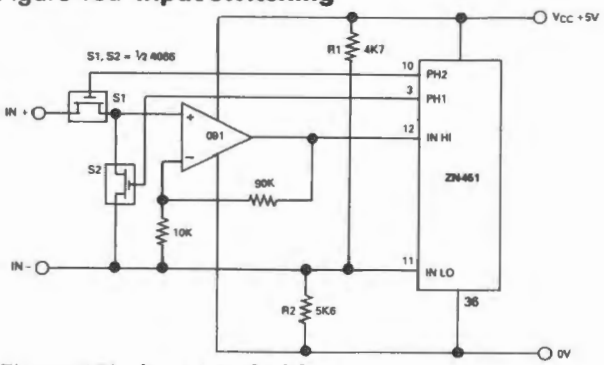
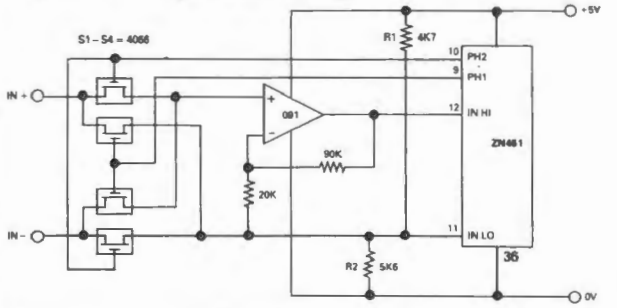


Figure 13b **Input switching**



Two practical circuits for 20mV full-scale DVM are given in Figures 13a and 13b. In the circuit of Figure 13b note that the gain of the op-amp is 5 since the effective full-scale sensitivity of the ZN451 is 100mV, whereas in Figure 13a it is 200mV. The same result could be achieved by making the op-amp gain 10 in both cases but doubling the value of R_{REF1} in Figure 13b.

These simple circuits can be used to illustrate some design precautions that must be observed when using the ZN451.

1. The output voltage of the signal conditioning circuits should be within the common-mode range of the ZN451.

2. The common-mode and differential input voltages must be within the input range of the switches and signal conditioning circuits.

These two criteria are met in Figures 13a and 13b by providing an analogue common point at approximately + 2.5V by means of R_1 and R_2. Assuming battery operation of the ZN451 this analogue common point will float up and down with the common-mode volatge of the input signal thus keeping the input voltage within the common-mode range of ZN451 and the input circuits.

3. The offset error at the input of the ZN451, when added to the full-scale input voltage, must not cause saturation of the DSM. Using input switching method (b) this means that the zero error can be 150% of the full-scale range of the DVM.

When designing signal conditioning circuits care must be taken to ensure that this limit is not exceeded.

In many circuits the principal souce of zero error will be the offset voltage of the op-amp, in which case a good rule of thumb is that the input offset voltage should not exceed the full-scale input voltage, to allow some overload margin to be retained.

However, in some signal conditioning circuits there may be sources of zero error other than the op-amp, in which case care must be taken to meet the offset criteria at the ZN451 inputs. An example of such a circuit is given in Figure 15.

Using low-cost monolithic op-amps it is a simple matter to design for full-scale inputs of ±20mV or less. For inputs below 2mV more expensive instrumentation amplifiers must be used. Alternatively the offset can be nulled out when calibrating the DVM, leaving the auto-zero to cope with long term and temperature drift of the zero.

4. There should be no rapid temperature fluctuations in the signal conditioning circuits as this could cause the zero error to vary from phase 1 to phase 2.
Example, with full-scale input of 1.999mV and an op-amp with an offset tempco of 10μV/°C a 0.1°C change in temperature between phase 1 and phase 2 will cause a zero error of 1μV = 1 count.

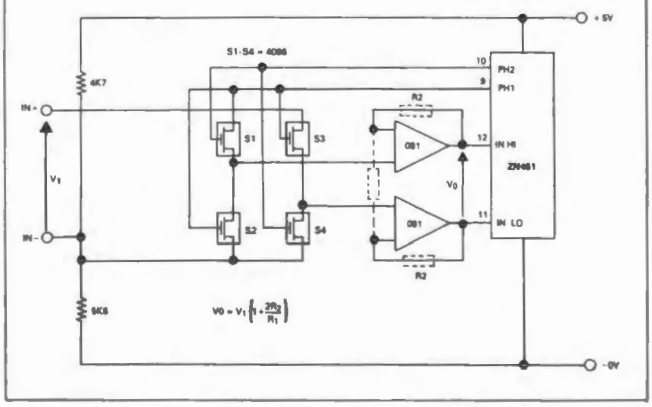
This is likely to be problem only with very small full-scale ranges. It can be reduced by thermally insulating the signal conditioning circuits or by potting them to increase the thermal inertia so that the temperature can only change slowly.

5. With very small input voltages thermal e.m.f.'s may become a problem. In this case care should be taken to ensure that the input + and input − signal paths to the conditioning circuits are identical so that thermal e.m.f.'s cancel out. Such precautions may include the use of identical input switches in series with both the input + and input − leads.

Although Figure 13b shows the simplest way of implementing input switching method (b), using only one op-amp, this configuration may have disadvantages in some applications, since the input LO terminal of the ZN451 is tied permanently to analogue common, whilst the input voltage is reversed. This means that the supply rails of the ZN451 shift up and down with respect to the input signal common. This is generally not a problem in battery-powered circuits unless the signal source impedance is very high, when charging and discharging of stray capacitance may cause errors.

Figure 14 shows a circuit in which the signal 0V is connected to a fixed analogue common whilst the inputs of the ZN451 are reversed. In order that the input impedanced seen by the signal is the same during both measurement phases both inputs of the ZN451 are driven from identical op-amp circuits. These are shown as voltage followers but can be given greater than unity gain by adding the dotted components.

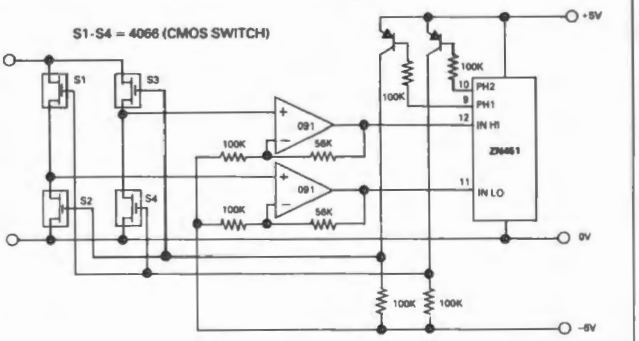
Figure 14 **Ground referenced input**



In some systems it may be necessary for analogue common to be the 0V supply rail or some other voltage not within the common-mode range of the ZN451.

This can be achieved by offsetting the output voltage of the signal-conditioning circuits to bring it within the common-mode range of the ZN451. Also if the input voltage falls outside the V_{CC} and 0V rails of the ZN451 the supply voltage to the analogue switches must be such that they can accommodate the signal, and the PH_1 and PH_2 outputs of the ZN451 must be level-shifted in order to control the switches. An example of such a circuit is shown in Figure 15. This is a ±200mV DVM operating from ±5V with the 0V rail as analogue common.

Figure 15 **Input conditioning**



The ZN451 operates from the +5V and 0V rails whilst the input switches and op-amps operate from ±5V. Two PNP transistors convert the 0 to +5V swing of the PH_1 and PH_2 outputs to a ±5V swing. Since they also invert the outputs the PH_1 and PH_2 outputs are transposed.

The two op-amps are connected in a non-inverting configuration but with the feed-back network returned to –5V instead of 0V. By making the op-amp gain 1.56 this gives an offset of approx. +2.8V with a 0V input which brings the output within the common-mode range of the ZN451.

Since the op-amp gain is 1.56 the values of R_{REF1} and R_{REF2} must be chosen for ±312mV full-scale to give a full-scale input range of ±200mV.

In this circuit there are two sources of zero error for which the ZN451 must compensate: firstly the offset voltages of the two op-amps multiplied by their gain; secondly and more significant the difference in the quiescent op-amp output voltages caused by gain mismatching between the two op-amps.

$$\pm\ [5 \times (\text{max. gain } A_1 - \text{min. gain } A_2)]$$

$$= \pm \left\{ 5 \times \left(\frac{98 + 57}{98} - \frac{102 + 55}{102} \right) \right\}$$

$$= \pm\ 212\text{mV}$$

This is 68% of the full-scale input range of the ZN451, which is acceptable.

RS data

Additional Input Conditioning Circuits

Figure 16 **Input attentuator**

For the measurement of voltages from 20mV to 2kV. This has a standard input resistance of 10M.

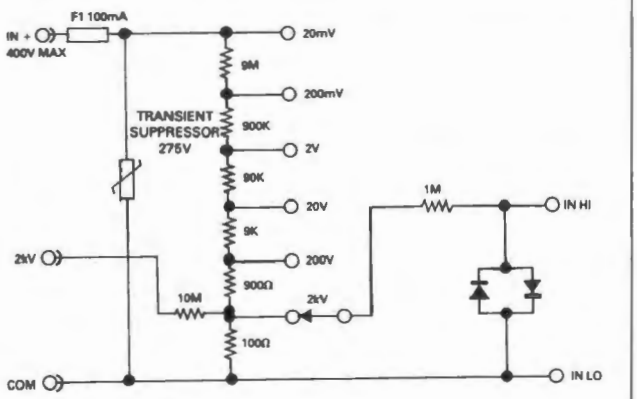
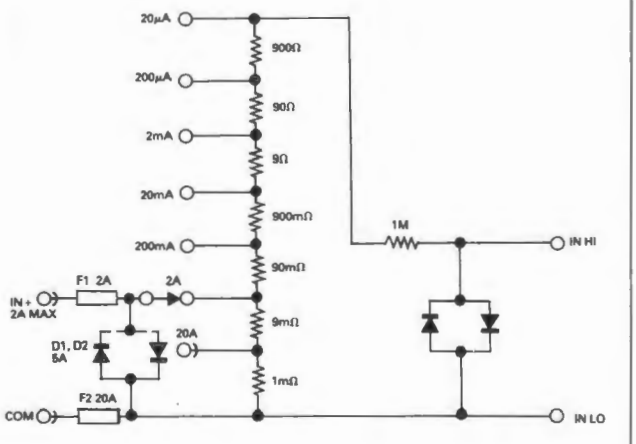


Figure 17 **Universal shunt**

For the measurement of currents from 20μA to 20A with a full-scale voltage drop of ± 20mV.



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RS data

Analogue multiplier RS1495

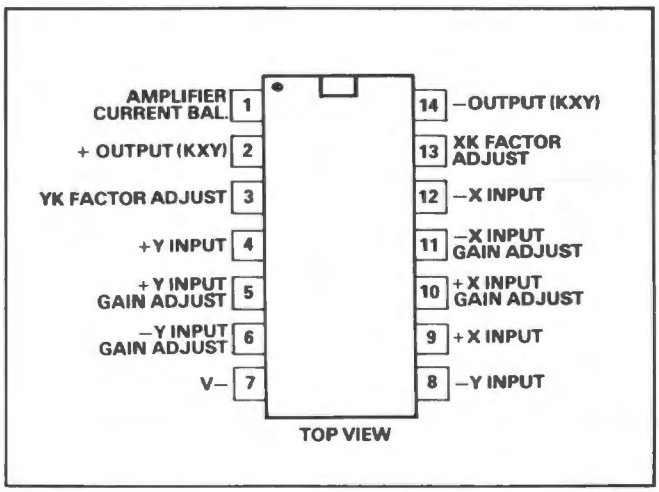
Stock No. 301-690

The RS1495 is a general purpose four quadrant analogue multiplier for use where the output voltage is a linear function of two input voltages. Any control or instrumentation problem which requires the product, square, square root or ratio of two analogue quantities can easily be achieved with the RS1495. Monitoring power, brake horse power, fluid flow, solving of complex non-linear equations (using analogue computer techniques), frequency doubling, phase detection, dynamic gain control, taking roots or powers, modulation circuits, navigational problems, velocity, acceleration and distance for linear or non-linear inputs, root mean square calculations and generation of trigonometric functions are only a few of the applications for this device.

A precision analogue multiplier is also available (Stock No. 302-154). For details see data sheet 4838.

Features

- Good linearity
- Adjustable scale factor
- Wide bandwidth
- High input voltage range
- Wide supply voltage operation



Absolute maximum ratings

Supply voltage ± 15V
Internal power dissipation 750mW
Input voltages X_1, X_2, Y_1, Y_2, Z_1, Z_2 ±Vs
Rated operating temperature range 0 to +70°C
Storage temperature range −65°C to +150°C

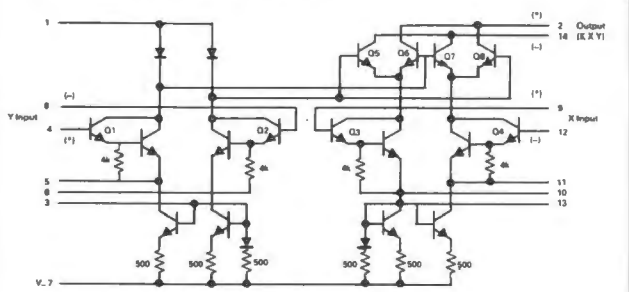
Electrical characteristics

$T_A = +25°C$, $V^+ = +32V$, $V^- = -15V$, $I_3 = I_{13} = 1mA$, $R_X = R_Y = 15k\Omega$, $R_L = 11k\Omega$ unless otherwise specified

Parameter	Conditions	Min.	Typ.	Max.	Units
Linearity: Output error in percentage of full scale	$-10<V_X<+10$ ($V_Y = \pm 10V$) $-10<V_Y<+10$ ($V_X = \pm 10V$)	– –	±1.0 ±2.0	±2.0 ±4.0	% %
Squaring Mode Error: Accuracy in percentage of full scale after offset and scale factor adjustment	$T_A = +25°C$ $T_A = 0$ to $+70°C$	– –	±0.75 ±1.0	– –	% %
Scale Factor (adjustable)	$K = \frac{2R_L}{I_3 R_X R_Y}$	–	0.1	–	
Input Resistance	f = 20Hz	–	20	–	MΩ
Differential Output Resistance	f = 20Hz	–	300	–	kΩ
Input Bias Current	$I_{bx} = \frac{(I_9 + I_{12})}{2}$ $I_{by} \frac{(I_4 - I_8)}{2}$	–	2.0	12	μA
Average Temperature Co-efficient of Input Offset Current	$T_A = 0$ to $+70°C$	–	2.0	–	nA/°C
Input Offset Current	$I_{14} - I_{12}$	–	–	2.0	μA

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Response	3.0 dB Bandwidth, $R_L = 11k\Omega$	–	3.0	–	MHz
	3° Relative phase shift between V_X and V_Y	–	750	–	kHz
	1% Absolute error due to input-output phase shift	–	30	–	kHz
Maximum Factor Adjust Current		–	–	10	mA
Common Mode Gain	(Either input)	–40	–50	–	dB
Common Mode Quiescent Voltage		–	21	–	V_{dc}
Common Mode Output Voltage		–	21	–	V_{dc}
Differential Output Voltage Swing Capability		–	±14	–	V_{peak}
Power Supply Sensitivity	S_+	–	5.0	–	mV/V
	S_-	–	10	–	mV/V
Power Supply Current		–	6.0	7.0	mA
D.C Power Dissipation		–	135	170	mW

Figure 1 **Circuit schematic**



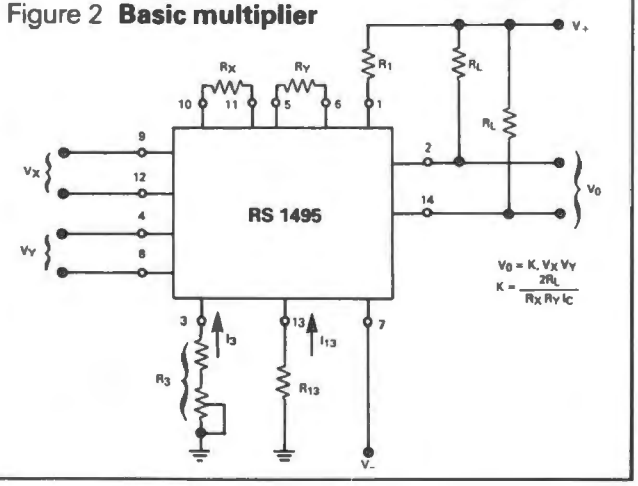
Theory of operation

The RS1495 is a monolithic, four quadrant analogue multiplier which operates on the principle of variable transconductance. Hence the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_3}$$

where I_A and I_B are the currents into pins 14 and 2 respectively and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

Figure 2 **Basic multiplier**



Design considerations

General

The RS1495 permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

Linearity output error

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in per cent of full scale.

One source of linearity error can arise from large signal non-linearity in the X and Y input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that non-linear base-emitter voltage variation can be ignored. Figures 3 and 4 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0mA$).

Figure 3 **Error contributed by input differential amplifier**

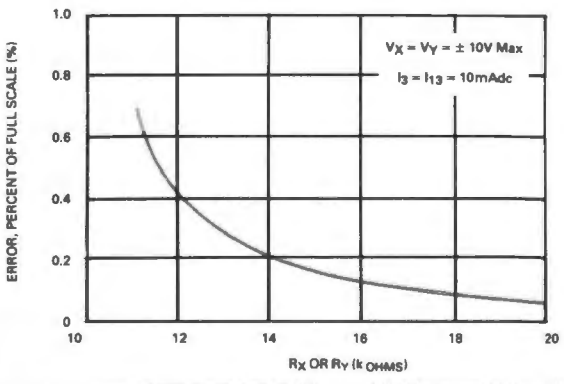
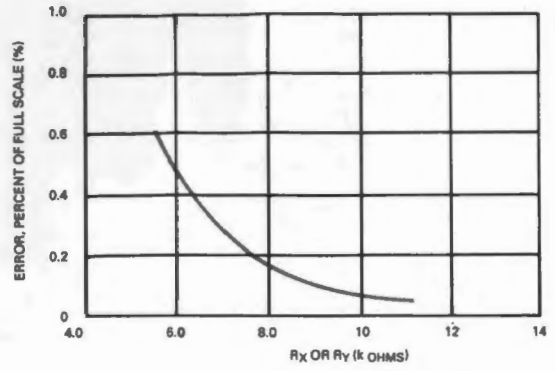


Figure 4 **Error contributed by input differential amplifier**



3 dB-Bandwidth and phase shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and /or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources; phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector of 5%.

Maximum input voltage

$V_{X(max)}$, $V_{Y(max)}$ maximum input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$
$$V_{Y(max)} < I_{13} R_Y.$$

Exceeding this value will drive one side of the input amplifier to 'cutoff' and cause non-linear operation.

Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5mA and 2.0mA, approximately 1.0mA. Then R_X and R_Y can be determined by considering the input signal handling requirement.

For $V_{X(max)} = V_{Y(max)} = 10$ volts:

$$R_X = R_Y > \frac{10V}{1.0mA} = 10k\Omega.$$

The equation $I_A - I_B = \frac{2V_X V_Y}{R_X R_Y I_3}$

is derived from $I_A - I_B = \frac{2V_X V_Y}{(R_X + \frac{2kT}{qI_{13}})(R_Y + \frac{2kT}{qI_3}) I_3}$

with the assumption $R_X > \frac{2kT}{qI_{13}}$ and $R_Y > \frac{2kT}{qI_3}$.

At $T_A = +25°C$ and $I_{13} = I_3 = 1mA$.

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\Omega$$

Therefore, with $R_X = R_Y = 10k\Omega$ the above assumption is valid. Reference to Figure 5 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or 'cutoff' of the input transistors, see Figure 5.

Maximum output voltage swing

The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 2 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7, and Q_8. This potential should be related so that negative swing at pins 2 or 14 does not saturate those transistors. See General design procedure for further information regarding selection of these potentials.

If an operational amplifier is used for level shift, as shown in Figure 6, the output swing of the multiplier is greatly reduced.

Figure 5 **Maximum allowable input voltage versus voltage at pin 1 or pin 7**

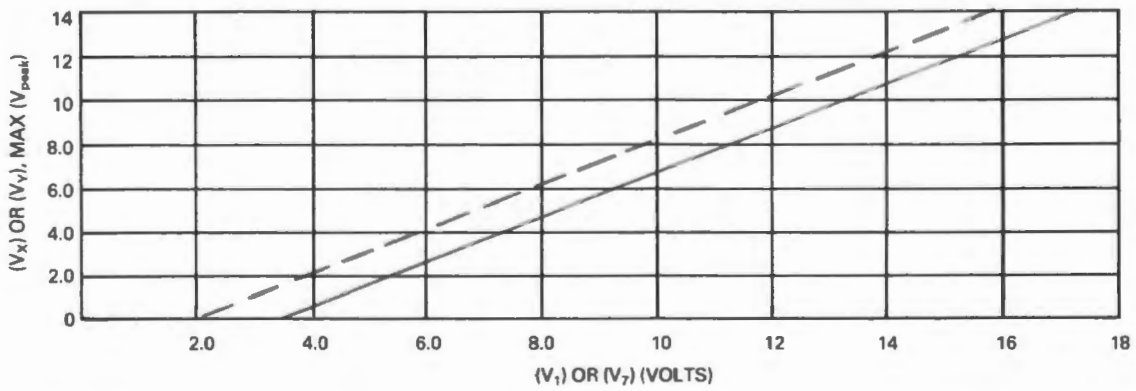
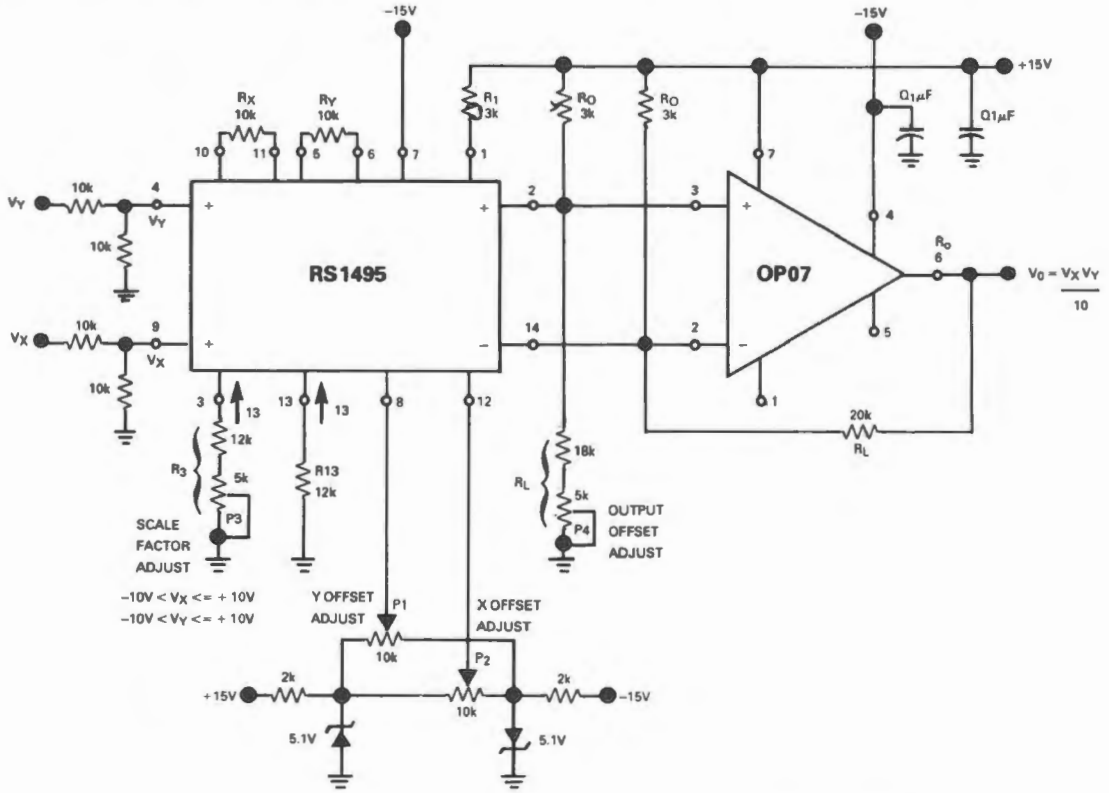


Figure 6 **Multiplier with op-ampl. level shift**



General design procedure

Selection of component values is best demonstrated by the following example: assume resistive dividers are used at the X and Y inputs to limit the maximum multiplier input to ±5.0 volts ($V_X' = V_Y'_{[max]}$) for a ± 10 volt input ($V_X = V_{Y\,[max]}$). (See Figure 6.) If an overall scale factor of 1/10 is desired, then

$$V_O = \frac{V_X' V_Y'}{10} = \frac{(2V_X)(2V_Y)}{10} = 4/10\, V_X V_Y.$$

Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The first step is to select current I_3 and current I_{13}. Selection of these currents may be limited by the dissipation of the device and must not exceed 10mA. I_3 and I_{13} will normally be one or two milliamperes. Further I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1\text{mA}.$$

To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between pin 13 and ground, and between pin 3 and ground. From the schematic shown in Figure 1 it can be seen that the resistor values necessary are given by:

$$R_{13} + 500\Omega = \frac{[V^-] - 0.7V}{I_{13}}$$

$$R_3 + 500\Omega = \frac{[V^-] - 0.7V}{I_3}$$

Let $V^- = -15V$

Then $R_{13} + 500 = \frac{14.3V}{1\text{mA}}$ or $R_{13} = 13.8\text{k}\Omega$

Let $R_{13} = 12\text{k}\Omega$

Similarly, $R_3 = 13.8\text{k}\Omega$

Let $R_3 = 15\text{k}\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 6 resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the simplest resistor would have a value of one-half the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To ensure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \qquad \frac{V_Y}{R_Y} < I_3$$

A good rule of thumb is to make $I_3 R_Y \geq 1.5\, V_{Y(max)}$ and $I_{13} R_X \geq 1.5\, V_{X(max)}$.

The larger the $I_3 R_Y$ and $I_{13} R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 3 and 4).

Let $R_X = R_Y = 10\text{k}\Omega$

Then $I_3 R_Y = 10V$

$I_{13} R_X = 10V$

since $V_{X(max)} = V_{Y(max)} = 5.0$ volts the value of $R_X = R_Y = 10\text{k}\Omega$ is sufficient.

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_X R_Y I_3} = \frac{4}{10}$$

$$\text{or } \frac{(2)(R_L)}{(10\text{k})(10\text{k})(1\text{mA})} = \frac{4}{10}$$

Thus $R_L = 20\text{k}\Omega$.

Step 4. To determine what power-supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 1. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_X' = V_Y' = 10V$ or $V_X = 5.0V$, $V_Y = 5.0V$), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 are at a potential which is two diode-drops below the voltage at pin 1. Thus, the voltage at pin 1 should be about two volts higher than the maximum input voltage. Therefore, to handle +5.0 volts at the inputs, the voltage at pin 1 must be at least + 7.0 volts. Let $V_1 = 9.0$ Vdc.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, R_1 from pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

$$\text{Let } V^+ = +15V$$

$$\text{Then } R_1 = \frac{15V - 9V}{(2)\,(1mA)}$$

$$R_1 = 3k\Omega.$$

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode-drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

Step 5. Level Shifting.
For dc applications, such as the multiply, diode and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 7 performs this function. It can be shown that the output voltage of this circuit is given by:

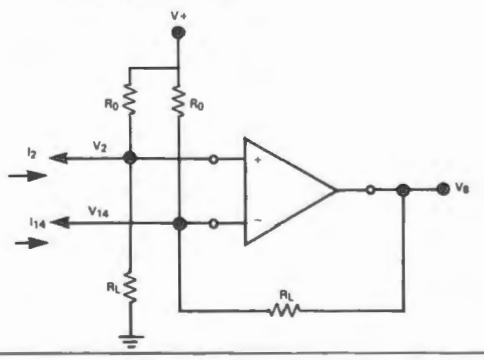
$$V_O = (I_2 - I_{14})\,R_L$$

$$\text{And since } I_A - I_B = I_2 - I_{14} = \frac{2I_X I_Y}{I_3} = \frac{2\,V_X\,V_Y}{I_3 R_X R_Y}$$

$$\text{Then } V_O = \frac{2R_L V_X' V_Y'}{4R_X R_X I_3}$$

where $V_X'V_Y'$ is the voltage at the input to the voltage dividers.

Figure 7 **Level Shift Circuit**



The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common-mode input voltage range as well as a high common-mode rejection ratio. The OP07 operational amplifier meet these requirements.

Referring to Figure 6, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 volts. From this information, R_O can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V_2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_O}$$

$$\text{And for this example, } \frac{11V}{20k\Omega} = 1mA = \frac{15V - 11V}{R_O}$$

Solving for R_O, $R_O = 2.6k\Omega$

Thus, select $R_O = 3.0k\Omega$

For $R_O = 3.0k\Omega$, the voltage at pins 2 and 14 is calculated to be:

$$V_2 = V_{14} = 10.4 \text{ volts.}$$

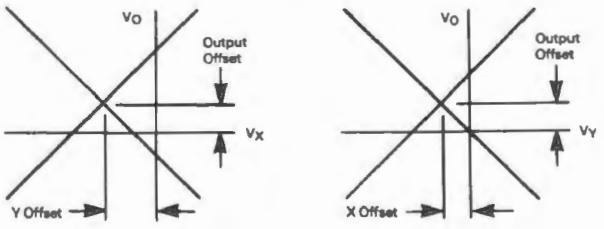
Offset and scale factor adjustment

Offset voltages
Within the monolithic multiplier (Figure 1) transistor base-emitter junctions are typically matched within 1mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error comprises X-input offset voltage, Y-input offset voltage, and output-offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 6. Offset terms can be shown analytically by the transfer function.

$$V_O = K(V_X \pm V_{IOX} \pm V_X \text{ off})\,(V_Y \pm V_{IOY} \pm V_Y \text{ off}) \pm V_{OO}$$

Where K = scale factor
V_X = X input voltage
V_Y = Y input voltage
V_{IOX} = X input offset voltage
V_{IOY} = Y input offset voltage
$V_{X\,off}$ = X input offset adjust voltage
$V_{Y\,off}$ = Y input offset adjust voltage
V_{OO} = output offset voltage

X, Y and Output Offset Voltages



For most dc applications, all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications.

RS data

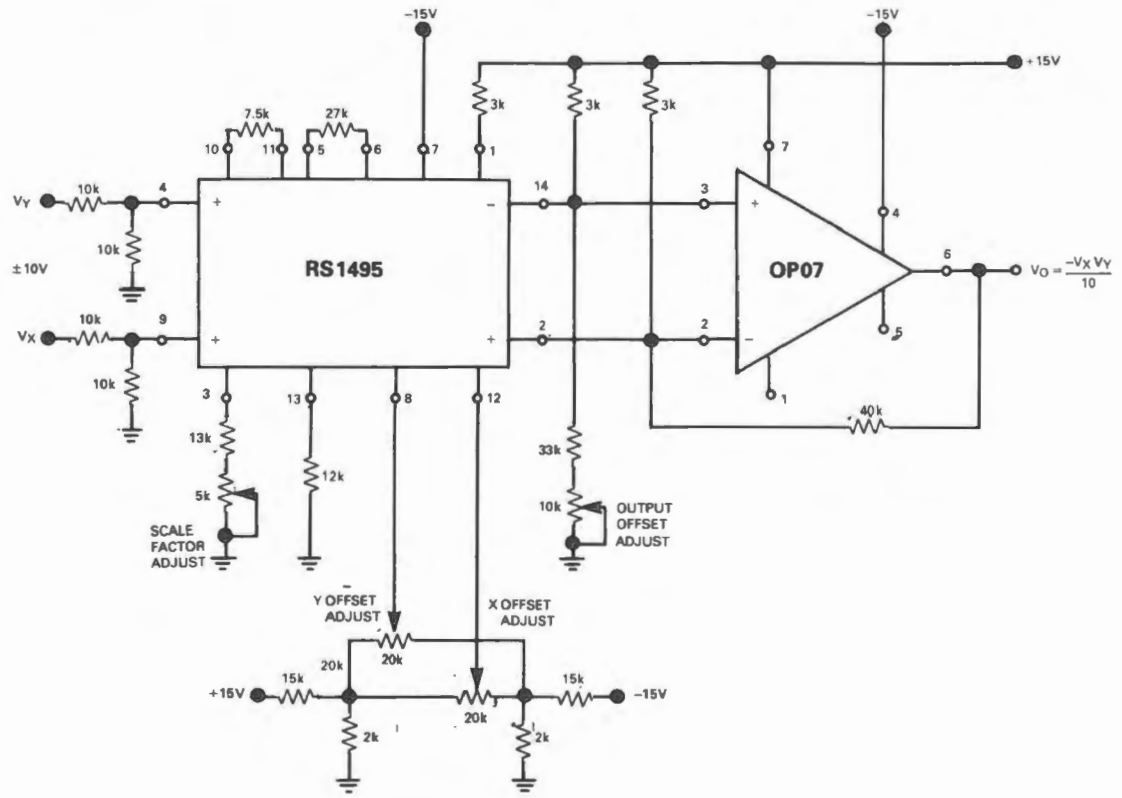
Scale factor
The scale factor, K, is set by P_3 (Figure 6). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (see Figure 1). Therefore, to ensure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see General design procedure).

Adjustment procedures
The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 6.)

1. X Input Offset
   (a) Connect oscillator (1kHz, 5 V_{pp} sinewave) to the 'Y' input (pin 4).
   (b) Connect 'X' input (pin 9) to ground.
   (c) Adjust X offset potentiometer, P_2, for an ac null at the output.
2. Y Input Offset
   (a) Connect oscillator (1kHz, 5 V_{pp} sinewave) to the 'X' input (pin 9)
   (b) Connect 'Y' input (pin 4) to ground.
   (c) Adjust 'Y' offset potentiometer. P_1, for an ac null at the output.
3. Output Offset
   (a) Connect both 'X' and 'Y' inputs to ground
   (b) Adjust output offset potentiometer, P_4, until the output voltage V_O is zero volts dc.
4. Scale Factor
   (a) Apply +10 V_{dc} to both the 'X' and 'Y' inputs
   (b) Adjust P_3 to achieve +10.00V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the RS1495 depends upon the characteristics of potentiometers P_1 through P_4. Multi-turn, infinite resolution potentiometers with low-temperature coefficients are recommended.

Figure 8 **Multiplier with improved linearity**



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RS data

CMOS Compatible logic gate optoisolator

Stock number 301-741

The 301-741 is an optically coupled logic gate that combines a GaAsP LED and an integrated high gain photon detector. The detector has a three state output stage and has a detector threshold with hysteresis. The three state output eliminates the need for a pullup resistor and allows for direct drive of data busses. The hysteresis provides typically 0.1 mA of differential mode noise immunity and eliminates the potential for output signal chatter. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of 1,000 volts/μsec, equivalent to rejecting a 300 volt sinusoid at 1 MHz. Improved power supply rejection eliminates the need for special power supply bypassing precautions.

The electrical and switching characteristics of the 301-741 are guaranteed over the temperature range of 0°C to 85°C. The 301-741 is guaranteed to operate over a V_{CC} range of 4.5 volts to 20 volts. Low I_F and wide V_{CC} ranges allow compatibility with TTL, LSTTL, and CMOS logic. Low I_F and low I_{CC} result in lower power consumption compared to other high speed optocouplers. Logic signals are transmitted with a typical propagation delay of 160 nsec when a 120 pF peaking capacitor is used in parallel with the 1.1kΩ current limiting resistor.

The 301-741 is useful for isolating high speed logic interfaces, buffering of input and output lines and implementing isolated line receivers in high noise environments.

Absolute maximum ratings

(No derating required up to 70°C)

Storage temperature ——— –55°C to +125°C
Operating temperature ——— –40°C to +85°C[1]
Lead solder temperature ——— 260°C for 10s (1.6mm below seating plane)
Average forward input current — I_F ——— 10mA
Peak transient input current — I_F ——— 1A (≤1 μs pulse width, 300pps)
Reverse input voltage ——— 5V
Supply voltage — V_{CC} ——— 0.0V min., 20V max.
Three state enable voltage — V_E ——— –0.5V min., 20V max.
Output voltage — V_O ——— –0.5V min., 20V max.
Total package power dissipation — P ——— 210mW[1]
Average output current — I_O ——— 25mA

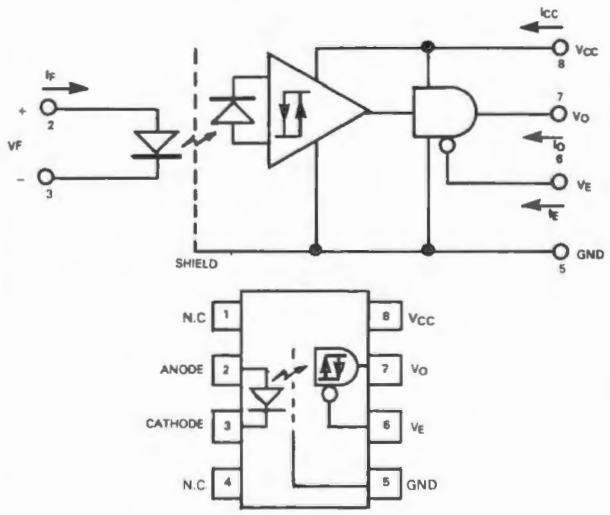
[1]. Derate total package power dissipation, P, linearly above 70°C free air temperature at a rate of 4.5mW/°C.

Features

- Compatible with LSTTL, TTL and CMOS logic
- 2.5 MBAUD guaranteed over temperature
- Low input current (1.6mA)
- Wide V_{CC} range (4.5 to 20 Volts)
- Three state output (no pullup resistor required)
- Guaranteed performance from 0°C to +85°C
- Internal shield for high common mode rejection

Applications

- Isolation of high speed logic systems
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Ground loop elimination
- Pulse transformer replacement
- Isolated buss driver
- High speed line receiver



TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	Z
L	H	Z
H	L	H
L	L	L

Electrical characteristics For $0°C \leq T_A$ [1] $\leq 85°C$, $4.5V \leq V_{CC} \leq 20V$, $1.6mA \leq I_{F(ON)} \leq 5mA$, $0.0mA \leq I_{F(OFF)} \leq 0.1mA$. All typicals at $T_A = 25°C$, $V_{CC} = 5V$, $I_{F(ON)} = 3mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4mA (4 TTL Loads)	1	
Logic High Output Voltage	V_{OH}	2.4			Volts	I_{OH} = −2.6mA	2	
Output Leakage Current ($V_{OUT} > V_{CC}$)	I_{OHH}			100	μA	V_O = 5.5V; I_F = 5mA		
				500	μA	V_O = 20V; V_{CC} = 4.5V		
Logic High Enable Voltage	V_{EH}	2.0			Volts			
Logic Low Enable Voltage	V_{EL}			0.8	Volts			
Logic High Enable Current	I_{EH}			20	μA	V_{EN} = 2.7V		
				100	μA	V_{EN} = 5.5V		
			.004	250	μA	V_{EN} = 20V		
Logic Low Enable Current	I_{EL}			−0.32	mA	V_{EN} = 0.4V		
Logic Low Supply Current	I_{CCL}		4.5	6.0	mA	V_{CC} = 5.5V; I_F = 0mA		
			5.25	7.5	mA	V_{CC} = 20V; V_E = Don't Care		
Logic High Supply Current	I_{CCH}		2.7	4.5	mA	V_{CC} = 5.5V; I_F = 5mA,		
			3.1	6.0	mA	V_{CC} = 20V; V_E = Don't Care		
High Impedance State Output Current	I_{OZL}			−20	μA	V_O = 0.4V; V_{EN}=2V, I_F=5mA		
	I_{OZH}			20	μA	V_O = 2.4V; V_{EN} = 2V, I_F = 0		
				100	μA	V_O = 5.5V		
				500	μA	V_O = 20V		
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	$V_O = V_{CC}$ = 5.5V; I_F = 0mA		2
		40			mA	$V_O = V_{CC}$ = 20V		
Logic High Short Circuit Output Current	I_{OSH}	−10			mA	V_{CC} = 5.5V; I_F = 5mA, V_O = GND		2
		−25			mA	V_{CC} = 20V		
Input Current Hysteresis	I_{HYS}		0.12		mA	V_{CC} = 5V	3	
Input Forward Voltage	V_F		1.5	1.70	Volts	I_F = 5mA, T_A = 25°C		
Input Reverse Breakdown Voltage	V_R	5			Volts	I_R = 10 μA at T_A = 25°C		
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		−1.7		mV/°C	I_F = 5mA		
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	V_{I-O} = 3000 VDC, T_A = 25°C, t = 5s, Relative Humidity = 45%		3
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC		3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1MHz, V_{I-O} = 0 VDC		3
Input Capacitance	C_{IN}		90		pF	F= 1MHz, V_F = 0V, Pins 2 and 3		

Notes: 2. Duration of output short circuit time should not exceed 10ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Switching characteristics For $0°C \leq T_A$ [1] $\leq 85°C$, $4.5V \leq V_{CC} \leq 20V$, $1.6mA \leq I_{F(ON)} \leq 5mA$, $0.0mA \leq I_{F(OFF)} \leq 0.1mA$. All typicals at $T_A = 25°C$, $V_{CC} = 5V$, $I_{F(ON)} = 3mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		210		ns	Without Peaking Capacitor	4.5	4.5
			160	400		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		170		ns	Without Peaking Capacitor	4.5	4.5
			115	400		With Peaking Capacitor		
Output Enable Time to Logic High	t_{PZH}		25		ns		7.9	
Output Enable Time to Logic Low	t_{PZL}		28		ns		7.8	
Output Disable Time from Logic High	t_{PHZ}		105		ns		7.9	
Output Disable Time from Logic Low	t_{PLZ}		60		ns		7.8	

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Output Rise Time (10-90%)	t_r		55		ns		4.6	
Output Fall Time (90-10%)	t_f		15		ns		4.6	
Logic High Common Mode Transient Immunity	CM_H	-1000	-10,000		V/μs	$T_A = 25°C$, $I_F = 1.6mA$		6
Logic Low Common Mode Transient Immunity	CM_L	1000	10,000		V/μs	$T_A = 25°C$, $I_F = 0$		6

Notes:

4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the output pulse.
5. When the peaking capacitor is omitted, propagation delay times may increase by 100ns.
6. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8V$). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0V$).

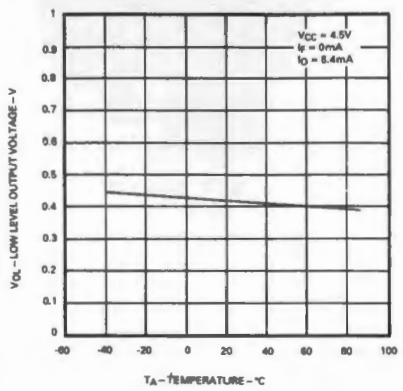


Figure 1 **Typical Logic Low Output Voltage vs. Temperature**

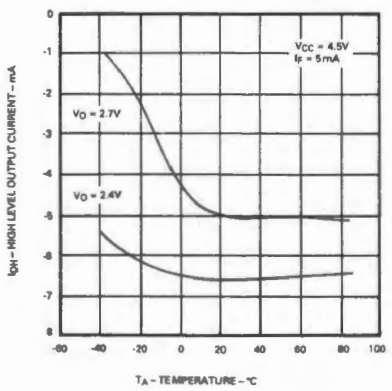


Figure 2 **Typical Logic High Output Current vs. Temperature**

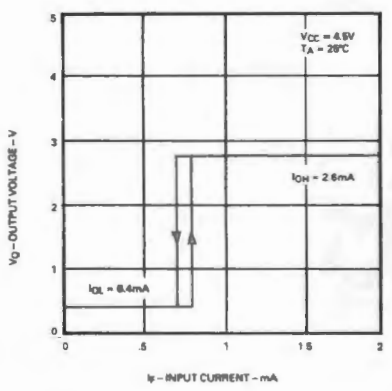


Figure 3 **Output Voltage vs. Forward Input Current**

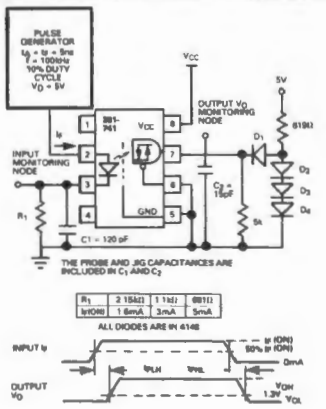


Figure 4 **Test Circuit for t_{PLH}, t_{PHL}, t_p and t_f**

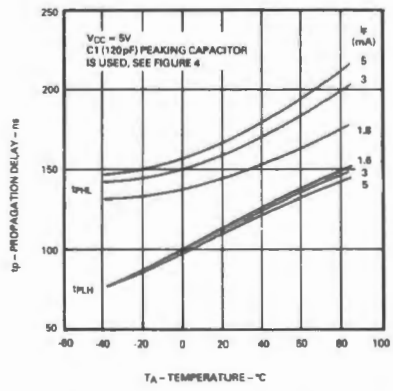


Figure 5 **Typical Propagation Delays vs. Temperature**

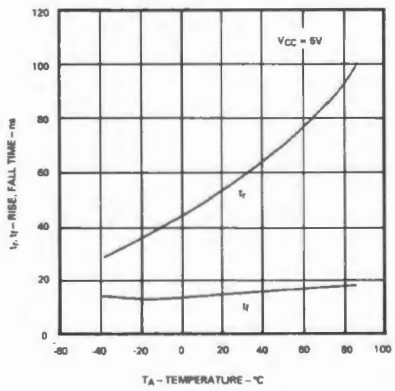


Figure 6 **Typical Rise, Fall Time vs. Temperature**

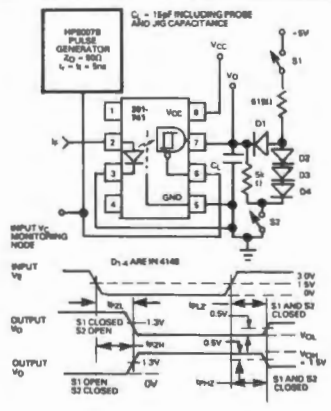


Figure 7 **Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}**

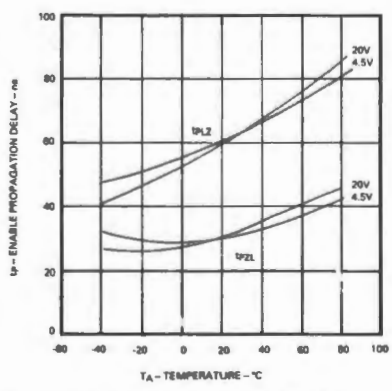


Figure 8 **Typical Logic Low Enable Propagation Delay vs. Temperature**

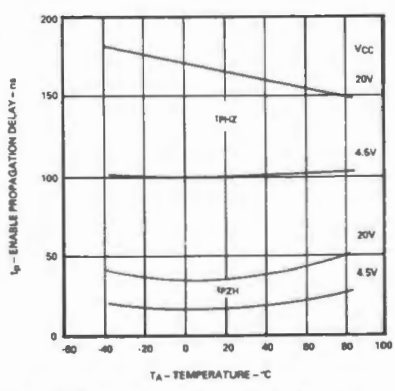
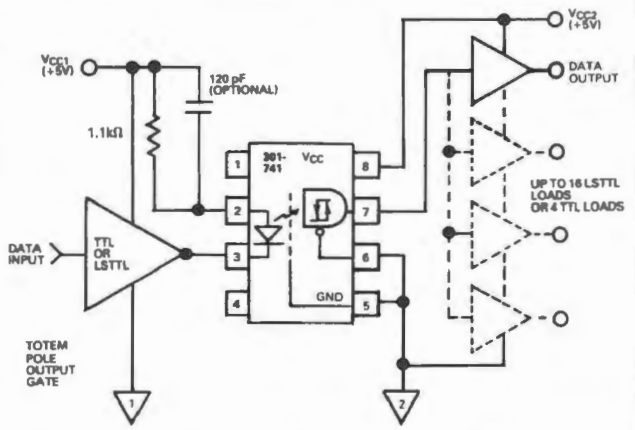


Figure 9 **Typical Logic High Enable Propagation Delay vs. Temperature**

RS data

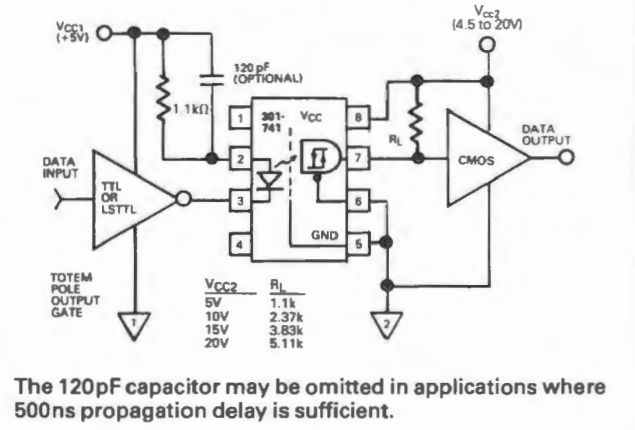
Recommended circuit design

Figure 10 **Recommended LSTTL to LSTTL Circuit**



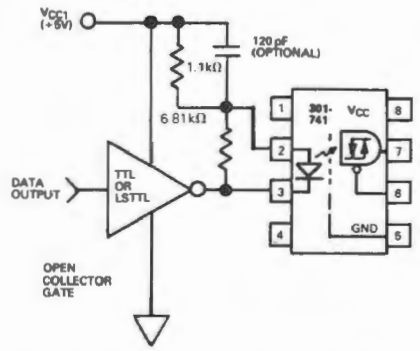
The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.

Figure 11 **LSTTL to CMOS Circuit**



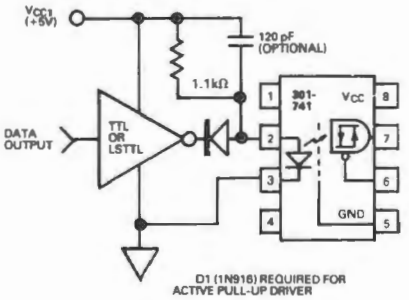
The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.

Figure 12 **Series LED Drive with Open Collector Gate (6.81kΩ Resistor Shunts I_{OH} from the LED)**



The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.

Figure 13 **Alternative LED Drive Circuit**



The 120pF capacitor may be omitted in applications where 500ns propagation delay is sufficient.

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RS data

Ultra-violet exposure system

A range of three ultra-violet exposure units for use in the preparation of RS photo-resist printed circuit boards and RS photo-sensitive imaging film.

Use of U-V exposure units

Note: The exposure unit lid should be closed before switching on.

(i) Stock No. 555-279, Small U-V unit, area 245 x 150mm.

Switch on the unit for the required time. Switch off before opening unit lid. Note that the warning light is illuminated while the mains supply is connected.

(ii) Stock nos. 556-238, Medium (245 x 255mm) and 559-934 Large (508 x 356mm) U-V units (with timer).

Switch on the mains supply to the unit. The amber mains warning light should illuminate. Rotate the timer control knob to the required time setting. To commence the timed exposure, press the U-V button once. The green indicator will illuminate to show that the tubes are energised and the timed period has commenced. After the preset time the tubes will be de-energised and the green indicator extinguished. The lid should not be opened until the timed period has been completed. Avoid altering the time setting or operating the U-V button during the timed period. However, if it is required to terminate the exposure before the end of the timed period, this may be achieved by switching off the mains. It should, however, be noted that the timed period cannot be completed by switching the mains back on; to do this it will be necessary to set the timer for the remaining time required and restart the exposure using the U-V button.

Warning

Whilst the ultra-violet light emitted is not dangerous, some eye discomfort may be experienced if the tubes are viewed directly particularly with the 40W tubes used on the large U-V unit.

Photo-resist printed circuit boards

1 Prepare artwork using RS drafting film. The 0.1in grid sheet may be used to align the layout to a 0.1in pitch. RS Etch Resist PCB Transfers are suitable for providing track and pad areas.

The photo-resist is positive, hence transfers on the polyester drafting film will represent copper left on the board after etching. For critical resolution with fine tracks the transfers should be placed on the underside of the film so as to be in contact with the copper surface. If this latter method is adopted a 'mirror-image' of the required artwork must be prepared.

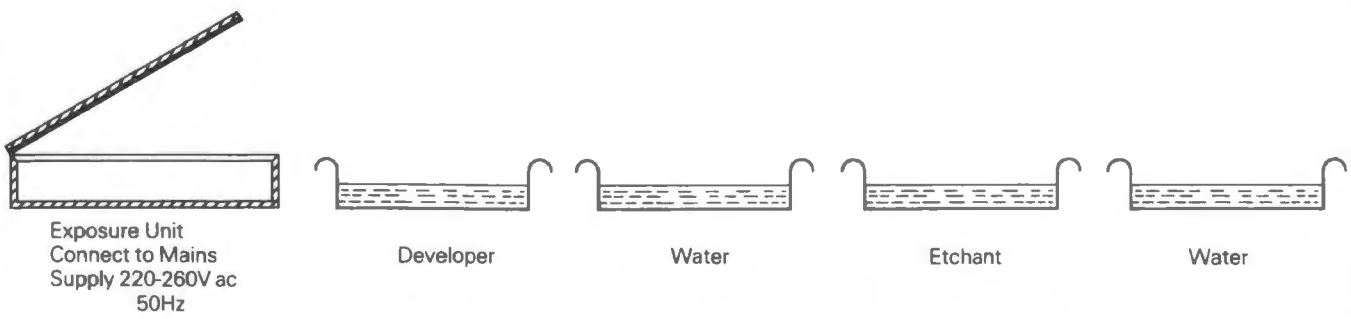
2 **Developer:** Make up a solution of sodium hydroxide* using 15-25 grams to 1 litre of cold water; this amount is sufficient to develop approximately 0.4m^2 of circuit board. **N.B.** Never store made-up solution, always use a fresh solution.

Etchant: Use ferric chloride hexahydrate crystals* dissolved in water in the proportion of 500 grams ferric chloride to 1 litre of water.

Place both these solutions in RS plastic trays together with two trays containing water as depicted in figure 1, alternatively the RS PCB Modular Preparation System may be used.

3 Peel off the black plastic protective film from the Photo Resist Board. It is not necessary to work in a safelight area but unprotected boards should not be exposed to sunlight or bright lights unnecessarily or left uncovered prior to development for periods greater than ten minutes.

Figure 1



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Open the exposure unit and place the artwork on the glass plate, checking for correct side up. Take the Photo Resist Board and position onto the artwork, resist side down, and close the lid. Expose the board in accordance with the above instruction. The recommended exposure time for Photo Resist Boards is as follows) 8-10 minutes for the small unit 555-279, 6-8 minutes for the medium unit 556-238 and 2-3 minutes for the large unit 559-934 but this may be varied to produce optimum results. It should be noted that diffusion occurs at the edge of artwork reducing the edge definition; this effect is accentuated with longer exposure times and narrower PCB tracks. It is, therefore, advantageous to experiment with exposure times to determine the optimum for the particular application and type of board in use.

4 Remove board from exposure unit and place in the developer solution for ½ to 1½ minutes. Development time depends on the temperature of the solution which should be between 18°C and 27°C. Do not exceed 27°C. Agitate solution by gently rocking the tray. (If using the RS heated process tank agitation is not necessary.) Once every 30 seconds is sufficient. The period for which the exposed board is left in the developing solution should be kept to the minimum necessary for removal of the unwanted resist. To this end it is permissible to brush the board (whist in the solution) with a *soft* brush.

When using the double side Photo Resist Board ensure that support is provided to enable developer to reach both sides equally.

5 Wash board in water to remove developer. If running water is available a 15 second rinse is sufficient. 'Forced' washing is not necessary. When trays are used for washing, the water should be changed after every few boards to ensure no undue contamination of the etchant and hence prolong etchant life. After this washing the desired track layout should be discernible. If there are traces of resist on unwanted areas, re-immerse board in developer for 20 seconds, then remove and wash.

6 Place board into the etchant until unwanted copper is removed. This may take 20 minutes or more (less time is required when using the RS bubble etch tank), depending on the strength of the solution and the area of copper to be removed. Etching will be aided by increasing the temperature of the solution and rocking the tray. Support double sided boards so that both sides are equally exposed to the etchant.

7 Wash board in water to remove etchant.

8 When board is dry it is ready for use. The photo resist left on the copper areas may be removed using RS PCB Solvent Cleaner 555-134 or one can solder directly through the photo resist which is 'self-fluxing'.

* Sodium hydroxide (caustic soda) 99% pearl W/W and ferric chloride hexahydrate crystals are available from most chemical suppliers and some chemists.

WARNING:
The developer and etchant are both highly corrosive. Care should be exercised during their preparation, storage and use.

Photo-sensitive imaging film

For preparation of artwork and recommended exposure times for the RS photo imaging system, refer to the instructions packed with the photo imaging film.

Open the exposure unit and place the artwork on the glass plate, checking carefully that the appropriate face is presented upwards to the photo-sensitive film according to whether the object is to produce a positive or negative final image. Position the photo-sensitive film emulsion (matt) side downwards over the artwork and close the exposure unit lid. For the recommended exposure time and details of development refer to the instructions supplied with the photo-imaging film. Expose the film in accordance with the above instructions for U-V units.

Note: servicing kits comprising two tubes and two starters are available.

For exposure units 555-279 and 556-238 use service set 556-250.

For exposure unit 559-934 use service set 559-990.

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Photo-imaging system

The RS photo-imaging system provides a simple, rapid means of self-adhesive label manufacture. Finished labels feature very high contrast images, wide ambient temperature ranges and have excellent wear and scratch resistance as the photosensitive material (and therefore final image) is beneath the surface of the film.

The RS photo-imaging system has three components: (a) photosensitive film, (b) self-adhesive laminating film, (c) developer. The photosensitive film is polyester non-silver negative working material which produces a clear image against a black blackground when exposed to ultra-violet light through suitable master artwork. After exposure the film is developed with RS aerosol foam developer (RS Stock No. 556-610).

The laminating film consists of sheets of polyester material, both sides of which are coated with pressure sensitive clear acrylic adhesive.

The opaque type is white on one side and green, yellow, blue or red on the other. The clear type is used to affix the label to front panels or other existing surfaces. The pressure sensitive adhesive is protected by white release paper through which the laminate colour is visible.

Artwork

This should be made from suitable UV opaque materials (eg. RS panelprint, etch resist transfers) on transparent film (such as RS drafting film).

Good contact must be maintained between artwork and photosensitive film. The actual print characters should be in contact with the sensitive (matt) side of the film for best definition, see Figure 1.

When using daylight a contact printing frame as used in photographic work is necessary.

Exposure

Remove the photosensitive film from the envelope (a darkroom is not necessary, but the film should be handled under yellow or subdued light).

The film may be cut using a sharp knife or scissors but care should be taken to handle the film by the edges only, and not to touch the sensitive side which may be identified by its matt finish.

Exposure times are not critical and the table gives a guide both for UV light boxes and daylight. If unsure, err on the side of over exposure.

Photo-imaging film ____ **Stock No. 556-553**
Clear laminate ____ **Stock No. 556-569**
White/Yellow laminate ____ **Stock No. 556-575**
White/Blue laminate ____ **Stock No. 556-581**
White/Green laminate ____ **Stock No. 556-597**
White/Red laminate ____ **Stock No. 556-604**
Aerosol developer ____ **Stock No. 556-610**

For further details of RS Exposure Units see Data Sheet 5235.

UV Source	Time (seconds)
RS U-V Exposure unit 555-279	180-210
RS U-V Exposure unit 556-238	180-210
RS U-V Exposure unit 559-934	120-150
Clear sunlight	60
Hazy sun – strong shadows	120
Hazy sun – weak shadows	180
Overcast – no shadows	240

Development

Development should be performed using RS aerosol developer 556-610. The exposed film should be laid matt side up in a suitable tray (eg. RS 555-572), flooded with foam solution from the aerosol and left for approximately 15 seconds. The film should then be rinsed under cold running water (gentle wiping with a soft brush or tissue will assist) and dried with a soft absorbent material – paper towel roll, etc. If black areas that should have been washed off remain the film may be re-immersed in developer for another 5 seconds, washed and dried as above.

If black areas have been washed away that should have been left on the film, the film was underexposed. In this case a longer exposure will have to be made with a new piece of film.

Note: It is recommended that protective gloves are worn while handling the developing solution to prevent possible skin irritation.

Lamination

To complete the label simply peel off the release paper from the required laminating sheet and carefully roll down the film onto the adhesive surface, avoiding trapping air underneath or producing creases. The image should be adjacent to the adhesive so that it is viewed through the

RS data

thickness of the film, thus rendering the label scratchproof. The release paper may then be peeled off the other side of the laminate sheet and the finished label applied to any smooth, dry, grease-free surface. Several colours on one label may be achieved by colouring the clear areas of a negative reproduction film with felt tip pens or thin coloured self adhesive films before attachment to the white laminating sheet.

Other background colours may be achieved by using the clear laminating sheet and attaching the label to any suitable coloured material.

Finished label specification

Total thickness approx. 0.4mm.

Adhesive strength 0.25kg/cm (180° pull back from aluminium).

Temperature range –40°C to +80°C (note: coloured laminate may change hue after prolonged high temperatures).

The labels are resistant to water, oils and most common chemicals. Label edges should be protected from prolonged contact with some solvents.

Coloured laminate may tend to fade after prolonged UV exposure. Black on white or black on clear labels are recommended for exterior use.

Figure 1 **Negative reproduction**

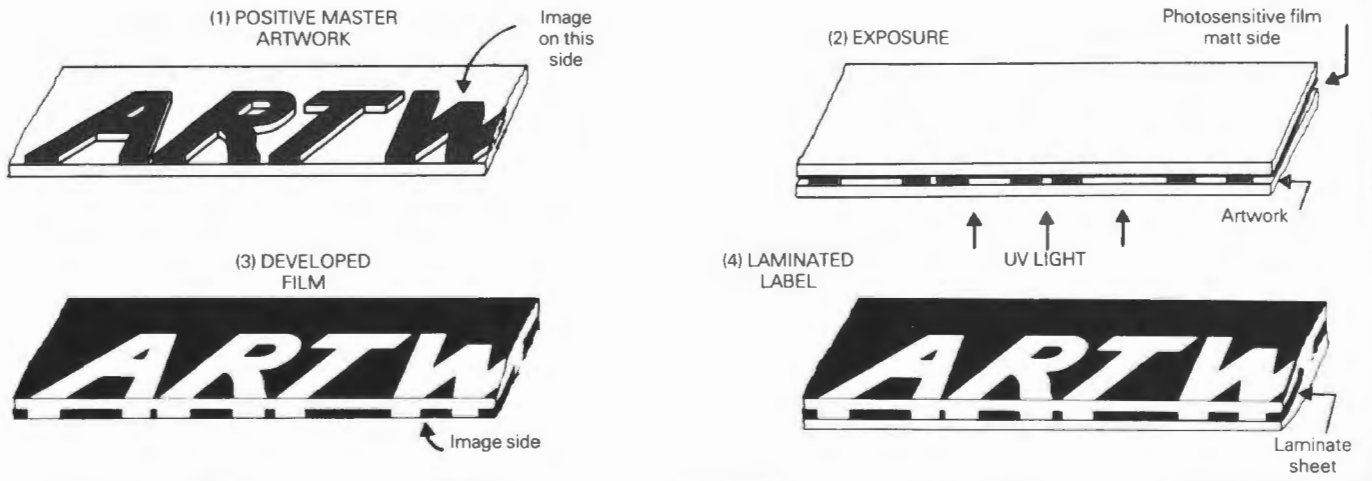
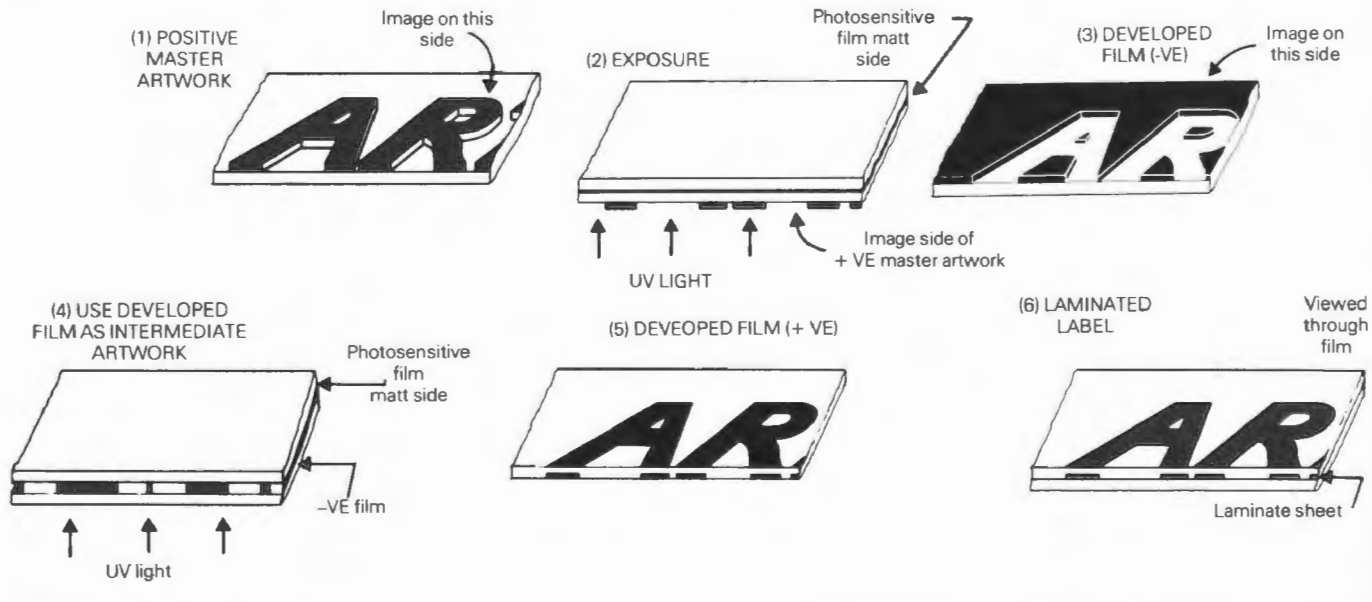


Figure 2 **Positive reproduction**



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Intruder detectors

Stock numbers 302-479, 301-423 and 630-544

Ultrasonic intruder detector (302-479)

The RS ultrasonic intruder detector is a volumetric detection device which utilises the doppler effect whereby a small change in frequency occurs when a low powered ultrasonic signal reflects off a moving target. The unit is intended primarily for use as an intruder detector, either individually in small areas, or in multiples for larger areas without the need for synchronisation. The alarm output is by a non-latching isolated reed relay.

Specification

Frequency — 32.765kHz (crystal controlled)
Linear range — 8 metres approximately
Operating temperature — −10°C to +40°C
Input voltage — 10.5 to 14.5 volts DC
Nominal current — 25mA
Alarm output
A relay contact rated at 200mA 30 volts DC which opens in an alarm condition
Walk test and/or
latch indication: Light emitting diode
Controls: a) Range potentiometer:
Min. setting 2 metres approx.
Max. setting 8 metres approx.
b) 'Detection' slide switch.
1 step and 2 step settings.
Dimensions — 226 x 90 x 52mm
Net weight — 0.4kg
Mounting: Direct on wall or in corners with 2 screws
Colour — White
Complies with BS4737 Part 3 Section 3.5.

Installation

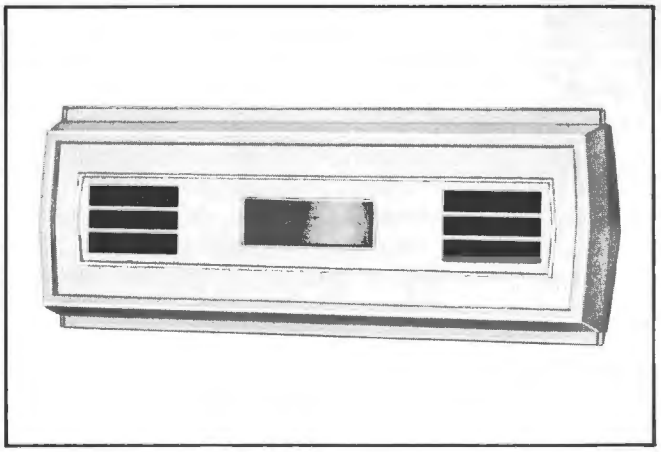
Although knowledge of how the system works is unnecessary, the installer should be familiar with approved wiring techniques and interface connections on this type of equipment.

Hard and soft environments

Ultrasonic energy is strongly reflected from solid objects such as plaster or brick walls, windows, metal filing cabinets etc but only weakly from softer furniture as found in domestic premises. This results in considerable differences in apparent sensitivity between dissimilar environments. Hard environments will in general give greater range, but air turbulence has a greater effect on the operation.

Features

- Adjustable for movement and range
- Low power consumption
- Individual or multiple operation
- LED walk test indication
- Crystal controlled transmitter with RF screening
- Compact styling with simple installation



Choice of position

Successful trouble free operation of a volumetric system depends on correct positioning, firm mounting and sound wiring. The signals transmitted will not penetrate beyond the physical confines of the room in which it is sited, ie there is no penetration through walls, closed doors or windows.

The unit should normally be mounted horizontally just above head height with the extrusion fixed on that face which angles the transducers towards the centre of the area to be protected. The area covered by the unit for a given application can be calculated from the polar diagram (see Figure 2). It is important that the detector is not positioned on the same wall as the entry/exit as the unit cannot give 180° coverage. Care should be taken to move the blind grommet if necessary to the exposed wiring hole (or to pass the cabling through a small hole in it) so as to exclude insects from within the housing. If a lower mounting is required it may be fixed either horizontally or vertically. If mounted vertically the case may be angled slightly to the left or right depending on which face it is fixed.

Individual units should:

a) Face towards or away from the direction of most likely intrusion.
b) Be firmly fixed to a rigid structure.
c) Be remote from sources of ultrasonic sound.
d) Not be accidentally earthed by screwing to foil lined wall board.
e) Have the range control turned as low as convenient.

Experience has shown that point (b) above is frequently misunderstood. If a detector designed to respond to movement of an intruder at extreme range is fixed to a structure which can vibrate, even with low amplitude, it will 'see' apparent movement of the whole of the room including walls, ceiling and floor. The structure must be completely rigid and pelmets, wooden stud partitioning and wall boards are not suitable fixing points.

Parallel operation

Two or more units may be operated in the same environment without either inhibiting or alarming each other. There is no fear of false alarms arising from two or more units 'talking' to each other.

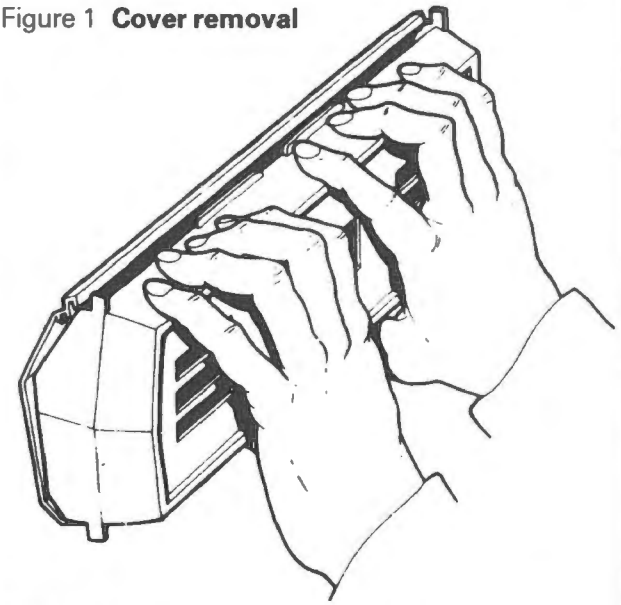
Do not use the RS device with any other type of ultrasonic motion detector, either those operating at about 32kHz or at any other ultrasonic frequency. Mixing ultrasonic systems will almost certainly result in false alarms.

Connections

The device may be connected to any reliable control unit. The terminals are clearly marked on the printed circuit board.

a) The unit should be connected to +12 volts DC supply (a conventional intruder alarm power supply should be used with voltage limits of 10.5 to 14.5 volts with a maximum ripple of 1 volt peak-to-peak and a current capacity of 25mA). The same power supply may be used to drive several devices without fear of mutual interference through the power leads.
b) Both the relay output terminals and the tamper loop circuit are isolated.
c) Remember to connect the case earth lead to −ve.
d) The negative output from the power supply must be earthed. This is essential for the suppression of RF interference.
e) Link the terminals marked W/T if the LED is required to operate when walk-testing.
f) When using the device no connection is made to RST. The unit will reset automatically a few seconds after the movement initiating the alarm has ceased.
g) There is one spare terminal for use with an end of line resistor if required.

Figure 1 **Cover removal**



Open by squeezing opposite sides of plastic housing gently towards each other and disengaging the two lugs on one side.

Range adjustment

Before range adjustments are made the tamper alarm must be muted. The range potentiometer is adjusted with a screwdriver, clockwise rotation of the potentiometer increasing the range. The front cover must be removed to gain access to the potentiometer. Always commence with the range potentiometer at minimum setting. Increase gradually, by walk testing until the desired coverage is obtained. Too high a setting of the range control will exacerbate air turbulence problems.

Detection adjustment

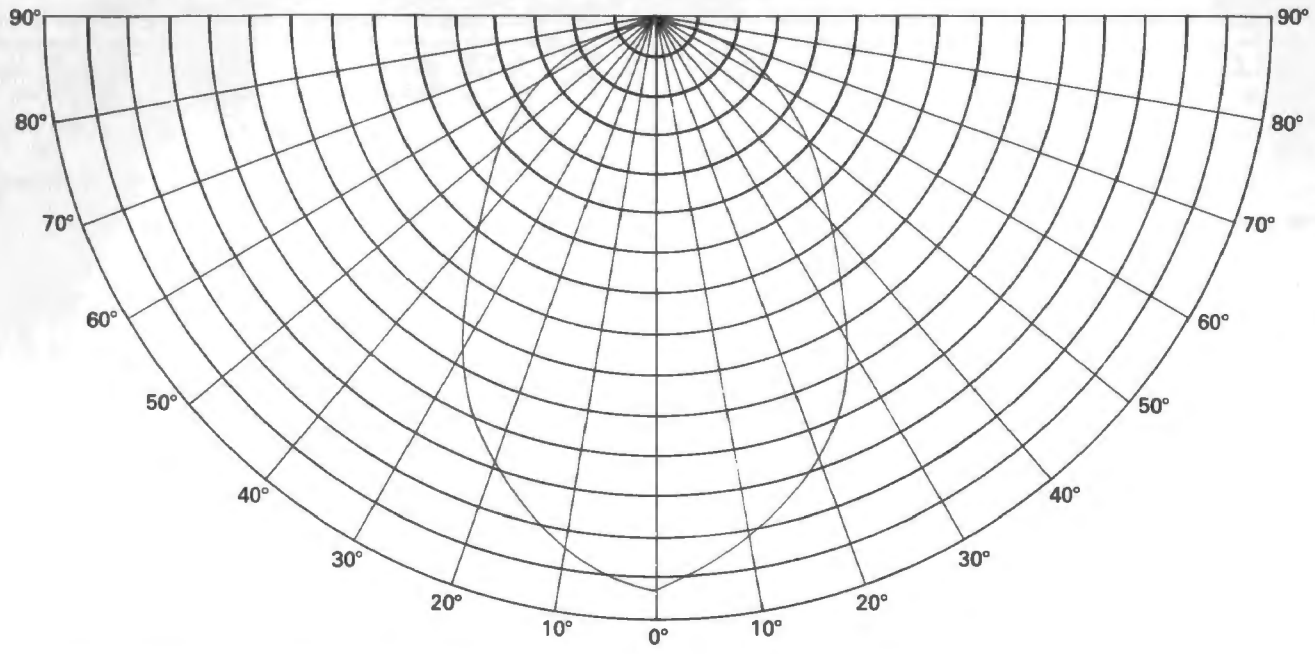
'One Step' setting corresponds to continuous movement slightly over a metre. The unit is set at one step detection sensitivity when the switch is slid to the left uncovering one spot.

'Two Step' setting corresponds to continuous movement of about 2½ metres. The device is set at Two Step detection sensitivity when the switch is slid to the right uncovering two spots.

Walk test

After connecting up the product, the LED will remain unlit until an alarm condition is reached. Provided that the W/T terminals have been linked the LED will light at the same moment that the relay is caused to drop out by an alarm condition. In order that a wide variety of control units may be used there is a slight delay before the relay is re-energised after the alarming movement ceases.

Figure 2 **Polar diagram**



The polar diagram is only applicable to freespace applications.

Avoidable problems

1. **Air movement**

Since air is the medium for ultrasonic transmission, severe turbulence or draughts will cause problems with any ultrasonic system. Much thought and careful design has gone into the circuity to reduce false alarms from air movement but ultimately no amount of electronic filtering or trickery can combat conditions of extreme air turbulence. Particular attention must be given to siting to eliminate problems of this type. For example a unit mounted immediately above a doorway or an ill-fitting window, through which draughts are likely, could give trouble. Fast moving heated air, such as that produced by fan heaters, is particularly turbulent. Under no circumstances should ultrasonic detectors be used in areas heated in this way.

2. **Extraneous noises**

The RS ultrasonic intruder detector operates at 32kHz. Hissing steam or airlines are particularly strong in high frequency sound components. Door bells and telephone bells can give rise to false alarms. A possible cure is to drill a hole or holes in the offending bell which reduces the amplitude of its high frequency components. Alternatively, re-site the unit.

Connection diagrams

Figure 3 **Single unit operation**

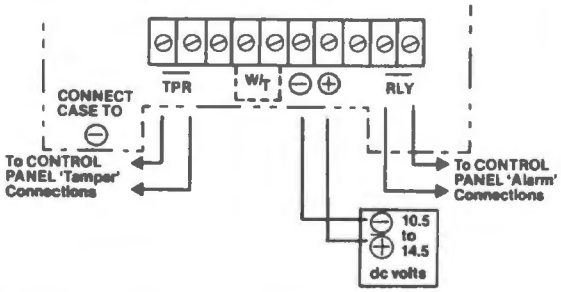
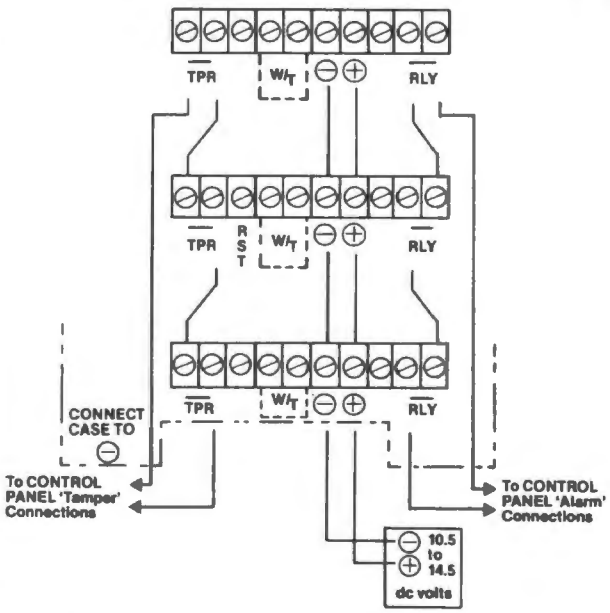


Figure 4 **Multiple unit operation**



Note

1 Sometimes it may be desired to mute the walk test LED in which case the link is omitted or switched. When control box design permits the use of a common return for tamper, power supply and relay, only 4 core cable is required.

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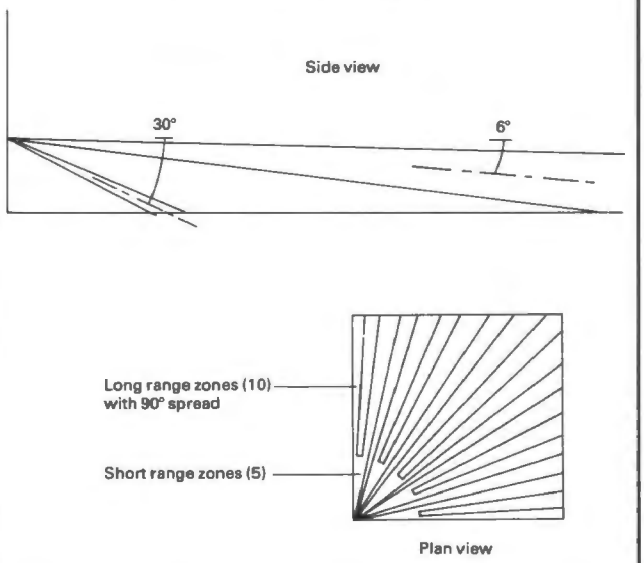
Passive infra-red intruder detector (301-423)

The RS passive infra-red intruder detector gives detection of a moving person at distances of up to 15 metres, over an angle of 90°. This detector uses a dual element pyro-electric sensor to detect a moving body whose thermal radiation is different from that of the background. It is arranged that no detection output is produced by radiation focused on both elements at the same time; such as from a stationary object, but an alarm signal is generated when radiation falls on just one and then the other element such as a moving object reflection. Thus the effects of sunlight, heaters and air currents are virtually ignored.

The faceted parabolic mirror splits the detection field into ten long and five short range fields with a spread of 90°. See Figure 5.

Figure 5 **Pattern of detection zones**



Siting

Although the RS detector is extremely stable it should be sited to avoid direct sunlight, strong lighting and heat sources. The best position for the detector is in a (hidden) corner where a maximum area of surveillance is achieved (Figure 6). It is important that the unit is fixed at the right height for optimum surveillance. The height will depend upon the size of area to be protected and will vary between 2.3m for a large area to 1.5m for a small area. Figure 7 shows how an increase in detector height increases the effective range. A further 12 degrees of tilt can be obtained by using the fixing bracket.

Features

- High immunity to false alarms
- Maximum range 15m
- 90° coverage
- Single or multiple operation
- Low power consumption

Figure 6 **Siting**

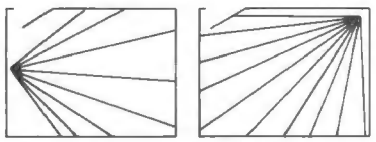
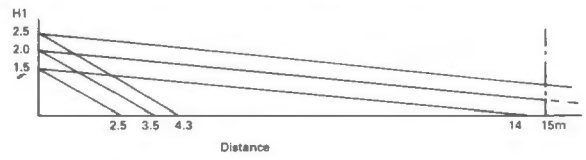


Figure 7 **Effect of range as a function of height**

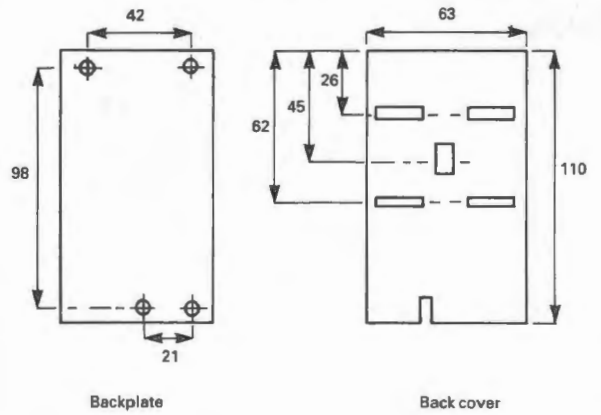


Fixing

The detector may be positioned and secured directly or by using the back cover fixing bracket. The back cover fixing bracket slots permit corner fixing.

1. **Direct fixing:** remove the front cover from the backplate. Remove and discard the fixing bracket. Secure the detector directly using the four 3.0mm holes in the backplate. Replace the front cover after the unit connections have been made.
2. **Back cover fixing bracket:** secure the fixing bracket in the required position using the slotted holes. Remove the front cover from the backplate then position the detector on the fixing bracket by pushing the holes over the fixing bracket pegs. Secure the detector to the fixing bracket by using the four self-tapping screws provided. Replace the front cover after the unit connections have been made.

Figure 8 **Fixing details**



Connections

The connections are made to the screw terminals at the top of the detector as in Figure 10. A small 'knockout' is provided in the back and top for cable entry. An internal micro-switch (tamper switch) is fitted with one pair of clean NC contacts for connection to an alarm control panel. The switch contacts will be opened when the unit front cover is removed.

Memory enable (terminal 8): To use the facility it will be necessary to connect terminal 8 to a +12V DC supply. This supply must be a separately switched +VE 12V DC output from the control panel actuated by the panel control switch. In this latched mode the walk test LED will be disabled.

Figure 9 **Front view – cover removed**

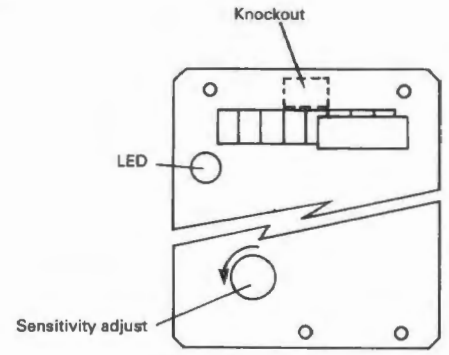
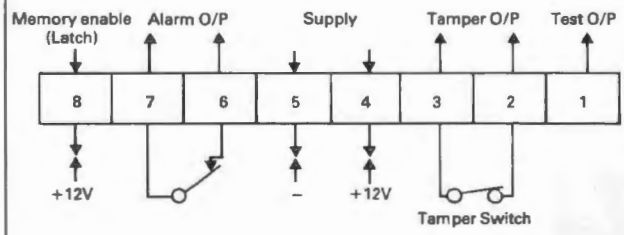


Figure 10 **Terminal strip connections**



Test and operation

On connecting a 12 volt supply to the detector the unit will go into alarm condition for about 50 seconds then reset to normal. The detector can be walk-tested on initial set-up to establish the correct coverage pattern. The walk-test LED will illuminate for approximately 8 seconds.

If severe thermal turbulence is present it may be necessary to reduce the sensitivity to ensure consistent operation.

To test for thermal turbulence connect a DC voltmeter (10V range) to terminal 1 and terminal 5 (–VE) with no movement in the area the meter should settle at about 3 volts. Under worst case conditions of turbulence reduce the sensitivity control until the meter fluctuates not more than 0.5V. Verify that the detection range is still adequate. It may be necessary to fit long test leads to ensure testing is carried out with the operator outside the detection field.

On completion of the tests connect the latching terminal to the 12 volt supply via the control panel and walk-test the detector. There should be no LED illuminated but the alarm should be activated. To reset, the switched 12V supply is switched off which will cause the walk-test LED to illuminate (if an intrusion has taken place). The detector will reset when the control panel is switched to the 'on' position and off again. Once the latch has been cleared the walk-test LED will operate as normal.

Note: The memory enable has no effect on the output relay which will switch on and off with detection in either mode.

Active infra-red intruder detector (630-544)

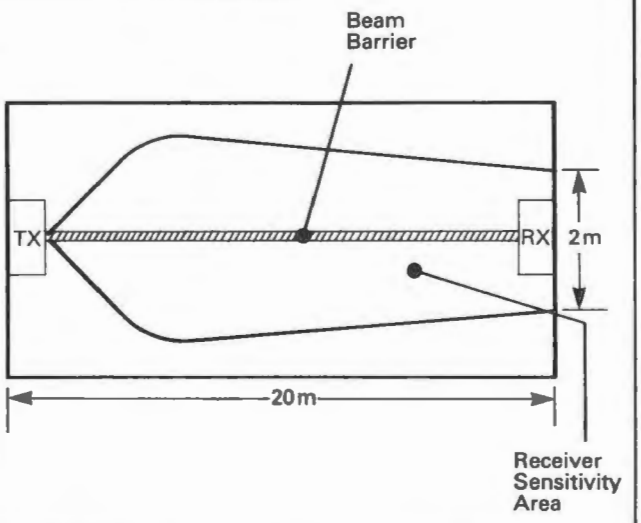
The RS active infra-red detector is a modulated infra-red beam barrier that is activated when the invisible beam is interrupted. The detector is suitable for use over any distance up to 20m. The transmitted beam is wide angle and does not rely on the setting of mirrors to focus the beam. Provided the receiver is installed within the beam area a 25mm dia. link will be achieved (see Figure 11).

Specification

Conforms to	BS4737
Range	20m
Temperature	0°C to +40°C
Voltage range	10.5V-14V
Typical current	20mA TX, 30mA RX
Alarm period	Minimum 1 sec
Response time	40ms
Dimensions	70×70×36mm
Weight	170g pair
Tamper	N/C 50mA 12V dc
Alarm relay	Change over contacts 1A at 24Vdc max 0.5A at 110Vac max
Alignment	2m diameter at 20m

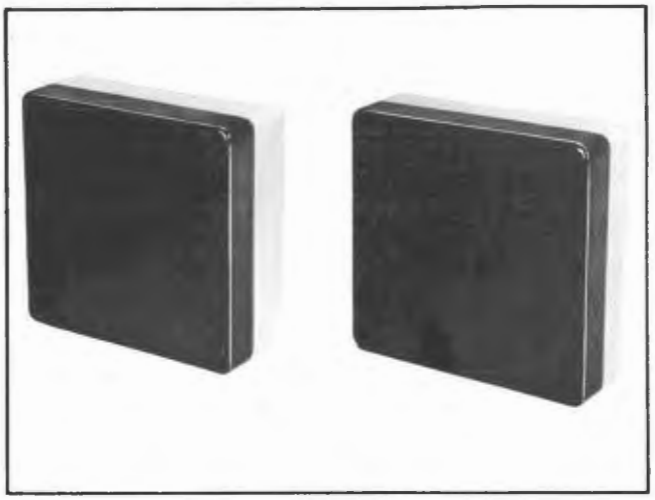
LED operation
Transmitter on. Receiver on when safe, off in alarm. Both LEDs may be blanked if required.

Figure 11 **Working area**



Features

- 20m Normal range
- Wide angle transmitted beam for ease of setting
- Low power consumption
- High immunity to false alarms



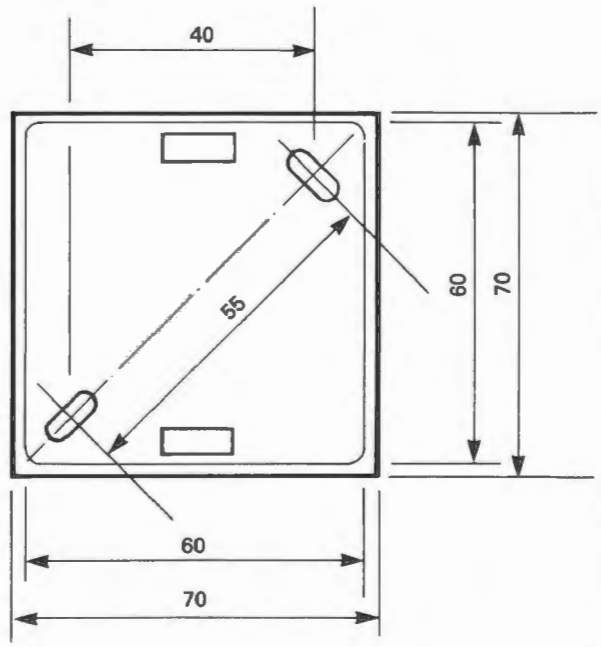
Siting

Ensure that sunlight does not fall directly on the receiver and that fluorescent light units are not close or in line of sight. Avoid mounting the units alongside reflective surfaces, eg. glass and painted walls as these will produce an alternative beam path and interfere with correct operation.

Fixing

1. Remove red and black fronts from units and unclip circuit boards, taking note of the differences between the two units.
2. Fix the white base units at the same height, opposite and directly facing each other not more than 20m apart. Ensure that the units are mounted on a firm structure remembering that the barrier is a single optical link less than 25mm in diameter.

Figure 12 **Fixing details – back view**



Connections

The connections are made to screw terminals at the side of the detector (when the board is fitted) as in Figure 13. An internal tamper switch is fitted to both transmitter and receiver with clean NC contacts for connection to an alarm control panel. The switch contacts will be opened when the unit front cover is removed.

Figure 13 **Terminal strip connections**

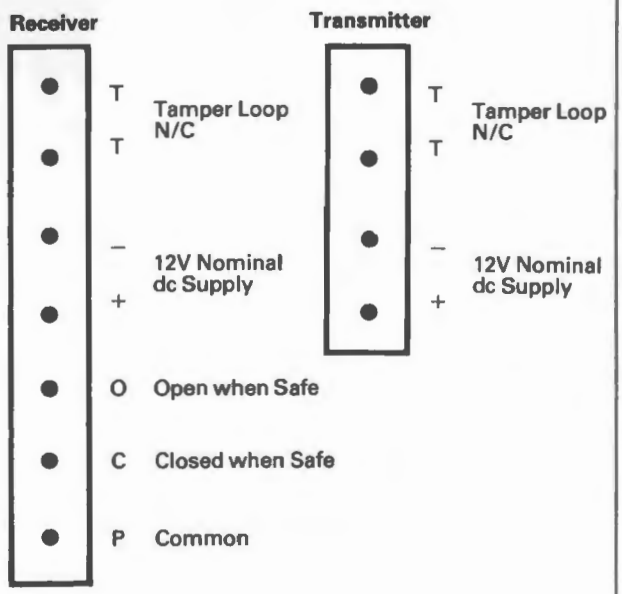
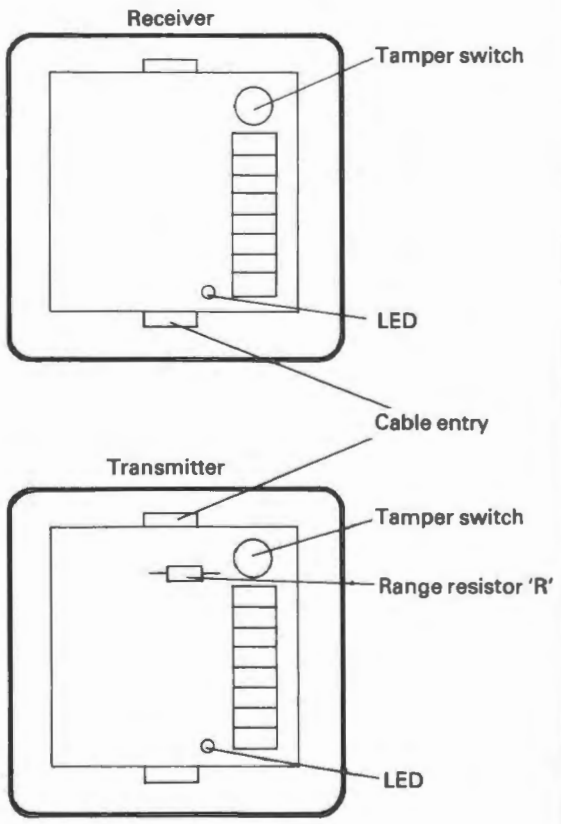


Figure 14 **Front view – cover removed**



Test and operation

Connect both units, transmitter and receiver, to the 12 Volt supply and if correctly aligned both LEDs will illuminate. The detection beam is only 25mm dia. and its sensitivity should be checked. Note that only the LED on the receiver is off in the alarm condition. If the transmitter and receiver are too close, less than 5m, then the resistor marked 'R' on the transmitter board should be cut.

Environment

The equipment will work in most indoor environments but as with all optical devices will not continue to give reliable operation in areas giving rise to dust, grease etc. which in time will tend to obscure the beam.

Problems can also arise in damp areas subject to low temperatures where condensation or frosting may occur.

RS data

Intruder detector comparison

The following table is intended as a guide for intruder detectors:

	Ultrasonic	Passive Infra-Red	Active Infra-Red
Vibration	Possible problem (see text)	OK	OK
Sensitivity	Not suitable	Possible problem	OK
Range reduction due to soft furnishings, curtains etc.	Possible problem (see text)	OK	OK
Draughts and air movement	Not suitable	Possible problem	OK
Moving machinery	Not suitable	Slight problem	OK
Ultrasonic noise – telephones etc.	Possible problem (see text)	OK	OK
Interference between two or more sensors	OK (see text)	OK	OK
Sunlight on sensor	OK	Possible problem	Possible problem
Effect of temperature	Slight problem	OK (see text)	OK
Effect of humidity	Slight problem	OK	Slight problem
Heaters	OK	Possible problem (see text)	OK
Unwanted detection through walls or glass	OK	OK	OK

Many of the problem areas mentioned above can be overcome by careful siting of the intruder detectors.

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
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Telephone: 0536 201234
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RS data

8-bit D to A/A to D converter ZN435

Stock number 301-735

General circuit operation

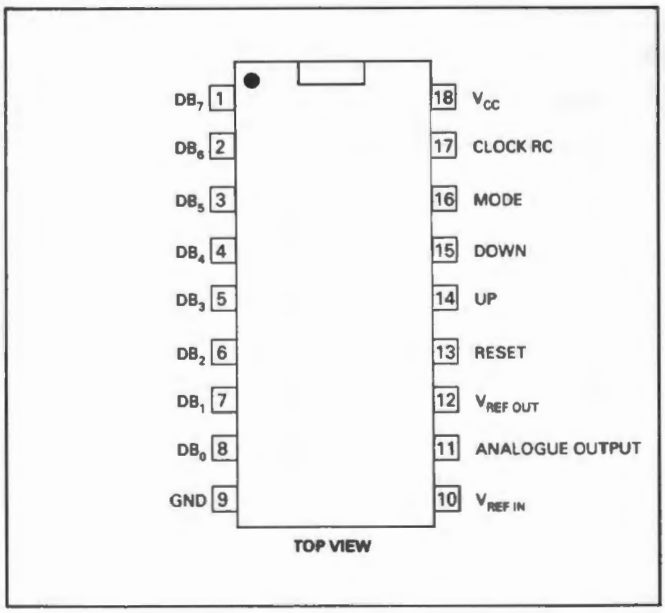
The 435 uses an 8-bit digital to analogue coverter based on an R-2R ladder network. The reference voltage required may be derived from the on-chip precision bandgap reference or an external source. An 8-bit up/down counter is also included and the converter may receive its digital input data from the counter with the counter outputs being simultaneously available at the 8-bit I/O port. Alternatively the counter outputs may be inhibited and the I/O port used to feed data directly to the converter inputs. An on-chip oscillator is provided to drive the up/down counter but may be overriden by an external clock.

Absolute maximum ratings

Supply voltage V_{CC} ____ +7V
Maximum voltage Logic and V_{REF} ____ V_{CC}
Operating temperature ____ 0°C to +70°C
Storage temperature ____ –55°C to +125°C

Features

- 8-bit resolution
- 800ns setting time
- Operation as DAC or ADC etc
- On chip up/down counter
- On chip clock and reference
- Single +5V suply operation



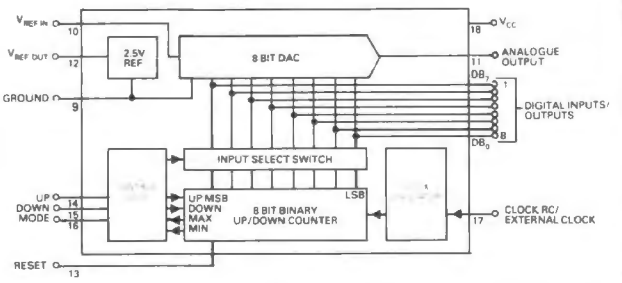
Electrical characteristics

T_{AMB} = 25°C, V_{CC} = +5V, V_{REF} = 1.5 – 3.0V

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply voltage		4.5	5.0	5.5	V
Supply current	V_{CC} = 5.5V		35	45	mA
Converter					
Resolution		8			bits
Linearity error	T_{Min} to T_{Max}		±0.25	±0.5	LSB
Differential linearity error			±0.25	±1	LSB
Zero error	All bits off		3.0	5.0	mV
Setting time to 0.5 LSB	All bits off to on		500		ns
	All bits on to off		800		ns
Full scale output	All bits on, 2.56V ref	2.545	2.550	2.555	V
Output resistance			4		kΩ
Full scale temp. coefficient	Ext. V_{REF} = 2.56V		4		ppm/°C
Reference voltage input		0		3	V
Voltage reference					
Reference output voltage	R_{REF} = 390Ω	2.4	2.59	2.7	V
Slope resistance	C_{REF} = 220nF		2	4	Ω
Temp. coeff. of V_{REF}			50		ppm/°C
Reference current		4		15	mA

Parameter	Conditions	Min.	Typ.	Max.	Units
Counter					
Counter high voltage threshold				2.3	V
Counter low voltage threshold		1.7			V
Counter max. clock frequency		1	1.5		MHz
Clock					
Max. frequency		500			kHz
Clock frequency temp. coeff.			100		ppm/°C
Clock resistor		3		100	kΩ
Clock capacitor		100			pF
High voltage threshold			4.6		V
Low voltage threshold			1.5		V
Supply rejection			0.8		%/V
Digital Inputs					
High level input voltage		2.0			V
Low level input voltage				0.8	V
High level input current	V_{IN} = 2.4V			–100	μA
Low level input current	V_{IN} = 0.4V			–220	μA
Digital Outputs					
High level output voltage	No load		5.0		V
Low level output voltage	No load		0.1		V
High level output current	V_{OUT} = 2.4V	125			μA
Low level output current	V_{OUT} = 0.4V	–3.0			mA
Control inputs					
High level input voltage		2			V
Low level input voltage				0.8	V
High level input current	V_{IN} = 2.4V			–25	μA
Low level input current	V_{IN} = 0.4V			–95	μA
Reset pulse width		200			ns

Figure 1 **System diagram**



Reset	Mode	Down	Up	Digital function	Analogue waveform
1	1	1	1	Counter Stopped.	
1	1	1	0	Count up continuously.	
1	1	0	1	Count down continuously.	VREF 0
1	1	0	0	Count up, reverse at FS, count down, reverse at zero.	VREF 0
1	0	1	1	Counter Stopped.	
1	0	1	0	Count up, Stop at FS.	0 VREF
1	0	0	1	Counter down, Stop at zero.	VREF 0
X	0	0	0	DAC MODE, Counter output disabled. Counter can still be reset by taking reset input low.	
0	X	X	X	Counter reset. Does not affect analogue output in DAC MODE.	

Table 1 **Control functions**

Up/Down counter

The counter is a high speed synchronous type which is controlled by four inputs Up, Down, Reset and Mode. Up, Down and Reset are standard functions with the Mode control determining the behaviour of the counter at zero and full scale. With the Mode input in the High State the counter will reset to zero if it is clocked past full scale in the up direction. Alternatively it will reset to 255 if it is clocked past zero in the down direction. When Mode is low the counter will stop on reaching full-scale or zero. See Table 1 for complete control function operation.

Data Port

Figure 2 shows one bit of the data port. Normally the converter is driven from the counter and the counter data is also available at the port. If required the counter outputs can be disabled with the coverter inputs then being accessed from the data port. The input data port is compatible with B series CMOS, TTL and LSTTL.

Figure 2 **Bit inputs/outputs**

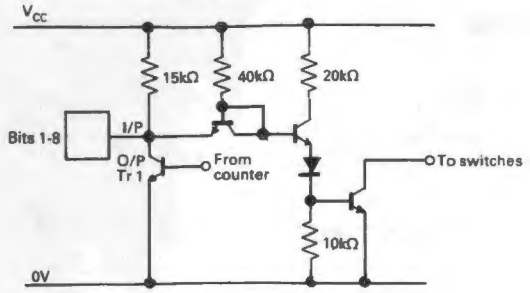
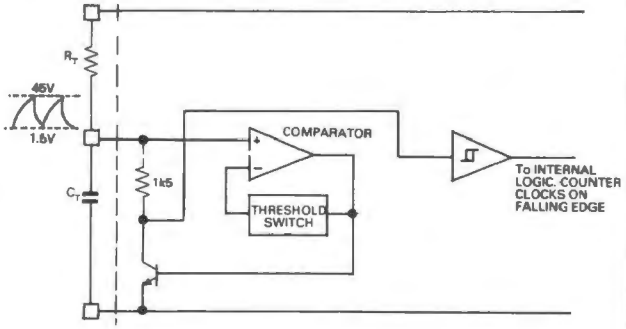


Figure 3 **Clock circuit**



Clock circuit

The circuit is shown in Figure 3 and the frequency of the clock is given by

$$f_{CK} = \frac{1}{4R_TC_C}$$

f in hertz
R in Ω
C in Farads.

See Figure 4 for characteristic graphs.

The clock can be overdriven directly by a TTL totem pole output see Figure 5 for other logic interfaces.

Figure 4

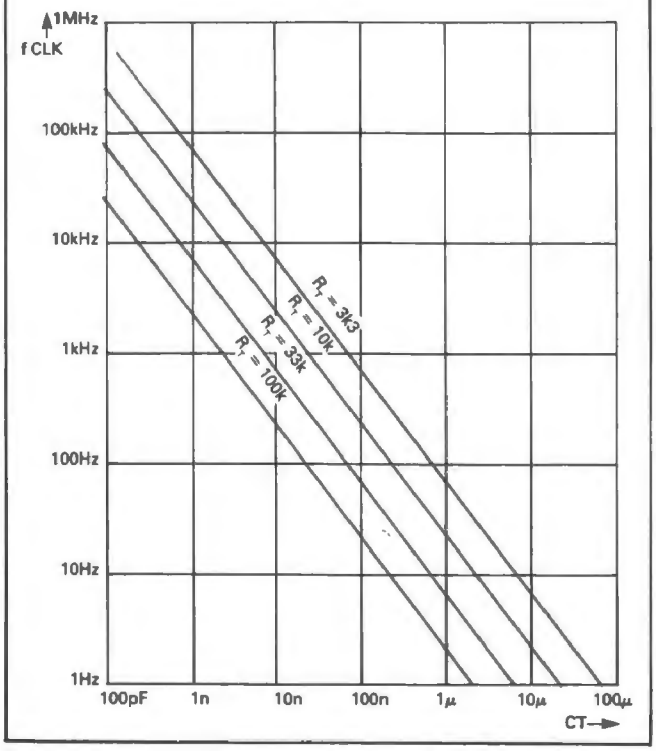
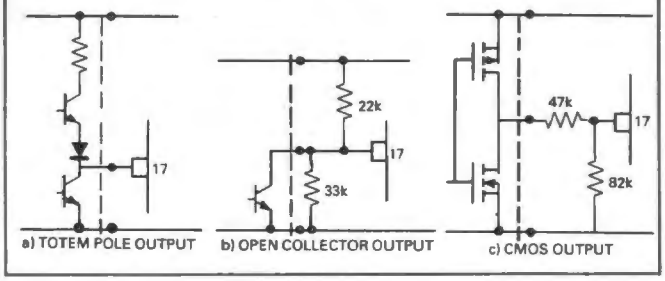


Figure 5 **Overdriving the clock input**



Analogue circuits

D to A converter

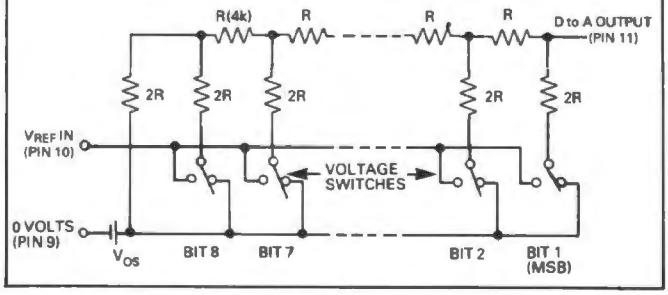
The converter uses a voltage switching R-2R ladder network where

$$V_{OUT} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input from the data port or counter.

V_{OS} is a small offset voltage produced by the device supply current flowing in the package lead resistance, being typically 3mV. This offset will normally be removed by the setting up procedure and as the offset temperature coefficient is small the zero drift will be small. The converter output range will be 0V to $V_{REF\ IN}$ with the output resistance R = 4K.

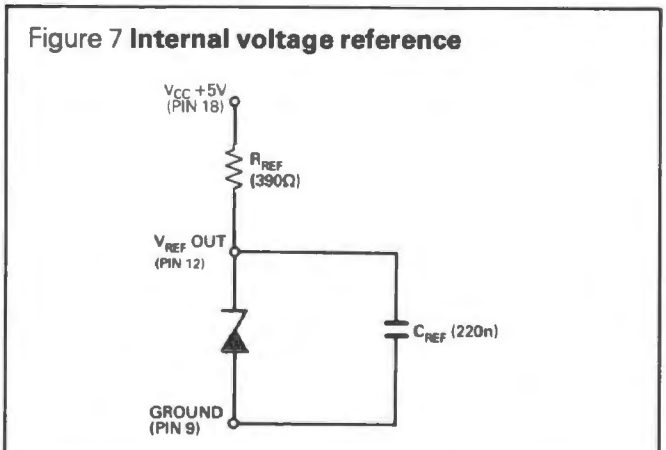
Figure 6 **R2-R ladder network**



Internal voltage reference

Figure 7 shows the connection of this circuit and to make use of this reference the $V_{REF\ OUT}$ pin 12 is connected to $V_{REF\ IN}$ pin 10. The circuit of Figure 7 will supply a reference current of 6.4mA which will drive up to five ZN435s.

Figure 7 **Internal voltage reference**



RS data

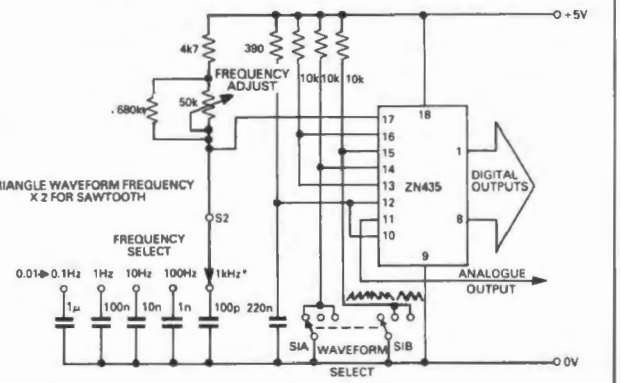
Application circuits

The following are some basic circuits which can be configured with the 435, however numerous possibilities exist.

Waveform generator

Figure 8 shows a low frequency waveform generator this will produce a linear sawtooth and triangular waveform generator.

Figure 8 **Waveform generator**

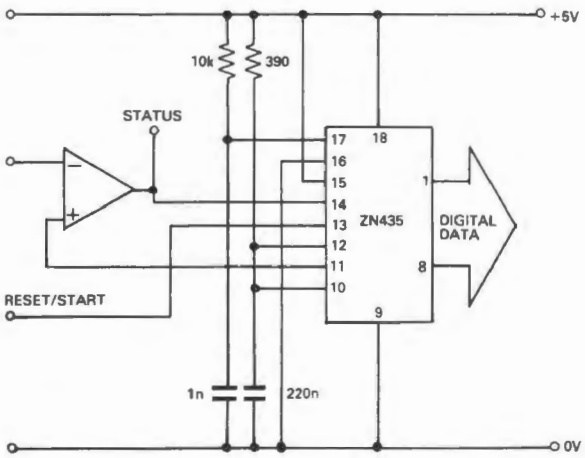


Ramp and compare A to D converter

A simple ramp and compare A to D converter can be built using the 435 and an external comparator see Figure 9. The counter is set to count up from zero, producing a positive going ramp at the analogue output. When the ramp voltage exceeds the analogue input the comparator output will go high inhibiting the clock and stopping the counter. The converter can be reset and restarted by applying a low going pulse to the reset input.

The basic analogue input range is 0 to V_{REF}, but other ranges can be accommodated by adding an attenuator to the comparator input. The comparator offset adjustment can be used for zero adjustment. Note that in this circuit the Mode input is tied low to make the counter stop at full scale. This prevents the counter cycling in the event of an overrange input.

Figure 9 **Ramp and compare ADC**



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RS data

Data bus isolators

Stock number 208-355

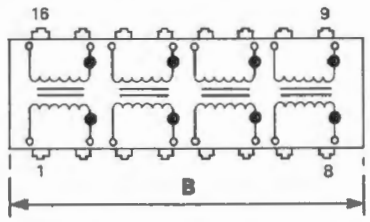
The RS Data Bus Isolators are pulse transformers with high input to output isolation. They are designed to give an optimum pulse width capability at high repetition rates making them ideal for microprocessor bus isolation applications. Four isolators are housed in a single 16 pin dual-in-line package. Isolation of the data, address and control buses of microprocessor based equipment can be achieved easily and effectively, and with the addition of a dc-dc converter whole systems can be isolated one from the other.

The isolators have three important features:

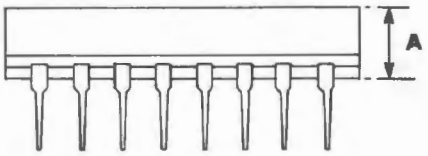
1) They are inherently bi-directional.
2) They can be connected to invert or non-invert as desired.
3) The frequency response is ideal for high speed logic circuitry.

The first of these features is essential for data bus systems since data is inherently bi-directional in nature. The second is convenient when control lines need either invert or non-invert facilities. A good high frequency response is necessary for operation with modern high speed microprocessors.

The power demand of these devices is negligible and more particularly no external current limiting components are needed. Direct connection can be made to logic buffers and/or tri-state gates.



Standard 0.3in 16 pin dip
MAX. DIMENSIONS: A 22.5mm
B 5.6mm



DIL CASE MATERIAL – DAP
(DIALLYL PHTHALATE)

Electrical characteristics

V_{BR} Isolation breakdown voltage ___ 500V rms (max)
R_{INS} Insulation resistance at 500V dc ___ $>10^{10}$ ohms
t_{pd} Propagation delay _____ <5ns
t_{pw} Maximum pulse width at logic supply voltage (see Figure 1)
t_{rr} Maximum repetition rate at pulse width (see Figure 2)
Storage temperature range _____ –40°C to +125°C
Operating temperature range _____ 0°C to +80°C

Figure 1 **Supply voltage/Pulse width**

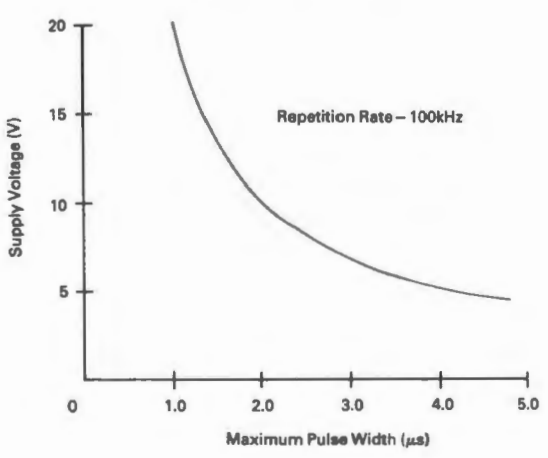
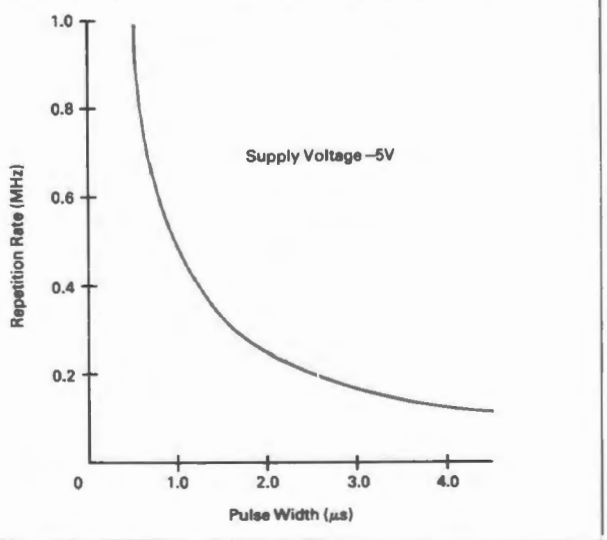


Figure 2 **Repetition rate/Pulse width**



Connection diagrams

Figure 3 **Non-inverted positive going pulses**

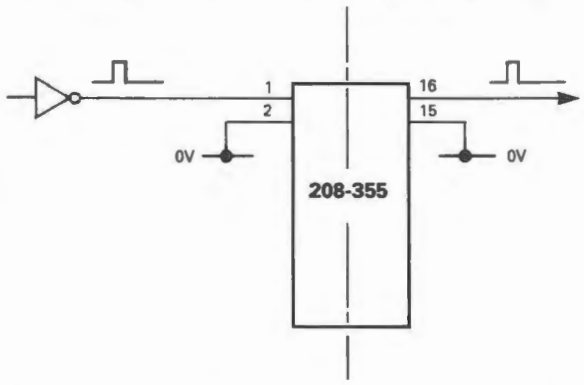


Figure 4 **Non-inverted negative going pulses**

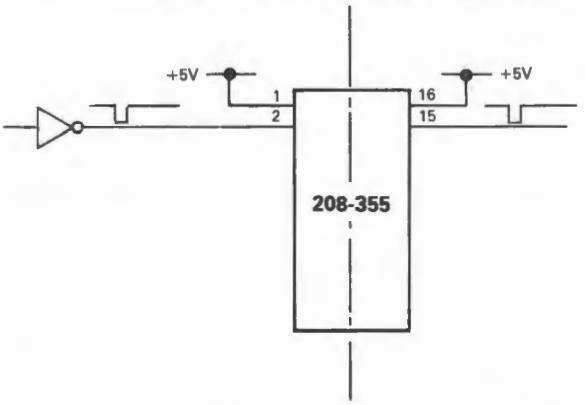


Figure 5 **Inverted positive going pulses**

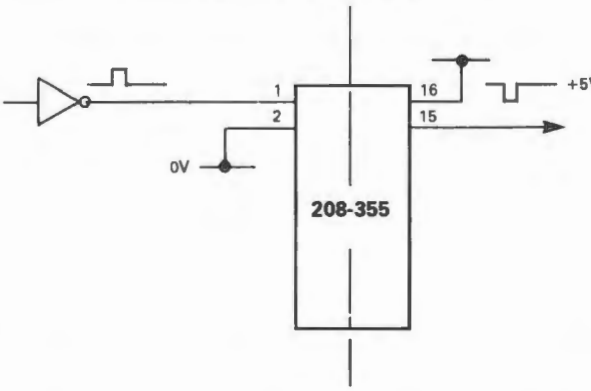
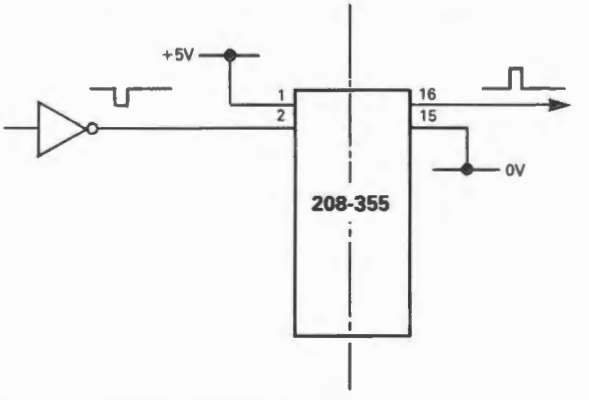


Figure 6 **Inverted negative going pulses**

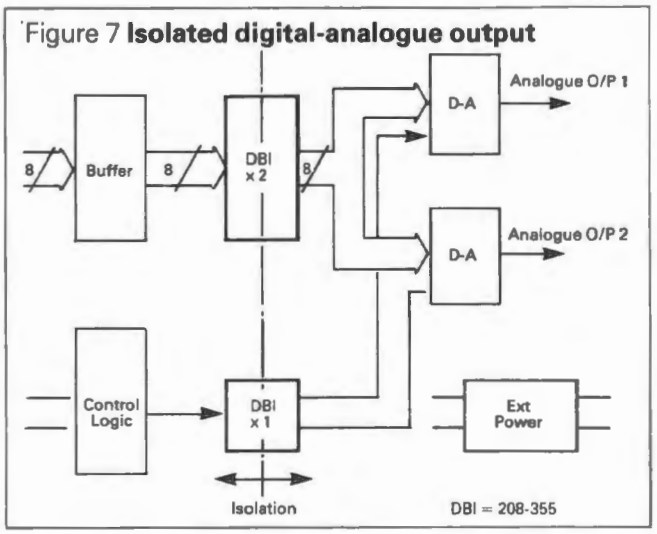


Data bus isolator applications

Isolated digital analogue output

The 8 bit data to be output to the D-A converters is latched into each of the converters via two Data Bus Isolators. The latching signals are also isolated via a Data Bus Isolator. If the isolated output circuitry is provided with an uninterruptable power source then 'level-freeze' can be accomplished should the system supplies fail. Common mode potentials can be present at the analogue outputs without affecting the system performance.

Figure 7 **Isolated digital-analogue output**

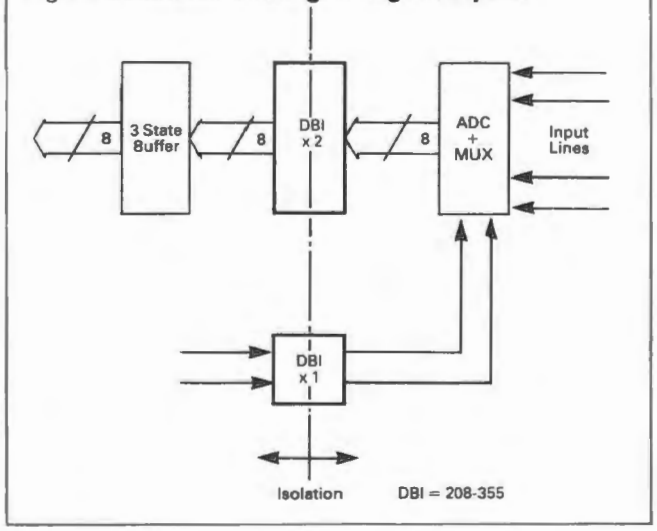


Isolated analogue-digital inputs

The multiplexer, amplifier and A-D converter of a typical data collection system can be isolated most effectively and with a minimal effect upon system accuracy by placing the isolation at the digital interface. The isolation is just before the 3-state buffers which place the converted data on to the system data bus. Control lines are isolated as required and a dc-dc converter supplies power for the isolated circuitry.

The whole 'front end' can now float to any local common mode potential present at the transducer under measurement while allowing an accurate conversion to take place. This approach is simpler and cheaper than the traditional 'flying capacitor' technique.

Figure 8 **Isolated analogue-digital inputs**

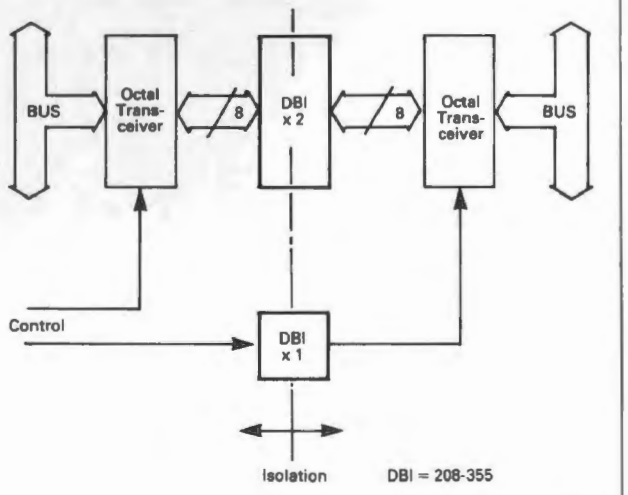


Isolated transceiver bus

Multi-microprocessor systems with different power supplies can suffer from latch-up and catastrophic failure problems at 'power-up' and if the supplies are more than a few hundred millivolts different from each other. Bus isolation is a simple and effective solution to such problems and as they are bi-directional the additional package count is low.

In the illustration two octal transceivers are isolated via a pair of Data Bus Isolators which effectively separates the two systems galvanically. Now either system can sit at any desired local potential and contention between different supplies during 'power-up' is not possible.

Figure 9 **Isolated transceiver bus**



RS data

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An Electrocomponents Group Company

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RS data

Video modulator RS 1889

Stock number 301-662

The RS1889 is designed to interface audio, colour difference and luminance signals to the aerial socket of a television receiver. It consists of a sound subcarrier oscillator, chroma subcarrier oscillator, quadrature chroma oscillators and RF oscillators and modulators for direct interface with two low VHF channels or with the addition of a basic frequency changer, will interface with VHF channels.

The RS1889 allows video information from video tape recorders, games, test equipment or similar sources to be displayed on black and white or colour television receivers, or additionally can provide a composite video output.

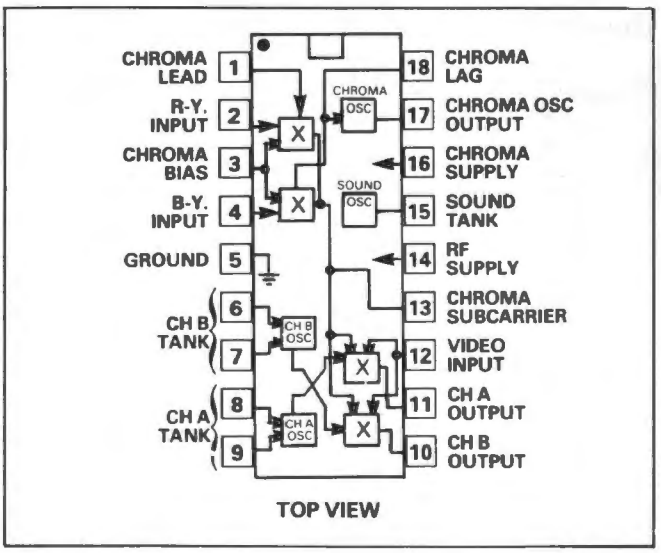
Absolute maximum ratings

Supply voltage V14, V16 max	19 V_{dc}
Power dissipation package (Note 1)	1390mW
Operating temperature range	0°C to +70°C
Storage temperature range	–55°C to +150°C
Chroma Osc current I_{17} max	10mA_{dc}
V16 – V15) max	±5V dc
(V14 – V10) max	7V
(V14 – V11) max	7V
Lead temperature (soldering, 10 seconds)	300°C

Note: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90° C/W junction to ambient.

Features

- DC channel switching
- 12V to 18V supply operation
- Excellent oscillator stability
- Low intermodulation products
- 5 Vp-p chroma reference signal
- May be used to encode composite video



TOP VIEW

DC Electrical characteristics (dc Test circuit, all SW normally pos. 1, V_A = 15V, V_B = V_C = 12V)

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Current, I_S		20	35	45	mA
Sound Oscillator, Current Change, ΔI_{15}	Change V_A from 12.5V to 17.5V	0.3	0.6	0.9	mA
Chroma Oscillator Balance, V17		9.5	11.0	12.5	V
Chroma Modulator Balance, V13		7.0	7.4	7.8	V
R-Y Modulator Output Level, ΔV13	SW 3, Pos. 2, Change SW 1 from Pos. 1 to Pos. 2	0.6	0.9	1.2	V
B-Y Modulator Output Level, ΔV13	SW 3, Pos. 2, Change SW 2 from Pos. 1 to Pos. 2	0.6	0.9	1.2	V
Chroma Modulator Conversion Ratio, ΔV13/ΔV3	SW 3, Pos. 2, Change SW 0 from Pos. 1 to Pos. 2. Divide ΔV13 by ΔV3	0.45	0.70	0.95	V/V
Ch. A Oscillator 'OFF' Voltage, V8, V9	SW 4, Pos. 2	0.5	1.5	3.0	V
Ch. A Oscillator Current Level, I_9	V_B = 12V, V_C = 13V	3.0	4.0	5.5	mA
Ch. B Oscillator 'OFF' Voltage, V6, V7		0.5	1.5	3.0	V
Ch. B Oscillator Current Level, I_6	SW 4, Pos. 2, V_B = 12V V_C = 13V	3.0	4.0	5.5	mA

Parameter	Conditions	Min.	Typ.	Max.	Units
Ch. A Modulator Conversion Ratio, $\Delta V11/(V13 - V12)$	SW 1, SW 2, SW 3, Pos. 2, V_B = 12V, Change V_C from 13V to 11V for $\Delta V11$ divide by V13 – V12	0.35	0.55	0.75	V/V
Ch. B Modulator Conversion Ratio, $\Delta V10/(V13 - V12)$	All SW, Pos. 2, V_B = 12V, Change V_C from 13V to 11V divide as above.	0.35	0.55	0.75	V/V

AC Electrical characteristics (ac Test Circuit, V = 15V)

Parameter	Conditions	Min.	Typ.	Max.	Units
Chroma Oscillator Output Level, V17	$C_{LOAD} \leq 20pF$	4	5		Vp-p
Sound Carrier Oscillator Level, V15	Loaded by RC Coupling Network	2	3	4	Vp-p
Ch. 3 RF Oscillator Level, V8, V9	Ch. Sw. Pos. 3, f = 61.25MHz, use FET Probe	200	350		mVp-p
Ch. 4 RF Oscillator Level, V6, V7	Ch. Sw. Pos. 4, f = 67.25MHz, Use FET Probe	200	350		mVp-p

Design characteristics (ac Test Circuit, V = 15V)

Parameter	Typ.	Units
Oscillator Supply Dependence		
Chroma, f_o = 3.579545MHz	3	Hz/V
Sound Carrier, RF	See Curves	
Oscillator Temperature Dependence (IC Only)		
Chroma	0.05	ppm/°C
Sound Carrier	–15	ppm/°C
RF	–50	ppm/°C
Chroma Oscillator Output, Pin 17		
t_{RISE}, 10-90%	20	ns
t_{FALL}, 90–10%	30	ns
Duty Cycle (+) Half Cycle	51	%
(–) Half Cycle	49	%
RF Oscillator Maximum Operating Frequency (Temperature Stability Degraded)	100	MHz
Chroma Modulator (f = 3.58MHz)		
B-Y Conversion Gain V13/(V4–V3)	0.6	Vp-p/V
R-Y Conversion Gain V13/(V2–V3)	0.6	Vp-p/V
Gain Balance	±0.5	dB
Bandwith	See Figure 5	

Parameter	Typ.	Units
RF Modulator		
Conversion Gain, f = 61.25MHz, $V_{OUT}/(V13 - V12)$	10	mVrms/V
3.58MHz Differential Gain	5	%
Differential Phase	3	degrees
2.5Vp-p Video, 87.5% mod.		
Output Harmonics Below Carrier		
2nd, 3rd	–12	dB
4th and above	–20	dB
Input Impedances		
Chroma Modulator, Pins 2, 4	500k//2pF	
RF Modulator, Pin 12	1M//2pF	
Pin 13	250k//3.5pF	

Figure 1 **DC test circuit**

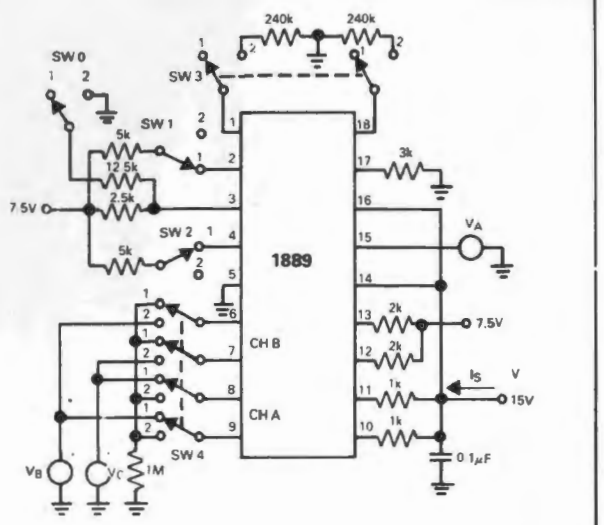


Figure 2 **AC test circuit**

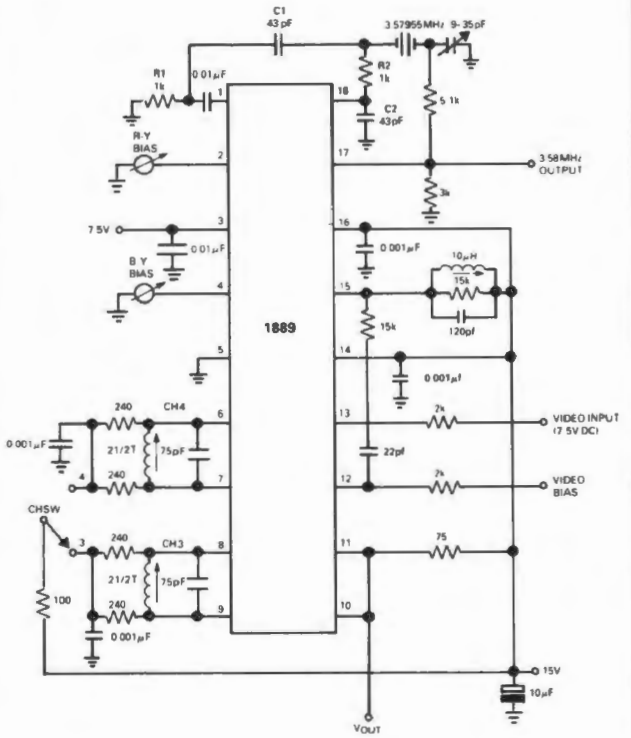


Figure 3
Sound carrier oscillator supply dependence
(f_O = 4.5 MHz)

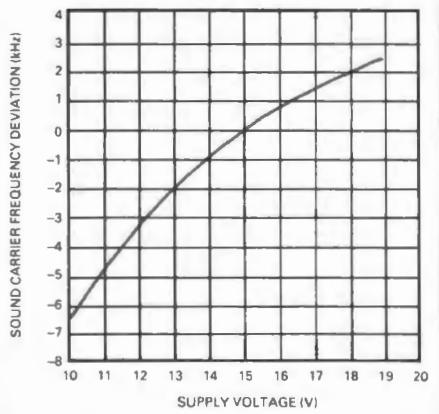


Figure 4
RF oscillator frequency supply dependence
f_O = 67.25MHz

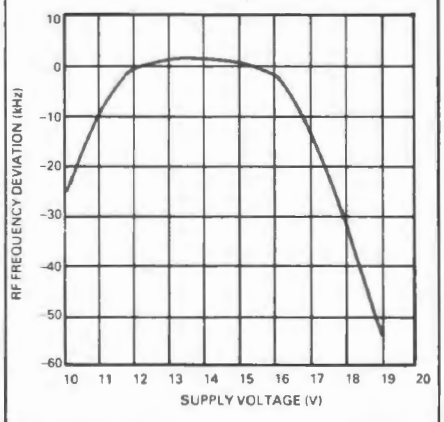


Figure 5
Chroma modulator transconductance bandwidth
$I_{OUT\ 13}/V1$ or 18

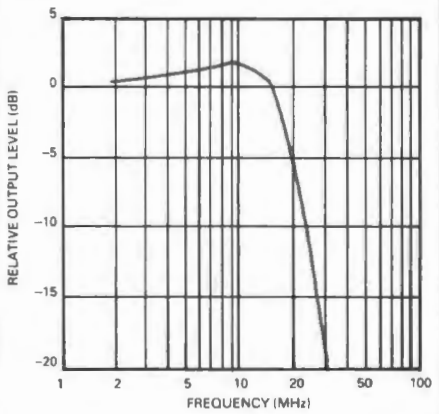


Figure 6
Chroma modulator common-mode input range
Pins 2, 3, 4

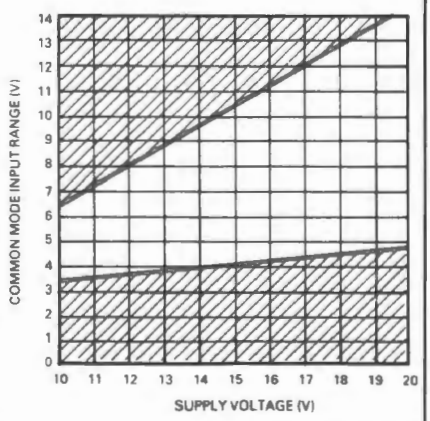
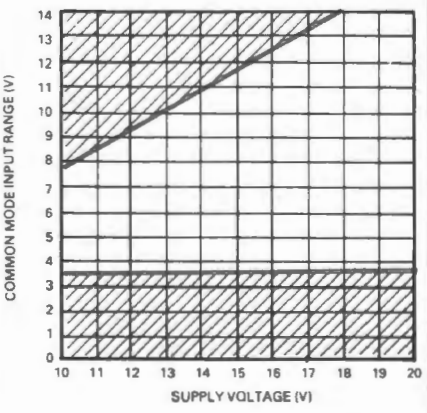


Figure 7
RF modulator common-mode input range
Pins 12, 13 (Application circuit)



Description (Refer to circuit diagram)

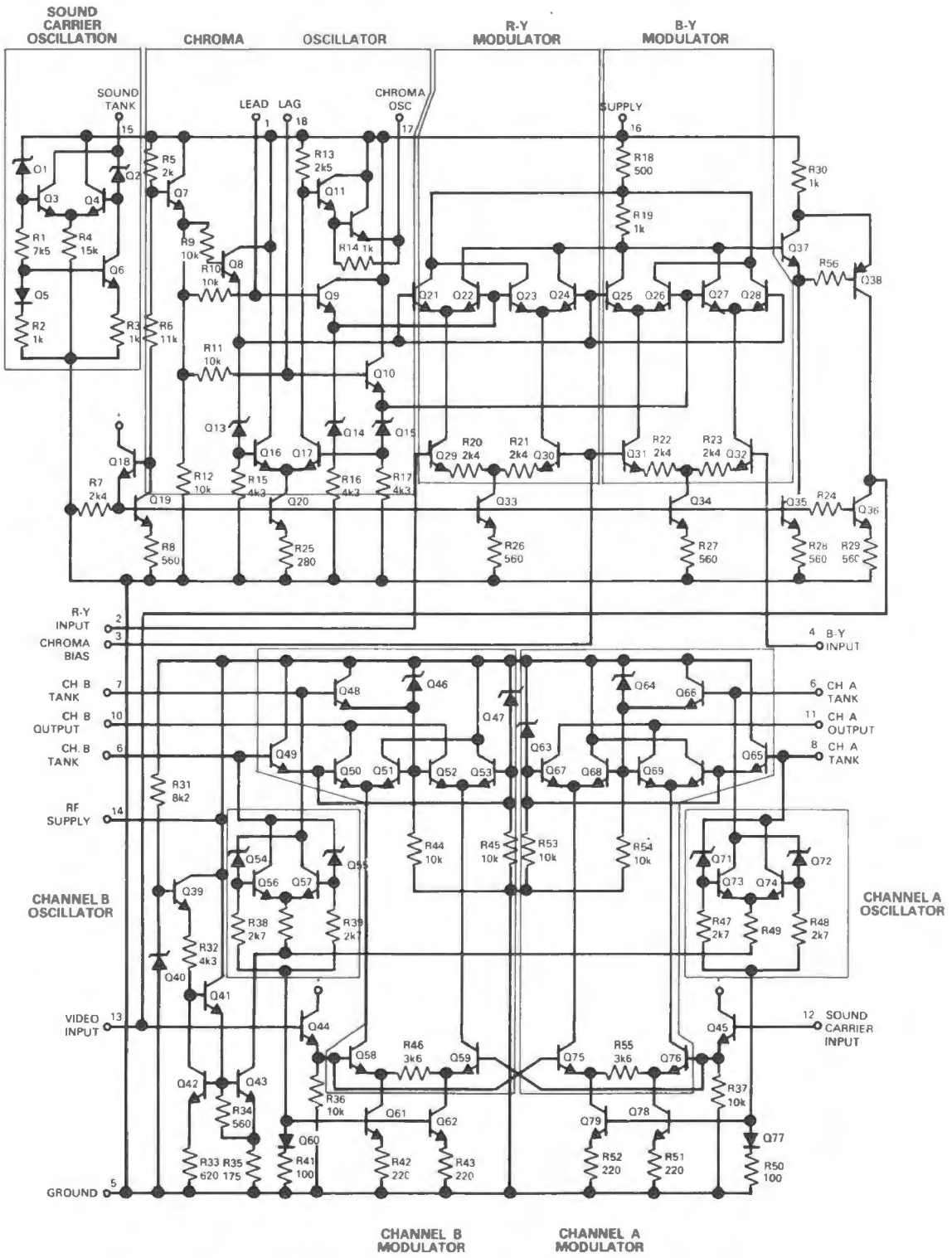
The sound carrier oscillator is formed by differential amplifier Q3, Q4 operated with positive feedback from the pin 15 tank to the base of Q4.

The chroma oscillator consists of the inverting amplifier Q16, Q17 and Darlington emitter follower Q11, Q12. An external RC and crystal network from pin 17 to pin 18 provides an additional 180 degrees phase lag back to the base of Q17 to produce oscillation at the crystal resonance frequency. (See ac test circuit.)

The feedback signal from the crystal is split in a lead-lag network to pins 1 and 18, respectively, to generate the subcarrier reference signals for the chroma modulators. The R-Y modulator consists of multiplier devices Q29, Q30 and Q21–Q24, while the B-Y modulator consists of Q31, Q32 and Q25–Q28. The multiplier outputs are coupled through a balanced summing amplifier Q37, Q38 to the input of the RF modulators at pin 13. With 0 offset at the lower pairs of the multipliers, no chroma output is produced. However, when either pin 2 or pin 4 is offset relative to pin 3 a subcarrier output current of the appropriate phase is produced at pin 13.

The channel B oscillator consists of devices Q56

Figure 8 **Circuit diagram**



and Q57 cross-coupled through level-shift zener diodes Q54 and Q55. A current regulator consisting of devices Q39–Q43 is used to achieve good RF frequency stability over supply and temperature.

The channel B modulator consists of multiplier devices Q58, Q59 and Q50–Q53. The top quad is coupled to the channel B tank through isolating devices Q48 and Q49. A dc offset between pins 12 and 13 offsets the lower pair to produce an output RF carrier at pin 10. That carrier is then modulated by both the chroma signal at pin 13 and the video and sound carrier signals at pin 12. The channel A modulator shares pin 12 and 13 buffers Q45 and Q44 with channel B and operates in an identical manner.

The current flowing through channel B oscillator diodes Q54, Q55 is turned around in Q60, Q61 and Q62 to source current for the channel B RF modulator. In the same manner, the channel A oscillator Q71–Q74 uses turn around Q77, Q78 and Q79 to source the channel A modulator. One oscillator at a time may be activated by connecting its tank to supply (see ac test circuit). The corresponding modulator is then activated by its current turn-around, and the other oscillator/modulator combination remains 'OFF'.

Applications information

Chroma oscillator

The oscillator is a crystal-controlled design to ensure the accuracy and stability required of the subcarrier frequency for use with television receivers. Lag-lead networks (R2C2 and C1R1) define a quadrature phase relationship between pins 1 and 18 at the subcarrier frequency of 3.579545MHz. Other frequencies can be used and where high stability is not a requirement, the crystal can be replaced with a parallel resonant L-C tank circuit – to provide a 2MHz clock, for example. Note that since one of the chrominance modulators is internally connected to the feedback path of the oscillator, operation of the oscillator at other than the correct subcarrier frequency precludes chrominance modulation.

When an external subcarrier source is available or preferred, this can be used instead. For proper modulator operation, a subcarrier amplitude of 500 mVp-p is required at pins 1 and 18. If the quadrature phase shift networks shown in the application circuit are retained, about 1 Vp-p subcarrier injected at the junction of C1 and R2 is sufficient. The crystal, C4 and R3 are eliminated and pin 17 provides a 5 Vp-p signal shifted +125° from the external reference.

Chrominance modulation

The simplest method of chroma encoding is to define the quadrature phases provided at pins 1 and 18 as the colour difference axes R-Y and B-Y. A signal at pin 2 (R-Y) will give a chrominance subcarrier output from the modulator with a relative phase of 90° compared to the subcarrier output produced by a signal at pin 4 (B-Y). The zero signal dc level of the R-Y and B-Y inputs will determine the bias level required at pin 3. For example, a pin 2 signal that is 1V positive with respect to pin 3 will give 0.6 Vp-p subcarrier at a relative phase of 90°. If pin 2 is 1V negative with respect to pin 3, the output is again 0.6 Vp-p, but with a relative phase of 270°. When a simultaneous signal exists at pin 4, the subcarrier output level and phase will be the vector sum of the quadrature components produced by pin 2 and 4 inputs. Clearly, with the modulation axes defined as above, a negative pulse on pin 4 during the burst gate period will produce the chrominance synchronizing 'burst' with a phase of 180°. Both colour difference signals must be dc coupled to the modulators and the zero signal dc level of both must be the same and within the common-mode range of the modulators.

The 0.6 Vp-p/V_{dc} conversion gain of the chrominance modulators is obtained with a 2kΩ resistor connected at pin 13. Larger resistor values can be used to increase the gain, but capacitance at pin 13 will reduce the bandwidth. Notice that equi-bandwidth encoding of the colour difference signal as is implied as both modulator outputs are internally connected and summed into the same load resistor.

Sound oscillator

Frequency modulation is achieved by using a 4.5MHz tank circuit and deviating the centre frequency via a capacitor or a varactor diode. Switching a 5pF capacitor to ground at an audio frequency rate will cause a 50kHz deviation from 4.5MHz this method is very effective in producing single frequency audio bleeps. A 1N5447 diode biassed –4V from pin 16 will give ±20kHz deviation with a 1Vp-p audio signal. The coupling network to the video modulator input and the varactor diode bias must be included when the tank circuit is tuned to centre frequency.

A good level for the RF sound-carrier is between 2% of the picture carrier level. For example, if the peak video signal offset of pin 12 with respect to pin 13 is 3V, this corresponds to a 30mVrms picture RF carrier. The source impedance at pin 12 is defined by the external 2kΩ resistor and so a series network at 15kΩ and 24pF will give a sound carrier level at –32 dB to the picture carrier.

RF Modulation

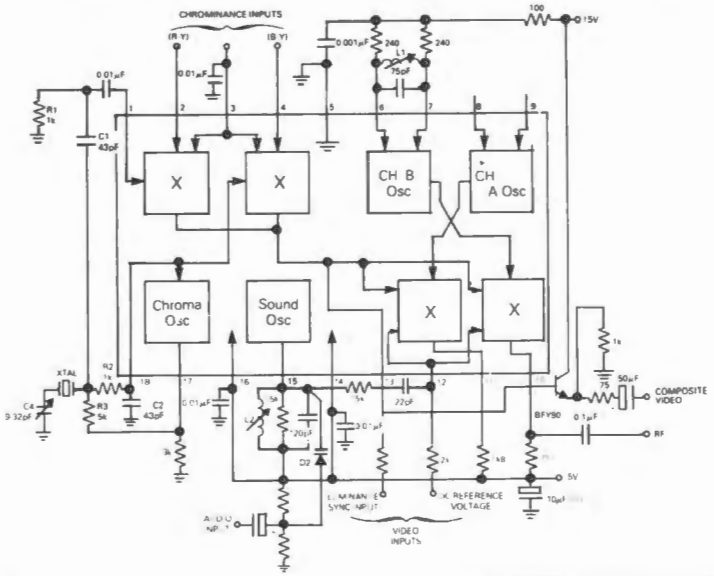
Two RF channels are available, with carrier frequencies up to 100MHz being determined by L-C tank circuits at pins 6, 7, 8 and 9. The signal inputs (pins 12, 13) to both modulators are common, but removing the power supply from an RF oscillator tank circuit will also disable that modulator.

As with the chrominance modulators, it is the offset between the two signal input pins that determines the level of RF carrier output. Since one signal input (pin 13) is also internally connected to the chrominance modulators, the 2kΩ load resistor at this point should be connected to a bias source within the common-mode input range of the video modulators. However, this bias source is independent of the chominance modulator bias and where chrominance modulation is not used, the 2kΩ resistor is eliminated and the bias source connected directly to pin 13.

To preserve the dc content of the video signal, amplitude modulation of the RF carrier is done in one direction only, with increasing video (toward peak white) decreasing the carrier level. This means the active composite video signal at pin 12 must be offset with respect to pin 13 and the sync pulse should produce the largest offset (i.e., the offset voltage of pin 12 with respect to pin 13 should have the same polarity as the sync pulses).

The largest video signal (peak white) should not be able to suppress the carrier completely, particularly if sound transmission is needed. For example, a signal with 1V sync amplitude and 2.5V peak white (3.5Vp-p – negative polarity sync) and a black level at 5 V_{dc} will require a dc bias of 8V on pin 13 for correct modulation. A simple way of obtaining the required offset is to bias pin 13 at 4 x (sync amplitude) from the sync tip level at pin 12.

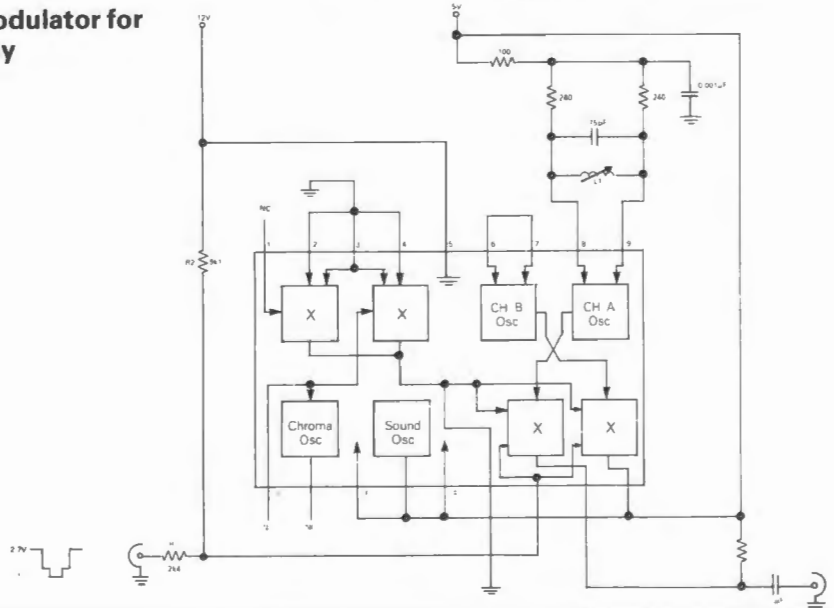
Figure 9 **Luminance and chrominance encoding composite video or RF output**



Split power supplies

The RS1889 is designed to operate over a wide range of supply voltages so that much of the time it can utilise the signal source power supplies. An example of this is shown in Figure 10 where the composite video signal from a character generator is modulated onto an RF carrier for display on a conventional home TV receiver. The RS1889 is biased between the –12V and +5V supplies and pin 13 is put at ground. A 9.1kΩ resistor from pin 12 to –12V dc offsets the video input signal (which has sync tips at ground) to establish the proper modulation depth – R1/R2 = V_{IN}/12 x 0.875. This design is for monochrome transmission and features an extremely low external parts count.

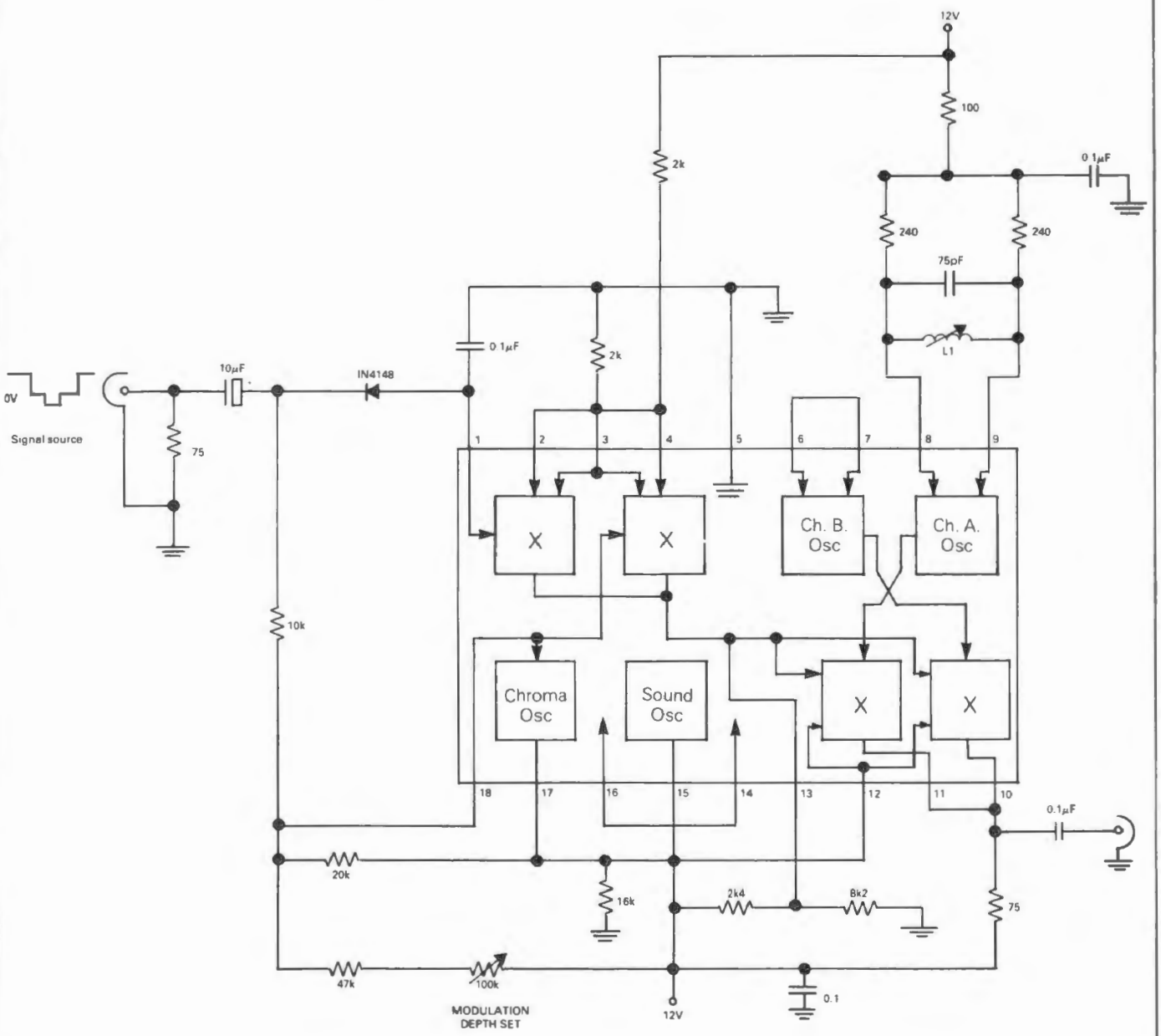
Figure 10 **Low cost monochrome modulator for character generator display**



DC Clamped inputs

Utilising a DC clamp will make matching the RS1889 to available signal generator outputs a simple process. Figure 11 shows the RS1889 configured to accept the composite video patterns available from a generator that has black level at ground and negative polarity syncs. In this application, the chroma oscillator amplifier is used to provide a gain of two. The 100k pot adjusts the overall DC level of the amplified signal which determines the modulation depth of the RF output. Clamping the input requires a minimum of DC correction to obtain the correct DC output 1evel. This allows the adjustment to be a high impedance that will have minimum effect on the amplifier closed loop gain.

Figure 11 **DC Clamped generator for NTSC pattern generators**



RS data

PAL and UHF operation

The LM1889 was originally devised for use with NTSC colour coding at VHF frequencies in the USA. However, this versatile i.c. is suitable for PAL colour encoding and can provide a UHF signal when used in conjunction with a basic frequency changer. It has become a popular choice with major home computer and video game manufacturers.

The PAL colour system is based on the NTSC system but one of the two chrominance signals, the R-Y signal, is reversed in phase for each alternate scanning lines. (Phase Alternating Lines.) A version of this modification to the NTSC system, known as system 1, is the UK colour television standard, where the sound sub carrier is spaced at 6MHz and the chroma carrier at 4.433619MHz. Phase alternation of the R-Y signal must be carried out before the R-Y input.

To provide a UHF output a basic frequency changer may be used. It can be shown that if the VHF output from the LM1889 is mixed with a UHF carrier that is much larger than the VHF signal, rectification of the combined waveform will give a signal at the difference frequency, with an amplitude directly proportional to the amplitude of the VHF signal. The modulation present at the VHF output will appear on the UHF carrier with the correct modulation characteristics of a TV broadcast carrier.

A suitable arrangement for superimposition is shown in Figure 12. The modulated signal E is used as a low impedance source driving the rectifier diode D. The carrier signal is superimposed by looping the anode lead of the diode into a cavity containing the UHF oscillator. Another method would be to form coupling loops by printed circuit board tracks (Figure 13). The output is taken across the inductor which also filters the original signal frequency to ground.

Figure 12 **Signal and carrier superimposition**

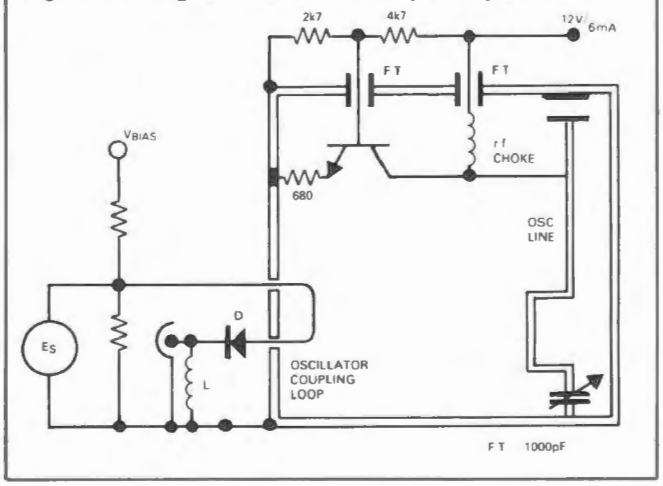
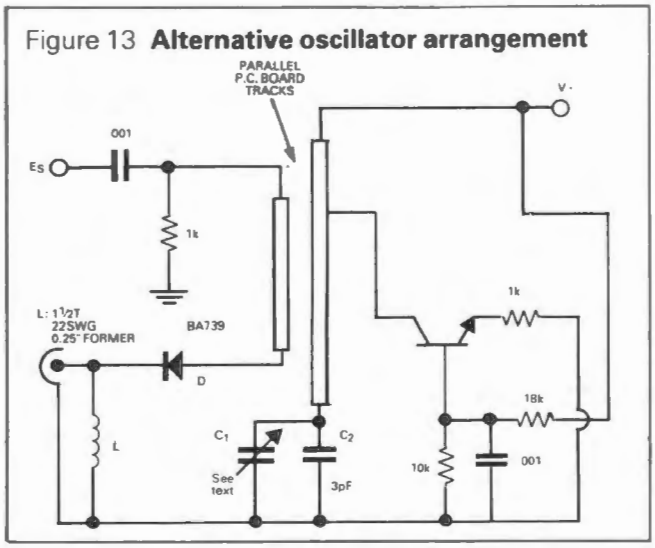


Figure 13 **Alternative oscillator arrangement**



Because of the plumbing nature of the UHF oscillator and the coupling link, it is difficult to specify component values as they will be substantially affected by the method of construction and component layout.

In Conclusion

The LM1889 can be operated in the standard VHF mode or used to supply composite video. In either case, superimposition on a UHF carrier followed by rectification will give a modulated UHF carrier. Using the LM1889 in the VHF mode will ensure that the proper modulation depth characteristic is obtained. If the composite video output is used extreme care must be taken to modulate correctly, or compressed syncs or over modulated whites can easily result. Over modulation of the peak whites will cause an unpleasant contrast ratio and a loss of fine detail. The UHF converter should be designed to ensure that the overall output level is at least 1mV so that a noise free signal will be displayed on the receiver. To allow for coupling losses a 2 to 4mV level is recommended.

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RS data

8-bit A to D converter ZN448

Stock number 301-729

General operation

The ZN448 is a successive approximation analogue to digital converter designed for easy interface to microprocessor and digital systems. The converter is designed as a single chip unit with an on-chip clock generator and 2.5V bandgap reference.

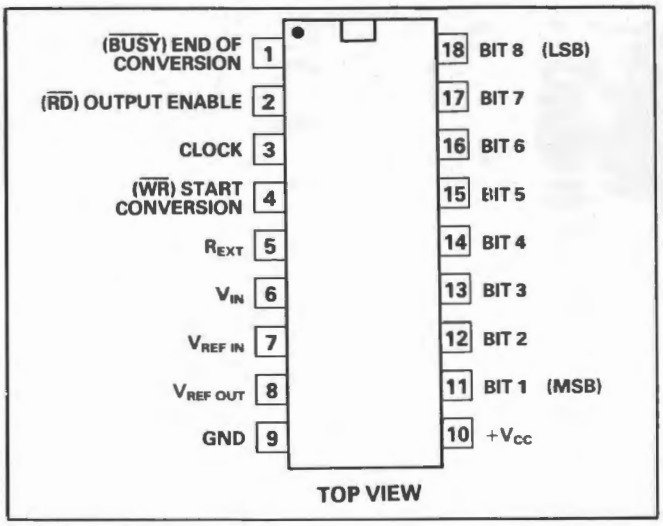
The converter only requires an external reference resistor and capacitor, clock resistor and capacitor and input resistors for operation.

Absolute maximum ratings

Supply voltage ..... +7.0V
Max. voltage logic and V_{REF} inputs ..... V_{CC}
Operating temperature range ..... 0°C to +70°C
Storage temperature range ..... −55°C to +125°C

Features

- Fast 9μs conversion time
- ½ LSB linearity
- On-chip clock
- Internal reference
- Unipolar or bipolar input ranges
- Microprocessor compatible



Electrical characteristics T_A = +25°C, V_{CC} = +5V, f_{CLK} = 900kHz. Unless otherwise stated.

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply voltage		4.5	5.0	5.5	V
Supply current			25	40	mA
Power consumption			125		mW
Reference input range		1		3	V
Resolution		8			bits
Linearity error				±½	LSB
Differential linearity error				±¾	LSB
Zero transition		12.0	15.0	18.0	mV
Full scale transition	V_{REF} = 2.560V	2.545	2.550	2.555	V
Linearity temp. coefficient			±3.0		ppm/°C
Differential linearity temperature coefficient			±6.0		ppm/°C
Full scale temp. coefficient			±2.5		ppm/°C
Zero temp. coefficient			±8.0		µV/°C
Comparator					
Input current	V_{IN} = +3V, R_{EXT} = 82kΩ		1		µA
Input resistance			100		kΩ
Tail current	V− = −5V	25	65	150	µA
Negative supply		−3	−5	−30	V
Input voltage		−0.5		+3.5	V
Reference					
Output voltage	R_{REF} = 390Ω	2.52	2.55	2.58	V
Slope resistance			0.5	2.0	Ω
V_{REF} Temp. coefficient			50		ppm/°C
Reference current		4		15	mA

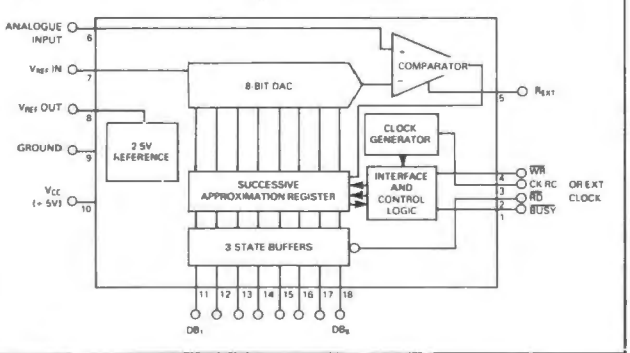
Electrical characteristics (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
Clock					
On-chip clock frequency				1	MHz
Clock frequency temp. coefficient			+0.5		%/°C
Clock resistor				2.0	kΩ
Max. external clock frequency			0.9	1	MHz
Clock pulse width		500			ns
High level input voltage		4.0			V
Low level input voltage				0.8	V
High level input current	V_{IN} = +4.0v, V_{CC} = Max.			800	μA
Low level input current	V_{IN} = +0.8V, V_{CC} = Max.			−500	μA
Convert input $\overline{WR}$					
High level voltage		2.0			V
Low level voltage				0.8	V
High level current	V_{IN} = +2.4V, V_{CC} = Max.		300		μA
Low level current	V_{IN} = +0.4V, V_{CC} = Max.		±10		μA
$\overline{RD}$ Input					
High level voltage		2.0			V
Low level voltage				0.8	V
High level current	V_{IN} = + 2.4V, V_{CC} = Max.		−150		μA
Low level current	V_{IN} = +0.4V, V_{CC} = Max.		−300		μA
High level output voltage	I_{OH} = Max, V_{CC} = Min.	2.4			V
Low level output voltage	I_{OL} = Max, V_{CC} = Min.			0.4	V
High level output current				−100	μA
Low level output current				1.6	mA
Three-state disabled output leakage	V_{OUT} = + 2.0V			2	μA
Input clamp diode voltage				−1.5	V
Enable time T_{E1}		180	210	260	ns
Enable time T_{E0}		60	80	100	ns
Disable delay time T_{D1}		80	110	140	ns
Disable delay time T_{D0}		60	80	100	ns
Convert pulse width $T_{\overline{WR}}$		200			ns
$\overline{WR}$ input to $\overline{Busy}$ output				250	ns

General circuit operation

The ZN448 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF/2}$ from the DAC. This is compared to the input voltage V_{IN}; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2} > V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$. Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the eighth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

Figure 1 **System diagrams**

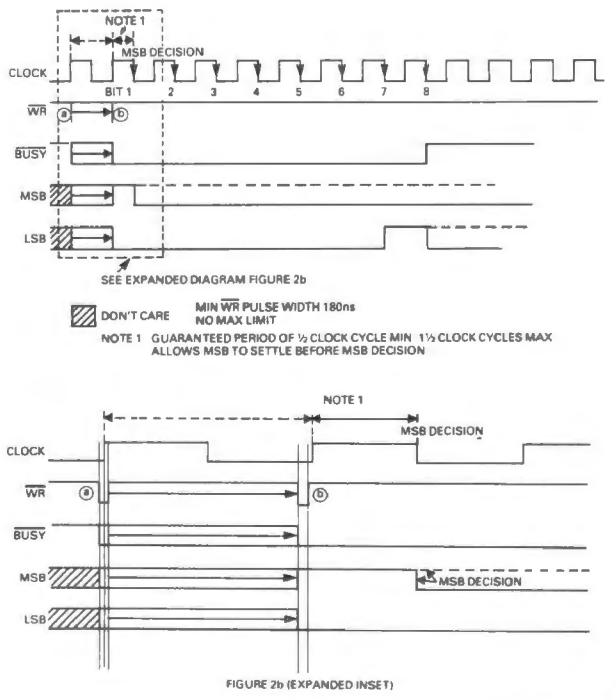


During a conversion the $\overline{RD}$ input will normally be held high to keep the 3-state buffers in their high impedance state. Data can be read out by taking $\overline{RD}$ low, thus enabling the 3-state outputs. Readout is non-destructive.

Conversion timing

The ZN448 will accept a low-going CONVERT

Figure 2 **ZN448 Timing diagrams**



pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 7½ and 8½ clock pulses later depending on the relative timing of the clock and CONVERT signals. Timing diagrams for a conversion are shown in Figure 2.

The converter is cleared by a low-going CONVERT pulse which sets the most significant bit and resets all the other bits and the $\overline{\text{BUSY}}$ flag. Whilst the CONVERT input is low the MSB output of the DAC is continuously compared with the analogue input, but otherwise the converter is inhibited.

After the CONVERT input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The CONVERT pulse can be as short as 200ns; however the MSB must be allowed to settle for at least 550ns before the MSB decision is made. To ensure that this criterion is met even with short CONVERT pulses the converter waits, after the CONVERT input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or 550ns at maximum clock frequency. The CONVERT input is not locked out during a conversion and if it is pulsed low at any time the conversion will restart.

The $\overline{\text{BUSY}}$ output goes high simultaneously with the LSB decision, at the end of a conversion indicating data valid. Note that if the three-state data outputs are enabled during a conversion the valid data will be available at the outputs after the rising edge of the $\overline{\text{BUSY}}$ signal. If, however, the outputs are not enabled until after $\overline{\text{BUSY}}$ goes high then the data will be subject to the propagation delay of the three-state buffers. (See under Data outputs.)

Continuous conversion

If a free-running conversion is required then the converter can be made to cycle by inverting the $\overline{\text{BUSY}}$ output and feeding it to the CONVERT input. To ensure that the converter starts reliably after power up an initial start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive going pulse which can be derived from a simple RC network that gives a single pulse when power is applied, as shown in Figure 3a.

The ADC will complete a conversion on every eighth clock pulse, with the $\overline{\text{BUSY}}$ output going high for a period determined by the propagation delay of the NOR gate, during which time the data can be stored in a latch. The time available for storing the data can be increased by inserting delays into the inverter path.

A timing diagram for the continuous conversion mode is shown in Figure 3b.

Figure 3a **Circuit for continuous conversion**

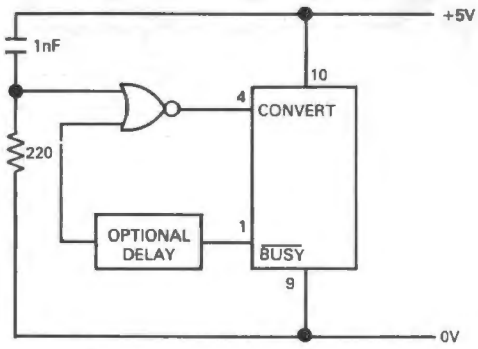
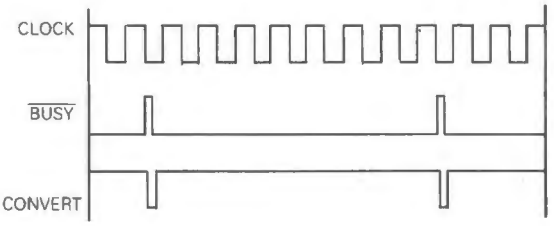


Figure 3b **Timing for continuous conversion**



As the $\overline{\text{BUSY}}$ output uses a passive pullup the rise time of this output depends on the RC time constant of the pullup resistor and load capacitance. In the continuous conversion mode the use of a 4k7 external pullup resistor is recommended to reduce the risetime and ensure that a logic 1 level is reached.

Data outputs

The data outputs are provided with 3-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Figure 4. Whilst the $\overline{\text{RD}}$ input is high both output transistors are turned off and the ZN448 presents only a high impedance load to the bus. When $\overline{\text{RD}}$ is low the data outputs will assume the logic states present at the outputs of the successive approximation register.

A test circuit and timing diagram for the output enable/disable delays are given in Figure 5.

Figure 4 **Data output**

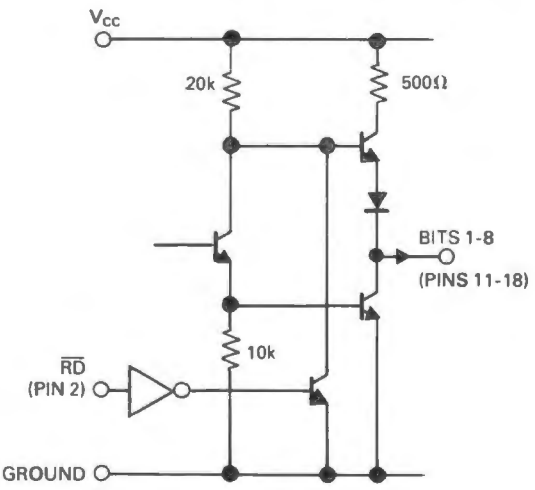
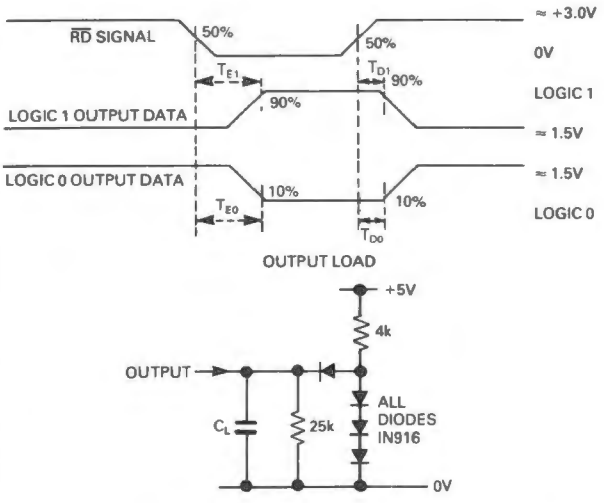


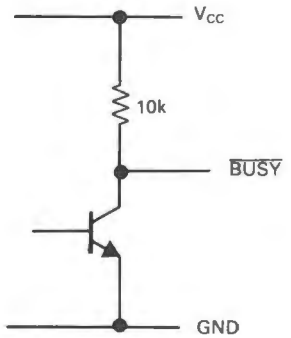
Figure 5 **Output enable/disable delays**



BUSY output

The BUSY output, shown in Figure 6, utilises a passive pullup for CMOS/TTL compatability. This also allows up to four BUSY outputs to be wire-ANDed together to form a common interrupt line.

Figure 6 **BUSY output**



On-chip clock

The on-chip clock operates with only a single external capacitor connected between pin 3 and ground as shown in Figure 7a. A graph of typical oscillator frequency versus capacitance is given in Figure 8. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor, as shown in Figure 7b. For optimum accuracy and stability of the oscillator frequency without trimming the use of a crystal or ceramic resonator is recommended, as shown in Figure 7c. The final option is to overdrive the oscillator input with an external clock signal from a TTL or CMOS gate, as shown in Figure 7d.

Figure7 **Clock circuit external components**

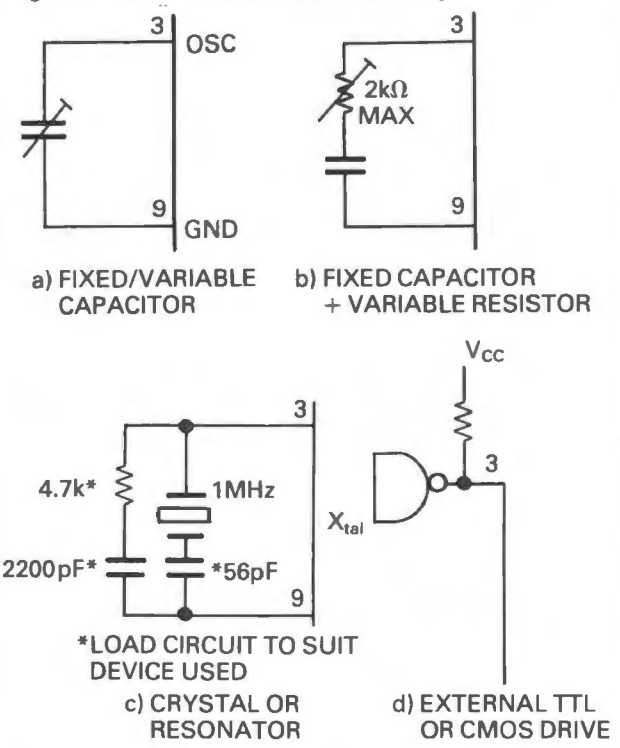
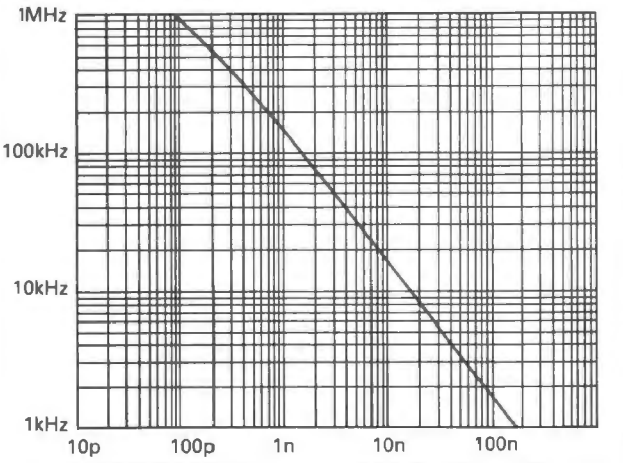


Figure 8 **Typical clock frequency vs. C_{CR} (R_{CK} = 0)**



Analogue circuits converter

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Figure 9. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt).

A binary weighted voltage is produced at the output of the R-2R ladder:

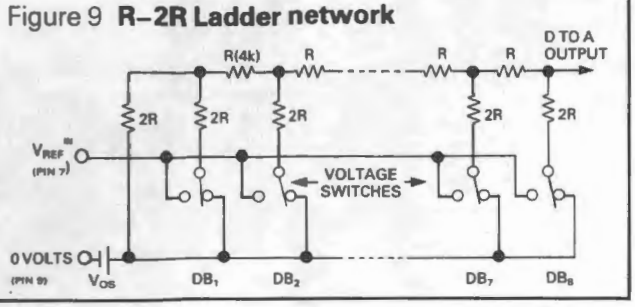
$$\text{D to A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8 μV/°C) the effect on accuracy will be negligible.

The D to A output range can be considered to be 0 – $V_{REF\ IN}$ through an output resistance R (4k).

Figure 9 **R–2R Ladder network**



Reference

Internal Reference

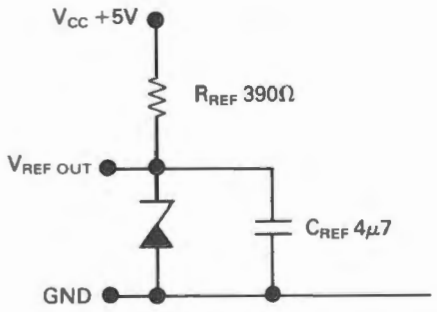
This is an active bandgap type which is equivalent to a 2.5V Zener diode with a very low slope impedance see Figure 10. To operate this reference a resistor should be connected between pins 8 and 10, the recommended value of 390Ω gives a reference current of

$$\frac{5.0-2.5}{390} = 6.4\text{mA}$$

Also a stabilizing/decoupling capacitor C_{REF} is required between pins 8 and 9 and pin 8 $V_{REF\ OUT}$ is connected to pin 7 $V_{REF\ IN}$.

Alternatively an external voltage reference may be used. This should be between +1.5V and +3.0V with a slope impedance of less than $\frac{2.5}{n}$ where n is the number of converters supplied.

Figure 10 **Internal voltage reference**



Ratiometric operation

If the output from a transducer varies with its supply then an external reference for the ZN448 should be derived from the same supply. The external reference can vary from +1.5 volts to +3.0 volts. The ZN448 will operate if $V_{REF\ IN}$ is less than +1.5 volts but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

Comparator

The ZN448 contains a fast comparator, the equivalent input circuit of which is shown in Figure 11. A negative supply voltage is required to supply the tail current of the comparator. However as this is only 25 to 150μA and need not be well stabilized it can be supplied by a simple diode pump circuit driven from the $\overline{\text{BUSY}}$ output.

Figure 11 **Comparator equivalent circuit**

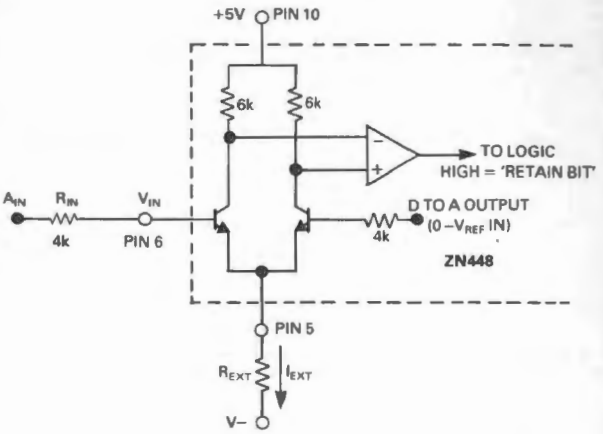
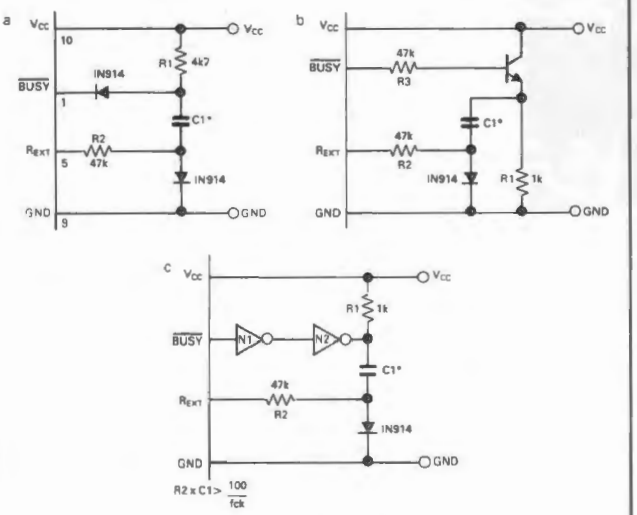


Figure 12 **Diode pump circuits to supply comparator tail current**



Several suitable circuits are shown in Figure 12. The principle of operation is the same in each case. Whilst the $\overline{\text{BUSY}}$ output is high, capacitor C1 is charged to about 4 – 4.5 volts. During a conversion the $\overline{\text{BUSY}}$ output goes low and the upper end of C1 is thus also pulled low. The lower end of C1 therefore applies about –4V to R2, thus providing the tail current for the comparator. The time constant R2. C1 is chosen according to the clock frequency so that droop of the capacitor voltage is not significant during a conversion.

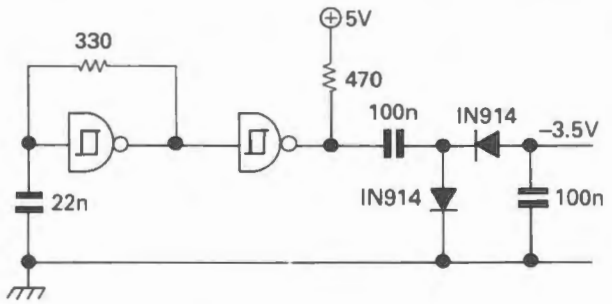
The constraint on using this type of circuit is that C1 must be recharged whilst the $\overline{\text{BUSY}}$ output is high. If the $\overline{\text{BUSY}}$ output is high for greater than one converter clock period then the circuit of Figure 12a will suffice. If this is not the case, for example, in the continuous conversion mode, then the circuits of Figures 12b and 12c are recommended, since these can pump more current into the capacitor.

Where several ZN448s are used in a system the self-oscillating diode pump circuit of Figure 13 is recommended. Alternatively, if a negative supply is available in the system then this may be utilised. A list of suitable resistor values for different supply voltages is given in Table 1.

TABLE 1

V– (Volts)	R_{EXT}(kΩ)
3	47
5	82
10	150
12	180
15	220
20	330
25	390
30	470

Figure 13 **Diode pump circuit to supply comparator tail current for up to five ZN448s**

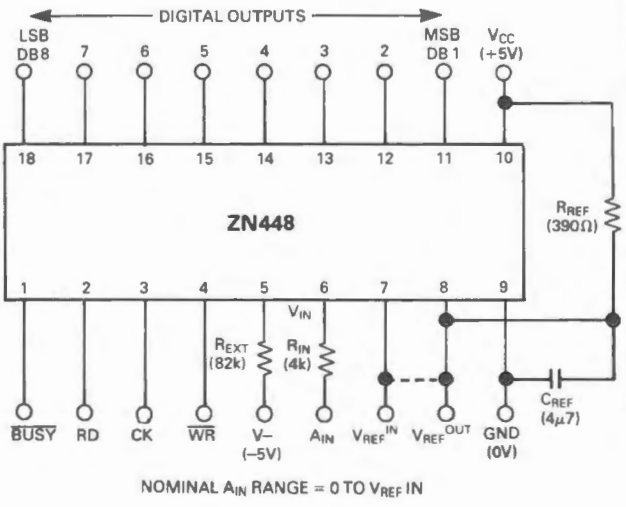


Analogue input ranges

The basic connection of the ZN448 shown in Figure 14 has an analogue input range 0 to $V_{REF\ IN}$ which, in some applications, may be made available from previous signal conditioning/scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by offsetting the analogue input range so that the comparator always sees a positive input voltage.

Figure 14 **External components for basic operation**



Unipolar operation

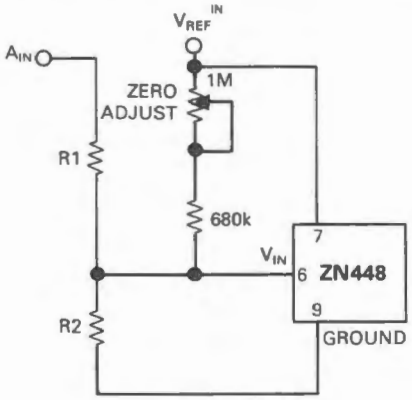
The general connection for unipolar operation is shown in Figure 15.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input (A_{IN}) is at full scale.

The resulting full scale range is given by: A_{IN} FS $= (1 + \frac{R1}{R_2}), V_{REF\ IN} = G. V_{REF\ IN}$.

To match the ladder resistance R1/R2 (R_{IN}) = 4k.

Figure 15 **General unipolar input connections**



The required nominal values of R_1 and R_2 are given by $R_1 = 4G$ k, $R_2 = \frac{4G}{G-1}$ k.

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

Input range	G	R_1	R_2
+5V	2	8k	8k
+10V	4	16k	5.33k

Gain adjustment

Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ± 5% of its nominal value is suggested.

Zero adjustments

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which corresponds to 1½ LSB with a 2.56 volt reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of + ½LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1½ times $V_{REF\ IN}$.

Practical circuit values for +5V and +10V input ranges are given in Figure 16 which incorporates both zero and gain adjustments.

Figure 16 **Unipolar operation component values**

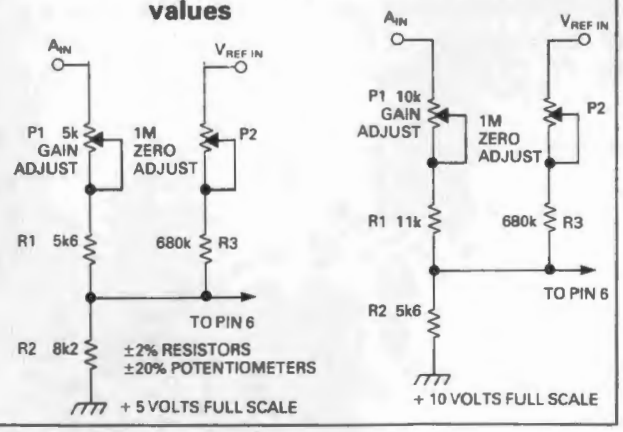
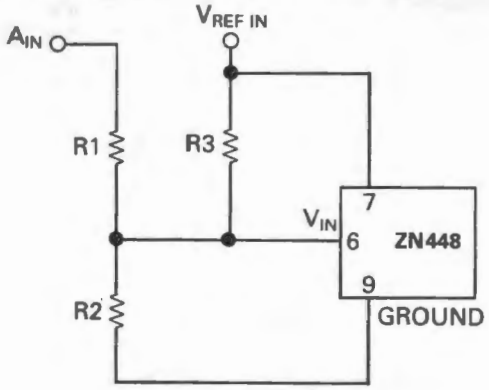


Figure 17 **Basic bipolar input connection**



Unipolar adjustment procedure

(i) Apply continuous convert pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply full scale minus 1½ LSB to A_{IN} and adjust gain until Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply ½ LSB to A_{IN} and adjust zero until Bit 8 just flickers between 0 and 1 with all other bits at 0.

Unipolar setting-up points

Input range, +FS	½ LSB	FS – 1½ LSB
+ 5V	9.8mV	4.9707 volts
+ 10V	19.5mV	9.9414 volts

$1\ LSB = \frac{FS}{256}$

Unipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (Binary)
FS – 1 LSB	11111111
FS – 2 LSB	11111110
¾ FS	11000000
½ FS + 1 LSB	10000001
½ FS	10000000
½ FS – 1 LSB	01111111
¼ FS	01000000
1 LSB	00000001
0	00000000

Bipolar operation

For bipolar operation the input to the ZN448 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Figure 17).

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full scale range is ± G. $V_{REF\ IN}$ then $R_1 = (G - 1)$. R_2 and $R_1 = G.R_3$ fulfil the required conditions.

To match the ladder resistance $R_1/R_2/R_3$ (= R_{IN}) = 4k.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8\ Gk$, $R_2 = 8G/(G-1)k$, $R_3 = 8k$.

A bipolar range of ± $V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) results if $R_1 = R_3 = 8k$ and $R_2 = \infty$.

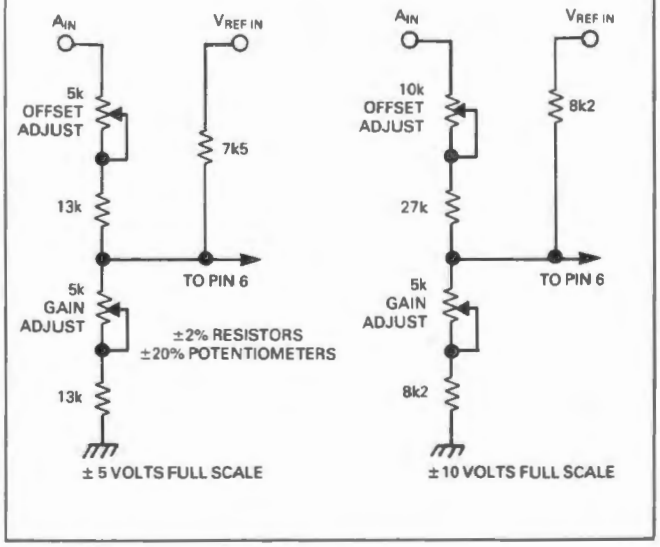
Assuming the $V_{REF\ IN}$ = 2.5 volts the nominal values of resistors for ± 5V and ±10V input ranges are given in the following table.

Input range	G	R_1	R_2	R_3
±5V	2	16k	16k	8k
±10V	4	32k	10.66k	8k

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Figure 18.

Figure 18 **Bipolar operation – component values**



RS data

Note that in the ± 5V case R_3 has been chosen as 7.5k (instead of 8.2k) to obtain a more symmetrical range of adjustment using standard potentiometers.

Bipolar adjustment procedure

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply – (FS – ½ LSB) to A_{IN} and adjust offset until the Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply + (FS – 1½ LSB) to A_{IN} and adjust gain until Bit 8 just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

Bipolar setting-up points

Input range, +FS	– (FS – ½ LSB	+ (FS – 1½ LSB)
+ 5V	–4.9805V	+4.9414V
±10V	–9.9609V	+9.8828V

$1\ LSB = \frac{FS}{256}$

Bipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (Offset binary)
+ (FS – 1 LSB)	11111111
+ (FS – 2 LSB)	11111110
+ ½ FS	11000000
+ 1 LSB	10000001
0	10000000
– 1 LSB	01111111
– ½ FS	01000000
– (FS – 1 LSB)	00000001
– FS	00000000

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RS data

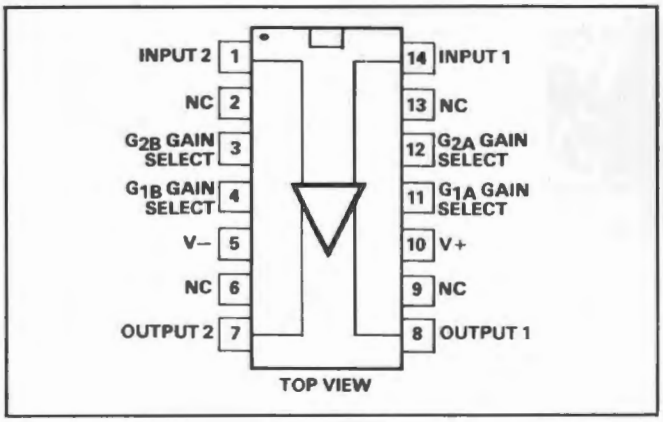
Video amplifier NE592

Stock number 301-583

The RS NE592 is a monolithic, two stage differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

Features

- 120MHz bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components



Absolute maximum ratings

Supply voltage	±8V
Differential input voltage	±5V
Common mode input voltage	±6V
Output current	10mA
Operating temperature range	0 to +70°C
Storage temperature range	–60 to +150°C
Power dissipation	500mW

DC Electrical characteristics

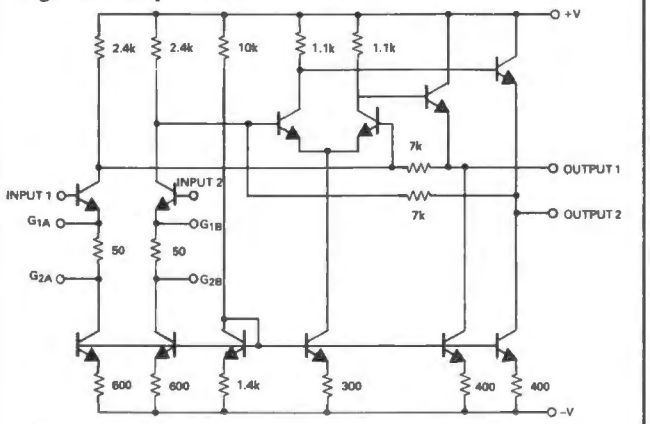
$T_A = +25°C, V_S = \pm 6V, V_{CM} = 0$ unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$

Parameter	Symbol	Test conditions	NE592			Unit
			Min.	Typ.	Max.	
Differential Voltage Gain Gain 1 (Note 1) Gain 2 (Note 2)	A_{VOL}	$R_L = 2k\Omega$, $V_{OUT} = 3Vp\text{-}p$	 250 80	 400 100	 600 120	V/V
Bandwidth Gain 1(Note 1) Gain 2 (Note 2)	BW			 40 90		MHz
Rise Time Gain 1 (Note 1) Gain 2 (Note 2)	t_r	$V_{OUT} = 1Vp\text{-}p$		 10.5 4.5	 12	ns
Propagation Delay Gain 1 (Note 1) Gain 2 (Note 2)	t_d	$V_{OUT} = 1Vp\text{-}p$		 7.5 6.0	 10	ns
Input Resistance Gain 1 (Note 1) Gain 2 (Note 2)	R_{IN}		 10	 4.0 30	 	kΩ
Input Capacitance (Note 2)	C_{IN}	Gain 2		2.0		pF
Input Offset Current	I_{OS}			0.4	5.0	μA
Input Bias Current	I_{BIAS}			9.0	30	μA
Input Noise Voltage	$\overline{e_n}$	BW = 1kHz to 10MHz		12		μVrms

Parameter	Symbol	Test conditions	NE592			Unit
			Min.	Typ.	Max.	
Input Voltage Range	ΔV_{IN}				±1.0	V
Common Mode Rejection Ratio Gain 2 (Note 2) Gain 2 (Note 2)	CMRR	 V_{CM} ± 1V, F < 100kHz V_{CM} ± 1V, F = 5MHz	 60	 86 60		dB
Supply Voltage Rejection Ratio Gain 2 (Note 2)	PSRR	 ΔV_S = ±0.5V	 50	 70		dB
Output Offset Voltage Gain 2 (Note 2)	V_{OOS}	 $R_L = \infty$		 0.35	 0.75	V
Output Common-Mode Voltage	V_{OCM}	$R_L = \infty$	2.4	2.9	3.4	V
Output Voltage Swing Differential	± V_O	R_L = 2kΩ	3.0	4.0		V
Output Resistance	R_O			20		Ω
Power Supply Current	I^+	$R_L = \infty$		18	24	mA

Note 1: Gain select pins G_{1A} and G_{1B} connected together.
Note 2: Gain select pins G_{2A} and G_{2B} connected together.

Figure 1 **Equivalent circuit**



Note: Resistor values nominal only.

Typical performance characteristics

Figure 2 **Voltage gain as a function of supply voltage**

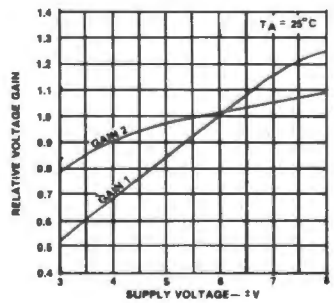


Figure 3 **Supply current as a function of supply voltage**

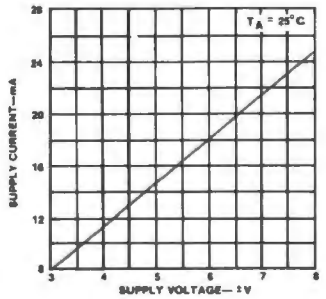


Figure 4 **Output voltage and current swing as a function of supply voltage**

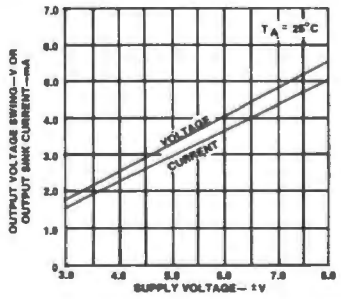


Figure 5 **Output voltage swing as a function of load resistance**

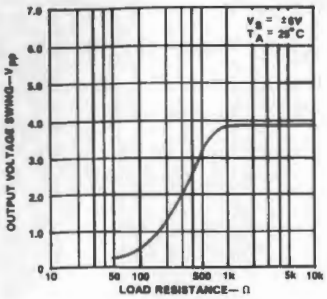


Figure 6 **Phase shift as a function of frequency**

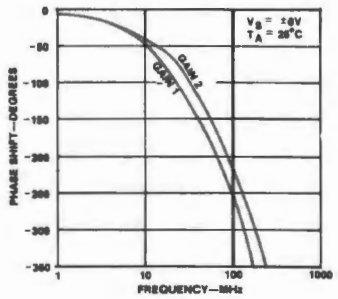


Figure 7 **Voltage gain as a function of frequency**

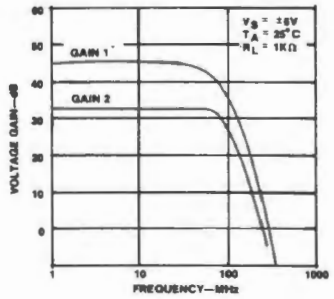
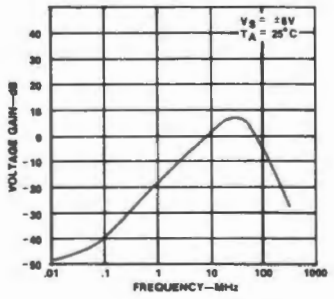
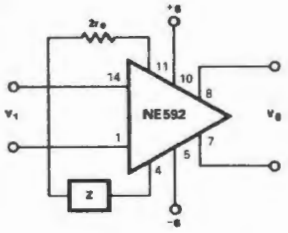


Figure 8 **Voltage gain as a function of frequency (all gain select pins open)**



Typical applications

Figure 9 **Filter networks**



$$\frac{V_0(s)}{V_1(s)} \simeq \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

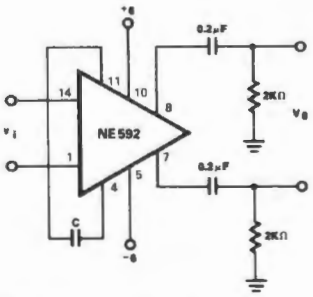
$$\simeq \frac{1.4 \times 10^4}{Z(s) + 32}$$

BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$\frac{V_o(s)}{V_i(s)}$ TRANSFER FUNCTION
R, L	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
R, C	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
R, L, C	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\,s + 1/LC}\right]$
R, L, C	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

Note: In the networks above, the R value used is assumed to include the internal $2r_e$ of approximately 32Ω.

Figure 10 **Differentiation with high common mode rejection**

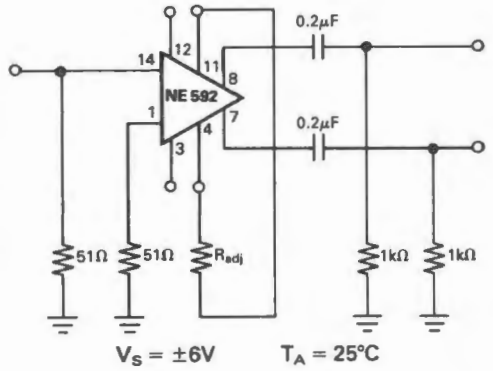


FOR FREQUENCY $F_1 \ll 1/2\pi(32)C$

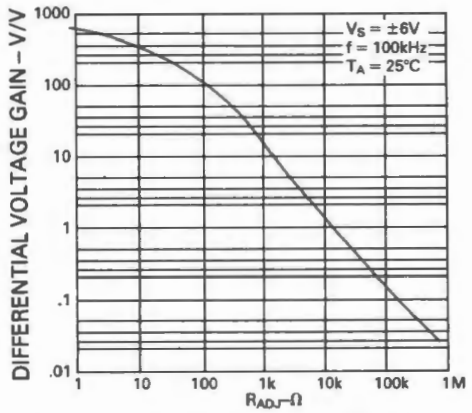
$V_0 \approx 1.4 \times 10^4 C \frac{dVi}{dT}$

RS data

Figure 11 **Voltage gain adjust circuit**



Voltage gain as a function of R_{adj}



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RS data

Trimmable voltage reference i.c.'s ZN REF

A range of five precision voltage references providing voltages from 2.5V to 10V. Featuring an initial tolerance of 1%, each device may be trimmed to an exact voltage by the use of an additional preset potentiometer. The references feature a knee current of 150μA and operate over a wide temperature range.

Features

- Trimmable output
- Excellent temperature stability
- Low output noise figure
- Low dynamic impedance
- 1% initial voltage tolerance

Absolute maximum ratings

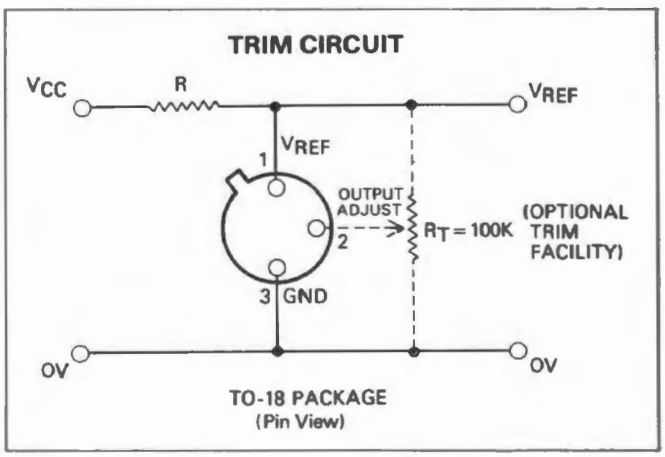
	ZN REF 025	ZN REF 040	ZN REF 050	ZN REF 062	ZN REF 100	Units
Reference current	10	75(a)	60(b)	50(c)	50(d)	mA
Power dissipation	300	300	300	300	500	mW
Operating temperature range	0 to +70	0 to +70	0 to +70	0 to +70	0 to +70	°C
Storage temperature range	–55 to +175	–55 to +175	–55 to +175	–55 to +175	–55 to +175	°C
Lead temperature (soldering 10 seconds)	300	300	300	300	300	°C

(a) Above 25°C this figure should be linearly derated to 52mA at +70°C
(b) Above 25°C this figure should be linearly derated to 42mA at +70°C
(c) Above 25°C this figure should be linearly derated to 34mA at +70°C
(d) Above 25°C this figure should be linearly derated to 34mA at +70°C

ZN REF 025 (283-514)

Temperature dependant electrical characteristics

Parameter	Symbol	Min.	Max.	Units
Output voltage change over operating temperature range (see note 1)	ΔV_{OT}	2.7	8.8	mV
Output voltage temperature coefficient (see note 2)	TCV_O	15	50	ppm/°C



Electrical characteristics

T_A = 25°C and pin 2 open circuit unless otherwise stated (Load should be less than 220pF or greater than 22nF).

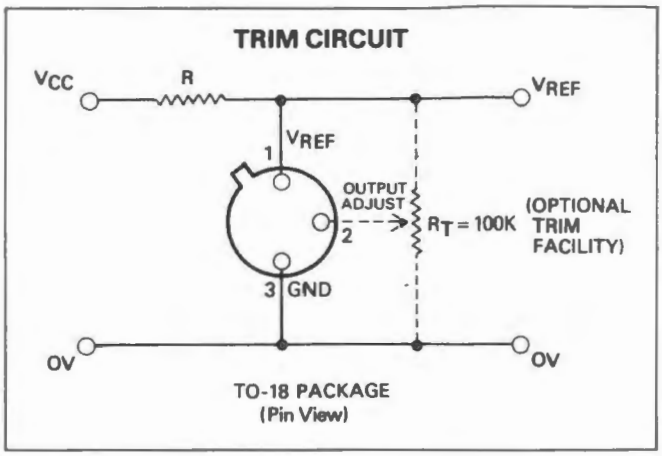
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output voltage	V_O	I_{REF} = 500μA	2.475	2.500	2.525	V
Output voltage adjustment range	V_{OR}	R_T = 100kΩ	—	±5	—	%
Change in TCV_O with output adjustment	TCV_{OR}		—	0.8	—	ppm/°C/%
Turn on or 'Knee' current	I_{ON}	Over full temperature range	—	120	150	μA
Operating current range	I_{REF}		0.15	—	10	mA
Turn on settling time to within 0.1% of V_O	t_{ON}	Overshoot typically less than 1%	—	5.0	—	μsec.
Output voltage noise (over the range 0.1Hz-10Hz)	$^{e}np\text{-}p$	Peak to peak measurement	—	50	—	μV
Dynamic impedance	R_D	I_{REF} 0.5mA-5mA See note 4 and 5	—	1.5	2.0	Ω

5314

ZN REF 040 (283-520)

Temperature dependant electrical characteristics

Parameter	Symbol	Min.	Max.	Units
Output voltage change over operating temperature range (see note 1)	ΔV_{OT}	4.2	14	mV
Output voltage temperature coefficient (see note 2)	TCV_O	15	50	ppm/°C



Electrical characteristics

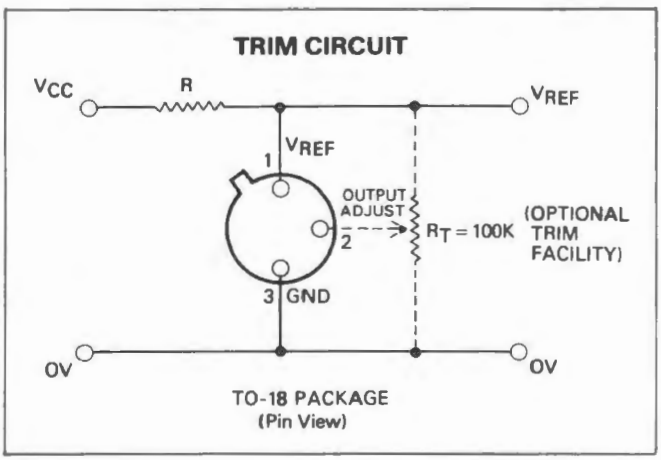
T_A = 25°C and pin 2 open circuit unless otherwise stated (Load should be less than 220pF or greater than 22nF).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output voltage	V_O	I_{REF} = 500μA	3.970	4.010	4.050	V
Output voltage adjustment range	V_{OR}	R_T = 100kΩ	—	±5	—	%
Change in TCV_O with output adjustment	TCV_{OR}		—	0.8	—	ppm/°C/%
Turn on or 'Knee' current	I_{ON}	Over full temperature range	—	120	150	μA
Operating current range	I_{REF}	See note 3	0.15	—	75	mA
Turn on settling time to within 0.1% of V_O	t_{ON}	Overshoot typically less than 1%	—	5.0	—	μsec.
Output voltage noise (over the range 0.1Hz-10Hz)	e_{np-p}	Peak to peak measurement	—	50	—	μV
Dynamic impedance	R_D	I_{REF} 0.5mA-5mA See note 4 and 5	—	2.0	3.0	Ω

ZN REF 050 (283-536)

Temperature dependant electrical characteristics

Parameter	Symbol	Min.	Max.	Units
Output voltage change over operating temperature range (see note 1)	ΔV_{OT}	5.4	17.2	mV
Output voltage temperature coefficient (see note 2)	TCV_O	15	50	ppm/°C



Electrical characteristics

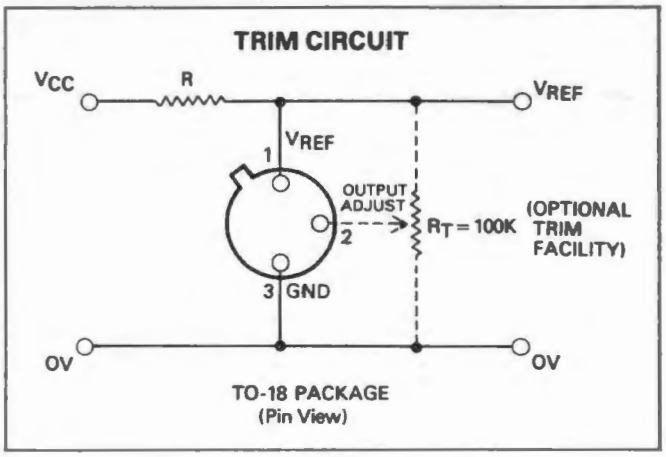
T_A = 25°C and pin 2 open circuit unless otherwise stated (Load should be less than 220pF or greater than 22nF).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output voltage	V_O	I_{REF} = 500μA	4.851	4.900	4.949	V
Output voltage adjustment range	V_{OR}	R_T = 100kΩ	—	±5	—	%
Change in TCV_O with output adjustment	TCV_{OR}		—	0.8	—	ppm/°C/%
Turn on or 'Knee' current	I_{ON}	Over full temperature range	—	120	150	μA
Operating current range	I_{REF}	See note 3	0.15	—	60	mA
Turn on settling time to within 0.1% of V_O	t_{ON}	Overshoot typically less than 1%	—	5	—	μsec.
Output voltage noise (over the range 0 1Hz-10Hz)	e_{np-p}	Peak to peak measurement	—	50	—	μV
Dynamic impedance	R_L	I_{REF} 0 5mA-5mA See note 4 and 5	—	1.5	2 0	Ω

ZN REF 062 (283-542)

Temperature dependant electrical characteristics

Parameter	Symbol	Min.	Max.	Units
Output voltage change over operating temperature range (see note 1)	ΔV_{OT}	6.5	11	mV
Output voltage temperature coefficient (see note 2)	TCV_O	15	50	ppm/°C



Electrical characteristics

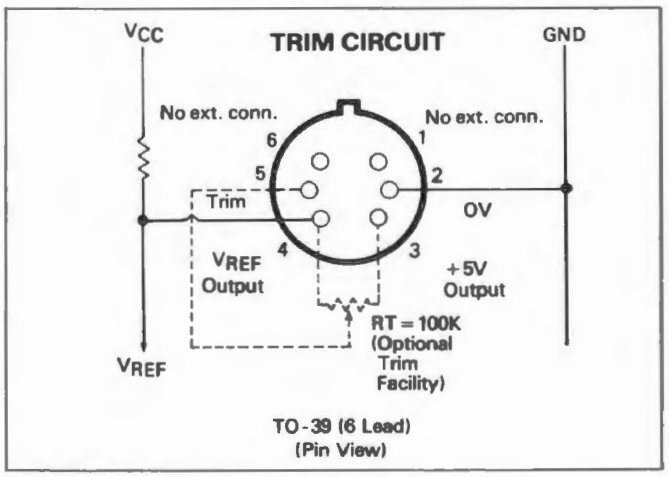
T_A = 25°C and pin 2 open circuit unless otherwise stated (Load should be less than 220pF or greater than 22nF).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output voltage	V_O	I_{REF} = 500μA	6.11	6.17	6.23	V
Output voltage adjustment range	V_{OR}	R_T = 100kΩ	—	±5	—	%
Change in TCV_O with output adjustment	TCV_{OR}		—	0.8	—	ppm/°C/%
Turn on or 'Knee' current	I_{ON}	Over full temperature range	—	120	150	μA
Operating current range	I_{REF}	See note 3	0.15	—	50	mA
Turn on settling time to within 0.1% of V_O	t_{ON}	Overshoot typically less than 1%	—	5	—	μsec.
Output voltage noise (over the range 0.1Hz-10Hz)	$^{e}np\text{-}p$	Peak to peak measurement	—	50	—	μV
Dynamic impedance	R_D	I_{REF} 0.5mA-5mA See note 4 and 5	—	2.0	3.0	Ω

ZN REF 100 (283-558)

Temperature dependant electrical characteristics

Parameter	Symbol	Min.	Max.	Units
Output voltage change over operating temperature range (see note 1)	ΔV_{OT}	10.8	34.4	mV
Output voltage temperature coefficient (see note 2)	TCV_O	15	50	ppm/°C



Electrical characteristics

T_A = 25°C and pins 3, 4 and 5 open circuit unless otherwise stated (Load should be less than 220pF or greater than 22nF).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output voltage	V_O	I_{REF} = 500μA	9.702	9.800	9.898	V
Output voltage adjustment range	V_{OR}	R_T = 100kΩ	—	±2.5	—	%
Change in TCV_O with output adjustment	TCV_{OR}		—	0.8	—	ppm/°C/%
Turn on or 'Knee' current	I_{ON}	Over full temperature range	—	120	150	μA
Operating current range	I_{REF}	See note 3	0.15	—	50	mA
Turn on settling time to within 0.1% of V_O	t_{ON}	Overshoot typically less than 1%	—	5	—	μsec.
Output voltage noise (over the range 0.1Hz-10Hz)	$^{e}np\text{-}p$	Peak to peak measurement	—	50	—	μV
Dynamic impedance	R_D	I_{REF} 0.5mA-5mA See note 4 and 5	—	3.0	4.0	Ω

RS data

Notes

1. *Output change with temperature* ($\triangle V_{ot}$) the absolute difference between the maximum output voltage and the minimum output voltage over the operating temperature range
$$V_{OT} = V_{max} - V_{min}$$
2. *Output temperature coefficient* (TCV_o)
The ratio of the output voltage change with temperature to the operating temperature range expressed in ppm/°C/%.
$$TCV_o = \frac{V_{OT} \times 10^6}{V_O \times \triangle T} \text{ ppm/°C/\%}$$
$\triangle T$ = Full temperature change.
3. *Operating current* (I_{REF})
Maximum operating current must be derated as indicated in Maximum Ratings.
4. *Dynamic impedance* (R_D)
The dynamic impedance is defined as
$$R_D = \frac{\text{Change in } V_O \text{ over specified current range}}{\triangle I_{REF}}$$
$\triangle I_{REF} = 5 - 0.5 = 4.5$mA (typically).
5. *Line regulation* ($\triangle V_{OL}$)
The ratio of the change in output voltage to the change in input voltage producing it.
$$\triangle V_{OL} = \frac{R_D \times 100}{V_O \times R_S} \text{ \%/V}$$
R_S = Source resistance.

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RS data

660 V Switch fuses and auxiliary contacts

Two panel mounting, door interlocking, 3 pole switch fuses available in 32A (334-167) or 63A (334-173) versions suitable for use up to 660V ac. The switch fuses feature high breaking capacity, fast make and break operation and high short circuit capacity. When fitted to an enclosure the door may only be opened in the OFF position. The fuselinks are totally isolated with the switch in the OFF position which permits fuse changing in complete safety. The units use RS BS88 A2 or A3 fuses. The door mounting method provides environmental protection to IP54 and the units comply with IEC408, BS5419 and VDE0660 regulations.

Reliable position indication. If the contacts will not open (e.g. welding due to high fault current) the operating handle will not travel beyond the mid position between on and off. This prevents the door from being opened by conventional means. A qualified person would have to be consulted to clear the fault.

Up to two auxiliary contact sets (334-189) each with 1 N/O + 1 N/C contacts may be fitted, the sets are supplied complete with mounting bracket, operating cam, terminal identification and shroud.

Features

- Suitable for up to 660V ac 32A and 63A versions available.
- High breaking and short circuit capacities. Can also be closed safely in fault conditions.
- Easily replaceable standard BS88 A2 or A3 fuselinks.
- Directly accessible screw terminals requiring no shrouds or lugs.
- Easy installation, telescopic shaft enables panel fitting depth of 111 to 200mm with no measuring or cutting required.
- Lockable in the OFF position as standard, up to three padlocks may be fitted.
- Door interlocking as standard.
- Auxiliary contact block available.

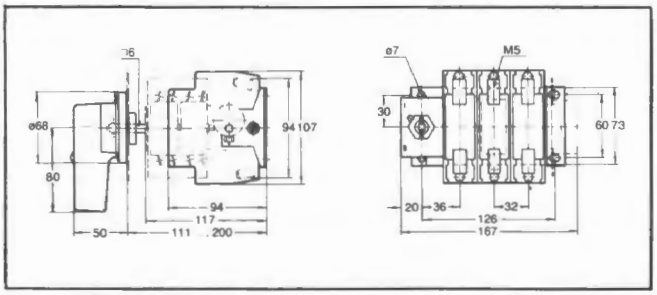
Technical specification

Parameter	32A version	63A version	Units
Number of main poles	3	3	
Maximum number of auxiliary contacts that can be added	2	2	
Rated insulation voltage	750	750	V
Rated thermal and operating current (AC22, 660V ac) @ ambient temperature 40°C in enclosure and free air (for 60°C derate 20%)	32	63	A
Rated operational current 3 phase D.O.L. motor starting and high inductive loads 415V, AC23*	32	63	A
Rated operational power 3 phase D.O.L. motor starting and high inductive loads 415V, AC23*	15	30	kW
Rated breaking capacity @ 500V ac COS Ø 0.35 @ 660V ac COS Ø 0.35	300 —	500 350	A A
Rated fused short circuit capacity and making capacity on fault level 660V RMS	50	50	kA
Rated capacitor power 415V**	15	30	kV_{Ar}

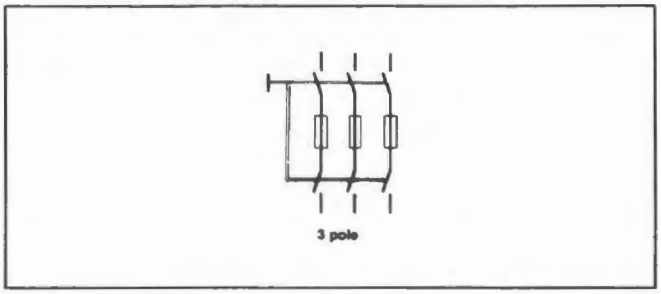
*Some fuselinks limit these figures further. Starting current characteristics must be considered separately.

**The capacity rating of the switchfuse is limited by the fuselink.

Dimensions



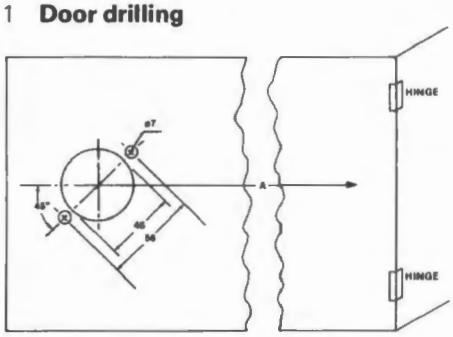
Circuit



RS data

Mounting details

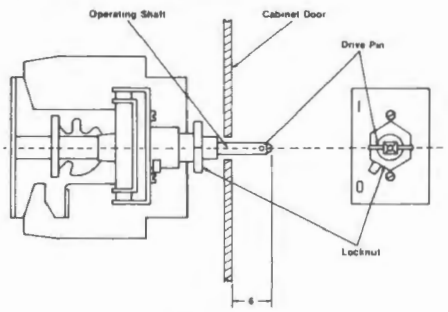
Figure 1 **Door drilling**



Measurement A – the distance between the centre of the operating shaft hole and a vertical line drawn through the hinges of the cabinet door – should not be less than 175mm.

The base switch fuse should be mounted so that the fuselinks, when fitted, are vertical and to the right (or hinge side) of the operating shaft (see Figure 1). The centre of this adjustable length shaft, looking end on, should pass through the centre of its Ø45 hole (tolerance ±3mm) and should protrude 6mm from the door face. The drive pin (see Figure 2) should be in a horizontal position with the switchfuse at OFF.

Figure 2 **Handle mechanism (side view)**



With the basic switch fuse correctly mounted and the operating shaft in the right position, carefully open the cabinet door and, with a spanner adjust to 23mm AF, turn the locknut (see Figure 2) clockwise to lock the operating shaft in position.

Attach the handle mechanism to the door so that the ON mark on the dial plate is at 12 o'clock. Close the cabinet door and settle the handle into position on the operating shaft. Tighten fixing screws on door.

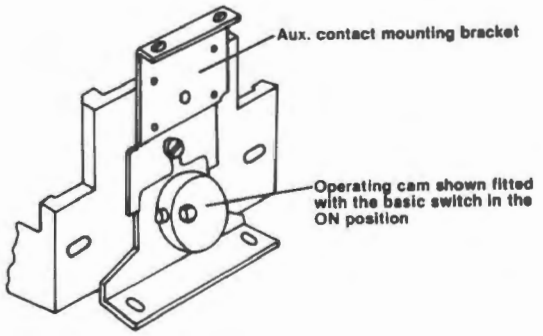
The shroud can be fitted to the switch fuse using the single screw provided. Provision is made for fitting the shroud to the handle if the switch fuse is to be used as a freestanding unit.

Fitting of auxiliary contacts (334-189)

The auxiliary contact set consists of the following:

1 Basic auxiliary contact block (IN/O + IN/C) with 2 captive mounting screws.
1 Transparent shroud and 2 M3 fixing screws.
1 Mounting bracket.
1 Operating cam with 3mm hexagon setscrews and locking nut.
1 Perspex, terminal identification label.

Figure 3 **Fitting the auxiliary contact mounting bracket**



The mounting bracket on the basic switch fuse (opposite side to the operating shaft) is secured to the moulding by 2 screws. The screw, furthest from the base, should be loosened to permit the auxiliary contact mounting bracket to be slid underneath (see Figure 3) and then tightened.

With the basic switch in the ON position, fit the operating cam, as in Figure 3, tighten the setscrew with a 3mm AF hexagon key and tighten the locking nut. The basic auxiliary contact block with its terminal identification label can now be screwed into position. The CENELEC EN50005 terminal markings should be conformed to. For 1 contact block use 13-14 N/C, 21-22 N/O. If a second contact block is required (available only as part of the complete kit) it can be fitted above the first block – terminal markings 33-34 N/C 41-42 N/O. The shroud, when finally fitted, will cover one or two auxiliary contact blocks.

Defeating the door interlock in the ON position

ONLY TO BE CARRIED OUT BY A QUALIFIED PERSON. ISOLATE MAINS FIRST. A small knockout in the switch handle at 10 o'clock (with the pointer at ON or 12 o'clock) is provided for access to the interlocking mechanism.

R.S. Components Ltd. 13-17 Epworth Street, London, EC2P 2HA Telephone: 01-250 4000
For technical enquiries ring: 01-202 8252 or 0536-201234
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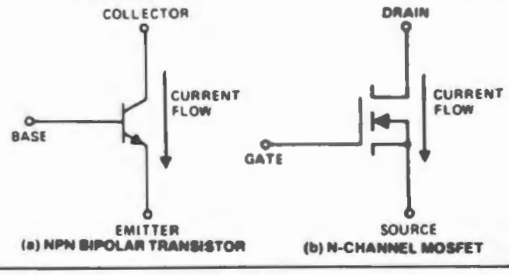
RS data

Power MOSFETs

RS power MOSFETs aid the design of advanced products by offering the superior characteristics of Field Effect Transistors at true high power levels. Power MOSFETs simplify circuitry because they are voltage-controlled devices and require only very small instantaneous currents from the signal source. They achieve switching times of less than 100 nanoseconds at high current levels. They have great ruggedness because of the absence of the second breakdown failure mechanism of bipolar transistors. In parallel operation they inherently 'current share' rather than 'current hog'. The stability of the gain and response time characteristics over a wide temperature range is outstanding.

Power MOSFETs are majority carrier semiconductor devices, and their construction and principles of operation are fundamentally different from those of traditional bipolar transistors, which are minority carrier semiconductors.

Figure 1 **Electrical symbols for bipolar and MOSFET**



MOSFET symbol and terminology

The collector, base and emitter terminology for the terminals of a bipolar transistor is replaced by drain, gate, and source, respectively for a MOSFET. Figure 1 shows the circuit symbol for an N channel MOSFET, and makes a comparison with a conventional bipolar transistor.

Electrical characteristics (at 25°C unless otherwise stated)

Type	Channel material	Case	P_T	R_{DS} (max.)	I_D (max.)	V_{DG}	V_{DS}	V_{GS} (TH) (max.)	I_{DSS} (max.)	I_{GSS} (max.)	tr, tf (max.)	gfs* (min.)
RS120	n	TO3	40W	0.3Ω	6A	100V	100V	4V	1mA	100nA	70ns	1.5S
RS130	n	TO3	75W	0.18Ω	12A	100V	100V	4V	1mA	100nA	150ns	3S
RS220	n	TO3	40W	0.8Ω	4A	200V	200V	4V	1mA	100nA	60ns	1.3S
RS330	n	TO3	75W	1.0Ω	4A	400V	400V	4V	1mA	100nA	100ns	2S
RS9130	p	TO3	75W	0.3Ω	8A	−100V	−100V	−4V	−1mA	−100nA	140ns	2S
RS510	n	TO220(AB)	20W	0.6Ω	3A	100V	100V	4V	0.5mA	500nA	25ns	1S
RS520	n	TO220(AB)	40W	0.3Ω	5A	100V	100V	4V	1mA	500nA	70ns	1.5S
RS530	n	TO220(AB)	75W	0.18Ω	10A	100V	100V	4V	1mA	500nA	150ns	3S
RS610	n	TO220(AB)	20W	1.5Ω	2A	200V	200V	4V	0.5mA	500nA	25ns	0.8S
RS630	n	TO220(AB)	75W	0.4Ω	6A	200V	200V	4V	1mA	500nA	140ns	2.5S
RS640	n	TO220(AB)	125W	0.18Ω	11A	200V	200V	4V	1mA	500nA	60ns	6S
RS720	n	TO220(AB)	40W	1.8Ω	2.5A	400V	400V	4V	1mA	500nA	50ns	1S
RS730	n	TO220(AB)	75W	1.0Ω	3.5A	400V	400V	4V	1mA	500nA	100ns	2S
RS830	n	TO220(AB)	75W	1.3Ω	3A	500V	500V	4V	1mA	500nA	80ns	1.5S
RS840	n	TO220(AB)	125W	0.85Ω	5A	500V	500V	4V	1mA	500nA	30ns	4S
RS9520	p	TO220(AB)	40W	0.6Ω	−4A	−100V	−100V	−4V	−1mA	−500nA	100ns	0.9S
RS9530	p	TO220(AB)	75W	0.3Ω	−7A	−100V	−100V	−4V	−1mA	−500nA	140ns	2S

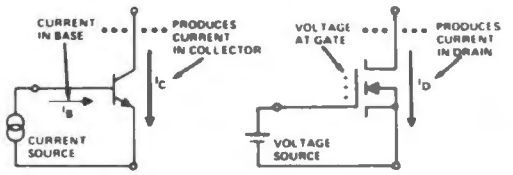
1 ms (milliSiemens) is equivalent to 1 mmho.

Driving the power MOSFET

The conventional bipolar transistor is essentially a current-driven device. As illustrated in Figure 2(a), a current must be applied between the base and emitter terminals to produce a flow of current in the collector. The amount of drive required to produce a given output depends upon the gain, but invariably a current must be made to flow into the base terminal to produce a flow of current in the collector.

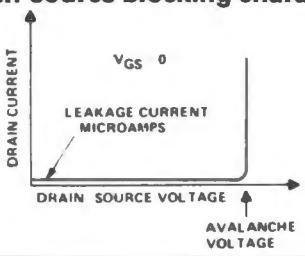
The MOSFET is fundamentally different; it is a voltage-controlled device. A voltage must be applied between the gate and source terminals to produce a flow of current in the drain, as illustrated in Figure 2(b). The gate is isolated electrically from the source by a layer of silicon oxide. Theoretically no current flows into the gate when a DC voltage is applied to it – though in practice there will be an extremely small leakage current, in the order of nanoamperes.

Figure 2 **Bipolar transistor is current-driven, MOSFET is voltage-driven**



With no voltage applied between the gate and source electrodes, the impedance between the drain and source terminals is very high, and only a small leakage current flows in the drain until the applied voltage exceeds the drain-to-source avalanche voltage. This is illustrated in Figure 3.

Figure 3 **Drain-source blocking characteristic**



When a voltage is applied between the gate and source terminals, an electric field is set up within the MOSFET. This field modulates the resistance between the drain and source terminals, and permits a current to flow in the drain in response to the applied drain circuit voltage. The amount of current that flows depends upon the amount of voltage applied to the gate, assuming that the impedance of the external drain circuit is not limiting.

Because the gate draws only a minute DC leakage current, the DC current gain is extremely high, typically in the order of 10^9. In fact, this is a rather meaningless parameter for a power MOSFET, and it is not normally used. Because a flow of *current* in the drain is produced essentially by a *voltage* applied to the gate, a more useful parameter for the MOSFET is the *transconductance*. This is the change of drain current brought about by a 1 volt change of gate voltage.

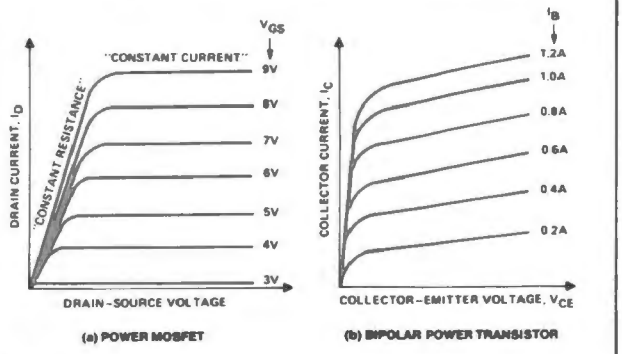
The extremely low drive current requirement of the power MOSFET, and the associated extremely high power gain, are a major advantage over the conventional bipolar transistor or Darlington. **This feature will often make it possible to drive the power MOSFET directly from CMOS or TTL integrated circuit logic.**

The static operating characteristics

The fundamental drain-source operating characteristics of the power MOSFET are illustrated in Figure 4(a). For comparison, Figure 4(b) shows the corresponding collector-emitter characteristics for a conventional bipolar transistor.

For any given value of gate voltage there are essentially two clearly separate regions on the drain current-voltage characteristic (with an intermediate zone that connects the two). The first is a 'constant resistance' region. As the drain-to-source voltage is increased, the current increases almost proportionately, though in practice the resistance does increase at higher currents. At a certain current level, however, a channel pinchoff effect is reached within the device, and the operating characteristic moves into a constant current region.

Figure 4 **Comparison of idealized output characteristics of power MOSFET and bipolar transistor**



The bipolar transistor also exhibits a generally similar type of collector characteristic. It does not, however, show a truly resistive effect in its saturation region, nor does it exhibit nearly such a well regulated constant current characteristic.

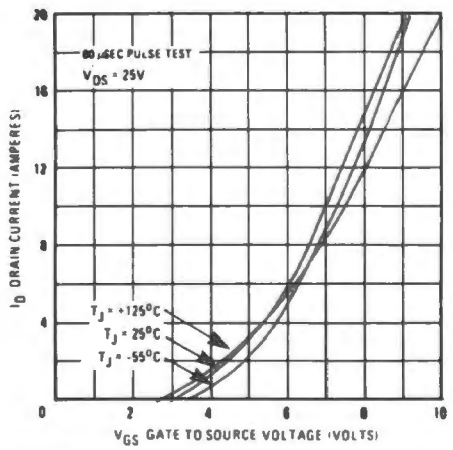
For switching applications, the On-Resistance $R_{DS(ON)}$ of the power MOSFET is obviously an important characteristic because it determines the power loss for a given drain current. The lower the On-Resistance the higher the current handling capability of the device. On-Resistance is thus an important 'figure of merit' of the power MOSFET.

Threshold voltage and transconductance

Inspection of the static drain-source operating characteristics of Figure 4 reveals that as the gate-to-source voltage is increased from zero, initially the drain current does not increase significantly. Only once a certain threshold gate voltage has been reached, does the drain current start to increase appreciably.

This is illustrated more clearly by the typical relationships between drain current and gate voltage shown in Figure 5. It is seen that in the operating region beyond the threshold gate voltage, the relationship between the drain current and the gate voltage is approximately linear. Stated another

Figure 5 **Transfer characteristics (RS130)**



way, the rate of change of drain current with gate voltage – the transconductance referred to earlier – becomes relatively constant at higher values of drain current.

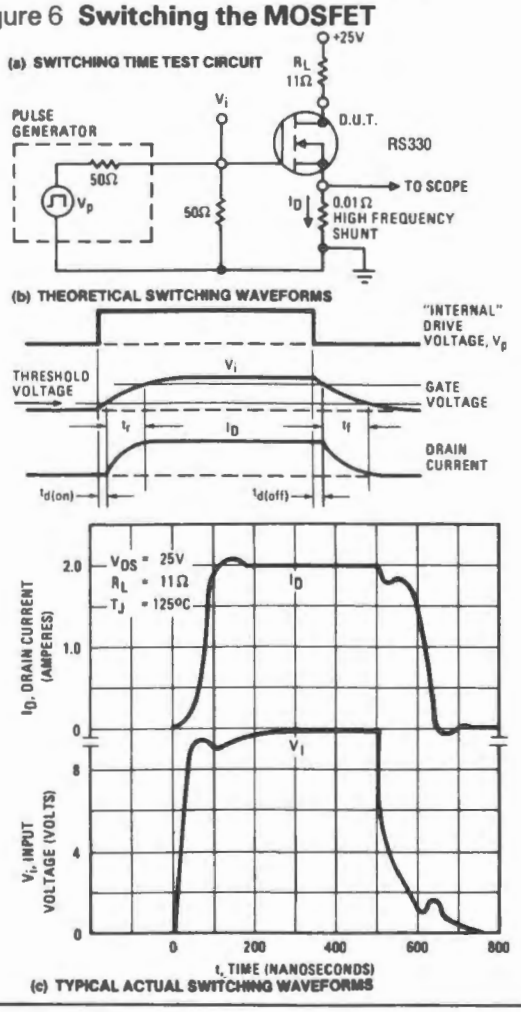
Switching times

MOSFET power transistors are much faster than bipolar power transistors of comparable size, primarily because they do not have minority carrier delay times. The response times of MOSFETs are determined primarily by the device capacitances, and secondarily by such factors as the extremely short channel transit time of the electrons.

The input capacitance, C_{iss}, is the primary factor which determines the response time of a MOSFET. Although MOSFETs can be controlled by extremely low currents (i.e. high source impedances), the relatively long charge and discharge time of the input capacitance, C_{iss}, results in a tradeoff of response time against extreme sensitivity. A first order approximation of the response time of a MOSFET can be made by determining the time constant which results from the input capacitance times the effective source impedance.

Figure 6 shows typical switching waveforms of an RS330 when driven by a 500 nanosecond-wide pulse. A good first order understanding of the switching response times $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f, can be made by considering the power MOSFET as an ideal switch with a 3 volt 'on' threshold. The output current can be considered controlled, without delay, by the instantaneous gate voltage which, in turn, is controlled by the time constant formed by $R_{input} \times C_{iss}$.

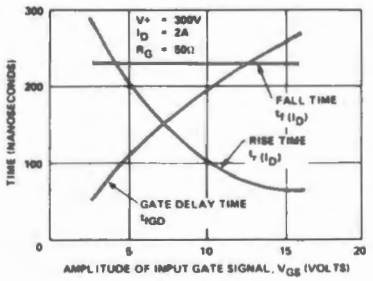
Figure 6 **Switching the MOSFET**



With these concepts in mind, the switching waveshapes of Figure 6(b) and the response times can be more easily understood. The turn-on delay, $t_{d(on)}$, is primarily the time for the transistor gate capacitance to be charged by the control signal to the threshold level of 3 volts maximum. The rise time, t_r, is the gate charging time required to drive from the threshold voltage, through the linear control region, to the gate voltage (typically 5 to 8 volts) required for full conduction of the drain current. In turn-off the procedure is reversed, and the turn-off delay time, $t_{d(off)}$, is primarily the time required for the gate capacitance to discharge from the gate overdrive saturation voltage (typically 10 volts) to the active gate control region (typically 5 to 8 volts). Finally, the fall time, t_f, is primarily the time delay required for the input capacitance to discharge through the active control region to the gate threshold voltage.

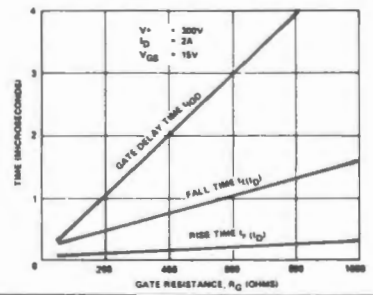
Figure 7 shows typical relationships for the RS330 between the amplitude of the applied gate voltage signal, the turn off delay time, the fall time, and the rise time of the drain current, with the simple 'resistive' gate drive circuit shown in Figure 6. Note that the turn off delay time increases with increasing gate drive, for the reasons already explained. The rise time of the drain current, on the other hand, decreases with increasing gate drive; this is because the higher the applied gate drive signal the faster the gate to source voltage reaches the level needed to support the drain current. The fall time of the drain current remains practically constant with applied gate drive; this is because the decay of the gate-to-source voltage below the point at which the drain current I_D can no longer be maintained, is practically independent of the amplitude of the applied gate signal.

Figure 7 **Typical relationships between switching times and applied gate voltage (RS330)**



Typical relationships between switching times and gate circuit resistance are shown in Figure 8. Predictably, the higher the gate resistance, the longer the switching times, because of the longer time constant $R_G C_{iss}$.

Figure 8 **Typical relationships between switching times and gate circuit resistance (RS330)**



Switching times with an inductive load

In many applications the load during the switching interval will be essentially inductive. Figure 9 shows a simple circuit with a clamped inductive load; corresponding idealized switching waveforms are shown in Figure 10. Note that at switch-on the current first rises, then the voltage falls. At switch off the drain voltage rises, then the current falls. Note that this assumes that the load is sufficiently inductive that current flows continuously in it; through the MOSFET when it is switched on, and through the clamping diode when the MOSFET is switched off. It is also assumed that stray circuit inductance between the clamping diode and the MOSFET is negligible. Thus at switch on, load current that is already flowing in the clamping diode commutates into the MOSFET, and the transfer of this current is unrestricted by stray circuit inductance. In general this assumption for the switch on condition is somewhat pessimistic, but it can be approximated in certain circuits.

Figure 9 **Simple circuit with clamped inductive load**

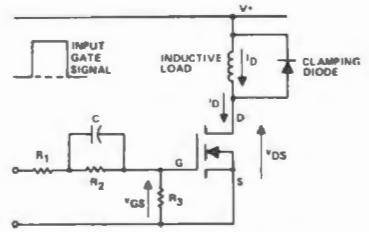
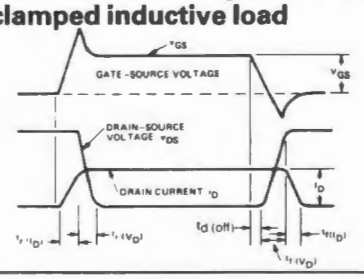


Figure 10 **Idealized switching waveforms for clamped inductive load**



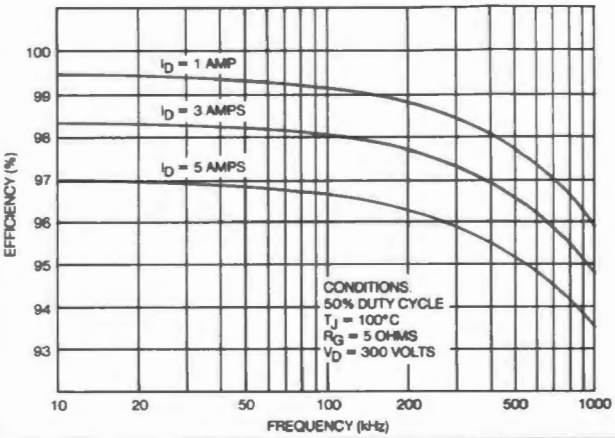
Maximum operating efficiency

Because of the extremely fast switching times of the power MOSFET – at least an order of magnitude faster than those of comparably rated bipolar transistors – the energy dissipated during switching is very much lower, and the power MOSFET is able to operate at switching frequencies an order of magnitude or more higher.

Relationships between operating frequency and switching efficiency of the RS330 power MOSFET with a resistive load, are shown in Figure 11. This data is based upon actual measured values of switching energy at a supply voltage of 300V, and a 50% duty cycle. Figure 11 takes account of the losses in the power MOSFET itself, and not of other components in the circuit; it does not therefore represent the overall circuit efficiency. Clearly, so far as the MOSFET itself is concerned, switching frequencies up to 500 kHz or higher are quite feasible. The switching efficiency is defined as:

$$\text{Switching Efficiency} = \frac{\text{Power Input} - \text{MOSFET losses}}{\text{Power Input.}}$$

Figure 11 **Switching efficiency (RS330)**

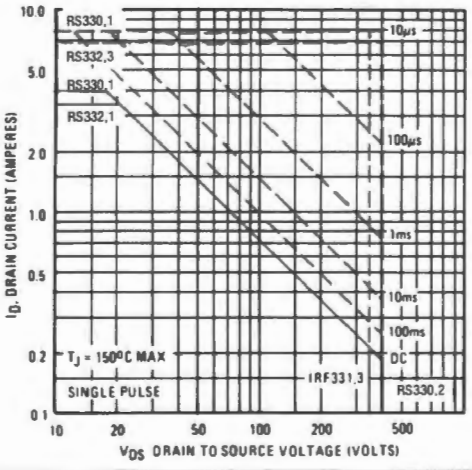


Safe operating area

One of the outstanding features of the RS power MOSFET range is that they do not display the second breakdown phenomenon which is frequently the Achilles heel of bipolar transistors. A simple physical explanation accounts for this superiority. If localized, potentially destructive, heating occurs within a MOSFET transistor, the carrier mobility in that area decreases. As a result the MOSFET has a positive temperature coefficient and acts in a self-protective manner by forcing currents to be uniformly distributed through the silicon die. In contrast a bipolar transistor, particularly under conditions of high collector-emitter voltage, displays 'current crowding' in the base region, which causes hot spots. Because of the bipolar's negative temperature coefficient, these hot spots tend to further 'hog' the current and cause instantaneous, catastrophic destruction of the die.

The rated maximum power dissipation of the bipolar device actually applies only over a very limited range of collector voltage, typically up to 10% of rated V_{CEO}. At higher voltages, the DC power dissipation is severely limited by second breakdown. Typically, at rated voltage the permissible power dissipation is only 5% of full rated power.

Figure 12 **Maximum safe operating area (RS330)**



The Safe Operating Area of the RS330 series MOSFET is shown as an example in Figure 12. Note that the DC current is limited throughout the voltage range only by the 75 watt power dissipation slope. There are no secondary slopes in the DC dissipation curve (or the pulse curve) that indicate the second breakdown limit commonly seen on bipolar Safe Operating Area curves. Note also the high values of pulse current and the corresponding long periods for which the pulse power can be safely tolerated.

The RS330, for example, can tolerate 0.375 amperes at 200 volts on a DC basis. By contrast, the popular 2N6545, a bipolar transistor with the same voltage rating, but double the continuous current rating, has only a 0.06 ampere DC second breakdown limit at 200 volts. At one millisecond pulse width and 300 volts, the RS330 rates at 1.0 amperes versus only 0.45 amperes for the 2N6545.

The absence of second breakdown means that the power MOSFET is generally a much more rugged device than the bipolar transistor. This is extremely important, both for 'linear' and 'switching' applications.

The V_{DS} absolute maximum rating of MOSFETs should not be exceeded by allowing them to operate in the avalanche region. However, it is possible to reliably turn off high level inductive currents, which can generate high voltage inductive transients, by using a simple voltage clamp circuit. All the RS MOSFETs have a clamped inductive rating such that the maximum rated pulse current can be turned off with a 100 microhenry inductor in series. Because MOSFETs are very fast devices, caution must be taken that the voltage clamp device has a sufficiently fast response, and that it is closely coupled to the drain-source terminals. A zener diode connected physically as close as possible to the drain and source terminals generally will provide acceptable voltage clamping.

The transconductance, g_{fs}, of a MOSFET is maximum at the highest allowable drain currents. In contrast, the DC gain, h_{FE}, of a bipolar transistor, decreases drastically at high collector currents. The high transconductance of MOSFETs at high currents, combined with the excellent SOA rating, result in MOSFETs being superb pulse amplifiers. All the RS power MOSFETs have a pulsed current rating, I_{DM}, that is at least twice the continuous current rating, I_D. RS's power MOSFETs operate excellently in the pulse region as long as the allowable average power dissipation, safe operating area, and ±20 volt maximum gate voltage ratings are not exceeded.

Temperature stability

MOSFETs have outstanding gain and switching time stability with temperature variations, relative to the stability of typical bipolar transistors. The transconductance of RS Power MOSFETs typically varies less than ±20% from the 25°C value, over a −55°C to 125°C range. The DC current gain of a power bipolar commonly varies by a factor of 2 or 3 over this temperature range.

A rough comparison of the typical DC gain stability for an RS power MOSFET versus a power bipolar would yield a transconductance, g_{fs}, temperature coefficient of about −0.2% per °C versus a bipolar current gain, h_{FE}, temperature coefficient of about +0.8% per °C – a four-fold difference.

Reference to Figure 5 will show that the threshold voltage (bias point) and the transconductance (DC gain) move with temperature in compensating directions. Therefore, an operating point on the DC transfer characteristic maintains unusually good open loop stability. Drift-free operation becomes easy in a linear, closed loop system.

The switching time of RS power MOSFETs is essentially independent of operating temperature. This is a tremendous advantage relative to bipolar transistors, for which the 25°C switching times and associated power losses commonly increase by a factor of 2 or 3 at the higher actual operating temperatures. The extraordinary switching time stability of MOSFETs results because the response times are primarily dependent on the input capacitance, C_{iss}, which is essentially temperature invariant.

The on-resistance, $R_{D(ON)}$ of power MOSFETs, has a positive temperature coefficient, of approximately +0.7% per °C. This is an advantage in paralleling MOSFETs, and as has been seen it also accounts for their excellent safe operating area. However, in determining the on-state power losses in a switching mode, the increased value of $RD_{(ON)}$ at the actual maximum junction operating temperature must be used. Sufficient heatsink must always be used so that a thermal runaway situation cannot occur.

Paralleling

Power MOSFETs are easy to parallel, because the positive temperature coefficient forces current sharing among the paralleled devices. Current sharing resistors, with their associated power losses, are not necessary. Some resistance in series with the gates (typically 100 ohms) and close paralleled lead connections may be necessary to assure that the good high frequency response of the MOSFETs does not cause oscillations.

MOS caution

The ±20 volt absolute maximum gate voltage rating of RS power MOSFETs should never be exceeded, or permanent damage can occur.

Zener diode protection should be used if there is a danger of transient gate overvoltages. This caution applies also to the buildup of static charge. RS power MOSFETs have large gate capacitances and thick oxide layers relative to low level MOS devices, where static charge damage can be particularly dangerous. Though significantly more rugged than such low level MOS devices, reasonable precautions which are normally taken in handling MOS devices should be observed until the installation of MOSFETs in a circuit.

Applications

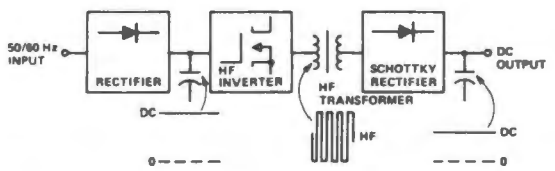
Power MOSFETs offer tremendous operating advantages over conventional bipolar transistors, and they will undoubtedly replace bipolars in many existing applications. In order to take full advantage of their unique operating features, and thus to produce an optimum overall system design, it will almost never be sufficient merely to make a one-for-one replacement of a bipolar with a MOSFET in an otherwise unmodified circuit. The much lower drive requirement of the MOSFET will usually mean that very significant simplifications can be made in the drive circuitry; the vastly superior switching speed will offer the possibility for lower

losses, or higher operating frequency, or both; and the superior safe operating area will offer greater loading and overloading capability, and minimization or elimination of protective snubber components.

Switching power supplies

Switching DC power supplies are rapidly replacing conventional 50 or 60 Hz transformer/rectifier supplies. The basic principle of the switching power supply is illustrated in Figure 13.

Figure 13 **Basic principle of switching power supply**



This switching scheme by comparison with the conventional line frequency power supply, offers smaller overall size, due to much smaller transformer and smoothing components, faster response, better regulation, and higher efficiency.

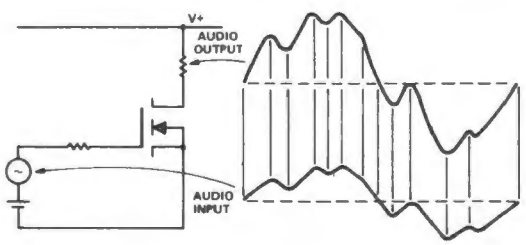
Switching power supplies presently use bipolar transistors, and usually operate in the 20-35 kHz frequency range. Higher operating frequencies are not generally practical, because bipolar switching times are too long. From the system viewpoint, an increase in the switching frequency to 200 kHz or higher would offer the possibility for further reductions in size, weight, and response time. Such high operating frequencies now become a practical reality, with the availability of the RS power MOSFET range. Other potential advantages would be elimination of electrolytic capacitors, smaller EMI filters, and simplified drive and snubber circuits.

The MOSFET also offers advantages in the existing 20 to 30 kHz range, in terms both of reduced overall losses, because of reduced switching losses, and reduced circuit complexity, because of the minimal gate drive requirement.

Audio amplifiers

The power MOSFET offers a quite linear input to output transfer characteristic. This means that with appropriate biasing it can be used as a simple high quality audio amplifier, illustrated in a simplified form in Figure 14.

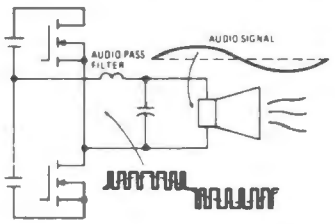
Figure 14 **Basic principle of audio amplification using power MOSFET**



The excellent Safe Operating Area of power MOSFETs makes them particularly well suited for class B amplifiers, which require extreme low frequency response at high power levels. The wide MOSFET bandwidth makes good high frequency response of the amplifier easy.

Another type of audio amplifier uses the class D pulsewidth modulation principle, illustrated diagrammatically in Figure 15. Implementation of this type of amplifier with bipolar transistors has not generally been successful, because the carrier frequency must be much higher than the audio frequency to produce a good quality output. The relatively long switching times of the bipolar are a fundamental limitation. With the availability of the RS power MOSFET range, these limitations are eliminated. This type of approach offers the possibility for an audio amplifier of extremely high efficiency, small size, and high fidelity.

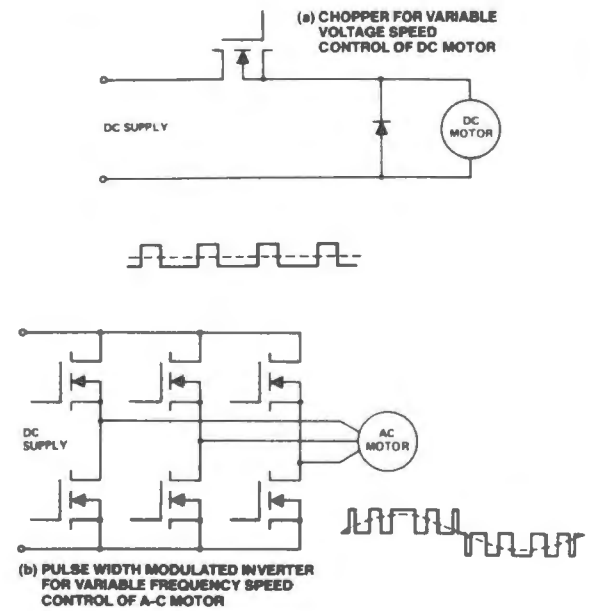
Figure15 **Class D audio amplifier – basic principle**



Motor speed control

Basic chopper and inverter schemes for motor speed control using power MOSFETs are shown in Figure 16.

Figure16 **Basic schemes for variable speed control of DC and AC motors using power MOSFETs**



The use of variable frequency DC to AC inverters, for efficient control of the speed of AC induction motors is becoming particularly topical in view of the present day emphasis on energy saving techniques.

In these circuits the switching frequency typically will be in the range of a few hundred Hz, to a few kHz. This, of course, is well within the capability of bipolar transistors. MOSFETs can however offer significant advantages, because of their substantially reduced drive power requirements, and improved safe operating area and ruggedness. These features will result in simplification of peripheral circuitry, improved reliability, and improved response time.

The ease of paralleling power MOSFETs for higher power output is also an important advantage, whilst the somewhat higher conduction voltage drop and hence higher power loss of the MOSFET is but a slight disadvantage – more theoretical than practical. The extra heatsink required to accommodate the greater power dissipation of the MOSFET is minimal indeed, and is greatly outweighed by the advantages to be gained.

Fluorescent lighting

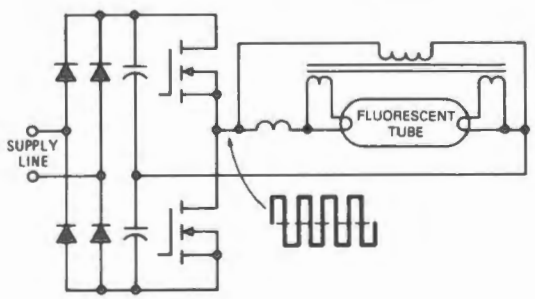
Conventional mains frequency fluorescent lighting requires bulky inductive ballasting and power factor capacitors, and is relatively inefficient. It is well known that by using high frequency to supply the fluorescent tube, power consumption for a given light output can be reduced by 30 to 35%, whilst tube life can be substantially increased, and bulky ballast components are eliminated.

Fluorescent lighting schemes using high frequency bipolar transistor inverters are presently used in applications such as transportation and emergency lighting systems.

Application of high frequency techniques to the general consumer market has so far been inhibited by the relative complexity of the drive circuitry required for the bipolar transistor. RS's power MOSFETs with their extremely simple drive requirements are potentially ideal for this application.

A basic schematic of a high frequency fluorescent lighting scheme using MOSFETs is shown in Figure 17.

Figure 17 **HF lighting system – basic principle**



RS data

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An Electrocomponents Group Company

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RS data

Phase locked loops NE 565 and 567

Stock numbers 307-288 and 307-294

Two phase locked loop integrated circuits suitable for use in a wide range of applications including tone and telemetry decoders, frequency multiplication, division and demodulation, phase shifting, oscillation, pulse generation, frequency tracking and filters etc.

NE565 (307-288)

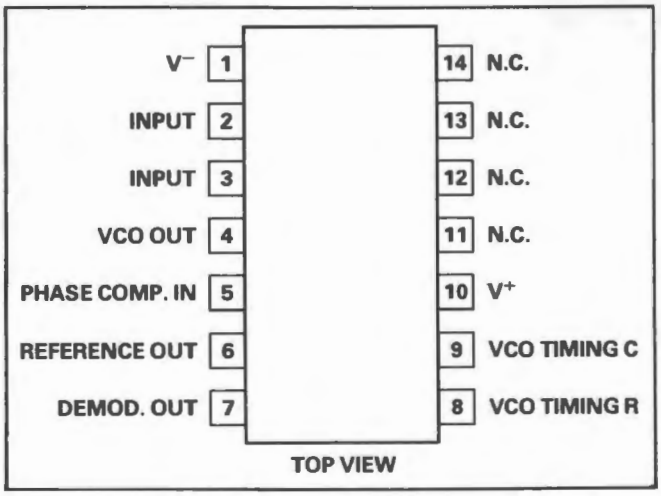
The RS NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001 Hz to 500 kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The centre frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

Absolute maximum ratings

Operating voltage	26V
Input voltage	3Vp-p
Storage temperature	–65°C to +150°C
Operating temperature	0 to +70°C
Power dissipation	300mW

Features

- Highly stable centre frequency (200ppm/°C typ.)
- Wide operating voltage range (±6 to ±12 volts)
- Highly linear demodulated output (0.2% typ.)
- Programmable centre frequency
- TTL and DTL compatible square-wave output; loop can be opened to insert digital frequency divider
- Highly linear triangle wave output
- Reference output for connection of comparator in frequency discriminator
- Bandwidth adjustable from < ±1% to > ±60%
- Frequency adjustable over 10 to 1 range



Electrical characteristics

$T_A = 25°C$, $V_{CC} = \pm 6V$ unless otherwise specified

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply requirements					
Supply voltage		±6		±12	V
Supply current			8	12.5	mA
Input characteristics					
Input impedance[1]		5	10		kΩ
Input level required for tracking	f_O = 50kHz, ±10% frequency deviation	10	1		mVrms
VCO characteristics					
Centre frequency					
Maximum value	C_1 = 300pF		500		kHz
Distribution[2]	Distribution taken about f_o = 50kHz, R_1 = 5.0kΩ, C_1 = 1200pF	-30	0	+30	%
Drift with temperature	f_o = 50kHz		300		ppm/°C
Drift with supply voltage	f_o = 50kHz, V_{CC} = ±6 to ±7 volts		0.2	1.5	%/V
Triangle wave					
Output voltage level		1.9	0		V
Amplitude			2.4	3	Vp-p
Linearity			0.5		%

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Square wave					
Logic '1' output voltage	f_o = 50kHz	+4.9	+5.2		V
Logic '0' output voltage	f_o = 50kHz		–0.2	+0.2	V
Duty cycle	f_o = 50kHz	40	50	60	%
Rise time			20		ns
Fall time			50		ns
Output current (sink)		0.6	1		mA
Output current (source)		5	10		mA
Demodulated output characteristics					
Output voltage level	Measured at pin 7	4.0	4.5	5.0	V
Maximum voltage swing[3]			2		Vp-p
Output voltage swing	±10% frequency deviation	200	300		mVp-p
Total harmonic distortion			0.4	1.5	%
Output impedance[4]			3.6		kΩ
Offset voltage (V6-V7)			50	200	mV
Offset voltage vs temperature (drift)			100		μV/°C
AM rejection			40		dB

Notes:
1. Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to –4 volts.
2. The external resistance for frequency adjustment (R1) must have a value between 2kΩ and 20kΩ
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

Figure 1 **Block diagram**

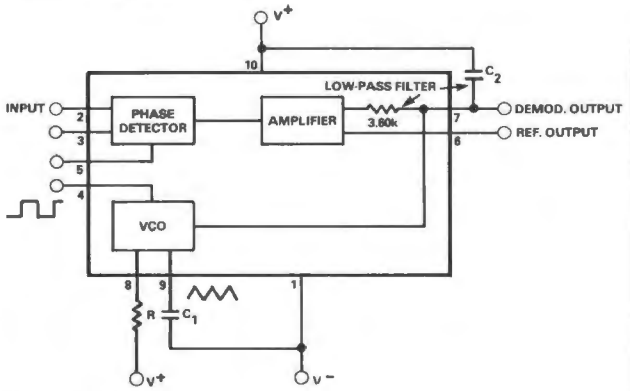
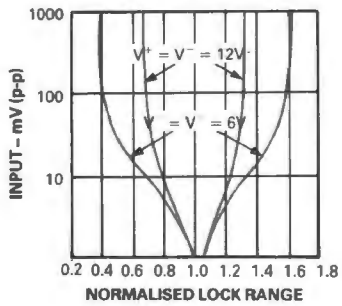


Figure 3 **Lock range as a function of input voltage**



Typical performance characteristics

Figure 2 **VCO conversion gain**

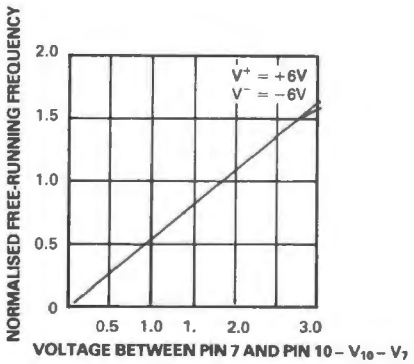
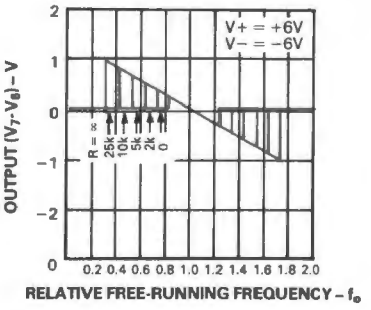


Figure 4 **Lock range as a function of gain setting resistance (Pins 6-7)**



Design formulas

(See Figure 5)

Free-running frequency of VCO: $f_o \simeq \frac{1.2}{4R_1C_1}$ in Hz

Lock-range: $f_L = \pm \frac{8f_o}{V_{CC}}$ in Hz

Capture-range: $f_C \simeq \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{r}}$

where $r = (3.6 \times 10^3) \times C_2$

Typical applications

FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

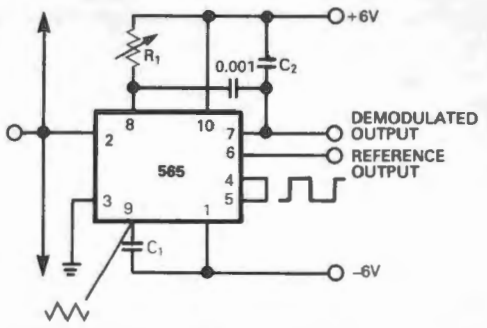
A typical connection diagram is shown in Figure 5. The VCO free-running frequency is given approximately by

$f_o = \frac{1.2}{4R_1C_1}$ and should be adjusted to be at the centre of the input signal frequency range. C1 can be any value, but R1 should be within the range of 2000 to 20,000 ohms with an optimum value in the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_o to approximately ±20% of f_o (at ±6V).

A small capacitor (typically 0.001 μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.

Figure 5 **FM demodulation**



Frequency shift keying (FSK)

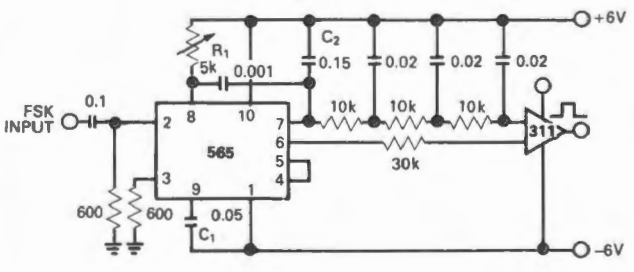
FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the '0' and '1' states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 6. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

The loop filter capacitor C2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output, The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R1 so as to result in a slightly-positive voltage at the output with f_{IN} = 1070Hz.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600 ohm input impedance).

Figure 6 **Frequency shift keying**



NE567 (307-294)

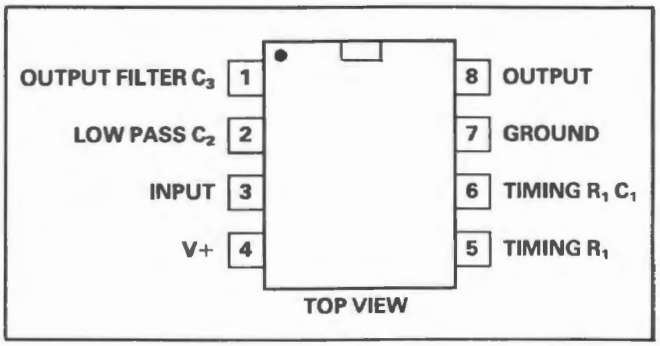
The RS NE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth centre frequency, and output delay are independently determined by means of four external components.

Absolute maximum ratings

Operating voltage ____ 10V
Positive voltage at input ____ 0.5V + V_S
Negative voltage at input ____ $-10V_{DC}$
Output voltage (collector of output transistor) ____ $15V_{DC}$
Storage temperature ____ −65°C to +150°C
Operating temperature ____ 0 to +70°C
Power dissipation ____ 300mW

Features

- Wide frequency range (0.01Hz to 500kHz)
- High stability of centre frequency
- Independently controllable bandwidth (up to 14 percent)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20 to 1 range with an external resistor

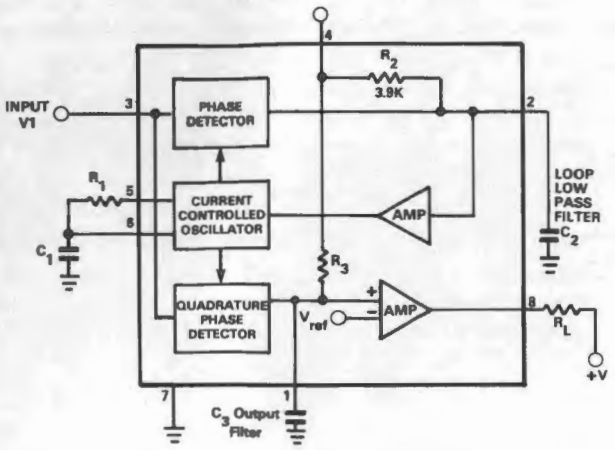


DC Electrical characteristics ($V+ = 5.0V$; $T_A = 25°C$ unless otherwise specified.)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Centre frequency[1]					
Highest centre frequency (f_o)		100	500		kHz
Centre frequency stability[2]	0 to +70°C		35±60		ppm/°C
Centre frequency shift with supply voltage	f_o = 100kHz		0.7	2	%/V
Detection Bandwidth					
Largest detection bandwidth	f_o = 100kHz	10	14	18	% of f_o
Largest detection bandwidth skew			3	6	% of f_o
Largest detection bandwidth–variation with temperature	V_i = 300mVrms		±0.1		%/°C
Largest detection bandwidth–variation with supply voltage	V_i = 300mVrms		±2		%/V
Input					
Input resistance			20		kΩ
Smallest detectable input voltage (V_i)	I_L = 100mA, $f_i = f_o$		20	25	mVrms
Largest no-output input voltage	I_L = 100mA, $f_i = f_o$	10	15		mVrms
Greatest simultaneous outband signal to inband signal ratio			+6		dB
Minimum input signal to wideband noise ratio	B_n = 140kHz		–6		dB
Output					
Fastest on-off cycling rate			f_o/20		
'1' output leakage current			0.01	25	μA
'0' output voltage	I_L = 30mA		0.2	0.4	V
	I_L = 100mA		0.6	1.0	V
Output fall time[3]	R_L = 50Ω		30		ns
Output rise time[3]	R_L = 50Ω		150		ns
General					
Operating voltage range		4.75		9.0	V
Supply current quiescent			7	10	mA
Supply current – activated	R_L = 20kΩ		12	15	mA
Quiescent power dissipation			35		mW

Notes:
1. Frequency determining resistor R_1 should be between 1 and 20kΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminating pulsing during turn-on and turn-off.

Figure 7 **Block diagram**



Typical performance characteristics

Figure 8 **Detection bandwith as a function of C_2 and C_3**

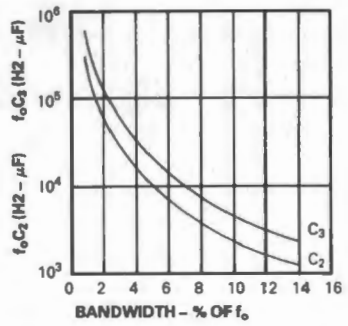


Figure 9 **Greatest number of cycles before output**

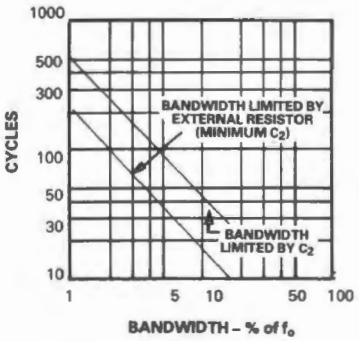
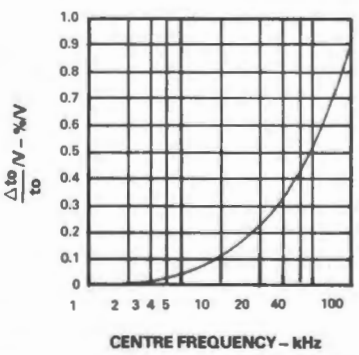


Figure 10 **Centre frequency shift with supply voltage change vs operating frequency**



Design formulas

$$f_o \simeq \frac{1.1}{R_1 C_1}$$

$$BW \simeq 1070\sqrt{\frac{V_1}{f_o C_2}} \text{ in \% of } f_o,\ V_i \leq 200\text{mVrms}$$

Where

V_i = Input Voltage (Vrms)
C_2 = Low-Pass Filter Capacitor (μF)

Phase locked loop terminology

Centre frequency (fo)
The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection bandwidth (BW)
The frequency range, centred about f_o, within which an input signal above the threshold voltage (typically 20mVrms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock range
The largest frequency range within which an input signal above the threshold voltage will hold a logic zero state on the output.

Detection band skew
A measure of how well the detection band is centred about the centre frequency, f_o. The skew is defined as $(f_{max} + f_{min} - 2f_o)/2f_o$ where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

Operating instructions

Figure 11 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

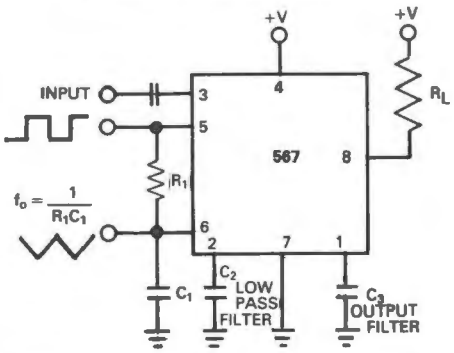
1. Select R_1 and C_1 for the desired centre frequency. For best temperature stability, R_1 should be between 2k and 20k ohm, and the combined temperature coefficient of the R_1C_1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.

2. Select the low pass capacitor, C_2, by referring to the Bandwith versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_oC_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_oC_2 product (f_o (Hz), C_2 (μfd)).

3. The value of C_3 is generally non-critical C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage

on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

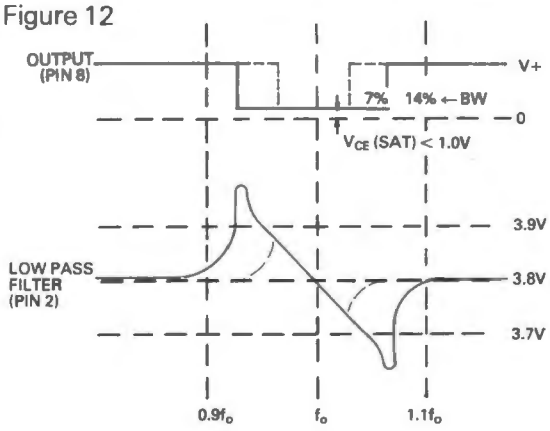
Figure 11 **Typical connections**

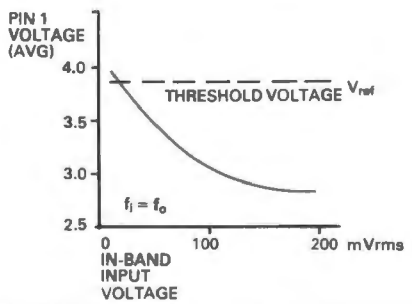


Available outputs (Figure 12)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_o with a slope of about 20mV per cent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2BV_{be}) \approx (+V - 1.4V)$ having a dc average of $+V/2$. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of $+V/2$. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

Figure 12





Operating precautions

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_o/3$, $f_o/5$, etc.

2. The 567 will lock onto signals near $(2n + 1)\ f_o$, and will give an output for signal as near $(4n + 1)\ f_o$ where $n = 0, 1, 2$, etc. Thus, signals at $5f_o$ and $9f_o$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and outband signals is afforded in the low input level (below 200mVrms) and reduced band-width operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph (Figure 9).

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energisation on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

Speed of operation

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band centre frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o}\ \mu F$$

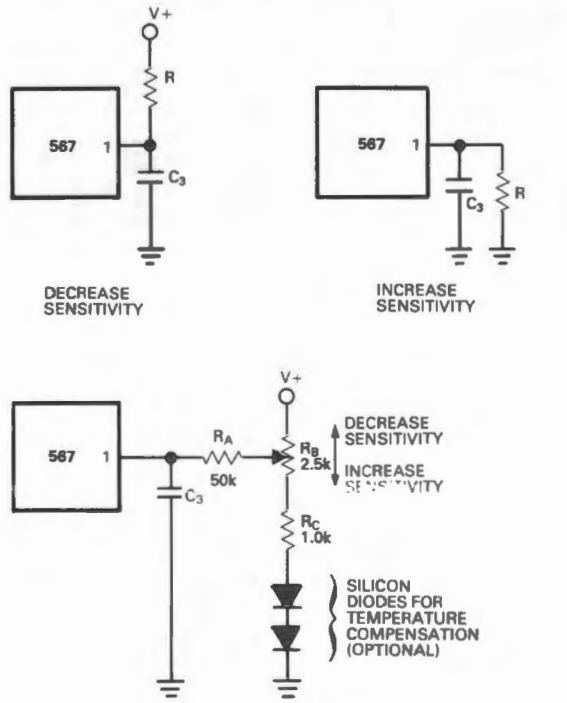
$$C_3 = \frac{260}{f_o}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

Optional controls (Figure 13).

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

Figure 13 **Sensitivity adjustment**



Sensitivity adjustment (Figure 13).

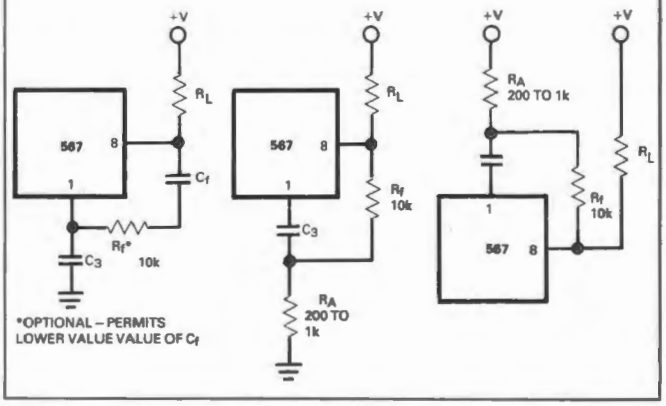
When operated as a very narrow band detector (less than 8 per cent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitising the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

Chatter prevention (Figure 14).

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognise the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 14. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to ensure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

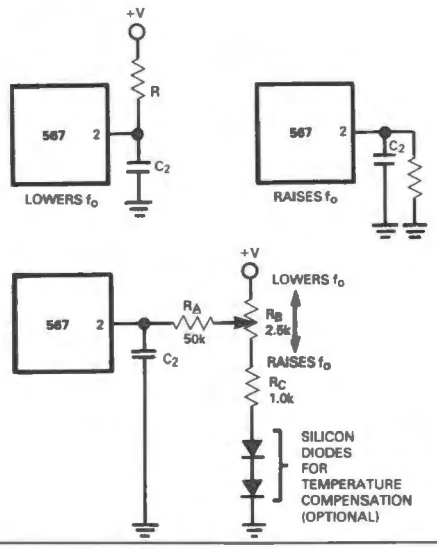
Figure 14 **Chatter prevention**



Detection band centring (or skew) adjustment (Figure 15).

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the centre frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

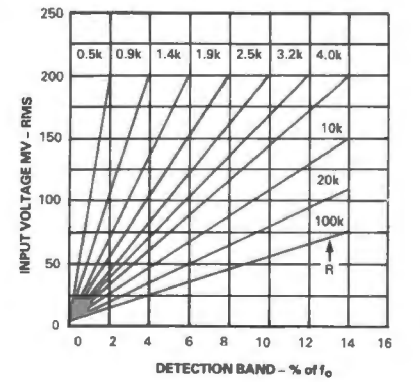
Figure 15 **Detection band centring (or skew) adjustment**

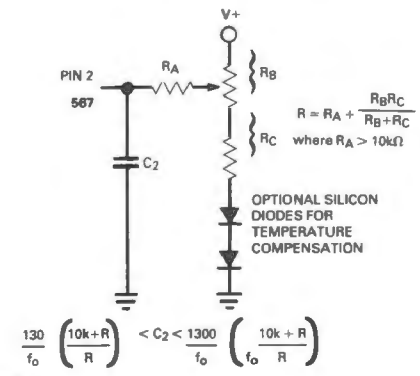


Alternative method of bandwidth reduction (Figure 16).

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cut-off frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

Figure 16 **Bandwidth reduction**



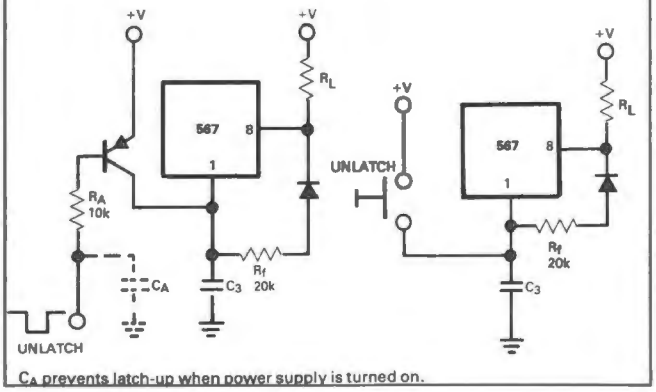


NOTE:
Adjust control for symmetry of detection band edges about f_o.

Output latching (Figure 17).

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

Figure 17 **Output latching**

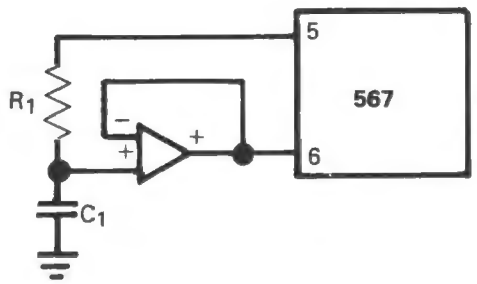


C_A prevents latch-up when power supply is turned on.

Reduction of C1 value (Figure 18).

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost saving may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

Figure 18 **Precision very low frequency operation**

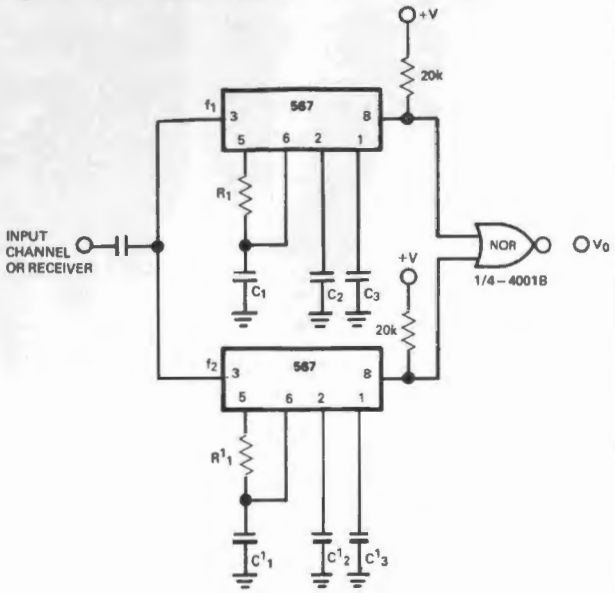


Programming

To change the centre frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.

Typical applications

Figure 19 **Dual tone decoder**



1. Resistor and capacitor values chosen for desired frequencies and bandwith.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

Figure 20 **24% Bandwith tone decoder**

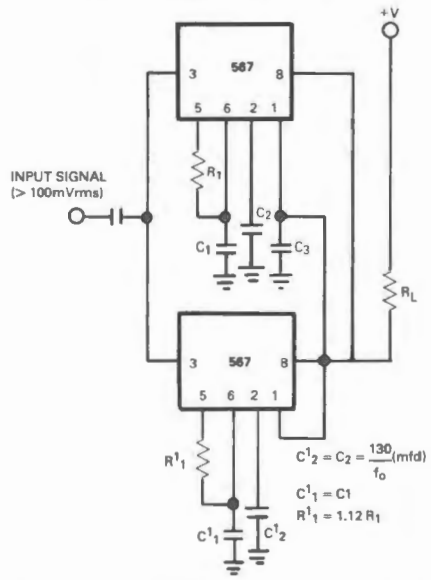
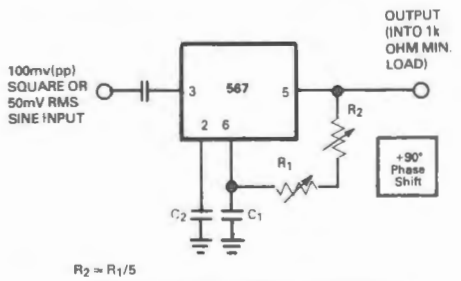


Figure 21 **0° to 180° phase shifter**



$R_2 \simeq R_1/5$

Adjust R_1 so that $\varnothing = 90°$ with control midway.

Figure 22 **Oscillator with quadrature output**

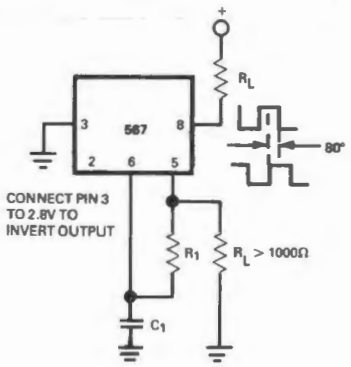


Figure 23 **Oscillator with double frequency output**

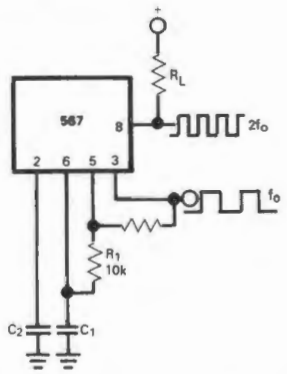


Figure 24 **Precision oscillator with 20ns switching**

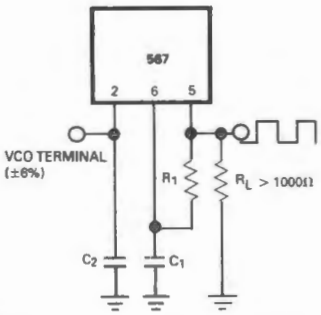
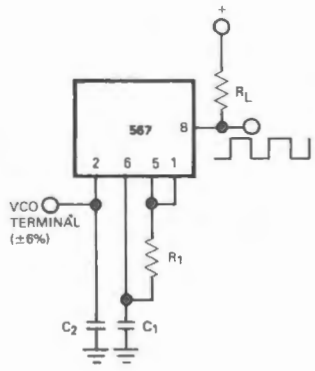


Figure 25 **Precision oscillator to switch 100mA loads**



RS data

Figure 26 **Pulse generator with 25% duty cycle**

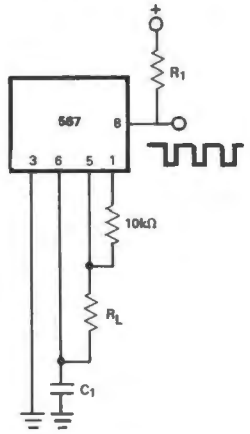
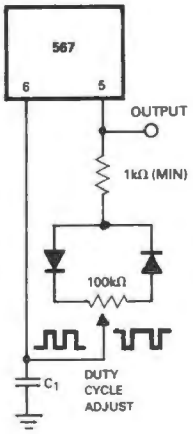


Figure 27 **Pulse generator**



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RS data

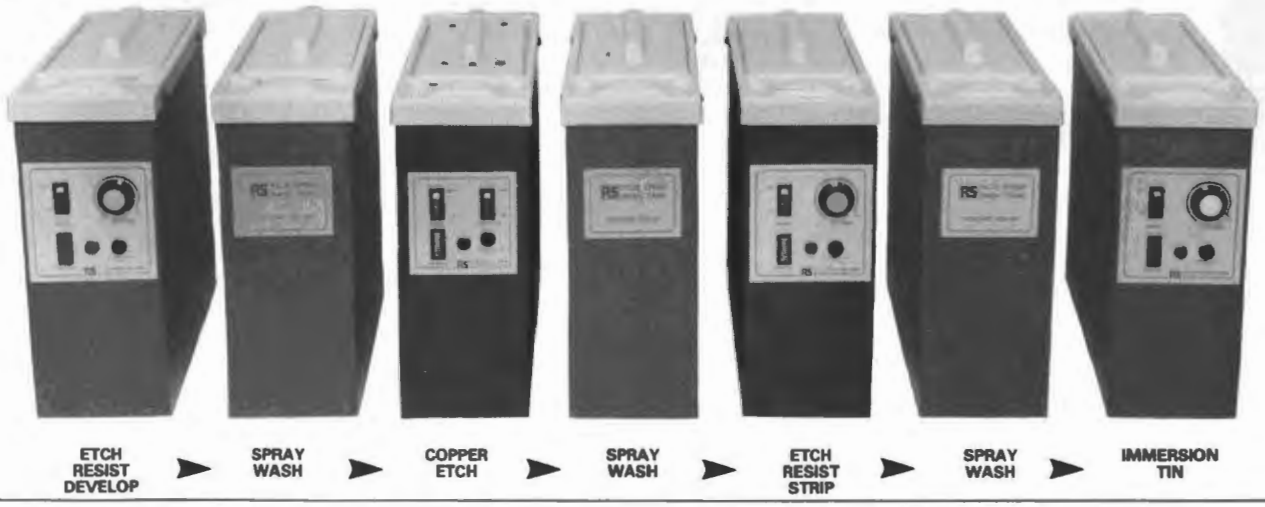
P.C.B. Modular preparation system

The RS p.c.b. modular preparation system comprises three units; a bubble etch tank (556-806), an uncommitted heated process tank (550-375), a spray wash tank (550-381) and a range of chemicals. The three free-standing bench top units may be used independently on a 'stand alone' basis, or intermixed and used in any order to suit the processes required. A typical four process, seven tank system would be as shown below.

Features

- Process, wash and bubble etch tanks available
- May be used individually, or together to form a complete system
- Thermostatic control on process and bubble etch tank
- All tanks incorporate baskets for safe p.c.b. handling

Typical four process, seven tank system



Electrical installation

(556-806 and 550-375 only)

The tank should be connected to a single phase 240V 50Hz supply via the integral cable. When using a mains plug with a fitted fuse, for example the British '13A ring main' system, the fuse fitted should be a 3A H.R.C. type. On other systems a 5A fuse should be fitted at the distribution board.

Note that the tank supply must be properly earthed.

Tank emptying

(556-806 and 550-375)

When the solution is exhausted or has exceeded its shelf life, empty the tank (using the pump siphon provided) into a suitable receptacle such as a plastic bucket. The solution must be disposed of in such a way as not to endanger personnel, animals, crops, water supplies, or contravene local drainage regulations.

Bubble etch tank

(556-806)

Warnings

1. This tank is suitable for use **ONLY** with ferric chloride which is both corrosive and poisonous. Use ferric chloride hexahydrate crystals, not anhydrous ferric chloride which is dangerously exothermic when mixed with water. Avoid contact with skin, eyes, and clothing. In case of accidental contact with skin or eyes, rinse with copious quantities of clean water. If irritation persists, seek medical advice. The use of protective gloves is strongly recommended.

   If accidentally ingested, seek medical attention immediately.

2. Do not switch on the tank when empty, as this will damage the heating element.

3. Do not switch on the agitator without the tank lid properly in position, as this could result in splashing of the corrosive ferric chloride solution.
4. The tank should be sited in a such a position that accidental spillage or splashing of the ferric chloride solution would not cause injury or damage.

Etchant preparation

Pour approximately 2 litres of clean cold water into a suitable receptacle, and add 2kg of finely ground ferric chloride hexahydrate crystals, taking care not to splash. The etchant should be thoroughly mixed and all the ferric chloride crystals dissolved **before** the solution is transferred to the tank. Under no circumstances should undissolved crystals be allowed to accumulate in the bottom of the tank, as this could cause overheating of the element and consequent damage to the tank walls.

Transfer the solution to the etch tank, and top up with water until the solution reaches the 'fill' line, denoted by the joint between the tank top and tank body (capacity approx. 3.8 litres total). Carefully replace the lid and switch on the unit and the agitator. Note that agitator operation is indicated by illumination of the red 'agitator' switch. The amber 'heater' indicator will illuminate and remain so until the etchant reaches working temperature (45°C/max.) when it will be extinguished. After working temperature has been reached, it is advisable to allow the agitator to operate for approximately 1 minute to facilitate even distribution of ferric chloride in the solution.

Use of etchant

1. Always wipe down any ferric chloride spillage with a wet cloth to avoid staining, whilst wearing suitable protective gloves to avoid skin contact with the etchant.
2. Never allow the etchant level to fall more than 40mm below the tank top. Make up level by adding water.
3. When the etching time reaches 15 minutes the solution must be replaced with fresh etchant, having first washed the tank out thoroughly with warm water.
4. At no time should ferric chloride crystals be added to an already made up working solution, either for topping up purposes or to decrease etching times.

Board etching

Ensure that agitator is switched off before opening the tank. Place the board to be etched in the basket which is attached to the underside of the tank lid. The board should be tilted so that one top edge contacts the side of the basket and one bottom edge contacts the base of the basket, allowing the etchant maximum access to both sides of the board. Lower the basket into the solution, taking care not to splash. Switch on the agitator. With new solution, a double sided p.c.b. with 305gm/m^2 (1oz/sq ft) copper will be completely etched in approx. 6 minutes. As the solution ages, etching times will be extended, and regular checking of boards is recommended to establish the progress of the etching. When the etching time exceeds 10-12 minutes, complete renewal of the etchant is recommended. Before removing the board from the etchant ensure that the agitator is switched off. Lift the lid and basket vertically, taking care not to splash. Allow the etchant to drain off the basket and board surfaces before transferring the board to the washing process.

Heated process tank

(550-375)

Warnings

1. This tank is suitable for use **only** with sodium hydroxide (caustic soda) in the solution strengths specified (see solution preparation), commercial sodium hydroxide based developing/stripping solutions, or stannous chloride based tinning salts mixed strictly in accordance with the supplier's instructions.

   The use of protective gloves is strongly recommended.

2. Do not switch on the tank when empty, as this will damage the heating element.
3. The tank should be sited in such a position that accidental spillage or splashing of the solution would not cause injury or damage.
4. When using tinning salts, which have a tendency to solidify (crystallise) when cold, the solution MUST be stirred gently from the moment of turning on the heater (when reheating an existing solution), until all the crystals have been dissolved.
5. Care should be exercised when dissolving sodium hydroxide in water as the reaction generated is highly exothermic.

Solution preparation

Etch resist developing/stripping

Sodium hydroxide (caustic soda) 99% pearl w/w is used for both etch resist developing and stripping. Solution strengths are as follows:

Developing:
Approx 20 grams per litre (75-80 grams per tank 'fill')

Stripping:
Approx 100 grams per litre (375-400 grams per tank 'fill')

Pour approximately 2 litres of clean cold water into a suitable receptacle and slowly add the appropriate quantity of sodium hydroxide for one tank 'fill' (as stated above) for either developing or stripping, taking care not to splash, while gently and continuously stirring the resulting solution. **On no account exceed the maximum stated solution strength for the required process.** Note that care should be exercised when dissolving sodium hydroxide in water as the reaction generated is highly exothermic. When the sodium hydroxide has completely dissolved, transfer the solution carefully to the tank, and top up with clean cold water until the solution reaches the 'fill' line denoted by the joint between the tank top and tank body (capacity approx, 3.8 litres total). Gently agitate the solution with a suitable implement for a few seconds to ensure uniform distribution of solution strength, taking care not to damage the heater. The quantities and solution strengths specified above are

sufficient to develop/strip approx. 1.5m^2 of photo-resist board. Note that, when using pure sodium hydroxide solutions, the old solution should be discarded at the end of work each day regardless of whether the full specified area of photo-resist has been processed, and fresh solutions prepared at the recommencement of work. Under no circumstances should old solution be re-used or any attempt be made to store made-up solutions.

Commercially available sodium hydroxide based developing/stripping agents may be used. Make up 3.8 litres of solution in a suitable receptacle in strict accordance with the supplier's instructions, then transfer to the tank, taking care not to splash. Adhere to the supplier's instructions regarding re-use and storage of solutions. In general, commercially available developing/stripping agents contain wetting agents and antioxidants and have a far longer shelf life than pure sodium hydroxide solution. **Processing agents based on or containing organic solvents must not be put into the tank.**

Immersion tinning solution

Stannous chloride based tinning salts are used for immersion tinning of printed circuit boards, by electroless deposition of tin on exposed copper areas.

Prepare the solution in a suitable vessel strictly in accordance with the supplier's instructions, to a total volume of 3.8 litres. Ensure that the salts are completely in solution, then transfer the solution to the tank taking care not to splash. If necessary, top up the tank to the 'fill' line with clean water at the temperature specified by the salts supplier for solution preparation.

Important note

Most tinning salts solutions are specified for use at temperatures substantially above ambient, typically 40°C-60°C. When switching off the tank heater at the end of board preparation, therefore, the salts have a tendency to crystallise out as the solution temperature falls. These crystals will collect in the base of the tank around the heating element and will cause localised overheating and damage to the tank and the heating element if the heater is simply switched on and left to re-heat the tank at the re-commencement of board preparation. It is, therefore, **essential** to gently and continuously stir the tinning salts solution from the moment of switching on the heater when reheating an existing solution, until all crystals have dissolved. Care should be exercised not to damage the heating element when stirring the solution.

Use of solutions

1. Always wipe down any solution spillage with a wet cloth, whilst wearing suitable protective gloves to avoid skin contact with the solution.
2. Never allow the solution to fall more than 40mm below the tank top. Make up level by adding water.
3. Solutions which become exhausted or exceed their shelf life should be discarded, and fresh solutions prepared. Do not attempt to extend the life of a solution by adding further quantities of the appropriate chemicals.

Solution temperatures and processing times

Sodium hydroxide solution for etch resist developing:
20-30 seconds at 22°C is optimum. Temperatures in the range 18°C-27°C are permissible, the higher the temperature the lower the processing time and vice-versa. Below 18°C processing time is so long as to be impractical, and above 27°C there is a strong likelihood that the photo-resist may be stripped off the laminate by the solution.

Sodium hydroxide solution for etch resist stripping:
2 minutes at 45°C.

Stannous chloride based tinning salts and commercial sodium hydroxide based etch resist developer/stripper:
adhere to the recommendations of the supplier.

Temperature setting

Either a mercury bulb type or electronic probe thermometer may be used. Gently agitate the solution to ensure even temperature distribution. Introduce the thermometer into the solution so that the probe or tip is approximately half way down the tank, i.e. in the middle of the solution, and clamp into position in such a way that the scale may be clearly read. Determine the required temperature for the solution in use. If the measured temperature is below the required temperature, switch on the 'mains on/off' switch on the tank and rotate the thermostat control knob (labelled 'set temp') fully clockwise. The 'heater' indicator will illuminate, indicating heater operation. At approximately 1 minute intervals gently agitate the solution, taking care not to damage the heating element or thermometer and read the temperature. When the required temperature has been reached, slowly turn the 'set temp' knob anticlockwise until the 'heater' lamp is extinguished and leave the knob at that setting.

If the measured temperature of the solution exceeds the required value, do not turn on the tank, but allow to cool, agitating gently but regularly until the temperature has fallen to the required value. At this point refer to the paragraph above regarding thermostat setting and carry out those instructions, thereby enabling the heater to maintain the required temperature.

Board processing

Place the board to be processed in the basket which is attached to the underside of the tank lid. The board should be tilted so that one top edge contacts the side of the basket and one bottom edge contacts the base of the basket, allowing the process chemicals maximum access to both sides of the board. Lower the basket into the solution, taking care not to splash. Allow the board to remain in the solution for the time stipulated in the paragraph headed 'Solution temperatures and processing times', or in the supplier's instructions if using commercial chemical preparations.

Where high resolution is required in the 'development' process due to a high density of narrow tracks it may be beneficial to experiment with times and temperatures using small test pieces until the optimum time/temperature combination is determined.

RS data

To remove the board from the solution, lift the lid and basket vertically, taking care not to splash. Allow the solution to drain off the board and basket back into the tank before transferring the board to the washing process.

Spray wash tank

(550-381)

This tank is suitable for cold water spray rinsing of process chemicals from printed circuit boards.

Installation

The tank must be connected to a cold water supply and drain. Suitable fittings are supplied with the tank.

Supply connection

The length of flexible ½in pipe should be used. One end should be push fitted onto the stub of pipe at the top of the tank (on the rear face) and secured with the hose clip provided. Fitting the flexible pipe to the stub will be facilitated if the end of the flexible pipe is first softened by immersion in hot water for a few seconds. If installing the tank in cold conditions it is **essential** that this softening process is used to prevent fracture of the stub or internal damage to the tank.

When installing a multiple tank processing facility involving more than one spray wash tank, all the wash tanks may be operated from one supply pipe by utilising the 'Y' coupling piece supplied with each wash tank. Cut the flexible pipe with a sharp knife at a convenient point. This should be done before fitting to the tank to avoid unnecessarily stressing the tank stub. Ensure that any fragments of pipe caused by cutting are removed from the pipe before connection, otherwise the small holes in the spray wash bars may become blocked. For this reason the use of a hacksaw to cut the flexible pipe is not recommended, as the removal of the many small particles generated by sawing cannot be guaranteed. The 'pipe feeds' to a multiple wash tank installation should be arranged so that each tank is fed via approximately the same total length of pipe and number of pipe couplings, so that the working pressure at all wash tanks is similar. The cut end of the flexible pipe is a push fit to the appropriate stub of the 'Y' piece. Immersion of the end of the flexible pipe in hot water to soften it prior to fitting to the 'Y' piece is recommended. The flexible pipe should be retained to the 'Y' piece by tightening the locking ring (hand pressure is sufficient).

The other end of the flexible pipe is fitted with a tap adaptor which is push fitted onto a standard ½in BSP tap. Tighten the securing clip after fitting to ensure that the adaptor is not forced off the tap by water pressure.

Drain connection

Connection to drain is made via the 1¼in drain pipe stub located at the bottom of the tank on the rear face. A 1¼in 'O-ring' type drain elbow is provided to facilitate connection to an existing drain pipe. This elbow is a push fit onto the drain stub, also to standard 1¼in drain pipe.

Matching drain pipe and fittings are readily available from plumbers' merchants.

When installing more than one spray wash tank in the same facility, these may be connected to a common drain pipe but note that it is **essential** that the drain pipes are routed so that there is a continual fall in level away from each tank. Failure to observe this requirement may result in one wash tank partially filling with waste water from the other wash tank(s).

Board washing

Turn on the tap gradually so that there is a steady flow of water from the wash bars, sufficient to rinse the boards gently. Forced (high pressure) washing is not only unnecessary, it is wasteful of water and may be detrimental to the developed photo-resist prior to etching, as the resist is then in a delicate condition and may be lifted off the board by high pressure washing. The washing water may be allowed, if required, to flow continuously during the processing of a batch of boards.

Place the board to be washed in the basket which is attached to the underside of the tank lid. Lower the basket into the wash tank. Allow the board to remain in the wash tank for 15-30 seconds. When removing the board from the wash tank, lift the lid and basket vertically and allow excess water to drain off the board and basket back into the tank. If traces of processing chemicals remain on the board surface the washing process may be repeated.

Ensure that the board surface will not be contaminated with dirt or chemical residues from protective gloves etc. when removing the board from the basket and transferring to the next process or the storage rack.

Chemicals

The following chemicals are available for the p.c.b. modular preparation system:

Ferric chloride hexahydrate crystals	2kg	551-277
	10kg	551-283
Sodium hydroxide crystals	480g	551-299

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RS data

LED Display with integral counter

Stock number 586-992

A red 0.27 in high 7-segment LED display containing a BCD counter, four-bit latch and decoder driver. The BCD counter has dual count inputs providing full look-ahead, enabling high speed fully synchronous multi-digit counter systems to be realised without the need for external logic. Other features include ripple blanking input/outputs for leading or trailing zero suppression, asynchronous parallel clear and latch strobe which permits counter to acquire data for display updating whilst viewing current display count. The internal latched BCD data are available for external processing on parallel data lines. The clock input is positive edge triggered and will count input frequencies up to 18MHz (typically). All inputs and outputs are TTL compatible.

Features

- High luminous intensity
- Easy system interface
- Wide viewing angle
- Internal TTL MSI chip with:- counter, latch, decoder and driver
- Constant current drive for LEDs
- Left decimal point

Absolute maximum ratings

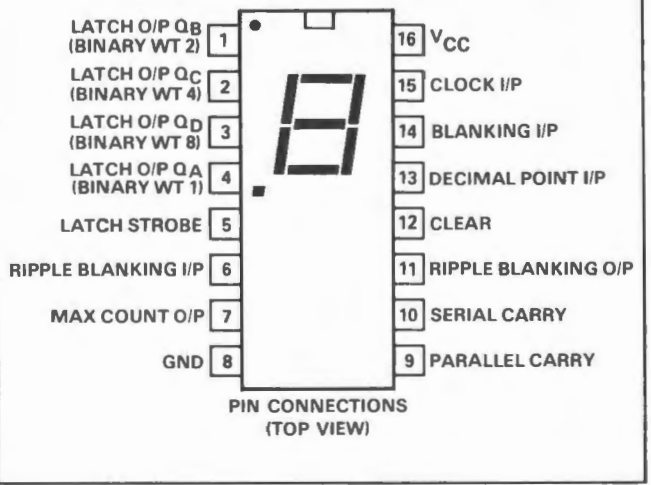
Supply voltage, V_{CC} (see Note 1):
- Continuous — 5.5V
- Nonrepetitive peak, $t_w \leq 100ms$ — 7V

Input voltage (see Note 1) — 5.5V

Operating case temperature range (see Note 2) — 0°C to 85°C

Storage temperature range — –25°C to 85°C

Notes:
1. Voltage values are with respect to network ground terminal.
2. Case temperature is the surface temperature of the plastic encapsulant measured directly over the integrated circuit. Forced air cooling may be required to maintain this temperature.



PIN CONNECTIONS (TOP VIEW)

Recommended operating conditions

Parameter			Min	Typ	Max	Unit
Supply Voltage, V_{CC}			4.75	5	5.25	V
Normalised Fan-Out from Each Output, N (to 74 Series integrated Circuits)	Low Logic Level	Q_A, Q_B, Q_C, Q_D, RBO			3	
		Maximum Count			5	
	High Logic Level	RBO			3	
		Q_A, Q_B, Q_C, Q_D			6	
		Maximum Count			10	
Clock Pulse Width, $t_{w(clock)}$		High Logic Level	25			ns
		Low Logic Level	55			
Clear Pulse Width, $t_{w(clear)}$			25			ns
Latch Strobe Pulse Width, $t_{w(latch\ strobe)}$			45			ns
Setup Time, t_{setup} (see Note 3)		Serial Carry and Parallel Carry	30			ns
		Clear Inactive State	60			

Note 3: Minimum setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognised must be maintained at the input to ensure its recognition.

Operating characteristics at 25°C case temperature

Parameter			Test Conditions	Min	Typ‡	Max	Unit
I_v	Luminous Insensity (See Note 4)	Figure 8	V_{CC} = 5V	700	1200		μcd
		Decimal Point		40	70		μcd
λ_P	Wavelength at Peak Emission		V_{CC} = 5V. See Note 5	640	660	680	nm
$\Delta\lambda$	Spectral Bandwidth		V_{CC} = 5V. See Note 5		20		nm
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IK}	Input Clamp Voltage		V_{CC} = 4.75V, I_I = –12mA			–1.5	V
V_{OH}	High Level Output Voltage	RBO	V_{CC} = 4.75V, I_{OH} = =120μA	2.4			V
		Q_A, Q_B, Q_C, Q_D	V_{CC} = 4.75V, I_{OH} = –240μA				
		Maximum Count	V_{CC} = 4.75V, I_{OH} = –400μA				
V_{OL}	Low-Level Output Voltage (See Note 6)	Q_A, Q_B, Q_C, Q_D, RBO	V_{CC} = 4.75V, I_{OL} = 4.8mA			0.4	V
		Maximum Count	V_{CC} = 4.75V, I_{OL} = 8mA				
I_I	Input Current at Maximum Input Voltage		V_{CC} = 5.25V, V_I = 5.5V			1	mA
I_{IH}	High-Level Input Current	Serial Carry	V_{CC} = 5.25V, V_I = 2.4V			40	μA
		RBO Node		–0.12	–0.5		mA
		Other Inputs				20	μA
I_{IL}	Low-Level Input Current	Serial Carry	V_{CC} = 5.25V, V_I = 0.4V			–1.6	mA
		RBO Node			–1.5	–2.4	
		Other Inputs				–0.8	
I_{OS}	Short-Circuit Output Current	Q_A, Q_B, Q_C, Q_D	V_{CC} = 5.25V	–9		–27.5	mA
		Maximum Count		–15		–55	
I_{CC}	Supply Current		V_{CC} = 5.25V, See Note 5		120	200	mA

‡ All typical values are at V_{CC} = 5V.

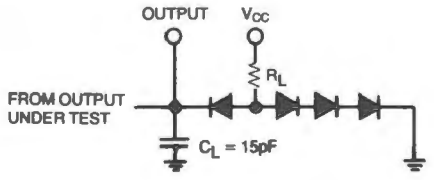
Notes: 4. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (International Commission on illumination) eye response curve.
5. These parameters are measured with all LED segments and the decimal point on.
6. This parameter is measured with the display blanked.

Switching characteristics V_{CC} = 5V, T_C = 25°C

Parameter§	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
f_{max}				12	18		MHz
t_{PLH}	Serial Look-Ahead	Maximum Count	C_L = 15pF, R_L = 560Ω See Figure 1		12		ns
t_{PHL}					23		
t_{PLH}	Clock	Maximum Count			26		ns
t_{PHL}					29		
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D	C_L = 15pF, R_L = 1.2kΩ, See Figure 1		28		ns
t_{PHL}					38		
t_{PHL}	Clear	Q_A, Q_B, Q_C, Q_D			57		ns

§ f_{max} = Maximum clock frequency.
t_{PLH} = Propagation delay time, low-to-high-level output.
t_{PHL} = Propagation delay time, high-to-low-level output.

Figure 1 **Load circuit**



Notes: A. C_L includes probe and jig capacitance.
B. All Diodes are IN4148.

Description

These internally-driven seven-segment light-emitting-diode (LED) displays contain a BCD counter, a four-bit latch, and a decoder/LED driver in a single 16-pin package. A description of the functions of the inputs and outputs of these devices follows:

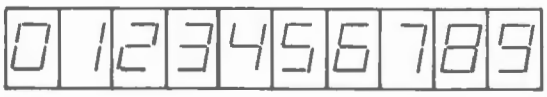
Function	Pin No.	Description
CLEAR INPUT	12	When low, resets and holds counter at 0. Must be high for normal counting.
CLOCK INPUT	15	Each positive-going transition will increment the counter provided that the circuit is in the normal counting mode (serial and parallel count enable inputs low, clear input high).
PARALLEL COUNT ENABLE INPUT (PCEI)	9	Must be low for normal counting mode. When high, counter will be inhibited. Logic level must not be changed when the clock is low.
SERIAL COUNT ENABLE INPUT (SCEI)	10	Must be low for normal counting mode, also must be low to enable maximum count output to go low. When high, counter will be inhibited and maximum count output will be driven high. Logic level must not be changed when the clock is low.
MAXIMUM COUNT OUTPUT	7	Will go low when the counter is at 9 and serial count enable input is low. Will return high when the counter changes to 0 and will remain high during counts 1 through 8. Will remain high (inhibited) as long as serial count enable input is high.
LATCH STROBE INPUT	5	When low, data in latches follow the data in the counter. When high, the data in the latches are held constant, and the counter may be operated independently.
LATCH OUTPUTS (Q_A, Q_B, Q_C, Q_D)	4, 1, 2, 3	The BCD data that drives the decoder can be stored in the 4-bit latch and is available at these outputs for driving other logic and/or processors. The binary weights of the outputs are: $Q_A = 1$, $Q_B = 2$, $Q_C = 4$, $Q_D = 8$.
DECIMAL POINT INPUT	13	Must be high to display decimal point. The decimal point is not displayed when this input is low or when the display is blanked.
BLANKING INPUT (BI)	14	When high, will blank (turn off) the entire display and force RBO low. Must be low for normal display. May be pulsed to implement intensity control of the display.
RIPPLE-BLANKING INPUT (RBI)	6	When the data in the latches is BCD 0, a low input will blank the entire display and force the RBO low. This input has no effect if the data in the latches is other than 0.
RIPPLE-BLANKING OUTPUT (RBO)	11	Supplies ripple-blanking information for the ripple-blanking input of the next decade. Provides a low if BI is high, or if RBI is low and the data in the latches is BCD 0; otherwise, this output is high. This pin has a resistive pull-up circuit suitable for performing a wire-AND function with any open collector output. Whenever this pin is low the entire display will be blanked; therefore, this pin may be used as an active-low blanking input.

The TTL MSI circuits contain the equivalent of 86 gates on a single chip. Logic inputs and outputs are completely TTL/DTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard 74 Series TTL input. The serial-carry input, actually two internal loads, is rated as one standard 74 Series load.

The logic outputs, except RBO, are active pull-up, and the latch outputs Q_A, Q_B, Q_C, and Q_D are each capable of driving three standard 74 Series loads at a low logic level or six loads at a high logic level while the maximum-count output is capable of driving five 74 Series loads at a low logic level or ten loads at a high logic level. The RBO node with passive pull-up serves as a ripple-blanking output with the capability to drive three 74 Series loads.

The LED driver outputs are designed specifically to maintain a relatively constant on-level current of approximately seven milliamperes through each LED segment and decimal point. All inputs are diode-clamped to minimise transmission-line effects, thereby simplifying system design. Maximum clock frequency is typically 18 megahertz and power dissipation is typically 600 milliwatts with all segments on.

The display format is as follows:



The displays may be interconnected to produce an n-digit display with the following features:

- Ripple-blanking input and output for blanking leading or trailing zeros
- Floating-decimal-point logic capability
- Overriding blanking for suppressing entire display or pulse-modulation of LED brightness
- Dual count-enable inputs for parallel look-ahead and serial ripple logic to build high-speed fully synchronous, multidigit counter systems with no external logic, minimising total propagation delay from the clock to the last latch output
- Provision for ripple-count cascading between packages
- Positive-edge-triggered synchronous BCD counter
- Parallel BCD data outputs available to drive logic processors or remote slaved displays simultaneously with data being displayed
- Latch strobe input allows counter to operate while a previous data point is displayed
- Reset to zero capability with clear input.

Typical characteristics

Figure 2 **Relative spectral characteristic**

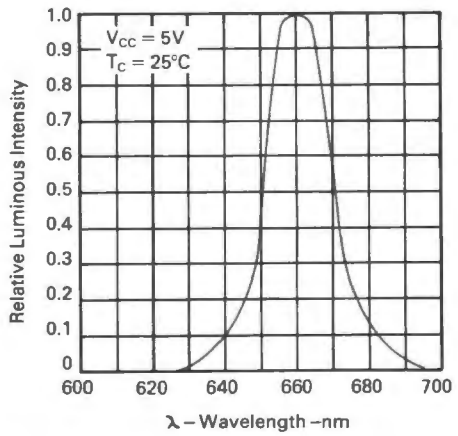
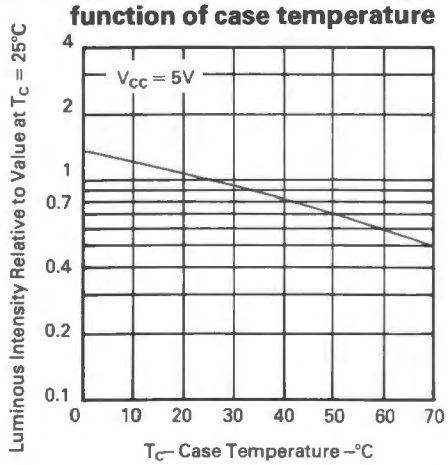


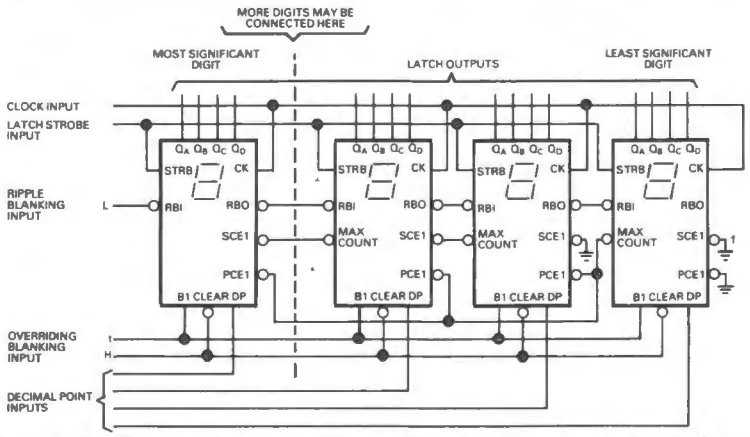
Figure 3 **Relative luminous intensity as a function of case temperature**



Typical application

This application demonstrates how the displays may be cascaded for N-bit display applications. It features:

Synchronous, look-ahead counting
Ripple blanking for leading zeros
Overriding blanking for total suppression or intensity modulation of display
Direct parallel clear
Latch strobe permits counter to acquire data for the next display while viewing current display.



† The serial carry input of the least significant digit is normally grounded, however, it may be used as a count-enable control for the entire counter (high to disable, low to count) provided the logic level on this pin is not changed while the clock line is low or false counting may result.

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RS data

High power operational amplifiers 759 and 165

Stock numbers 303-258 and 301-599

Two high power operational amplifiers featuring high current output stages. Ideally suited for use in applications where conventional operational amplifier output current (typically 16mA) is insufficient.

759

An operational amplifier with characteristics similar to a 741 but featuring a power output stage capable of providing a minimum of 325mA output current into a 50Ω load. Operation is from a single or dual rail supply and the input common mode voltage range includes the ground or negative rail. This device features internal current limiting, thermal shutdown protection and safe operating area protection for increased reliability. Suited for a wide range of applications including voltage regulators, servo amplifiers, power drivers, etc. 4-lead package with heat sink tab.

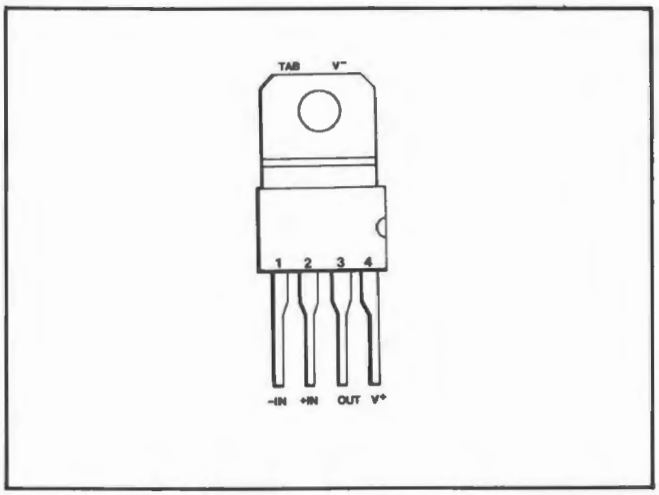
Absolute maximum ratings

Supply voltage (between V_+ and V_-) _____ 36V
Differential input voltage (see note) _____ 30V
Input voltage (see note) _____ (V_- –0.3V) to V_+
Operating junction temperature range _____ 0°C to +125°C
Storage temperature range _____ –55°C to +150°C
Lead temperature (soldering 10s) _____ 260°C

Note: For a supply voltage less than 30V between V_+ and V_-, the absolute maximum input voltage is equal to the supply voltage.

Features

- Minimum output current of 325mA
- Internal short-circuit current limiting
- Internal thermal overload protection
- Safe area protection of internal output transistors
- Input common mode voltage range includes ground or negative supply.



Electrical characteristics $V_S = \pm 15V$, $T_J = 25°C$ unless otherwise specified

Characteristic		Condition	Min.	Typ.	Max.	Unit
Input Offset Voltage		$R_S \leq 10k\Omega$		1.0	6.0	mV
Input Offset Current				5.0	50	nA
Input Bias Current				50	250	nA
Input Resistance			0.25	1.5		MΩ
Input Voltage Range			+13 to $-V_S$	+13 to $-V_S$		V
Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_{OUT} = \pm 10V$	25	200		V/mV
Supply Current				12	18	mA
Peak Output Current		$3V \leq \lvert V_S - V_{OUT} \rvert < 10V$	±325	±500		mA
Short Circuit Current		$\lvert V_S - V_{OUT} \rvert = 30V$		±200		mA
Transient Response Unity Gain)	Risetime	$R_L \geq 50\Omega$		300		ns
	Overshoot	$R_L \geq 50\Omega$		10		%
Slew Rate		$R_L \geq 50\Omega$		0.5		V/μs
Unity Gain Bandwith				1.0		MHz

Characteristic	Condition	Min.	Typ.	Max.	Unit
The following specifications apply for $-55°C \leq T_J \leq 125°C$					
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5	mV
Input Offset Current				100	nA
Input Bias Current				400	nA
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	80	100		dB
Output Voltage Swing	$R_L \geq 50\Omega$	±10	±12.5		V

Thermal resistance

Typ	Max	Typ	Max
θ_{JC} °C/W	θ_{JC} °C/W	θ_{JA} °C/W	θ_{JA} °C/W
8.0	12	75	80

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

(Without a heat sink)

$\theta_{CA} = \theta_{CS} + \theta_{SA}$

Solving for T_J: $T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where: T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction to ambient thermal resistance
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink thermal resistance
θ_{SA} = Heat sink to ambient thermal resistance

Heat sinking

The RS759 is designed to be attached by the tab to a heat sink. The heat sink can be either; a conventional type (see current RS catalogue) or a piece of metal such as the equipment chassis. It is important to remember that the negative power supply connection to the op-amp must be made through the tab. Furthermore, adequate heat sinking must be provided to keep the junction temperature below 125°C under worse case load and ambient temperature conditions.

Typical performance curves

Figure 1 **Open loop gain and phase response as a function of frequency**

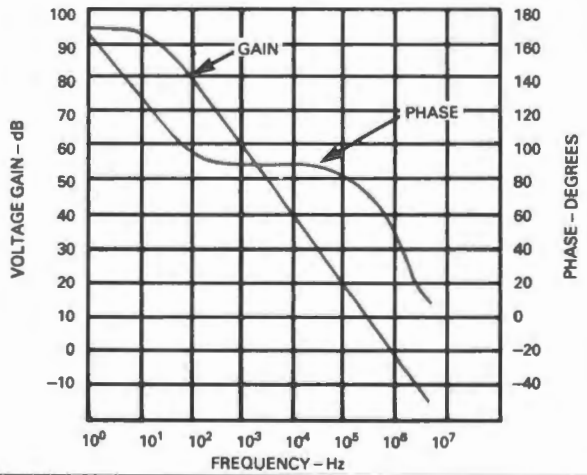


Figure 2 **Output voltage as a function of frequency**

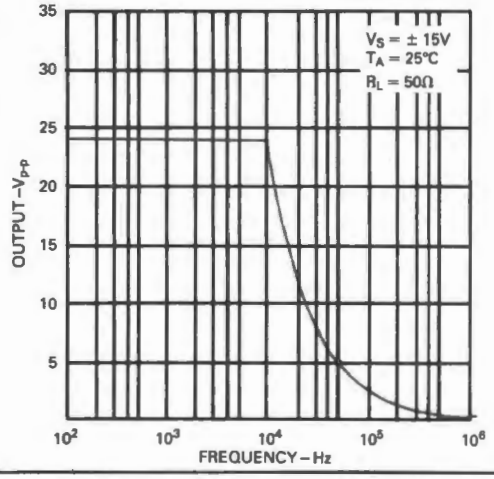


Figure 3 **P-P output voltage as a function of load resistance**

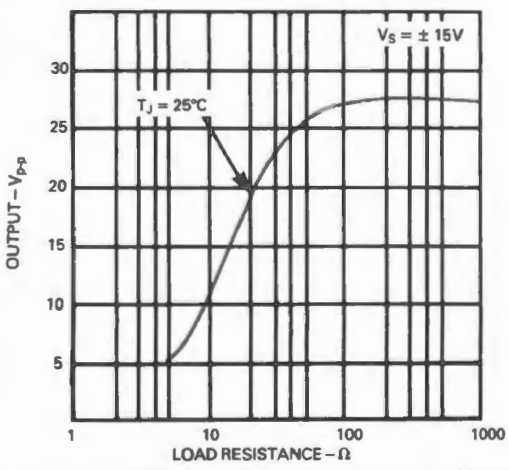


Figure 4 **Total harmonic distortion as a function of frequency**

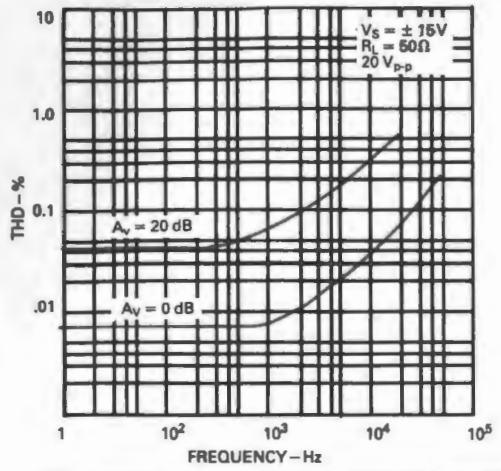


Figure 5 **Total harmonic distortion as a function of power output**

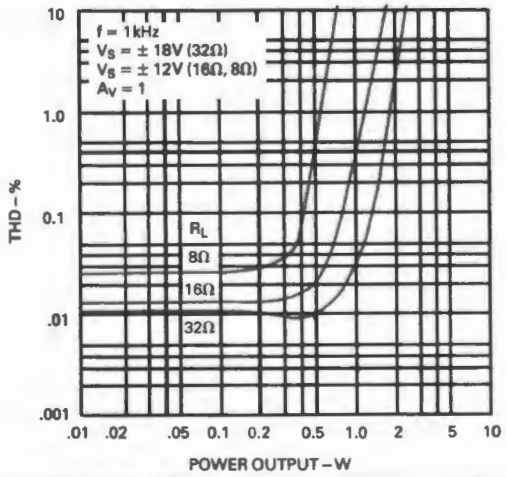
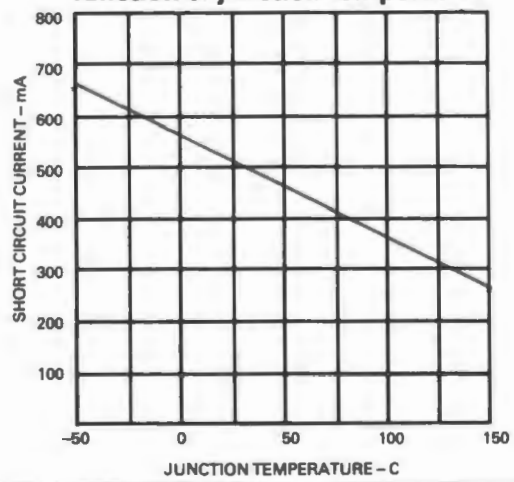


Figure 6 **Output short circuit current as a function of junction temperature**



Typical applications

Figure 7 **Adjustable voltage regulator**

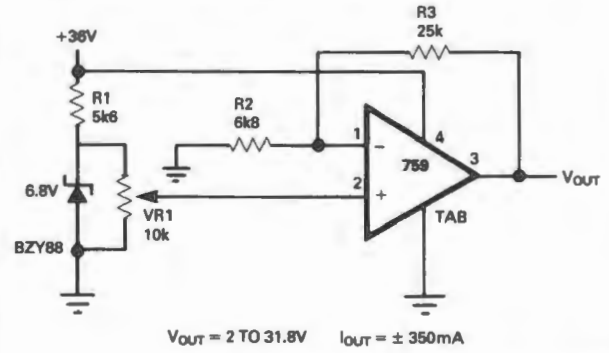


Figure 8 **Offset null circuit**

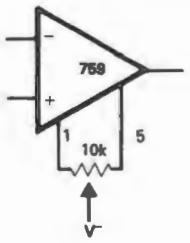


Figure 9 **Paralleling 759 op-amp**

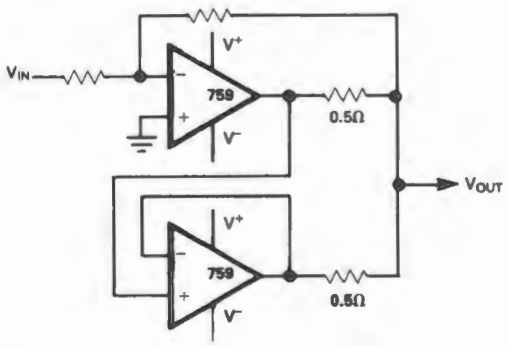


Figure 10 **Headphone amplifiers**

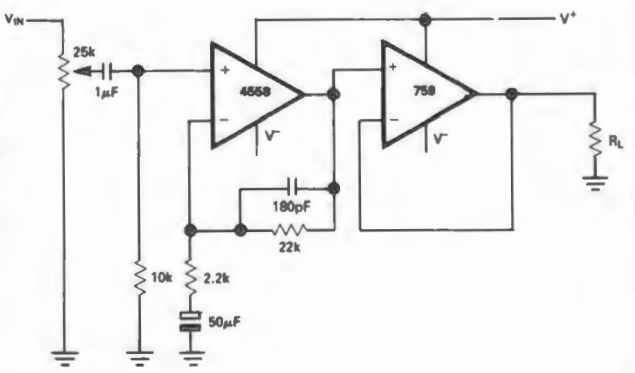
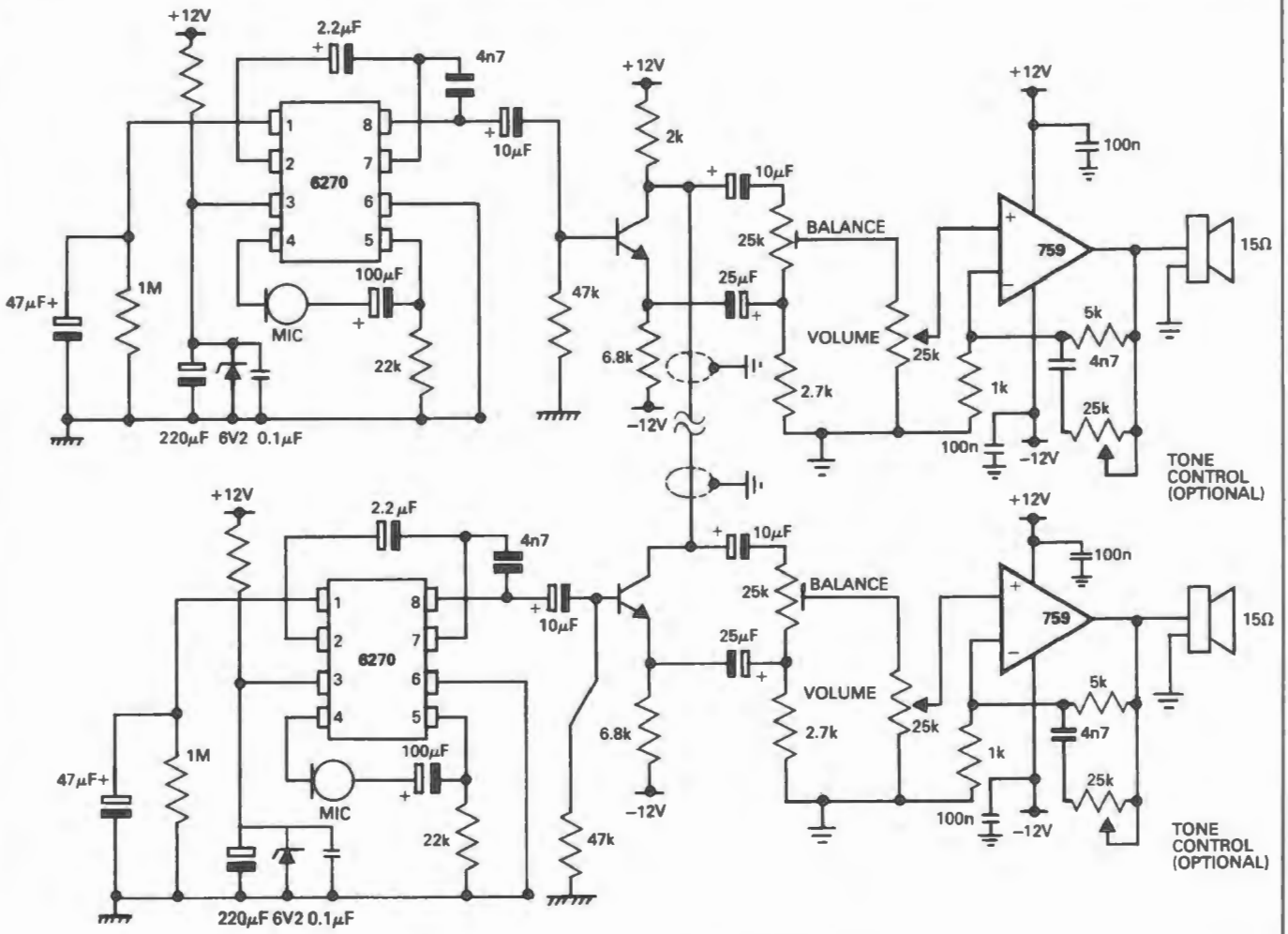
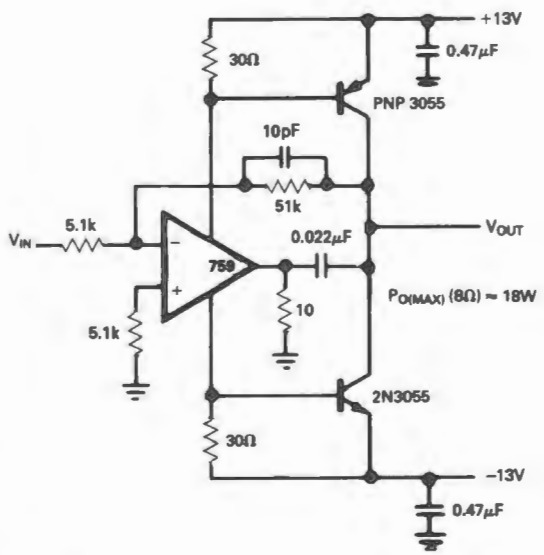


Figure 11 **Two way, two wire intercom system**



Note: The balance trimmers should be set for minimum distortion.

Figure 12 **High slew rate power OP amp/audio amp**



Features
- High slew rate 9V/μs
- High 3dB power bandwidth 85kHz
- 18 Watts peak output power into an 8Ω Load.
- Low distortion – 0.2%, 10 VRMS, 1kHz into 8Ω.

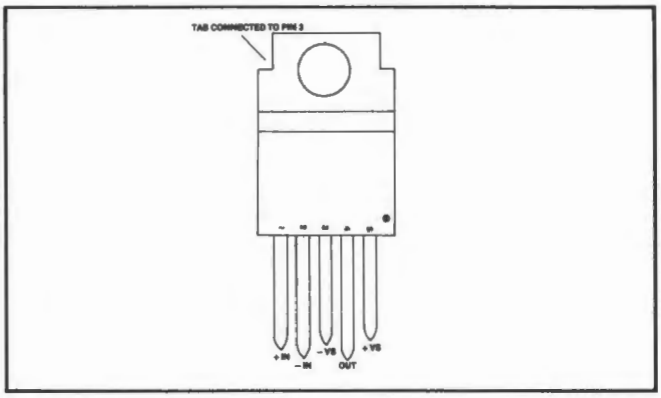
Design Consideration
- $A_V \geq 10$

165

The RS165 is a high power operational amplifier providing a maximum of 3A output current. Incorporating safe operating area and thermal protection the device is ideally suited for use in a wide range of applications where an op-amp/power booster combination would normally be used. These include: servo amplifiers, power supplies, audio amplifiers, power oscillators etc.

Features

- Maximum output current 3A
- Large common mode and differential mode ranges
- Internal thermal overload protection
- Safe operating area protection.



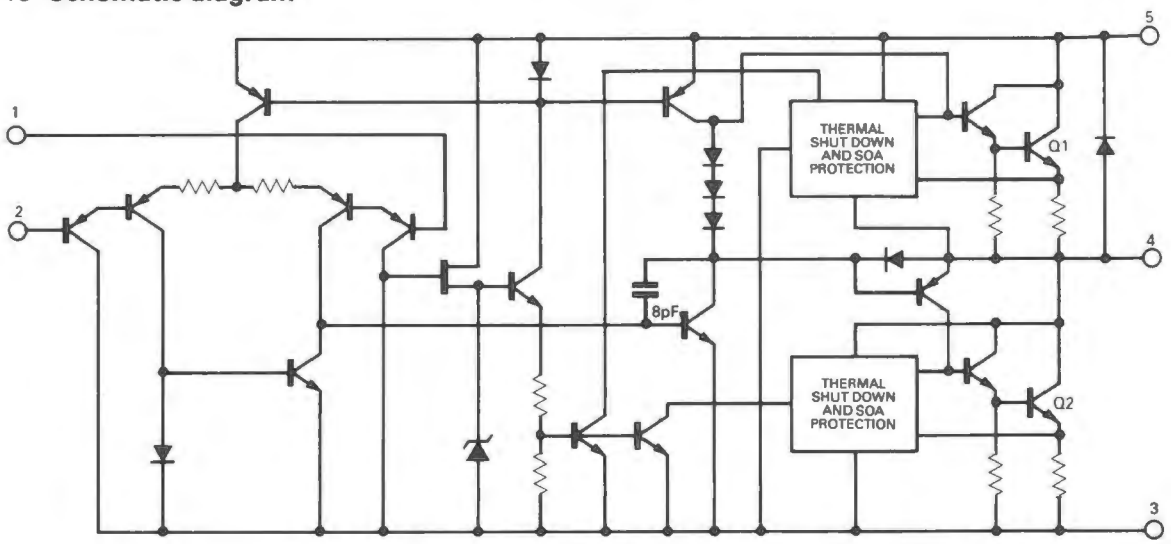
Absolute maximum ratings

Supply voltage (between V^+ and V^-) ——— 36V
Differential input voltage ——— 30V
Input voltage ——— V_S
Peak output current (internally limited) ——— 3.5A
Power dissipation at T_{case} = 90°C ——— 20W
Storage and junction temperature —— −40 to +150°C

Electrical characteristics (V_S = ±15V, T_{amb} = 25°C unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply voltage		±6		±18	V
Quiescent drain current			40	60	mA
Input bias current	V_S = ± 18V		0.2	1	µA
Input offset voltage			±2	±10	mV
Input offset current			±20	±200	nA
Slew-rate	G_V = 10		8		V/µs
	G_V = 1 (See figure 21)		6		
Output voltage swing	f = 1kHz I_p = 0.3A		27		V_{pp}
	f = 1kHz I_p = 3A		24		V_{pp}
	f = 10kHz I_p = 0.3A		27		V_{pp}
	f = 10kHz I_p = 3A		23		V_{pp}
Input resistance (pin 1)	f = 1kHz	100	500		KΩ
Voltage gain (open loop)			80		dB
Input noise voltage	B = 10 to 10000Hz		2		µV
Input noise current			100		pA
Common mode rejection	$R_g \leq 10k\Omega$ G_V = 30dB		70		dB
Supply voltage rejection	$Rg = 22k\Omega$, $V_{ripple} = 0.5\ V_{rms}$, $f_{ripple} = 100Hz$, G_V = 10		60		dB
	$Rg = 22k\Omega$, $V_{ripple} = 0.5\ V_{rms}$, $f_{ripple} = 100Hz$, G_V = 100		40		dB
Efficiency	f = 1kHz, $R_L = 4\Omega$, I_p = 1.6A; P_O = 5W		70		%
	f = 1kHz, $R_L = 4\Omega$, Ip = 3A; P_O = 18W		60		%
Thermal shut-down case temperature	P_{tot} = 12W		110		°C
	P_{tot} = 6W		130		
Thermal resistance junction to case				3	°C/W

Figure 13 **Schematic diagram**



Heat sinking

The RS 165 is designed to be attached by the tab to a heat sink. The heat sink can be either; a conventional type (see current RS catalogue) or a piece of metal such as the equipment chassis. It is important to remember that the negative power supply is also connected to this pin. Furthermore adequate heat sinking must be provided to keep the junction temperature below 150° under worse case load and ambient temperature conditions.

Figure 14 **Open loop frequency response**

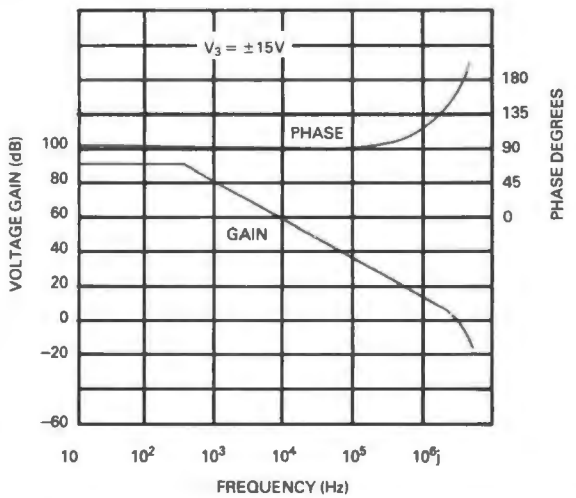


Figure 15 **Closed-loop frequency response (circuit of Figure 21)**

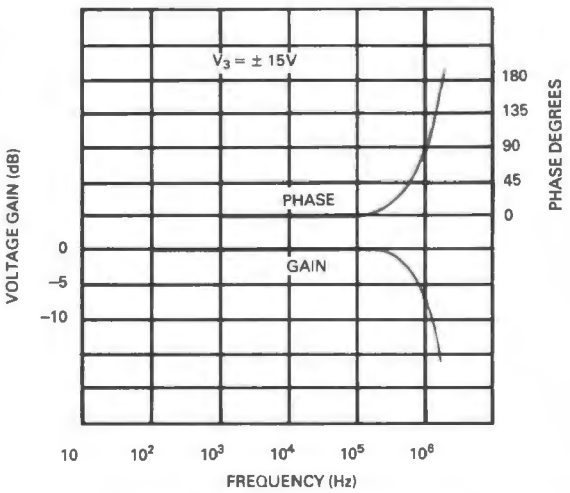


Figure 16 **Large signal frequency response**

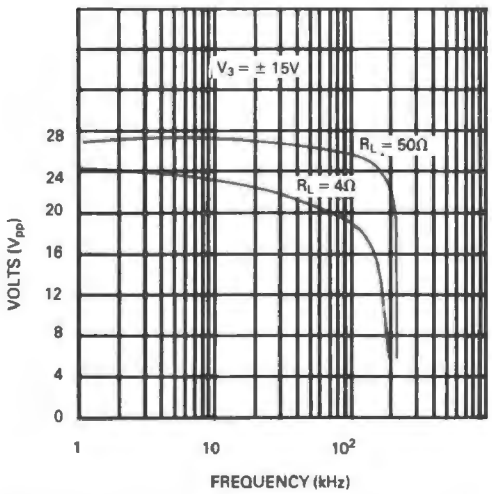


Figure 17 **Maximum output current vs. voltage (V_{CE}) across each output transistor**

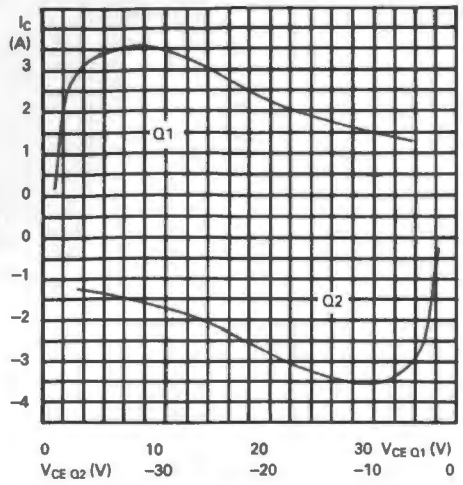


Figure 18 **Safe operating area and collector characteristics of the protected power transistor**

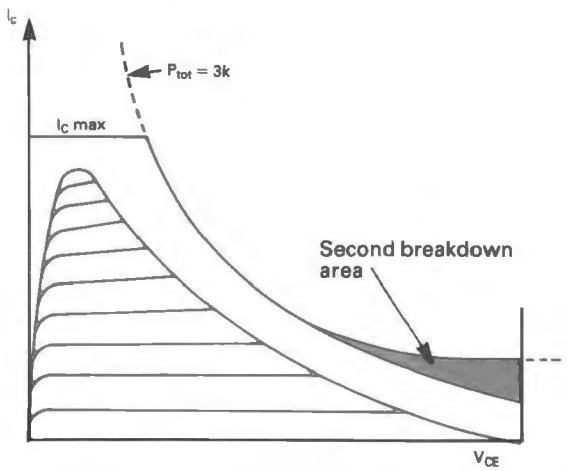
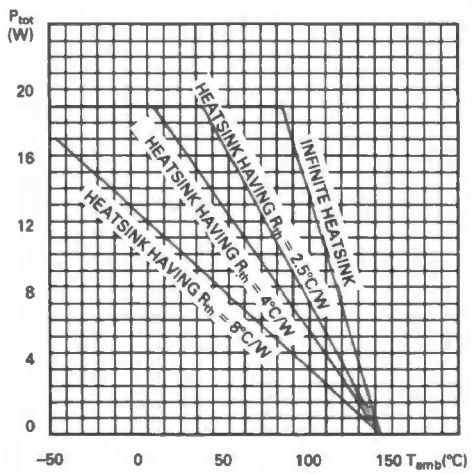


Figure 19 **Maximum allowable power dissipation vs. ambient temperature.**



Typical applications

Figure 20 **Basic amplifier**

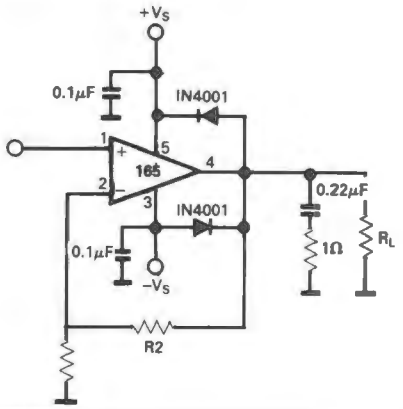


Figure 21 **Unity gain configuration**

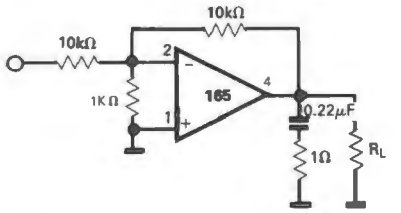


Figure 22 **Bidirectional speed control of DC motor**

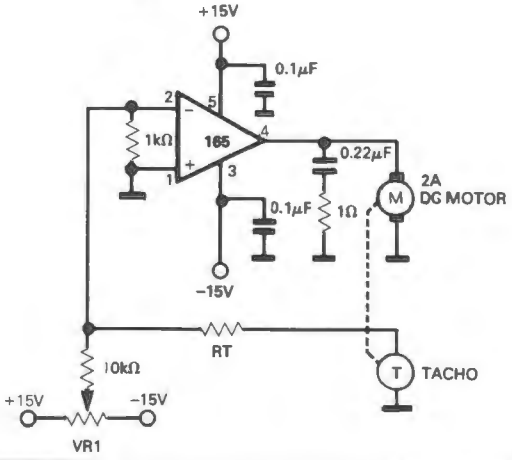
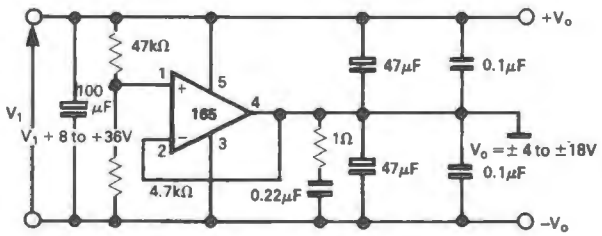
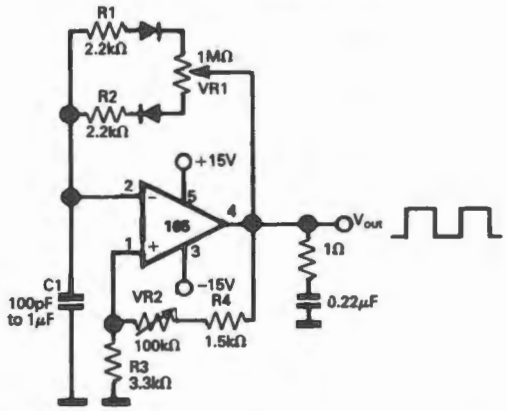


Figure 23 **Split power supply**



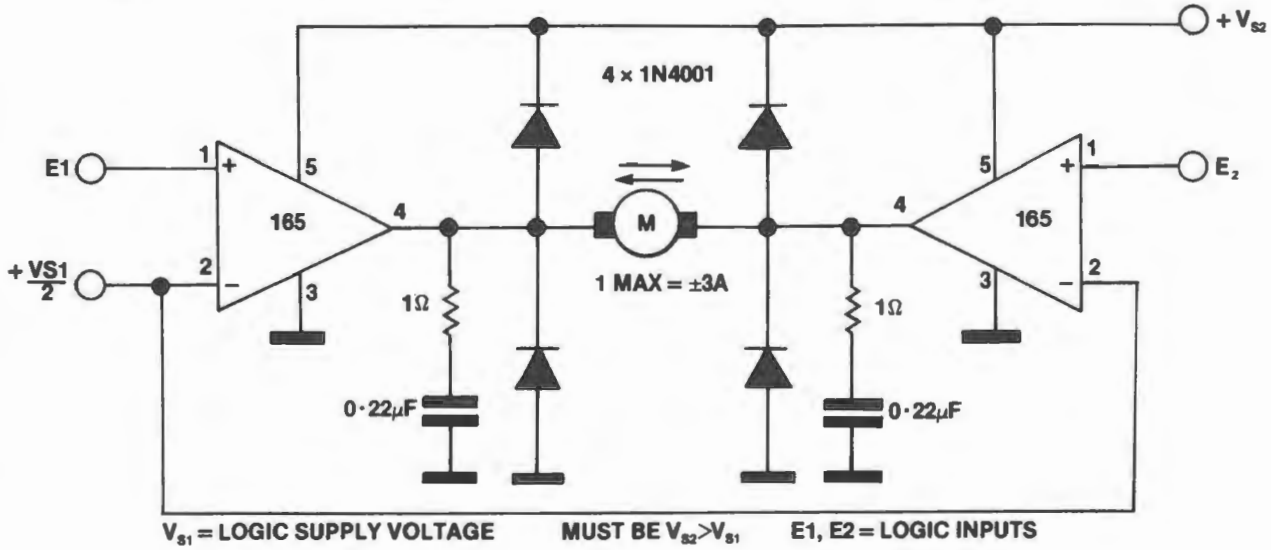
RS data

Figure 24 **Power squarewave oscillator with independent adjustments for frequency and duty cycle.**



VR1: duty-cycle adjust
VR2: frequency adjust (f = 700Hz with C1 = 10nF, VR3 = 100kΩ, f = 25Hz with C1 = 10nF, VR2 = 0)

Figure 25 **Bidirectional DC motor control with TTL/CMOS/μP compatible inputs**



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RS data

Line drivers and receivers

1488 Line driver

The 1488 is a quad line driver containing 3 NAND function drivers and one inverting driver. The device meets the specification of the Electronic Industries Association standard RS232C. The 1488 is used to interface data terminals with data communications equipment.

Features

- Meets specification of EIA RS232C.
- Current-limited output typically 10mA.
- Minimum power-off output impedance of 300Ω.
- Slew rate control via load capacitor.
- Input compatible with most TTL and DTL circuits.

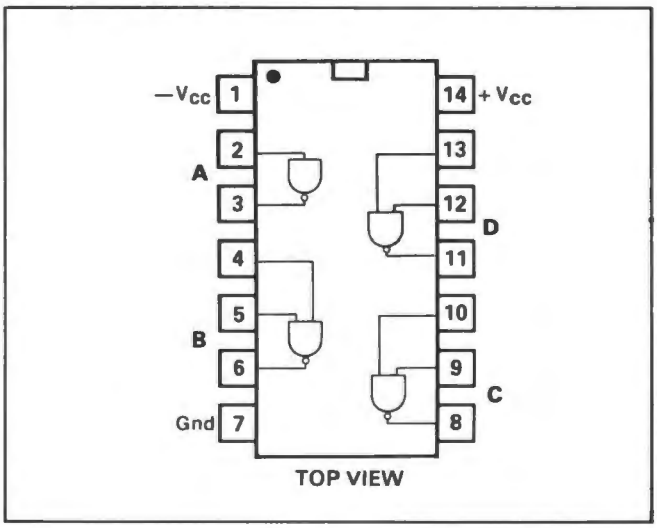
Absolute maximum ratings

(at 25°C unless otherwise noted)

Power supply voltages:

V_{CC+}	+15V
V_{CC-}	−15V
Input voltage range (V_{IR})	−15V dc to +7.0V dc
Output signal voltage	±15V dc
Continuous total power dissipation (see note)	800mW
Operating temperature	0°C to +70°C
Storage temperature	−65°C to +150°C
Maximum lead temperature (soldering, 6 seconds)	260°C

Note:
Above 60°C ambient temperatures, derate linearly at 8.3mW/°C.



Electrical characteristics

Electrical characteristics over operating free-air temperature range, V_{CC+} = 9V, V_{CC-} = −9V (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.†	Max.	Unit
V_{IH}	High-level input voltage			1.9			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{IL} = 0.8V, R_L = 3kΩ	V_{CC+} = 9V, V_{CC-} = −9V	6	7		V
			V_{CC+} = 13.2V, V_{CC-} = −13.2V	9	10.5		
V_{OL}	Low-level output voltage	V_{IH} = 1.9V, R_L = 3kΩ	V_{CC+} = 9V V_{CC-} = −9V		−7	−6	V
			V_{CC+} = 13.2V, V_{CC-} = −13.2V		−10.5	−9	
I_{IH}	High-level input current	V_I = 5V				10	μA
I_{IL}	Low-level input current	V_I = 0			−1	−1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level♦	V_I = 0.8V	V_O = 0	−6	−10	−12	mA
$I_{OS(L)}$	Short-circuit output current at low level♦	V_I = 1.9V,	V_O = 0	6	10	12	mA
r_o	Output resistance, power off	V_{CC+} = 0, V_O = −2V to 2V	V_{CC-} = 0,	300			Ω

Electrical characteristics

Electrical characteristics over operating free-air temperature range, V_{CC+} = 9V, V_{CC-} = –9V (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.†	Max.	Unit
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 9V, No load	All inputs at 1.9V		15	20	mA
			All inputs at 0.8V		4.5	6	
		V_{CC+} = 12V, No load	All inputs at 1.9V		19	25	
			All inputs at 0.8V		5.5	7	
		V_{CC+} = 15V, No load, T_A = 25°C	All inputs at 1.9V			34	
			All inputs at 0.8V			12	
I_{CC-}	Supply current from V_{CC-}	V_{CC-} = –9V, No load	All inputs at 1.9V		–13	–17	mA
			All inputs at 0.8V			–0.015	
		V_{CC-} = –12V, No load	All inputs at 1.9V		–18	–23	
			All inputs at 0.8V			–0.015	
		V_{CC-} = –15V, No load, T_A = 25°C	All inputs at 1.9V			–34	
			All inputs at 0.8V			–2.5	
P_D	Total power dissipation	V_{CC+} = 9V, No load	V_{CC-} = –9V,			333	mW
		V_{CC+} = 12V, No load	V_{CC-} = –12V,			576	

† All typical values are at T_A = 25°C.
♦ Not more than one output should be shorted at a time.

Switching characteristics V_{CC+} = 9V, V_{CC-} = –9V, T_A = 25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay time, low-to-high-level output			220	350	ns
t_{PHL}	Propagation delay time, high-to low-level output	R_L = 3kΩ, C_L = 15pF,		100	175	ns
t_{TLH}	Transition time, low-to-high-level output (Note 1)			55	100	ns
t_{THL}	Transition time, high-to-low-level output (Note 1)			45	75	ns
t_{TLH}	Transition time, low-to-high-level output (Note 2)	R_L = 3kΩ to 7kΩ, C_L = 2500pF		2.5		μs
t_{THL}	Transition time, high-to-low-level output (Note 2)			3.0		μs

Notes:
1. Measured between 10% and 90% points of output waveform.
2. Measured between +3V and –3V points on the output waveform (EIA RS-232C conditions).

Typical characteristics

Figure 1 **Voltage transfer**

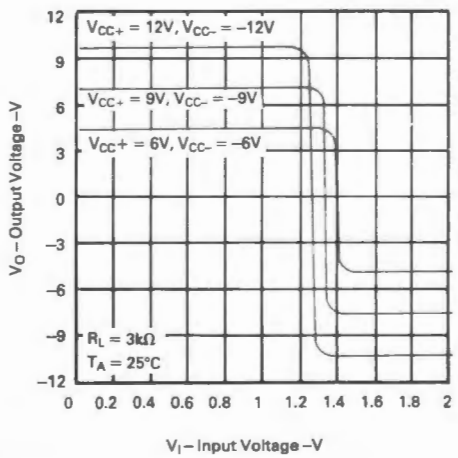


Figure 2 **Output current as a function of output voltage**

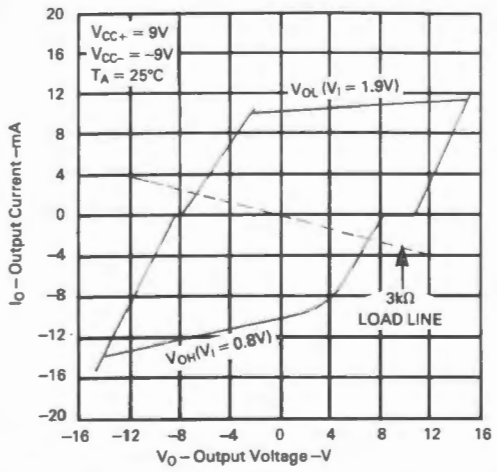
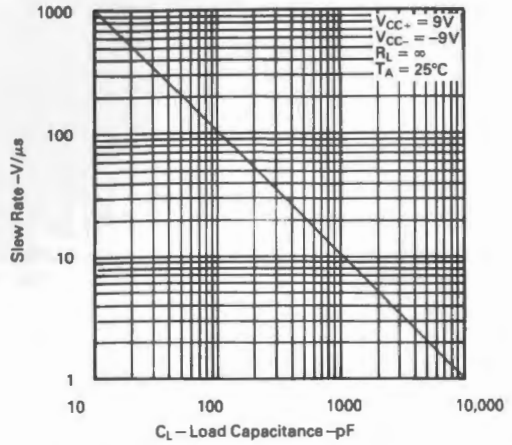
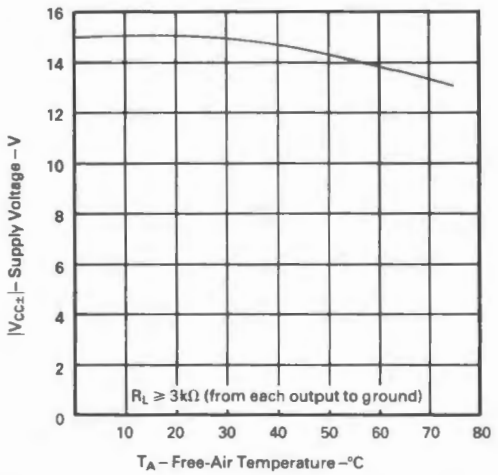


Figure 3 **Slew rate as a function of load capacities**



Thermal characteristics

Figure 4 **Maximum supply voltage as a function of free air temperature**



Typical applications

Figure 5 **Logic translator**

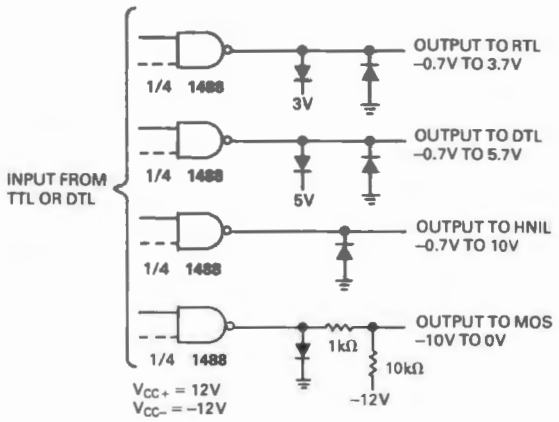
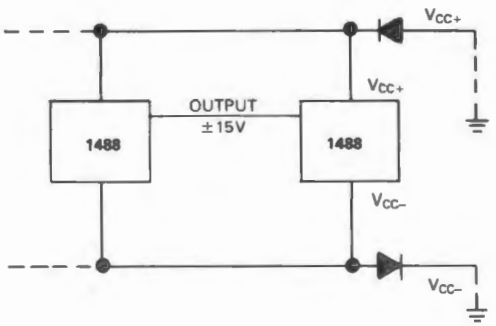


Figure 6 **Power supply protection to meet power-off fault conditions of EIA RS232C**



Diodes placed in series with the V_{CC+} and V_{CC-} leads will protect the 1488 in the fault condition where the device outputs are shorted to ± 15V and the power supplies are at low voltage and provide low-impedance paths to ground.

1489 Line receiver

The 1489 is a quadruple line receiver meeting the requirements of the EIA RS232C standards. A separate response control terminal is provided for each receiver; to shift the input voltage threshold levels via a bias voltage source and/or an external resistor, or to provide input noise filtering via an external capacitor.

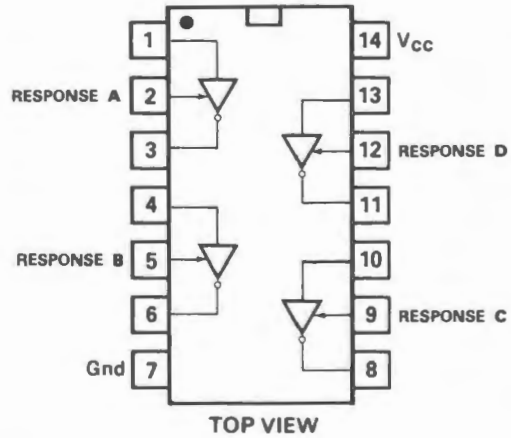
Features

- Meets requirements of EIA RS232C.
- Input resistance 3kΩ to 7kΩ.
- Input signal range ±30V.
- Internal input threshold hysteresis.
- Response control provides:
  Input threshold shifting.
  Input noise filtering.

Absolute maximum ratings

Power supply voltage	+10Vdc
Input voltage range	±30Vdc
Output load current	20mA
Continuous total power dissipation (see note)	800mW
Operating temperature	0°C to 70°C
Storage temperature	–65°C to + 175°C
Maximum lead temperature (soldering, 6 seconds)	260°C

Note:
Above 60°C ambient temperature, derate linearly at 8.3mW/°C.



DC characteristics

V_{CC} = 5.0V ± 1%, response control pin is open, T_A = 0°C to 70°C (unless otherwise noted)

Symbol	Characteristic	Condition	Min.	Typ.	Max.	Unit
I_{IH}	Positive Input Current	V_{IH} = 25V V_{IH} = 3.0V	3.6 0.43		8.3	mA
I_{IL}	Negative Input Current	V_{IL} = –25V V_{IL} = –3.0V	–3.6 –0.43		–8.3	mA
V_{IHL}	Input Turn-on Threshold Voltage	T_A = 25°C, $V_{OL} \leq$ 0.45V	1.0		1.5	V
V_{ILH}	Input Turn-off Threshold Voltage	T_A = 25°C, $V_{OH} \geq$ 2.5V, I_L = –0.5mA	0.75		1.25	V
V_{OH}	Output HIGH Voltage	V_{IH} = 0.75V, I_L = –0.5mA	2.6	4.0	5.0	V
		Input open circuit, I_L = –0.5mA				
V_{OL}	Output LOW Voltage	V_{IL} = 3.0V, I_L = 10mA		0.2	0.45	V
I_{OS}	Output Short-circuit Current			3.0		mA
I_{CC}	Power Supply Current	V_{IH} = 5.0V		20	26	mA
P_C	Power Consumption	V_{IH} = 5.0V		100	130	mW

AC characteristics V_{CC} = 5.0V ± 1%, T_A = 25°C

Symbol	Characteristic	Condition		Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay Time	R_L = 3.9kΩ	C_L = 15pF		25	85	ns
t_{PHL}		R_L = 390Ω			25	50	
t_r	Rise Time	R_L = 3.9kΩ			120	175	ns
t_f	Fall Time	R_L = 390Ω			10	20	

Typical characteristics

Figure 7 **Output voltage as a function of input voltage**

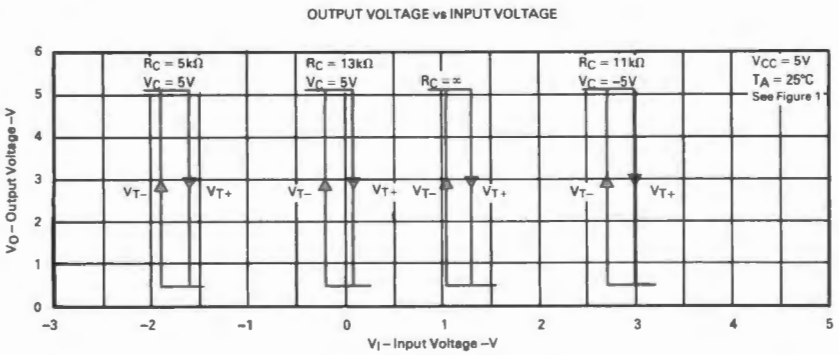


Figure 8 **Input threshold voltage as a function of supply voltage**

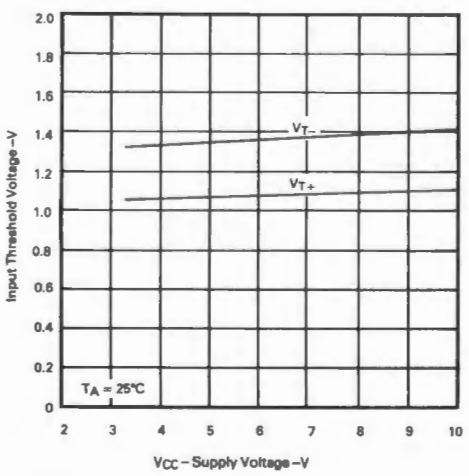


Figure 9 **Input current as a function of input voltage**

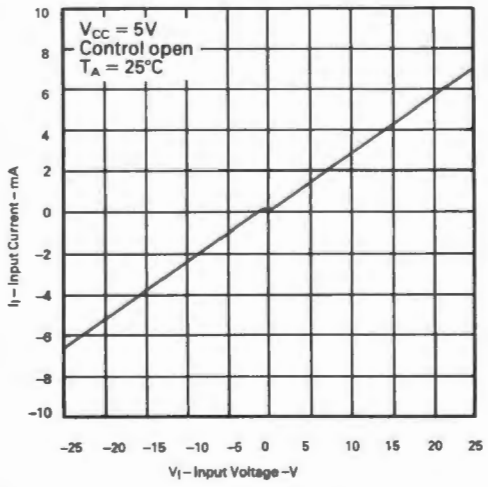
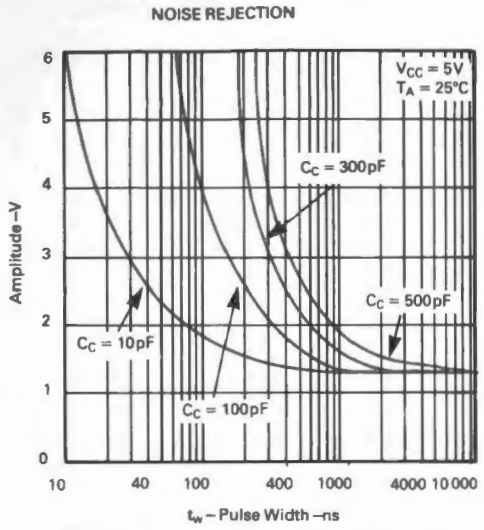
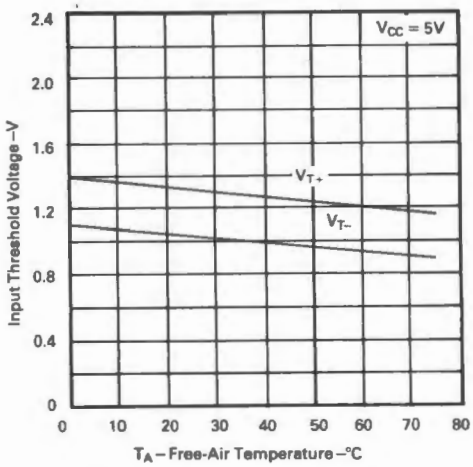


Figure 10 **Noise rejection**



Thermal characteristics

Figure 11 **Input threshold voltage as a function of free-air temperatire**



3691 Line driver

The 3691 is a low power Schottky TTL line driver meeting the requirements of EIA RS422 and RS423. The device features four buffered outputs with high source and sink current capability, plus internal short circuit protection. A mode control input provides a choice of operation either as four independent line drivers or two differential line drivers. A rise time control pin allows the use of an external capacitor to reduce rise time for suppression of near end cross talk to other receivers in the cable.

Features

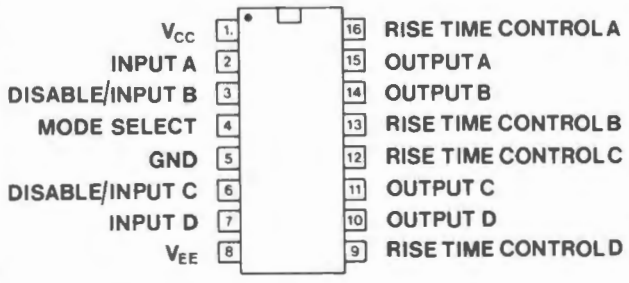
- Dual RS422 line driver with mode pin low, or quad RS423 line driver with mode pin high.
- Short circuit protection for both source and sink inputs.
- Individual rise time control for each output.
- 100Ω transmission line drive capability.
- TTL, MOS and CMOS compatible inputs.

Absolute maximum ratings

Supply voltage:

V_{CC}	7V
V_{EE}	–7V
Maximum power dissipation at 25°C (see note)	1476mW
Input voltage	15V
Output voltage (power OFF)	±15V
Storage temperature	–65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C

Note:
Above 25°C, derate linearly at 11.9mW/°C.



DC electrical characteristics (Notes 1, 2, 3 and 4)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
RS-422 CONNECTION, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	μA
		V_{IN} ≤ 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			–30	–200	μA
V_I	Input Clamp Voltage	I_{IN} = –12mA				–1.5	V
V_O	Differential Output Voltage	R_L = ∞	V_{IN} = 2V		3.6	6.0	V
$\overline{V_O}$	$V_{A,B}$		V_{IN} = 0.8V		–3.6	–6.0	V
V_T	Differential Output Voltage	R_L = 100Ω	V_{IN} = 2V	2	2.4		V
$\overline{V_T}$	$V_{A,B}$	V_{CC} ≥ 4.75V	V_{IN} = 0.8V	–2	–2.4		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	V
$\lvert V_{OS}\rvert - \lvert\overline{V_{OS}}\rvert$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	V

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
RS-422 CONNECTION, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_{SS}	$\|V_T - V_T\|$	$R_L = 100\Omega$, $V_{CC} \geq 4.75V$		4.0	4.8		V
V_{CMR}	Output Voltage Common-Mode Range	$V_{DISABLE} = 2.4V$		±10			V
I_{XA}	Output Leakage Current Power OFF	$V_{CC} = 0V$	$C_{CMR} = 10V$			100	μA
I_{XB}			$V_{CMR} = -10V$			-100	μA
I_{OX}	TRI-STATE Output Current	V_{CC} = Max	$V_{CMR} \leq 10V$			100	μA
			$V_{CMR} \geq -10V$			-100	μA
I_{SA}	Output Short Circuit Current	$V_{IN} = 2.4V$	$V_{OA} = 6V$		80	150	mA
			$V_{OB} = 0V$		-80	-150	mA
I_{SB}	Output Short Circuit Current	$V_{IN} = 0.4V$	$V_{OA} = 0V$		-80	-150	mA
			$V_{OB} = 6V$		80	150	mA
I_{CC}	Supply Current				18	30	mA

AC electrical characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RS422 CONNECTION, V_{CC} = 5V, MODE SELECT = 0.8V						
t_r	Output rise time	$R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_f	Output fall time	$R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_{PDH}	Output propagation delay	$R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_{PDL}	Output propagation delay	$R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_{PZL}	TRI-STATE delay	$R_L = 450\Omega$, $C_L = 500pF$ $C_C = 0pF$		250	350	ns
t_{PZH}	TRI-STATE delay	$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$		180	300	ns
t_{PLZ}	TRISTATE delay	$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$		180	300	ns
t_{PHZ}	TRI-STATE delay	$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$		250	350	ns

DC electrical characteristics (Notes 1, 2, 3 and 4)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
RS423 CONNECTION, V_{CC} = V_{EE}, MODE SELECT ≥2V							
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{IH}	High-level input current	$V_{IN} = 2.4V$ $V_{IN} \leq 15V$			1 10	40 100	μA μA
I_{IL}	Low level input current	$V_{IN} = 0.4V$			-30	-200	μA
V_I	Input clamp voltage	$I_{IN} = -12mA$				-1.5	V
V_O	Output voltage	$R_L = \infty$ $V_{CC} \geq 4.75V$	$V_{IN} = 2V$	4.0	4.4	6.0	V
$\overline{V_O}$			$V_{IN} = 0.4V$	-4.0	-4.4	-6.0	V
V_T	Output voltage	$R_L = 450\Omega$ $V_{CC} \geq 4.75V$	$V_{IN} = 2.4V$	3.6	4.1		V
$\overline{V_T}$			$V_{IN} = 0.4V$	-3.6	-4.1		V
$\|V_T\| - \|\overline{V_T}\|$	Output unbalance	$\|V_{CC}\| = \|V_{EE}\| = 4.75V$, $R_L = 450\Omega$			0.02	0.4	V
I_X^+	Output leakage power OFF	$V_{CC} = V_{EE} = 0V$	$V_O = 6V$		2	100	μA
I_X^-	Output leakage power OFF	$V_{CC} = V_{EE} = 0V$	$V_O = -6V$		-2	-100	μA
I_S^+	Output short circuit current	$V_O = 0V$	$V_{IN} = 2.4V$		-80	-150	mA
I_S^-	Output short circuit current	$V_O = 0V$	$V_{IN} = 0.4V$		80	150	mA
I_{SLEW}	Slew control current				±140		μA
I_{CC}	Positive supply current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative supply current	$V_{IN} = 0.4V$, $R_L = \infty$			-10	-22	mA

Notes:

1. Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the 3691. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.
2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.
3. Only one output at a time should be shorted.
4. Symbols and definitions correspond to EIA RS422 and/or RS423 where applicable.

AC electrical characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RS423 CONNECTION, V_{CC} = 5V, V_{EE} –5V, MODE SELECT = 2.4V						
t_r	Rise time	R_L = 450Ω, C_L = 500pF, C_C = 0		120	300	ns
t_f	Fall time	R_L = 450Ω, C_L = 500pF, C_C = 0		120	300	ns
t_r	Rise time	R_L = 450Ω, C_L = 500pF, C_C = 50pF		3.0		μs
t_f	Fall time	R_L = 450Ω, C_L = 500pF, C_C = 50pF		3.0		μs
t_{rc}	Rise time coefficient	R_L = 450Ω, C_L = 500pF, C_C = 50pF		0.06		μs/pF
t_{PDH}	Output propagation delay	R_L = 450Ω, C_L = 500pF, C_C = 0		180	300	ns
t_{PDL}	Output propagation delay	R_L = 450Ω, C_L = 500pF, C_C = 0		180	300	ns

Typical characteristics

Figure 12 **Switching waveforms**

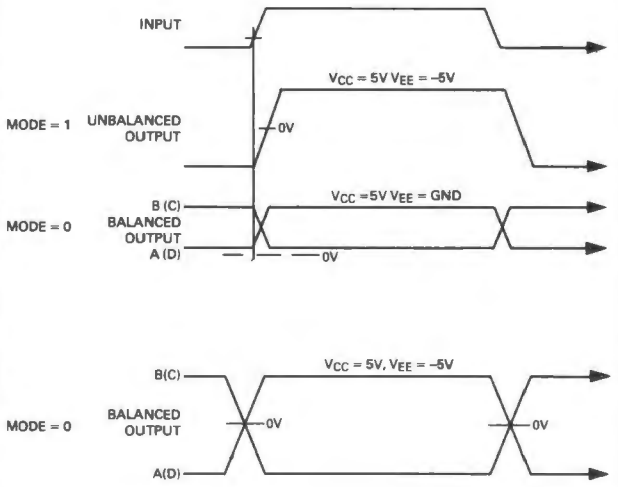
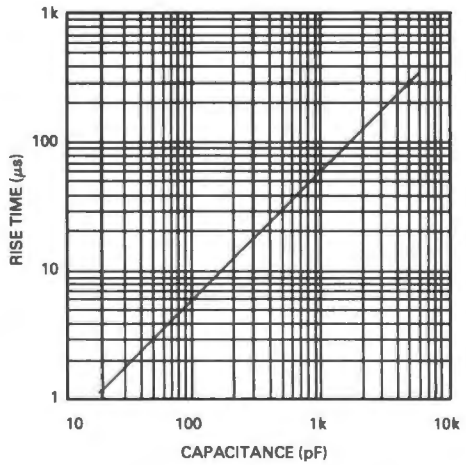


Figure 13 **Rise time as a function of external capacitor**

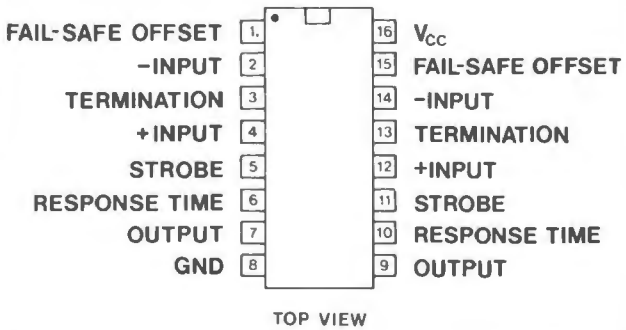


88LS120 Line receiver

The 88LS120 is a dual differential, TTL compatible, line receiver for both balanced and unbalanced data transmission. The device features hysteresis and a response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe protection, should the input be open or short circuited. Each receiver includes an optional 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination.

Features

- Meets specifications of RS232C, RS422 and RS423
- Input voltage range of ±15V.
- Separate strobe input for each receiver.
- Input impedance typically 5kΩ.
- Input hysteresis 50mV.
- Separate fail-safe mode.



Absolute maximum ratings

Supply voltage ——— 7V
Input voltage ——— ±25V
Strobe voltage ——— 7V
Output sink current ——— 50mA
Maximum power dissipation
at 25°C (see note) ——— 1362mW

Note:
Above 25°C, derate linearly at 10.9mW/°C.

Electrical characteristics (Notes 1 and 2)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{TH}	Differential threshold voltage	$I_{OUT} = -400\mu A$, $V_{OUT} \geq 2.5V$	$-7V \leq V_{CM} \leq 7V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
V_{TL}	Differential threshold voltage	$I_{OUT} = 4mA$, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$		-0.08	-0.2	V
			$-15V \leq V_{CM} \leq 15V$		-0.08	-0.3	V
V_{TH}	Differential threshold voltage	$I_{OUT} = -400\mu A$, $V_{OUT} \geq 2.5V$	$-7V \leq V_{CM} \leq 7V$		0.47	0.7	V
V_{TL}	With fall safe offset = 5V	$I_{OUT} = 4mA$, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$	-0.2	-0.42		V
R_{IN}	Input resistance	$-15V \leq V_{CM} \leq 15V$, $0V \leq V_{CC} \leq 7V$		4	5		kΩ
R_T	Line termination resistance	$T_A = 25°C$		100	180	300	Ω
R_O	Offset control resistance	$T_A = 25°C$		42	56	70	kΩ
I_{IND}	Data input current (unterminated)	$V_{CM} = 10V$	$0V \leq V_{CC} \leq 7V$		2	3.1	mA
		$V_{CM} = 0V$			0	-0.5	mA
		$V_{CM} = -10V$			-2	-3.1	mA
V_{THB}	Input balance	$I_{OUT} = -400\mu A$, $V_{OUT} \geq 2.5V$, $R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		-0.1	-0.4	V
		$I_{OUT} = 4mA$, $V_{OUT} \leq 0.5V$, $R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		-0.1	-0.4	V
V_{OH}	Logical '1' output voltage	$I_{OUT} = -400\mu A$, $V_{DIFF} = 1V$, $V_{CC} = 4.5V$		2.5	3		V
V_{OL}	Logical '0' output voltage	$I_{OUT} = 4mA$, $V_{DIFF} = -1V$, $V_{CC} = 4.5V$			0.35	0.5	V
I_{CC}	Power supply current	$V_{CC} = 5.5V$,	$V_{CM} = 15V$		9	12	mA
		$V_{DIFF} = -0.5V$, (both receivers)	$V_{CM} = -15V$		10	16	mA
$I_{IN(1)}$	Logical '1' strobe input current	$V_{STROBE} = 5.5V$, $V_{DIFF} = 3V$			1	100	μA
$I_{IN(0)}$	Logical '0' strobe input current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$			-290	-400	μA
V_{IH}	Logical '1' strobe input voltage	$V_{OL} \leq 0.5$, $I_{OUT} = 4mA$		2.0	1.12		V
V_{IL}	Logical '0' srobe input voltage	$V_{OH} \geq 2.5V$, $I_{OUT} = -400\mu A$			1.12	0.8	V
I_{OS}	Output short-circuit current	$V_{OUT} = 0V$, $V_{CC} = 5.5V$, $V_{STROBE} = 0V$, (note 3)		-30	-100	-170	mA

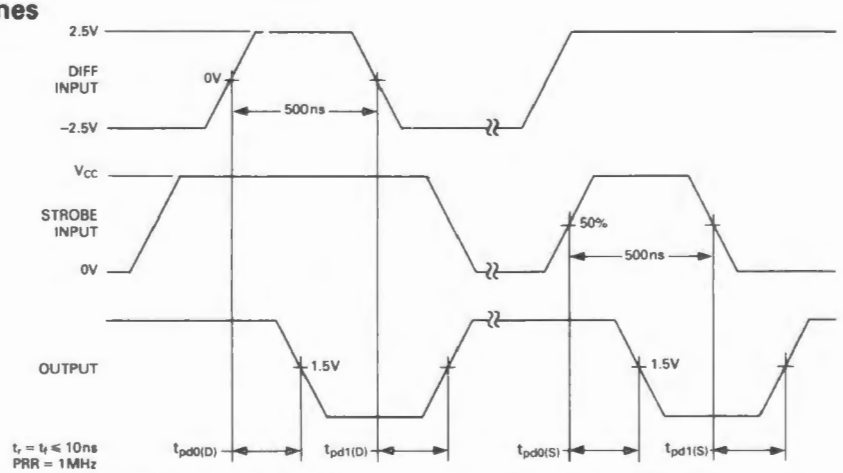
Switching characteristics $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{pd0(D)}$	Differential input '0' output	Response pin open, $C_L = 15pF$, $R_L = 2k\Omega$		38	60	ns
$t_{pd1(D)}$	Differential input to '1' output			38	60	ns
$t_{pd0(S)}$	Strobe input to '0' output			16	25	ns
$t_{pd1(S)}$	Strobe input to '1' output			12	25	ns

Note:

1. Unless otherwise specified min/max limits apply across the 0°C to +70°C for the 88LS120. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.
2. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
3. Only one output at a time should be shorted.

Figure 14 **Switching times**



Note: Optimum switching response is obtained by minimising stray capacitance on Response Control pin (no external connection).

Applications

Figure 15 **Balanced data transmission**

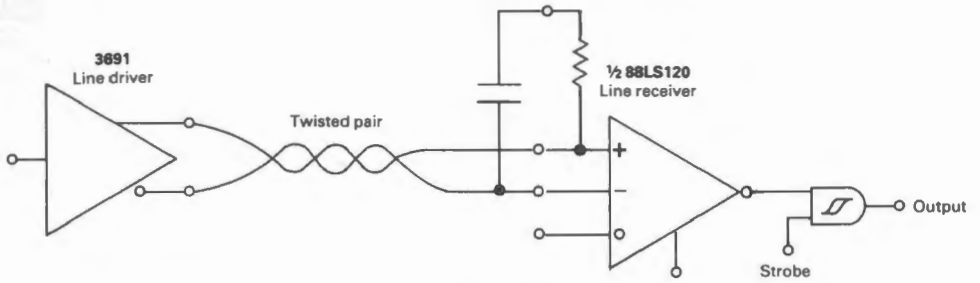
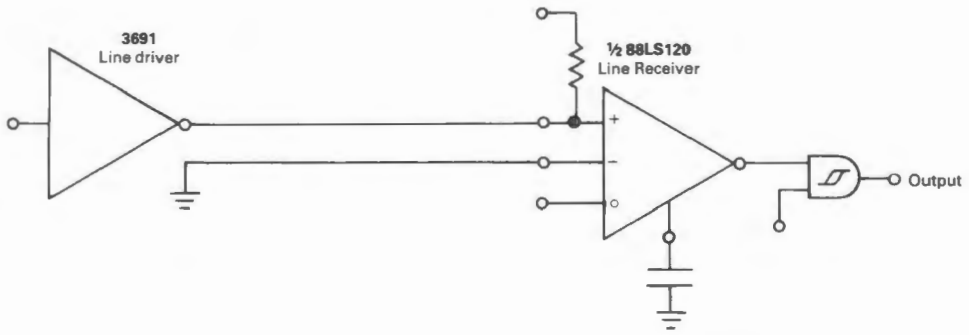
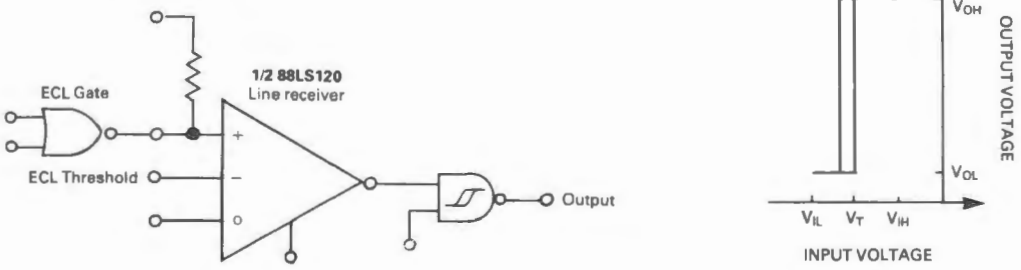


Figure 16 **Unbalanced data transmission**



The 88LS120 may be used as a level translator between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to ½ the voltage of the input signal, and the other input to the driving gate.

Figure 17 **Logic level translator**



Transmission line techniques

Response control and hysteresis

In unbalanced (RS232/RS423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the 88LS120 by the 50mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50mV can be reduced in amplitude by filtering the device input. On the 88LS120 a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection versus the value of the response control capacitor is shown in Figures 18 and 19. This combination of filters followed by hysteresis will optimise performance in a worse case noise environment.

Figure 18 **Noise pulse width as a function of response control capacitor**

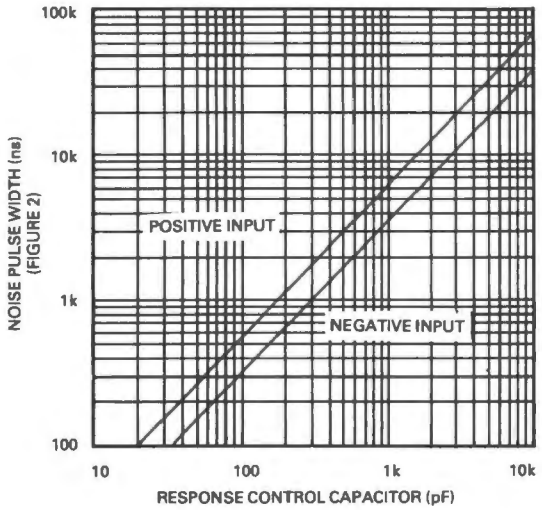
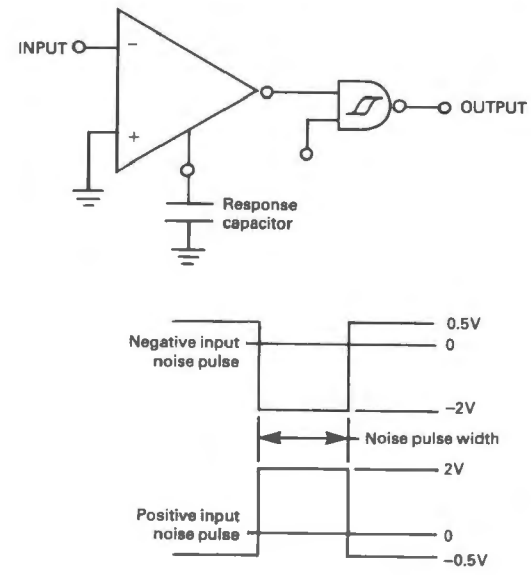


Figure 19 **Response control**



Transmission line termination

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/cross-talk. A 180Ω termination resistor is provided in the 88LS 120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimise power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value.

Example: if the transmission line is 1000 feet long, (approximately 1000ns), and the termination resistor value is 180Ω, the capacitor value should be 1852pF.

Fail-safe operation

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or shorts. To facilitate the detection of input opens or short, the 88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input theshold is ±200mV, an input signal greater than ±200mV ensures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200mV to 700mV, referred to the non-inverting input, or −200mV to −700mV, referred to the inverting input. Therefore, if the input is open or short, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ + 0.45V or $V_{IN(INVERTING)}$ + 0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to ensure it will detect an open circuit in the presence of noise.

The offset control can be used to ensure fail-safe operation for unbalanced interface (RS423) or for balanced interface (RS422) operation.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to 5V offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of the NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

In a communications system, only the control signals are required to detect input fault conditions. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3. Long line lengths.

Figure 20 **Unbalanced RS423 and RS232 Fail-safe**

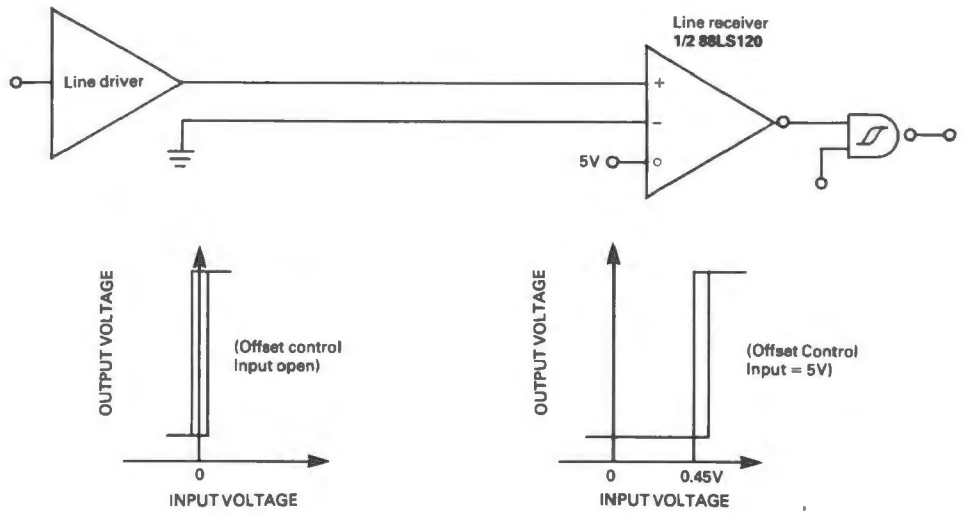
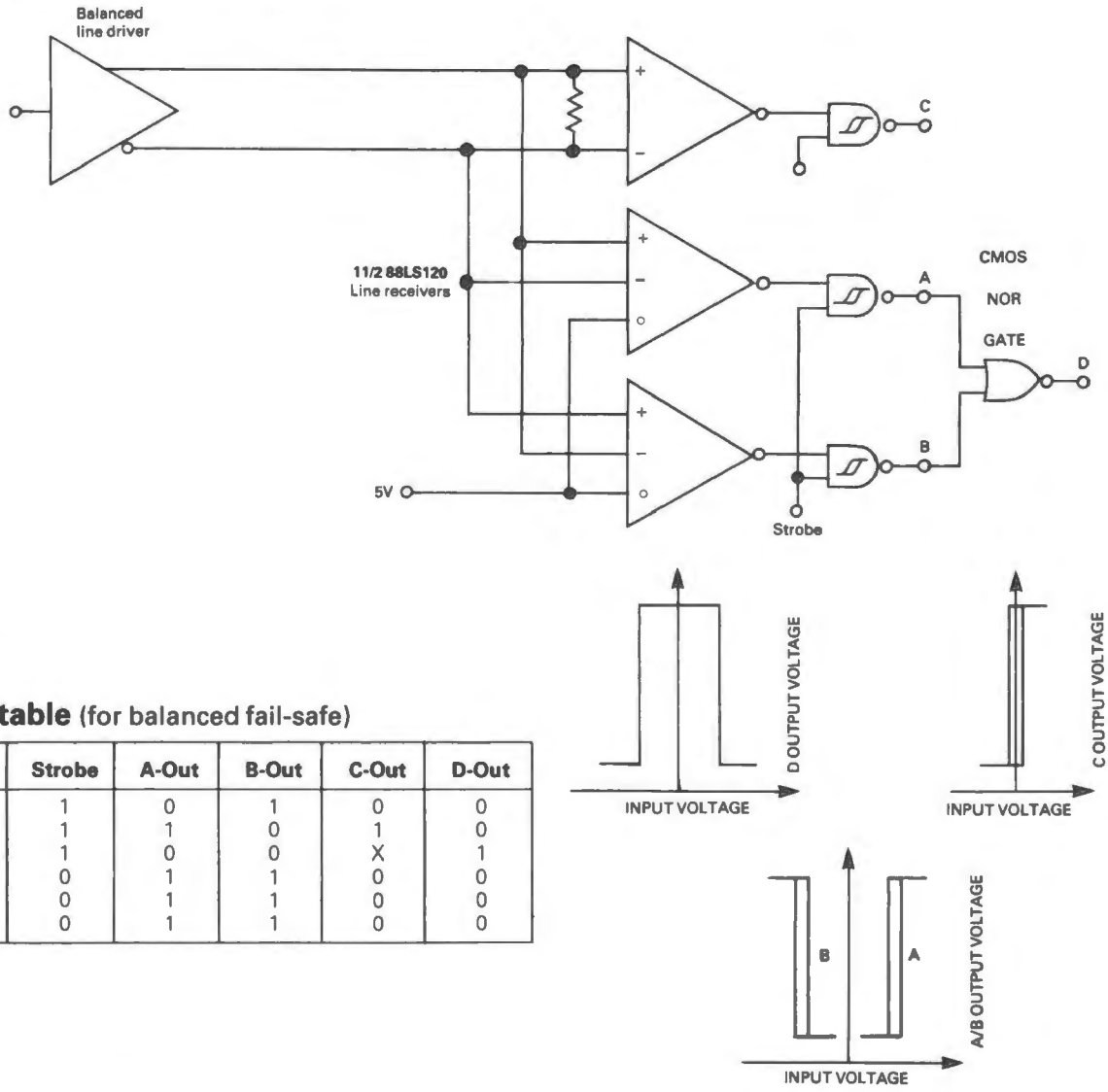


Figure 21 **Balanced RS422 Fail-safe**

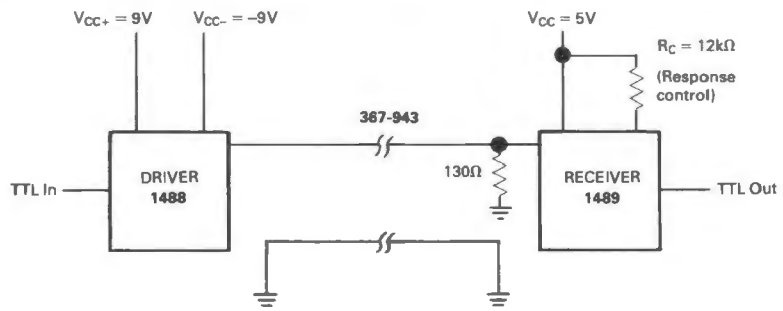


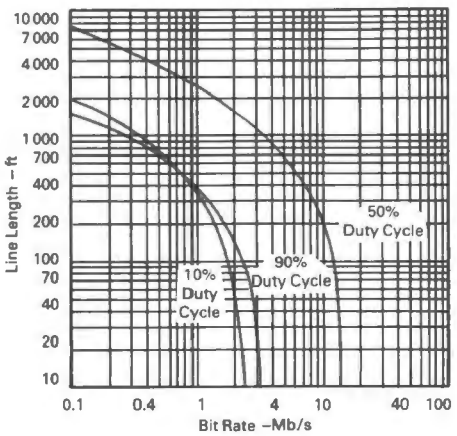
Truth table (for balanced fail-safe)

Input	Strobe	A-Out	B-Out	C-Out	D-Out
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

RS data

Figure 22 **Line length capability as a function of bit rate**





Summary of interface parameters

	RS232C	RS422A	RS423A
Maximum cable length	50ft	4000ft	4000ft
Maximum data rate	20Kb/s	100Kb/s	10Mb/s
Number of drivers on one line	1	1	1
Number of receivers on one line	1	10	10

For further details of the RS232 system a book entitled 'RS232 Made Easy' (902-732) is available, see current RS Catalogue for further details.

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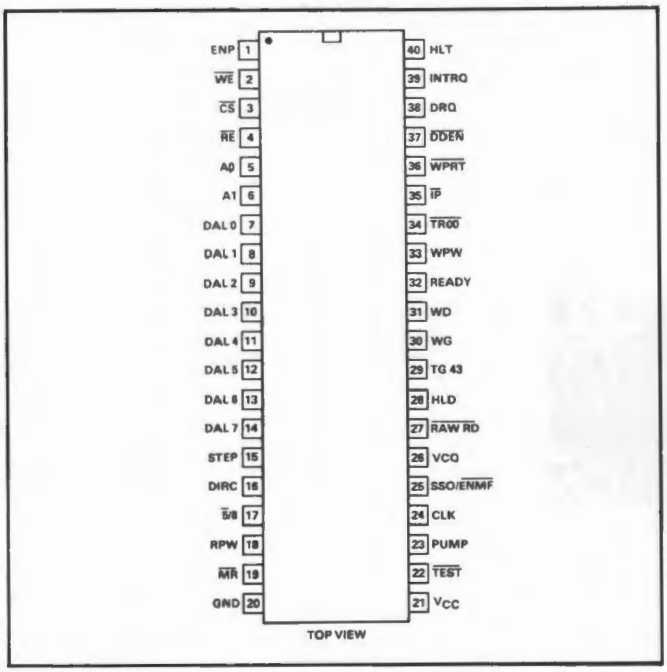
RS data

Floppy Disc Driver Controller i.c. 2797

Stock number 301-117

The 2797 is a single chip floppy disc drive formatter and controller using the latest n-channel MOS LSI technology. It incorporates control circuitry compatible with the older 179X types, with the addition of an internal data separator and write precompensation circuitry. Frequency-Modulated (FM) and Modified-Frequency-Modulated (MFM) operation is possible for single and double density modes on both 8in, 5¼in and RS 3½in drives. A side select output is also available allowing operation of double sided drives.



Absolute maximum ratings

Voltage on any input with respect to V_{SS} +15V to –0.3V

C_{IN} and C_{OUT} all other pins grounded ——— 15pF

Operating temperature range ——— 0°C to +70°C

Storage temperature range ——— –55°C to +125°C

Features

- Single +5V supply
- On-chip PLL data separator
- On-chip write precompensation logic
- Single density IBM 3740 FM Format and
- Double density IBM 34 MFM Format
- Compatible with S400 (Shuggart) drive interfaces
- Automatic seek with Verify
- Multiple sector Read/Write
- Programmable control of Track-to-Track access and Head load timing
- Software compatible with 179X series
- Side select output.

ATTENTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

Electrical characteristics

T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ±5%

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input leakage	I_{IL}	$V_{IN} = V_{CC}$			10	μA
Output leakage	I_{OL}	$V_{OUT} = V_{CC}$			10	μA
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	$I_O = -100\mu A$	2.4			V
Output Low Voltage	V_{OL}	$I_O = 1.6mA$			0.45	V
Output High Pump	V_{OHP}	$I_{op} = -1.0mA$	2.2			V
Output Low Pump	V_{OLP}	$I_{op} = +1.0mA$			0.2	V
Power Dissipation	P_D	All outputs open			0.75	W
Internal Pull-up	R_{PU}	V_{IN} = 0V Note 1	100		1700	μA
Supply Current	I_{CC}	All outputs open		70	150	mA

Note 1: These internal pull-up resistors are on Pins 1, 17, 22, 25, 37 and 40.

Table 1 **Pin designations**

Pin Number	Pin Name	Symbol	Function
1	ENABLE PRECOMP	ENP	A logic high on this input enables write precompensation to be performed on the Write Data output.
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ± 5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5, 6	REGISTER SELECT LINES	A0, A1	These inputs select the register of receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit bi-directional bus used for transfer of commands, status, and data.
24	CLOCK	CLK	This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ± 1% for 8in drives, 1 MHz ± 1% for 5¼in floppy disc drives.
38	DATA REQUEST	DRQ	This output indicates that the Data Register contains assembled data in Read operations, or the DR is empty in Write operations. The signal is reset when serviced by the computer through reading or loading the DR.
39	INTERRUPT REQUEST	INTRQ	This output is set at the completion of any command and reset when the Status register is read or the Command register is written to.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	5¼in, 8in SELECT	$\overline{5/8}$	This input selects the internal VCO frequency for use with 5¼in drives or 8in drives.
18	READ PULSE WIDTH	RPW	An external potentiometer tied to this input controls the phase comparator within the data separator.
22	TEST	$\overline{TEST}$	A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins.
23	PUMP	PUMP	High-impedance output signal which is forced high or low to increase/decrease the VCO frequency.
25	SIDE SELECT OUTPUT	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = 0, SSO is set to a logic 0. The SSO is compared with the side information in the Sector I.D. Field. If they do not compare Status Bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	VOLTAGE-CONTROLLED OSCILLATOR	VCO	An external capacitor tied to this pin adjusts the VCO centre frequency.
27	RAW READ	$\overline{RAW\ READ}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the disc.
31	WRITE DATA	WD	A 250ns (MFM) of 500ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disc readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format at Status Register bit 7.
33	WRITE PRECOMP WIDTH	WPW	An external potentiometer tied to this input controls the amount of delay in Write precompensation mode.
34	TRACK 00	$\overline{TR00}$	This input informs the WD2797 that the Read/Write head is positioned over Track 00.
35	INDEX PULSE	$\overline{IP}$	This input informs the WD2797 when the index hole is encountered on the disc.

Pin Number	Pin Name	Symbol	Function
36	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	$\overline{DDEN}$	This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected.
40	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a 1 shot triggered by HLD.

General description

The WD2797 is an N-Channel Silicon Gate MOS LSI device which performs the functions of a Floppy Disc Formatter/Controller in a single chip implementation. The WD2797, which can be considered the end result of both the FD1771 and FD1797 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The WD2797 contains all the features of its predecessor the FD1797 plus a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic. In Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the FD1771, FD1797 and WD2797 designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The WD2797 is set up to operate on a multiplexed bus with other bus-oriented devices.

The WD2797 is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads.

The 2797 has a side select output for controlling double sided drives.

Organisation

The Floppy Disc Formatter block diagram is illustrated in Figure 1. The primary sections include the parallel processor interface and the Floppy Disc interface.

Data Shift Register – This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register – This 8-bit register is used as a holding register during Disc Read and Write operations in Disc Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disc Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disc Read, Write and Verify operations. The Track Register can be loaded from or translated to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR) – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during the disc Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) – This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a forced interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) – This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic – This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) – The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disc recorded ID field.

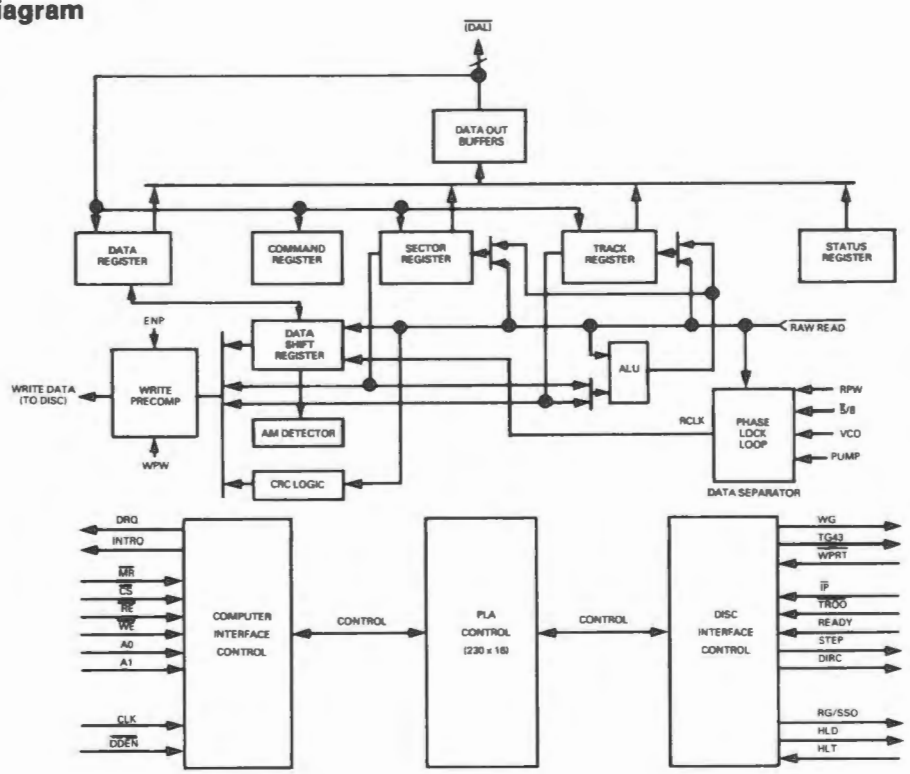
Timing and Control – All computer and Floppy Disc interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector – The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation – enables write precompensation to be performed on the Write Data output.

Data Separator – a high performance Phase-Lock-Loop Data Separator with on-chip VCO and phase comparator allows adjustable frequency range for 5¼in or 8in Floppy Disc interfacing.

Figure 1 **Block diagram**



Processor interface

The processor interface is achieved through the eight Data Access Lines (DAL) and associated control signal lines. The DAL lines are used for transfer of Data, Status and control words into and out of the 2797 controller. These lines are three-state buffers that are enabled as output drivers with $\overline{CS}$ and $\overline{RE}$ active low or act as receivers with $\overline{CS}$ and $\overline{WE}$ active low.

When transfer of data with the Floppy Disc Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1	A0	Read ($\overline{RE}$)	WRITE ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the WD2797 and the processor, the Data Request (DRQ) output is used in Data Transfer control. The signal also appears as status bit 1 during Read and Write operations.

On Disc Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disc Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disc, a byte of zeroes is written on the disc and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

The 2797 has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8in or 1 MHz for 5¼in drives.

The internal VCO frequency must also be set to the proper value. The $\overline{5}/8$ input (Pin 17) is used to select data separator operation by internally dividing the Read Clock. When $\overline{5}/8$ = 0, 5¼in data separation is selected; when $\overline{5}/8$ = 1, 8in drive data separation is selected.

Clock (24)	$\overline{5}/8$(17)	Drive
2MHz	1	8in
1MHz	0	5¼in

Functional description

The WD2797-02 is software compatible with the FD1797-02 series of Floppy Disc Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the 1797 can be transferred to a 2797 system without modification.

In addition to the 1797, the 2797 contains an internal Data Separator and Write precompensation circuit. The $\overline{\text{TEST}}$ (Pin 22) line is used to adjust both data separator and precompensation. When $\overline{\text{TEST}}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second one-shot tracks the precomp setting at approximately 3:1 to ensure adequate Write Data pulse widths to meet drive specifications.

Similarly, Data separation is also adjusted with $\overline{\text{TEST}}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the Read Clock output (.5MHz for 8in drives). The VCO Trimming capacitor (Pin 26) is adjusted for centre frequency.

Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in-circuit. The $\overline{\text{TEST}}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{\text{TEST}}$ pin, overriding the pull-up. The $\overline{\text{TEST}}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the 1797.

Other pins on the device also include pull-up resistors and may be left open to satisfy a Logic 1 condition. These are: ENP, 5/8, $\overline{\text{ENMF}}$, $\overline{\text{WPRT}}$, and $\overline{\text{DDEN}}$.

General disc read operations

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical '1'. For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical '0.' Sector lengths are determined at format time by the fourth byte in the 'ID' field.

The number of sectors per track as far as the 2797 is concerned can be from 1 to 255 sectors. The number of tracks as far as the 2797 is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

General disc write operation

When writing is to take place on the disc the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the 2797 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

For write operations, the 2797 provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

Ready

Whenever a Read or Write command (Type II or III) is received the 2797 samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated. TG43 may be tied to ENP to enable write precompensation on tracks 44-76.

Command description

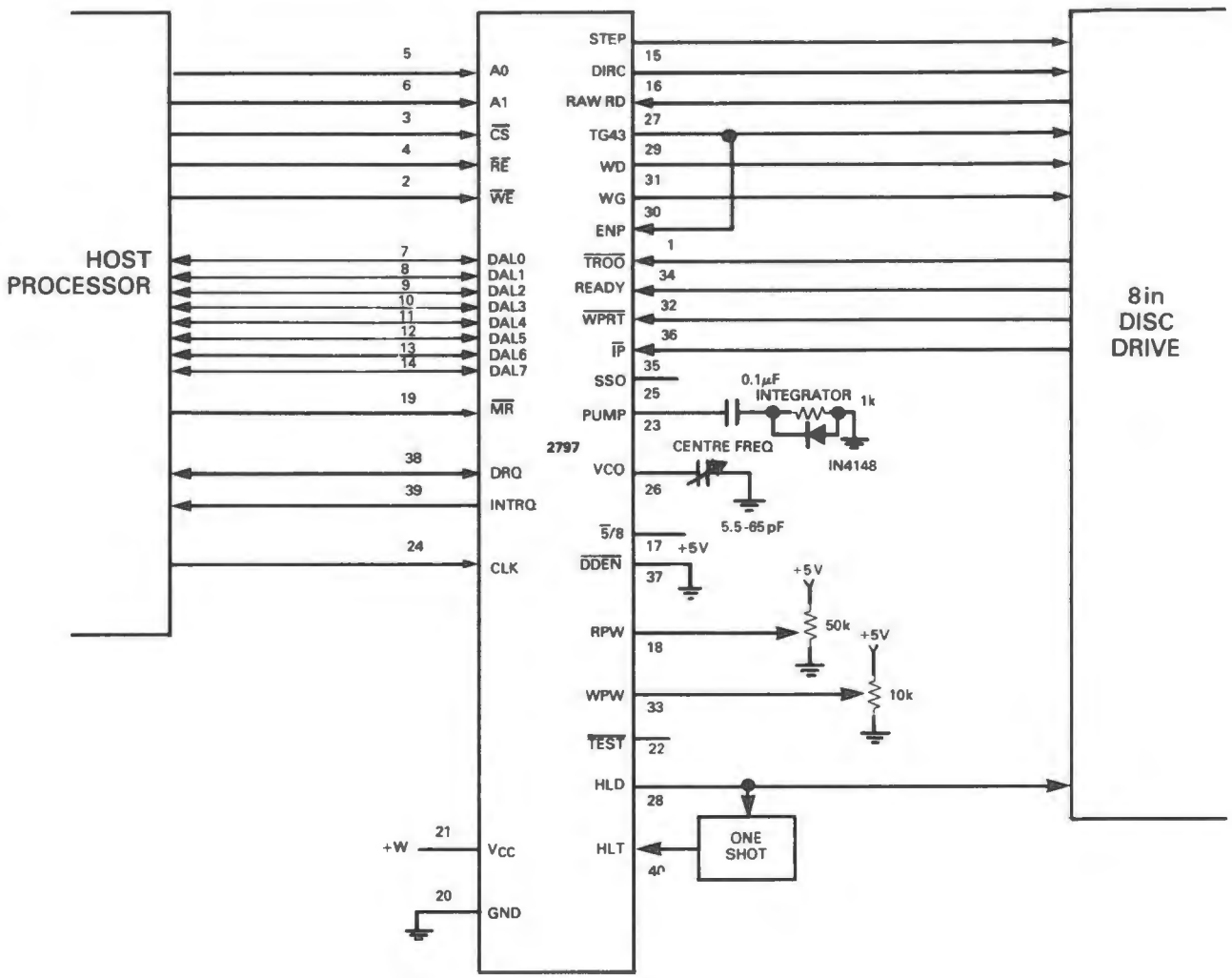
The WD2797 will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarised in Table 2.

Commands

Table 2

		Bits							
Type	**Command**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0
II	Read sector	1	0	0	m	L	E	U	0
II	Write sector	1	0	1	m	L	E	U	a_0
III	Read address	1	1	0	0	0	E	U	0
III	Read track	1	1	1	0	0	E	U	0
III	Write track	1	1	1	1	0	E	U	0
IV	Force interrupt	1	1	0	1	I_3	I_2	I_1	I_0

Figure 2 **Application Circuit**



Flag summary

Table 3

Command Type	Bit No(s)		Description
I	0, 1	r_1 r_0 = Stepping Motor Rate See Table 4 for Rate Summary	
I	2	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning
I	4	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	0	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	2	E = 15ms Delay	E = 0, No. 15 ms delay E = 1, 15 ms delay (30 ms for 1 MHz)
II	3	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	3	L = Sector Length Flag	LSBs Sector Length in ID Field 00: L=0: 256; L=1: 128 01: L=0: 512; L=1: 256 10: L=0: 1024; L=1: 512 11: L=0: 128; L=1: 1024
II	4	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	0-3	I_x = Interrupt Condition Flags I_0 = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset* I_3-I_0 = 0 Terminate With No Interrupt (INTRQ)	

NOTE: See Type IV Command Description for further information.

Write precompensation

When operating in Double Density mode ($\overline{DDEN}$ = 0), the 2797 has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.

Setting the Write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a Logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{TEST}$ = 0.

Data separation

The 2797 can operate with either an external data separator or its own internal recovery circuits. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.

To programme the 2797 for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST}$ = 0. A clock equivalent to eight times the data rate (e.g., 4.0 MHz for 8 in Double Density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a Logic 1 for normal operation. Note: To maintain this mode, $\overline{TEST}$ must be held low whenever $\overline{MR}$ is applied.

For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a Logic 0 for the adjustment procedure.

A 50K Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8 in Double Density). An external variable capacitor of 5.5-65 pf is tied to the VCO input (Pin 26) for adjusting centre frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate Data Rate (500 KHz for 8 in Double Density). The $\overline{DDEN}$ line must be low while the 5/8 line is held high or the adjustment times above will be doubled.

After adjustments have been made, the $\overline{TEST}$ pin is returned to a Logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.

The PUMP output (Pin 23) consists of positive and negative pulses, their duration is equivalent to the phase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a Filter is needed to connect these pulses to slow moving dc voltage.

The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favour of a PUMP UP condition. Therefore, it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.

A first order lag-lead filter can be used at the PUMP output (Pin 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift, i.e., the lock-up time. A balance must be accomplished between the two conditions to inhibit over-responsiveness to jitter and to prevent an extremely wide lock-up response, leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The Source Impedance for a PUMP UP/DOWN condition is 600/120 ohms, respectively, therefore the change in bias voltage for each pump can be approximated:

$$dV = \frac{dt\ \triangle V}{RC}$$

$dt = 250ns.$ (set by RPW)
$C = 0.1\mu F$
$R = R_S + R$
$\triangle V = 2.6V$ for PUMP UP
$0.9V$ for PUMP DOWN

Look up response (T_L) is the transient time for the Loop to lock from centre frequency (F_O) to maximum lock range.

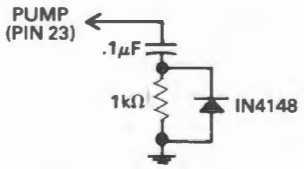
$$T_L = 10\%\ F_L \times K_O \times \triangle P$$

Where:

K_O = VCO Conversion Gain = 3.7KHz/mV
F_L = Lock Range = 4.00MHz
$\triangle P$ = Change in Bias for each Pump = 4mV/PUMP

400KHz x 3.7KHz x 4mV = 27 pumps
27 pumps = 54μsec = 3.4 Byte times
(8in Double Density)

The following Filter Circuit is recommended for 8in FM/MFM:



Since 5¼in Drives operate at exactly one-half the data rate (250Kb/sec) the above capacitor should be doubled to .2 or .22μF.

Type I Commands

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field ($r_0\ r_1$), which determines the stepping motor rate as defined in Table 4.

A 2μs (MFM) or 4μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output. The chip will step the drive in the same direction it last stepped unless the command changes the direction.

The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12μs before the first stepping pulse is generated.

The rates (shown in Table 4) can be applied to a Step-Direction Motor through the device interface.

Stepping rates

Table 4

CLK		2MHz	1MHz
R1	R0	$\overline{TEST} = 1$	$\overline{TEST} = 1$
0	0	3ms	6ms
0	1	6ms	12ms
1	0	10ms	20ms
1	1	15ms	30ms

After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type 1 commands. Note that this time doubles to 30ms for 1MHz clock. There is also a 15ms head settling time if the E flag is set in any Type II or III command.

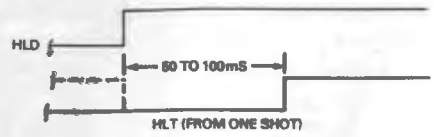
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disc for the verification operation.

The WD2797 must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated. If V = 0, no verification is performed.

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type 1 command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the 2797 is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load timing (HLT) is an input to the 2797 which is used for the head engage time. When HLT = 1, the 2797 assumes the head is completely engaged. The head engage time is typically 30 to 100ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the 2797.

Figure 3 **Head load timing**



When both HLD and HLT are true, the 2797 will then read from or write to the media. The 'and' of HLD and HLT appears as status Bit 5 in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15ms occurs, and the 2797 waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15ms delay occurs and the 2797 then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15ms delay occurs and then HLT is sampled until true.

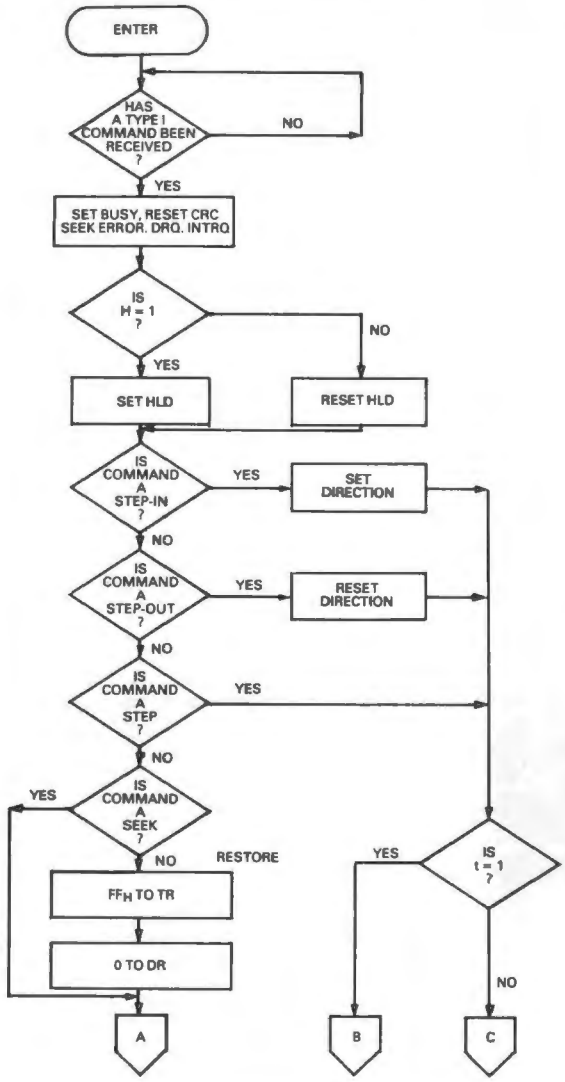
Restore (Seek Track 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the 2797 terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

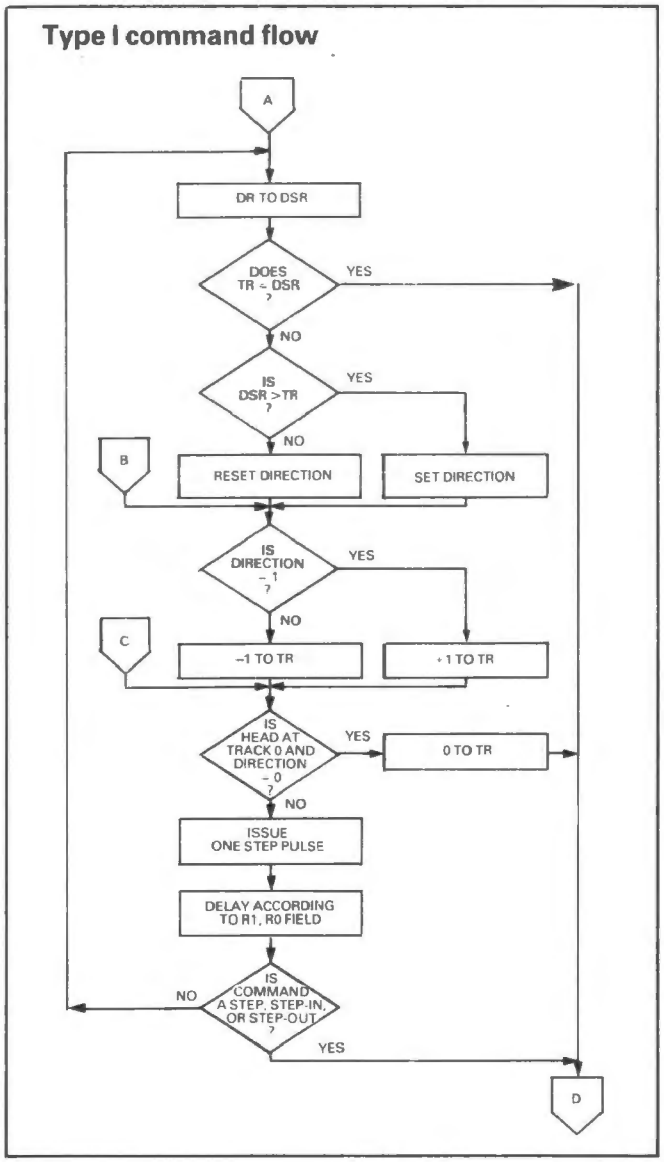
Seek

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The WD2797 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

Type I command flow



in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.



Step

Upon receipt of this command, the 2797 issues one stepping pulse to the disc drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

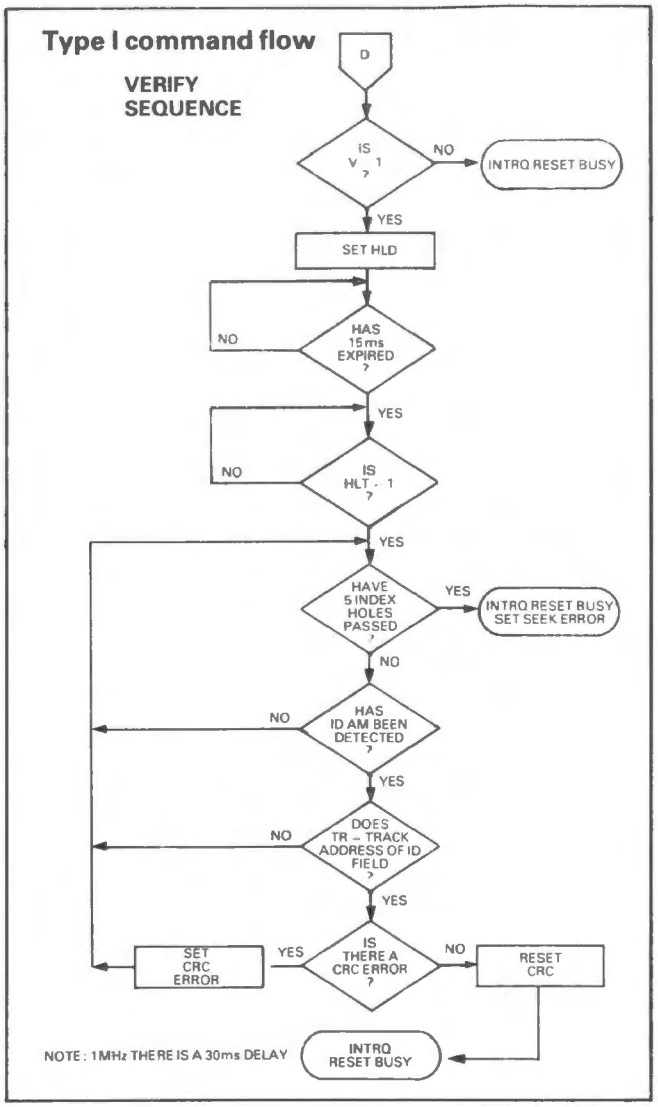
Step-in

Upon receipt of this command, the 2797 issues one stepping pulse in the direction towards track 76. If the T flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-out

Upon receipt of this command, the 2797 issues one stepping pulse in the direction towards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

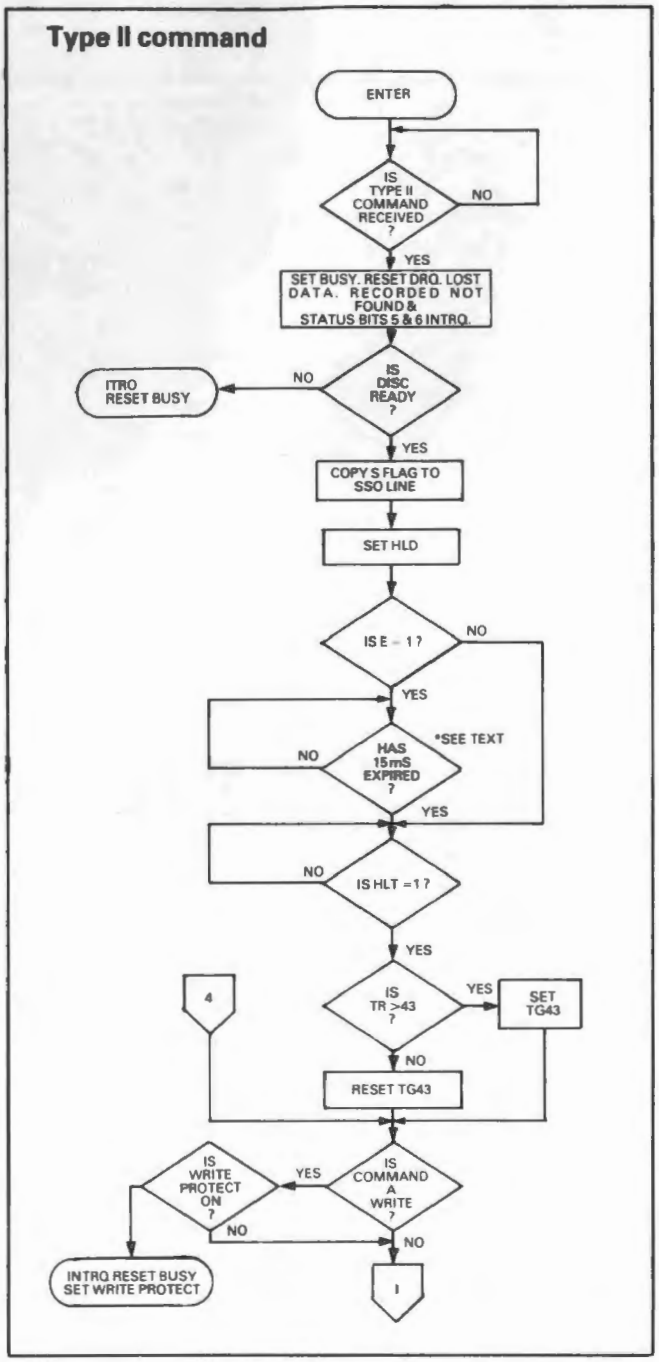
On the 2797 the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify Flag is on.

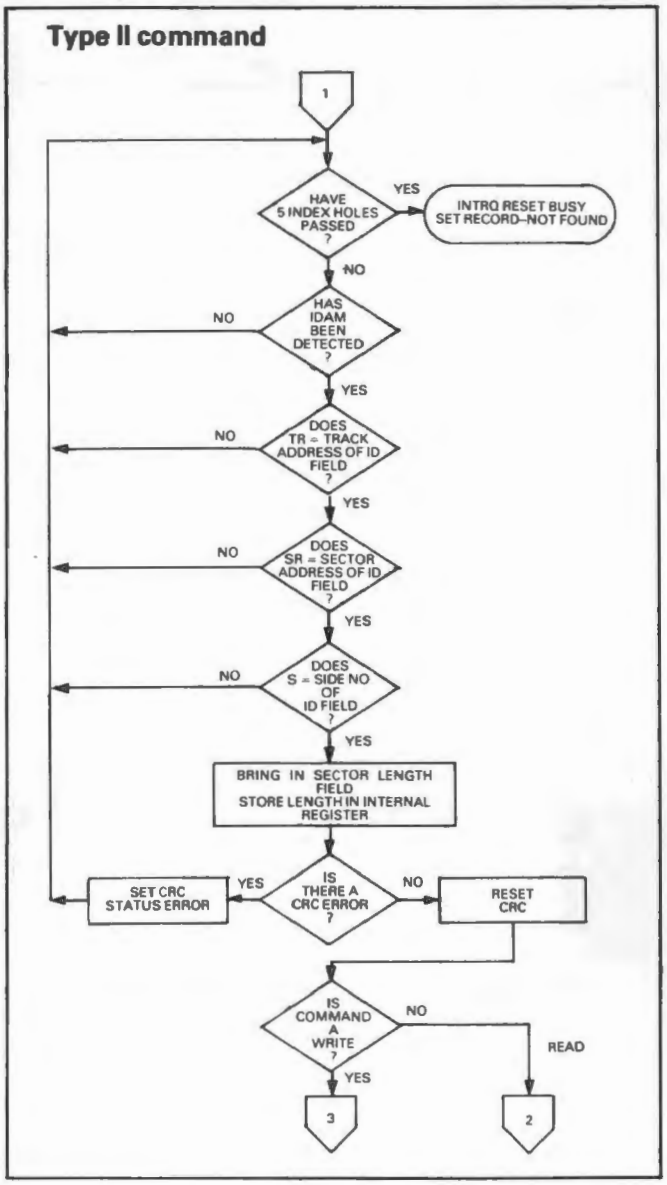


Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15msec delay.

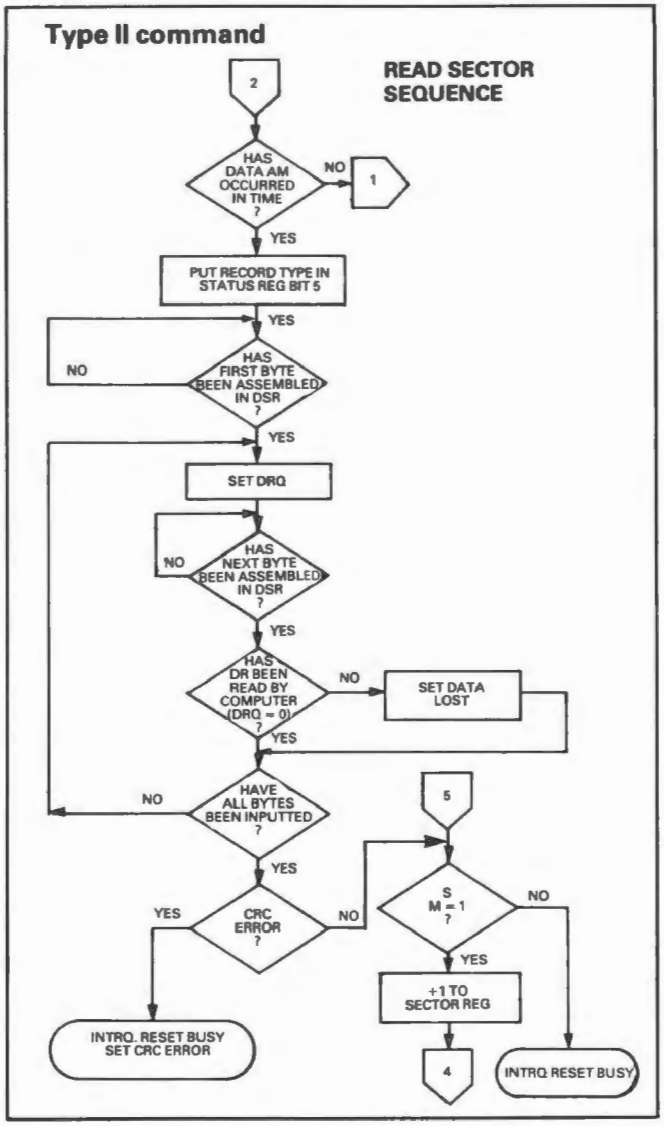
When an ID field is located on the disc the 2797 compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disc and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The 2797 must find an ID field with a Track number, Sector number, side number, and CRC within 5 revolutions of the disc; otherwise, the Record not found status bit is set (Status bit 4) and the command is terminated with an interrupt.

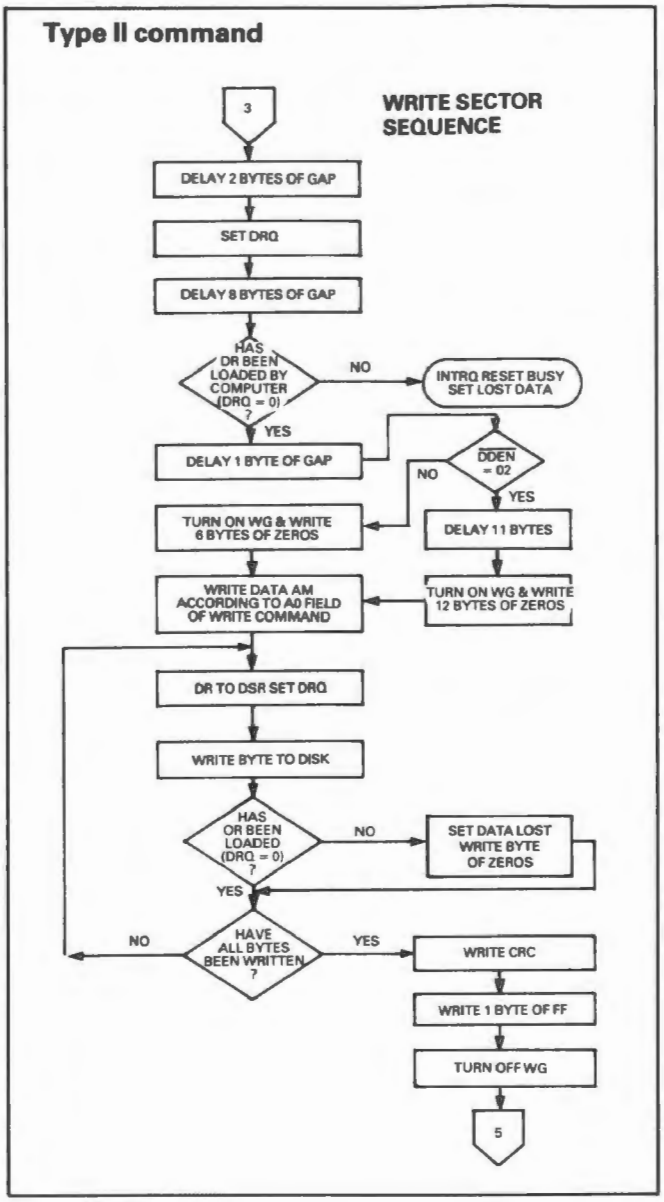




Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 2797 will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the 2797 is instructed to read sector 27 and there are only 26 on the track, the sector register exceeds the number available. The 2797 will search for 5 disc revolutions, interrupt out, reset busy, and set the record not found status bit.





The Type II and III commands for the 2797 contain a side select flag (Bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The 2797 READ SECTOR and WRITE SECTOR commands include an 'L' flag. The 'L' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'L' flag should be set to a one.

Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field search is repeated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

Write sector

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The 2797 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single

density and 12 bytes in double density are then written on the disc. At this time the Data Address Mark is then written on the disc as determined by the *0 field of the command as shown below:

*0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The 2797 then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeroes is written on the disc. The command is not terminated. After the last data byte has been written on the disc, the two-byte CRC is computed internally and written on the disc followed by one byte of FE in FM or in MFM. The WG output is then deactivated. For a 2MHz clock the INTRQ will set 8 to 12 μsec after the last CRC byte is written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the lost data status and improper CRC Bytes.

Type III commands

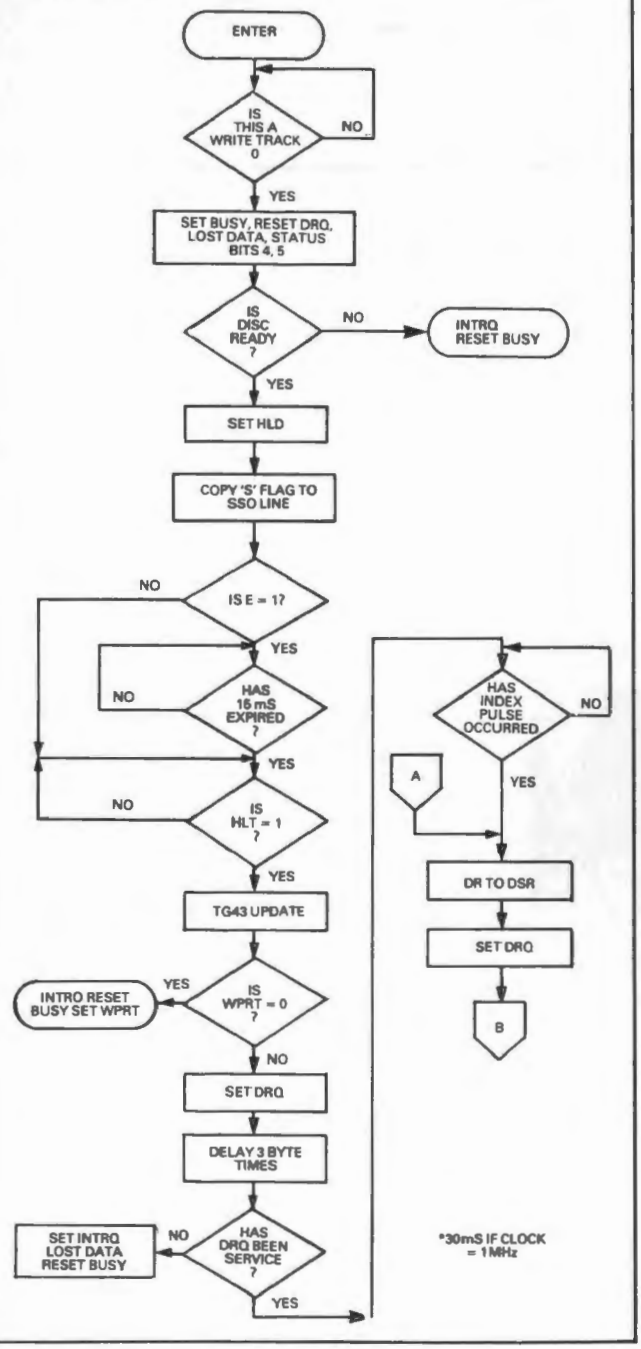
Read address

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disc, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the 2797 checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy Status is reset.

Type III command write track

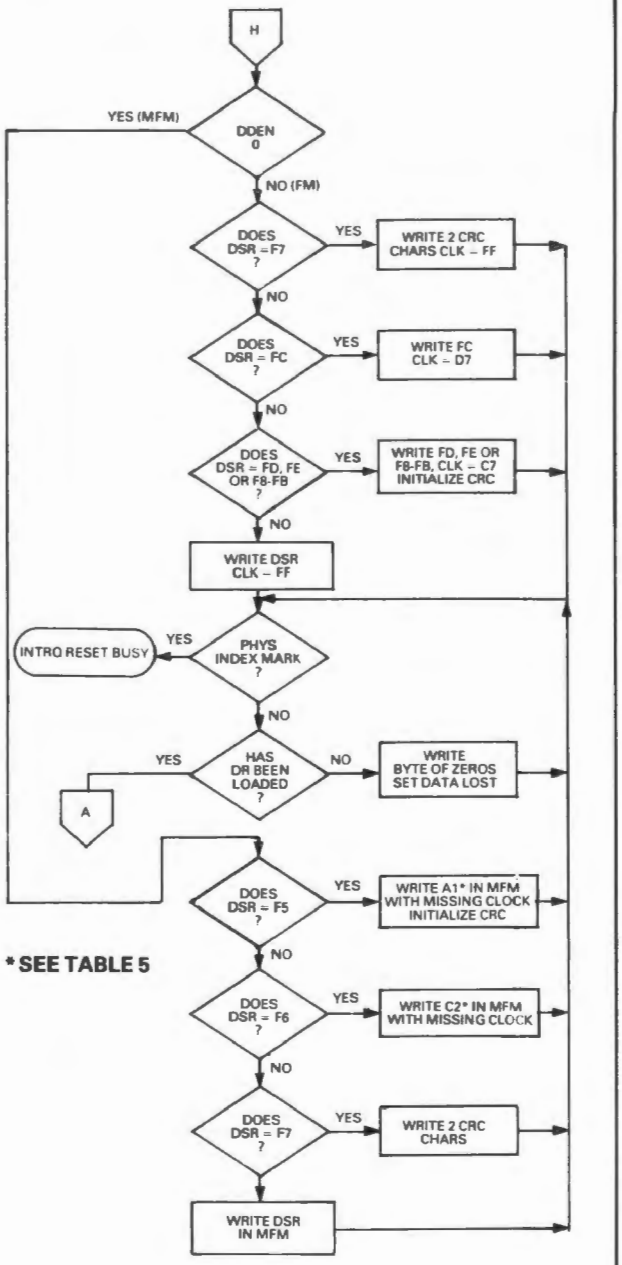


Read track

Upon receipt of the READ track command, the head is loaded, and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All Gap, Header, and data bytes are assembled and transferred to the data register and DRQs are generated for each byte. The accumulation of bytes is synchronised to each address mark encountered. An interrupt is generated at the completion of the command.

This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the AM detector is always on, write splices or noise may cause the chip to look for an AM. If an address mark does not appear on schedule with the Lost Data status flag being set.

Type III Command Write Track



The ID AM, ID field, ID CRC bytes, DAM, Data and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronisation.

Write track formatting the disc

(Refer to section on Type III commands for flow diagrams.)

Formatting the disc is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disc is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disc with a normal clock pattern. However, if the 2797 detects a data pattern of F5 through FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialised when any data byte from F8 to FE is about to be transferred from the DR to the DSR or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern.

Discs may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

Type IV commands

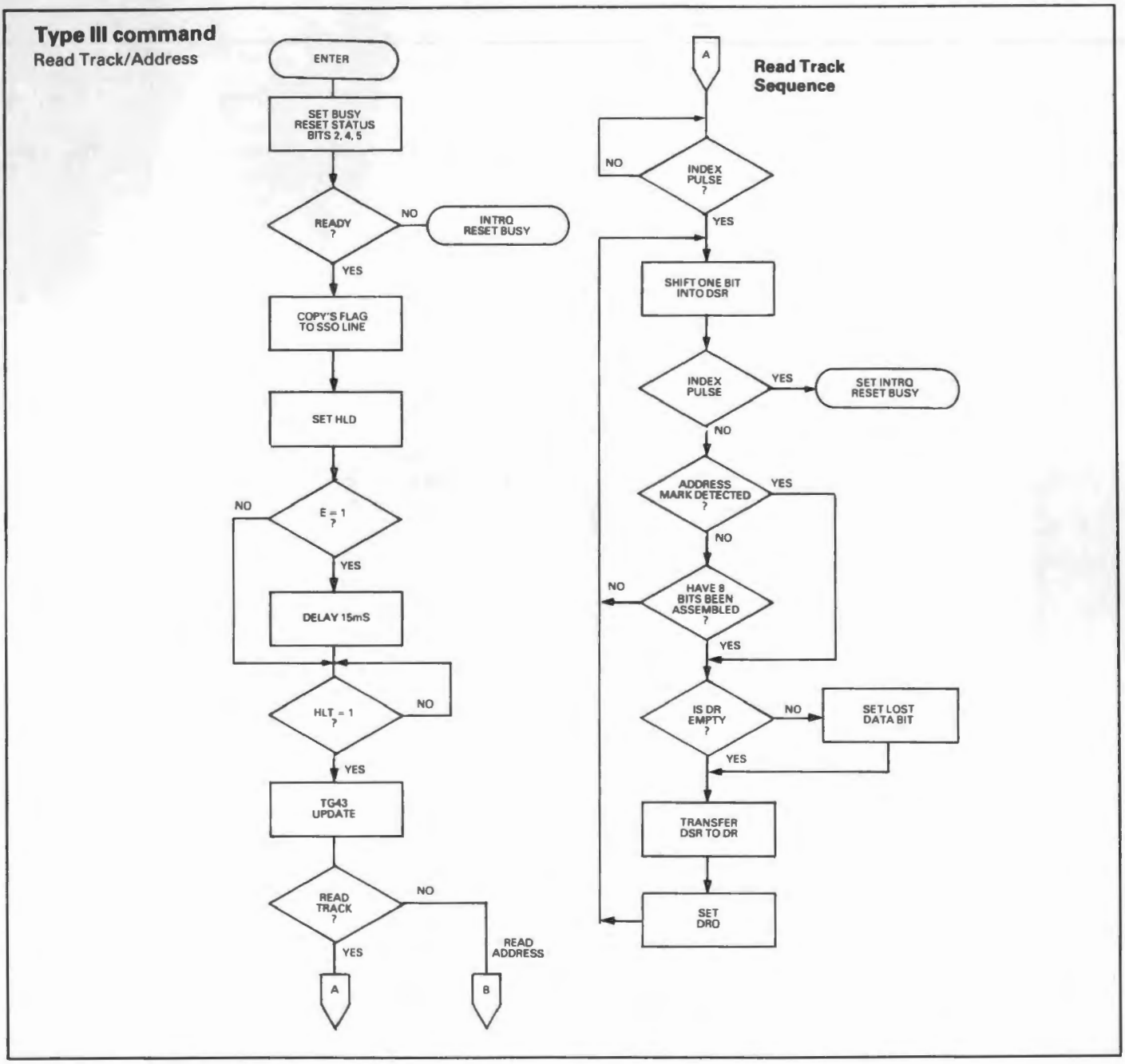
The Forced Interrupt command is generally used to terminate a multiple sector read or write command or to ensure Type I status in the status register. This command can be loaded into the command register at any time. If there is a current command under execution (busy status bit set) the command will be terminated and the busy status bit reset.

The lower four bits of the command determine the conditional interrupt as follows:

I_0 = Not-Ready to Ready Transition
I_1 = Ready to Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3-I_0) are set to a 1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I_3-I_0 are all set to zero (HEX D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I_3 = 1), an interrupt will be immediately generated and the current command

terminated. Reading the status or writing to the command register will not automatically clear the interrupt. The HEX D0 is the only command that will enable the immediate interrupt (HEX D8) to clear on a subsequent load command register or read status register operation. Follow a HEX D8 with D0 command.



Control bytes for initialisation

Table 5

Data Pattern in DR (HEX)	2797 Interpretation in FM ($\overline{DDEN}$ = 1)	2797 Interpretation in MFM ($\overline{DDEN}$ = 0)
00 through F4	Write 00 through F4 with CLK = FF	Write 00 through F4, in MFM
F5	Not allowed	Write $A1_1$, in MFM, Preset CRC
F6	Not allowed	Write $C2_2$ in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 through FB	Write F8 through FB, CLK = C7 Preset CRC	Write F8 through FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLK = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

Notes:
1 Missing clock transition between bits 4 and 5.
2 Missing clock transition between bits 3 and 4.

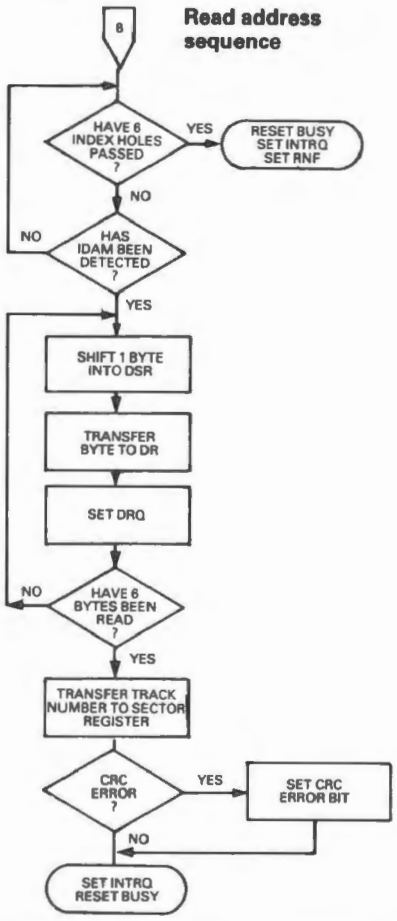
Wait 8 micro sec (double density) or 16 micro sec (single density) before issuing a new command after issuing a forced interrupt (times double when clock = 1MHz). Loading a new command sooner than this will nullify the forced interrupt.

Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are complete (CRC calculations, compares, etc.)

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX 'DA'. The 'OR' function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

Type III command

Read Track/Address



Status register

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy Status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQs to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 14.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are: (times double when clock = 1MHz 5¼in operation).

Operation	Next Operation	Delay Req'd. FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12μs	6μs
Write to Command Reg.	Read Status Bits 1-7	28μs	14μs
Write Any Register	Read From Diff. Register	0	0

IBM 3740 format – 128 bytes/sector

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one Data Request.

Table 6 **IBM 3740 format**

Number of Bytes	Hex value of Byte written
40	FF (or 00)[3]
6	00
1	FC (Index Mark)
26[1]	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 through 1A)
1	00 (Sector Length)
1	F7 (2 CRCs written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRCs written)
27	FF (or 00)
247[2]	FF (or 00)

1. Write bracketed field 26 times.
2. Continue writing until 2797 interrupts out. Approx. 247 bytes.
3. A '00' option is allowed on 2797 only.

IBM system 34 format

256 bytes/sector

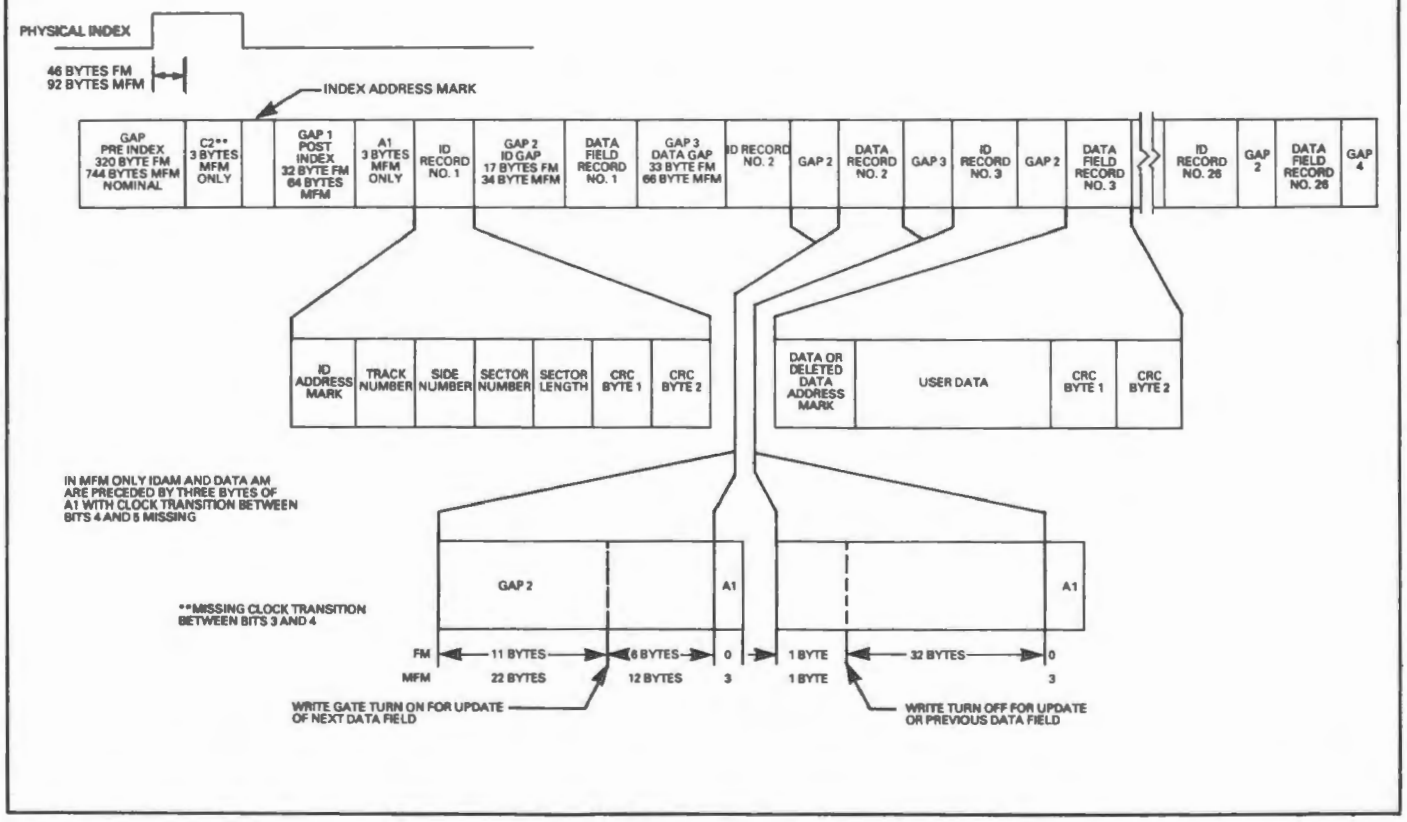
Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a disc the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

Table 7 **IBM system 34 format**

Number of Bytes	Hex value of Byte written
80	4E
12	00
3	F6 (Writes C2)
1	FC (Index Mark)
50[1]	4E
12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	Side Number (0 or 1)
1	Sector Number (1 through 1A)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598[2]	4E

[1] Write bracketed field 26 times.
[2] Continue writing until 2797 interrupts out. Approx. 598 bytes.

Figure 4 **IBM track format**



1. Non-IBM Formats

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 or 1024 bytes.
2) Gap 2 cannot be varied from the IBM format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the 2797. Gap 1, 3, and 4 lengths can be as short as 2 bytes for 2797 operation, however PLL lock up time, motor speed variation, write splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format be used for highest system reliability.

Table 10 **Non-IBM format**

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
note I	6 bytes 00	12 bytes 00
note I		3 bytes A1
Gap III note 2	10 bytes FF	24 bytes 4E
	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

Notes:

1. Byte counts must be exact.
2. Byte counts are minimum, except exactly 3 bytes of A1 must be written.

Timing characteristics

T_A = 0°C to 70°C, V_{SS} = 0V, V_{CC} +5V ± .25V

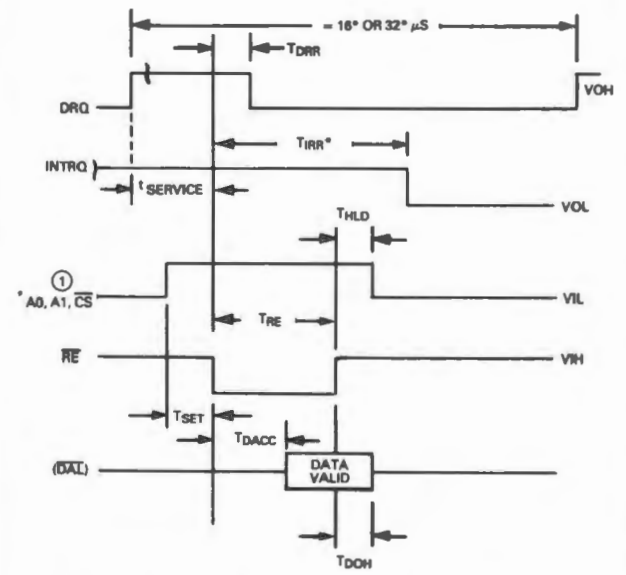
Table 8 **Read enable timing**

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
T_{SET}	Setup ADDR & $\overline{CS}$ to $\overline{RE}$	50			nsec	
T_{HLD}	Hold ADDR & $\overline{CS}$ from $\overline{RE}$	10			nsec	
T_{RE}	$\overline{RE}$ Pulse Width	200			nsec	C_L = 50 pf
T_{DRR}	DRQ Reset from $\overline{RE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{RE}$		500	3000	nsec	
T_{DACC}	Data Valid from $\overline{RE}$		100	200	nsec	C_L = 50 pf
T_{DOH}	Data Hold from $\overline{RE}$	20		150	nsec	C_L = 50 pf

Table 9 **Write Enable Timing**

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
T_{SET}	Setup ADDR & $\overline{CS}$ to $\overline{WE}$	50			nsec	
T_{HLD}	Hold ADDR & $\overline{CS}$ from $\overline{WE}$	10			nsec	
T_{WE}	$\overline{WE}$ Pulse Width	200			nsec	
T_{DRR}	DRQ Reset from $\overline{WE}$		100	200	nsec	
T_{IRR}	INTRQ Reset from $\overline{WE}$		500	3000	nsec	
T_{DS}	Data Setup to $\overline{WE}$	150			nsec	
T_{DH}	Data Hold from $\overline{WE}$	20			nsec	

Figure 5 **Read enable timing**



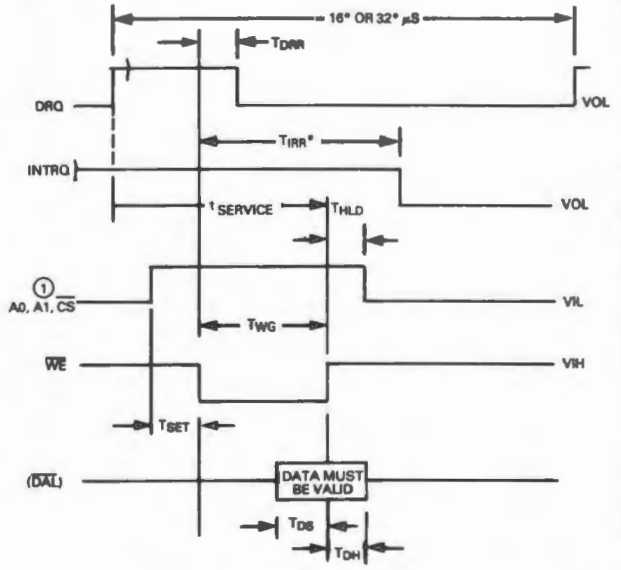
NOTE 1 CS MAY BE PERMANENTLY TIED LOW IF DESIRED
*TIME DOUBLES WHEN CLOCK = 1MHz.

t SERVICE (WORST CASE)
*FM = 27.5µS
*MFM = 13.5µS

DRQ RISING EDGE: INDICATES THAT THE DATA REGISTER HAS ASSEMBLED DATA.

DRQ FALLING EDGE: INDICATES THAT THE DATA REGISTER WAS READ
INTRQ RISING EDGE: OCCURS AT END OF COMMAND.
INTRQ FALLING EDGE: INDICATES THAT THE STATUS REGISTER WAS READ.

Figure 6 **Write enable timing**



NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED
2. WHEN WRITING DATA INTO SECTOR TRACK OR DATA REGISTER USER CANNOT READ THIS REGISTER UNTIL AT LEAST 4µSEC IN MFM AFTER THE RISING EDGE OF WE WHEN WRITING INTO THE COMMAND REGISTER STATUS IS NOT VALID UNTIL SOME 28µSEC IN FM. 14µSEC IN MFM LATER THESE TIMES ARE DOUBLED WHEN CLK = 1MHz.

t SERVICE (WORST CASE)
*FM = 23.5µS
*MFM = 11.5µS

*TIME DOUBLES WHEN CLOCK = 1MHz.

DRQ RISING EDGE: INDICATES THAT THE DATA REGISTER IS EMPTY
DRQ FALLING EDGE: INDICATES THAT THE DATA REGISTER IS LOADED.
INTRQ RISING EDGE: INDICATE THE END OF A COMMAND.
INTRQ FALLING EDGE: INDICATES THAT THE COMMAND REGISTER IS WRITTEN TO.

Table 11 **Input data timing**

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
T_{PW}	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	
T_{BC}	$\overline{\text{Raw Read}}$ Cycle Time	1500	2000		nsec	

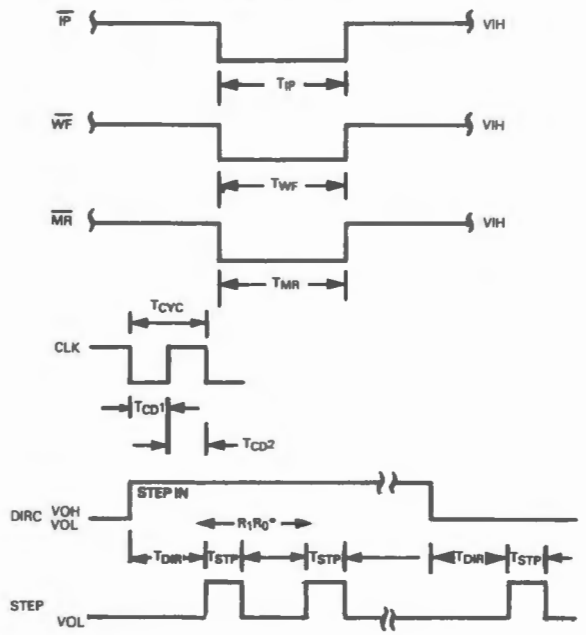
Table 12 **Write data timing: (all times double when CLK = 1MHz 5¼in operation)**

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
T_{WP}	Write Data Pulse Width	400	500	600	nsec	FM
		240		1000	nsec	MFM
T_{WG}	Write Gate to Write Data		2		µsec	FM
			1		µsec	MFM
T_{WF}	Write Gate off from WD		2		µsec	FM
			1		µsec	MFM

Table 13 **Miscellaneous timing:**

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
T_{CD^1}	Clock Duty (low)	230	250	20000	nsec	
T_{CD^2}	Clock Duty (high)	230	250	20000	nsec	
T_{STP}	Step Pulse Output	2 or 4			µsec	See Note
T_{DIR}	Dir Setup to Step		12		µsec	± CLK ERROR
T_{MR}	Master Reset Pulse Width	50			µsec	
T_{IP}	Index Pulse Width	10			µsec	See Note
RPW	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
WPW	Write Data Pulse Width					Input 0-5V
		300		1000	nsec	MFM
			500		nsec	FM
	Precomp Adjust.	100		250	nsec	MFM
RPW	Read Window Pulse Width					Input 0-5V
		120		700	nsec	MFM
		240		1400	nsec	FM ± 15%
WPW	Write Data Pulse Width					Input 0-5V
		300		1000	nsec	MFM
			500		nsec	FM
	Precomp Adjust.	100		250	nsec	MFM
VCO	Free Run Voltage Controlled	6.0			MHz	Ext. C = 0
	Oscillator. Adjustable by ext. capacitor on Pin 26		4.0		MHz	Ext. C = 35pf
	Pump Up + 25%	5.0			MHz	PU = 2.2V Cext = 35pf
VCO	Pump Down –25%			3.0	MHz	$\overline{\text{PD}}$ = 0.2V Cext = 35pf
VCO	5% Change V_{CC}	3.8		4.2	MHz	Cext = 35pf
	T_A = 75°C	3.5			MHz	Cext = 35pf
Cext	Necessary external capacitor	10	35	80	pf	VCO = 4.0MHz nom
RCLK	Derived read clock = VCO ÷ 8, 16, 32					VCO = 4.0MHz
			500		KHz	$\overline{\text{DDEN}}$ = 0 5/8 = 1
			250		KHz	$\overline{\text{DDEN}}$ = 0 5/8 = 0
			250		KHz	$\overline{\text{DDEN}}$ = 1 5/8 = 1
			125		KHz	$\overline{\text{DDEN}}$ = 1 5/8 = 0
PU/DON	PU/$\overline{\text{PD}}$ time on (pulse width)			250	ns	MFM
				500	ns	FM

Figure 7 **Miscellaneous timing**



Notes:

1. Times double when clock = 1 MHz 5¼in operation.
2. Output timing readings are at V_{OL} = 0.8v and V_{OH} = 2.0v.

Figure 8 **Write data timing**

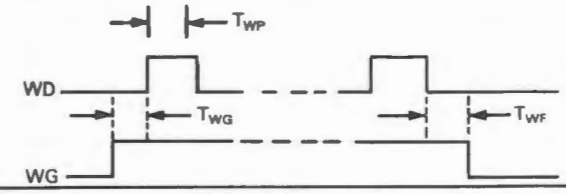


Figure 9 **Read data timing**

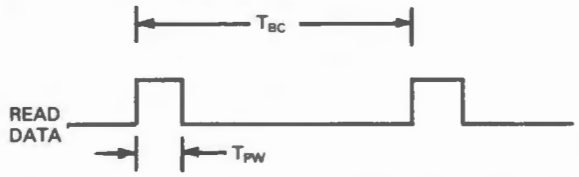


Table 14 **Status register summary**

Bit	All Type I Commands	Read Address	Read Sector	Read Track	Write Sector	Write Track
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX PULSE	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Table 15 **Status for Type I commands**

Bit Name	Meaning
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with $\overline{MR}$.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical 'and' of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

Table 16 **Status for Type II and III commands**

Bit Name	Meaning
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with $\overline{MR}$. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: Forced to a Zero.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side was not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

Summary of adjustment procedure

Write Precompensation

1) Set $\overline{TEST}$ (Pin 22) to a logic high.
2) Strobe $\overline{MR}$ (Pin 19).
3) Set $\overline{TEST}$ (Pin 22) to a logic low.
4) Observe pulse width on WD (Pin 31).
5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
6) Set $\overline{TEST}$ (Pin 22) to a logic high.

Data Separator

1) Set $\overline{TEST}$ (Pin 22) to a logic high.
2) Strobe $\overline{MR}$ (Pin 19). Ensure that 5/8, and $\overline{DDEN}$ are set properly.
3) Set $\overline{TEST}$ (Pin 22) to a logic low.
4) Observe Pulse Width on TG43 (Pin 29).
5) Adjust RPW (Pin 18) for 1/8 of the read clock (250ns for 8in DD, 500ns 5¼in DD, etc.).
6) Observe Frequency on DIRC (Pin 16).
7) Adjust variable capacitor on VCO pin for Data Rate (500KHz for 8in DD, 250KHz for 5¼in DD, etc.)
8) Set $\overline{TEST}$ (Pin 22) to a logic high.

NOTE: To maintain internal VCO operation, ensure that $\overline{TEST}$ = 1 whenever a master reset pulse is applied.

General disc information

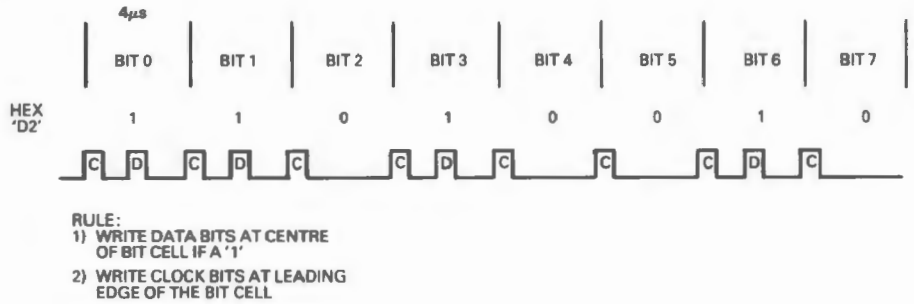
Table 17 **Storage capacities for different disc types**

Size	Density	Sides	Unformatted Capacity (Nominal)		Byte Transfer Time	Formatted Capacity	
			Per Track	Per Disc		Per Track	Per Disc
5¼in	SINGLE	1	3125	109,375[1]	64μs	2304[2]	80,640
5¼in	DOUBLE	1	6250	218,750	32μs	4608[3]	161,280
5¼in	SINGLE	2	3125	218,750	64μs	2304	161,280
5¼in	DOUBLE	2	6250	437,500	32μs	4608	322,560
8in	SINGLE	1	5208	401,016	32μs	3328	256,256
8in	DOUBLE	1	10,416	802,032	16μs	6656	512,512
8in	SINGLE	2	5208	802,032	32μs	3328	512,512
8in	DOUBLE	2	10,416	1,604,064	16μs	6656	1,025,024

Notes:

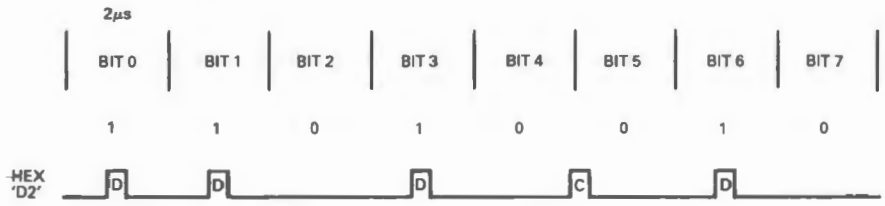
1. Based on 35 Tracks/Side.
2. Based on 18 Sectors/Track (128 byte/sec).
3. Based on 18 Sectors/Track (256 bytes/sec).

Figure 10 **FM Recording**



RULE:
1) WRITE DATA BITS AT CENTRE OF BIT CELL IF A '1'
2) WRITE CLOCK BITS AT LEADING EDGE OF THE BIT CELL

Figure 11 **MFM Recording**



RULE:
1) WRITE DATA BITS AT CENTRE OF BIT CELL IF A '1'
2) WRITE CLOCK BITS AT LEADING EDGE OF THE BIT CELL IF:
A) NO DATA BIT HAS BEEN WRITTEN LAST
–AND–
B) NO DATA BIT WILL BE WRITTEN NEXT

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RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company

Telephone: 0536 201234
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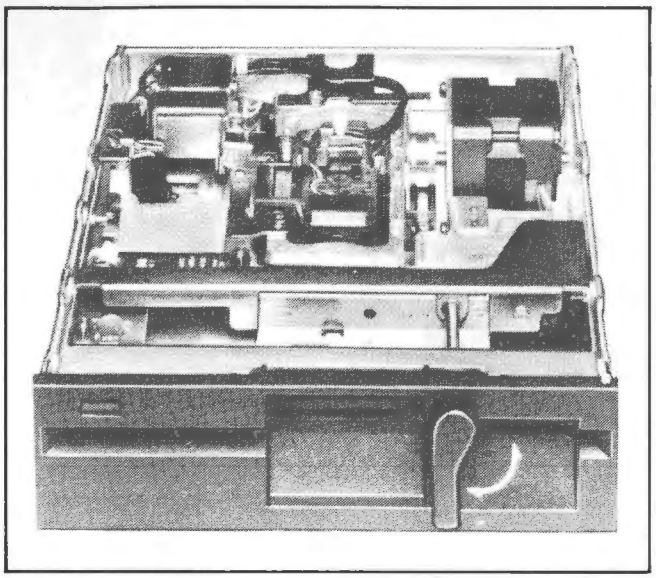
RS data

Floppy disc drives and accessories (5¼in)



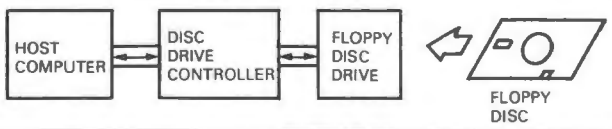
This data sheet covers the following stock numbers:

Stock No.	Description
300-142	Floppy Disc Drive, single sided 40 track, 48 TPI
300-760	Floppy Disc Drive, double sided 40 tracks per side, 48 TPI
300-158	Floppy Disc Drive, double sided 80 tracks per side, 96 TPI
300-164	Floppy Disc Drive Controller Board
300-170	Floppy Disc Drive Alignment Disc
591-972	Disc Drive Power Supply
501-626	Floppy Disc Drive Case

Floppy disc drives

Floppy Disc Drives (FDDs) are precision magnetic recording instruments with a digital interface, making them particularly suitable for high capacity storage with fast access digital systems. Typical system connection is shown below:

Figure 1 **Typical system connection**

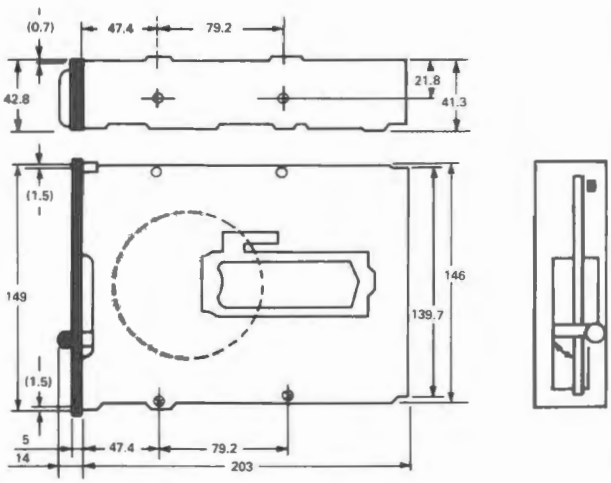


The host computer processes data which is accessed via the disc drive controller. The controller organises the packaging, formatting and timing of the floppy disc data. The floppy disc drive contains Read/Write and motion control electronics for storing, selecting and reading data from the disc.

Features

- Compatibility with industry standard S.400 (Shuggart) controller drive signal interface.
- Long life zinc-ferrite head, gimbal supported to ensure accurate tracking.
- Increased reliability and low power consumption provided by two custom LSIs which control read/write functions.
- Simple system planning with low power/heat generation, allowing smaller power supplies.
- Perfect disc centering. When the disc is inserted, the spindle motor automatically runs for 10 seconds ensuring perfect disc registration as it is clamped down.
- Durable motor (lifetime over 10,000 hr) can be left running continuously to eliminate start-up time, allowing faster data access.
- The electrical noise caused by brushes in conventional motors has been eliminated using a brushless dc direct drive motor.
- High speed data retrieval enabled by fast track to track access times (3ms in FD55F).
- Increased data security achieved by head load solenoid and voltage sensing circuit which prevents spurious writes when power switched on and off.
- High precision and reliability using solid state LED/photo sensor system for write protect, index and track 00 sensing.
- Precision head tracking using high accuracy band positioning system with stepper motor.
- Protection against accidental erasure.
- Daisy chain up to four drives.
- Compatible with RS floppy disc drive controller board or can be used with the RS2797 floppy disc drive controller i.c. (refer to Semiconductors section of current RS catalogue), where disc drive control circuitry is not provided.
- Power supply and case available.

Figure 2 **Physical details**



Specification

Recording method:
FM (single density), MFM (double density)

Motor starting time: 400ms

MTBF: more than 10,000 hours

Error rates:
Soft errors: 1 per 10^9 bits (up to 2 retries)
Hard errors: 1 per 10^{12} bits
Seek errors: 1 per 10^6 seeks

Temperature:
Operating: +4°C to +46°C
Transportation: –40°C to +65°C
Storage: –22°C to +60°C

Relative humidity
Operating: 20 to 80% (non-condensing)
Maximum wet bulb temperature: +29°C.
Transportation: 5 to 95% (non-condensing)
Maximum wet bulb temperature +45°C.
Storage: 10 to 90% (non-condensing)
Maximum wet bulb temperature +40°C.

Window margin
> ± 600ns (Bit cell centre)

Write compensation:
125ns (for MFM recording)

Power requirements:
DC + 12V ± 5% 0.25 A Typ., 0.9 A max.
DC + 5V ± 5% 0.38 A typ., 0.6 A max.

Power consumption
Operating: 4.9W
Non-operating: 1.6W

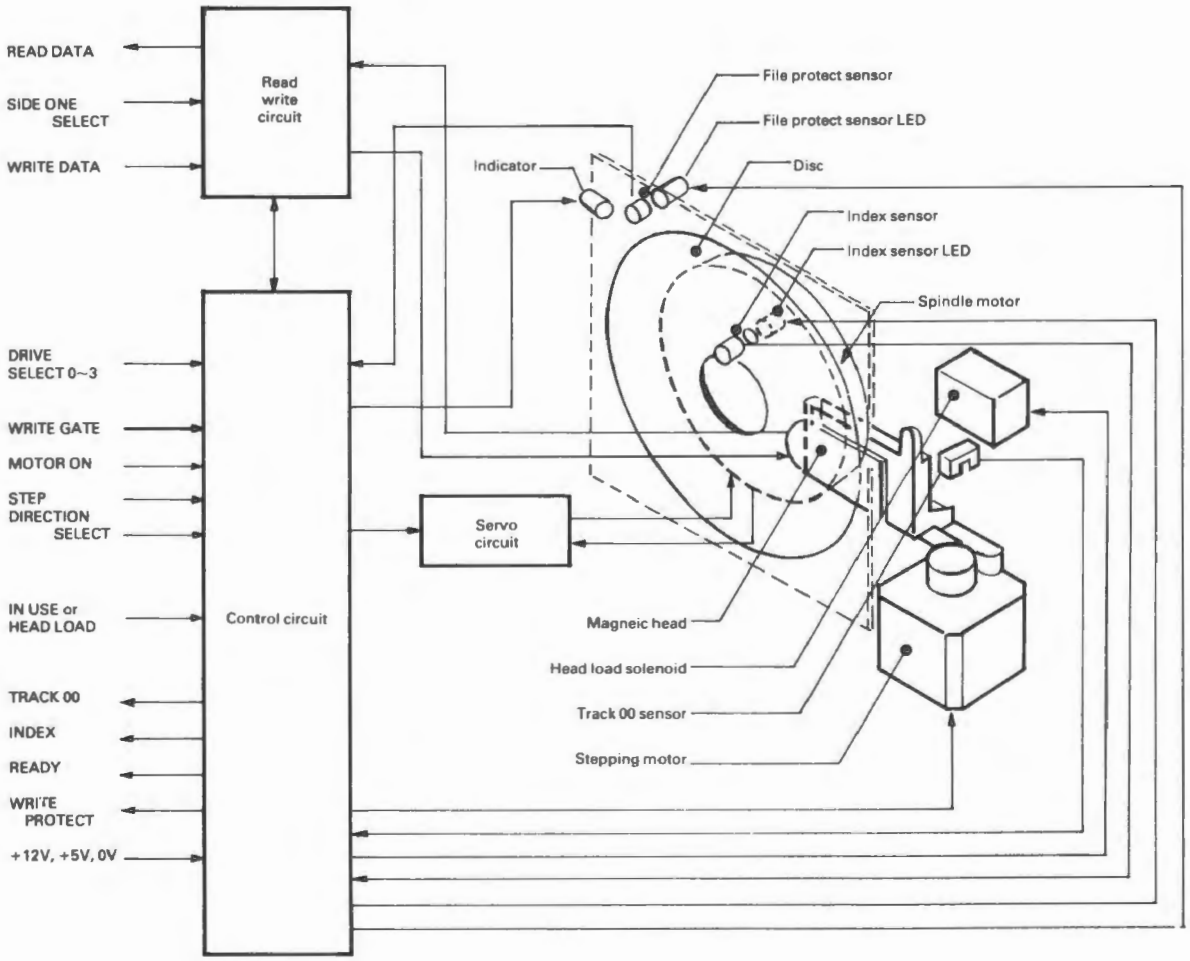
Dimensions:
(W x H x D): 146 x 41 x 203mm
(5¾in x 1⅝in x 8in)

Weight:
less than 1.5kg (3lb 5oz)

Component life:
5 years

Safety standard:
Complying with UL and CSA

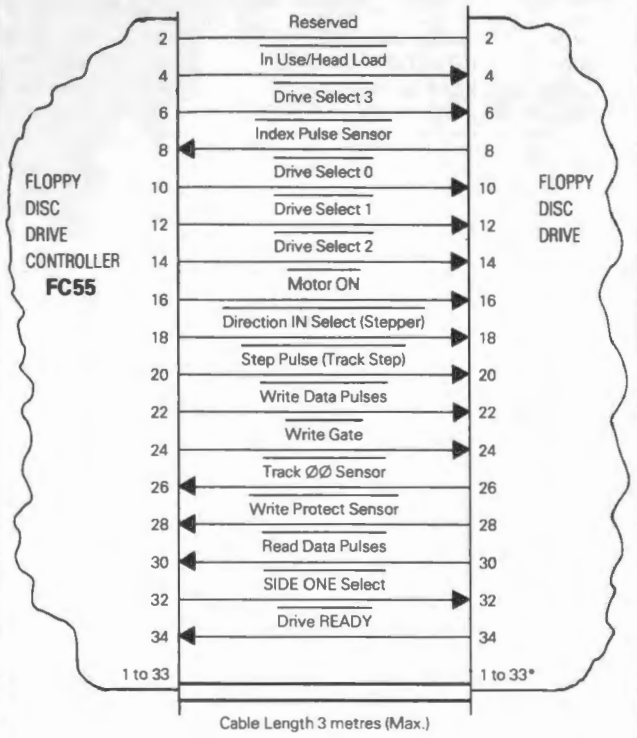
Figure 3 **General block diagram**



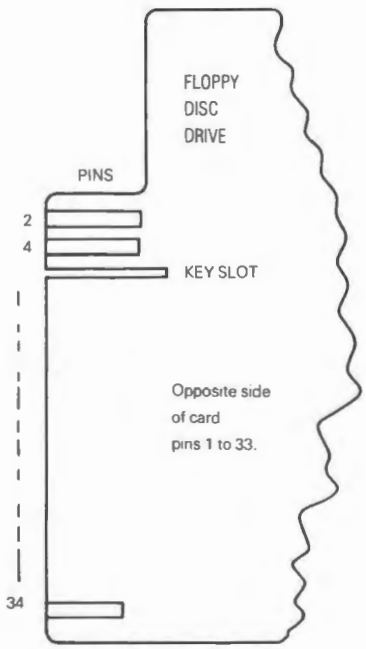
Interfacing

The RS disc drives conform to the industry standard S.400 controller/drive signal interface, where normal TTL logic levels apply, TRUE being active low. Pin layouts and designations are given below:

Figure 4 **Pin layouts and designations**



* Pins 1-33 Signal OV Guard lines.



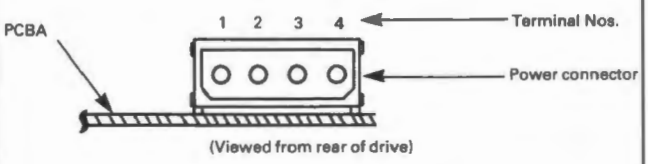
For suitable connector refer to the current RS catalogue: 34-way IDC card edge connector, inter-contact polarising key between contacts 4 and 6, stock number 471-288. For information on the host computer to controller interface see section of this data sheet on Floppy Disc Drive controller board.

Power cable

Any appropriate cable capable of taking the maximum drive power consumption and power voltage will be acceptable. The cable should be kept as short as possible to avoid noise generation.

For suitable cable connector refer to the current RS catalogue: 4 way in-line disc drive power socket housing, stock number 471-424.

Figure 5 **Drive power connections**

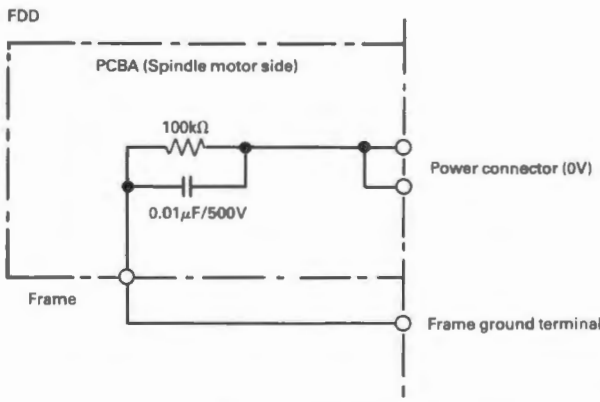


Voltage	Terminal Nos.
DC + 12V	1
0V	2
0V	3
DC + 5V	4

Frame Grounding

For suitable cable connector refer to connectors section of current RS catalogue: 0.187in push-on in-line receptacle connector.

Figure 6 **Frame grounding**



Track density

For a 40 Track drive this is 48 Tracks Per Inch (TPI) and 96 TPI for an 80 Track drive. 96 TPI drives require the best available Floppy Disc Media such as 96 TPI RS Magnetic Media to guarantee reliable storage and recovery of data.

Formatting

This is dependent on the Disc Controller and is the process that divides a blank magnetic disc into tracks and the tracks into sectors. Each sector has an address block which allows an individual length of track to be identified and accessed. Recommended formats are given below. For further information consult the RS FC55 Controller user instructions or the RS2797 disc drive controller I.C. Data Sheet (number 5409).

Table 1 **Formatting specification**

Stock number			**300-142**		**300-760**		**300-158**		**Units**
Disc Drive Type			FD-55A		FD-55B		FD-55F		
Recording Method			FM	MFM	FM	MFM	FM	MFM	
Transfer Rate			125	250	125	250	125	250	k bits/sec
Capacity	Unformatted	Per Track	3.125	6.25	3.125	6.25	3.125	6.25	k bytes
		Per Disc	125	250	250	500	500	1000	
	Formatted (16 sectors/track)	Per Sector	0.128	0.256	0.128	0.256	0.128	0.256	
		Per Track	2.048	4.096	2.048	4.096	2.048	4.098	
		Per Disc	81.92	163.84	163.84	327.68	327.68	655.36	
Inside Track Recording Density			2768	5536	2938	5876	2961	5922	bpi
Inside Track Flux Density			5536		5876		5922		frpi
Tracks/Disc			40		80		160		
Track Density			48		48		96		tpi
Track radius		Outside	57.150		57.150 side 0 55.033 side 1		57.150 side 0 55.033 side 1		mm
		Inside	36.513		36.513 side 0 34.396 side 1		36.248 side 0 34.131 side 1		mm
Average Access Time			93		93		94		ms
Track Access Time			6		6		3		
Settling Time			15		15		15		
Disc Rotational Speed			300		300		300		rpm

Note: bpi = bits per inch frpi = flux reversals per inch tpi = tracks per inch

Recording method and media selection

There are two recording methods in common use, Frequency Modulation (FM) and the less reliable but double capacity Modified Frequency Modulation (MFM). These are selected at the Disc Controller. Where MFM recording is chosen a phase locked data separator is recommended to compensate for bit jitter on the Read Data line from the drive.

Figure 7 **FM recording**

FM (frequency modulation) encoding has the following rules:

A. A data bit, if it is a '1', occurs at the centre of the bit cell.

B. A clock bit occurs at the start of the bit cell.

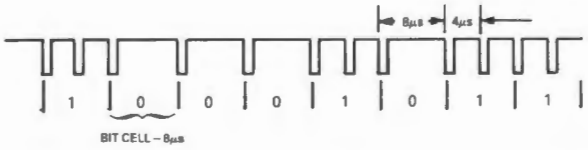
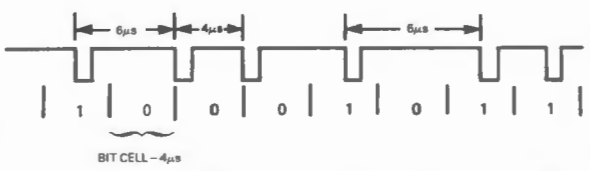


Figure 8 **MFM recording**

MFM (modified FM) encoding has the following rules:

A. A data bit, if it is a '1', occurs at the centre of the bit cell.

B. A clock bit occurs at the start of the bit cell, but only if no data bit occurred in the previous bit cell and no data bit will occur in the current bit cell.



For FM recording single density media is required, and for MFM recording double density media is necessary. When using double density at 96TPI it is usually necessary to employ a technique called 'Write Precompensation' at the controller to ensure reliable recovery of data from the inner tracks. For MFM recording using the FD55F disc drive a value of 125ns for write precompensation is recommended.

Read compatibility between drives

This depends on optimum head radial alignment to the Disc Centre Datum Point. To achieve this an Alignment Disc is required. For further information consult the Alignment Disc section of this data sheet.

Input/Output signals

Input signals are those received by the FDD while output signals are those transmitted from the FDD. True is active low.

Drive select 0-3 input signals

The DRIVE SELECT lines provide a means of selecting and deselecting the drives. Four separate DRIVE SELECT lines are provided so that up to four drives may be connected to a single controller. By placing only one of these jumpers in each drive, only one drive will be selected when activating any one of the DRIVE SELECT lines, provided the MX strap is removed.

When the signal level is true (low), the disc drive electronics are activated, and the drive is conditioned to respond to step or read/write commands. When the signal level is false (high), the input control lines (except motor ON) and output status lines are disabled.

A delay time of 0.5μsec max. (including delay time through the interface cable) must be allowed before other input/output signals are effective.

Motor on input signal

The spindle motor reaches the rated rotational speed within 40msec after this signal becomes true.

Direction select input signal

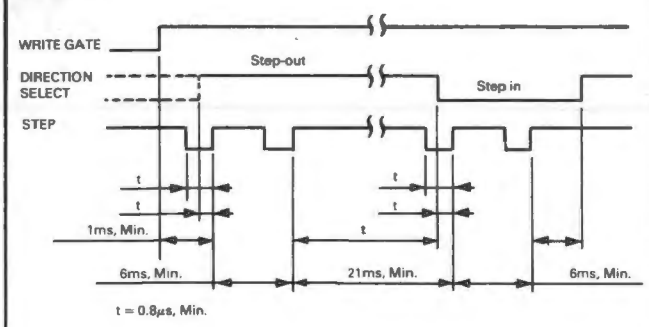
The direction of motion of the Read/Write head is defined by the state of this input line. A true (low) level defines direction as 'IN' (towards centre of the disc); a false (high) level defines the direction as 'OUT'.

Step input signal

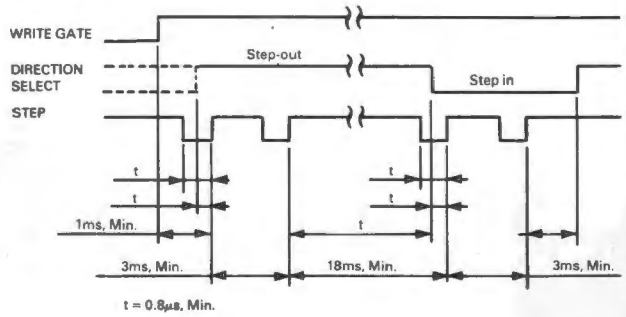
A single pulse on this input will move the Read/Write head one track in or out, dependent on the state of the DIRECTION SELECT line. The motion of the head is initiated on the trailing edge of STEP pulse. A minimum of a 0.8μs pulse width at a maximum frequency of 333Hz for 96 TPI (3ms track to track); 167Hz for 48 TPI (6ms track to track) should be maintained to ensure step integrity.

Figure 9 **Step timing**

9a 48 TPI



9b 96 TPI



Write gate input signal

When true, this input line permits writing of data. When inactive, it permits transmission of data to the controller. This signal is ineffective when the write protect signal is true. This signal should be made true only after satisfying all of the following four conditions:

i) FDD is in ready state.
ii) More than 35msec after head loading started.
iii) More than 18msec after receiving final STEP pulse.
iv) More than 100μsec after a level change of the SIDE ONE SELECT signal.

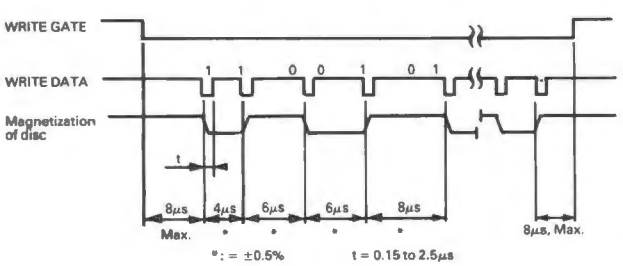
Allow a minimum of 1ms after dropping WRITE GATE before:

i) Stopping spindle motor.
ii) Making drive select signal false.
iii) Moving head with STEP pulse.
iv) Changing sides with SIDE ONE SELECT input signal.

Write data input signal

The frequency of the WRITE DATA is dependent upon the encoding scheme used, the density option exercised, and the data pattern to be written. The write oscillator frequency stability should be held to 0.5%. The data pulse width should be a minimum of 0.15μs and a maximum of 2.5μs wide. WRITE DATA is effective when WRITE GATE is true and WRITE PROTECT is false. It is recommended that the leading edge of the first WRITE DATA pulse occurs no sooner than 4μs and no later than 8μs after the leading edge of the WRITE GATE true signal. The WRITE GATE false signal should occur no sooner than 4μs and no later than 8μs after the last data pulse.

Figure 10 **WRITE DATA timing (MFM method)**



Side one select input signal

This input is used to select either the upper or lower head. The signal is false (high) to select side 0 and true (low) for side 1. A 100μsec delay should be allowed after a head select event occurs. Only then will valid data be present. When the other side of the disc is selected after the completion of a write operation, a 1ms delay should be allowed after making the WRITE GATE signal false.

In Use/Head Load input signal

The function of this signal is selected by the IU and HL selection links.

(a) When IN USE function is selected:

Signal to indicate that the FDD is in use under the control of the host system, by illumination of front bezel indicator.

(b) When HEAD LOAD function is selected:

This signal, when true loads the head. Head loading can be executed only when the FDD is in a ready or pre-ready state (see READY OUTPUT signal).

Allow a minimum 35msec settling delay after the start of the head load operation, before data read or write operations. If the MX link is on, head loading starts when this signal becomes TRUE.

If the MX link is off (multiple drive systems), the head loading starts when both the DRIVE SELECT signal (DS0 to DS3) of the relevant drive and this signal becomes true.

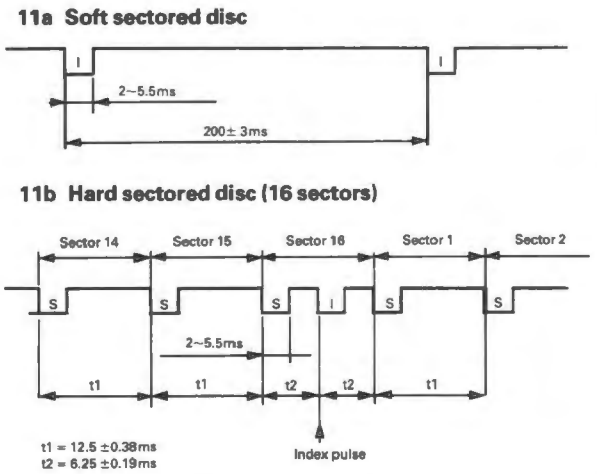
Track 00 output signal

This output, when true, indicates that the Read/Write head(s) are located over TRACK 00. Allow 2.8msec after the STEP pulse for this signal to become valid.

Index/Sector output signal

When utilizing a soft-sectored disc an INDEX pulse is transmitted to the controller once every revolution indicating the beginning of a track. If a hard-sectored disc is utilized, one SECTOR pulse for every sector in addition to one INDEX pulse per revolution will be transmitted to the controller.

Figure 11 **INDEX/SECTOR timing**



Read data output signal

This output represents data consisting of encoded clock and data bits. The pulse width of both clock and data bits will be 1μsec ±0.5μsec. The leading edge of each READ DATA pulse represents the true position of the flux transition on the recording media.

This signal becomes valid when all the following five conditions are satisfied:

i) The FDD is in a ready state (refer to READY output signal).

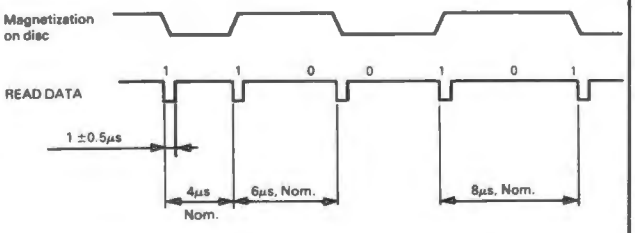
ii) More than 35msec after head loading has started.

iii) More than 18msec (96 TPI) and 21msec (48 TPI) after final STEP pulse receipt.

iv) More than 1msec after WRITE GATE signal becomes false.

v) More than 100μmsec after a level change of the SIDE ONE SELECT signal for double sided drives.

Figure 12 **READ DATA timing (MFM method)**



Note: The displacement of any bit position does not exceed ±20% from its nominal position.

Write protect output signal

This signal indicates the write enable notch of the floppy disc is masked.

When this signal is true, the data on the disc is protected from erasure and the writing of new data is inhibited.

Ready output signal

This signal indicates that the FDD is in a ready state.

For soft sectored discs, the READY output signal is true when all of the following five conditions are satisfied:

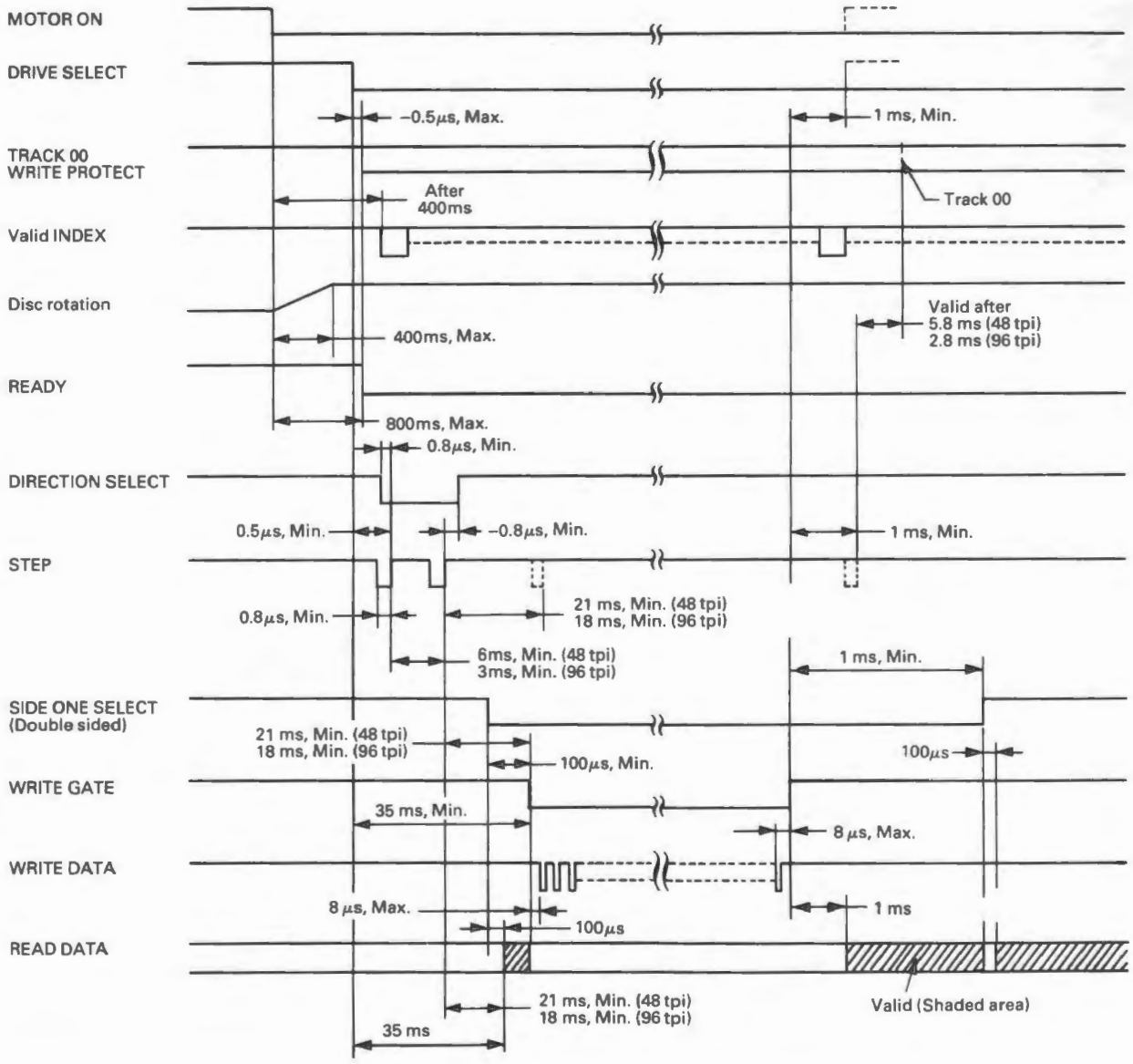
i) The FDD is powered on.
ii) The floppy disc is inserted.
iii) The disc rotates at more than 50% of the rated speed.
vi) Two INDEX pulses have been counted after item iii) is satisfied.
v) Allow >800msec after the spindle motor has started.

Note: Pre-ready is the state where at least one INDEX pulse has been detected after item iii) is satisfied.

For hard sectored discs, the READY output signal is true when all of the following three conditions are satisfied:

i) The FDD is powered on.
ii) The floppy disc is inserted.
iii) Allow >400msec after the spindle motor has started.

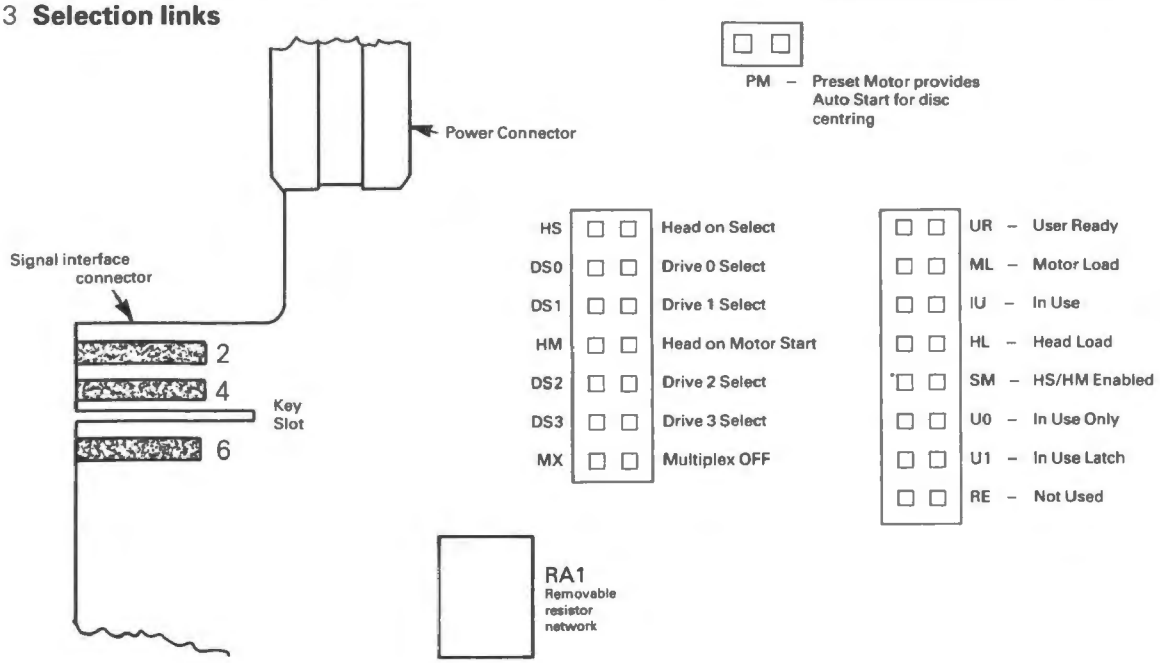
Table 2 **Composite control timing**



Selection links

Insertion of a selection link defines the ON condition of that link.

Figure 13 **Selection links**



Links can be configured in a variety of positions, the more useful configurations using the links supplied are:

Table 3 **Selectable links**

Link Configurations	Turn ON conditions for			Comments
	Head load solenoid	Spindle motor	Front LED	
1. DSO HS SM IU	DSO line active	Motor ON line active	DSO or IN USE line active	Drive supplied in this configuration
2. DSO HM SM IU	Motor ON line active and DRIVE READY	Motor ON line active	DSO or IN USE line active	Motor On to DRIVE READY 400ns
3. DSO HS SM ML	DSO line active	DSO or Motor ON lines active	DSO line active	Conserves Motor Power to one drive
4. DSO HS HL ML	IN USE line active	DSO or Motor ON lines active	DSO line active	Separate Head Load Facility
5. DSO HS SM UR	DSO line active	Motor ON line active	READY line active	Front Indication of READY status
6. DSO HL IU ML	DSO line or IN USE lines active	DSO or IN USE or MOTOR ON lines active	DSO line or IN USE lines active	Most flexible configuration

Drive multiplexing of floppy disc drives

MX link

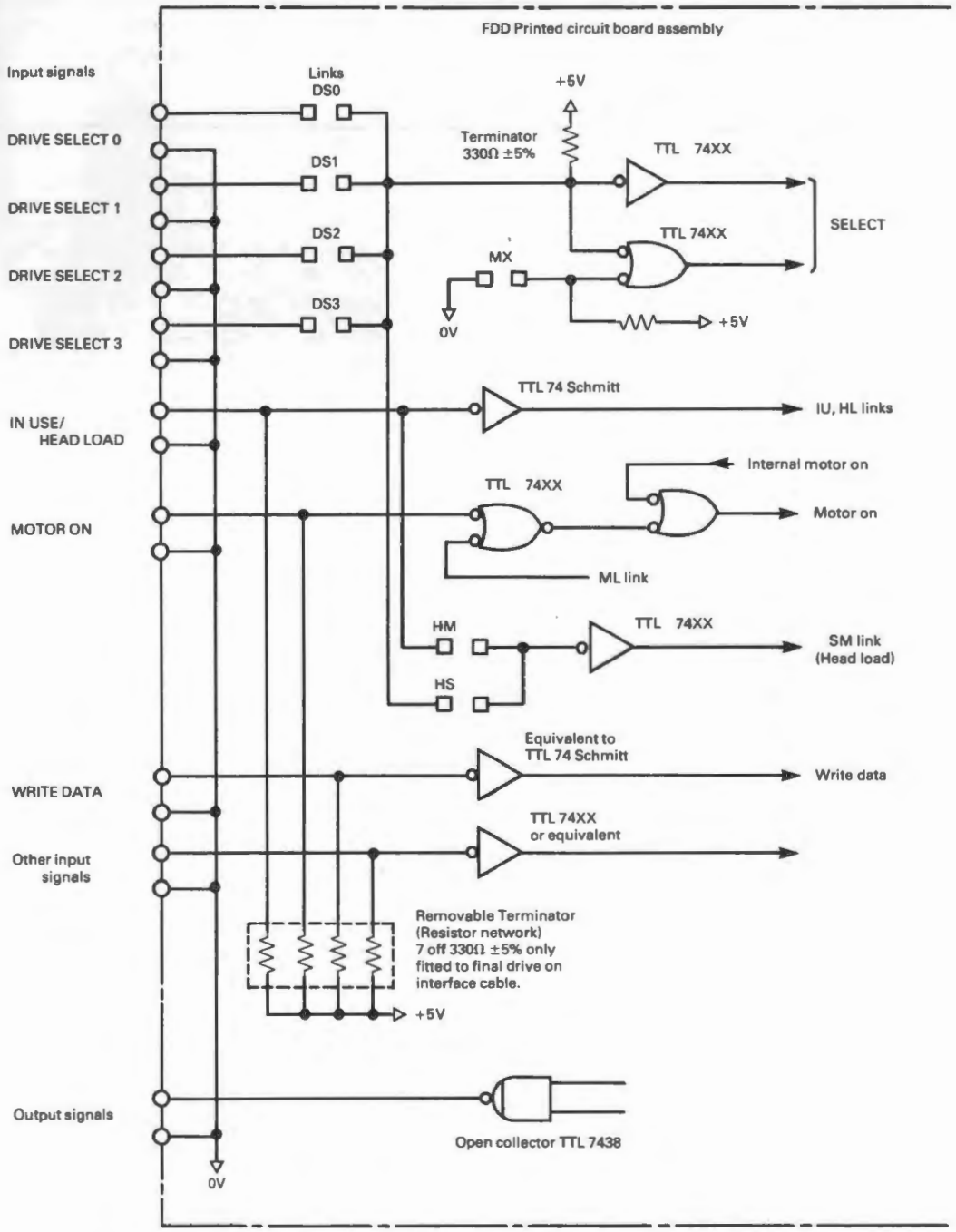
The on-state of this link is used when only one FDD is connected to the system. All the input/output signals act independently of the DRIVE SELECT 0 to 3 signals. At the off-state of this link, 4 FDDs, Max. can be controlled by daisy chaining.

This link has no relation to the turn-on condition of the front bezel indicator or the rotating condition of the spindle motor.

Terminators

330Ω Terminator resistors for Drive Select 0 to 3 input signals are soldered in. A terminator resistor network for other drive functions is mounted on an IC socket on the PCB at shipment. This removable resistor network should be removed from all FDDs except the final FDD in a multiple daisy-chain connection.

Figure 14 **Terminators**



Drive Select 0 to 3: radial connection.

In Use, Motor ON, Direction Select, Step Pulse, Write Data, Write Gate, Side One Select: Daisy Chain connection.

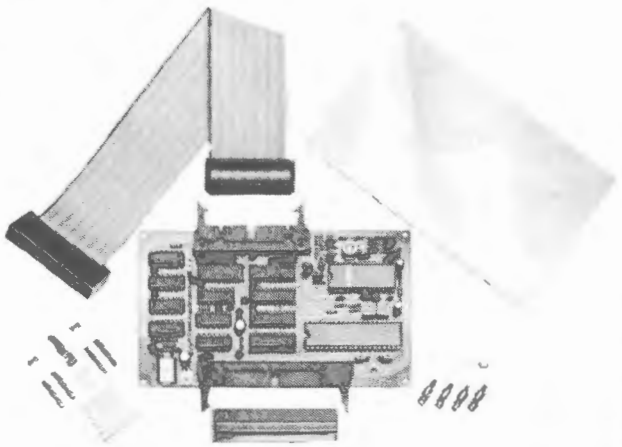
All Input/Output signals only active with selected drive in daisy chain connection.

Floppy disc drive controller board

The RS FC55 Floppy Disc Drive Controller Board allows direct connection of floppy disc drives to microprocessor bus lines.

Supplied complete with drive cable assembly, 50-way IDC host system connector, mounting plate mounting hardware and user instructions. It is fully compatible with the RS FD55 series floppy disc drives.

Figure 15



Features

- Uses the highly reliable, multi-function 1793 floppy disc formatter/controller LSI chip (Western Digital FD1793)
- Uses either double-density MFM or single-density FM recording format
- Up to four drives may be connected
- Can be used with double-sided type drives
- IBM sector format compatible
- Automatic track seek and verify
- Performs either single or chained sector reads and sector writes
- Software settable sector length
- Data may be transferered via DMA or under program control
- Interface levels are TTL compatible
- A data separator using a VFO is built in
- Write precompensation circuit built in
- The controller is constructed on a single, compact printed circuit board and can be attached directly to the frame of RS FD55 series drives

Figure 16 **Block diagram**

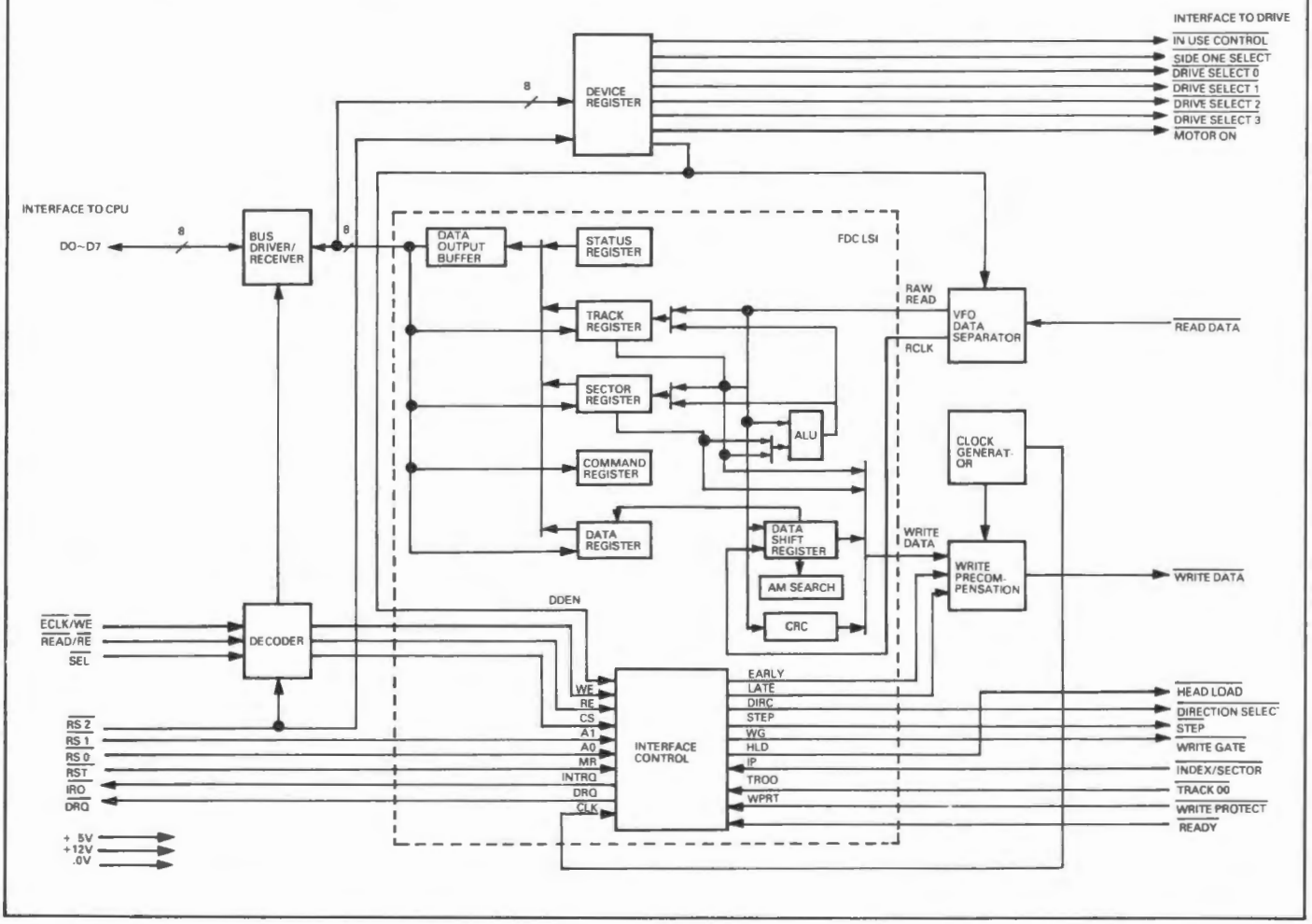
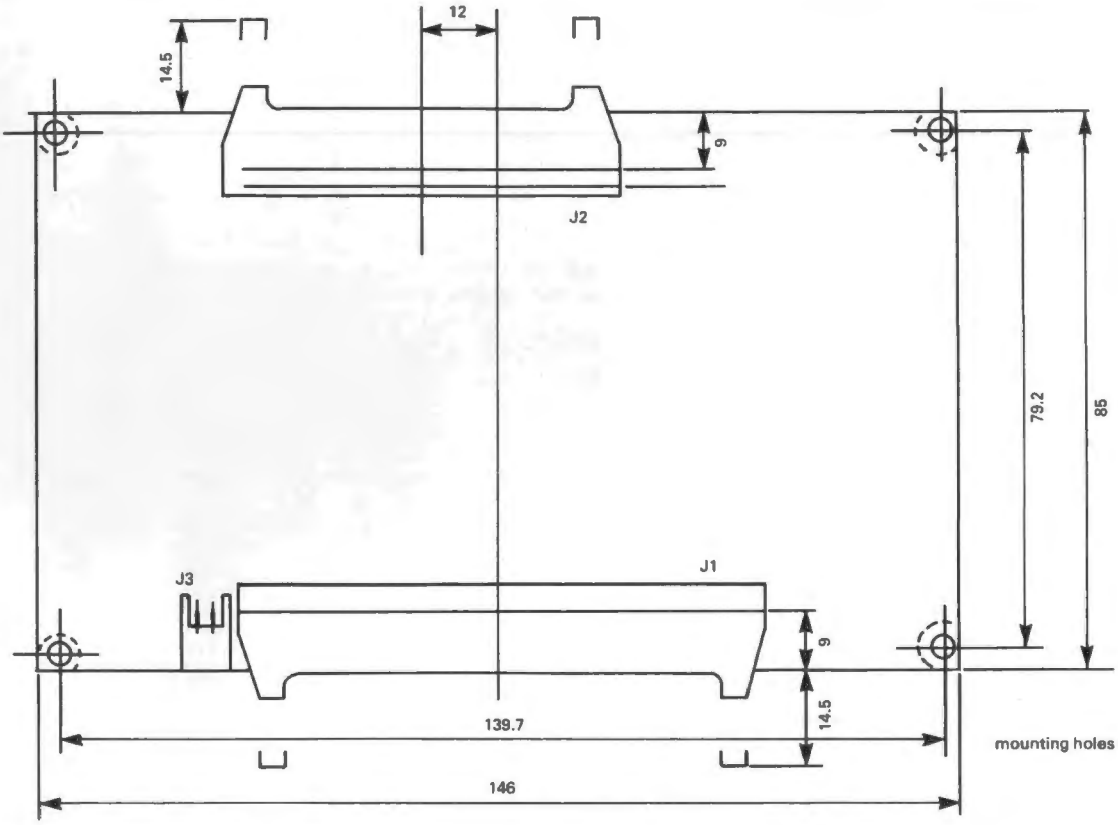


Figure 17 **External dimensions**



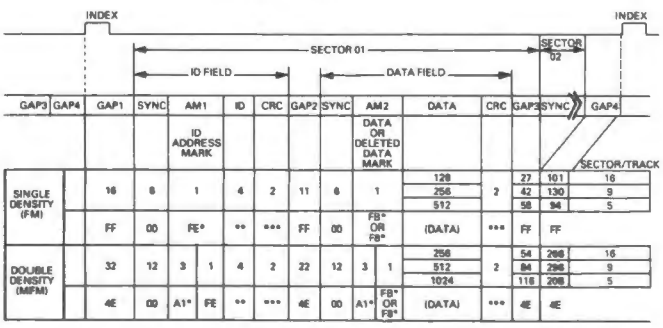
Specification

Encoding Method	MFM, FM
Maximum Number of Tracks	256
Track-to-Track Access Time	3, 6, 10 and 15msec
Settling Time	15msec
Head Load Time	35msec
Data Transfer Rate	
MFM	31.3k bytes/sec
FM	15.6k bytes/sec
Maximum Number of Drives	4
Drive Connection Method	Daisy chain
Double-Sided Type Drives	Connectable
Programming	Polling, interrupts, and DMA are all usable
Power Requirements	DC + 5V ±5%, less than 0.4A

Recording format

The disc recording format is IBM compatible. This is the most popular 5¼in floppy disc format.

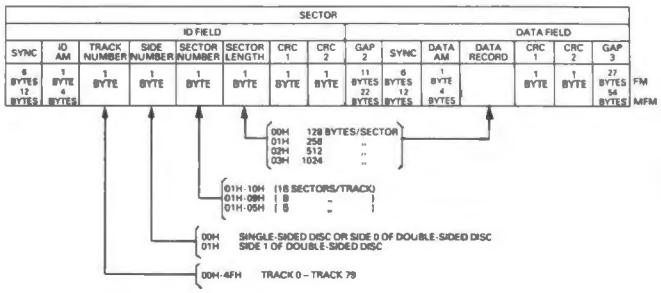
Table 4 **Recording format**



Notes: * Shows waiting for missing clock.
** Shows ID field.
*** The CRC polynomial used is $G(X) = X^0 + X^5 + X^{12} + X^{16}$

Sector Format

Table 5 **Sector format**



Six internal registers

The FC55 has six internal registers for inputting and outputting commands, statuses and data. The table below shows the functions of these registers:

Table 6 **Internal registers**

REGISTER SELECT			READ	WRITE
$\overline{RS2}$	$\overline{RS1}$	$\overline{RS0}$		
1	1	1	STATUS REGISER (STR)	COMMAND REGISTER (CR)
1	1	0	TRACK REGISTER (TR)	
1	0	1	SECTOR REGISTER (SCR)	
1	0	0	DATA REGISTER (DR)	
0	1	1		DEVICE REGISTER (DVR)

Commands

The FC55 has 10 basic commands. These are divided into several types according to the command code:

Table 7 **Type I, II and III commands**

TYPE	COMMAND	EFFECT	COMMAND CODE (HEX)	OPERATION KEY				
				SPECIFY TRACK	VERIFY	MULTI RECORD	DATA MARK 'FB'	DELETED DATAMARK 'F8'
TYPE I COMMANDS	RESTORE	MOVES HEAD TO DISC TRACK	03H	NO	NO	NO	NO	NO
			07H	NO	YES	NO	NO	NO
	SEEK	MOVES HEAD TO SPECIFIED TRACK	13H	NO	NO	NO	NO	NO
			17H	NO	YES	NO	NO	NO
	STEP	MOVE HEAD ONE TRACK IN EITHER DIRECTION	23H	NO	NO	NO	NO	NO
			27H	NO	YES	NO	NO	NO
			33H	YES	NO	NO	NO	NO
			37H	YES	YES	NO	NO	NO
	STEP IN	MOVE HEAD ONE TRACK TOWARDS CENTRE	43H	NO	NO	NO	NO	NO
			47H	NO	YES	NO	NO	NO
			53H	YES	NO	NO	NO	NO
			57H	YES	YES	NO	NO	NO
	STEP OUT	MOVE HEAD ONE TRACK TOWARDS OUTSIDE	63H	NO	NO	NO	NO	NO
			67H	NO	YES	NO	NO	NO
			73H	YES	NO	NO	NO	NO
			77H	YES	YES	NO	NO	NO
TYPE II COMMANDS	READ DATA	READS DATA FROM DISC	80H	NO	NO	NO	NO	NO
			90H	NO	NO	YES	NO	NO
	WRITE DATA	WRITES DATA TO DISC	A0H	NO	NO	NO	YES	NO
			A1H	NO	NO	NO	NO	YES
			B0H	NO	NO	YES	YES	NO
			B1H	NO	NO	YES	NO	YES
TYPE III COMMANDS	READ ADDRESS	READ ID FIELD (FIRST SECTOR) (ONLY)	C4H	NO	NO	NO	NO	NO
	WRITE TRACK	WRITE AN ENTIRE TRACK OF DATA	F4H	NO	NO	NO	NO	NO

Table 8 **Type IV commands**

TYPE	COMMAND	EFFECT	
TYPE IV COMMAND	FORCE INTERRUPT	CAUSES AN INTERRUPT	$1101I_3I_2I_1I_0$

(Type IV Commands)

I_1: INTERRUPT CONDITON FLAGS (BITS 0-3)	
$I_0 = 1$	INTERRUPT – DRIVE HAS BECOME READY
$I_1 = 1$	INTERRUPT – DRIVE HAS BECOME NOT READY
$I_2 = 1$	THIS INTERRUPT OCCURS AT EACH INDEX HOLE
$I_3 = 1$	SET ON EVERY INTERRUPT
$I_0 – I_3 = 0$	COMMAND TERMINATED WITHOUT INTERRUPTING

(Type IV Command Flags)

Statuses

All commands except for type IV commands set the status register to indicate the results of execution.

Table 9 **Status register bits**

STATUS REGISTER BIT	TYPE I	TYPE II		TYPE III			TYPE IV		MASTER RESET
	ALL COMMANDS	READ DATA	WRITE DATA	READ ADDRESS	READ TRACK	WRITE TRACK	COMMAND IN PROGRESS	NO COMMAND IN PROGRESS	
STR 7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	FOLLOWS TYPE 1 COMMAND
STR 6	WRITE PROTECT	0	WRITE PROTECT	0	0	WRITE PROTECT	STATUS OF COMMAND IN PROGRESS	WRITE PROTECT	
STR 5	HEAD LOADED	RECORD TYPE	0	0	0	0		HEAD LOADED	
STR 4	SEEK ERROR	RECORD NOT FOUND	RECORD NOT FOUND	RECORD NOT FOUND	0	0		0	
STR 3	CRC ERROR	CRC ERROR	CRC ERROR	CRC ERROR	0	0		0	
STR 2	TRACK 00	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA		TRACK 00	
STR 1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ		INDEX	
STR 0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY	0	0	

Table 10 **Status bits**

STATUS BIT	MEANING
NOT READY (STR 7)	NOT READY = 1: Spindle motor is stopped. NOT READY = 0: Spindle motor is running.
WRITE PROTECT (STR 6)	WRITE PROTECT = 1: Writing to the disc is forbidden. WRITE PROTECT = 0. Writing to the disc is permitted. (Depends on whether a Write-Protect tab is in place.)
HEAD LOADED (STR 5)	HEAD LOADED = 1: Head is in contact with the disc. HEAD LOADED = 0: Head is away from the disc.
SEEK ERROR (STR 4)	SEEK ERROR = 1: Verify Error on a verify command. SEEK ERROR = 0. No Verify Error. This error is reset on the next command.
CRC ERROR (STR 3)	CRC ERROR = 1: A CRC error has occurred. CRC ERROR = 0. No CRC error. This error is reset on the next command.
TRACK 00 (STR 2)	TRACK 00 = 1: The head is over Track 00. TRACK 00 = 0: The head is not over Track 00.
INDEX (STR 1)	INDEX = 1: An Index hole has been detected. INDEX = 0 No Index hole has been detected.
BUSY (STR 0)	BUSY = 1: Command in progress. BUSY = 0: No command in progress next command can be issued.
RECORD TYPE (STR 5)	On a read, displays type of data address mark. Inoperative on a read track command. Record type = 1: Deleted data mark detected. Record type = 0: Data mark detected. This status is reset on the next command.
RECORD NOT FOUND (STR 4)	RECORD NOT FOUND = 1: This specified track or sector was not found. RECORD NOT FOUND = 0: The specified track and sector were found.
LOST DATA (STR 2)	LOST DATA = 1: A DR read or write was not performed within the prescribed time. LOST DATA = 0: DR read or write was performed within the prescribed time.
DRQ (STR 1)	DRQ = 1: The DR was empty on a write or full on a read. This status is equivalent to the DRQ output signal.

Interface to CPU bus

Table 11 **Signal connector pin numbers**

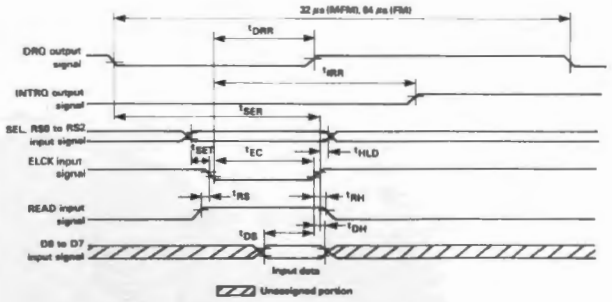
SIGNAL NAME	PIN No.	SIGNAL NAME	PIN No.
NC	1	0V	2
$\overline{RST}$	3	0V	4
$\overline{ECLK/WE}$	5	0V	6
$\overline{READ/RE}$	7	0V	8
D7	9	0V	10
D6	11	0V	12
D5	13	0V	14
D4	15	0V	16
D3	17	0V	18
D2	19	0V	20
D1	21	0V	22
D0	23	0V	24
$\overline{SEL}$	25	0V	26
$\overline{INTRQ}$	27	0V	28
$\overline{DRQ}$	29	0V	30
NC	31	0V	32
$\overline{RS\,2}$	33	0V	34
$\overline{RS\,1}$	35	0V	36
$\overline{RS\,0}$	37	0V	38
0V	39	0V	40
0V	41	0V	42
+ 5V	43	+ 5V	44
+ 5V	45	NC	46
NC	47	NC	48
NC	49	POLARISING KEY	50

NC: NOT CONNECTED

Write and read timing

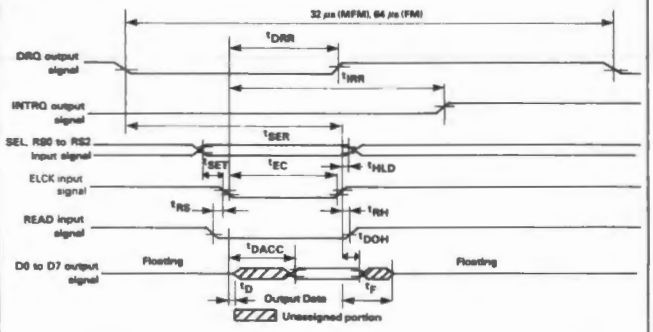
Figure 18 **Write timing with the select link 'CPU 68' ON.**

Note: At 10% and 90% points of the signal level. With SEL, RS0 to RS2, D0 to D7, at 50% point.



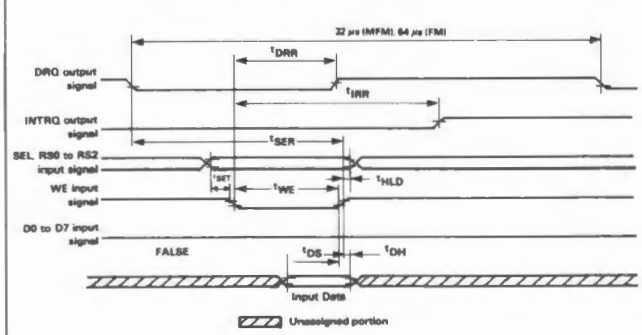
Item	Symbol	Standard			Unit	
		Min.	Typ.	Max.		
Service time	t_{SER}			23	μs	(MFM)
				47	μs	(FM)
Address setup time	t_{SET}	50			ns	
Address hold time	t_{HLD}	10			ns	
ECLK pulse width	t_{EO}	200			ns	
DRQ reset time	t_{DRR}			250	ns	
INTRQ reset time	t_{IRR}			1	μs	
Data setup time	t_{DS}	250			ns	
Data hold time	t_{DH}	20			ns	
READ setup	t_{RS}	20			ns	
READ hold time	t_{RH}	20			ns	

Figure 19 **Read timing with the select link 'CPU 68' ON.**



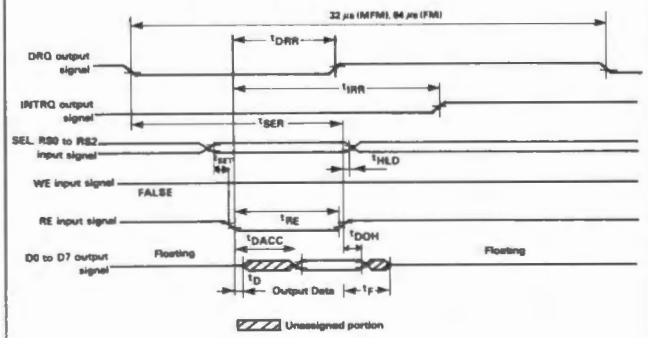
Item	Symbol	Standard			Unit	
		Min.	Typ.	Max.		
Service time	t_{SER}			27	μs	(MFM)
				55	μs	(FM)
Address setup time	t_{SET}	50			ns	
Address hold time	t_{HLD}	10			ns	
ECLK pulse width	t_{EO}	280			ns	
DRQ reset time	t_{DRR}			250	ns	
INTRQ reset time	t_{IRR}			1	μs	
Data access time	t_{DACC}			250	ns	
Data hold time	t_{DOH}	50		150	ns	
READ setup time	t_{RS}	20			ns	
READ hold time	t_{RH}	20			ns	
Data bus drive time	t_D	0			ns	
Data bus float time	t_P			300	ns	

Figure 20 **Write timing with the select link 'CPU 80' ON.**



Item	Symbol	Standard			Unit	
		Min.	Typ.	Max.		
Service time	t_{SER}			23	μs	(MFM)
				47	μs	(FM)
Address setup time	t_{SET}	50			ns	
Address hold time	t_{HLD}	10			ns	
WE pulse width	t_{WE}	200			ns	
DRQ reset time	t_{DRR}			250	ns	
INTRQ reset time	t_{IRR}			1	μs	
Data setup time	t_{DS}	250			ns	
Data hold time	t_{DH}	20			ns	

Figure 21 **Read timing with the select link 'CPU 80' ON.**



Item	Symbol	Standard			Unit	
		Min.	Typ.	Max.		
Service time	t_{SER}			27	μs	(MFM)
				55	μs	(FM)
Address setup time	t_{SET}	50			ns	
Address hold time	t_{HLD}	10			ns	
RE pulse width	t_{RE}	280			ns	
DRQ reset time	t_{DRR}			250	ns	
INTRQ reset time	t_{IRR}			1	μs	
Data access time	t_{DACC}			250	ns	
Data hold time	t_{DOH}	50		150	ns	
Data bus drive time	t_D	0			ns	
Data bus float time	t_P			300	ns	

RS data

Floppy disc drive alignment disc

The RS Alignment Disc can be used for 48/96 TPI drives with either single or double sided heads. It is physically compatible with industry standard 5.25in floppy discs.

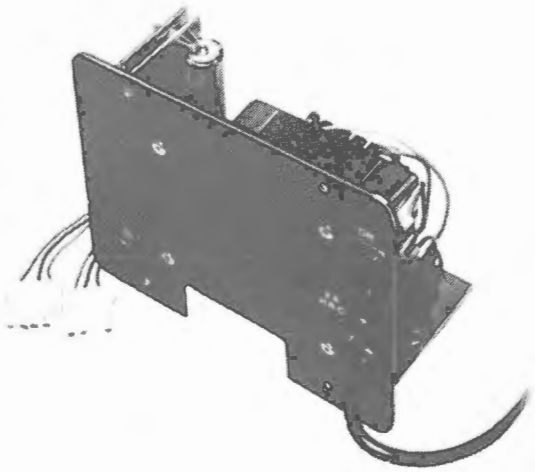
The following signals are available:

Trace Number		Signal	Check/Adjustment
48TPI	96TPI		
01	02	Index Burst	Index/Sector Photo sensor Timing
16	32	'Cats Eye' lobe pattern	Track alignment
34	68	Index burst	Radial tracking

For detailed instructions consult alignment disc instruction leaflet for the following:

1. Check and Adjustment of Track Radial Alignment.
2. Check and Adjustment of Index Data Burst Timing.
3. Check and Adjustment of Track 00 Sensor.
4. Check and Adjustment of Track 00 Stopper.

Disc drive power supply



The power supply, capable of powering two RS 5¼in floppy disc drives, has been designed specifically to fit into the rear of the RS disc drive case.

Input:	240Vac ±6% 50Hz
Output:	Two identical outputs of:
	+12Vdc ±5%, 0.9A peak
	+5Vdc ±5%, 0.6A peak
Fuse:	2A HRC (20mm)
Dimensions:	W. 150, H. 121, D. 65

Floppy disc drive case

The RS disc drive case has been designed to house up to two 5¼in disc drive units.

There is sufficient space within the case to accommodate one or two disc drives (a blanking plate is supplied for use when only one disc drive is fitted). A suitable power supply for the drives may be fitted inside the rear of the case, alternatively, the rear panel of the case may be replaced with the RS disc drive power supply for direct mains operation.

Case dimensions: L. 319, W. 155, H. 126.6.

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
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RS data

IP Ratings

The IP rating system provides a means of classifying the degrees of protection from dust, water and impact afforded by electrical equipment and enclosures. The system is recognised in most European countries and is set out in a number of British and European standards. These include BS5490:1977 (IEC529:1976) Classification of Degrees of Protection Provided by Enclosures, BS5420:1977 (IEC144:1963) Specification for Degrees of Protection of Enclosures of Switchgear and Control Gear for Voltages up to and Including 1000V a.c. and 1200V d.c.

Details of a third IP numeral are also shown. Whilst not specified by the British Standards Institute, this figure is used in corresponding international standards, to indicate degrees of resistances to impact.

FIRST NUMBER
Protection against solid objects

IP	TESTS
0	no protection
1	protected against solid objects up to 50mm, eg accidental touch by hands.
2	protected against solid objects up to 12mm, eg fingers.
3	protected against solid objects over 2.5mm (tools + wires).
4	protected against solid objects over 1mm (tools, wires + small wires).
5	protected against dust – limited ingress (no harmful deposit).
6	totally protected against dust.

SECOND NUMBER
Protection against liquids

IP	TESTS
0	no protection
1	protected against vertically falling drops of water (eg condensation).
2	protected against direct sprays of water up to 15° from the vertical.
3	protected against sprays to 60° from the vertical.
4	protected against water sprayed from all directions – limited ingress permitted.
5	protected against low pressure jets of water from all directions – limited ingress permitted.
6	protected against strong jets of water, eg for use on shipdecks – limited ingress permitted.
7	protected against the effects of immersion between 15cm and 1m.
8	protected against long periods of immersion under pressure.

THIRD NUMBER
Protection against mechanical impacts

IP	TESTS
0	no protection
1	impact 0,225 joule
2	impact 0,375 joule
3	impact 0,50 joule
5	impact 2,00 joule
7	impact 6,00 joule
9	impact 20,000 joule

RS data

Note: When an IP rating is included in the catalogue, certain points should be taken into consideration as to its interpretation:

1. Although an enclosure has a high IP rating, the equipment being used in conjunction with it may reduce this (eg through mounted components and methods of cable entry).
2. An IP rating may be quoted with regard to the maximum protection from the front of the enclosure (eg a pushbutton may afford protection through the actuator and by means of sealing around the mounting hole). This rating may not apply to the rear of the component.

The following products are available from RS with IP ratings. Please refer to current catalogue for full details.

ABS sealed boxes
Appliance connectors
Cam switch enclosures
Camsafe switch
Crimp BNC connection
DOL starters
DIN rail enclosures and mounting boxes
Diecast boxes
Distribution boards
Electrically operated bolt
Emergency lighting
Emergency stop buttons
Flush mounting enclosures
Fuseholders
General purpose wall mounting enclosures
Impulse counters
Industrial footswitch
Industrial key switches
Industrial latching switches
Industrial lever switches
Industrial microswitches
Industrial push button stations
Industrial start/stop switches
Industrial switch enclosures
Industrial wall mounting enclosures
Keypad switches
Light sensitive switches
Light switches
Local isolators
Manual motor starters
Moulded enclosures
Proximity switches
Panel switches
Pliable conduit
Programmable 7-day timeswitch
Rear mounting enclosures
Rechargeable handlamp
Rotary cam switches
Rotating mirror beacons
Sealed limit switches
Single path photo-relay systems
Sub-miniature limit switches
Surface mounting enclosures
Switch fuses
Universal guard switch
Wall mounting RCCB/MCB enclosures
Wall mounting RCCB/MCB socket outlet
Wall mounting enclosures and housings
Weatherproof thermostats.

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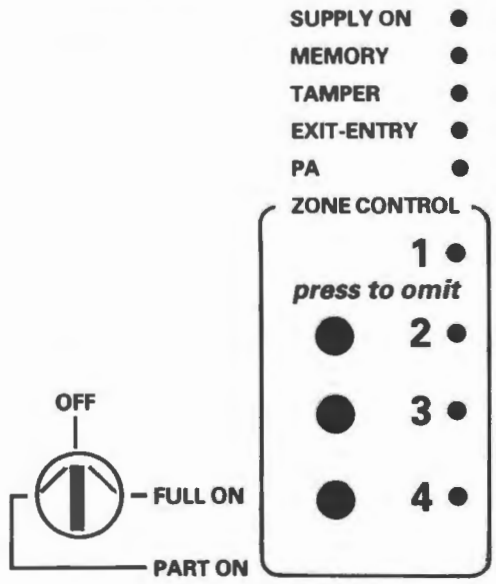
RS data

Four zone alarm control panel

The RS four zone control panel meets the requirements of BS4737 pts 1 and 2 ('Intruder alarm systems in buildings') and can be wired to conform with any Police or NSCIA Code of Practice. The four zone (three switchable) control panel facilities incorporate a personal attack circuit, separate dual entry/exit circuit with independently adjustable exit and entry timers, adjustable bell cut-off timers, two alarm output circuits with the facility to drive a flashing beacon continuously, and full alarm status indication on the front panel.

The control panel is totally self-contained operating from a 240V ac supply and has the facility to charge a 12V sealed lead acid back-up battery, up to 5.7Ah capacity, RS591-944. The panel is fitted with an anti-tamper switch and security key switch supplied with two keys: additional keys are not available for security reasons.

Figure 1 **Front panel**



Features

- Totally self-contained
- Four zone, three switchable
- 24 hour anti-tamper loop
- Personal attack circuit
- Separate adjustable dual exit/entry timers
- Full status indication on front panel
- Dual alarm output
- British Telecom approved
- Complies with BS5839 Pt. 1 and 2

Supply On
The 'Supply On' indicator illuminates only when the mains voltage is present.

Memory
The 'Memory' indicator illuminates and latches whenever there has been an alarm.

Tamper
The 'Tamper' indicator illuminates and latches whenever the tamper circuit is in Fault/Alarm condition.

P.A. (Personal Attack)
The P.A. indicator illuminates (latching) whenever the P.A. is in Fault/Alarm condition.

Exit/Entry
The Exit/Entry indicator illuminates whenever the Entry Circuit is operated, and latches in Alarm condition.

Zone 1
The Zone 1 indicator illuminates whenever Zone 1 is in Fault/Alarm condition.

Zone 2-4

Zone 2-4 indicators illuminate whenever there is a Fault/Alarm condition as in Zone 1. For any Zone that has been switched off by using the push switches, the indicator for that Zone will flash for the duration of the exit time.

Guide to installation

Draw a plan of the building to be protected and decide on the location of the control panel, detection devices and bell housing.

The control panel should be sited as near as practicable to the usual point of entry and, if possible, it should not be conspicuous.

Detection devices will vary depending on the layout of the building. However, the most likely point of unauthorised entry (usually at the back of buildings or places of easy access where an intruder can 'work' without being noticed) should be particularly well protected as should areas containing articles of high value. Ideally design your system to detect the intruder as early as possible, on entry rather than after entry. It is also worthwhile to protect internal doors as intruders nearly always move around as soon as they have gained entry. Internal protection devices are especially useful if the layout of the building makes it difficult to protect the exterior thoroughly. All the detection devices on your system can function in any circuit. All zones are operative in the 'part on' and 'full on' key position (exit/entry is not operative in the 'part on' position).

Decide in which circuit you want each detector to work, on setting the control panel there is no delay on any circuit except for the 'exit/entry' circuit and therefore the 'exit/entry' circuit should include all detectors that could be used during authorised exit/entry even if only very occasionally. Zones 2, 3 and 4 can be programmed out in the 'part on' key position, or manually switched out in any key position and, as for exit/entry, care should be taken when grouping detectors between switchable zones.

The main bell should be mounted outside, where it can be seen and heard. Normally it should be mounted where it is not accessible without a ladder. Also it is good practice to run the cable to the bell straight through the wall at the back of the bell housing so that the cable is not exposed. To comply with BS4737 the cabling to the main bell should be monitored for open or short circuit, this can be achieved by using the RS Self Activating Bell Module 301-577.

The total output current capacity of the RS control panel is 1amp therefore it is essential that the total load drawn by the complete system, in full alarm condition does not exceed the rating of the power supply. Ideally it should not run at more than 80% of maximum i.e. 800mA.

Many false alarms are caused by poor joints wrapped in insulation tape. To satisfy the British Standard a tamperproof junction box or a soldered joint (sleeved with heat shrink sleeving) should be used when making connections to the master detection circuit.

If you use ultrasonics, passive infra-red or similar devices refer to the manufacturer's instructions for wiring. However in almost all cases, a 12V Supply to the unit will be required (±12V terminals are available at the zone output). In this case, in addition to two supply wires a further 4 wires (2 tamper wires and 2 which form the alarm loop) are required. Therefore a six core cable should be used.

Functional description

Figure 2 **PCB layout**

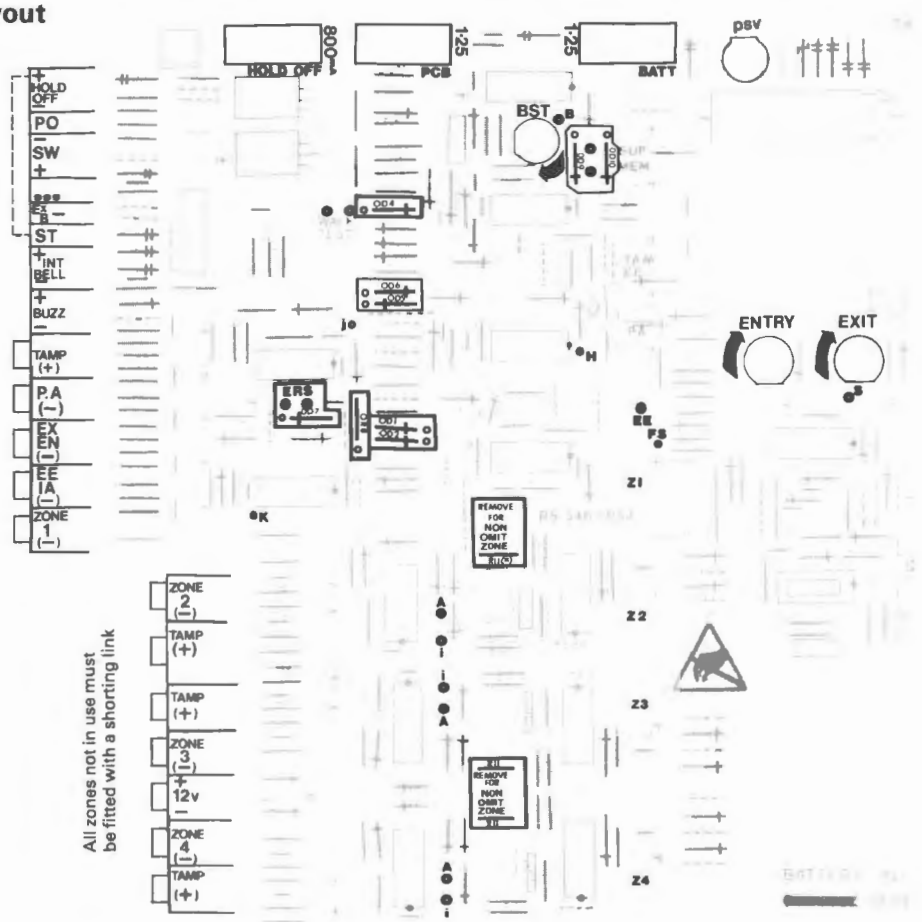


Table 1 **Main terminal block supply output terminals**

Terminals	Voltage Output			Max current	Comment
	Key 'off'	'Part on'	'Full on'		
Hold Off + –	+12V 0V	+12V 0V	+12V 0V	800mA	Fused 800mA
PO	+12V	0V	+12V	25mA	
SW – +	+12V 0V	0V +12V	0V +12V	250mA 50mA	
999	0V	0V	+12V	5mA	Alarm cond. only pulsed
EXB–	+12V	0V	0V	1A	Alarm cond.
Int Bell + –	+12V +12V	+12V 0V	+12V 0V	1A	Alarm cond. only
12V+ –	+12V 0V	+12V 0V	+12V 0V	200mA	

Tamper circuit

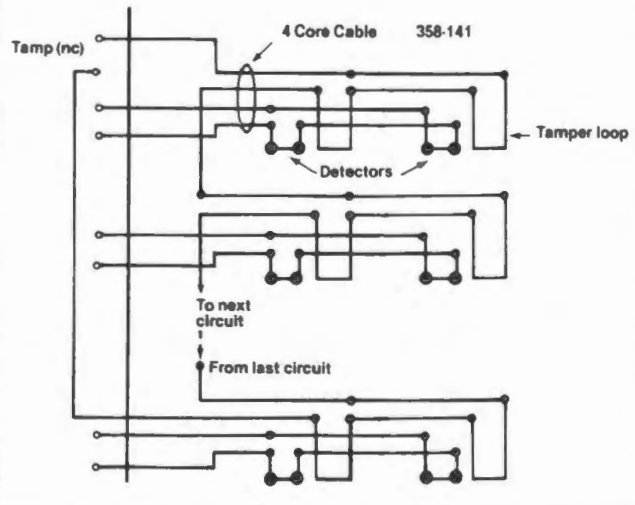
This loop is the 'monitor' circuit to be run with all the other detector circuits. The Tamper Circuit is of positive (+ve) polarity.

Breaking of the Tamper loop results in an 'alarm' condition. This loop is always 'active' irrespective of the key position, but the alarm condition varies according to the key position, i.e.

'Part On' Bell alarm and buzzer sounding
'Full on' Bell alarm, buzzer sounding and '999' output
'Off' Buzzer only

The alarm is silenced by turning the key switch to 'on' and 'off' again. The circuit LED will remain illuminated until the fault is cleared. All wiring loops going into any one detection circuit must be wired in series as in Figure 3. Separate tamper circuits are supplied for zones 2, 3 and 4.

Figure 3 **Tamper circuit**

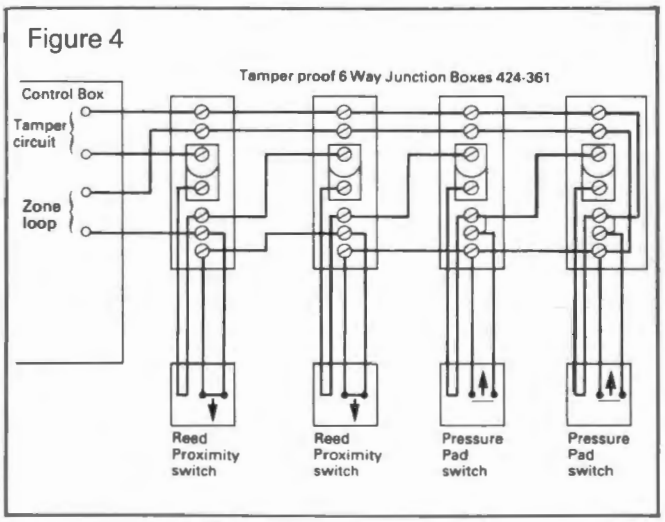


If the trip is via a zone tamper circuit the appropriate zone LED will light in addition.

Zone 1

The protection of this zone is achieved through two loops; the tamper loop, and a switch zone loop. This four wire zone may be used in conjunction with detection devices such as pressure pad switches, reed proximity switches, etc., in any combination see Figure 4 for an example.

Figure 4



Note how in the example shown above the tamper circuit is continuous and the normally closed reed switch is connected in the switch loop. The normally open pressure mat switch is connected between the tamper loop and the switch loop zone 1.

Full alarm condition will result:

1. When an O/C appears in the tamper loop (bell and buzzer sounding).
2. When an O/C appears in the circuit loop (bell only sounding).
3. When an S/C appears between zone 1 and tamper (bell only sounding).

Zones 2-4

Affords the same protection as zone 1 and the same types of detection devices may be used.

Full alarm condition will result:

1. When an O/C appears in the tamper loop (bell and buzzer sounding).
2. When an O/C appears in the circuit loop (bell only sounding).
3. When an S/C appears between the zone and tamper terminals (bell only sounding).

Zone omit (not on zone 1): Any zone may be omitted by momentarily depressing the zone push button during exit time. The zone LED will flash for the remainder of exit time to confirm the omission.

Following a full alarm condition, when the panel is

turned off, the LEDs of zones which had been omitted at the time of the alarm will again flash, until the panel is re-set.

Alternatively, zones may be pre-programmed to be automatically omitted in 'Part Guard' by connecting pin 'I' on each of the appropriate zones, to the 'PO' terminal (see Figure 2).

The tamper circuit of an omitted zone will remain live, and will give a *non-latching* indication on the zone in addition to the main Tamper indication.

P.A. (Personal attack)

The protection of this zone differs from all the others in as much as breaking of the P.A. circuit loop will activate the alarm (bells and 999 output) irrespective of the control key position, (even in the 'OFF' position). This circuit is not controlled by the 'Bell Stop Timer'. The input latch may be cleared by turning the control on and off again AFTER the circuit has been cleared.

Exit-Entry circuitry

The exit and entry delay times are separately adjustable (between 0-2 minutes, approx.) using the variable controls provided on the printed circuit board (turn clockwise to increase time setting). Two circuits are provided. 'EXEN' (Exit/Entry) and 'EEIA' (Exit/Entry instant alarm). On Exit, both function in the same delayed mode, and will automatically extend exit time indefinitely as long as either circuit is open. The system will automatically set when the circuit is closed, or when the pre-set time has expired; whichever is the longer. Therefore it is possible to use either circuit for the exit route, but only the 'EXEN' circuit for entry.

On entry:

(a) If 'EXEN' circuit is broken FIRST (i.e. via normal authorised entry route), the pre-set entry time will be started, and at the expiry of that time, a full alarm condition will be generated, unless the panel has previously been switched off. Subsequent tripping of the EEIA circuit will have no effect.

b) If 'EEIA' circuit is broken FIRST (i.e. by an attempt to reach the entry route via an unauthorised point), a full alarm condition will be generated immediately.

Shunt lock operation may be used by shunting a +ve voltage onto PIN 'S'. A normally open 'push to set' button may be used to shunt a –ve voltage onto pin 'S' via a 1k resistor.

The exit buzzer may be disabled in 'Part Guard' key position by connecting Pin 'S' to the 'PO' terminal via a 1N4148 diode (anode towards Pin 'S').

All detection circuits

If any N/C detection circuit is not to be used the short link should be left across the terminals.

Detection circuit faults

Detection circuit faults are individually indicated by LEDs. In the 'off' key position, these LEDs (except for 'EXIT-ENTRY') will indicate and latch on.

At Switch 'On', these indications will clear for all circuits which are clear. Should any indicators remain lit, the keyswitch should immediately be turned off. The detection circuits will not set unless all other circuits are clear.

Walk test

Walk test of the system is possible by temporarily shorting together the two pins 'WT'. This will connect the system buzzer to give an audible indication whenever any circuit (except Exit/Entry) is in fault condition. A latching visual indication will be provided by the LEDs to confirm the results of the test. The link between 'WT' pins should, of course, NOT be left in place whilst the panel is in normal use.

Stabilized supply

13.5V d.c. (Nominal) is available at the terminals marked ±12V for auxiliary equipment. The total system requirement should not exceed 1 amp. It is important that if a dryfit battery is used an open circuit voltage or 13.65V d.c. should not be exceeded. When adjustment is required the voltage should be set by variable resistor 'psv'.

Rechargeable back-up battery

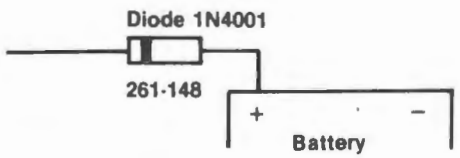
Should be connected to the flying leads provided Red +ve Black –ve. The back-up battery provides power for all circuits including the Auxiliary Output in the event of mains failure. The size of battery should be chosen to have sufficient capacity for 8 hours normal operation without external power.

Current drain of pcb: Quiescent 10mA.
Alarm condition 55mA

Non-rechargeable back-up battery

A 12V non-rechargeable back-up battery may be used by connecting a 1A diode in series with the positive lead to the battery (see Figure 5). The initial nominal capacity of the primary battery should be sufficient for 36 hours normal operation including 2 hours operation in the alarm condition without external power.

Figure 5



Fuses

Mains	Providing power for the transformer	1A
Bell	Providing power for the bell	800mA
Battery	Providing power for the battery	1.25A
Pcb	Provides power for auxiliary outputs	1.25A

Low voltage warning

If the control panel voltage falls below approximately 9V, the tamper circuit will be activated (latching).

Sounder output

There are two output circuits for the bells/sounders, 'EXB' and 'INT BELL'. The 'EXB' (external bell) is for use with a self-activating bell module. (See S.A.B. section) and is used with the 'HOLD-OFF +ve terminal.

999 Output

Voltage start output (+ve drive). Normal output provides pulse of approximately 2 seconds to initiate drive of police call unit. The output will then be locked out awaiting reset **except** for a personal attack alarm. This provides a continuous output whilst the panel is in alarm condition and is live in **all** key positions, even whilst panel is locked out awaiting reset following a previous trip. As supplied, the 999 output is isolated when the panel is set in 'Part Guard' (except for PA).

Memory LED

The memory LED provides an indication that the 999 output has been triggered, and that the panel requires resetting before it can be used again (except for PA).

British Telecommunications approval

Quote approval No. NS/2550/3/D/022034.

Alarm output duration

Adjusting the variable resistor (BST) determines the alarm duration time, once this time has expired the alarm output will shut down and the control panel can only be reset by the key. The time is adjustable from 0 to 45 minutes. One-third adjustment is approximately 20 minutes. Note: visual indication on the front panel remains.

To simplify setting up, pin 'B' is provided which may be used as follow:

Apply voltmeter –ve probe to supply negative and +ve probe to Pin B, when an alarm is initiated, a series of voltage pulses will be observed on the meter. The length of these pulses (in seconds) approximately equals one half of the time (in minutes) that the bells will ring.

The BST can be isolated from the internal bell circuit by removing option diode 'OD9'. This feature will enable the internal bell circuit to be used as a continuous output for xenon beacons etc.

Reset

As supplied the panel is set for engineer reset following a full alarm trip. The 'Memory' LED will light and remain so until pins ERS are shorted together. For customer re-set on non-police call system, remove option diode OD7, and reset will take place when the keyswitch is turned on.

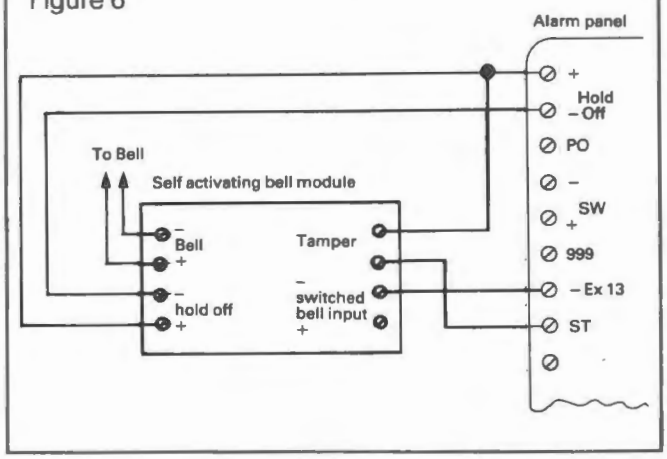
To convert to auto-reset

(Non-police call systems only.) Remove OD7 and OR8 and join pins AR together. After the preset bell cut off time, the entire system will reset for continued security **unless** any of the detection circuits are left in fault condition. Every circuit tripped will indicate, not merely the first to alarm.

Self activating bell (SAB)

When using the RS Self Activating bell module it should be securely fixed to the interior of the bell box and wired in accordance with Figure 6. The control panel has been designed so that only a 4 core cable is required.

Figure 6



Ultrasonic and passive infra-red detectors

Ultrasonic and passive infra-red detectors are extremely reliable units that operate by safe and well proven techniques. In many cases, especially where there are large doors or windows which can be difficult to protect in other ways, they offer a far greater degree of security than would otherwise be possible and can eliminate a lot of unnecessary wiring.

However the following points should be borne in mind:

a) Whenever you are using volumetric devices ensure the power supply is regulated.

b) When using a latching detector a switched positive or negative is available from the printed circuit board of the control panel. See Figure 2.

c) Remember that ultrasonics are most sensitive to an object moving towards them while passive infra-reds are most sensitive to objects crossing the beam tangentially. Actual range will depend on the unit you are using (see specifications with the unit) but typically a passive infra-red device has an angle of 90° while an ultrasonic has an angle of 120°.

d) Certain types of environment are hostile to ultrasonics. These include any powerful air currents (from ducted air central heating, fans etc.); powerful draughts (strong enough to make curtains sway for example); telephone bells within the range of the sonic; open fires; pets; letters coming through a letter-box etc.

Where possible mount ultrasonics so that none of these are present within the range, or at least turn down the sensitivity/environmental control, following closely the instructions supplied with the unit. (RS data sheet 5257.)

e) When using passive infra-reds bear in mind they should not be subjected to bright sunlight or rapid changes in temperatures. Also the ray should not be directed at an open fire.

Function options

Exit/Entry: To have 'EXEN' circuit functional in both key on positions, remove OD1. To have 'EEIA' circuit functional in both key on positions, remove OD2.

Alarm output: To have the '999' output function in both key on positions, remove OD4. To have a silent personal attack (police call systems only) remove OD5 and OD6. To have internal bell latched on after BST operation remove 0D9. To isolate BST remove OD9 and OD10.

Zones: To inhibit the omit switch remove Resistor R11 on the required zone.

Option and output pins available

A Logic (High) output for transmission of fault on switched zones.

AR Two pins to be linked together in auto-reset mode.

B Logic output for monitoring BST timing.

EE Logic (High) output for indication of fault on access circuits.

ERS Two pins to short together as engineer reset of memory.

FST Logic output changing polarity to that shown at end of exit time.
This is used to supply the latching terminal of a space detector when on the 'Exit/Entry' circuit.

H Logic (High) output for transmission of fault on Tamper circuit.

I Inhibit point on all switchable zones, connect to PO terminal for automatic isolation of zone in 'Part Guard'.

J Logic (High) output for transmission of fault on PA circuit.

K Logic (High) output for transmission of fault on Zone 1.

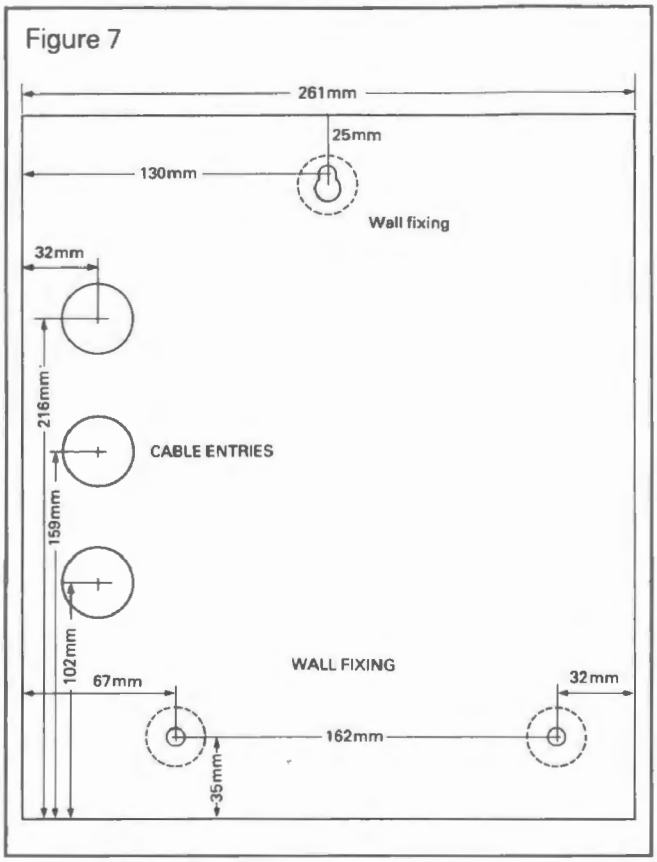
S Shunt connection.

WT Two pins to be temporarily shorted together for audible system walk test.
The output pins are suitable for connection to Digital Communicator for transmission of detail circuit information.

Mounting details

The control box should be mounted within the building to be protected (see Figure 7). It is recommended that the control box is mounted on an internal wall close to the point of entry, but not visible from the outside of the building.

Figure 7



Testing and maintenance

A programme of routine testing is described in BS4737 Part 1 Section 1.2, and this should be strictly adhered to. The minimum testing and maintenance required is as follows:

Every 12 months or 6 months if primary batteries are used:

1. Check the installation, location and siting of all equipment and devices against the record.
2. Check the satisfactory operation of all detection devices, including deliberately-operated devices.
3. Inspect all flexible connections against the relevant requirements.
4. Check that the normal and stand-by power supplies are functioning and appear to be in order.
5. Check the control equipment and service it in accordance with the alarm company's procedure.
6. Check the satisfactory operation of every audible alarm and warning device.
7. Check that the intruder alarm system is fully operational.

Fault identification/repair service

The electronics of this product have been carefully designed to be contained on a single printed circuit board. If you suspect a fault with the alarm control panel then it should only be necessary to return the PCB assembly to RS for repair/exchange (see the latest RS catalogue for details). Before returning the PCB assembly it is advisable to test the control panel in isolation. This is best done by removing the field wiring and replacing it with wire links to all the detector circuits (see Figure 2). Should it prove to be functioning correctly then each field circuit can be tested by replacing them in succession.

Should the PCB assembly need returning it is easily removed as follows:

a) Isolate mains supply.
b) Remove the mains fuse within the control panel.
c) Disconnect the battery.
d) Remove all field wiring from the terminal blocks.
e) Remove the transformer secondary from the terminal block.
f) Unplug the key switch.
g) Remove the six screws securing the PCB assembly.

The PCB assembly may now be removed and packed carefully for returning to the RS repair department together with the 'Repair/Exchange' form.

Associated security products

It is recommended that the RS alarm control panel is used in conjunction with the products specifically designed for security applications. This data sheet has been written assuming RS security products have been used throughout. A list of suitable security products is given below.

4-core signal cable	358-141
6-core signal cable	359-914
Tamper proof 6 way terminal block	424-361
Flexible jumper loop	424-377
Pressure pad switch	317-140
Flush mounting reed proximity switch	333-158
Flush mounting reed proximity switch	337-396
Surface mounting reed proximity switch	333-192
Surface mounting reed proximity switch	335-536
Roller shutter reed proximity switch	333-170
Window foil	609-994
Window foil make off block	489-330
Surface pass key switch	533-164
Pass key switch	335-952
Security key switch	334-864
Low current AWD	248-404
High output low current AWD	249-924
12-24V dc alarm bell	249-637
Bell enclosure	249-895
Multiple tone siren	249-570
Xenon beacon	565-456
Passive infra-red detector	301-123
Ultrasonic intruder detector	302-479
Rechargeable dryfit battery	591-944
Two tone buzzer	249-429
Self activating bell module	301-577

5437

RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

Video monitors

Stock number 300-108 to 136

A range of 14in (diagonal screen measurement) metal cased monitors suitable for industrial, business and educational use. They offer excellent performance, precise definition and high reliability.

The following versions are available:

Stock No.

300-108 Standard resolution; RGB (TTL) input.

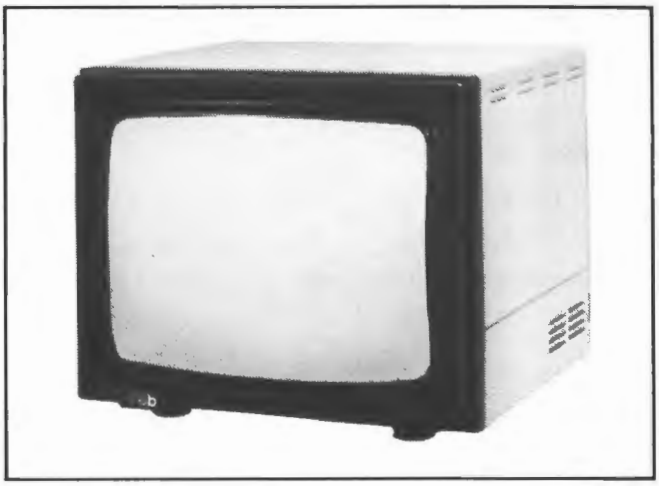
300-114 Standard resolution; RGB (TTL), PAL encoded composite video and audio inputs.

300-120 Medium resolution; RGB (TTL) input.

300-136 High resolution; RGB (TTL) input.

Features

- Fully isolated switch mode power supply giving very high raster stability.
- Low power consumption (typically 65W).
- High contrast self converging precision in-line tube giving excellent purity and colour convergence.
- Rugged metal cabinet.
- Choice of interfaces.
- Wide bandwidth video stages.
- Automatic de-gaussing at switch-on.
- Well proven PCBs for maximum reliability.



Technical specification

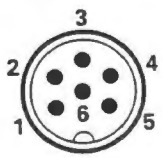
Stock number	**300-108**	**300-114**	**300-120**	**300-136**
Type	**Standard resolution 1**	**Standard resolution 2**	**Medium resolution**	**High Resolution**
Model	1431/MS4	1431AP/MS4	1451/MS4	1441/MS4
System	625 lines, 50 fields interlaced or 624/626 lines 50 fields non-interlaced			
Supply	180-265 Vac, 48-64Hz			
Time base	Nominal 15.625kHz. Pull-in range ± 500Hz. Lock-in range ± 700Hz.			
Positional error	± 2%			
Convergence error (max)	0.3mm within 90mm of screen centre, 1.6mm within 14mm of screen edge.		0.3mm within 90mm of screen centre. 1.2mm within 14mm of screen edge.	0.3mm within 90mm of screen centre. 0.8mm within 15mm of screen edge.
E.H.T.	Approximately 24kV at 500μA beam current			
Video bandwidth	18MHz			
Resolution (625 lines)	452 (H) x 585 (V) pixels		653(H) x 585(V) pixels	895(H) x 585(V) pixels

Stock number	300-108	300-114	300-120	300-136
Type	**Standard resolution 1**	**Standard resolution 2**	**Medium resolution**	**High resolution**
C.R.T.	Rectangular 335.4mm (screen diagonal) 90° diagonal deflection. Automatic degaussing at switch on. Precision-in-line gun. 0.64mm dot pitch. High focus voltage. Stripe phosphor.		Rectangular 335mm (screen diagonal) 90° diagonal deflection. Automatic degaussing at switch on. Precision-in-line gun. 0.43mm dot pitch. High focus voltage.	Rectangular 333mm (screen diagonal) 90° diagonal deflection. Automatic degaussing at switch on. Precision-in-line gun. 0.31mm dot pitch. High focus voltage. Black matrix screen with pigmented phosphors.
Inputs	R.G.B. (TTL level) R.G.B. (0-4V, 1500Ω – link selectable)	R.G.B. (TTL level); PAL encoded composite video; Audio.	R.G.B. (TTL level) R.G.B. (0-4V, 1500Ω – link selectable)	R.G.B. (TTL level) R.G.B. (0-4V, 1500Ω – link selectable)
Ambient operating temperature range	0 to + 40°C			
Power consumption	65W (typ.)			
Weight	7.6kg			8.7kg
Phosphor colour	P22: red, green, blue			
Phosphor persistence measured for 100% to 10% of brightness	Medium – short (1.2ms red, 0.3ms green, 0.25ms blue)			
Audio input	—	200mV rms signal into 47kΩ impedance, 4" single cone speaker 5W audio amplifier.	—	—
Composite video input	—	1V peak to peak signal input 75Ω impedance	—	—
M.T.B.F.	20,000 hours			

Inputs

RGB (TTL level) input for all monitors
This input can be used to connect to the RGB (TTL) outputs of various computers. The input uses a 6-pin DIN socket:

Figure 1 **RGB socket, monitor rear view**



1. Red
2. Green
3. Blue
4. Sync A
5. Ground
6. Sync B

The black lead supplied, terminated in a 6-pin DIN plug at each end is suitable for connecting to the BBC microcomputer. For other applications refer to the current RS catalogue for suitable connectors. When using this input with stock number 300-114 ensure the PAL/TTL switch is in the TTL position.

The Red, Green and Blue inputs on pins 1, 2 and 3 respectively (Figure 1) are set up to take standard **positive-going** signals. For negative-going signals refer to note on inverse video in Appendix A.

The Sync A input on pin 4 is set up to take a standard **negative-going, composite** horizontal (line) and vertical (field) synchronisation signal, provided pin 6 is either disconnected or connected to +5V (ie. not grounded). Alternatively the monitor will also accept **separate negative-going** line (pin 4, Sync A) and field (pin 6, Sync B) sync inputs. The timing is broadcast frequency compatible.

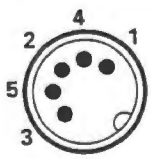
For non-standard sync inputs refer to note on sync options in Appendix A.

RGB (linear, 0 to 4V, 1500 ohm) input conversion (Stock nos 300-108, 300-120, 300-136)
Three links on the main pcb need to be moved. Refer to Appendix A, item 3.

PAL composite video input (Stock no. 300-114 only)
The main PAL input is via a BNC socket, which should be used for connecting to VCRs, video disc players etc. The BNC to BNC lead supplied with the monitor is for this purpose. Ensure the PAL/TTL switch is in the PAL position.

Audio input (Stock no. 300-114 only)
This can be used for connecting to PAL computers, VCRs and other video equipment. The audio input is via a 5-way 180° DIN socket:

Figure 2 **Audio socket, monitor rear view**



1. N.C.
2. Ground
3. Audio input
4. PAL input
5. N.C.

N.C. = No connection

For suitable connectors refer to the current RS catalogue.

Controls

All RS colour monitors are extensively soak-tested before despatch, and should require no setting-up of operator controls. However to take account of different or changing ambient conditions, user controls are found on the back of the monitor.

Depending on the model of colour display, the type and position of each control may vary.

1. On-off switch

A. A rocker switch, when switched ON, a neon will be illuminated in the switch or on the front panel.

B. A push-pull switch, extended position-ON, recessed position – OFF.

C. A rotary switch, clockwise-ON, anti-clockwise – OFF.

2. Contrast/Brilliance control

A rotary control, clockwise – increase, anti-clockwise – decrease.

3. Brightness control (when fitted)

A rotary control, clockwise – increase, anti-clockwise – decrease.

4. Volume control (when fitted)

A rotary control, clockwise – increase, anti-clockwise – decrease.

5. Colour saturation control (when fitted)

A rotary control, clockwise – increase, anti-clockwise – decrease.

Operating safety

WARNING: This monitor must be earthed. The monitor is supplied with a moulded-on 3A square-pin mains plug, meeting BS.1363A.

The wires in the mains lead are coloured in accordance with the following code:

Green and Yellow:	Earth
Blue:	Neutral
Brown:	Live

For alternative plugs, proceed as follows:
The wire which is coloured green and yellow must be connected to the terminal in the plug which is marked by the letter E or by the safety earth symbol ⏚ or coloured green or green and yellow. The wire which is coloured blue must be connected to the terminal which is marked with the letter N or coloured black. The wire which is coloured brown must be connected to the terminal which is marked with the letter L or coloured red.

If a 13A plug is used, fit a 3A fuse. For any other plug or connector protect with a 3A fuse or fuse wire on a distribution board.

If any doubt exists about the practical implications of the above precautions, or if the above does not fully cover your application, please contact RS Components Limited for advice.

Ventilation

The monitor should be used in conditions of adequate ventilation, with a clear air flow and with an operating ambient temperature range of 0°C to +40°C.

Under no circumstances should the access panel be removed. This could be dangerous and will invalidate the guarantee.

Computer compatibility

All four monitors are compatible with the BBC Micro, Acorn Electron, Oric 1/Atmos, RML 480Z and the Sharp. All these computers have an RGB (TTL level) output. Other computers with this output are also compatible.

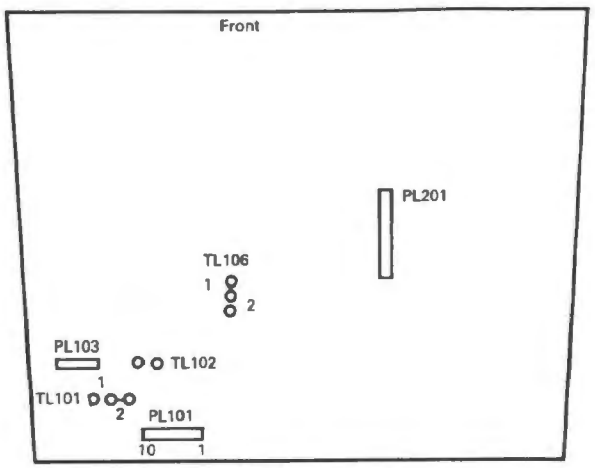
Stock No. 300-114 has (in addition) a PAL encoded composite video input, which makes it also compatible with the Atari, Vic 20, Commodore 64, Dragon 32/64, Tandy and any other computer with a 1V, 75ohm, PAL encoded composite video output. Stock No. 300-114 is also suitable for use with video recorders for television reception by using the video and audio inputs.

Appendix A

This appendix contains information to enable modification of standard RS monitors for non-standard applications. Modifications should only be carried out by suitably qualified service personnel. The monitor must be disconnected from the mains before removing the back panel and care should be taken to avoid dangerous discharge of electricity stored in transformers and capacitors. If modifications are not carried out with care and in accordance with these instructions they may invalidate the warranty and the standard repair charge will not apply.

1. Inverse video (all models, RGB (TTL) input)
Negative-going Red, Green and Blue (TTL level) input signals (pins 1, 2, 3 of DIN socket, Figure 1) can be accommodated by either
a) moving link TL101 on main printed circuit board to position 1.
b) removing TL101 and feeding a positive TTL level in to pin 9 of PL101.

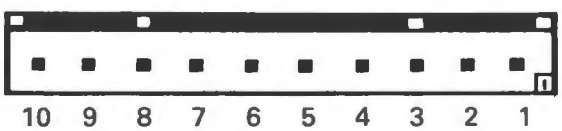
Figure 3 **Main printed circuit board. Link layout**



2. Synchronisation input options

Sync options		DIN socket (fig. 1)	PL101 (figs. 3 and 4)	Link position	Notes
Composite line and field	negative going	pin 4	pin 7	TL102 not fitted TL106 in position 1	Monitor supplied suitable for this configuration. Pin 6, DIN socket must not be grounded.
	positive going	pin 4	pin 7	TL102 fitted TL106 in position 1	
Separate line and field	negative line negative field	pin 4 pin 6	pin 7 pin 5	TL102 not fitted TL106 in position 1	Monitor supplied suitable for this configuration
	positive line positive field	pin 4 pin 6	pin 7 pin 3	TL102 fitted TL106 in position 2	Need to move lead and crimped connector from pin 5 to pin 3 in PL101
	negative line positive field	pin 4 pin 6	pin 7 pin 3	TL102 not fitted TL106 in position 1	Need to move lead and crimped connector from pin 5 to pin 3 in PL101

Figure 4 **Signal input connections for PL101 on main pcb**

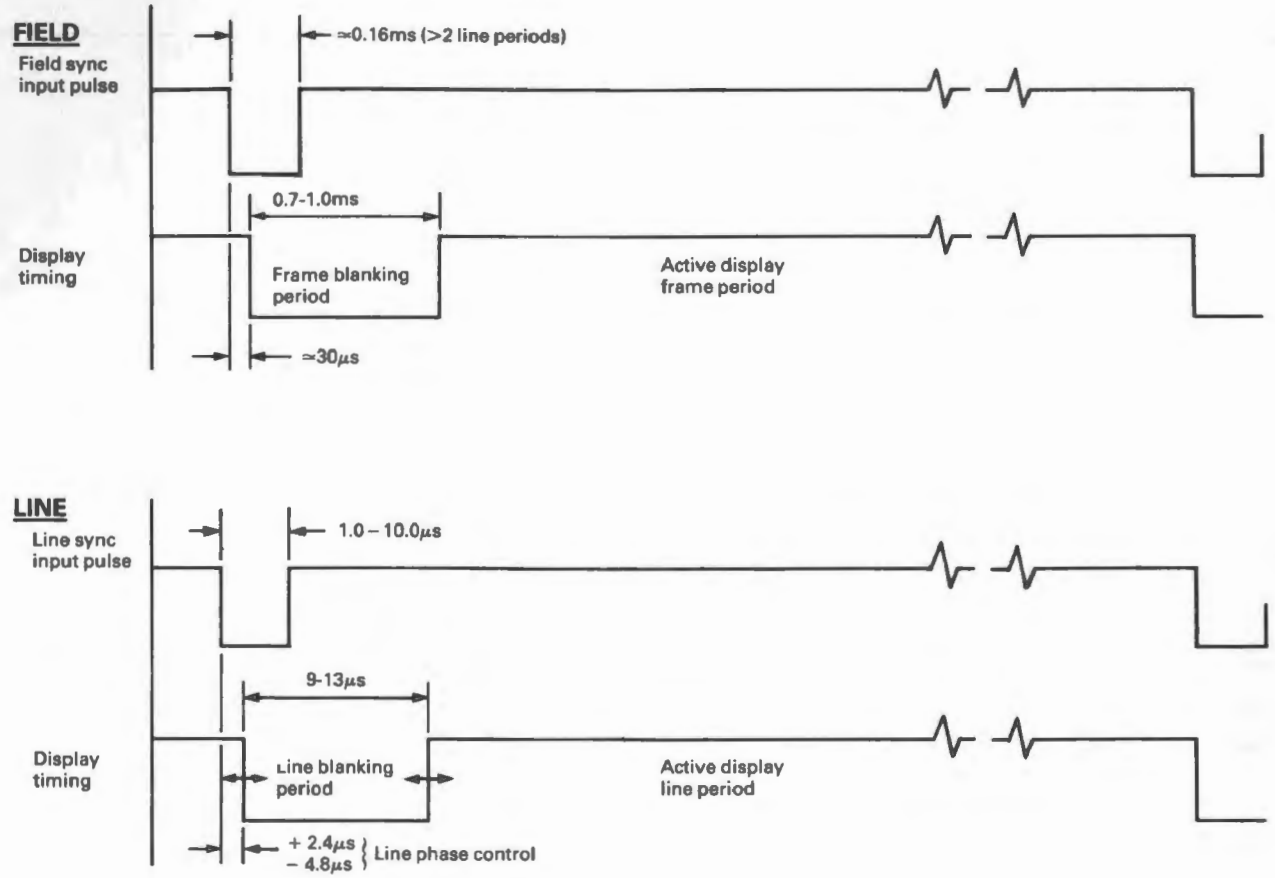


PL101

Pin Connections:

1. +12V
2. No Connection
3. Sync 3; Positive Field Sync
4. Red Video
5. Sync 2; Negative Field Sync
6. Green Video
7. Sync 1; Composite Sync or Line Sync
8. Blue Video
9. Normal/Inverse TTL Video
10. Ground

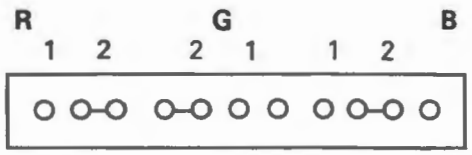
Figure 5 **Sync and Display timing. Example shows negative separate sync**



3. RGB (linear, 0-4V, 1500ohm) input conversion (Stock nos. 300-108, -120, -136)

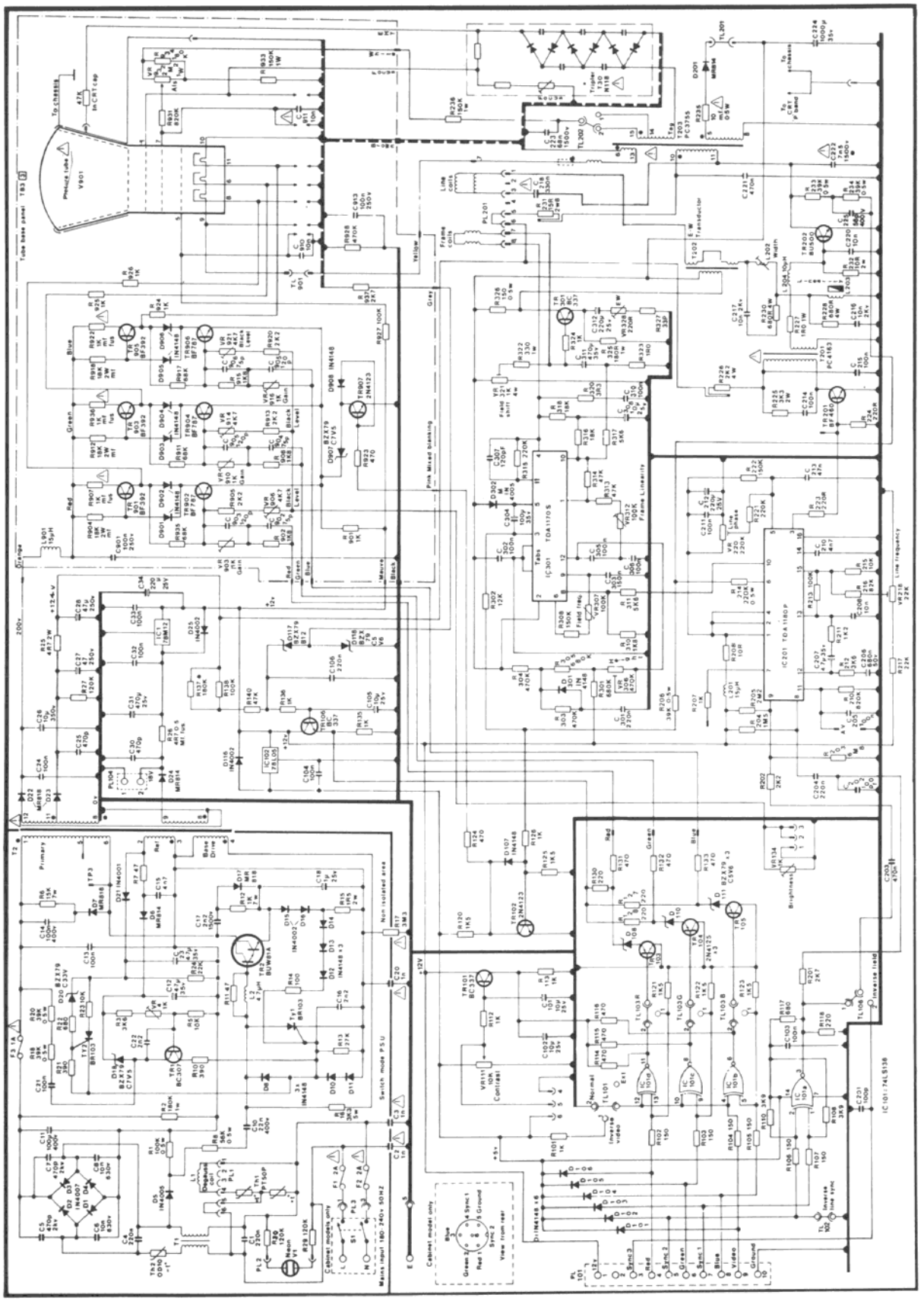
The three links on PL103 are each in positions R2, G2 and B2 to accept positive-going RGB (TTL level) inputs. For RGB (linear, 0-4V, 1500ohm) inputs each of the links, (R, G and B) need to be moved to positions R1, G1 and B1 (see Figures 3 and 6).

Figure 6 **PL103 showing R, G and B links in position 2, as supplied, for RGB(TTL) inputs**



For RGB (linear, 0-4V, 1500Ω) inputs move links R, G and B to position 1.

Figure 7 **Circuit diagram schematic**



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RS data

Static RAM with battery back-up 48Z02

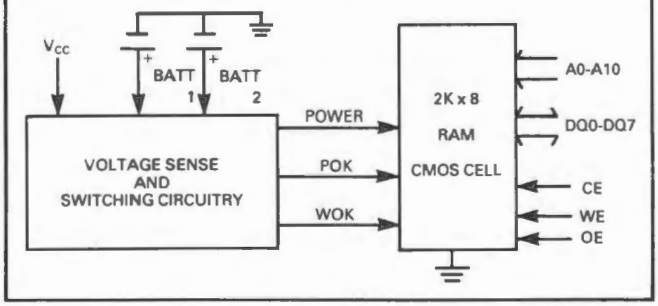
Stock number 301-016

A 2K x 8 bit CMOS static RAM with integral lithium batteries giving data retention for up to ten years. All control and switching circuitry is included on chip for data integrity at all times.

Absolute maximum ratings

Voltage on any pin relative to V_{SS} —0.3V to +7.0V
Operating temperature T (ambient) 0°C to +70°C
Storage temperature –20°C to +70°C
Power dissipation 1 Watt
Output current 20mA

Figure 1 **Internal block diagram**



Electrical characteristics

dc (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 volts + 10%-5%)

Parameter	Symbol	Min.	Max.	Units
Average V_{CC} Power Supply Current	I_{CC1}		80	mA
Input Leakage Current (any input)	I_{IL}	–1	1	µA
Output Leakage Current	I_{OL}	–5	5	µA
Output Logic '1' Voltage I_{OUT} = 1mA	V_{OH}	2.4		V
Output Logic '0' Voltage I_{OUT} = 2.1mA	V_{OL}		0.4	V
Standby V_{CC} Power Supply Current, CE = V_{IH}, all other inputs –.2 ≤ V_I ≤.2; or, V_{CC} –.2≤ V_I ≤ V_{CC} +.2	I_{CC2}		3	mA

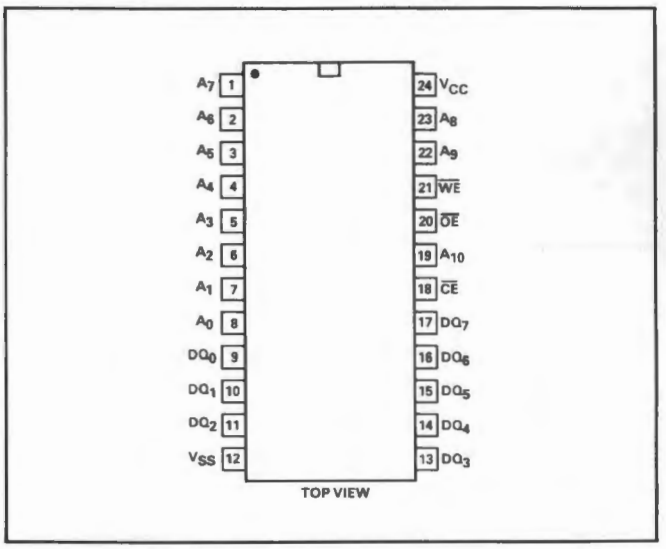
ac (0°C ≤ T_A ≤ 70°C) (V_{CC} = +5.0 volts +10%-5%)

Parameter	Symbol	Typ.	Max.
Capacitance on all pins (except D/Q)	C_I		7pF
Capacitance of D/Q pins	$C_{D/Q}$		10pF

Parameter	Symbol	Min.	Max.	Units
Read Cycle Time	t_{RC}	250		ns
Address Access Time	t_{AA}		250	ns
Chip Enable Access Time	t_{CEA}		250	ns

Features

- Ten year data retention in the absence of power
- Internal support circuit provides write protection
- Static operation
- Organisation: 2K x 8 bit RAM JEDEC pinout



Parameter	Symbol	Min.	Max.	Units
Chip Enable Data Off Time	t_{CEZ}		50	ns
Output Enable Access Time	t_{OEA}		75	ns
Output Enable Data Off Time	t_{OEZ}		50	ns
Output Hold from Address Change	t_{OH}	15		ns
Write Cycle Time	t_{WC}	250		ns
Address Setup Time	t_{AS}	0		ns
Address Valid to End of Write	t_{AW}		180	ns
Chip Enable to End of Write	t_{CEW}	160		ns
Data to Write Setup Time	t_{DSW}	100		ns
Data from Write Hold Time	t_{DHW}	0		ns
Write Pulse Duration	t_{WD}	160		ns
Write Enable Data Off Time	t_{WEZ}		80	ns
Write Recovery Time	t_{WR}	10		ns

Notes:
All voltages referenced to V_{SS}.
Measured with 0≤V_I≤5.0V outputs deselected and V_{CC} = 5.
AC measurements assume Transition Time = 5ns levels V_{SS} to 3.0V.

RS data

Figure 2 **Static read cycle**

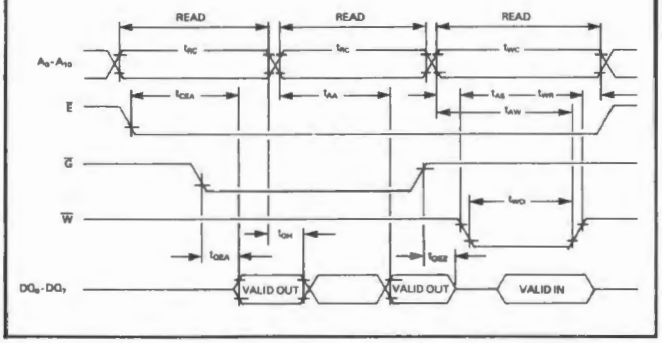
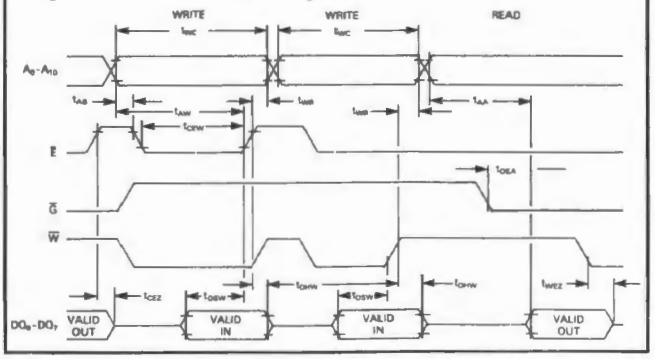


Figure 3 **Static write cycle**

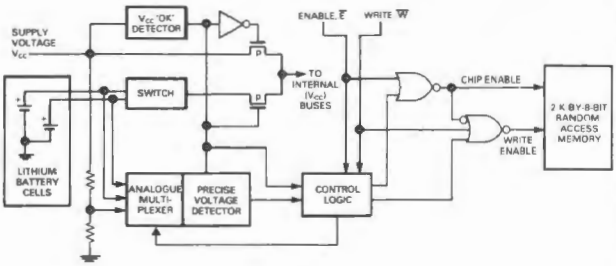


The voltage detector monitors the state of the lithium cells and the supply. Below a 3V supply the lithium batteries take over and V_{CC} is disconnected. A battery voltage below 2V is signalled by disabling the next write cycle.

Recommended dc operating conditions
($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Logic '1' Voltage All Inputs	V_{IH}	2.2		V_{CC}+.5V	V
Logic '0' Voltage All Inputs	V_{IL}	–0.3		.8	V

Figure 4 **Complete internal circuitry**



Truth table

V_{CC}	E	G	W	Mode	DQ
<5.5V volts	V_{IH}	X	X	Deselect	High Z
>4.75 volts	V_{IL}	X	V_{IL}	Write	D_{IN}
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High Z
<4.5 volts	X	X	X	Write Protect	High Z

X = Don't Care State.

Theorectical retention calculations

$$t = \frac{1}{a} \ln\left(1 + \frac{aE_0}{I_L}\right)$$

t = data retention time
a = battery capacity loss
E_0 = initial battery capacity
I_L = battery leakage current
ln = natural log

Temperature (C)	I_L (nA)	E_0 (nA-years)	a (fraction/year)	Retention time: first cell	Retention time: second cell		Total retention time, $t_1 + t_2$ (years)
				t_1 (years)	Capacity at t_1 (nA-years)	t_2 (years)	
25	5	4,000	0.005	320	800	118	438

As the retention time is so long the limiting factor will be the shelf life of the lithium cells, typically ten years.

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RS data

Rotary cam switches

A range of rotary cam switches for use in mains, control and instrument switching applications. Suitable for direct switching of motor loads, electric heating and lighting circuits (refer to electrical specification).

Conformity to standards

VDE0660: German specification for low-voltage switchgear.

BS4794 (IEC337) specification for control devices.

BS5419 (IEC408) specification for air break switches.

BS2771 (IEC204) specification for electrical equipment of machine tools.

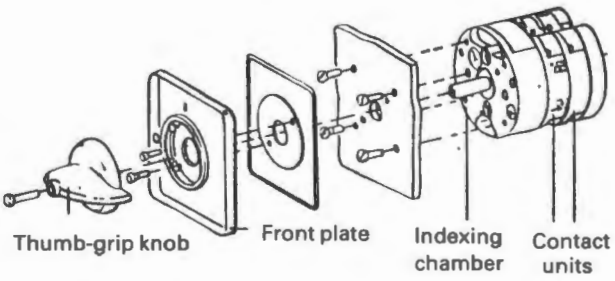
Approvals

VDE, IEC, NEC, NEMA, BSS, SEV, DEMKO, NEMKO, SEMKO, Finland.

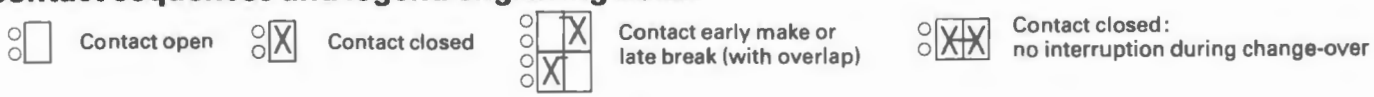
Stock No.	Description
337-251	on/off switch, 2 pole 0-1
337-245	on/off switch, 3 pole 0-1
336-595	on/off switch, 4 pole 0-1
337-273	change-over switch, 1 pole 1-2
336-589	change-over switch, 3 pole 1-2
337-267	change-over switch, 1 pole 2-0-1
333-350	c/o switch, 1 pole, hand-0-auto
336-573	change-over switch, 3 pole 2-0-1
336-567	voltmeter switch, phase/phase
336-551	voltmeter switch, ph/ph, ph/N
336-545	ammeter switch
Accessories:	
337-239	insulating boot
336-539	blank legend plate

Features

- Choice of three mounting methods, through front panel, as standard.
- Environmental protection through front panel up to IP55.
- Protection to rear of switch up to IP54 by using an insulating boot (see accessories).
- Attractive appearance – brushed aluminium legend plate with black surround and operating knob.
- High contact pressure and silver contacts ensure minimum contact resistance, high degree of control circuit reliability and a long life.
- Double break contacts ensure a high switching capacity for size of switch.



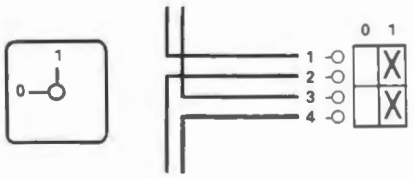
Contact sequences and legend engraving detail



On/Off switches

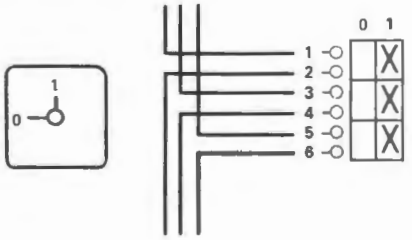
337-251

2 pole 0-1



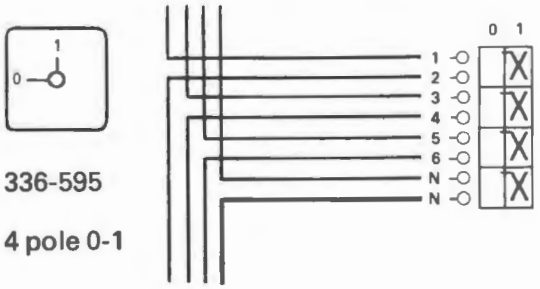
337-245

3 pole 0-1



336-595

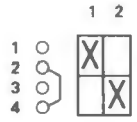
4 pole 0-1



Change-over switches

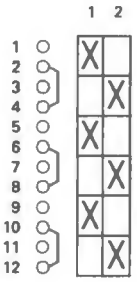
337-273

1 pole 1-2



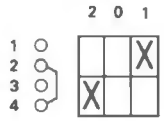
336-589

3 pole 1-2



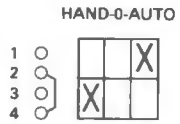
337-267

1 pole 2-0-1



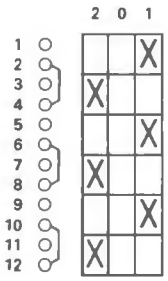
333-350

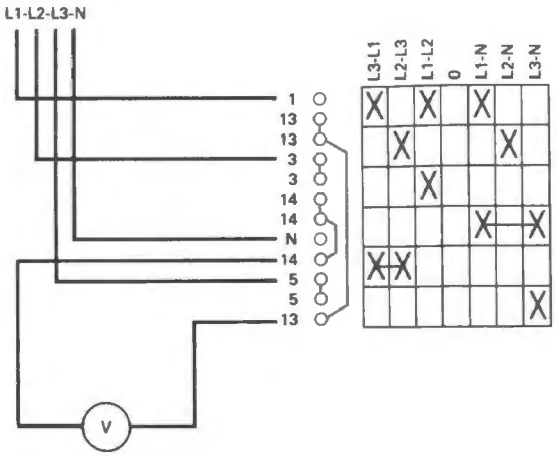
1 pole

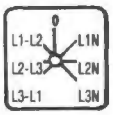


336-573

3 pole 2-0-1

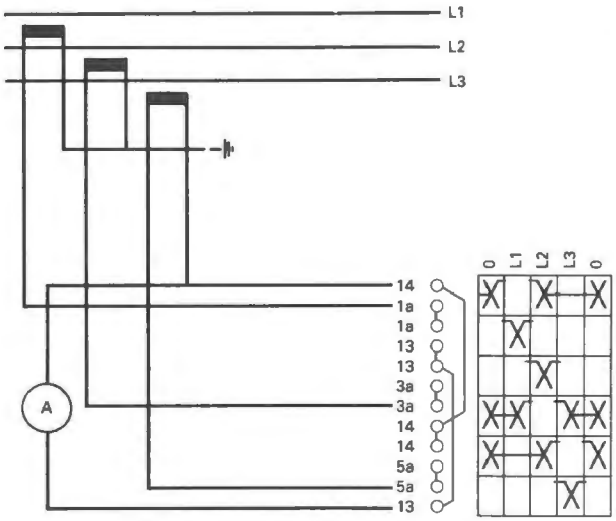


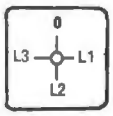




336-551

Voltmeter switch
ph/ph, ph/N

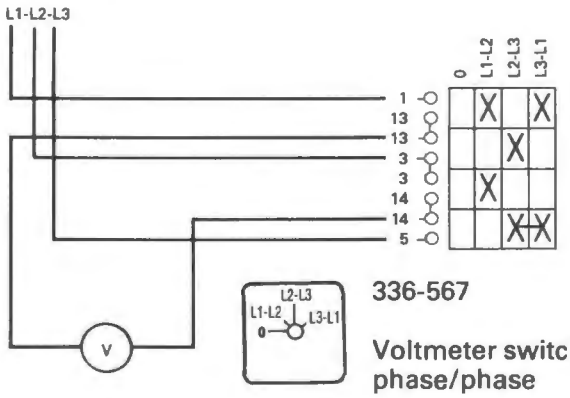




336-545

Ammeter switch

Instrument switches



336-567

Voltmeter switch
phase/phase

Markings on terminals

For on/off and change-over switches the terminals are consecutively marked (as CENELEC EN50005 for main contacts) incoming terminals are marked 1, 3, 5 etc, outgoing terminals are marked with the next even number.

Instrument switches are marked as shown above.

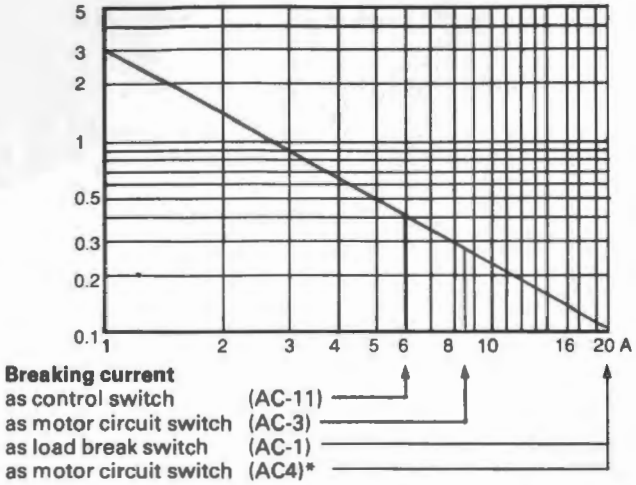
Technical data

Ambient temperature open –25/+50°C
enclosed –25/+40°C

Mechanical life span 3×10^6 operations

Max. frequency of operation 3000 ops/hr

Electrical life; dependent on breaking current (see curve).



*In order to achieve the life span, shown in the curve for AC4, the stalled motor current should not exceed the rated operational current (Ie) of 20A.

Contact ratings

Insulation voltage	660V a.c. 800V d.c.
Maximum frequency	5kHz
Continuous current	open 22A
	enclosed 20A

Switching capacities

AC1 Load break switches rated operation current (Ie) 20A

Three phase	110V	220/240V	380/440V	500V	660V
AC2/3	1.1kW (1.5hp)	3kW (4hp)	4kW (5.4hp)	5.5kW (7.4hp)	4kW (5.4hp)
AC4	0.6kW (0.8hp)	2.2kW (3hp)	3kW (4hp)	4kW (5.4hp)	3kW (4hp)
Single phase	0.4kW (0.5hp)	2.2kW (3hp)	2.2kW (3hp)	3kW (4hp)	2.2IW (3hp)
AC11	12A	6A	4A	3A	
DCI	(60V max per contact)		6A		
DCII	(32V max per contact)		10A		

The above utilisation categories are defined in
BS5424 part 1: 1977 (IEC 158-1)
BS4794 part 1: 1979 (IEC 337-1)

Mounting hole dimensions (All dimensions in mm)

Multi fixing cutouts

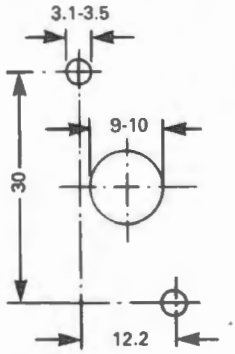


Figure 1

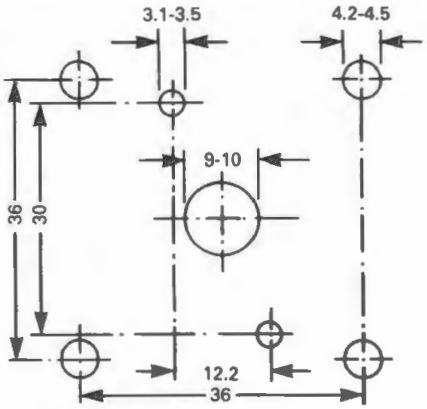
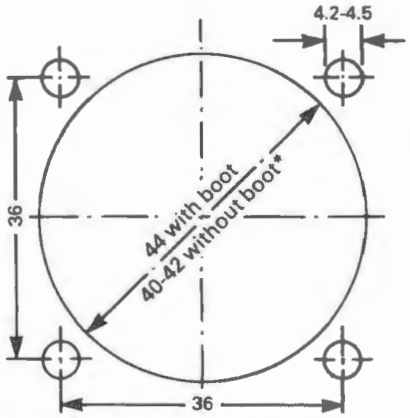


Figure 2



*40mm hole cutter available (543-670)

Figure 3

Single hole fixing cutouts

22.5mm (543-585) and 30mm (543-608) hole cutters available.

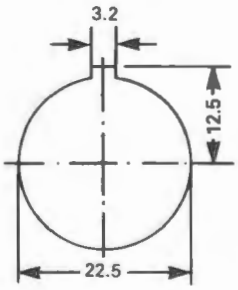


Figure 4

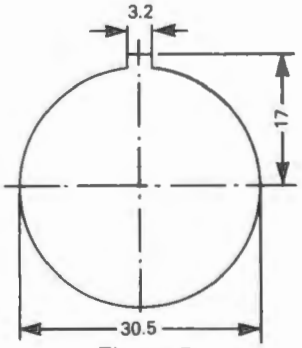


Figure 5

RS data

Mounting instructions

Screws supplied:
A 2.9 x 16mm self tapping, holding single hole adaptor to body.
B 2.9 x 13mm self tapping, supplied loose to mount bezel.
C 3.9 x 19mm self tapping, supplied loose with protective cover.

Single hole fixing

The switches may be mounted by a single hole; either 22.5mm, or 30.5mm with the adaptor ring (see Figures 4 and 5 for cutout dimensions). Panel thickness of 1.5 to 5mm may be accommodated with the screws as supplied, however, if screws A and B are interchanged panels of 5 to 8mm may be used.

N.B. The bezel is automatically polarised with respect to the switch body when mounted in this mode.

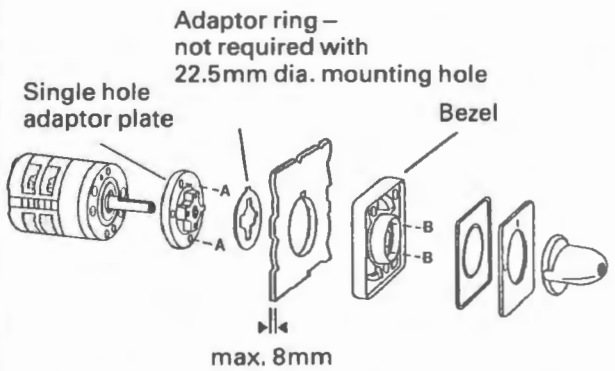


Figure 6 **Single hole fixing** (see Figures 4 and 5)

Multi-hole fixing

When mounting the switches, using one of the multi-hole fixing methods (see Figures 1, 2 and 3), the single hole adaptor plate and 30.5mm adaptor ring should be removed. The bezel may be mounted using four countersunk screws of up to 4mm diameter or if the protective boot is fitted the four supplied self tapping screws may be used (see Figure 8). The conical cable lead-outs at the rear of the protective boot should be cut according to the cable diameter and only one cable should be fed through each lead-out.

N.B. Figure 9 shows the correct orientation of the bezel with respect to the switch shaft.

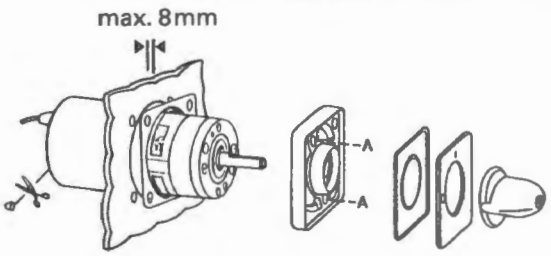


Figure 7 **Multi-hole fixing** (see Figure 3) – N.B. Protective boot may be omitted if not required

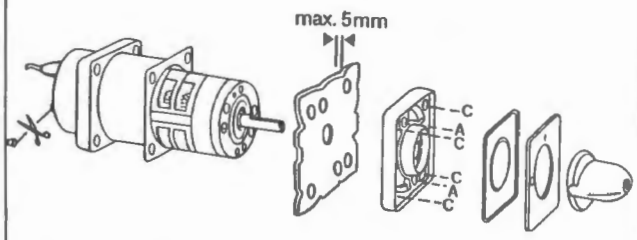


Figure 8 **Multi-hole fixing** (see Figures 1 and 2) – N.B. Protective boot may be omitted if not required

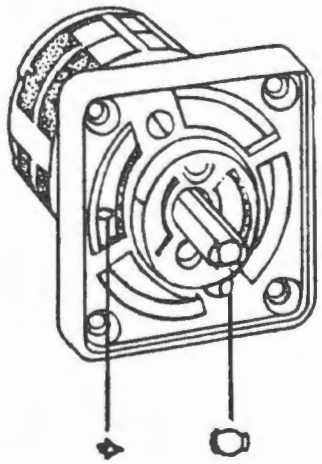


Figure 9 **Bezel and shaft orientation for multi-hole fixing**

Connection information

Connections are made by clamps using captive M3 screws with wire size range of 1mm^2 to 2.5mm^2 for solid wire, and 0.75mm^2 to 1.5mm^2 for flexible wire. Alternatively 4BA spade crimp connectors may be used. These are available from RS (please see current catalogue).

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RS data

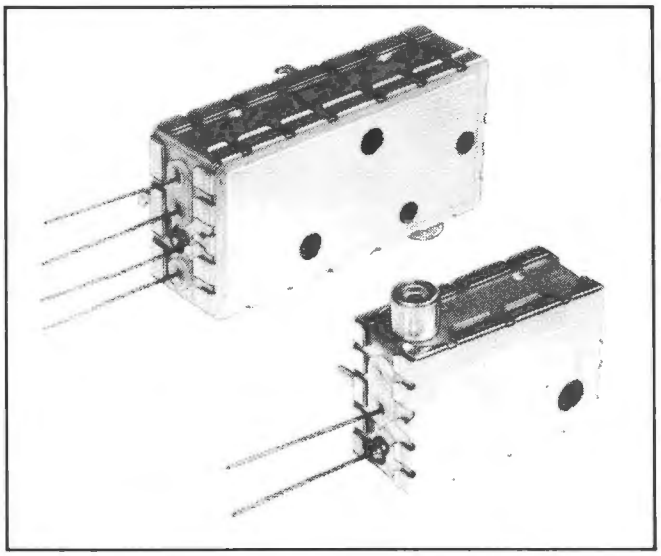
Video modulators UM1233 and UM1286

Stock numbers 300-316 and 300-322

Two UHF modulators primarily intended for use as an interface for a colour or black and white television and; computer graphics, computer games, Teletext and Viewdata etc. The modulators are high performance units featuring low radiation and harmonics in line with European specifications. Both modulators are pretuned to channel 36 and have a 75Ω output from a standard phono socket. The UM1233 is video only and the UM1286 has in addition a built in 6MHz intercarrier facility for use where a sound carrier is required. Both modulators feature good subcarrier intermodulation performance to minimise visible patterning due to chroma and sound signals beating.

Features

- Good modulation linearity
- Pretuned to channel 36
- Low RF radiation
- Low current drain
- 75Ω output from a standard phono socket
- Suitable for PCB mounting



Specifications

	UM1233	UM1286	Units
Channel	E36	E36	
Channel frequency (nominal)	591.5	591.5	MHz
Supply voltage	5 ±0.2	5 ±0.2	V
Supply current (typ.)	6	9	mA
Bandwidth	8	8	MHz
Sound subcarrier	–	6	MHz
Transfer characteristic	Negative	Negative	
Audio signal	–	5	Vp-p
Maximum RF output (nominal)	1.5	2.0	mV

Both modulators are designed to work at a supply voltage (V_{CC}) of 5V DC ± 0.2 volts.

Modulation occurs when a positive going voltage is applied to the modulation input (video) pin. The transfer characteristic is negative which means a positive input causes the RF output to decrease. (See typical input waveforms.)

When using the UM1286 Intercarrier Frequency Modulation takes place when an audio signal is applied to the sound input pin. A 5V p-p audio signal gives the standard 100kHz maximum FM deviation. The sound subcarrier frequency can be fine tuned by applying a DC voltage at the fine tune pin, or a 100k trimpot tied from the fine tune pin to V_{CC} (+5V). For simpler applications, a 39k resistor can be connected to V_{CC} (+5V). A DC level of +3.2V at the fine tune pin gives typically a 6.0MHz subcarrier frequency.

RS data

Typical input waveforms

Figure 1 **UM1233**

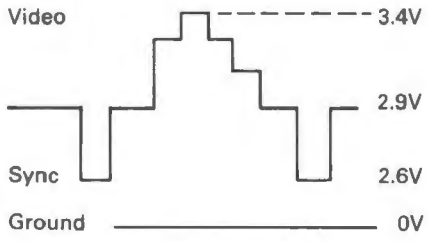
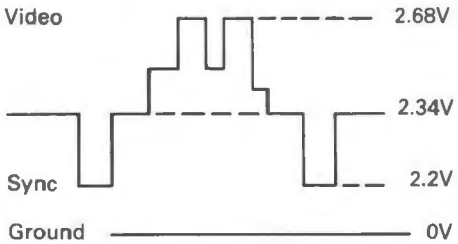


Figure 2 **UM1286**



Dimensions and recommended PCB hole centres

Figure 3 **UM1233**

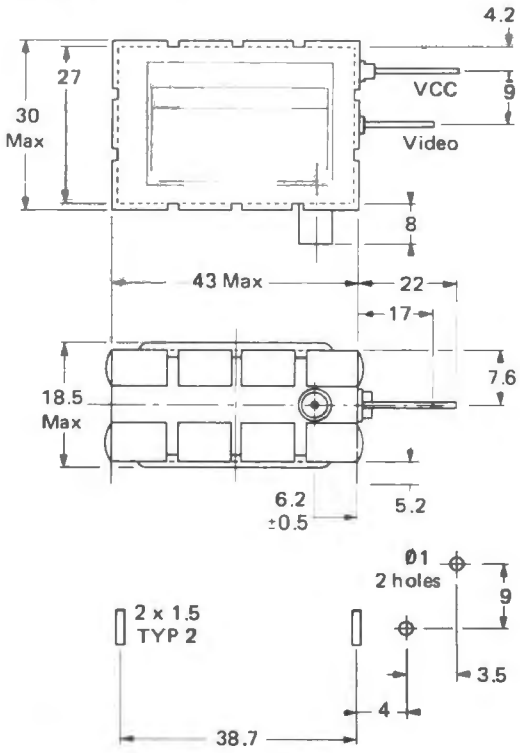


Figure 4 **UM1286**

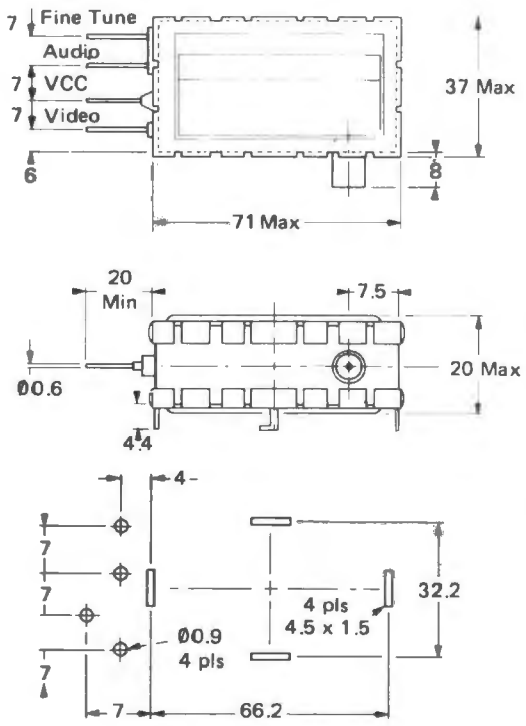
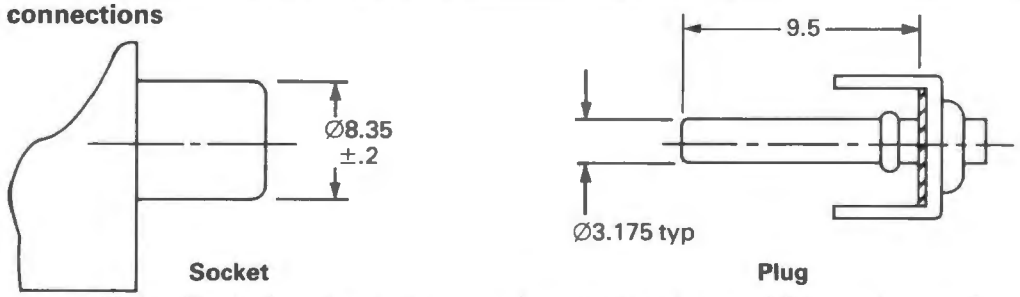


Figure 5 **Phono connections**



Note: Central contact of phono plug must not exceed 9.5mm in length

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RS data

Hall effect switches

Hall effect ic switch (307-446)

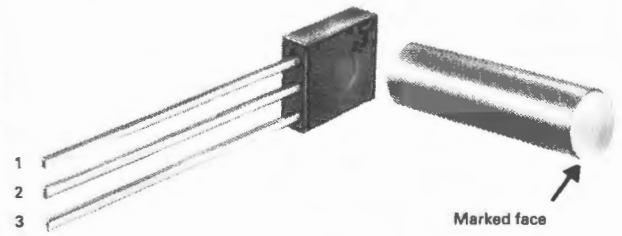
A miniature semi-conductor proximity switch utilising the Hall effect to give 'bounce-free' switching when influenced by a magnetic field. A magnet is supplied which allows switching at distances up to 4mm. This may be increased if the Hall effect ic is mounted against a ferromagnetic surface. The device is magnetically unidirectional requiring the marked south pole of the magnet to face away from the magnetic centre indicated by the dimple, or alternatively the magnet may be positioned on the other side of the ic but in this instance the marked face of magnet should be towards the ic. Ideal for use in logic circuits where 'bounce free' switching is necessary.

The device will typically operate up to a 100kHz repetition rate.

The circuit output can be interfaced directly with bipolar or MOS logic circuits.

Features

- Operates from 4.5V to 24V DC power source
- Supplied complete with permanent magnet
- High reliability – eliminates contact wear, contact bounce; no moving parts
- Small size
- Constant amplitude output
- Output compatible with all logic families



1. Output
2. Common
3. Supply

Absolute maximum ratings

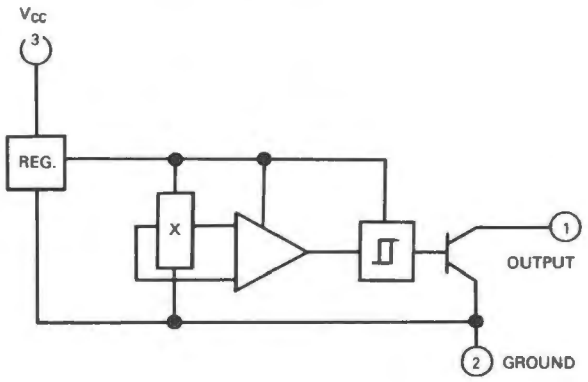
Power supply, V_{CC} ——— 25V
Magnetic flux density, B ——— Unlimited
Output 'OFF' Voltage, $V_{OUT(OFF)}$ ——— 25V
Output 'ON' current, I_{SINK} ——— 50mA
Storage temperature range, T_S —— –65°C to +150°C
Operating temperature range, T_A —— 0°C to +70°C

Electrical characteristics V_{CC} = 4.5V to 24V DC, T_A = 25°C

Characteristic	Symbol	Test conditions	Limits			Units
			Min.	Typ.	Max.	
Magnetic flux density 'Operate point' 'Release point'	 B_{OP} B_{RP}		 – 50	 220 165	 350 –	 Gauss Gauss
Hysteresis	B_H		20	55	–	Gauss
Output saturation voltage	V_{SAT}	B ≥ 350 Gauss, I_{SINK} = 15mA	–	85	400	mV
Output leakage current	I_{OFF}	B ≤ 50 Gauss, V_{OUT} = 24V	–	0.1	20	μA
Supply current	I_{CC}	V_{CC} = 4.5V, output open	–	5	9	mA
		V_{CC} = 24V, output open	–	6	14	mA
Output rise time	t_r	V_{CC} = 12V, R_L = 820Ω, C_L = 20pF	–	15	–	ns
Output fall time	t_f	V_{CC} = 12V, R_L = 820Ω, C_L = 20pF	–	100	–	ns

Note: 10 gauss = 1 milliTesla (1mT).

Figure 1 **Functional block diagram**

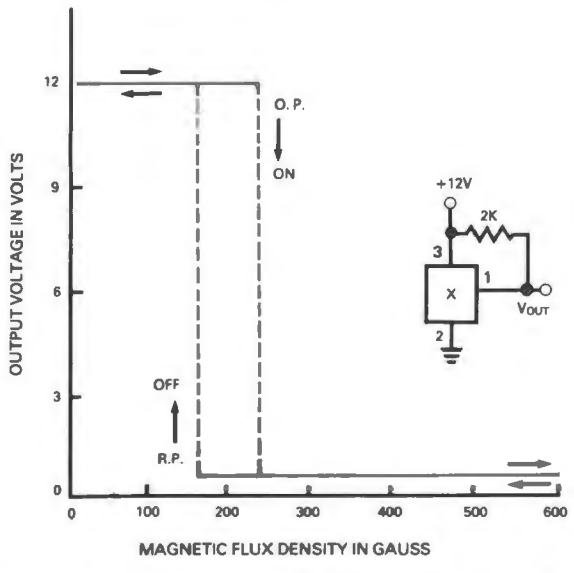


Operation

The output transistor is normally 'off' when the magnetic field perpendicular to the surface of the chip is below the threshold or 'operate point.' When the field exceeds the 'operate point,' the output transistor switches 'on' and is capable of sinking 20mA of current.

The output transistor switches 'off' when the magnetic field is reduced below the 'release point' which is less than the 'operate point'. This is illustrated graphically in the transfer characteristics curve, see Figure 2. The hysteresis characteristic provides for unambiguous or non-oscillatory switching.

Figure 2 **Transfer characteristics showing hysteresis**



Switching point variations with temperature should be considered in applications covering a wide temperature range (see Figure 3).

Figure 3 **Switching point variation with temperature**

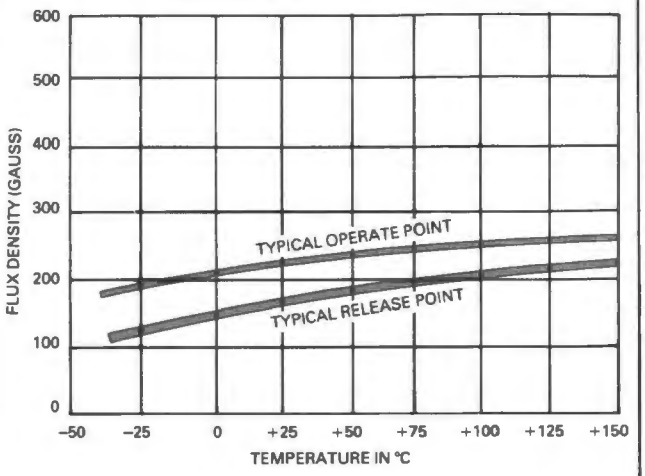


Figure 4

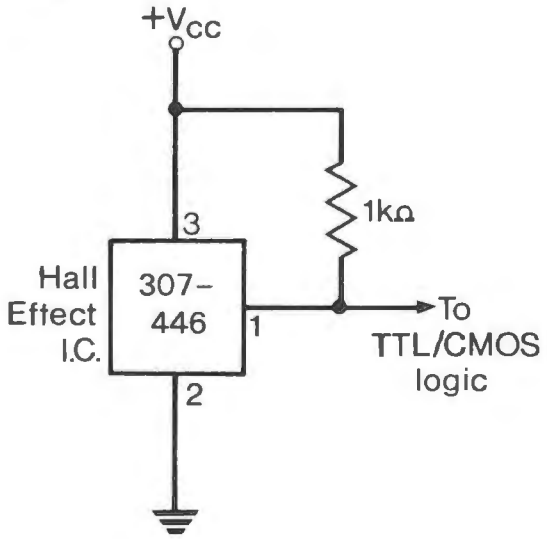
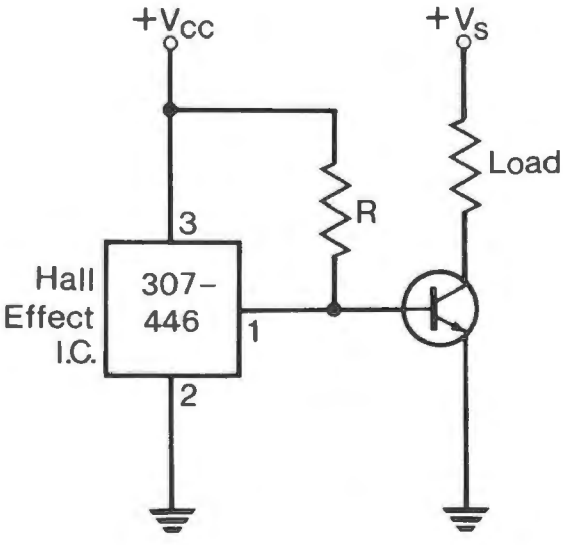


Figure 5



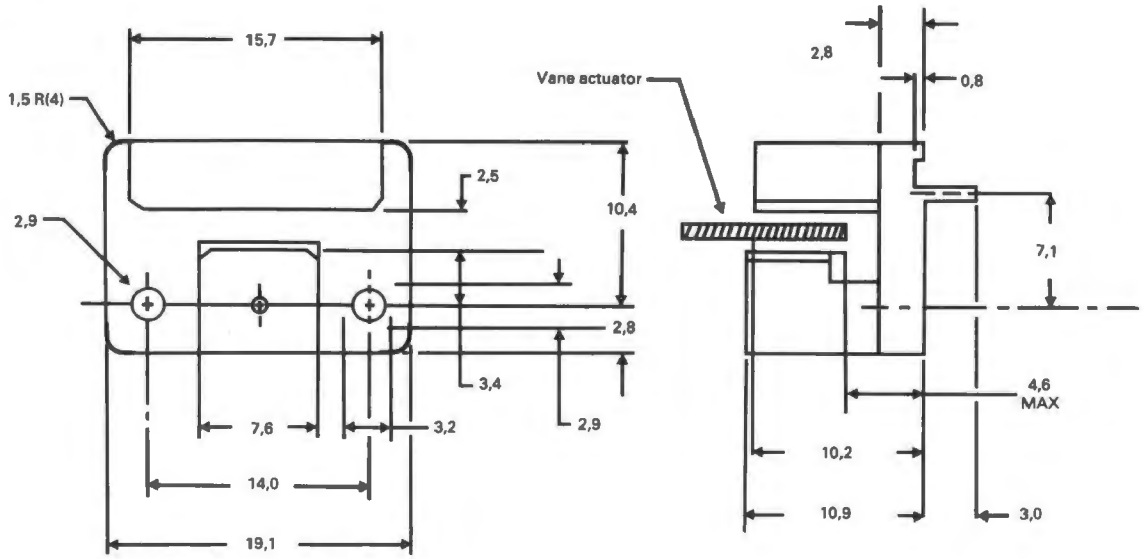
Hall effect vane switch (309-492)

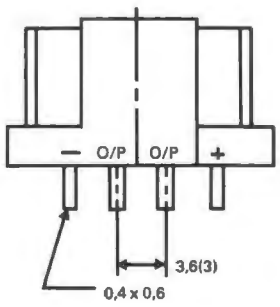
A Hall effect sensor and magnet house in a pcb mounting package which will detect the presence of a ferrous metal vane passing through the gap between sensor and magnet to produce a 'bounce free' switched output. The device, which operates from 5V DC (7mA quiescent current) features two independent TTL compatible outputs capable of sinking up to 4mA each or 8mA combined. This versatile device will find many uses in position or counting applications, particularly in dusty or high ambient light environments, where an optical switch would be unsuitable.

Electrical specification

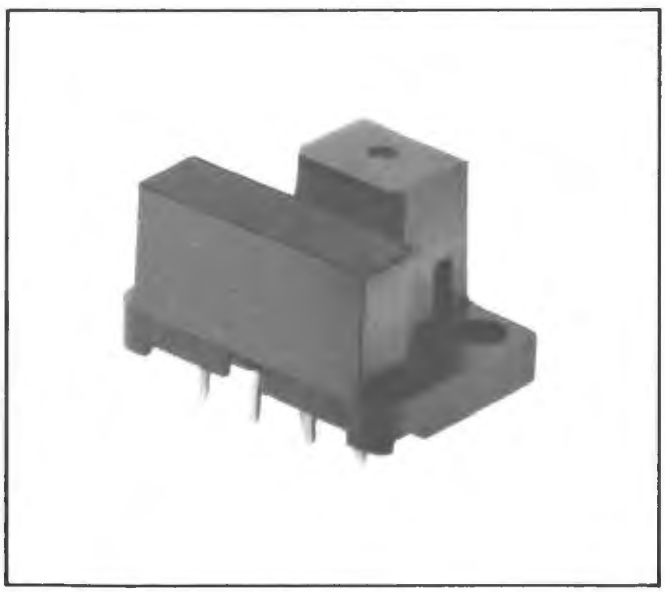
Supply voltage	+4.5V to + 5.5V DC
Supply current	7mA (max)
Output voltage (each output)	0.4V (sinking 4mA)
Output current (each output)	4mA (max)
Output leakage current	10μA (max)
Max operating frequency	100kHz
Switching time: rise	2.0μs (max)
fall	1.0μs (max)
Operating temperature	–40°C to +85°C

Figure 6 **Dimensions**





Tin plated terminals (4)

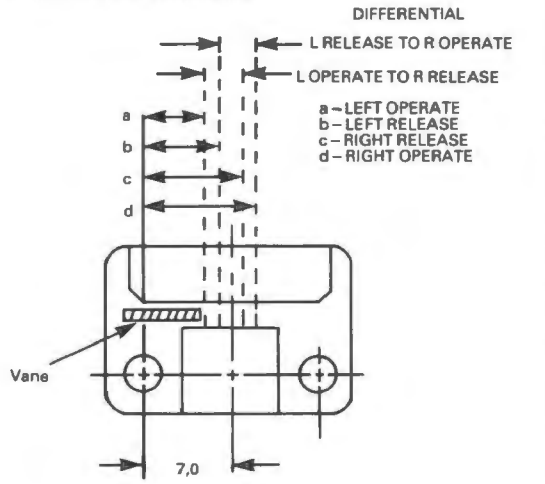


Actuation details

With no vane in gap, output is operated (conducting).

With vane in gap, output is released (non-conducting).

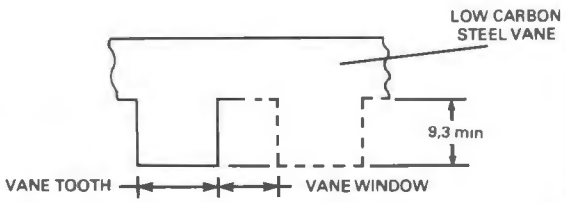
Figure 7 **Actuation details**



From left to right				
Left		Right		
a	b	d	c	Diff.
5.36	6.07	8.61	7.90	0.71

Vane dimensions

Thickness	Min. window	Min. tooth
1.0	10.2	10.2
1.6	10.2	6.3



Typical applications

Figure 8 **Basic circuit**

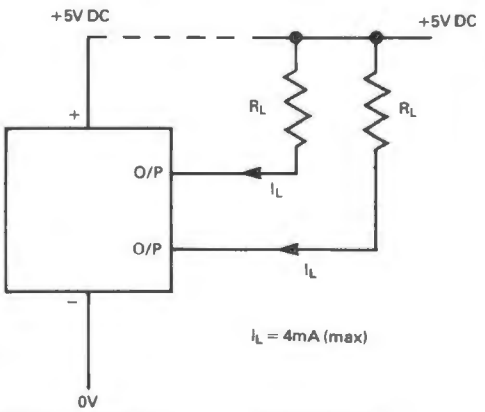


Figure 9 **Driving TTL**

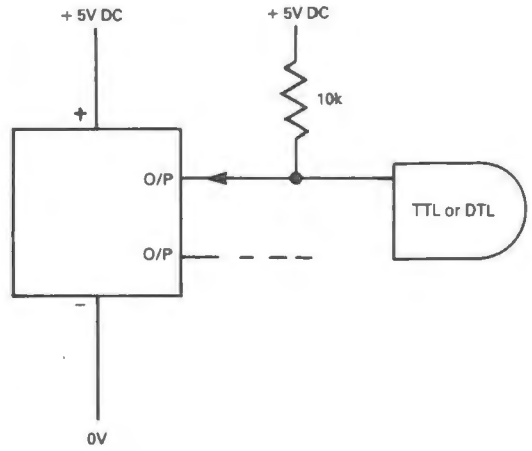


Figure 10 **Increased output**

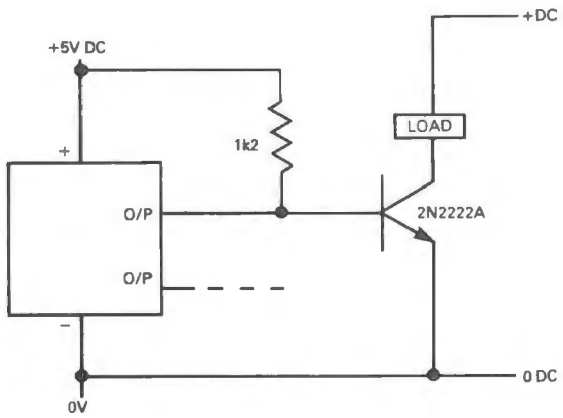
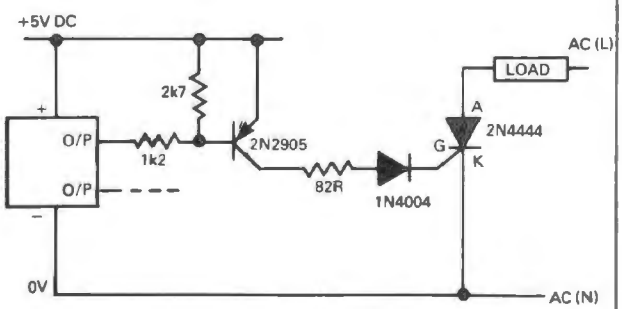


Figure 11 **Thyristor drive**



Linear Hall effect ic (304-267)

A miniature linear output Hall effect sensor in a moulded 4-pin dil plastic package. This device features a differential output stage. One output increases linearly in voltage whilst the other decreases for a linear increase in magnetic flux density over a ±40mT range.

Typical applications for this versatile ic include magnetic field investigation in the vicinity of transformers and cables, current sensors with high isolation, linear feedback elements in analogue control systems, etc. The sensor is immune from damage by high values of flux density.

Absolute maximum ratings

Supply voltage	+12V DC
Output current	20mA
Operating frequency	100kHz
Operating temperature	–40°C to +100°C
Storage temperature	–55°C to +150°C

Electrical characteristics

Supply voltage (VDC)	Supply current (mA)	Output type	Output voltage	Sensitivity
4 to 10	3.5 typ.	Differential outputs, linear	1.75 to 2.25V at 5V & 0 Gauss	(–400 to +400 Gauss) 0.75 to 1.06mV/Gauss

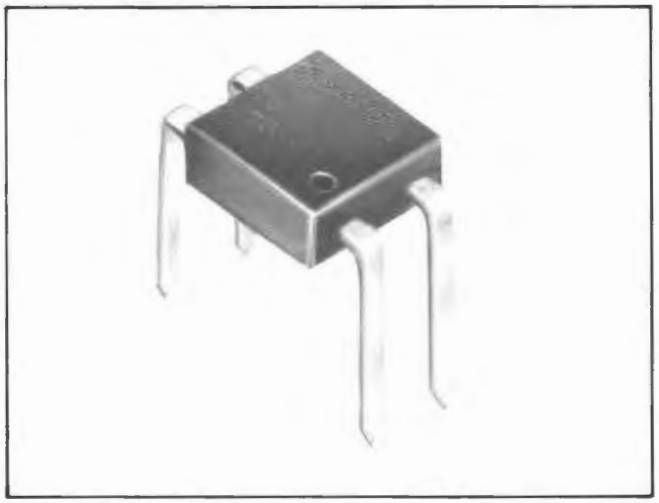
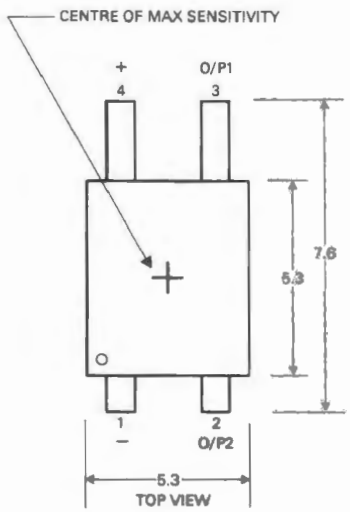


Figure 11 **Dimensions**



Typical linear output characteristics

The linear Hall effect ic features differential outputs. One output increases, whilst the other output decreases with an increase in Gauss.

Figure 12 **Typical output characteristics as a function of supply voltage**

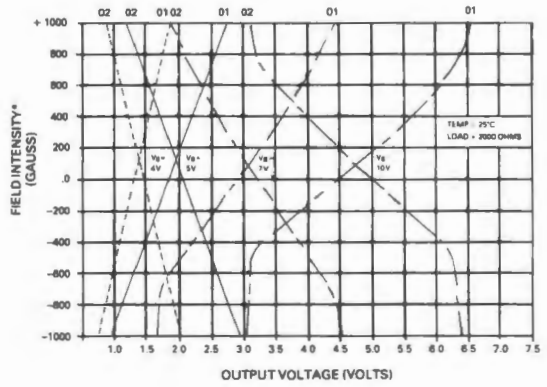
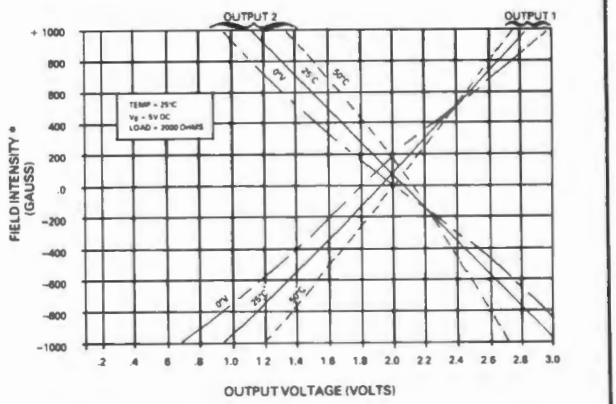


Figure 13 **Typical output characteristics as a function of temperature**

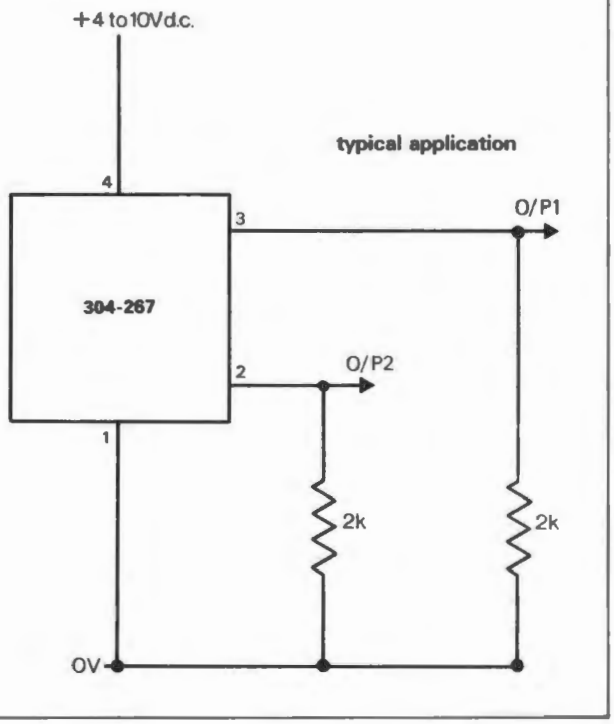


* Positive Gauss represents the South pole of the magnet facing the sensing area. Negative Gauss represents the North pole of the magnet facing the sensing area.

RS data

Typical application

Figure 14



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RS data

Bucket-brigade delay line TDA 1097

Stock number 300-350

In the electronic production and reproduction of music and speech, artificial delay has many potential applications. In electronic organs, for example, it can be used to introduce vibrato and chorus effects. In playing back recorded music it can be used to simulate reverberation, restoring the spatial presence that is often deliberately avoided in the recording studio. It can improve the intelligibility of announcements broadcast over multiple loudspeakers in large halls or public gathering places. And it can even be used to restore the natural timbre and pitch of speech played back faster or slower than the speed at which it was recorded.

For some applications of artificial delay, various expedients have gained a limited acceptance. These include magnetic discs and loops, tape recorders with multiple heads, and metal springs and plates. In general, though, the best of these are too expensive or too specialized for common use, and the performance of the cheaper and less specialized is too limited.

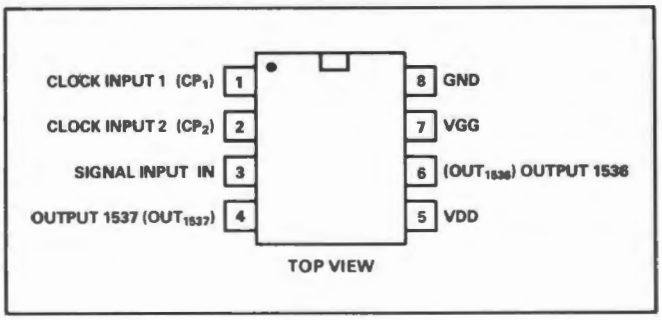
The TDA1097 is a 1536-stage delay line particularly suitable for analogue signal processing. The delay time imposed between signal input and signal output can be varied between 153.6ms and 7.68ms by using clock frequencies in the range 5kHz to 100kHz.

Absolute maximum ratings

Voltage range for all pins,
with respect to GND (pin 8) ——— 0 to −20V
Current into any input or output ——— ± 10mA
Operating temperature range ——— −20 to +60°C
Storage temperature range ——— −40 to +150°C

Features

- Analogue delays from 153.6 to 7.68ms.
- Easily cascaded for greater delays.
- d.c. to 25kHz input frequency range.
- 1536 stages.
- Ideally suited for generating musical effects.



WARNING!

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Operating conditions $T_{amb} = -20$ to $+60°C$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Negative supply voltage	$-V_{DD}$	12	–	16	V
Tetrode gate voltage	V_{GG}	–	$V_{DD}+1$	–	V
Clock voltage HIGH	V_{CPH}	0	–	–1,5	V
Clock voltage LOW	V_{CPL}	–	V_{DD}	–	V
Clock input capacitance	C_{CP}	–	–	600	pF
Clock frequency	f_{CP}	5	–	100	kHz
Clock pulse width (see note 1)	t_{CPW}	–	–	$0,5 \times T_{CP}$	
Clock rise/fall time (see note 1)	t_r, t_f	–	$0,05 \times T_{CP}$	500	ns
Clock cross point	V_x	0	–	–3	V
Signal input frequency	f_{IN}	0	–	$0,3 \times f_{CP}$ or 25	kHz
DC input bias voltage (see note 2)	$-V_{INbias}$	6	–	8	V
Load resistance	R_L	10	50	–	kΩ

Notes: **1.** T_{CP} = period time = $1/f_{CP}$ (see also Figure 5).
2. Adjust V_{INbias} for minimum distortion.

Characteristics

$T_{amb} = 25°C$; $-V_{DD} = -V_{CPL} = 15V$; $V_{CPH} = 0V$; $-V_{GG} = 14V$; $R_L = 50k\Omega$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal input voltage swing (rms value) at $f_{CP} = 40kHz$; $f_{IN} = 1kHz$; total harmonic distortion at output = 2%	V_{IN}(rms)	–	–	1,5	V
Attenuation from input to output at $f_{CP} = 40kHz$; $f_{IN} = 1kHz$	A	–2	0	2	dB
Change in attenuation when f_{CP} varies from 5kHz to 100kHz at $f_{IN} = 1kHz$; V_{IN}(rms) = 1V	ΔA	–	0,5	1	dB
DC output voltage shift when f_{CP} varies from 5 to 100kHz	ΔV_{OUT}	–	–	0,5	V
Output noise voltage (rms value) at $f_{CP} = 100kHz$; weighted according to IEC 173 (A-curve)	V_{no}(rms)	–	0,3	0,6	mV
Signal-to-noise ratio at $f_{CP} = 100kHz$; weighted according to IEC 173 (A-curve)	S/N	–	77	–	dB

Introduction to the bucket-brigade delay line

To characterise an analogue signal of B hertz completely, at least 2B samples per second are needed. If these are stored in the stages of a kind of shift register then the attractive features of the shift register – especially as a delay line – can be used for analogue signal handling.

Sampled values of the analogue signal are stored in the form of charges on a series of capacitors. Between successive capacitors is a switch that transfers the charge from one capacitor to the next on command of a clock pulse. By analogy with the old fire-fighting method, in which buckets of water were passed along the line from man to man, a delay line of this sort is known as a bucket-brigade.

Since each capacitor cannot take up a new charge until it has passed on its previous one, only half the capacitors carry information and the ones in between are empty. Starting from the condition shown in Figure 1(a), the transfer proceeds in two stages:

in the first, bucket 1 empties into bucket 2, and bucket 3 into bucket 4;

and in the second, bucket 2 empties into bucket 3, and bucket 4 into bucket 5.

Two antiphase clock signals are required; one to govern the emptying of even-numbered, and the other of odd-numbered buckets.

There is a practical drawback to the scheme illustrated in Figure 1. The buckets in which the samples are stored must empty completely during each transfer. In practice, the buckets are capacitors and the samples are charges on them. Owing to leakage current, complete discharge is difficult to ensure. So instead, the scheme illustrated in Figure 2 is adopted.

Figure 2(a) represents the initial condition; buckets 2 and 4 are full, and samples are stored in buckets 1

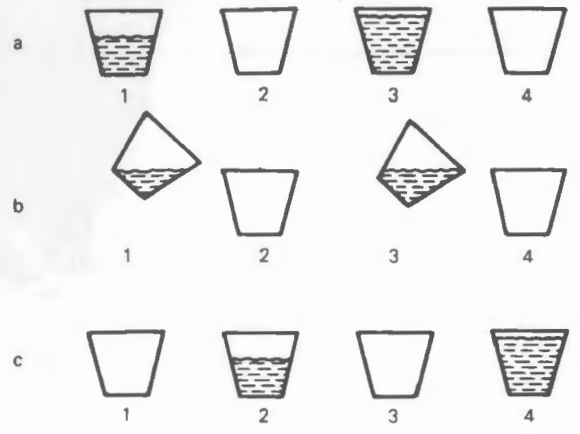


Figure 1 **Sample transfer in a bucket-brigade, simplified scheme. Samples in buckets 1 and 3 (a) are poured into empty buckets 2 and 4 (b); thus, the samples move step by step from left to right (c)**

and 3. During the first transfer, bucket 2 fills bucket 1, and bucket 4 fills bucket 3. What remains in bucket 2 is then equal to the original contents of bucket 1, and what remains in bucket 4 is equal to the original contents of bucket 3. During the next transfer, bucket 3 fills bucket 2, and bucket 5 fills bucket 4. Thus, as the buckets empty from right to left, the sampled quantities move, as before, from left to right; that is, from input to output. This is the scheme used in a practical bucket-brigade delay line.

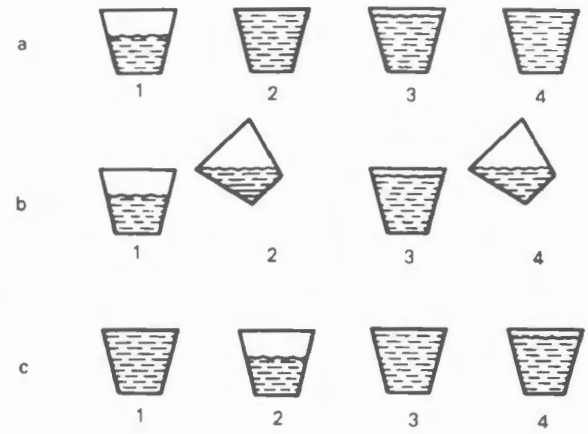


Figure 2 **Sample transfer in a bucket-brigade, practical scheme. Buckets 1 and 3 contain samples (a); when full buckets 2 and 4 are poured into them (b), the sample quantities move, as before, from left to right (c)**

Bucket-brigade delay line as an integrated circuit

A bucket-brigade delay line based on discrete components would be impracticable. Even at the low frequencies encountered in audio applications, the number of storage capacitors and switches needed to give any reasonable delay would be prohibitive. The alternative is therefore integration, and the most advantageous technology is MOS.

Figure 3 shows the circuit of the TDA1097, an integrated bucket-brigade having 1536 delay stages. The transistors of which it is made up are p-channel enhancement-mode MOS, which means that the clock signals, CP1 and CP2, must be negative with respect to earth.

When clock signal CP1 goes negative, the input transistor connects the sampling capacitor C_S to the analogue input signal at pin 3. As long as the transistor conducts, the voltage across the capacitor tracks the voltage at pin 3, so the sample ultimately stored in the capacitor is the signal voltage at the instant when CP1 goes positive and the transistor ceases to conduct. The sample is shifted into the first 'bucket' capacitor, C_1, when CP2 goes negative, and from the first to the second when CP1 again goes negative.

If the output of the delay line were to be taken direct from the 1536th stage, its envelope would be as shown in Figure 4(a), where the clock frequency is fully present. Strong low-frequency filtering would be required and the filters would be expensive because their characteristics would have to be very steep-sided to ensure adequate bandwidth. Precautions would also have to be taken about restoring the sampled amplitudes of low-frequency signals, for heavy filtering would distort the higher audio frequencies.

To avoid these problems the TDA1097 is split into two paths after the 1535th stage. One path goes from the 1536th stage to the output buffer connected to pin 6 (see Figure 3); and the other goes via a 1537th stage, giving an extra half-clock-period delay, to the output buffer connected to pin 4. Summing the outputs at pins 4 and 6 gives the envelope shown in Figure 4(b).

The delay obtainable, t, is given by

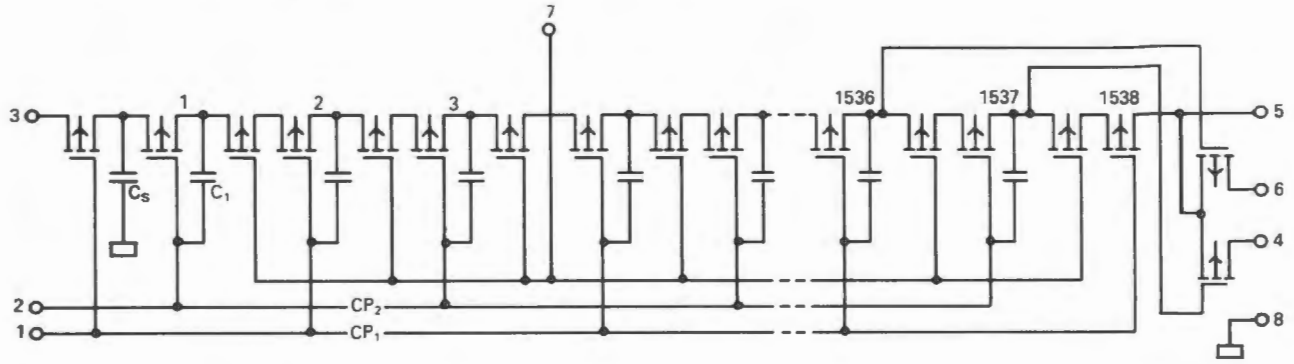
$$t = \frac{n}{2f_{cp}}$$

where n is the number of stages and f_{CP} is the clock frequency ($f_{CP} = f_{CP}1 = f_{CP}2$). Since the TDA1097 is designed for operation at clock frequencies from 5 kHz to 100 kHz, the delay obtainable from a single device (effectively 1536 stages) is 153.6 ms to 7.68 ms.

The timing diagram of the clock pulses is shown in Figure 5. Clock pulse voltage level HIGH is 0 to −1.5 V and LOW is $-V_{DD}$. Rise and fall times are typically 0.05 T, where T is the period, $1/f_{CP}$. The clock pulse width should be equal to or less than 0.5 T.

The TDA1097 is designed for input signal frequencies from 0 to 0.3 x f_{CP} (or 25kHz max) at levels up to 1.5 V rms (4.2 V peak-to-peak). The highest signal frequency to be delayed, f_{max} imposes a further limitation on the delay obtainable. To characterise the signal completely, the sampling rate must be at least $2f_{max}$; however, to avoid sideband interference a higher rate is required, at least $3f_{max}$. Thus, if

Figure 3 **The 1097 integrated bucket-brigade delay line**



f_{max} is, say, 10 kHz, the clock frequency must be at least 30 kHz. The maximum delay obtainable from a single TDA1097 is then

$$t = \frac{1536}{2 \times 30 \times 10^3} = 25.6\,\text{ms}.$$

For greater delays, additional TDA1097s must be cascaded. However, shorter delays, down to the 7.68 ms minimum, can be obtained merely by increasing the clock frequency. The DC shift over all stages of the TDA1097 is less than 0.5 V as the clock frequency is varied between 5 and 100 kHz.

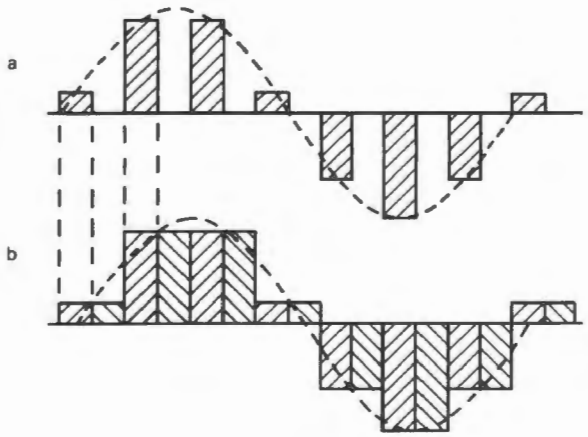
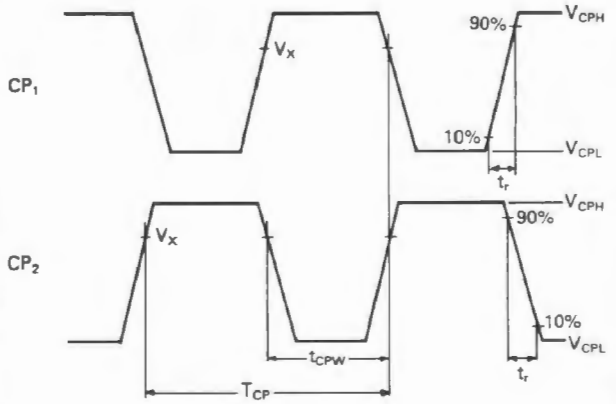


Figure 4 **(a) Envelope of clocked pulse samples requires strong low-pass filtering to suppress clock-frequency. (b) Supplementing main output by half-clock-period delayed pulses restores continuity and simplifies filtering**

Figure 5 **Clock pulse timing**

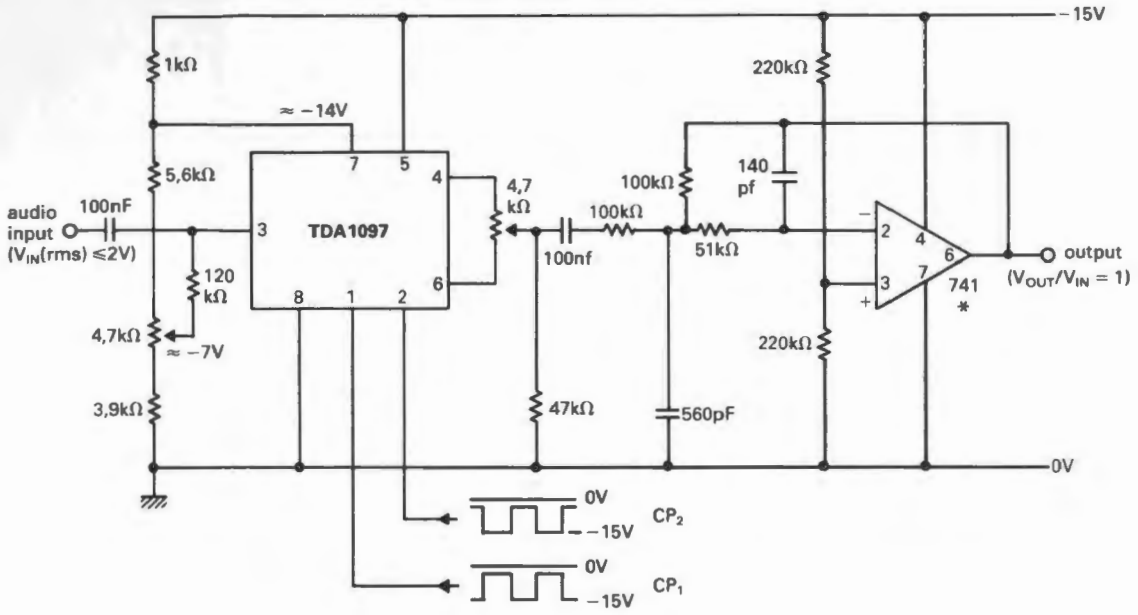


Applications information

Figure 6 shows the TDA1097 used as a simple delay line. The delayed signal is fed to a low pass fitter with a cut-off frequency of 8 kHz that is used to remove the sampled nature of the waveform. With a 20 kHz clock frequency a delay of 38.4 ms is produced. Longer or shorter delays may be generated by altering the clock frequency however to maintain the same degree of filtering the break point of the filter must be changed correspondingly.

Longer delays may be produced by cascading two or more TDA1097s as shown in Figure 7. Both devices are run from the same clock. To prevent voltage offsets from adding, each device is biased separately with the input AC coupled.

Figure 6 **Single delay line: t_D = 38.4ms; f_{CP} = 20kHz**



*741 used as a low-pass filter; cut-off frequency = 8kHz.

Figure 7 **Cascade operation of five TDA 1097 delay lines**

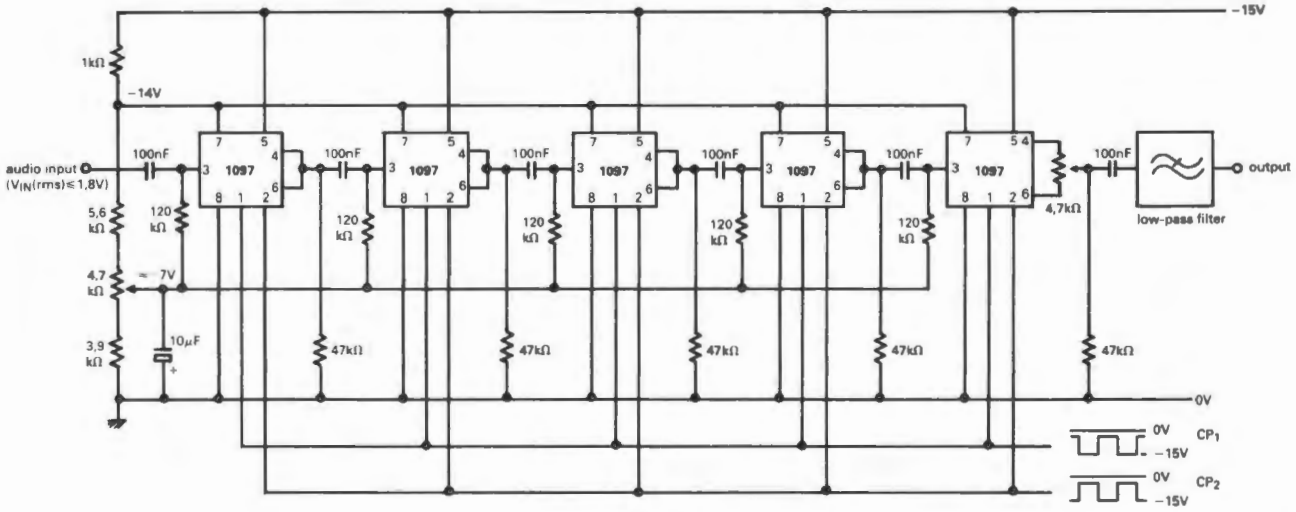
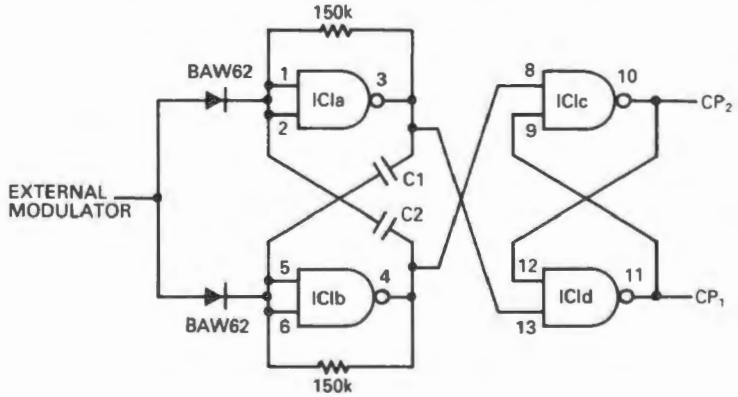
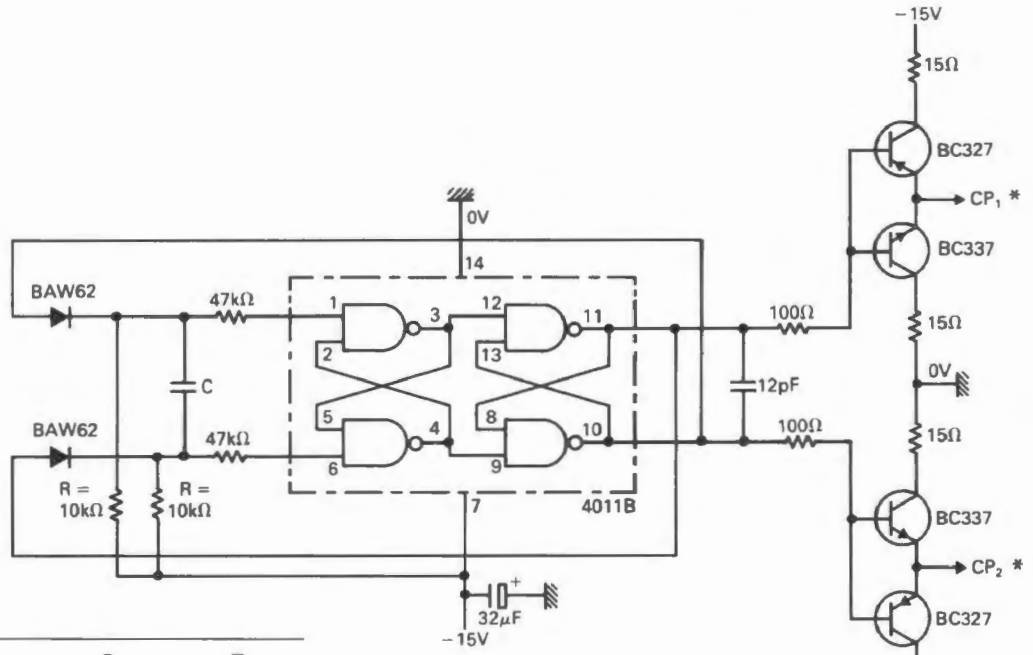


Figure 8 **Clock oscillator which can be modulated by external voltages (eg. for vibrato); using quadruple 2-input NAND gates 4011B (ICIa-d).**



f_{Cp} (kHz)	$C_1 = C_2$ (pF)
15	470
30	220
60	100

Figure 9 **Clock oscillator and driver circuit for up to ten TDA1097 delay lines**



f_{CP} (kHz)	C (pF)	R (kΩ)
5	8400	10
10	3900	10
30	1300	10
100	330	10
300	68	10
500	30	10

* t_r and $t_f < 100$ns.

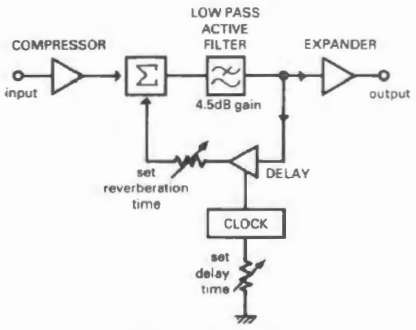
Bucket-brigade line sound enhancement system

In the reproduction of recorded music, one thing is conspicuously missing: no matter how good the recordings or reproduction equipment, the true ambience of 'live' music still cannot be re-created in the home. This is because the original sound would have reached our ears in two ways; direct sound from the instruments and indirect sound reflected from the walls and ceiling of the auditorium. Since the indirect sound travels much further than the direct sound in a large hall, it is considerably delayed and, furthermore, it is reflected many times, each reflection being weaker than its predecessor. In other words, the indirect sound reverberates.

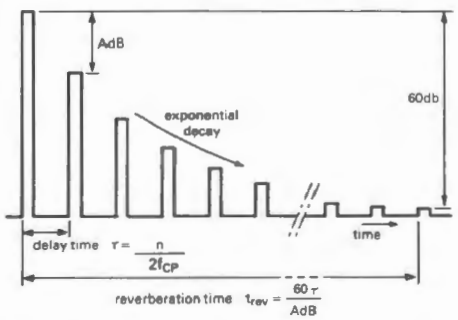
To re-create this effect in the comparatively small home listening room, at least one other loudspeaker must be added and fed with a muted, delayed and slowly decaying version of the signal as fed to the main loudspeakers. Until recently, achievement of the necessary initial delay (up to 300ms) by inexpensive and purely electronic means posed a problem. That problem was solved by the development of integrated charge-transfer devices cascaded to form a 'bucket-brigade' delay line. One of the first of these was the TDA1022 with 512 'buckets', delay up to 25ms and insertion loss of only 4dB. This circuit is mainly intended for creating sound effects for electronic musical instruments.

The TDA 1097 has now been introduced with 1536 'buckets', producing a delay up to 75ms and zero

Figure 10 **Operating principles of the sound enhancement system**



(a) simplified block diagram



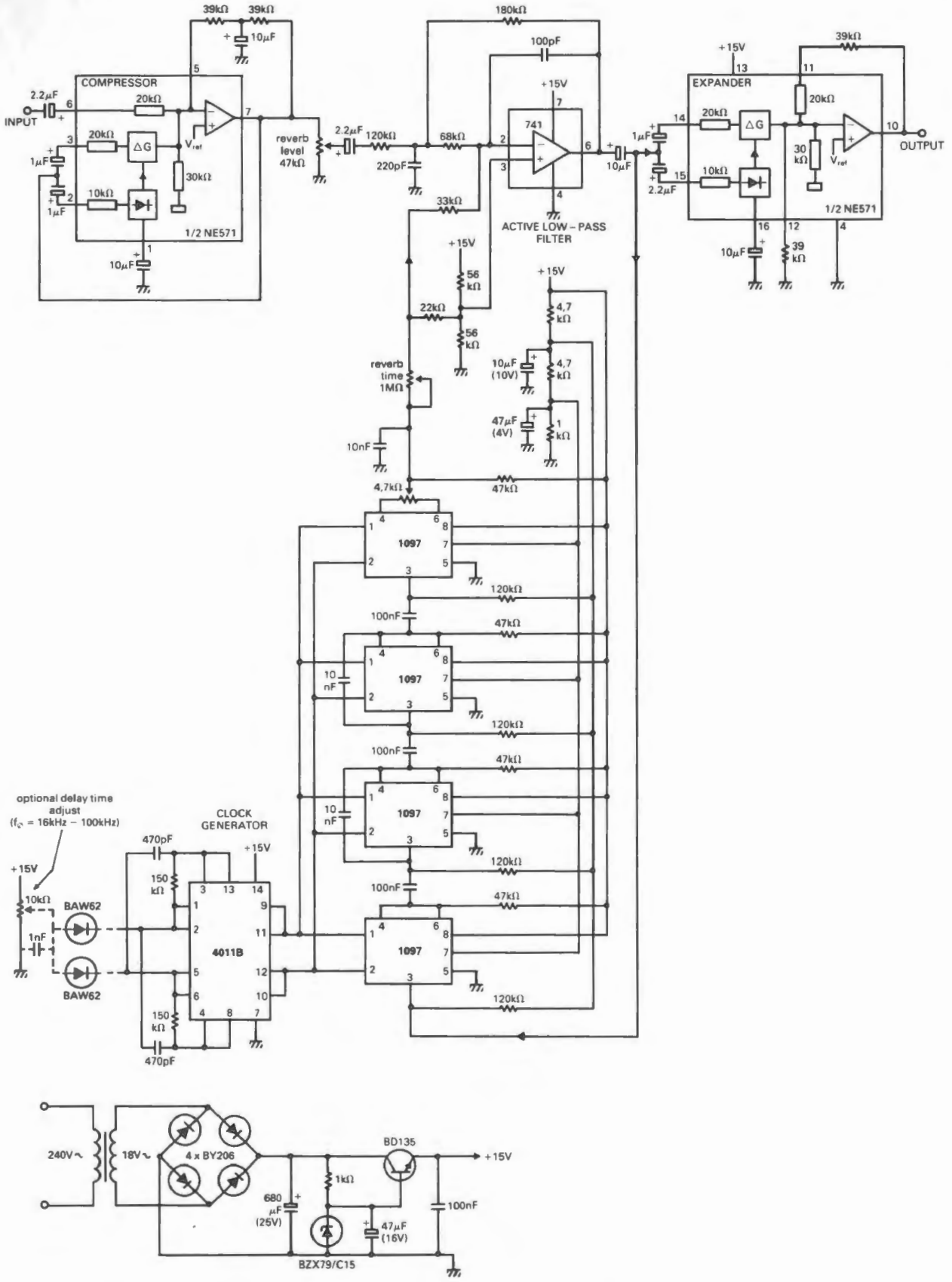
A = closed loop gain of active filter/delay loop in dB
f_{cp} = clock frequency
n = number of 'buckets' in delay chain (1536 per IC)

(b) impulse response

insertion loss. Four of these circuits in cascade form the heart of an add-on listening room expansion system that can bring a new dimension to high-fidelity sound reproduction.

The operating principles of the 'bucket-brigade' are explained earlier in this data sheet and will not be repeated here. The principles of operation of a laboratory model of a listening room expansion system are shown in Figure 10. From the block diagram it can be seen that, if an impulse is applied to the input of the system, it will pass around the delay loop once for each delay period and will be attenuated each time by the closed-loop gain (–3dB or less). Since the delay time π is equal to n/2fø it can be varied by adjusting the clock frequency. The reverberation time (decay time) is inversely proportional to the closed-loop gain and can be varied by adjusting the amount of delayed feedback.

Figure 11 **Sound enhancement system**



RS data

If the fundamental or a harmonic frequency of the incoming signal approaches half the clock frequency, it will be sampled less than twice per cycle and an erroneous lower frequency (alias frequency) signal will appear at the output. It is therefore necessary to restrict the high-frequency response of the reverberation system to not more than half the clock frequency. In practice, it is restricted to one-third of the clock frequency by a low-pass, second-order active filter which also provides about 4.5dB of gain. This bandwidth restriction is of little consequence to the audible results since the higher frequencies in a 'live' listening environment are quickly absorbed and do not therefore reverberate.

A system as shown in Figure 11 would normally exhibit a frequency response like that of a comb filter instead of the desirable all-pass characteristic. This would impart a hollow, reedy or metallic quality to the reverberated sound. The required all-pass characteristic is simulated by applying an additional feedback loop around some of the delay circuits.

The full circuit diagram of one channel of the system is given in Figure 11 and its performance, is given in the table.

There are many ways of adding this variable reverberation system to an existing sound installation. As an example, the system could be entirely separate with its own stereo amplifier and loudspeakers. The level of the reverberated sound should be about half that of that from the main system, and the loudspeakers, which need not have an extended frequency response, should be positioned so that they cannot be heard as identifiable sound sources. The reverberated signals can also of course be applied to the main amplifier and mixed with the normal signals. In this case, separate loudspeakers and amplifier are not necessary.

Performance of the circuit shown in Figure 11

Clock frequency	10kHz	16kHz	100kHz
Delay time	307ms	192ms	31ms
Maximum reverberation time	6s	3.8s	620ms
Delay bandwidth (–3dB)	3kHz	5.3kHz	25kHz
S/N ratio referred to V_O = 1Vrms		>60dB	
THD at V_O = 1Vrms		<1%	
Minimum input voltage		70mVrms	
Maximum output voltage		1Vrms	
Input impedance		20kΩ	
Output impedance		<1kΩ	
Current consumption with V_S = 15V, V_O = 1Vrms		<100mA	

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RS data

Quad 8-bit D to A converter i.c. 7226

Stock number 300-388

The RS7226 contains four 8-bit voltage-output digital-to-analogue converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external adjustments are required to achieve full specified performance for the device.

Separate on-chip latches are provided for each of the four D/A converters. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Control inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. The control logic is speed-compatible with most 8-bit microprocessors.

Each D/A converter includes an output buffer amplifier capable of driving up to 5mA of output current. The amplifiers' offsets are laser-trimmed during manufacture, thereby eliminating any requirement for offset nulling.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V with dual supplies. The part is also specified for single supply operation at a reference of +10V.

Absolute Maximum Ratings

V_{DD} to analogue or digital ground	−0.3V to +17V
V_{SS} to analogue or digital ground	−7V to V_{DD}
V_{DD} to V_{SS}	−0.3V to +24V
Analogue ground to digital ground	−0.3V to V_{DD}
Digital input voltage to digital ground	−0.3V to V_{DD}
V_{REF} to Analogue ground	−0.3V to V_{DD}
V_{OUT} to Analogue ground	V_{SS} to V_{DD}
Power dissipation	500mW
Operating temperature range	0 to +70°C
Storage temperature range	−65 to +150°C
Lead temperature soldering 10s	+300°C

WARNING!

ESD SENSITIVE DEVICE

CAUTION
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Features

- Four 8-bit converters with output amplifiers
- Compact 0.3in wide 20-pin DIL package
- Microprocessor compatible
- TTL and CMOS compatible
- No user adjustments required
- Single supply operation is possible.

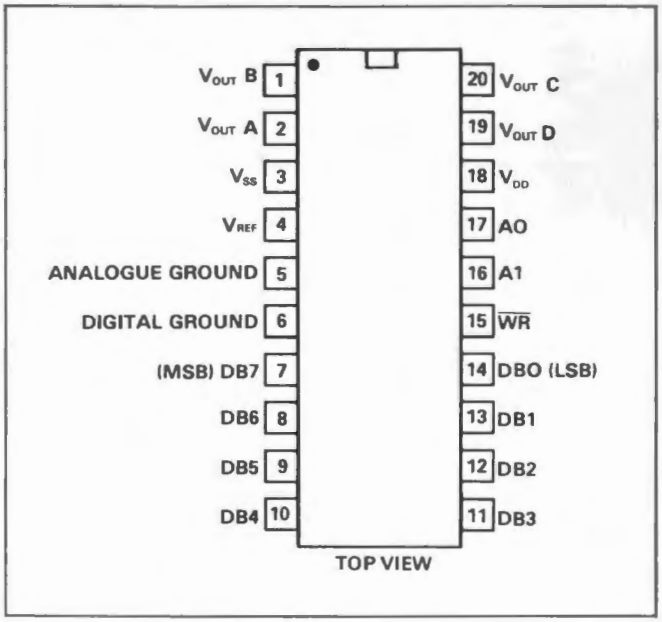
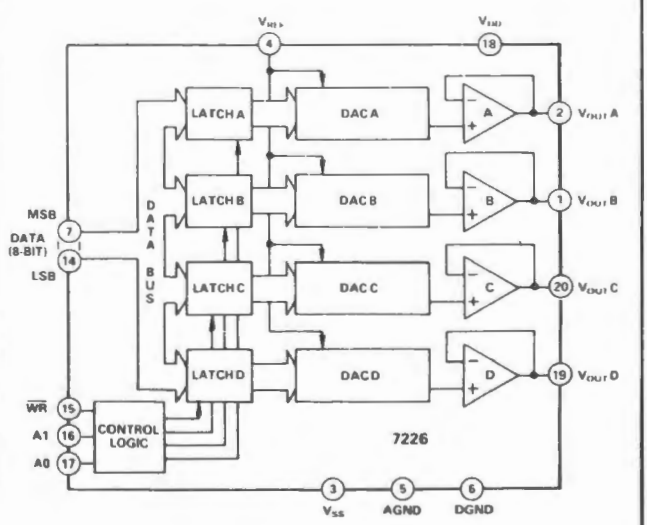


Figure 1 **Block diagram**



Electrical characteristics dual supply specification

V_{DD} = 11.4V to 16.5V; V_{SS} = –5V ±10%; AGND = DGND = 0V; V_{REF} = 2V to (V_{DD} –4V); T_A = 0 to +70°C

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} range		11.4		16.5	V
I_{DD}	Outputs unloaded			12	mA
I_{SS}	Outputs unloaded			9	mA
Resolution			8		Bits
Total unadjusted error	V_{DD} = +15V ±5%, V_{REF} = +10V			±2	LSB
Relative accuracy				±1	LSB
Differential nonlinearity	Guaranteed monotonic			±1	LSB
Full scale error				±1½	LSB
Full scale temperature coefficient	V_{DD} = 14V to 16.5V, V_{REF} = +10V		±20		ppm/°C
Zero code error				±30	mV
Zero code error temp. coefficient			±50		μV/°C
Reference input voltage range		2		(V_{DD}-4)	V
Reference input resistance		2			kΩ
Reference input capacitance[1]	Each DAC loaded with all 0s Each DAC loaded with all 1s	65		 300	pF pF
Digital inputs: Input high voltage, V_{INH} Input low voltage, V_{INL} Input leakage current Input capacitance[1] Input coding	V_{IN} = 0V or V_{DD}	 2.4 –	 BINARY	 0.8 ±1 8 –	 V V μA pF
Voltage output slew rate[2]		2.5			V/μs
Voltage output setting time[2] Positive full scale change Negative full scale change	 V_{REF} = +10V; setting time to ±½LSB V_{REF} = +10V; setting time to ±½LSB			 5 7	 μs μs
Digital crosstalk			50		nVsecs
Minimum load resistance	V_{OUT} = +10V	2			kΩ

Electrical characteristics single supply specification

V_{DD} = +15V±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; T_A 0 to +70°C

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} range	For specified performance	14.25		15.75	V
I_{DD}	Outputs unloaded; V_{IN} = V_{INL} or V_{INH}			12	mA
Resolution			8		Bits
Total unadjusted error				±2	LSB
Differential nonlinearity	Guaranteed monotonic			±1	LSB
Reference input resistance		2			kΩ
Reference input capacitance[1]	Each DAC loaded with all 0s Each DAC loaded with all 1s	65		 300	pF pF
Digital inputs: Input high voltage V_{INH} Input low voltage V_{INL} Input leakage current Input capacitance[1] Input coding	V_{IN} = 0V or V_{DD}	 2.4 –	 BINARY	 0.8 ±1 8 –	 V V μA pF
Voltage output slew rate[2]		2			V/μs
Voltage output setting time:[2] Positive full scale change Negative full scale change	 Setting time to ±½LSB Setting time to ±½LSB			 5 20	 μs μs
Digital crosstalk			50		nV secs
Minimum load resistance	V_{OUT} = +10V	2		kΩ	

Notes:
1. Guaranteed by design, not production tested.
2. Sample tested at 25°C to ensure compliance.

Switching characteristics

Single and dual supply operation $T_A = 25°C$. Where figure varies 0° to +70°C in brackets.

Parameter	Symbol	Min.	Typ.	Max.	Units
Address to write setup time	t_{AS}	0			ns
Address to write hold time	t_{AH}	10			ns
Data valid to write setup time	T_{DS}	90(100)			ns
Data valid to write hold time	T_{DH}	10			ns
Write pulse width	t_{WR}	150(200)			ns

Description of parameters

Total unadjusted error
This is a comprehensive specification which includes full scale error, relative accuracy and zero code error. Absolute full scale is $V_{REF} - 1$ LSB (ideal), where 1 LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the offset will, relative to the LSB size, increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the offset, will also vary in terms of LSBs over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10V.

Relative accuracy
Relative accuracy or end-point nonlinearity, is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

Differential nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

Digital crosstalk
The glitch impulse transferred to the output of one converter due to a change in the digital input code to another of the converters. It is specified in nV secs and is measured at $V_{REF} = 0V$.

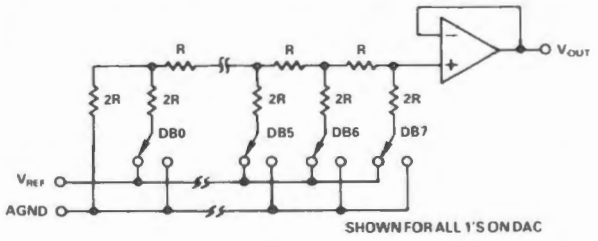
Full scale error
Full scale error is defined as:
Measured value – zero code error – ideal value.

Circuit information

D/A section
The 7226 contains four, identical, 8-bit, voltage-mode digital-to-analogue converters. The output voltages from the converters have the same polarity as the reference voltage allowing single supply operation. A novel DAC switch pair arrangement on the 7226 allows a reference voltage range from +2V to +12.5V.

Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high speed NMOS, single-pole, double-throw switches. The simplified circuit diagram for one channel is shown in Figure 2. Note that V_{REF} (pin 4) and AGND (pin 5) are common to all four DACs.

Figure 2 **D/A simplified circuit diagram**



The input impedance at the V_{REF} pin of the 7226 is the parallel combination of the four individual DAC reference input impedances. It is code dependent and can vary from 2kΩ to infinity. The lowest input impedance (ie., 2kΩ) occurs when all four DACs are loaded with the digital code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminal is also code dependent and typically varies from 100pF to 250pF.

Each V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage of:

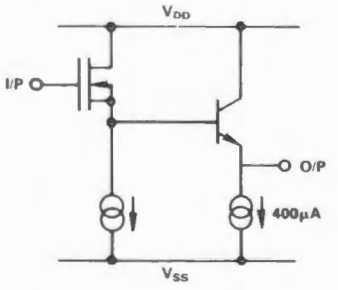
$$V_{OUTX} = D_X V_{REF}$$

where D_X is a fractional representation of the digital input code and can vary from 0 to 255/256.

The source impedance is the output resistance of the buffer amplifier.

Op-amp section
Each voltage-mode D/A converter output is buffered by a unity gain, noninverting CMOS amplifier. This buffer amplifier is capable of developing +10V across a 2kΩ load and can drive capacitive loads of 3300pF. The output stage of this amplifier consists of a bipolar transistor from the V_{DD} line and a current load to V_{SS}, the negative supply for the output amplifiers. This output stage is shown in Figure 3.

Figure 3 **Amplifier output stage**

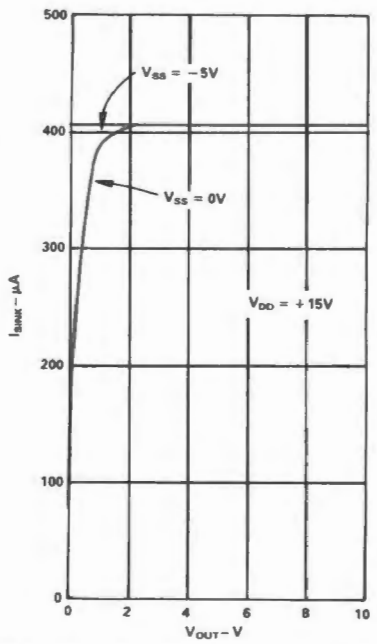


The NPN transistor supplies the required output current drive (up to 5mA). The current load consists of NMOS transistors which normally act as a current sink of 400μA to V_{SS}, giving each output a current sink capability of approximately 400μA if required.

The 7226 can be operated as a single supply or dual supply resulting in different performance in some parameters from the output amplifiers.

In single supply operation (V_{SS} = 0V = AGND), with the output approaching AGND (ie., digital code approaching all 0s) the current load ceases to act as a current sink and begins to act as a resistive load of approximately 2kΩ to AGND. This occurs as the NMOS transistors come out of saturation. This means that, in single supply operation, the sink capability of the amplifiers is reduced when the output voltage is at or near AGND. A typical plot of the variation of current sink capability with output voltage is shown in Figure 4.

Figure 4 **Variation of I_{SINK} with V_{OUT}**



If the full sink capability is required with output voltages at or near AGND (= 0V), then V_{SS} can be brought below 0V by 5V and thereby maintain the 400μA current sink as indicated in Figure 4. Biasing V_{SS} below 0V also gives additional headroom in the output amplifier which allows for better zero code error performance on each output. Also improved is the slew-rate and the negative-going settling-time of the amplifiers (discussed later).

Each amplifier offset is laser trimmed during manufacture to eliminate any requirement for offset nulling.

Digital section

The digital inputs of the 7226 are both TTL and CMOS (5V) compatible from V_{DD} = +11.4V to +16.5V. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimise power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

Interface logic information

Address lines A0 and A1 select which DAC will accept data from the input port. Table I shows the the selection table for the four DACs with Figure 5 showing the input control logic. When the $\overline{WR}$ signal is LOW, the input latches of the selected DAC are transparent and its output responds to activity on the data bus. The data is latched into the addressed DAC latch on the riding edge of $\overline{WR}$. While $\overline{WR}$ is high the analogue outputs remain at the value corresponding to the data held in the respective latches.

Table I **7226 Truth Table**

7226 Control inputs			7226
WR	**A1**	**A0**	**Operation**
H	X	X	No Operation Device Not Selected
L	L	L	DAC A Transparent
↓	L	L	DAC A Latched
L	L	H	DAC B Transparent
↓	L	H	DAC B Latched
L	H	L	DAC C Transparent
↓	H	L	DAC C Latched
L	H	H	DAC D Transparent
↓	H	H	DAC D Latched

L = Low State, H = High State, X = Don't Care

Figure 5 **Input control logic**

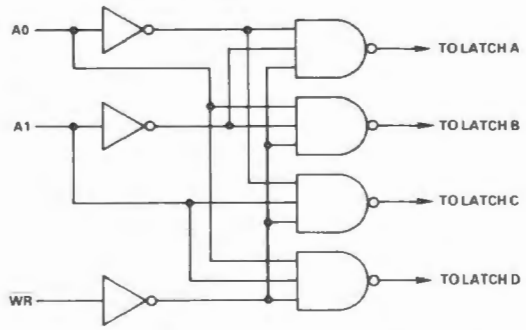
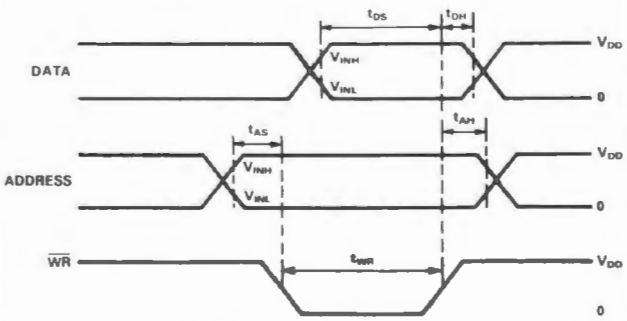


Figure 6 **Write cycle timing diagram**



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% of V_{DD}
   $t_r = t_f$ = 20ns OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS
   $\frac{V_{INH} + V_{INL}}{2}$
3. SELECTED INPUT LATCH IS TRANSPARENT WHILE $\overline{WR}$ IS LOW, THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS

Typical performance characteristics

Figure 7 **Channel-to-channel matching**

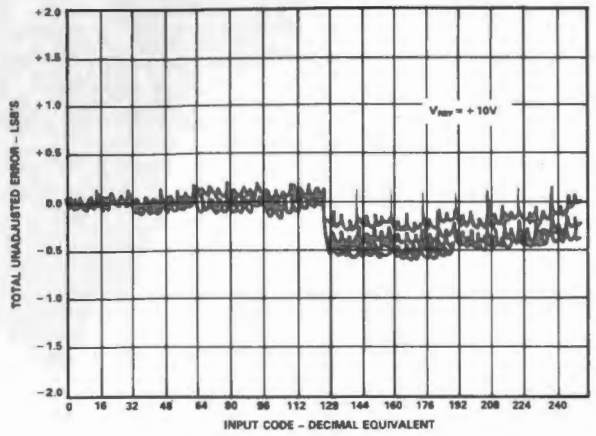


Figure 8 **Relative accuracy vs. V_{REF}**

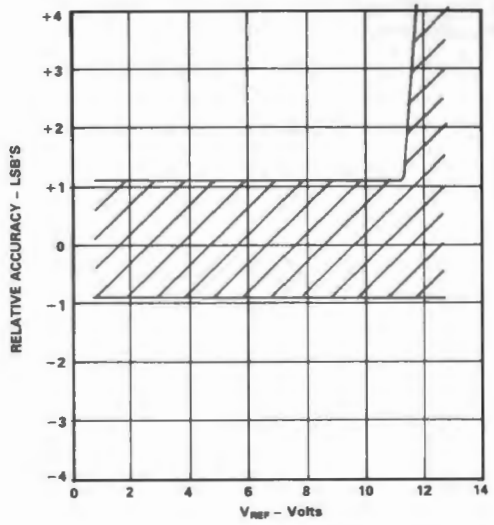


Figure 9 **Differential nonlinearity vs. V_{REF}**

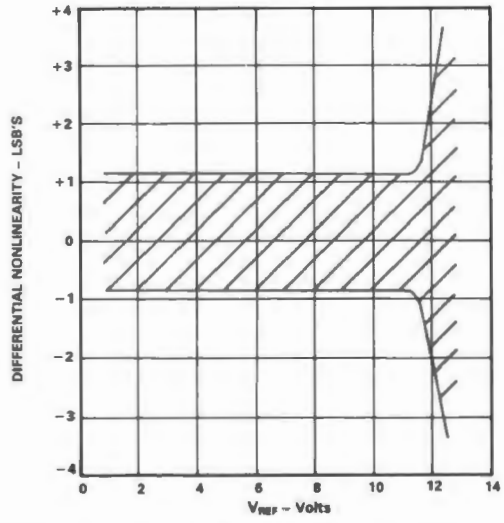
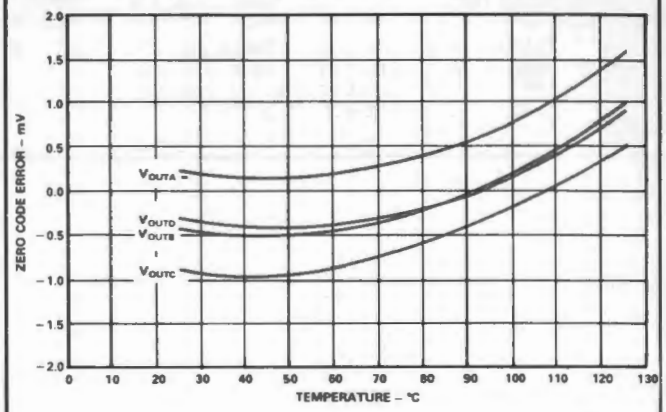


Figure 10 **Zero code error vs. temperature**



Specification ranges

In order for the DACs to operate to their specifications, the reference voltage must be at least 4V below the V_{DD} power supply voltage. This voltage differential is required for correct generation of bias voltages for the DAC switches.

The 7226 is specified to operate over a V_{DD} range from +12V ±5% to +15V ±10% (ie., from 11.4V to +16.5V) with a V_{SS} of –5V ±10%. Operation is also specified for a single +15V ±5% V_{DD} supply. Applying a V_{SS} of –5V results in improved zero code error, improved output sink capability with outputs near AGND, and improved negative-going settling-time.

Performance is specified over a wide range of reference voltages from 2V to (V_{DD} –4V) with dual supplies. This allows a range of standard reference generators to be used. Note that in order to achieve an output voltage range of 0V to +10V, a nominal +15 ±5% power supply voltage is required by the 7226.

Figure 11 **Dynamic response (V_{SS} = –5V)**

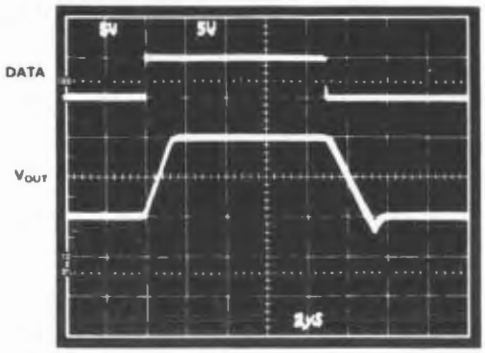


Figure 12a **Positive-step settling-time (V_{SS} = –5V)**

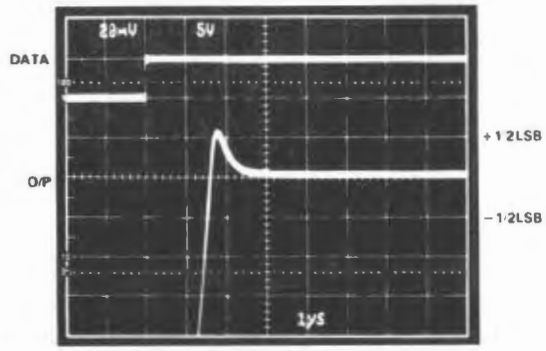
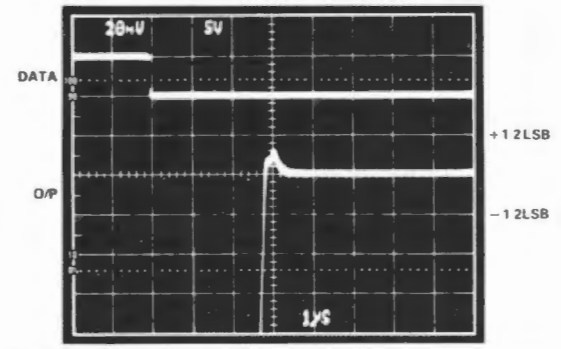


Figure 12b **Negative-step settling-time (V_{SS} = –5V)**



Settling time

The output stage of the buffer amplifiers consists of a bipolar NPN transistor from the V_{DD} line and a constant current load to V_{SS}. V_{SS} is the negative power supply for the output buffer amplifiers. As mentioned in the op-amp section, in single supply operation the NMOS transistor will come out of saturation as the output voltage approaches AGND and will act as a resistive load of approximately 2kΩ to AGND. As a result, the settling-time for negative-going signals approaching AGND in single supply operation will be longer than for dual supply operation where the current load of 400μA is maintained all the way down to AGND. Positive-going settling-time is not affected by V_{SS}.

The settling-time for the 7226 is limited by the slew-rate of the output buffer amplifiers. This can be seen from Figure 11 which shows the dynamic response for the 7226 for a full scale change. Figures 12a and 12b show expanded settling-time photographs with the output waveforms derived from a differential input to an oscilloscope. Figure 12a shows the settling-time for a positive-going step and Figure 12b shows the settling-time for a negative-going output step.

Ground management

AC or transient voltages between AGND and DGND can cause noise at the analogue output. This is especially true in microprocessor systems where digital noise is prevalent. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the 7226. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the 7226 AGND and DGND pins (IN4148 or equivalent).

Unipolar output operation

This is the basic mode of operation for each channel of the 7226, with the output voltages having the same positive polarity as + V_{REF}. The 7226 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). The code table for unipolar output operation is shown in Table II. Note that the voltage at V_{REF} must never be negative with respect to DGND in order to prevent parasitic transistor turn-on. Connections for the unipolar output operation are shown in Figure 13.

Figure 13 **Unipolar output circuit**

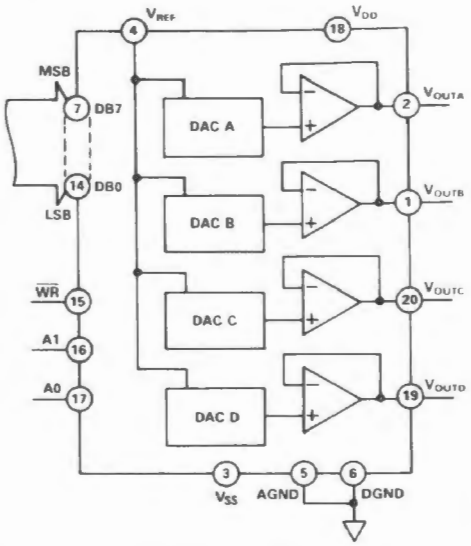


Table II **Unipolar code table**

DAC Latch Contents MSB	LSB	Analogue output
1111	1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000	0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000	0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111	1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000	0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000	0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Bipolar output operation

Each of the DACs of the 7226 can be individually configured to provide bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 14 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the 7226. In this case

$$V_{OUT} = \left(1+\left(\frac{R2}{R1}\right)\right) \times (D_A V_{REF}) - \left(\frac{R2}{R1}\right) \times (V_{REF}).$$

With R1 = R2

$$V_{OUT} = (2D_A - 1) \cdot V_{REF}$$

where D_A is a fractional representation of the digital word in latch A.

Mismatch between R1 and R2 causes gain and offset errors and therefore these resistors must match and track over temperature. Once again the 7226 can be operated in single supply or from positive/negative supplies. Table III shows the digital code versus output voltage relationship for the circuit in Figure 14 with R1 = R2.

Figure 14 **7226 Bipolar output circuit**

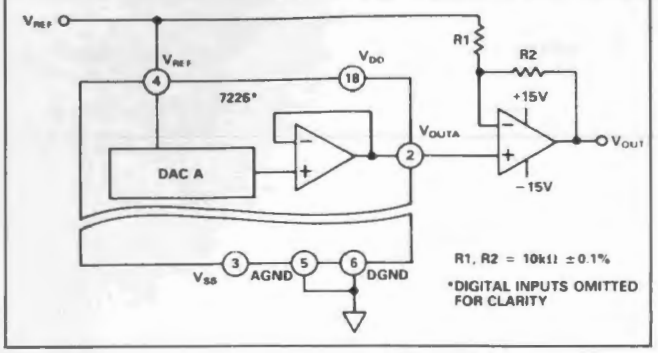
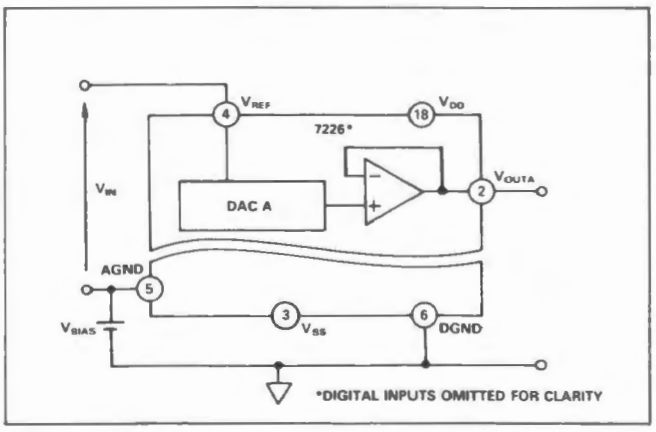


Table III **Bipolar (Offset Binary) Code Table**

DAC Latch Contents MSB	LSB	Analogue output
1111	1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000	0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000	0000	0V
0111	1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000	0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000	0000	$V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

AGND bias

The 7226 AGND pin can be biased above system GND (7226 DGND) to provide an offset 'zero' analogue output voltage level. Figure 15 shows a circuit configuration to achieve this for channel A of



the 7226. The output voltage, V_{OUTA}, can be expressed as:

$$V_{OUTA} = V_{BIAS} + D_A (V_{IN})$$

where D_A is a fractional representation of the digital input word ($0 \leq D \leq 255/256$).

For a given V_{IN}, increasing AGND above system GND will reduce the effective $V_{DD}-V_{REF}$ which must be at least 4V to ensure specified operation. Note that because the AGND pin is common to all four DACs, this method biases up the output voltages of all the DACs in the 7226. Note that V_{DD} and V_{SS} for the 7226 should be referenced to DGND.

3-Phase sine wave

The circuit of Figure 16 shows an application of the 7226 in the generation of 3-phase sine waves which can be used to control small 3-phase motors. The proper codes for synthesising a full sine wave are stored in EPROM, with the required phase-shift of 120° between the three D/A converter outputs being generated in software.

Data is loaded into the three D/A converters from the sine EPROM via the microprocessor or control logic. Three loops are generated in software with each D/A converter being loaded from a separate loop. The loops run through the look-up table producing successive triads of sinusoidal values with 120° separation which are loaded to the D/A converters producing 3 sine wave voltages 120° apart. A complete sine wave cycle is generated by stepping through the full look-up table. If a 256-element sine wave table is used then the resolution of the circuit will be 1.4° (360°/256). Figure 18 shows typical resulting waveforms. The sine waves can be smoothed by filtering the D/A converter outputs.

The fourth D/A converter of the 7226, DAC D, may be used in a feedback configuration to provide a programmable reference voltage for itself and the other three converters. This configuration is shown in Figure 16. The relationship of V_{REF} to V_{IN} is dependent upon digital code and upon the ratio of R_F to R and is given by the formula

$$V_{REF} = \frac{(1+G)}{(1+G.D_D)} \times V_{IN}$$

where $G = R_F/R$

and D_D is a fractional representation of the digital word in latch D.

Alternatively, for a given V_{IN} and resistance ratio, the required value of D_D for a given value of V_{REF} can be determined from the expression

$$D_D = (1 + R/R_F) \times \frac{V_{IN}}{V_{REF}} - \frac{R}{R_F}$$

Figure 17 shows typical plots of V_{REF} versus digital code for three different values of R_F. With V_{IN} = +2.5V and R_F = 3R the peak-to-peak sine wave voltage from the converter outputs will vary between +2.5V and +10V over the digital input code range of 0 to 255.

Figure 16 **3-phase sine wave generation circuit**

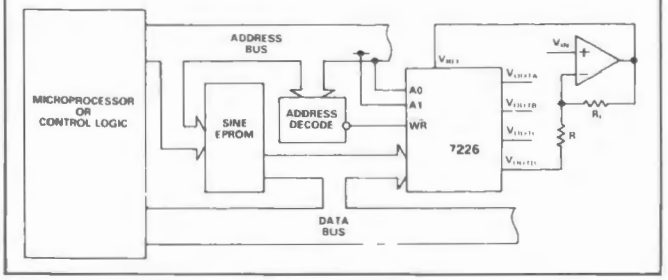


Figure 17 **Variation of V_{REF} with feedback configuration**

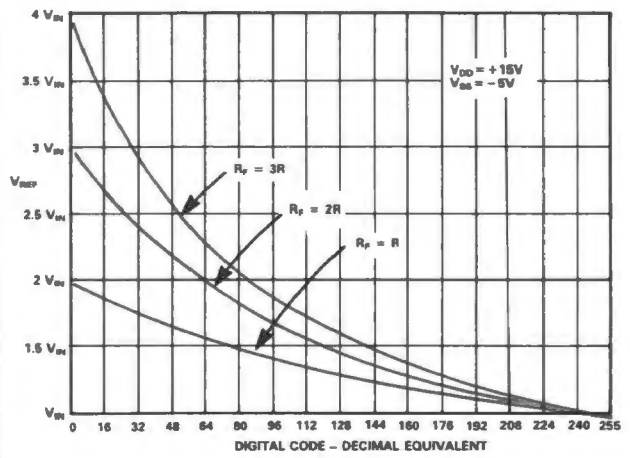
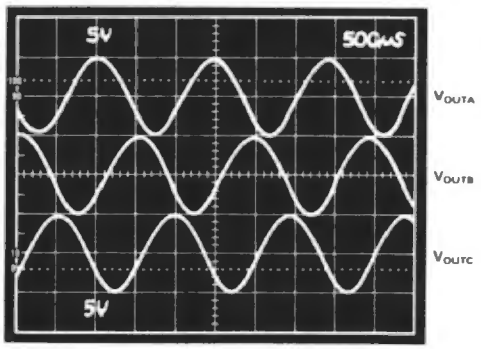


Figure 18 **3-phase sine wave output**



Staircase window comparator

In many test systems, it is important to be able to determine whether some parameter lies within defined limits. The staircase window comparator of Figure 19a is a circuit which can be used, for example, to measure the V_{OH} and V_{OL} thresholds of a TTL device under test. Upper and lower limits on both V_{OH} and V_{OL} can be programmably set using the 7226. Each adjacent pair of comparators forms a window of programmable size. If V_{TEST} lies within a window then the output for that window will be high. With a reference of 2.56V applied to the V_{REF} input, the minimum window size is 10mV.

The circuit can easily be adapted to allow for overlapping of windows as shown in Figure 20a. If the three outputs from this circuit are decoded then five different nonoverlapping programmable windows can again be defined.

Figure 19a **Logic level measurement**

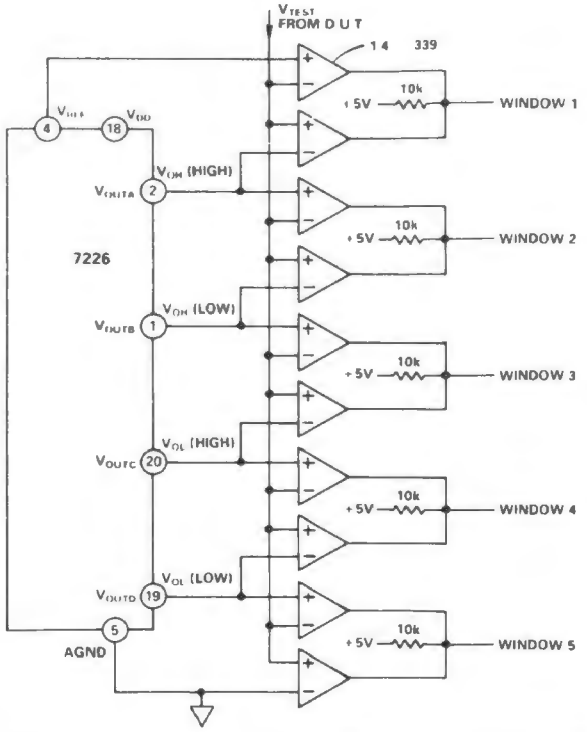


Figure 19b **Window structure**

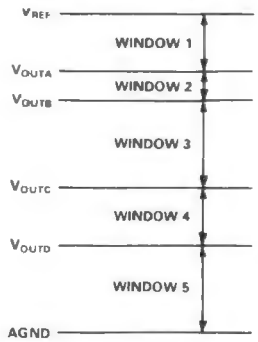


Figure 20a **Overlapping windows**

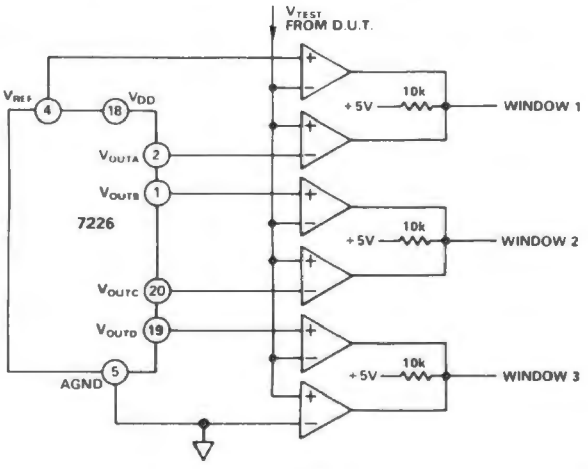


Figure 20b **Window structure**

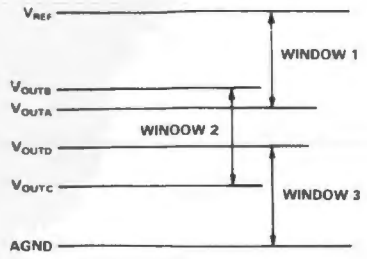
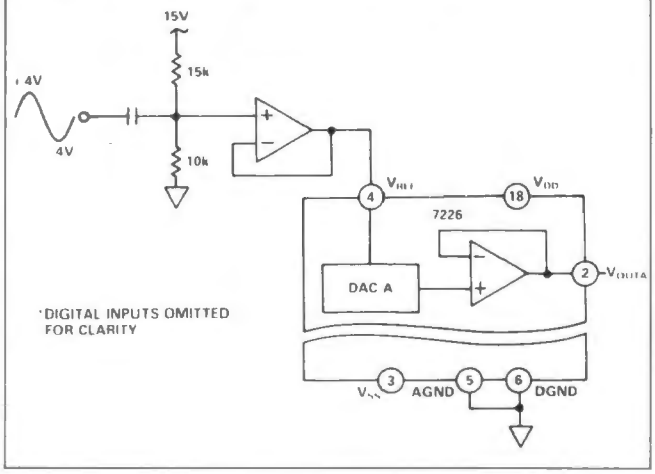


Figure 21 **Varying reference signal**



Varying reference signal

In some applications, it may be desirable to have a varying signal applied to the reference input of the 7226. The 7226 has multiplying capability within upper and lower limits of reference voltage when operated with dual supplies. The upper and lower limits are those required by the 7226 to achieve its linearity specification. Figure 21 shows a sine wave signal applied to the reference input of the 7226. For input signal frequencies up to 50kHz the output distortion typically remains less than 0.1%. Typical 3dB bandwidth figure is 700kHz.

Microprocessor interfaces

Figure 22 **7226 to 8085A interface**

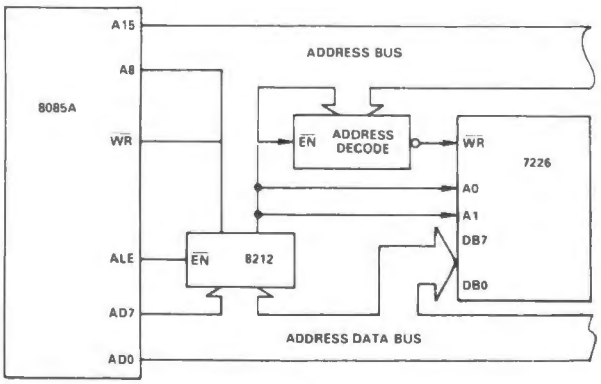


Figure 23 **7226 to 6809 interface**

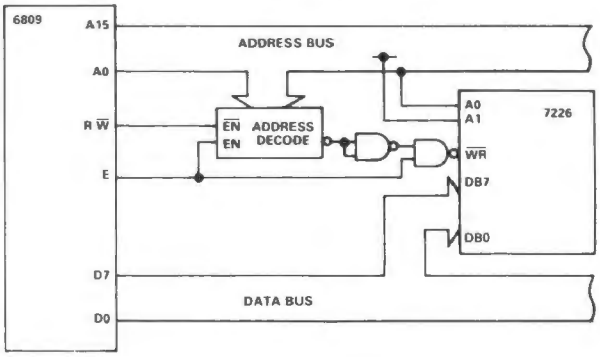


Figure 24 **7226 to 6502 interface**

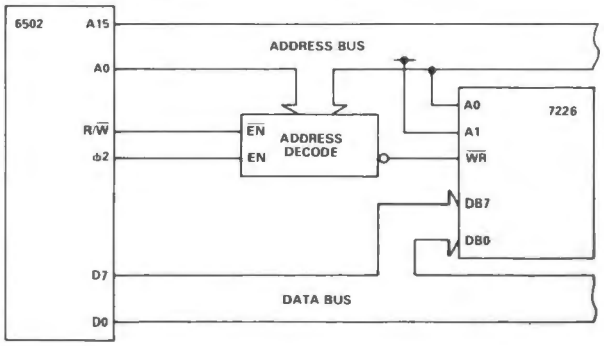
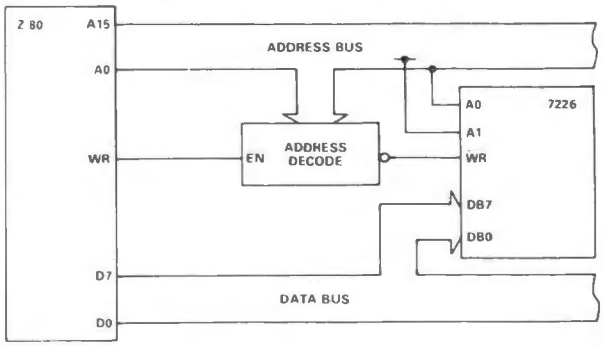


Figure 25 **7226 to Z 80 interface**



RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company

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RS data

Sensing relays

The sensing relays act as threshold detectors for voltage, current or resistance values as appropriate. The state of the output relay (ie. ON or OFF) depends on whether the value of the variable (voltage, current or resistance) is above or below the value set by the front panel on the relay body.

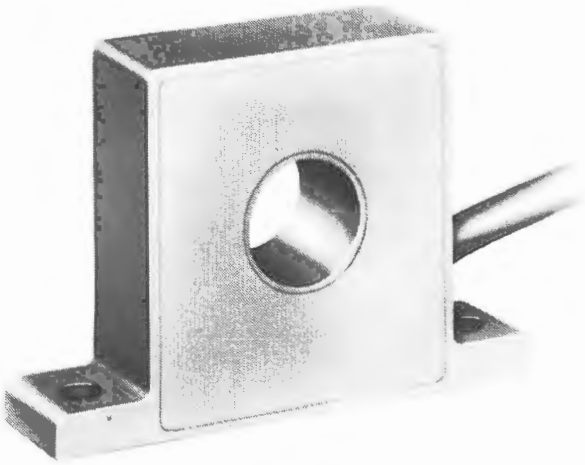
Features

- Voltage, current and resistance versions available
- Ideal for process control and monitoring systems
- Relays utilise standard 11 pin plug-in bases or may be panel mounted

Sensing relay range

Type	Supply voltage	Sensing range	Stock number
Voltage sensing relay	240V AC 240V AC 120V AC 120V AC	2 to 20V 50 to 500V 2 to 20V 50 to 500V	349-816 348-605 346-154 346-160
Current sensing relay	240V AC 120V AC	See text See text	349-800 346-176
Current transformer	– –	0.5 to 5A 2 to 20A	346-182 346-198
Resistance sensing relay	240V AC	50 to 5000Ω	349-822

Sensing relay
(Shown with panel mounting bezel)



Current transformer

Technical specifications (relays)

Supply voltage
120V types ____ 120V AC ±10% 45-60Hz
240V types ____ 240V AC ± 6% 45-60Hz
Power consumption ____ 2.5VA typ.
Relay contact ratings ____ 380V AC 10A 2500VA
(Resistive load) ____ 250V DC 1A 250W
25V DC 10A 250W
Contact isolation ____ Test voltage 2000V AC
Ambient temp range ____ Operating –20°C to +50°C
Storage –50°C to +85°C
Mechanical life (relay) ____ 3×10^7 operations
Electrical life ____ 2.5×10^5 operations
Operating rate (max)
7200 (resistance type, 3600) ops/hour

Front panel scale

Dial calibration markings are nominal, for accurate level setting use external calibration standards. Dial range is linear and for current sensing it corresponds to a linear input voltage of 0.1 – 4V.

Current and voltage sensing relay operation

The relay will energise when the sense voltage or current reaches the value set by the front panel control. The relay will release when the level falls by more than 10% of the 'energise' level, or when the supply is removed. This hysteresis can be increased to approximately 75% by connecting resistance between pins 8 and 9, range 1MΩ to 15kΩ (hysteresis increases as resistance falls). The relay will latch on if these pins are directly linked.

Figure 1 **Pin connections**

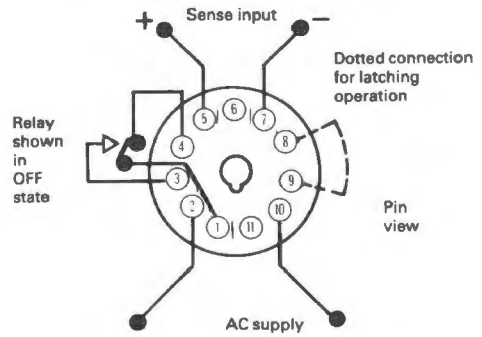
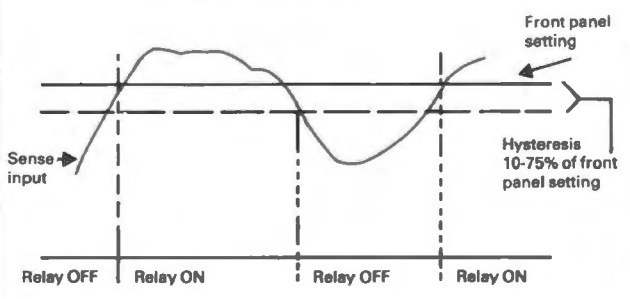


Figure 2 **Output hysteresis**



Voltage sensing relays	**346-154, 349-816**	**346-160, 348-605**
Sense input range	2–20V AC (peak)/DC	50–500V AC (peak)/DC
Input resistance	50kΩ	1MΩ
Absolute max. input voltage	100V	500V

Current sensing relays 346-176, 349-800

Current sensing is achieved using a sensing relay together with a single external resistor or a current transformer.

1. External resistor method (for DC/AC (peak) current sensing).

The relay measures the voltage produced by passing the sense current through a fixed resistor. The resistor value R is calculated as shown:

$$R = \frac{V}{I}$$

Where I is the current level to be detected and V is the voltage corresponding to the front panel control setting position required (eg. 2V for centre reading).

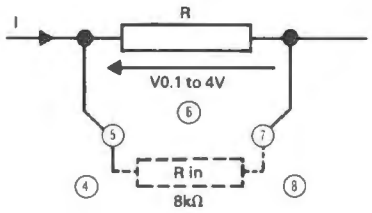
If the current to be detected is 10mA or less the internal resistance of the sense input should be taken into account (R in = 8kΩ), and R is calculated as below:

$$R = \frac{V \times 8000}{(I \times 8000) - V}$$

Sense input range ____ 0.1 to 4V AC (peak)/DC
Maximum input voltage ____ 20V
(Pin 5 positive with respect to Pin 7)

2. Current transformer method (for AC current sensing) – see current transformers.

Figure 3 **Connection method for DC/AC (peak) current sensing**



Current transformers 346-182, 346-198

Technical specifications	**346-182**	**346-198**
Current range through centre conductor	0.5–5A rms	2–20A rms
Output voltage	0.1-4V	0.1–4V
Max. Current (peak)	20A	50A
Output resistance	700Ω	200Ω
Ambient temperature	–20°C to +60°C	

The transformer output voltage is proportional to the AC current in the conductor through the centre hole. The measuring range of the transformer may be proportionately reduced by drawing the current carrying conductor through the centre hole (in the same direction) more than once eg. 5 times results in a measuring range for the 0.5–5A transformer of 0.1 – 1A rms.

Figure 4 **AC current sensing using current transformer**

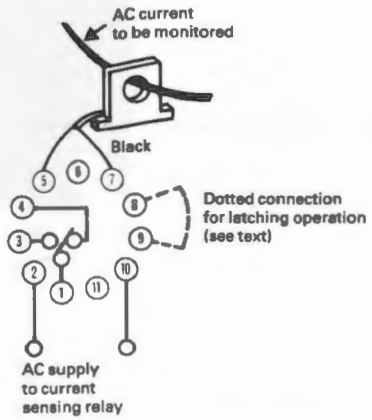
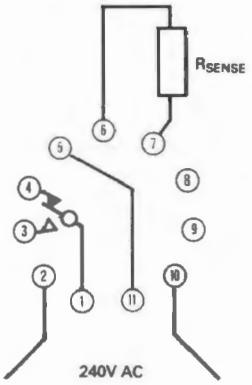


Figure 6 **Under-resistance sensing**



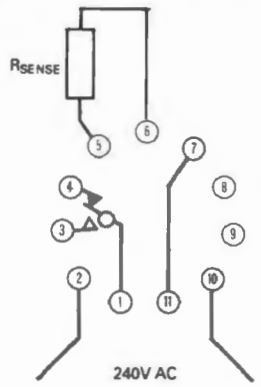
Resistance sensing relay 349-822

With the circuit connected as in Figure 5 the relay will be energised when the external resistance to be sensed (R sense) is greater than the value set by the front panel control.

With the circuit connected as in Figure 6 the relay will be energised when the external resistance to be sensed (R sense) is less than the value set by the front panel control.

Sense input range ——— 50 to 5000Ω
Measuring voltage source
(Pin 5 is +ve, Pin 7 is –ve) ——— 1.4V DC
Hysteresis ——— <1%
Maximum operating rate ——— 1Hz

Figure 5 **Over-resistance sensing**



RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

Stepper motors

7.5° Types 332-947 and 332-953
1.8° Type 332-082
Stepper motor drive board 332-098

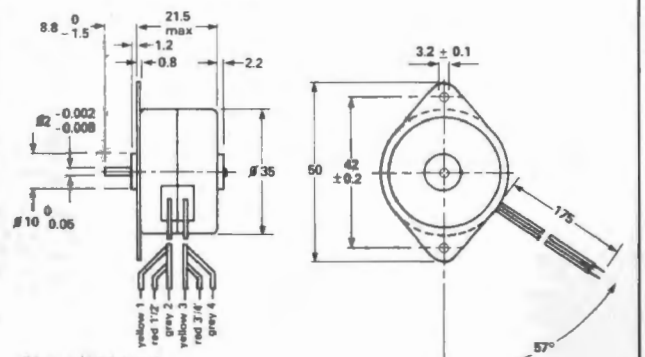
7.5° Stepper motors size 1 (332-947) and size 2 (332-953)

Two 7.5° stepper motors each with four 12V dc windings (coils) and permanent magnet rotor construction. Designed for unipolar drive, these motors are easily interfaced to simple and relatively low power electronics thus providing economical means of motion and speed control. Due to their permanent magnet rotors these motors have a braking torque even when not energised. This is the detent (residual) torque which is a useful feature for positional integrity.

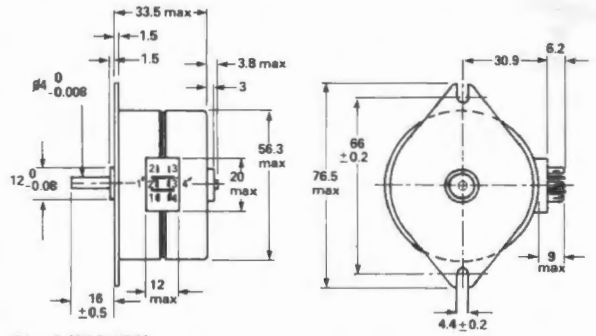
The size 1 motor is ideal for applications requiring low torque drive but it can also be used with the RS range of synchronous gearboxes (336-400 etc.) to provide finer step angle and increased torque at lower speeds.

The size 2 motor is a more powerful general purpose motor ideally suited for direct drive applications.

7.5° Stepper motors



Size 1 (332-947)



Size 2 (332-953)

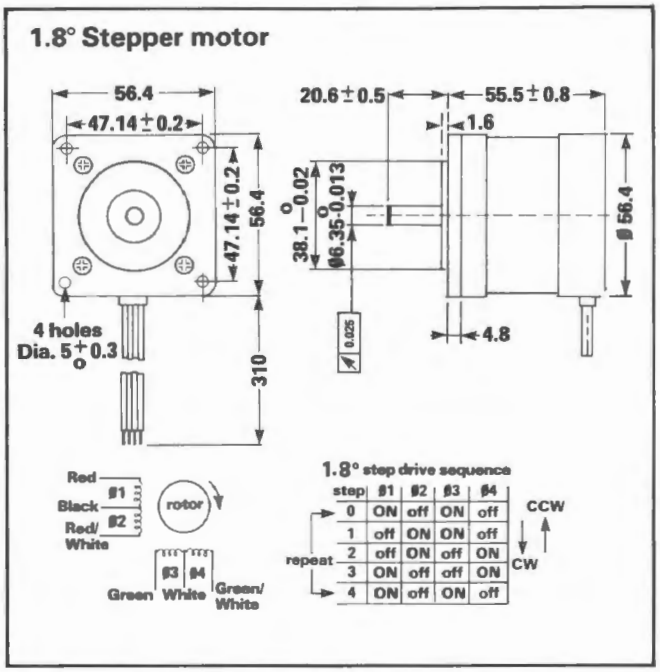
Technical specification

	Size 1	Size 2	Units
Power consumption of motor only	2	5.3	W
Maximum working torque	6	57	mNm
Holding torque	10	85	mNm
Torque derating	–0.4	–0.4	%/°C
Maximum pull-in rate	350	130	steps/s
Resistance per phase at +20°C	120	47	Ω
Inductance per phase	160	400	mH
Current per phase	100	240	mA
Permissible ambient temperature range	–20 to +70	–20 to +70	°C
Permissible storage temperature range	–40 to +100	–40 to +100	°C
Permissible motor temperature	120	120	°C
Insulation resistance at 500V (CEE 10)	>2	>2	MΩ
Step angle	7° 30′	7° 30′	
Step angle tolerance, not cumulative	±40′	±20′	
Number of steps per revolution	48	48	
Direction of rotation	reversible	reversible	
Rotor inertia	2.6	45	gcm^2

	Size 1	Size 2	Units
Mass	80	300	g
Maximum radial force	2.5	10	N
Maximum axial force	0.75	1.5	N
Bearings	slide (bronze)	slide (sintered bronze)	

1.8° Stepper motor (332-082)

This 4-phase hybrid stepper motor is capable of delivering much higher working torque and stepping rates than the 7.5° permanent magnet types while at the same time maintaining a high detent torque even when not energised. This feature is particularly important for positioning integrity. The motor is directly compatible with the RS stepper motor drive board 332-098 (see motor drive methods).



Technical specification

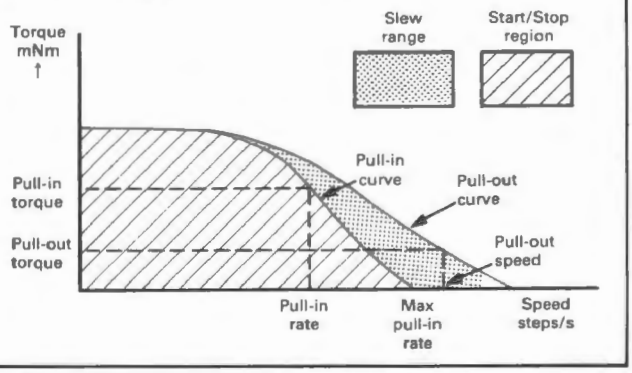
Step angle	1.8°
Step angle tolerance	±5.4′, non cumulative
Nominal coil (winding) parameters & ratings	
voltage	5Vdc
current	1A
resistance	5Ω
inductance	10mH
Holding torque	460mNm
Working torque, max.	320mNm
Detent torque (nominal)	30mNm
Rotor inertia	Less than 135gcm^2
Pull-in rate	880 steps/s (min.)
Ambient temperature	−20°C to +50°C
Temperature rise, max.**	80°C (above ambient)
Insulation class	B
Weight	600g

** Measured with two phases energised 1A, 5Vdc per phase.

Characteristics and terminology

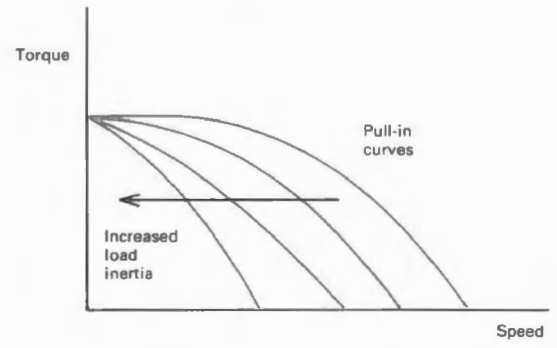
Torque-speed characteristic for a stepper motor may be represented as in Figure 1.

Figure 1 **Torque-speed characteristics**



The pull-in curve describes the maximum constant start/stop rate that a frictionally loaded motor can achieve without loss of step. This curve is dependent on the method of driving the motor and the load inertia. The effect of the latter is shown in Figure 2.

Figure 2 **Effect of load inertia on pull-in curve**



The pull-out curve describes the maximum stepping rate which a frictionally loaded motor can follow without losing steps, assuming sufficient time is allowed to accelerate the motor by ramping the frequency of the command drive circuit. Within the start/stop region the motor can be started, stopped or forced to change direction of rotation following a sudden command change from the drive circuit. However, within the slew range the motor can only be accelerated or decelerated to the

required speed and it cannot suddenly change direction.

Detent torque: the maximum torque that can be applied to the spindle of an unexcited motor without causing continuous rotation.

Holding torque: the maximum steady torque that can be externally applied to the spindle of an excited motor without causing continuous rotation.

Maximum working torque: the maximum torque that can be obtained from the motor.

Pull-in torque: the maximum torque that can be applied to a motor spindle when starting at the pull-in rate.

Pull-in rate (speed): the maximum switching rate (speed) at which a frictionally loaded motor can start without losing steps.

Maximum pull-in rate (speed): the maximum switching rate (speed) at which an unloaded motor can start without losing steps.

Pull-out rate (speed): the maximum switching rate (speed) which a frictionally loaded motor can follow without losing steps.

Pull-out torque: the maximum torque that can be applied to a motor spindle when running at the pull-out rate.

Step angle: the nominal angle that the motor spindle must turn through between adjacent step positions.

Stepping rate: the number of step positions passed by a fixed point on the rotor per second.

Positional accuracy

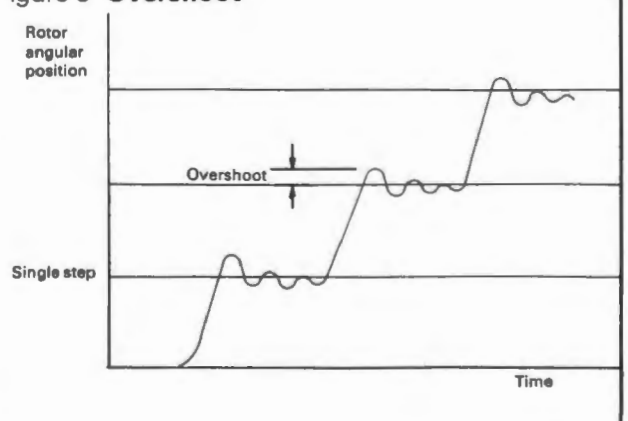
This represents the tolerance of each angular step movement. Typically within 5-10% of one step angle this error is non-cumulative ie. remains constant regardless of the number of steps advanced.

For a 4-phase motor this error averages to zero in 4 steps (corresponding to a full drive cycle). For this reason when accurate positioning is desired it is recommended, whenever possible, that the movement is divided into multiples of 4 steps.

Overshoot

When making a single step the rotor tends to overshoot and oscillate about its new position. The response depends on the drive method and load inertia. The greater the torque to inertia ratio, the less is the overshoot. In addition friction damping reduces the amount of overshoot.

Figure 3 **Overshoot**



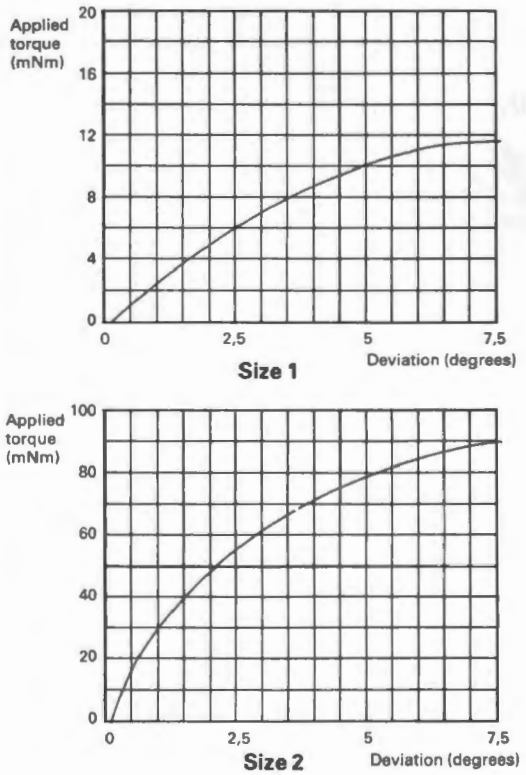
Resonance

Certain operating frequencies cause resonance and the motor loses track of the drive input. Audible vibration may accompany resonance conditions. These frequencies should be avoided if possible. Driving the motor on the half step mode (see motor drive methods) greatly reduces the effect of resonance. Alternatively extra load inertia and external damping may be added to shift resonance regions away from the operating frequency.

Deviation

The change in spindle position from the unloaded holding position due to external torque application to the spindle of an excited motor. Torque-deviation curves for size 1 and size 2 motors are shown in Figure 4.

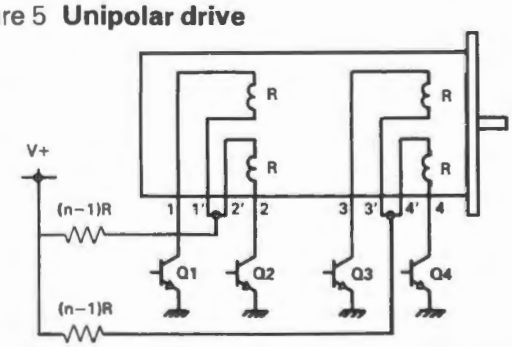
Figure 4 **Deviation as a function of applied torque**



Motor drive methods

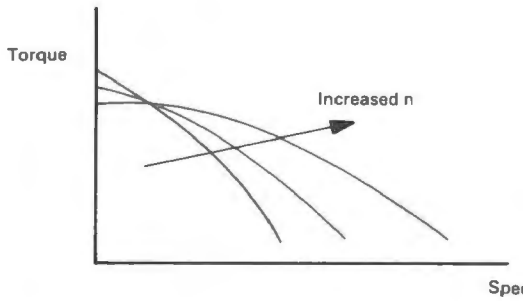
The normal way of driving a 4-phase stepper motor is shown in Figure 5.

Figure 5 **Unipolar drive**



This is commonly known as the 'Unipolar L/nR drive'. Here the current in each winding, when energised, flows in one direction only. 'n', value is ≥1 (but not necessarily an integer) and nR is the sum of the external resistance plus the winding resistance (R). By selecting a higher value for n (ie. larger external resistance) and using a higher dc supply to maintain the rated voltage and current for each winding, improved torque speed characteristics can be obtained (see Figure 6). Thus a 6V, 6Ω motor (1A per phase) can be driven from a 6Vdc supply without any series resistor, in the L/R mode. Alternatively it can be driven from a 24Vdc supply using 18Ω series resistance in the L/4R mode with much improved performance.

Figure 6 **Effect on motor performance of higher supply voltages and larger series limiting resistance**



To step a motor in a particular direction a specific switching sequence for the drive transistors Q1-Q4 needs to be followed. If this sequence is as in Table 1 (known as the unipolar full step mode) it results in the rotor advancing through one complete step at a time.

Table 1 **Full step mode**

Step No.	Q1	Q2	Q3	Q4
Start position →	ON	OFF	OFF	ON
1	ON	OFF	ON	OFF
2	OFF	ON	ON	OFF
3	OFF	ON	OFF	ON
Above sequence repeating → 4	ON	OFF	OFF	ON
5				

Anti-clockwise ↑ / Clockwise ↓

Alternatively the motor can be driven in the half step mode by a mixed single/dual phase switching as shown in Table 2. This results in the rotor advancing through half the step angle at a time. This mode stabilizes the motor operation and allows faster stepping rates (refer to stepper motor drives).

Table 2 **Half step mode**

Step No.	Q1	Q2	Q3	Q4
Start position →	ON	OFF	ON	OFF
1	ON	OFF	OFF	OFF
2	ON	OFF	OFF	ON
3	OFF	OFF	OFF	ON
4	OFF	ON	OFF	ON
5	OFF	ON	OFF	OFF
6	OFF	ON	ON	OFF
7	OFF	OFF	ON	OFF
Above sequence repeating → 8	ON	OFF	ON	OFF
9				

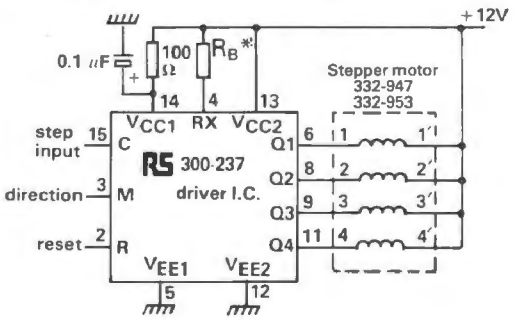
Anti-clockwise ↑ / Clockwise ↓

RS stepper motor drives
1. Driver IC SAA 1027 (300-237)

The RS 7.5° stepper motors, size 1 (332-947) and size 2 (332-953) can both be driven by this IC (in the full step mode) which provides the bi-directional switching sequence and output drive. For further details refer to RS data sheet 5566.

Circuit diagram for connecting both motors to the drive IC is given in Figure 7.

Figure 7 **Circuit diagram using SAA1027 stepper motor driver IC**

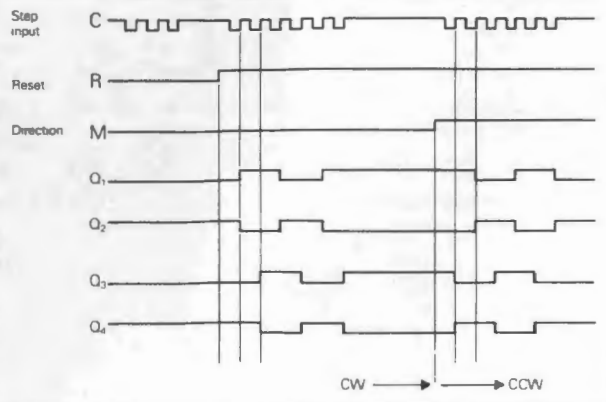


*R_B = 270Ω, 0.5W for size 1 motor and
180Ω, 1W for size 2 motor

Total driver IC + motor current is
300mA – size 1 motor and
600mA – size 2 motor

Waveform diagram for the driver IC is shown in Figure 8.

Figure 8 **Waveform diagram for SAA1027 stepper motor driver IC**



When the RS driver IC is used to drive RS size 1 and size 2 stepper motors, the torque-speed curves for both motors under no inertial load conditions (ie. frictional load only) are given in Figures 9 and 10.

Figure 9 **Torque-speed curves for size 1 stepper motor**

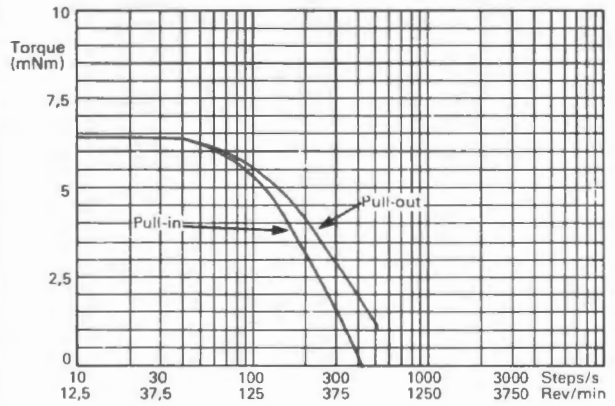
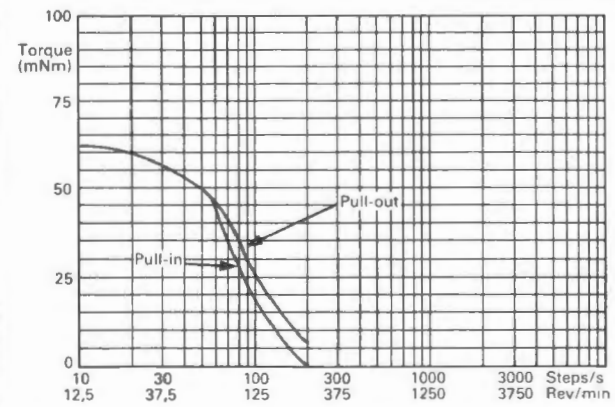


Figure 10 **Torque-speed curves for size 2 stepper motor**



Note: for a 7.5° motor.

$$\text{speed in rev/min} = \frac{60}{48} \times \text{speed in steps/sec.}$$

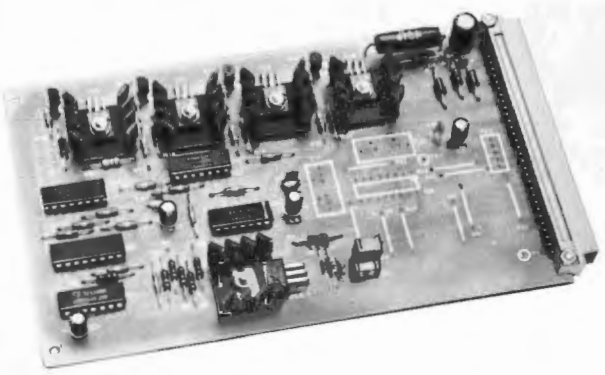
$$\text{or } \frac{60}{96} \times \text{speed in half steps/sec.}$$

2. Stepper motor drive board (332-098)

This board is capable of driving in the unipolar mode any 4-phase stepper motor up to 2A, 30Vdc/phase (including the RS 7.5° motors with much improved stepping rates over the driver IC).

- Directly compatible with any of the RS stepper motors.
- Eurocard system compatible. Alternatively it may be surface mounted.
- Full step and half step drive modes.
- External control inputs are CMOS and open collector TTL logic compatible.
- Pre-set control for setting predetermined motor phase excitation pattern.
- On-board 12V, 50mA dc output for external circuit energisation.
- Drive board and motor can share the same dc power supply.
- Provision for assembling on board oscillator (if external clock not available), having clock pulse output, base speed, running speed and stop/run controls.

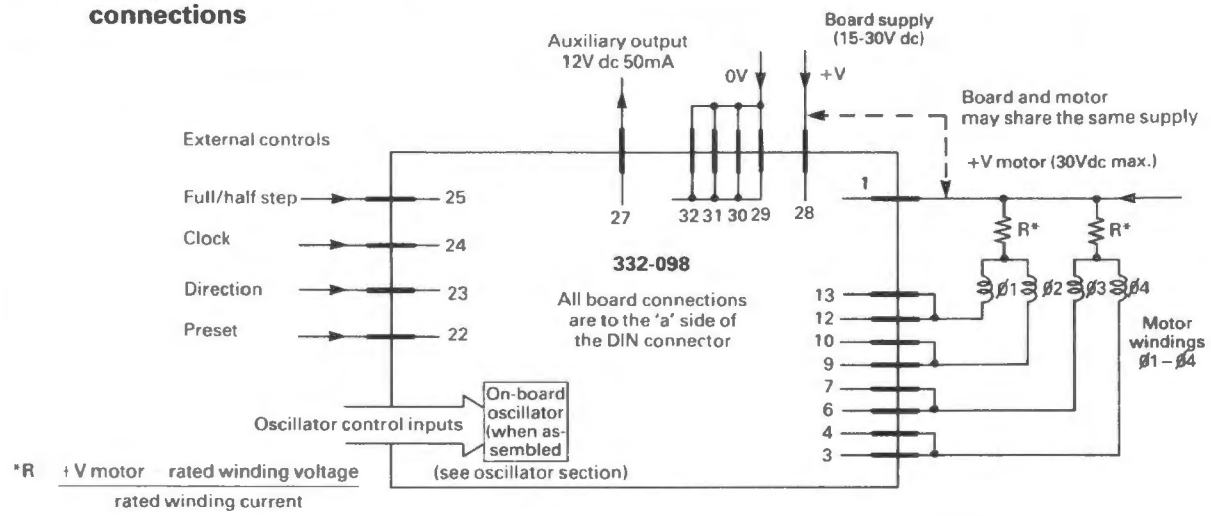
Stepper motor drive board



Technical specification

Size	Standard Eurocard 168 × 100 × 15
Mating edge connector	Standard 32 Way DIN 41612 socket eg. RS 471-503 or 467-453
Supply (board and motor)	15-30Vdc + 10% max. Unregulated smoothed.
Current consumption:	
a) board only	60mA
b) motor windings	dependent on motor used – up to 2A/phase max.
On-board auxiliary output	12Vdc 50mA max. regulated
Switching logic control inputs	Level '0' 0V } CMOS and open collector Level '1' 12V } TTL compatible
a) Full/Half step	Level '1' full step Level '0' half step
b) Direction	Clockwise or anti-clockwise
c) Clock step	1Hz-25KHz, 10μs minimum pulse with negative edge triggered
d) Preset	Active level '0' Sets motor drive states to Q1 & Q3 OFF, Q2 & Q4 ON (full step mode) Q1, Q2 & Q3 OFF, Q4 ON (half step mode) – See Figure 11, Automatic preset at switch ON.

Figure 11 **Stepper motor drive board connections**

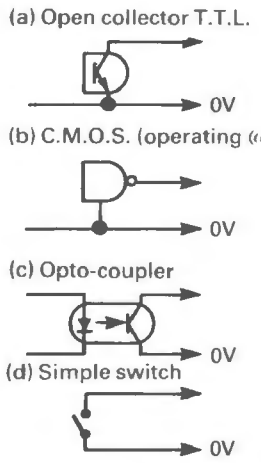


Maximum power dissipated through R = (rated motor current)^2 × R. If the power dissipation is high it is advisable to arrive at the required value of R by using a network of series or parallel resistors. The use of heat sinks and higher wattage resistors may be necessary in applications where power dissipation is excessive.

Maximum current consumption (motor + board) = 2x (current per phase) + 60mA. Thus ensure power supply cables used are sufficiently rated.

External control signal eg. full/half step, direction etc as well as the oscillator (if fitted) stop/run signal can be applied to the board in any of the methods of Figure 12.

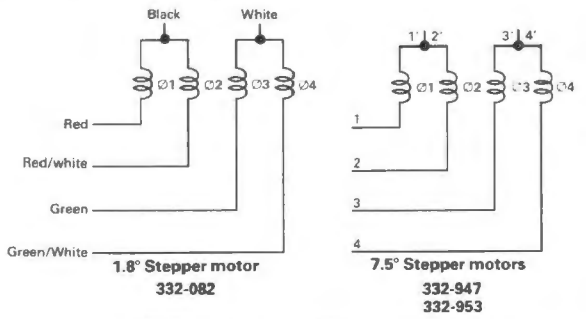
Figure 12 **External control input applications**



Connection to RS stepper motor

When the windings of the RS stepper motors are assigned (Ø1–Ø4) as shown in Figure 13, they can be connected to the board according to Figure 11.

Figure 13 **Motor winding connections**



If the supply voltage is set to 24Vdc then R values for use with the RS motors are given in Table 3.

Table 3

motor	rated current (A)	rated winding voltage (V)	R (Ω)	power dissipation through R (W)
332-947	0.1	12	120	1.2
332-953	0.24	12	47	3
332-082	1	5	19	19

Here the 7.5° motors are driven in the L/2R mode while the 1.8° motor is driven in the L/5R (approx.) mode.

Typical pull-out performance characteristics (under no-load conditions) for the RS motors when being driven by the drive board 332-098 using a 24Vdc supply and series resistance as in Table 3 are given in Figures 14, 15 and 16.**

Figure 14 **Pull-out performance for 7.5° size 1 stepper motor (with RS drive board 332-098)**

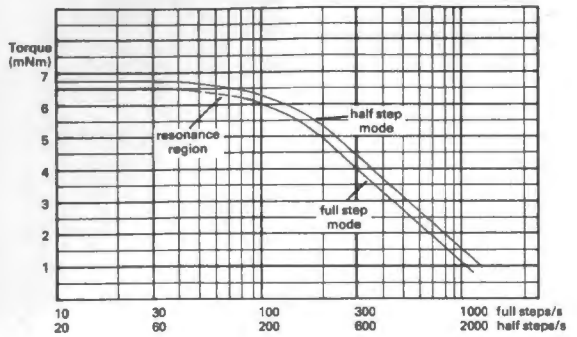


Figure 15 **Pull-out performance for 7.5° size 2 stepper motor (with RS drive board 332-098)**

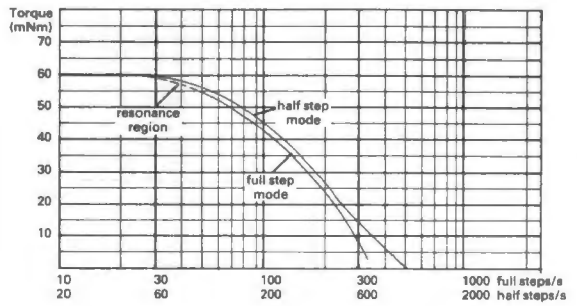
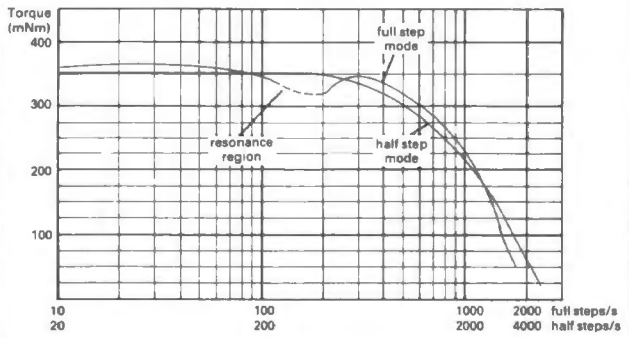


Figure 16 **Pull-out performance for 1.8° stepper motor (with RS drive board 332-098)**

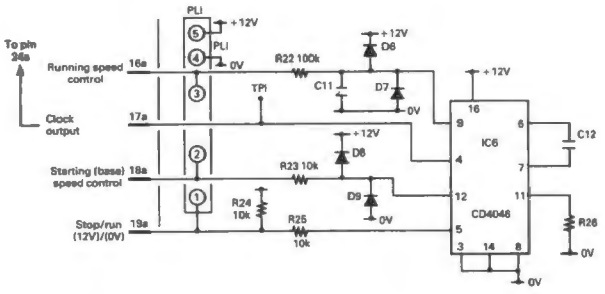


** These results are typical at 20°C. If the motor temperature rises due to power dissipation in the windings and/or higher ambient temperatures the torque capability decreases (typical torque derate −0.4% per degree rise in temperature).

On-board oscillator assembly

If external clock source is not available an on-board oscillator can be assembled simply by soldering into place the required components listed below – see current RS catalogue. (Note the oscillator clock output must be externally wired to the clock input – pin 24a.)

Figure 17 **On-board oscillator**



R22	100kΩ resistor	RS 131-491	1 off
R23, 24, 25	10kΩ resistor	RS 131-378	3 off
D6, 7, 8, 9	Signal diode	RS 271-606	4 off
IC6	CMOS IC	RS 306-645	1 off
R26, C11 & C12	(Value depends on application)		1 off each

If oscillator remote controls are required (eg. front panel controls) then plug PL1 (5 Way inter-pcb RS 467-576) can be added together with mating cable shell RS 467-627 and crimp terminals RS 467-598.

Starting (base) and running speed control

The on-board oscillator can be arranged to start at a fixed frequency (thus a fixed motor speed) and then ramp up to a final value (the running motor speed). This facility is available to start the motor within its pull-in performance region and then accelerate the motor to its final speed such that it can operate within the pull-out mode. On switch-off the motor decelerates automatically.

Three parameters need to be determined for any application:

a) The starting speed: this should be below pull-in speed for the motor (including any additional load).

b) The running (final) speed: this should be within the pull-out capability of the motor (including any additional load).

c) The acceleration and deceleration rate between starting and running speeds: this is limited by the motor capability to accelerate through its own, plus any load, inertia.

Figure 18 **External oscillator controls**

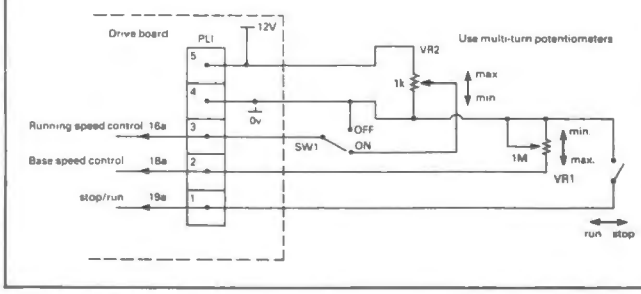
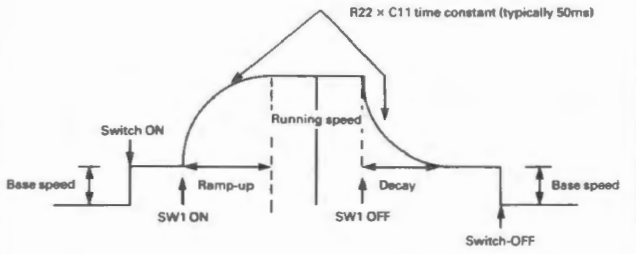


Figure 19 **Motor speed ramping characteristics**



Note: Oscillator frequency corresponds directly to motor speed in steps/s or half step/s depending on the motor drive mode.

For a 1.8° stepper motor

$$\text{speed in revs/min} = \frac{60}{200} \times \text{speed in step/s}$$

$$\text{or} \quad \frac{60}{400} \times \text{speed in half step/s}$$

Oscillator frequency setting

Recommended component values (refer to Figures 17 and 18)

VR1	0 – 1MΩ	use multiturn
VR2	1kΩ	potentiometers
R26	10kΩ – 1MΩ	
C12	greater than 100 pF	

Determine the base frequency and maximum running frequency. Using Figure 20 choose a value for C12 and VR1. Calculate the ratio maximum running frequency/base frequency to determine the ratio of

$$\frac{\text{VR1 + R23 (fixed at 10kΩ)}}{\text{R26}}$$

and thus using Figure 21 establish the required value for R26.

Figure 20 **Base frequency variations with timing capacitor C12**

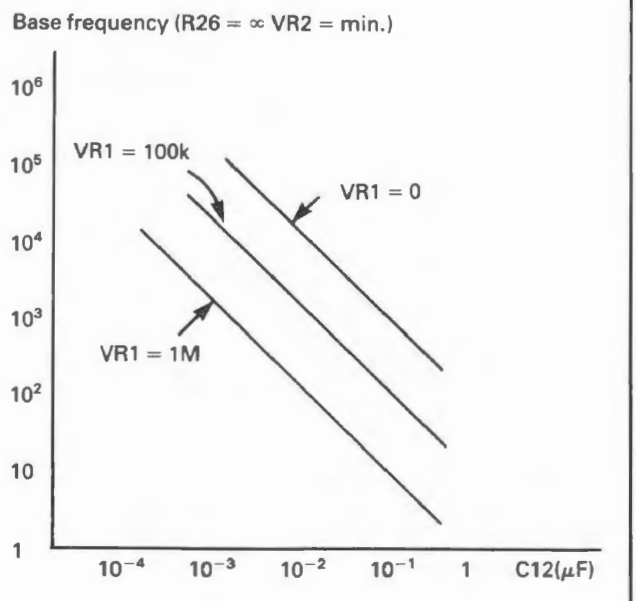


Figure 21 **Resisitor value as a function of maximum frequency/base frequency**

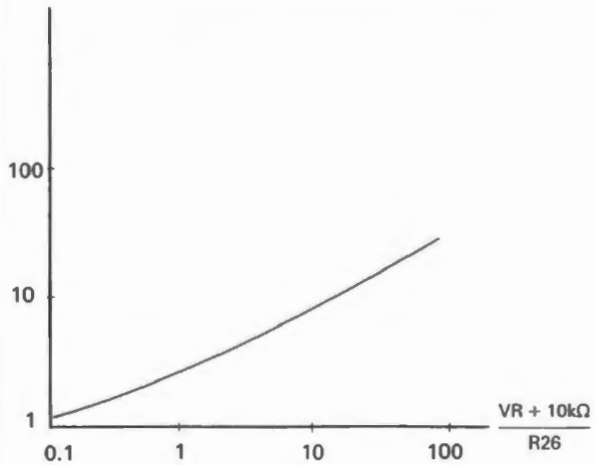
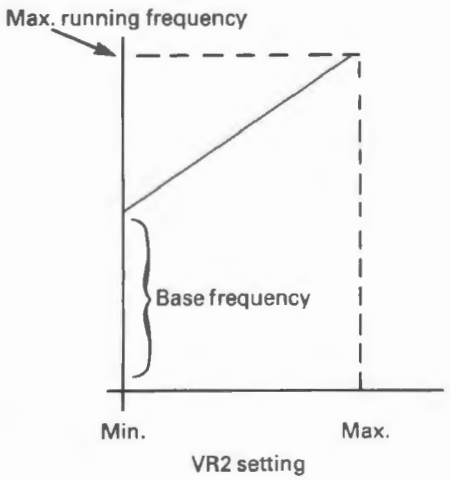


Figure 22 **Oscillator frequency range**



Once all component values are established and assembled the oscillator frequency range is as shown in Figure 22. If SW1 is OFF the oscillator runs at base frequency. When SW1 is ON the oscillator builds up (at a rate depending on $R_{22} \times C_{11}$ time constant) to a frequency determined by VR2 setting.

Use of size 1 motor with the RS range of synchronous gearboxes

The RS stepper motor (size 1) may be fitted to the RS range of synchronous gearboxes 336-400 etc. to provide improved resolution (finer step angle) and increased torque at lower speeds. Another important advantage is the greatly increased capability of the motor to drive higher inertial loads since load inertia seen by the motor is $(I/\eta n^2)$, I being the load inertia at the gearbox output, n is the gearbox ratio and is the gearbox efficiency. Optimum power transfer is achieved when load inertia (seen by the motor) matches that of the motor's rotor. With loads of this magnitude the start/stop without error (pull-in) curve is slightly different from the no load condition. Maximum allowable load inertia (seen at

the motor end) is five times the optimum load inertia. The table below gives the load inertia values at the gearbox output shaft for each gearbox used with size 1 motor.

Gearbox	Gearbox ratio	Recommended optimum load (kg cm^2)	Max. allowable load (kg cm^2)
332-868	25:6	0.034	0.17
336-450	25:2	0.27	1.36
336-444	25:1	1.1	5.5
336-438	50:1	4.44	22.2
336-422	125:1	24.85	124
336-416	250:1	100	380*
336-400	15000:1	6000*	6000*

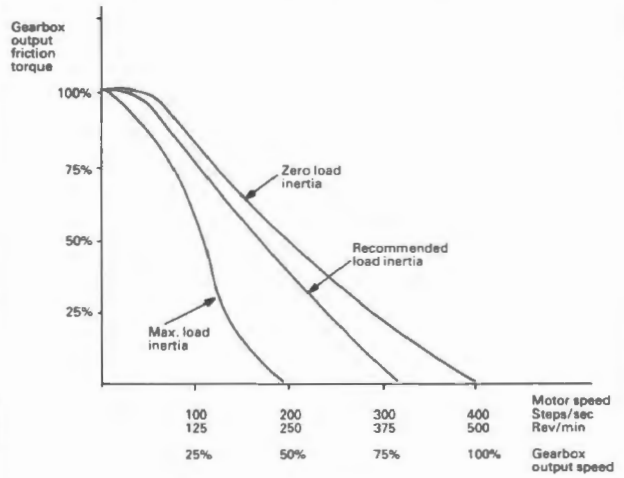
* limited by gearbox maximum ratings.

In addition the following limiting values must not be exceeded at the gearbox output shaft:

maximum radial force : 40 Newtons
maximum axial force : 20 Newtons

When size 1 motor is fitted to any of the RS synchronous gearboxes and driven by the RS driver IC the torque-speed characteristic of the combined motor and gearbox under various load conditions is shown in Figure 23. However, if the motor is driven by the RS stepper motor drive board 332-098 which gives improved performance, these results are correspondingly improved.

Figure 23 **Torque-speed characteristics for motor-gearbox combination**



Percentage values above are to be found, for any particular gearbox, in the table below.

Gearbox	100% output torque (Ncm)	100% output speed rpm	Output step angle
332-868	1.9	120	1.8°
336-450	5.1	40	0.6°
336-444	10.3	20	0.3°
336-438	20.5	10	0.15°
336-422	46.6	4	0.06°
336-416	80*	2	0.03°
336-400	80*	0.033	0.03′

* output torque limited by gearbox.

Note: Typical backlash at gearbox output = 2° and should be considered if positional accuracy is critical.

Design considerations

The torque-speed characteristic must be consulted whenever a stepper motor is chosen for a particular application. The following equations generally apply.

Required torque = friction torque + acceleration torque where
friction torque = friction force x radius
acceleration torque = load inertia x acceleration
acceleration =

$$\frac{\text{change in speed (steps/sec)}}{\text{acceleration time (sec)}} \times \frac{2\pi}{\text{steps/rev}}$$

Thus for a 7.5° stepper motor

$$\text{acceleration} = \frac{\triangle \text{ speed}}{\triangle t} \times 0.13$$

Units: Torque – mNm
Inertia – gm^2
Acceleration – radians/sec

Unit conversion

Unit	x 10^{-4}	x 10^{-1}	x 10	x 10^3
mNm			Ncm	Nm
gm^2	gcm^2	kgcm^2		kgm^2

Acceleration control is achieved by varying the input frequency to the motor drive circuit eg. using an RC time constant and a voltage controlled oscillator.

Note: The pull-out torque capability of the motor at the required speed must be higher than the required torque to ensure correct operation.

Use of gearbox

The following equations apply when the motor drives a load through a gearbox.

$$I_r = \frac{I_L}{n^2} \quad \text{and} \quad T_r = \frac{T_L}{n}$$

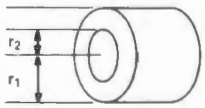
where

I_r = reflected load (including gearbox inertia at motor shaft).
I_L = load inertia at gearbox output.
T_r = reflected load torque at motor side.
T_L = load torque required at gearbox output.
n = gearbox ratio.
= gearbox efficiency (typically 0.6 – 0.7 for the RS range of synchronous gearboxes).

Moment of inertia (load inertia)

1. Cylinder

$$I = \frac{M}{2}(r_1^2 + r_2^2)$$



M = mass of cylinder

2. Disc or shaft

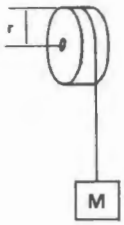
$r_2 = 0$ in above equation thus

$$I = \frac{M}{2} r_1^2$$

RS data

3. Pulley and weight (or rack and pinion)

$I = Mr^2$



In the above equations
M is in grams
r is in metres
I is in gram. (metres)^2

Examples

1) A frictional load of 20 mNm must be moved 300° in 2 seconds. Thus using a 7.5° motor

$$\text{Stepping rate} = \frac{300}{7.5 \times 2} = 20 \text{ steps/sec}$$

Consulting the torque-speed curve for size 2 motor shows that at 20 steps/sec the torque capability is 60 mNm. Thus acceleration torque available = 60 – 20 = 40 mNm.

It is always useful in practice to apply a safety margin by devaluing the available motor torque to say 60% of theoretical value, ie. 40% safety margin.

2) A 0.2gm^2 load is to be accelerated to 200 steps/sec against a frictional torque of 60mn/m using a size 1 motor and a 25:1 reduction gearbox (RS336-444). Calculate acceleration time and number of steps required to reach terminal speed.

Using the formulae in this data sheet;

$$\text{Reflected load inertia} = \frac{0.2}{(25)^2 \times 0.7} = 45 \times 10^{-5} \text{gm}^2$$

$$\text{Motor rotor inertia} = 26 \times 10^{-5} \text{gm}^2$$

$$\text{Reflected friction torque} = \frac{60}{25 \times 0.7} = 3.43 \text{mNm}$$

From the pull-out curve for the size 1 motor the torque at 200steps/sec is 4mNm

Acceleration torque = 4–3.43 = 0.57mNm.

$$\text{Acceleration} = \frac{0.6 \times 0.57}{(26 + 45) \times 10^{-5}} = 482 \text{rad/sec}^2$$

allowing 40% safety margin.

$$\text{Acceleration time} = \frac{200}{482} \times 0.13 = 54 \text{m sec.}$$

Therefore number of steps required during acceleration = average speed x time = $\frac{200}{2} \times 0.054$

or 6 complete steps.

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RS data

Stepper motor driver i.c. SAA 1027

Stock number 300-237

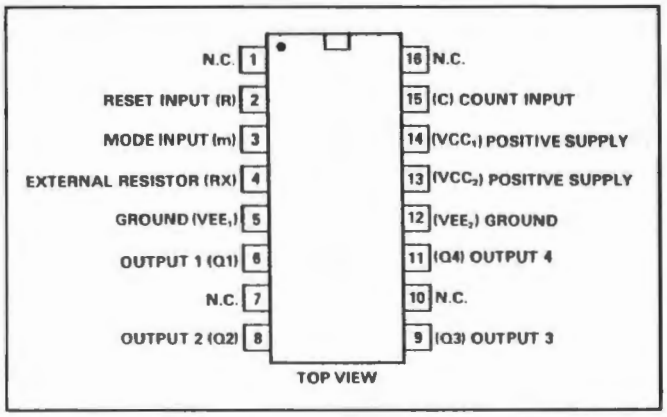
The RS SAA1027 is a bipolar integrated circuit intended for driving a 4-phase two stator stepper motor. The circuit consists of a bidirectional 4-state counter and a code converter to drive the four outputs in the sequence required for driving a stepper motor.

It features high noise immunity inputs, clockwise and anticlockwise operation, a reset facility and high current outputs that are protected against damage by voltage overshoots.

For further details of RS stepper motors please see Data Sheet 5550.

Features

- High noise immunity inputs
- Clockwise and counter-clockwise rotation
- Reset facility
- High output current
- Outputs protected against damage by overshoots



Absolute maximum ratings

Supply voltage	18V DC
Input voltage, all inputs	18V
Current into pin 4	120mA
Output current	500mA
Storage temperature range	−40°C to +125°C
Operating temperature range	−20°C to +70°C

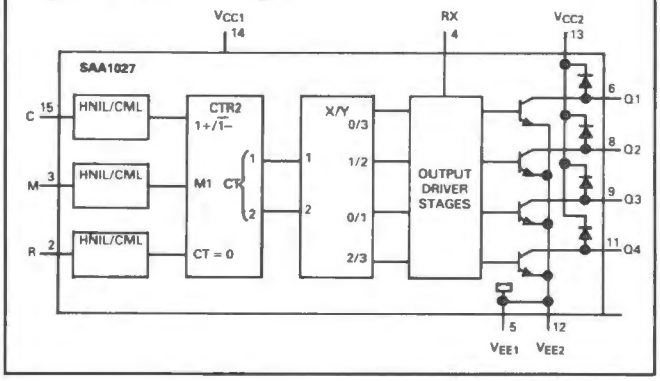
Electrical characteristics

V_{CC} = 9,5 to 18V; V_{EE} = 0V; T_{amb} = −20 to +70°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply V_{CC1} and V_{CC2} (pins 14 and 13)					
Supply current at V_{CC1} = 12V; unloaded; all inputs HIGH; pin 4 open	I_{CC}	2	4,5	6,5	mA
Inputs C, M and R (pins 15, 3 and 2)					
Input voltage					
HIGH	V_{IH}	7,5	–	–	V
LOW	V_{IL}	–	–	4,5	V
Input current					
HIGH	I_{IH}	–	1	–	μA
LOW	$-I_{IL}$	–	30	–	μA
External resistor pin RX (pin 4)					
Voltage at RX at V_{CC} = 12V ±15%; R_X = 130Ω ± 5%	V_{RX}	3	–	4,5	V
Outputs Q1 to Q4					
Output voltage LOW					
at I_{OL} = 350mA	V_{OL}	–	500	1000	mV
at I_{OL} = 500mA	V_{OL}	–	700	–	mV
Output current					
LOW	I_{OL}	–	–	500*	mA
HIGH at V_Q = 18V	$-I_{OH}$	–	–	50	μA

* See Figures 3 and 4.

Figure 1 **Block diagram**



The blocks marked HNIL/CML are high noise immunity input stages, the block marked CTR2 is a bidirectional synchronous 2-bit (4-state) counter and the block marked X/Y is a code converter. C is the count input, M the mode input to select forward or reverse counting and R is the reset input which resets the counter to content zero.

Functional description

Count input C (pin 15)
The outputs change state after each L to H signal transition at the count input.

Mode input M (pin 3)
With the mode input the sequence of output signals, and hence the direction of rotation of the stepping motor, can be chosen, as shown in the following table.

Counting sequence	M = L				M = H			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
0	L	H	L	H	L	H	L	H
1	H	L	L	H	L	H	H	L
2	H	L	H	L	H	L	H	L
3	L	H	H	L	H	L	L	H
0	L	H	L	H	L	H	L	H

Reset input R (pin 2)
A LOW level at the R input resets the counter to content zero. The outputs take on the levels shown in the upper and lower line of the table above.

If this facility is not used the R pin should be connected to the supply.

External resistor pin RX (pin 4)
The external resistor R4 connected to RX sets the base current of the output transistors. Its value has to be chosen in accordance with the required output current (see Figure 5).

Outputs Q1 to Q4 (pins 6, 8, 9 and 11)
The circuit has open-collector outputs. To prevent damage by an overshooting output voltage the outputs are protected by diodes connected to V_{CC2}, pin 13. High output currents mainly determine the total dissipation, see Figure 3.

Figure 2 **Waveform diagram**

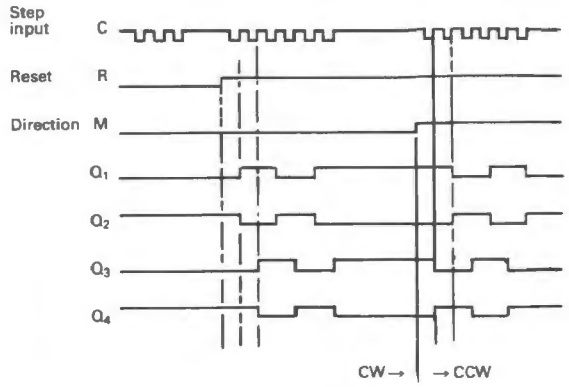


Figure 3 **Total power dissipation P_{tot} as a function of output current I_{OL}**

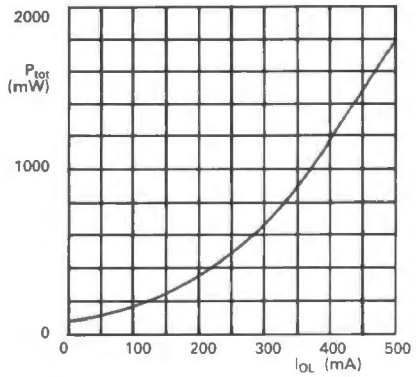


Figure 4 **Power derating curve**

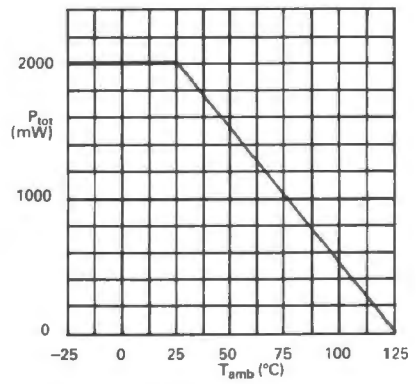
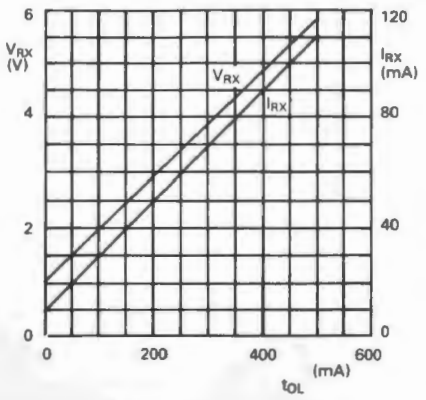
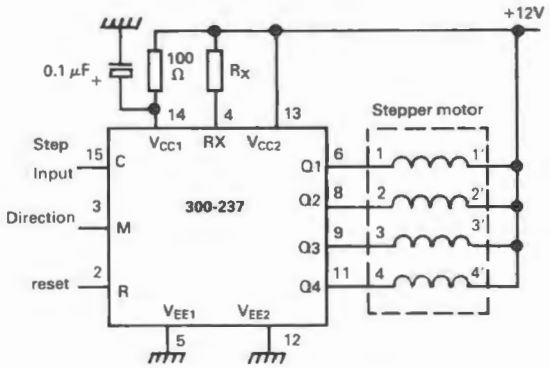


Figure 5 **Current I_{RX} into RX and voltage V_{RX} on RX as a function of required output current I_{OL}**



Applications

Figure 6 **Typical application of the SAA 1027 as a stepper motor driver**



RS data

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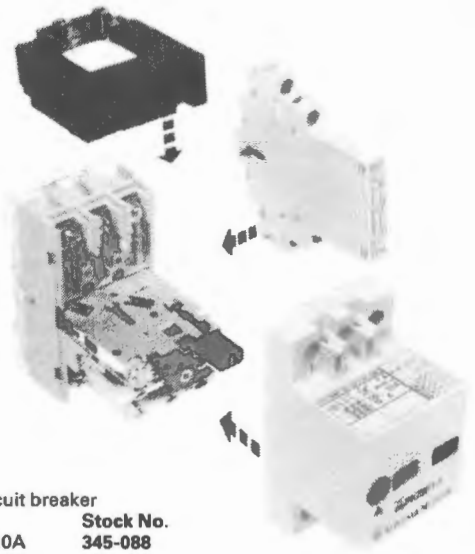
RS data

Motor circuit breakers and accessories



Undervoltage trip
240V 50Hz **345-151**
415V 50Hz **345-167**

Auxiliary contacts
1 N/O + 1N/C
345-173

Basic circuit breaker

flc	Stock No.
0.6 – 1.0A	345-088
1.0 – 1.6A	345-094
1.6 – 2.4A	345-101
3.4 – 4.0A	345-117
4.0 – 6.0A	345-123
6.0 – 10.0A	345-139
10.0 – 16.0A	345-145

A range of 3 pole, motor circuit breakers (manual motor starters) with three adjustable, thermal overload trips which provide both overcurrent and phase failure protection and three instantaneous magnetic trips for short circuit protection. The unit may be either used as a manual motor starter (ie. a hand operated motor switch/protector) or coupled to a contactor to provide combined back-up protection. In the latter application, the motor circuit breaker is left in the 'on' position, the on/off switching is accomplished by the contactor control circuit.

Conformity to standards
VDE 0660, IEC 157-1 (BS 4752)
IEC 292-1 (BS 4941)

Environmental protection
Dust/Water _____ IP20
(covers finger and back of hand protection to VDE 0106 pt 100)
Impact resistance (during 20ms) _____ 20g
Ambient temperature open: _____ –25°C to +50°C
enclosed: _____ –25°C to +40°C
Overload temp. compensation _____ –5°C to +40°C

Features

- Overcurrent protection – user adjustable with ambient temperature compensation
- Short circuit protection, instantaneous magnetic trips at 12X rated current
- Phase failure protection. Single phase sensitivity to IEC 292, VDE 0105 and VDE 0660 pt 104
- High breaking capacity. May be used, in most applications, without the need for back-up fuses (see tables on Page 2)
- May be mounted in any position
- Three pole switching but may be wired for single phase applications (see Figure 6)
- Test facility for checking switch operation and trip indicator
- Fail-safe remote tripping possible using undervoltage trip. Ideal for safety interlocks
- Modular construction to DIN 43 880 permits the unit to be housed in a standard enclosure, either singularly or alongside associated equipment (modular contactors etc.)

Safety applications
The motor circuit breaker when fitted with an undervoltage trip can be switched off remotely using emergency pushbuttons, level switches, positive break door interlocks or guard switches, magnetic safety switches, limit switches and similar devices. The low-volt release feature is useful on appliances or machines that would present a danger if an interrupted mains supply was suddenly restored causing them to restart without warning eg. kitchen equipment such as potato peelers, bacon slicers etc.

Where the unit is combined with a contactor, a double safe means of remote switching off may be achieved by simultaneous interruption of the power supplies to the undervoltage trip and contactor coil.

Motor starting applications
The motor circuit breakers meet the requirements of IEC 292-1 and BS 4941: part 2 1977 for Direct-on-line AC starters. They have a switching capacity which corresponds to the motor starting currents (approx 6 x flc). Suitable for frequent switching a maximum of 40 ops/hr. This is in excess of intermittent duty class 0.3 (30 ops/hr) as set out in 4.4.4.3.1. of IEC 292-1. All poles are interrupted in the event of an overcurrent. The tripping time is in accordance with the curve shown in Figure 1. A trip-free feature prevents the operation of the 'on' button with an uncleared fault.

5572

Explosion proofed motors Ex-e
Characteristic curves and data for PTB certification (applied for) available on request.

Adjustment of bimetal trips
The bimetal trips are screwdriver adjustable over the stated range. This adjustment is ambient temperature compensated (–5°C to +40°C) but does not affect the fixed, instantaneous magnetic trip which is set at 12 x I_e max. where I_e max. is the highest bimetal trip setting.

Example: stock no. 345-094
bimetal trip setting adjustable 1-1.6A instantaneous magnetic trip setting 19A (12 x 1.6A).

Short circuit protection
The instantaneous magnetic trips in each current path can handle high currents (see table for Breaking capacity). The high inherent resistance of the bimetal trips has a current limiting effect such that, for low rated motor currents, it is kept to within the high switching capacity of these units. The motor circuit breaker is then said to be inherently short circuit proof.

For larger motors the prospective fault current at the point of installation must be taken into consideration. If this prospective fault current exceeds the breaking (or switching) capacity, as set out in the table, then back up protection may be required.

Breaking capacity (IEC 157-1, VDE 0660. Part 101).

Values shown at various operating voltages kA rms/cos θ

Setting range of bimetal trips	**Operating voltages**				
	220/ 240V	380/ 415V	440V	500V	660V
1 – 10A	∞	6/07	35/08	15/095	1/095
10 – 16A	6/07	4/08	25/09	15/095	1/095

∞ = inherently short circuit proof.

Back-up fuses (BS.88)

Setting range of bimetal trips (flc)	**Fixed magnetic trip setting**	**Max. back-up fuses required when fault level exceeds breaking capacity of starters**			
		220/ 240VC	380/ 415V	500V	600V
0.6 – 1.0A	12A	*	*	*	*
1.0 – 1.6A	19A	*	*	*	*
1.6 – 2.4A	29A	*	*	25A	20A
2.4 – 4.0A	48A	*	*	35A	25A
4.0 – 6.0A	72A	*	*	50A	35A
6.0 – 10.0A	120A	*	50A	50A	35A
10.0 – 16.0A	192A	63A	63A	63A	50A

* No back-up fuse required. Short circuit proof up to highest fault currents.

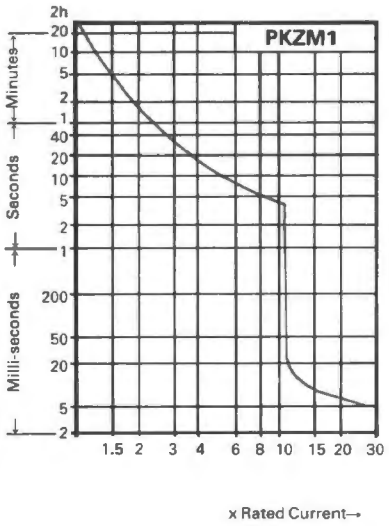
For suitable industrial fuselinks and fuseholders to BS88 see current RS catalogue.

Time/Current characteristic curve
The characteristic curve shows the tripping time of the starter in relation to the current.

Mean values of tolerance ranges at 20°C ambient temperature from initial cold state.

At operating temperature, the tripping time of the bimetal trips is approximately ¼ of that stated.

Figure 1



Cable protection
Overcurrent and short-circuit:
(to IEC 364 part 43)
Protection of PVC insulated cables against thermal overload in fault conditions

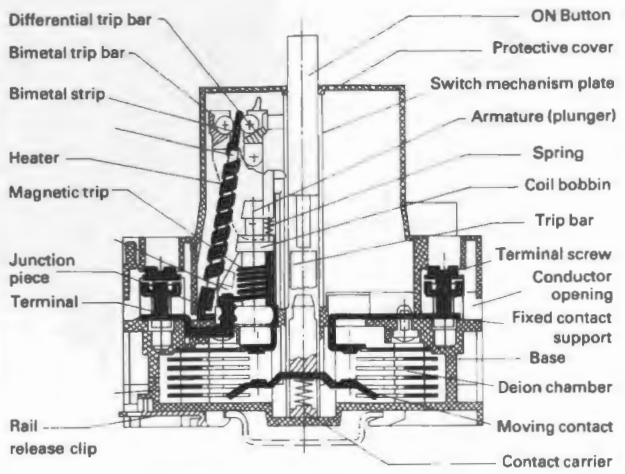
Minimum cross-section protected 380/415V, 50 Hz, Cu. mm²					**Type (bi-metal trip setting)**
4	2,5	1,5	1	0,75	
					0.6 – 1.0A
					4.0 – 6.0A
					6.0 – 10.0A
					10.0 – 16.0A

Shaded section shown on the table shows the cable cross-sections for which the RS Motor circuit breaker provides positive protection.

Phase failure protection
The design of the bimetal trips and the differential trip bar (see Figure 2) ensures interruption of all three current paths, in the event of a loss of a phase, down to 90% of preset flc.

This fulfils the requirements 7.5.3.2.3. of BS.4941: Part 1: Table VIIIB (IEC 292-IC).

Figure 2



Technical specification (main contacts)

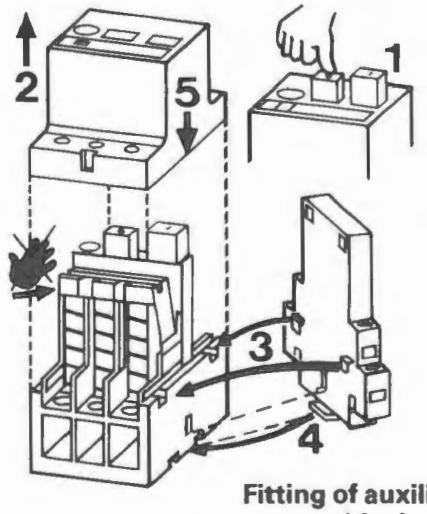
Rated insulation voltage U_i _____ 660V
Continuous current I_u = } _____ bitmetal trip
rated operating current I_e } _____ /setting
Mechanical life _____ 0.1×10^6 ops
Maximum switching frequency _____ 40ops/hr
Contact life (AC3) _____ 0.1×10^6 ops

Accessories

Auxiliary contacts

An auxiliary contact block, with 1N/O +1N/C contacts may be fitted as shown in Figure 3.

Figure 3



Fitting of auxiliary contact block on either one or both sides

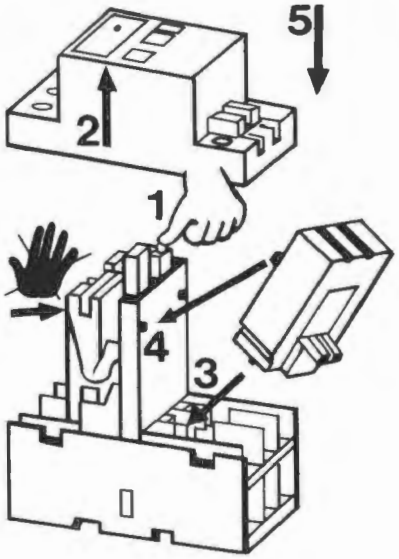
Contact ratings: rated insulation voltage 500V. Continuous current I_{th} = 6A.

Voltage	AC11	voltage	DC11 (T = 200ms)
220-240V	3.5A	60V	1.5A
380-415V	2.0A	110V	1.0A
400-500V	1.5A	220V	0.5A

Terminal capacity (up to 2 cables) 0.75–2.5mm^2

Undervoltage trips

Figure 4



Fitting of under-voltage trip

Two versions of undervoltage trip are available:

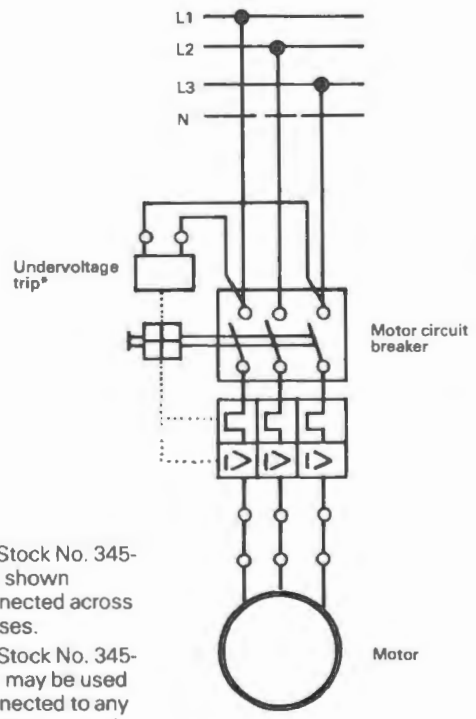
Stock no.	Coil voltage
345-151	240V 50Hz
345-167	415V 50Hz

For typical applications see 'Safety applications' on page 1, also Figures 5 and 6.

Pick-up voltage _____ 80% coil voltage
Drop-out voltage _____ 70-35% coil voltage
Coil rating _____ 100% duty factor

Supply voltage monitoring of a motor circuit breaker, by means of undervoltage trip

Figure 5



*RS Stock No. 345-167 shown connected across phases.
RS Stock No. 345-151 may be used connected to any phase to neutral.

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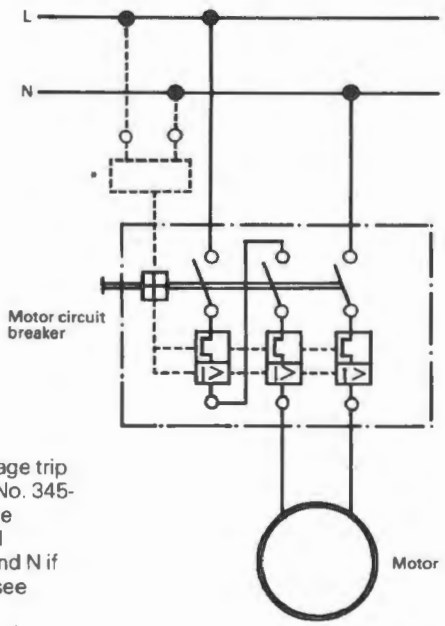
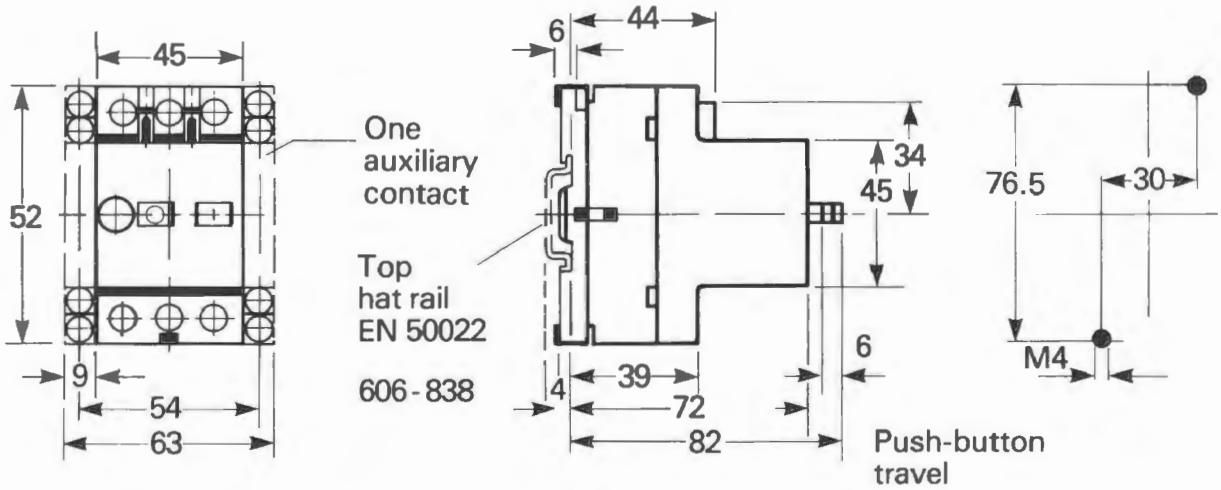
Connections for single phase motors

Figure 6



*Undervoltage trip RS Stock No. 345-151 may be connected across L and N if required (see safety applications).

Figure 7 **Dimensions**



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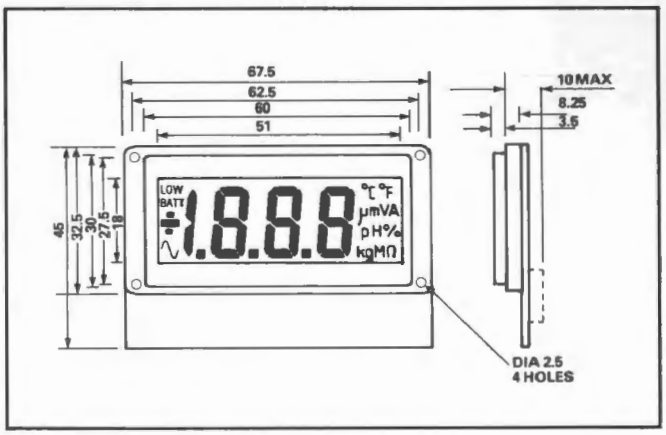
Single rail supply LCD DVM module

Stock number 257-852

A very low profile, d.v.m. module especially designed for single rail power supply working. This enables the power supply 0V to be connected to the signal 0V and allows a flexibility in system design not usually associated with this style of module. The 3½ digit clear LCD display is further enhanced by an extensive set of user-selectable legends as shown. A particularly useful feature is the solder pads on the rear of the module that allow very easy linking of connections to bring up the desired legends on the display. All the usual features such as auto-zero, auto-polarity, overrange and low battery indicator are present. Digit height is 15mm (0.6in). Maximum display is 1999, giving an effective 'full scale deflection' of 200mV. Accuracy is 0.05% of input ±1 count. Current consumption is typically 1mA. An internal bandgap reference assures excellent stability of the reading.

Features

- System flexibility – module 'ground' can also be signal 'ground'
- Extensive set of display annunciators (legends)
- Auto-zero
- Auto-polarity
- Overrange and low battery indications
- 15mm (0.6in) digit height
- 199.9mV basic fsd
- Bandgap reference for stability



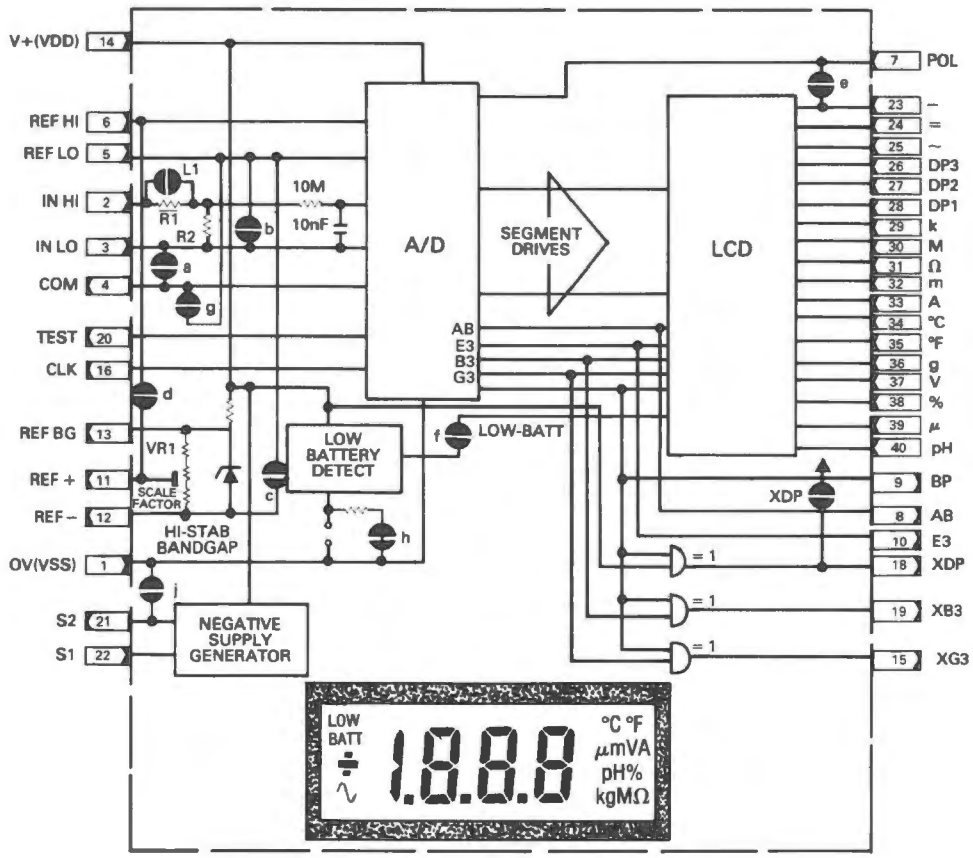
Electrical characteristics $T_A = 25°C$

Parameter		Value (typical)
Power supply voltage, V_{SS} to V_{DD}	Single ended mode (Figure 4)	2.5 to 7.5 Vdc
	Conventional connection (Figure 6)	5 to 15 Vdc
Supply current (excluding common current)		1mA
Display resolution		1999, 1 count = 100µV (without attenuators)
Input impedance (See note 1)		>1000MΩ
Error		0.05% of input ± 1 count
Range temperature coefficient		50ppm/°C
Input leakage current		1pA
Common mode rejection ratio		86dB
Sample rate		3/sec

Operating temperature 0°C to +50°C
Storage temperature –20°C to +60°C

Note 1: Operations under many practical conditions ie. facilitated by connection of a 10mΩ resistor across the input.

Figure 1 **Schematic diagram**



Note: Pad j **must** be linked for single-ended operation.

Circuit notes

The module incorporates a dual-slope-integration analogue-to-digital converter which consumes typically 50µA from the power supply.

The converter functions ratiometrically and has fully differential analogue signal and reference inputs.

An RC network provides signal input filtering and overload protection.

Internally, the converter operates with 200mV full scale although a hermetically sealed trimmer is provided to facilitate display adjustment for individual sensor scaling. For larger changes in scaling, input voltage attenuators or current shunts may easily be added to the instrument. A high stability bandgap voltage reference ic produces 100mV reference, or an external voltage may be applied to the reference input. The display reading
= (Signal Input ÷ Reference Input) x 1000.

Standard features include autozero circuitry, automatic polarity, and overrange indication of a 1 displayed in the most significant digit position and remaining digits blanked. Correct autozero operation is facilitated by connection of 10mΩ resistor across the input terminals. The autopolarity circuitry functions at zero signal voltage for precise null detection.

An internal RC oscillator provides a reading rate of approximately 3 per second.

Low battery detection circuitry provides advance warning of battery failure directly on the display. The value of R10 may be altered, if required, by adding a resistor at the rear of the pcb and splitting pad h to isolate the internal resistor. Resistors in the range 100k to 200k are usually required.

The differential analogue inputs may be operated within 0.5V below the positive supply (V_{DD}) and 1V above the negative supply (V_{SS}). A common mode reference point (COM) is provided to enable measurement of signals fully floating with respect to the power supply. The single-ended operation facility removes the restriction with respect to negative supply, which may then be connected direct to signal low.

Connections

The module is extremely versatile and the connections are listed below.

Pin 1 Supply negative 0V (V_{SS})
Pin 2 Analogue signal HI input (IN HI)
Pin 3 Analogue signal LO input (IN LO)
Pin 4 Analogue common (COM)

Internally derived common mode reference point established approximately 3V below V+, for use with signals floating with respect to supply.

Pin 5 Reference LO input (Ref LO)
Pin 6 Reference HI input (Ref HI)

Differential reference voltage inputs, against which the input signal is compared and displayed ratiometrically.

Pin 7 Polarity output (POL)

The polarity output signal is in antiphase to the backplane signal when IN HI is negative with respect to IN LO. Connecting POL to – provides automatic indication of negative inputs and positive inputs are implied by lack of the – legend. To obtain + and – indication connect POL to: via a FET inverter and connect – to XDP.

Pin 8 AB output for use in autoranging circuits
Pin 9 Backplane (BP)

Square wave signal derived from internal oscillator, to which all LCD symbol drives are referred. Symbols are turned on when driven by a signal in antiphase to BP.

Pin 10 E3 output for use in autoranging circuits
Pin 11 Reference HI output (REF +)
Pin 12 Reference LO output (REF –)

Adjustable 100mV reference voltage provided when REF – correctly terminated (usually to COM).

Pin 13 Bandgap reference (REF BG)

High-stability output from bandgap voltage reference, typically 1.2V wrt REF – when the latter is correctly terminated.

Pin 14 Supply positive V+ (V_{DD})
Pin 15 XG3 Output for use in autoranging circuits
Pin 16 Clock (CLK)

Internal RC oscillator of approximately 48kHz providing 3 readings per second. An external oscillator or capacitor may be applied between CLK and TEST to alter the timing.

Connecting CLK to TEST implements elementary form of display hold function by stopping the clock and preventing information update. Prolonged use may damage the LCD due to steady DC levels being present in this mode.

Pin 17 Not used
Pin 18 LCD symbol drive output (XDP)

Square wave in antiphase to BP, may be connected to any combination of LCD symbols or decimal points for indication.

Pin 19 XB3 Output for use in autoranging circuits
Pin 20 TEST Internal digital ground which may be used as the negative supply for external circuits, subject to 1mA maximum load.

When TEST is connected to V+ the main LCD digits will be turned on, with the test pattern shown in Figure 3. (If POL is connected to polarity bar–, this will also be turned on). The display test should not be activated for extended periods.

Pin 21 S2
Pin 22 S1 Negative Supply Generator

Auxiliary power supply connections to enable the instrument to measure true single ended signal with IN LO connected to SUPPLY V_{SS}.

Pin LMP2
Pin LMP1 Not used

Pins 23-40 LCD annunciators
–, :, ~, DP3, DP2, DP1, k, M, Ω, m, A, °C, °F, g, V, %, μ, pH

Direct connections to the LCD segments, any combination of which may be turned on by connecting to XDP. Connection to BP permanently turns off the segments.

Solder pads are provided at strategic points on the module which may be bridged to eliminate wiring otherwise required to establish a particular mode of operation.

Solder pads function

a COM to IN LO
b REF LO to IN LO
c REF– to REF LO
d REF+ to REF HI
e POL to –
f Automatic LOW BATT indication is provided by a normally bridged pad which may be cut if not required or the indication may be controlled by external circuitry.
g Com to REF LO.
h For modifying R10 value - see text.
j V_{SS} to S2. Link for single-ended operation.
XDP In addition to the output at the main edge connector, XDP annunciator drive pads are provided between alternate pairs of annunciator connections, for convenient commitment of them by solder bridging if required.
L1 IN HI signal input link on reverse side of pcb.

Figure 2 **Pcb pin connection diagram**

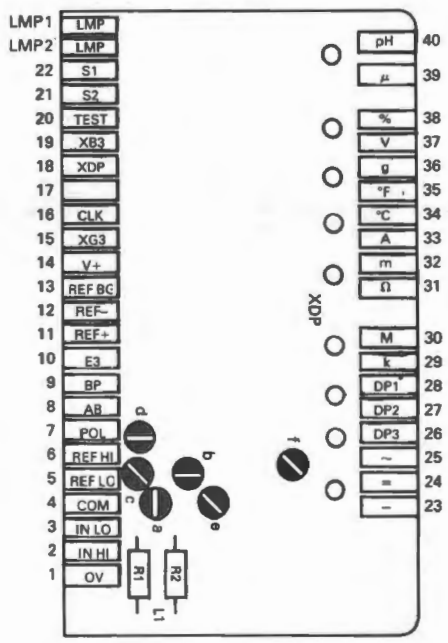
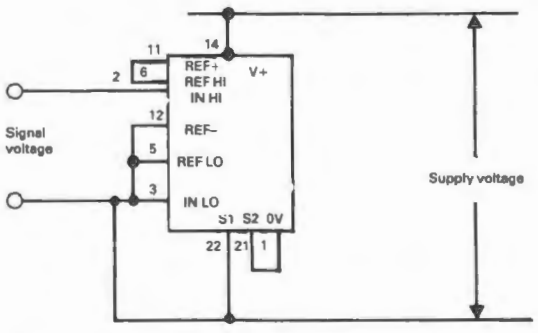


Figure 3 **Display in 'TEST' condition**

Application circuits

Figure 4 **Measurement of single-ended inputs**



All links may be achieved using the pads provided.

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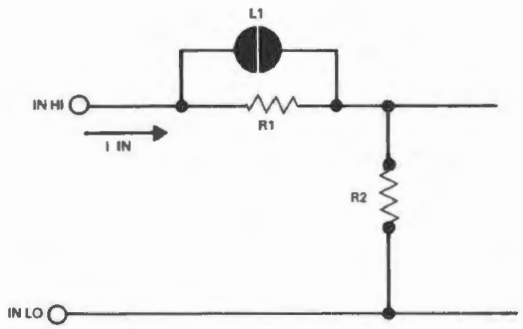
Figure 5 **Alternative full scale reading**



Voltage attenuator or current shunt components may be added as shown to alter the full scale reading. (10M value may be used for R1 with adjustment of the trimmer provided.)

Full scale	L1/R1	R2
200mV	LINK	–
2V	9M	1M
20V	9M9	100K
200V	9M99	10K
2000V	9M999	1K
200uA	LINK	1K
2mA	LINK	100R
20mA	LINK	10R
200mA	LINK	1R
2A	LINK	OR1

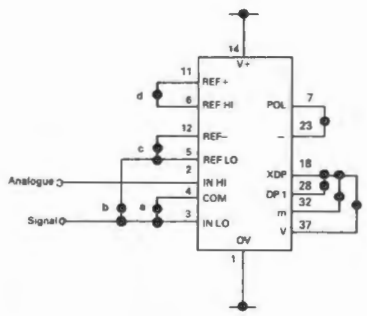
Voltage Input:

$$\text{Full scale} = 2000 \times \frac{R1 + R2}{R2}\ \text{mV}$$

Current input:

Meter input voltage = $I_{IN} \times R_2$

Figure 6 **Measurement of floating voltage with 200mV full scale and annunciators**



Using the solder-bridge connections only four wires are required for signal and supply.

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4½ digit DPM i.c. 7129

Stock number 300-192

The 7129 is a very high-performance 4½-digit analogue-to-digital converter that directly drives a multiplexed liquid crystal display. This single-chip CMOS integrated circuit requires only a few passive components and a reference to operate. And it is ideal for high-resolution hand-held digital multimeter applications.

The performance of the 7129 has not been equalled before in a single-chip A/D converter. The successive integration technique used in the 7129 results in accuracy better than 0.005% of full-scale and resolution down to 10μV/count.

The 7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a 'LOW BATTERY' condition. Autoranging instruments can be made with the 7129 which provides overrange and underrange outputs and 10:1 range changing input. The 7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible signal. These features and the high performance of the 7129 make it an extremely versatile and accurate instrument-on-a-chip.

Absolute maximum ratings

Supply voltage (V^+ to V^-) — 15V
Reference and input voltage
HI or LO inputs — V^+ to V^-
V_{DISP} — V^+ to DGND −0.3V
Digital input pins 1, 2, 19, 20, 21, 22, 27, 37, 38, 39, 40 — DGND to V^+
Power dissipation — 800mW
Operating temperature range — 0°C to +70°C
Storage temperature range — −65°C to +160°C
Lead temperature soldering — 300°C

Electrical characteristics

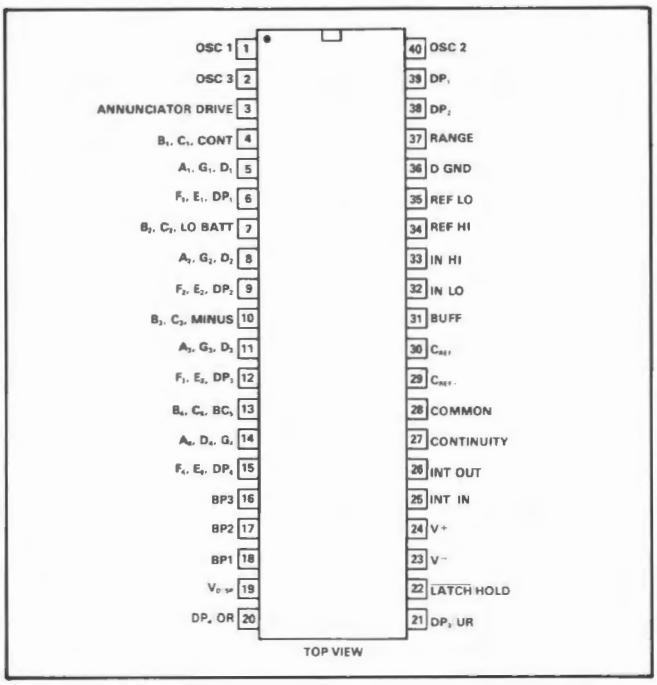
V^+ to V^- = 9V, V_{REF} = 1.00V, T_A = +25°C, f_{CLK} = 120KHz unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
Supply voltage range	V^+ to V^-	6	9	14	V
Supply current excluding common current	V^+ to V^- = 9V		1.0	1.4	mA
Zero input reading	V_{IN} = 0V, 200mV scale	−0000	0000	+0000	Reading
Zero reading drift	V_{IN} = 0V, 0°C < T_A < 70°C		±0.5		uV/°C
Ratiometric reading	V_{IN} = V_{REF} = 1000mV, Range = 2V	9998	9999	10000	Reading
Range change accuracy	V_{IN} = 0.10000V on low range: V_{IN} = 1.0000V on high range	0.9999	1.0000	1.0001	Ratio
Rollover error	$-V_{IN}$ = $+V_{IN}$ = 199mV		0.5	1.0	Counts
Linearity error	200mV scale		0.5		Counts
Input common-mode rejection ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV scale		110		dB
Input common-mode voltage range	V_{IN} = 0V, 200mV scale	(V^-)+1.5		(V^+) −0.5	V
Noise (P-P value not exceeding 95% of time)	V_{IN} = 0V, 200mV scale		7.0		μV
Input leakage current	V_{IN} = 0V, Pins 32, 33		1	10	pA
Scale factor temp. coefficient	V_{IN} = 199mV, 0°C<T_A<+70°C, External V_{REF} = 0ppm/°C		2	5	ppm/°C
Common voltage	V^+ to pin 8	2.8	3.2	3.5	V
Common sink current	Δ common = +0.1V		0.6		mA
Common source current	Δ common = −0.1V		12		μA

Parameter	Conditions	Min	Typ	Max	Units
DGND voltage	V^+ to pin 36, V^+ to V^- = 9V	4.5	5.3	5.8	V
DGND sink current	△ DGND = +0.5V		1.2		mA
Clock frequency			120	360	KHz
Display multiplex rate	f_{CLK} = 120KHz		100		Hz
V_{DISP} Resistance	V_{DISP} to V^+		50		KΩ
Low battery flag activation voltage	V^+ to V^-	6.3	7.2	7.7	V
Continuity comparator threshold voltages	V_{OUT} pin 27 = HI V_{OUT} pin 27 = LO	100	200 200	 400	mV mV
Pull-down current	Pins 37, 38, 39		2	10	μA
'Weak output' current sink/source	Pins 20, 21		3/3		μA
	Pin 27 sink/source		3/9		μA
Pin 22 source current			40		μA
Pin 22 sink current			3		μA

Features

- Converter accurate to ±1 count over full range
- 10μV resolution on 200mV scale
- Direct LCD display drive, including decimal points
- True differential input
- Overrange and underrange outputs
- Low battery detection and indication
- 10 : 1 range change input



Operation

The 7129 is a uniquely designed single-chip A/D converter. It features a new 'successive integration' technique to achieve 10μV resolution on a 200mV full-scale range. To achieve this resolution a 10 : 1 improvement in noise performance over previous monolithic CMOS A/D converters was accomplished. Previous integrating converters used an external capacitor to store an offset correction voltage. This technique worked well but greatly increased the equivalent noise bandwidth of the converter. The 7129 removes this source of error (noise) by not using an auto-zero capacitor. Offsets are instead cancelled using digital techniques. Savings in external parts cost are realised as well as improved noise performance and elimination of a source electromagnetic and electrostatic pick-up.

The overall block diagram of the 7129 is shown in Figure 1. The heart of this A/D converter is the sequence counter/decoder which drives the control logic and keeps track of the many separate phases required for each conversion cycle.

The sequence counter is constantly running and is a separate counter from the up/down results counter which is activated only when the integrator is de-integrating. At the end of a conversion the data remaining in the results counter is latched, decoded and multiplexed to the liquid crystal display.

The analogue section block diagram shown in Figure 2 includes all of the analogue switches used to configure the voltage sources and amplifiers in the different phases of the cycle. The input and reference switching schemes are very similar to those in other less accurate integrating A/D converters. There are five basic configurations used in the full conversion cycle. Figure 3 illustrates a typical waveform on the integrator output. INT, INT_1, and INT_2 all refer to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage.

Figure 1 **Simplified block diagram of 7129 digital section**

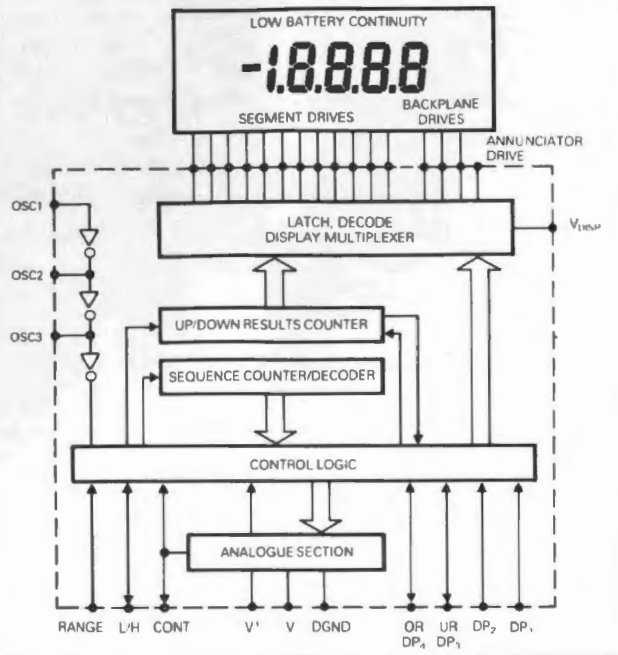


Table 1 **Pin assignments and functions**

PIN	NAME	FUNCTION
1	OSC1	Input to first clock inverter.
2	OSC3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments
8	A_2, G_2, D_2	Output to display segments
9	F_2, E_2, DP_2	Output to display segments
10	B_3, C_3, MINUS	Output to display segments
11	A_3, G_3, D_3	Output to display segments
12	F_3, E_3, DP_3	Output to display segments
13	B_4, C_4, BC_5	Output to display segments
14	A_4, D_4, G_4	Output to display segments
15	F_4, E_4, DP_4	Output to display segments
16	BP3	Backplane #3 output to display.
17	BP2	Backplane #2 output to display.
18	BP1	Backplane #1 output to display.
19	V_{DISP}	Negative rail for display drivers.
20	DP_4/OR	INPUT: When HI, turns on most significant decimal point. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	INPUT: Second most significant decimal point on when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{\text{LATCH}}$/HOLD	INPUT: When floating, A/D converter operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal, and positive rail for display drivers
25	INT IN	Input to integrator amplifier
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	INPUT: When LO continuity flag on the display is off. When HI,continuity flag is on OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	Sets common-mode voltage of 3.2V below V^+ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	$C_{REF}+$	Positive side of external reference capacitor.
30	$C_{REF}-$	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference voltage input terminal.
36	DGND	Ground reference for digital section.
37	RANGE	3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP_2	Internal 3μA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3μA pull-down. When HI, decimal point 1 will be on.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

DE_1, DE_2, and DE_3 are the de-integrate phases where the reference capacitor is switched in series with the buffer amplifier and the integrator ramps back down to the level it started from before integrating. However, since the de-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The 7129 amplifies this overshoot by 10 and DE_2 begins. Similarly DE_2's overshoot is amplified by 10 and DE_3 begins. At the end of DE_3 the results counter holds a number with 5½ digits of resolution. This was obtained by feeding counts into the results counter at the 3½ digit level during DE_1, into the 4½ digit level during DE_2 and the 5½ digit level for DE_3. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted and subtracting the results from the original reading. For this phase INT_2 switch is closed to give the same common-mode voltage as the measurement cycle. This assures excellent CMRR. At the end of the cycle the data in the up/down results counter is accurate to 0.005% of full-scale and is sent to the display driver for decoding and multiplexing.

COMMON, DGND, and 'LOW BATTERY'

The COMMON and DGND (Digital GrouND) outputs of the 7129 are generated from internal zener diodes (Figure 4). COMMON is included primarily to set the common-mode voltage for battery operation or for any system where the input signals float with respect to the power supplies. It also functions as a pre-regulator for an external precision reference voltage source. The voltage between DGND and V^+ is the supply voltage for the logic section of the 7129 including the display multiplexer and drivers. Both COMMON and DGND are capable of sinking current from external loads, but caution should be taken to ensure that these outputs are not overloaded. Figure 5 shows the connection of external logic circuitry to the 7129. This connection will work providing that the supply current requirements of the logic do not exceed the current sink capability of the DGND pin. If more supply current is required, the buffer in Figure 6 can be used to keep the loading on DGND to a minimum. COMMON can source approximately 12μA while DGND has no source capability.

The 'LOW BATTERY' annunciator of the displays is turned on when the voltage between V^+ and V^- drops below 7.2V typically. The exact point at which this occurs is determined by the 6.3V zener diode and the threshold voltage of the n-channel

Figure 2 **7129 analogue block diagram**

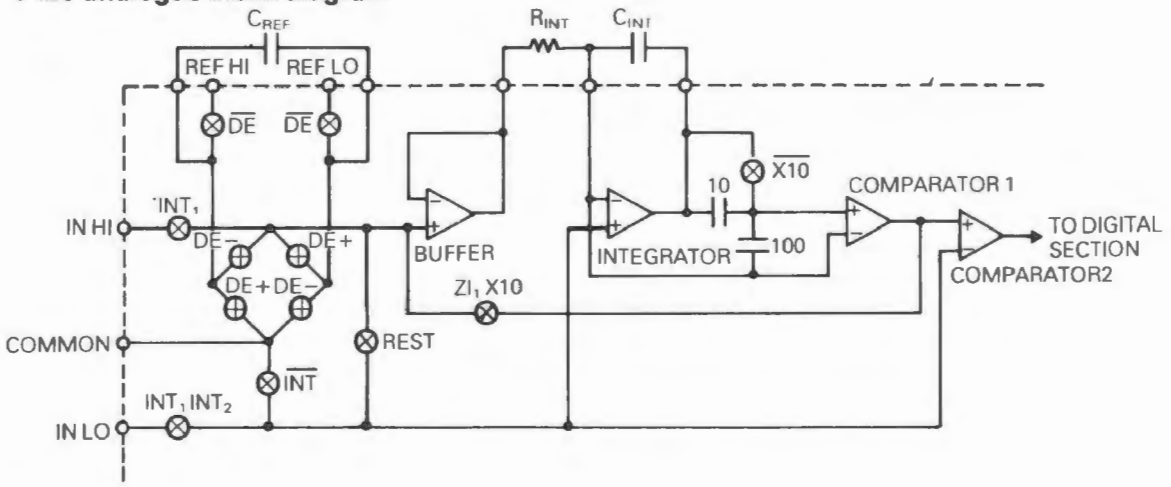
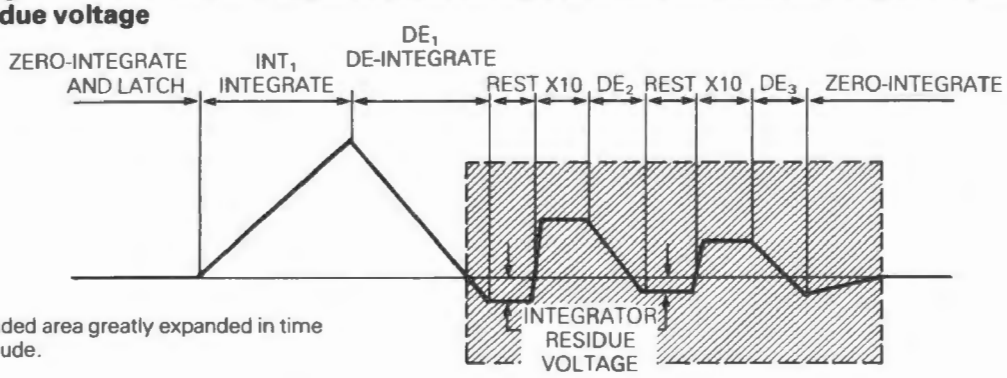


Figure 3 **Integrator waveform for negative input voltage showing successive integration phases and residue voltage**



Note: Shaded area greatly expanded in time and amplitude.

transistor connected to the V^- rail in Figure 4. As the supply voltage increases, the n-channel transistor connected to the V^- rail eventually turns off and the 'LOW BATTERY' input to the logic section is pulled HIGH, turning on the 'LOW BATTERY' annunciator.

Figure 4 **Biasing structure for COMMON and DGND**

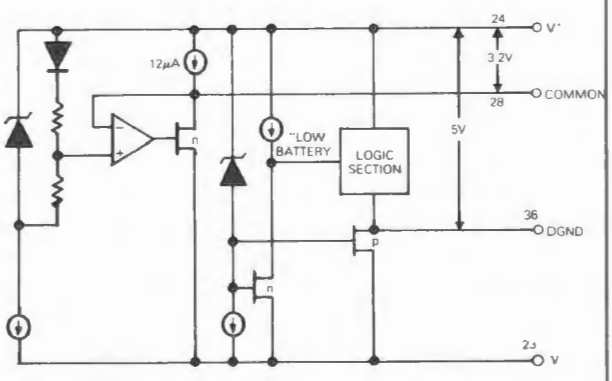


Figure 5 **DGND sink current**

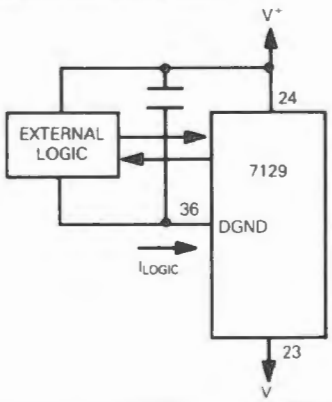
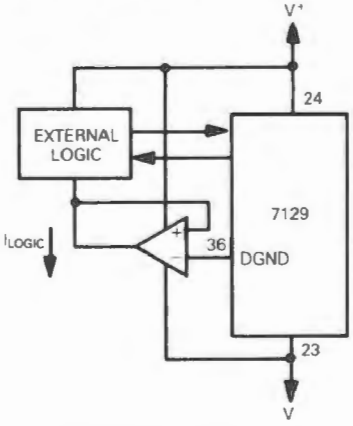


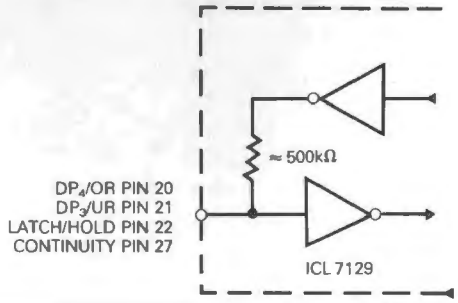
Figure 6 **Buffered DGND**



I/O Ports

Four of the pins of the 7129 can be used as either inputs or outputs. The specific pin numbers and functions are described on the Pin Assignments and Functions (Table 1). If the output function of the pin is not desired in an application it can easily be overridden by connecting the pin to V^+ (HI) or DGND (LO). This connection will not damage the device because the output impedance of these pins is quite high. A simplified schematic of these input/output pins is shown in Figure 7. Since there is approximately 500kΩ in series with the output driver, the pin (when used as an output) can only drive very light loads such as 4000 series, 74HCXX type CMOS logic, or other high input impedance devices. The output drive capability of these four pins is limited to 3μA, nominally.

Figure 7 **'Weak output'**



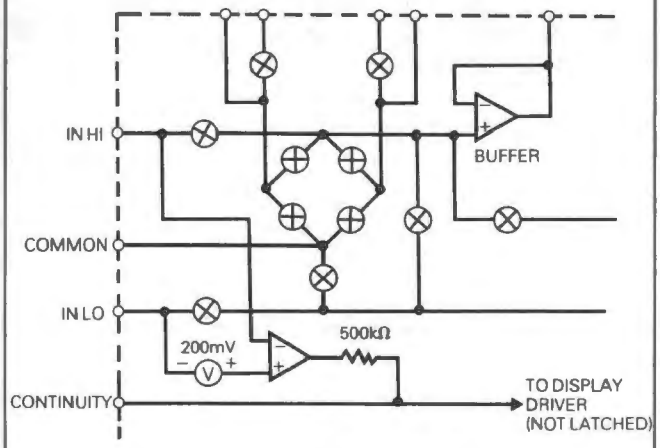
LATCH/HOLD, OverRange, and UnderRange timing

The LATCH/HOLD output (pin 22) will be pulled low during the last 100 clock cycles of each full conversion cycle. During this time the final data from the 7129 counter is latched and transferred to the display decoder and multiplexer. The conversion cycle and LATCH/HOLD timing are directly related to the clock frequency. A full conversion cycle takes 30,000 clock cycles which is equivalent to 60,000 oscillator cycles. OverRange (OR pin 20) and UnderRange (UR pin 21) outputs are latched on the falling edge of LATCH/HOLD and remain in that state until the end of the next conversion cycle. In addition, digits 1 through 4 are blanked during overrange. All three of these pins are 'weak outputs' and can be overridden with external drivers or pull-up resistors to enable their input functions as described in the Pin Assignments and Functions (Table 1).

Instant continuity

A comparator with a built-in 200mV offset is connected directly between INPUT HI and INPUT LO of the 7129 (Figure 8). The CONTINUITY output (pin 27) will be pulled high whenever the voltage between the analogue inputs is less than 200mV. This will also turn on the 'CONTINUITY' annunciator on the display. The CONTINUITY output may be used to enable an external alarm or buzzer, thereby giving the 7129 an audible continuity checking capability. Since the CONTINUITY output is one of the four 'weak outputs' of the 7129, the 'continuity' annunciator on the display can be driven by an external source if desired. The continuity function can be overridden with a pull-down resistor connected between CONTINUITY pin and DGND (pin 36).

Figure 8 **'Instant continuity' comparator and output structure**



Display configuration

The 7129 is designed to drive a triplexed liquid crystal display (588-049) see Figures 9 and 10. The specific display format is shown in Figure 9. Notice that the polarity sign, decimal points, 'LOW BATTERY', and 'CONTINUITY' annunciators are directly driven by the 7129. The individual segments and annunciators are addressed in a manner similar to row-column addressing. Each backplane (row) is connected to one-third of the total number of segments. BP1 has all F, A, and B segments of the four least significant digits. BP2 has all of the C, E, and G segments. BP3 has all D segments, decimal points, and annunciators. The segment lines (columns) are connected in groups of three bringing all segments of the display out on just 12 lines.

Figure 9 **4½ digit triplexed LCD display 588-049**

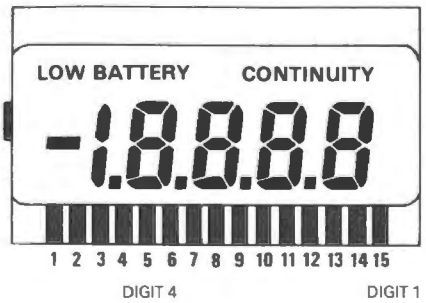


Figure 10 **Connection table**

Pad	1	2	3	4	5	6	7	8	9	10	11	12
Com 1	P4	D4	'1'	P3	D3	–	P2	D2	Low battery	P1	D1	Continuity
Com 2	E4	G4	C4	E3	G3	C3	E2	G2	C2	E1	G1	C1
Com 3	F4	A4	B4	F3	A3	B3	F2	A2	B2	F1	A1	B1

Backplane connections: Com 1 pad 13; Com 2 pad 14; Com 3 pad 15.

Annunciator drive

A special display driver output is provided on the 7129 which is intended to drive various kinds of annunciators on custom multiplexed liquid crystal displays. The ANNUNCIATOR DRIVE output (pin 3) is a squarewave signal running at the backplane frequency, approximately 100Hz. This signal swings from V_{DISP} to V^+ and is in sync with the three backplane outputs BP1, BP2, and BP3. Figure 12 shows these four outputs on the same time and voltage scales.

Any annunciator associated with any of the three backplanes can be turned on simply by connecting it to the ANNUNCIATOR DRIVE pin. To turn an annunciator off connect it to its backplane. An example of a display and annunciator drive scheme is shown in Figure 13.

Figure 11 **Triplexed liquid crystal display layout for 7129**

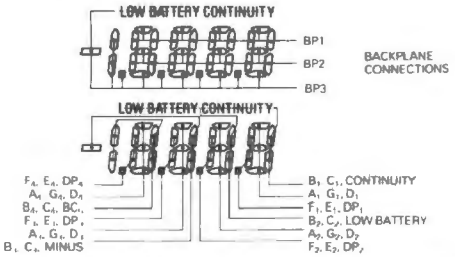
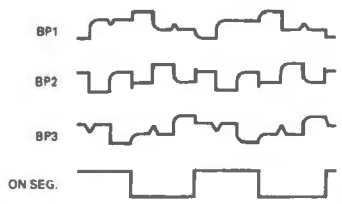


Figure 12 **Typical backplane and annunciator drive waveforms**



Display temperature compensation

For most applications an adequate display can be obtained by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is encountered, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Figure 14 shows two circuits that can be adjusted to give a temperature compensation of $\approx$ +10mV/°C between V^+ and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage to ensure that no forward current is injected on the chip if V_{DISP} is more negative than DGND.

Figure 13 **Multimeter example showing use of annunciator drive output**

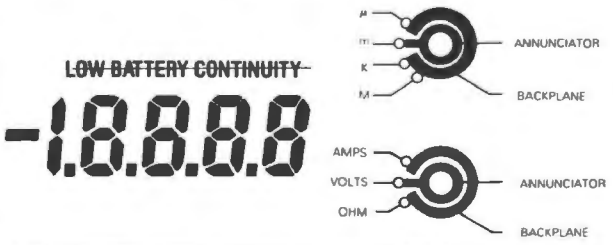
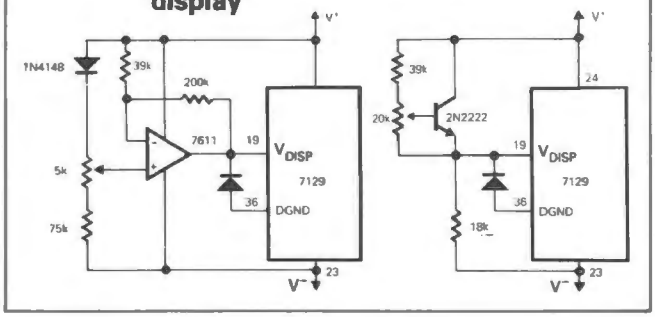


Figure 14 **Two methods for temperature compensating the liquid crystal display**



Component selection

There are only three passive components around the 7129 that need special consideration in selection. They are the reference capacitor, integrator resistor, and integrator capacitor. There is **no** auto-zero capacitor like that found in earlier integrating A/D converter designs.

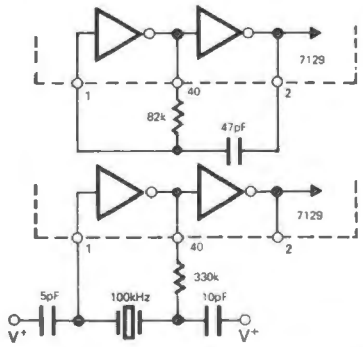
The integrating resistor is selected high enough to ensure good current linearity from the buffer amplifier and integrator and low enough that PC board leakage is not a problem. A value of 150k should be optimum for most applications. The integrator capacitor is selected to give an optimum integrator swing at full-scale. A large integrator swing will reduce the effect of noise sources in the comparator but will affect rollover error if the swing gets too close to the positive rail ($\approx$ 0.7V). This gives an optimum swing of $\approx$ 2.5V at full-scale. For 150k integrating resistor and two conversions per second the value is 0.10μF. For different conversion rates, the value will change in inverse proportion. A second requirement for good linearity is that the capacitor have low dielectric absorption. Polypropylene caps give good performance at a reasonable price. Finally the foil side of the cap should be connected to the integrator output to shield against pick-up.

The only requirement for the reference cap is that it be low leakage. In order to reduce the effects of stray capacitance, a 1.0μF value is recommended.

Clock oscillator

The 7129 achieves its digital range changing by integrating the input signal for 1000 clock pulses (2,000 oscillator cycles) on the 2V scale and 10,000 clock pulses on the 200mV scale. To achieve complete rejection of 60Hz on both scales, an oscillator frequency of 120kHz is required, giving two conversions per second.

Figure 15 **RC and crystal oscillator circuits**



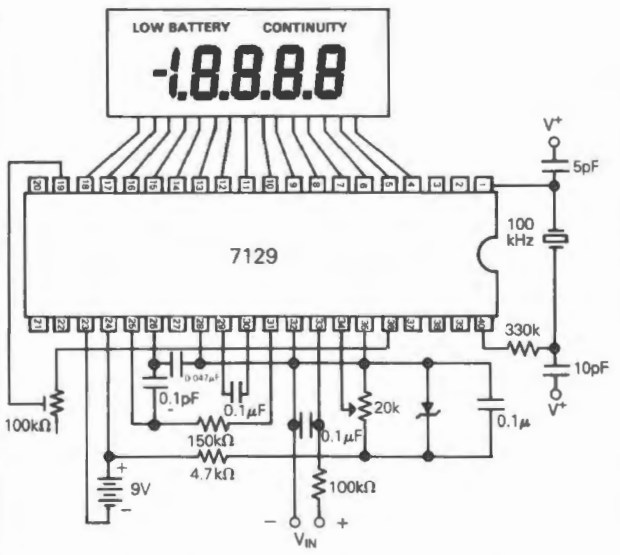
In low resolution applications, where the converter uses only 3½ digits and 100μV resolution, an R-C type oscillator is adequate. In this application a C of 47pF is recommended and the resistor value selected from $f_{OSC} = 0.45/RC$. However, when the converter is used to its full potential (4½ digits and 10μV resolution) a crystal oscillator is recommended to prevent the noise from increasing as the input signal is increased due to frequency jitter of the R-C oscillator. Both R-C and crystal oscillator circuits are shown in Figure 15.

Powering the 7129

The 7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies. Figures 16, 17 and 18 show various powering modes that may be used with the 7129.

The standard battery connection using a 9V battery is shown in Figure 16. The power connection for systems with +5V and −5V supplies available is shown in Figure 17. Notice that measurements are with respect to ground. COMMON is not connected to INPUT LO but is used only as a pre-regulator for the external voltage reference.

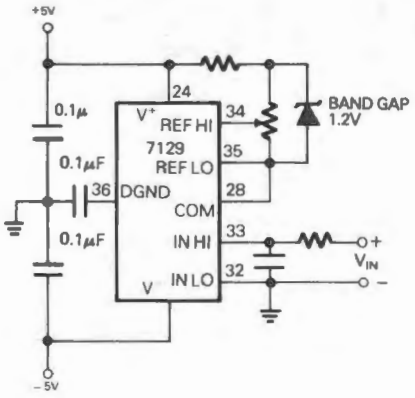
Figure 16 **Typical application**



The 100kΩ preset potentiometer is used to adjust display contrast.

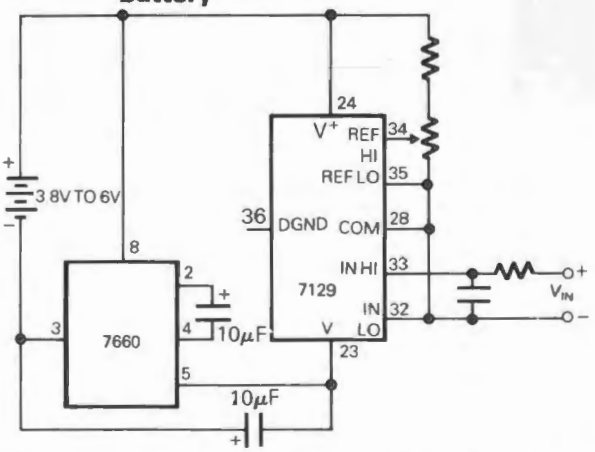
It is important to notice that in Figure 17 digital ground of the 7129 (DGND pin 36) is **not** directly connected to power supply ground. DGND is set internally to approximately 5V less than the V^+ terminal and is not intended to be used as a power input pin. It may be used as the ground reference for external logic, as shown in Figures 5 and 6. In Figure 5, DGND is used as the negative supply rail for external logic provided that the supply current for the external logic does not cause excessive loading on DGND. The DGND output can be buffered as shown in Figure 6. Here, the logic supply current is shunted away from the 7129 keeping the load on DGND low. This treatment of the DGND output is necessary to ensure compatibility when the external logic is used to interface directly with the logic inputs and outputs of the 7129.

Figure 17 **Powering the 7129 from +5V and −5V power supplies**



When a battery voltage between 3.8V and 6V is desired for operation, a voltage doubling circuit should be used to bring the voltage on the 7129 up to a level within the power supply voltage range. This operating mode is shown in Figure 18.

Figure 18 **Powering the 7129 from a 3.8V to 6V battery**



Again measurements are made with respect to COMMON since the entire system is floating. Voltage doubling is accomplished by using a 7660 CMOS voltage converter and two inexpensive electrolytic capacitors. The same principle applies in Figure 19 where the 7129 is being used in a system with only a single +5V power supply. Here measurements are made with respect to power supply ground.

A single polarity power supply can be used to power the 7129 in applications where battery operation is not appropriate or convenient **only** if the power supply is **isolated** from system ground. Measurements must be made with respect to COMMON or some other voltage within its common-mode range.

Voltage references

The COMMON output of the 7129 has a temperature coefficient of ±80ppm/°C typically. This voltage is only suitable as a reference voltage for applications where ambient temperature variations are expected to be minimal. When the 7129 is used in most environments, other voltage references should be considered. Figure 16 shows a 1.2V

band-gap voltage source used as the reference for the 7129 and the COMMON output as its pre-regulator. The reference voltage for the 7129 is set to 1.000V for both 2V and 200mV full-scale operation.

Figure 20 shows another method for generating precision references that are compatible with the 7129. Both reference voltage and input voltage are connected to power supply ground. The voltage drop across $R_1 \approx 2.8V$ to minimise rollover error caused by stray capacitance charging or discharging the reference capacitor. The reference voltage in this case is taken with respect to V^+ and is adjusted with the trim potentiometer connected to REF LO (pin 35).

Figure 19 **Powering the 7129 from a single polarity power supply**

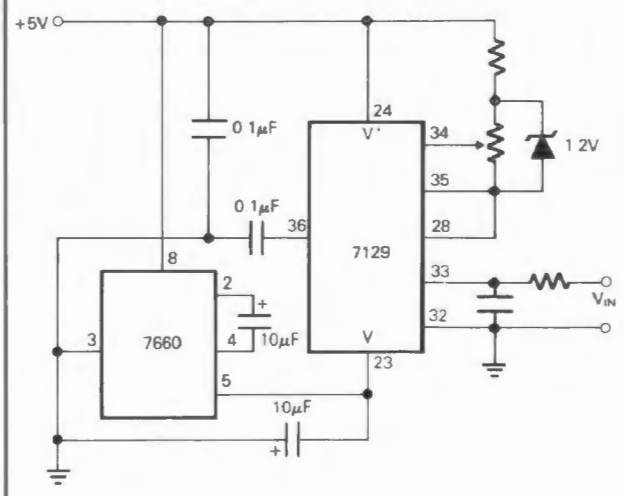
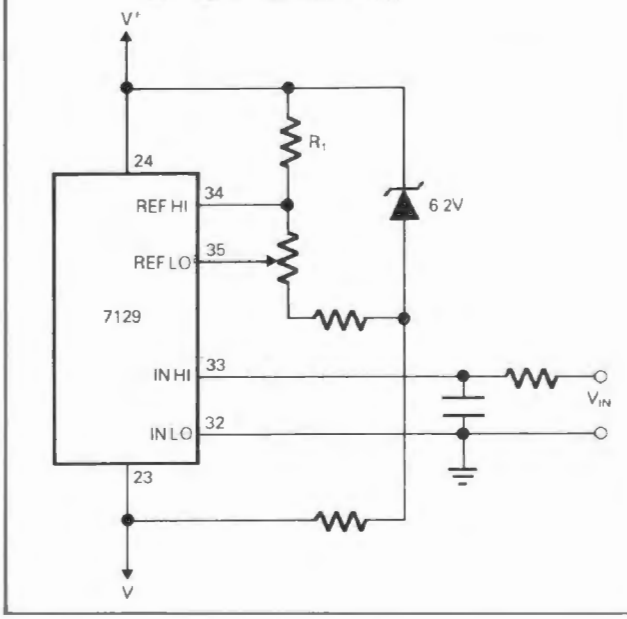


Figure 20 **Using a 6.2V reference diode or 6.2V ZN ref with the 7129**



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RS data

Ultra high speed operational amplifier 5539

Stock number 300-221

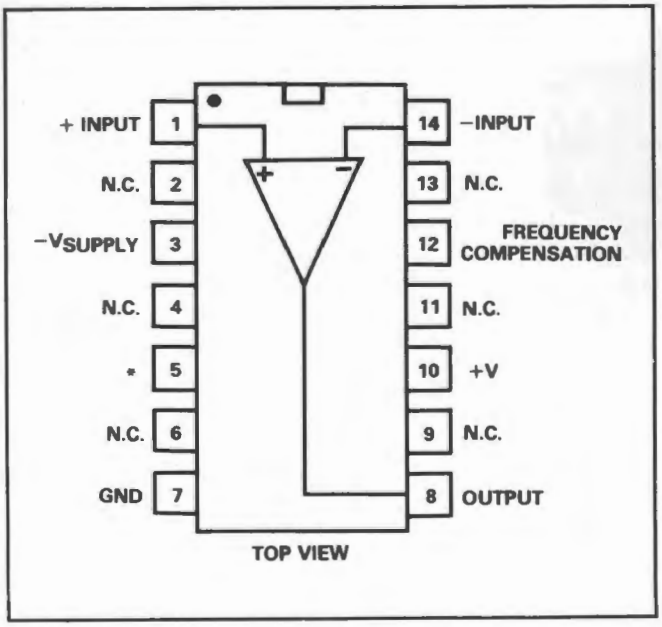
The RS 5539 is a very wide bandwidth, high slew rate op-amp. It features emitter follower inputs to provide a true differential high input impedance. External frequency compensation allows operation over a wide range of closed loop gains, both inverting and non-inverting, and this together with the gain bandwidth product of 1.2 GHz (at 17 dB) and slew rate of 600 V/μs make it ideally suited for use in video amplifiers, r.f. amplifiers and extremely high slew rate amplifiers.

Absolute maximum ratings

Supply voltage	±12V
Internal power dissipation	550mW
Storage temperature range	–65°C to +150°C
Junction temperature	+150°C
Operating temperature range	0 to +70°C
Lead temperature (soldering)	+300°C

Features

- Gain bandwidth product: 1.2GHz at 17dB
- Slew rate: 600V/μsec
- Full power response: 48MHz
- A_{VOL}: 52dB typical



AC ELECTRICAL CHARACTERISTICS V_{CC}= ±8V, R_L= 150Ω to GND & 470Ω to – V_{CC} unless otherwise specified.

PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
Gain bandwidth product	A_{CL} = 7 V_O = 0.1 Vp-p		1200		MHz
Small signal bandwidth	A_{CL} = 2 R_L = 150Ω[1]		110		MHz
Settling time	A_{CL} = 2 R_L = 150Ω[1]		15		nSec
Slew rate	A_{CL} = 2 R_L = 150Ω[1]		600		V/μSec
Propagation delay	A_{CL} = 2 R_L = 150Ω[1]		7		nSec
Full power response	A_{CL} = 2 R_L = 150Ω[1]		48		MHz
Full power response	A_V = 2, R_L = 150Ω[1]		20		MHz
Wide band noise (RMS)	B_W = 5MHz, R_S = 50Ω		4		nV/√ Hz

NOTE 1: External compensation.

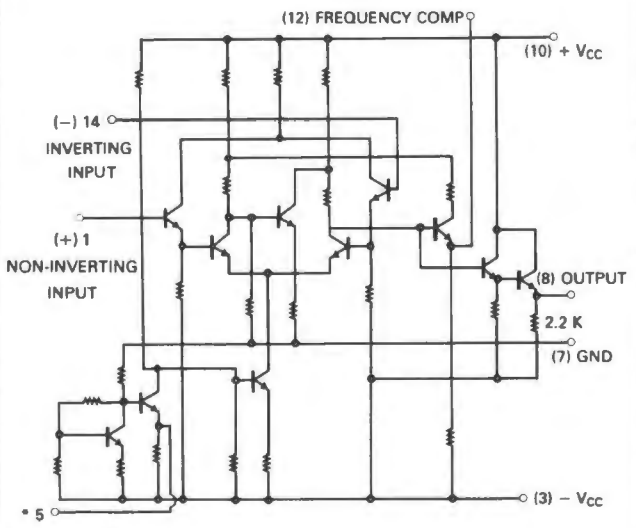
DC ELECTRICAL CHARACTERISTICS V_{CC} = ±8V, T_A = 25°C unless otherwise specified

PARAMETER		TEST CONDITIONS		Min	Typ	Max	UNIT
V_{OS}	Input offset voltage	V_O = OV, R_S = 100Ω			2.5	5	mV
$\Delta V_{OS}/\Delta T$					5		µV/°C
I_{OS}	Input offset current					2	µA
$\Delta I_{OS}/\Delta T$					.5		nA/°C
I_B	Input bias current				5	20	µA
$\Delta I_B/\Delta T$					10		nA/°C
CMRR	Common mode rejection ratio	F = 1kHz, R_S = 100Ω, V_{CM} ± 1.7V		70	80		dB
R_{IN}	Input impedance				100		kΩ
R_{OUT}	Output impedance				10		Ω
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 470Ω to − V_{CC}	+ Swing	+2.3	+2.7		V
			− Swing	−1.7	−2.2		V
I_{CC}+	Positive supply current	V_O = O, R_1 = ∞			14	18	mA
I_{CC}−	Negative supply current	V_O = O, R_1 = ∞			11	15	mA
PSRR	Power supply rejection ratio	ΔV_{CC} = ± 1V			200	1000	µV/V
A_{VOL}	Large signal voltage gain	V_O = +2.3V, −1.7V R_L = 150Ω to GND, 470Ω to −V_{CC}		47	52	57	dB
A_{VOL}	Large signal voltage gain	V_O = +2.3V, −1.7V R_L = 2K to GND		47	52	57	dB

NOTE

1 Differential imput voltage should not exceed 0.25 volts to prevent excessive input bias current and common mode voltage 2.5 volts. These voltage limits may be exceeded if current limit is 10mA

Figure 1 **Equivalent circuit**



*optional gain control pin in open loop operation.

Figure 2 **Open loop phase**

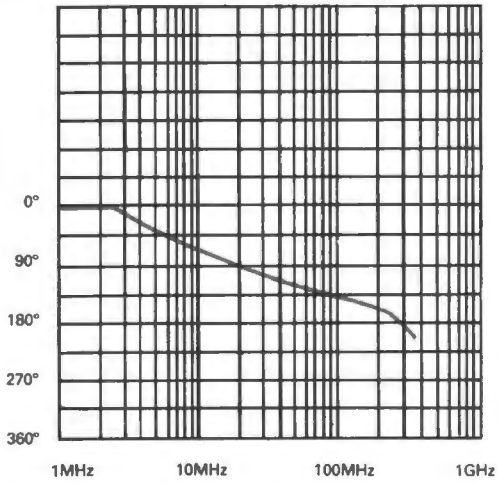


Figure 3 **Open loop gain**

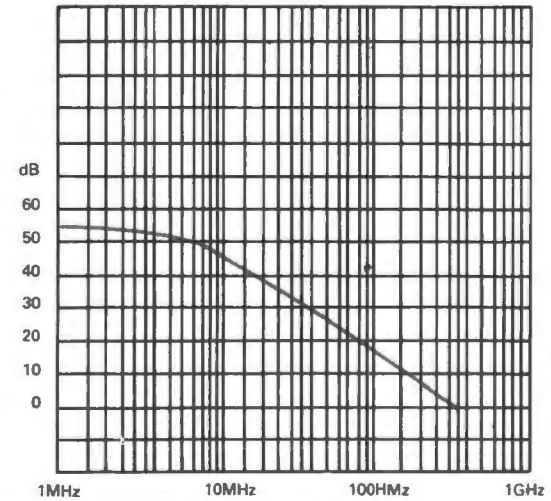


Figure 4: **Power bandwidth**

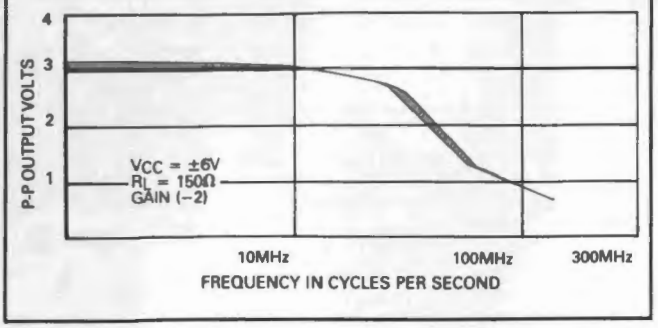


Figure 5: **Power bandwidth**

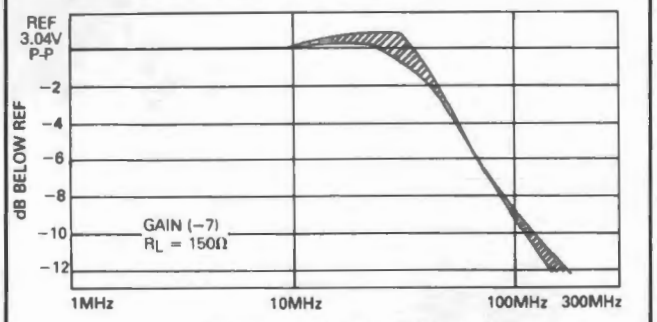
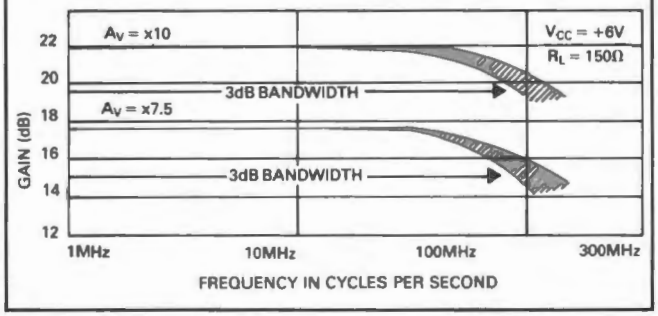


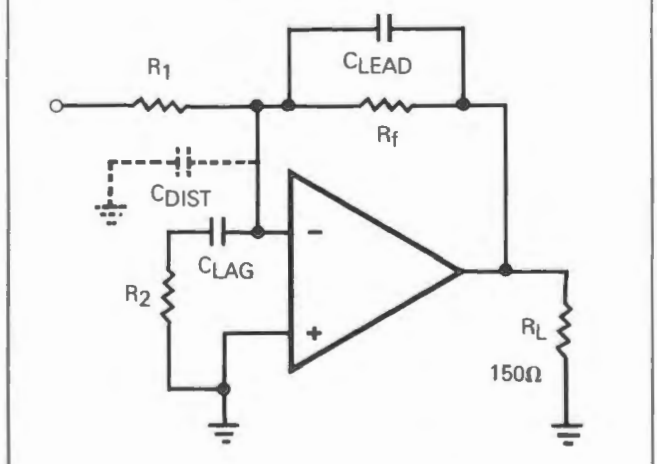
Figure 6 **Gain bandwidth product as a function of frequency**



Compensation for closed loop gain of less than 7 (17dB)

The 5539 is stable for all closed loop gains greater than seven (17dB). When operating at gains less than seven, the device can become unstable. The circuit in Figure 7 is one example of a unity gain inverting amplifier. The compensation components are added to obtain stable operation.

Figure 7: **Inverting amplifier circuit**



Capacitor C_{LEAD} improves the phase margin of the operational amplifier by compensation for the lag introduced by the distributed capacitor (C_{DIST}).

It can be shown that the optimal conditions for amplifier stability occur when $R_1 C_{DIST} = R_F C_{LEAD}$. However, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed loop amplifier will be reduced.

The actual value for C_{LEAD}, based on a distributed capacitance of 3.5pF and a gain of 1, would be ≃ 3.5pF.

Another way of stating the relationship between the distributed capacitance, closed loop gain (A_{CL}), and the lead compensation capacitor is:

$$C_{LEAD} = \frac{C_{DIST}}{A_{CL}}$$

Also,

$$C_{LEAD} = \frac{1}{2\pi (GBW) R_F}$$

can be used to approximate C_{LEAD} where GBW is the unity gain bandwidth or cross-over frequency, which is ≃350MHz.

For closed loop stability and gains less than 5, C_{LEAD} become a practical consideration. When bandwidth is of primary concern, the simple lead compensation will usually be adequate.

However, if transient response is also a factor in the design, then a lag compensation network (C_{LAG}, R_2) may be necessary.

For practical applications, the following equations can be used to determine the proper lag compensation components:

$$\frac{R_F}{R_1 \| R_2} \geq 7 \qquad (1)$$

$$\therefore R_2 \leq \frac{R_F}{7 - A_{CL}} \qquad (2)$$

Using Equation 1 to insure a closed loop gain of 7 above the network break frequency allows you to solve for R_2, the lag network resistor.

C_{LAG} may be approximated by the following equations. First set the lag network break frequency in relation to the amplifier unity gain product or crossover frequency of approximately 350MHz.

$$\text{Set } W_{LAG} \simeq \frac{2\pi (GBW)}{10} \text{ rad/sec}$$

$$\simeq \frac{\pi (GBW)}{5} \text{ rad/sec}$$

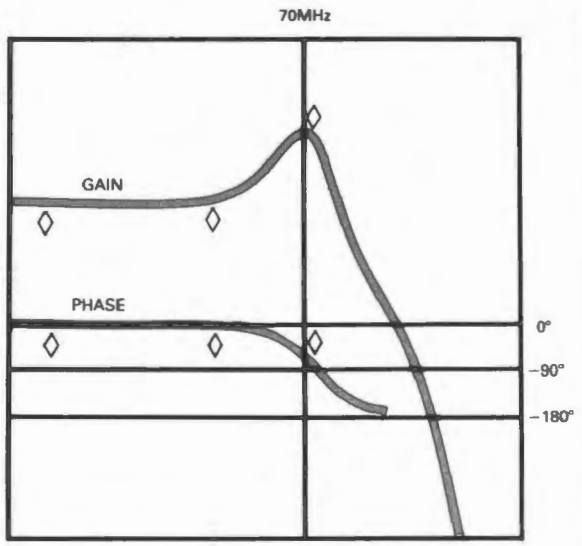
$$\text{Where } W_{LAG} = \frac{1}{R_2 C_{LAG}}$$

$$\therefore \frac{1}{R_2 C_{LAG}} = \frac{\pi (GBW)}{5}$$

$$\text{And } C_{LAG} = \frac{5}{\pi R_2 (GBW)}$$

The primary reasoning behind this procedure is to force the closed loop circuit to appear as a gain of 7 above the critical frequency where phase changes rapidly (approximately 70MHz); refer to Figure 8.

Figure 8: **Inverting gain of 7 gain phase response (uncompensated)**



The lag network raises the phase at the upper operating frequencies, greatly improving the phase margin.

The calculations below show the applications of these principles to the circuit in Figure 9.

The circuit shown has an inverting gain of 2, therefore solving for R_2:

$$R_2 \leq \frac{R_F}{7 - |A_{CL}|} \leq \frac{2K}{7-2} \leq 400$$

Let $R_2 = 330\Omega$

Assuming a gain bandwidth product of 350MHz, C_{LAG} may now be calculated as follows:

$$C_{LAG} \simeq \frac{5}{(\pi)(330)(350.10^6)} \simeq 14pF$$

For lead compensation the following can be used:

$$C_{LAG} \simeq \frac{1}{2\pi (350.10^6)(2K)} \simeq .23pF$$

But since this is smaller than the distributed capacitance, the equation

$$C_{LEAD} = \frac{C_{DIST}}{A_{CL}}$$

will be used (assume $C_{DIST} \simeq 3.5pF$ as used earlier).

$$C_{LEAD} = \frac{3.5pF}{2}$$

$$\simeq 1.8pF$$

In the circuit shown (Figure 9), a 2-22pF trimmer capacitor was used for C_{LAG} to optimize overshoot and reduce ringing.

Rise and fall times of 2.8 to 3ns were measured in the small signal mode.

Pin 12 compensation method

Another method of compensation that works the same as the lag and lead compensation is shown in Figure 10. This form of compensation utilizes Pin 12 and a shunt resistor across the input pins.

This method works as well as the one shown in Figure 9 with the savings of 1 capacitor. For the inverting, R_C should be 720Ω and C_C from 2-6pF. For the non-inverting, R_C should be 200Ω and C_C from 2-6pF.

Typical applications

Figure 9: **Inverting gain of 2 amplifier with lag-lead compensation**

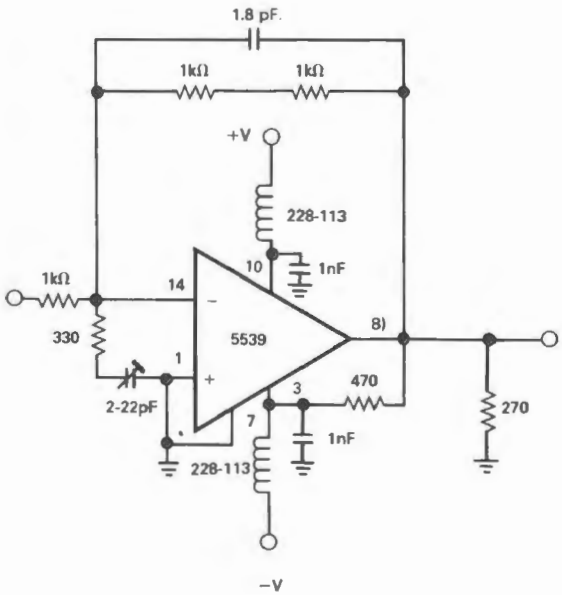
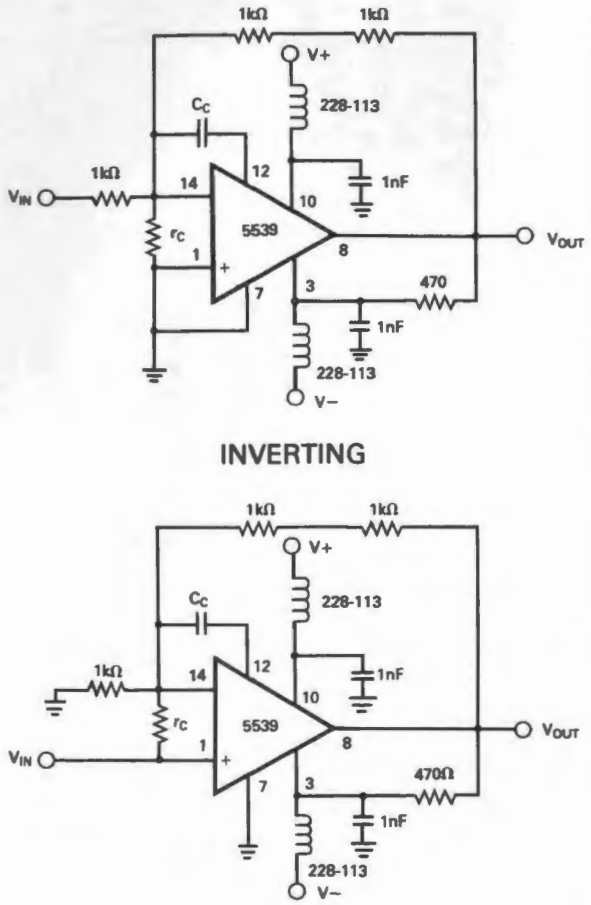


Figure 10 **Pin 12 compensation method**



INVERTING

NON-INVERTING

Figure 11 **Colour video amplifier**

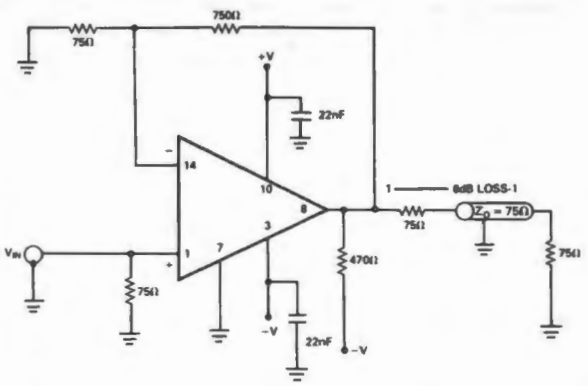


Figure 12 **Non-inverting follower**

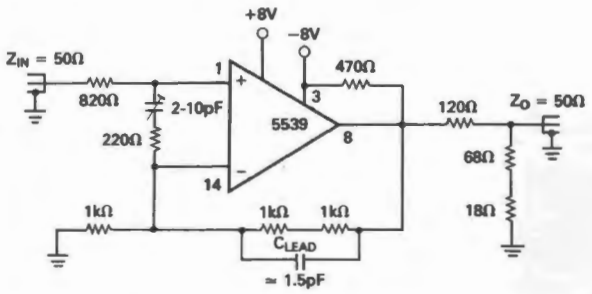
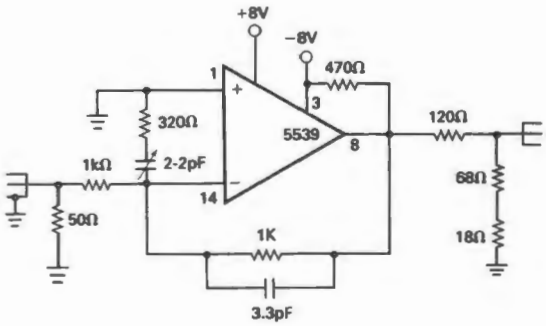


Figure 13 **Inverting follower**



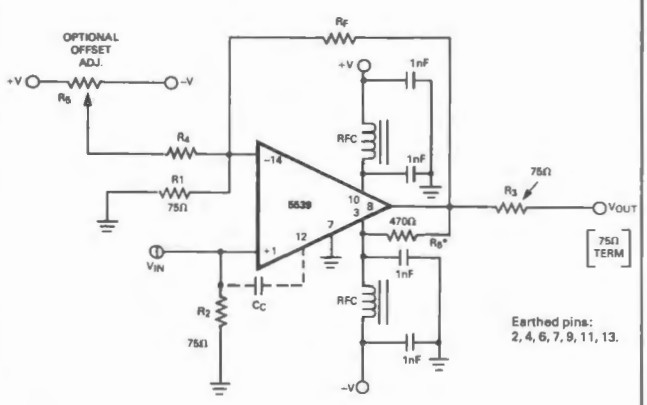
RS data

Circuit layout considerations

As may be expected for an ultra-high frequency, wide gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper clad printed circuit board will result in more favourable system operation.

A suitable double-sided epoxy glass board is available under RS stock number 435-664. When populated in accordance with the circuit diagram and component listing of Figure 14 this will form a wide band 28dB non-inverting amplifier. This printed circuit board has in addition the provision for compensation components providing an excellent basis for further experimentation.

Figure 14

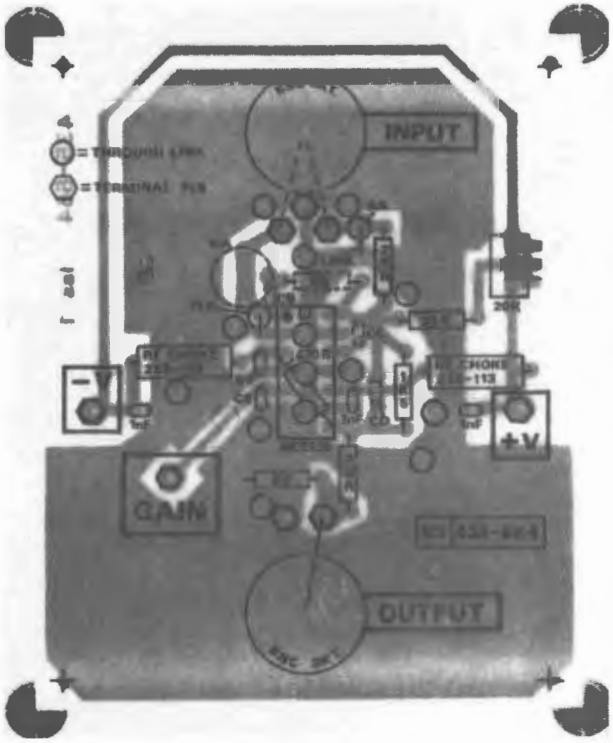


Component List

R1	= 75Ω	(148-225)
R2	= 75Ω	(148-225)
R3	= 75Ω	(148-225)
R4	= 33kΩ	(148-859)
R5	= 20k Cermet Pot	(186-536)
RF	= 1k5	(148-540)
R6*	= 470Ω	(148-427)
4 x Caps	= 1n	(125-749)
2 x RFC	= 1u, 2.7A	(228-113)
2 x SKT	= BNC	(455-680)
Pins	=	(433-854)

* Note: R6 is mounted on the track side of the pcb.

Figure 15 **Printed circuit board**



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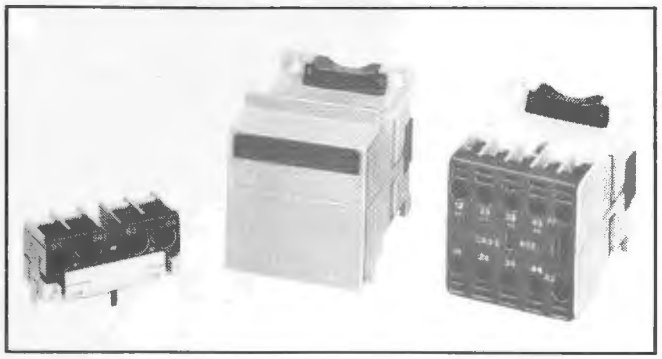
RS data

Control gear components 'E' range



The 'E' range of contactors, control relays and accessories offers the user the maximum flexibility. The compact, modular design looks aesthetically pleasing alongside electronic equipment or when fitted in the purpose-built enclosures to DIN 43 880 as supplied by RS.

Conformity to standards
IEC, 158-1, 337 and 255. VDE 0660, NFC 63-110 and 45-250, BS 5424, JIS C8325, JEM 1038.

Approvals
CSA, UL Listed, NEMKO, DEMKO, SEMKO, ASE, SETI

Environmental protection

Dust/Water (without paralleling links) IP20
n.b. this covers finger and back of hand protection to VDE 0106 part 100.

Ambient temperature:
Operating: ——— −40 to +60°C
Storage: ——— −55 to +70°C

Protective treatment: Suitable for moderate corrosive atmospheres, i.e. those containing ammonia, lime, soda, potassium, etc. This treatment is equivalent to 'Kilmafest' or 'Climateproof'.

Limits of use (to retain protection)

Temperature	°C	20	30	40	45	50	60
Relative humidity	%	95	90	80	60	50	30

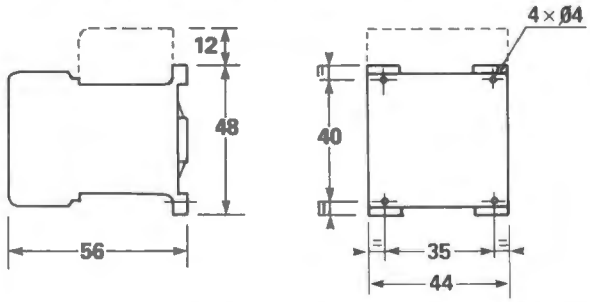
Resistance to vibration
(IEC 68-2-6) On horizontal plane (worst situation)
Energised state:
Maximum acceleration: 8g (10 to 200Hz)
De-energised state:
Maximum acceleration: 3g (10 to 200Hz)

Resistance to shock
(IEC 68-2-27) On horizontal plane (worst situation)
Energised state:
Maximum acceleration: 50g
De-energised state for 11ms duration:
Maximum acceleration: 10g

Features

- Five control voltages available (ac 50/60Hz see table)
- Two contactors (2.2kW and 4.0kW) and three control relays (4N/O, 3N/O + 1N/C, 2N/O + 2N/C) in the same frame size
- Coil changing accomplished in seconds without the need for tools
- Clip-fit auxiliary contact blocks (2N/O or 1N/O + 1N/C) available
- Low consumption coils, average of 40/4VA (inrush/sealed) 50 or 60Hz
- Test facility for checking contactors by manual operation
- Choice of mounting. Directly onto a flat surface, snap-fit on DIN rail (top hat profile) or in purpose built modular housings
- Meets modular dimensions (DIN 43 880) even when auxiliaries are attached

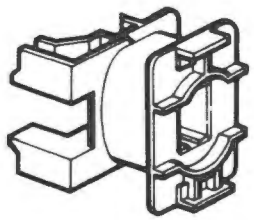
Figure 1 **Contactor and control relay dimensions**



Stock number	Description
345-189	Contactor 5A 2.2kW (AC3)
345-195	Contactor 9A 4.0kW (AC3)
345-202	Control relay 4N/O
345-218	Control relay 3N/O, 1N/C
345-224	Control relay 2N/O, 2N/C
Accessories	
345-280	Modular cover
345-296	Auxiliary contacts 2N/O
345-303	Auxiliary contacts 1N/O, 1N/C
345-319	Paralleling links 2 pole, set of 4
345-325	Paralleling links 4 pole, set of 2

Ordering

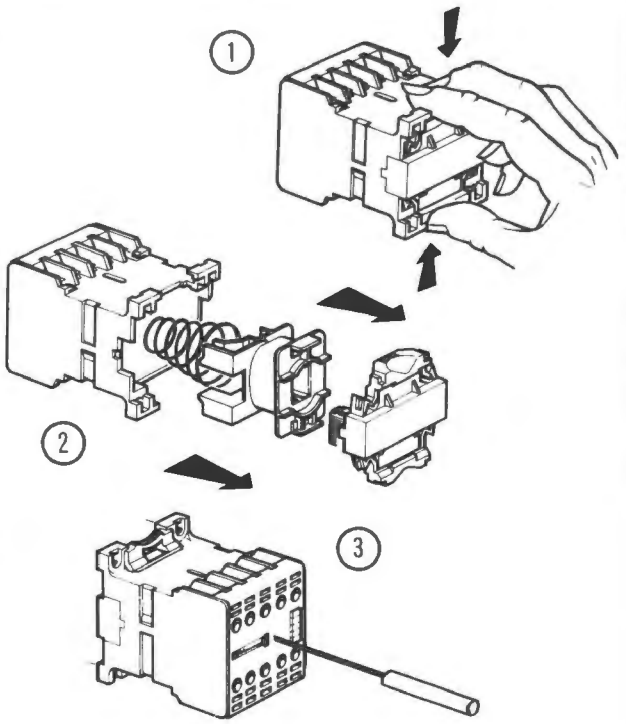
When placing an order for the contactors or control relays the coils are to be ordered separately. The coil size is uniform throughout the range. Care should be exercised in selecting the correct control voltage. Refer to the coil selection table for a complete list of control voltages for 50/60Hz and operating limits.



Control voltage range

Stock No.	Operating Voltages 50Hz	60Hz	Resistance Ω	Closed circuit inductance (H)
345-230	24V	24V	14.7	0.45
345-246	42-48V	48V	55.0	1.65
345-252	100-110V	100-120V	262	8.27
345-268	240-250V	265-277V	1525	48.90
345-274	380-415V	440-480V	4075	132

Figure 2 **Coil adding/changing**



1 Firmly squeeze the base moulding between thumb and forefinger.

2 Pull unit apart. Examination of the upper housing will reveal where the coil contacts are located (directly under markings A1 and A2). When inserting the new coil, check that these contacts mate with their opposite pair on the coil. Ensure that the captive spring is properly seated on the coil moulding. The base will now snap into position (either way round).

3 Insert a small screwdriver in the manual test position and depress to ensure unrestricted movement of the contacts and spring return to the de-energised position.

Note: The control voltage information, printed on the coil moulding, may be read without having to take the unit apart. It may be seen under the finger release mouldings on the base. One side shows the ratings for 50Hz, the other for 60Hz.

Coil characteristics

Average consumption (50 and 60Hz)	Inrush: 40VA Sealed: 4VA
Heat dissipation	Sealed: 1.2W
Power factor	Inrush: cosφ : 0.8 Sealed: cosφ : 0.3

Average operating times with coil voltage Un

On energisation	
Between coil energisation and pole closure	6 to 18ms
Between coil energisation and opening of N/C contact	4 to 13ms
On de-energisation	
Between the coil de-energisation and opening of poles	5 to 19ms
Between the coil de-energisation and re-closing of N/C contacts	7 to 25ms

Operating limits

Permanent maximum voltage ≤ 60°C	110% of Un (1)
Pull-in voltage ≤ 60°C	85% of Un (2)
Pull-in voltage ≤ 40°C	80% of Un (2)
Drop-out voltage	20% to 65% of Un (2)

(1) Maximum operating voltage for appropriate frequency (see 'control voltage range' table).

(2) Minimum operating voltage for appropriate frequency (see 'control voltage range' table).

Maximum time of supply voltage loss without affecting energised state of contactor/relay	3ms
Maximum operating rate	7200 ops/hr

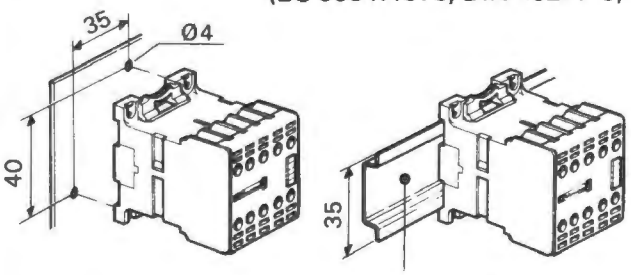
Contactors/Control relays

Choice of mounting

Figure 3 **Mounting options**

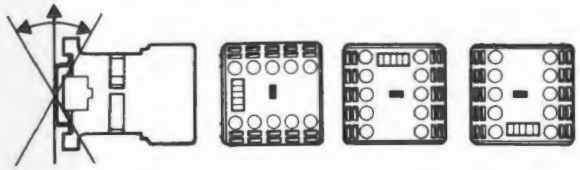
Onto a flat surface

On DIN rail to EN 50022 (BS 5584:1978, DIN 46277-3)



Stock No. 606-838

Operating position
Operation, without derating, up to 30° either side of vertical, in the positions shown



Variation to voltage rating in other positions

−8% on energisation +8% on energisation
−5% on de-energisation +5% on de-energisation

Cabling
Without ferrule* 1 x 0.75 mm² to 2 x 2.5 mm²
With ferrule* 2 x 1 mm² or 1 x 2.5 mm²
*Bootlace ferrules provide a neat end termination to multi-stranded wires and are available from RS (see Connectors section in the catalogue).

Contactors – main poles

(† also applies to control relays)

†Rated insulation voltage
Conforming to IEC 158.1, BS 5424, VDE 0110C, NF C 20-040 660V

Conforming to CSA 22-2 No. 14 600V

†Nominal frequency 50/60 Hz

†Frequency limits 0/400 Hz

†Maximum operating voltage 660V

Making capacity 160A
Conforming to IEC 158.1

Breaking capacity
Conforming to IEC 158.1 (at various operating voltages 50/60 Hz)

220V	380V	415V	440V	500V	660V
100A	100A	100A	100A	90A	80A

Short time rating
Ambient temperature around the component ≤40°C

0.3s	1s	5s	10s	30s	1mn	3mn	15mn
380A	200A	90A	70A	50A	42A	30A	16A

Contact material Silver cadmium oxide alloy

AC1 applications
(Resistive loads, lighting, heating)
Rated thermal current ≤40°C 16A

Rated thermal current ≤60°C 12A

Rated current according to on-load factor and operating rate:

On load factor		90%	60%	30%
Rate of operation	300	10A	12A	14A
(ops/h)	120	12A	14A	15A
	30	15A	16A	16A

Coefficients to apply to increase rated current (AC1) by paralleling poles:
Using 345-319 2 poles in parallel: K = 1.60
Using 345-325 4 poles in parallel: K = 2.80

AC3 applications
(Squirrel cage motors)
AC3 duty‡ (utilisation categories defined in BS 4941: Part 1: 1975)

Stock No.	Operating voltages 50Hz/60Hz		240V 1ph	220/240V 3ph	380/415V 3ph	440/480V 3ph	600/660V 3ph
345-189	Nominal	kW	0.75	1.5	2.2	3.0	3.0
	Motor rating	hp	1.0	2.0	3.0	4.0	4.0
345-195	Nominal	kW	1.1	2.2	4.0	4.0	4.0
	Motor rating	hp	1.5	3.0	5.5	5.5	5.5

‡Valid up to 600 ops/hr
For 900 ops/hr multiply ratings by 0.75, for 1200 ops/hr x 0.5.
For overcurrent, short circuit and phase failure protection a motor circuit breaker is recommended. (See current catalogue – control gear/accessories)

Full load current (FLC) tables

		3 phase motors				
Motor rating hp	kW	FLC at line volts 220V	240V	380V	415V	500V
¼	0.19	1.29	1.19	.75	.68	.5
½	0.37	2.48	2.27	1.43	1.31	1.0
¾	0.56	3.09	2.84	1.78	1.64	1.3
1	0.75	3.5	3.2	2.0	1.8	1.5
1½	1.1	4.9	4.5	2.8	2.6	2.2
2	1.5	6.4	5.8	3.7	3.4	2.8
3	2.2	9.5	8.7	5.5	5.0	3.9
5	3.7	14.6	13.4	8.4	7.7	6.5

Single phase motors				
Motor rating hp	kW	FLC at line volts 110V	220V	240V
1/12	0.07	2.31	1.16	1.06
⅛	0.1	3.15	1.58	1.44
⅙	0.13	4.41	2.21	2.02
¼	0.19	5.88	2.94	2.69
⅓	0.25	7.77	3.88	3.55
½	0.37	11.1	5.56	5.08
¾	0.56	13.7	6.82	6.24
1	0.75	18.9	9.44	8.64

Control relays

The contacts on the control relays are designed for control circuit switching. The wiping action and serrated surfaces ensure reliability particularly for low power switching. The moulding design prevents the closure of a N/O contact set in the event of a N/C set welding. The contacts are marked in accordance with EN50011E (BS 5583:1978) for control relays.

Contact characteristics

Contact relays and auxiliary contact blocks

Rated thermal current 6A

Making and breaking capacity
Conforming to IEC 337.1 Refer to the curves on page 4

Minimum switching capacity
With minimum voltage 6V and minimum current 10mA 0.6VA

Insulation resistance
Between contacts, between contacts and earth, between input and output of an open contact >10MΩ

Mechanical life 5×10^6 ops

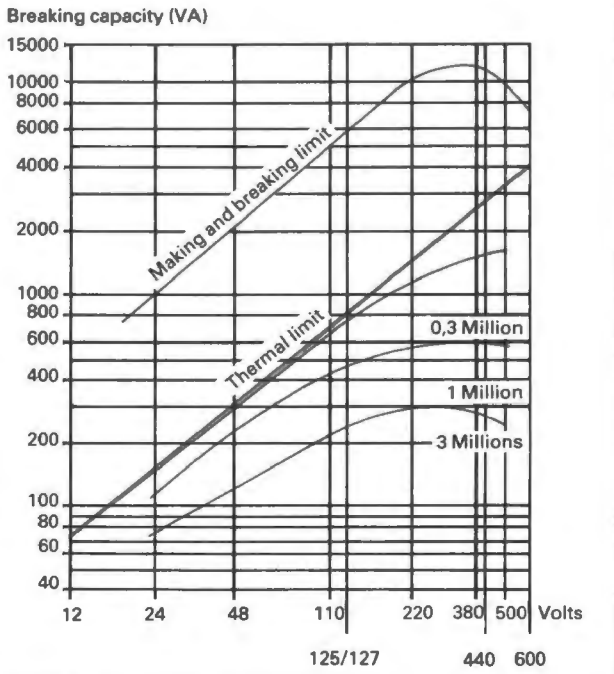
Non-overlap time
Between N/C and N/O contacts on energisation and de-energisation

5617

Control relay/aux. contact block ≥1ms/≥0.3ms

Contact material 90% silver, small percentage cadmium for hardness.

Figure 4 **AC, duty category AC11**

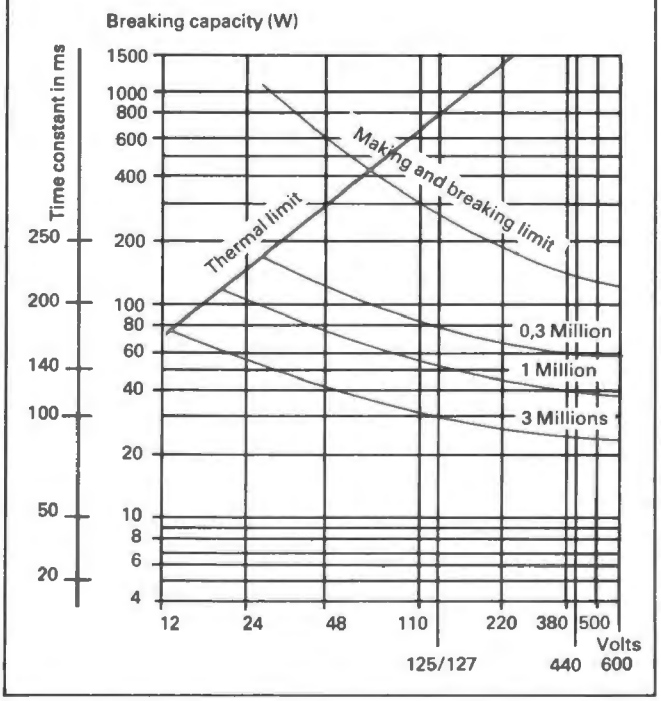


Electrical life (valid up to 1200 ops/hour) on inductive load such as the coil of an electro-magnet: making current (Cos ∅ 0.7) = 10 times the breaking current (Cos ∅ 0.4).

AC Breaking limit of instantaneous and time delay with contacts:

50 operations with at least 10 second intervals (Breaking current = making current; Cos ∅ = 0.7).

Figure 5 **DC, duty category DC11**



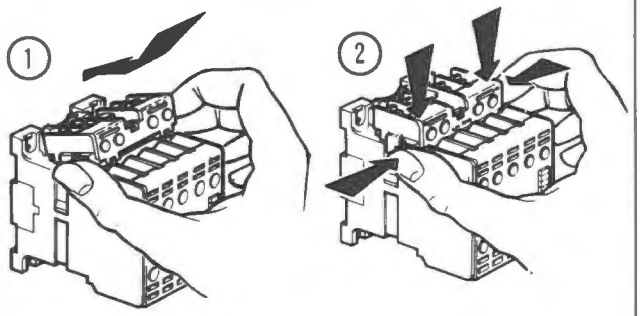
Electrical life (valid up to 1200 ops/hour on inductive load such as the coil of an electro-magnet without economy resistor, the time constant increasing with power.

DC Breaking limit of instantaneous contacts:

20 operations with at least 10 second intervals and with current passing for 0.5 seconds per operation.

Fitting of auxiliary contact blocks

Figure 6 **Auxiliary contact block fitting**



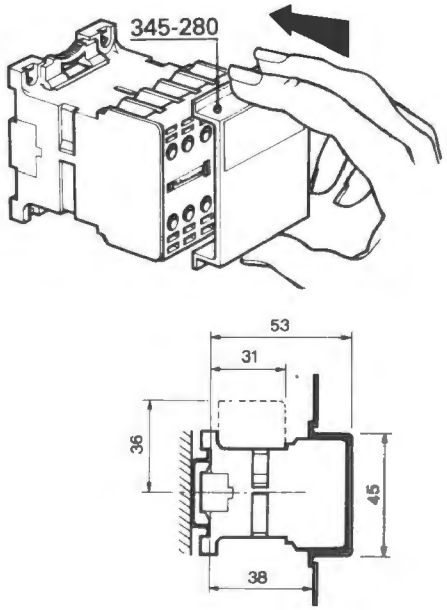
1 Position auxiliary block under the two locating pips, in the finger release moulding, on the base of the contactor/control relay.

2 Press firmly on the top of the auxiliary contact block to snap-fit the side clips.

To release the auxiliary block, exert pressure on the side clip serrations and lift up.

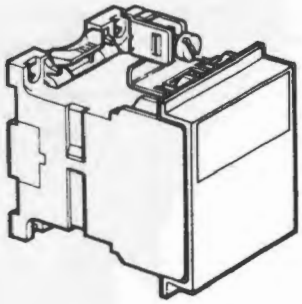
Fitting of modular cover

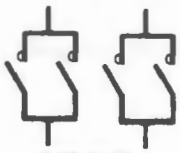
Figure 7 **Modular cover fitting**



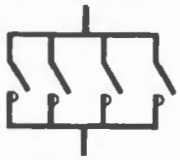
Used to provide complete protection of terminals when the contactor/control relay is mounted in a modular enclosure.

Paralleling links





345-319



345-325

Note: The paralleling links, as supplied by RS, are designed to be used with the modular cover. They cannot be used where an auxiliary contact block is fitted.

Terminal capacities

345-319	2-pole	10mm^2 max.
345-325	4-pole	16mm^2 max.

Modular enclosures

A range of modular enclosures is available from RS (see Equipment housings in the current catalogue). These comply with the specification for Built-In Equipment DIN 43 880.

When ordering an enclosure, the 'modular width' has to be considered.

The E range contactors and control relays are 2½ modules wide (2.5 x 18mm).

Blanking plates are available, to ensure a neat appearance, for unused module space.

5617

RS data

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RS data

Fire alarm system and installation

There are two main reasons for installing fire alarm systems, the protection of life and the protection of property.

Fire can kill or maim in many ways e.g. by asphyxiation, irradiation, poisoning or burning and legislation has come a long way in defining the premises to be protected and standard of fire alarm equipment that should be used. The first requirement is covered by the Fire Precautions Act 1971 and the Health and Safety at Work Act 1974. The second requirement (for equipment standards) is now covered by BS5839 1980 "Fire Detection and Alarm Systems in Buildings" and BS3116 1974 'Automatic Fire Alarm Systems In Buildings.'

BS5839: Pt 1 sets out recommendations for the installation and servicing of fire detection and alarm systems in buildings and is now the accepted code of practice for premises requiring fire protection and detection systems under the Fire Precautions Act 1971.

Throughout this Data Sheet advice and data has been based on this code of practice and refers to equipment available from RS Components Limited. The information contained in this data sheet is intended for guidance only. As the circumstances for each installation can vary substantially, we recommend that you consult your local fire prevention officer and a qualified electrician.

A copy of BS5839 is obtainable from the British Standard Institution, Linford Wood, Breckland, Milton Keynes, MK14 6LE.

Guide to Installation

The first decision to make is whether the system is required for the protection of life or property, or both. Generally, if an alarm system is required to protect life in a building housing normally active persons a manual system may be sufficient, but automatic detection will ensure that an alarm is raised in good time throughout the premises to enable all occupants to be safely evacuated. When installing a system to protect property automatic fire detection devices are a must to ensure that an alarm is raised with minimum delay between ignition and effective fire fighting action. It is also important to ensure that any system installed meets with the user requirements and national and local legislation. If there is any doubt as to whether a system to be installed meets these requirements you should consult your local Fire Prevention Officer.

Draw a plan of the building to be protected; for small systems this plan can be very basic but should show all walls, partitions, doors and exit routes. The plan should be large enough to show all cable runs and detail location of equipment. This plan should be kept for maintenance and record purposes.

Alarm Control Panel

The RS Fire Alarm Control Panel is suitable for single storey buildings with an area up to 2000m² or for multi-storey buidings having an area of no greater than 300m² (total all floors). The control panel should be sited where it is clearly visible at all times, in an area of low fire risk to reduce the possibility of being involved in a fire before adequate warning is given. A good location for the alarm control panel is in the main entrance where the fire brigade would enter the building.

Manual Call Points

Manual call points should be located on all exit routes and in particular on floor landings of staircases and at exits to the open air. In general they should be fixed at a height of 1.4m above the floor and sited so that no person need travel more than 30m from any position within the building to actuate the alarm.

Smoke and Heat Detectors

The four types of fire detectors available from RS are the ionisation smoke detector, RS 300-473, the optical smoke detector, RS 300-489, the fixed temperature heat detector, RS 300-495, and the rate of rise heat detector, RS 300-502. No one type of detector is suitable for all applications and the final choice will depend on individual circumstances.

The correct selection of smoke detectors will depend mainly on what type of smoke can be expected to be produced by a fire condition within the protected area. In general, materials producing smoke with large particles e.g. P.V.C. insulation, fabrics and furnishings, are best protected by optical smoke detectors whereas for materials producing small particles (normally clean burning fires e.g. spirit and solvent) the ionisation smoke detector will give a faster response. With the majority of fire risks, ionisation type units will provide rapid detection. If, however, the hazard includes – for instance – electrical equipment, where dense smoke from burning P.V.C. can be expected then the optical smoke detector will give a faster response.

To avoid unwanted alarms the following areas should be avoided when using **smoke detectors** and should be protected by other means of fire detection such as heat detectors.

Areas with a high level of dust or dirt.
Dust or dirt from the environment can accumulate in a detector sensing chamber making it over sensitive.

Damp or humid areas. Any damp or humid areas including showers, bathrooms and out-door applications should be avoided.

Areas where corrosive vapours are present.
Detectors should not be mounted where gases, vapours or fumes are present such as in some manufacturing areas or battery rooms.

Switch rooms. Ionisation detectors should not be mounted in switch rooms where air ionised by circuit breaking contacts may be present. Optical detectors are normally used in this instance.

Cold storage areas. Other areas that should be avoided include kitchens, garages, welding shops, ovens, burners and boiler houses. Detectors should never be installed in areas where the temperature can drop below 0°C because crystals or condensation can affect detector sensitivity. Rate of rise heat detectors are normally used in this instance.

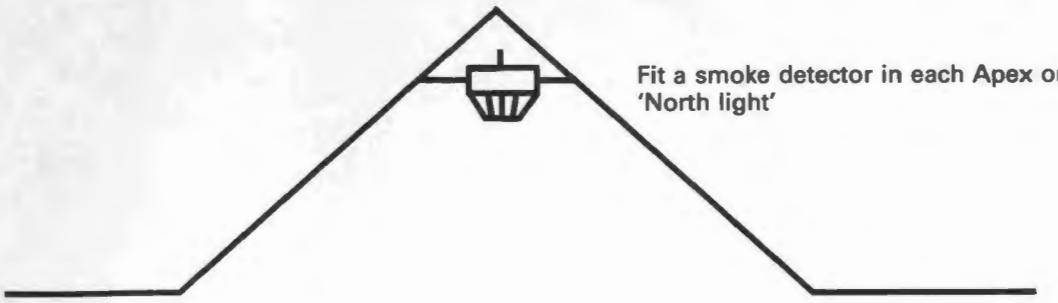
Heat detectors are designed either to detect an abnormal rate of rise of ambient temperature or to operate at a pre-determined fixed temperature. Although heat detectors give a slower response time than smoke detectors they can provide ideal protection in areas where smoke detectors cannot be used.

Although in general all types of fire detectors should be positioned at the highest point of the area to be covered, height does reduce the efficiency of heat and smoke detectors. Heights greater than 9.0m can cause problems.

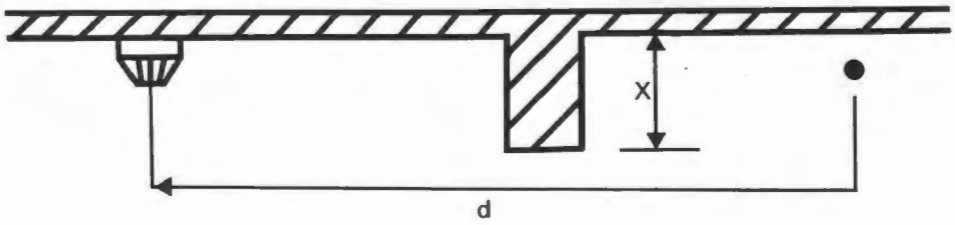
Conversely, with low ceilings, the sensitivity of smoke detectors increases and care in sighting is necessary to avoid nuisance operation by tobacco smoke etc.

The area covered by any one RS detector should not normally be in excess of 100m² for smoke detectors or 50m² for heat detectors. In open areas under flat ceilings the horizontal distance between any point within an area and the nearest detector to that point should not exceed 7.5m for smoke detectors and 5.3m for heat detectors.

Figure 1 **Siting of smoke and heat detectors**



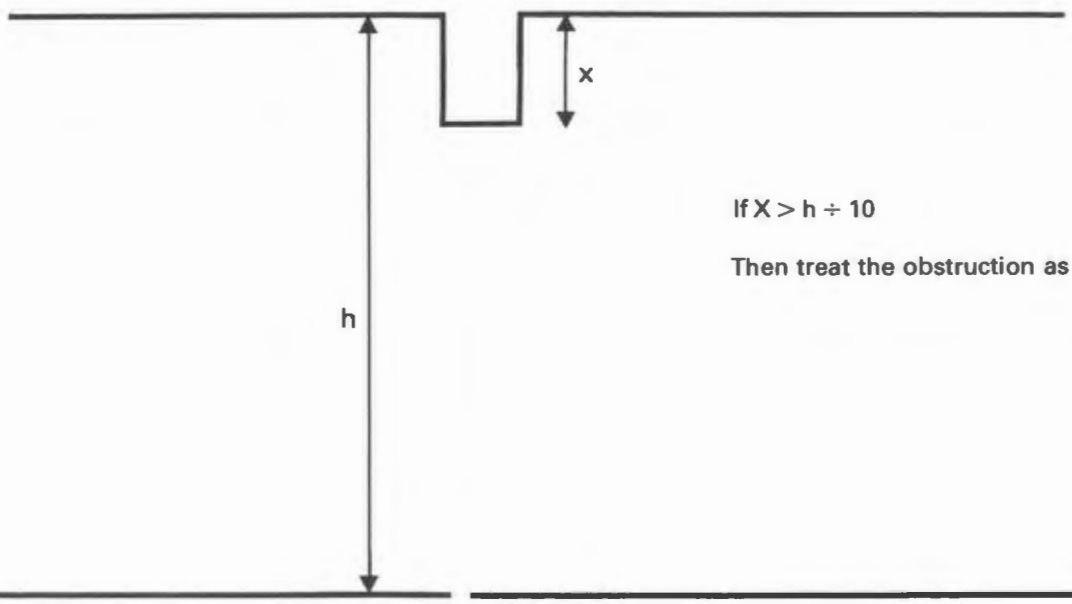
Distance between any point and the nearest detector should not be more than 7.5m for Smoke detectors or 5.3m for heat detectors



The distance between any point and the nearest detector with an obstruction greater than 150mm for heat detectors or 600mm for smoke detectors must be reduced by twice the depth of obstruction.

Smoke detector distance $d = 7.5 - 2X$ m

Heat detector distance $d = 5.3 - 2X$ m



If $X > h \div 10$

Then treat the obstruction as a Wall.

When mounting RS detectors the sensing elements should be mounted not less than 25mm (nor more than 150mm for heat detectors, or 600mm for smoke detectors) below the ceiling or roof. If a protected area has a pitched roof or north-light roof then detectors should be installed within each apex at a level not more than 150mm below an apex for heat detectors, or 600mm below an apex for smoke detectors. If the difference in height between the top and bottom of each apex is less than 150mm when using heat detectors or 600mm when using smoke detectors then the apex may be disregarded. With ceiling obstructions (having a depth greater than 150mm) that can disturb the flow of smoke the horizontal distance between any point on the ceiling and the nearest detector should be decreased by twice the depth of the obstruction. If the depth of the obstruction is greater than 10% of the height of the ceiling then the obstruction should be treated as a wall and each side of the obstruction should be considered as a separate room. It is also important that detectors are mounted further than 500mm away from any walls, partitions or obstructions.

Audible Alarms

The number of alarm sounders used in a system should be capable of producing a sound level of either 65dB(A) minimum or 5dB(A) above any background noise likely to persist for a period longer than 30 seconds whichever is the greater. The sounders should be evenly distributed to give this sound level at all parts of the building giving special regard to sound attenuation by walls, doors and furnishings etc.

If the alarm system is to be used in premises such as hotels, boarding houses etc, where it is required to wake sleeping persons then the sound level should be 75dB(A) minimum at the bedhead.

All audible warning devices used in the same system should have a similar sound and be distinct from any other audible alarms used for other purposes.

When audible warning devices are installed in noisy areas caused by mains powered machinery, it is permissible to have back up sounders operated from the same mains supply so that they only operate when the machines are running. If there is any possibility that the mains supply to sounders can fail whilst the machine supply is maintained then an audible/visual fault warning should be given.

Cables & Wiring

The satisfactory operation of a fire alarm system depends on the interconnections made between the component items. It is essential that connections between detectors and manual call points function correctly when they are operated. The destruction of a cable connected to a detector or manual call point after it has operated will not affect the sounding of the alarm since this will be maintained by the Control Panel.

Certain cables may be required to function correctly for a significant period after being attacked by fire. These include the power supply cables to the control equipment and the cables connecting the audible warning devices to the fire alarm control panel. It should be noted that the monitoring of cables and connections, whilst giving a warning of damage or a connection failure, does not ensure that the system remains effective at all times. The cable monitoring should not be considered to improve the integrity of cables during a fire condition.

Types of cable permissible for use where continued operation is required after the cable is attacked by fire are as follows:

i) 'FP200' to IEC332 and BS4066
ii) M.I.C.C. to BS6207:pt 1 with or without a P.V.C. sheath. Cables for operating in damp, corrosive or underground installations should be P.V.C. sheathed overall.
iii) P.V.C. insulated non-sheathed or sheathed cable to BS6004 provided it is protected by conduit or trunking.
iv) General purpose elastomer-insulated textile braided and compounded cable to BS6007 provided it is protected by conduit or trunking.

Additional types of cable permissible where prolonged operation during a fire is not required can be one of the following:

i) P.V.C. insulated sheathed cable to BS6004 provided it forms part of the monitored circuit. Where there is a risk of mechanical damage by rodents and where it is installed less than 2.5m above the floor level the cable must be protected by conduit or trunking.
ii) P.V.C. insulated cable complying with the requirements of types BK, BR and BU of BS6231 provided they are protected by a conduit or trunking and have a cross sectional area of not less than 1mm^2.

Cable runs should be continuous from one component to another and joints in cables should be avoided. Where joints are necessary they should be enclosed in a suitable terminal box and preferably marked "Fire Alarm".

Fire alarm control panel

The RS single zone fire alarm control panel meets the requirements of BS5839:pt1:1980 "Fire Detection and Alarm Systems In Buildings" and the functional requirements of BS 3116:pt4:1974 "Automatic Fire Alarm Systems"

The RS panel has been designed for use in smaller premises and is suitable for both automatic and manual fire detection. The very low operating current of this control panel enables a 72 hour standby with a minimum 1 hour alarm at 0.75 amps, from a 1.8Ah sealed lead acid battery.

All panel controls are safeguarded against unauthorised use by a lockable door with perspex windows which allow clear identification of the panel indicators. Operating instructions are printed on the inner front panel enabling easy operation.

Features

- Meets the requirements of BS 5839:pt 1 and BS 3116:pt 4.
- Low power consumption
- Totally self contained
- 72 hour standby from 1.8Ah batteries
- Full status indication on front panel
- Fully monitored circuits.

Front panel controls

SUPPLY ON

The Supply On indicator illuminates when the mains voltage is present and d.c. supply is within operating parameters.

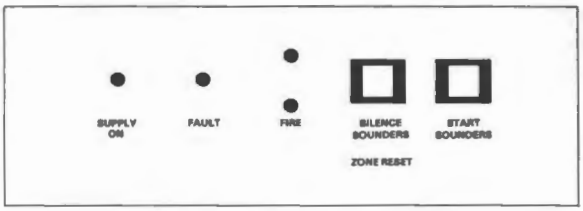
FAULT

The Fault indicator illuminates when there is a fault with any monitored circuit (non latching)

FIRE

The Fire indicators illuminate and latch on when the detector circuits are short circuited (fire condition). These can only be reset by the Zone reset operation. See below.

Figure 2 **Front panel controls**



SILENCE SOUNDERS/RESET

Pushing the "Silence Sounders" switch once will isolate the two sounder output circuits and activate the 'supervisory' buzzer to indicate the system has not been reset. This switch may also be used to silence the fault warning buzzer when the panel is in a fault condition.

Pushing the "Silence Sounder" switch a second time will reset the control panel after an alarm.

START SOUNDERS

The Start Sounders switch will actuate the sounders no matter what the panel status. (Latching fire indicators do not light).

Functional description

The control circuitry is contained on a single p.c.b. (see Figure 3) and all terminations are made via the 9 way terminal block TBI.

Detector input (Z+ and Z−)

The detector input terminals serve two functions:–

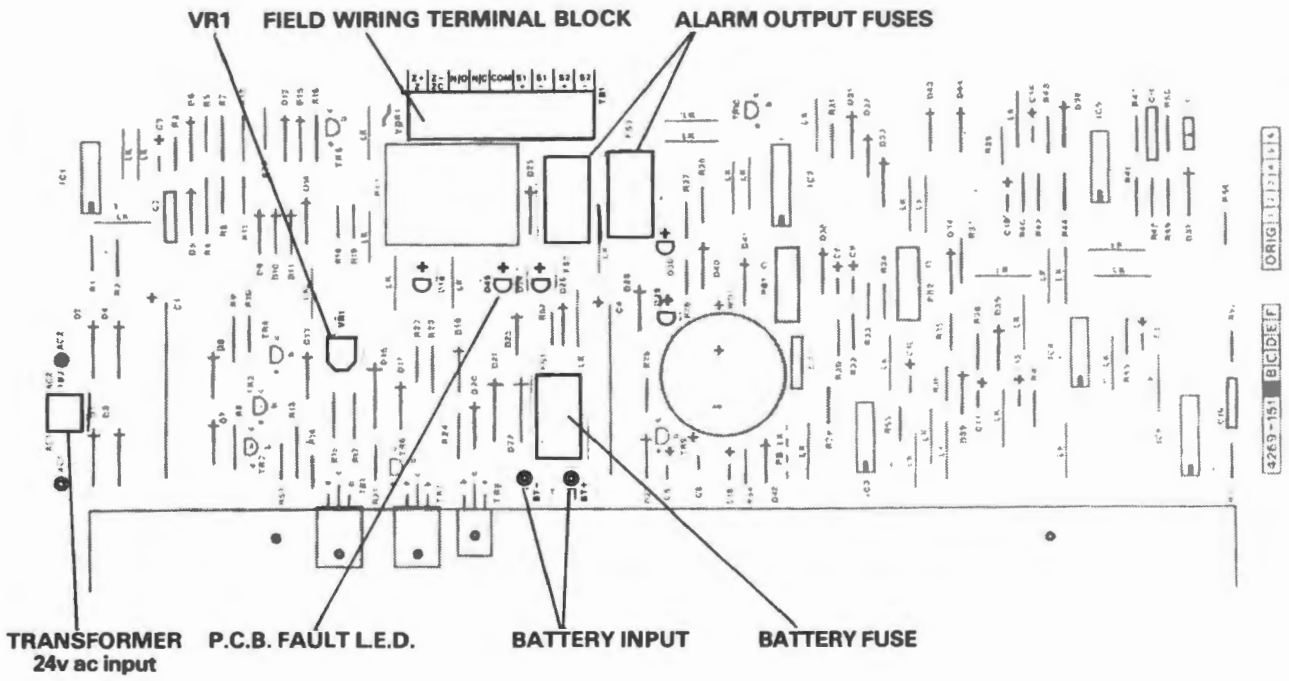
a) to monitor the cables for open circuit (fault and short circuit (alarm)
b) to supply the detector with 24V d.c.

The monitoring is achieved by monitoring an end-of-line element at the last detector of the parallel circuit. If there is an open circuit the fault warning circuit is activated and if there is a short circuit there is an alarm output (fire condition).

The detector 24V d.c. supply is capable of driving up to 20 smoke or heat detectors (total zone current 2mA max). This number of detectors should not be exceeded as the increase in supply current can cause false alarms. If detectors other than those supplied by RS Components are used then the detector manufacturer's advice should be sought.

Detectors and manual call points are wired on the same circuit in parallel. As manual call points consume no power there is no limit to the number that can be used.

Figure 3 **PCB layout**

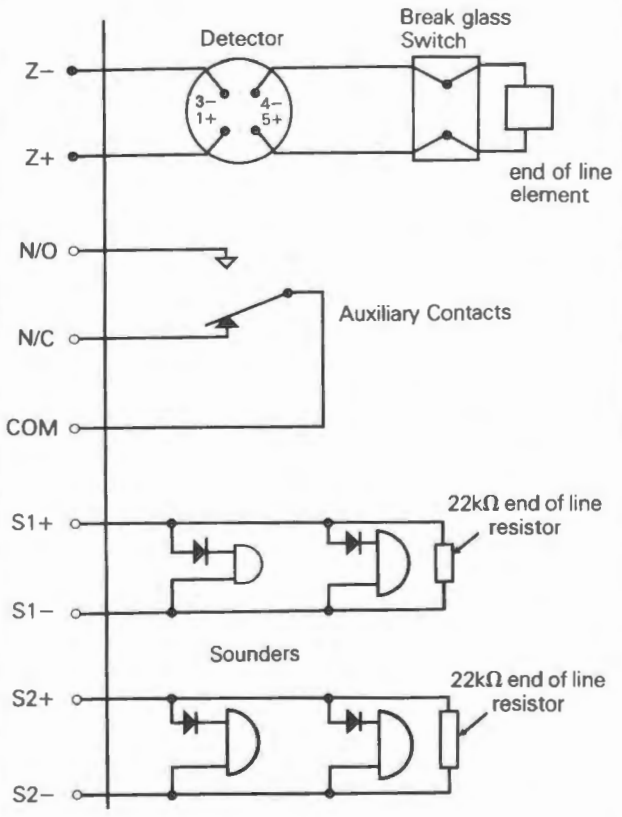


Auxiliary Contacts
Single pole change over contacts are supplied for remote signalling or for control of other equipment e.g. plant shut down. The auxiliary relay operates when there is an alarm condition or when the "Start Sounders" switch is actuated. The three normal contacts, normally open (N/O), normally closed (N/C) and common (com) are voltage free and capable of switching 30V a.c. or d.c. at 1.0 amp.

Sounder Outputs (S_1+S_1- and S_2+S_2-)
There are two sounder outputs which are separately fused. Both circuits are fully monitored for both open and short circuit. The sounders should be wired in two parallel circuits, see figure 4, with an end of line resistor (22kΩ) for monitoring purposes at the end of each sounder circuit. The sounders must be rated at 24 Volts d.c. and polarised by a series diode (RS audible warning devices suitable for fire alarm systems are already polarised) to ensure the correct operation of the monitoring circuits. The maximum sounder load that the panel can supply is 1.0 amp. Spurs or tees must not be used.

Cable Entries
Cables should be brought into the Control Panel using the 20mm cable entry knockouts on the upper face and back of the case. To use these entries simply tap out the knockouts as necessary and fit the required glands or conduit adaptors.

Figure 4: **Terminal block connections**



Earth Bonding
The main point for earth bonding is on the mains input terminal block between the "Live" and "Neutral" terminals. A maximum cable size of 2.5mm² cross sectional area can be used. Insulated cable must be used and care must be taken to ensure that fouling of the internal components does not occur.

Cable Maximum Ratings

	Detector Circuit	Sounder Circuit
Loop resistance	150Ω max	100Ω* max
Capacitance between cores	2μF max	–
Core to core leakage resistance	1MΩ min	–

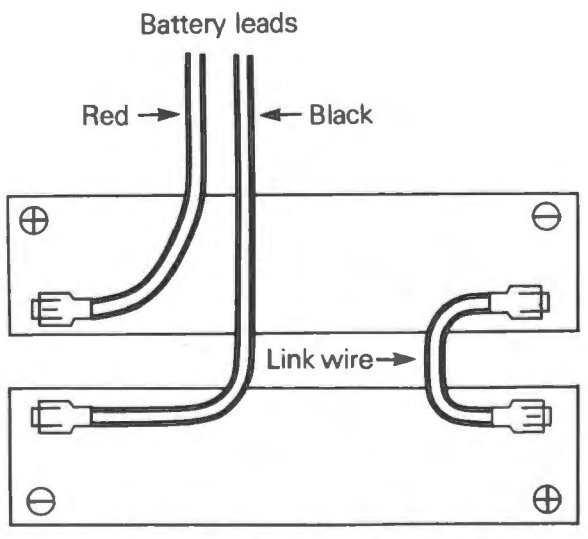
* In practice the cable must be of sufficiently low resistance to pass full alarm load, and deliver the rated voltage to the furthest sounder.

Stabilised Supply
The control panel has a stabilised 24V d.c. supply that is capable of supplying 1 amp. This supply is monitored and should it fail or should any fuse fail there will be a fault warning given.

The supply also charges the rechargeable batteries and it is important that an open circuit voltage of 27.3V d.c. is not exceeded. When adjustment is required the voltage should be set by variable resistor VR1.

Rechargeable back-up battery
The control panel has the facility to charge two 12V 1.8Ah A300 dryfit batteries RS 591-966 which must be sited in the bottom of the cabinet. The batteries must be connected observing the correct polarity and wired in accordance with Figure 5. Because of the low power consumption a set of two 12V, 1.8Ah batteries is sufficient for a standby time of 72 hours with a 1 hour alarm duration at 0.75 amp or ½ hour alarm time at 1.0 amp.

Figure 5: **Rechargeable battery connections**



2 × A300 12V 1.8Ah batteries (591 – 966)

Fuses
Mains
providing power for isolating transformer
1A HRC

Alarm output
providing power for sounder output circuits
2×800mA

Battery
provides power to and from the Standby batteries
2.5A

Mains Input Cabling
The 240 volt AC mains supply must be brought in via a cable entry, to the mains input terminal block situated on the main chassis below the printed circuit board. Check that a 1 amp fuse to BS 1362 is fitted into the carrier on the terminal block; do not switch on the mains supply until installation is complete.

Note: It is recommended that the mains supply is connected to an unswitched fused spur to prevent the panel from being inadvertently switched off.

Mains Input Ratings

Min	Nom	Max
217V	240V	264V at 50Hz a.c.

Mounting Details
Remove the door by opening fully and sliding sideways. Remove both front panel and battery cover – this will expose all fixing holes and cable entries. Care should be taken not to damage the p.c.b. assembly and if necessary this should be removed (see installation instructions).

The case is secured to the wall by three No. 10 screws, 50mm long. The overall wall space required for the installation is 270mm high × 350mm wide; in addition space should be allowed all round for access and to allow the door to be hinged open downwards and removed sideways.

Fault Identification/Repair Service
The electronics of this product have been carefully designed to be contained on a single printed circuit board. If you suspect a fault with the alarm panel then it will be necessary to return the p.c.b. assembly to RS for repair/exchange (see the latest RS catalogue for details). Before returning the p.c.b. assembly it is advisable to test the control panel in isolation. This is simply carried out by removing the field wiring and replacing it with the end-of-line elements at the terminal strip. Should it prove to be functioning correctly then each field circuit can be replaced and tested in succession.

Because all incoming and outgoing circuits are monitored for faults it is possible to recognise the type of circuit fault by the state of the fault LED indicators.

Type of Fault	Fault Indication
Supply Fault A.C. Mains failure Battery Disconnected Blown Fuse	 Green LED OFF, flashing amber fault LED, pulsed fault buzzer
Zone Fault End-of-line element disconnected Smoke or heat detector removed Broken cable or poor joint	 Flashing amber fault LED, flashing pcb LED Pulsed fault buzzer
Sounder Fault End-of-line element disconnected Poor joint or broken cable Blown fuse	 Flashing amber fault LED, continuous p.c.b. LED, Pulsed fault buzzer

Should the p.c.b. assembly need returning it is easily removed following the instructions outlined in the installation instruction leaflet.

Automatic detectors

A series of smoke and heat detectors providing a comprehensive range of sensing devices for use on d.c. monitored, automatic fire detection systems. The series has been designed to provide easy installation and maintenance with full detector interchangeability.

Particular emphasis has been given to the overall series design, in order to minimise the incidence of false alarms from electrical or other sources of interference. The heat detectors are designed to meet the requirement of BS 5445:pt5, as recommended by BS 5839:pt1:1980 and the smoke detectors are designed to meet the requirements of BS 5446:pt1 and the draft European standard PrEN54:pt 7.

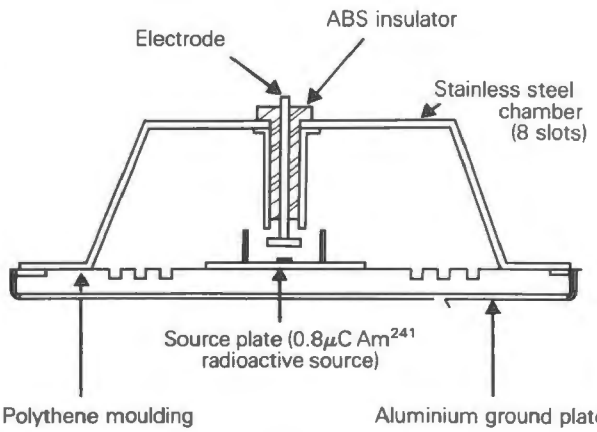
Features

- Designed to minimize possibility of false alarms.
- Computer set sensitivity for optimum operation.
- Complies with all relevant British and European standards.
- Fully electronic ensuring reliable operation.
- Common base unit for ease of installation and interchangeability.

Ionisation Smoke Detector

The Ionisation smoke detector is ideal for detecting smoke and the invisible products of combustion generated by "fast" burning, high energy type fires. It is ideal for risk areas such as solvent stores.

Figure 6: **Ionisation smoke detector schematic**



Visual indication of an alarm is given by a light emitting diode, clearly visible on the detector casing.

Operation

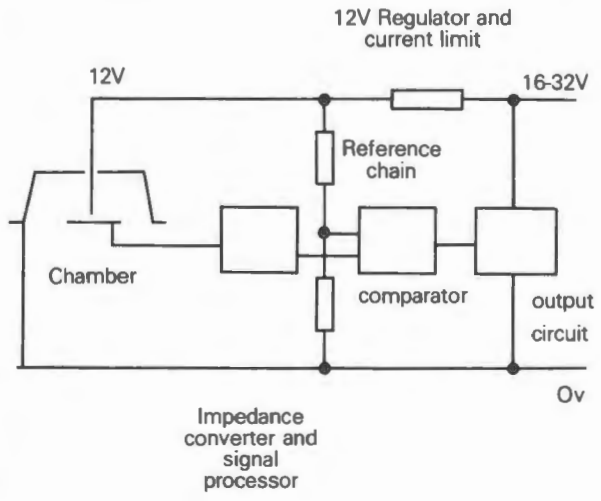
Under normal conditions ionised molecules of the gases in the air flow freely across the ionisation chamber causing a small current to flow. The chamber includes a low energy ionising radiation source (0.8μC Americium 241, complying with the activity requirement of OECD Directive on Smoke Detectors). Ionised smoke particles, even those not visible, impede the flow of and have a lower mobility than the ions and so reduce the current in the chamber. When the current has dropped to a predetermined level the alarm circuit is triggered.

SPECIFICATION

	Ionisation smoke detector (300 – 473)	Optical smoke detector (300-489)	Fixed temperature heat detector (300-495)	Rate of rise heat detector (300-502)
Supply Voltage	16-32V D.C.	16-32V D.C.	16-32V D.C.	16-32V D.C.
Supervisory Current (At 28V Nom.)	50μA	90μA	45μA	45μA
Max Alarm Current	75mA	75mA	75mA	75mA
Min. Current in Alarm Mode	10mA	10mA	10mA	10mA
Nominal Alarm Voltage developed across the detectors in Fired Condition at Limiting Currents as shown 10mA	5.5V	5.5V	5.5V	5.5V
20mA	7.7V	7.7V	7.7V	7.7V
50mA	13.7V	13.7V	13.7V	13.7V
75mA	18.4V	18.4V	18.4V	18.4V
Fire Indication White when off	Red LED on casing	Red LED on casing	Red LED on casing	Red LED on casing
Ambient Temp. Range	0°C – 50°C	0°C – 50°C	0°C – 50°C	−20°C – +50°C
Base Connection (Base supplied with each detector)	3 sets of stainless steel contacts within the base mate with 3 spring grade stainless steel spring contacts in the detector			
Casing	ABS Engineering plastic Spectrum 2000 – 24015 (off-white)			
Dimensions Without Base –				
Max. dia	93mm	93mm	93mm	93mm
Distance across LED Moulding	104mm	104mm	104mm	104mm
Depth With Base –	75mm	75mm	44mm	44mm
Max. dia.	97mm	97mm	97mm	97mm
Distance across LED Moulding	107mm	107mm	107mm	107mm
Depth	94mm	94mm	59mm	59mm
Weight With Base –	255gms	250gms	150gms	150gms
Without Base –	175gms	170gms	70gms	70gms
Detection Method –	Americium 241 radiation source 0.8μC (complies with activity requirements of OECD directive on smoke detectors containing radioactive material)	Optical smoke detection by infra-red beam scatter (Tyndal effect)	Thermistor sensor	Dual Thermistor sensors

The detector incorporates a circuit which reduces the probability of false alarms caused by vibration, shock, insects or electrical line transients.

Figure 7: **Ionisation smoke detector block diagram.**



Optical Smoke Detector

The Optical smoke detector is particularly effective in the detection of visible smoke from slow smouldering fires, for example overheated PVC.

Operation

The Optical smoke detector operates on the long proven principle of smoke detection by light scatter, the Tyndal effect.

The inside of the smoke chamber is black and reflects very little light. A concentrated, pulsed infra-red beam is projected across the smoke chamber and an alarm photosensor is fitted in a special housing at an obtuse angle to the beam.

Figure 8: **Optical smoke detector schematic**

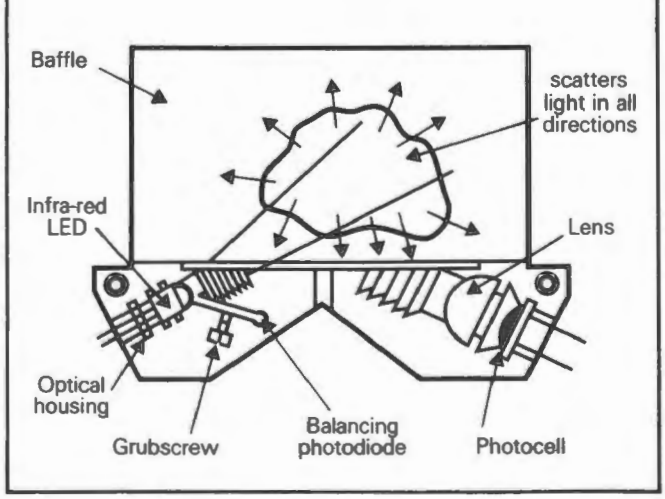
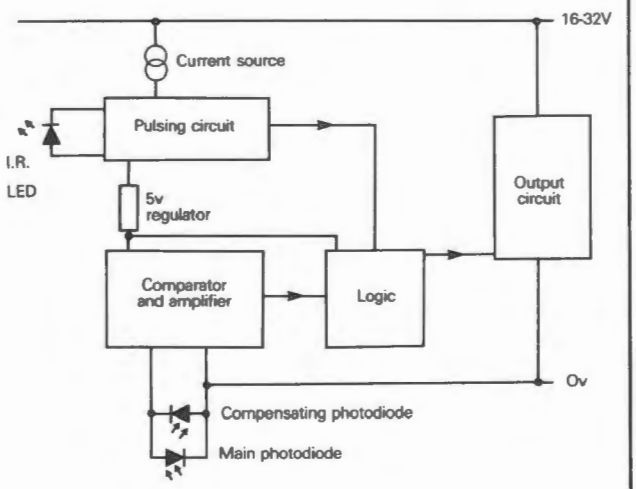


Figure 9: **Optical smoke detector block diagram**



Under normal conditions virtually no infra-red reaches the photosensor.

When smoke enters the smoke chamber the infra-red pulses are scattered by reflection from the smoke particles and affect the photosensor. The small electrical signal from the photosensor is amplified and after a verification period (of 3 pulses) initiates the operation of the alarm circuit.

Fixed Temperature Heat Detector

The fixed temperature heat detector is set to a nominal operating temperature of 57°C (135°F) to give the best possible results for normal fire alarm purposes consistent with early warning and the absence of false alarms. This detector setting allows the detector to conform to the operational requirements of Grade 2 of BS 5445 Part 5.

A thermistor heat sensor is employed to actuate the electronic alarm circuit at the predetermined temperature.

Rate-of-Rise Heat Detector

The rate-of-rise heat detector provides a high degree of protection for areas with normally constant ambient temperatures.

Rate of rise detectors are also effective in areas of low ambient temperature (cold rooms and refrigerated areas) where the large difference between ambient and fixed temperature detector setting could delay early warning.

The rate of rise heat detector also includes a fixed temperature "backstop" circuit which is set to operate at 57°C (135°F).

The detector is available with a sensitivity performance to Grade 2 of BS 5445 Part 5.

Thermistors are incorporated to detect both rate of temperature rise and the fixed temperature level.

Figure 10: **Fixed temperature heat detector schematic**

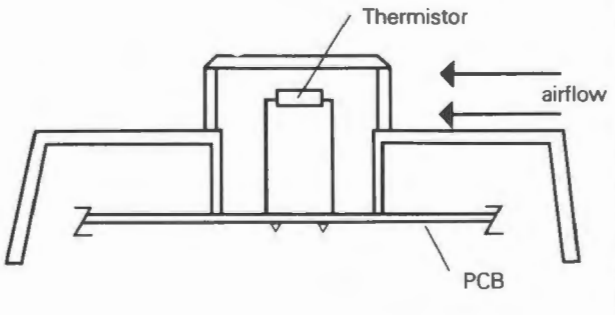


Figure 11: **Rate of rise heat detector schematic**

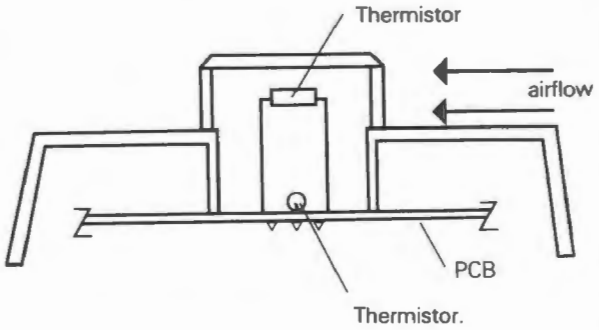


Figure 12: **Fixed heat and rate of rise temperature detector block diagram**

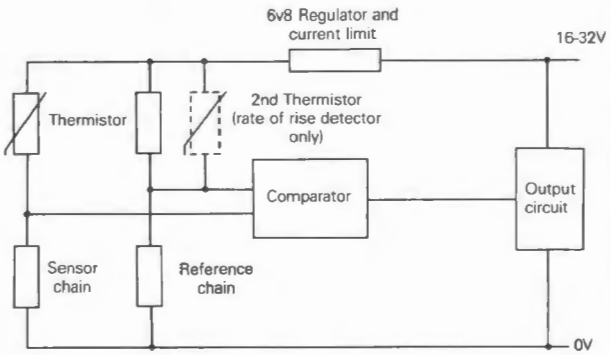
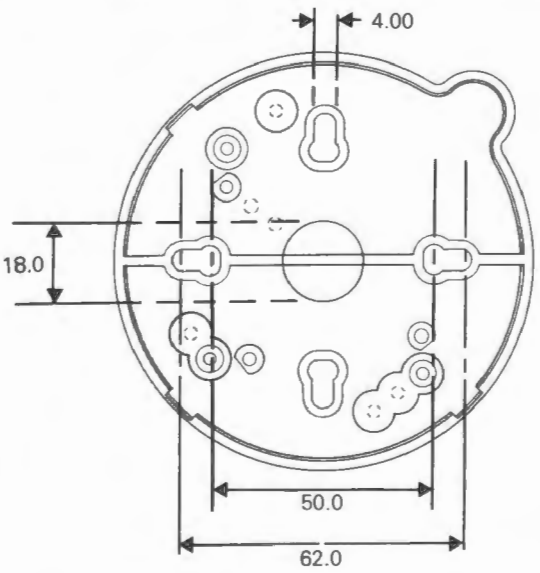


Figure 13: **Smoke detector base**



Installation

The RS range of detectors are supplied complete with mounting bases which are common to all types. This will enable all the bases to be mounted and wired without the need to match a particular type of detector to its own base.

The base is suitable for two-wire circuits using surface or concealed wiring methods. The detector is fitted to the base by a simple plug and twist locking action.

Care has been taken in designing the base unit to ensure ease of installation. The easily accessible terminals are capable of accepting most conventional cables up to 2.5mm².

Four fixing holes are provided to allow fixings to be made at centres variable between 50mm and 60mm. The holes also enable the detector to be positioned so that the alarm indicator LED is visible from a doorway etc. A remote LED indicator may also be connected to the base terminals (see figure 14). The detector bases should be wired in accordance with figure 14 and the wiring insulation tested in accordance with the IEE regulations. **All high voltage insulation tests should be carried out with the detctors removed and not connected to the fire alarm control panel.**

All smoke detectors come packed in a polythene bag to protect them from dust and dirt and they should not be installed until the system is ready to be commissioned. A dusty environment can affect the sensitivity of detectors and cause false alarms.

If a detector is contaminated then the detector should be cleaned or returned to the RS repair department together with the "Repair/Exchange form" for service and recalibration. See latest RS catalogue for details.

The finish of the detector is of vital importance and under no circumstances must it be painted at any time as this will affect the operational characteristics.

Service and Cleaning

It is recommended that in normal service each smoke detector is cleaned once per year in order to maintain its sensitivity at the correct level. However in dusty or dirty environments it may be necessary to clean detectors more frequently.

Cleaning of detectors should be carried out by a competent technician and under no circumstances must any recalibration be attempted. All detectors are factory set and only require routine cleaning. All cleaning should be carried out in a dust free atmosphere.

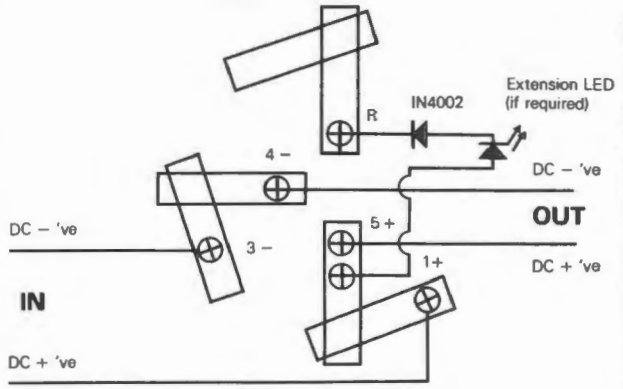
The equipment and materials required for cleaning RS smoke detectors is as follows:–

a) Torx screwdriver size T-10
b) Superdriv No. 1 screwdriver
c) Small stiff brush
d) Methylated spirit
e) Two brushes with soft nylon bristles
f) Photographic lens brush with puffer bulb ("blower brush")

Remove the smoke detector from its base by twisting it anti-clockwise until a solid stop is felt. The detector will then drop clear of the base.

Removal of the detector from its base will cause an open circuit fault signal to be given at the indicator panel. This fault indication can be cancelled and the zone circuit maintained in operation by temporarily

Figure 14: **Smoke detector base wiring**



substituting with a heat detector or another smoke detector providing it is compatible with the system as a whole.

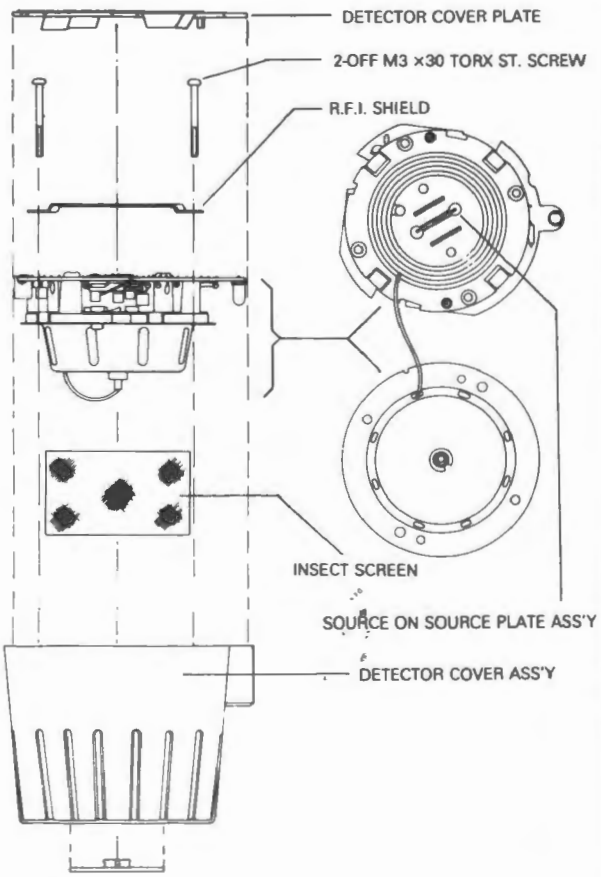
Unclip the plastic base cover and remove it to expose the pcb assembly (see Figure 15).

Unscrew the two Torx screws situated either side of the screening plate and remove the detector assembly from the case.

Clean any dust and accumulated dirt from the cover using the stiff brush.

The two nylon brushes must now be designated "Wet" and "Dry". The "wet" one must be kept solely for use with the methylated spirit and the

Figure 15: **Exploded view of ionisation smoke detector.**



"dry" one solely for buffing up after cleaning.

Using the stiff brush remove dust, dirt and insect remains from the chamber mesh. If the mesh appears greasy or sticky it must be cleaned with methylated spirit using the "Wet" soft nylon brush.

Remove the two Superdriv screws retaining the centre electrode assembly. Lift the assembly clear taking care not to damage the connecting lead.

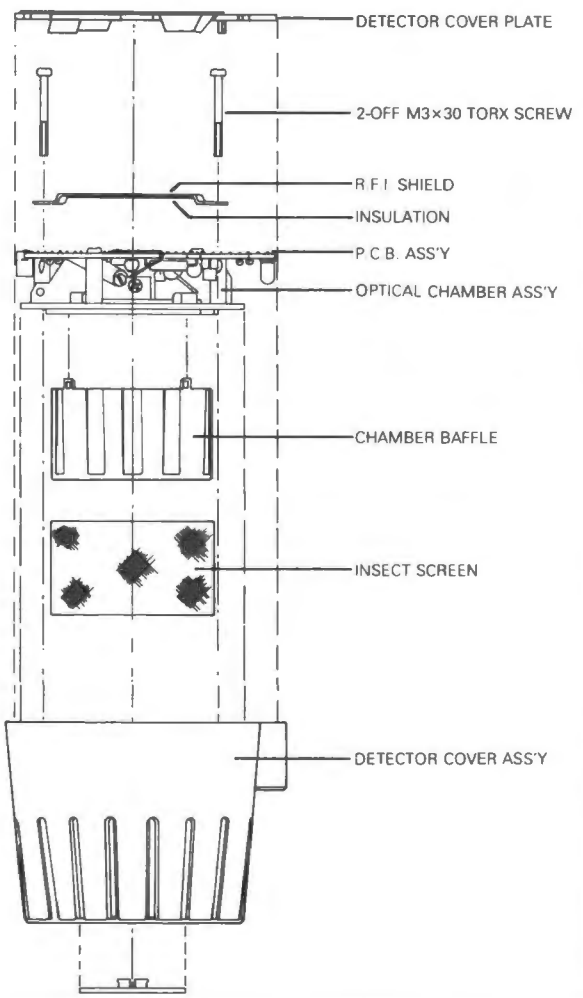
The radiation source is now exposed and it is important that the following precautions are followed.

Although the radio-active element is a very low energy source (0.8μC Americium 241) these procedures have been devised to ensure that the cleaning operation is safe.

When the chamber assembly has been removed from the detector it is very important that the following precautions are taken to avoid receiving unnecessary doses of ionising radiation.

1. Hold the brush with the fingers at least 2" from the radio-active source.
2. Never touch the radio-active source.
3. Do not allow the naked eyes to come within 6" of an exposed source.
4. Clean the "wet" brush in methylated spirit for each operation.

Figure 16: **Exploded view of optical smoke detector**



Torx is a trade name of Camcar Textron Inc,. Superdriv is a trade mark of Guest Keen and Nettlefold Ltd.

5. After dipping into the methylated spirit, the brush must be allowed to drain off surplus fluid to avoid droplets forming on the radio-active source.
6. DO NOT get into any position where it is possible to inhale vapour from contaminated methylated spirit, whether it be directly from the source or from the contaminated brush.
7. Thoroughly clean the "wet" brush in fresh methylated spirit at the end of the operation and do not at any time use methylated spirit that is dirt contaminated.
8. Keep the "dry" brush clean with soap and water. Allow this brush to dry completely before reuse.

Using the "wet" soft nylon bristle brush and clean methylated spirit, brush the source, source plate, source mounting and baffle to remove any surface contamination. After allowing one minute for the methylated spirit to evaporate, buff up the surface with the "dry" brush to remove any residue. If any residue remains repeat the cleaning process until all surfaces are clean.

Reassemble the detector remembering to replace the chamber mesh before screwing back the assembly into the housing. The Torx screws only need to be tightened sufficiently to hold the assembly firmly together.

Optical Smoke Detectors

Unclip the plastic base cover and remove it to expose the pcb assembly see figure 16.

Unscrew the two Torx screws situated either side of the screening plate and remove the detector assembly from the case.

Remove the gauze and baffle from the housing, slide the gauze off the baffle and clean both components with methylated spirit if necessary. Be especially vigilant to detect light coloured dust which can make the interior of the detector seem grey instead of its correct absolutely black appearance.

With the soft photographic brush clean the optical housing surface, the collimating grooves, the transmitting LED's head and the receiver lens. Do not rub or in any way polish the detector chamber surfaces as this will increase their reflectivity and give rise to false alarms. Make sure none of the dislodged dust remains, particularly in the recesses housing the transmitting LED and the receiver lens.

Reassemble the detector by sliding the wire gauze over the baffle from the top and locate the baffle assembly onto the optical housing. Slide the detector housing over the assembly and tighten the two Torx screws. Replace the base cover.

Heat detectors

Regular cleaning of heat detectors is unnecessary but dirt and grease should not be allowed to build up. When cleaning is necessary the housing and p.c.b. assembly should be cleaned with methylated spirit using a soft nylon brush as previously described.

Testing

Apart from the routine testing of installed smoke detectors in a fire alarm system, it is also recommended that each cleaned detector be tested for correct functioning and, in practice, this can be

most conveniently done as part of the system maintenance programme. The response of the associated fire alarm system will reveal that an alarm has been raised successfully by the activation of the detector due to the introduction of smoke.

A piece of smouldering sash cord is very suitable for generating smoke because its side effects are minimal from the point of view of presenting a fire hazard, discolouration of the ceiling or deposition within the detector. The user should blow across the end of the smouldering sash cord to project the smoke into the detector.

In this connection we must warn against the use of chemically generated "smoke". This can be highly corrosive and, if sprayed from a pressurised cannister, it can coat and contaminate the smoke detector.

Commissioning, Testing and Maintenance

The complete installation should be checked and inspected to ensure that all cables and wires have been correctly installed and connected and that all cables are installed in accordance with the IEE regulations.

Insulation testing using high voltage test sets e.g. Megger, must be carried out with the control panel, sounders and smoke detectors disconnected.

Ensure that all end-of-line elements have been fitted across the last device on each line. Labels are supplied to stick alongside the last detector or sounder for ease of identification.

Connect the leads to the battery ensuring correct polarity. After a short delay the fault indicator and buzzer will operate (indicating a mains failure). If not recheck the battery connections and the fuses.

Connect the mains supply to the panel. The fault indicator and buzzer will stop. If a fault still exists then the fault finding sequence should be carried out as described earlier.

When the control panel is operating satisfactorily each detector and sounder should be tested, and any remote signalling equipment checked for correct function. The installer should certify that the installation complies with the recommendations of BS 5839 code of practice and issue a certificate of installation and commissioning (see installation instructions for the RS Control Panel).

User responsibility

It is the user's responsibility to carry out or have carried out routine tests at regular intervals as specified below.

Daily.

1. Check that the panel indicates normal operation. If not, record any fault indicated in the Event log and report the fault to a responsible person.
2. Check that any fault recorded for the previous day has received attention.

Weekly

1. Operate a manual call point or smoke detector to ensure the system operates properly. Each week a different detector should be checked.
2. Check that the sounders have operated and then reset the system.
3. Check battery connections.
4. Complete the Event log with details of date, time, trigger device tested and enter "Routine Weekly Test" in the Event section. Any defects should be entered in the "Action required" and reported to a responsible person.

Quarterly

1. Check entries in the log book and take any necessary action.
2. Examine the batteries and their connections.
3. Operate a manual call point or detector to ensure the system operates properly, checking that all sounders are operating.
4. Check that all functions of the alarm control panel operate by simulating fault conditions.
5. Visually check that structural alterations have not been made that could have an effect on the siting of detectors and other trigger devices.
6. Complete the Event log with details of date, time, trigger device tested and "Quarterly Test" in the Event section. Any defects or alterations to equipment should also be entered.
7. On completion of all work a certificate of testing should be completed as recommended by BS 5839, appendix C.

Annually

1. Carry out an inspection as detailed for the quarterly inspection.
2. Every detector should be taken down, cleaned and tested in situ.
3. All cable fittings and equipment should be checked that they are secure and undamaged.
4. Complete the Event log and issue a test certificate as previously mentioned.

The above maintenance programmes are for use as a guide only and the frequency of testing should be adapted to suit the environment that the equipment is working in.

Fire Alarm Products

This data sheet has been written assuming RS fire alarm products have been used throughout. It is recommended that all equipment used complies with the requirement of BS 5839:1980. A list of suitable fire alarm products are given below:–

Single Zone Fire Alarm Control Panel	345–353
Rechargeable Dryfit Battery	591–966
Ionisation Smoke Detector	300–473
Optical Smoke Detector	300–489
Fixed Temperature Heat Detector	300–495
Rate of Rise Heat Detector	300–502
Break Glass Fire Alarm Switch	333–108
Low Current High Output AWD 24V d.c.	249–930
Low Current High Output AWD 110/240V a.c.	248–375
Low Current Variable Output AWD	248–397
Alarm Bell	248–432
Xenon Beacon – Red	565–620
Xenon Beacon – Clear	565–478
"FP 200" Fire Resistant Cables	378–050

For other associated products please refer to the latest RS catalogue for details.

RS data

Appendix C

Model certificate of testing of a fire alarm system

Certificate of testing of fire alarm system at:

Protected area .....

Address .....

.....

The system is operational and has been checked and tested in accordance with BS 5839: Part 1: 1980:

- ***clause 27 Extensions and alterations**
- ***subclause 29.2.4 Quarterly inspection and test**
- ***subclause 29.2.5 Quarterly inspection and test**
- ***subclause 29.2.5, items (a), (b) and (c) Annual inspection and test**
- ***subclause 29.2.6 Attention by the user after any fire whether automatically detected or not.**

***Delete if not applicable.**

Signed ..... **Status** ..... **Date** .....

For and on behalf of (user or service organization nominated by user) .....

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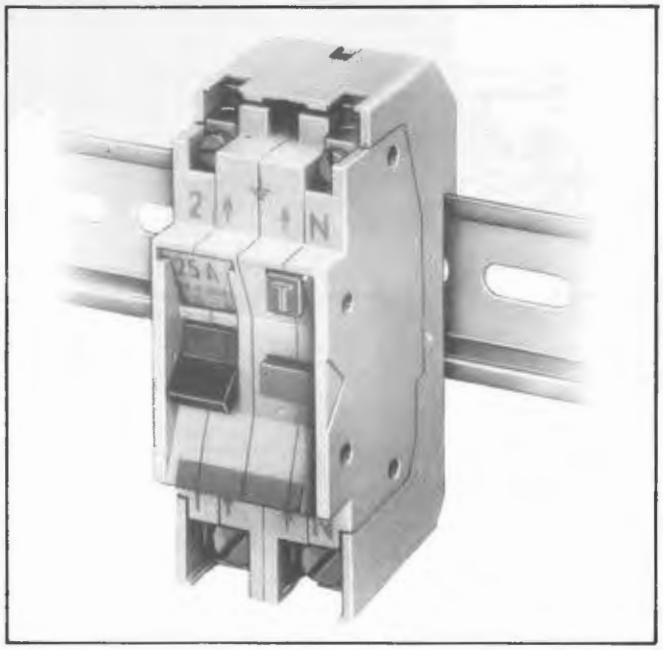
RS data

Combined MCB/RCCB

Stock numbers 332-874 to 919



Stock No.	In (A)	I△n (mA)
332-874	6	30
332-880	10	30
332-896	16	30
332-903	25	30
332-919	32	30

In = mcb rating
I△n = rated tripping current of the rccb

A range of residual current circuit breakers incorporating overcurrent protection. The unit uses an up-to-date electronic sensing system which is capable of detecting a range of fault current types (various waveforms – see Figure 4).

How the unit works

The miniature circuit breaker and residual current circuit breaker incorporates an active current transformer, the primary winding of which is formed by all the conductors of the circuit to be protected.

The secondary winding is an integral part of an oscillator with a clock frequency of 5kHz. Under normal circumstances, ie. with no fault current, there is no modulation to the 5kHz signal, and the voltage across the capacitor C is zero.

AC currents (50/60Hz) and DC currents are both treated as DC in relation to the 5kHz. When the 5kHz is modulated it is due to the presence of a fault current. The voltage across the capacitor is directly proportional to the level of the AC or DC earth-leakage current. The capacitor provides a clearly defined threshold point. If the voltage across this exceeds the threshold value, the device will trip.

Features

- Protects against overcurrent, short-circuit and earth fault currents
- Double pole switching
- High breaking capacity (3kA) and transient protected
- Consistent response time at rated tripping current (see comparison curves)
- Device operates on earth fault currents even when the neutral is interrupted
- Responds to sinusoidal and non-sinusoidal earth fault currents (AC and DC)
- Visible indication of earth fault of short circuit/ overload fault
- Modular construction to DIN 43880 (2 modules wide) means that the unit may be snap-on fitted to DIN rail (top hat profile) or mounted in a standard modular enclosure
- Timing and sensitivity of tripping consistent at supply voltage extremities (including permitted tolerances)

Figure 1 **Dimensions**

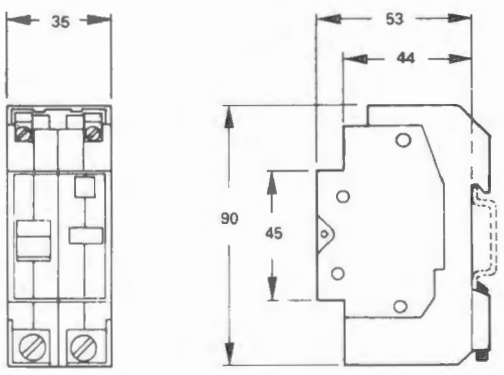


Figure 2 **Block diagram**

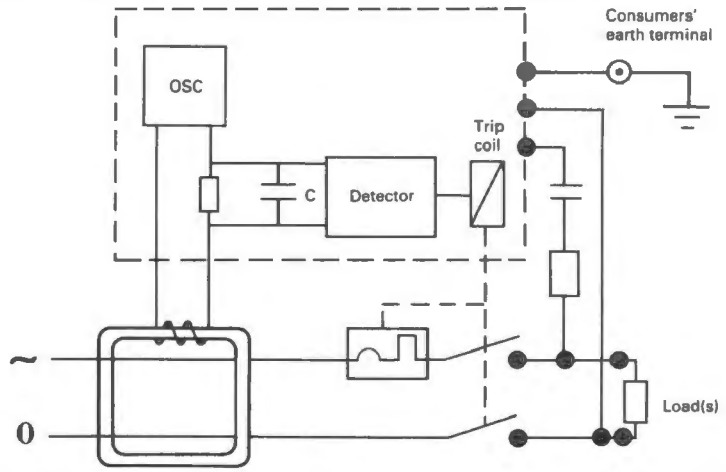
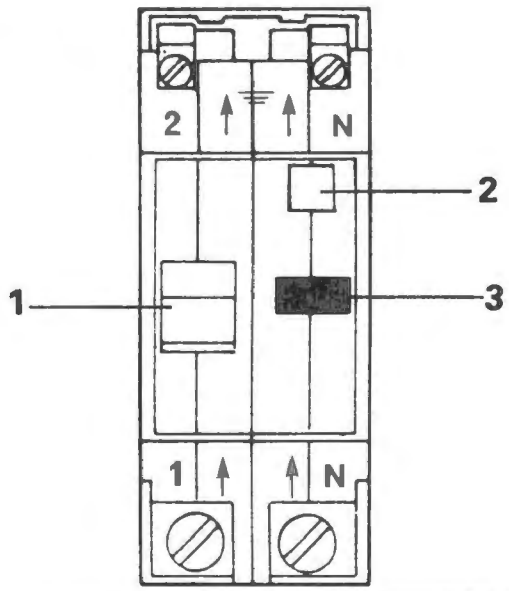


Figure 3 **Installation and testing**



1. Toggle switch MCB
2. Test-button
3. Reset earth-fault current protection

Installation

The device is clearly marked as follows:

1 and 2 are the phase (L) connections. The incoming line conductor should be connected to terminal 1. The outgoing load conductor should be connected to terminal 2.

The earth should be connected to the consumers' earth terminal. This will ensure that the device will function on an earth fault current even with a disconnected neutral.

The neutral terminals are marked N and are adjacent to their respective incoming and outgoing phase terminals.

All wiring should be in accordance with the latest edition of the IEE wiring regulations.

Testing

With the mains connected, test that the unit is operating correctly by pressing the orange test button. The green toggle switch will revert to the off position ('O' inscribed on toggle). The blue reset button will also revert to the off position, which is indicated by the button being in the fully raised position (flush with the surround). Note that in this condition (which simulates an earth leakage trip), the mcb/rccb cannot be reset by just re-closing the green toggle switch since it will not latch in the on '1' position without first depressing the blue reset button. The unit is now ready for use.

Testing as outlined above, should be carried out immediately after installation and at three monthly intervals thereafter.

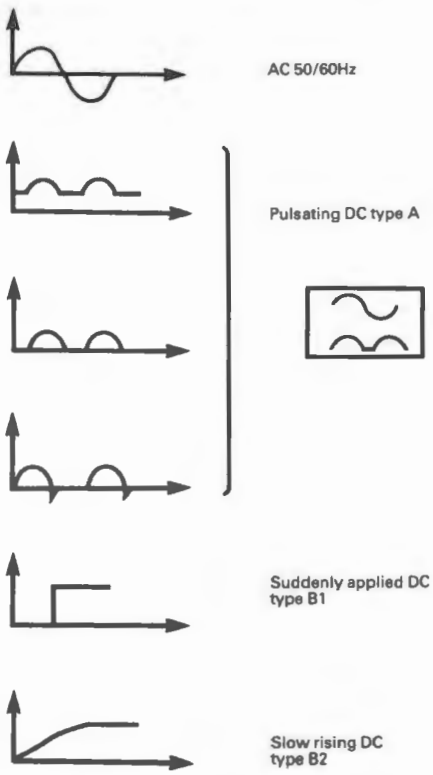
Fault indication

The unit is a switched double pole device with a visible indication of the nature of the fault interrupted.

Overload and short circuit faults will cause the green toggle switch to revert to the off 'O' position. The blue reset button will remain depressed so that, on clearling the fault, only the green toggle switch need be reset to on '1' for the power to be restored.

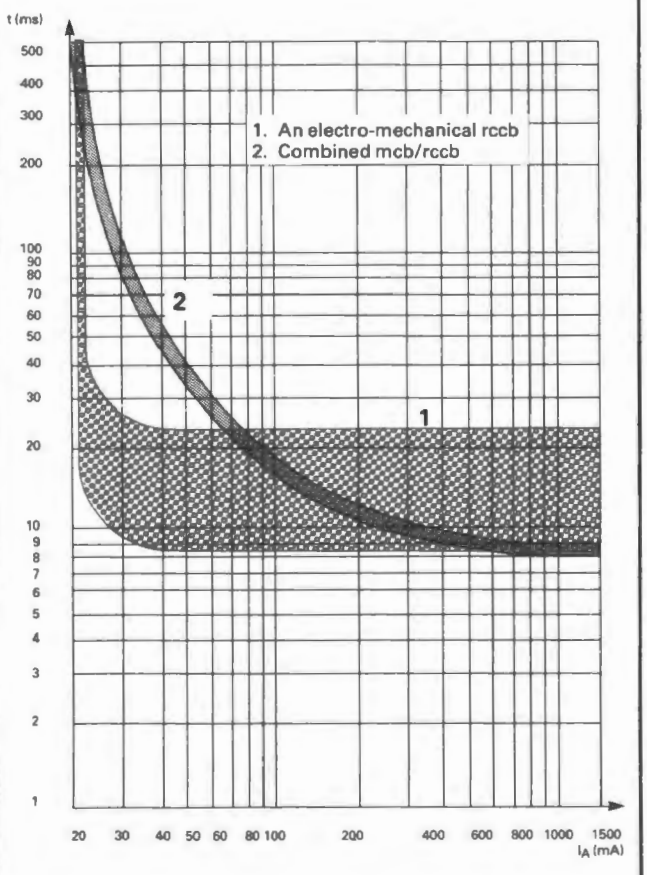
Earth leakage faults will cause both the green toggle switch and the blue reset button to revert to the off position. The unit may be reset in the same sequence as described above under 'testing'.

Figure 4 **Types of fault current**



The mcb/rccb will detect any of the above types of fault current.

Figure 5 **Typical tripping curves (30mA)**



Technical data

Rated voltage — 220/240V 50Hz
Rated current — See table on page 1
Rated breaking capacity — 3kA, two pole (M3)
Maximum permissible I^2t-value — $2000A^2s$ at 800A
Rated fault current — 30mA
Speed of operation (rccb) — See typical tripping curves
MCB time/current characteristics in accordance with the requirements in BS.3871, type 2
Permissible impulse voltage between phase and neutral — 6kV
Permissible impulse voltage between earth and neutral — 8kV
Operating temperature — −10°C to +40°C (in enclosure)
Storage temperature — −20°C to +85°C

RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company

Telephone: 0536 201234
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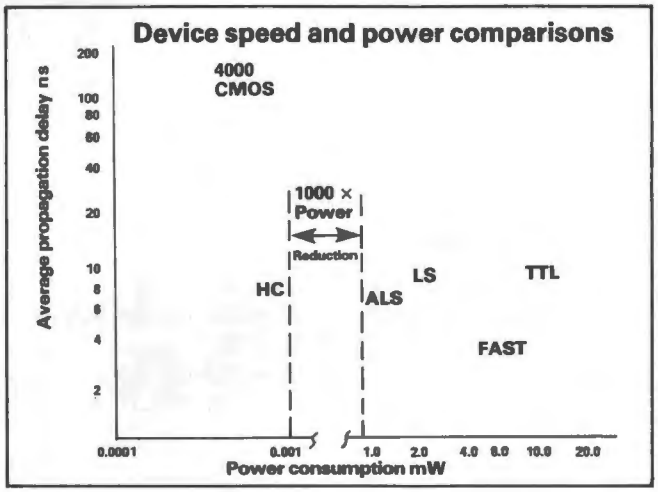
RS data

74 Series logic families



This data sheet gives the pin connections and availability for the six 74 series logic families offered.

Standard 74 Series TTL

A range of popular transistor – transistor logic integrated circuits for use in basic circuits. 5Vdc supply, 0°C to +70°C operating temperature range.

Low power Schottky 74 LS Series TTL

A Schottky process using shallower diffusions yields devices with a five fold decrease in power consumption and an increase in speed compared to standard 74 TTL. 5Vdc supply, 0°C to +70°C operating temperature range.

Advance low power Schottky 74 ALS TTL

Advanced low power Schottky TTL devices are directly compatible with LS and standard TTL devices. An advanced oxide isolated construction uses small geometries giving approximately twice the speed with half the power consumption of 74 LS TTL. 5Vdc supply, 0°C to +70°C operating temperature range.

FAST

FAST circuits are constructed using an advanced isoplanar II process. This produces transistors with very high, well controlled switching speeds, the extremely small parasitic capacitances give f_T values in excess of 5GHz. Propagation delays are typically 3ns with 4mW per gate power dissipation. This family is designed for use in all high speed high performance applications and may also be used as pin-for-pin 74S replacements with 3 to 4 times less power consumption and higher speed capabilities. 5Vdc supply, 0°C to +70°C operating temperature range.

High speed CMOS 74 HC and 74 HCT

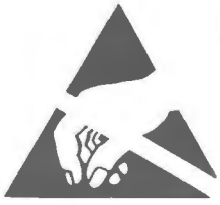
High speed CMOS devices are fabricated using the latest technology oxide isolated CMOS process giving good speed performance comparable with LS TTL but with much lower power consumption of the same order as 4000 CMOS.

Two families are offered 74 HC with CMOS compatible inputs for high noise immunity and 74 HCT with directly TTL compatible inputs. Both families outputs are compatible with TTL and CMOS. 74 HC devices work on a 2 to 6Vdc supply with 74 HCT types functioning with a 4.5 to 5.5Vdc supply. Operating temperature range for both families is a wide −40°C to +85°C.

Connections shown are top view. A 'negation' circle at any output or input within the schematic indicates that the terminal is active LOW or at clocking inputs the device is negative edge triggered.

Connections shown are top view. A 'negation' circle at any output or input within the schematic indicates that the terminal is active LOW or at clocking inputs the device is negative edge triggered.

Unused inputs should be connected to the appropriate defined logic level in order to achieve output conditions in line with the device truth table. As with standard CMOS high speed CMOS unused inputs must be connected to defined logic levels. For active HIGH inputs with standard TTL and ALS TTL a pull up resistor to V_{cc} should be used; up to 25 unused inputs can be connected to each resistor. With LS TTL, HC, HCT and FAST unused active HIGH inputs can be directly tied to +ve supply so long as the connecting leads are short and the supply is adequately decoupled. Unused active LOW inputs can be directly connected to ground with all families.



ATTENTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

HC, HCT and FAST devices

Abbreviations used throughout this data sheet

A, B, C, D and E	Data inputs binary weight (where applicable) A = 1; B = 2; C = 4; D = 8; E = 16
a, b, c, d, etc	Segment outputs on 7-segment decoder drive
BCD	Binary coded decimal
BI	Blanking input
$C_{in, out}$	Carry in or out
CEP	Count enable parallel input
CER	Count enable ripple input
CK	Clock
CS	Clip select
D, JK	Data input to flip-flops
EN	Enable
GND	Ground 0V terminal
I/O	Input/Output
LT	Lamp test
MR	Master test
OEN	Output enable
PE	Parallel enable (active low) input
Q	Output, may have a letter indicating weighting
RBI	Ripple blanking input
RBO	Ripple blanking output
RC, C, R	Capacitor and resistor timing on monostables
RCO	Ripple carry output
S	Sum output
SDL	Serial data in left shift
SDR	Serial data in right shift
SQ	Serial output
SR	Synchronous reset
TC	Terminal count output
V_{cc}	+ supply terminal
⎍	Schmitt device or function

Fan-in/Fan-out of logic families

1 unit load is:
High state 40μA
Low state 1.6mA

HC, HCT, LS TTL, 4000 CMOS and FAST characteristics

	Metal gate CMOS	LS TTL	HCT	HC	FAST
Supply voltage range (V_{CC})	3-15V	5V ± 5%	5V ± 10%	2-6V	5V ± 5%
Typical quiescent dissipation per gate	2.5nW	2mW	2.5nW	1μW	5.5mW
Max. quiescent current per package at 85°C	7.5μA	3mA	20μA	20μA	10.2mA
Typical power dissipation per gate (V_{CC} = 5V, C_L = 50pF) at 10kHz at 100kHz at 1MHz at 10MHz	 25μW 250μW 2.5mW	 2mW 2mW 2.8mW 12.5mW	 14μW 140μW 1.4mW 14mW	 14μW 140μW 1.4mW 14mW	 –
Typical propagation delay C_L = 15pF C_L = 100pF	 90ns 175ns	 10ns 17ns	 9ns 11.5ns	 8ns –	 3.7ns at C_L = 50pF
Max. operating frequency with C_L = 15pF	3MHz	25MHz	25MHz	40MHz	125MHz
Operating temperature range °C	–40 to +85	0 to +70	–40 to +85	–40 to +85	0 to +70

Typical Fan-ins/Fan-outs in unit loads

	Family	METAL GATE CMOS	METAL GATE HC	HCT	TTL	LSTTL	ALS	FAST
Fan-In	Low state	0.025	0.05	0.05	1	0.25	0.0625	0.375
	High state	0.025	0.05	0.05	1	0.5	0.5	0.5
Fan-Out	Low state	0.5	2.5	2.5	10	5	5	12.5
	High state	0.5	2.5	2.5	20	10	10	25

High speed CMOS comparisons

HC logic implements TTL equivalent functions with the same pin outs as TTL. HC is not designed to be directly plug-in replaceable, but, with care, some TTL systems can be converted to 74HC with little or no modification. The replaceability of HC is determined by several factors.

One factor is the difference in input levels. In systems where all TTL is not being replaced and TTL outputs feed CMOS inputs, the input high voltages, as specified, are not totally compatible. Although TTL outputs will typically drive HC inputs correctly, an external pull-up resistor should be added to the TTL outputs, or a 74HCT TTL compatible circuit should be used.

HCT inputs are directly compatible with TTL outputs, and HCT outputs are completely compatible with the various TTL family's input specifications; therefore, there is no problem when HCT and TTL is mixed. Another source of possible problems can occur when the LS design floats device inputs. This practice is not recommended when using LS-TTL, but it is sometimes done. Usually, TTL inputs float high; however, CMOS inputs may float either high or low depending on the static charge on the input. It is therefore important to always tie unused CMOS inputs to either V_{CC} or ground to avoid incorrect logic functioning.

A third factor to consider when replacing any TTL logic is ac performance. The logic functions provided by 74 HCT are equivalent to LS-TTL, and the propagation delay, set-up and hold times are similar to LS. However, there are some differences in the way CMOS circuits are implemented which will cause differences in speed. For the most part, these differences are minor, but it is important to verify that they do not affect the design.

Conclusion

The 74 HC families represent a major step forward in CMOS performance. They are capable of being designed into virtually any application which now uses LS-TTL with substantial improvement in power consumption, or used exclusively for high performance new designs. ALS offers faster speeds than HCMOS, but still does not have the input and output advantages or the lower power consumption of CMOS. Because of its high input impedance and large output drive, HC logic is actually easier to use.

Figure 1 **Power-speed product for HCMOS and LSTTL gate shows the advantage of HCMOS at frequencies below 10MHz**

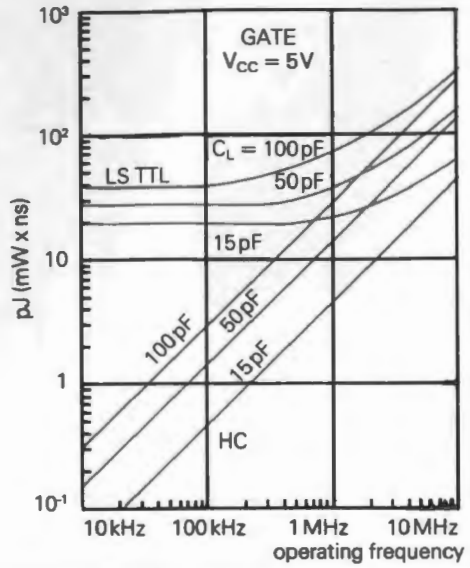


Figure 2 **The power cross-over frequency is about 5MHz for a single gate and above 10MHz for a single flip-flop**

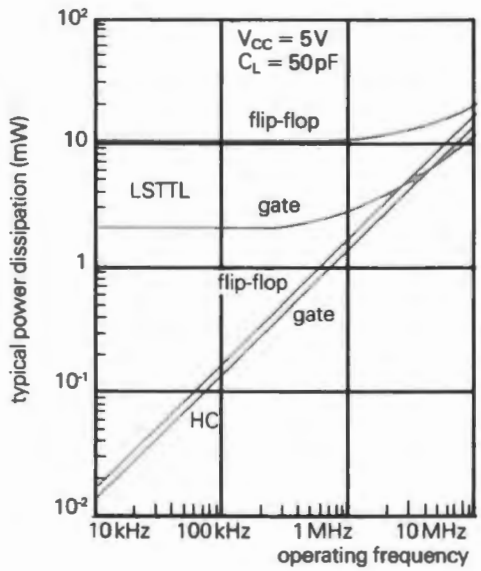


Figure 3 **A simulated MSI circuit shows distinct power saving at all frequencies**

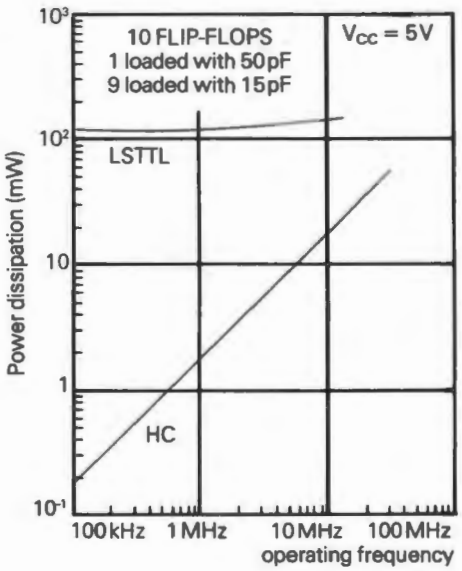


Figure 4 **Input current for HCMOS is symmetrical and much lower than that of LSTTL. Theoretically, one HCMOS output can drive nearly a thousand inputs, but capacitance considerations will probably predominate**

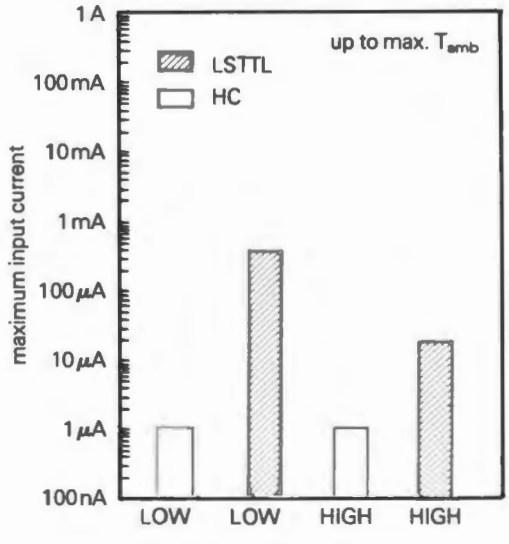


Figure 5 **As its name suggests high speed CMOS is fast. Gate propagation delay with 50pF load is ⅛th that of earlier silicon gate CMOS and 1/12th that of metal gate CMOS**

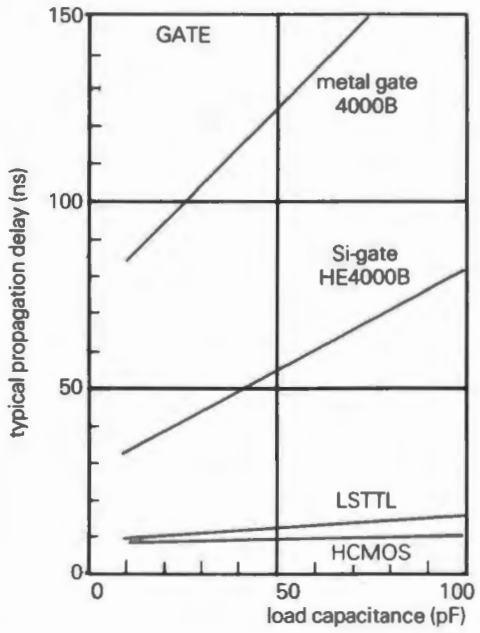


Figure 6 **Even a total HCMOS package of four gates under worst case static conditions consumes more than two orders of magnitude less power than an equivalent LSTTL gate package**

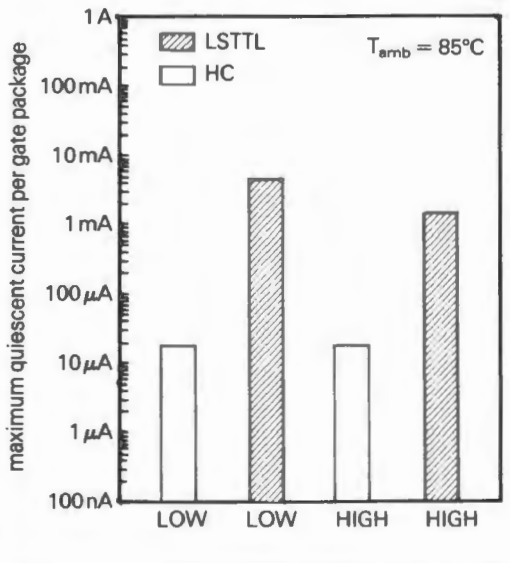


Figure 7 **Unlike LSTTL circuits, HCMOS circuits consume very little power when they are not switching**

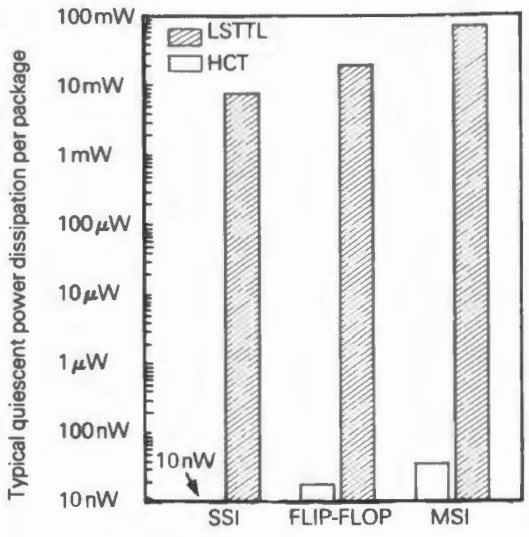
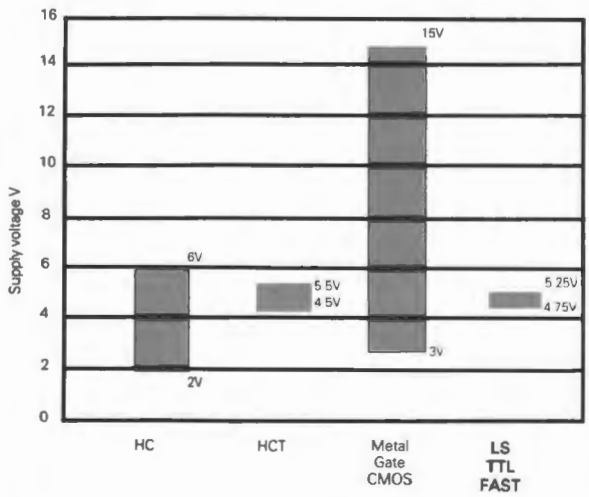


Figure 8 **Comparison of supply voltage range**



To summarise, the outstanding features of high-speed CMOS are:

- Low power dissipation. Typical quiescent current per package is 2nA for gates, 4nA for flip-flops and 8nA for MSI. For gates, maximum quiescent current per package at 85°C is 20μA. Typical gate operating current is 3μA at 10kHz, 30μA at 100kHz and 300μA at 1MHz with a 5V supply. This compares with LS TTL operating currents of 400μA up to 100kHz and 560μA at 1MHz for each gate.
- Typical operating frequency up to 50MHz (15pF, 25°C). With a 5V supply, typical propagation delay for a gate is 9 to 11.5ns for either HIGH to LOW or LOW to HIGH transitions into capacitive loads of between 15 and 100pF. This is a fifth of the gate propagation delay for earlier silicon-gate CMOS.
- Functions and pinning identical to popular LSTTL.
- TTL input switching level HCT devices. These circuits operate from a 5V ±10% supply and are mainly for use as pin-compatible CMOS replacements for LS TTL to reduce power consumption without loss of speed. These types are also suitable for converting switching levels from TTL to CMOS. CMOS input switching level HC devices, with an operating supply voltage of 2 to 6V, are ideal for wide noise margin new designs.
- Fan-out of 10 LS TTL loads (4mA) for standard outputs, 15 LS TTL loads (6mA) for bus driver outputs. This is ten times more drive capability than earlier CMOS circuits.
- Standardised output buffers allow symmetrical output current sourcing and sinking for equal output rise and fall times (7.5ns for standard outputs and 6ns for bus driver outputs). This results in simplified design combined with optimum speed and performance.
- High immunity to electrostatic discharges.
- Wide operating temperature range: −40°C to +85°C.
- Virtually latch-up free.

FAST

Mixing with other logic families

High speed 74F devices are designed with relatively low input and output impedances. The speed is determined by fast rise and fall times internally as well as at the input and output nodes. These fast transitions cause noise of various types in the system. Power and ground line noise is generated by the large currents needed to charge and discharge the circuit and load capacitances, signal line noise is generated by the fast output transitions and the relatively low output impedances which tend to increase reflections. The noise generated in 74F systems can be minimised in systems designed with very short signal leads, ground planes and well designed bypassed power distribution networks.

Mixing slower speed logic families such as 74TTL and 74LSTTL with 74F is possible but must be done with caution. Slower speed families tend to be more susceptible to induced noise than the higher speed families this being due to their higher input and output impedances. Where families are mixed, separate or isolated power and ground systems are recommended. Also the slower speed family input signal lines should not be run adjacent to lines driven by 74F devices.

Figure 9 **Transfer functions at Room Temperature**

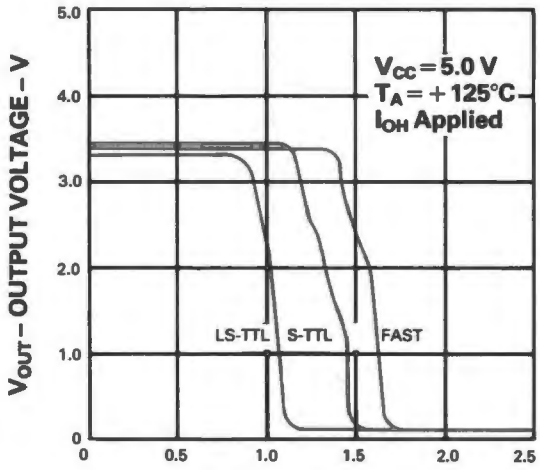


Figure 10 **Propagation delay vs V_{CC}**

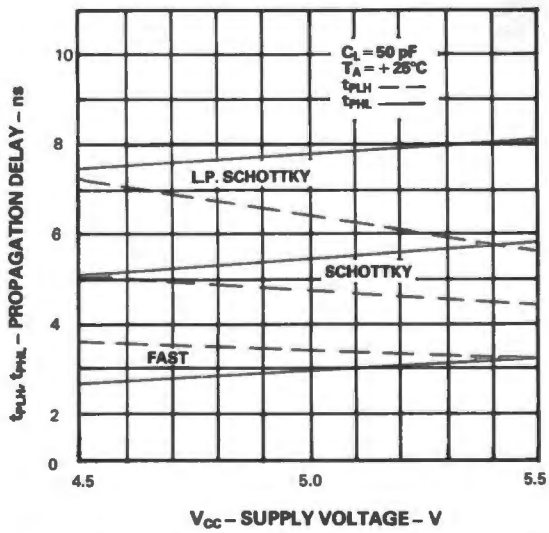


Figure 11 **Propagation delay vs Temperature**

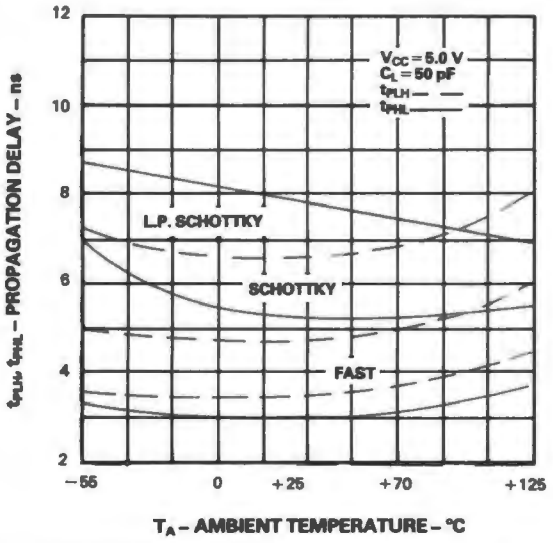
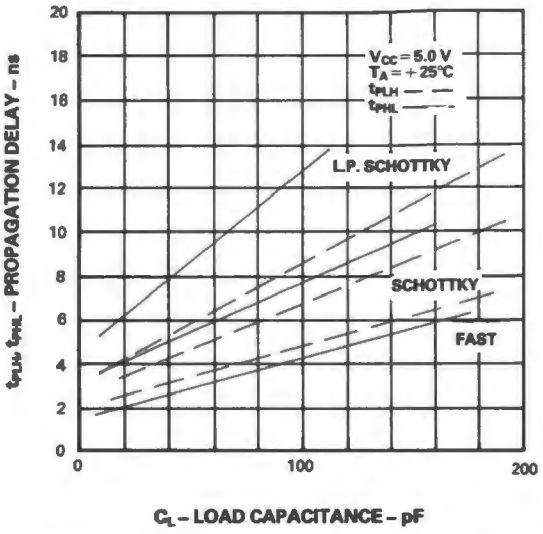
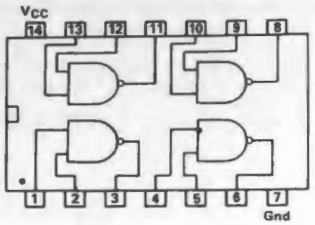


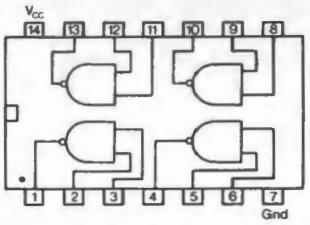
Figure 12 **Propagation delay vs Load Capacitance**



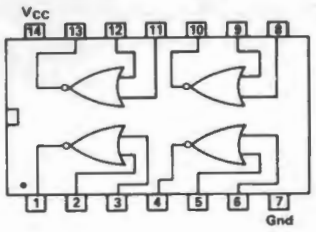
00 Quadruple 2-input NAND gate



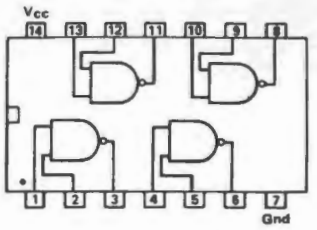
01 Quadruple 2-input NAND gate with open collector output



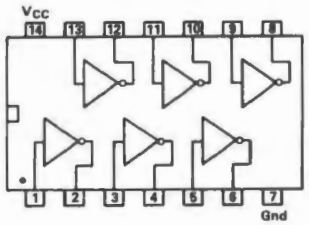
02 Quadruple 2-input NOR gate



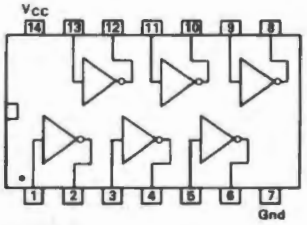
03 Quadruple 2-input NAND gate — open collector inputs



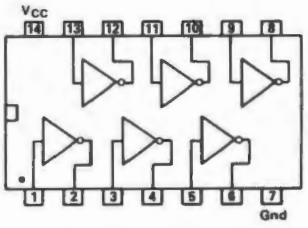
04 Hex inverter



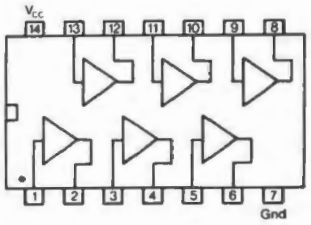
05 Hex inverter-open collector outputs



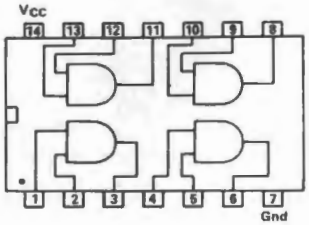
06 Hex inverter with high voltage open collector output



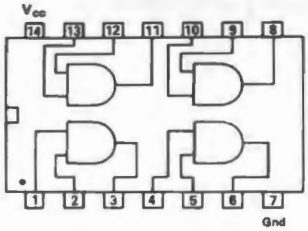
07 Hex driver with open collector output



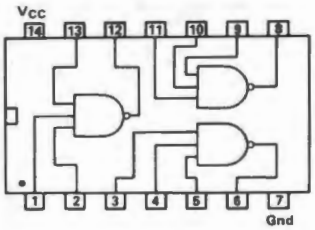
08 Quadruple 2-input AND gate



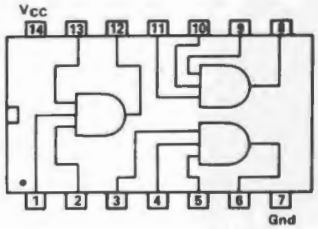
09 Quad 2-input AND gate-open collector outputs



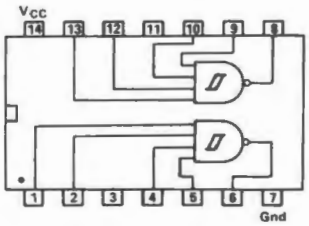
10 Triple 3-input NAND gate



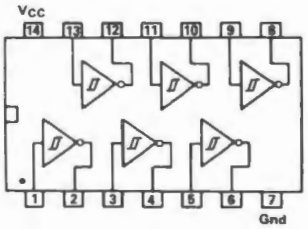
11 Triple 3-input AND gate



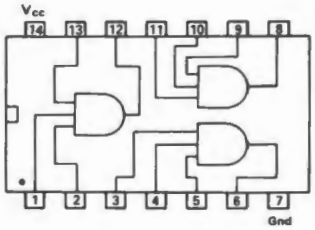
13 Dual 4-input NAND gate Schmitt trigger



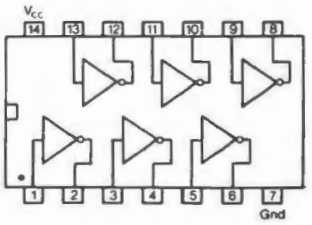
14 Hex Schmitt Trigger



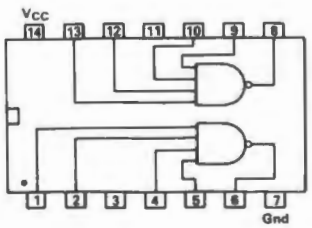
15 Triple 3- input AND gate — open collector outputs



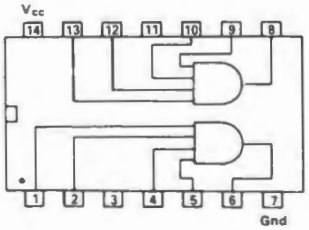
16 Hex Inverter with open collector output



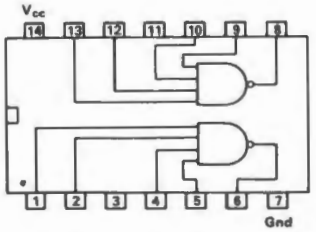
20 Dual 4-input NAND gate



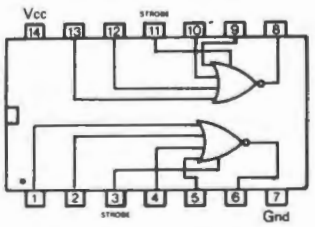
21 Dual 4-input AND gate



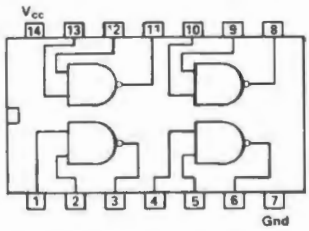
22 Dual 4-input NAND gate — open collector outputs



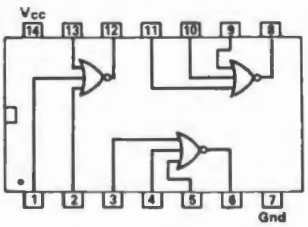
25 Dual 4-input NOR gate with strobe



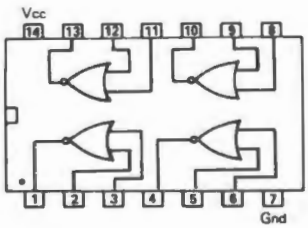
26 Quad 2-input NAND buffer-open collector outputs



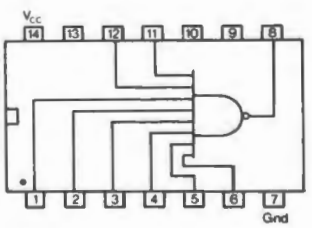
27 Triple 3-input NOR gate



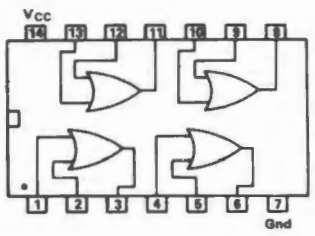
28 Quad 2-input NOR buffer



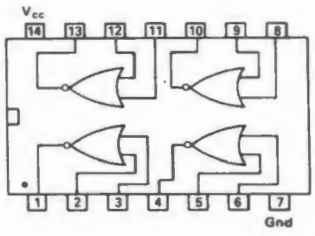
30 8-input NAND gate



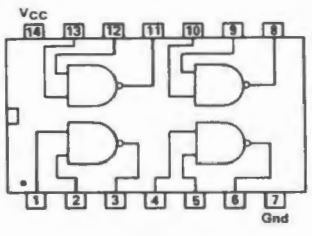
32 Quadruple 2-input OR gate



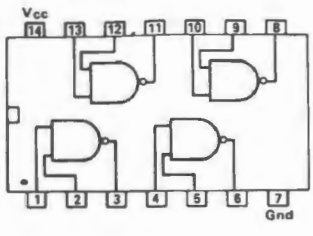
33 Quad 2-input NOR buffer-open collector outputs



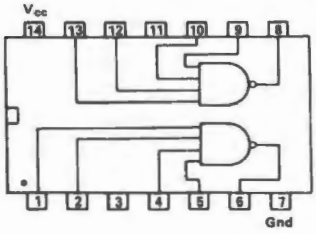
37 Quadruple 2-input NAND buffer



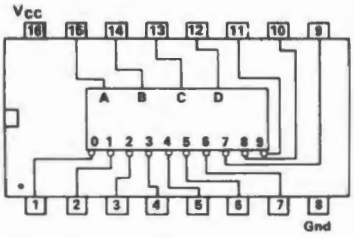
38 Quadruple 2-input NAND buffer — open collector outputs



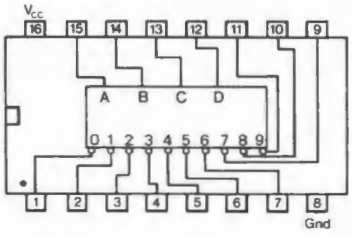
40 Dual 4-input NAND buffer



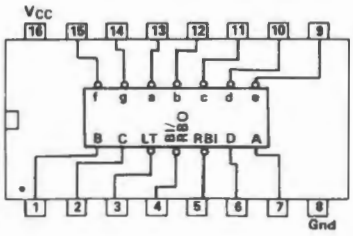
42 BCD-to-decimal decoder



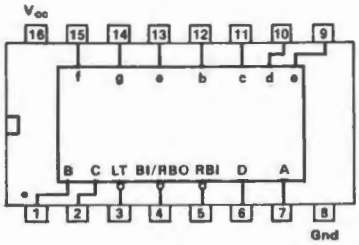
45 BCD-to decimal decoder/driver



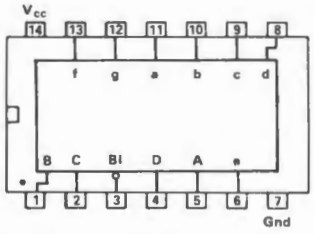
47 BCD-to-7 segment decoder/driver — open collector outputs



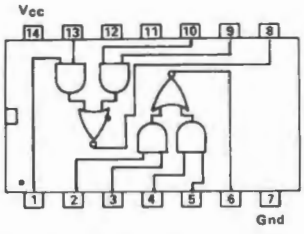
48 BCD-to-7 segment decoder/driver



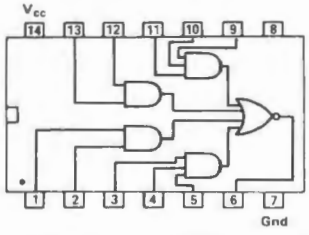
49 BCD-to-7-segment decoder/driver — open collector outputs



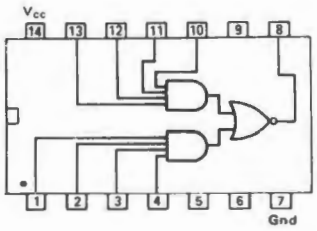
51 Dual 2-wide 2-input/3-input AND-OR-INVERT gate



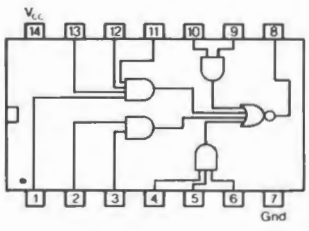
54 3-2-2-3 input AND-OR-INVERT gate



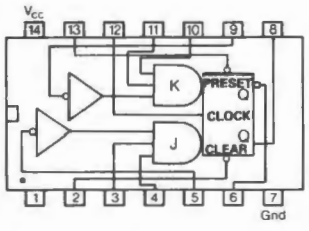
55 2-wide 4-input AND-OR-INVERT gate



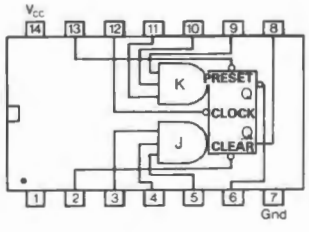
64 4-2-3-2- Input AND-OR invert gate



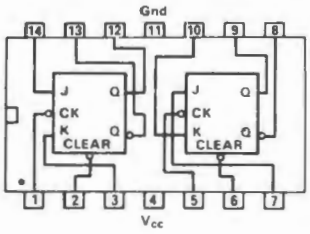
70 J-K flip-flop



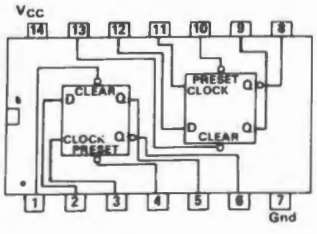
72 J-K master-slave flip-flop



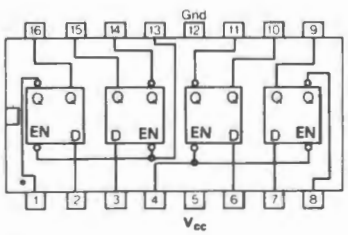
73 Dual JK negative edge-triggered Flip-Flop



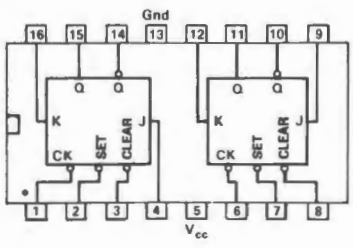
74 Dual D-type edge-triggered Flip-Flop



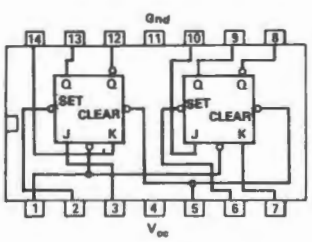
75 4-bit D Latch



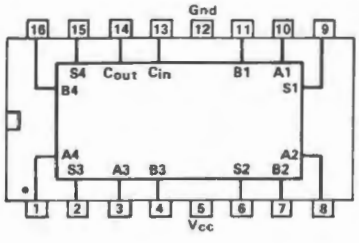
76 Dual JK Flip-Flop with set and clear



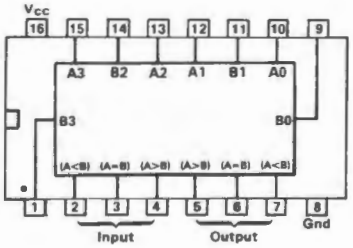
78 Dual JK Flip-Flop



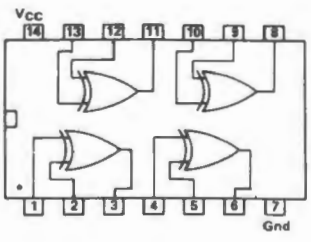
83A 4-bit Binary full adder



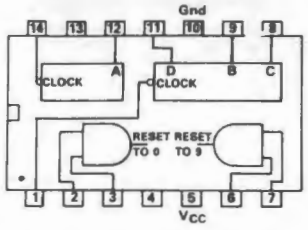
85 4-bit magnitude comparator



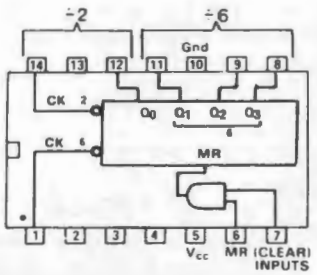
86 Quadruple 2-input exclusive OR gate



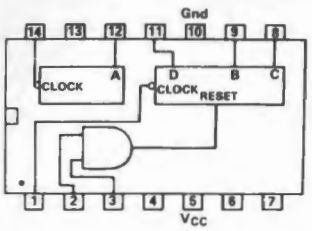
90 Decade counter



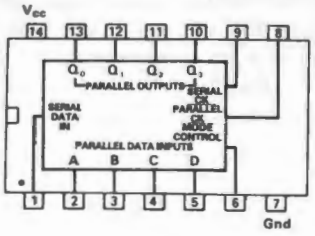
92 Divide-by-twelve counter



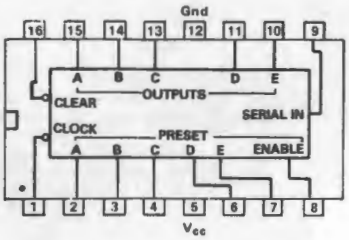
93 4-bit binary counter



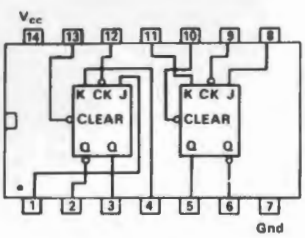
95B 4-bit shift register



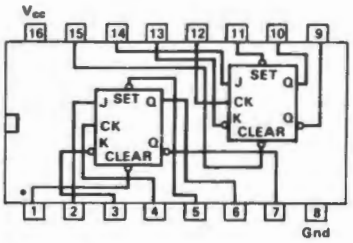
96 5-bit shift register



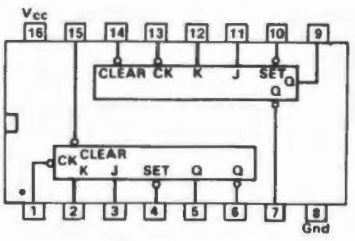
107 Dual JK Flip-Flop



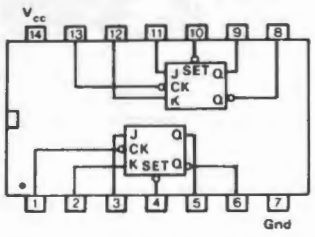
109 Dual JK positive edge-triggered Flip-Flop



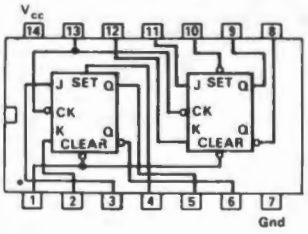
112 Dual JK edge triggered flip-flop



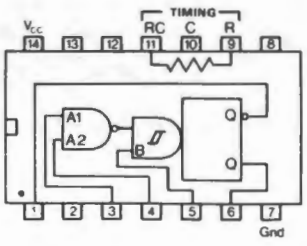
113 Dual JK negative edge-triggered Flip-Flop



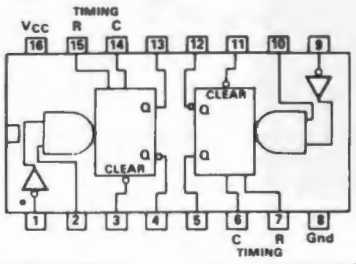
114 Dual JK negative edge-triggered Flip-Flop



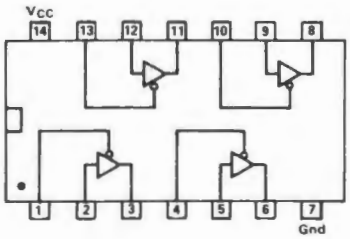
121 Monostable multivibrator



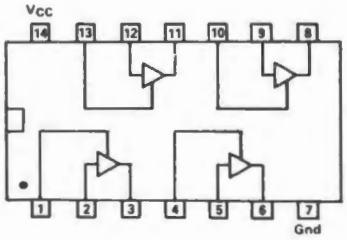
123 Dual monostable - retriggerable



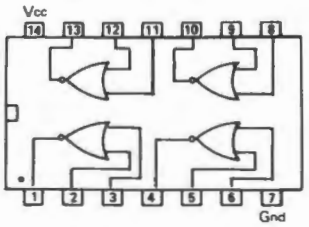
125 Quad 3-state buffer (active low enable)



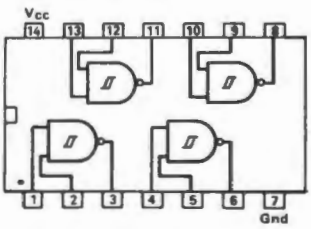
126 Quad 3-state buffer (active high enable)



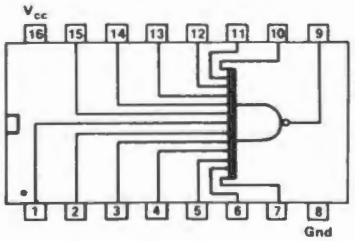
128 Quad line driver



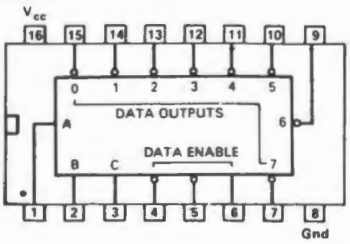
132 Quadruple 2-input NAND Schmitt gate



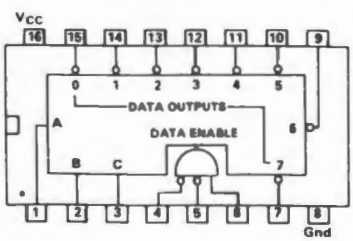
133 13-input NAND gate



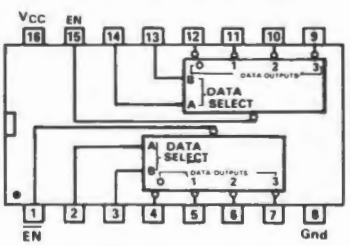
137 3-line to 8-line Decoder/Demultiplexer with address latches



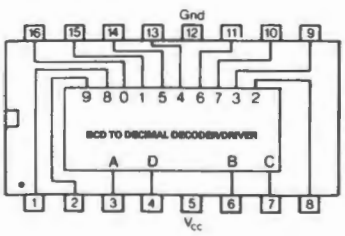
138 3 to 8 line Decoder/Multiplexer



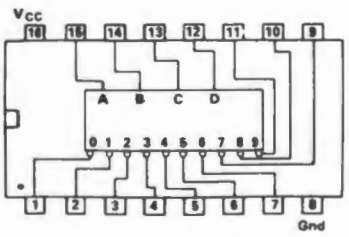
139 Dual 1 of 4 Decoder



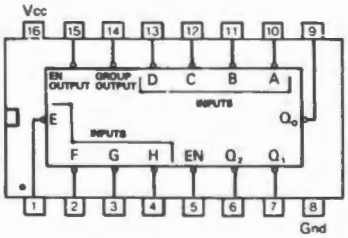
141 BCD-to-decimal decoder driver



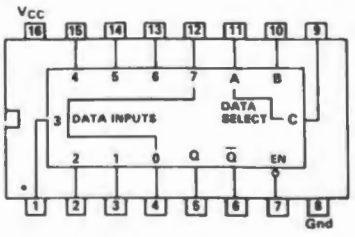
145 BCD-to-decimal decoder/driver



148 Octal priority encoder 8 line to 3 line

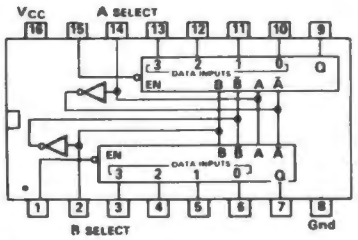


151 1 of 8 Data Selector/Multiplexer

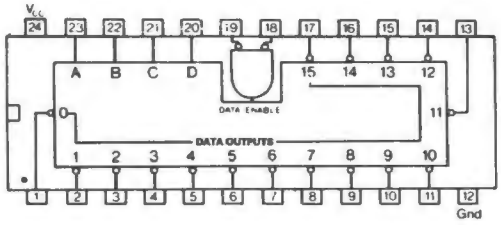


5667

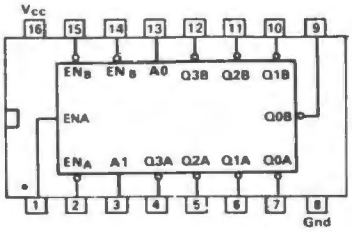
153 Dual 4-line to 1-line Data Selectors/Multiplexers



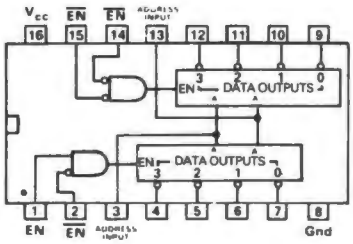
154 4 to 16 line Decoder



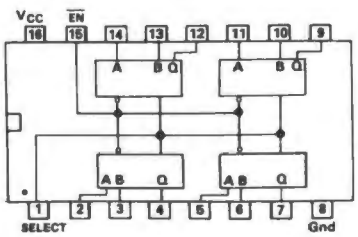
155 Dual 1 of 4 Decoder/Demultiplexer



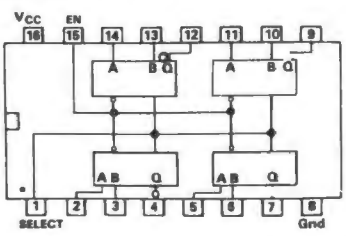
156 Dual 1-of-4 Decoder/Demultiplexer with open collector outputs



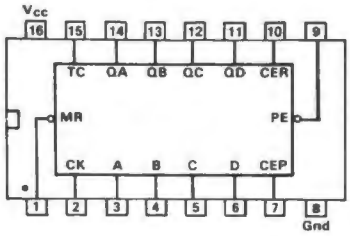
157 Quad 2 to 1-line Data Selectors /Multiplexers



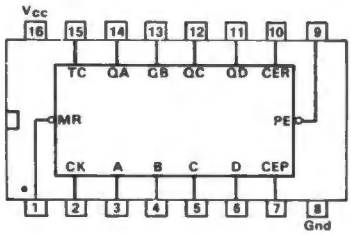
158 Quad 2 to 1-line Data selectors/Multiplexers with Inverted outputs



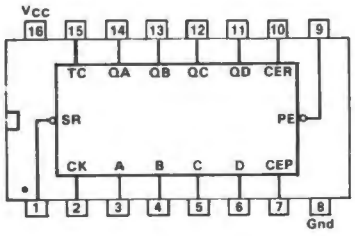
160 BCD decade counter — asynchronous reset



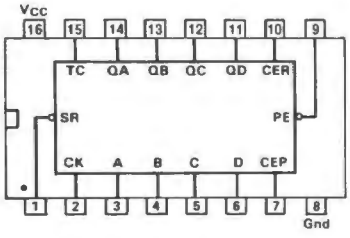
161 Binary counter — asynchronous reset



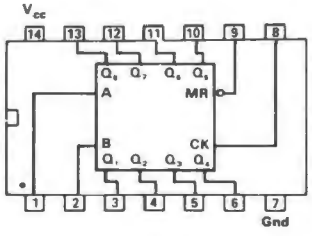
162 BCD counter — synchronous reset



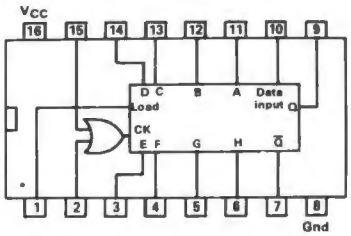
163 Binary counter — synchronous reset



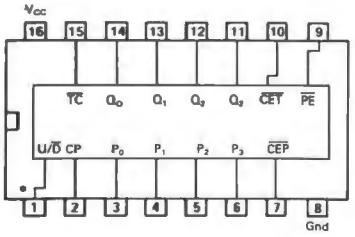
164 Serial-in parallel-out shift register



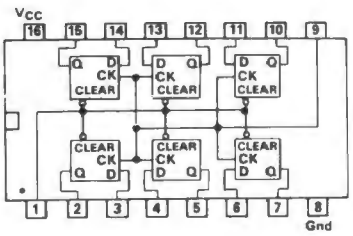
165 8-bit parallel to serial converter



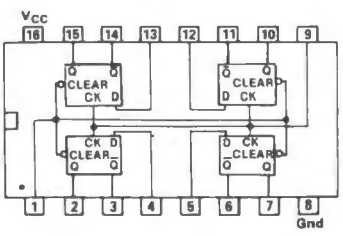
169 4-Stage synchronous bidirectional counter



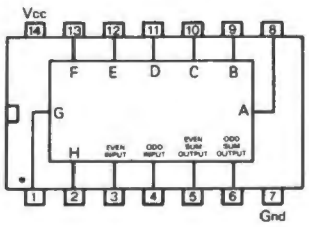
174 Hex D-type Flip-Flops



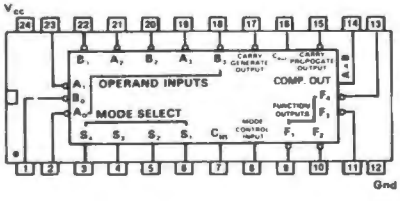
175 Quad D-type Flip-Flops



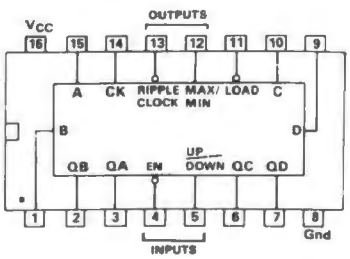
180 Parity generator/checker 9-bit odd/even



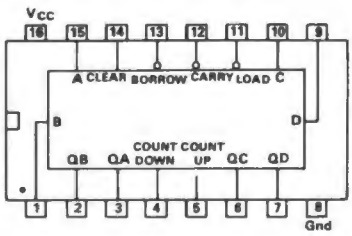
181 4-bit arithmetic logic unit



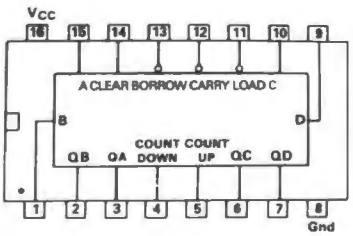
191 Binary synchronous up/down counter



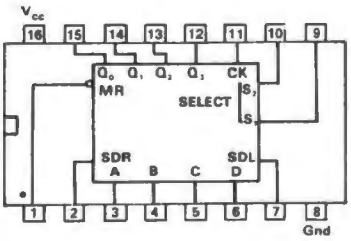
192 Up/Down decade counter — with preset inputs



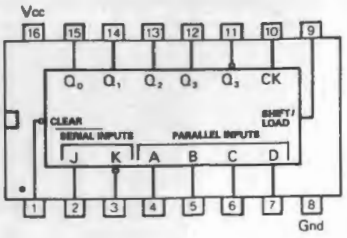
193 Up/Down binary counter-with preset inputs



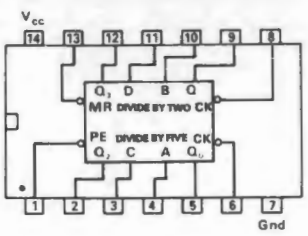
194 A 4-bit bidirectional universal shift register



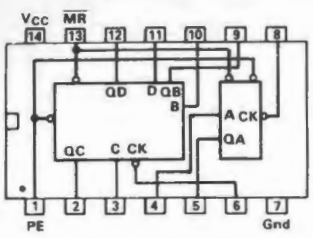
195 4-bit parallel-access shift register



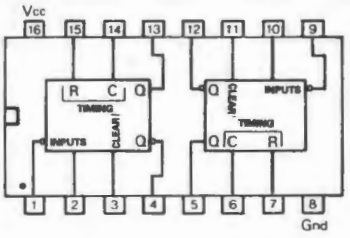
196 4-stage presettable ripple counter



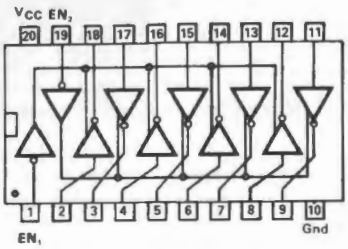
197 Presettable binary ripple counter



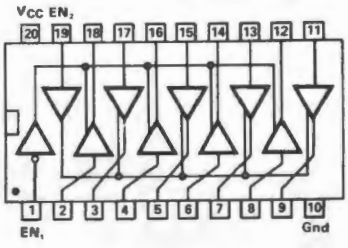
221 Dual monostable multivibrator



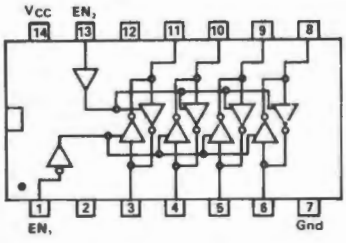
240 Octal buffer — three state inverting



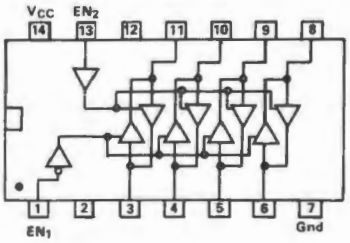
241 Octal buffer — three state non-inverting



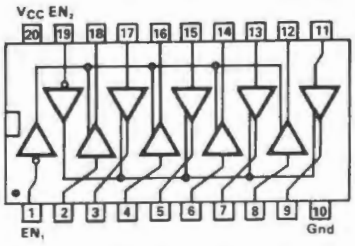
242 Quad bus transceiver — inverting



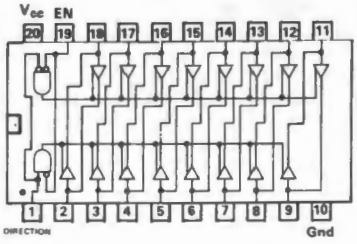
243 Quad bus transceiver — non-inverting



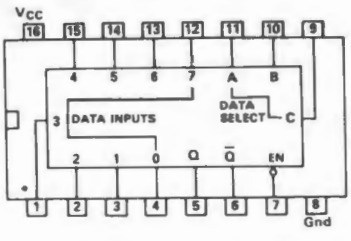
244 Octal buffer — three state non-inverting



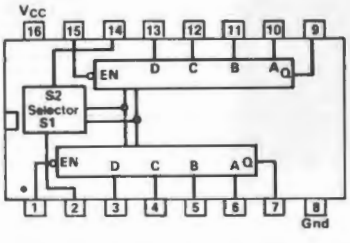
245 Octal bus transceiver with 3 state outputs



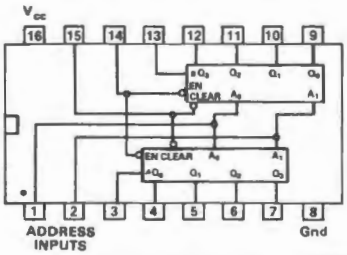
251 1 of 8 Data selector/Multiplexer with 3 state outputs



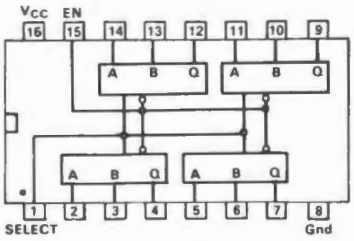
253 Dual 4 - input multiplexer with 3 state outputs



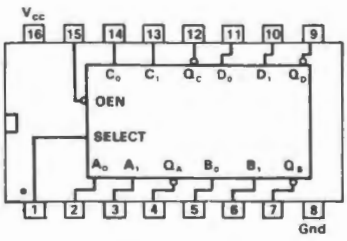
256 Dual 4-bit addressable latch



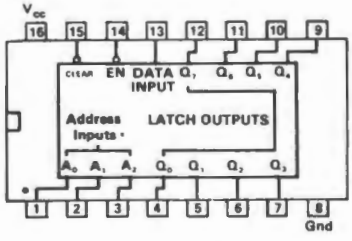
257 Quad 2-input multiplexer with 3 state outputs



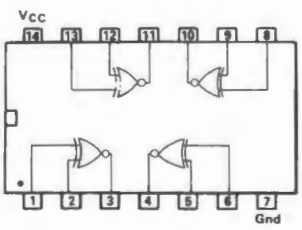
258 Quad 2-input multiplexer with 3 state outputs



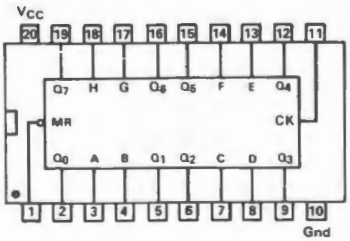
259 8-bit addressable latch



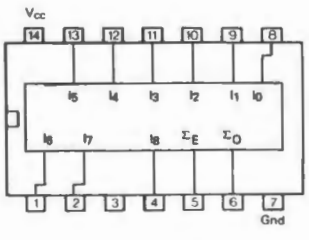
266 Quad 2-input Exclusive NOR gate



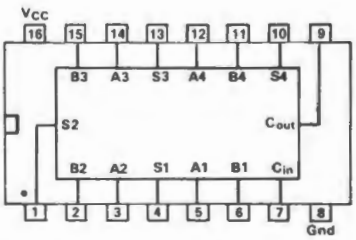
273 8-bit register with clear



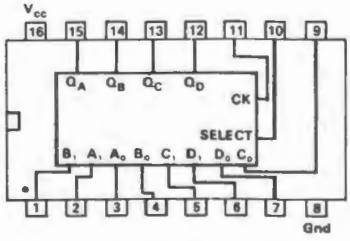
280 9-Bit parity generator/checker



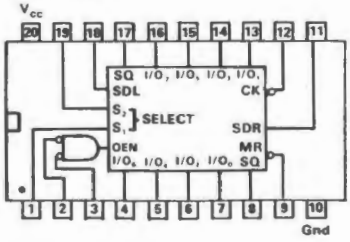
283 4-bit binary full adder



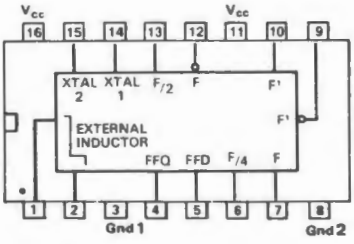
298 Quad 2-port register (Quad 2-input multiplexer with storage)



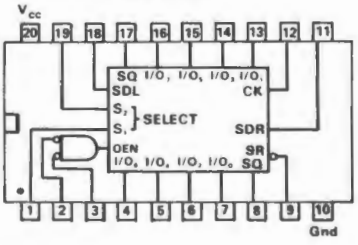
299 8-bit-universal shift /storage register with common parallel I/O pins 3 state



321 Crystal controlled oscillator

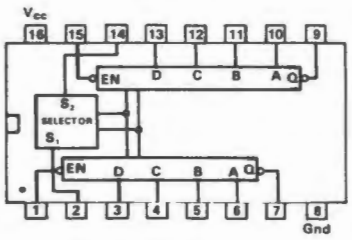


323 8-bit universal shift/storage register with synchronous reset and common I/O pins 3 state

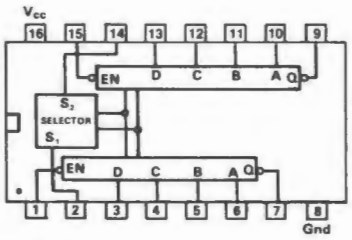


5667

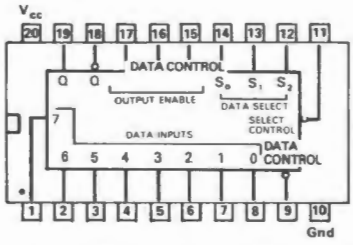
352 Dual 4-input multiplexer inverting



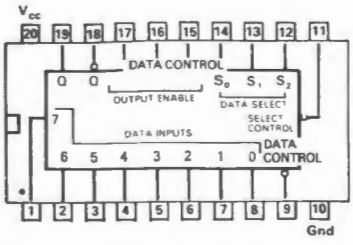
353 Dual 4-input multiplexer with 3 state outputs inverting



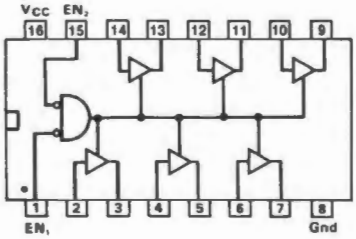
354 8-line to 1-line data selector/multiplexer/register



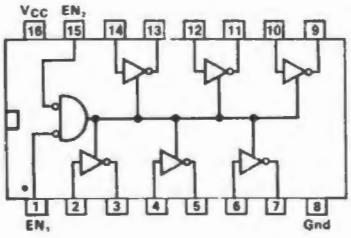
356 8-line to 1-line data selector/multiplexer/register



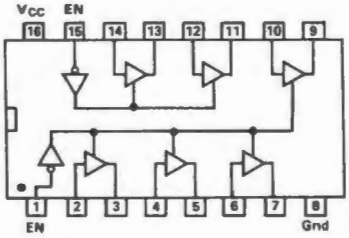
365 Hex 3 state buffer non-inverting



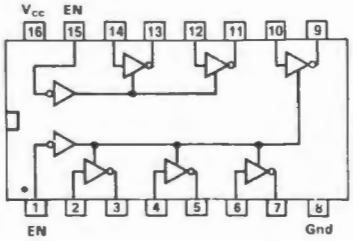
366 Hex 3 state buffer inverting



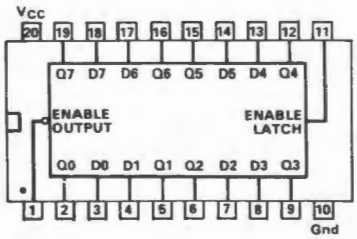
367 Hex 3-state buffer



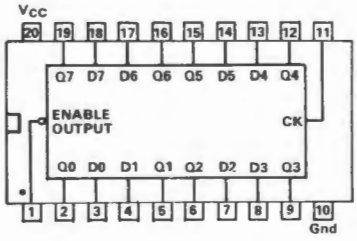
368 Hex 3-state inverter buffer (separate 2-bit & 4-bit sections)



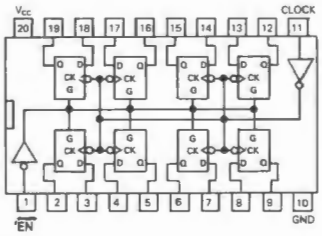
373 Octal transparent latch with 3 state outputs



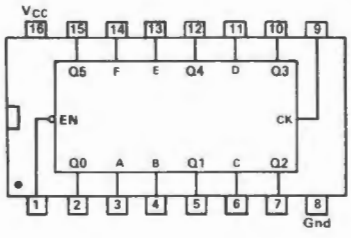
374 Octal D-type flip-flop with 3 state outputs



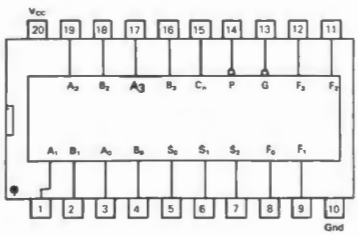
377 Octal D-type flip-flop with enable



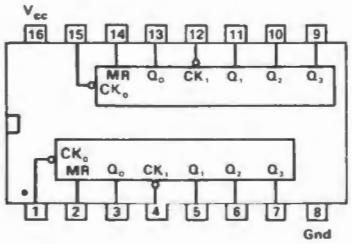
378 Hex D register



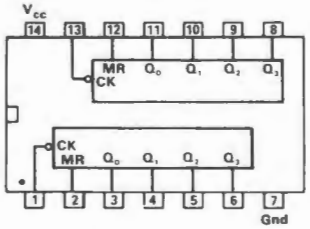
381 4-Bit arithmetic logic unit



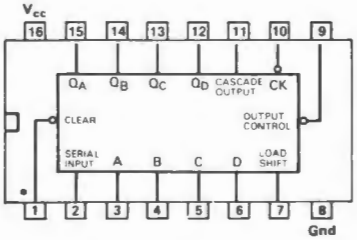
390 Dual decade counter



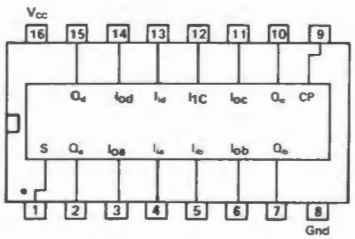
393 Dual 4 stage binary counter



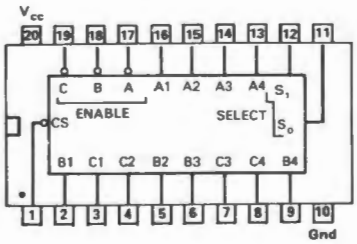
395 4-bit cascadable shift register 3 state



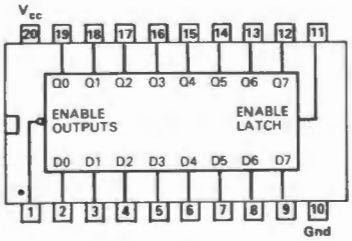
399 Quad 2-part register



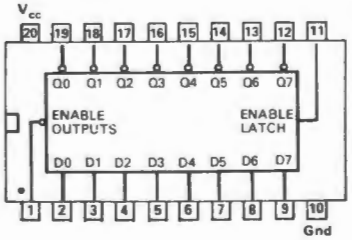
442, 443, 444 Quad tridirectional bus transceivers 3 state



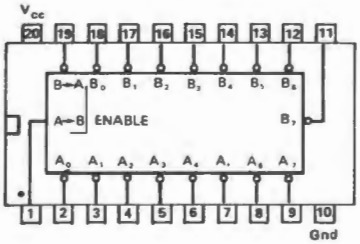
573 Octal D-type transparent latch



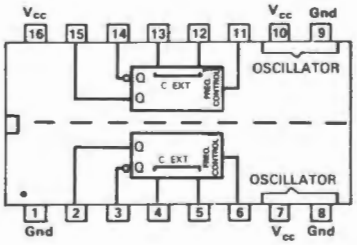
580 Octal D-type transparent latch inverted outputs



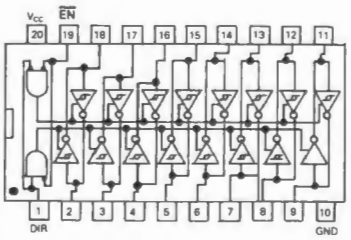
620 Octal bus transceiver



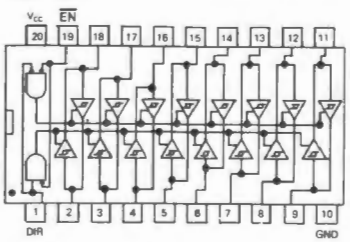
625 Voltage controlled oscillator



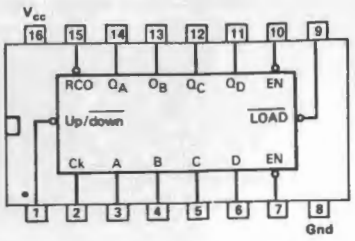
640 Tri-state, inverting octal bus transceiver



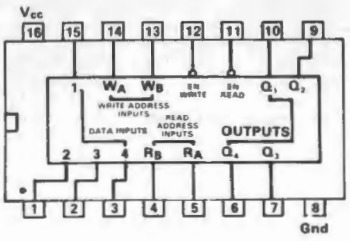
643 Tri-state, true and inverting octal bus transceiver



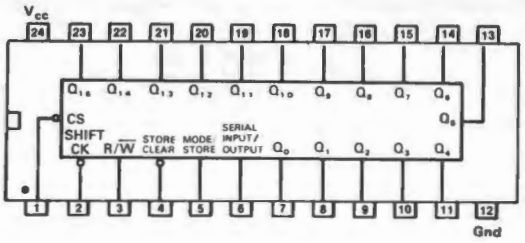
669 Up/down binary counter synchronous



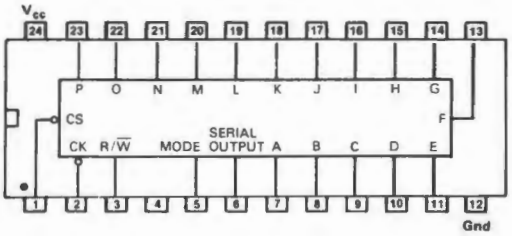
670 4 x 4 Register file with 3-state outputs



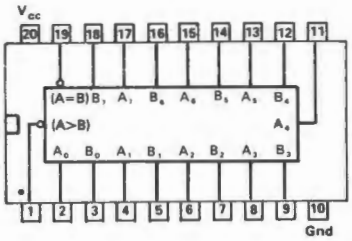
673 16-bit shift register, serial to parallel



674 16-bit shift register, parallel to serial



682 8-bit magnitude comparator



RS data

Standard LS, ALS, HC, HCT and FAST availability guide

	STD	LS	ALS	HC	HCT	FAST
00	■	■	■	■	■	■
01	■					
02	■	■	■	■		■
03	■	■	■	■		
04	■	■	■	■	■	■
05		■	■			
06	■					
07	■					
08	■	■		■	■	■
09		■	■			
10	■	■	■	■	■	■
11		■	■		■	■
13	■	■				
14	■	■		■		■
15		■				
16	■					
20	■	■	■			■
21		■	■			
22		■				
25	■					
26		■				
27	■	■	■		■	
28	■					
30	■	■	■	■		
32	■	■	■	■		■
33		■	■			
37	■	■	■			■
38	■	■	■			■
40	■	■				
42	■					
45	■					
47	■	■				
48		■				
49		■				
51	■	■				
54		■				
55		■				

	STD	LS	ALS	HC	HCT	FAST
64						■
70	■					
72	■					
73	■	■				
74	■	■	■	■		■
75	■	■		■		
76	■	■		■		
78		■				
83		■				
85		■		■		■
86	■	■			■	■
90	■	■				
92		■				
93	■	■				
95	■	■				
96	■					
107	■	■				
109	■	■				■
112	■	■	■			
113	■	■				
114	■	■				
121	■					
123	■	■				
125	■	■				
126	■	■				
128	■	■				
132	■	■				■
133	■	■				
137	■	■				
138	■	■		■	■	■
139	■	■		■	■	■
141	■	■				
145		■				
148	■					
151	■	■		■	■	■
153	■	■		■		■
154	■				■	■

	STD	LS	ALS	HC	HCT	FAST
155	■	■				
156		■				
157	■	■		■		■
158		■				■
160		■				
161	■	■		■		■
162		■				
163		■		■		■
164		■		■	■	■
165		■			■	
169						■
174	■	■		■	■	■
175	■	■		■		■
180	■					
181		■				
191	■	■				
192	■	■				
193	■	■				
194	■	■				■
195	■	■				
196	■	■				
197	■	■				
221	■					
240						■
241		■			■	■
242		■				■
243		■				
244		■		■	■	■
245		■				■
251		■			■	
253		■				
256		■				
257		■				■
258		■				
259	■	■		■		
266		■		■		
273	■	■		■		

	STD	LS	ALS	HC	HCT	FAST
280						■
283	■	■				■
298		■				
299		■				
321		■				
323		■				
352		■				
353		■				
354		■				
356		■				
365	■	■				
366		■				
367	■	■				
368		■				
373		■				■
374		■		■		■
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378		■				
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395		■				
399		■				■
442		■				
443		■				
444		■				
573		■				■
580		■		■		
620		■				
625		■				
640		■				■
643		■				■
669		■				
670		■				
673		■				
674		■				
682		■				

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An Electrocomponents Group Company

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Teledata keyboard

Stock number 333-467 & 333-473

The RS 69-key teledata keyboards are intended for use with Viewdata (Prestel) and other compatible message sending systems. Very high reliability is achieved by utilizing low profile, full key travel, sealed contact keyboard switches. A silicon rubber toroidal seal prevents the ingress of dirt and moisture enabling silver contacts to be used. Silver is less expensive and has a lower contact resistance than gold. The keycaps are ⅝in double shot moulded brown with white lettering. The switches are compatible with the RS low profile keyboard switches and the keytops are compatible with the RS ⅝in blank charcoal coloured keytops (see current RS catalogue for details).

Features

- Viewdata (Prestel) compatible
- Beige cover, with brown end castings and keycaps
- Low profile, compact design, D146, W362, H23
- Serial and parallel versions with 1.5m flying leads terminated with a 6 pin DIN plug and a 15 pin D-type plug respectively
- Encoding via a COP402N microprocessor
- Life 10 x 10^6 switch operations
- 2-key rollover
- 69 keys
- Single rail operating voltage +5V
- Low contact resistance 20mΩ
- Switch de-bounce time 3ms
- Operating temperature range 0°C to +65°C

Figure 1 **Keytop legend drawing.**

Encoding

The alpha-numeric encoding is ASCII compatible (see Figure 2). Each key when depressed will transmit one of up to three keycodes (specific for each key) depending upon the mode of operation: lower case, caps lock, shift and control modes. Modes are selected by the shift, caps lock and control keys (see Figure 2).

Lower case mode

Caps lock LED indicator OFF in this mode, lower case letters or the lower character on double function keys will be transmitted.

Caps lock mode

Selected by depressing the caps lock key, an LED indicator will illuminate when selected. This key toggles the caps lock mode on and off. With the LED ON the keyboard will transmit upper case letters and the lower characters on double function keys.

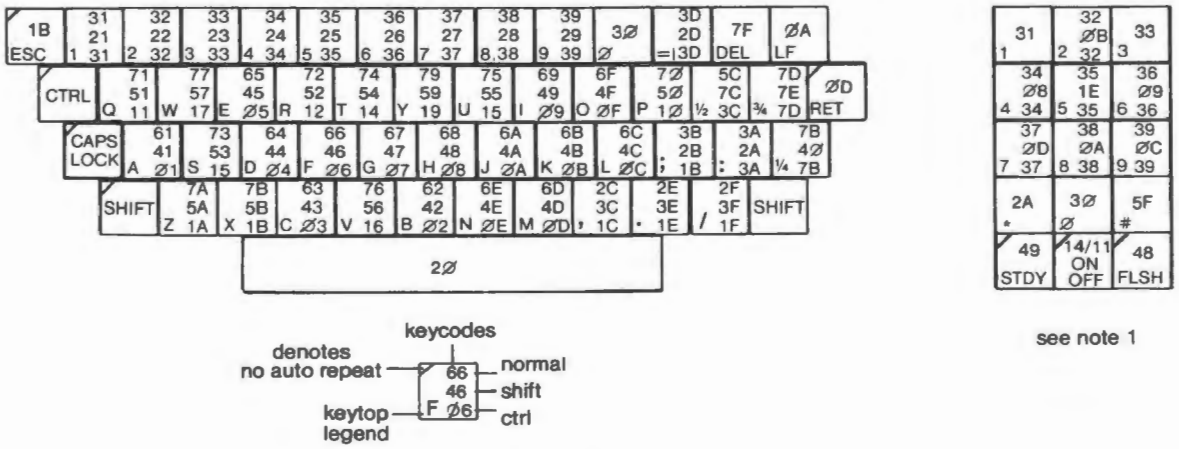
Upper case mode

Selected by holding down the shift key whilst depressing any other key. The 'shifted' character will be transmitted i.e upper case letters or the upper characters on double function keys.

Control mode

Selected by holding down the control key whilst depressing any other key. The control keycode of the appropriate key will be transmitted.

Figure 2 **Keycode drawing**



Notes: 1. 'off/on' switch position keycodes alternate i.e. toggle
2. A through to Z key positions give shift codes when caps lock is enabled

Cursor control

The cursor is controlled in shift mode, by the cursor control keys on the numeric keypad.

The ON/OFF key will toggle the cursor on and off.

Shift	↑	moves cursor up
Shift	←	moves cursor left
Shift	→	moves cursor right
Shift	↓	moves cursor down
Shift	↖	moves cursor to top left of screen

Clear screen

The keycode FF moves the cursor to the top left position and clears the screen. This code is transmitted by 'shift 9'.

Auto repeat

If a key is held down it will automatically repeat at a frequency of 8Hz after a 500ms delay following the first character transmission. See Figure 2 for keys not affected.

Flash and steady

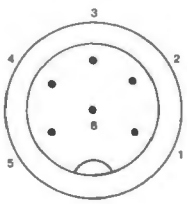
These are used in conjunction with the escape key. ESC FLASH will cause all further entries on the current line to flash. ESC STDY enables entry of steady characters after use of ESC FLASH.

Special function key combinations

Keys	Function	Keys	Function
CTRL A	SOH Start of heading	ESC A	Red characters
CTRL B	STX Start of text	ESC B	Green characters
CTRL C	ETX End of text	ESC C	Yellow characters
CTRL D	EOT End of transmission	ESC D	Blue characters
CTRL E	ENQ Enquiry	ESC E	Magenta characters
CTRL F	ACK Acknowledge	ESC F	Cyan characters
CTRL G	BEL Bell	ESC G	White characters
CTRL H	BS Backspace	ESC H	Flashing characters
CTRL I	HT Horizontal tabulation	ESC I	Steady characters
CTRL J	LF Line feed	ESC J	End editing
CTRL K	VT Vertical tabulation	ESC K	Start editing
CTRL L	FF Form feed	ESC L	Normal height characters
CTRL M	CR Carriage return	ESC M	Double height characters
CTRL N	SO Shift out	ESC Q	Red graphics
CTRL O	SI Shift in	ESC R	Green graphics
CTRL P	DLE Data link escape	ESC S	Yellow graphics
CTRL Q	DC1 Device control 1	ESC T	Blue graphics
CTRL R	DC2 Device control 2	ESC U	Magenta graphics
CTRL S	DC3 Device control 3	ESC V	Cyan graphics
CTRL T	DC4 Device control 4	ESC W	White graphics
CTRL U	NAK Negative acknowledge	ESC X	Generate concealed character
CTRL V	SYN Synchronous idle	ESC Y	Contiguous graphics
CTRL W	ETB End of transmission block	ESC Z	Separated graphics
CTRL X	CAN Cancel		
CTRL Y	EM End of medium		
CTRL Z	SUB Substitute		

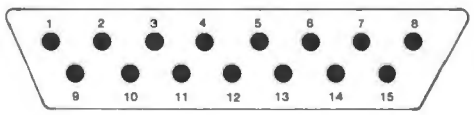
Interfacing

A. **Serial keyboard (stock number 333-467).**
The connection is made via a flying lead terminated in a 6-pin DIN plug.



Cable connector end view
1. 0V 2. +5V 5. Serial output, 75 baud.
Pins 3, 4 and 6 no connection.
Word format: 1 start bit, 7 data bits, 1 even parity bit, 1 stop bit.
Transmission rate: 75 baud.

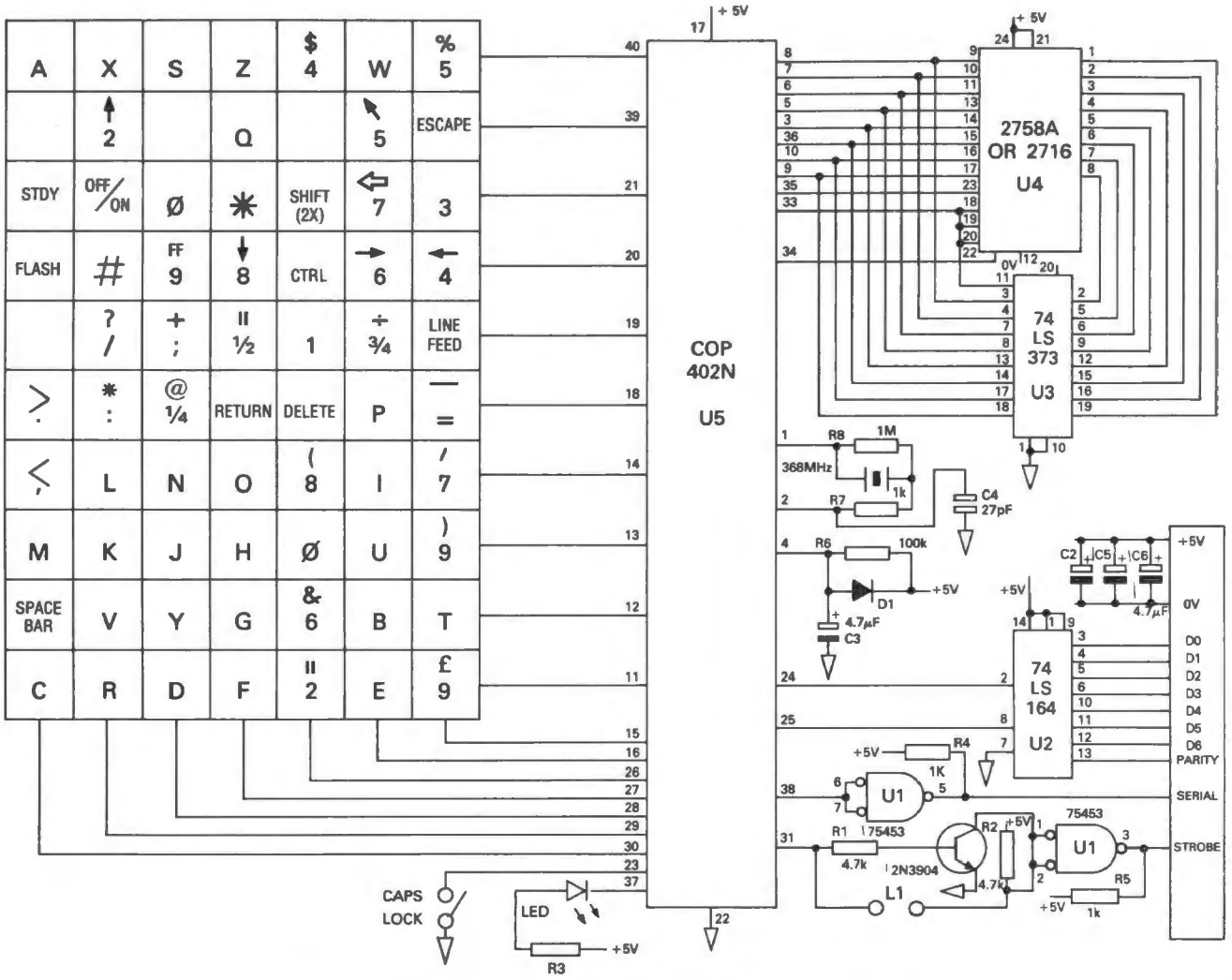
B. **Parallel keyboard (stock number 333-473).**
The connection is made via a flying lead terminated in a 15-pin D type plug (male).



Cable connector, end view. Pins 1 to 7 are data lines DØ to D6 respectively, 8. Even parity, 10. Strobe, 11. +5V, 15. 0V.
Pins 9, 12, 13 and 14 no connection.
Strobe: 100μs negative going
Data and Parity (pins 1 to 8) valid for 50ms after leading edge of strobe.

RS data

Figure 3 **Circuit diagram**



Note: Serial keyboard – pins 24 and 25 U5 not used.
Parallel keyboard – pin 38 of U5 not used.

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RS data

Alphanumeric dot matrix LCD displays

Stock number 588-500 to 588-538

Intelligent, alphanumeric, dot matrix modules with integral CMOS microprocessor and LCD display drivers. The modules utilise a 5 x 7 dot matrix format, with cursor, and are capable of displaying the full ASCII character set plus up to 8 additional user programmable custom symbols. The displays are virtually burden free to the host processor. Internal registers store up to 80 characters and all update and refresh is internal. Software is greatly eased by powerful, single step, instructions which eliminate many lines of conventional coding.

Applications

- ▲ Telecommunications
- ▲ Medical instruments
- ▲ Hand-held terminals
- ▲ Electronic typewriters
- ▲ Point of sale terminals
- ▲ Test instruments
- ▲ Light meters
- ▲ Chemical analysers
- ▲ Word processors
- ▲ Navigation equipment

Features

- 5V, 2mA, single power supply
- High contrast, dot matrix characters for good readability
- Wide adjustable viewing angle
- Compact and lightweight
- TTL and 5V CMOS compatible
- Direct interface to any 4 or 8-bit data bus
- Powerful instructions save lines of coding
- Display 'Blank', 'Flash' or 'Flash Limited Area'
- Full ASCII compatibility
- 192-Character generator ROM (96 Alphanumerics/Symbols, 64 Kata kana, 32 Euro/Greek/Symbols)
- 8-User programmable RAM locations for custom symbols
- 80-Character memory allows easy Scrolling or general purpose storage
- Cursor 'Flash', or off
- Automatic display shift – simple command structure
- Scrolls left or right or alternates complete lines.

Figure 1 **Module block diagrams**

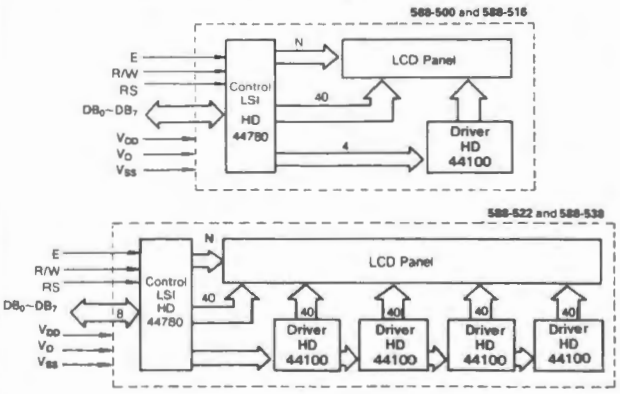

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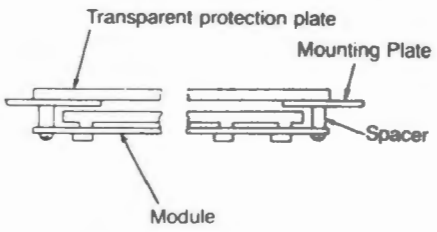
Figure 2 **Typical module mounting**



Absolute maximum ratings

Item	Symbol	Min.	Max.
Logic circuit power supply voltage*	V_{DD}–V_{SS}	0V	7.0V
LC driver circuit supply voltage†	V_{DD}–V_O	0V	13.5V
Input voltage	V_I	V_{SS}	V_{DD}
Operating temperature		0°C	50°C
Storage temperature		–20°C	70°C

* Reverse polarity connection to the logic circuit will cause irreparable damage.

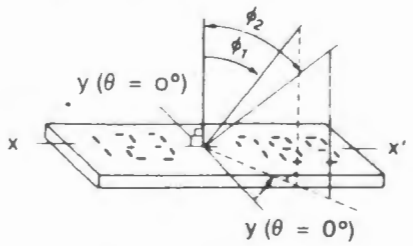
† Instantaneous value.

Electro-optical characteristics V_{DD} = 5.0 ±0.25V, Ta = 25°C

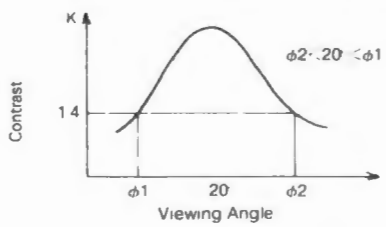
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input 'High' Voltage	V_{IH}		2.2	–	V_{DD}	V
High 'Low' Voltage	V_{IL}		–0.3	–	0.6	V
Output 'High' Voltage	V_{OH}	$-I_{OH}$ = 0.205mA	2.4	–	–	V
Output 'Low' Voltage	V_{OL}	I_{OL} = 1.6mA	–	–	0.4	V
Power Supply Current	I_{DD}	V_{DD} = 5.0V	–	0.5	2.0	mA
1 Line Module Drive Voltage (1/8 Duty) 5 x 7 Font + Cursor	V_{DD}-V_O	T_a = 0°C	4.2	4.3	4.4	V
		T_a = 25°C	3.8	3.9	4.0	V
		T_a = 50°C	3.4	3.5	3.6	V
2 Line Module Drive Voltage (1/16 Duty) 5 x 7 Font + Cursor	V_{DD}-V_O	T_a = 0°C	4.8	4.9	5.0	V
		T_a = 25°C	4.3	4.4	4.5	V
		T_a = 50°C	3.8	3.9	4.0	V
Viewing Angle	ø1 -ø2	K= 1.4	20	–	–	deg.
Contrast Ratio	K	ø =20°, 0 = 0°	3	–	–	
Rise Time	tr	ø = 20°	–	150	250	ms
Fall Time	tr	ø = 20°	–	150	250	ms

Figure 3 **Definition**

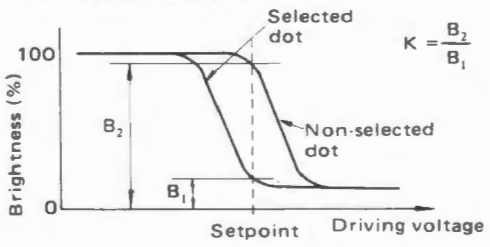
A) ANGLE ø AND θ



B) VIEWING ANGLE ø AND θ2



C) CONTRAST 'K'



D) OPTICAL RESPONSE

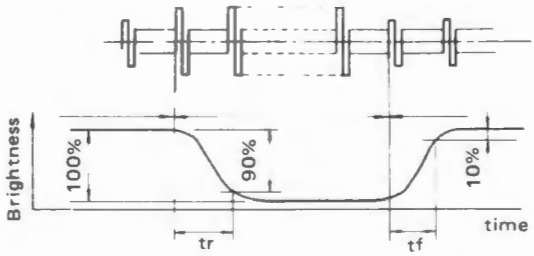
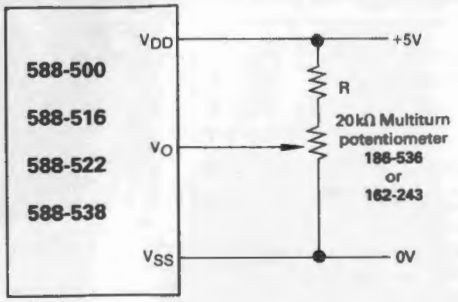
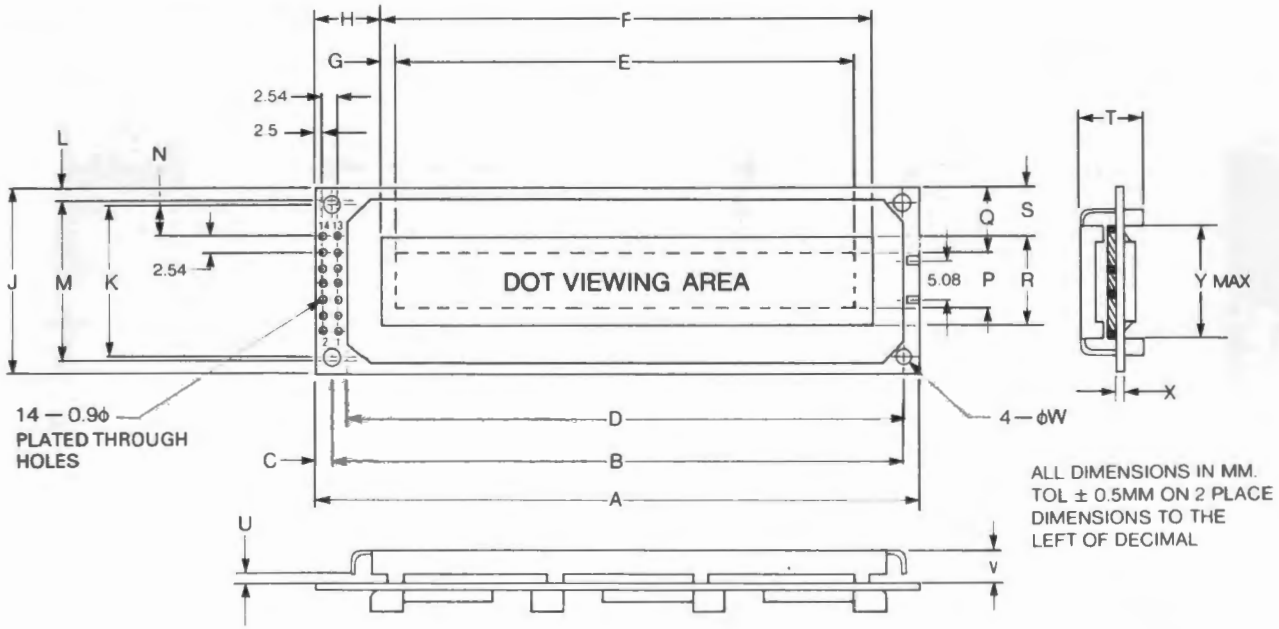


Figure 4 **Power supply**



Note: $V_O \approx +0.7V$.
A padding resistor R may be required to limit voltage swing at V_O.

Figure 5 **Mechanical dimensions**

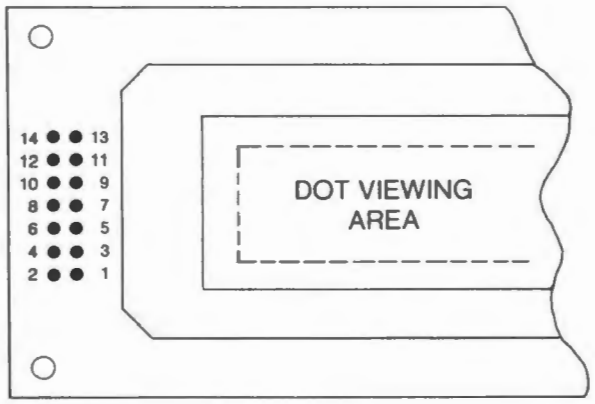


* FRAME DIMENSION

Stock No.	A	B	C	D	E	F	G	H	J	K	L	*M
588-500	85.0	80.0	2.5	73.5	59.4	63.5	2.05	13.25	36.0	31.0	2.5	28.5
588-516	85.0	80.0	2.5	73.5	59.4	63.5	2.05	13.25	36.0	31.0	2.5	28.5
588-522	182.0	175.0	3.5	163.5	149.4	154.5	2.85	16.30	33.5	26.5	3.5	32.5
588-538	182.0	175.0	3.5	163.5	149.4	154.5	2.85	16.30	33.5	26.5	3.5	32.5

	N	P	Q	R	S	T	U	V	W	X	Y	Weight(g)
588-500	7.88	8.7	13.65	15.8	10.1	9.3	1.4	4.7	2.5	1.6	20.0	28
588-516	7.88	12.3	11.85	15.8	10.1	9.3	1.4	4.7	2.5	1.6	20.0	28
588-522	7.00	8.7	13.25	15.8	8.5	9.3	1.4	4.7	3.5	1.6	22.5	66
588-538	7.00	12.3	10.60	15.8	8.5	9.3	1.4	4.7	3.5	1.6	22.5	66

Figure 6 **Pin connections**



(Top View)

PIN NO.	SIGNAL	LEVEL
1	V_{SS}	GROUND
2	V_{DD}	+ 5.0V
3	V_O	≈ + 0.7V
4	RS	L = INST, H = CHAR
5	R/W	L = W, H = R
6	E	⎍ LATCH ON FALL
7	DB0	POSITIVE LOGIC
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	

Table 1 **Pin functions**

Pin Name	I/O	Function
V_{SS}		Ground; 0V
V_{DD}		+ 5V
V_O		Power supply for LC driving
RS	I	Signal to select registers '0': Instruction register (for write) Busy flag; address counter (for read) '1': Data register (for read and write)
RW	I	Signal to select read (R) and write (W) '0': write MPU → LCD Module '1': read MPU ← LCD Module
E	I	Operation start signal for data read or write
DB0 ~ DB3	I/O	Data bus of lower order 4 lines having bidirectional tri-state. Used for data transfer between the MPU and the module. These four are not used during 4-bit operation.
DB4 ~ DB7	I/O	Data bus of higher order 4 lines having bidirectional tri-state. Used for data transfer between the MPU and the module. DB7 can be used as a BUSY flag.

NOTE: In order that the module can accommodate both 4-bit and 8-bit MPUs, the data may be sent in either a repeated 4-bit or a single 8-bit operation

(1) When the module is in the 4-bit mode, DB4 ~ DB7 are used for data transfer, DB0 ~ DB3 are not used. A complete data transfer consists of loading the higher order bits of the 8-bit instruction first, followed by the low order bits. The second transfer completes the sequence.

(2) When the interface data is 8 bits wide, data is transferred using all 8 data lines of DB0 ~ DB7.

Font table


UPPER 4 BIT HEXADECIMAL
LOWER 4 BIT HEXADECIMAL
Higher 4 bit
Lower 4 bit
0 2 3 4 5 6 7 A B C D E F
0000 0010 0011 0100 0101 0110 0111 1010 1011 1100 1101 1110 1111
0 xxxx0000 CG RAM (1)
1 xxxx0001 (2)
2 xxxx0010 (3)
3 xxxx0011 (4)
4 xxxx0100 (5)
5 xxxx0101 (6)
6 xxxx0110 (7)
7 xxxx0111 (8)
8 xxxx1000 (1)
9 xxxx1001 (2)
A xxxx1010 (3)
B xxxx1011 (4)
C xxxx1100 (5)
D xxxx1101 (6)
E xxxx1110 (7)
F xxxx1111 (8)

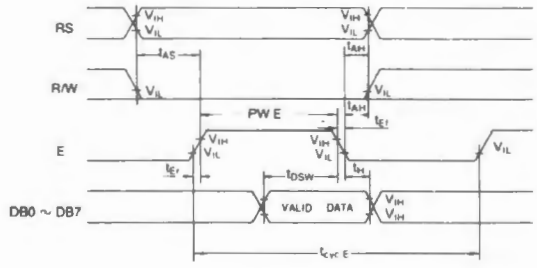
Instructions

Instruction	Code										Description	Execution Time (when f_{cp} or f_{osc} is 250KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears the display and returns the cursor to the home position (Address 0)	82 μs ~ 1.64ms
Return Home (cursor)	0	0	0	0	0	0	0	0	1	X	Returns the cursor to the home position (Address 0). A shifted display will also be restored to its original position. DD RAM contents remain unchanged.	40 μs ~ 1.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor direction and enables display shift. These operations are performed during data write and read.	40 μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Selects display ON/OFF (D), cursor ON/OFF (C), and flash of character at cursor position character (B).	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Moves the cursor and shifts the display without changing DD RM contents.	40 μs
Function Set	0	0	0	0	1	DL	N	F	X	X	Sets interface data mode (DL), number of display lines (L), and character font (F).	40 μs
Set CG RAM Address	0	0	0	1	A_{CG}						Selects CG RAM address. Following this instruction all data is stored in/read from CG RAM.	40 μs
Set DD RAM Address	0	0	1	A_{DD}							Selects DD RAM address. Following this instruction all data is stored in/read from DD RAM.	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents.	40 μs
Write Data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs
Read Data to CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs
	I/D = 1: Increment S = 1: Enable S/G = 1: Display shift R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bit mode N = 1: 2 lines F = 1: Not used BF = 1: Display process or busy BF = 0: Ready for next instruction						I/D = 0: Decrement S/C = 0: Cursor move DL = 0: 4 bit mode N = 0: 1 line F = 0: 5 x 7 dots				DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address (Corresponds to cursor address.) AC: Address counter, both DD and CG RAM addresses.	Execution time changes when frequency changes. (Example) When f_{cp} or f_{OSC} is 270kHz: $40\mu s \times \frac{250}{270} = 37\mu s$

X = Don't care

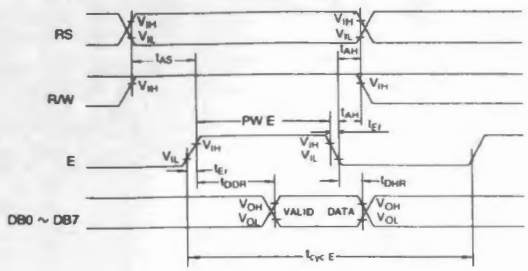
Timing characteristics

Figure 7 **Write operation**



Item	Symbol	Min.	Typ.	Max.	Unit
Enable Cycle Time	$t_{cyc\,E}$	1.0	–	–	μs
Enable Pulse Width	PW E	450	–	–	ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	–	25	ns
Address Set-up Time	t_{AS}	140	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Data Set-up Time	t_{DSW}	195	–	–	ns
Data Hold Time	t_H	10	–	–	ns

Figure 8 **Read operation**

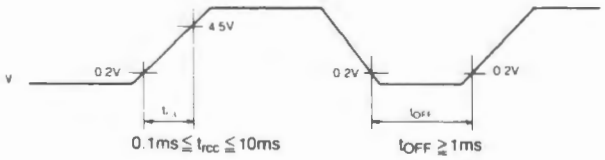


Item	Symbol	Min.	Typ.	Max.	Unit
Enable Cycle Time	$t_{cyc\,E}$	1.0	–	–	μs
Enable Pulse Width	PW E	450	–	–	ns
Enable Rise/Fall Time	t_{Er}, t_{Ef}	–	–	25	ns
Address Set-up Time	t_{AS}	140	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Data Delay Time	t_{DDR}	–	–	320	ns
Data Hold Time	t_{DHR}	20	–	–	ns

Reset function

The module has internal circuitry to initialise itself automatically upon the application of power. The reset sequence followed is:

1) Clear display
   The busy flag is set (BF = 1) during initialisation (approx. 15ms).
2) Function set.....DL=1 : 8 bit wide interface mode.
   N=0 : 1-line display
   F=0 : 5 x 7 dot character font
3) Display ON/OFF control....D=0 : Display OFF
   C=0 : Cursor OFF
   B=0 : Flash OFF
4) Entry mode set .....I/0=1 : +1 (increment)
   S=0 : No shift
5) DD RAM is selected
   The display module power supply must have the following timing characteristic for the internal initialisation circuitry to function correctly.



Note:
t_{OFF} must be observed, particularly in the case of momentary power interruption, to ensure orderly initialisation of the module. If this restriction is not adhered to, the interface mode will be undefined and must first be set up to allow further initialisation commands to be recognised. The function set instruction, sent twice, will always select the 8-bit wide interface mode.

Function set:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	X	X	X
0	0	0	0	1	1	X	X	X	X

X = Don't care

When this instruction is sent, the module enters the 8-bit data length mode without fail.

Instruction description

Outline

Only two registers of the HD44780, the Instruction Register (IR) and the Data Register (DR) can be controlled by the MPU directly. Control information is temporarily stored in these registers, prior to execution to allow interface to various types of MPUs which operate at different speeds from the HD44780 or to allow interface to peripheral control ICs. The HD44780 internal operation is determined by signals sent from the MPU, including register selection signals (RS), read/write signals (R/W) and data bus signals ($DB_0 \approx DB_7$). The table on page 6 shows the instructions and their execution times.

Details are explained in the following sections. The instructions can be divided into the following 4 types:

1) Instructions that designate the HD44780 functions such as display format, data mode, etc.
2) Instructions that give internal RAM addresses.
3) Instructions that perform data transfer with internal RAM.
4) Other utility instructions.
   In normal use, instructions of category (3), (to send display data), are used most frequently. The HD44780 internal RAM addresses are configured to be automatically incremented (or decremented) by +1 after each data write, and hence the programme overhead on the MPU is reduced. Display Shift can be selected to occur with Display Write to further reduce this load. High speed (≈50kHz) operation can be maintained by monitoring the user accessible busy flag (DB_7).

Clear Display

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	0	1

Writes ASCII space code '2Ø' (hexadecimal) into all the DD RAM addresses. The cursor returns to Address 0 (A_{dd}='8Ø') and the display, if it has been shifted, returns to the original position. In other words, the display disappears and the cursor goes to the left edge of the display (the first line if 2 lines are displayed).

Return Home (Cursor)

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	1	X

X = (Don't Care)

Returns the cursor to Address 0 (A_{DD}='8Ø') and the display, if it has been shifted, to the original position. The DD RAM contents remain unchanged.

Entry mode set

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D=1) or decrements (I/D=0) the DD RAM address by one upon writing into or reading a character code from the DD RAM. The cursor moves to the right when incremented by one. The same applies to the writing and reading of CG RAM data.

S: Shifts the entire display to either the right or the left when S is 1; to the left when I/D=1 and to the right when I/D=0. Therefore, the cursor appears static with the display moving. The display is not shifted when reading from the DD RAM or when S=0.

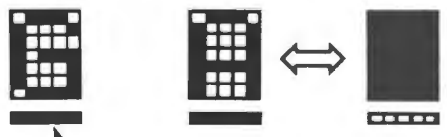
Display On/Off Control

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	1	D	C	B

D: Display is turned ON when D=1 and OFF when D=0. When display is turned off the display data remains in the DD RAM and it can be recalled at any time by setting D=1.

C: The cursor is displayed when C=1 and not displayed when C=0. With the cursor disabled all internal operations (eg I/D) function normally during a display data write. The cursor is displayed using 5 dots in the 8th character row.

B: The cursor character flashes at approx. 2.5Hz when B=1. The cursor and flash enable can be set simultaneously.



Cursor

Alternating Display

(a) Cursor Display Example

(b) Flashing Display Example

Cursor or Shift Display

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	X	X

X = (Don't Care)

Shifts the cursor position or display to the right or the left without writing or reading the display data. This function is used for correction or search of the display.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. (The cursor follows the display shift.)
1	1	Shifts the entire display to the right. (The cursor follows the display shift.)

Function set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	1	DL	N	F	X	X

X = (Don't Care)

DL: Sets interface data mode. Data is sent or received in 8 bit (using DB_7~DB_0) when DL=1 or 4 bit words (using DB_7~DB_4) when DL=0. When the 4 bit mode is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

N	F	No. of Display Lines	Character Font	Duty Cycle
0	0	1	5 x 7 dots	1/8
1	X	2	5 x 7 dots	1/16

X = (Don't Care)

Set CG RAM address

	RS	R/W	DB_7							DB_0
Code	0	0	0	1	A	A	A	A	A	A

← Higher Order Bits — Lower Order Bits →

Places the binary number AAAAAA into the address counter (AC) and refers all following data transfers to CG RAM.

Set DD RAM address

	RS	R/W	DB_7							DB_0
Code	0	0	1	A	A	A	A	A	A	A

← Higher Order Bits — Lower Order Bits →

Places the binary number AAA ↔ AAAA into the address counter (AC) and refers all following data transfers to DD RAM. For a one line display (N=0) valid addresses range from 'ØØ' → '4F' (hexadecimal). For a two line display (N=2) the first line is addressed from 'ØØ' → '27' and the second from '4Ø' → '67' (hexadecimal).

Read Busy Flag and address

	RS	R/W	DB_7							DB_0
Code	0	1	BF	A	A	A	A	A	A	A

Higher Order Bits ← → Lower Order Bits

Reads Busy Flag (BF) and current Address Counter (AC) contents. When BF=1, an internal operation is in progress and the next instruction is not accepted until BF is cleared to '0'. Check the BF status before attempting a write operation. At the same time, the value of the address counter is read as a binary number AAAAAA. The address counter is used by both CG and DD RAM and its value is determined by previous instructions. Address contents are those of the CG RAM or DD RAM last used.

Write Data to CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	0	D	D	D	D	D	D	D	D

Higher Order Bits ← → Lower Order Bits

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM. The destination of the data is defined by the last 'set RAM address' instruction. After a Write Data instruction, an address adjust or display shift occurs as defined by Entry Mode.

Read Data from CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D

Higher Order Bits ← → Lower Order Bits

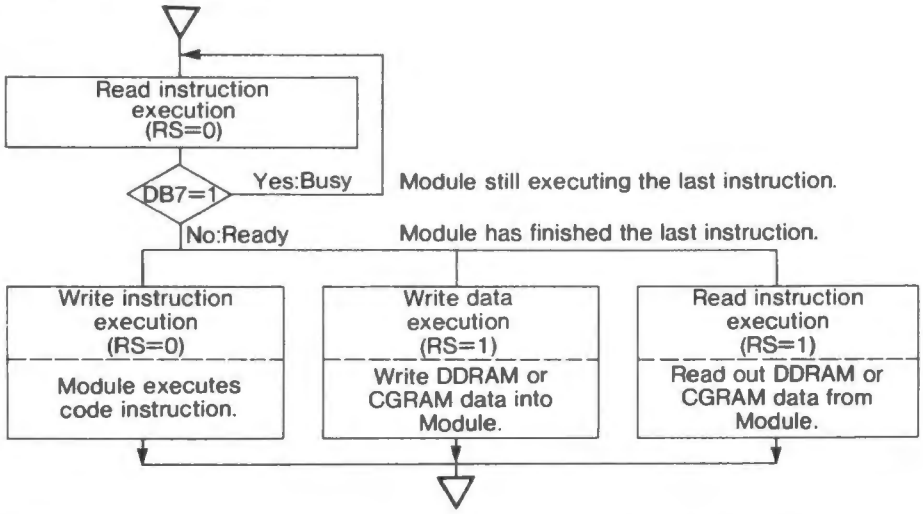
Reads binary 8 bit data DDDDDDDD from the CG or the DD RAM. The source of the data is defined by the last 'set RAM address' instruction. If a Read Data is attempted before execution of a set RAM address instruction then the data returned to the MPU is invalid. After a Read Data instruction, an address adjust occurs as defined by Entry Mode but the display shift is not actioned.

Table 2 **Relation between CG RAM Addresses, Character Codes (DD RAM) and Character Patterns (CG RAM Data)**

Character Codes (DD RAM Data) 7 6 5 4 3 2 1 0 (◄ Higher Order Bits / Lower Order Bits ►)	CG RAM Address 5 4 3 | 2 1 0	Character Patterns (CG RAM Data) 7 6 5 | 4 3 2 1 0	
0 0 0 0 X 0 0 0	0 0 0 | 0 0 0	X X X | 1 1 1 1 1 0	Character Pattern Example (1)
	0 0 0 | 0 0 1	X X X | 1 0 0 0 1 0	
	0 0 0 | 0 1 0	X X X | 1 0 0 0 1 0	
	0 0 0 | 0 1 1	X X X | 1 0 0 0 1 0	
	0 0 0 | 1 0 0	X X X | 1 0 1 1 0 0	
	0 0 0 | 1 0 1	X X X | 1 0 0 0 1 0	
	0 0 0 | 1 1 0	X X X | 1 0 0 0 1 0	Cursor Position
	0 0 0 | 1 1 1	X X X | 0 0 0 0 0 0	
0 0 0 0 X 0 0 1	0 0 1 | 0 0 0	X X X | 1 0 0 0 1 0	Character Pattern Example (2)
	0 0 1 | 0 0 1	X X X | 0 1 0 1 0 0	
	0 0 1 | 0 1 0	X X X | 1 1 1 1 1 0	
	0 0 1 | 0 1 1	X X X | 0 0 1 0 0 0	
	0 0 1 | 1 0 0	X X X | 1 1 1 1 1 0	
	0 0 1 | 1 0 1	X X X | 0 0 1 0 0 0	
	0 0 1 | 1 1 0	X X X | 0 0 1 0 0 0	
	0 0 1 | 1 1 1	X X X | 0 0 0 0 0 0	
	0 0 0 | 0 0 0	X X X	
	0 0 0 | 0 0 1	X X X	
0 0 0 0 X 1 1 1	1 1 1 | 1 0 0	X X X	X Don't Care
	1 1 1 | 1 0 1	X X X	
	1 1 1 | 1 1 0	X X X	
	1 1 1 | 1 1 1	X X X	

Note
1. Character code bits 0~2 correspond to CG RAM address bits 3~5.
2. CG RAM address bits 0~2 define character pattern row address. The 8th row is the cursor position and the display is logically OR ed with the cursor.
3. Character pattern column positions within a row correspond to CG RAM data bits 0~4, as shown in the figure (Bit 4 being at the left end). Since CG RAM data bits 5~7 are not used for display, they can be used as general data RAM.
4. CG RAM character patterns are selected when character code bits 4~7 are all '0'. However, since character code bit 3 is a "don't care" bit, character pattern example 1, for instance, is selected by character code 'ØØ' (hexadecimal) or 'Ø8' (hexadecimal).
5. '1' for CG RAM data corresponds to pixel displayed (ON) and '0' pixel absent (OFF).

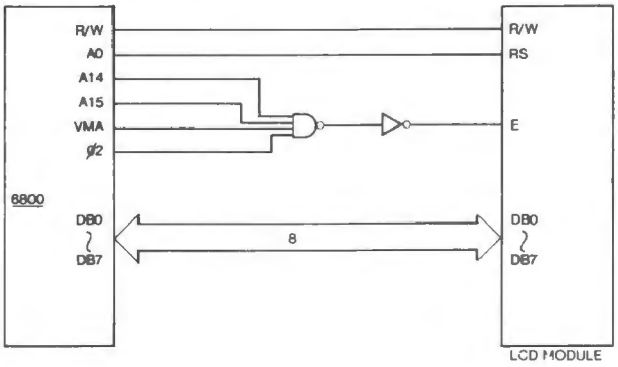
Interfacing with microprocessors



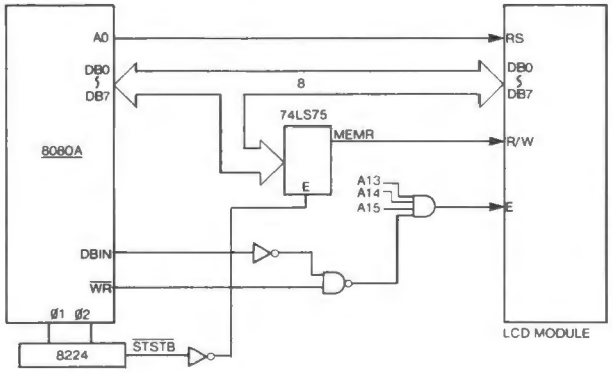
Note • In this flowchart, Read and Write instructions correspond with external RAM reference instruction or I/O instruction.

• By providing sufficient instruction execution time, it may be unnecessary to monitor the 'Busy Flag.'

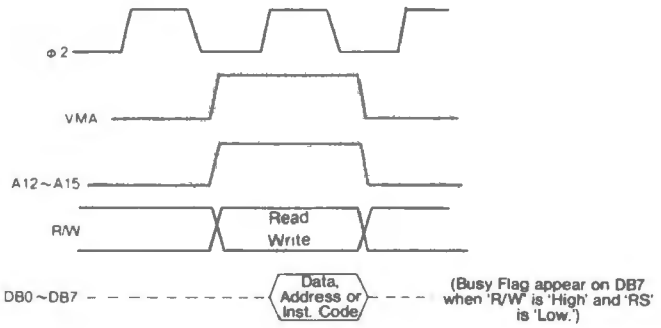
Interface with 6800



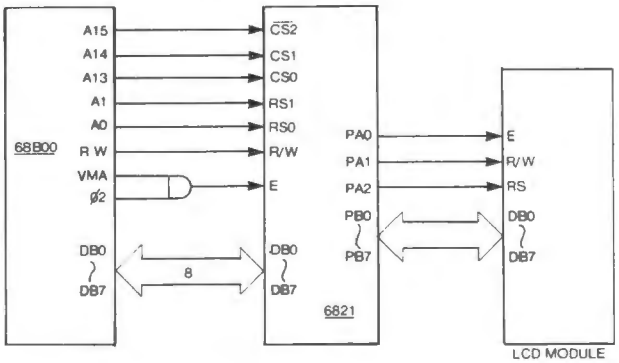
Interface with 8080A



TIMING CHART



Interface with 68B00



- **6800**
- LCD module is treated as an I/O or RAM device.
- A_0 is connected to RS and hence its level selects either the instruction register or the data register.
- The addresses of the module (as I/O) in the address map of the 6800 are:

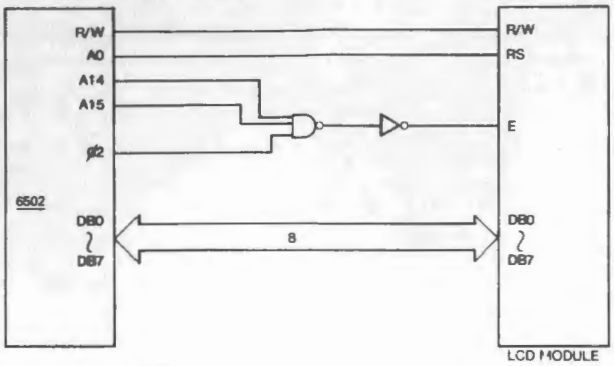
Write function	# 'FXX0' (R/W = 0)
Write CGRAM/DDRAM data	# 'FXX1' (R/W = 0)
Read Busy flag/address	# 'FXX0' (R/W = 1)
Read CGRAM/DDRAM data	# 'FXX1' (R/W = 1)

Note: the lead bit 'F' may be 'C', 'D', or 'E', X = Don't Care.

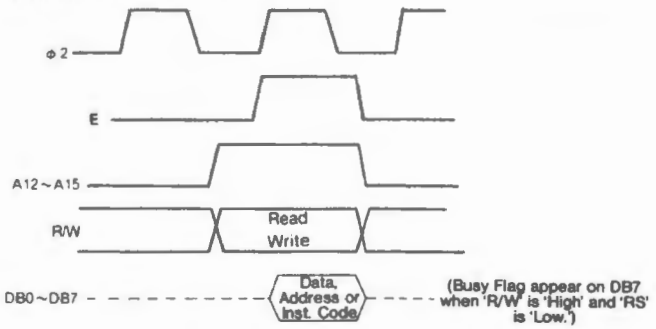
- **68B00**

The 68B00 is a high speed version of the 6800. The 02 signal is too narrow to drive the LCD module correctly. A simple interface uses the 6821 PIA between the CPU and module. This, in conjunction with appropriate user provided software, provides an E pulse of adequate width.

Interface with 6502



TIMING CHART

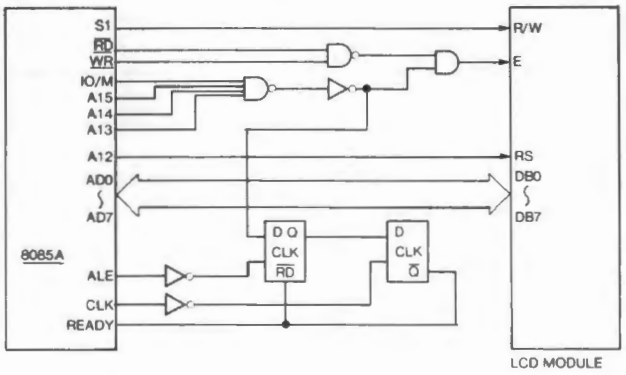


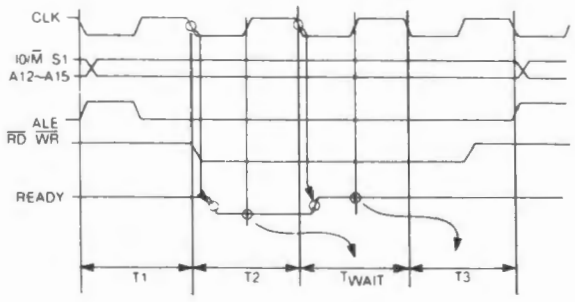
- 6502
- LCD module is treated as a RAM device.
- Ao is connected to RS and hence its level selects either the instruction register or the data register.
- The Addresses of the module in the address map of the 6502 are:

Write function	# FXXØ' (R/W = 0)
Write CGRAM/DDRAM data	# FXX1' (R/W = 0)
Read Busy flag/address	# FXXØ' (R/W = 1)
Read CGRAM/DDRAM data	# FXX1' (R/W = 1)

Note: the lead bit 'F' may be 'C', 'D' or 'E'.

Interface with 8085A



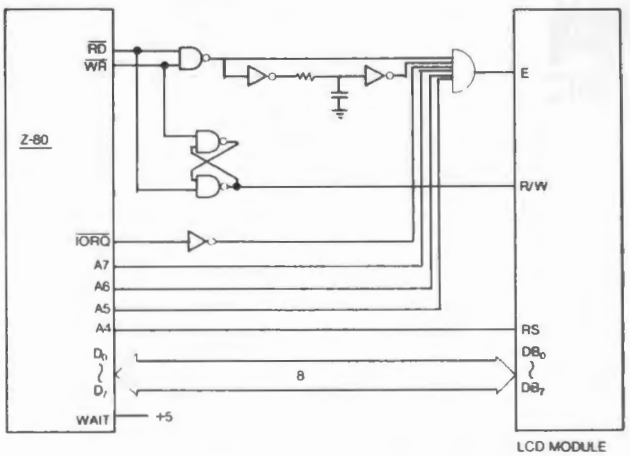


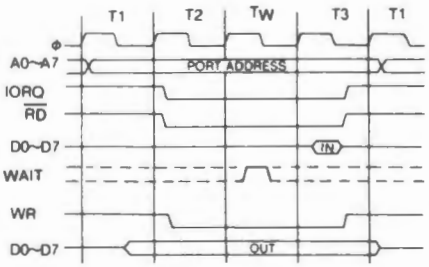
- LCD module is treated as I/O or RAM device.
- The E pulse to the module should be 450nsec min. The RD and WR pulses of the 8085A are specified as 400nsec min and hence need to be lengthened by a slower clock or by the addition of Wait states.
- The addresses of the module as I/O device in the address area of the 8085A are:

Write function	# 'EX' (R/W = 0)
Write CGRAM/DDRAM data	# 'FX' (R/W = 0)
Read busy flag/address	# 'EX' (R/W = 1)
Read CGRAM/DDRAM data	# 'FX' (R/W = 1)

X = Don't Care

Interface with Z-80



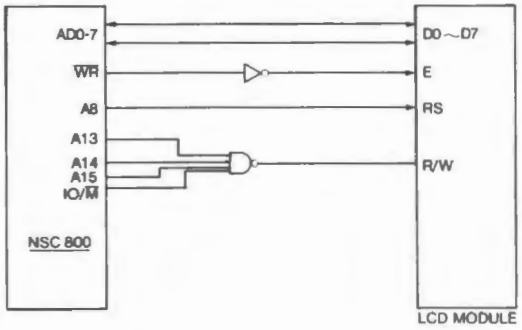


- The module is treated as an I/O device.
- When accessing I/O, a wait state is inserted automatically by the Z80 and the OR of RD and WR can be at least 450nsec and hence could drive the E input directly. R and C need to be selected to ensure the setup time restriction is met.
- If the module is treated as RAM, the user must insert a wait state.
- The addresses of the module as I/O device in the address area of the Z-80 are:

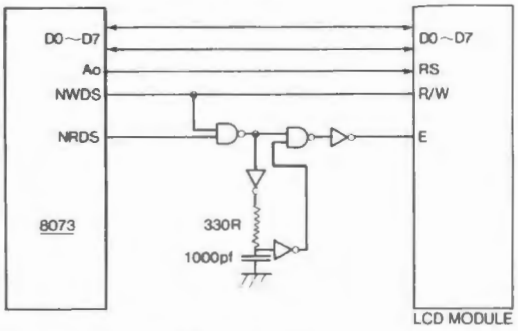
Write fuction	# 'EX' (R/W = 0)
Write CGRAM/DDRAM data	# 'FX' (R/W = 0)
Read busy flag/address	# 'EX' (R/W = 1)
Read CGRA/DDRAM data	# 'FX' (R/W = 1)

X = Don't Care

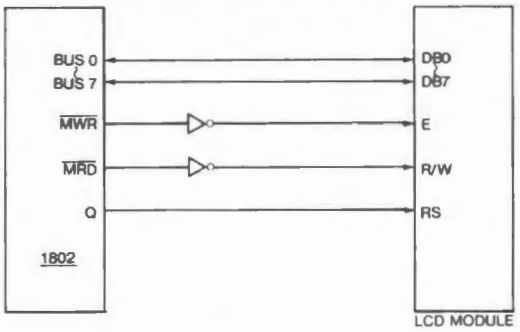
Interface with NSC 800 CMOS Micro



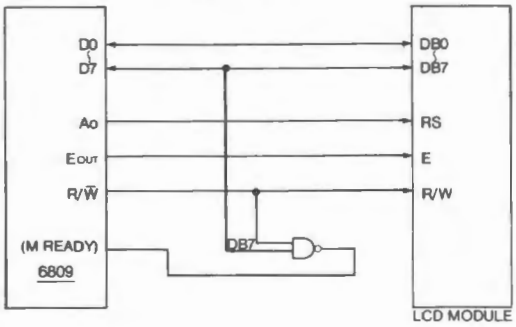
Interface with NSC 8073 Tiny Basic Microinterpreter



Interface with HUGHES/RCA 1802 CMOS Micro



Interface with MOTOROLA HIGH PERFORMANCE 6809



Handling precautions

1. The polarisers in the panel are easily scratched. Do not touch, press or rub the display panel with hard tools such as tweezers.
2. Do not use organic solvents to clean the display panel as they can cause deterioration of the polarizers
3. Do not remove the LCD panel from the main unit.
4. Never use or store the LCD module under conditions of abnormally high temperature and humidity.
5. **Static electrical charges can damage CMOS/LSI circuitry. Observe normal antistatic handling procedures.**

Operational notes

1. Never connect or disconnect the LCD Module from the main system whilst power is applied.
2. If the operating temperature falls below the temperature limit, the flashing speed of the display will decrease. If the temperature exceeds the prescribed limit, the display will turn black. Operation returns to normal when the temperature returns to within the normal limits.
3. Adjust V_O for optimum display contrast. (0.2-0.7V).

Operation of the RS alphanumeric dot matrix modules

Common problems

1. Transmitting too fast to the display:
   a) upon initialisation allow 15ms before sending data,
   b) after transmitting hex Ø1 or Ø2 allow 1.6ms,
   c) after all other data allow at least 40μs.
2. Not generating a positive going enable pulse at least 700ns wide.
3. Data, RS and R/W signals are not stable for at least 500ns before, and after, the falling edge of the enable pulse.
4. V_O pin voltage level incorrect – should be 0.7 volt approximately.
5. Display misconnection: crossed, open or incorrectly terminated cable.
6. LCD input assumed to be configured as an IC.
7. Failure to properly initialize the display.
8. Signal levels too low at the display. Ensure that at least 2.4V (H) is present.
9. Data bus contention. More than one external bus device selected.
10. Not all data bus components have TTL type outputs causing conflict with the on board databus.

Troubleshooting

a) Display appears blank: check +5V and gnd at display: check 4, 5, 6 and 7 above.
b) Displayed characters enter unreliably or at random: check 1, 3, and 9 above.
c) Same symptoms as (b) but system has multiple components tied to the data bus: check 8, 9, 10 above.

Bus connections

The data bus is a 'pseudo' tri-state. There is no means to deselect the display microprocessor. In the absence of an external TTL output device the display will 'pull' the data bus up to +5V. Each bit of the data bus can source up to 0.2mA at a Voh of 2.4V.

The display can be directly connected to a shared data bus if each bus accessing component can legitimately sink 1.5mA with its output low. In this manner the selected device will dominate and the bus operation will be correct. This current sinking specification is standard with TTL-type bus output.

Some all-CMOS systems may not have an adequate 'pull-down' capability. In this instance a tri-state buffer should be used between the system data bus and the display. This buffer would then be selected to access the display.

A similar, PMOS type source is used on the E, RS and R/W lines but as these signals are not generally 'bussed', the effect should not cause any difficulty.

Display operation

The display area is a 16 or 40 character width 'window' on a continuous 80 character RAM. The window displays the first 16 or 40 characters of the RAM depending on the module type. The shift instruction permits the display window to move across the RAM. At 1 to 3Hz, shifts cause the display to scroll and higher speeds give the appearance of the message to be overwritten. During a shift, only the window position alters, not the display memory. The RAM addresses range from 8Ø to CF (hexadecimal) with 8Ø being the origin (home).

External electronics communicate with the display using the data bus and only 3 control lines, RS, R/W and E. A data transfer is only required when the external CPU needs to update or read the display and hence only minimal demands are placed on the external system.

RAM and ROM integration

Most applications will employ ROM and RAM in combination. The ROM will usually contain the display initializing codes, fixed format messages, and addressing instructions. The RAM will contain 'live' data which may change. In a CPU system memory devices will normally be 'selected' to access the data bus. Alternatively, dedicated, hardware only, designs can employ counters which 'steer' the bus control between ROM and RAM. Data selectors may also be employed between memory data lines and the display. In either case bus contention must be avoided. Set-up and hold times must be maintained by all components which may eventually 'talk' to the LCD display.

Reading the display

Reading the display consists of monitoring the 'busy flag' and examining the contents of any location within the display data RAM. The busy flag is first read to determine the earliest time that the display module can accept new instructions. The data bus is then read to recover the required information, verify its correctness, or determine any need for a display update. This feature may eliminate the need for external RAM, as single line displays have 40 to 64 locations not displayed which can be used as general purpose RAM.

The busy flag is read by setting RS = R/W = 1 and pulling the enable line high. The flag appears on D7 and is active high. Any write attempted to the module before the Busy Flag has been cleared to a Low state may be ignored or corrupted with the possibility of error.

The display data is read by first executing a display data address set instruction (RS = R/W = 0), and then by setting RS = R/W = 1. The data bus will contain the valid data on the trailing edge of the enable pulse. The display data address is automatically incremented to allow consecutive 'reads' to read a data block easily.

Sending Character Strings

Messages may be shown in several ways. Most applications will require a new message to replace an existing one.

Each message to be displayed should be preceded with a 'Clear Display' instruction (Ø1 hexadecimal). Following the 1.6ms set up delay, the message can be input. After the last character has been entered, the display is then 'idled' by either preventing further enable pulses, setting RS = 1 or by sending a code which has no effect, ØE (hexadecimal) for instance.

Alternatively, multiple messages may be stored in the Display RAM in one data transfer. Rapid shift codes can be be used to rotate each new message into the window. To ensure that extraneous characters do not appear in the window when this mode is used, surround each message with an appropriate number of blanks.

Viewing angle control

RS LCD modules are best viewed from slightly below the 'Head-on' viewing angle and hence are ideally suited to keyboard/display units where an angled display enclosure is inconvenient. Single line displays have an optimum contrast ratio about 20 degrees off the perpendicular. Two line versions shift the visual cone about 15 degrees further.

Pin 3 of the module, V_O, allows individual viewers to optimize the display contrast to their particular taste and position and it should be connected to a variable voltage of 0.2 to 0.7V.

Levels higher than these shift the viewing angle so far that the display may be unreadable. There is no benefit in returning the voltage control to a negative potential.

The best technique in maximising contrast is to adjust the contrast control with some characters on display. Turn the control just to the point where undesired dots (those not part of a display character) become invisible. Note: this does not produce the darkest dot. Adjusting for darkest dots overemphasizes the undesired dots resulting in loss of contrast ratio.

Display initialisation

It is always recommended to follow an initialisation routine before using the display to ensure that the display processor has correctly formatted the display window and that it can correctly interpret further instructions.

A suggested sequence to set up an automatically incremented display with steady line cursor follows:

RS = R/W = 0.
8 bit, 1 line, 5 x 7
  3Ø, 2Ø, Ø6, ØE, Ø1
8 bit, 2 lines: 5 x 7 only
  38, 38, Ø6, ØE, Ø1

It is possible to write to just one line of a two line display. Using the '3Ø' instruction will improve the contrast by eliminating line 2.

Four bit machines may also incorporate the display module. Initialisation is critical and this format should be closely followed. As 4 bit operation requires that data be sent twice over the D4-D7 bus, memory requirements are doubled. An advantage is the ability to store all 4 data bits, RS, and R/W in a standard 8 bit wide memory. The 8 bit data bus mode will require at least 9 bits of memory. (Assuming R/W is held low.)

4 bit, 1 line, 5 x 7

2, Ø, 2, Ø, Ø, 6, Ø, E, Ø, 1

* (The single terminating 1 is crucial).

For 2 lines change the repeated 2Ø code to repeated 24 or 28. ie. 2, 4, 2, 4, Ø, 6, Ø, E, Ø, 1 etc.

Key operational codes

These are key operational codes which are decoded by the Instruction Register. As these codes are commands they are sent with RS = R/W = 0.

Description	Code
Clear display	Ø1
Home display	Ø2
Direction of next character entry:	
Left	Ø4
Right	Ø6
Display shift with data entry:	
Left	Ø7
Right	Ø5
Cursor:	
On	ØE
Off	ØC
Flash	ØD
Shift left	1Ø
Shift right	14
Display control:	
On	ØE
Off	ØA
Display shift, no data entry:	
Left	18
Right	1C
Display data addresses:	
Home position	8Ø
Rightmost, top	8F(16), A7 (40 char. display)
Linefeed and C.R.	CØ
To 2nd line	
Rightmost, bottom	CF(16), E7(40)

Programming CG RAM

The character generator (CG) RAM allows 8 custom 5 x 8 characters. Once programmed, the newly created symbols are accessed exactly as if they were in ROM. As the RAM is a volatile memory power must be maintained. Alternatively the programming format may be programmed into external ROM and sent following display initialization. All dots of the character matrix may be programmed, including the cursor position, if desired.

The module's RAM is divided into 2 parts: display data and custom graphics. The CG portion of RAM is located between hex 4Ø and 7F, and is continuous. Locations 4Ø-47 hold the 1st CG character, 48-4F the 2nd, 5Ø-57 the 3rd, and 78-7F the 8th. If, during initialization, the display was set to automatically increment, then only the single address, 4Ø need be sent. Adjacent row data will automatically appear at 41, 42 etc. All 8 CG characters may therefore be programmed with the single initial address entry 4Ø and 64 data writes.

CG RAM is 8 bits wide although 5 bits fill a CG row. The leftmost dot of the CG row corresponds to D4, in the most significant nibble, with the other 4 dots in the least significant nibble (D3-DØ). DØ corresponds the rightmost dot. Thus 1F = all dots on. ØØ = all dots off, 15 (HLHLH) = 3 dots on, ØA (LHLHL) = 2 dots on. In each case, 5 bits of the 8 bit code program one row of a CG character. When all 7, or 8 rows are programmed, the CG character definition is complete. For example:

RS	R/W	Data	Display	Description
Ø	Ø	4Ø		addresses 1st row, 1st CG character
1	Ø	11	* *	result of 11, 1st row
1	Ø	ØA	* *	result of ØA, 2nd row
1	Ø	1F	*****	result of 1F, 3rd row
1	Ø	Ø4	*	result of Ø4, 4th row
1	Ø	1F	*****	result of 1F, 5th row
1	Ø	Ø4	*	result of Ø4, 6th row
1	Ø	Ø4	*	result of Ø4, 7th row
1	Ø	ØØ		result of ØØ, 8th row (cursor position)
1	Ø	15	* * *	1st row, 2nd CG character. Note: addressing not now required, hex 48 is next in the sequence.

Additional software control

Additional effects can be created by alternating certain codes, exploiting the CG RAM, or altering the system timing. For example:

Flash the display screen

Send the message to the display and then alternate the codes ØA and ØE. The period of ØA will determine the length of time the display is off. This is an effective warning condition.

Flash a selected display zone

Send the desired message noting the display address of the leading character in the zone. Send the address of the lead character and then hex 2Ø for each remaining flashing position. Wait an appropriate time and then rewrite the flashing data. Repeat. While somewhat tedious, the technique is visually effective. A dedicated subroutine could be used to achieve this function.

Scroll the display

Single op codes shift the display left, right, or together shift, and enter, new data. Codes 18, 1C, Ø7, and Ø5 are used. A single line display has an 8Ø character ram allowing the user to 'fill' the ram and then 'step' the data either left or right. Vertical scrolling, where entire 'chunks' of display screen size data are sequentially viewed, can be achieved with a reasonably simple host CPU subroutine.

Create multi-channel bar graphs

Bar graphs are relatively easy to create. The linear bar graph is an excellent trend indicator and can greatly enhance operator feedback. Up to 3 bar graphs can be simultaneously displayed. The CG RAM is programmed with double dot-thickness rows. Blank rows separate each bar, with dots filling rows 1, 2, 4, 5, 7 and 8 of each CG RAM character. 3 graphs use 7 CG RAM characters. The CG is programmed to contain all 3 bars, 3 combinations of 2 bars, and 3 single bars. The host MPU measures each input channel and outputs the appropriate CG RAM character, one at a time. The consecutive RAM characters create the bar of the graph. Single or dual channel graphs are similarly derived.

4 bit operation

Four bit operation has been discussed under 'Display Initialisation'.

The four bit data bus mode will be particularly suitable if:

a) a 4 bit MPU is in use.
b) Insufficient I/O lines are available to support an 8 bit wide bus.

c) Operation direct from an 8 bit Eprom or RAM is required. (At least 9 bits are needed if an 8 bit bus is employed).

D7-D4 are used during 4 bit data transfers. D3-DØ may float. The 8 bit hex code is sent one nibble at a time, with the most significant nibble leading.

The 4 bit data mode is particularly suitable when the module is to be driven directly from an EPROM/ counter combination, as RD and R/W can be programmed alongside the data. Care must be taken to ensure that RS is correct during each part of the instruction. An easy way to ensure that RS is correct when programming an 8 bit wide EPROM is to make D4 = RS and use 3Ø-3F (hexadecimal) for character data and 4Ø-4F (hexadecimal) for commands.

Code	Character	Command
Ø	0	@
1	1	A
2	2	B
3	3	C
4	4	D
5	5	E
6	6	F
7	7	G
8	8	H
9	9	I
A	:	J
B	;	K
C	<	L
D	=	M
E	>	N
F	?	O

RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

Logic analyser LA-160

Stock number 611-290

Introduction

The LA-160 logic analyser enables the activity of many digital signal points to be recorded simultaneously, and then examined in detail. The information is stored with respect to a 'clock' signal and the analyser records whether each signal point is 'high' or 'low' at each active edge of the clock signal. This information is stored in memory and is then available for detailed analysis via the logic analyser's display.

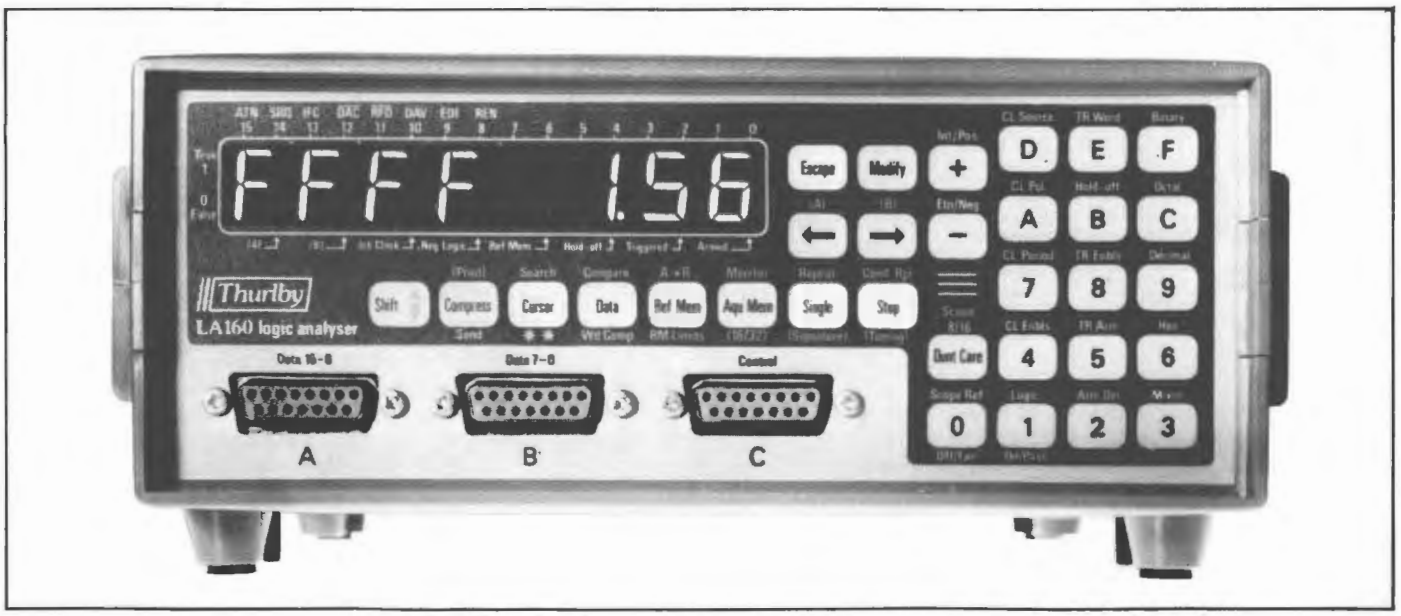
There are two basic forms of display. A 'timing diagram', where a series of successive logic levels for each channel is displayed from left to right on a screen. This is similar to the way that an oscilloscope displays information, since the trace represents the signals plotted against time. A 'state display' which is used to show the relationship between the various signals at each point in time (ie. each active edge of the clock signal). The analyser reads the logic levels for all the signals at each active clock edge and displays them as a 'word'. This word may be in binary, octal, decimal or hex formats. The display then becomes a list of successive words. This method is particularly relevant to bus organised digital systems such as microprocessor based equipment, parallel data transmission systems etc.

In order to define the section of data that is recorded, the logic analyser must be triggered. Triggering may be a simple change of level on a single line (as with triggering an oscilloscope) or it may be the simultaneous occurrence of a set of levels on a set of lines (eg. triggering on a 16 bit word from a microprocessor address bus). The LA-160 logic analyser stores data that occurred both before and after the trigger event.

There are two basic ways of recording data. These are synchronous acquisition and asynchronous acquisition. In the synchronous mode, the clock signal for the analyser is synchronised with a clock signal within the unit under test, and each piece of data is stored at a defined point; normally when the data is known to be stable. In the asynchronous mode, the clock signal for the analyser is independent of the unit under test and consequently data can be stored at any point on the data stream. If the analyser clock is set to be much faster than the data being stored, a timing diagram display will show a plot of the data against time, enabling the exact timing of level changes to be observed.

Features

- 16 data channels
- Internal or external clock, maximum speed 10MHz
- 2,000 word data acquisition memory
- Timing diagram via an oscilloscope
- Built-in single word state display
- Binary, octal, decimal, hex or mixed display formats
- 20 bit trigger word recognition
- Non-volatile 200 word reference memory
- Word search capability
- Block compare facility, pass or fail against reference memory
- Automatic repeat acquisitions, dependent on a comparison result



Data acquisition

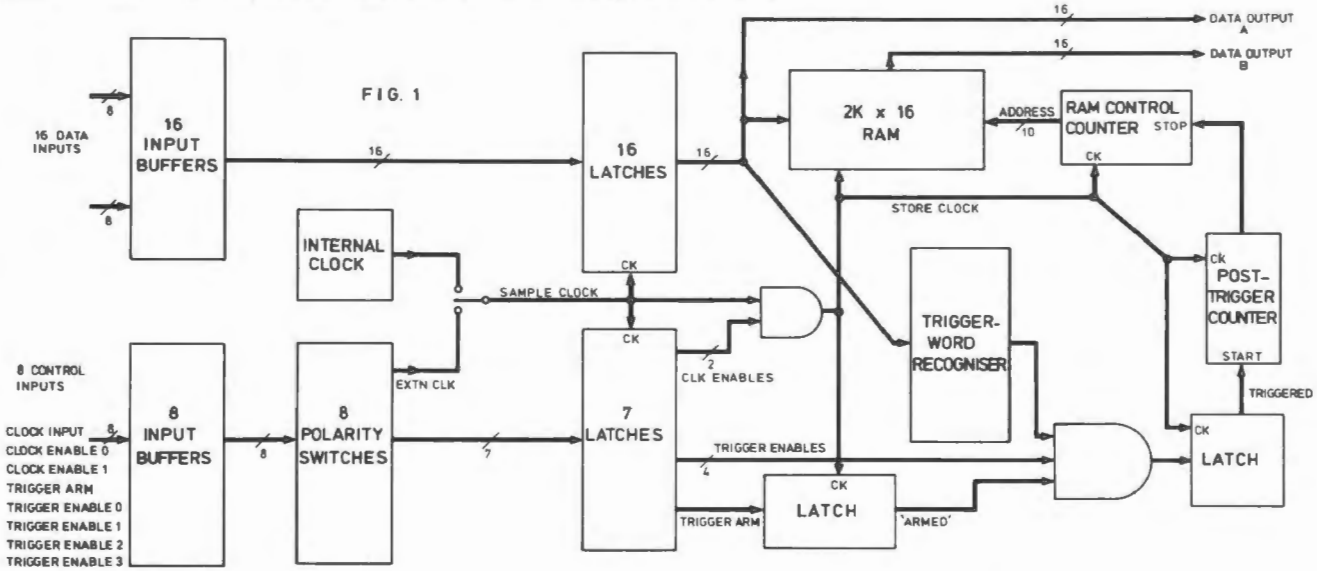
The LA-160 logic analyser operates by sampling the logic levels at its 16 data inputs in synchronism with an internally or externally generated clock signal, and storing them in a memory prior to detailed examination.

The Sample Clock may be generated within the LA-160 or generated externally and supplied via the clock input. The state of the 16 data inputs and 7 other control inputs is latched on every positive going (or negative going) transition of the sample clock. If the two Clock Enable inputs are True at this point, a further clock signal is generated known as the Store Clock. (The Clock Enable inputs can be set to be True with either a high or a low signal level.) The Store Clock causes the latched state of the sixteen data inputs to be written into memory, it also enables the trigger latch circuitry.

When the LA-160 is instructed to start a data acquisition sequence, it writes data into the memory on every cycle of the store clock, overwriting the old data with new. If the sequence is then stopped with the 'Stop' key after at least 2,047 store clock cycles have occurred, the memory will contain the data present at the 2,047 store clock cycles prior to this. Normally, however, the sequence will be terminated by a Trigger event. This causes the acquisition sequence to stop after a delay of 1,023 Store Clock cycles. The memory then contains the data present for the 1,024 Store Clock cycles before and the 1,023 Store Clock cycles after the Trigger event. This is a normal triggered acquisition.

The Trigger event is generated by the AND function of 6 signals; a Valid Trigger Word signal, 4 latched Trigger Enable inputs and the Trigger Armed signal. The Valid Trigger Word signal is generated by comparing the latched data inputs with a trigger word set via the keyboard. This can contain 'don't care' states and therefore can be made always valid if required. The Trigger Armed signal is generated by permanently latching the state of the Trigger Arm input with the Store Clock. Once latched, the Trigger Armed signal remains True for the duration of the acquisition sequence. The Trigger Enable and Trigger Arm inputs can be set to be True with either a high or a low signal level.

Figure 1 **LA-160 Acquisition section simplified block diagram.**



Data display

The single word display

The built-in 8 digit display shows the state of all 16 data inputs at the same moment in time using one of five display formats. These are binary, octal, decimal, hex or mixed (lines 15 to 8 in binary, lines 7 to 0 in hex). Data line 15 is the most significant bit and line 0 is the least significant bit.

8 indicators along the bottom of the display provide further information.

For example the same word can be displayed in five ways:

The data displayed comes from one of three locations, the Data Latches (Data Output A Figure 1), the Acquisition Memory (Data Output B Figure 1), or the Reference Memory.

In the 'Monitor' mode the display acts as a simple logic monitor and is updated continuously to show the state of the data inputs (subject to the presence of a Sample Clock waveform).

When recalling data from one of the memories the display shows the single 16 bit word at the cursor position. The cursor can be moved to any position in either memory and the position can be shown in decimal on the display (+999 to −999 for the Acquisition Memory, or +99 to −99 for the Reference Memory).

The oscilloscope display

The LA-160 can be connected to any conventional oscilloscope with variable timebase to obtain a timing diagram display of 8 or 16 channels from either of the memories.

The logic levels for the word at the memory cursor position are displayed at the centre of the oscilloscope screen, preceded by the levels for the 25 words before the cursor and followed by the levels of the 25 words after the cursor. Thus the oscilloscope displays a plot of the logic states for each channel during 51 cycles for the storage clock.

Connections

The LA-160 has 24 inputs. Sixteen of these are used for recording the data, while the other eight are used for controlling the recording process. The inputs are split into three groups each of which uses a 15 way female D connector.

Each input has a threshold level of about 1.4V and a load equivalent to one LSTTL gate input. This is suitable for use with most 5V logic families including TTL, DTL, NMOS, PMOS, and CMOS.

Great care must be taken to ensure that the inputs are not taken outside of the voltage range −0.5V to +5.5V, as might occur when working on circuits which have auxiliary voltage rails in addition to +5V. To avoid any possibility of damage we recommend that connections are made via the optional LC-01 buffered input pods since these allow voltages up to ±15V to be applied to the inputs without damage.

Table 1 **Input Characteristics**

The 24 inputs have characteristics as follows:

Data inputs:
1 x LSTTL Schmitt trigger gate load
typical positive going threshold +1.7V
typical negative going threshold +0.9V

Trigger Enable inputs:
1 x LSTTL standard gate load typical
threshold +1.4V

Clock input Clock Enable inputs Trigger Arm input:	1 x F series standard gate load typical threshold +1.5V

Typical input current for all inputs is +20μA with the input level high and −400μA with the input level low.

NB. An unconnected input will always be 'high'.

Important. The inputs must not be taken outside the voltage range −0.5V to +5.5V. In circumstances where overvoltage could occur accidently we recommend the use of the optional LC-01 buffered data pods.

Set-up conditions

The 'set-up' conditions for the LA-160 can be inspected and modified using the key-pad. The 'set-up' parameters are marked in orange above the keys 1 to F. Depressing a key will cause the display to show the current state of that parameter, and allow it to be 'modified' if required.

The 'set-up' conditions are stored in permanent memory and are retained even when power is removed. As supplied the LA-160 is set-up as shown in Table 2.

The LA-160 can be returned to its original set-up conditions at any time by holding the Escape key depressed until the display shows '88888888'.

Table 2 **Set-up conditions**

Parameter	Initial set-up	Alternatives
Clock Source	Internal	External
Clock Polarity	Positive	Negative
Clock Period	100ns	Fifteen alternatives up to 800μs
Clock Enables	Both 1s	0
Logic	Positive	Negative
Trigger Word	All don't cares	As required
Trigger Hold-off	Off	On
Trigger Enables	All 1s	0
Trigger Arm	1	0
Trigger Arm Delay	Off	On
Data Display Format	Hex	Binary, Octal, Decimal, Mixed
Acquisition Memory cursor position	000	−999 to +999
Reference Memory cursor position	00	−99 to +99
Reference Memory Limits	−99, +99	As required
Search Word	All don't cares	As required
Oscilloscope display mode	All 16 channels	Lo8, Hi8
Conditional Repeat mode	Stop on Fail	Pass

Setting the clock parameters

Clock Source

The Clock Source can be Internal (ie. generated within the LA-160) or External (ie. supplied via the clock input). When Internal Clock is selected the appropriate indicator is illuminated.

Clock Polarity

The analyser can be set to sample data on either the positive or negative going transition of the Sample Clock waveform.

Clock Period

The Internal clock can be set to any one of the sixteen frequencies between 10MHz and 1.25kHz. This is equivalent to a period between successive samples variable from 100nsecs up to 300μs.

Clock Enables

Sampling only occurs when both clock enables are True. The Clock Enables use positive logic, ie. a high level at the input represents a 1. Each enable can be set to be True with the input high (1) or low (0).

NB. Unconnected inputs will always be high.

Setting the data display format

The 16 channels can be displayed in one of five formats; binary, octal, decimal, hex or mixed (upper lines binary, lower lines hex). The format set for

the display of data is also used for the display of the Trigger Word and the Search Word.

The data is always displayed with the most significant digit on the left hand side and the least significant on the right hand side.

Binary format

Depress 'Binary', the data is shown in binary format (16 upper or lower segments).

In Binary format the data input line number corresponding to each bit displayed is marked above the display. The upper eight lines (8 to 15 inclusive) are also marked with the mnemonics for the control lines of the General Purpose Interface Bus.

Octal format

Depress 'Octal', the data is shown in octal format (6 digits, 0 to 7) with a letter 'o' on the right hand side.

Decimal format

Depress 'Decimal', the data is shown in decimal format (5 digits, 0 to 9) with a letter 'd' on the right hand side.

Hex format

Depress 'Hex', the data is shown in hexadecimal format (4 digits, 0 to F). In this mode the cursor position is simultaneously displayed to the right of the data whenever data is being recalled from either of the memories. When reviewing the trigger word or search word a letter 'h' is displayed on the right hand side.

Mixed format

Depress 'Mixed', the data is displayed in mixed format (8 upper or lower segments plus 2 digits, 0 to F).

Don't Care states

A Don't Care state is indicated by a ¦ symbol in binary mode, and a ≡ symbol in octal or hex modes. Don't Care states cannot be entered in decimal. If a word that contains Don't Care states is reviewed in a mode other than that in which it was set, those digits which partially contain Don't Care states will flash to indicate this.

Setting the trigger parameters

Trigger Word

The Trigger Word can be set in any of the five display formats (Binary, Octal, etc). If it is required to change the format depress the appropriate display format key prior to setting the Trigger Word. Don't Care states can be included within the trigger word in all display formats except decimal.

Trigger Word Hold-off

This facility prevents a Valid Trigger Word signal from being generated unless the trigger conditions have been satisfied for at least two clock periods. This prevents spurious triggering on glitches or transitory states when bus lines are changing and is useful when capturing data asynchronously. It should not be used during high speed synchronous acquisition (2MHz and above).

Trigger Enables

A Trigger Event only occurs when all four Trigger Enables are 'True'. The Trigger Enables use positive logic, ie. a high level at the input represents a 1. Each enable can be set to be True with the input high (1) or low (0).

NB. Unconnected inputs will always be high.

Trigger Arm

The Trigger Arm facility enables the triggering of the analyser to be delayed until after the occurrence of some external event. If a data acquisition is started with the Arm input false, the instrument will not trigger until after the input has been taken True. In order to be accepted, the arm input must be True during at least one active transition of the Store Clock waveform, its condition following this is then ignored. An LED on the display illuminates as soon as the Trigger Arm is accepted.

The Arm input uses positive logic and can be set to be true with the input high (1) or low (0).

NB. An unconnected input will always be high.

Trigger Arm Delay

When no external Trigger Arm signal is available, the Arm input will normally be set so as to be permanently True. In this circumstance the analyser may trigger before 1,000 Store Clock cycles have occurred, in which case the pre-trigger information in the Acquisition Memory will be only partially valid. To avoid this condition the operation of the Trigger Arm can be delayed by 1,024 Storage Clock cycles, ensuring that the memory always contains valid pre-trigger information.

Setting the data logic polarity

All the control inputs operate in positive logic only, ie. a high level on a control input always represents a logic level 1. The Data Inputs, however, can be set to operative or positive or negative logic.

Using the LA-160 as a logic monitor

By depressing 'Shift' followed by 'Monitor', the analyser operates as a simple logic monitor. In this mode the display shows the state of the Data Inputs updated in synchronism with the Sample Clock waveform, irrespective of the trigger conditions.

The data can be displayed in any of the display formats. No oscilloscope display is available in this mode.

The Monitor mode is useful as a means of continuously observing the state of the data lines.

Data acquisition

The analyser has three acquisition modes:
single shot, repeat, and conditional repeat. The following instructions assume that the Clock parameters have been set up to achieve a valid Storage Clock signal and that the Trigger parameters have been set up to enable a Trigger Event to occur.

Single shot

Depress 'Single'. The analyser starts writing data into the acquisition memory synchronously with the Storage Clock waveform. As soon as the Trigger Arm is accepted the 'Armed' light will illuminate. Following this, as soon as a Trigger Event occurs the 'Triggered' light will illuminate and the analyser will stop writing data into its memory 1,023 clock pulses later. (NB The total memory size is 2,048 words but only 1,999 are accessible). The display will then show the message 'Full' to show that the memory has been filled. The 'Data' and 'Cursor' keys may then be used to examine the memory contents.

Automatic Repeat

Depress 'Shift' followed by 'Repeat'. The analyser will then perform a data acquisition and, when completed, will display the data at the Acquisition Memory position indicated by cursor. It will display the data for just under two seconds before automatically performing another acquisition and so on until 'Stop' is depressed.

Conditional Repeat

The analyser can be set to perform acquisitions repeatedly with minimum delay and to stop auto-

matically, either when the contents of a portion of the Reference Memory becomes identical with a portion of the Acquisition Memory (Stop on Pass) or not identical with it (Stop on Fail).

In this mode the analyser is repeatedly using the Memory Compare function described later.

Set the Acquisition Memory cursor position and the Reference Memory limits as required. Depress 'Shift' followed by 'Cond Rpt', the display will show 'Stop = P' or 'Stop = F' indicating whether the repeating acquisitions are to be stopped on a Pass or a Fail condition, use 'Modify' to change this if required. Depress 'Cond Rpt' again, the analyser will commence data acquisitions.

Using the Acquisition Memory

The Acquisition Memory has a total capacity of 2,048 sixteen bit words of which only 1,999 are accessible.

When the analyser is first switched on, the memory contents are entirely random. When a data acquisition is started the analyser starts to write data into the Acquistion Memory in synchronism with the Storage Clock overwriting the existing data. When 2,048 words of data have been written in, this data starts to be overwritten with newer data and so on. This process can be stopped in one of two ways:

i) by a Trigger Event: the LA-160 defines the memory address to which data is being written when the Trigger Event occurs as 000, it then continues to write data into the memory for 1,023 cycles of the Storage Clock before stopping. Thus 1,023 words of post trigger data are stored, of which 999 are accessible. The amount of pre-trigger data is equal to the number of cycles of the Storage Clock that occurred between the start of the acquisition and the Trigger Event, the maximum being 1,024 words of which 999 are accessible. Trigger Arm Delay can be used to prevent triggering until at least 1,024 cycles have occurred thus ensuring the maximum amount of valid pre-trigger data.

ii) by depressing 'Stop': this stops the acquisition immediately and defines the memory address then being written to as 000. The display will show 'Not Trig' and the memory will contain pre-stop data equal to the number of cycles of the Storage Clock that had occurred, the maximum being 2,047 of which 999 are directly accessible.

If 'Stop' is depressed after a Trigger Event has occurred but before 1,023 further Storage Clock cycles have occurred, the display will show 'Not Full' and only a limited amount of valid post trigger data will then be available.

Displaying the contents of the Acquisition Memory

The keys marked 'Aqu Mem' and 'Ref Mem' select between a display of the Acquisition Memory contents and the Reference Memory contents. Having selected the Acquisition Memory, depressing the key marked 'Cursor' will cause the display to show the current position of the acquisition memory cursor in decimal. Depressing the key marked 'Data' will cause the display to show the data stored at the cursor position. (In hex mode the cursor position will be displayed simultaneously with the data.)

Displaying and moving the cursor position

By depressing the key marked 'Cursor', the single line display will show the position of the cursor in decimal. This can be anywhere between +999 and −999 if the acquisition memory is being recalled, or +99 or −99 if the reference memory is being recalled. To return to a display of the data at the memory position indicated by the cursor, depress the key marked 'Data'.

Simultaneous display of cursor position and data

In hex mode only, depressing 'Data' will cause the display to show the data in hex on the left hand side and cursor position on the right hand side.

Moving the cursor position

The two keys marked with arrows are used to shift the cursor position. The key with the arrow pointing right moves the cursor towards more recently stored data (a more positive value) whilst the key with the arrow pointing left moves the cursor the other way.

A single depression of these keys moves the cursor one memory location, if the keys are held depressed they will autorepeat.

Alternatively the cursor position can be moved using 'Modify'. With the cursor position displayed, depress 'Modify', the existing position will start to flash, enter the required position (changing the sign with the +/− key first if required), the cursor position is moved as the final digit is entered.

Returning the cursor position to zero

If the 'Cursor' key is held depressed the cursor position will be automatically reset to 000 or 00.

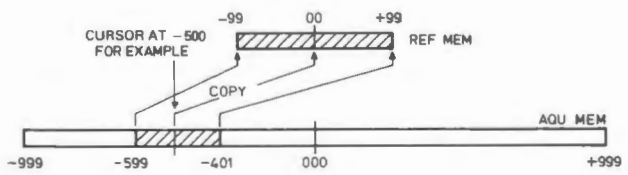
Using the Reference Memory

The Reference Memory has a capacity of 199 sixteen bit words. This memory can be loaded from the Acquisition Memory and can be modified via the keyboard.

The Reference Memory is non-volatile and therefore its data is retained when the analyser is switched off.

Loading the Reference Memory

The Reference Memory can be loaded automatically with a block of 199 words from the Acquisition Memory. The position of the block which is copied is defined by the position of the acquisition memory cursor, see below.



Position the Acquisition Memory cursor at the centre of the block of data which is to be copied into the reference memory. Depress 'Shift' followed by 'A→R'.

Displaying the contents of the Reference Memory

Depressing 'Ref Mem' causes the display to show either the Reference memory cursor position or the data at that cursor position in exactly the same way as for the Acquisition Memory.

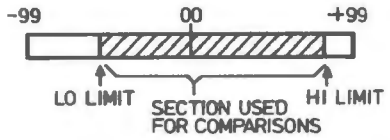
When in this mode the 'Ref Mem' indicator on the display flashes. To return to displaying the Acquisition Memory depress 'Aqu Mem'.

Modifying the contents of the Reference Memory

The contents of the Reference Memory may be modified using the 'Modify' key in the same way as a Trigger Word or a Search Word is modified. Don't Care states can be included.

Limiting the size of the Reference Memory

When using the Automatic Memory compare facilities (Compare or Conditional Repeat), it may be desirable to limit the size of the block of data which is used for the comparison. This can be achieved by limiting the effective size of the Reference Memory.



Using the Oscilloscope Display

Depress either 'Data' or 'Cursor'. The logic levels for the word at the memory cursor position are then displayed at the centre of the oscilloscope graticule preceded by the levels for the 25 words before the cursor and followed by the levels for the 25 words after the cursor. Each word appears on one of the major or minor divisions of the graticule. Thus the logic waveforms of each of the sixteen input channels covering 51 cycles of the Storage Clock are displayed. Line 15 is at the top and line 0 is at the bottom. the lines are arranged in blocks of four to make identification easier.

The oscilloscope can display data from either the Acquisition or the Reference Memory. When the cursor is moved the display will scroll left or right.

As an alternative to displaying sixteen channels, the oscilloscope can be set to display the upper or lower eight channels only. This enables the waveforms to be examined in more detail and increases the trace brightness.

Depress 'Scope 8/16' until the display reads 'Lo 8' or 'Hi 8' as required and change the oscilloscope's vertical sensitivity to 100 mV/div.

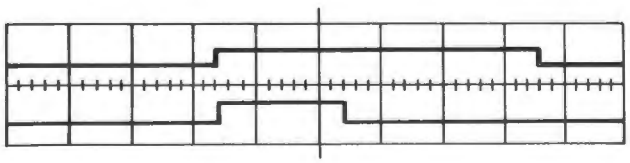
Depressing 'Scope Ref' causes the set-up waveform to be displayed for as long as the key is held depressed. This enables the graticule centering to be quickly checked and the low state of all the lines to be observed. Alternatively the analyser can be put permanently into this state by depressing 'Escape'.

Holding 'Compress' depressed when viewing the Acquisition Memory causes the display to show 51 words at 10 word intervals, thus giving an overview of 510 words. This can be useful in locating the position of a particular event such as a line changing polarity.

Making time measurements

When the clock speed is known (eg. when using the internal clock), the oscilloscope display can be used for timing measurements.

As an example, the diagram below shows two pulses sampled with a 100 ns clock period. They appear with coincident leading edges, but non-coincident trailing edges; thus demonstrating that the leading edge positions are within 100 ns of one another, whilst the trailing edge positions differ by 16 x 100 ns (ie. 1.6 μs $\pm$0.1 μs).



Where a timing measurement across more than 50 clock periods is required, this can be done by moving the cursor until each point falls on the graticule centre, and then subtracting the two cursor location values.

Using the Word Search facility

The LA-160 can be made to automatically search through its Acquisition Memory in order to find a specified word. This facility is very useful during software analysis for locating specific sections of code.

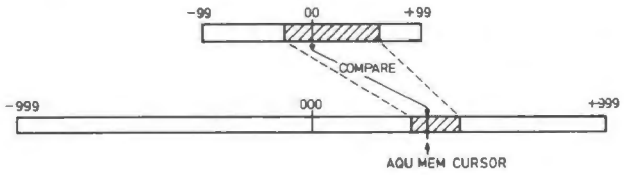
Depress 'Shift' followed by 'Search'. The display will show the existing state of the search word. This can be modified using the 'Modify' key in the same way as setting the Trigger Word. Don't Care states can be included.

Depress either of the cursor shift keys (→ or ←) and the analyser will automatically move the cursor backwards or forwards from its present position until an occurrence of the search word is found. The analyser then stops with the display showing the cursor position. Depress one of these keys again and the cursor will move on to the next occurrent of the search word.

If the cursor gets to either end of the acquisition memory, the display will show the message Fail 999 or Fail −999.

Using the Memory Compare facility

The LA-160 can be made to automatically compare the contents of the Reference Memory with the contents of the block of the Acquisition Memory of the same size.



The portion of the Reference Memory used is as defined by the Reference Memory Limits facility, whilst the portion of the Acquisition Memory used is defined by the current position of the Acquisition Memory cursor. The current position of the Reference Memory cursor is ignored.

Depress the 'Shift' key followed by the key marked 'Compare'. The LA-160 will automatically move both cursors from one end of each memory block to the other, continuously comparing the data at each point. If all the data matches, the cursors will be returned to the Reference Memory 00 position and the display will show the message PASS. If a mismatch is found, the cursors will be returned to the Reference Memory 00 position and the display will show the message FAIL.

The analyser can be made to perform a Memory Compare automatically every acquisition.

Using the Word Compare facility

The LA-160 can be made to automatically compare the contents of the Reference Memory one word at a time.

The section of the Acquisition Memory used is defined by the current position of the Acquisition Memory cursor. The current position of the Reference Memory cursor is ignored.

Depress 'Shift' twice followed by 'Word Comp'. The display will show the current Acquisition Memory cursor position, or 00 for the Reference Memory cursor position along with the message PASS if the two words of data match, or FAIL if they mismatch.

Depressing either of the cursor shift keys will step the comparison words forwards or backwards. Holding either key depressed will cause them to autorepeat. Whenever a change from PASS to FAIL or from FAIL to PASS occurs, a short bleep will be produced.

The memory contents 'Send' facility

The LA-160 can be made to output the entire content of its acquisition memory as serial ASCII data at RS423 levels.

128 strings of 73 eight bit ASCII characters are transmitted with a baud rate of 9,600 and a character repetition rate of 1.25msecs.

CR	Carriage Return
LF	Line Feed
Null Null	Two Nulls
S	Letter S
XXXX	Address of 1st data word in Hex
XXXX XXXX etc	16 sequential data words in Hex

Thus the first string contains the address 0000, the second string 0010 etc. All 2048 data words are sent starting with the earliest pre-trigger word and ending with the last post-trigger word. The trigger word is sent in the 65th string as the first data word after the address 0400.

The 'Send' facility is intended for use with a computer, where the data can be written directly into memory and then analysed further (eg. disassembled). It can also be used to drive a printer which has a suitable serial interface.

Depress 'Shift' twice followed by 'Send'. The analyser will start to output data, and will return to 'ready' when this is completed.

The rear panel connector signals

Five output signals and one input signal are available on the nine pin D connector mounted on the rear panel. The connections are as follows:

Pin No.	Function
1	Trigger Word Recognition output
2	RS423 Data output
3	'Clear to Send' input
4	Internal Clock output
5	Internal Clock 10 output
6	'Triggered' output
7	Ground
8	Ground
9	Ground

Internal Clock output

When the internal clock is selected, a TTL level signal at the same frequency is available on pin 4. This can be used to drive the circuit under test for synchronous acquisition using the internal clock.

Internal Clock 10 output

When the internal clock is selected a TTL level signal at one tenth of this frequency is available on pin 5. If this is used to drive the circuit under test then synchronous acquisition will be achieved with the analyser taking ten samples for every clock period of the circuit under test. This can be very useful for locating hardware faults.

'Triggered' Output

The 'Triggered' Output is a TTL level signal available on pin 6. This signal goes low at the start of a data acquisition and is then latched high by the occurrence of a trigger event. This signal may be useful for driving external equipment eg. generating a hardware break for a microprocessor system.

Trigger Word Recognition output

The Trigger Word Recognition output is a TTL level signal with an open collector output and 1kΩ pull-up impedance. It is available on pin 1. The output goes high whenever the data word matches the trigger word, at all other times it is low.

This signal can be useful for such things as qualifying the point at which the LA-160 responds to a trigger event. For example if the signal is fed to a counter whose output is connected to the Trigger Arm input of the LA-160, triggering can be prevented until the nth occurrence of the trigger word as set by the counter.

NB. This signal must not be loaded by more than 50pF if correct operation is to be maintained.

RS423 Serial output

This is a bipolar output available on pin 2. The typical output level is ±4V (8V pk-pk) at Z_{OUT} = ½kΩ. The idle state is low. The signal is used for sending data to a computer or printer which has a serial data input at RS423 or RS232 levels. Operation of the RS423 output is controlled by the 'Send' or 'Print' routines.

'Clear to Send' input

This input has a threshold of about +1.4V and will accept bipolar signals up to the RS232 maximum of ±25V. It is available on pin 3.

When this input is taken high, the RS423 output is enabled to output data as controlled by the 'Send' or 'Print' routines. The RS423 output is disabled during periods when 'Clear to Send' input is taken low or left unconnected.

LC-01 Buffered input pod (611-307)

The LC-01 provides a convenient means of connecting the LA-160 to the circuit under test whilst at the same time providing protection against accidental overvoltage of the inputs. One LC-01 is required per input connector, so that three will normally be needed.

The LC-01 consists of a 15 way D connector linked to a pod by 0.6 metres of ribbon cable. The pod is automatically powered from the analyser and contains eight high impedance buffers along with protection components which enable voltages up to ±15V to be applied without damage. The input impedance is 100kΩ, and the threshold is +1.4V, as per standard TTL.

At the end of the pod is a standard 10 way 0.1in pitch header providing 8 signal inputs plus two grounds. This header mates with either the ten way wireable socket provided or with the optional LG-09 logic grabber set which consists of nine colour coded logic grabbers wired to a ten way socket.

LR-64 Extended facilities ROM (611-408)

The LR-64 is an additional ROM which extends the software facilities of the LA-160. It is easily retro-fitted by the user.

The additional facilities are those marked in brackets on the keyboard. If these facilities are selected on an LA-160 which is not fitted with the LR-64, a brief "error" message will be displayed.

The additional facilities are as follows:

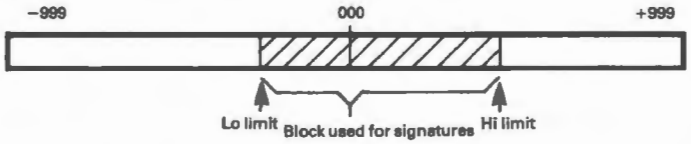
Signature

This function enables a section of data within the acquisition memory to be compressed into a 4 digit hex 'signature'. The purpose of this is to enable the user to immediately identify a block of data as being correct or incorrect by means of its unique signature.

The signature facility is a very fast way of comparing suspect data with known good data, and allows go, no-go testing to be performed by unskilled operators by comparing signatures against prepared documentation.

The LA-160 calculates 17 signatures simultaneously, a signature for all 16 data channels together and a signature for each individual data channel. Thus the data can first be verified for all 16 channels and then, if incorrect, each data channel can be checked separately.

The user can select the size and position of the acquisition memory block used for signatures by specifying a low and high address limit.

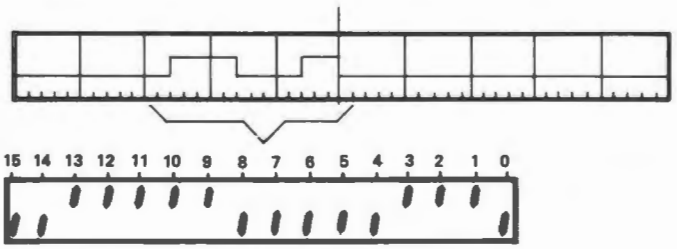


As supplied these limits are pre-set to −099 and +099. The length of time taken to calculate signatures varies between 300msec for 50 words or less, and 10 seconds for 1,999 words.

Timing

This function enables the built-in single line display to show a timing diagram for any one channel. This is intended primarily for applications where no oscilloscope is available.

The display shows the state of the channel at the cursor position plus the states for the 15 store clock cycles prior to this.



The cursor can be moved using the cursor shift keys, with the Timing display scrolling left or right accordingly. The display can be rapidly switched between channels enabling Timing comparisons to be made. Both the acquisition and reference memories can be displayed in this mode.

Trigger Count Delay (**)

There may be occasions when it is desirable to prevent the analyser from triggering on the first occurrence of a trigger event, but to trigger on some later occurrence instead. For example the user might require to trigger on the third call of a subroutine within a nested loop.

The Trigger Count Delay facility enables the point at which the analyser triggers to be delayed by up to 9,999 occurences of the trigger event. The trigger count delay number represents the number of occurrences of the trigger event which must occur between the analyser being 'armed' and the analyser being enabled to respond to a trigger event. This can be set anywhere between 0 and 9,999. Thus if it is set to 0002 the analyser will trigger on the third occurence of the trigger event.

Once set, the Trigger Count Delay will operate in all three of the acquisition modes ie. Single, Repeat and Conditional Repeat. During periods when the delay is operating the display will be blanked apart from a letter C on the left-hand side. This letter will be brighter than normal because the display multiplexing is disabled. During these periods the 'Stop' key will not operate and the acquisition can only be terminated by depressing 'Escape'.

The trigger counting system has a minimum repetition period of 50µsecs and therefore if any trigger events occur less than 50µsecs apart the analyser will ignore them.

NB. With the Trigger Count Delay set to 0000, the facility is completely inoperative. This is the condition set when supplied.

Print

This function enables a data print-out to be obtained using any printer which has an RS-232 serial input. Four print-out formats are available: state listing for sixteen data channels, signature listing, combined timing diagram and state listing, and a state listing for thirty-two data channels. All the formats, except the combined timing diagram and state listing, are available with any type of printer. The combined timing diagram and state listing format will only operate with an RS printer, Epson printer or a printer with Epson emulation.

The RS-232 printer input should be connected to the RS-423 logic analyser output as follows:

LA-160 RS-423 output		Printer RS-232 input
Data output (pin 2)	to	Data input (RCD) (pin 3)
Clear to send input (pin 3)	to	Data terminal ready (DTR) (pin 20)
Ground (pins 7, 8 & 9)	to	Ground (pin 7) link (pin 6 to pin 20)

A cable with the above connections is supplied with the LR-64 extended facilities ROM.

The printer interface must be set-up as follows: 9,600 baud: 8 bits: no parity: 1 start bit: 1 or 2 stop bits.

Print formats

Four format numbers are available. Formats 0, 1 and 3 will operate with any printer. Format 2 will only operate with an RS printer, an Epson printer or a printer with Epson emulation. Format 3 will only operate when the LE-32 thirty two channel extender is fitted.

All the formats include a statement of the analyser set-up parameters (ie. trigger word, clock source etc.)

Format 0 is a 16 channel state listing of whichever memory was most recently selected (acquisition or reference). When printing the acquisition memory the printout will list all the data between the two limits set-up using the 'signature' function (see 'Signature' section) which can be anywhere between −999 and +999 but which are factory initialised to −099 and +099. When printing the reference memory, the print-out will list all the data between the two limits set-up using the 'RM limits' function which are factory initialised to −99 and +99.

The data at each memory location is printed simultaneously in three formats: binary plus ASCII plus octal, decimal, hex or mixed. The last format is selected by the LA-160 display format-keys.

Format 1 is a listing of the signatures as would be calculated using the 'signature' function. In this format depressing 'Shift', 'Print' causes all 17 signatures to be calculated (using the present signature limits) and then printed out.

Format 2 is a combined timing diagram and state listing. It uses Epson graphics-mode control codes.

A sixteen channel timing diagram covering 51 words centred about the cursor is printed out. This can come from either memory and is identical to the timing diagram that would appear on the oscilloscope display. A state listing for these 51 words in binary plus ASCII plus octal, decimal, hex or mixed is also printed out.

Format 3 this can only be used when the LE-32 thirty two channel extender is fitted. It is similar to Format 0 but prints the state listing for all 32 channels.

RS data

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RS Data Library

Z8 applications

Introduction

The Z8601 is a single-chip microcomputer with four 8-bit I/O ports, two counter/timers with associated prescalers, asynchonous serial communication interface with programmable baud ranges, and sophisticated interrupt facilities. The Z8601 can access data in three memory spaces: 2K bytes of on-chip ROM and 62K bytes of external program memory, 144 bytes of on-chip Register, and 62K bytes of external data memory.

The Z8671 is a Z8601 with a Basic/Debug Interpreter and Debug monitor preprogrammed into the 2K bytes of on-chip ROM. This application note discusses some considerations in designing a low-complexity board that runs the Basic/Debug Interpreter and Debug monitor with an external 4K bytes of RAM and 2K bytes of ROM. The board stands alone, allowing users to connect it with a terminal via an RS232 connector and run the Basic/Debug Interpreter.

The user of this board can run Basic/Debug with little knowlege of the Z8601. The board, however, derives its power through its ability to execute assembly language programs. To use the board to its full potential, the Z8 Technical Manual/Z8671 Basic/Debug Reference Manual 903-921 (two volumes) should be read. The Manual includes general information, statement syntax, memory allocations, and other material regarding Basic/Debug and the Debug monitor provided by the Z8671.

Basic/Debug

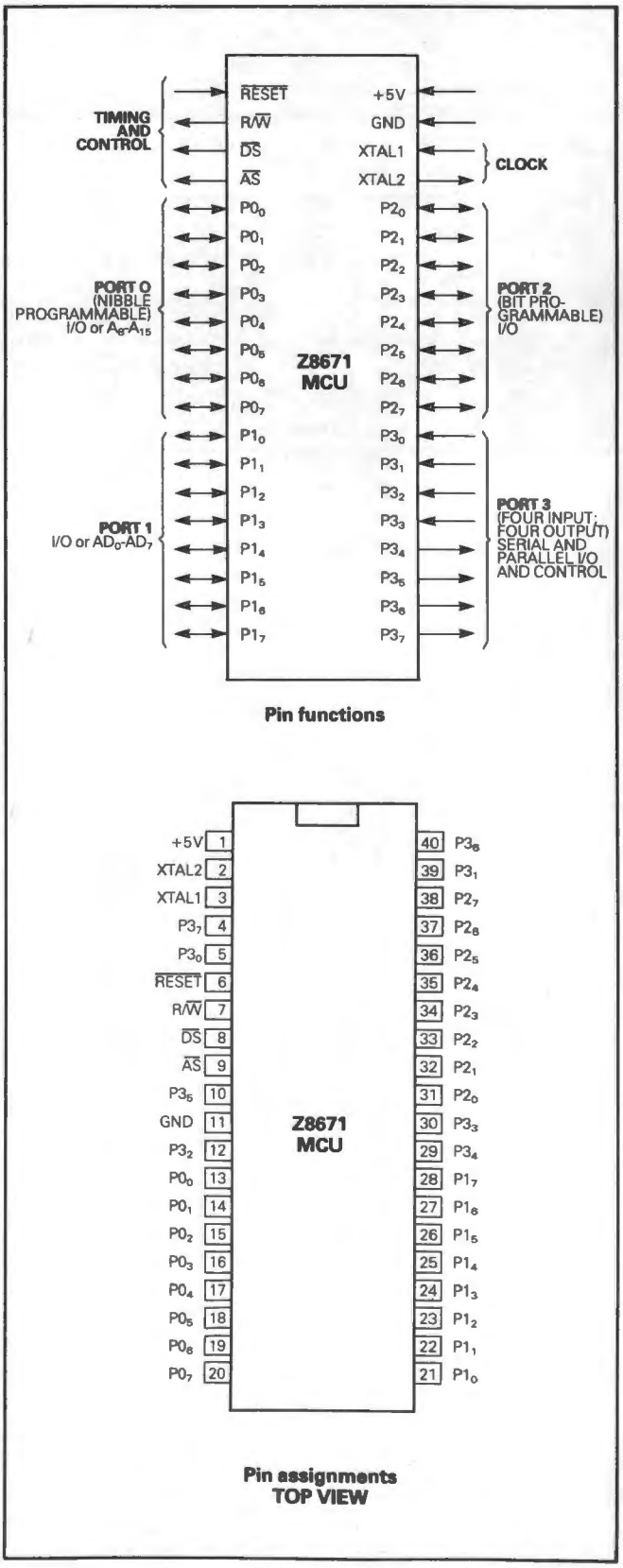
Basic/Debug is a subset of Dartmouth Basic, which interprets Basic statements and executes assembly language programs located in memory. Basic/Debug can implement all the Dartmouth Basic commands directly or indirectly.

One advantage to programming in Basic/Debug is the interactive programming approach realized because Basic/Debug is interpreted, not assembled or compiled. Modules are tested and debugged using the interactive monitor provided with Basic/Debug. Using Basic/Debug saves program development time by providing higher-level language statements that simplify program development. Using the INPUT and PRINT statements simplify debugging.

The Z8671 microcomputer

Basic/Debug controls the memory interface, serial port, and other housekeeping functions performed by the assembly language programmer.

The Z8671 uses ports 0 and 1 for communicating with external memory. Port 1 provides the multiplexed address/data lines (AD_0-AD_7); port 0 supplies the upper address bits (A_8-A_{15}). The Z8671



also uses the serial communications port for communicating with a terminal. Serial communication takes two pins from port 3, leaving six I/O pins from port 3 available to the user. The serial communication interface uses one of the two counter/timers on the Z8671 chip.

All other functions and features on the Z8601 are available with the Z8671. The user may reconfigure the Z8671 in software as a Z8601 if desired.

Applying the Z8671

Applications of the Z8671 range from a low-complexity home microcomputer that is memory intensive to an inexpensive, I/O-oriented microcontroller.

For home computer users, Basic/Debug is used like other available Basic interpreters. The Z8671, however, has many advantages over other computers. For example, the programmer can use the available functions such as interrupts to perform sophisticated tasks that are beyond the scope of other computer products. There is also a counter/timer that is used as a watchdog counter, a time-of-day clock, a variable pulse width generator, a pulse width measurement device, or a random number generator.

As an inexpensive microcontroller, Basic/Debug speeds program development time by calling assembly language subroutines (for time critical applications) and by supplying high-level Basic language statements that simplify the programming of noncritical subroutines.

Architecture

Two major design goals were set for this Z8671 Basic board. First, the board was to be simple. Second, the board needed to allow the user to write Basic programs and to utilize the features of the Z8601.

Overview

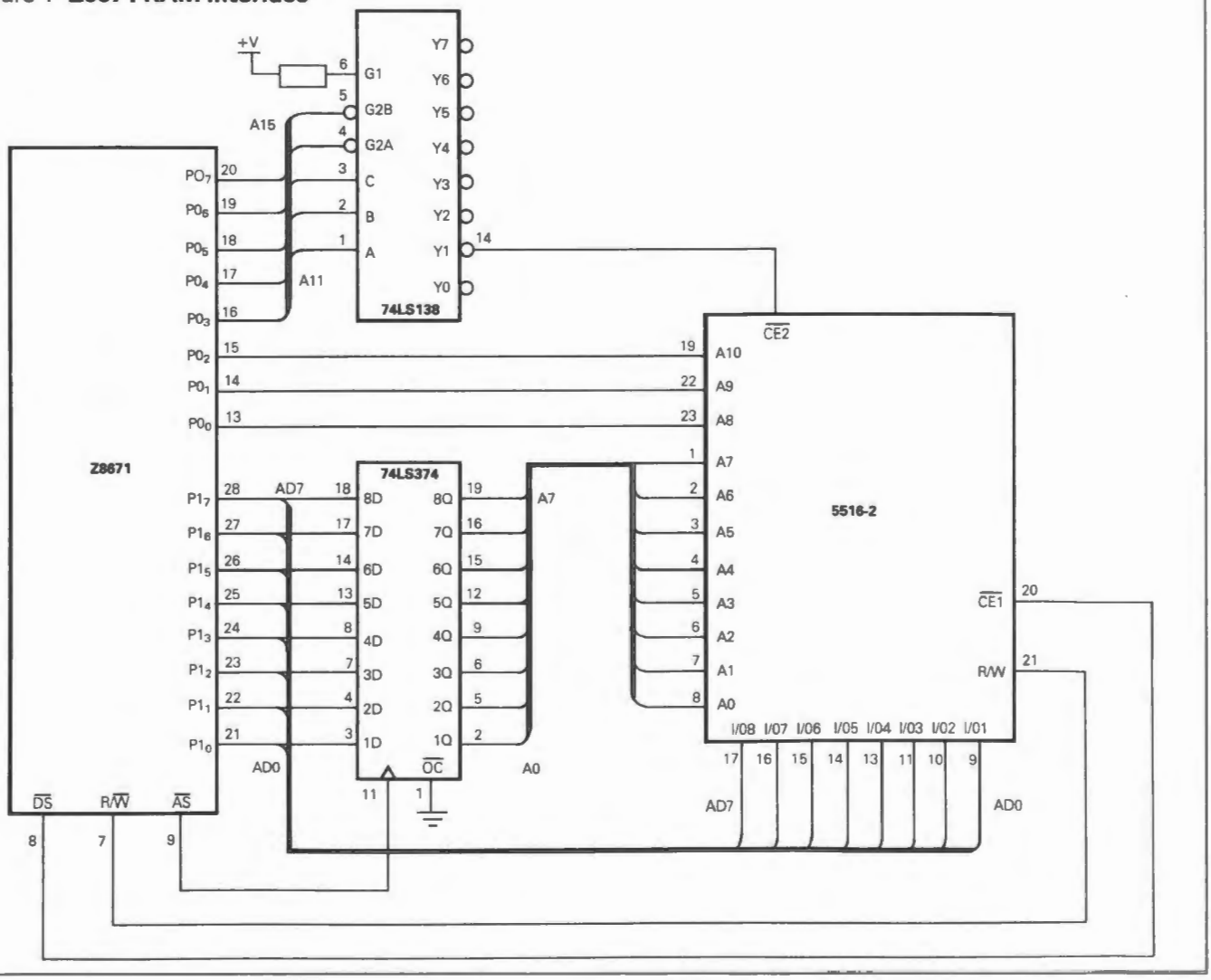
The board has eight IC packages:

- Z8671 (Z8601 preprogrammed with Basic/Debug)
- 5516 (2K bytes of static RAM) or 6264 (8K bytes of static RAM)
- 2732 (4K bytes of EPROM)
- 1488 (RS232 line driver)
- 1489 (RS232 line receiver)
- 74LS00 or 74LS10 (NAND gate package)
- 74LS138 (3 to 8 line decoder)
- 74LS374 (Octal Latch).

With these chips, a complete microcomputer system can be built with the following features:

- 2K byte Basic/Debug interpreter in the internal ROM.
- 2K or 8K bytes of user RAM
- 4K bytes of user-programmable EPROM
- Full-duplex serial operation with programmable baud rates
- RS232 interface
- 8-bit counter/timer with associated 6-bit prescalers
- 124 general-purpose registers internal to the Z8671

Figure 1 **Z8671 RAM interface**



- ★ 14 I/O lines available to the user
- ★ 3 lines for external interrupts
- ★ 3 sources of internal interrupts
- ★ Sophisticated, vectored interrupt structure with programmable priority levels. Each can be individually enabled or disabled, and all interrupts can be globally enabled or disabled
- ★ External memory expansion up to 124K bytes
- ★ Memory-mapped I/O capabilities.

This microcomputer can be used as a microcontroller, in which case a terminal is attached, via the RS232 interface, and Basic/Debug is used to create, test, and debug the system. When the system is debugged, the program is put into the EPROM, the terminal disconnected, and the board run standing alone. The terminal can be reattached at any time to monitor the subroutines running on the board.

The proposed boards meet the design requirements of simplicity and of allowing the user to write and debug programs in Basic while maintaining access to the Z8671 on-chip features.

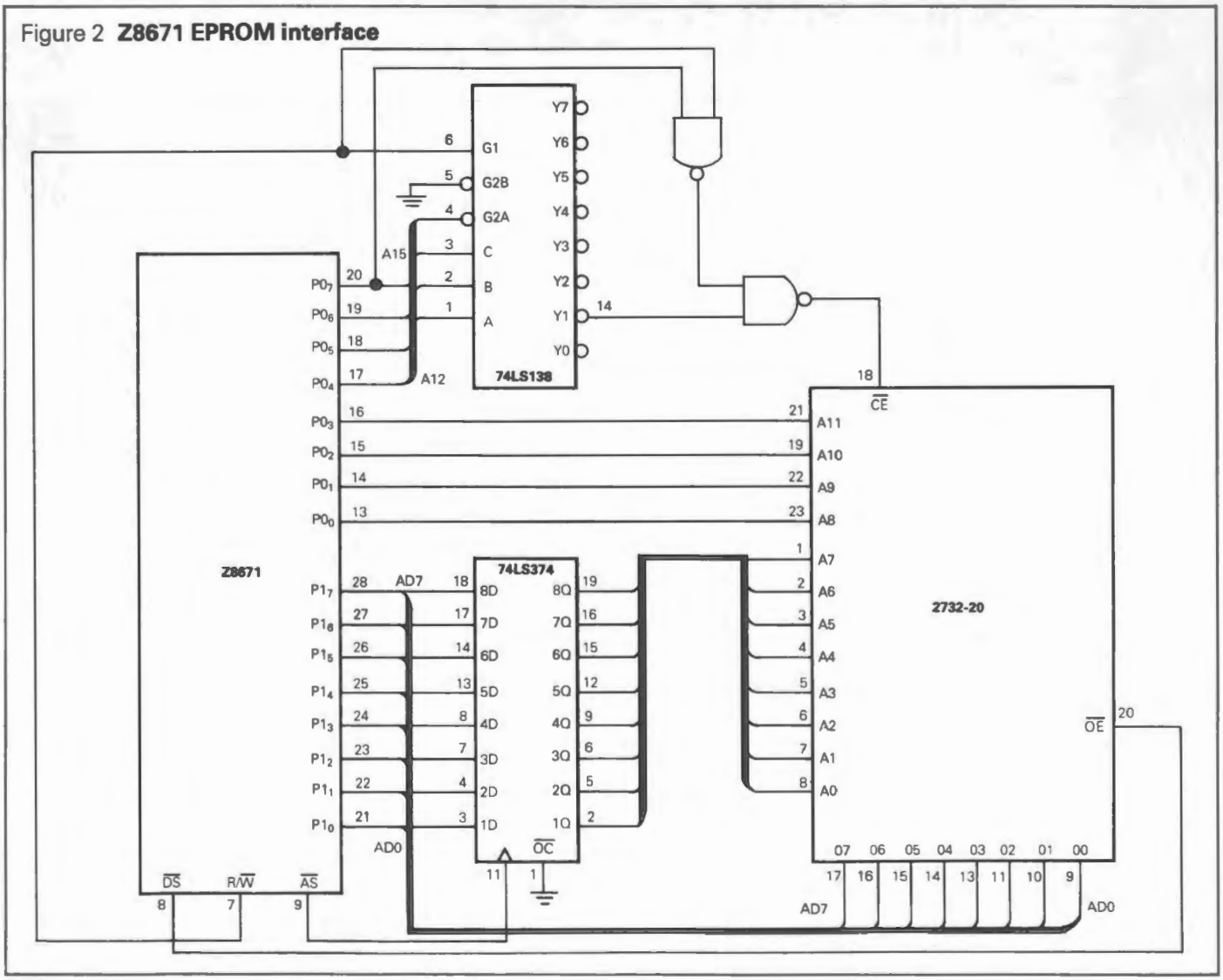
Interfacing the Z8671 with external memory

A simple RAM interface using the 5516 (2K byte) static Ram is shown in Figure 1, and a ROM interface using the 2732 (4K byte) EPROM in Figure 2. It is a fairly standard circuit with the 74LS374 being used to latch the low byte of the address and a 74LS138 providing address decoding. The major difference between the two is that the ROM circuit prevents memory accesses during a write cycle thus avoiding bus contention. This is carried out using the R/$\overline{W}$ signal as an enable on the address decoder. For a circuit using ROM and RAM this method cannot be used because the address decoder is used for both ROM and RAM. Examples of a mixed circuit can be seen in the full board designs (Figures 4 and 5).

Mapping the ROM at address 1000H to 1FFFH maintains compatability with Basic/Debug's Auto Start-up procedure. If this feature is not required then the address decoder can be omitted and $\overline{CE}$ can be obtained from the high order address bits.

Unique address space decoding can also be omitted for the RAM circuit but the Z8671, which sizes the RAM on power-up, could think that it has more RAM than there really is. This could cause problems with the GOSUB stack corrupting the Basic program and so care must be taken if a large Basic program is being run from RAM.

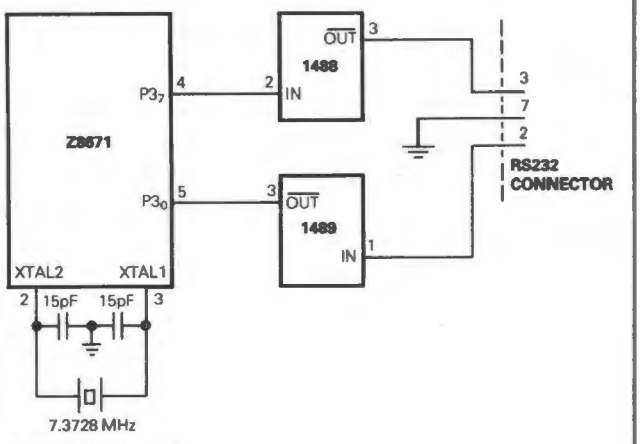
Figure 2 **Z8671 EPROM interface**



Interfacing the Z8671 with RS232 port

The Z8671 uses its serial communication port to communicate with the RS232 port. Driver and receiver circuits are required to supply the proper signals to the RS232 interface. The circuit of Figure 3 shows the interface between the Z8671 and the 1488 and 1489 for serial communication via the RS232 interface.

Figure 3 **Z8671 Interface for serial communications**



The serial interface is a simple type using only SI, SO and GND. The control signals CTS, DSR etc are therefore not required.

The Z8671 uses one timer and its associated prescaler for baud rate control. When the Z8671 is reset, it reads location FFFD and uses the byte stored there to select the baud rate. The boards described in this application note use EPROM to select the baud rate. On reset, the Z8671 reads FFFD, which is in the EPROM, and decodes the baud rate from the contents of that location. The baud rate can be changed in software.

Figures 4 and 5 show the full board designs implemented for this application note.

Figure 4 **Z8 Basic/Debug system with 4K EPROM and 2K RAM**

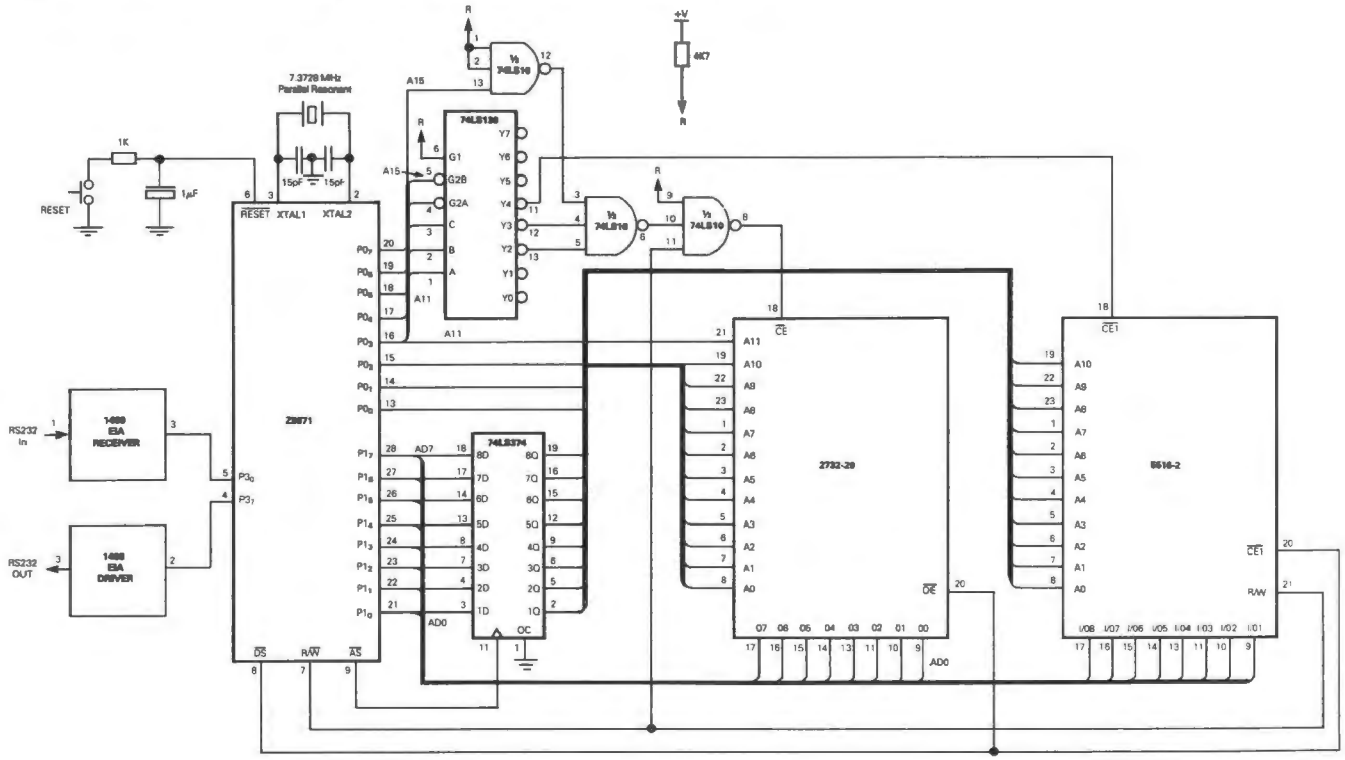
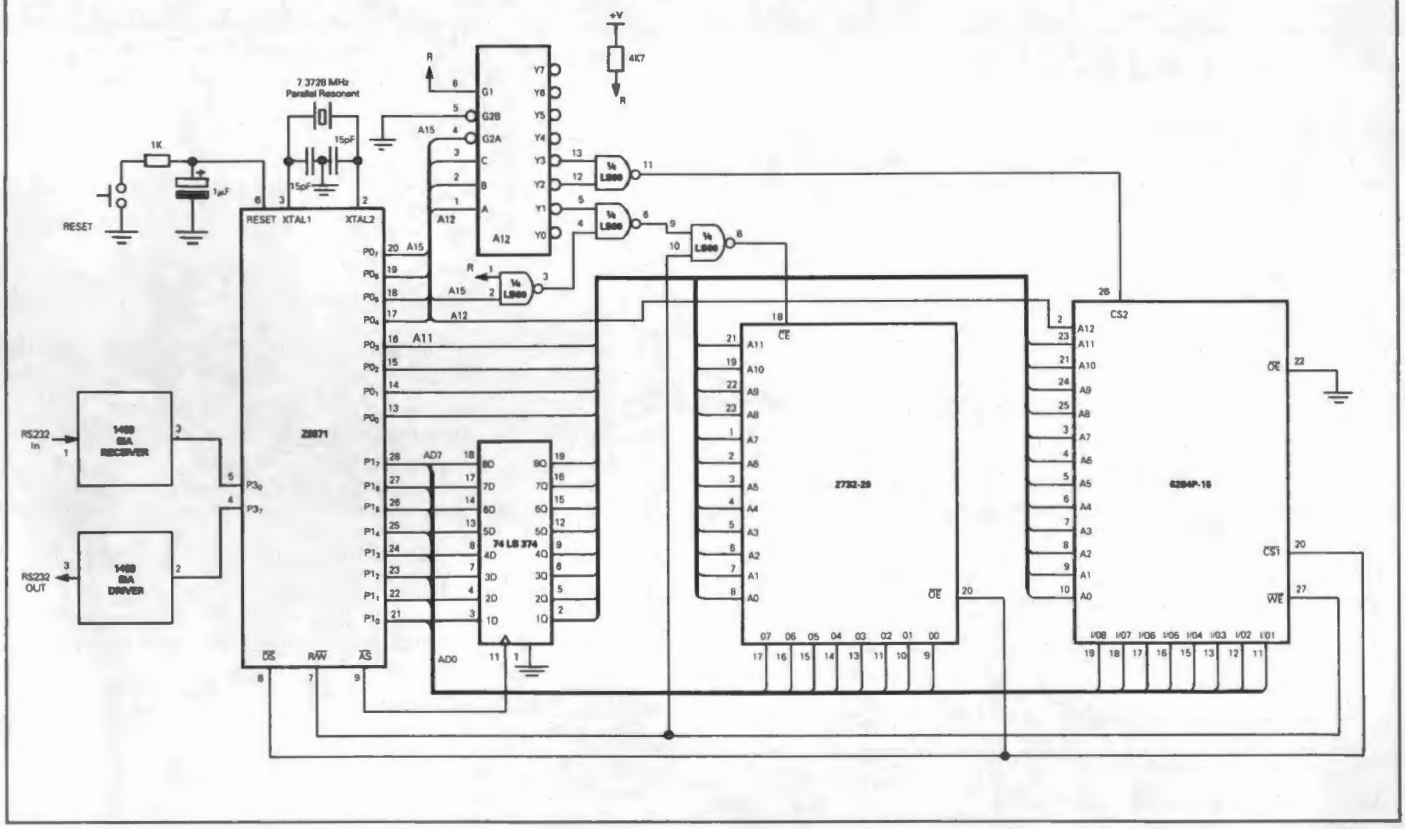


Figure 5 **Z8 Basic/debug system with 4K EPROM and 8K RAM**



Uncommitted I/O pins and other pins

Using the above design, port 2 is available for user applications. Any of the port 2 pins can be individually configured for input or output. There are also six pins in port 3 available to the user. The port 3 input pins can be used for interrupts.

Software

Getting started

The Z8671 board needs +5V and ground to run all components on the board except the 1488 EIA line driver. The 1488 needs +12V and −12V in addition to ground. (If not using terminal, the EIA driver/receiver circuit is disconnected. Consequently, the +12V and −12V lines are not required.)

The RS232 port can interface to any ASCII Terminal if the baud rate setting is matched to the value programmed into the EPROM. With power supplied to the board and the terminal connected to it, the reset button resets the Z8671 and the prompt character appears (":").

The board is ready for a Basic command when the ":" appears. The following sequence is a simple I/O example:

```
:10 input a
:20 "a=";a
:run
?5
a=5
:list
10 input a
20 "a=";a
:
```

When a number is entered as the first character of a line, the Basic monitor stores the line as part of a program. In this example, "10 input a" is entered. Basic stores this instruction in memory and prints another ":" prompt. The Run command causes execution of the stored program. In this example, Basic asked for input by printing "?". A number (5) is typed at the terminal. Basic accepts the number, stores it in the variable "a", and executes the next instruction. The next instruction (20 "a=";a) is an implied print statement; writing an actual "print" command is not necessary here. This line of code produced the output "a=5". The command "list" caused Basic to display the program stored in memory on the terminal.

Reading directly from memory

Basic lets the user directly read any byte or word in memory using the Print command and "@" for byte references or " ↑ " for word references:

```
:print @8
32
:printhex (@8)
20
:printhex ( ↑ 8)
2000
:
```

The first statement prints the decimal value of Register 8. The next statement prints the hexadecimal value of Register 8 and the last statement prints the hexadecimal value of Register 8 (20H) and Register 9 (00H).

Writing directly to memory

Basic lets the user write directly to any register or RAM location in memory using the Let command and either "@" or " ↑ ".

```
:@% a=%ff
: ↑ 8192=255
:print @10
255
:printhex ( ↑ %2000)
FF
:
```

The Let command is implied to save memory space but can be included. The first statement loads the

hexadecimal value FF into register 10 decimal (AH). The next instruction loads the decimal value 255 into register 8192 decimal (2000H). The print commands write to the terminal the values that were put in with the first two instructions.

Memory environment

Table 1 gives the memory configuration for the Z8671 application examples. Chip select is controlled from the address decoder for the RAM and the address/decode logic for the EPROM. In both cases several outputs of the 74LS138 are left free and these can be used for memory expansion or to decode addresses from peripheral devices. Mapping the EPROM at 1000H to 1FFFH maintains compatability with the Z8671 Auto Start-up feature and the mapping from 8000H to FFFFH allows the Z8671 to read the baud rate from the EPROM at address FFFDH (address FFDH in the EPROM).

Table 1 **The memory environment**

Decimal	Hex	Contents
0-2047	0-7FF	Internal ROM (Basic/Debug)
4098-8191 & 32768-65535	1000-1FFF & 8000-FFFF	EPROM (2732)
8192-10239	2000-27FF	RAM (5516)
8192-16383	2000-3FFF	RAM (6264)

Switching from RAM to EPROM

Register 8 and Register 9 contain the address of the first byte of a user program or, if there is no program, the address where the Z8671 will put the first byte of a user program. In this application example, when the Z8671 is reset and the EPROM does not contain the address, Register 8 and Register 9 contains a Basic program which points into RAM. EPROM is selected by changing the contents of Register 8 from 20H to 10H (see Table 2).

Table 2 **The registers**

Decimal	Hex	Contents
22-23	16-17	Current Line Number
8-9	8-9	Address of the First Byte of User Program

For more details on the register assignments, refer to the Pointer Registers-RAM System section of the Z8 Basic/Debug Software Reference Manual.

After the instruction " ↑8=%1000" is executed, the Z8671 accesses the EPROM on the Basic/Debug Board.

The example below shows how to switch from RAM to EPROM. The example uses two separate programs, one in RAM and one in EPROM. The RAM program is listed first, then the EPROM.

```
:printhex ( ↑8)
2000
:list
10 "executing out of RAM"
: ↑8=%1000
:printhex ( ↑8)
1000
:list
10 "executing out of EPROM"
:
```

Baud control

The baud rate is selected automatically by reading location FFFDH and decoding the contents of that location when the Z8671 is reset (the Z8 Basic/Debug Software Reference Manual contains the baud rate switch settings in Appendix B). This application example holds the baud rate settings in its EPROM. The least significant bits of location FFFD hex will provide baud rates as follows:

Baud rate	Value read
110	110
150	000
300	111
1200	101
2400	100
4800	011
9600	010
19200	001

After a reset, the baud rate is programmed by loading a new value into counter/timer 0 (see the Z8 Technical Manual, section 1.5.7). A Reset always changes the baud rate back to the rate selected from the contents of location FFFD.

Burning an EPROM

The EPROM contains the baud rate section byte in location FFDH. The other locations in memory are used for program storage. See section 6.3 of the Basic/Debug Manual for the format used to store programs in memory. This format is used to store programs in EPROM.

Example

The following is a printout of a game Super Brain written in Basic/Debug.

```
10 @243=7
20 @242=10
30 @241=14
40 x=usr(84): a=@242-1: x=usr(84): b=@242-1
50 x=usr(84): c=@242-1: x=usr(84): d=@242-1
55 "":i=0
100 "guess ",: in e,f,g,h
110 i=i+1
300 j=%7f22: k=%7f2a
301 t=0
302 r=0: p=0
310 if ↑j= ↑kp=p+1
320 j=j+2: k=k+2: t=t+1: if4>t310
330 j=%7f22: k=%7f2a
331 t=0
340 if ↑j= ↑kr=r+10: ↑j= ↑j+10: l=3
341 j=j+2
350 t=t+1: if 4>t310
351 j=%7f22
352 t=0
360 k=k+2: if%7f31>k340
363 j=%7f22: k=%7f2a
366 if ↑j>9 ↑j= ↑j-10
367 j=j+2
368 if%7f29>j366
370 "right";r; "place";p
380 if4>p100
390 y=999
400 "right in";i;"guesses; play another y/n":
    input x
410 if x=y10
```

Lines 10 through 50 comprise the random number generator for the program. The three lines:

```
10 @243=7
20 @242=10
30 @241=14
```

initialize counter/timer 1 to operate in modulo-10 count. Refer to the Z8 Technical Manual for complete information on initializing timers.

The "user (84)" function waits for keyboard input, the ASCII value of the key is returned in a variable

with the following command:

```
:10 x=usr(84): ""
:15 printhex(x)
:run
5
35
:
```

In the above example, the program waits at line 10 until keyboard input, in this case the number 5. The input value is stored in ASCII format in the variable "x". The line:

```
40 x=usr(84): a=@242-1: x=usr(84): b=@242-1
```

waits for input, reads the current value of timer 1, subtracts 1 (to get a number between 0 and 9), and stores the number in variable a. Then it waits for keyboard input at the second user function call, reads the current value of timer 1, subtracts 1, and stores the number in variable b. Line 50 of the example program gets two more random numbers and stores them in variables c and d. The four-digit random number is located in variables a,b,c, and d.

Line 300 assigns the location of variable a to variable j and the location of variable e (the first variable in the guess string) to the variable k. The strategy is to access these variables indirectly and to increment pointers j and k to access the variables.

A colon is used to separate commands on the same line. This is useful in packing the program into a small amount of memory space. The code, however, is harder to read. See section 5 of the Basic/Debug manual for more information on memory packing techniques.

Below is a sample run of the Super Brain Program:

```
:run
(<RETURN> on the keyboard is entered four times
  here)
guess ?0,1,2,3
right 2 place 0
guess ?4,5,6,7
right 2 place 1
guess ?0,2,4,6
right 3 place 2
guess ?4,2,1,6
right 4 place 4
right in 4 guesses
play another? y/n
?n
:
```

Conclusion

The design of these application examples met the major design goals of simplicity and functionality. The first goal is accomplished by prudent selection of support components, excluding any unnecessary chips. The board allows the user to exercise the full power and flexibility of the Z8601 not used by Basic/Debug. The user can write and debug Basic programs without detailed knowledge of the Z8601.

The Basic application example demonstrates a memory interface that is applicable for all Z8 Family members.

The software section explains the memory environment and gives several examples of Basic/Debug. These examples are a good introduction to the board and to Basic/Debug.

The Z8671 is a customized extension of the Z8601 single-chip microcomputer. The simplicity of the Basic application example demonstrates the flexibility of the Z8601 microcomputer in an expanded memory environment.

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RS data

Programmable logic controller (PLC) system

Introduction

A programmable logic controller is a system for controlling industrial and production processes, electomechanical equipment and automated assembly operations. This control function is performed by continuously monitoring the states of all the input devices connected to the controller (eg. proximity switches and mechanical contacts). Following the user instructions stored in the controller (known as the programme) the states of all of its output devices are set as appropriate (eg. relays, solid state relays or transistors). These output elements can in turn control the operation of an external system.

Due to the simplicity of entering and modifying the programmed instructions to suit the requirements of the process under control, the PLC is a truly versatile and flexible device that can be employed easily and efficiently to repeatedly control tasks that vary in nature and complexity.

A schematic diagram of the basic PLC control system is shown in Figure 1.

In this representation the central processing unit controls the overall operation of the system. Input devices may be switches, relay contacts, timers, solid state switches, proximity and limit switches, sensors, analogue to digital converters or other electronic circuits. The output devices may be external relays, heating elements, lights, alarms, subassemblies, electronic and electrical circuits, motors or other electromechanical devices.

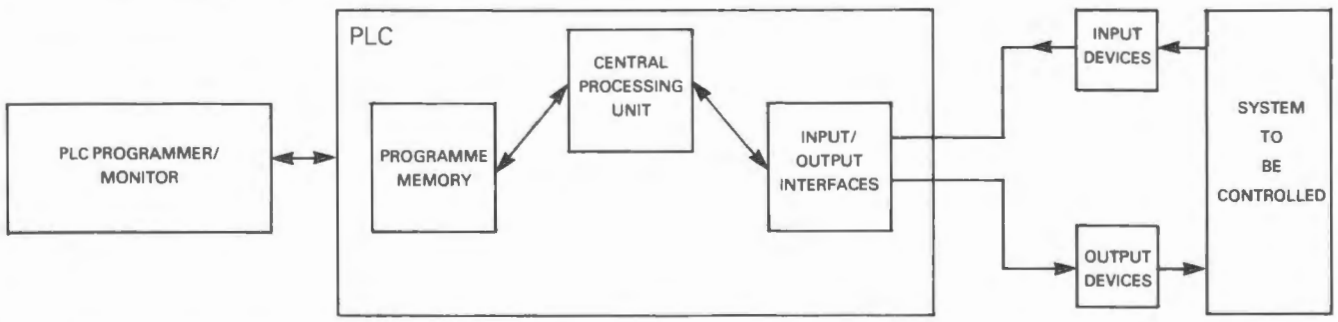
To illustrate the advantages of using a PLC over a traditional electromechanical system consider a control system with 20 input/output points. This assembly could comprise 60-80 relays, some counters and/or timers and a great deal of wiring. This assembly would be cumbersome with a power consumption of 30-40VA. A considerable time would be required to design, build, test and commission the assembly and once it is in full working order any desired modifications, even of a minor nature, could require major hardware changes. Alternatively, in the majority of applications the same control function can be performed using the RS PLC base unit 332-745. Once programmed (using the programming panel) the controller can be directly connected to the input and output devices. Programming will typically take 1-2 hours. Any alterations to the control function of the system can be simply implemented within minutes by modifying the stored programme. Other advantages over more conventional systems include compact size, low power consumption, fast response, versatility and lower overall cost. By doubling the input/output requirements the advantage of using a PLC becomes much more significant due to the complexity of the equivalent hardwired system and its labour and material costs.

The RS programmable logic controller system

The RS PLC system is a powerful, compact, modular system with an input/output (I/O) capability of up to 40 devices. It can replace efficiently and cost effectively traditional hardwired relay systems, timers, counters and sequence controllers. The ease of installation and connection to a particular assembly greatly reduces the cost and effort normally associated with traditional hardwired systems. In addition, the ability to quickly change the programme results in simple alterations to the control function if required. Thus the PLC can be used to control a certain task and then, when no longer required, it can be removed, reinstalled onto another system and reprogrammed to perform an entirely different control function.

The RS PLC system comprises a base unit (20 I/O), an extension unit (20 I/O), a programming panel, an EPROM programmer and a blank EPROM cassette. In addition a standard 35mm DIN rail mounting kit is available to suit the base and extension units. A base unit plus a programming panel are required to form a basic operational system.

Figure 1 **Schematic diagram**



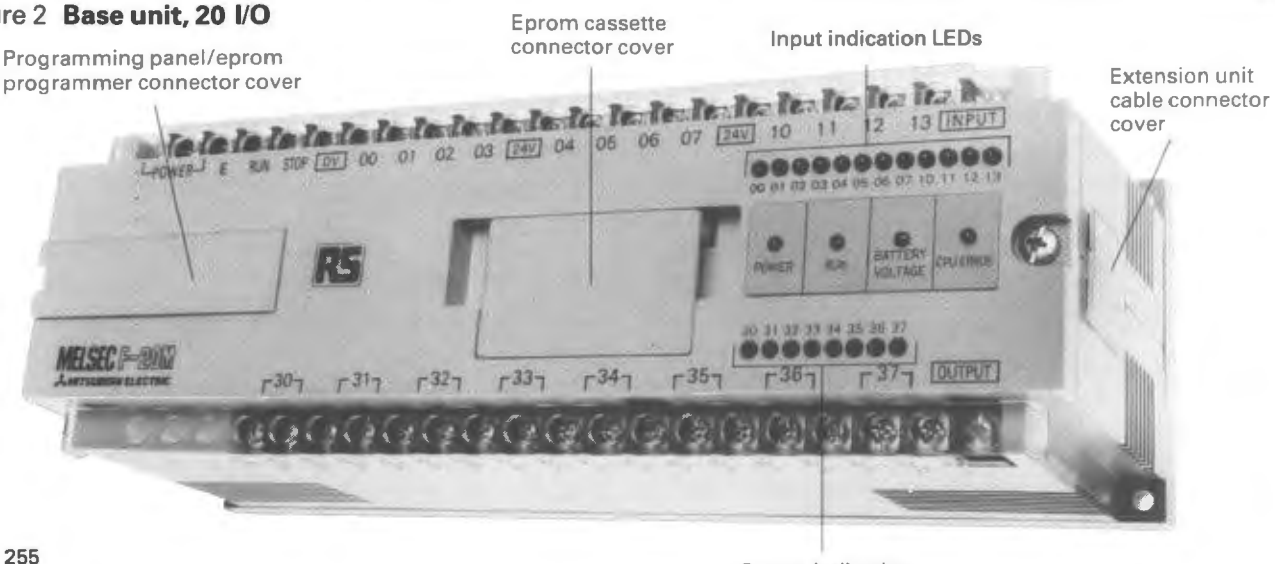
Base unit, 20 I/O (332-745)

Equivalent to Mitsubishi part no. F-20MR-ES1. The base unit is the heart of the PLC system. It contains the central processing unit (CPU), the programme memory and input/output interface devices. Once programmed, it controls the entire operation of the system connected to the PLC input and output points, including those of the extension unit if used.

Features include

- Compact size.
- 12 Opto-isolated input points.
- Integral 24Vdc power supply for energisation of input points.
- 8 Independent, single pole changeover relay outputs with suppressor protected contacts.
- 8 cascadable counters, each with a range of 1-99.
- 8 Cascadable timers, each in the range 0.1 – 99 seconds for use as ON or OFF delay, interval and cyclic timers etc. Cascading of timers and counters for much longer time periods is possible.
- 64 Internal flags (auxiliary relays), including 16 with battery back-up, used for sequence control programmes. Shift registers (each comprising a string of 8 flags) can be formed (see programming section) to implement the required sequence.
- User programme capacity of 320 steps on internal CMOS RAM memory with a 5 year battery back-up. Alternatively the programme may be permanently stored in a non-volatile (EPROM) memory module (RS 332-789) which may be plugged into an integral connector on the base unit.
- LED indication for all input and output states, power supply, operating mode, battery low and CPU error.
- Terminal connections via screw clamps.
- Surface mounting or standard 35mm DIN rail mounting using the DIN rail kit RS 332-795.

Figure 2 **Base unit, 20 I/O**



W. 255
H. 100
D. 80

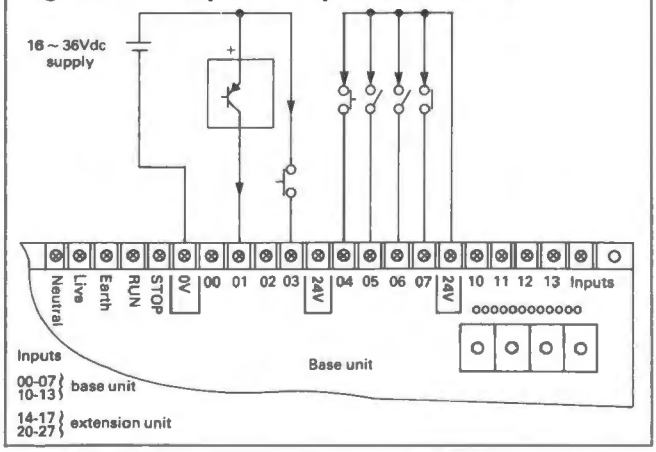
Technical specification

Inputs

Each of the 12 input points, numbered 00 to 07 and 10 to 13 (octal representation) requires 6mA (typ.) at 24Vdc to be turned 'ON'. The integral 24Vdc (200mA) supply can provide input currents via switches, relay contacts, limit switches and other mechanical contacts.

In general sensors with relay outputs or PNP transistor outputs (having OFF state leakage current in the order of 1mA or less) are compatible with the PLC inputs. In addition if the sensor can be powered from 24Vdc, it can be directly energised from the integral PLC supply. However, the current capability of this supply must be considered. External power supplies can be used to energise solid state output devices (see Figure 3), minimum input pulse time 50ms. Some of the RS proximity switches directly compatible with the PLC inputs are as follows:

Figure 3 **Examples of input connections**



Stock number	Description	Total current consumption
304-194	Capacitive proximity switch	14mA
303-703	Diffuse scan optical proximity switch	76mA
302-508	Diffuse scan optical proximity switch	23mA
348-194*	Through scan optical proximity switch	36mA

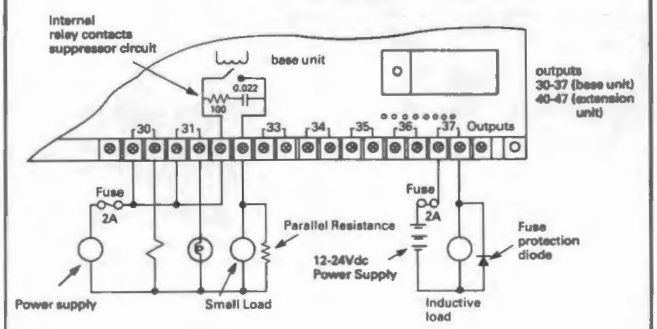
*For use with transmitter 348-201 which requires 40mA if connected to a 24V supply.

Outputs
8 independent, single pole changeover relay outputs (numbered 30-37) rated as shown below:

Resistive load	2A @ 24Vdc/220-240Vac
Inductive load	35VA
Lamp load	100W
Inrush current	10A per cycle
Minimum inductive load	2.3VA
Minimum lamp load	1.5W

For loads in excess of the rated maximum current, external relays or high power transistors should be used to switch the load. For loads below the minimum limits eg. (neons) additional parallel resistance will be needed (it provides a path for the leakage current required by the relay contact suppressor circuit). This current is of the order of 2.4 (1.2)mA at 240 (120)Vac (see Figure 4).

Figure 4 **Examples of output connections**



Other specifications

Mains voltage	220/240Vac
	50/60Hz, 11VA (excluding external loads)
RAM back up	Lithium battery, 5 year life
Programme scan/execution speed	
	50μs/step (average)
Operating temperature	0-55°C
Storage temperature	–15 to 65°C
Relative humidity	95% max.
Insulation resistance (between terminals and earth)	
	5MΩ @ 500Vdc

Input/Output scan
When switched to 'RUN' mode the PLC scans all the inputs and records their states. It then scans the programme and updates the outputs following the newly recorded inputs. This sequence is repeatedly performed. Single scan duration is 16ms (max) depending on programme length. Thus maximum delay time between input status change and output response is 2 scan cycles ie. if the input changed immediately after the PLC has scanned all input states.

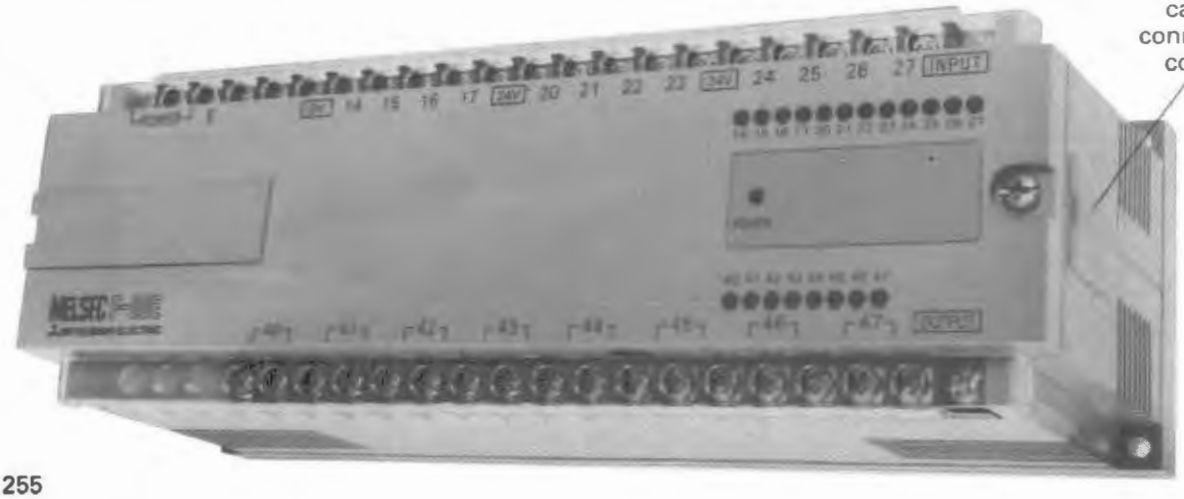
Extension unit, 20 I/O (332-751)

Equivalent to Mitsubishi part no. F-20-ER-ES. This module doubles the input/output capability of the PLC base unit (RS 322-745). Only one extension unit can be used with each base unit.

Features

- 12 inputs and 8 outputs
- On board 24Vdc supply for input requirements.
- Terminal connections via screw clamps.
- Connection to base unit via 300mm long 16 way ribbon cable (supplied) which carries instructions to and feedback from the extension unit. In areas with low electrical noise longer connection leads (up to 1m) may be used. **Note:** ensure cable connectors are fully inserted at both ends (note connector polarization) before switch 'ON'.
- Standard 35mm DIN rail mounting using the DIN rail kit (stock no. 332-795). Surface mounting is also possible using 4 screws (not supplied).
- Dimensionally identical to the base unit.
- LED indication for all inputs, outputs and power supply.

Figure 5 **Extension unit, 20 I/O**



W. 255
H. 100
D. 80

Technical specifications

Inputs and outputs

12 inputs, numbered 14-17 and 20-27 (octal representation) having the same specifications as the base unit inputs. 8 relay outputs, numbered 40-47 with the same specifications as the base unit outputs.

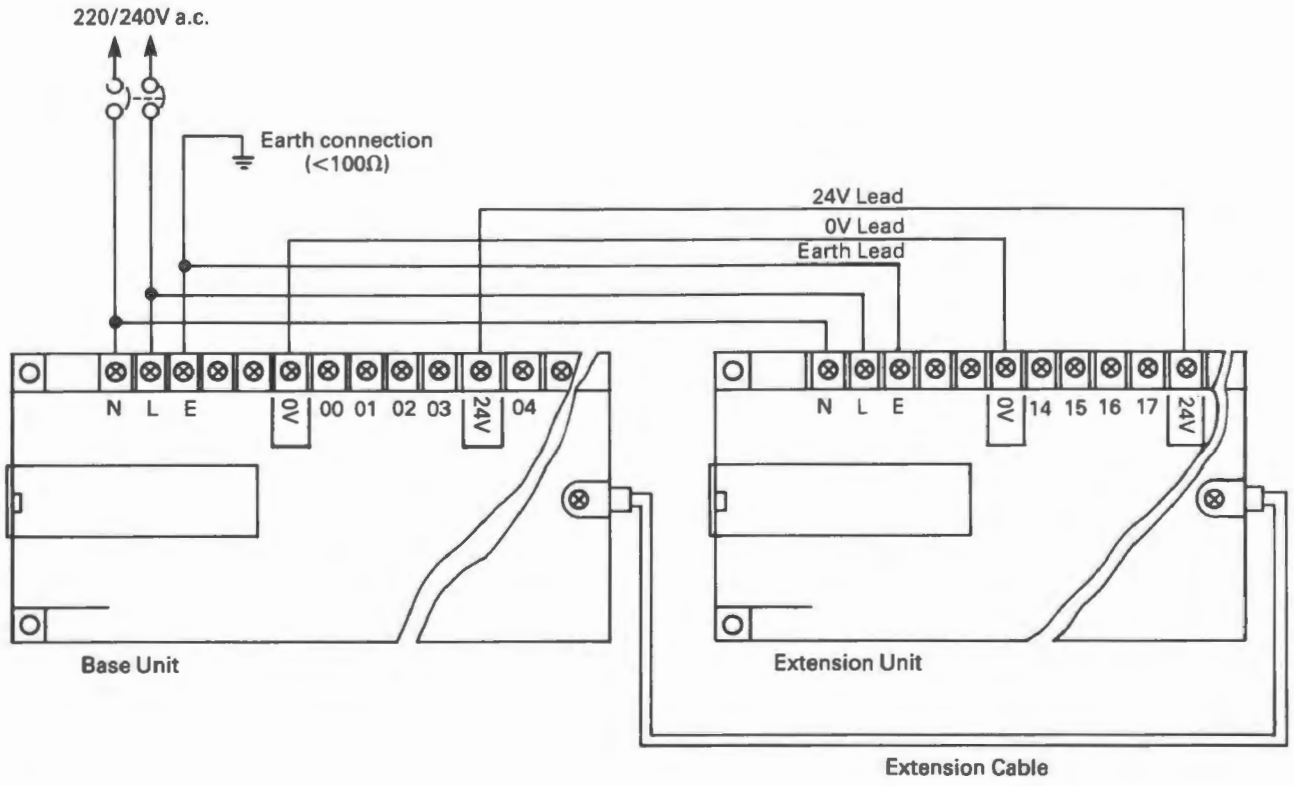
Other specifications as for base unit except:

Power consumption	6VA (excluding external loads)
Programme scan speed	not applicable

It is recommended that each of the input and output leads is no longer than 20m. However particular lead length depends on interference noise levels and acceptable voltage drop.

IMPORTANT: switch the system power supply OFF before interconnecting the PLC elements. The instructions for installation should be properly followed.

Figure 6 **Base and extension unit interconnections**



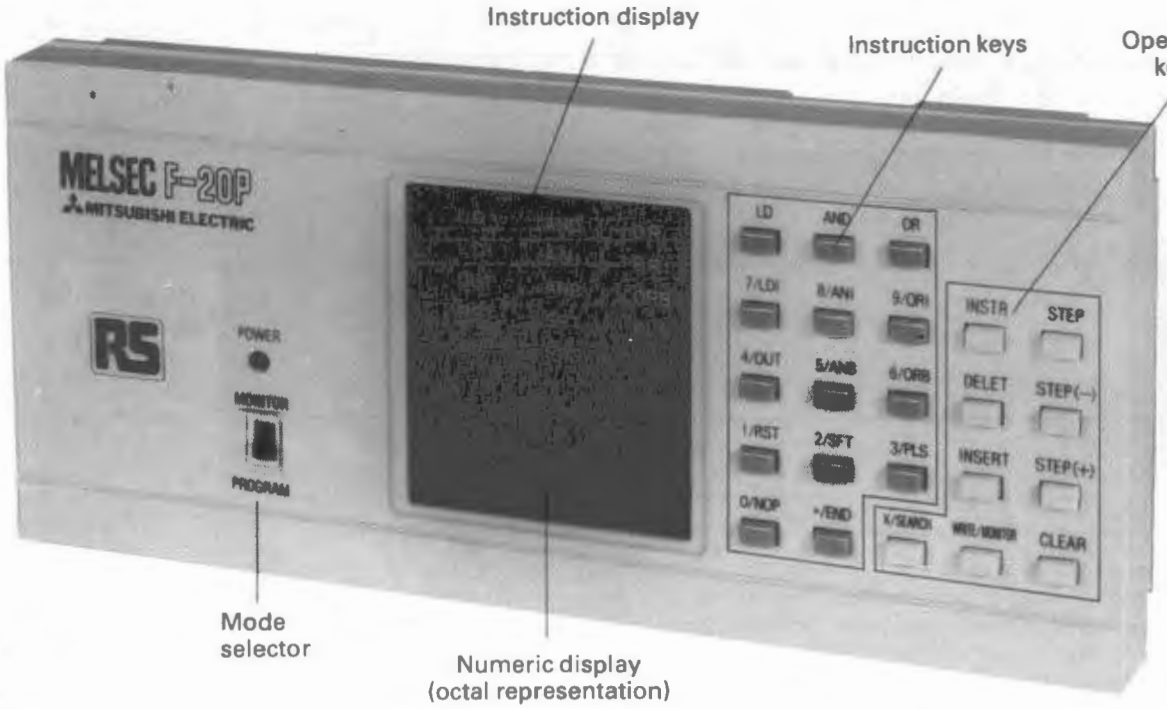
Programming panel (332-767)

Equivalent to Mitsubishi part no. F-20P-E. A light weight, clip-on unit for entering, modifying and monitoring the system programme in the base unit (RAM) memory. If an EPROM memory cassette is fitted onto the base unit, the panel can be used to monitor the programme in ROM.

Features

- Programming keypad.
- Plugs directly onto the base unit – no leads are required.
- LED indication for programme monitoring.
- Panel is removable, ensuring unauthorised programme changes cannot be made.
- Mode selection switch.
- Power 'ON' indicator.
- A single portable panel can be used to programme any number of base units.

Figure 7 **Programming panel**



W. 180
H. 80
D. 20

Connection to base unit

It is recommended that the base unit's power supply is switched off prior to inserting/removing the panel. Remove panel connector cover (see Figure 2). This cover may be held in a recess on the back of the panel. Align the panel feet with their respective recesses on the base unit and plug the panel directly into the base connector. For details of panel use refer to programming section.

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EPROM programmer (332-773)

Equivalent to Mitsubishi part no. F-20MW. This unit clips onto the base unit for the transfer of programmed instructions between the base unit battery backed RAM memory and the non volatile memory on the EPROM cassette (RS 332-789).

Features

- Bidirectional data transfer (EPROM to RAM or RAM to EPROM).
- Comparison of programme data in RAM and EPROM.
- Data transfer error detection and diagnosis.
- Plugs directly into the base unit – no lead required.
- A single portable unit can be used to programme EPROMs on any number of base units.

Figure 8 **Eprom Programmer**

W.225
H. 80
D. 30

Connection to base unit

Switch off the system power supply prior to inserting/removing the programmer. Remove EPROM connector cover (see Figure 2). Remove the system EPROM cassette (supplied) from the programmer and plug it into the base unit. Plug an EPROM cassette, RS 332-789 (blank or user programmed) in place of the system EPROM on the programmer. The latter may now be connected to the base unit in the same way as the programming panel.

Bidirectional data transfer between RAM and user EPROM cassette (not system EPROM) can now be initiated.

EPROM cassette (332-789)

Equivalent to Mitsubishi part no. F-ROM-1. This unit plugs into a special connector port on the base unit. It is programmed using the EPROM programmer RS 332-773 (see above) by transferring data from the RAM in the base unit into the memory IC. Once the fully programmed cassette is plugged in, it overrides the RAM programme in the base unit and controls the system operation. The plugged-in cassette programme can also be monitored using the programming panel (RS 332-745). Different programmes can be stored on various cassettes if required. Thus a system's operation can be quickly changed using a different EPROM cassette. The EPROM may be erased using a suitable UV eraser eg. RS 424-254.

Technical specification

Typical life	100 programme/erase operations
Erase time	42 minutes (minimum) using 6mW/cm² eraser.

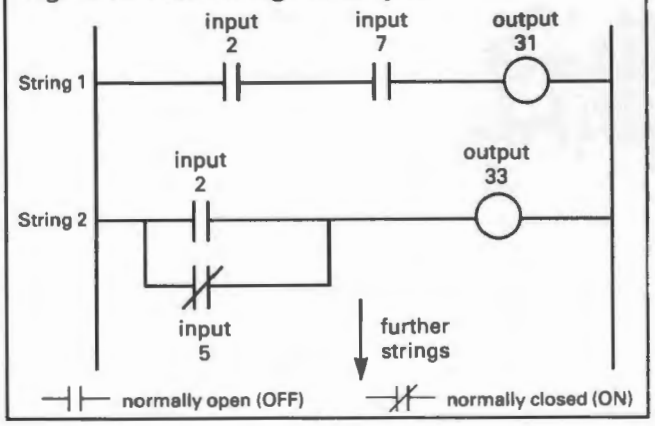
Figure 9 **EPROM cassette**

W.50
D. 31
H. 16

Programming

Programming is the entering and storing of a sequence of instructions in a PLC memory. This memory is normally built into the base unit. Alternatively the programme may be stored on an external memory. The programme is executed by the PLC to control the states of its output relays depending on the conditions of the PLC inputs. These inputs are continuously scanned by the PLC to detect any changes and react accordingly. The RS PLC uses the simple 'ladder logic' programming method. Here a ladder logic diagram is drawn to represent the required operation of the system under control. This diagram is then translated into a sequence of instructions and entered as a programme into the base unit using the programming panel (full programming details are supplied with the programming panel).

Figure 10 **Ladder logic example**



Ladder logic representation of a programme

Starting from the left, string 1 implies an instruction to switch On output 31 only when input 2 AND input 7 are both ON. String 2 instructs the PLC to switch output 33 ON when input 2 is ON OR input 5 is OFF – either condition when satisfied will switch output 33 ON.

Note: inputs and outputs may refer to the 12 inputs and 8 outputs on the PLC base (and extension) units or they may represent the states of counters, timers and internal flags. These elements carry their own assigned and distinguished numbers (see Table 1) examples of implementation of ladder logic diagrams with various elements will be given later.

Table 1 **Numeric assignment (octal representation)**

	base unit	extension unit
Inputs (12)	00-07 10-13	14-17 20-27
Outputs (8)	30-37	40-47
Timers (8)	50-57	
Counters (8)	60-67	
Internal flags (auxiliary relays) without battery back-up (48)	100-107 110-117 120-127 130-137 140-147 150-157	
Internal flags with battery back-up (16)	160-167 170-177	
Special function** auxiliary relays (5)	70, 71, 72 76, 77	

**

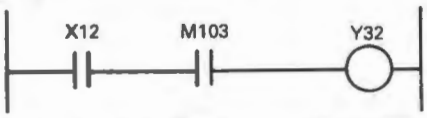
The special auxiliary relays have the following functions:

70 Permanently ON when the unit is in 'RUN' mode.
71 Introduces a single pulse when the PLC is switched to 'RUN' mode.
72 Provides a continuous pulse train to any selected output. Pulse width is 50ms with 50ms space between pulses ie. 10 pulses per second.
76 Indicates when the battery power is running low.
77 The activation of relay 77 in a programme causes all outputs to be switched off.

To avoid confusion when ladder logic diagrams are being drawn, it is recommended that the following letters should accompany the numeric assignment of each element.

Element type	Letter
Input terminal	X
Output relay	Y
Timer	T
Counter	C
Auxiliary relay	M

Thus

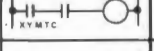
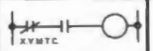
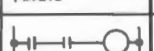
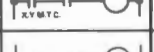
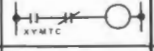
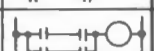
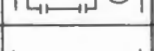
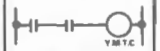


represents an instruction to switch output relay 32 ON when input 12 and auxiliary relay 103 are both ON.

Ladder logic diagram implementations

To convert the ladder diagram into instructions acceptable by the PLC, the programming panel is equipped with a set of instruction keys. Together with the numeric assignments of the various elements in the diagram these instructions form the PLC programme corresponding to the original ladder diagram. Table 2 shows the application of each instruction key. Letters X, Y etc. underneath certain elements represent the allowable types of operable instructions for that element (ie. inputs, outputs, counters etc.)

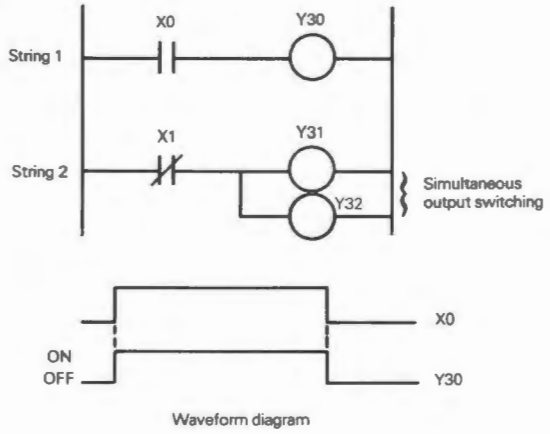
Table 2 **Programming**

Key	Function	Application	Description
LD	load		Start the branch with a normally open contact.
LDI	load inverse		Start the branch with a normally closed contact.
AND	AND		Connect a normally open contact in series.
ANI	AND inverse		Connect a normally closed contact in series.
OR	OR		Connect a normally open contact in parallel.
ORI	OR inverse		Connect a normally closed contact in parallel.
ANB	AND block		Series connection of branch circuit with the previous one.
ORB	OR block		Parallel connection of branch circuit with previous one.
OUT	output		Output on output relay, auxiliary relay, timer or counter.
RST	reset memory & counter		Reset of counter, shift register.
SFT	shift memory		Shift (on shift register).
PLS	pulse generate		Positive pulse output on auxiliary relay.
NOP	no process		No process (Empty step location)./Jump Instruction (Skip some programme).
END	end		End of programme

Examples of converting various ladder diagram configurations into PLC programme instructions using the programming panel keypad are given as follows (additional configurations are available in the manual supplied with the programming panel).

Examples

1. LD, LDI, OUT

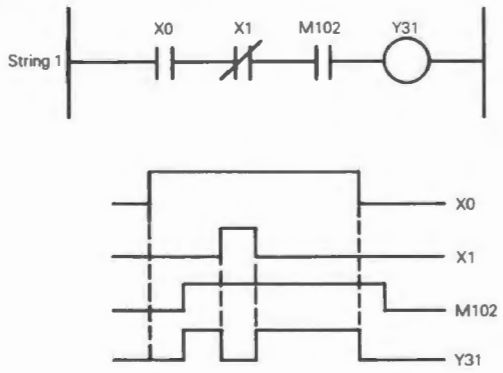


String 1 implies output 30 (relay) turns ON when input 0 is ON. String 2 implies outputs 31 and 32 (relays) turn ON when input 1 is OFF. The output element(s) in a particular string can subsequently be entered as input(s) in other parts of the ladder diagram. The corresponding instruction set for the above diagram is:

	step	instruction	element
String 1	0	LD	0
	1	OUT	30
	2	LDI	1
String 2	3	OUT	31
	4	OUT	32

It is advisable when forming the instruction set to follow the same string order as the ladder diagram. Note: Step No. is only to indicate the programme order and size and is not physically entered via the programming panel.

2. AND, ANI (AND INVERSE)

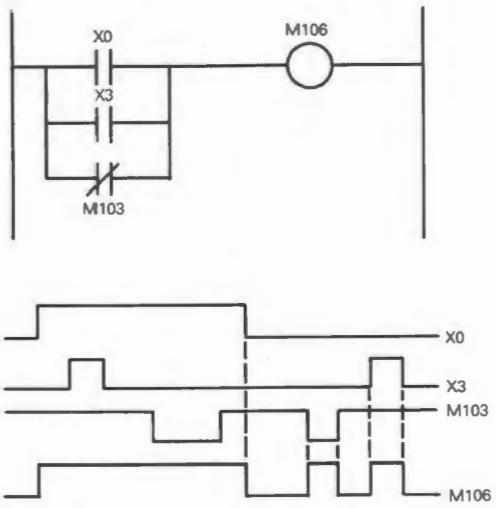


String 1 implies output 31 (relay) turns ON when input 0 is ON, input 1 is OFF and auxiliary relay 102 is ON.

Equivalent instructions

step	instruction	element
0	LD	0
1	ANI	1
2	AND	102
3	OUT	31

3. OR, ORI (OR INVERSE)



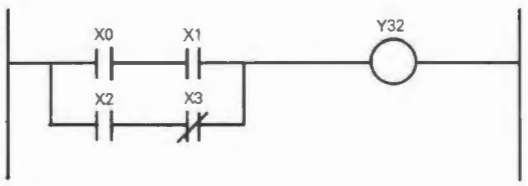
This implies auxiliary relay 106 is ON when input 0 is ON or input 3 is ON, or auxiliary relay 103 is OFF ie. any one or more of these input conditions will turn the output ON.

Equivalent instructions

step	instruction	element
0	LD	0
1	OR	3
2	ORI	103
3	OUT	106

4. ORB (OR BRANCH)

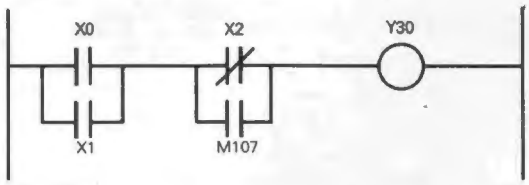
Connects two branches in parallel



Equivalent instructions

step	instruction	element
0	LD	0
1	AND	1
2	LD	2
3	AN1	3
4	ORB	–
5	OUT	32

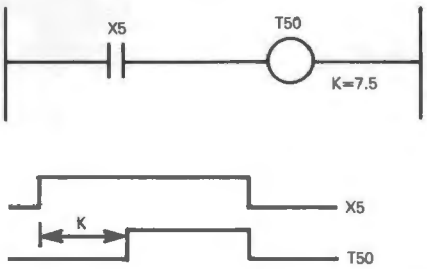
5. ANB (AND BRANCH)
Connects two groups in series



Equivalent instructions

step	instruction	element
0	LD	0
1	OR	1
2	LDI	2
3	OR	107
4	ANB	–
5	OUT	30

6. Setting a timer



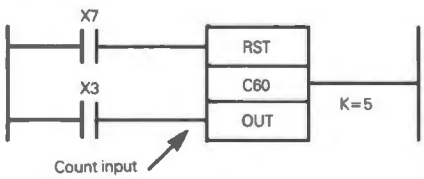
Implies that when input 5 turns ON the output of timer 50 turns ON after 7.5 seconds (K=7.5).

Equivalent instructions

step	instruction	element
0	LD	5
1	OUT	50
2	K	7.5

The value of K can be set within 0.1 – 9.9 in 0.1 second increments or 1-99 in 1 second increments. The timer output resets if the input is switched OFF. Timer cascading with other timers and counters is possible.

7. Setting a counter

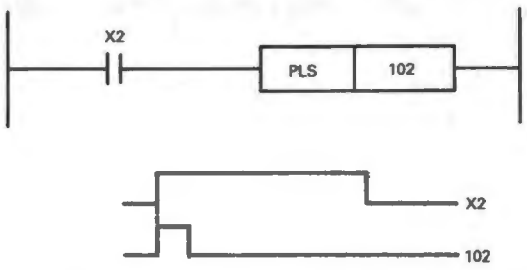


A positive pulse on X7 resets counter 60 to OFF state. If 5 positive pulses (or OFF to ON transmissions) appear on X3 the counter output turns ON (K=5). Any changes on X3 are disregarded as long as X7 is ON.

Equivalent instructions

step	instruction	element
0	LD	7
1	RST	60
2	LD	3
3	OUT	60
4	K	5

8. PLS (PULSE)
Introduces a positive pulse onto an auxiliary relay.

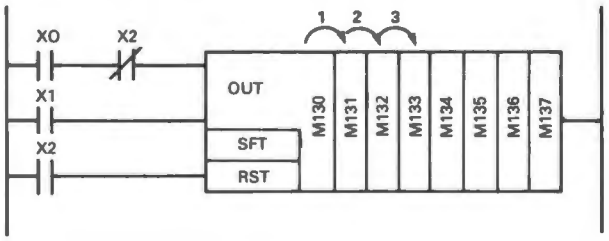


Whenever input 2 turns ON a positive pulse is generated on auxiliary relay 102. This pulse can feed internally elsewhere eg. to reset a counter. Pulse width equals one programme execution cycle time. (32ms max.).

Equivalent instructions

step	instruction	element
0	LD	2
1	PLS	102

9. SFT (SHIFT)
This instruction applies to a shift register which is a block of 8 auxiliary relays with consecutive numbers starting with a 3 digit multiple of 10 ie. 100-107, 110-117 . . . up to and including 170-177.



step	instruction	element
0	LD	0
1	ANI	2
2	OUT	130
3	LD	1
4	SFT	130
5	LD	2
6	RST	130

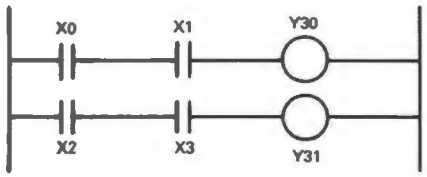
The ladder diagram implies that when input 2 is OFF M130 has the same state as input 0. Input 1 is the shift input and every time this input switches ON (or pulsed) the original state of M130 advances one step through the register until it 'drops off' or feeds through to another element. If input 1 continues to be clocked any subsequent changes on input 0 (ie. M130) will similarly advance through the register.

This facility is used in sequence control applications by utilising the auxiliary relay states to control various output devices. Input 2, when turned ON, resets the shift register (ie. turns OFF all the auxiliary relays) and shift pulses are not accepted whilst input 2 is ON.

Note: shift register cascading is possible for longer sequence requirements.

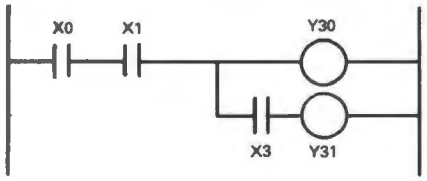
10. NOP (NO OPERATION)

This instruction produces a blank programme step which the PLC scans without taking any action. If this instruction replaces another programme instruction it can change the programme flow eg.:



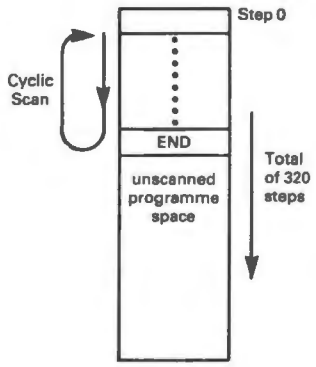
instruction	element
LD	0
AND	1
OUT	30
LD	2
AND	3
OUT	31

Should LD2 be replaced by 'NOP' instruction ie. 'rubbed off'. The resulting ladder diagram is:



End

This instruction terminates the programme. When not used the PLC scans the full programme space (320 steps) regardless of the programme length. However if 'END' is used the PLC will only scan and execute the programme portion up to the 'END' position thus increasing the speed of the PLC response to fast I/O changes.



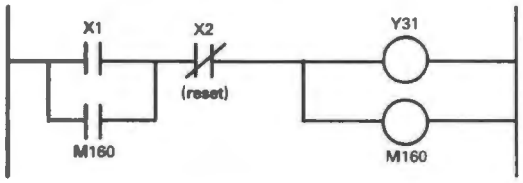
Operation keys

In addition to the instruction keypad, the programming panel is equipped with 9 distinguished operation keys used to easily and quickly enter, delete, modify and monitor the complete or part programme.

Useful circuit examples

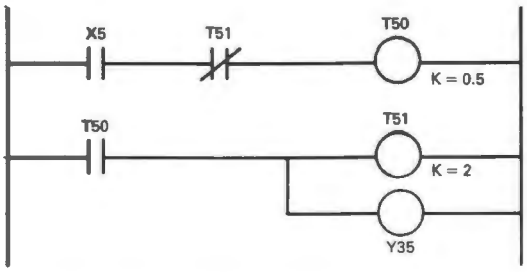
Some common circuit programmes are shown below.

1. Latching circuit with reset



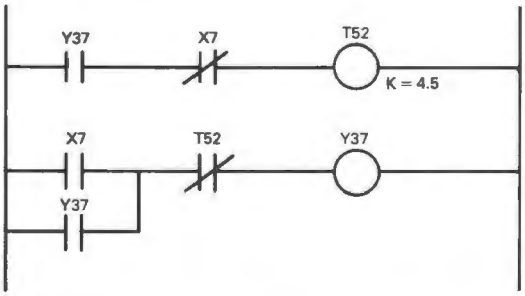
The outputs Y31 and M160 will be switched ON as soon as input 1 is turned ON (providing X2 is OFF). The outputs remain ON even if X1 is turned OFF. When X2 is turned ON it forces the outputs to switch OFF.

2. Cyclic timer



While input X5 is ON, output Y35 continues to cyclically turn ON for 2 seconds and OFF for 0.5 seconds. ON and OFF periods can be set to a minimum of 0.1 seconds. Considerably longer periods can be achieved by timer/timer (or counter/timer) cascading.

3. Delay on de-energise

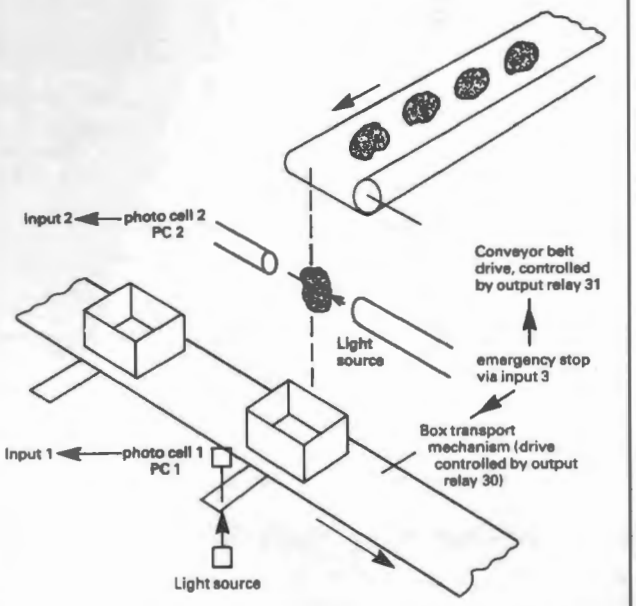


Output Y37 immediately follows input X7 on switch ON but when input X7 is turned OFF output Y37 remains energised for 4.5 seconds before switching OFF.

Typical control application

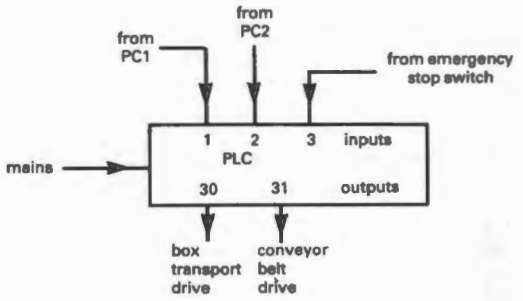
This example shows how the RS PLC can be used to control a conveyor belt system as in Figure 11.

Figure 11 **Conveyor belt system control example**



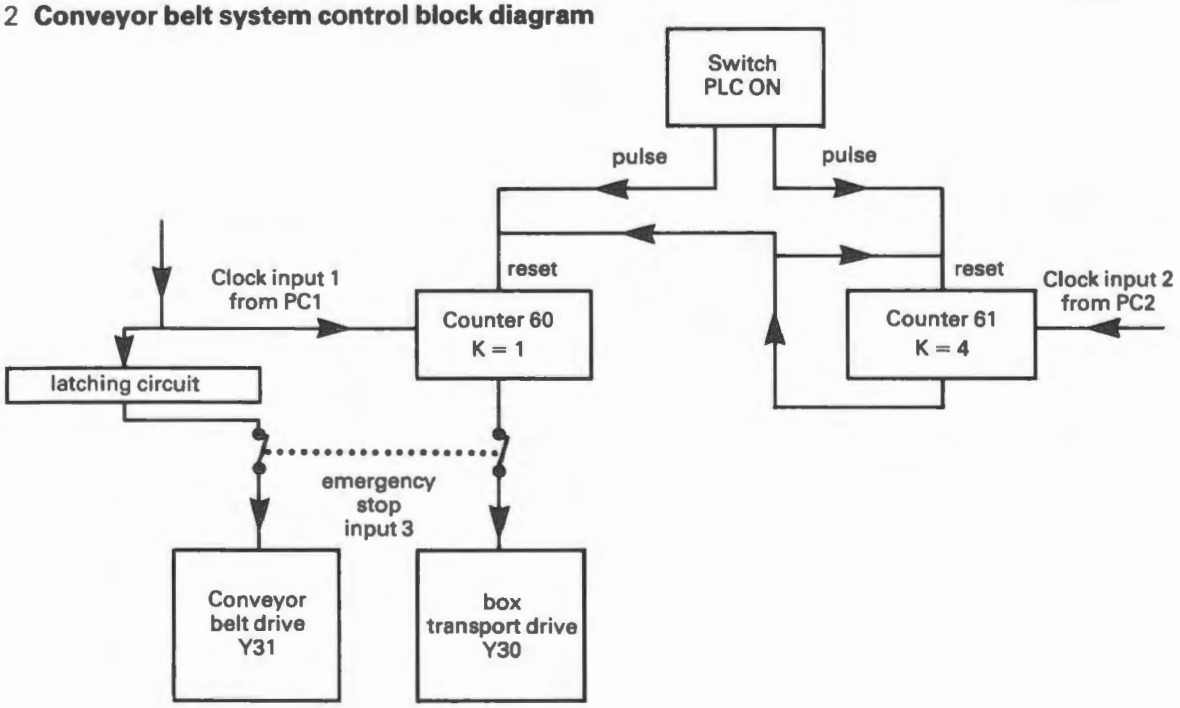
The PLC task is to initially move the box transport mechanism (low inertia assembly) until the first box is directly underneath the conveyor belt roller.

The PLC is then to start the conveyor belt and when 4 items fall into the box it is to be swiftly replaced by another empty box with the conveyor belt still moving (assuming sufficient time between the production items falling into the box). This process is to continue until the system is turned OFF. In addition, the two drive mechanisms are to have a common emergency stop switch. In order to programme the PLC for controlling this system all the inputs and outputs used must be assigned. In this example the following connections are chosen.



Before programming it is useful to draw a block diagram to represent the detailed system operation and then convert this into a ladder logic diagram, which can be translated into programme instructions. For the conveyor belt system the block diagram is shown in Figure 12.

Figure 12 **Conveyor belt system control block diagram**

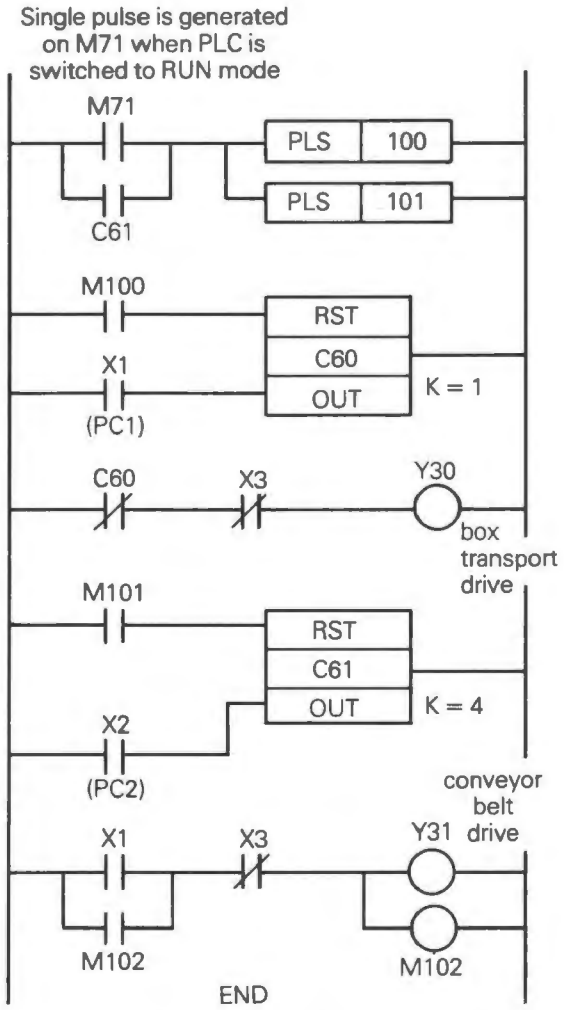


When the PLC is switching ON two pulses are generated, one resets counter 61, the other resets counter 60 and starts the box transport drive until PC1 detects the correct positioning of a box and increments C60 (to the specified K value) which turns the box transport OFF. At the same time the conveyor belt starts moving and PC2 detects the production items falling into the box. When four of these have dropped, counter C61 resets C60 thus starting the box transport again, and at the same time C61 resets itself ready to count the next four items.

The flow chart can now be converted into a ladder logic diagram and the actual programme can also be listed as shown in Table 3.

RS data

Table 3 **Ladder logic diagram for conveyor belt system**



1	LD	71	generates reset pulses after switch ON and whenever four production items fall into a box
2	OR	61	
3	PLS	100	
4	PLS	101	
5	LD	100	moves box transport until photo cell or emergency switch 3 stops the mechanism.
6	RST	60	
7	LD	1	
8	OUT	60	
9	K	1	
10	LD1	60	
11	ANI	3	
12	OUT	30	
13	LD	101	when four items fall into a box. This part resets counter 61 which in turn resets counter 60 thus restarting box transport mechanism
14	RST	61	
15	LD	2	
16	OUT	61	
17	K	4	
18	LD	1	Latching circuit which maintains the belt drive 'ON' after the 1st signal from PC1 (unless reset by the emergency switch 3)
19	OR	102	
20	ANI	3	
21	OUT	31	
22	OUT	102	
23	END		

Note: the length of the programme (terminated by 'END' instruction) determines the frequency at which the PLC scans the programme (31 cycles/second for a 320 step programme). The shorter the programme the faster the scan – resulting in a faster response to varying input/output conditions.

Important: if the PLC is programmed to control a particular plant or assembly, it is essential to check that the required control sequence can be correctly achieved by simulating the input and output conditions and testing the entire programme before connecting the PLC to the actual system requiring control.

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RS data

LED Flasher, oscillator, trigger or alarm. RS3909

Stock number 300-372

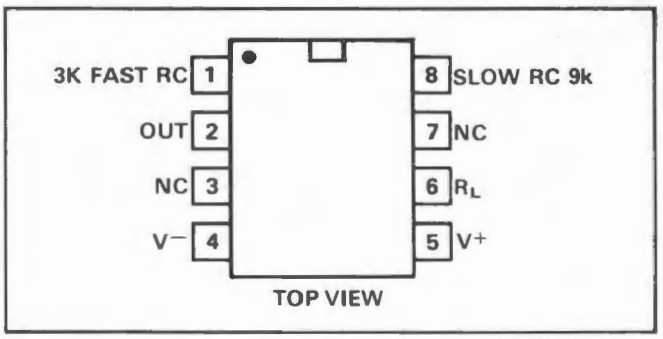
The RS3909 is a simple to use monolithic relaxation oscillator which, by using the voltage developed across the timing capacitor for voltage boost can flash LEDs whilst running from a supply as low as 1.4Vdc. It is optimised for lower power drain and will typically operate from one alkaline C size cell for 15 months. Application is made simple by inclusion of internal timing resistors optimised for 1.5V and 3Vdc operation requiring the addition of only a battery and capacitor to function as an LED flasher. Different configurations allow use as a sawtooth generator or direct 8Ω speaker oscillator driver.

Features

- Operates for over one year from one C size alkaline cell
- Bright, high current LED pulse
- Minimum external parts
- Very versatile
- Low voltage operation, from just over 1V to 5V
- Low current drain, averages under 0.5mA during battery life
- Powerful; as an oscillator directly drives an 8Ω speaker
- Wide temperature range

Absolute Maximum Ratings

Power dissipation ____ 500mW
V^+ voltage ____ 6.4V
Operating temperature range ____ −25°C to +70°C



Electrical characteristics

Parameter	*Condition	Min	Typ	Max	Units
Supply voltage	(In oscillation)	1.15		6.0	V
Operating current			0.55	0.75	mA
Flash frequency	300μF, 5% capacitor	0.65	1.0	1.3	Hz
High flash frequency	0.30μF, 5% capacitor		1.1		kHz
Compatible LED forward drop	1mA forward current	1.35		2.1	V
Peak LED current	350μF capacitor		45		mA
Pulse width	350μF capacitors at ½ amplitude		6.0		ms

*V^+ = 1.4V
T_{amb} = 25°C
$V_{(LED)}$ = 1.5V to 1.7V

Introduction

Most linear integrated circuits are designed to operate with power supplies of 4.5 to 40V. Practically no battery/portable equipment is provided with indicator lights due to unacceptable power drain. Even LEDs won't light from a 1.5V battery, and would drain the common 9V radio battery in a few hours. The RS3909 changes all this, obtaining long life from a single 1.5V cell.

Sufficient voltage for flashing a light emitting diode is generated with cell voltage down to 1.4V. In such low duty cycle applications batteries will last for months to years of continuous operation. Such flasher circuits then become practical for marking the locations of flashlights, emergency equipment, and boat mooring floats in the dark.

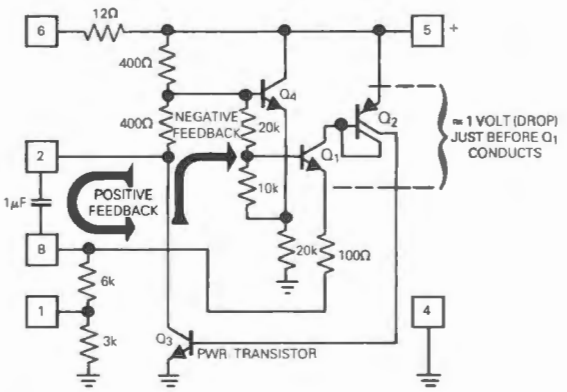
The RS3909 is simple in design, easy to use, and includes extra resistors to minimise external cir-

cuitry and the size of the completed flasher or oscillator.

Circuit operation

The circuit in Figure 1 shows the RS3909 connected as the simplest type of oscillator. Ignoring the capacitor for a moment, and assuming 1.5V on pin 5, current will flow in the 3k and 6k timing resistors through the emitter of Q_1. This current will be amplified approximately three times by Q_2 and passed to the base of Q_3. Q_3 will then conduct, pulling down on the base of Q_4 and hence the base of Q_1. This is a negative feedback since it will reduce timing resistor current and current to the power transistor's base until a balance is reached. This will occur with the collector of Q_3 about 0.5V, the base of Q_4 at about 1V, and a very small voltage from pin 8 to ground. The difference between these two voltages is the base-emitter drop of Q_1 and ⅔ the base-emitter drop of Q_4 as set by the high resistance divider from its base to emitter.

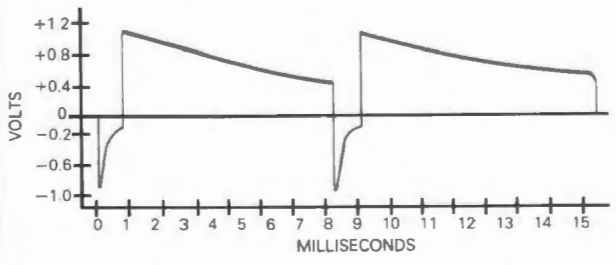
Figure 1 **The basic oscillator**



Note that negative feedback *voltage* is attenuated by at least a factor of 2 due to the divider of two 400Ω resistors. Now considering the capacitor, its positive feedback factor is initially unity. Therefore the dc bias condition and the temporary excess positive feedback conditions are met and the circuit must oscillate.

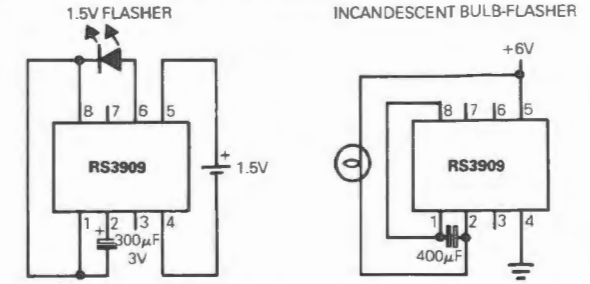
The waveform at pin 8 of the above oscillator is shown in Figure 2. The waveform at pin 2, the power transistor collector, is almost a rectangle. It extends from a saturation voltage of 0.1V or less to within about 0.1V of the supply voltage. The 'on' period of course coincides with the negative pulses at pin 8. Other circuit voltages can easily be inferred from these two waveforms.

Figure 2 **Waveforms at pin 8**



The simplicity of LED and incandescent pilot lamp flashers is illustrated below. In the LED flasher, the RS3909 uses the single capacitor for both timing and voltage boosting.

Figure 3 **Two simple flashers**

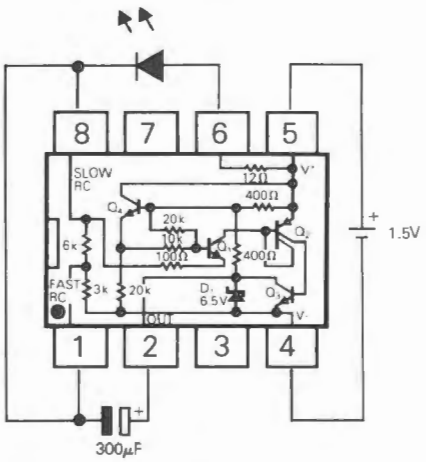


The RS3909, although designed as an LED flasher, is ideal for other applications such as a high current, trigger pulse generator for SCRs and Triacs. The frequency of oscillation adjusts from under 1Hz to hundreds of kHz. Waveshape can be set from pulses a few μs wide to approximately a square wave.

Circuit description

The circuit of Figure 4 again shows the typical 1.5V LED flasher, but with the internal circuitry of the IC illustrated.

Figure 4 **Circuit operation**



The flasher achieves minimum power usage in two ways. Operated as above, the LED receives current only about 1% of the time. The rest of the time, all transistors but Q_4 are off. The 20k resistor from Q_4's emitter to supply-common draws only about 50μA. The 300μF capacitor is charged through the two 400Ω resistors connected to pin 5 and through the 3k resistor connected to pin 4 of the circuit.

Transistors Q_1 through Q_3 remain off until the capacitor becomes changed to about 1V. This voltage is determined by the junction drop of Q_4, its base-emitter voltage divider, and the junction drop of Q_1. When voltage at pin 1 becomes a volt more negative than that at pin 5 (the supply positive terminal) Q_1 begins to conduct. This then turns on Q_2 and Q_3.

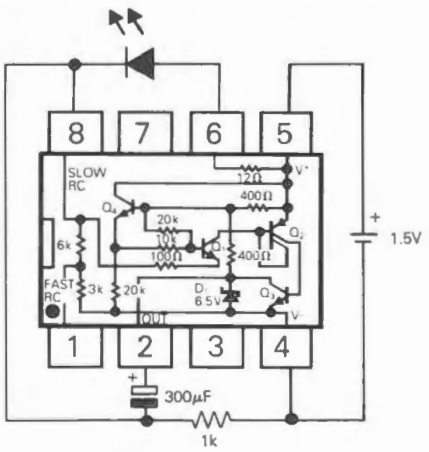
The RS3909 then supplies a pulse of high current to the LED. Current amplification of Q_2 and Q_3 is between 200 and 1000. Q_3 can handle over 100mA and rapidly pulls pin 2 close to supply common (pin 4). Since the capacitor is charged, its other terminal at pin 1 goes *below* the supply common. The voltage at the LED is then higher than battery voltage, and the 12Ω resistor between pins 5 and 6 limits the LED current.

Many of the other oscillator circuits work in a similar fashion. If voltage boost is not needed (with or without current limiting) loads can be hooked between pins 2 and 6 or pins 2 and 5.

Applications: flasher and indicator

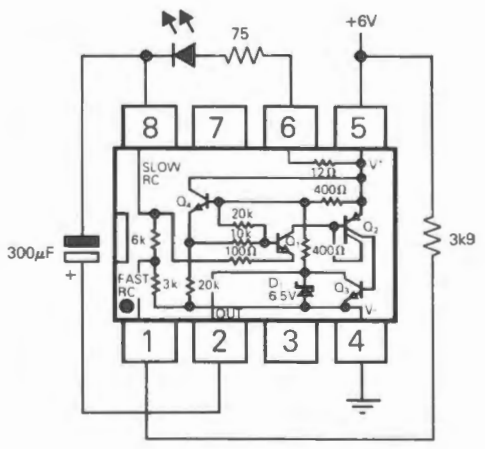
Differing uses and supply voltages will require adjustment of flashing rates. Often it is convenient to leave the capacitor the same value to minimise its size, or to fix the pulse energy to the LED. First, the internal RC resistors can be used to obtain 3k, 6k, or 9k by connecting to or shorting the appropriate pins. Further adjustment methods are shown in the two parts of Figure 5.

Figure 5a **Fast flasher**



In Figure 5a it can be seen that the internal RC resistors are shunted by an external 1k between pins 8 and 4. This will give a little over 3 times the flashing rate of the typical 1.5V flasher of Figure 3.

Figure 5b **6 volt flasher**

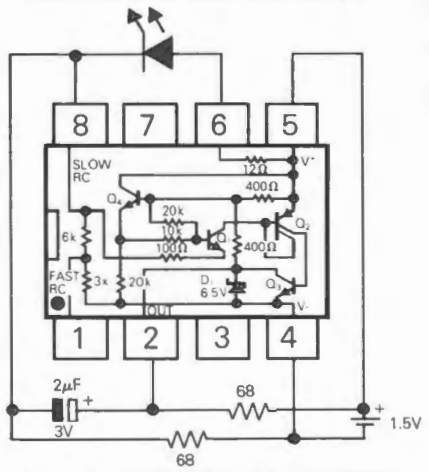


The 3.9k resistor in Figure 5b connected from pin 1 to the 6V supply raises the voltage at the bottom of the 6k RC resistor. Charging current through that resistor is greatly reduced, bringing flashing rate down to about that of the 1.5V circuit (1Hz). As will be explained later, this biasing method also ensures the start of oscillation even under unfavourable conditions.

Two precautions are taken for circuit reliability. The added 75Ω series resistor for the LED keeps current peaks within safe limits for the diode and IC. Also, in operation above a 3V supply, the electrolytic capacitor sees momentary voltage reversals. It should be rated for periodic reversals of 1.5V.

A continuously appearing indicator light can also be powered from a single 1.5V cell. Duty cycle and frequency of the current pulses to the LED are increased until the average energy supplied provides sufficient light. At frequencies above 2kHz, even the fastest movement of the light source or the observer's head will not produce significant flicker.

Figure 6 **Continuous 1.5V indicator**



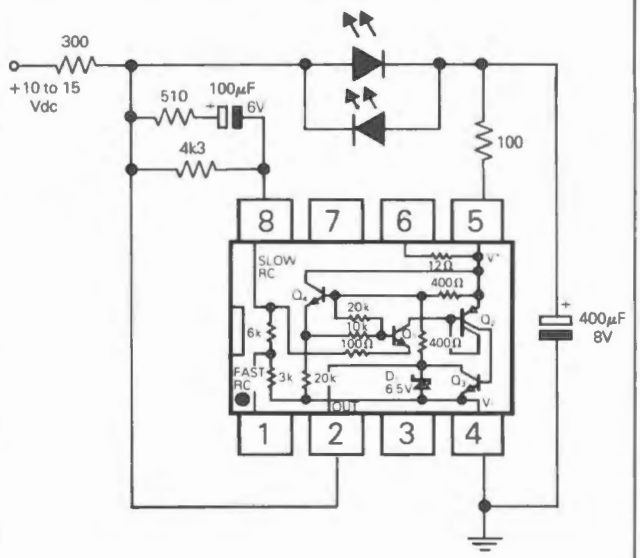
Since this indicator powering circuit uses the smallest capacitor that will reliably provide full output voltage, its operating frequency is well above the 2kHz point. The indicator is not, however, intended as a long life system, since battery drain is about 12mA.

High frequency operation requires the addition of two external resistors, typically of the same value. One shunts the high internal timing resistors. If this was the only one used, the capacitor charging current would have to pass through the two 400Ω resistors internally connected between pin 5 and the collector of Q_3. Oscillation at a slower rate and lower duty cycle than desired would occur, and oscillation might cease altogether before the battery was full discharged. The second 68Ω resistor shunting the two 400Ω resistors eliminates this possibility.

The circuit of Figure 7 is a relaxation type oscillator flashing 2 LEDs sequentially. With a 12Vdc supply, repetition rate is 2.5Hz. C_2, the timing and storage capacitor, alternately charges through the upper LED and is discharged through the other by the IC's power transistor Q_3.

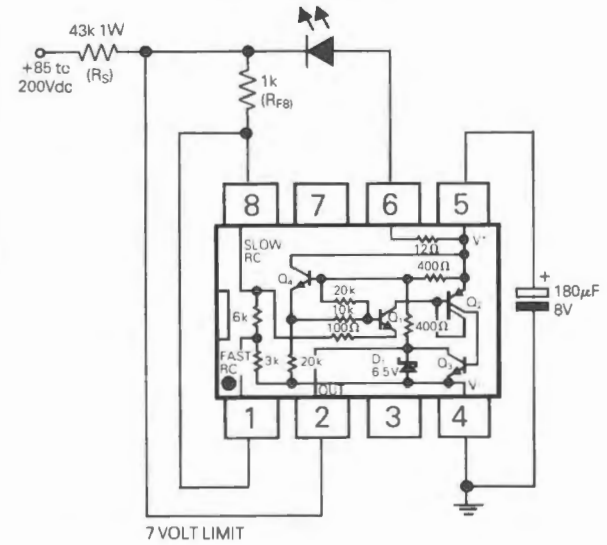
If a red/green flasher is desired, the green LED should have its anode or positive lead towards pin 5 (like the lower LED). A shorter but higher voltage

Figure 7 **Alternating flasher**



pulse is available in this position. A bi-colour LED may be substituted for the individual LEDs if desired.

Figure 8 **High voltage flasher**



Typical operating conditions

V+	Flash Hz	C_r	R_S	R_{FB}	V^+_{RANGE}
6V	2	400µF	1k	1.5k	5-25V
15V	2	180µF	3.9k	1k	13-50V
100V	1.7	180µF	48k 1W	1k	85-200V

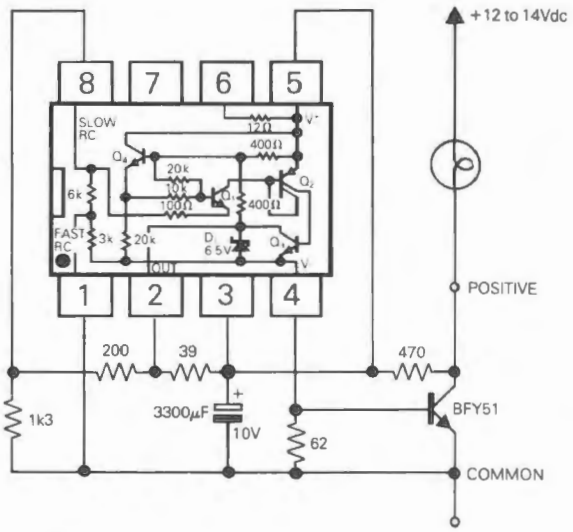
Indication or monitoring of a high voltage power supply at a remote location can be done much more safely than with neon lamps. If the dropping resistor (43k as in Figure 8) is located at the source end, all other voltages on the line, the IC, and the LED will be limited to less than 7V, above ground.

The timing capacitor is charged through the dropping resistor and the two 400Ω collector loads between pins 2 and 5 of the IC. When capacitor voltage reaches about 5V, there is enough voltage across the 1k resistor (to pin 8) to turn on Q_1, and hence trigger on the whole IC to discharge the capacitor through the LED.

Incandescent bulbs can also be flashed, as already illustrated in Figure 3. However, most such bulbs draw more than 150mA which exceeds the limit of the RS3909. The following circuit therefore uses an added power transistor rated at 1A or more. In the circuit, an NPN transistor is used, so the power transistor's base drive is obtained from the common or ground pin of the flasher IC.

Figure 9 shows a high power application such as would use a car battery for power. It provides about a 1Hz flash rate and powers a lamp drawing a nominal 600mA.

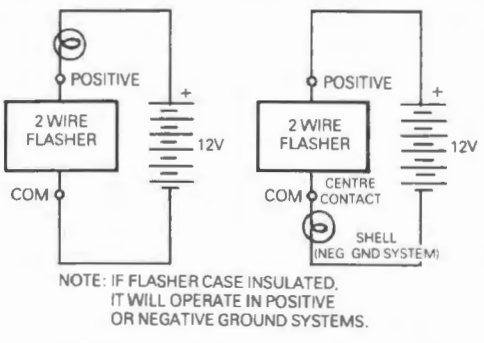
Figure 9 **12 volt flasher (2 wire)**



A particular advantage of this circuit is that it has only 2 external wires and thus may be connected in either of the two ways shown below in Figure 10. Further, no circuit failure can cause a battery drain greater than that of the bulb itself, continuously lit.

In the circuit of Figure 9 the 3300µF capacitor performs a number of other functions. It makes the RS3909 immune to supply spikes, and provides the means of limiting the IC's supply voltage. Since the

Figure 10

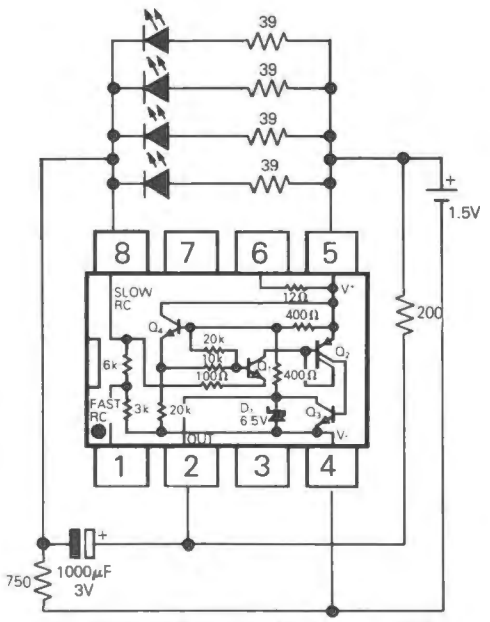


RS3909 can only operate with 7.5V or less on pin 5 (in this circuit) the 200Ω/1.3k divider attached to pin 8 of the IC causes it turn fully on at 7V or less on pin 5. Then the RS3909 discharges the timing capacitor (its own supply voltage) to 4V or less, whereupon it turns off. The capacitor discharge

current comes out of pin 4 of the IC, turning on the BFY51 transistor. It is the large size of the timing capacitor that allows it to *store* all the needed energy for turning on the power transistor. This in turn permits the whole flasher circuit to operate as a 2 wire device.

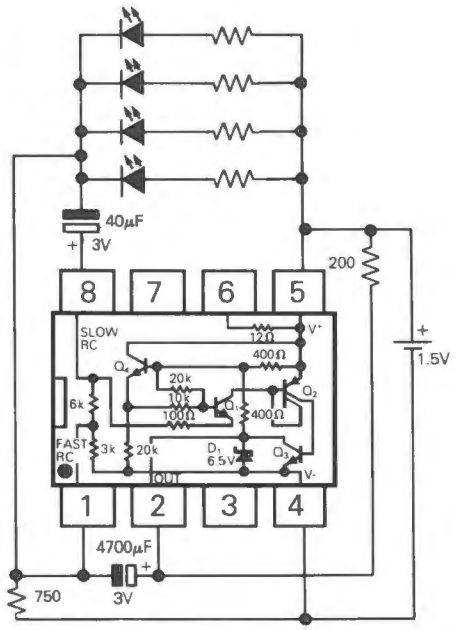
Many other flasher possibilities exist. LED flash rate can be varied from 0 to 20Hz, or a number of LEDs may be flashed in parallel as shown in Figures 11 and 12. With a 3V supply, yellow and green LEDs may be flashed. A 6V incandescent 'emergency lantern' can be made and its bulb may be made to give continuous light or flash by switch selection. This is a more reliable, longer life system, than a lantern with a second thermal flasher bulb. The RS constant current LED makes possible flashing many LEDs in parallel or with high voltages without series resistors.

Figure 11 **4 parallel LEDs**



NOTE: Nominal flash rate 1.3Hz, Average I_{DRAIN} = 2mA

Figure 12 **High efficiency parallel circuit**



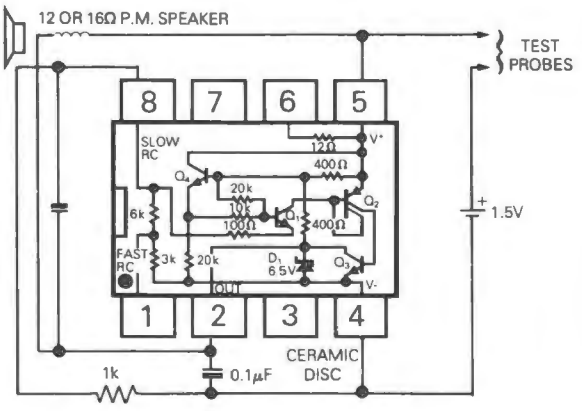
NOTE: Nominal flash rate: 1.5Hz, average I_{DRAIN} = 1.5mA

Applications: audio and oscillator

Very economical continuity checkers, tone generators, and alarms may be made from the RS3909. No matching transformer is needed because the 150mA capability of the RS3909 output can drive many standard permanent magnet (transistor radio) loudspeakers directly. The 1.5V battery used in most applications is both lower in cost and longer lasting than the conventional 9V battery.

In the continuity checker of Figure 13, a short, up to about 100Ω, across the test probes provides enough power for audible oscillation. By probing 2 values in quick succession, small differences such as between a short and 5Ω can be detected by differences in tone.

Figure 13 **'Buzz-box' continuity and coil checker**

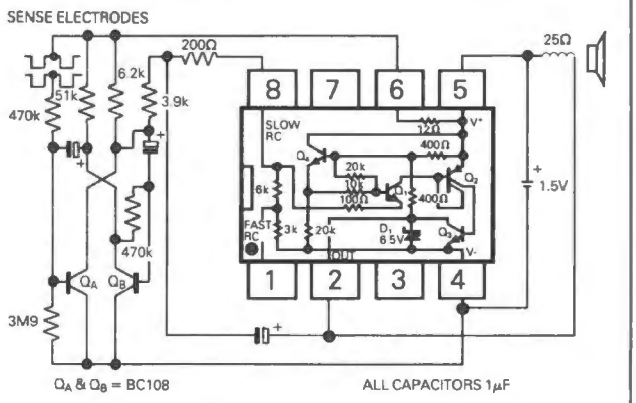


A novel use of this circuit is found in setting the ignition timing of certain types of petrol engine. This is due to the difference in tone that can be heard from the tester depending whether a short circuit is present or not across the low resistance

primary of the ignition coil. In other words, the difference between a 1Ω resistor and a 1Ω inductor can be heard. Quick checks for short and open circuits in transformers and motors can therefore be made.

Darkrooms, laundry rooms, laboratories, and cellar workshops can often suffer damage from spills or water seepage ruining wooden fittings, chemicals, fertilizers, bags of dry concrete, etc. The circuit of Figure 14 is safe on potentially damp floors since

Figure 14 **Water seepage alarm**



there is no connection to the power line. Further, its standby battery drain of 100μA yields a battery life close to shelf life.

Without moisture, multivibrator transistor Q_a is completely off, and its collector load (7.2k) provides enough current to hold pin 8 of the RS3909 above 0.75V where it cannot oscillate. When the sense electrodes pass about 0.25μA due to moisture, Q_a starts turning on, and since Q_b is already partially biased on, positive feedback now occurs. Q_a and Q_b are now an astable multivibrator whjch starts at about 1Hz and oscillates faster as more leakage passes across the sense electrodes.

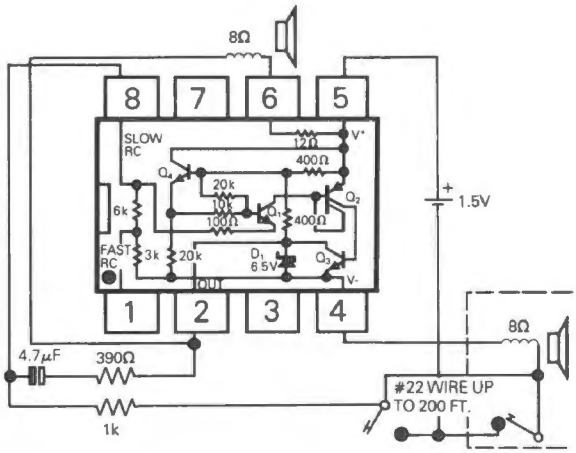
The multivibrator then acts as both an amplifier and a modulator. The pulse waveform at the collector of Q_a varies the timing current through the 3.9k resistor to pin 8 of the RS3909 resulting in a distinctively modulated tone output.

The sensor should be part of the base of the box in which the alarm circuitry is contained. It consists of two electrodes six or eight inches long spaced about ⅛inch apart. Two strips of stainless steel on insulators, or the appropriate zig-zig path cut in the copper cladding of a circuit board will work well. The bare circuit board between the copper sensing areas should be coated with warm wax so that moisture on the floor, not that absorbed by the board will be detected. The circuit and sensor can be tested by just touching a damp finger to the electrode gap.

Minimum cost, simplicity, and very low power drain are the aims of the Morse Code set of Figure 15. One oscillator simultaneously drives speakers at both sending and receiving ends. Calculations and actual use tests indicate life of a single alkaline AA cell to be 3 months to over a year depending on usage.

Commonly available, low cost 8Ω speakers are effectively in series to better match RS3909 characteristics. The three wire system and parallel telegraph keys allow beginners and children to use the set without having to understand the use of a 'transmit-receive' switch.

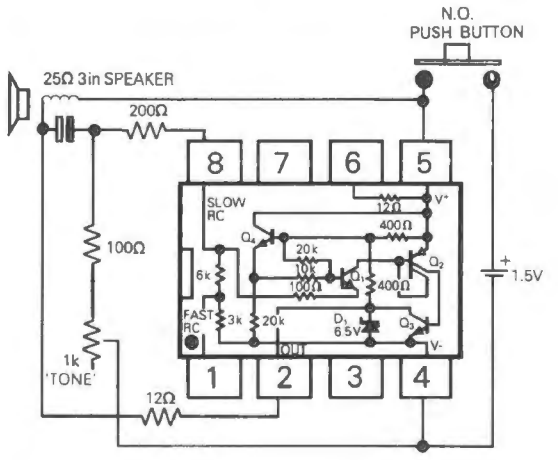
Figure 15 **Morse code set**



The two resistors are added to obtain a suitable average power output and electrically force the oscillator toward the desired 50% duty cycle. Acoustically, both speakers are operated at resonance (about 400Hz in the prototype) for maximum pleasing tone with minimum power drain. Each of the two speaker enclosures has holes added to augment this resonance. For each different type of speaker and size of box; hole and capacitor sizes will have to be determined by experiment for the most stable resonant tone over the expected battery voltage variation.

Experiments with the above circuit led to development of the circuit in Figure 16. It is optimised to oscillate at any *acoustic* load frequency of resonance! With just a speaker, oscillation occurs at the speaker cone 'free-air' resonance. If the speaker is in an enclosure with a higher resonant frequency... this becomes the frequency at which the circuit oscillates.

Figure 16 **Electronic trombone**



An educational audio demonstration device, or simply an enjoyable toy, can be fabricated as follows. A roughly cubical box of about 64in³ was made with one end able to slide in and out like a piston. The box was stiffened with thin layers of pressed wood, etc. Minimum volume with the piston in was about 10in³. Speaker, circuit and battery were mounted on the sliding end with the speaker facing through a 2¼in hole. A tube was provided (2½in long 5/16in ID) to bleed air in and out as the piston was moved while not affecting resonant frequency.

'Slide tones' can be generated, or a tune can be played by properly positioning the piston part and working the push button. Position and direction of the piston are rather intuitive, so it is not difficult to play a reasonable semblance of a tune after a few tries.

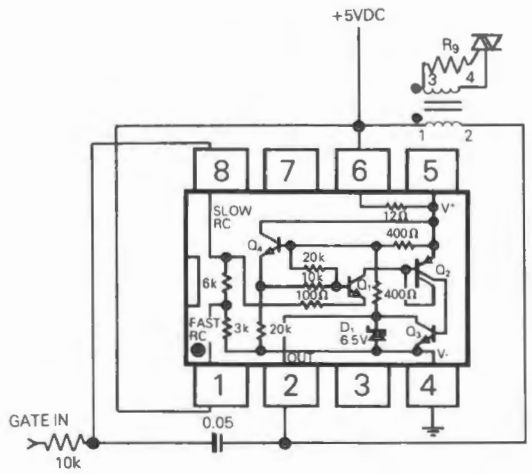
The 12Ω resistor in series with pin 2 (output transistor Q_3's collector) and the speaker, decouples voltages generated by the resonating speaker system from the low impedance switching action of Q_3. The 100μF feedback capacitor would normally set a low or even sub-audio oscillation frequency. Therefore, the major positive feedback voltage to pin 8 is the resonant motion *generated* voltage from the speaker voice coil. Therefore, the RS3909 will continue to drive the speaker at the resonance with the highest combined amplitude and frequency.

It can be seen already that the RS3909 having direct speaker drive and resonance following capability, can perform functions that are considerably less practical with older timer and unijunction circuitry.

Applications: trigger and other.

With its high pulse current capability, the RS3909 is a good pulse-transformer driver. Further, it uses fewer parts and operates more successfully from low voltage supplies than do the equivalent unijunction circuits. The 'Triac' trigger of Figure 17 operates from a 5V logic supply and provides gate trigger pulses of up to 200mA.

Figure 17 **Triac driver**



With no gate input, or a TTL logic high input, the RS3909 is biased off since pin 1 is tied to V⁺. With a logic low at the gate in, the IC provides 10μs pulses at about a 7kHz rate. A TTL gate loaded only by this circuit is assumed since otherwise worst-case voltage swing may be insufficient. This trigger is not of the 'Synchronised Zero Crossing' type since the first trigger pulse after gating on could occur at any time. However, the repetition rate is such that after the first cycle, a triac is triggered within 16V of zero with a resistive load and a 240Vac line.

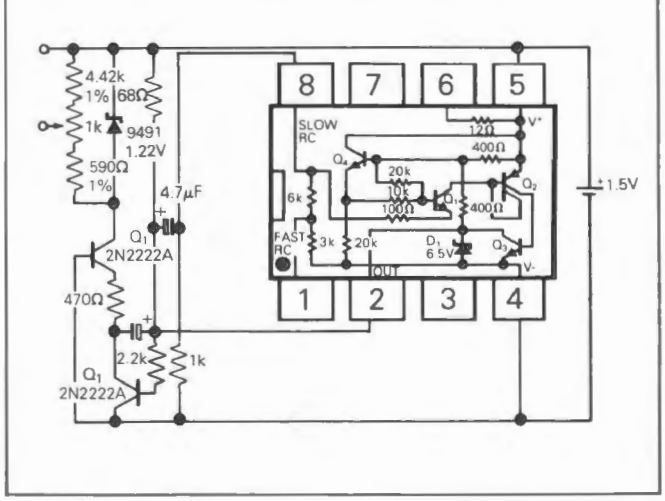
The RS pulse transformer 196-454 provides a 2:1 current step-up, and suitable isolation between the low voltage circuitry and power which lines up to 240Vac. Resistor R_g, which includes transformer winding, resistance, can be as little as 3 or 4Ω for high current triacs. Low current types may need excessive 'holding' current with such low R_g, so it may be raised to as much as 100Ω with a sensitive gate triac.

Oscillation of the RS3909 will start when the dc bias at pin 8 is between 1.6 and 3.9V. In Figure 17 pin 8 is connected between the 10k input resistor and a 6k resistor to 5V. With 3.8V in, pin 8 is at 4.5V so there is no oscillation. with 1V, or less, in, pin 8 is at 3.5V or below and oscillation occurs. From this example, it can be seen that other input resistors or bias dividers can be calculated to gate the RS3909 triac trigger from other logic levels.

A useful electronic laboratory device is a precision square wave generator/calibrator. If the output is held at a few tenths per cent of 1V, peak-to-peak, it is useful in calibrating oscilloscopes and adjusting 'scope probes. Many lower cost or battery-portable oscilloscopes do not have this feature built in. Also it is useful in checking gain and transient response of various amplifiers including 'hi-fi' power amplifiers.

Battery powered equipment is free from both the inconvenience of a mains lead, and from some of the noise and hum effects of equipment attached to the power line. Operation for over five hundred hours from a single flashlight 'D' cell is the bonus provided by the circuit shown in Figure 18. The lowest voltage band gap ref. the 9491 is used in conjuction with a current source, and the voltage boost characteristic of the RS3909.

Figure 18 **Oscilloscope calibrator**



Output is a clean rectangular wave which can be adjusted to exactly a 1V amplitude. A rectangular wave of approximately 1.5ms 'on' and 5.5ms 'off' was chosen for circuit simplicity and low battery

drain. Waveform clipping is virtually flat due to complete turn-off of the current switch Q_2 and the typical 'on' impedance of 2Ω provided by the 9491. The temperature coefficient of 30ppm/°C at room temperature allows negligible drift of the waveform amplitude under laboratory conditions. Loading by an oscilloscope probe will also be insignificant.

The circuit will work properly down to battery voltages of 1.22V. This is because the 100μF electrolytic capacitor drives the emitter Q_2 below the supply minus terminal. At a battery voltage of 1.22, the collector of Q_2 can still swing more than 1.6V. Q_1 uses the 'off' periods of the RS3909 to ensure that the 100μF capacitor is charged to almost the entire battery voltage. Thus when the RS3909 turns on and pin 2 drives almost to the minus supply voltage, the negative side of the capacitor is driven 0.9 to 1.2V below this terminal. Low battery voltage cannot lead to an undetected error in the 1V squarewave. This is because the waveform becomes distorted rather than just decreasing in amplitude as battery voltage becomes too low.

The following two circuits are examples of logic or computer type functions. They use 3V power supplies (2 cells) because the RS3909 was designed not to have any stable or 'latching' states with a 1.5V supply.

Switches on both circuits are momentary types. In each case a small charge or impulse affects the circuit's state. The circuit of Figure 19 switches to and *holds* its condition whenever the switch changes sides, even if contact is made only briefly. The circuit of Figure 20 delivers about a ½ second flash from the LED every time its pushbutton makes contact, whether briefly or for a much longer period of time. Such circuits are used with keyboards, limit switches, and other mechanical contacts that must feed data into electronic digital systems.

By again leaving out the positive feedback capacitor, the RS3909 can become a low power amplifier. This little audio amplifier can be used as a one-way intercom or for 'listening in' on various situations. Operating current is only 12 to 15mA. It can hear fairly faint sounds, and someone speaking directly into the microphone generates a full 1.4V peak-to-peak at the loudspeaker.

Figure 19 **Latch circuit**

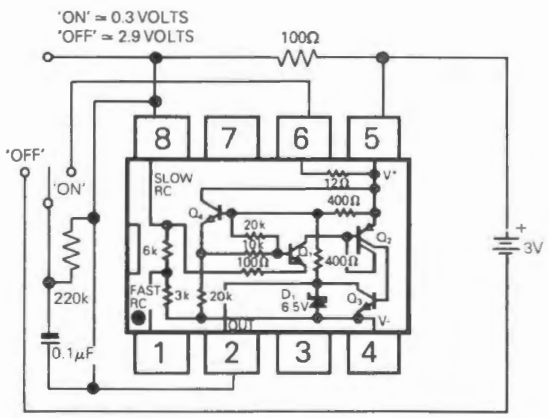


Figure 20 **Indicating one-shot**

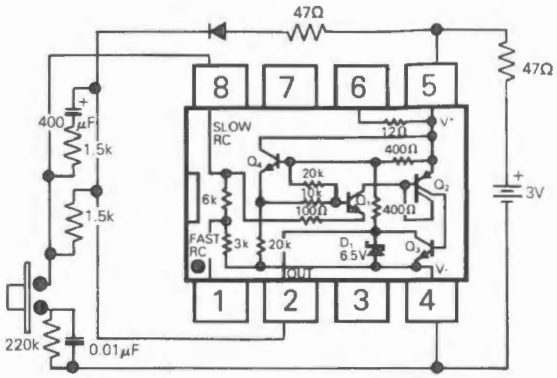
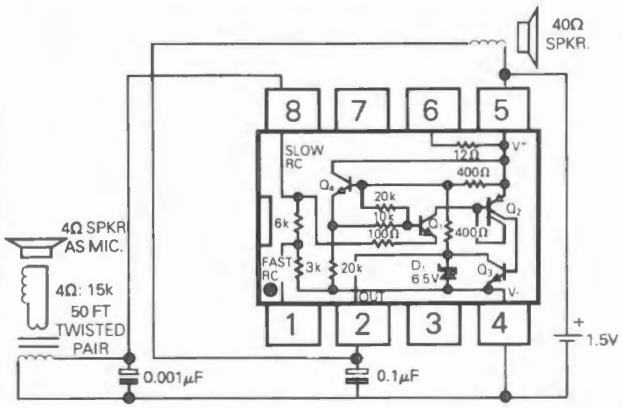


Figure 21 **Miniature power amplifier**



Application hints

With 1.5V supplies, certain problems can occur to stop oscillation or flashing. Due to the way gain is achieved and the type of feedback, too heavy a load may stop an RS3909 from oscillating. 20Ω of pure resistive load will sometimes be sufficient. Strangely enough, lamp filaments, probably because of some inductance, don't seem to follow this rule. Also in flasher circuits, an LED with leakage or conductivity between 0.9 and 1.2V will stop the RS3909.

Great frequency stability was not one of the design aims of the RS3909. In LED flasher circuits it is better than might be expected because the negative temperature coefficient of the LED partially compensates the IC.

Simple oscillators, without the LED, are uncompensated for temperature, This is due to using one and two-thirds of a silicon junction drop as the on-off trip point and the use of the integrated timing resistors with their positive temperature coefficient. Further, most capacitors of 1μF or over, shown in the circuits, will usually be electrolytics for size reasons. These, however, are not particularly stable with temperature and their initial tolerances vary greatly with different types of capacitors.

In most of the oscillator circuits, frequency is also proportional to battery voltage. This must be considered when starting with a completely unused cell

at 1.54V or so, and deciding what the 'end-of-life' voltage is to be. This can be in the range of 1.1 to 0.9V, a drastic change. It helps to remember how bright flashlights are with a fresh set of batteries, and how dim they are when the batteries are finally changed.

Flashers and tone generators for alarms are not, however, demanding for stability. Flash rate changes of 50% or tone shifts of ½ an octave are not particularly annoying or even too noticeable.

One interesting point is that the low operating power of most of the circuits presented allows them to be powered by solar cells as well as regular batteries. In bright sunlight, 3 to 4 cells in series will be needed. In dimmer light, 4 to 6 cells will be sufficient. Current from cells considerably under an inch in area generally will be sufficient, but circuits drawing a high pulse current (such as SCR triggers) will need a surge storgage capacitor across the solar cell array.

The RS3909 was designed to be inherently self-starting as an oscillator, and LED flasher circuits are, at any voltage, because the load is nonlinear. A load with sufficient self inductance will always self-start, although possibly at a higher than expected frequency. There is an exception for largely resistive loads on an oscillator operating with a supply larger than 2 or 2.5V. A stable state exists with Q_3 turned completely 'on' and the timing resistors from pin 8 to the supply minus still drawing current. A reliable solution is to bias pin 8 (for instance with a resistor to V^+) so that its DC voltage is half a volt less than half the supply voltage.

The duty cycle of the basic LED flasher is inherently low since the timing capacitor is also driving the very low LED 'on' impedance. For other oscillators the 'on' duty cycle can be stretched by adding resistance in series with the timing capacitor. Additionally, nonlinear resistance can be used as timing resistance.

RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company
Telephone: 0536 201234
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RS data

Programmable 7-day, 4 channel timer

Stock number 332-852

This compact, easily programmed, electronic timer has four isolated, single pole changeover relays that can be switched independently or synchronously depending on the user programme entered via the front keypad. The front panel is protected by a hinged transparent cover. A large LCD display indicates, in normal running mode, the time in hours, minutes and seconds, day of the week (1 = Mon, 2 = Tues, etc.) and the state of each of the four channels, ie. ON or OFF. This display is also used when entering and checking programmes. **The timer has a setting accuracy and minimum 'ON/OFF' interval of one second.**

The user programme is entered into the memory as a series of steps. Each step specifies an 'ON' time and the days of the week when this time is valid, similarly an 'OFF' time and the days of the week when this 'OFF' time is valid and the specific channels that will respond to the ON/OFF programme. Thus using one programme step only, an ON/OFF cycle can be repeated over any combination of week days (up to seven) and implemented on one or more channels simultaneously. While entering and checking the programme, each step is displayed as a 'picture' showing the specified ON and OFF times, days and channels. Up to 62 programme steps may be entered in any order and the timer will automatically detect the chronological sequence based on the specified 'ON' time of each step. Alteration to a particular programme step can be performed without affecting the remainder of the programme. Manual override facility can be used to set the state of any of the four outputs regardless of the programmed instructions. In the event of power failure or disconnection, battery reserve ensures continued operation (including outputs switching) for approximately 100 hours. The timer can be surface mounted using the plug-in base provided, DIN rail (RS424-131) mounted using the DIN-rail attachment or though panel mounted using the panel bracket included.

Features

- Four outputs which can be switched independently or synchronously
- Output rating per channel – 4A at 250V ac
- Minimum ON/OFF interval of one second
- Independent manual override switch for each channel
- Up to 62 programme steps available for each channel
- Rechargeable battery reserve maintains the programme and output switching for a minimum of 100 hours after supply disconnection
- Front keypad and display protected by a hinged transparent cover
- Unit can be surface, through panel, or DIN rail mounted.

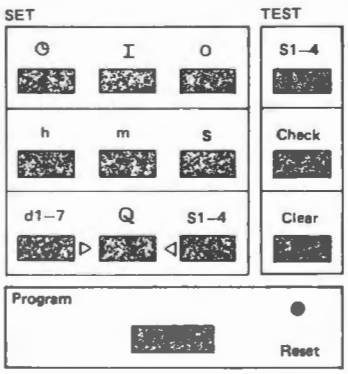
5730

Specification

Supply voltage _____ 240V ac +10%-15%, 50/60Hz
Power consumption _____ 2VA
Output _____ 4 independent change-over relays, voltage free contacts
Contact rating, each _____ 4A 250V ac resistive
Maximum current per contact _____ 8A peak
Clock accuracy ____ ±5 min. per annum (worst case)
Battery reserve _____ 100 hours approximately
Minimum 'ON' or 'OFF' period _____ 1 second
Operating temperature _____ 0 to +50°C
Storage temperature _____ –10 to +65°C

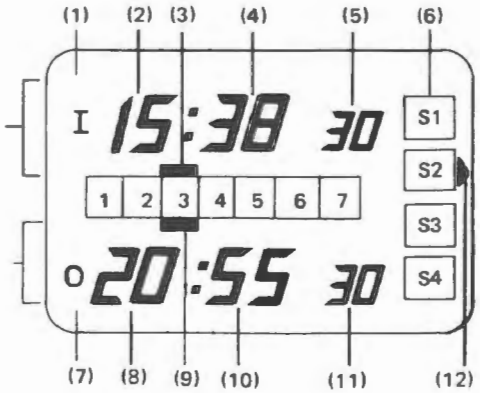
Keypad description

◷	Initiates clock setting mode.
I	Selects 'Switch-ON' time.
O	Selects 'Switch-OFF' time.
h	Hours setting (0-24).
m	Minutes setting (0-60).
s	Seconds setting (0-60).
d1–7	Day selection.
S1–4	Channel selection ('TEST' and 'SET' modes).
Q	Confirmation of day and channel selection.
Program	Programme step storing and return display to real time mode.
Check	Calling up programme step.
Clear	Cancellation of part or complete programme step.
Reset	Deletes complete programme and resets the clock to 00.00, day one – tool operated.



Display description

1. 'ON' time identifier.
2 & 8. Hours indicator.
3. Day selection cursor for 'ON' time or day indication (real time display mode).
4 & 10. Minutes indicator.
5 & 11. Seconds indicator.
6. Output channel.
7. 'OFF' time identifier.
9. Day selection cursor for 'OFF' switching.
12. Channel selection cursor or 'channel ON' indicator (real time display mode).



Setting the time (clock)

(i) Press ◷ .
(ii) Set time in hours, minutes and seconds using keys h , m & s respectively. When pressed momentarily, each of these keys advances the appropriate setting by one count. Fast setting can be achieved by pressing and holding the key down.
(iii) Using d1-7 key, select the present day of the week (eg. 1 = Monday, 2 = Tuesday, etc.) by advancing day selection cursor to the correct day. The day of the week selected is shown by the cursor above the 1 to 7 screen legend.
(iv) Press program to start the clock running – indicated by the seconds count incrementing.

During normal running (time display mode) the upper display indicates time and the day of the week. The state of each output relay is shown by a cursor next to the channel number S1 etc. (cursor present indicates 'ON' state for that channel).

Programming

Up to 62 programme steps (ie. an 'ON' and 'OFF' time combination) can be stored in the timer. When programming each step the display shows the specified 'ON/OFF' times, the days of the week when switching is to take place and the channel (or channels) to be switched. Each step can select one or more of the channels to synchronously switch 'ON' and 'OFF' for any combination of the seven days in a week.

(i) Press I and set the time for 'ON' switching in hours, minutes and seconds (as detailed in (ii) above).
(ii) Select the day (or days) when the 'ON' switching is required using d1–7 to index the day selection cursor. If more than one day is to be selected press Q when the cursor has reached each day that is required before continuing the indexing. This will mark that day number. Up to seven days can be set.

(iii) Press [0] and set the time for 'OFF' switching in hours, minutes and seconds.

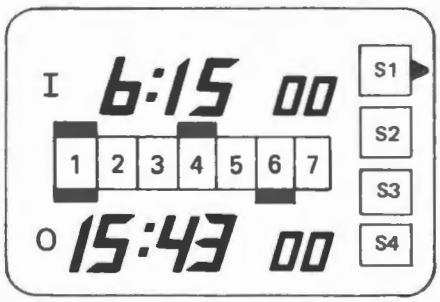
(iv) Repeat (ii) for day(s) selection when the 'OFF' switching is to apply – note these days may be different from 'ON' days as switching period may span midnight.

(v) Select the channel(s) that will follow the specified 'ON' & 'OFF' switching programme using [S1–4] to index the channel selection cursor. If more than one channel is to be selected press [0] when the cursor has reached each channel that is required before continuing to index. All four channels can be selected if required.

(vi) Press [Program] to enter the programme step into the memory as a valid instruction. **Note:** if any of the details are missing from the step specification, eg. a day number or a switching time, the step will not be accepted as an instruction until it is fully specificed. This is indicated by the display not reverting to the real time mode immediately after [Program] has been pressed. However, the unit will revert to real time mode after approximately 40 seconds if no complete programme step detail has been keyed during that time. At any stage in the programming of a step, the whole step may be cleared by pressing [Clear], [Program] & [Clear] again – Pressing [Clear] alone will delete the last entry made only.

(vii) Repeat (i) to (vi) above to enter the next programme step. It is not necessary to enter programme steps in any particular order as the timer will automatically detect the chronological sequence based on the programmed 'ON/OFF' time of each step.

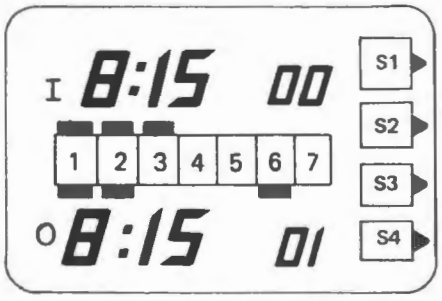
Programme step examples



represents instruction for output relay on channel one to switch as follows:

'ON' at 6:15 on Monday
'OFF' at 15:43 on Monday
'ON' at 6:15 on Thursday
'OFF' at 15:43 on Saturday

This routine repeats every week.



Instructs all 4 channels to synchronously switch as follows:

'ON' at 8:15 00 on Monday
'OFF' at 8:15 01 on Monday
'ON' at 8:15 00 on Tuesday
'OFF' at 8:15 01 on Tuesday
'ON' at 8:15 00 on Wednesday
'OFF' at 8:15 01 on Saturday

This routine repeats every week.

Programme check

This procedure is for checking the programme in memory but no actual test of output state switching is performed.

(i) Press [S1–4] once in the 'TEST' keypad area (NOT the [S1–4] in the 'SET' area). Channel cursor appears next to channel [S1]. Further key operation advances the cursor through channels 2-4. When a particular channel is selected all programme steps relating to that channel can be checked.

(ii) Press [Check] once. The complete 'picture' of the first step (in time) with the instructions related to the selected channel in (i) will be displayed. Press [Check] again to display the next step relating to that channel. Continue the sequence to display all the steps related to the channel under test. When the last step has been displayed the next check operation displays all zeros for the 'ON' and 'OFF' times. Further [Check] operations will simply recycle the programme for the selected channel.

(iii) Repeat (i) and (ii) to check all programme steps relating to the other channels. For any step with instructions common to other channels as well as the channel under test, the step picture display will also indicate the number(s) of the other channel(s).

(iv) Press [Program] to return the display to time mode.

Programme modification

To delete or modify a programme step, proceed as for programme check until the particular step picture is displayed. To modify the step, press [1] or [0], make the required changes and press [Program] to store the modified step. To delete a step while on display press [Clear] followed by [Program]. The entire contents of the memory as well as the real time record can be deleted if a tool is inserted to depress the front panel 'RESET' button.

Note: while checking or modifying the programme, the timer is still in the normal running mode (except there is no real time display). Thus, any instructions that are valid during testing and programme modification will be obeyed and the relevant output relays will operate.

Manual override

For each of the four channels, an independent 3-position selector switch is provided. When the switch is in 'progr' position the output state is dictated by the programme. When the switch is in 'I' or 'O' position the output state for the channel is

'ON' or 'OFF' respectively, regardless of the programme. This override may be desirable when entering or changing the programme as it ensures that no output switching takes place during that time.

Power failure

In the event of mains failure or disconnection a back-up battery ensures full continuous operation (including output switching) for approximately 100 hours. If power failure exceeds this period, clock setting and re-programming may be needed.

Note: the back-up battery may require up to 100 hours continuous mains operation to achieve full charge.

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Video matrix D to A RS1886

RS data

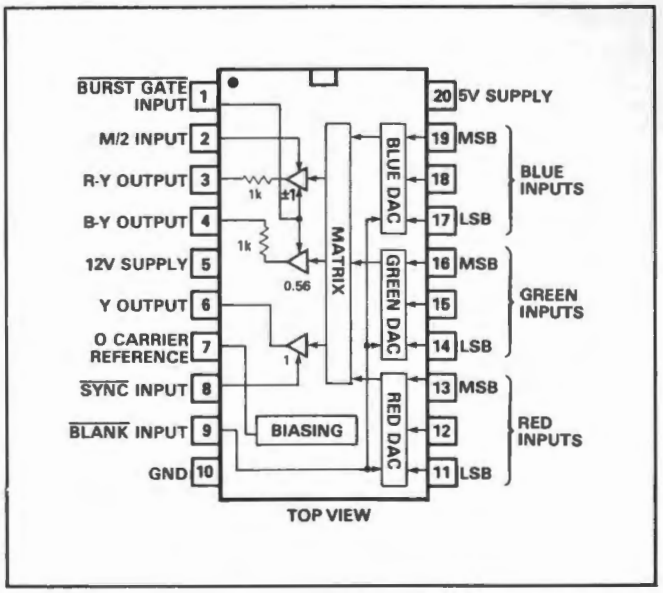
Stock number 300-984

The RS1886 is a TV video matrix D to A converter which encodes luminance and colour difference signals from 3-bit red, green and blue inputs. The luminance output is encoded from the equation Y = 0.3R + 0.59G + 0.11B and the R-Y and B-Y outputs are weighted to prevent over-modulation. A built-in R-Y and burst gate polarity switch allow European PAL compatible, or NTSC, signals to be encoded. All output levels including an RF O Carrier Bias Voltage have been referenced to 5V for direct connection to the RS1889 video modulator. When used in combination with the RS1889 and a suitable sync generator, 3-bit R, G and B information may be encoded to both composite video and VHF channel carrier. (UHF channels may be generated with the addition of a basic frequency changer or by using a UHF modulator, see data sheet 5493).

For full details of RS1889 video monitor modulator please refer to Data Sheet 5285.

Features

- Complete digital to composite video or VHF encoding with RS1889
- 1-pin PAL/NTSC mode select
- 8 levels of grey scale
- Allows wide range of colorimetry
- Low power TTL inputs
- Wideband luminance output
- Weighted R-Y, B-Y outputs



Absolute maximum ratings

Supply voltage	
Pin 5	15V
Pin 20	6V
Input voltage (Pins 1, 8, 9, 11-19)	–0.5V, +12V
Pin 2 voltage relative to pin 20	0.8V
Output current	5mA
Power dissipation, T_A = 25°C (Note 1)	1.67W
Storage temperature range	–55°C to +150°C
Operating temperature range	0°C to 70°C
Lead temperature (soldering, 10 seconds)	300°C

Electrical characteristics T_A = 25°C, (Figure 1, Note 2)

Parameter	Conditions	Min.	Typ.	Max.	Units
5V Supply Current (Pin 20)	$\overline{BLANK}$ = 0.8V	7	11	16	mA
12V Supply Current (Pin 5)	$\overline{BLANK}$ = 0.8V	9	13	17	mA
Logic '1' Input Current (Pins 1, 2, 8, 9, 11-19)	Input Voltage = 5.0V		0	10	μA
Logic '0' Input Current (Pins 1, 2, 8, 9, 11-19)	Input Voltage = 0.3V		–0.01	–0.18	mA
Output Offsets ΔV_Y ΔV_{R-Y} ΔV_{B-Y}	R, G, B = 0.8V		 0 0 0	 ±50 ±50 ±50	 mV mV mV
R-Y Full Scale, $(\Delta V_{R-Y})_{FS}$	R = 2V; G, B = 0.8V	1.0	1.23	1.4	V
B-Y Full Scale, $(V_{B-Y})_{FS}$	B = 2V; R, G = 0.8V	0.7	0.87	1.0	V
Green Full Scale ΔV_{R-Y} ΔV_{B-Y}	G = 2V; R, B = 0.8V	 –0.85 –0.45	 –1.03 –0.58	 –1.2 –0.7	 V V

Parameter	Conditions	Min.	Typ.	Max.	Units
Y Full Scale $(\Delta V_Y)_{FS}$ ΔV_{R-Y} ΔV_{B-Y}	R, G, B = 2V	1.6	1.75 0 0	1.9 ±100 ±75	V mV mV
O Carrier Reference, ΔV_O		2.0	2.2	2.5	V
Blanking Level, ΔV_Y	$\overline{BLANK}$ = 0.8V		0	±50	mV
Sync Level, ΔV_Y	$\overline{BLANK}$, $\overline{SYNC}$ = 0.8V	–0.67	–0.77	–0.87	V
NTSC Burst, ΔV_{B-Y}	$\overline{BLANK}$, $\overline{BURST\ GATE}$ = 0.8V	–0.26	–0.35	–0.46	V
PAL Burst ΔV_{R-Y} ΔV_{B-Y}	SW in PAL Position; $\overline{BLANK}$, $\overline{BURST\ GATE}$, H/2 = 0.8V	–0.2 –0.2	–0.25 –0.25	–0.32 –0.32	V V
PAL Inversion Ratio $(\Delta V_{R-Y})_{PAL}/(\Delta V_{R-Y})_{FS}$	R = 2V; G, B, H/2 = 0.8V SW to PAL Position	–0.9	–1.0	–1.1	
Y Linearity Error	Figure 1b Input Connection		±1	±6	%FS
Y Switching Times Rise Time, t_R Fall Time, t_F Settling Time ± 1 LSB	15kHz Square Wave Switching R, G, B in Parallel		 35 30 50		 ns ns ns

Note 1: Above T_A = 25°C, derate based on $T_{J(MAX)}$ = 150°C and θ_{JA} = 75°C/W.

Note 2: Unless otherwise stated, $\overline{BLANK}$, $\overline{SYNC}$, $\overline{BURST\ GATE}$ = 2V and SW is in the NTSC position. All outputs are referenced to the +5V supply as shown in Figure 1a.

Test circuits

Figure 1a **6 colour input connections**

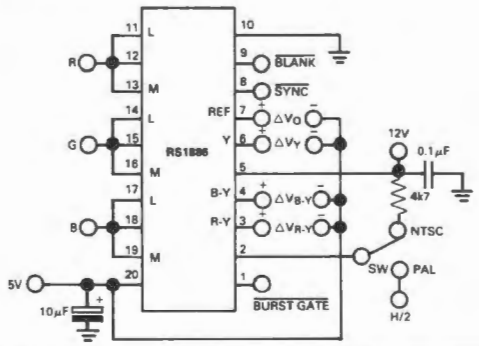
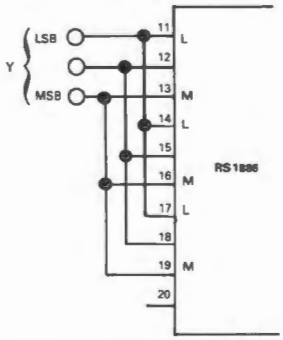
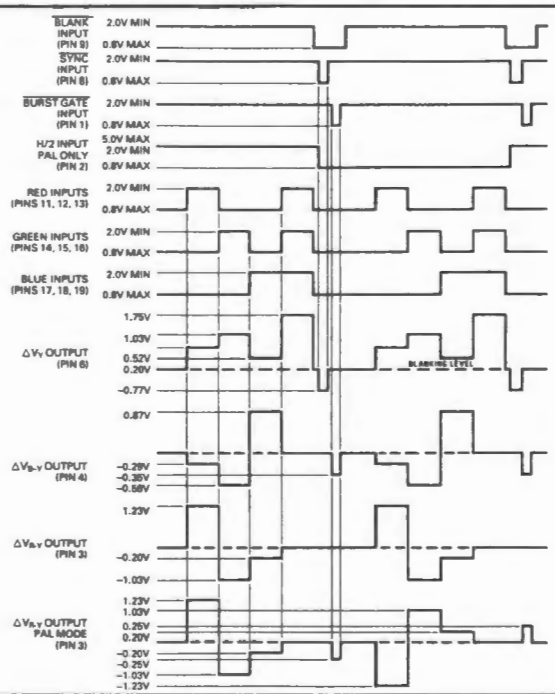


Figure 1b **8 level grey scale input connections**



Typical input and output waveforms



Circuit description

The 3-bit red, green, and blue inputs go to identical 3-bit current-mode digital-to-analogue converters (DACs). Each DAC consists of three binary-weighted current sources controlled by differential-amp current switches. The DAC output currents are arbitrarily given a weighting factor of 0.59, which is the green coefficient in the luminance equation. Portions of the red and blue currents are split off, so that the remaining currents combined with the green current from the luminance current $I_Y = 0.3\ I_R + 0.59\ I_G + 0.11\ I_B$. I_Y develops the luminance voltage V_Y across R_O in a summing amplifier referenced to the +5V supply. A current switch operated by pin 8 adds (–) sync pulses to the Y output at pin 6.

The portions of red and blue currents previously split off flow through resistors $R_O/0.29$ and $R_O/0.48$, which are weighted to form the red and blue voltages respectively. Since the opposite ends of the two resistors are connected to V_Y, the red and blue voltages across the resistors subtract from V_Y to develop the colour difference voltages V_{Y-R} and V_{Y-B}. V_{Y-B} is coupled through a x.56 gain, 5V referenced inverting amplifier to the B-Y output at pin 4. V_{Y-R} feeds parallel inverting and non-inverting unity gain amplifiers which allow either polarity to be coupled to the R-Y output pin 3. Switching between the two amplifiers is controlled by a current switch activated by the H/2 pin 2.A (–) burst gate pulse on pin 1 controls current switches which add the burst pulse components to the B-Y and R-Y outputs.

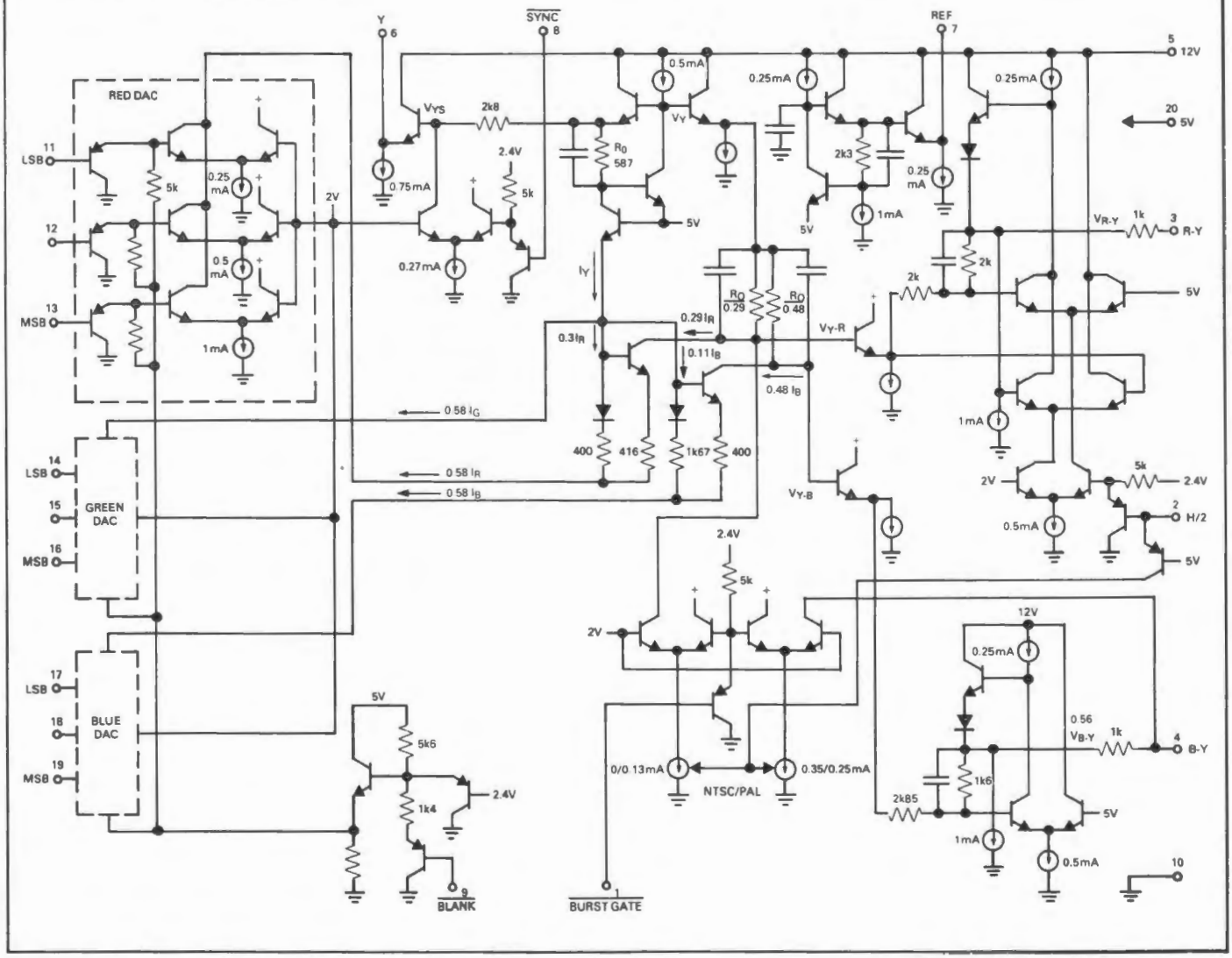
The requirements for PAL and NTSC encoding differ in the areas of burst gate operation and R-Y polarity, both of which are controlled via pin 2 as follows:

PAL, pin 2 fed by a half-line frequency TTL square wave, in this mode a PNP switch between pin 2 and +5V is held off continuously, which results in equal burst pulse components on the B-Y and R-Y outputs. In addition, the H/2 square wave causes the R-Y output polarity to reverse every line. (When fed to the RS1889 chroma modulator this causes the phase of the R-Y subcarrier to change 180° as required in PAL.)

NTSC, pin 2 tied through an external resistor to +12V, this turns on the PNP switch continuously, which eliminates the burst pulse on the R-Y output and increases the amplitude of the B-Y pulse. Since pin 2 is being held high, the R-Y output is locked in the positive polarity.

Blanking is activated by a low on pin 9, which de-biases the left side of the DAC differential-amps, so that $I_R = I_G = I_B = 0$ independent of the input states. When blanked, the Y, B-Y and R-Y outputs all go to +5V. An additional amplifier produces a 0 carrier reference voltage at pin 7 which is 25% above the peak white voltage on the Y output, relative to +5V.

Figure 2 **RS1886 equivalent circuit**



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Application notes

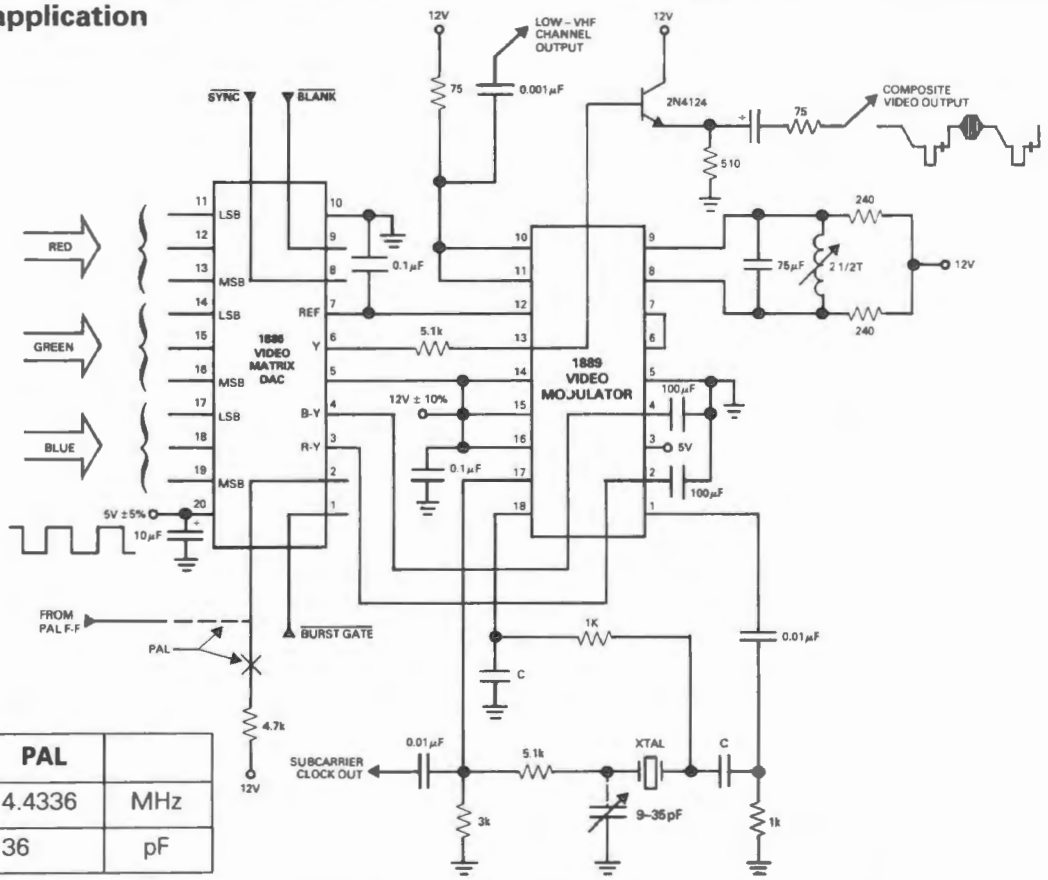
All inputs are low-power TTL compatible. Because of the very low typical input currents, the colour inputs may be paralleled in various combinations. For simple colour requirements, the Figure 1a input connection may be used to produce the 6 primary and complementary colours listed in Table 1, along with black and white. To add complex colours such as those at the bottom of Table 1, all 9 inputs may be required separately. When choosing input codes for other colours, always check the new colour against both light and dark backgrounds.

All outputs are referenced to the +5V supply for direct connection to the RS1889. The resistor on the luminance output pin 6 is used to sum the chroma subcarrier from the RS1889 and must be wired as closely as possible to preserve the video bandwidth. For the addition of sound or second RF channel, refer to RS Data Sheet 5285.

Table 1 **Input code examples for common colours**

		Input code					
		Red		Green		Blue	
	Colour	M	L	M	L	M	L
	Black	0 0 0		0 0 0		0 0 0	
	Dark Grey	0 1 0		0 1 0		0 1 0	
	Light Grey	1 0 1		1 0 1		1 0 1	
	White	1 1 1		1 1 1		1 1 1	
Primary	Red	1 1 1		0 0 0		0 0 0	
Primary	Green	0 0 0		1 1 1		0 0 0	
Primary	Blue	0 0 0		0 0 0		1 1 1	
Complementary	Cyan	0 0 0		1 1 1		1 1 1	
Complementary	Magenta	1 1 1		0 0 0		1 1 1	
Complementary	Yellow	1 1 1		1 1 1		0 0 0	
	Brown	0 1 1		0 1 1		0 0 0	
	Orange	1 1 1		1 0 0		0 0 0	
	Flesh tone	1 1 1		1 1 0		1 0 1	
	Pink	1 1 1		1 1 0		1 1 0	
	Sky Blue	1 0 1		1 0 1		1 1 1	

Figure 3 **Typical application**



	NTSC	PAL	
XTAL	3.5795	4.4336	MHz
C	43	36	pF

Note: For PAL operation, the H/2 square wave may be obtained by a ÷ 2 from horizontal sync.

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The decibel

The bel was named in honour of Alexander Graham Bell. It is defined as the common logarithm of the ratio of two power levels P_1 and P_2. Hence the number of bells B is:

$$B = \text{Log}\left(\frac{P_2}{P_1}\right)$$

A positive value of B represents power gain, a negative value for power loss and zero for no change.

The bel is a rather large unit for use in electrical engineering. A smaller and more convenient unit is the decibel with a magnitude of 1/10 B. So

$$dB = 10\,\text{Log}\left(\frac{P_2}{P_1}\right)$$

Or conversely

$$\frac{P_2}{P_1} = 10^{\left(\frac{dB}{10}\right)}$$

Power is often a difficult quantity to measure directly and is commonly calculated from the equations $P = I^2R$ or $P = V^2/R$ where current or voltage is more easily measured. So the change in power level becomes

$$dB = 20\,\text{Log}\left(\frac{V_2}{V_1}\right) - 10\,\text{Log}\left(\frac{R_2}{R_1}\right)$$

and

$$dB = 20\,\text{Log}\left(\frac{I_2}{I_1}\right) + 10\,\text{Log}\left(\frac{R_2}{R_1}\right)$$

Where this is measured in a system of consistent impedance ($R_1 = R_2$) these equations can be simplified to:

$$dB = 20\,\text{Log}\left(\frac{V_2}{V_1}\right)$$

and

$$dB = 20\,\text{Log}\left(\frac{I_2}{I_1}\right)$$

Or conversely

$$\frac{V_2}{V_1} = 10^{\left(\frac{dB}{20}\right)}$$

and

$$\frac{I_2}{I_1} = 10^{\left(\frac{dB}{20}\right)}$$

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dB	$\frac{I_2}{I_1}$ or $\frac{V_2}{V_1}$	$\frac{P_2}{P_1}$
+100	1.0×10^5	1.0×10^{10}
+90	3.2×10^4	1.0×10^9
+80	1.0×10^4	1.0×10^8
+70	3200	1.0×10^7
+60	1000	1.0×10^6
+50	320	1.0×10^5
+40	100	1.0×10^4
+35	56.2	3165
+30	31.6	1000
+25	17.78	316
+20	10.00	100
+15	5.62	31.6
+10	3.16	10.00
+9.5	2.98	8.91
+9.0	2.82	7.94
+8.5	2.66	7.08
+8.0	2.51	6.31
+7.5	2.37	5.62
+7.0	2.24	5.01
+6.5	2.11	4.47
+6.0	1.995	3.98
+5.5	1.884	3.55
+5.0	1.778	3.16
+4.5	1.679	2.82
+4.0	1.585	2.51
+3.5	1.496	2.24
+3.0	1.413	1.995
+2.5	1.334	1.778
+2.0	1.259	1.585
+1.8	1.230	1.514
+1.6	1.202	1.445
+1.4	1.175	1.380
+1.2	1.148	1.318
+1.0	1.122	1.259
+0.9	1.109	1.230
+0.8	1.096	1.202
+0.7	1.084	1.175
+0.6	1.072	1.148
+0.5	1.059	1.122
+0.4	1.047	1.096
+0.3	1.035	1.072
+0.2	1.023	1.047
+0.1	1.012	1.023
0	1	1

dB	$\frac{I_2}{I_1}$ or $\frac{V_2}{V_1}$	$\frac{P_2}{P_1}$
0	1	1
−0.1	0.989	0.977
−0.2	0.977	0.955
−0.3	0.966	0.933
−0.4	0.955	0.912
−0.5	0.944	0.891
−0.6	0.933	0.871
−0.7	0.923	0.851
−0.8	0.912	0.832
−0.9	0.902	0.813
−1.0	0.891	0.794
−1.2	0.871	0.759
−1.4	0.851	0.724
−1.6	0.832	0.692
−1.8	0.813	0.661
−2.0	0.794	0.631
−2.5	0.750	0.562
−3.0	0.708	0.501
−3.5	0.668	0.447
−4.0	0.631	0.398
−4.5	0.596	0.355
−5.0	0.562	0.316
−5.5	0.531	0.282
−6.0	0.501	0.251
−6.5	0.473	0.224
−7.0	0.447	0.200
−7.5	0.422	0.178
−8.0	0.398	0.158
−8.5	0.376	0.141
−9.0	0.355	0.126
−9.5	0.335	0.112
−10.0	0.316	0.100
−15	0.178	0.0316
−20	0.100	0.0100
−25	0.0562	0.00316
−30	0.0316	1.0×10^{-3}
−35	0.0178	3.16×10^{-4}
−40	0.01	1.0×10^{-4}
−50	0.00316	1.0×10^{-5}
−60	0.001	1.0×10^{-6}
−70	0.000316	1.0×10^{-7}
−80	1.0×10^{-4}	1.0×10^{-8}
−90	3.2×10^{-5}	1.0×10^{-9}
−100	1.0×10^{-5}	1.0×10^{-10}

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RS data

RM Series ferrite cores

Stock numbers 228-214 to 258

A range of 5 of the most popular pcb mounting ferrite cores covering three sizes. Of square design which allows maximum board utilisation, this series enables transformers or inductors to be constructed to meet exact customer requirements. The core material is equivalent to the commonly known grades: A13-Q3-N28. Each core is supplied in kit form and consists of the following: one pair of matched half cores, one single section bobbin with integral pins on an 0.1 in grid, one pair of retaining clips with earth spikes and one core adjuster.

To determine the number of turns required for a particular inductance use the following formula:

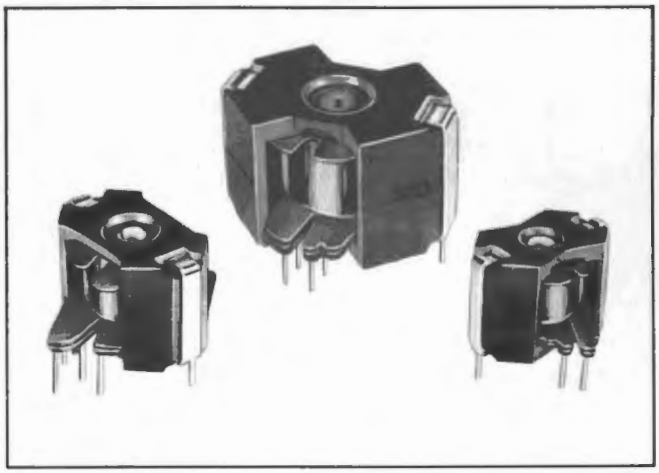
$$\text{No. turns} = \sqrt{\frac{L}{A_L}}$$

Where L = inductance in nH (10^{-9}H).

For frequencies in excess of 30kHz, the use of stranded wire is beneficial when maximum Q is required.

Features

- 5 versions available in three popular sizes
- PCB mounting
- Compact design
- Mounting pins have 2.54mm (0.1 in) spacing



Properties of core assemblies at 25°C (without adjusters)

Stock number		*RM6* **228-214**	*RM6* **228-220**	*RM7* **228-236**	*RM10* **228-242**	*RM10* **228-258**
Inductance factor (nH/turns²)	A_L	160 ±2%	250 ±2%	250 ±2%	250 ±2%	400 ±2%
Turns factor (turns for 1 mH)	a	79.06 ±1%	63.25 ±1%	63.25 ±1%	63.25 ±1%	50.00 ±1%
Effective permeability	μ_e	109.5	171.1	146.0	99.67	159.5
Temp. coeff. of μ_e (+25 to 50°C) ppm/°C		51 min. 154 max.	80 min 241 max.	73 min. 219 max.	50 min. 149 max.	80 min. 239 max.
Adjuster range		+20%	+14%	+15%	+17%	+20%
Max. residual plus eddy current core loss						
Tangent $\tan\delta_r + _f$ at 30kHz		0.34×10^{-3}	0.53×10^{-3}	0.47×10^{-3}	0.32×10^{-3}	0.51×10^{-3}
at 100kHz		0.58×10^{-3}	0.91×10^{-3}	0.82×10^{-3}	0.60×10^{-3}	0.96×10^{-3}
Recommended frequency range (kHz)		5.5 to 800	3.5 to 700	3 to 650	2 to 650	1.2 to 500
Energy storage capability (mJ)	LI^2_{sat}	0.383	0.245	0.406	1.731	1.082
B_{sat}	mT	250	250	250	250	250

Magnetic properties of cores

	symbol	*RM6*	*RM7*	*RM10*
Effective path length	l_e	26.9mm	29.6mm	41.7mm
Effective path area	A_e	31.3mm²	40.3mm²	83.2mm²
Effective volume	V_e	840mm³	1190mm³	3470mm³

Maximum turns accommodated on bobbin

wire dia. (mm)	*RM6*	*RM7*	*RM10*	*wire dia. (mm)*	*RM6*	*RM7*	*RM10*
0.2	205	306	612	0.56	25	36	87
0.224	160	250	484	0.71	19	33	59
0.25	127	209	402	0.8	13	19	44
0.315	87	131	246	1.0	9	11	25
0.4	47	76	160	1.25	4	9	19
0.5	36	50	98	1.5	3	7	11

RS data

Figure 1 **Exploded view of kit**

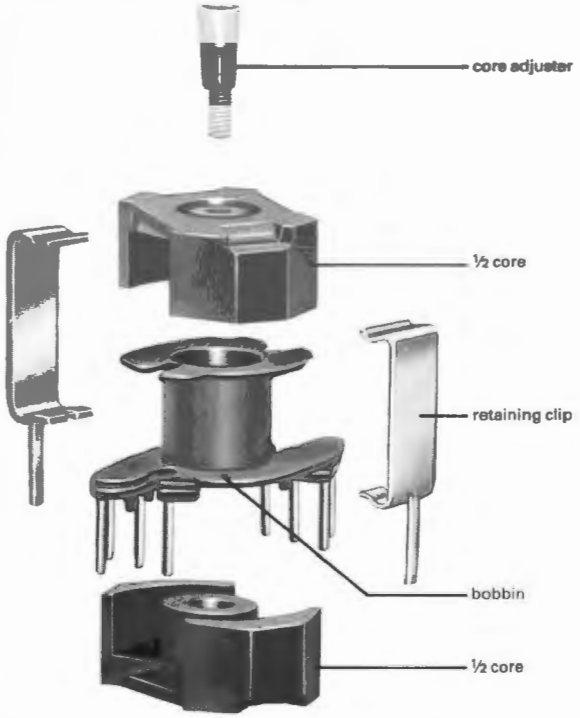
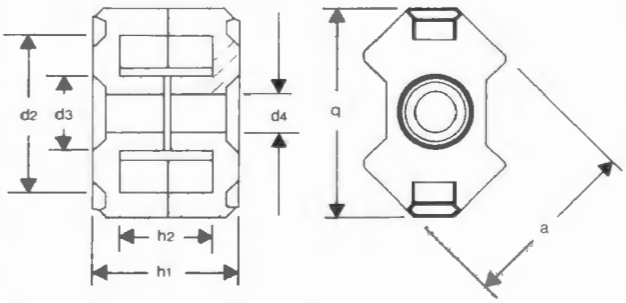
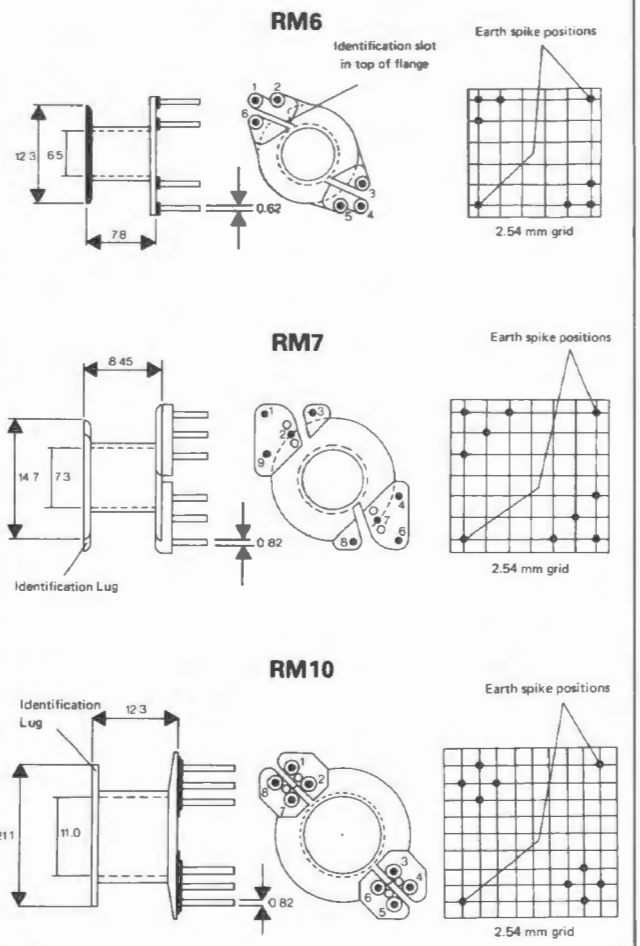


Figure 2 **Core dimensions**



	RM6	*RM7*	*RM10*
a (max.)	14.7	17.2	24.7
d2 (min.)	12.4	14.76	21.2
d3 (max.)	6.4	7.24	10.9
d4 (min.)	3.05	3.05	5.4
h1 (max.)	12.5	13.5	18.7
h2 (min.)	8.0	8.93	12.4
q (max.)	17.9	20.3	28.5

Figure 3 **Bobbin dimensions**



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Speech synthesis i.c. 263

RS data

Stock number 630-695

The 263 is a versatile, high-quality, phoneme-based speech synthesiser circuit contained in a single monolithic CMOS integrated circuit. It is designed to produce an audio output of unlimited vocabulary, music and sound effects at an extremely low data input rate.

Speech is synthesised by combining phonemes, the building blocks of speech, in an appropriate sequence. The 263 contains five eight-bit registers that allow software control of speech rate, pitch, pitch movement rate, amplitude, articulation rate, vocal tract filter response, and phoneme selection and duration.

Features

- Single low power CMOS i.c. speech synthesiser
- Extremely low data input rate
- 8-bit bus compatible with selectable handshaking modes
- Non-dedicated speech allowing text-to-speech programming
- Programmable and hard power down/reset mode
- On-chip switched capacitor filter
- Single +5V supply operation.

Absolute maximum ratings

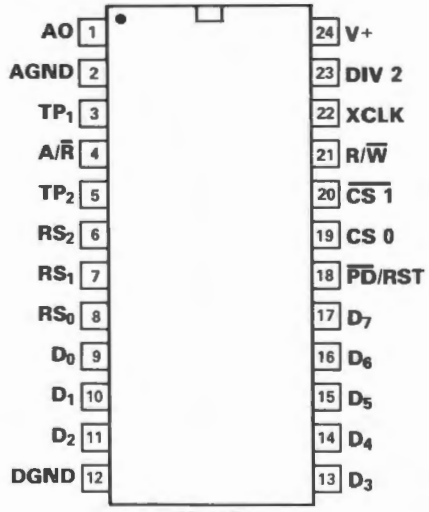
Supply voltage V^+ 7.0V
Input voltage V_{IN} ..... –0.5 to V^+ +0.5V
dc current at inputs I_{INM} ..... ±1.0mA
Power dissipation 500mW
Operating temperature range ..... –40 to +85°C
Storage temperature range ..... –55 to +125°C

ATTENTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

Pin connections



TOP VIEW

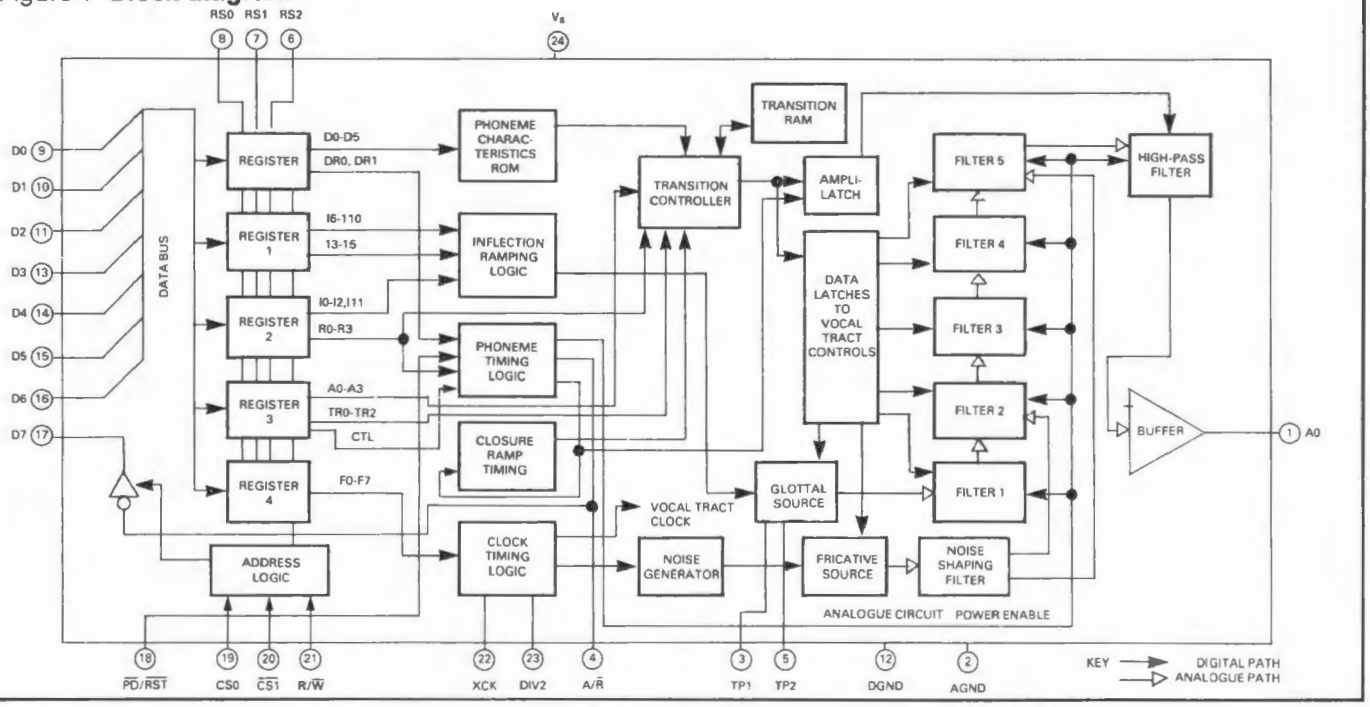
Electrical characteristics

Conditions 4.5 $< V^+ \leq$ 5.5V –40°C $\leq T_A \leq$ 85°C
1.5MHz ≤ XCK frequency ≤ 2.0MHz, when XCK/2 = logic 1 or
0.75MHz ≤ XCK frequency ≤ 1.0MHz, when XCK/2 = logic 0.

Parameter	Conditions	Min.	Typ.	Max.	Units
Power supply current	$\overline{PD}/\overline{RST}$ = 1, CTL = 0 $\overline{PD}/\overline{RST}$ = 0, CTL = 1		8 7	20 18	mA mA
Audio Output Output level dc output offset Resistive loading		 0.28V^+ 0.5V^+ 10	 0.37V^+ 0.6V^+	 0.50V^+ 0.7V^+	 V_{PP} V kΩ
Bus Control Inputs, Data inputs (RS0, RS1, RS2, CS0, $\overline{CS1}$, D0-D7, $\overline{PD}/\overline{RST}$) Input high voltage V_{IH} Input low voltage V_{IL} Input leakage current I_{IN} Input capacitance C_{IN} Input Capacitance D7 input Input current D7 in TR1-state 'OFF' state	 V_{IN} = 0 to V^+ V_{IN} = 0, T_A = 25°C measured at f = 1.0MHz V_{IN} = 0.4 to 2.4V	 GND + 2.4 –0.3	 2.0	 V^+ +0.3 +0.8 5 10 20 5.0	 V V µA pF pF µA

Parameter	Conditions	Min.	Typ.	Max.	Units
D7 Output					
Output low voltage V_{OL}	I_{LOAD} = 0.4mA into D7			0.4	V
Output high voltage V_{OH}	I_{LOAD} = 205μA out of D7		V^+ –2.0		V
A/$\overline{R}$ Output					
Output low voltage I_{OL}	I_L = 3.2mA into A/$\overline{R}$			0.4	V
Output high leakage current I_L	V_{OUT} = 0.0 to V^+			10	μA
Output capacitance C_{OUT}	V_{OUT} = 0V, T_A = 25°C, f = 1.0MHz		15		pF
DIV 2 Input					
Input low voltage V_{IL}		–0.3		0.2V^+	V
Input high voltage V_{IH}		0.8V^+		V^+ +0.3	V
Input leakage	V_{IN} = 0.0 to V^+			5	μA
XCLK					
Input low voltage V_{IL}		–0.3		0.8	V
Input high voltage V_{IH}		2.4		V^+ +0.3	V
Input current I_{IN}	V_{IN} = 0.0 to V^+			5	μA
Input capacitance C_{IN}				10	pF
Duty cycle		0.4		0.6	–

Figure 1 **Block diagram**



The production of speech

To produce different speech phonemes (sounds) the 263 uses a model of the human vocal tract. Within the device this analogue tract is modelled with five cascaded programmable low pass filter sections. The filter sections are programmed internally by a digital controller. Either a glottal (pitch) or a pseudo-random noise source is used to excite the vocal tract, depending on whether a voiced or non-voiced phoneme is selected. During speech production the phonemes will typically last between 25 and 100 ms.

The speech attribute registers

Speech is produced by programming speech attribute (characteristic) data into five eight-bit registers. These internal registers allow selection of phonemes and speech characteristics. Refer to the Register Input Formats for the functional allocations.

Device response to attribute register data

The 263 has two general classes of attribute data: 'control' data (speech rate, filter frequency, phoneme articulation rate, phoneme duration, immediate inflection setting, and inflection movement rate) and 'target' data (phoneme selection, audio amplitude, and transitioned inflection). The 263 responds immediately upon loading 'control' data: upon loading 'target' data the device will begin to move towards that target at the prescribed transition rates. This fully internal linear transitioning between target values, done in a manner as is found in normal speech, is a key factor in reducing control data rate without sacrificing speech quality.

Attribute register writing

The eight bit data bus D7-D0 loads the particular attribute register selected by the three bit address bus RS2-RS0. To write the data, R/$\overline{W}$ (Read/Write), CS0 (Chip Select 0), and $\overline{CS1}$ pins must first be in the 0,1,0 state, respectively. The data is then written when at least one of these pins changes state. Refer to the Write Timing Diagram. Writing is accomplished by changing preferably CS0 or $\overline{CS1}$. Following device power up, nominal values should

be loaded into the attribute registers as described below.

Approximate data transfer rate
For speech production using the 263, the actual data rate depends on the amount of speech attribute manipulation. For example, the production of monotonic speech, where phoneme and duration are the only attribute manipulations, requires a data rate less than 100 bits-per-second. A higher data rate of about 500 bits-per-second is required for high quality speech due to the associated full attribute manipulation.

Selectable operation modes
The state of the Duration/Phoneme Register bits DR1 and DR0 determine the operating mode of the device when the Control bit (CTL) is changed from a logic one to a logic zero. The four modes of operation include choice of timing response between 'frame' or 'phoneme' timing (as explained below), transitioned or immediate inflection response, and setting the A/$\overline{R}$ (Acknowledge/Request Not) pin active or disabled. Refer to the Mode Selection Table 5.

Phoneme selection
The 263 can produce the 64 phonemes listed on the Phoneme Chart. Bits P5-P0 are used for phoneme selection. The relative phoneme duration is set by bits DR1 and DR0.

Phoneme articulation adjustment
A particular phoneme is produced by the combination of vocal-tract low-pass filter settings, excitation source type, and source amplitude. When a new phoneme is selected, the device performs a linear transition to the new set of characteristics. The rate of this transition is controlled by the articulation setting, bits TR2-TR0. This rate is relative in that articulation is not affected by speech rate bits R3-R0. A typical articulation register setting is '5'.

Programming inflection (pitch)
When the 263 is in the mode of immediate inflection, bits I11-I0 provide immediate adjustment with seven octaves of pitch on an even tempered scale. With the device in the transitioned inflection mode, bits I10-I6 select the target pitch and bits I5-I3 determine the inflection rate of change. Bits I11, I2, I1, and I0 always provide immediate adjustment. A typical value used for speech production is 90Hz where:

$$\text{Inflection frequency} = \frac{\text{XCK frequency}}{8 \times (4096\text{-}I)}$$

I = decimal equivalent of Inflection Register setting.

Filter frequency setting
Data bits FF7-FF0 set the clock frequency for the switched-capacitor vocal tract filters. This determines overall filter frequency response. Inflection pitch is not affected by these bits. Typically this is set to give a clock frequency of about 20kHz (see formula below), but may be manipulated to fine-tune speech quality or to change 'voice type'; bass, baritone, etc.

$$\text{Filter frequency} = \frac{\text{XCK frequency}}{2\,(256\text{-}FF)}$$

FF = decimal equivalent to the Filter Frequency Register setting.

Speech rate
Rate of speech is controlled by bits R3-R0, the Speech Rate Register. In Frame Timing Mode new attribute data is requested at the end of a 'frame' where:

$$\text{Frame duration} = \frac{4096 \times (16\text{-}R)}{\text{XCK frequency}}$$

R = decimal equivalent of Rate Register setting.

In the Phoneme Timing Mode the frame duration is modified by the phoneme duration bits DR1 and DR0 where:

Phoneme Duration = (Frame Duration) x (4-D)
D = decimal equivalent of Duration Register setting

All internal attribute transitioning is performed relative to the Speech Rate Register setting. Speech rate does not affect inflection or filter frequency. A typical rate setting is hexadecimal 'A'.

Amplitude adjustment
The overall Audio Output level is set with register bits A3-A0. Since each phoneme has a preset amplitude relative to other phonemes, it is not necessary to programme the amplitude of each phoneme; however, amplitude changes may be used to enhance the speech quality and add emphasis. Amplitude is transitioned linearly at rate dependent on the phoneme duration setting. A typical amplitude setting is hexadecimal 'C'.

Control bit and Power Down mode
Setting the Control bit (CTL) to a logic one puts the device into Power Down mode, a sort of 'standby'. This bit is also set high when the $\overline{PD}/\overline{RST}$ pin is brought low and also upon power up. The Power Down mode turns off the excitation sources and analogue circuits to reduce power consumption, but maintains the present register settings. Upon a Control bit logic one-to-zero transition, the present settings of DR1 and DR0 determine the operation mode as described above.

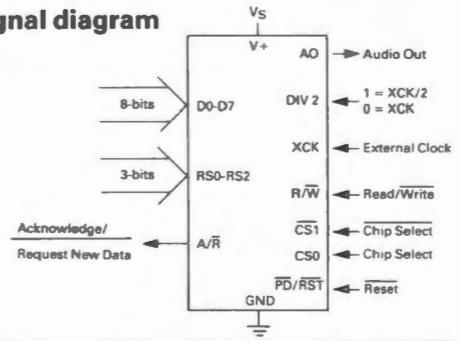
Register reading
Device pin D7 becomes an output, as the inverted state of A/$\overline{R}$, when the device is put into Read (R/$\overline{W}$ is a logic 1 and the chip is selected, $\overline{CS1}$ = 0, CSO = 1). Refer to the Read Timing Diagram. The register address bits are ignored.

Time base
Many different time bases may be utilised (see external clock input specifications). It is desirable to establish a stable crystal controlled time base from 800 to 1000kHz when DIV2 is set low, or twice the frequency when DIV2 is set high. A good time base can be easily accomplished with a 3.5795MHz crystal in conjunction with a divide-by-two circuit. The actual device timing and output frequencies are directly related to the time base frequency used.

Microprocessor interfacing
Either the A/$\overline{R}$ line, or D7 as an output, are used as an interrupt to indicate when the duration of a frame or phoneme has been exceeded. No detect-

able degradation to speech quality results when several milliseconds occur between data request and load.

Figure 2 **Signal diagram**



Pin assignment descriptions Table 1

Pin No.	Symbol	Active Level	Description
1	AO		Analogue Audio Output biased @ $V_{DD}/2$ requires an external audio amp for speaker drive
2	AGND		Analogue Ground
3	TP1		Do not use
4	A/$\overline{R}$		Acknowledge/Request Not – open collector output a low requests new data (see also pin 17)
5	TP2		Do not use
6	RS2		Register Select Input – used to select one of five internal registers in conjunction with RS1 and RS0
7	RS1		Register Select (see pin 6)
8	RS0		Register Select (see pin 6)
9	D0		LSB of 8-bit data bus – input only
10	D1		Data Input (only)
11	D2		Data Input (only)
12	DGND		Digital Ground
13	D3		Data Input (only)
14	D4		Data Input (only)
15	D5		Data Input (only)
16	D6		Data Input (only)
17	D7		MSB of 8-bit data bus. Bi-directional, inverse of pin 4 when read is high
18	$\overline{PD}/\overline{RST}$	Low	Power Down Control Input – Silences audio output and retains dc bias without disturbing register contents. Disables A/$\overline{R}$ output.
19	CS0	High	Chip Select Input
20	$\overline{CS1}$	Low	Chip Select Input
21	R/$\overline{W}$		Read/Write Control Input – Write is active low for loading internal registers. Read is active high but enables D7 only
22	XCK		Clock Input (≃ 1 or 2 MHz)
23	DIV2	High	Clock Divide by Two – used when external clock is ≃ 2MHz
24	V+		Positive Voltage Supply

Table 2
Phoneme Chart

Hex Code*	Phoneme Symbol	Example Word (or Usage)
00	PA	(pause)
01	E	MEET
02	E1	BENT
03	Y	BEFORE
04	YI	YEAR
05	AY	PLEASE
06	IE	ANY
07	I	SIX
08	A	MADE
09	AI	CARE
0A	EH	NEST
0B	EH1	BELT
0C	AE	DAD
0D	AE1	AFTER
0E	AH	GOT
0F	AH1	FATHER
10	AW	OFFICE
11	O	STORE
12	OU	BOAT
13	OO	LOOK
14	IU	YOU
15	IU1	COULD
16	U	TUNE
17	U1	CARTOON
18	UH	WONDER
19	UH1	LOVE
1A	UH2	WHAT
1B	UH3	NUT
1C	ER	BIRD
1D	R	ROOF
1E	R1	RUG
1F	R2	MUTTER (German)
20	L	LIFT
21	L1	PLAY
22	LF	FALL(final)
23	W	WATER
24	B	BAG
25	D	PAID
26	KV	TAG (glottal stop)
27	P	PEN
28	T	TART
29	K	KIT
2A	HV	(hold vocal)
2B	HVC	(hold vocal closure)
2C	HF	HEART
2D	HFC	(hold fricative closure)
2E	HN	(hold nasal)
2F	Z	ZERO
30	S	SAME
31	J	MEASURE
32	SCH	SHIP
33	V	VERY
34	F	FOUR
35	THV	THERE
36	TH	WITH
37	M	MORE
38	N	NINE
39	NG	RANG
3A	:A	MARCHEN (German)
3B	:OH	LOWE (French)
3C	:U	FUNF (German)
3D	:UH	MENU (French)
3E	E2	BITTE (German)
3F	LB	LUBE

*Note – Hex codes shown with DR0, DR1 = 0 (longest duration)

Table 3

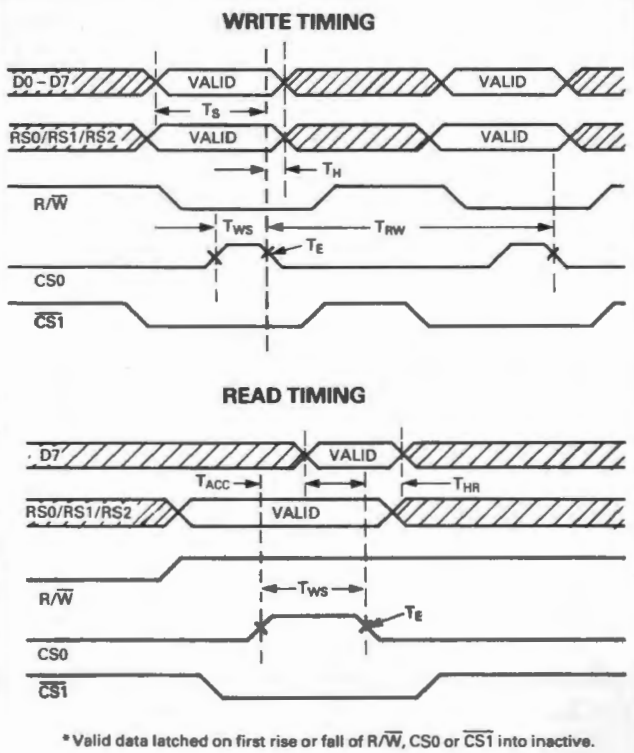
Timing characteristics

V+ = 4.5 to 5.5V. T_A = 40 to +85°C

Parameter	Symbol	Limits		Units
		Min.	Max.	
Data setup time	TS	120[1]		ns
Data hold time	TH	10[1]		ns
Strobe width	TWS	200		ns
Read/Write cycle time	TRW	2.25[2]		μs
Rise/Fall time	TE		100	ns
D7 output access time	TACC		180	ns
D7 output hold time	THR		180	ns

Notes:
1. Timing relative to deselect by either CS0, $\overline{CS1}$ or R/$\overline{W}$ changing.
2. Based on 3.5795 MHz crystal frequency.

Figure 3 **Timing diagrams**



*Valid data latched on first rise or fall of R/$\overline{W}$, CS0 or $\overline{CS1}$ into inactive.

Table 4

Register Input Formats

Register Address			Register Name	Bus Input Bit Position							
RS2	RS1	RS0		D7	D6	D5	D4	D3	D2	D1	D0
LO	LO	LO	Duration/Phoneme (DR/P)	DR1	DR0	P5	P4	P3	P2	P1	P0
LO	LO	HI	Inflection (I)	I10	I9	I8	I7	I6	I5	I4	I3
LO	HI	LO	Rate/Inflection (R/I)	R3	R2	R1	R0	I11	I2	I1	I0
LO	HI	HI	Control/Articulation/Amplitude (C/A/A)	CTL	T2	T1	T0	A3	A2	A1	A0
HI	X	X	Filter Frequency (F)	F7	F6	F5	F4	F3	F2	F1	F0

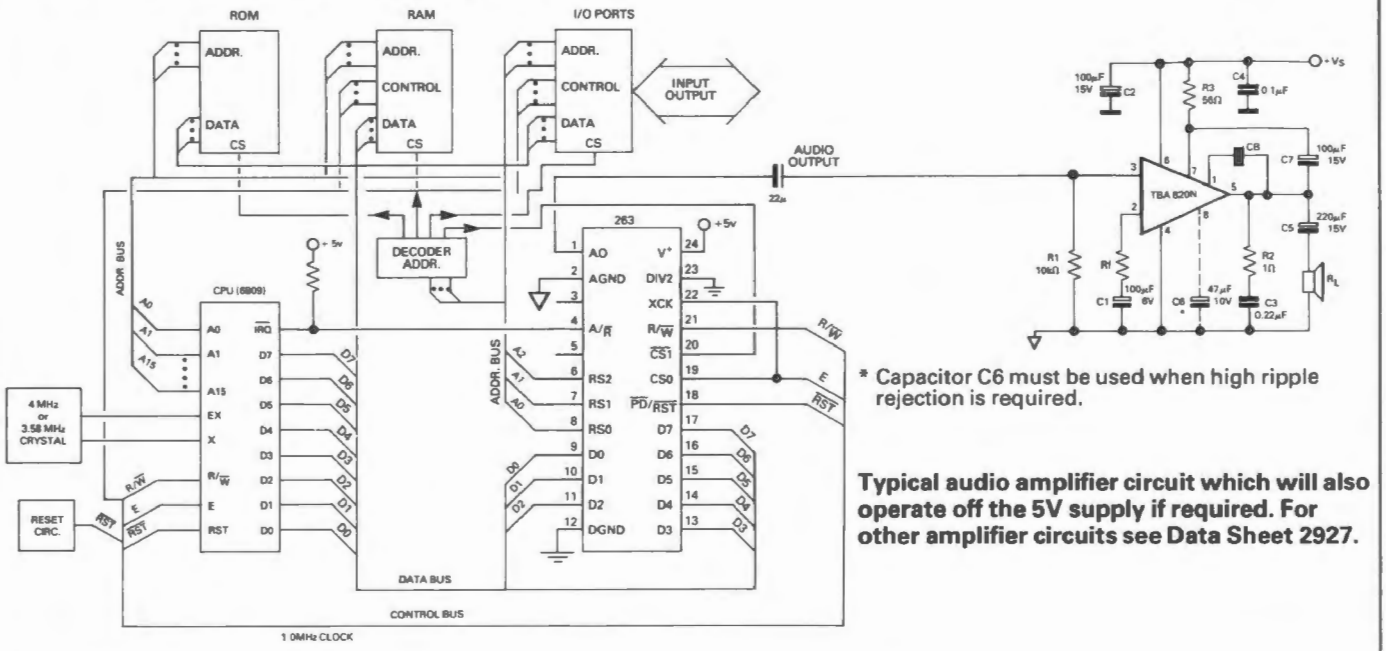
DR1, DR0 Define the phoneme duration.
P5 → P0 . . Address the phoneme required.
I11 → I0 . . Define inflection target frequencies and rate of change.
R3 → R0 . . Define the rate or speed of speech.
CTL . . . . . Define the mode of A/$\overline{R}$ response in conjunction with DR1 and DR0. Also directly set by $\overline{PD}$/$\overline{RST}$.
T2 → T0 . . Define the rate of movement of the formant position for articulation purposes.
A3 → A0 . . Define the amplitude of the output
F7 → F0 . . audio.
Define the frequency of all vocal tract filters.

Table 5

Mode Selection

DR1	DR0	'CTL' BIT	Function
H	H	H ⟶ L	A/$\overline{R}$ active, phoneme timing response, transitioned inflection (most commonly used mode).
H	L	H ⟶ L	A/$\overline{R}$ active, phoneme timing response, immediate inflection.
L	H	H ⟶ L	A/$\overline{R}$ active, frame timing response, immediate inflection.
L	L	H ⟶ L	Disables A/$\overline{R}$ output only, does not change previous A/$\overline{R}$ response.

Figure 4 **Typical microprocessor implementation**



* Capacitor C6 must be used when high ripple rejection is required.

Typical audio amplifier circuit which will also operate off the 5V supply if required. For other amplifier circuits see Data Sheet 2927.

A guide to phonetic programming using the 263

Phonetics

Every speech sound (phoneme) in any language may be represented by a special symbol (phonetic symbol). These symbols are used in WRITING precisely the sound sequence (phonetic transcription) of a word according to the way it is pronounced. There are many different phonetic symbol sets (phonetic alphabets). Each would contain a minimum number of symbols to represent the basic sounds (phonemes) required to pronounce any word in the language. Additional symbols are usually included which represent sounds with slight to great variations in the basic sounds (allophones). These symbols are used to assist in the transciption of words that reflect a regional, dialectic, or foreign pronunciation.

The process of transcribing a spoken word into its phonetic components begins with identifying the number of sounds in the word, then tagging each with a label to specify its type. Consonants and vowels are the most familiar labels but these may be broken down into subtypes (eg., stop consonants, back vowels, etc.) as the need for greater accuracy arises. Once the sounds have been identified, their symbols are selected, then written in sequence. The resulting transcription should allow another person to identify the pronunciation without having heard the word spoken.

Note that when using a phonetic alphabet to transcribe words into their sound sequences, there is not a one-to-one correspondence between the alphabet characters (orthographics) used to spell words and the phonetic symbols (phonetics) used to represent their pronunciations. For example, in the word 'phones' there are 6 letters but only 4 sounds. Conversely, the word 'I' has 1 letter but 2 sounds. It may be of some assistance to keep a dictionary handy for reference. Dictionaries use their own phonetic system to describe the pronunciations of every word entry. It will be necessary to learn at least one phonetic alphabet in order to engage in phonetic transcription. The 263 Phonetic Alphabet is the reference used in this manual. However, if another system is already known, it is easily translated into the reference.

When transcribing vocabulary from orthography (standard alphabet spelling) to phonetics, it is common to place the phonetic sequence between right slash marks when the transcription appears in running text. The word 'phones', for example, would be transcribed as /F O N Z/ when using 263 phonetic symbols. This allows the reader easier identification of phonetic segments.

263 Phonetic alphabet

The phonetic alphabet used to represent the 263 phonemes is the 263 Phonetic Alphabet. Refer to the Phoneme Chart Table 2 for a complete listing of the phoneme symbols.

Of the 64 alphanumeric symbols in the 263 Phonetic Alphabet, 34 represent sound BASIC to the pronunciation of American English. The remaining 30 symbols fall into 2 groups: the ALLOPHONE group and the NO-SOUND group. The BASIC sound symbols are:

A, AE, AH, AW, B, D, E, EH, ER, F, HF, I, J, K, KV, L, M, N, NG, O, OO, P, R, S, SCH, T, TH, THV, U, UH, V, W, Y, Z.

Symbols in the ALLOPHONE group represent speech sounds that vary in pronunciation from one of the basic sounds. They may be used in transcribing words or word segments (syllables or morphemes) whose pronunciations are not satisfied by the basic phonemes alone (words rooted in a foreign language, words adapted by a regional dialect, etc.). The ALLOPHONE symbols are:

A1, AE1, AH1, AY, E1, E2, EH1, HN, HV, IE, IU, IU1, L1, LB, LF, OU, R1, R2, U1, UH1, UH2, UH3, Y1, :A, :OH, :U, :UH.

The NO-SOUND symbols represent silent states. One of these symbols represents a 'pause' state. It is used to separate phoneme sequences into phrase-like segments which assist in more closely imitating the natural pausing in human speech for breathing or for delayed emphasis. The 'pause' is treated as a phoneme when it is selected for a

transcription and will be subject to phoneme parameter programming. It has the ability to maintain the parametric levels of duration, inflection, amplitude, etc. during its silence, thus audibly affecting the movement of the preceding and following phonemes. Other NO-SOUND symbols represent 'hold' states. They are used in combination with BASIC phonemes or ALLOPHONEs to generate articulation variations on their pronunciations. The NO-SOUND symbols are:

HFC, HVC, PA.

Now that there is a tool to use for writing the sounds that are heard, the next stage is to identify the sounds that are produced by the 263 speech synthesiser.

263 Phoneme review

So far in this programme, it has been established that: (1) spoken words are made up of a series of sounds; (2) each speech sound in a language may be represented by an identifying symbol; and (3) the spoken word may be written according to its sound sequence using these special symbols. Before a word may be written phonetically, however, users may wish to study further the 263 speech sounds. What makes one sound different from another and how these differences may be helpful to phonetic programming will be essential information for phonetic programmers.

The sound that is represented by each phonetic symbol in the 263 Phonetic Alphabet must be audibly learned. The easiest way to approach this task is to start with the sounds already known and associate a symbol with them. For example, from spelling we have already learned that vowels may be 'long' or 'short' and are often differentiated by their particular spelling formats. Every time a word with a 'short a' sound is heard (sat, fat, cat, bat, happy, plaster, ankle, Saturday, amplify, contaminate, etc.) the symbol /AE/ should come to mind. A 'long a' sound (fate, state, bait, lace, maybe, stable, arrangement, etc.) is actually a diphthong (two sounds combined into a single unit) and may be represented by the symbols /A AY/.

In standard orthography, there are only 5 vowel letters to represent 17 vowel sounds. In phonetics, each vowel sound will be represented by its own symbol or symbol combination.

Again from spelling, we have learned that the letter 'c' may have a hard sound as in 'cat' or a soft sound as in 'city'. The hard sound is actually a /K/ as in 'kite' and the soft sound is an /S/ as in 'sing'. Users must identify which sound (/K/ or /S/) is used in the transcription of a 'c'. You will not find a symbol C in a phonetic alphabet. Like 'C', letters 'Q' and 'X' will not be found in phonetic alphabets. They are transcribed into the sound sequences /K W/ and /K PA S/. Refer to the Phoneme Chart during this learning period. It provides example words to describe the pronunications corresponding to each symbol.

Users may add more words to the examples above to continue identifying the symbol-sound relationship for /AE/ and /A AY/. Follow this technique for each symbol in the alphabet. For auditory verification, enter the sound that is being reviewed into the device. Speak aloud your example word for the 263 sound in an attempt to match that which the synthesiser is emitting.

Example: /E/ = 'long e' vowel sound
= meat, read, need, repair, before, phoneme, erase, brief, people, timeliness, seniority, receive, catastrophe.

Example: /F/ = 'voiceless fricative' consonant
= farm, false, aft, feet, finger, phrase, phone, Africa, alphabet, cough.

Once users have reviewed auditorily the sounds they already had a familiarity with from spelling, proceed to the BASIC sound list on the above text and continue the review. Be aware that several consonant sounds will not provide outputs unless they have another sound following. This is the case with /B/, /D/, /P/, /T/, and /K/. When one of these sounds is entered into the 263, follow it by a vowel and listen to both in sequence.

Users who already have a familiarity with phonetics and 263 synthetic sounds, may wish to follow the sound review procedures in order to auditorily determine the difference between two sounds or identify new ones. For example, enter the /UH/ phoneme into the device. Then enter /UH1/, /UH2/, and /UH3/. Listen to each sound noting the pronunciation variations. Be aware that there are no duplicate sounds resident on the 263 chip.

Whenever a 263 sound is audited that cannot be readily identified as to its appropriate usage, do not be concerned. The review is designed only to provide a method for establishing an auditory memory for each sound and a visual memory for its symbol. Phonetic programming may begin anytime after the initial review. Return to the review later as your familiarity with the BASIC sounds increases and as your need for sound alternatives to those BASIC sounds becomes more apparent.

If there is question as to which symbols should be chosen to transcribe a word into its sound sequence, make a written note circling the letter(s) that present the problem. Later, when phonetic programming has begun, a phoneme sequence may be created for the word and users may verify auditorily which phonetic selection produces the most appropriate translation.

263 Phoneme discussion

The 263 Phonetic Alphabet is divided into 3 groups for the purpose of differentiating between phonemes and allophones. Another way of dividing the Alphabet is according to usage. The most familiar division is a two section split: CONSONANTS sounds and VOWELS sounds. Within each of these sections, sounds may be further subdivided according to the distinctive features that best describe the sounds phonetically or acoustically. The more that is known about a sound, the easier it is to determine how it may be used in transcribing and phonetically programming a word.

———CONSONANT Sounds———

There are 22 Consonant Phonemes, subdivided according to their manner of production in the human speech mechanism. Some are characterised by the noise emitted when the articulators obstruct the air flow (Fricatives like /S/). Vowel-like consonants have the least amount of obstruction and may occasionally be used as vowel substitute. Stop consonants are obstructed completely, re-

lease of air flow occurring at the onset of the next sound. Notice that Affricates are a sequence of 2 sounds (a Stop followed by a Fricative) spoken as a single unit. Unlike vowels, which always have a vocal source during production, consonants may be voiced (V) or unvoiced (U) (no vocal source during air flow). When listening to the manner in which a consonant is produced during speech, note its special characteristics that distinguish it from all other consonants. Table 6 displays all of the consonant sounds within their production groups.

Table 6

Consonant chart

	stops	fricatives	affricates	semivowels	glides	nasals
voiced	B, D, KV	Z, V, J, THV	(D, J)	R, L	W, Y	M, N, NG
voiceless	P, T, K	S, F, SCH, TH, HF	(T, SCH)			

Voiced and voiceless consonants are subdivided into 6 categories according to the manner in which they are produced in the human vocal tract: ie. how the air flow is obstructed by the articulators to make each sound different.

Consonant sounds are selected for a sequence in much the same manner as an alphabet character would be selected for the spelling of a word. Users must be alert, however, to identify the exceptions. Occasionally, a consonant appears in the spelling of a word but not in its sound sequence: the 'b' in 'comb' is not pronounced and the sound sequence reflects the absence of the 'b': /K OU M/. Some exceptions have grammatical rules that may be used in determining the appropriate sound. For example, a consonant may have 2 pronunciations according to its sound environment. The 's' used to pluralize the two words that follow are pronounced differently based on whether the sound that precedes it is voiced or unvoiced. An 's' pronunciation will match the voicing characteristics of the sound it follows.

Examples tips = /T I P S/
tabs = /T AE B Z/

There are other types of consonantal exceptions. For example, the 't' in a word like 'nation' is pronounced /SH/ and the program might look like this: nation = /N A AY SH UH3 N/. Users must listen to each word's pronunciation to determine the appropriate selection.

There are 7 Consonant Allophones, each noted in the table below. The /L/consonant is used in the initial position of a sequence for words beginning with 'l', while the /LF/ allophone will occupy a medial or final position in a sequence: eg., lull = /L UH LF/. The /LB/ and the /L1/ allophones would be used when a most constricted pronunciation of an 'l' was required, as would occur for some words of foreign languages.

Consonant phoneme	Consonant allophones	Consonant phoneme	Vowel allophone
L	L1, LB, LF	R	ER
R	R1, R2	Y	YI

ALLOPHONE LISTING FOR /L/, /R/, & /Y/

The /R/ is an initial position phoneme. Both /R1/ and /R2/ have more constricted pronunciations than /R/ and may be used in sequence with soundless interrupts to create a trilled /R/. Often when the /R/ is required in a medial or final position, it is vowelised and the /ER/ is used. Listening to the production of all four of these sounds will auditorily show that they may, occasionally, be used interchangeably.

Examples red = /R EH D/
bird = /B ER D/
motor = /M OU T ER/

The /Y/ consonant, used as the final sound in words ending with 'y', has a vowel allophone that may be used as the initial sound of words starting with 'y'. Note that both /Y/ and /Y1/ are auditorily very close to the /E/ and the /IE/ vowels and may be considered interchangeable.

———VOWELS Sounds———

There are 12 BASIC Vowel Phonemes. Vowels are subdivided according to the manner in which they are produced. All vowels are voiced sounds but each has a different output based on the degree of obstruction created by the opening of the mouth and the tongue position. Lip positions, another obstructing articulator, may range from spread flat to round. While the lips are in any of these positions, the jaw may be simultaneously dropped from a closed to an open position.

	Front Vowels	Medial Vowels	Back Vowels
	SPREAD ← →		ROUNDED
CLOSED	E		U
↑	I		OO
	A	UH	O
↓	EH	(ER)	AW
OPEN	AE		AH

Vowel quadrilateral

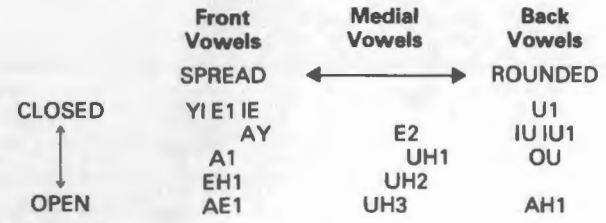
Vowels begin their production with the same voiced energy. Changes in the position of the tongue (front or back), the shape of the lips (from spread flat to rounded), and the position of the lower jaw (from closed to open) determine the final characteristics that allow listeners to distinguish between vowel sounds.

Refer to the 263 Phoneme Chart for the pronunciation reference on each BASIC vowel sound. Utilise the sound review techniques on the previous pages to practise identifying the vowel sounds in words and associating them with their phonetic symbols.

The allophonic variations of vowels, 20 in number, are used in a phonetic program to enhance the pronunciation of a word. There are some cases where the allophone is required for articulate pronunciations. This is true for /AY/, /YI/ and /IU/, which are integral components in the phonetic sequences for the 'long a' and the varied 'long u'.

Examples same = /S A AY M/
you = /YI IU U/

The next table places each allophone into the vowel quadrilateral to demonstrate approximately how they might relate to the BASIC vowels. Users are in no way restricted to traditional transcriptions that use only the BASIC vowel phonemes. Be encouraged to experiment with allophones. Place them in different positions in a sequence to auditorily check how they effect the overall pronunciation of a word.



Allophone placement in vowel quadrilateral

Vowel allophones are placed in the vowel quadrilateral according to their production features. The sounds they emit vary slightly from the BASIC vowels that occupy the same positions.

Four vowel allophones – /:A/, /:OH/, /:U/, and /:UH/ – are adapted pronunciations of four of the BASIC vowels. These sounds are most commonly used for phonetically programming a foreign word. They may also be used as transitory sounds to link phonemes with opposite production features such as a round, open vowel with a very constricted, narrow consonant.

There are five vowels that require two or more vowel sounds in sequence in order to achieve their pronunciations. These are generally referred to as diphthongs. Refer to the Diphthong Conversion Chart.

The vowel quadrilateral is a handy tool to use for selecting vowel phonemes for diphthongs and other multi-phoneme units. For example, the diphthong in the word 'I' starts with an /AH/ and ends with an /E/. In order to move smoothly from the first sound to the second (transition), another vowel may be inserted between these two sounds in sequence. The most likely choice would be a vowel that falls somewhere between /AH/ and /E/ in the quadrilateral: eg., /UH/, /EH/, /I/, etc. The sequence may look like this: /AH EH E/ or /AH1 UH3 IE/ or /AH1 EH3 AY/. In their fullest durations, a three-sound sequence would over articulate the diphthong. Shortening the first and last sounds by 1 duration and the medial sound by 2 durations will produce a more acceptable pronunciation (see 263 Phoneme Parameters).

263 Phoneme parameters (attributes)

To achieve an accurate pronunciation of a word produced by the 263 synthesiser requires more than a selection of the appropriate phonemes. Like human speech sounds, synthesised sounds are further defined by the rate at which they are emitted (duration), the level of pitch at which they are emitted (inflection or frequency), and the intensity with which they are produced (amplitude). These are considered the three major speech parameters which give the overall production of a word its linguistic character, transforming simple speech into more complex language. Inflection, amplitude, and duration are only three of the parameters that users have control of during the programming process. The rate at which one sound moves into another (articulation) is also a controllable parameter. Other parameters are: the slope of the inflection (slope), the rate of each selected duration (rate), and the extended inflection frequencies (extension). Users may also select the base frequency at which speech may be produced (filter frequency). Refer to 263 Phoneme Parameters, the range of each and typical default values selected.

Every phoneme selected for a sequence must be accompanied by assignments for each of the eight parameters. As users become more aware of their need to create different language effects with their synthesised speech output, they will require the flexibility and choice that comes with programmable parameters. For example, with 4 selectable durations per phoneme, each actual pronunciation of each sound may be changed. Thus, every sound has four possible outputs increasing the user's choice from 64 phonemes and allophones to 256. Each of the 256 may be affected differently by each of the 32 possible inflection assignments. Add to these possibilities 16 variations in amplitude and 16 variations in rate. The possible combinations are not limitless, of course, but they are very great and users are encouraged to experiment with as many as possible.

Several of the parameters affect synthetic speech output as a whole. These are articulation, pitch extension, and filter frequency. Users may select a single level at which to set the filter frequency, for example, and maintain that level throughout the programming process.

Phonetic programming methodology

Due to the great variety of phonemes and parameter choices, as well as the different effects the parameter selections have on the speech sounds, a systematic approach to selecting the variables is advised. The approach described below is only one of several that might be used. It may be adjusted to accommodate the user's special programming style or to accommodate later implementation of automatic control techniques.

The first step is to transcribe the target word, phrase, etc. into its basic phonetic components. Next, enter these sounds into the 263 and auditorily check the output. Use the default values suggested in the Nominal Phoneme Parameter Table 7. The results should be a bit stilted if not misarticulated for the first trial program. Phoneme adjustment is next. Continue to make changes in the phoneme sequence, auditorily monitoring the changes, until an adequate pronunciation of the target is established.

Begin parameter adjustments. First, maintain articulation, pitch extension and filter frequency at nominal values. The device should be kept in the transitioned inflection mode. Make adjustments in the levels of only one of the remaining 4 parameters at a time, beginning with the duration and moving on to the inflection, rate, and amplitude (in that order) once the specific effect that the parameter can make has been made. Return to a previously adjusted parameter at any time based on need.

263 Diphthong conversion chart

Phoneme sequence	Example words
A AY Y	rain, became, stay
A IE EH1 UH3 LF	mail, hale, avail
AH1 AE1 EH1 Y	time, rhyme, sky
AH1 EH1 IE AW UH3 LF	smile, style, while
AH1 EH1 IE UH3 ER	fire, liar, inspire
UH3 AH1 Y	mice, right, sniper
O U	road, stone, lower
OU O O	tore, four, floor
AH1 AW O U	loud, flower, hour
UH3 AH1 O U	house, about, ouch
O UH1 AH1 I IE	boy, noise, annoy
O UH3 EH1 I OO LF	boil, spoil, doily
IU U U	tune, spoon, do
YI IU U U	you, few, music

RS data

263 Multi-unit conversion chart

Phoneme sequence	Example words
T HFC SCH	church, latch
KV HVC HF	good, lag, angry
D J	just, ledge, wage
KV HF HFC	lake, corn, check
P HF	pipe, pay, poor
K HF W	quest, quick, aqua
T HF	top, trip, strain
HFC K HF HVC S	six, exit, taxi

Table 7

Nominal Phoneme Parameter

(Suggested default values for speech development)

Amplitude (A3→ A0)
Range – 0 to F (softest to loudest, 0 = silent)
Default – C
Exceptions – KV = 0, B = 6, D = 6

Duration (DR1, DR0)
Range – 3 to 0 (shortest to longest)
Default – 0

Filter frequency range (F7 → F0)
Range – 00 to FF (lowest to highest)
Default – E9

Inflection (pitch) (I10 → 16, Transitioned inflection mode only)
Range – 0 to 1F (lowest to highest, 0 = silent)
Default – 04

Extension and range of pitch (I11, 12 → I0)
Range – 0 to 7 (low); 8 to F (high)
Default Value – 8

Rate of speech (R3 → R0)
Range – 0 to F (slowest to fastest)
Default – A

Slope of inflection (I6 → I3, Transitioned inflection mode only)
Range – 0 to 7
Default – 0

Articulation (rate of) (A3 → A0)
Range – 0 to 7 (slow to fast)
Default – 5

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RS data

'Ferroxcube' switched-mode power supply cores

Stock numbers 228-264 & 228-270

These components are recognised industry-standard parts used for output transformer service in switched-mode power supplies and other high frequency applications where high operating flux and low core losses have to be maintained, even at elevated temperatures. Maximum power throughout is dependent on the switching frequency and the output voltage, as well as the permissible temperature rise. As a guide, in the stringent case of a 5V dc output, transformers based on these cores can supply 100W (FX3730) or 50W (FX3720).

Each kit comprises two E-cores in grade 3C8 (A16) Ferroxcube and one bobbin of black maranyl. Brass studding (refer to the current RS catalogue) may be used as a mounting aid: M2·5 for DX3730, M2 for FX3720.

Assembled kit

Exploded view

Nominal design data for a pair of cores

Parameter	Symbol	FX3730	FX3720	Unit
Stock number		228-264	228-270	
Total ferrite volume	—	12,600	7,780	mm^3
Centre pole volume	V_{cp}	2.950	1,740	mm^3
Back and leg volume	V_b	9,650	6,040	mm^3
Centre pole area	A_{cp}	106	71	mm^2
Minimum centre pole area	A_{cp} min	100.3	66.5	mm^2
Total back and leg area	$2 \times A_b$	130	96	mm^2
Total surface area of fully wound core	A_c	5,900	4,350	mm^2
Mean turn length	l_w	60	50	mm

Electrical and magnetic properties of a pair of cores

To avoid core saturation it is essential that the flux density in the centre pole does not exceed 320 mT (at a core temperature of 100°C).

Parameter	Temperature (°C)	Frequency (Hz)	NI (A)		Effective flux density $\hat{B}_e$* (mT)	Value	
			FX 3730	FX 3720		FX 3730	FX 3720
Amplitude permeability (μ_a)	25 100	<100 <100	– –	– –	300 230	>1,000 >1,000	>1,000 >1,000
$\frac{V.t}{N}$ (= Φ)	25 100	<100 <100	21.4 16.1	18.6 13.9	– –	>36.3 μVs >27.8 μVs	>25.3 μVs >19.4 μVs
Effective total loss (P)	25 100	25k 25k	– –	– –	160 160	<2.2W <2.2W	<1.1W <1.1W

$$*\hat{B}_e = \sqrt{2}\,\frac{V}{\omega A_e N}$$

Definition of $\frac{V.t}{N}$ (= Φ)

The total flux (in webers) due to the application of a constant voltage V to a winding of N turns for a time t, the flux being zero at t = 0. In the following graphs this parameter is expressed in μVs or $\mu\omega$b.

Legends:

$\hat{B}_e$ = Maximum instantaneous value of alternating flux density in milliteslas.

V = Step or peak amplitude voltage.

ω = 2π x (f the alternating frequency).

Effective parameters

For calculating the magnetic properties of a pair of cores the following parameters should be used.

Parameter	Symbol	FX3730	FX3720	Unit
Effective magnetic path length	l_e	89.3	77.4	mm
Effective area of magnetic path	A_e	121	84.3	mm^2
Effective magnetic volume	V_e	10,800	6,530	mm^3
$\sum \frac{l}{A}$	C_1	0.735	0.918	mm^{-1}

Physical dimensions

Figure 1 **FX3730**

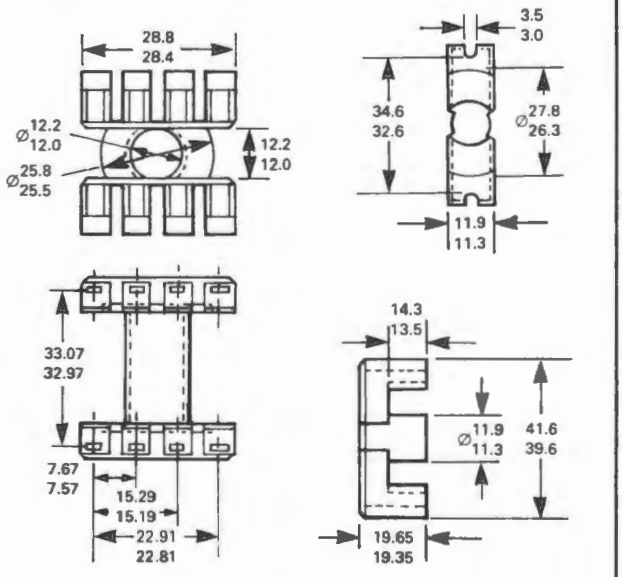
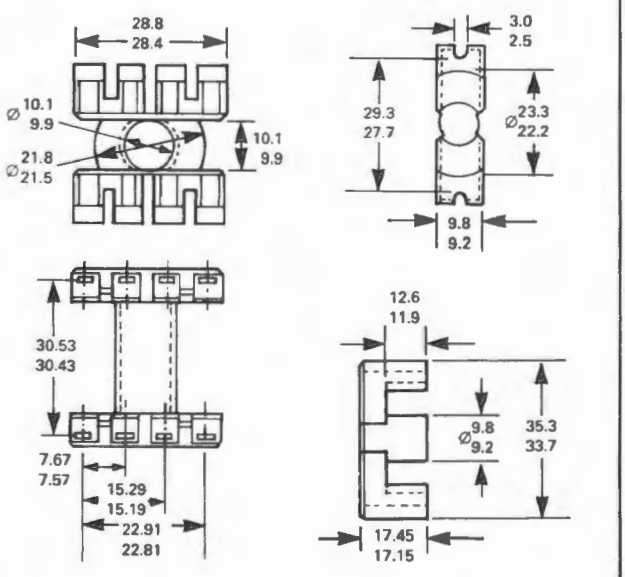


Figure 2 **FX3720**

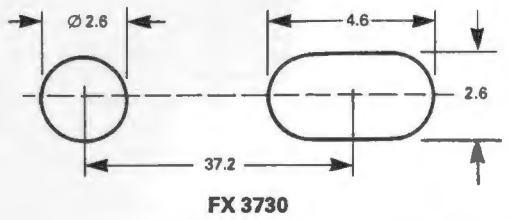


Assembly and mounting

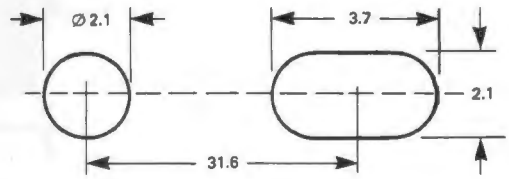
The wound coil former and cores may be assembled by means of non-magnetic M2 screws or studs along the grooves provided. The use of a clamping bar is strongly recommended to ensure that the maximum clamping force of 200N (≃ 20kgf) is uniformly distributed over the cross-section of the outer poles.

The assembly studs can be extended for mounting purposes or to support another sub-assembly.

Figure 3 **Recommended piercing diagrams**



FX 3730



FX 3720

Application data for symmetrical magnetization

FX 3730

Figure 4 **Typical magnetization curves for a pair of cores with ambient temperature as parameter**

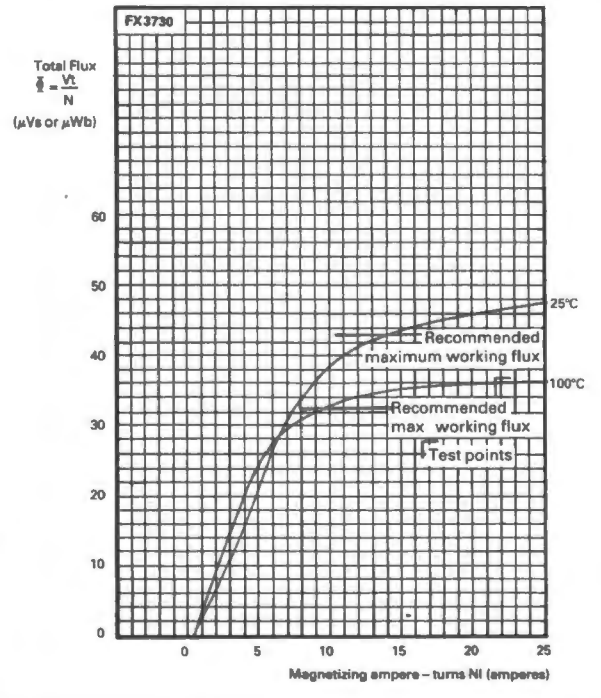


Figure 5 **Total flux as a function of core temperature**

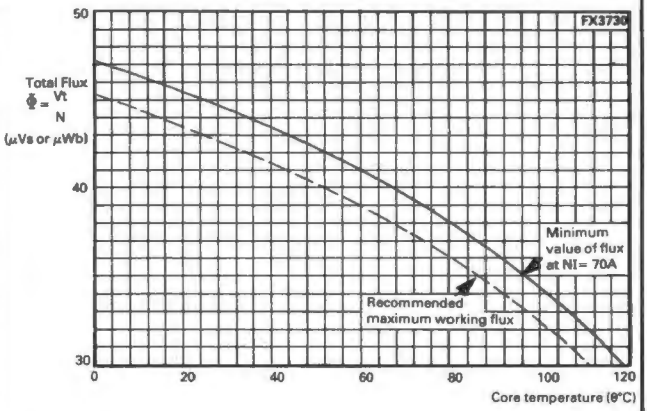


Figure 6 **Core loss as a function of total flux at 100°C with frequency as parameter**

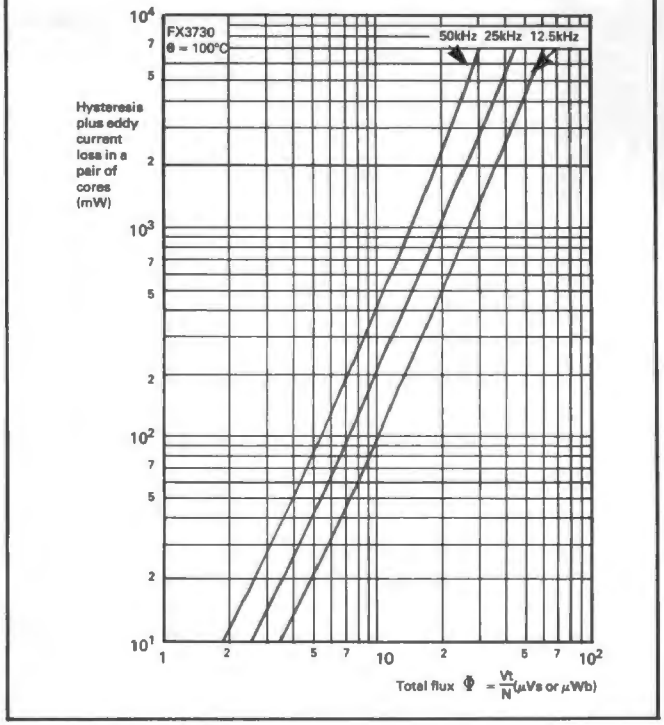


Figure 7 **Typical transformer temperature rise as a function of total transformer loss in free air conditions**

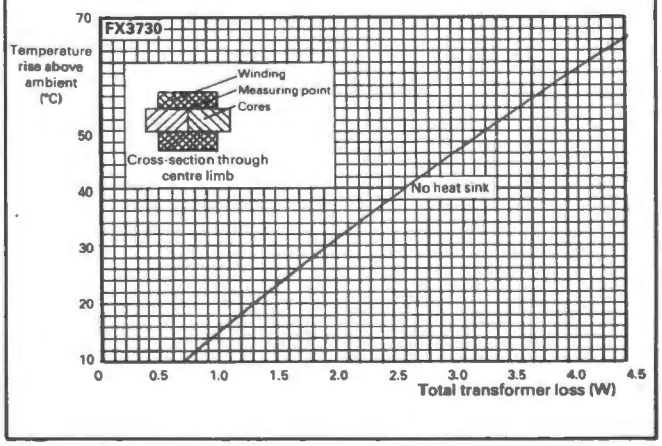


Figure 8 **A_L Based on a typical initial permeability of 2000 as a function of spacer thickness**

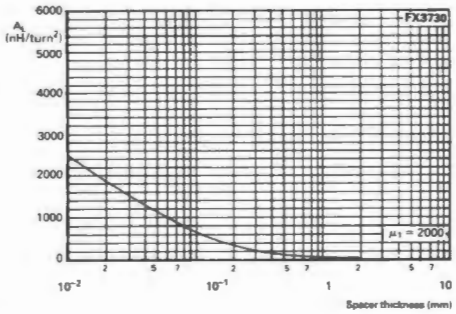
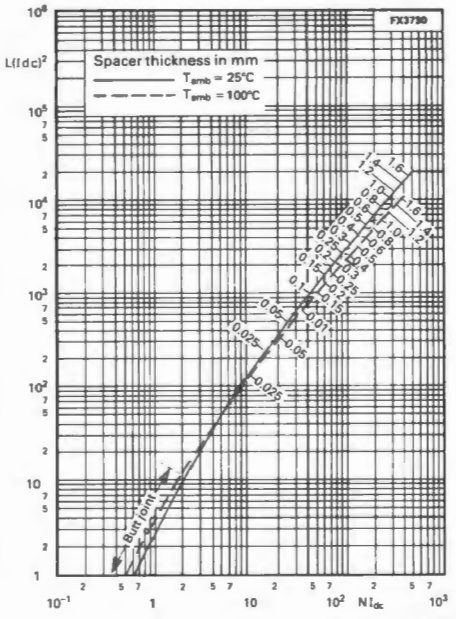


Figure 9 **Hanna curves**



I_{dc} = current in amperes N = number of turns L = inductance in micro-henrys

For convenience in the design of inductors carrying direct current, Hanna curves may be used to determine the magnitude of the magnetic circuit gap to avoid case saturation.

FX3720

Figure 10 **Typical magnetization for a pair of cores with ambient temperature as parameter**

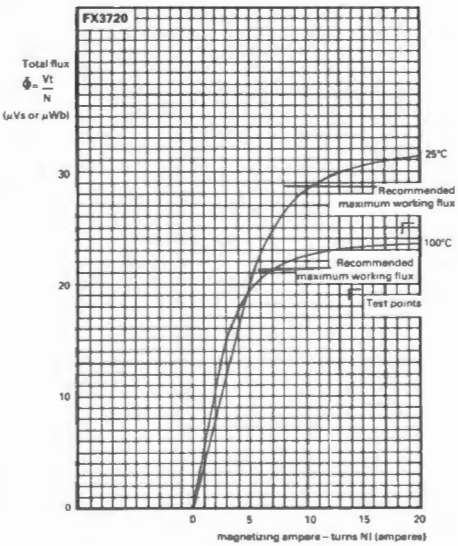


Figure 11 **Total flux as a function of core temperature**

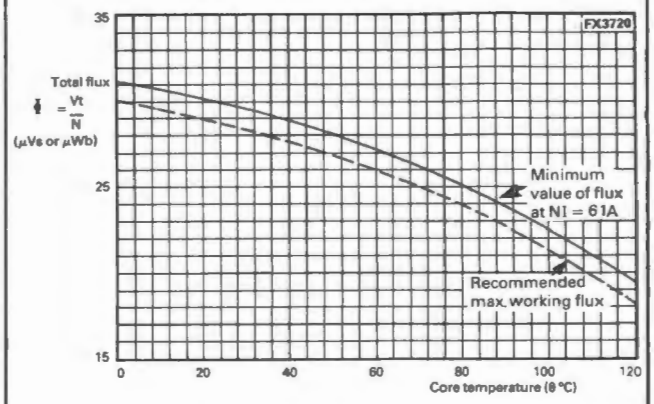


Figure 12 **Case loss as a function of total flux**

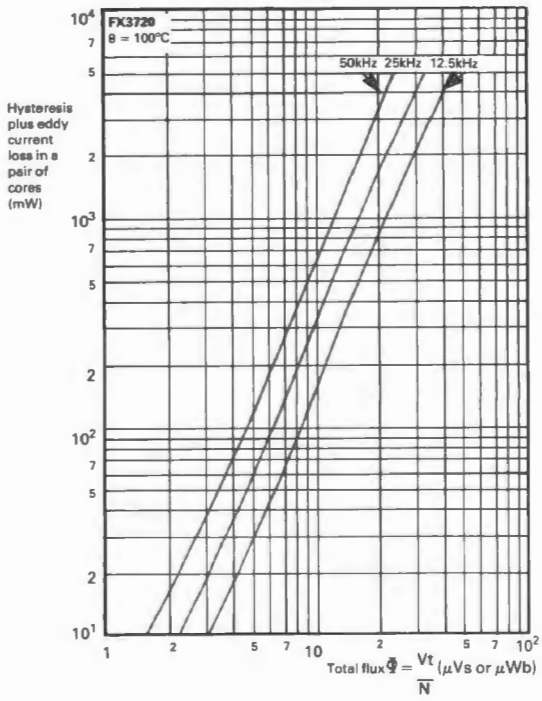


Figure 13 **Typical transformer temperature rise as a function of total transformer loss in free air conditions**

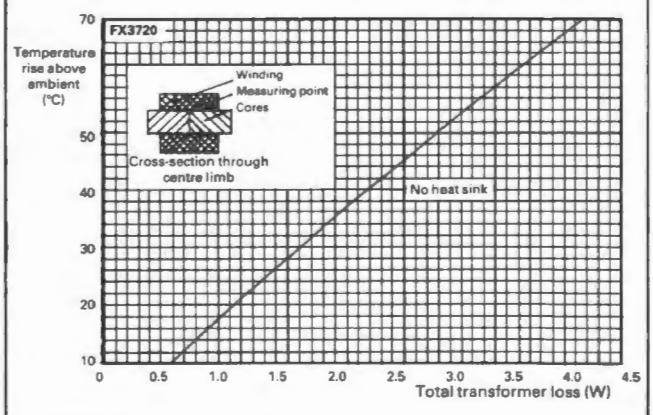


Figure 14 **A_L Based on a typical initial permeability of 2000 as a function of spacer thickness**

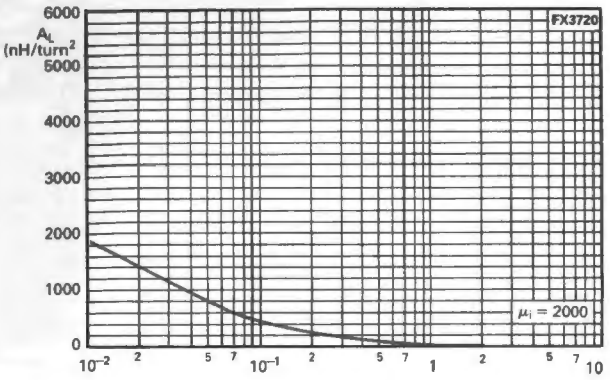
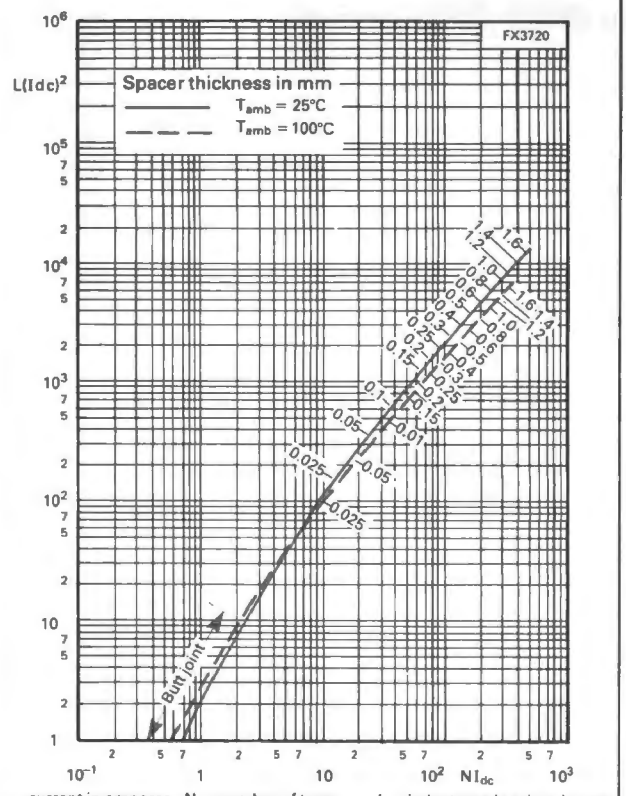


Figure 15 **Hanna curves**



I_{dc} = current in amperes N = number of turns L = inductance in micro-henrys

For convenience in the design of inductors carrying direct current, Hanna curves may be used to determine the magnitude of the magnetic circuit gap to avoid case saturation.

Worked examples utilising Ferroxcube FX 3720

a. **General purpose low stored energy inductor calculators**

Where the peak flux excursion does not exceed the magnetising curves shown in Figure 10, the turns requirement for an ungapped core inductor can be obtained directly using the figure for A_L (nano henrys/turn^2).

Note. FX3730 offers a 50% increase in peak working flux over the FX3720).

b. **Calculations for inductors carrying a dc component**

When the value of dc in an inductor could lead to core saturation, the design can be modified to include a small air gap in the magnetic path. To simplify the calculation of turns and spacer requirements, the Hanna curves in Figure 15 can be usefully employed.

Example: design requirement is for a 150μH smoothing choke, carrying a dc component of 0.6A, with a peak ripple current of 1.0A. The choke is to have an overload capacity of 25% and an ambient operating temperature of 25°C.

Referring to Figure 15, taking a peak current for the choke of 2 amps [(1 +0.6) +25%] gives an $L1^2$ (figure of merit) of 600 and an optimised spacer thickness around 0.08mm. Relating the latter to Figure 14 a modified value for A_L is obtained around 500nH/turn^2 being only 25% of the ungapped value for the core.

$$\text{Hence } N = \sqrt{\frac{L}{A_L}} = \sqrt{\frac{150 \times 10^{-6}}{500 \times 10^{-9}}} = 17 \text{ turns}$$

NI for the peak current of 2A is therefore 34.

With an ungapped core this value of magnetising ampere turns would put the core into the saturated state (see Figure 10). However with the introduced air gap, the effective NI is reduced from 34 to approximately 9 (A_L being reduced to 25% of that for an ungapped core). From Figure 10 a total flux of 25μWb is obtained for the new NI figure of 9.

c. **Using the other curves**

Let us assume that the frequency of the power source is 50kHz and a stated ripple current of 1A and overload of 25% the peak current excursion is 1.25A. The excursion would correspond with flux change of 15μWb and from Figure 12 projects a core loss of 1.5 watts. Copper loss is negligible as 17 turns of 2mm dia wire would have a resistance of less than 10mΩ and thus the value of I^2R would be small.

RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

Dot matrix printers and accessories

This data sheet covers the following stock numbers:

Stock No.	Description
630-774	RS105 Printer, 80 Column
630-780	RS105 Serial Interface
630-796	RS105 Ribbon
630-011	RS160 Printer, 80 Column
630-027	RS160 Serial Interface
630-033	RS160 Tractor
630-049	RS160 Ribbon
630-055	RS160-15 Printer, 136 Column
630-061	RS160-15 Serial Interface
630-077	RS160-15 Ribbon

Features

- High quality serial impact dot matrix printers
- 9 x 7 dot character structure
- Near letter quality mode
- Long-life 9 pin head
- Quiet mode
- Compact, robust design
- Tractor feed (standard in RS105 and RS160-15, optional for the RS160)
- Pin feed (standard in RS160)
- Friction feed
- Bidirectional logic seeking
- Programmable bit image graphics
- ®IBM PC compatible (RS160 and RS160-15)
- Subscripts and superscripts
- True descenders
- Proportional spacing
- Programmable character styles
- User definable download characters
- 9 International character sets
- 2k Bytes buffer expendable to 8k Bytes with ic 301-870 (refer to Semiconductors section of current RS catalogue) – see respective printer manual for installation details
- Self-test mode
- Printer functions set by easily accessible dil switches.

Figure 1 **RS160-15 printer (630-055)**

Impact dot matrix printers

General

Impact printing is achieved by the action of a print head striking an inked ribbon located between the print head and the paper. For standard size printing 10 characters are printed per inch (ie. 10 cpi) with 80 or 132 characters on a line depending on the width of the paper. The line feed is normally 1/6in (ie. 6 lines per inch), but is reprogrammable.

Printing normally takes place after a complete line has been received, the characters being held in the printer buffer. The end of the line is indicated by a full line (say 80 or 132 characters) being received or a carriage return character. This carriage return will be interpreted either as a carriage return (only causing the printhead to return to the beginning of the line) or a carriage return and line feed depending on the the position of DIP SW 1-4. A line feed is always interpreted as a line feed. Therefore, if DIP SW1-4 is in the wrong position for a particular application this will cause double line spacing or continuous printing on the same line. Toggling DIP SW1-4 to its other position will solve the problem.

With the RS printers it is possible to set the line length by software using the left margin (ESC l + n) and right margin (ESC Q + n) commands. Also, with the RS printers it is possible to set the printer (using the incremental print and view, ESC i +n command) to a mode in which all characters are printed as they are received and the paper is moved up to display the text after an interval of 0.1s, and automatically moved back down for further printing.

Printhead

The RS needle printheads consist of 9 hammers. Each hammer comprising a wire and an electromagnetic solenoid. The solenoids are mounted radially, thereby reducing flexing of the wires and increasing reliability. Once one column has been printed the head moves on to the next column and so on. When a full character has been printed the head moves to the next character position and the process is repeated.

Figure 2 **RS105 printer (630-774)**

Bidirectional logic-seeking

The RS printers use microprocessor control to provide maximum throughput. The movement of the head is minimised depending on whether the next line should be printed left to right or right to left. Also, to increase speed, multiple spaces are combined into one operation. These two items require that a complete line of text must be received prior to printing, as is the case in normal text mode. Undirectional printing can be selected with an ESC U + n command.

Horizontal formatting

Up to 32 tab positions can be set along a line using the ESC D command. The horizontal tab character will then move the head to the next pre-set position. Upon power-up tab positions are set at every 8 characters. The left and right margin can also be set.

Figure 3 **RS160 printer (630-011)**

Vertical formatting

Vertical formatting commands include variable line feed settings, variable forward feed, variable reverse feed, variable page length setting, skip over perforation and vertical tab. For vertical tabbing, up to 8 sequences (channels) can be set with each sequence having up to 16 positions.

There is a command to select the channel and a vertical tab character will then move the paper to the next pre-set position. Upon power-up vertical tab is set at one line.

Character size

The normal character size (called, pica style) is 2.1mm (width) x 2.55mm (height). These characters are printed at a spacing of 10 characters per inch (10 cpi). Other styles available include élite (12 cpi), condensed pica, expanded pica, condensed élite etc. Various combinations of the above are allowed eg. it is possible to select both condensed and expanded at the same time and get a result somewhere in between but different from the normal character.

Subscripts and superscripts can also be selected.

Proportional spacing
With normal printing each character takes up the same amount of space on a line ie. the character 'i' takes up the same space as the character 'W'.

However, for better presentation it is sometimes desirable to print less-wide characters closer together. This is termed proportional spacing (or proportional printing) since the space allocated to each character is proportional to its actual width. With the RS printers proportional printing can be selected by the ESC p + n command.

True descenders
The RS printers use a column size of 9 vertical dots in the character structure allowing the use of true descenders in characters such as y or g where the tails descend below the writing line.

Download characters
It is easy to define special characters such as special scientific symbols and store these in the download character area. Thus a user could pre-define his own special characters and have them printed by single pre-defined character codes.

Programmable bit-image graphics
With the RS printers it is possible not only to define your own special characters but it is also possible to generate your own patterns or drawings by controlling each dot on the page. There are 5 different bit image graphic modes, each having a different horizontal dot density ranging from 60 dots per inch to 240 dots per inch.

Interfacing

Figure 4 **RS160 serial interface (630-027)**

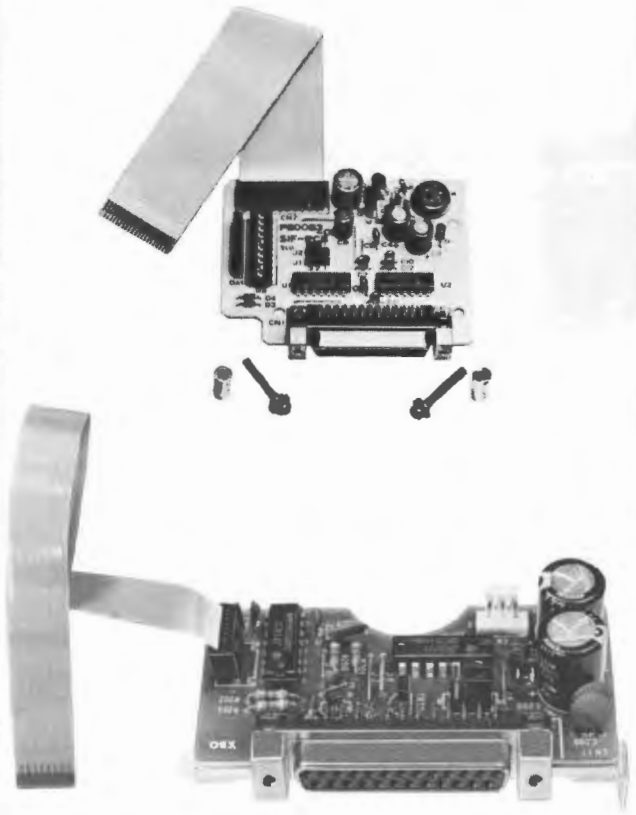
All printers are supplied fitted with an 8-bit Centronics compatible parallel interface.

An optional RS232 serial interface is available for each printer. All the interfaces conform to the following specification and are supplied complete with installation instructions.

Table 1 **Serial interface specification all printers**

Dil switch selectable options	
Baud Rates	150, 200, 300, 600, 1200, 2400, 4800 or 9600
Parity	Odd, Even or Off
Word length	7 or 8 bits
Stop bit	1 or 2 bits
Data protocol	Ready/Busy, Xon/Xoff or ETX/ACK

Figure 5



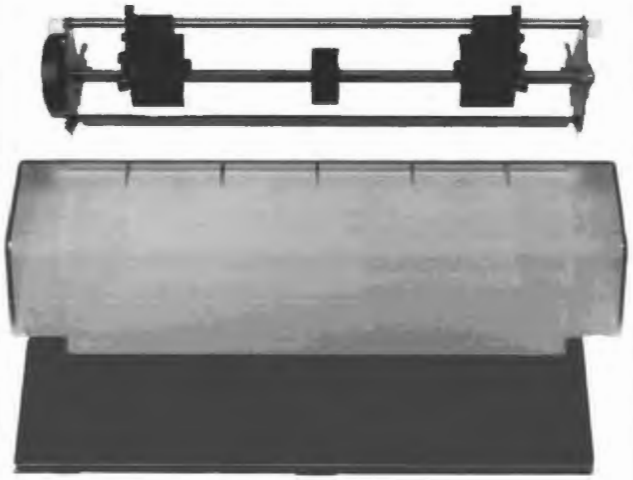
RS160-15 serial interface (630-061)

Paper handling
All three printers are fitted with a friction feed for single sheet or non-sprocket paper.

In addition the RS105 and RS160-15 are supplied with a tractor mechanism fitted as standard. This allows handling of sprocket paper between 4in and 10in wide (for the RS105) and 4in and 15½in wide (for the RS160-15).

The RS160 printer has a pin feed mechanism that can be used with sprocket paper between 9½in and 10in wide. Alternative paper widths between 4in and 10in wide can be accommodated in the RS160 by using the optional tractor unit (stock number 630-033).

Figure 6 **RS160 tractor unit (630-033)**



Note if the A4 size micro-perforation, 85gsm paper (stock number 620-632) is to be used with the RS160, the tractor option must be fitted, due to the paper width of 9¼in. However, normal 80 column listing paper (stock number 620-626) does not need the tractor option (since it is 9½in wide).

List of control codes

Code	Name
BEL	Bell
BS	Back space
HT	Horizontal tab
LF	Line feed
VT	Vertical tab
FF	Page feed
CR	Carriage return
SO	Double-width expanded characters
SI	Compressed characters
DC1	Device control 1
DC2	Cancels compressed characters
DC3	Device control 3
DC4	Cancels double-width expanded characters
CAN	Cancel
DEL	Delete
ESC SO	Double-width expanded characters
ESC SI	Compressed characters
ESC £ +n	Print mode selection
ESC #	Accepts eighth bit from computer
ESC % 0+n	Internal character set selection
ESC % 1+n	Download character set selection
ESC &+s+n +m+a+P_1+...+P_{11}	Download character definition
ESC *+m+n_1+n_2	Bit image mode select
ESC -+n	Underline mode set/reset
ESC /+n	VFU channel selection
ESC 0	Paper feed 1/8in setting
ESC 1	Paper feed 7/72in setting
ESC 2	Paper feed 1/6in setting
ESC 3+n	Paper feed n/216in setting
ESC 4	Italic character setting
ESC 5	Cancels italic character setting
ESC 6	Printable code area expansion
ESC 7	ESC 6 cancel
ESC 8	Paper-empty detect disable
ESC 9	Paper-empty detect enable

Code	Name
ESC :0+n+m	Copy of the internal character into the download character set
ESC <	Home head
ESC =	Sets MSB as 0
ESC >	Sets MSB as 1
ESC ? +n+m	Bit image mode selection and change
ESC @	Reset printer
ESC A+n	Paper feed n/72in setting
ESC B+n_1 +n_2...n_k+NUL	Vertical Tab set
ESC C+n	Page length setting by lines
ESC C0+n	Page length setting by inches
ESC D+n_1+n_2 n_k+NUL	Horizontal Tab set
ESC E	Emphasized printing
ESC F	Cancels emphasized printing
ESC G	Double-strike printing
ESC H	Cancels double-strike printing
ESC I+n	Control code selection
ESC J+n	Execution of print and forward paper feed
ESC K+n_1 +n_2	Single-density full-graphic assignment
ESC L+n_1+n_2	Double-density full-graphic assignment
ESC M	Elite size character assignment
ESC N+n	Skip perforation set
ESC O	Skip perforation cancels
ESC P	Pica size character assignment
ESC Q+n	Right margin setting
ESC R+n	International character set selection
ESC S+n	Super-/subscript character set
ESC T	Super-/subscript deactivate
ESC U+n	Uni-directional printing set/reset
ESC W+n	Double-width expanded character set/reset
ESC Y+n_1+n_2	Double-speed double-density full-graphic assignment
ESC Z+n_1+n_2	Quadruple-density assignment
ESC^ +m+n_1+n_2	9-pin Dot Image mode selection
ESC b+n+m_1+...m_k+NUL	VFU position set
ESC i+n	Incremental print
ESC j+n	Print and reverse feed
ESC l+n	Left margin setting
ESC m+n	Selection of character code table
ESC p+n	Proportion print set
ESC s+n	Half-speed assignment

Technical specification

Printer	RS105	RS160	RS160-15
Stock number	630-774	630-011	630-055
Printer speed	105cps	160cps	160cps
No. of columns	80	80	136
Paper feed			
Friction feed	•	•	•
Pin feed	–	•	–
Tractor feed	•	optional (630-033)	•
Programmable page length	•	•	•
Programmable page break	•	•	•
Programmable line spacing	•	•	•
1/6in	•	•	•
1/8in	•	•	•
7/72in	•	•	•
n/72in	•	•	•
n/216in	•	•	•
Programmable character styles			
Combinations	128	128	128
Pica	•	•	•
Elite	•	•	•
Condensed	•	•	•
Expanded	•	•	•
Emphasized	•	•	•
Double strike	•	•	•
Underline	•	•	•
Super/Subscripts	•	•	•
Italics	•	•	•
Proportional spacing	•	•	•
Download characters	•	•	•
Character sets			
®IBM Graphic characters	–	•	•
American	•	•	•
French	•	•	•
German	•	•	•
British	•	•	•
Danish	•	•	•
Swedish	•	•	•
Italian	•	•	•
Spanish	•	•	•
Near letter quality mode	•	•	•
Graphic modes			
60 dots/inch	•	•	•
72 dots/inch	•	•	•
80 dots/inch	•	•	•
90 dots/inch	•	•	•
120 dots/inch	•	•	•
240 dots/inch	•	•	•
Quiet mode	•	•	•
Interfaces			
Centronics parallel	•	•	•
RS-232C Serial (optional) – stock no.	630-780	630-027	630-061
Power supply, 240V ac	•	•	•
Power consumption	30W	70W	70W

RS data

Example printouts

Normal ASCII character set:

```
>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~ /"#$%
/0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstu
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdef
pqrstuvwxyz{|}~ /"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVW
```

IBM® character set:

```
>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~áióúñÑ
»▒▓│┤╡╢╖╕╣║╗╝╜╛┐└┴┬├─┼╞╟╚╔╩╦╠═╬╧╨╤╥╙╘╒╓╫╪┘┌
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdef
pqrstuvwxyz{|}~áióúñÑªº¿⌐¬½¼¡«»▒▓│┤╡╢╖╕╣║╗╝╜╛┐└┴┬├─┼╞╟╚╔╩╦╠═╬╧
ßΓπΣσµτΦΘΩδ∞ØϵΠ≡±≥≤⌠⌡÷≈° ∙·√ⁿ² ■ !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGH
RSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~áióúñÑªº¿⌐¬½¼¡«»▒▓│┤╡╢╖╕
```

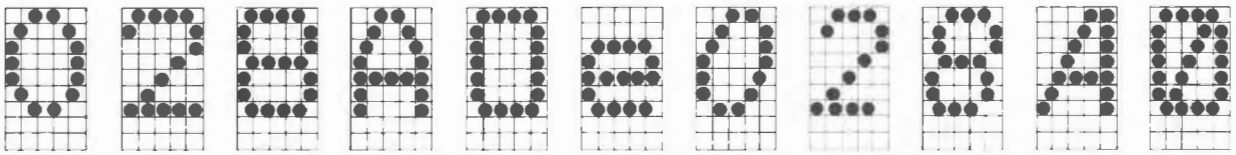
Near letter quality character set:

```
>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_'abcdefghijklmnopqrstuvwxyz{|}~ /"#$%
/0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_'abcdefghijklmnopqrstu
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_'abcdef
pqrstuvwxyz{|}~ /"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVW
```

The following details the difference between normal, near letter quality, emphasized and double strike characters. The RS range of printers will support all of these modes.

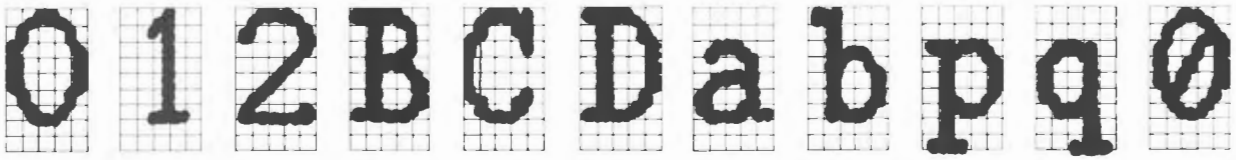
A **normal dot matrix** is printed in a matrix of 5 (horizontal) by 9 (vertical) dots with a dot spacing of one dot (horizontally and vertically). Character examples are shown in Figure 7.

Figure 7 **Normal dot matrix characters (note some characters are shown in italics)**



In **near letter quality** mode the dot spacing is one half dot (horizontally and vertically) as shown in Figure 8.

Figure 8 **Near letter quality characters**



In the **emphasized** mode, a normal character is printed and then printed again on top of itself but shifted one half dot to the right. The vertical dot spacing remains at one.

In the **double-strike** mode the character is simply printed again on top of itself, producing a bold image. Characters will appear wider in emphasized mode than in double-strike mode.

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RS data

Micropower adjustable voltage regulators RS7663B and RS7664B

Stock number 630-718 and 630-724

One positive (RS7663) and one negative (RS7664) adjustable voltage regulator providing output voltages from 1.6V to 10V at currents up to 25mA.

Fabricated in CMOS the operating current is typically less than 4μA regardless of load making these regulators ideal for battery powered or energy conserving applications.

Both regulators feature output current sensing and remote shutdown.

A unique feature on the RS7663 only is a negative temperature coefficient output. This can be used, for example, to efficiently tailor the voltage applied to a multiplexed LCD through the driver so as to extend the display operating temperature range.

Features

- Ideal for battery-operated systems: less than 4μA typical current drain
- Will handle input voltages from 1.6V to 10V
- Very low input-output differential voltage
- 1.3V bandgap voltage reference
- Up to 25mA output current
- Output shutdown via current-limit sensing or external logic signal
- Output voltages programmable from 1.3V to 10V
- Output voltages with programmable negative temperature coefficients (RS 7663 only).

ATTENTION

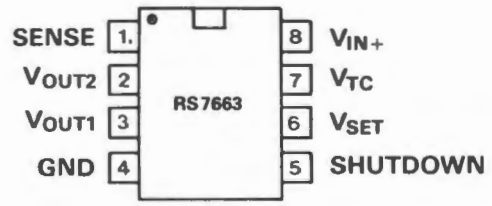
OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

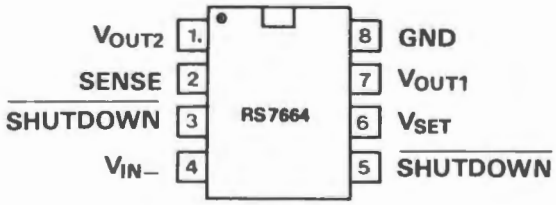
Absolute maximum ratings (RS7663)

Input supply voltage ..... +12V
Any input or output voltage ..... (GND –0.3V) to
(Terminals 1, 2, 3, 5, 6, 7) (Note 1) ..... (V_{IN}^+ +0.3V)
Output source current
(Terminal 2) 50mA
(Terminal 3) 25mA
Output sinking current (Terminal 7) ..... –10mA
Power dissipation (Note 2) 200mW
Operating temperature range ..... 0 to +70°C

Pin connections



TOP VIEW



TOP VIEW

Operating characteristics $V_{IN}^+ = 9V$, $V_{OUT} = 5V$, $T_A = +25°C$, unless otherwise specified.

Parameter	Symbol	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Voltage	V_{IN}^+	$T_A = +25°C$ $20°C \leq T_A \leq +70°C$	1.5 1.6		10.0 10.0	V
Quiescent Current	I_Q	$R_L = \infty$ $1.4V \leq V_{OUT} \leq 8.5V$ $V_{IN}^+ = 9V$		3.5	10	μA
Reference Voltage	V_{SET}		1.2	1.3	1.4	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	$8.5V < V_{IN}^+ < 9V$		±200		ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET} \Delta V_{IN}}$	$2V < V_{IN}^+ < 15V$		0.03		%/V

Parameter	Symbol	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{SET} Input Current	I_{SET}			±0.01	10	nA
Shutdown Input Current	I_{SHDN}			±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN} HI: Both V_{OUT} Disabled V_{SHDN} LO: Both V_{OUT} Enabled	1.4		0.3	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold Voltage	V_{CL}	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		0.7		V
Input-Output Saturation Resistance (Note 3)	SAT	$V_{IN}^{+} = 2V$ $V_{IN}^{+} = 9V$		200 70		Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	$\Delta I_{OUT1} = 100\mu A$ @ $V_{OUT1} = 5V$ $\Delta I_{OUT2} = 10mA$ @ $V_{OUT2} = 5V$		2.0 1.0		Ω
Available Output Current (V_{OUT2})	I_{OUT2}	$V_{IN}^{+} = 3V$ $V_{OUT} = V_{SET}$ $V_{IN}^{+} = 9V$ $V_{OUT} = 5V$	10 25			mA
Negative-Tempco Output (Note 4)	V_{TC}	Open-Circuit Voltage		0.9		V
	I_{TC}	Maximum Sink Current	0	8	2.0	mA
Temperature Coefficient	$\frac{\Delta V_{TC}}{\Delta T}$	Open Circuit		+2.5		mV/°C
Minimum Load Current	$I_{L(MIN)}$	(Includes V_{SET} Divider)			1.0	μA

Note 1. Connecting any terminal to voltages greater than V_{IN}^{+} + 0.3V) or less than (GND –0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to RS7663 power-up.

Note 2. Derate linearly above 50°C at 5mW/°C.

Note 3. This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

Note 4. This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}.

Absolute maximum ratings RS7664

Input supply voltage ——— −12V
Any input or output voltage (GND +0.3V) to
(Terminals 1, 2, 3, 5, 6, 7) (Note 1) ——— ($V_{\overline{IN}}$ −0.3V)
Output sink current (Terminals 1, 7) ——— −25mA
Power dissipation (Note 2) ——— 200mW
Operating temperature range ——— 0 to +70°C

Operating characteristics $V_{\overline{IN}} = -9V$, $V_{OUT} = -5V$, $T_A = +25°C$, unless otherwise specified.

Parameter	Symbol	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Voltage	$V_{\overline{IN}}$	$T_A = +25°C$ $0°C \leq T_A \leq +70°C$	−1.5 −1.6		−10.0 −10.0	V
Quiescent Current	I_Q	$\left.\begin{matrix}R_L = \infty \\ -1.4V \geq V_{OUT} \geq -8.5V\end{matrix}\right\}$ $V_{\overline{IN}} = 9V$		3.5	10	μA
Reference Voltage	V_{SET}		−1.2	−1.3	−1.4	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	$-8.5V < V_{\overline{IN}} < -9V$		±200		ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	$-2V < V_{\overline{IN}} < -15V$		0.03		%/V
V_{SET} Input Current	I_{SET}			±0.01	10	nA
Shutdown Input Current	$I_{\overline{SHDN}}$			±0.01	10	nA
Shutdown Input Voltage	$V_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ HI: Both V_{OUT} Disabled $V_{\overline{SHDN}}$ LO: Both V_{OUT} Enabled	−0.3		−1.4	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold Voltage	V_{CL}	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		−0.35		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	$V_{\overline{IN}} = 2V$ $V_{\overline{IN}} = 9V$		150 40		Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	$\Delta I_{OUT} = 100\mu A$ @ $\Delta I_{OUT} = -5V$		2.0		Ω
Output Current, V_{OUT1} or V_{OUT2}	I_{OUT}	$V_{\overline{IN}} = 3V$ $V_{OUT} = V_{SET}$ $V_{\overline{IN}} = 9V$ $V_{OUT} = -5V$		−2 −20		mA
Minimum Load Current (includes V_{SET} Divider)	$I_{L(min)}$				1.0	μA

Note 1. Connecting any terminal to voltages greater than (GND + 0.3V) or less than ($V_{\overline{IN}}$ −0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to RS7664 power-up.

Note 2. Derate linearly above 50°C at 5mW/°C.

Note 3. This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

Typical characteristics RS7663

Figure 1 **Output voltage as a function of output current**

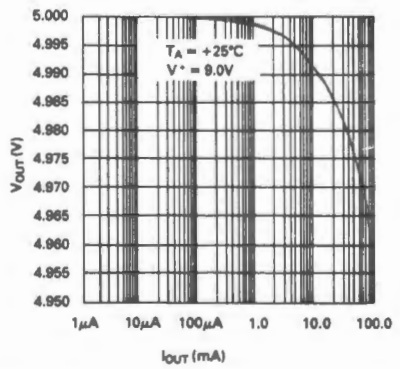


Figure 2 **V_{OUT1} Input-output differential as a function of output current**

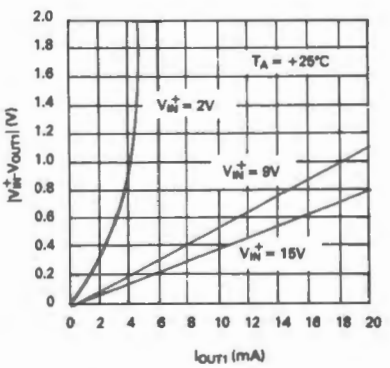


Figure 3 **V_{OUT2} Input-output differential as a function of output current**

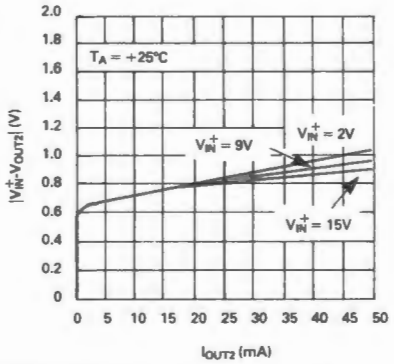


Figure 4 **Input power supply rejection ratio**

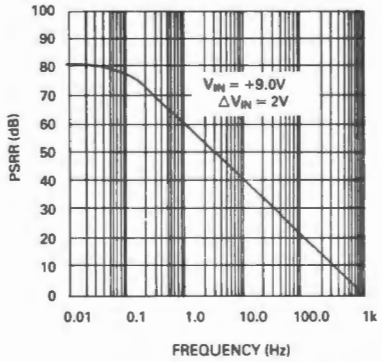


Figure 5 **Quiescent current as a function of input voltage**

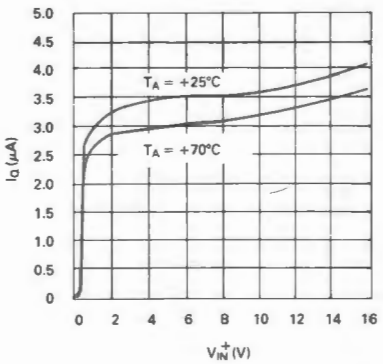
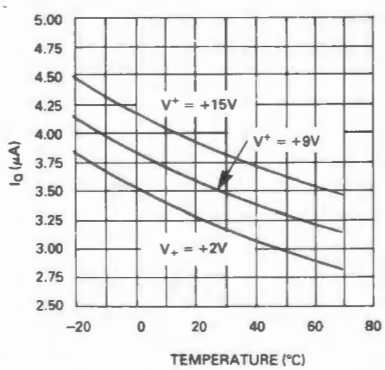


Figure 6 **Quiescent current as a function of temperature**



Typical characteristics RS7664

Figure 7 **Output voltage as a function of output current**

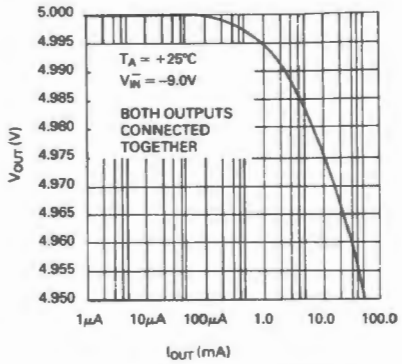


Figure 8 **V_{OUT1} Input-output differential as a function of output current**

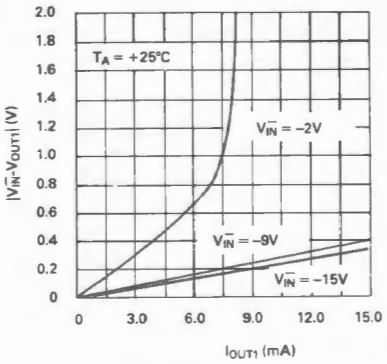


Figure 9 **V_{OUT2} Input-output differential as a function of output current**

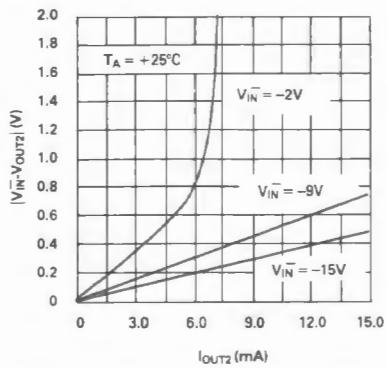


Figure 10 **Input power supply rejection ratio**

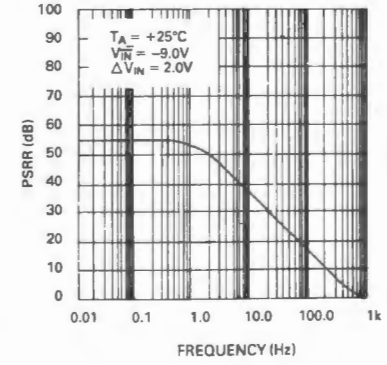


Figure 11 **Quiescent current as a function of input voltage**

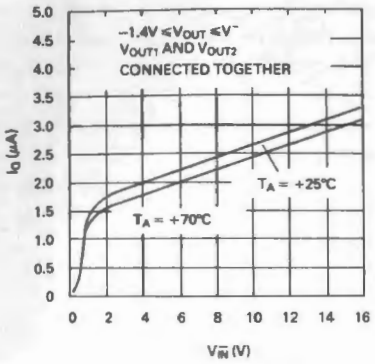
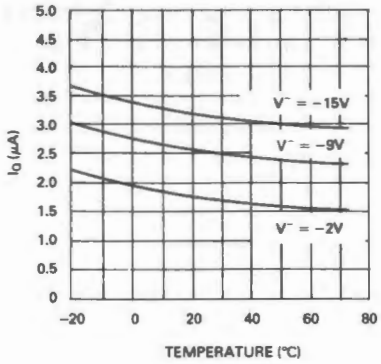


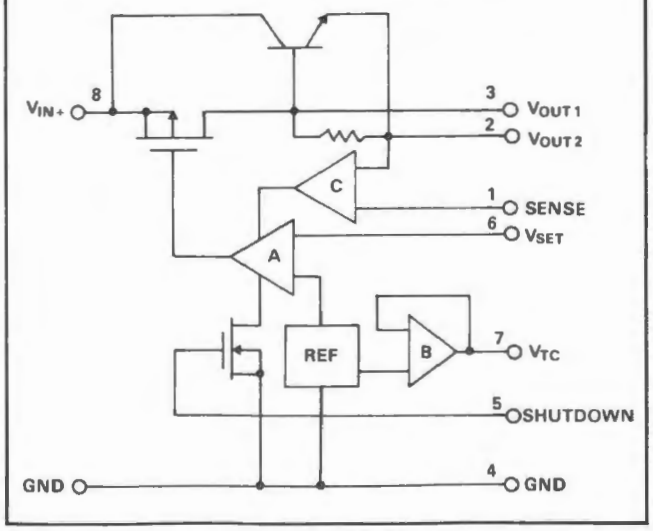
Figure 12 **Quiescent current as a function of temperature**



Detailed description

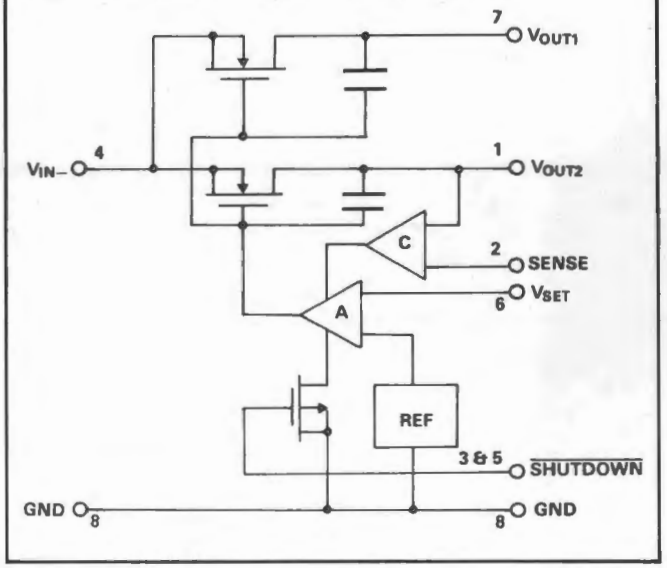
The RS7663 and RS7664 are CMOS integrated circuits which contain all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the block diagrams (Figures 13 and 14), each contains a bandgap-type voltage reference of 1.3 volts; this voltage, therefore is the lowest output voltage the regulators can control (–1.3V for the RS7664). Error amplifier A drives either a P-channel (RS7663) or an N-channel (RS7664) pass transistor which is sufficient for low (under about 5mA) currents; this transistor is augmented by a duplicate in the RS7664, which permits higher current outputs. In the RS7663, the high current output is formed by an NPN transistor connected as a follower. This configuration gives more gain and lower output imedance.

Figure 13 **Block diagram of the RS7663**



Logic-controlled shutdown is implemented via an MOS transistor of the appropriate polarity. Current-sensing is achieved with comparator C, which functions with the V_{OUT2} line on each chip. Finally, the positive regulator (RS7663 only) has an output (V_{TC}) from a buffer amplifier (B), which can be used to generate programmable-temperature-coefficient output voltages.

Figure 14 **Block diagram of the RS7664**



The amplifiers, reference and comparator circuitry all operate at bias levels well below 1μA to achieve the extremely low quiescent current. This does limit the dynamic response of the circuits, however, and transients are best dealt with outside the regulator loop.

Basic operation

The RS7663 and RS7664 are designed to regulate battery voltages in the 5V to 10V region at maximum load currents of about 5mA to 30mA. Although intended as low power devices, power dissipation limits must be observed. For example, the power dissipation in the case of a 15V supply regulated down to 5V with a load current of 30mA clearly exceeds the power dissipation rating of the package: (15-5) (30) (10^{-3}) = 300mW. Although the following discussion refers to the RS7663, it applies as well to the parallel features of the RS7664 as long as the appropriate polarities are reversed. Individual features and precautions will be discussed where appropriate.

CMOS devises generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or non-operation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

Input voltages

These regulators accept working inputs of about 1.4V to 10V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulators, where internal operation currents are in the nanoampere range. The 0.047μF capacitor on the device side of the switch will limit inputs to a safe level around 2V/μs. Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHUTDOWN pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulators by RC filtering, zener protection, or even fusing.

Output voltages

The resistor divider R_2/R_1 is used to scale the reference voltage, V_{SET}, to the desired output using the formula $V_{OUT} = (1 + R_2/R_1)\ V_{SET}$. In the RS7664, V_{IN}^- and V_{SET} are negative, so V_{OUT} will be also. Suitable arrangements of these resistors, using a potentiometer, enables exact values for V_{OUT} to be obtained. Because of the low leakage current of the V_{SET} terminal, these resistors can be tens of megohms for minimum additional quiescent drain current. However, *some* load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least 1μA. This can include the current for R_2 and R_1.

Output voltages up to nearly the V_{IN} supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the V_{OUT1} terminal.

Output currents

For the RS7663, low output currents of less than 5mA are obtained with the least input-output differential from the V_{OUT1} terminal (connect V_{OUT2} to V_{OUT1}). Either output may be used on the RS7664, with the unused output connected to V_{IN}^-. Where higher currents are needed, use V_{OUT2} on the RS7663 (V_{OUT1} should be left open in this case) and parallel V_{OUT1} and V_{OUT2} on the RS7664.

High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

Current-limit sensing

The on-chip comparator (C in the block diagrams) permits shutdown of the regulator output in the event of excessive current drain. As Figures 16, 17 and 18 show, a current-limiting resistor, R_{CL}, is placed in series with V_{OUT2}, and the SENSE terminal is connected to the load side of R_{CL}. When the current through R_{CL} is high enough to produce a voltage drop equal to V_{CL} (0.7V for RS7663, 0.35V for RS7664) the voltage feedback is bypassed and the regulator output will be limited to this current. Therefore, when the maximum load current (I_{LOAD}) is determined, simply divide V_{CL} by I_{LOAD} to obtain the value for R_{CL}.

Logic-controllable shutdown

When equipment is not needed continuously (eg., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it *is* required. This usually means switches, with their unreliable contacts. Instead, the RS7663 and RS7664 can be shut down by a logic signal, leaving only I_Q (under 4μA) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less than 0.3V for the RS7663, and greater than –0.3V for the RS7664 will keep the regulator ON, and a voltage level of more than 1.4V but less than V_{IN}^+ for the RS7663, and less than –1.4V but not less than V_{IN}^- for the RS7664 control will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input (V_{IN}^+ or V_{IN}^-), the current from this signal should be limited to 100μA maximum by a high-value (1MΩ) series resistor. This situation may occur when the logic signal originates from a separately-powered system from that of the regulator.

Additional circuit precautions

These regulators have poor rejection of voltage fluctuations from ac sources above 10Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20ms. From

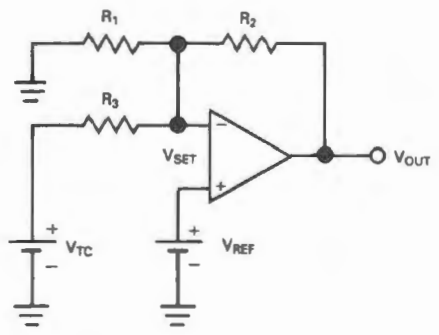
$$I = C\frac{\Delta V}{\Delta t},\ C = I_{OUT}\frac{(20 \times 10^{-3})}{0.9V_{OUT}} = 0.022\ \frac{I_{OUT}}{V_{OUT}}.$$

In addition, where such a capacitor is used, a current-limiting resistor is also suggested (see 'Current-limit sensing').

Producing output voltages with negative temperature coefficients

The RS7663 has an additional output (not present on the RS7664) which is 0.9V relative to GND and has a tempco of +2.5mV/°C. By applying this voltage to the inverting input of amplifier A (ie., the V_{SET} pin), output voltages having negative TC may be produced. The TC of the output voltage is controlled by the R_2/R_3 ratio (see Figure 15 and its design equations).

Figure 15 **Generating negative temperature coefficients**



EQ. 1: $V_{OUT} = V_{SET}\left(1 + \frac{R_2}{R_1}\right) + \frac{R_2}{R_3}(V_{SET} - V_{TC})$

EQ. 2: $TC\,V_{OUT} = -\frac{R_2}{R_3}(TC\,V_{TC})$ in mV/°C

Where: $V_{SET} = 1.3V$
$V_{TC} = 0.9V$
$TCV_{TC} = +2.5mV/°C$

Applications information

Figure 16 **RS7663 positive regulator with current limit**

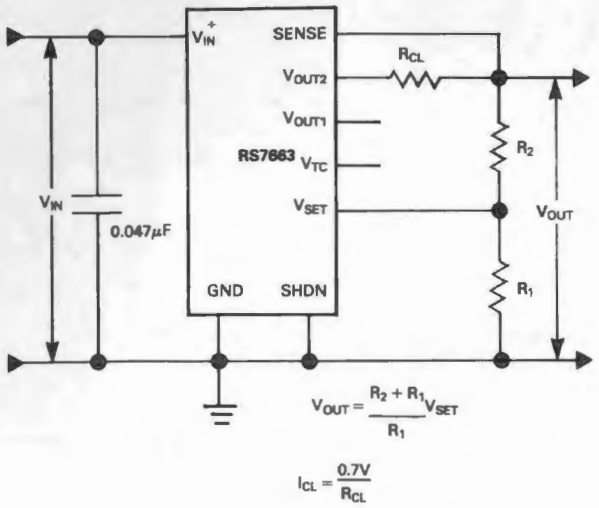


Figure 17 **RS7664 negative regulator with current limit**

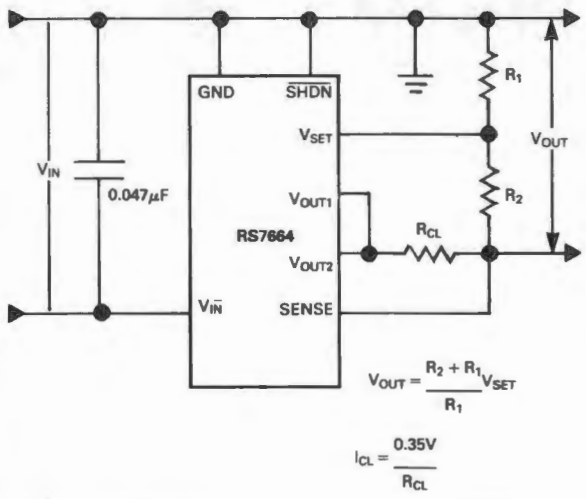
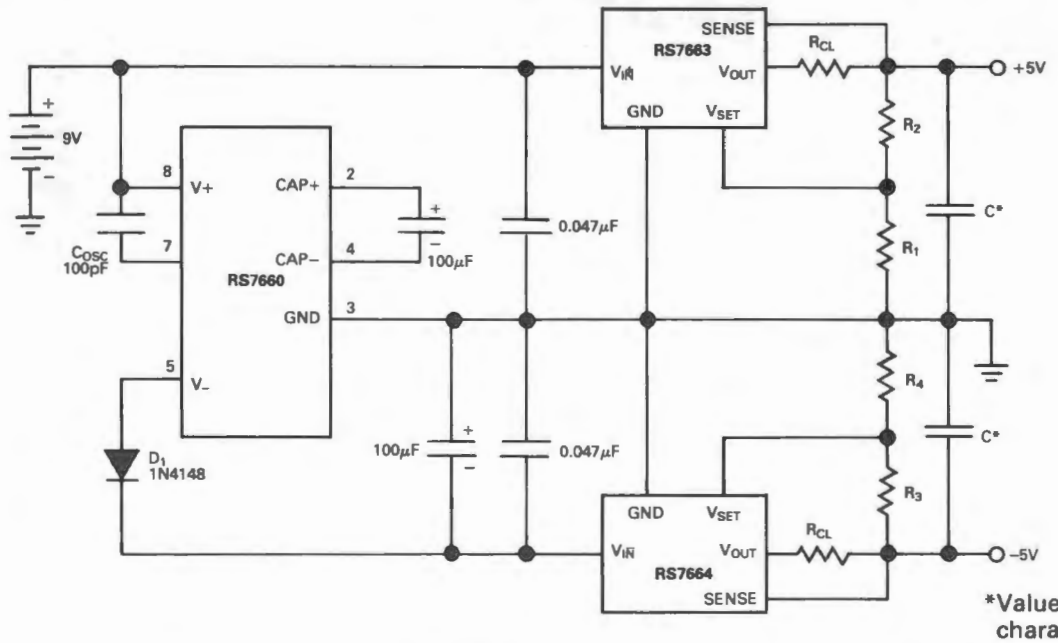


Figure 18 **Generating regulated split supplies from a single supply**



*Values depend on load characteristics

The oscillation frequency of the RS7660 is reduced by the external capacitor, so that it inverts the battery voltage more efficiently.

RS data

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An Electrocomponents Group Company

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RS data

Low dropout fixed 5V regulators RS2931

Stock numbers 630-702 (TO-92) and 630-730 (TO-220)

Two 5V positive voltage regulators with maximum output currents of 400mA (TO-220) and 150mA (TO-92).

Featuring very low quiescent currents and extremely low drop-out voltage these regulators are ideally suited for standby power systems. Designed primarily for automotive applications the regulators and all regulated circuitry are protected from reverse battery installations or two battery jumps. During line transients such as load dump (60V) the regulator will automatically shut down to protect both internal circuits and the load. Familiar regulator features such as short circuit protection and thermal overload protection are also provided.

Applications include memory standby circuits, CMOS and other low power processor power supplies as well as systems demanding as much as 400mA of output current.

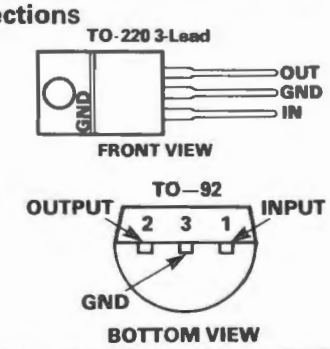
Features

- Very low quiescent current
- Output current in excess of 150mA (TO-92), 400mA (TO-220)
- Input-output differential less than 0.6V
- Reverse battery protection
- 60V load dump protection
- Reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Mirror-image insertion protection
- Available in plastic TO-220 or TO-92.

Absolute maximum ratings

Forward input voltage	26V
Over-voltage protection (t = 100ms)	±60V
Operating temperature range	–40°C to +85°C
Maximum junction temperature	+125°C
Storage temperature range	–65°C to +150°C

Pin connections



Electrical characteristics (V_{IN} = 14.4V, I_o = 10mA, T_j = 25°C unless otherwise specified).

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	6V ≤ V_{IN} ≤ 26V, I_o ≤ 150mA –40°C ≤ T_j ≤ + 125°C	4.75	5	5.25	V
ΔV_o	Line regulation	9V ≤ V_{IN} ≤ 16V		2	10	mV
		6V ≤ V_{IN} ≤ 26V		4	30	mV
ΔV_o	Load regulation	5mA ≤ I_o ≤ 150mA		14	50	mV
R_o	Output impedance	100mA$_{DC}$ & 10mA(rms), 100Hz – 10kHz		200		mΩ
I_d	Quiescent current (TO-220)	I_o = 10mA 6V ≤ V_{IN} ≤ 26V –40°C ≤ T_j ≤ +125°C I_o = 150mA, V_{IN} = 14V, Tj = 25°C		0.8 20	2 40	mA mA
I_d	Quiescent current (TO-92)	I_o ≤ 10mA 6V ≤ V_{IN} ≤ 26V, T_j = 25°C I_o = 150mA, V_{IN} = 14V, T_j = 25°C		0.4 15	1	mA mA
e_N	Output noise voltage	10Hz – 100kHz		500		μVrms
	Long term stability			20		mV/ 1000hr
SVR	Supply voltage rejection	f_o = 120Hz		80		dB

Electrical characteristics (V_{IN} = 14.4V, I_o = 10mA, T_j = 25°C unless otherwise specified).

	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}–V_o	Dropout voltage (TO-220)	I_o = 10mA I_o = 150mA I_o = 400mA		0.05 0.2 0.4	0.1 0.4	V V V
V_{IN}-V_o	Dropout voltage (TO-92)	I_o = 10mA I_o = 150mA		0.05 0.3	0.2 0.6	V V
I_o	Current limit			650		mA
R_{th} j-case	Thermal resistance junction-case (TO-220)				4	°C/W
R_{th} j-case	Thermal resistance junction-case (TO-92)				55	°C/W

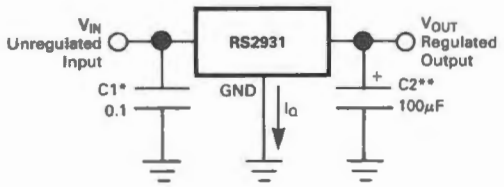
Application hints

One of the distinguishing factors of the RS2931 series regulators is the necessity of the output capacitor required for device stability. The value required varies greatly depending upon the application circuit and other factors. Thus some comments on the characteristics of both capacitors and the regulator are in order.

High frequency characteristics of electrolytic capacitors depend greatly on the type and even the manufacturer. As a result, a value of capacitance that works well with the RS2931 for one brand or type may not necessarily be sufficient with an electrolytic of different origin. Sometimes actual bench testing, as decribed later, will be the only means to determine the proper capacitor type and value. Experience has shown that, as a rule of thumb, the more expensive and higher quality electrolytics generally require a smaller value for regulator stability. As an example, while a quality 100μF aluminium electrolytic covers covers all general application circuits, similar stability can be obtained with a tantalum electrolytic of only 47μF. This factor of two can generally be applied to any special application circuits also.

Another critical characteristic of electrolytics is their performance over temperature. While the RS2931 is designed to operate to –40°C, the same is not always true with all electrolytics (heat is generally not a problem). The electrolyte in many aluminium types will freeze around –30°C, reducing its effective value to zero. Since the capacitance is needed for regulator stability, the natural result is oscillation (and lots of it) at the regulator output. For all application circuits where cold operation is necessary, the output capacitor must be rated to operate at the minimum temperature. By coincidence, worst-case stability for the RS2931 also occurs at minimum temperatures. As a result, in applications where the regulator junction temperature will never be less than 25°C, the output capacitor can be reduced approximately by a factor of two over the value needed for the entire temperature range. To continue our example with the tantalum electrolytic, a value of only 22μF would probably thus suffice. For quality aluminium, 47μF would be adequate in such an application.

Figure 1 **The regulator with associated capacitors**



*Required if regulator is located far from power supply filter.

**C2 must be at least 100μF to maintain stability. May be increased without bound. Locate as close as possible to regulator.

Another regulator characteristic that is noteworthy is that stability decreases with higher output currents. This sensible fact has important connotations. In many applications, the RS2931 is operated at only a few milliamps of output current or less. In such a circuit, the output capacitor can be further reduced in value. As a rough estimation, a circuit that is required to deliver a maximum of 10mA of output current from the regulator would need an output capacitor of only half the value compared to the same regulator required to deliver the full output current of 150mA. If the example of the tantalum capacitor in the circuit rated at 25°C junction temperature and above were continued to include a maximum of 10mA of output current, then the 22μF output capacitor could be reduced to only 10μF.

At this point, the procedure for bench testing the minimum value of an output capacitor in a special application circuit should be clear. Since worst-case occurs at minimum operating temperatures and maximum operating currents, the entire circuit, including the electrolytic, should be cooled to the minimum temperature. The input voltage to the regulator should be maintained at 0.6V above the output to keep internal power dissipation and die heating to a minimum. Worst-case occurs just after input power is applied and before the die has had a chance to heat up. Once the minimum value of capacitance has been found for the brand and type of electrolytic in question, the value should be doubled for actual use to account for production variations both in the capacitor and the regulator. (All the values in this data sheet were determined in this fashion.)

Definition of terms

Dropout voltage. The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input voltage. The dc voltage applied to the input terminals with respect to ground.

Input-output differential. The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line regulation. The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load regulation. The change in output voltage for a change in load current at constant chip temperature.

Long term stability. Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output noise voltage. The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent current. That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple rejection. The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature stability of V_o. The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

RS data

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An Electrocomponents Group Company

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RS data

92 Key data entry keyboard

Stock number 332-329

The RS low profile 92 key data entry keyboard is the user interface to a host computer terminal. The keyboard detects key depressions, encodes them and transmits the information to the host. Communication between the keyboard and terminal can be 8-bit parallel data plus strobe or asynchronous serial data at a user selectable baud rate of 300, 600, 1200 or 2400 with either standard TTL or RS232C interface. The supply voltage may be set to +5 or +12 volts for the TTL interface or ± 12 volts for the RS232C.

Features

- Low profile design – meets DIN66234 part 6
- High reliability with mechanical and electrical life of 100×10^6 switch operations
- 92 contactless capacitance switches
- Double-shot moulded, sculptured keytop set
- 2m coiled cable (extended length) fitted with a 9 pin D-type plug
- Three output configurations:
  a) TTL serial
  b) RS232C serial
  c) 8-bit parallel
- 5V or 12V operation
  (±12V required for RS232C)
- Optional baud rates for serial output
- ASCII compatible keycodes
- Pre-programmed function keys
- All keycodes may be pre-programmed to suit user requirements.

Connections

The RS keyboard as supplied is configured for +5V supply TTL serial output at 1200 baud. Connection between keyboard and terminal is by means of a multicore coiled cable. A 9-pin 'D' type connector is fitted and connections are detailed in Table 1.

Table 1 **Keyboard cable pin connections**

Pin no.	Function
2	Serial data output
7	Supply ground (0V) + cable screen
8	Supply (+5V or +12V)

User options

The RS 92 key data entry keyboard is designed to offer various user options in terms of interface, keycodes and power supply. These are:

Data output Serial TTL or RS232C. Data rate is selectable at 300, 600, 1200 or 2400 baud.

Word format: 1 start bit, 8 data bits, two stops bits, no parity.

Parallel 8 bit data with strobe, TTL levels. Positive strobe, 70 microsecond width. See timing diagram, Figure 3.

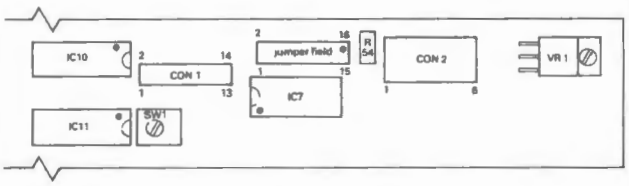
Keycodes Function keys can be re-configured by changing the hexadecimal code stored in a defined location in Eprom.

Power supply Serial or parallel TTL outputs, may be operated from +5, or +9 to +12V dc.

RS 232C requires +12 and –12V.

As supplied, the RS keyboard is configured for operation at +5V (+0.35/–0.15V) dc serial TTL output at 1200 baud. These options are detailed below.

Figure 1 **Connector and link locations**



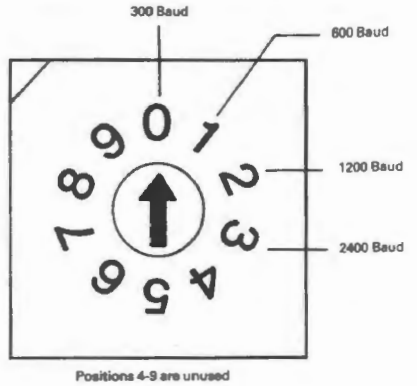
CON 1 is the parallel interface connector.
CON 2 is the serial interface connector.
The links are located in the jumper field.

Data output

Baud rate

Locate the baud rate rotary switch (SW1) mounted on the top side of the printed circuit board, by means of a small screwdriver, set this to the required baud rate. See Figure 2 (these settings are relevant to both TTL and RS 232C configurations).

Figure 2 **Baud rate switch (SW1)**



Positions 4-9 are unused

RS 232C Configuration

Table 2 **Cable connections**

Keyboard connector		RS 232 connector	
Pin	**Function**	**Pin**	**Function**
1	OV	7	OV
2	OV (screen)	1	Protective ground
3	+12V	11	+12V
4	–12V	23	–12V
5	Data	2	Tx
6	N/C		

Disconnect the coiled cable from the keyboard connector. Remove ic 7 (see Figure 1) and replace with an RS 232C driver ic (RS stock no. 309-587).

Ensure correct ic orientation (see Figure 1).

Locate the jumper field situated adjacent to ic 7. If fitted, remove links connecting pins 14 to 16, 13 to 15 and 9 to 11. Using a wire wrapping tool and suitable insulated wire, link pins 15 to 16 and 7 to 9 (suitable wire wrapping tool RS stock no. 554–005). See Table 5 for Link Summary.

The replacement cable assembly should be configured so that the keyboard connections are as detailed in Table 2 (for standard RS 232C).

Note: both +12 and –12V are required by the keyboard for RS 232C.

Parallel data configuration

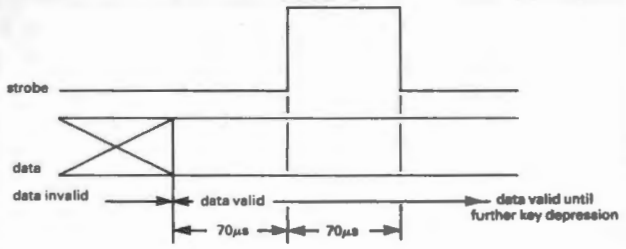
Disconnect the coiled cable from the keyboard connector, CON2. Fit a 74LS374 (RS Stock No. 309-262) into socket position ic 11, ensuring that the device is correctly orientated (see Figure 1). (ic 7 is not required for parallel output and so may be removed to decrease power consumption.)

The replacement cable assembly should consist of a 14 pin insulation displacement socket, (RS No. 471-036) complete with the required length of ribbon cable and terminal mating connector. This should be fitted to CON 1 on the keyboard (see Figure 1). Connections are detailed in Table 3.

Table 3 **Pin connections on parallel connector, CON 1 (see Figure 1)**

Pin	Functions
1	Data bit 0
2	Data bit 1
3	Data bit 2
4	Data bit 3
5	Data bit 4
6	Data bit 5
7	Data bit 6
8	Data bit 7
9	Strobe
10	Supply (see power supply section)
11	OV
12	OV
13	No connection
14	No connection

Figure 3 **Parallel word format timing diagram**



User definable keys

The RS keyboard is supplied with a complete row of keys marked F1 to F20 which may be user programmed for special functions.

This is achieved by the use of an Erasable Programmable Read Only Memory (EPROM) to store the keycodes for the keyboard. It should be noted that the entire operating system for the keyboard is also stored in this device, so it is imperative that before any modifications are made, **the entire contents should be copied into a backup store, such as another EPROM, as a safeguard.**

An EPROM programmer such as RS Stock no. 301-785 and an additional 2516 single rail EPROM (Stock no. 301-987) is necessary.

Table 4 gives the low and high bytes of the location of the user definable keycodes for normal, shifted and controlled modes of individual key depressions.

Table 4 **EPROM locations for user defineable keys**

EPROM location	High Byte	$04	$05	$06	$07
Low Byte	Legend	KEYCODES			
		Normal mode	Ctrl mode	Shift mode	Shift & ctrl mode
$89	F1				
$8A	F2				
$7A	F3				
$82	F4				
$72	F5				
$6A	F6				
$69	F7				
$62	F8				
$5A	F9				
$52	F10				
$21	F11				
$2A	F12				
$29	F13				
$11	F14				
$19	F15				
$1A	F16				
$42	F17				
$4A	F18				
$32	F19				
$39	F20				

Note: $ prefix indicates value in hexadecimal

For example, if it is required to generate the keycode $ 3A for the simultaneous depression of 'CTRL' and F5, then the address at which this code must be located is $0572. Similarly, if the simultaneous depressions of 'SHIFT' and F10 is required to generate $8F, then this code must be located at $0652. For normal mode code outputs eg. 'F6' by itself, the keycode would be inserted at $046A.

Figures 4 and 5 show the EPROM locations and standard codes respectively for the complete keyboard. These are not normally use definable, since the legends are specific but may be refined if required as detailed on the previous page.

Figure 4 **EPROM locations (addresses) for keycodes. All values are in hexadecimal. The contents of these addresses are indicated in Figure 5.**

89	8A	7A	82	72	6A	69	62	5A	52	21	2A	29	11	19	1A	42	4A	32	39
88	79	78	81	70	71	68	61	59	51	20	23	28	10	18		40	48	30	38
8B	7B	83	80	73	6B	63	5C	5B	53	24	2B	13	1B			43	4C	34	3C
8C	7C	86	74	76	6E	64	5E	56	54	26	2C	14	1C			46	4E	36	3F
8E	87	75	6F	6D	67	66	5F	57	27	2F	17	1F				47	4F	37	
8D	7D	85				65					2D	15	1D			45	4D	35	3D

04	Normal
05	Control
06	Shift
07	Shift +Control

The above diagram shows low-byte addresses of the individual keys. The high-byte depends on the mode of key use – normal, control, shift or shift and control. eg. the F1 keycode (top left key) is located at 0489 (hex) when pressed on its own (normal). When pressed in conjunction with the shift key ie. 'Shift F1' the keycode transmitted is located at 0689 (hex).

Figure 5 **Standard keycodes transmitted when the relevant key is pressed. All values are in hexadecimal. For address of these keycodes in the keyboard EPROM see Figure 4.**

80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93
80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93
80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93

1B	31	32	33	34	35	36	37	38	39	1F	2D	1E	7F	08		37	38	39	2B
1B	21	22	23	24	25	26	27	28	29	5F	3D	7E	7F	08		37	38	39	2B
1B	31	32	33	34	35	36	37	38	39	30	2D	5E	7F	08		37	38	39	2B
09	11	17	05	12	14	19	15	09	0F	10	00	1B		0D		34	35	36	2D
09	51	57	45	52	54	59	55	49	4F	50	60	7B		0D		34	0B	36	2D
09	71	77	65	72	74	79	75	69	6F	70	40	5B		0D		34	35	36	2D
	01	13	04	06	07	08	0A	0B	0C	3B	3A	1D		CAPS		31	32	33	
CTRL	41	53	44	46	47	48	4A	4B	4C	2B	2A	7D		LOCK		08	0C	09	0D
	61	73	64	66	67	68	6A	6B	6C	3B	3A	5D				31	32	33	0D
	1A	18	03	16	02	0E	0D	2C	2E	2F	1C					2C	30	2E	0D
SHIFT	5A	58	43	56	42	4E	4D	3C	3E	3F	7C		SHIFT			2C	0A	2E	0D
	7A	78	63	76	62	6E	6D	2C	2E	2F	5C					2C	30	2E	
						20													
						20													
						20													

CTRL
SHIFT
NORMAL

(Shift+Ctrl codes are supplied the same as Ctrl codes)

Miscellaneous functions

Other functions of the keyboard may be modified as indicated in Table 5. The hexadecimal codes shown should replace the existing code at the EPROM location associated with the function.

Table 5 **Optional parameters for miscellaneous keyboard functions**

Function	Eprom location (hex)	Parameter	Codes (hex)
Strobe width	01F1	70) 100) 200) µs 400) 600) 800)	0A (std) 10 24 4C 74 9C
Repeat delay	00C2	500ms 750ms 1s 1.25s	04 (std) 06 08 0A
Repeat rate	00DD	8) 10) 12) chr/sec 16)	0A 08 (std) 06 05
Parity	0225	No parity Odd parity Even parity	40 (std) 55 62

Power supply

The RS keyboard may be configured to operate from +5V or from +12V dc at 250mA (see note below), depending on the application. It is suggested that if the keyboard is to be used with cables other than supplied, (particularly those of lesser conductor diameter and/or greater length eg. ribbon cable) then the keyboard should be configured for 12V operation.

For RS232C the keyboard also requires – 12V at 50mA (no load).

The keyboard is supplied for +5V operation (pin 9 linked to pin 11). If it is required to convert to between +9V and 12V operation consult Table 6. (Remove link from pins 9 to 11 and link pins 7 and 9 together, for +12V operation.)

Note: the use of a 12V supply when the keyboard is configured for 5V operation (as supplied), or supply reversal, will result in damage to the keyboard electronics.

Table 6 **Link summary**
Links are located in the jumper field – see Figure 1.

Option	Link	Break
5V	9 to 11	7 to 9
12V	7 to 9	9 to 11
TTL	14 to 16 13 to 15	 16 to 15
RS 232C	16 to 15	14 to 16 13 to 15

RS data

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RS data

Peltier mini module

Stock number 300-518

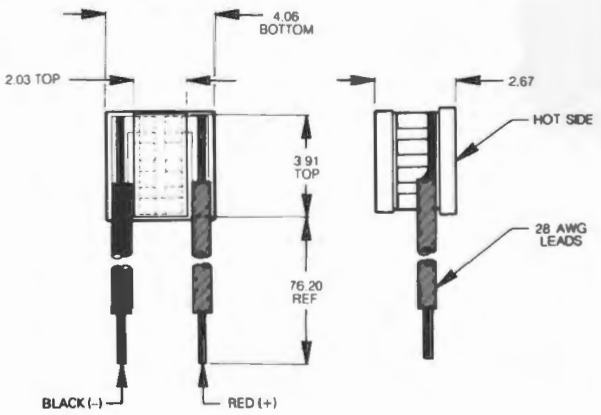
The RS300-518 is a semiconductor thermoelectric device working on the Peltier effect. When supplied with a suitable electric current it can either cool or heat. When subjected to an externally applied temperature gradient the device will generate a small amount of electric power.

Many electronic devices exhibit temperature dependent parameters. Typically, dc amplifiers, voltage references crystals, oscillators etc will all drift with temperature change. The small size of the Peltier Mini Module makes it ideally suited for use with such miniature electronic components. The module can be used to maintain a constant component temperature thereby minimising these effects. Alternatively by varying the Peltier device current, and hence device temperature, it can be used to investigate temperature effects on these components.

Reducing component temperature can provide increased reliability and reduced thermal noise. The Peltier Mini Module can be used to cool miniature electronic components including low level pre-amp transistors, infra red detector chips, microwave integrated circuits, fibre optic lasers and detectors.

Features

- Low input current
- Miniature size, small enough to fit within most JEDEC packages
- Wide operating temperature range from −100°C to +150°C
- Lightweight – less than 0.7 grams
- Solid state, long term reliability
- Capable of heating and cooling
- Accurate temperature control ±1°C typical.



Dimensions in millimetres

Electrical characteristics at hot side temperature (TL) +50°C

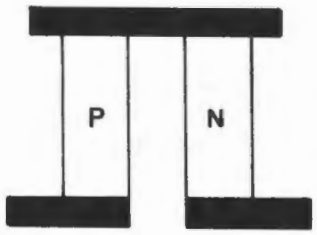
Parameter	Valve
Maximum temperature difference (ΔT)	60°C or greater
Maximum current	1.1A
Nominal voltage	0.48V at max. current
Heat pumping capacity (Q_c)	0.29W or greater
Maximum operating temperature	+150°C

Introduction to The Peltier Effect

In 1834 Jean C. A. Peltier discovered that the passage of an electric current through the junction of two dissimilar conductors can either cool or heat this junction depending on the direction of current. Heat generation or absorption rates are proportional to the magnitude of the current and also the temperature of the junction.

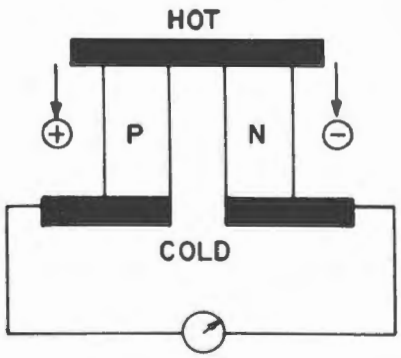
Practical Peltier Effect Heat Pumps consist of many such couples connected electrically in series and thermally in parallel.

Figure 1 **A single couple**



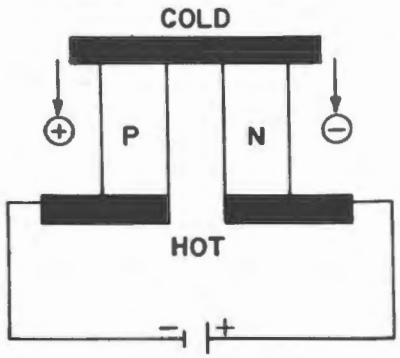
Semiconductors doped both p and n type form the elements of the couple and are soldered to copper connecting strips. Ceramic faceplates electrically insulate these connecting strips from external surfaces. The semiconductor material used is bismuth telluride as this shows the most pronounced effect at moderate operating temperatures.

Figure 2 **Generation of voltage**



At open circuit a temperature gradient maintained across the device creates a potential across its terminals proportional to the temperature difference. If the temperature difference is maintained, and if the device is connected to an electrical load power is generated.

Figure 3 **Use as a heat pump**



If, instead the device is connected to a dc source, heat will be absorbed at one end of the device, cooling it, while heat is rejected at the other end, where the temperature rises. Reversing the current reverses the flow of heat. Therefore the module can generate electric power or, depending on how it is connected to external circuitry, heat or cool an object.

A common misconception is that the Peltier device somehow absorbs heat and carries it away, perhaps with the electric current. This is simply not true. The device only transfers or pumps heat from one of its sides to the opposite side. At the hot side, the heat must be removed through the use of a heat sink or by some other means. It is important to realise that the heat delivered to the hot side of the device includes the pumped heat plus the electrical power dissipated within the device.

Using the Peltier Device

The Peltier mini module is a small semiconductor heat pump containing four couples. Its small size makes it ideal for use where miniature electronic components require cooling or temperature control. Singly it is small enough to fit in most JEDEC packages or can be attached to the outer surface of dual in line packages, crystal cans, transistor packages etc. Where a greater degree of heat pumping is required multiple devices can be used.

When trying to determine the heat pumping capacity required, two factors must be considered; Active Heating Elements and Heat Leak.

Active Heating Elements are any components which have a power consumption. All of this power consumption (input power) will eventually be converted to heat and should be considered as heat load.

An object that is held at a temperature below ambient will draw heat from the surroundings onto its cold surface. The results of this additional heat is that a cooled object which is not insulated will not be able to maintain temperatures as low as one which has insulation. This additional heat load requirement is called the heat leak. Three main factors affect the magnitude of the heat leak. These are:

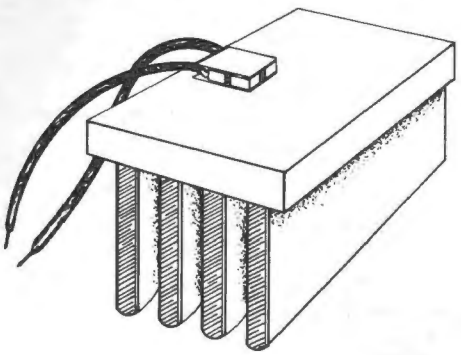
1. The temperature difference between ambient and the cooled device.
2. The surface area of the cooled device.
3. The amount of insulation used. It is advantageous to thermally insulate the device being cooled in order to reduce the heat leak to a minimum.

There are other sources of heat leak such as conduction heat from electrical wires or heat leak from the heat sink back to the cold plate of the Peltier Device. Hence precise calculation of heat leak is difficult and it may be best determined empirically.

The total heat pumping capacity required is the sum of the active heat load and the heat leak.

Choosing the proper heat sink

Figure 4 **Hot side mounted to a heat sink**



Once the required heat pumping capacity has been determined the next step is choosing the proper heat sink. A Peltier Device is not a sponge which absorbs heat, rather, it is a heat pump. The heat which is pumped out of the cold surface is deposited on the hot side of the module. This heat must be dissipated in some way. If it is not the hot side of the device will heat up the point where it will stop functioning as a cooling device and actually begin to heat the cold surface.

From fundamentals, a heat sink must be maintained at a temperature higher than ambient to transfer heat from its surface out into the surroundings. The higher the heat sink temperature above the ambient temperature the more heat can be transferred out of the heat sink. This points to choosing a heat sink which will get as hot as possible. However, reference to the performance curves of Figure 5 shows that as the △T across the module becomes larger (as a result of the increased hot side temperature) the heat pumping capacity and the coefficient of performance (COP) both decrease. Considering both these phenomena a heat sink which rises to a temperature between 5 and 15°C above ambient is a practical choice. This is not a difficult criteria to meet with a single mini module since the typical power appearing at the hot side will be no greater than 0.83W which would require a heat sink of 6°C/W to sustain a 5°C rise in temperature.

Figure 5 **Pumped heat vs current**

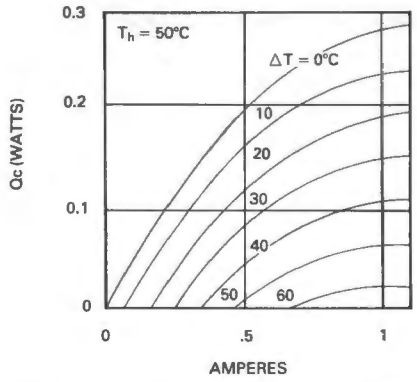


Figure 6 **Coefficient of performance vs current**

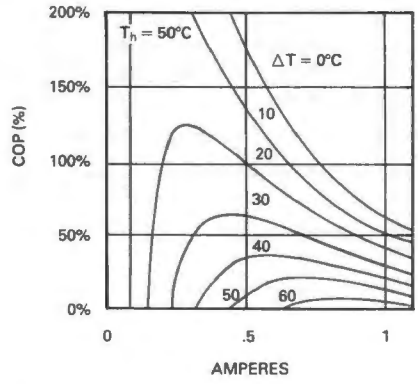


Figure 7 **Input voltage vs current**

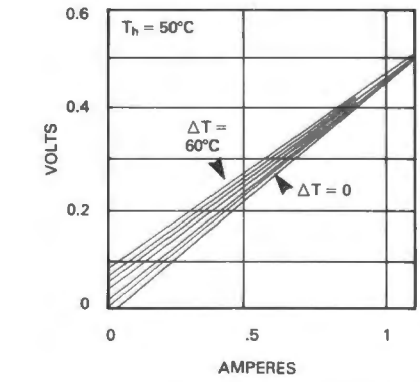


Figure 8 **Voltage vs operating current**

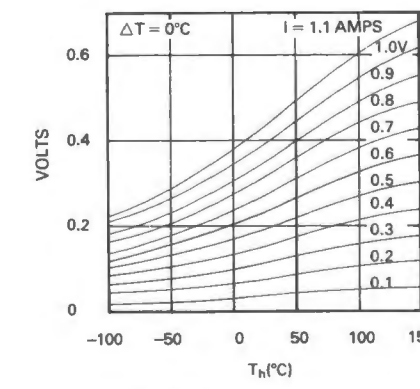
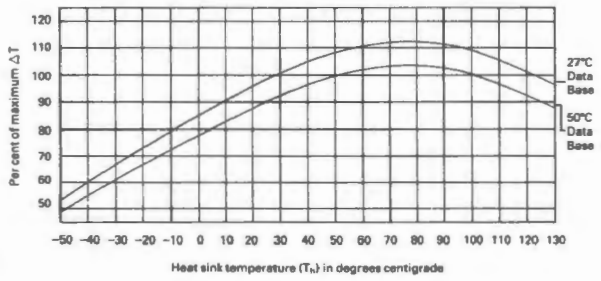
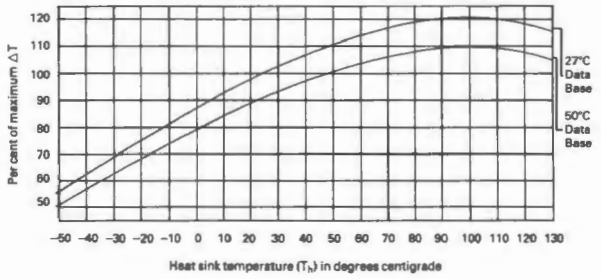


Figure 9 **Percentage of maximum ΔT for various heat sink temperatures**



The maximum ΔT of thermoelectric devices is dependent upon the temperature of the heat sink. Performance at heat sink temperatures other than the specified reference temperature of 50°C may be determined from this graph.

Figure 10 **Percentage of rated heat pumping capacity for various heat sink temperatures**



The rated heat pumping capacities of thermoelectic devices is dependent upon the temperature of the heat sink. Performance at heat sink temperatures other than the specified reference temperature of 50°C may be determined from this graph.

How to use the Performance graphs

Example:

An IC consumes 130mW of power. It is desired to maintain this object at 10°C the ambient temperature is 25°C. Heat leak from the surroundings is 20mW.

1. Hence Total Heat Load is

Heat generated	130mW
Heat leak	20mW
Total heat load: Q_c =	150mW

2. Heat sink temperature selection

The hot side of the Peltier Device is mounted on the base of the heat sink for heat rejection. The selection of the heat sink base temperature (or hot side temperature) will determine the size and type of heat sink, and the number of Peltier Devices required to handle the heat load.

When a lower heat sink temperature is selected a lesser number of Peltier Devices is required to handle the heat load.

In this case the heat sink base temperature is assumed to be 5°C above ambient ie. T_h = 30°C

3. Design Condition

T_h = 30°C
T_c = 10°C
Q_c = 150mW

We need to find the following:

Input current	Heat rejection
Input voltage	No. of modules
Input power	Heat sink requirements

a. Maximum Q_c Design

From Figure 5 When Q_c = 150mW
I = 0.6A (ΔT = 20°C)

From Figure 6 When I = 0.6A
COP = 80% (ΔT = 20°C)

Hence power input at I = 0.6A is:

$$P = \frac{Q_c}{COP} = \frac{150mW}{80\%} = 187mW$$

Input voltage is found as:

$$V = \frac{P}{I} = \frac{187mW}{0.6A} = 0.31V$$

Heat rejected from one module:

$Q_h = Q_c + P = 187mW + 150mW = 337mW$

Required thermal resistance of heat sink is:

$$O = \frac{(T_h - T_a)}{Q_h} = \frac{5°C}{.337} = 14.8°C/W$$

b. Maximum coefficient of performance (COP) design

From Figure 6

COP = 125% at 0.26A (for ΔT = 20°C)
Q_c = 50mW at 0.26A (for ΔT = 20°C)

Number of modules required is:

$$N = \frac{Q}{Q_c} = \frac{150}{50} = 3$$

Total power input to modules:

$$P = \frac{Q_c}{COP} \times N = \frac{50mW \times 3}{125\%} = 120mW$$

When three modules are connected in series:

$$V = \frac{P}{I} = \frac{120mW}{0.26A} = 0.46V$$

Heat rejection from three modules:

$Q_h = Q_c + P = 120mW + 150mW = 270mW$

Required Thermal resistance of heat sink is:

$$O = \frac{T_h - T_a}{Q_h} = \frac{5°C}{270mW} = 18.5°C/W$$

In this example the use of three modules with a resultant improvement of efficiency saves 190mW of power. In practice the cost of extra Peltier Devices must be weighed up against the additional power consumed by running fewer devices at a lower efficiency.

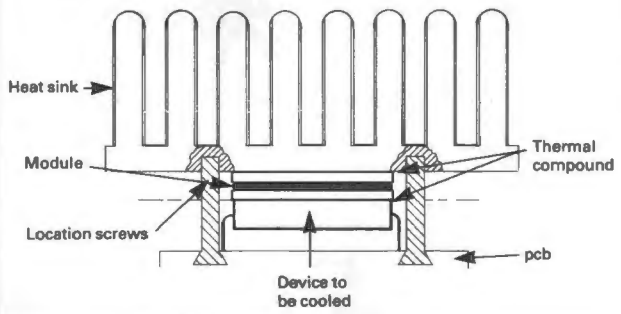
Installation of Peltier Devices

Peltier Devices are only as strong as the semiconductor materials used in their fabrication and thus may be damaged by the application of excessive stress. Modules should never be designed as a mechanical supporting member of an assembly.

Two mounting methods are recommended with the clamping method being generally preferred. Epoxy bonding should not be used when operation in a vacuum is required.

Clamping method

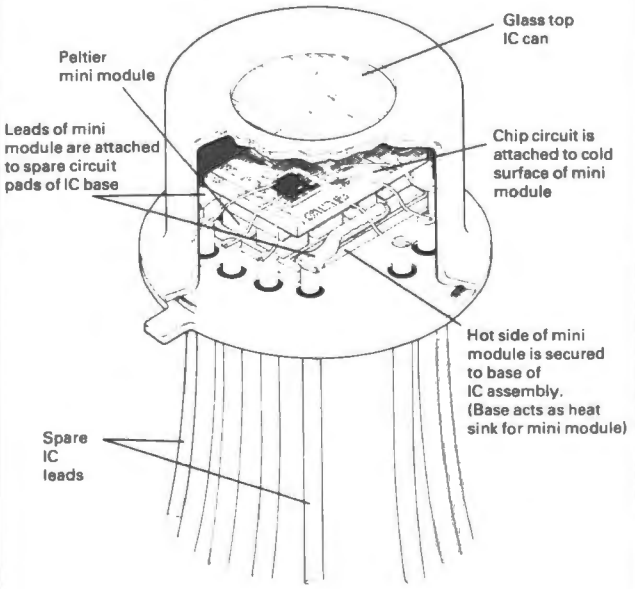
Figure 11 **Fixing by clamping**



1. The mounting surfaces should be smooth to within ±0.001 in.
2. Clean the module and mounting surfaces to remove any burrs, grit, etc.
3. Coat the module hot side with a thin film of heatsink compound and place the module on the heat sink. Applying firm but even downward pressure, rock the module from side to side until a slight resistance is felt and excess heatsink compound is squeezed out.
4. Coat the cold side of the module with a thin film of heatsink compound. Place the object to be cooled in contact with the module and rock the object slightly from side to side to squeeze out excess thermal grease.
5. Bolt the object to be cooled and heat sink together using either stainless steel screws with spring washers or nylon screws. To ensure even pressure across the module surfaces, tighten all screws finger tight and then continue tightening in an alternate or diagonal pattern starting with the centre screws (if any) first. Maximum recommended compression loading is 15 pounds per square inch of module surface. DO NOT OVER TIGHTEN.

Epoxy bonding method

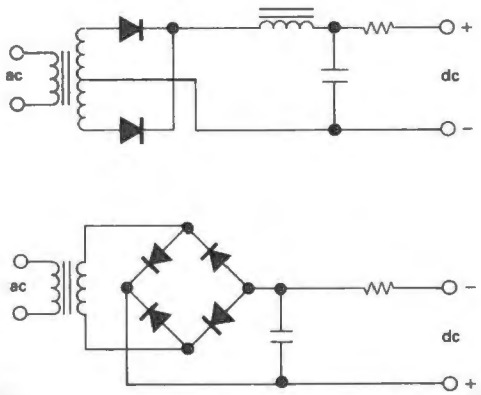
Figure 12 **Fixing by bonding**



1. The mounting surfaces should be smooth, flat and free from grease or burrs.
2. Coat the module hot side with a thin layer of silver loaded epoxy.
3. Place the module on the heat sink and rock slightly to squeeze out excess epoxy.
4. Weight or lightly clamp the module to hold it in place until the epoxy has cured.

Power supply considerations

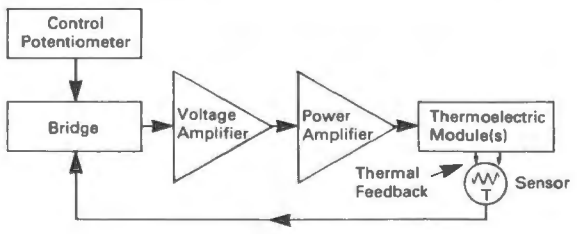
Figure 13 **Base power supplies**



Peltier devices operate from direct current and the power requirements are usually not stringent or precise. For most applications, unregulated dc power with a ripple content of 10% or less is satisfactory and it is possible that higher levels of ripple can be tolerated for certain non-critical applications. However, because this ripple will degrade module performance it is generally recommended that the ripple component be limited to 10% or less.

There are many methods of temperature controlling Peltier Devices in either open or closed loop modes. With open loop arrangements manual adjustment of the input current is made, normally by means of a variable power supply, and the temperature is thereby maintained reasonably near the desired set point.

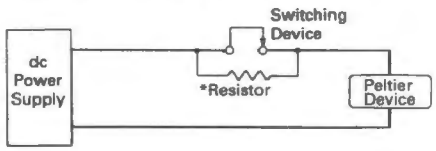
Figure 14 **Closed loop control block diagram**



With closed loop methods, a temperature sensor, such as a thermocouple, is used to sense the temperature of the device and appropriate electronic circuitry effects automatic control of the Peltier device current. Very precise control can be achieved by this method but relative cost and complexity are greater than for open loop arrangements.

RS data

Figure 15 **Improved switch control**



*The resistor value is selected to reduce the current to approximately 30% of the normal operating level. The optimum value may be determined experimentally.

In either of the above control arrangements a proportional on/off mark space control can be used but it has been found that premature module failure may occur because of the frequent expansion and contraction that results. When this means of control is adopted the arrangement of Figure 15 is recommended to reduce the thermal expansion effects.

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RS data

Universal asynchronous receiver transmitter 6402C

Stock number 630-689

The 6402C universal asynchronous receiver transmitter (UART) is intended for interfacing computers or microprocessors to asynchronous serial data channels. It is ideally suited to provide the necessary formatting and control for interfacing between serial and parallel data channels.

The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity and stop bits.

The transmitter converts parallel data into serial form and automatically adds start parity and stop bits.

The data word can be 5, 6, 7 or 8 bits in length. Parity may be odd, even or inhibited. Stop bits can be 1, 1.5 or 2 (when transmitting 5-bit code).

Absolute maximum ratings

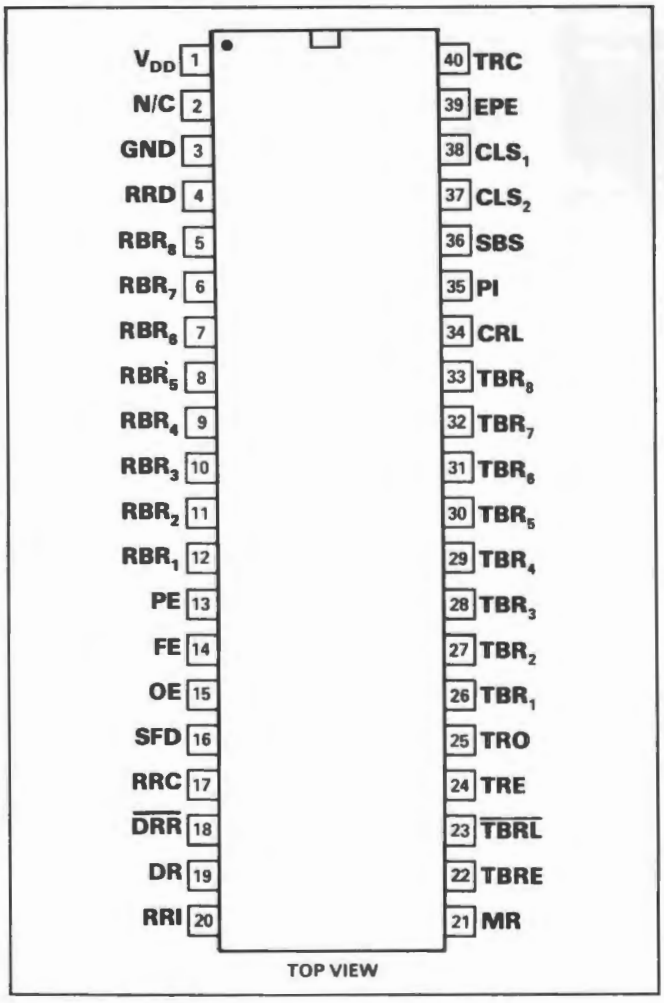
Supply voltage range (V_{DD}) ——— −0.5 to +7V
Input voltage range, all inputs −0.5V to V_{DD} +0.5V
dc input current, any one input ——— ±100μA
Power dissipation −40 to +60°C ——— 500mW
Derate linearly above +60°C at 12mW/°C to 200mW
Device dissipation per output transistor ——— 100mW
Operating temperature range ——— −40 to +85°C
Storage temperature range ——— −65 to 150°C
Load temperature (soldering 10s) ——— +265°C

Operating conditions at T_A = full package – temperature range. For maximum reliability, operating conditions should be selected so that operation is always within the following range.

Characteristic	Min.	Max.	Units
dc operating voltage range	4	6.5	V
Input voltage range	V_{SS}	V_{DD}	V

Features

- Low power – typically 7.5mW at 3.2MHz
- Baud rate – dc to 200k bits/s
- Automatic data formatting and status generation
- Programmable word length, stop bits and parity
- CMOS and LS TTL compatile.



TOP VIEW

ATTENTION

OBSERVE PRECAUTIONS FOR HANDLING

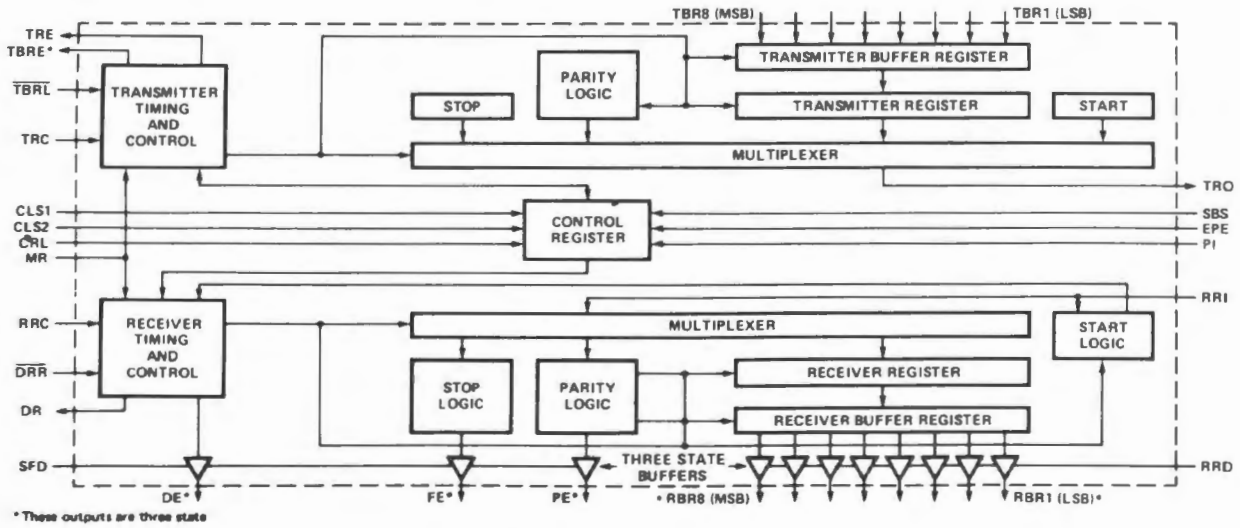
ELECTROSTATIC SENSITIVE DEVICES

Static electrical characteristics at $T_A = -40$ to $+85°C$, $V_{DD} \pm 10\%$, except as noted

Characteristic		V_O (V)	V_{IN} (V)	V_{DD} (V)	Min.	Typ.*	Max.	Units
Quiescent device current	I_{DD}	–	0,5	5	–	0.02	200	μA
Output low drive (sink) current	I_{OL}	0.4	0,5	5	1.2	2.4	–	mA
Output high drive (source) current	I_{OH}	4.6	0,5	5	–0.55	–1.1	–	
Output voltage low-level	V_{OL}‡	–	0,5	5	–	0	0.1	V
Output voltage high level	V_{OH}‡	–	0,5	5	4.9	5	–	
Input low voltage	V_{IL}	0.5, 4.5	–	5	–	–	0.8	
Input high voltage	V_{IH}	0.5, 4.5	–	5	V_{DD}–2.0	–	–	
Input leakage current	I_{IN}	Any input	0,5	5	–		±1	μA
3-state output leakage current	I_{OUT}	0,5	0,5	5	–	$\pm 10^{-4}$	±1	
Operating current	I_{DD1}#	–	0,5	5	–	1.5	–	mA
Input capacitance	C_{IN}	–	–	–	–	5	7.5	pF
Output capacitance	C_{OUT}	–	–	–	–	10	15	

*Typical values are for $T_A = 25°C$ and nominal V_{DD}. ‡$I_{OL} = I_{OH} = 1\mu A$.
#Operating current is measured at 200kHz or $V_{DD} = 5V$ with open outputs (system operating at maximum speed of 3.2MHz).

Figure 1 **Block diagram**



Description of operation

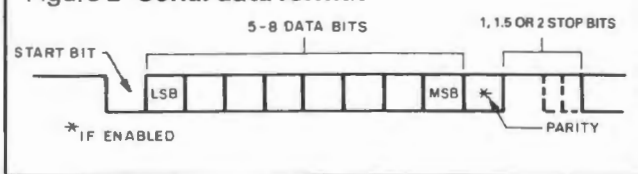
Initialisation and controls

A positive pulse on the Master Reset (MR) input resets the control, status, and receiver buffer registers, and sets the serial output (TRO) High. Timing is generated from the clock inputs RRC and TRC at a frequency equal to 16 times the serial data bit rate. The RRC and TRC inputs may be driven by a common clock, or may be driven independently by two different clocks. The Control Register Load (CRL) input is strobed to load control bits for Parity Inhibit (PI), Even Parity Enable (EPE), Stop Bit Selects (SBS), and Character Length Selects (CLS1 and CLS2). These inputs may be hand wired to V_{SS} or V_{DD} with CRL to V_{DD}. When the initialisation is completed, the UART is ready for receiver and/or transmitter operations.

Transmitter operation

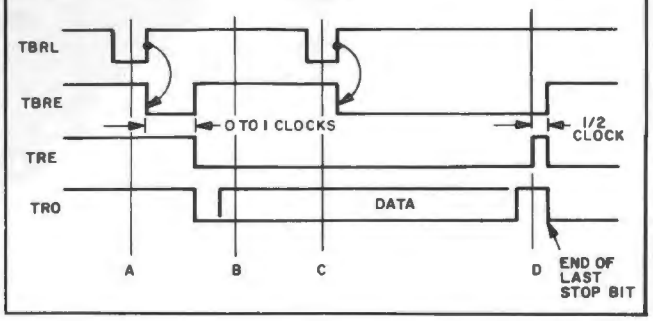
The transmitter section accepts parallel data, formats it, and transmits it in serial form (Figure 2) on the TRO terminal. Transmitter timing is shown in Figure 3. (A) Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{TBRL}$ input. Valid data must be present at least t_{DT} prior to, and t_{TD} following, the rising edge of $\overline{TBRL}$. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. (B) The rising edge of $\overline{TBRL}$ clears TBRE. Zero to 1 clock cycle later data is transferred to the transmitter register and TRE is cleared and trans-

Figure 2 **Serial data format**



mission starts. TBREmpty is reset to a logic high. Output data is clocked by TRC. The clock rate is 16 times the data rate. (C) A second pulse on $\overline{TBRL}$ loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of the character begins.

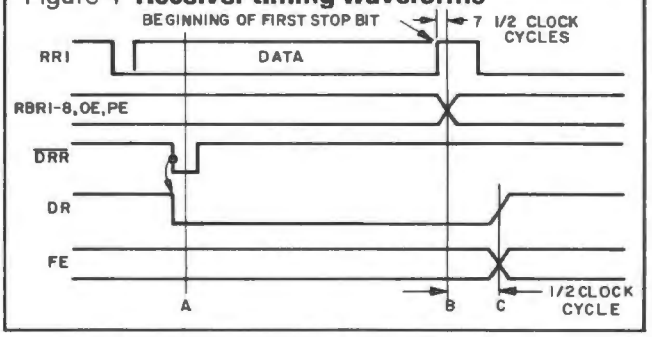
Figure 3 **Transmitter timing diagrams**



Receiver operation

Data is received in serial form at the RRI input. When no data is being received, RRI input must remain high. The data is clocked through the RRC.

Figure 4 **Receiver timing waveforms**



The clock rate is 16 times the data rate. Receiver timing is shown in Figure 4.

(A) A low level on $\overline{DRR}$ clears the DR line. (B) During the first stop bit data is transferred from the receiver register to the RB register. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OE indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. A logic high on PE indicates a parity error. (C) ½ clock cycle later DR is set to a logic high and FE is evaluated. A logic high on FE indicates an invalid stop bit was received.

Start bit detection

The receiver uses a 16X clock for timing (Figure 5). The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The centre of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the centre of the start bit will be located within ±½ clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at 9 clocks into the first stop bit.

Figure 5 **Start bit timing waveforms**

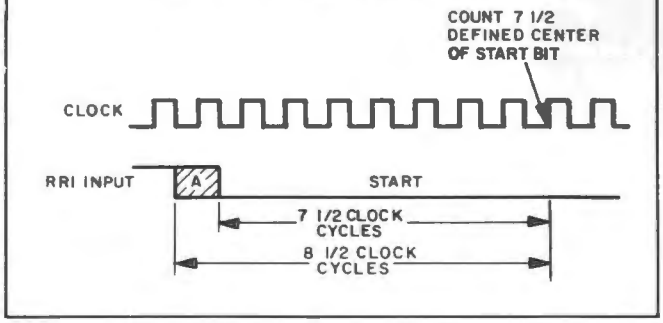


Table 1 **Control word function**

Control word					Data bits	Parity bit	Stop bit(s)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	Odd	1
L	L	L	L	H	5	Odd	1.5
L	L	L	H	L	5	Even	1
L	L	L	H	H	5	Even	1.5
L	L	H	X	L	5	Disabled	1
L	L	H	X	H	5	Disabled	1.5
L	H	L	L	L	6	Odd	1
L	H	L	L	H	6	Odd	2
L	H	L	H	L	6	Even	1
L	H	L	H	H	6	Even	2
L	H	H	X	L	6	Disabled	1
L	H	H	X	H	6	Disabled	2
H	L	L	L	L	7	Odd	1
H	L	L	L	H	7	Odd	2
H	L	L	H	L	7	Even	1
H	L	L	H	H	7	Even	2
H	L	H	X	L	7	Disabled	1
H	L	H	X	H	7	Disabled	2
H	H	L	L	L	8	Odd	1
H	H	L	L	H	8	Odd	2
H	H	L	H	L	8	Even	1
H	H	L	H	H	8	Even	2
H	H	H	X	L	8	Disabled	1
H	H	H	X	H	8	Disabled	2

X = Don't Care

Table II **Function pin definition**

Pin	Symbol	Description
1	V_{DD}	Positive Power Supply
2	N/C	No Connection
3	GND	Ground (V_{SS})
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See pin 5 – RBR8.
7	RBR6	
8	RBR5	
9	RBR4	
10	RBR3	
11	RBR2	
12	RBR1	
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if DRR has been performed (ie. DRR; active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	RRC	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DDR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register, and is required after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transistion on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.

Table II **Function pin definition (cont'd)**

Pin	Symbol	Description
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	TBR1	Character data is loaded into TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length.
27	TBR2	See pin 26 – TBR1.
28	TBR3	
29	TBR4	
30	TBR5	
31	TBR6	
32	TBR7	
33	TBR8	
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs programme the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits) CLS1 high CLS2 low 6-bits) CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits).
38	CLS1*	See pin 37 – CLS2.
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	TRC	The TRANSMITTER REGISTER CLOCK is 16 × the transmit data rate.

*See Table 1 (Control Word Function)

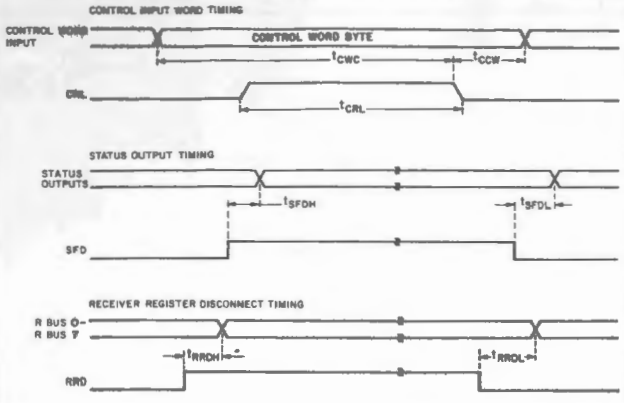
Dynamic electrical characteristics at T_A = –40 to +85°C, V_{DD} ± 5%, t_r, t_f = 20ns, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$, C_L = 100pF

System timing (see Figure 6)

Characteristic		V_{DD} (V)	Limits Typ.[1]	Limits Max.[2]	Units
Minimum pulse width: CRL	t_{CRL}	5	50	150	ns
Minimum setup time control word to CRL	t_{CWC}	5	20	50	
Minimum hold time control word after CRL	t_{CCW}	5	40	60	
Propagation delay time SFD high to SOD	t_{SFDH}	5	130	200	
SFD low to SOD	t_{SFDL}	5	130	200	
RRD high to receiver register high impedance	t_{RRDH}	5	80	150	
RRD low to receiver register active	t_{RRDL}	5	80	150	

[1]Typical values for T_A = 25°C and nominal V_{DD}.
[2]Maximum limits of minimum characteristics are the values above which all devices function.

Figure 6 **System timing waveforms**

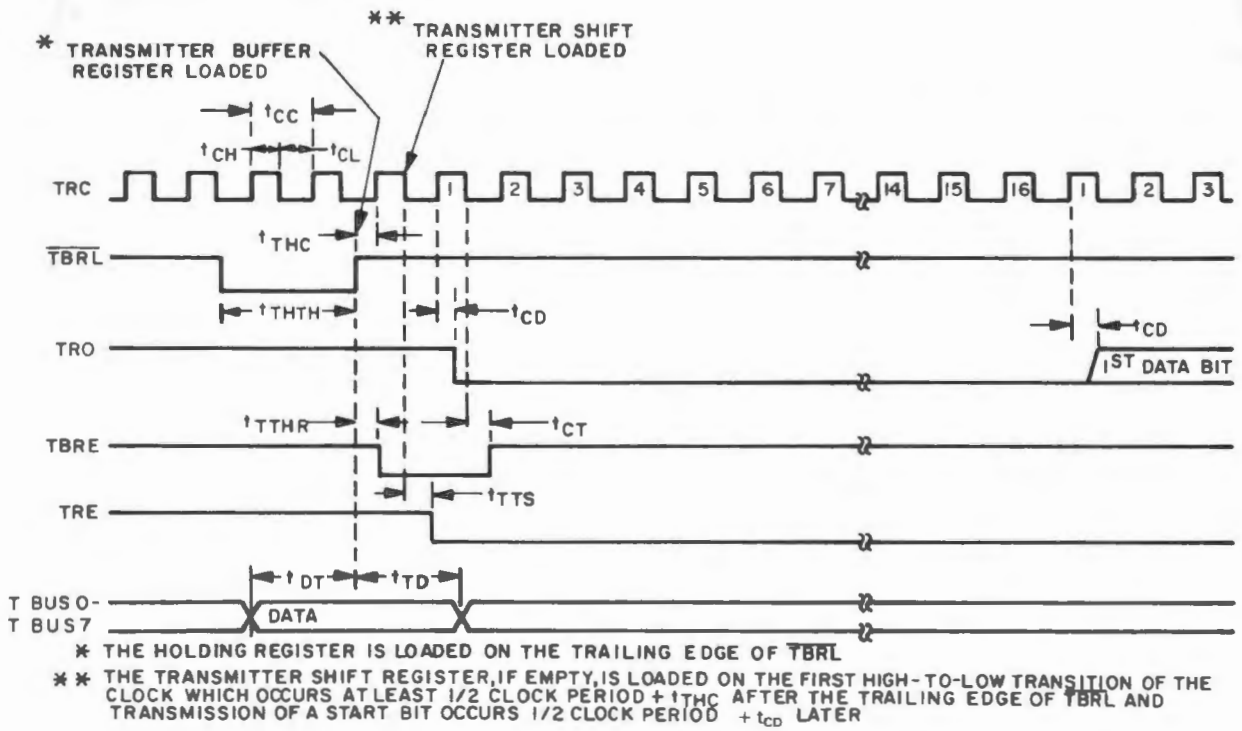


Transmitter timing (see Figure 7)

Characteristic		V_{DD} (V)	Limits Typ.[1]	Limits Max.[2]	Units
Minimum clock period (TRC)	t_{CC}	5	250	310	ns
Minimum pulse width: Clock low level	t_{CL}	5	100	125	
Clock high level	t_{CH}	5	100	125	
$\overline{TBRL}$	t_{THTH}	5	80	200	
Minimum setup time: $\overline{TBRL}$ to clock	t_{THC}	5	175	275	
Data to $\overline{TBRL}$ ↓	t_{DT}	5	20	50	
Minimum hold time: Data after $\overline{TBRL}$ ↓	t_{TD}	5	40	60	
Propagation delay time: Clock to data start bit	t_{CD}	5	300	450	
Clock to TBRE	t_{CT}	5	330	400	
$\overline{TBRL}$ to TBRE	t_{TTHR}	5	200	300	
Clock to TRE	t_{TTS}	5	330	400	

[1] Typical values for $T_A = 25°C$ and nominal V_{DD}.
[2] Maximum limits of minimum characteristics are the values above which all devices function.

Figure 7 **Transmitter timing waveforms**



* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF $\overline{TBRL}$

** THE TRANSMITTER SHIFT REGISTER, IF EMPTY, IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD + t_{THC} AFTER THE TRAILING EDGE OF $\overline{TBRL}$ AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER

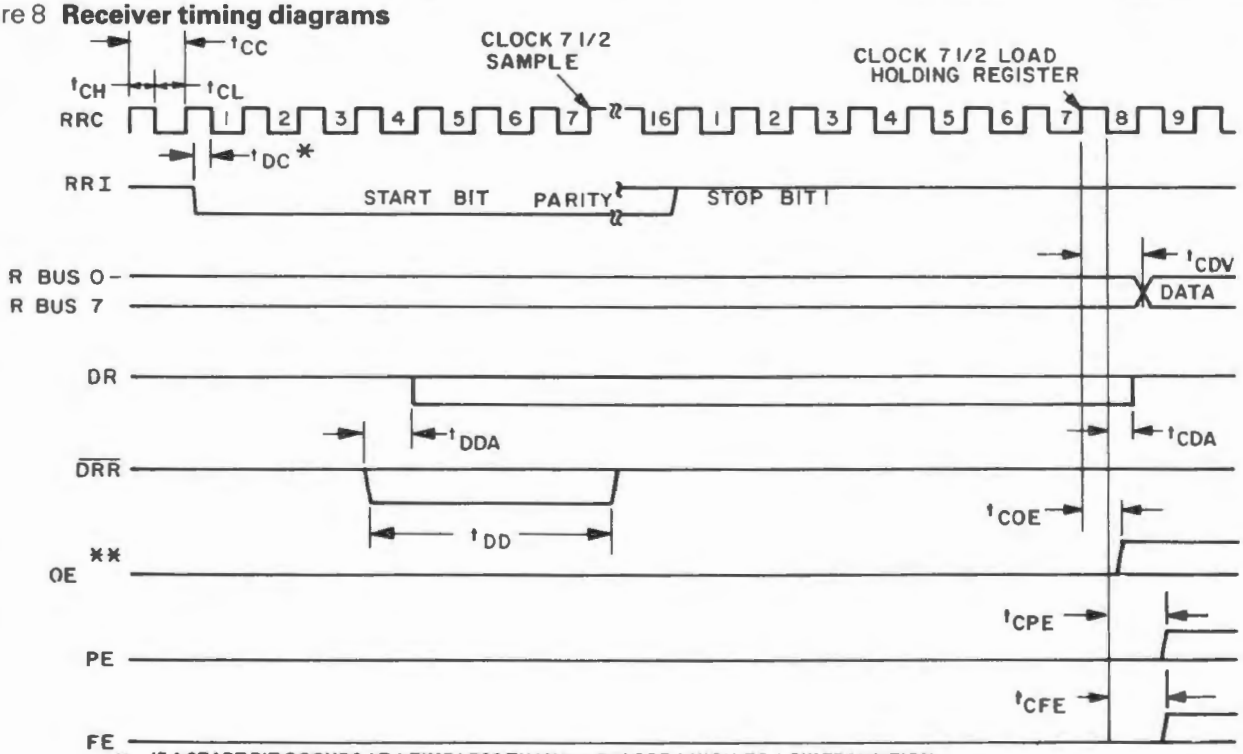
RS data

Receiver timing (see Figure 8)

Characteristic		V_{DD} (V)	Limits Typ.[1]	Limits Max.[2]	Units
Minimum clock period (RRC)	t_{CC}	5	250	310	ns
Minimum pulse width: Clock low level	t_{CL}	5	100	125	
Clock high level	t_{CH}	5	100	125	
$\overline{\text{Data Received Reset}}$	t_{DD}	5	50	75	
Minimum setup time: Data start bit to clock	t_{DC}	5	100	150	
Propagation delay time: $\overline{\text{Data Received Reset}}$ to Data Received	t_{DDA}	5	150	250	
Clock to Data Valid	t_{CDV}	5	275	400	
Clock to DR	t_{CDA}	5	275	400	
Clock to Overrun Error	t_{COE}	5	275	400	
Clock to Parity Error	t_{CPE}	5	240	375	
Clock to Framing Error	t_{CFE}	5	200	300	

[1] Typical values for $T_A = 25°C$ and nominal V_{DD}.
[2] Maximum limits of minimum characteristics are the values above which all devices function.

Figure 8 **Receiver timing diagrams**



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

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RS data

Tuned radio frequency receivers ZN414Z and ZN416E

Stock numbers 307-266 and 630-550

Two tuned radio frequency (TRF) circuits that provide a complete RF Amplifier, detector and AGC circuit on one chip.

The ZN414Z is a 10 transistor TRF circuit packaged in a 3 pin TO-92 case. The circuit requires six external components only to give a high quality AM tuner. Effective AGC action is available and is simply adjusted by selecting one external resistor value. Excellent audio quality can be achieved and current consumption is extremely low. No setting up or alignment is required and the circuit is completely stable in use.

The ZN414Z will drive a sensitive earpiece directly. In this case, an earpiece of equivalent impedance to R_{AGC} is substituted for R_{AGC} in the basic tuner circuit. Unfortunately, the cost of a sensitive earpiece is high, and unless an ultra-miniature radio is wanted, it is considerably cheaper to use a low cost crystal earpiece and add a single gain stage.

The ZN416E is a buffered output version of the ZN414Z in an 8 pin DIL package, giving typically 120mV (rms) output into a 64Ω load.

Features

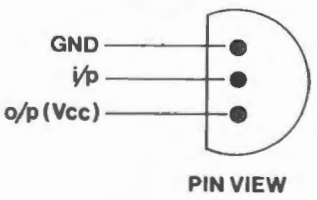
- Single cell operation (1.1 to 1.6V operating range)
- Low current consumption
- 150kHz to 3MHz frequency range (ie. full coverage of medium and long wavebands)
- Easy assembly, no alignment necessary
- Simple and effective AGC action
- Will drive crystal earphone direct (ZN414Z)
- Will drive headphones direct (ZN416E)
- Excellent audio quality
- Typical power gain of 72dB (ZN414Z)
- Minimum number of external components required.

Electrical characteristics $T_A = 25°C$, $V_{CC} = 1.4V$

Parameters apply to both devices unless otherwise stated.

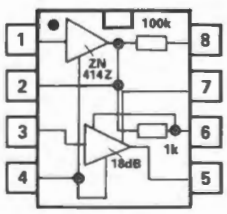
Parameter		Min.	Typ	Max.	Units
Supply voltage, V_{CC}		1.1	1.3	1.6	volts
Supply current, I_S	ZN414Z	–	0.3	0.5	mA
Supply current, I_S with 64Ω headphones	ZN416E	–	4	5	mA
Input frequency range		0.15	–	3.0	MHz
Input resistance		–	4.0	–	MΩ
Threshold sensitivity (Dependent on Q of coil)		–	50	–	μV
Selectivity		–	4.0	–	kHz
Total harmonic distortion		–	3.0	–	%
AGC range		–	20	–	dB
Power gain	ZN414Z	–	72	–	dB
Voltage gain of output stage	ZN416E	–	18	–	dB
Output voltage before clipping	ZN414Z	–	60	–	mVpp
Output voltage into 64Ω load before clipping	ZN416E	–	340	–	mVpp
Upper cut-off frequency of output stage, No capacitor	ZN416E	20	–	–	kHz
With 0.01μF between pin 7 and 0V	ZN416E	–	10	–	kHz
Lower cut-off frequency of output stage 0.47μF between pins 2 and 3	ZN416E	–	50	–	Hz
Quiescent output voltage	ZN414Z	–	40	–	mV
	ZN416E	–	200	–	mV
Operating temperature range		0	–	+70	°C
Maximum storage temperature		–65	–	+125	°C

ZN414Z



PIN VIEW

ZN416E



TOP VIEW

ZN414Z Characteristics

Figure 1 **Gain and AGC characteristics**

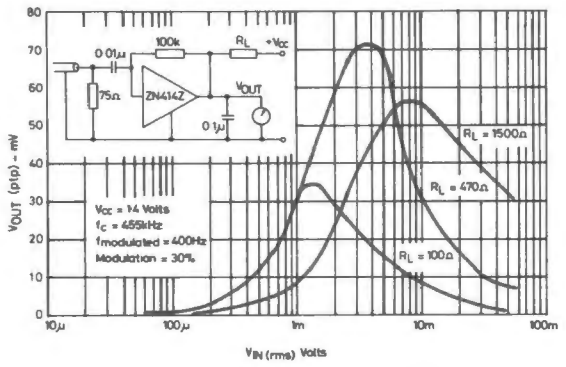
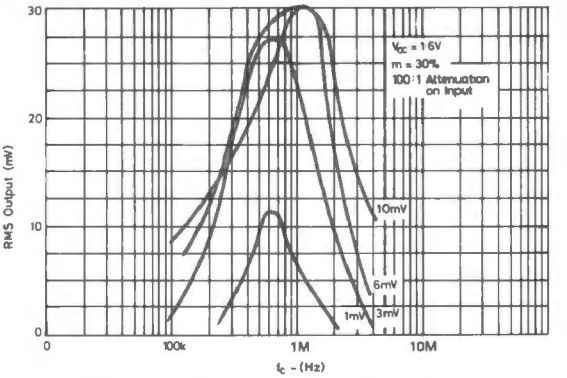


Figure 2 **Frequency response**



*Note that this graph represents the chip response, and not the receiver bandwidth.

Figure 3 **Gain variation with supply volts**

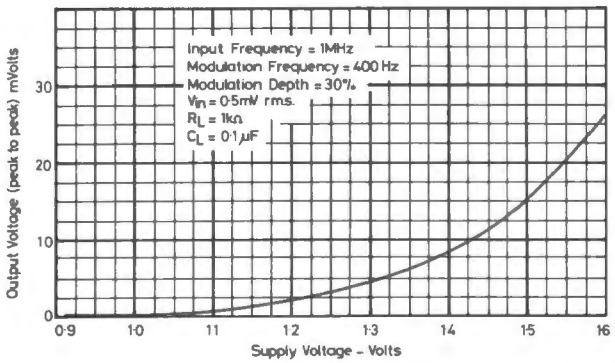
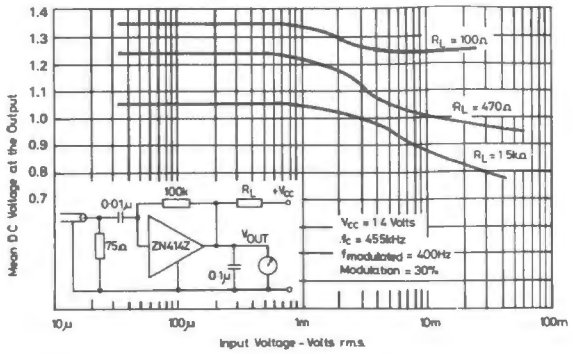


Figure 4 **DC level at output**



Layout requirements

As with any high gain RF device, certain basic layout rules must be adhered to if stable and reliable operation is to be obtained. These are listed below:

1. The output decoupling capacitor should be soldered as near as possible to the output and earth leads of the ZN414Z. Furthermore, its value together with the AGC resistor (R_{AGC}) should be calculated at ≈ 4kHz, ie.:

$$C\,(\text{farads}) = \frac{1}{2\pi \times R_{AGC} \times 4 \times 10^3}$$

2. All leads should be kept as short as possible, especially those in close proximity to the ZN414Z.
3. The tuning assembly should be some distance from the battery, loudspeaker and their associated leads.
4. The 'earthy' side of the tuning capacitor should be connected to the junction of the 100kΩ resistor and the 0.01µF capacitor.

Operating notes

Selectivity

To obtain good selectivity, essential with any TRF device, the ZN414Z must be fed from an efficient, high 'Q' coil and capacitor tuning network. With suitable components the selectivity is comparable to superhet designs, except that a very strong signal in proximity to the receiver may swamp the device unless the ferrite rod aerial is rotated to 'null-out' the strong signal.

Gain (AGC)

To obtain optimum results using the ZN414Z it is important that the AGC mechanism is understood. Signal strength, ferrite rod size and the 'Q' of the coil all affect the signal ultimately presented to the AGC network. To compensate for these variables, the gain of the chip is variable, by varying the supply voltage (see Figure 3). With the gain set too high, the AGC circuit will swamp, causing strong stations to appear to occupy large bandwidths. The effect is similar to poor selectivity, except that in extreme cases distortions may also occur. If the gain is set too low, the signal-to-noise ratio worsens. A compromise between the two extremes is needed, and whilst the circuits given in this data sheet work adequately under most operating con-

ditions, the experimenter may well like to note the effect of varying the supply voltage to the ZN414Z with a view to optimising for his individual requirements.

The value of the AGC resistor may be varied; for most applications 1.5kΩ represents the optimum value. For some earpiece circuits, where the operating requirements are somewhat different, 680Ω gives better results. If the value of the resistor is altered, note that the supply current for the ZN414Z flows through it (typically 0.3mA), and the supply voltage will also have to be changed.

$V_{ZN414} = V_{supply} - 0.3\ R_{AGC}$ where R_{AGC} is in kilohms.

The voltage, and hence gain, of the ZN414Z can be increased until instability results. A further gain increase, at the expense of audio quality, can be achieved by increasing the capacitor across the output and earth terminals from 0.22μF up to a maximum of 0.82μF.

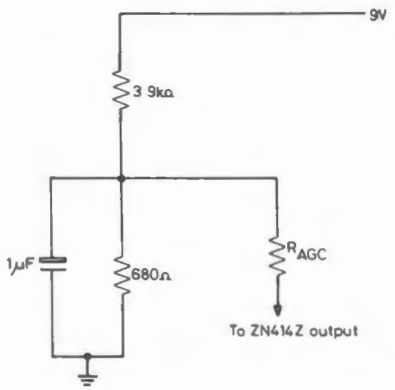
Ferrite aerial size

Because of the gain variation available by altering supply voltage, the size of the ferrite rod is relatively unimportant. However, the ratio of aerial rod length to diameter should ideally be large to give the receiver better directional properties. Successful receivers have been constructed with ferrite rod aerials of 4cm (1.5in) and up to 20cm (8in).

Drive circuits ZN414Z

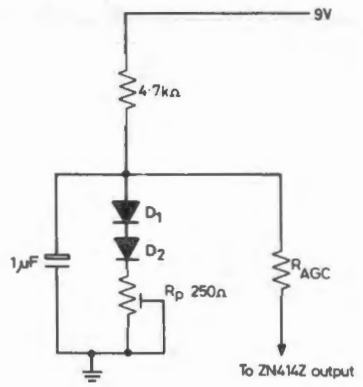
Three types of drive circuit are shown, each has been used successfully. The choice is largely an economic one, but Figure 7 is recommended wherever possible, having several advantages over the other circuits. Values for 9V supplies are shown, simple calculations will give values for other supplies.

Figure 5 **Resistive divider**



Note: Replacing the 680Ω resistor with a 500Ω resistor and a 250Ω preset, sensitivity may be adjusted and will enable optimum reception to be realised under most conditions.

Figure 6 **Diode drive**

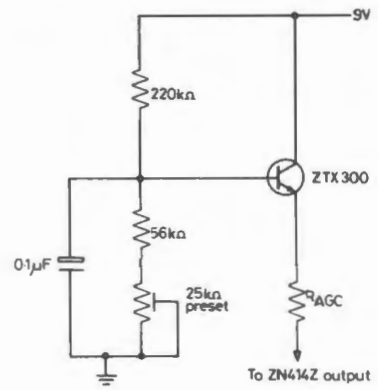


$D_1 = D_2$ = Any general purpose silicon diode

R_p = Optional sensitivity control, a recommended value being 250Ω.

Current consumption ≈ 1.5mA

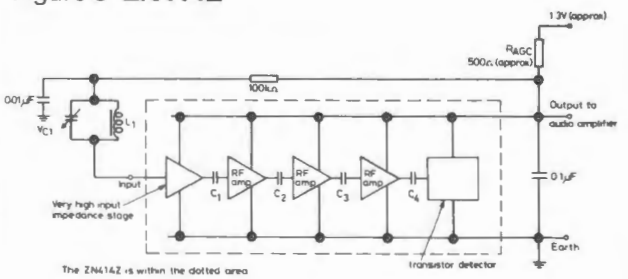
Figure 7 **Transistor drive**



Current consumption is virtually that which is taken by the ZN414Z (0.3mA)

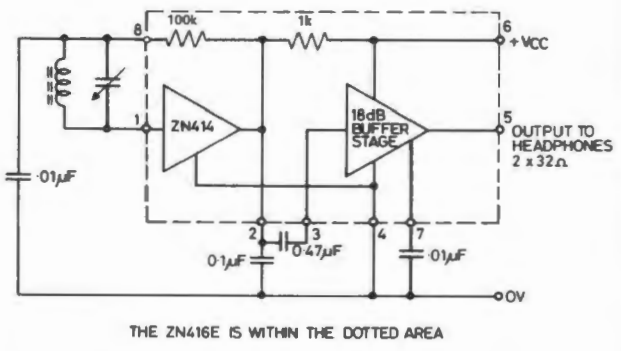
Applications information

Figure 8 **ZN414Z**



RS data

Figure 9 **ZN416E**



THE ZN416E IS WITHIN THE DOTTED AREA

©RS Components Ltd. 1985

RS data

Real time clock ic 58274

Stock number 630-601

The 58274 is fabricated using low threshold metal gate CMOS technology and is designed to operate in bus oriented microprocessor systems where a real time clock and calendar function are required. The on-chip 32.768kHz crystal controlled oscillator will maintain timekeeping down to 2.2V to allow low power standby battery operation. This device is pin compatible with the 58174A but continues timekeeping up to tens of years. Faster access times are also offered.

Absolute maximum ratings

Voltage at all inputs and outputs
V_{DD} +0.3V to V_{SS} –0.3V
$V_{DD} - V_{SS}$ ——— 6.5V
Operating temperature ——— –40°C to +85°C
Storage temperature ——— –65°C to +150°C
Lead temperature soldering 10s ——— 300°C

ATTENTION

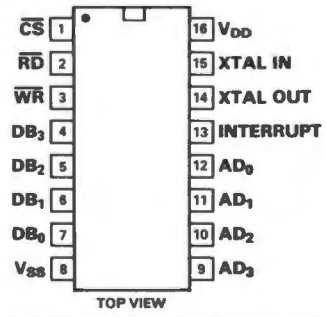
OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

Features

- Same pin-out as 58174A
- Timekeeping from tenths of seconds to tens of years in independently accessible registers
- Hours counter is programmable for 12 or 24 hour operation
- Buffered crystal frequency output is available in test mode for accurate oscillator setting
- A data changed flag allows simple testing for rollover error
- Independent interrupt timer
- Fully TTL compatible
- Low power standby operation 10μA at 2.2V
- Single 5V supply.

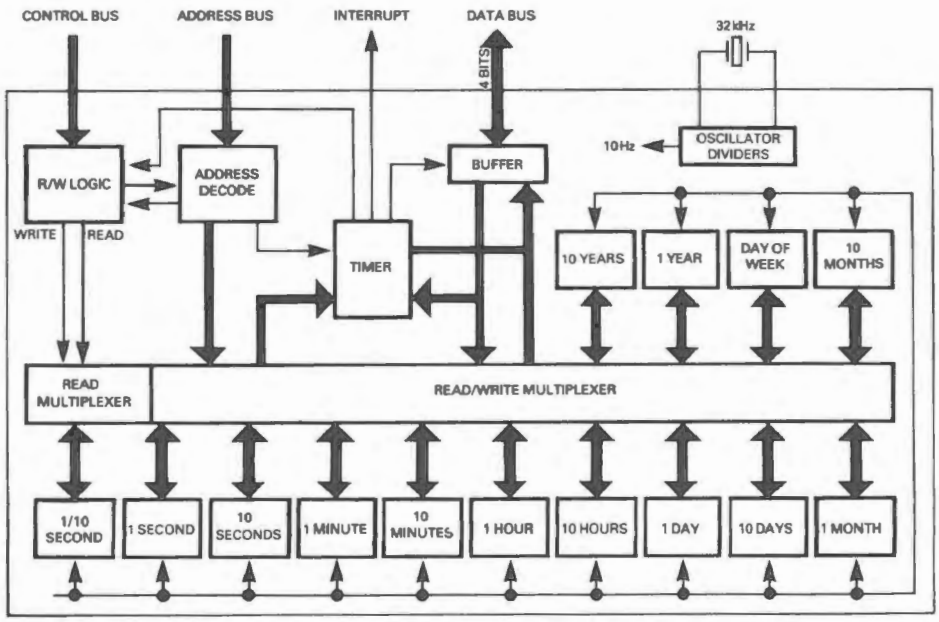
Pin connections



Electrical characteristics T_A = –40°C to +85°C, V_{DD} = 5V ±0.5V unless otherwise stated.

Parameter		Conditions	Min.	Typ.	Max.	Units
V_{DD} Supply voltage		Standby mode (No read or write instructions)	2.2			V
		Operational mode	4.5		5.5	V
I_{DD} Supply current		Standby mode (V_{DD} = 2.2V)		4	10	μA
		Operational mode (V_{DD} = 5V)		1		mA
Logic level inputs (except XTAL IN)						
High input voltage V_{IH}			2.0			V
Low input voltage V_{IL}					0.8	V
Input capacitance					10	pF
Input current levels AD_0 to AD_3 and DB_0 to DB_3		Active pull-ups to V_{DD}, V_{IN} = V_{SS}, V_{DD} = 5V			20	μA
Internal resistor to V_{DD}						
WR			30	100		kΩ
RD			30	100		kΩ
CS			10	40		kΩ
Output logic levels						
DB_0 to DB_3	Logic 1	I_{OH} = 0.2mA	2.4			V
	Logic 0	I_{OL} = 3.2mA			0.4	V
Interrupt	Logic 0	I_{OL} = 3.2mA			0.4	V
	Off leakage				2	μA

Figure 1 **Block diagram**



Functional description

The 58274 is a bus oriented microprocessor real time clock. It has the same pin-out as the 58174A while offering extended timekeeping up to units and tens of years. To enhance the device further, a number of other features have been added including: 12 or 24 hours counting, a testable data-changed flag giving easy error-free time reading and simplified interrupt control.

A buffered oscillator signal appears on the interrupt output when the device is in test mode. This allows for easy oscillator setting when the device is initially powered up in a system.

The counters are arranged as 4-bit words and can be randomly accessed for the time reading and setting. The counters output in BCD (binary coded decimal) 4-bit numbers. Any register which has less than 4 bits (eg., days of week uses only 3 bits) will return a logic 0 on any unused bits. When written to, the unused inputs will be ignored.

Writing a logic 1 to the clock start/stop control bit resets the internal oscillator divider chain and the tenths of seconds counter. Writing a logic 0 will start the clock timing from the nearest second. The time then updates every 10ms with all counters changing synchronously. Time changing during a read is detected by testing the data-changed bit of the control register after completing a string of clock register reads.

Interrupt delay times of 0.1s, 0.5s, 1s, 5s, 10s, 30s or 60s can be selected with single or repeated interrupt outputs. The open drain output is pulled low whenever the interrupt timer times out and is cleared by reading the control register.

Circuit description

The block diagram in Figure 1 shows the internal structure of the chip. The 16-pin package outline is shown on Page 1.

Crystal oscillator

This consists of a CMOS inverter/amplifier with an on-chip bias resistor. Externally a 20pF capacitor, a trimmer capacitor and a crystal are required to complete the 32.768kHz timekeeping oscillator circuit.

The trimmer capacitor fine tunes the crystal load impedance, optimising the oscillator stability. When properly adjusted (ie., to the crystal frequency of 32.768kHz), the circuit will display a frequency variation with voltage of less than 3ppm/V.

When the chip is enabled into test mode, the oscillator is gated onto the interrupt output pin giving a buffered oscillator output that can be used to set the crystal frequency when the device is installed in a system. For further information see the section on Test mode.

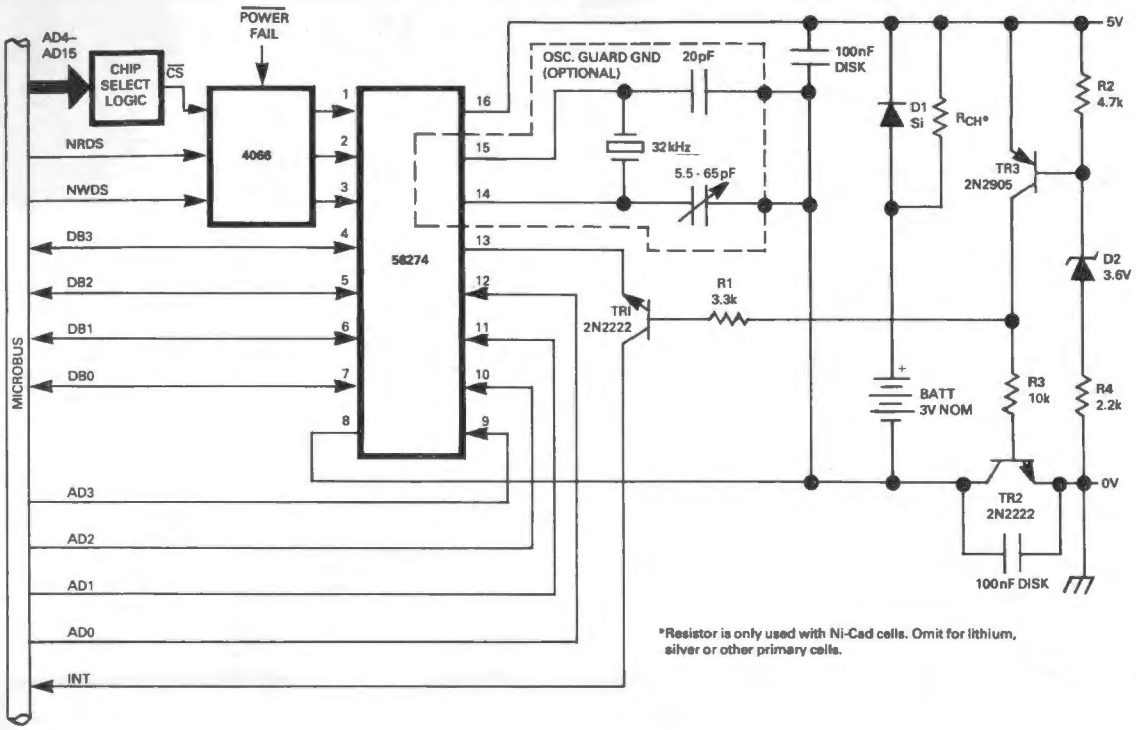
Divider chain

The crystal oscillator is divided down in three stages to produce a 10Hz frequency setting pulse. The first stage is a non-integer divider which reduces the 32.768kHz input to 30.720kHz. This is further divided by a 9-stage binary ripple counter giving an output frequency of 60Hz. A 3-stage Johnson counter divides this by six, generating a 10Hz output. The 10Hz clock is gated with the 32.768kHz crystal frequency to provide clock setting pulses of 15.26μs duration. The setting pulse drives all the time registers on the device which are synchronously clocked by this signal. All time data and the data-changed flag change on the falling edge of the clock setting pulse.

Data-changed flag

The data-changed flag is set by the clock setting pulse to indicate that the time data has been altered since the clock was last read. This flag occupies bit 3 of the control register where it can be tested by the processor to sense data-changed. It will be reset by a read of the control register. See the section, 'Methods of device operation', for suggested clock reading techniques using this flag.

Figure 2 **Typical system connection diagram**



Seconds counters
There are three counters for seconds:
a) tenths of seconds
b) units of seconds
c) tens of seconds.
The registers are accessed at the addresses shown in Table 1. The tenths of seconds register is reset to 0 when the clock start/stop bit (bit 2 of the control register) is set to logic 1. The units and tens of seconds are set up by the processor, giving time setting to the nearest second. All three registers can be read by the processor for time output.

Minutes counters
There are two minutes counters:
a) units of minutes
b) tens of minutes.
Both registers may be read to or written from as required.

Hours counters
There are two hours counters:
a) units of hours
b) tens of hours.
Both counters may be accessed for read or write operations as desired.
In 12-hour mode, the tens of hours register has only one active bit and the top three bits are set to logic 0. Data bit 1 of the clock setting register is the AM/PM indicator; logic 0 indicating AM, logic 1 for PM.
When 24-hour mode is programmed, the tens of hours register reads out two bits of data and the two most significant bits are set to logic 0. There is no AM/PM indication and bit 1 of the clock setting register will read out a logic 0.
In both 12/24-hour modes, the units of hours will read out four active data bits. 12 or 24-hour mode is selected by bit 0 of the clock setting register; logic 0 for 12-hour mode, logic 1 for 24-hour mode.

Days counters
There are two days counters:
a) units of days
b) tens of days.
The days counters will count up to 28, 29, 30 or 31 depending on the state of the months counters and the leap year counter. The microprocessor has full read/write access to these registers.

Months counters
There are two months counters:
a) units of months
b) tens of months.
Both these counters have full read/write access.

Years counters
There are two years counters:
a) units of years
b) tens of years.
Both these counters have full read/write access. The years will count up to 99 and roll over to 00.

Table 1 **Address decoding of real-time clock internal registers**

Register selected	Address (Binary)				(Hex)	Access
	AD3	AD2	AD1	AD0		
0 Control Register	0	0	0	0	0	Split Read and Write
1 Tenths of Seconds	0	0	0	1	1	Read Only
2 Units Seconds	0	0	1	0	2	R/W
3 Tens Seconds	0	0	1	1	3	R/W
4 Units Minutes	0	1	0	0	4	R/W
5 Tens Minutes	0	1	0	1	5	R/W
6 Units Hours	0	1	1	0	6	R/W
7 Tens Hours	0	1	1	1	7	R/W
8 Units Days	1	0	0	0	8	R/W
9 Tens Days	1	0	0	1	9	R/W
10 Units Months	1	0	1	0	A	R/W
11 Tens Months	1	0	1	1	B	R/W
12 Units Years	1	1	0	0	C	R/W
13 Tens Years	1	1	0	1	D	R/W
14 Day of Week	1	1	1	0	E	R/W
15 Clock Setting/ Interrupt Registers	1	1	1	1	F	R/W

Day of week counter

The day of week counter increments as the time rolls from 23:59 to 00:00 (11:59 PM to 12:00 AM in 12-hour mode). It counts from 1 to 7 and rolls back to 1. Any day of the week may be specified as day 1.

Clock setting register/Interrupt register

The interrupt select bit in the control register determines which of these two registers is accessible to the processor at address 15. Normal clock and interrupt timing operations will always continue regardless of which register is selected onto the bus. The layout of these registers is shown in Table 2.

The clock setting register is comprised of three separate functions:

a) leap year counter: bits 2 and 3

b) AM/PM indicator: bit 1

c) 12/24-hour mode set: bit 0 (see Table 2A).

The leap year counter is a 2-stage binary counter which is clocked by the months counter. It changes state as the time rolls over from 11:59 on December 31 to 00:00 on January 1.

The counter should be loaded with the 'number of years since last leap year' eg., if 1980 was the last leap year, a clock programmed in 1983 should have 3 stored in the leap year counter. If the clock is programmed during a leap year, then the leap year counter should be set to 0. The contents of the leap year counter can be read by the μP.

The AM/PM indicator returns a logic 0 for AM and a logic 1 for PM. It is clocked when the hours counter rolls from 11:59 to 12:00 in 12-hour mode. In 24-hour mode this bit is set to logic 0.

The 12/24-hour mode set determines whether the hours counter counts from 1 to 12 or from 0 to 23. It also controls the AM/PM indicator, enabling it for 12-hour mode and forcing it to logic 0 for the 12-hour mode. The 12/24-hour mode bit is set to logic 0 for 12-hour mode and it is set to logic 1 for 24-hour mode.

Important note: hours mode and AM/PM bits cannot be set in the same write operation. See the section on initialisation (Methods of device operation) for a suggested setting routine.

All bits in the clock setting register may be read by the processor.

The interrupt register controls the operation of the timer for interrupt output. The processor programmes this register for single or repeated interrupts at the selected time intervals.

The lower three bits of this register set the time delay period that will occur between interrupts. The time delays that can be programmed and the data words that select these are outlined in Table 2B.

Data bit 3 of the interrupt register sets for either single or repeated interrupts; logic 0 gives single mode, logic 1 sets for repeated mode.

Using the interrupt is described in the Device operation section.

Table 2A **Clock setting register layout**

Function	Data Bits Used				Comments	Access
	DB3	DB2	DB1	DB0		
Leap Year Counter	X	X			0 Indicates a Leap Year	R/W
AM/PM Indicator (12-Hour Mode)			X		0 =AM 1 = PM 0 in 24-Hour Mode	R/W
12/24-Hour Select Bit				X	0 = 12-Hour Mode 1 = 24-Hour Mode	R/W

Table 2B **Interrupt control register**

Function	Comments	Control Word			
		DB3	DB2	DB1	DB0
No Interrupt	Interrupt output cleared, start/stop bit set to 1.	X	0	0	0
0.1 Second	DB3 = 0 for single interrupt DB3 = 1 for repeated interrupt	0/1	0	0	1
0.5 Second		0/1	0	1	0
1 Second		0/1	0	1	1
5 Seconds		0/1	1	0	0
10 Seconds		0/1	1	0	1
30 Seconds		0/1	1	1	0
60 Seconds		0/1	1	1	1
Timing Accuracy: single interrupt mode (all time delays): ± 1 ms Repeated Mode: ±1 ms on initial timeout, thereafter synchronous with first interrupt (ie., timing errors do not accumulate).					

Control register

There are three registers which control different operations of the clock:

a) the clock setting register

b) the interrupt register.

c) the control register.

The clock setting and interrupt registers both reside at address 15, access to one or the other being controlled by the interrupt select bit; data bit 1 of the control register.

The clock setting register programmes the timekeeping of the clock. The 12/24-hour mode select and the AM/PM indicator for 12-hour mode occupy bits 0 and 1, respectively. Data bits 2 and 3 set the leap year counter.

The interrupt register controls the operation of the interrupt timer, selecting the required delay period and either single or repeated interrupt.

The control register is responsible for controlling the operations of the clock and supplying status information to the processor. It appears as two different registers; one with write only access and one with read only access.

The write only register consists of a bank of four latches which control the internal processes of the clock.

The read only register contains two output data latches which will supply status information for the

processor. Table 3 shows the mapping of the various control latches and status flags in the control register. The control register is located at address 0.

The write only portion of the control register contains four latches.

A logic 1 written into the test bit puts the device into test mode. This allows setting of the oscillator frequency as well as rapid testing of the device registers, if required. A more complete description is given in the Test mode section. For normal operation the test bit is loaded with logic 0.

The clock start/stop bit stops the timekeeping of the clock and resets to 0 the tenths of seconds counter. The time of day may then be written into the various clock registers and the clock restarted synchronously with an external time source. Timekeeping is maintained thereafter.

A logic 1 written to the start/stop bit halts clock timing. Timing is restarted when the start/stop bit is written with a logic 0.

The interrupt select bit determines which of the two registers mapped onto address 15 will be accessed when this address is selected.

A logic 0 in the interrupt select bit makes the clocksetting register available to the processor. A logic 1 selects the interrupt register.

The interrupt start/stop bit controls the running of the interrupt timer. It is programmed in the same way as the clock start/stop bit; logic 1 to halt the interrupt and reset the timer, logic 0 to start interrupt timing.

When no interrupt is programmed (interrupt control register set to 0), the interrupt start/stop bit is automatically set to a logic 1. When any new interrupt is subsequently programmed, timing will not commence until the start/stop bit is loaded with 0.

In the single interrupt mode, interrupt timing stops when a timeout occurs. The processor restarts timing by writing logic 0 into the start/stop bit.

In repeated interrupt mode the interrupt timer continues to count with no intervention by the processor necessary.

Interrupt timing may be stopped in either mode by writing a logic 1 into the interrupt start/stop bit. The timer is reset and can be restarted in the normal way, giving a full time delay period before the next interrupt.

In general, the control register is set up such that writing 0s into it will start anything that is stopped, pull the clock out of test mode and select the clock setting register onto the bus. In other words, writing 0 will maintain normal clock operation and restart interrupt timing, etc.

The read only portion of the control register has two status outputs.

Since the 58274 keeps real time, the time data changes asynchronously with the processor and this may occur while the processor is reading time data out of the clock.

Some method of warning the processor when the time data has changed must thus be included. This is provided for by the data-changed flag located in bit 3 of the control register. This flag is set by the clock setting pulse which also clocks the time registers. Testing this bit can tell the processor whether or not the time has changed. The flag is cleared by a read of the control register but not by any write operations. No other register read has any effect on the state of the data-changed flag.

Data bit 0 is the interrupt flag. This flag is set whenever the interrupt timer times out, pulling the interrupt output low. In a polled interrupt routine the processor can test this flag to determine if the 58274 was the interrupting device. This interrupt flag and the interrupt output are both cleared by a read of the control register.

Table 3 **The control register layout**

Access (addr0)	DB3	DB2	DB1	DB0
Read from:	Data-changed flag	0	0	Interrupt flag
Write to:	Test 0 = Normal 1 = Test Mode	Clock Start/Stop 0 = Clock Run 1 = Clock Stop	Interrupt Select 0 = Clock Setting Register 1 = Interrupt Register	Interrupt Start/Stop 0 = Interrupt Run 1 = Interrupt Stop

Both of the flags and the interrupt output are reset by the trailing edge of the read strobe. The flag information is held latched during a control register read, guaranteeing that stable status information will always be read out by the processor.

Interrupt timeout is detected and stored internally if it occurs during a read of the control register, the interrupt output will then go low only after the read has been completed.

A clock setting pulse occurring during a control register read will *not* affect the data-changed flag since time data read out before or after the control read will not be affected by the time change.

Methods of device operation

Test mode

The test mode is used for functionally testing the 58274 after fabrication and again after packaging. Test mode can also be used to set up the oscillator frequency when the part is first commissioned.

Figure 4 shows the internal clock connections when the device is written into test mode. The 32.768 kHz oscillator is gated onto the interrupt output to provide a buffered output for initial frequency setting. This signal is driven from a TRI-STATE® output buffer, enabling easy oscillator setting in systems where interrupt is not normally used and there is no external resistor on the pin.

If an interrupt is programmed, the 32.768 kHz output is switched off to allow high speed testing of the interrupt timer. The interrupt output will then function as normal.

The clock start/stop bit can be used to control the fast clocking of the time registers as shown in Figure 3.

Initialisation

When it is first installed and power is applied, the

device will need to be properly initialised. The following operation steps are recommended when the device is set up (all numbers are decimal).

1) Disable interrupt on the processor to allow oscillator setting. Write 15 into the control register. The clock and interrupt start/stop bits are set to 1, ensuring that the clock and interrupt timers are both halted. Test mode and the interrupt register are selected.

2) Write 0 to the interrupt register: ensure that there are no interrupts programmed and that the oscillator will be gated onto the interrupt output.

3) Set oscillator frequency: all timing has been halted and the oscillator is buffered out onto the interrupt line.

4) Write 5 to the control register: the clock is not out of test mode but is still halted. The clock setting register is now selected by the interrupt select bit.

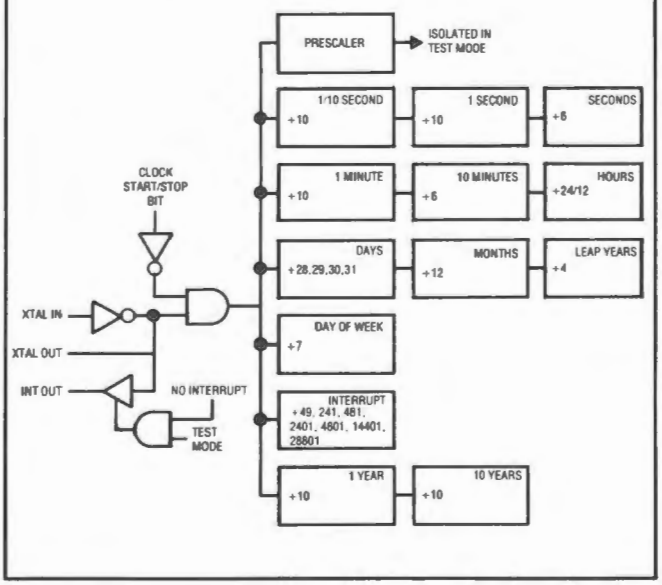
5) Set 12/24 Hours Mode: write to the clock setting register to select the hours counting mode required.

6) Load Real-Time Registers: all time registers (including Leap Years and AM/PM bit) may now be loaded in any order. Note that when writing to the clock setting register to set up Leap Years and AM/PM, the Hours Mode bit must not be altered from the value programmed in step 5.

7) Write 0 to the control register: this operation finishes the clock initialisation by starting the time. The final control register write should be synchronised with an external time source.

In general, timekeeping should be halted before the time data is altered in the clock. The data can, however, be altered at any time if so desired. Such may be the case if the user wishes to keep the clock corrected without having to stop and restart it; ie., winter/summer time changing can be accomplished without halting the clock. This can be done in software by sensing the state of the data-changed flag and only altering time data just after the time has rolled over (data-changed flag set).

Figure 3 **Test mode operation**



Reading the time registers

Using the data-changed flag technique supports microprocessors with block move facilities, as all the necessary time data may be read sequentially and then tested for validity as shown below.

1) Read the control register, address 0: this is a dummy read to reset the data-changed flag (DCF) prior to reading the time registers.

2) Read time registers: all desired time registers are read out in a block.

3) Read the control register and test DCF: if DCF is cleared (logic 0), then no clock setting pulses have occurred since step 1. All time data is guaranteed good and time reading is complete.

If DCF is set (logic 1), then a time change has occurred since step 1 and time data may be consistent. Repeat steps 2 and 3 until DCF is clear. The control read of step 3 will have reset DCF, automatically repeating the step 1 action.

Interrupt programming

The interrupt timer generates interrupts at time intervals which are programmed into the interrupt register. A single interrupt after delay or repeated interrupts may be programmed. Table 2B lists the different time delays and the data words that select them in the interrupt register.

Once the interrupt register has been used to set up the delay time and to select for single or repeat, it takes no further part in the workings of the interrupt system. All activity by the processor then takes place in the control register.

Initialising:

1) Write 3 to the control register (AD0): clock timing continues, interrupt register selected and interrupt timing stopped.

2) Write interrupt control word to address 15: the interrupt register is loaded with the correct word (chosen from Table 2B) for the time delay required and for single or repeated interrupts.

3) Write 0 or 2 to the control register: interrupt timing commences. Writing 0 selects the clock setting register onto the data bus; writing 2 leaves the interrupt register selected. Normal timekeeping remains unaffected.

On interrupt.

Read the control register and test for interrupt Flag (bit 0).

If the flag is cleared (logic 0), then the device is not the source of the interrupt.

If the flag is set (logic 1), then the clock did generate an interrupt. The flag is reset and the interrupt output is cleared by the control register read that was used to test for interrupt.

Single interrupt mode.

When appropriate, write 0 or 2 to the control register to restart the interrupt timer.

Repeated interrupt mode.

Timing continues, synchronised with the control register write which originally started interrupt timing. No further intervention is necessary from the processor to maintain timing.

In either mode interrupt timing can be stopped by writing 1 into the control register (interrupt start/stop set to 1). Timing for the full delay period recommences when the interrupt start/stop bit is again loaded with 0 as normal.

Important note. Using the interrupt timer places a constraint on the maximum Read Strobe width which may be applied to the clock. Normally all registers may be read from with a t_{RW} down to DC (ie., $\overline{CS}$ and $\overline{RD}$ held continuously low). When the

interrupt timer is active however, the maximum read strobe width that can be applied to the control register (Addr 0) is 30ms.

This restriction is to allow the interrupt timer to properly reset when it times out. Note that it only affects reading of the control register – all other addresses in the clock may be accessed with DC read strobes, regardless of the state of the interrupt timer. Writes to any address are unaffected.

Notes on AC timing requirements

Although Figures 4 and 5 show MICROBUS control signals used for clock access, this does not preclude the use of the 58274 in other non-MICROBUS systems. Figure 6 is a simplified logic diagram showing how the control signals are gated internally to control access to the clock registers. From this diagram it is clear that $\overline{CS}$ could be used to generate the internal data transfer strobes, with $\overline{RD}$ and $\overline{WR}$ inputs set up first. This situation is illustrated in Figure 7.

The internal data busses of the 58274 are fully CMOS, contributing to the flexibility of the control inputs. When determining the suitability of any given control signal pattern for the 58274, the timing specifications in Tables 4 and 5 should be examined. As long as these timings are met (or exceeded) the 58274 will function correctly.

When the 58274 is connected to the system via a peripheral port, the freedom from timing constraints allows for very simple control signal generation, as in Figure 8. For reading (Figure 8a), Address, $\overline{CS}$ and $\overline{RD}$ may be activated simultaneously and the data will be available at the port after t_{AD}-max (700ns). For writing (Figure 8b), the Address and data may be applied simultaneously and $\overline{CS}$ and $\overline{WR}$ strobed together.

Table 4 **Read timing: data from peripheral to microprocessor**
$V_{DD} = 5V \pm 0.5V$, $C_L = 100pF$

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AD}	Address Bus Valid to Data Valid		550	700	ns
t_{CSD}	Chip Select On to Data Valid		250	375	ns
t_{RD}	Read Strobe On to Data Valid		250	375	ns
t_{RW}	Read Strobe Width (Note 1)			DC	
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	0			ns
t_{CSH}	Chip Select Hold Time from Trailing Edge of Read Strobe	0			ns
t_{RH}	Data Hold Time from Training Edge of Read Strobe	50	80	150	ns
t_{HZ}	Time from Trailing Edge of Read Strobe until O/P Drivers are TRI-STATE	50	80	200	ns

Table 5 **Write timing: data from microprocessor to peripheral $V_{DD} = 5V \pm 0.5V$**

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AW}	Address Bus Valid to Write Strobe ↓ (note 2)	650			ns
t_{CSW}	Chip Select On to Write Strobe ↓	350			ns
t_{DW}	Data Bus Valid to Write Strobe ↓	350			ns
t_{WW}	Write Strobe Width	350			ns
t_{WCS}	Chip Select Hold Time Following Write Strobe ↓	0			ns
t_{WA}	Address Bus Hold Time Following Write Strobe ↓	50			ns
t_{WD}	Data Bus Hold Time Following Write Strobe ↓	50			ns

Note 1: Except for special case restriction: with interrupts programmed, max read strobe width of control register (ADDR 0) is 30ms. See section on Interrupt programming.

Note 2: All timings measured to the trailing edge of write strobe (data latched by the trailing edge of $\overline{WR}$).

Figure 4 **Read timing cycle**

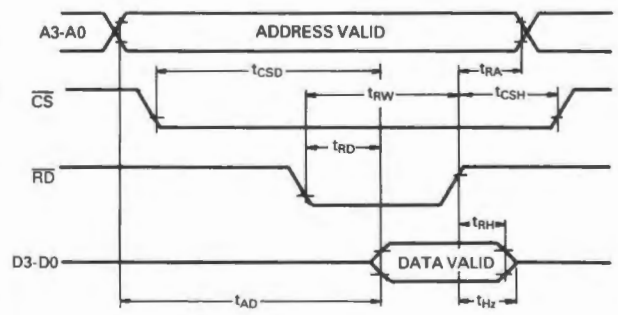


Figure 5 **Write timing cycle**

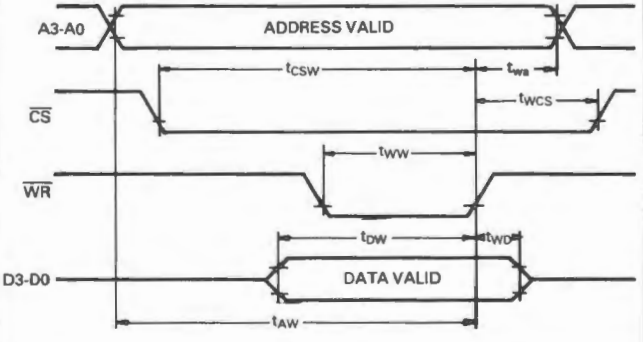


Figure 6 **58274 Microprocessor interface diagram**

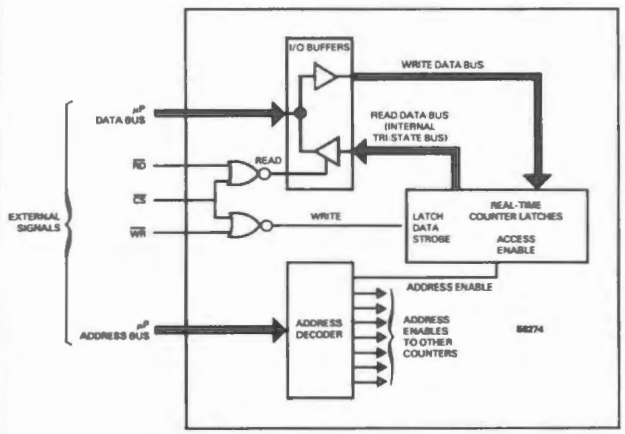


Figure 7 **Valid 58274 control signals using chip select generated access strobes**

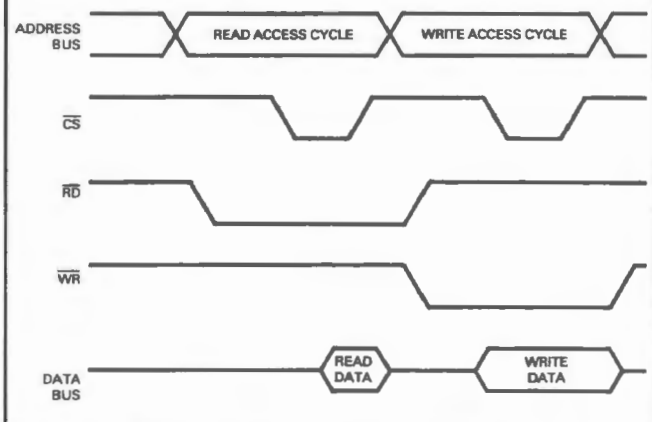
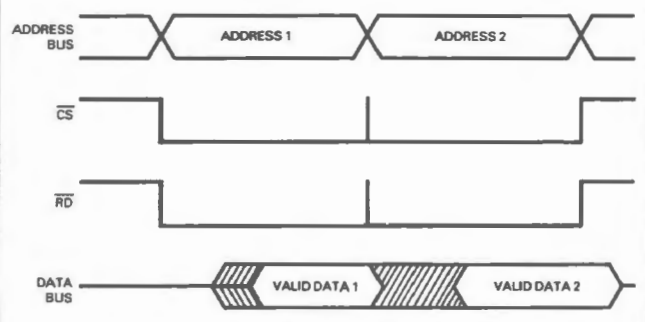
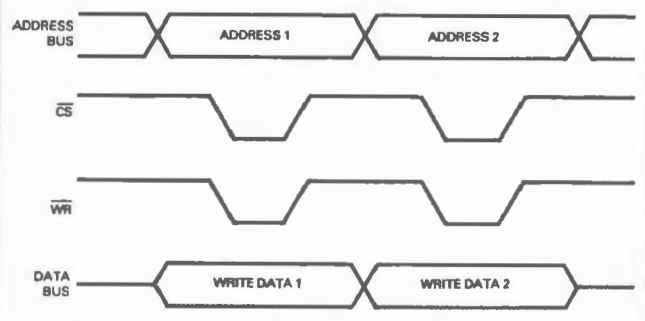


Figure 8 **Simple port generated control signals**



a. Port generated read access – 2 addresses read out



b. Port generated write access – 2 addresses written to

Application notes

Time reading using interrupt

In systems such as point of sale terminals and data loggers, time reading is usually only required on a random demand basis. Using the data-changed flag as outlined in the section on methods of operation is ideal for this type of system. Some systems, however, need to sense a change in real time; eg., industrial timers/process controllers. TV/VCR clocks, any system where real time is displayed.

The interrupt timer on the 58274 can generate interrupts synchronously with the time registers changing, using software to provide the initial synchronisation.

In single interrupt mode the processor is responsible for initiating each timing cycle and the timed period is accurate to ±1ms.

In repeated interrupt mode the period from the initial processor start to the first timeout is also only accurate to ±1ms. The following interrupts maintain accurate delay periods relative to the first timeout. Thus, to utilise interrupt to control time reading, we will use repeated interrupt mode.

In repeated mode the time period between interrupts is exact, which means that timeouts will always occur at the same point relative to the internal clock setting pulses. The case for 0.1s interrupts is shown in Figure 9a. The same is true for other delay periods, only there will be more clock setting pulses between each interrupt timeout. If we set up the interrupt timer so that interrupt always times out just after the clock setting pulse occurs (Figure 9b), then there is no need to test the data-changed flag as we know that the time data has just changed and will not alter again for another 100ms.

This can be achieved as outlined below.

1) Follow steps 1 and 2 of the section on interrupt programming. In step 2 set up for repeated interrupt.

2) Read control register AD0: This is a dummy read to reset the data-changed flag.

3) Read control register AD0 until data-changed flag is set.

4) Write 0 or 2 to control register. Interrupt timing commences.

Time reading with very slow read cycles

If a system takes longer than 100ms to complete reading of all the necessary time registers (eg., when CMOS processors are used or where high level interpreted language routines are used, then the data-changed flag will always be set when tested and is of no value. In this case, the time registers themselves must be tested to ensure data accuracy.

The technique below will detect both time changing between read strobes (ie., between reading tens of minutes and units of hours) and also time changing during read, which can produce invalid data.

1) Read and store the value of the lowest order time register required.

2) Read out all the time registers required. The registers may be read out in any order, simplifying software requirements.

3) Read the lowest order register and compare it

Figure 9a **Time delay from clock setting pulses to interrupt is constant**

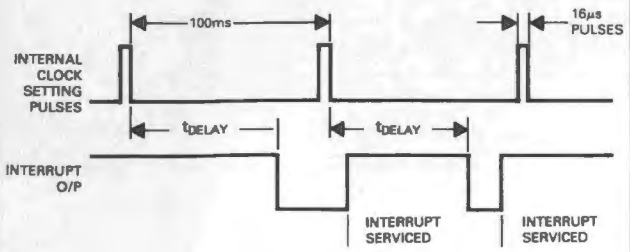
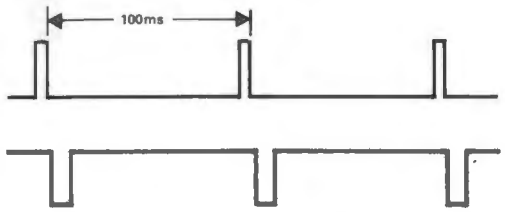


Figure 9b **Interrupt timer synchronized with clock setting pulses**



with the value stored previously in step 1. If it is still the same, then all time data is good. If it is changed, then store the new value and go back to step 2.

In general, the rule is that the first and last reads must both be of the lowest order time register. These two values can then be compared to ensure that no change has occurred. This technique works because for any higher order time register to change, all the lower order registers must also change. If the lowest order register does not change, then no higher order register has changed either.

RS data

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RS data

Floppy disc drives and accessories (3½in)

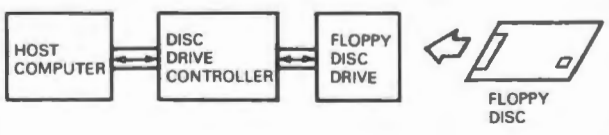
This data sheet covers the following stock numbers:

Stock No.	Description
630-566	3½in Floppy Disc Drive, single sided 40 tracks, 67.5 TPI, 250kB (MFM)
630-572	3½in Floppy Disc Drive, double sided 40 tracks per side, 67.5 TPI, 500kB (MFM)
630-588	3½in Floppy Disc Drive, single sided 80 tracks, 135 TPI, 500kB (MFM)
630-594	3½in Floppy Disc Drive, double sided 80 tracks per side, 135 TPI, 1MB (MFM)
630-639	3½in Floppy Disc Drive Alignment Disc
501-963	3½in Disc Drive Case
592-010	3½in Disc Drive Power Supply

Floppy disc drives

Floppy disc drives (FDDs) are precision magnetic recording instruments with a digital interface, making them particularly suitable for high capacity storage with fast access digital systems. Typical system connection is shown below:

Figure 1 **Typical system connection**

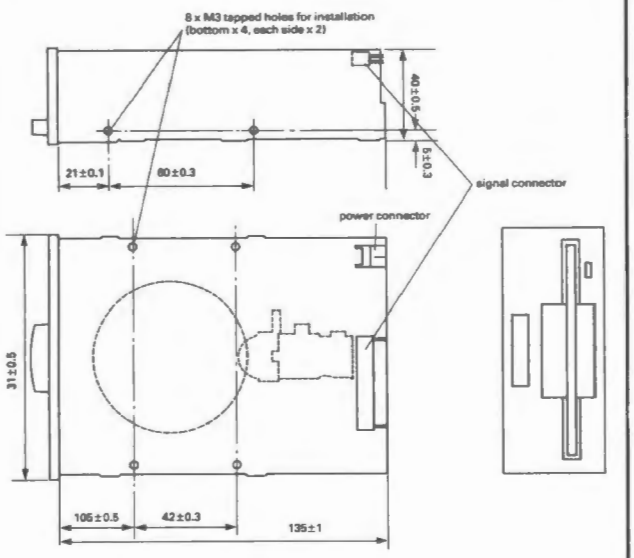


The host computer processes data which is accessed via the disc drive controller. The controller organises the packaging, formatting and timing of the floppy disc data. The floppy disc drive contains Read/Write and motion control electronics for storing, selecting and reading data from the disc.

Features

- Compact size (W x H x D): 102 x 40 x 135mm
- Long-life zinc-ferrite Read/Write head with tunnel erase, gimbal supported to ensure accurate tracking
- Compatible with the 5¼in industry standard S.400 (Shugart) controller to drive signal interface
- Uses highly reliable 34-way, pcb header for signal interface
- Can replace 5¼in disc drives by simple change of signal and power connector
- Uses 3½in media having a durable plastic shell ensuring easy portability and increased data security
- Head and drive electronics shielded to protect against stray magnetic fields and handling
- Brackets allow for horizontal or vertical mounting
- Use of custom LSI IC's for low power consumption and high reliability
- High speed data retrieval enabled by fast track to track access times (3ms for 135 TPI and 6ms for 67.5 TPI) – compatible with RS 5¼in disc drives
- Protection against spurious writes when power switched on and off
- High precision and reliability using solid state LED/photosensor for write protect and track 00 sensing; Hall ic for index sensing; and reed-relay for disc insertion sensing
- Up to four drives may be daisy chained
- Can be used with RS floppy disc drive controller board (stock number 300-164) or the RS 2797 floppy disc drive controller ic. (stock number 301-117)
- Power supply and case available

Figure 2 **Physical details**



Specification

Recording method:
FM (single density), MFM (double density)

MTBF: more than 10,000 power on hours.

Error rates:

Soft errors:	1 per 10^9 bits
Hard errors:	1 per 10^{12} bits
Seek errors:	1 per 10^6 seeks

Environmental conditions

Temperature, operating	: +4°C to +50°C
transportation	: –40°C to +70°C
storage	: –22°C to +60°C
Temperature gradient	: <15°C per hour during operation
Relative humidity	: 20% to 80% during operation
Wet bulb temperature	: 29°C max
Vibration, operating	: <0.5G (to 100Hz) <0.25G (100 to 500Hz)
transportation	: <2G (to 100Hz)
Shock, operating	: <5G (10msec max.)
transportation	: <50G (10msec max.)
Altitude, operating	: <12,000m

Power requirements

dc + 12V:	±10% voltage tolerance <200mV p-p allowable ripple 110mA (typ.), 210mA (max.) at read/write 225mA (typ.), 290mA (max.) at seek 330mA (max.) peak for spindle motor start 40mA (typ.), 60mA (max.) waiting
dc + 5V:	±5% voltage tolerance <100mV p-p allowable 200mA (typ.), 260mA (max.) at read/write 160mA (typ.), 210mA (max.) at seek 180mA (typ.), 240mA (max.) waiting
Consumption:	2.32W (typ.), 3.82W (max.) at read/write 3.50W (typ.), 4.53W (max.) at seek 1.38W (typ.), 1.92W (max.) waiting
Power voltage rise time:	1 to 100ms (0 to 90%)
Power reset time:	<500msec after power on. During this reset time correct control command response may not be obtained.

Power on/off protection:

a) If +5V power is less than +3.4V writing and erasing is prevented irrespective of input signal states.

b) No writing or erasing allowed unless WRITE GATE signal is TRUE irrespective of other signals (subject to condition a).

c) Drive can always be recovered by a control command from host system eliminating 'hung-up' conditions.

Operational characteristics

Spindle motor:	Direct dc brushless motor 300 rpm disc speed <±1.5% long term speed variation <±2% instantaneous speed variation Frequency servo control by ac tachometer <400msec start time 100msec average latency
Index:	1 pulse per disc revolution Detection by Hall ic. Detection cycle 200msec ±1.5% <±400μs timing error with test disc.

Track construction:
375μm nom, track pitch (67.5 TPI, 40 tracks)
187.5μm nom. track pitch (135 TPI, 80 tracks)
<±25μm position error (67.5 TPI drive)
<±15μm position error (135 TPI drive)

Magnetic head:
Gimbal supported zinc ferrite read/write head with tunnel erase.
Track width after tunnel erase: 0.115 ±0.01mm
Read/write-erase gap spacing: 0.7 ± 0.05mm
Read/write gap azimuth error: 0° ± 30' (test disc)

Track seek mechanism:
Four phase stepping motor with steel belt
One step per track
Track 00 detection by LED and phototransistor
Track to track access time : 3ms (135 TPI)
6ms (67.5 TPI)
Settling time: 15ms (max.) excluding track to track access time
Average track access time: 94msec including settling time.

Head load mechanism:
Nil. The head is loaded whenever disc is installed.

File protect mechanism:
Detection of transparent write enable hole by LED and phototransistor.

Window margin:
>600nsec, with test disc, MFM method, analogue PLO separator and zero write precompensation.

Signal interface

The RS 3½in disc drives conform to the industry standard S.400 controller/drive signal interface, where normal TTL logic levels apply, TRUE being active low. However, note that a pcb header is used instead of the card-edge connector of 5¼in disc drives.

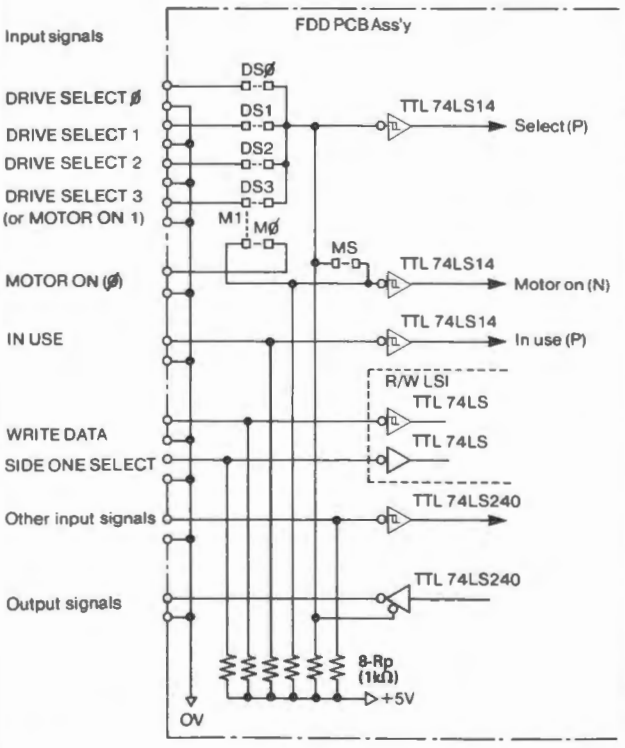
Input signals

Receiver: 74LS series or equivalent
Low level (TRUE): 0V to 0.5V
High level (FALSE): 2.5V to 5.25V
Low level input current (incl. pull-up resistor)
DRIVE SELECT signal line: –12mA (max.)
Other input signal lines: –6mA (max.)
High level input current: 50μA (max.)

Output signals

Driver: 74LS 240 (3-state) or equivalent
Low level (TRUE): 0V to 0.4V
High level (FALSE): 5.25V (max.) (depending on host side terminator)
Low level sink current capability: 12mA (max.) (24mA (max) for 0.5V low level)
High impedance state (drive not selected): leakage current ± 20μA (max.)
Input pull-up resistor (not removable) 1kΩ ±5% provided on all input signals
Signal cable: max. length 1.5m (total cable length for multiple drive configurations).

Figure 3 **FDD signal interface circuit**



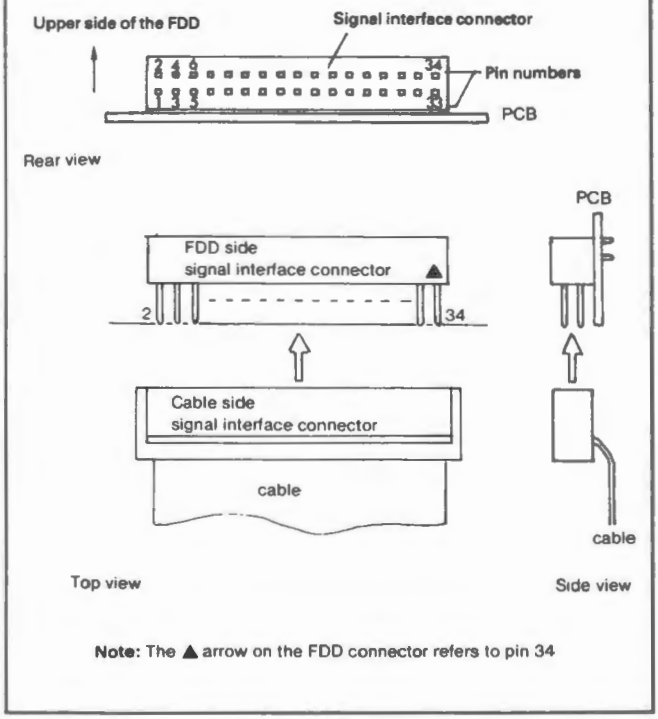
Note: SIDE ONE SELECT signal is used only for double sided FDD.

Figure 4 **Signal interface connections**

Signals	Directions	Terminal Nos.	
		Signals	0V
Reserved		2	1
In Use (or Motor On 2)	Input	4	3
Drive Select 3 (or Motor On 1)	Input	6	5
Index	Output	8	7
Drive Select Ø	Input	10	9
Drive Select 1	Input	12	11
Drive Select 2	Input	14	13
Motor On (Ø)	Input	16	15
Direction Select	Input	18	17
Step	Input	20	19
Write Data	Input	22	21
Write Gate	Input	24	23
Track 00	Output	26	25
Write Protect	Output	28	27
Read Data	Output	30	29
Side One Select	Input	32	31
Ready	Output	34	33

Note: SIDE ONE SELECT signal is used only for double sided FDD.

Figure 5 **Signal interface connector**



Note: The ▲ arrow on the FDD connector refers to pin 34

The FDD signal connector is a 34 way, 0.1in pitch pcb mounting, right angle header. For suitable cable connector refer to current RS catalogue: 34 way IDC cable mounting socket, stock number 471-238. Note that this connector is not polarised for use with the disc drive.

Power interface

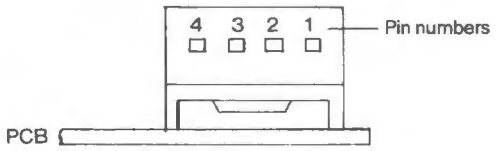
Any appropriate cable capable of taking the maximum drive power consumption will be acceptable. The cable should be kept as short as possible to avoid noise generation.

The drive is supplied with a suitable power cable connector and four appropriate crimp terminals. If these need to be replaced refer to connectors section of current RS catalogue:

i) Stock no. 467-611 4 way cable shell
ii) Stock no. 467-598 crimp terminals
iii) Stock no. 533-241 crimp tool.

Note: If the above RS cable shell is to be used the plastic shroud on the disc drive power connector needs to be removed first.

Figure 6 **Drive power connections**



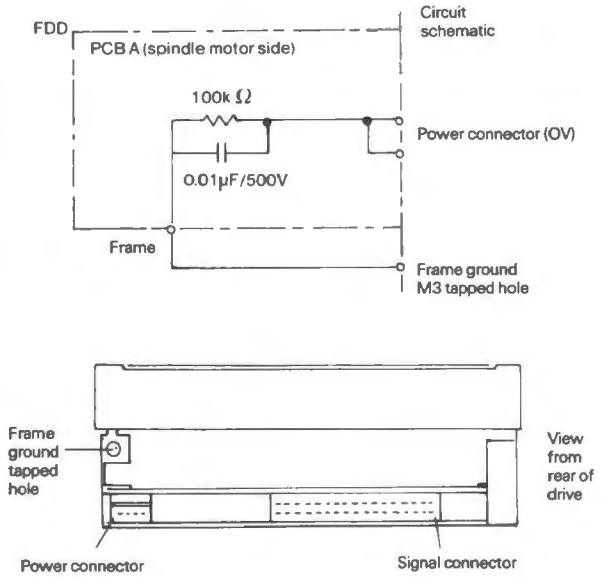
(Viewed from rear of drive)

Power voltage	Pin numbers
dc +5V	1
0V	2
0V	3
dc +12V	4

Frame grounding

An M3 tapped hole is provided at the rear of the disc drive for frame grounding.

Figure 7 **Frame grounding**



Read compatibility between drives

This depends on optimum head radial alignment to the Disc Centre Datum Point. To achieve this an Alignment Disc is required. For further information consult the Alignment Disc section of this data sheet.

Input/Output signals

Input signals are those received by the FDD (Floppy Disc Drive) while output signals are those transmitted from the FDD. True is active low.

Drive select Ø-3 input signals

The DRIVE SELECT lines provide a means of selecting and deselecting the drives. Four separate DRIVE SELECT lines are provided so that up to four drives may be connected to a single controller. By placing only one of these jumpers in each drive, only one drive will be selected when activating any one of the DRIVE SELECT lines.

When the signal level is true (low), the disc drive electronics are activated, and the drive is conditioned to respond to step or read/write commands. When the signal level is false (high), the input control lines (except MOTOR ON and IN USE) and output status lines are disabled.

A delay time of 0.5μsec max. (including delay time through the interface cable) must be allowed before other input/output signals are effective.

Motor on input signal

The spindle motor reaches the rated rotational speed within 400msec after this signal becomes true.

Direction select input signal

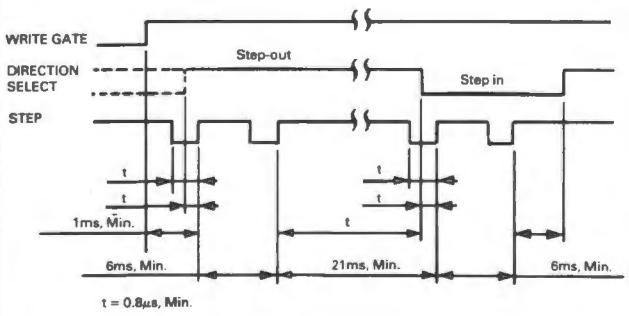
The direction of motion of the read/write head is defined by the state of this input line. A true (low) level defines direction as 'IN' (towards centre of the disc); a false (high) level defines the direction as 'OUT'.

Step input signal

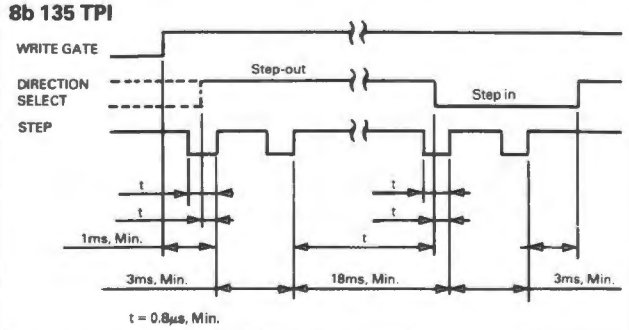
A single pulse on this input will move the Read/Write head one track in or out, dependent on the

Figure 8 **Step timing**

8a 67.5 TPI



8b 135 TPI



state of the DIRECTION SELECT line. The motion of the head is initiated on the trailing edge of STEP pulse. A minimum of a 0.8μs pulse width at a maximum frequency of 333Hz for 135 TPI (3ms track to track); 167Hz for 67.5 TPI (6ms track to track) should be maintained to ensure step integrity.

Write gate input signal

When true, this input line permits writing of data. When inactive, it permits transmission of data to the controller. This signal is ineffective when the write protect signal is true. This signal should be made true only after satisfying all of the following four conditions.

i) FDD is in ready state.
ii) More than 18msec after receiving final STEP pulse (135 TPI) or 21ms for 67.5 TPI drives.
iii) More than 100μsec after a level change of the SIDE ONE SELECT signal.

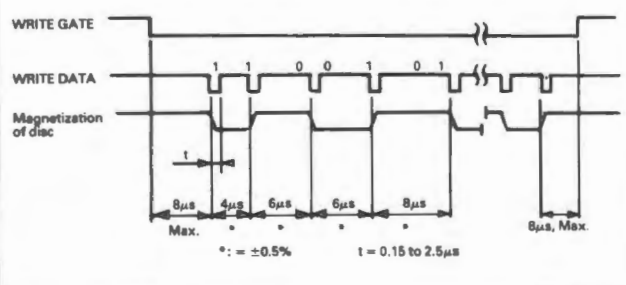
Allow a minimum of 1.2ms after dropping WRITE GATE before:

i) Stopping spindle motor.
ii) Making drive select signal false.
iii) Moving head with STEP pulse.
iv) Changing sides with SIDE ONE SELECT input signal.

Write data input signal

The frequency of the WRITE DATA is dependent upon the encoding scheme used, the density option exercised, and the data pattern to be written. The write oscillator frequency stability should be held to 0.5%. The data pulse width should be a minimum of 0.15μs and a maximum of 2.5μs wide. WRITE DATA is effective when WRITE GATE is true and WRITE PROTECT is false. It is recommended that the leading edge of the first WRITE DATA pulse occurs no sooner than 4μs and no later than 8μs after the leading edge of the WRITE GATE true signal. The WRITE GATE false signal should occur no sooner than 4μs and no later than 8μs after the last data pulse.

Figure 9 **Write data timing (MFM method)**



Side one select input signal

This input is used to select either the upper or lower head. The signal is false (high) to select side 0 and true (low) for side 1. A 100μsec delay should be allowed after a head select event occurs. Only then will valid data be present. When the other side of the disc is selected after the completion of a write operation, a 1.2ms delay should be allowed after making the WRITE GATE signal false.

In use input signal

When IN USE function is selected:

Signal to indicate that all of the daisy chained FDDs are in use under the control of the host system. The front bezel indicator is illuminated when this signal is true.

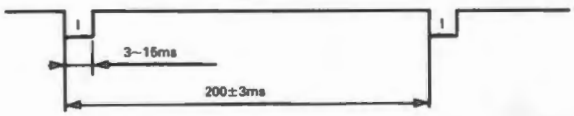
Track 00 output signal

This output, when true, indicates that the read/write head(s) are located over TRACK 00. Allow 2.8msec after the STEP pulse for this signal to become valid (135 TPI) or 5.8msec (67.5 TPI).

Index output signal

An INDEX pulse is transmitted to the controller once every revolution indicating the beginning of a track.

Figure 10 **Index timing**



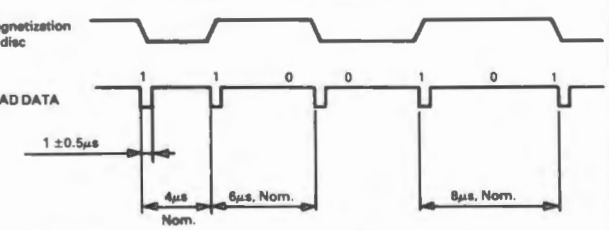
Read data output signal

This output represents data consisting of encoded clock and data bits. The pulse width of both clock and data bits will be 1μsec ±0.5μsec. The leading edge of each READ DATA pulse represents the true position of the flux transition on the recording media.

This signal becomes valid when all the following five conditions are satisfied:

i) The FDD is in a ready state (refer to READY output signal).
ii) More than 35msec after head loading has started.
iii) More than 18msec (135 TPI) and 21msec (67.5 TPI) after final STEP pulse receipt.
iv) More than 1.2msec after WRITE GATE signal becomes false.
v) More than 100μsec after a level change of the SIDE ONE SELECT signal for double sided drives.

Figure 11 **Read data timing (MFM method)**



Note: The displacement of any bit position does not exceed ±20% from its nominal position.

Write protect output signal

This signal indicates the write enable notch of the floppy disc is masked.

When this signal is true, the data on the disc is protected from erasure and the writing of new data is inhibited.

Ready output signal

This signal indicates that the FDD is in a ready state.

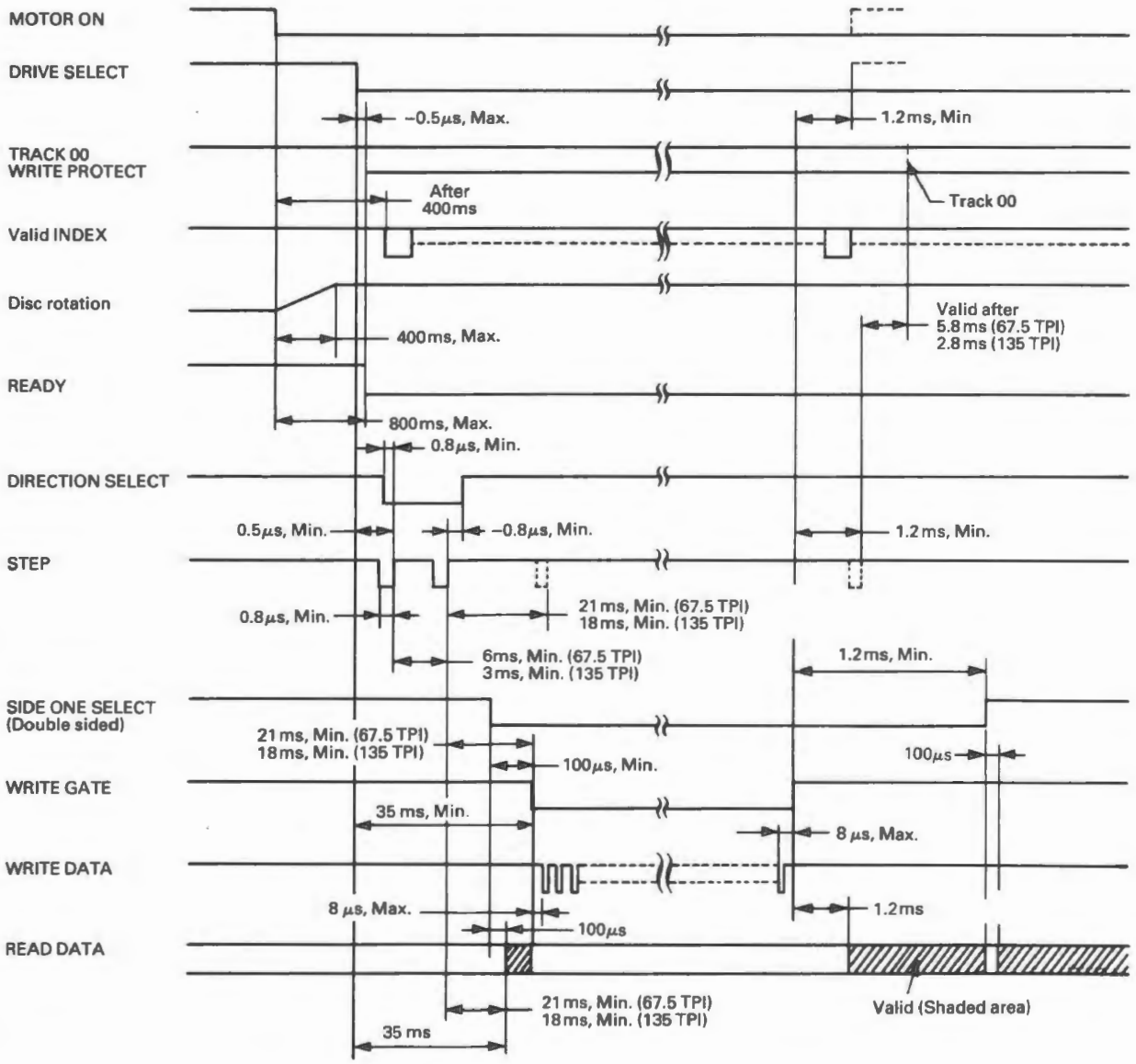
For soft sectored discs, the READY output signal is true when all of the following five conditions are satisfied:

i) The FDD is powered on.
ii) The floppy disc is inserted.
iii) The disc rotates at more than 50% of the rated speed.
iv) Two INDEX pulses have been counted after item iii) is satisfied.
v) Allow >800msec after the spindle motor has started.

Note: Pre-ready is the state where at least one INDEX pulse has been detected after item iii) is satisfied.

If the MOTOR ON input is made false then this signal goes false immediately.

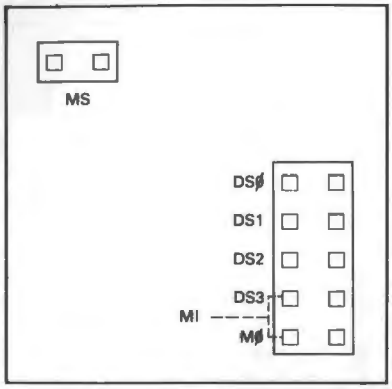
Figure 12 **Composite control timing**



Selection links

All the selection links are mounted on the main pcb of the disc drive. Insertion of the appropriate link is defined as the ON-state of the link function.

Figure 13 **Selection link assignment**



The disc drive is despatched with the DSØ and MØ selection links set to the on-state.

DSØ to DS3 selection links

These links designate the address of the disc drive in a multiplex daisy chain connection. Four addresses (Ø to 3) can be designated using the Drive Select Signals (Ø to 3) on the interface. No more than 2 drives should be assigned to the same address.

MØ, MI, MS selection links (see also Table 3)

These links designate the conditions under which the spindle motor will rotate.

The MØ and M1 links select the interface line (interface pin) of the MOTOR ON signal (see Figure 3). With the MØ link set to on, the MOTOR ON (Ø) signal (pin no. 16) has the same function as that for the conventional standard 5.25in disc drive. With the M1 link set on and with the two drives in a daisy chain configuration, the DRIVE SELECT 3 signal (pin no. 6) is used as the MOTOR ON (1) signal. The second option (M1 link set to on) is useful if your application requires the spindle motor rotation to be independent of the DRIVE SELECT signal.

The MS link is set to on to rotate the spindle motor by the DRIVE SELECT Ø to 3 signals (see Figure 3). In this case the MØ and M1 links are usually set to the off-state. However, if the MØ link is set to the on-state the spindle motor will rotate by the ORed (Logical OR) result of the DRIVE SELECT signal and the MOTOR ON (Ø) signal.

Setting up drive for operation

Front bezel indicator

This turns on either a) while the DRIVE SELECT signal selected by the DSØ to DS3 links is TRUE, or b) while the IN USE signal is TRUE.

Spindle motor

Five options are offered:

Figure 14 **Spindle motor rotating conditions**

Selection	Links			Signals (when TRUE) causing rotation
	MØ	M1	MS	
1	ON	–	–	MOTOR ON Ø
2	–	ON	–	MOTOR ON 1 (DRIVE SELECT 3)
3	–	–	ON	DRIVE SELECT Ø to 3
4	ON	–	ON	MOTOR ON Ø + DRIVE SELECT Ø to 3
5	–	ON	ON	MOTOR ON 1 + DRIVE SELECT Ø to 2

Note: '–' indicates the off-state of the link
'+' indicates logical OR

3½in alignment disc (630-639)

The RS 3½in alignment disc can be used for 67.5/135 TPI 3½in drives, with either single or double sided heads. It is physically compatible with industry standard 3½in floppy discs.

The following signals are available:

Track number		Signal	Check/Adjustment
67.5 TPI	135 TPI		
20	40	Index Burst	Sensor Timing
20	40	Alignment Burst	Track Alignment

For detailed instructions consult alignment disc instruction leaflet for the following:

1. Check and adjustment of Track Radial Alignment.
2. Check and adjustment of Index Data Burst Timing.
3. Check and adjustment of Track 00 Sensor.
4. Check and adjustment of Track 00 Stopper.

RS data

3½in Disc drive case 501-963

The RS disc drive case has been designed to house up to two 3½in disc drive units.

There is sufficient space within the case to accommodate one or two disc drives (a blanking plate is supplied for use when only one disc drive is fitted). A suitable power supply for the drives may be fitted inside the rear of the case, alternatively, the rear panel of the case may be replaced with the RS disc drive power supply for direct mains operation.

Case dimensions: L. 295, W. 123, H. 110.

Disc drive power supply

This power supply (see Power Supplies section of current RS catalogue) is designed to simultaneously power two standard 3½in disc drives and incorporates two output connectors, each carrying 12V and 5V supplies. The unit has been designed to fit into the rear of the disc drive case (see above). Complete with fitting instructions.

Input:	240V ac ±6% 50Hz
Outputs:	Two identical outputs of: +12V dc ±5%, 0.26A peak +5V dc ± 5%, 0.33A peak
Fuse:	2A HRC (20mm)
Dimensions:	W.118, H.105, D.114.

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company
Telephone: 0536 201234
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RS data

Relative humidity meter

Stock number 611-385

The RS relative humidity meter is a handheld, battery powered instrument, capable of measuring the relative humidity of gases from 5%r.h. to 100%r.h. and the temperature of the gas from −10°C to +50°C, and displaying the result via a 3 digit liquid crystal display.

The humidity meter is supplied in an attache case with moulded foam interior, complete with calibration chamber, calibration capsules and comprehensive instruction booklet.

Features

- Measures from 5% to 100%r.h.
- Measures from −10°C to +50°C
- Battery condition indicator
- User-calibratable

Technical specification

Measuring range – relative humidity	5 to 100%r.h.
– temperature	−10 to +50°C
Accuracy (at 25°C) – relative humidity	±2%r.h.
– temperature	±0.3°C
Display resolution – relative humidity	0.1%r.h.
– temperature	0.1°C
Hysteresis (10-95-10%r.h.)	<2%r.h.
Response time (at 25°C)	<10s
Temperature coefficient	±0.05%r.h./°C

Warning

The sensor, although robust, will be damaged if exposed to concentrations of pollutants greater than that noted below:

Substance	Max. concentration allowable for continuous operation with error of ±2.5%r.h.		1980 Threshold limit value (Health & Safety Executive)	
	p.p.m.	g/m³	p.p.m.	g/m³
Ethyl alcohol	3500	6	1000	1.9
Isopropyl alcohol	4800	12	400	0.98
Toluene	1300	5	100	0.38
Xylene	1300	5	100	0.38
Pure benzine	33000	100	10	0.03
Petrol		100		
Ethylene glycol	1200	3	100	0.26
Acetone	3300	8	1000	2.4
Ethylmethyl ketone	3300	8		
Ethyl acetate	4000	15	400	1.4
Acetic acid	800	2	10	0.025
Ammonia	5500	4	25	0.018
Hydrogen chlorine	300	0.5	5	0.007
Hydrogen sulphide	350	0.5	10	0.015
Sulphur dioxide	5	0.013	2	0.005

The threshold limit value is the maximum concentration of harmful substances allowable at a work place, as defined by the Health & Safety Executive.

RS data

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RS data

Batteries

A comprehensive range of rechargeable cells and batteries is available in addition to alkaline primary cells (non rechargeable). Each chemical couple used is best suited to a particular application and the table overleaf details the performance of all battery types. In addition a short description is given on each type indicating their prime uses and charging methods.

The capacity of RS cells and batteries is stated in ampere hours (Ah) and is the product of discharge current and time. The discharge time is limited by the cell or battery reaching its endpoint voltage. The rated capacity is generally specified for discharge times of 5 (C_5), 10 (C_{10}) or 20 hours (C_{20}). Thus, for example, the rated capacity C_{20} is the value in ampere hours obtained with 20 hours uniform, uninterrupted discharge to the end point voltage. The rated current I_{20} in amperes is $\frac{1}{20}$ of the rated capacity in ampere hours.

Lead acid RS dryfit A200: suitable for regular cyclic use (ie. regular discharge/recharge cycles) and standby float applications; equipment requiring high discharge currents; unattended equipments requiring batteries with low self discharge currents; stationary or mobile installations.

Batteries available are 2V (9.5Ah), 6V (1.1Ah, 3.0Ah and 5.7Ah), 12V (1.8Ah, 3.0Ah, 5.7Ah, 9.5Ah, 20Ah, 63Ah and 110Ah).

Lead acid RS dryfit A300: suitable for standby/float applications in alarm control panels and other security related products; standby power for unattended equipments.

Batteries available are all 12V types in 1.1Ah, 1.8Ah, 3.0Ah and 5.7Ah capacities.

Lead acid RS cyclon: applications as dryfit, but where some battery abuse may be expected and where charging procedures are to be relaxed.

2V cells available are 2.5Ah, 5Ah and 25Ah.

Alkaline primary cells: these cells and batteries offer very long service life compared with Leclanché types in equipments having high current drains, e.g. tape recorders, electronic flash units, torches, calculators, etc. In addition these cells have very low self discharge currents and are completely sealed.

Available in sizes AAA,AA, C, D and PP3.

Ni-Cad sintered cells: applications where extreme ruggedness and/or high peak currents are required. In addition these cells offer very long service life and can be electrically misused without damage.

Available in sizes N, AAA, AA, C, D and PP9.

Ni-Cad high temperature sintered cells: primarily for use in emergency lighting installations these cells and batteries are particularly suitable for charging and discharging at elevated temperatures. Other applications include alarm control panels and emergency and standby areas where higher ambient temperatures are experienced.

Available as single D cells and 3 × D cell battery packs.

Note: sintered cells have fairly high self discharge currents and are therefore not suitable for equipments which have to be operational without recharging, after being left unattended for long periods of time.

Ni-Cad mass plate cells: applications where small size and ruggedness are required. These cells have low self discharge currents and are ideal in many small portable equipments.

A range of sizes including PP3.

Table 1: **Battery ratings and storage**

Battery type and Stock Nos.		Ratings: Voltage Fully charged	Ratings: Voltage Discharged	Ratings: Capacity	Storage: Shelf life (see note 1)	Storage: Storage life	Storage: Storage temp.
Lead Acid RS Dryfits A200				(20hr discharge rate)			
591-348	**2V, 9.5Ah**	2.10- 2.15V	1.75V	9.5Ah			
591-354	**6V, 1.1Ah**	6.30- 6.45V	5.25V	1.1Ah			
591-360	**6V, 3.0Ah**	6.30- 6.45V	5.25V	3.0Ah			
591-376	**6V, 5.7Ah**	6.30- 6.45V	5.25V	5.7Ah			fully charged
591-382	**12V, 1.8Ah**	12.60-12.90V	10.50V	1.8Ah		10 years	−50°C +70°C
591-770	**12V, 3.0Ah**	12.60-12.90V	10.50V	3.0Ah	16 months	to 80% stated	half charged
591-398	**12V, 5.7Ah**	12.60-12.90V	10.50V	5.7Ah	@ T_a = 20°C	capacity	−10°C +70°C
591-786	**12V, 9.5Ah**	12.60-12.90V	10.50V	9.5Ah		(see note 3)	discharged
591-613	**12V, 20Ah**	12.60-12.90V	10.50V	20Ah			−5°C +70°C
591-865	**12V, 63Ah**	12.60-12.90V	10.50V	63Ah			
591-871	**12V, 110Ah**	12.60-12.90V	10.50V	110Ah			
Lead Acid RS Dryfits A300				(10hr discharge rate)			
							fully charged
591-922	**12V, 1.1Ah**	12.60-12.90V	10.50V	1.1Ah		10 years	−50°C +70°C
591-966	**12V, 1.8Ah**	12.60-12.90V	10.50V	1.8Ah	16 months	to 80% stated	half charged
591-938	**12V, 3.0Ah**	12.60-12.90V	10.50V	3.0Ah	@T_a=20°C	capacity	−10°C +70°C
591-944	**12V, 5.7Ah**	12.60-12.90V	10.50V	5.7Ah		(see note 3)	discharged
							−5°C +70°C
Lead Acid RS Cyclons				(10hr discharge rate)			
591-461	**2V, 2.5Ah**			2.5Ah	150 days	10 years	
591-483	**2V, 5.0Ah**	2.15-2.18V	1.60V	5.0Ah	T_a=20°C	to 80% stated	−65°C +65°C
591-629	**2V, 25Ah**			25.0Ah		capacity	
						(see note 5)	
Alkaline Cells				(see note 4)			
591-657	AAA	1.50V	0.90V	0.7Ah			
591-225	AA	1.50V	0.90V	1Ah	24	24	
591-231	C	1.50V	0.90V	4Ah	months	months	−20°C +50°C
591-247	D	1.50V	0.90V	8Ah	@T_a=20°C	@T_a=20°C	
591-792	PP3	9.00V	5.40V	0.4Ah		(see note 2)	
Ni-Cad Sintered Cells				(5hr discharge rate)			
592-026	N	1.24-1.27V	1.00V	150mAh			
591-146	AAA	1.24-1.27V	1.00V	180mAh	120 days		
591-051	AA	1.24-1.27V	1.00V	500mAh	T_a=0°C		
591-045	C	1.24-1.27V	1.00V	2Ah	40 days	>5 years	−40°C +60°C
591-039	D	1.24-1.27V	1.00V	4Ah	T_a=20°C	(see note 2)	
591-095	PP9	8.68-8.90V	7.00V	1.2Ah	11 days		
					T_a=40°C		
Ni-Cad High Temp Cells				(5hr discharge rate)			
592-032	D	1.24-1.27V	1.00V	4Ah			−45°C +65°C
592-048	3 × D, Stick	3.72-3.81V	3.00V	4Ah	55 days	>5 years	possible
592-054	3 × D, Plate	3.72-3.81V	3.00V	4Ah	T_a=20°C	(see note 2)	0°C + 45°C
							recommended
Ni-Cad Mass Plate				(10hr discharge rate)			
591-477	PCB Battery	3.72-3.81V	3.00V	100mAh	26 months		
591-089	PP3	8.70-8.90V	7.00V	110mAh	T_a=0°C		Max limits
591-168	Button Cell	1.24-1.27V	1.00V	170mAh	10 months	>5 years	−40°C +50°C
591-174	Button Cell	1.24-1.27V	1.00V	280mAh	T_a=20°C	(see note 2)	0°C +45°C
591-180	Stack	8.70-8.90V	7.00V	170mAh	1 month		recommended
591-196	Stack	6.00-6.20V	5.00V	280mAh	T_a=40°C		

Notes:

1. Period after which capacity has fallen to 60% (Dryfits 50%) of its original fully charged level.
2. Period after which only 60% of the stated capacity is obtainable.
3. Recharge every 16 months.
4. Capacity depends very much upon load current. (Quoted when R_L = 40Ω for cells, R_L = 150Ω for PP3.)
5. Recharge every 3 years when stored at 25°C.

Table 2: **Battery charge information**

Battery type and stock numbers	Charge mode	Charge rate Continuous	Max	Charge ∅ (note 1)	Temp range	Stock numbers for suitable RS chargers
Lead Acid RS Dryfits A200			(see text)			
591-348 2V, 9.5Ah		2.30V	2.35V			591-578
591-354 6V, 1.1Ah		6.90V	7.05V			591-584
591-360 6V, 3.0Ah		6.90V	7.05V			591-584
591-376 6V, 5.7Ah	Parallel	6.90V	7.05V			591-584
591-382 12V, 1.8Ah	constant	13.80V	14.10V			591-590
591-770 12V, 3.0Ah	voltage	13.80V	14.10V	90%	−30°C +50°C	591-590 591-691 (5A) 591-411 (1A)
591-398 12V, 5.7Ah		13.80V	14.10V			591-590 591-691 (5A) 591-411 (1A)
591-786 12V, 9.5Ah		13.80V	14.10V			591-590 591-691 (5A) 591-893 (20A)
591-613 12V, 20Ah		13.80V	14.10V			591-590 591-691 (5A) 591-893 (20A)
591-865 12V, 63Ah		13.80V	14.10V			591-590 591-691 (5A) 591-893 (20A)
591-871 12V, 110Ah		13.80V	14.10V			591-590 591-691 (5A) 591-893 (20A)
Lead Acid RS Dryfits A300			(see text)			
591-922 12V, 1.1Ah		13.80V	14.10V			
591-966 12V, 1.8Ah	Parallel	13.80V	14.10V			591-590 (1A), 591-411 (1A)
591-938 12V, 3.0Ah	constant	13.80V	14.10V	90%	−30°C +50°C	591-691 (5A), 591-893 (20A)
591-944 12V, 5.7Ah	voltage	13.80V	14.10V			
Lead Acid RS Cyclons						
591-461 2V, 2.5Ah	Constant					591-685
591-483 2V, 5.0Ah	voltage	2.3-2.4V	2.55V			591-685
591-629 2V, 25Ah	(or constant current)	(see text)	(see text)	≥95%	−40°C +65°C	591-685
Alkaline Cells						
591-657 AAA						
591-225 AA						
591-231 C			Not rechargeable			
591-247 D						
591-792 PP3						
Ni-Cad Sintered Cells						
592-026 N		15mA	2C			
591-146 AAA		20mA	2C	60% @ C/8		A wide range of suitable RS chargers is available. Please refer to current RS catalogue.
591-051 AA	Series	66mA				
591-045 C	constant	250mA	10C	80% @ C/2	+10°C +45°C	
591-039 D	current	500mA				
591-095 PP9		100mA	2C	90% @ C		
Ni-Cad High Temp. Cells						
592-032 D	Series	500mA			(see Note 2)	591-067, 591-714
592-048 3 × D, Stick	constant	500mA	2C	84%	−20°C + 65°C (reduced spec)	591 – 067
592-054 3 × D, Plate	current	500mA			+10°C +35°C (full spec)	591 – 067
Ni-Cad Mass Plate						
591-477 PCB Battery		1.0mA				—
591-089 PP3	Series	1.1mA			Max limits	591-152
591-168 Button Cell	constant	1.7mA	C/10	72%	0°C +45°C	—
591-174 Button Cell	current	2.8mA			+10°C +35°C	—
591-180 Stack		1.7mA			recommended	—
591-196 Stack		2.8mA				—

Note:

1. ∅ = energy stored in the battery / energy supplied to the battery
2. At temperature below 0°C charge current is limited for 120mA and voltage to a maximum of 1.55V/cell.

Table 3: **Battery discharge information**

Battery type and stock numbers	Discharge temp	I max (see note 1)	Cyclic life	Standby life	R_{int} (DC)	R_{int} (AC) 50Hz
Lead Acid RS Dryfits A200					(see note 6)	(see note 6)
591-348 2V, 9.5Ah		80A			7.4mΩ	6mΩ
591-354 6V, 1.1Ah		40A			191mΩ	130mΩ
591-360 6V, 3.0Ah		60A			70mΩ	57mΩ
591-376 6V, 5.7Ah		80A			37mΩ	30mΩ
591-382 12V, 1.8Ah		40A	200-20,000		233mΩ	190mΩ
591-770 12V, 3.0Ah	−30°C +50°C	60A	cycles	8-10 years	140mΩ	114mΩ
591-398 12V, 5.7Ah		80A	(see note 2)		74mΩ	60mΩ
591-786 12V, 9.5Ah		80A			44mΩ	36mΩ
591-613 12V, 20Ah		100A			21mΩ	17mΩ
591-865 12V, 63Ah		440A			6.7mΩ	5.4mΩ
591-871 12V, 110Ah		770A			3.8mΩ	3.1mΩ
Lead Acid RS Dryfits A300						
591-922 12V, 1.1Ah		40A			380mΩ	311mΩ
591-966 12V, 1.8Ah	−30°C +50°C	40A	60-6000	8-10 years	233mΩ	190mΩ
591-938 12V, 3.0Ah		80A	cycles		140mΩ	114mΩ
591-944 12V, 5.7Ah		80A	(see note 2)		74mΩ	60mΩ
Lead Acid RS Cyclons						(see note 3)
591-461 2V, 2.5Ah		130A	≥250	8-10 years		10mΩ
591-483 2V, 5.0Ah	−40°C +65°C	200A	cycles	to 80% capacity		5mΩ
591-629 2V, 25Ah		750A	(see note 5)	(see note 4)		2.2mΩ
Alkaline Cells						(see note 3)
591-657 AAA						175mΩ
591-225 AA						160mΩ
591-231 C	−20°C +50°C	0.9A	1 cycle	2 years		130mΩ
591-247 D						120mΩ
591-792 PP3						2.7Ω
Ni-Cad Sintered Cells						
592-026 N		0.9A			105mΩ	
591-146 AAA		1.0A			80mΩ	
591-051 AA		35A	700-1000		20mΩ	
591-045 C	−30°C +50°C	70A	cycles	7 years	8mΩ	
591-039 D		110A			5mΩ	
591-095 PP9		2.4A				
Ni-Cad High Temp Cells						
	(see note 7)					(see note 3)
592-032 D	−40°C + 65°C				6.5mΩ	3.75mΩ
592-048 3 × D, Stick	(reduced spec)	24A	800-1000	4-6 years	19.5mΩ	11.25mΩ
592-054 3 × D, Stick	−20°C +45°C (full spec)		cycles		19.5mΩ	11.25mΩ
Ni-Cad Mass Plate	(see note 8)					(see note 3)
591-477 PCB Battery		180mA			1.5Ω	930mΩ
591-089 PP3	Max limits	180mA			3.5Ω	2.17Ω
591-168 Button Cell	−20°C +50°C	300mA	300	5 years	375mΩ	190mΩ
591-174 Button Cell		560mA	cycles		200mΩ	100mΩ
591-180 Stack	0°C +45°C	200mA			1.87Ω	850mΩ
591-196 Stack	recommended	560mA			1.4Ω	700mΩ

Notes:

1. These currents are only possible if the leads have sufficiently low resistance and are soldered onto the tags provided.
2. See text.
3. At 1kHz.
4. Kept on float charge of 2.40V/cell at T_a=25°C.
5. At 2.45V charging voltage to 80% capacity.
6. Max values for fully charged batteries at 20°C.
7. A maximum of 75°C is permissible for up to 24 hours.
8. At temperatures below 0°C, maximum discharge is C/2.

Lead Acid Batteries

Lead acid RS dryfits A200 and A300.
Note: unless otherwise specified all details refer to both A200 and A300 types.

Dryfit A200 batteries are suitable for both standby/float applications and also for applications where many regular discharge and recharge cycles are required.

Dryfit A300 batteries are designed specifically for use in standby/float applications where an occasional complete discharge/recharge cycle may occur. They are also highly suited for applications with long intervals between individual discharges.

All dryfit batteries are made with a thixotropic gel of acid electrolyte locked between sets of anode and cathode plates housed in a vented high impact ABS case. (Except for the 12V 63Ah and 110Ah which have polypropylene cases.)

Particularly for standby/float applications we recommend coating the battery connections with a silicone grease (RS 555-083) or petroleum jelly.

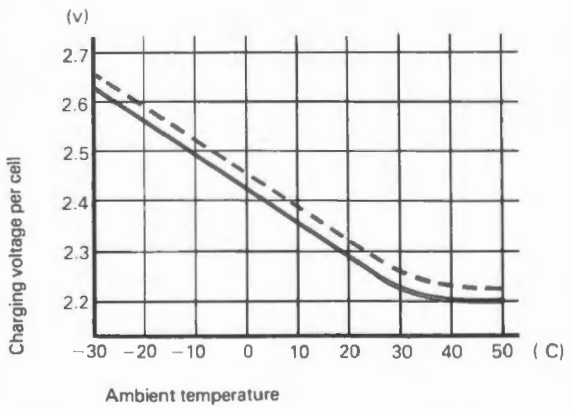
Charging information

These batteries **must** be charged from a **constant voltage** source. The optimum continuous charging voltage for a dryfit battery is 2.30V/cell at +20°C ie. for a 6V battery the charging voltage is 3 x 2.30V = 6.90V. In the case of continuous operation at higher/lower temperatures, the charging voltage should be adjusted according to the curve in Figure 1.

It should be noted that with constant voltage charging the charge current is regulated automatically by the battery.

To avoid reaching the temperature-dependent gassing voltage, the charging voltage, including any ripple should not deviate by more than ±30mV per cell.

Figure 1 **RS Dryfits A200 and A300 Charging voltage versus ambient temperature**



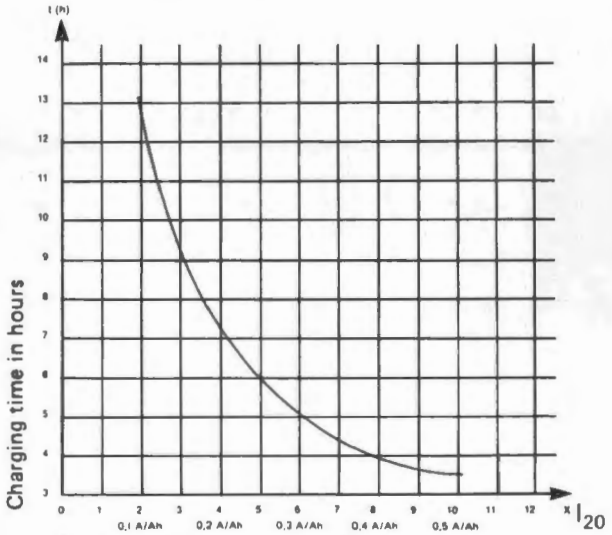
Dependency of the optimum final charging voltage for attaining full charge on extreme ambient temperatures. Dotted line = highest permissible, short time peak values, e.g. a superimposed a.c. ripple.

After being fully discharged the charging current can initially be 3A/Ah for several seconds and then decrease during the remaining charge period. It is therefore essential that current limiting is employed if smaller charge currents are required. The charge period can be calculated using Figure 2. When the charge current has settled and is say 0.3A/Ah then the total charge period will be approximately 5 hours.

When the battery is used for standby purposes only and the charger is permanently connected then the charging voltage may be reduced to a nominal 2.25V/cell. Such a charging voltage is often used in alarm control panels.

If the method of operation is entirely cyclic (dryfit A200 types only), ie. the battery is continually charged and discharged, then a slightly higher charging voltage may be used to achieve a shorter charging time. Under cyclic operation and at normal temperature a maximum charging voltage of 2.35V/cell is permissible provided that the battery never remains connected to the charger for longer than a week.

Figure 2 **RS Dryfits A200 and A300 Charging time* versus charging current**



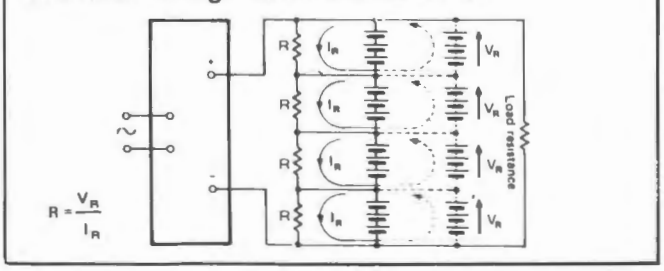
*for a fully discharged battery to achieve 90% full charge.

Charging methods

Series charging: is only recommended for batteries which have the same Ah capacity, state of charge and age. Normally these conditions only occur when the batteries are also discharged in series.

The recommended maximum number of cells that can be charged in series is limited to 12 ie. giving a 24V battery. To maximise battery life this maximum should only be exceeded if some form of active voltage sensing and current sharing is applied on every 12 or 24V block of cells. With such precautions against overcharging of particular cells there is no limit to the number of series connected cells.

Figure 3 **Series/Parallel charging circuit** Constant voltage current limited PSU



Series/Parallel charging: for maximum life the batteries should be connected as in Figure 3. The resistors R should be matched to within 5% and have their values chosen to provide an I_R of 5-10mA/Ah of the battery stack. It should be noted however that some practical tests have shown that there is little or an insignificant degredation in life if these precautions are not taken.

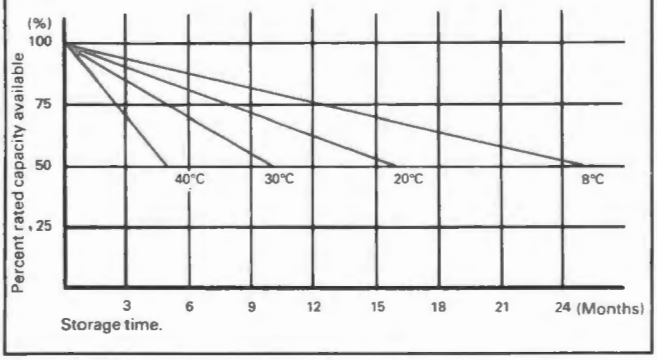
Parallel charging: parallel charging should present no difficulties but due to the higher currents that can flow, care must be taken to allow for sufficient current from the charger. A circuit of a simple multi-range Lead Acid cell charger is shown in Figure 16.

RS dryfits may be operated and stored in any position and are maintenance free. However, the possibility of charging equipment malfunction resulting in gassing should not be ignored. In the event of a build-up of gas pressure in the battery the automatically resealing safety valves ensure that this excess pressure can be immediately released. For this reason the valves must never be covered in an installation and batteries must not be enclosed within an unventilated enclosure. In fixed installations, care should be taken to ensure that these valves point upwards (ideally) or to the side. Severe overcharge can result in both gas and electrolyte being released. The presence of sparking components in the vicinity of the installed battery should be avoided.

Discharge performance

The self discharge rate of all dryfit types is low and long shelf-life is obtained (see Figure 4) by storing in a suitable environment. When storing lead acid batteries for a long time however, the state of charge should not be allowed to fall below the critical level and cycle charging is recommended every 16 months. Batteries should not be stored permanently below −10°C.

Figure 4 **RS Dryfits A200 and A300**
Self discharge at different temperatures



The rated capacity of all dryfit A200 batteries is stated for a discharge current of I_{20} and for A300 for a discharge current of I_{10} (both at an ambient temperature of 20°C). It should be noted that the removable capacity is reduced when the discharge current is increased. Figure 5 shows this for the A300 types and Figure 6 shows this, and also the reduced capacity at lower temperatures, for the A200 types.

Figure 5 **RS Dryfit A300**
Percentage available capacity at different discharge currents

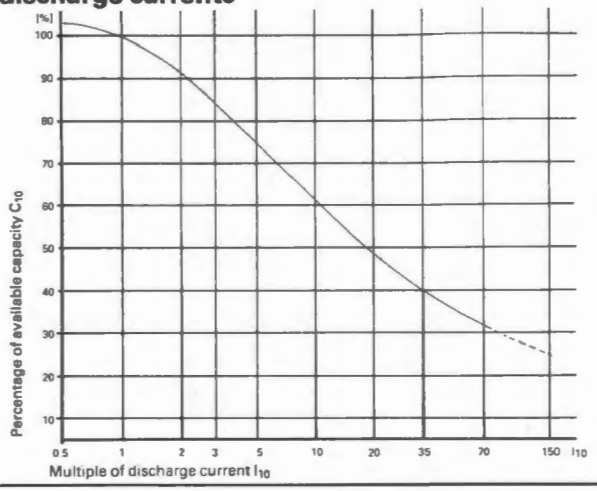
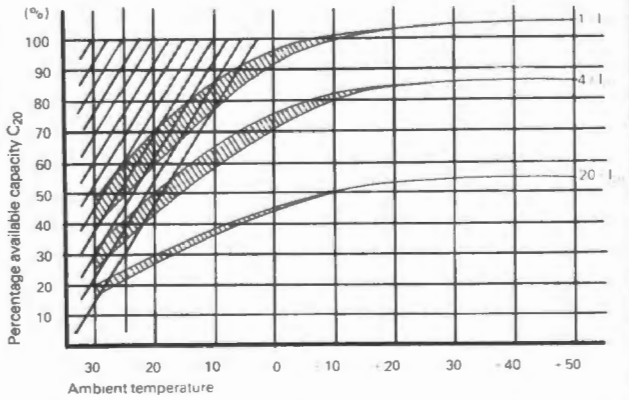


Figure 6 **RS Dryfit A200**
Percentage available capacity at different temperature and load conditions



Upper edge of curves: Charge at +20°C, discharge at temp. specified
Lower edge of curves: Charge and discharge at temp. specified
Note: To prevent permanent damage to the capacity of batteries at extremely low temperatures, the cross-hatched area //// should be avoided.

In open circuit, the fully charged dryfit battery has an ambient temperature dependent voltage of between 2.10 and 2.15V/cell. Up to one day after charging, any residual gas loading of the plates will give a higher voltage, although after a longer period this will approach the values stated, or will quickly collapse under load.

The dryfit on load voltage and on load endpoint voltage will be respectively 2.12V/cell and 1.75V/cell at the C/20 rate for A200 types and C/10 rate for A300 types. These voltages however are significantly lower at higher discharge rates and this is clearly shown (Figures 7 and 8).

Figure 7 **RS Dryfit A200**
Endpoint voltage versus discharge time

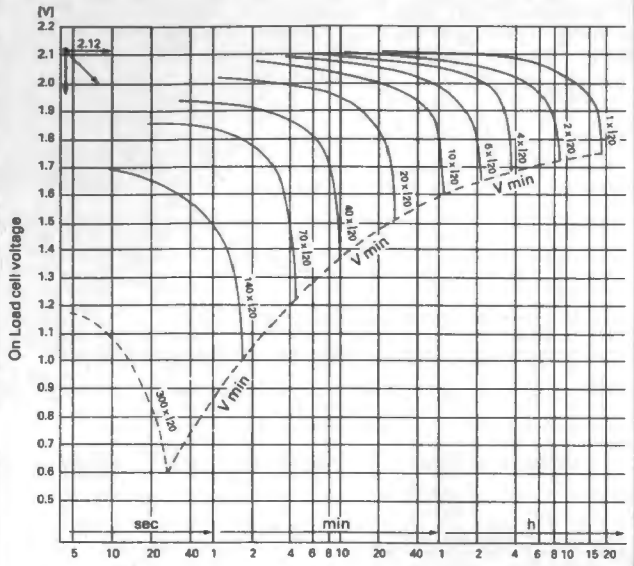
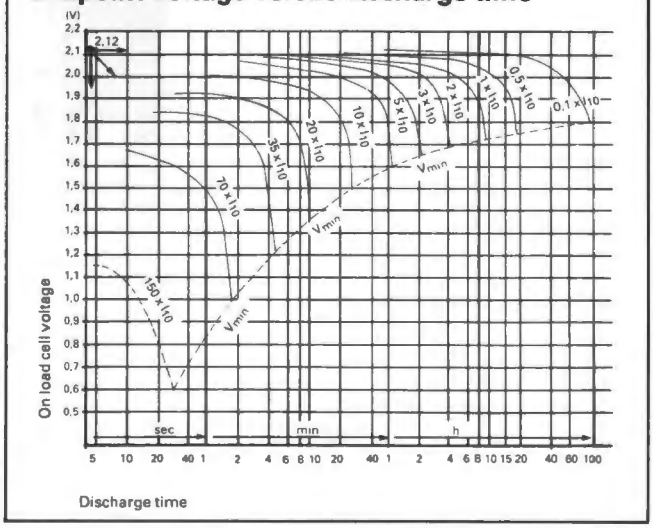


Figure 8 **RS Dryfit A300**
Endpoint voltage versus discharge time



The discharge times for the various Ah capacities of dryfit are shown against discharge current in Figure 9 (A200) and Figure 10 (A300).

Figure 9 **RS Dryfit A200**
Discharge time versus discharge current

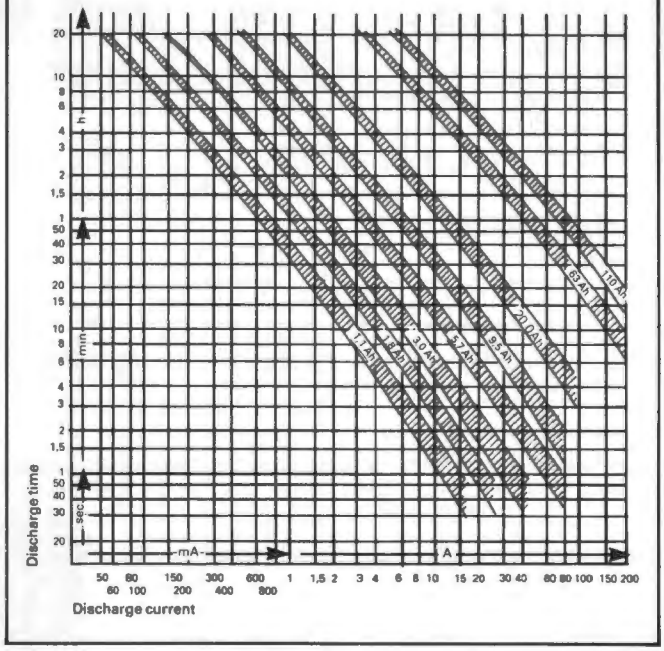
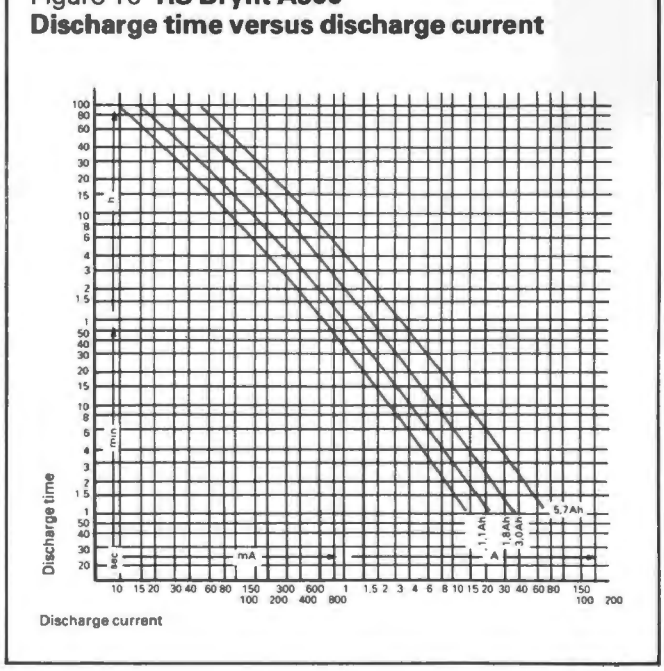


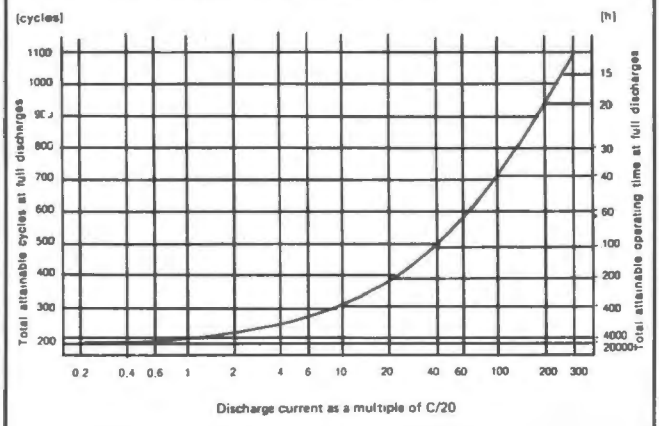
Figure 10 **RS Dryfit A300**
Discharge time versus discharge current



Cyclic life

The cyclic life of a dryfit battery is dependent on the amount of capacity withdrawn during each discharge/recharge cycle. Each dryfit A200 will deliver a total of 200 times its nominal capacity during its cyclic life, eg. 200 cycles at 100% capacity withdrawn, 400 cycles at 50%, 2000 cycles at 10% and 20,000 cycles at 1%. The same rule can be applied to the 60 cycles at 100% of the dryfit A300. In addition to this the cyclic life of a dryfit increases with increased discharge current and this is clearly shown for the A200 in Figure 11.

Figure 11 **RS Dryfit A200**
Cyclic life versus discharge current



N.B. Deep discharge of RS dryfits
When RS dryfits have been left connected to a permanently discharging load, or when the on load terminal voltage falls below V min as given in Figures 7 and 8 (eg. 1.75V/cell at a discharge rate of C/20 for a dryfit A200) then the battery is in a deep discharged condition.

Provided the battery is recharged within 4 weeks then no damage to the cell(s) will occur. However very low charge rates (5mA/Ah or less) and greatly extended charge periods (up to 72 hours or above) should be expected. It **may** still be possible to recover the battery from deep discharge conditions in excess of four weeks duration but the likelihood of damage from excessive discharging is minimised if the battery is put on charge as soon as possible.

Pressure limits
The maximum pressure limit for dryfit batteries is 4 bar, equivalent, for example, to a water depth of 30m. Suitable precautions must, however, be taken to ensure in this type of application that no water can penetrate the valves and that no self discharge can occur via the live parts.

The minimum permissible pressure limit is 0.03bar, equivalent to a height of 30km, with the temperature not exceeding +25°C. At the short term permissible maximum temperature of +80°C, the minimum pressure limit is 0.3bar, corresponding to a height of 9.5km. Since ambient temperatures at altitude are generally extremely low, the resultant reduction in capacity shown in Figure 6 must be taken into account.

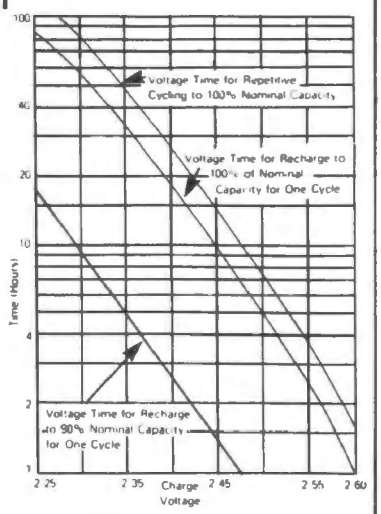
Lead acid RS cyclon

Charging information
These batteries may be charged either *constant voltage* or *constant current*. They should not be charged in a gas tight container.

Constant voltage charging is the most efficient and fastest way to charge the RS Cyclon. The constant voltage charge ranges between 2.30 and 2.55V/cell with the appropriate charge times for a 100% discharged cell given in Figure 12.

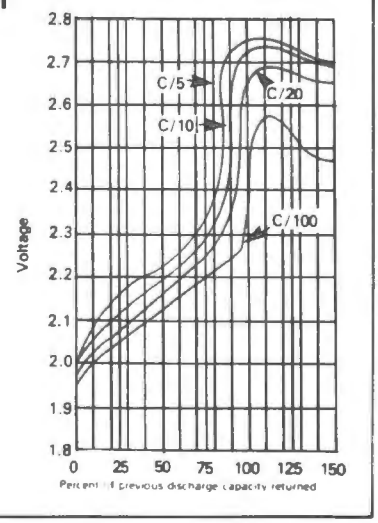
Note: the curves apply to a charger capable of giving charge rates in excess of 2C (i.e. 5A for each 2.5Ah cell, 10A for each 5.0Ah cell and 50A for each 25Ah cell connected in parallel). For chargers with charge rates less than 2C the charge times given in Figure 12 should be increased by approximately the hourly rate at which the charger is limited ie. if the charger is limited to the C/10 rate then 10 hours should be added to each of the charger voltage/time relationships; if the charger is limited to the C/5 rate then 5 hours should be added etc.

Figure 12 **RS Cyclon**
Charge voltage vsTime on charge at 23°C



Floatcharging: the recommended voltages can vary between 2.30 and 2.40V/cell. Depending on battery voltages the following charge voltages are recommended: 2.35V/cell up to a 12V battery; 2.38V/cell up to a 50V battery; 2.4V/cell up to a 110V battery. Lower charge voltages may be used if longer recharge times are acceptable.

Figure 13 **RS Cyclon**
Voltage curves for constant current charge rates at 23°C



Cyclic charging: for cyclic charging, voltages between 2.40 and 2.55V/cell may be selected. The time duration of the charge can be determined from Figure 12. Figure 17 gives circuit details for a suitable constant voltage charger.

Constant current charging is particularly effective when many cells are to be charged in series. It tends to eliminate any charge imbalance in a battery stack as it is independent of the charge voltage of the cell.

The recommended indefinite constant current charge is C/500. The battery can be charged at higher rates but voltage or time limitation must be used for rates in excess of this, see Figure 13.

Figure 14 **RS Cyclon**
Open circuit terminal voltage versus capacity

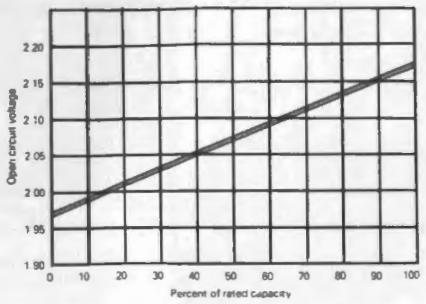
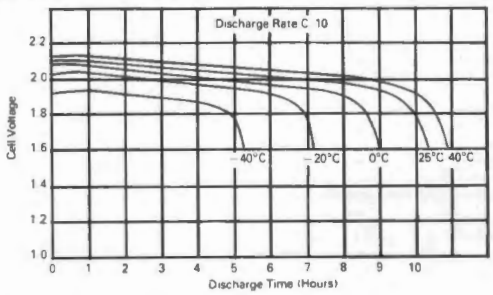


Figure 15 **RS Cyclon**
Endpoint voltage versus discharge time



Discharge performance
The Cyclon cell has a low self discharge rate. An indication of the state of charge can be obtained by monitoring the open-circuit terminal voltage. Figure 14 shows a curve of this voltage versus capacity for a Cyclon cell as 23°C, with the capacity being that available at the C/10 rate of discharge. The returned capacity of the Cyclon is dependent on temperature and Figure 15 shows the discharge characteristics for C/10 discharge rate at various temperatures.

N.B. Deep discharge of RS Cyclons
When RS Cyclons have been left connected to a permanently discharging load or the terminal voltage on load falls below 1.6V (at C/10 rate) the cell is then in a deep discharge state. Recovery from this state without cell damage is possible if the cells are recharged immediately. Very low initial charge rates and greatly extended charging periods are likely to be experienced under these conditions.

Circuits for lead acid battery chargers

Figure 16 **Simple multi-range lead acid battery charger**

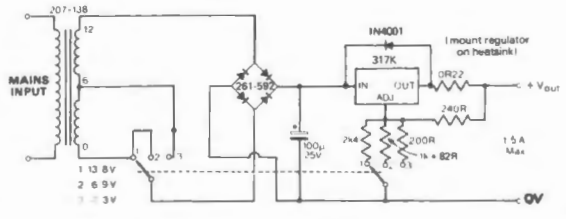
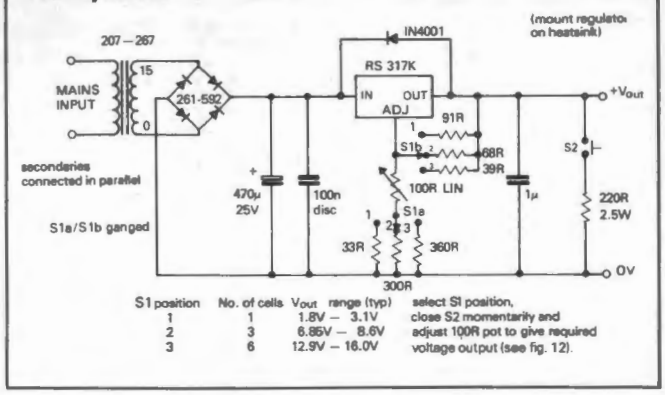


Figure 17 **Constant voltage charger for RS Cyclons**



S1 position	No. of cells	Vout range (typ)	select S1 position, close S2 momentarily and adjust 100R pot to give required voltage output (see fig. 12).
1	1	1.8V – 3.1V	
2	3	6.85V – 8.6V	
3	6	12.9V – 16.0V	

Alkaline batteries

The Ah capacity of these cells is greatly dependent upon the load, in general the heavier the load the better the performance of the cell. The cells are fully sealed and when disposed of they should not be incinerated.

These cells cannot be recharged and if attempted, explosion of the battery may occur.

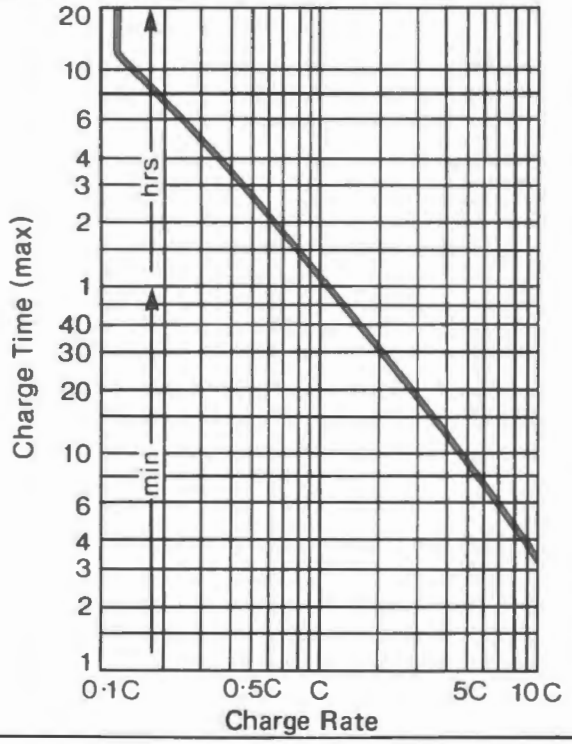
Nickel-cadmium batteries and cells

All types of nickel-cadmium batteries and cells can be charged and discharged in any position and can be satisfactorily used in comparatively hostile environments. Unlike lead acid batteries Ni-Cads can be stored for periods in excess of 5 years without the need for periodic recharging to ensure good life. All cells and batteries are supplied holding only a residual charge and will therefore usually require a full charge before use. Cells can be potted provided the temperature does not rise above 50°C (60°C short term) during the potting stage. The vent in the top of the case (sintered cells) must have an external air space to allow for the escape of gas when severely overcharging.

Charging information
It is recommended that Ni-Cad cells are charged from a constant current source only. Non constant current charging is only permissible if the recommended continuous charge rate is not exceeded once the cell has reached a fully charged state.

The maximum indefinite charge rate for *standard sintered cells* and *high temperature sintered cells* is C/8, ie. for a 4Ah cell this represents a charging current of 500mA. At this charge rate the cell will fully charge in approximately 12 hours (ie. when the charge equivalent of 150% of the Ah capacity has been returned to the cell). Higher charge rates, which result in an accelerated charge, are permitted for sintered cells. The N, AAA, PP9 and high temperature cells have a maximum charge rate of 2C and the AA, C and D cells a maximum rate of 10C. It is recommended that at charge rates of C or greater the cell is fully discharged prior to recharging. The cell should then be charged for the time shown in Figure 18. Thus for a 4Ah standard D cell charged at the 8C rate (32A) the total charging time, which must not be exceeded, is 5 minutes.

Figure 18 **Charge period versus charge rate**



When fast charging adequate ventilation must be arranged in order to allow any gases which may be generated to escape. All the sintered cells are fitted with an automatically resealing safety vent which will operate under conditions of charge abuse. When charging at low rates it should be noted that sintered cells have a minimum charge acceptance rate of C/40.

The nickel cadmium *mass plate* cells and batteries have lower recommended maximum charge rates (C/10) than sintered cells because of their plate construction. They are however ideal for use under continuous trickle charge conditions, e.g. memory back-up supply applications, having a recommended continuous charge rate of C/100 (1.1mA for the PP3 battery). At the maximum charge rate of C/10 (11mA for the PP3) the cells will be fully charged in approximately 14 hours. Although fully charged after this time the charging period can be extended by up to 300% without damage to the cells.

A typical general purpose charging circuit for Ni-Cad batteries and cells is shown in Figure 25.

The primary use of the PCB battery is to provide onboard C-MOS or N-MOS volatile memory support in the event of main supply failure. The circuit shown in Figure 26 is a simple, permanently connected, circuit for trickle charging the battery from the logic supply. Diode D_1 protects the power supply regulator in the event of an ac mains supply failure and may be omitted if protection is already provided.

Discharge information

Ni-Cad cells exhibit a relatively flat voltage/time discharge characteristic which is dependent on the discharge current. Except at higher discharge rates the end point voltage is usually taken to be 1.0V. Typical discharge curves are shown for sintered and mass plate cells in Figures 19 and 20 respectively.

Figure 19 **Sintered cell discharge time versus cell voltage for different discharge rates**

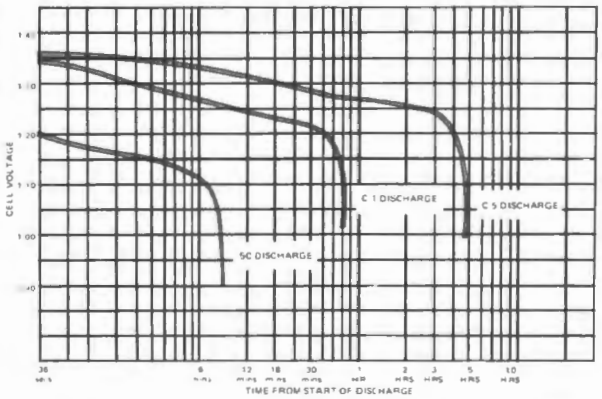
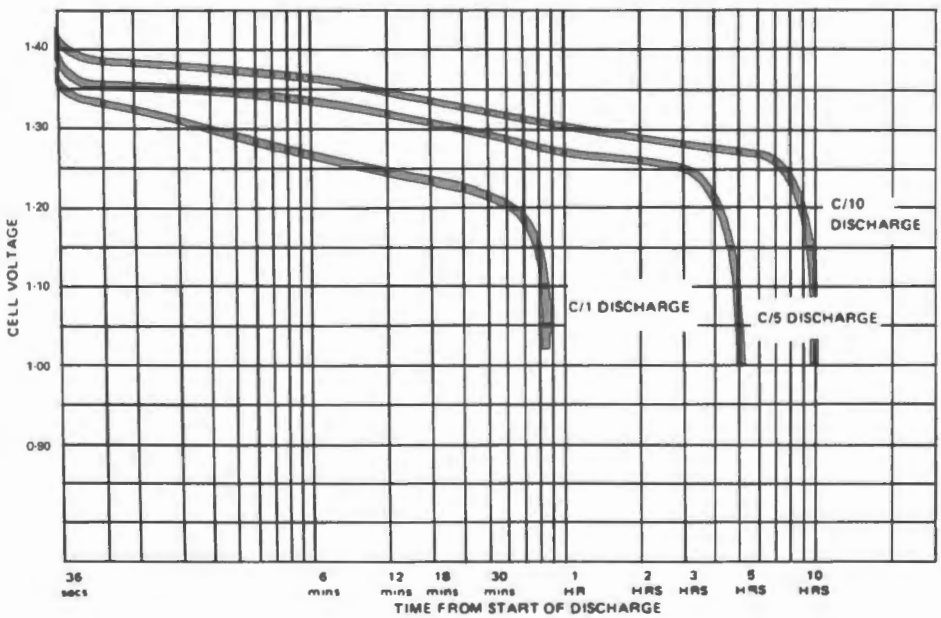


Figure 20 **Mass plate cell discharge time versus cell voltage for different discharge rates**



When discharging Ni-Cad cells in series care must be taken not to allow the voltage to fall below 1V/cell when discharging at rates greater than C/5 (sintered cells) or C/10 (mass plate cells) as damage may occur due to a cell being reverse charged.

The construction of sintered cells is such that they have a relatively low internal resistance and therefore considerable maximum discharge currents can be obtained (see Table 3).

Although the on charge voltage is between 1.4 and 1.5V per cell this falls to an average of 1.25V during discharge.

High temperature applications

For applications where higher ambient temperatures are likely to be experienced the high temperature sintered D cells and battery packs offer the best solution. Although standard cells can be charged and discharged at temperatures up to 45°C and 50°C respectively the charge acceptance and charge retention properties of the cells at these temperatures may be affected resulting in reduced capacity. Certainly at temperatures above 50°C the reliability and capacity of standard sintered cells is degraded by oxidation of the electrodes and degradation of the non woven separator material. The high temperature cells use special electrodes and polypropylene separators to minimise these effects. They exhibit a good charge acceptance at elevated temperatures (see Figure 21) and improved charge retention, ie. self discharging performance (Figure 22) compared with standard sintered cells (Figure 23). It should be noted however that mass plate cells have better discharge figures than any of the sintered plate types (Figure 24).

Figure 21 **Charge acceptance of high temp. cells - Achievable capacity versus charge rate**

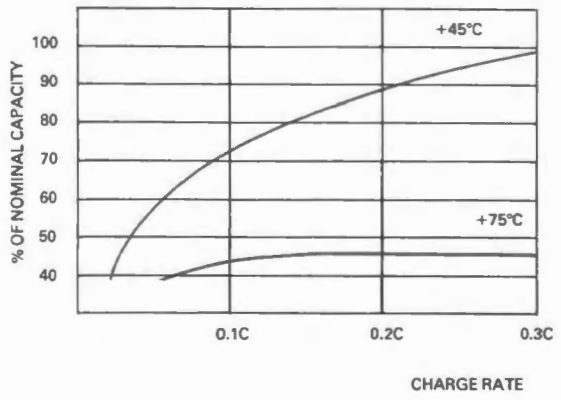


Figure 22 **Capacity versus time at different temperatures for high temp. cells**

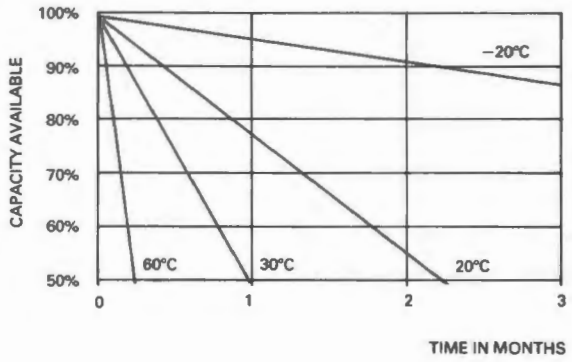


Figure 23 **Capacity versus time at different temperatures for standard sintered cells**

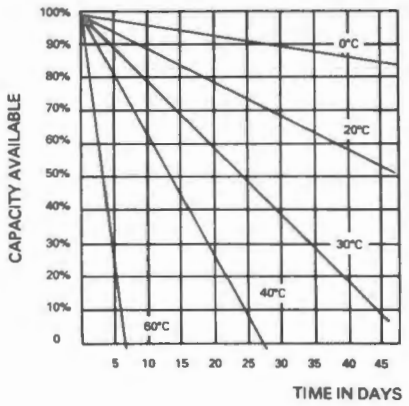
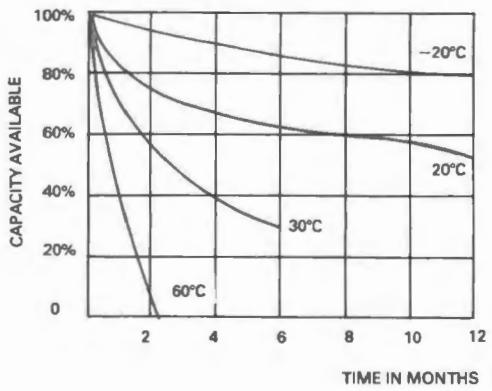
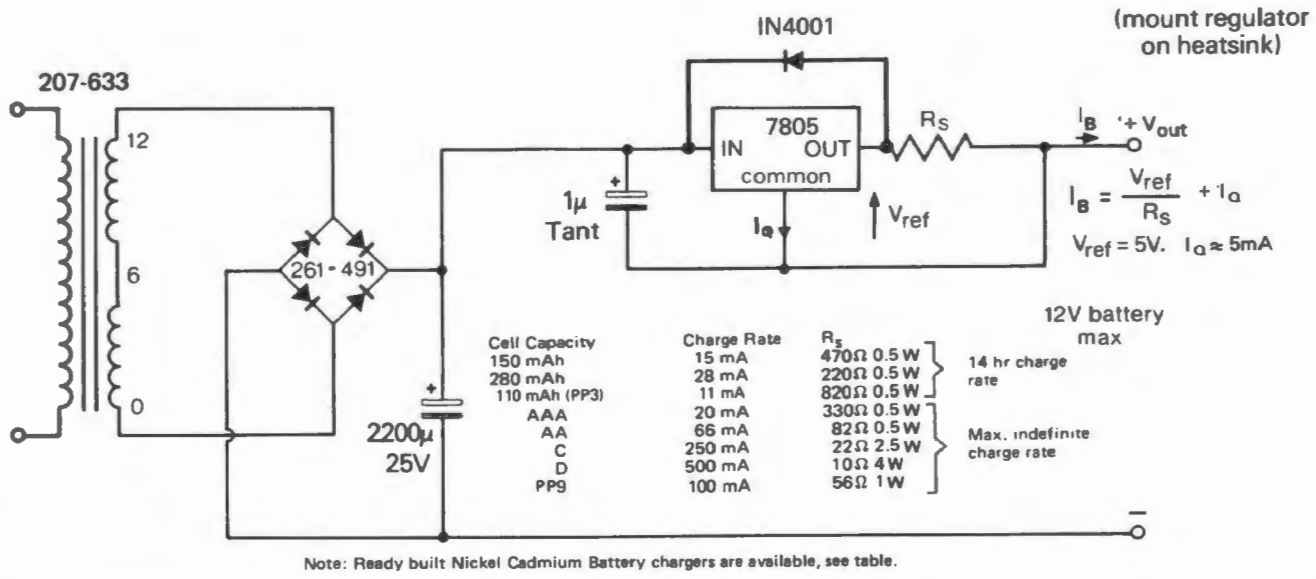


Figure 24 **Capacity versus time at different temperatures for mass plate cells**



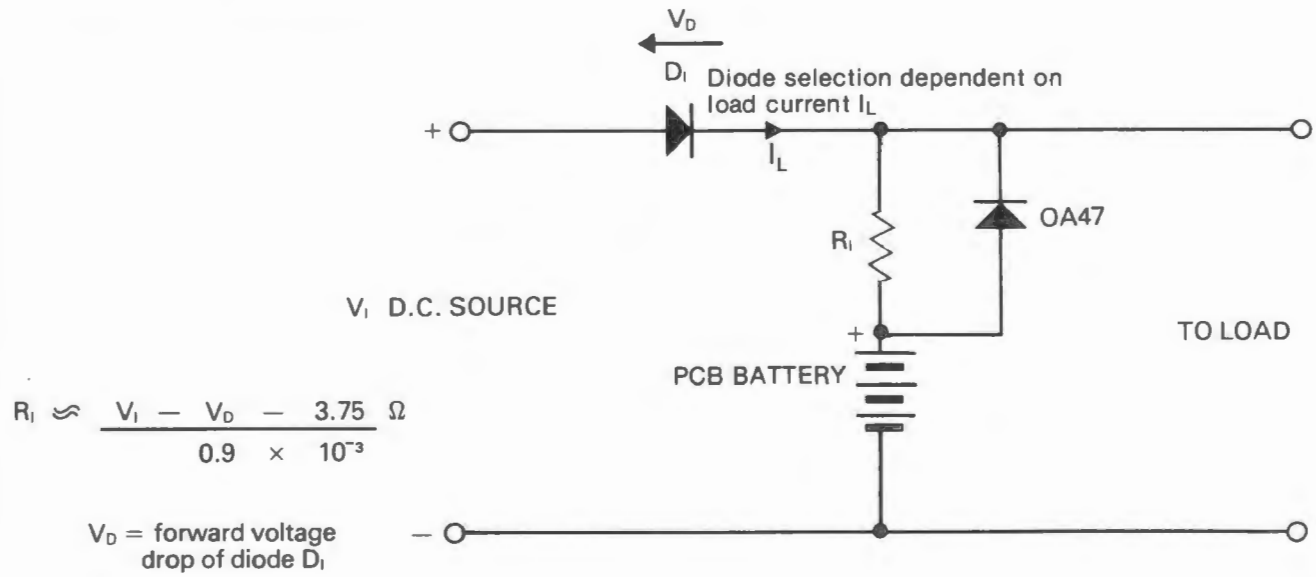
RS data

Figure 25 **Ni-Cad battery charger**



Note: Ready built Nickel Cadmium Battery chargers are available, see table.

Figure 26 **PCB battery charger**



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RS data

Industrial sockets and plugs, metal-clad, weathertight IP55

A range of pressure diecast zinc alloy weathertight sockets and plugs for industrial use. The range comprises:

Stock no.	13A BS 1363 gauge types*	
487-491	Plug, fused 12A	2p+E
487-508	Socket, surface mounting	2p+E
487-514	Socket in modular housing	2p+E
487-520	Socket with 15A IP Switch	2p+E
Stock no.	**5A Walsall gauge types**	
487-536	Plug, unfused	2p+E
487-542	Plug, unfused	3p+E
487-564	Socket, surface mounting	2p+E
487-570	Socket, surface mounting	3p+E
Stock no.	**15A Walsall 'B' gauge types**	
487-558	Plug, unfused	3p+E
487-586	Socket, surface mounting	3p+E
487-592	Socket in modular housing	3p+E

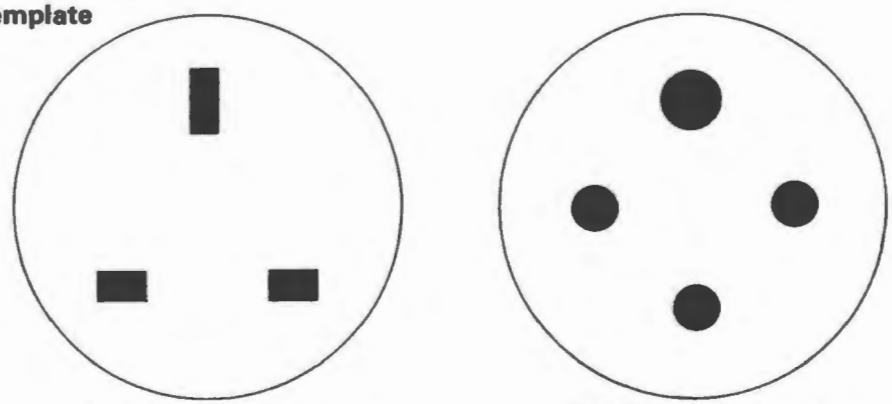
Maximum voltage ratings 240V dc 500 V ac.

*** 13A BS 1363 gauge types**
Since this specification was written for domestic/commercial applications we only claim that the pins are to that gauge. The specification has some requirements which are not relevant to the specific weathertight design.

Features

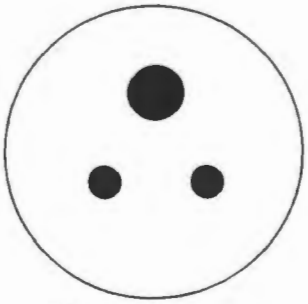
- **Metal-clad exteriors** providing good mechanical strength.
- **Environmentally protected to IP55.** Sockets are designed to maintain the protection, even when not in use, by using the protective screw cap.
- **Corrosion resistant.** Finished in a black epoxy resin stoved powder coating which is superior to conventional paints in resisting corrosion and weathering. All steel screws and chains are zinc plated and passivated yellow.
- **Single and three phase applications.** The range includes both two pole and three pole versions in 5A ratings. Two pole + earth 13A and three pole + earth 15A units are also available. This covers a wide range of industrial applications.
- **Fused plug and shuttered socket.** The 13A BS 1363 gauge types* retain the two excellent features that are the accepted 'norm' in domestic applications. Firstly the facility to 'fuse down' so as to provide protection to the appliance. Secondly the shuttering on the socket to discourage unorthodox use.
- **Modular housing** available for the 13A BS 1363 gauge and the 15A, 3p+E, Walsall 'B' gauge types. This allows for combining the socket outlets with a variety of equipment to DIN 43 880 dimensions (mcb's, rccb's, timers etc.).

Figure 1 **Gauge template**

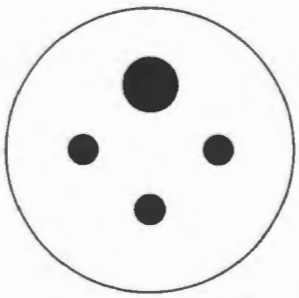


13A BS 1363 gauge*
2 pole + Earth

15A Walsall 'B' gauge
3 pole + Earth



5A Walsall gauge
2 pole + Earth



5A Walsall gauge
3 pole + Earth

*** See note on page 1.**

Plugs

All the plugs in the range are fitted with a locking ring and a rubber facia gasket. When the plug is mated with a socket and the locking ring hand tightened the sockets and pins are protected. A rubber gaiter provides further protection at the cable entry point.

To wire up a plug, first the gaiter has to be removed from the plug and fitted over the cable. This will expose the two screws holding the internal polypropylene cable clamp (see H on Figure 3). A further two screws, one on the barrel and the other on the plug face under the gasket, have to be unscrewed so that the moulded interiors (glass filled polypropylene) can be removed. This then gives access to the screw terminals.

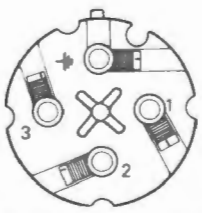
The 2 pole + earth versions are marked with the phase (L) neutral and earth symbols. The 3 pole + earth versions are not always marked so care has to be taken to ensure that the phases are properly sequenced. The plug interiors diagram (Figure 2) shows the correct number sequencing to correspond with the numbering on the sockets.

The 13A BS 1363 gauge plug is supplied with a 13A BS 1362 fuselink. This may be replaced by one of a lower rating, if desired. The RS range of BS 1362 fuselinks is available in packs of 10 as follows.

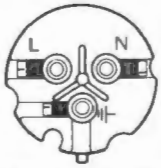
Current rating (A)	Stock number
1	412-986
2	412-554
3	412-560
5	412-576
7	412-582
10	412-598
13	412-605

Figure 2 **Plug interiors**

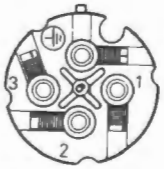
13A BS 1363 gauge 2 pole +E



15A Walsall 'B' gauge 3 pole +E



5A Walsall gauge 2 pole +E



5A Walsall 'B' gauge 3 pole +E

All interiors, except the BS 1363 gauge version, are in two parts. The diagrams show the main part and are intended as a wiring guide only.

Sockets

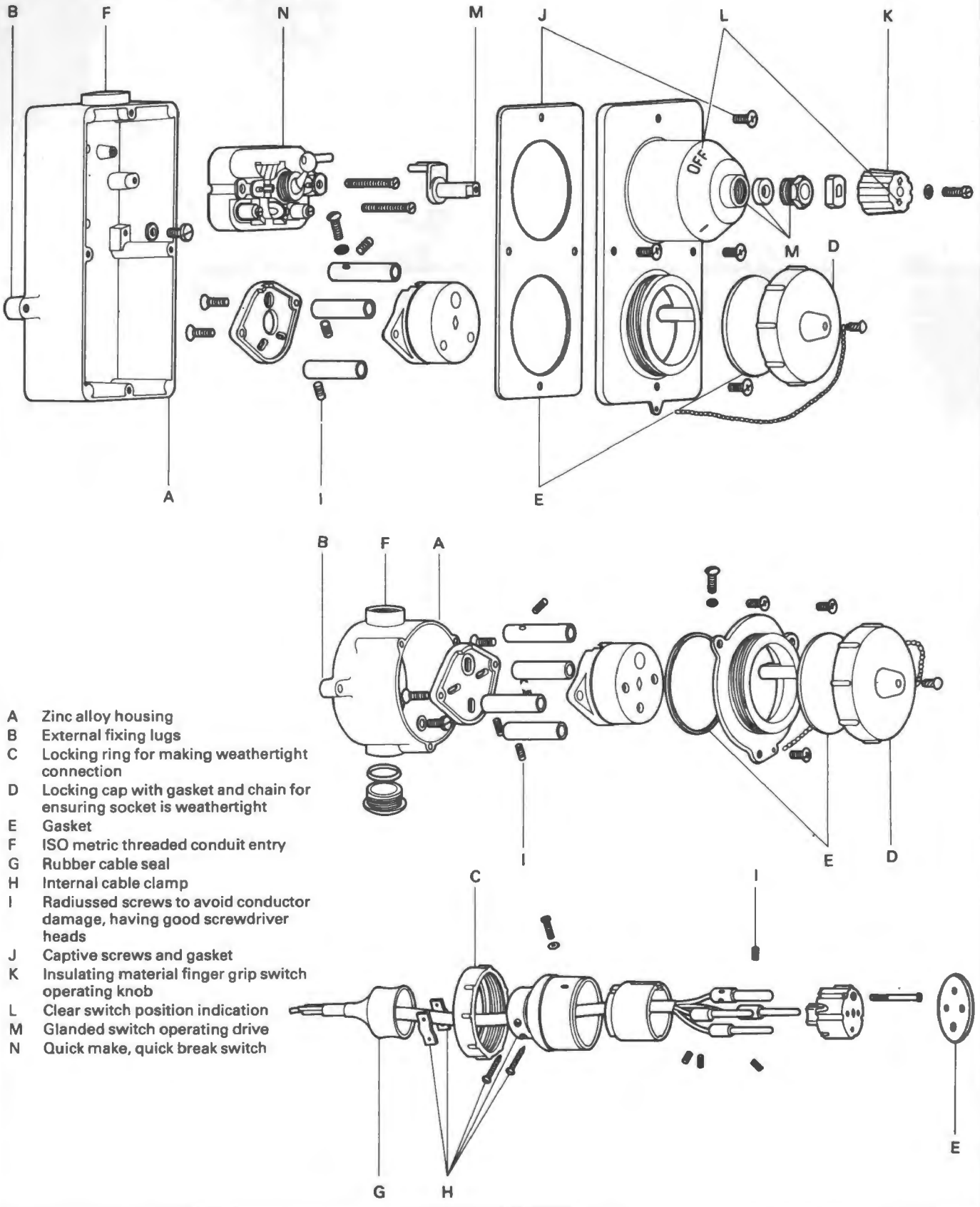
The sockets have a locking cap with gasket secured to the socket body by a chain. This cap should be fitted to the socket and hand tightened so as to environmentally protect the unit when not in use. Access to the terminals may be gained by removing three exterior screws which hold the socket assembly onto its zinc alloy base. The cover, on the socket interior, need not be removed since the terminal screws are now accessible. The zinc alloy bases have 20mm ISO metric threaded entries. The 5A versions have one whereas the 13A and 15A versions have two with one blanking plug fitted. Mounting is via external lugs (see dimension drawings, Figures 8-11).

Switched socket

This unit combines a 13A BS 1363 socket outlet with a 15A single pole switch which has a quick make and break action. The switch is not wired to the socket. The socket is fitted with a locking cap, with gasket, to enable the unit to be protected when not in use. This cap should be hand tightened.

The locking cap is secured by a chain to the switch body. Four screws hold the socket and switch actuator to the zinc alloy base. The quick make, quick break switch (N) is mounted in the base. A single 25mm ISO metric threaded entry is provided. Mounting is via external lugs (see construction details drawings Figure 3).

Figure 3 **Construction details**

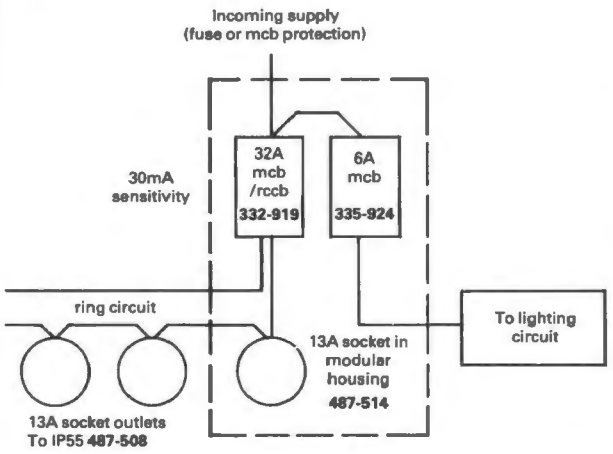


A Zinc alloy housing
B External fixing lugs
C Locking ring for making weathertight connection
D Locking cap with gasket and chain for ensuring socket is weathertight
E Gasket
F ISO metric threaded conduit entry
G Rubber cable seal
H Internal cable clamp
I Radiussed screws to avoid conductor damage, having good screwdriver heads
J Captive screws and gasket
K Insulating material finger grip switch operating knob
L Clear switch position indication
M Glanded switch operating drive
N Quick make, quick break switch

5910
Socket in modular housing

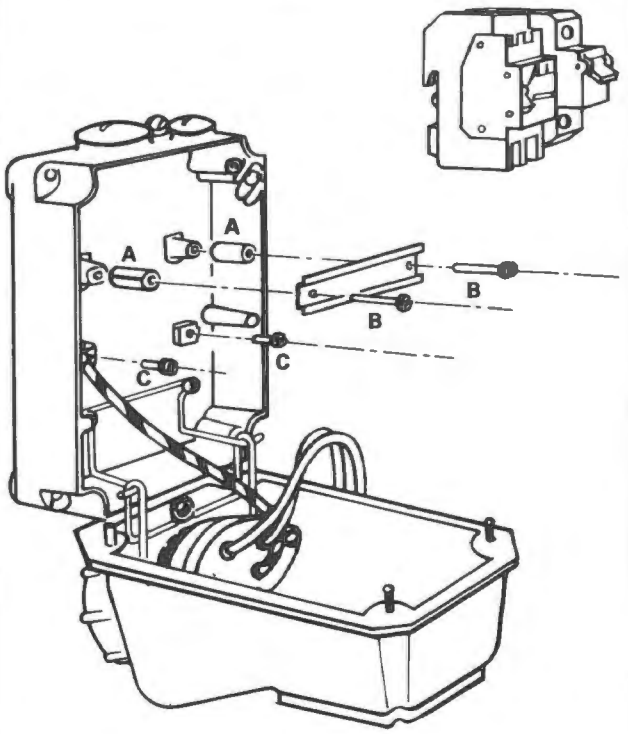
The 13A BS 1363 and 15A Walsall 'B' sockets are available combined with a housing that can accommodate electrical equipment, to DIN 43 880 dimensions, up to a maximum of 4 modules wide for front access. A variety of equipment is available for internal mounting. The use of mcb's, rccb's and motor circuit breakers can provide protection. Time clocks and remotely controlled contactors can provide control, either for starting, stopping or safety interlocking. A series of socket outlets can begin with a combined unit offering protection to the other sockets in the same circuit. A lighting circuit could also be included. The following typical illustration uses only three modules (width).

Figure 4 **Typical application**



Although most devices designed to DIN 43 880 have a uniform modular width (expressed in multiples of 17.5mm $^{+0.5mm}_{-0}$) and will fit through a front opening 45mm high, their depth from the rail can vary considerably. For this reason the modular housing has been designed to provide two mounting depths. In most cases the 34mm stand-off will be found to be suitable. The RS range of motor circuit breakers (see control gear/accessories section in the RS catalogue) requires a greater mounting depth. This may be achieved by removing the spacers (A) and attaching the 35mm symmetric DIN rail directly to the integral mounting pillars. This will provide a 16mm stand-off. The fixing screws (B) may be substituted by the shorter screws (C) (see Figure 5).

Figure 5 **Mounting screws**



At this 16mm stand-off the greater mounting width of the DIN rail can be utilized providing that access is not required from the front. This additional width (max. 28mm) allows for a motor circuit breaker (2½ modules) to be mounted alongside a contactor chosen from the E range (2½ modules). The former may be operated through the front. The latter, being of a smaller depth, can take advantage of the additional length on the rail. Where access is required through the front, a clear polycarbonate window, hinged at the top and sealed around the edge, is incorporated in the lid of the housing. A knurled, lid locking screw is used to secure the seal. Behind this window a vacuum formed pvc blanking piece is attached which may be sectioned out to permit equipment to fit through. This blanking piece is ribbed in half modular widths so that the sections can be accurately removed using a sharp knife (see Figure 6).

Figure 6 **Blanking piece cutting**

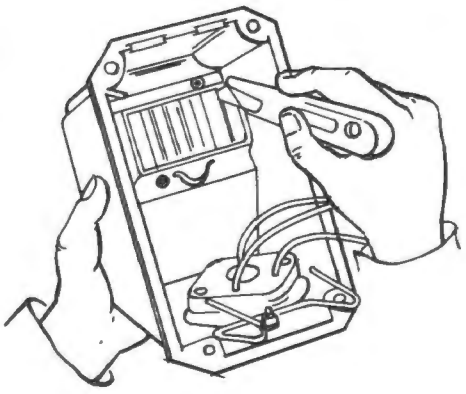
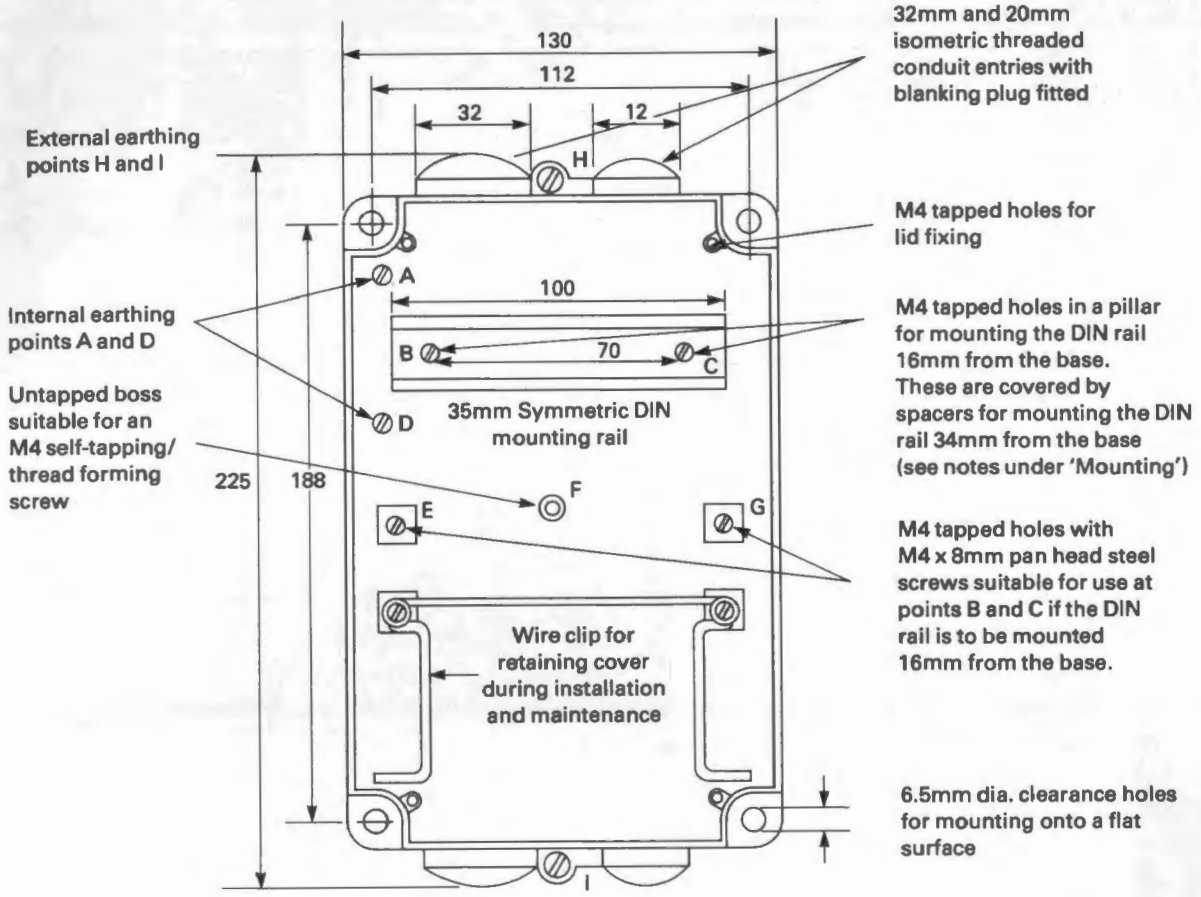


Figure 7 **Distribution within the modular housing**



Earth connections. The incoming protective conductor should be first connected to one of the internal earthing points A or D. Further earth connections may be made to either these internal points or to the external points H or I. An earth cable (green/yellow) is supplied wired to the socket and to earthing point D.

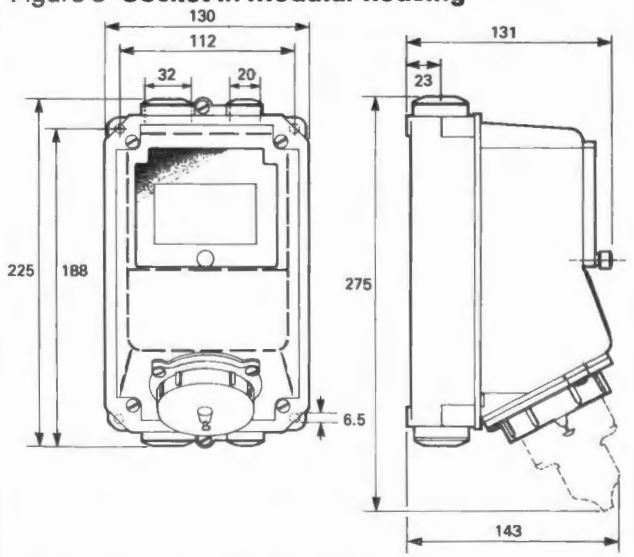
Neutral connections. The incoming neutral conductor will normally be connected to the modular equipment being used. Where neutral distribution is required (eg. to the socket outlet and to the motor of a time clock) a suitable terminal block may be selected from the RS catalogue. This may be a DIN rail mounting type chosen from the 'Universal' range or, where clearance permits, a panel mounting type. If the latter is chosen, one of the unused mounting pillars can be used for fixing purposes. A section cut from the 32A 12-way terminal block (Stock no. 425-083) can be mounted at point E using M4 steel screws. Point F can also be chosen for securing the terminal block with a self-tapping screw. A neutral cable (blue) is supplied, with the 13A BS 1363 gauge, 2 pole + earth unit, wired to the socket.

Phase connections. The 13A BS 1363 gauge unit is supplied with one brown, phase (L) cable wired to the socket at the terminal marked L. The 15A Walsall 'B' gauge 3 pole + earth unit is supplied with three brown, phase (L) cables wired to the socket. The socket terminals are numbered 1-3. Care should be exercised in ensuring that the phases are connected in the right sequence. It is recommended that a phase and continuity check is made after installation. A suitable instrument for this purpose is available from RS (Stock No. 424-585).

All wiring should be in accordance with the latest edition of the IEE Wiring Regulations.

Dimensions

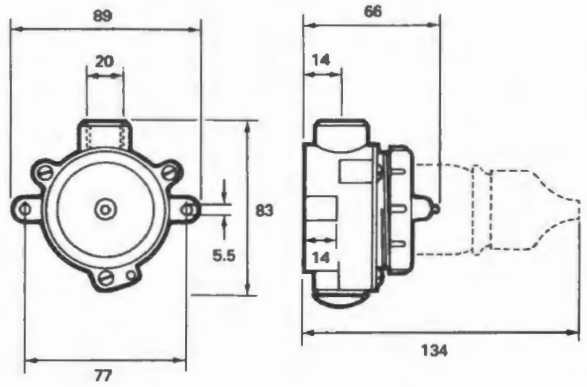
Figure 8 **Socket in modular housing**



13A BS 1363 gauge type 2 pole +Earth 487-514
15A Walsall 'B' gauge type 3 pole +Earth 487-592
For terminal capacities see page 6.

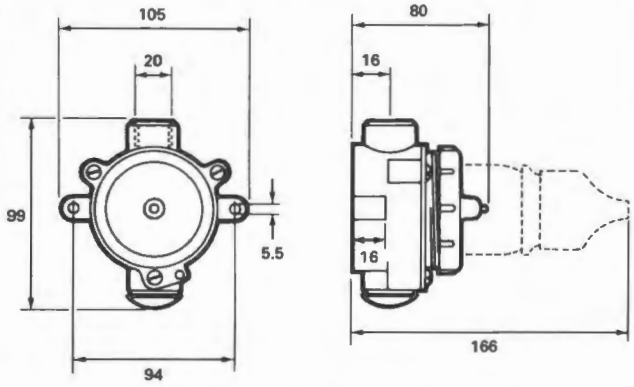
RS data

Figure 9 **Surface mounting sockets**



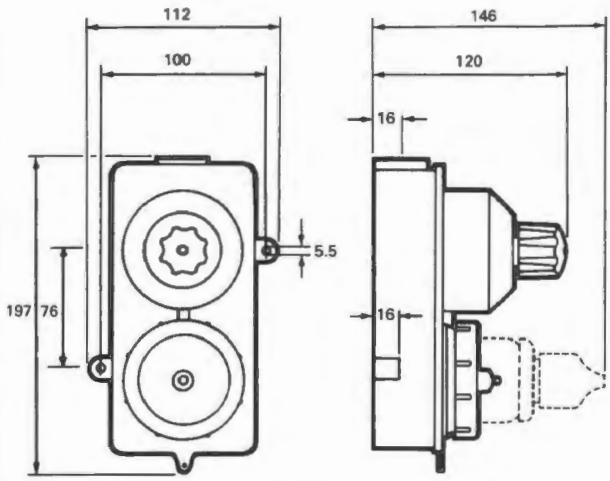
5A Walsall gauge type 2 pole +Earth 487-564
5A Walsall gauge type 3 pole +Earth 487-570

Figure 10 **Surface mounting sockets**



13A BS 1363 gauge type 2 pole +Earth 487-508
15A Walsall 'B' gauge type 3 pole +Earth 487-586

Figure 11 **Socket with 15A 1 pole switch**



13A BS 1363 socket with 15A 1 pole switch 487-520

Terminal capacities (maximum)

Dimensions are for csa of stranded connectors (mm^2)

Current rating (A)	Plug	Socket	
		One conductor	Looping conductors
5	6	6	2 x 4
13	6	10	2 x 4
15	10	10	2 x 4

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RS data

Disc drive exerciser

Stock numbers 630-083 and 630-099

This data sheet covers the following stock numbers:

Stock No.	Description
630-083	Disc drive exerciser
630-099	Adaptor pod for the RS disc drive exerciser to enable connection to 8in drives

Disc drive exerciser

Disc drive exerciser

The RS disc drive exerciser is a robust, compact unit capable of exercising the interfaces of most 3½in, 5¼in and, via an adaptor pod, Shugart compatible 8in disc drives

The unit contains two sections, an active and a passive. The active section allows drives to be stepped to 3 sets of the most commonly used tracks on alignment discs (also known as CE discs, Customer Engineering discs, and Cat's Eyes discs).

Features

- Simple to use
- Suitable for 40,77 and 80 track drives
- Robust, compact unit suitable for the field service engineer or bench use
- Signal connections suitable for 5¼in and 3½in disc drives, utilising the industry standard S.400 (Shugart) interface
- Optional adaptor pod for signal connection to Shugart compatible 8in disc drives
- Power connectors suitable for 5¼in disc drives. Adaptor power cables may be made up for 3½in and 8in drives
- Designed for high reliability with high quality switches and connectors
- Firmware (software encoded into EPROM) to speed up optimisation of track positioning mechanisms and limit switches.

The stepping rate can be set in half octave bands from 2.25ms per step to 24ms per step, (the value the unit defaults to on 'power up'). The active section of the unit requires that the track zero indicator line is working properly and if there is a fault in this part of a drive, it may be cleared using the passive section of the unit where stepping commands are given manually.

The unit has a standard drive power connector at the back and a flying power lead at the front. When 'daisy-chained' in series with the drive power connection, the unit picks up its 5V power (380mA) and indicates the 12V power (20mA).

The interface lines are all TTL compatible being either pulled up by terminating resistors of 150ohms on drive outputs or pulled up by 1kΩ resistors which are switched to ground. The 'step' and 'direction' lines are driven by open collector 7438 drivers with 1kΩ pullups to +5V. This enables the drive to be tested with or without a terminating resistor network with equal effect.

The ability to address all interface lines is available except drive select '2' and '3'. If a drive with this address is tested, it will need to be patched to either drive '0' or '1' temporarily.

The ability to check that all lines can be addressed by the interface is useful where a drive may have suffered electrical damage leaving some or all of the outputs stuck 'Enabled'. (This is a typical failure mode for drives which have suffered nearby CRT flashover.)

The unit is robust enough to live in the toolbox, the only socketed component being the programme EPROM.

RS data

Interface assignment of exerciser.

Table 1 **Signal interface**

Pin number	Function
All odd pins	Ground
2	Head load (normal)
4	Head load (optional)
6	Ready (Euro & some US)
8	Index pulse
10	Drive select Ø
12	Drive select 1
14	(drive select 2 not used on RS Exerciser)
16	Motor on
18	Direction. (low = step in)
20	Step pulse
22	Write data
24	Write enable
26	Track 00
28	Write protected
30	Raw read data
32	Side select
34	Ready (Japan, some US & Euro)

Table 2 **Power interface**

Pin number	Function
1	+12V
2	12V supply ground.
3	5V supply ground.
4	+5V

Interface assignment of 8in drive adaptor pod

Table 3 **8in drive interface assignment**
The lines which are most commonly found to come out at standard positions are as follows:

RS Exerciser pin no.	8in drive pin no.	Function
All odds pins	All odd pins	Ground
2	18	Head load
6	22	Ready
8	20	Index
10	26 &	Drive select
–	30	Drive select 2
12	28 &	Drive select 1
–	32	Drive select 3
14	–	(Not used on RS Exerciser)
16	2 &	Low write current (TK 43)
–	8	Low write current (TK 43)
18	34	Direction (low = step in)
20	36	Step pulse
22	38	Write data
24	40	Write enable
26	42	Track 00
28	44	Write protected
30	46	Raw read data
32	14	Side select

Table 4 **Single and double sided exceptions**
There are other pins which can change their function depending on whether the drive is single or double sided.

RS Exerciser pin no.	8in drive pin no.	Function
4	16	Low write current or doorlock or drive select led
32	14	On single sided, may be used to activate the erase head so if asserted, can crash CE discs
34	10	Not used on single sided. On double sided, indicates when a double sided disc is loaded
–	6	Not used on single sided. On double sided, may sometimes be used to activate the erase head

8in drive adaptor pod

Comprehensive instruction manual
The Exerciser is supplied with a comprehensive instruction manual with a chapter on each of the following.

1. Basics
2. Write amplifier checks
3. Drive alignment and cleaning
4. Catastrophic drive failures
5. CE disc types
6. Interface assignment
7. Using the exerciser with 8in drives
8. Drive problems
9. CE discs for 8in drives
10. Power for 8in drives
11. Using the exerciser with 3½in drives.

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RS data

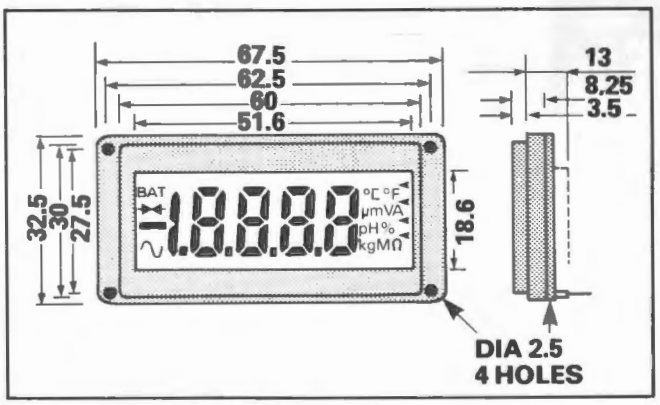
Single rail supply LCD 4½ digit DVM module

Stock number 267-571

A very low profile, 4½ digit dvm module, especially designed for single rail power supply working. This enables the power supply 0V to be connected to the signal 0V, and allows a flexibility in system design not usually associated with this style of module. The 4½ digit clear liquid crystal display is further enhanced by an extensive set of of user-selectable legends as shown. A particularly useful feature is the use of solder pads on the module rear that allow easy linking of connections to bring up the desired legends on the display. All the usual features such as auto-zero, auto-polarity, overrange indication and low battery indicator are present, as well as a digitally controlled range change and a display hold facility. Digit height is 13mm (0.5in). Maximum display is 19999, giving an effective 'full scale deflection' of 200mV (or 2V using the range change). Accuracy is 0.01% of input ±1 count. Current consumption is typically 1mA. An internal bandgap reference assures excellent stability of the reading.

Features

- System flexibility – module 'ground' can be Signal 'ground' as well
- Extensive set of display annunciators
- Auto-zero
- Auto-polarity
- Overrange and low battery indications
- Instant continuity indicator
- 13mm (0.5in) digit height
- 199.99mV basic fsd
- Bandgap reference for stability.



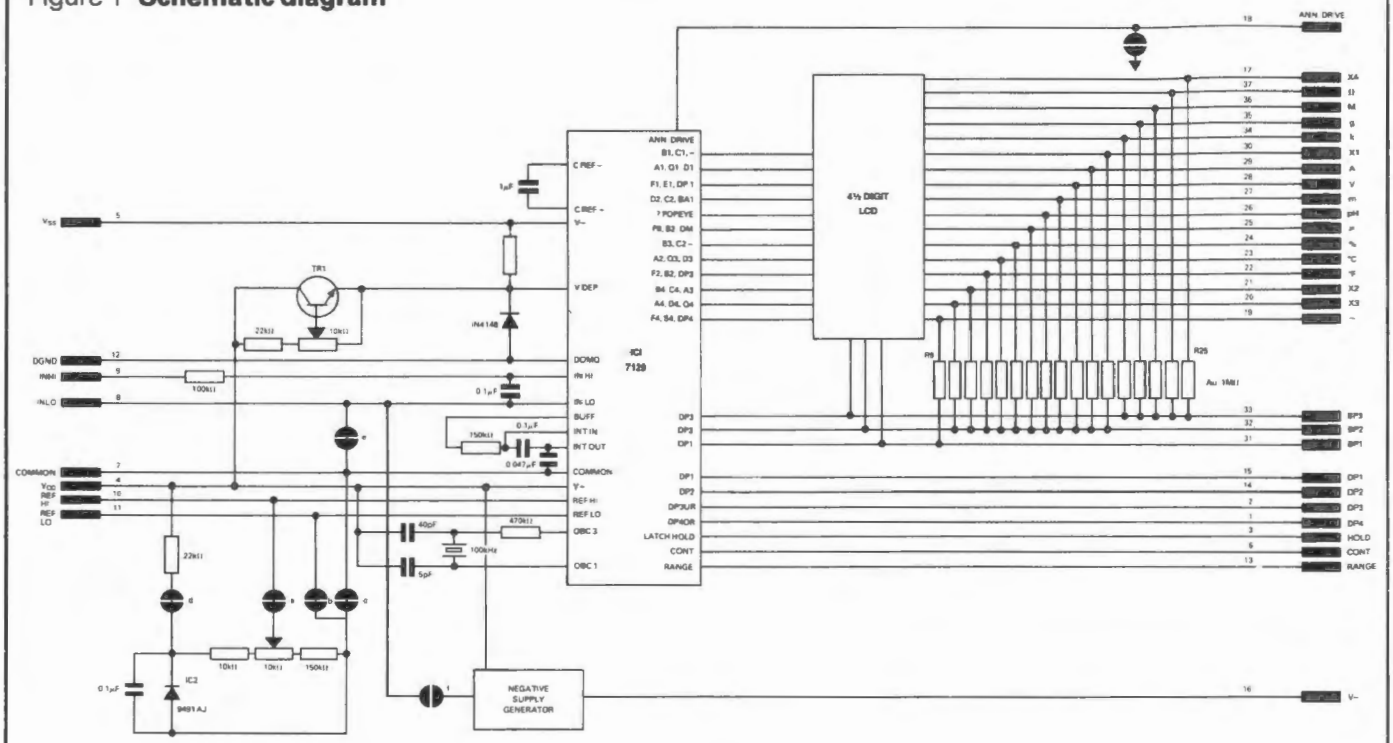
Electrical characteristics $T_A = 25°C$

Parameter		Value (typical)
Power supply voltage,	Conventional connection	9V dc nominal (6-15V)
	Single ended mode	5V dc nominal (3-7.5V)
Supply current (excluding common current)		1mA
Display resolution		19999, 1 count = 10µV
Input impedance (see Note 1)		> 1000MΩ
Error		0.01% of input ± 1 count
Range temperature coefficient		50ppm/°C
Input leakage current		1pA
Common mode rejection ratio		110dB
Sample rate		1.6/sec

Operating temperature 0°C to +50°C
Storage temperature –20°C to +60°C

Note 1 Operation under many practical conditions is facilitated by connection of a 10MΩ resistor across the input.

Figure 1 **Schematic diagram**



Note: Pad f **must** be linked for single ended operation.

Circuit notes

The module incorporates a dual slope integration analogue-to-digital converter which consumes typically 1mA from the power supply.

The converter functions ratiometrically and has fully differential analogue signal and reference inputs.

An RC network provides signal input filtering and overload protection.

Internally, the converter operates with 200mV full scale, although a multiturn trimmer is provided to facilitate display adjustment for individual sensor scaling. For larger changes in scaling, input voltage attentuators or current shunts may easily be added to the module (see Figure 2). A high stability bandgap voltage reference i.c. produces 1V reference, or an external voltage may be applied to the reference input. The display reading = (signal input/reference input)
x 10000. A 10:1 range changing input allows for a range change to 2V full scale with digital control.

Standard features include auto-zero circuitry, automatic polarity, and overrange indication of '1' displayed in the most significant digit position and the remaining digits blanked. Correct auto-zero operation is facilitated by connection of a 10M resistor across the input terminals. The auto-polarity circuitry functions at zero signal voltage for precise null detection.

A crystal oscillator provides a reading rate of approximately 1.6 per second.

Low battery detection circuitry provides advance warning of battery failure directly on the display.

A continuity function is incorporated, with automatic visual indication, and a logic level output which can be used to generate an audible signal.

The differential analogue inputs may be operated to within 0.5V below the positive supply (V_{DD}) and 1.5V above the negative supply (V_{SS}). A common mode reference point (COM) is provided to enable measurement of signals fully floating with respect to the power supply. The single-ended operation facility removes the restriction with respect to negative supply, which may then be corrected direct to signal low.

Connections

Pin 1 DP4/OVERRANGE. Connect HI to obtain DP4, connect LO if not required. The output will go HI if the display exceeds ±19999.

Pin 2 DP3/UNDERRANGE. Connect HI to obtain DP3, connect LO if not required. The output will go HI if the display is less than ±1000.

Pin 3 LATCH/HOLD. Left floating, the converter operates normally. Connect HI to hold the last displayed reading.

Pin 4 V+ (V_{DD}) Positive power supply.

Pin 5 V– (V_{SS}) Negative power supply.

Pin 6 CONTINUITY. The output will be HI and the continuity indicator (⋈) turned on when the signal is below nominally 200mV. An immediate continuity indication is provided, independent of the converter cycle, and the logic output may be buffered to drive an audible alarm. Connect LO to disable the continuity indication.

Pin 7 COMMON. Internally derived common mode reference point, established approximately 3V below V_{DD}, for use with signals floating with respect to the supply.

Pin 8 IN LO. Analogue signal low input.

Pin 9 IN HI. Analogue signal high input.

Pin 10 REF HI. Reference input.

Pin 11 REF LO. Reference input. Differential reference voltage inputs, against which the signal input is compared and displayed ratiometrically. The reference inputs are internally connected to the high stability bandgap voltage source. If an external reference is to be applied, pads (a) and (b) should be split to isolate the bandgap before the external reference is applied.

Pin 12 DIGITAL GROUND. The voltage between V_{DD} and DGND is the internal supply voltage for the module logic circuits. External logic circuits may be similarly powered up to a maximum of 1mA.

Pin 13 RANGE. Incorporates internal 3μA pull down, need not be connected if 200mV range required. Connect HI for 2V range.

Pin 14 DP2.

Pin 15 DP1. Incorporates internal 3μA pull down, need not be connected if the decimal point indications are not required. Correct HI if the decimal point is required.

Pin 16 V–. Connect to pin 5 for single ended operation.

Pin 18 Annunciator Drive. Connect to required annunciator(s) via solder pads or terminal pins.

Pins17-37 Annunciators.

Solder pad functions

a connects internal bandgap reference voltage to REF IN

b connects internal bandgap reference common to REF LO

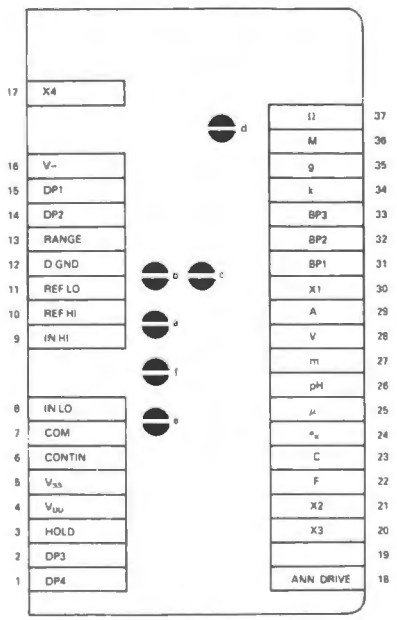
c connects internal bandgap reference common to COM

d connects internal bandgap reference circuit to V_{DD}

e connects analogue signal input low to COM

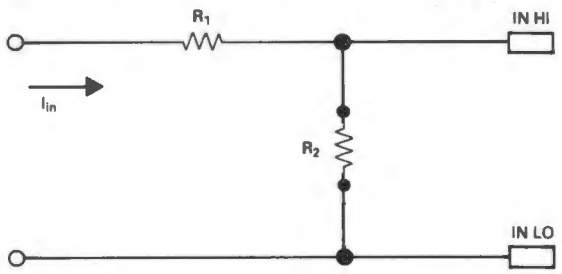
f connects internal negative voltage generator to INLO (for single ended operation).

Figure 2 **PCB pin connection diagram**



Alternative full scale reading

Figure 3 **Alternative full scale reading**

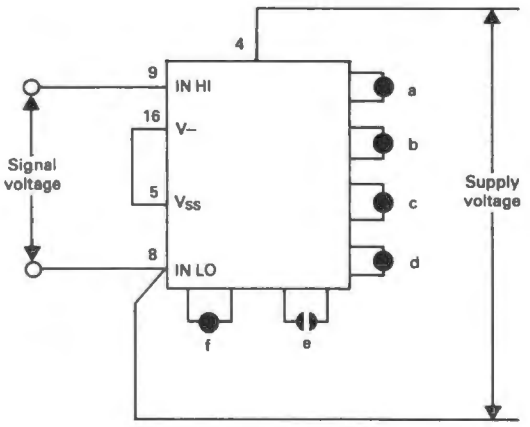


Voltage attenuator or current shunt components may be used as shown to alter the full scale reading (10MΩ resistor may be used for R_1 with adjustment of trimmer provided).

Full Scale	'RANGE' input	R1	R2
200mV	LO (o/c)	(o/c)	(o/c)
2V	HI	(o/c)	(o/c)
20V	HI	9M	1M
200V	HI	9M9	100K
2000V	HI	9M99	10K
200μA	LO (o/c)	(s/c)	1K
2mA	LO (o/c)	(s/c)	100R
20mA	LO (o/c)	(s/c)	10R
200mA	LO (o/c)	(s/c)	1R

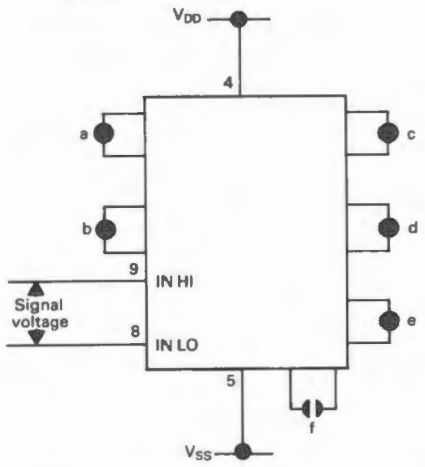
Applications

Figure 4 **Measurement of single-ended inputs**



RS data

Figure 5 **Measurement of floating voltage with 200mV full scale**



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RS data

Electronic motor protection relay and accessories

Stock numbers 345-448, 346-255, 346-261, 346-277, 346-283, 346-299

A solid-state overload, stall current and phase failure protection relay designed for use on three phase ac supply systems. Line currents are monitored by means of separately mounted current transformers. In addition to the precise setting of minimum overload, the tripping time and the delay before permissible reset time is also adjustable. The relay incorporates an optional phase failure trip which is fast in operation and is independent of the overload trip settings.

These additional features are not normally available on conventional bi-metallic (thermal) or solenoid overload devices.

The need for such a product

When a large motor burns out, the cost of repair or replacement, besides the dismantling and re-installation, is high.

Even with small motors, their application may warrant a greater degree of protection. An industrial process may be involved which, if interrupted, would result in spoilage or costly 'down time'.

An improved degree of protection is also needed for maximum continuous rated (MCR) and Ex-e motors.

A means of delaying restart after an overload condition is also a requirement.

Indiscriminate repeated starting, or attempts to start a stalled motor is considered to be the biggest cause of electrical failures, whether directly due to overheating or as a result of the mechanical stresses set up in the machine. A severe example is where a motor is working in high ambient temperatures, eg. near a furnace, hot pipe etc., the motor may not cool down, after an overload trip, as quickly as the overload relay. The motor is re-started causing further overheating until eventual burn out.

In applications where long run-up times are experienced, delayed tripping is called for.

Heavy duty starts may cause a conventional overload relay to trip out before the run-up time has expired. It is not good practise to increase the trip current to a level which will prevent this 'nuisance' tripping since this may be well above the rated motor current, thus reducing motor protection.

The RS three phase, electronic motor protection relay is designed to cater for these needs.

Features

- Precise setting to minimum overload, aided by LED indication, to match actual load conditions
- Constant repeatability (no thermal drift)
- Tripping time based on I^2 which gives an inverse time characteristic and approximates to the thermal behaviour of the load
- Delay before permissible reset adjustable 2-20 minutes
- Tripping time adjustable (up to 40 seconds at 6 x flc) to take into account slow run-up times but can be set as low as 2.5 seconds
- Rapid phase failure tripping feature independent of overload current and time settings. Approximate tripping time is 2 seconds
- Phase failure tripping feature optional. A facility to link-out this protection is incorporated. This may be necessary on unbalanced loads or where the sinusoidal waveform of the motor current is deliberately distorted (eg. soft start systems) causing unwanted tripping
- Hand reset (remote pushbutton) or auto reset (by wire link)
- Full load current (f.l.c.) range from 0.65A to 2 times nominal current transformer rating (see selection chart)
- Electrically separate N/O and N/C output contacts allow for indication of state of relay
- Choice of mounting location allowing relay to be sited with other control equipment on DIN rail, eg. not necessary to mount adjacent to current transformers.

Basic relay (345-448)

The electronic overload relay is mounted in a moulded enclosure and has three customer adjustable settings – trip current, trip delay and reset delay. A LED trip indicator is mounted on the top face. A test button is also provided.

Adjustments

Trip current setting can be pre-set over a nominal range of 70% to 200% of current transformer rating.

Trip delay on overload can be adjusted over a range of approximately 20:1 (refer to trip curves).

Reset delay time selection from a nominal range of 2 to 20 minutes.

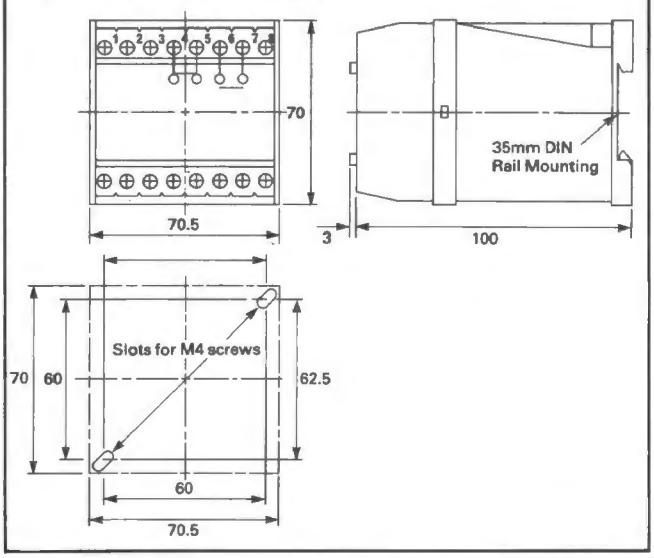
Test pushbutton simulates approximately 8 x f.l.c. for manual check of performance.

Hand reset (remote push button) or auto (by wire link). For safety reasons this reset adjustment will not override either the trip or reset delay functions.

Cable terminations (max cable size 2.5mm^2)
16 terminals are utilised in the following manner:

Terminal numbers	Function
6 & 7	N/O output contact rated 1A (AC11) at 240V ac
4 & 5	N/C output contact rated 1A (AC11) at 240V ac
	Relay energises when supply applied and unit reset
3 & 2 (N)	Supply 240V 50/60Hz (line to neutral)
14, 15 & 16	Input from current transformers 25mA secondary winding
12 & 13	Remote reset (or link if auto reset is required)
1	Single phase trip link-out when connected to 12.

Figure 1 **Relay dimensions**



Voltage dropper (346-255)

A series wired unit for use with 240V relay on 415V supply.

Power consumption 0.6W.

Figure 2 **Voltage dropper circuit**

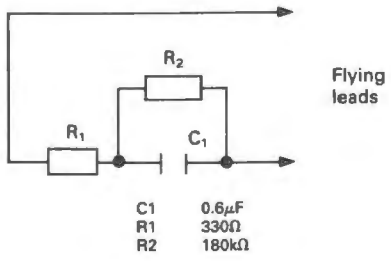
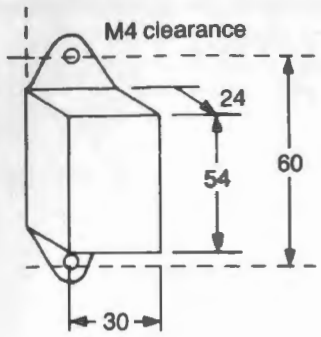


Figure 3 **Voltage dropper dimensions**



Current transformers

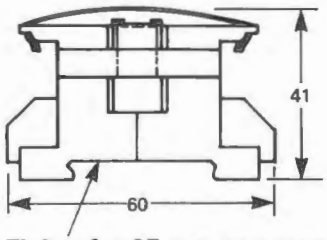
A range of current transformers with a 25mA secondary winding, saturating at about 10 x flc. Specially designed for use with the Electronic Motor Protection Relay. The types available from RS are as follows:

Primary/secondary	Stock No.
1A/25mA	346-261
20A/25mA	346-277
50A/25mA	346-283
100A/25mA	346-299

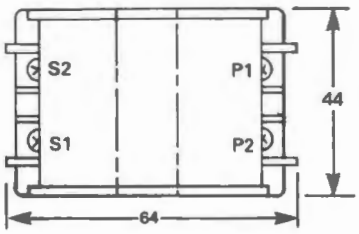
These current transformers are supplied in pairs which is normally sufficient for monitoring three wire connected loads. Three current transformers are essential for four wire connected loads and recommended when current transformers are to be connected in the phases of a delta connected motor (see current transformer selection chart on page 7).

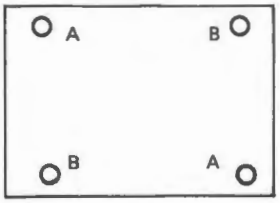
Figure 4 **Current transformer dimensions**

Type 1A/25mA (346-261)



Fixing for 35mm symmetric DIN rail

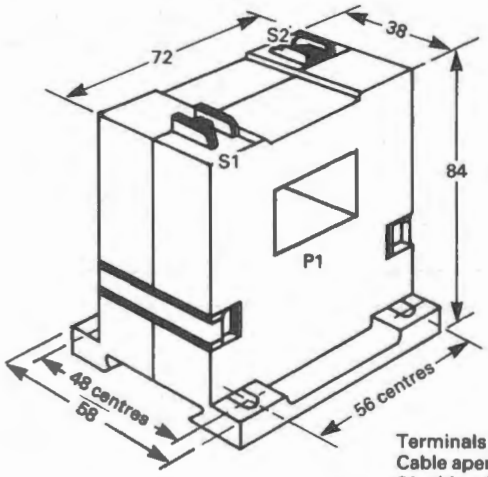




Drill Plan
Normal fixing (holes A)
50mm horizontal
35mm vertical
Alternative fixing (holes B)
48mm horizontal
34mm vertical

Figure 5 **Current transformer dimensions**

Types 20A/25mA (346-277), 50A/25mA (346-283) and 100A/25mA (346-299)



Terminals M3.5
Cable aperture
21 wide x 26 high.
Fixing slots 5.5 wide

Fixing for standard 35mm symmetrical DIN rail (EN 50 022) RS Stock No. 424-131

Installation

The basic relay should be mounted onto a vertical and flat surface free from significant vibrations. The unit may be clipped onto 35mm symmetric DIN rail to BS5584:1978 (EN 50 022) top hat profile.

The two wire controls for remote push-button reset, should be twisted for up to 3 metres but for longer runs it is recommended that the wires should be screened.

The current transformers should be wired up as shown in the appropriate diagram under 'typical circuit configurations' however the phase conductors may need to pass through the current transformers several times in order to obtain the desired secondary current for the relay (see current transformer selection chart).

Operation

The measured current from the current transformers is rectified by the basic relay and the resultant output is used to determine:

a) If the current setting is being exceeded. This being the case, then the unit will trip out in accordance with the trip time setting and the percentage overload (see typical trip curves).

b)* If the ripple frequency is correct. This frequency alters when a phase is lost. The sensing circuit detects this difference and causes the unit to trip out in approximately 2 seconds.

Resetting the relay, either by remote pushbutton or automatically when a link is in circuit, can only occur after the preset delay period.

The relay is energised in the 'healthy' condition and will fail safe, tripping on the loss of unit supply. There is a short delay (approx. ½ second) before contacts attain the 'healthy'' position on initial application of supply to the unit.

* Not applicable when linked out.

5948

Specification

Operating voltage ____ 240V 50Hz
or 415V 50Hz
by means of external voltage dropper

Tolerance (basic relay) ____ –25% + 10%

Consumption (operating voltage) ____ 12.5Va

Relay output ____ two separate contacts electrically isolated 1N/O and 1N/C rated 1A (AC11) at 240V ac

Maximum working ambient temperature around unit ____ –25°C to +60°C

Storage temperature ____ –25°C to +85°C

Phase failure trip ____ Tripping will occur when a phase loss occurs at currents greater than 0.65 nominal CT rating

Current setting ____ 70% to 200% nominal CT rating

Trip delay ____ adjustable 2.5 to 40 seconds (time to trip at 8 x flc) and approximates to current squared

Time to reset ____ adjustable 2 to 20 minutes
Overload will not reset during this period.

Setting up

1. Initial setting up of unit.
   Two alternative methods are possible, the first of which should prove to be the most accurate.
   a) With both current and trip delay settings at maximum, start motor in normal manner. Reduce current settings until LED on unit is illuminated then increase setting until LED is extinguished – unit is now correctly set and will go into overload mode (ie. LED illuminated) if current increases by approx. 10%. Trip delay setting and reset time setting should now be adjusted to 'desired values'.

      'Desired value' of trip delay should be just sufficient for motor to run up to speed on maximum load, ie. a high inertia load will usually require a higher setting than a low inertia load.

      'Desired value' of reset time should be sufficient to allow motor to cool down prior to restart; ie. a large motor will usually require a longer cooling time than a small motor.

      N.B. This method can only be used if the motor can be run on max. load (even if this does not correspond to max flc). If motor cannot be fully loaded and is to trip only when current exceeds rated flc then use method b.

   b) The current setting potentiometer is scaled as percentage of nominal CT rating. Actual setting can therefore be estimated by means of the following calculation or by reference to the CT selection table.

      ie.
      $$\frac{(100 \times \text{flc})}{\text{Nominal CT rating}}$$

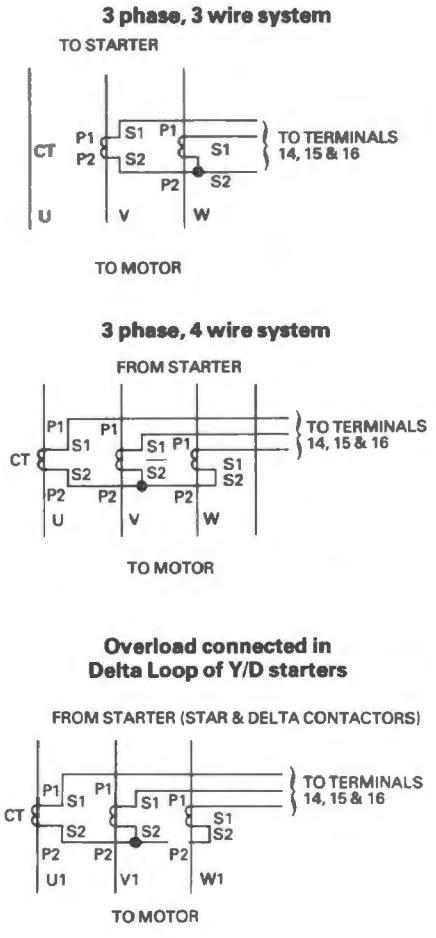
      Trip delay and reset time setting should then be adjusted to desired values.

2. After setting up unit, the stalled motor trip delay can be checked by means of the Trip Test button. This will give the approximate delay available for both 'hot' and 'cold' conditions.

Note. Current setting is nominal, tripping cycle will start when current attains approx 1.1 x current setting.

Current measurement

Figure 6 **Current measurement**



NOTE: Common point of CTs MUST NOT be earthed

Typical control circuit configurations

Figure 7 **L-N control, DOL starter, 240V coil**

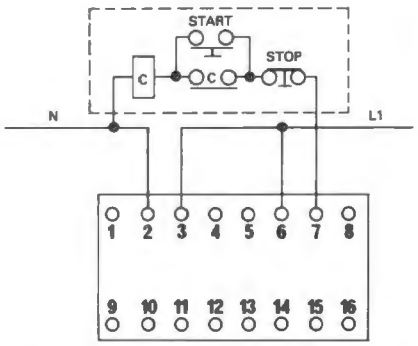


Figure 8 **L-N control, DOL starter, 415V coil**

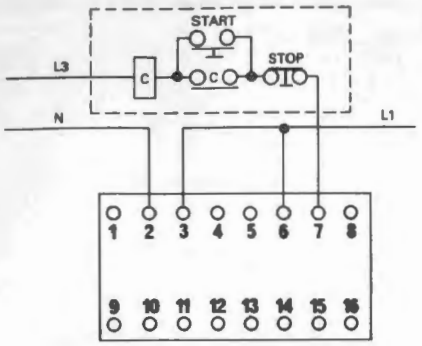
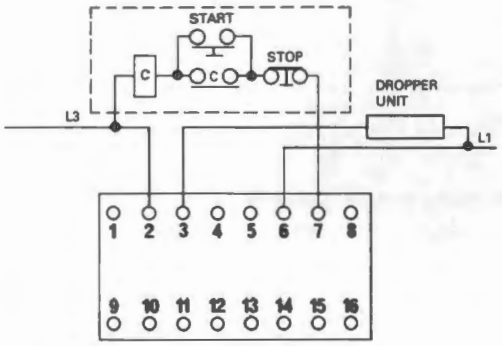


Figure 9 **L-L control, DOL starter, 415V coil**



Reset arrangement

Figure 10 **Manual reset**

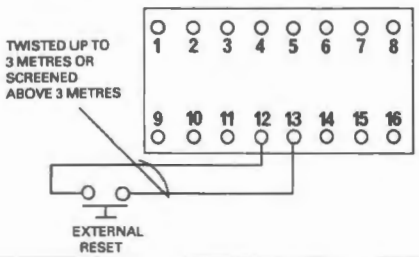
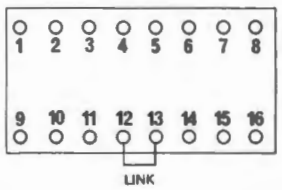
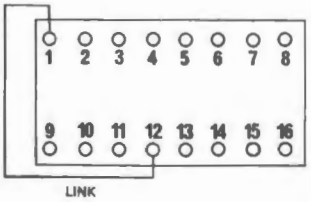


Figure 11 **Auto reset**

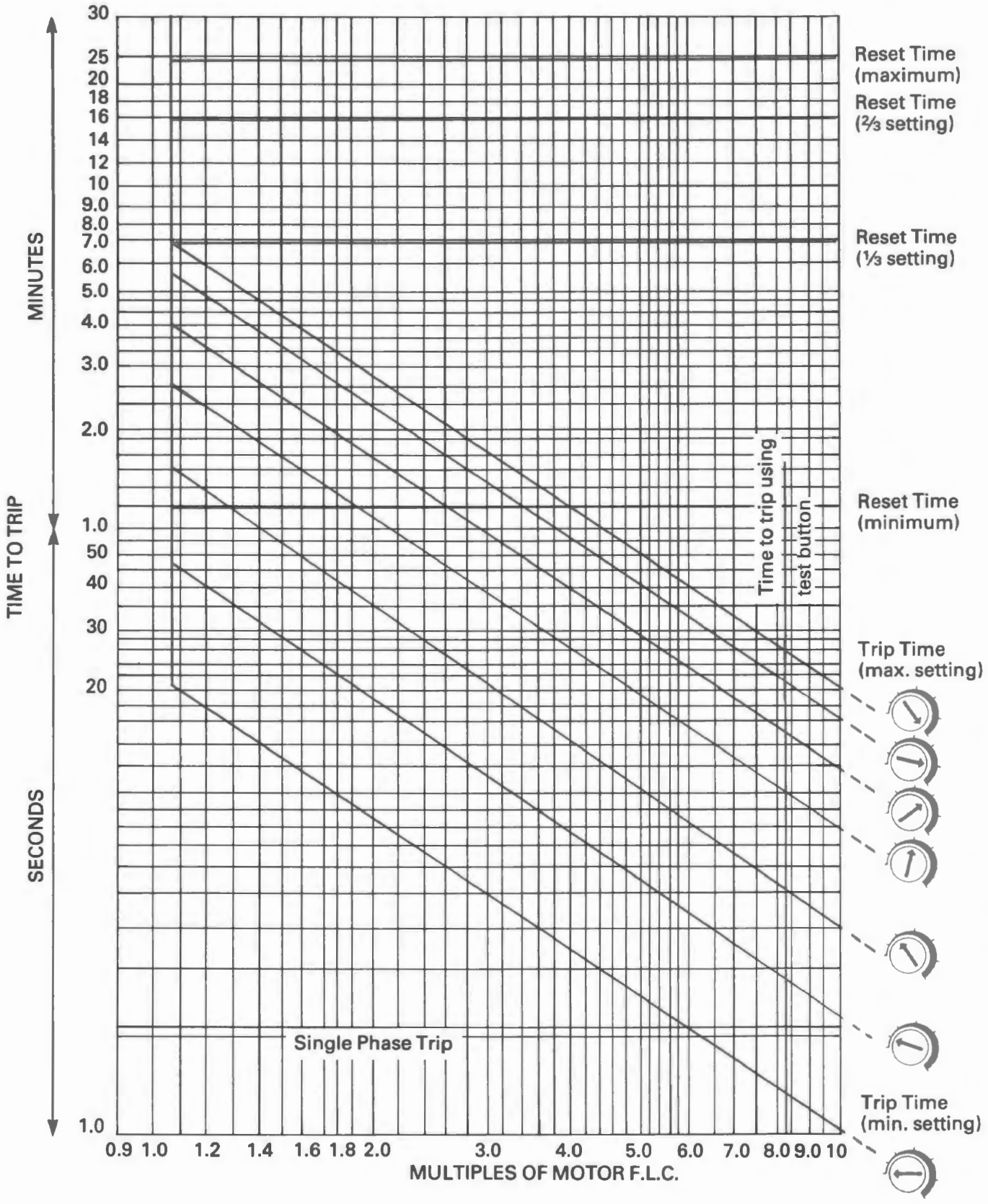


Phase failure trip link out

Figure 12 **Phase failure link out connections**



Typical trip curves



Current transformer selection chart

Motor flc (amps)	Connected in supply lines		Setting range[2]						
	CT	Turns through CT	70%	85%	100%	125%	150%	175%	200%
			Current setting % of CT rating						
0.7 to 1.6	1 amp/25mA (346-261)		.7	.85	1.0	1.25	1.5	1.75	2.0
1.7 to 3.5	20 amp/25mA (346-277)	10	1.4	1.7	2.0	2.5	3.0	3.5	4.0
3.6 to 5.4		5	2.8	3.4	4.0	5.0	6.0	7.0	8.0
5.5 to 8.5		4	3.5	4.25	5.0	6.25	7.5	8.75	10.0
8.6 to 17.5		2	7.0	8.5	10.0	12.5	15.0	17.5	20.0
17.6 to 29.2		1	14.0	17.0	20.0	25.0	30.0	35.0	40.0
29.3 to 42.8	50 amp/25mA (346-283)	2	17.5	21.25	25.0	31.3	37.5	43.8	50.0
42.9 to 87		1	35.0	42.5	50.0	62.5	75.0	87.5	100.0
87.1 to 180	100 amp/25mA (346-299)	1	70.0	85.0	100.0	125.0	150.0	175.0	200.0
180.1 to 257	200 amp/1 amp + 1 amp/25mA or 200 amp/5 amp + 4 turns through 20 amp/25mA	1 through Main CT Direct conn. Secondary CT	140.0	170.0	200.0	250.0	300.0	350.0	400.0
		1 through Main CT 4 through Secondary C T	140.0	170.0	200.0	250.0	300.0	350.0	400.0
257.1 to 350	300 amp/1 amp + 1 amp/25mA or 300 amp/5 amp + 4 turns through 20 amp/25mA	1 through Main CT Direct conn. Secondary CTR	210.0	255.0	300.0	375.0	450.0	525.0	600.0
		1 through Main CT 4 through Secondary CT	210.0	255.0	300.0	375.0	450.0	525.0	600.0
350.1 to 450	400 amp/1 amp + 1 amp/25mA or 400 amp/5 amp + 4 turns through 20 amp/25mA	1 through Main CT Direct conn. Secondary CT	280.0	340.0	400.0	500.0	600.0	700.0	800.0
		1 through Main CT 4 through Secondary CT	280.0	340.0	400.0	500.0	600.0	700.0	800.0
450.1 to 550	500 amp/1 amp + 1 amp/25mA or 500 amp/1 amp + 4 turns through 20 amp/24mA	1 through Main CT Direct conn. Secondary CT	350.0	425.0	500.0	625.0	750.0	875.0	1000.0
		1 through Main CT 4 through Secondary CT	350.0	425.0	500.0	625.0	750.0	875.0	1000.0

For connection in phases of YD starters see Page 8.

RS data

Motor flc (amps)	Connected in phases of Y D starters[1]		Setting range[2]						
	CT	Turns Through CT	70%	85%	100%	125%	150%	175%	200%
			Current setting % of CT rating						
1.21 to 3.1	1 amp/25mA (346-261)		1.21	1.47	1.73	2.17	2.6	3.0	3.46
3.2 to 5.4	20 amp/25mA (346-277)	10	2.42	2.94	3.46	4.33	5.2	6.06	6.93
5.5 to 8.5		5	4.85	5.88	6.92	8.66	10.4	12.1	13.8
8.6 to 15.7		4	6.06	7.36	8.66	10.83	13.0	15.2	17.3
15.8 to 29.2		2	12.1	14.7	17.3	21.7	26.0	30.3	34.6
29.3 to 54.3		1	24.2	29.4	34.6	43.3	52.0	60.6	69.3
54.4 to 74.2	50 amp/25mA (346-283)	2	30.3	36.8	43.3	54.1	65.0	75.8	86.6
74.3 to 160		1	60.6	73.6	86.6	108.3	130.0	152.0	173.0
160.1 to 307	100 amp/25mA (346-299)	1	121.0	147.0	173.0	217.0	260.0	303.0	346.0
307.1 to 450	200 amp/1 amp + 1 amp/25mA or 200 amp/1 amp + 4 turns through 20 amp/25mA	1 through Main CT Direct conn. Secondary CT	242.0	294.0	346.0	433.0	520.0	606.0	693.0
		1 through Main CT 4 through Secondary CT	242.0	294.0	346.0	433.0	520.0	606.0	693.0
450.1 to 550	300 amp/1 amp + 1 amp/25mA or 300 amp/5 amp + 4 turns through 20 amp/25mA	1 through Main CT Direct conn. Secondary CT	364.0	442.0	520.0	650.0	780.0	910.0	1040.0
		1 through Main CT 4 through Secondary CT	364.0	442.0	520.0	650.0	780.0	910.0	1040.0

1) It is recommended that 3 CXTs are used for this application – ie. 1 in each phase.

2) These figures are only applicable if main CT is linear up to twice nominal rating.

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RS data

LinCMOS™ programmable op-amp RS251

Stock number 630-522

The RS251 is a low minimum supply voltage, low power, programmable op-amp designed to operate on single or dual supplies. Unlike traditional metal gate CMOS op-amps, this device utilises the silicon gate LinCMOS™ process, giving it a stable input offset voltage without sacrificing the advantages of metal gate CMOS.

Featuring a 1 volt minimum supply voltage, a typical input common-mode range that extends to the negative rail and extremely low power consumption this op-amp is ideally suited for battery powered or energy conserving applications.

A bias pin can be used to select one of three ac performance and power dissipation levels and no frequency compensation is required down to unity gain.

Absolute maximum ratings

Supply voltage, V_{DD} (see Note 1) 18V
Differential input voltage (see Note 2) ..... ±18V
Input voltage range, any input (exceeding this parameter can cause latchup or permanent damage) (see text) ..... –0.3V to 18V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) ..... Unlimited
Continuous total dissipation at (or below) 25°C free air temperature (see Note 4) 1000mW
Operating free-air temperature range ..... 0°C to +70°C
Storage temperature range ..... –65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from the case for 10 seconds ..... 260°C

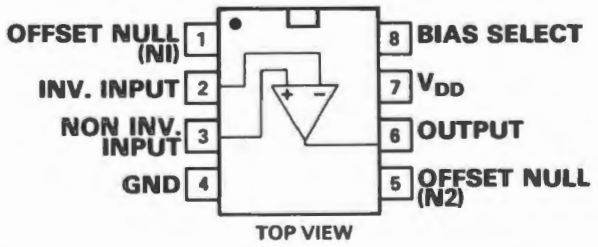
Notes:

1. All voltage values, except differential voltages, are with respect to network ground terminals.
2. Differential voltages are at the non-inverting input terminal with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
4. For operation above 25°C derate at 8mW/°C.

Features

- Wide range of supply voltages: 1V to 16V
- True single supply operation
- Common-mode input voltage range includes the negative rail
- Selectable supply current:
  Low = 10μA Typ
  Medium = 150μA Typ
  High = 1000μA Typ
- Extremely low input bias and offset currents:
  I_{IB} 1pA Typ
  I_{IO} 1pA Typ
- Ultra stable input offset voltage:
  0.1μV/Month Typ
  0.7μV/°C Typ (low bias)
- Low noise 30nV √Hz Typ at 1kHz (high bias)
- High slew rate:
  High bias 4.5V/μs Typ
  Medium bias 0.6V/μs Typ
  Low bias 0.04V/μs Typ

Pin connections



TOP VIEW

ATTENTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

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Recommended operating conditions

Parameter		Min.	Max.	Unit
Supply voltage, V_{DD}		1	16	V
Common-mode input voltage V_{IC}	V_{DD} = 1V	0	0.2	V
	V_{DD} = 4V	0	3	
	V_{DD} = 10V	–0.2	9	
	V_{DD} = 16V	–0.2	14	
Operating free-air temperature T_A		0	70	°C
Bias select pin voltage		See application notes		

Electrical characteristics at specified free-air temperature, V_{DD} = 10V (unless otherwise specified)

Parameter		Test conditions†		Bias	Min.	Typ.	Max.	Unit
V_{IO}	Input offset voltage	V_O = 1.4V, R_S = 50Ω	25°C	Any		10		mV
$\propto V_{IO}$	Average temperature coefficient of input offset voltage		Full range	Low		0.7		μV/°C
				Medium		2		
				High		5		
I_{IO}	Input offset current	V_{IC} = 5V, V_O = 5V	25°C	Any		1		pA
			Full range				100	
I_{IB}	Input bias current	V_{IC} = 5V, V_O = 5V	25°C	Any		1		pA
			Full range				150	
V_{ICR}	Common-mode input voltage range		25°C	Any	–0.2 to 9			V
V_{OM}	Peak output voltage range‡	V_{ID} = 100mV	25°C	Any	8	8.6		V
			Full range		7.8			
A_{VD}	Large-signal differential voltage amplification	V_O = 1 to 6V, R_S = 50Ω	25°C	Low	30	500		V/mV
				Medium	20	280		
				High	10	40		
			Full range	Low	25	500		
				Medium	15	280		
				High	7.5	40		
CMRR	Common-mode rejection ratio	V_O = 1.4V, V_{IC} = V_{ICR}^{min}	25°C	Any	70	88		dB
k_{SVR}	Supply voltage rejection ration ($\Delta V_{CC}/\Delta V_{IO}$)	V_{DD} = 5 to 10V, V_O = 1.4V	25°C	Low	70	85		dB
				Medium	70	85		
				High	65	82		
I_{OS}	Short-circuit output current	V_O = 0, V_{ID} = 100mV	25°C	Any		–55		mA
		V_O = 0, V_{ID} = –100mv				15		
$I_{IH(SEL)}$	High-level input current to bias select	$V_{I(SEL)}$ = 0V	25°C	High		10.5		μA
$I_{IL(SEL)}$	Low-level input current to bias select	$V_{I(SEL)}$ = 10V	25°C	Low		1.3		μA
I_{DD}	Supply current	No load, V_O = 5V, V_{IC} = 5V	25°C	Low		10	20	μA
				Medium		150	300	
				High		1000	2000	
			Full range	Low			30	
				Medium			400	
				High			2200	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is 0°C to 70°C. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ for medium bias R_L = 100kΩ, and for high bias R_L = 10kΩ.

‡ The output will swing to the potential of the ground pin.

Electrical characteristics at specified free-air temperature, V_{DD} = 1V

Parameter		Test conditions†		Bias	Min.	Typ.	Max.	Unit
V_{IO}	Input offset voltage	V_O = 0.2V, R_S = 50Ω	25°C	Any			10	mV
			0°C to 70°C				12	
$\propto V_{IO}$	Average temperature coefficient of input offset voltage		0°C to 70°C	Any		1		μV/°C
I_{IO}	Input offset current	V_O = 0.2V	25°C	Any		1		pA
			0°C to 70°C				100	
I_{IB}	Input bias current	V_O = 0.2V	25°C	Any		1		pA
			0°C to 70°C				150	
V_{ICR}	Common-mode input voltage range		25°C	Any	0 to 0.2			V
V_{OM}	Peak output voltage swing‡	V_{ID} = 100mV	25°C	Any		450		mV
A_{VD}	Large-signal differential voltage amplification	V_O = 100 to 300mV, R_S = 50Ω	25°C	Low		20		V/mV
				High		10		
CMRR	Common-mode rejection ratio	R_S = 50Ω, V_O = 0.2V, $V_{IC} = V_{ICR\ min}$	25°C	Any		77		dB
I_{DD}	Supply current	V_O = 5V, V_{IC} = 5V, No load	25°C	Low		2		μA
				High		12		

† All characters are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1MΩ, for medium bias R_L = 100kΩ, and for high bias RL = 10kΩ.

‡ The output will swing to the potential of the ground pin.

Operating characteristics V_{DD} = 1V, T_A = 25°C

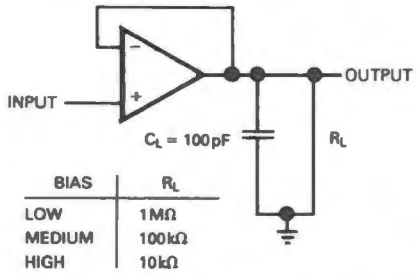
Parameter		Test conditions	Bias	Min.	Typ.	Max.	Unit
B_1	Unity-gain bandwidth	C_L = 10pF	Low		12		kHz
			High		75		
SR	Slew rate at unity gain	See Figure 1	Low		0.001		V/μs
			High		0.01		
	Overshoot factor	See Figure 1	Low		35		%
			High		35		

Operating characteristics V_{DD} = 10V, T_A = 25°C

Parameter		Test conditions	Bias	Min.	Typ.	Max.	Unit
B_1	Unity-gain bandwidth	A_V = 40dB, C_L = 10pF	Low		0.1		MHz
			Medium		0.7		
			High		2.3		
SR	Slew rate at unity gain	See Figure 1	Low		0.04		V/μs
			Medium		0.6		
			High		4.5		
	Overshoot factor	See Figure 1	Low		30		%
			Medium		35		
			High		35		
$Ø_m$	Phase margin at unity gain	A_V = 40dB, R_S = 100Ω, C_L = 10pF	Low		43°		
			Medium		43°		
			High		50°		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 100Ω	Low		70		nV√Hz
			Medium		38		
			High		30		

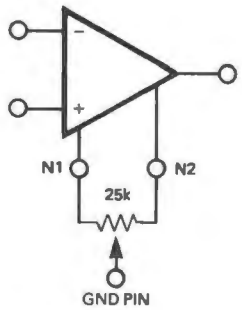
Test circuits

Figure 1 **Unity gain amplifier**



BIAS	R_L
LOW	1MΩ
MEDIUM	100kΩ
HIGH	10kΩ

Figure 2 **Input offset voltage null circuit**



Typical characteristic curves

Figure 3 **Supply current vs bias select pin voltage**

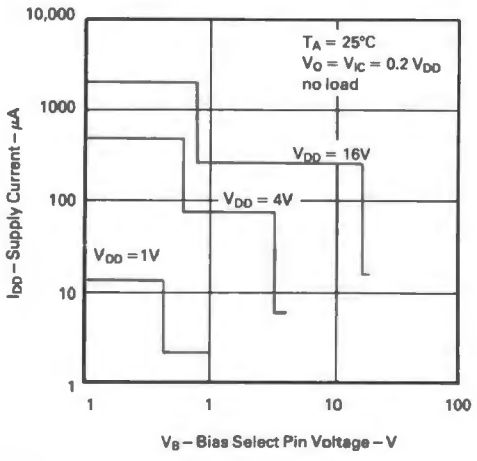


Figure 4 **Supply current vs supply voltage**

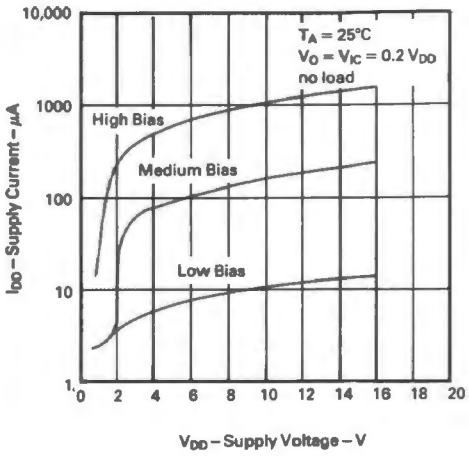


Figure 5 **Supply current vs free air temperature**

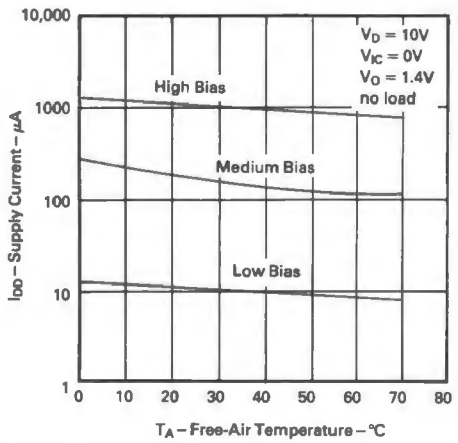


Figure 6 **Low bias, large signal, differential voltage amplification and phase shift vs frequency**

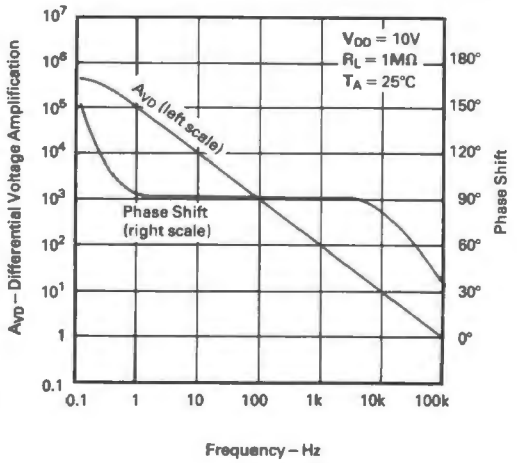


Figure 7 **Medium bias, large signal, differential voltage amplification and phase shift vs frequency**

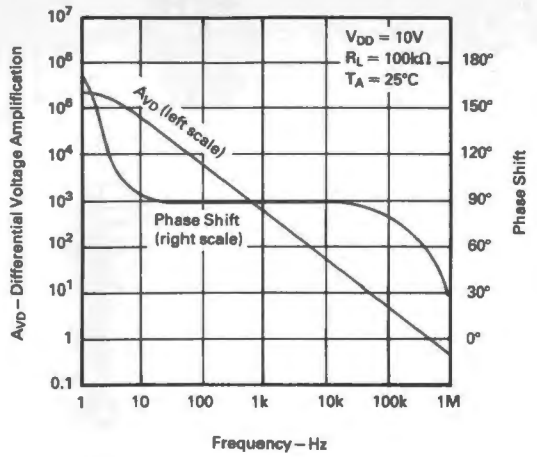
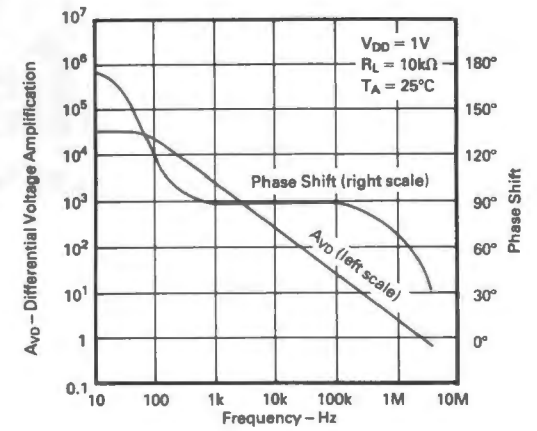


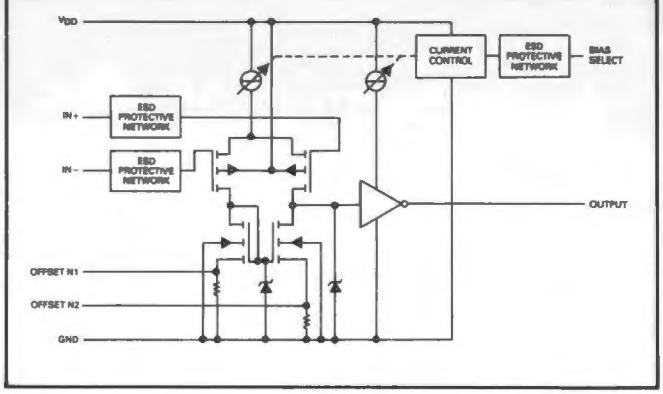
Figure 8 **High bias, large signal, differential voltage amplification and phase shift vs frequency**



Applications information

Because of the extremely high input impedance and low input bias and offset currents, applications for the RS251 include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of this device. Many features associated with bipolar technology are available with this LinCMOS™ operational amplifier without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analogue calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the RS251. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the RS251. In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption. The RS251 is well suited to solve the difficult problems associated with single-battery and solar-cell applications.

Figure 9 **Amplifier schematic**



Static protection

The inputs of the RS251 are protected by series resistors and clamp diodes. As with any integrated circuit, ESD handling precautions should be used to avoid damage from strong electrostatic fields.

Latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, the SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the op-amp supplies should be applied simultaneously with, or before, application of any input signals.

Using the bias select pin

The RS251 has a bias select pin that allows the selection of one of three I_{DD} conditions (10, 150, and 1000μA typical). This allows the user to trade-off power and ac performance. As shown in the typical supply current (I_{DD}) vs supply voltage (V_{DD}) curves (Figure 4), the I_{DD} varies only slightly from 4 to 16V. Below 4V, the I_{DD} varies more significantly. Note that the I_{DD} values in the medium and low-bias modes at V_{DD} = 1V are typically 2μA, and in the high mode are typically 12μA. The following table shows the recommended bias select pin connections at V_{DD} = 10V:

Recommended bias select pin use at V_{DD} = 10v

Bias mode	ac performance	Bias select connection†	Typical I_{DD}§
Low	Low	V_{DD}	10μA
Medium	Medium	0.8V to 9.2V	150μA
High	High	Ground pin	1000μA

† The Bias Select pin may also be controlled by external circuitry to conserve power, etc. For information regarding the bias select pin, see Figure 3 in the typical characteristic curves.

§ For I_{DD} characteristics at voltages other than 10V, see Figure 4 in the typical characteristics curves.

The bias select pin may also be controlled by external circuitry to conserve power, etc. For information regarding the bias select pin, see Figure 3 in the typical characteristics curves.

For I_{DD} characteristics at voltages other than 10V, see Figure 4 in the typical characteristics curves.

Output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD}

selection, and increases with high values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

Input offset nulling
The RS251 offers external offset null control. Nulling may be achieved by adjusting a 25kΩ potentiometer connected between the offset null terminals with the wiper connected to the device GND pin as shown in Figure 2. The amount of nulling range varies with the bias selection. On I_{DD} settings of 150 and 1000μA (medium and high bias), the nulling range will allow the maximum offset specified to be trimmed to zero. In low bias or when the RS251 is used below 4V, total nulling may not be possible on all units.

Supply configurations
Even though the RS251 is characterised for single-supply operation, they can be used effectively in a split-supply configuration when the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

Circuit layout precautions
Please note: whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive leakages.

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RS data

Modem ic 6926 CCITT V21 data format

Stock number 630-976

The 6926 is 300 bit per second single chip modem designed to transmit and receive serial binary data over a switched telephone network using frequency shift keyed (FSK) modulation. CCITT V21 data format allows compatability with equipment operating to this standard. All the necessary modulation, demodulation and filtering to implement a serial, asynchronous communications link are included on-chip.

Absolute maximum ratings

Power supply voltage +12V (V_A) ——— −0.3 to +15V
+5V (V_D) ——— −0.3 to +7V
Analogue input voltage ——— −0.3 to V_A +0.3V
Digital input voltage ——— −0.3 to V_D +0.3V
Storage temperature range ——— −55 to +150°C
Operating temperature range ——— 0 to +70°C

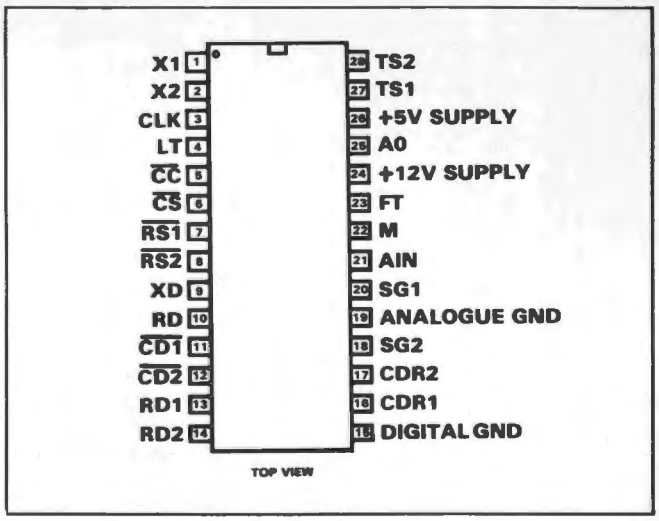
ATTENTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

Features

- CCITT V21 compatible
- Full duplex (2-wire) operation
- Data rate up to 300 b/s
- Originate and answer modes
- Filtering, modulation, demodulation on-chip
- Full DTE interface
- Low power CMOS construction
- TTL compatible digital interface.



Electrical characteristics

dc and digital interface (VA = 12V ±10%, VD = 5V ±5%, T_a = 0 ~ 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Power supply current		IA	Ordinary operation		7.5	15.0	mA
		ID			1.0	2.0	
Input leakage current	*1	I_{IL}	$V_I = 0_V$	−10		10	μA
		I_{IH}	$V_I = V_D$	−10		10	
Input voltage	*1	V_{IL}		0		0.8	V
		V_{IH}		2.2		VD	
Output voltage	*2	V_{OL}	I_{OL} = 1.6mA	0		0.4	V
		V_{OH}	I_{OH} = 400μA	0.8 x VD		VD	

*1	LT, $\overline{CC}$, $\overline{RS1}$, $\overline{RS2}$, XD, $\overline{CD2}$*, RD2, M, FT, T_{S1}, T_{S2}
*2	CLK, $\overline{CS}$, RD, $\overline{CD1}$, $\overline{CD2}$*, RD1

* $\overline{CD2}$ is I/O terminal

Recommended operating conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage Analogue VA +12V Digital VD +5V	VA	With respect to AG	10.8	12.0	13.2	V
	VD	With respect to DG	4.75	5.00	5.25	
	AG, DG			0		
Operating temperature	T_{OP}		0		70	°C
CRYSTAL				3.579545		MHz
R_1		Transformer impedance = 600Ω		600		Ω
R_2				51		kΩ
R_3				51		
R_4				51		
R_5				51		
R_6				51		
R_7				51		
R_8				33		
R_9				51		
C_0, C_1				0.047		μF
C_2				2.2		
C_3			1.0			
C_4			0.01			
C_5				10		
C_6				10		

Application circuits using above conditions are provided in Figure 6.

Analogue interface characteristics

(VA = 12V ±10%, VD = 5V ±5%, T_a = 0 ~ 70°C)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Transmit carrier out (a_O)							
ORIGINATE MODE Carrier frequency	Mark 1	f_{OM}	$f_{CRYSTAL}$ = 3.579545 MHz	974	980	986	Hz
	Space 0	f_{OS}		1174	1180	1186	
ANSWER MODE Carrier frequency	Mark 1	f_{AM}		1644	1650	1656	
	Space 0	f_{AS}		1844	1850	1856	
Output resistance		R_{OXA}				200	Ω
Load resistance		R_{LXA}		50			kΩ
Load capacitance		C_{LXA}				100	pF
Transmit level		V_{OXA}		4	6	8	*1 dBm
Output offset voltage		V_{OSX}		$\frac{VA}{2}-1$	$\frac{VA}{2}$	$\frac{VA}{2}+1$	V
Out-of-band energy (referred to carrier level)		E_{OX}	C_1 = 0.047μF	Refer to Figure 2			dB
Receive carrier input (A_{IN})							
Input resistance		R_{IRA}		100			kΩ
Receive signal level range		V_{IRA}		–48		–6	*1 dBm
Carrier detect level	ON	V_{CD} ON	R_8 = 33kΩ *2 R_9 = 51kΩ			–43	
	OFF	V_{CD} OFF		–48			
Carrier detect hysteresis		H_{YS}	V_{CD} ON – V_{CD} OFF	2			dB

Note *1. OdBm = 0.775Vrms *2. The resistor values are typical.

Receive filter

Group delay distortion	D_{DL}	ORIG. MODE	1600 ~ 1900 Hz		800		μS
		ANS. MODE	930 ~ 1230 Hz		850		
Adjacent channel rejection	L_{AC}	V_{AIN} = –6dBm		50			dB

Figure 1 **Block diagram**

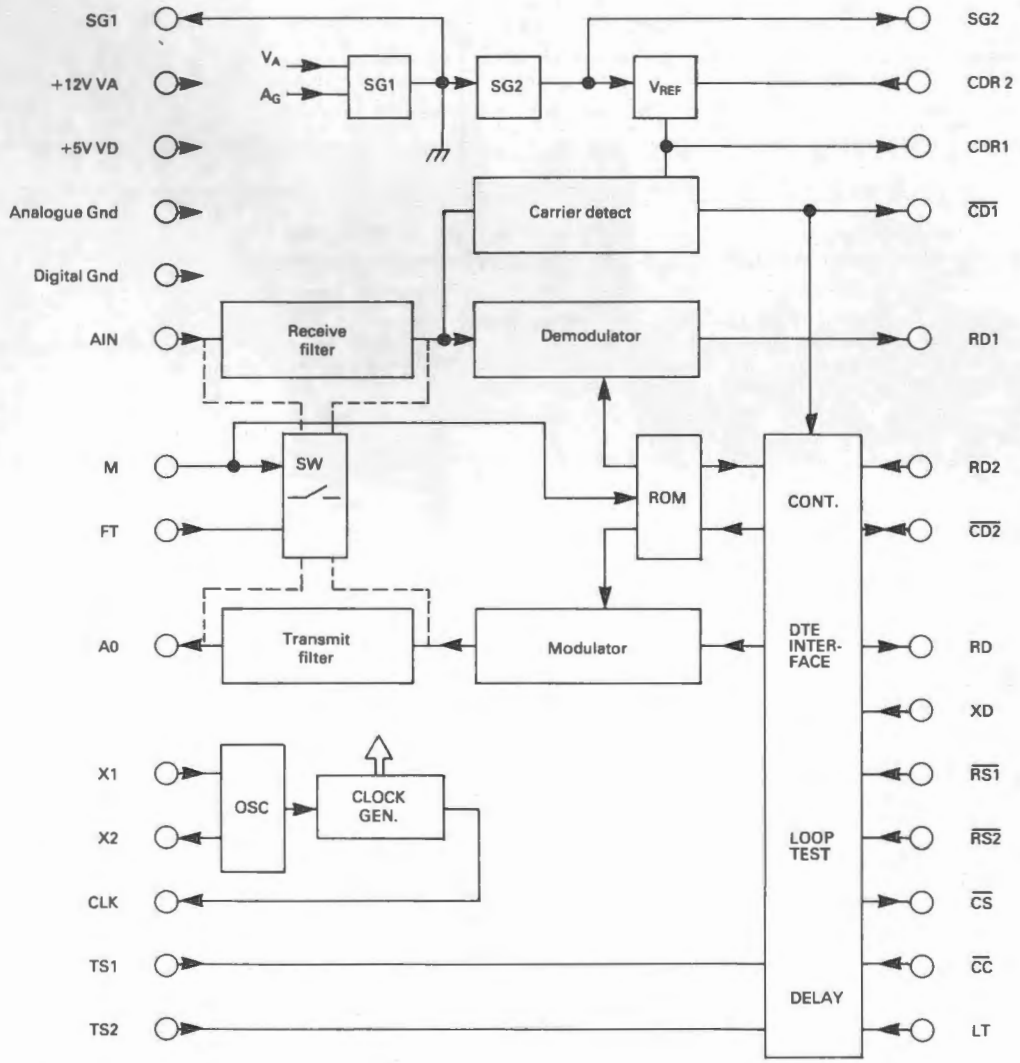


Figure 2 **Out-of-band energy referred to carrier level** (C_1 = 0.047 μF)

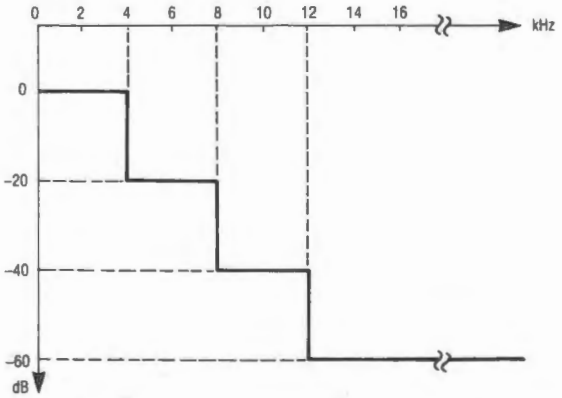


Figure 3 **Low band filter**

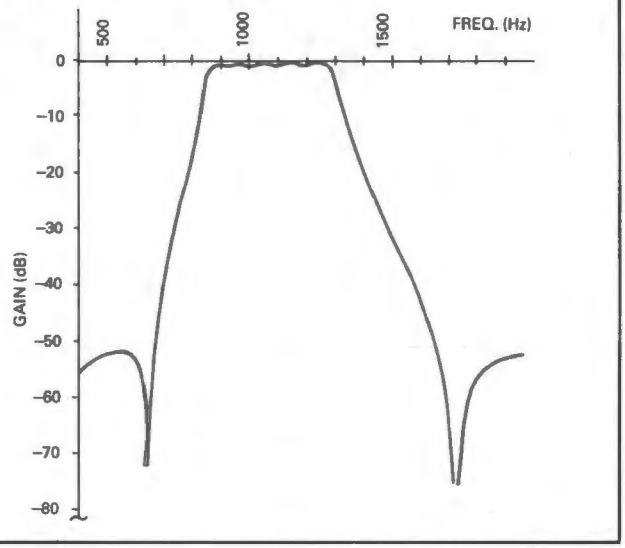
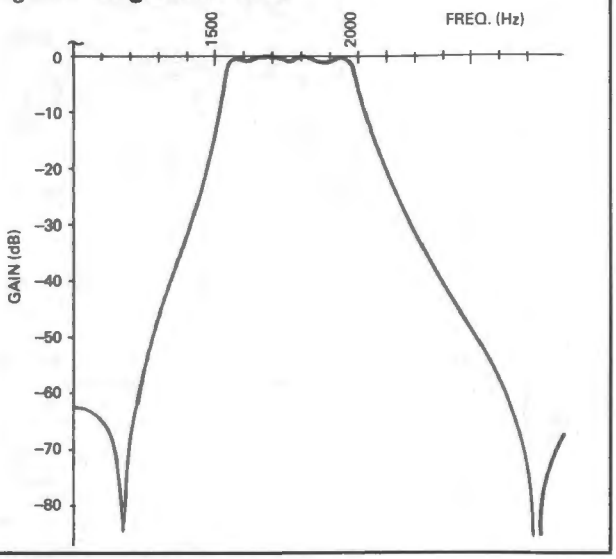


Figure 4 **High band filter**



Demodulated bit characteristics (VA = 12V ±10%, VD = 5V ±5%, T_a = 0 ~70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Peak intersymbol distortion	ID	Back-to-back over input signal range –6 to –40dBm. 511-bit test pattern.		6		%
Bit error rate	BER	Back-to-back with 0.3 ~ 3.4kHz flat noise. Receive signal level –25dBm. 511-bit test pattern; S/N (dB) 5		10^{-5}		

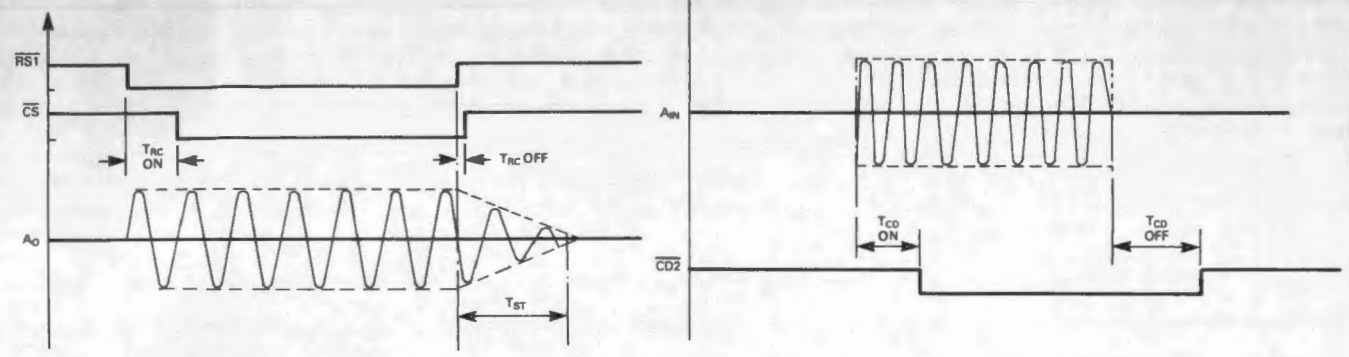
Timing characteristics (VA = 12V ±10%, VD = 5V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	TS2	TS1	Min	Typ	Max	Unit
RS/CS delay time	T_{RC} ON	$\overline{RS1}$ = '0' → $\overline{CS}$ = '0'	0	0	395	400	405	ms
			0	1	25	30	35	
			1	0	345	350	355	
			1	1	External delay timer			
	T_{RC} OFF	$\overline{RS1}$ = '1' → $\overline{CS}$ = '1'	*	*	0		0.5	
CD/ON delay time	T_{CD} ON		0	0	300		320	
			0	1	5		20	
			1	0	150		170	
			1	1	External delay timer			
CD/OFF delay time	T_{CD} OFF		0	0	20		70	
			0	1	20		70	
			1	0	10		40	
			1	1	External delay timer			
Soft Turn-OFF time	T_{ST}		*	*		10		

Refer to Figure 5.

Note *Irrespective of I/O condition.

Figure 5 **Timing diagrams**



Pin descriptions

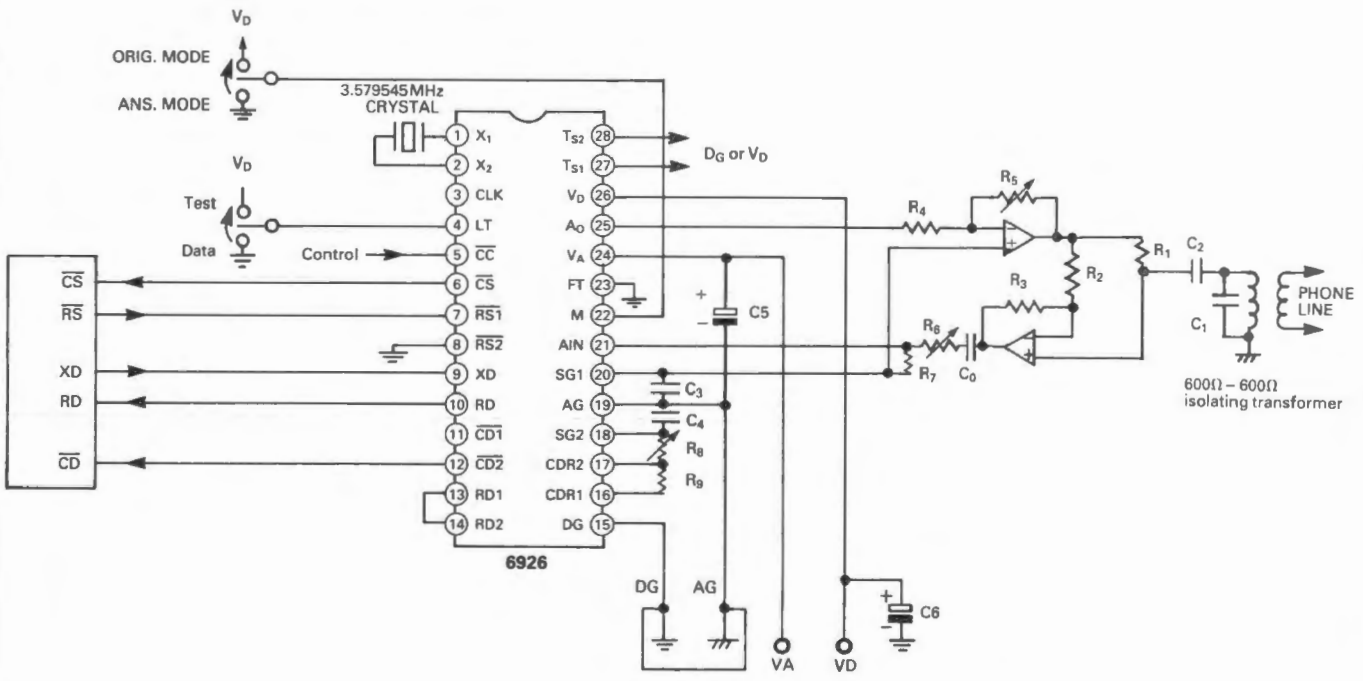
Name	Pin No.	I/O	Function
Power			
DG	15		Ground reference of V_D (digital ground)
AG	19		Ground reference of V_A (analogue ground)
V_A	24		Supply voltage (+12V nominal)
V_D	26		Supply voltage (+5V nominal)
Clocks			
X1 X2	1 2		Master clock timing is provided by either a crystal (3.579545MHz ±0.01%) connected across X1 and X2, or by an external TTL/CMOS clock driving X2 with ac coupling where X1 is left unconnected. See Figure 7.
CLK	3	O	873.9Hz clock output. This clock is used to implement external delay circuits etc.
Control			
LT	4	I	Digital loop back. During digital 'High', any data sent on the $\underline{X_D}$ pin will appear on the RD pin, and any data sent on the $\overline{RS1}$ pin will immediately appear on the $\overline{CS}$ pin. Any data demodulated from the received carrier on the A_{IN} pin will be the modulated data to implement the transmitted carrier. In this case, sending the transmitted carrier to the phone line depends on the $\overline{CC}$ line status and not on $\overline{RS1}$.
$\overline{CC}$	5	I	During digital loopback, the data on this pin becomes a control signal for sending the transmitted carrier to the phone line in place of $\overline{RS1}$.
$\overline{RS2}$	8	I	When an external circuit gives the RS/CS delay time which is not possible within the device, this pin should be connected to the external circuit output. See Figure 8.
$\overline{CD1}$	11	O	Fast carrier detection output. This pin is internally connected to the input of the built-in carrier detect delay circuit. When an external delay circuit provides the delay time which is not possible with the device alone, $\overline{CD1}$ should be connected to the external circuit input. See Figure 8.
$\overline{CD2}$	12	I/O	When an external circuit provides the carrier detect delay time which is not possible with the device alone, this pin becomes the input for the external circuit output signal. In other cases (when using the delay time within the device, the data on the TS1 or TS2 is not a digital 'High'), this pin becomes the Carrier-Detect signal output.
RD1	13	O	The RD1 data is demodulated data from the received carrier. RD2 is the input of the following logic circuits. See Figure 9. Usually, RD1 data is input directly to RD2. In some cases RD2 data is controlled by an NCU (Network-Control-Unit) etc. this may be required instead of the RD1 data.
RD2	14	I	
CDR1	16	O	These two pins are the output (CRD1) and inverting input (CDR2) of the buffer operational amplifier of which the noninverting input is connected to the built-in voltage reference, stabilized to variations in the supply voltage and temperature. See Figure 10. An adequate carrier-detect level can be set by selecting the ratio of R_8 and R_9. Therefore, the loss in the received carrier level by the phone-line transformer can be compensated for by adjusting the ratio of R_8 and R_9. $R_8 + R_9$ should be greater than 50kΩ.
CDR2	17	I	
M	22	I	Answer/Originate mode select. During digital 'High', the originate mode is selected. A low input selects the answer mode.
FT	23	I	This pin may be used for device tests only. During digital 'High', the A_O pin will be connected to the receiving filter output instead of transmitting filter output.

Name	Pin No.	I/O	Function
TS1	27	I	RS/CS delay and carrier detect delay options are selected by TS1 and TS2 inputs. If the external timing option is required, digital 'High' should be applied to TS1 and TS2 pins and the external delay circuits used to obtain the desired delay characteristics. In this case, the CD2 pin becomes not only the input for the externally delayed signal, but also the Carrier Detect output. See Figure 8.
TS2	28	I	

Inputs/Outputs

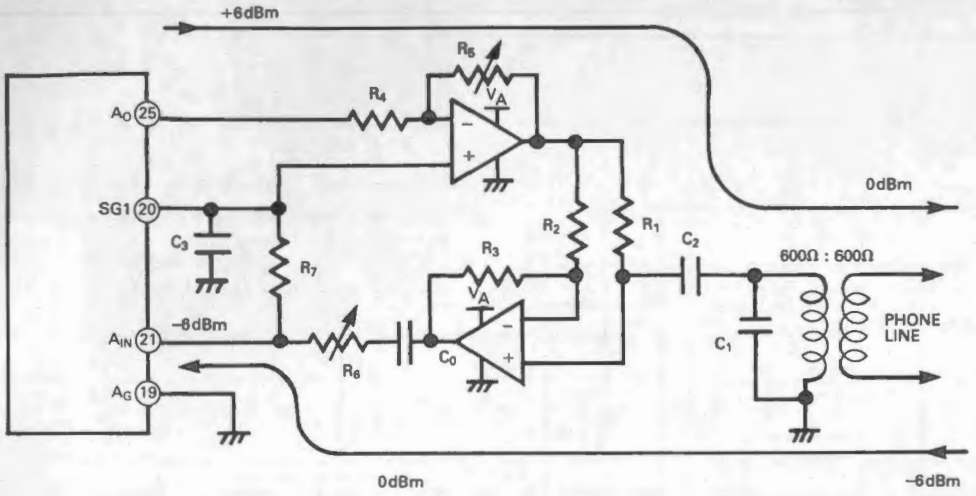
$\overline{CS}$	6	O	Clear-to-Send signal output. A digital 'High' level indicates the 'OFF' state and a digital 'Low' indicates the 'ON' state. This output goes 'Low' at the end of a delay (RS/CS delay) initiated when $\overline{RS1}$ (Request-to-Send) goes 'Low'.
$\overline{RS1}$	7	I	Request-to-Send signal output. A digital 'High' level indicates the 'OFF' state. A digital 'Low' level indicates the 'ON' state and instructs the modem to enter the transmit mode. This input must remain 'Low' for the duration of data transmission. 'High' turns the transmitter off.
XD	9	I	This is the digital data to be modulated and transmitted via A_O. A digital 'High' will be transmitted as 'Mark'. A digital 'Low' will be transmitted as 'Space'. No signal appears at A_O unless $\overline{RS1}$ is 'Low'.
RD	10	O	Serial digital data demodulated from A_{IN} is available at this output. A digital 'High' indicates 'Mark' and a digital 'Low' indicates 'Space'. For example, under the following condition, this output is forced to be a 'Mark' state because the data may be invalid. • When $\overline{CD2}$ (Carrier-detect) is in the 'OFF' state.
SG2	18	O	SG1 and SG2 are built-in analogue signal grounds. SG2 is used only for the Carrier-Detect function. The dc voltage of SG1 is approximately 6V, so the analogue line interface must be implemented by ac coupling. See Figure 6. To make these impedances lower and ensure device performance, it is necessary to put bypass capacitors on SG1 and SG2 in close physical proximity to the device.
SG1	20	O	
A_{IN}	21	I	This is the input pin for the analogue signal from the phone line. The modem extracts the information in this modulated carrier and converts it into a serial data stream for presentation at RD output.
A_O	25	O	This analogue output is the modulated carrier to be conditioned and sent over the phone line.

Figure 6 **Typical application circuits**



Notes

1. The crystal should be wired in close physical proximity to the device.
2. High level signals should not be routed next to low level signals.
3. Bypass capacitors on V_A, SG1 and SG2 should be as close to the device as possible.
4. AG and DG should be linked as close to the system ground as possible.
5. C_5 and C_6 are supply decoupling capacitors typically 10μF.



C_0, C_1	0.047 μF	R_2	51 kΩ	R_6	(51 kΩ) Receive signal level
C_2	2.2 μF	R_3	51 kΩ	R_7	51 kΩ
C_3	1 μF	R_4	51 kΩ	R_8	(33 kΩ) Carrier detect level
R_1	600Ω	R_5	(51 kΩ) Transmit signal level	R_9	51 kΩ

Note The signal level on the A_{IN} pin should not exceed −6dBm.

Figure 7

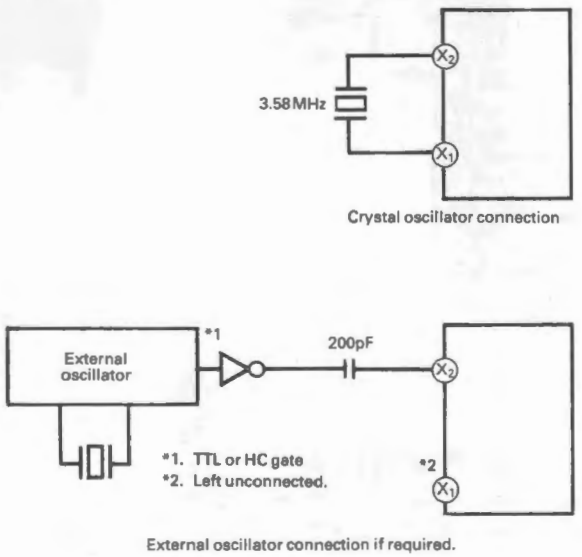
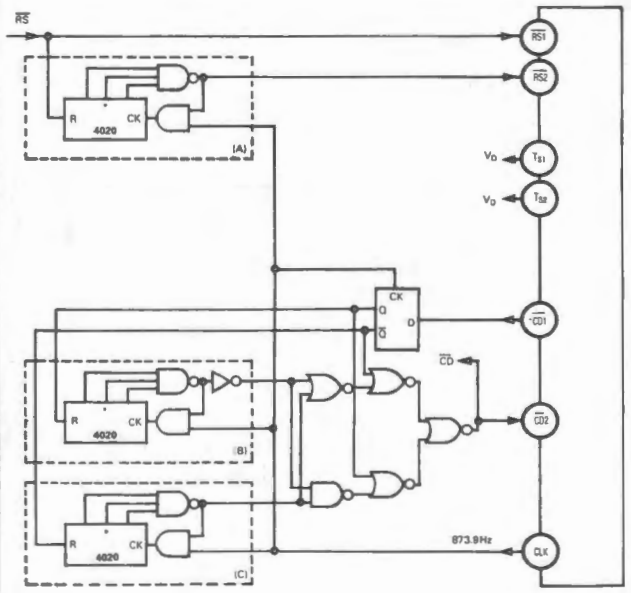


Figure 8 **External delay connection**



(A) RS/CS delay, (B) . . . CD/ON delay, (C) . . . CD/OFF delay

Note Supply voltage equals V_D for all gates.

* : The desired delay can be realised by selecting the appropriate bits from 4020's outputs. The number of the bits is not always 3. Each delay can be set differently from built-in delays.

Figure 9 **Equivalent logic interface of the integrated modem**

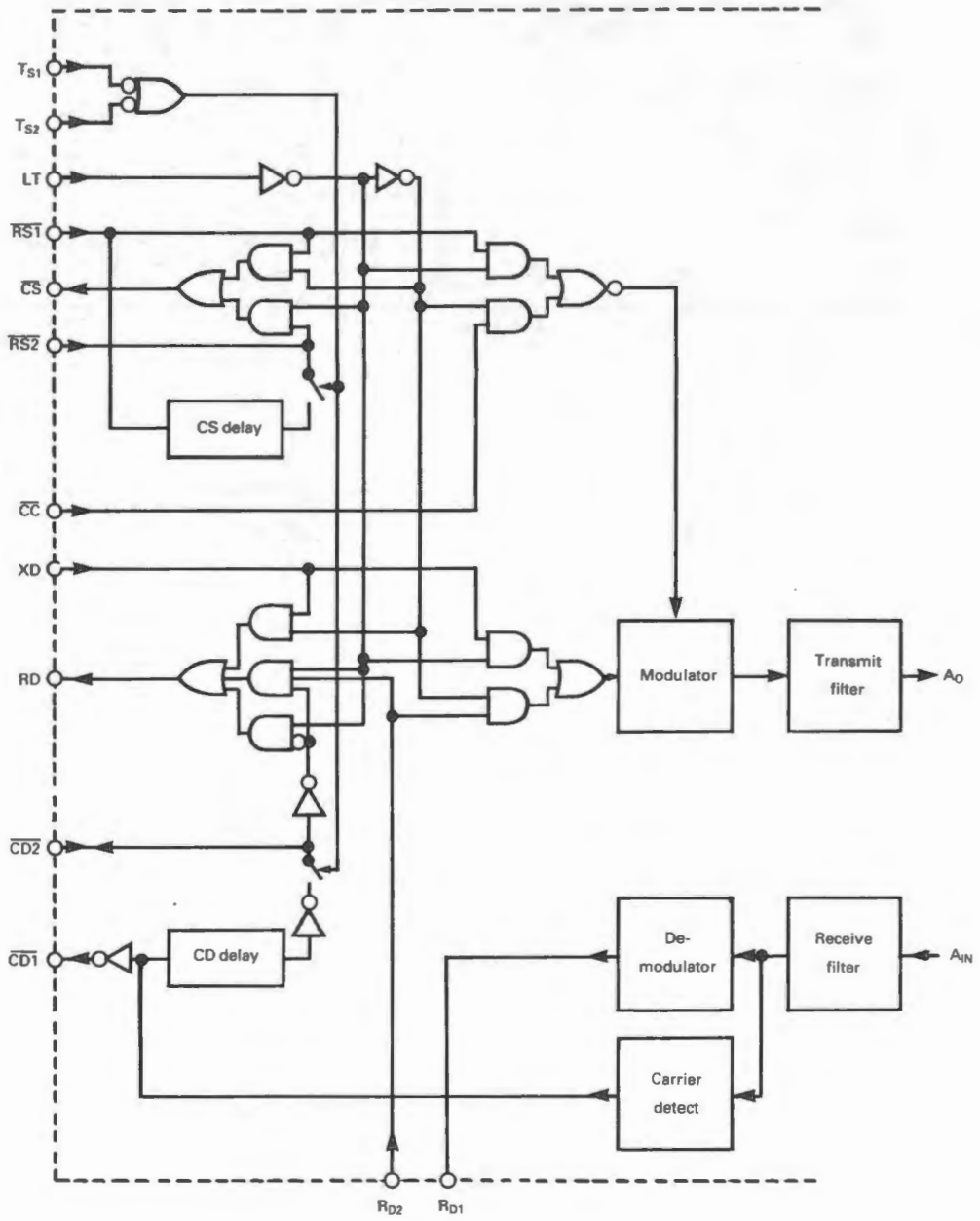
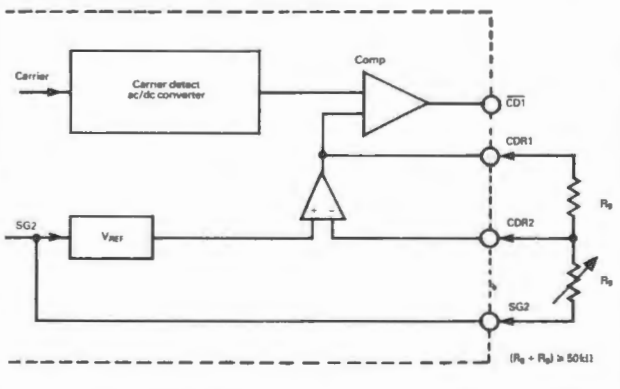


Figure 10 **External resistor connection for the setting of carrier detect level**



General information

The telephone line allows transmission of analogue audio frequency signals, but the digital data signal, as such, cannot be passed through. For this reason, modems are required as interface to existing analogue transmission lines.

The basic role of a modem is to convert digital logic signals '1' and '0' into an analogue equivalent that can be passed through a telephone line, and vice versa.

A data signal (digital signal) from a data terminal is converted into an analogue audio signal, and transmitted to the modem of a receiving terminal utilising the public telephone network. At the receiving end, the analogue audio signal thus received is then converted by its modem into a corresponding digital signal and conveyed to the receiving data terminal.

In this way, two distant data terminals can communicate for the exchange of data by means of modems.

Referring to Figure 11, modulation and demodulation means the conversion of digital signals into analogue and vice versa. The duplexer transmits a signal to the telephone line or receives it from the telephone line, and is designed to ignore the locally generated transmitted signal. Usually, it uses a hybrid transformer or hybrid resistor circuit consisting of two operational amplifiers, resistors and a line transformer.

Modem communication systems

The modem communication systems are largely divided into modes of operation. One is called the full duplex system, and the other the half-duplex system. The telephone line is a balanced two-wire circuit, and usually is called the 2-wire (2W) line. The full-duplex and half-duplex are terms which conform to the common use of this 2-wire line.

a) **4-wire full-duplex communication**
The 4-wire half-duplex communication is another widely practised method in which two dedicated telephone lines are used for transmission and reception, respectively. This method provides transmission and reception simultaneously, but requires two telephone lines.

b) **2-wire half-duplex communication**
The 2-wire half-duplex communication is a method which links two terminals in either direction, but only one direction at a time. Namely, when one terminal is transmitting, the other must operate in the receiving mode. This limitation may be a drawback for certain applications.

c) **2-wire full-duplex communication**
The 2-wire full-duplex communication is a method in which duplexers or the like are used to permit two distant terminals to work in both directions simultaneously through a 2-wire line. This method is more economical compared with 2-wire half duplex.

The above three methods are schematically shown in Figure 12.

Figure 11 **Typical modem system**

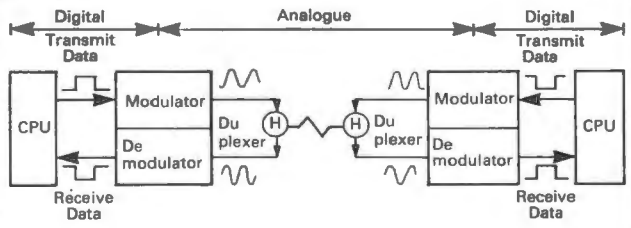


Figure 12 **Modem communication systems**

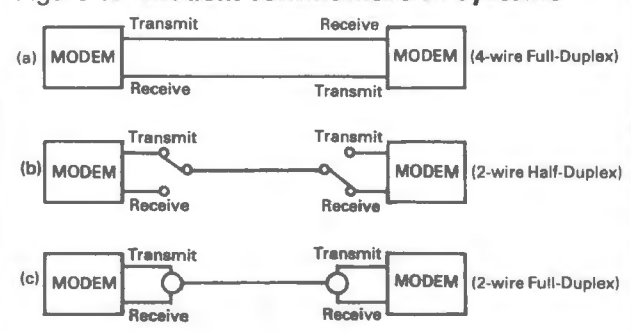
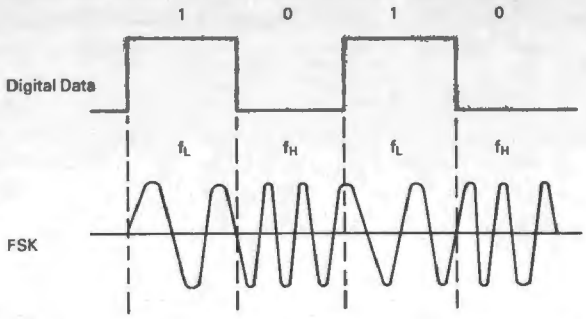


Figure 13 **FSK transmission**



Modem operation

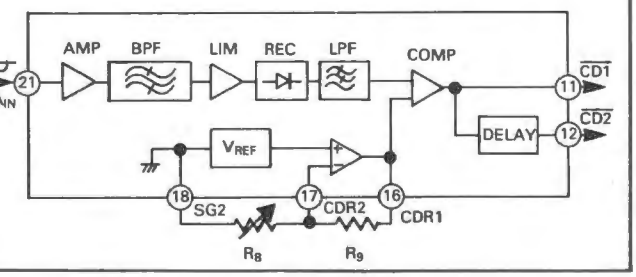
In case of manual calling, the modem is placed in the originate and voice mode (telephone line connected to the telephone handset), and a call is made using the telephone handset.

When an answer is detected (ie. an answer mark tone is heard), the modem is placed in the data mode (the telephone line connected to the modem), and the indicator will light up showing that a carrier signal from the answering modem is received.

Setting of the carrier detect level

In the 6926, the receive carrier detect ON and OFF levels can be set within the range of –43 to –48 dBm by adjusting the ratio of the external resistors R_8 and R_9.

Figure 14



After adjustment, the voltage between Pin 16 (CDR1) and Pin 18 (SG2) will be about 3V. Since the input signal level is referenced to Pin 21 (A_{IN}) of the LSI, it may have to be amplified if attenuated by a line transformer, etc.

Figure 15

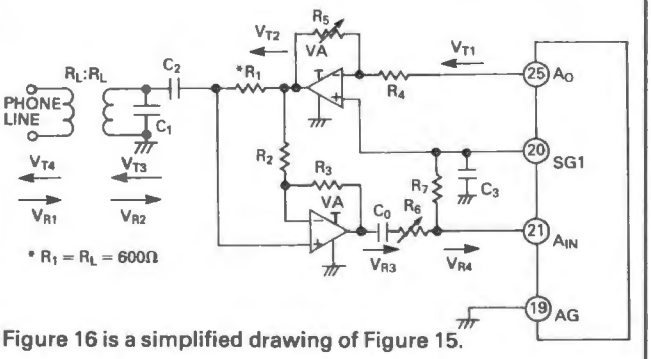
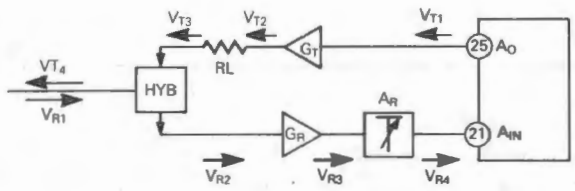


Figure 16 is a simplified drawing of Figure 15.

RS data

Figure 16



GR	$1 + \frac{R_3}{R_2}$	2 ≡ +6dB
A_R	$\frac{R_7}{R_6 + R_7}$	1/2 ≡ –6dB
G_T	$\frac{R_5}{R_4}$	1 ≡ 0dB

Typical Design Values

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RS data

Heatsink performance guide

An outline guide to the selection of heatsinks with regard to their thermal performance.

Defining the necessary heat sink performance

In order to calculate the maximum acceptable thermal resistance for the heat sink so that the device being cooled does not overheat it is first necessary to define the thermal parameters under which it is to operate.

The basic equation for thermal equilibrium is:

$$\text{Power dissipated} = \frac{\text{Temperature difference across the system}}{\text{Sum of all the thermal resistances in the heat flow path.}}$$

$$\text{Thus PD} = \frac{Tj - Ta}{\theta jc + \theta cs + \theta sa} \qquad \text{(equ 1)}$$

Where PD = Power dissipation (W)
Tj = Max allowable junction temp (°C) (specified by device manufacturer)
Ta = Ambient temperature (°C)
θjc = Thermal resistance, junction to case (°C/W) (specified by manufacturer)
θcs = Thermal resistance, case to heat sink (°C/W)
θsa = Thermal resistance, heat sink to ambient air (°C/W)

The maximum value for thermal resistance heat sink to air (sa) is usually determined by rearranging equation 1 to the following:

$$\theta sa = \frac{Tj - Ta - (\theta jc + \theta cs)}{PD} \qquad \text{(equ 2)}$$

The result of the above equation provides a thermal resistance value which must be equalled or bettered by the heat sink selected.

Example

A semi-conductor device is to be operated with its junction temperature not exceeding 90°C whilst dissipating 14.50 watts to ambient air at a temperature of 45°C. The thermal resistance, junction to case, is specified by the manufacturer as 2.25°C/W and the thermal resistance, case to sink (using an insulating washer and thermally conductive compound) is taken as 0.50°C/W

$$\therefore \theta sa = \frac{90 - 45}{14.50} - (2.25 + 0.50)$$

$$= 0.35°C/W$$

The heat sink therefore must have a thermal resistance which does not exceed 0.35°C/W.

A suitable heat sink may therefore be the 0.3°C/W type 403-112.

RS data

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Group Company

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RS data

Switching regulator L296

Stock number 631-648

The L296 is a stepdown power switching regulator delivering 4A at a voltage variable from 5.1V to 40V.

Features of the device include programmable current limiting, soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronisation in multichip configurations.

Efficient operation at switching frequencies up to 200kHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

The L296 is mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

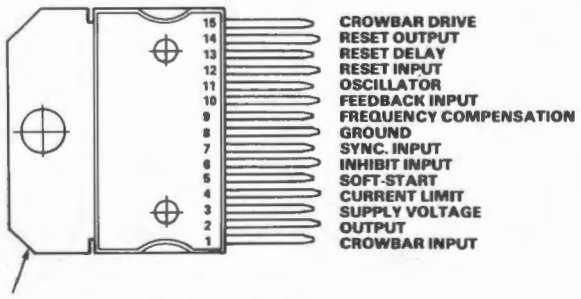
Absolute maximum ratings

Input voltage (pin 3)	50V
Input to output voltage difference	50V
Output dc voltage	−1V
Output peak voltage at t = 0.1 μsec f = 200kHz	−7V
Voltage at pins 1, 12	10V
Voltage at pins 6 and 15	15V
Voltage at pins 4, 5, 7 and 9	5.5V
Voltage at pins 10 and 6	7V
Voltage at pin 14 ($I_{14} \leq 1mA$)	V_{IN}
Pin 9 sink current	1mA
Pin 11 source current	20mA
Pin 14 sink current ($V_{14} < 5V$)	50mA
Power dissipation at $T_{case} \leq 90°C$	20W
Junction and storage temperature	−40°C to +150°C

Features

- 4A output current
- 5.1V to 40V output voltage range
- 0 to 100% duty cycle range
- Precise (± 2%) on-chip reference
- Switching frequency up to 200kHz
- Very high efficiency (up to 90%)
- Very few external components
- Soft start
- Reset output
- Control circuit for crowbar SCR
- Input for remote inhibit and synchronus PWM
- Thermal shutdown.

Pin connections (Top view)

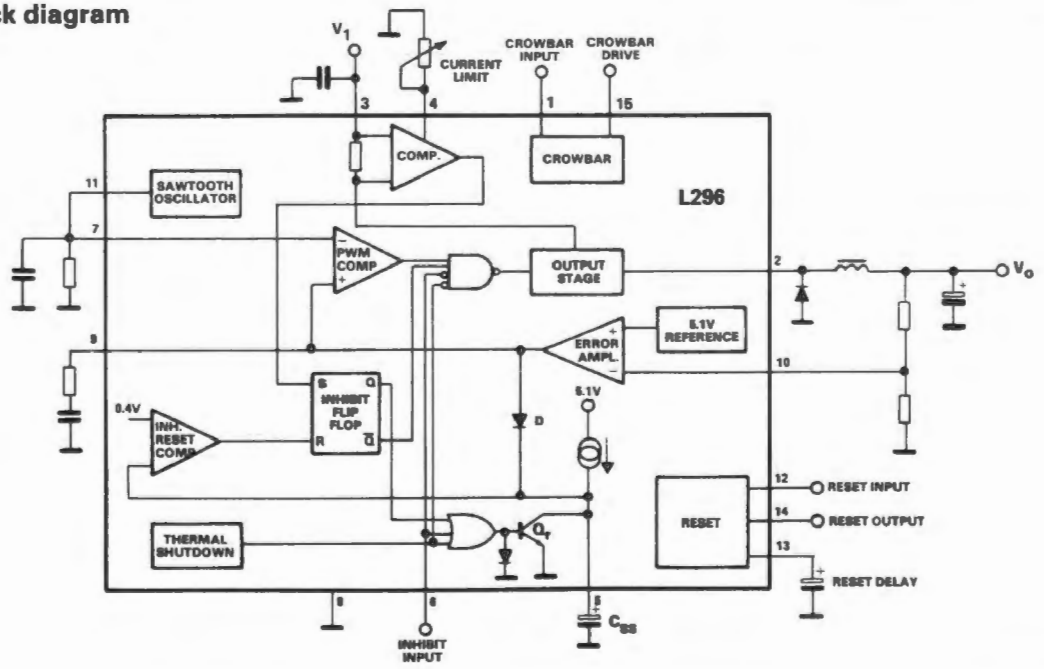


Tab connected to pin 8

Pin functions

No.	Name	Function
1	Crowbar input	Voltage sense input for crowbar overvoltage protection. Normally connected to the feedback input thus triggering the SCR when V_{OUT} exceeds nominal by 20%. May also monitor the input and a voltage divider can be added to increase the threshold. Connect to ground when SCR not used.
2	Output	Regulator output.
3	Supply voltage	Unregulated voltage input. An internal regulator powers the L296's internal logic.
4	Current limit	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical characteristics).
5	Soft start	Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	Inhibit input	TTL – level remote inhibit. A logic high level on this input disables the L296.
7	Sync input	Multiple L296s are synchronised by connecting pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	Ground	Common ground terminal
9	Frequency compensation	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	Feedback input	The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
11	Oscillator	A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
12	Reset input	Input of the reset circuit. The threshold is roughly 5V. It may be connected to the feedback point or via a divider to the input.
13	Reset delay	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	Reset output	Open collector reset signal output. This output is high when the supply is safe.
15	Crowbar output	SCR gate drive output of the crowbar circuit.

Figure 1 **Block diagram**



Electrical characteristics (T_j = 25°C, V_i = 35V, unless otherwise specified)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
Dynamic characteristics (pin 6 to GND unless otherwise specified)							
V_o	Output voltage range	V_i = 46V	I_o = 1A	V_{ref}		40	V
V_i	Input voltage range	V_o = V_{ref} to 36V	I_o = 4A	9		46	V
ΔV_o	Line regulation	Vi = 10V to 40V, V_o = V_{ref}, I_o = 2A			15	50	mV
ΔV_o	Load regulation		I_o = 2A to 4A		10	30	mV
		V_o = V_{ref}	I_o = 0.5A to 4A		15	45	mV
V_{ref}	Internal reference voltage (pin 10)	V_i = 9V to 46V I_o = 2A		5	5.1	5.2	V
$\frac{\Delta V_{ref}}{\Delta T}$	Average temperature coefficient of reference voltage	T_j = 0°C to 125°C	I_o = 2A		0.4		mV/°C
V_d	Dropout voltage between pin 2 and pin 3	I_o = 4A			2	3.2	V
		I_o = 2A			1.3	2.1	V
Io_m	Maximum operating load current	V_i = 9V to 46V, V_o = V_{ref} to 36V		4			A
1_{2L}	Current limiting threshold (pin 2)	V_i = 9V to 46V V_o = V_{ref} to 40V	Pin 4 open			8	A
			R_{lim} = 33kΩ		2.5		A
I_{SH}	Input average current	V_i = 46V; Output short-circuited			60	100	mA
n	Efficiency	I_o = 3A	V_o = V_{ref}		75		%
			V_o = 12V		85		%
SVR	Supply voltage ripple rejection	ΔV_i = $2V_{rms}$ V_o = V_{ref}	f_{ripple} = 100Hz I_o = 2A	50	56		dB
f	Switching frequency			85	100	115	kHz
$\frac{\Delta f}{\Delta V_i}$	Voltage stability of switching frequency	V_i = 9V to 46V			0.5		%
$\frac{\Delta f}{\Delta T_j}$	Temperature stability of switching frequency	T_j = 0°C to 125°C			1		%
f_{max}	Maximum operating switching frequency	V_o = V_{ref}, I_o = 1A		200			kHz
T_{sd}	Thermal shutdown junction temperature			135	145		°C
dc characteristics							
I_{3Q}	Quiescent drain current	V_i = 46V V_7 = 0V	V_6 = 0V		66	85	mA
			V_6 = 3V		30	40	mA
$-I_{2L}$	Output leakage current	V_i = 46V, V6 = 3V, S1:B,S2: A, V7 =0V				2	mA
Soft start							
I_{5so}	Source current	V_6 = 0V, V_5 = 3V		100	130	160	μA
I_{5si}	Sink current	V_6 = 3V, V_5 = 3V		50	70	120	μA
Inhibit							
V_{6L}	Low input voltage	V_i = 9V to 46V		–0.3		0.8	V
V_{6H}	High input voltage	V_7 = 0V		2		5.5	V
$-I_{6L}$	Input current with low input voltage	V_i = 9V to 46V	V_6 = 0.8V			10	μA
$-I_{6H}$	Input current with high input voltage	V_7 = 0V	V_6 = 2V			3	μA

Error amplifier

V_{9H}	High level output voltage	V_{10} = 4.7V, I_9 = 100μA	3.5			V
V_{9L}	Low level output volt.	V_{10} = 5.3V, I_9 = 100μA			0.5	V
I_{9si}	Sink output current	V_{10} = 5.3V	100	150		μA
$-I_{9so}$	Source output current	V_{10} = 4.7V	100	150		μA
I_{10}	Input bias current	V_{10} = 5.2V		2	10	μA
G_v	dc open loop gain	V_9 = 1V to 3V	46	55		dB

Oscillator and PWM comparator

$-I_7$	Input bias current of PWM comparator	V_7 = 0.5V to 3.5V			5	μA
$-I_{11}$	Oscillator source current	V_{11} = 2V	5			mA

Reset

V_{12R}	Rising threshold voltage	V_i = 9V to 46V		V_{ref} −150mV	V_{ref} −100mV	V_{ref} −50mV	V
V_{12F}	Falling threshold voltage			4.75	V_{ref} −150mV	V_{ref} −100mV	V
V_{13D}	Delay threshold voltage	V_{12} = 5.3V		4.3	4.5	4.7	V
V_{13H}	Delay threshold voltage hysteresis				100		mV
V_{14S}	Output saturation voltage	I_{14} = 16mA; V_{12} = 4.7V				0.4	V
I_{12}	Input bias current	V_{12} = 0V to V_{ref}			1	3	μA
$-I_{13so}$	Delay source current	V_{13} = 3V	V_{12} = 5.3V	70	110	140	μA
I_{13si}	Delay sink current		V_{12} = 4.7V	10			mA
I_{14}	Output leakage current	V_i = 46V, V_{12} = 5.3V				100	μA

Crowbar

V_1	Input threshold voltage			5.5	6	6.4	V
V_{15}	Output saturation voltage	V_i = 9V to 46V, I_{15} = 5mA	V_1 = 5.4V		0.2	0.4	V
I_1	Input bias current	V_1 = 6V				10	μA
$-I_{15}$	Output source current	V_i = 9V to 46V, V_{15} = 2V	V_1 = 6.5V	70	100		mA

Thermal data

$R_{th\ j\text{-}case}$	Thermal resistance junction-case			3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient			35	°C/W

Typical characteristic curves

Figure 2 **Quiescent drain current vs. supply voltage (0% duty cycle)**

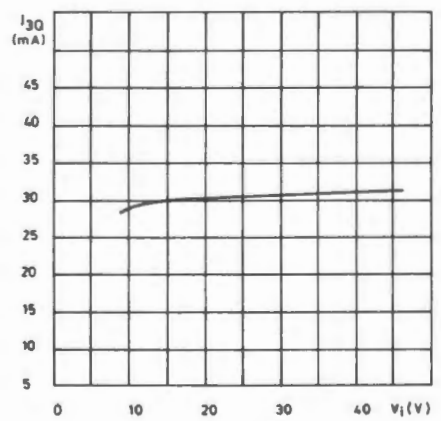


Figure 3 **Quiescent drain current vs. supply voltage (100% duty cycle)**

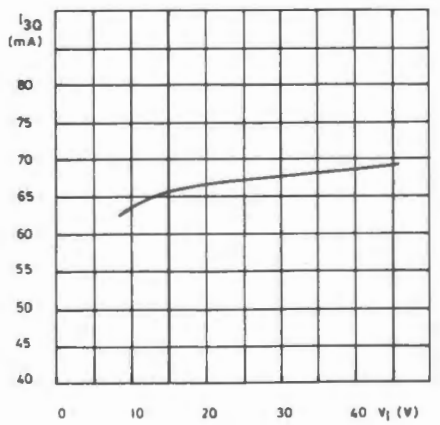


Figure 4 **Quiescent drain current vs. junction temperature (0% duty cycle)**

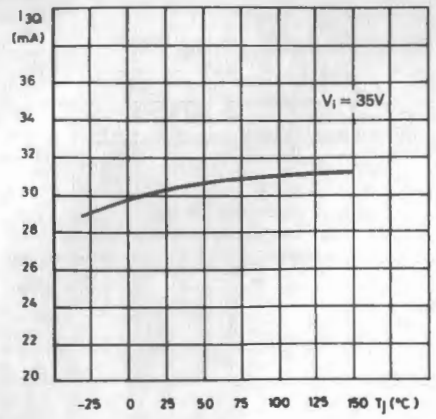


Figure 5 **Quiescent drain current vs. junction temperature (100% duty cycle)**

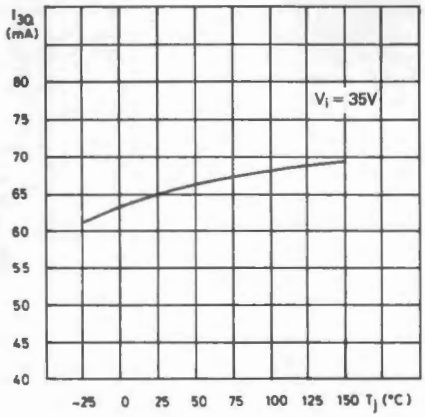


Figure 6 **Reference voltage (pin 10) vs. V_i**

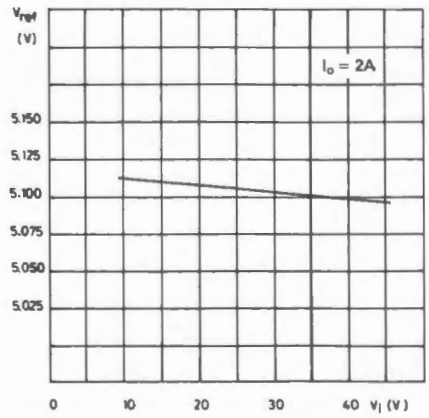


Figure 7 **Reference voltage (pin 10) vs. junction temperature**

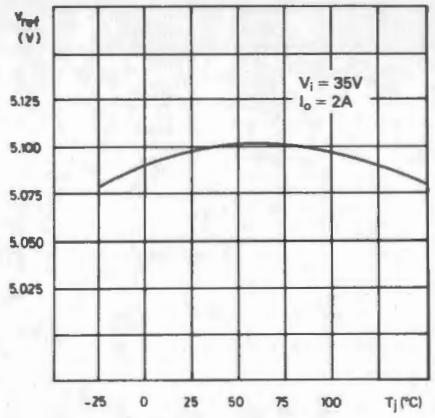


Figure 8 **Open loop frequency and phase response of error amplifier**

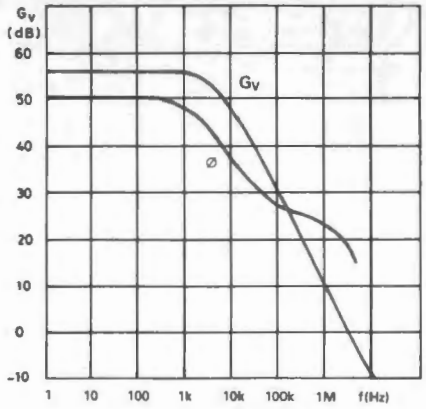


Figure 9 **Switching frequency vs. input voltage**

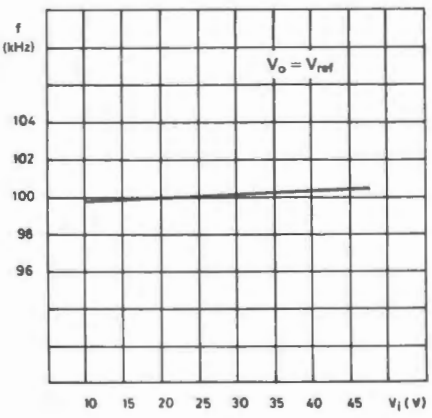


Figure 10 **Switching frequency vs. junction temperature**

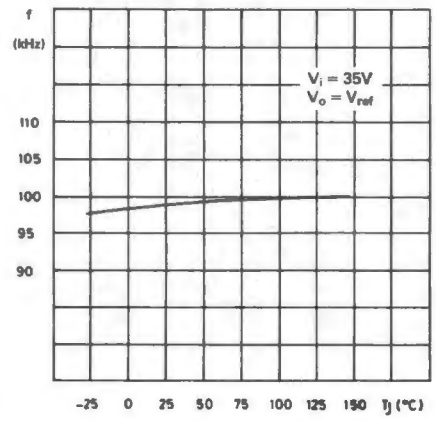


Figure 11 **Switching frequency vs. R1**

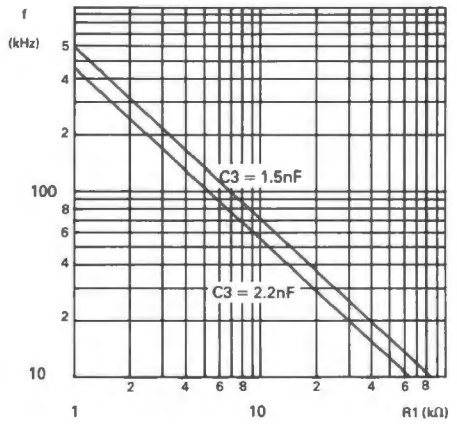


Figure 12 **Line transient response**

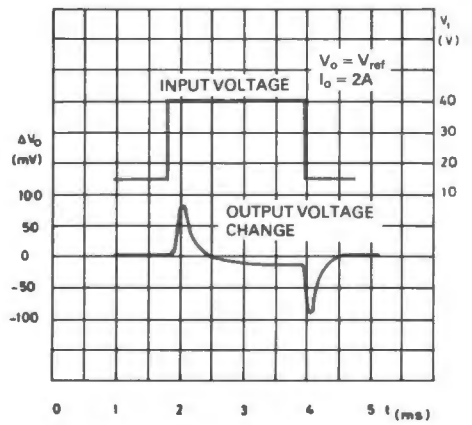


Figure 13 **Load transient response**

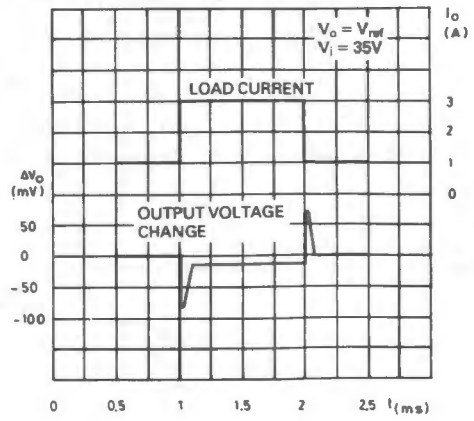


Figure 14 **Supply voltage ripple rejection vs. frequency**

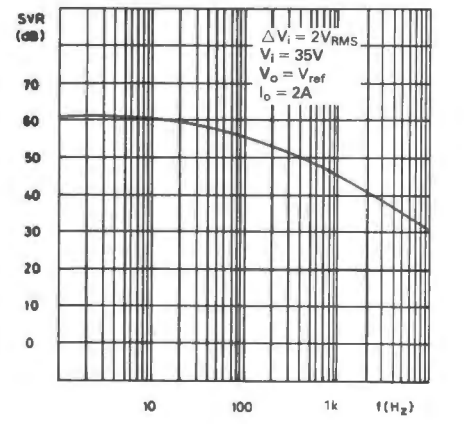


Figure 15 **Dropout voltage between pin 3 and pin 2 vs. current at pin 2**

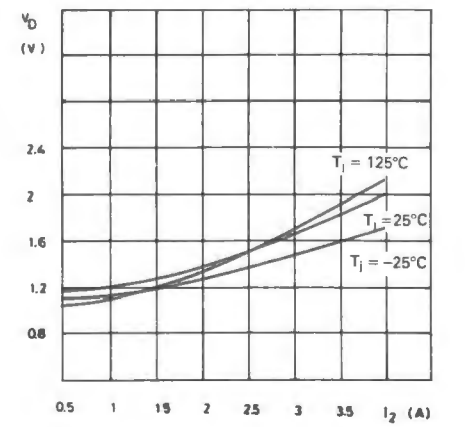


Figure 16 **Dropout voltage between pin 3 and pin 2 vs. junction temperture**

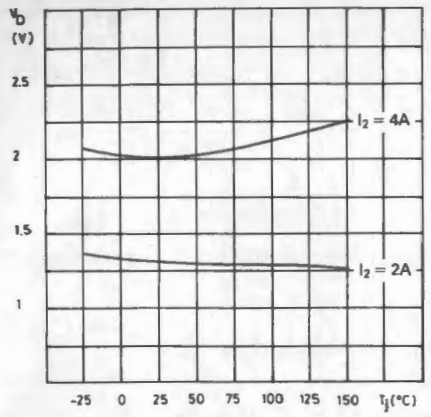


Figure 17 **Power dissipation derating curve**

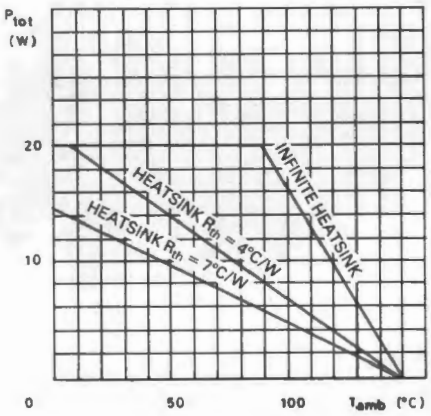


Figure 18 **Power dissipation vs. input voltage**

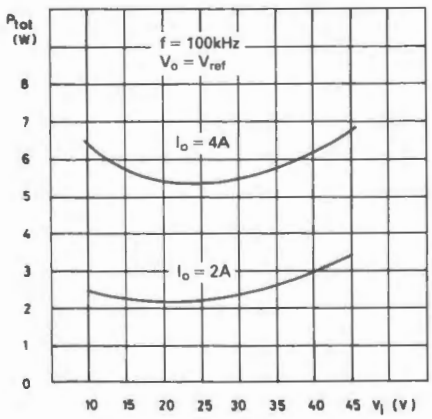


Figure 19 **Power dissipation vs. input voltage**

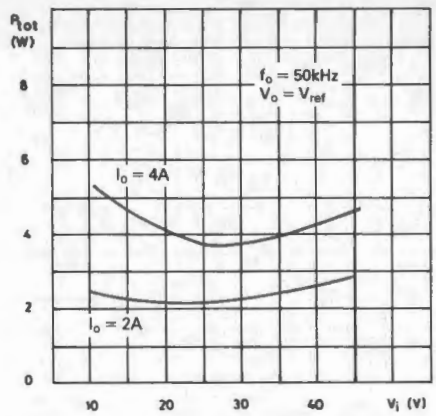


Figure 20 **Power dissipation vs. output voltage**

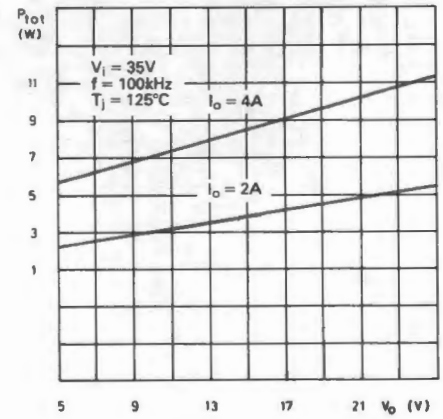


Figure 21 **Power dissipation vs. output voltage**

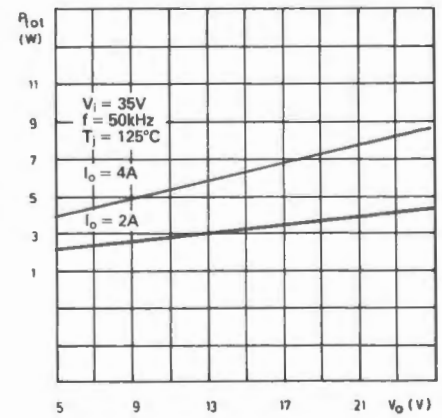


Figure 22 **Voltage and current waveforms at pin 2**

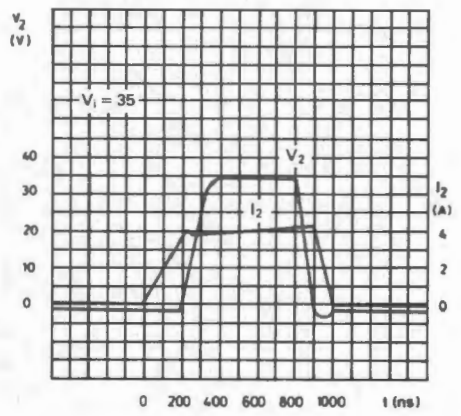


Figure 23 **Efficiency vs. output current**

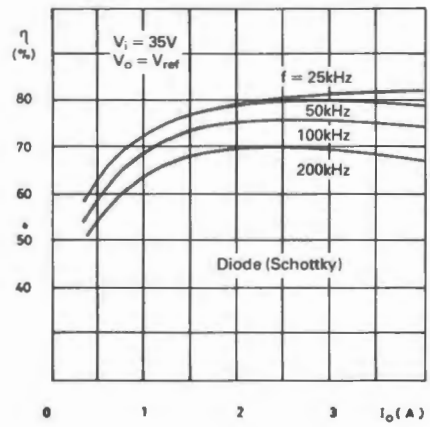


Figure 24 **Efficiency vs. output current**

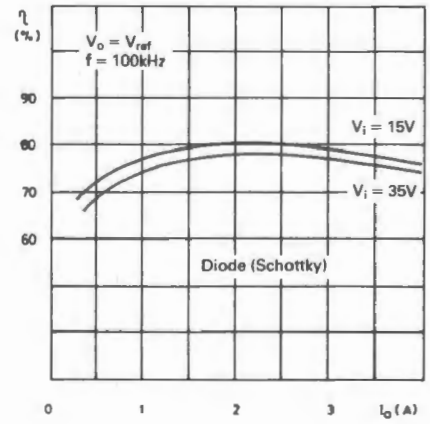


Figure 25 **Efficiency vs. output voltage**

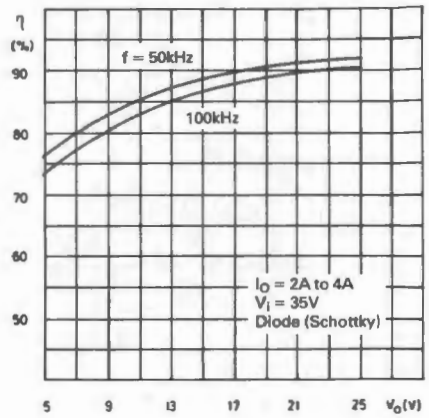
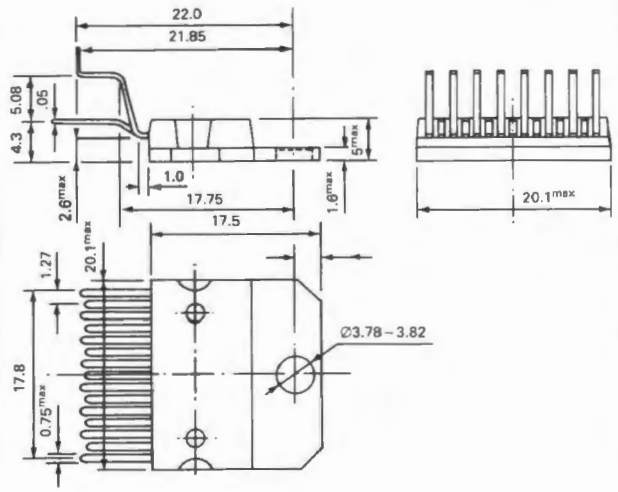


Figure 26 **Mechanical data**
(Dimensions in mm)



Switching vs. Linear

Switching regulators are more efficient than linear types so the transformer and heatsink can be smaller and lower cost. But how much can be gained.

The savings can be estimated by comparing equivalent linear and switching regulators. For example, suppose that a 4A/5V supply is required.

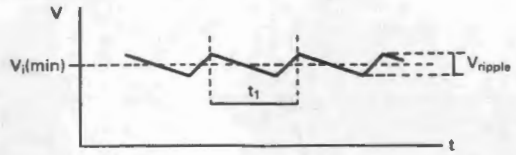
Linear

For a good linear regulator the minimum dropout will be at least 5V at 4A. The minimum input voltage is given by:

$$V_i \min = V_o + V_{drop} + \frac{1}{2} V_{ripple}$$

where:

$$V_{ripple} \simeq \frac{I_o t_1}{C} = \frac{4 \times 10 \times 10^{-3}}{10 \times 10^{-3}} = 4.0V$$



T_1 is 10ms at a mains frequency of 50Hz and using 10.000μF for C, the filter capacitor after the bridge). Therefore $V_{i\ min} \simeq 12V$. Since operation must be guaranteed even when the mains voltage falls 10%, the nominal voltage on load at the terminals of the regulator must be:

$$V_{nom} = \frac{V_{i\ min}}{0.9} = \frac{12}{0.9} = 13.33V$$

To allow even a small margin we have to choose:

$V_{nom} = 14V$

The power that the series element must dissipate is therefore:

$P_d = (V_{nom} - V_o)\, I_o = 36W$

and a heatsink will be necessary with a thermal resistance of:

$R_{th\ heats.} = 0.8°C/W$

and the transformer must supply a power of:

$P_{diss} = 14 \times 4 = 56W$

It must therefore be dimensioned for:

$$P_D = \frac{56}{0.9} = 62VA$$

Switching (L296)

Assuming the same nominal voltage (14V), the L296 data sheet indicates that the power dissipated in this case is only 7W. And this power is dissipated in two elements; the L296 itself and the recirculation diode.

It follows that the transformer must be roughly 30VA and the heatsink thermal resistance about 11°C/W.

	Linear	Switching
Transformer	62VA	30VA
Heatsink	0.8°C/W	11°C/W

This comparison shows that the L296 switching regulator allows a saving of roughly 50% on the cost of the transformer and an impressive 80-90% on the cost of the heatsink. Considering also the extra functions integrated by the L296 the total cost of active and passive components is roughly the same for both types.

Finally, it is important to note that a lower power dissipation means that the ambient temperature in the regulator enclosure can be lower – particularly when the circuit is enclosed in a box – with all the advantages cooler operation brings.

If for some reason it is necessary to use higher supply voltages the switching technique, and hence the L296, becomes even more advantageous.

Device description

The illustration on page 1 shows the package in which the device is mounted and the pin function assignments.

The internal structure of the device is shown in Figure 1. Each block will now be examined.

Power supply

The device is provided with an internal stabilized power supply that, besides supplying the reference voltage of 5.1V for the whole system, also supplies the internal analogue blocks.

Special features of the voltage reference are its accuracy, temperature stability and high line rejection. Through zener-zap trimming, the voltage is within ±2% limits.

Oscillator

The oscillator block generates the saw-tooth waveform that sets the switching frequency of the system. The signal, when compared with the output voltage of the error amplifier, generates the PWM signal to be sent to the power output stage. The saw-tooth, of which amplitude is between 1.2V and 3.2V, is generated by charging rapidly the C_{osc} capacitor which then discharges across the R_{osc} resistance. As shown in Figure 27, the oscillator is realised by a comparator (with ground compatible input) with hysteresis whose thresholds are 1.2V and 3.2V respectively. The C_{osc} capacitor and the R_{osc} resistor are connected to the non-inverting input of the comparator which sets the oscillating frequency. When the voltage on pin 11 is less than 3.2V, the switch S_1 is closed and the current generator charges the C_{osc} capacitor rapidly; in this phase S_2 is also closed. As soon as 3.2V is reached the comparator output drives S_2 open (also opening S_1); the inverting input voltage is reduced to about 1.2V and the capacitor starts to discharge itself across the R_{osc} resistor (the I_{bias} effect is neglected). When the voltage reaches 1.2V, S_2 and S_1 close again and a new cycle starts. The generated waveform is shown in Figure 28.

To achieve a good accuracy of the switching frequency it is essential to have a charging time of the capacitor which is much smaller than the discharging time. In this way, the oscillation frequency only depends on the external components C_{osc} and R_{osc}. For this reason the capacitor charging current (when S_1 is ON) is typically around 10mA. For example, with a 2.2nF capacitor to switch from 1.2V to 3.2V about 400ns is required, which is negligible compared to the 10μs period that occurs when the operation is performed at 100kHz. The diagrams shown in Figure 29 allow the selection of the R_{osc} value (R_1 in Figure 29) with C_{osc} as a parameter (C_3 in Figure 29) when the oscillation frequency required for operation has been previously fixed.

Figure 27 **Internal schematic of the oscillator**

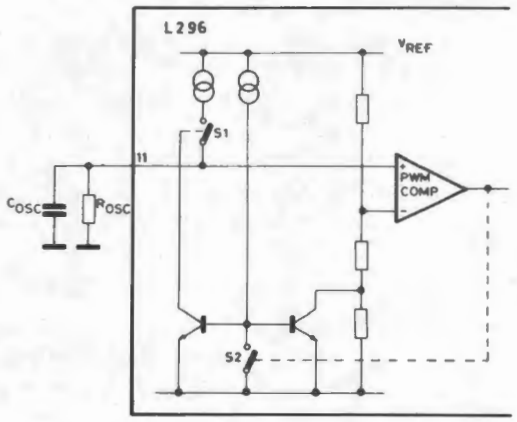


Figure 28a **Oscillator waveform at pin 11 with f = 100kHz (R_{OSC} = 4.3kΩ, C_{OSC} = 2.2nF)**

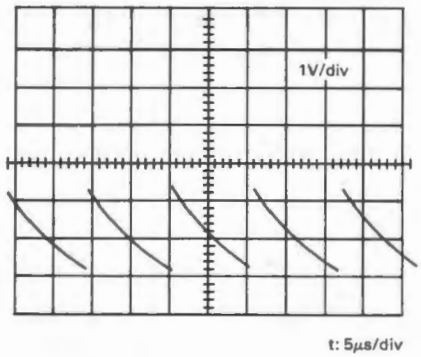


Figure 28b **Oscillator waveform at pin 11 with f = 50kHz (R_{OSC} = 9.1kΩ, C_{OSC} = 2.2nF)**

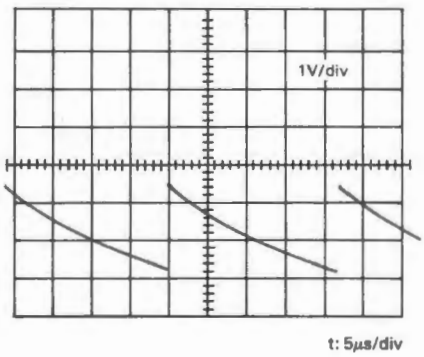


Figure 29 **Nomogram for the choice of oscillator components**

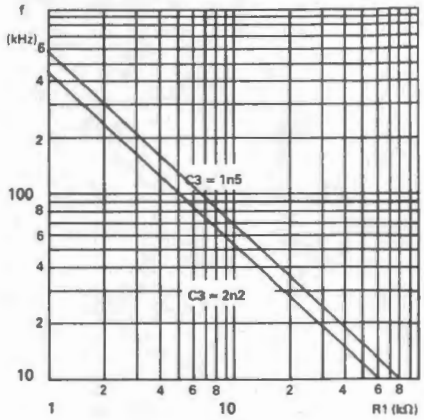


Figure 29 shows two suggested values for the C_{OSC} capacitance. Excessively low capacitance value may give rise to an inaccuracy of the upper threshold due to the switching delays of the comparator. This inaccuracy is caused by an excessively short rise time of the voltage. A capacitance value too high gives rise to a charging time which is too long compared to the discharging time. An additional inaccuracy cause would be therefore present for the switching frequency, now due to the spread of the charge current.

The oscillation frequency is given by the following formula:

$$f_{osc} = \frac{1}{R_{OSC}\, C_{OSC}} \qquad (26)$$

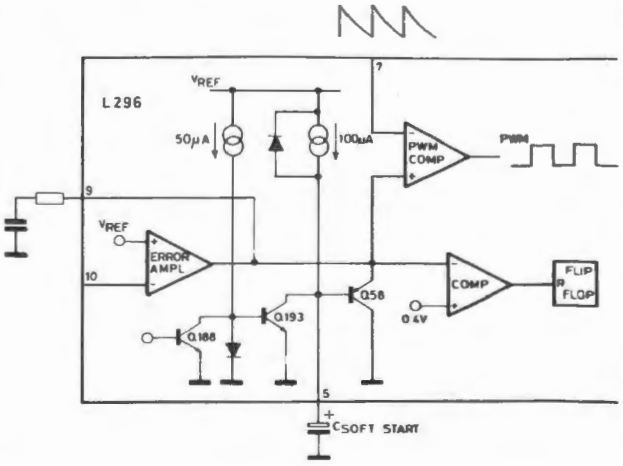
PWM (see Figure 30)

The PWM signal is generated on the comparator output; the triangular-shaped waveform and the continuous signal coming from the output of the transconductance error amplifier are sent to its inputs. The PWM signal is then transferred to the driving stage of the output power transistor.

Soft start (see Figure 30)

Soft start is an essential function for correct start-

Figure 30 **Partial internal schematic showing PWM and soft start blocks**



up, to prevent stresses and possible breakdown from occurring in the power transistor and to obtain a monotonically increasing output voltage.

In particular, the L296, as it does not have any duty cycle limitation and due to the type of current limitation does not allow the output to be forced to a steady state without the aid of the soft-start facility. Soft-start operates at the start-up of the system, after the inhibit has been activated, after an intervention of the current limit and after the intervention of the thermal protection.

The soft-start function is realised through a capacitor connected to pin 5 which is charged at constant current ($\simeq 100\mu A$) up to a value of about V_{REF}. During the charging time, through PNP transistor Q58, the voltage on pin 9 is forced to increase with the same rising speed as on pin 5. Starting from the discharged capacitor condition (pin 5 voltage = 0V) the power transistor is in the OFF condition, as the voltage on pin 9 is smaller than the minimum level of the ramp voltage. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp; the power stage starts to switch with steadily increasing duty cycle. The behaviour is shown in Figure 31. As soon as the steady condition is reached the duty cycle sets itself to the right value due to the effect of the feedback network while the soft-start capacitor completes its charging to a value very close to V_{REF}.

The soft-start effect is set to keep the mean value of the current absorbed by the power supply low, during overloads or short circuits and also to set the switch-on time.

Moreover from Figure 32 it may be observed that since the voltage on pin 9 can decrease under the minimum ramp level and increase over the maximum level no limitations have been provided on the duty cycle, which therefore may vary between 0 and 100%.

Figure 31 **Soft-start waveforms. When power is applied, or after an inhibit, the L296's output current rises slowly under the control of the soft start circuit**

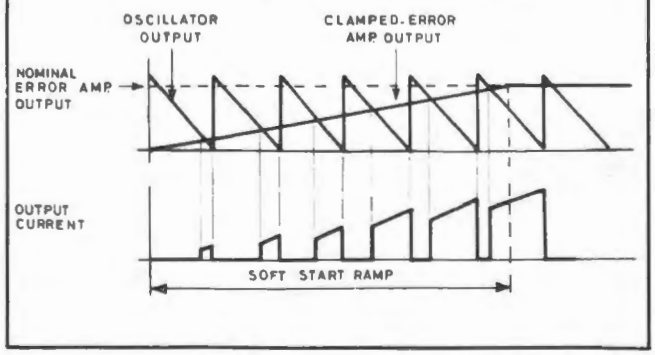
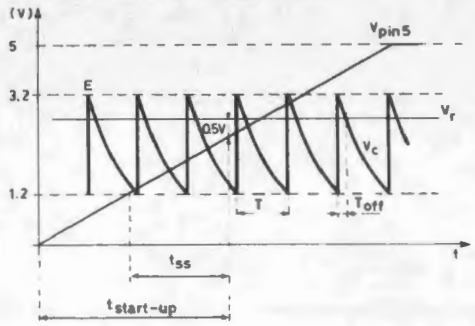


Figure 32 **Waveform for calculation of duty cycle and soft start time**



Calculating the duty cycle and soft-start time

Assume, for simplicity, that the rising edge of the ramp is instantaneous; V_r is the output voltage of the error amplifier and V_c the ramp voltage (see Figure 32). The PWM comparator block switches when $V_r = V_c$; therefore:

$$V_r = V_c = E \times e^{-\frac{t}{R_{osc} C_{osc}}}$$

Consequently:

$$t = R_{osc} C_{osc} \ln\left(\frac{E}{V_r}\right)$$

The time obtained from this expression is the T_{OFF} time of the power transistor. The duty cycle d is given by:

$$d = \frac{T_{ON}}{T} = \frac{T - R_{osc} C_{osc} \ln\left(\frac{E}{Vr}\right)}{T} = \quad (1)$$

$$= 1 - \frac{R_{osc} C_{osc}}{T} \ln\left(\frac{E}{V_r}\right) = \frac{V_o}{V_i}$$

Consequently, starting with the capacitor discharged, the output of the regulator will be at the nominal level when the voltage at the terminal of the capacitor (which is charged by a constant current) has reached $V_r - 0.5V$.

$$t\ start\text{-}up = \frac{C_{SS}\,(V_r - 0.5V)}{I_{5so}}$$

where C_{SS} is the soft-start capacitor and I_{5SO} is the charging current.

Considering as the soft-start time the time required for the soft-start capacitor to charge from 1.2V to $V_r - 0.5V$, gives:

$$t_{ss} = \frac{C_{SS}\,(V_r - 0.5 - 1.2)}{I_{5so}} \quad (2)$$

substituting V_r from (1) gives:

$$V_r = E \times e^{-\frac{T}{R_{osc} C_{osc}} \left[1 - \left(\frac{V_o}{V_i}\right)\right]}$$

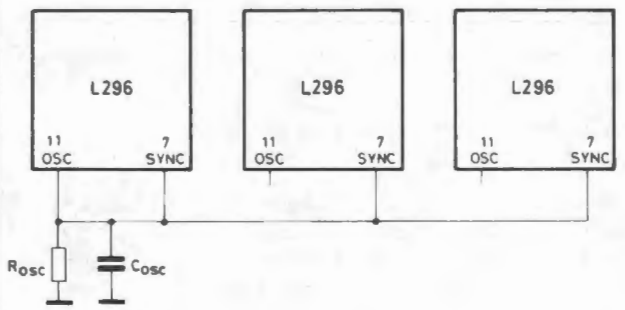
substituting into (2) gives:

$$t_{ss} = \frac{C_{SS}}{I_{5so}}\ E \times e^{-\frac{T}{R_{osc} C_{osc}} \left[1 - \left(\frac{V_o}{V_i}\right)\right]} - 1.7$$

Synchronization

The synchronization function is available on pin 7, this function allows the device to be switched at an externally generated frequency (leaving pin 11 open), or to mutually synchronise several devices, using one of them as master and the others as slave (Figure 33).

Figure 33 **In multiple supplies several L296's can be synchronized as shown here**



This allows several devices to be operated at the same frequency, avoiding undesirable intermodulation phenomena. The number of mutually synchronisable devices may be more than the three devices shown in the figure. It is difficult to establish an exact maximum number of devices, as it depends on a number of different conditions.

The first consideration concerns the accuracy which must be achieved and maintained on the oscillation frequency. Since the bias current on pin 7 is an output current, the sum of all the bias currents must be much smaller than the capacitor discharge current in close proximity to the lower discharge threshold. Therefore, assuming C_{OSC} = 2.2nF and R_{OSC} = 4.3kΩ, it follows that:

$$\frac{1.2V}{4.3k\Omega} = 280\mu A$$

Assuming that a 10% variation may be accepted, it follows therefore that the number of synchronizable devices is given by:

$$N = \frac{28\mu A}{I_{bias\ max}}$$

This means that if the overall I_{bias} is too high it may modify the discharging time of the capacitor.

The second consideration concerns the layout design.

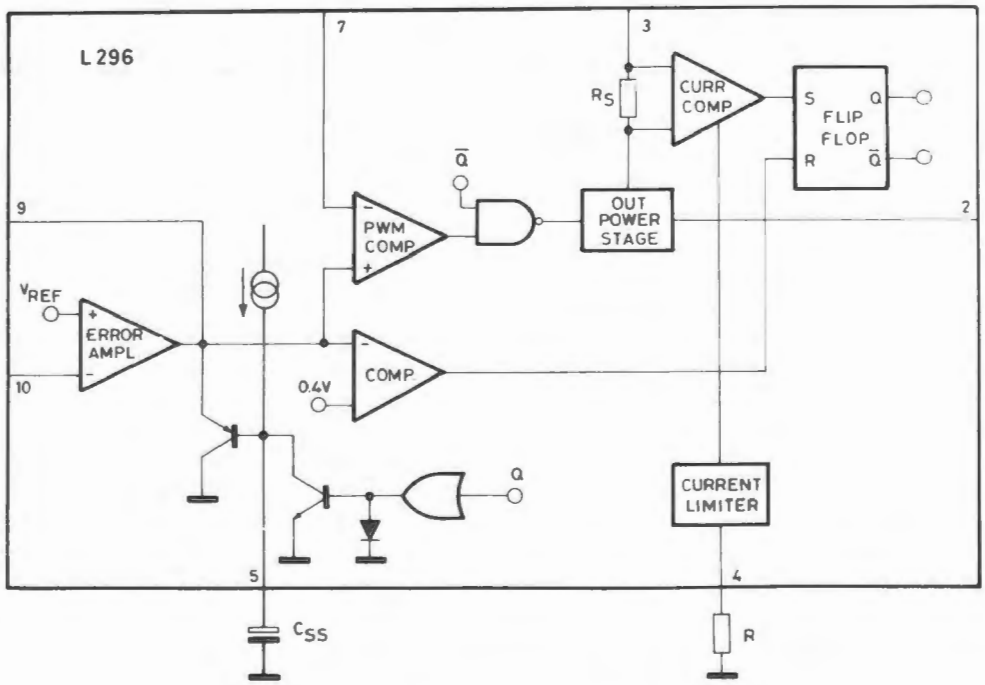
In the presence of a great number of devices to be synchronized, the combined length of the paths may become significant and therefore the distributed inductance introduced along the paths may begin to modify the triangular shaped waveform, particularly the rising edge which is very steep. This effect would affect the devices that are physically located more distant from the master device.

The amplitude of the saw-tooth to be externally connected must be within 0.5V and 3.5V, values also representing the maximum swing of the error amplifier output.

Current limitation

The current limitation function has been realised in a rather innovative way to avoid overload condition during the short circuit operation. In fact, while for all the other devices a constant current limitation is implemented by acting on the duty cycle (therefore, in short circuit conditions the output current is equal to the maximum limitation current), the new control approach allows operation in short circuit conditions with a mean current much smaller than the allowed 4A value. Operation of the current limiter will now be described. Refer to the block diagram, Figure 34.

Figure 34 **Partial schematic showing the current limiter circuit**



The current which is delivered from the output transistor to the load flows through the current sensing resistor R_S. When the voltage drop on R_S is equal to the offset voltage of the current comparator, the comparator generates a set pulse for the flip-flop, with a delay of about 1μsec. The purpose of this delay is to avoid triggering the protection circuit on the current peak that occurs during the recirculation phase. Therefore, the output $\overline{Q}$ goes low and the power stage is immediately switched off, while the output Q goes high and acts directly on the soft-start capacitor discharging the soft-start capacitor at a constant current (about 50μA).

When the voltage on pin 5 reaches 0.4V the comparator triggers, supplying a reset pulse to the flip-flop; from now on, the power stage is enabled and the soft-start phase starts again. When the limitation cause, either overload or short circuit, is still present the cycle repeats again. The waveform of the output current on pin 2 is shown in Figure 35c.

From Figure 35 it may be observed this current limitation technique allows the short circuit operation with a very low output current value.

By inserting a resistor between pin 4 and ground, the offset voltage of the current comparator is reduced thereby lowering the triggering threshold. A 22kΩ resistor in series with a 100kΩ variable resistor will allow the current to be reduced to 2.5A. The variable resistor will allow for production tolerances.

Figure 35a **Current limiter waveforms**

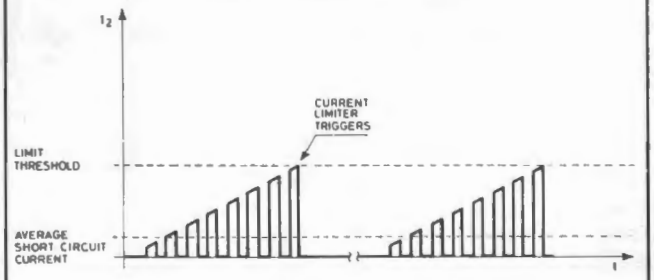


Figure 35b **Load current in short circuit conditions (V_i = 40V, L = 300μH, f = 100kHz)**

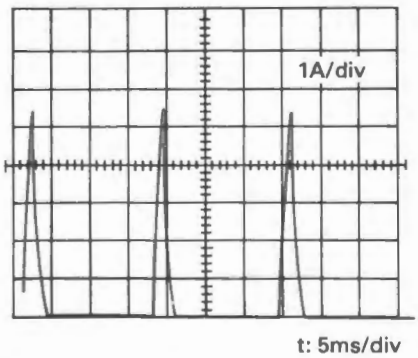
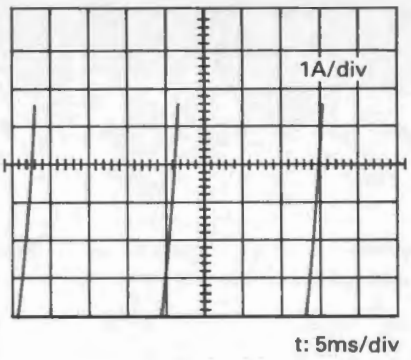


Figure 35c **Current at pin 2 when the output is short circuited**



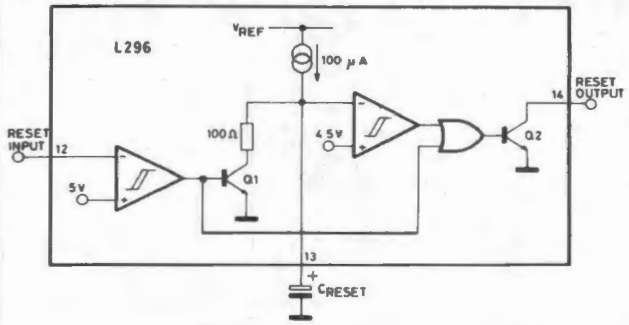
Reset

The reset function is of great importance when the device is used to supply microprocessors, logic devices, and so on. This function differentiates the L296 device from all previous devices. The block diagram of the function is shown in Figure 36. A reset signal is generated when the output voltage is within the limits required to supply the microprocessor correctly.

The reset function is realised through the use of 3 pins: the reset input pin 12, the reset delay pin 13 and the reset output pin 14. When the voltage on pin 12 is smaller than 5V the comparator output is high and the reset capacitor is not charged because the transistor Q is saturated and the voltage on pin 14 is at low level, since Q2 is also saturated. When the voltage on pin 12 goes above 5V, the transistor Q switches OFF and the capacitor can start to charge through a current generator of about 100μA. When the voltage on pin 13 goes above 4.5V the output of the related comparator switches low and the pin 14 goes high. As the output consists of an open collector transistor, a pull-up resistor is required. In contrast, when the reset input voltage goes below 5V, less an hysteresis voltage of about 100mV, the comparator triggers again and instantaneously sets the voltage on pin 14 low, therefore forcing to saturation the Q1 transistor, that starts the rapid discharge of the capacitor. Obviously, the reset delay is again present when the voltage on pin 13 is allowed to go under 4.5V.

To achieve switching operations without uncertainties the two comparators have been provided with an hysteresis of about 100mV. In every operating condition the reset switching is guaranteed with a minimum reset input of 4.75V, the value required for correct operation of the microprocessor even in the presence of the minimum V_{REF} value.

Figure 36 **Partial schematic showing reset circuit**



Normally pin 12 is used connected to pin 10. When it is connected to the output, the function may be more properly called 'reset'; on the other hand, when it is connected through a resistive divider, to the input voltage, the function is called 'power fail'. Figure 37 and Figure 38 show the two possible usages.

Figure 37 **For power – on reset the reset block is connected as shown here**

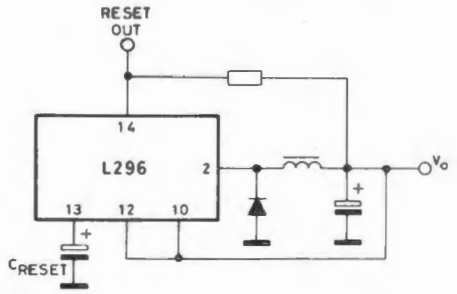
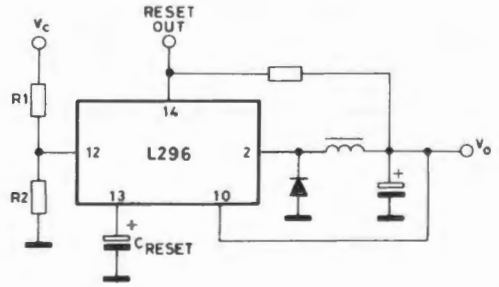
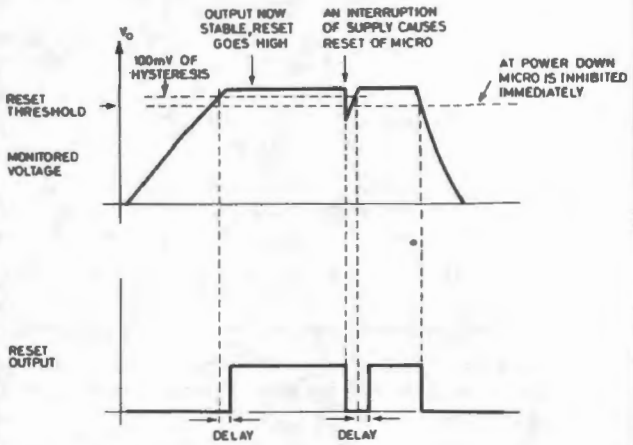


Figure 38 **To obtain a power fail signal, the reset block is connected like this**



The 'power-fail' function is used to predict, with a given advance, the drop of the regulator output voltage, due to mains failures, which is sufficient to save the data being processed into protected memory areas. Figure 39 summarises the reset function operation.

Figure 39 **Waveform of the reset circuit**



Crowbar

This protection function is realised by a completely independent block, using pin 1 as input and pin 15 as output. It is used to prevent dangerous overvoltages from occurring when the output exceeds 20% of rated value. Pin 15 is able to output a 100mA current to the gate of an SCR which when triggered, short circuits either the output or the input. When connected to the input, as the SCR is triggered a fuse connected in series to the power supply is blown and to bring the system back to operation manual intervention is required. Figures 40, 41 and 42 show the different configurations.

When the voltage on pin 1 exceeds by about 20% the V_{REF} value the output stage is activated, which sends a current to the SCR gate, after a delay of about 5μsec to make the system insensitive to low-duration spikes. When activated, the output stage delivers about 100mA; when not activated, it drains about 5mA and shows a low impedance to the SCR gate to avoid incorrect triggering due to random noise. If the crowbar function is not used connect pin 1 to ground.

Figure 40 **Connection of crowbar circuit at output for 5.1V output applications**

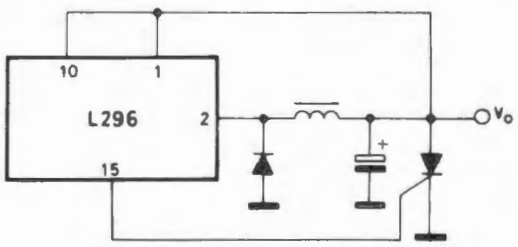


Figure 41 **Connection of crowbar circuit at output for output voltages above 5.1V**

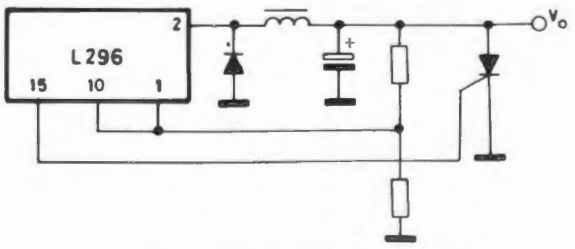
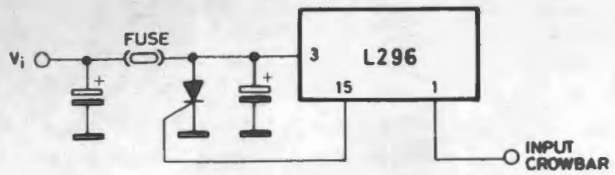


Figure 42 **Connection of crowbar circuit to protect input. When triggered, the SCR blows the fuse**



Thermal protection

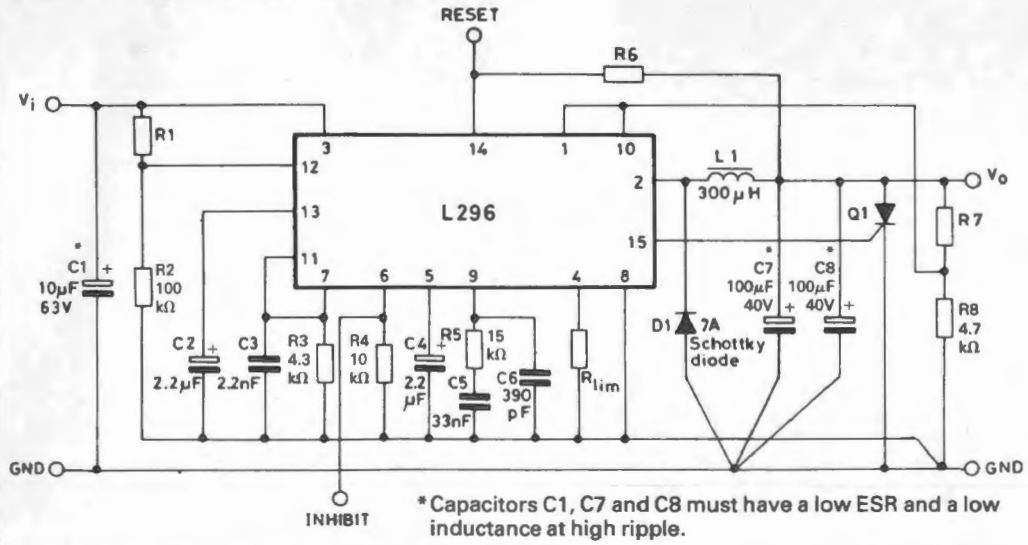
The thermal protection function operates when the junction temperature reaches 150°C; it acts directly on the power stage, immediately switching it off, and also on the soft-start capacitor, discharging it. The thermal protection is provided with hysteresis and, therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease to about 30%C below the intervention threshold.

Inhibit

The inhibit input (pin 16) is TTL compatible and is activated when the voltage exceeds 2V and deactivated when the voltage goes under 0.8V. As may be seen in the block diagram, the inhibit acts on the power transistor, instantaneously switching it off and also acts on the soft-start, discharging its capacitor. When the function is unused, pin 6 must be grounded.

Applications information

Figure 43 **Typical application circuit**



*Capacitors C1, C7 and C8 must have a low ESR and a low inductance at high ripple.

Resistor values for standard output voltages

V_o	R8	R7
12V	4.7kΩ	6.2kΩ
15V	4.7kΩ	9.1kΩ
18V	4.7kΩ	12kΩ
24V	4.7kΩ	18kΩ

Selection of component values (See Figure 43)

Component	Recommended value	Purpose	Allowed range Min.	Allowed range Max.	Notes
R1 R2	– 100kΩ	Set input voltage threshold for reset	–	 220kΩ	$R1/R2 = \frac{V_{i\,min}}{5} - 1$ If output voltage is sensed, R1 and R2 may be limited and pin 12 connected to pin 10.
R3	4.3kΩ	Sets switching frequency	1kΩ	100kΩ	
R4	10kΩ	Pull-down resistor		22kΩ	May be omitted and pin 6 grounded if inhibit not used.
R5	15kΩ	Frequency compensation	10kΩ		
R6		Collector load for reset output	$\frac{V_o}{0.05A}$		Omitted if reset function not used
R7 R8	– 4.7kΩ	Divider to set output voltage	– –	– 10kΩ	$R7/R8 = \frac{V_o - V_{ref}}{V_{ref}}$
R_{lim}	-	Sets current limit level			If R_{lim} is omitted and pin 4 left open the current limit is internally fixed.

Selection of component values (cont)

Component	Recommended value	Purpose	Allowed range Min.	Max.	Notes
C1	10μF	Stability	1μF		
C2	2.2μF	Sets reset delay	–	–	Omitted if reset function not used.
C3	2.2nF	Sets switching frequency	1nF	3.3nF	
C4	2.2μF	Soft start	1μF	–	Also determines average short circuit current.
C5	33nF	Frequency compensation			
C6	390pF	High frequency compensation	–	–	Not required for 5V operation
C7, C8 L1	100μF 300μH	Output filter			
Q1		Crowbar protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.
D1		Recirculation diode			7A Schottky or high efficiency diode in D0220 package

Choosing the inductor and capacitor

The input and output capacitors of the L296 must have a low ESR and low inductance at high current ripple.

The inductor must not saturate at current levels below 1.5 times the current limiter levels. Preferably this will be wound on a core having very soft saturation characteristics.

$$L = \frac{(V_i - V_o)\,V_o}{V_i\, f\, \Delta I_L}$$

$$C = \frac{(V_i - V_o)\,V_o}{8L\, f^2\, \Delta V_o}$$

f = frequency

ΔI_L = Inductance current ripple

ΔV_o = Output ripple voltage

The step-down configuration

Figure 44 shows the simplified block diagram of the circuit realising the step-down configuration. This circuit operates as follows: Q1 acts as a switch at the frequency f and the ON and OFF times are suitably controlled by the pulse width modulator circuit. When Q1 is saturated, energy is absorbed from the input which is transferred to the output through L. The emitter voltage of Q1, V_E, is Vi-Vsat when Q is ON and $-V_F$ (with V_F the forward voltage across the D diode as indicated) when Q1 is OFF. During this second phase the current circulates again through L and D1. Consequently a rectangular-shaped voltage appears on the emitter of Q1 and this is then filtered by the L-C-D network and converted into a continuous mean value across the capacitor C and therefore across the load. The current through L consists of a continuous component, I_{LOAD}, and a triangular-shaped component superimposed on it, ΔI_L, due to the voltage across L.

Figure 44 **The basic step-down switching regulator configuration**

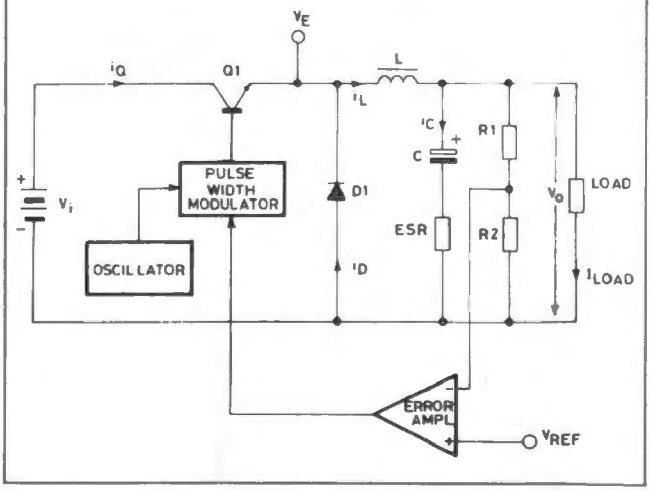


Figure 45 **Principal circuit waveforms**

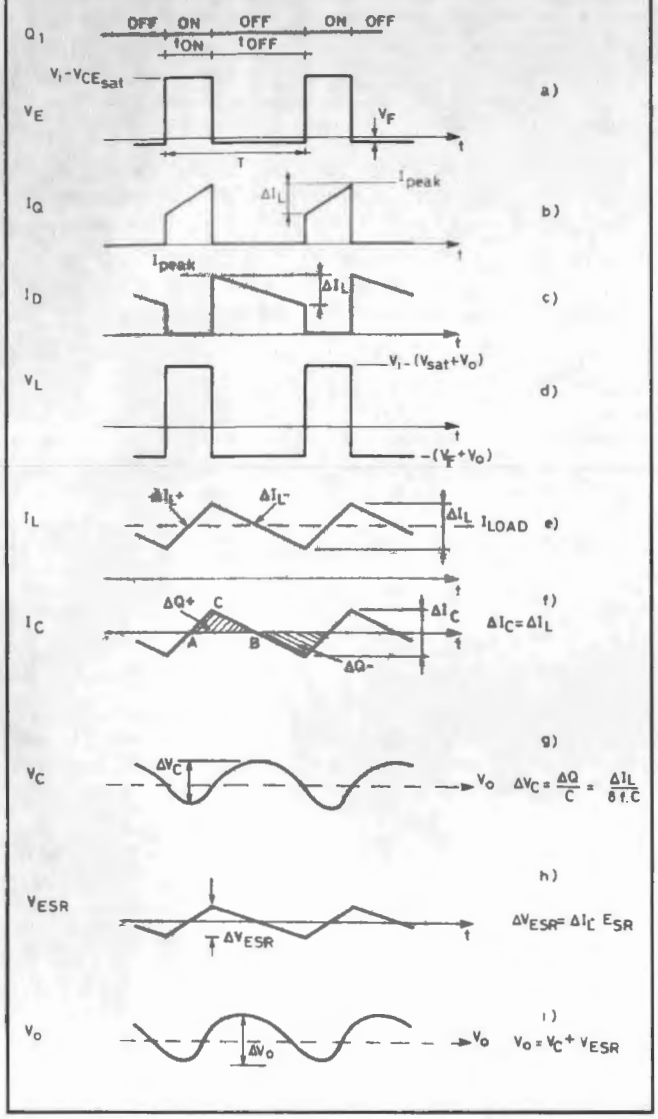


Figure 45 shows the behaviour of the most significant waveforms, in different parts of the circuit, which help to understand better the operaton of the power section of the switching regulator. For the sake of simplicity, the series resistance of the coil has been ignored. Figure 45a shows the behaviour of the emitter voltage (which is practically the voltage across the recirculation diode), where the power saturation and the forward V_F drop across the diode are taken into account.

The ON and OFF times are established by the following expression:

$$V_O = (V_i - V_{sat}) \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

Figure 45b shows the current across the switching transistor. The current shape is trapezoidal and the operation is in continuous mode. At this stage, the phenomena due to the catch diode, that we consider as dynamically ideal, are ignored. Figure 45c shows the current circulating in the recirculation diode. The sum of the currents circulating in the transistor Q_1 and in the diode D_1 is the current circulating in the coil as shown in Figure 45e. In balanced conditions the ΔI_L + current increase occurring during T_{ON} has to be equal to the ΔI_L^- decrease occurring during T_{OFF}. The mean value of I_L corresponds to the charge current.

The current ripple is given by the following formula:

$$\Delta I_L^+ = \Delta I_L^- = \frac{(V_i - V_{sat}) - V_o}{L} T_{ON} = \frac{V_o + V_F}{L} T_{OFF}$$

It is a good rule to respect the $Io_{MIN} \geq I_L/2$ relationship, that implies good operation in continuous mode. When this is not done, the regulator starts operating in discontinuous mode. This operation is still safe but variations of the switching frequency may occur and the output regulation decreases.

Figure 45d shows the behaviour of the voltage across coil L. In balanced conditions, the mean value of the voltage across the coil is zero. Figure 45f shows the current flowing through the capacitor, which is the difference between I_L and I_{LOAD}.

In balanced conditions, the mean current is equal to zero, and $\Delta I_C = \Delta I_L$. The current I_C through the capacitor gives rise to the voltage ripple.

This ripple consists of two components: a capacitive component, ΔV_C, and a resistive component, ΔV_{ESR}, due to the ESR equivalent series resistance of the capacitor. Figure 45g shows the capacitive component ΔV_C of the voltage ripple, which is the integral of a triangular-shaped current as a function of time. Moreover, it should be observed that v_C (t) is in quadrature with i_C(t) and therefore with the voltage V_{ESR}. The quantity of charge ΔQ^+ supplied to the capacitor is given by the area enclosed by the ABC triangle in Figure 45f.

$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2}$$

which therefore gives:

$$\Delta V_C = \frac{Q}{C} = \frac{\Delta I_L}{8fc}$$

Figure 45h shows the voltage ripple V_{ESR} due to the resistive component of the capacitor. This component is V_{ESR} (t) = i_C (t). ESR. Figure 45i shows the overall ripple V_O, which is the sum of the two previous components. As the frequency increases (>20kHz), which is required to reduce both the cost and the sizes of L and C, the V_{ESR} component becomes dominant. Often it is necessary to use capacitors with greater capacitance (or more capacitors connected in parallel to limit the value of ESR within the required level.

We will now examine the stepdown configuration in more detail, referring to Figure 44 and taking the behaviour shown in Figure 45 into account.

Starting from the initial conditions, where Q = ON, $V_C = V_O$ and $i_L = i_D = 0$, using Kirchoff's second principle we may write the following expression:

$V_i = v_L + v_C$ (Vsat is neglected against V_i).

$$V_i = L \frac{di_L}{dt} + v_C = L \frac{di_L}{dt} + V_o \qquad (1)$$

which gives:

$$\frac{di_L}{dt} = \frac{(V_i - V_o)}{L} \qquad (2)$$

The current through the inductance is given by:

$$I_L = \frac{(V_i - V_o)}{L} t \quad (3)$$

When V_i, V_o, and L are constant, I_L varies linearly with t. Therefore, it follows that:

$$\Delta I_L + = \frac{(V_i - V_o) T_{ON}}{L} \quad (4)$$

When Q is OFF the current through the coil has reached its maximum value, I_{peak} and because it cannot vary instantaneously, the voltage across the coil is inverted and the diode D1 becomes forward biased to allow the recirculation of the current through the load.

When Q switches OFF, the following situation is present:

$v_C(t) = V_o$, $i_L(t) = i_D(t) = I_{peak}$

And the equation associated to the following loop may be written:

$$V_F + L\frac{di_L}{dt} + v_C = 0 \quad (5)$$

where:

$v_C = V_o$

$$\frac{di_L}{dt} = -(V_F + V_o)/L \quad (6)$$

It follows therefore that:

$$i_L(t) = -\frac{V_F + V_o}{L} t \quad (7)$$

The negative sign may be interpreted with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_O, during the OFF time the following behaviour occurs:

$$I_L = \frac{V_O}{L} t \quad (8)$$

therefore:

$$\Delta I_L^- = \frac{V_O}{L} T_{OFF} \quad (9)$$

But, because

$\Delta I_L^+ = \Delta I_L^-$, it follows that:

$$\frac{(V_i - V_o) T_{ON}}{L} = \frac{V_O T_{OFF}}{L}$$

which allows us to calculate V_o:

$$V_o = Vi \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_i \frac{T_{ON}}{T} \quad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_o to the input voltage V_i and to the duty cycle. The relationship between the currents is the following:

$$I_{iDC} = I_{oDC} \cdot \frac{T_{ON}}{T}$$

Efficiency

The system efficiency is expressed by the following formula:

$$\eta\% = \frac{P_o}{P_i} 100$$

where $P_o = V_o I_o$ (with $I_o = I_{LOAD}$)

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_o, plus all the other system losses. The expression of the efficiency becomes therefore the following:

$$\eta = \frac{P_o}{P_o + P_{sat} + P_D + P_L + P_q + p_{sw}} \quad (12)$$

dc losses

P_{sat}: saturation losses of the power transistor Q1. These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot 1_o \frac{T_{ON}}{T} = V_{sat} I_o \frac{V_o}{V_i} \quad (13)$$

where $\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ and V_{sat} is the power transistor saturation at current I_O.

P_D: losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F I_o \frac{V_i - V_o}{V_i} = V_F I_o \left(1 - \frac{V_o}{V_i}\right) \quad (14)$$

where V_F is the forward voltage of the recirculation diode at current I_O.

P_L: losses due to the series resistance R_S of the coil

$$P_L = R_S I_o^2 \quad (15)$$

P_q: losses due to the standby current and to the power driving current:

$$P_q = V_i I'_{3q} + V_i I''_{3q} \frac{T_{ON}}{T} \quad (16)$$

where being:

$\frac{T_{ON}}{T} = \frac{V_o}{V_i}$ it follows that:

$P_q = V_i I'_{3q} + V_o I''_{3q}$ in which:

$I'_{3q} = I_{3q}$ at 0% duty cycle

$I''_{3q} = I_{3q}(100\%\ dc) - I_{3q}(0\%\ dc)$

Switching losses

p_{SW}: switching losses of the power transistor:

$$p_{SW} = V_i I_o \frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are neglected (which are anyway negligible) as it is assumed that diode is used with recovery time much smaller than the rise time of the power transistor.

We can neglect losses in the coil (it is assumed that ΔI_L is very small compared to I_o) and in the output capacitor, which is assumed to show a low ESR.

Calculation of the inductance value, L

Calculating T_{ON} and T_{OFF} through (4) and (9) respectively it follows that:

$$T_{ON} = \frac{\Delta I_L^+ \cdot L}{V_i - V_o} \qquad T_{OFF} = \frac{\Delta I_L^- \cdot L}{V_o}$$

but because:

$T_{ON} + T_{OFF} = T$ and $\Delta I_L^- = \Delta I_L^- = \Delta I_L$,

it follows that:

$$\frac{\Delta I_L \cdot L}{V_i - V_o} + \frac{\Delta I_L \cdot L}{V_o} = T$$

Calculating L, the previous relation becomes:

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, \Delta I_L} T \qquad (18)$$

Fixing the current ripple in the coil required by the design (for instance 30% of I_o), and introducing the frequency instead of the period, it follows that:

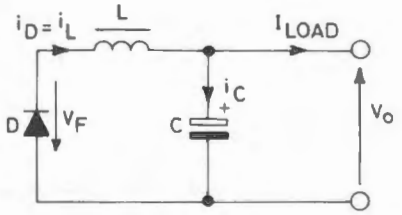
$$L = \frac{(V_i - V_o)\, V_o}{V_i \cdot 0.3 \cdot I_o \cdot f}$$ where L is in Henrys and f in Hz

Calculation of the output capacitor C

From the output node in Figure 46 it may be seen that the current through the output capacitor is given by:

$i_c(t) = i_L(t) - I_o$

Figure 46 **Equivalent circuit showing recirculation when Q_1 is turned off**



From the behaviour shown in Figure 45 it may be calculated that the charge current of the output capacitor, within a period, is $\Delta I_L/4$, which is supplied for a time T/2. It follows therefore that:

$$\Delta V_C = \frac{\Delta I_L}{4C} \frac{T}{2} = \frac{\Delta I^2 L\, T}{8C} = \frac{\Delta I_L}{8fC} \qquad (19)$$

but, remembering expression (4):

$$\Delta I_L^+ = \frac{(V_i - V_o)\, T_{ON}}{L}$$ and $T_{ON} = \frac{V_o}{V_i} T$

therefore equation (19) becomes:

$$\Delta V_C = \frac{(V_i - V_o)\, V_o}{8\, V_i\, f^2\, L\, C}$$

Finally, calculating C it follows that:

$$C = \frac{(V_i - V_o)\, V_o}{8\, V_i\, \Delta V_C\, f^2\, L} \qquad (20)$$

where: L is in Henrys
C is in Farads
f is in Hz

Finally, the following expression should be true:

$$ESR_{max} = \frac{\Delta V_{Cmax}}{\Delta I_L} \qquad (21)$$

It may happen that to satisfy relation (21) a capacitance value much greater than the value calculated through (20) must be used.

Transient response

Sudden variations of the load current give rise to overvoltages on the output voltage. Since $i_c = C\,(dv_c/dt)$ (22), where $dv_c = \Delta V_o$, the instantaneous variation of the load current ΔI_o is supplied during the transient by the output capacitor. During the transient, also current through the coil tends to change its value.

Moreover, the following is true:

$$v_L = L \frac{di_L}{dt}$$ (23) where $di_L = \Delta I_o$.

$v_L = V_i - V_o$ for a load increase

$v_L = V_o$ for a load decrease

Calculating dt from (22) and 23 and equalising, it follows that:

$$L \frac{di_L}{v_L} = C \frac{dv_c}{i_c}$$

Calculating dv_c and equalising it to ΔV_o, it follows that:

$$\Delta V_o = \frac{L\, \Delta I_o^2}{C(V_i - V_o)} \qquad (24) \qquad \text{for} + \Delta I_o$$

$$\Delta V_o = \frac{L\, \Delta I_o^2}{C\, V_o} \qquad (25) \qquad \text{for} + \Delta I_o$$

From these two expressions the dependence of overshoots and undershoots on the L and C values may be observed. To minimise ΔV_o it is therefore necessary to reduce the inductance value L and to increase the capacitance value C. Should other auxiliary functions be required in the circuit like reset or crowbar protections with variable loads, it is worthwhile to take special care for minimising these overshoots, which could cause spurious operation of the crowbar, and the undershoot, which could trigger the reset function.

Layout considerations

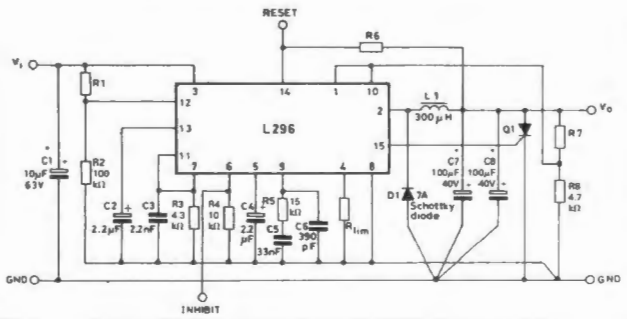
Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes important to achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are overimposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

When operating at high frequencies the path length becomes extremely important. The paths introduce distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to pin 2, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

Figure 47 shows the earthing arrangement. Greater care must be taken to follow these rules when two or more mutually synchronised devices are used.

Figure 47 **Typical application circuit showing how the signal and power grounds are connected**

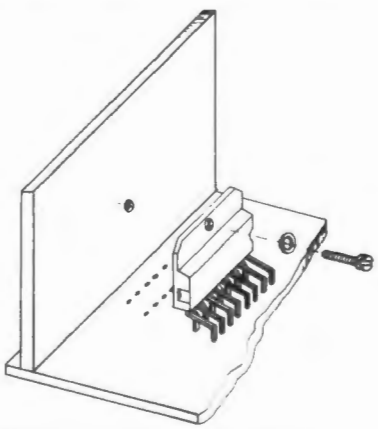


Mounting instructions

The power dissipated in the circuit must be removed by adding an external heatsink.

The Multiwatt® package enables simple attachment to the heatsink, a single screw being sufficient. Between the heatsink and the package it is better to insert a layer of heatsink compound, to optimise the thermal contact; no electrical isolation is needed between the two surfaces.

Figure 48 **Mounting example**



Heatsink dimensioning

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150°C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150°C for long periods or of more than 170°C for short periods. In any case the temperature accelerates the ageing process and therefore influences the device life; an increase of 10°C can halve the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Figure 48 shows the structure of a power device. As demonstrated in thermodynamics, a thermal circuit can be considered to be an electrical circuit where R_1, R_2 represent the thermal resistance of the elements (expressed in °C/W) (see Figure 49).

Figure 49

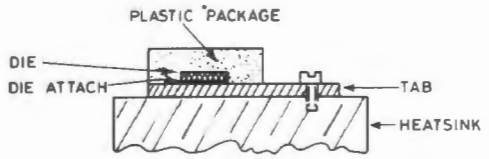
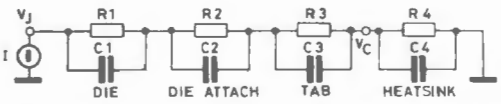


Figure 50



C1, C2 are the thermal capacitance (expressed in J/°C)

I is the dissipated power

V is the temperature difference with respect to the reference (ground)

This circuit can be simplified as shown in Figure 51, where:

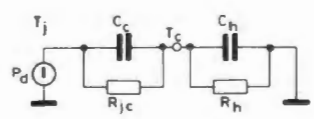
C_C is the thermal capacitance of the die plus that of the tab.

C_h is the thermal capacitance of the heatsink

R_{jc} is the junction case thermal resistance

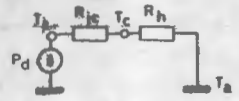
R_h is the heatsink thermal resistance

Figure 51



But for steady state the circuit can be further reduced as shown in Figure 52.

Figure 52



If we now consider the ground potential as ambient temperature, we have:

$$Tj = T_a + (R_{jc} + R_h)\,P_d \qquad a)$$

$$Rh = \frac{T_j - T_a - R_{jc}\,P_d}{P_d} \qquad b)$$

$$T_c = T_a + R_h\,P_d \qquad c)$$

Thermal contact resistance depends on various factors such as the mounting, contact area and planarity of the heatsink. With no material between the device and heatsink the thermal resistance is around 0.5°C/W; with heat sink compound roughly 0.3°C/W and with heat sink compound plus a mica insulator about 0.4°C/W. See Figure 53. In applications where one external transistor is used on the same heatsink, the dissipated power must be calculated for each component. The various junction temperatures can be calculated by solving the circuit shown in Figure 54. This applies if the dissipating elements are fairly close with respect to the dissipator dimensions, otherwise the dissipator can no longer be considered as a concentrated constant and the calculation becomes difficult. This concept is better explained by the graph in Figure 55 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of heatsink and the same dissipated power. The graph in Figure 55 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the total dissipated power and on the devices geometrical positions. We want to show that there exists an optimal position between the two devices:

$$d = \frac{1}{2} \times \text{side of the plate}$$

Figure 53

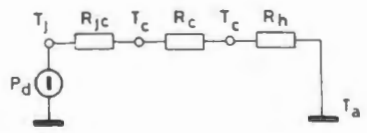


Figure 54

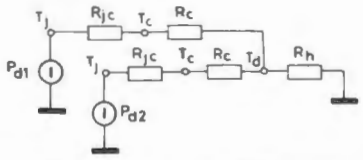


Figure 56 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4). This graph may be useful in application with two L296s synchronised.

Figure 55

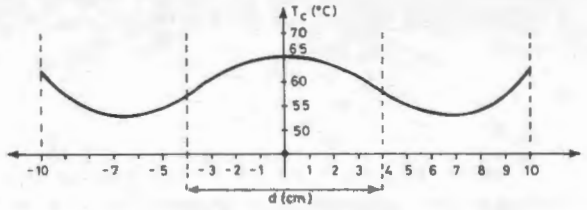
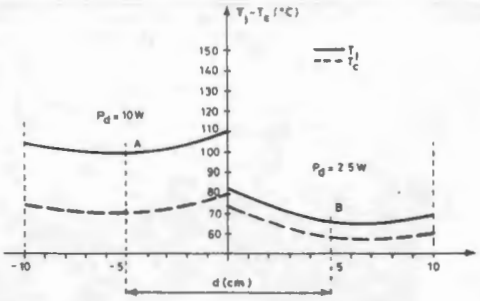


Figure 56



Appendix A:

Calculating system stability

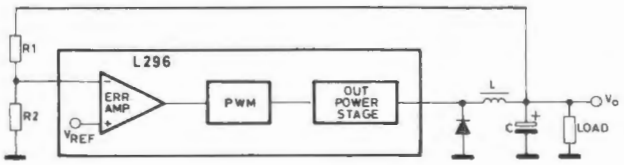
This section is intended to help the designer in the calculation of the stability of the whole system.

Figure 57 shows the entire control system of the switching regulator.

The problem which arises immediately is the transfer function of the PWM block and output stage, which is non-linear. If this function can be considered linear the analysis is greatly simplified.

Since the circuit operates at a constant frequency and the internal logic is fairly fast, the error introduced by assuming that this function is linear is minimised. Factors which could contribute to the non-linearity are an excessive delay in the output power transistor, ringing the parasitic oscillations generated in the power stage and non-linearity introduced by the inductor.

Figure 57 **The control loop of the switching regulator**



In the case of the L296, in which the power transistor is internal and driven by well-controlled and efficient logic, the contribution to non-linearity is further reduced.

For the assumption of linearity to be valid the cutoff frequency of the LC filter must be much lower than the switching frequency. In fact, switching opera-

tion introduces singularities (poles) at roughly half the switching frequency. Consequently, as long as the LC filter is still dominant, its cut-off frequency must be at least an order of magnitude lower than the switching frequency. This condition is not, however, difficult to respect.

Gain of the PWM block and output stage

The equation which links V_o to V_i is:

$$V_o = V_i \frac{T_{ON}}{T}$$

A variation ΔT_{ON} in the conduction time of the switching transistor causes a corresponding variation in the output voltage, ΔV_o, giving:

$$\frac{\Delta V_o}{\Delta T_{ON}} = \frac{V_i}{T}$$

Indicating with V_r the output voltage of the error amplifier, and with V_{ct} the amplitude of the ramp (the difference between the maximum and minimum values), T_{ON} is zero when V_r is at the minimum value and equal to T when V_r is at a maximum. Consequently:

$$\frac{\Delta T_{ON}}{\Delta V_r} = \frac{T}{V_{ct}}$$

The gain is given by:

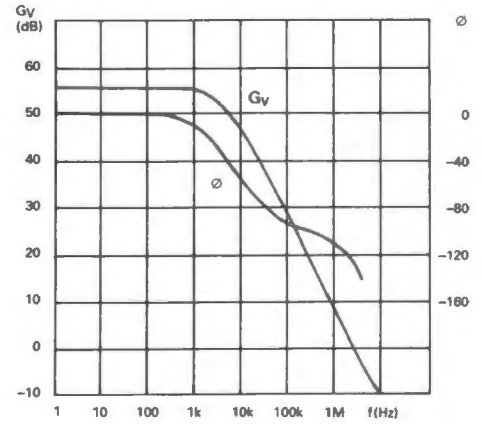
$$\frac{\Delta V_o}{\Delta V_r} = \frac{V_i}{V_{ct}}$$

Since V_{ct} is absolutely constant the gain of the PWM block is directly proportional to the supply voltage V_i.

Error amplifier

The error amplifier is a transconductance amplifier (it transforms a voltage variation at the input into a current variation at the output). It is used in an open loop configuration inside the main control loop and its gain and frequency response are determined by a compensation network connected between its output and ground.

Figure 58 **Open loop frequency and phase response of error amplifier**



In the application a series RC network is recommended which gives high system gain at low frequency – to ensure good precision and mains ripple rejection and a lower gain at high frequencies to ensure stability of the system. Figure 58 shows the gain and phase curves of the uncompensated error amplifier.

The amplifier has one pole at about 7kHz and a phase shift which reaches about – 90° at frequencies around 1MHz.

The introduction of a series network R_C C_C between the output and ground modifies the circuit as shown in Figure 59.

Figure 60 shows the gain and phase curves of the compensated error amplifier.

Figure 59 **Compensation network of the error amplifier**

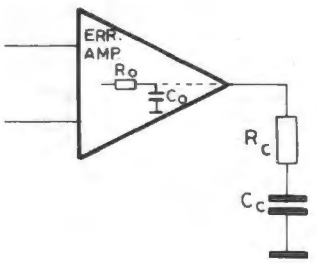
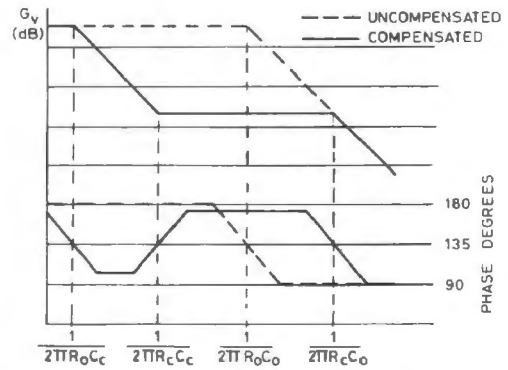


Figure 60 **Bode plot showing gain and phase of compensated error amplifier**



Calculating the stability

For the stability calculation refer to the block diagram shown in Figure 61.

The transfer functions of the various blocks are rewritten as follows.

The simplified transfer function of the compensated error amplifier is:

$$G_{EA} = g_m Z_c = g_m \frac{1 + s R_c C_c}{s C_C} \qquad (g_m = \frac{1}{2500})$$

The dc gain must be considered equal to

$$A_o = gm\, R_o$$

PWM block and output stage:

$$G_{PWM} = \frac{Vi}{V_{ct}}$$

LC filter:

$$G_{LC} = \frac{1 + s\,C \cdot ESR}{s^2\,LC + s\,C\,ESR + 1}$$

where ESR is the equivalent series resistance of the output capacitor which introduces a zero at high frequencies, indispensable for system stability. Such a filter introduces two poles at the angular frequency.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

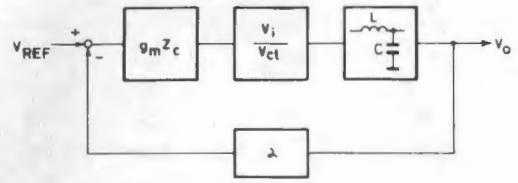
Feedback: consist of the block labelled α

$\alpha = 1$ when $V_o = V_{REF}$ (and therefore $V_o = 5.1V$)

and

$$\alpha = \frac{R_2}{R_1 + R_2} \text{ when } V_o > V_{REF}$$

Figure 61 **Block diagram used in stability calculation**



To analyse the stability we will use a Bode diagram. The values of L and C necessary to obtain the required regulator output performance, once the frequency is fixed, are calculated with the following formulae:

$$L = \frac{(V_i - V_o)\, V_o}{V_i\, f\, \Delta I_L}$$

$$C = \frac{(V_i - V_o)\, V_o}{8\, L\, f^2\, \Delta V_o}$$

Since this filter introduces two poles at the angular frequency

$$\omega o = \frac{1}{\sqrt{LC}}$$

we place the zero of the R_c C_c network in the same place:

$$\omega z = \frac{1}{R_c\, C_c}$$

Taking into account also the gain of the PWM block, the Bode plot of Figure 62 is obtained.

The slope where the curve crosses the axis at 0dB is about 40dB/decade therefore the circuit is unstable.

Taking into account now the zero introduced by the equivalent series resistance (ESR) of the output capacitor, we have a further condition for dimensioning the R_C C_C network. Knowing the ESR (see RS catalogue) we can determine the value of R_C so that the axis is crossed at 0dB with a single slope. The zero introduced by the ESR is at the angular frequency:

$$\omega\, zESR = \frac{1}{ESR \cdot C}$$

The overall Bode diagram is therefore as shown in Figure 63.

Figure 62 **Bode plot of system taking filter and compensation network into account**

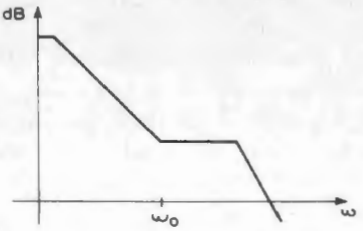
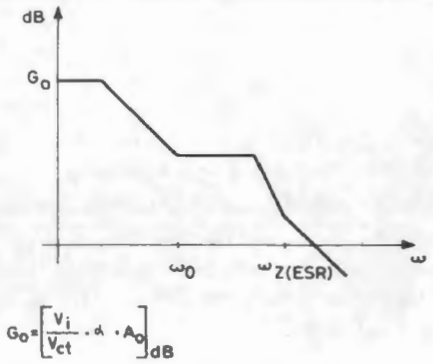


Figure 63 **Bode plot of complete system taking into consideration the equivalent series resistance of the capacitor**



dc gain and line regulation

Indicating the open-loop gain of the error amplifier with A_o, the overall open-loop gain of the system is:

$$A_t = A_o \frac{V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}$$

When $V_o = V_{REF}$, the gain becomes:

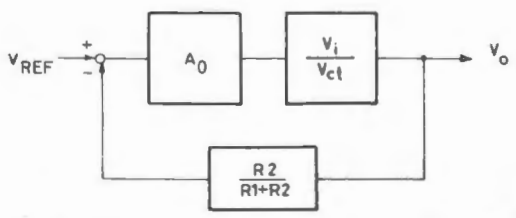
$$A_t = A_o \frac{V_i}{V_{ct}}$$

Considering the block diagram of Figure 64 and calculating the output variation ΔV_o caused by a variation of V_i, from the literature we obtain:

$$\frac{\Delta V_o}{V_o} = \frac{\dfrac{\Delta V_i}{V_i}}{\dfrac{A_o V_i}{V_{ct}} \cdot \dfrac{R_2}{R_1 + R_2}}$$

This expression is of general validity. In our case the percentage variation of the reference must be added by vector addition.

Figure 64 **Block diagram for calculation of line regulation**



Appendix B:
Reducing interference

The main disadvantage of the switching technique is the generation of interference which can reach levels which cause malfunctions and interfere with other equipment.

For each application it is therefore necessary to study specific means to reduce this interference within the limits allowed by the appropriate standards.

Among the main sources of noise are the parasitic inductances and capacitances within the system which are charged and discharged quickly. Parasitic capacitances originate mainly between the device case and the heatsink, the windings of the inductor and the connection wires. Parasitic inductances are generally found distributed along the strips of the printed circuit board.

Fast switching of the power transistors tends to cause ringing and oscillations as a result of the parasistic elements. The use of a diode with a fast reverse recovery time (trr) contributes to a reduction in the noise flowing by the current peak generated when the diode is reverse biased.

Radiated interference is usually reduced by enclosing the regulator in a metal box.

To reduce conducted electromagnetic interference (or radio frequency interferences – RFI) to the levels permitted a suitably dimensioned filter is added on the supply line. The best method, generally, to reduce conducted noise is to filter each output terminal of the regulator. The use of a fixed switching frequency allows the use of a filter with a relatively narrow bandwidth. For off-line switching regulators this filter is usually costly and bulky. In contrast, if the device is supplied from a 50/60Hz transformer the RFI filter problem is greatly reduced.

Tests have been carried out to determine the dimensions of a mains supply filter which satisfies the VDE 0871/6.78, class B standard. The measurements (see Figures 65 and 66) refer to the application with the L296 supplied with a filtered secondary voltage of about 30V, with V_o = 5.1V and I_o = 4A. The switching frequency is 100kHz.

Figure 65 shows the results obtained by introducing on the transformer primary a 0.01μF/250V~ class X capacitor. To reduce interference further below the limit set by the standards an additional inductive filter must be added on the primary of the transformer.

Figure 66 shows the curves obtained by introducing an inductive filter.

Measurements have also been performed beyond 30MHz; the maximum value measured is still well below the limit curve.

Figure 65 **EMI measurements with a capacitor connected across the primary transformer with screen grounded (A) and floating (B)**

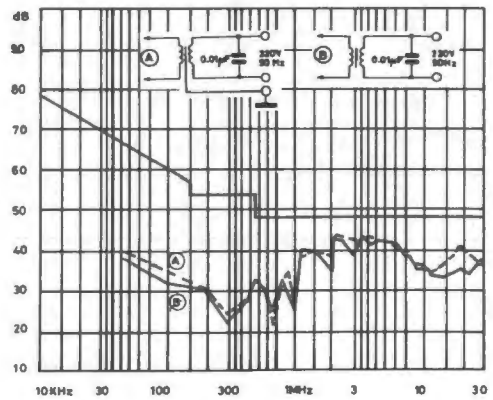
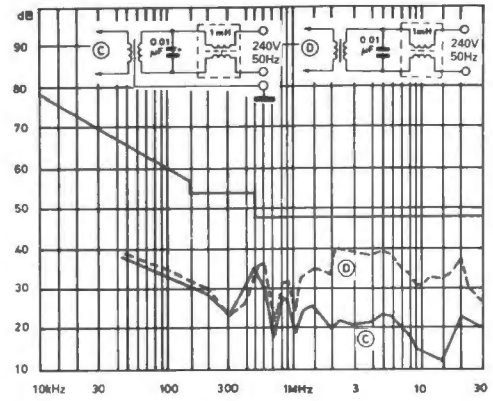


Figure 66 **EMI results with the addition of an inductive filter on the mains input**



Other applications

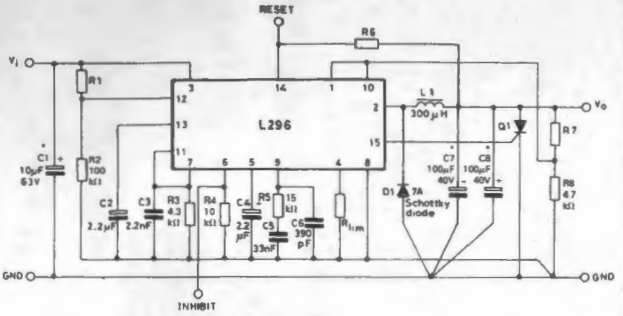
Though the L296 has been designed for step-down regulator configurations it may be used in a variety of other applications. We will now examine these possibilities and show how the capabilities of the device may be extended.

In Figure 67 the complete typical application is shown, where all the functions available on the device are being used. The circuit delivers to the load a maximum current of 4A and a voltage which is established by the voltage divider constituted by R_7 and R_8 resistances. The following table is helpful for a quick calculation of some standard output voltages:

Resistor value for standard output voltages		
V_o	R_8	R_7
12V	4.7kΩ	6.2kΩ
15V	4.7kΩ	9.1kΩ
18V	4.7kΩ	12kΩ
24V	4.7kΩ	18kΩ

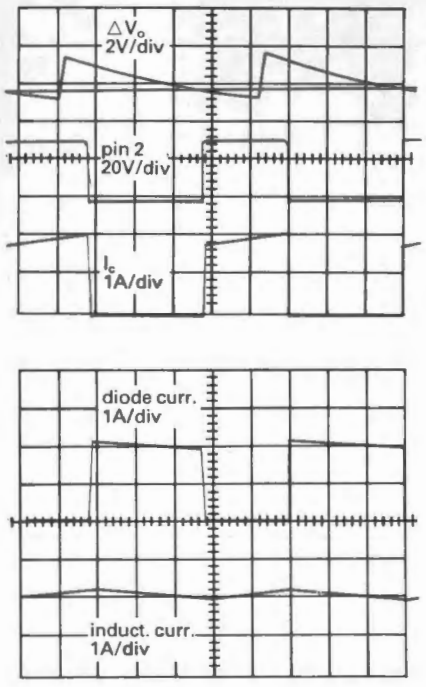
To obtain $V_o = V_{REF}$ the pin 10 is directly connected to the output, therefore eliminating both R_7 and R_8. The switching frequency is 100kHz.

Figure 67 **Schematic – this is a typical stepdown application which exercises all the device's functions**



*Capacitors C1, C7 and C8 must have a low ESR and a low inductance at high ripple.

Figure 68 **Oscilloscope diagrams showing main waveforms of the Figure 67 circuit**



The oscilloscope diagrams of the main waveforms are shown in Figure 68. The output voltage ripple $\triangle V_o$ depends on the current ripple in the coil and on the performance of the output capacitor at the switching frequency (100kHz). A capacitor suitable for this kind of application must have a low ESR and be able to accept a high current ripple, at the working frequency. To minimise the effects of ESR, two 100µF/40V capacitors have been connected in parallel.

Also the selection of the catch diode requires special care. The best choice is a Schottky diode which minimises the losses because of its smaller forward voltage drop and greater switching frequency rate. A possible limitation comes from the backward voltage, that generally reaches 40V max.

When the full input voltage range of the device is required in this application it is possible to use super fast diodes with 35 to 50ns rated recovery time, where no more problems on the backward voltage occur (on the other hand, they show a greater forward voltage). The use of slower diodes, with trr = 100ns or more is not recommended. Diodes showing trr greater than 35-50ns will reduce the overall efficiency of the system, increasing the power dissipated by the device.

The third component requiring care is the inductor. Besides having the required inductance value, the coil has to show a very high saturation current.

Therefore, a correct dimensioning requires a saturation current above the maximum value of I_{2L}, the current limit threshold.

To achieve high saturation with ferrite cores an air gap between the two core halves must be provided; the air gap causes a leakage flux which is radiated in the surrounding space. To better limit this phenomenon 'pot cores' may be used, whose geometry is such to better limit the flux radiated to the outside.

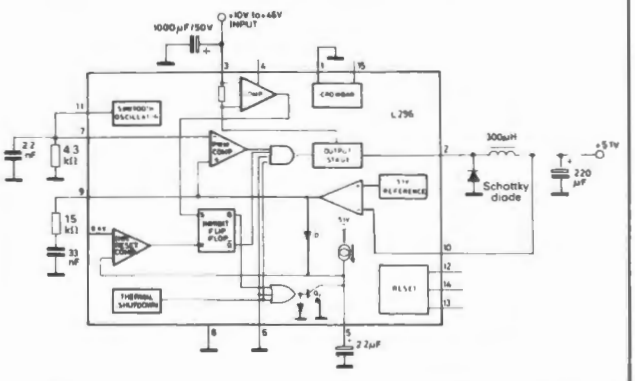
Using toroidal cores, for instance the moly-permalloy kind, both the requirements of high saturation and low leakage flux are satisfied. The saturation is softer than the saturation shown by the ferrite materials. The air gap is not concentrated in one area, but is finely distributed along the whole core; this gives the low leakage flux value.

Careful selection of the external components therefore allows the realisation of a power supply system whose benefits are significant when compared to a system with the same performance but realised with the linear technique.

Low cost application and preregulator

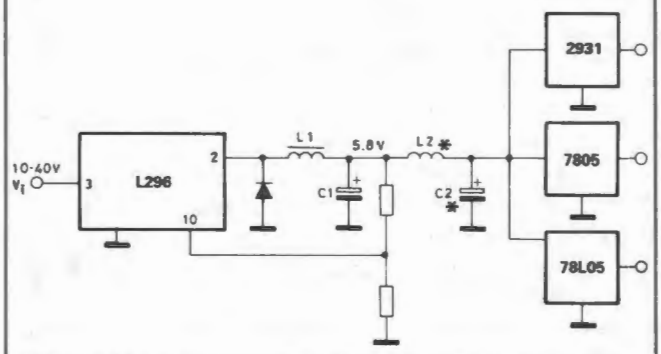
Figure 69 shows the low cost application of a 4A and V_o = 5.1V power supply. A minimum amount of essential external components is required, which is necessary for correct operation. It is impossible to save other components, specially the soft-start capacitor. Without soft-start, the system cannot reach the steady state and there is also a serious risk of damaging the device.

Figure 69 **A minimal component count 5.1V/4A supply**



This application is very well suited not only as a low-cost power supply, but also as pre-regulator for linear-regulators distributed in different circuit points, or even on different boards (Figure 70). The linear-regulators may be selected among the low-drop types, like the 2931 to obtain high efficiency or, standard 7800 regulators can be used.

Figure 70 **Preregulator for distributed supplies**



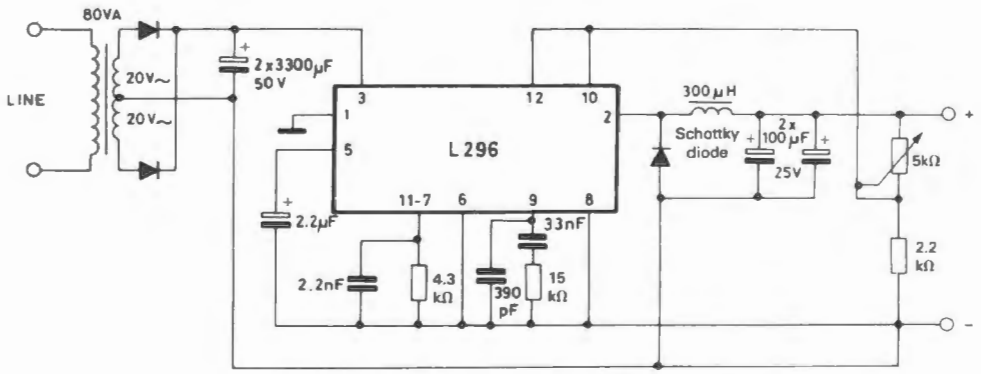
* L2 and C2 are necessary to reduce the switching frequency spikes.

Power supply complete with transformer

Figure 71 shows a power supply complete of transformer, bridge and filter, with regulation on the output voltage from 5.1V to 15V.

As already stated previously, the output capacitors have to show some special features, like low ESR and high current ripple, to obtain low voltage ripple values and high reliability. The input filter capacitors must not be neglected because they have to show excellent features, too, having to supply a pulsed current, required by the device at the switching frequency. The current ripple is rather high, greater than the load current. For this application, two parallel connected 3300μF/50V capacitors have been used.

Figure 71 **A typical variable supply showing the mains transformer**



V_o = 5.1 to 15V
I_o = 4A max. (min. load current = 100mA)
ripple ≤ 20mV
load regulation (1A to 4A) = 10mV (V_o = 5.1V)
line regulation (240V ± 15% and to I_o = 3A) = 15mV
(V_o = 5.1V)

Power supply with 0-30V adjustable voltage

When output voltages lower than 5V are required, the circuit shown in Figure 72 may be used.

Calibration is performed by grounding the P1 slider. Acting on P2, the current which flows through the 10kΩ resistor is fixed at approximately 2.5mA to obtain an output voltage of 30V. The equivalent circuit is shown in Figure 73.

Acting now on the slider of P1, the current flowing through the divider may be varied. The new equivalent circuit is shown in Figure 74.

Reducing the current flowing, also the voltage drop across the 10kΩ resistance is reduced, together with V_o. When the current reaches zero, it follows that $V_o = V_{REF}$. When the voltage on the slider of P1 exceeds V_{REF} , the current starts to flow in the opposite direction and V_O begins to decrease below 5V.

When $I_1 \times 10k\Omega = V_{REF}$ it follows that $V_o = 0$.

Figure 72 **Variable 0-30V supply illustrating how output voltages below 5.1V are obtained**

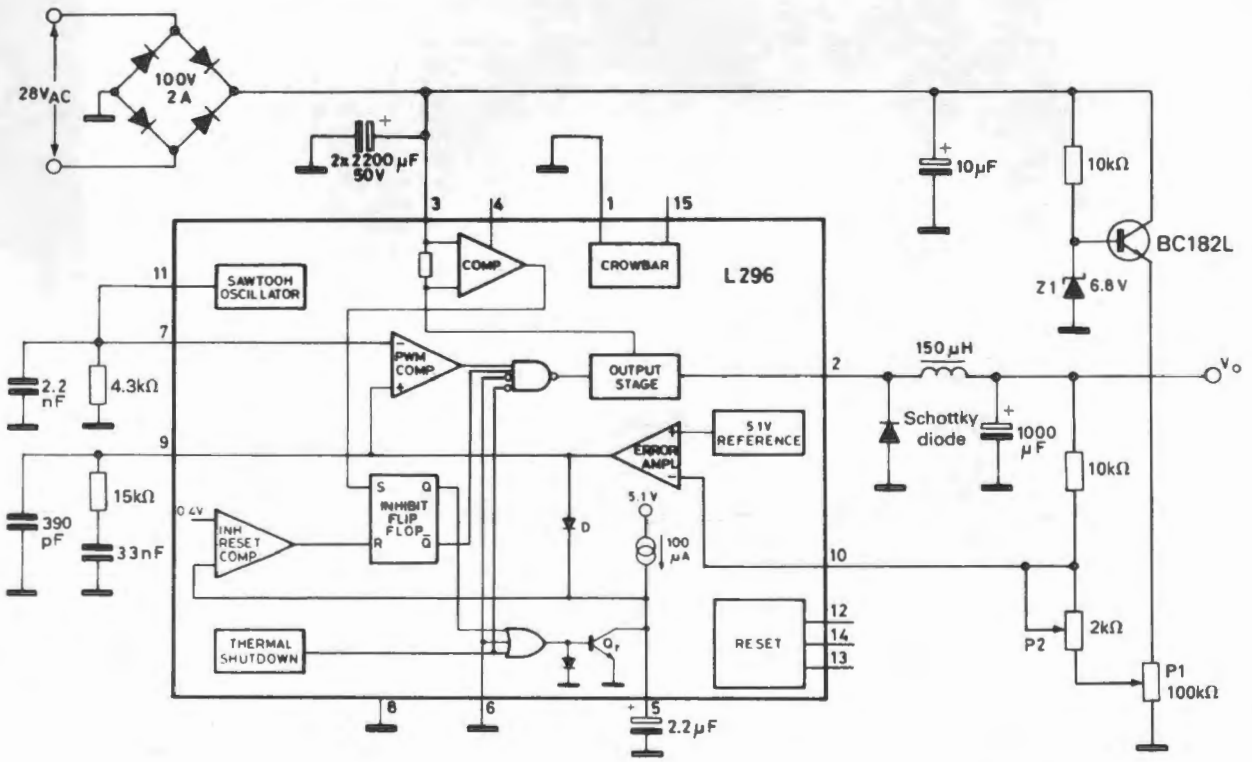


Figure 73 **When setting up the Figure 72 circuit the slider of P1 is grounded, giving the equivalent circuit shown here, and P2 adjusted to give an output voltage of 30V**

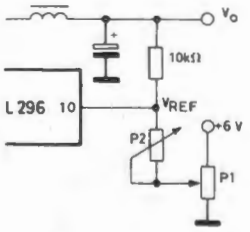
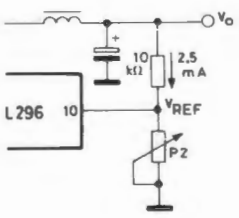


Figure 74 **Partial schematic showing output voltage adjustment of Figure 72**

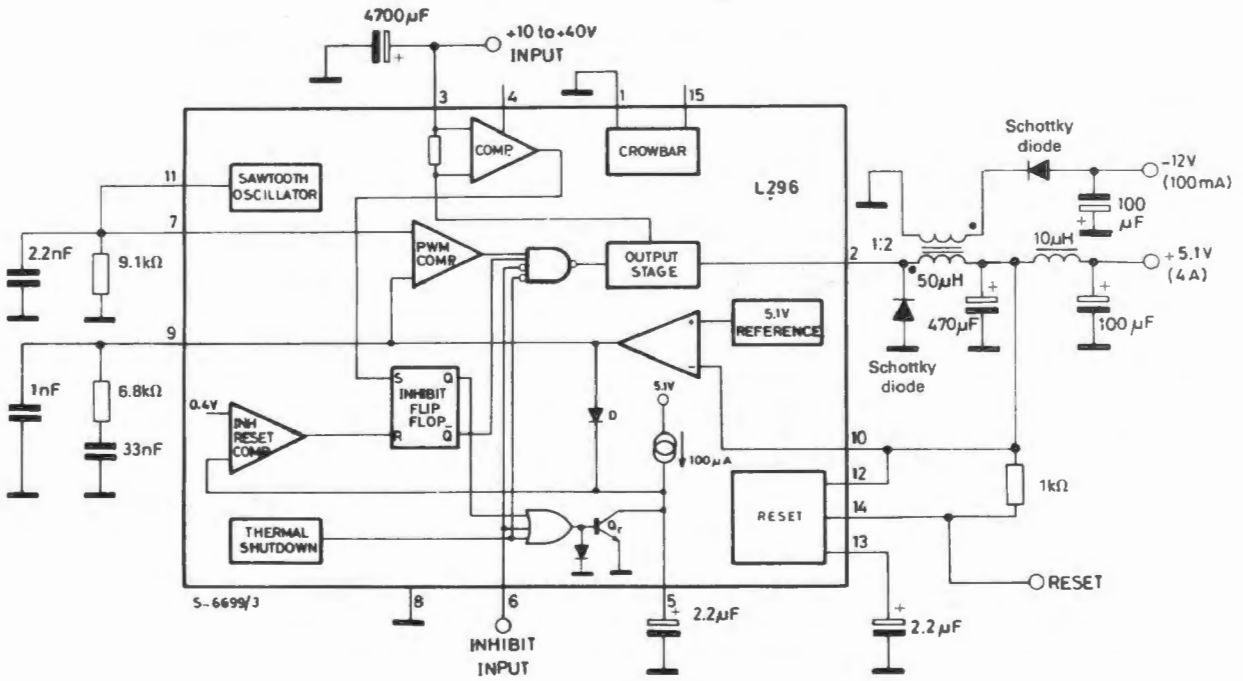


Dual output regulator

The application shown in Figure 75 is specially interesting because it provides two output voltages. The first voltage, the main one, is directly controlled by the feedback circuit. The second voltage is obtained through an auxiliary winding.

In applications where microprocessors, logic devices etc., are used a main 5V output and an auxiliary +12V or –12V output are required, the latter with lower current requirements (100 to 200mA) and a reduced stabilization level. As the auxiliary power supply is obtained through a completely separated winding, it is possible to obtain either a positive or negative voltage (compared to the main voltage or also a completely isolated voltage. With V_i variable between 20V and 40V, V_o = 5.1V and I_o = 2.5A, the auxiliary –12V/0.1 voltage is within a ±2% tolerance.

Figure 75 **Dual output regulator showing how an additional winding can be added to the inductor to generate a secondary output**



Personal computer power supply

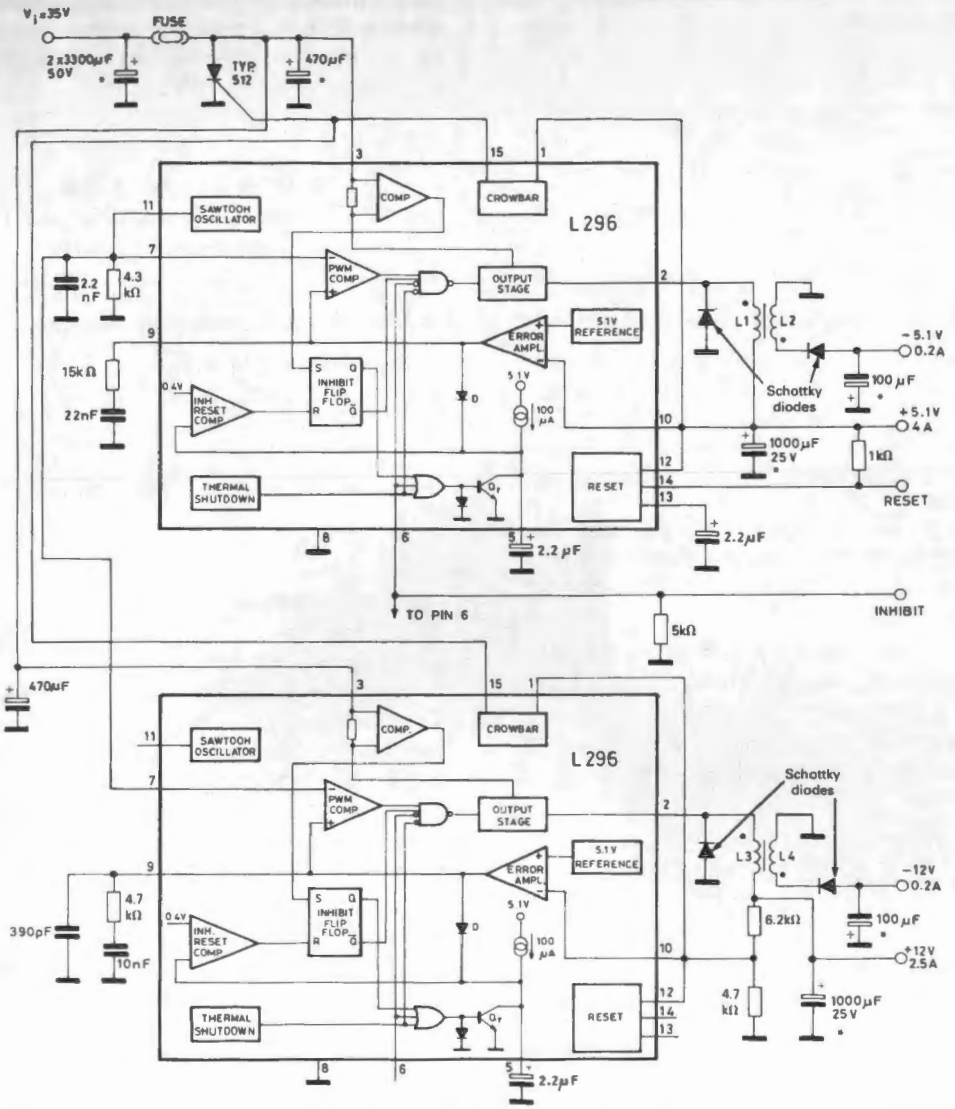
Using two mutually synchronised devices it is possible to obtain a four output power supply suitable to power a microprocessor system.

V_{01} + 5.1V/4A
V_{02} = 12V/2.5A (up to 4A)
V_{03} = –5V/0.2A
V_{04} = –12V/0.2A

The circuit diagram is shown in Figure 76. The 5V output is also provided with the reset function, that is available also for the 12V output.

The feedback is direct, no other external component is used and no calibration is therefore required. An output is obtained with the accuracy of the reference voltage (± 2%). For the 12V output, by using a resistive divider with 1% resistance an output is obtained whose spread is within ±4%.

Figure 76 **Microcomputer supply with 5V, –5V, 12V and –12V outputs**



* These capacitors must have a low ESR and a low inductance at high ripple.

The two devices are mutually synchronised so as not to give rise to intermodulation which could generate unpleasant noise and, at the same time, a further component saving is achieved.

The crowbar function is implemented on both 5V and 12V outputs, using a single SCR connected to the input. The latter, by discharging to ground the electrolytic filter capacitors, blows the fuse connected in series with the device's power supply. In this way, should a fault be present on either of the main outputs, the supply is switched off for the whole system.

To inhibit both the devices with a single input signal, it is possible to connect the two inhibit inputs (pin 6) together; the 5kΩ resistor is used when the inhibit input is left open. If this input is not used it must be grounded.

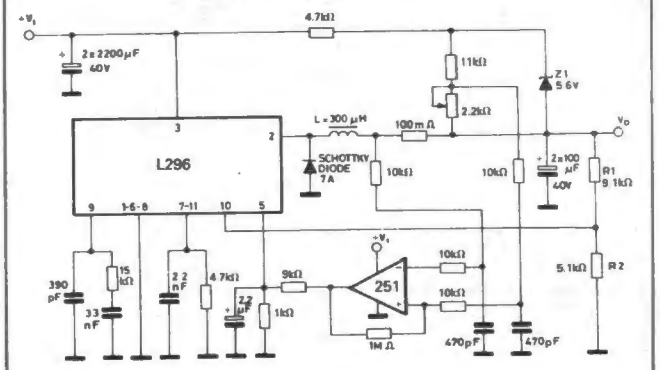
As may be noted in the diagram, obtaining the two auxiliary voltages is very simple and cost-effective.

It is suggested that the diodes are fast types (trr< 50nsec); should slower diodes be used some more turns have to be added to the auxiliary winding.

Battery charger

When the device has to be used as a current generator it is necessary to avoid the internal current limiter being operated. Figure 77 shows the circuit realising constant current limitation. In this way it is possible to obtain a 6V, 12V and 24V battery charger. For each of these voltages a max current of 4A is available, which is large enough for batteries up to 40-45Ah (for 12V type). With reference to the circuit diagram using the 2kΩ potentiometer the max output current is set, while through the $R_1 - R_2$ output divider the voltage is set. (R_1 may be replaced by either a potentiometer or a 3 position switch, to directly obtain the three 6V, 12V and 24V voltages).

Figure 77 **Battery charger circuit illustrating how the device is used to regulate the output current**



Higher input voltage

Since a maximum input voltage of 46V (operating value) may be applied to the device the diagram shown in Figure 78 may be used when it is necessary to exceed this limit.

This system is particularly useful when operating at low output voltages. In this case a mean current I_{iDC} which has a low value when compared to I_o is obtained. In fact, since $V_o = V_i (T_{ON}/T)$ and $V_o I_o = V_i I_{iDC}$ (assuming the device has an ideal efficiency), it follows that $I_{iDC} = I_o (T_{ON}/T)$.

Assuming to be:

$V_o = 5V$ $I_o = 4A$ and $V_3 \simeq 37V$,

it follows that:

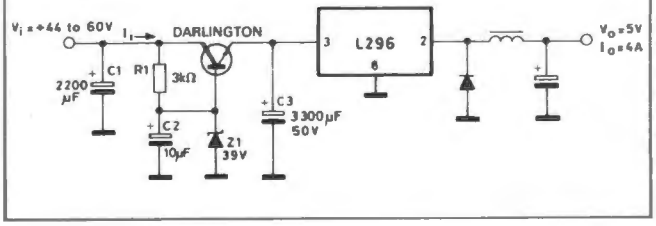
$$T_{ON}/T = V_o/V_i = \frac{5}{37} = 0.135$$

$I_{iDC} = 4 \times 0.135 = 0.54A$.

With input voltage 50V and $I_o = 4A$, the external transistor dissipates about 7W. High efficiency is still achieved, around 74%; in the real case, considering also the device losses, an efficiency around 62% is achieved.

During output short circuits the external transistor is not overloaded because in this condition I_{iDC} reduces to values lower than 100mA. It is not possible to utilise this application with a series post-regulator because the efficiency would be unacceptably low.

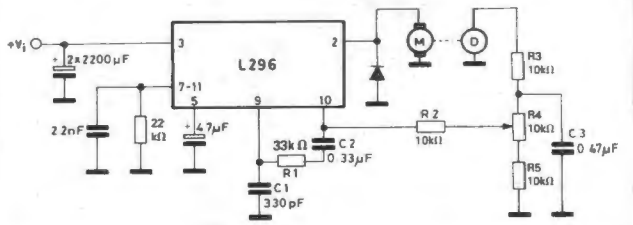
Figure 78 **The maximum input voltage can be raised above 46V by adding a transistor as shown here**



Motor control

The L296 is also suitable for use in motor control applications. Figure 79 shows how to use the device to drive a motor with a maximum power of about 100W and provided with a tachometer generator for a good speed control.

Figure 79 **With a tacho dynamo supplying feedback the L296 can be used as a motor speed controller**



Higher current regulators

It is possible to increase the output current to the load above 4A through the use of an external power transistor. Figure 80 shows a suitable circuit. The frequency is around 40kHz to prevent the device from losing excessive power due to switching on the external power transistor.

The circuits shown in Figures 81 and 82 show how current limitation may be realised in two different ways: through a sensing resistor connected in series with the collector of the external power transistor or through a current transformer.

In the first case, the sensing resistor is a low value resistor able to withstand the maximum load current required. The V_{CE} of the power transistor is higher than its V_{CEsat}; when the resistor is connected in series to the collector V_{CE} is reduced; consequently since the overall dissipated power is constant, the power dissipated by the sensing resistor is subtracted from that dissipated by the power transistor. The values indicated in Figures 81 and 82 realise adjustable current limitation for load currents around 10A.

Figure 80 **The output current may be increased by adding a power transistor as shown in this circuit**

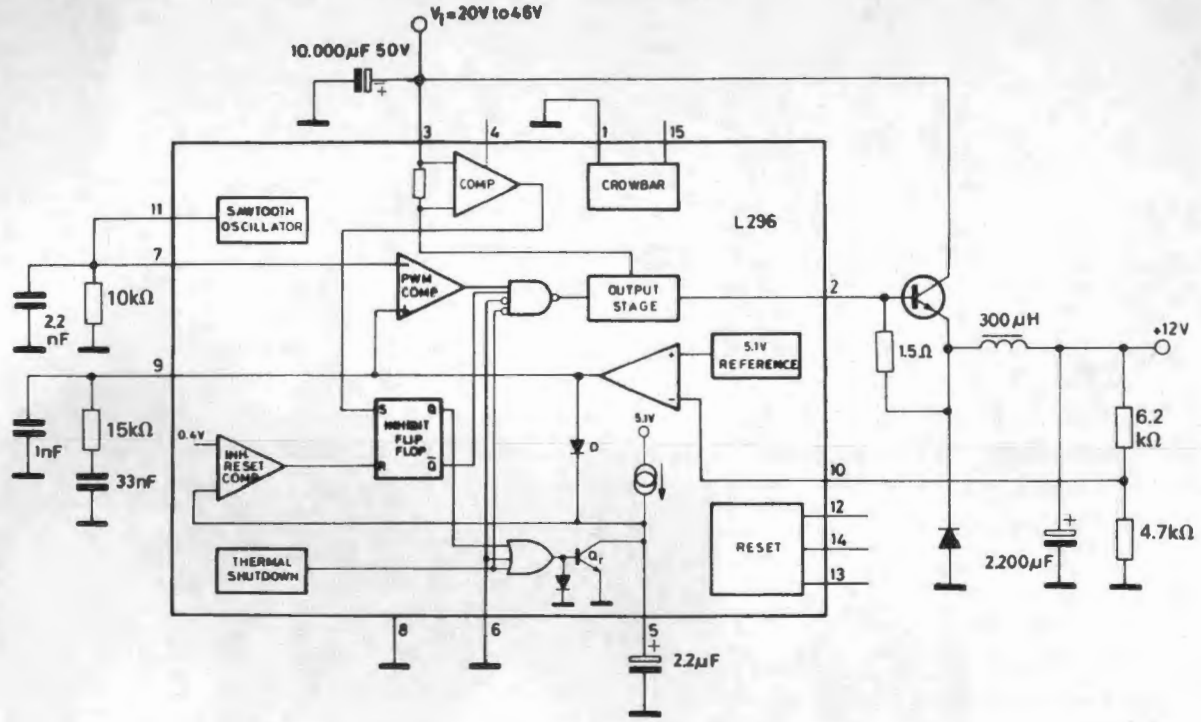


Figure 81 **This circuit shows how current limiting for the external transistor is obtained with a sensing resistor**

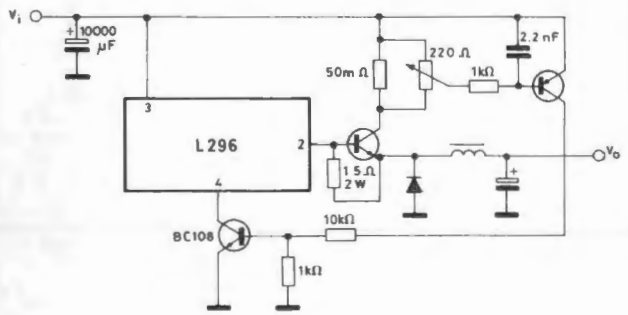
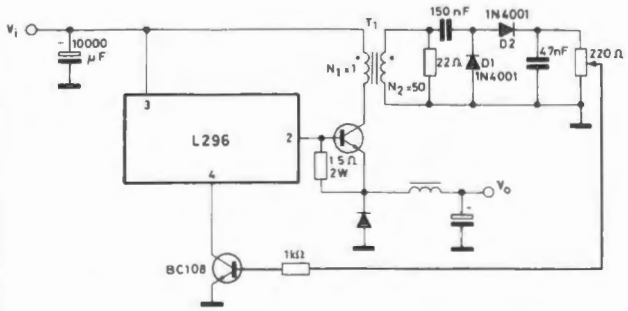


Figure 82 **A small transformer is used in this example for current limiting**



Step-up converter

With the L296 it is also easy to realise a step-up converter, by using a MOS power transistor. Figure 83 shows the circuit diagram of the step-up converter. The frequency is 100kHz, operation is in discontinuous mode and the device internal current limiter is used. Therefore no other external protection is required.

The input voltage could be a 12V car battery, from which an output voltage of 35V may be obtained. Lower output voltage values may be obtained by reducing the value of R_7.

Description of operation

Figure 84 shows the diagram of the circuit realising the step-up configuration.

When the transistor Q1 is ON, the inductance L charges itself with a current given by:

$$i_L = \frac{V_i}{L} t$$

The peak current in the coil is:

$$I_{peak} = \frac{V_i}{L} T_{ON}$$

Figure 83 **A step-up converter using a power MOS transistor**

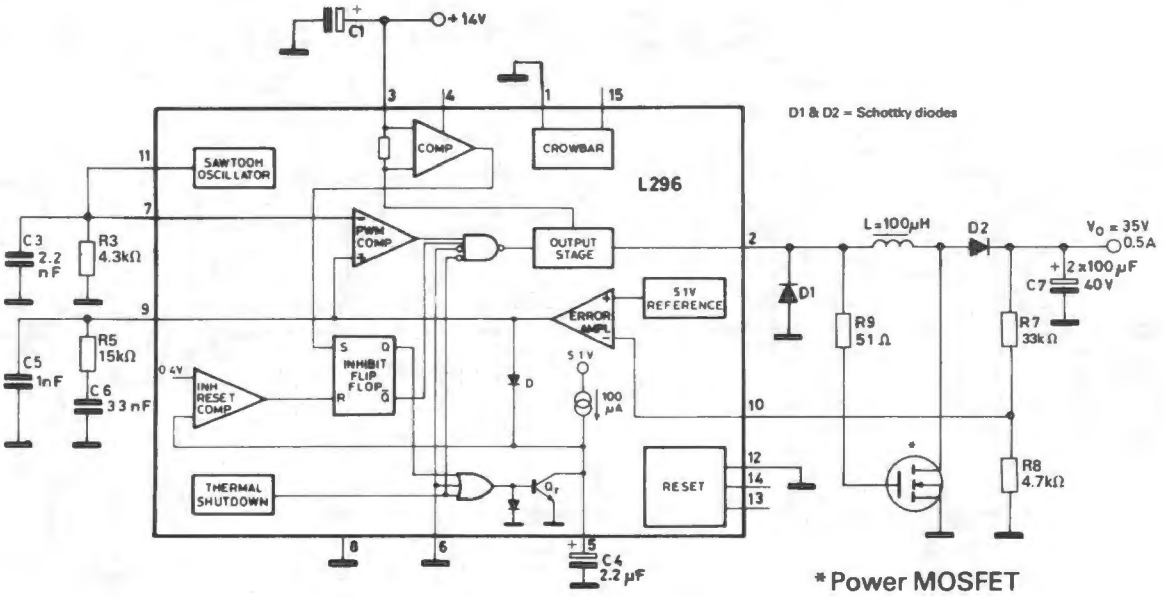
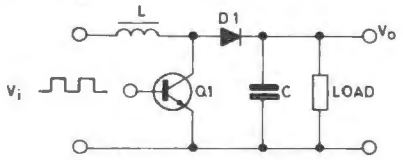


Figure 84 **Basic schematic for step-up configurations**



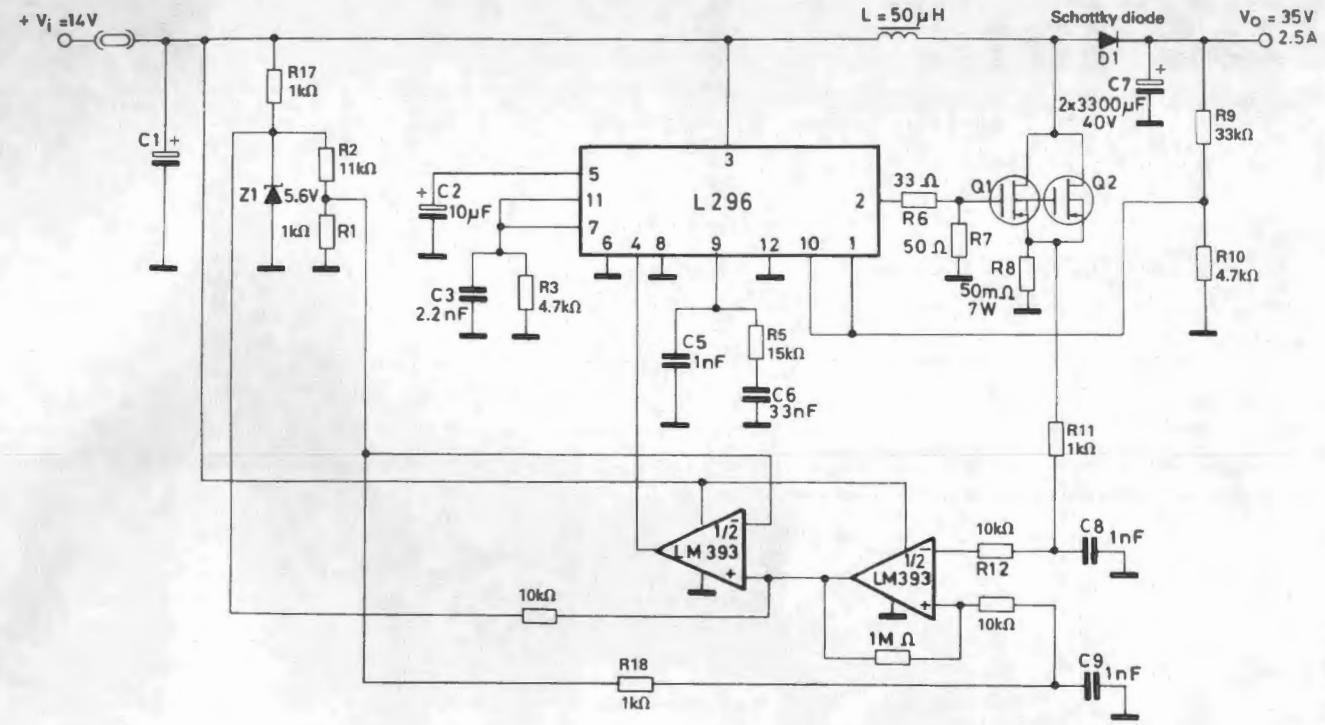
In this configuration, unlike the step-down configuration, the peak current is not strictly related to the load current. The energy stored in the coil is successively discharged across the load when the transistor switches OFF. To calculate the I_o load current, the following procedure may be used:

$$\frac{1}{2} L I_{peak}^2 = V_o I_o T$$

$$I_o = \frac{L I_{peak}^2}{2 V_o T} + \frac{V_i^2 T_{ON}^2}{2 L V_o T}$$

For a greater output power to be available, the internal limitation must be replaced by an external circuit to protect the external power devices and to limit the current peak to a convenient value. A dual comparator (LM393) with hysteresis is used to avoid uncertainties when the current limit operates. The circuit diagram is shown in Figure 85.

Figure 85 **High power step-up converter showing how the current limiting function is realised externally**



RS data

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An Electrocomponents Group Company

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RS data

Suppression

The susceptibility of modern electronic systems to interference, particularly those with microprocessor control, is of increasing concern to the engineer. Voltage transients and signals with fast transition times contain rf energy, and can generate interference in local circuitry. Transmission occurs both by conduction and radiation.

Common sources of noise are:

- Turn-on spikes resulting from initial charging current taken by capacitive loads, notably input filter capacitors on power supplies.
- Turn-off spikes resulting from the release of energy stored in the magnetic field of inductors, such as transformers, contactors, lighting ballast etc.
- Repetitive spikes generated by commutator motors, control gear, radio/radar transmitting equipment, welders, phase controlled triac/SCR circuits etc.
- High speed data lines with fast pulse transition times, giving the possibility of capacitive coupling between signal paths in digital equipment.
- High power amplifiers with low output impedance, (hence high currents) giving the possibility of inductive coupling to high impedance circuitry.

The aim of suppression

In an ideal system there will be no form of conducted or radiated electromagnetic energy other than intended signals following intended routes. It should therefore be the designer's aim to suppress all possible generators of unwanted noise as close to the source as possible. This will generally be carried out by selectively routing the noise to a suitable sink, for example, earth, or dissipating it in a resistive element.

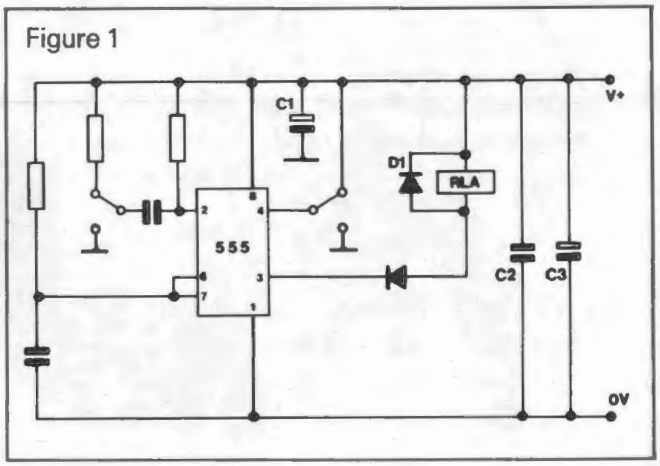
Suppression components are typically frequency dependent networks comprising L, C, and R, or specifically designed voltage dependent components offering a low resistance path to voltages above a predetermined level.

Methods of suppression

1. Coils

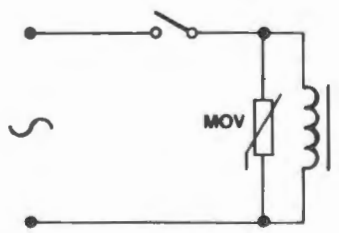
Breaking the supply to an inductive load results in the generation of a large voltage pulse, of reverse polarity to the original supply. The size of pulse will be determined by supply voltage, coil inductance and circuit resistance.

Figure 1



On a dc supply, a common example being the relay coil in Figure 1, the solution is fortunately simple. A diode, D1, connected across the coil in a normally reverse biased configuration, serves to prevent the turn-off spike from damaging the timer output. The switching *on* of the relay in this example could also generate a momentary dip in supply voltage, owing both to the totem-pole output of a standard 555 timer, and also to the additional current taken by the relay coil. In order to reduce the effect of such supply transients, either out of or into the circuit, decoupling components C1, C2 and C3 are added. C1 might be a 47μf tantalum mounted close to the ic, C2 a 0.1μf disc ceramic and C3 a 100 μf tantalum or standard electrolytic across the incoming supply.

Figure 2



In an ac application, the size of the spike will also depend on the point in the mains cycle at which the circuit is broken. Clearly a diode cannot be used and a non-polarised device is necessary.

Metal Oxide Varistors (MOV) also known as voltage dependent resistors, offer a solution (Figure 2) giving a non-linear voltage dependent characteris-

tic. Spikes above the working voltage are presented with a low resistance and are hence attenuated. Being resistive in nature MOVs dissipate the energy in the spike and are therefore available at different energy ratings; the higher the energy, the larger the MOV. This method has the additional benefit of increasing switch life by reducing arc damage to the contacts.

Table 1

Metal oxide varistors
Maximum ratings

Parameter	Value								Units
Stock No.	238-564	238-570	238-586	238-592	238-609	238-615	238-621	238-637	
RMS working voltage	60	130	130	130	275	275	275	460	V
dc working voltage	85	170	170	170	350	350	350	615	V
Transient energy 8/20μs (Note 1)	6	14	30	53	8.5	26	61	16	J
Transient energy 10/1000μs (Note 1)	4.6	9.5	16	26	11	20	35	20	J

Electrical characteristics

Parameter	Value								Units
Stock No.	238-564	238-570	238-586	238-592	238-609	238-615	238-621	238-637	
Minimum MOV voltage (Note 2)	90	185	185	185	387	387	387	675	V
Maximum MOV voltage (Note 2)	110	225	225	225	473	473	473	825	V
Maximum clamping voltage at 50A	—	—	—	—	820	—	—	1480	V
Maximum clamping voltage at 100A	210	425	385	360	—	850	815	—	V
Typical capacitance at 1kHz	600	390	730	1300	60	140	290	50	pF

Notes: 1. A current impulse as defined in IEC 60-2 Section 6.
2. Voltage measured at a current of 1mA, after an impulse time of 50ms with a rise time of 10ms to 1ms.

Switch contacts

In cases where total removal of the transient is not possible at source for one reason or another, protection may be added to the switch contacts in question to reduce arcing, (a source of radiated interference in addition to generating a line transient). This also has the advantage of prolonging the contact life.

Figure 3a

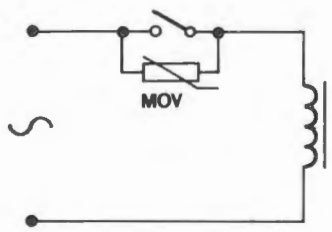
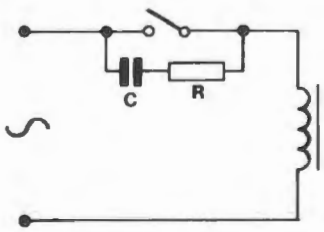


Figure 3b

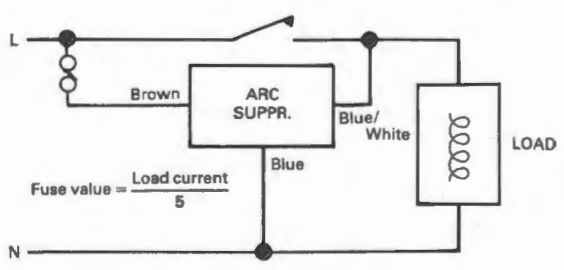


The MOV may be connected across a pair of switch contacts as in Figure 3a or alternatively, an RC network as in Figure 3b can be used to suppress the higher order harmonic content of the 'step pulse' (or square wave) created when the switch is operated. This method cannot be expected to completely remove arcing, and may allow the passage of a transient beyond the switch, but is an economic solution to smaller problems. Typical value for R and C would be 0.1μf and 100 ohms; RS type 238-463 offers these in a convenient package.

In cases of severe arcing across contacts in an ac circuit, a solid state 'bypass' method is available: assuming the problem load to be reactive, use can be made of the phase shift and back-emf to trigger a triac, connected across the switch contacts, at the instant they open. Hence the load current is carried by the triac for up to half a cycle, in which time the switch has opened beyond the arcing potential.

A comparatively small triac can be used, given this ½ cycle maximum rating, for quite heavy loads. Our 238-378 (see Figure 4) operates on a similar principle to the above.

Figure 4 **Solid state contact arc suppressor**



General supply-line borne interference

Industrial environments can generally be expected to have noisy electrical supplies; pulses of 200V superimposed on single phase 240V ac supplies are not uncommon. In view of this, and any additional general RF noise that can be present on the mains, it is advisable to equip any sensitive equipment with suitable input filtering. The capacitor/choke network shown in Figure 5 appears in many package forms in the 'Mains Suppression Filters' section of the RS catalogue. Plug-in versions are available for addition to ready-built equipment.

Figure 5 **In-line suppressor – typical values**

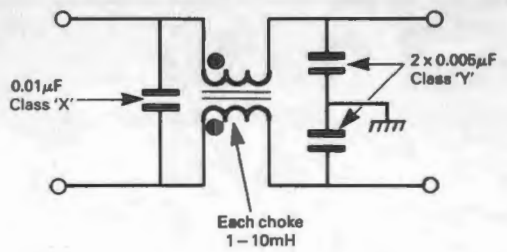
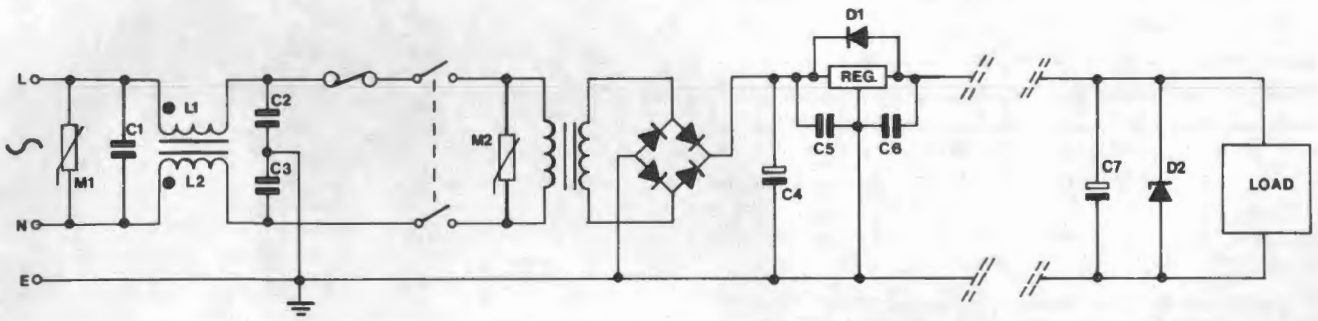


Figure 6



Applications

Figure 6 shows a 'belt and braces' example of a mains input, dc output, power supply unit using a 3 terminal regulator.

MOV M1 serves to attenuate large incoming spikes; RFI filtering is then provided by X class capacitator C1, in-line chokes L1 and L2 (wound on a common core) and Y-class capacitors C2 and C3. M2 serves to suppress switch off transients.

Capacitor C4 provides smoothing for the full-wave bridge, C5 and C6 are low value (0.1 to 0.47μF) ceramic disc decoupling capacitors for the regulator and should be mounted close to the package. Diode D1 provides some degree of reverse polarity protection.

If the load is somewhat remote, further decoupling in the form of C7 may be added. D2 represents a high speed transient suppressor of the type specifically designed for use in suppression, unlike a zener diode whose normal function is voltage regulation. Such devices are available for use on common values of supply rail, refer to Table 2 for specifications.

Table 2

High speed suppressors

Max. ratings (all types)

Peak pulse power (1ms pulse) 1500W

Clamp time (0_v to B_v min) $<1 \times 10^{-12}$ sec

Operating and storage temperature –65°C to +175°C

Forward surge rating 200A (8ms at 25°C)

Steady state power dissipation 5.0W
(lead temp. 75°C, lead length 9.5mm)

Duty cycle 0.01%

Electrical characteristics at 25°C

Stock number	283-255	283-261	283-277
Reverse standoff voltage V_R	5.5V	12.9V	14.5V
Breakdown voltage B_V at (mA)	6.12 to 7.48V (10)	14.4 to 17.6V (1)	16.2 to 19.8V (1)
Maximum clamping voltage at I_{PP} (1ms)	10.8V	23.5V	26.5V
Maximum peak current I_{PP}	139A	64A	56.5A
Maximum reverse leakage at V_R	1mA	5μA	5μA
Maximum temp. coeff of B_V% per °C	0.057	0.086	0.088

RS data

Summary

There are two methods of interference coupling:

Conduction

Shared conductive paths between circuits, or 'common impedance coupling'. Most common in power and ground distribution systems; design considerations would be:

a) Supply rails should be of low impedance.

b) Supply distribution should be arranged such that currents which potentially carry noise do not mix with currents in sensitive circuits. A 'star point' earth system for example is used to avoid current mixing and earth loops; each stage of a system is individually earthed to one incoming earth point.

c) Bypass filtering and decoupling should be employed on power supply rails between stages.

Radiation

The coupling by electromagnetic field through circuit capacitance or inductance. High voltage/high impedance circuitry will be prone to capacitive (electric field) coupling, whereas high current/low impedance circuitry will radiate a magnetic field. Design considerations here would be:

a) Field coupling between circuit elements such as pcb tracks, inter-board wiring, power rails etc. is reduced by reducing conductor length and increasing physical separation.

b) 'High noise' signal lines should be segregated from lines sensitive to pick up, and shielding (ie. screened cables or enclosures) or interposed ground lines used.

c) Decrease crosstalk by using lower frequency signals if possible; ie. increase transition time.

d) The use of local ground planes on a pcb reduces circuit impedance and hence reduces capacitive coupling.

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RS data

Audio preamplifiers LM381, HA12017 and 6270

Stock numbers 306-825, 304-576, 302-132

Two high quality audio preamplifier i.c.s. suitable for magnetic cartridge amplification using RIAA equalisation, or microphone amplification using a "flat" characteristic. Also a microphone preamplifier incorporating a Voice Operated Gain Adjusting Device (V.O.G.A.D.).

LM381

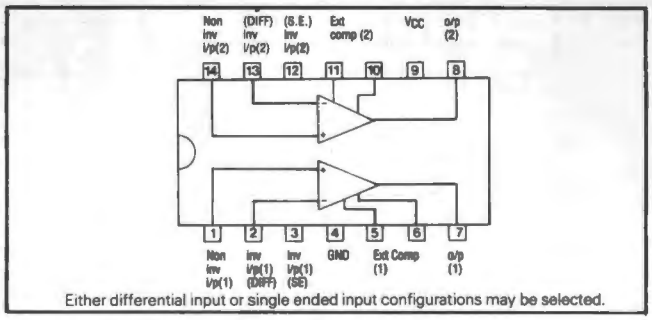
A dual preamplifier specially designed to meet the requirements of amplifying low level signals in low noise applications. Each amplifier contains an internal power supply decoupler-regulator, providing 120dB supply rejection and 60dB channel separation. Other features include high gain, large output voltage swing and a wide power bandwidth. Operation is from a single supply in the range 9 to 40V and the device is internally compensated and short-circuit protected.

Maximum ratings

Supply voltage	40V
Dissipation	715mW
Operating temperature range	0 to 70°C
Input voltage for linear swing	300mV rms

Typical electrical characteristics

Voltage gain open loop single ended	320,000 (110dB)
Voltage gain open loop single differential	160,000 (104dB)
Total supply current ($R_L = \infty$)	10mA
Input resistance	100kΩ
Open loop output resistance	150Ω
Voltage swing	$V_{CC} - 2V$
Full power bandwidth	75kHz
Channel separation	60dB
Harmonic distortion at 60dB gain	0.1% at 1kHz



Either differential input or single ended input configurations may be selected.

NOTES
A ready made pc board RS stock number 434-396 is available to accommodate the LM 381 and associated components (including the tone and volume controls) for a stereo pre-amplifier giving RIAA flat characteristics.

Applications

Figure 1 **Magnetic cartridge amplifier to the RIAA characteristic**

An amplifier to RIAA characteristics for use with dynamic cartridges with a standard load of 50kΩ. When a crystal or ceramic cartridge is used the LM380 "single ended amplifier" circuit may be connected directly. Gain ≃ $\frac{30,000}{Re\,\Omega}$

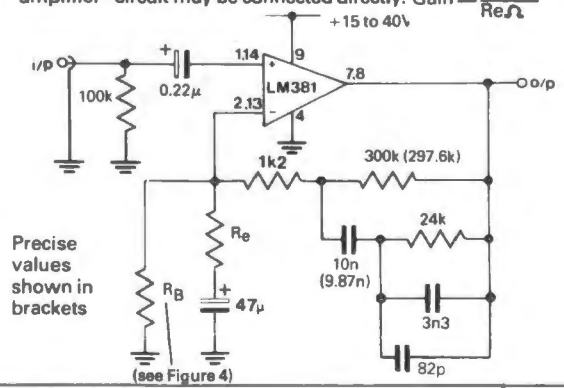
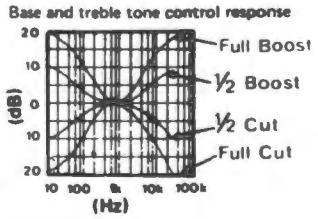
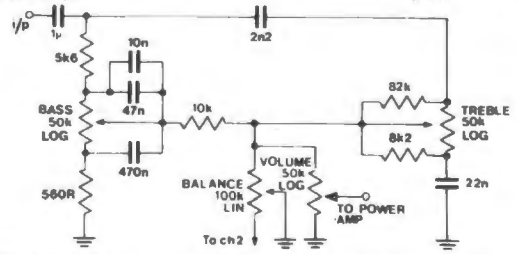


Figure 2 **Tone control stage**

Some audio applications require bass and treble tone controls. Normally two preamplifiers are required to compensate for the insertion loss of the controls. However, due to the excellent gain and large output of the LM381, only a single preamplifier is needed.





The i/p of the tone control stage can be put in series with any preamplifier circuit.

Figure 3 **Audio mixer**

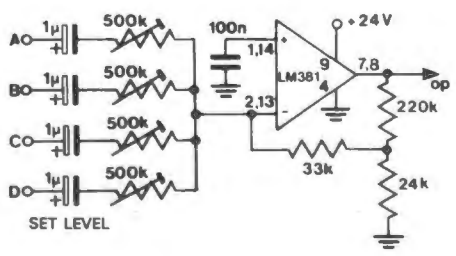
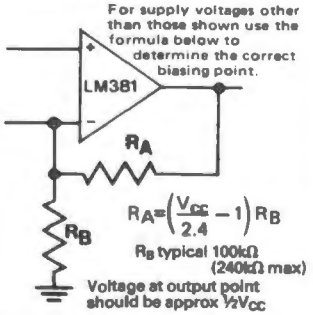


Figure 4 **Biasing**

For supply voltages other than those shown use the formula below to determine the correct biasing point.



$$R_A = \left(\frac{V_{CC}}{2.4} - 1\right) R_B$$

R_B typical 100kΩ (240kΩ max)

Voltage at output point should be approx ½V_{CC}

Figure 5 **Biasing – split supply**

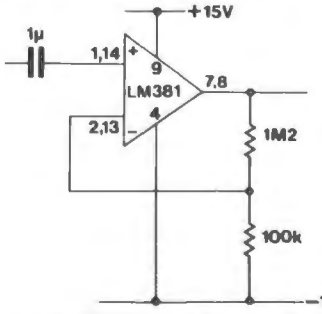
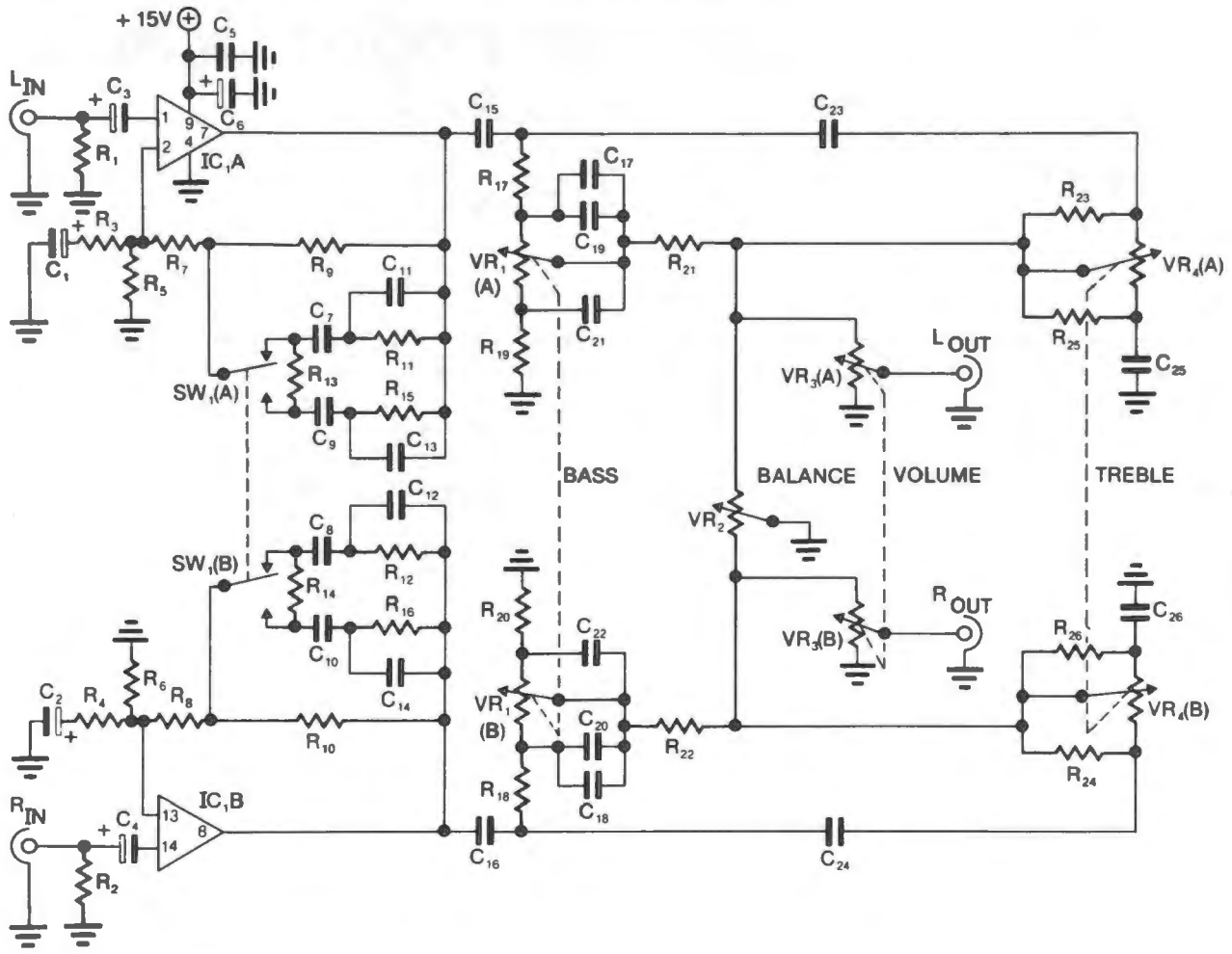


Figure 6 **Circuit diagram of preamplifier using RS printed circuit board 434-396**



List of components

Resistors

R_1 R_2 R_{11} R_{12}	47k	148-893
R_3 R_4	120R	148-281
R_5 R_6	100k	148-972
R_7 R_8	1k2	148-578
R_9 R_{10}	510k	148-433
R_{13} R_{14}	10M	158-159
R_{15} R_{16}	750R	148-477
R_{17} R_{18}	5k6	148-679
R_{19} R_{20}	560R	148-449
R_{21} R_{22}	10k	148-736
R_{23} R_{24}	82k	148-950
R_{25} R_{26}	8k2	148-714

All 0.5W Metal Oxide except R_{13} R_{14} Hi-Stab Carbon Film.

Miscellaneous

VR_1 VR_3 VR_4	50k Log	162-451
VR_2	100k Lin	161-818
IC_1	LM 381	306-825
SW_1	D.P.D.T.	327-658
IC socket	14-pin	402-305
P.C.B.		434-396

Capacitors

C_1 C_2	47μ	16V P.C.B. Electrolytic	104-461
C_3 C_4	100n	35V Solid Tantalum	101-743
C_5	100n	30V Disc Ceramic	124-178
C_6	470μ	16V P.C.B. Electrolytic	104-499
C_7 C_8	6n8	160V Polystyrene	113-386
C_9 C_{10}	2μ2	63V Polyester	114-446
C_{11} C_{12}	1n5	160V Polystyrene	113-336
C_{13} C_{14}	33p	160V Polystyrene	113-235
C_{15} C_{16}	1μ	Min. Dipped Polyester	115-152
C_{17} C_{18}	10n	Min. Dipped Polyester	115-051
C_{19} C_{20}	47n	Min. Dipped Polyester	115-089
C_{21} C_{22}	470n	Min. Dipped Polyester	115-130
C_{23} C_{24}	2n2	Miniature Polyester	112-721
C_{25} C_{26}	22n	Min. Dipped Polyester	115-067

HA12017

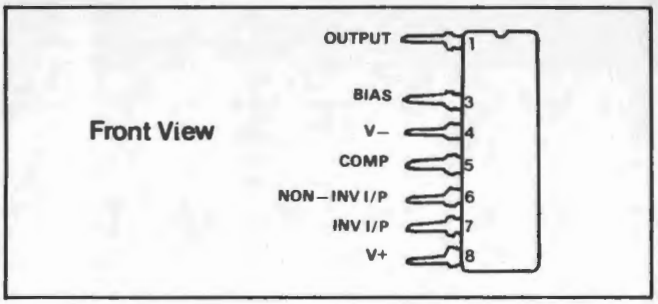
A low noise, very low distortion pre-amplifier i.c. designed for high quality magnetic cartridge amplification using RIAA equalisation.

Absolute maximum ratings

Supply voltage V_{CC} ±26.5V
Power dissipation (T_A 25°C) P_T 500mW
Storage temperature range T_{stg} −55 to +125°C

Recommended operating conditions

Power supply voltage V_{CC} ±24V
Minimum power supply voltage ±6V
Operating temperature range −30 to +75°C



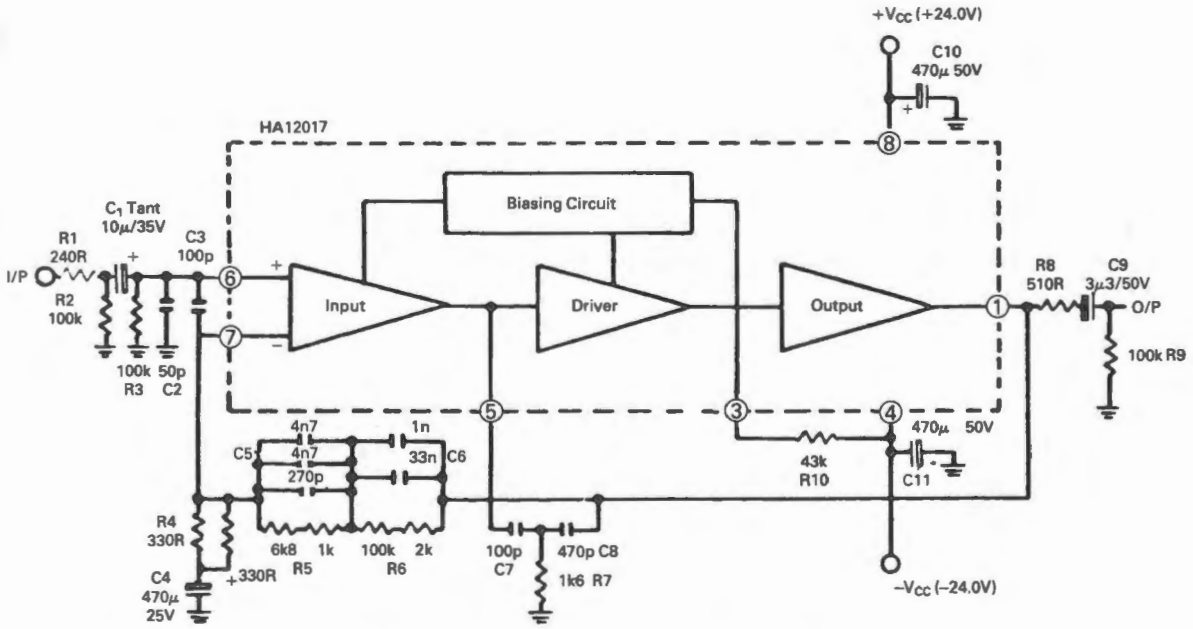
Electrical characteristics

(V_{CC} = ±24V, T_A = 25°C)

Parameter	Symbol	Test Conditions	min.	typ.	max.	unit
Quiescent Current	Iq	no input signal		4.0	6.0	mA
Open Loop Voltage Gain	$G_{V(OL)}$	f = 1kHz	95	105	–	dB
Total Harmonic Distortion	THD	f = 1kHz, V_{out} = 10V	–	0.002	0.01	%
Output Voltage	V_{out}	f = 1kHz,THD = 0.1%	13.5	14.7	–	V
Overload Margin	–	f = 1kHz, THD = 0.1% G_v = 35.9dB		235		mV
Supply Ripple Rejection	SVR+	f = 100Hz Rg = 43Ω		56		dB
	SVR−	f = 100Hz Rg = 43Ω		45		dB
Output Noise Voltage 1	V_{n1}	R_k = 43Ω, IHF-A Network	–	11.5	15.6	μV
Output Noise Voltage 2	V_{n2}	R_k = 3.3kΩ, BW −20Hz to 20kHz	–	53	90	μV

NOTES: 1. All the parameters except $G_{V(OL)}$ are tested with RIAA curve and G_V = 35.9dB. (Av = 62).
2. R_k = Source impedance to pin 6.

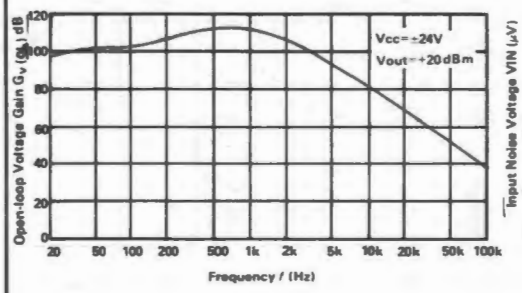
Figure 7 **RIAA pre-amplifier**



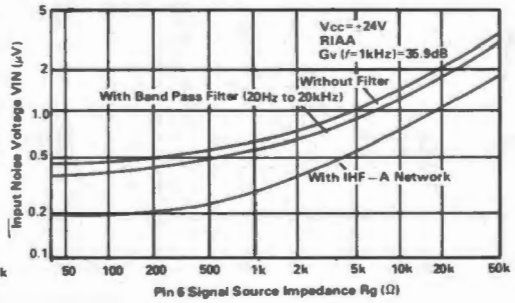
The RIAA pre-amplifier circuit is designed to accurately follow the RIAA playback curve, consequently some of the components in the feedback circuit consist of combinations of standard value capacitors and resistors in order to achieve an accurate response (e.g. 4n7 + 4n7 +270p). For less demanding applications standard preferred value components may be substituted in place of these networks. Input impedance of the amplifier circuit is approximately 50kΩ in order to match the load impedance requirements of the popular dynamic cartridges.

Figure 8

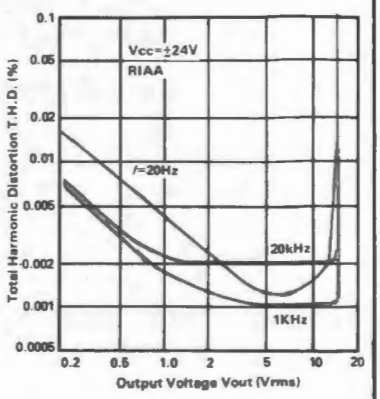
Open loop voltage gain V frequency



Input noise voltage V source impedance



THD V output voltage

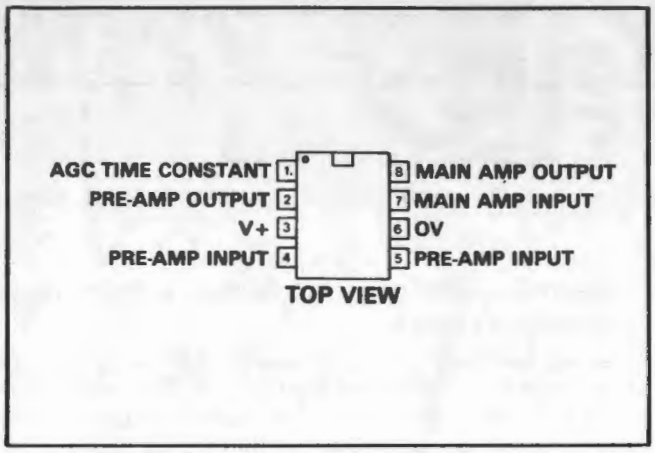


RIAA Pre-amplifier external component functions

Component	Recommended Value	Function
R1	240Ω	Protects the i.c. from abnormal input voltage. Prevents parasitic oscillation caused by signal-source impedance. Decreases high-frequency disturbance.
R2	100kΩ	Passes the electric charge of C1. Decides Rin (input resistance) Rin – R1 + (R2/R3)
R3	100kΩ	Supplies DC bias to pin-6 (input pin). Decides input resistance.
R4	165Ω	Decides voltage gain as feedback resistance.
R5 R6	7.8kΩ 102kΩ	Decides RIAA characteristics, in pairs with C5 and C6.
R7	1.6kΩ	In a pair with C8, decides the frequency at which Gv (OL) characteristic changes from –12dB/oct to –6dB/oct.
R8	510Ω	Prevents parasitic oscillation caused by capacitive load.
R9	100kΩ	Keeps the voltage of output terminals at DC standard level. Prevents shock noise caused by function-switching.
R10	43kΩ	Decides basic bias current R10 – (+V_{CC}– (–V_{CC}) –5) kΩ
C1	10uF	Input coupling.
C2	50pF	In combination with C3, increases stability of large-amplitude operation in high frequency range.
C3	100pF	In strong field, prevents detection of TV, FM and AM signals.
C4	470uF	Supplies full DC-feedback. Decides roll off frequency (f_L) in low frequency range. F_L = 3Hz (Typical application) $F_L = \frac{1}{2\pi C4.R4}$
C5 C6	9670pF 34000pF	Decides RIAA characteristics in pairs with R5 and R6.
C7	100pF	Supplies phase-compensation.
C8	470pF	In a pair with R7, decides the frequency at which Gv (OL) characteristic changes from –12dB/oct to –6dB/oct.
C9	3.3uF	Output-coupling.
C10 C11	470uF 470uF	Removes ripple on V_{CC} line.

6270

An integrated circuit combining the functions of audio amplifier and Voice Operated Gain Adjusting Device (V.O.G.A.D.), designed to accept signals from a low output microphone and to provide an essentially constant output signal of 90mV for a 60dB range of input. The dynamic range, attack and decay times are controlled by external components. Typical applications include audio A.G.C. systems, transmitter overmodulation protection, tape recorders, etc.



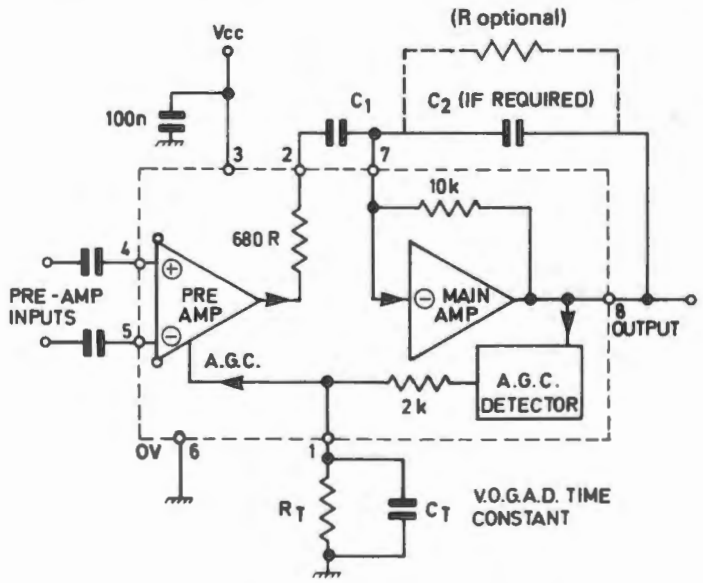
Absolute Maximum Ratings

Supply voltage V_{CC} ——— +12V
Storage temperature range T_{stg} ——— −55 to +125°C

Electrical characteristics

Parameter	Symbol	Test Conditions	min.	typ.	max.	units
Supply voltage	V_{CC}		4.5	6	10	V
Supply current	I_Q		—	5	10	mA
Input impedance	$Z_{IN(S)}$	Single ended, pin 4 or pin 5	—	150	—	Ω
Differential input impedance	$Z_{IN(D)}$	Input between pins 4 & 5	—	300	—	Ω
Voltage gain	G_V	72μV rms input pin 4	40	52	—	dB
Output level	V_{OUT}	4mV rms input pin 4	55	90	140	mV rms
Total harmonic distortion	T.H.D.	90mV input pin 4	—	2	5	%
Operating temperature range	T_{AMB}		−30		+85	°C

Figure 9



Circuit description

The principal elements of the device are shown in figure 9. The differential input preamplifier is A.G.C. controlled. The output from this stage is a.c. coupled via a capacitor to the second stage which is gain programmable by a single resistor to enable the overall sensitivity to be set. Adding a capacitor in parallel with this resistor permits the H.F. response to be tailored, if required. The output from the second stage provides the main audio output from the device, and also drives the A.G.C. detector. The detected output, which is input level dependent, is applied to the time constant circuit and the A.G.C. controlled first stage. The second stage is run in inverting mode.

RS data

Determination of gain, bandwidth, attack and decay times

The mid band gain of the second stage, which is run in parallel feedback configuration, is determined by the ratio of the 10k internal feedback resistor and the 680R resistor in series with the output of the first stage. This gain may be reduced by wiring an external feedback resistor, R_{ext}, between pins 7 and 8. The gain will then be given by the expression:

$$G = \frac{R_{ext} \times 10{,}000}{(R_{ext} + 10{,}000) \times 680} \qquad (R_{ext} \text{ in ohms})$$

The minimum permissible value for R_{ext} is 680R. The threshold point, i.e. the input level at which A.G.C. action commences, is approximately 1mV for $R_{ext} = \infty$ and approximately 8mV for $R_{ext} = 1k$.

The low frequency −3dB point is determined by the series combination of the internal 680R resistor and C_1. The high frequency −3dB point is determined by the parallel combination of the internal 10k gain-setting resistor, any external resistor R_{ext}, and C_2. Using the typical values $C_1 = 1\mu$, $C_2 = 4n7$, and $R_{ext} = \infty$, the −3dB points will occur at 234Hz and 3386Hz.

Normally the 6270 device is required to respond quickly by holding the output level almost constant as the input is increased. This "attack time", i.e. the time taken for the output to return to within 10% of the original level following a 0dB increase in the input level, will be approximately 0ms with the circuit in figure 11. It is determined by the value of C_T and can be calculated approximately by the formula:

$$\text{Attack time} \simeq 0.4\text{ms}/\mu\text{F}$$

The decay time is determined by the discharge rate of the capacitor, this being dependent on the values of R_T and C_T. For $R_T = 1M$ and $C_T = 47\mu$ the decay time is approximately 20dB/second. Other values of R_T may be used to vary the decay time for specific applications.

Figure 10(a) **Voltage gain (single ended input) – typical**

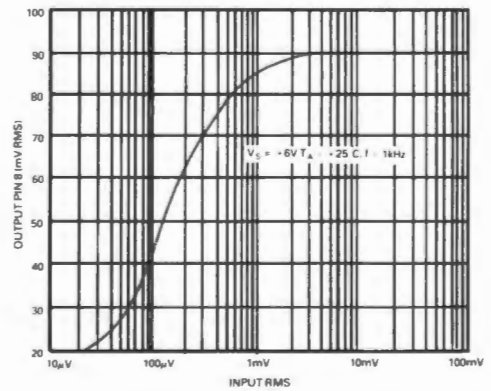
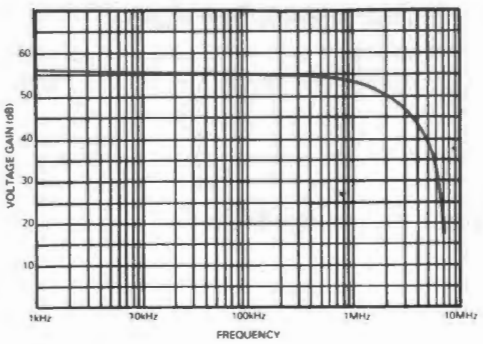


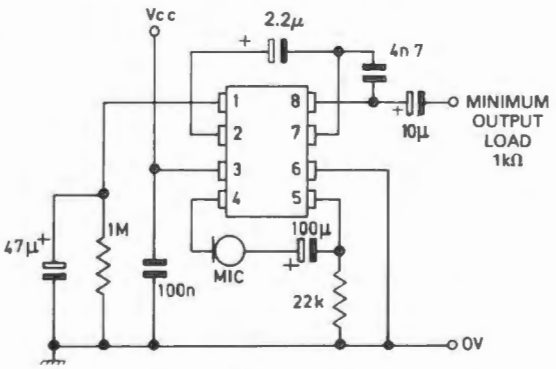
Figure 10(b) **Open loop frequency response (typical)**



Typical application

Figure 11 shows a typical application with the 6270 used as preamplifier for a 300Ω microphone. The bandwidth is approximately from 30Hz to 3,400Hz (−3dB). The input should normally be a.c. coupled, but if for any reason the coupling capacitor is omitted, the d.c. resistance between pins 4 and 5 should be less than 10 ohms. The 2k resistor

Figure 11



between pin 5 and ground is necessary to ensure that the offsets in the device at the onset of A.G.C. are of such polarity as to inhibit oscillation. If it is required to use the device with an unbalanced source, then the input may be A.C. coupled to pin 4 or pin 5, the unused input remaining floating. Any tendency to pick up noise when used in this mode may be inhibited by decoupling the unused input to ground by a 1000p capacitor. **The inputs must not be D.C. grounded.**

Bandwidth, gain, attack and decay times may be altered in accordance with the information given above to suit the differing requirements of specific applications.

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RS data

Adjustable voltage and current regulator L200

Stock number 632-944

The L200 is a monolithic regulator featuring user programming of both the output voltage and current-limit over the range of 2.85 to 36V and up to 2A respectively. In addition to current limit it has on board power limiting, thermal shutdown and input voltage protection (up to 60V) making the L200 very robust.

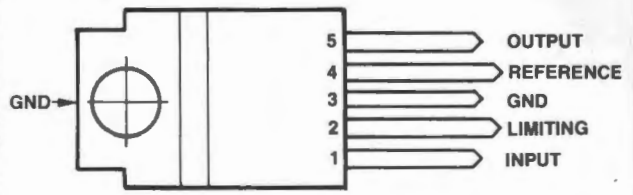
Absolute maximum ratings

V_i	dc input voltage	40V
V_i	Peak input voltage (10ms)	60V
ΔV_{i-o}	Input to output voltage	32V
I_o	Output current	internally limited
P_{tot}	Power dissipation	internally limited
T_{stg}	Storage temperature	−55 to 150°C
T_{op}	Operating junction temperature	−25 to 150°C

Features

- Adjustable output current up to 2A (guaranteed up to T_j = 150°C)
- Adjustable output voltage down to 2.85V
- Input overvoltage protection (up to 60V, 10ms)
- Short circuit protection
- Output transistor S.O.A. protection
- Thermal overload protection
- Low bias current on regulation pin
- Low standby current drain.

Pin connections



Front view

Electrical characteristics (T_{amb} = 25°C, unless otherwise specified)

Voltage regulation loop

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_d	Quiescent drain current (pin 3)	V_i = 20V		4.2	9.2	mA
e_N	Output noise voltage	$V_o = V_{ref}$ I_o = 10mA B = 1MHz		80		μV
V_o	Output voltage range	I_o = 10mA	2.85		36	V
$\frac{\Delta V_o}{V_o}$	Load voltage regulation (note 1)	ΔI_o = 2A ΔI_o = 1.5A		0.15 0.1	1 0.9	% %
$\frac{\Delta V_i}{\Delta V_o}$	Line regulation	V_o = 5V V_i = 8 to 18V	48	60		dB
SVR	Supply voltage rejection	V_o = 5V I_o = 500mA $\Delta V_i = 10V_{pp}$ f = 100Hz (note 2)	48	60		dB

Note 1. A load step of 2A can be applied provided that input-output differential voltage is lower than 20V (see Figure 2).
Note 2. The same performance can be maintained at higher output levels if a bypassing capacitor is provided between pins 2 and 4.

Electrical characteristics (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
ΔV_{i-o}	Dropout voltage between pins 1 and 5	$I_o = 1.5A$	$\Delta V_o \leq 2\%$		2	2.5	V
V_{ref}	Reference voltage (pin 4)	$V_i = 20V$	$I_o = 10mA$	2.64	2.77	2.86	V
ΔV_{ref}	Average temperature coefficient of reference voltage	$V_i = 20V$	$I_o = 10mA$ for $T_j = -25$ to 125°C for $T_j = 125$ to 150°C		 –0.25 –1.5		 mV/°C mV/°C
I_4	Bias current at pin 4				3	10	μA
$\frac{\Delta I_4}{\Delta T \cdot I_4}$	Average temperature coefficient (pin 4)				–0.5		%/°C
Z_o	Output impedance	$V_i = 10V$ $I_o = 0.5A$	$V_o = V_{ref}$ f = 100Hz		1.5		mΩ

Current regulation loop

V_{SC}	Current limit sense voltage between pins 5 and 2	$V_i = 10V$ $I_5 = 100mA$	$V_o = V_{ref}$	0.38	0.45	0.52	V
$\frac{\Delta V_{sc}}{\Delta T \cdot V_{sc}}$	Average temperature coefficient of V_{SC}				0.03		%/°C
$\frac{\Delta I_O}{I_O}$	Current load regulation	$V_i = 10V$ $I_O = 0.5A$ $I_O = 1A$ $I_O = 1.5A$	$\Delta V_O = 3V$		 1.4 1 0.9		 % % %
I_{SC}	Peak short circuit current	$V_i - V_o = 14V$ (pins 2 and 5 short circuited)				3.6	A

Thermal data

$R_{th\ j\text{-}case}$	Thermal resistance junction-case	max 3°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max 50°C/W

Figure 1 **Block diagram**

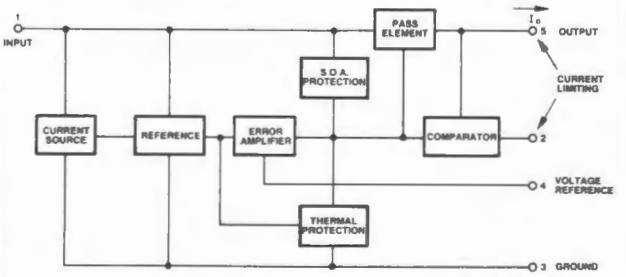


Figure 2 **Package details**

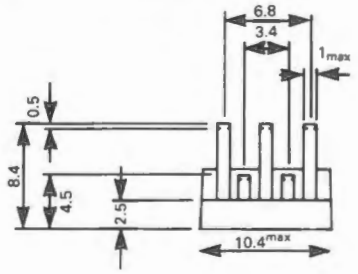


Figure 3 **Typical safe operating area protection**

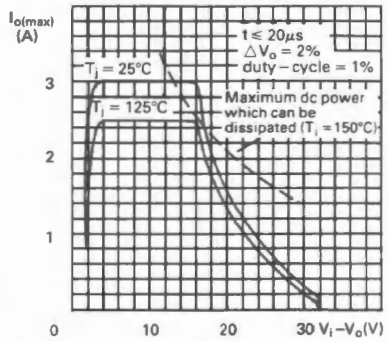


Figure 4 **Quiescent current vs. junction temperature**

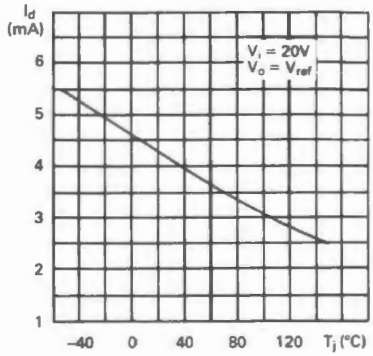


Figure 5 **Quiescent current vs. output current**

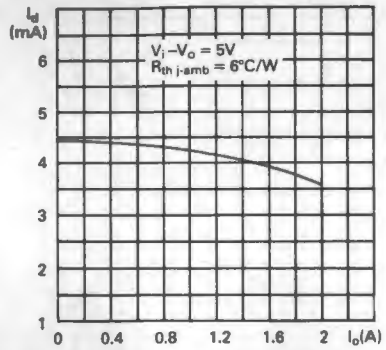


Figure 6 **Output noise voltage vs. output voltage**

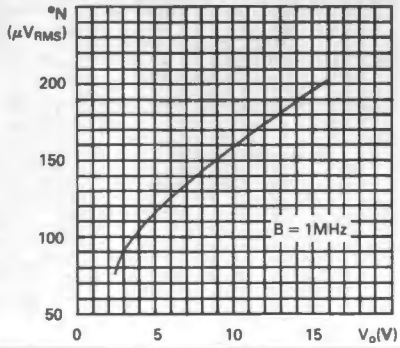


Figure 7 **Output noise voltage vs. frequency**

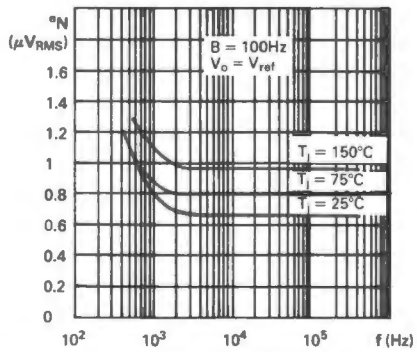


Figure 8 **Reference voltage vs. junction temperature**

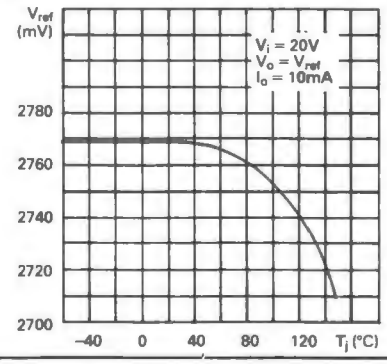


Figure 9 **Dropout voltage vs. junction temperature**

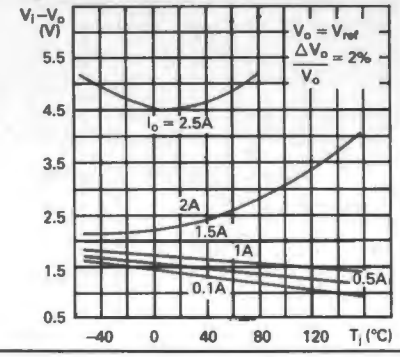


Figure 10 **Output impedance vs. frequency**

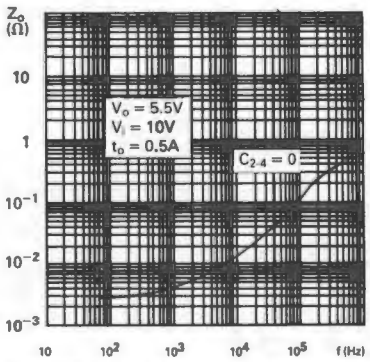


Figure 11 **Current limit sense voltage vs. junction temperature**

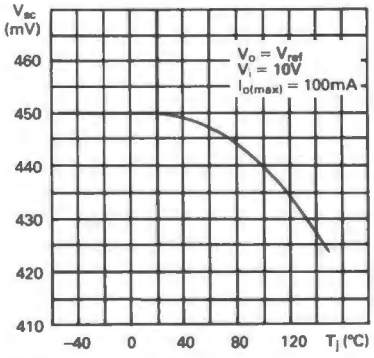


Figure 12 **Voltage transient response**

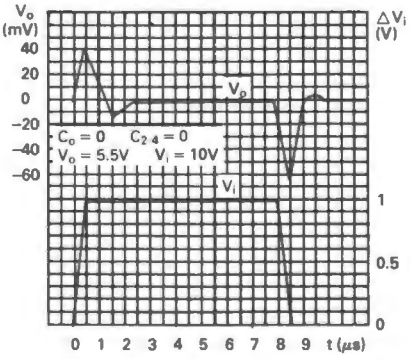


Figure 13 **Load transient response**

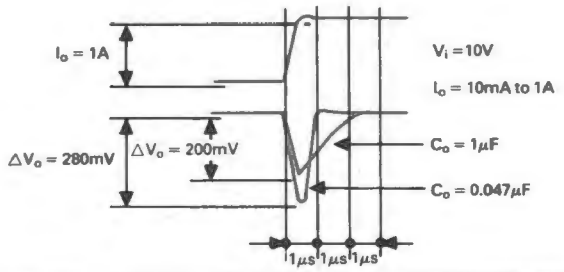
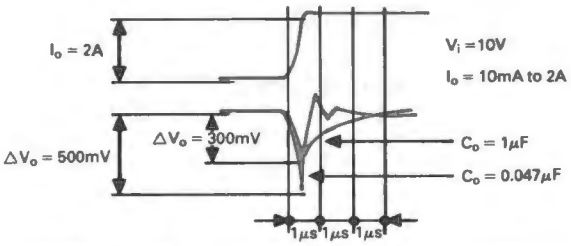


Figure 14 **Load transient response**



Application circuits

Figure 15 **Programmable voltage regulator**

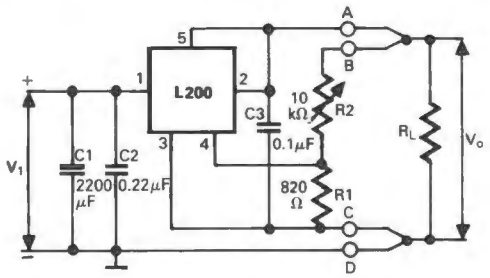


Figure 16 **Programmable voltage regulator with current limiting**

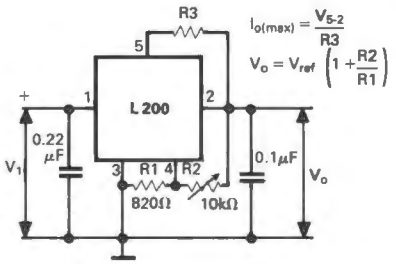


Figure 17 **Programmable current regulator**

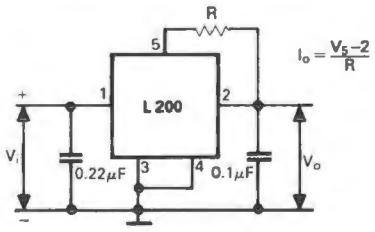


Figure 18 **Digitally selected regulator with inhibit**

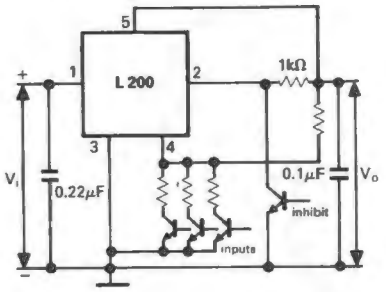
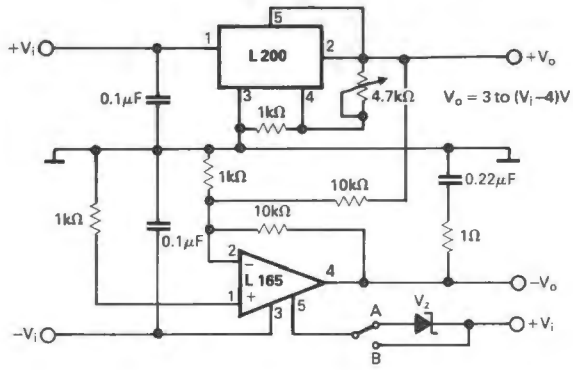


Figure 19 **High current tracking regulator**

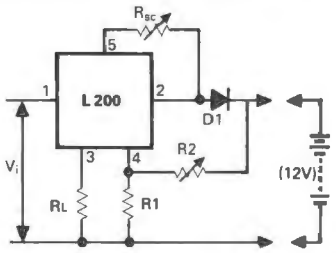


A: for $\pm 18 \leqslant V_i \leqslant \pm 32$

Note. V_z must be chosen in order to verify $2V_i - V_z \leqslant 36V$

B: for $V_i \leqslant \pm$ 18V

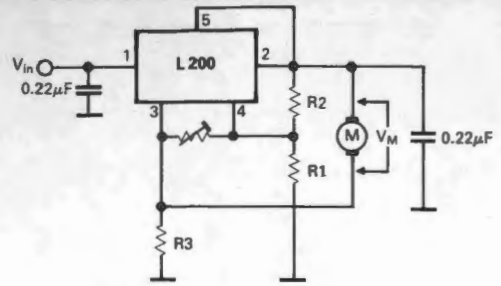
Figure 20 **Constant current battery charger**



Resistors R_1 and R_2 determine the final charging voltage and R_{sc} the initial charging current. D_1 prevents discharge of the battery through the regulator.

The resistor R_L limits the reverse currents through the regulator (which should be 100 mA max) when the battery is accidentally reverse connected. If R_L is in series with a bulb of 12V/50mA rating this will indicate incorrect connection.

Figure 21 **30W motor speed control**



$$R_3 = \frac{R_1}{R_2} \cdot R_M$$

$$V_M = V_{ref} \cdot (1 + \frac{R_2}{R_1})$$

Figure 22 **Light controller**

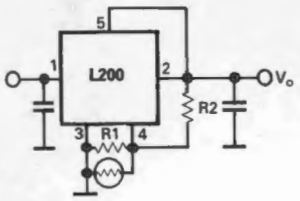
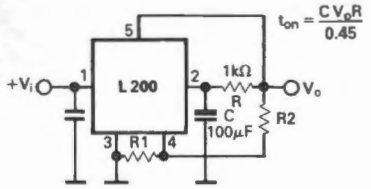


Figure 23 **Low turn on**



RS data

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An Electrocomponents Group Company

Telephone: 0536 201234
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RS data

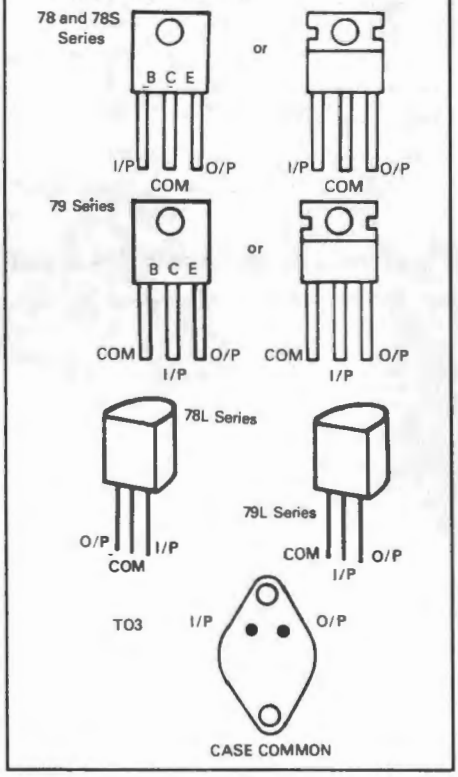
Fixed voltage series regulators

A range of 23 fixed voltage linear regulators with outputs covering a wide range of positive or negative output voltages.

Quick selection table

Description	Output Voltage	Output Current	Case	Stock No.	Suitable transformer Stock No.	Sec. Voltage	VA
78L05	5V	100mA	T092	**306-190**	207-188	9(S)	6
RS309K (LM309K)	5V	1.2A	T03	**305-614**	207-122	9(S)	20
7805	5V	1.0A	T0220	**305-888**	207-122	9(S)	20
78S05	5V	2A	T0220	**633-026**	207-239	9(S)	50
78H05	5V	5A	T03	**307-301**	207-239	9(S)	50
78L12	12V	100mA	T092	**306-207**	207-217	15(P)	6
7812	12V	1.0A	T0220	**305-894**	207-267	15(P)	50
78S12	12V	2A	T0220	**633-032**	207-267	15(P)	50
78H12	12V	5A	T03	**307-317**	207-289	12(S)	100
78L15	15V	100mA	T092	**306-213**	207-217	15(P)	6
7815	15V	1.0A	T0220	**305-901**	207-267	15(P)	50
78S15	15V	2A	T0220	**633-048**	207-267	15(P)	50
78L24	24V	100mA	T092	**306-229**	207-201	24(S)	6
7824	24V	1.0A	T0220	**305-917**	207-251	24(S)	50
78S24	24V	2A	T0220	**633-054**	207-295	24(S)	100
79L05	–5V	–100mA	T092	**306-235**	207-188	9(S)	6
7905	–5V	–1.2A	T0220	**306-049**	207-122	9(S)	20
79L12	–12V	–100mA	T092	**306-241**	207-217	15(P)	6
7912	–12V	–1.2A	T0220	**306-055**	207-267	15(P)	50
79L15	–15V	–100mA	T092	**306-251**	207-217	15(P)	6
7915	–15V	–1.2A	T0220	**305-923**	207-267	15(P)	50
79L24	–24V	–100mA	T092	**306-263**	207-201	24(S)	6
7924	–24V	–1.0A	T0220	**306-184**	207-251	24(S)	50

Pin connections



Electrical characteristics – Positive regulators

Parameter \ Type	78H05	78H12	78S05	78S12	78S15	78S24	RS309K	Units
Voltage output	**5**	**12**	**5**	**12**	**15**	**24**	**5**	V
Current output	5	5	2	2	2	2	1.2	A
Input voltage range	8 to 25	15 to 25	8 to 35	15 to 35	18 to 35	27 to 40	7 to 35	V
Load regulation	0.5	0.17	2	1.33	1.2	1.04	1	%
Ripple rejection	60	60	60	53	52	48	70	dB
Output impedance	2	2	17	18	19	28	50	mΩ
Line regulation	0.2	0.17	2	2	2	2	0.1	%
Output noise voltage	40	75	40	75	90	170	40	μV
Short circuit current	7	7	0.5	0.5	0.5	0.5	dependant on V_{IN}	A
Max. operating junction temperature	150*	150*	150*	150*	150*	150*	125	°C
Total power dissipation	50	50	–	–	–	–	12.75	W
Thermal resistance (junction to case)	2	2	3	3	3	3	3	°C/W
Thermal resistance (junction to ambient)	33	33	50	50	50	50	35	°C/W

*** T case = 25°C (internally limited), derate linearly to 0W at 150°C.**

Electrical characteristics – Positive regulators (cont.)

Parameter \ Type	7805	7812	7815	7824	78L05	78L12	78L15	78L24	Units
Voltage output	**5**	**12**	**15**	**24**	**5**	**12**	**15**	**24**	V
Current output	1	1	1	1	0.1	0.1	0.1	0.1	A
Input voltage range	7 to 25	14.5 to 30	17.5 to 30	27 to 38	7 to 30	14.5 to 35	17.5 to 35	27 to 35	V
Load regulation	0.2	0.4	0.5	0.6	0.2	0.2	0.3	0.4	%
Ripple rejection	70	61	60	56	60	55	52	49	dB
Output impedance	30	75	95	150	200	200	200	200	mΩ
Line regulation	0.2	0.2	0.3	0.3	1	1	1.5	1.5	%
Output noise voltage	40	80	90	170	40	60	90	200	μV
Short circuit current	0.75	0.35	0.23	0.15	–	–	–	–	A
Max. operating junction temperature	150*	150*	150*	150*	125	125	125	125	°C
Total power dissipation	20	20	20	20	0.9	0.9	0.9	0.9	W
Thermal resistance (junction to case)	4	4	4	4	N/A	N/A	N/A	N/A	°C/W
Thermal resistance (junction to ambient)	50	50	50	50	180	180	180	180	°C/W

* T case = 25°C (internally limited), derate linearly to 0W at 150°C.

Electrical characteristics – Negative regulators

Parameter \ Type	7905	7912	7915	7924	79L05	79L12	79L15	79L24	Units
Voltage output	**–5**	**–12**	**–15**	**–24**	**–5**	**–12**	**–15**	**–24**	V
Current output	1	1	1	1	0.1	0.1	0.1	0.1	A
Input voltage range	–7 to –25	–14.5 to –30	–17.5 to –30	–27 to –38	–7 to –25	–14.5 to –35	–17.5 to –35	–27 to –35	V
Load regulation	0.2	0.4	0.5	0.6	0.2	0.2	0.3	0.4	%
Ripple rejection	70	61	60	56	60	55	52	49	dB
Output impedance	30	75	95	150	200	200	200	200	mΩ
Line regulation	0.2	0.2	0.3	0.3	1	1	1.5	1.5	%
Output noise voltage	40	80	90	170	40	60	90	200	μV
Short circuit current	0.75	0.35	0.23	0.15	–	–	–	–	A
Max. operating junction temperature	150*	150*	150*	150*	125	125	125	125	°C
Total power dissipation	20	20	20	20	0.9	0.9	0.9	0.9	W
Thermal resistance (junction to case)	4	4	4	4	N/A	N/A	N/A	N/A	°C/W
Thermal resistance (junction to ambient)	50	50	50	50	180	180	180	180	°C/W

* T case etc. = 25°C (internally limited), derate linearly to 0W at 150°C.

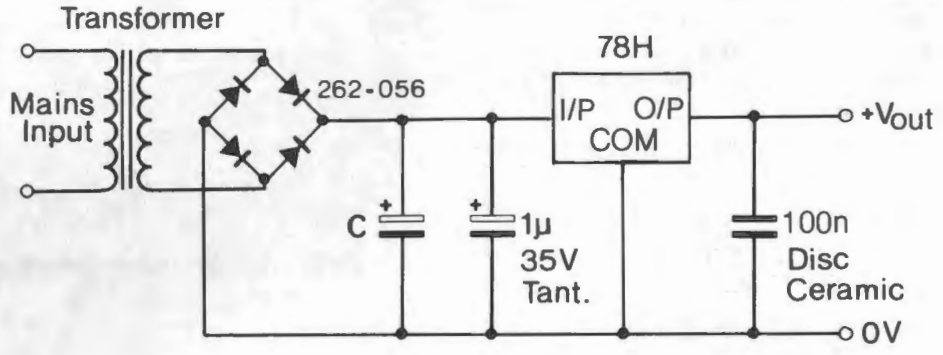
78H05 and 78H12 fixed hybrid regulators

Two fixed voltage hybrid regulators, housed in TO3 style metal cases, capable of supplying output currents up to 5 amps. The internal circuitry limits the junction temperature to a safe value and provides automatic thermal overload protection. Safe operating protection is also incorporated making the regulators virtually damage proof.

In order to achieve maximum performance the internal power dissipation must be kept below 50W. Transformer and heatsink selections are dependent upon the exact application.

78H – Basic circuit, fixed voltage

Figure 1



Regulator	Output voltage	Transformer	Heatsink	C
78H05	+5V dc	207-239 (S)	401-807, 1.1°c/w	15,000µF 16V
78H12	+12V dc	207-289 (S)	401-403, 2.1°c/w	22,000µ 25V

Fixed voltage monolithic regulators

Figure 2 **Basic circuit – 78 series positive regulators**

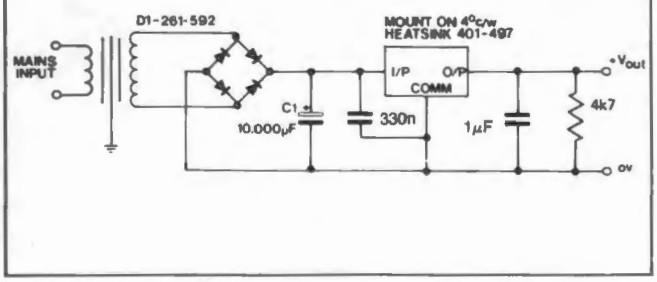


Figure 3 **Basic circuit – 79 series negative regulators**

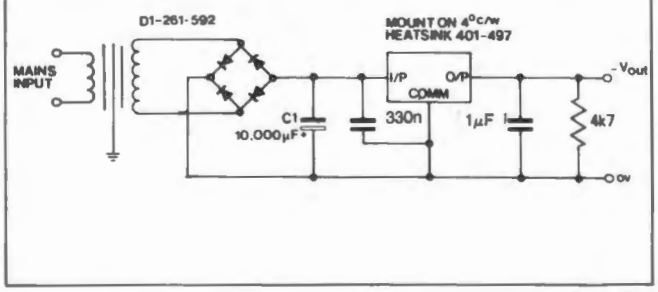
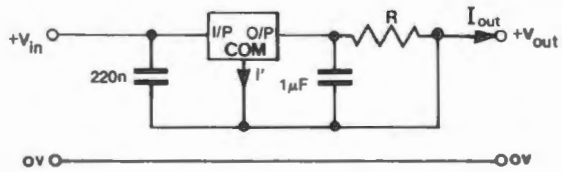


Figure 4 **Constant current generator**



For T03 types	I' = 10mA typ.
For 78S series	I' = 8mA typ.
For 78/79 series	I' = 4.5mA typ.
For 78L/79L series	I' = 3.5mA typ.

Circuit gives constant current through load provided V_{out} does not exceed $V_{in} - (V_R + 2.5)$. [$V_{in} - (V_R + 3)$ for 78S series]. Select R to give designed constant current I_{out}

$$I_{out} = \frac{V_R}{R} + I'$$

Where V_R is the basic regulator voltage.

RS data

Increasing basic regulator voltage

The input voltage V_{in} should be derived from a suitable transformer, rectifier and smoothing capacitor circuit. Note V_{in} must be greater (within maximum ratings) than $V_{out} + 2.5V$.

Figure 5 – gives higher output voltage than basic circuit but with reduced regulation.

$$V_{out} = V_R (1 + \frac{R_2}{R_1}) + I'R_2$$

$$I_{R1} \geq 5 \times I'$$

where V_R = basic regulator voltage
I' = 10mA (T03)
= 8mA (78S series)
= 4.5mA (78/79 series)
= 3.5mA (78L/79L series)

Figure 5

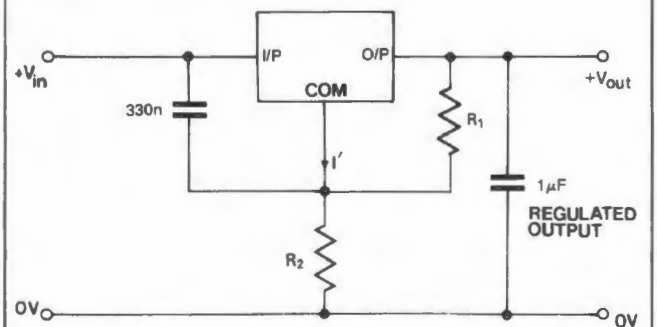


Figure 6 – gives better regulation than Figure 5.

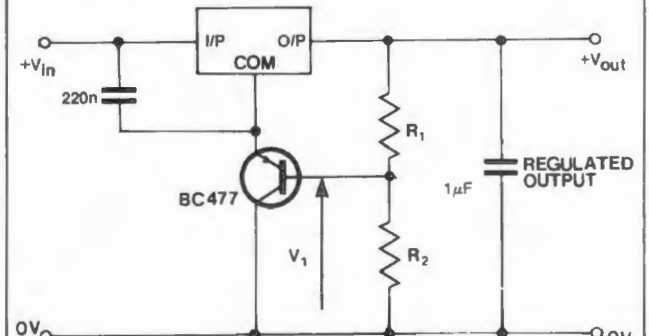
$$V_{out} = V_R + V_1 + 0.6$$

$$\text{where } V_1 = \frac{R_2 V_{out}}{R_1 + R_2}$$

$$\text{and } \frac{R_1}{R_2} = \frac{V_R + 0.6}{V_{out} - (V_R + 0.6)}$$

e.g. For 9V output with 5V regulator
R1 = 5k6 R2 = 3k3

Figure 6



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RS data

Regulating pulse width modulator SG3524

Stock number 633-789

The SG3524 incorporates on a single monolithic chip all the functions required for the construction of regulating power supplies inverters or switching regulators. It can also be used as the control element for high power output applications. The SG3524 was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. The device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry.

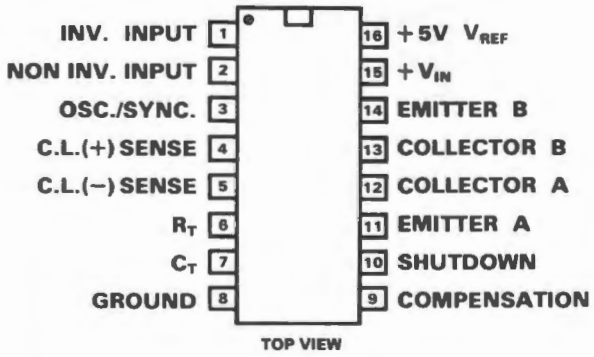
Features

- Complete PWM power control circuitry
- Uncommitted outputs for single-ended or push-pull applications
- Low standby current, typically 8mA
- Operation up to 300kHz
- 1% maximum temperature variation of reference voltage.

Absolute maximum ratings

Supply voltage ——— 40V
Collector output current ——— 100μA
Reference output current ——— 50mA
Current through C_T terminal ——— −5mA
Total power dissipation at T_{amb} = 70°C ——— 1W
Storage temperature range ——— −65°C to +150°C
Operating temperature range ——— 0 to +70°C

Pin connections



Electrical characteristics T_j = 0°C to +70°C, V_{IN} = 20V, f = 20kHz unless otherwise stated.

Parameter		Test condition	Min.	Typ.	Max.	Unit
Reference section						
V_{REF}	Output voltage		4.6	5	5.4	V
ΔV_{REF}	Line regulation	V_{IN} = 8 to 40V		10	30	mV
ΔV_{REF}	Load regulation	I_L = 0 to 20mA		20	50	mV
	Ripple rejection	f = 120Hz, T_j = 25°C		66		dB
	Short circuit current limit	V_{REF} = 0, T_j = 25°C		100		mA
$\Delta V_{REF}/\Delta T$	Temperature stability	Over operating temperature range		0.3	1	%
ΔV_{REF}	Long term stability	T_j = 25°C, t = 1000hours		20		mV
Oscillator section						
f_{MAX}	Maximum frequency	C_T = 0.001μF, R_T = 2kΩ		300		kHz
	Initial accuracy	R_T and C_T constant		5		%
	Voltage stability	V_{IN} = 8 to 40V, T_j = 25°C			1	%
$\Delta f/\Delta T$	Temperature stability	Over operating temperature range			2	%
	Output amplitude	Pin 3, T_j = 25°C		3.5		V
	Output pulse width	C_T = 0.01μF, T_j = 25°C		0.5		μs

Parameter		Test condition	Min.	Typ.	Max.	Unit
Error amplifier section						
V_{OS}	Input offset voltage	V_{CM} = 2.5V		2	10	mV
I_b	Input bias current	V_{CM} = 2.5V		2	10	μA
G_V	Open loop voltage gain		60	80		dB
CMV	Common mode voltage	T_j = 25°C	1.8		3.4	V
CMR	Common mode rejection	T_j = 25°C		70		dB
B	Small signal bandwidth	A_v = 0dB, T_j = 25°C		3		MHz
V_O	Output voltage	T_j = 25°C	0.5		3.8	V
Comparator section						
	Duty-cycle	% Each output On	0		45	%
V_{IT}	Input threshold	Zero duty-cycle		1		V
V_{IT}	Input threshold	Maximum duty-cycle		3.5		V
I_b	Input bias current			1		μA
Current limiting section						
	Sense voltage	Pin 9 = 2V with error amplifier Set for maximum out, T_j = 25°C	180	200	220	mV
	Sense voltage TC			0.2		mV/°C
CMV	Common mode voltage		–1		+1	V
Output section (each output)						
	Collector-emitter voltage		40			V
	Collector leakage current	V_{CE} = 40V		0.1	50	μA
	Saturation voltage	I_c = 50mA		1	2	V
	Emitter output voltage	V_{IN} = 20V	17	18		V
t_r	Rise time	R_c = 2kΩ, T_j = 25°C		0.2		μs
t_f	Fall time	R_c = 2kΩ, Tj = 25°C		0.1		μs
I_q*	Total standby current	V_{IN} = 40V		8	10	mA

(*) Excluding oscillator charging current, error and current limit dividers, and with outputs open.

Thermal data

$R_{th\ j\text{-}amb}$	Thermal resistance junction – ambient				80	°C/W

Typical performance characteristics

Figure 1 **Open-loop voltage amplification of error amplifier vs. frequency**

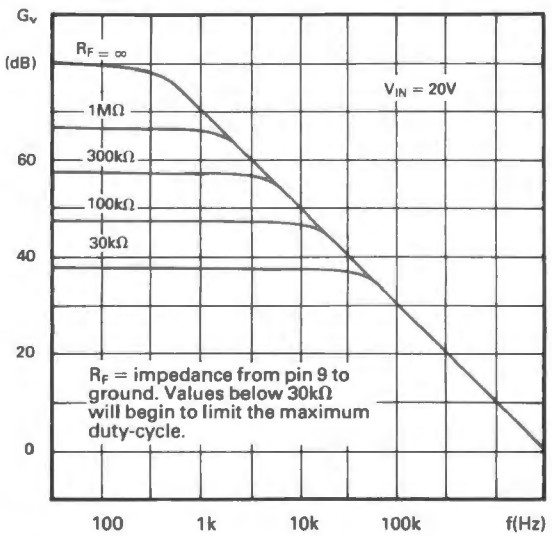


Figure 2 **Oscillator frequency vs. timing components**

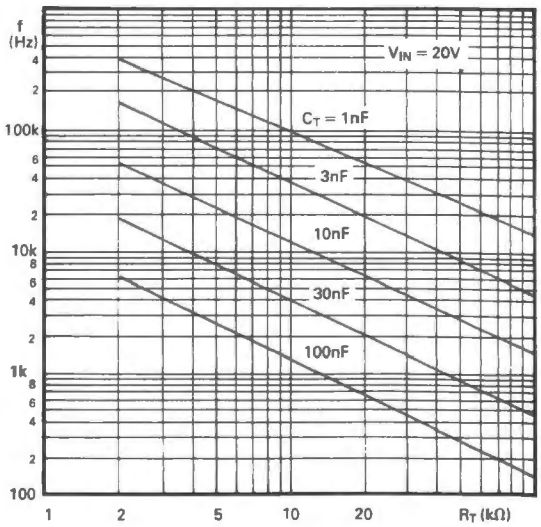


Figure 3 **Output dead time vs. timing capacitance value**

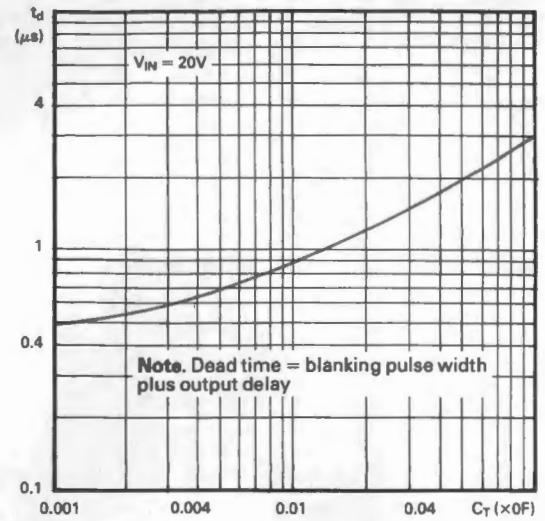


Figure 4 **Output saturation voltage vs. load current**

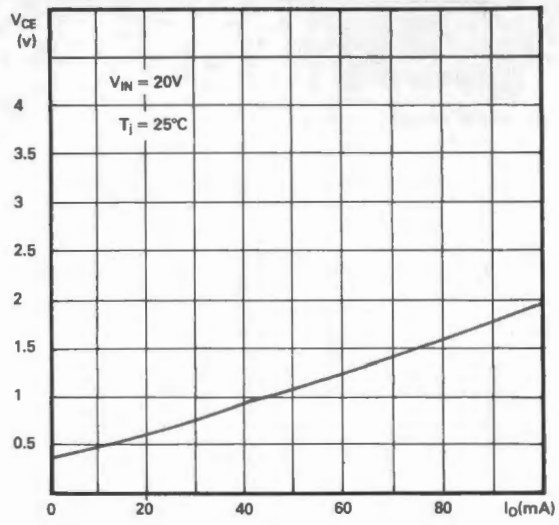
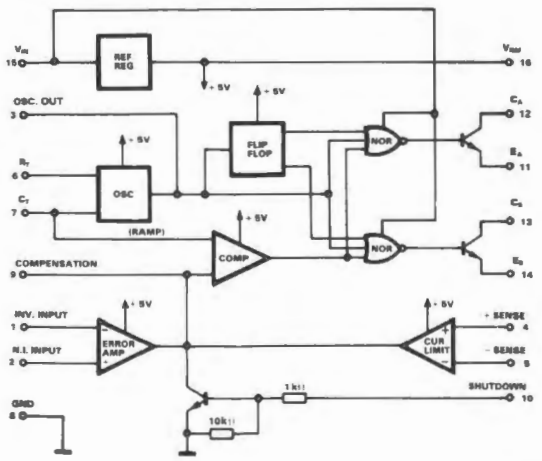


Figure 5 **Block diagram**



Principles of operation

The SG3524 is a fixed-frequency pulse-with-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T) and one timing capacitor (C_T). R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The SG3524 contains, an on-board 5V regulator that serves as a reference as well as powering the SG3524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistors (Q_A or Q_B) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to ensure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier, or to provide additional control to the regulator.

Recommended operating conditions

Supply voltage V_{IN}	8 to 40V
Reference output current	0 to +20mA
Current through C_T terminal	−0.03 to −2mA
Timing resistor, R_T	1.8 to 100kΩ
Timing capacitor, C_T	0.001 to 0.1μF

Typical applications data

Oscillator

The oscillator controls the frequency of the SG3524 and is programmed by R_T and C_T according to the approximate formula:

$$F \simeq \frac{1.18}{R_T C_T}$$

Where R_T is in kΩ
C_T is in μF
f is in kHz

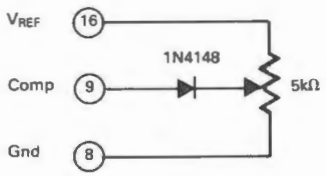
Practical values of C_T fall between 0.001 and 0.1μF. Practical values of R_T fall between 1.8 and 100kΩ. This results in a frequency range typically from 120Hz to 500kHz.

RS data

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit shown in Figure 6.

Figure 6 **Blanking**



Synchronous operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2kΩ. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more SG3524 regulators are to be operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to a single timing capacitor, and the timing resistor connected to a single R_T terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between C_T terminals.

The transformers and chokes, used in Figures 7 and 8, can be constructed using SMPS Ferrox cores, see current RS catalogue for details.

Figure 7 **Push-pull transformer-coupled circuit**

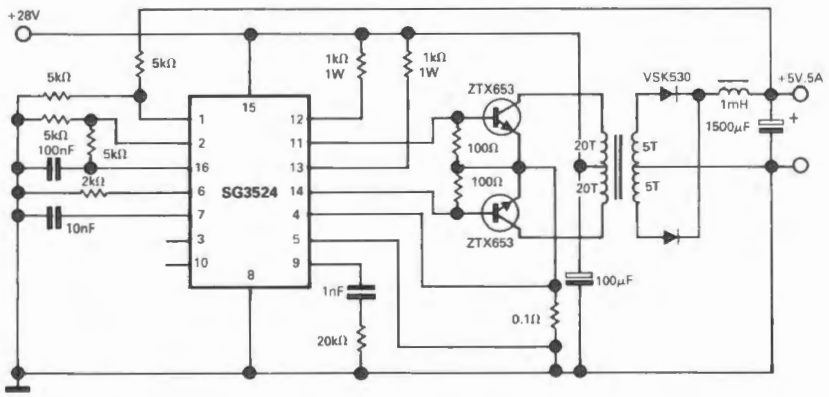
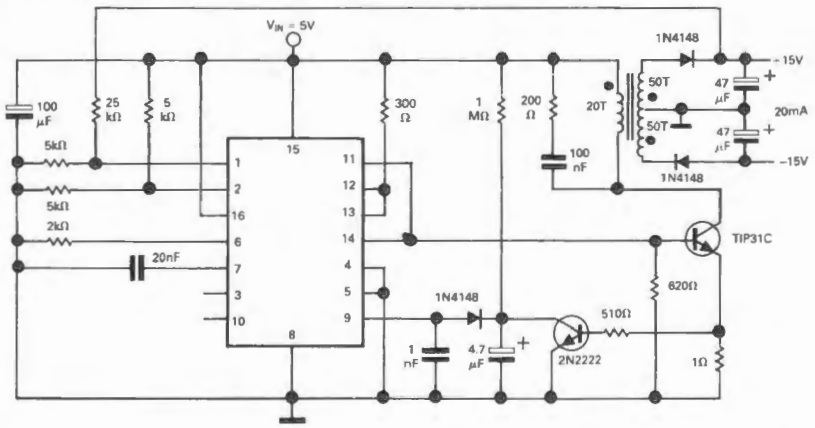


Figure 8 **Flyback converter circuit**



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RS data

Dual switched capacitor instrumentation building block LTC1043

Stock number 633-896

The LTC1043 is a charge-balanced, dual switched-capacitor instrumentation building block manufactured using the silicon gate LTCMOS™ process. A pair of switches alternately connects an external capacitor to an input voltage and then connects the charged capacitor across an output port. The switches have a break-before-make action. An internal clock is provided and its frequency can be adjusted with an external capacictor or the LTC1043 can be driven with an external C-MOS clock.

When used with low clock frequencies the LTC1043 provides ultra precision dc functions without the need for precise external components. Such functions are differential voltage to single-ended conversion, voltage inversion, voltage multiplication by 2, 3, 4, 5, etc. The LTC1043 can also be used for precise V to F and F to V circuits without the need for trimming, and may be used as a building block for switched capacitor filters, oscillators and sample and hold circuits. Operates from 3V to 18V. 18-pin dil plastic package. Equivalent to LTC1043CN.

Absolute maximum ratings

Supply voltage _____ 18V

Input voltage at any pin ___ $-0.3V \leq V_{IN} \leq V^+ + 0.3V$

Operating temperature range ___ $-40°C \leq T_A \leq 85°C$

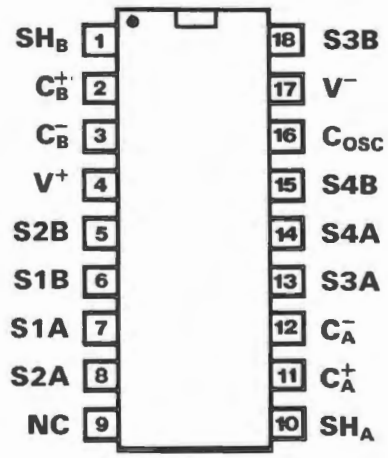
Storage temperature range _____ –65°C to 150°C

Lead temperature (soldering, 10 sec.) _____ 300°C

Features

- Instrumentation front end with 120dB CMRR
- Precise, charge-balanced switching
- Operates from 3V to 18V
- Internal or external clock
- Operates up to 5MHz clock rate
- Low power
- Two independent sections with one clock.

Pin connections



ATTENTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

LTCMOS™ is a trademark of Linear Technology Corporation

Electrical characteristics ($V^+ = 10V$, $V^- = 0V$, $T_A = 25°C$ unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S	Power supply current	Pin (16) connected high or low		0.25	0.4 0.7	mA mA
		C_{OSC} (pin 16 to V^-) = 100pF		0.4	0.65 1	mA mA
I_I	OFF leakage current	Any switch		6		nA
R_{ON}	ON resistance	V_{IN} = 7V, I = ±0.5mA V^+ = 10V, V^- = 0V		240	400 700	Ω Ω
R_{ON}	ON resistance	V_{IN} = 3.1V, I = ±0.5mA V^+ = 5V. V^- = 0V		400	700 1	Ω kΩ
f_{OSC}	Internal oscillator frequency	C_{OSC} (pin 16 to V^-) = 0pF C_{OSC} (pin 16 to V^-) = 100pF	 20	185 34	 50	kHz kHz
I_{OSC}	Pin source or sink current	Pin 16 at V^+ or V^-		40	70 100	μA μA
	Break-before-make time			25		ns
	Clock to switching delay	C_{OSC} pin externally driven		75		ns
f_M	Maximum external CLK frequency	C_{OSC} pin externally driven with CMOS levels		5		MHz
CMRR	Common-mode rejection ratio	V^+ = 5V, V^- = –5V, –5V < V_{CM} < 5V, dc to 400Hz		120		dB

Characteristic curves

Figure 1 **Power supply current vs. power supply voltage**

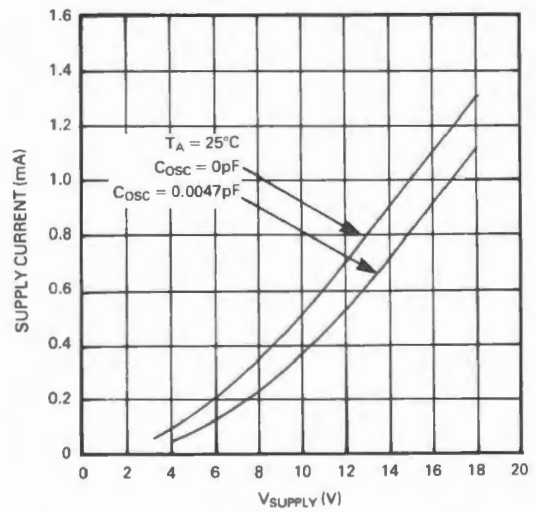


Figure 2 **R_{ON} vs. V_{IN}**

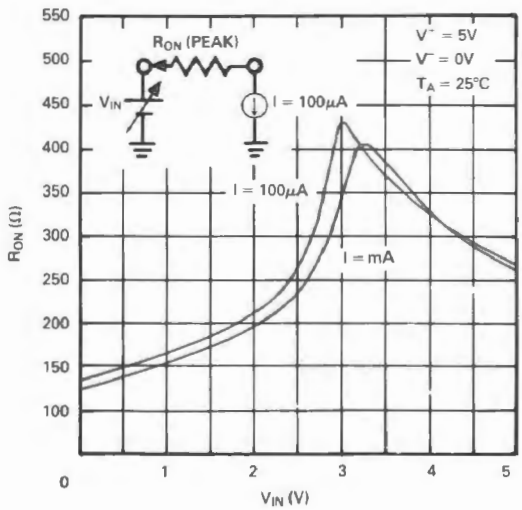


Figure 3 **R_{ON} vs. V_{IN}**

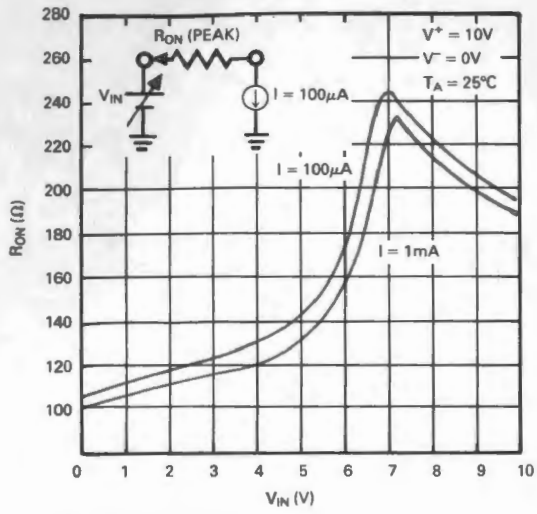


Figure 4 **R_{ON} vs. V_{IN}**

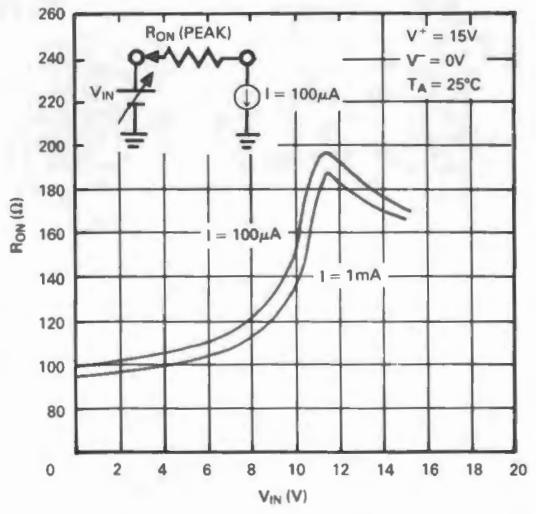


Figure 5 **R_{ON} (peak) vs. power supply voltage**

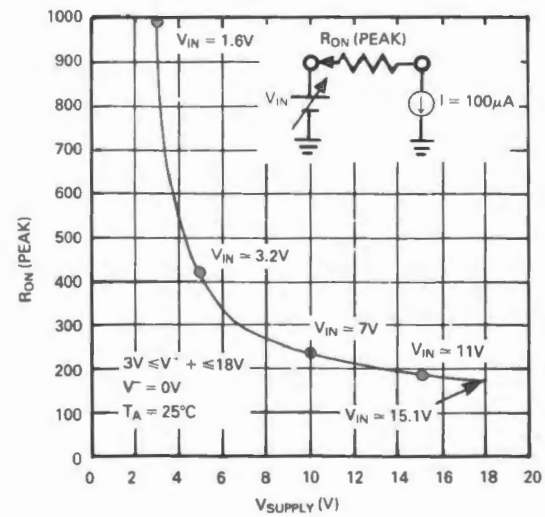


Figure 6 **R_{ON} (peak) vs. power supply voltage**

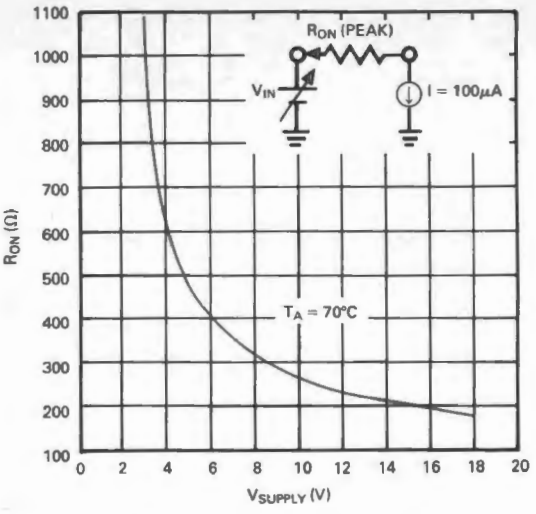


Figure 7 **Oscillator frequency, f_{osc}, vs. C_{osc}**

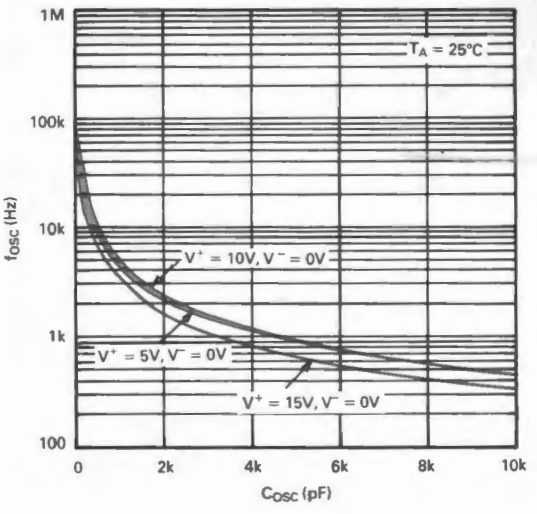


Figure 8 **Oscillator frequency, f_{osc}, vs. supply voltage**

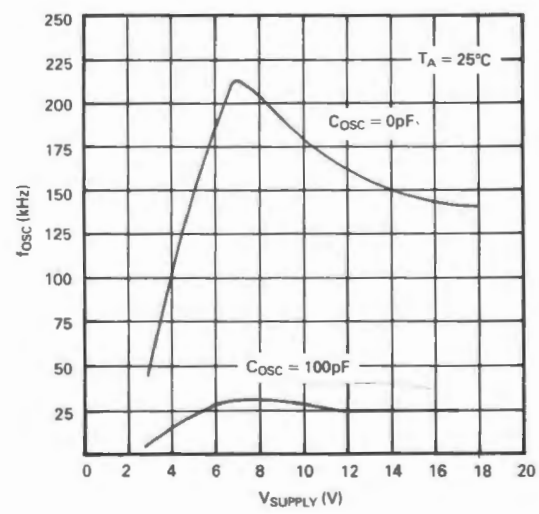


Figure 9 **Normalised oscillator frequency, f_{osc}, vs. supply voltage**

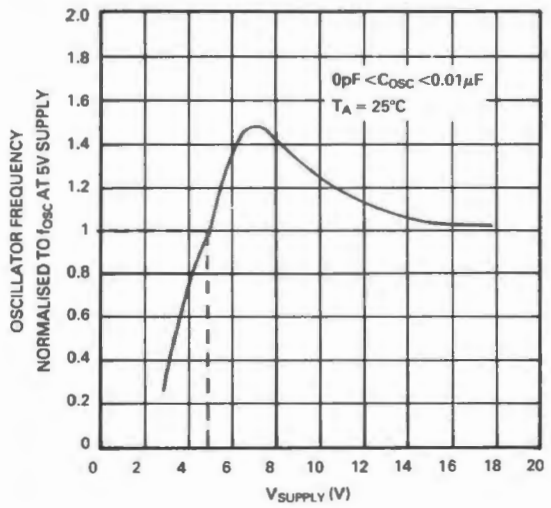


Figure 10 **Oscillator frequency, f_{osc}, vs. ambient temperature, T_A**

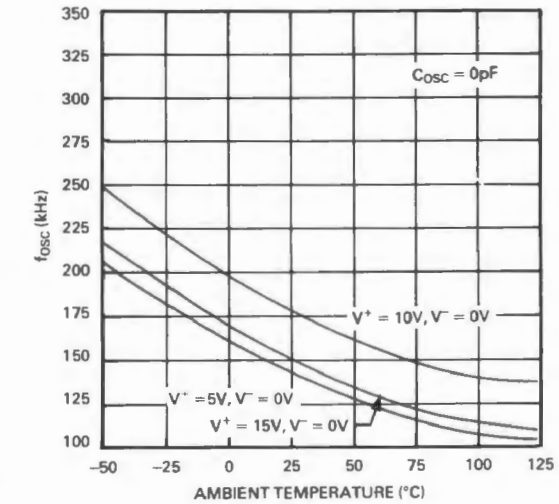


Figure 11 **C_{osc} pin I_{SINK}, I source vs. supply voltage**

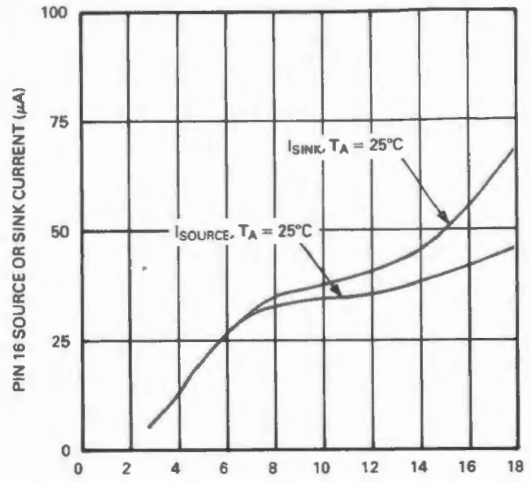


Figure 12 **Break before make time, t_{nov}, vs. supply voltage**

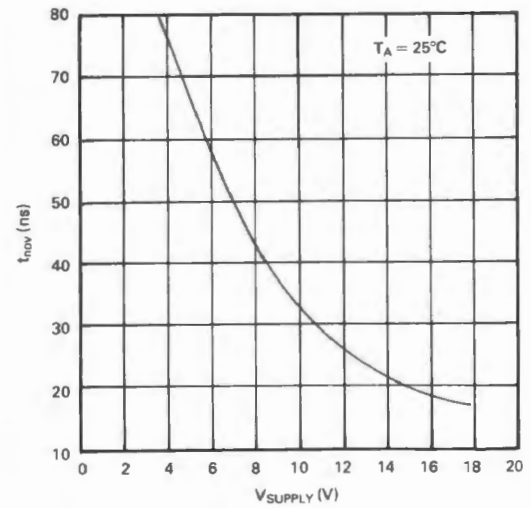
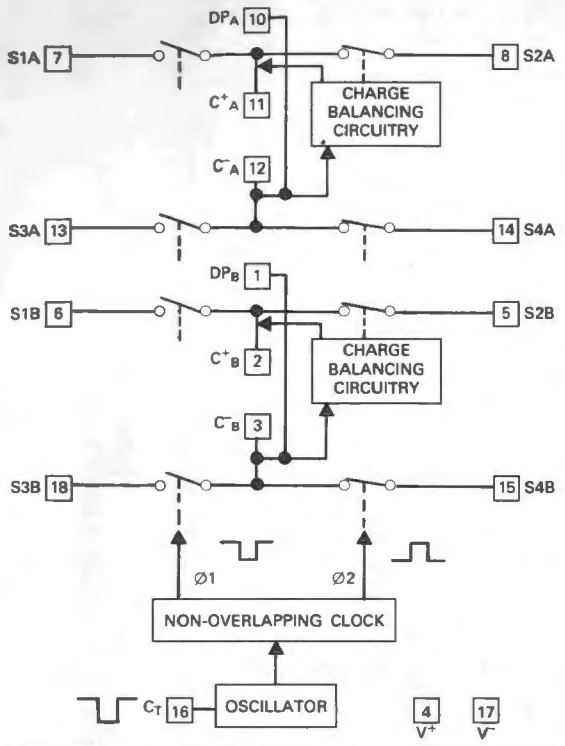


Figure 13 **Block diagram showing individual switches**

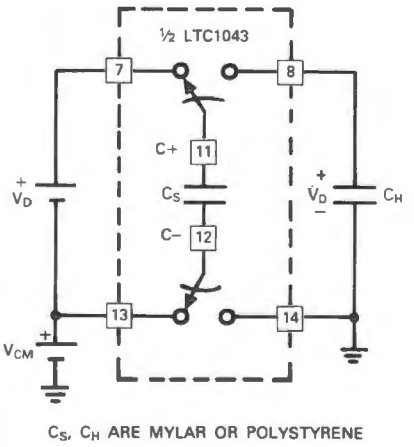


Device description

Common-mode rejection ratio (CMRR)

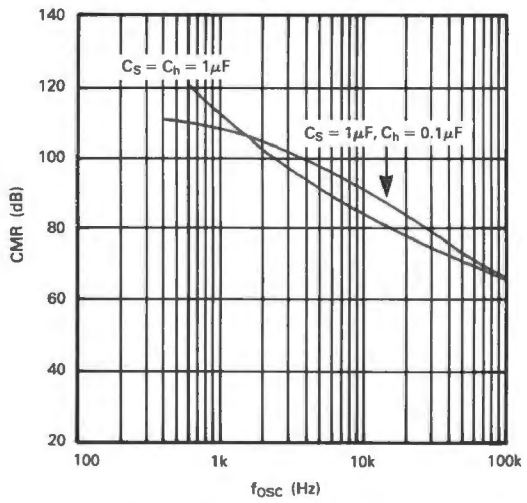
The LTC1043, when used as a differential to single-ended converter (Figure 14) rejects common-mode signals and preserves differential voltages. Unlike other techniques, the LTC1043's CMRR does not degrade with increasing common-mode voltage frequency. During the sampling mode, the impedance of pins 2, 3 (and 11, 12) should be reasonably balanced, otherwise, common-mode signals will appear differentially. The value of the CMRR depends on the value of the sampling and holding capacitors (C_S, C_H) and the sampling frequency. Since the common-mode voltages are not sampled, the common-mode signal frequency can well exceed the sampling frequency without experiencing aliasing phenomena. The CMRR of Figure 14 is measured by shorting pins 7 and 13 and by observing, with a precision DVM, the change of the voltage across C_H with respect to an input CM voltage variation. During the sampling and holding mode, charges are being transferred and minute voltage transients will appear across the holding capacitor. Although the R_{ON} on the switches is low enough to allow fast setting, as the sampling frequency increases, the rate of charge transfer increases and the average voltage measured with a DVM across it will increase proportionally; this causes the CMRR of the sampled data system, as seen by a 'continuous' instrument (DVM), to decrease, Figure 15.

Figure 14 **Differential to single-ended converter**



C_S, C_H ARE MYLAR OR POLYSTYRENE

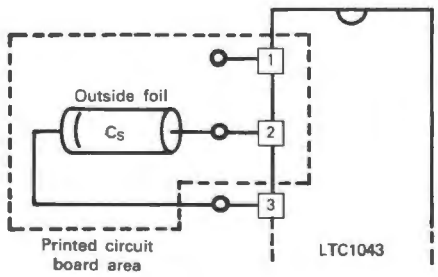
Figure 15 **CMMR vs. sampling frequency**



Shielding the sampling capacitor for very high CMRR

Internal or external parasitic capacitors from the C^+ pin(s) to ground affect the CMRR of the LTC1043, (Figure 14). The common-mode error due to the internal junction capacities of the C^+ pin(s) 2 and 11 is cancelled through internal circuitry. The C^+ pin, therefore, should be used as the top plate of the sampling capacitor. The interpin capacitance between pin 2 and dummy pin 1 (11 and 10) appears in parallel with the sampling capacitor so it does not degrade the CMRR. A shield placed underneath the sampling capacitor (Figure 16) and connected to either pin 1 or 3 helps to boost the CMRR in excess of 120dB.

Figure 16 **Printed circuit board layout showing shielding and sampling capacitor**



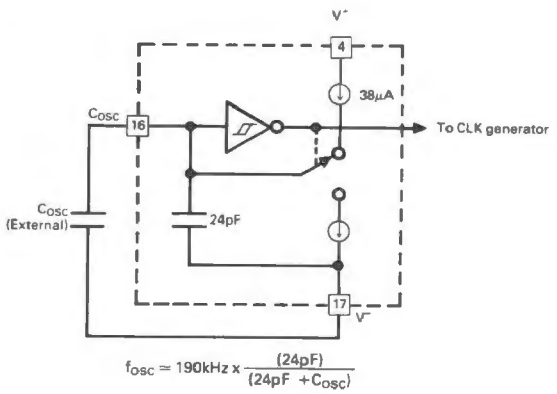
Excessive external parasitic capacitance between the C^- pins and ground indirectly degrades CMRR; this becomes visible especially when the LTC 1043 is used with clock frequencies above 2kHz. Because of this, if a shield is used, the parasistic capacitance between the shield and circuit ground should be minimised.

It is recommended that the outer plate of the sampling capacitor be connected to the C^- pin(s).

Input pins, SCR sensitivity

An internal 60Ω resistor is connected in series with the input of the switches (pins 5, 6, 7, 8, 13, 14, 15, 18) and it is included in the R_{ON} specification. When the input voltage exceeds the power supply by a diode drop, current will flow into the input pin(s). The LTC1043 will not latch until the input current reaches 2mA-3mA. The device will recover from the latch mode when the input drops 3V-4V below the voltage value which caused the latch. For instance, if an external resistor of 200Ω is connected in series with an input pin, the input can be taken 1.3V above the supply without latching the IC. The same applies for the C^+ and C^- pins.

Figure 17 **Internal oscillator**



C_{OSC} pin (16), Figure 17

The C_{OSC} pin can be used with an external capacitor, C_{OSC}, connected from pin 16 to pin 17, to modify the internal oscillator frequency. If pin 16 is floating, the internal 24pF capacitor plus any external interpin capacitance set the oscillator frequency around 190kHz with ±5V supply. The typical performance characteristics curves provide the necessary information to set the oscillator frequency for various power supply ranges. Pin 16 can also be driven with an external clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of pin 16, they will in reality drive the C_{OSC} pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1043 C_{OSC} pins. The typical trip levels of the Schmitt trigger, Figure 17, are given below.

Supply	Trip levels
$V^+ = 5V, V^- = 0V$	$V_H = 3.4V$ $V_L = 1.35V$
$V^+ = 10V, V^- = 0V$	$V_H = 6.5V$ $V_L = 2.8V$
$V^+ = 15V, V^- = 0V$	$V_H = 9.5V$ $V_L = 4.1V$

Typical applications

Figure 18 **Divide by 2**

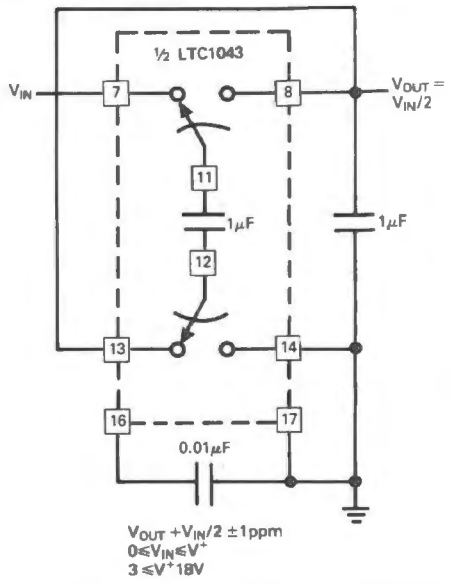


Figure 19 **Multiply by 2**

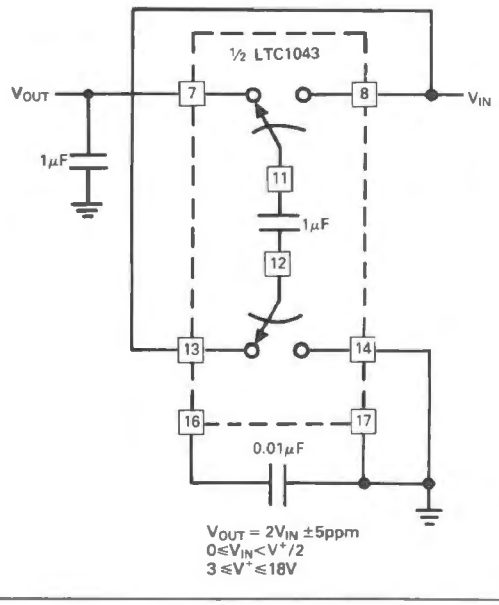


Figure 20 **Ultra precision voltage inverter**

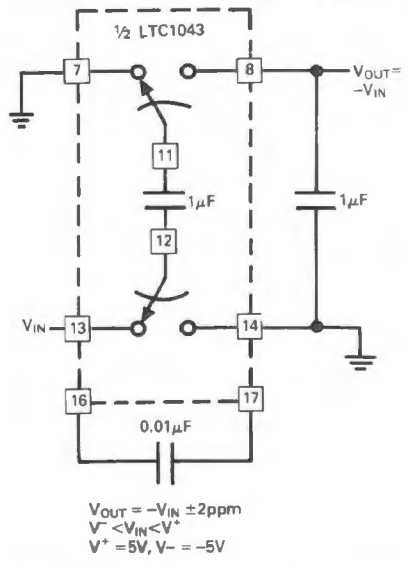
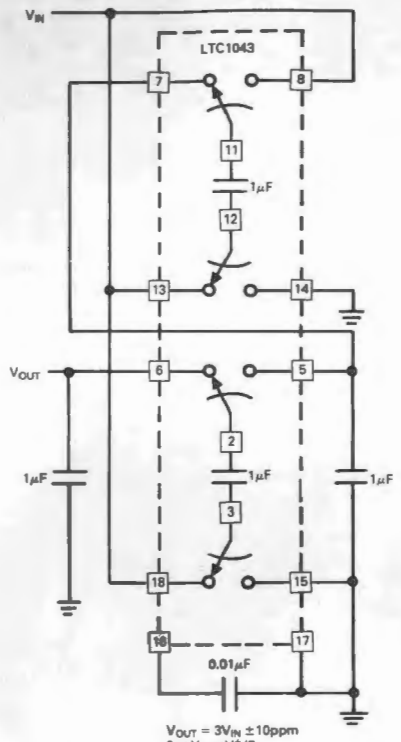
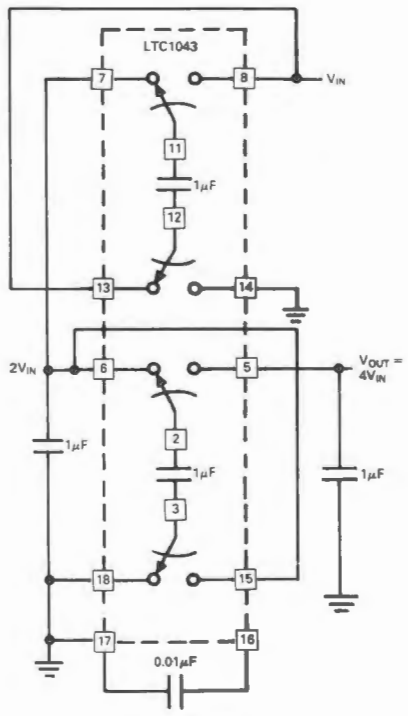


Figure 21 **Precision multiply by 3**



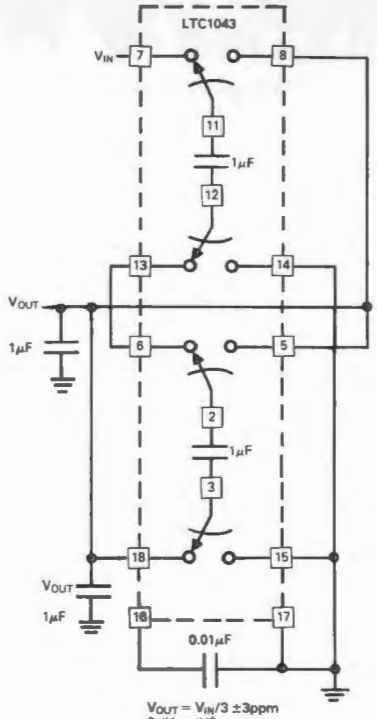
$V_{OUT} = 3V_{IN} \pm 10ppm$
$0 < V_{IN} < V^+/3$
$3V < V^+ < 18V$

Figure 22 **Precision multiply by 4**



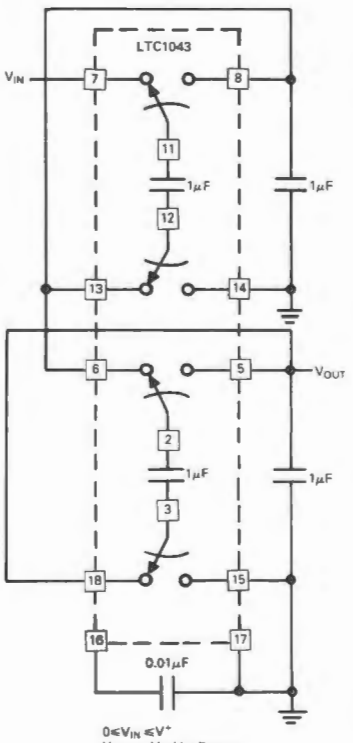
$V_{OUT} = 4V_{IN} \pm 40ppm$
$0 < V_{IN} < V^+/4$
$3V < V^+ < 18V$

Figure 23 **Divide by 3**



$V_{OUT} = V_{IN}/3 \pm 3ppm$
$0 \leq V_{IN} \leq V^+$

Figure 24 **Divide by 4**



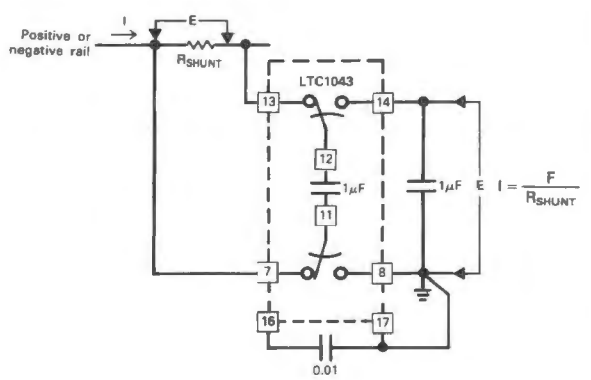
$0 \leq V_{IN} \leq V^+$
$V_{OUT} = V_{IN}/4 \pm 5ppm$

RS data

Current sensing in supply rails

The LTC1043 can sense current through a shunt in either of its supply rails (Figure 25). This capability has wide application in battery and solar-powered systems. If the ground-referred voltage output is unloaded by an amplifier, the shunt can operate with very little voltage drop across it, minimising losses.

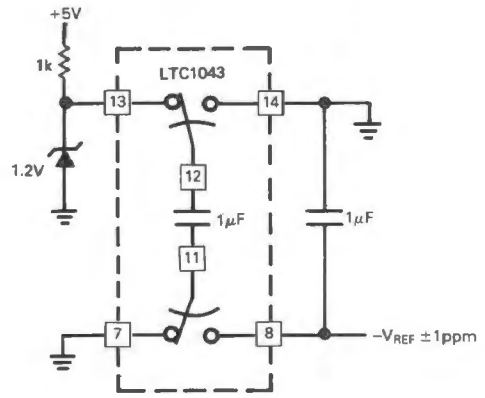
Figure 25 **Current sensing in supply rails**



Inverting reference

Figure 26 allows a reference to be inverted with 1ppm accuracy. The circuit features high input impedance and requires no trimming.

Figure 26 **Precision voltage inverter**



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RS data

5th order low pass filter LTC1062

Stock number 633-880

The LTC1062 is a 5th order all pole maximally flat lowpass filter, with no dc error, that is manufactured using the silicon gate LTCMOS™ process. This device features an unusual architecture that puts the filter outside the dc path, so offset and low frequency noise problems are eliminated making it useful for LPFs where dc accuracy is important.

The filter input and output are simultaneously taken across an external resistor with the LTC1062 coupled to the signal through an external capacitor. This RC network reacts with the internal switched capacitor network to form a 5th order rolloff at the output.

The filter cutoff frequency is set by an internal clock which can be externally driven. The clock to cutoff frequency ratio is typically 100:1, allowing the clock ripple to be easily removed.

Two LTC1062s can be cascaded to form a 10th order quasi max. flat lowpass filter. The device can be operated with single or dual supplies ranging from ± 2.5V to ± 9V.

8-pin dil plastic package. Equivalent to LTC1062CN8.

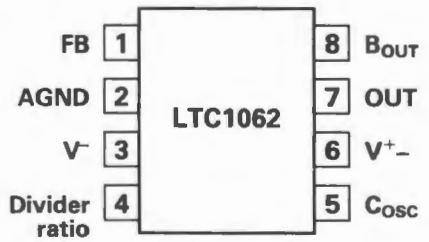
Absolute maximum ratings

Total supply voltage (V^+ to V^-) ——— 18V
Input voltage at any pin — V^- −0.3V ≤ V_{IN} ≤ V^+ +0.3V
Operating temperature range — −55°C ≤ T_A ≤ 125°C
Storage temperature range ——— −65°C to 150°C
Lead temperature range (soldering, 10 sec.) — 300°C

Features

- Low pass filter with no dc error
- Low passband noise
- Operates dc to 20kHz
- Operates on a single 5V supply or up to ±8V
- 5th order filter
- Maximally flat response
- Internal or external clock
- Cascadable for faster rolloff
- Buffer available
- 8 pin DIP package.

Pin connections



ATTENTION

OBSERVE PRECAUTIONS FOR HANDLING

ELECTROSTATIC SENSITIVE DEVICES

LTCMOS™ is a trademark of Linear Technology Corporation

Electrical characteristics (Test conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$ unless otherwise specified)

Parameter	Conditions		Min.	Typ.	Max.	Units
Power supply current	C_{OSC} (pin 5 to V^-) = 100pF	 ●		4.5	7 10	mA mA
Input frequency range				0-20k		Hz
Filter gain at $f_{IN} = 0$ $f_{IN} = 0.5f_C$ (Note 1) $f_{IN} = f_C$ $f_{IN} = 2f_C$ $f_{IN} = 4f_C$	f_{CLK} = 100kHz, Pin 4 at V^+ C = 0.01μF, R = 25.78k	 ● ● ●	 –2 –28 –54	0 –0.02 –3 –30 –60	 –0.3	dB dB dB dB dB
Clock to cutoff frequency ratio, f_{CLK}/f_C	Same as above			100±1		%
Filter gain at f_{IN} = 16kHz	f_{CLK} = 400kHz, Pin 4 at V^+ C = 0.01μF, R = 6.5k	●	–48	–52		dB
f_{CLK}/f_C temperature coefficient	Same as above			10		ppm/°C
Filter output (pin 7) dc swing	Pin 7 buffered with an external op amp	●	±3.5	±3.8		V
Clock feedthrough				10		mVp-p
Internal buffer						
Bias current				2	50	pA
Bias current		●		170	1000	pA
Offset voltage				2	20	mV
Voltage swing	R1 = 20kΩ	●	±3.5	±3.8		V
Short circuit current source/sink				40/3		mA
Clock (Note 2)						
Internal oscillator frequency	C_{OSC} (pin 5 to V^-) = 100pF C_{OSC} (pin 5 to V^-) = 100pF	 ●	25 15	32	50 65	kHz kHz
Max clock frequency				4		MHz
Pin 5 source or sink current		●		40	80	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1. f_C is the frequency where the gain is –3dB with respect to the input signal.

Note 2. The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. When pin 4 = V^+, ratio = 1; when pin 4 = GND, ratio = 2; when pin 4 = V^-, ratio = 4.

Characteristic curves

Figure 1 **Amplitude response normalized to cut-off frequency**

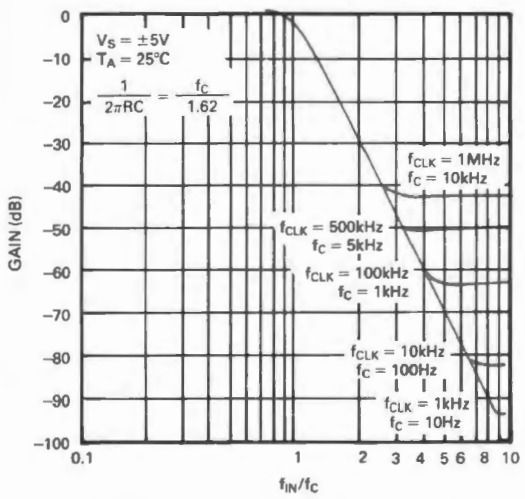


Figure 2 **Amplitude response normalized to cut-off frequency**

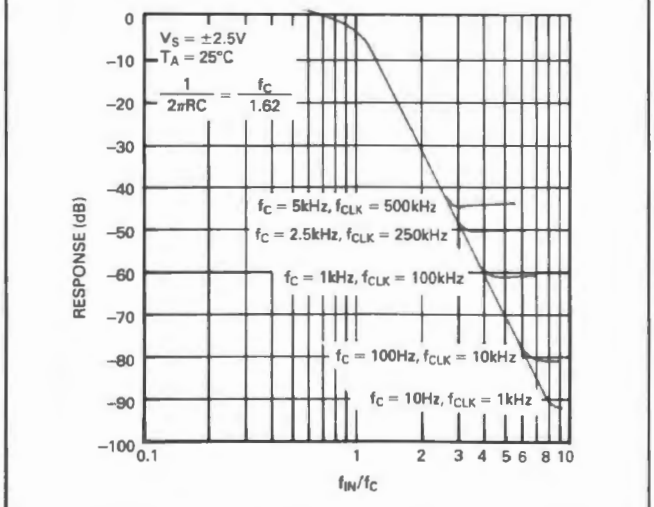


Figure 3 **Passband gain vs. input frequency**

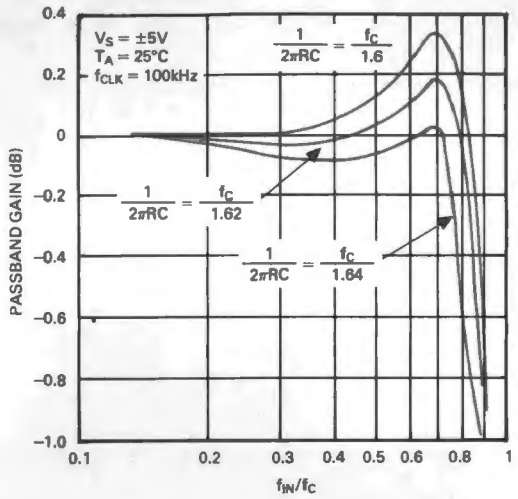


Figure 4 **Passband phase shift vs. input frequency**

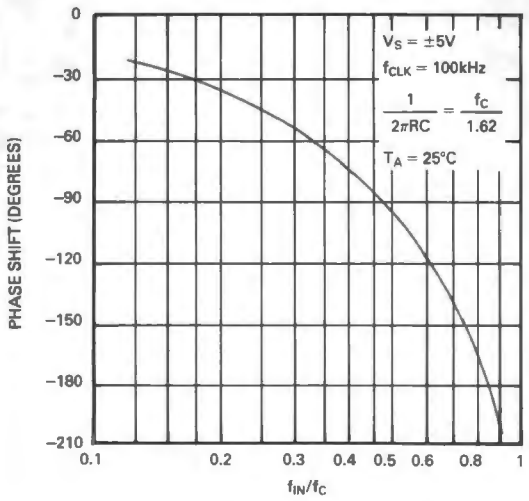


Figure 5 **Filter noise spectral density**

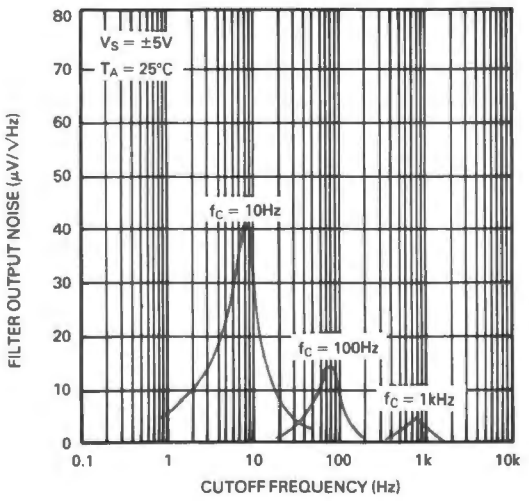


Figure 6 **Normalized oscillator frequency f_{osc} vs. supply voltage**

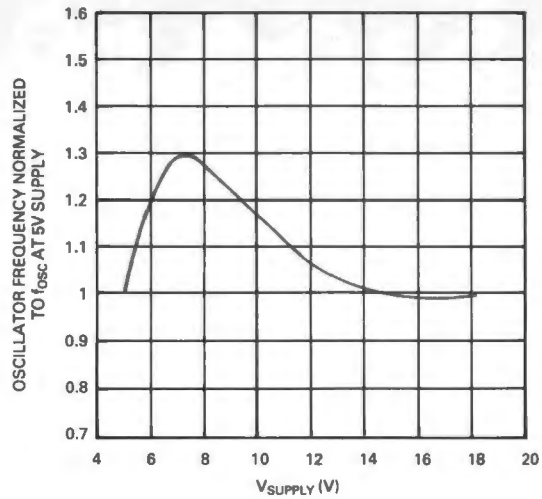


Figure 7 **Oscillator frequency f_{osc} vs. ambient temperature**

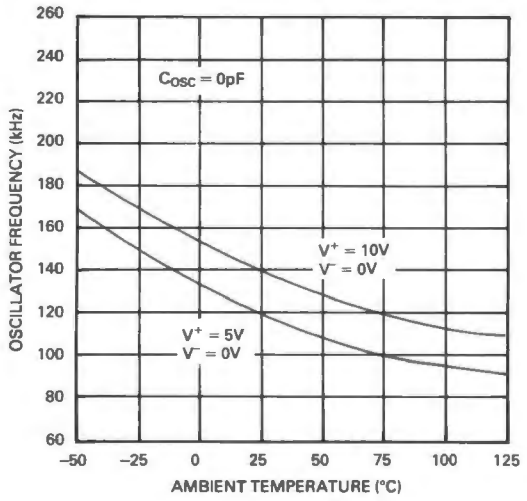
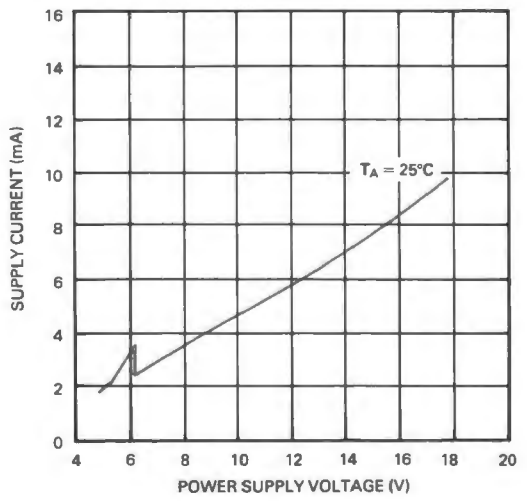
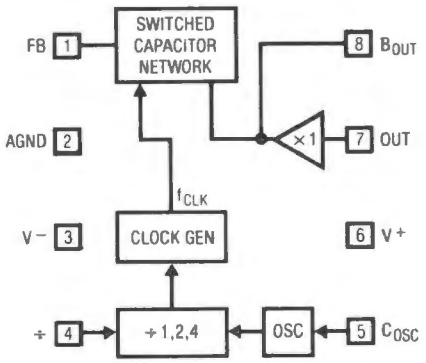


Figure 8 **Power supply current vs. power supply voltage**



Device description

Figure 9 **Block diagram**



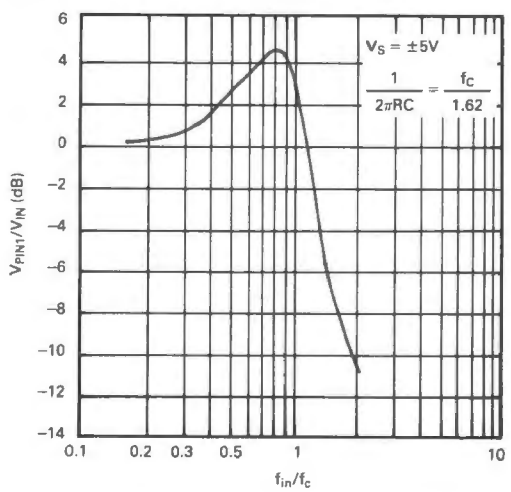
By connecting pin 4 to V^+, AGND, or V^-, the output frequency of the internal clock generator is the oscillator frequency divided by 1, 2, 4. The (f_{CLK}/f_C) ratio of 100:1 is with respect to the internal clock generator output frequency. Pin 5 can be driven with an external CMOS level clock. The LTC1062 can also be self-clocked by connecting an external capacitor (C_{OSC}) to ground (or to V^- if C_{OSC} is polarized). Under this condition and with ±5V supplies, the internal oscillator frequency is:

$$f_{OSC} \simeq 140kHz\,[33pF/(33pF + C_{OSC})].$$

Filter input voltage range

Every node of the LTC 1062 typically swings within 1V of either voltage supply, positive or negative. With the appropriate external (R,C) values, the amplitude response of all the internal or external nodes does not exceed a gain of 0dB with the exception of pin 1. The amplitude response of the feedback node (pin 1) is shown in Figure 10. For an input frequency around 0.8 x f_c, the gain is 1.7 V/V and, with ± 5V supplies, the peak-to-peak input voltage should not exceed 4.7V. If the input voltage goes beyond this value, clipping and distortion of the output waveform occur, but the filter will not get damaged nor will it oscillate. Also, the absolute maximum input voltage should not exceed the power supplies.

Figure 10 **Amplitude response of pin 1**



Internal buffer

The internal buffer out (pin 8) and pin 1 are part of the signal ac path. Excessive capacitive loading will cause gain errors in the passband, especially around the cutoff frequency. The internal buffer gain at dc is typically 0.006dB. The internal buffer output can be used as a filter output, however it has a few millivolts of dc offset. The temperature coefficient of the internal buffer is typically 1μV/°C.

Filter attenuation

The LTC1062 rolloff is typically 30dB/octave. When the clock, and the cutoff frequencies increase, the filter's maximum attenuation decreases. This is shown in the characteristic curves. The decrease of the maximum attenuation, is due to the roll off at higher frequencies of the loop gains of the various internal feedback paths and not to the increase of the noise floor. For instance, for a 100kHz clock and 1kHz cutoff frequency, the maximum attenuation is about 64dB. A 4kHz, 1Vrms input signal will be predictably attenuated by 60dB at the output. A 6kHz, 1Vrms input signal will be attenuated by 64dB and not by 77dB as an ideal 5th order maximum flat filter would have dictated. The LTC 1062 output at 6kHz will be about 630μVrms. The measured rms noise from dc to 17kHz was 100μVrms which is 16dB below the filter output.

C_{OSC}, pin 5

The C_{OSC}, pin 5, can be used with an external capacitor, C_{OSC}, connected from pin 5 to ground. If C_{OSC} is polarized it should be connected from pin 5 to the negative supply, pin 3. C_{OSC} lowers the internal oscillator frequency. If pin 5 is floating, an internal 33pF capacitor plus the external interpin capacitance set the oscillator frequency around 140kHz with ±5V supply. An external C_{OSC} will bring the oscillator frequency down by the ratio (33pF)/(33pF + C_{OSC}). The typical performance characteristics curves provide the necessary information to get the internal oscillator frequency for various power supply ranges. Pin 5 can also be driven with an external CMOS clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of pin 5, they will, in reality, drive the C_{OSC} pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1062 C_{OSC} pins. The typical trip levels of the internal Schmitt trigger which input is pin 5, are given below.

Power supply		Trip levels	
$V^+ = +5V$	$V^- = 0V$	$V_H = 3.4V$	$V_L = 1.35V$
$V^+ = +10V$	$V^- = 0V$	$V_H = 6.5V$	$V_L = 2.8V$
$V^+ = +15V$	$V^- = 0V$	$V_H = 9.5V$	$V_L = 4.1V$

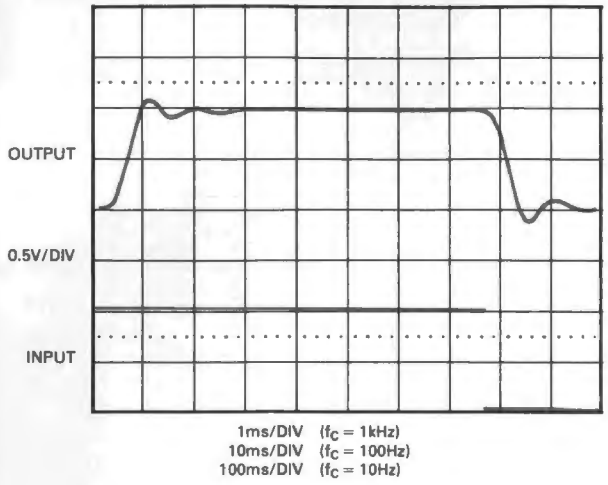
Divide by 1, 2, 4 (pin 4)

By connecting pin 4 to V^+, to mid supplies or to V^-, the clock frequency driving the internal switched capacitor network is the oscillator frequency divided by 1, 2, 4, respectively. Note that the f_{CLK}/f_C ratio of 100:1 is with respect to the internal clock generator output frequency. The internal divider is useful for applications where octave tuning is required. The ÷ 2 threshold is typically ± 1V from the mid supply voltage.

Transient response

Figure 11 shows the LTC1062 response to a 1V input step. The setting time approximates that of an ideal 5th order maximally flat filter.

Figure 11 **Transient response**



Filter noise

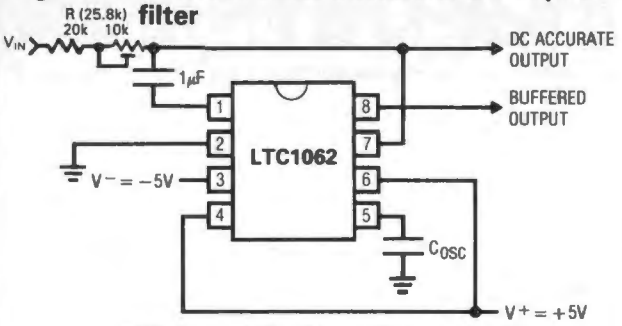
The filter wideband rms noise is typically 100μVrms for $\pm$5V supply and it is nearly independent from the value of the cutoff frequency. For single 5V supply the rms noise is 80μVrms. Sixty-two per cent of the wideband noise is in the passband, that is from dc to f_c. The noise spectral density, unlike conventional active filters, is nearly zero for frequencies below 0.1 x f_C. This is shown in the typical performance characteristics section. Table 1 shows the LTC 1062 rms noise for different noise bandwidths.

Table 1

Noise BW	rms Noise $V_S = \pm 5V$
dc – 0.1 x f_C	2μV
dc – 0.25 x f_C	8μV
dc – 0.5 x f_C	20μV
dc – 1 x f_C	62μV
dc – 2 x f_C	100μV

Typical applications

Figure 12 **10Hz 5th order Butterworth lowpass filter**



NOTE: TO ADJUST OSCILLATOR FREQUENCY, USE A 6800pF CAPACITOR IN SERIES WITH A 50k POT FROM PIN 5 TO GROUND.

Filter amplitude response and noise

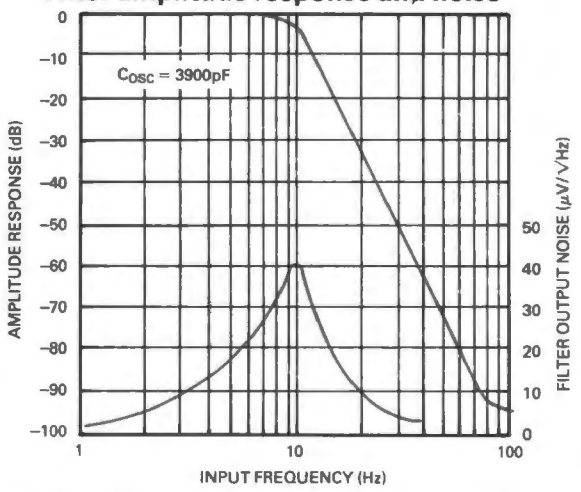
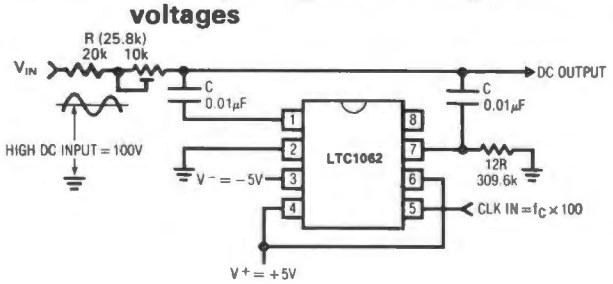
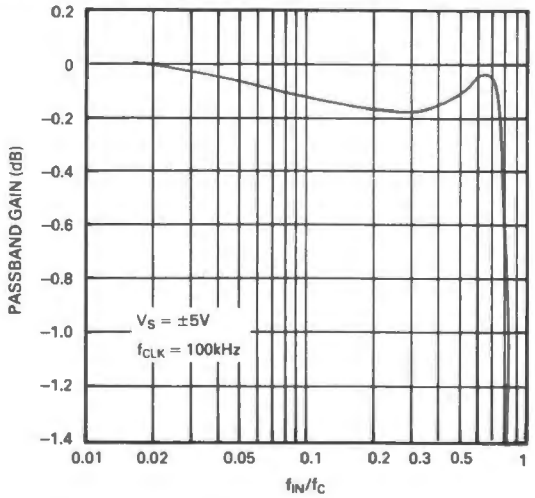


Figure 13 **Filtering ac signals from high dc voltages**



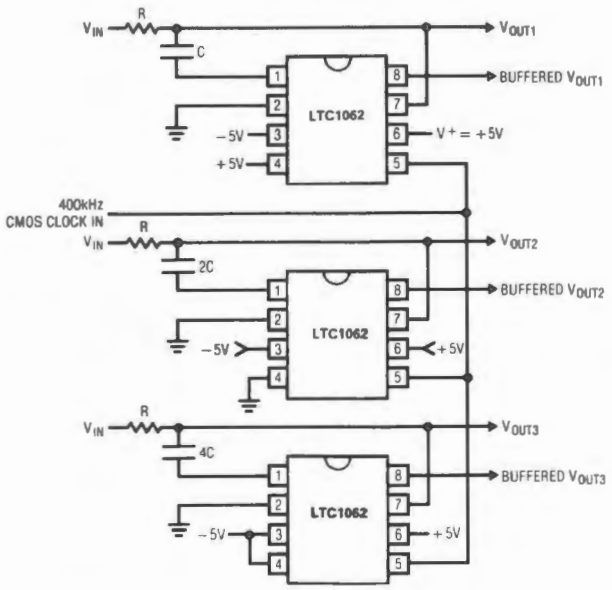
EX f_{CLK} = 100kHz, f_C = 1kHz. The filter accurately passes the high dc input and acts as 5th order LP filter for the ac signals riding on the dc. The amplitude response in the passband is shown below.

Passband amplitude response for the high dc accurate 5th order filter



RS data

Figure 14 **Octave tuning with a single input clock**



Amplitude response for the octave tuning circuit

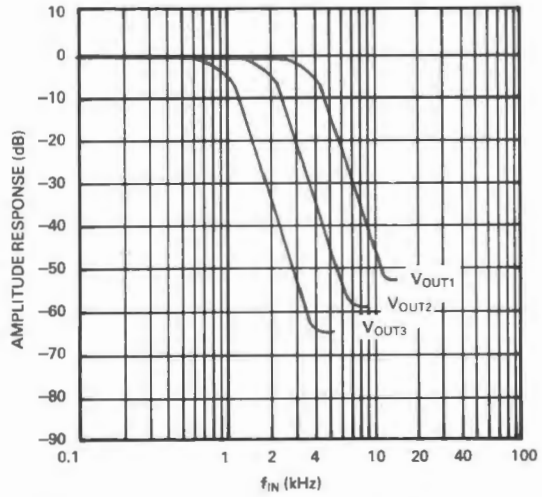
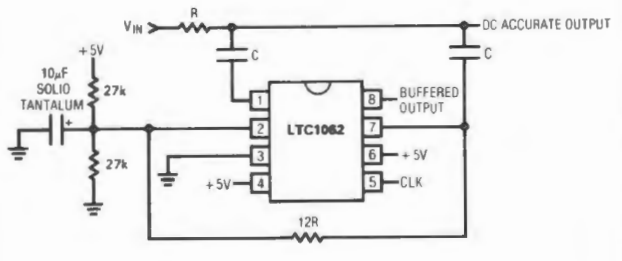


Figure 15 **Single 5V supply 5th order low pass filter**



FOR A 10Hz FILTER R = 29.4k, C = 1μF, f_{CLK} = 1kHz

THE FILTER IS MAXIMALLY FLAT FOR $\frac{1}{2\pi RC} = \frac{f_C}{1.84}$

Figure 16 **100Hz, 50Hz, 25Hz 5th order dc accurate low pass filter**

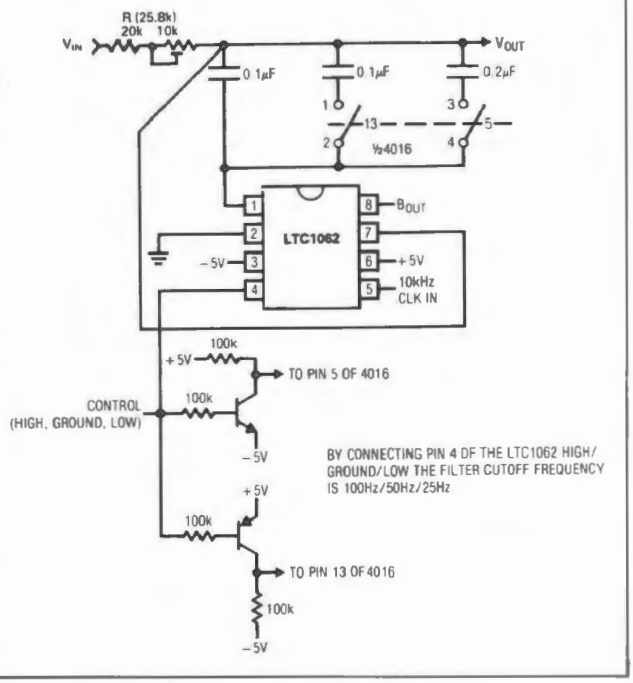
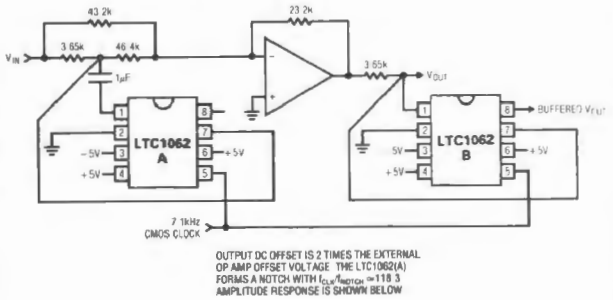
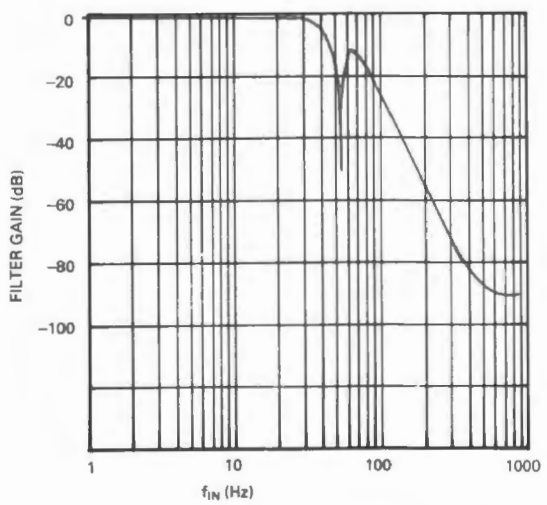


Figure 17 **5th order lowpass filter with 60Hz notch**





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RS Data Library

STE bus computer boards and accessories

Introduction

This data sheet describes how computer systems can be configured from the RS STE bus computer boards. It contains information on the boards and how they can be connected together, and to other devices, to form a selection of computer based systems for industrial control applications. Each board is described in detail in the instruction leaflet or manual supplied with the board.

The manuals are also available separately (stock numbers 632-039, 633-155, 633-587 and 633-117). It is recommended that instruction leaflets and manuals are read carefully before attempting to put a system together.

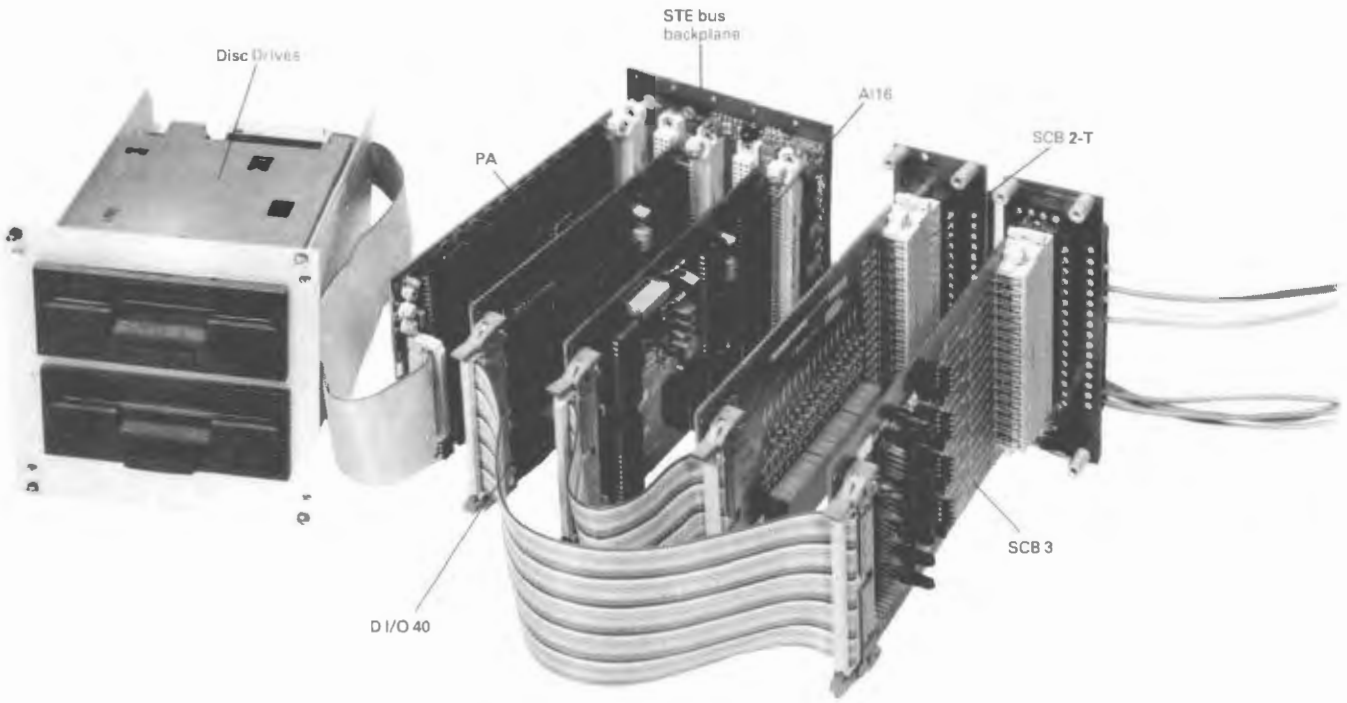
The system is based on the STE bus backplane bus. This is a new standard (IEEE number P1000). There are three types of boards. Processor boards are bus masters, peripheral (I/O) boards are bus slaves and signal conditioning boards modify signals to peripheral boards. Backplanes are used to connect bus masters and slaves.

The processor boards are based on the Z80 microprocessor, stand-alone BASIC, stand-alone 'C' and the Digital Research CP/M Plus disc operating systems are available.

Peripheral boards include analogue input, digital input and output, real-time clock with RAM (or EPROM), EPROM programmer and a watchdog controller.

Signal conditioning boards (SCBs) exist for modifying analogue and digital signals. Analogue signal conditioning boards are available for temperature transducers and 4-20mA current inputs. Digital SCBs can take opto isolators for inputs and drive Darlington outputs. In addition there is a prototyping signal conditioning board which can be wired to suit individual applications. The signal conditioning boards can connect to a cable terminator to accommodate heavy duty wiring.

Two backplanes are available, with 5 and 10 slots.



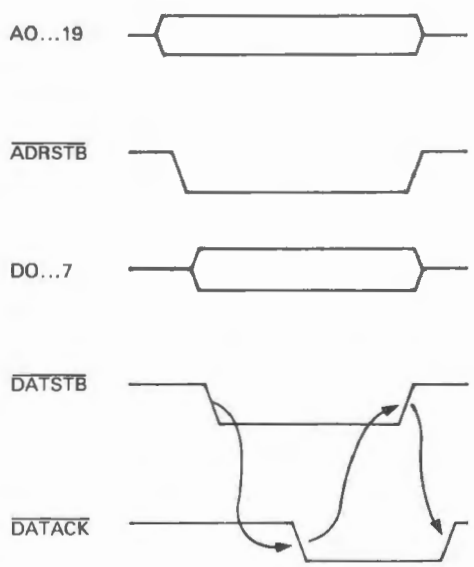
A system configuration suitable for data logging applications. The AI16 and SCB2-T would allow monitoring of up to 16 temperature inputs. The D I/O 40 will support up to 4 of the SCB3 optoisolator input boards daisy-chained from the front 50-way ribbon cable.

7512

Features

- Professional eurocard computer system for industrial control, instrumentation and data logging
- Industry-standard STE bus (IEEE P1000)
- Z80 based processor boards for disc drive based CP/M systems or stand-alone target systems
- Industry standard CP/M Plus operating system from Digital Research
- BASIC language, 'C' language and Z80 assembler
- EPROM programming commands included with both BASIC and CP/M Plus
- Range of peripheral boards for I/O (input/output), memory expansion and EPROM programming
- System designer's sets of manuals available separately

Figure 1 **Data transfer**



The manuals for the processor boards contain more information on bus signals and pinouts.

This data sheet covers the following stock numbers (in stock number order).

Stock No.	Description
631-862	Processor A, Z80, 64KB DRAM, floppy disc controller, two RS232 ports and boot EPROM for CP/M Plus.
631-878	Processor B, Z80, 4KB RAM (expandable to 16KB), two EPROM sockets, two RS232 ports and a counter/timer.
631-884	CP/M Plus from Digital Research for Processor A, on both 3½in and 5¼in floppy discs.
631-890	BASIC on both 3½in and 5¼in discs runs under CP/M Plus for Processor A or B, and in EPROM for Processor B.
631-907	Monitor and EPROM programming software for Processor B.
631-913	EPROM programmer board.
631-929	Real time clock with back up battery and sockets for 6 CMOS RAMS. (Up to 48 KB.)
631-935	40 line digital I/O board.
631-941	16 analogue input board, 12 bit resolution.
631-957	SCB1 prototyping signal conditioning board.
631-963	SCB2-T 16 channel temperature transducer input signal conditioning board.
631-979	SCB2-C 16 channel 4-20mA input signal conditioning board.
631-985	SCB3 8 channel digital input signal conditioning board with sockets for opto isolators.
631-991	SCB4 32 channel Darlington driver output signal conditioning board.
632-001	SCT1 cable terminator for signal conditioning boards.
632-017	SBPL5 5 slot terminated backplane.
632-023	SBPL10 10 slot terminated backplane.
632-039	Set of nine extra manuals supplied with the stock numbers from 631-862 to 631-941.
632-067	Digital Research CP/M Plus manuals.
633-111	Floppy disc controller board for up to four disc drives.
633-127	CP/M Plus from Digital Research for Processor B and floppy disc controller board.
633-133	Serial communications board with four channels.
633-149	System watchdog and controller board for system monitoring, protection and control.
633-155	Set of four extra manuals supplied with 633-111 to 633-149.
633-420	M80 software utility from Microsoft runs under CP/M Plus for Processor A or B.
633-543	64KB dynamic RAM board (expandable to 512KB).
633-559	SCB7 4 channel type K thermocouple input signal conditioning board.
633-565	SCT2 cable terminator for SCB7 signal conditioning board.
633-571	SCB 9 16 channel digital input signal conditioning board fully populated with ILD 74 opto isolators. Input voltage range between 3V and 50V ac or dc is selected by inserting a series resistor.
633-587	Set of two extra manuals supplied with 633-543 and 633-688.
633-688	C-language compiler with Mathpak on both 3½in and 5¼in floppy discs each containing the software, to run under CP/M Plus.
634-782	IEEE 488 to STE bus interface board. Meets all requirements for controller, talker and listener.
634-811	Basic compiler software with multi-tasking capability.
634-849	An I/O 8/2 8-bit analogue input and output board with 8 inputs and 2 outputs.
634-855	STMC stepper motor control board compatible with RS stepper motors.
635-101	IOP input/output prototyping board with STE bus interface.
635-117	Set of five extra manuals as supplied with 634-782, 634-811, 634-849, 634-855 and 635-101.

The STE bus

The STE bus is a new high performance 8-bit bus standardised by the IEEE (IEEE number P1000). It has a 1MB memory address range and a 4KB I/O address range. Two features in particular set it apart from other 8 bit busses. The first is that it is multimaster. This means that more than one bus master (processor) can be connected to the bus. Decisions about which processor actually drives the bus are made by a bus arbiter. An example is a PA (master processor) running a disc operating system such as CP/M Plus on the same bus as a PB (slave processor) doing real-time process control. The second feature is that the bus is asynchronous and it is not necessary to specify processor and I/O board 'speed', because all bus masters are compatible with all bus slaves. This works because the bus uses a handshake. When a bus master wants to write data, or is ready to read data, it sets up bus addresses and asserts address strobe (ADRSTB) to show that they are valid. It asserts data strobe (DATSTB) to show the data is valid and then waits for the slave to acknowledge with a DATACK. It then releases ADRSTB and DATASTB. Figure 1 shows this.

The STE bus is designed to be used in such areas as data acquisition, control and information processing.

For data acquisition, an example would be a disc drive based system with a processor board, the CPM Plus operating system and a BASIC program reading various inputs and recording the information on a floppy disc. The BASIC compiler (634-811) contains commands such as INP (address) which will return the byte at the I/O address indicated. This address range is between 0 and 4095 corresponding to the STE bus 4k I/O address space. The appropriate RS peripheral boards can be configured to reside at specific I/O locations and SCB boards may be used to connect the system to the required real-world signals. Commands in the BASIC compiler such as OPEN IN ('filename') and INPUT# can be used to store the values to the disc file. The subsequent output of that data is achieved by OPEN OUT ('filename') and PRINT# command. This flexibility allows very sophisticated customised data acquisition systems.

For control applications programs can be developed either on disc using any of the wide range of languages such as BASIC, 'C' or Z80 assembler, or on a stand-alone PB board based system using the BASIC compiler. Combined data acquisition and control systems can be built and a wide range of peripheral and signal conditioning boards are available. For the more sophisticated systems.

Multi-processors on the STE bus allow the division of tasks between separate processor boards allowing fast, efficient processing and enabling the speed required for some real-time control tasks.

Processor boards

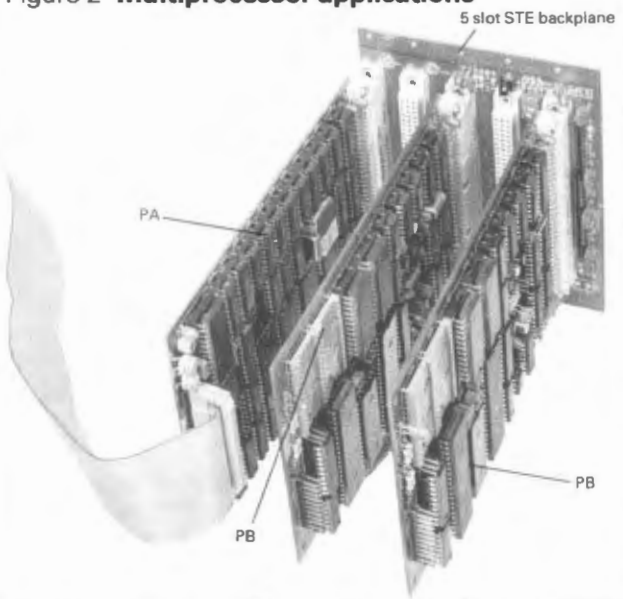
Processor A (631-862)

Processor A (PA) is a complete computer on a single eurocard. It contains a 4MHz Z80 microprocessor, 64KB of dynamic RAM, a boot EPROM for CP/M Plus, two serial RS232 channels, an optional parallel keyboard port, a floppy disc controller for 3½in or 5¼in drives and an STE bus interface. The PA is designed to run the CP/M Plus disc operating system from Digital Research. To do this it simply needs one or two disc drives, a power supply and an RS232 video display terminal (VDT). The PA can also drive the STE bus and has a bus arbiter, so it acts as the default master on the bus.

Processor B (631-878)

Processor B (PB) is designed for stand-alone target system applications. It has a 4MHz Z80 microprocessor and four memory sockets, capable of carrying up to 32KB of EPROM and 16KB of RAM. Two serial RS232 channels are provided and a counter/timer circuit (CTC) supplies baud rates, timers and clock functions. The PB can drive the STE bus as a single master and can also request the bus from a PA board. A PA and up to two PBs can share the bus. It can access disc drives via an STE bus backplane and the FDC board.

Figure 2 **Multiprocessor applications**



One PA and up to two PBs may be used in the same system for multiprocessor applications.

Peripheral boards

a) **Input/Output boards**

The **IOP** input/output prototyping board (635-101) has an STE bus interface and a matrix of plated through holes (measuring 95mm x 90mm) on a 0.1in pitch allowing custom I/O boards to be configured.

The **D I/O 40** (631-935) has 40 digital I/O lines, 32 of these are buffered with 24mA TTL drivers. Directions and enable signals for the drivers are controlled by software in groups of 8.

The **A I/O 8/2** 8-bit analogue input/output board (634-849) has 8 differential input channels and 2 output channels.

The **AI16** analogue board (631-941) has sixteen differential input channels with 12 bit resolution. It uses an integrating A to D converter for high stability and low noise. Conversion time is 30ms per channel.

b) **Memory boards**

The **C-RAM** clock board (631-929) with back-up battery has a real time calendar clock and sockets for six CMOS RAMs or EPROMs of 2 or 8KB each.

The **DRAM** dynamic memory board (633-543) has 16 sockets which may be populated to provide 64Kbytes, 128Kbytes, 256Kbytes or 512Kbytes of memory. It is supplied fitted with 64Kbytes of memory.

c) **Specialised system boards**

The **SERCOM 4** serial communications board (633-133) has four channels that can simultaneously transmit and receive at up to 115K baud asynchronously.

The **SWC** watchdog and controller board (633-149) is a multifunction peripheral board with a power line monitor, watchdog timer, reset circuit, system clock, parallel (centronics) port, LCD driver and an interface for the signal conditioning boards.

The **FDC** floppy disc controller board (633-111) is based around the Western Digital 279X floppy disc controller i.c. and can control up to four disc drives.

The **IEEE 488** interface board (634-782) allows the STE bus to be connected directly to an IEEE 488 bus system. It allows the STE bus processor to meet all of the requirements for controller, talker and listener.

The **STMC** stepper motor control board features an on-board 4-phase driver with heatsink for motors of up to 2 amps per phase. For larger motors the drive signals may be taken to the SCB 1 and a custom interface built. The stepper motor control ic controls motor excitation independently of the main processor, accepting commands as they are issued.

The **EP** (631-913) EPROM programmer can be program EPROMs of 2716, 2732, 2764, 27128 amd 27256 types. It has an on-board switch mode power supply driven by a D to A to generate any programming voltage up to 25.5V and can use the fast programming algorithm.

Signal conditioning boards

Signal conditioning boards (SCBs) are designed to convert external equipment signals into voltages or logic levels which the peripheral boards can read, and to provide a simple and robust method of making connections to plant, machinery and sensors. The system has been designed such that all digital boards (peripheral and SCB) have a defined pin out for a 50 way ribbon cable at the front of the board. Analogue boards have a similar pin out and connector. These pin-outs are shown in Figure 3.

Connections are made using 50 way ribbon cable between a peripheral board and the SCBs. To take signals from external equipment, the SCB has a heavy duty (6A per contact) DIN 41612 'F' type connector on the other end. This can plug into an SCT1 cable terminator mounted on the back of the rack, and the SCT1 has screw terminal connections for heavy duty cables. This is illustrated in Figure 4.

Figure 3 **50 way pcb mounted connector pin-out**

(peripheral board/SCB board end view)

DIGITAL

+5V	50	49	+5V
+12V	48	47	−12V
D	46	45	D
D	44	43	D
S	42	41	GND
D7	40	39	D6
D5	38	37	D4
D3	36	35	D2
D1	34	33	D0
S	32	31	GND
D7	30	29	D6
D5	28	27	D4
D3	26	25	D2
D1	24	23	D0
S	22	21	GND
D7	20	19	D6
D5	18	17	D4
D3	16	15	D2
D1	14	13	D0
S	12	11	GND
D7	10	9	D6
D5	8	7	D4
D3	6	5	D2
D1	4	3	D0
GND	2	1	GND

D = Digital I/O
S = 'Special' Digital I/O

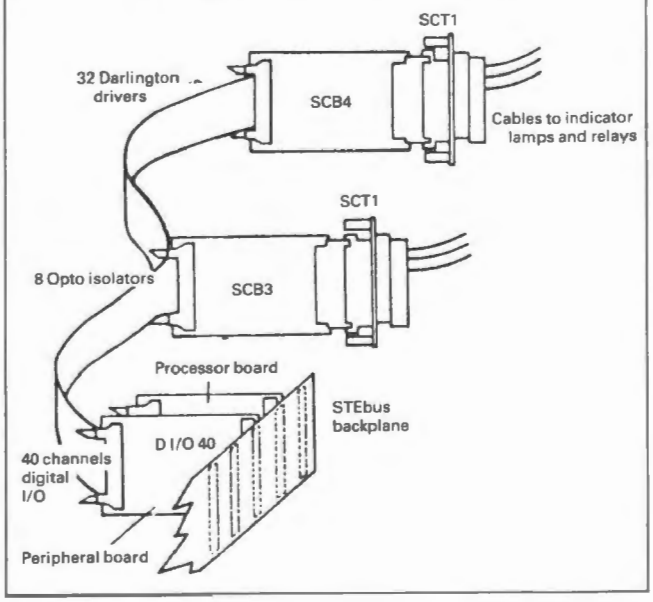
ANALOGUE

+5V	50	49	+5V
+12V	48	47	−12V
DA3	46	45	DA2
DA1	44	43	DA0
X	42	41	GND
CH15—	40	39	CH15+
14—	38	37	14+
13—	36	35	13+
12—	34	33	12+
X	32	31	GND
11—	30	29	11+
10—	28	27	10+
9—	26	25	9+
8—	24	23	8+
X	22	21	GND
7—	20	19	7+
6—	18	17	6+
5—	16	15	5+
4—	14	13	4+
X	12	11	GND
3—	10	9	3+
2—	8	7	2+
1—	6	5	1+
0—	4	3	0+
GND	2	1	GND

DA = D/A out
CH− = inverting input
CH+ = non-inverting input
X = function not assigned

Note: There are two pin-out conventions for STE peripheral board and SCB compatibility (one for digital and one for analogue boards). Pin 1 is marked by an ▲ on the connector.

Figure 4 **A typical system configuration**



For the SCB 7 the specialised thermocouple cable is connected via the screw terminal on a SCT2 cable terminator.

a) **Digital SCBs**

The **SCB 3** (631-985) is supplied socketed and ready to fit up to the 8 ac or dc opto-isolators which may be selected to suit the applications.

The **SCB 4** (631-991) has 32 darlington driver outputs capable of sinking 0.5 amp at up to 50V on any output.

The **SCB 9** (633-571) is supplied fitted with sixteen ILD 74 opto-isolators allowing opto-isolation up to 50Vac or dc, by inserting an appropriate series resistor.

b) **Analogue SCBs**

The **SCB 2-T** (631-963) is a temperature transducer input signal conditioning board. It allows direct connection of up to 16 RS temperature sensors (308-809).

The **SCB 2-C** (631-979) is designed to allow direct connection of up to sixteen standard 4-20mA input signals, eg as provided by the RS current transducer (257-420).

The **SCB 7** (633-559) is a four channel thermocouple input signal conditioning board. It allows screw connection via the SCT 2 cable terminator to any type K thermocouple, eg stock number 158-913.

c) **General purpose SCBs**

The **SCB 1** (631-957) has been designed for specialist applications where interfaces need to be prototyped. It features an 85mm x 105mm matrix of plated through holes on a 0.1 in pitch.

Software

CP/M Plus is available in two configurations, one for the PA (631-884) and one for the PB and FDC (633-127). Note that this latter version also requires a memory board of at least 48K bytes to be present on the bus. A fully populated C-RAM with six 8K x 8 devices is suitable. Two 8K x 8 devices on the PB board make up the balance of 64K bytes of RAM required for CP/M Plus in configuration B. CP/M Plus is the latest 8 bit version of CP/M from Digital Research (version 3.0) and is compatible with CP/M 2.2 and earlier versions. EPROM programming software for use with the EP EPROM programmer board is included.

```
dir
A: CPM3     SYS : BDOS3    SPR : BNKBDOS3 SPR : RESBDOS3 SPR : SCB      ASM
A: TIME     ASM : BOOTB    REL : BOOTN    REL : BOOT     ASM : CHARIO   REL
A: BIOSKRNL ASM : CPMLDR   REL : CHARIO   ASM : FLOPPY   REL : GENCPM   DAT
A: MEMORY   REL : FDPH     ASM : SCB      REL : TIMES    ASM : BIOS3    SPR
A: BNKBIOS3 SPR : DRVTBL   ASM
SYSTEM FILE(S) EXIST
A>dirs
A: CCP      COM : COPY     COM : LIB      COM : DATE     COM : DEVICE   COM
A: DIR      COM : DUMP     COM : ED       COM : ERASE    COM : GENCOM   COM
A: GET      COM : HEXCOM   COM : INITDIR  COM : LINK     COM : MAC      COM
A: RMAC     COM : PATCH    COM : PIP      COM : PUT      COM : RENAME   COM
A: SID      COM : SAVE     COM : SET      COM : SETDEF   COM : SHOW     COM
A: ZSID     COM : SUBMIT   COM : SYSCOPY  COM : CPM3     LIB : DIRLBL   RSX
A: GENCPM   COM : HELP     COM : EPROM    COM : HIST     UTL : MODEBAUD LIB
A: CPMLDR   COM : TRACE    UTL : TYPE     COM : XREF     COM : Z80      LIB
A: DISCCOPY COM : DISCFORM COM : HELP     HLP
NON-SYSTEM FILE(S) EXIST
A>
```

BASIC (631-890) is supplied on two discs each containing the program, one 3½in and one 5¼in to run on the PA or PB under CP/M Plus and in an EPROM for use on the PB board. Both the PA and PB versions of BASIC can produce programs in EPROM which will run in stand-alone mode on the PB board. A PB board and an EP EPROM programmer board can be used with a VDT to develop, save and load EPROMs containing BASIC programs for use on the PB.

The **C-compiler** (633-688) package runs under CP/M Plus and is supplied on two discs, 3½in and 5¼in each containing the software. The package includes the Software Toolworks C/80 compiler, Mathpak and a library of routines to allow the compiled code to run stand-alone in EPROM in a target Processor B system.

```
  dir
A: HELLO    C   : CLIBRARY ASM : CLIBRARY REL : PRINTF   C   : TAB      C
A: TPRINTF  C   : CTRACE   C   : SEEK     C   : SCANF    C   : COMMAND  C
A: CLIBIO   C   : EXEC     C   : CMP      C   : TREE     C   : CPROF    C
A: MATHLIB  C   : FLIBRARY REL : MATHLIB  REL : FLOATLIB ASM : LGFLTLIB ASM
A: LONGLIB  ASM : FPRINTF  C
SYSTEM FILE(S) EXIST
A>dirs
A: C        COM : AS       COM : CCONFIG  COM : PRINTF   H   : SCANF    H
A: STDLIB   C   : STDLIB   REL : CCONFIGF COM : FPRINTF  H
NON-SYSTEM FILE(S) EXIST
A>
1A>dirs
A: PB       MAC : PB       REL : SACLIB   REL : START    REL : SACFLT   REL
A: TRIM     COM : STDIO    H
1A>
```

The **PB monitor** (631-907) is a machine code monitor for use on the PB board. It has examine and modify commands for the registers and memory, single stepping, breakpoints and EPROM programming routines.

M80 (633-420) is Microsoft's complete Z80 assembly language development package to run under CP/M Plus. It consists of an assembler, linking loader, cross reference facility and library manager.

```
  dir
A: M80      COM : L80      COM : CREF80   COM : LIB80    COM :
A>
```

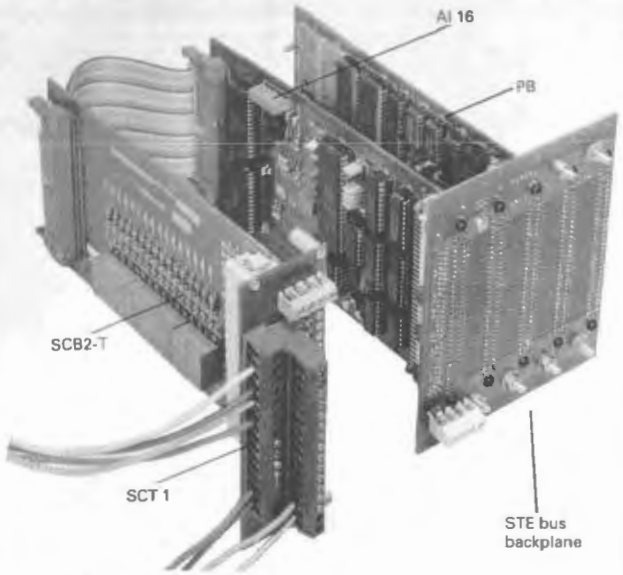
Building a system

System concepts

Consider a typical configuration in an industrial plant as detailed in Figure 5. The SCT1 (signal cable terminators) allow simple and robust wiring to the plant. Plant signals are converted by the SCBs (signal conditioning boards) to levels compatible with the peripheral and processor boards. The digital signal conditioning boards have a defined pin-out compatible with the digital peripheral boards. Similarly all analogue signal conditioning boards have a defined pin-out compatible with the analogue peripheral boards. These pin-outs appear on the 50 way connectors at the front of the boards and are detailed in Figure 3.

Communication between the peripheral boards and the processor boards is via the STE bus backplane (see Figure 6).

Figure 5 **A typical industrial configuration**



The SCT1 allows easy cable termination to the computer system.

In addition to the I/O peripheral boards, other peripheral boards are available for extra memory, a real time clock and EPROM programming.

Figure 6 **STE bus connector pin-out**

Pin		Row A	Row C		Pin
1	gnd	+	+	gnd	1
2	+5V	+	+	+5V	2
3	D0	+	+	D1	3
4	D2	+	+	D3	4
5	D4	+	+	D5	5
6	D6	+	+	D7	6
7	A0	+	+	gnd	7
8	A2	+	+	A1	8
9	A4	+	+	A3	9
10	A6	+	+	A5	10
11	A8	+	+	A7	11
12	A10	+	+	A9	12
13	A12	+	+	A11	13
14	A14	+	+	A13	14
15	A16	+	+	A15	15
16	A18	+	+	A17	16
17	CM0	+	+	A19	17
18	CM2	+	+	CM1	18
19	$\overline{\text{ADRSTB}}$	+	+	gnd	19
20	$\overline{\text{DATACK}}$	+	+	$\overline{\text{DATSTB}}$	20
21	$\overline{\text{TRFERR}}$	+	+	gnd	21
22	$\overline{\text{ATNRQ0}}$	+	+	$\overline{\text{SYSRST}}$	22
23	$\overline{\text{ATNRQ2}}$	+	+	$\overline{\text{ATNRQ1}}$	23
24	$\overline{\text{ATNRQ4}}$	+	+	$\overline{\text{ATNRQ3}}$	24
25	$\overline{\text{ATNRQ6}}$	+	+	$\overline{\text{ATNRQ5}}$	25
26	gnd	+	+	$\overline{\text{ATNRQ7}}$	26
27	$\overline{\text{BUSRQ0}}$	+	+	$\overline{\text{BUSRQ1}}$	27
28	$\overline{\text{BUSAK0}}$	+	+	$\overline{\text{BUSAK1}}$	28
29	SYSCLK	+	+	+STBY	29
30	−12V	+	+	+12V	30
31	+5V	+	+	+5V	31
32	gnd	+	+	gnd	32

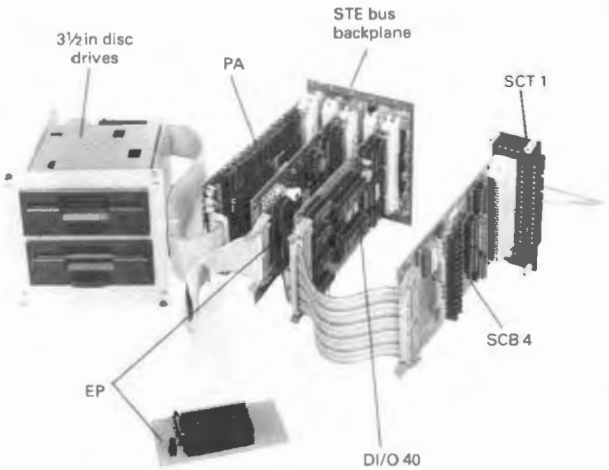
STE bus 64-way a/c DIN 41612 connector pin-out (connector on backplane viewed from board side).

Typical system configurations

PA system

This is an example of how to configure a software development system for a temperature control application (see Figure 7). It uses a PA processor board, terminal, two 3½in disc drives (630-594), CP/M Plus operating system, EP EPROM programmer board, D I/O 40 and AI16 peripheral boards, SCB2-T and SCB4 signal conditioning boards, power supply (612-013) and the associated hardware. It can be used to develop software in 8080 assembly language modules using the CP/M Plus utilities. Alternatively BASIC programs may be developed under CP/M Plus control using RS BASIC. These programs may be stored on, or run, from disc. In addition, the programs may be programmed into an EPROM using the EP board and used to run a target system based on the PB board. Target systems based on the PA board would be ideally suited to data logging type applications where large amounts of information may be stored on the discs. Target systems not requiring the storage capacity of discs could be based around the lower-cost PB board.

Figure 7 **PA based development system**



A PA based system allows the use of disc drives for the storage of large amounts of data. Removing the EP board and adding an AI 16 and SCB2-T would convert the above to a PA based temperature control system.

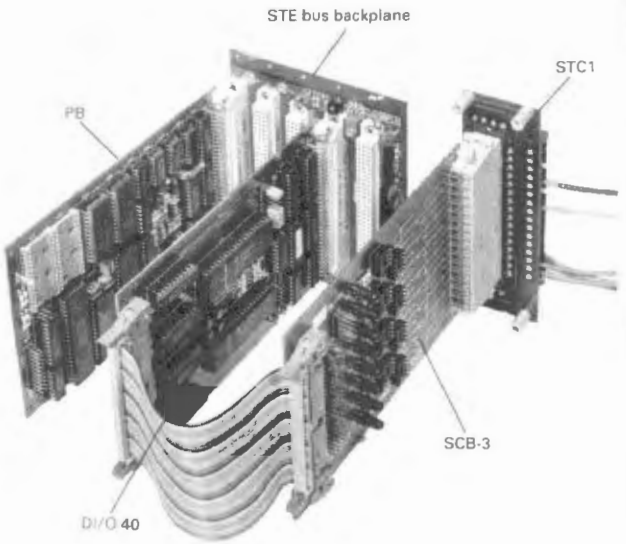
The AI16 and SCB2-T convert temperatures measured with 590kH sensors (stock number 308-809) to digital values which can be displayed on the screen and used by the PA to decide for example, whether to switch heater relays on or off. The relays can be switched by a D I/O 40 board connected to an SCB4 Darlington driver board. The Darlington driver inputs and the temperature sensor outputs connect to external equipment via SCT1 cable terminators.

PB System

The PB board may be used as a low cost development system without disc drives (for simpler applications) or as a low-cost target system where the storage capacity of disc drives is not needed. To configure a PB board development system the following items are required: PB processor board, a terminal, EP EPROM programmer board, power supply, associated hardware, RS BASIC (631-890) for BASIC language program development and/or PB monitor (631-907) for writing and debugging Z80 machine code programs. Also needed would be the appropriate peripheral and signal conditioning boards. For the target system the EP EPROM programmer board may be removed, and the programmed EPROM plugged in to the target PB board. A typical PB board system for machine control with the DI/O 40 peripheral board and the SCB3 opto isolator signal conditioning board is shown in Figure 8.

With the addition of an FDC board the PB can access disc drives and run CP/M Plus (633-127). This can allow the development of real-time assembly language programs using the Microsoft M80 package. Programs may be debugged under CP/M using the ZSID utility (supplied with CP/M Plus). Also disc based BASIC may be used under CP/M Plus.

Figure 8 **PB based system**



A low cost PB target system. The addition of an EP board, terminal and software (see text) would convert it to a low cost development system.

Wiring considerations

Power supply wiring

If a PA or PB board is being used in a system without any other processor or peripheral boards a backplane is unnecessary and the power supply connection to the boards may be made using the 5-way cable socket housing and crimps supplied with the board. A suitable crimp tool is stock no. 533-241, and wires should have 0.5mm^2 conductors with a max. overall diameter of 1.6mm including the insulation. Consult the board manual for pin assignment details of the power connectors (PL5 for the PA board and PL2 for the PB board).

With other processor or peripheral boards in the system an STE backplane is necessary.

Figure 9 shows how a 5-slot backplane should be wired, and Figure 10 shows how a 10-slot backplane should be wired.

Figure 9 **5-slot backplane (viewed from rear)**

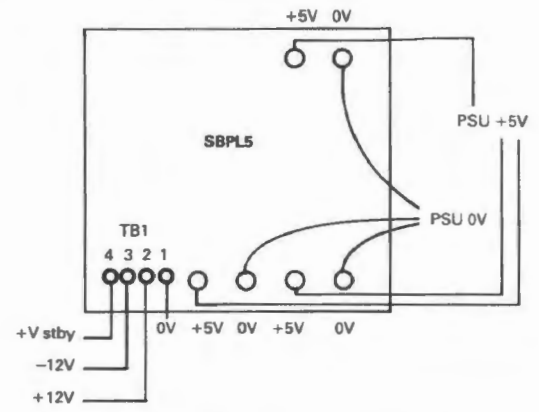
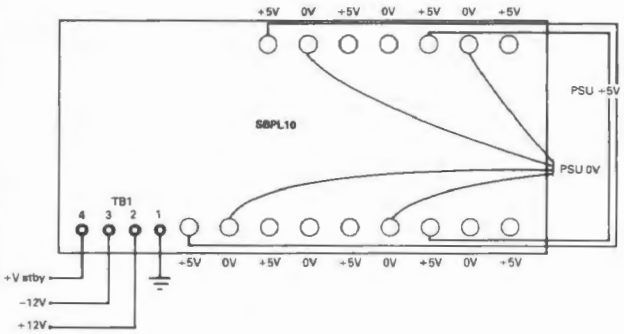


Figure 10 **10-slot backplane (viewed from rear)**



Use heavy-gauge wire for the +5V and 0V lines to minimise voltage drop. Connections to the backplane studs should be made with M4 (2BA) tags (stock number 532-529 for solder tags or 532-715 for crimp tags). The ±12V wires carry relatively low current, and are screwed into the terminal block TB1 on the backplane. The +V standby line can be used for battery backup on CMOS RAMs if connected to a suitable supply (note that the C-RAM board already has a battery on it so you may not need this feature).

A detailed specification of the power supply (stock no. 612-013) is given in the current RS catalogue. For board power consumption details see Table 1.

It is recommended that two bleed resistors and a diode are fitted if the minimum load requirement of the RS switch mode power supply (612-013) is not met i.e. 1A across the 5V, 8A output and a total load of 13W across all outputs. Suitable resistors are 4R7, 25W (stock No. 157-544) for the +5V, 8A output and 10R, 25W (stock No. 157-550) for the +12V, 3A output. These aluminium clad resistors should be fitted in parallel with the respective outputs and may be bolted directly to the sub-rack side panels. The inclusion of a reverse-biased high

Table 1 **Typical power consumption figures for processor and peripheral boards.**

Board \ Voltage	+5V±0.25V	+12V±1V	−12V±1V
PA	1.2A	30mA	30mA
PB	700mA	30mA	30mA
EP	350mA	120mA	–
C-RAM fully populated with 8KB devices	550mA (operating)*	–	–
DRAM fully populated with 256K bit devices	550mA	–	–
DI/O 40	550mA	–	–
AI 16	400mA	30mA	30mA
FDC	550mA	–	–
SERCOM 4	700mA	100mA	40mA
SWC	450mA	10mA	10mA
IEEE 488	400mA	–	–
A I/O 8/2	400mA	20mA	20mA
STMC (excluding motor current)	500mA	–	–
IOP (excluding any custom circuitry)	180mA	–	–

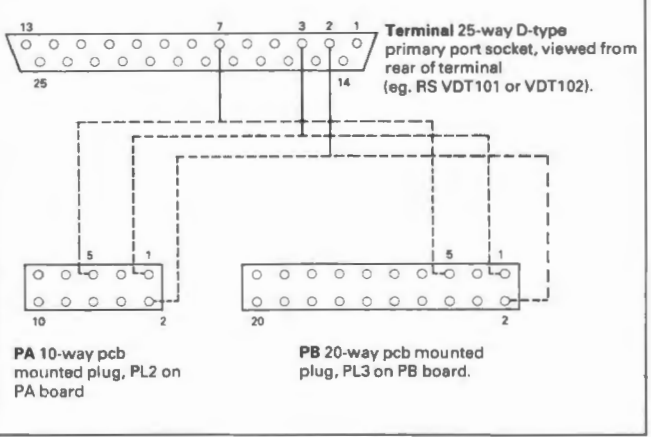
*** The powered down battery drain of a fully populated C-RAM is 200μA.**

power zener diode (stock No. 283-334) across the semi-regulated +12V, 3A output will help protect against over voltage conditions. This diode may also be bolted directly to the sub-rack side panel with an insulating mounting kit (stock No. 261-283). The +12V power for floppy disc drives should be taken from the fully regulated +12V, 1.5A output.

Video display terminal connection

There are only three connections to be made between the terminal and the PA or PB. They are shown in Figure 11.

Figure 11



The video display terminal should be set to 9600 baud, bit 8 = 0 (8-bit words), no parity, two stop bits and full duplex character mode. The handshaking, if required, should be set to Xon/Xoff (since both RS BASIC and CP/M Plus will support this) but is not necessary and may be set to 'NONE'.

Note that the RS terminals (VDT 101 and 102) have a key labelled 'NO SCROLL' which toggles scrolling on and off. If this is inadvertedly pressed the terminal will appear to 'hang-up'. To solve the problem press the key again.

Disc drive connection

The PA board will connect directly to one or two disc drives, whilst the FDC will connect up to four drives, which may be any combination of the RS 3½in or 5¼in double sided, double density drives (630-594 and 300-158). If using any other drives it is important to establish that they are completely compatible with these. Of particular importance is the track to track access time which must be 3ms.

Link selection

One of the drives must be link selected to be drive 0 and the other must be set to be drive 1. These are designated under CP/M Plus as drive A and drive B respectively. The other link selections for an RS disc drive are shown below in Table 2.

Table 2 **Disc drive link selection**

3½in: (630-594)	MO, FG set on. Either DS0 or DS1 selected as appropriate. All other links not selected. (The FG links connects 0V to frame ground and may be removed if not required.)
5¼in: (300-158)	UR, SM, HS set on. Either DS0 or DS1 selected as appropriate. All other links not selected.
5¼in: (633-509)	IU, RY, EO, FG. Either DS0 or DS1 selected as appropriate. All other links not selected. If both U1 and U2 are also selected, the drive indicator will illuminate only whilst the drive is being accessed.

Mounting and power connection

A pair of drives may be mounted in a 3U sub-rack with the disc drive mounting kits (632-045 for 3½in and 632-051 for 5¼in drives). The drives require +5V, +12V and ground connections to the power supply. These drive power leads should be wired directly between the disc drives and power supply and NOT via the terminals on the backplane. This is to prevent introducing noise on the backplane when the drives are selected/deselected.

Alternatively, the drives may be mounted separately from the sub-rack in the free-standing disc drive cases 501-963 for 3½in or 501-626 for 5¼in. These cases can be fitted with the optional disc drive power supplies 592-010 for 3½in or 591-972 for 5¼in.

Signal connection

This is made using a 34-way ribbon cable. A suitable mating connector for the PA board end of the cable is the 34-way cable mounting IDC socket 467-302. This will plug directly into PL4 of the PA board. Note that since the connector is not polarised it is important to ensure that pin 1 on the cable is connected to pin 1 on the board. At the disc drive end of the cable, suitable connectors are

467-302 for the 3½in drives and 471-288 for the 5¼in drives.

Note that the pcb connector on the RS 3½in drives have pin 34 marked with a ▲, contrary to the normal convention where pin 1 is marked with a ▲.

The terminators on 3½in drives are not removable, whereas with 5¼in drives the terminator network must be removed from all drives except the final drive in a multiple drive configuration.

Note on 8in drives

Both configurations of CP/M Plus as supplied will actually support 3 drives and it may be possible, if sufficient design expertise is available to connect an 8in single sided single density drive (with a 3ms step rate) to the system as 'drive C'. The drive must use the industry standard IBM system 3740 format (FM recording). On the Processor A drive C is selected when both the drive 0 and drive 1 signals are low, so some external logic is necessary because drive 0 and drive 1 are also selected when their respective drive select signals are low. Since 8in drives may vary in the pin-out configuration of the signal connector the wiring must be custom designed. Refer to the appropriate manufacturer's 8in drive manual and the RS PA board manual for pin-out details. The FDC has two disc drive signal connectors, one for RS 3½in and 5¼in disc drives and the other for 8in drives having a signal interface compatible with the Shugart 800 series drives.

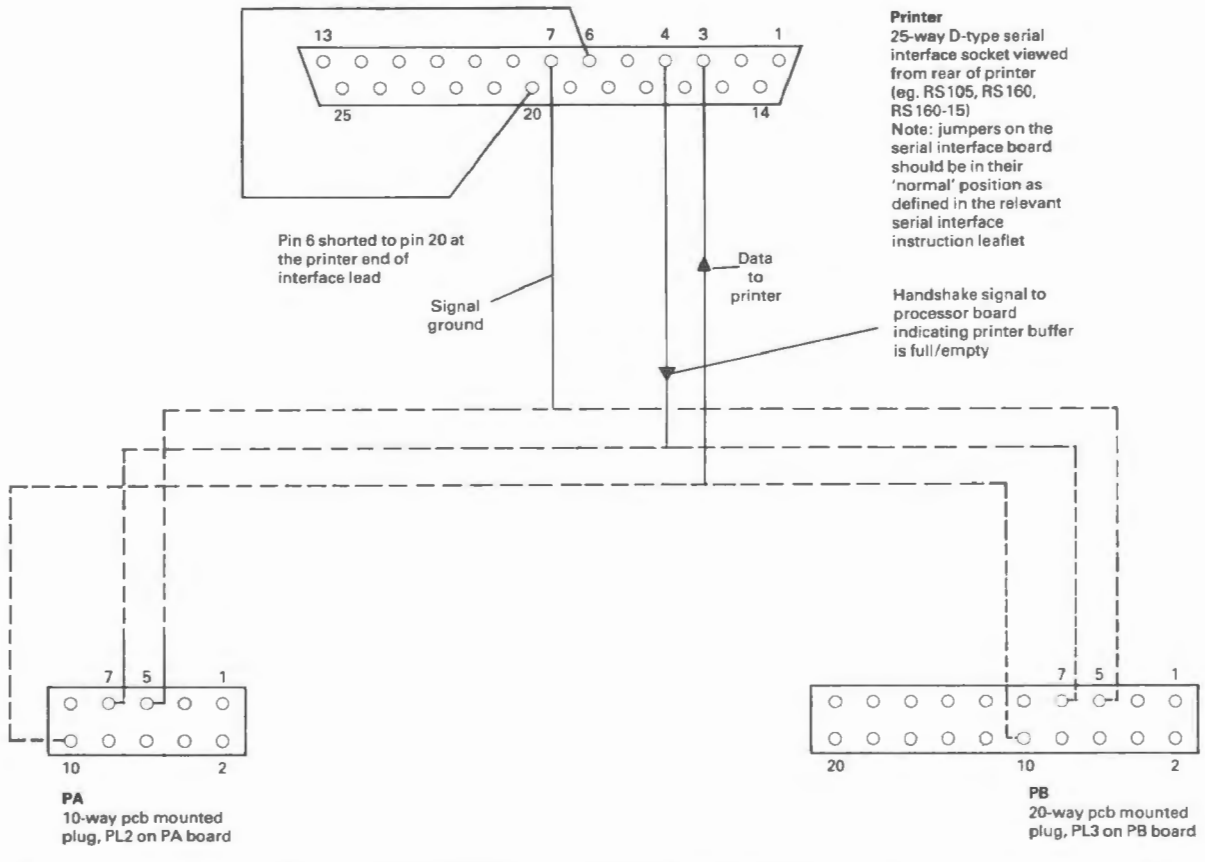
The inclusion of this 8in drive support in the software does allow system designers the ability to transfer CP/M file software from older 8in drive systems where considerable time investment in software development may have been made, or where CP/M software is only available on 8in discs with the IBM 3740 single density format. Alternatively, it may be possible to transfer software files via a serial link using the CP/M PIP command.

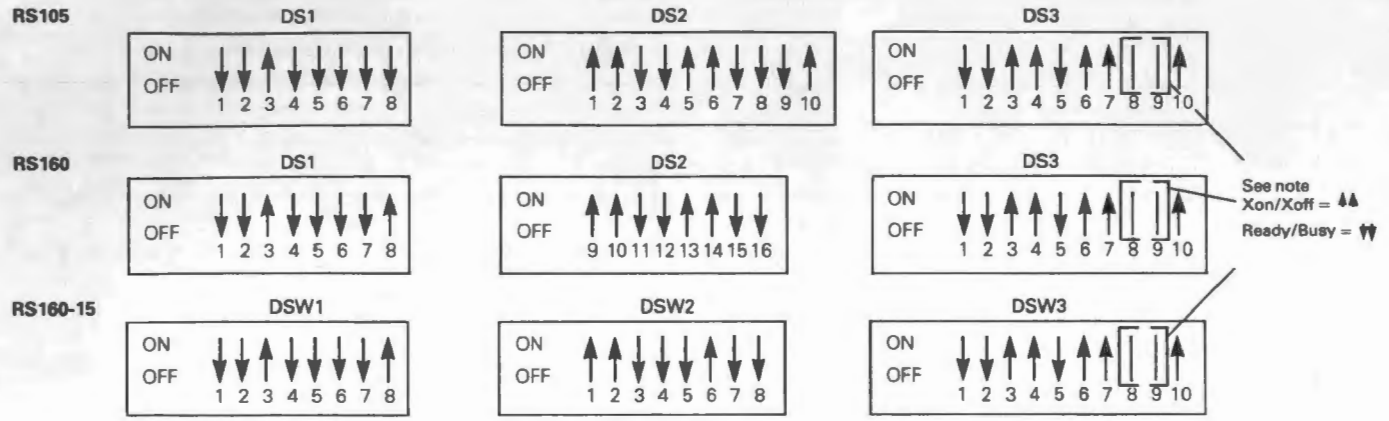
Printer connection

a) Ready/Busy hardwire handshaking

There are three connections to be made between an RS printer (RS105, RS160, or RS160-15) and the PA or PB processor boards (see Figure 12).

Figure 12





Note: DS3-8 and DS3-9 select the handshake protocol: with both switches set to ON, Xon/Xoff is selected; and with both switches set to OFF, Read/Busy handshaking is selected.

For other printers: The essential set-up details are:
RS232 serial interface
Standard ASCII character set
CR code = CR (CR = CRLF will give double spacing)
Character receiving buffer
1200 baud
No parity
8 data bits
2 stop bits

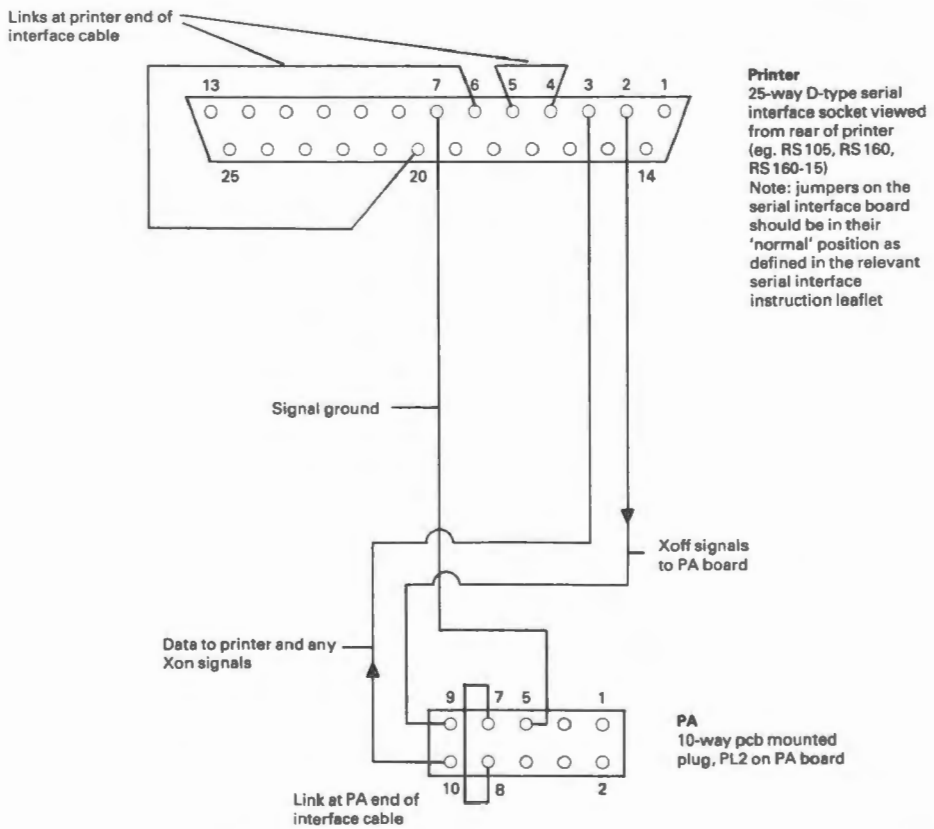
b) Software Xon/Xoff handshaking

The PA board could be used with Xon/Xoff handshaking if the printer is tied in an active state and if Xon/Xoff handshaking is enabled in CP/M Plus using the DEVICE command:

DEVICE LST: = LPT [1200, XON]

to disable Xon/Xoff handshaking, XON in the above command is replaced by NOXON. For connections between the RS printer and the PA board, see Figure 13.

Figure 13



Support hardware

The processor and peripheral boards are all designed to allow fitting into a eurocard sub-rack together with either a 5 or 10 slot backplane.

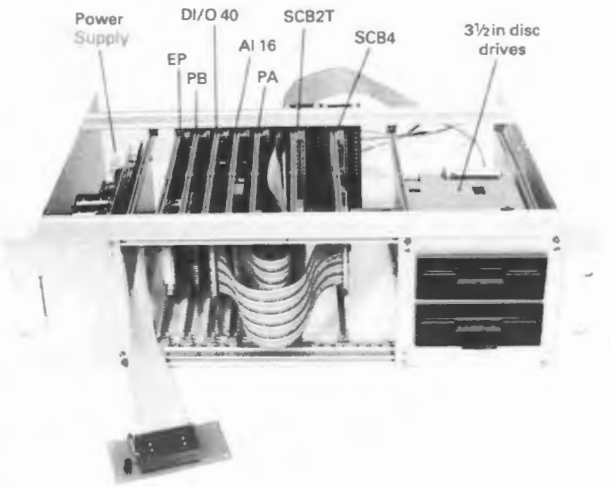
Table 4 lists the support hardware available to enable a compact system to be built in a 3U 84E sub-rack. This list includes rack mounting kits for RS3½in and 5¼in disc drives and the RS612-013 switched mode power supply.

Figure 14 illustrates a system fitted to a eurocard sub-rack.

Details

Although the boards are all 160mm eurocards the 3U sub-rack kit should be assembled for 220mm deep cards as described on RS Eurocard sub-rack Data Sheet (see current catalogue for details) to enable the front mounting cables and the RS 612-013 power supply to fit neatly into the rack.

Figure 14 **STE board computer system fitted in a eurocard rack**



A 5 or 10 slot backplane should be fitted to the motherboard mounting rails as illustrated in Figure 15 (note the fitting of the two insulated strips supplied between the rail and backplane). Adequate clearance should be allowed at one end of the case for the power supply; when using an RS power supply 612-013 which occupies 14E the first connector on the backplane should be aligned with position 18 on the mounting rails. The card guides should then be fitted and where possible a eurocard should be plugged in before tightening the backplane screws, to ensure correct alignment of the backplane.

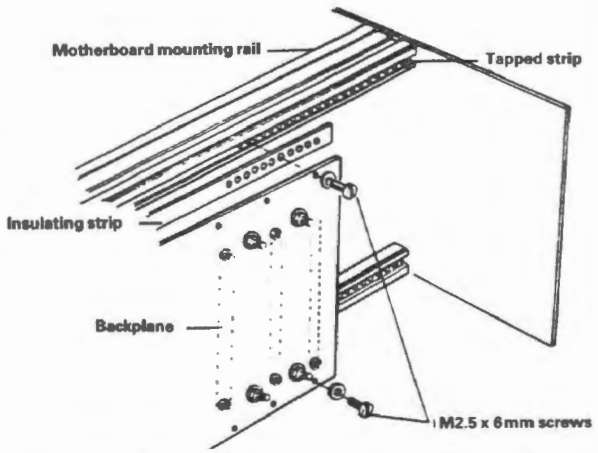
Power supply

The RS power supply 612-013 is supplied fitted with a front panel and support plate to enable the unit to be fitted on a pair of 220mm card guides into the sub-rack unit.

Disc drive mounting kits

There are two mounting kits available RS 632-045 for 3½in disc drives and RS 632-051 for 5¼in disc drives. Each kit provides a front panel and support plate to enable two drives to be fitted into the sub-rack. To minimise interference it is recommended that disc drives are fitted away from power supply and processor boards.

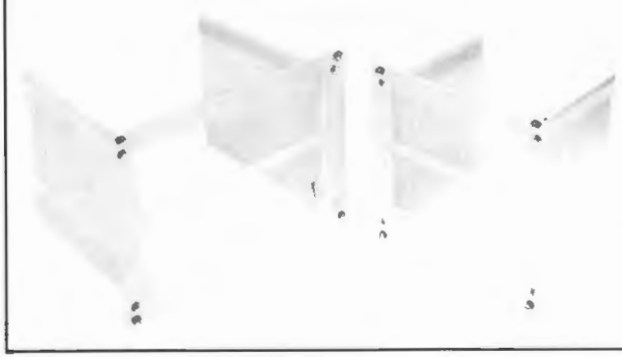
Figure 15 **Fitting of STE backplane**



Note position of insulating strip between motherboard mounting rail and backplane.

The total usable width of the RS sub-rack is 84E (1E = 0.2in) and the current RS catalogue details the relevant unit widths to enable calculation to be made of the possible combinations that will fit into the sub-rack.

Figure 16 **Disc drive mounting kits**



Interboard connections

Figures 7 and 8 illustrate typical configurations and shows how all processor and peripheral board interconnections are made via the STE backplane, connections between the peripheral boards and the signal conditioning boards are made from the front of the boards using 50 way ribbon cable RS 360-201 and 50 way ribbon cable mounting sockets RS 474-344. Similarly, connections from the processor board to disc drives, terminals and printers are made at the front of the board. In order to achieve an organised layout of cables it is recommended the boards are fitted in the orders shown in Figure 14. This allows ribbon cables from the processor boards to be passed round the side of the backplanes to the rear of the disc drives and to printer and terminal connectors, also the peripheral (I/O) to conditioning board connections will be conveniently nested.

To enclose the front of the sub-rack 3U 10E card fronts (508-841) and 3U 4E card fronts (508-835) can be used.

Table 4 **Support hardware**

Item	Stock No.	Comments
3U eurocard sub-rack kit	502-916	
19in racking case 3U		Consult equipment housing section of current RS catalogue for further details.
Style 1	508-778	
Style 2	501-165	
Style 3	502-219	
STE bus backplanes		
5 slot	632-017	Supplied with insulating strips, and on-board terminators.
10 slot	632-023	
Signal cable terminators (SCT1)	632-001	Screw terminals for I/O cable connections.
Power supply	612-013	Eurocard mounting, secured by front plate screws. Supplied with mating connector. Suitable for mounting on 220mm card guides.
Disc drive mounting kits		
3½in	632-045	Allows horizontal mounting of two RS disc drives in a eurocard sub-rack fitted with card guides.
5¼in	632-051	
Card guides (eurocard sub-rack)		
160mm	502-764	The 220mm deep mounting of the STE bus boards allows sufficient space at the front for interconnecting cables and the locking latches on the board connectors if fitting a front panel to the sub-rack, as would be required for installed control systems. The 160mm deep mounting allows easier access to the connectors at the front and facilitates insertion/removal of the boards and is therefore better suited to development systems. Note: the power supply (as supplied) is 185mm deep and will therefore protrude through the rear mounting rails on a 160mm deep sub-rack. It is also suited to 220mm deep systems.
220mm	502-770	
M2.5 x 20mm slotted pan head screws	523-812	Necessary for fixing SCT1 to motherboard mounting rails. Supplied in packs of 100.
M2.5 x 6mm slotted pan head screws	523-799	Necessary for fixing STE bus backplane to motherboard mounting rails. Supplied in packs of 100.
Connectors		
50-way cable mounting socket	474-344	Necessary for ribbon cable interconnection of peripheral boards and signal conditioning boards (right angle pcb mounting plug at front of boards). Note the socket is 'bump' polarised.
34-way cable mounting socket	467-302	Necessary for disc drive cable connection to PA board.
10-way cable mounting socket	467-273	Necessary for connection to serial channels on PA board.
20-way cable mounting socket	467-289	Necessary for connection to serial channels on PB board.
Solder tags	532-529	} Power supply connection to mother boards
Crimp tags	532-715	

R.S. Components Ltd. PO Box 99, Corby, Northants, NN17 9RS
An Electrocomponents Company

Telephone: 0536 201234
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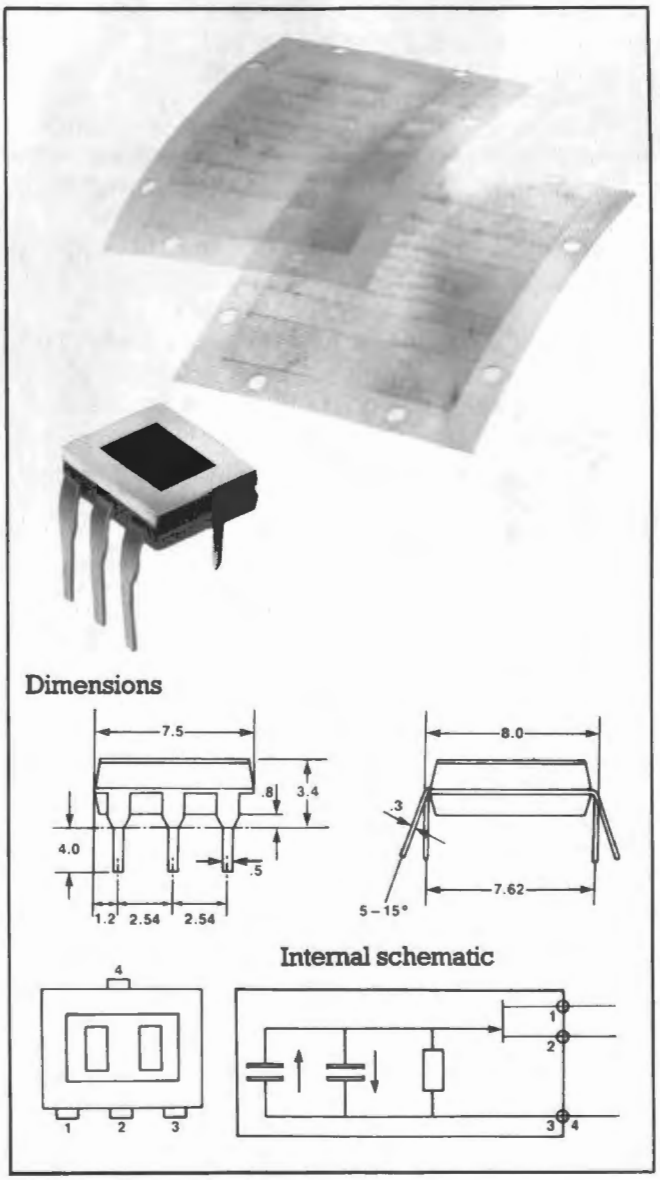
RS
Data Library

Pyroelectric detector kit

Stock number 256-275



Features

- Sensitive to changes in 'target' temperature (in field of view)
- Fast IR analysis
- Temperature measurement by radiation
- Flame observation
- Counting facility
- Positioning facility.

Applications

- ▲ Passive infra-red alarms/intruder units
- ▲ Automatic light switches
- ▲ Automatic door openers
- ▲ Counting/Positioning equipment
- ▲ Radiation thermometers
- ▲ Radiometry
- ▲ Spectrometry
- ▲ Gas analysis
- ▲ Flame control.

Specifications

Frequency response	0 – 0.3Hz : + 6dB/oct. 0.3 – 0.5Hz : flat 1Hz + : −6dB/oct.
Supply voltage	3 to 15Vdc
Source resistor*	100 – 200kΩ
Current consumption	200μA max
Output impedance	5 – 10kΩ
Operating temperature	−40°C to +100°C
Storage temperature	−55°C to +125°C

*When operated in source follower circuit.

The pyroelectric detector kit available in the RS range is suitable for many applications, some of which are described in this Data sheet.

General

Pyroelectric radiation detectors are used to indicate electromagnetic radiation, particularly infra-red radiation.

The internal sensor element consists of a capacitor in the shape of a thin plate (the dielectric), which has a temperature dependent spontaneous polarisation perpendicular to the electrode surfaces. The radiation to be measured is absorbed by the sensor material, causing a rise in temperature, which in turn causes changes in this polarisation that can be measured as a voltage at the electrodes, proportional to the incident radiation.

Due to their thermal and electrical properties, pyroelectric detectors have a frequency dependent band pass characteristic, whose centre frequency is within the range of 0.2 – 1Hz.

They are therefore ideal as radiation sensitive elements in passive infra-red motion sensors for operation from 0.1 up to several kHz in direct or multiplex mode.

Detector characteristics

Package	Dual in line machine insertable	Units
Element spacing	1	mm
Actual element size (equivalent to Industry Standard 2 × 1)	1.7 × 0.9	mm
Field of view geometrical	h=120 v=100	deg.
Field of view optical	h=116 v=96	deg.
Optical bandwidth	7.....13.5	μm
Voltage responsivity R (500°K:1Hz)	3200	V/W
Noise equivalent power (500°K:10Hz:1Hz)	1×10^{-9}	W
D (500°K:10Hz:1Hz)	1.4×10^{8}	cm$\sqrt{\text{Hz/W}}$
Maximum of peak noise	40	μV
Offset voltage*	0.3....2.5	V
Common mode rejection	> 20	dB
Maximum of temperature change	2	K/minute

*Following conditions apply:
1 Supply voltage 9V, 2 Load resistance = 100kΩ, 3 Source resistance = 100kΩ,
4 Measured at pin 2.

Types of performance

As the sensor unit represents a capacitive signal source with extremely high output impedance, a noise adjusted impedance transformer is required for the electric signal transmission. Thus, the impedance transformer is a part of the detector and hermetically sealed together with the sensing elements.

The IR sensing material lithium-tantalate is used, therefore the responsivity is independent of the temperature within the operating temperature limits.

Due to the high level of common mode rejection the main applications of dual element detectors are in the field of PIR-burglar alarm systems, positioning units, automatic light switches and dooe openers.

Spectral sensitivity
Standard window material of detectors is silicon, coated for an optical bandwidth of 7 – 14μm.

The noise equivalent power 'NEP'
The limit of evidence of a radiation detector is reached, when the signal produced by the low incoming radiation power can no longer be distinguished from the inevitable noise. This smallest provable radiation power is described by the quotient of radiation flux H and the signal to noise ratio us/un respectively is/in (with un = noise voltage and in = noise current).

In addition, λ or Ts, respectively, the frequency f and the electrical bandwidth Δf of the noise voltage are also stated:

$$NEP\ (\lambda : f : \Delta f) = Hx\ (us/un)\ (W)$$
$$NEP\ (Ts: f : \Delta f) = Hx\ (us/un)\ (W)$$

Correspondingly, *i*/in stands for current.

The detectivity 'D'
The detectivity 'D' is reciprocal to the noise equivalent power 'NEP':

$$D\ (\lambda : f : \Delta f) = (NEP)^{-1}\ (W)^{-1}$$

If the output noise is only produced by the actual detector element itself and not by the following electronics, then the parameter (D × A) ½ is a constant when A is the effective detector area. Also, in many radiation detector types the noise voltage is independent of frequency over a wide frequency range, and therefore the Detectivity 'D' is inversely proportional to the square root of the electrical bandwidth ΔF. For this reason the generalised detectivity equations:

$$D^*\ (\lambda : f) = (\Delta f \times A)\ ½\quad (NEP)^{-1}$$
$$D^*\ (Ts : f) = (\Delta f \times A)\ ½\quad (NEP)^{-1}$$

were introduced with (cm$\sqrt{\text{Hz/W}}$) as a unit of quality of radiation detectors.

The performance of different detectors can be compared by taking the values of D* into consideration.

However, it is not possible to compare detectors if the condition, D (A × f) = constant, is not fulfilled, as is the case with pyroelectric detectors. In this case the bandwidth of the noise measurement should be indicated as D* (Ts : f : Δf) which deviates from the standard notation. As defined in this way, D and NEP are related in terms of signal and RMS noise – it is not possible therefore to use these figures when designing intrusion sensors. This application demands the definition of the maximum peak noise voltage occurring within the operating temperature of the device.

Therefore, to assist the designer, the IR detectors specify both RMS noise and maximum peak noise.

Characteristics of thermal radiation detectors

In order to select the most suitable detector for any application, three basic characteristics must be stated:

1. The spectral dependence of the response required
2. The response time or the frequency response required
3. The noise equivalent power required.

The responsivity 'R'
Depending on the detector being either a current or a voltage source, the current responsivity Rc = i/H or the voltage responsivity Rv = u/H is defined.

Here 'H' represents the radiant flux incident on the detector and i or u for the signal current or signal voltage generated by the detector.

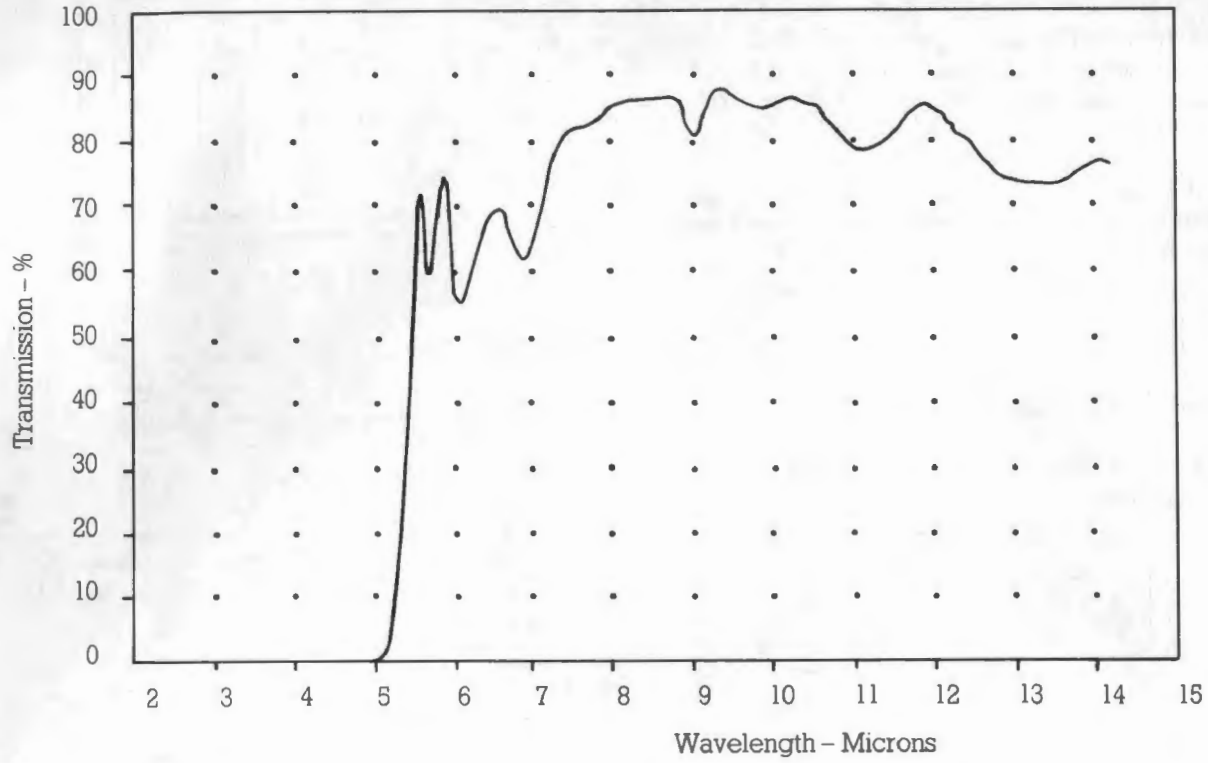
In addition, the corresponding wavelength or the temperature Ts of the blackbody radiation source are indicated.

The frequency response of the responsivity 'R'
This is the dependence of the responsivity 'R' on the modulation frequency 'f' of the incoming radiation.

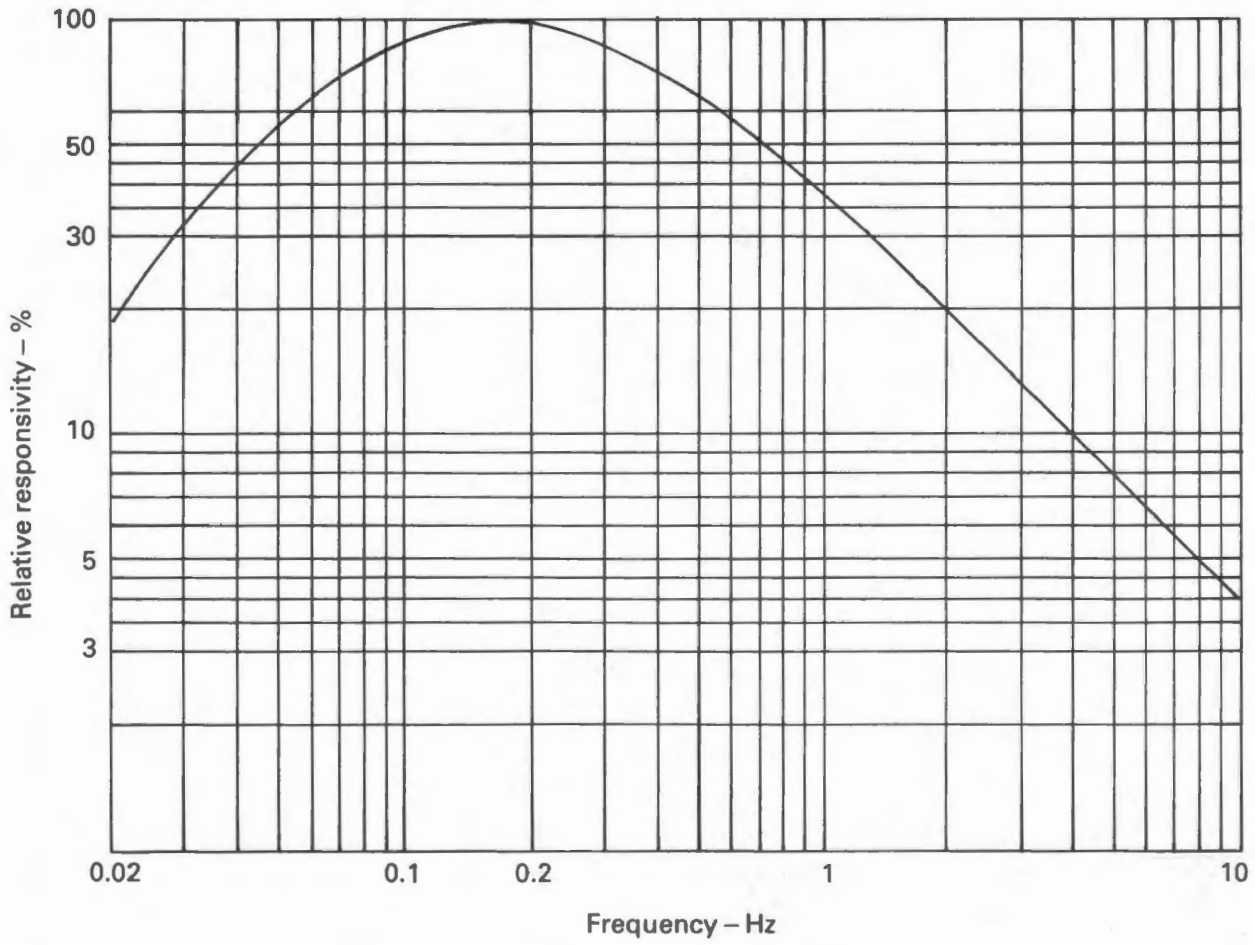
The frequency response of most detectors shows low pass characteristics. Beyond an upper frequency limit $fg = (2\pi\tau)^{-1}$ the responsivity of a thermal detector increases with I/f, where 't' represents the time constant (response time) of the detector; below fg it is constant (dc sensitivity).

Therefore the responsivity is fixed as: R (λ : f) or R (Ts : f) where λ is the radiation wavelength and Ts the absolute temperature of the blackbody radiation source.

Spectral transmission of standard window



Relative responsivity vs. frequency



Lenses

Material. These Fresnel lenses are made from UV-inhibited high density polyethylene. This material resists breakdown for up to 4 times longer than non-inhibited material.

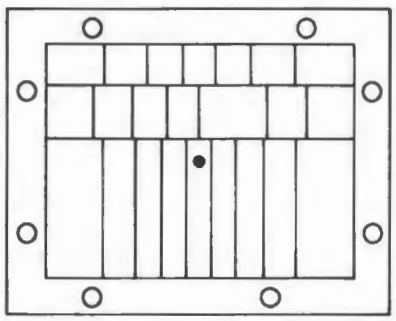
Design of optics. All Fresnel surfaces are aspheric in form, giving sharper zone edges and greater sensitivity and range for a given gain. The detector will therefore be less susceptible to **false alarms**.

Construction. A unique mastering technique ensures cleaner facet edges and tighter thickness tolerance. More reliable performance is thereby ensured.

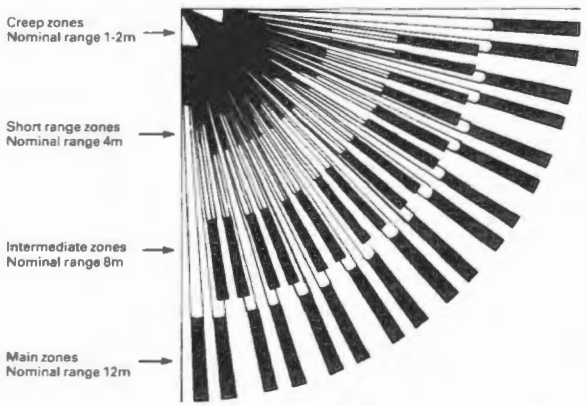
Beam patterns. These have been designed so that intruders crossing the pattern are caught; not only that, intruders approaching the lens from the front are also detected. The unique integral creep zones face downwards at 60° and cannot be avoided.

Technical details and fields of view

Volumetric lens



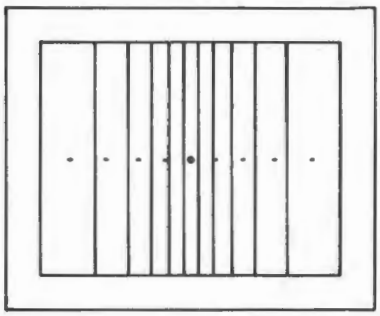
24 facets	9 main, 8 intermediate 5 short, 2 creep zones
Detector position	Dead centre
Lens focal length	25mm
Lens dimensions (optics)	52×40mm
Lens dimensions (frame)	64×52mm
Facets face	Towards detector
Facet form	Aspheric
Refractive index	n=1.52 at 10.6 microns
Nominal range	12m at normal gain
Use in flat or curved format	(25mm radius)



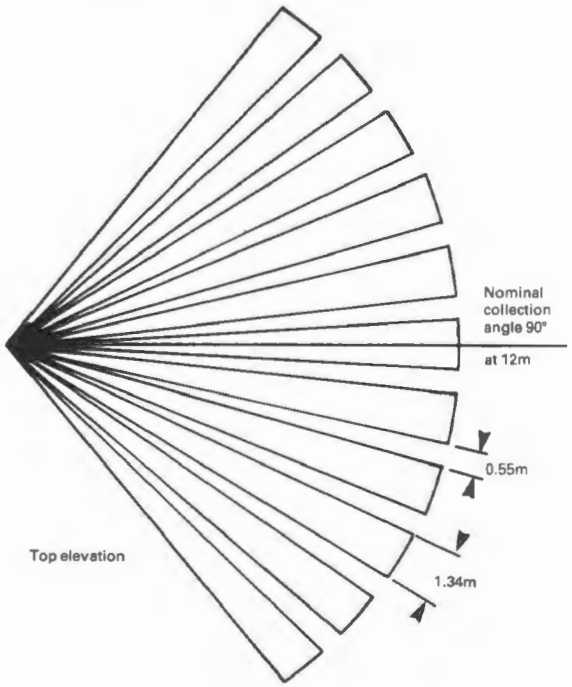
PF24 fields of view – top elevation

PF24 fields of view – side elevation
Dual element detector mounted at a height of 2 metres

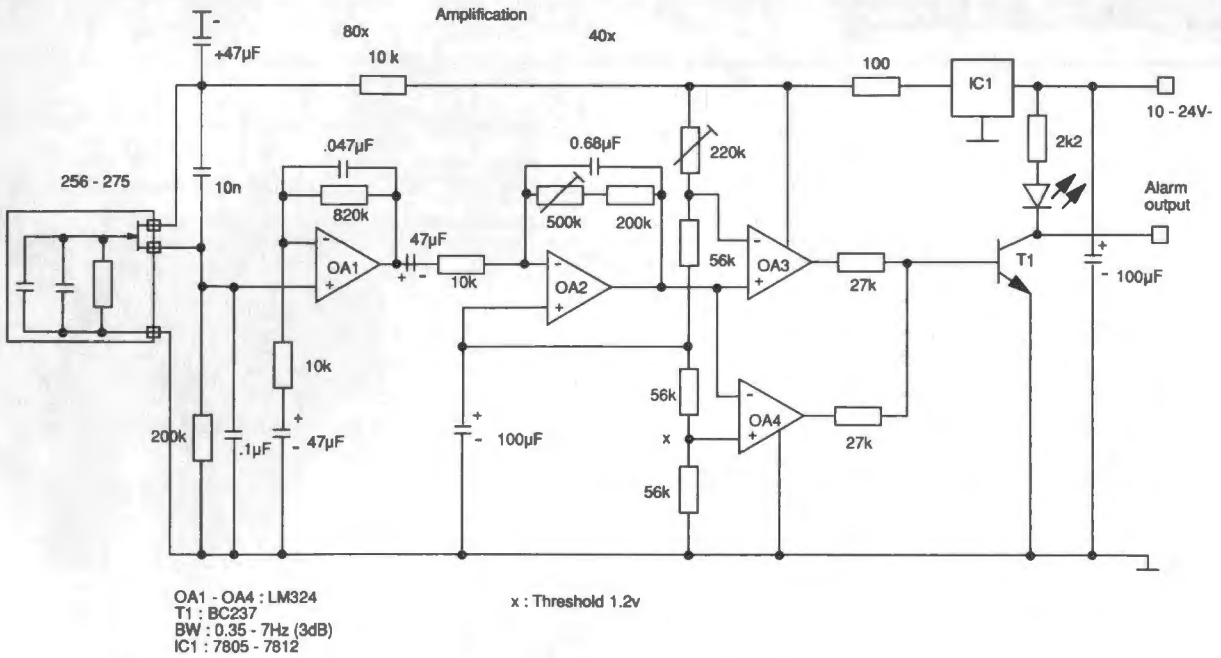
Curtain lens



11 facets	
Facets face	Towards detector
Facet form	Aspheric
Refractive index	n=1.52 at 10.6 microns
Nominal range	12m
Use in flat format	
Detector position	Dead centre
Lens focal length	25mm
Lens dimensions (optics)	52×40mm
Lens dimensions (frame)	64×52mm



Typical circuit for light switching and alarm applications



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