6 Fault Localization to Component Level

6.1 Fault Localization in the Frequency Converter

6.1.1 Information on the Frequency Response Correction for Bands 0, 1, 2 and 3

If any module in the signal path from the input socket [12] through to (6)J2 including all waveguides is repaired or replaced, adjustment of the frequency response is necessary.

A special test setup is used to determine the frequency response correction values during "adjustment". Compensation tables are generated and stored in the SNA for each of the receive bands (0, 1, 2 and 3). The values in the tables are then applied to the measured values during normal operation of the SNA to give the correct display values.
Recording the frequency response correction values requires a complex computer-controlled test setup and can only be performed by service centers specially equipped for this task.

> ***Caution!***
>
> If a fault is located in a microwave module, the entire module and associated control circuit should be replaced. The microwave module should not be opened. Opening the modules invalidates the guarantee and such modules can no longer be repaired in the factory.

Troubleshooting within the microwave modules is therefore not covered by this service manual. Chapter 5 describes fault localization to defective microwave modules. If the fault is in the control circuit for the module, a repair may be possible in exceptional cases. Normally, the entire module, complete with control circuit, should be replaced.

6.1.2 Integration Band 0 Control [2101-CF]

Error signals F1 and F2 are generated by the microwave module "Integration Band 0". The error signals are not evaluated by the instrument software; they can be checked on the Integration Band 0 Control board using an oscilloscope. Use the circuit diagram as an aid to troubleshooting and check the DC working points first.

DC working points (voltages at test points and connectors)

U_J6 and U_J7	+5.0 V ± 50 mV		
U_J8 and U_J9	-3.6 V		
U_J4	+11 V		
U_J5	-2.5 V to -1.5 V	if Band 0 ON;	(MP1.8: 5 V)
	-0.4 V to 0 V	if Band 0 OFF;	(MP1.8: 0 V)
U_J10	+10.7 V		

Error signal F1

The +5 V supply voltage for the hybrid working point regulator (J6, J7) is current-limited. This voltage is also compared with a reference voltage at the same time. If the voltage drops below the reference, error signal F1 is generated (HIGH to MP10.9).

Error signal F1 may be due to the following:

- Current drain on the +5 V supply too high
- +12 V, -12 V, +6.5 V operating voltages missing

Error signal F2

A check is made that the VCO is locked. If the VCO is not locked, error signal F2 is generated (HIGH to MP10.10).

Error signal F2 may be due to the following:

- 400 MHz signal to socket J22 missing
- Supply voltage (J10) for 400 MHz amplifier missing
- +18 V, +12 V, -12 V operating voltages missing
- Beat frequency at TP1 >15 MHz (offset range too high). Once it is certain that there is no error in the RF circuit and that none of the above faults is present, R54 must be re-adjusted, as described in section 7.6.2 on page 7-15.

The PLL circuit can assume four states:

- I VCO locked, normal operating state
- II VCO not locked and offset range <15 MHz, search oscillator oscillating at approx. 80 Hz, VCO locks within about 20 ms.
- III VCO not locked, offset range approx. 15 to 20 MHz, search oscillator oscillating, VCO cannot lock because voltage span of tuning voltage is max ± 0.6 V.
- IV VCO not locked, offset range >20 MHz, search oscillator off as offset range too high.

6.1.3 YIG Filter 3FL1 and YIG Filter Control

Introduction

The YIG filter characteristic is determined individually and stored in Flash ROM on the YIG filter controller.
Recording the YIG filter characteristic requires complex computer-controlled equipment and can therefore only be performed in service centers specially equipped for this purpose.

If the YIG filter or the YIG filter controller is replaced, the YIG filter characteristic must be recorded and stored for the new components (see section 7.5.3).

6.1.3.1 YIG Filter Control [2101-AS1]

Checking the power supply

Measure the following voltages on circuit board [2101-AS1] using a DVM:

Test point	Value	Notes
U46, Pin1	+24 V	Operating voltages for (1)ST6 (PSU / Voltage distribution)
R1	+23 V	
R79	+5 V	
R75	-18 V	
Voltages "generated" on-board		
Q4 (emitter)	+15 V	
Q5 (emitter)	-15 V	
U42 Pin7	+7 V (V-Ref)	DAC reference voltage
Voltage drop across R74	approx. 220 mV	YIG heater current , approx . 220 mV (ca. 100 mA) when YIG thermally stable.

Table 6-1 YIG filter controller [2101-AS1] operating and supply voltages

Checking the function of the YIG filter controller

The basic function of the controller is checked by measuring the current through the YIG filter at various frequency settings. To do this, open the connection J21/P21 (MCX plug) and insert an ammeter in series with the YIG filter. Set the D.U.T. to FSTART = 3.2 GHz and FSTOP = 30 GHz. Manually tune the SNA to various frequencies in the range 3.2 to 30 GHz. A certain current, dependent on the frequency setting, must flow through the YIG filter; this value should increase continuously as the frequency increases. Typical values of YIG current for a given YIG frequency are shown in table 6-2.

Important: The current increase is not necessarily linear, as it depends on the YIG characteristic which is determined during adjustment (see section 7). The correction values are programmed into the Flash ROM on the YIG filter controller board during adjustment. The measured values (FCENT, current through YIG filter) may thus differ from the values in the table, but a continual increase in the current with increasing frequency must be measurable.

FCENT	Current through YIG filter	FCENT	Current through YIG filter
3.2 GHz	95 mA	16 GHz	480 mA
4 GHz	120 mA	18 GHz	540 mA
4.5 GHz	135 mA	20 GHz	600 mA
6 GHz	180 mA	22 GHz	660 mA
8 GHz	240 mA	24 GHz	720 mA
10 GHz	300 mA	26 GHz	785 mA
12 GHz	360 mA	28 GHz	845 mA
14 GHz	420 mA	30 GHz	905 mA

Table 6-2 Typical YIG frequency / YIG current values

If no increase in current can be measured for increasing frequencies, there is a fault in the YIG controller or in the interfaces to the input section controller (control, frequency band information) or to the synthesizer (frequency information).

Checking the interface to the synthesizer

The synthesizer frequency information can be checked against table 6-3. Set the D.U.T. to FSPAN = 0 (MAN Tuning) and to the frequencies (FCENT) in the table. If the frequency information is correct, the signals given in the table will be present at U1 and U2 of the YIG filter controller board [2101-AS1].

Test point	FCENT			Signal name
	2 MHz	15 GHz	29.662 GHz	
U1 PIN2	1	1	1	FS(0)
U1 PIN3	0	0	1	FS(1)
U1 PIN4	0	0	1	FS(2)
U1 PIN5	0	0	1	FS(3)
U1 PIN6	0	0	1	FS(4)
U1 PIN7	0	1	1	FS(5)
U1 PIN8	0	1	1	FS(6)
U1 PIN9	0	1	0	FS(7)
U2 PIN2	0	1	0	FS(8)
U2 PIN3	0	1	1	FS(9)
U2 PIN4	0	1	1	FS(10)
U2 PIN5	0	0	1	FS(11)
U2 PIN6	0	1	0	FS(12)
U2 PIN7	0	1	1	FS(13)
U2 PIN8	0	0	1	FS(14)
U2 PIN9	0	0	0	FS(15)

Table 6-3 Table for checking the synthesizer frequency information

If the signals do not correspond to the table, there is a fault in the synthesizer controller board [2101-A] in the area of the YTF-PORT.

6.1.3.2 Checking the YIG Filter

Once the tests above have been made, the pass-band characteristic of the YIG filter in its built-in state can be checked. This check assumes correct function of the YIG filter controller.

Connect a sweepable RF generator to the input of the D.U.T. and set the instruments as follows:

D.U.T.

FCENT:	5.5 GHz (any frequency above 3.2 GHz)
FSPAN:	120 MHz
REFERENCE:	= TX level of generator
SCALE:	50 dB
SWT	100 s

Generator

FCENT:	5.5 GHz (any frequency above 3.2 GHz)
FSPAN:	120 MHz
SWT:	0.5 s (or smallest possible value)

First tune the D.U.T.to FCENT (5.5 GHz) (FSPAN = 0) and set switch 3S2 on the YIG filter controller board to YIG Hold. This locks the YIG filter at the previously set frequency (5.5 GHz) even if the input frequency to the D.U.T. is changed.
Set the SPAN to 120 MHz again, and sweep the D.U.T. slowly. If the controller is working properly, the pass-band of the YIG filter will be shown on the display. A typical pass band characteristic is shown in fig. 6-1.

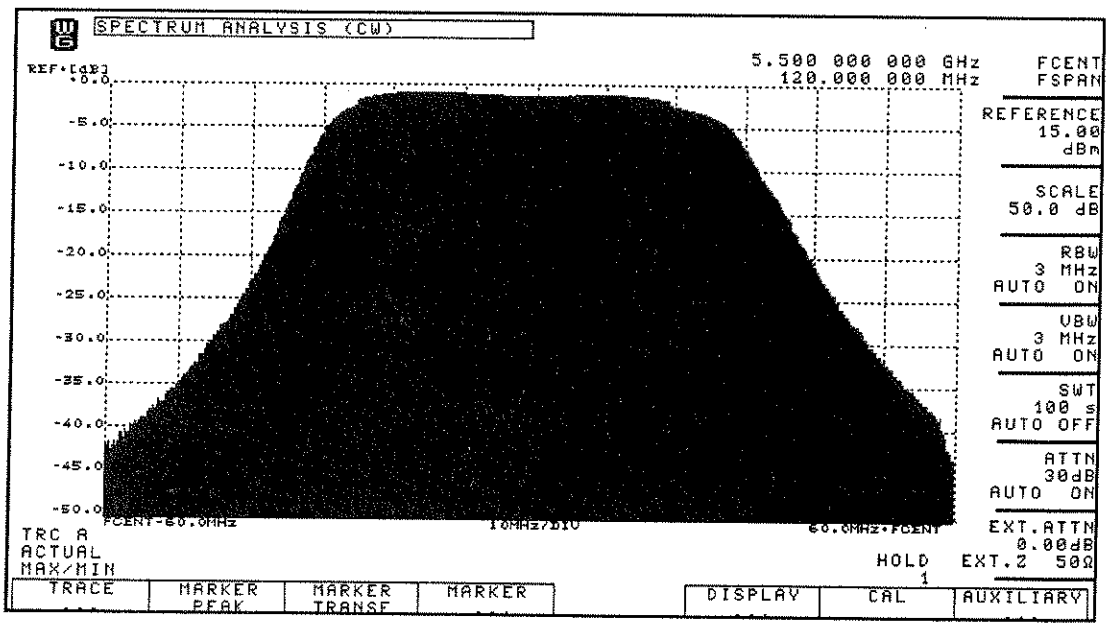

Fig. 6-1 Typical pass-band characteristic of YIG filter 3FL1

If the YIG filter is faulty, it must be replaced. Frequency response correction is required after replacing the YIG filter (see "Information on the Frequency Response Correction for Bands 0, 1, 2 and 3" on page 6-1).

6.1.4 Fundamental Mixer Controller [2101-AV1]

The error signal is generated on the fundamental mixer controller. It is not evaluated by the instrument software but can be checked with an oscilloscope at MP2.4; ERROR SIGNAL on the fundamental mixer controller board.

Error signal

The error signal may be due to the following causes:

- Current drain on +5 V voltage too high
- +6.5 V operating voltage missing
- +12 V operating voltage missing
- -12 V operating voltage missing

DC working points (voltages at the test points and plug connectors)

U_TP1	+ 9.3 V
U_TP2	- 9.3 V
U_J1, U_J2, U_J3	+ 5.0 V ± 50 mV
U_J6	- 3.5 V

Band switching control signals

The band switching control signals can be checked against table 6-4. Set the D.U.T. to FSPAN = 0 and set FCENT to a frequency in the band required. Band ranges are listed in table 6-5.

Band	TP6	TP7	J9	J10	J11	J12	J13	J14
0	L	L	1	1	0	1	1	0
1	H	L	0	1	1	1	0	1
2	L	H	0	1	0	0	1	1
3	H	H	1	0	1	0	1	1

Table 6-4 Band switching control signals on the fundamental mixer controller board

L : 0 V
H : 5 V
0 : negative voltage: approx. -6 V to -10 V, depending on control pin
1 : positive voltage: approx. 10 V

Note: Remove the fundamental mixer from its fixing plate to access the test points.

Band	Start of band	End of band
0	0 Hz	3.199999999 GHz
1	3.2 GHz	7.499999999 GHz
2	7.5 GHz	14.999999999 GHz
3	15.0 GHz	26.5 GHz (30 GHz)

Table 6-5 SNA-23 frequency band limits

6.1.5 IF Switch [2101-AQ1]

Checking the supply voltages

The operating voltages for the IF switch module [2101-AQ1] are derived from the input section controller board (5). Check the voltages against the table below.

Test point	Value
C245	+12 V
C244	-12 V

Table 6-6 IF switch [2101-AQ1] operating voltages

Checking the drive signals

The IF switch allows one of the three inputs (421.99 MHz IF level) to be switched through to the output (J204)The three input signals are fed into the MCX sockets (J201, J202 and J203).

- J201: Input signal fed from "Band 0 frequency converter" microwave module, when the SNA is tuned to a frequency in Band 0 (RF 0 to 3.199 GHz).
- J203: Input signal fed from "Fundamental mixer" microwave module, when the SNA is tuned to a frequency in Band 1,2 or 3 (RF 3.2 GHz to 30 GHz).
- J202: Input signal fed from socket [70] "IF-INPUT". This input is selected when the SNA is in SPECTRUM ANALYSIS (EXT MIXER) mode.
- J204: IF switch output.

Check the IF switch control signals against the following table:

Setting	Test point		Notes
	C243	C242	
Band 0	1	0	Insrument tuned in Band 0, IF switch input J201 selected
Band 1 ... 3	0	0	Insrument tuned in Band 1,2 or 3, IF switch input J203 selected
EXT MIXER	0	1	SPECTRUM ANALYSIS (EXT MIXER) mode set, IF switch input J202 selected (= BU 70 on instrument back panel)

Table 6-7 IF switch [2101-AQ1] control signals

Checking the signal paths

Use a network analyzer, e.g. SNA-62 to measure the gain of the three signal paths at 421.99 MHz. Normalize the SNA-62 (short circuit) before each measurement. The SNA-62 input is connected to J204 (output) of the IF switch.

Important: The gain values quoted for the three paths are approximate; the actual values may differ (by approx. ± 2 dB) without a fault being present. Level matching has been carried out in this module to cope with the scatter in component values between different series of the instrument. A much larger difference in the level is to be expected if there is a fault, so that this method can be used to check for a faulty IF switch.

Band 0 signal path

Set the SNA-62 TX level to -42 dBm (50 Ω) and connect the generator output to input J201 of the IF switch. Set the D.U.T. to a frequency in Band 0 (e.g. FCENT 100MHz, FSPAN 0). Read off the gain on the SNA-62.

Nominal value: Gain +9 dB

Band 1, 2 and 3 signal path

Set the SNA-62 TX level to -58 dBm (50 Ω) and connect the generator output to input J203 of the IF switch. Set the D.U.T. to a frequency in Band 1,2 or 3 (e.g. FCENT 10 GHz, FSPAN 0). Read off the gain on the SNA-62.

Nominal value:	Gain +16 dB	(Series A + B)
	Gain +19 dB	(Series C onward)

External mixer signal path

Set the SNA-62 TX level to -30 dBm (50 Ω) and connect the generator output to input J202 of the IF switch (or Bu 70 on the back panel). Set the D.U.T. to SPECTRUM ANALYSIS (EXT MIXER) mode. Read off the gain on the SNA-62.

Nominal value:	Gain +16 dB	(Series A + B)
	Gain +19 dB	(Series C onward)

If the gains of the three signal paths differ significantly from these values, the IF switch chould be replaced.

6.1.6 Input Section Control [2101-AR]

Attenuator drive

The settings of switches S2.2, 2.3 and 2.4 select a control table for driving the attenuator (ATTN) as determined by the setting made. The switch settings are scanned by the PIO module (5)U11 and the control words corresponding to the selected control table are output for controlling the attenuator from this same module (Port 3).
To check the attenuator drive, the settings of switches S2.4, S2.3 and S2.2 must first be determined. These settings determine the control table (see table 6-8). The table lists all attenuator types which have been used up till now.

S2.4	S2.3	S2.2	Attenuator (Range/Steps/ Frequency range)	Control table no.
0	0	0	65 dB/5 dB/26.5 GHz (Weinschel 5690-1)	1
0	0	1	70 dB/10 dB/40. 27 GHz (W&G FED-5/02, HP 33321 G/K)	2
0	1	0	70 dB/5 dB/4 GHz (W&G FED-5/01)	3
0	1	1	70 dB/10 dB/4 GHz (Weinschel 151-70)	4
1	0	0	Not used	-

Table 6-8 Control table for selecting various types of attenuator (control table no.)

Once the correct control table has been established, the attenuator drive can be checked against one of the tables below. Set the input attenuator (ATTN) to the values stated and check the control words at the stated test points using an oscilloscope.

Note: The control words shown in the control tables can only be measured during the switching phase of the attenuator, as the attenuator relays are bistable. In the idle state, all test points are HIGH ("1").

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
0	1	1	1	1	0	0	0	0
5	1	1	1	0	0	0	0	1
10	1	1	0	1	0	0	1	0
15	1	1	0	0	0	0	1	1
20	1	0	1	1	0	1	0	0
25	1	0	1	0	0	1	0	1
30	1	0	0	1	0	1	1	0
35	1	0	0	0	1	1	1	1
40	0	1	0	1	1	0	1	0
45	0	1	0	0	1	0	1	1
50	0	0	1	1	1	1	0	0

Table 6-9 Control table no.1

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
55	0	0	1	0	1	1	0	1
60	0	0	0	1	1	1	1	0
65	0	0	0	0	1	1	1	1

Table 6-9 Control table no.1

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
0	1	1	1	1	0	0	0	0
10	1	1	1	0	0	0	0	1
20	0	1	1	1	1	0	0	0
30	0	1	1	0	1	0	0	1
40	0	0	1	1	0	1	0	0
50	0	0	1	0	1	1	0	1
60	0	0	0	1	1	1	1	0
70	0	0	0	0	1	1	1	1

Table 6-10 Control table no.2

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
0	1	1	1	1	0	0	0	0
5	1	0	1	1	0	1	0	0
10	1	1	1	0	0	0	0	1
15	1	0	1	0	0	1	0	1
20	0	1	1	1	1	0	0	0
25	0	0	1	1	1	1	0	0
30	0	1	1	0	1	0	0	1
35	1	1	0	1	0	0	1	0
40	1	0	0	1	0	1	1	0
45	1	1	0	0	0	0	1	1
50	1	0	0	0	0	1	1	1
55	0	1	0	1	1	0	1	0

Table 6-11 Control table no.3

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
60	0	0	0	1	1	1	1	0
65	0	1	0	0	1	0	1	1
70	0	0	0	0	1	1	1	1

Table 6-11 Control table no.3

ATTN attenuation/ dB	Test point							
	IC 4.11	IC 4.13	IC 4.12	IC 4.15	IC 4.14	IC 4.16	IC 4.17	IC 4.18
0	X	1	1	1	X	0	0	0
10	X	1	1	0	X	0	0	1
20	X	0	1	1	X	1	0	0
30	X	0	1	0	X	1	0	1
40	X	1	0	1	X	0	1	0
50	X	1	0	0	X	0	1	1
60	X	0	0	1	X	1	1	0
70	X	0	0	0	X	1	1	1

Table 6-12 Control table no.4 (X = no significance)

Checking the EXT mixer bias current

Switch (5) S2.10 must be closed (BIAS ON setting). Unsolder the connection to (2) C241 (IF_U\Bias EXM) and connect an ammeter (digital multimeter, range ± 20 mA DC) between (2) C241 and the unsoldered cable. Set the D.U.T. to SPECTRUM ANALYSIS (EXT MIXER) mode.

Set the "DC-Bias" to 12.8 mA (SPECTRUM ANALYSIS (EXT MIXER) menu) and compare with the display on the digital multimeter.

Nominal value: 12.8 mA ± 0.05 mA

Set the "DC-Bias" in the external mixer menu to 0 mA and compare with the display on the digital multimeter.

Nominal value: 0 mA ± 0.05 mA

6.1.7 Interdigital Filter (6IF1)

The interdigital filter can be checked with a network analyzer (e.g. SNA-62). The settings for the SNA-62 are shown in fig. 6-2. Make these settings and then normalize the SNA-62. Connect the SNA-62 generator output to the filter input (J1) and the filter output (J2) to the SNA-62 input.

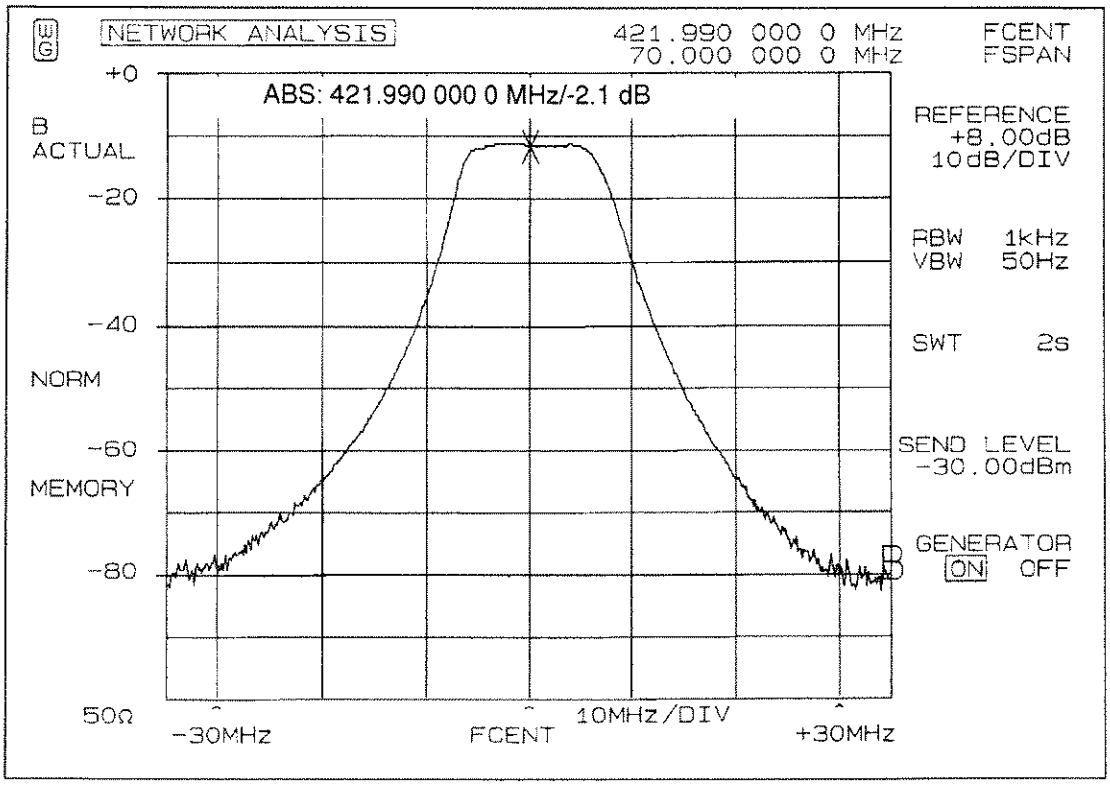

Fig. 6-2 Typical pass-band characteristic for interdigital filter 6IF1

The insertion loss of the interdigital filter at f_0 (422 MHz) should not exceed 2.5 dB. The attenuation minimum must be at exactly 422 MHz (421.99 MHz). If these values are not obtained (particularly the minimum at 422 MHz), the filter should be replaced. Do not attempt to adjust the filter, as special equipment is required for this.

6.1.8 422 MHz/22 MHz Converter [2101-X]

Checking the power supply

Measure the following voltages with a DVM:

Test point	Nominal value
TP 2.1	10.5 V ± 0.2 V
TP 2.2	5.2 V ± 0.2 V
TP 1.3	-10.0 V ± 0.2 V
C 13	5.0 V ± 0.1 V

Table 6-13 422 MHz/22 MHz converter [2101-X] power supplies

If the nominal values are not met, use the circuit diagram to troubleshoot.

Checking the 400 MHz carrier generator

Measure the following voltages with a DVM:

Test point	Nominal value
IC 5.2	3.0 V ± 0.2 V
GL 4	6.5 V ± 0.5 V

Table 6-14 400 MHz carrier generator

If the nominal values are not met, there is a fault in the frequency generator.

Set the D.U.T. to SPECTRUM ANALYSIS (CW) and measure the level of the 400 MHz carrier using a probe (with 1:10 divider) and a spectrum analyzer as in the following table.

Test point	Nominal value
IC 9.4	+19 dBm ± 1 dB (50 Ohm)
R 57	+ 9 dBm ± 1 dB (50 Ohm)
T 8.E	+12 dBm ± 1 dB (50 Ohm)

Table 6-15 Frequency generator test points

Remember to take the 20 dB attenuation of the 1:10 divider into account.
The frequency may be between about 380 MHz and 420 MHz if the frequency generator is faulty.

If the carrier level and frequencies are correct, further troubleshooting as under "Checking the 422 MHz/22 MHz converter signal path" on page 6-16.

Checking the 400 MHz oscillator

Open the regulator loop by unsoldering **(6) R 26** and feed an external control voltage from a PSU to (6) R 26 - R 25.
If the oscillator still does not oscillate, troubleshoot using the circuit diagram and check the following working points:

Test point	Nominal value
C 67	9.7 V
C 27	9.5 V
C 22	9.5 V
C 47	9.5 V
C 37	4.8 V

Table 6-16 Typical working points for checking the 400 MHz oscillator

If the oscillator oscillates when the external control voltage is applied, measure the frequency at (6) IC 9.4 using a probe (with 1:10 divider) and a spectrum analyzer. Alter the control voltage from the PSU as per the table and compare the frequencies with the values in the table.

Control voltage	Frequency
0 V	377 MHz
2 V	383 MHz
4 V	388 MHz
6 V	396 MHz
8 V	405 MHz
10 V	415 MHz
12 V	425 MHz

Table 6-17 Typical frequency values as a function of control voltage

Checking the frequency divider (400 MHz)

Set the control voltage from the PSU so that the oscillator runs at approx. 400 MHz. Measure the following signals with an oscilloscope (see fig. 6-3).

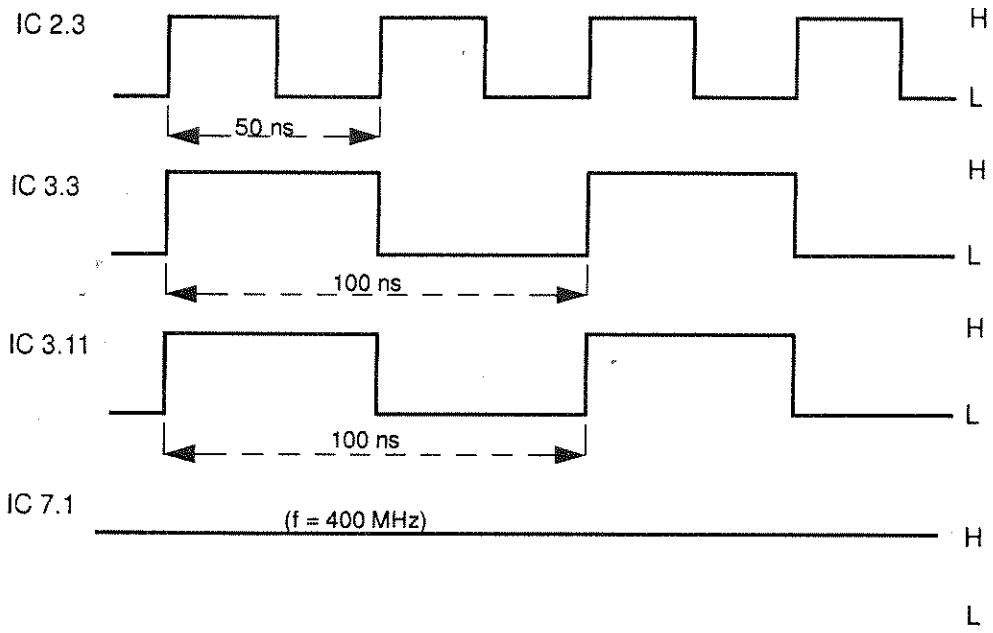

Fig. 6-3 Test points for checking the 40:1 divider (L = 0 V, H = 5 V)

If the oscillograms look different, troubleshoot using the circuit diagrams.

Checking the phase meter (400 MHz)

Set the control voltage from the PSU so that the oscillator runs at approx. 390 MHz. Measure the following signals with an oscilloscope (L = 0 V, H = 5 V):

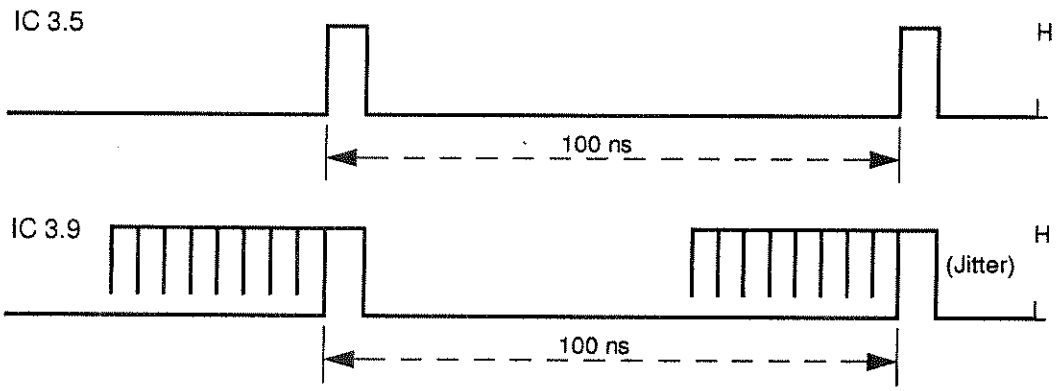

Fig. 6-4 Oscillograms for checking the phase meter

Set the control voltage from the PSU so that the oscillator runs at approx. 410 MHz. Measure the following signals with an oscilloscope (L = 0 V, H = 5 V):

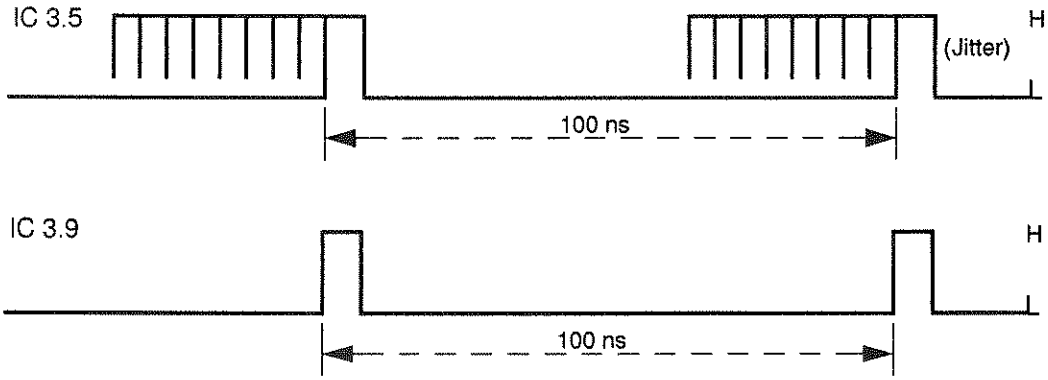

Fig. 6-5 Oszillogramme zur Überprüfung des Phasenmessers

If the oscillograms look different, troubleshoot using the circuit diagrams.

Note: Solder (6) R 26 back in place after the measurements.

Checking the 422 MHz/22 MHz converter signal path

Checking the DC working points in the signal path

Measure the following DC working points using a DVM:

Test point	Nominal value
IC 8.3	5.5 V ± 0.5 V
IC 13.3	5.5 V ± 0.5 V
IC 14.3	4.4 V ± 0.2 V

Table 6-18 Signal path DC working points

If the nominal values are not met, troubleshoot using the circuit diagrams.

Signal path level check

Connect a level generator to the input of the D.U.T.

D.U.T.: SPECTRUM ANALYSIS (CW)
FCENT 22 MHz
FSPAN 0 Hz, (RUN MAN)
REFERENCE 0 dBm
ATTN 40 dB

Level generator: 22 MHz, 0 dBm (50 Ω)

Measure the signal level using a probe and a spectrum analyzer (see table 6-19).
Measure the 400 MHz carrier level at IC9.4 using a probe (with 1:10 divider) and a spectrum analyzer (see table 6-15 on page 6-13).

Test point	Frequency	Nominal value
R 102	421.99 MHz	-40 dBm ± 1 dB (50 Ω)
R 103	421.99 MHz	-42 dBm ± 1 dB (50 Ω)
R 65	421.99 MHz	-30 dBm ± 1 dB (50 Ω)
R 64	421.99 MHz	-33 dBm ± 1 dB (50 Ω)
R 60	21.99 MHz	-40 dBm ± 1 dB (50 Ω)
R 59	21.99 MHz	-43 dBm ± 1 dB (50 Ω)
R 11	21.99 MHz	-31 dBm ± 1 dB (50 Ω)
R 114	21.99 MHz	-29 dBm ± 1 dB (50 Ω)

Table 6-19 Signal path levels

If the nominal values are not met, troubleshoot using the circuit diagrams.

6.2 Troubleshooting the IF measurement section

6.2.1 IF selection [2101-L]

Function check

Bu4 on the IF selection board leads to the external IF output Bu10 [60] on the back panel. The function of the IF selection can thus be checked without opening the instrument
Feed a level of -30 dBm (50 Ω) into the D.U.T input, socket [12] eingespeist. Set the D.U.T. to the frequency of the generator (FCENT = TX frequency, e.g. 20 MHz; FSPAN = 0 Hz; RUN MAN). The D.U.T. REFERENCE is also set to -30 dBm gesetzt. At a D.U.T. resolution bandwidth (RBW) of 10 MHz (bypass path), the signal at Bu4 or Bu10 [60] on the back panel should be -10 dBm, F = 21.99 MHz when terminated with Ra = 50 Ω.
The level result should be approximately the same for RBWs of 3 MHz, 1 MHz, 300 kHz, 100 kHz, 30 kHz, 10 kHz and 1 kHz.

If there is a level error during the above check, a manual measurement can be used for troubleshooting:

Measurement of operating voltages

TP16:	+12 V	(I ≤ 0.2 A)
TP18:	-12 V	(I ≤ 0.2 A)
TP17:	+5 V	(4.75 V to 5.45 V)
TP19:	-5 V	(-4.75 V to -5.45 V)
TP15:	-10 V	(-9.16 V to -10.86 V. Inverted reference voltage from GI400 for DAC)
TP10:	-7.8 V	(-7.15 V to -9.0 V, reference voltage for amplifier stages V2 to V5 referred to +5 V.

Measuring the signal path level (without selection filter)

Feed a level of approx. -30 dBm (f = 21.99 MHz) into the IF selection input socket (7BU1) and set the D.U.T. as follows:

FCENT	21.99 MHz
FSPAN	0 Hz (RUN MAN)
SCALE	10 dB
RBW	10 MHz (bypass path, no selection filter active)
VBW	10 MHz
INPUTT ATTN	0 dB
REFERENCE	-27 dBm
AUTO CAL	OFF

Close wire link 17.1 - 18 on the IF selection board. This drives IF selection amplifier stage V1 with maximum gain, v = 6 to 7.5 dB (v = 1 with wire link open).

This setting switches the following signal path on the IF selection board:

Input:	7BU1
Pre-attenuator 0/-14 dB:	0 dB
Amplifier V1:	maximum (v = 6 to 7.5 dB)
Filter path:	bypass (no LC or crystal filter switched in)
Amplifier V2	0 dB
Attenuator 0/-2 dB	0 dB
Amplifier V3	0 dB

Attenuator 0/-1 dB	0 dB
Amplifier V4	0 dB
Amplifier V5	0 dB

Use a level meter or spectrum analyzer to troubleshoot by measuring the level as per table 6-20 with a high-impedance probe (e.g. TK-10).

> ***Caution!***
> Some test points are DC coupled, so always use a test probe.

Test point	Level	Notes
Bu1	-39 dB	Reference level f = 21.99 MHz
C 14	- 39dB	Pre-attenuator 0 dB
Pin 1 von V1	- 26 dB	Input V1; gain T2/UE2 ca. 13 dB
TP 3	- 19 dB	Output V1; gain V1 = max
Pin 1 von V2	- 19 dB	Input V2
TP 6	- 19 dB	Output V2; gain V2 = 0 dB
Pin 1 von V3	- 19 dB	Attenuator 0/-2 dB set to 0 dB
TP 7	- 19 dB	Output V3; gain V3 = 0 dB
Pin 1 von V4	- 19 dB	Attenuator 0/-1 dB set to 0 dB
TP 8	- 19 dB	Output V4; gain V4 = 0 dB
TP 9	-19 dB	Output V5; gain V5 = 0 dB
BU3; TP 14	-7 dB	Output amplifier gain approx. 12 dB

Table 6-20 IF selection level table

Checking the IF amplifier stages and pre-attenuator

After this, the individual attenuators and amplifier stages can be switched singly or together and their function checked by setting the D.U.T. REFERENCE as per table 6-21 on page 6-20. Measure the output level at 7BU3 (use high-impedance probe, test point is DC coupled) and reduce or increase the input level in accordance with the attenuator or amplifier setting (see table 6-21 on page 6-20). The output level at 7BU3 must remain constant (same as for reference measurement, input level -30 dBm and D.U.T. reference setting -27 dBm). The D.U.T. reference settings required for full checking of the IF amplifier stages are shown in bold type in the table. The input signal to 7Bu1 required for these settings is also shown in the table.

Important: The pre-attenuator 0/-14 dB and amplifier V3 (0/-16 dB) cannot be activated singly. With the check method used, combinations of amplifiers are switched in such cases (reference settings -23 dBm and -56 dBm). If a fault occurs at these settings, all other amplifier stages and attenuators which can be switched singly should be checked first. A defective stage can thus be isolated.

Reference D.U.T.	Pre-attenuator 0/-14 dB	V2 0/16 dB	0/-2 dB	V3 0/16 dB	0/-1 dB	V4 0/8 dB	V5 0/4 dB	Input level at 7Bu1
-23 dBm	**1**	0	**1**	0	0	**1**	**1**	-26 dBm
-24 dBm	0	0	1	0	1	0	0	
-25 dBm	0	0	**1**	0	0	0	0	-28 dBm
-26 dBm	0	0	0	0	**1**	0	0	-29 dBm
-27 dBm	0	0	0	0	0	0	0	-30 dBm (ref. level)
-28 dBm	0	0	1	0	1	0	1	
-29 dBm	0	0	1	0	0	0	1	
-30 dBm	0	0	0	0	1	0	1	
-31 dBm	0	0	0	0	0	0	**1**	-34 dBm
-32 dBm	0	0	1	0	1	1	0	
-33 dBm	0	0	1	0	0	1	0	
-34 dBm	0	0	0	0	1	1	0	
-35 dBm	0	0	0	0	0	**1**	0	-38 dBm
-36 dBm	0	0	1	0	1	1	1	
-37 dBm	0	0	1	0	0	1	1	
-38 dBm	0	0	0	0	1	1	1	
-39 dBm	0	0	0	0	0	1	1	
-40 dBm	0	1	1	0	1	0	0	
-41 dBm	0	1	1	0	0	0	0	
-42 dBm	0	1	0	0	1	0	0	
-43 dBm	0	**1**	0	0	0	0	0	-46 dBm
-44 dBm	0	1	1	0	1	0	1	
-45 dBm	0	1	1	0	0	0	1	
-46 dBm	0	1	0	0	1	0	1	
-47 dBm	0	1	0	0	0	0	1	
-48 dBm	0	1	1	0	1	1	0	
-49 dBm	0	1	1	0	0	1	0	
-50 dBm	0	1	0	0	1	1	0	
-51 dBm	0	1	0	0	0	1	0	

Table 6-21 Divider and gain settings as a function of the REFERENCE setting

Reference D.U.T.	Pre-attenuator 0/-14 dB	V2 0/16 dB	0/-2 dB	V3 0/16 dB	0/-1 dB	V4 0/8 dB	V5 0/4 dB	Input level at 7Bu1
-52 dBm	0	1	1	0	1	1	1	
-53 dBm	0	1	1	0	0	1	1	
-54 dBm	0	1	0	0	1	1	1	
-55 dBm	0	1	0	0	0	1	1	
-56 dBm	0	1	1	1	1	0	0	-59 dBm

Table 6-21 Divider and gain settings as a function of the REFERENCE setting

Checking the selection filter

The selection filter can be checked using the procedure in the section "Checking the Specifications" in this service manual. If a fault is detected during checking of the selection filter, troubleshoot using the circuit diagram and the adjustment instructions in section 7.7.1.

6.2.2 Logarithmizer [2101-M]

6.2.2.1 Operating and bias voltages

The voltages should be measured in the order given below unless there are good reasons for not doing so:

Supply voltages

TP16: +6.5 V ± 0.3 V
TP17: -6.5 V ± 0.3 V
TP18: +12 V ± 0.5 V
TP19: -11.9 V to -13 V

Important: The voltage at TP19 is critical. It must not be below 11.9 V.

Voltages generated on the circuit board

TP21: +5 V ± 50 mV
TP22: -5 V ± 50 mV

D to A converter reference voltage

TP20: +10.6 V to +11.0 V

Logarithmic amplifier working point

Measure between TP19 (-12 V operating voltage) and TP10.

$U_{(TP19-TP10)}$ 4 V ± 10 mV

Rectifier reference voltage

TP7: -5.05 V to -5.15 V

Reference voltage after the buffer amplifier

U(TP8) = U(TP7) ± 2 mV

Rectifier threshold voltage

Measure between TP8 and TP9

$U_{(TP8 - TP9)}$ 900 mV ± 1.5 mV

Rectifier current source voltage

The voltage at TP6 must be 5.8 V ± 10 mV below the voltage at TP8.

TP6 ≈ -10.9 V

6.2.2.2 Troubleshooting the logaritnmizer signal path

The logarithmizer signal path can be checked using a spectrum analyzer (e.g. SNA-3 with TK-11) or a selective level meter (e.g. SPM-19 with TK-11). All signals in the logarithmizer signal path are in the IF range of 21.99 MHz. The test points andpositions of the log. stages are shown in fig. 6-6.

A level of -40 dBm at a frequency of e.g. 10 MHz is fed into the input of the SNA-20/-23. The following settings are made on the D.U.T/:

D.U.T.: SPECTRUM ANALYSIS (CW)
FCENT 10 MHz (= frequency of feed signal)
FSPAN 0 Hz, (RUN MAN)
REFERENCE 30 dBm
SCALE 100 dB
RBW 1 kHz
ATTN 35 dB

Level generator: 10 MHz, -40 dBm (50 Ω)

The measured levels should be as given in table 6-22.

Test point	Value	Notes
(7) TP14	approx. - 60 dB	IF selection output level, f = 21.99 MHz, **= reference level**
TP 23,25	approx. -63 dB	Level after buffer stage, corresponds to log. stage 1 input level. The two test points are identical
Log. stage 1, Pin 3, 9	- 63 dB	Log. stage 1 input level
Log. stage 1, Pin 13, 21	- 53 dB	Log. stage 1 output level
Log. stage 2, Pin 3, 9	- 53 dB	Log. stage 2 input level
Log. stage 2, Pin 13, 21	- 43 dB	Log. stage 2 output level
Log. stage 3, Pin 3, 9	- 43 dB	Log. stage 3 input level
Log. stage 3, Pin 13, 21	- 33 dB	Log. stage 3 output level
Log. stage 4, Pin 3, 9	- 33 dB	Log. stage 4 input level
Log. stage 4, Pin 13, 21	- 23 dB	Log. stage 4 output level

Table 6-22 Level table for checking the logarithmizer signal path

Test point	Value	Notes
Log. stage 5, Pin 3, 9 Log. stage 5, Pin 13, 21	- 23 dB - 13 dB	Log. stage 5 input level Log. stage 5 output level
Log. stage 6, Pin 3, 9 Log. stage 6, Pin 13, 21	- 13 dB - 3 dB	Log. stage 6 input level Log. stage 6 output level (corresponds to noise filter input level)
Log. stage 7, Pin 3, 9	- 3 dB	Log. stage 7 output signal, signal after noise filter If the level at htis point is incorrect, check the noise filter
Reduce the level at the input of the D.U.T. by 30 dB		
Log. stage 7, Pin 3, 9 Log. stage 7, Pin 13, 21	- 33 dB - 23 dB	Log. stage 7 input level Log. stage 7 output level
Log. stage 8, Pin 3, 9 Log. stage 8, Pin 13, 21	- 23 dB - 13 dB	Log. stage 8 input level Log. stage 8 output level
Log. stage 9, Pin 3, 9 Log. stage 9, Pin 13, 21	- 13 dB - 3 dB	Log. stage 9 input level Log. stage 9 output level
Log. stage 10, Pin 3, 9 Log. stage 10, Pin 13, 21	- 3 dB + 7dB	Log. stage 10 input level Log. stage 10 output level

Table 6-22 Level table for checking the logarithmizer signal path

Important: The above test checks only the signal path of the logarithmizer (10 x 10 dB log. amplifiers). A rectifier is connected after each log. stage; this converts the analog 21.99 MHz (AC) output signal form the amplifier into a DC signal. The above test does not check the function of the rectifiers (see circuit description, section 9). If the signal path is error-free, the rectifiers and the adder circuit should be checked.

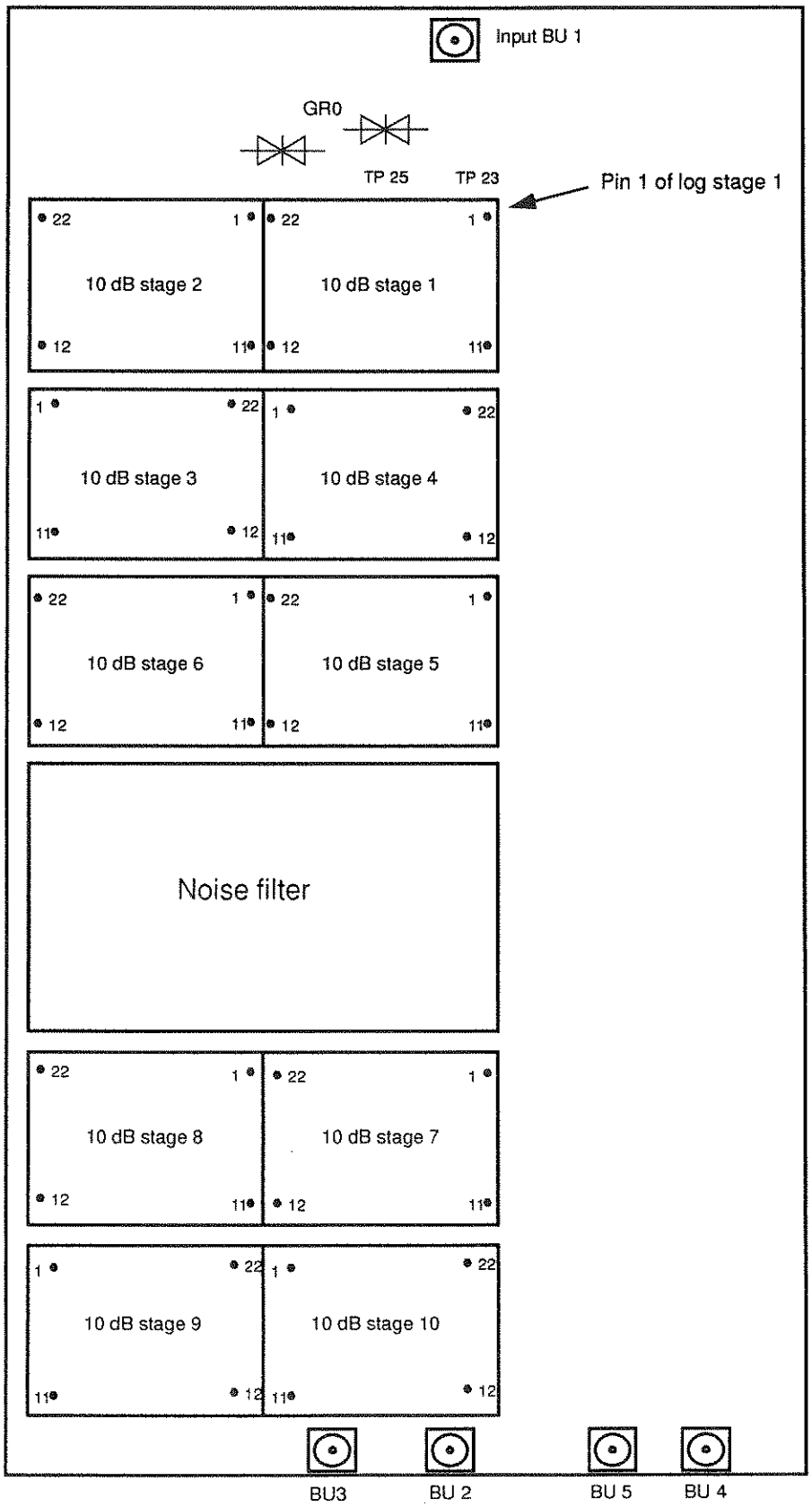

Fig. 6-6 Layout of log. stages and test points on the logarithmizer board (simplified diagram)

6.2.3 IF converter [2101-O] (series A +B)

Operating and bias voltages

The voltages should be measured in the order given below unless there are good reasons for not doing so:

Supply voltages

Voltage	Test point	Value	Tolerance	Notes
+12 V	TP5	+11.6 V	± 0.2 V	
-12 V	TP6	-11 V	± 0.2 V	
+6.5 V	TP7	+6.4 V	± 0.2 V	Only required for ADC
-6.5 V	TP8	-6.4 V	± 0.2 V	Only required for ADC
+5 V	TP4	+5 V	± 0.2 V	

Table 6-23 Supply voltages on the IF converter board

Checking the analog signal path

Unplug the plug from 9Bu1 (connection to logarithmizer) and feed a DC voltage of about 2.5 V into TP1.
If +2.5 V is fed in (check voltage at TP1), the following values apply for the signal path:

Test point	Value
IC2.2	+2.5 V
IC7.8	+2.5 V
IC13.6	+2.5 V
TP2	-1 V ± 50 mV
TP3	+2.5 V ± 50 mV

Table 6-24 Analog signal path test points on the IF converter board

Checking the 8-bit converter

The following signals must be present at the 8-bit converter (IC 16) for correct operation:

Test point	Value	Notes
IC16.17	20 MHz digital signal	Clock, HCMOS level
IC16.26	-2 V ± 50 mV	Reference voltage, derived from IC11, generated by IC12/T300
IC16.27	-1 V ± 50 mV	Center of reference voltage
IC16.12, 28	+5 V	+VCC, digital control signal for output format

Table 6-25 Signals at the IF converter 8-bit converter (IC 16)

Test point	Value	Notes
IC16.23	-1 V ± 50 mV	Analog input
IC16.6,10	+5 V ± 0.2 V	VCC
IC16.7,8,9	-5 V ± 0.2 V	VEE

Table 6-25 Signals at the IF converter 8-bit converter (IC 16)

Checking the 16-bit converter

The following signals must be present at the 16-bit converter (IC 20) for correct operation

Test point	Value	Notes
IC20.20	4 MHz digital signal	Main clock, HCMOS level
IC20.1	40 kHz digital signal	Converter clock, HCMOS level
IC20.28	+5 V ± 50 mV	Reference voltage generated by IC19, derived from the 8-bit ADC reference voltage
IC20.29	+5 V ± 50 mV	Reference output, same as IC20.28
IC20.26	2.5 V	Analog input
IC20.11	+5 V ± 0.2 V	VCC digital
IC20.25	+5 V ± 0.2 V	VCC analog
IC20.36	-5 V ± 0.2 V	VEE digital
IC20.30	- 5V ± 0.2 V	VEE analog
IC20.37	40 kHz digital signal	End of track
IC20.39		Serial clock; 16 x 1 MHz clock pulses every 25 µs (40 kHz)
IC20.40		Serial data
IC20.21..24,32..35		Digital control inputs. The measurement mode states are:
IC20.21	H	
IC20.22	H	
IC20.23	H	
IC20.24	L	
IC20.32	L	
IC20.33	H	
IC20.34	H	
IC20.35	L	

Table 6-26 Signals at the IF converter 16-bit converter (IC 20)

Checking the RMS rectifier

The RMS rectifier is tested with a DC voltage. Unplug the plug from 9Bu1 (connection to logarithmizer) and feed a DC voltage of about 2.5 V into TP1. If +2.5 V is fed in (check voltage at TP1), the following values can be measured with a voltmeter:

Test point	Value
IC9.6	0.35 to 0.45 V
IC10.7	-0.75 to -0.7 V
IC8.7	2.5 V (same as TP1, ± 10 mV
IC15.2	0.35 to 0.45 V
IC15.6	1.3 to 1.4 V
IC8.2	2.7 to 2.8 V
IC8.1	5.5 to 6.5 V
IC10.2	0.35 to 0.45 V

Table 6-27 Test points for checking the RMS amplifier

6.2.4 IF converter [2101-O] (series C onwards)

The 8-bit converter (IC 16) is replaced by a 10-bit converter (IC 16) in instruments from series C onwards. There are some minor changes in the circuit compared with series A + B; these are unimportant for troubleshooting. The same procedure can be used as described under "Checking the 8-bit converter" on page 6-25 in section 6.2.3.

6.2.5 Calibration generator [2101-N]

The following instructions are for a rapid, systematic check. For precise checking of the calibration level, refer to section 7.7.4 ("Calibration generator (11)[2101-N]").

Operating voltages

Check the operating voltages for the calibration generator board against the following table:

Test point	Value	Notes
TP14	+12 V	If one of these voltages is missing, check the AC PSU
TP18	-12 V	
TP16	+6.5 V	
TP19	-6.5 V	
TP20	+5V	Voltage looped-through to measurement unit controller, not used by calibration generator
TP17	+5V	Voltages "generated" on-board. Check the area around IC40, T400, T401, GL401 if there is a fault.
TP15	+10 V	

Table 6-28 Operating and supply voltages on the calibration generator board

Checking the calibration synthesizer (PLL)

Test point	Value	Notes
TP4	20 MHz	Reference frequency, HCMOS level
TP3	1.818 MHz	Reference frequency divided by 11. If this frequency is missing, check IC7. Check that : P0 = 0, P1 = 1, P2 = 1, P3 = 0; in the event of a fault, IC8 is not initialized correctly, check the computer bus.

Table 6-29 Table for checking the calibration synthesizers

Checking the VCO

The calibration generator must be switched on to check the VCO (GL101 off, anode at 0).

The calibration source cannot be permanently activated from the software menu. The following procedure should be used:

Activating the calibration source: Connect an external keyboard to the SNA. Switch on and wait for the measurement screen to appear. Then press <ALT> and <F10> simultaneously (SNA switches to DOS mode). Enter "SET CALOUT=1" from the keyboard and press return to confirm. Now enter "K" followed by return to re-start the SNA measurement program. Select AUTO CAL OFF in the CAL menu of the D.U.T. The calibration source can now be activated/ deactivated from this menu (CAL. OUTPUT: ACTIVE/INACTIVE).

Unplug the shorting link 1.2-1.3 and use it to close link 1.1-1.2 (U_{VCO} = 0 V):

Frequency at TP2: 40 to 42 MHz
at TP6: 20 to 21 MHz

Remove the shorting link completely (U_{VCO} = -12 V):

Frequency at TP2: 64 to 70 MHz
at TP6: 32 to 35 MHz

VCO slope

To check the VCO slope, remove shorting link (BR1) completely and remove R110 (otherwise TP1 is pulled down to -12 V. Feed the appropriate DC voltage (see table) in at TP1 and measure the VCO frequency. The following values must be obtained.

Frequency (TP6)	$U_{VCO} = U_{TP1}$
17 MHz	+2.2 V ± 0.2 V
20 MHz	+0.1 V ± 0.2 V
22 MHz	-1.2 V ± 0.2 V
24 MHz	-2.7 V ± 0.2 V
27 MHz	-5.0 V ± 0.3 V

Table 6-30 Table for checking the VCO slope

If no frequency can be measured at TP2, the oscillator is not running. Check the potentials at T100 to T102 and check transformer UE1 for short circuits.

Checking the level control

Unplug the shorting link from 2.1-2.2 and use it to link 2.2-2.3. This feeds the maximum level to the output (BU12, BU13). This level is approx.-23 dBm (50 Ω) if the board has been adjusted.

Under the above condition, the following DC working points apply (see table 6-31).

Test point	Value	Notes
IC20.8	-9.2 V	**Note:** The "pip" on IC20 indicates pin 12
IC20.9	-10.0 V	
IC20.4,7	-6.2 V	
IC20.5,6	-1.0 V	
IC20.2	-5.7 V	All voltages are approximate (± 0.2 V)
IC20.3	-6.5 V	
IC20.1,10	-5.2 V	
IC20.11,12	-4.0 V	
GL200	-6.4 V	± 0.5 V

Table 6-31 Table for checking the level control

Checking the FM demodulator

Feed a stable frequency, e.g. 10 MHz from instrument back panel, into the SNA input. Set the SNA as follows:

FCENT 10 MHz
FSPAN 5 MHz
RBW 3 MHz
SEEP(RUN) MAN TUNING

First set f = FCENT and check the demodulator input signal at TP11:
f = 21.99 MHz
u = approx. 200 mV_{pp}

The signal should be 2 V_{pp} at IC 31.1 and 4 with a phase difference between the signals of 180.

Check the DC voltage levels at IC31 against the following table:

Test point	Value
IC31.8,10	+4V
IC31.5	-10.5 V
IC31.6,12	+8.2 V ± 0.3 V

Table 6-32 DC voltage levels at IC31

Connect a DVM to TP12 (= IC31.12). Stepwise increase in the frequency (manual tuning) by 10 kHz should increase the voltage by approx. 200 mV for each step. Reducing the frequency should result in voltage drop.

Final values (approx.):

12 MHz: 11.1 V
8 MHz: 4.8 V

6.3 Troubleshooting the controller

6.3.1 AT CPU

This service manual does not support troubleshooting of the AT CPU to component level. We do not recommend repairing this board, due to the complex SMD chip set components.
The AT CPU runs a self-test of its computer core immediately after switch on (BIOS TEST, see section 4). If a fault in the AT CPU is detected during this test, the module should be replaced. Special PC test programs, such as "Checkit" can be used for further checking. These provide comprehensive tests for the interfaces, RAM and other CPU peripherals. Such programs are available from PC accessory shops.

6.3.2 Memory [2101-AF] (series A - E)

Supply voltages

The supply voltages are fed from the interface board via 3 50-way ribbon cables(P1,P2 and P3).

The following voltages must be present on the memory board:

Test point	Value	Notes
e.g. D701 (anode)	+5 V	+5 V ± 5%; I = 400 mA
Q701 (emitter)	+12 V	+12 V ± 5%; I = 60 mA Program voltage for Flash-ROMs

Table 6-33 Memory board [2101-AF] operating voltages

Effects of memory board errors

Error during BIOS test (e.g. test aborted)

As the memory is directly connected to the AT bus, a fault on the board can affect data and address communications via the bus (bus conflict).

To check whether the memory board is the cause of a bus conflict, decouple the memory board from the bus system by setting the control signal "NDOE" = HIGH. This is done by removing (17)U203. The memory board then only passes the bus from the AT CPU to the interface board and provides the supply voltage for the AT CPU.

Important: If (17)U203 is removed to prevent the AT CPU from accessing the memory board, the operating system and instrument software will not be loaded when the instrument is switched on. Prepare a system disk (operating system) beforehand. The instrument can also be booted from the service disk.

Operating system/instrument software does not load

If the operating system system and/or the instrument software is not loaded after switching on but the BIOS test is completed successfully, a fault on the memory board (17) is likely, since both the operating system and the instrument software are stored in the Flash-ROMs on this board.

To determine which of the Flash components is defective, the instrument software should be re-programmed into the Flash-ROMs (see "Installing the Instrument Software / Updating Software" on page 4-14). If an error occurs during deletion and re-programming, the program indicates the

address which caused the error. Use table 6-34 to determine the pair of Flash ROMs (16-bit data) for the given address. It is not possible to determine which of the two Flash ROMs thus identified is faulty.

Important: The addresses are assigned to different components, depending on whether 1 Mbit or 2 Mbit Flash ROMs are fitted.

Hexadecimal address	Memory type	Components
580 000 - 5BF FFF	SRAM, battery-buffered	U300, U303, U205, U207
5C0 000 - 5FF FFF	SRAM, battery-buffered	U301, U304, U205, U207
920 000 - 920 3FF	Flash ROM VPP control signal	U204
921 800 - 921 8FF	Memory status port control signal	U204
When fitted with 1 Mbit memory components:		
940 000 - 97F FFF	Flash; correction value memory	U512, U513, U205, U207
C80 000 - CBF FFF	Flash; program memory	U510, U511, U205, U207
CC0 000 - CFF FFF	Flash; program memory	U508, U509, U205, U207
D00 000 - D3F FFF	Flash; program memory	U506, U507, U205, U207
D40 000 - D7F FFF	Flash; program memory	U504, U505, U205, U207
D80 000 - DBF FFF	Flash; program memory	U502, U503, U205, U207
DC0 000 - DFF FFF	Flash; program memory	U500 U501, U205, U207
E00 000 - E3F FFF	Flash; program memory	U412, U413, U205, U207
E40 000 - E7F FFF	Flash; program memory	U410, U411, U205, U207
E80 000 - EBF FFF	Flash; program memory	U408, U409, U206, U208
EC0 000 - EFF FFF	Flash; program memory	U406, U407, U206, U208
F00 000 - F3F FFF	Flash; program memory	U404, U405, U206, U208
F40 000 - F7F FFF	Flash; program memory	U402, U403, U206, U208
F80 000 - FBF FFF	Flash; program memory	U400, U401, U206, U208
0E0 000 - 0EF FFF	Flash; extended BIOS	U400, U401, U206, U208
When fitted with 2 Mbit memory components:		
940 000 - 9BF FFF	Flash; correction value memory	U512, U513, U205, U207
9C0 000 - A3F FFF	Flash; program memory	U508, U509, U205, U207
A40 000 - ABF FFF	Flash; program memory	U506, U507, U205, U207
AC0 000 - B3F FFF	Flash; program memory	U504, U505, U205, U207
B40 000 - BBF FFF	Flash; program memory	U502, U503, U205, U207
BC0 000 - C3F FFF	Flash; program memory	U500 U501, U205, U207
C40 000 - CBF FFF	Flash; program memory	U412, U413, U205, U207
CC0 000 - D3F FFF	Flash; program memory	U410, U411, U205, U207
D40 000 - DBF FFF	Flash; program memory	U408, U409, U206, U208
DC0 000 - E3F FFF	Flash; program memory	U406, U407, U206, U208

Table 6-34 Addresses and corresponding components on the memory board [2101-AF]

Hexadecimal address	Memory type	Components
E40 000 - EBF FFF	Flash; program memory	U404, U405, U206, U208
EC0 000 - F3F FFF	Flash; program memory	U402, U403, U206, U208
F40 000 - FBF FFF	Flash; program memory	U400, U401, U206, U208
0E0 000 - 0EF FFF	Flash; extended BIOS	U400, U401, U206, U208
Memory components U510 and U511 are not fitted		

Table 6-34 Addresses and corresponding components on the memory board [2101-AF]

Correction tables deleted after switching off

After switching on and booting of the operating system, the message

General failure reading drive B
Abort, Retry, Fail?

is displayed.

The memory board is fitted with 512 kByte of battery-buffered SRAM (U300, U301, U303 and U304) in which the correction data for the frequency response and logarithmizer are stored (see "Installation of compensation (correction) data" on page 7-11). Data loss can be caused by a defective memory component, a faulty battery (BT1) or a fault in U306 and its associated circuitry (Q300, R301, R302, R303).

Measure the following voltages with the instrument switched off:

Test point	Value	Notes
U306 Pin1	> 2.2 V	Battery voltage when connected up
TP308, U306 Pin 2	> 2.1 V	Instrument switched off. If faulty, test U306 and associated circuitry
U300,301,303,304 Pin 12	> 2.1 V	VCC1 for SRAM components 2.1 V - 3.7 V instrument switched off approx. 5 V instrument switched on
TP 309	HIGH	Status signal NLOW_BAT, LOW if battery voltage < 2.2 V

Table 6-35 Test points for checking the SRAM buffer voltage on the memory board

Error writing to Flash ROMs

If errors occur during write operations to the Flash ROMs, the program voltage "generated" on the board may be faulty. During delete and programming operations, 12 V ± 5% must be present on pin 1 of the Flash components. The same voltage must be present at the emitter of Q701. The SVPP signal (MP700) should also be checked.

SVPP (MP700) HIGH: Program voltage for Flash ROMs is on. VPROG = +12 V

SVPP (MP700) LOW: Program voltage for Flash ROMs is off. VPROG = +5 V

6.3.3 Keyboard [2101-AJ]

Supply voltages

The supply voltages are fed via ribbon cable (MT3) from the interface board via the keyboard controller board.

The following supply voltages can be measured on the keyboard:

Test point	Value	Notes	
e.g. IC1,IC3, IC4 Pin 20	+5 V	+5 V ± 5%	
MT3.6	+12 V	+12 V ± 5%	These voltages are not required on this board
MT3.8	-12 V	-12 V ± 5%	

Table 6-36 Power supply voltages for the keyboard [2101-AJ]

Faulty key

The control of the key matrix can be checked with an oscilloscope connected to the outputs of IC2. Individual rows are driven cyclically with a LOW signal. Check the inputs of IC1 to see if pressing a key generates the corresponding LOW signal at the input of IC1 for the row being driven.

Faulty LED

The LED states can be measured at the outputs of IC3 and IC4. HIGH means that the LED should be onl The individual LEDs can be switched on and off by changing the operating mode. If the contents of latches IC3 and IC4 remain constant, the fault is in the latch drive, the data bus or in the latches themselves.

6.3.4 Keyboard controller [2101-AL]

Supply voltages

The supply voltages for the keyboard controller are derived from the interface board and fed in via ribbon cable (MT3).
The following voltages can be measured on the keyboard controller board:

Test point	Value	Notes	
ST6.3	+5 V	+5 V ± 5%	
ST6.5	+12 V	+12 V ± 5%	These voltages are not required on this board. They are fed to boards (20) and (21) via ST5.
ST6.7	-12 V	-12 V ± 5%	

Table 6-37 Supply voltages for the keyboard controller [2101-AL]

Keyboard controller function groups

The keyboard controller can be split into the following function groups for troubleshooting:

No.	Function group	Components in function group
1	Computer core	IC2, IC3, IC6, IC15.6, Q1
2	Built-in keyboard controller	IC8
3	External keyboard interface	IC13.1, IC13.2, IC13.5, IC13.6
4	Output to external keyboard	IC13.3, IC13.4, IC14.1, IC14.2
5	Input from external keyboard	IC7, IC8, IC9, IC10, IC11, IC12, IC14.3-5
6	Rotary control controller	IC7, IC8

Table 6-38 Keyboard controller function groups and their components

Fault location

Error message: "Keyboard error"

If this error message is displayed during boot-up, the fault is likely to be in function group 1 or 3.

Internal keyboard does not work, external keyboard works properly

Function group 2 or keyboard printed circuit board is defective.

External keyboard does not respond

If the external keyboard LEDs do not respond, the fault is likely in function group 4.

External keyboard does not work, internal keyboard works properly

Function group 5 or external keyboard is defective.

Rotary control does not respond

Function group 1 or 6 is defective.

6.4 Troubleshooting the synthesizer OD-11

6.4.1 Standard frequency oscillator

The 10 MHz sinusoidal signal from the standard frequency oscillator ("10MHZRF") can be output to an oscilloscope from St101 Pin 9. The peak value is > 0.7 V. It is also present as a FACT signal at IC15. Signals synchronous with the standard frequency oscillator only appear at outputs "20MHZ_1" to "20MHZ_3" (50BU 3 to BU 5) and "10MHZ_RW" 50BU 2 (BU13 [64] on the instrument back panel) if the 400 MHz PLL is locked, as these output signals are derived from the 400 MHz oscillator by division (see section 6.4.3.3, "Timebase 2 (400 MHz PLL)" on page 6-37). The frequency accuracy of the standard frequency oscillator can be measured within the framework of the synthesizer module using e.g. a frequency counter. The stability of the counter directly affects the reliability of the measurement.

6.4.2 YIG oscillator

The general function of the YIG oscillator can be checked as follows:
Connect the YTO RF output BU10 or the synthesizer RF output "1.LO" [71] (on the instrument back panel) to a spectrum analyzer and measure the signal. Open wire link (50)S1 and close switch S3. This interrupts the control loop (S1) and limits the gain of the PI controller (IC26) to a finite value (S3). This setting drives the YTO to the lower limit (2.8 GHz if the lower YTO limit is properly adjusted).

If this lower limit does not result, the YTO can be tuned directly by connecting a DC source between contacts TC+ and TC- of the YTO (disconnect and feed in at H011 and H04). Check the YIG oscillator against the following table; the actual frequency values may differ slightly due to component tolerances in the YIG oscillator.

The YTO frequency is actually governed by the current through the tuning coil.

If the YIG oscillator is not faulty, check the signal path between (50)S1 Pin3 and TP22 (see section 6.4.4.1 on page 6-38).

Frequency	U (H011 - H04)	Frequency	U (H011 - H04)
3.1 GHz	1.9 V	5.5 GHz	3.5 V
3.5 GHz	2.2 V	6 GHz	3.9 V
4 GHz	2.5 V	6.5 GHz	4.2 V
4.5 GHz	2.9 V	7 GHz	4.5 V
5 GHz	3.2 V	7.5 GHz	4.8 V

Table 6-39 YTO frequency as a function of control voltage

Note: If the YIG oscillator is defective, it must be replaced. After replacement of the YIG oscillator, the frequency response of the instrument must be re-determined as the oscillator output level affects the instrument frequency response (see section 7.5.1).

6.4.3 Timebase/YTO driver [2101-B]

6.4.3.1 Power supply

Supply voltages

The supply voltages for the timebase/YTO driver board [2101-B] are fed in directly from the AC PSU (1) via plug (50) ST 13. Check the voltages against the following table.

Test point	Value
IC41.7	+12 V
IC42.7	+6,5 V
IC43.4	-12 V
IC44.4	-6.5 V
L49	+18 V

Table 6-40 supply voltages for board [2101-B]

Central filter (DC-PREFILTER)

The ± 12 V and ± 6.5 V supply voltages are filtered by active OP filters.

Checking the OP filter circuits

An oscillograph of (e.g.) the +12 V filter control voltage at IC41 Pin 6 (same applies for -12 V and ± 6.5 V) shows a DC voltage of ≈ +1 V. This voltage derives from the residual current from electrolytic capacitor C143 through R265. The superimposed AC signal is the interference voltage on the +12 V line. If control is correct, approximately the same potential (ground) should be present at IC41 Pins 2 and 3. The filter function can be tested by feeding in an interference signal via a transformer.
The DC drop across L41 and R266 is typically 0.2 V.

Filter timebase

The controller function of the OP filters can be checked by approximate equality of the potentials at the positive and negative OP inputs:
The DC voltages at IC8 Pins 3 and 2 are +5 V and at IC9 Pins 3 and 2 they are -5 V. Check that the base-emitter voltages of the transistors is ≈ 0.7 V.

The following voltages are "generated" by filtering the timebase.

Test point	Value
L16/C58	+10.5 V
L13/C52	+5 V
L12/C47	-5.2 V
L17/C61	-10.5 V
L49	+18 V

Table 6-41 Voltages "generated" on the timebase filter board

DC CONTROL/Reference voltage generation

The function of the "-5 VYTO" and "+15 VYTO" reference voltage generators can be checked by measuring the OP input and output voltages. IC40 Pins 2 and 3 should have approximately equal potentials of +5 V with ≈ 12 V at the output. IC29.1 Pins 2 and 3 should both be at approximately ground potential. IC29.1 Pin 1 as well as IC29.2 Pins 5 and 6 should be at approximately -5 V.

6.4.3.2 Timebase 1 (10 MHz external synchronization control circuit)

A 10 MHz signal fed into the "Fext10MHz" input (10 MHz input [62] on the instrument back panel) closes the slow PLL (loop bandwidth ≈ 14 Hz) for external synchronization. This can be verified by a HIGH level at IC4 Pin 8 ("external level") or the equality of the potentials at IC4 Pins 6 and 7. When the loop is locked, PI controller IC6 Pins 6 and 5 are at approximately the same level of ≈ +2.7 V and OP output IC6 Pin 7 is driven linearly. In addition, the two 10 MHz signals at IC31 Pins 3 and 11 are synchronous with a small phase shift (≈ 30 degrees); see also section 6.4.1 on page 6-35. The "external level" AND gate (IC7 Pin 2) and the "Phase meter lock signal" (High level at IC7 Pin 8) produce the status signal "EXT_SYNC", St9 Pin 18. The function of the second status signal, "OFEN_WARM" is checked by measuring the voltage drop across R14 and by calculating the current drawn by the heater for the standard frequency oscillator. Comparator IC6.1 should flip to HIGH for currents of ≈ 250 mA.

6.4.3.3 Timebase 2 (400 MHz PLL)

The function of the 400 MHz PLL can be tested by checking that the voltages at PI controller IC35 Pins 3 and 2 are approximately equal (≈ 2.75 V). The control voltage at IC35 Pin 6 should be between 4 and 6 V. The frequency divider chain is checked by tracing the signal path. A 400 MHz sinusoidal signal at ≈ 7 dBm appears at connector MT65.The 10:1 ECL divider output IC3 Pin 11 yields a 40 MHz FACT level; the first 2:1 divider IC12.1 Pin 5 yields a 20 MHz FACT level, with the 10 MHz FACT level appearing finally at 2:1 divider IC12.2 Pin 9. This latter is fed into the comparator input of phase meter IC32.1 Pin 3. All signals have a duty cycle of 1:1. The timebase reference signals "20MHZ_1" to "20MHZ_3", the 20 MHz ECL pulse to the synchronous divider/phase meter, and the 10 MHz signal "10MHZ_RW" are all divided down from the 400 MHz oscillator and are thus only synchronous with the standard frequency oscillator when the 400 MHz PLL is locked. The PLL can be disconnected at link BR4 for manual tuning of the 400 MHz oscillator (a variable DC source is connected to BR4 Pin 1).

6.4.4 400 MHz oscillator [2101-F]

The frequency of the 400 MHz LC oscillator can be offset by opening solder link BR4 and connecting a variable voltage source to BR4 Pin 1. Connect the RF output socket BU7 "400MHZ" to a frequency counter for measurement. The oscillator should be tunable from about 397 MHz to 403 MHz for an input voltage of ≈ 3 to 9 V, with a slope of ≈ 1 MHz/V in the working range (≈ 4...6 V). The level at RF output BU7 "400MHZ" settles at ≈ 0 dBm/50 Ω.

Typical circuit working points

Test point	Value	Notes
T403 /S	≈ +1.3 V	Source connection S (= -Ugs)
HO63	≈ -4.3 V	
T402 /E	≈ -0.3 V	Emitter, transistor T402
T404 /E	≈ -0.5 V	Emitter, transistor T404
T401 /G1	≈ -0.6 V	Gate 1 G1 of T401
T401 /S	≈ -0.4 V	Source connection S (Ug1s = -0.2 V)
T401 /G2	≈ 3.8 V	Gate 2 G2 of T401 (Ug2s ≈ +4.2 V)

Table 6-42 Typical working points for the 400 MHz oscillator

6.4.4.1 Regulator/YTO driver

The individual components of the regulator/YTO driver can be checked by measureemnt with the control loop disconnected. Open wire link S1 and connect an AC voltage source (+ signal to S1 Pin 3, - signal to S1 Pin 1). If an AC signal with F = 20 kHz and 100 mVpp is fed in and the D.U.T. is set as below, the signal path measurement values in table 6-43 will be obtained.

D.U.T. settings

FSPAN	0 Hz
RUN	MAN

Test point	Value
S1 Pin 3	100 mVpp
IC22.7	100 mVpp
IC22.1	100 mVpp
TP2	200 mVpp
TP12	200 mVpp
TP22	150 mVpp

Table 6-43 Test points in the YTO diver signal path

Check the signal path in this setting with a control bandwidth setting of 10 kHz (default). The signal path can be checked at the other control bandwidths in the same way.

Note: Exact settings of the control bandwidth using the analog switch (control signals DS(0) to DS(15)) for switching through a specific path must be made via the DSP of the synthesizer controller. This can only be done in specially equipped service centers as special equipment is required.

YTO frequency limiter

The YTO frequency limiter IC38.1 to IC38.4 must be inactive when the YTO current is within the frequency range (1st LO in the range 3 to 8 GHz), i.e. a negative potential of <0 V must be present at IC38.2 Pin 7 (upper limit control output) as well as at IC38.3 Pin 8 (lower limit control output).

YTO synchronization monitor

In parallel with the controller signal path, the arithmetic mean of the phase meter output at test point TP13 is measured by double-way rectifier IC17.2 and IC17.4, and fed to Schmitt trigger IC17.3. This generates the status signal "YTO_SYNC" indicating synchronicity in CW operation (FSPAN = 0).
The circuit function can be tested by unplugging the contacts BU11 "PD+" and BU12 "PD-" and feeding in a (e.g.) 1 kHz sinusoidal signal into BU12. The arithmetic mean Ua = 2*Up/π (Up is the peak value set at TP13) appears at IC17.4 Pin 14 or IC17.3 Pin 9. The Schmitt trigger should trigger as per its characteristic (on level Uon ≈ 120 mV, off level Uoff ≈ 60 mV).

6.4.5 Synchronous divider/Phase meter [2101-K]

Note: Specific troubleshooting is only possible on this board if the gate array (PLLIA) can be programmed. This requires special equipment and can therefore only be carried out in sppecially equipped service centers.

6.4.6 Synthesizer controller [2101-A]

6.4.6.1 Controller filters

The active OP filters which operate in addition to the central filters are identical in principle to those described in the section "Filter timebase" on page 6-36 (q.v.).

6.4.6.2 Control

The 20 MHz clock for the DSP (digital signal processor) is derived from the timebase (contact HO18 connected to HO17). It can be output to an oscilloscope from IC1 Pin 127 (link HO17-HO18).

Caution!

The DSP can be destroyed if the clock signal is missing.

For AT bus address decoding, first check the synthesizer base address set by BR3 to BR8 and BR11. Links BR8 to BR5 and BR11 must be closed, BR4 and BR3 must be open.

Interrupt and clock generation

To generate the interrupt and clock periods, a 10 MHz signal "CLK_10MHz" is fed to IC 34 Pin 10 as a divider input signal. The following signals are produced: at output "Q2" IC34 Pin 7 2.5 MHz, at "Q4" IC34 Pin 5 625 kHz (1.6 s) and at "Q12" IC34 Pin 1 2.44 kHz (409.6 µs). The long-term interrupt "INTB" IC33 Pin 3 ("Q13") is 3.36 sec (≈ 300 mHz).

Address decoding

Specific troubleshooting of the address decoding requires special control software and equipment and can therefore only be carried out in sppecially equipped service centers.

Checking the interfaces

Specific troubleshooting of the 8-bit output ports IC19, IC30 and the 8-bit input port IC18 requires special control software and equipment and can therefore only be carried out in sppecially equipped service centers.

6.4.7 SHF pre-divider module

The SHF pre-divider module is fed with the YTO signal "FYTO" from socket (50)BU10 in the frequency range 3.1 to 8 GHz. The output signal must be this signal divided by 16.

The SHF pre-divider module can be tested at the lower limit frequency of the YTO. To drive the YTO to the lower limit, proceed as follows:

Open wire link (50)S1 and close switch S3. This interrupts the control loop (S1) and limits the gain of the PI controller (IC26) to a finite value (S3). This setting drives the YTO to the lower limit (2.8 GHz if the lower YTO limit is properly adjusted). Connect the YTO RF output BU10 or the synthesizer RF output "1.LO" [71] (on the instrument back panel) to a spectrum analyzer and measure the signal. Then measure the output signal of the SHF pre-divider module.
The results should be as below:

SHF pre-divider module input
Lower limit: FYTO approx. 2.8 GHz

SHF pre-divider module output
FYTO /16 = 175 MHz (FYTO signal divided by 16)

If the input frequency divided by 16 is not measureable at the output of the SHF pre-divider module, the complete SHF pre-divider module should be replaced. The information in section 2.3 should be observed.