7 Adjustment instructions

7.1 Introduction

After repairing a circuit board or module, follow the relevant adjustment instructions (see section 7.2 on page 7-2). Circumstances will determine whether the entire section or only a part of it need to be followed. In case of doubt, perform all the adjustments given in the section. If circuit boards or modules are replaced, the instructions as listed under "List of adjustments required after replacing circuit boards or modules" (see section 7.3 on page 7-4) should be carried out.

Microwave modules and waveguides must not be repaired. They should be replaced as complete units.

The adjustments listed in section 7.5 can only be performed in specially-equipped Service Centers.

Note: When making adjustments, only those screening can covers necessary for accessing the adjustment controls should be removed. In some cases, the covers must not be removed for adjustments. Covers with holes allowing access to the controls should be used. The instrument should have reached thermal equilibrium and be within the nominal ranges of use for the influence quantities when adjustments are being made.

Adjustments fall into the following categories:

- Check sum correction of hardware status for certain circuit boards (see section 7.4)
- Recording of correction data for the measurement section and synthesizer (see section 7.5)
- Manual adjustments (see section 7.6 ff.)

7.2 List of all adjustment controls

Circuit diagram no.	Adjustment control	Notes	Adjustment instructions in section
1	P1	Overtemperature cutout	7.10.2
2	R54	Reference tuning voltage, 4 GHz VCO	7.6.2
	R20	PLL breakthrough frequency	7.6.2
5	P101	External mixer bias	7.6.1
	P102	External mixer bias	7.6.1
	P103	-	-
6	L1	400 MHz oscillator adjustment	7.6.3
	P1	Frequency converter level adjustment	7.6.3
	R117	Frequency converter level adjustment	7.6.4
7	5 x C86	LC circuit band center frequencies	7.7.1
	5 x P81	LC circuit insertion loss	7.7.1
	5 x C602	Crystal stages stop-band attenuation	7.7.1
	5 x L601	Crystal stages pass-band attenuation	7.7.1
	P7	30 kHz crystal bandwidth	7.7.1
	P8	Bypass path level adjustment	7.7.1
	P4	IF single gain 1 dB	7.7.1
	P2	IF single gain 2 dB	7.7.1
	P6	IF single gain 4 dB	7.7.1
	P5	IF single gain 8 dB	7.7.1
	P1	IF single gain 16 dB	7.7.1
	P3	IF single gain 16 dB	7.7.1
8	P800	+5 V regulator	7.7.2
	P503	Log amplifier working point	7.7.2
	P501	Rectifier threshold voltage (log.)	7.7.2
	P500	Current source bias voltage	7.7.2
	P400	Video amplifier offset	7.7.2
	P401	Adder stage zero point (offset)	7.7.2
	P502	Rectifier threshold voltage (lin.)	7.7.2
	L400, L401, L402	10 MHz video filter	7.7.2
	C227	10 MHz noise filter (symmetry)	7.7.2
	L208	400 kHz noise filter (center frequency)	7.7.2
	10 x P151	10 dB log. amplifier gain	7.7.2

Table 7-1 List of all adjustment controls

Circuit diagram no.	Adjustment control	Notes	Adjustment instructions in section
9	P300	Bipolar offset	7.7.3
	P303	8-bit linearity	7.7.3
	P400	16-bit gain	7.7.3
	P401	16-bit offset	7.7.3
	P301	Overall offset	7.7.3
	P302	Overall gain	7.7.3
	P200	RMS value meter offset	7.7.3
11	P1	External calibration level	7.7.4.1
	P2	Internal calibration level	7.7.4.1
	C317	FM demodulator center frequency	7.7.4.2
	C301	Search demodulator center frequency	-
21	P1	Rotary control offset	7.9.1
50	P101	10 MHz standard frequency	7.8.1
	P2	Upper YTO frequency limit	7.8.2
	P3	Lower YTO frequency limit	7.8.3
	P4	Offset preset (100 Hz control bandwidth)	No adjustment reqd.
	P5	Lower YTO freq. limit (external YTO)	No adjustment reqd.
	P6	Gain, external YTO	No adjustment reqd.
	P7	Gain for internal sinusoidal sweep	No adjustment reqd.
	L406	400 MHz oscillator LC resonator adjustment	7.8.4
51	P1	ADC offset	No adjustment reqd.

Table 7-1 List of all adjustment controls

7.3 List of adjustments required after replacing circuit boards or modules

Note: If an adjustment control is indicated in the column "Adjustment required" the adjustment instructions pertaining to this control in the section indicated must be carried out. If the column indicates a section number only, the entire section including any sub-sections should be followed.

Circuit board or module replaced		Adjustment required	
Circuit board or circuit diagram no.	Name	Adjustment control	Adjustment instructions in section
CG44 (Gossen)	Power supply		7.10.1
2101-BD	Voltage distribution		7.10.2
2101-BE	24/12 V converter		No adjustment
(2), (3), (4),	Any module in the signal path from the input socket to (2) P/J204, including all waveguides. Also YIG filter (3)FI1and input socket	(6) P1, (6) R117	7.6.3, 7.6.4, 7.5.1
2 P38	RF adapter (Rosenberger)		7.5.1
2 AT1	Step attenuator		7.5.1
2 FL1	8 GHz low-pass filter (Suhner)	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
2 K1 2101-ZH (2 DX1)	Coaxial relay (series A+ B) Diplexer (from series C on, replaces coaxial relay 2K1)	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
2101-ZA	Integration Band 0, complete (series A through E)	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
2101-ZA1	Integration Band 0, complete (series E onward)	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
2101-ZC	Fundamental mixer, complete	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
2101-ZE	IF switch, complete	(6) P1, (6) R117	7.5.1, 7.6.3, 7.6.4
3FL1	YIG filter (ferretec)		7.5.1, 7.5.3
2101-AS1	YIG filter controller		7.5.3
2101-AR	Input section controller		7.6.1
6 IF-1	422 MHz bandpass (Interdigital filter)	(6) P1, (6) R117	7.6.3, 7.6.4
2101-X[1]	422/22 MHz converter	(6) P1, (6) L1	7.6.3
2101-Y* 2101-7023.538 (series A + B)	422/22 MHz/10 kHz converter (for instruments fitted with "narrow bandwidth" option)	(6) R117 (6) C28, C31, C32	7.6.4
2101-Y* 2101-7023.554 (series C on)	422/22 MHz/10 kHz converter (for instruments fitted with "narrow bandwidth" option)	(6) R117 (6) C28, C31, C32	7.6.4

[1] 2101-X or -Y fitted depending on version (2101-Y for narrow bandwidth option)

Table 7-2 List of all adjustments required after replacing circuit boards or modules

Circuit board or module replaced		Adjustment required	
Circuit board or circuit diagram no.	Name	Adjustment control	Adjustment instructions in section
2101-L	IF selection		7.7.1
2101-R	5 x LC bandpass filters (on IF selection)	(7)C86, (7)P81 on circuit board replaced	7.7.1
2101-S	5 x amplifier stages (on IF selection)	Gain potentiometer on board replaced, (7)P1,P3, P5 or P6	7.7.1
2101-M 2101-Q	Logarithmizer 10 x 10 dB log. stages	Gain pot. on board replaced, (8)P151	7.7.2, 7.5.2 7.7.2, 7.5.2
2101-O	IF converter		7.7.3
2101-P	Measurement section controller		No adjustment
2101-N	Calibration generator		7.7.4
2101-AO	Connector board		No adjustment
2101-AG	Interface board (series A to E)		No adjustment, 7.4.5
2101-AF	Memory board		No adjustment, 7.4.6
(18) AT 386	AT CPU (3011-9305.006)		No adjustment, 7.4.7
(18) A1	Floppy disk drive	---	---
2101-AL	Keyboard controller		No adjustment, 7.4.8
2101-AJ	Keyboard		No adjustment
2101-AK	Rotary control		7.9.1
4111-A	Display control board (BSK-3)		No adjustment, 7.4.9
2101-B	Timebase/YTO driver (excluding YTO)		7.8
2101-F	400 MHz oscillator	50L406	7.8.4
2101-C	Standard frequency adapter (NFO adapter)	50P101	7.8.1
50 OS1	YTO YIG oscillator (Sievers)		7.5.1
2101-A	Synthesizer controller	[(51)P1]	Not adjusted in SNA
2101-ZG	SHF pre-divider		No adjustment
2101-K	Synchronous divider / phase meter		No adjustment

[1] 2101-X or -Y fitted depending on version (2101-Y for narrow bandwidth option)

Table 7-2 List of all adjustments required after replacing circuit boards or modules

7.4 Special instructions for replacing circuit boards and modules

Certain measures in addition to the adjustments described are required to ensure correct function when certain circuit boards are replaced. These measures and special instructions are summarized in this section.

7.4.1 Circuit boards with different hardware status

The hardware status for some of the controller boards is stored in an EEPROM on the circuit board. This data is stored when the circuit board is manufactured. This hardware status is read out from the board during the boot-up sequence and is taken into account by the controller during measurement operations. If a circuit board fitted with an EEPROM containing such status data is replaced, the EEPROM contents (check sums) must be checked and corrected if necessary using the "EEPROM" service program. The following circuit boards are fitted with EEPROMs containing hardware status data:

- AT CPU (18)
- Keyboard controller (19)
- Memory (17)
- Interface board (16)
- Display control board BSK-3 (92)

The hardware status of other circuit boards or modules is readable from a port on the board. The status of these boards is set using DIP switches or pull-up/pull-down resistors which are fitted during manufacture. This status is fixed and can be read by the controller for use during measurement operations.

Note: The fixed hardware status of a board must not be changed. If the coded status does not match the actual board status, malfunctions will occur as the board will not be correctly controlled by the controller.

Note: The EEPROM on the interface board (16) alos contains the instrument serial number in addition to the hardware status (see section 7.4.4).

"EEPROM" service program

Starting the service program

Insert the service program floppy disk into drive A: and switch on the instrument. Once the instrument hass booted the operating system from this disk (prompt A:\ appears on the display) type in <EEPROM> using an external keyboard. Once the program has loaded, the display shown on the next page appears:

```
serial number is PR207, id = F88E
CPU EEPROM
3011  7001  0002  0618  1990  0001  0618  1990
0020  0504  1990  0315  0014  0000  0000  0000
55AA  C101  0060  D561  6462  0064  0E65  8066
0067  0068  0069  A06A  C26B  006C  006D  006E
0A6F  55AA  0C08  0000  0000  0000  0000  0000
0000  0000  0000  0000  0000  0000  0000  0000
0000  0000  0000  0000  0000  0000  0000  0000
0000  0000  0000  0000  0000  0000  0000  0C1C
checksum CPU-EEPROM  OK.
checkpat CPU-EEPROM  OK.                          (Press <RETURN> key)
BSK3 EEPROM
4111  7000  0001  0409  1991  5555  AAAA  0000
FFFF  FFFF  FFFF  0972  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  5DA2
checksum BSK3-EEPROM  OK.
checkpat BSK3-EEPROM  OK.                         (Press <RETURN> key)
MEMORY EEPROM
2101  7030  A002  1112  1990  5555  AAAA  0000
FFFF  FFFF  FFFF  0A28  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  5DA2
checksum MEMORY-EEPROM  OK.
checkpat MEMORY-EEPROM  OK.                       (Press <RETURN> key)
CONTROLLER EEPROM
2101  7035  FFFF  FFFF  FFFF  5555  AAAA  0000
FFFF  FFFF  FFFF  0EB9  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  5DA2
checksum CONTROLLER-EEPROM  OK.
checkpat CONTROLLER-EEPROM  OK.                   (Press <RETURN> key)
INTERFACE EEPROM
2101  7031  FFFF  FFFF  FFFF  5555  AAAA  0000
FFFF  FFFF  FFFF  0EB5  FFFF  FFFF  FFFF  FFFF
0004  001E  0005  FFFF  0000  0001  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF
F88E  5052  3230  373E  FFFF  FFFF  FFFF  FFFF
FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  FFFF  5DA2
checksum INTERFACE-EEPROM  OK.
checkpat INTERFACE-EEPROM  OK.
end.
```

Fig. 7-1 "EEPROM" service program display when no check sums were corrected.

If the EEPROM on the interface board does not yet contain the serial number of the instrument, this must first be entered using the program. In such cases, the program branches to a different menu (see section 7.4.5).

Otherwise, the EEPROM content for the AT CPU is displayed first, and the check sums are checked for correctness. Pressing the <RETURN> key causes the next EEPROM to be checked.
If the check sum of one of the EEPROMs is incorrect, the message: <Type "c" to try to correct else any other key> will be displayed. After entering <c>, the incorrect check sum will be recalculated and written to the appropriate EEPROM.

Note: The "EEPROM" service program only corrects the check sums in the EEPROMs. The circuit board hardware status which has been programmed in cannot be altered in this way. Alterations can only be carried out at the factory.

7.4.2 YIG filter control (3) and YIG filter (3) FL 1

7.4.2.1 YIG filter control (3)

Check the settings of the DIP switches before fitting a new board.

There are two Flash EPROMs (U10, U11) on the YIG filter control board; these contain the characteristic curve for the YIG filter (3)FL1.

Three procedures may be followed for replacing the YIG filter control board:

- Replacement of entire board [2101-AS1] including the Flash EPROMs. In this case, the YIG filter characteristic will need to be re-determined and stored (see section 7.5.3).
- Replacement of entire board [2101-AS1] with re-use of the two Flash EPROMs from the old board containing the filter characteristic (unplug EEPROMs froom old board and insert them into sockets on new board). This is of course only feasible if both EEPROMs are undamaged. This procedure avoids re-determining the filter characteristic.
- Replacement of entire board [2101-AS1] including the YIG filter. The filter and filter control are matched, with the filter correction data stored in the EEPROMs of the control board. After replacement, the frequency response of the instrument must be corrected (see section 6.1.1).

Note: After replacement of board [2101-AS1], a thorough check of the function of the YIG filter control for the entire frequency range (bands 1, 2 and 3).

7.4.2.2 YIG filter (3) FL 1

If the YIG filter must be replaced, the characteristic curve must be recorded. See section 7.4.2.1 and section 7.5.3.

7.4.3 Input section controller (5) [2101-AR, 2101-AR1]

DIP switch settings

Before replacing the board [2101-AR], [2101-AR1] check the settings of the DIP switch (5)S2 and correct them if necessary.

Switch	Meaning ON = closed = true
S 2.1	Circuit board 422/22 MHz/10 kHz [2101-Y] fitted (switch = ON when narrow bandwidth option fitted)
S 2.2	Step attenuator control table, bit 0 see step attenuator control table, table 7-4
S 2.3	Step attenuator control table, bit 1 see step attenuator control table, table 7-4
S 2.4	Step attenuator control table, bit 2 see step attenuator control table, table 7-4
S 2.5	Fundamental mixer with preamplifier fitted ? SNA-33 only = ON
S 2.6	Not used
S 2.7	Not used
S 2.8	Not used
S 2.9	Instrument without fundamental mixer (e.g. SNA-20, SNA-30 = ON)
S 2.10	= ON allows bias to be fed in when using an external mixer

Table 7-3 Meanings of switch (5)S2 positions on the input controller board

S2.4	S2.3	S2.2	Step attenuator characteristic (attenuation range/steps/frequency range)
0	0	0	65 dB/5 dB/26.5 GHz (Weinschel 5690-1)
0	0	1	70 dB/10 dB/40. 27 GHz (W&G FED-5/02, HP 33321 G/K)
0	1	0	70 dB/5 dB/4 GHz (W&G FED-5/01)
0	1	1	70 dB/10 dB/4 GHz (Weinschel 151-70)
1	0	0	Not used

Table 7-4 Control table for sellecting various types of step attenuator

Adjusting the coaxial relay operating voltage (series A + B)

The SNA is fitted with various coaxial relays (2) K1 from different manufacturers which operate from different voltages.
Before replacing circuit board [2101-AR] the correct supply voltage (+12 V or +23 V) should be selected for the relay by fitting link R54 **or** R52 (0 Ω resistor).

Note: Coaxial relay 2K1 is replaced by an electronic switch (diplexer) from series C onward. Control of the diplexer (band 0/band 1 to 3) requires fitting of circuit board [2101-AR1], input section control.

Adjusting the step attenuator operating voltage

The SNA is fitted with various step attenuators (2) AT1 from different manufacturers which operate from different voltages.
Before replacing circuit board [2101-AR], [2101-AR1] the correct supply voltage (+12 V or +23 V) should be selected for the step attenuator by fitting link R55 **or** R56 (0 Ω resistor).

7.4.4 Logarithmizer (8) [2101-M]

If the Logarithmizer board (8) [2101-M] is replaced, the correction tables for the new board "pkor_log.tab" and "pkor_lin.tab" must be copied into the instrument. The replacement Logarithmizer module must be completely adjusted (including the files "pkor_log.tab" and "pkor_lin.tab" on floppy disk). The files must be copied to the subdirectories listed below.

- Logarithmizer correction, linear to file: SNA\DATA\ pkor_lin.tab
- Logarithmizer correction, log to file: SNA\DATA\ pkor_log.tab

See also section 7.5.2 on page 7-14.

7.4.5 Interface board (16)

An EEPROM (16 IC18) containing the board hardware status and **the instrument serial number** is located on the interface board. After exchanging the board, the "EEPROM" service program must be started (see section 7.4.1). The following message appears on the display.

```
enter serial number of this device or 'e' = ENTRY OFF to abort
the serial number must be a name with a size of five characters,
beginning with a alpha letter and ending with at least 3 digits!
for example HM002, FM028, PR205 and A0055 are valid serial numbers.
enter serial number of this device

<a0125>                                          (entry of serial number)

serial number = a0125 (y/n)?y                    (confirmation of serial no.)
```

Fig. 7-2 "EEPROM" service program display after replacing the interface board requesting entry of the instrument serial number (input from the keyboard is shown in bold type).

When the correct serial number has been entered, the "EEPROM" service program checks the check sums of all EEPROMs in the instrument and corrects them if necessary (see "Circuit boards with different hardware status" on page 7-6).

Note: If a serial number has already been entered for a new interface board for test purposes, this cannot be changed using the "EEPROM" program. The display shown above only appears when there is no serial number stored in the interface board EEPROM.
The serial number stored in the interface board EEPROM of the instrument is displayed under the menu MODE/CONFIGURATION/HARDWARE/SOFTWARE (see section 3.1.1).

7.4.6 Memory (17)

The entire instrument software including the operating system is stored on the memory board. If this board is replaced because of a fault, the following must be borne in mind:

Check the jumper settings

Jumper P210 must be set to match the memory chip modules used.

P210:
Pin 2,3 ON: 1 Mbit chips
Pin 1,2 ON: 2 Mbit chips. ON = Jumper fitted

P211 sets whether EPROMs or FLASH-EPROMs (U400 through U413 and U500 through U511) are fitted.

P211:
Pin 2,3 ON; Vpp = +5 V ==> EPROMs fitted
Pin 2,1 ON: Vpp = VPROG ==> FLASH EPROMs fitted (default)

Fitting the lithium battery

There is a 512 kB battery-buffered SRAM on the memory board in which the correction tables are permanently stored (see "Recording correction data" on page 7-13). The lithium battery must be fitted before a new memory board is used.

Check and eventual correction of EEPROM check sums

Start the "EEPROM" service program after replacing the memory board (see section 7.4.1). The check sums for the EEPROMs on the memory board are corrected once the program has ended.

Installation of operating system and instrument software

If a new memory board is fitted, the software must be loaded again (see section 4.6).
Once the instrument software has been installed, the SNA should be switched off and then switched on again after a short wait (make sure you remove floppy disks from the drive before switching on again). The isstrument should now boot from the memory board and the normal display should appear on the screen.

Installation of compensation (correction) data

Finally, the compensation data for the SNA must be re-loaded (see section 4.7).

Note: The compensaion data is measured for each instrument individually. A floppy disk which includes this data is supplied with each SNA ("Compensation Data").

7.4.7 AT CPU (18)

After fitting a new CPU, switch on the SNA and make the correct CMOS settings (see section 4.5). Once the setup settings are complete, the instrument re-boots and should exhibit normal boot-up behavior until the measurement screen appears. Switch the instrument off and insert the service disk in the floppy drive <A>. Switch the SNA on to boot it from the service disk and type in <EEPROM> from the external keyboard to start the service program. The check sums contained in all EEPROMs are checked and corrected if necessary.

7.4.8 Keyboard controller (19)

Check all jumpers

Jumpers ST2, ST3 and ST4 must be fitted (shorts).
Links BR1 and BR2 must be closed.

Check and eventual correction of EEPROM check sums

Start the "EEPROM" service program after replacing the keyboard controller (see section 7.4.1). The check sums for the EEPROMs on the keyboard controller are corrected once the program has ended..

7.4.9 Display control board (92)

If this board is replaced because of a fault, the following must be borne in mind:

Check all jumpers

Check that all jumpers are fitted as per "Service manual appendix" (circuit diagram).

Check and eventual correction of EEPROM check sums

Start the "EEPROM" service program after replacing the display control board BSK-3 (see section 7.4.1). The check sums for the EEPROMs on the display control board are corrected once the program has ended.

7.5 Recording correction data

To achieve the high accuracy of the SNA-20/-23, certain modules or components of the instrument must be calibrated. The calibration data is stored in the instrument in the form of correction tables which are applied during measurements made with the SNA.

Note: Correction data can only be recorded by service centers which are specially equipped for this purpose.

Series A through E

The correction data, with the exception of the YIG filter data, are stored on a RAM disk (battery buffered SRAM on board (17), Memory). The RAM disk is drive B:\ and the correction data are located in subdirectory SNA\DATA. The following correction data are determined and stored for each SNA:

Frequency response Band 0 through Band 3

- Frequency response correction, Band 0 File: SNA\DATA\ fckor_b0.tab
- Frequency response correction, Band 1 File: SNA\DATA\ fckor_b1.tab
- Frequency response correction, Band 2 File: SNA\DATA\ fckor_b2.tab
- Frequency response correction, Band 3 File: SNA\DATA\ fckor_b3.tab

Logarithmizer characteristic, linear and logarithmic

- Logarithmizer correction, linear File: SNA\DATA\ pkor_lin.tab
- Logarithmizer correction, logarithmic File: SNA\DATA\ pkor_log.tab

YIG filter characteristic

The YIG filter characteristic is determined individually and stored in Flash ROM on the YIG filter controller.

Series F onwards

The correction data, with the exception of the YIG filter data, are stored on the built-in hard disk.

7.5.1 Frequency response adjustment, bands 0, 1,2 and 3

If any module in the signal path from the input socket [12] through to (6)J1 including all waveguides is repaired or replaced, adjustment of the frequency response is necessary. The synthesizer output level (1st LO) also affects the frequency response of the instrument. If the YTO oscillator of the synthesizer is replaced, frequency response adjustment is necessary.

Frequency response correction values are determined using a special test setup and software. Correction tables are generated and stored in the SNA for each receive band (Band 0, 1, 2 and 3). These correction values are applied mathematically to the results of normal measurements displayed by the SNA.

Recording of frequency response correction values requires complex computer-controlled equipment and can therefore only be performed in service centers specially equipped for this purpose.

7.5.2 Logarithmizer characteristic

This measurement generates and stores the correction table values for the logarithmizer characteristic.
Here, too, a special software-controlled test setup is required for determining the logaritmizer correction values. The software supports recording of the uncorrected logarithmizer characteristic and the calculation of the correction data for both "linear" and "logarithmic" operating modes (see section 7.5 on page 7-13).

Recording the logarithmizer characteristic requires complex computer-controlled equipment and can therefore only be performed in service centers specially equipped for this purpose.

7.5.3 YIG filter (3) characteristic

The YIG filter (band-pass) is tuned by a control current. The relationship between the control current and the filter frequency is non-linear and differs for each YIG filter. For this reason, the characteristic relationship between current and tuning frequency is recorded for each YIG filter. The YIG filter characteristic is determined using a special software-controlled setup and stored in the SNA in Flash EPROMs (U10, U11) on the "YIG filter controller" board (3), [2101-AS1]. If the YIG filter or the "YIG filter controller" board (3), [2101-AS1] is replaced, the YIG filter characteristic must be recorded and stored for the new components (see section 7.4.2 on page 7-8)

Recording the YIG filter characteristic (correction values) requires complex computer-controlled equipment and can therefore only be performed in service centers specially equipped for this purpose.

7.6 Frequency converter adjustments

7.6.1 Input section controller (5) [2101-AR]

Adjusting the external mixer bias current

Switch off the instrument and unplug the ribbon cable from socket P4. Close switch S2.10 (Bias on setting).
Connect contact P4.1 of socket P4 to an ammeter (digital multimeter with range ± 20 mA DC) and switch the instrument on.

5P102 Adjustment: Select the "External mixer" menu and initially enter a value of 12.8 mA for "External mixer bias".
Adjust trimmer P102 (input section control) so that the digital multimeter displays a current value of +12.8 mA ± 0.05 mA.

5P103 In the "External mixer" menu enter a value of 0 mA. Adjust trimmer P103 so that the digital multimeter displays a current value of 0 mA ± 0.05 mA.

7.6.2 "Band 0 frequency conversion control" (2) [2101-CF]

Adjustments required after replacing the " Band 0 frequency conversion control" board (2) [2101-CF]

Note: The Band 0 frequency conversion control board (2) [2101-CF] should only be replaced under exceptional circumstances by experienced and specially-equipped Service Centers, as the adjustment is very difficult. A minimal error in the adjustment can lead to temporary outage of the 4 GHz VCO e.g. when temperature changes occur.
Under normal circumstances, the entire microwave module should be replaced.
The Band 0 frequency converter module (including controller) is available as a spare part. The module is adjusted in the factory, and no further adjustment is necessary.

PLL breakthrough frequency

2R20 The PLL breakthrough frequency is determined by the value of resistor R20. The value of the resistor is determined by a program which takes the slope of the VCO tuning characteristic and the phase detector slope into account. The determination can only be performed in the factory at present.

If the control board is replaced, the value of R20 on the old board should be noted and the same value fitted to the new control board.

Reference tuning voltage

2R54 The reference tuning voltage is adjusted using potentiometer R54. The VCO must first be allowed to run uninterruptedly for 3 minutes, locked to a frequency of 4.000 GHz. If the VCO is not locked by this time, adjust R54 until the VCO locks (U_TP4 typically -6 V to -7 V). Connect a DVM between TP4 and TP6, and adjust R54 to give a value of 50 mV. Make sure that the VCO remains locked during the adjustment.

7.6.3 422 MHz/22 MHz converter (6) [2101-X]

For instruments not fitted with the "Narrow bandwidth" option.

Level adjustment

6P1

Connect a level generator to the measurement input of the device under test and connect a spectrum analyzer to the IF output of the 422 MHz/22 MHz converter 6BU2.

Instrument settings

D.U.T.:	
MODE	SPECTRUM ANALYSIS (CW)
FCENT	22 MHz
FSPAN	0 Hz (RUN MAN)
REFERENCE	0 dBm
ATTN	40 dB
Level generator:	
F	22 MHz
L	0 dBm (50 Ω)
Spectrum analyzer:	
MODE	SPECTRUM ANALYSIS (CW)
FCENT	22 MHz
FSPAN 5 MHz	
REFERENCE	-30 dBm/1 dB/DIV (SCALE 10 dB)

Use the spectrum analyzer to measure the level at IF output 6BU2 and use 6P1 to adjust the level to -30 dBm (50 Ω).

Adjustment of 400 MHz oscillator

6L1

Open the circuit bridges 6 L 1 (printed inductances) until the voltage at 6GL4 is 5.2 V ± 0.2 V.

7.6.4 422 MHz/10 kHz converter (6) [2101-Y]

For instruments fitted with the "Narrow bandwidths" option.

Level adjustment

6R117

Connect a level generator to the measurement input of the device under test and connect a spectrum analyzer to the 21.99 MHz output 6J12.

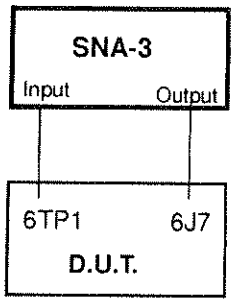
Instrument settings: see level adjustment in section 7.6.3.

Use the spectrum analyzer to measure the level at 6J12 and adjust using 6R117:
Series A, B: to -30 dBm (50 Ω)
Series C on: to -34 dBm (50 Ω)

Adjustment of 21.99 MHz crystal band-pass filter

6C28, C31, C32

Test setup



CAUTION: Remove all other RF cables from 2101-Y, otherwise the cutoff poles will be worse.

Fig. 7-3 Test setup 2 for adjusting calibration level

Initial instrument settings

SNA-3:

NETWORK ANALYSIS	
FCENT	21,99 MHz
FSPAN	10 kHz
REFERENCE	+6.5 dB
RBW	100 Hz
VBW	150 Hz
Sweeptime	1 s
SCALE	0.5 dB/Div.
SEND LEVEL	-12 dBm
GENERATOR	ON

Normalize the SNA-3.
When measuring at TP1 ensure good earth contact and a short inner conductor.

Adjusting the passband

Use C28, C31 and C32 to adjust the passband to < 0.3 dB at 21.99 MHz ± 2 kHz.

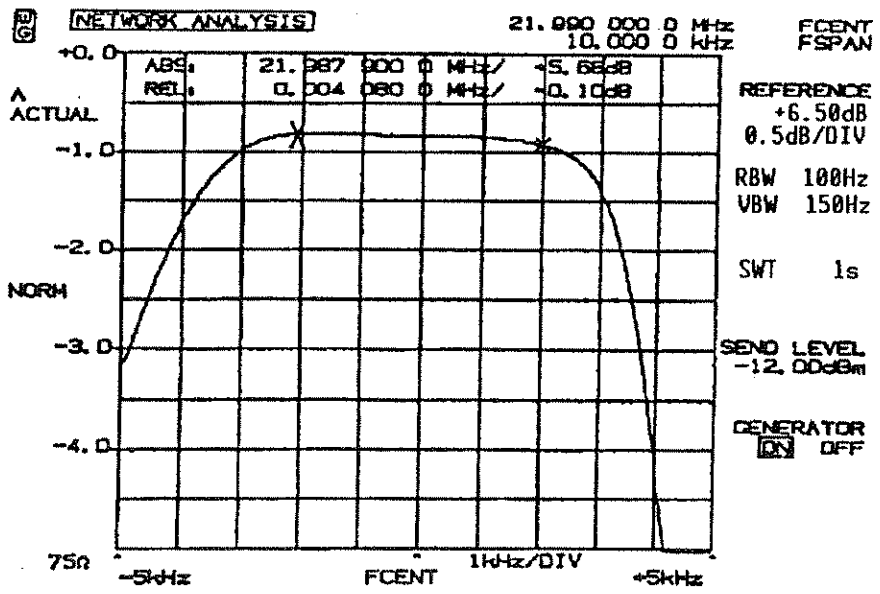


Fig. 7-4 21.99 MHz crystal band-pass filter passband

Adjustment (check) of stop-band

Set the SNA-3 to FCENT = 22.01 MHz.

Adjust cutoff pole using C28 at 22.010 MHz
C31 at 22.008 MHz
C32 at 22.012 MHz

Requirement: at 22.01 MHz ± 2 kHz: < -90 dB

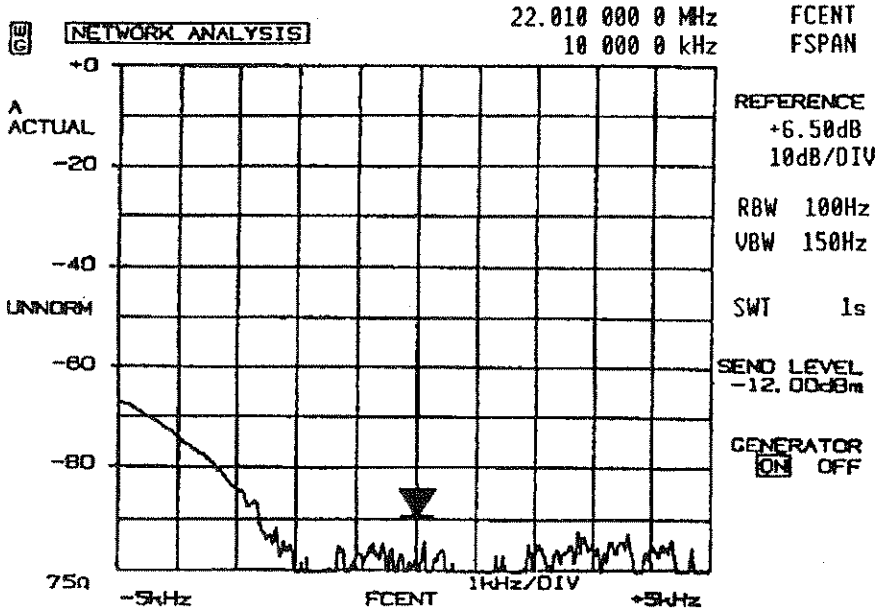


Fig. 7-5 21.99 MHz crystal band-pass filter stop band

Note: The adjustments affect one another. The passband should be rechecked (and readjusted if necessary) after adjusting the stop band.

7.7 IF measurement section adjustments

7.7.1 IF selection (7) [2101-L]

Test equipment and D.U.T. settings

SNA-3:	
SEND LEVEL	-15 dBm/75 Ω
FCENT	21.99 MHz
PSS-16:	
L	-24.3 dBm/75 Ω
D.U.T.:	
Reference	0 dBm

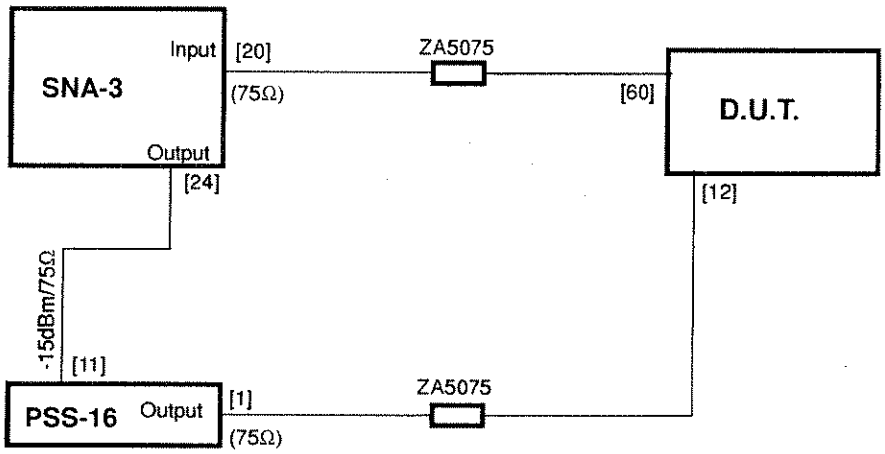


Fig. 7-6 Test setup for adjusting the IF selection

Adjustment of LC circuits

Select the maximum measurement bandwidth in the LC path of the D.U.T. (RBW = 3 MHz). Close links BR15.1-16. This connects the varicap diodes GL82 to an average tuning voltage of +5 V.

Adjustment of band center frequency

7C86 Use S1.6 to set the LC band-pass filter FI1 to minimum bandwidth (approx. 80 kHz). Set the SNA-3 to a SPAN of 1 MHz and adjust C86 (ceramic plate trimmer) on FI1 to give an attenuation minimum at 21.99 MHz (screening can lids with holes for adjustment must be fitted). If the screening can lids are not available, the adjustment can also be made but the attenuation minimum should be adjusted at f = 21.91 MHz.

Adjustment of insertion loss

7P81 Set switch S1.6 to the measurement setting and measure the level using the SNA-3 (SNA settings same as for adjustment of band center frequency). Now close switch S1.6 again (test setting) and adjust potentiometer P81 of FI1 to give a level value which is 0.5 dB higher than that obtained previously with S1.6 open.

Follow the same procedure for adjustment of the other LC stages FI2, FI3, FI4 and FI5, making sure that only the stage to be adjusted is set to the minimum bandwidth with S1.6 through 10.

Caution!

The temperature of the LC modules [2101-R] FI1, FI2, FI3, FI4 and FI5 must remain constant during adjustment (avoid drafts) as the circuits contain temperature compensation components (C7, R7).
Fitting the screening covers to the cans shifts the LC circuits by about +80 kHz compared with the adjustment without the covers.

After completing adjustment, close the links BR15.1 - 15.2again!

Adjustment of crystal stages

Select a measurement bandwidth for the crystal path of 30 kHz (RBW = 30 kHz).
All crystal stages except the one to be adjusted are bypassed using the links provided for this purpose (see figure 7-7 on page 7-20).

Adjustment of symmetry (stop-band attenuation)

7C602 Set the SNA-3 to a SPAN of 2 MHz to adjust the stop-band. Using the C trimmer C602 of the crystal stage being adjusted, set the stop-band attenuation at the sweep limits to the maximum possible **identical** values. None of the side resonances should be less than the minimum attenuation of 16 dB referred to the pass-band attenuation.

Adjustment of pass-band attenuation

7L601 Set the SNA-3 to a SPAN of 50 kHz to adjust the pass-band attenuation.
Use L601 (shell core) to set the broadest attenuation characteristic with attenuation minimum at f = 21.99 MHz.

Adjust all the crystal stages using this procedure (without screening covers fitted).

Links BR1 through BR14 must be set as follows for the adjustments:

Crystal stage	Links closed
1	BR1.1 - 1.2; 3.1 - 3.2; 5 - 6.1; 7.1 - 8; 9.1 - 10.1; 11.1 - 12.1; 13.2 - 14
2	BR1.1 - 2; 4.1 - 4.2; 6.1 - 6.2; 7.1 - 8; 9.1 - 10.1; 11.1 - 12.1, 13.2-14
3	BR1.1 - 2; 3.1 - 4.1; 5 - 6.1; 7.1 - 7.2; 9.1 - 9.2; 11.1 - 12.1; 13.2 - 14
4	BR1.1 - 2; 3.1 - 4.1; 5 - 6.1; 7.1 - 8; 10.1 - 10.2; 11.1 - 11.2; 13.2 - 14
5	BR1.1 - 2; 3.1 - 4.1; 5 - 6.1; 7.1 - 8; 9.1 - 10.1; 12.1 - 12.2; 13.1 - 13.2

Fig. 7-7 Links which must be closed for adjustment of the IF selection crystal stages

Link and switch settings for normal measurement operation

The links must be set as follows for normal measurement operation:

BR1.1 - 1.2; 3.2 - 4.2; 6.1 - 6.2; 7.1 - 7:2; 9.2 - 10.2; 11.2 - 12.2 und 13.1 - 13.2.

All switches of S1 must be set to "OFF".

Adjustment of 30 kHz crystal bandwidth

7P7 Set all switches S1of the D.U.T. to "OFF", all links to normal measurement operation and set RBW = 30 kHz. Test setup is as for adjustment of the LC filters (see figure 7-6 on page 7-19) . Set the SNA-3 so that the pass-band of the crystal filter (FCENT = 21.99 MHz) is visible on the screen. Use P7 to adjust the 3 dB bandwidth to B_{max} = 31 kHz.

Adjustment of IF gains

Attenuation matching of the crystal, LC and bypass paths

7P8

Note: Only the attenuation of the bypass path can be adjusted using (7) P8.

Test setup as in figure 7-6 on page 7-19.

Note: The output attenuator of the PSS-16 is used as reference attenuator for this adjustment. To ensure that the required accuracy for the IF amplifier adjustment is achieved, the output attenuator of the PSS-16 should first be calibrated and the actual value taken into account. A precision step attenuator (e.g. Siemens D2053) can be used instead of the PSS-16. The attenuator settings should then be chosen to ensure that the input level to the IF selection is approx. -32 dBm (50 Ω) for the reference measurement.

Select the LC, crystal and bypass paths consecutively by setting the RBW of the D.U.T. appropriately and measure the displayed level using the SNA-3 Set potentiometer P8 so that the attenuation of the bypass path lies between that of the LC and crystal paths.
The filter path is selected by the RBW setting of the D.U.T.:

- bypass path RBW 10 MHz
- LC filter path RBW 3 MHz
- crystal filter path RBW 30 kHz

Adjustment of IF amplifiers

Test setup as in figure 7-8 on page 7-22. Set the D.U.T. as follows:

FSTART	21.99 MHz
FSTOP	21.99 MHz
ATTN	0 dB
EXT. ATTN	0 dB
SCALE	10 dB
RBW	10 MHz
VBW	10 MHz
REFERENCE	-27 dBm

Reference measurement

Remove link BR17.1 - 17.2 (amplifier V1 ==> v = 1).

Set the PSS-16 (level) and the D.U.T. (reference) as specified for the reference measurement in table 7-5 on page 7-22.

Measure the reference level using the SNA-3.

Note: If the PSS-16 is set to a level of -24 dBm, the level after the ZA 5075 (matching pad) at the input to the IF selection (BU1) will be about -30 dBm (50 Ω). This corresponds to the nominal IF selection input level.

Adjustment

7P1, P2, P3, P4, P5, P6

Switch in the IF single gain stages 1, 2, 4, 8 and 16 dB one after the other individually, reducing the PSS-16 output level appropriately, and use P1 through P6 to adjust each stage to the reference level. Settings for adjusting the amplifier stages are shown in table 7-5 on page 7-22. During adjustment of the 2nd 16 dB amplifier stage (V3), the 1st 16 dB amplifier is also switched on as the instrument software does not allow individual control of this amplifier stage (reference shifted).

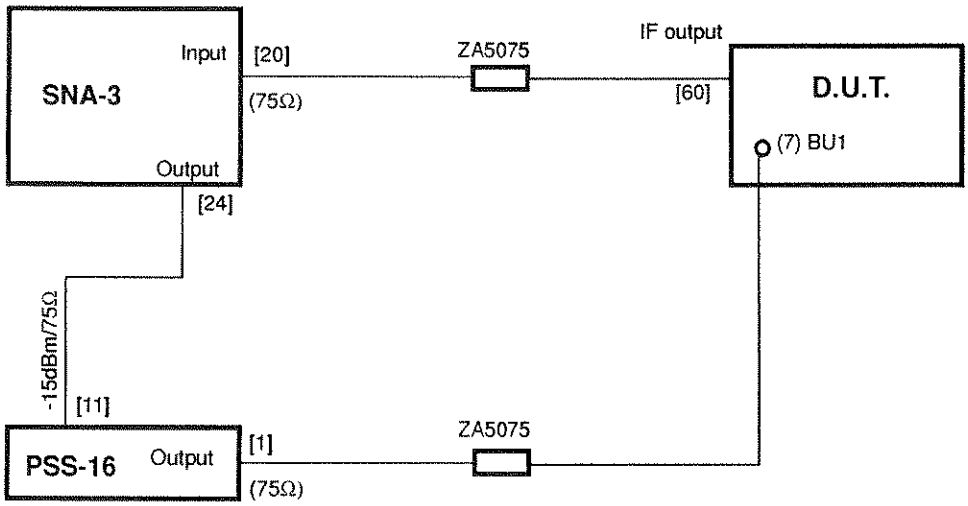


Fig. 7-8 Test setup for adjustment of the IF amplifier stages

Reference D.U.T.	Level PSS-16	V2 0/16 dB	0/-2 dB	V3 0/16 dB	0/-1 dB	V4 0/8 dB	V5 0/4 dB	Adjust using
-27	-26 dBm	0	0	0	0	0	0	Reference measurement
-25	-24 dBm	0	**1**	0	0	0	0	P2
-26	-25 dBm	0	0	0	**1**	0	0	P4
-31	-30 dBm	0	0	0	0	0	**1**	P6
-35	-34 dBm	0	0	0	0	**1**	0	P5
-43	-42 dBm	**1**	0	0	0	0	0	P1
-59	-58 dBm	1	0	**1**	0	0	0	P3

Table 7-5 Parameter settings for adjustment of the IF amplifier stages

Note: "1" in the table means that this stage is switched on. For the 0/-2 dB and 0/-1 dB stages, "1" means that the stage is switched to attenuation (-2 dB, -1 dB).

Frequency response check

Sweep the frequency range 17 MHz to 27 MHz. The attenuation minimum should be at f = 22 MHz.
The increase in attenuation at the limit frequencies must not exceed 2 dB for any IF gain setting.

7.7.2 Logarithmizer (8) [2101-M]

+5 V regulator

8P800 Measure the voltage at TP 21 using a DVM and use P800 to set the voltage to +5.0 V.

The -5 V regulator derives its output from the +5 V and cannot be set independently. During adjustment with P800, make sure that both voltages are within the tolerance of ± 50 mV.

Logarithmic amplifier working point

8P503 Measure the voltage between TP 10 and TP 19 (-12 V U_B) using a DVM and use P503 to set it to +4.0 V ± 10 mV.

Rectifier threshold voltage

8P501 Measure the voltage between TP 8 and TP 9 using a DVM and use P501 to set it to +900 mV ± 1.5 mV.

Current source bias

8P500 Measure the voltage between TP 6 and TP 8 using a DVM and use P500 to set it to - 5.75 V ± 10 mV.

Video amplifier offset adjustment

8P0401, P0400 Set the D.U.T. scale to 100 dB. Open link BR1.1 - 1.2 and close link BR3.1 - 3.2. Measure the voltage at TP24 using a DVM and use P0401 to set it to 1 mV ± 1 mV.
Open link BR3.1 - 3.2 öffnen. Measure the voltage at TP24 using a DVM and use P0400 to set it to 1 mV ± 1 mV.

A high-impedance DVM must be used for this measurement.

****** Close link BR1.1 - 1.2 again *****

Adjustment of linear rectifier threshold

8P0502 (Set the SNA to linear scale). Measure the voltage at TP24 using a DVM and use P0502 to set it to 35 mV ± 15 mV.

10 MHz video filter

8L400, L401, L402 Open links BR1.1 - 1.2 and BR3.1 - 3.2 and close link BR2.1 - 2.2 (video test input activated).

Using a spectrum and network analyzer (e.g. SNA-3), determine and adjust the attenuation characteristic of the 10 MHz video filter for "low" (log. scale) and "high" (linear scale) gain. Make the following settings on the spectrum and network analyzer (e.g. SNA-3):

Network Analysis	
FSTART	1 MHz
FSTOP	12 MHz
SCALE	1 dB/DIV
REF	+16 dB
SEND LEVEL	-30 dBm/Z = 75 Ω

Connect the TX output of the SNA-3 to the video test input (8)BU6 of the D.U.T. Connect a high-impedance test probe (TK-11) to the input of the SNA-3 and connect the TK-11 to TP5. Normalize the test setup. Set the D.U.T. to the log. scale 100 dB (= small video gain) and measure at TP24 **(TP24 is DC-coupled!)** using the TK-11. The filter frequency response should

drop off steadily with increasing frequency. The attenuation at the limit frequency of 10 MHz referred to the level maximum at 1 MHz should be 5 dB ± 0.5 dB. Use L400, L401 and L402 to adjust approximately to the trace and attenuation value shown in figure 7-9 on page 7-24.

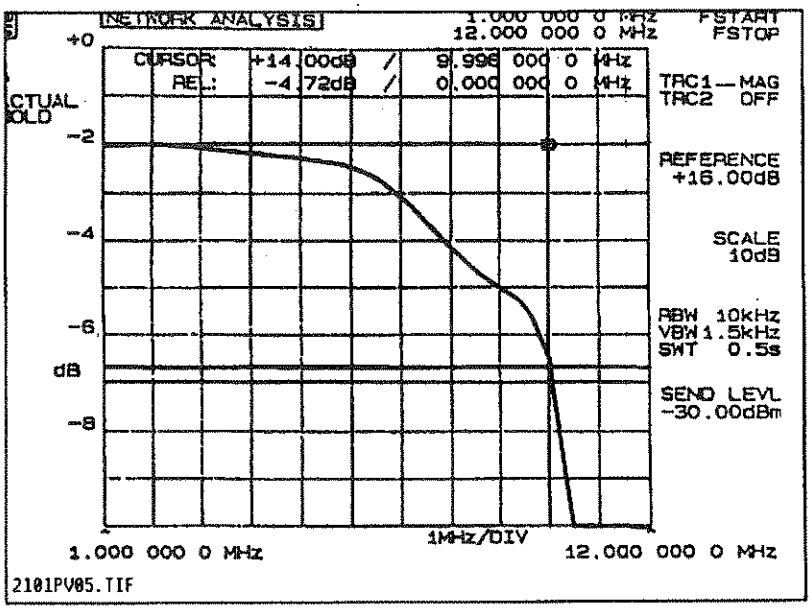


Fig. 7-9 Typical attenuation characteristic of the 10 MHz video amplifier at low gain

Now set the D.U.T. to linear scale (high video gain) and set the REFERENCE on the SNA-3 to +37 dB. The attenuation at the limit frequency of 10 MHz referred to the level maximum at 1 MHz should be 5 dB ± 0.5 dB. Use L400, L401 and L402 to adjust approximately to the trace and attenuation value shown in figure 7-10 on page 7-24.

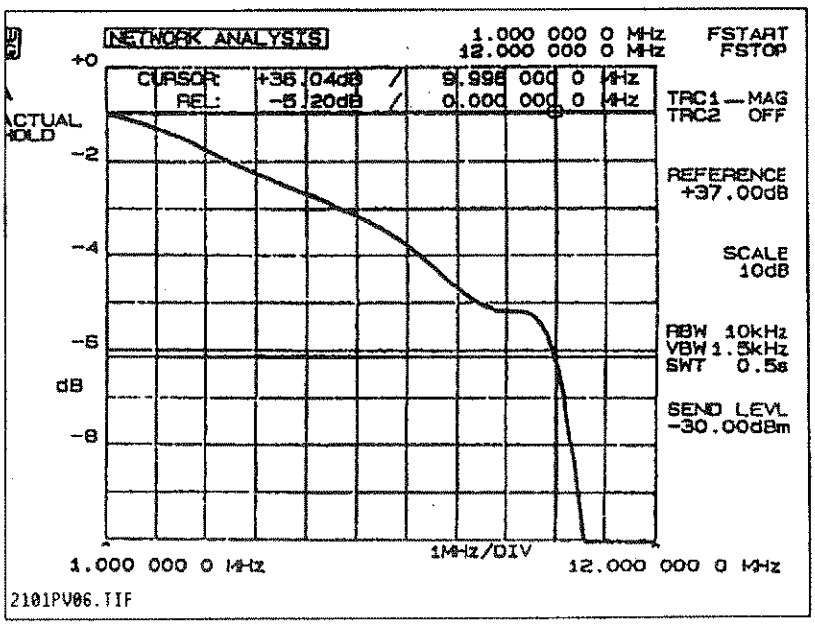


Fig. 7-10 Typical attenuation characteristic of the 10 MHz video amplifier at high gain

As the same adjustment components are used for both adjustments, a trade-off must be achieved such that both measurements lie within the given tolerances.

After completing the adjustment, set all links back to normal measurement positions.

10 MHz noise filter

8C227 Use a spectrum and network analyzer (e.g. SNA-3) to determine and adjust the symmetry of the 10 MHz noise filter (NBW). make the following settings on the spectrum and network analyzer (e.g. SNA-3):

Network Analysis	
FCENT	21.99 MHz
FSPAN	20 MHz
SCALE	0.5 dB/DIV
REF	+1 dB
SEND LEVEL	- 30 dBm/Z = 75 Ω
RBW	30 kHz
D.U.T. settings	
RBW	≥ 1 MHz

Replace log. stage no. 5 with **test board 34-2101** and connect the output of the SNA-3 to the test board socket (noise filter input). Use the TK-11 to measure at one of the two amplifier outputs of log. stage 6 (pin 13 or pin 21) and normalize the SNA-3. Now connect the TK-11 to TP26 or TP27 (noise filter outputs) and adjust the filter using C227 so that the attenuations at 21.99 MHz are symmetrical and 0.5 dB below the normalization trace (see figure 7-11 on page 7-25). The permitted deviation from the reference value (normalization trace) for FCENT ± 4 MHz is +0.2 dB to -1.2 dB.

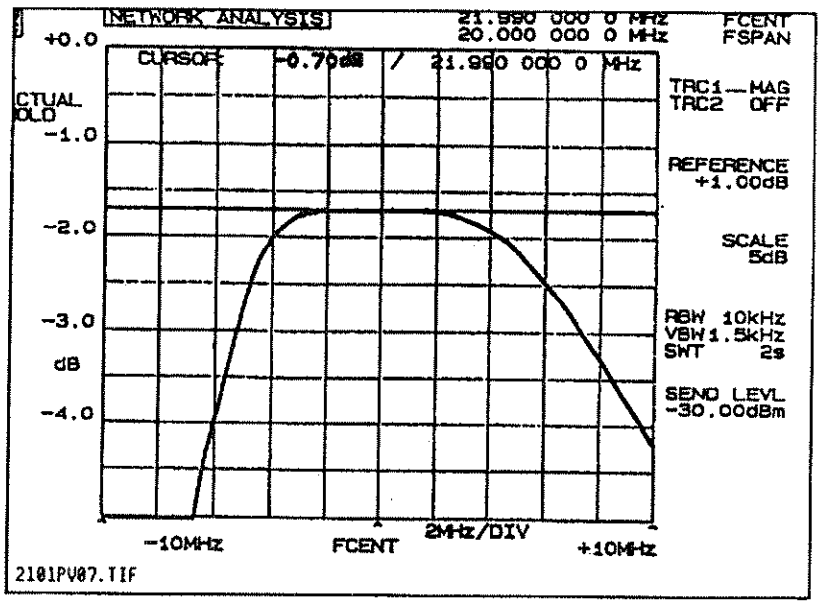


Fig. 7-11 Typical attenuation characteristic for the 10 MHz noise filter (bypass path)

Adjustment of the 400 kHz noise filter

8L208 The center frequency and gain of the 400 kHz noise filter are set automatically by computer-controlled calibration equipment. The center frequency is set with a control voltage between 0 and -11 V at (8)TP1; the gain is set with a control voltage between 0 and -11 V at (8)TP2. Adjustment of the center frequency is very difficult without the special test program.

Adjustment without test program

Note: This adjustment should only performed in exceptional circumstances, as p.c.b. tracks must be broken to perform it.

The center frequency calibration and the gain of the noise filter must be disabled for the adjustment (break the p.c.b track between IC82.2 Pin7 and TP1, and between IC64.15 and TP2). Feed a voltage of -3.9 V in at TP1, and feed an average voltage of about -4.5 V in at TP2. Set the noise bandwidth of the D.U.T. to 400 kHz (set the RBW from 1 kHz to 100 kHz, see table 7-6). The test setup and other settings are as for measurement of the 10 MHz noise bandwidth. Set the filter attenuation of the 400 kHz noise filter to 0 dB (normalization trace) by varying the voltage at TP2. Use L208 to set the center frequency of the 400 kHz filter to exactly 21.99 MHz (use L208 and the control voltage at TP2 alternately to achieve a gain of 0 dB at the center frequency). The attenuation characteristics of the noise filter are shown together in figure 7-12 on page 7-26.

Noise bandwidth	Use at resolution bandwidth (RBW)
> 10 MHz (bypass path)	≥ 1 MHz
1 MHz	300 kHz
400 kHz	1 kHz to 100 kHz

Table 7-6 Noise filter settings as dependent on the selected RBW

The peak of the 400 kHz filter trace must lie exactly on the normalization or 10 MHz filter trace at 21.99 MHz.

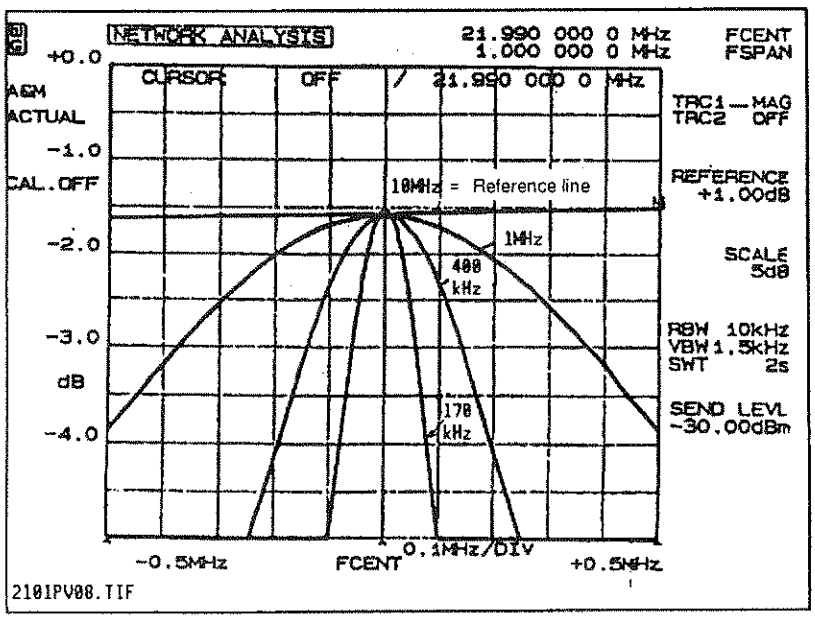


Fig. 7-12 Simultaneous display of all noise filter characteristics

Adjustment of 10 dB logarithmic amplifier gain

8P151 The gain of the 10 dB logarithmic amplifier must be adjusted to exactly 10 dB.

Note: Gain adjustment of the 10 dB logarithmic amplifier requires special test equipment and can only be performed by Service Centers specially equipped for the purpose.

Correction of logarithmizer characteristic

Note: This measurement generates and stores correction tables for the logarithmizer. This requires special test equipment and can only be performed by Service Centers specially equipped for the purpose.

Replacement of p.c.b.

If the "Logarithmizer" board (8) [2101-M] is replaced, the correction values for the new board in the files "pkor_log.tab" and "pkor_lin.tab" must be copied into the instrument. The replacement logarithmizer module must be previously calibrated (including the files "pkor_log.tab" and "pkor_lin.tab" on floppy disk). IThe following files must be copied into the specified directories.

- Logarithmizer correction, linear to file: SNA\DATA\ pkor_lin.tab
- Logarithmizer correction, logarithmic to file: SNA\DATA\ pkor_log.tab

7.7.3 IF converter (9) [2101-O]

Note: Adjustment of the IF converter board requires special test equipment and can only be performed by Service Centers specially equipped for the purpose.

The following adjustments must have been made to the board:

P303, P400 ; P401 • Linearity and synchronism
P301, P302 • Overall gain and offset
P200 • DC adjustment of rms rectifier
P300 • Adjustment of bipolar offset

Replacement of the circuit board

The IF converter module 2101-O is available as a completely adjusted spare part.

7.7.4 Calibration generator (11)[2101-N]

7.7.4.1 Adjusting internal and external calibration levels

Test setup 1

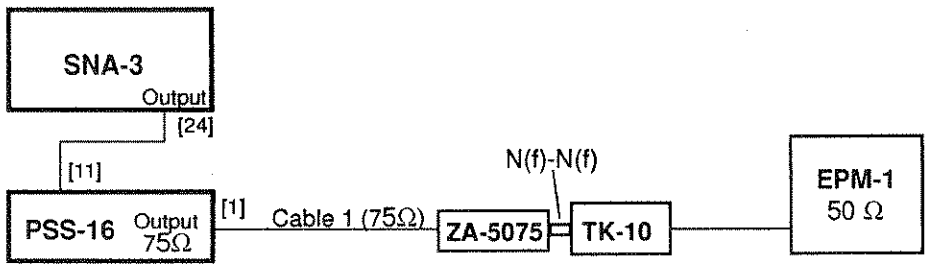


Fig. 7-13 Test setup 1 for adjustment of calibration level

Test setup 2

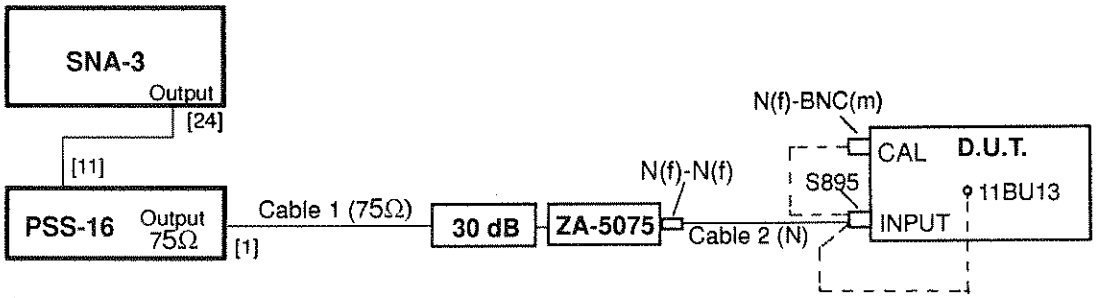


Fig. 7-14 Test setup 2 for adjustment of calibration level

Initial instrument settings

SNA-3:	NETWORK ANALYSIS	
	FCENT	21.99 MHz
	FSPAN	0 Hz
	SEND LEVEL	-15 dBm
	GENERATOR	ON
PSS-16:	Level	+5.8 dBm
EPM-1, 50 Ω:	0 dBm, R_i = 50 Ω	
D.U.T.:	PRESET, SPECTRUM ANALYSIS (CW)	

Enabling permanent operation of the CAL output:

- Connect a PCkeyboard to the D.U.T. socket [1].
- Press Alt + F10 followed by ENTER (sets instrument to DOS mode)
- If necesary, match the keyboard driver (see section 4.10).
- Further entries: set calout=1 ENTER
  k ENTER (returns to measurement program)

--> Permanent operation is now enabled but not activated.

Further D.U.T. settings:

FCENT:	21.99 MHz
FSPAN:	0 Hz
REFERENCE:	-29.5 dBm
SCALE:	10 dB
RBW:	1 kHz
VBW:	10 Hz
SWT:	25 ms
ATTN:	10 dB

Providing the reference signal

Calibrate the EPM-1.
Test setup 1 as in figure 7-13.
Adjust the output level of the generator until the EPM-1 indicates a value as near as possible to 0.00 dBm. Note the difference as correction value "X_1".

Measuring the reference signal

Test setup 2 as in figure 7-14 with connection from ZA-5075 to the INPUT of the D.U.T. Make sure that the same ZA-5075 is used as for test setup 1.
Activate the ABS and REL markers (press the "MKR" twice).
The display shows the reference as a trace at approx. -30 dBm.
Use the MARKER / MARKER UPDATE softkeys to set the ABS marker to HOLD. Press RTN to return to the main menu.
This stores the reference signal.

Adjusting the internal calibration level

11P2

Connect the internal CAL output of the D.U.T. (11) BU13 to the input of the D.U.T.
The output signal from the CAL output is displayed with a relative value of approx. -30 dBm.
Note the relative value as "X_2".
-> Nominal value = X_2 - X_1
Use (11)P2 to adjust the relative value to the nominal value.

Adjusting the external calibration level

11P1

Connect the CAL output [11] of the D.U.T to the INPUT using cable 2 (N). Make sure you use the same cable as was used for the reference measurement.
Switch the CAL output on permanently from the CAL menu: Press "CAL.OUTPUT ACTIVE", then "RTN".
The output signal from the CAL output is displayed with a relative value of approx. -30 dBm.
Note the relative value as "X_3".
-> Nominal value = X_3 - X_1
Use (11) P1 to adjust the relative value to the nominal value.

Note: Always adjust the internal calibration level first, as the external level is dependent on both 11P1 and 11P2.

7.7.4.2 FM demodulator center frequency

D.U.T. setting

FCENT 22 MHz

Feed a level of -30 dBm (50Ω) at F = 22 MHz into (7)BU1.

11C317 Measure the voltage between pins (11)IC31.6 and (11)IC31.12 (TP12) using a DVM and use C317 to adjust such that the magnitude of the voltage is <0.3 V.
After this perform the checks as detailed in "Checking the FM demodulator" on page 6-29.

7.8 Synthesizer adjustments

7.8.1 10 MHz standard frequency adjustment

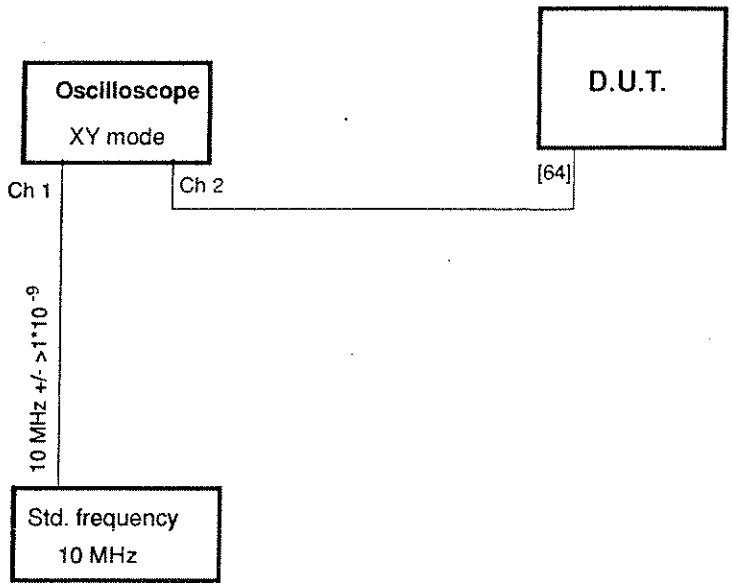


Fig. 7-15 Test setup for adjustment of 10 MHz standard frequency

50P101

Preparation: Allow the instrument to warm up for about 1 hour.

Test setup as per figure 7-15. Set the oscilloscope to X/Y mode. Adjust the instrument's 10 MHz standard frequency using P101 until the Lissajous figure on the oscilloscope screen is practically stationary (a maximum of one rotation in 11 seconds is permitted).

If an external frequency standard is not available, the 10 MHz standard frequency can be measured with a very accurate frequency counter and P101 adjusted to give 10 MHz 0.1 Hz.

Note: The accuracy of the frequency standard or frequency counter used directly affects the frequency accuracy of the SNA.

7.8.2 Upper YTO frequency limit (maximum frequency)

Setting or checking

50 P2

Connect the synthesizer RF output "1.LO" ([71] on the back panel) to a spectrum analyzer. Turn potentiometer (50) P2 to the right as far as it will go. Set D.U.T. FCENT to 7.499 999 999 GHz (FSPAN = 0 Hz, RUN = MAN). The 1st LO frequency must be 7,921 989 999 GHz which should be measurable with the spectrum analyzer connected to socket [71]. Now turn potentiometer P2 to the left until the frequency of the 1st LO just begins to drop. Now turn potentiometer P2 back approximately 1 turn to the right. This sets the upper YTO limit to approx. 8.2 GHz.

Note: Exact setting of the upper YTO limit to 8.2 GHz requires special test equipment and can only be performed by Service Centers specially equipped for the purpose.

7.8.3 Lower YTO frequency limit (minimum frequency)

Setting or checking

50P3

Connect the synthesizer RF output "1.LO" ([71] on the back panel) to a spectrum analyzer. Open switch (50)S1 (wire link) and close switch (50)S3. This interrupts the regulator loop (S1) and limits the DC gain of the PI regulator (50 IC26) to a finite value (S3). This drives the YTO to the lower limit (2.8 GHz when the lower YTO limit is adjusted correctly).
Adjust potentiometer P3 to set the lower YTO limit to 2.8 GHz ± 10 MHz.

7.8.4 400 MHz oscillator adjustment (400 MHZ_RESONATOR)

Note: Adjustment is only required if board 2101-F is replaced.

50L406

Function: LC resonator adjustment in the 400 MHz oscillator (adjustment of printed inductance L406).

Preparation: Adjustment of the 10 MHz standard frequency must have been performed first.

Connect the 400 MHz output "400MHZ" BU7 to a frequency counter. The frequency display should settle as described under adjustment of the 10 MHz standard frequency (if not, adjust the 10 MHz standard frequency). The cover of the 400 MHz oscillator must be closed. Use a DVM to measure the control voltage at IC35 Pin 6. It should be between 4 and 6 V. If not, remove as many links in the printed inductance L406 until the voltage is within this range. The voltage changes by ≈ +2 V for each link removed.

7.9 Controller adjustments

7.9.1 Rotary control (21) [2101 AK]

Adjustment of IC9 offset

21P1 The pulse generator must be idle (do not move rotary control). Use a DVM to measure the voltage between TP1 and ground. Use P1 to set +2.5 V at TP1.

7.10 Power supply unit adjustments

7.10.1 PSU CG44 (1) [Gossen]

Preparation

The PSU is fitted in the instrument and all modules are connected (nominal load).
The following output voltages can be set and should be adjusted. The potentiometers on the PSU are labelled accordingly.

+5 V output voltage

The +5 V rail is measured on the memory board / AT-CPU at plug J2 betwen Pin C29 (+5V) and Pin C31 (ground) and adjusted to **+4.9 to 5.0 V**.
As a check, measure the voltage between the screw connectors MT1/ MT3 (+5V) and MT2 (ground). The voltage must not exceed +5.30 V.

> ***Caution!***
> This adjustment is important for correct function of the instrument. If the +5 V rail is set too low, the instrument may not work at all (does not boot, operates erratically). If the voltage directly on the PSU (MT1/ MT3) is more than +5.30 V the PSU may switch off under certain conditions (overvoltage protection).

+6.5 V output voltage

The +6.5 V rail is measured on the voltage distribution board (1), [2101-BD] at capacitor C16 and adjusted to **+6.8 V ± 0.1 V**.

-6.5 V output voltage

The -6.5 V rail is measured on the voltage distribution board (1), [2101-BD] at connector B8 and adjusted to **-6.5 V ± 0.1 V**.

If the PSU together with the voltage distribution board [2101-BD] is replaced, the adjustments in section 7.10.2 should also be made.

7.10.2 Voltage distribution (1) [2101-BD]

Adjustment of overtemperature cutoff

1P01 Adjustment with P01 should be made when the temperature is measured. The casing cover of the SNA should be placed loose on the instrument (self-heating).
The instrument should switch to "standby" mode at a temperature of > 55 °C (thermal cabinet).
If a thermal cabinet is not available for making the adjustment, set the voltage at IC 5.3 Pin 9 at room temperature to ≈ 4.3 V.