LC102 "AUTO Z" CIRCUIT DESCRIPTION & ANALYZER NOTES

The LC102 "Auto Z" Meter Capacitor—Inductor Analyzer is the only microprocessor controlled instrument in the service industry that is dedicated to finding defective capacitors and inductors reliably, accurately, and automatically. It has the ability to completely analyze the condition of capacitors and coils with only the push of a button. Other instruments check capacitors for value only, but that is only half of the picture. Capacitors also tend to get leaky, develop dielectric absorption, or develop ESR which other testers cannot measure. Coils can develop a single-shorted turn, thereby changing its quality (Q) characteristics, but not change in value appreciably. The LC102 "Auto Z" will test all of these parameters. Another advantage of the LC102 is the fact that this unit is portable. It can be powered by battery and will turn itself off after approximately 15 minutes after its last reading.

POWER SUPPLIES

Looking at the block diagram, we will begin by describing the power supplies. The LC102 contains two power supplies: one is the main supply which generates the needed voltage for the microprocessor and measuring circuitry and the other is a variable 1 to 1000 volt leakage supply. These two power supplies are located on the 3000 board. The LC102 can be powered by a BY234 battery, or a PA251 power adapter, or both. When the PA251 is connected, its output is fed to the 14.5 volt regulator section. This regulator section performs two functions. It reduces and regulates the PA251's 18 volt output and also charges the battery when installed. The Pulse Width Modulator, transformer, and rectifier section of the main supply converts the 12-14.5 volts delivered from the battery or power adaptor to multiple voltage outputs. The power supplies' outputs are: +18 volts, +12 volts, +5 volts, and -5 volts.

The Leakage Supply produces the voltage for the capacitor leakage test. The output of the leakage supply is controlled by the microprocessor via two digital-to-analog converters. This supply operates by converting the 12 volts received from the main supply to a lower or higher value as controlled by the Pulse Width Modulator. The 12 volts is amplified by a 1:3 turns ratio transformer and then rectified and filtered. A portion of this output voltage, determined by the D/A converters, is sampled, peak detected, and compared to a reference voltage. When the sampled portion is equal to the reference, the supply is stable and its output will remain constant. The leakage supply also incorporates an active load which has several purposes. First, switching supplies must be properly loaded in order for them to operate correctly. The active load provides a constant 200 uA drain to load the supply at all times. Second, the active load is used to reduce overshoot of the output during turn on. When the output reaches its full selected voltage, the active load temporarily increases the supply load thus slowing the fast rise in output voltage. Last, the active load provides a safe means of discharging the filters once the supply is turned off. If this feature was not incorporated, a dangerous voltage would remain on the filter capacitors, thus creating a shock hazard not only to the technician working on the unit, but also to the technician using the unit.

MICROPROCESSOR

The Main board (2000 board) contains the circuitry for performing all of the tests to effectively test capacitors and inductors. The heart of this board is the microprocessor.

It, with its software held in the EPROM, controls the extensive array of memory mapped I/O. The microprocessor also determines all automatic good/bad indicators and performs any calculations needed for these indicators or any other calculated display outputs.

Looking at the block diagram, we can see that the microprocessor is connected to every section of the LC102 main board through either its control bus or data bus. The microprocessor, operating at 6 MHz, receives its instructions, or program, from the EPROM. The Address Latch holds the address information used by the EPROM and also Control and Data I/O.

CAPACITANCE

The LC102 measures capacitance by the formula C=(I x dt)/dv. During the test, a known current (I) is applied to a capacitor. While this current is charging the capacitor, the time it takes to pass between two voltage points is measured. This time is then converted directly to a measurement of capacitance.

Although there are twelve software ranges for displaying capacitance, only four hardware ranges exist. A full 12 ranges are accomplished by using the hardware ranges to cover wider capacitances and adjusting the display accordingly. The table shown below tells which hardware ranges are used with each software range.

SOFTWARE RANGE	HARDWARE RANGE	CURRENT	MODE	TRIP LEVELS
1pF-199.9pF	0 -.002uF	3.3 uA	Continuous	.5v-3.5v
200pF-1999pF	"	"	"	"
.002uF-.0199uF	.002uF - 2uF	330 uA	"	"
.02uF -.1999uF	"	"	"	"
.2uF - 1.999uF	"	"	"	"
2uF -19.99uF	2uF - 2000uF	60 mA	"	"
20uF -199.9uF	"	"	"	"
200uF -1999uF	"	"	"	"
2000uF-19990uF	2000uF - 2F	416 mA	"	1v-1.75v
20000-199900uF	"	"	"	"
.2F - 1.999F	"	416 mA	Pulsed	"
		60 mA	"	
2F - 20F	"	416 mA	"	"
	"	60 mA	"	"

TABLE 1.

The capacitance measuring sequence begins with the largest current source selected. If the capacitor is smaller than the particular hardware range is capable of measuring, the microprocessor down ranges and selects the next lower hardware range until either the lowest range is reached or a valid capacitance reading is taken. If, while in the first range, the LC102 encounters a large capacitor that does not read within a specific amount of time, or a large capacitor with high ESR is seen, the unit assumes that the capacitor is a large cap ().2F) and enters a mode where the capacitor is pulsed with the 60 mA and 416 mA current source. The reason that the capacitor is pulsed is so the ESR usually found within large capacitors and the internal resistance of the LC102 circuitry will not effect the capacitance readings as the upper trip limit is set at a low 1.75 volts. The upper trip level is tested only during the time that the 60 mA and 416 mA source is off. (Pulsed mode)

The different trip levels used in the capacitance test are shown in Table 2. There is also a .25 volt lower trip level used during the discharge cycles of the top two hardware ranges.

Because the testing of large value, double layer capacitors takes longer that the testing of standard capacitors, a "thinking bar" indicator has been incorporated into the double layer test to signify its operation and inform the user as to the operation of the test. When the capacitance value button is pressed and the unit determines that a double layer capacitor is being tested, the "0000" display turns to the thinking bars. The bars continue to scroll across the display as the test progresses. Two seconds between bar movement indicates that the unit is in the discharge mode and one second between bar movement indicates that the capacitor is charging. Once a reading is displayed, the units holds that reading, giving no futher updates. Note that this reading hold only takes place after a double layer capacitor has been read.

DIELECTRIC ABSORPTION

When the LC102 first enters the D/A test, it checks to see if the capacitor under test has a charge on it. If it does, the unit will enter a "wait" mode and discharge the capacitor through a low resistance discharge FET. It will discharge the capacitor for two seconds and test it again, only continuing on with the D/A test if the capacitor has been fully discharged.

Once the capacitor is discharged, the unit enters the actual D/A test. For two seconds, a 416 mA current source is turned on and the capacitor is charged. The voltage applied to the capacitor at this time is limited to 3 volts to avoid damaging any low voltage capacitors. After the two second charge time, the supply is turned off and a discharge FET is turned on. The capacitor is discharged for two seconds and then released to a high impedence. After 2/3 of a second from the release of the discharge FET, a measurement of the voltage on the capacitor is taken. This voltage is then converted to a percentage by the microprocessor and displayed as Dielectric Absorption in percentage.

CAPACITOR LEAKAGE

In order to effectively measure leakage current through a capacitor, the voltage across the device must be kept constant and no voltage should be developed across the measuring circuitry. Also, if the measuring circuitry ranges, there can be no effect seen by the capacitor because of this ranging. By utilizing a current-to-voltage converter, the ground lead or ground return is constantly kept at ground potential. The I/V Converter used in the LC102 has four automatically selected ranges and produces an output voltage relative to its input current or in this case, the leakage current of the capacitor. The four ranges with their respective current capabilities are listed below.

RANGE	CURRENT RANGE
1	0 - 19.99uA
2	20uA-199.9uA
3	200uA-1.99mA
4	2mA-19.99mA

TABLE 2

ESR BLOCK

The circuitry for ESR measurement will be explained in block diagram form at this time. First of all, what is ESR? ESR (Equivalent Series Resistance) is the inherent characteristic of a capacitor to have a certain amount of resistance in series with its capacitance qualities. If ESR becomes large enough, the capacitor becomes in essence, an "open" capacitor. The voltage developed across a capacitor with no ESR when it is charged, rises in a straight line because a constant current generator is used. The formula for the charge ramp is dv = (I/C)(dt). On a capacitor with ESR, the charge current must first overcome any internal resistance. Because voltage across a resistance changes instantly, the charge curve will be a straight vertical line on the waveform. After the resistance is overcome and the capacitance takes effect, a normal charge ramp results. The formula for this ramp is dv = (I/C)(dt) + IR, where R is the ESR. ESR is measured in the first instant of a charge ramp.

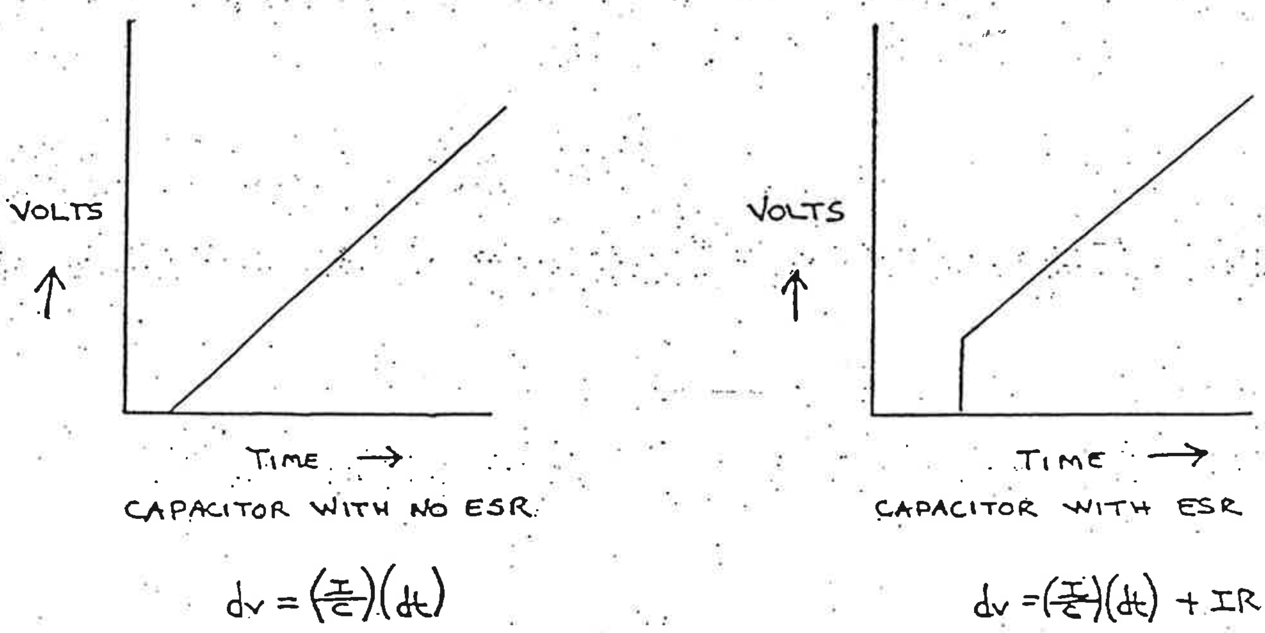

FIGURE 1

The current for charging the capacitor-under-test is derived from one of three constant current generators. The generator that will be selected is determined by the microprocessor just as the microprocessor controls the timing of the entire circuit. First the 10uS Pulse Generator is triggered. This generator then controls the current that is used to charge the capacitor-under-test. This capacitor is charged for 10uS. Immediately, after the charge cycle begins, a pulse generated by the .5uS Pulse Generator allows the Sample and Hold circuit to measure the voltage developed across the tested capacitor during the first .5uS of the charge cycle. At the end of the 10uS charge period, the selected current generator turns off and a transistor in the discharge circuit is turned on. The capacitor-under-test is then discharged and a new charge and discharge cycle is ready to begin. After the Sample and Hold circuit has measured and held and ESR voltage reading, it is then passed on to the A/D converter. The adjusted ESR voltage is then read directly as ESR in ohms.

INDUCTANCE BLOCK

Inductance measurements are made by supplying a constantly increasing current (ie..current ramp) through the coil under test and sampling the peak DC current across the coil. The constantly varying current causes a reverse EMF across the coil, according to the defining equation for inductance E = L di/dt. Therefore, by changing the constant di/dt for the different ranges, the reverse EMF is directly proportional to the inductance. However, when the current reaches its peak value, there is also an IR component in the voltage that is seen across the coil.

We then hold the peak DC current across the coil and measure this IR component. The voltage across the coil is supplied to two peak detectors by means of the inductance buffer, IC28. The Inductance Peak Detector measures and holds the voltage pulse across the coil during the time that the current is increasing. This voltage has a peak value of L di/dt + IR, where I is the peak current and R is the resistance of the coil. Now this peak current is held for a time, during which the Resistance Peak Detector stores the IR drop across the coil. These two stored voltages are then subtracted by the difference Amp IC28, so that we are left with only the L di/dt voltage, which is then measured by the A/D converter and microprocessor. We will look at this circuit in more detail when we get into the schematic.

RINGER BLOCK

In the LC102 ringer circuit, a pulse, triggered by the microprocessor and formed by TR17 and TR18, is fed to the coil under test. The ringing signal from the coil is detected, converted into TTL pulses, and finally counted by the microprocessor. Impedance matching is not selected manually, but instead, the microprocessor sequentially scans through four impedance matching capacitors and displays only the highest ringing value. All of the guess work of which impedance match is to be used is removed by allowing the microprocessor to make the decision.

The level at which the LC102 quits counting rings is determined by the selection of the front panel component type switches. At least one of the lower three component types must be selected or an Error 1 will result. With Coils or Switching Transformers selected, the LC102 counts all of the ringing pulses received from the coil. When the Yokes and Flybacks component type is selected, only the top 75% of the received ringing pulses are counted. The ringer counting circuitry cuts off at the 25% level.

FRONT PANEL AND DISPLAY BLOCK

The LC102 front panel board provides two very important functions. It allows information and control to be entered into the unit and displays processed information for user interpretation. Input to the LC102 is accomplished on a 8x5 membrane keyboard. This keyboard is scanned by the microprocessor.

There are two LCD displays on the front panel of the LC102. One is a 6 digit and is used for displaying entered value and all test values and results. The other is a 4 digit and is used to constantly display the voltage that is entered for the leakage supply. The two displays can be tested by accessing a display test routine. This routine is called by holding the On/Battery test and pressing the CLR button at the same time.

There are also 9 LED's, which are used to indicate component type selection, and two flashing LED's. One is used to warn the user when >25 volts has been entered into the leakage supply. The other flashing LED is used, in conjunction with a buzzer, to warn the user of possible shock hazard should the test lead fuse ever blow.

CIRCUIT DESCRIPTION

POWER SUPPLIES

Now, turning to the schematic of the Power Supply Board, let's discuss in detail the circuitry associated with the two power suplies used in the LC102. The PA251 Power Adaptor is connected to the terminal marked AC. Here, the 18 volts delivered by the power adaptor is passed through CR25 and additionally filtered by C14 and C16. The 14.5 volt regulator is composed of IC5, and LM317T Adustable Regulator and its associated control resistors. R40 is adjusted for a regulator output of 14.5 volts. CR16 and R45 make up the battery charging section which will charge the BY234 when installed. Also note that at the AC input, there is a line sync generator made up of TR9, TR10, and several bias resistors. The circuit tells the microprocessor when the AC Power Adaptor is connected and whether or not to incorporate the auto off function. The main power switch FET (TR15) is used to pass the battery and/or power adaptor voltage to the switching section of the main supply. A FET is used here to allow not only standard on/off control by SW1, but also microprocessor controlled auto off capabilities. The battery voltage is passed through CR18, a 3 amp Schottky diode for low forward voltage drop, and the AC Power Adaptor voltage is passed through CR17.

A Pulse Width Modulator (IC4) is the central control of the main switching power supply. The supply operates as follows: Current pulses are generated in T2 by the switching of TR13 and TR14 as dictated by the output of IC4, pin 10. Voltage is then developed across T2's secondary and is rectified and filtered. The positive voltage is rectified by CR23 and filtered by C26 and C28. The negative voltage is in turn rectified by CR24, filtered by C25 and C27, and regulated to -5 volts by IC7. The positive voltage is fed back to Pin 1 of IC4, a non-inverting input of an internal op-amp comparator. At Pin 14, there exists an accurate 5 volt reference. This reference, passed through R56 is fed into the inverting input of the internal op-amp. R50 and C31 provide feedback for stable operation. The Pulse Width Modulator does just as its name implies; it controls the width of the pulses that are generated in T2's primary. When the pulse width is wide, a larger voltage is developed across T2's output thus creating a larger rectified DC voltage. When the pulse width is narrow, just the opposite happens. A narrow pulse width produces a lower voltage output on T2's secondary. The output pulse width of IC4 is then automatically adjusted until the 5 volts that is fed back from the rectified secondary output equals that of the internal 5 volt reference. Once the output has settled to 5 volts, the pulse width will remain constant, changing only for variances in load current, which must be compensated for to maintain a stable and accurate output voltage. The circuit runs at a frequency of around 27 KHz as is determined by C20 and R51. There is also a reference voltage at Pin 4, labeled as dead time. This reference voltage determines the maximum duty cycle that the output pulses can achieve. If the duty cycle would become too high (ie...not enough off time) the transformer (T2) would become saturated. Minimum dead time prevents this from happening. Looking to the switched side of T2 (the primary winding) we see that this "flyback" voltage is also rectified and filtered by CR21 and C21. The voltage developed at this point is used to supply the 18 volt regulator and also to keep the main switch FET turned on as the voltage across the gate must be kept higher than the voltage present at its source. Zener diode CR20 limits the amount of voltage at this point to 15 volts above the normal 12 volt supply line. This not only keeps the voltage from running too high for the filter capacitors and 18 volt regulator, but also protects TR14 from transients developed across the primary of T2 by dumping the energy back onto the 12 volt line. TR11 is normally held on by the microprocessor which in turn keeps TR12 turned off. When the auto off sequence begins, the microprocessor allows TR11 to turn off thus allowing TR12 to turn on. Now that the voltage which is normally kept TR15, the main switch FET turned on, is removed, the switch turns off and removes from the power supply and LC102 circuitry.

Using 11 to 13 volts to produce an output that if capable of 1 to 1000 volts at 6 Watts, the leakage supply incorporates much of the same technology that is used in the main supply. Here, a Pulse Width Modulator (IC3) controls and regulates the output voltage via a closed loop feedback system. The start of the loop is a flyback switching transformer and associated switching circuitry. When IC3 switches from 0 to 12 volts, a charge is dumped into TR4, thus turning it on. This in turn causes the current to flow in the primary of T1 and creates a magnetic field. When IC3's output drops back to 0 volts, TR3 is turned on which in turn pulls the charge out of TR4, thus turning it off. TR3 is used to aid in the turn off of TR4 for faster and more reliable switching action. When TR4 turns off, current stops flowing in the primary of T1 and the magnetic field collapses. This action induces current in T1's secondary. The output of T1 is then rectified by CR8 and CR9 and then filtered by C10, C11, C13, C32, and L1. The rectifying and filtering section is balanced by R27, R28, R29, R30, and R31.

Output voltage selection is achieved by selecting a reference current via Digital-to-Analog Converter on the main board. The D/A Converters are microprocessor controlled and will be discussed later. By setting a reference current at the D/A control pin, it takes a certain output voltage to produce a corresponding current through R32 and R33 that will offset the reference current and end up with a respective reference voltage. The D/A outputs and IC2 are protected against excessive voltage by CR13, CR14, and CR15.

The reference voltage, located at the D/A control pin, is buffered by IC2b and summed with a calibrated reference voltage buffered by IC2a. This calibrated reference voltage is adjusted by R69 and is set during power supply calibration. The summed voltage, located at Pin 8 of IC1 is peak detected to keep any ripple and/or noise on the supply output below the selected output voltage. The peak detector voltage is then referred to as the conditioned output reference voltage.

Pin 14 of IC3 produces a stable and accurate 5 volt reference. This reference passed through R10 and CR4, is compared to the output voltage reference. If the output reference voltage is lower than the reference voltage, IC3 increases the pulse width which in turn increases the output voltage. When the reference voltages are equal, IC3 lowers the pulse width and continues to adjust it in order to keep the output voltage constant.

The leakage supply is initially turned on and off by a control line from the microprocessor. When 5 volts is applied to the base of TR1, through R15, TR1 conducts thus lowering the voltage at Pin 16 of IC3. This voltage is then below the voltage on Pin 15 and the supply begins to turn on and come up to voltage. When the microprocessor control line goes to ground, TR1 turns off allowing Pin 16 to rise to 12 volts and thus turning off the output of IC3. Another thing that happens during turnoff is that TR8 turns on and discharges the output filters through the active load, which will be described later.

While the supply is initially turning on, the output voltage is rising at a fairly fast rate. Just as the output reaches full voltage, TR7 is momentarily turned on to slow the output voltage rise by drawing 33 times the normal current through the active load. This keeps the output voltage from overshooting the entered voltage. The control of this operation comes from IC1a after comparing the output reference voltage and a value just above the main reference voltage.

The active load is a very important part of the leakage supply. First, in order for a switching supply to operate correctly, it must have some amount of load on its output. The active load used here keeps a constant load of about 200uA on the power supply, no matter what the output voltage is set to. The active load also keeps the supply from overshooting and discharges the filter capacitors when it is shut off as mentioned before.

The active load operates as follows; Five volts is fed to the gate of TR6 via R22. This voltage turns the FET (TR6) on, which in turn develops a voltage across the 100K source resistor (R24). This voltage is around 2 volts, which equates to a 200uA load (2v/100K = 200uA). Because there is a balanced condition between the voltage on the source and the gate voltage, any change in output voltage will reflect in a corresponding change in FET resistance to keep the voltage across R24 constant.

As the voltage on the drain of TR2 rises, the source will follow because the FET is turned on via R23. The voltage at the source of TR2 is limited to approximately 400 volts by CR6 and CR7. This distributes the high voltage between the two discharge FETs.

The discharge load (R25) and the overshoot load (R26) are selected via TR8 and TR7 respectively. The reason that the heavier loads work is that TR6 will turn on as hard as necessary to develop a balanced voltage across the "load" resistors R24, R25, or R26; whichever is selected.

The supply is current limited by the circuit consisting of TR1, R21, and R35. When the voltage drop across R35 becomes greater than .6 volts, TR2 begins to conduct and raises Pin 3 of IC3. When this feedback pin is pulled high, the Pulse Width Modulator decreases the pulse width and in turn limits the output voltage.

CAPACITANCE CIRCUIT DESCRIPTION

To measure capacitance the LC102 uses 1 of 4 current sources and applies this constant current to a capacitor, measuring the time it takes for the voltage to pass between two predetermined points. The lowest two current sources are simple transistor switches, applying 5 volts to a calibrated resistor network. Here, 5 volts charges the capacitor under test through 1.52 Meg +/-50K (R55 & R56) adjustable resistance for the 3.3uA current source and through a 15.2K +/-500 ohm (R59 & R60) adjustable resistance for the 330uA current source. The 60mA is controlled by IC22, Pin 14, and incorporates IC41, a LM317T voltage regulator, as an adjustable current source. The 60mA from IC41 is passed to the capacitor under test by CR25 thru CR30. The 416mA source funtions as more than a current source. First, it uses as its current source driver, a LM317T (IC24) voltage regulator and is adjusted by R81. Its primary turn on signal is derived at IC23, Pin 1. IC4 and CR31 limit the maximum voltage that the 416mA current source can achieve to 3 volts. Two more sections of IC23 are used not only to control the current source, but also to force the voltage at the current source's output to follow the voltage present on the leads (ie. track the output). This is done to keep the internal capacitance of CR14 from affecting capacitance readings. During the pulse test for Double Layer capacitors, the 3V limit is removed from the 417mA source and the pulse voltage limit is allowed go as high as approximately 8 volts. This is done to help overcome the ESR associated with these types of capacitors.

The upper and lower voltage trip points are determined by the voltage on Pins 5 & 9 of IC27, a LM319 high speed comparator. The lower trip point, Pin 5 of IC27, is normally held at 1V by resistor divider network R161 & R76. When TR40 is turned on by the microprocessor, the lower trip level becomes .5V and when TR41 is turned on, the trip level becomes .25V. Only TR40 or TR41 is on at one time, never both. On Pin 9 of IC27, the upper 3.5V trip level resides. This voltage is set by R74 & R164, and when TR16 is turned on by the "F" latch, the upper trip level is lowered to 1.75 volts. R71 is used to calibrate this voltage.

During the charging of the CUT, IC27 serves as a window comparator, allowing 6MHz to pass through 1/4 of IC25, only during the time that the voltage across the capacitor is between the two "window" voltages. This 6MHz is passed during this time, through IC25 & IC13 to IC31, where it is divided down for the input to the microprocessor, T1. The input pulses counted at T1 and left over in IC31 are used for the capacitance calculations. During the time between ranges, TR15, as controlled by the microprocessor, discharges the CUT.

D/A CIRCUIT DESCRIPTION

The 416mA current source is the same as that used in the capacitance measuring section. During the initial phase of the test, 416mA is passed through relay L9 to the test leads and on to the CUT. After the two second charge time, relay L9 releases and relay L1 engages. Discharge FET TR8 is turned on and the capacitor discharges for 2 seconds. TR8 is then turned off and L1 is released. After 2/3 of a second, the voltage on the cap is measured via a high impedance buffer, IC33. R33, adjusting the offset of IC33, is used to calibrate the D/A readings. The output of the D/A input buffer is fed to the A/D converter IC14, via the A/D input selector, IC15.

LEAKAGE CIRCUIT

Part of the leakage measuring system is the leakage power supply which has been previously covered. But, part of the leakage supply which was not covered is the digital-to-analog converter which sets up a reference current that the supply uses to determine what the output voltage will be. When a valid voltage is entered via the front panel keyboard IEEE, the LC102 microprocessor calculates what code must be sent to the D/A converter. This code is latched by IC35 for the MSB and IC37 for the LSB. In order to cover the full range of 1 to 999.9 volts in .1 volt increments, two D/A converters must be used. Two D/A converters give a resolution of 16 bits. The MSB D/A converter's maximum output current is .5ma and it is trimmed by R201. The LSB D/A converter's output current is 2uA and it is trimmed by R202. These pots are adjusted during the leakage supply voltage calibration. The two D/A converters are combined by tying their outputs together.

When measuring leakage current, one of four automatically selected ranges are used to set the gain of the current-to-voltage converter made up of IC43 and its associated circuitry. When the leakage button is pressed, the microprocessor starts the current voltage converter in the highest range by engaging L5 and connecting the 10 ohm resistor (R171) into the feedback loop. Also, the output of IC44 is connected to the A/D converter (IC14) via the A/D input selector (IC15). If the microprocessor reads too low of an input for that range, it will range down until the reading is valid or the bottom range is reached. As the unit ranges downward, it will sequentialy select R172 (100 ohm), R177 (1.1K), and then only R178 (10K) for the lowest range. Also, during the leakage test, L4 is engaged which diverts the return current from ground to the I/V converter.

The following table shows which resistors and relays are used for each particular range:

RANGE	RELAY ENGAGED	RESISTOR USED	CURRENT RANGE
1. Highest	L5	R171, R178	2mA-20mA
2.	L6	R172, R178	200uA-1.9mA
3.	L7	R177, R178	20uA-199uA
4. Lowest	None	R178	0uA-19.9uA

TABLE 3

Troubleshooting hint: If the unit reads several mA with no load connected and can not be calibrated out, L4 may be fused.

ESR CIRCUIT DESCRIPTION

During the ESR test, L1 is energized and any signal sent to or received from the leads is passed via this relay. At the start of the ESR test, the microprocessor sets Pin 5 of IC21, a 4066 bilateral switch, high and stores any initial voltage on the capacitor in C8. Pin 5 of IC21 drops low and a selected current source is turned on for a period of about 10uS. "F4" is also set high when a ramp is turned on. At this time, a 1uS pulse, generated by C10, R30, and IC20 is sent to Pin 6 of IC21 to sample the voltage developed across the CUT at the instant the current is applied. This voltage is then held in C12. Normally, the 1uS sample and hold pulse is delayed .1uS by R165 and C11, but when the highest range is used (200-2Kohm) the sample and hold pulse is delayed 5uS to sample further into the ramp. This additional delay, switched in by TR42, is incorporated because of the rounding of the leading edge of the current pulse due to internal capacitance and the high impedance of the generator.

After the resistance value has been stored, the D/A voltage value, stored in C8, is subtracted and the final ESR value is sent to the A/D converter (IC14) via A/D input select, IC15.

Under the control of the microprocessor, the three ESR ranges are sequentially stepped through, highest to lowest range. In between ranges, TR8 is turned on to discharge the CUT.

INDUCTANCE

The LC102 measures inductance by applying a current ramp to the coil under test, as described in the inductance circuit block diagram description. The current ramp is generated by IC26, C32, and one of the resistor networks selected by IC16, an analog multiplier. The ramp speed is determined by the resistor network value selected by the microprocessor. When IC16 selects one of its seven inputs, capacitor C32 begins to charge. As the voltage at Pin 6 of IC26 rises, it charges C32 and raises the voltage on Pin 2. Because Pin 2 is being pulled toward -5 volts, it opposes the current coming from C32. The rise of the voltage is then a linear ramp whose speed is determined by how hard Pin 2 of IC 26 is being pulled toward -5 volts and counteracting the rise of voltage caused by the charging C32. Knowing how this circuit operates, we can tell that R104 and R105 will produce the strongest current and opposition to C32, thus producing the steepest ramp. R111 and R117 being the highest resistance value will produce less opposition to C32 and consequentially, the slowest and most gradual ramp.

The selected ramp located on Pin 6 of IC26 is then fed to selected voltage-to-current converters via IC17, another 4051 analog multiplier. The selection of IC16 and IC7 is always identical to divert the current voltage ramp to its current voltage-to-current converter. Both are microprocessor controlled. When the top of the ramp is detected by comparator LM306 (IC29), two things happen. IC30, Pin 4 goes high and turns the range off. Also, at this time, IC32 is clocked producing a logic high on Pin 13 and low on Pin 12. The inductance sample and hold is then turned off, leaving the inductance sample stored in C37. IC30, Pin 3 goes high after a short delay set by R142 and C35, resistance of the coil is then sampled and held in C35. IC28d subtracts the resistance from the inductance value and sends the corrected inductance value to the A/D converter via the analog data selector, IC15.

Also, note that the output of IC28, Pin 7 is divided down by R152 and R154 and sent to the A/D converter. This point is used by the microprocessor to test if a high resistance across the leads exists, thus indicating an open coil.

During the inductance test, L8 is energized and the microprocessor sequences through the ranges (Range G to Range A) until a value reading is taken or range A, the lowest range, is reached. Figure 2 shows the waveforms across various points in the inductance measuring current.

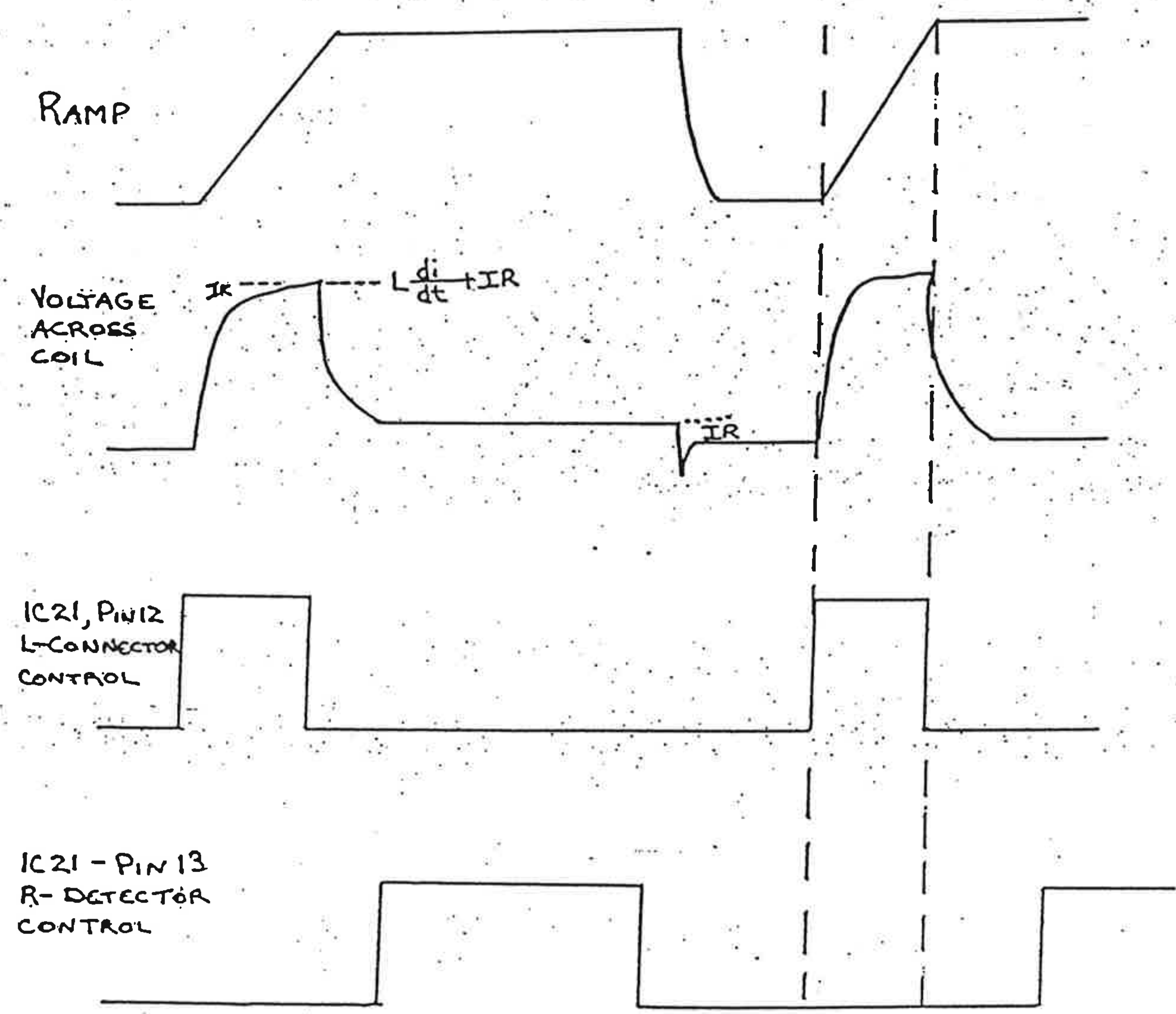

FIGURE 2

RINGER CIRCUIT DESCRIPTION

After the "Inductor Ringer" button on the front panel of the LC102 is pressed, (coils, yokes & flybacks or switching transformers must be selected), the microprocessor latch E4 is temporarily dropped from a high to a low state. This in turn causes TR17 & TR18 to conduct and send a 5 volt pulse through CR16 and on the test coil via energized L10. The returned pulses from the ringing coil are buffered by TR19 & TR20. The buffered ring signal is then squared by TR22. R95 is calibrated to bias TR22 into conduction. For the 25% cutoff level, R91, switched in by the microprocessor via TR21, is set so TR22 will count only the upper 75% of the incoming ring signal. The squared ringing signal passes through 1/4 of IC2 and 1/4 of IC13 and on to IC31, a HEF4040 binary counter. This counter stores the value of ringing pulses and is then emptied into the microprocessor timer/counter input pin, T1.

Auto ranging is accomplished by sequentially selecting the impedance matching capacitors C26, C27, and C28; storing the ring value; and displaying the highest value received. The impedance matching capacitors are switched by TR24, TR25, and TR26; and are under microprocessor control via the "F" latch.

FRONT PANEL CIRCUIT

The front panel board is connected to the main board with a 26 conductor ribbon cable. The front panel membrane switches are then connected to the front panel board via a separate flex cable. The keyboard is scanned by the microprocessor. Scanning is done by sequentially outputing a low to each column on the keyboard via a latch on the main board (IC40). During each column output, an input buffer on the main board (IC5) tests the rows of the keyboard to see if any have been pulled low. A low would indicate that a key has been pressed. The microprocessor also sends a pulse to the latch inputs of IC4 and IC5. This, in turn, latches the respective component type LED on.

The two LED displays receive their data from DB7 of the microprocessor. The main display and the voltage display each have their own clock which is used to put the data into the particular display latch. IC6 produces the backplane for the LCDs and also flashes the warning LED when instructed to do so by the microprocessor.

PROTECTION CIRCUIT

In order to protect the user from possible shock hazard, the LC102 incorporates a circuit to detect a blown test lead fuse and warn the user should such a condition ever exist. This circuit operates by passing 8 volts to the test lead (after the fuse) through CR42, CR43, and R218. If the fuse is good, the 8 volts will be dropped through R218 and approximately 0 volts will be delivered to pin 3 of IC48. However, should the fuse be blown, the 8 volts will no longer be shunted through R34 and R35 to ground, but will remain and be delivered to IC46, thus tripping the comparator and setting off the warning system. The warning system consists of a front panel LED and a buzzer which is pulsed. Should the >25 volt LED be flashing at the time when the fuse blows, that LED's flashing will stop as soon as the fuse warning LED begins to flash.