LC75 CIRCUIT DESCRIPTION

DVM CIRCUIT

The DVM circuit is used for three functions in the LC75, inductance, ESR, and leakage. The circuit functions as a ramp slope A/D.

The ramp generating circuit consists of IC2009, IC2008, IC2007, IC1038, and C2022. IC2009 is a -3.6V supply. IC2008 and C22 generate the ramp, IC2007 discharges C22, and IC1038 controls the timing of the circuit by feeding the input of IC2008 with the 'Q not output' and the gate of IC2007 with the 'Q output'.

IC2006 is the comparator of the circuit. The ramp is fed to pin 10 and compared to the voltage on pin 9. When the ramp voltage is equal to the input voltage the output, pin 8, toggles. The voltage on pin 9 comes from an absolute value circuit for inductance and ESR measurements. This circuit is used so the voltage fed to the comparator is always a positive voltage. The circuit consists of three op-amps. The input, which comes from the inductance and ESR measuring circuits, is pin 3 of IC2008. The voltage on pin 3 is reflected through the op amp to pin 2 which is connected to pin 6. Connecting them in this fashion insures that one of them will always have a positive output. The outputs are then coupled to the comparator through CR2031 and CR2030 insuring that only a positive voltage is coupled through. Also included in this circuit is the polarity driver. The inputs are fed by the outputs of the diodes and the output goes high or low depending on which one's high. One more feature of this circuit is the DVM zero. The DVM zero pot is fed to pin 5 of IC2008. This allows you to zero out any offsets in the circuit, so the display will read zero while no measurements are being taken.

The final circuit for the A/D is the counter. The counter for this circuit is IC1037. The output from the comparator, IC2006, is fed to the latch enable (LE) input of the counter, through the latch pass circuitry. When the counter gets a latch pulse the count in the counter is latched into the outputs of the chip. These outputs are multiplexed and are fed to the display driver.

COMMON PROBLEMS IN THE DVM CIRCUIT

Problem	Possible causes
Unit overanges with nothing pushed.	Check + and - 7V and - 3.6V. The outputs of IC1038 may not be getting to IC1008 & IC1007. If inductance and ESR are dead check for a glitch on the back of the ramp.

INDUCTANCE

The inductance circuit is basically four circuits. These are the ramp generators, the sample and hold circuit, -3.6V IR correction, and the inductance ramp peak control. The sample and hold circuit is divided into two parts, one part samples the inductance value, and one samples the resistance of the coil. These are summed in a difference amplifier to give the true value of the coil. The DVM circuit is also used in taking inductance measurements.

The inductance is basicly determined by hitting the inductor with a pulse that has a known rise time and amplitude. The voltage developed by the coil will then be proportional to the value of the coil. The Smaller the coil the Faster the rise time of the pulse.

To begin the measurement, we have to generate a ramp. The ramp generator circuits are slightly different for each range and are selected by IC's 2001 and 2002. This is a series of nand gates fed by the range control lines and a 60 hz. timing pulse. The 60 hz. is very important because it keeps all the circuits synchronized for taking the measurement. The ramp is then fed in two directions. One of the paths is to the leads and the other is to the ramp peak control circuit. The instant that the coil is hit with the ramp, it will develop a voltage because of the current surge. At that time we want to sample the voltage on the coil. This is accomplished by resetting IC2015 (a D type flip-flop) with the same 60 hz. timing pulse used to gate the ramp generator and feeding the 'Q not output' to the switch in the inductance part of the sample and hold circuit. When the amplitude of the ramp is equal to the reference voltage in the ramp peak control circuit it clocks IC2015 and the 'Q not output' goes low, turning off the switch in the sample and hold circuit. At the same time, we want to get a sample of the resistance of the coil. This is done by gating the switch for the IR part of the sample and hold with the 60 hz. timing signal and holding the voltage of the ramp at a constant voltage that is equal to the reference voltage on the peak control comparator. This is done by gating the - 3.6V to the ramp generators with the output of the comparator. The voltages in the sample and hold circuits are summed in the difference amp, and fed to the DVM circuit via the absolute value circuit. The lead zero voltage is also added to the resistance side of the summing amp when the unit is in the lowest range. The DVM circuit converts this to a count that is fed to the display. The count must be more than 90, unless it is in the lowest range. This is done with a 90 count detector in the latch pass circuitry.

COMMON PROBLEMS IN THE INDUCTANCE CIRCUITS

PROBLEM	POSSIBLE CAUSE
All ranges reading low.	Check 20V supply. Check the reference in the peak control circuit.
One range is dead.	Use a range locker and trace the ramp generator for that range.
Not enough range on the cal pot. One range reads high.	Check the capacitors and resistors for that ramp generator. It is sometimes nescessary to change the 2.7K resistor in series with the cal pot to 3.3K .
The inductance won't zero.	The poly cap in the lowest range may be bad.
	The gating signals in the sample and hold circuit may be missing.
	The sample and hold summing amp may have an offset in it.
	The sample and hold circuit may have an offset in it. This can be checked by trying to zero the ESR.
Inductance won't overrange.	Check to see if inductance will read anything. If it does not, take a reading. The output may be shorted, or the gating signal for the inductance side of the sample and hold may be missing.
	Check the reset line on IC1022 to see that it is not being reset at the wrong time.
	The overange line may not be getting to the display.
	If the display goes blank except for a decimal point check the overange blanking.

RINGER

The ringer circuit basically just hits the coil with pulse, and counts the number of times the coil rings. The coil should read at least 10 rings in one of the ranges to be considered good.

The ringer function has three basic circuits. These are the pulse generator, the impedance matching switch, and the counter. A pulse is derived on the digital board at pin 7 of IC1035. This pulse is used to gate on IC2007 causing a 7 volt pulse to be sent to the output. This line is also tied to the impedance matching switch. The rings on the line are then rectified and used to drive a transistor into saturation which gives a square wave which is used to clock the counter.

The ringer is calibrated in two positions. It is first caled in the first position and in the third position Rxx is put in parallel with Rxx changing the bias on TRxx and is used to cal the upper four positions.

ESR

ESR is equivilant series resistance. This parameter of a capacitor is used primarily for large filter caps, where a large series resistance would inhibit the filtering action of the capacitor.

When voltage is first applied to a capacitor, it has maximum current flow. During this time we can assume that any voltage developed accross the capacitor is proportinal to the ESR of the cap. At this time we can sample the voltage accross the capacitor and determine its ESR.

The timing of the ESR measurement is very critical so a 60 hz. timing signal derived from the line is used to keep everything in sync. IC2004 is used to shape the timing signal into pulses to gate on the pulse generators. It is also used to shape a pulse of approximately 5 microseconds used to gate the sample and hold circuit as soon as the pulse is generated. Pin 3 of IC2004 goes to TR22 which is used to discharge any voltage stored on the cap before the next sample is taken.

The voltage for the ESR zero pot is taken from the wiper of the lead zero pot. This voltage is buffered by part of IC2006. Another part of IC2006 is used to buffer the voltage on the sampling cap. These two voltages are then summed in a difference amp and fed to the absolute value circuit and then to the DVM circuit. The voltage on the output of the difference amp is directly proportional to ESR of the cap. This easily seen by looking at how the resistances in the voltage divider, consisting of the resistors on the ramp

generators and the capacitor being tested are set up in multiples of 20, the voltage used to generate the pulses, and the xxrangexx of each range.

The ESR circuitry also includes a circuit used to insure that the unit will range down to the C range, the highest ESR range, before taking a reading. This is necessary because offsets in the circuit may exceed .09V which would cause a count to be latched to the display since we are using the 90 count detector in the latch pass circuitry. The circuitry used to prevent this holds the sample and hold side of the summing amp at ground, unless the unit is in one of the ESR ranges.