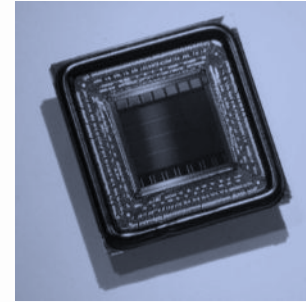

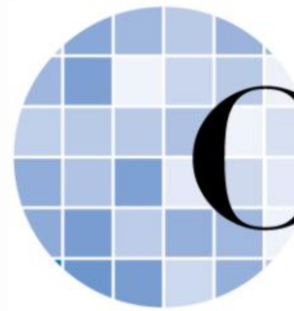

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Technology Updates Brief

February 2012

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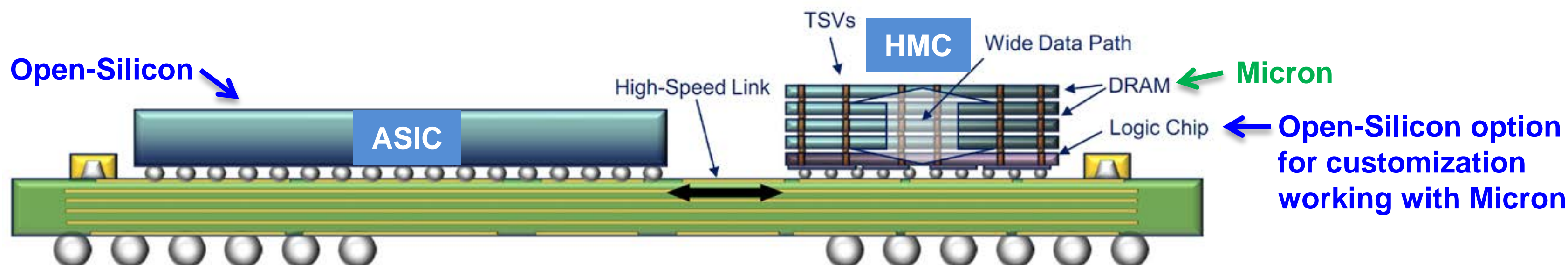
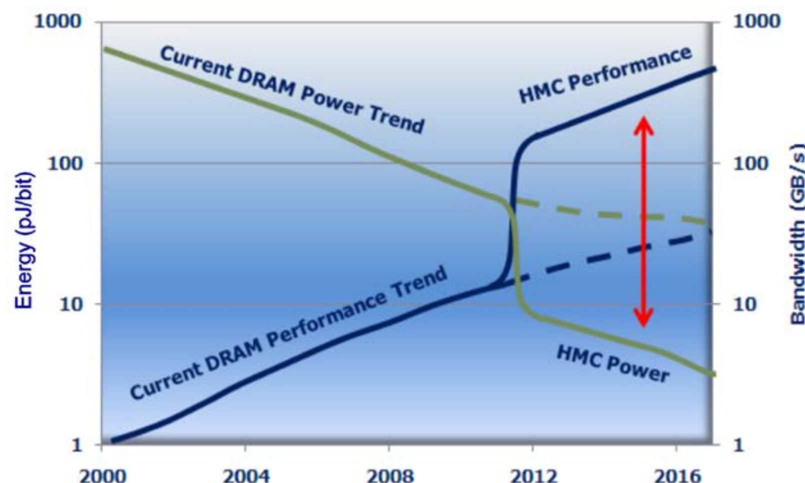
Hybrid Memory Cube (HMC) with Micron

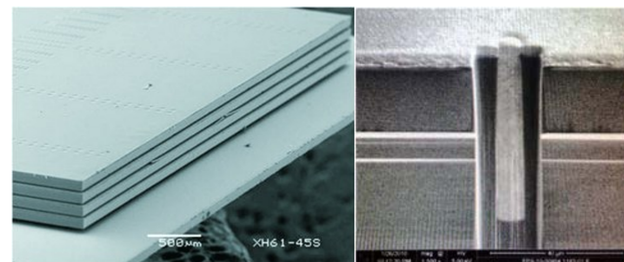


▶ HMC Benefits:

- ∼20 times the performance of a DDR3 DIMM
- ∼10% of the energy per bit compared to current DIMMs

	Bandwidth	Power	W / GBs
DDR3-1333	10.66 GB/s	5.52 W	518 x
DDR4-2666	21.34 GB/s	6.60 W	309 x
HMC (4 DRAMs)	128.00 GB/s	11.08 W	87 x





4 DRAM chips stacking   Through Silicon Via

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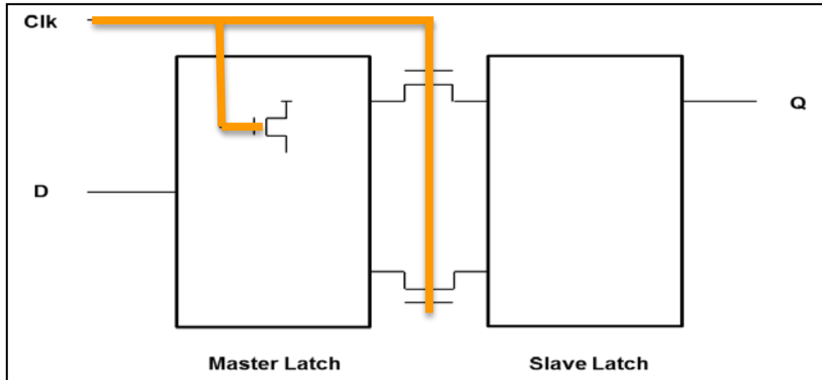
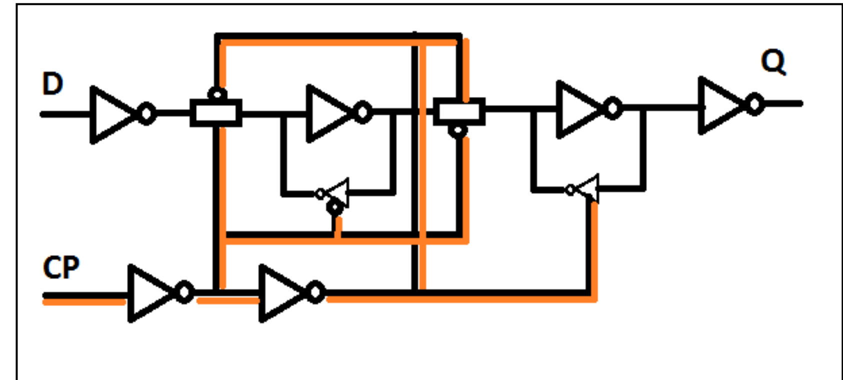
PowerMAX: New Flip-Flop Architecture

New Flip-Flop



Conventional Flip-Flop



- **New flop design Benefits:**
  - Lower CLK pin internal Power
  - No silicon area penalty
  - Can replace existing flops
  - Faster CLK to Q (output) delay

Test Case in TSMC 40nm Design	Effectiveness
Flops Swapped	76%
Clock pin Power Reduction	42%
Total Dynamic Power Reduction	9.2%

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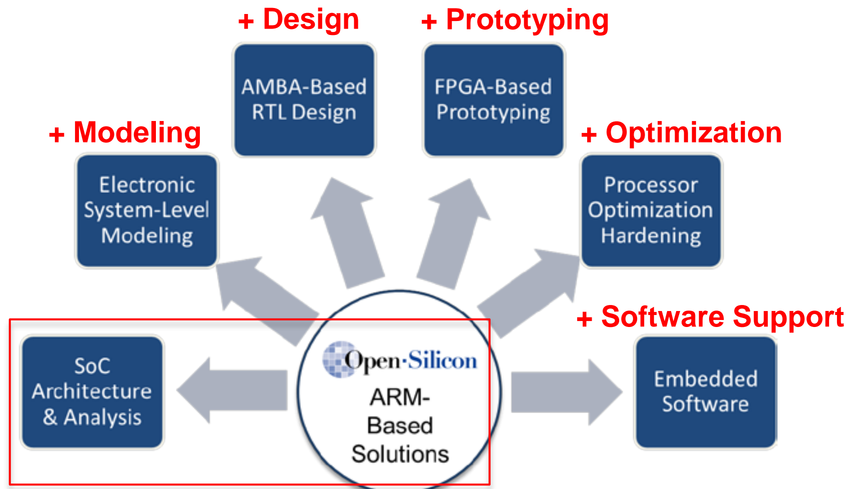
Expanded support for ARM processors



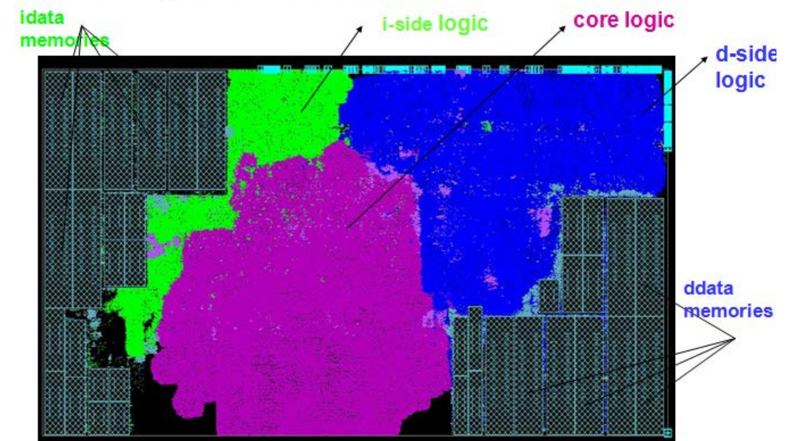
Not only ARM inside ASIC development

Portion of Currently Running ARM Projects

ASIC Design	Processor	Core	Technology
Home G/W	Cortex A9	Dual	GF 28SLP
Networking	Cortex A9	Quad	TSMC 40LP
Entertainment	Cortex A9	Dual	TSMC 40LP
Storage	Cortex M0	-	TSMC 65G
Storage	ARM 968	-	GF 40LP
General	Cortex A9	Dual	TSMC 28HPM
Reference	Cortex A9	Single	TBD
Industrial	Cortex M3	-	TBD
Host CPU	Cortex A9	Dual	TBD

- **Example: Hardening Core**
  - Quad-Core Cortex A9
  - 32/32KB L1, 128KB L2, SCU
  - TSMC 40LP, 8LM
  - POP w / HS LVT L1 SRAMs, RVT L2 SRAMs
  - 7% OCV margin, 50ps clock uncertainty
  - 10.94mm2
  - Achieved Frequency
    - 890MHz (@ wc, 0.99V, -40/125C)
    - 950MHz (@ wc, 1.08V, 125C)
  - Power:
    - 1.5W (Dynamic), 25mW (Leakage)
  - Design TAT: 16 weeks

CA9 Single Core Floorplan



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