

## 4.1.2 – SERIAL PRESENCE DETECT STANDARD, General Standard

Introduction: New memory technologies are continually being introduced to the industry. As these new technologies are considered, the need for expansion modules becomes evident; consequently, new memory technologies are being incorporated onto existing module form factors. Unfortunately, upon a module's first implementation, the module designer is often unable to predict all of the (as yet unreleased) memory technologies which would eventually be used on the module form factor; hence the parallel Presence Detect method did not allow for these newer technologies. Given that memory modules do not regularly change form factor when a new memory technology is implemented, a Serial Presence Detect (SPD) method should be available and predefined so that it can be considered for new memory modules when needed.

- 1 Scope:** This standard defines the means to implement a Presence Detect (PD) scheme serially. This Serial Presence Detect (SPD) standard is intended for use on any memory module independent of memory technology or module form factor. At the point of standardization of any given memory module, SPD being defined within this standard, may be easily implemented if so chosen. The body of this standard will depict generally how SPD is implemented; this will be independent of the module's memory technology.

When a specific memory technology is being depicted (e.g. Fast Page Mode DRAM), an appendix to this standard will be added describing the characteristics, features, and attributes of that memory technology needed for Presence Detection. The entire address map of the SPD scheme must be presented in each appendix.

When a new module form factor implementing SPD is standardized, the (proposed) standard for that module must also include the following information pertinent to the SPD:

- SPD Interface protocol (see section 2 herein)
- Acceptable module configurations,
- Legitimate architectures: depth, width, #banks, addressing
- Acceptable error checking schemes (ECC, Parity...)
- SPD Wiring diagram and pinout to module.

**NOTE: All writable memory modules that include a Serial Presence Detect (SPD) feature must also support "Page Write" operations of at least 4 sequential addresses.**

- 2 Interface Protocol.** Upon the development/standardization of a new module form factor incorporating SPD, the SPD interface protocol will be defined. As long as that module form factor is used, this protocol must remain constant. Examples of SPD interface protocol include IIC, Microwire, etc. The physical implementation (pinouts etc.) must also be defined in the standard for the module form factor if it implements SPD.
- 3 Data Order and PD Size:** This document will present the order in which the PD bytes should follow. It also defines how many bytes must be used to define a given PD; in most cases it will be one byte per PD. The SPD address map is fixed upon selection of any given fundamental technology, this includes all required and optional data; when a fundamental memory technologies' PD bits are defined, then the entire address map for those SPDs must also be defined.
- 4 SPD Data Types:** SPD data is stored in a non-volatile serial memory device. The different types of data include, but are not limited to:
  - Look Up Table entries
  - Binary data
  - Optional data (Binary, ASCII, etc.)
  - Checksums
- 4.1 Look Up Table (LUT) Entries:** Much of the SPD data is organized as a series of table entries. Each table entry contains one or more bytes of information. Each table entry represents one particular characteristic pertinent to the memory module; e.g. fast page mode DRAM will have specific tables for tRAC, tCAC, # of banks, number of row addresses, number of column addresses, error detection/correction, refresh rates, data width, and interface standard. Each table entry corresponds to a position on a look-up-table specified within an appendix within this standard. The number of bytes (one or more) needed to express a particular aspect of the module is fixed and defined in this standard or in one of its appendices.
- 4.2 Optional Data:** The current Jedec Standard allows for manufacturers to insert some of their own specific data into the SPD EEROM. This data includes manufacturer ID, manufacturers' module serial numbers, and other ASCII, Binary Coded Decimal, or binary data.

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**4.3 Checksums:** In various cases, checksums are required. This procedure applies to all situations where a Checksum is required. Checksum calculation method is as follows:

- 1) Convert binary information, in byte locations 0 to 62 to decimal
- 2) Summ all decimal values for locations 0 to 62.
- 3) Divide "sum" by 256.
- 4) Convert remainder to binary (will be less than 256).
- 5) Store result (single byte) in location 63 as 'Checksum'.

\* NOTE: The same result can be obtained by summing the binary values in locations 0 to 62, and eliminating all but the low order byte. The low order byte would be the 'checksum'.

Example

SPD Byte Address	Serial PD		Convert to Decimal	
0	0010 0100	⇒	36	
1	1111 1110	⇒	254	
2	0000 0000	⇒	0	
3	0000 0000	⇒	0	
–	–	–	–	
–	–	–	–	
–	–	–	–	
V	0000 0000	⇒	0	
60	0000 0000	⇒	0	
61	0000 0000	⇒	0	
62	0000 0000	⇒	<u>0</u>	
			290	(Sum of all Decimal values)
			290/256	(Divide by 256)
				= 1, with a remainder of 34
			34	(Keep remainder)
			0010 0010	(Convert remainder to Binary)
63	0010 0010			Store Checksum in address location #63

**5 SPD Content:** The Serial Presence Detect standard calls for various features and items to be defined. Specifically, the following must be addressed in any SPD implementation:

Description	Data Type	Address Map Byte #
SPD size	LUT Entry	0
Total SPD memory size	LUT Entry	1
Fundamental memory type	LUT Entry, Appendix A	2
Definition of features specific to the fundamental memory	See pertinent appendix	3–XX
↓	↓	↓
(Optional) Superset memory type	See appendix B	XX–60
(Optional) definition of features specific to the superset memory	See pertinent appendix	33–61
SPD Revision designator	LUT	62
Checksum for bytes 0–62	Checksum	63
Manufacturers Jedec ID code per JEP–106	LUT	64–71
Manufacturing location	Supplier Unique	72
Manufacturer's Part Number	Supplier Unique	73–90
Revision Code	Supplier Unique	91–92
Manufacturing date	BCD	93–94
Assembly Serial Number	Supplier Unique	95–98
Manufacturer Specific Data	Supplier Unique	99–125
Reserved	N/A	126–127
Open free–form area	Application Specific	128–255

Detailed descriptions follow in paragraphs 5.x

**5.1 Byte 0, Number of Bytes used by Module Manufacturer:** This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data:

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

**5.2 Byte 1, Total SPD Memory Size:** This field describes the total size of the serial memory (often an EEPROM) used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

- 5.3 Byte 2, Fundamental Memory Type:** This field will identify the fundamental type of memory. The fundamental type of memory may include Fast Page Mode DRAM, EDO DRAM, Masked ROM, EEPROM, Synchronous DRAM, etc. The table listing all the types of Fundamental memory is contained in **appendix A** herein. New fundamental types can be added to this table anytime after standardization of a fundamental memory type. Note that if a given new technology is completely backward compatible with pre-existing technology, then it should be considered a Superset technology and so described as detailed (in paragraph 5.5) within this standard.
- 5.4 Bytes 3–31:** Descriptions of Module Specific Features: Appendices to this standard detail the tables for the features specific to each of the fundamental memory types as described above. For example, see appendix C for details of SPD features for Fast Page Mode and Extended Data Out DRAM Modules.
- 5.5 Byte 32:** Superset Memory Type: When a new technology is developed which is completely backward compatible to an already specified (fundamental) technology, then it may be considered a 'Superset' technology. The benefits of specifying a technology as a superset are obvious; if a system is capable of operating in a 'fundamental' mode only and a superset module is inserted, then the system can still use the module. The memory superset type or technology is specified in appendix B to this standard. Appendix B provides the decode of specific superset technologies. It references other appendices where the specific superset PDs are further detailed. As new supersets are created, appendices must also be added. Presence Detects for a superset technology are specified just as for any given fundamental technology except that any and all backward compatible fundamental technologies must be referenced.
- 5.6 Bytes 33–62:** Superset Features: Appendices to this standard detail the tables for the features specific to each of the superset memory types as described above. A new appendix must be added to this standard detailing the PDs for that superset technology detailed in appendix B and represented in byte 32. Appendix B would identify the superset technology type and would also reference the appropriate appendix where the superset is detailed.
- 5.7 Byte 63:** Checksum of Bytes 0 to 62 as defined in par. 4.3
- 5.9.0 Bytes 64–127:** Module manufacturers may include information which is pertinent to their particular modules. This information is detailed below in paragraph 5.9.X:
- 5.9.1 Bytes 64–71:** Manufacturer's Jedec ID code per EIA/JEP106. Manufacturers of a given module may include their identifier per JEDEC spec EIA/JEP106. 00h is not allowed in bytes 64 to 67 (bank 1) and a 7Fh (continuation code) indicates that the manufacturer's code is beyond the limit of this field and will reside in bytes 68 to 71 (bank 2). 00h or FFh may be used in bytes 68 to 71 if they are unused.
- 5.9.2 Byte 72:** Manufacturing Location. Manufacturers may include an identifier which uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.
- 5.9.3 Bytes 73–90:** Manufacturer's Part Number: Manufacturers may include their part number in 6-bit ASCII format within these bytes.
- 5.9.4 Bytes 91–92:** Revision Code: This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.
- 5.9.5 Bytes 93–94:** Date of Module Manufacture: The module manufacturer may include a date code for the module. If this is done, then specifically, byte 93 must contain the year in Binary Coded Decimal (BCD) and byte 94 must contain the week in Binary Coded Decimal (BCD).
- 5.9.6 Bytes 95–98:** Module Serial Number: The supplier may include a serial number for module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.
- 5.9.7 Bytes 99–125:** Manufacturers specific data, open area. The module manufacturer may add any additional information desired into the module within these locations.
- 5.9.8 Bytes 126–127:** Reserved. These bytes are reserved and cannot be later allocated.
- 5.10 Bytes 128–255:** System Integrators specific information: The system integrator may choose to use the SPD ROM for various items. If so, then bytes 128–255 may be used.