

# DDR4 DIMM Slot Compliance Interposer

## Flexible Command Timing Compliance Validation

- Cost Optimized visibility
- Passive 284-pin DIMM Slot Interposer
- Address, Command and Control Timing with Command Decode
- Automated Logic Analyzer Setup for fast Time-to-Data
- DDR4 Compliance Analysis S/W (optional)



## Overview

Nexus Technology recommends DDR4 slot interposers for applications where the customer must have the greatest flexibility for probing of different DDR4 DIMMs.

This interposer is an extender design and does not require a dedicated DIMM slot. The logic analyzer connects above the standard DIMM height so that there is no mechanical interference with adjacent DIMMs.

This is a passive interposer with no added buffers to conceal system performance.

## Performance You Can See™

Sample	Timestamp	NewFilter_NEX_COMM	NewF_NEX	NewFilter_NEX_CO	NewFi_NEX
3545	9.004 ns	RANK 1	RD	Bank 5	03C0
3581	54.024 ns	RANK 1	PRE	Bank 5	0000
3584	4.472 ns	RANK 1	ACT	Bank 7	3010
3593	13.536 ns	RANK 1	WR	Bank 7	03B8
3597	6.015 ns	RANK 1	WR	Bank 7	03C0
3599	2.969 ns	RANK 0	PREA	Bank 0	0400
3609	15.000 ns	RANK 0	PRE	Bank 0	0000
3634	37.500 ns	RANK 1	ACT	Bank 5	3090
3641	10.508 ns	RANK 1	PRE	Bank 7	0000
3643	3.008 ns	RANK 1	RD	Bank 5	03C8
3649	9.023 ns	RANK 1	RD	Bank 5	03D0
3686	55.469 ns	RANK 1	PRE	Bank 5	0000
3688	3.008 ns	RANK 1	ACT	Bank 7	3010
3697	13.535 ns	RANK 1	WR	Bank 7	03C8
3701	5.996 ns	RANK 1	WR	Bank 7	03D0
3739	56.992 ns	RANK 1	ACT	Bank 5	3090
3746	10.488 ns	RANK 1	PRE	Bank 7	0000
3748	3.008 ns	RANK 1	RD	Bank 5	03D8
3754	9.004 ns	RANK 1	RD	Bank 5	03E0
3791	55.508 ns	RANK 1	PRE	Bank 5	0000
3793	3.008 ns	RANK 1	ACT	Bank 7	3010
3802	13.515 ns	RANK 1	WR	Bank 7	03D8
3806	5.996 ns	RANK 1	WR	Bank 7	03E0
3844	56.993 ns	RANK 1	ACT	Bank 5	3090
3851	10.488 ns	RANK 1	PRE	Bank 7	0000
3853	3.027 ns	RANK 1	RD	Bank 5	03E8
3859	8.985 ns	RANK 1	RD	Bank 5	03F0
3896	55.488 ns	RANK 1	PRE	Bank 5	0000

Figure 1 State Display of Command, Address, & Control



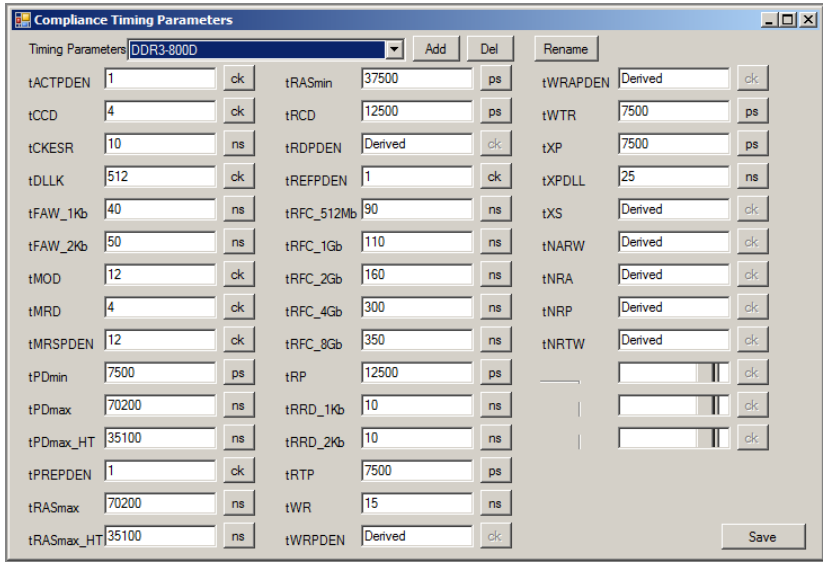
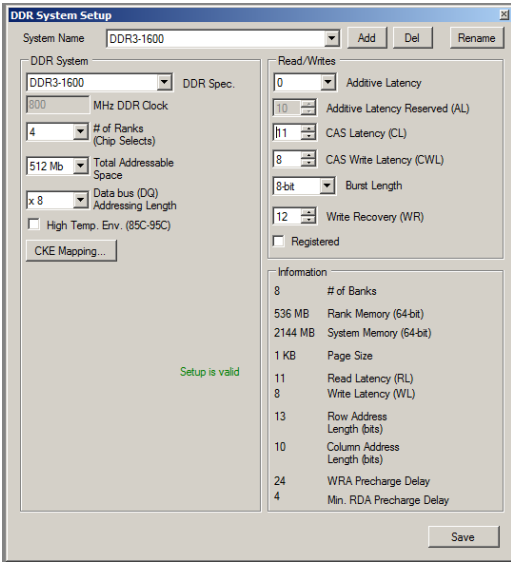
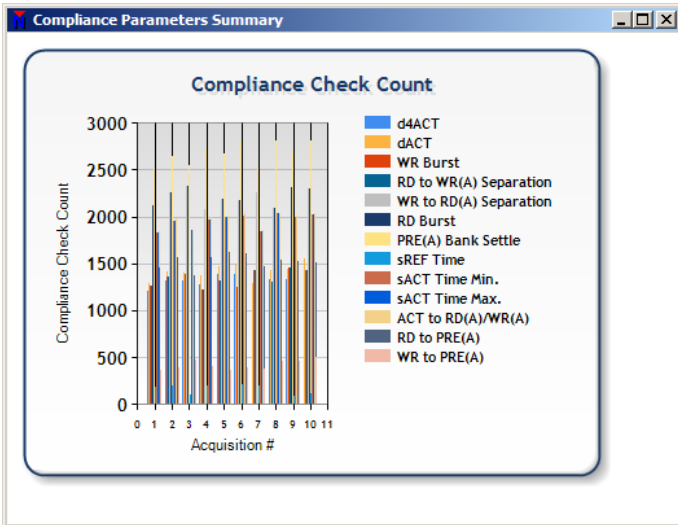
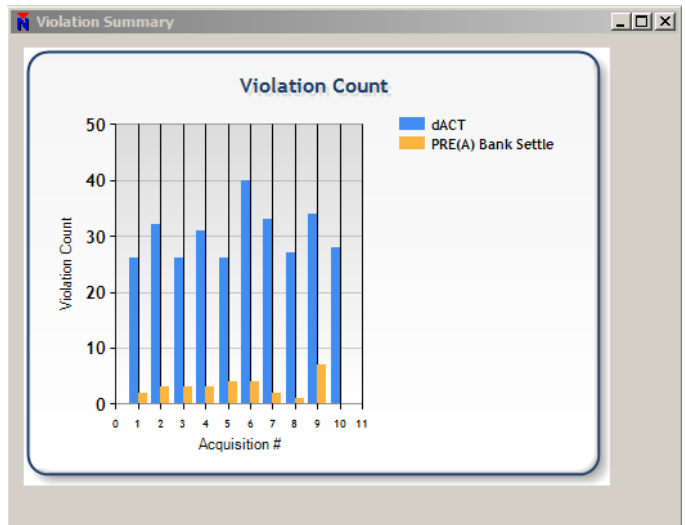


Figure 3 Compliance Analysis S/W Easy Setup



Shows the distribution of commands that were compliance checked



Shows the distribution of commands that violated the spec

Figure 4 Compliance Analysis Graphical Results

## Logic Analyzer Setup Software

The logic analyzer setup software (Tektronix refers to these as 'Support Packages') provides a quick setup of the logic analyzer channels and logic analyzer clocking/acquisition parameters. This software also provides disassembly of the DDR4 transactions (Command, Address and Control only) for easy display of the DDR bus cycles and logic analyzer settings for triggers and filters.

## Compliance Analysis Software

The optional DDR4 Memory Compliance Analysis package enables and automates measurement of the DDR4 bus activity for fast and easy functional testing and extensive compliance, statistical, and performance analysis.

- Extensive JEDEC DDR4 Compliance Analysis
- Quick and Easy Setup w/No Calibration Required
- Automated Acquisition and Measurement
- Powerful in-application graphical and tabular analysis results
- Memory controller & JEDEC parameters predefined
- Quickly navigate through multiple acquisitions
- Listing and waveform windows with violation analysis built in



	Min.(ps)	Max.(ps)	Average(ps)	Margin(%)	Spec.
R1 R0	NA	NA	NA	NA	959,880
R2 R0	28,007	10,273,985	2,106,353	6.7	26,250
R3 R0	7,441	878,808	123,227	3.3	7,200
R4 R0	NA	NA	NA	NA	5,625
R5 R0	NA	NA	NA	NA	70,200,000
R6 R1 R0	1,855	8,189,726	945,496	-85.9	13,125
R7 R1 R0	114,121	8,169,101	6,001,631	3.7	110,000
R8 R1 R0	42,969	2,839,180	267,945	14.6	37,500
R9 R1 R0	42,969	2,839,180	267,945	-99.9	70,200,000
R10 R1 R0	18,652	116,172	20,254	42.1	13,125
R11 R1 R0	13,066	316,308	170,537	16.1	11,250
R12 R1 R0	NA	NA	NA	NA	20,625
R13 R0	37,383	326,054	162,946	10.8	33,750

Figure 5 Tabular Results Detail of Compliance Analysis

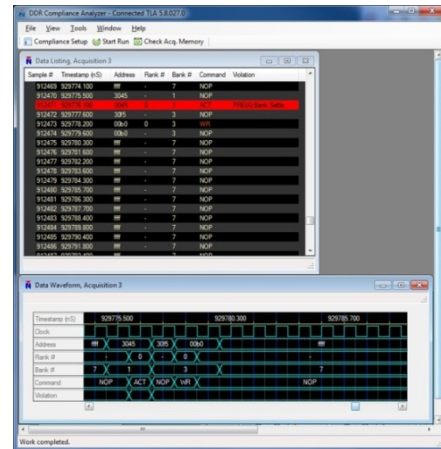


Figure 6 Waveform & Timing Displays of Compliance Analysis

Test	Name	Occurrences	Violations	Series	Min(ps)	Max(ps)	Average(ps)	Margin(%)	Spec. Voltage	Description
1	CDR/REFRESH Rate	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. A refresh (REFRESH) command did not occur in a self-refresh mode.
2	SRE w/ACT Fork	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. A Self Refresh Entry (SRE) command did occur in an active rank.
3	WRR w/ACT Fork	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. A Write Refresh Entry (WRR) command did occur in an active rank.
4	PROHIBIT/ACT Fork	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. A read (RD) or write (WR) or refresh (RR) command did occur during rank PROHIBIT.
5	CDR/REFRESH Rate	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. A refresh (REFRESH) command did occur in an active rank.
6	PROHIBIT/ACT Fork	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. A read (RD) or write (WR) or refresh (RR) command did occur during rank PROHIBIT.
7	SRE w/ACT Fork	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. A Self Refresh Entry (SRE) command did occur in an active rank.
8	WRR w/ACT Fork	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. A Write Refresh Entry (WRR) command did occur in an active rank.
9	REFRESH Rate	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. A refresh (REFRESH) command did occur in an active rank that is not in a self-refresh mode.
10	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.
11	ACT	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A read (RD) or write (WR) command did not occur during an active rank power-up.
12	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.
13	ACT	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A read (RD) or write (WR) command did not occur during an active rank power-up.
14	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.
15	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.
16	SRE Separation Rate R0V	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. As soon as refresh (REFRESH) command is required before another SRE is issued.
17	SRE Separation Rate R0V	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. As soon as refresh (REFRESH) command is required before another SRE is issued.
18	SRE Separation Rate R0V	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. As soon as refresh (REFRESH) command is required before another SRE is issued.
19	SRE Separation Rate R0V	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. As soon as refresh (REFRESH) command is required before another SRE is issued.
20	SRE Separation Rate R0V	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. As soon as refresh (REFRESH) command is required before another SRE is issued.
21	SRE Separation Rate R0V	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. As soon as refresh (REFRESH) command is required before another SRE is issued.
22	SRE Separation Rate R0V	0	0	0	NA	NA	NA	NA	1.2V	Sequential check. As soon as refresh (REFRESH) command is required before another SRE is issued.
23	WRR Rate	0	0	0	NA	NA	NA	NA	1.2V	Maximum time from one write refresh (WRR) command to the next valid command that is not an SRE must meet RCD.
24	WRR Rate	0	0	0	NA	NA	NA	NA	1.2V	Maximum time from one write refresh (WRR) command to the next valid command that is not an SRE must meet RCD.
25	vRRP Time	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time to self-refresh must meet vRRP.
26	vRRP Time	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time to self-refresh must meet vRRP.
27	RD to vRRP Separation	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time between read (RD) and write (WR) commands must meet RCD.
28	RD to vRRP Separation	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time between read (RD) and write (WR) commands must meet RCD.
29	Rank DLL Reset to R0V	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. The Rank DLL Reset (R0V) command did not occur in an active rank.
30	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.
31	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.
32	vRRP Time	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time to self-refresh must meet vRRP.
33	vRRP Time	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time to self-refresh must meet vRRP.
34	vRRP Time	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time to self-refresh must meet vRRP.
35	vRRP Time	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time to self-refresh must meet vRRP.
36	vRRP Time	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time to self-refresh must meet vRRP.
37	vRRP Time	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time to self-refresh must meet vRRP.
38	vRRP Time	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time to self-refresh must meet vRRP.
39	RD to PRR0V	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time from a read (RD) to a power refresh (PRR0V) command must meet RCD.
40	RD to PRR0V	0	0	0	NA	NA	NA	NA	1.2V	Maximum amount of time from a read (RD) to a power refresh (PRR0V) command must meet RCD.
41	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.
42	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.
43	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.
44	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.
45	RRD/ACT Fork to SRE Rate	0	0	0	NA	NA	NA	NA	1.2V	Power-up check. A refresh (REFRESH) or write (WR) command did not occur during an active rank power-up.

Figure 7 Detailed Compliance Analysis Results



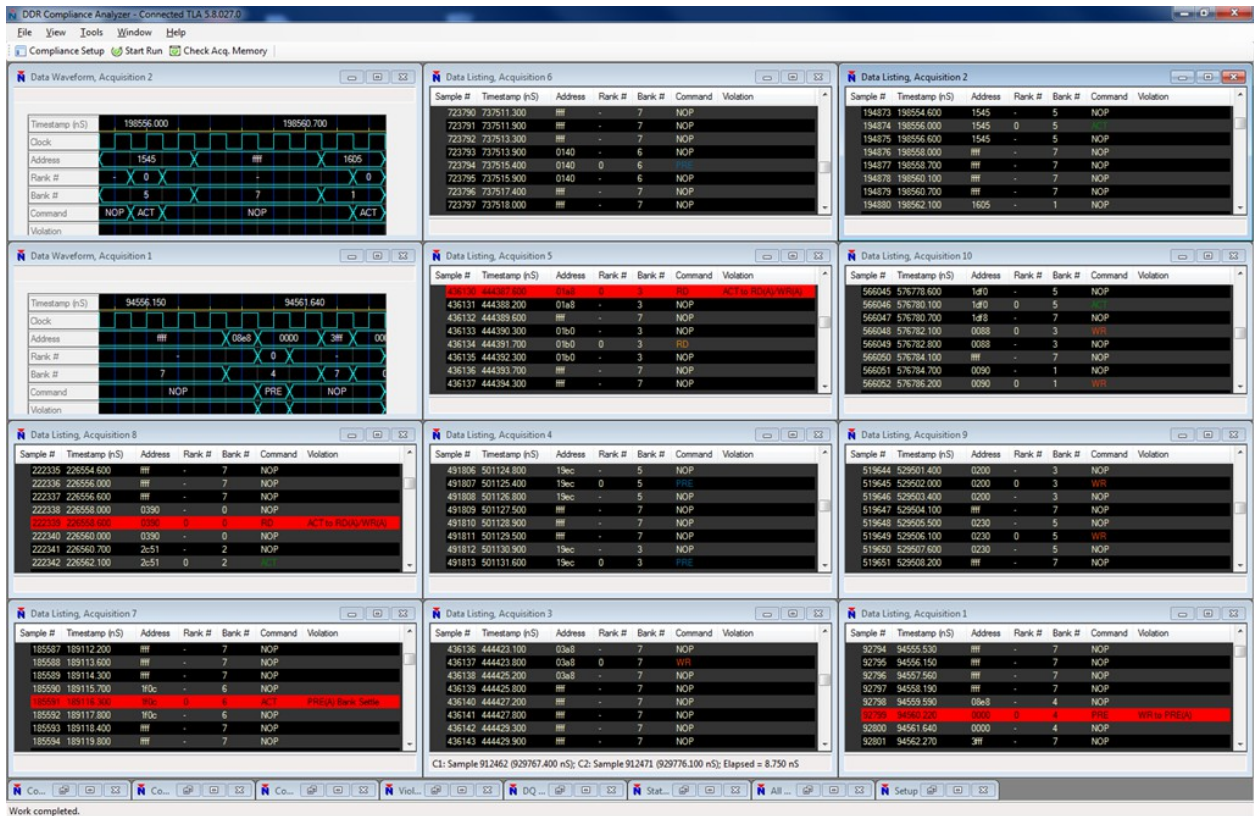


Figure 8 View of Violation in Data Across Many Acquisitions

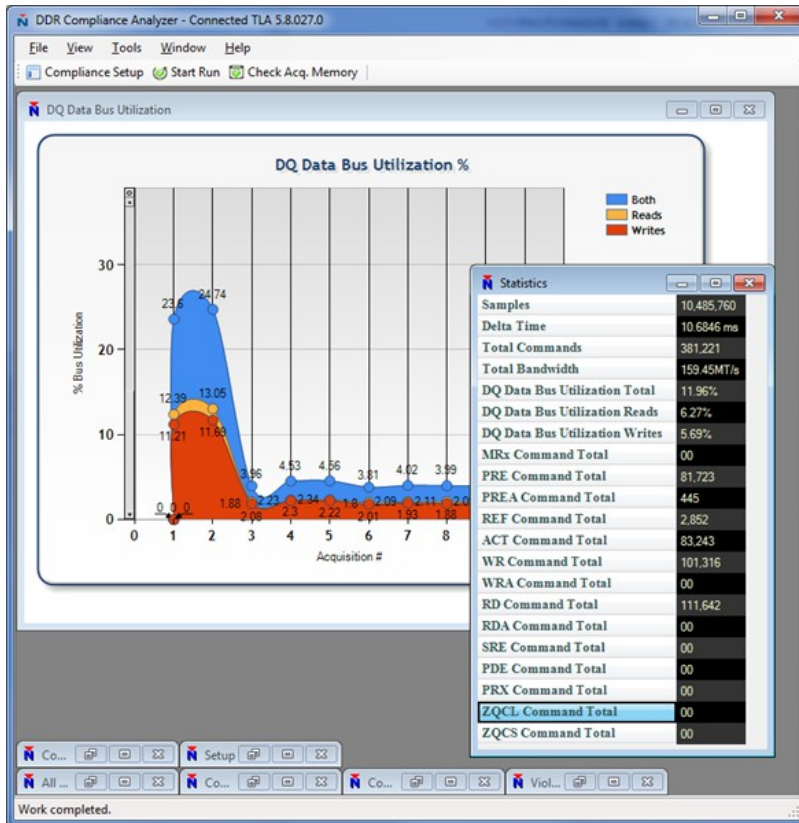


Figure 9 Bus Utilization Measurements

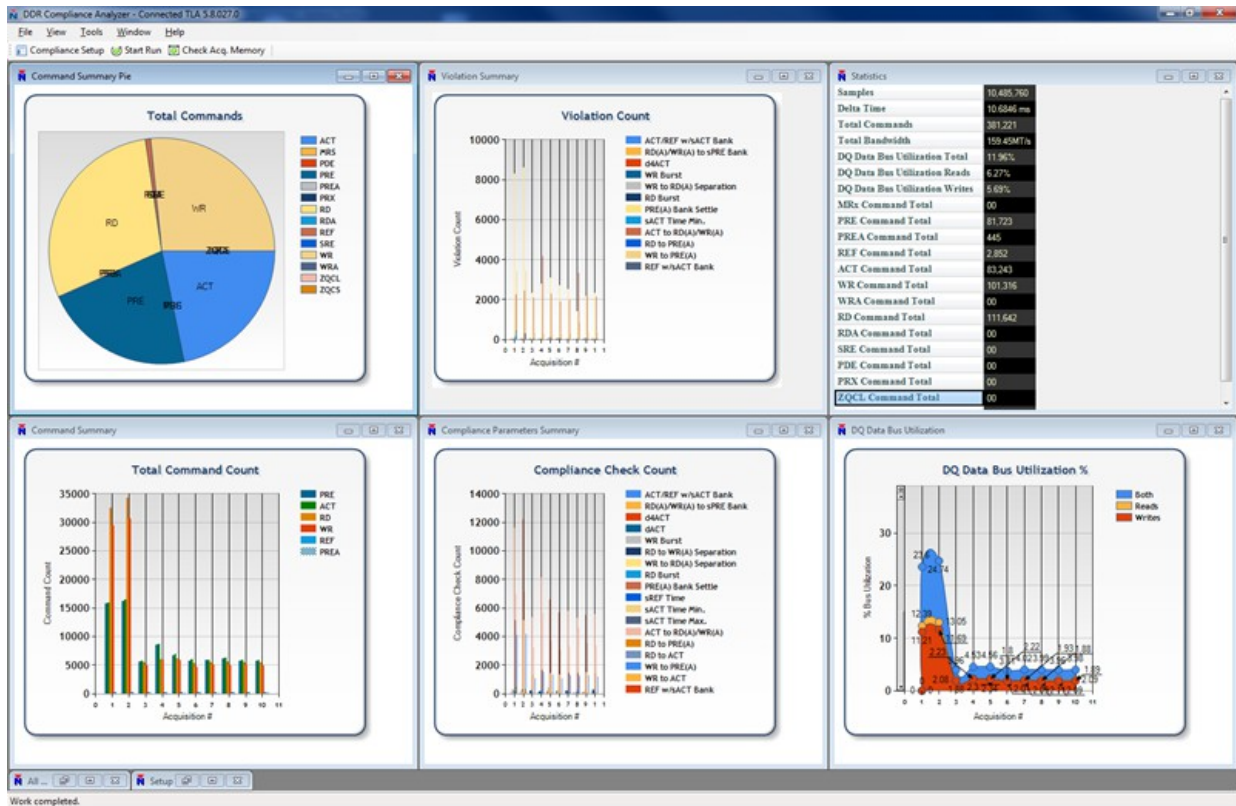


Figure 10 Graphical and Tabular Compliance Analysis Example

# DDR4 DIMM Slot Compliance Interposer

## NEX-DDR4INTR-CMPL Technical Specification

### General

Specification	Detail
Interface Type	Passive Interposer
LA Interface	NEX-PRB1-XL
JEDEC Module Type	DDR4 SDRAM Unbuffered or Registered DIMM

### Tektronix Hardware

Specification	Detail	Quantity
Logic Analyzer Mainframe	TLA7000	1
Logic Analyzer Module(s)	TLA7BB2/3/4 (1.4GHz Opt. Required)	1
Logic Analyzer Probes	NEX-PRB1-XL	2 (See note)

Note: A single NEX-PRB1-XL probe will enable the acquisition of all but 4 of the DDR4 control signals

### Product Configurations

Nomenclature	Detail
NEX-DDR4INTR-CMPL	1 – DDR4 DIMM Address, Command, Control Interposer 1 – TLA Setup & Decode Software <sup>1</sup>
NEX-MCATLA-DDR4-SWL	1 – DDR4 Compliance Analysis Software License (Optional)

1: Package comes with TLA Support Package, SPA, and iCiS tool.

## Further Information

Please contact us by telephone, email or mail as listed below. Normal business hours are 9:00 – 5:00 EDT/EST.

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