Design Specification

DDR2 UDIMM
Enhanced Performance Profiles

Document Change History

REV	Date	Reason for Change
01	05/12/06	Initial Release

Table of Contents

Chapter 1. Enhanced Performance Profiles 1
1.1. Performance Profiles 1
1.1.1. Full Profiles 1
1.1.2. Abbreviated Profiles 2
1.2. Address Mapping 2
Chapter 2. Field Definitions 1
2.1. .Global Field Definitions 1
2.1.1. Field: EPP Identifier String 1
2.1.2. Field: EPP Profile Type Identifier 1
2.1.3. Field: Profile for Optimal Performance 2
2.1.4. Field: Profile Enables 2
2.2. Profile-Specific Field Definitions 3
2.2.1. Field: Voltage Level 3
2.2.2. Field: Address Command Rate 3
2.2.3. Field: Address Drive Strength 4
2.2.4. Field: Chip Select Drive Strength 4
2.2.5. Field: Clock Drive Strength 4
2.2.6. Field: Data Drive Strength 5
2.2.7. Field: DQS Drive Strength 5
2.2.8. Field: Address/Command Fine Delay 5
2.2.9. Field: Address/Command Setup Time 5
2.2.10. Field: Chip Select Fine Delay 6
2.2.11. Field: Chip Select Setup Time 6
2.3. Field Definitions Derived from JEDEC Standard 7
2.3.1. Field: SDRAM Cycle Time 7
2.3.2. Field: CAS Latency 7

Chapter 1.
Enhanced Performance Profiles

All DDR2 Unbuffered DIMM modules are required to include a Serial Presence Detect (SPD) EEPROM to allow them to be properly recognized by target systems. The contents of the SPD are defined by JEDEC.

While the JEDEC SPD definitions have been used very effectively, they are not sufficiently comprehensive for overclocking applications. In such applications there are many parameters that are modified, and no provision exists in the JEDEC SPD specification to allow the system to make these changes automatically.

This document defines an enhanced SPD which contains additional performance-specific information known as Enhanced Performance Profiles (EPP). This information is contained in an unused area of the SPD, so modules implementing EPP may continue to be JEDEC compliant.

1.1. Performance Profiles

The EPP section of the SPD may contain one of two defined profile types:

- Full Profile
- Abbreviated Profiles

The following sections describe both of these profiles.

1.1.1. Full Profiles

The EPP may contain up to two full performance profiles. The full profiles are very comprehensive, and are tailored towards modules where the highest degree of parametric specification is desired. Table 1 describes the profiles stored in the Manufacturer's Specific Data area of the SPD (bytes 99 - 127).

Table 1. Full Performance Profiles

Byte Number	Description
99-103	Profile Index - Version, enables, etc.
104-115	Profile FP0
116 - 127	Profile FP1

1.1.2. Abbreviated Profiles

The EPP may contain up to four abbreviated performance profiles. Some detailed parameters are not included in the abbreviated profiles; only the most commonly modified parameters are included. The abbreviated list of parameters allows four profiles to reside within the EPP, rather than just two. Table 2 describes the profiles stored in the Manufacturer's Specific Data area of the SPD (bytes 99 - 127)

Table 2. Abbreviated Performance Profiles

Byte Number	Description
99-103	Profile Index - Version, enables, etc.
104-109	Profile AP0
110 - 115	Profile AP1
116 - 121	Profile AP2
122 - 127	Profile AP3

1.1.3. Address Mapping

Tables 3 and 4 contain the address mapping for full performance profile and abbreviated performance profile, respectively.

Table 3. Full Performance Profile Map

Byte Number	Bit Field	Profile Number	Description	*
99-101	7:0	Global	EPP Identifier String	
102	7:0	Global	EPP Profile Type Identifier	
103	1:0	Global	Profile for Optimal Performance	
103	5:4	Global	Profile Enables	
104	6:0	0	Voltage Level	
104	7	0	Address Cmd Rate	
105	1:0	0	Address Drive Strength	
105	3:2	0	Chip Select Drive Strength	
105	5:4	0	Clock Drive Strength	
105	7:6	0	Data Drive Strength	
106	1:0	0	DQS Drive Strength	
107	4:0	0	Address/Command Fine Delay	
107	5	0	Address/Command Setup Time	
108	4:0	0	Chip Select Delay	

Byte Number	Bit Field	Profile Number	Description	*
108	5	0	Chip Select Setup Time	
109	7:0	0	Minimum Cycle time at Supported CAS Latency	9
110	7:0	0	CAS Latency	18
111	7:0	0	Minimum RAS to CAS delay (tRCD)	29
112	7:0	0	Minimum Row Precharge Time (tRP)	27
113	7:0	0	Minimum Active to Precharge Time (tRAS)	30
114	7:0	0	Write Recovery Time (tWR)	36
115	7:0	0	Minimum Active to Active/Refresh Time (tRC)	41
116	6:0	1	Voltage Level	
116	7	1	Address Cmd Rate	
117	1:0	1	Address Drive Strength	
117	3:2	1	Chip Select Drive Strength	
117	5:4	1	Clock Drive Strength	
117	7:6	1	Data Drive Strength	
118	1:0	1	DQS Drive Strength	
119	4:0	1	Address/Command Fine Delay	
119	5	1	Address/Command Setup Time	
120	4:0	1	Chip Select Delay	
120	5	1	Chip Select Setup Time	
121	7:0	1	Minimum Cycle time at Supported CAS Latency	9
122	7:0	1	CAS Latency	18
123	7:0	1	Minimum RAS to CAS delay (tRCD)	29
124	7:0	1	Minimum Row Precharge Time (tRP)	27
125	7:0	1	Minimum Active to Precharge Time (tRAS)	30
126	7:0	1	Write Recovery Time (tWR)	36
127	7:0	1	Minimum Active to Active/Refresh Time (tRC)	41

* Based on JEDEC Byte Number

Table 4. Abbreviated Performance Profile Map

Byte Number	Bit Field	Profile Number	Description	*
99-101	7:0	Global	EPP Identifier String	
102	7:0	Global	EPP Profile Type Identifier	
103	1:0	Global	Profile for Optimal Performance	
103	7:4	Global	Profile Enables	
104	6:0	0	Voltage Level	
104	7	0	Address Cmd Rate	
105	7:0	0	Minimum Cycle time at Supported CAS Latency	9
106	7:0	0	CAS Latency	18
107	7:0	0	Minimum RAS to CAS delay (tRCD)	29
108	7:0	0	Minimum Row Precharge Time (tRP)	27
109	7:0	0	Minimum Active to Precharge Time (tRAS)	30
110	6:0	1	Voltage Level	
110	7	1	Address CMD Rate	
111	7:0	1	Minimum Cycle time at Supported CAS Latency	9
112	7:0	1	CAS Latency	18
113	7:0	1	Minimum RAS to CAS delay (tRCD)	29
114	7:0	1	Minimum Row Precharge Time (tRP)	27
115	7:0	1	Minimum Active to Precharge Time (tRAS)	30
116	6:0	2	Voltage Level	
116	7	2	Address Cmd Rate	
117	7:0	2	Minimum Cycle time at Supported CAS Latency	9
118	7:0	2	CAS Latency	18
119	7:0	2	Minimum RAS to CAS delay (tRCD)	29
120	7:0	2	Minimum Row Precharge Time (tRP)	27
121	7:0	2	Minimum Active to Precharge Time (tRAS)	30
122	6:0	3	Voltage Level	
122	7	3	Address Cmd Rate	
123	7:0	3	Minimum Cycle time at Supported CAS Latency	9
124	7:0	3	CAS Latency	18
125	7:0	3	Minimum RAS to CAS delay (tRCD)	29
126	7:0	3	Minimum Row Precharge Time (tRP)	27
127	7:0	3	Minimum Active to Precharge Time (tRAS)	30

***** Based on JEDEC Byte Number

Chapter 2.
Field Definitions

2.1. .Global Field Definitions

2.1.1. Field: EPP Identifier String

The EPP Identifier String field describes whether this DIMM adheres to *The Enhanced Performance Profile SPD Specification*. The value is specified most significant nibble first. So byte 99 should contain the hex value 6D. Table 5 shows the EPP SPD support strings.

Table 5. EPP SPD Support String Field

Support String	Hex Value
Yes	4E566Dh
No	All other values

2.1.2. Field: EPP Profile Type Identifier

The EPP Profile Type Identifier field describes which version this DIMM supports. Table 6 shows the EPP profile types.

Table 6. EPP Profile Type Field

Profile Type Supported	Hex Value
Abbreviated Profiles	A1
Full Profiles	B1

2.1.3. Field: Profile for Optimal Performance

The Profile for Optimal Performance field specifies which Profile should be loaded to maximize system performance. Table 7 shows the profile for the optimal performance.

Table 7. Profile for Optimal Performance Field

Best Profile	Hex Value
0	0
1	1
2	2
3	3

2.1.4. Field: Profile Enables

The Profile Enables field specifies which profiles contain valid data. At least one profile must be marked valid. Table 8 lists the profiles.

Table 8. Profile Enables Field

Profile Enable	Hex Value
Profile 0 Valid	1
Profile 1 Valid	2
Profile 2 Valid	4
Profile 3 Valid	8

2.2. Profile-Specific Field Definitions

2.2.1. Field: Voltage Level

The Voltage Level field describes the voltage level required for this profile. The value is defined as 25mV increments above the nominal operating voltage. All Hex values between 00h-1Ch are valid. Table 9 lists the voltage levels.

Table 9. Voltage Level Field

Voltage Level	Example Hex Values
1.8V	00h
1.9V	04h
2.0V	08h
2.1V	0Ch
2.2V	10h
2.3V	14h
2.4V	18h
2.5V	1Ch

2.2.2. Field: Address Command Rate

The Address Command Rate field defines the address command rate. If the command rate is set to 1T, then commands can be sent on every clock edge. If the command rate is set to 2T, then commands can be sent on every other clock edge. Table 10 shows the command rates.

Table 10. Address Command Rate Field

Command Rate	Hex Value
1T	0h
2T	1h

2.2.3. Field: Address Drive Strength

The Address Drive Strength field defines the address drive strength. Table 11 lists the drive strengths.

Table 11. Address Drive Strength Field

Drive Strength	Hex Value
1.0x	0h
1.25x	1h
1.5x	2h
2.0x	3h

2.2.4. Field: Chip Select Drive Strength

This field defines the chip select drive strength. Table 12 lists the chip select drive strengths.

Table 12. Chip Select Drive Strength Field

Drive Strength	Hex Value
1.0x	0h
1.25x	1h
1.5x	2h
2.0x	3h

2.2.5. Field: Clock Drive Strength

This field defines the clock drive strength. Table 13 lists the clock drive strengths.

Table 13. Clock Drive Strength Field

Drive Strength	Hex Value
.75x	0h
1.0x	1h
1.25x	2h
1.5x	3h

2.2.6. Field: Data Drive Strength

This field defines the data drive strength. Table 14 lists the data drive strengths.

Table 14. Data Drive Strength Field

Drive Strength	Hex Value
.75x	0h
1.0x	1h
1.25x	2h
1.5x	3h

2.2.7. Field: DQS Drive Strength

This field defines the DQS drive strength. Table 15 lists the DSQ drive strengths.

Table 15. DQS Drive Strength Field

Drive Strength	Hex Value
.75x	0h
1.0x	1h
1.25x	2h
1.5x	3h

2.2.8. Field: Address/Command Fine Delay

The Address/Command Fine Delay field defines how long the address and command pins are delayed with respect to the default setup time. Table 16 lists the address fine delays.

Table 16. Address Fine Delay Field

Fine Delay	Hex Value
No delay	00h
1/64 MEMCLK delay	01h
2/64 MEMCLK delay	02h
31/64 MEMCLK delay	1Fh

2.2.9. Field: Address/Command Setup Time

This field defines the default setup time for address and command pins.

Table 17. Address Setup Time Field

Setup Time	Hex Value
½ MEMCLK	0h
1 MEMCLK	1h

2.2.10. Field: Chip Select Fine Delay

The Chip Select Fine Delay field defines how long the chip-select and ODT pins are delayed with respect to the default setup time. Table 18 lists the fine delay times.

Table 18. Chip Select Fine Delay Field

Fine Delay	Hex Value
No delay	00h
1/64 MEMCLK delay	01h
2/64 MEMCLK delay	02h
31/64 MEMCLK delay	1Fh

2.2.11. Field: Chip Select Setup Time

The Chip Select Setup Time field defines the default setup time for chip select and ODT pins. Table 19 lists the setup times.

Table 19. Chip Select Setup Time Field

Setup Time	Hex Value
½ MEMCLK	0h
1 MEMCLK	1h

2.3. Field Definitions Derived from JEDEC Standard

The remaining fields are copied from the JEDEC specification. Refer to *JC45 SPD* for DDR2 SDRAM Module revision 1.2.

2.3.1. Field: SDRAM Cycle Time

The SDRAM Cycle Time field specifies the minimum cycle time at the desired CAS Latency. The JEDEC standard does not have a value to exactly specify 1066 MHz bus speed.

Therefore, one value has been added to extend the programmability of this field to cover this case. Table 20 lists the cycle time.

Table 20. SDRAM Cycle Time

Cycle Time	Hex Value
1.875ns	1Eh

2.3.2. Field: CAS Latency

The CAS Latency field specifies which CAS Latency should be programmed for this Profile. Unlike the JEDEC Standard, only a single CAS Latency should be specified. Table 21 lists the CAS latency values.

Table 21. CAS Latency Field

CAS Latency	Hex Value
2	04h
3	08h
4	10h
5	20h
6	40h