DDR3 migration to DDR4

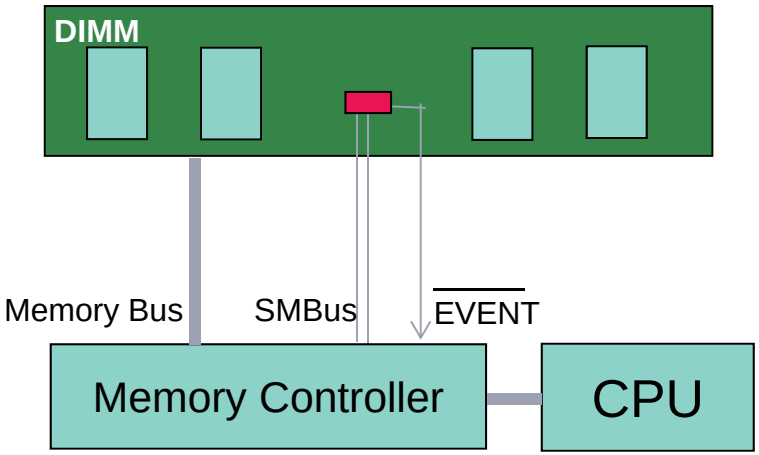
DIMM Thermal Sensor and SPD changes

Guru Prasad (G.prasad@nxp.com)
Business Development Manager, BL Interface Products
October 5 , 2011

Temp Sensor on Memory Module

- Historically, 256 byte EEPROM were mounted on DIMM to provide DRAM operating characteristics and manufacturer that was read during system start-up.
- As systems started to run hotter it was determined that mounting a thermal sensor onto the DIMM would provide better thermal margins and allow the processor to work closer to the + 85 °C DRAM limit.
- Industry is currently using this combination thermal sensor and SPD device on all DDR3 RDIMMs.
- Changes in the operating environment will require DDR4 DIMM to operate at lower voltages, higher bus speed and have a larger SPD size.

Thermal Sensor on Memory Module



RDIMM

- DDR3
  - 3.0 – 3.6V @ 400 kHz (Fast-mode)
- DDR4 – backward to DDR3
  - 2.2 – 3.6V @ 1 MHz (Fast-mode Plus)

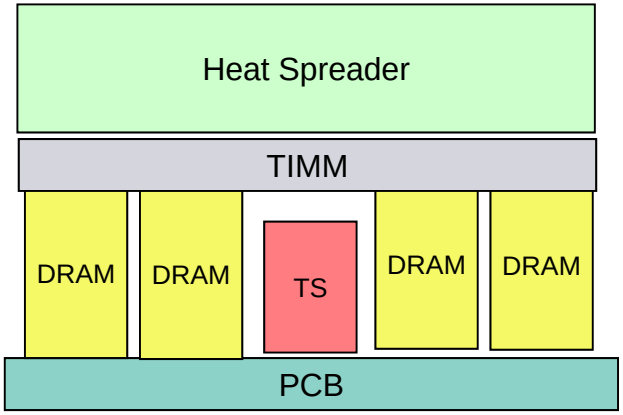
Device	Temp Sensor	SPD
TSE2002	Yes	2Kbit
TS2002	Yes	No
EE1002	No	2Kbit
TSE2004	Yes	4Kbit
EE1004	No	4Kbit

Temp Sensor on Memory Module

- Placing the temp sensor (TS) on memory module allows accurate monitoring of the module temperature to better estimate the DRAM case temperature (Tcase) to prevent it from exceeding the max operating temperature of 85 °C.
- The chipset throttles the memory traffic based on the actual temperatures instead of the calculated worst-case temperature or the ambient temperature using a temp sensor mounted on the motherboard.
- There is up to a 30% improvement in thin and light notebooks that are using one or two 1G SO-DIMM modules that support new Microsoft™ Vista.
- TS is mandatory for RDIMM to support better reliability and with need for /EVENT to go to 1.5 V pull up.
- Future uses of the TS will include more dynamic control over thermal throttling, the ability to use the Alarm Window to create multiple temperature zones for dynamic throttling and to save processor time by scaling the memory refresh rate.

DDR3 & DDR4 – Where the TS will be used

- TS/SPD on DDR3 and DDR4 DIMM
  - Mandatory on RDIMM, LRDIMM and UDIMM-ECC used by Server and Workstations
  - Optional , but not being used on SO-DIMM notebooks
  - Not being used on UDIMM for desktop due to no heat constraint
- OEMs using 3.3V V_{DDSPD} for DDR3 TS/SPD. V_{DDSPD} will be 2.5V for DDR4 but TSE2004 & EE1004 devices backward compatible to DDR3.
  - DDR2 DIMM is 1.8V ±10%
  - DDR3 DIMM is 1.5V > 1.35V > 1.25/1.20 ±10%
  - DDR4 DIMM is 1.2V ±10%
- TIM (Thermal Interface Material Layer)
  - Used on 4GB RDIMM or greater
  - Not required on 1GB and 2 GB RDIMM
- Industry standard naming for 2 x 3 packages
  - DFN < 1 mm
  - TDFN < 0.8 mm – Thermal Sensor/SPD
  - UDFN < 0.6 mm – SPD only



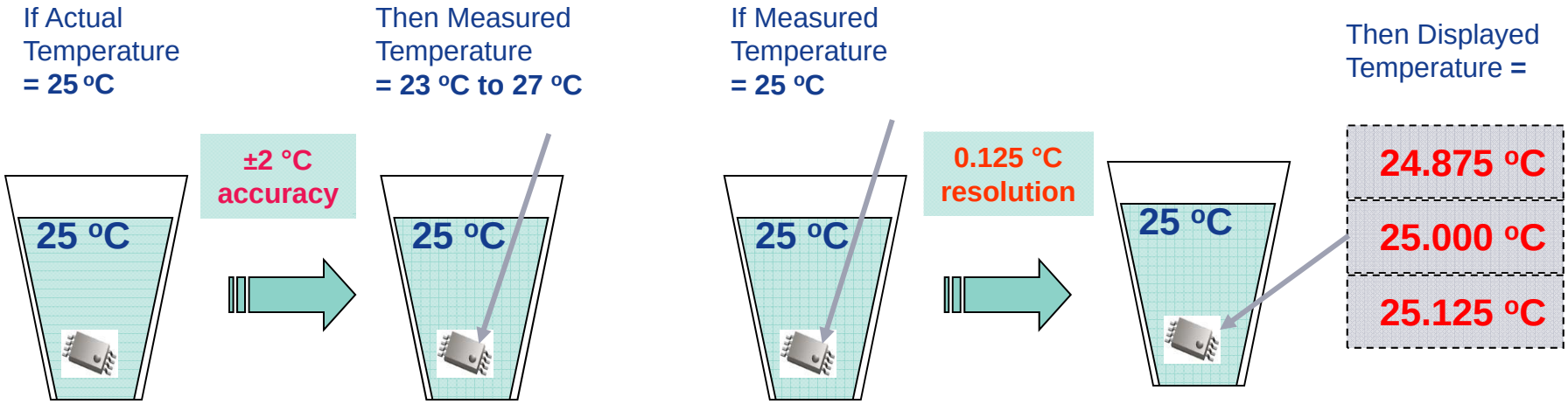
Temperature Accuracy Versus Resolution

Temperature Accuracy

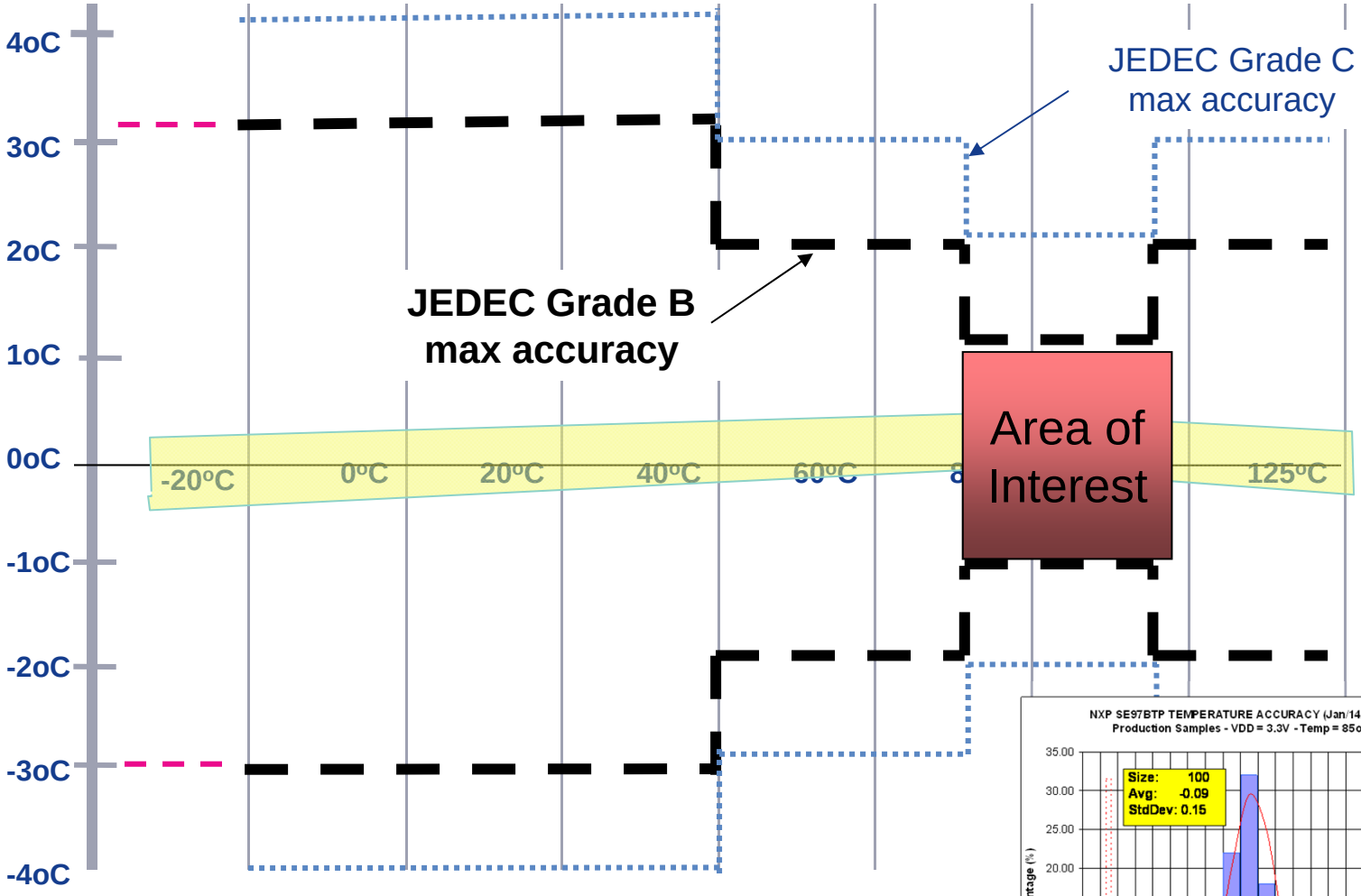
- Accuracy and error are used synonymously, and is the measure of how precisely the temperature sensor reading matches the ambient temperature
- Dependant on design, wafer lot variance and trimming (linear and offset) and varies over temp and V_{DD} range.
- Example: Temperature accuracy = ±2 °C

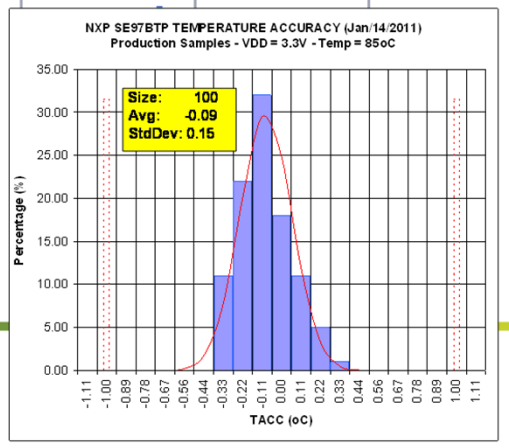
Temperature Resolution

- Temperature sensor's smallest measuring step
- Dependant on the number of bits used in Analog to Digital Converter (e.g., 8-bit = 1 °C, 11-bit = 0.125 °C and 13-bit = 0.03125 °C)
- Example: Temperature resolution = 0.125 °C



JEDEC Temperature Accuracy - Graph



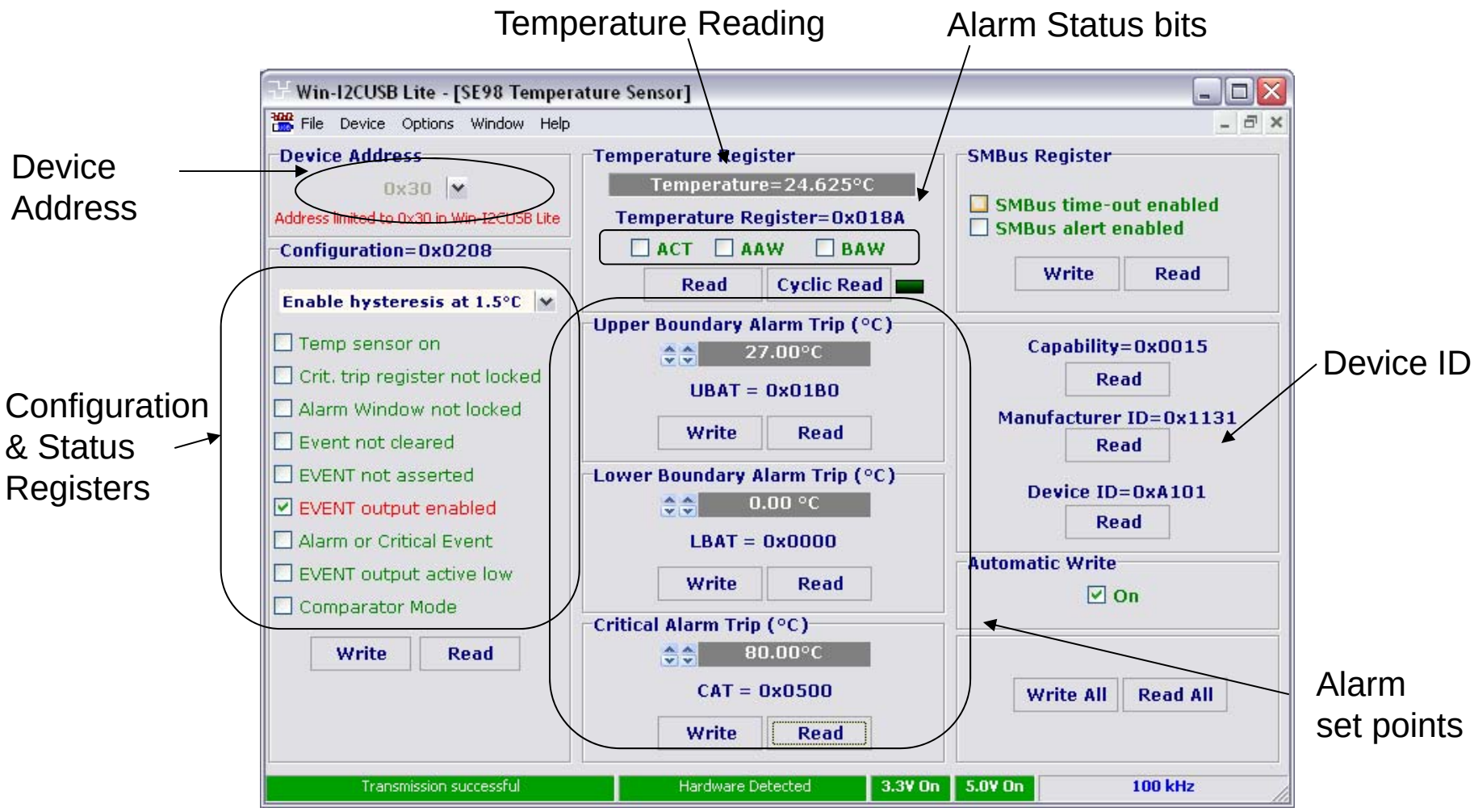


* Temperature accuracy data taken @3.3V for standard sample size

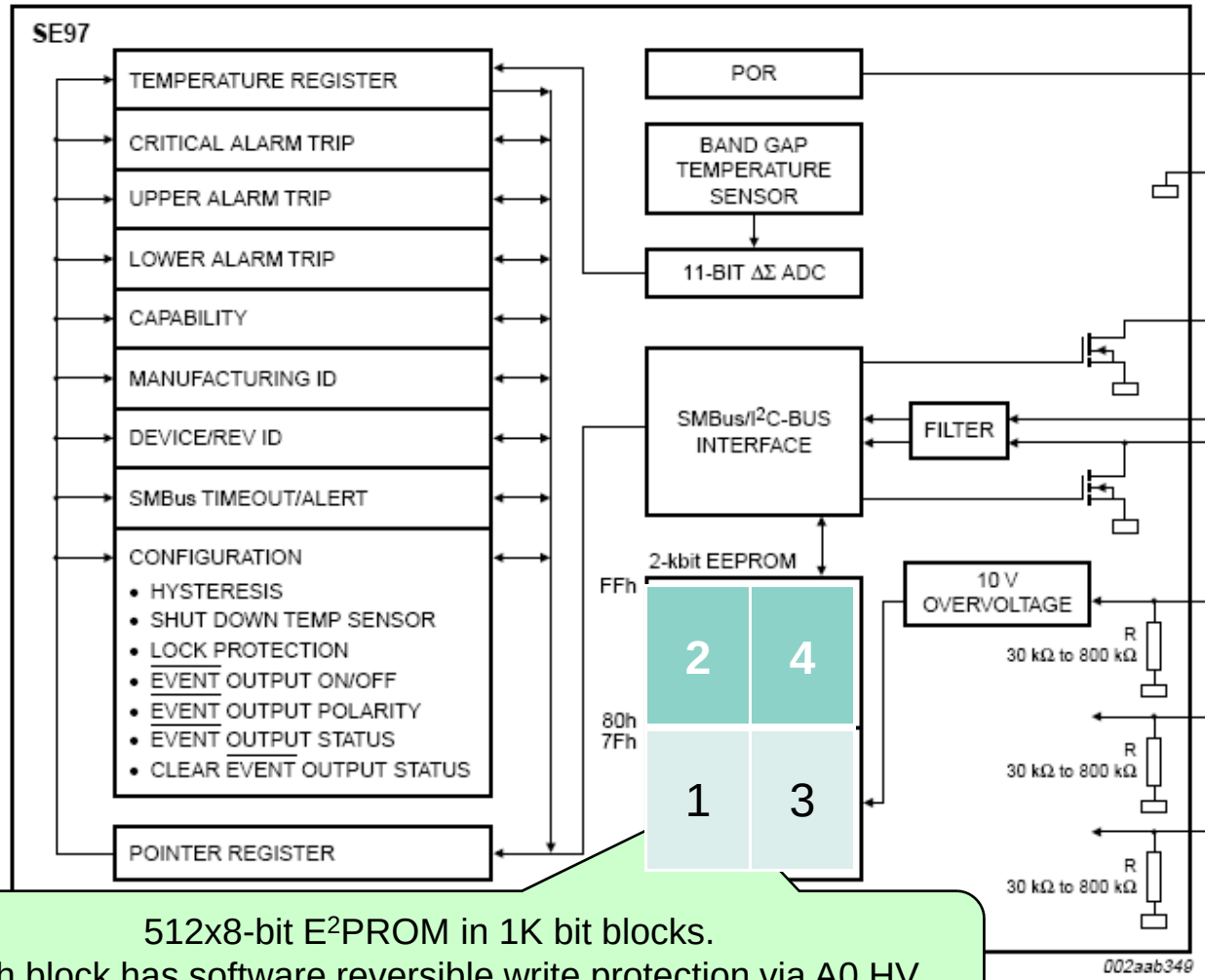
DDR3 to DDR4 changes

- Proposed changes to DDR3 Thermal Sensor and SPD
  - Will only offer B-grade sensitivity (no C-grade), no change to TS operation
  - Same I^2C interface protocol including SMBus timeout but use 1 MHz Fast-mode Plus
  - Supply range of 2.2 – 3.6V operation to support DDR4 VPP = 2.5V and DDR3 = 3.3V
  - SPD density double to 512 bytes with write protect for each 128 byte/1 Kbit block
  - SPD will be backward compatible for use in DDR3 sockets where the larger 4Kbit SPD is desired or higher 1 MHz speed or lower operating voltage
  - Remove Permanent Write Protection
  - Continue to use V_{HV} for Reversible Write Protection
  - Reduce the number of address pins
    - Allow 4 addresses on SA0 for So-DIMM
    - Allow 8 addresses on 2 pins (SA0 – 4 states/SA1 – 2 states) for UDIMM/RDIMM/LRDIMM
  - Defined power on (1.6V) /off (0.9V for 1 mS) trip points for power on and power down
- JEDEC task group just ratified the combined EE1004 & TSE2004 spec
- DDR4 initial introduction late 2013

Thermal Sensor Features/Operation



DDR3 to DDR4 Block Diagram



2.2 to 3.6V operation

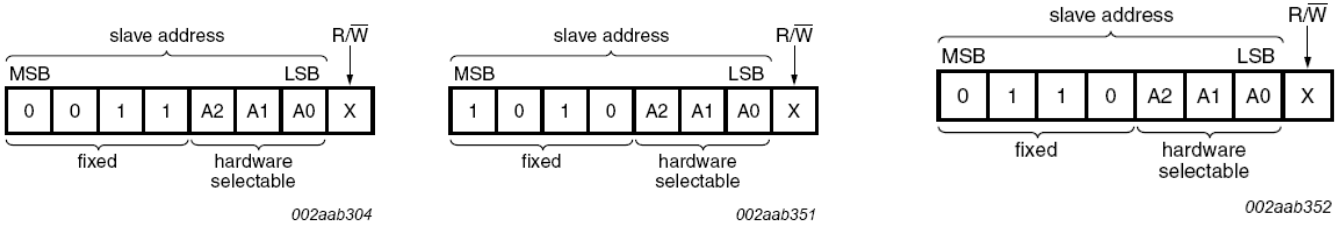
POR levels 1.6V / 0.9V

1 MHz SMBus

4 states from A0 pin to support 4 SO-DIMM with only one pin on connector. 2 states from A1 pin to support eight RDIMM addresses

512x8-bit E²PROM in 1K bit blocks.
Each block has software reversible write protection via A0 HV.
There is no more Permanent Write Protection.

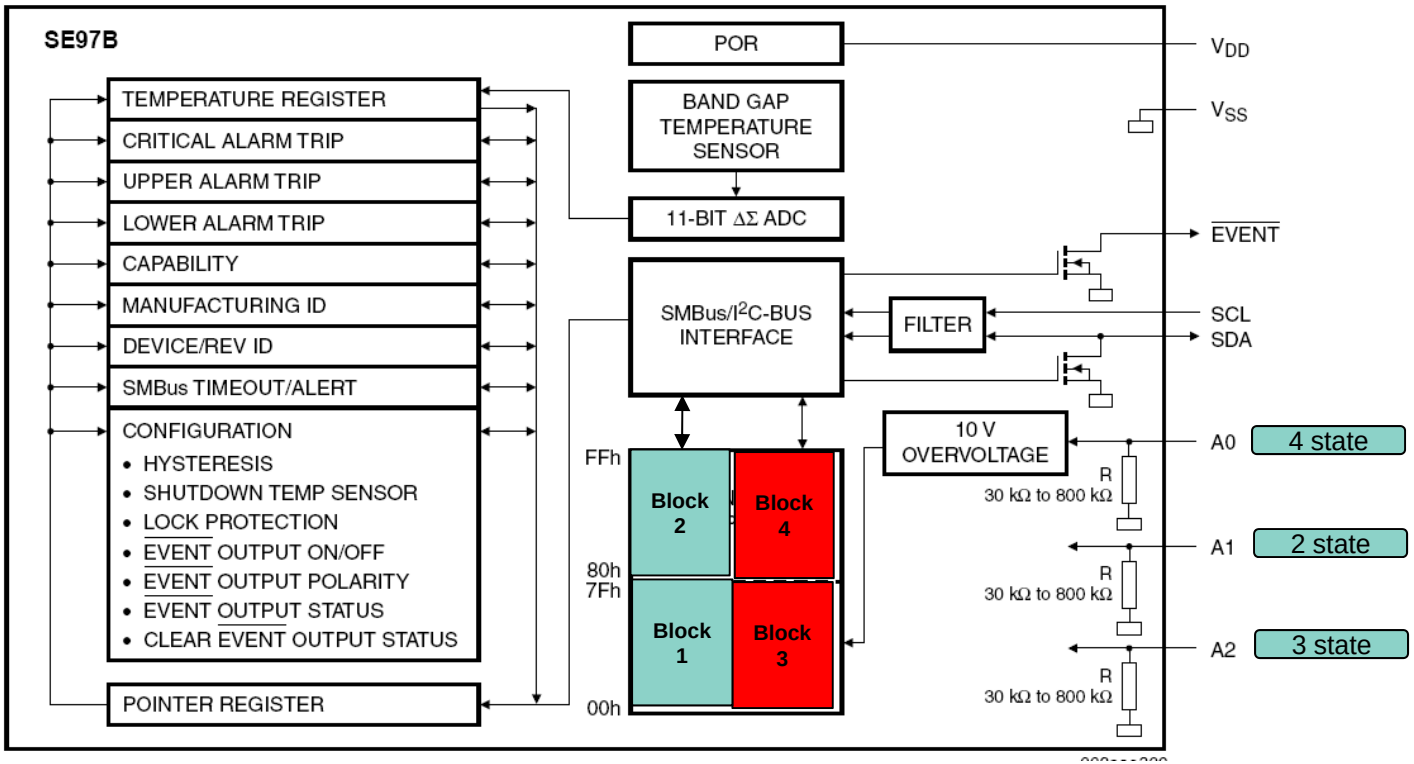
DDR3 & 4 Thermal Sensor & SPD Addresses



a. Temperature sensor

b. EEPROM (normal read/write)

c. EEPROM (software protection command)



DDR3 vs DDR4 Addressing

- Allow the address pins to work the same as currently being done in DDR3 but also allow the new DDR4 addressing modes that uses one fewer address pin.

Table 18 — DIMM Slot Addressing Modes

DIMM Slot	SMBus Address Compatibility Mode			SMBus Address Expansion Mode		
	SA2/MODE	SA1	SA0	SA2/MODE	SA1	SA0
0	0	0	0	Floating	0	0
1	0	0	1		0	1
2	0	1	0		1	0
3	0	1	1		1	1
4	1	0	0		0	1 KΩ[2]
5	1	0	1		0	10 KΩ[2]
6	1	1	0		1	1 KΩ[2]
7	1	1	1		1	10 KΩ[2]

Note 1: 0 = V_{SSSPD}, 1 = V_{DDSPD}, Floating = No Connect

Note 2: External resistor with ±5% tolerance on the system board from SA0 to V_{SSSPD}

DDR3 DDR4

DDR4 SPD – Upper and Lower Byte Access

- Command to EEPROM software write protection address space will toggle between lower and upper 256 byte page to be backward compatible to DDR3 but offer larger 512 byte memory space for future expansion needs.