PCI Express

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Agilent Technologies

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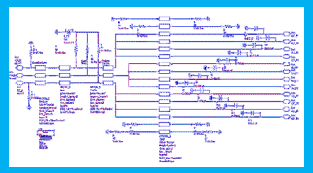
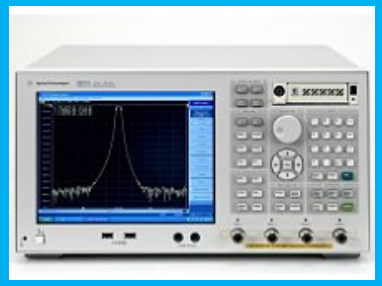
PCI Express® 3.0 – Agilent Total Solution

Physical layer – interconnect design



ADS design software

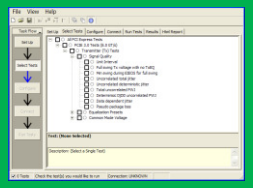
86100D DCA-J/TDR



E5071C ENA option TDR

Physical layer- transmitter test

90000 X-Series oscilloscope



N5393C PCI Express electrical compliance software

86100CU-400 PLL and Jitter Spectrum Measurement SW

Physical layer- receiver test

J-BERT N4903B –complete receiver tolerance

N4916B 4-tap de-emphasis signal converter

N4880A Clock Multiplier

N5990A automated compliance and device characterization test software

Data link/transaction layer

Digital Test Console

- U4301A Protocol Analyzer
- U4305A Exerciser
- Protocol Test Card
- Multiple probes with ESP technology

Industry's lowest scope noise floor/sensitivity and trigger jitter

DSA-X Series & Q Series Real-Time Oscilloscopes

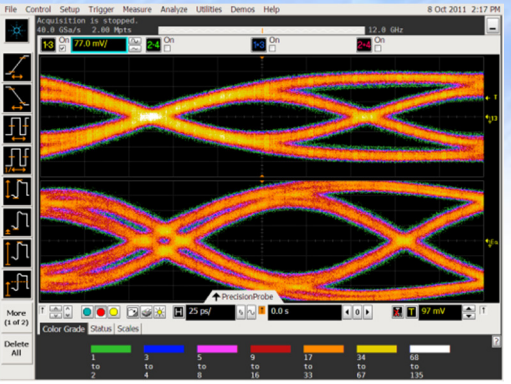
Automated compliance software – accurate, efficient and consistent

X1 through x16 Analysis and Exerciser support, with industry's only ESP probing technology

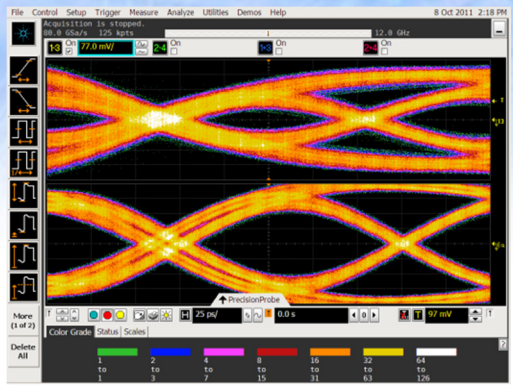
Agilent Technologies

CEM TX Measurement Challenges for PCIe 3.0

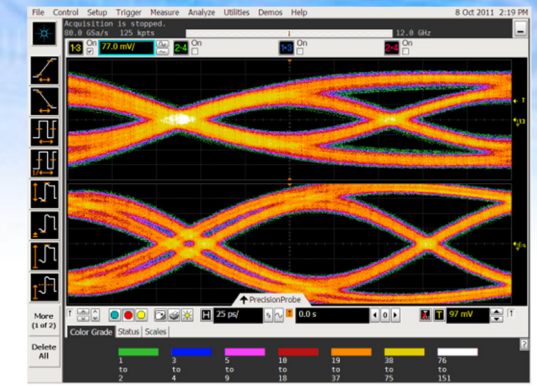
PCI Express 3.0 Root Complex Eyes (CTLE only)



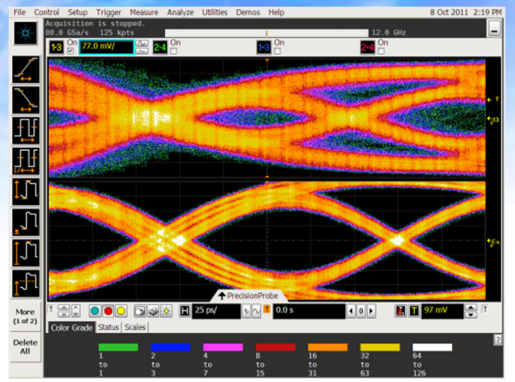
P0 Preset



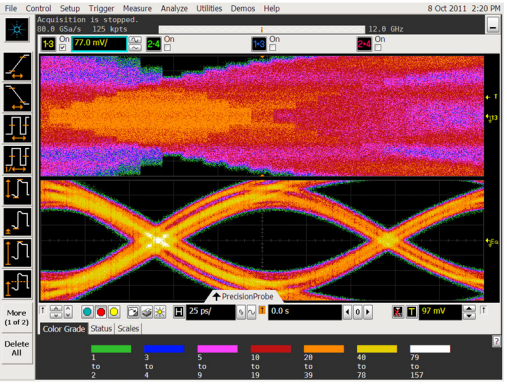
P1 Preset



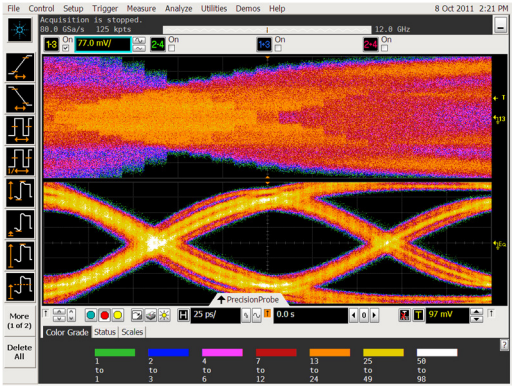
P2 Preset



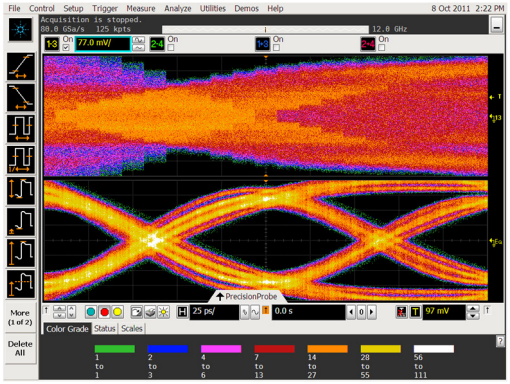
P3 Preset



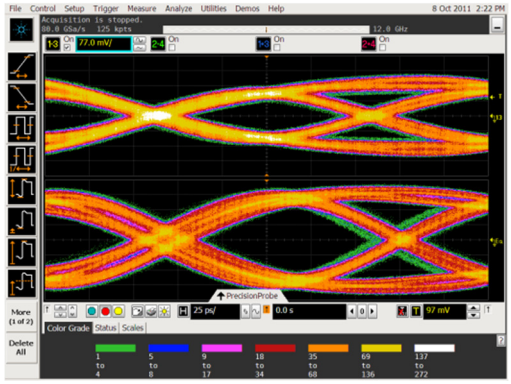
P4 Preset



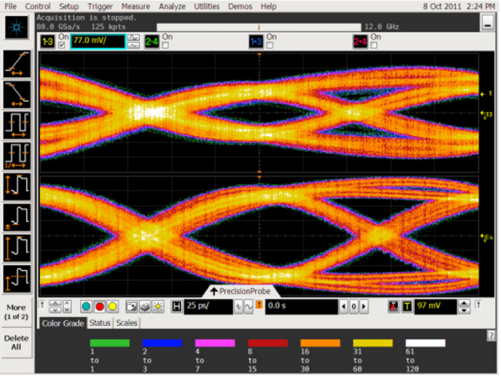
P5 Preset



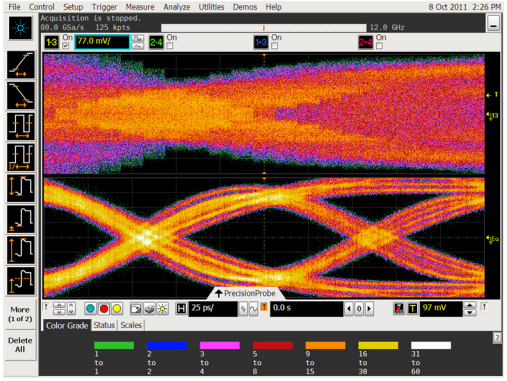
P6 Preset



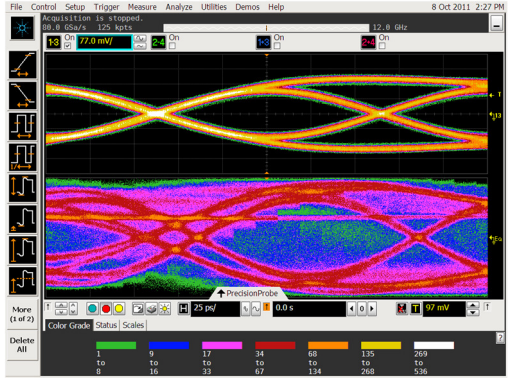
P7 Preset



P8 Preset



P9 Preset



P10 Preset

Not all PCIe 3.0 presets yield closed eyes – even without equalization.

PCIe 3.0 Compliance Test Overview

- **Physical layer**
  - 3.0 CLB and CBB fixtures
  - Add receiver and link equalization testing
  - New Sigtest
    - Reference CTLE+DFE
    - Test Channel Embedding
  - New Clock Tool
    - Provides clock phase jitter test to 3.0 base specification
  - PLL Bandwidth
- **Configuration Space**
  - Updated PCIeCV for new fields and capabilities
- **Link & Transaction layer**
  - Run existing 2.0 tests at 8.0GT/s for 3.0 8GT/s capable devices
  - New tests covering link equalization and other new features
- **Platform Configuration**
  - Run existing tests at 8GT/s
  - New tests for 3.0

Test Specs at or close to 0.9 workgroup approval

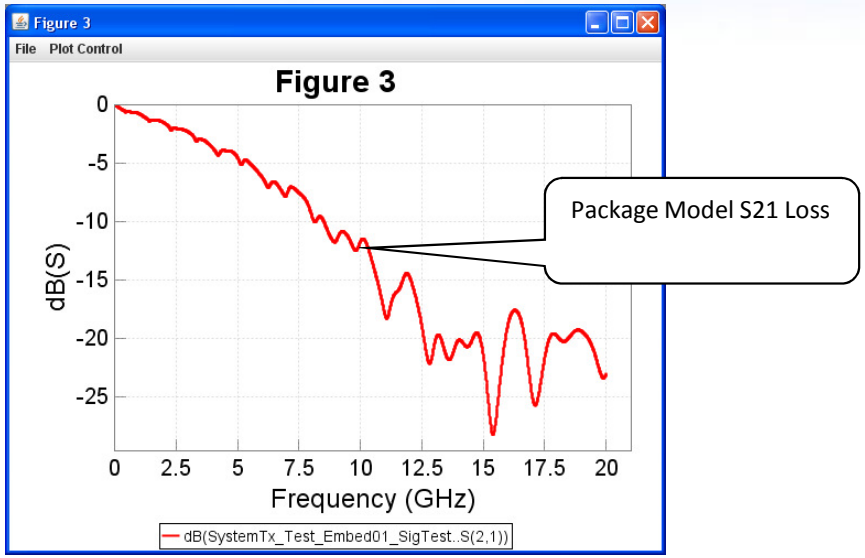
3.0 Transmitter Tests

- TX signal quality test
  - Must pass with at least one preset
  - Similar to 2.0 signal quality test/procedure
- TX preset test
  - Verify DUT can generate all presets and equalization levels meet spec requirements.
- Tx link equalization test
  - Test that DUT changes TX EQ in phase 2/phase 3 and check equalization levels with real traffic

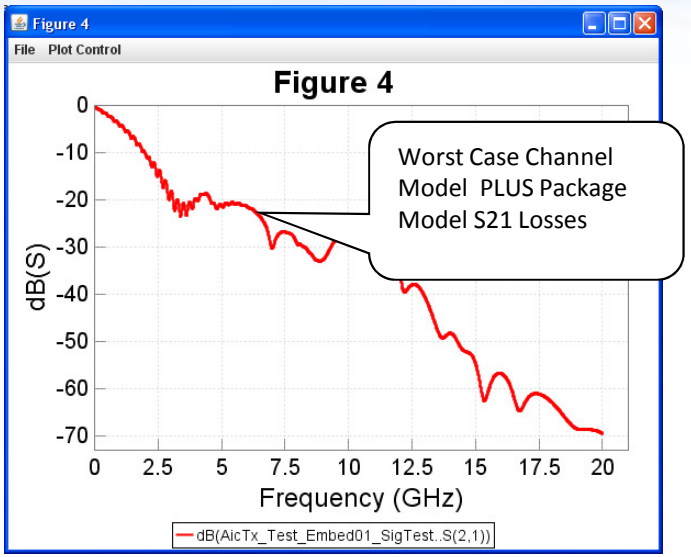
Electrical Validation of Transmitters

CEM Testing Procedures

Motherboard Testing



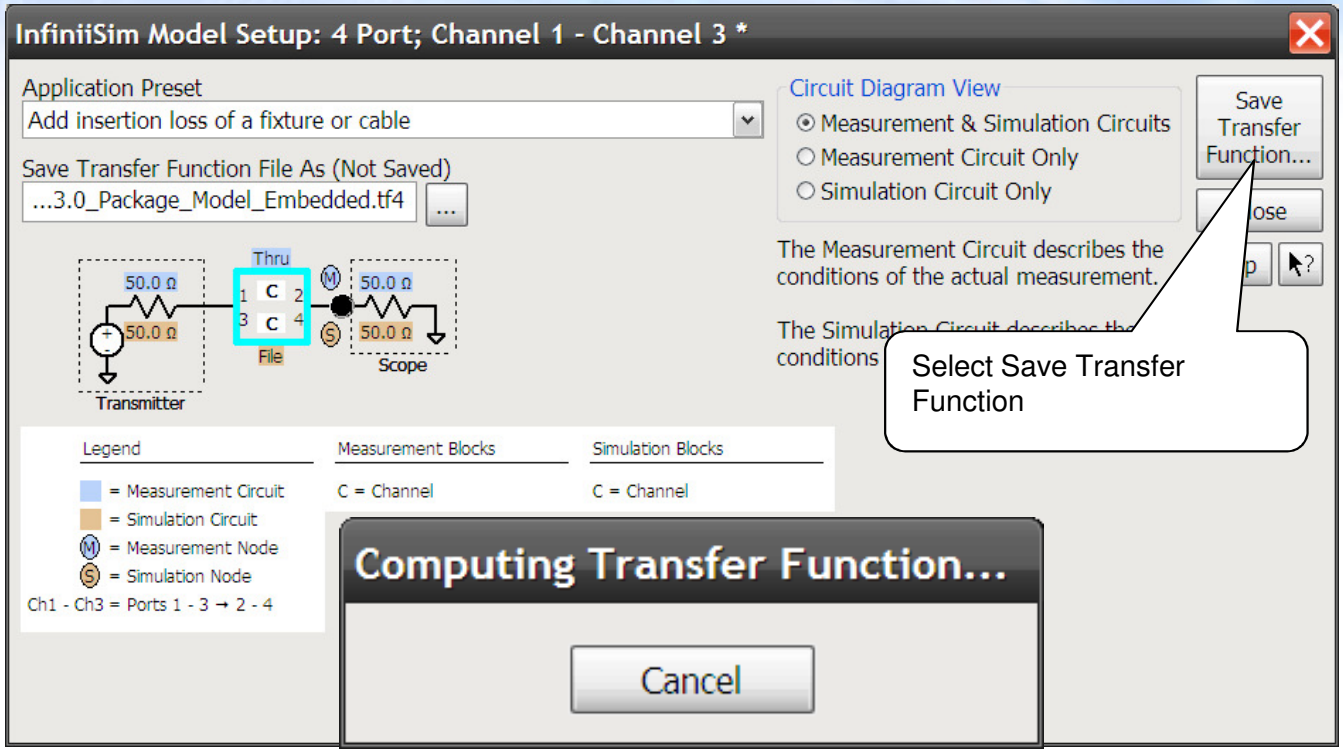
Add-in Card Testing

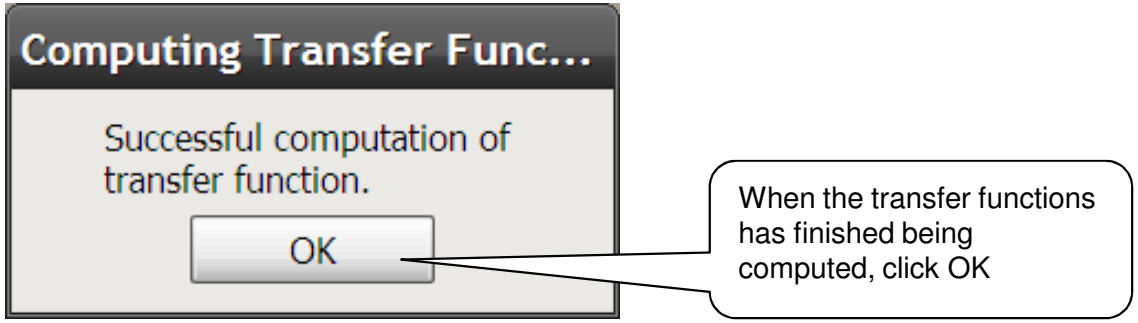


- Embed loss using Agilent InfiniiSim
- Embed loss using Sigtest Embed Template selection

Agilent InfiniiSim Software (cont'd)

- Select ***Save Transfer Function***
- Click ***OK***
- When the operation completes click ***OK***
- When completed you will be returned to the InfiniiSim setup screen. Click ***Close***.
- This will return you to the Channel Setup Screen. Click ***Close***.





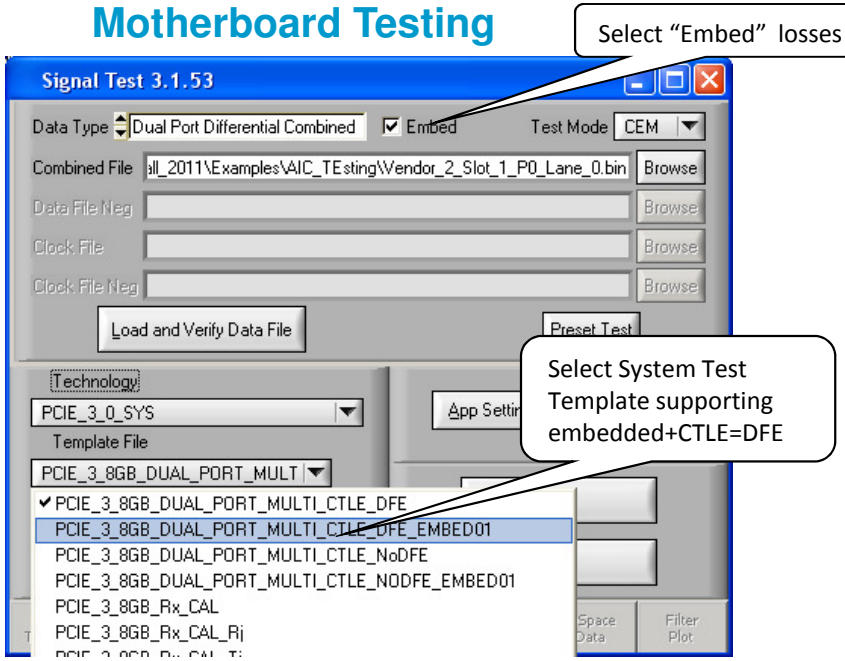
Embedded Waveform Display

- ***CH1-3*** is transformed with InfiniiSim into the embedded waveform (using hardware differential channels). Amplitude is slightly lower due to added loss.
- A saved waveform of the original waveform is shown for comparison
- After InfiniiSim is applied, you capture and save waveform files normally for post-processing with Sigtest.

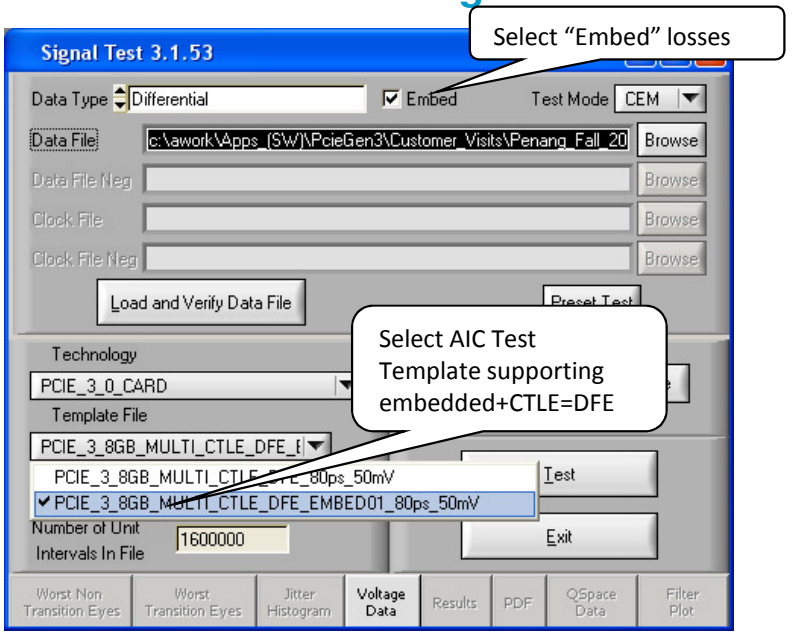
Testing Transmitters with SigTest

PCIe Validation for PC devices

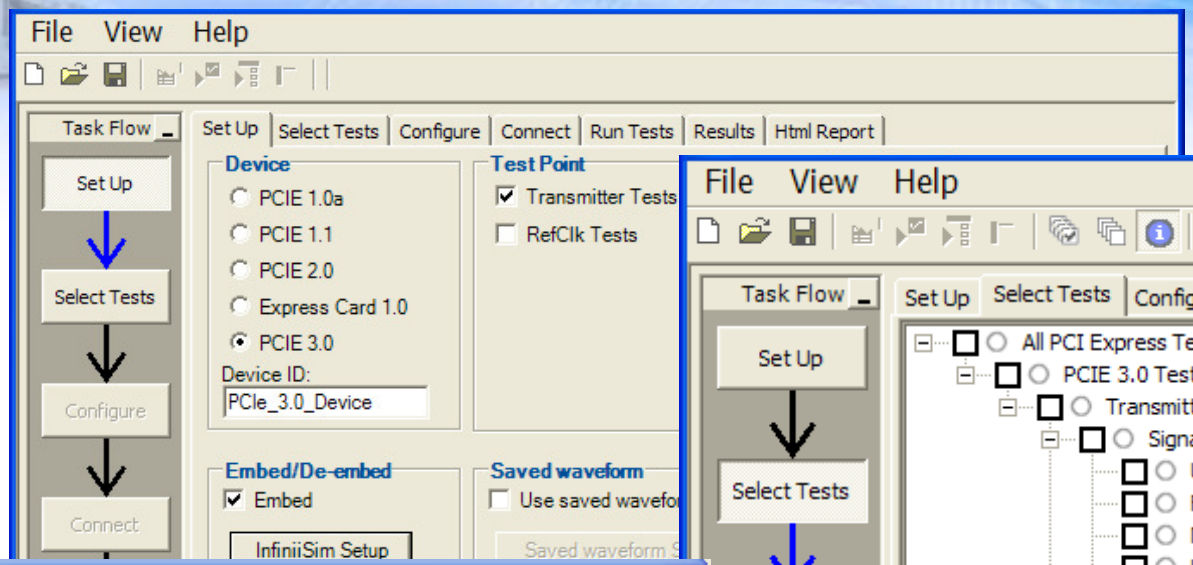
Motherboard Testing

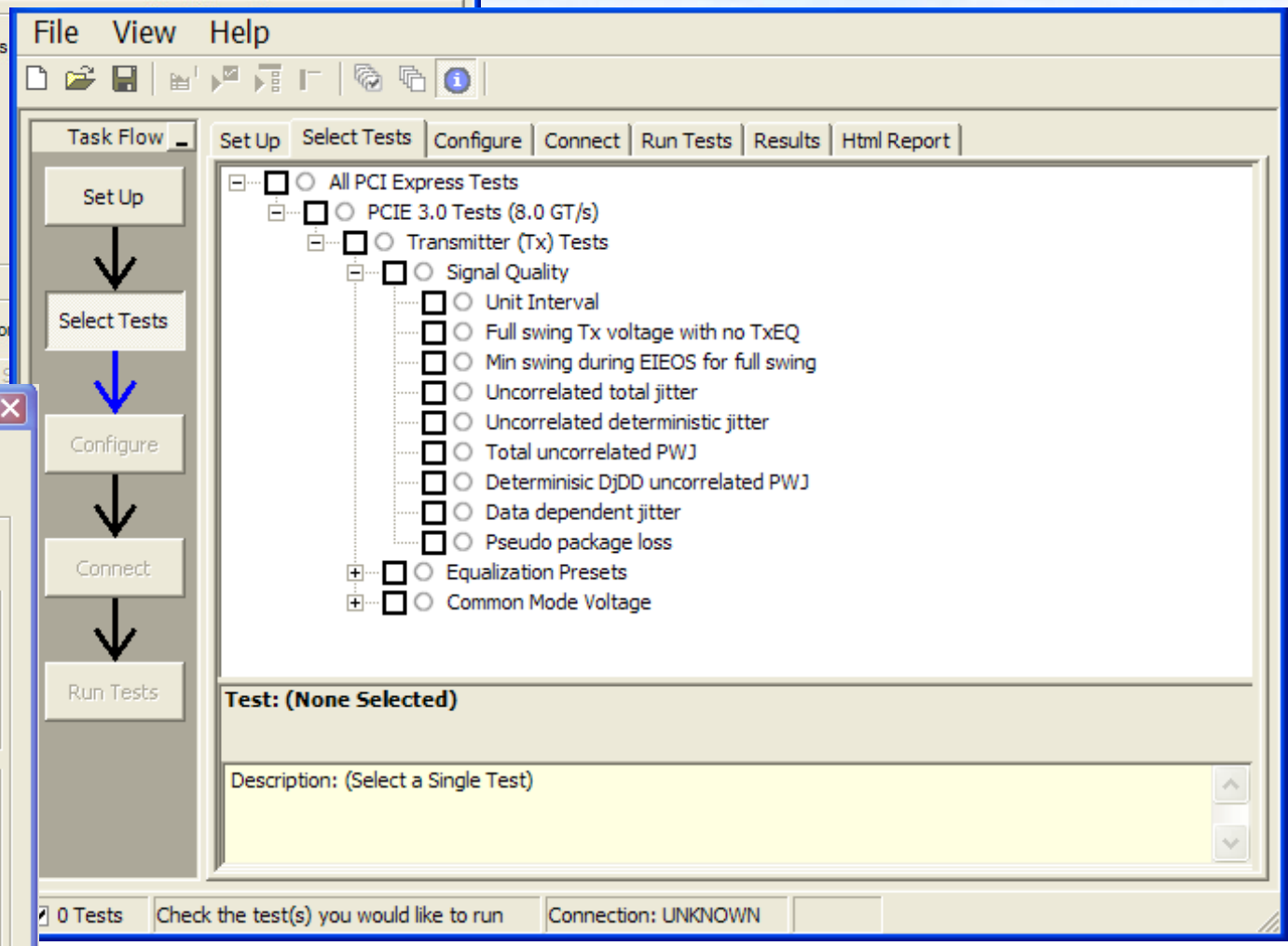


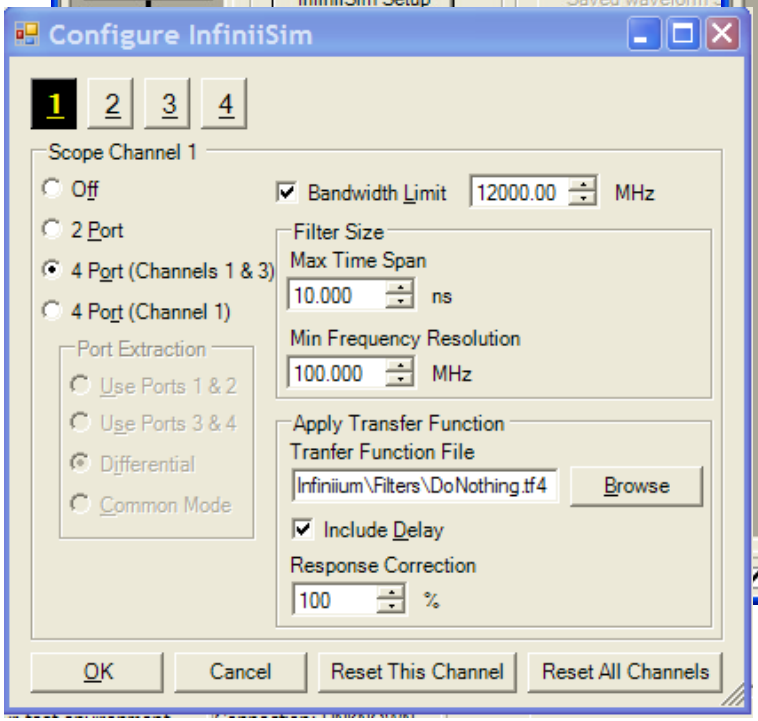
Add-in Card Testing



Agilent N5393C TX Test Application







N5393C TX Test Application Preset Tests

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

De-emphasis Result for each Gen3 Preset

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	Tx, Full swing Tx voltage with no TxEQ (PCIE 3.0, 8.0 GT/s)	9[illegible]1mV	39.8 %	800.0m V <= VALUE <= 1.3000 V
✓	0	1	Tx, De-emphasis Preset #0 (PCIE 3.0, 8.0 GT/s)	-6.1397dB	45.3 %	-7.5000 dB <= VALUE <= -4.5000
✓	0	1	Tx, De-emphasis Preset #1 (PCIE 3.0, 8.0 GT/s)	-3.6954dB	40	
✓	0	1	Tx, De-emphasis Preset #2 (PCIE 3.0, 8.0 GT/s)	-4.2832dB	46	
✓	0	1	Tx, De-emphasis Preset #3 (PCIE 3.0, 8.0 GT/s)	-2.2623dB	38	
✓	0	1	Tx, Preshoot Preset #5 (PCIE 3.0, 8.0 GT/s)	1.7665dB	43	
✓	0	1	Tx, Preshoot Preset #6 (PCIE 3.0, 8.0 GT/s)	2.2379dB	36	
✓	0	1	Tx, De-emphasis Preset #7 (PCIE 3.0, 8.0 GT/s)	-6.0455dB	48	
✓	0	1	Tx, Preshoot Preset #7 (PCIE 3.0, 8.0 GT/s)	3.5287dB	48	
✓	0	1	Tx, De-emphasis Preset #8 (PCIE 3.0, 8.0 GT/s)	-3.2598dB	38	
✓	0	1	Tx, Preshoot Preset #8 (PCIE 3.0, 8.0 GT/s)	3.2355dB	36	
✓	0	1	Tx, Preshoot Preset #9 (PCIE 3.0, 8.0 GT/s)	3.6573dB	42	
✓	0	1	Tx, De-emphasis Preset #10 (PCIE 3.0, 8.0 GT/s)	-7.7604dB	29	

✓ Tx, Preshoot Preset #7 (PCIE 3.0, 8.0 GT/s)

Reference: PCI Express Base Specification, Rev 3.0, Section 4.3.3.5.2, Table 4-16

Test Summary: Pass | Test Description: The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.

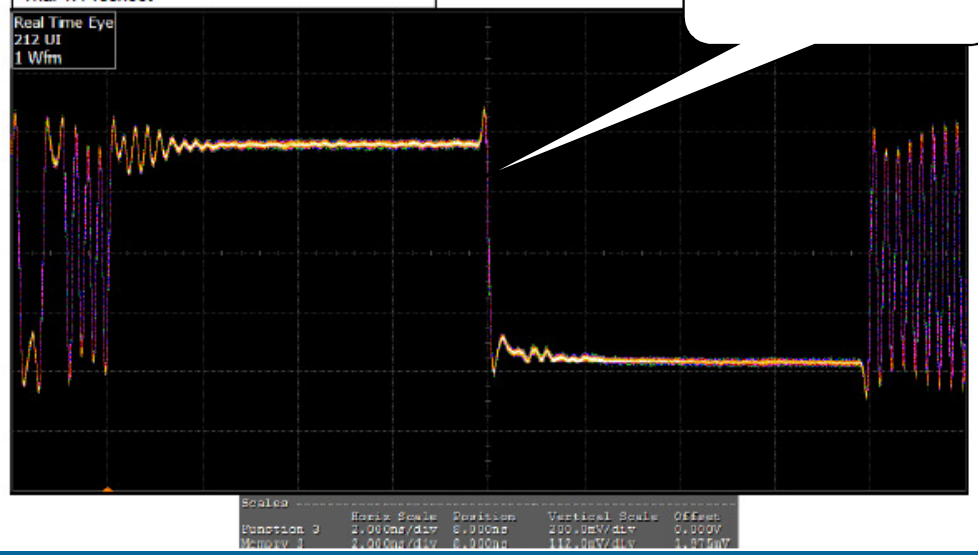
Test Limits: [2.5000 dB to 4.5000 dB] **Preshoot** 3.5287dB

Result Details

Vb P7 406.450mV | Vb P2 610.160mV | Lane Number Lane 0 | Connection

Trial 1

Trial 1: Preshoot



Report Detail includes waveform captures useful for debug.

Tradition Method for De-Embedding Cable Losses

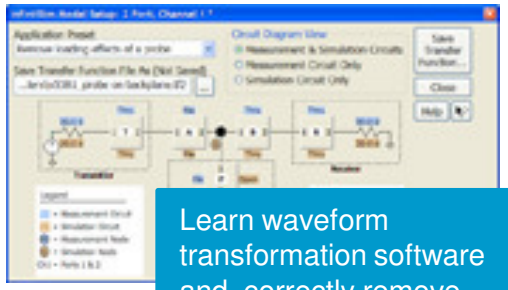
Option 1: Six steps (you would need to do the following)

Find a VNA

Find a someone that knows how to use a VNA and measure the cable

Create s-parameter file

Save s-parameter file to USB drive and load on scope

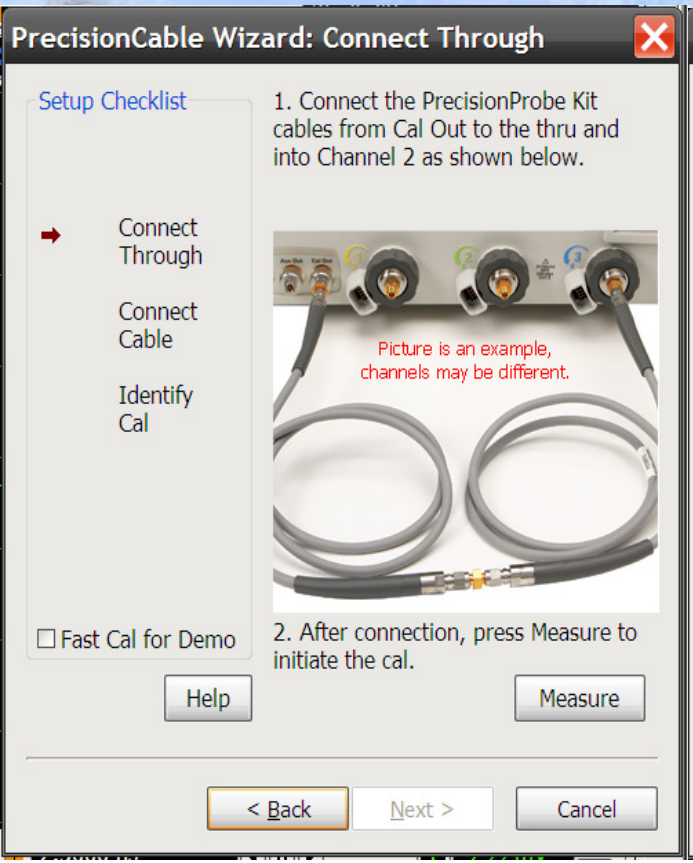


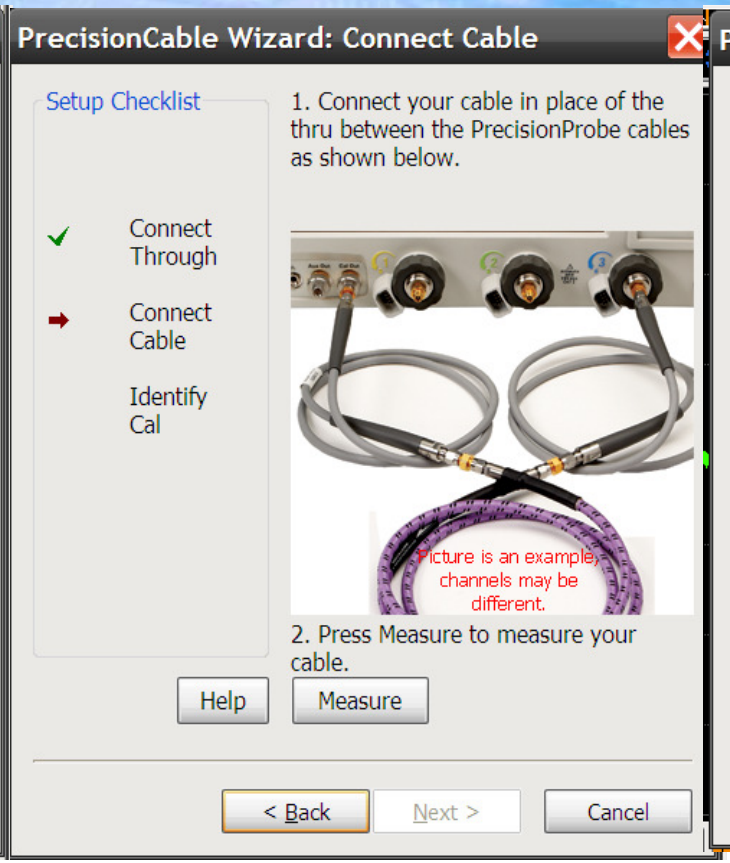
Learn waveform transformation software and correctly remove loss

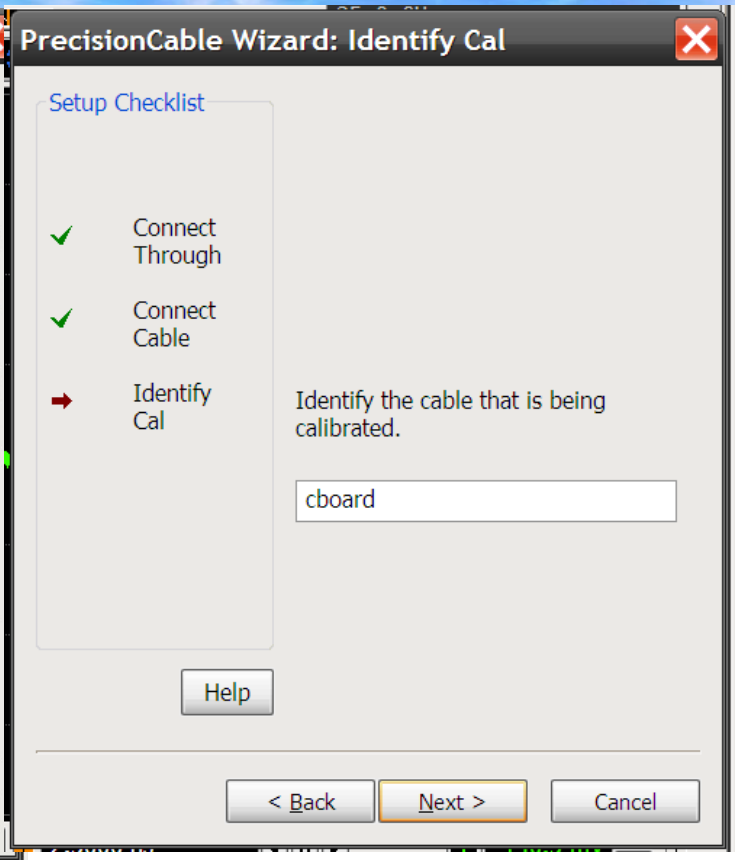
Analyze the data

Option 2: Purchase the highest quality cables you can afford and accept those losses in your measurements.

PrecisionProbe characterizes and corrects in three easy steps



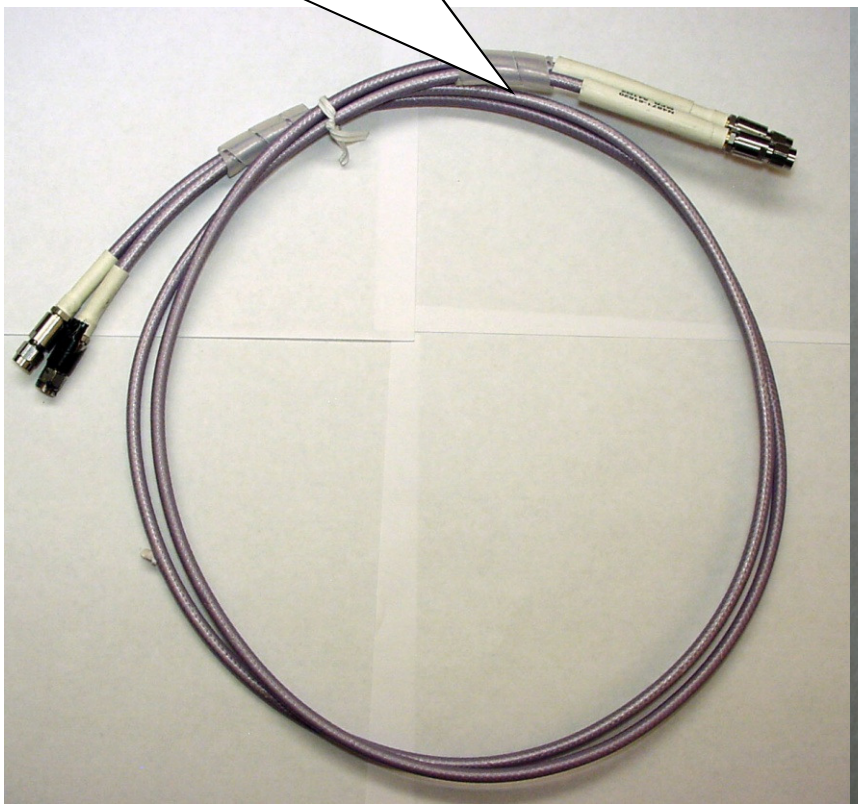




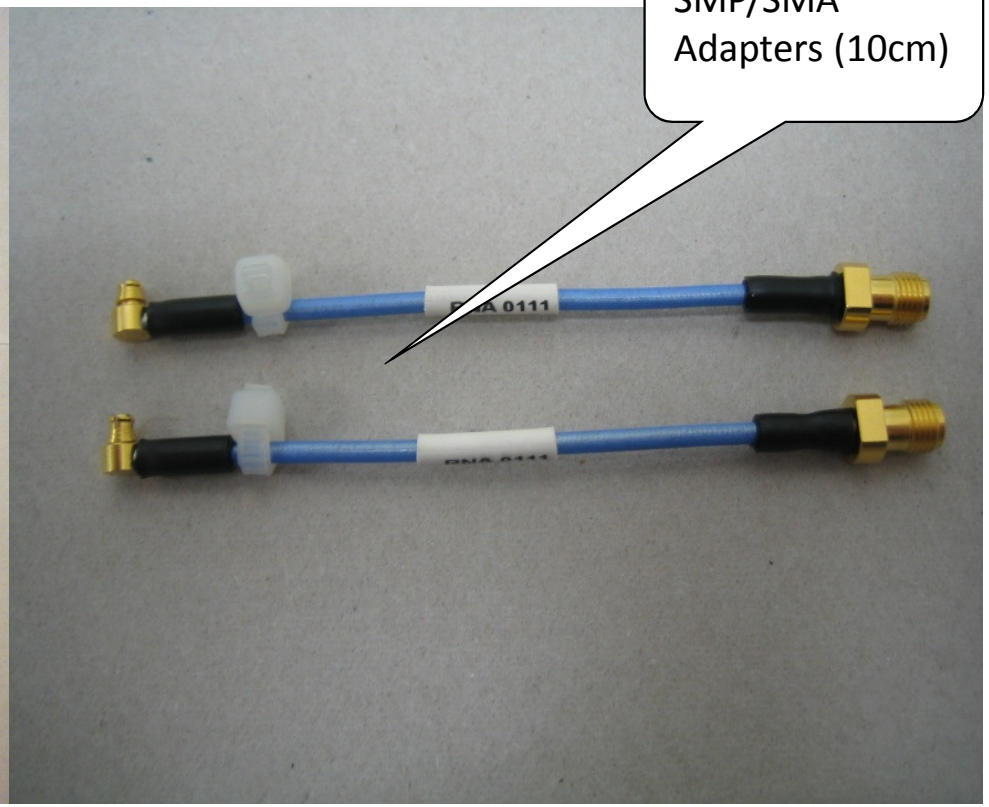
1. Measure Reference Plane
2. Measure loss of DUT cable
3. Save File

Source Cable for PCIe 3.0

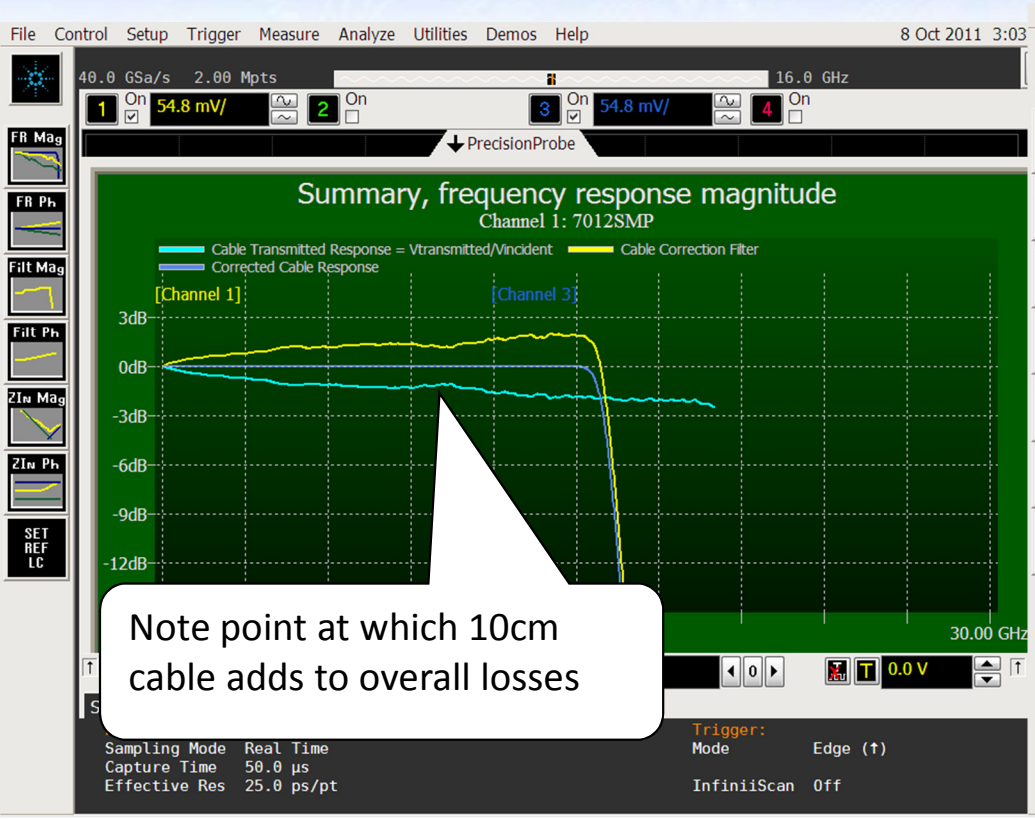
Low Loss Phase Matched 3.5mm SMA compatible precision cables (1M).



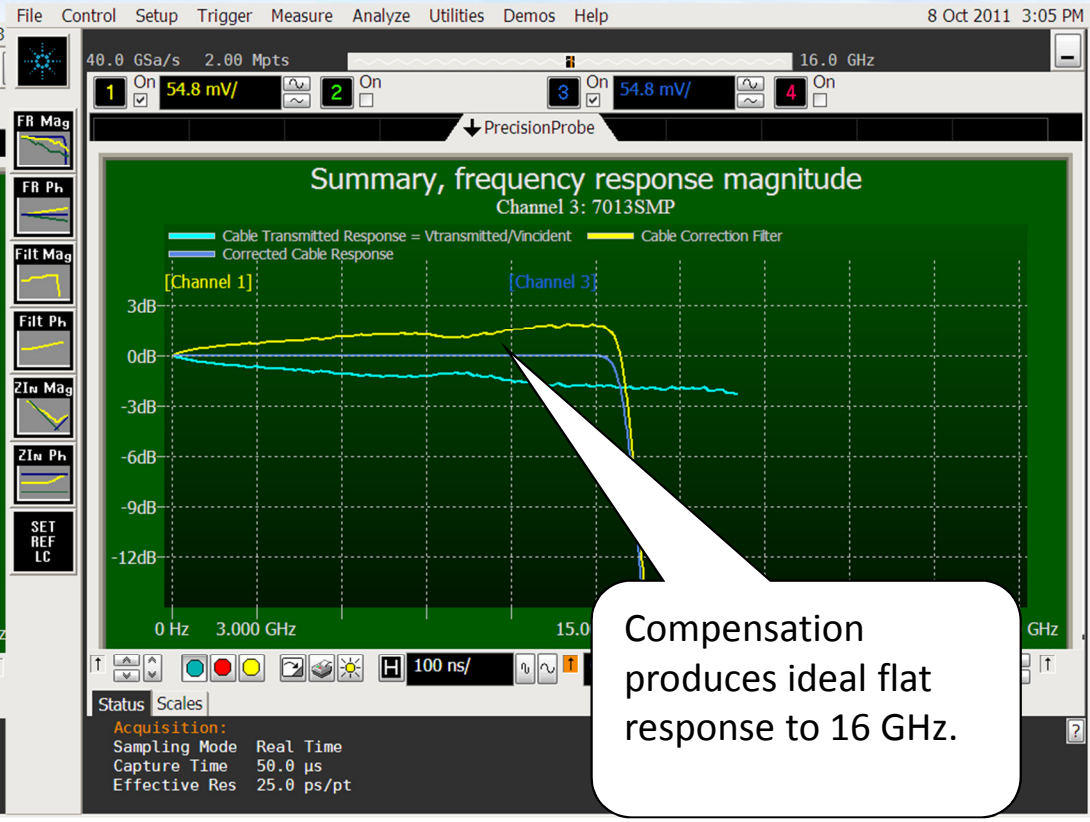
SMP/SMA Adapters (10cm)



Frequency Response of Each Cable



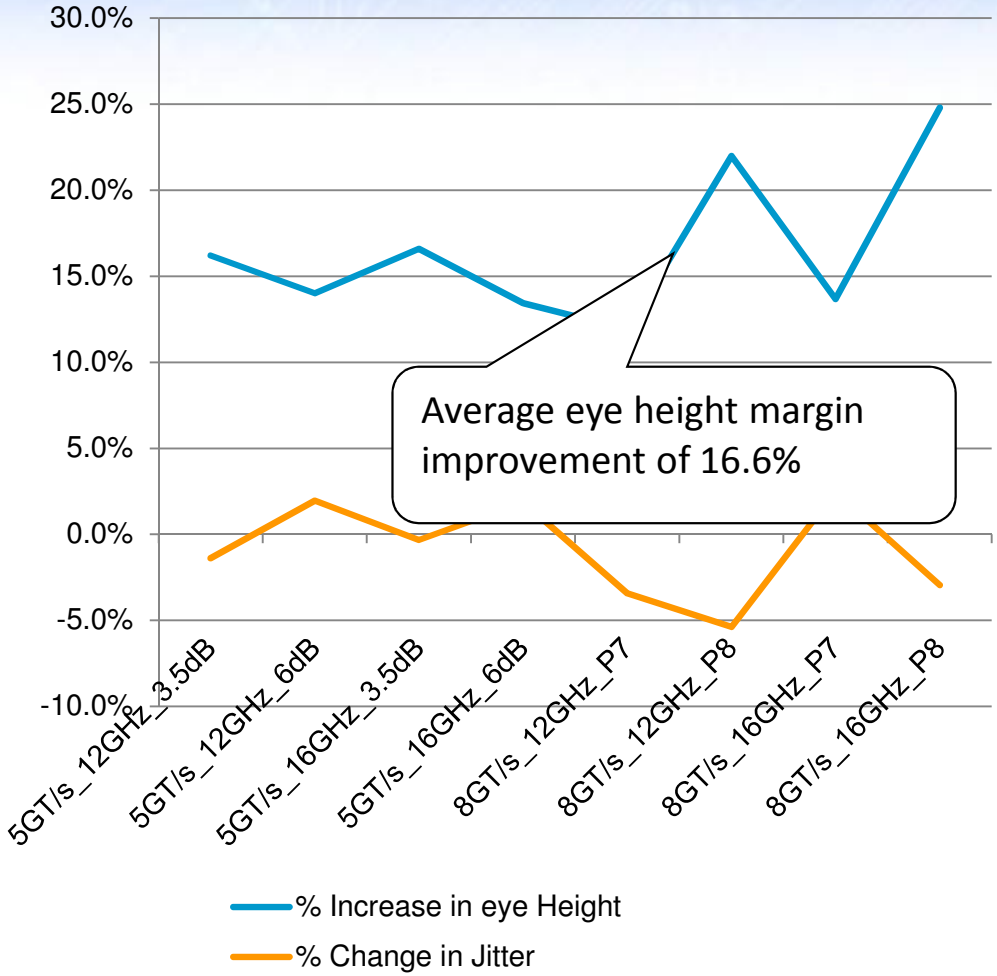
Note point at which 10cm cable adds to overall losses



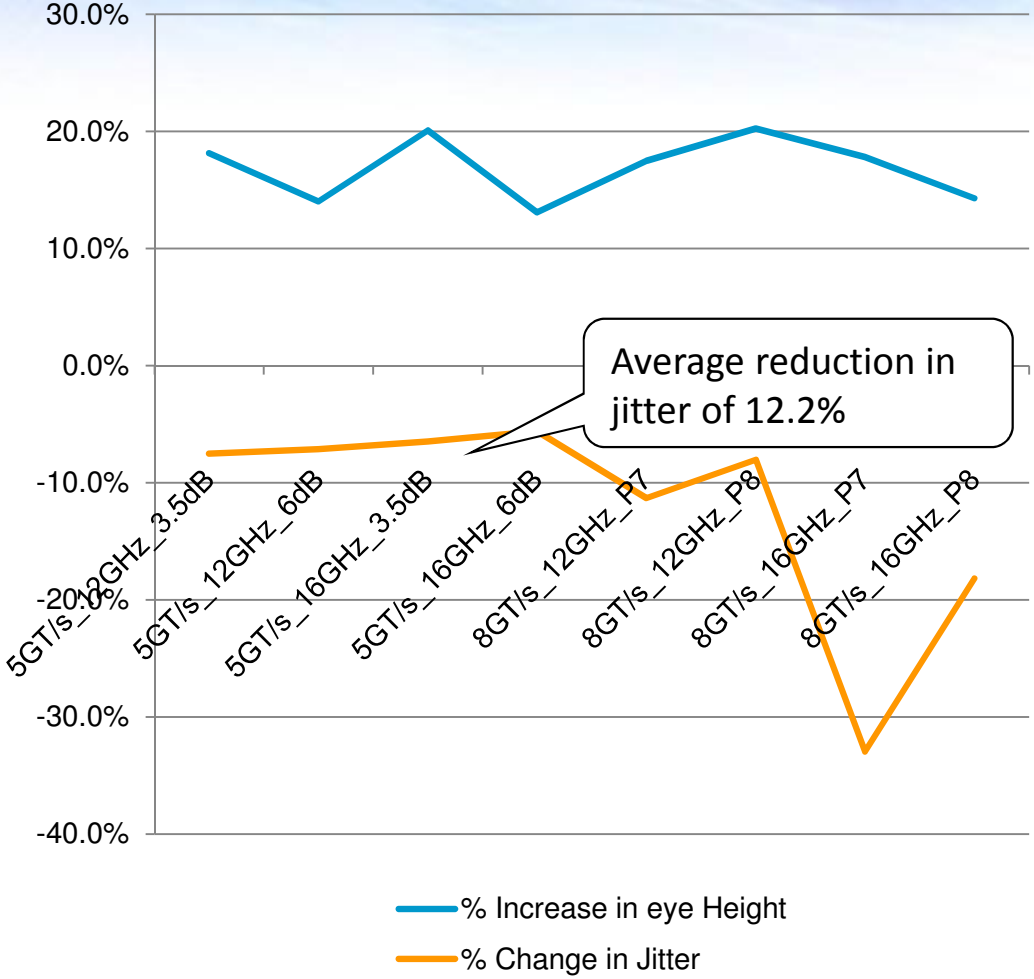
Compensation produces ideal flat response to 16 GHz.

How much of a difference?

Add-in Card Precision Probe
Eye Height and Jitter Differences



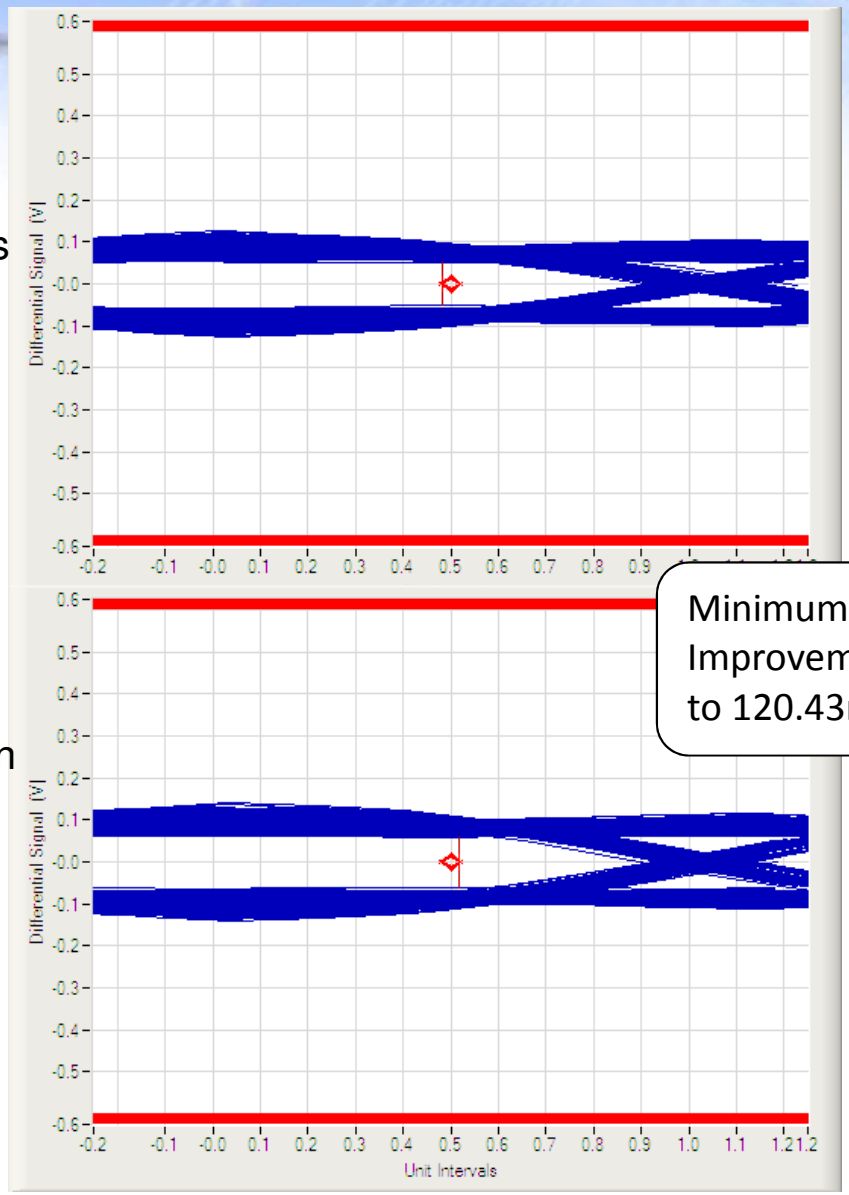
Root Complex Precision Probe
Eye Height and Jitter Differences

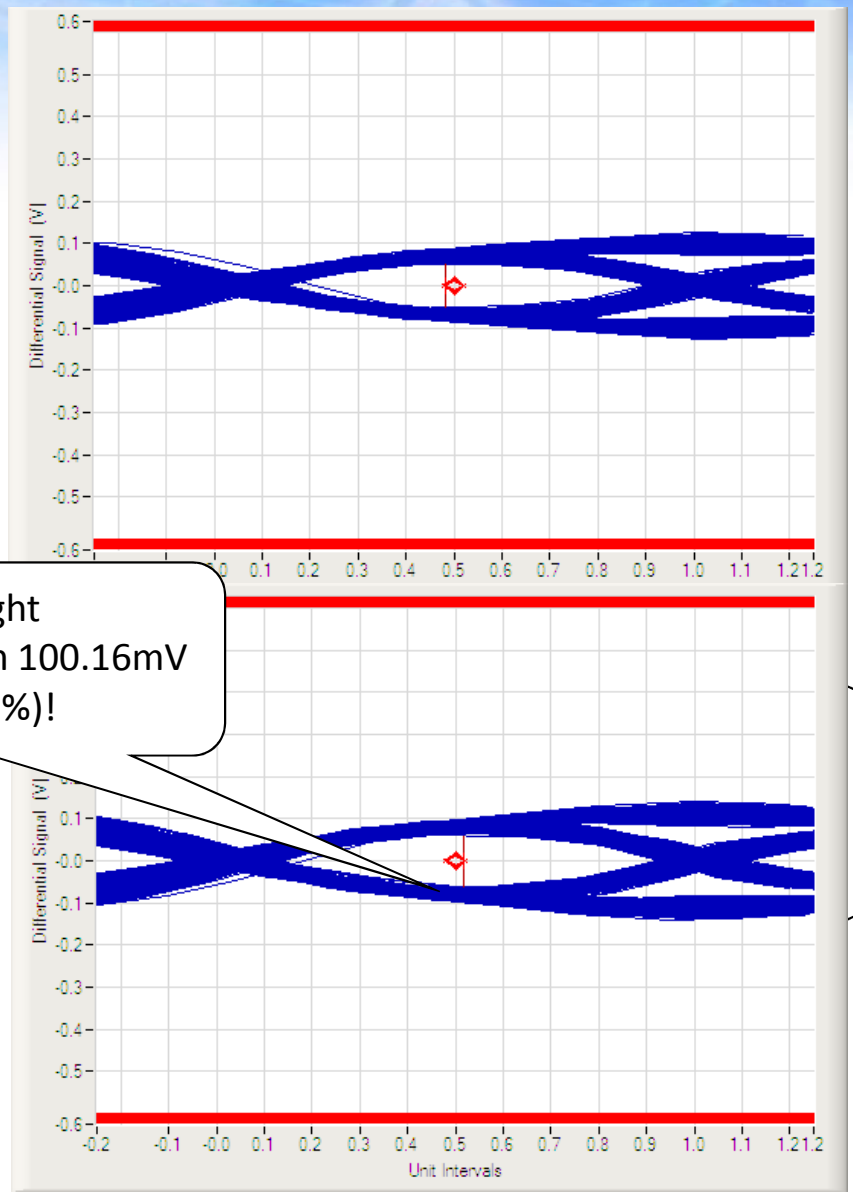


Frequency Response of Each Cable

Raw Cables

Precision Probe Cables





Minimum Eye Height Improvement from 100.16mV to 120.43mV (20.2%)!

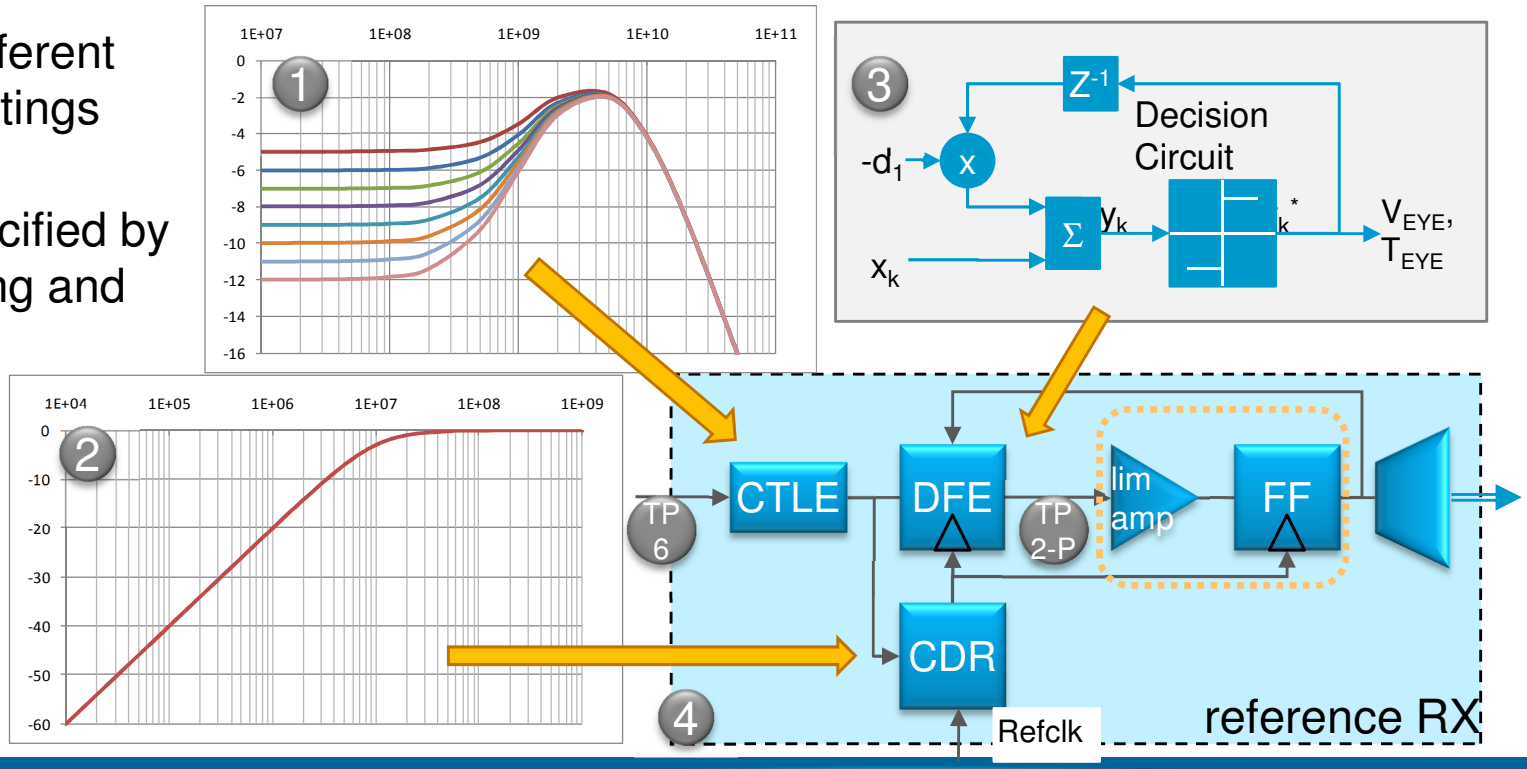
PCIe 3.0 Receiver Testing Preview (BASE/CEM)

Practical considerations of 8GT/s Signaling on RX Architecture

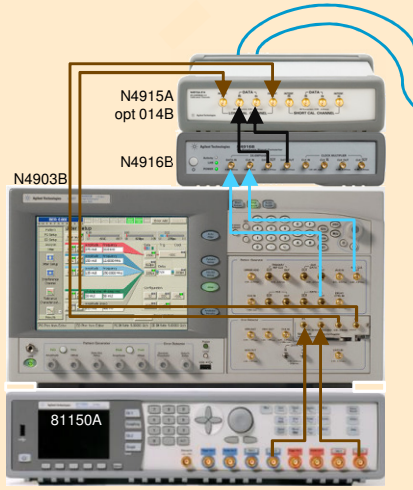
- Effective data rate shall be doubled
- Existing infrastructure of PCs and servers shall be reusable, which means:
  all PCIe2-compliant channels shall also be compliant with PCIe3
  simulations showed: TX-de-emphasis not sufficient to achieve desired eye opening

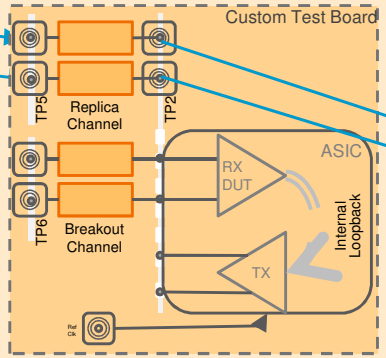
⇨ **RX equalization is necessary**

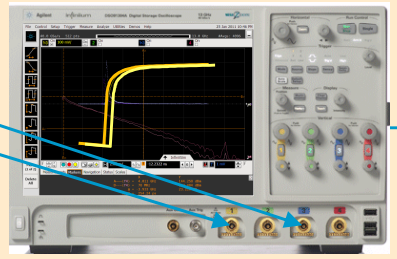
1. CTLE with seven different "DC-attenuation" settings peaking at 4 GHz
2. Reference CDR specified by OJTF with no peaking and 10MHz BW
3. One tap DFE with a limit for d1 of +/- 30mV
4. Π-type reference package model also specified



Comparison of Calibration Methods Base vs CEM

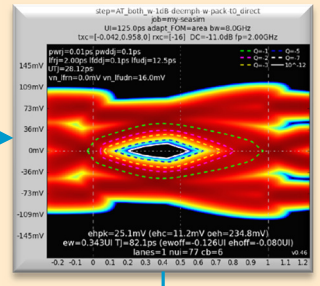


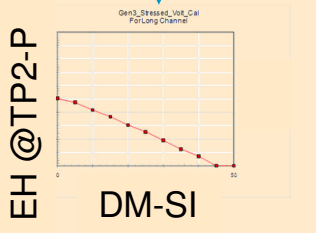




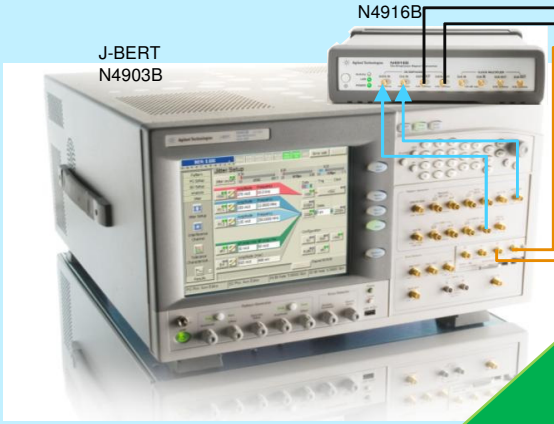
input parameters:
RJ = 2ps,rms
SJ = 0.1UIpp
DM-SI =14mVpp

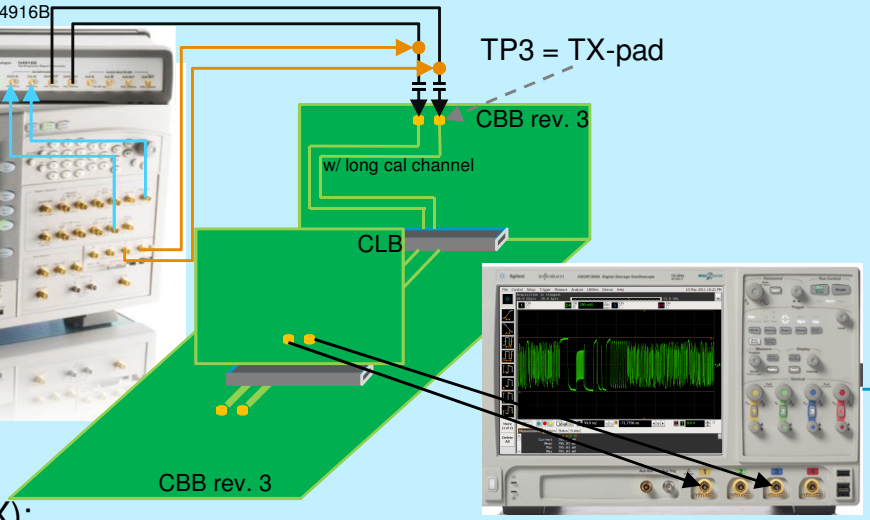
SEASIM





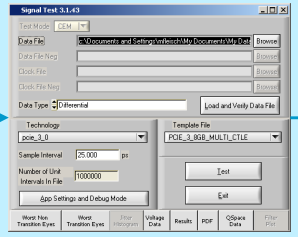
Base-Spec method utilizing Seasim :
averaged step response,
simulated pattern & impairments & ref RX

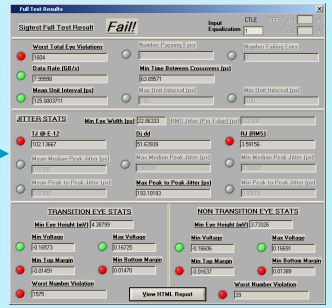




TP6/TP2 = RX-pin

SigTest SW

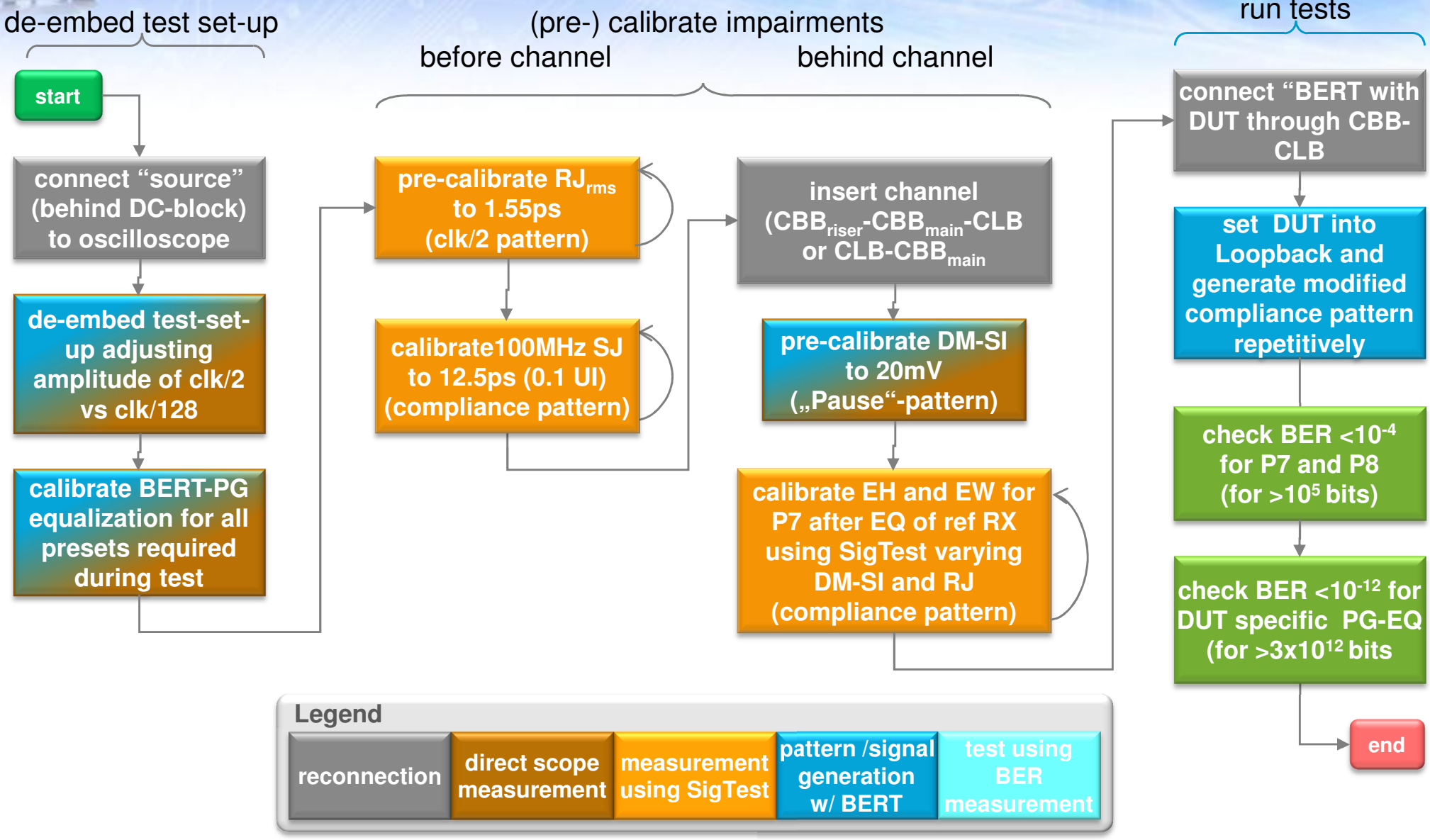




TP2-P = RX behind EQ

CEM method
utilizing SigTest (for ref RX):
compliance pattern w/ impairments „on“ w/o scope averaging

Calibration and Test Flow Chart



Set-Up for Calibration of RX Test Signal

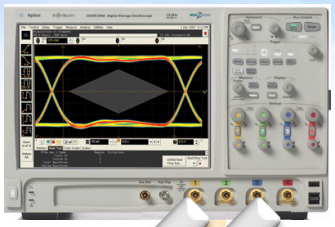
N4916B

assymetrical splitters

DC-blocks

2/14 dB

2/14 dB



For Calibration

before channel :

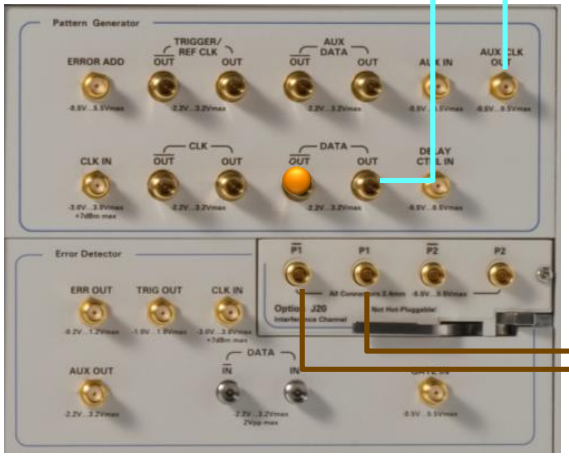
cables ① via SMP=>SMA adaptors to oscilloscope

after channel:

cables ① to RX SMP connectors of CBB-riser card or CLB and

cables ② from TX SMP connectors of CLB or CBB-main card to oscilloscope

N4903B

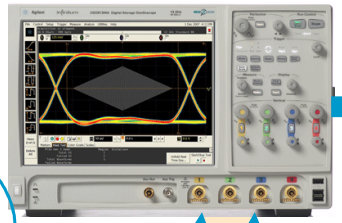


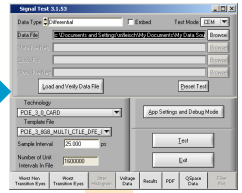
DM-SI

①

①

CBB + CLB





②

TP3 = TX-pad

numbering of test points according to base specification

TP6 = RX-pin

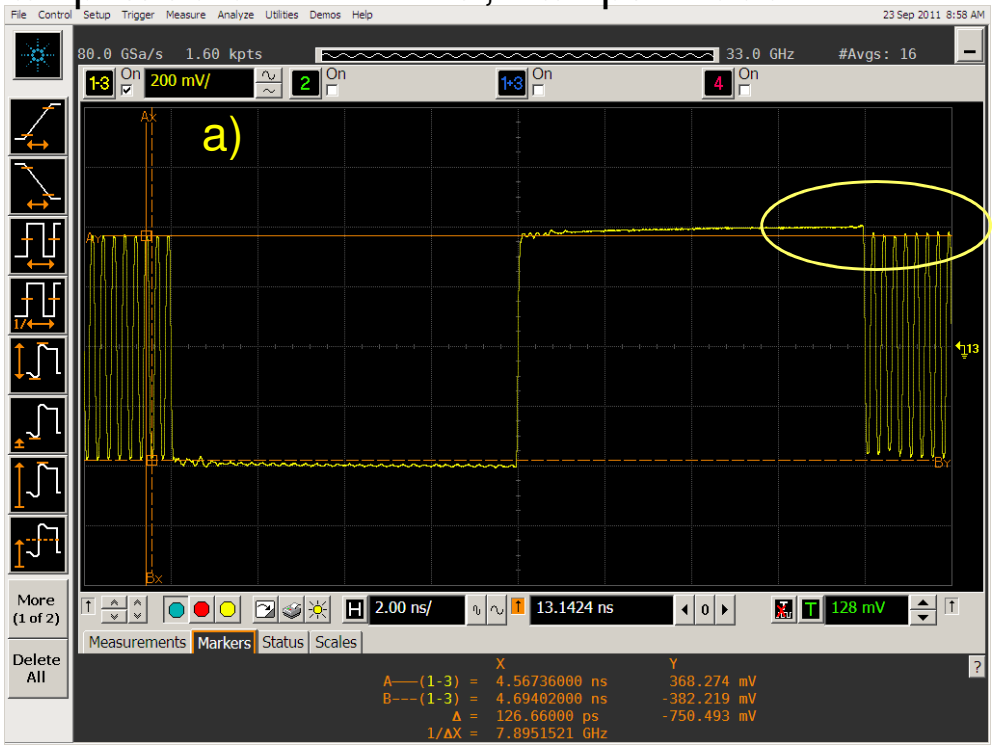
TP2-P = RX behind EQ

- Agilent J-BERT N4903B
  with internal jitter generation and
  option J20 for 2.1GHz DM-SI generation
- N4916B de-emphasis signal converter
- DC-blocks and asymmetrical adders

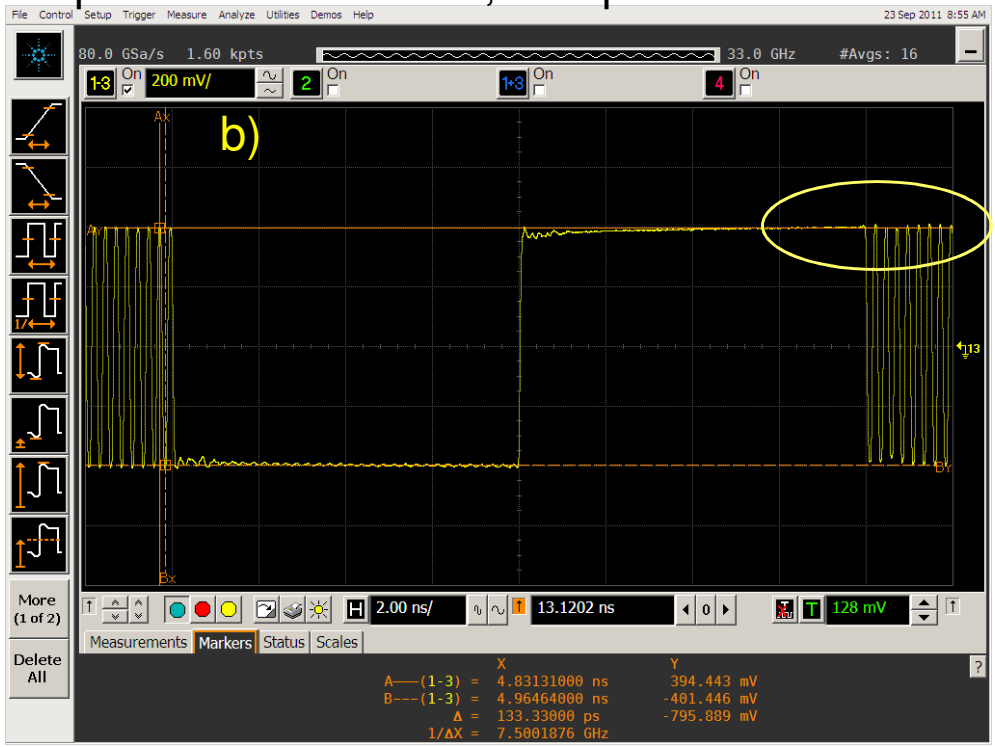
De-embedding of Test Set-up

- Cables, couplers, DC-blocks … not ideal in frequency response
- Slightly lower amplitude for clk/2 (HF signal) vs clk/128 signal (LF-signal)
- Correction of frequency response (same amplitude for HF and LF) per de-emphasis post-cursor (Note: per definition: amplitude correction required)

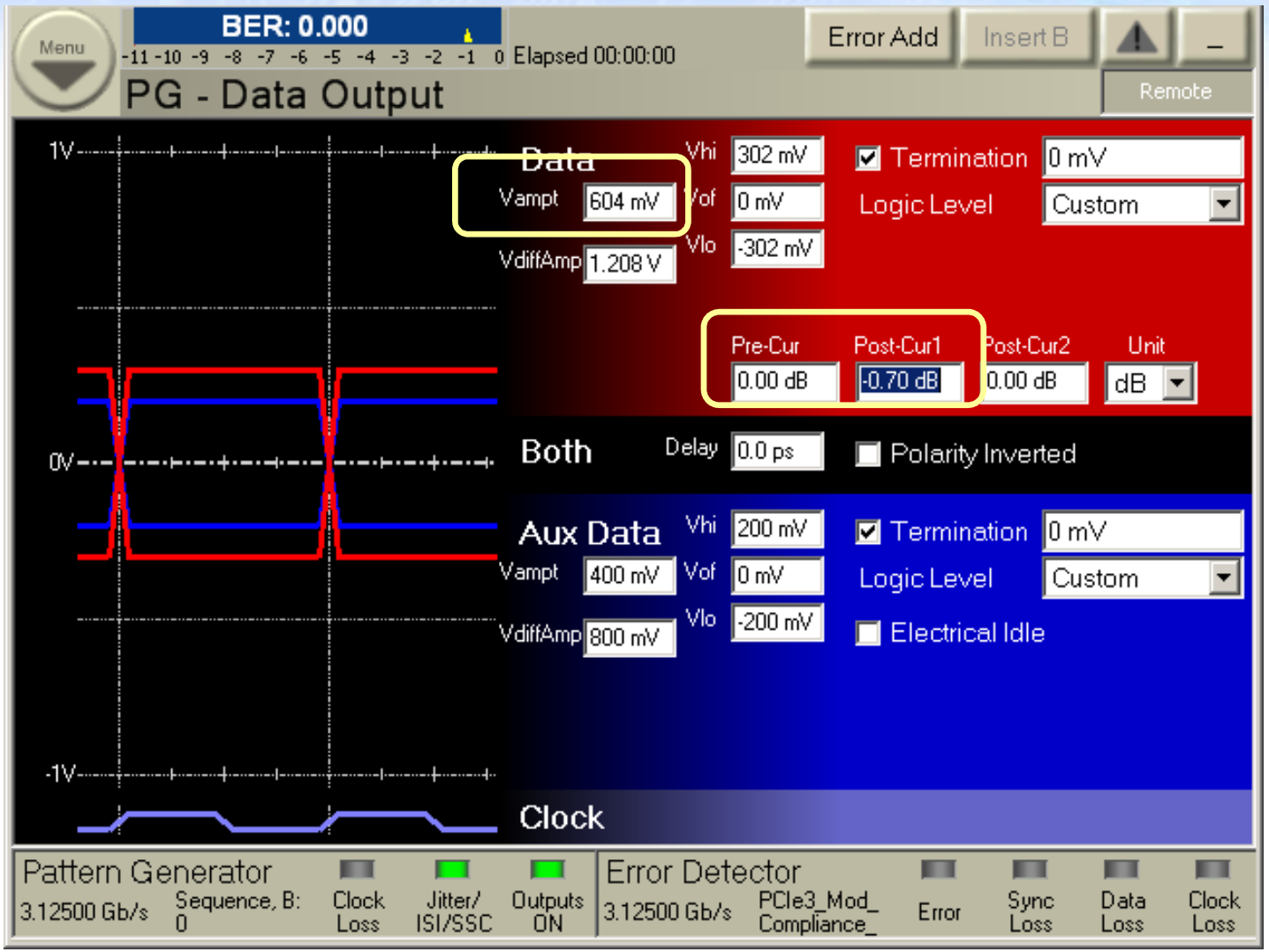
measured amplitude of HF signal ~ 750mV
de-emphasis, Post-Cur1 = 0.0dB
amplitude of BERT-PG, Vampt = 558 mV



measured amplitude of HF signal ~ 800mV
de-emphasis Post-Cur1 = - 0.70dB
amplitude of BERT-PG, Vampt = 604 mV



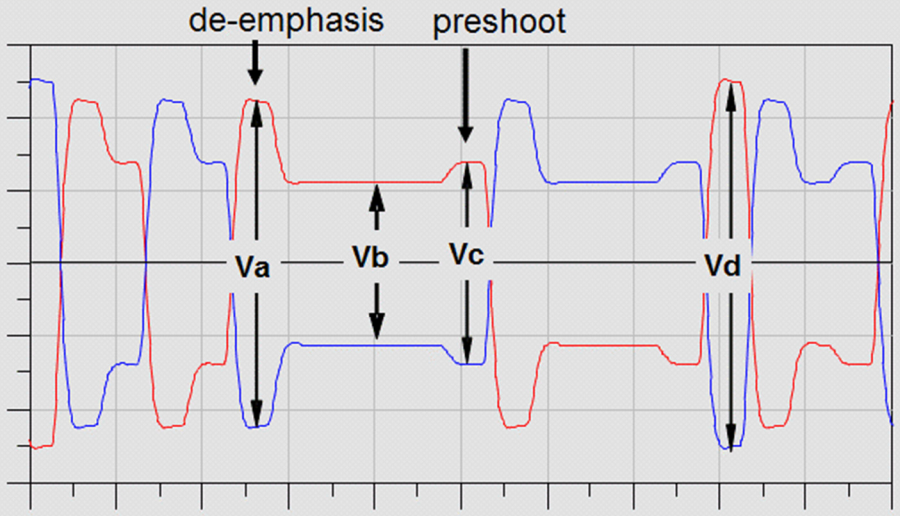
J-BERT GUI Data Output Page, De-embedding



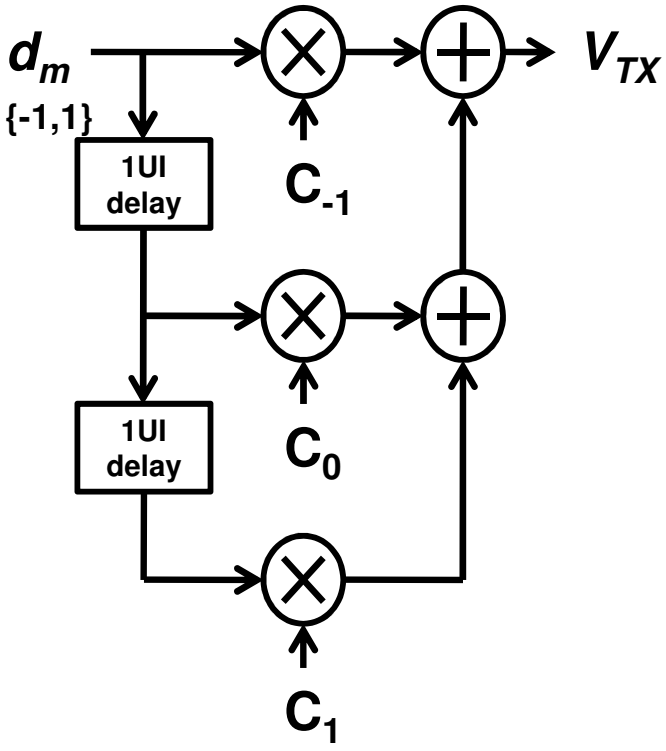
set-up of signal amplitude Vampt and de-emphasis Post-Curs1

Possible TX EQ Settings and Presets

Preset Number	Preshoot		De-emphasis		Va/mV	Vb/mV	Vc/mV
	(dB)	Tol.: ± dB	(dB)	Tol.: ± dB	@ Vd = 800 mV		
P4	0		0		800	800	800
P1	0		-3.5	1	800	534	534
P0	0		-6	1.5	800	400	400
P9	3.5	1	0		534	534	800
P8	3.5	1	-3.5	1	600	400	600
P7	3.5	1	-6	1.5	640	320	480
P5	1.9	1	0		640	640	800
P6	2.5	1	0		600	600	800
P3	0		-2.5	1	800	600	600
P2	0		-4.4	1.5	800	480	480

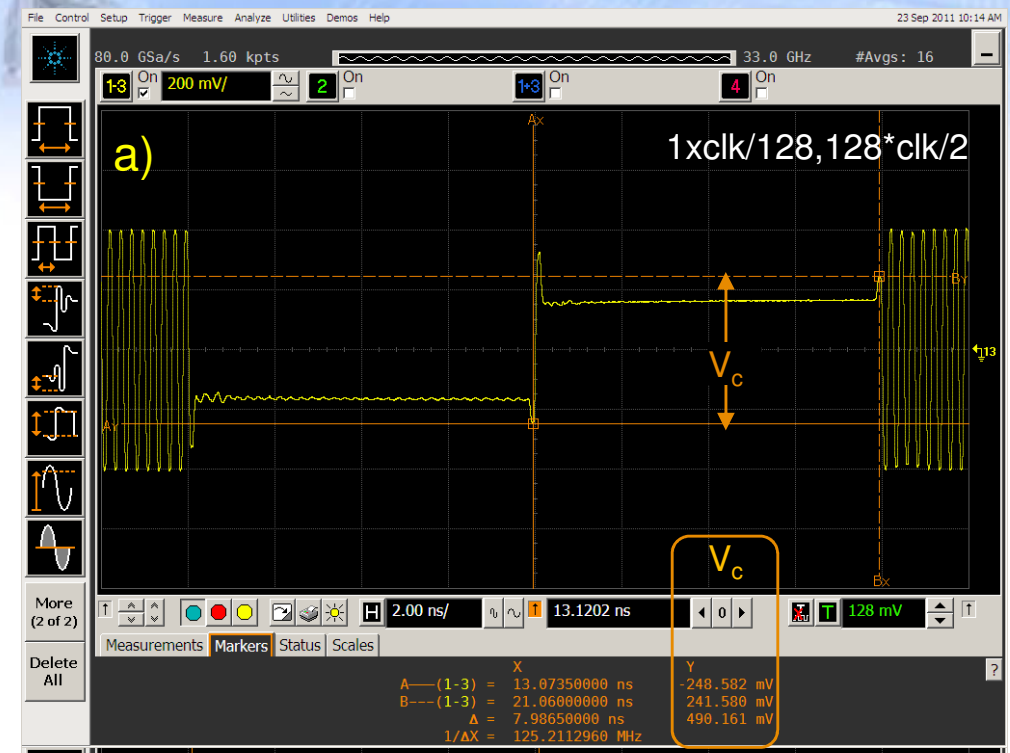


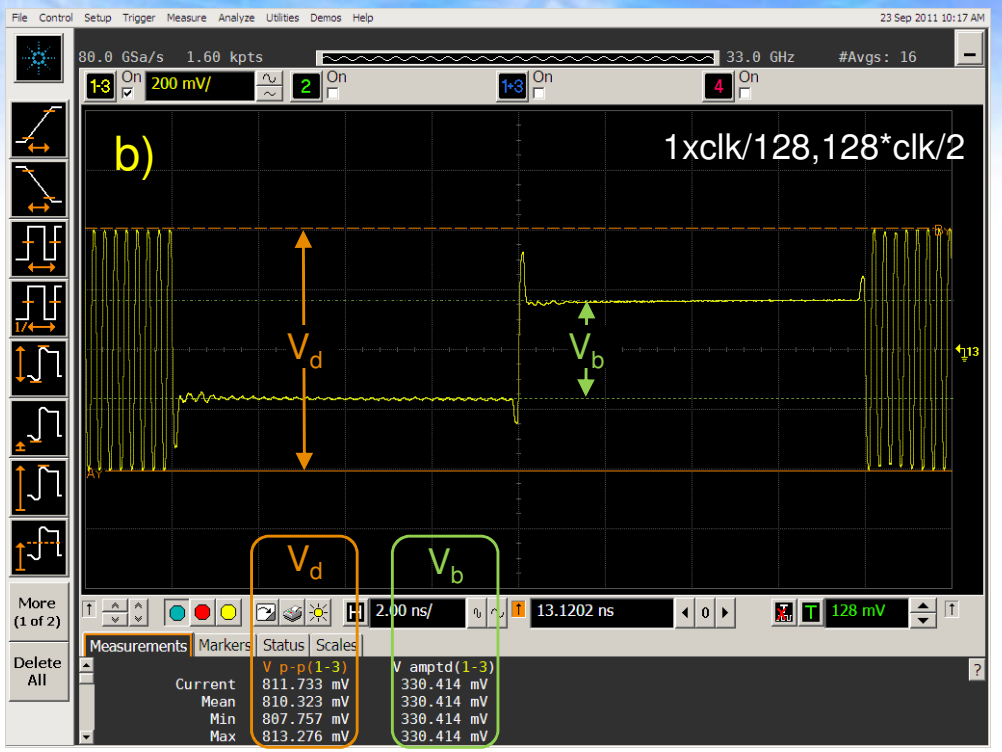
De-emphasis = 20 $\log_{10}$Vb/Va
Preshoot = 20$\log_{10}$Vc/Vb
Boost = 20$\log_{10}$ Vd/Vb



$$V_{TX} = V_{PK} \sum_{n=\{-1,0,1\}} c_n d_{m-n} \text{ and } \sum_{n=\{-1,0,1\}} |c_n| = 1$$

BERT-PG Calibration for P7 with HF-LF-pattern

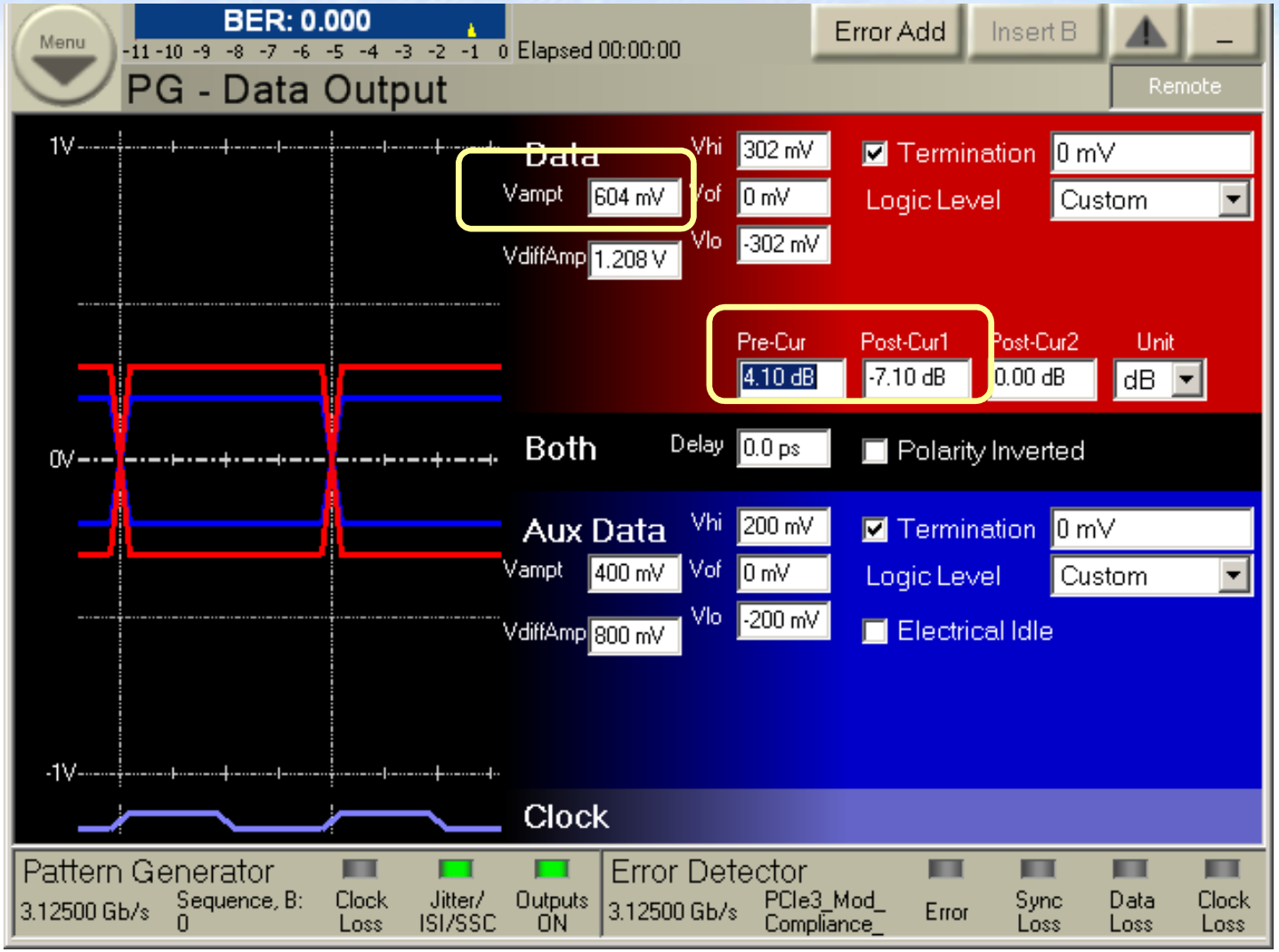




V_a [mV]	V_b [mV]	V_c [mV]	V_d [mV]
658	332	494	810

	Pre-shoot	De-emphasis	Boost
measured [dB]	3.45	- 5.94	7.75
ideal [dB]	3.5	- 6.0	7.9

J-BERT GUI Data Output Page, EQ-P7

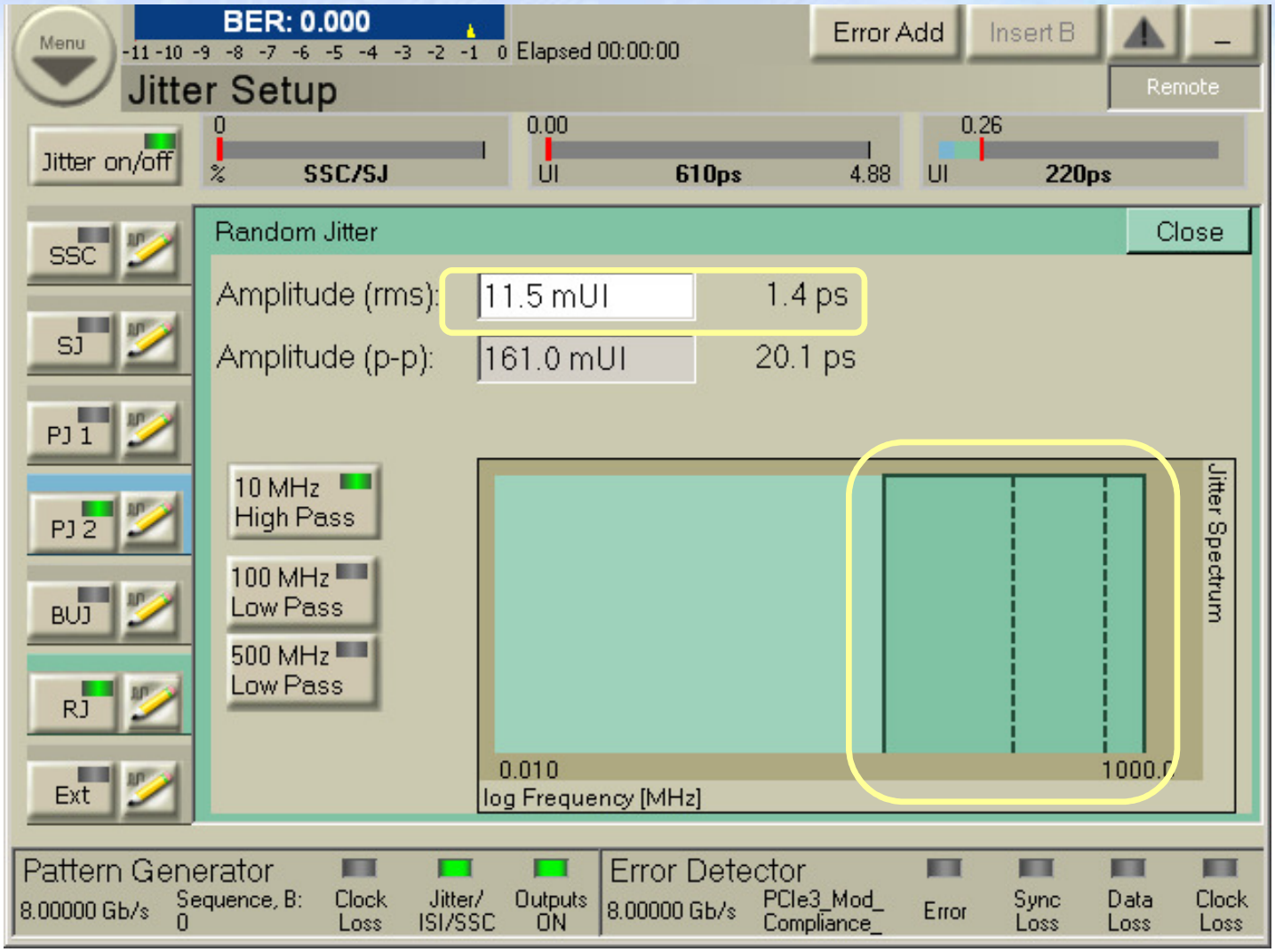


set-up of signal amplitude Vampt, pre-shoot PreCur and de-emphasis Post-Curs1

Target Values for Calibration

Parameter	Min	Max	Unit	SigTest	
				Technology	Template
Vpp		800	mV	N/A	N/A
$V_{RX\text{-}EH\text{-}8G}$ Eye Height		50	mV	PCI_3_0_CARD	PCIE_3_8GB_MULTI_CTLE_DFE_80ps_50mV
$T_{RX\text{-}EH\text{-}8G}$ Eye Width		0.36 (45)	UI (ps)	PCI_3_0_CARD	PCIE_3_8GB_MULTI_CTLE_DFE_80ps_50mV
Rj (Random Jitter)	1.5	1.6	ps RMS	PCI_3_0_RX_CAL	PCIE_3_8GB_Rx_Sj_CAL
Sj (Sinusoidal Jitter) 100 MHz	12.5	14.5	ps PP	PCI_3_0_RX_CAL	PCIE_3_8GB_Rx_Sj_CAL
Differential Mode Sinusoidal Interference at 2.1 GHz	14	15	mV PP	N/A	N/A

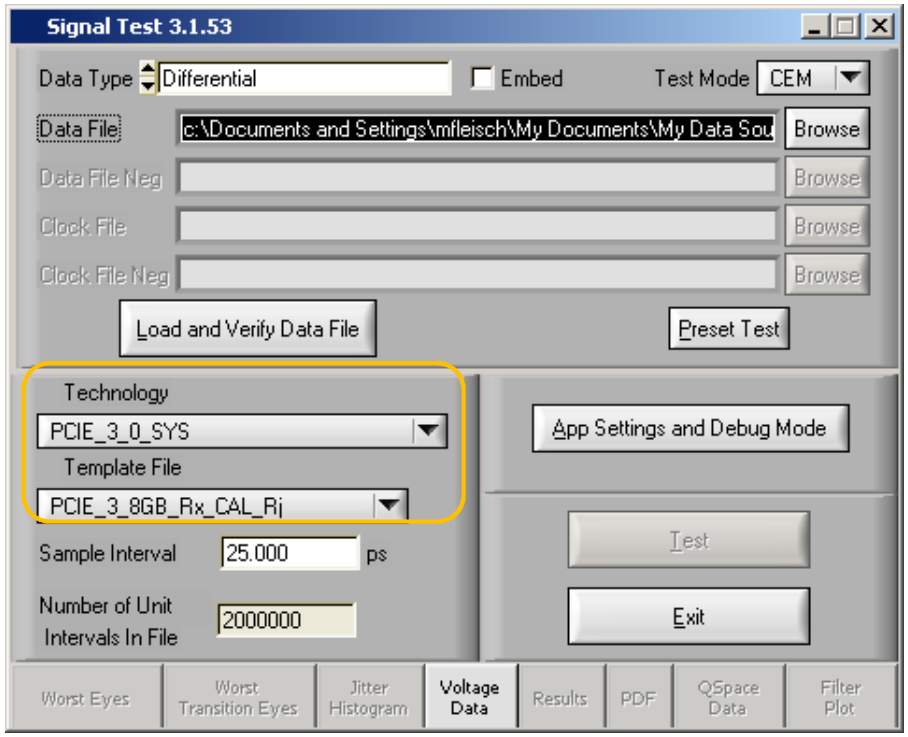
J-BERT GUI Jitter Setup Page, Set-up of RJ



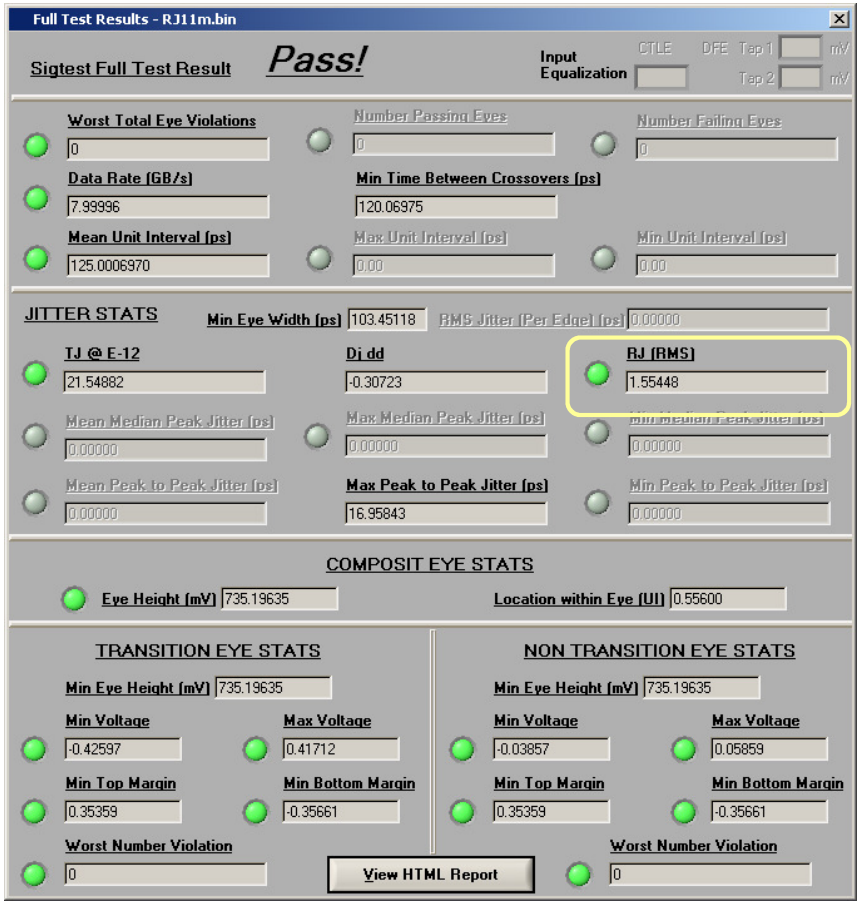
set-up of RJ-amplitude (rms) and frequency range of 10-MHz-1GHz utilizing 10MHz high pass filter

SigTest SW
Used for Calibration of Jitter Components,RJ

- For jitter decomposition and measurement the SEG provides the SigTest SW tool to rule out discrepancies arising from proprietary jitter separation algorithms implemented on the oscilloscopes of different vendors



input panel



result panel

SigTest SW
Used for Calibration of Jitter Components,RJ

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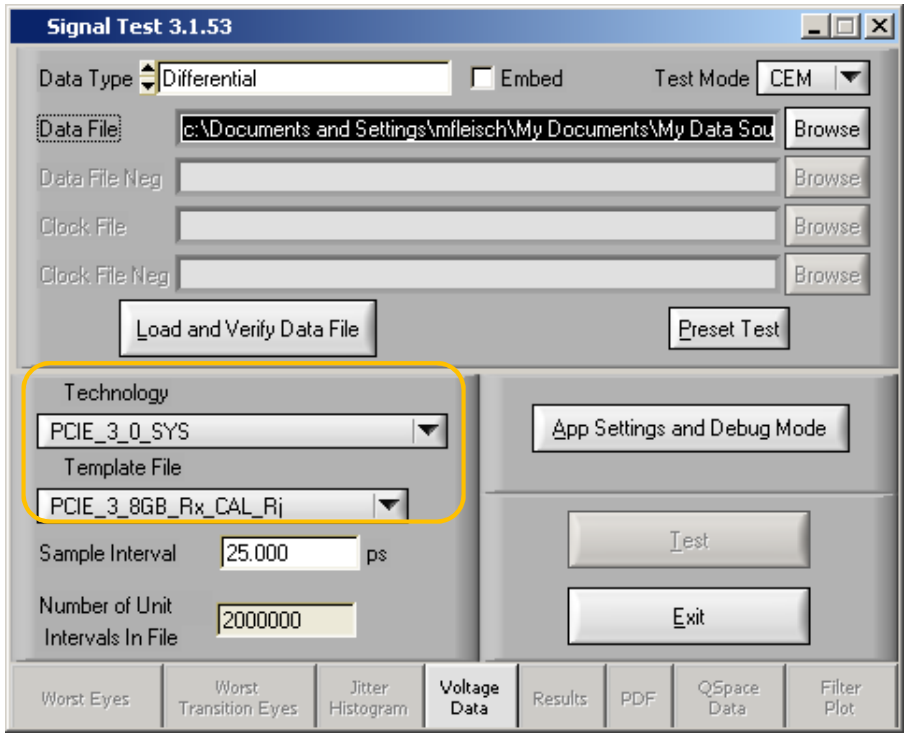
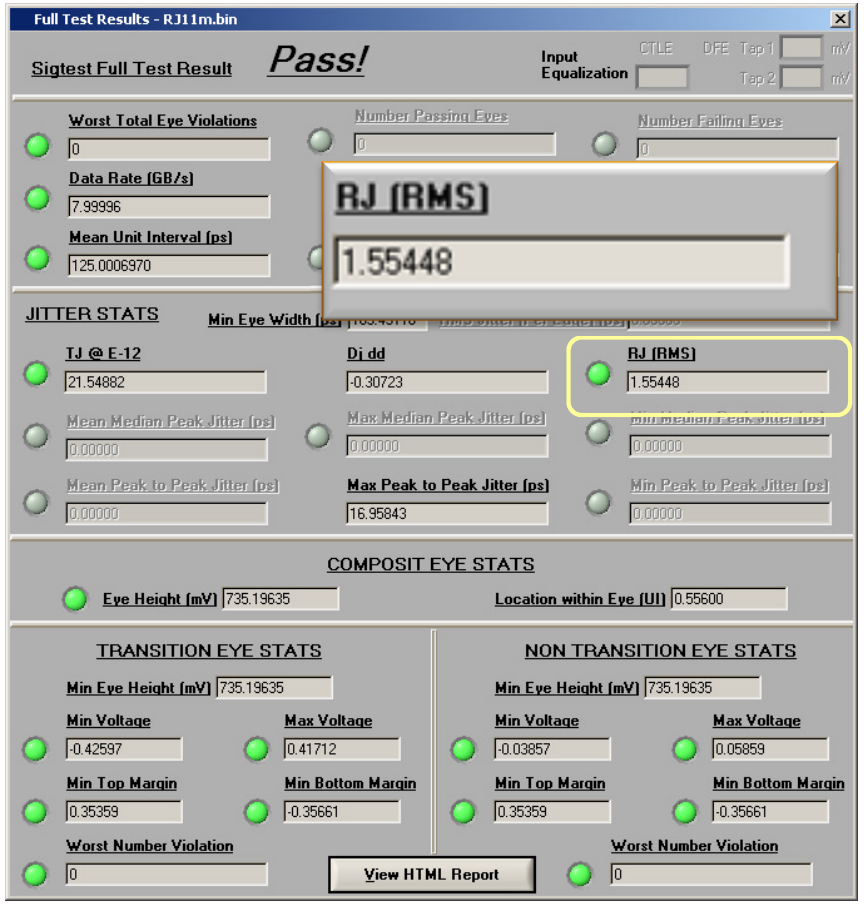
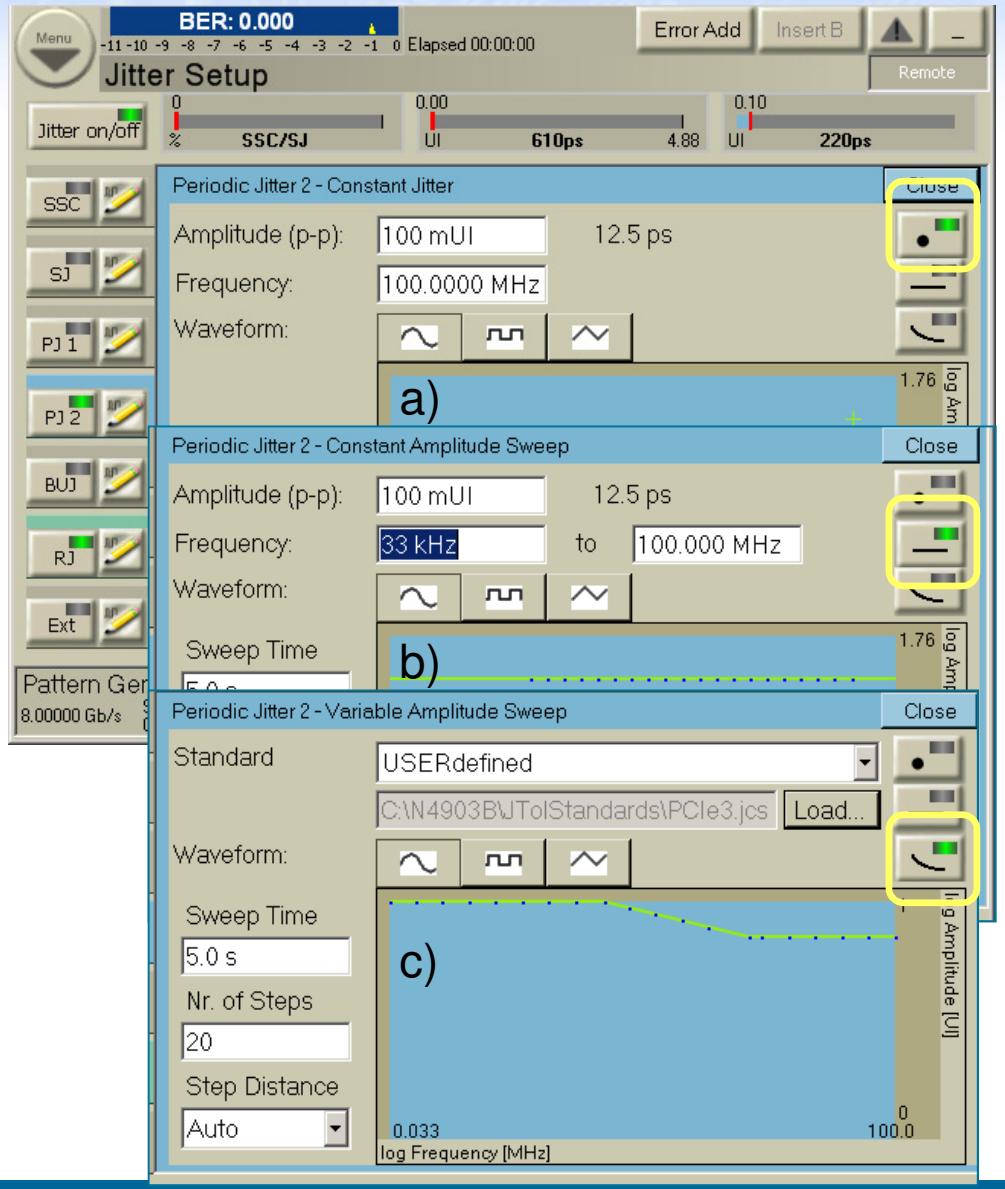


input panel



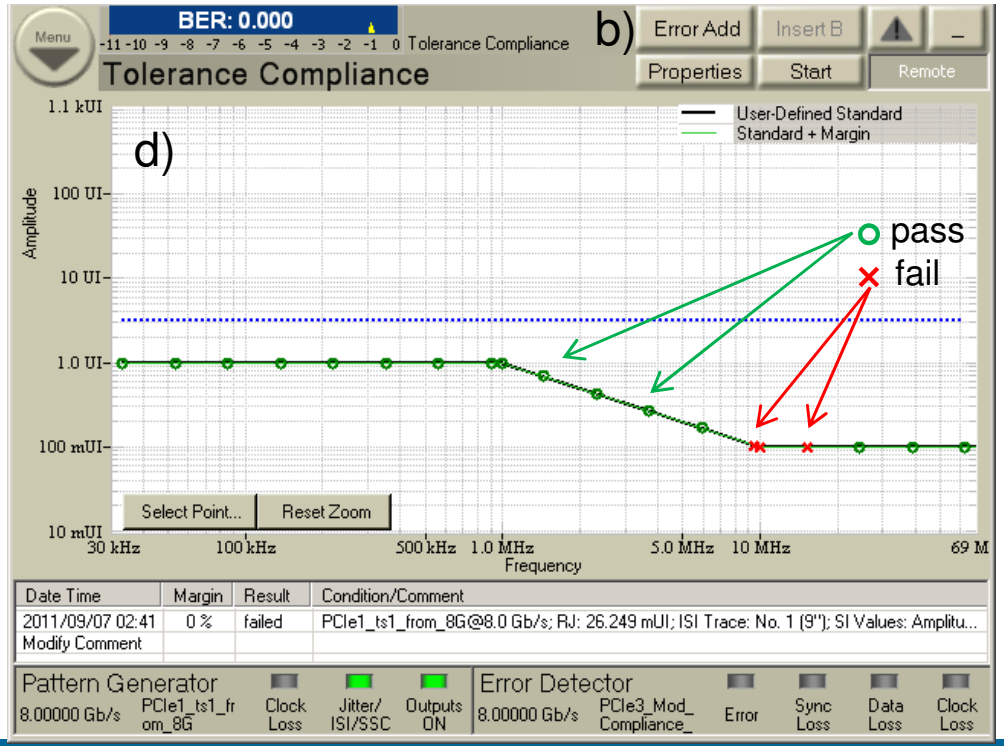
result panel

PJ2 Background Sweep and Jitter Tolerance Compliance Measurement



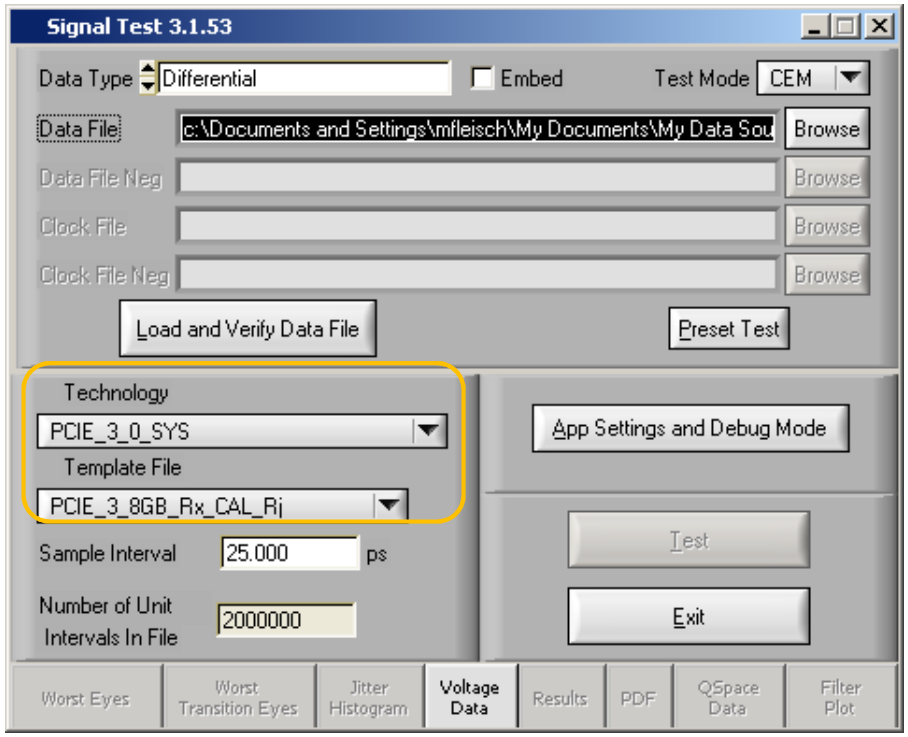
jitter set-up page showing PJ2

jitter tolerance compliance measurement reporting BER pass-fail result for every step

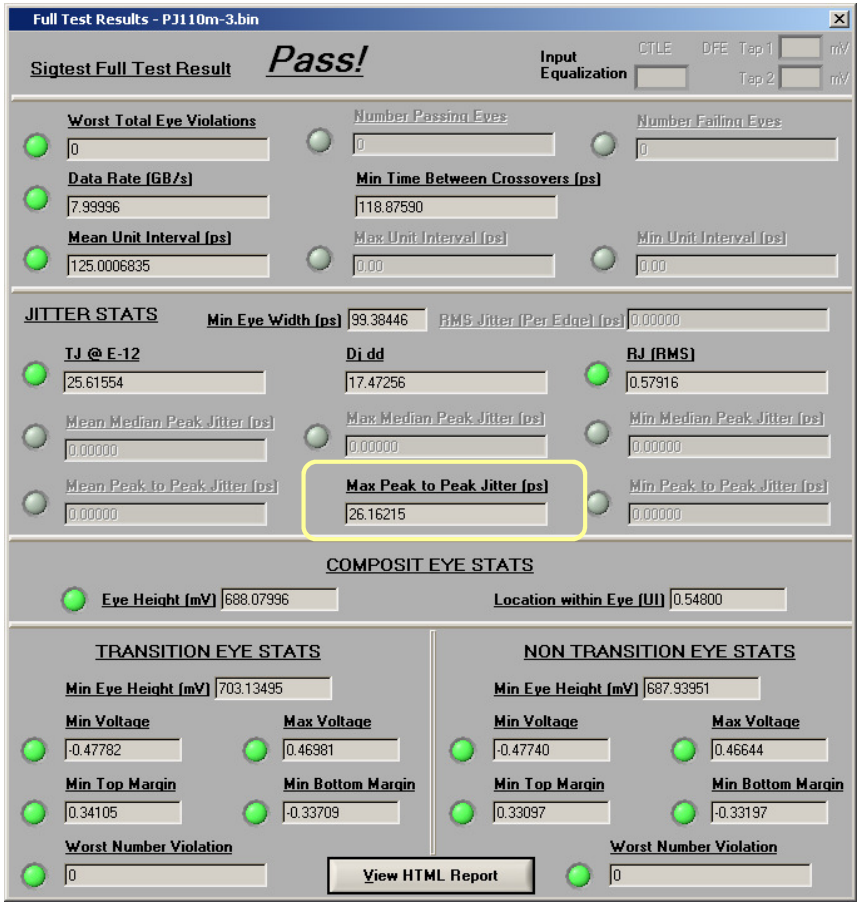


SigTest SW
Used for Calibration of Jitter Components, SJ

- At first the intrinsic jitter (for PJ=0) is measured for reference
- in this case (not shown) TJ_0 = 12.4 ps was determined
- increase PJ until max pp-jitter ranges from 24.9 to 26.9 ps



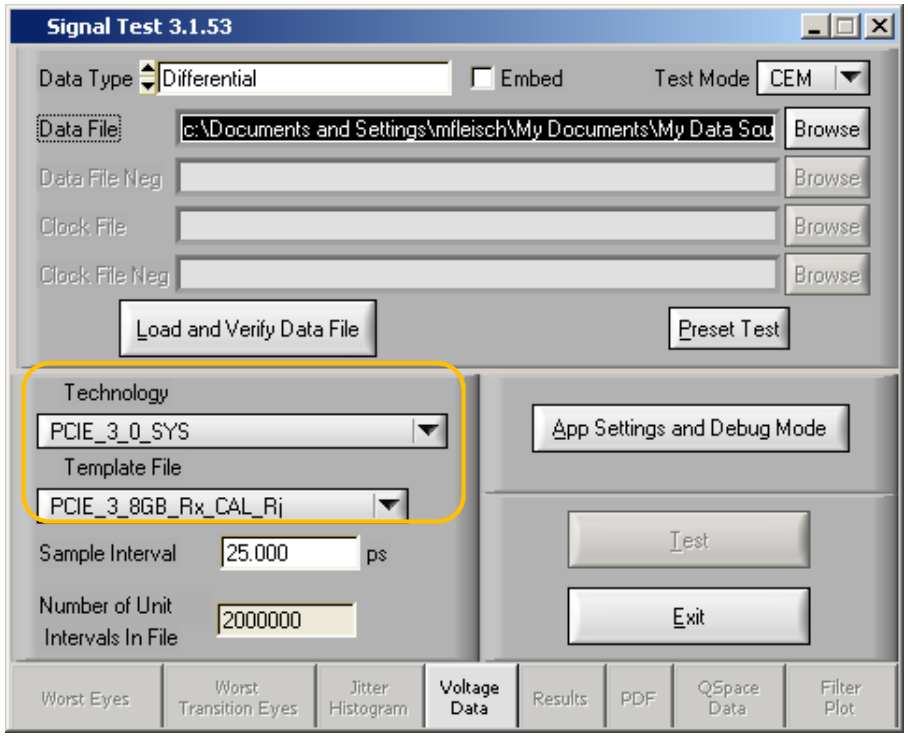
input panel



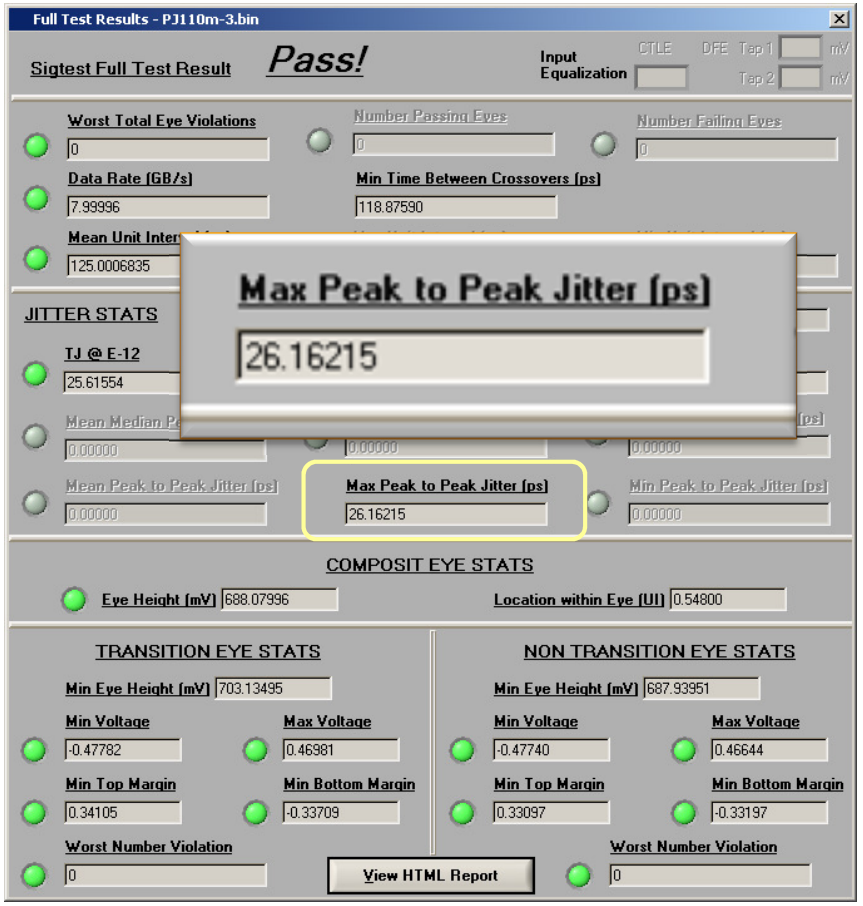
result panel

SigTest SW
Used for Calibration of Jitter Components, SJ

- At first the intrinsic jitter (for PJ=0) is measured for reference
- in this case (not shown) TJ_0 = 12.4 ps was determined
- increase PJ until max pp-jitter ranges from 24.9 to 26.9 ps

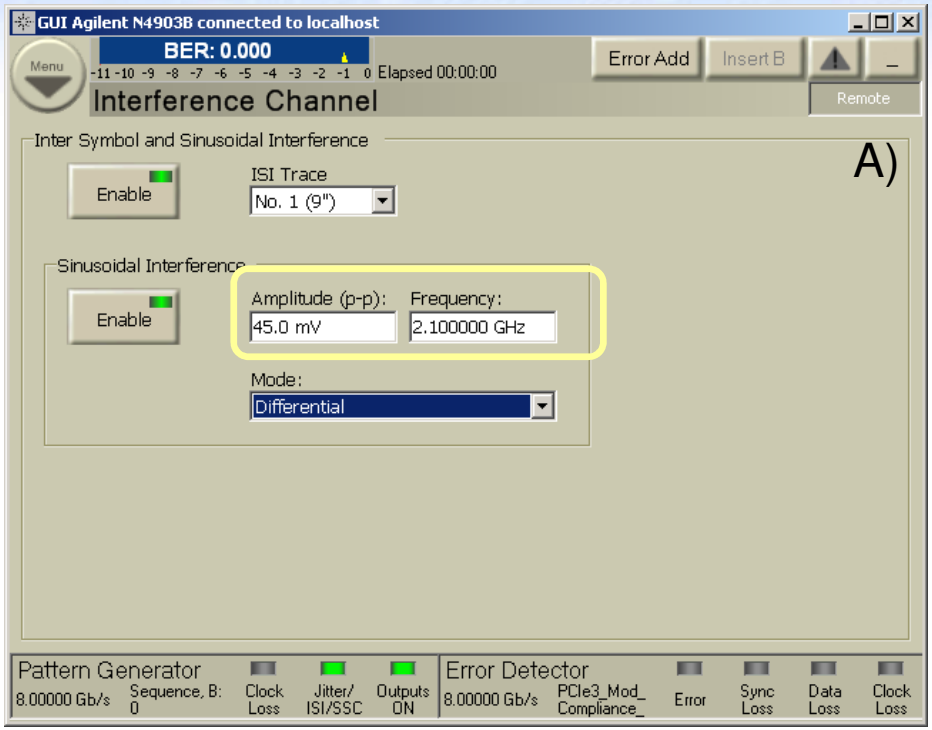


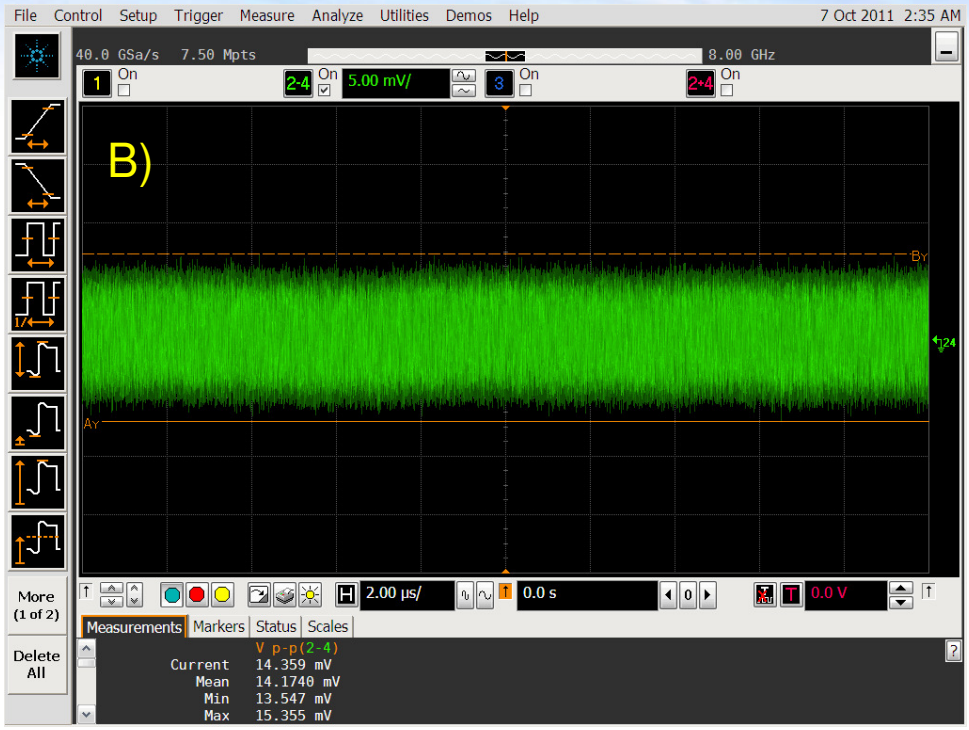
input panel



result panel

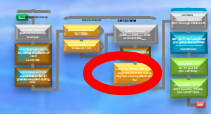
Differential Mode Sinusoidal Interference (DM-SI)





- BERT-PG generates a „Pause“-pattern (with 0mV amplitude)
- J-BERT Interfernce Channel is set to generate a 2.1GHz differential mode sinusoid
- DM-SI is calibrated behind the channel (Vp-p measurement)

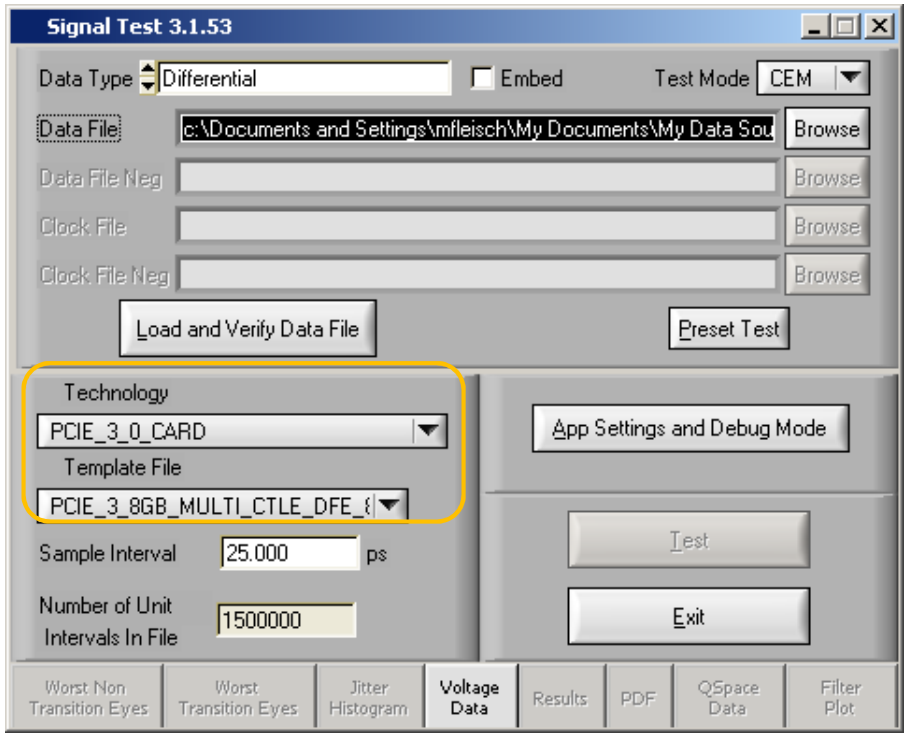
Final Adjust Procedure for EH and EW



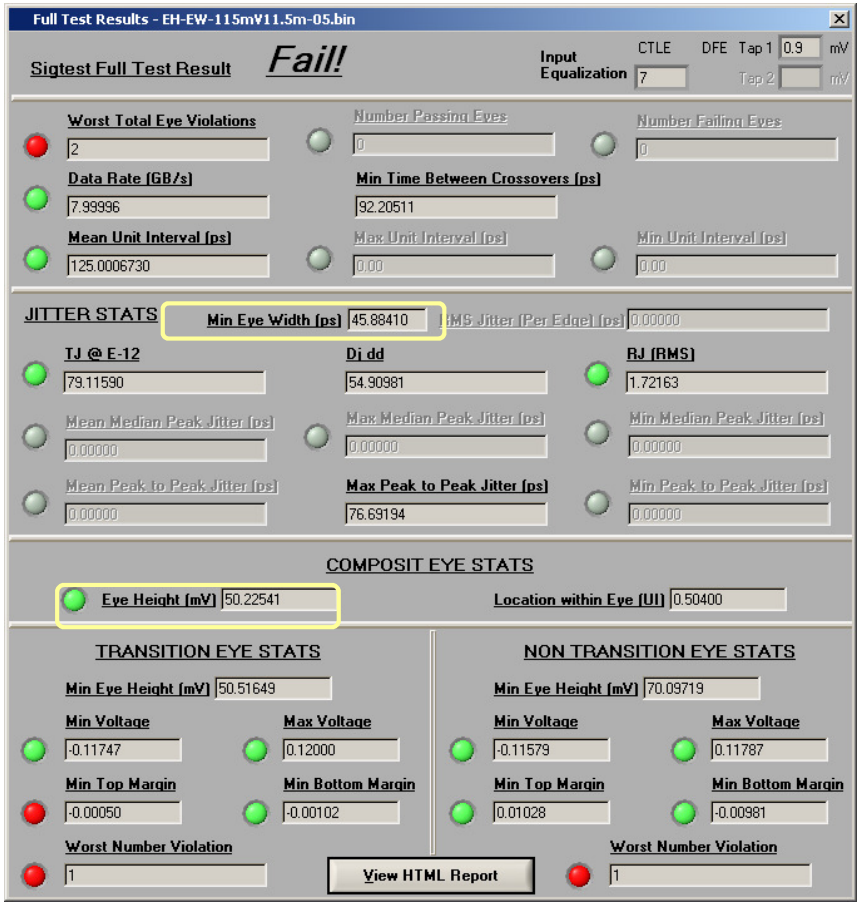
- Set up J-BERT to generate compliance pattern with P7 activated
- Each of the following steps consists of a sequence of:
  1. set the parameter on J-BERT
  2. capture the waveform on the oscilloscope
  3. load waveform into SigTest
  4. determine eye opening parameters using SigTest
- Adjust DM-SI to meet specified EH
- Adjust RJ to meet specified EW
- Re-check EH and if necessary re-adjust DM-SI once
- Record the final calibration values RJ_{cal} and $DM\text{-}SI_{cal}$ for later usage

SigTest SW
Used for Calibration of Stressed Eye, EH and EW

- Waveform (compliance pattern) with all impairments “on” is captured
- Different “technology” and “template” is chosen
- DM-SI and RJ varied until target values EH=50mV and EW=45ps achieved

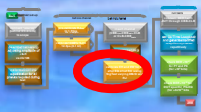


input panel



result panel

Typical Values on J-BERT Achieving a Calibrated Stress Signal

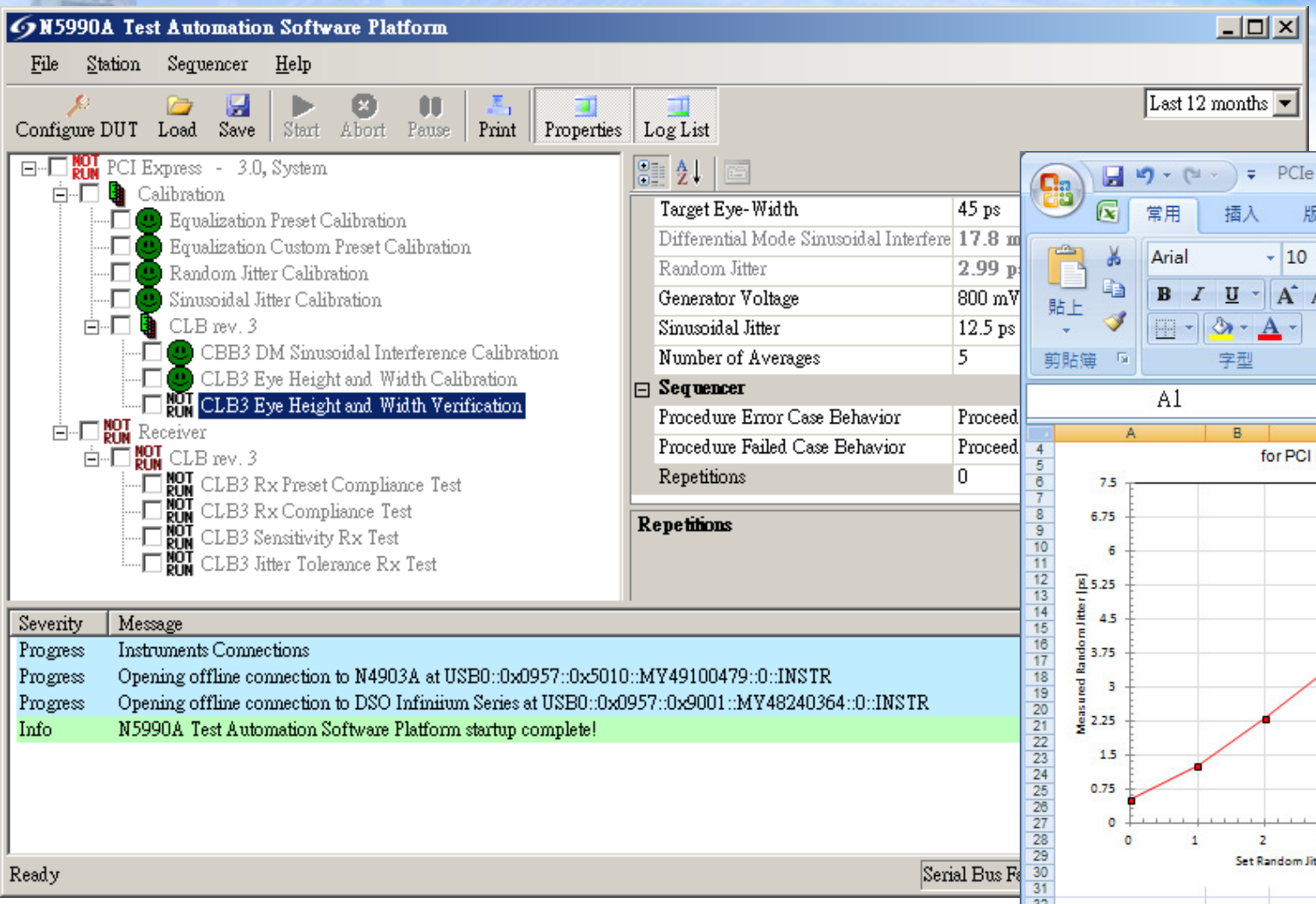


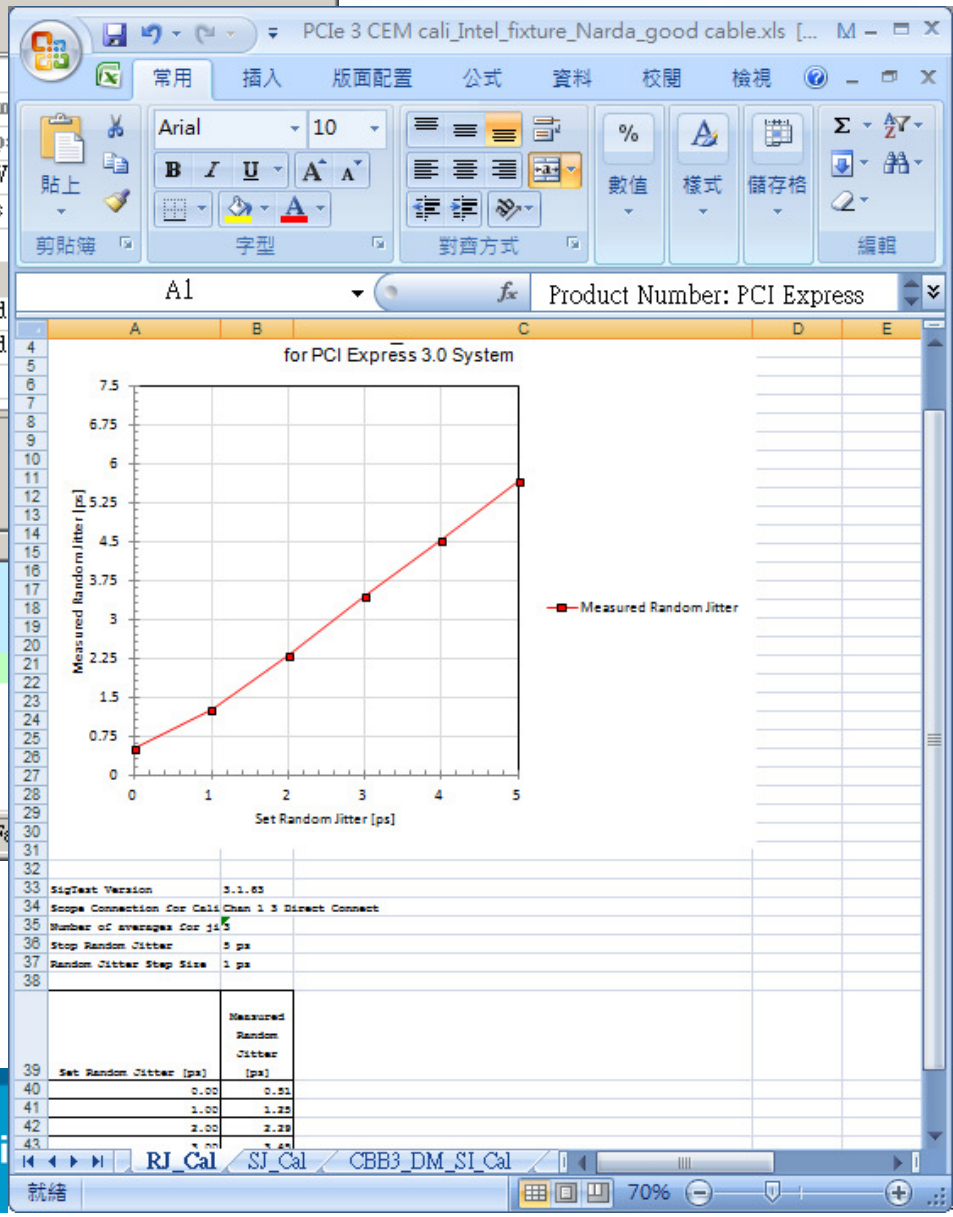
	de-embed	P8	P7
Vampt / mV	604	604	604
Pre-Curs / dB	0	4.1	4.1
Post-Cur1 / dB	-0.7	-4.5	-7.1

	pre-adjust	final adjust (EW/ EH)
RJ / mUI (ps) RMS	11.5 (1.44)	11.5 (1.44)
PJ2 / mUI (ps)	110 (13.8)	110 (13.8)
DM-SI /mV	45	110

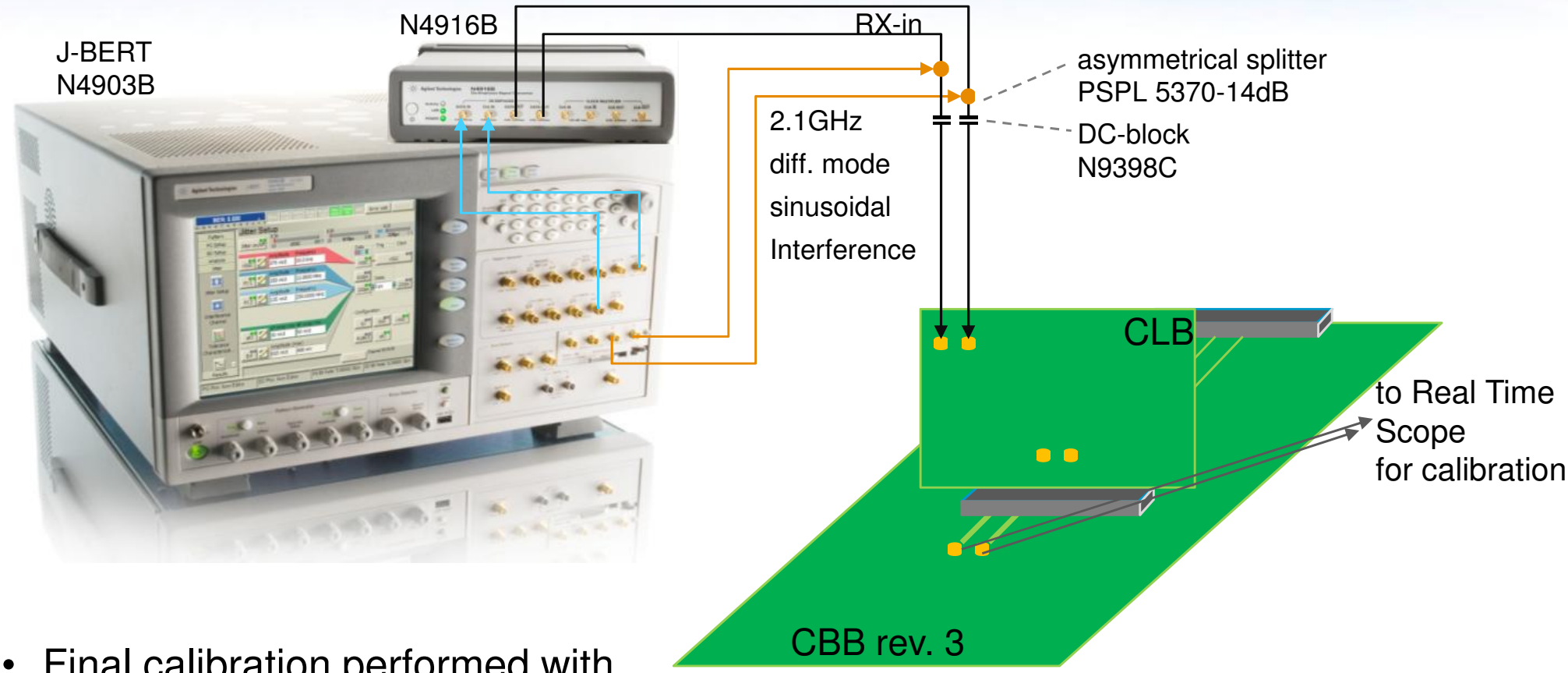
actual values may differ because they depend on parameters of individual units in use, as well instrumentation, accessories or SIG-boards

N5990 Automation SW



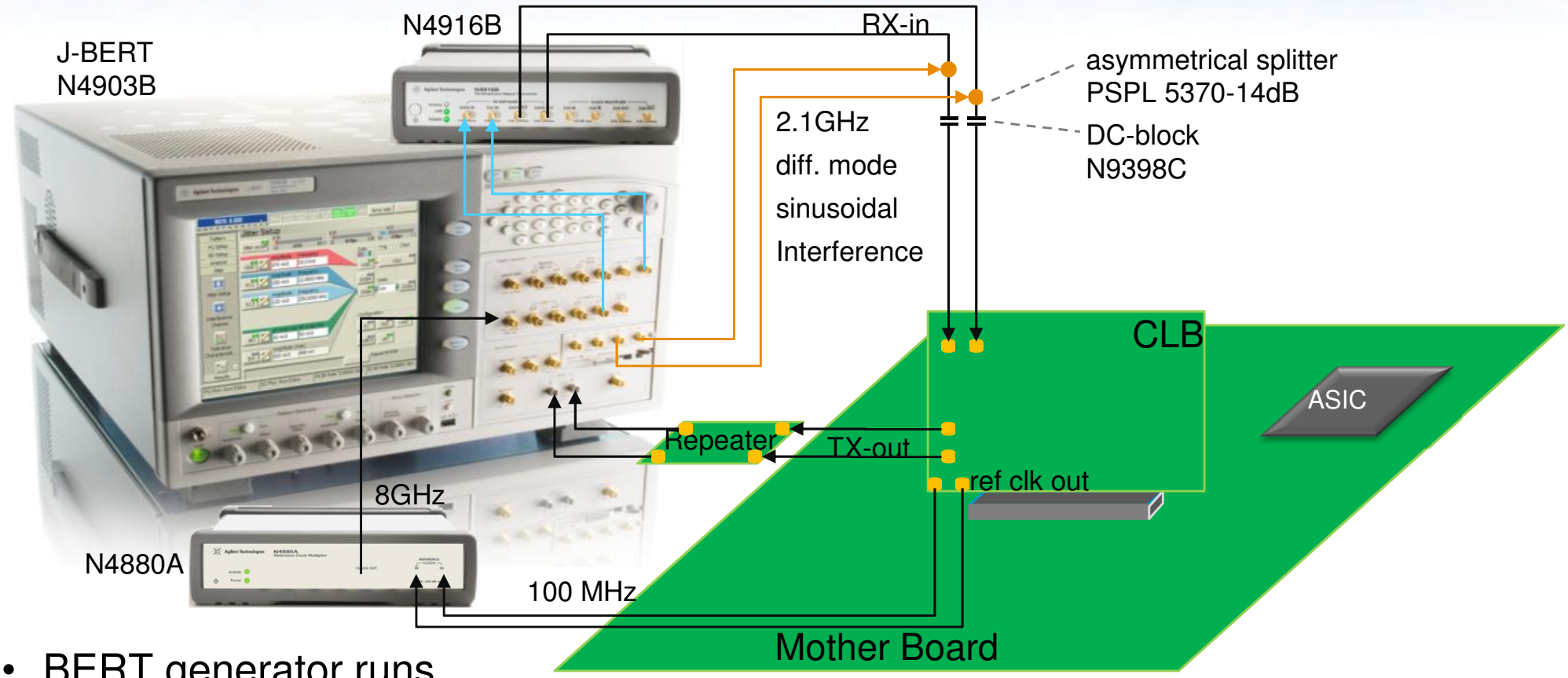


Set-Up for Mother Boards (Calibration) According to CEM Specification Rev. 3.0



- Final calibration performed with PCIe3 compliance pattern and all impairments turned on
- SigTest SW calculates EW and EH

Set-Up for Mother Boards (Test) According to CEM Specification Rev. 3.0



- BERT generator runs on mother board ref clock
- N4880A Reference Clock Multiplying operates according to PCIe specs

How to Set the DUT into Loopback

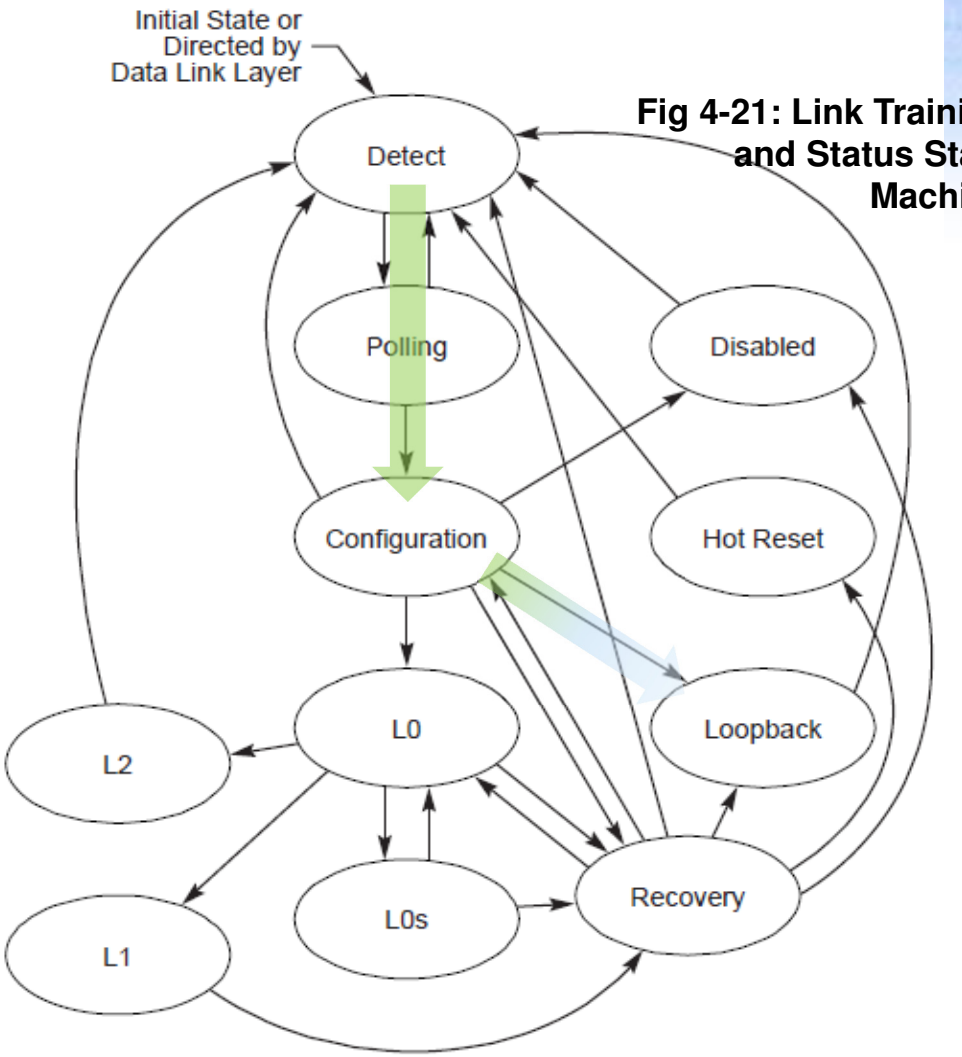
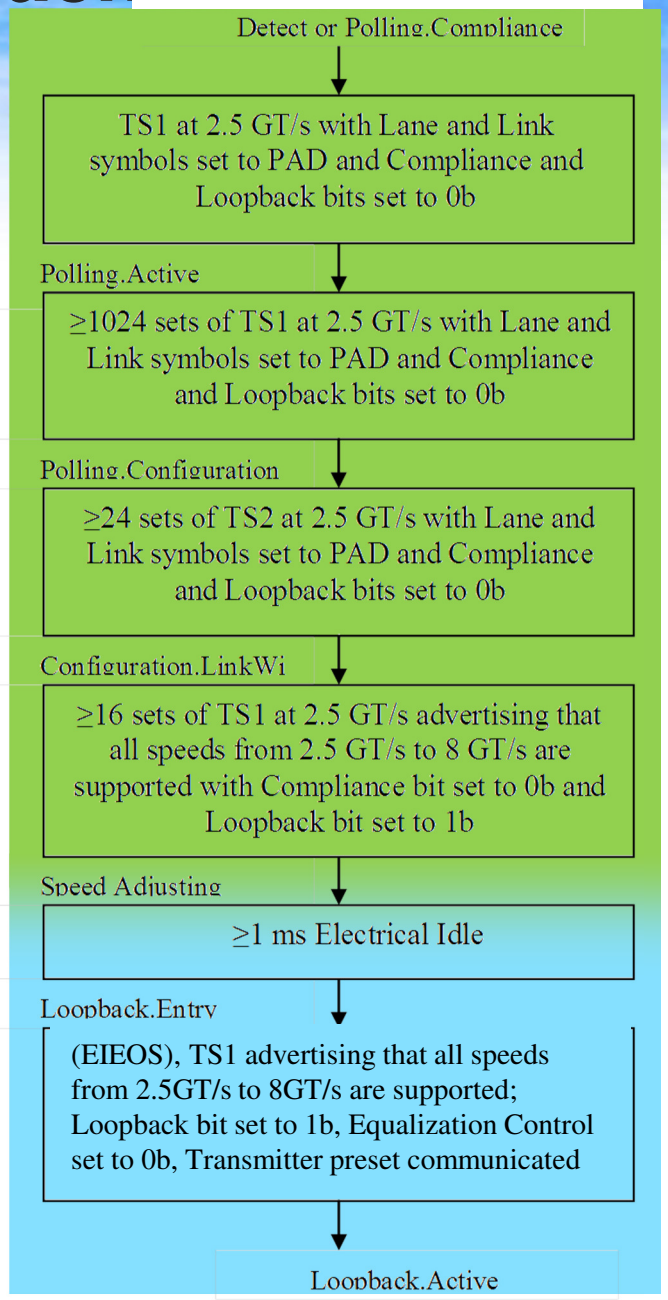


Fig 4-21: Link Training and Status State Machine



- Same procedure as for PCIe 1 and 2 until speed adjustment only that 8GT/s is advertised
- Loopback entry not yet defined in rev.3 Test Spec →

Conclusions

1. De-embedding Cables alone can increase eye height up to 20%.

2. RX Calibration is the biggest challenge of PCIe 3.0 Testing

3. PCIe 3.0 Presets can yield open eyes in the presence of a PCIe 3.0 Compliant Channel, especially after only CTLE equalization

4. Calibration of the stressed eye for receiver test should minimize effect of instrument noise. BASE Spec since it must be calibrated to 10E-12 BER.

5. AIC TX Testing must convolve reference Channel in addition to Reference Package model losses.