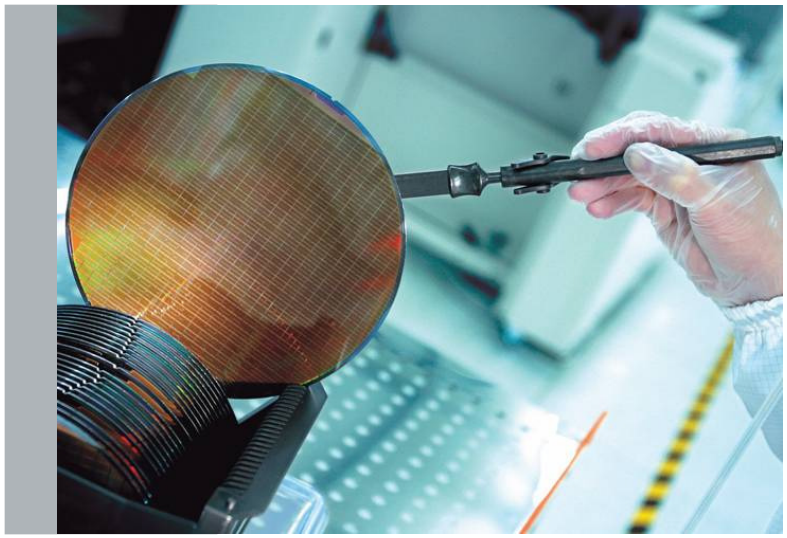
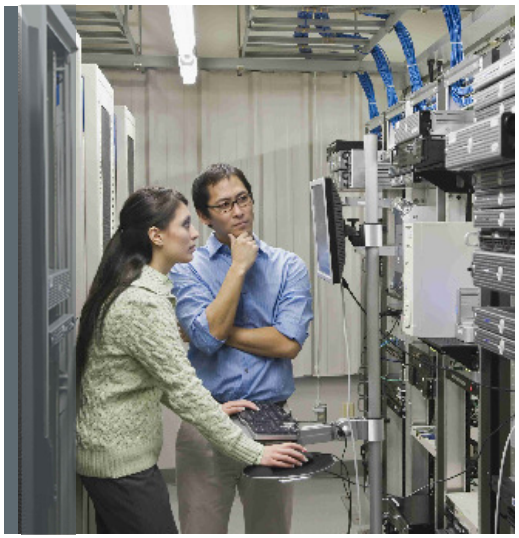
# PCI Express 3 Receiver Testing Using the Tektronix BERTScope

Jacky Huang-AE, Tek Taiwan





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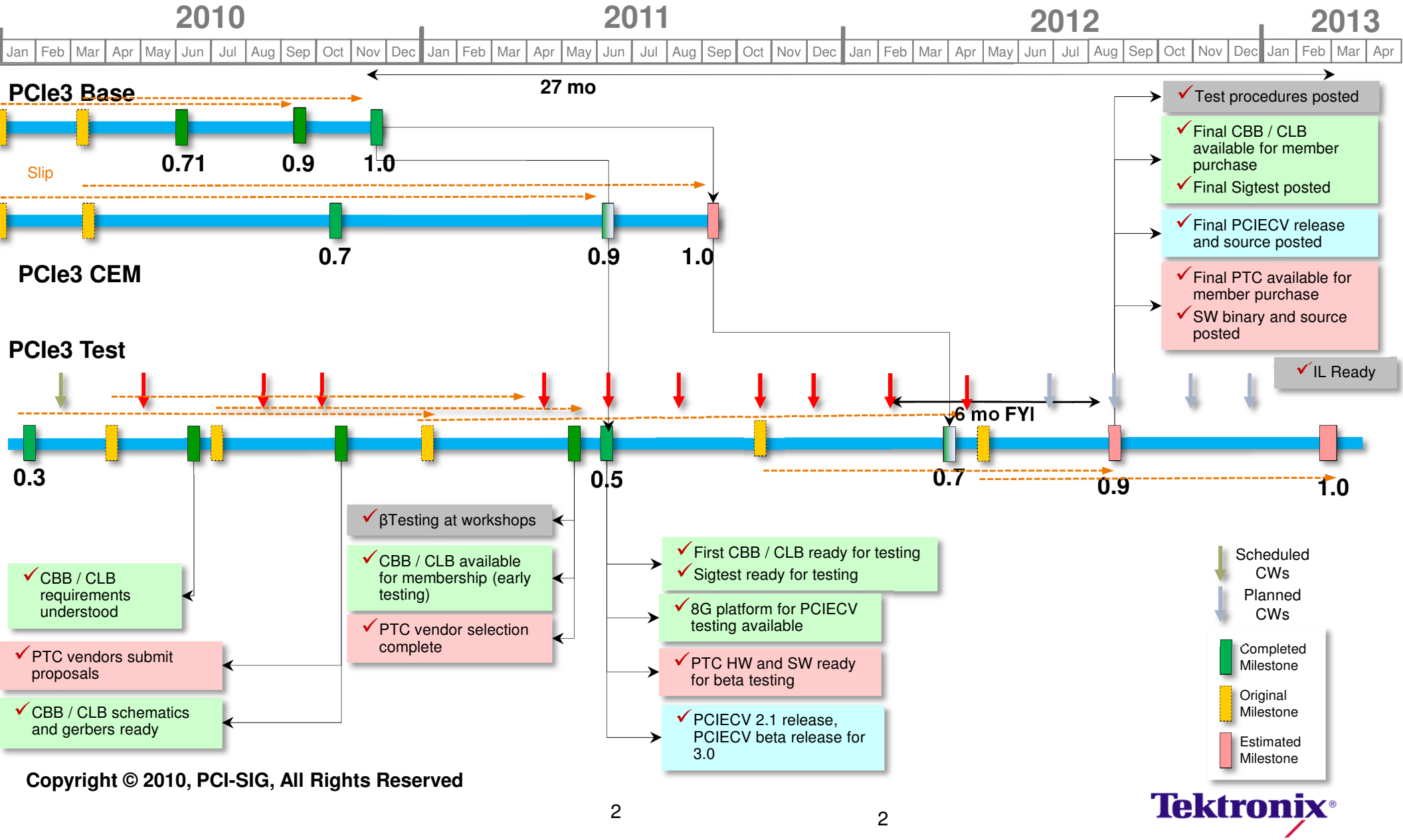
# PCIe 3.0 Timeline as of June 2012

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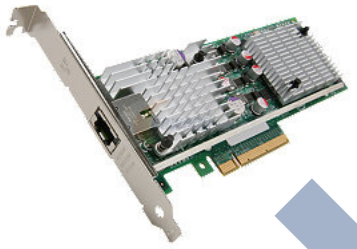
# Which PCIe3 Specification Applies? Plus Embedded PCIe 3.0

**PCI Express®**
**Base Specification**
**Revision 3.0**

November 10, 2010

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**PCI Express® Architecture**
**PHY Test Specification**
**Revision 3.0**

*July 18, 2012*

PCI EXPRESS



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# Base Specification vs. CEM Test Philosophies

- CEM Testing is primarily focused on Compliance
  - Ensure Interoperability of Systems (Hosts) and Add-In Cards (Endpoints)
  - Pass/Fail
  - Margin Testing mainly to verify manufacturability

- Base Specification Testing is generally focused on Characterization
  - Verify chip performance across a wide range of operating conditions
    - Voltage, Temperature, Eye Height, Eye Width, Equalization, etc.
  - Margining is Key
    - Increase OEM's latitude in choice of backplane material and PCB layout


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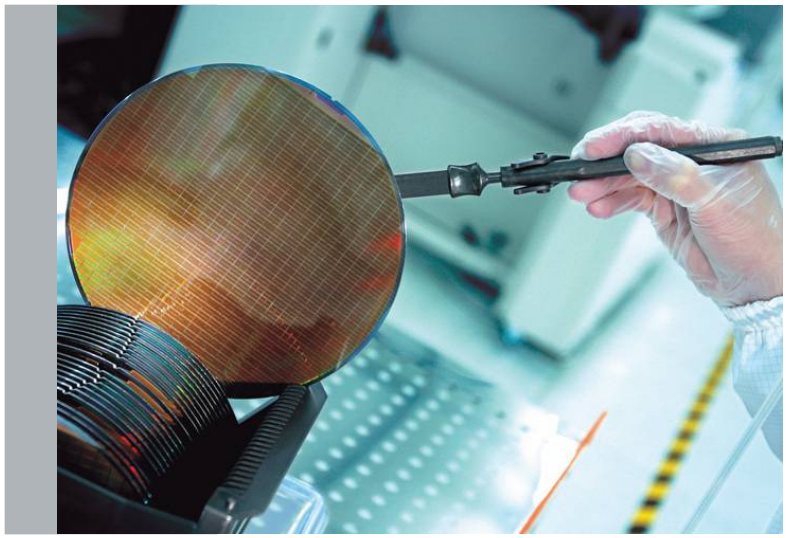
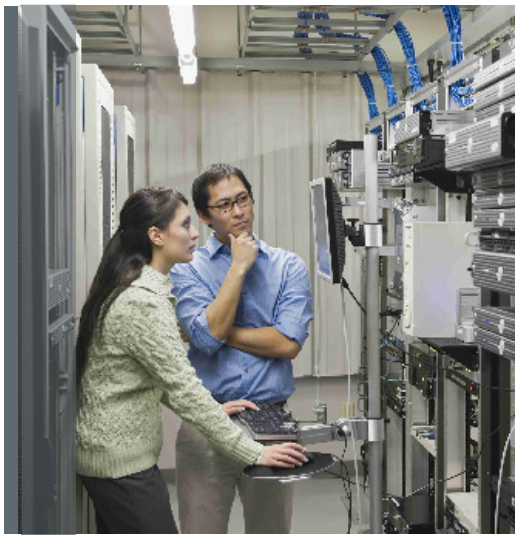
# PCIe 3.0 Rx Solutions





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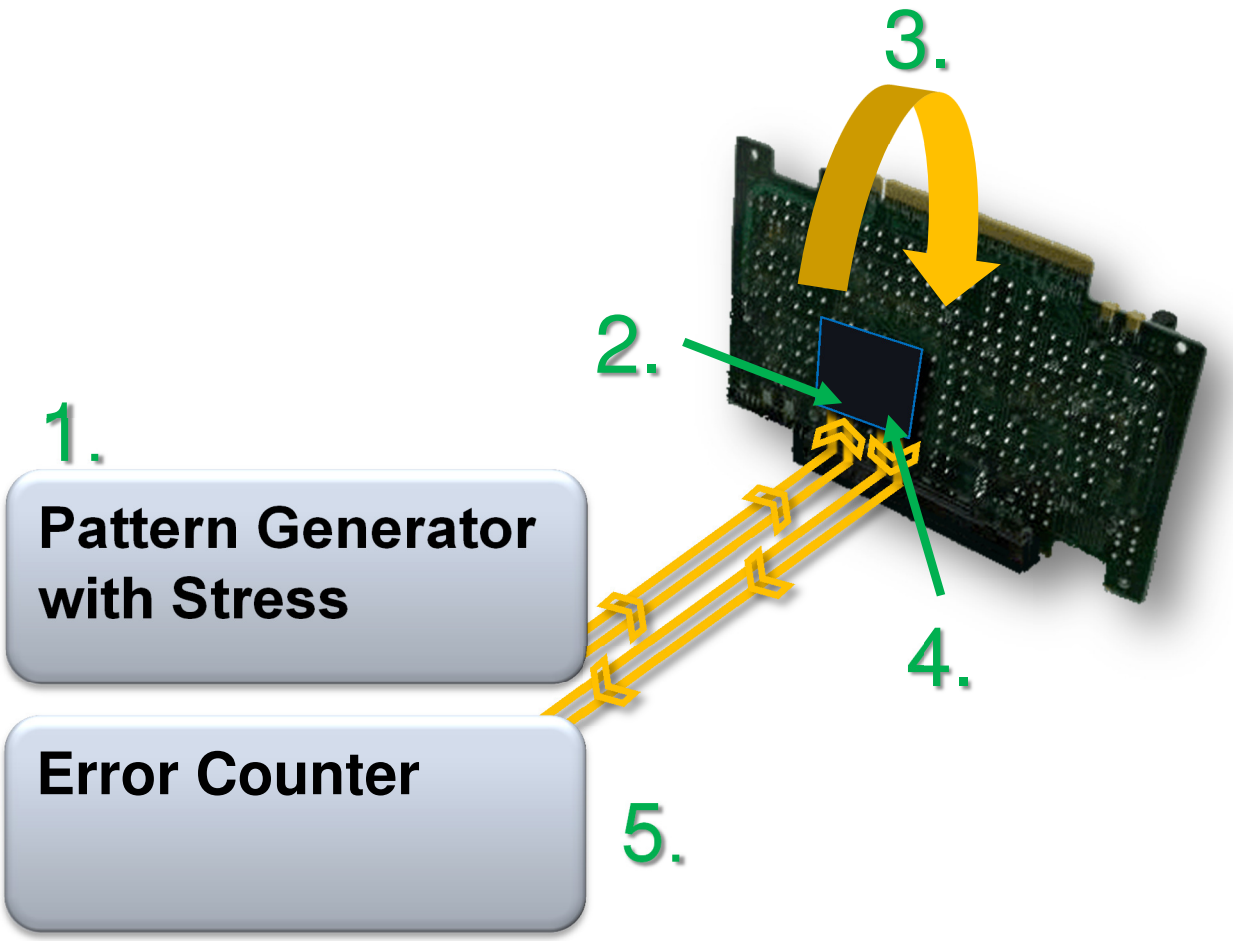
# Basic Receiver Testing




At the simplest level, receiver testing is composed of:

1. Send impaired signal to the receiver under test
2. The receiver decides whether the incoming bits are a one or a zero
3. The chip loops back the bit stream to the transmitter
4. The transmitter sends out exactly the bits it received
5. An error counter compares the bits to the expected signal and looks for mistakes (errors)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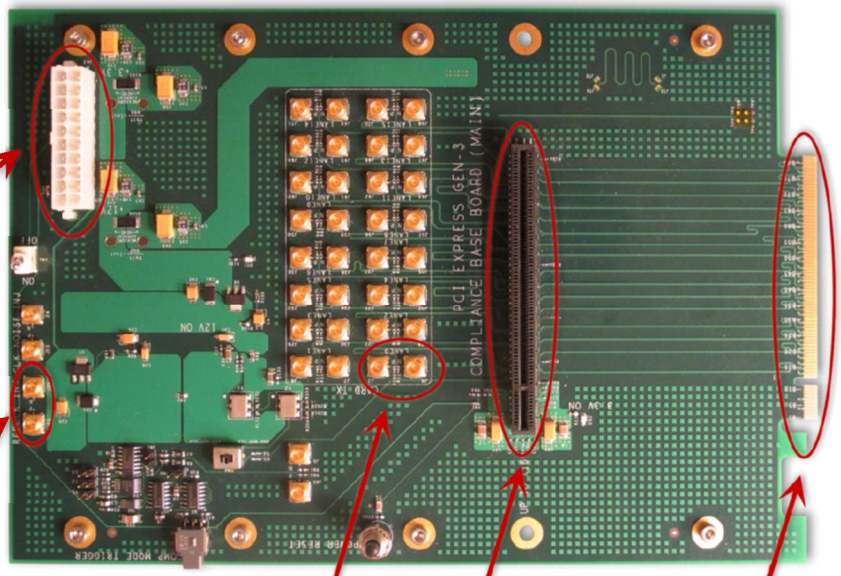
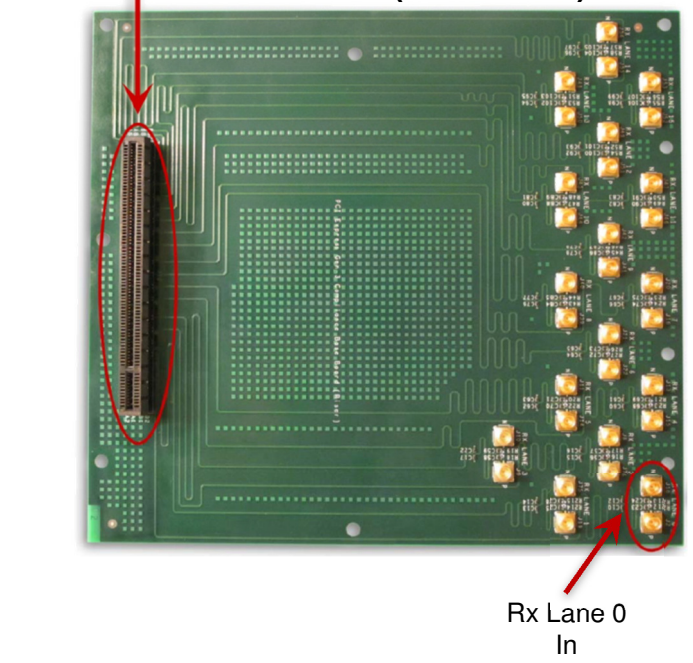
# PCIe 3 CEM Test Fixtures

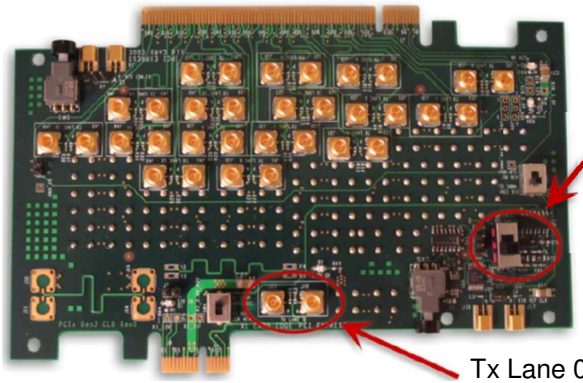
## Compliance Base Board (CBB)




## Compliance Base Board Riser Card (CBB Riser)




## Compliance Load Board (CLB)





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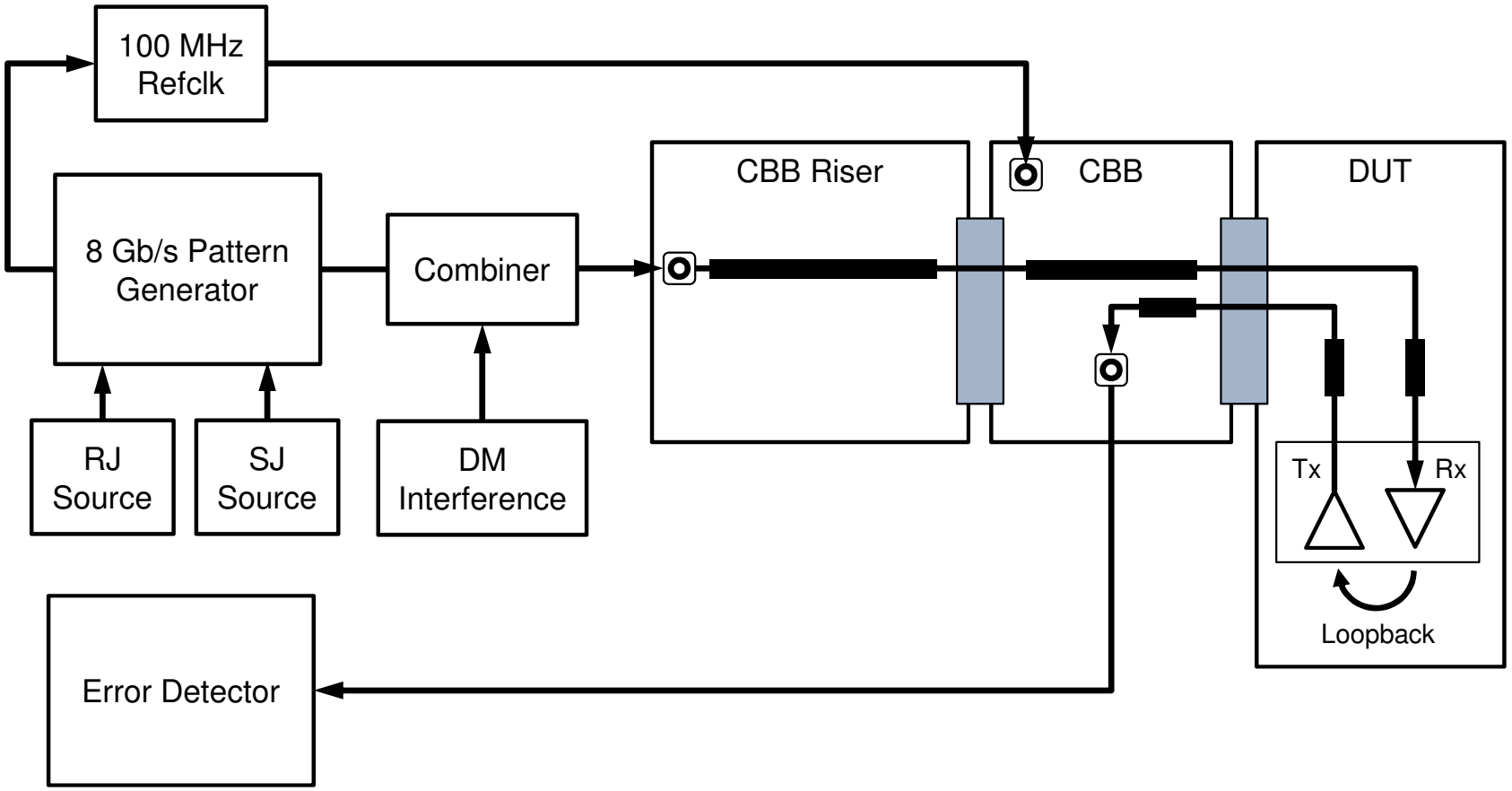
# PCIe 3 CEM/Add-In Card Receiver Test





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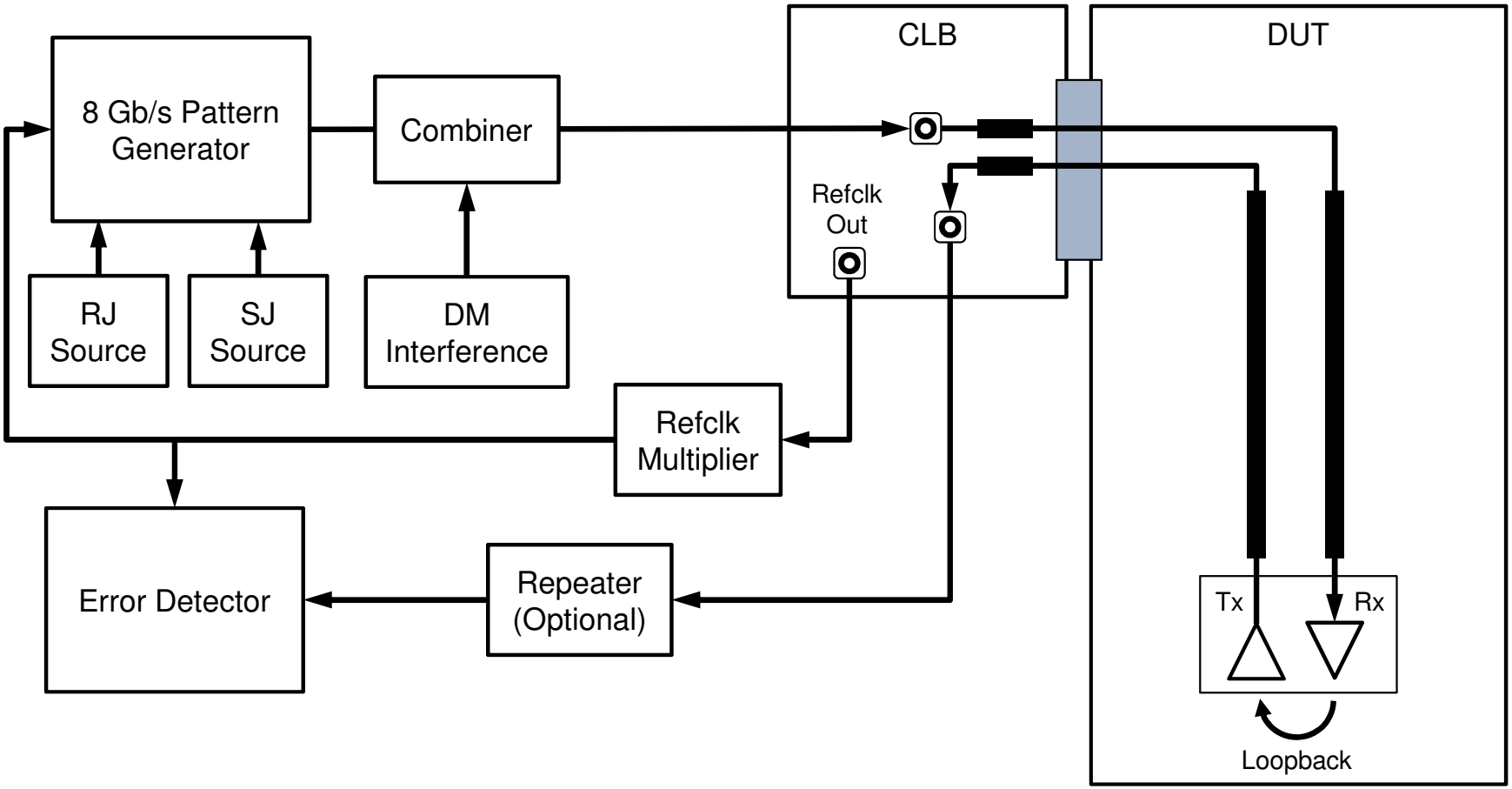
# PCIe 3 CEM/System Receiver Test





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# Tektronix Receiver Test Solution

- BERTScope
  - Stressed Pattern Generator and Error Detector
  - Various models cover 2.5, 5, 8, and 16 GT/s
- DPP125
  - 3 or 4 tap pre-shoot and de-emphasis in accordance with PCIe Gen 3 requirements
- BERTScope CR125A
  - Flexible and compliant clock recovery
- DSA/DSO70000 Series Real-Time Oscilloscope
  - Bandwidths to 33 GHz
  - TX testing
  - RX Stressed Eye Calibration


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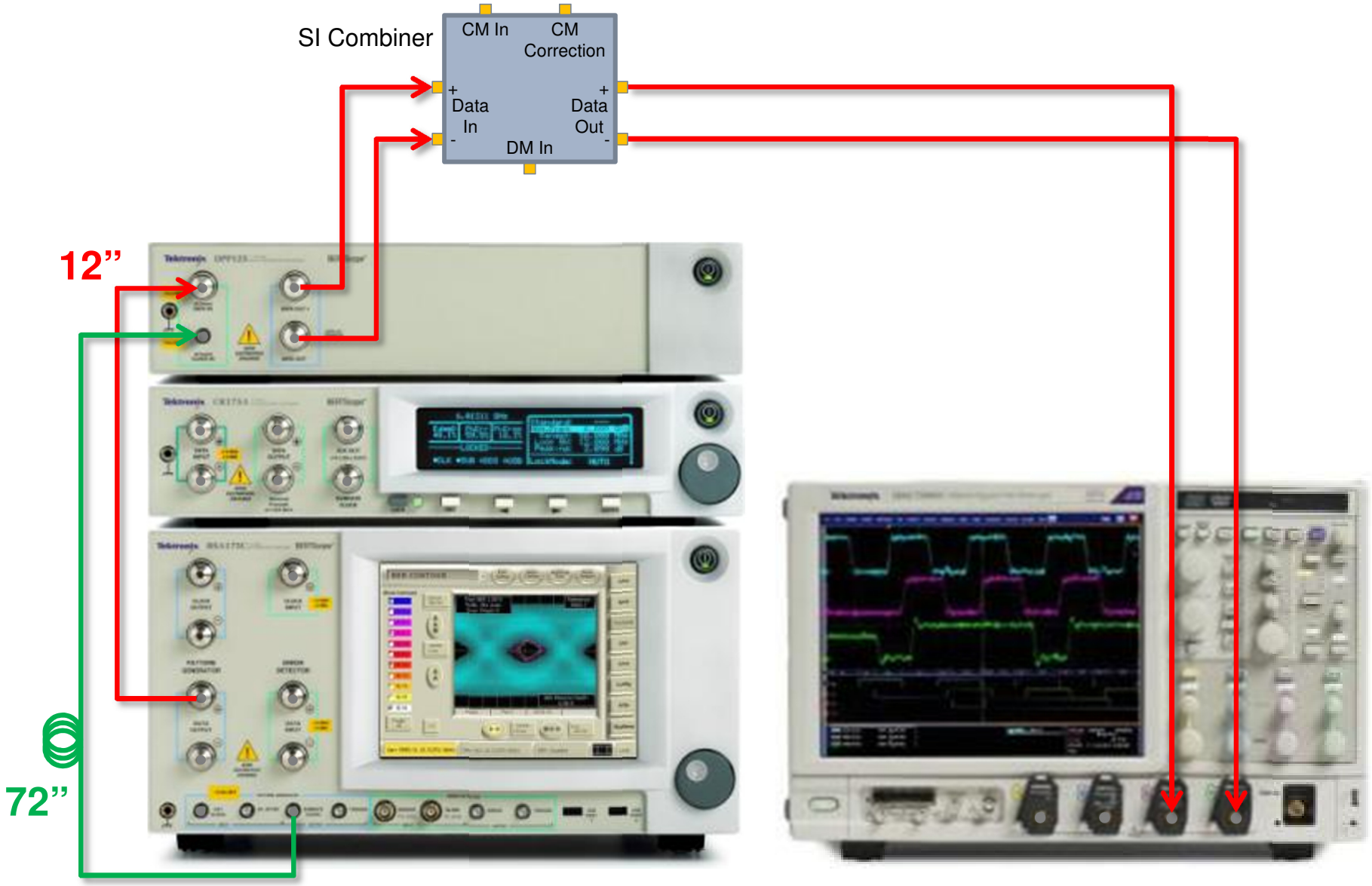
# Equipment Setup for Amplitude, Emphasis, SJ and RJ Calibration





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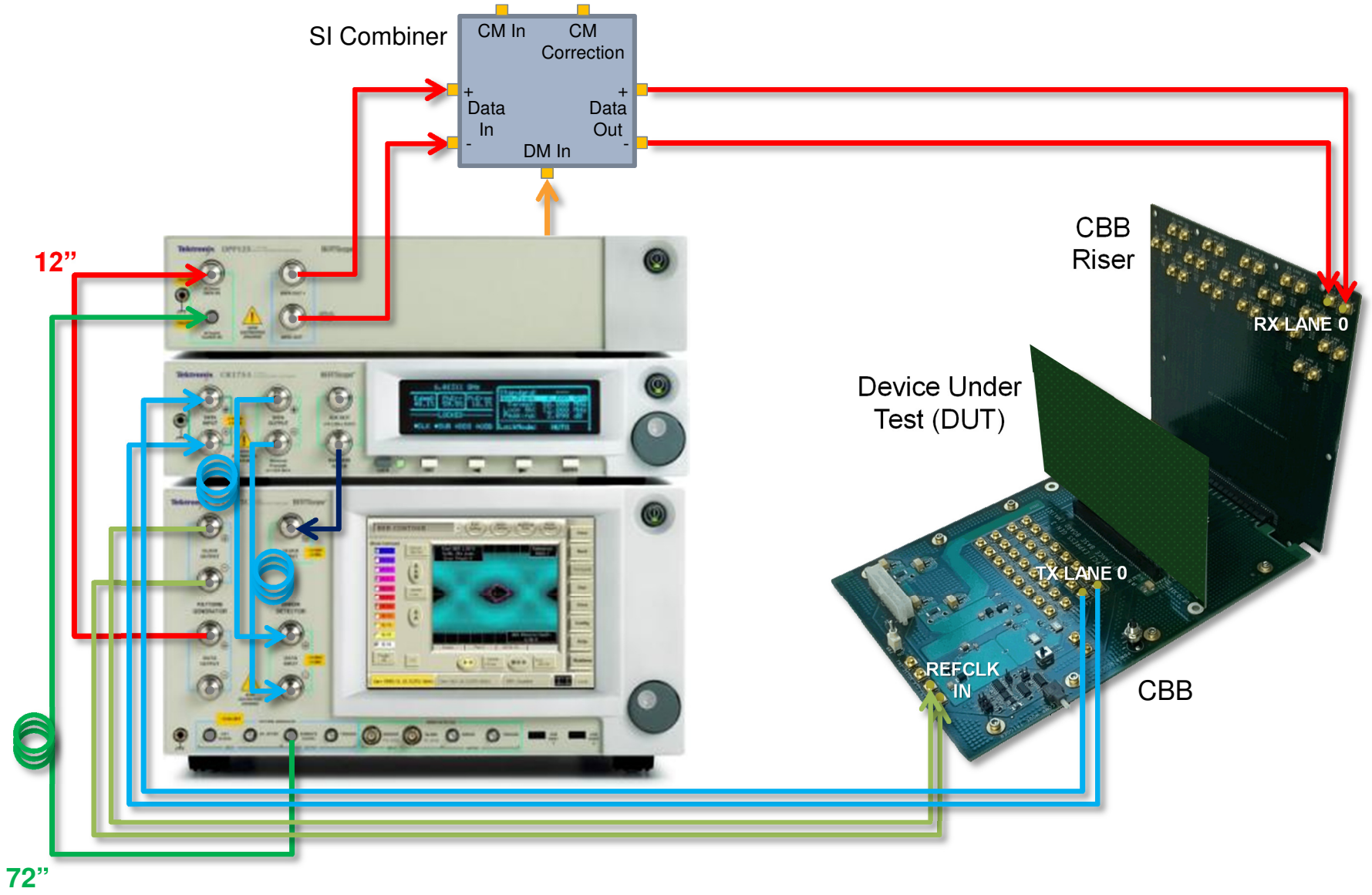
# Equipment Setup for CEM/Add-In Card Receiver Testing





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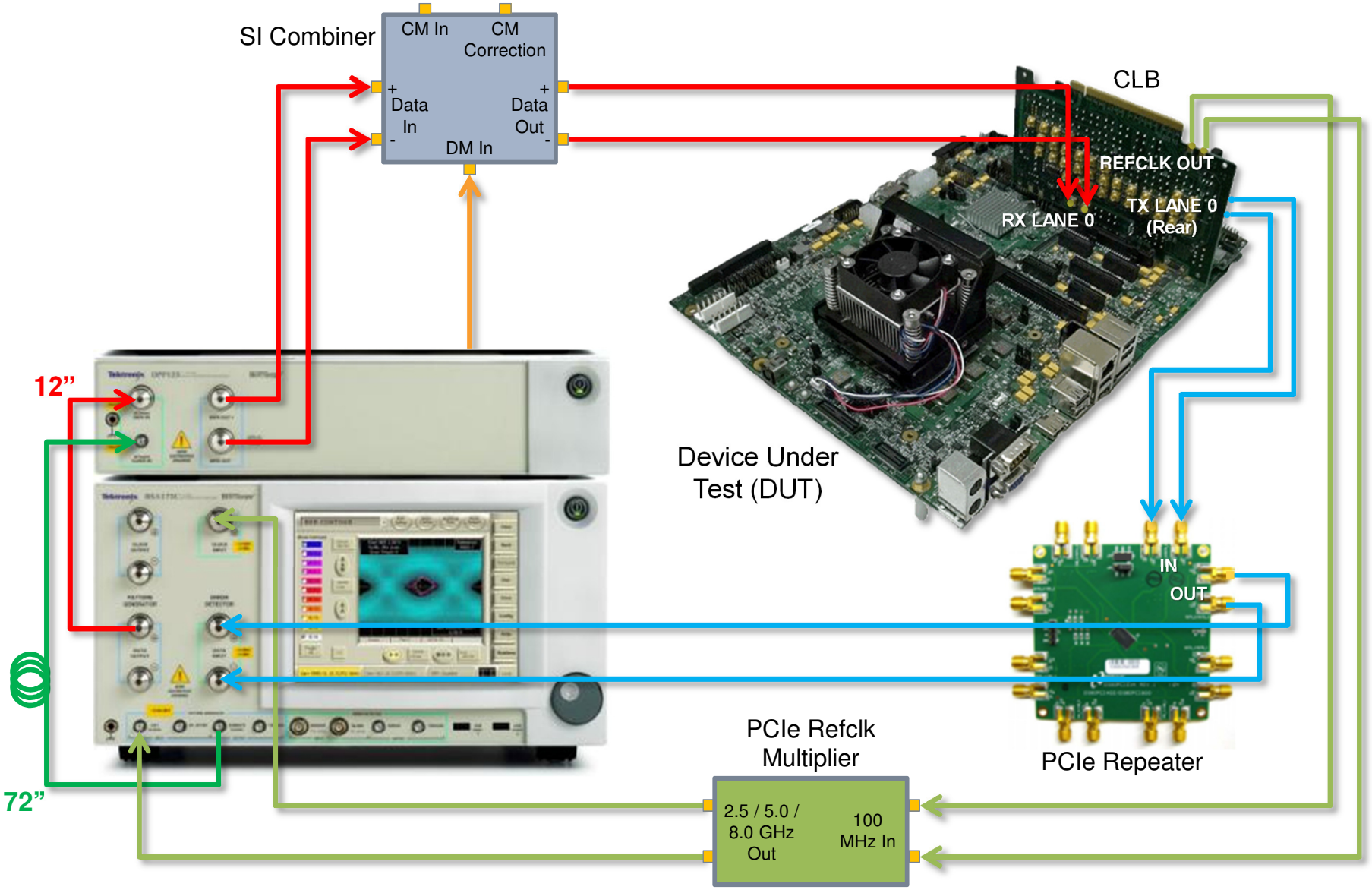
# Equipment Setup for CEM/System Receiver Testing





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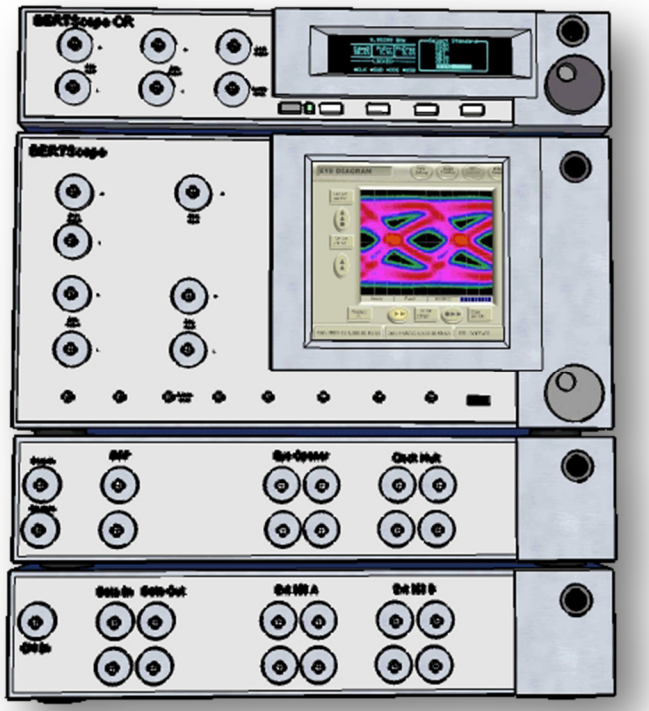
# NEW! -Components of the Receiver Test Solution

- BERTScope C Model
  - PG, stressed eye sources, ED
- **New! DPP125C Option ECM**
  - **Eye opener, Clock doubler/Multiplier**
- **New! BSAITS125**
  - **CM/DM interference**
  - **ISI for Gen2 & Gen3**
  - **Option EXP for variable ISI**
- **New! CR125A Opt PCIE8G**
  - **PLL analysis for Gen1/2/3**
- **New! BSAPCI3 SW**
  - **Auto calibration, Link training, and test**
- Cables, adapters, compliance boards
- DSA/DPO/MSO70K Series Real-Time Oscilloscope
  - Stressed Eye Calibration





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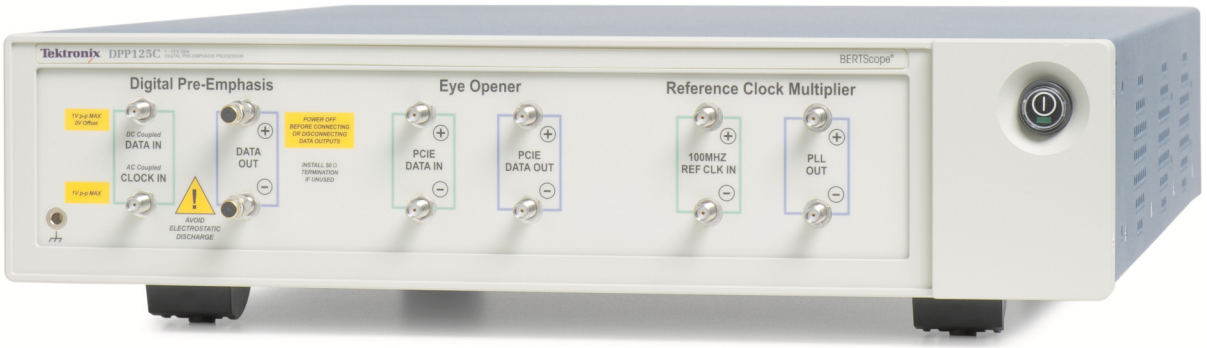
# New! DPP125C with Option ECM

- **Integrated reference clock multiplication to PCIe compliant 2.5 GHz, 5 GHz, and 8 GHz.**
- **Integrated eye opener functionality for testing DUTs with long channels.**
- **New microcontroller to provide more processing power.**
- **RS-232 interface enhancement to speed-up PCIe receiver equalization link training.**
- **SW to accommodate channel de-embedding and ISI fine adjustments.**



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# New! BSAITS125 Interference Test Set

- **Programmable, variable ISI for automated testing and precision setting**
- **Built-in compliant PCIe2 and PCIe3 Medium and Long ISI channels**
- **Integrated PCIe3 CM and DM interference combiner**
- **Integrated PCIe3 Base Spec CM interference calibration**
- **Continuously Variable, Expanded ISI for automated testing of multiple standards with Option EXP**




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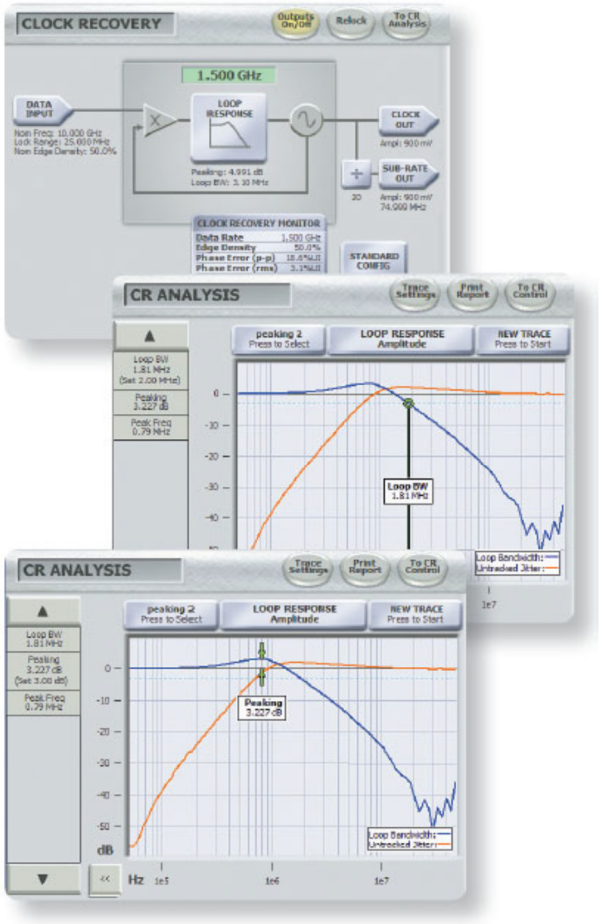
# New! CR125A Opt PCIE8G

- **PLL Loop BW Analysis for Gen1/2/3**
- **Uses CR125A and Test SW**
  - **Similar to Gen1/2 PLL Loop BW solution**

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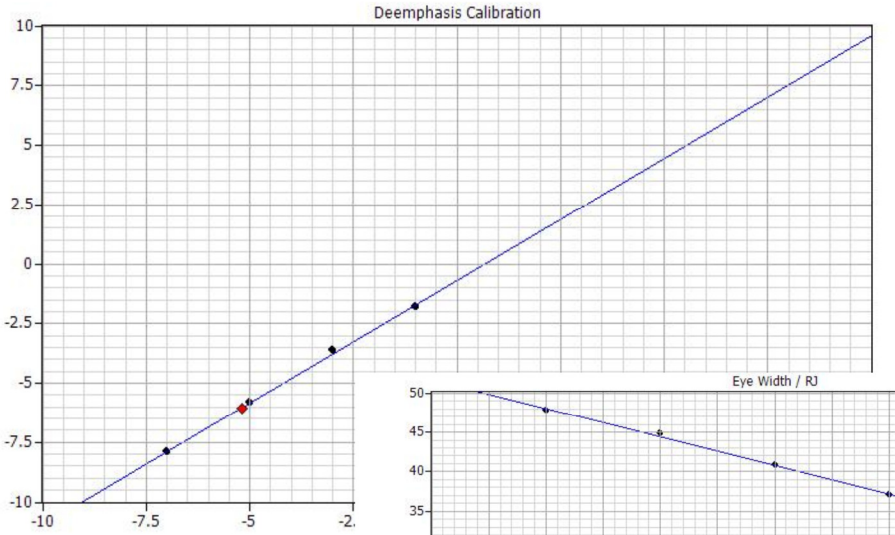
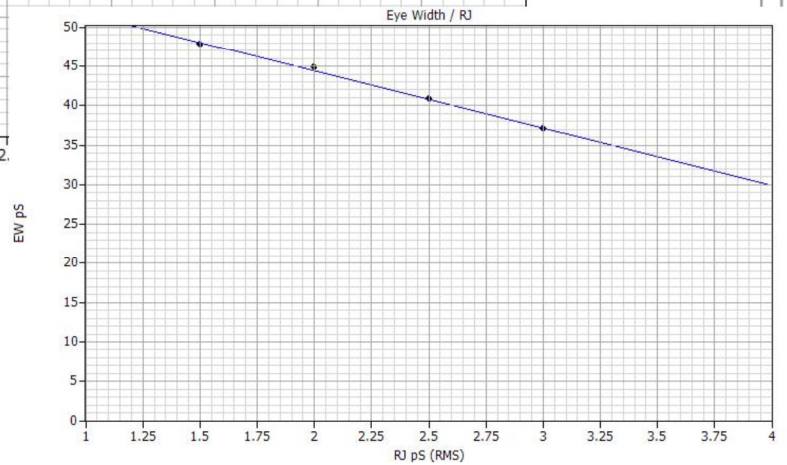
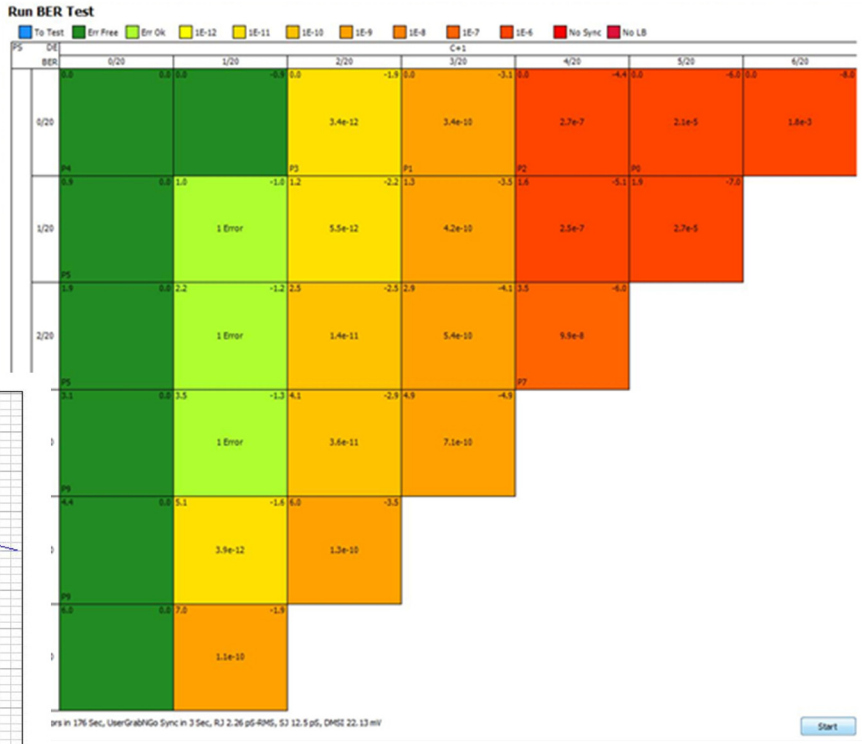
# New! BSAPCI3 PCIe 3.0 Automation SW

- **Automated calibration, link training, loopback initiation, and testing.**
- **BER Map feature for TxEQ optimization.**
- **Reduces the time and minimizes the skill-set required to perform the calibration and testing.**
- **Increases the reliability and accuracy by removing inconsistencies with manual calibration.**

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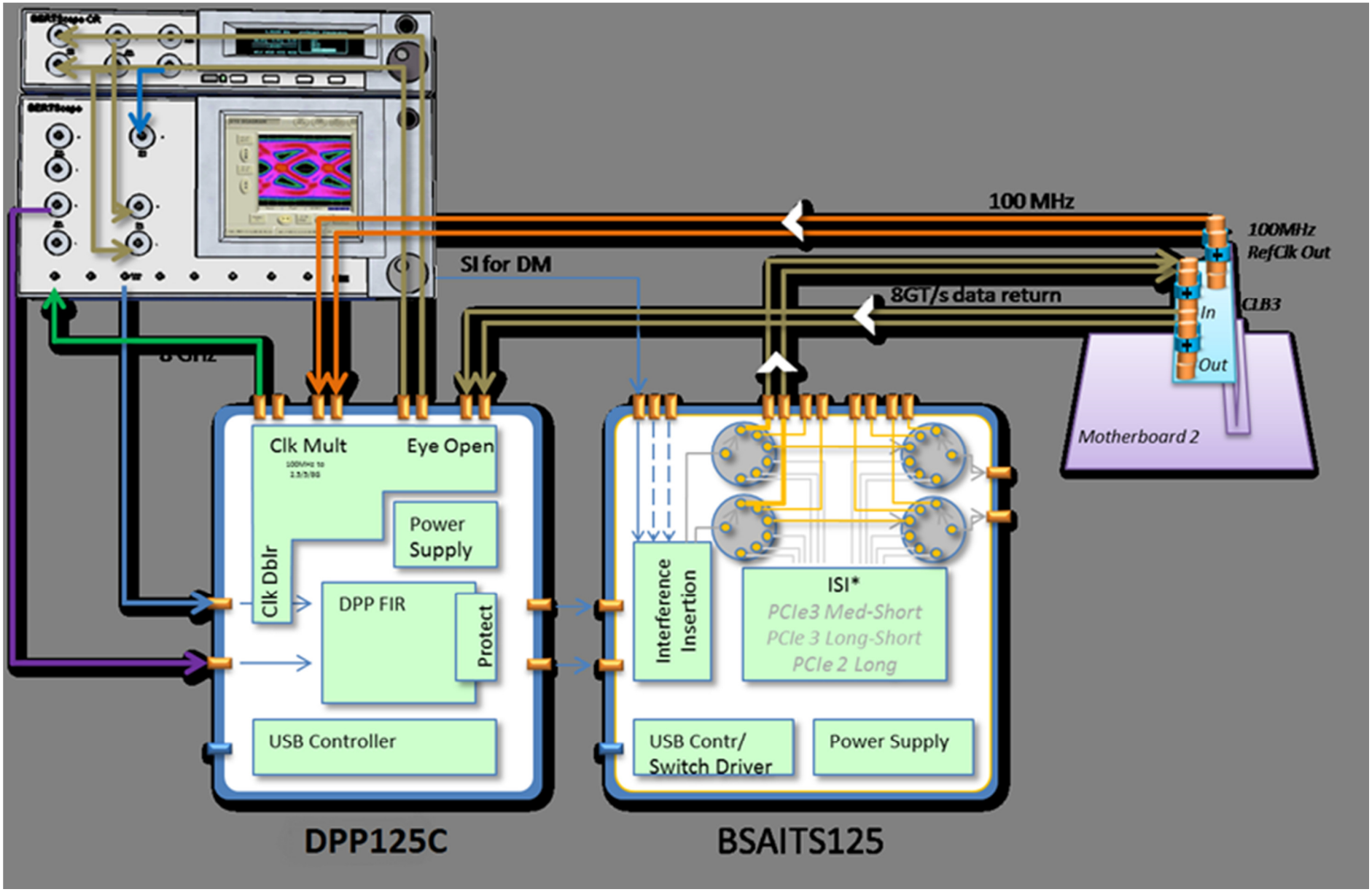
# Typical Test Configuration



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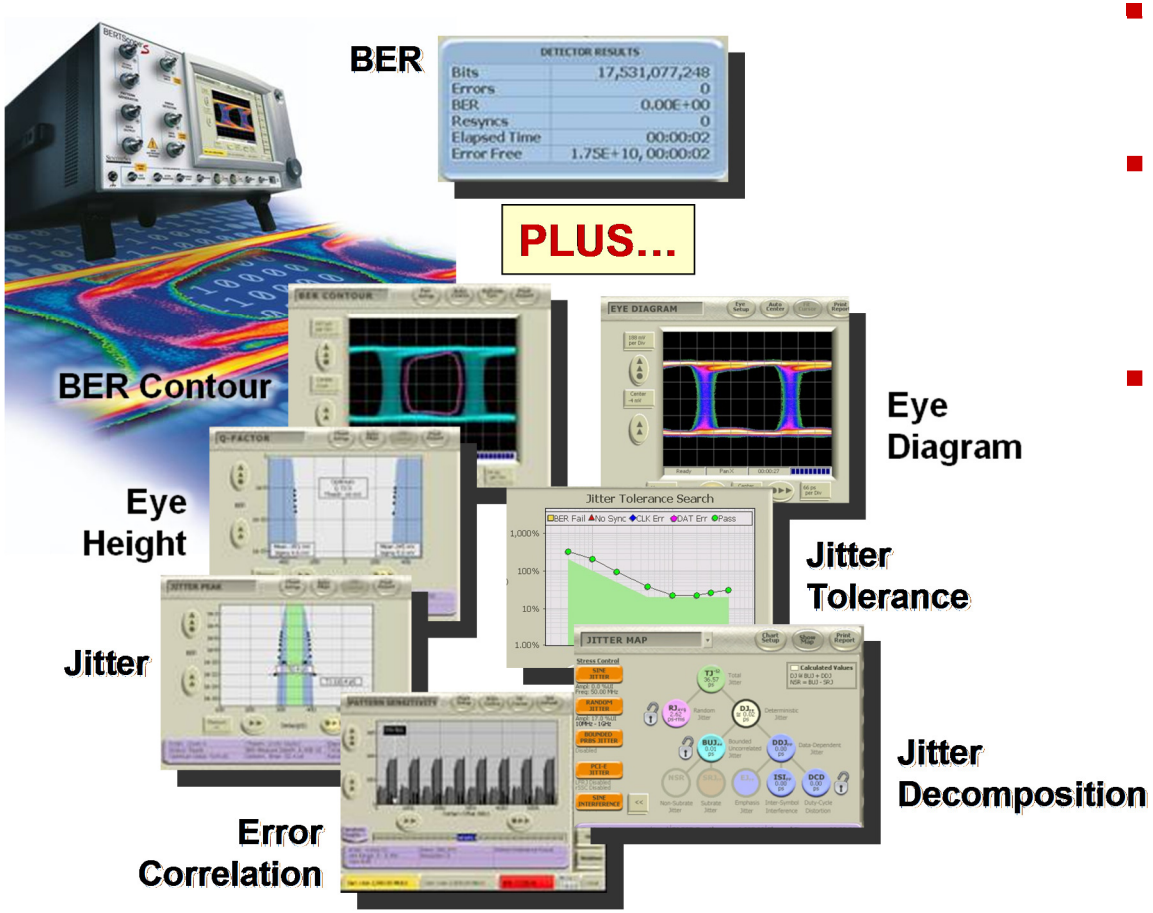
# Beyond Compliance: BERTScope Analysis Tools

- Besides being a BERT, the BERTScope's **"Scope" functionality** brings benefits that complement those of the Tektronix scopes
- **Analysis tools are full featured and easy to use**




- Frees up the scope for other tasks
- **Eye diagram for quick diagnosis** of synchronization and BER failure issues
- **Debug** challenging **signal integrity problems**
  - **Error Location Analysis**
  - **Pattern Capture**
  - **Jitter Map**
  - **BER Contour**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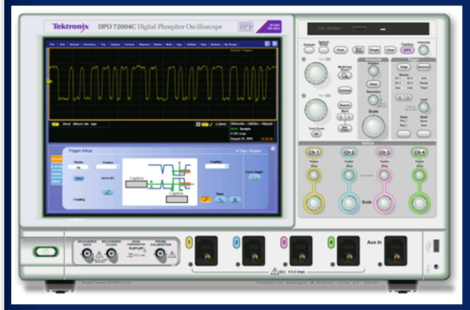
# Comprehensive PCI Express Solution

## Transmitter



## Receiver

## Protocol

Component Level Testing
System Level Debug
HW/SW Integration
Characterization
Compliance



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# Thank You!

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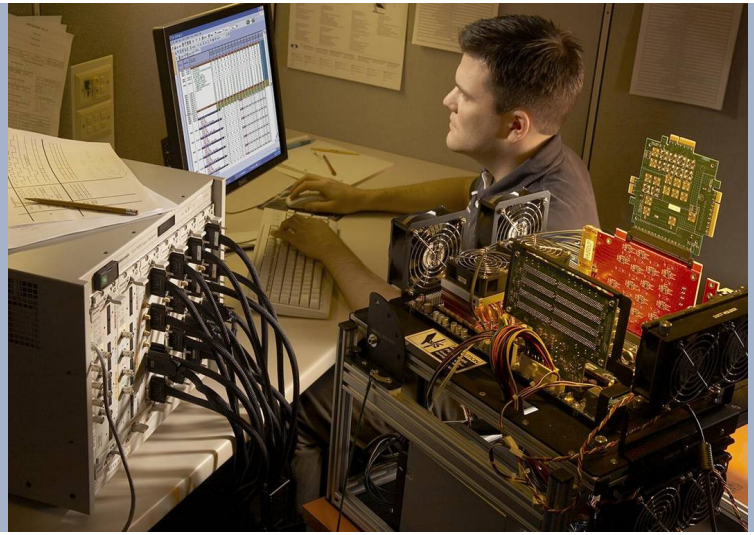

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