USB 3.1 ENGINEERING CHANGE NOTICE

Title: USB 3.1 LTM
Applied to: USB_3_1r1.0_07_31_2013

Brief description of the functional proposed:

The USB 3.1 Specification changes in this ECN are intended to facilitate use of Latency Tolerance Messaging (LTM) to achieve greater system power savings. This objective is already described in Appendix C.4 of the USB 3.1 Specification:

> "Computer systems typically maintain a high state of readiness to service devices even when the computer system is idle. LTM supports a mechanism for a system to reduce its state of readiness with the cooperation of Enhanced SuperSpeed devices. This may result in substantial system power savings without requiring additional cost to devices."

However, LTM as currently defined enables devices to advertise a BELT value less than tBELTdefault, which would generally increase system power consumption.

To facilitate use of LTM for greater system power savings, two USB 3.1 Specification changes are requested:

1. Tighter definition of the legal range of BELT values permitted in Latency Tolerance Message Device Notifications.
2. Elimination of the recommendation to disable LTM before suspending a device. The objective of this recommendation was to ensure that BELT is no less than tBELTdefault while the device is suspended, and thereby avoid wasting power. With LTM BELT constrained to values greater than tBELTdefault, disabling LTM is no longer necessary.

Benefits as a result of the changes:

1. Constraining BELT to values greater than or equal to tBELTdefault will give software implementers confidence that enabling LTM cannot increase power consumption.
2. Eliminating the requirement to disable LTM before suspending a device will reduce software complexity, which will further increase software vendors' confidence in implementing LTM support.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

The changes herein have no known impact on systems that currently conform to the USB specification. LTM has not been widely enabled, in part due to the concern about increased power consumption.

An analysis of the hardware implications:

The changes herein have no known impact to existing designs. Device designs must already accommodate tBELTdefault when LTM is not enabled by software.

An analysis of the software implications:

The changes herein should simplify software support, as software won't have to toggle LTM_Enable when suspending and resuming a device.

An analysis of the compliance testing implications:

Any compliance testing exposure to BELT should be changed to reflect the change in BELT range specified below.

Actual Change

(a) Section 8.5.6.5.1, 'Optional Normative LTM and BELT Requirements'

From Text:

General Device Requirements

…

- The minimum value for a BELT is 125 µs (refer to Table 8-36).

To Text:

General Device Requirements

…

- The minimum value for a BELT is 1 ms (refer to Table 8-36).

(b) Table 8-36. Timing Parameters

From Text:

Name	Description	Min	Max	Units
…	…	…	…	…
tBELTmin	Minimum value of best effort latency tolerance allowed in a Latency Tolerance Message	125		µs
…	…	…	…	…

To Text:

Name	Description	Min	Max	Units
…	…	…	…	…
tBELTmin	Minimum value of best effort latency tolerance allowed in a Latency Tolerance Message	1		ms
…	…	…	…	…

(c) Appendix C.4.1, 'Device State Machine Implementation Example'

From Text:

In this example, two device Latency Tolerance states (LT-states) are defined:

- **LT-idle state**: the device is idle and can tolerate a larger latency from the system (this is the default state).
- **LT-active state**: the device has determined a need to perform data transfers with the host and wants a shorter latency from the system.

A state machine is illustrated in Figure C-8.

To Text:

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- **LT-idle state**: the device is idle and can tolerate a larger latency from the system (this is the default state).
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A state machine for this example is illustrated in Figure C-8.

Note: the state machine described in this example is implementation-specific and is not intended to constrain implementers' design choices in any way. For example, another implementation might use the same BELT value at all times.

(d) Appendix C.4.1, 'Device State Machine Implementation Example'

From Text:

The following device design goals are to be met:

- Design for a minimum LTM BELT of 1 ms when in LT-idle
- Design for a minimum LTM BELT of 125 μs when in LT-active

To Text:

The following device design goals are to be met:

- Design for a minimum LTM BELT of 3 ms when in LT-idle
- Design for a minimum LTM BELT of 1 ms when in LT-active

(e) Appendix C.4.1.1, 'LTM-Idle State BELT'

From Text:

To achieve a minimum LT-idle state BELT of 1 ms, the total latency the device must be able to tolerate is 1 ms plus the worst case value for U2SEL, or a total of approximately 3.1 ms (refer to Section C.1.5.1). The worst case U2SEL is based on a worst case device-to-host U2 exit latency of 2.053 ms for t1 (2.047 ms device exit latency plus 1 μs for each of five hubs), plus 0.003 ms for t2, plus 0.001 ms for t4, plus some guard band.

For system implementations where U2SEL is less than its worst case value, the device reports a BELT value larger than 1 ms.

To Text:

To achieve a minimum LT-idle state BELT of 3 ms, the total latency the device must be able to tolerate is 3 ms plus the worst case value for U2SEL, or a total of approximately 5.1 ms (refer to Section C.1.5.1). The worst case U2SEL is based on a worst case device-to-host U2 exit latency of 2.053 ms for t1 (2.047 ms device exit latency plus 1 μs for each of five hubs), plus 0.003 ms for t2, plus 0.001 ms for t4, plus some guard band.

For system implementations where U2SEL is less than its worst case value, the device reports a BELT value larger than 3 ms.

(f) Appendix C.4.1.2, 'LTM-Active State BELT'

From Text:

To achieve a minimum LT-active state BELT of 125 μs, the total latency the device must be able to tolerate is 125 μs plus the maximum value for U1SEL, or a total of approximately 145 μs. The worst case U1SEL is based on a worst case device-to-host U1 exit latency of 15 μs for t1 (10 μs device exit latency plus 1 μs for each of five hubs), plus 3.1 μs for t2, plus 1.3 μs for t4, plus some guard band. This assumes the device will not allow its link to enter U2 prior to changing its state to LT-idle. If the device will allow its link to enter U2 when in LT-active, then the total latency the device must be able to tolerate is 125 μs plus the worst case value for U2SEL.

For system implementations where U1SEL is less than its worst case value, the device reports a BELT value larger than 125 μs.

To Text:

To achieve a minimum LT-active state BELT of 1 ms, the total latency the device must be able to tolerate is 1 ms plus the maximum value for U1SEL, or a total of approximately 1.020 ms. The worst case U1SEL is based on a worst case device-to-host U1 exit latency of 15 µs for t1 (10 µs device exit latency plus 1 µs for each of five hubs), plus 3.1 µs for t2, plus 1.3 µs for t4, plus some guard band. This assumes the device will not allow its link to enter U2 prior to changing its state to LT-idle. If the device will allow its link to enter U2 when in LT-active, then the total latency the device must be able to tolerate is 1 ms plus the worst case value for U2SEL.

For system implementations where U1SEL is less than its worst case value, the device reports a BELT value larger than 1 ms.

(g) Appendix C.4.2, 'Other Considerations'

From Text:

The following are additional considerations associated with device support of LTM:

- The BELT represents a latency tolerance for an entire peripheral device. The BELT value must be aggregated across all endpoints within the device, including all functions within a composite device. The smallest BELT value across all endpoints should be selected. For LTM purposes, isochronous endpoints are ignored when determining the BELT value.
- If LTM is supported by a device, LTM should be disabled prior to placing the device into suspend (refer to the PORT_LINK_STATE feature selector in Chapter 10). Devices send an updated LTM when LTM is enabled, or immediately before LTM is disabled, as defined in Chapter 8. Disabling LTM in this way ensures that a suspended device does not keep the system in a high state of readiness, wasting power.

To Text:

- The BELT represents a latency tolerance for an entire peripheral device. The BELT value must be aggregated across all endpoints within the device, including all functions within a composite device. The smallest BELT value across all endpoints should be selected. For LTM purposes, isochronous endpoints are ignored when determining the BELT value.