USB 3.1 ENGINEERING CHANGE NOTICE

Title: USB3.1 SKP Ordered Set Definition
Applied to: USB_3_1r1.0_07_31_2013

Brief description of the functional changes:

Section 6.4.3.2 contains the SKP Order Set Rules for Gen2 operation. The current SKP OS set definition is geared toward minimizing the BW overhead of SKP OS, but requires re-timers to meet exceptionally stringent elastic buffer design requirements. The current definition specifies that 1 SKP OS (12 SKPs) shall be transmitted once every 22 to 90 blocks, which requires elastic buffers to meet a very stringent SKP removal quantization error threshold. If a given elastic buffer exceeds the SKP removal quantization error threshold, then downstream elastic buffers may be starved of SKPs, leading to an elastic buffer overflow condition. There is also a concern that the worst case dynamic PPM profile across the re-timers has not been discovered and could lead to more stringent/resource intensive requirements for re-timers/endpoints. To mitigate these risk factors, this ECN changes the SKP OS definition to guarantee that each elastic buffer receives enough SKPs in a SKP OS to fully compensate for SI drift that occurred between a SKP OS interval, regardless of the SKP removal quantization error each elastic buffer introduces. In order to accomplish this, the transmitted SKP OS shall contain 20 SKPs (4 SKPs * 5 Elastic Buffers), and be transmitted on average of once every 40 blocks since the last transmitted SKP Ordered Set. The maximum SI drift over 40 blocks is less than 4. Therefore, upon receiving a SKP OS each re-timer in the link will be allowed to add 4 SKPs, remove 4 SKPs, or make no adjustments. This definition guarantees that each elastic buffer will have the opportunity to remove 4 SKPs for every received SKP OS, even when all other elastic buffers in the link remove 4 SKPs.

Benefits as a result of the changes:

This change drastically reduces the re-timer elastic buffer design requirements and the overall risk associated with clock frequency compensation for USB3.1.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:

No certified SSP product yet.

An analysis of the hardware implications:

Re-timer design based on USB3.1 specification has not begun at this point, so this will be the baseline.
Host and Device will need to make moderate modification to SKP OS handling/processing logic.

An analysis of the software implications:

None

An analysis of the compliance testing implications:

Compliance testing complexity for SKP OS will be drastically reduced. In order to verify that the SKP OS definition is being met, the compliance test will need to make sure a port either removes 4 SKPs, adds 4 SKPs or does nothing for each received SKP Ordered set.

USB 3.1 ENGINEERING CHANGE NOTICE

Actual Change

Section 6.3.2.2 Normative 128b/132b Decode Rules

From Text:

The physical layer shall encode the data on a per block basis. Each block shall comprise a 4-bit Block Header and a 128-bit payload. The 4-bit header is set to 0011b for data and 1100b for control blocks. This header format allows for the correction of single bit errors in the header information.

To Text:

The physical layer shall encode the data on a per block basis. Each block, except for the SKP Ordered Set control block, shall comprise a 4-bit Block Header and a 128-bit payload. The SKP Ordered Set control block shall be comprised of a 4-bit Block Header and a 192-bit payload. The 4-bit header is set to 0011b for data and 1100b for control blocks. This header format allows for the correction of single bit errors in the header information.

Section 6.4.3 Elasticity Buffer and SKP Ordered Set

From Text:

The Enhanced SuperSpeed architecture supports a separate reference clock source on each side of the Enhanced SuperSpeed link. The accuracy of each reference clock is required to be within +-300 ppm. This gives a maximum frequency difference between the two devices of the link of +- 600 ppm. In addition, SSC creates a frequency delta that has a maximum difference of 5000 ppm. The total magnitude of the frequency delta can range from -5300 to 300 ppm. This frequency delta is managed by an elasticity buffer that consumes or inserts SKP ordered sets.

SKP Ordered Sets shall be used to compensate for frequency differences between the two ends of the link. The transmitter sends SKP ordered sets at an average of every 354 symbols. However, SKP ordered sets shall not be inserted within any packet. The transmitter is allowed to buffer the SKP ordered sets up to a maximum of four SKP ordered sets. For Gen 1 operation the receiver shall implement an elasticity buffer capable of buffering (or starving) eight symbols of data. For Gen 2 operation, due to the presence of retimers along the signal path, a receiver shall tolerate not receiving any SKP Symbols for up to 180 blocks. Thus during Gen 2 operation a receiver must implement an elasticity buffer capable of buffering (or starving) twenty two symbols of data.

To Text:

The Enhanced SuperSpeed architecture supports a separate reference clock source on each side of the Enhanced SuperSpeed link. The accuracy of each reference clock is required to be within +-300 ppm. This gives a maximum frequency difference between the two devices of the link of +- 600 ppm. In addition, SSC creates a frequency delta that has a maximum difference of 5000 ppm. The total magnitude of the frequency delta can range from -5300 to 300 ppm. This frequency delta is managed by an elasticity buffer that consumes or inserts SKP ordered sets.

SKP Ordered Sets shall be used to compensate for frequency differences between the two ends of the link. For Gen1 operation, the transmitter sends SKP ordered sets at an average of every 354 symbols. However, SKP ordered sets shall not be inserted within any packet. The transmitter is allowed to buffer the SKP ordered sets up to a maximum of four SKP ordered sets. For Gen 1 operation the receiver shall implement an elasticity buffer capable of buffering (or starving) eight symbols of data.

For Gen 2 operation, the average interval between transmitted SKP Ordered Sets is 40 blocks. However, SKP Ordered Sets shall not be inserted within any packet. Consequently, the transmitter is allowed to buffer up to three SKP Ordered Sets. For Gen 2 operation the receiver shall implement an elasticity buffer capable of buffering (or starving) eleven symbols of data.

Section 6.4.3.2 SKP Rules (Host/Device/Hub) for Gen 2 Operation

From Text:

Table 6-12 describes the layout of the SKP Ordered Set when using 128b/132b encoding. A transmitted SKP Ordered Set always starts out as 16 Symbols long. The granularity for which SKP Symbols can be added or removed by a Port is two symbols. A port may add or remove more than 2 SKP symbols, but the number of SKP symbols that is added or removed shall be a multiple of two. This includes retimers within the signal path. Thus, a receiver may receive a SKP OS with anywhere from 0 to thirty six SKP symbols with the number of SKP symbols being a multiple of two. A SKP OS with 0 SKP symbols has only a SKPEND symbol followed by the three symbols that describe the LFSR state. Another impact of receiving variable length SKP OS is that a receiver is always allowed to add up to 12 SKP symbols to any SKP OS regardless of the length of the received SKP OS.

The SKPEND Symbol indicates the last four Symbols of SKP Ordered Set so that receivers can identify the location of the next Block Header in the bit stream. The three Symbols following the SKPEND Symbol contain different information depending on the LTSSM state.

A receiver must always perform single bit error correction on the SKP and SKPEND (and all other special) symbols. However, since the Hamming distance between the SKP and SKPEND symbols is 8, once a receiver has determined that it is dealing with a non-empty SKP OS (by proper detection of a first SKP symbol) it may be beneficial to use multiple bit (up to 3-bit) error correction in differentiating between a SKP and a SKPEND symbol.

Table 6-1. Gen 2 SKP Ordered Set

Symbol Number	Value	Description
0 through 2*N-1 [N can be 0 through 18]	CCh	SKP Symbol Symbol 0 is the SKP Ordered Set Identifier Note: for an empty SKP OS, the first symbol will be a SKPEND.
2*N	33h	SKPEND Symbol
2*N+1	00-FFh	(i) If prior block was a Data Block: Bit[7] = Even Data Parity Bit[6:0] = LFSR[22:16] (ii) Else: Bit[7] = ~LFSR[22] Bit[6:0] = LFSR[22:16]
2*N+2	00-FFh	(i) If LTSSM state is Compliance mode: Error_Status[7:0] (ii) Else LFSR[15:8]
2*N+3	00-FFh	(i) If LTSSM state is Compliance mode: ~Error_Status[7:0] (ii) Else LFSR[7:0]

The following rules apply for SKP insertion for Gen 2 operation:

1. A transmitter shall keep a running count of the number of transmitted blocks since the last SKP Ordered set. The value of this count will be referred to as Y. The value of Y is reset whenever the transmitter enters Polling.Active or when a SKP OS is transmitted.
2. Once the count, Y, gets to 21 a transmitter must insert a SKP OS at the next legitimate opportunity. The fastest a transmitter can insert SKP OS is once every 22 blocks. Situations

that delay the immediate insertion of a SKP OS are the following: a transmitter shall not interrupt a data packet or a SYNC OS to insert a SKP OS. In the worst case it may take 90 blocks before there is an opportunity to insert a SKP OS. In Gen 2 operation there is no accumulation of SKP OS, each time a SKP OS is transmitted the SKP counter,Y, is reset to 0.

3. SKP Ordered Sets do not count as interruptions when monitoring for Ordered Sets (i.e., consecutive TS1, TS2 Ordered Sets in Polling and Recovery).
4. SYNC ordered sets have priority of SKP ordered sets. A SKP OS that is scheduled to be sent at the same time as a SYNC OS shall have to be delayed until the SYNC OS is transmitted.
5. The Data parity bit should be even parity for last three symbols in the SKP OS. The parity is a check of the LFSR seed value.

To Text:

Table 6-12 describes the layout of the SKP Ordered Set for Gen2 operation. A transmitted SKP Ordered Set is 24 symbols. The granularity for which SKP Symbols can be added or removed is four SKP symbols. Upon receiving a SKP ordered set, a re-timer shall perform one and only one of the following adjustments: add four SKPs, remove four SKPs, or make no adjustment. Thus, a received SKP OS can have anywhere from 4 to 36 SKP symbols with the number of SKP symbols being a multiple of four. The SKPEND Symbol indicates the last four Symbols of SKP Ordered Set so that receivers can identify the location of the next Block Header in the bit stream. The three Symbols following the SKPEND Symbol contain the transmitter LFSR state.

A receiver shall always perform single bit error correction on the SKP and SKPEND (and all other special) symbols. However, since the Hamming distance between the SKP and SKPEND symbols is 8, once a receiver has determined that it is dealing with a SKP OS (by proper detection of a first SKP symbol) it may be beneficial to use multiple bit (up to 3-bit) error correction in differentiating between a SKP and a SKPEND symbol.

Table 6-2. Gen 2 SKP Ordered Set

Symbol Number	Value	Description
0 through 4*N-1 [N can be 1 through 9]	CCh	SKP Symbol Symbol 0 is the SKP Ordered Set Identifier
4*N	33h	SKPEND Symbol
4*N+1	40-BFh	Bit[7] = ~LFSR[22] Bit[6:0] = LFSR[22:16]
4*N+2	00-FFh	LFSR[15:8]
4*N+3	00-FFh	LFSR[7:0]

Note: The transmitted LFSR state is intended for use by test equipment vendors needing to re-synch their data scramblers. The transmitted LFSR state is not intended to be used by ports in normal operation.

The following rules apply for SKP insertion for Gen 2 operation:

1. A port shall keep a running count of the number of transmitted blocks since the last SKP Ordered Set. The value of this count will be referred to as Y. The value of Y is reset whenever the transmitter enters Polling.Active. Y is not incremented for transmitted SKP Ordered Sets.
2. A port shall calculate the integer result of Y/40 when an opportunity to insert a SKP Ordered Set arises. The integer result of Y/40 is the number of accumulated SKP Ordered Sets that need to be transmitted – this value will be referred to as Z. The value of Z can be either 0, 1, 2, or 3.

Note: The non-integer remainder of the Y/40 SKP calculation shall not be discarded and shall be used in the calculation to schedule the next SKP Ordered Set.

3. Unless otherwise specified, when the LTSSM is not in the loopback state, a transmitter shall insert Z SKP Ordered Sets immediately after each transmitted SYNC, TS1, TS2, SDS, LMP, Header Packet, Data Packet, or Logical idle. When the LTSSM is in the Loopback state, the Loopback Master transmitter shall insert 2*Z SKP Ordered Sets immediately after each transmitted SYNC, TS1, TS2, SDS, LMP, Header Packet, Data Packet, or Logical idle. A transmitter shall not transmit SKP Ordered Sets at any other time.
4. SKP Ordered Sets do not count as interruptions when monitoring for Ordered Sets (i.e., consecutive TS1, TS2 Ordered Sets in Polling and Recovery).
5. SYNC ordered sets have priority over SKP ordered sets. A SKP OS that is scheduled to be sent at the same time as a SYNC OS shall be delayed until the SYNC OS is transmitted.
6. The Data parity bit should be even parity for last three symbols in the SKP OS. The parity is a check of the LFSR seed value.

6.8.4 Receiver Loopback

From Text:

The entry and exit process for receiver loopback is described in Chapter 7.
Receiver loopback must be retimed. Direct connection from the Rx amplifier to the transmitter is not allowed for loopback mode. The receiver shall continue to process SKPs as appropriate. SKP symbols shall be consumed or inserted as required for proper clock tolerance compensation. Over runs or under runs of the clock tolerance buffers will reset the buffers to the neutral position.
During loopback the receiver shall process the Bit Error Rate Test (BERT) commands.
Loopback shall occur in the 10-bit domain for Gen 1 operation and in the 132-bit domain for Gen 2 operation. No error correction is allowed. All symbols shall be transmitted as received with the exception of SKP and BERT commands.

To Text:

The entry and exit process for receiver loopback is described in Chapter 7.
Receiver loopback must be retimed. Direct connection from the Rx amplifier to the transmitter is not allowed for loopback mode. The receiver shall continue to process SKP Ordered Sets as appropriate. For Gen1 operation, SKP symbols shall be consumed or inserted as required for proper clock tolerance compensation. For Gen2 operation, the receiver can either add 4 SKPs, remove 4 SKPs or make no adjustment to the received SKP Ordered Set. The modified SKP Ordered Set shall meet the requirements specified in Section 6.4.3.2 (i.e. must contain between 4 and 36 SKPs followed by the SKPEND Symbol and 3 Symbols that proceed the SKPEND.) Over runs or under runs of the clock tolerance buffers will reset the buffers to the neutral position.
During loopback the receiver shall process the Bit Error Rate Test (BERT) commands.
Loopback shall occur in the 10-bit domain for Gen 1 operation and in the 132-bit domain for Gen 2 operation. No error correction is allowed. All symbols shall be transmitted as received with the exception of SKP and BERT commands.