# USB 3.1 ENGINEERING CHANGE NOTICE

## Title: TSEQ Gen2 Clarification
## Applied to: USB_3_1r1.0_07_31_2013

| **Brief description of the functional changes:** |
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| Clarification of the TSEQ rules for Gen 2 operation. |

| **Benefits as a result of the changes:** |
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| Eliminate confusion about the number of times that the Gen 2 TSEQ ordered set is transmitted and about the periodicity of the training pattern. |

| **An assessment of the impact to the existing revision and systems that currently conform to the USB specification:** |
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| Applies to Gen 2 only. No existing systems with Gen 2 implementation, so no impact. |

| **An analysis of the hardware implications:** |
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| Ensures TSEQ is implemented correctly. |

| **An analysis of the software implications:** |
|---|
| None |

| **An analysis of the compliance testing implications:** |
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| Ensures test equipment suppliers implement TSEQ algorithms correctly. |

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## Actual Change

## (a). From Text (and location): Section 6.4.1.2.2, Page 6-16

#### 6.4.1.2.2 Training Sequence Values for Gen 2 Operation

Transmitters are required to track the running DC Balance of the bits transmitted on the wire (after scrambling) for TSEQ, TS1 and TS2 Ordered Sets. The running DC Balance is the difference between the number of 1s transmitted and the number of 0s transmitted.

## (a). To Text (and location): Section 6.4.1.2.2, Page 6-16

#### 6.4.1.2.2 Training Sequence Values for Gen 2 Operation

The TSEQ training sequence is transmitted 524,288 times to allow for testing many coefficient settings.

Transmitters are required to track the running DC Balance of the bits transmitted on the wire (after scrambling) for TSEQ, TS1 and TS2 Ordered Sets. The running DC Balance is the difference between the number of 1s transmitted and the number of 0s transmitted.

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## (b). From Text (and location): Section 7.5.4.7.1, Page 7-61

#### 7.5.4.7.1 Polling.RxEQ Requirements

- The detection and correction of the lane polarity inversion in SuperSpeed operation shall be enabled, as is described in Section 6.4.2.
- The port shall transmit the corresponding TSEQ ordered sets defined in Table 6-2.

## (b). To Text (and location): Section 7.5.4.7.1, Page 7-61

#### 7.5.4.7.1 Polling.RxEQ Requirements

- The detection and correction of the lane polarity inversion in SuperSpeed operation shall be enabled, as is described in Section 6.4.2.
- The port shall transmit the corresponding TSEQ ordered sets defined in Table 6-2 for SuperSpeed operation, or Table 6-8 for SuperSpeedPlus operation.

## (c). From Text (and location): Section 7.5.4.7.2, Page 7-62

#### 7.5.4.7.2 Exit from Polling.RxEQ

- The port in SuperSpeed operation shall transition to Polling.Active after 65,536 consecutive TSEQ ordered sets defined in Table 6-2 are transmitted.
- The port in SuperSpeedPlus operation shall transition to Polling.Active after 262,143 TSEQ ordered sets defined in Table 6-8 are transmitted. Refer to Section 6.4.1.2.1 for SYNC ordered set insertion while transmitting TSEQ ordered sets.

## (c). To Text (and location): Section 7.5.4.7.2, Page 7-62

#### 7.5.4.7.2 Exit from Polling.RxEQ

- The port in SuperSpeed operation shall transition to Polling.Active after 65,536 consecutive TSEQ ordered sets defined in Table 6-2 are transmitted.
- The port in SuperSpeedPlus operation shall transition to Polling.Active after 524,288 TSEQ ordered sets defined in Table 6-8 are transmitted. Refer to Section 6.4.1.2.1 for SYNC ordered set insertion while transmitting TSEQ ordered sets.

## (d). From Text (and location): Section 6.8.1, Page 6-35

The 3rd paragraph of section 6.8.1:

During Gen 2 operation, the training period is ~8ms. The training pattern is periodic with a period of 16384 132-bit blocks (2162688UI ). The much longer pattern greatly increases the richness of the pattern compared to Gen 1. The Gen 2 training pattern spectrum is essentially white. Due to the length of the Gen 2 training interval and the potential desire to examine the data, SKPs are inserted during polling.TSEQ.

## (d). To Text (and location): Section 6.8.1, Page 6-35

During Gen 2 operation, the training period is ~8ms. The training pattern is periodic with a period of 16385 132-bit blocks (16384 TSEQ blocks plus a SYNC OS block). The much longer pattern greatly increases the richness of the pattern compared to Gen 1. The Gen 2 training pattern spectrum is essentially white. Due to the length of the Gen 2 training interval and the potential desire to examine the data, SKPs are inserted during polling.TSEQ.