E   Repeaters

E.1   Overview

E.1.1   Definitions

In this document, the following definitions apply:

Repeater refers to any active component that acts on a signal in order to increase the physical lengths and/or interconnect loss over which the signal can be transmitted successfully. The category of repeaters includes both retimers and re-drivers, which are defined below.

Retimer refers to a component that contains a clock-data recovery (CDR) circuit that "retimes" the signal. The retimer latches the signal into a synchronous memory element before re-transmitting it. It is used to extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the retimer.

Re-driver refers to an analog component that operates on the signal without re-timing it. This may include equalization, amplification, and transmitter. The re-driver does not include a CDR.

Device captive retimer refers to a retimer that is located on the same printed circuit as the device silicon. The retimer is said to be associated with the device.

Host captive retimer refers to a retimer that is located on the same printed circuit as the host silicon. In this case, the retimer is said to be associated with the host.

Link segment refers to a transmitter-channel-receiver combination between a downstream port and a retimer, and upstream port and a retimer, or between two retimers. This is demonstrated in Figure E-1.
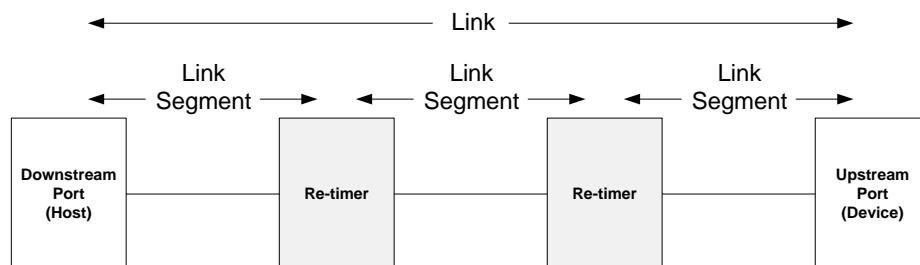

Figure E-1. Link segment definition.

E.1.2   Scope

E.1.2.1 Retimers

This appendix defines the requirements for CDR-based (re-timing) repeaters, a.k.a. retimers, and includes requirements for both the physical and link layers. A retimer may be used on a printed circuit board in conjunction with a host or device, or as part of a cable assembly.

The USB usage model, which matches hosts, devices and cables at the time of usage, allows for the construction of systems that include retimers on all three components. The requirements set forth in this appendix comprehend the use of up to four retimers in a system.

Figure E-2 depicts examples of USB systems that employ repeaters. Note that the figure does not depict all allowed configurations.
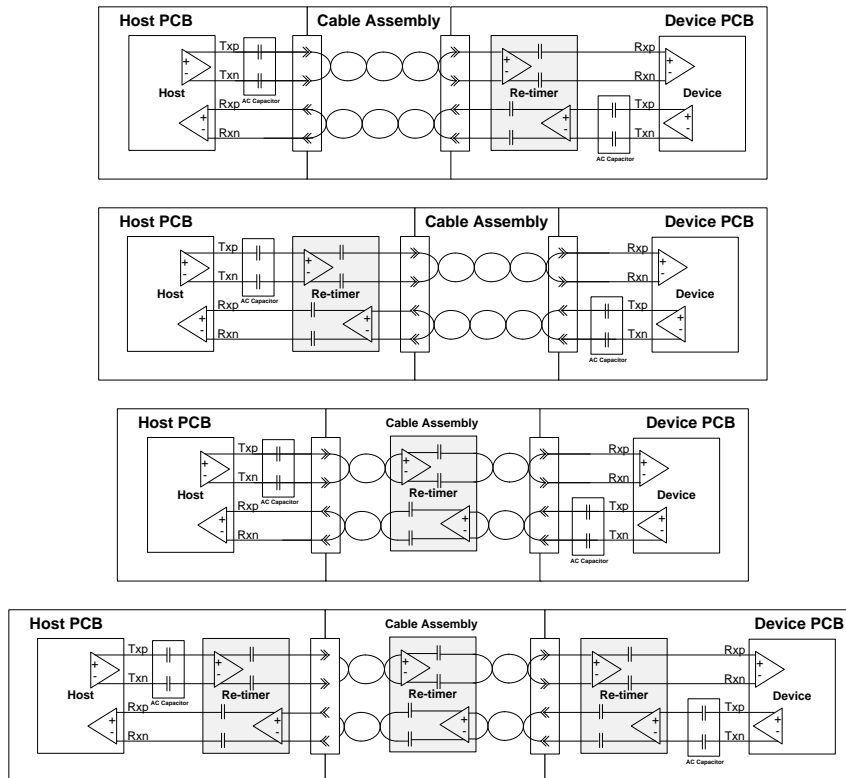

Figure E-2. Retimer implementation examples.

E.1.2.2 Re-drivers

Analog re-drivers are beyond the scope of this document.

E.2 Retimer Architectural Overview and Requirement

The primary motivation of a retimer is to relay the communications by re-generating the signal to the quality matching the transmitter requirement defined in Chapter 6. To achieve this, the incoming data at the receiver is recovered and re-transmitted by the retimer with the transmit clock generated based on a local reference clock. Given this basic retimer operation, some retimer specific architectural considerations and requirements need to be addressed and are covered by this section.
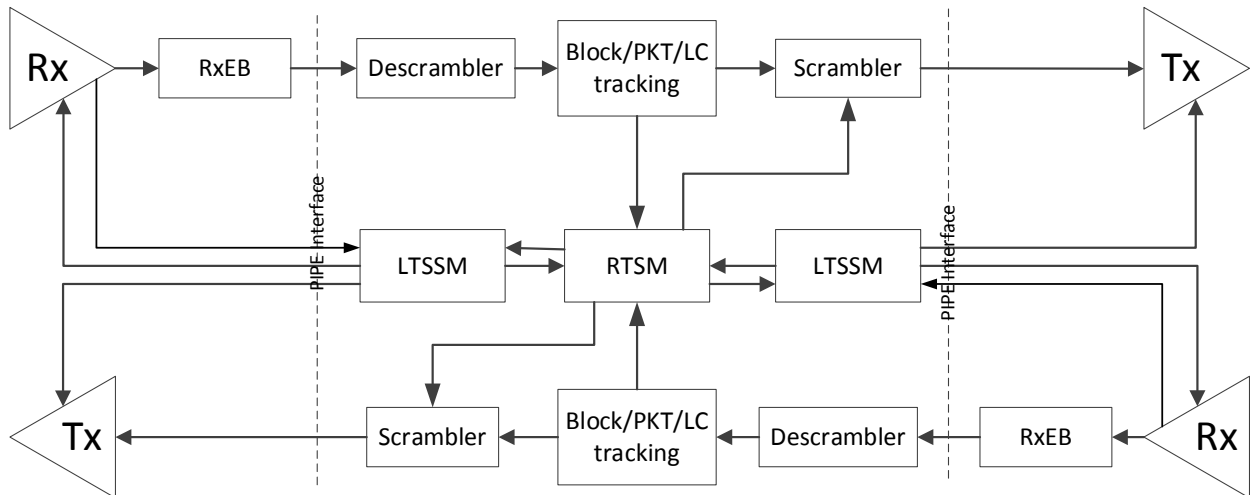
Figure E-3. Example high level retimer architecture in Gen 2 operation

E.2.1 Architectural Overview

Shown in Figure E-3 is a high level retimer architectural example for gen 2 operation. Although the data path architecture from a receiver to its transmitter for gen 2 operation maybe different from Gen 1 operation, the architectural framework between Gen 1 operation and Gen 2 operation is the same. Refer to Figure E-3 for a retimer architectural example for Gen 1 operation.

Each retimer consists of a downstream port and an upstream port to perform clock data recovery at its receivers and data transmission at its transmitters. Each port has its own LTSSM to manage the operation in various link states, and both LTSSMs are very similar to LTSSM defined in chapter 7, but with differences unique to retimer operations that are described in Section E.2.3. A retimer state machine (RTSM) is employed to coordinate the operation between its upstream port and downstream port. In addition, the RTSM is also responsible to serve the following management functions:

- Link state detection and retimer power management.
- Data path management and clock offset compensation.
- Packet/link command detection, error detection and correction (if applicable).

E.2.2 General requirements

A retimer shall include the capability to successfully train and operate in both SuperSpeed Gen 1 and Gen 2 modes. This includes implementation of all training and power states defined in chapters 6 and 7.

The timing budgets, signal levels, and compliance specifications defined in chapter 6 apply to retimers. As with SuperSpeed and SuperSpeedPlus hosts and devices, retimers shall implement spread spectrum clocking (SSC) in compliance with the requirements contained in section 6.5.3 and 6.5.4 of the base specification.

E.2.2.1 Physical Layer Requirements

Retimers shall meet the transmitter requirements defined in section 6.7 including:

- the normative requirements defined in table 6-17
- the normative eye mask requirements defined in table 6-19

The informative transmitter requirements defined in table 6-18 also apply to retimers. Table 6-15 in section 6.5 defines transmitter jitter targets which apply to retimers.

The transmitter shall implement the low frequency periodic signaling (LFPS) and LFPS-based pulse modulation (LBPM) features defined in section 6.9, meeting all requirements defined in that section.

E.2.2.2 Link Layer Requirements

The purpose for retimers to implement partial link layer function includes the following.

- TS2 ordered set decoding. A retimer shall decode the link configuration field to determine the link operation during Polling.Idle or Recovery.Idle. Refer to Section E.2.3 for retimer specific link configuration and operation.
- Link command tracking. A retimer shall track the link command for link power management.
- IS and DPP tracking. A retimer operating at SuperSpeed shall track IS and DPP for the clock offset compensation. Refer to Section E.4.1 for details.

Some additional rule of the link layer operation may apply.

- A retimer shall correct any single symbol error detected in any framing order sets when forwarding.
- A retimer may optionally correct the link command that contains one invalid link command field replica.

E.2.3   Retimer Operation

The primary responsibility of a retimer shall include the following:

- Connectivity detect and monitoring. A retimer upon power-up shall perform the presence detect of its remote link partners, being a hub downstream port, or an upstream port, or a retimer port. This is achieved by performing far-end receiver termination detection periodically. A retimer shall also monitor the operation and be aware when its link partners may be disconnected or disabled.
- Participation of link initialization and training. A retimer, upon establishing connection with its link partners, shall participate the link initialization and training. This includes:
  - o Speed negotiation: a retimer in Polling substates shall either forward or re-generate and monitor the Polling.LFPS signal and LBPMs in order to determine the data rate its link partners has agreed upon completion of speed negotiation, and configure itself towards the negotiated data rate.
  - o Equalization training: a retimer shall transmit TSEQ OS based on its local reference clock to train the receivers of its link partners, while training its own receiver equalization.
  - o Bit/symbol/block alignment and link configuration: a retimer shall perform bit/symbol/block alignment to achieve end to end link training and decode TS2 OS in order to determine what the link configuration is. This includes: U0, Hot Reset, Local Loopback, and PassThrough Loopback. Clock offset compensation shall be

performed in these Polling substates. Refer to Section E.2.5 for details of clock offset compensations in SS and SSP operations.

- Traffic relay. A retimer in U0 shall relay the traffic in both directions. This includes eSS packets and IS. Clock offset compensation shall be performed accordingly in this state depending on the rate it is operating. Refer to Section E.2.5 for details of clock offset compensations in SS and SSP operations.

- LFPS relay. LFPS signal may be detected under all link states except eSS.Disabled. A retimer shall process and re-transmit the LFPS signals meeting the electrical and timing requirements defined in Section 6.9. Refer to Section E.2 for special treatment of LFPS transmission under different link states.

- Link power management. While forwarding the traffic, the retimer shall track the link command to determine if link is preparing to enter a low power link state. When in a low power state, the retimer shall also monitor the connectivity of its link partners and prepare for link state transition.

- Error recovery. While the retimer may perform error correction at its inbound traffic (U0 only), such as single-bit block header error, single/double-bit SSP SKP symbol error, and etc., to preserve the quality of link operation, it shall leave the decision of entry to Recovery to the host and device.

E.3   Retimer Training and Status State Machine (RTSSM)

The RTSSM shown in Figure E-4 is similar to the LTSSM defined in Chapter 7. The main differences between RTSSM and LTSSM are summarized in the following.

- eSS.Inactive is combined with Rx.Detect as the behaviors of a retimer in those two states are the same. A retimer, even upon detecting the presence of its far-end link partners, will not transition to Polling until Polling.LFPS is received.

- eSS.Disabled is defined in the LTSSM for a self-powered peripheral device where it may operate at USB2 mode. The eSS operation is disabled and the link may enter the lowest power state. For retimer operation, unless it is aware of the link configuration, it will not be able to take the advantage of this state. However, it is kept for implementations capable of managing the retimer operation under proprietary mechanism, which is out of the scope of this specification.

- PassThrough Loopback is introduced for a retimer. It is a special operation pertained to a retimer only when the LTSSM is in Loopback. A retimer in this state passes the inbound traffic directly as if it is in U0.

- Local Loopback is named to contrast PassThrough Loopback. The purpose and the operation of a retimer in this state are the same as Loopback defined in LTSSM.
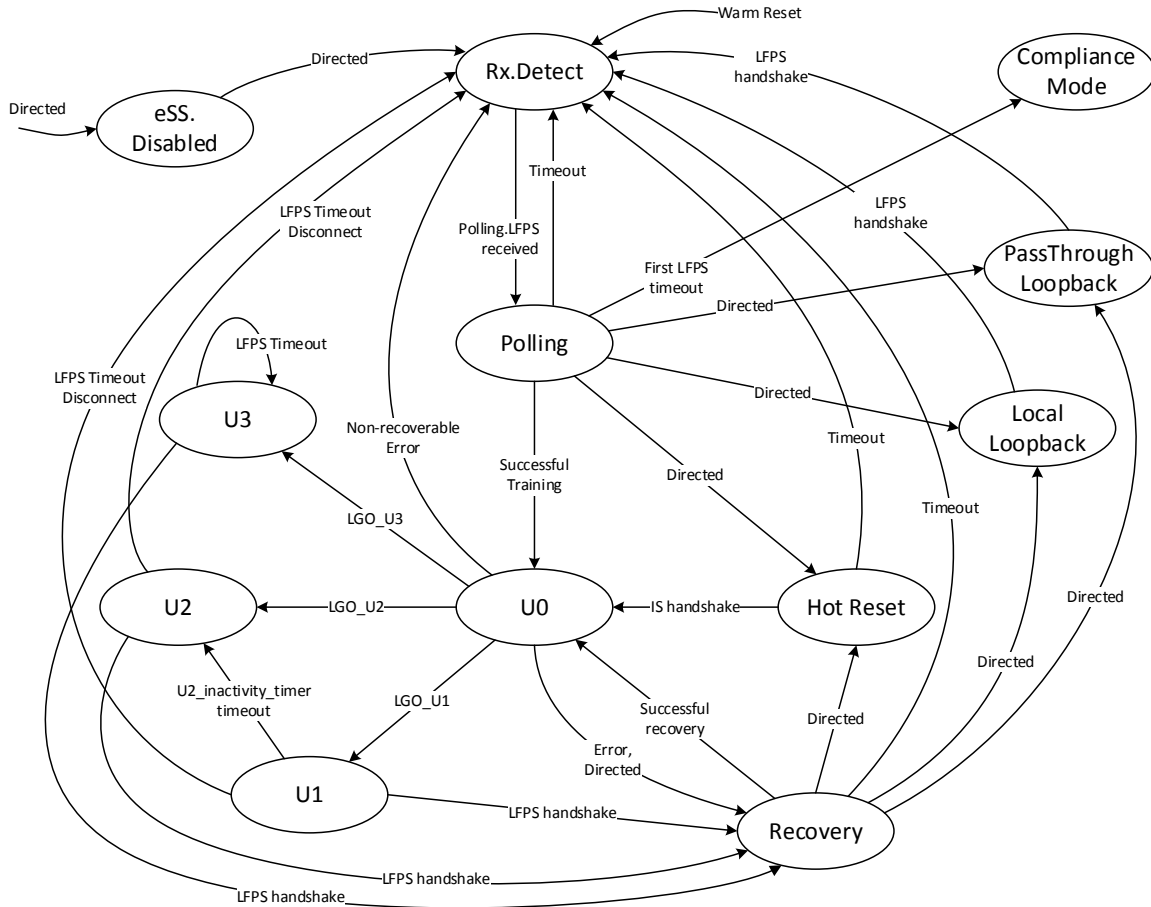
Figure E-4. Retimer Training and Status State Machine

In the following subsections, the details of RTSSM are described. The operations that are common to LTSSM will not be elaborated.

It is worth mentioning that the main purpose of RTSSM is to describe and define the retimer operation under various LTSSM states. The external behavior of the RTSSM shall reflect that of the LTSSM. The implementation may vary regarding RTSSM optimization.

E.3.1 Rx.Detect

Rx.Detect is the default power-on state of the retimer. The retimer's responsibility is to detect the presence of its link partners by performing far-end receiver termination periodically and mirror the presence status of its link partners.

E.3.1.1 Rx.Detect Requirement

- The retimer's receiver terminations at both ports shall present high impedance to ground of $Z_{RX-HIGH-IMP-DC-POS}$ defined in Table 6-21. Note that a retimer may not have the knowledge to which port a host or a device is connected upon power-on.
- The retimer shall initiate a far-end receiver termination detection at both ports every 12ms.

- The retimer, upon detecting far-end low-impedance receiver termination (R_{RX-DC}) defined in Table 6-21, shall enable its low-impedance receiver termination (R_{RX-DC}) at its respective port to mirror the presence of its link partner.
- The retimer shall forward Polling.LFPS it may receive in this state.
- The retimer shall forward and decode Warm Reset it may receive. The retimer shall ensure the duration of forwarded Warm Reset meeting the timing requirement defined in Section 6.9.3. Note that the retimer may also map its port receiving Warm Reset as USP, and its port transmitting Warm Reset as DSP.

E.3.1.2 Exit from Rx.Detect

- A retimer shall transition to Polling if Polling.LFPS is received.

E.3.2 eSS.Disabled

eSS.Disabled is an optional state where no eSS activity is enabled. The retimer is at its lowest possible power state. Note that there is no defined mechanism for entry to and exit from eSS.Disabled. It is implementation's responsibility to manage eSS.Disabled based on its capabilities.

E.3.2.1 eSS.Disabled Requirements

- The retimer shall present high impedance to ground of $Z_{RX-HIGH-IMP-DC-POS}$ defined in Table 6-21 at both ports.
- The retimer shall be in its lowest power state.

E.3.2.2 Exit from eSS.Disabled

- The retimer shall transition to Rx.Detect upon direction.

E.3.3 Polling

Polling is a state for retimer to participate in speed negotiation, link training and determine the state of operation upon exit from Polling. A simplified Polling substate machine of the retimer is shown in Figure E-5. Note that the transition to Rx.Detect due to Warm Reset is not shown.
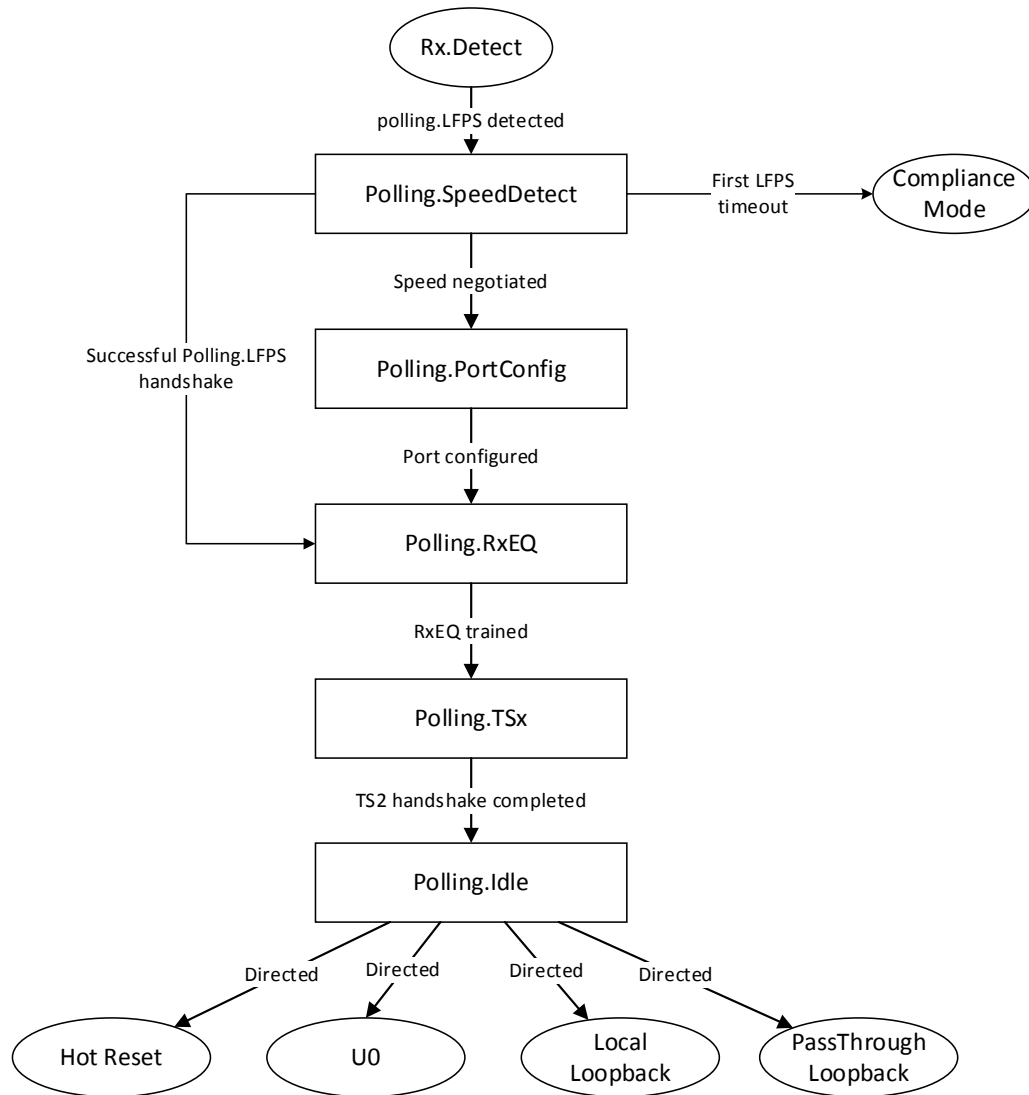
Figure E-5. Polling Substate Machine

E.3.3.1 Polling.SpeedDetect

Polling.SpeedDetect is a substate that covers the following substates in LTSSM.

- Polling.LFPS
- Polling.LFPSPlus
- Polling.PortMatch

The retimer's responsibility in this substate includes:

- Relay the LFPS based signals include Polling.LFPS, SCD1/SCD2, and LBPM.

- Decode the LFPS signal to determine the negotiated data rate.

E.3.3.1.1 Polling.SpeedDetect Requirements

- The retimer shall decode the following received LFPS signals and monitor the status and progression of the LTSSM.

- o Polling.LFPS
- o SCD1/SCD2
- o LBPM
- o Warm Reset

- The retimer shall forward the LFPS signals meeting the electrical and timing requirements defined in Section 6.9. The retimer shall perform the following when forwarding the LFPS signals.
  - o If it's Polling.LFPS or SCD1/SCD2, the retimer shall qualify between Polling.LFPS and SCD1/SCD2. The retimer may store before forward between four to eight Polling.LFPS to determine if it's Polling.LFPS with non-variant tRepeat, or SCD1/SCD2.
  - o If it's Warm Reset, it shall ensure that the forwarded Warm Reset shall meet the timing specification defined in Section 6.9. The retimer shall start forwarding Warm Reset upon finding it is neither Polling.LFPS, nor SCD1/SCD2, nor LBPM. Note that the retimer may not be able to declare Warm Reset until the minimum duration of LFPS qualifies itself as Warm Reset. The retimer shall not wait until Warm Reset declaration before start the forwarding. Also note that the retimer shall follow similar approach when in other link states.

- The retimer shall start the tPollingLFPSTimeout timer upon receiving Polling.LFPS.
- The retimer shall start the tPollingLBPMLFPSTimeout timer upon observing LBPM.
- The retimer shall implement a tPollingSCDLFPSTimeout timer to monitor the absence of LFPS signal after the completion of SuperSpeed Polling.LFPS handshake.
- The retimer shall enable the transition path to Compliance Mode at its other port if only SCD2 is detected.

E.3.3.1.2 Exit from Polling.SpeedDetect

- Both ports of the retimer shall enter Compliance Mode upon timeout of the tPollingLFPSTimeout timer and the following three conditions are met.
  - o SCD2 is received upon entry to the substate.
  - o No Polling.LFPS handshake is achieved.
  - o The condition to transition to Polling.RxEQ or Polling.LFPSPlus is not met.
- The retimer shall transition to Polling.RxEQ for SS operation if the following two conditions are met.
  - o Successful Polling.LFPS handshake is observed.
  - o Upon timeout of the tPollingSCDLFPSTimeout timer.
- The retimer shall transition to Polling.PortConfig if it has observed successful LBPM handshake for port match.
- The retimer shall transition to Rx.Detect if one of the following conditions is met.
  - o Warm Reset is detected.
  - o The tPollingLBPMLFPSTimeout timer has expired.

E.3.3.2 Polling.PortConfig

Polling.PortConfig is a substate for the retimer to configure itself towards the negotiated data rate it has detected. The operation of the retimer is the same.

E.3.3.2.1 Polling.PortConfig Requirements

- The retimer shall not forward any PHYReady LBPMs before it is ready for SSP training.

- The retimer shall monitor and forward the received LBPMs until a successful handshake is reached. Note that the forwarded LBPMs shall meet the electrical and timing requirements defined in Section 6.9.

- The retimer shall start the tPollingLBPMLFPSTimeout timer upon entry to this substate.

E.3.3.2.2 Exit from Polling.PortConfig

- The retimer shall transition Polling.RxEQ if it has observed successful PHYReady LBPM handshake.

- The retimer shall transition to Rx.Detect if one of the following conditions is met.
    - Warm Reset is detected.
    - The tPollingLBPMLFPSTimeout timer has expired.

E.3.3.3 Polling.RxEQ

Polling.RxEQ is a substate for eSS receiver equalization training. The training mechanism is the same as defined in LTSSM except the exit.

E.3.3.3.1 Polling.RxEQ Requirements

- The lane polarity detection and correction for SS operation shall be enabled.

- The retimer shall generate TSEQ OS based on its own reference clock.

- The retimer shall not forward any TSEQ OS it has received.

- Upon completing the number of TSEQ OS transmission, the retimer shall continue the TSEQ OS transmission until TS1 OS at its other port has been recovered and ready to be forwarded.

- The retime shall start a 12-ms timer upon entry to the substate.

E.3.3.3.2 Exit from Polling.RxEQ

- The retimer shall transition to Polling.TSx if all the following conditions are met.
    - Its receiver equalization is trained.
    - TS1 OS is received.
    - The operation of the retimer EB is established and the TS1 OS is ready to be forwarded.

- The retimer shall transition to Rx.Detect if Warm Reset is one of the following conditions is met:
    - Warm Reset is detected.
    - The expiration of the 12-ms timer and the transition conditions to Polling.TSx are not met.

E.3.3.4 Polling.TSx

Polling.TSx is a substate where the retimer tracks the TS1/TS2 OS to achieve end to end symbol/block alignment.

E.3.3.4.1 Polling.TSx Requirements

- The lane polarity detection and correction shall be completed.
- The retimer shall monitor the status and progression of the LTSSM.
- The retimer shall perform the clock offset compensation based on the following.
    - For SS operation, the retimer shall perform the clock offset compensation as defined in Section E.3.4.1.
    - For SSP operation, the retimer shall perform the clock offset compensation as defined in Section 6.4.3.
- The retimer shall maintain synchronicity of the scrambler/descrambler operation with its link partners.
- The retimer shall maintain DC balance of its forwarded TS1/TS2 OS.
- The retimer shall not perform error correction within its received TS1/TS2 OS. This includes block headers in SSP operation.
- The retimer shall start the tPollingActiveTimeout timer upon entry to this substate.
- The retimer shall start the tPollingConfigurationTimeout timer upon observing TS2 OS at both ports.

E.3.3.4.2 Exit from Polling.TSx

- The retimer shall transition to Polling.Idle upon observing successful TS2 handshake.
- The retimer shall disable its eSS transceivers and remain in this substate if both of the following two conditions are met.
    - The tPollingActiveTimeout timer has expired for three consecutive times. Note this implies the retimer has remained in this substate for 36-ms.
    - No successful TS1 and/or TS2 OS handshakes have been observed.

Note that this is an error state where retimer can remain until Warm Reset is received.

- The retimer shall transition to Rx.Detect if one of the following conditions is met.
    - Warm Reset is detected.
    - The tPollingActiveTimeout timer has expired.

E.3.3.5 The tPollingConfigurationTimeout timer has expired.Polling.Idle

Polling.Idle is a substate where the retimer decodes TS2 OS and decides the next operation state.

E.3.3.5.1 Polling.Idle Requirements

- The retimer shall decode the link configuration field in TS2 OS and configure itself to the corresponding operation state.
- The retimer in SS operation shall not delete any idle symbols for the overflow clock offset compensation.

- The retimer shall manage its scrambler operation according to the link configuration field in TS2 OS.

- The retimer shall start the tPollingIdleTimeout timer to monitor the progression of LTSSM.

E.3.3.5.2 Exit from Polling.Idle

- The retimer shall transition to U0 if successful idle symbol handshake is observed.

- The retimer shall transition to PassThrough Loopback if the Loopback bit (bit 2 of the link configuration field) in the link configuration field is asserted.

- The retimer shall transition to Local Loopback as the loopback slave if the retimer loopback bit (bit 4 in the link configuration field) is asserted. Note that it is illegal to have both bit4 and bit 2 asserted. If both bits are asserted, the retimer shall give priority to PassThrough Loopback.

- The retimer shall transition to Hot Reset if the Reset bit is asserted.

- The retimer shall transition to Rx.Detect if one of the following conditions is met.
    - Warm Reset is detected.
    - The tPollingIdleTimeout timer has expired.

E.3.4   Compliance Mode

The retimer operation in Compliance Mode is the same as LTSSM.

E.3.5   U0

U0 is the normal operational state where packets are forwarded by the retimer in both directions.

E.3.5.1 U0 Requirements

- The retimer shall monitor and decode the link command to participate retimer and link power management.
- The retimer shall monitor LMP based link initialization upon entry to U0 in order to determine its port orientation towards a hub downstream port or device upstream port.
- The retimer shall decode U2 Inactivity timeout LMP from host, when acknowledged by device with ACK.
- The retimer shall maintain its scrambler synchronization with its link partners.
- The retimer shall maintain DC balance on its outbound traffic.
- The retimer shall perform the clock offset compensation as defined in Section E.3.6.
- The retimer shall not initiate entry to Recovery due to bit errors at its inbound traffic.
- The retimer shall remain in this state even if the bit/symbol lock or block alignment is lost. Under this scenario, the retimer shall perform necessary bit/symbol lock and block alignment. The retimer shall transmit IS until inbound traffic is recovered, or entry to Recovery is detected.
- The retimer in SS operation shall perform single symbol error correction on any framing OS.
- The retimer in SSP operation shall perform error correction if the following bit errors are detected.
    - Single-bit block header error.
    - Single/double-bit SKP symbol error.

- o   Single-symbol framing OS error.
- o   Replica link command word error.

E.3.5.2 Exit from U0

- The retimer shall transition to U1 upon successful completion of LGO_U1 entry sequence. Refer to Section 7.2.4.2 for details.
- The retimer shall transition to U2 upon successful completion of LGO_U2 entry sequence. Refer to Section 7.2.4.2 for details.
- The retimer shall transition to U3 upon successful completion of LGO_U3 entry sequence. Refer to Section 7.2.4.2 for details.
- The retimer shall transition to Recovery upon observing TS1 OS.
- The retimer shall transition to Rx.Detect when Warm Reset is detected.

E.3.6   U1

U1 is a low power state where no packets are observed and the retimer is in a standby state.

E.3.6.1 U1 Requirements

- The retimer shall distinguish between Ping.LFPS, and U1 LFPS exit signal.
- The retimer, upon detecting an inbound LFPS signal that is not Ping.LFPS, shall initiate simultaneous U1 LFPS exit by performing the following.
    - o   It shall respond with U1_Exit LFPS handshake.
    - o   It shall forward the received LFPS signal outbound to its other link partner meeting the electrical and timing requirements defined in Section 6.9.
    - o   It shall monitor the duration of the received LFPS signal to determine if it is Warm Reset. The retimer may declare Warm Reset if the received LFPS signal is more than 2-ms.

Note that the beginning of Warm Reset will be treated by the retimer as U1 LFPS exit signal, and exit from U1 to Recovery may be achieved. However, the ensuing declaration of Warm Reset detection shall bring the retimer to Rx.Detect, if it has not been there already.

- The retimer shall enable an U2 inactivity timer upon entry to this state if the U2 inactivity timer has a non-zero timeout value.
- The retimer shall enable a 300-ms timer (tU1PingTimeout). This timer will be reset and restarted when a Ping.LFPS is received.
- The retimer shall transmit Ping.LFPS at its upstream port independently to Ping.LFPS received at its downstream port.
- The retimer shall declare device disconnect upon timeout of the tU1PingTimeout timer, and perform the following.
    - o   It shall disable its receiver termination at its upstream port.
    - o   It shall stop transmitting Ping.LFPS at its upstream port.

Note that the propagation of disconnect declaration eliminates a potential race contention between a hub downstream port and the retimer. If the hub downstream port declare device disconnect ahead of the retimer, it may enter Rx.Detect first and exit from Rx.Detect to Polling after performing far-end receiver termination detection, as the retimer has not declared the device disconnect and still has its low-impedance receiver termination presented at its upstream port.

E.3.6.2 Exit from U1

- The retimer shall transition to Recovery upon successful completion of a LFPS handshake meeting the U1 LFPS exit handshake signaling in Section 6.9.2.
- The retimer shall transition to U2 upon the timeout of the U2 inactivity timer defined in Sections 10.4.2.4 and 10.6.2.4.
- The retimer shall transition to Rx.Detect if one of the following three conditions is met.
  - Upon the 300-ms timer (tU1PingTimeout) expiration and removal of the receiver termination at its own corresponding port mirroring the far-end receiver termination.
  - Upon detecting Warm Reset.
  - Upon the 2-ms LFPS handshake timer timeout (tNoLFPSResponseTimeout) and a successful LFPS handshake meeting the U1 LFPS exit handshake signaling in Section 6.9.2 is not achieved.

E.3.7   U2

U2 is a link state where more power saving is allowed for the retimer as compared to U1, but with an increased exit latency. The operation of the retimer is the same as is defined in LTSSM with a few exceptions.

E.3.7.1 U2 Requirements

- The retimer shall perform simultaneous U2 LFPS exit handshake upon detecting U2 LFPS exit signals.
- The retimer's downstream port shall distinguish between Ping.LFPS, and U1/U2 LFPS exit signal.
- The retimer, upon detecting an inbound LFPS signal that is not Ping.LFPS, shall initiate simultaneous U2 LFPS exit by performing the following.
  - It shall respond with U2_Exit LFPS handshake.
  - It shall forward the received LFPS signal outbound to its other link partner meeting the electrical and timing requirements defined in Section 6.9.
  - It shall monitor the duration of the received LFPS signal to determine if it is Warm Reset.

Note that the beginning of Warm Reset will be treated by the retimer as U2 LFPS exit signal, and exit from U2 to Recovery may be achieved. However, the ensuing declaration of Warm Reset detection shall bring the retimer to Rx.Detect, if it has not been there already.

E.3.7.2 Exit from U2

- The retimer shall transition to Recovery upon successful completion of a LFPS handshake meeting the U2 LFPS exit signaling defined in Section 6.9.2.
- The retimer shall transition to Rx.Detect if one of the following three conditions is met.
  - Upon detection of a far-end high-impedance receiver termination ($Z_{RX-HIGH-IMP-DC-POS}$) defined in Table 6-21 and removal of the receiver termination at its own corresponding port mirroring the far-end receiver termination.
  - Upon detecting Warm Reset.
  - Upon the 2-ms LFPS handshake timer timeout (tNoLFPSResponseTimeout) and a successful LFPS handshake meeting the U2 LFPS exit handshake signaling in Section 6.9.2 is not achieved.

E.3.8   U3

U3 is a link state where a device is put into a suspend state. Significant link and retimer powers can be saved. The retimer operation is the same as is defined in LTSSM except that U3 LFPS exit is propagated.

E.3.8.1 U3 Requirements
- The retimer shall perform propagated U3 LFPS exit, rather than simultaneous U1/U2 LFPS exit. This is primarily due to the fact that a port may not be ready to respond in time, and attempt U3 LFPS exit when it is ready. The retimer shall perform the following to facilitate the propagated U3 LFPS exit.
  - o Upon detecting the U3 LFPS exit signal, the retimer shall propagate the received U3 LFPS exit signal within 100-us.
  - Note: if the retimer is implemented based on the PIPE specification, it shall not wait for the PIPE direction to start the LFPS signal transmission. Instead, while updating the Rx status to indicate the LFPS reception, it shall establish the operating condition of its LFPS transmitter by concurrently powering on its LFPS clock source and ramping up its DC operating point, and start propagating the U3 LFPS exit signal when it is ready to transmit the LFPS signal.
  - o The retimer shall start propagating the U3 LFPS exit handshake signal only if it has detected the U3 LFPS exit handshake signal.
- The retimer shall establish its eSS operating condition within 2-ms upon detecting U3 LFPS exit signal.
- Upon observing the successful completion of U3 LFPS exit handshake, if the retimer has not established its eSS operating condition, it shall continue the LFPS transmission until it is ready for eSS operation.
- Note: situation may exist that the retimer's eSS operating condition may not be established upon successful U3 LFPS exit handshake. To make sure that the maximum gap of electrical idle between the LFPS transmission and the eSS transmission does not exceed the specification defined in Section 6.9.2, the retimer shall continue the LFPS transmission until it is ready to transmit eSS signal.
- The retimer shall remain in U3 if the U3 LFPS exit handshake has failed.

E.3.8.2 Exit from U3
- The retimer shall transition to Recovery if the following two conditions are both met.
  - o Upon observing the successful completion of the U3 LFPS exit handshake meeting the U3 wakeup signaling defined in Section 6.9.2.
  - o The retimer is ready for eSS operation.
- The retimer shall remain in U3 upon failure to achieve a successful U3 LFPS exit handshake meeting the U3 wakeup signaling in Section 6.9.2.
- The retimer shall transition to Rx.Detect if one of the following three conditions is met.
  - o Upon detection of a far-end high-impedance receiver termination ($Z_{RX-HIGH-IMP-DC-POS}$) defined in Table 6-21 and removal of the receiver termination at its own corresponding port mirroring the far-end receiver termination.
  - o Upon detecting Warm Reset.

E.3.9 Recovery

The retimer operation in Recovery is the same as its operation in Polling.Active, Polling.Configuration, and Polling.Idle. There is only one behavioral difference upon entry to Recovery.

- Upon entry to Recovery, the retimer shall transmit its locally generated TS1 OS to train its link partners.

  Note: in case of exit from a low power state, the retimer may not have its receiver trained in time to forward the received TS1 OS. To avoid unmanaged electrical idle between the end of Ux LFPS exit signal and the start of TS1 OS, the retimer shall fill the gap with the locally generated TS1 OS.

- Upon completing the receiver training at both of its ports, the retimer shall switch the outbound TS1 OS to the received TS1 OS or TS2 OS.

  Note: situation exists that the retimer may have its receiver trained later than its link partner. This may result in retimer missing any TS1 OS to be forwarded. Under this situation, the retimer shall not forward any TS2 OS until its other receiver has been trained.

Recovery contains only two substates, Recovery.TSx and Recovery.Idle as shown in Figure E-6. The exit conditions in the two substates are the same as those in Polling.TSx and Polling.Idle.
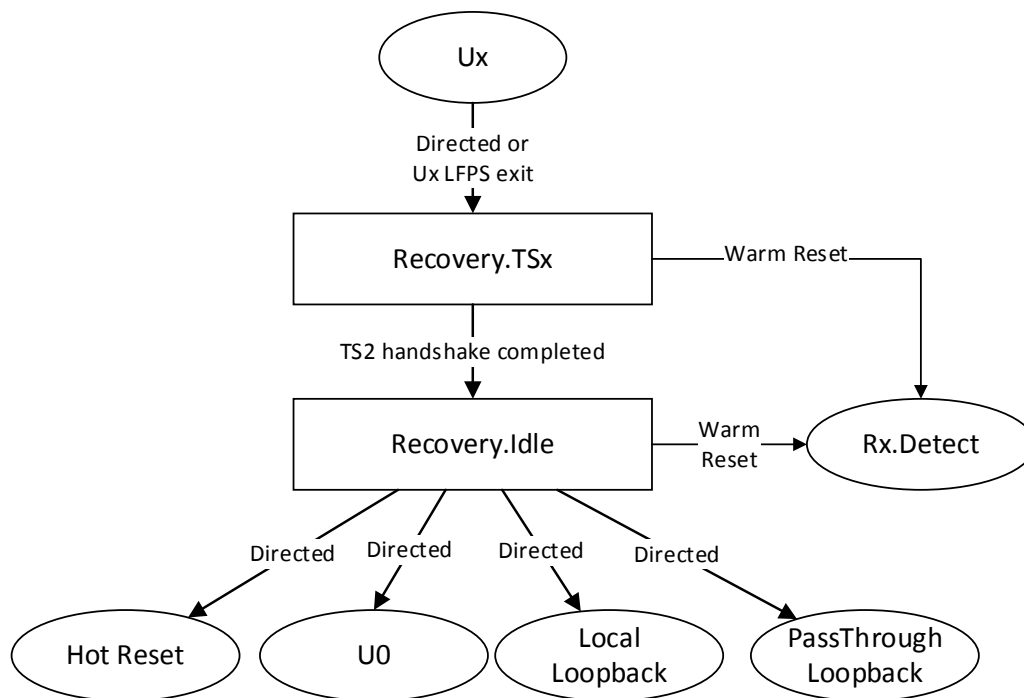

Figure E-6. Recovery Substate Machine

E.3.10 PassThrough Loopback

PassThrough Loopback is a retimer only state as defined in Section E.3.3.5. In this state, the retimer operation shall be the same as if it's U0, except no error correction is allowed. The retimer does not need to implement the two substates.

E.3.10.1 PassThrough Loopback Requirements

- The retimer shall monitor the LTSSM progression.

- The retimer shall not perform any error correction while looping through the traffic.

- The retimer in SS operation shall perform the overflow clock offset compensation based on SKP OS. Note that in loopback, the loopback master will insert enough SKP OS for the retimer to perform the overflow clock offset compensation.

- The retimer shall implement and start the tLoopbackExitTimeout timer upon detecting Loopback LFPS exit signal.

E.3.10.2 Exit from PassThrough Loopback

- The retimer shall transition to Rx.Detect if any one of the following conditions is met.
  - Upon detecting successful Loopback LFPS exit handshake.
  - Upon timeout of the tLoopbackExitTimeout timer.
  - Upon detecting Warm Reset.

E.3.11 Local Loopback

Local Loopback is the same as the Loopback state defined in LTSSM. The retimer always operates as a loopback slave.

E.3.11.1 Local Loopback Requirements

- The retimer shall configure the two ports in the following.
  - It shall configure its port receiving TS2 OS with the Loopback bit asserted in Local Loopback.
  - It shall configure its other port in Rx.Detect.

- The retimer shall implement the two substates defined in LTSSM.

- The retimer operation shall meet the requirements defined in LTSSM.

E.3.11.2 Exit from Local Loopback.Active

- The retimer shall transition to Rx.Detect upon detecting Warm Reset at its port in Rx.Detect. Note that the retimer will not declare Warm Reset at its port in Local Loopback.Active since the beginning of the Warm Reset will be treated as the start of the Loopback LFPS exit signal.

- The retimer shall transition to Local Loopback.Exit upon detection of Loopback LFPS exit signal.

E.3.11.3 Exit from Local Loopback.Exit

- The retimer shall transition to Rx.Detect if one of the following conditions is met.
  - Upon detecting Warm Reset.
  - Upon completing the Loopback LFPS exit handshake meeting Loopback LFPS exit signaling defined in Section 6.9.2.

E.3.12   Hot Reset

Hot Reset is a state where no actions need taken for the retimer. The retimer's responsibility is to monitor the progression of Hot Reset until its completion. The retimer does not need to implement two substates in Hot Reset.

E.3.12.1 Hot Reset Requirements

- The retimer shall track and monitor the progression of LTSSM.

- The retimer in SS operation shall not delete any inbound TS2 OS with the Reset bit de-asserted in order to perform the over clock offset compensation. Note that the TS2 OS with the Reset bit de-asserted is used for Hot Reset.Active exit handshake.

- The retimer in SS operation shall not delete any inbound IS to perform the overflow clock offset compensation. Note that IS used for Hot Reset.Exit exit handshake.

- The retimer shall start the tHotResetActiveTimeout timer upon entry to the state.

- The retimer shall disable and reset the tHotResetActiveTimeout timer and start the tHotResetExitTimeout timer upon detecting successful TS2 OS based Hot Reset.Active handshake.

E.3.12.2 Exit from Hot Reset

- The retimer shall transition to U0 upon observing successful Hot Reset.Exit handshake.

- The retimer shall transition to Rx.Detect if one of the following conditions is met.

    o Upon timeout of the tHotResetActiveTimeout timer and no successful Hot Reset.Active handshake is observed.

    o Upon timeout of the tHotResetExitTimeout timer and no successful Hot Reset.Exit handshake is observed.

    o Upon detecting Warm Reset.

E.4   Clock Offset Compensation

Retimers are expected to implement a reference clock in the generation of the high frequency local data clock. The reference clock may be common with the host or device with which the retimer is associated, or it may be an independent reference clock. This section describes the requirement and operation of the retimer clock offset compensation based on independent reference clock, and with the maximum number of four retimers in the link topology.

E.4.1   Gen 1 Operation

Retimer clock offset compensation for Gen 1 operation is not based on the mechanism defined in Chapter 6 using SKP OS to manage a receiving port's EB. This is mainly due to the fact that the number of SKP OS inserted at a transmitting port is budgeted only for the receiving port to manage its EB. No additional SKP OS is considered to account for retimer clock offset compensation. Therefore, a retimer needs to perform its clock offset compensation without consuming any SKP OS it has received. This section describes the means a retime may employ to achieve clock offset compensation. An example architectural concept is also provided.

E.4.1.1 Underflow Clock Offset Compensation

The underflow clock offset compensation refers to a condition that the average throughput of an inbound traffic is lower than that of an outbound traffic based on the local clock frequency of the retimer. This implies a potential underflow situation where the retimer is forwarding the data out faster than the data received. The treatment for the underflow clock offset compensation is consistent with the mechanism defined in Chapter 6 using SKP OS.

- A retimer shall insert SKP OS to perform the underflow clock offset compensation.
- A retimer shall follow SKP OS insertion rule defined in Chapter 6.
- A retimer shall implement its EB that can tolerate the worst case underflow clock offset for at least the duration of a DP with the maximum DPP size.

E.4.1.2 Overflow Clock Offset Compensation

The overflow clock offset compensation refers to a condition that the average throughput of an inbound traffic is higher than that of an outbound traffic based on the local clock frequency of the retimer. This implies a potential overflow situation where the retimer is forwarding the data out slower than the data received. Given no additional SKP OS is budgeted for a retimer to consume, the treatment for the overflow clock offset compensation is different and shall be performed in the following way.

- A retimer shall implement its EB that can tolerate at least eight consecutive DPs of the maximum DPP size under the worst case overflow clock offset.
- A retimer in Polling.Active, Polling.Configuration, Recovery.Active, Recovery.Cnfiguration, and Hot Reset shall employ TS1 OS, or TS2 OS removal to perform the overflow clock offset compensation, while still not violating the exit conditions defined by LTSSM.
- A retimer in U0 shall employ IS removal to perform the overflow clock offset compensation. A retimer shall adhere to the following rules.
  - A retimer shall maintain the scrambler synchronization with its link partner.
  - A retimer shall maintain the running disparity when the forwarded data stream is 8b/10b encoded at the transmitter.
  - There shall be no restriction regarding the number of IS removal to perform overflow clock offset compensation.
  - The IS removal shall only be employed for the overflow clock offset compensation, and a retimer shall not remove more IS than is necessary.

  Note: the preservation of IS necessary for consumption by additional retimers that may exist.

- A retimer is allowed to drop or truncate the DPP of a DP for the overflow clock offset compensation if and only if the following conditions are met.
  - It has forwarded eight consecutive DPs of the maximum DPP size.
  - Its EB has reached the overflow limit.
  - It has no IS to consume.
- A retimer shall not drop any link commands and header packets to perform the overflow clock offset compensation.

- A retimer may re-organize the SKP OS it received and re-construct them in different orders as long as the SKP OS insertion in its forwarded data stream meets the requirements defined in Chapter 6 and Chapter 7 in terms of SKP OS insertion interval and locations of SKP OS insertion.

- In case of multiple retimer coexistence, a retimer may perform the overflow clock offset compensation by deleting the SKP OS if the retimer is able to identify that those SKP OS are added by other retimers.

Note: a retimer may implement a SKP OS count to track the SKP OS insertion interval, and based on that to determine if the SKP OS is added by retimers.

Shown in Figure E-3 is a conceptual example block diagram of a retimer in SuperSpeed operation.
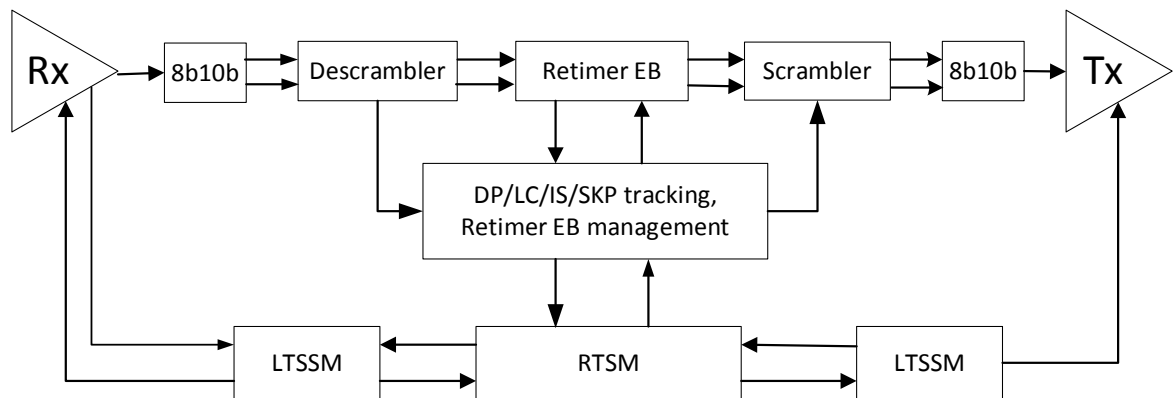

Figure E-7. Example block diagram of a retimer operating at SuperSpeed

E.4.2 Gen 2 Operation

Retimers shall perform its clock offset compensation as defined in Section 6.4.3.2.

E.5 Compliance

E.5.1 Host and Device Product Compliance

Host and device products with retimers shall meet the transmitter compliance requirements defined in section 6.7.3 and the receiver jitter tolerance requirements defined in section 6.8.5 of the base specification. During all host or device product compliance testing the retimer shall be in the normal operation state (U0).

E.5.2 Component-Level Retimer Compliance

Retimer products may also undergo component level compliance testing. The transmitter and receiver compliance requirements specified in sections 6.7.3 and 6.8.5 apply to component level compliance testing. When undergoing component level compliance testing for the transmitter, the retimer shall generate appropriate compliance patterns. When undergoing component level compliance testing for the receiver, the retimer shall be placed into loopback mode.