TEXAS INSTRUMENTS

ADS1262, ADS1263

SBAS661A – FEBRUARY 2015 – REVISED MAY 2015

ADS126x 32-Bit, Precision, 38-kSPS, Analog-to-Digital Converter (ADC) with Programmable Gain Amplifier (PGA) and Voltage Reference

1 Features

- Precision, 32-bit, ΔΣ ADC
- Auxiliary 24-Bit ΔΣ ADC (ADS1263)
- Data Rates: 2.5 SPS to 38400 SPS
- Differential Input, CMOS PGA
- 11 Multifunction Analog Inputs
- High-Accuracy Architecture
  - Offset Drift: 1 nV/°C
  - Gain Drift: 0.5 ppm/°C
  - Noise: 7 nVrms (2.5 SPS, Gain = 32)
  - Linearity: 3 ppm
- 2.5-V Internal Voltage Reference
  - Temperature Drift: 2 ppm/°C
- 50-Hz and 60-Hz Rejection
- Single-Cycle Settled Conversions
- Dual Sensor Excitation Current Sources
- Internal Fault Monitors
- Internal ADC Test Signal
- 8 General-Purpose Input/Outputs

2 Applications

- High-Resolution PLCs
- Temperature, Pressure Measurement
- Weigh Scales and Strain-Gauge Digitizers
- Panel Meters, Chart Recorders
- Analytical Instrumentation

3 Description

The ADS1262 and ADS1263 are low-noise, low-drift, 38.4-kSPS, delta-sigma (ΔΣ), ADCs with an integrated PGA, reference, and internal fault monitors. The ADS1263 integrates an auxiliary, 24-bit, ΔΣ ADC intended for background measurements. The sensor-ready ADCs provide complete, high-accuracy, one-chip measurement solutions for the most-demanding sensor applications, including weigh scales, strain-gauge sensors, thermocouples, and resistance temperature devices (RTD).

The ADCs are comprised of a low-noise, CMOS PGA (gains 1 to 32), a ΔΣ modulator, followed by a programmable digital filter. The flexible analog front-end (AFE) incorporates two sensor-excitation current sources suitable for direct RTD measurement.

A single-cycle settling digital filter maximizes multiple-input conversion throughput, while providing 130-dB rejection of 50-Hz and 60-Hz line cycle interference.

The ADS1262 and ADS1263 are pin and functional compatible. These devices are available in a 28-pin TSSOP package and are fully specified over the –40°C to +125°C temperature range.

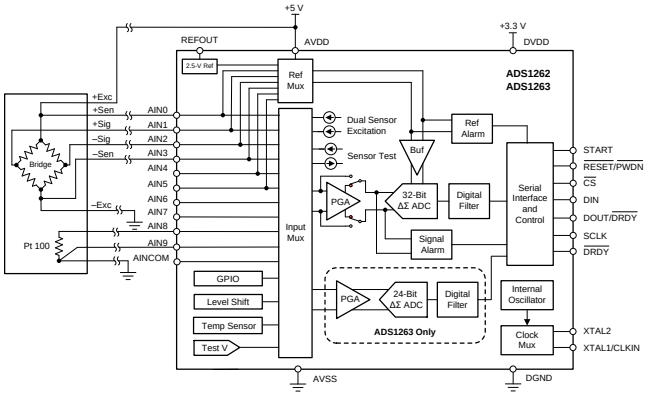
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS1262	TSSOP (28)	9.70 mm × 4.40 mm
ADS1263[2]		

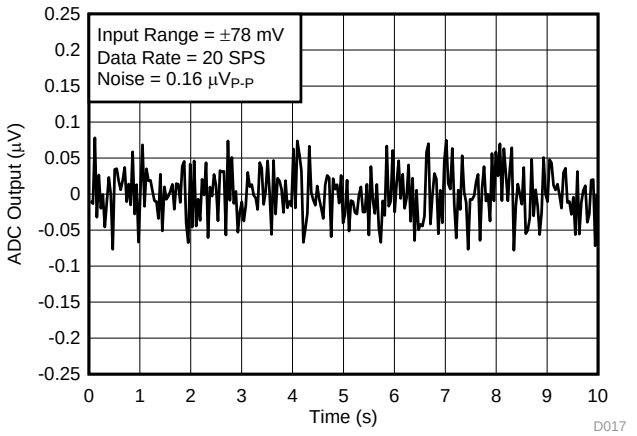
(1) For all available packages, see the package option addendum at the end of the data sheet.

(2) ADS1263 is product preview. Contact TI sales for more information.

Temperature Compensated Bridge Measurement



ADC Conversion Noise



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

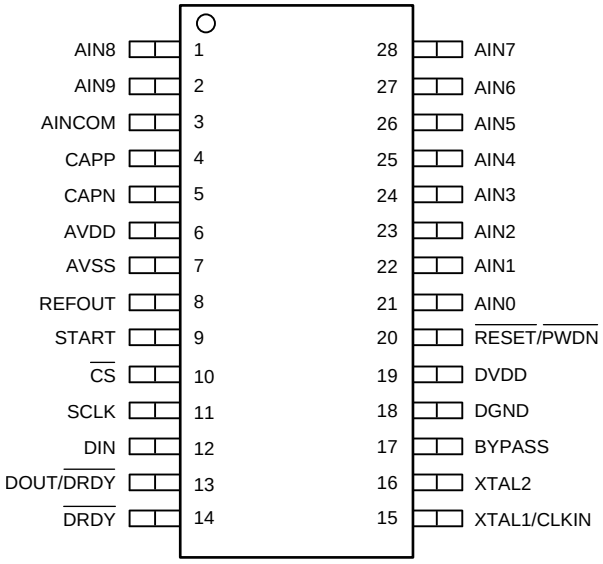
Changes from Original (February 2015) to Revision A	Page
• Changed ADS1262 from product preview to production data	1

5 Device Comparison

PRODUCT	INPUTS	AUXILIARY 24-BIT ADC
ADS1262	11	No
ADS1263	11	Yes

6 Pin Configuration and Functions

PW Package
28-Pin TSSOP
Top View (Not To Scale)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	AIN8	Analog input/output	Analog input 8, IDAC1, IDAC2, GPIO5
2	AIN9	Analog input/output	Analog input 9, IDAC1, IDAC2, GPIO6
3	AINCOM	Analog input/output	Analog input common, IDAC1, IDAC2, GPIO7, VBIAS
4	CAPP	Analog output	PGA output P: connect a 4.7-nF C0G dielectric capacitor from CAPP to CAPN
5	CAPN	Analog output	PGA output N: connect a 4.7-nF C0G dielectric capacitor from CAPP to CAPN
6	AVDD	Analog	Positive analog power supply
7	AVSS	Analog	Negative analog power supply
8	REFOUT	Analog Output	Internal reference voltage output, connect 1-µF capacitor to AVSS
9	START	Digital Input	Start conversion control
10	$\overline{CS}$	Digital Input	Serial interface chip select (active low)
11	SCLK	Digital Input	Serial interface shift clock
12	DIN	Digital Input	Serial interface data input
13	DOUT/$\overline{DRDY}$	Digital output	Serial interface data output and data ready indicator (active low)
14	$\overline{DRDY}$	Digital output	Data ready indicator (active low)
15	XTAL1/CLKIN	Digital Input	1) Internal oscillator: Connect to DGND 2) External clock: Connect clock input 3) Crystal oscillator: Connect to crystal and crystal load capacitor
16	XTAL2	Digital Input	1) Internal oscillator: No connection (float) 2) External clock: No connection (float) 3) Crystal oscillator: Connect to crystal and crystal load capacitor
17	BYPASS	Analog Output	2-V subregulator external bypass; connect 1-µF capacitor to DGND
18	DGND	Digital	Digital ground
19	DVDD	Digital	Digital power supply
20	$\overline{RESET}$/$\overline{PWDN}$	Digital input	Reset (active low); hold low to power down the ADC
21	AIN0	Analog input/output	Analog input 0, REFP1, IDAC1, IDAC2
22	AIN1	Analog input/output	Analog input 1, REFN1, IDAC1, IDAC2
23	AIN2	Analog input/output	Analog input 2 ,REFP2, IDAC1, IDAC2
24	AIN3	Analog input/output	Analog input 3, REFN2, IDAC1, IDAC2, GPIO0
25	AIN4	Analog input/output	Analog input 4, REFP3, IDAC1, IDAC2, GPIO1
26	AIN5	Analog input/output	Analog input 5, REFN3, IDAC1, IDAC2, GPIO2
27	AIN6	Analog input/output	Analog input 6, IDAC1, IDAC2, GPIO3, TDACP
28	AIN7	Analog input/output	Analog input 7, IDAC1, IDAC2, GPIO4, TDACN

7 Specifications

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage	AVDD to AVSS	–0.3	+7	V
	AVSS to DGND	–3	+0.3	V
	DVDD to DGND	–0.3	+7	V
	Analog input	V_{AVSS} – 0.3	V_{AVDD} + 0.3	V
	Digital input	V_{DGND} – 0.3	V_{DVDD} + 0.3	V
Current	Input current(2)	–10	+10	mA
Temperature	Junction, T_J	–50	+150	°C
	Storage, T_{stg}	-60	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power supply rails. Limit the input current to 10 mA or less if the analog input voltage exceeds V_{AVDD} + 0.3 V or is below V_{AVSS} – 0.3 V, or if the digital input voltage exceeds V_{DVDD} + 0.3 V or is below V_{DGND} – 0.3 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	V_{AVDD} to V_{AVSS}	4.75	5	5.25	V
		V_{AVSS} to V_{DGND}	–2.6		0	V
	Digital power supply	V_{DVDD} to V_{DGND}	2.7		5.25	V
ANALOG INPUTS ADC1						
FSR	Full-scale differential input voltage range(1)		$-V_{REF}$ / Gain		$+V_{REF}$ / Gain	V
V_{INP},V_{INN}	Absolute input voltage (2)	PGA mode	See Equation 11			V
		PGA bypass	V_{AVSS} - 0.1		V_{AVDD} + 0.1	V
VOLTAGE REFERENCE INPUTS						
V_{REF}	Differential reference voltage	$V_{REF} = V_{REFP} - V_{REFN}$	0.9		$V_{AVDD} – V_{AVSS}$ + 0.2	V
V_{REFN}	Negative reference voltage		V_{AVSS} – 0.1		V_{REFP} - 0.9	V
V_{REFP}	Positive reference voltage		V_{REFN} + 0.9		V_{AVDD} + 0.1	V
CLOCK INPUT						
f_{CLK}	External clock frequency		1	7.3728	8	MHz
	External clock duty cycle		30%		70%	
	External crystal frequency		1	7.3728	8	MHz
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)						
	Input voltage		V_{AVSS}		V_{AVDD}	V
DIGITAL INPUTS (other than GPIO)						
	Input voltage		V_{DGND}		V_{DVDD}	V
TEMPERATURE						
T_A	Operating ambient temperature		–40		+125	°C

(1) FSR is the Ideal full-scale differential input voltage range, excluding noise, offset and gain errors. Maximum available FSR is achieved with V_{REF} = 5 V and the PGA bypassed. If the PGA is enabled and V_{REF} = 5 V, the maximum available FSR is limited by the PGA input range.
(2) V_{INP}, V_{INN} = Absolute Input Voltage. V_{IN} = Differential Input Voltage = $V_{INP} – V_{INN}$.

7.4 Thermal Information

THERMAL METRIC(1)		ADS126x PW (TSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Minimum and maximum specifications applied from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, PGA mode, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC1 INPUTS							
	Absolute input current	Gain = 32			2		nA
		PGA bypass			150		nA
	Differential input current	Gain = 32			0.1		nA
		PGA bypass, V_{IN} = 5 V			150		nA
	Differential input impedance	PGA mode			1		GΩ
		PGA bypass			40		MΩ
	Channel-to-channel crosstalk	DC, $V_{AVSS} \le V_{INX} \le V_{AVDD}$			0.5		µV/V
ADC1 PERFORMANCE							
	PGA gain				1, 2, 4, 8, 16, 32		V/V
	Resolution			32			Bits
DR	Data rate			2.5		38400	SPS
	Noise performance				See Table 1		
INL	Integral nonlinearity	Gain = 1 to 32, PGA bypass			3	12	ppm
V_{OS}	Offset voltage	T_A = 25°C	Chop mode off		350 / Gain	800 / Gain	µV
			Chop mode on		±0.1 / Gain	±0.5 / Gain	µV
		After calibration(1)			Noise / 4		
	Offset voltage drift	Chop mode off			30 / Gain + 10	100 / Gain + 50	nV/°C
		Chop mode on			1	5	nV/°C
GE	Gain error	T_A = 25°C, gain = 1 to 32			±50	±300	ppm
		After calibration(1)			Noise / 4		
	Gain drift	Gain = 1 to 32, and PGA bypass			0.5	4	ppm/°C
NMRR	Normal-mode rejection ratio(2)				see Table 9		
CMRR	Common-mode rejection ratio(3)	f_{IN} = 60 Hz, f_{DATA} = 20 SPS			130		dB
		f_{IN} = 60 Hz, f_{DATA} = 400 SPS		100	120		dB
PSRR	Power-supply rejection ratio(4)	AVDD and AVSS		80	90		dB
		DVDD		80	120		dB
EXTERNAL VOLTAGE REFERENCE INPUTS							
	Reference input current(5)				150		nA
	Input current vs voltage	V_{REF} = 2 V to 4.8 V			10		nA/V
	Input current drift				0.1		nA/°C
	Input impedance	Differential			50		MΩ
	Low reference monitor	Threshold			0.4	0.6	V
INTERNAL VOLTAGE REFERENCE							
	Reference voltage				2.5		V
	Initial accuracy	T_A = 25°C			±0.1%	±0.2%	
	Reference voltage drift	T_A = 0°C to +85°C			2	6	ppm/°C
		T_A = –40°C to +105°C			4	12	ppm/°C
	Thermal hysteresis	First 0°C to 85°C cycle			50		ppm
	Output current			-10		10	mA
	Load regulation				40		µV/mA
	Start-up time	Settling time to ±0.001% final value			50		ms

(1) Offset and gain calibration accuracy is on the order of the ADC conversion noise / 4. The conversion noise depends on the data rate and PGA gain.
(2) Normal-mode rejection ratio is dependent on the digital filter setting.
(3) Common-mode rejection ratio is specified at date rate 20 SPS and 400 SPS.
(4) Power-supply rejection ratio is specified at dc.
(5) Specified with $V_{AVSS} \le V_{REFN}$ and $V_{REFP} \le V_{AVDD}$. For reference input voltage exceeding V_{AVDD} or V_{AVSS}, the reference input current = 10 nA/ mV.

Electrical Characteristics (continued)

Minimum and maximum specifications applied from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, PGA mode, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE SENSOR						
	Voltage	T_A = 25°C		122.4		mV
	Temperature coefficient			420		µV/°C
CURRENT SOURCES (IDAC1, IDAC2)						
	Currents			50, 100, 250, 500, 750, 1000, 1500, 2000, 2500, 3000		µA
	Compliance range	All currents	V_{AVSS}		V_{AVDD} – 1.1	V
	Absolute error	All currents		±0.7%	±4%	
	Match error	IDAC1 current = IDAC2 current		±0.1%	±1%	
		IDAC1 current ≠ IDAC2 current		±1%		
	Temperature drift	Absolute		50		ppm/°C
		Match		5	20	ppm/°C
LEVEL-SHIFT VOLTAGE						
	Voltage			(V_{AVDD} + V_{AVSS}) / 2		V
	Output impedance			100		Ω
SENSOR BIAS						
	Currents			±0.5, ±2, ±10, ±50, ±200		µA
	Pull-up/pull-down resistor			10		MΩ
TEST DAC (TDAC)						
	DAC reference voltage			V_{AVDD} – V_{AVSS}		V
	Differential output voltage	18 binary weighted settings	-4		+4	V
	Absolute output voltage	To V_{AVSS}	0.5		4.5	V
	Accuracy			±0.1%	±1.5%	
	Output impedance			See Table 10		
PGA OVER-RANGE MONITOR						
	Differential alarm	Threshold		±105%		FSR
	Differential alarm accuracy			±1%	±3%	
	Absolute alarm thresholds	Low threshold		V_{AVSS} + 0.2		V
		High threshold		V_{AVDD} – 0.2		V
ADC2 (ADS1263 Only)						
	Resolution			24		Bits
	PGA gain			1, 2, 4, 8, 16, 32, 64, 128		V/V
DR	Data rate			10, 100, 400, 800		SPS
ADC CLOCK						
	Internal oscillator frequency			7.3728		MHz
	Internal oscillator accuracy			±0.5%	±2%	
	External crystal startup time	See Table 20 for recommended crystals		20		ms
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)(6)						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 · V_{AVDD}			V
V_{OL}	Low-level output voltage	I_{OL} = –1 mA			0.2 · V_{AVDD}	V
V_{IH}	High-level input voltage		0.7 · V_{AVDD}		V_{AVDD}	V
V_{IL}	Low-level input voltage		V_{AVSS}		0.3 · V_{AVDD}	V
	Input hysteresis			0.5		V

(6) GPIO input and output voltages are referenced to V_{AVSS}.

Electrical Characteristics (continued)

Minimum and maximum specifications applied from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, PGA mode, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT (Other Than GPIO)						
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 · V_{DVDD}			V
		I_{OH} = 8 mA		0.75 · V_{DVDD}		V
V_{OL}	Low-level output voltage	I_{OL} = –1 mA			0.2 · V_{DVDD}	V
		I_{OL} = –8 mA		0.2 · V_{DVDD}		V
V_{IH}	High-level input voltage		0.7 · V_{DVDD}		V_{DVDD}	V
V_{IL}	Low-level input voltage		V_{DGND}		0.3 · V_{DVDD}	V
	Input hysteresis			0.1		V
	Input leakage				±10	µA
POWER SUPPLY						
	Analog supply current	Active mode, voltage reference off		4		mA
		Active mode, voltage reference on		4.2	6.5	mA
		Power-down mode		2	15	µA
I_{DVDD}	Digital supply current	Active mode		1	1.25	mA
		Power-down mode(7)		25	50	µA
P_D	Power dissipation	Active mode, voltage reference on		24	37	mW
		Power-down mode		90	240	µW

(7) External CLK input stopped. All other digital inputs maintained at V_{DVDD} or V_{DGND}.

7.6 Timing Requirements: Serial Interface

		MIN	MAX	UNIT
$t_{d(CSSC)}$	$\overline{CS}$↓ before first SCLK↑: delay time(1)	50		ns
$t_{d(DRSC)}$	$\overline{DRDY}$↓ or $\overline{DRDY}$/DOUT↓before first SCLK↑: delay time	0		ns
$t_{su(DI)}$	Valid DIN to SCLK↓: setup time	35		ns
$t_{h(DI)}$	SCLK↓to valid DIN: hold time	25		ns
$t_{c(SC)}$	SCLK period(2)	125	10^6	ns
$t_{w(SCH)}$,$t_{w(SCL)}$	SCLK high pulse width or SCLK low pulse width	40		ns
$t_{d(SCCS)}$	Last SCLK↓ to CS↑: delay time	40		ns
$t_{w(CSH)}$	$\overline{CS}$ high pulse width	30		ns

(1) $\overline{CS}$ can be tied low.
(2) If serial interface timeout mode enabled, minimum SCLK frequency = 1 kHz. If serial interface timeout mode disabled (default), there is no minimum SCLK frequency.

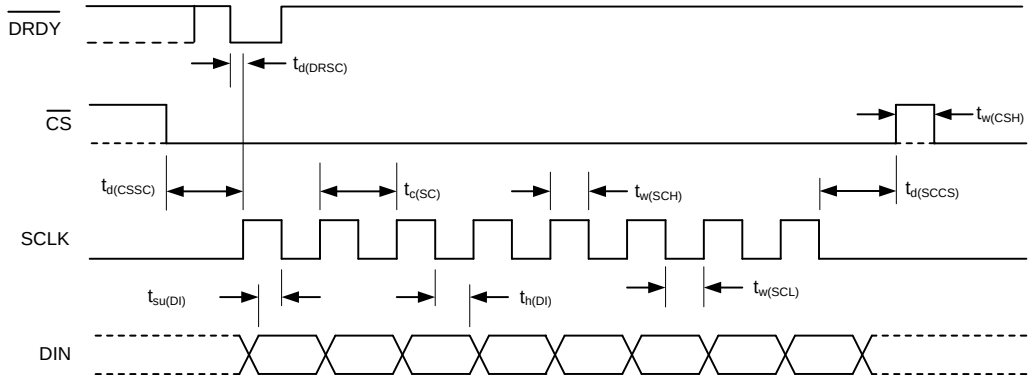
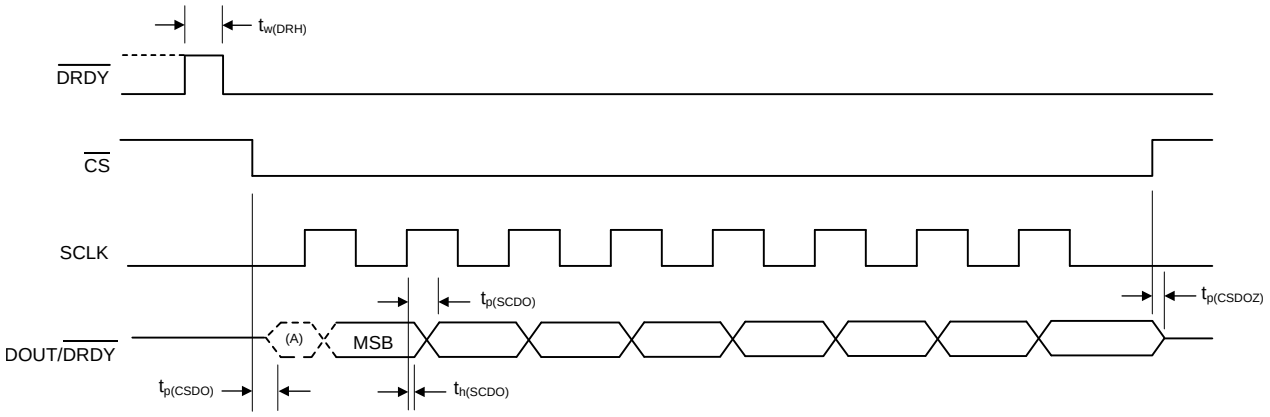


Figure 1. Serial Interface Timing Requirements

7.7 Switching Characteristics: Serial Interface

over operating the ambient temperature range and DVDD = 2.7 V to 5.25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(DRH)}$	$\overline{DRDY}$ high pulse width			16		$1/f_{CLK}$
$t_{p(CSDO)}$	$\overline{CS}\downarrow$ to DOUT/$\overline{DRDY}$ driven: propagation delay time	DOUT/$\overline{DRDY}$ load: 20 pF || 100 kΩ to DGND	0		40	ns
$t_{p(SCDO)}$	SCLK↑ to valid DOUT/$\overline{DRDY}$: propagation delay time	DOUT/$\overline{DRDY}$ load: 20 pF || 100 kΩ to DGND			60	ns
$t_{h(SCDO)}$	SCLK↑ to invalid DOUT/$\overline{DRDY}$: hold time	DOUT/$\overline{DRDY}$ load: 20 pF || 100 kΩ to DGND	0			ns
$t_{p(CSDOZ)}$	$\overline{CS}\uparrow$ to DOUT/$\overline{DRDY}$ high impedance: propagation delay time	DOUT/$\overline{DRDY}$ load: 20 pF || 100 kΩ to DGND			40	ns



(A): If new ADC data is ready since the last operation, DOUT/$\overline{DRDY}$ is logic low during this interval. Otherwise, DOUT/$\overline{DRDY}$ can be logic high or low depending on the previous state of the pin.

Figure 2. Serial Interface Switching Characteristics

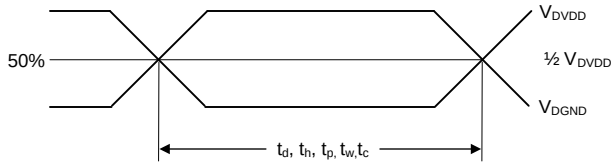
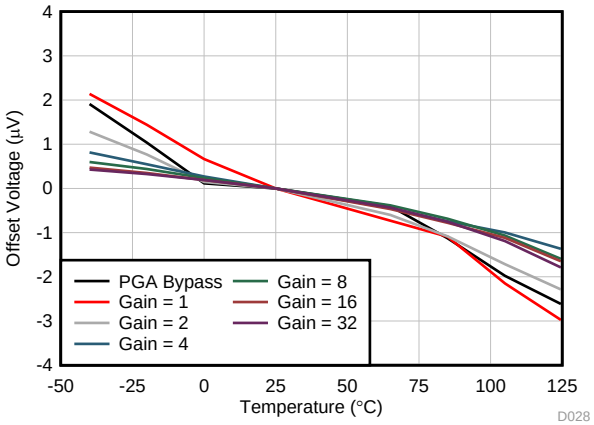


Figure 3. Timing Reference

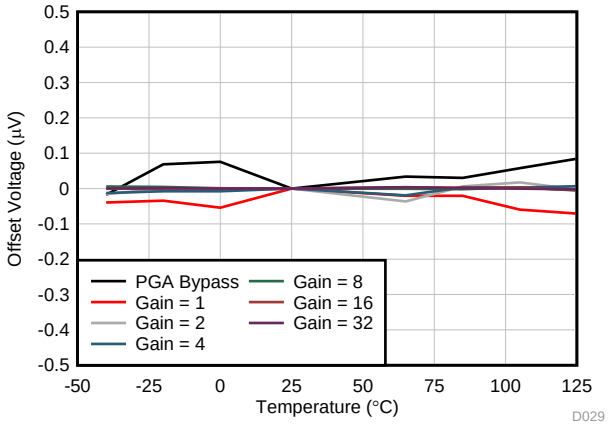
7.8 Typical Characteristics

Typical ADC1 characteristics at T_A = 25°C. V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and PGA gain = 1 (unless otherwise noted)



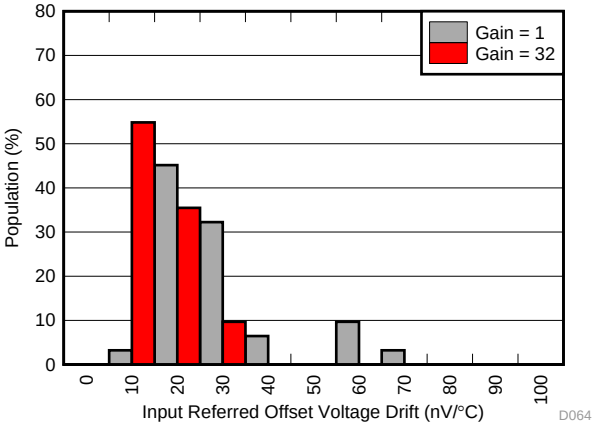
After offset calibration, shorted inputs

Figure 4. Offset Voltage vs Temperature



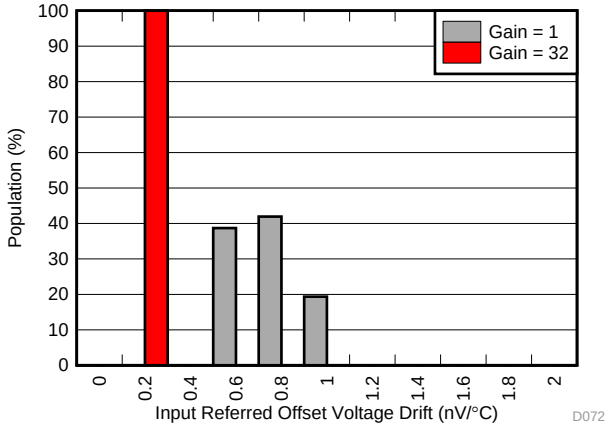
Chop mode on, after offset calibration, shorted inputs

Figure 5. Offset Voltage vs Temperature



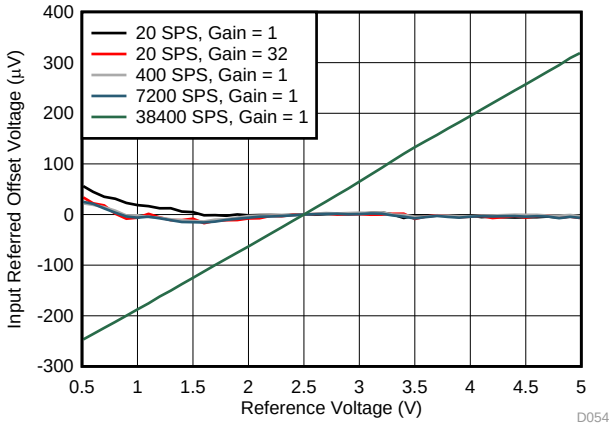
Shorted inputs

Figure 6. Offset Voltage vs Temperature Distribution



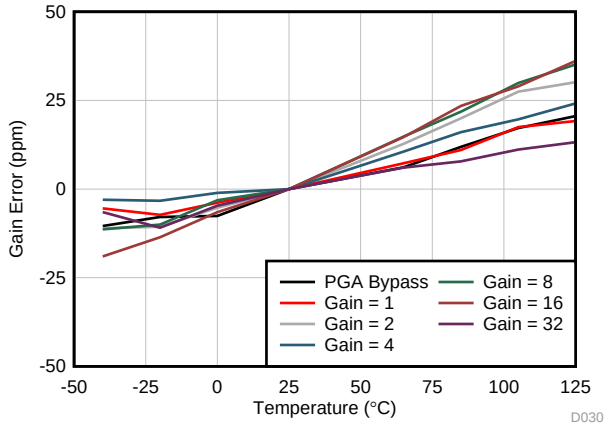
Chop mode on, shorted inputs

Figure 7. Offset Voltage vs Temperature Distribution



Shorted inputs

Figure 8. Offset Voltage vs Reference Voltage



After gain calibration

Figure 9. Gain Error vs Temperature

Typical Characteristics (continued)

Typical ADC1 characteristics at T_A = 25°C. V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and PGA gain = 1 (unless otherwise noted)

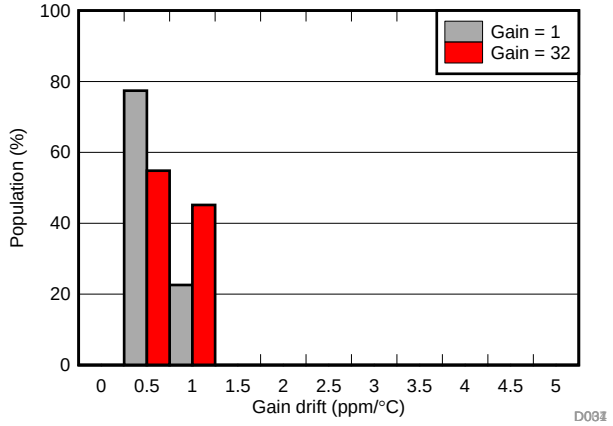


Figure 10. Gain vs Temperature Distribution

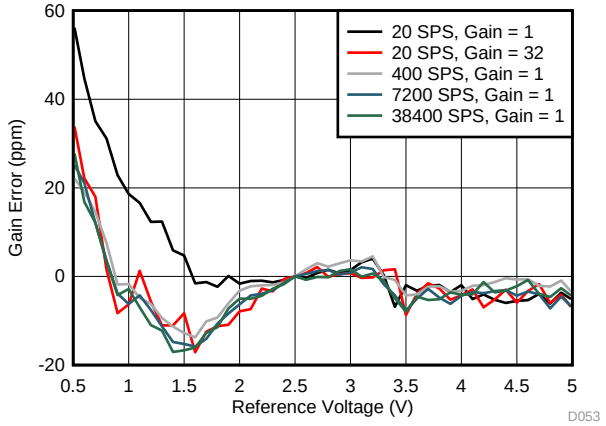


Figure 11. Gain Error vs Reference Voltage

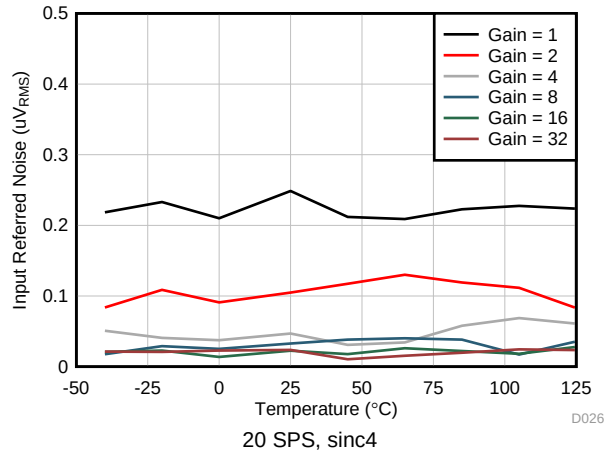


Figure 12. Noise vs Temperature

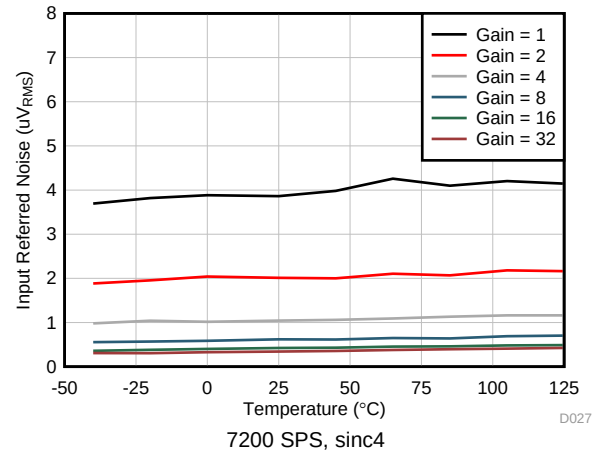


Figure 13. Noise vs Temperature

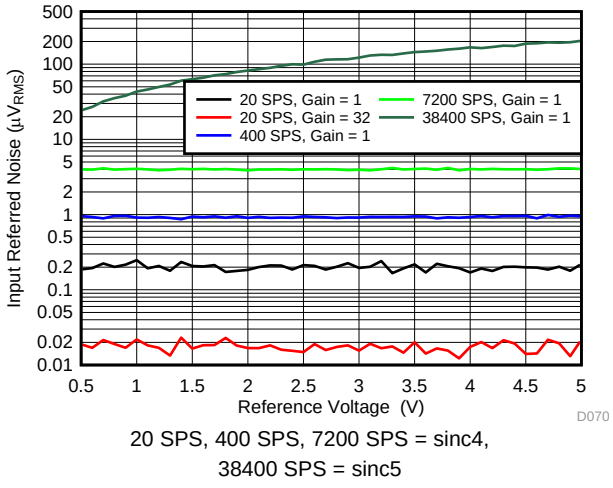


Figure 14. Noise vs Reference Voltage

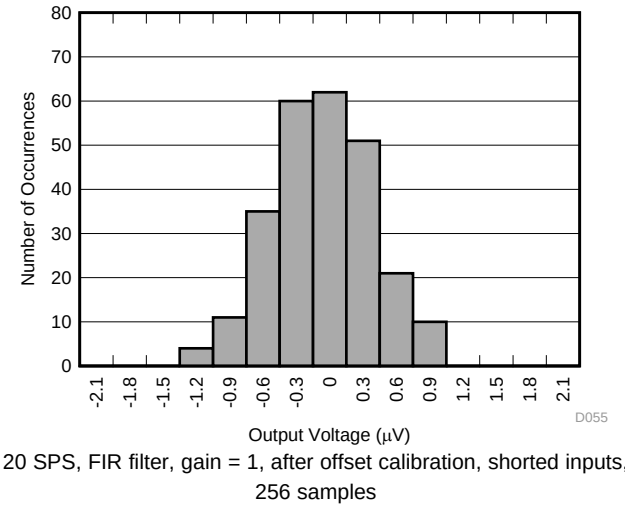
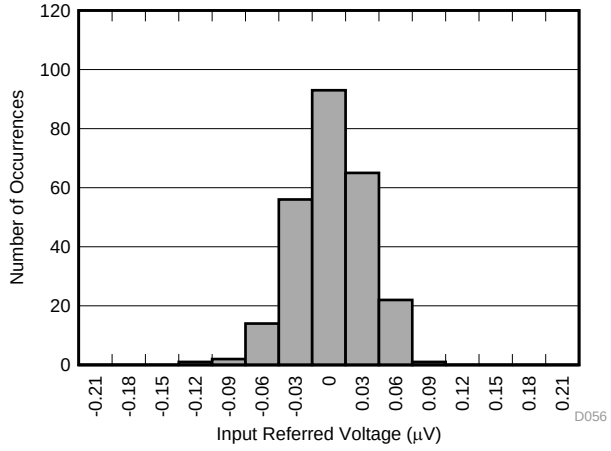


Figure 15. Output Reading Distribution

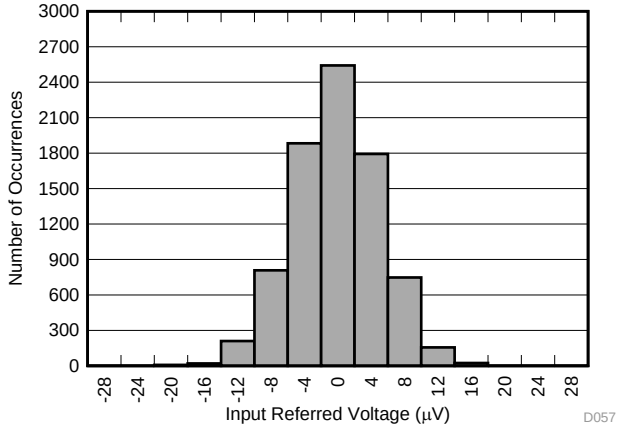
Typical Characteristics (continued)

Typical ADC1 characteristics at T_A = 25°C. V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and PGA gain = 1 (unless otherwise noted)



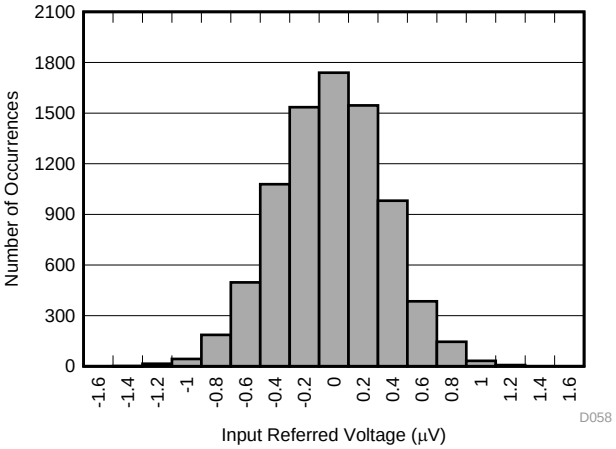
20 SPS, FIR filter, Gain = 32, after offset calibration, shorted inputs, 256 samples

Figure 16. Output Reading Distribution



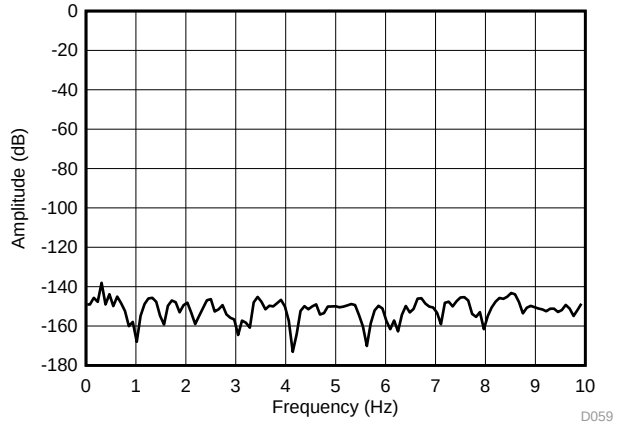
7200 SPS, sinc4 filter, Gain = 1, after offset calibration, shorted inputs, 8192 samples

Figure 17. Output Reading Distribution



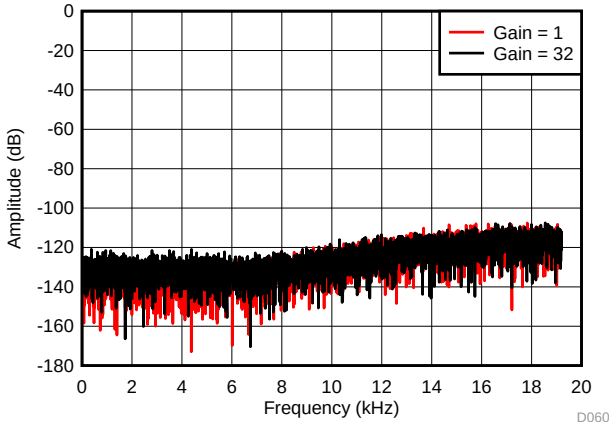
7200 SPS, sinc4 filter, Gain = 32, after offset calibration, shorted inputs, 8192 samples

Figure 18. Output Reading Distribution



20 SPS, Gain = 1, 256 points

Figure 19. Output Spectrum



38400 SPS, 8192 points

Figure 20. Output Spectrum

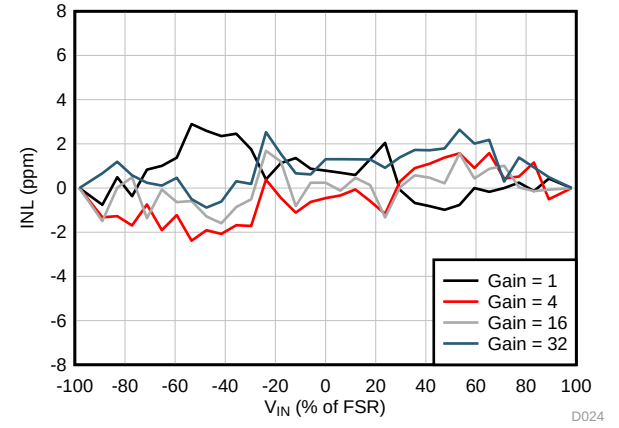


Figure 21. INL vs V_{IN}

Typical Characteristics (continued)

Typical ADC1 characteristics at T_A = 25°C. V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and PGA gain = 1 (unless otherwise noted)

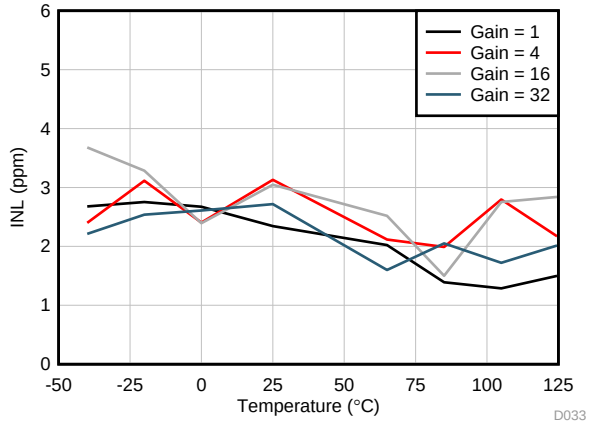


Figure 22. INL vs Temperature

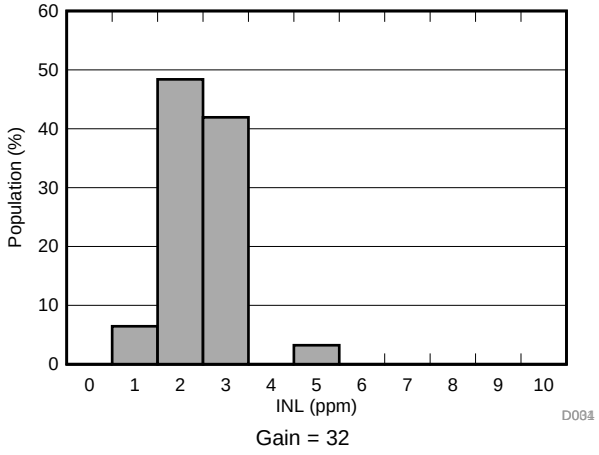


Figure 23. INL Distribution

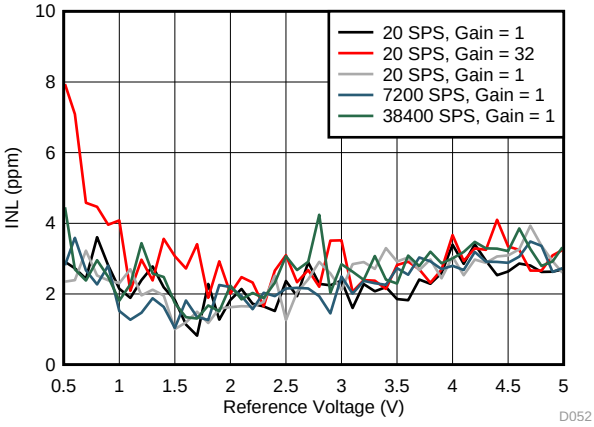


Figure 24. INL vs Reference Voltage

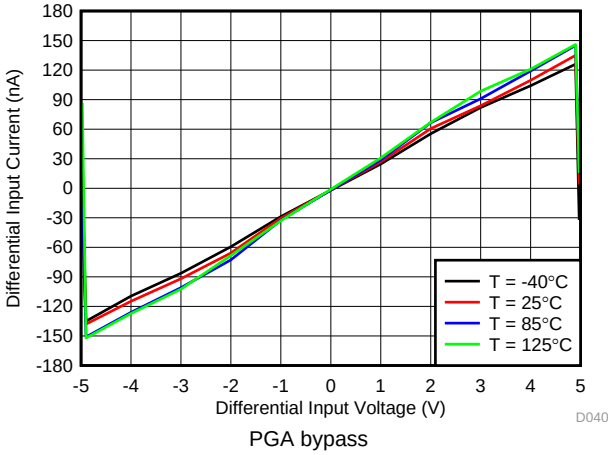


Figure 25. Differential Input Current vs Differential Input Voltage

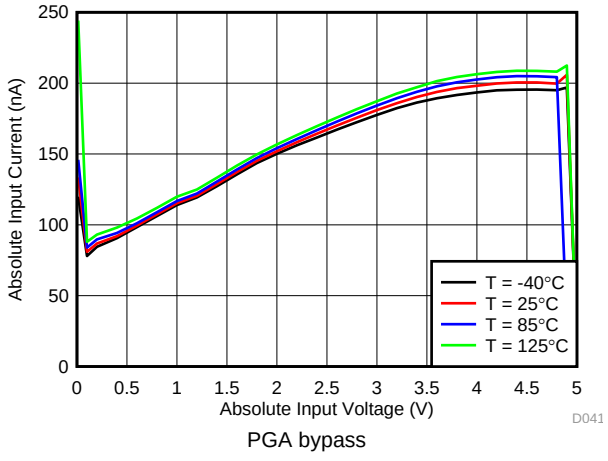


Figure 26. Absolute Input Current vs Absolute Input Voltage

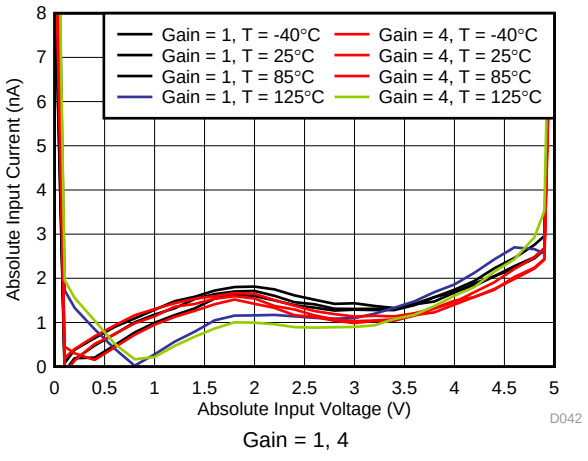
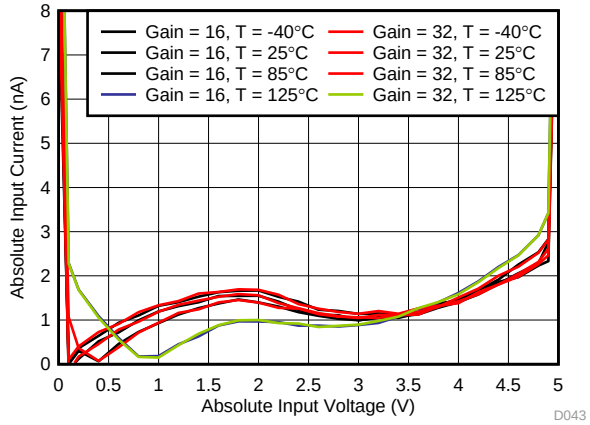


Figure 27. Absolute Input Current vs Absolute Input Voltage

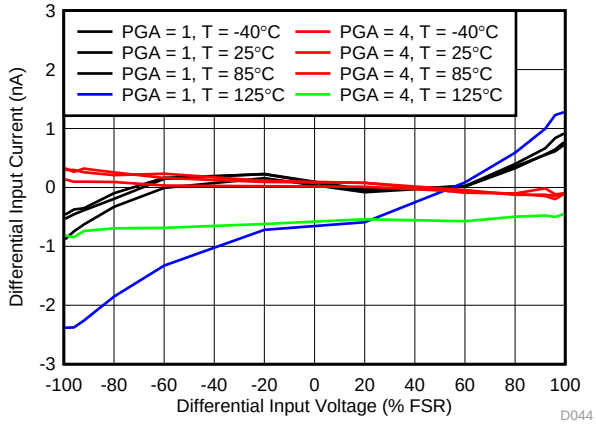
Typical Characteristics (continued)

Typical ADC1 characteristics at T_A = 25°C. V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and PGA gain = 1 (unless otherwise noted)



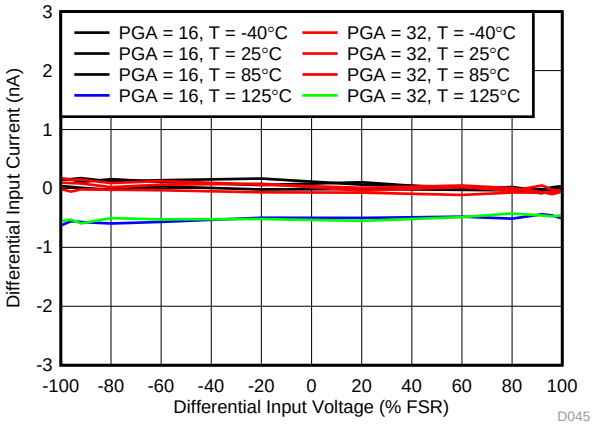
Gain = 16, 32

Figure 28. Absolute Input Current vs Absolute Input Voltage



Gain = 1, 4

Figure 29. Differential Input Current vs Differential Input Voltage



Gain = 16, 32

Figure 30. Differential Input Current vs Differential Input Voltage

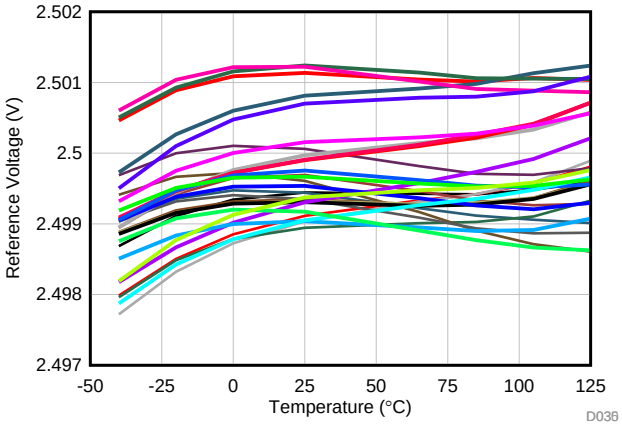


Figure 31. Internal Voltage Reference vs Temperature

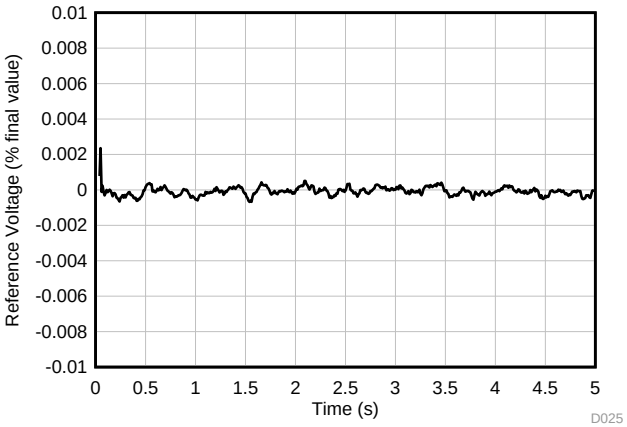
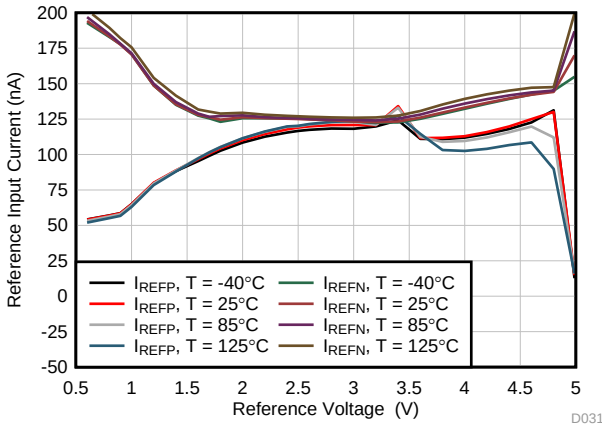


Figure 32. Voltage Reference Startup Time



I_{REFP} measured with $V_{REFN} = V_{AVSS}$, I_{REFN} measured with $V_{REFP} = V_{AVDD}$

Figure 33. Reference Input Current vs Reference Input Voltage

Typical Characteristics (continued)

Typical ADC1 characteristics at T_A = 25°C. V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and PGA gain = 1 (unless otherwise noted)

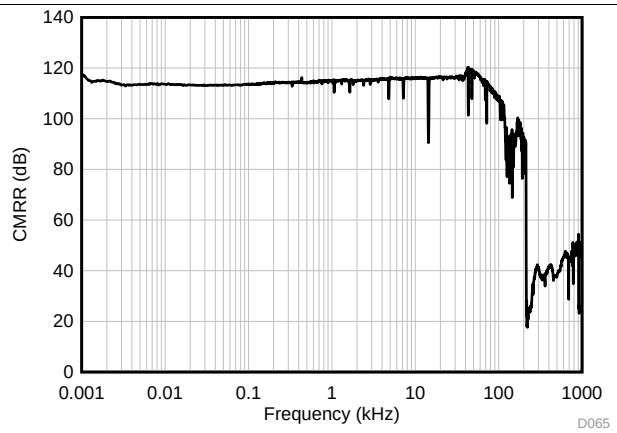


Figure 34. CMRR vs Frequency

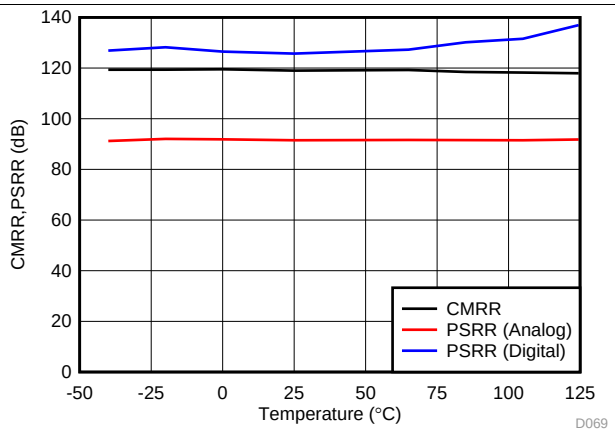
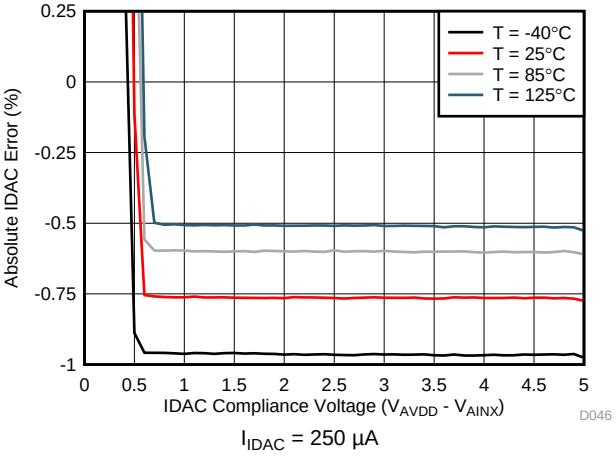
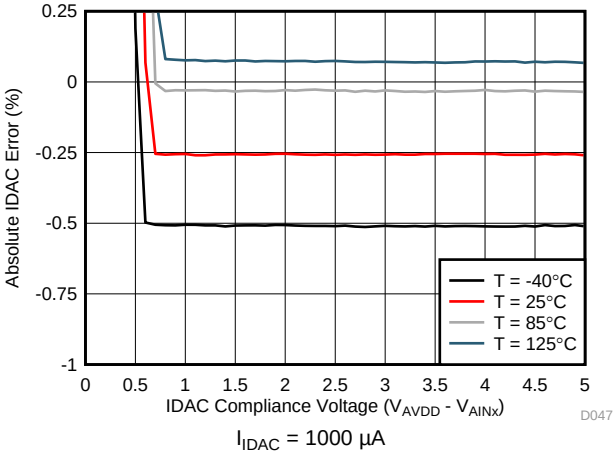


Figure 35. CMRR, PSRR vs Temperature



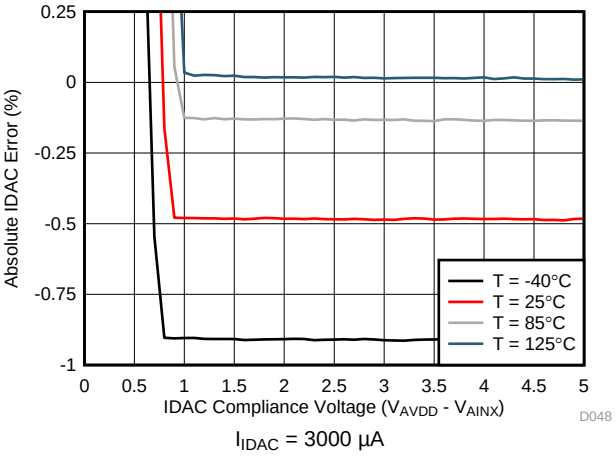
I_{IDAC} = 250 µA

Figure 36. IDAC Error vs Compliance Voltage



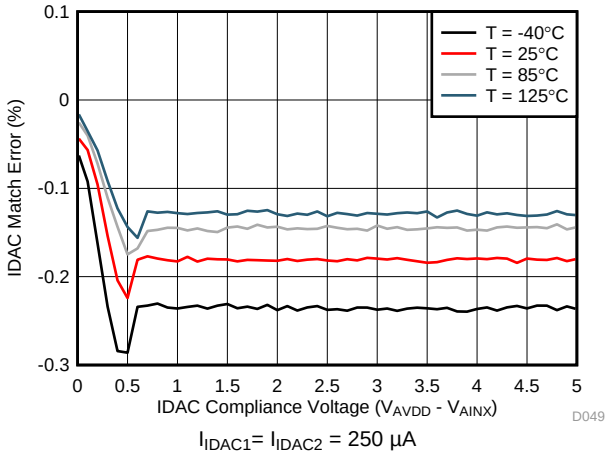
I_{IDAC} = 1000 µA

Figure 37. IDAC Error vs Compliance Voltage



I_{IDAC} = 3000 µA

Figure 38. IDAC Error vs Compliance Voltage



I_{IDAC1}= I_{IDAC2} = 250 µA

Figure 39. IDAC Current Error vs Compliance Voltage

Typical Characteristics (continued)

Typical ADC1 characteristics at T_A = 25°C. V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and PGA gain = 1 (unless otherwise noted)

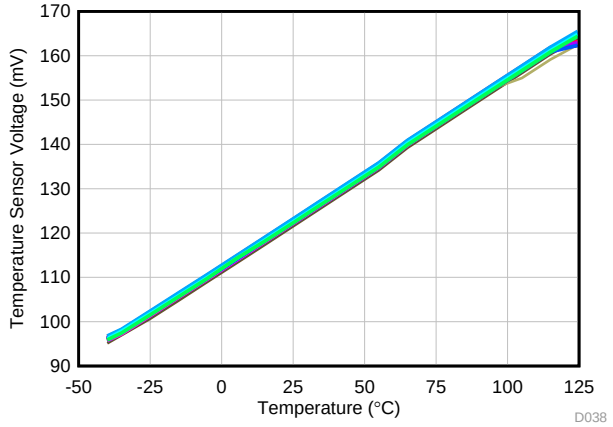


Figure 40. Temperature Sensor Voltage vs Temperature

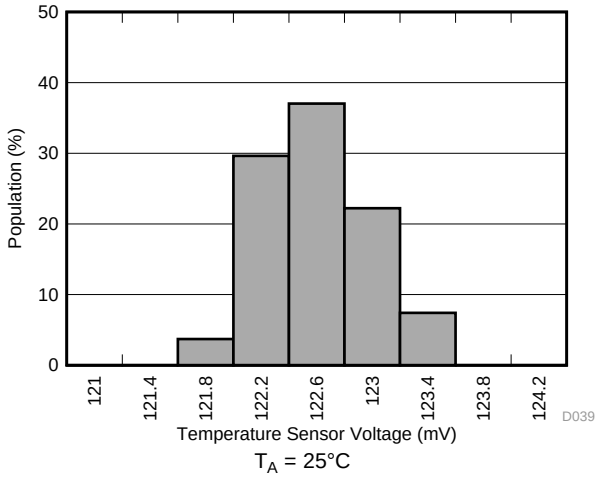


Figure 41. Temperature Sensor Voltage Distribution

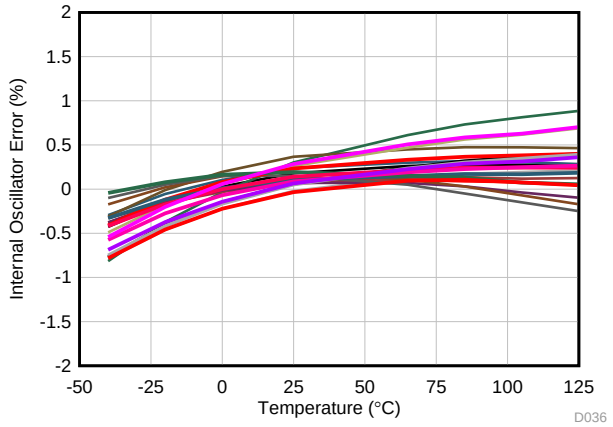


Figure 42. Internal Oscillator Frequency vs Temperature

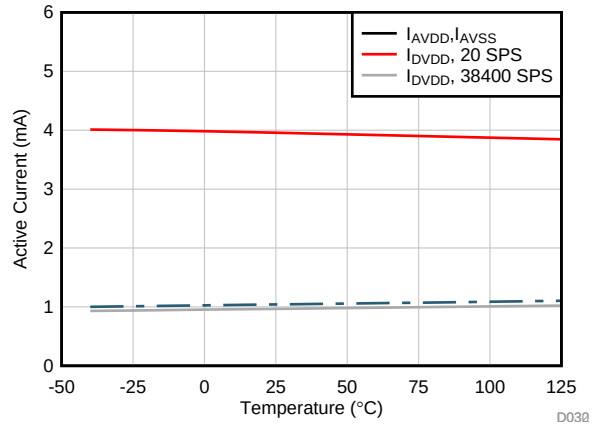


Figure 43. Operating Current vs Temperature

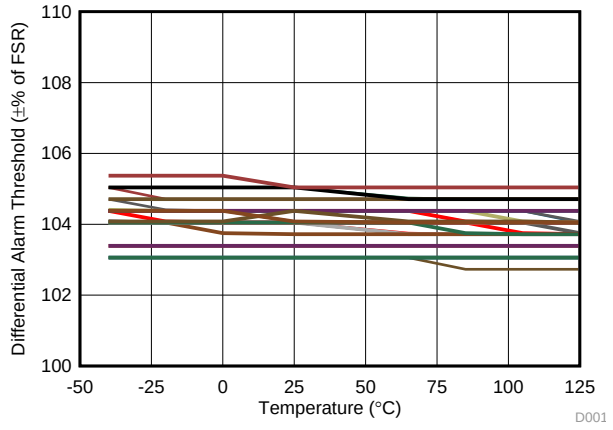


Figure 44. PGA Differential Over-range Alarm Threshold vs Temperature

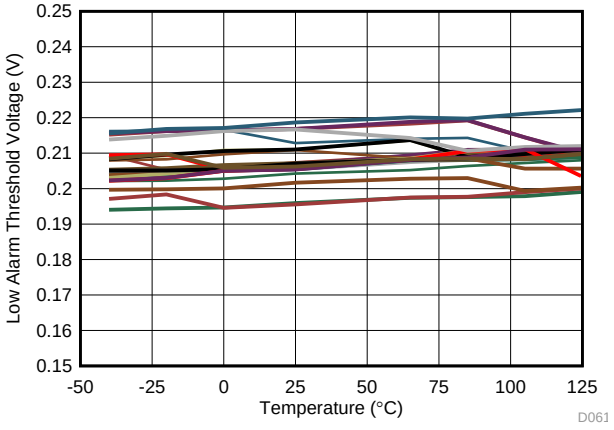


Figure 45. PGA Absolute Low Alarm Threshold vs Temperature

Typical Characteristics (continued)

Typical ADC1 characteristics at T_A = 25°C. V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{DVDD} = 3.3 V, V_{REF} = 2.5 V, f_{CLK} = 7.3728 MHz, data rate = 20 SPS, and PGA gain = 1 (unless otherwise noted)

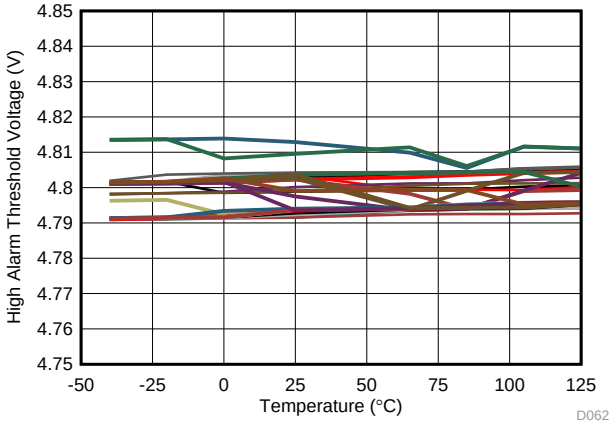


Figure 46. PGA Absolute High Alarm Threshold vs Temperature

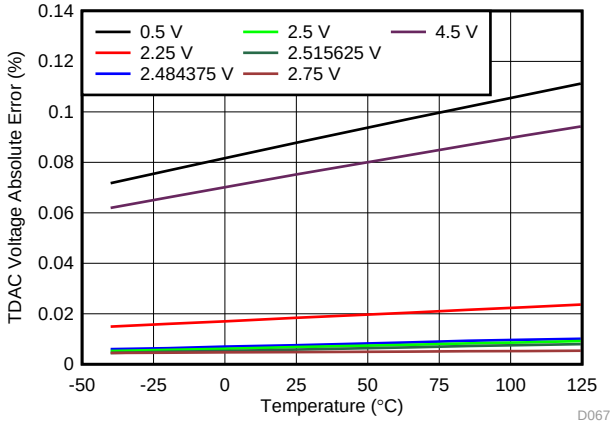


Figure 47. TDAC Error vs Temperature

8 Parameter Measurement Information

8.1 Offset Temperature Drift Measurement

Offset temperature drift is defined as the maximum change of offset voltage measured over the specified temperature range. The offset voltage drift is input referred and is calculated using the box method, as described by Equation 1:

$$\text{Offset Voltage Drift} = (V_{OSMAX} - V_{OSMIN}) / (T_{MAX} - T_{MIN}) \quad (1)$$

where

- V_{OSMAX} and V_{OSMIN} are the maximum and minimum offset voltages, respectively
- T_{MAX} and T_{MIN} are the maximum and minimum temperatures, respectively, over the specified temperature range

8.2 Gain Temperature Drift Measurement

Gain temperature drift is defined as the maximum change of gain error measured over the specified temperature range. The gain error drift is calculated using the box method, as described by Equation 2:

$$\text{Gain Error Drift} = (GE_{MAX} - GE_{MIN}) / (T_{MAX} - T_{MIN}) \quad (2)$$

where

- GE_{MAX} and GE_{MIN} are the maximum and minimum gain errors, respectively
- T_{MAX} and T_{MIN} are the maximum and minimum temperatures, respectively, over the specified temperature range

8.3 Common-Mode Rejection Ratio Measurement

Common-mode rejection ratio (CMRR) is defined as the rejection of the ADC output to an applied common-mode input voltage. The common-mode input voltage is 60 Hz with a peak-to-peak amplitude equal to the specified absolute input voltage range. The standard deviation (RMS) value of the ADC output is calculated and scaled to volts. In order to measure CMRR, two ADC readings are recorded. The first reading (V_A) is with no common-mode input signal. The first reading represents the baseline ADC noise. The second reading (V_B) is with the common-mode input applied. The second reading represents the combination of the ADC baseline noise plus the increased RMS noise caused by the common-mode input. The ADC baseline noise is extracted from the combined noise to yield the noise induced by the common-mode input voltage. The CMRR measurement is described by Equation 3:

$$CMRR = 20 \cdot Log (V_{IC} / V_{OC})$$

where

- V_{IC} = RMS value of the input common-mode voltage = 1.56 V_{RMS}
- V_{OC} = Calculated RMS value of output voltage = $(V_B^2 – V_A^2)^{0.5}$
- V_A = RMS output voltage with no common-mode input
- V_B = RMS output voltage with common-mode input (3)

For gains > 1, add 6 dB of compensation value for each binary increase of gain.

8.4 Power-Supply Rejection Ratio Measurement

Power-supply rejection ratio (PSRR) is defined as the rejection of the ADC output to the DC change of the power supply voltage referred to the input range. PSRR is calculated using two ADC mean-value readings with inputs shorted, scaled to volts. The first ADC reading (V_{OA}) is acquired at one power-supply voltage, and the second ADC reading (V_{OB}) is acquired after changing the power-supply voltage 0.5 V. The PSRR calculation is described by Equation 4:

$$PSRR = 20 \cdot Log |(V_{PSA} – V_{PSB}) / (V_{OA} – V_{OB})| – 20 \text{ dB}$$

where

- $V_{PSA} – V_{PSB}$ = power-supply dc voltage change = 0.5 V
- $V_{OA} – V_{OB}$ = ADC dc output voltage change (V)
- Range compensation factor = 20 · log (0.5 V / 5 V) = –20 dB for gain = 1 (4)

For gains > 1, add an additional 6 dB of compensation value for each binary increase of gain.

8.5 Reference-Voltage Temperature-Drift Measurement

Internal reference-voltage temperature drift is defined as the maximum change in reference voltage measured over the specified temperature range. The reference voltage drift is calculated using the box method, as described by Equation 5:

$$\text{Reference Drift} = (V_{REFMAX} – V_{REFMIN}) / (V_{REFNOM} \cdot (T_{MAX} – T_{MIN})) \cdot 10^6 \text{ (ppm)}$$

where

- V_{REFMAX}, V_{REFMIN} and V_{REFNOM} are the maximum, minimum and nominal (T_A = 25°C) reference voltages, respectively
- T_{MAX} and T_{MIN} are the maximum and minimum temperatures, respectively, over the specified temperature range (5)

8.6 Reference-Voltage Thermal-Hysteresis Measurement

Internal reference-voltage thermal hysteresis is defined as the change in reference voltage after operating the device at T_A = 25°C, cycling the device through the T_A = 0°C to 85°C temperature range for ten minutes at each temperature and returning to T_A = 25°C. The internal reference thermal hysteresis is defined in Equation 6:

$$\text{Reference Thermal Hysteresis} = |V_{REFPRE} – V_{REFPOST}| / V_{REFPRE} \cdot 10^6 \text{ (ppm)}$$

where

- V_{REFPRE} and $V_{REFPOST}$ are the reference voltages before and after the temperature cycle, respectively (6)

8.7 Noise Performance

The ADC noise performance depends on the following ADC settings: PGA gain, data rate, digital filter mode, and chop mode. Generally, the lowest input-referred noise is achieved using the highest gain possible, consistent with the input signal range. Do not set the gain too high or the result is ADC overrange. Noise also depends on the output data rate and mode of the digital filter. As the data rate reduces, the ADC bandwidth correspondingly reduces. As the order of the digital filter mode increases, the ADC bandwidth also reduces. This reduction in total bandwidth results in lower overall noise. The ADC noise is reduced by a factor of 1.4 with chop mode enabled.

Table 1 shows the noise performance in units of μV_{RMS} (RMS = root mean square) under the conditions shown. The values in parenthesis are peak-to-peak values. Table 2 shows the noise performance in effective number of bits (ENOB) with an external 5-V reference voltage. The values shown in parenthesis are noise-free bits. The definition of *noise-free bits* is the resolution of the ADC with no code flicker. The noise-free bits data are based on the μV_{PP} values. Note that for data rate = 38400 SPS, noise scales with increased reference voltage. For all other data rates, noise does not scale with reference voltage.

The ENOB and noise-free bits shown in the table are calculated using Equation 7.

$$ENOB = \ln (FSR / V_{NRMS}) / \ln (2) \quad (7)$$

where

- FSR = full scale range = $2 \cdot V_{REF}$
- V_{NRMS} = noise voltage

Note if the reference voltage = 5 V and gain = 1, the full FSR cannot be used because of the limited PGA range

The data shown in the noise performance tables represent typical ADC performance at T_A = 25°C. The noise-performance data are the standard deviation and peak-to-peak computations of the ADC data. Because of the statistical nature of noise, repeated noise measurements may yield higher or lower noise results. The noise data are acquired with inputs shorted, from consecutive ADC readings for a period of ten seconds or 8192 data points, whichever occurs first.

Table 1. ADC1 Noise in μV_{RMS} (μV_{PP}) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 2.5 V

DATA RATE	FILTER MODE	GAIN					
		1	2	4	8	16	32
2.5 SPS	FIR	0.145 (0.637)	0.071 (0.279)	0.038 (0.149)	0.023 (0.089)	0.014 (0.064)	0.011 (0.051)
2.5 SPS	Sinc1	0.121 (0.510)	0.058 (0.249)	0.033 (0.143)	0.018 (0.073)	0.012 (0.054)	0.008 (0.037)
2.5 SPS	Sinc2	0.101 (0.437)	0.055 (0.225)	0.025 (0.104)	0.015 (0.064)	0.010 (0.043)	0.007 (0.031)
2.5 SPS	Sinc3	0.080 (0.307)	0.046 (0.195)	0.026 (0.116)	0.013 (0.052)	0.008 (0.034)	0.006 (0.023)
2.5 SPS	Sinc4	0.080 (0.308)	0.043 (0.180)	0.020 (0.078)	0.013 (0.049)	0.008 (0.031)	0.007 (0.027)
5 SPS	FIR	0.206 (1.007)	0.098 (0.448)	0.054 (0.252)	0.028 (0.123)	0.020 (0.098)	0.015 (0.073)
5 SPS	Sinc1	0.161 (0.726)	0.090 (0.432)	0.047 (0.246)	0.026 (0.120)	0.017 (0.083)	0.012 (0.057)
5 SPS	Sinc2	0.146 (0.661)	0.069 (0.308)	0.038 (0.195)	0.021 (0.100)	0.013 (0.061)	0.011 (0.050)
5 SPS	Sinc3	0.128 (0.611)	0.067 (0.325)	0.033 (0.153)	0.019 (0.095)	0.012 (0.054)	0.010 (0.046)
5 SPS	Sinc4	0.122 (0.587)	0.063 (0.269)	0.030 (0.144)	0.017 (0.076)	0.011 (0.048)	0.008 (0.039)
10 SPS	FIR	0.284 (1.418)	0.142 (0.753)	0.077 (0.379)	0.041 (0.197)	0.027 (0.156)	0.023 (0.118)
10 SPS	Sinc1	0.229 (1.220)	0.123 (0.662)	0.060 (0.322)	0.035 (0.177)	0.023 (0.118)	0.018 (0.103)
10 SPS	Sinc2	0.193 (1.019)	0.093 (0.488)	0.048 (0.254)	0.028 (0.149)	0.019 (0.099)	0.016 (0.079)
10 SPS	Sinc3	0.176 (0.896)	0.088 (0.452)	0.043 (0.217)	0.028 (0.137)	0.018 (0.091)	0.014 (0.067)
10 SPS	Sinc4	0.164 (0.788)	0.076 (0.389)	0.040 (0.200)	0.024 (0.119)	0.016 (0.081)	0.013 (0.065)
16.6 SPS	Sinc1	0.306 (1.708)	0.147 (0.810)	0.077 (0.436)	0.044 (0.250)	0.030 (0.176)	0.024 (0.138)
16.6 SPS	Sinc2	0.248 (1.401)	0.122 (0.729)	0.068 (0.403)	0.037 (0.213)	0.024 (0.136)	0.020 (0.111)
16.6 SPS	Sinc3	0.216 (1.221)	0.120 (0.667)	0.060 (0.332)	0.033 (0.197)	0.022 (0.130)	0.017 (0.095)
16.6 SPS	Sinc4	0.214 (1.169)	0.101 (0.544)	0.054 (0.302)	0.031 (0.175)	0.022 (0.129)	0.016 (0.092)
20 SPS	FIR	0.393 (2.467)	0.191 (1.102)	0.104 (0.603)	0.057 (0.353)	0.039 (0.222)	0.030 (0.167)
20 SPS	Sinc1	0.336 (1.861)	0.167 (0.964)	0.085 (0.486)	0.049 (0.266)	0.033 (0.191)	0.026 (0.138)
20 SPS	Sinc2	0.270 (1.560)	0.136 (0.745)	0.070 (0.376)	0.039 (0.231)	0.028 (0.149)	0.021 (0.111)

Noise Performance (continued)

Table 1. ADC1 Noise in μV_{RMS} (μV_{PP}) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 2.5 V (continued)

DATA RATE	FILTER MODE	GAIN					
		1	2	4	8	16	32
20 SPS	Sinc3	0.237 (1.415)	0.124 (0.701)	0.067 (0.399)	0.035 (0.192)	0.024 (0.130)	0.020 (0.109)
20 SPS	Sinc4	0.229 (1.285)	0.113 (0.612)	0.060 (0.325)	0.034 (0.193)	0.022 (0.123)	0.017 (0.098)
50 SPS	Sinc1	0.514 (2.925)	0.255 (1.584)	0.140 (0.940)	0.077 (0.457)	0.051 (0.315)	0.042 (0.264)
50 SPS	Sinc2	0.426 (2.400)	0.209 (1.217)	0.108 (0.666)	0.064 (0.381)	0.042 (0.265)	0.033 (0.200)
50 SPS	Sinc3	0.389 (2.324)	0.196 (1.185)	0.104 (0.624)	0.057 (0.367)	0.038 (0.228)	0.030 (0.179)
50 SPS	Sinc4	0.358 (2.319)	0.175 (1.023)	0.096 (0.597)	0.055 (0.319)	0.036 (0.217)	0.028 (0.176)
60 SPS	Sinc1	0.558 (3.574)	0.285 (1.703)	0.151 (0.913)	0.085 (0.515)	0.055 (0.335)	0.045 (0.271)
60 SPS	Sinc2	0.465 (2.753)	0.235 (1.424)	0.121 (0.760)	0.068 (0.417)	0.046 (0.276)	0.036 (0.208)
60 SPS	Sinc3	0.414 (2.704)	0.208 (1.187)	0.112 (0.655)	0.064 (0.396)	0.042 (0.276)	0.034 (0.197)
60 SPS	Sinc4	0.383 (2.288)	0.195 (1.174)	0.105 (0.623)	0.059 (0.347)	0.040 (0.242)	0.031 (0.188)
100 SPS	Sinc1	0.734 (4.715)	0.361 (2.276)	0.192 (1.209)	0.108 (0.679)	0.071 (0.473)	0.058 (0.362)
100 SPS	Sinc2	0.604 (3.662)	0.305 (1.934)	0.156 (1.072)	0.088 (0.579)	0.059 (0.371)	0.048 (0.321)
100 SPS	Sinc3	0.531 (3.431)	0.277 (1.780)	0.143 (0.935)	0.081 (0.545)	0.054 (0.343)	0.043 (0.288)
100 SPS	Sinc4	0.511 (3.340)	0.255 (1.632)	0.134 (0.861)	0.076 (0.479)	0.050 (0.322)	0.041 (0.271)
400 SPS	Sinc1	1.438 (10.374)	0.734 (5.410)	0.380 (2.657)	0.215 (1.469)	0.143 (1.066)	0.116 (0.843)
400 SPS	Sinc2	1.186 (8.523)	0.607 (4.333)	0.313 (2.280)	0.178 (1.313)	0.119 (0.884)	0.095 (0.676)
400 SPS	Sinc3	1.072 (7.923)	0.550 (3.999)	0.285 (1.991)	0.161 (1.132)	0.107 (0.781)	0.087 (0.630)
400 SPS	Sinc4	0.995 (7.107)	0.508 (3.664)	0.266 (1.947)	0.151 (1.061)	0.101 (0.708)	0.081 (0.583)
1200 SPS	Sinc1	2.451 (17.755)	1.254 (9.305)	0.651 (5.044)	0.368 (2.807)	0.244 (1.846)	0.197 (1.519)
1200 SPS	Sinc2	2.038 (15.480)	1.037 (8.128)	0.545 (4.107)	0.309 (2.315)	0.205 (1.586)	0.165 (1.283)
1200 SPS	Sinc3	1.858 (14.005)	0.960 (7.223)	0.494 (3.833)	0.281 (2.145)	0.186 (1.374)	0.148 (1.094)
1200 SPS	Sinc4	1.743 (13.428)	0.890 (6.585)	0.459 (3.405)	0.261 (2.018)	0.174 (1.337)	0.139 (1.032)
2400 SPS	Sinc1	3.411 (26.095)	1.724 (13.528)	0.903 (6.609)	0.510 (3.920)	0.335 (2.626)	0.270 (2.107)
2400 SPS	Sinc2	2.870 (21.677)	1.468 (11.032)	0.770 (5.932)	0.435 (3.379)	0.286 (2.123)	0.230 (1.758)
2400 SPS	Sinc3	2.656 (20.100)	1.337 (9.936)	0.705 (5.355)	0.395 (3.035)	0.262 (1.951)	0.211 (1.533)
2400 SPS	Sinc4	2.475 (19.447)	1.262 (9.452)	0.657 (4.966)	0.371 (2.869)	0.245 (1.885)	0.198 (1.576)
4800 SPS	Sinc1	4.590 (34.155)	2.329 (17.298)	1.221 (8.943)	0.682 (5.252)	0.446 (3.239)	0.361 (2.957)
4800 SPS	Sinc2	4.091 (30.903)	2.070 (15.168)	1.077 (8.141)	0.606 (4.777)	0.398 (2.986)	0.321 (2.397)
4800 SPS	Sinc3	3.720 (28.423)	1.894 (14.842)	0.998 (7.626)	0.560 (4.176)	0.367 (2.890)	0.297 (2.211)
4800 SPS	Sinc4	3.535 (27.437)	1.784 (13.760)	0.926 (7.273)	0.527 (4.004)	0.349 (2.626)	0.277 (2.184)
7200 SPS	Sinc1	5.326 (42.076)	2.709 (19.749)	1.407 (11.126)	0.792 (5.784)	0.516 (3.881)	0.409 (3.189)
7200 SPS	Sinc2	4.867 (36.820)	2.467 (18.627)	1.280 (9.874)	0.726 (5.612)	0.472 (3.531)	0.379 (2.792)
7200 SPS	Sinc3	4.567 (35.194)	2.310 (17.516)	1.209 (9.036)	0.682 (5.181)	0.445 (3.590)	0.359 (2.666)
7200 SPS	Sinc4	4.365 (34.008)	2.211 (17.432)	1.143 (8.804)	0.642 (5.075)	0.426 (3.261)	0.341 (2.467)
14400 SPS	Sinc5	6.377 (48.242)	3.235 (25.178)	1.675 (12.508)	0.929 (7.280)	0.596 (4.430)	0.466 (3.524)
19200 SPS	Sinc5	8.720 (65.389)	4.432 (32.931)	2.285 (17.055)	1.227 (9.870)	0.747 (5.725)	0.555 (4.058)
38400 SPS	Sinc5	103.55 (759.91)	51.76 (371.46)	25.95 (192.20)	13.02 (99.09)	6.493 (46.060)	3.276 (24.435)

Table 2. ADC1 ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 5 V

DATA RATE	FILTER MODE	GAIN					
		1 (BYPASS)	2	4	8	16	32
2.5 SPS	FIR	26.0 (23.9)	25.9 (23.9)	25.8 (23.8)	25.5 (23.6)	25.4 (23.0)	24.6 (22.4)
2.5 SPS	Sinc1	26.3 (24.2)	26.2 (24.1)	26.0 (23.9)	25.9 (23.8)	25.6 (23.3)	25.0 (22.8)
2.5 SPS	Sinc2	26.6 (24.4)	26.3 (24.2)	26.4 (24.3)	26.1 (24.0)	25.8 (23.6)	25.2 (23.1)
2.5 SPS	Sinc3	26.9 (25.0)	26.5 (24.4)	26.3 (24.2)	26.3 (24.3)	26.1 (23.9)	25.6 (23.5)
2.5 SPS	Sinc4	26.9 (25.0)	26.6 (24.5)	26.7 (24.7)	26.3 (24.4)	26.2 (24.1)	25.2 (23.3)
5 SPS	FIR	25.5 (23.2)	25.4 (23.2)	25.3 (23.1)	25.2 (23.1)	24.8 (22.4)	24.1 (21.9)
5 SPS	Sinc1	25.9 (23.7)	25.5 (23.3)	25.5 (23.1)	25.4 (23.1)	25.0 (22.7)	24.4 (22.2)
5 SPS	Sinc2	26.0 (23.9)	25.9 (23.8)	25.8 (23.4)	25.7 (23.4)	25.4 (23.1)	24.6 (22.4)
5 SPS	Sinc3	26.2 (24.0)	26.0 (23.7)	26.0 (23.8)	25.8 (23.5)	25.6 (23.3)	24.7 (22.5)
5 SPS	Sinc4	26.3 (24.0)	26.1 (24.0)	26.1 (23.9)	25.9 (23.8)	25.7 (23.5)	25.0 (22.8)
10 SPS	FIR	25.1 (22.7)	24.9 (22.5)	24.8 (22.5)	24.7 (22.4)	24.4 (21.8)	23.5 (21.2)
10 SPS	Sinc1	25.4 (23.0)	25.1 (22.7)	25.1 (22.7)	24.9 (22.6)	24.6 (22.2)	23.8 (21.4)
10 SPS	Sinc2	25.6 (23.2)	25.5 (23.1)	25.4 (23.0)	25.2 (22.8)	24.9 (22.4)	24.1 (21.7)
10 SPS	Sinc3	25.8 (23.4)	25.6 (23.2)	25.6 (23.3)	25.2 (22.9)	25.0 (22.5)	24.2 (22.0)
10 SPS	Sinc4	25.9 (23.6)	25.8 (23.4)	25.7 (23.4)	25.5 (23.1)	25.1 (22.7)	24.4 (22.0)
16.6 SPS	Sinc1	25.0 (22.5)	24.8 (22.4)	24.8 (22.3)	24.6 (22.1)	24.2 (21.6)	23.5 (20.9)
16.6 SPS	Sinc2	25.3 (22.8)	25.1 (22.5)	24.9 (22.4)	24.8 (22.3)	24.6 (21.9)	23.7 (21.2)
16.6 SPS	Sinc3	25.5 (23.0)	25.1 (22.7)	25.1 (22.7)	25.0 (22.4)	24.6 (22.0)	23.9 (21.5)
16.6 SPS	Sinc4	25.5 (23.0)	25.4 (22.9)	25.3 (22.8)	25.1 (22.6)	24.7 (22.0)	24.0 (21.5)
20 SPS	FIR	24.6 (22.0)	24.5 (21.9)	24.3 (21.8)	24.2 (21.6)	23.9 (21.2)	23.1 (20.7)
20 SPS	Sinc1	24.8 (22.4)	24.7 (22.1)	24.6 (22.1)	24.4 (22.0)	24.1 (21.5)	23.3 (20.9)
20 SPS	Sinc2	25.1 (22.6)	24.9 (22.5)	24.9 (22.5)	24.7 (22.2)	24.3 (21.8)	23.6 (21.2)
20 SPS	Sinc3	25.3 (22.8)	25.1 (22.6)	25.0 (22.4)	24.9 (22.4)	24.5 (22.0)	23.7 (21.3)
20 SPS	Sinc4	25.4 (22.9)	25.2 (22.8)	25.1 (22.7)	25.0 (22.4)	24.6 (22.1)	23.9 (21.4)
50 SPS	Sinc1	24.2 (21.7)	24.0 (21.4)	23.9 (21.2)	23.8 (21.2)	23.5 (20.7)	22.6 (20.0)
50 SPS	Sinc2	24.5 (22.0)	24.3 (21.8)	24.3 (21.7)	24.0 (21.5)	23.7 (21.0)	23.0 (20.4)
50 SPS	Sinc3	24.6 (22.0)	24.4 (21.8)	24.3 (21.8)	24.2 (21.5)	23.9 (21.2)	23.1 (20.6)
50 SPS	Sinc4	24.7 (22.0)	24.6 (22.0)	24.4 (21.8)	24.3 (21.7)	24.0 (21.3)	23.2 (20.6)
60 SPS	Sinc1	24.1 (21.4)	23.9 (21.3)	23.8 (21.2)	23.6 (21.0)	23.4 (20.6)	22.5 (20.0)
60 SPS	Sinc2	24.4 (21.8)	24.2 (21.6)	24.1 (21.5)	24.0 (21.3)	23.6 (20.9)	22.9 (20.3)
60 SPS	Sinc3	24.5 (21.8)	24.3 (21.8)	24.2 (21.7)	24.0 (21.4)	23.7 (20.9)	23.0 (20.4)
60 SPS	Sinc4	24.6 (22.1)	24.4 (21.8)	24.3 (21.8)	24.1 (21.6)	23.8 (21.1)	23.1 (20.5)
100 SPS	Sinc1	23.7 (21.0)	23.5 (20.9)	23.5 (20.8)	23.3 (20.6)	23.0 (20.1)	22.2 (19.5)
100 SPS	Sinc2	24.0 (21.4)	23.8 (21.1)	23.8 (21.0)	23.6 (20.9)	23.2 (20.5)	22.4 (19.7)
100 SPS	Sinc3	24.2 (21.5)	23.9 (21.2)	23.9 (21.2)	23.7 (20.9)	23.4 (20.6)	22.6 (19.9)
100 SPS	Sinc4	24.2 (21.5)	24.0 (21.4)	24.0 (21.3)	23.8 (21.1)	23.5 (20.7)	22.7 (20.0)
400 SPS	Sinc1	22.7 (19.9)	22.5 (19.6)	22.5 (19.7)	22.3 (19.5)	22.0 (19.0)	21.2 (18.3)
400 SPS	Sinc2	23.0 (20.2)	22.8 (20.0)	22.7 (19.9)	22.6 (19.7)	22.2 (19.2)	21.5 (18.6)
400 SPS	Sinc3	23.2 (20.3)	22.9 (20.1)	22.9 (20.1)	22.7 (19.9)	22.4 (19.4)	21.6 (18.7)
400 SPS	Sinc4	23.3 (20.4)	23.0 (20.2)	23.0 (20.1)	22.8 (20.0)	22.5 (19.6)	21.7 (18.8)
1200 SPS	Sinc1	22.0 (19.1)	21.7 (18.9)	21.7 (18.7)	21.5 (18.6)	21.2 (18.2)	20.4 (17.5)
1200 SPS	Sinc2	22.2 (19.3)	22.0 (19.0)	21.9 (19.0)	21.8 (18.9)	21.5 (18.4)	20.7 (17.7)
1200 SPS	Sinc3	22.4 (19.4)	22.1 (19.2)	22.1 (19.1)	21.9 (19.0)	21.6 (18.6)	20.8 (17.9)
1200 SPS	Sinc4	22.5 (19.5)	22.2 (19.3)	22.2 (19.3)	22.0 (19.1)	21.7 (18.6)	20.9 (18.0)
2400 SPS	Sinc1	21.5 (18.5)	21.3 (18.3)	21.2 (18.3)	21.0 (18.1)	20.7 (17.7)	20.0 (17.0)
2400 SPS	Sinc2	21.7 (18.8)	21.5 (18.6)	21.4 (18.5)	21.3 (18.3)	21.0 (18.0)	20.2 (17.3)

Table 2. ADC1 ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 5 V (continued)

DATA RATE	FILTER MODE	GAIN					
		1 (BYPASS)	2	4	8	16	32
2400 SPS	Sinc3	21.8 (18.9)	21.7 (18.8)	21.6 (18.6)	21.4 (18.5)	21.1 (18.1)	20.3 (17.5)
2400 SPS	Sinc4	21.9 (19.0)	21.7 (18.8)	21.7 (18.8)	21.5 (18.5)	21.2 (18.2)	20.4 (17.4)
4800 SPS	Sinc1	21.1 (18.2)	20.8 (18.0)	20.8 (17.9)	20.6 (17.7)	20.3 (17.4)	19.5 (16.5)
4800 SPS	Sinc2	21.2 (18.3)	21.0 (18.1)	21.0 (18.0)	20.8 (17.8)	20.5 (17.5)	19.7 (16.8)
4800 SPS	Sinc3	21.4 (18.4)	21.1 (18.2)	21.1 (18.1)	20.9 (18.0)	20.6 (17.5)	19.8 (16.9)
4800 SPS	Sinc4	21.4 (18.5)	21.2 (18.3)	21.2 (18.2)	21.0 (18.1)	20.7 (17.7)	19.9 (16.9)
7200 SPS	Sinc1	20.8 (17.9)	20.6 (17.8)	20.6 (17.6)	20.4 (17.5)	20.1 (17.1)	19.4 (16.4)
7200 SPS	Sinc2	21.0 (18.1)	20.8 (17.8)	20.7 (17.8)	20.5 (17.6)	20.2 (17.2)	19.5 (16.6)
7200 SPS	Sinc3	21.1 (18.1)	20.9 (17.9)	20.8 (17.9)	20.6 (17.7)	20.3 (17.2)	19.5 (16.7)
7200 SPS	Sinc4	21.1 (18.2)	20.9 (17.9)	20.9 (17.9)	20.7 (17.7)	20.4 (17.4)	19.6 (16.8)
14400 SPS	Sinc5	20.6 (17.7)	20.4 (17.4)	20.3 (17.4)	20.2 (17.2)	19.9 (16.9)	19.2 (16.3)
19200 SPS	Sinc5	20.1 (17.2)	19.9 (17.0)	19.9 (17.0)	19.8 (16.8)	19.6 (16.6)	18.9 (16.0)
38400 SPS	Sinc5	15.6 (12.6)	15.4 (12.6)	15.4 (12.5)	15.3 (12.5)	15.5 (12.6)	15.4 (12.5)

9 Detailed Description

9.1 Overview

The ADS1262 and ADS1263 are precision 32-bit, delta-sigma (ΔΣ) ADCs with an integrated analog front end (AFE) to simplify connection to sensors. The 32-bit ADC (ADC1) provides output data rates from 2.5 SPS to 38400 SPS for flexibility in resolution and data rates over a wide range of applications. The ADC low noise and low drift architecture make these devices suitable for precise digitization of low-level transducers, such as load cell bridges and temperature sensors. The ADS1263 includes an auxiliary 24-bit delta-sigma ADC (ADC2).

The ADS1262 and the ADS1263 integrate several functions that provide increased utility. The key integrated functions include:

- Low-drift voltage reference
- Dual, matched, sensor-excitation current sources (IDAC)
- Input-level-shift voltage
- Eight GPIOs
- Dual-sensor, bias current sources
- Low-noise, CMOS PGA with integrated signal fault detection
- Internal test signal source (TDAC)
- Temperature sensor
- Internal oscillator
- Three sets of buffered external reference inputs with low reference voltage alarm

As seen in the Functional Block Diagram, the ADC features 11 analog inputs that are configurable as either ten single-ended inputs, five differential inputs, or any combination, to either ADC1 or ADC2. Many of the analog inputs are multifunction as programmed by the user. The analog inputs can be programmed to the following extended functions:

- Three external reference inputs: pins AIN0, AIN1, AIN2, AIN3, AIN4 and AIN5
- Two sensor excitation current source: all analog input pins
- Level shift (VBIAS): AINCOM pin
- Eight GPIO: pins AIN3, AIN4, AIN5, AIN6, AIN7, AIN8, AIN9, AINCOM
- Sensor break current source: all analog input pins
- Two test signal output: pins AIN6, AIN7

Following the input multiplexer, ADC1 features a high-impedance, CMOS, programmable gain amplifier (PGA). The PGA provides very low voltage and current noise, enabling direct connection to low-level transducers, and in many cases, eliminating the need for an external amplifier. The PGA gain is programmable from 1 V/V to 32 V/V in binary steps. The PGA can be bypassed to allow the input range to extend below ground. The PGA has voltage overrange monitors to improve the integrity of the conversion result. The PGA overrange alarm is latched during the conversion phase and appended to the conversion data. The programmable sensor bias uses a test current to help detect a failed sensor or sensor connection.

An inherently stable delta-sigma modulator measures the ratio of the input voltage to the reference voltage to provide the ADC result. The ADC operates with the internal 2.5-V reference, or with up to three external reference inputs. The external reference inputs are continuously monitored for low (or missing) voltage. The reference alarm status is latched during the conversion phase and appended to the conversion data. The REFOUT pin is the buffered 2.5-V internal voltage reference output.

Dual excitation current sources (IDAC) provide bias to resistance sensors (such as 3-wire RTD). The ADC integrates several system monitors for readback, such as temperature sensor and supply monitor. The ADC features an internal test signal voltage (TDAC) that is used to verify the ADC operation across all gains. The TDAC has two outputs to provide test voltages for single-ended and differential input configurations. Eight GPIO ports are available on the analog input pins.

The digital filter provides two functional modes, sinc and FIR, allowing optimization of settling time and line-cycle rejection. The sinx/x (sinc) filter is programmable to sinc orders one through four to tradeoff filter settling time and 50-Hz and 60-Hz line-cycle rejection. The finite impulse response (FIR) filter mode provides single-cycle settled data with 50-Hz and 60-Hz line cycle rejection at data rates up to 20 SPS.

Overview (continued)

The ADS1263 includes an auxiliary 24-bit delta-sigma ADC (ADC2) featuring buffered PGA inputs, gains from 1 V/V to 128 V/V, and data rates up to 800 SPS. All analog inputs and reference inputs are available to ADC2. ADC2 can be used to provide redundant measurements or system measurements such as sensor temperature compensation and thermocouple cold junction compensation (CJC). The ADS1263 is pin and functionally compatible to the ADS1262.

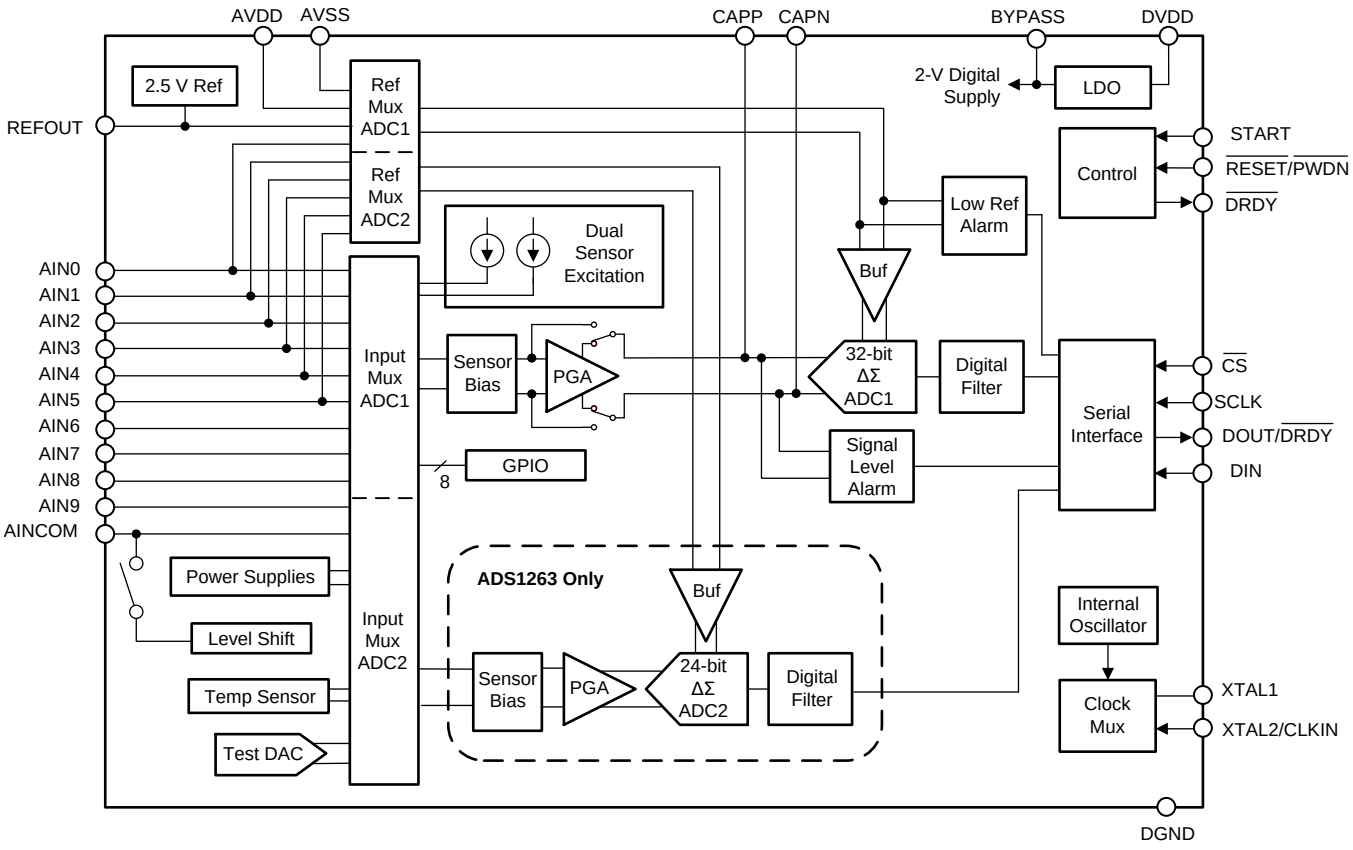
The SPI™-compatible serial interface is used to read the conversion data and also to configure and control the ADC. The serial interface consists of four signals: $\overline{CS}$, SCLK, DIN and DOUT/$\overline{DRDY}$. The conversion data are provided with a CRC code for improved data integrity. The dual function DOUT/$\overline{DRDY}$ output indicates when conversion data are ready and also provides the data output. The serial interface can be implemented with as little as three connections by tying $\overline{CS}$ low.

The ADC has three clock options: internal oscillator, external crystal, and external clock. The ADC detects the clock mode automatically. The nominal clock frequency is 7.3728 MHz.

ADC conversions are started by a control pin or by commands. The ADC can be programmed to free-run mode or perform one-shot conversions. The $\overline{DRDY}$ and DOUT/$\overline{DRDY}$ pins are driven low when the conversion data are ready. The $\overline{RESET}$/PWDN digital input resets the ADC when momentarily pulsed low, and when held low, enables the ADC power-down mode.

The ADC operates with bipolar (± 2.5 V) supplies, or with a single 5-V supply. For single-supply operation, use the internal level-shift voltage to level-shift isolated (floating) sensors The digital power-supply range is 2.7 V to 5.25 V. The BYPASS pin is the subregulator output (2 V) that is used for internal digital supply.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Multifunction Analog Inputs

The ADC has 11 multifunction analog inputs that can be configured in a variety of extended functions. Figure 48 shows the internal analog signal routing to the circuit blocks. Table 3 summarizes the input pin functions. The ADC has two cross-point multiplexers, one multiplexer for ADC1 and one multiplexer for ADC2. The multiplexers select any analog input for the positive PGA input and any input for the negative PGA input. The ADCs can also be configured for a number of internal monitor functions. The internal monitors are temperature sensor, TDAC test voltage, analog power supply voltage and digital power supply voltage. The dual excitation current sources (IDAC1 and IDAC2) can be independently connected to any analog input pin. Eight analog inputs can be configured as GPIO. The GPIO can be programmed as inputs or outputs and are referenced to the analog power supplies voltages (V_{AVDD} and V_{AVSS}). The level shift function (VBIAS) is available on AINCOM and can be used to provide an input level-shift voltage for isolated sensors. The internal TDAC test voltage is available on output pins AIN6 and AIN7. The ADC has two voltage reference multiplexers, one reference multiplexer for ADC1 and one reference multiplexer for ADC2. Through the reference multiplexers, the internal reference, three external reference sources or the analog power supply voltage ($V_{AVDD} – V_{AVSS}$) can be selected.

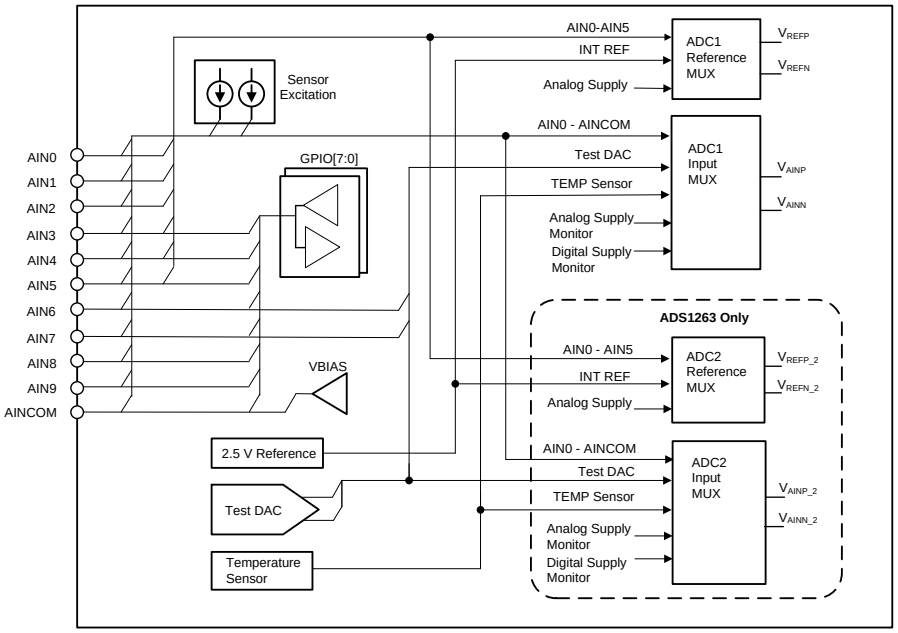


Figure 48. Analog Input Routing Overview

Table 3. Analog Input Pin Functions

PIN	ADC1 INPUT	ADC2 INPUT	ADC1 REF INPUT(1)	ADC2 REF INPUT	IDAC1 OUTPUT	IDAC2 OUTPUT	GPIO	TDAC OUTPUT	LEVEL SHIFT
AIN0	Yes	Yes	REFP1, REFN1	REFP1	Yes	Yes	—	—	—
AIN1	Yes	Yes	REFP1, REFN1	REFN1	Yes	Yes	—	—	—
AIN2	Yes	Yes	REFP2, REFN2	REFP2	Yes	Yes	—	—	—
AIN3	Yes	Yes	REFP2, REFN2	REFN2	Yes	Yes	GPIO[0]	—	—
AIN4	Yes	Yes	REFP3, REFN3	REFP3	Yes	Yes	GPIO[1]	—	—
AIN5	Yes	Yes	REFP3, REFN3	REFN3	Yes	Yes	GPIO[2]	—	—
AIN6	Yes	Yes	—	—	Yes	Yes	GPIO[3]	TDACP	—
AIN7	Yes	Yes	—	—	Yes	Yes	GPIO[4]	TDACN	—
AIN8	Yes	Yes	—	—	Yes	Yes	GPIO[5]	—	—
AIN9	Yes	Yes	—	—	Yes	Yes	GPIO[6]	—	—
AINCOM	Yes	Yes	—	—	Yes	Yes	GPIO[7]	—	Yes

(1) The reference voltage of ADC1 can be either polarity and reversed by programming.

9.3.2 Analog Input Description

As shown in Figure 49, the analog inputs of the device consist of ESD protection diodes, an ADC1/ADC2 cross-point input multiplexer, the sensor bias circuit, and individual PGAs for each ADC. The ADC has 11 external inputs, four internal monitor signals, and one no-connection (float). Note that in figures throughout this document, italic text shows the associated register and register settings.

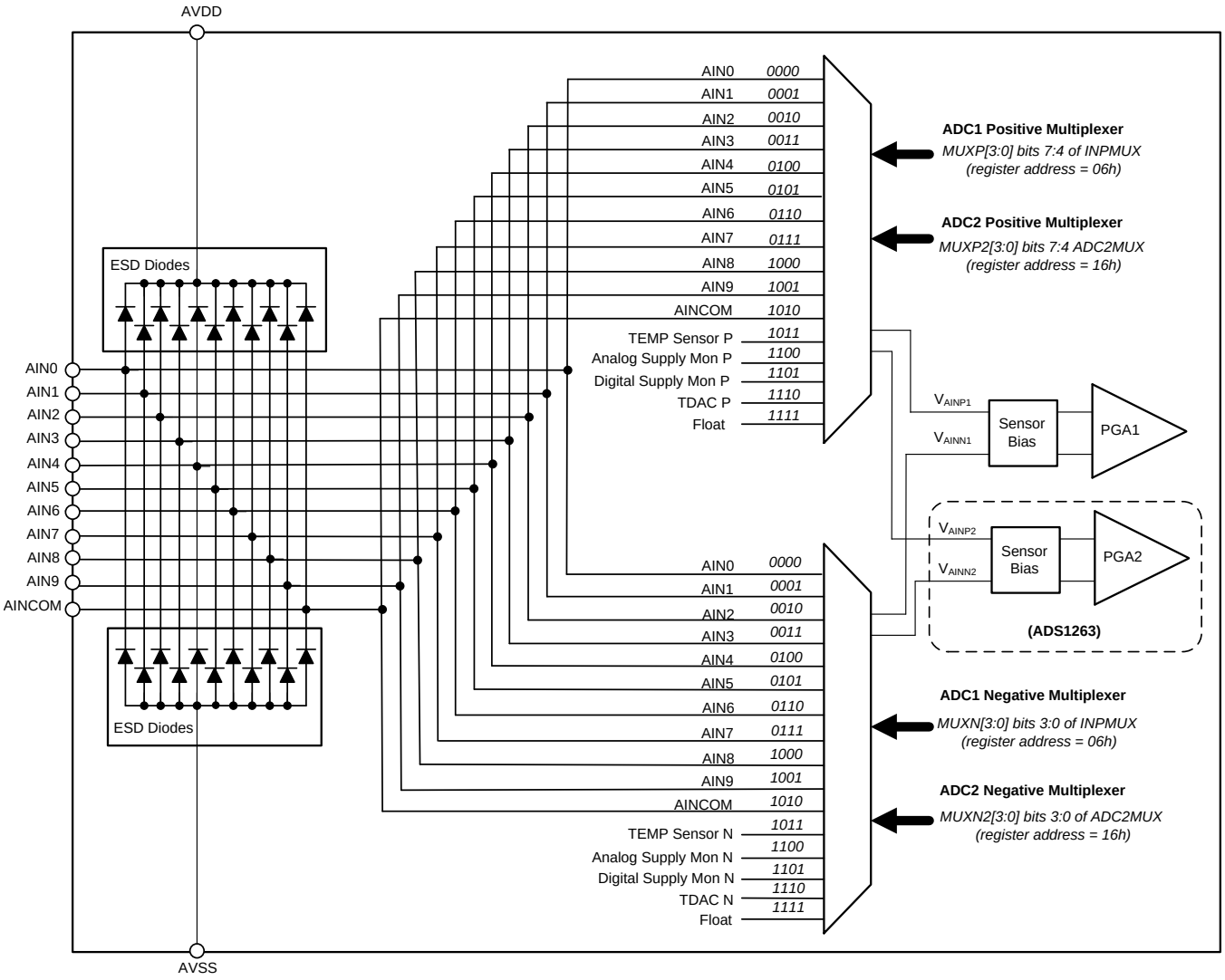


Figure 49. ADC1 and ADC2 Input Block Diagram

9.3.2.1 ESD Diode

The analog inputs have internal ESD diodes that are connected to the analog supplies (AVDD and AVSS). The function of the diodes is to protect the ADC inputs from ESD events. If the input signal exceeds V_{AVDD} by more than 0.3 V or goes below V_{AVSS} by more than -0.3 V, the diodes may conduct and as a result, input current will flow into the analog inputs through the AVDD or AVSS pins. If an input over-voltage is possible, the input current must be limited to < |±10 mA|. In many applications, a resistor in series with the input is sufficient to limit the current. Depending on the application requirements, the thermal noise of the current limit resistor should be considered.

9.3.2.2 Input Multiplexer

The dual, cross-point input multiplexers are used to select from one of the 11 external inputs, 4 internal monitors and one floating connection, in any combination to either ADC. One input must be selected by the positive multiplexer and one input is selected by the negative multiplexer. The ADC1 positive and negative multiplexers are programmed by register INPMUX (address = 06h), bits MUXP[3:0] and bits MUXN[3:0]. The ADC2 positive and negative multiplexers has identical functionality and are programmed by register ADC2MUX (address = 16h), bits MUXP2[3:0] bits and bits MUXN2[3:0].

9.3.3 Sensor Bias

The ADC incorporates a sensor bias current source that can be used to apply a small test current to diagnose broken sensor leads or problems existing in the sensor. Figure 50 shows the sensor bias block diagram. The sensor bias circuit consists of programmable current sources and bias resistors. The sensor bias circuit connects to the outputs of either the ADC1 or ADC2 multiplexers. The sensor bias can be selected to either pull-up or pull-down mode. In pull-up mode, the current flows into the positive input and the current flows out of the negative input. In pull-down mode, the polarities are reversed. The sensor bias can be programmed to 10 MΩ bias resistor or current magnitudes of ±0.5, ±2, ±10, ±50 and ±200 µA.

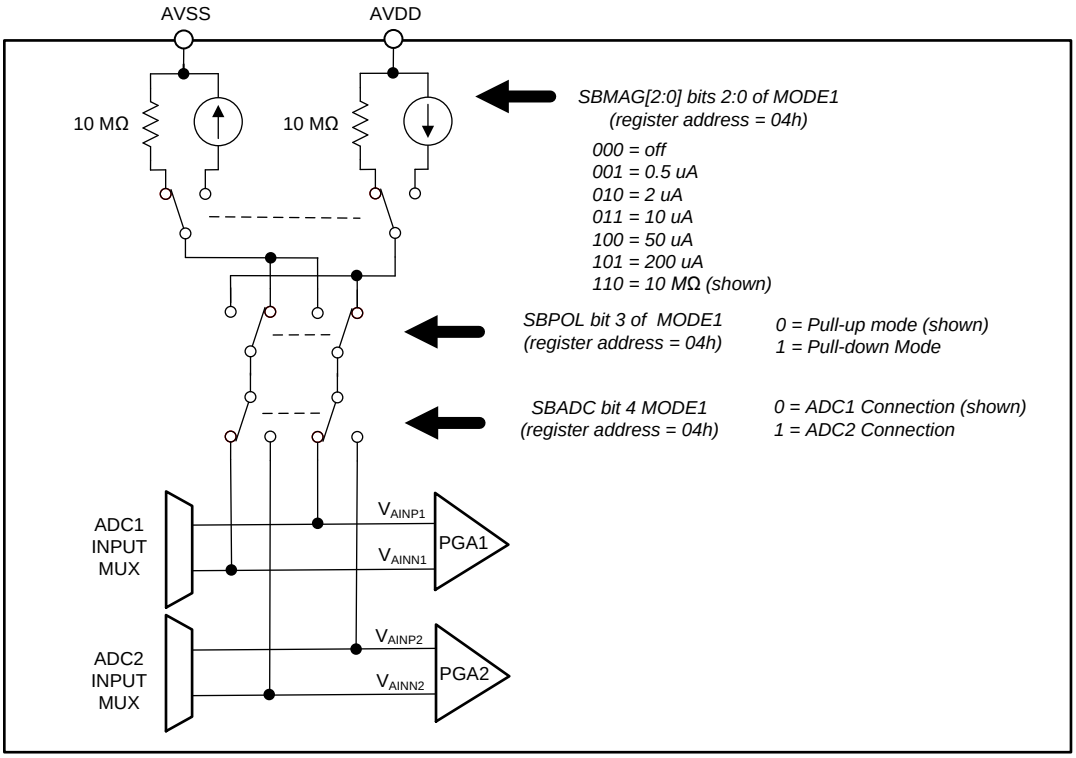


Figure 50. Sensor Bias Block Diagram

In pull-up mode, an open sensor results in the positive input pulled to V_{AVDD} and the negative input pulled to V_{AVSS}. An open sensor in pull-up mode results in a positive full-scale reading. A full-scale reading may also indicate that the sensor is overloaded or that the reference voltage is lower than expected. The sensor bias can remain on while actively converting or pulsed-on periodically to test the sensor. Note external capacitance may load the sensor bias when first enabled. Additionally, an offset error may exist as the senor bias current flows through the multiplexer switch resistance.

9.3.4 Temperature Sensor

The ADC integrates a temperature sensor. The temperature sensor is comprised of two internal diodes with one diode having 16x the current density of the other, as shown in Figure 51. The difference in current density of the diodes yields a differential output voltage that is proportional to absolute temperature. The temperature sensor voltage can be measured by either ADC1 or ADC2. For ADC1 measurement, set Register INPMUX (address 06h) to BBH. For ADC2 measurement, set Register ADC2MUX (address 16h) to BBh. Equation 8 shows how to convert the temperature sensor reading to ˚C.

Temperature (°C) = [(Temperature Reading (µV) – 122,400) / 420 µV/°C] + 25°C

where

- Temperature reading is scaled from codes to µV (8)

Prior to the temperature sensor measurement, enable PGA gain = 1, disable chop mode and ensure the internal voltage reference is powered on. As a result of the low package-to-PCB thermal resistance, the internal device temperature tracks the PCB temperature closely. Note that ADC self heating results in an increase of 0.7°C relative to the temperature of the surrounding PCB.

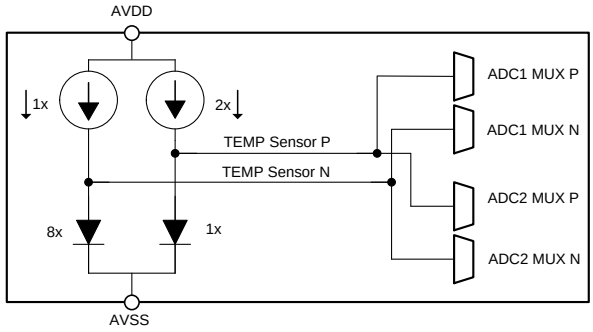


Figure 51. Temperature Sensor

9.3.5 Power-Supply Monitor

The ADC power supplies can be monitored internally by either ADC1 or ADC2. Shown in Figure 52, the power supply voltages are divided by a resistor network to reduce the voltages to within the ADC input range. The reduced power-supply voltage is routed to the ADC input multiplexers. The analog and digital power supply readings are scaled by Equation 9 and Equation 10.

$$V_{ANLMON} = (V_{AVDD} – V_{AVSS}) / 4 \quad (9)$$

$$V_{DIGMON} = (V_{DVDD} – V_{DGND}) / 4 \quad (10)$$

The supply monitor readings can be measured using either internal or external reference. When an external reference is used, the minimum reference voltage is 1.5 V. Set the PGA gain = 1 and disable Chop prior to the measurement. For analog supply monitor ADC1 measurement, set the INPMUX register (address 06h) to CCH. For digital supply monitor ADC1 measurement, set the bits to DDh. For analog supply monitor ADC2 measurement, set the ADC2MUX register (address 16h) to CCh. For digital supply monitor ADC2 measurement, set the ADC2MUX register to DDh.

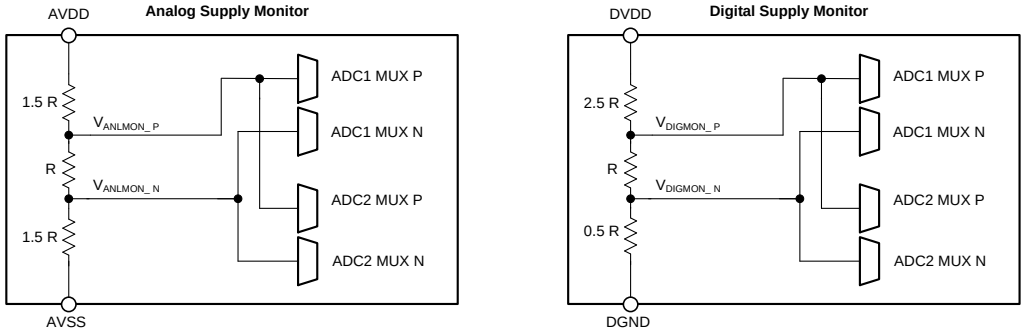


Figure 52. Power-Supply Monitors

9.3.6 PGA

The ADC1 PGA is a low noise, programmable gain, CMOS differential-input, differential-output amplifier. The PGA extends the ADC dynamic range of sensors with low input-signal levels. The PGA provides gains of 1, 2, 4, 8 ,16 and 32. The PGA can be bypassed to extend the analog input range to below ground (V_{AVSS}).

Figure 53 shows the PGA block diagram. The PGA consists of two chopper stabilized amplifiers (A1 and A2) and a resistor network that is programmed to set the PGA gain. The PGA input is equipped with high frequency electro-magnetic interference (EMI) input filter consisting of two 350 Ω input resistors and filter capacitors as shown in the figure. The PGA can be bypassed to directly connect the inputs to the ADC. The PGA output is monitored by an over-range voltage monitor. The voltage monitor provides an alarm when the absolute or the differential PGA output voltage exceeds the linear range of operation. Pins CAPP and CAPN are the PGA outputs, P and N respectively. Connect a 4.7 nF (C0G) capacitor as shown in the figure. The capacitor provide an analog anti-alias filter as well as the de-glitch filter for the ADC modulator sampling. Place the capacitor close to the pins using short, direct traces. Avoid running clock traces or other digital traces close to the pins.

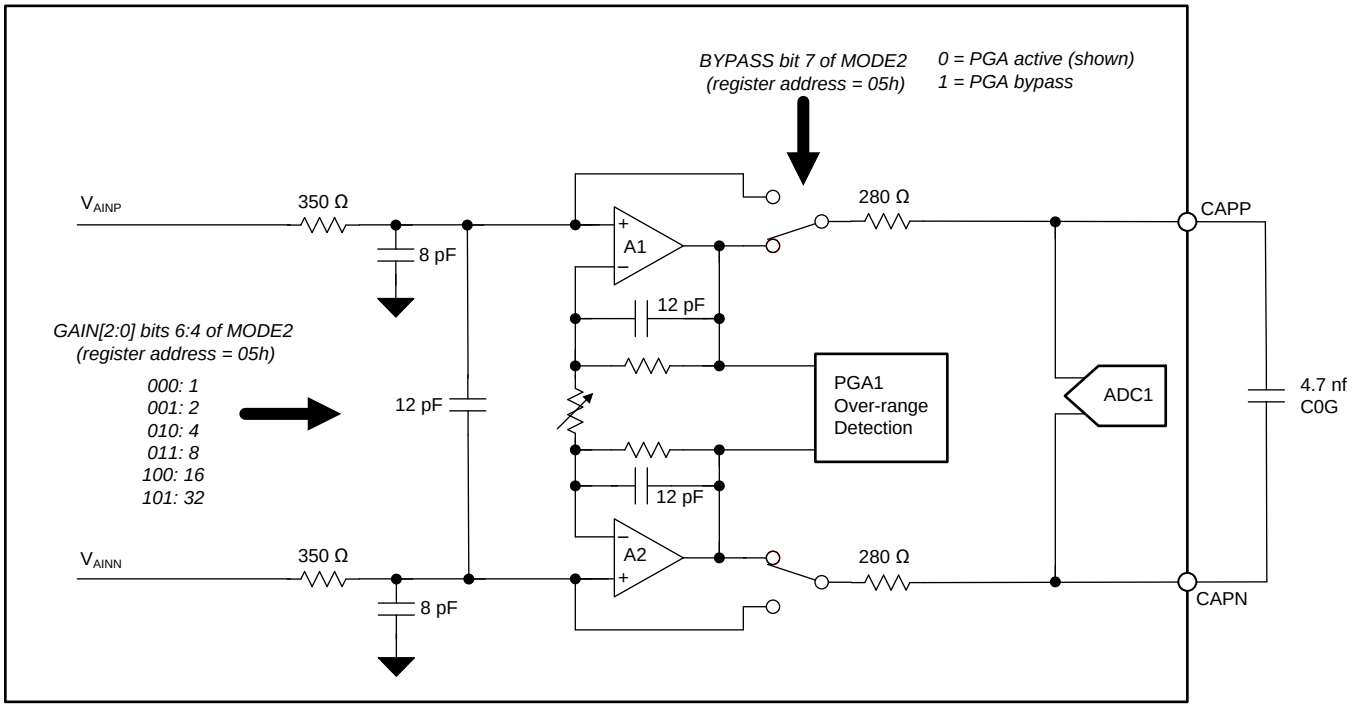


Figure 53. ADC1 PGA Block Diagram

The ADC input voltage range is determined by the reference voltage and the PGA gain. Table 4 shows the input voltage range verses gain for reference voltage = 2.5 V. The input voltage range scales with the reference voltage and can be increased or decreased by changing the reference voltage.

Table 4. ADC1 Input Range

GAIN[2:0] BITS OF REGISTER MODE2	GAIN (V/V)	INPUT RANGE (V)(1)
000	1	± 2.500 V
001	2	± 1.250 V
010	4	± 0.625 V
011	8	± 0.312 V
100	16	± 0.156 V
101	32	± 0.078 V

(1) V_{REF} = 2.5 V . The input voltage range is proportional to V_{REF}

As with many amplifiers, the PGA has an absolute input voltage range requirement that cannot be exceeded. The maximum input voltage is limited by the voltage swing capability of the PGA output. The specified minimum and maximum absolute input voltages (V_{INP} and V_{INN}) depend on the PGA gain, the magnitude of input differential voltage (V_{IN}) and the tolerance of the analog power supply voltages (V_{AVDD},V_{AVSS}). It is necessary that the absolute positive and negative input voltage are within specified range as shown in the Equation 11.

$$V_{AVSS} + 0.3 + |V_{IN}| \cdot (Gain - 1) / 2 \cdot < V_{INP} \text{ and } V_{INN} < V_{AVDD} - 0.3 - |V_{IN}| \cdot (Gain - 1) / 2$$

where

- V_{INP}, V_{INN} = Absolute input voltage
- V_{IN} = Differential input voltage = V_{INP} - V_{INN} (11)

The relationship between the PGA input to the PGA output is shown graphically in Figure 54. The PGA output voltages (V_{OUTP}, V_{OUTN}) depend on the PGA gain and the input voltage magnitudes. To maintain linear operation, the PGA output voltages cannot exceed V_{AVDD} – 0.3 V or V_{AVSS} + 0.3 V. Note the diagram depicts a positive differential input voltage that results in a positive differential output voltage.

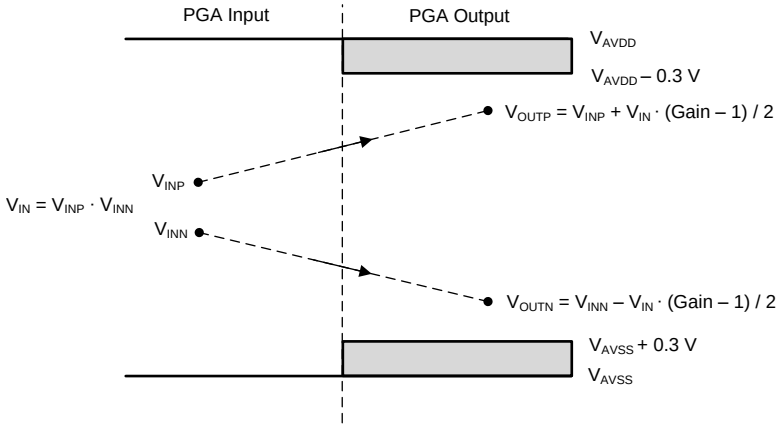


Figure 54. PGA Input/Output Range

If the PGA is bypassed, the ADC input range extends beyond the V_{AVDD} and V_{AVSS} supply voltages as shown in Equation 12:

$$V_{AVSS} - 0.1 < V_{INP} \text{ and } V_{INN} < V_{AVDD} + 0.1 \quad (12)$$

9.3.7 PGA Voltage Overrange Monitors

ADC1 integrates two PGA output voltage monitors. The monitors trigger an alarm if the PGA output is driven into overrange. The corresponding bits are set (= 1) in the data output status byte when an alarm occurs. The PGA output voltage is monitored in two ways:

1) Differential: If the PGA differential output voltage exceeds either +105% or –105% FSR.

2) Absolute: If either PGA absolute output voltage is higher than V_{AVDD} – 0.2 V or lower than V_{AVSS} + 0.2 V.

The alarms automatically reset when the PGA is no longer in voltage overload. Note the monitors consist of fast responding analog level-comparators. Therefore, the monitors can detect short duration voltage overranges that are not necessarily evident in the output as clipped codes. This is due to averaging of the digital filter that may span one or more conversion cycles. The monitor function can be used to detect certain type of faults, such as signal over-range, incorrect gain setting, sensor faults, input mis-wiring, and so on, without the need to change input configuration or interrupt readings.

9.3.7.1 PGA Differential Output Monitor

ADC1 integrates a differential PGA output voltage monitor. The voltage monitor triggers an alarm when the magnitude of the *differential* PGA output voltage is more positive than +105% or more negative than -105% of full scale. The alarm indicates that the PGA output voltage has exceeded the modulator range during the course of an active conversion cycle. The alarm event, corresponding to the conversion cycle that triggers the alarm, is set in the status byte. For the next conversion. the alarm is cleared. If the magnitude of differential output voltage is within the range of +105% to –105% of full scale range, the alarm remains cleared. The PGA differential monitor block diagram is shown in Figure 55.

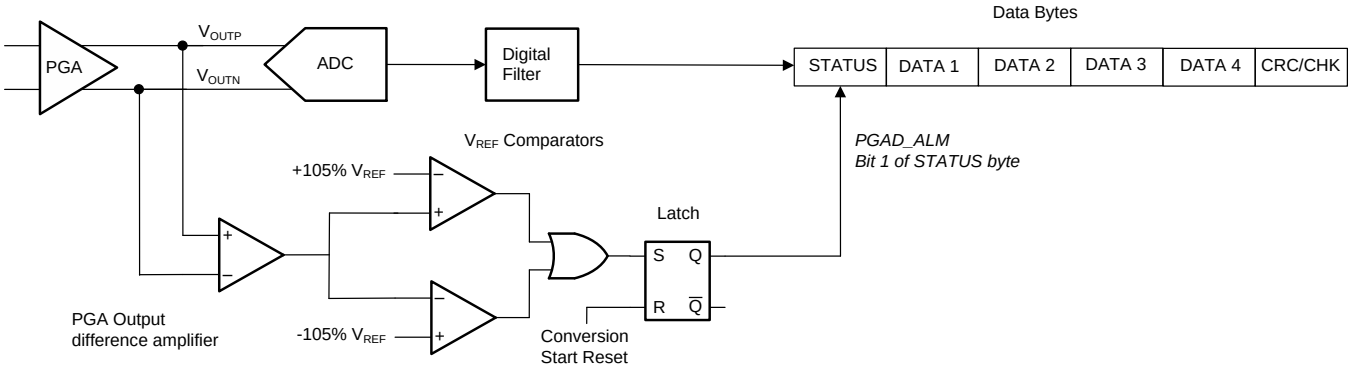


Figure 55. PGA Differential Overload Monitor

Figure 56 shows an example of the differential overrange monitor event.

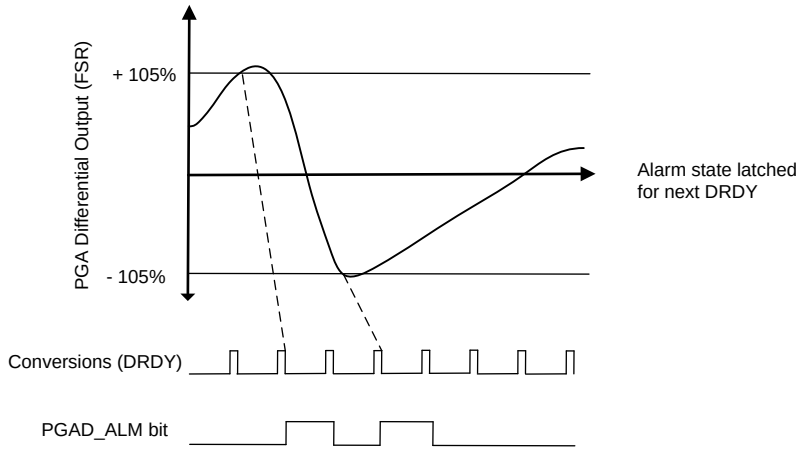


Figure 56. PGA Differential Alarm

9.3.7.2 PGA Absolute Output-Voltage Monitor

The ADC integrates a PGA absolute output-voltage monitor. If the absolute level of the PGA positive or negative output exceeds V_{AVDD} – 0.2 V, the PGA high alarm is triggered (PGAH). If the absolute level of the PGA positive or negative output voltage is less than V_{AVSS} + 0.2 V the PGA low alarm is triggered (PGAL). The alarms are set in the status byte corresponding to the conversion cycle in which the alarms occurred. For the next conversion cycle, the alarms are cleared. if the magnitude of PGA output voltages remains within the range (V_{AVDD} - 0.2 V and V_{AVSS} + 0.2 V), the alarms remain cleared. The PGA absolute output-voltage monitor block diagram is shown in Figure 57.

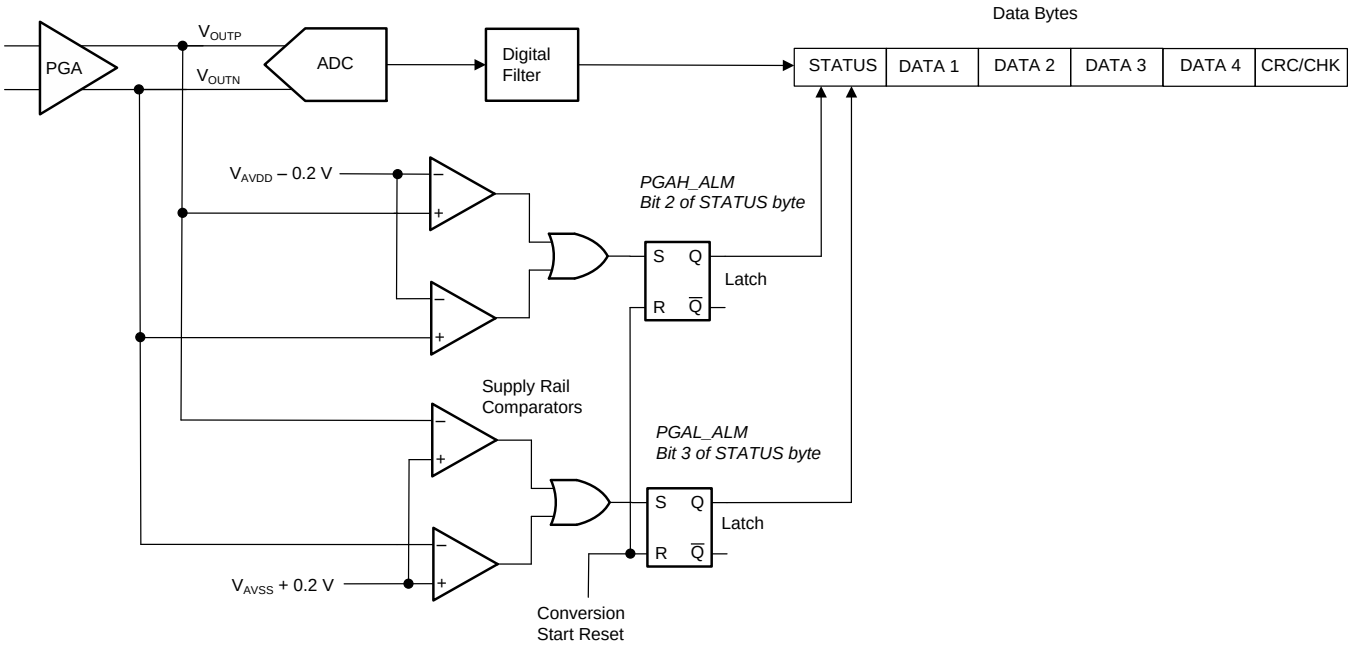


Figure 57. PGA Absolute Output-Voltage Monitor

Figure 58 shows an example of the PGA absolute output-voltage monitor overrange event.

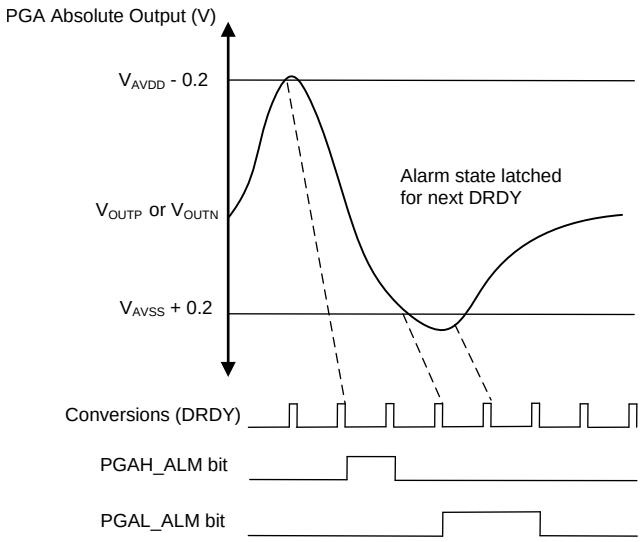
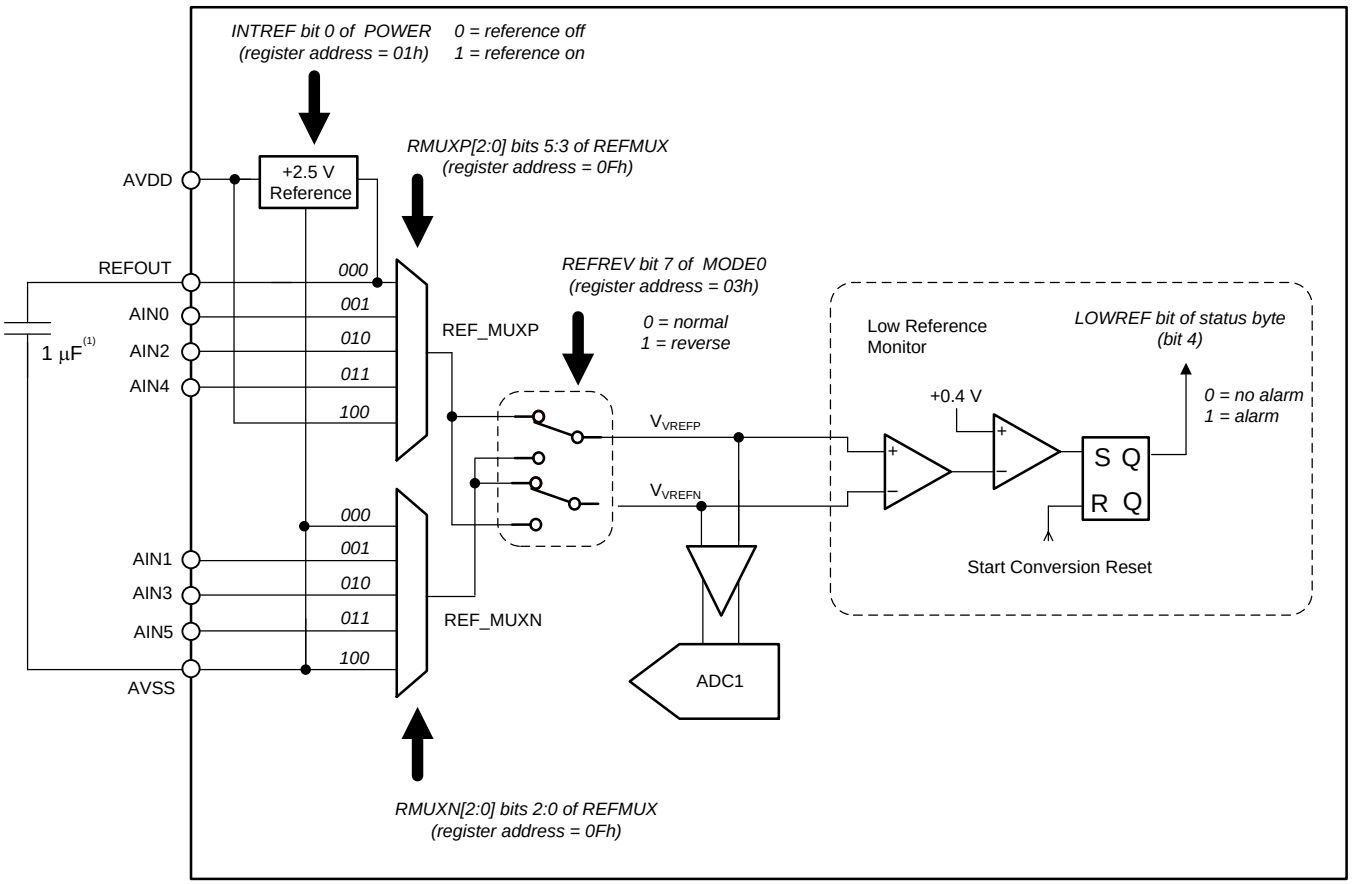


Figure 58. PGA Absolute Alarm

9.3.8 ADC Reference Voltage

The ADC requires a reference voltage for operation. The reference voltage of ADC1 can be independent of the ADC2 reference voltage. The reference voltage can be provided internally by the internal reference (2.5 V) or externally, by one of the three external reference inputs. The specified external reference voltage range is 0.9 V to 5 V. The reference voltage is defined as $V_{REF} = V_{REFP} - V_{REFN}$, where V_{REFP} and V_{REFN} are the absolute positive and absolute negative reference voltages, respectively. The reference voltage polarity must always be positive. The magnitude of the reference voltage together with the PGA gain establishes the ADC differential input range ($V_{IN} = \pm V_{REF}$ / Gain). Figure 59 shows the block diagram of the ADC1 reference multiplexer. Use the reference multiplexer to select the internal reference, one of three external reference inputs, or the analog power supply.



(1) The internal reference requires a 1 µF capacitor connected to pins REFOUT and AVSS.

Figure 59. ADC1 Reference Multiplexer Block Diagram

The ADC1 reference multiplexer consists of a positive multiplexer and a negative multiplexer. The multiplexers are programmed independently by register bits RMUX[2:0] and RMUXN[2:0], of register REFMUX, respectively. The positive reference selection is either internal 2.5 V reference (positive), external on pins AIN0, AIN2, AIN4 or the analog power supply voltage (V_{AVDD}). The negative reference selection is either internal 2.5 V reference (negative), external on pins AIN1, AIN3, AIN5 or the analog supply voltage (V_{AVSS}). A reference polarity reversal switch changes the reference polarity from negative to positive. The polarity switch allows either a positive or negative external reference polarities. Program the reversal switch to the normal position (REFREV = 0) when using the internal reference. The ADC integrates a low reference voltage monitor. The monitor provides continuous detection of a low or missing reference during the conversion cycle. The low reference alarm is appended to the data output status byte (LOWREF, bit 4 of the status byte).

9.3.8.1 Internal Reference

The ADC integrates a precision 2.5 V reference featuring very low drift. The internal reference is enabled by setting INTREF equal to 1 (default is on). To select the internal reference for use with ADC1, set both RMUXP and RMUXN bits of register REFMUX to 000. The REFOUT pin provides a buffered reference output voltage. The reference negative (return) is the AVSS pin, as shown in Figure 59. Care must be taken in layout of the REFOUT return to the AVSS pin. Connect a 1-uF capacitor from the REFOUT pin to the AVSS pin. If the internal reference is not used the capacitor is not required. Note the internal reference must be powered if using the IDAC or the internal temperature sensor. After internal reference start-up, the reference requires settling time before starting the first conversion. See Figure 32.

9.3.8.2 External Reference

The ADC provides three external reference inputs. The reference input is differential with positive and negative inputs. The reference inputs are the analog pins, AIN0 - AIN5. Typically, the positive reference is applied to pins AIN0, AIN2 or AIN4, and the negative reference is applied to pins AIN1, AIN2 or AIN3. The reference polarity can be negative, but the ADC requires a positive voltage reference. In this case, the polarity can be reversed by an internal switch (ADC1 reference only). The reference inputs are high impedance, however note the reference input current Figure 33. The reference input current can lead to loading effects in non-zero reference source impedance. However, in many applications, an external reference buffer is not required. Connect a 100 nF bypass capacitor across the external reference input pins. Observe the specified absolute and differential reference voltage requirements.

9.3.8.3 Power-Supply Reference

A third option for ADC reference is the internal analog power supply. However, an increase of linearity error results with this connection and therefore this option is recommended only for less critical applications such as ADC self-diagnostics. For precision measurements, such as 6-wire load cell measurements, connect the bridge excitation voltages to the external reference inputs.

9.3.8.4 Low Reference Monitor

The ADC integrates a low reference monitor to detect a low or missing reference. If the differential reference voltage ($V_{REF} = V_{REFP} - V_{REFN}$) falls below 0.4 V (typical), a low reference alarm is triggered. The low reference alarm sets the corresponding bit in the conversion data status byte. The alarm bit is cleared at the start of each new conversion. The low reference monitor is typically used to detect a missing or failed reference voltage connection. Connect a 100-kΩ resistor across the reference inputs. If either reference input is missing or unconnected, the external resistor biases the reference inputs toward each other. Note that the low-reference monitor is a fast-responding level comparator; therefore, reference voltage transients may be detected.

9.3.8.5 Sensor-Excitation Current Sources (IDAC1 and IDAC2)

The ADC integrates two matched current sources (IDAC1, IDAC2). The current sources are intended to provide excitation current to Resistive Temperature Devices (RTD), thermistors, diodes and other sensors that require constant current biasing. The ADCs incorporates an internal IDAC multiplexer that allows connection of IDAC1 or IDAC2 to one of the 11 analog pins (AIN0 to AINCOM). The IDACs can be programmed over the current ranges: 50 µA, 100µA, 250 µA, 500 µA, 750 µA, 1000 µA, 1500 µA, 2000 µA and 3000 µA. Figure 60 details the IDAC connection. The IDAC switches shown in the diagram are used in the IDAC rotation mode.

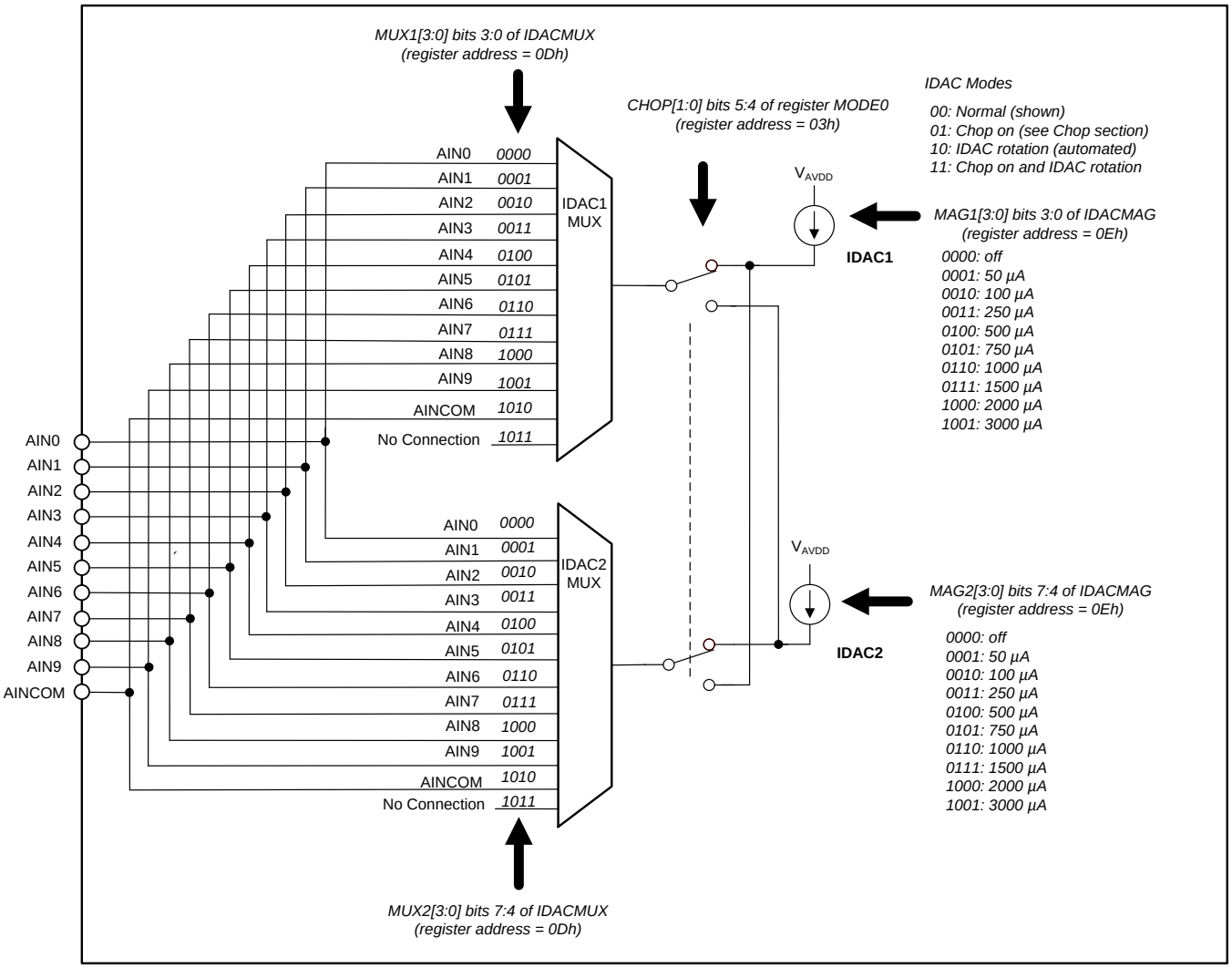


Figure 60. IDAC Block Diagram

The internal reference must be enabled for IDAC operation. Care should be taken not to exceed the compliance voltage of the IDACs. In other words, the voltage on the input pin should not exceed V_{AVDD} – 1.1 V, otherwise the specified accuracy of the IDAC current is not met.

The current sources track the internal voltage reference. As a result of using the same reference voltage for IDAC1 and IDAC2, the currents sources have matched characteristics. Matched performance is important for applications such as hardware compensated, 3-wire RTDs. IDAC matching can be improved further by use of the IDAC rotation mode. The rotation mode interchanges the IDAC1 and IDAC2 connections on alternate conversions. The alternate conversions are averaged to eliminate the IDAC mis-match. IDAC rotation can be performed manually by the user (by alternating the IDAC pin connections) or by the IDAC rotation mode. The IDAC rotation mode interchanges the IDAC pin connections and averages the conversion results. The IDAC rotation sequence is shown as follows:

- Conversion 1: IDAC1, IDAC2 normal → first output result withheld
- Conversion 2: IDAC1, IDAC2 rotated positions → Output result 1 = (Conversion 1 + Conversion 2) / 2
- Conversion 3: IDAC1, IDAC2 normal → Output result 2 = (Conversion 3 + Conversion 2) / 2
- Conversion 4: IDAC1, IDAC2 rotated positions → Output result 3 = (Conversion 4 + Conversion 3) / 2

The sequence repeats for all conversions.

In rotation mode, the ADC allows for settling after the IDAC pin connections are alternated. The settling time results in a reduction of the nominal data rate (see the *Conversion Latency* section). Nevertheless, the existing frequency response nulls remain unchanged. IDAC switching transients may interact with external components, requiring time to settle. Additional settling time can be provided by the ADC DELAY parameter.

9.3.8.6 Level Shift

The ADC integrates an optional level shift voltage on the AINCOM pin. As shown in Figure 61, the level shift voltage is the mid-voltage of the analog power supply. The level shift is intended for level-shift floating sensors (that is, sensors isolated from the ADC ground) to within the ADC specified input range. Thermocouple and 4-20mA transmitters (isolated supply) are examples of floating signals.

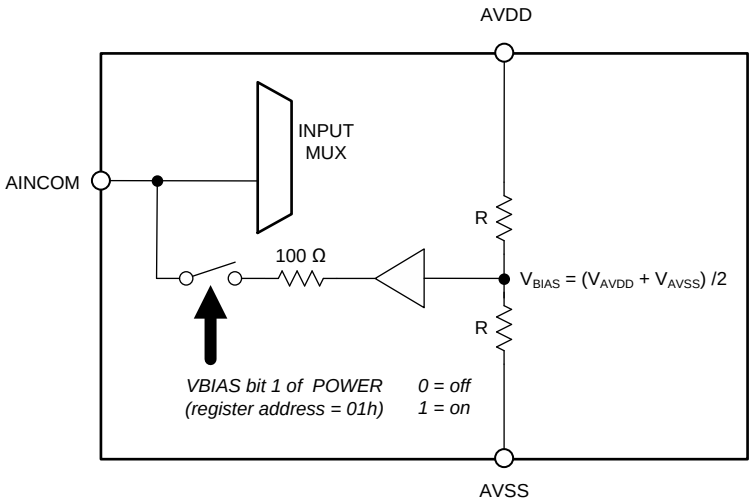


Figure 61. Level Shift Voltage Diagram

When the ADC is operated with ±2.5 V analog supplies, the AINCOM pin can be grounded instead of using the level shift voltage. Level shift of other inputs is possible by connecting the pins to the REFOUT pin (2.5 V) . The turn-on time of the level shift voltage depends on the pin load capacitance. The capacitance includes those connected to AVDD, AVSS and ground. Table 5 lists the level shift voltage settling times for various external load capacitors. Be certain the level shift voltage is fully settled before starting a conversion.

Table 5. Level Shift Enable Time

LOAD CAPACITANCE	LEVEL SHIFT VOLTAGE SETTLING TIME
0.1 µf	0.22 ms
1 µf	2.2 ms
10 µf	22 ms

9.3.9 Digital Filter

The digital filter receives the modulator output data and produces a high-resolution conversion result. The digital filter low pass filters and down-samples the modulator data, yielding the final output data. By adjusting the type of filtering, tradeoffs can be made between resolution, data rate, line cycle rejection and conversion latency.

The digital filter has two selectable modes: sin (x) / x (sinc) mode or finite impulse response (FIR) mode (see Figure 62). The sinc mode provides data rates of 2.5 SPS though 38400 SPS with selectable sinc orders of 1 through 5. The FIR filter provides simultaneous rejection of 50-Hz and 60-Hz power-line frequencies with data rates 2.5 SPS through 20 SPS with single-cycle settled conversions.

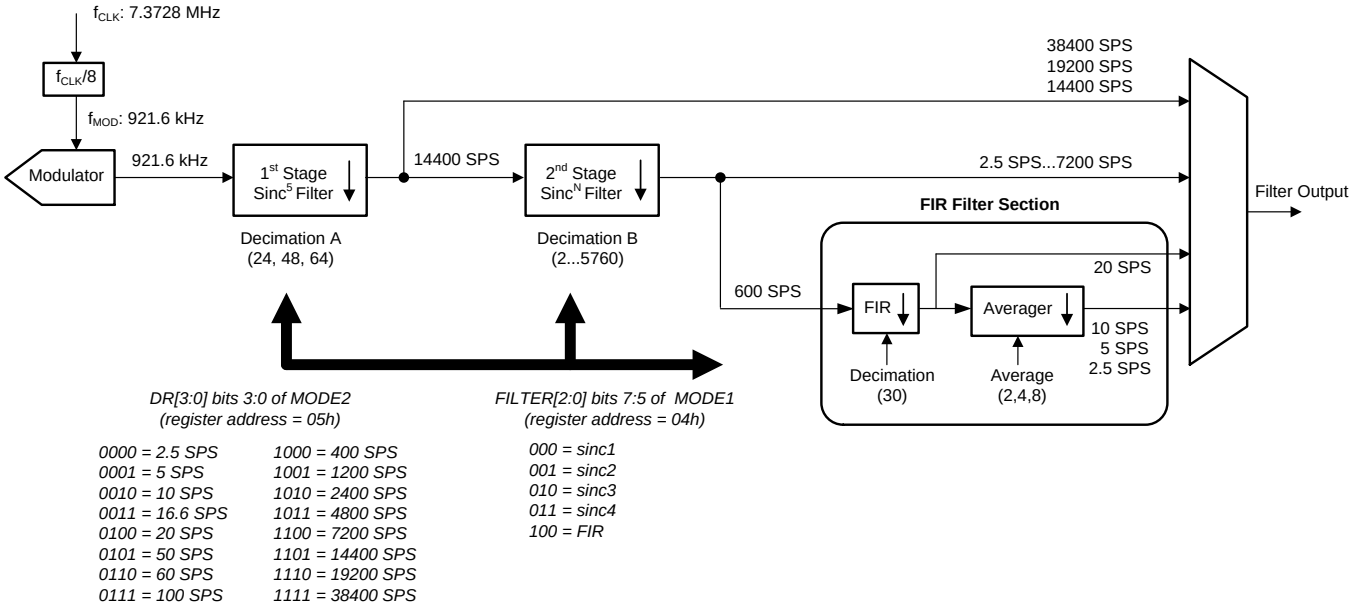


Figure 62. Digital Filter Block Diagram

9.3.9.1 Sinc Filter Mode

The sinc filter consists of two stages: a variable-decimation, fixed order sinc5 filter followed by a variable-decimation, variable order sinc filter. The first-stage filter is sinc5 and reduces the rate of the modulator data (f_{CLK} / 8 = 921.6 kHz) to 38400 SPS, 19200 SPS and 14400 SPS by decimating to 24, 48 and 64, respectively. These data rates bypass the second filter stage and as result have a sinc5 frequency response profile. The second filter stage receives the data from the first-stage at 14400 SPS. The second stage reduces the data rate to produce output data of 7200 SPS to 2.5 SPS. The second stage is a variable-order sinc filter that is programmable.

The overall decimation ratio of the first and second stages determine the output data rate as follows: data rate = 921.6 kHz / (A · B). The filter order of the second stage determines the 50-Hz and 60-Hz rejection together with conversion latency. The higher-order sinc filter provides the widest 50-Hz and 60-Hz null widths, but increases the conversion latency. The sinc order is programmed by the FILTER[2:0] bits of register MODE1 Table 6 lists the decimation ratio corresponding to the first and second filter stages (A and B, respectively) for each data rate. The data rate is programmed by the DR[3:0] bits of register MODE2.

Table 6. Sinc Filter Mode Data Rates and Decimation Ratio

DATA RATE (SPS)(1)	DR[3:0] BITS OF REGISTER MODE2	FIRST-STAGE DECIMATION RATIO A	SECOND-STAGE DECIMATION RATIO B
2.5	0000	64	5760
5	0001	64	2880
10	0010	64	1440
16.6	0011	64	864
20	0100	64	720
50	0101	64	288
60	0110	64	240
100	0111	64	144
400	1000	64	36
1200	1001	64	12
2400	1010	64	6
4800	1011	64	3
7200	1100	64	2
14400	1101	64	1
19200	1110	48	1
38400	1111	24	1

(1) f_{CLK} = 7.3728 MHz. Data rate scales with f_{CLK}

9.3.9.1.1 Sinc Filter Frequency Response

The low pass filtering effect of the sinc filter sets the overall frequency response of the ADC. The frequency response of data rates 14400 SPS, 19200 SPS and 38400 SPS is that of the first filter section. The frequency response of data rates 2.5 SPS ranging to 7200 SPS is the product of the first and second individual frequency responses. The overall filter response is given in Equation 13:

$$\left|H_{(f)}\right| = \left|H_{sinc^5}(f)\right| \times \left|H_{sinc^N}(f)\right| = \left|\frac{\sin\left[\frac{8\pi f A}{f_{CLK}}\right]}{A \times \sin\left[\frac{8\pi f}{f_{CLK}}\right]}\right|^5 \times \left|\frac{\sin\left[\frac{512\pi f B}{f_{CLK}}\right]}{B \times \sin\left[\frac{512\pi f}{f_{CLK}}\right]}\right|^N \quad (13)$$

where

- f = signal frequency
- f_{CLK} = ADC clock frequency
- A = First-stage decimation ratio (see Table 6)
- B = Second-stage decimation ratio (see Table 6)
- N = Second-stage filter order where N = 1 (sinc1), 2 (sinc2), 3 (sinc3), or 4 (sinc4)

The digital filter attenuates out of band noise that may be present in the signal and also noise within the PGA and ADC modulator. Adjusting the filter by changing the decimation ratio and sinc order changes the filter bandwidth. Tradeoffs can be made between signal bandwidth, noise and filter latency.

As shown in Figure 63 and Figure 64, the first stage sinc5 filter has frequency response nulls occurring at the data rate (f_{MOD} / A) and at data rate multiples. At the null frequencies, the filter has zero gain.

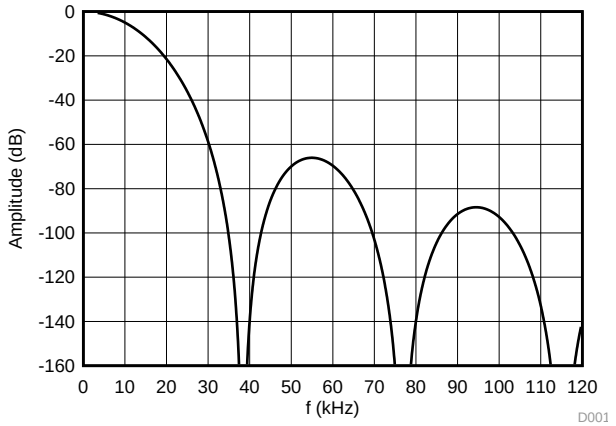


Figure 63. Sinc Frequency Response (38400 SPS)

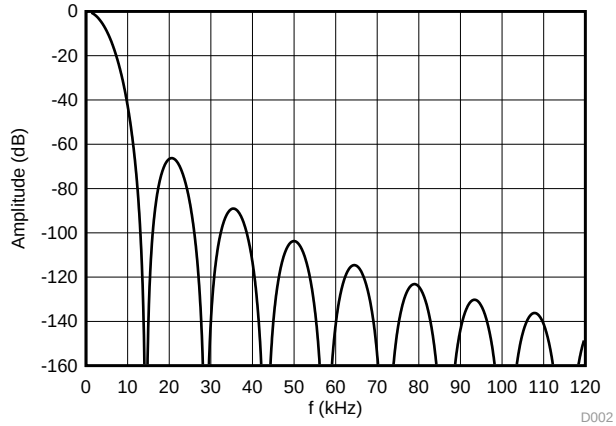


Figure 64. Sinc Frequency Response (14400 SPS)

The second stage superimposes new nulls in the frequency response over the nulls produced by the first stage. The first of the superimposed frequency response nulls occur at the output data rate, followed by nulls occurring at data rate multiples.

Figure 65 illustrates the frequency response of data rate 2400 SPS produced by the second stage filter. This data rate has five equally-spaced nulls between the larger nulls produced by the first stage. The frequency response is also characteristic of data rates 2.5 SPS to 7200 SPS that are also produced by the second stage filter. Figure 66 shows the frequency response nulls at 10 SPS.

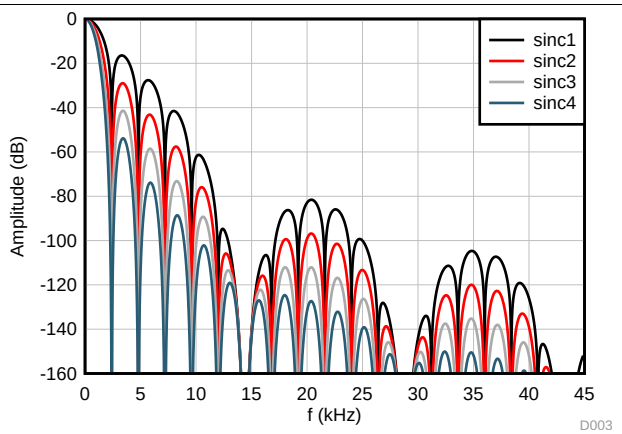


Figure 65. Sinc Frequency Response (2400 SPS)

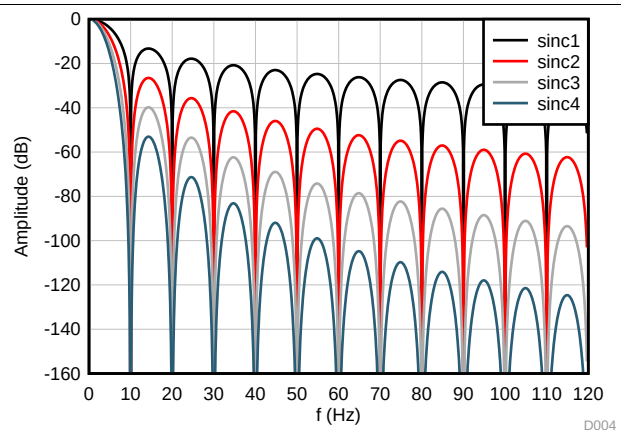


Figure 66. Sinc Frequency Response (10 SPS)

Figure 67 and Figure 68 illustrate the frequency response of data rates 50 SPS and 60 SPS. The frequency response is plotted out to the 50-Hz 12th harmonic (10th harmonic for 60 Hz). The 50-Hz or 60-Hz fundamental frequency and harmonics are suppressed by increasing the filter order, as shown in the figures.

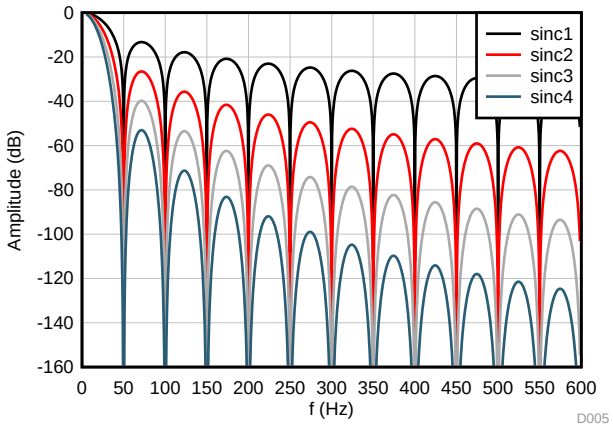


Figure 67. Sinc Frequency Response (50 SPS)

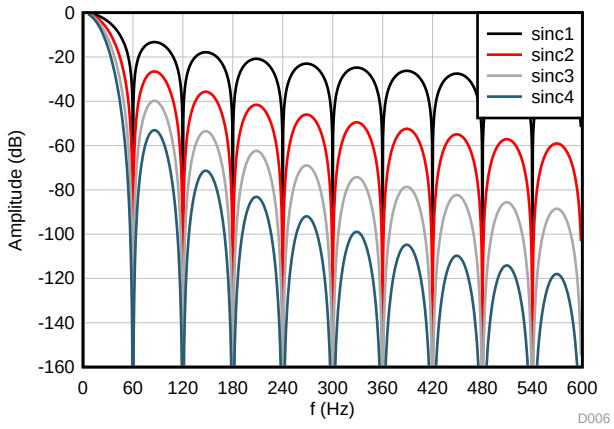


Figure 68. Sinc Frequency Response (60 SPS)

Figure 69 and Figure 70 plots the detailed frequency response of 50-SPS and 60-SPS data rates for the different sinc filter orders. Note the high-order sinc filter settings increase the width of the null, improve line cycle rejection, and increases the tolerance of the ADC clock accuracy and that of the prevailing 50-Hz and 60-Hz line frequency. As shown in the plots, the best 50-Hz or 60-Hz rejection is provided by the sinc4 order, but has longer filter latency compared to the sinc1 order.

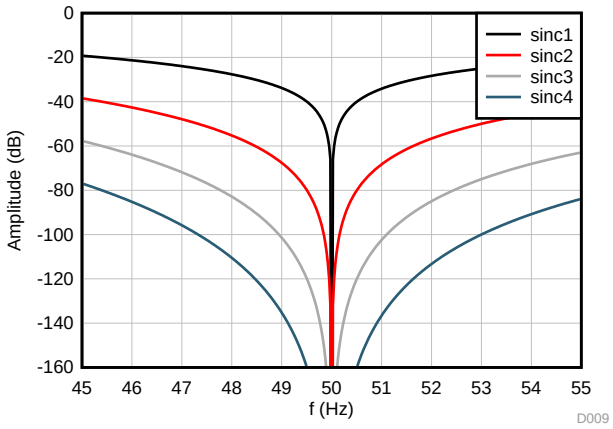


Figure 69. Sinc Frequency Response Zoom (50 SPS)

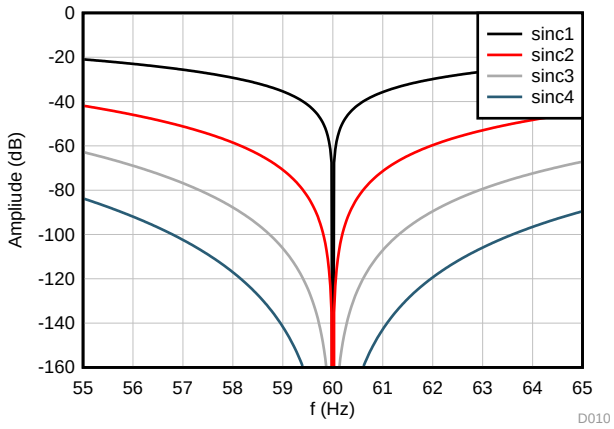


Figure 70. Sinc Frequency Response Zoom (60 SPS)

The overall sinc filter frequency response is similar to analog low-pass filter that rolls off high frequency components in the signal. The signal bandwidth depends on the output data rate and the order of the sinc filter. Note the overall system bandwidth is the combination of the digital filter, the anti-alias filter and external filter components. Table 7 lists the –3-dB filter bandwidth of the sinc filter. Note the bandwidth reduction of the higher-order sinc filters.

Table 7. Sinc Filter Bandwidth

DATA RATE (SPS)	-3-dB BANDWIDTH (Hz)				
	SINC1	SINC2	SINC3	SINC4	SINC5
2.5	1.10	0.80	0.65	0.58	—
5	2.23	1.60	1.33	1.15	—
10	4.43	3.20	2.62	2.28	—
16.6	7.38	5.33	4.37	3.80	—
20	8.85	6.38	5.25	4.63	—
50	22.1	16.0	13.1	11.4	—
60	26.6	19.1	15.7	13.7	—
100	44.3	31.9	26.2	22.8	—
400	177	128	105	91.0	—
1200	525	381	314	273	—
2400	1015	751	623	544	—
4800	1798	1421	1214	1077	—
7200	2310	1972	1750	1590	—
14400	—	—	—	—	2940
19200	—	—	—	—	3920
38400	—	—	—	—	7740

9.3.9.2 FIR Filter

The finite impulse response (FIR) filter is a coefficient based filter that provides simultaneous rejection of 50-Hz and 60-Hz line cycle frequencies and harmonics. The FIR filter data rates are 2.5, 5, 10 and 20 SPS. All of the FIR data rates settle within a single conversion cycle. The slower FIR data rates provide improved line cycle frequency rejection. As shown in Figure 62, the FIR filter section receives data from the second-stage sinc filter at 600 Hz. The FIR filter section decimates by 30 to yield the output data rate of 20 SPS. A first-order averager (sinc1) with variable decimation provides the data rates of 10 SPS, 5 SPS, and 2.5 SPS.

As shown in Figure 71 and Figure 72, the FIR filter frequency response has a series of response nulls centered at the 50 Hz and 60 Hz. The response nulls repeat at the 50-Hz and 60-Hz harmonics. The FIR frequency response superimposes with the response of the 600-SPS pre-stage filter.

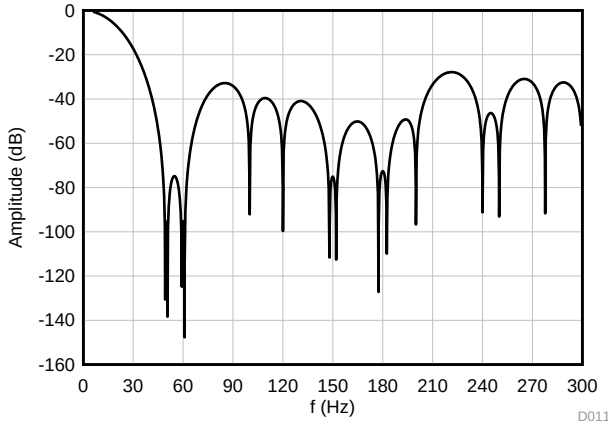


Figure 71. FIR Frequency Response (20 SPS)

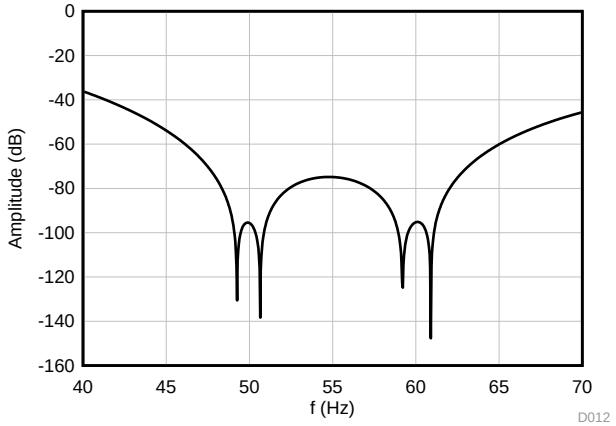


Figure 72. FIR Frequency Response Zoom (20 SPS)

Figure 73 is the FIR filter response at 10 SPS. As a result of the sinc1 averager in the FIR filter block, new frequency response nulls are superimposed to the response shown in Figure 71. The first of the added response nulls occur at 10 Hz. Additional nulls occur at folded frequencies around 20-Hz multiples. These additional nulls can be seen at 10 Hz and 30 Hz.

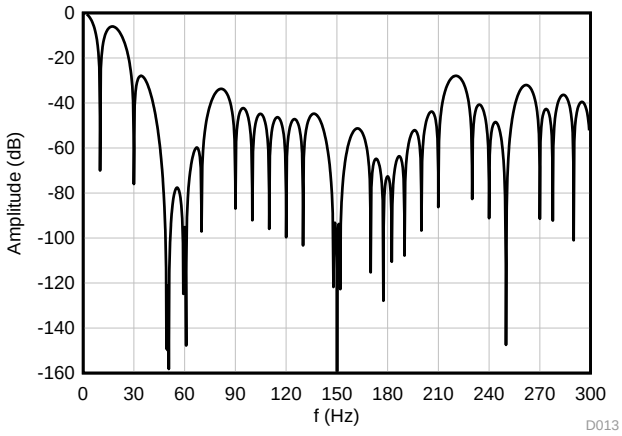


Figure 73. FIR Frequency Response (10 SPS)

Similar to the response of the sinc filter, the overall FIR filter frequency response is similar to an analog low-pass filter that rolls off high frequencies of the signal. The response is such that the FIR filter limits the bandwidth of the input signal. The FIR filter signal bandwidth depends on the output data rate. Table 8 lists the –3dB filter bandwidth of the FIR filter. Note the system bandwidth is the combination of the digital filter, the anti-alias filter and external signal filter components.

Table 8. FIR Filter Bandwidth

DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)
2.5	1.2
5	2.4
10	4.7
20	13

9.3.9.3 50-Hz and 60-Hz Line Cycle Rejection

In some applications, due the proximity of the ADC signal leads to industrial motors and conductors, coupling of 50-Hz and 60-Hz power line frequencies can occur. The coupled noise can interfere with the signal voltage leading to inaccurate or unstable conversions. The digital filter rejects power-line interference for data rates of 60 SPS and less. Program the filter to tradeoff data rate and conversion latency versus the desired level of line cycle rejection. Table 9 summarizes the 50-Hz and 60-Hz line-cycle rejection based on 2% and 6% tolerance of power-line frequency to ADC clock frequency.

Table 9. 50-Hz and 60-Hz Line Cycle Rejection

DATA RATE (SPS)	FILTER TYPE	DIGITAL FILTER MAGNITUDE (dB)			
		50 Hz ±2%	60 Hz ±2%	50 Hz ±6%	60 Hz ±6%
2.5	FIR	–113	–99	–88	–80
2.5	Sinc1	–36	–37	–40	–37
2.5	Sinc2	–72	–74	–80	–74
2.5	Sinc3	–108	–111	–120	–111
2.5	Sinc4	–144	–148	–160	–148
5	FIR	–111	–95	–77	–76
5	Sinc1	–34	–34	–30	–30
5	Sinc2	–68	–68	–60	–60
5	Sinc3	–102	–102	–90	–90
5	Sinc4	–136	–136	–120	–120
10	FIR	–111	–94	–73	–68
10	Sinc1	–34	–34	–25	–25
10	Sinc2	–68	–68	–50	–50
10	Sinc3	–102	–102	–75	–75
10	Sinc4	–136	–136	–100	–100
16.6	Sinc1	–34	–21	–24	–21
16.6	Sinc2	–68	–42	–48	–42
16.6	Sinc3	–102	–63	–72	–63
16.6	Sinc4	–136	–84	–96	–84
20	FIR	–95	–94	–66	–66
20	Sinc1	–18	–34	–18	–24
20	Sinc2	–36	–68	–36	–48
20	Sinc3	–54	–102	–54	–72
20	Sinc4	–72	–136	–72	–96
50	Sinc1	–34	–15	–24	–15
50	Sinc2	–68	–30	–48	–30
50	Sinc3	–102	–45	–72	–45
50	Sinc4	–136	–60	–96	–60
60	Sinc1	–13	–34	–12	–24
60	Sinc2	–27	–68	–24	–48
60	Sinc3	–40	–102	–36	–72
60	Sinc4	–53	–136	–48	–96

9.3.10 General-Purpose Input/Output (GPIO)

Eight analog inputs can be programmed as GPIO functions (GPIO[0] through GPIO[7]). The GPIO function is a digital input/output with a logic value that is read and written by the GPIODAT data register. The GPIO voltage levels are referenced to the ADC analog power supply voltages, V_{AVDD} and V_{AVSS}. The GPIO input voltage threshold for logic 1 is (V_{AVDD} + V_{AVSS}) / 2. As shown in Figure 74, analog inputs, AIN3 through AINCOM, can be programmed for GPIO function. Register GPIOCON programs the GPIO connection for each pin (1 = connect). Register GPIODIR programs the direction of each pin, either as input or output (0 = output). Register GPIODATA is the GPIO data value register. Note if a GPIO pin is programed as an output, the data value readback is the data that was written to the GPIODAT register, not the pin voltage itself.

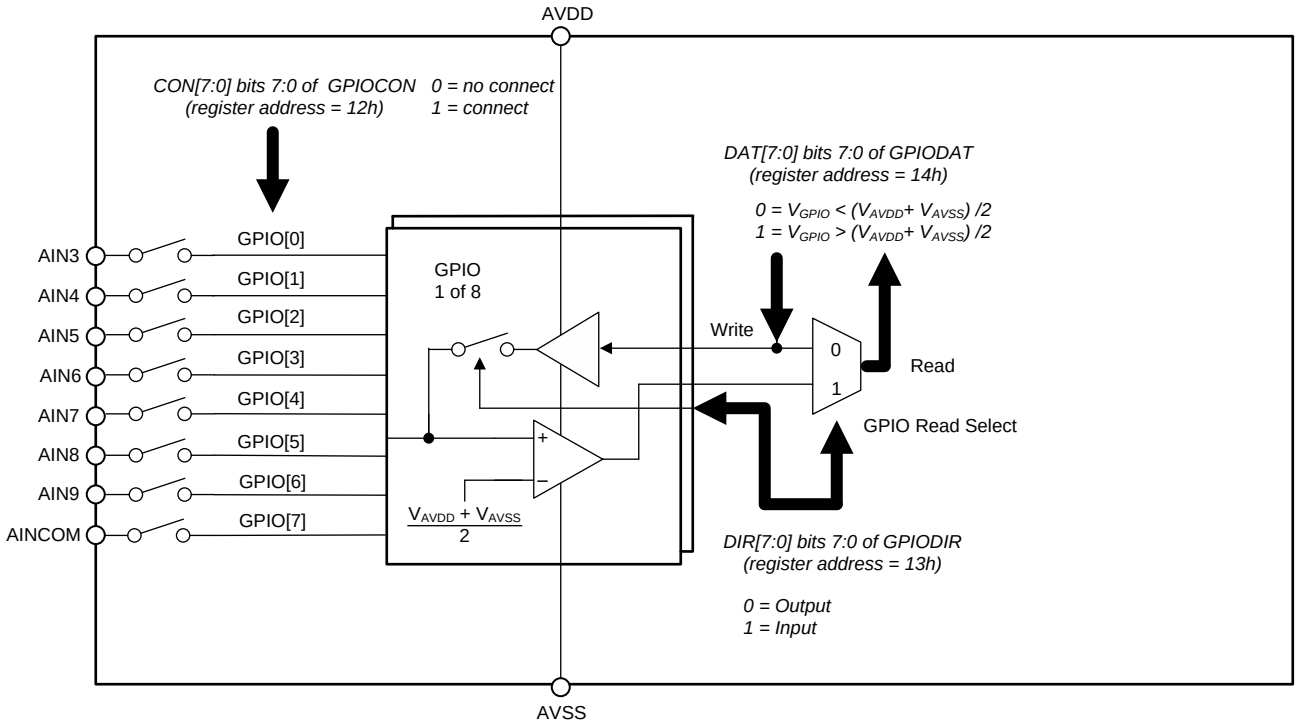


Figure 74. GPIO Block Diagram

9.3.11 Test DAC (TDAC)

The ADC includes a test and verification digital-to-analog converter (TDAC) intended for ADC self-testing and verification. The TDAC is capable of providing combinations of single-ended, differential and/or common mode test signals. The voltages levels generated are suitable to test the ADC under all gains and input configurations.

As shown in Figure 75, the TDAC consists of two independent DACs, TDACP and TDACN. The DACs have separate control registers to program the output voltage. TDACP is programmed by register TDACP and the TDACN is programmed by register TDACN. The TDACP output connects to the ADC1 and ADC2 positive input multiplexer input and TDACN connects to the ADC1 and ADC2 negative input multiplexer. The OUT1 and OUT2 bits can be programmed to connect the TDAC outputs to pins AIN6 and AIN7. The TDAC outputs are unbuffered and should not be loaded. The TDAC reference voltage is the analog supply (V_{AVDD} - V_{AVSS}), therefore, the output levels scale with the analog power supply. Note the Chop option must be disabled to test the ADC with the TDAC.

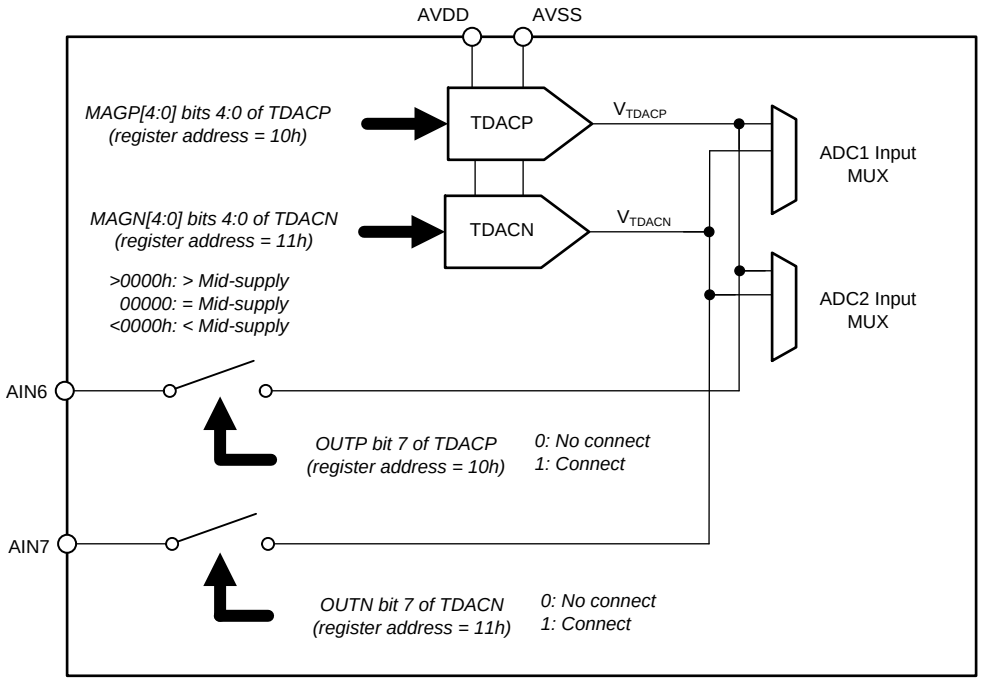


Figure 75. Test DAC Block Diagram

Table 10 shows the TDAC output levels and the corresponding output impedance. The TDAC settings are binary-weighted to corresponds to the binary ADC gains. To generate a single ended voltage, set TDACN = 00h to fix this voltage to mid-supply. TDACP can be set above and below the TDACN voltage to generate positive and negative single-ended voltages. Differential signals are generated by setting both TSIGP and TSIGN to symmetric values centered at code value = 00h = 0 V output. For example, use code values equal to 01h/11h, 02h/12h, and so forth. A common mode voltage is generated by setting TDACP and TDACN to the same value.

Table 10. TDAC Output Voltage

TDAC1, TDAC2 REGISTER VALUES	DIVIDER RATIO (V/V)	OUTPUT VOLTAGE (V), 5-V SUPPLY(1)	OUTPUT VOLTAGE (V), ±2.5V SUPPLY(1)	OUTPUT IMPEDANCE (kΩ)
09h	0.9	4.5	2	2.9
08h	0.7	3.5	1	6.4
07h	0.6	3	0.5	8.7
06h	0.55	2.75	0.25	10
05h	0.525	2.625	0.125	10.7
04h	0.5125	2.5625	0.0625	9.6
03h	0.50625	2.53125	0.03125	8.7
02h	0.503125	2.515625	0.015625	8.1
01h	0.5015625	2.5078125	0.0078125	7.8
00h	0.5	2.5	0	7.5
11h	0.4984375	2.4921875	–0.0078125	7.8
12h	0.496875	2.484375	–0.015625	8.1
13h	0.49375	2.46875	–0.03125	8.7
14h	0.4875	2.4375	–0.0625	9.6
15h	0.475	2.375	–0.125	10.7
16h	0.45	2.25	–0.25	10
17h	0.4	2	–0.5	8.7
18h	0.3	1.5	–1	6.4
19h	0.1	0.5	–2	2.9

(1) Output voltages relative to V_{AVSS}.

9.3.12 ADC2 (ADS1263)

The ADS1263 includes an auxiliary 24-bit delta-sigma ADC (ADC2). ADC2 operation is independent of ADC1, with independent selection of input channel, reference voltage, sample rate and channel gain. All input configurations (channel select, IDAC, level shift, sensor bias) are available to ADC2. ADC2 can be used to perform main channel (ADC1) cross-checking measurements for diagnostics purposes, redundant channel measurements, system background measurements or temperature compensation of the primary sensor (such as thermocouple cold junction compensation). Using data rates of 10, 100 and 400 SPS for both ADCs, ADC2 can perform virtual parallel conversions with ADC1 on the same input channel.

As shown in Figure 76, the ADC2 consists of an input signal multiplexer followed by a high impedance PGA. The input multiplexer has the same functionality as ADC1 input multiplexer. The sensor bias current source or a 10 MΩ bias resistor can be connected to the multiplexer output. The sensor bias can be connected to either of the ADCs. ADC2 provides gains of 1, 2, 4 ,8, 16, 32, 64 and 128. Depending on the gain settings, the ADC2 gains are either implemented in the PGA or in the modulator. For gains of 1, 2 and 4, the PGA is bypassed and the gain is performed in the modulator. For gains of 8, 16, 32, 64 and 128 the modulator gain is fixed at gain = 4, and the gains are performed in the PGA. The PGA drives an inherently stable, second-order delta-sigma modulator. The modulator output data is filtered and down sampled by a programmable decimation, sinc3 digital filter. The digital filter provides data rates of 10, 100, 400 or 800 SPS with 24-bit resolution. A user programed calibration block follows the digital filter. The calibration block consists of 16-bit offset correction and 16-bit full scale correction registers. The ADC2 reference multiplexer selects from one of three external reference input pairs, the analog power supply or the internal reference. The reference input is buffered to minimize errors caused by external circuit loading.

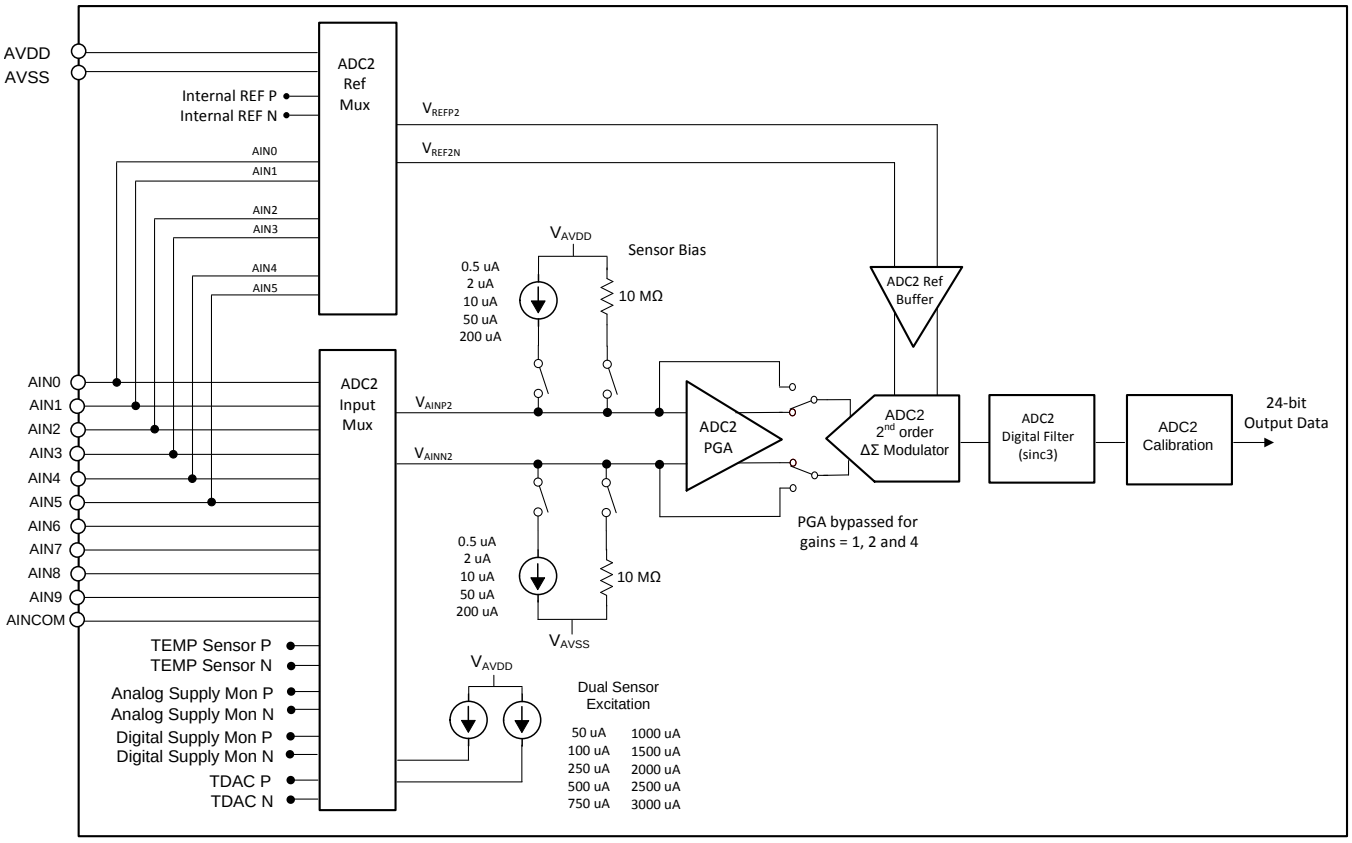


Figure 76. ADC2 Block Diagram

9.3.12.1 ADC2 Inputs

ADC2 features an independent input multiplexer with identical channel selections of ADC1. As shown in Figure 49, all the external and internal inputs available to ADC2. The ADC2 positive input is programmed by the value of MUXP2[3:0] bits (register ADC2MUX) and the negative input is programmed by the value of the MUXN2[3:0] bits of same ADC2MUX register. The ADC2MUX register address is 16h.

9.3.12.2 ADC2 PGA

ADC2 features a low drift, low noise CMOS PGA. The ADC2 PGA is bypassed for gains = 1, 2 and 4. Therefore, for these gains the input signal is connected directly to the buffered modulator input.

9.3.12.3 ADC2 Reference

ADC2 requires a reference voltage for operation. As shown in Figure 77, the ADC2 reference multiplexer is used to select from one of the external reference sources on pins AIN0 to AIN5, the internal 2.5 V internal reference or the analog power supply. The external reference are P and N pairs for reference positive and reference negative. The external reference input pairs are pins AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, for reference positive/reference negative, respectively.

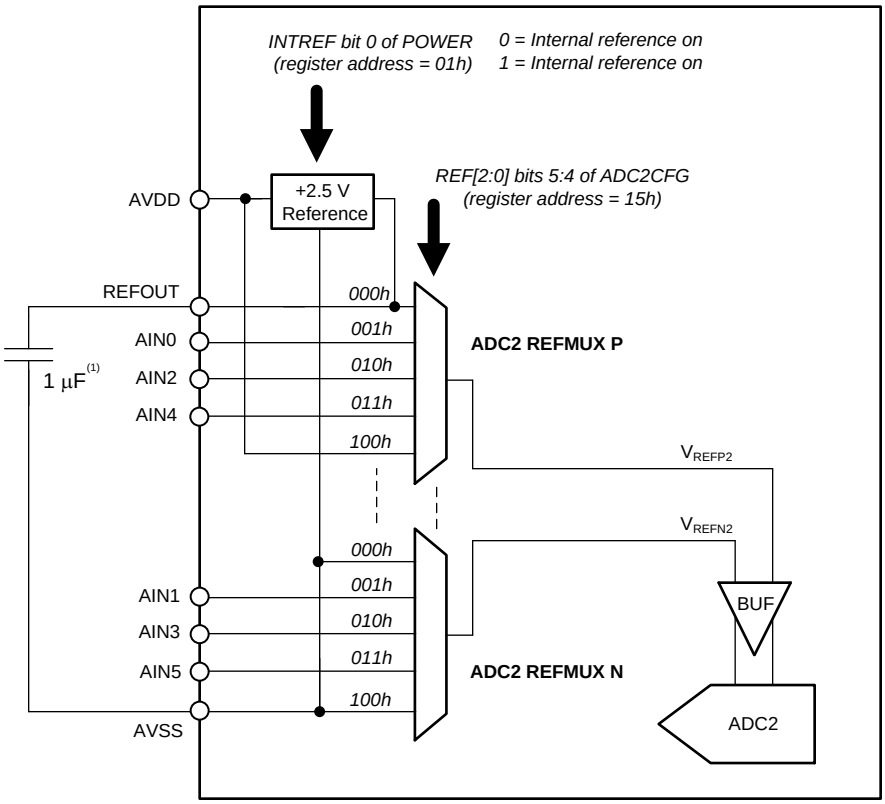


Figure 77. ADC2 Reference Multiplexer

9.3.12.4 ADC2 Modulator

ADC2 is an inherently stable, second-order, ΔΣ modulator. The modulator samples the analog input voltage at $f_{MOD2} = f_{CLK}/144 = 51.2$ kHz and converts the analog input to a 1's density bit-stream output. The digital filter receives the 1's density bit stream output where it is filtered and decimated to yield the final conversion result.

9.3.12.5 ADC2 Digital Filter

The ADC2 digital filter receives the modulator output and produces a 24-bit digital output. The digital filter low-pass filters and down-samples the modulator data to yield the final data rate. The ADC2 digital filter consist of two stages. The first stage is a fixed decimation sinc3 filter that derives data rate of 800 SPS. The second stage is a sinc1 filter with variable decimation that derives the remaining data rates of 400, 100 and 10 SPS, as illustrated in Figure 78. The second stage is bypassed for data rate of 800 SPS Table 11 shows the sinc filter data rates and decimation ratio that corresponds to the second filter stage. The data rate is programmed by the DR2[1:0] bits of register ADC2CFG. The default sample rate of ADC2 is 10 SPS.

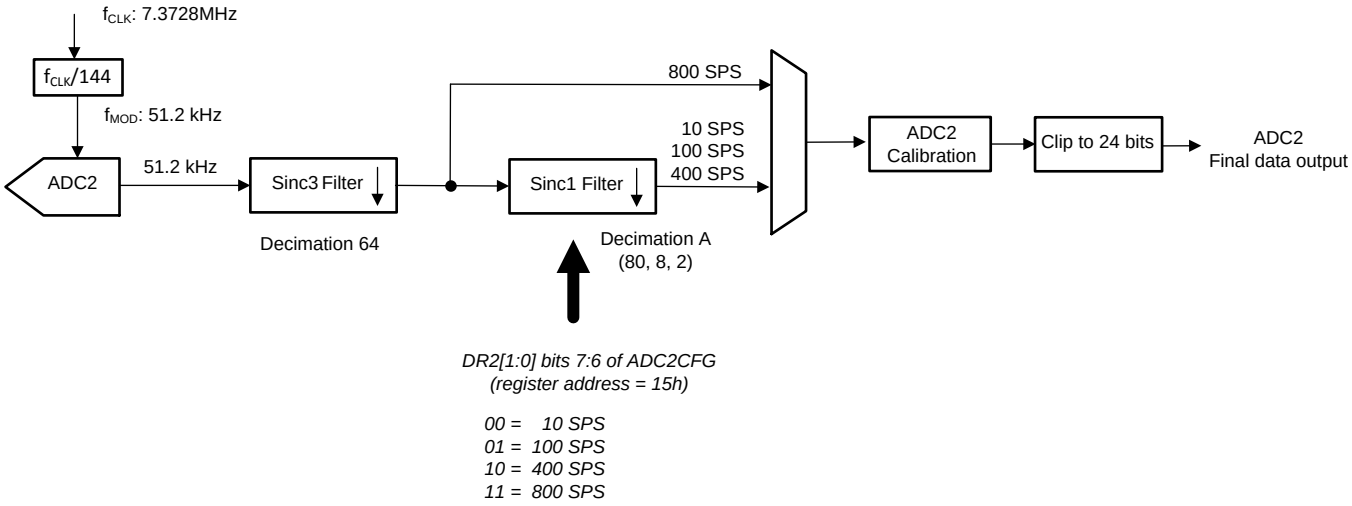


Figure 78. ADC2 Digital Filter Block Diagram

Table 11. ADC2 Data Rates and Filter Decimation

DATA RATE (SPS)(1)	DR2[1:0] BITS OF REGISTER ADC2CFG	DECIMATION A
10	00	80
100	01	8
400	10	2
800	11	—

(1) f_{CLK} = 7.3728 MHz. The data rate scales with f_{CLK}.

The low pass nature of the ADC2 sinc filter establishes the overall frequency response. The frequency response is given by Equation 14:

$$\left|H_{(f)}\right| = \left|H_{sinc^3}(f)\right| \times \left|H_{sinc^1}(f)\right| = \left|\frac{\sin\left[\frac{9216\pi f}{f_{CLK}}\right]}{64\times\sin\left[\frac{144\pi f}{f_{CLK}}\right]}\right|^3 \times \left|\frac{\sin\left[\frac{9216\pi f A}{f_{CLK}}\right]}{A\times\sin\left[\frac{9216\pi f}{f_{CLK}}\right]}\right| \quad (14)$$

where

- f = Input frequency
- f_{CLK} = ADC clock (7.3728 MHz)
- A = Decimation ratio

Figures Figure 79 through Figure 83 show the frequency response of different ADC2 data rates. Nulls are located in the frequency response at the data rate and at data rate multiples. Figure 79 (data rate = 10 SPS) has nulls in the frequency response at 50 Hz and 60 Hz and their multiples. Therefore, the rate of 10 SPS provides rejection of power line cycle frequencies. Figure 80 shows filter response detail of frequencies centered around 50 Hz and 60 Hz.

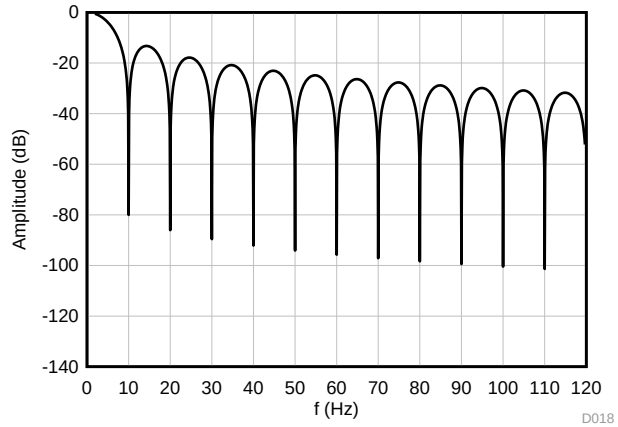


Figure 79. ADC2 10 SPS Frequency Response

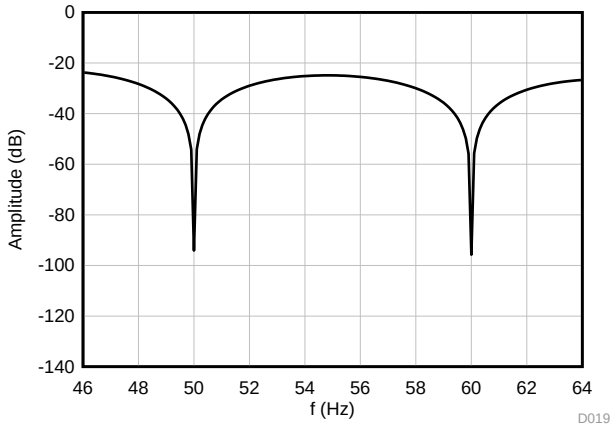


Figure 80. ADC2 10 SPS Frequency Response 50/60 Hz Detail

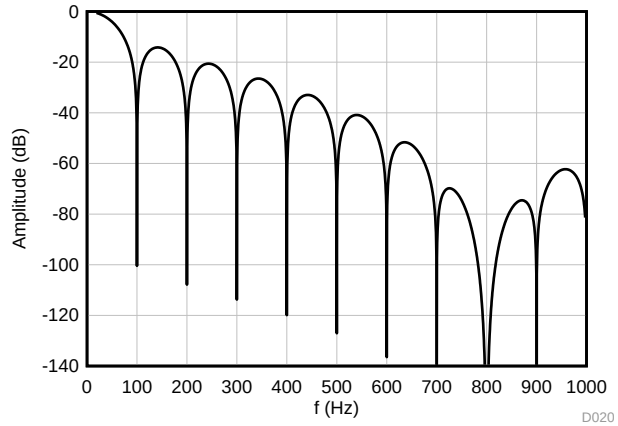


Figure 81. ADC2 100 SPS Frequency Response

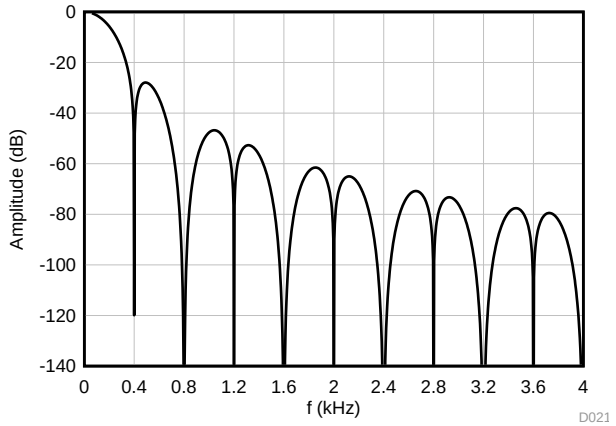


Figure 82. ADC2 400 SPS Frequency Response

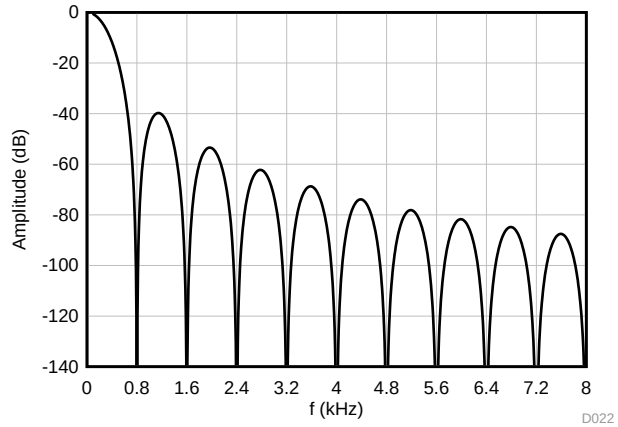


Figure 83. ADC2 800 SPS Frequency Response

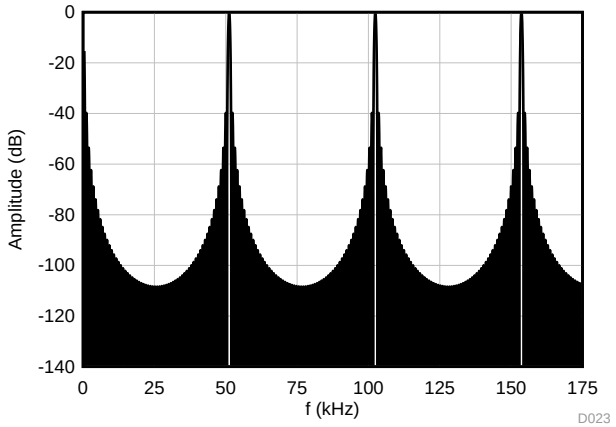


Figure 84. ADC2 Frequency Response to 175 kHz

The ADC digital filter provides attenuation of frequencies greater than ½ of the data rate (Nyquist frequency) to minimize out of band interference folding back to the bandwidth of interest. As with all digital filters, response images appear at frequency multiples of the filter's input frequency ($f_{MOD} = f_{CLK}/144 = 51.2$ kHz). Figure 84 shows the frequency response to 175 kHz for 800 SPS. The response near DC is the desired signal bandwidth. Note how the filter response repeats at multiplies of 51.2 kHz. The filter response repeats at frequencies: $N \cdot f_{MOD} \pm f_{DR}$, where N = 1,2,3... The digital filter attenuates signal or noise up to the frequency where the response repeats. However, signal or noise that may be present within the frequency bands where the response repeats can alias into the passband; unless attenuated by an analog filter. Often, the simple the RC analog filter is sufficient to reject these frequencies.

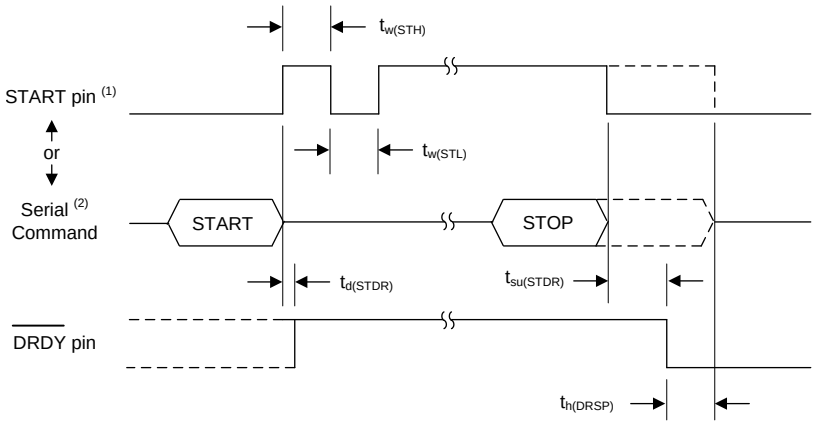
9.4 Device Functional Modes

9.4.1 Conversion Control

ADC1 conversions are controlled by the START pin or by serial commands. If using commands to control ADC1 conversions, keep the START pin low to avoid possible contentions between the START pin control and commands.

ADC2 conversions are controlled by serial commands only. The START2 command starts the ADC2 conversions and conversions continue until the STOP2 command is received. The default setting of ADC2 is idle mode (stop conversion mode).

ADC1 has two conversion modes: continuous or pulse. Continuous conversion mode converts indefinitely until stopped by the user. Pulse conversion mode performs one conversion after the START pin is taken high or after the START command is sent. The conversion mode is programmed by the RUNMODE bit (bit 6 of register MODE0). Figure 85 show the START and STOP timing to control ADC conversions.



(1) START and $\overline{DRDY}$ pins apply only to ADC1 operation.

(2) START and STOP opcodes take effect on the 7th SCLK falling edge.

(3) START and STOP opcodes:

- START1 for ADC1: 08h or 09h
- START2 for ADC2: 0Ch or 0Dh
- STOP1 for ADC1: 0Ah or 0Bh
- STOP2 for ADC2: 0Eh or 0Fh

Figure 85. ADC1 START and STOP Conversion Timing

Table 12. ADC1 START and STOP Conversion Timing Requirement

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(STH)}$	START pin high: pulse width		4		t_{CLK} (1)
$t_{w(STL)}$	START pin low to *re-start* conversion: pulse width		4		t_{CLK}
$t_{d(STDR)}$	START condition to $\overline{DRDY}$ high : delay time	Pulse conversion mode		2	t_{CLK}
$t_{su(STDR)}$	STOP condition to $\overline{DRDY}$ low stopping additional conversions: set-up time	Continuous conversion mode	16		t_{CLK}
$t_{h(DRSP)}$	$\overline{DRDY}$ low to STOP condition to continue current conversion: hold time	Continuous conversion mode		16	t_{CLK}

(1) $t_{CLK} = 1 / f_{CLK}$

9.4.1.1 Continuous Conversion Mode

ADC1 conversions are started by taking the START pin high or by sending the START1 command. The ADC continues with conversions until stopped by taking the START pin low or by sending the STOP1 command. If a conversion is in progress and a new conversion is started by the START pin or the START command, the conversion stops and re-starts. DRDY is driven high if conversions are re-started. DRDY is driven low when the conversion data is ready. See Figure 85 for STOP to DRDY timing requirements in order to stop further conversions.

9.4.1.2 Pulse Conversion Mode

In Pulse conversion mode, the ADC1 performs one conversion each time the START pin is taken high or the START1 command is sent. After the first conversion completes, further conversions are automatically stopped. If during an on-going conversion the START pin is taken high again or the START command is resent, the conversion is stopped and re-started. The DRDY output is driven high to indicate conversion start and is driven low when the conversion data is ready. If a STOP command is sent during an ongoing conversion, the command has no effect as the ADC completes the conversion.

9.4.2 Conversion Latency

The digital filter averages and down-samples data from the modulator to provide the final data rate (rate reduction). The order of the digital filter affects the amount of data averaging and in turn, the time delay of the conversion (or filter latency). The FIR and sinc1 filter modes are zero latency providing the conversion result in single cycle. The higher order sinc filters (sinc2, 3, 4, 5) have more than one conversion latency and therefore require more conversion cycles to provide fully settled data. Tradeoffs can be made between 50-Hz and 60-Hz line cycle rejection verses conversion latency by selection of the sinc filter order. Higher order sinc filter increases the magnitude of the 50-Hz and 60-Hz line cycle rejection but also increases the filter latency. Filter latency can be an important consideration when multiplexing (scanning) through input channels. To ensure fully settled conversions after changing channels, start a new conversion for each channel by the START pin or command. Note if the multiplexer is changed during ongoing conversions, the conversion is stopped and re-started at the time multiplexer register is changed.

Table 13 lists the filter latency of the *first* conversion after START. Note the conversion latency is dependent on the filter setting. The conversion latency is illustrated in Figure 86. Parameter $t_{d(STDR)}$ shows the latency from START to conversion data ready ($\overline{DRDY}$ low). Note that settled data is provided assuming the analog input is settled prior to START. After the first conversion is completed (in continuous conversion mode), subsequent conversions occur at the nominal data rate. The latency values are for the conversion time delay parameter programmed to off (DELAY[3:0] = 000).

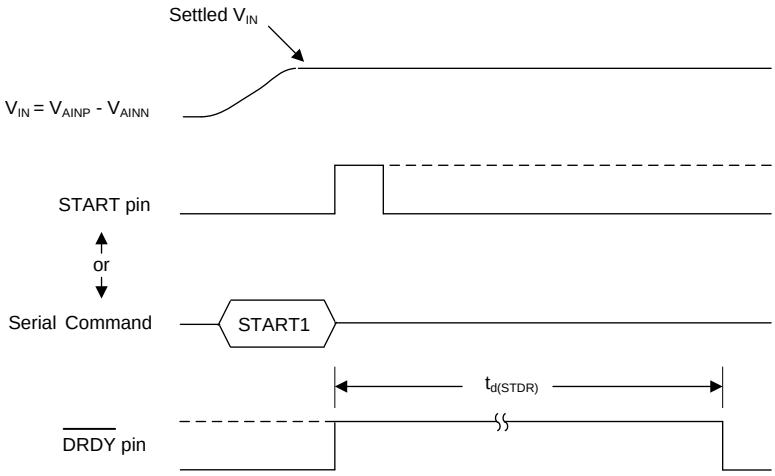


Figure 86. Conversion Latency after START

Table 13. Conversion Latency, $t_{d(STDR)}$

DATA RATE (SPS)	CONVERSION LATENCY(1) (ms)					
	SINC1	SINC2	SINC3	SINC4	SINC5	FIR
2.5	400.4	800.4	1,200	1,600	—	402.2
5	200.4	400.4	600.4	800.4	—	202.2
10	100.4	200.4	300.4	400.4	—	102.2
16.6	60.35	120.4	180.4	240.4	—	—
20	50.35	100.4	150.4	200.4	—	52.22
50	20.35	40.42	60.42	80.42	—	—
60	17.02	33.76	50.42	67.09	—	—
100	10.35	20.42	30.42	40.42	—	—
400	2.855	5.424	7.924	10.42	—	—
1200	1.188	2.091	2.924	3.758	—	—
2400	0.771	1.258	1.674	2.091	—	—
4800	0.563	0.8409	1.049	1.258	—	—
7200	0.494	0.702	0.841	0.980	—	—
14400	—	—	—	—	0.424	—
19200	—	—	—	—	0.337	—
38400	—	—	—	—	0.207	—

(1) Chop and IDAC rotation off, DELAY[3:0] = 0000.

If using chop or IDAC rotation modes, the latency of the first conversion increases. The latency of chop and IDAC rotation modes is shown in Equation 15 and Equation 16.

Chop *or* IDAC rotation mode: latency = 2 · ($t_{d(STDR)}$ + DELAY[3:0] value) (15)

Chop *and* IDAC rotation modes: latency = 4 · ($t_{d(STDR)}$ + DELAY[3:0] value) (16)

In addition, chop or IDAC rotation mode can reduce the nominal conversion data rate depending on the programmable delay time value. Note the 50-Hz and 60-Hz response nulls are not altered by chop or IDAC rotation modes. Equation 17 shows the effective data rate with the DELAY parameter.

Chop or IDAC rotation mode data rate = 1 / ($t_{d(STDR)}$ + DELAY[3:0] value) (17)

If the input signal should change while the ADC is continuously converting, the data is a mix of old and new data, as shown in Figure 87. The filter latency values for *settled data* ($t_{d(STDR)}$) while continuously converting is shown in Table 14 The filter latency values listed in the table ($t_{d(STDR)}$) assume the analog input is settled prior to the start of the first whole conversion period.

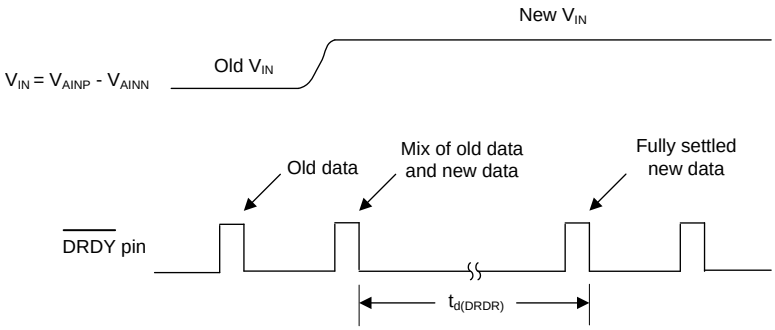


Figure 87. Continuous Conversion Latency

Table 14. Continuous Conversion Latency

DIGITAL FILTER	CONVERSION DELAY $t_{d(DRDR)}$ (1 / DR)(1)
FIR	1
Sinc1	1
Sinc2	2
Sinc3	3
Sinc4	4
Sinc5	5

(1) Chop and IDAC rotation modes off.

9.4.3 Programmable Time Delay

When a conversion is started, the ADC delays 52 µs before beginning the actual start of the conversion. The delay is provided to allow the analog anti-alias filter to settle. In some cases, additional time may be necessary to allow for external settling. Additional time, beginning when the START pin is taken high (or at the START command) to the actual start of the conversion, can be programmed by the DELAY[3:0] bits of register MODE. The programable range is 8.7 µs to 8.8 ms in binary steps. As an alternative to using the programmable delay time, the user can delay the initiation conversion start such as may be required after an ADC configuration change. Note for CHOP of IDAC rotation modes, additional delay time may be necessary to allow for external settling effects; see Table 34 for the delay settings.

9.4.4 Serial Interface

The ADC has an SPI compatible, bi-directional serial interface that is used to read the conversion data; and to configure and control the ADC. The serial interface consists of four control lines: $\overline{CS}$, SCLK, DIN and DOUT/$\overline{DRDY}$. If the ADC is the only device connected to the SPI™ bus, the $\overline{CS}$ input can be tied low, resulting in a minium of three control signals for communications, SCLK, DIN and DOUT/$\overline{DRDY}$. The ADC has a data ready output signal ($\overline{DRDY}$) that asserts regardless if the interface is selected. The $\overline{DRDY}$ functionality is also integrated with the DOUT/$\overline{DRDY}$ pin.

9.4.4.1 Chip Select ($\overline{CS}$)

$\overline{CS}$ is an active low input that enables the ADC serial interface for communication. $\overline{CS}$ must be low during the entire data transaction. When $\overline{CS}$ is high, the serial interface is reset, SCLK input activity is ignored (blocking input commands) and the DOUT/$\overline{DRDY}$ output pin enters a high-impedance state. ADC conversions are not affected by the $\overline{CS}$ input. If the serial bus is dedicated to the ADC, the $\overline{CS}$ pin may be tied low. Tying the $\overline{CS}$ pin low permanently enables the ADC serial interface. Note the $\overline{DRDY}$ output pin always asserts during conversions and is not affected by $\overline{CS}$.

9.4.4.2 Serial Clock (SCLK)

The serial interface clock is a noise filtered, Schmidt-triggered input used to clock data into and out of the ADC. Input data to the ADC is latched on the falling SCLK edge and data output from the ADC is updated on the rising SCLK edge. Return SCLK low after the data sequence is complete. Even though the SCLK is a noise immune, Schmidt-trigger input, it is recommended to keep SCLK as clean as possible to prevent unintentional SCLK transitions. Avoid ringing and voltage over-shoot on the SCLK input. A series termination resistor placed at the SCLK drive pin can often help to reduce ringing.

9.4.4.3 Data Input (DIN)

DIN is the serial data input pin to the ADC. DIN is used to input commands and register data to the ADC. The ADC latches input data on the falling edge of SCLK. During read-back of ADC data, when no command is intended, keep DIN low.

9.4.4.4 Data Output/Data Ready (DOUT/$\overline{DRDY}$)

DOUT/$\overline{DRDY}$ is a dual-function output pin. The pin functions as the digital data output and as the ADC1 data-ready indication. When $\overline{CS}$ is high, the DOUT/$\overline{DRDY}$ pin is in high-impedance mode (tri-state). Data is updated on the rising edge of SCLK. As a data ready indicator, the DOUT/$\overline{DRDY}$ pin transitions low at the same time with the $\overline{DRDY}$ pin. Therefore, the user can monitor either the DOUT/$\overline{DRDY}$ pin or the $\overline{DRDY}$ pin to determine when ADC1 data are ready. Note that $\overline{CS}$ must be low to monitor DOUT/$\overline{DRDY}$ as the data ready indicator.

9.4.4.5 Serial Interface Auto-Reset

The $\overline{CS}$ input resets the serial interface when taken high. Applications that tie the $\overline{CS}$ pin low do not have the ability to reset the serial interface by this pin. If a false SCLK occurs, such as caused by a noise pulse or clocking glitch, the serial interface could advance a bit position(s) resulting in loss of synchronization to the external microcontroller. If loss of synchronization occurs, the interface may not respond correctly until reset. For applications that tie $\overline{CS}$ ow, the ADC provides an automatic feature to reset the serial interface in the event of a glitch. As shown in Figure 88, after an SCLK low to high transition is detected by the ADC (either caused by a glitch or by a normal SCLK input), the remaining 7 data bits must be completed within 65536 f_{CLK} cycles (approximately 8.9 ms). If the remaining 7 bits are not sent within 65536 f_{CLK} cycles, the serial interface resets. After reset, the interface is ready for the next transaction 4 f_{CLK} cycles later. If the 7 bits are transmitted within the 65536 f_{CLK} cycles, no reset occurs and the SCLK detection cycle is restarted. To force a serial timeout, hold SCLK low for 65536 f_{CLK} cycles. The serial interface timeout function is enabled by the setting the TIMEOUT bit = 1 (Bit 3 of register INTERFACE). The default mode is off.

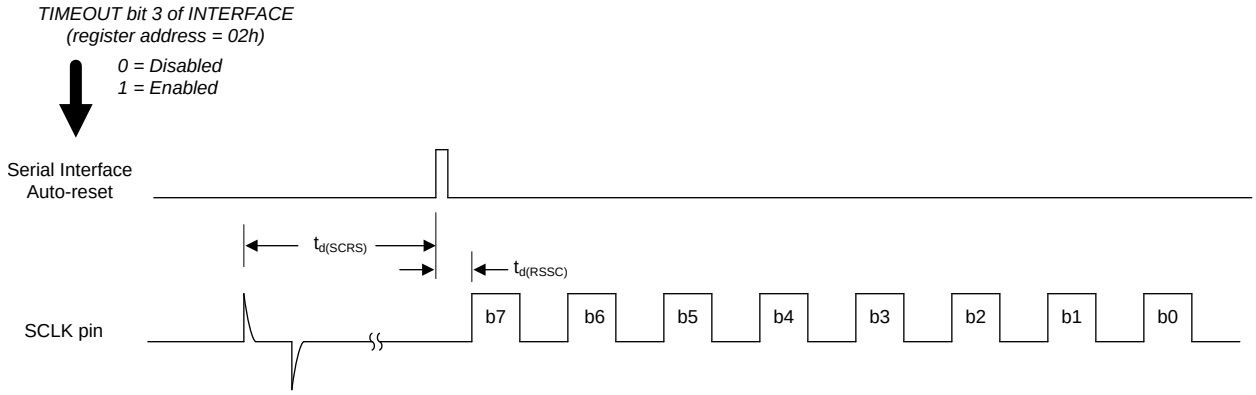


Figure 88. Serial Interface Auto-Reset

Table 15. Auto-Reset Timing Requirement

PARAMETER		TEST CONDITIONS	MIN	UNIT
$t_{d(SCRS)}$	SCLK↑transition to interface reset : delay time	TIMEOUT bit =1	65536	t_{CLK} (1)
$t_{d(RSSC)}$	Serial interface reset to first SCLK↑: delay time	TIMEOUT bit =1	4	t_{CLK}

(1) $t_{CLK} = 1 / f_{CLK}$.

9.4.5 Data Ready (DRDY)

DRDY is an output that transitions low to indicate when *ADC1* conversion data is ready for retrieval. Figure 89 depicts the DRDY operation. Initially, DRDY is high at power-on. When converting, the state of DRDY depends on the conversion mode (continuous or pulse) and whether the conversion data is retrieved or not. In Continuous conversion mode, after DRDY goes low, DRDY is driven high on the first SCLK falling edge. If data is not read, DRDY remains low and then pulses high 16 f_{CLK} cycles before the next DRDY falling edge. The data must be retrieved before the next DRDY falling edge otherwise the data is over-written by new data and previous data is lost. In Pulse mode, DRDY is driven high when a conversion is started and goes low when the conversion data is ready. DRDY remains low until the next conversion is started.

The DOUT/DRDY output operates similarly to DRDY. DOUT/DRDY transitions low when ADC1 conversion data is ready. If data is not retrieved, the DOUT/DRDY pin stays low and is pulsed high for 16 f_{CLK} cycles at the next data ready. Note that CS must be low to enable the DOUT/DRDY pin.

New conversion data can also be determined by software polling. In software polling, the user reads either ADC1 or ADC2 conversion data and polls the STATUS byte ADC1 or ADC2 data ready bits. The bit(s) are set if conversion data has been updated since ADC1 or ADC2 data was last read by the user, otherwise the bit(s) are cleared. Note that new ADC2 data can only be determined by polling the ADC2 bit.

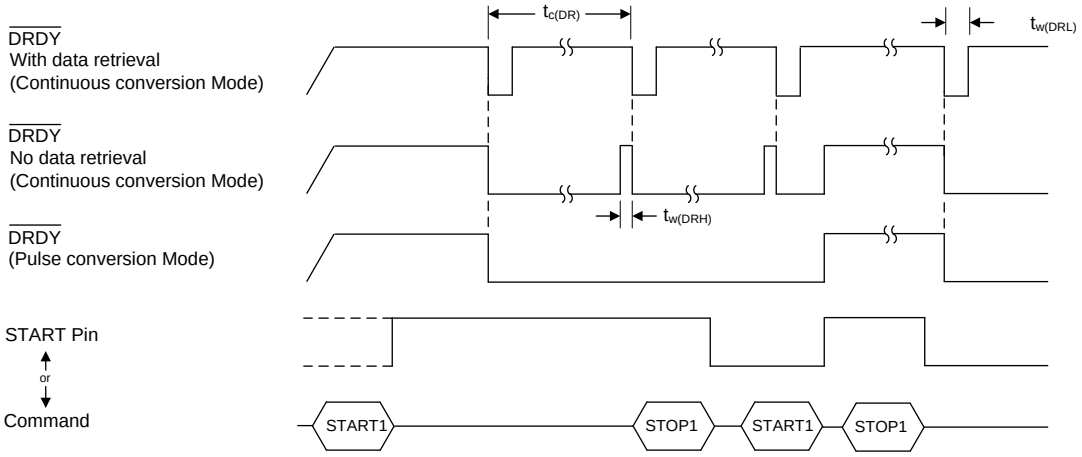


Figure 89. DRDY Operation

Table 16. DRDY Timing Characteristics

PARAMETER		TEST CONDITIONS	TYP	UNIT
$t_{c(DR)}$	DRDY↓ to DRDY↓ conversion time: DRDY period	After first conversion	1	1/data rate
$t_{w(DRL)}$	DRDY↓ to DRDY↑: delay time	With data retrieval, Continuous conversion mode	DRDY drives high on first falling SCLK edge	
$t_{w(DRH)}$	DRDY pulse high: pulse width	No data retrieval, Continuous conversion mode,	16	t_{CLK} (1)

(1) $t_{CLK} = 1 / f_{CLK}$.

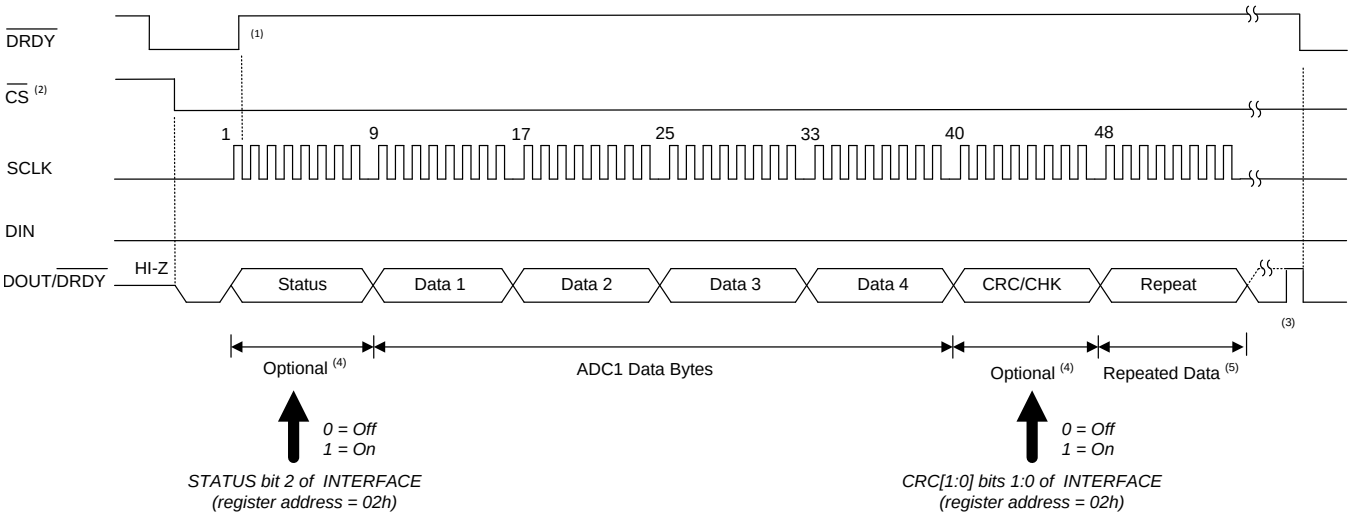
9.4.6 Read Conversion Data

ADC1 data can be read by two methods: Read data direct and Read data by command. The ADC writes new conversion data to the output shift register and also writes the data to an internal data holding register. Because two registers hold the conversion data, data can be read either from the output shift register (direct mode) or read from the data holding register (command mode). Reading data from the data holding register (command mode) does not necessarily require synchronization to DRDY. ADC2 data can only be read from the ADC2 data holding register (command mode).

9.4.6.1 Read Data Direct

In this method of data retrieval, the conversion data is shifted out directly from the output shift register. No opcode is necessary. Read data direct requires that no serial activity occurs from DRDY low to the readback itself or the data can be invalid. Because the interface is full duplex, commands are decoded during the readback. If no command is intended, keep the DIN pin low during the readback. If an input command is sent during the read-back, the ADC executes the command and this may result in data interruption depending on the command. The data readback operation must be completed 16 f_{CLK} cycles before the next DRDY or the old data will be overwritten with new data. It is recommended to synchronize the data read-back to DRDY or to DOUT/DRDY to ensure the data is read before the next DRDY falling edge. If new ADC1 conversion data is ready during an on-going data or configuration register read or write operation, data is not loaded to the output register and is written only to the data holding register. The conversion data can retrieved later from the holding register by sending a read command.

As shown in Figure 90, the ADC1 data field is 4, 5 or 6 bytes long, depending on programming. The data field consists of an optional status byte, four bytes of conversion data and an optional CRC/checksum byte. After all the bytes are read, the data byte sequence is repeated starting with the first byte in the sequence. The user can read the same data multiple times in each conversion interval in order to compare the data to help verify error free communications.



(1) In Continuous conversion mode, DRDY returns high on the first SCLK falling edge. In Pulse Conversion mode, DRDY stays low until the next conversion is started.

(2) CS may be tied low . If CS is low, DOUT/DRDY asserts low at the same time as DRDY.

(3) Data read must be completed before DOUT/DRDY and DRDY goes high (16 t_{CLK} before new data ready).

(4) The STATUS and CRC/CHK bytes are optional.

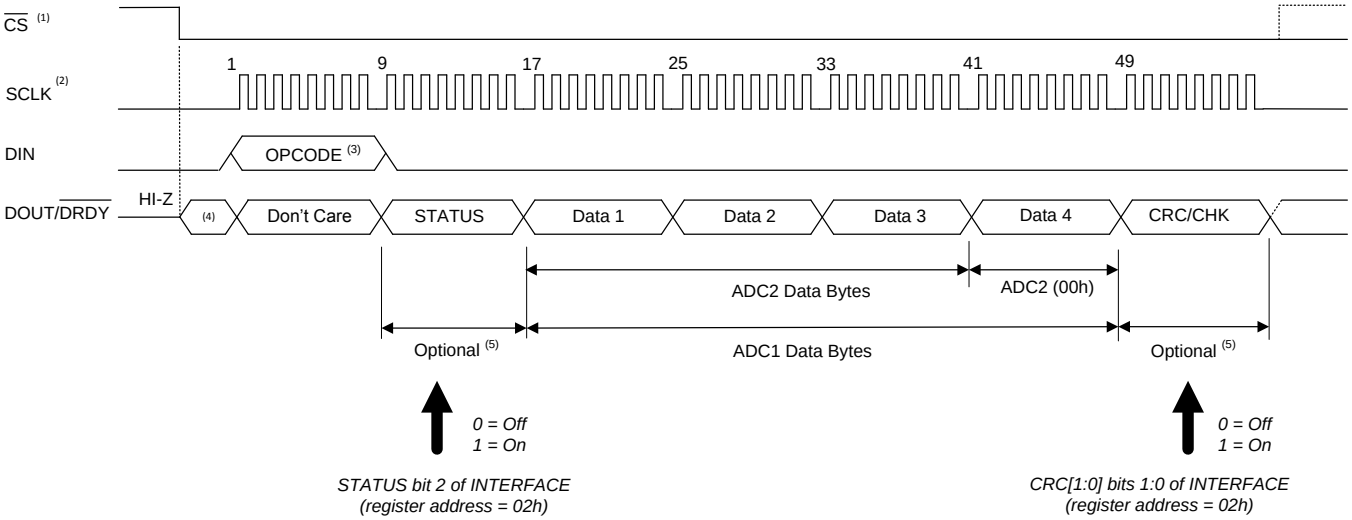
(5) The data bytes are repeated by continuing SCLK.

Figure 90. Data Read Direct

9.4.6.2 Read Data by Command

In this method of data retrieval, a command is sent to read ADC1 or ADC2 data. When the command is sent, the data is retrieved from the holding register for readback. The command method does not require synchronizing to $\overline{DRDY}$ and the data can be read at anytime. The ADC1 and ADC2 bits of the status byte can be polled to determine new data. If the ADC1 or ADC2 status bit(s) are 1, the ADC1 or ADC2 data is new since the last ADC1 or ADC2 read operation. If data is read again before the data is updated new, the ADC bit(s) are 0 and the previous data is returned. ADC2 data can only be read by the command method.

Figure 91 shows the Read data by command sequence. The output data MSB begins on the first rising edge of SCLK after the command. The output data field can be 4, 5 or 6 bytes long, depending on user programming. The data field consists of an optional status byte, four bytes of conversion data and an optional CRC/checksum byte. The ADC2 data block consists of the optional status byte, 3 bytes of data, a fixed value byte that is equal to 00h and the optional CRC/checksum byte. The read data opcode must be sent for each read operation.



(1) $\overline{CS}$ may be tied low. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low with $\overline{DRDY}$.

(2) In Continuous Conversion mode, $\overline{DRDY}$ returns high on the first SCLK falling edge of sending the opcode. For Pulse Conversion mode, $\overline{DRDY}$ stays low until the next conversion is started.

(3) Read ADC1 command byte = 12h or 13h, Read ADC2 command byte = 14h or 15h

(4) DOUT/$\overline{DRDY}$ is driven low with $\overline{DRDY}$, If a read operation occurs after $\overline{DRDY}$ falling edge, then DOUT can be high or low.

(5) The STATUS and CRC/CHK bytes are optional.

Figure 91. Read Data by Command

9.4.6.3 Data Byte Sequence

The ADC1 data sequence can be 4, 5 or 6 bytes long, depending if the optional STATUS and CRC/CHK bytes are included. The entire data sequence consists of the status byte, four bytes of the 32-bit conversion word and the CRC/CHK byte. The ADC2 data sequence is the same except the conversion data is 3 bytes long (24-bit word) followed by a fixed value byte (00h). If the STATUS byte is not enabled, the remaining bytes are left shifted.

9.4.6.3.1 Status byte (STATUS)

The STATUS byte is the first byte in the sequence. The STATUS byte reports the status of ADC1 and ADC2 data, ADC1 PGA and low reference alarms, ADC clock and RESET status. The status byte is enabled by the STATUS bit of register INTERFACE (bit 2 of register 02h). Figure 92 and Table 17 shows the STATUS byte bits.

Figure 92. Status Byte (STATUS)

7	6	5	4	3	2	1	0
ADC2	ADC1	EXTCLK	REF_ALM	PGAL_ALM	PGAH_ALM	PGAD_ALM	RESET
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Status Byte (STATUS) Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC2	R	0 - ADS1262 x - ADS1263	**ADC2 Data** This bit indicates the status of ADC2 conversion data 0: ADC2 data not new since the last ADC2 read operation 1: ADC2 data new since the last ADC2 read operation
6	ADC1	R	x	**ADC1 Data** This bit indicates the status of ADC1 conversion data 0: ADC1 data not new since the last ADC1 read operation 1: ADC1 data new since the last ADC1 read option
5	EXTCLK	R	x	**ADC Clock** This bit indicates the ADC clock source 0: ADC clock is internal 1: ADC clock is external
4	REF_ALM	R	x	**ADC1 Low Reference Alarm**(1) This bit is the low reference voltage alarm of ADC1. The alarm bit is set if V_{REF} ≤ 0.4 V, typical. 0: No alarm 1: Low reference alarm
3	PGAL_ALM	R	x	**ADC1 PGA Output Low Alarm** (1) This bit is the ADC1 PGA absolute low voltage alarm. The alarm is set if the absolute voltage of either PGA output is less than V_{AVSS} + 0.2 V. See PGA Absolute Output-Voltage Monitor 0: No alarm 1: PGA low voltage alarm
2	PGAH_ALM	R	x	**ADC1 PGA Output Positive Alarm** (1) This bit is the ADC1 PGA absolute high voltage alarm. The alarm is set if the absolute voltage of either PGA output is greater than V_{AVDD} - 0.2 V. See PGA Absolute Output-Voltage Monitor 0: No alarm 1: PGA high voltage alarm
1	PGAD_ALM	R	x	**ADC1 PGA Differential Output Alarm** (1) This bit is the ADC1 PGA differential output range alarm. The bit is set if the PGA differential output voltage exceeds +105% FS or -105% FS. See PGA Differential Output Monitor 0: No alarm 1: PGA differential range alarm
0	RESET	R	1	**RESET** Indicates device reset. Device reset occurs at power-on, by the RESET/PWDN pin or by the RESET command. This bit is the same as the RESET bit of register POWER Table 32 0: No reset occurred since the RESET bit in POWER register cleared by the user 1: Device reset has occurred

(1) These bits are valid during the readback of ADC1 data only. All other bits are valid during the readback of either ADC1 or ADC2.

9.4.6.3.2 Data Byte Format

ADC1 data is 32 bits, in two's complement format that represents positive and negative values. The data is most significant bit (MSB) first. The data is scaled such that V_{IN} = 0 V results in ideal code value of 00000000h. The ideal positive full scale and negative full scale code values are 7FFFFFFFh + 01h and 80000000h, respectively. See Table 18. In some applications, it may be desired to reduce the 32-bit data to 24-bit data to provide compatibility to 24-bit systems. This can be done by simple truncation (or rounding) of the 32-bit data to 24 bits. See Figure 93 for the ADC1 data byte field.

Table 18. ADC Output Code

INPUT SIGNAL (V)(1)	ADC1 OUTPUT CODE (32 BITS) (2)	ADC2 OUTPUT CODE (24 BITS) (2)
≥ V_{REF} / Gain · (2^{N-1} - 1) / 2^{N-1}	7FFFFFFFh	7FFFFFh
V_{REF} / (Gain · 2^{N-1})	00000001h	000001h
0	00000000h	000000h
–V_{REF} / (Gain · 2^{N-1})	FFFFFFFFh	FFFFFFh
≤ –V_{REF} / Gain	80000000h	800000h

(1) N = 32 (ADC1), N = 24 (ADC2)
(2) Ideal output code, excluding effects of ADC noise, offset, gain and linearity errors.

Figure 93. ADC1 Data Field, 32 bits

31	30	29	28	27	26	25	24
ADC1[31:24]							
R-x							
23	22	21	20	19	18	17	16
ADC1[23:16]							
R-x							
15	14	13	12	11	10	9	8
ADC1[15:8]							
R-x							
7	6	5	4	3	2	1	0
ADC1[7:0]							
R-x							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The ADC2 data is 24 bits in two's complement data format that represents positive and negative code values. The data is output most significant bit (MSB) first. The data is scaled such that a zero voltage input results in ideal code value of 000000h. The ideal positive full scale and negative full scale code values are 7FFFFFh + 01h and 80000h, respectively. See Figure 94 for ADC2 data byte field.

Figure 94. ADC2 Data Field, 24 bits

23	22	21	20	19	18	17	16
ADC2[23:16]							
R-x							
15	14	13	12	11	10	9	8
ADC2[15:8]							
R-x							
7	6	5	4	3	2	1	0
ADC2[7:0]							
R-x							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.4.6.3.3 Checksum byte (CRC/CHK)

The CRC/CHK byte is the last byte in the conversion data sequence. The CRC/CHK byte can be programmed for checksum mode or cyclic redundancy check (CRC) mode. This byte is optional and is enabled by the CRC[1:0] bits of register INTERFACE. The CRC/CHK byte can used to detect transmission errors during data read-back. Figure 95 and Table 19 shows the checksum byte description. Note the CRC/CHK byte is not provided for register data.

Figure 95. Checksum Byte (CRC/CHK)

7	6	5	4	3	2	1	0
SUM[7:0]							
R-x							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Checksum Byte (CRC/CHK) Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SUM[7:0]	R	x	**CRC or Checksum byte** This byte is CRC or Checksum of four ADC1 data bytes; or three ADC2 data bytes

Checksum Mode CRC[1:0] = 01h

In checksum mode, the CRC/CHK byte is the lower 8-bit sum of the data conversion bytes plus an offset value 9Bh. The offset value is added to detect if the DOUT/DRDY has failed in a permanent low state. For ADC1, four data bytes are summed and for ADC2, three data bytes are summed. To verify the correct checksum, the user sums the data bytes plus 9Bh and compares the value read from the ADC. If the checksum values do not match, a data transmission error has occurred. In the event of a data transmission error, the data can be read again for verification. The checksum provides basic levels of error detection that are caused by single bit and limited combinations of multi-bit errors.

Example computation of ADC1 4 data byte checksum calculation:

Data byte 1: 12h

Data byte 2: 34h

Data byte 3: 56h

Data byte 4: 78h

Constant: 9Bh

Checksum value = EBh

CRC Mode CRC[1:0] = 10h

In CRC mode, the CRC/CHK byte is the 8-bit remainder of bitwise exclusive-OR (XOR) of the data bytes by a CRC polynomial. For ADC1, four conversion data bytes are used in the calculation and for ADC2, three conversion data bytes are used. The CRC is based on the CRC-8-ATM (HEC) polynomial:

$X^8 + X^2 + X + 1$.

The nine binary coefficients of the polynomial are: 100000111. The user calculates the CRC by dividing (XOR operation) the data bytes (excluding the CRC itself) with the polynomial and compares the calculated CRC values to the ADC CRC value. If the values do not match, a data transmission error has occurred. In the event of a data transmission error, the data can be read again. The CRC provides a higher level of detection of multiple bit errors.

The following shows a general procedure to compute the CRC value:

1) Left shift the initial ADC1 32-bit data value by 8 bits, with zero's padded the right, creating a new 40-bit data value. This is the starting data value. For ADC2, left shift the 24-bit value to create a new 32-bit data value.

2) Align the MSB of the CRC polynomial (100000111) to the left-most 1-bit position of the data value.

3) Perform XOR operation of the data value with the newly aligned CRC polynomial. The XOR operation creates a new, shorter length value. The bits of the data values that are not in alignment with the CRC polynomial drop down and append to the right of the new XOR result.

4) When the XOR result is less than 100h, the procedure ends, yielding the 8-bit CRC value. Otherwise, continue with the XOR operation at step 2) using the current data value. The number of loop iterations depends on the value of the initial data.

9.4.7 ADC Clock

The ADC requires a clock for operation. The nominal clock frequency is 7.3728 MHz. The output data rate and the corresponding 50-Hz and 60-Hz frequency response nulls scale with clock frequency. Good line-cycle rejection requires an accurate clock frequency. The ADC has three clock operating modes:

1) Internal Oscillator

2) External Clock

3) External Crystal

As depicted in Figure 96, the ADC integrates a clock generator and detection circuit. If no external clock is detected, the internal oscillator is selected. If the external clock is detected, the ADC selects the external clock automatically. The clock operating mode can be verified by reading the EXTCLK bit, bit 5 of the status byte (0 = internal clock).

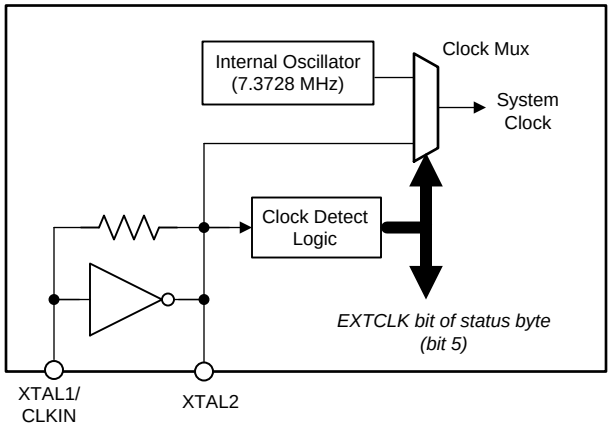


Figure 96. ADC Clock Block Diagram

Figure 97 illustrates the configuration for the three clock modes.

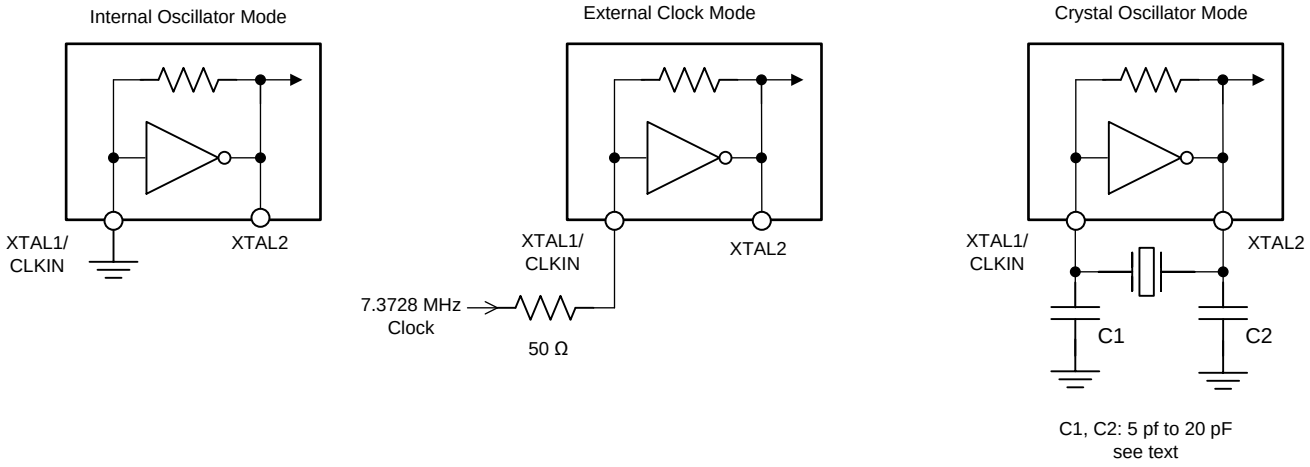


Figure 97. Clock Mode Configurations

9.4.7.1 Internal Oscillator

The ADC integrates an 7.3728-MHz internal oscillator. After ADC power-on, the internal oscillator starts immediately. The internal oscillator is selected by grounding the XTAL1/CLKIN pin. Float the XTAL2 pin . See Figure 97 (Internal Oscillator Mode)

9.4.7.2 External Clock

The ADC can be driven by an external clock. Apply the clock input to the XTAL1/CLKIN pin and float the XTAL2 pin as shown in Figure 97 (External Clock Mode). The ADC automatically detects the external clock. Be sure the external clock is free of overshoot and glitches. A source terminating resistor placed at the external clock buffer often helps to reduce overshoot.

9.4.7.3 Crystal Oscillator

The ADC integrates an oscillator circuit for use with an external crystal. Connect the crystal and load capacitors to the XTAL1/CLKIN and XTAL2 as shown in Figure 97 (crystal oscillator mode). Place the crystal and crystal load capacitors close to the ADC pins using short direct traces. Connect the load capacitors to digital ground. No other external circuit should connect to the crystal oscillator. Table 20 shows approved crystals for use with the ADS1262 and ADS1263. Note the crystal oscillator start-up time has been characterized at 10 ms typical and can be longer depending on the crystal characteristics.

Table 20. Recommended Crystals

MANUFACTURER	FREQUENCY	LOAD CAPACITORS	OPERATING TEMPERATURE RANGE	PART NUMBER
Citizen	7.3728 MHz	18 pF	-40°C to +85°C	HCM497372800ABJT
CTS	7.3728 MHz	18 pF	-40°C to +85°C	ATS073BSM-1E
Abracon	7.3728 MHz	18 pF	-40°C to +125°C	ABLS-7.3728MHZ-K4T

9.4.8 Calibration

The ADC incorporates a number of offset and gain calibration commands as well as user accessible 24-bit offset and 24-bit full scale calibration registers (ADC2 has 16-bit registers). Calibration can be used to correct ADC errors or to correct the overall system errors. Calibration can be performed by sending calibration commands to the ADC, or performed directly by the user (user calibration). User calibration writes the correction values to the calibration registers. The ADC can perform self or system offset calibration, or system full scale calibration. Offset calibration should be performed before full scale calibration. After power-on, wait for the power supplies and reference voltage to fully settle prior to calibration.

9.4.8.1 Offset and Full Scale Calibration Registers

ADC error can be corrected by offset and full-scale (gain) registers. As shown in the Figure 98, the value of the offset calibration register is subtracted from the filter output and then multiplied by the full scale register value divided by 400000h. The data is then clipped to a 32-bit value to provide the final output.

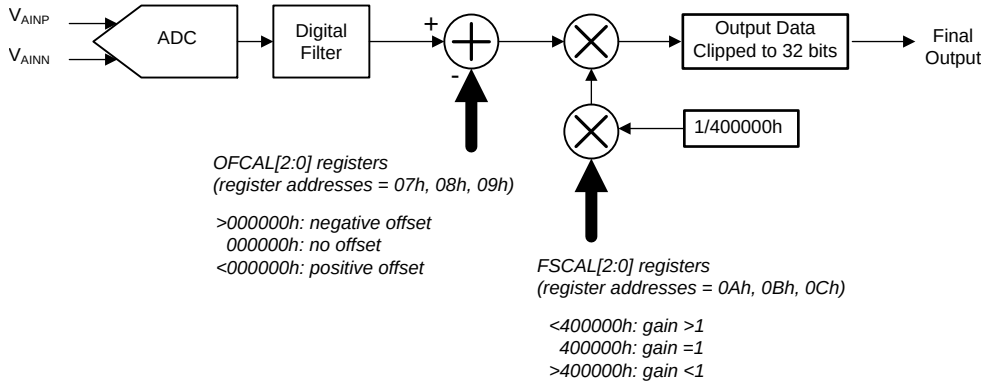


Figure 98. ADC1 Calibration Block Diagram

Equation 18 shows the internal calibration. Note the ADC2 calibration registers are 16 bit. For ADC2, the ADC2FSC[1:0} registers are for full scale calibration and the ADC2OFC[1:0] registers are for offset calibration.

$$\text{ADC1 Final Output Data} = (\text{Filter Output} - \text{OFCAL}[2:0]) \cdot \text{FSCAL}[2:0]/400000\text{h} \quad (18)$$

9.4.8.2 Offset Calibration Registers OFCAL[2:0]

The ADC1 offset calibration register is 24 bits, consisting of three 8-bit registers as shown in Table 21. The offset value is two's complement format with a maximum positive value equal to 7FFFFFh (for negative offset) and a maximum negative value equal to 800000h (for positive offset). The 24-bit register is internally left-shifted to align with the 32-bit data before the subtraction occurs. Register value equal to 000000h has no offset correction. Note that while the offset calibration register allows a wide range of offset values, to prevent over-ranging the ADC, the input signal cannot exceed +106% or -106% of the pre-calibrated range. Table 22 shows example settings of the offset register.

Table 21. ADC1 Offset Calibration Registers

REGISTER	BYTE ORDER	ADDRESS	BIT ORDER							
OFCAL0	LSB	07h	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
OFCAL1	MID	08h	B15	B14	B13	B12	B11	B10	B9	B8
OFCAL2	MSB	09h	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

Table 22. ADC1 Offset Calibration Register Values

OFCAL[2:0] REGISTER VALUE	OFFSET CALIBRATED 32-BIT OUTPUT CODE(1)
000001h	FFFFFF00h
000000h	00000000h
FFFFFFh	00000100h

(1) Ideal output code with shorted input, excluding ADC noise and offset voltage error.

9.4.8.3 Full-Scale Calibration Registers FSCAL[2:0]

The ADC1 full-scale calibration is a 24-bit word consisting of three 8-bit registers, as shown in Table 23. The full scale calibration value is straight binary, normalized to correction factor equal to 1 for a register value equal to 400000h. Table 24 shows register values for selected gain factors. Note that while ADC gain can be corrected for gain error > 1 (resulting in a register value < 400000h, or < 4000h for ADC2). However, to prevent ADC over-range, the input signal cannot exceed +106% or –106% of the pre-calibrated input range. Do not exceed the PGA input range limits during full scale calibration.

Table 23. ADC1 Full-Scale Calibration Registers

REGISTER	BYTE ORDER	ADDRESS	BIT ORDER							
FSCAL0	LSB	0Ah	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
FSCAL1	MID	0Bh	B15	B14	B13	B12	B11	B10	B9	B8
FSCAL2	MSB	0Ch	B23 (MSB)	B22	B21	B20	B19	B18	B17	B16

Table 24. ADC1 Full-Scale Calibration Register Values

FSCAL[2:0] REGISTER VALUE	GAIN FACTOR
433333h	1.05
400000h	1.00
3CCCCCh	0.95

9.4.8.4 ADC1 Offset Self-Calibration (SFOCAL1)

The offset self-calibration command corrects for internal ADC1 offset error. Program the ADC1 input multiplexer register (INPMUX) to 0FFh to force open all input connections prior to sending the command. When the SFOCAL1 self-calibration command is sent, the ADC shorts together the internal PGA inputs, then averages 16 readings to reduce the conversion noise for an accurate calibration. When calibration is complete, the calibration result is written to the 24-bit offset calibration register (OFCAL[2:0]). After calibration, set the input multiplexer to the desired channel.

9.4.8.5 ADC1 Offset System-Calibration (SYOCAL1)

The offset system-calibration command corrects the ADC1 system offset error. For this type of calibration, the user externally shorts the system inputs prior to the command. When the SYSOCAL1 command is sent, the ADC averages 16 readings to reduce conversion noise for an accurate calibration. When calibration is complete, the offset calibration result is written to the 24-bit offset calibration register (OFCAL[2:0]).

9.4.8.6 ADC2 Offset Self-Calibration ADC2 (SFOCAL2)

The offset self-calibration command corrects internal ADC2 offset error. Program the ADC2 input multiplexer register (ADC2MUX) to 0FFh to force open all input connections prior to sending the command. When the SFOCAL2 self-calibration command is sent, the ADC shorts together the internal PGA inputs of ADC2, then averages 16 readings to reduce conversion noise for an accurate calibration. When calibration is complete, the offset calibration result is written to the 16-bit ADC2 offset calibration register ADC2OFC[1:0]. After calibration, set the input multiplexer to the desired channel.

9.4.8.7 ADC2 Offset System Calibration ADC2 (SYOCAL2)

The offset system-calibration command corrects the ADC2 system offset error. For this offset calibration, the user externally shorts the ADC2 inputs prior to sending the command. When the SYOCAL2 command is sent, the ADC averages 16 readings to reduce conversion noise for an accurate calibration. When calibration is complete, the calibration result is written to the 16-bit ADC2 offset calibration register (ADC2OFC[1:0)].

9.4.8.8 ADC1 Full-Scale System Calibration (SYGCAL1)

The full-scale calibration command corrects the ADC1 gain error. To calibrate, apply a positive full scale DC signal to the ADC, wait until the signal is fully settled, and then send the command. When the SYGCAL1 command is sent, the ADC averages 16 readings to reduce conversion noise for an accurate calibration. When calibration is complete, the full scale calibration is computed such that the applied voltage calibrates to positive full scale code value. The computed result is written to the 24-bit offset calibration register (FSCAL[2:0]). The pre-calibrated ADC over- range limit is +106%.

9.4.8.9 ADC2 Full-Scale System Calibration ADC2 (SYGCAL2)

The full-scale system-calibration command corrects the ADC2 full scale error. To calibrate, apply a positive full scale DC signal to ADC2, wait until the signal is fully settled, and then send the command.. When the SYGCAL2 command is sent, the ADC averages 16 readings to reduce conversion noise for an accurate calibration. When calibration is complete, the full scale calibration is computed such that applied voltage calibrates to positive full scale. The computed result is written to the ADC2 16-bit full scale calibration register (ADC2FSC[1:0]). The pre-calibrated ADC over-range limit is 106%.

9.4.8.10 Calibration Command Procedure

The procedure shows the sequence for ADC calibration using commands. It is important that the reference voltage is stable before calibrating the ADC. Perform offset calibration before full scale calibration.

1) Select the desired ADC gain and reference voltage.

2) For offset self-calibration, program the ADC1 or ADC2 input multiplexer register to 0FFh to open all inputs prior to sending the calibration command.

3) For *system* calibration commands, select the input channel and short the external inputs (offset calibration); or apply positive full scale input (full scale calibration). If performing full-scale calibration, the analog inputs cannot exceed ±106% full scale range. Do not exceed the specified absolute or differential PGA input range when calibrating.

4) If calibrating ADC1, start ADC1 conversions by taking the START pin high (or send the ADC1 start command). If calibrating ADC2, start ADC conversions by sending the ADC2 START command.

5) Send the desired calibration command. When the calibration command is received, calibration is started. Keep $\overline{CS}$ low and SCLK low during the calibration time. The calibration time is dependent on the data rate and digital filter mode as shown in Table 25.

6) $\overline{DRDY}$ output goes high at the start of calibration. Note in pulse conversion mode, $\overline{DRDY}$ goes high when the START pin is high.

7) $\overline{DRDY}$ output goes low when calibration is complete. The new offset or full scale calibration values are written to the calibration registers. New conversion data is ready at this time using the new calibration coefficients.

Table 25. Calibration Time (ms)

DATA RATE (SPS)	FILTER MODE (1)					
	SINC1	SINC2	SINC3	SINC4	SINC5	FIR
2.5	6801	7601	8401	9201	—	6805
5	3401	3801	4201	4601	—	3405
10	1701	1901	2101	2300	—	1705
16.6	1021	1141	1261	1381	—	—
20	850.7	951.0	1051	1151	—	854.5
50	340.9	380.9	421.0	460.9	—	—
60	284.1	317.7	350.9	384.4	—	—
100	170.8	190.9	210.9	230.8	—	—
400	43.27	48.43	53.42	58.41	—	—
1200	14.93	16.72	18.40	20.07	—	—
2400	7.845	8.816	9.643	10.48	—	—
4800	4.302	4.858	5.276	5.692	—	—
7200	3.123	3.534	3.815	4.095	—	—
14400	—	—	—	—	1.941	—
19200	—	—	—	—	1.490	—
38400	—	—	—	—	0.812	—

(1) f_{CLK} = 7.3728 MHz. CHOP disabled

9.4.8.11 User Calibration

The user calibration procedure is similar to using calibration commands, except the user computes the calibration values and writes the values to the calibration registers. Before starting user calibration, pre-set the ADC1 or ADC2 offset and full scale registers to 000000h and 400000h (ADC2 = 0000h and 4000h), respectively. For offset calibration, the ADC inputs or system inputs are shorted by the user and N readings are averaged (averaging by N reduces noise for a more accurate calibration). The user writes the average value to the offset calibration registers. The ADC subtracts the value from the conversion result. To calibrate full scale, the user applies a DC calibration voltage that is less than positive full scale to avoid clipped codes (V_{IN} < +FSR) and averages N readings to reduce noise for a more accurate calibration. Full scale calibration is computed as: (Expected Code Value / Actual Code Value) x 400000h (ADC2 = 4000h). If the actual code is higher than the expected value, the calculated calibration value will be less than 400000h and the ADC gain is subsequently reduced. Write the calibration value to the full scale register.

9.4.9 Reset

The ADC is reset in one of three ways:

1) Power-on reset

2) $\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ pin

3) RESET command

When the ADC is reset, the device registers default to initial values and the A/D conversion cycles are restarted. The RESET bit of the status byte and of the POWER register are set to 1 to indicate reset has occurred. Set the RESET register bit to 0 to clear the reset flag. If the RESET bit is equal to 1 after clearing the bit, this indicates the ADC has since occurred a reset.

9.4.9.1 Power-On Reset (POR)

After turn-on of the power supplies, the ADC is held in reset until V_{DVDD}, the internal LDO output (BYPASS pin voltage) and the combined (V_{AVDD} – V_{AVSS}) power supply voltage levels have exceeded their respective POR voltage thresholds. Figure 99 shows the POR sequence. When the power supplies have crossed the level thresholds, the ADC is operational 65536 f_{CLK} cycles later (9 ms typical). Note the 1-uF capacitor connected to the BYPASS pin requires charging at power-on and can result in delay when the ADC is operational. Wait at least 9 ms after the power supplies have fully stabilized before beginning ADC communication.

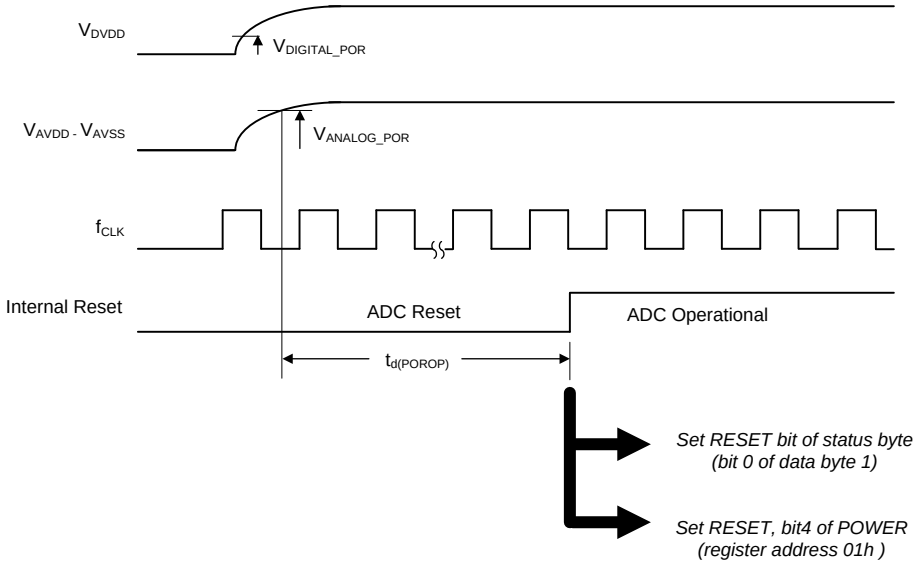


Figure 99. Power-On Reset

Table 26. POR Characteristics

PARAMETER		TEST CONDITIONS	TYP	UNIT
$V_{DIGITAL\_POR}$	Digital power supply POR threshold	V_{DVDD} and V_{BYPASS}	1	V
V_{ANALOG_POR}	Analog power supply POR threshold	V_{AVDD} – V_{AVSS}	3.5	V
$t_{d(POROP)}$	Propagation delay from last POR supply threshold to ADC operational		65536	t_{CLK} (1)

(1) $t_{CLK} = 1 / f_{CLK}$

9.4.9.2 RESET/PWDN pin

The ADC is reset by taking the RESET/PWDN pin low for a minimum 4 f_{CLK} cycles, and then returning the pin high (see Figure 100). Holding the RESET/PWDN pin low for longer than 65536 fclk cycles (9 ms) engages the power down mode. As depicted in the diagram, after RESET/PWDN is taken high, a delay time is required before sending the first serial interface command.

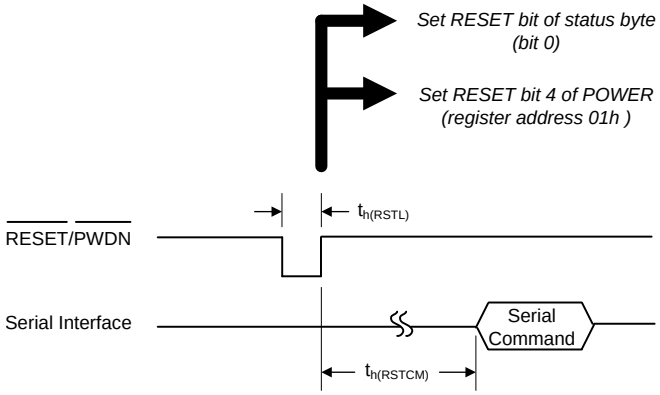


Figure 100. RESET/PWDN Pin Timing

Table 27. RESET/PWDN Pin Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	UNIT
$t_{h(RSTL)}$	RESET/PWDN low for *reset*::Hold time		4	t_{CLK} (1)
	RESET/PWDN low for *power down*: Hold time		65536	t_{CLK}
$t_{h(RSTCM)}$	RESET/PWDN high to serial command: Hold time	after reset	8	t_{CLK}
	RESET/PWDN high to serial command: Hold time	after exiting power down	65536	t_{CLK}

(1) $t_{CLK} = 1 / f_{CLK}$

9.4.9.3 RESET Command

The ADC can be reset by the RESET command (opcode = 06h or 07h). Toggle $\overline{CS}$ high first to ensure reset of the serial interface before sending the command. For applications that tie $\overline{CS}$ low; see the *Serial Interface Auto-Reset* section for information on how to reset the serial interface. After sending the RESET command provide 8 f_{CLK} cycle delay before sending the next command (See Figure 101).

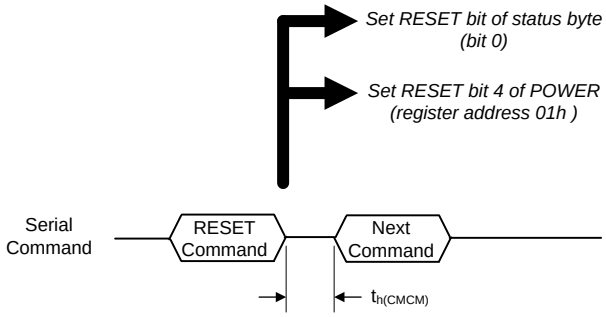


Figure 101. RESET Command Timing

Table 28. RESET Command Timing Requirements

PARAMETER		MIN	UNIT(1)
$t_{h(CMCM)}$	RESET command to next command: hold time	8	t_{CLK}

(1) $t_{CLK} = 1 / f_{CLK}$

9.4.10 Power Down

The ADC can be powered-down by holding the $\overline{RESET}/\overline{PWDN}$ pin low. Pulsing the pin low for less than 65536 clock cycles resets the ADC without engaging power down mode. In power-down mode, the ADC is shutdown including the internal reference. The internal low dropout regulator (LDO) output to the BYPASS pin remains on, typically drawing 25-µA idle current from the DVDD power supply. To exit power down mode, take the pin high.

While in power down mode, maintain the digital inputs at V_{IH} or V_{IL} levels (do not float the inputs). The ADC digital outputs remain driven and the analog inputs and reference inputs are high impedance. When power down mode is exited, the ADC resets, resulting in register reset to default value. Wait the required 65536 f_{CLK} periods (9 ms) before first communication to the ADC. Additionally, allow the internal reference to settle before starting the first conversion.

9.4.11 Chop Mode

The device utilizes a chopper-stabilized PGA and modulator in order to provide very low input voltage offset drift (V_{OS}/dT). However, due to non-idealities arising from chopper-stabilization, a small amount of offset voltage drift can remain. ADC1 incorporates a global chop option to reduce the offset voltage and offset voltage drift to very low levels. When Chop is enabled, the ADC performs two internal conversions to cancel the input offset voltage. The first conversion is taken with normal input polarity. The ADC internally reverses the input polarity for the second conversion. The difference of the two conversions is computed to yield the final corrected result. See Figure 102. The ADC internal offset voltage is modeled as V_{OFS}.

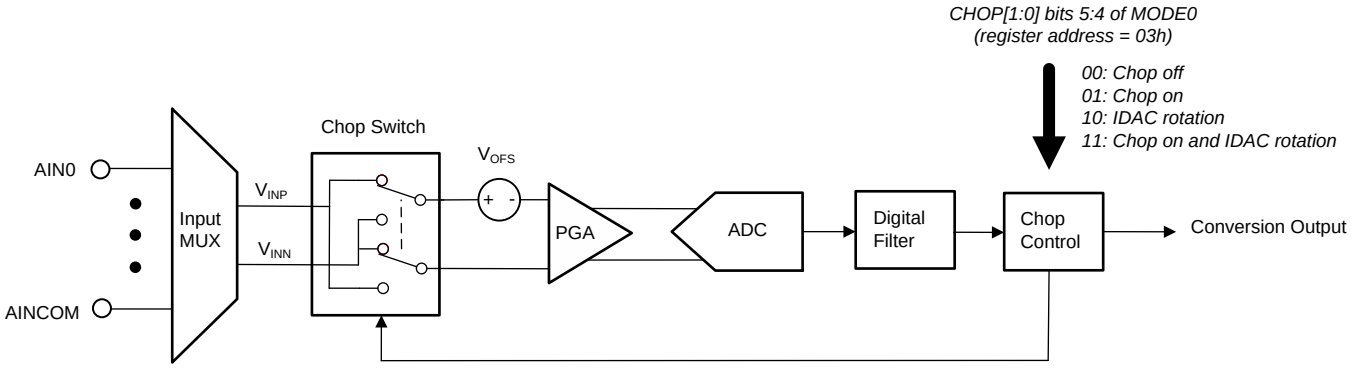


Figure 102. ADC1 Chop Block Diagram

The following is the internal Chop mode sequence.

Internal Conversion 1: V_{AINP} - V_{AINN} - V_{OFS} => First conversion withheld

Internal Conversion 2: V_{AINN} - V_{AINP} - V_{OFS} => Output result 1 = (Conversion 1 - Conversion 2) /2 = V_{AINP} - V_{AINN}

Internal Conversion 3: V_{AINP} - V_{AINN} - V_{OFS} => Output result 2 = (Conversion 3 - Conversion 2) /2 = V_{AINP} - V_{AINN}

Internal Conversion 4: V_{AINN} - V_{AINP} - V_{OFS} => Output result 3 = (Conversion 3 - Conversion 4) /2 = V_{AINP} - V_{AINN}

The internal Chop sequence repeats for N conversions.

Due to the delay required by the digital filter to settle after reversing the inputs, the Chop mode data rate is reduced from the nominal data rate depending on the digital filter order and programmed settling delay. Nevertheless, if the data rate currently used has 50-Hz and 60-Hz frequency response nulls, the null frequencies remain unchanged. Due to averaging of two conversions, the Chop mode also reduces ADC noise by x1.4 factor. In some cases it may be necessary to increase the delay time parameter DELAY[3:0] to allow for settling of external components.

9.5 Programming

Commands are used to access the configuration and data registers and also to control the ADC. Many of the ADC commands are of stand-alone operation (that is, single byte) while the register write and register read commands are multiple-byte, consisting of two opcode bytes plus the register data bytes(s). The commands are listed in Table 29.

Commands can be sent at any time, either during a conversion or while conversions are stopped. However, If register read/write commands are in progress while conversion data is ready, the ADC blocks loading of conversion data to the output shift register. In this case, the data can be read later by RDATA1 command. The $\overline{CS}$ input pin can be taken high between commands; or held low between consecutive commands. $\overline{CS}$ must stay low for the entirety of the command sequence. The command should be completed; or can be terminated by taking $\overline{CS}$ high. Only send the commands that are listed in the table

Table 29. ADC Commands

COMMAND MNEMONIC	COMMAND TYPE	DESCRIPTION	OPCODE 1 BYTE	OPCODE 2 BYTE
NOP	NOP	No Operation	0000 0000 (00h)	
RESET	Control	Reset the ADC	0000 011x (06h or 07h)(1)	
START1		Start ADC1 Conversions	0000 100x (08h or 09h)(1)	
STOP1		Stop ADC1 Conversions	0000 101x (0Ah or 0Bh)(1)	
START2		Start ADC2 Conversions	0000 110x (0Ch or 0Dh)(1)	
STOP2		Stop ADC2 Conversions	0000 111x (0Eh or 0Fh)(1)	
RDATA1	Conversion Data Read	Read ADC1 Data	0001 001x (12h or 13h)(1)	
RDATA2		Read ADC2 Data	0001 010x (14h or 15h)(1)	
SYOCAL1	Calibration	ADC1 System Offset Calibration	0001 0110 (16h)	
SYGCAL1		ADC1 System Gain Calibration	0001 0111 (17h)	
SFOCAL1		ADC1 Self Offset Calibration	0001 1001 (19h)	
SYOCAL2		ADC2 System Offset Calibration	0001 1011 (1Bh)	
SYGCAL2		ADC2 System Gain Calibration	0001 1100 (1Ch)	
SFOCAL2		ADC2 Self Offset Calibration	0001 1110 (1Eh)	
RREG	Register Data Read and Write	Read Registers	001r rrrr (20h+000r rrrr)(2)	000n nnnn(3)
WREG		Write Registers	010r rrrr (40h+000r rrrr)(2)	000n nnnn(3)

(1) x = do not care
(2) r rrrr = register address
(3) n nnnn = number of registers to read or write minus 1

9.5.1 NOP (no operation) Command

The NOP command opcode is 00h. Hold the DIN pin low for the NOP command.

9.5.2 RESET Command

The RESET command resets the ADC operation and resets the device registers to default. See RESET Command.

9.5.3 START1, STOP1, START2, STOP2 Commands

These commands start and stop the conversions of ADC1 and ADC2. See Conversion Control.

9.5.4 RDATA1, RDATA2 Command

These command are used to read ADC1 or ADC2 conversion data from the respective data holding buffers. See Read Conversion Data .

9.5.5 SYOCAL1, SYGCAL1, SFOCAL1, SYOCAL2, SYGCAL2, SFOCAL2 Commands

These commands are used to calibrate ADC1 or ADC2. See Calibration.

9.5.6 RREG Command

The RREG command is used to read the device configuration register data. The register data may be read one register at a time or read as a block of register data. The starting register address may be any register in the map. The RREG opcode consists of two bytes. The first byte specifies the starting register address: 001r rrrr: where r rrrr is the starting register address. The second opcode byte is the number of registers to read (minus 1): 000n nnnn: where n nnnn is the number of registers to read minus 1. After the read command is sent, the ADC responds with one or more register data bytes, most significant bit first. If the byte count exceeds the last register address, the ADC begins to output zero data (the address pointer does not wrap). During the register read operation, if ADC1 data is ready, the conversion data is not loaded to the output shift register to avoid data contention. However, the conversion data can be later retrieval by the RDATA1 command. Once the register read command has been started, further commands are disabled until one of the following conditions:

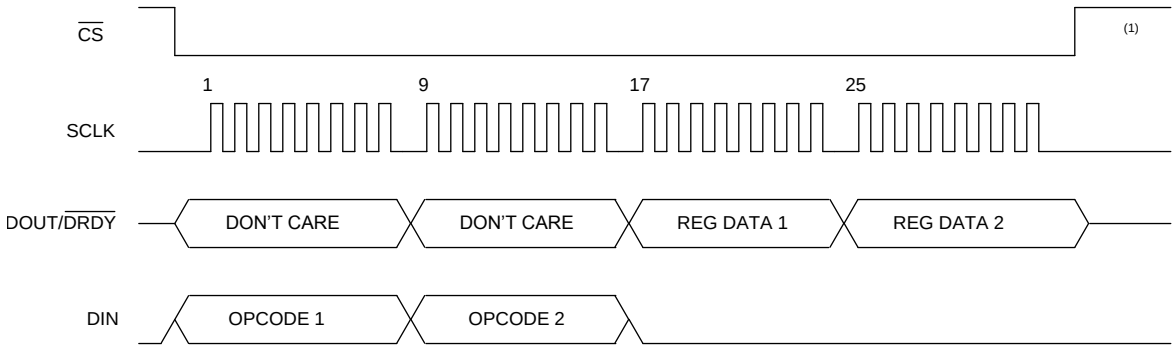
1) The read operation is completed

2) The read operation is terminated by taking $\overline{CS}$ high

3) The read operation is terminated by a serial interface auto-timeout

4) The ADC is reset by toggling the $\overline{RESET}$/$\overline{PWDN}$ pin

Figure 103 depicts a two register read operation. For example, the required opcodes to read data from two registers starting at register MODE2 (address = 05h) are: OPCODE1 = 25h and OPCODE2 = 01h. Keep the DIN input low after the two opcode bytes are sent.



(1) $\overline{CS}$ can be set high or kept low between commands. If kept low, the command must be completed.

Figure 103. Read Register Sequence

9.5.7 WREG Command

The WREG command is used to write the device configuration register data. The register data may be written one register at a time or as a block of register data. The starting register address may be any register in the map. The WREG opcode consists of two bytes. The first byte specifies the starting register address: 010r rrrr: where r rrrr is the starting register address The second opcode byte is the number of registers to write (minus 1): 000n nnnn: where n nnnn is the number of registers to write minus 1. The following byte(s) is the register data, most significant bit first. If the byte count exceeds the last register address, the ADC ignores the data (the address pointer does not wrap). During the register write operation, if ADC1 data is ready, the ADC blocks the loading of data to the output shift register. However, the conversion data can be retrieved later by the RDATA1 command. After the register write command has been started further commands are disabled until one of these conditions occur:

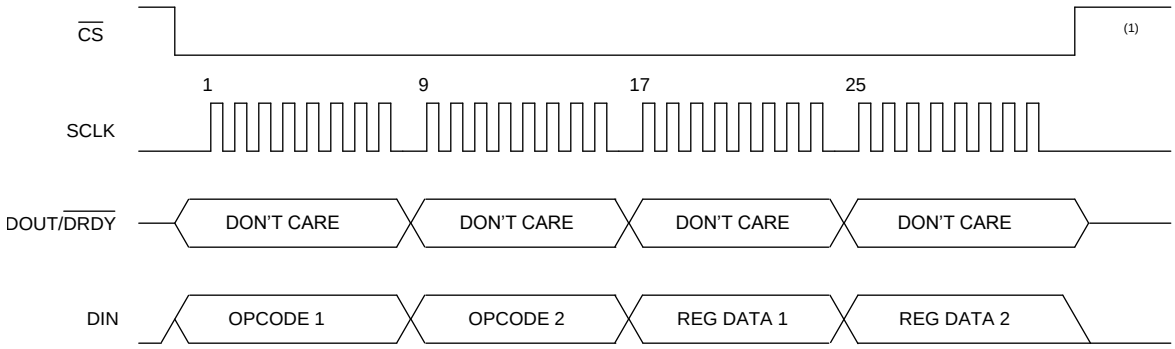
1) The write operation is completed

2) The write operation is terminated by taking $\overline{CS}$ high

3) The write operation is terminated by a serial interface auto-timeout

4) The ADC is reset by toggling the $\overline{RESET}$/$\overline{PWDN}$ pin

Figure 104 depicts a two register write operation. For example, the required opcodes to write data to two registers starting at register MODE2 (address = 05h) are: OPCODE1 = 45h and OPCODE2 = 01h.



(1) CS can be set high or kept low between commands. If kept low, the command must be completed.

Figure 104. Write Register Sequence

In the above example, the MODE2 and INPMUX registers are modified. Typically, register changes take effect immediately after the data is written. However, if the registers are part of a group, then the data is written only after all data for the grouped registers in the write block have been sent. The data for MODE2 and INPMUX is written only after the data for INPMUX is sent. See Register Map for those registers that are grouped when writing data.

9.6 Register Map

The ADS1262 register map consists of 21, 8-bit registers. The ADS1263 has six additional registers totaling 27 registers. Registers with addresses 15h through 1Ah apply exclusively to the ADC2. Collectively, the registers are used to configure and control the ADC to the desired mode of operation. The registers are accessed through the serial interface by the use of the RREG and WREG register read and write commands. At power-on or reset, the registers default to their initial settings (shown in the *DEFAULT* column, Table 30).

Writing new data or changing data of certain registers results in restart of ADC conversions. The registers that result in conversion restart (either ADC1 or ADC2) are shown in the ADC Restart column in the table. Additionally, register data can be written as a continuous block of data. If data are written as a block, the data of certain registers will take effect as soon as the data is shifted in, while the data of other registers are buffered and the data are written to these registers when the write register command is completed. The registers that update as a group are identified in *group update* column in the table. The group update registers that pertain to ADC1 operation are labeled group 1. The group update registers that pertain to ADC2 operation are labeled group 2. Updating registers as a group minimizes the ADC recovery time after a configuration change. Note that the $\overline{\text{DRDY}}$ output is driven high when ADC1 is restarted.

Table 30. Configuration Register Map

ADDR	REGISTER	DEFAULT	ADC RESTART	GROUP UPDATE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	xxh			DEV_ID[2:0]			REV_ID[4:0]				
01h	POWER	11h			0	0	0	RESET	0	0	VBIAS	INTREF
02h	INTERFACE	05h			0	0	0	0	TIME OUT	STATUS	CRC[1:0]	
03h	MODE0	00h	ADC1	Group1	REFREV	RUN MODE	CHOP[1:0]		DELAY[3:0]			
04h	MODE1	80h	ADC1	Group1	FILTER[2:0]			SBADC	SBPOL	SBMAG[2:0]		
05h	MODE2	04h	ADC1	Group1	BYPASS	GAIN[2:0]			DR[3:0]			
06h	INPMUX	01h	ADC1	Group1	MUXP[3:0]				MUXN[3:0]			
07h	OFCAL0	00h			OFC[7:0]							
08h	OFCAL1	00h			OFC[15:8]							
09h	OFCAL2	00h			OFC[23:16]							
0Ah	FSCAL0	00h			FSC[7:0]							
0Bh	FSCAL1	00h			FSC[15:8]							
0Ch	FSCAL2	40h			FSC[23:16]							
0Dh	IDACMUX	BBh	ADC1	Group2	MUX2[3:0]				MUX1[3:0]			
0Eh	IDACMAG	00H	ADC1	Group2	MAG2[3:0]				MAG1[3:0]			
0Fh	REFMUX	00H	ADC1	Group2	0	0	RMUXP[2:0]			RMUXN[2:0]		
10h	TDACP	00H			OUTP	0	0	MAGP[4:0]				
11h	TDACN	00H			OUTN	0	0	MAGN[4:0]				
12h	GPIOCON	00H			CON[7:0]							
13h	GPIODIR	00H			DIR[7:0]							
14h	GPIODAT	00H			DAT[7:0]							
15h	ADC2CFG	00H	ADC2	Group	DR2[1:0]		REF2[2:0]			GAIN2[2:0]		
16h	ADC2MUX	01H	ADC2	Group	MUXP2[3:0]				MUXN2[3:0]			
17h	ADC2OFC0	00H			OFC2[7:0]							
18h	ADC2OFC1	00H			OFC2[15:8]							
19h	ADC2FSC0	00H			FSC2[7:0]							
1Ah	ADC2FSC1	40H			FSC2[15:8]							

9.6.1 Device Identification Register (offset = 00h) [reset = x]

Figure 105. Device Identification Register (ID)

7	6	5	4	3	2	1	0
DEV_ID[2:0]			REV_ID[4:0]				
R-x			R-x				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. Device Identification Register (ID) Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DEV_ID[2:0]	R	x	**Device ID register**. 000: ADS1262 001: ADS1263
4:0	REV_ID[4:0]	R	x	**Revision ID register** *Note: the chip revision ID can change without notification*

9.6.2 Power Register (offset = 01h) [reset = 11h]

Figure 106. Power Register (POWER)

7	6	5	4	3	2	1	0
RESERVED			RESET	RESERVED		VBIAS	INTREF
R-0h			R/W-1h	R-0h		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Power Register (POWER) Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	**Reserved** Always write 000
4	RESET	R/W	1h	**Reset** Indicates ADC reset has occurred. This bit can be cleared by the user. 0: No reset has occurred since the bit last cleared by the user 1: Reset has occurred (default)
3:2	RESERVED	R	0h	**Reserved** Always write 00
1	VBIAS	R/W	0h	**VBIAS** Enables the internal level shift voltage to the AINCOM pin. VBIAS = (V_{AVDD} + V_{AVSS})/2 0: Disabled (default) 1: VBIAS enabled
0	INTREF	R/W	1h	**INTREF** Enables the 2.5 V internal voltage reference. Note the IDAC and temperature sensor require the internal voltage reference. 0: Disabled 1: Internal reference enabled (default)

9.6.3 Interface Register (offset = 02h) [reset = 05h]

Figure 107. Interface Register (INTERFACE)

7	6	5	4	3	2	1	0
RESERVED				TIMEOUT	STATUS	CRC[1:0]	
R-0h				R/W-0h	R-1h	R/W-1h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. Interface Register (INTERFACE) Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0h	**Reserved** Always write 00h
3	TIMEOUT	R/W	0h	**TIMEOUT** Enables the serial interface automatic time-out mode 0: Disabled (default) 1: Enable the interface automatic time-out
2	STATUS	R/W	1h	**STATUS** Enables the inclusion of the STATUS byte during conversion data read-back 0: Disabled 1: STATUS byte included during conversion data read-back (default)
1:0	CRC[1:0]	R/W	1h	**CRC** Enables the inclusion of the CRCCHK byte during conversion data read-back 00: CRC/CHK byte disabled 01: Enable *Checksum* byte during conversion data read-back (default) 10: Enable *CRC* byte during conversion data read-back 11: Reserved

9.6.4 Mode0 Register (offset = 03h) [reset = 00h]

Figure 108. Mode0 Register (MODE0)

7	6	5	4	3	2	1	0
REFREV	RUNMODE	CHOP[1:0]		DELAY[3:0]			
R/W-0h	R/W-0h	R/W-0h		R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Mode0 Register (MODE0) Field Descriptions

Bit	Field	Type	Reset	Description
7	REFREV	R/W	0h	**REFREV** Reverses the ADC1 reference multiplexer output P and N polarity 0: Normal polarity of reference multiplexer output (default) 1: Reverse polarity of reference multiplexer output
6	RUNMODE	R/W	0h	**RUNMODE** Selects the ADC conversion (run) mode 0: Continuous conversion (default) 1: Pulse conversion (one shot conversion)
5:4	CHOP[1:0]	R/W	0h	**CHOP** Enables the ADC chop and IDAC rotation options 00: Input chop and IDAC rotation disabled (default) 01: Input chop enabled 10: IDAC rotation enabled 11: Input chop *and* IDAC rotation enabled
3:0	DELAY[3:0]	R/W	0h	**DELAY** Provides delay from user conversion start to the beginning of the actual conversion 0000: no delay (default) 0001: 8.7 µs 0010: 17 µs 0011: 35 µs 0100: 69 µs 0101: 139 µs 0110: 278 µs 0111: 555 µs 1000: 1.1 ms 1001: 2.2 ms 1010: 4.4 ms 1011: 8.8 ms 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved

9.6.5 Mode1 Register (offset = 04h) [reset = 80h]

Figure 109. Mode1 Register (MODE1)

7	6	5	4	3	2	1	0
FILTER[2:0]			SBADC	SBPOL	SBMAG[3:0]		
R/W-80h			R/W-0h	R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. Mode1 Register (MODE1) Field Descriptions

Bit	Field	Type	Reset	Description
7:5	FILTER[2:0]	R/W	4h	**DIGITAL FILTER** Configures the ADC digital filter 000: Sinc1 mode 001: Sinc2 mode 010: Sinc3 mode 011: Sinc4 mode 100: FIR mode (default) 101: Reserved 110: Reserved 111: Reserved
4	SBADC	R/W	0h	**Sensor bias ADC connection** Selects the ADC to connect the sensor bias 0: Sensor bias connected to ADC1 mux out (default) 1: Sensor bias connected to ADC2 mux out
3	SBPOL	R/W	0h	**Sensor bias polarity** Selects the sensor bias for pull-up or pull-down 0: Sensor bias pull-up mode (AIN_P pulled high, AIN_N pulled low) (default) 1: Sensor bias pull-down mode (AIN_P pulled low, AIN_N pulled high)
2:0	SBMAG[2:0]	R/W	0h	**Sensor Bias Magnitude** Selects the sensor bias current magnitude or the bias resistor 000: No sensor bias current or resistor (default) 001: 0.5-µA sensor bias current 010: 2-µA sensor bias current 011: 10-µA sensor bias current 100: 50-µA sensor bias current 101: 200-µA sensor bias current 110: 10-MΩ resistor 111: Reserved

9.6.6 Mode2 Register (offset = 05h) [reset = 04h]

Figure 110. Mode2 Register (MODE2)

7	6	5	4	3	2	1	0
BYPASS	GAIN[2:0]			DR[3:0]			
R/W-0h	R/W-0h			R/W-04h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. Mode2 Register (MODE2) Field Descriptions

Bit	Field	Type	Reset	Description
7	BYPASS	R/W	0h	**PGA Bypass Mode** Selects PGA bypass 0: PGA enabled (default) 1: PGA bypassed
6:4	GAIN[2:0]	R/W	0h	**PGA Gain** Selects the PGA gain 000: 1 V/V (default) 001: 2 V/V 010: 4 V/V 011: 8 V/V 100: 16 V/V 101: 32 V/V 110: Reserved 111: Reserved
3:0	DR[3:0]	R/W	4h	**Data Rate** Selects the ADC data rate. In FIR filter mode, the available data rates are limited to 2.5, 5, 10 and 20 SPS. 0000: 2.5 SPS 0001: 5 SPS 0010: 10 SPS 0011: 16.$\overline{6}$SPS 0100: 20 SPS (default) 0101: 50 SPS 0110: 60 SPS 0111: 100 SPS 1000: 400 SPS 1001: 1200 SPS 1010: 2400 SPS 1011: 4800 SPS 1100: 7200 SPS 1101: 14400 SPS 1110: 19200 SPS 1111: 38400 SPS

9.6.7 Input Multiplexer Register (offset = 06h) [reset = 01h]

Figure 111. Input Multiplexer Register (INPMUX)

7	6	5	4	3	2	1	0
MUXP[3:0]				MUXN[3:0]			
R/W-0h				R/W-01h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. Input Multiplexer Register (INPMUX) Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MUXP[3:0]	R/W	0h	**Positive Input Multiplexer** Selects the positive input multiplexer. 0000: AIN0 (default) 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: AINCOM 1011: Temperature sensor monitor positive 1100: Analog power supply monitor positive 1101: Digital power supply monitor positive 1110: TDAC test signal positive 1111: Float (open connection)
3:0	MUXN[3:0]	R/W	1h	**Negative Input Multiplexer** Selects the negative input multiplexer. 0000: AIN0 0001: AIN1 (default) 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: AINCOM 1011: Temperature sensor monitor negative 1100: Analog power supply monitor negative 1101: Digital power supply monitor negative 1110: TDAC test signal negative 1111: Float (open connection)

9.6.8 Offset Calibration Registers (offset = 07h, 08h, 09h) [reset = 00h, 00h, 00h]

Figure 112. Offset Calibration Registers (OFCAL0, OFCAL1, OFCAL2) 24-bit, 3 Rows

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
OFC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
OFC[23:16]							
R/W-00h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. Offset Calibration Registers (OFCAL0, OFCAL1, OFCAL2) Field Descriptions

Bit	Field	Type	Reset	Description
23:0	OFC[23:0]	R/W	000000h	**Offset Calibration Registers** 3 registers compose the 24-bit offset calibration word. The 24-bit word is 2's complement format and is internally left shifted to align with the 32-bit conversion result. The register value is subtracted from the 32-bit conversion result before the full scale operation.

9.6.9 Full Scale Calibration Registers (offset = 0Ah, 0Bh, 0Ch) [reset = 40h, 00h, 00h]

Figure 113. Full Scale Calibration Registers (FSCAL0, FSCAL1, FSCAL2) 24-bit, 3 Rows

7	6	5	4	3	2	1	0
FSCAL[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
FSCAL[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
FSCAL[23:16]							
R/W-40h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 39. Full Scale Calibration Registers (FSCAL0, FSCAL1, FSCAL2) Field Descriptions

Bit	Field	Type	Reset	Description
23:0	FSCAL[23:0]	R/W	400000h	**Full Scale Calibration Registers** Three 8-bit registers compose the 24-bit full scale calibration word. The 24-bit word format is straight binary. The 24-bit value is internally divided by 400000h to derive the gain coefficient. The gain coefficient is multiplied with the 32-bit conversion result after the offset operation.

9.6.10 IDACMUX Register (offset = 0Dh) [reset = 0BBh]

Figure 114. IDAC Multiplexer Register (IDACMUX)

7	6	5	4	3	2	1	0
MUX2[3:0]				MUX1[3:0]			
R/W-0Bh				R/W-0Bh			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 40. IDAC Multiplexer Register (IDACMUX) Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MUX2[3:0]	R/W	0Bh	**IDAC2 Output Multiplexer** Selects the analog input pin to connect IDAC2 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: AINCOM 1011: No Connection (default) 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved
3:0	MUX1[3:0]	R/W	0Bh	**IDAC1 Output Multiplexer** Selects the analog input pin to connect IDAC1 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: AINCOM 1011: No Connection (default) 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved

9.6.11 IDACMAG Register (offset = 0Eh) [reset = 00h]

Figure 115. IDAC Magnitude Register (IDACMAG)

7	6	5	4	3	2	1	0
MAG2[3:0]				MAG1[3:0]			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 41. IDAC Magnitude (IDACMAG) Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MAG2[3:0]	R/W	0h	**IDAC2 Current Magnitude** Selects the current values of IDAC2 0000: off (default) 0001: 50 µA 0010: 100 µA 0011: 250 µA 0100: 500 µA 0101: 750 µA 0110: 1000 µA 0111: 1500 µA 1000: 2000 µA 1001: 2500 µA 1010: 3000 µA 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved
3:0	MAG1[3:0]	R/W	0h	**IDAC1 Current Magnitude** Selects the current values of IDAC1 0000: off (default) 0001: 50 µA 0010: 100 µA 0011: 250 µA 0100: 500 µA 0101: 750 µA 0110: 1000 µA 0111: 1500 µA 1000: 2000 µA 1001: 2500 µA 1010: 3000 µA 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved

9.6.12 REFMUX Register (offset = 0Fh) [reset = 00h]

Figure 116. Reference Multiplexer Register (REFMUX)

7	6	5	4	3	2	1	0
RESERVED		RMUXP[2:0]			RMUXN[2:0]		
R/W-0h		R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 42. Reference Multiplexer Register (REFMUX) Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R	0h	**Reserved** Always write 0h
5:3	RMUXP[2:0]	R/W	0h	**Reference Positive Input** Selects the positive reference input 000: Internal 2.5 V reference - P (default) 001: External AIN0 010: External AIN2 011: External AIN4 100: Internal analog supply (V_{AVDD}) 101: Reserved 110: Reserved 111: Reserved
2:0	RMUXN[2:0]	R/W	0h	**Reference Negative Input** Selects the negative reference input 000: Internal 2.5 V reference - N (default) 001: External AIN1 010: External AIN3 011: External AIN5 100: Internal analog supply (V_{AVSS}) 101: Reserved 110: Reserved 111: Reserved

9.6.13 TDACP Control Register (offset = 10h) [reset = 00h]

Figure 117. TDACP Control Register (TDACP)

7	6	5	4	3	2	1	0
OUTP	RESERVED			MAGP[4:0]			
R/W-0h	R-0h			R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 43. TDACP Output Register (TDACP) Field Descriptions

Bit	Field	Type	Reset	Description
7	OUTP	R/W	0h	**TDACP Output Connection** Connects TDACP output to pin AIN6 0: No connection 1: TDACP output connected to pin AIN6
6:5	Reserved	R	0h	**Reserved** Always write 0
4:0	MAGP[4:0]	R/W	0h	**MAGP Output Magnitude** Select the TDACP output magnitude. The TDAC output voltages are ideal and are with respect to V_{AVSS} 01001: 4.5 V 01000: 3.5 V 00111: 3 V 00110: 2.75 V 00101: 2.625 V 00100: 2.5625 V 00011: 2.53125 V 00010: 2.515625 V 00001: 2.5078125 V 00000: 2.5 V 10001: 2.4921875 V 10010: 2.484375 V 10011: 2.46875 V 10100: 2.4375 V 10101: 2.375 V 10110: 2.25 V 10111: 2 V 11000: 1.5 V 11001: 0.5 V Remaining codes are reserved

9.6.14 TDACN Control Register (offset = 11h) [reset = 00h]

Figure 118. TDACN Control Register (TDACN)

7	6	5	4	3	2	1	0
OUTN	RESERVED			MAGN[4:0]			
R/W-0h	R-0h			R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 44. TDAC Negative Output Register (TDACN) Field Descriptions

Bit	Field	Type	Reset	Description
7	OUTN	R/W	0h	**TDACN Output Connection** Connects TDACN output to pin AIN7 0: No external connection 1: TDACN output connected to pin AIN7
6:5	Reserved	R	0h	**Reserved** Always write 0h
4:0	MAGN[4:0]	R/W	0h	**TDACN Output Magnitude** Select the TDACN output magnitude. The TDAC output voltages are ideal and are with respect to V_{AVSS} 01001: 4.5 V 01000: 3.5 V 00111: 3 V 00110: 2.75 V 00101: 2.625 V 00100: 2.5625 V 00011: 2.53125 V 00010: 2.515625 V 00001: 2.5078125 V 00000: 2.5 V 10001: 2.4921875 V 10010: 2.484375 V 10011: 2.46875 V 10100: 2.4375 V 10101: 2.375 V 10110: 2.25 V 10111: 2 V 11000: 1.5 V 11001: 0.5 V Remaining codes are reserved

9.6.15 GPIO Connection Register (offset = 12h) [reset = 00h]

Figure 119. GPIO Connection Register (GPIOCON)

7	6	5	4	3	2	1	0
CON[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 45. GPIO Connection Register (GPIOCON) Field Descriptions

Bit	Field	Type	Reset	Description
0	CON[0]	R/W	0h	**GPIO[0] Pin Connection** Connects GPIO[0] to analog input pin AIN3 0: GPIO[0] not connected to AIN3 (default) 1: GPIO[0] connected to AIN3
1	CON[1]	R/W	0h	**GPIO[1] Pin Connection** Connects GPIO[1] to analog input pin AIN4 0: GPIO[1] not connected to AIN4 (default) 1: GPIO[1] connected to AIN4
2	CON[2]	R/W	0h	**GPIO[2] Pin Connection** Connects GPIO[2] to analog input pin AIN5 0: GPIO[2] not connected to AIN5 (default) 1: GPIO[2] connected to AIN5
3	CON[3]	R/W	0h	**GPIO[3] Pin Connection** Connects GPIO[3] to analog input pin AIN6 0: GPIO[3] not connected to AIN6 (default) 1: GPIO[3] connected to AIN6
4	CON[4]	R/W	0h	**GPIO[4] Pin Connection** Connects GPIO[4] to analog input pin AIN7 0: GPIO[4] not connected to AIN7 (default) 1: GPIO[4] connected to AIN7
5	CON[5]	R/W	0h	**GPIO[5] Pin Connection** Connects GPIO[5] to analog input pin AIN8 0: GPIO[5] not connected to AIN8 (default) 1: GPIO[5] connected to AIN8
6	CON[6]	R/W	0h	**GPIO[6] Pin Connection** Connects GPIO[6] to analog input pin AIN9 0: GPIO[6] not connected to AIN9 (default) 1: GPIO[6] connected to AIN9
7	CON[7]	R/W	0h	**GPIO[7] Pin Connection** Connects GPIO[7] to analog input pin AINCOM 0: GPIO[7] not connected to AINCOM (default) 1: GPIO[7] connected to AINCOM

9.6.16 GPIO Direction Register (offset = 13h) [reset = 00h]

Figure 120. GPIO Direction Register (GPIODIR)

7	6	5	4	3	2	1	0
DIR[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 46. GPIO Direction Register (GPIODIR) Field Descriptions

Bit	Field	Type	Reset	Description
0	DIR[0]	R/W	0h	**GPIO[0] Pin Direction** Configures GPIO[0] as a GPIO input or GPIO output 0: GPIO[0] is an output (default) 1: GPIO[0] is an input
1	DIR[1]	R/W	0h	**GPIO[1] Pin Direction** Configures GPIO[1] as a GPIO input or GPIO output 0: GPIO[1] is an output (default) 1: GPIO[1] is an input
2	DIR[2]	R/W	0h	**GPIO[2] Pin Direction** Configures GPIO[2] as a GPIO input or GPIO output 0: GPIO[2] is an output (default) 1: GPIO[2] is an input
3	DIR[3]	R/W	0h	**GPIO[3] Pin Direction** Configures GPIO[3] as a GPIO input or GPIO output 0: GPIO[3] is an output (default) 1: GPIO[3] is an input
4	DIR[4]	R/W	0h	**GPIO[4] Pin Direction** Configures GPIO[4] as a GPIO input or GPIO output 0: GPIO[4] is an output (default) 1: GPIO[4] is an input
5	DIR[5]	R/W	0h	**GPIO[5] Pin Direction** Configures GPIO[5] as a GPIO input or GPIO output 0: GPIO[5] is an output (default) 1: GPIO[5] is an input
6	DIR[6]	R/W	0h	**GPIO[6] Pin Direction** Configures GPIO[6] as a GPIO input or GPIO output 0: GPIO[6] is an output (default) 1: GPIO[6] is an input
7	DIR[7]	R/W	0h	**GPIO[7] Pin Direction** Configures GPIO[7] as a GPIO input or GPIO output 0: GPIO[7] is an output (default) 1: GPIO[7] is an input

9.6.17 GPIO Data Register (offset = 14h) [reset = 00h]

Figure 121. GPIO Data Register (GPIODAT)

7	6	5	4	3	2	1	0
DAT[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 47. GPIO Data Register (GPIODAT) Field Descriptions

Bit	Field	Type	Reset	Description
0	DAT[0]	R/W	0h	**GPIO[0] Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[0] is low 1: GPIO[0] is high
1	DAT[1]	R/W	0h	**GPIO[1] Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[1] is low 1: GPIO[1] is high
2	DAT[2]	R/W	0h	**GPIO[2] Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[2] is low 1: GPIO[2] is high
3	DAT[3]	R/W	0h	**GPIO[3] Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[3] is low 1: GPIO[3] is high
4	DAT[4]	R/W	0h	**GPIO[4] Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[4] is low 1: GPIO[4] is high
5	DAT[5]	R/W	0h	**GPIO[5] Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[5] is low 1: GPIO[5] is high
6	DAT[6]	R/W	0h	**GPIO[6] Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[6] is low 1: GPIO[6] is high
7	DAT[7]	R/W	0h	**GPIO[7] Pin Data** Configured as an output, read returns the register value Configured as an input, write sets the register value only 0: GPIO[7] is low 1: GPIO[7] is high

9.6.18 ADC2 Configuration Register (offset = 15h) [reset = 00h]

Figure 122. ADC2 Configuration Register (ADC2CFG)

7	6	5	4	3	2	1	0
DR2[1:0]		REF2[2:0]			GAIN2[2:0]		
R/W-0h		R/W-0h			R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 48. ADC2 Configuration Register (ADC2CFG) Field Descriptions

Bit	Field	Type	Reset	Description
7:6	DR2[1:0]	R/W	0h	**ADC2 Data Rate** These bits select the data rate of ADC2 00: 10 SPS (default) 01: 100 SPS 10: 400 SPS 11: 800 SPS
5:3	REF2[2:0]	R/W	0h	**ADC2 Reference Input** Selects the reference inputs of ADC2 as P-N pairs 000: Internal 2.5 V reference positive and negative inputs (default) 001: External AIN0/AIN1 pin pairs as positive/negative reference inputs 010: External AIN2/AIN3 pin pairs as positive/negative reference inputs 011: External AIN4/AIN5 pin pairs as positive/negative reference inputs 100: Internal V_{AVDD} and V_{AVSS} 101: Reserved 110: Reserved 111: Reserved
2:0	GAIN2[2:0]	R/W	0h	**ADC2 Gain** These bits configure the gain of ADC2 000: 1 V/V (default) 001: 2 V/V 010: 4 V/V 011: 8 V/V 100: 16 V/V 101: 32 V/V 110: 64 V/V 111: 128 V/V

9.6.19 ADC2 Input Multiplexer Register (offset = 16h) [reset = 01h]

Figure 123. ADC2 Input Multiplexer Register (ADC2MUX)

7	6	5	4	3	2	1	0
MUXP2[3:0]				MUXN2[3:0]			
R/W-0h				R/W-01h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 49. ADC2 Input Multiplexer Register (ADC2MUX) Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MUXP2[3:0]	R/W	0h	**ADC2 Positive Input Multiplexer** Selects the ADC2 positive input 0000: AIN0 (default) 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: AINCOM 1011: Temperature sensor monitor positive 1100: Analog power supply monitor positive 1101: Digital power supply monitor positive 1110: TDAC test signal positive 1111: Open connection
3:0	MUXN2[3:0]	R/W	01h	**ADC2 Negative Input Multiplexer** Selects the ADC2 negative input 0000: AIN0 0001: AIN1 (default) 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: AINCOM 1011: Temperature sensor monitor negative 1100: Analog power supply monitor negative 1101: Digital power supply monitor negative 1110: TDAC test signal negative 1111: Open Connection

9.6.20 ADC2 Offset Calibration Registers (offset = 17h, 18h) [reset = 00h, 00h]

Figure 124. ADC2 Offset Calibration Registers (ADC2OFC0, ADC2OFC1) 16-bit, 2 Rows

7	6	5	4	3	2	1	0
OFC2[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
OFC2[15:8]							
R/W-00h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 50. ADC2 Offset Calibration Registers (ADC2OFC0, ADC2OFC1) Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OFC2[15:0]	R/W	0000h	**ADC2 Offset Calibration Registers** Two registers compose the ADC2 16-bit offset calibration word. The 16-bit word is twos complement format and is internally left-shifted to align with the ADC2 24-bit conversion result. The register value is subtracted from the conversion result before the full scale operation.

9.6.21 ADC2 Full Scale Calibration Registers (offset = 19h, 1Ah) [reset = 00h, 00h]

Figure 125. ADC2 Full Scale Calibration Registers (ADC2FSC0, ADC2FSC1) 16-bit, 2 Rows

7	6	5	4	3	2	1	0
FSC2[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
FSC2[15:8]							
R/W-40h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 51. ADC2 Full-Scale Calibration Registers (ADC2FSC0, ADC2FSC1) Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FSC2[15:0]	R/W	4000h	**ADC2 Full Scale Calibration Registers** Two registers compose the ADC2 16-bit full scale calibration word. The 16-bit word format is straight binary. The 16-bit value is internally divided by 4000h to derive the scale factor for calibration. After the offset operation, the scale factor is multiplied with the conversion result .

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Floated (Isolated) Inputs

Floating (isolated) sensors (sensors that are not referenced to the ADC ground) must have the common mode voltage established within the specified ADC input range. The common mode voltage can be established by external resistor biasing or by connecting the negative lead to ground (bipolar analog supply) or connecting to a DC offset voltage (unipolar analog supply). The level shift voltage option is available on the AINCOM pin for this purpose. The 2.5-V reference output voltage can also be used to level shift other floating sensor inputs.

10.1.2 Single-Ended Measurements

Single-ended measurements typically have one input connected to a fixed potential (ground or offset voltage) and the other input is the signal. Usually, the fixed connection is the negative input. The positive input is the signal and is driven above and below the negative input, as shown in Figure 128. This is an example of a bipolar signal because the positive input can swing above and below the negative input. Unipolar signals are those that the positive signal is equal to or greater than the negative signal. The single-ended signal plus the offset voltage must be within the ADC specified operating range. In single supply configurations (5 V), the offset voltage is usually 2.5 V. This type of input configuration is shown in Figure 126. For bipolar power supplies (±2.5 V), the negative voltage can be grounded. This type of input is shown in Figure 127

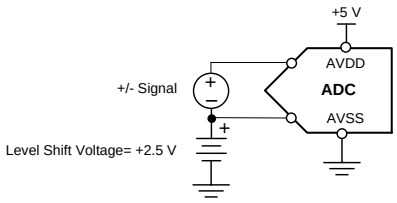


Figure 126. Single-Ended Input with Offset

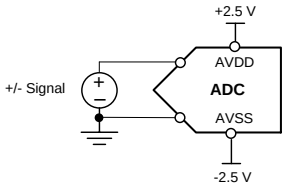


Figure 127. Single-Ended Input with Ground

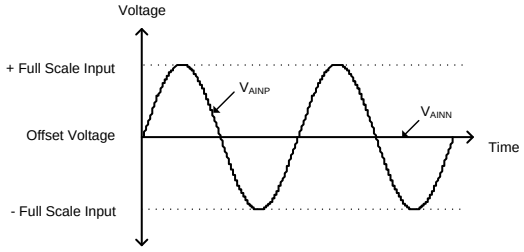


Figure 128. Single-Ended Input Voltage Diagram

Application Information (continued)

10.1.3 Differential Measurements

A differential signal is one where both inputs are driven in symmetric and opposite polarities centered at a common-mode voltage. Optimally, the common-mode voltage is the midpoint of the ADC input range. The common-mode voltage plus the signal must always be within the ADC specified operating range to avoid signal clipping. As shown in Figure 131, the magnitude of each signal is maximum ½ of the ADC full-scale range. The maximum differential signal ($V_{AINP} – V_{AINN}$) is equal to or less than the ADC FSR. For single 5-V operation, the common-mode voltage is typically equal to midsupply (2.5 V) in order to use the full ADC input range. This type of input with single 5-V supply operation is shown in Figure 129. For bipolar supplies (±2.5 V), the common-mode voltage of V_{AINP} and V_{AINN} are typically ground potential. This type of input of configuration is shown in Figure 130. Certain types of differential signals, such as from a bridge circuits, are derived from the ADC power supply; therefore, the common-mode voltage is defined.

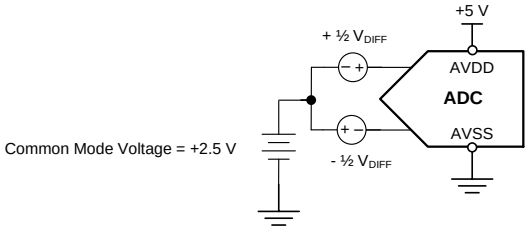


Figure 129. Differential Input with Common Mode Offset

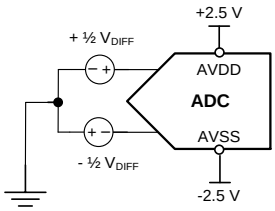


Figure 130. Differential Input with Common Mode Ground

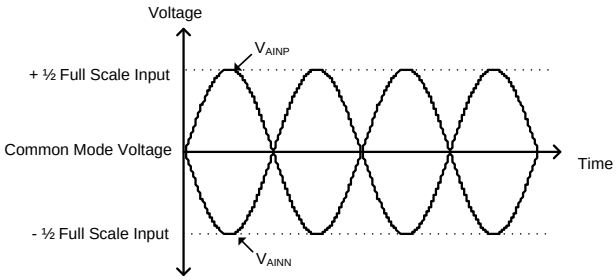


Figure 131. Differential Input Voltage Diagram

Application Information (continued)

10.1.4 Input Range

For proper operation of the ADC, the PGA absolute input voltages, V_{INP} and V_{INN}, must always remain within the valid PGA input range as shown in Equation 11 and repeated here in Equation 19.

$$V_{AVSS} + 0.3 + |V_{IN}| \cdot (Gain -1) / 2 < V_{INP} \text{ and } V_{INN} < V_{AVDD} – 0.3 – |V_{IN}| \cdot (Gain – 1) / 2$$

where

- V_{INP}, V_{INN} = Absolute input voltages
- V_{IN} = Differential input voltage = $V_{INP} – V_{INN}$ (19)

The following shows an example of how to determine the input range requirement. A thermocouple is used with the negative lead connected the internal level shift (2.5 V) and with a maximum thermocouple voltage of 60 mV (differential). The PGA gain used in this example is 32 and the ADC is operated with a single 5-V power supply. The following conditions are used to verify the PGA input range requirement:

V_{INN} = 2.5 V

V_{INP} = 2.56 V

V_{IN} = 60 mV

V_{AVDD} = 4.75 V (worst case minimum)

V_{AVSS} = 0 V

Gain = 32

$0 + 0.3 + 0.06 \cdot (32-1) / 2 < 2.5 \text{ and } 2.56 < 4.75 – 0.3 – 0.06 \cdot (32 – 1) / 2 \rightarrow$ **1.23 V < 2.5 V and 2.56 V < 3.52 V**

The inequality is satisfied, therefore the V_{INN} and V_{INP} absolute input voltages are within the required PGA input range. Alternatively, the PGA output voltages (pins CAPP and CAPN) can be measured by a voltmeter to verify that each PGA output voltage is < V_{AVDD} – 0.3V and > V_{AVSS} – 0.3 V under the expected minimum and maximum input conditions.

Application Information (continued)

10.1.5 Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

10.1.5.1 Aliasing

As with all ADCs, out of band input signals can fold back *or alias* if not band-limited. Aliasing describes the effect of input frequencies greater than ½ the sample rate folding back to the bandwidth of interest. An anti-alias filter placed at the ADC inputs reduces the magnitude of the aliased frequencies. The ADS1262 and ADS1263 integrates analog and digital anti-aliasing filters to attenuate the aliased frequencies. There are two ranges of aliased frequencies: frequencies greater than ½ of the down-sampled output data rate (Nyquist frequency) and frequencies occurring at multiples of the modulator sample rate.

Aliasing can occur at frequencies greater than ½ the ADC output data rate. For example, at data rate of 50 SPS, aliasing occurs at frequencies greater than 25 Hz. The ADC digital filter rejects the aliased frequencies as input frequency increases. The amount of aliased frequency rejection is given by the filter type and order. Figure 132 shows the frequency response of the sinc filter. Note the sinc4 filter provides the best rejection of aliased frequencies.

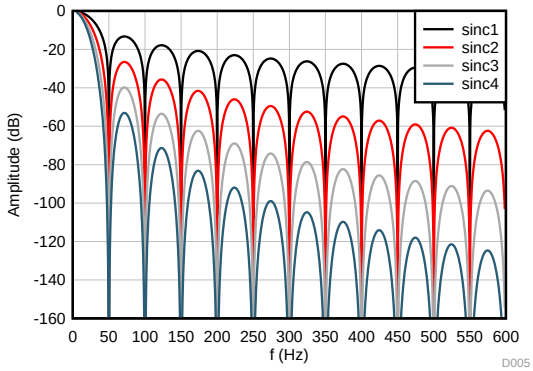


Figure 132. Frequency Response (50 SPS)

The second band of aliased frequencies occur at the ADC modulator sample rate multiples (f_{MOD} = f_{CLK} / 8 = 921.6 kHz, multiples = 1843.2 kHz and so on). Figure 133 shows the 38400 SPS frequency response plotted to 1.2 MHz. The response near DC is the signal bandwidth of interest. Note how the digital filter response repeats on either side of the modulator sample rate of 921.6 kHz. Figure 133 shows the repeated response at the modulator frequency multiples = N · f_{MOD} ± f_{DATA}, where N = 1, 2, 3 and so on. The digital filter attenuates signal or noise up to where the response repeats. However, signal or noise occurring at the modulator sample rate is not attenuated by the digital filter and therefore, is aliased to the passband.

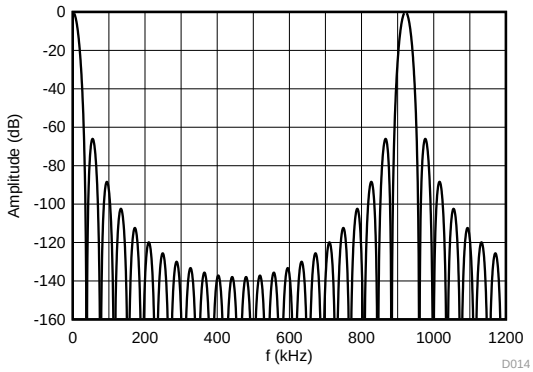


Figure 133. Frequency Response to 1.2 MHz (38400 SPS)

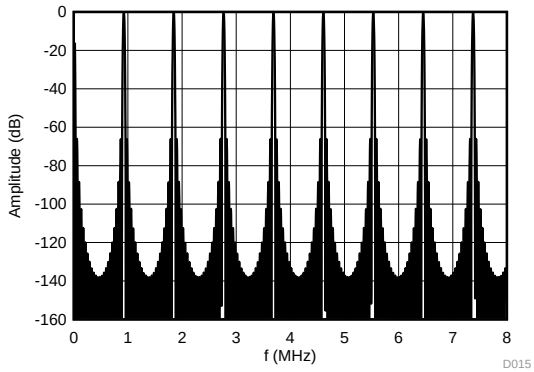


Figure 134. Frequency Response to 8 MHz (38400 SPS)

Application Information (continued)

Figure 135 illustrates how the frequencies alias near the modulator sample rate frequency. The final figure shows the aliased frequency rejection provided by an anti-alias filter. The ADC integrates an analog anti-alias filter with a cut-off frequency equal to 60 kHz.

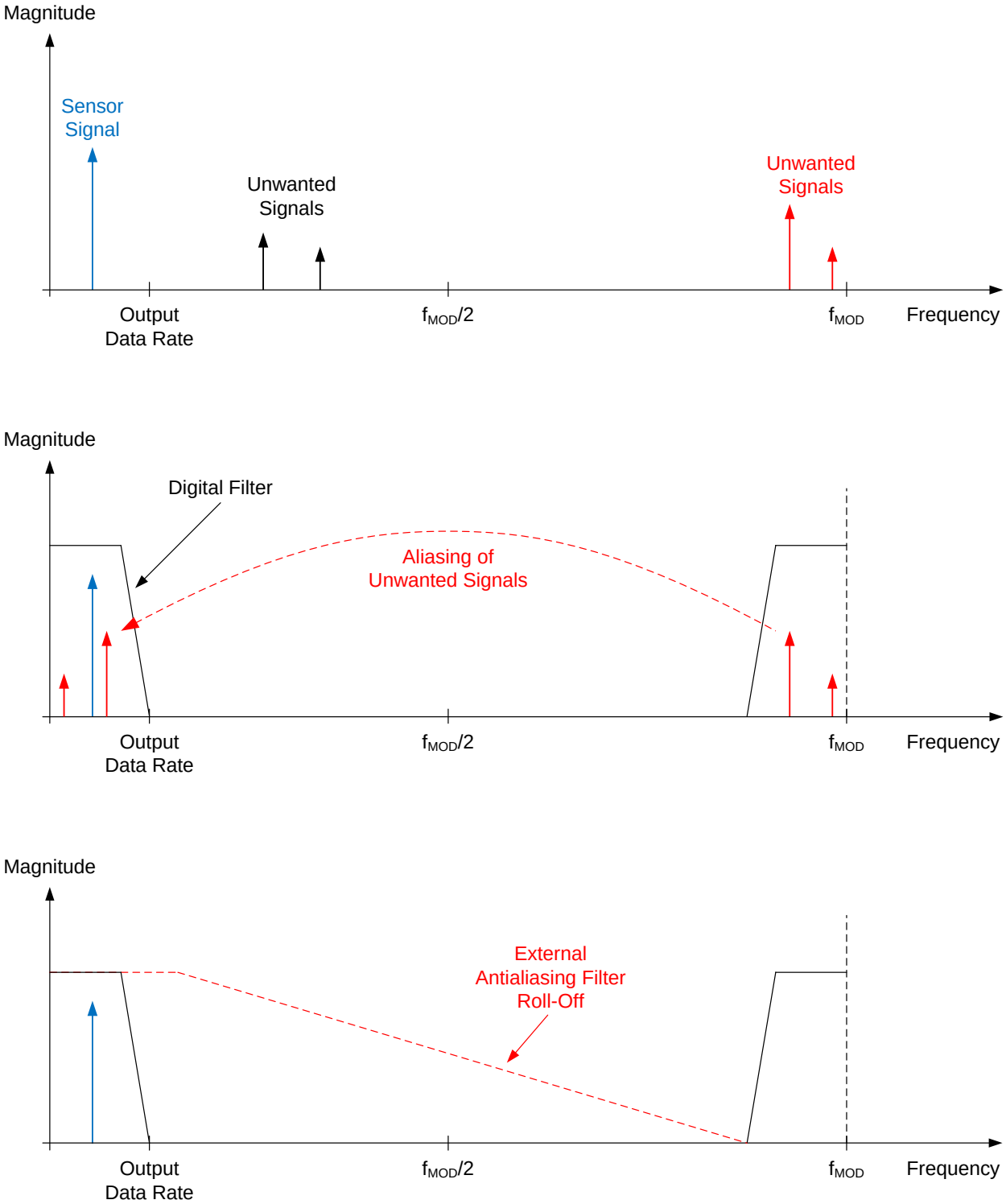


Figure 135. Alias Effect

Application Information (continued)

Many sensor signals are inherently band-limited; for example, the output of a thermocouple has a limited rate of change. In this case the sensor signal does not alias back into the pass-band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass-band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source can exist on the printed circuit board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result. The ADC incorporates an low-pass, anti-alias filter with a corner frequency of 60 kHz to reduce the aliased frequencies. The filter is composed of the external 4.7-nF PGA output capacitor (CAPP and CAPN pins) and internal 300-Ω resistors.

An input filter can be used to provide increased rejection of aliased noise frequencies and also to further attenuate possible strong hi-frequency interference signals. For best performance, strong interference frequencies should be filtered at the ADC inputs. Ideally, the low pass corner frequency is selected to allow frequencies within the desired bandwidth and attenuate those frequencies outside the desired bandwidth. Due to the stable and linear dielectric characteristics, C0G type MLCC capacitors are recommended for use in analog signal filters. In applications where high energy transients can be generated, such as caused by inductive load switching, transient voltage suppressor (TVS) diodes or external ESD diodes should be used to protect the ADC inputs.

10.1.6 Input Overload

Input over-voltage precautions should be observed as outlined in the ESD Diode section. However, if an over-voltage condition occurs on an unused channel, the over-voltage channel may cross-talk to the measurement channel. One solution is to externally clamp the inputs with low-forward voltage diodes and shown in Figure 136. The external diodes shunt the over voltage fault current around the ADC inputs. The reverse leakage current of the external clamp diodes should be considered in the application.

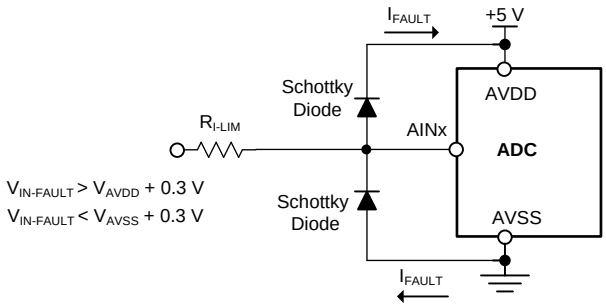


Figure 136. External Diode Voltage Clamp

10.1.7 Unused Inputs

To minimize input leakage of the measurement channel, tie the unused input channels to mid-supply (V_{AVDD} + V_{AVSS}) / 2. The 2.5 V reference output voltage can be used for this purpose if operating with single 5-V supply. Unused digital inputs should not float. Tie all unused digital inputs to the appropriate levels, V_{DVDD} or ground, including when in power down mode. Do not float (three-sate) the digital inputs to the ADC or excessive power supply leakage current can result. Unused digital outputs can be unconnected.

10.1.8 Voltage Reference

For non-ratiometric measurements, where the input signal is not derived from the voltage reference, a low noise, low drift reference is essential for best performance. Examples of these types of measurements are thermocouples, 20 mA receivers and accelerometers. For ratiometric measurements, where the input signal is derived from the voltage reference, reference noise and drift are cancelled by the same ratio of noise and drift within the signal. Ratiometric operation is common with many types of bridge and RTD measurements. In general, the best Signal-to-Noise ratio from the ADC is achieved with large amplitude signals, large reference voltage and the highest gain setting possible.

Application Information (continued)

10.1.9 Serial Interface Connections

After power up, take the $\overline{CS}$ input high to reset the ADC serial interface. $\overline{CS}$ high ensures the serial interface is reset in the event an unintentional SCLK glitch may have occurred during power-on initialization. If $\overline{CS}$ is tied low, the SCLK should be glitch free after power up or serial interface synchronization may be lost. In this case, reset the ADC using the PWDN/$\overline{RESET}$ input. The SCLK input is edge sensitive and therefore should be free of noise, glitches and overshoot. A terminating resistor located at the SCLK buffer can smooth the edges and reduce overshoot.

Most microcontroller SPI peripherals can operate with the ADC. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are updated or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the device can be found in the Timing Requirements: Serial Interface. Place a 47-Ω resistor in series with all digital input and output pins (CS, SCLK, DIN, DOUT/$\overline{DRDY}$, and $\overline{DRDY}$). The resistor source terminates the PCB trace and helps to reduce over-shoot and ringing.

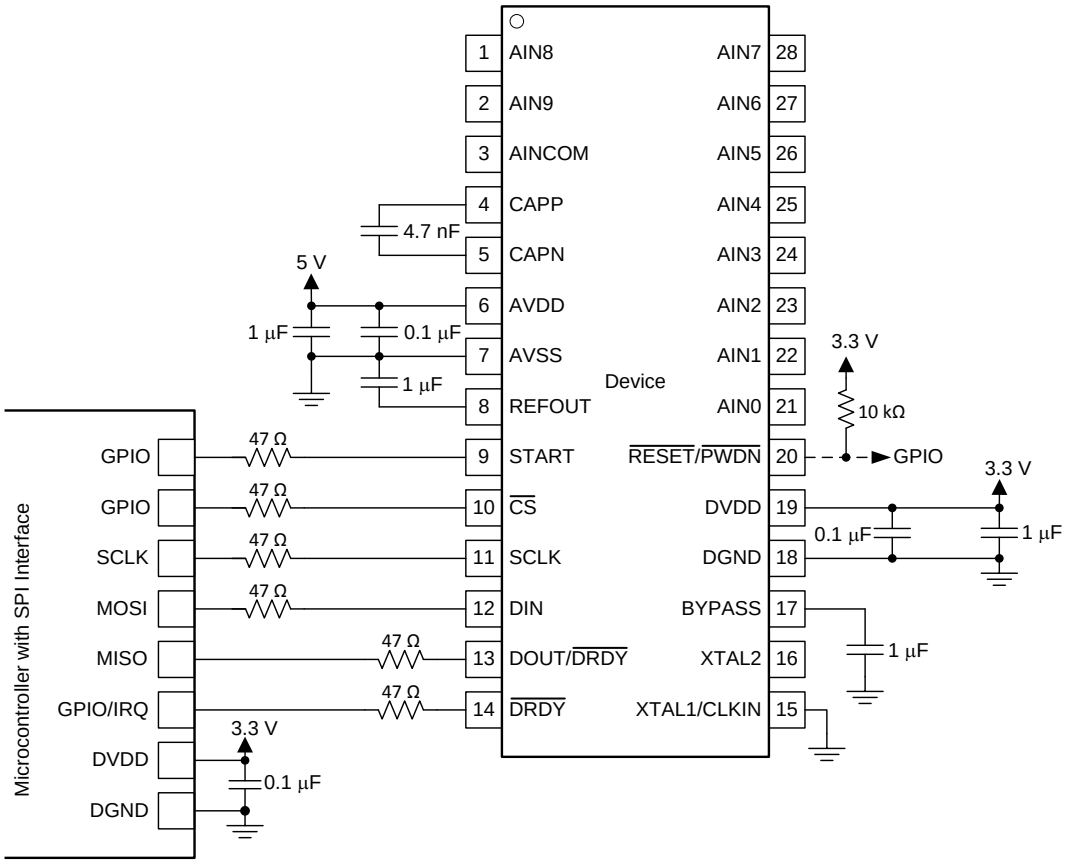


Figure 137. Serial Interface Connections

10.2 Typical Applications

10.2.1 3-Wire RTD Measurement with Lead-Wire Compensation

Figure 138 is a fault-protected and filtered, 3-wire RTD application circuit with hardware-based lead wire compensation. Two IDAC current sources are used to provide the lead wire compensation. One IDAC current source (IDAC1) provides excitation to the RTD element. The ADC reference voltage input (pins AIN2 and AIN3) is derived from the same current by resistor R_{REF}, providing ratiometric cancellation of current source drift. The other current source (IDAC2) has the same current setting, providing cancellation of lead wire resistance by generating a voltage drop across the lead wire resistance R_{LEAD2} equal to the voltage drop of R_{LEAD1}. Because the R_{RTD} voltage is measured differentially at ADC pins AIN4 and AIN5, the voltages across the lead wire resistance cancel. Resister R_{BIAS} level shifts the RTD signal to within the ADC specified input range. Note the current sources are provided by two additional pins and are routed to the RTD through blocking diodes. The additional pins (AIN1 and AIN6) are used to route the currents around the input resistors, avoiding the voltage drop otherwise caused by the filter resistors R_{F1} and R_{F4}. The diodes block the fault voltage in the event of a mis-wire connection to protect the ADC inputs. The input filter resistors also limit the input fault currents flowing into the ADC.

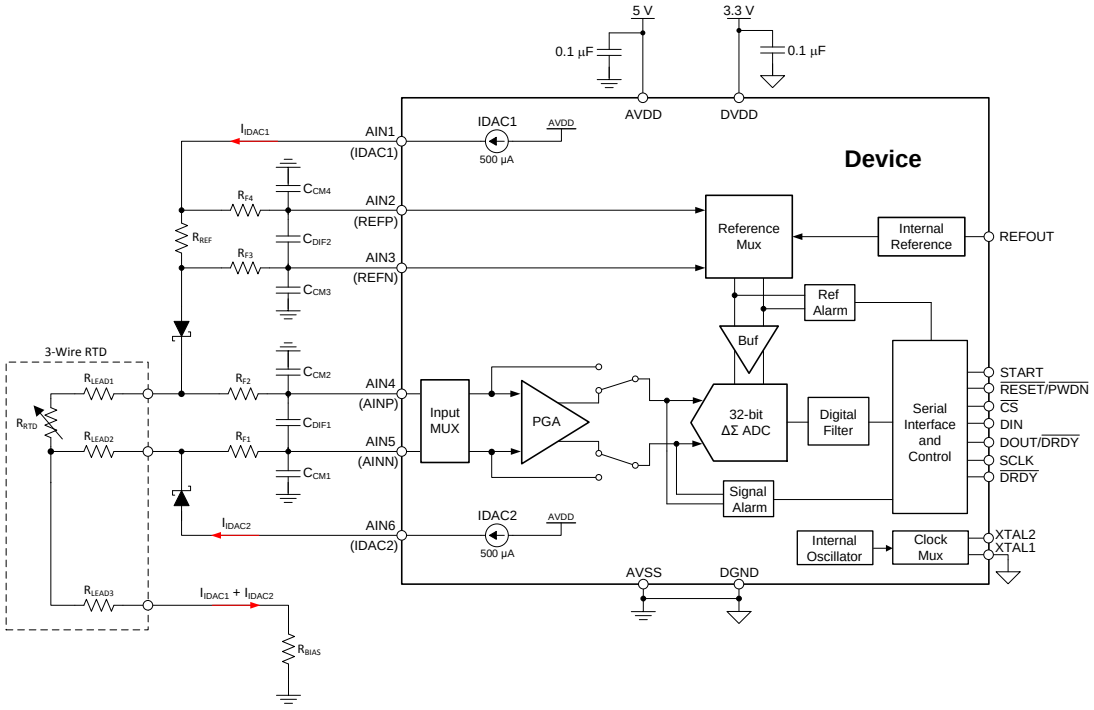


Figure 138. 3-Wire RTD Application

10.2.1.1 Design Requirements

Table 52 shows the design requirements of the 3-wire RTD application.

Table 52. Design Requirements

DESIGN PARAMETER	VALUE
ADC supply voltage	4.75 V (minimum)
RTD sensor type	3-wire Pt100
RTD resistance range	0 Ω to 400 Ω
RTD lead resistance range	0 Ω to 10 Ω
RTD self heating	< 1 mW
Accuracy (1)	±0.02 Ω

(1) T_A = 25°C. After offset and full-scale calibration.

10.2.1.2 Detailed Design Procedure

The two major considerations In the design of a 3-wire RTD circuit are the RTD self-heating and the measurement resolution. As the design values of Table 53 illustrates, there are several magnitudes of excitation currents available for use. The various excitation current settings can be used to tradeoff measurement resolution against RTD self-heating. In general, measurement resolution improves by increasing the excitation current value. Increasing the excitation current beyond 1000 µA results in no further improvement in measurement resolution. The design procedure is based on 500-µA excitation current, as this level of current low self-heating power (0.4 mW). The measurement resolution is expressed in noise free resolution (NFR). Noise free resolution is the resolution with no code flicker.

Table 53. RTD Circuit Design Parameters

I_{IDAC} (µA)	NFR (bits)	P_{RTD} (mW)	V_{RTD} (V)(1)	Gain (V/V)(2)	V_{REFMIN} (V)(3)	V_{REF} (V)(4)	R_{REF} (kΩ)(5)	V_{INNLIM} (V)(6)	V_{INPLIM}(V)(7)	R_{BIAS} (kΩ)(8)	V_{RTDN} (V)(9)	V_{RTDP} (V)(10)	V_{IDAC1} (V)(11)
50	16.8	0.001	0.02	32	0.64	0.90	18	0.6	4.1	7.10	0.7	0.7	1.9
100	17.8	0.004	0.04	32	1.28	1.41	14.1	0.9	3.8	5.10	1.0	1.1	2.8
250	18.8	0.025	0.10	16	1.60	1.76	7.04	1.1	3.7	2.30	1.2	1.3	3.3
500	19.1	0.100	0.20	8	1.60	1.76	3.52	1.0	3.8	1.10	1.1	1.3	3.4
750	18.9	0.225	0.30	4	1.20	1.32	1.76	0.8	4.0	0.57	0.9	1.2	2.8
1000	19.3	0.400	0.40	4	1.60	1.76	1.76	0.9	3.9	0.50	1.0	1.4	3.5
1500	19.1	0.900	0.60	2	1.20	1.32	0.88	0.6	4.2	0.23	0.7	1.3	3.0
2000	18.3	1.600	0.80	1	0.80	0..90	0.45	0.3	4.5	0.10	0.4	1.2	2.4

(1) V_{RTD} is the RTD input voltage
(2) Gain is the ADC gain
(3) V_{REFMIN} is the minimum reference voltage required by the design
(4) V_{REF} is the design target reference voltage allowing for 10 % over-range or set to the minimum 0.9 V reference voltage requirement
(5) R_{REF} is the resistor that senses the IDAC current to generate V_{REF}
(6) V_{INNLIM} is the absolute minimum input voltage required by the ADC
(7) V_{INPLIM} is the absolute maximum input voltage required by the ADC
(8) R_{BIAS} establishes the level shift voltage
(9) V_{RTDN} is the designed negative input voltage
(10) V_{RTDP} is the designed positive input voltage
(11) V_{IDAC1} is the designed IDAC1 loop voltage

Initially, R_{LEAD1} and R_{LEAD2} are considered to be zero ohms. The IDAC1 current is routed through the external reference resistor, R_{REF}. The ADC reference voltage, V_{REF}, is generated across the reference resistor. This voltage is defined by: $V_{REF} = I_{IDAC1} \cdot R_{REF}$. The second current (IDAC2) is routed to the second RTD lead. Both IDAC1 and IDAC2 are programmed to the same value, by the IDACMAG register, but only the IDAC1 current flows through the reference resistor and RTD. The IDAC1 current excites the RTD to produce a voltage proportional to the RTD resistance. The RTD voltage is defined by: $V_{RTD} = R_{RTD} \cdot I_{IDAC1}$. The ADC amplifies the RTD signal voltage (V_{RTD}) and measures the resulting voltage against the reference voltage to produce a proportional digital output code. This is illustrated in Equation 20 through Equation 22 .

$$\text{Code} \propto V_{RTD} \cdot \text{Gain} / V_{REF} \quad (20)$$

$$\text{Code} \propto (R_{RTD} \cdot I_{IDAC1}) \cdot \text{Gain} / (I_{IDAC1} \cdot R_{REF}) \quad (21)$$

$$\text{Code} \propto (R_{RTD} \cdot \text{Gain}) / R_{REF} \quad (22)$$

As can be seen by Equation 22, the RTD measurement only depends on the value of the RTD, the PGA gain, and the reference resistor R_{REF}, but not on the IDAC1 value. The absolute accuracy and temperature drift of the excitation current therefore does not matter.

The second excitation current (IDAC2) is used to provide a second voltage drop across the second RTD lead resistance R_{LEAD2}. The second voltage drop compensates the voltage drop caused by I_{DAC1} and R_{LEAD1}. Because the leads of a 3-wire RTD typically have the same length, the lead resistance is the same. Taking the lead resistance into account ($R_{LEADx} \neq 0$), the differential voltage (V_{IN}) across the ADC inputs, AIN0 and AIN1, is shown in Equation 23:

$$V_{IN} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) - I_{IDAC2} \cdot R_{LEAD2} \quad (23)$$

If $R_{LEAD1} = R_{LEAD2}$ and $I_{IDAC1} = I_{IDAC2}$, the expression for V_{IN} reduces to Equation 24:

$$V_{IN} = I_{IDAC1} \cdot R_{RTD} \quad (24)$$

In other words, the measurement error resulting from the voltage drop across the RTD lead resistance is compensated, as long as the lead resistance values and the IDAC values are well matched.

The 500 µA IDAC current offers a balance between measurement resolution and sensor self-heating. The maximum value of RTD resistance (400 Ω) and the excitation current (500 µA) yields an RTD voltage V_{RTD} = 500 µA · 400 Ω = 0.2 V. The gain is selected to be 8 V/V to reduce the required reference voltage (V_{REF}) as well as the total IDAC1 loop voltage. The loop voltage is limited by the IDAC voltage compliance range. Selecting Gain = 8 V/V requires a minimum reference voltage V_{REFMIN} = 0.2 V · 4 = 1.6 V. To provide a margin for the ADC operating range, the target reference voltage is increased by 10% (V_{REF} = 1.6 V · 1.1 = 1.76 V). The value of the reference resistor can now be calculated as follows: $R_{REF} = V_{REF} / I_{IDAC1}$ = 1.76 V/ 500 µA = 3.52 kΩ. The reference resistor R_{REF} should be precision and have low temperature drift (< 10 ppm/°C).

The next step in the design is to determine the value of the R_{BIAS} resistor to provide the level shift voltage in order to meet the ADC absolute input voltage specification. The amount of level shift voltage required is determined by calculating the required minimum absolute voltage (V_{INNLIM}) as shown in Equation 25.

$$V_{AVSS} + 0.3 + V_{RTD} \cdot (Gain – 1) / 2 \le V_{INNLIM}$$

where

- V_{RTD} = maximum differential RTD voltage = 0.2 V
- Gain = 8
- V_{AVSS} = 0 V (25)

The result of the equation requires the minimum absolute input voltage, V_{RTDN} > 1.0 V. Therefore, the RTD voltage must be level shifted to a minimum of 1.0 V. To meet this requirement, a target level shift value of 1.1 V is chosen to provide 0.1 V margin. The value of R_{BIAS} is calculated as shown in Equation 26:

$$R_{BIAS} = V_{INN} / (I_{IDAC1} + I_{IDAC2}) = 1.1 V / (2 \cdot 500 µA) = 1.1 kΩ. \quad (26)$$

Now that the level shift voltage is known, the positive RTD voltage (V_{RTDP}) must be verified to be less than the maximum absolute input voltage (V_{INPLIM}). V_{INPLIM} is shown in Equation 27.

$$V_{INPLIM} \le V_{AVDD} – 0.3 – V_{RTD} \cdot (Gain – 1) / 2$$

where

- V_{RTD} = maximum differential RTD voltage = 0.2 V
- Gain = 2
- V_{AVDD} = 4.75 V (minimum) (27)

Solving the V_{INPLIM} equation requires V_{RTDP} to be less than 3.8 V. V_{RTDP} input voltage is calculated by Equation 28

$$V_{INP} = V_{RTDN} + I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) = 1.1 V + 500 µA \cdot (400 Ω + 10 Ω) = 1.3 V \quad (28)$$

Because 1.3 V is less than the 3.65 V maximum input voltage limit, the absolute positive and negative RTD voltages are within the ADC specified input range.

The next step in the design is to verify that the loop voltage of the excitation current is less than the specified IDAC compliance voltage.. The IDAC compliance voltage is the maximum voltage drop developed across each IDAC current path to AVSS. In this circuit, IDAC1 has the largest voltage drop developed across its current path. The IDAC1 calculation is sufficient to satisfy IDAC2 because the IDAC2 voltage drop is always less than IDAC1 voltage drop. The sum of voltages in the IDAC1 loop is shown in Equation 29:

$$V_{IDAC1} = [(I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD3} + R_{BIAS})] + [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1} + R_{REF})] + V_D$$

where

- V_D = external blocking diode voltage. (29)

The equation results in a loop voltage of V_{IDAC1}= 3.4 V. The worst case current source compliance voltage is: (V_{AVDD} – 1.1 V) = (4.75 V – 1.1 V) = 3.64 V. The V_{IDAC1} loop voltage is less than the specified current source compliance voltage (3.4 V < 3.64 V).

Many applications benefit from using an analog filter at the inputs to remove noise and interference from the signal. Filter components (R_{F1}, R_{F2}, C_{DIF1}, C_{CM1}, and C_{CM2}) are placed on the ADC inputs, as well as on the reference inputs (R_{F3}, R_{F4}, C_{DIF2}, C_{CM3}, and C_{CM4}). The filters remove both differential and common-mode noise. The application shows a differential input noise filter formed by R_{F1}, R_{F2} and C_{DIF}, with additional differential mode capacitance provided by the common-mode filter capacitors, C_{M1} and C_{M2}. The differential cutoff frequency is calculated as shown in Equation 30:

$$f_{DIF} = 1 / [2\pi \cdot (R_{F1} + R_{F2}) \cdot (C_{DIF1} + C_{M1} || C_{M2})] \quad (30)$$

The common-mode noise filter is formed by components R_{F1}, R_{F2}, C_{M1} and C_{M2}. The common-mode signal cutoff frequency is calculated as shown in Equation 31:

$$f_{CM} = 1 / (2\pi \cdot R_{F1} \cdot C_{M1}) = 1 / (2\pi \cdot R_{F2} \cdot C_{M2}) \quad (31)$$

Mismatches in the common-mode filter components can convert common-mode noise into differential noise. To reduce the effect of mismatch, the differential mode filter should have a corner frequency that is 10x lower than the common-mode filter corner frequency. The low frequency differential filter removes the common-mode converted noise. The filter resistors R_{Fx}) also serve as current-limiting resistors. These resistors limit the current into the analog inputs (AINx) of the device to safe levels when an over-voltage occurs on the inputs. The filter resistors can lead to an offset voltage error due to the DC input current leakage flowing into and out of the device. However, the voltage error can be removed by system offset calibration. Resistor values that are too large can generate excess thermal noise and degrade the overall noise performance. The recommended range of the filter resistor value is 2 kΩ to 10 kΩ. The electrical characteristics of the capacitors are important because the capacitors filter the signal; use high quality C0G ceramics or film type capacitors.

For consistent noise performance across the full range of RTD measurements, the corner frequencies of the input and reference filter must be matched. Detailed information on matching the input and reference filter can be found in Application Report SBAA201, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248.*

10.2.2 Application Curve

Figure 139 shows the resistance measurement results. The measurements are taken at T_A = 25°C. A system offset calibration is performed using shorted inputs. A system gain calibration is performed using a 390 Ω precision resistor. The data are taken using a precision resistor simulator instead of a 3-wire Pt100. Note that the measurement data are in Ohms and does not include the error of the RTD sensor itself. The measured resistance error is < ±0.02 Ω over the 0-Ω to 400-Ω range.

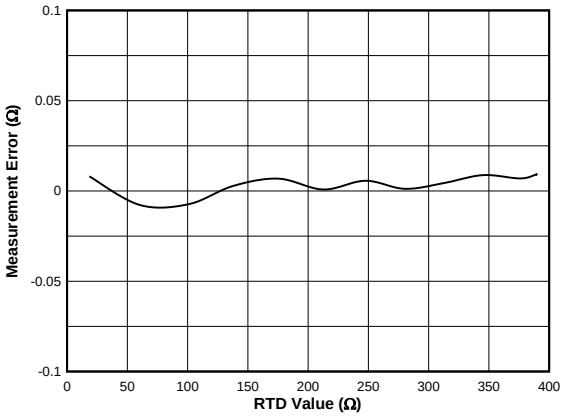


Figure 139. Resistance Measurement Error

10.3 Do's and Don'ts

- Do partition the analog, digital and power supply circuitry into separate sections on the PCB
- Do use a single ground plane for analog and digital grounds
- Do place the analog components close to the ADC pins using short, direct connections
- Do keep the SCLK pin free of glitches and noise
- Do verify that the analog input voltages are within the specified PGA input voltage range under all input conditions
- Do tie unused analog input pins to midsupply to minimum input leakage current
- Do provide current limiting to the analog inputs if over-voltage faults may occur
- Do use an LDO regulator to reduce ripple voltage generated by switch-mode power supplies
- Don't route digital clock traces in the vicinity of the CAPP and CAPN pins
- Don't cross digital signals over analog signals
- Don't allow the analog and digital power supply voltages to exceed 7 V under all conditions, including at power-up and power-down

Figure 140 shows Do's and Don'ts of ADC circuit configurations.

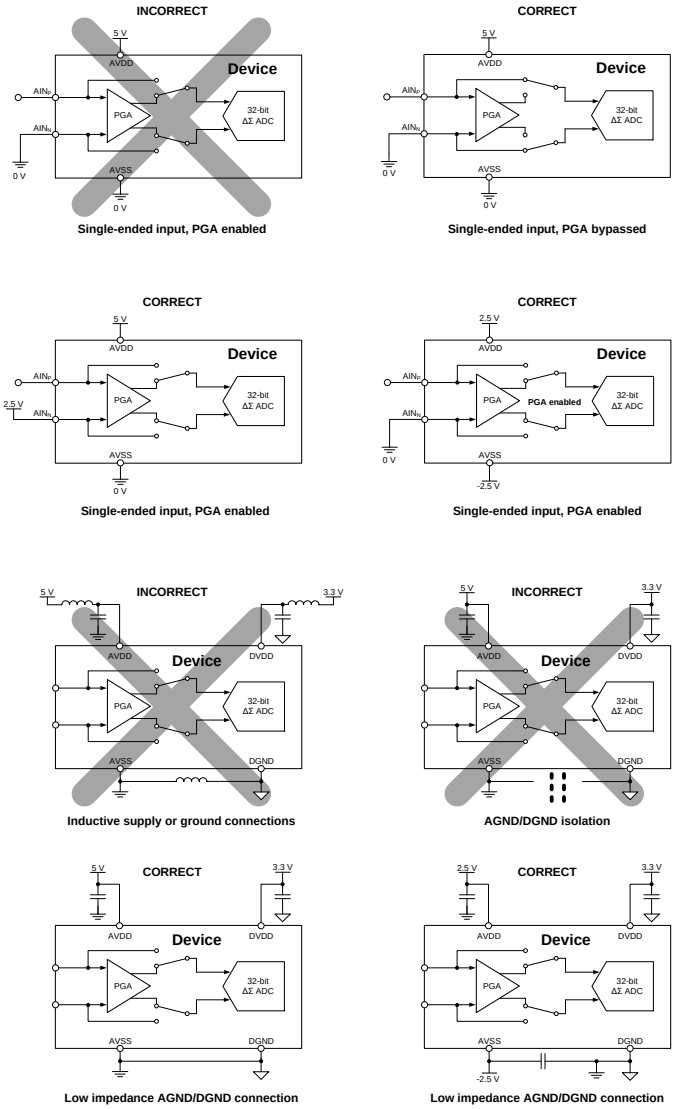


Figure 140. Do's and Don'ts Diagrams

10.4 Initialization Set Up

Figure 141 is a flow chart showing a typical configuration and measurement procedure for the ADS1262.

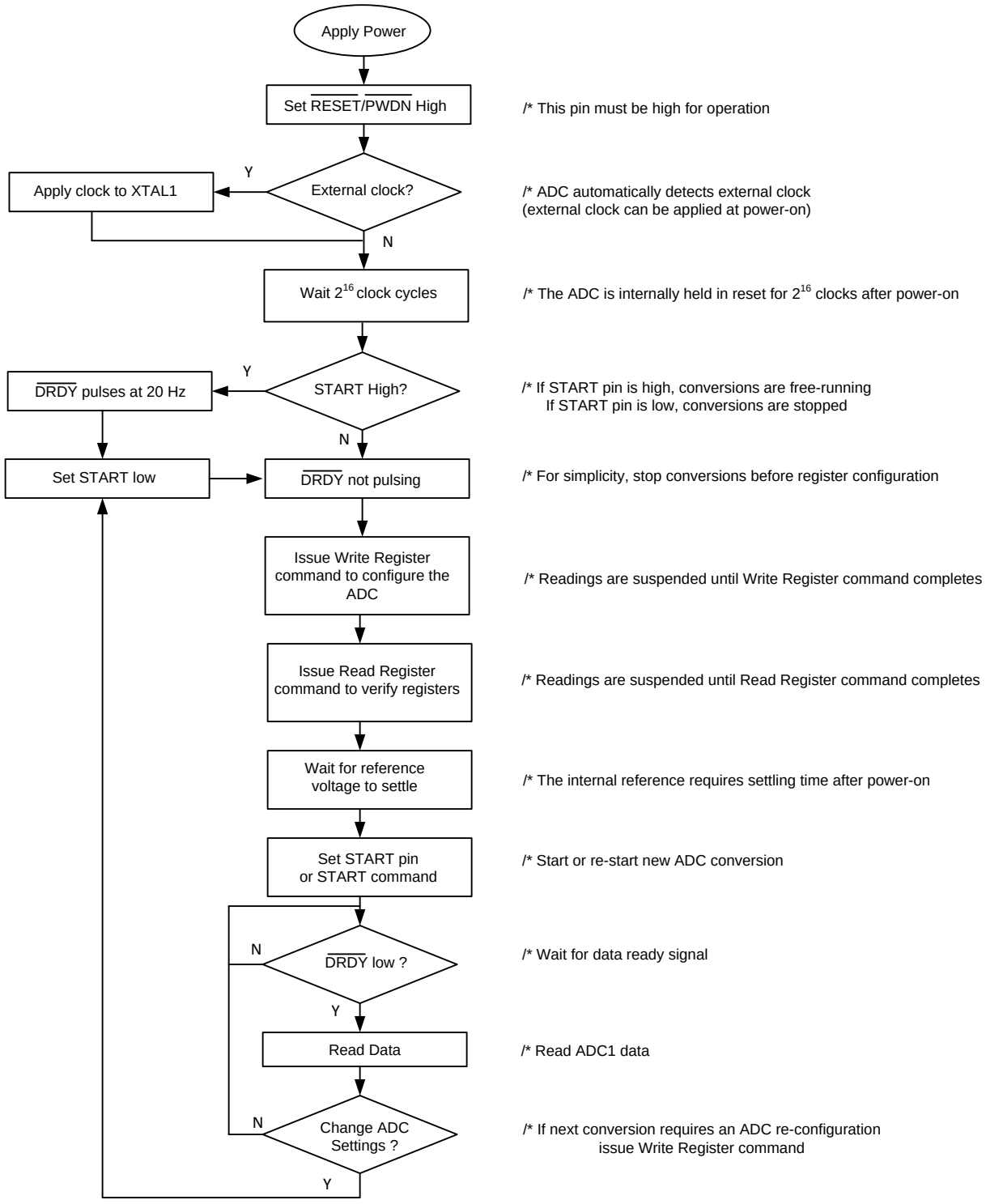


Figure 141. ADS1262 Configuration and Measurement Procedure

11 Power-Supply Recommendations

The ADS1262 and ADS1263 require an analog power supply (V_{AVDD}, V_{AVSS}) and digital power supply (V_{DVDD}). The analog power supply can be bipolar (for example, V_{AVDD} = +2.5 V, V_{AVSS} = –2.5 V) or unipolar (for example, V_{AVDD} = 5 V, V_{AVSS} = 0 V). The digital supply (V_{DVDD}) range is 2.7 V to 5.25 V. The digital supply voltage determines the digital I/O logic levels. NOTE: The GPIO logic levels (AIN3-AINCOM) are referenced to the analog supply voltage and may be different from the digital I/O logic level. The analog and digital sections of the ADC are not internally isolated and the grounds for analog and digital must be connected together. Output voltage ripple produced by switch mode regulators can interfere with the ADC and can result in reduced performance. Low drop-out regulators (LDO) should be used to reduce the power supply ripple voltage of switch-mode regulators.

11.1 Power-Supply Sequencing

The power supplies can be sequenced in any order but in no case may any analog or digital input exceed the respective analog or digital power-supply voltage limits without limiting the input fault current. The ADC is held in reset until both analog and digital power supplies exceed the respective power-on reset (POR) thresholds. Figure 99 shows the power-on reset sequence. After the power supplies have crossed the reset levels (including the infernal 2-V LDO), the ADC executes the power-on reset (POR) and is ready for communication 65536 clock periods later (nominally 9 ms).

It is recommended delaying communication 50 ms after the power supplies have stabilized within the specified range. In addition to POR, it is important that the reference voltage has fully settled before starting the conversions. When using a 1-µF reference capacitor allow a minimum of 50 ms for the internal reference to settle after power up. External references may require additional settling time.

11.2 Power-Supply Decoupling

Good power-supply decoupling is important in order to achieve optimum performance. Power supplies V_{AVDD}, V_{AVSS} and V_{DVDD} must be decoupled to a common ground potential. It is recommended that a 0.1-µF capacitor be placed as close as possible to the supply with an additional 1-µF bulk capacitor placed nearby. Figure 142 shows decoupling for bipolar supply and single supply operation. When using bipolar supplies, it is recommended to bypass both AVDD and AVSS to ground separately, and including a bypass capacitor between AVDD and AVSS. Use a multi-layer ceramic chip capacitors (MLCCs) that offers low equivalent series resistance (ESR) and equivalent series inductance (ESL) characteristics for power-supply decoupling purposes. The BYPASS pin is the bypass output of an internal 2-V regulator. The 2-V regulator powers the digital circuitry. Connect a ceramic or tantalum 1uF capacitor from this pin to DGND. Do not load this voltage by external circuits.

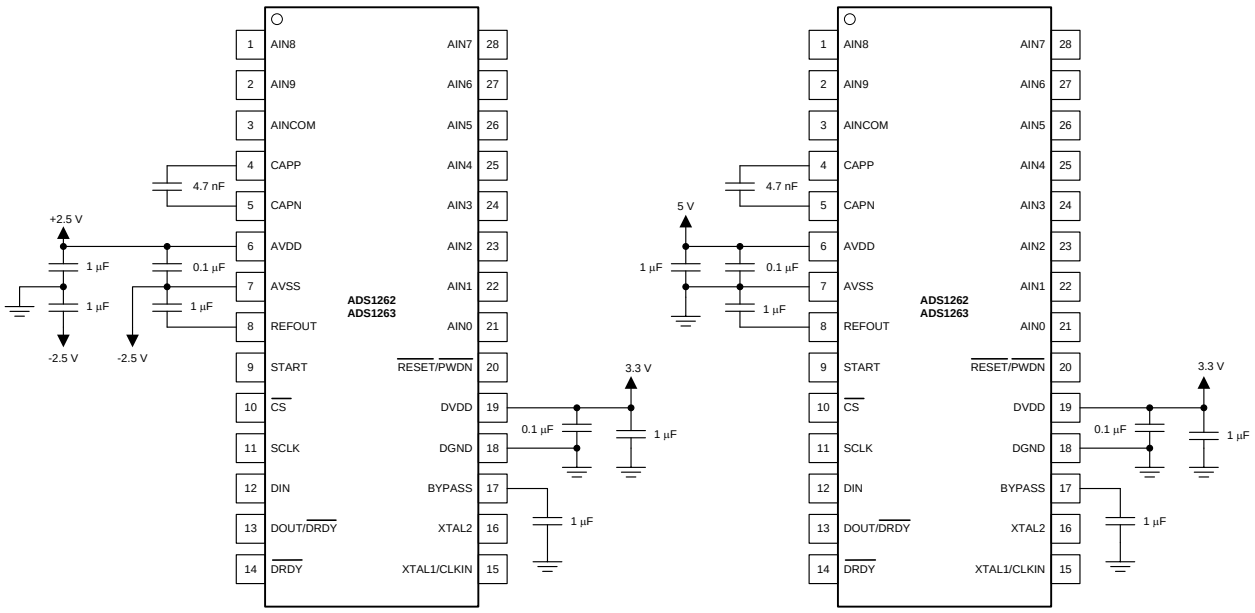


Figure 142. Power-Supply Decoupling

11.3 Analog Power-Supply Clamp

It is important to evaluate circumstances when an input signal may be present while the ADC power is present or not present. When the input signal exceeds the power-supply voltage, it is possible the analog power supply voltage can be back-driven by the input signal, through a conduction path in the internal diodes. Backdriving the ADC power supply can also occur when the ADC supply voltage is on. The fault current path is illustrated in the Figure 143. Depending on the external power supply components, it is possible to exceed the maximum analog supply voltage. Power supply over-voltage of the ADC must be prevented in all cases. One solution is to clamp the AVDD to AVSS voltage with an external 6-V Zener diode.

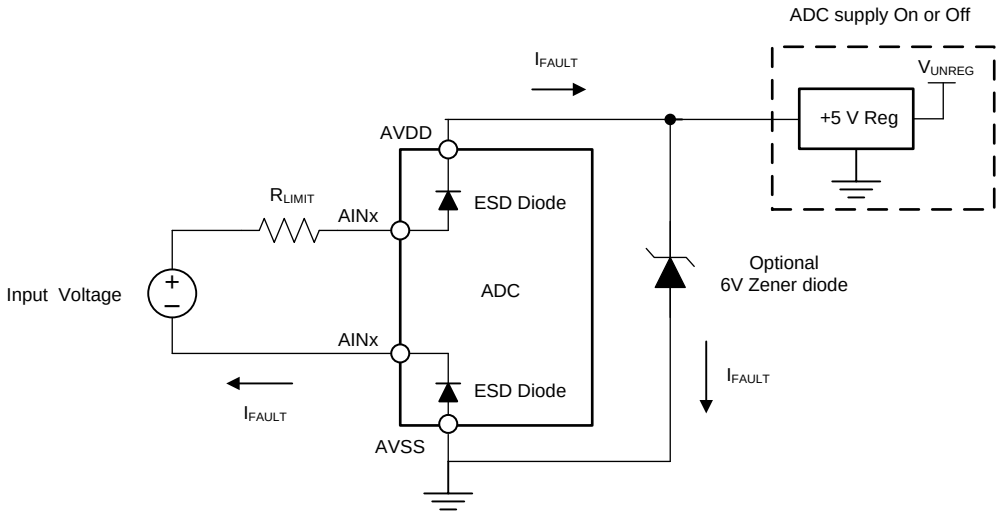


Figure 143. Analog Power-Supply Clamp

12 Layout

Good layout practices are crucial to realize the full-performance of the ADS1262 and ADS1263. Poor grounding can quickly degrade the noise performance of the main 32-bit ADC and auxiliary 24-bit ADC. The following layout recommendations are given to help provide best results.

12.1 Layout Guidelines

Ground should be a low impedance connection for return currents to flow undisturbed back to their respective sources. It is recommended that an entire PCB layer is dedicated to a ground plane and that no other signal traces be routed on this layer. Connections to the ground plane should be kept as short and direct as possible. When using vias to connect to the ground layer it is beneficial to use multiple vias in parallel to reduce impedance to ground.

A mixed signal layout can sometimes incorporate separate analog and digital ground planes that are tied together at one location; however, separating the ground planes is not necessary when analog, digital and power supply components are properly placed. Proper placement of components partitions the analog, digital and power supply circuitry into different PCB regions to prevent digital return currents from coupling into sensitive analog circuitry. If ground plane separation is necessary, then make the connection at the ADC. Connecting individual ground planes at multiple locations creates ground loops, and is not recommended. A single ground plane for analog and digital avoids ground loops.

If isolation is required in the application, isolate the digital signals between the ADC and controller, or provide the isolation from the controller to the remaining system. if an external crystal is used to provide the ADC clock, place the crystal and load capacitors directly to the ADC pins using short direct traces. See Crystal Oscillator.

Supply pins must be bypassed with a low-ESR ceramic capacitor. The placement of the bypass capacitors must be close as possible to the supply pins using short, direct traces. The ground-side connections of the bypass capacitors must also be low-impedance connections for optimum performance. The supply current flows through the bypass capacitor pin first and then to the supply pin to make the bypassing most effective (also known as a *Kelvin connection*). If multiple ADCs are on the same PCB, use wide power supply traces or dedicated power supply planes to minimize the potential of cross-talk between ADCs.

If external filtering is used for the analog inputs, use C0G type ceramic capacitors when possible. C0G capacitors have stable properties and low noise characteristics. Ideally, differential signals should be routed as pairs to minimize the loop area between the traces. For the ADC CAPP and CAPN pins, place the 4.7 nF C0G capacitor close to the pins using short direct traces. Route digital circuit traces (such as clock signals) away from all analog pins. Note the internal reference output return shares the same pin as the AVSS power supply. To minimize coupling between the power supply trace and reference return trace route the two traces separately, ideally as star connection at the AVSS pin.

It is important the SCLK input of the serial interface is free from noise and glitches. Even with relatively slow SCLK frequencies, short digital signal rise and fall times may cause excessive ringing and noise. It is recommended to keep the digital signal traces short, use termination resistors as needed, and ensure all digital signals are routed directly above the ground plane with minimal use of vias.

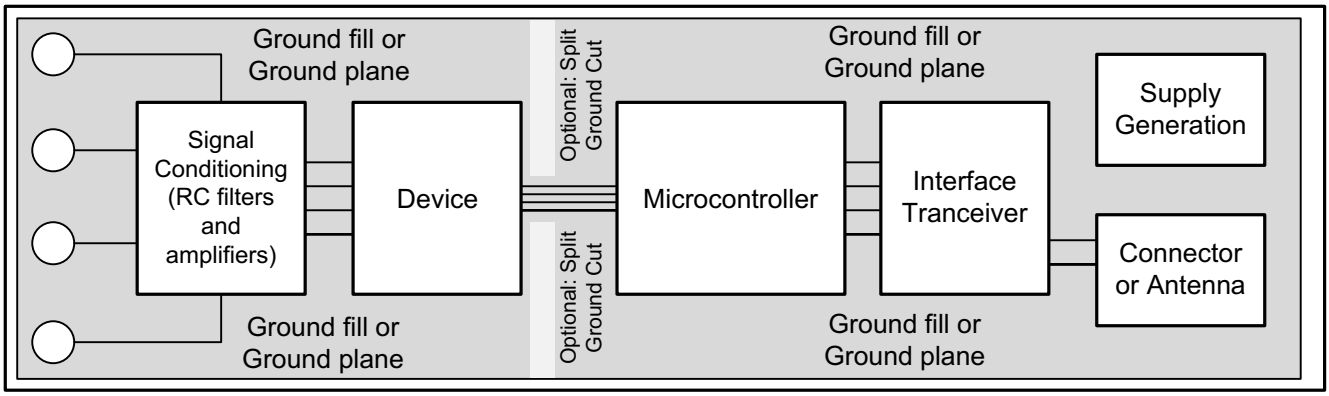


Figure 144. System Component Placement

12.2 Layout Example

Figure 145 is an example layout of the ADS1262/1263 requiring a minimum three PCB layers. The example circuit is shown for a single analog supply (5 V) connection and an external crystal oscillator. In this example, an inner layer is dedicated to the ground plane and the outer layers are used for signal and power traces. If a four-layer PCB is used, the additional inner layers can be dedicated to route power traces. The ADC orientation is shown left to right to minimize crossover of the analog and digital signal traces. The PCB is partitioned with analog signals routed from the left, digital signals routed to the lower-right, and power routed from the upper-right. Analog supply bypass capacitors are placed opposite to the ADC on the bottom layer to allow the reference and PGA output capacitors to be placed closer to the ADC.

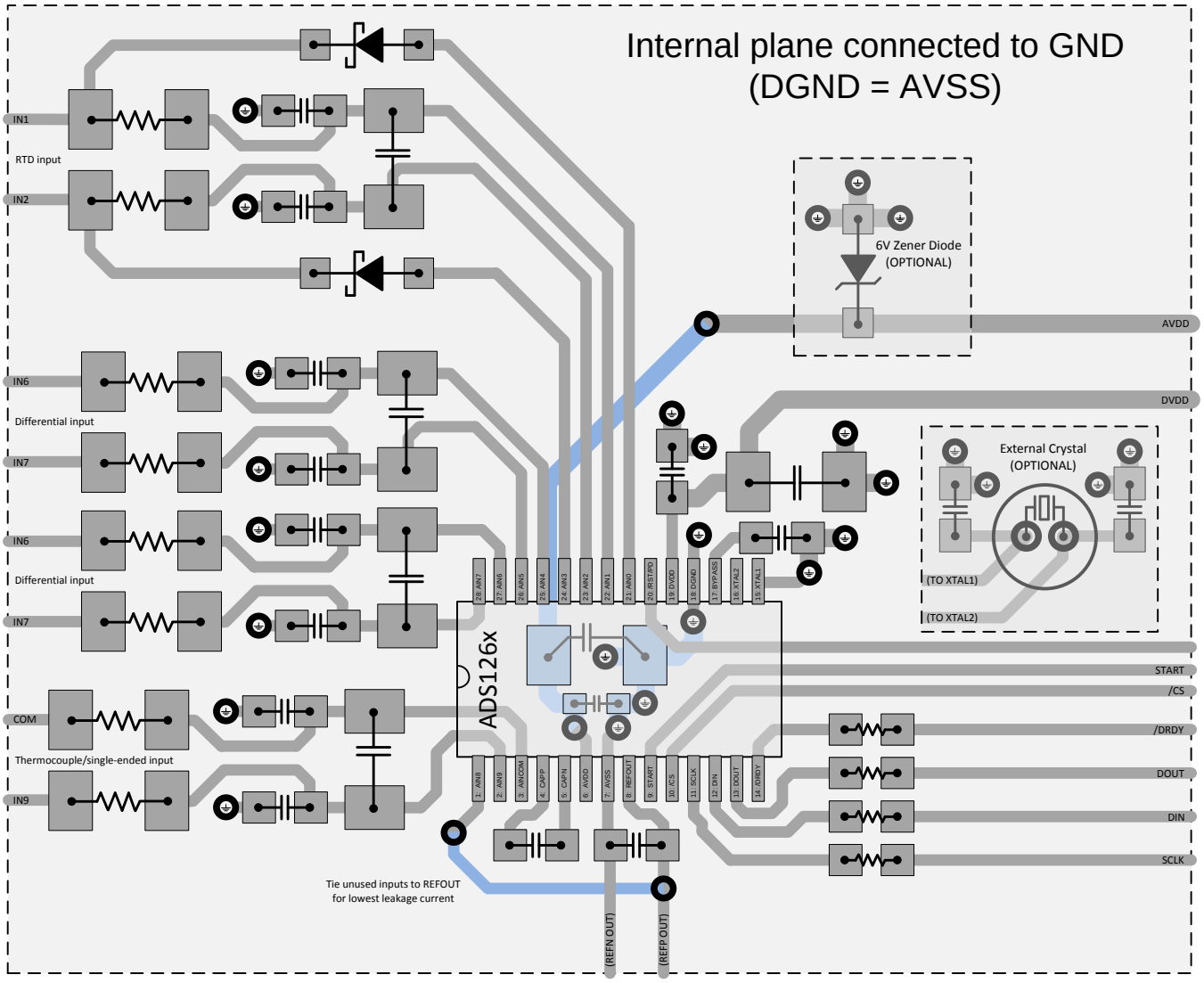


Figure 145. PCB Layout Example

13 Device and Documentation Support

13.1 Related Links

Table 54 below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 54. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS1262	Click here	Click here	Click here	Click here	Click here
ADS1263	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
SPI is a trademark of Motorola Inc.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1262IPW	PREVIEW	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1262	
ADS1262IPWR	PREVIEW	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1262	
ADS1263IPW	PREVIEW	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1263	
ADS1263IPWR	PREVIEW	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1263	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

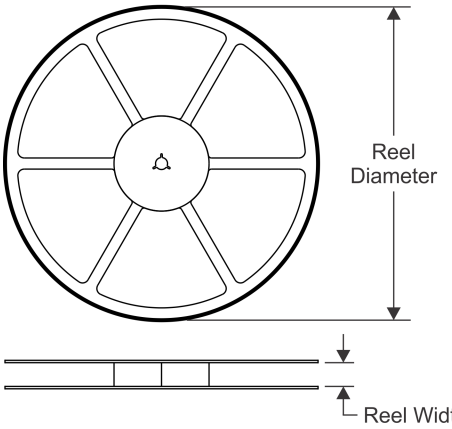
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

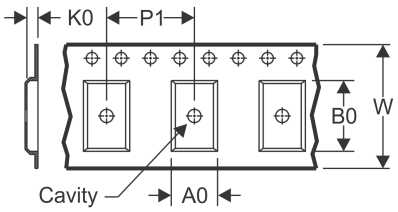
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

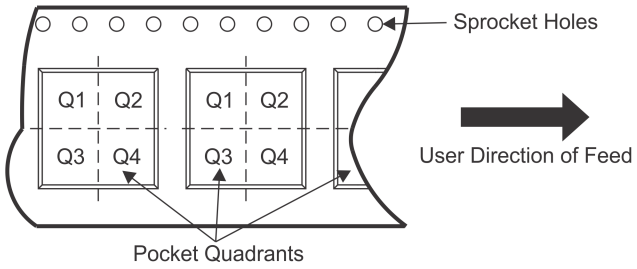


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

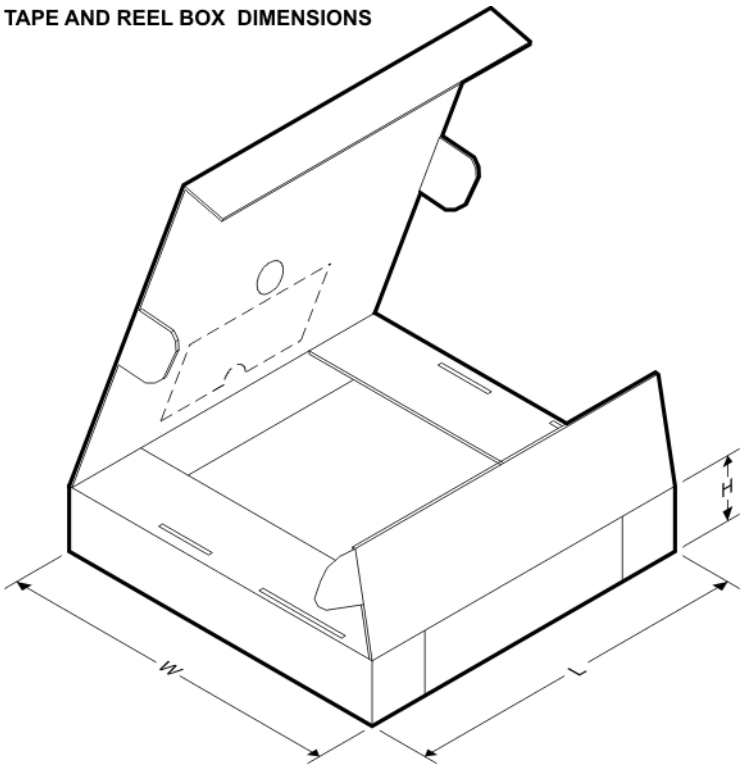
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1262IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

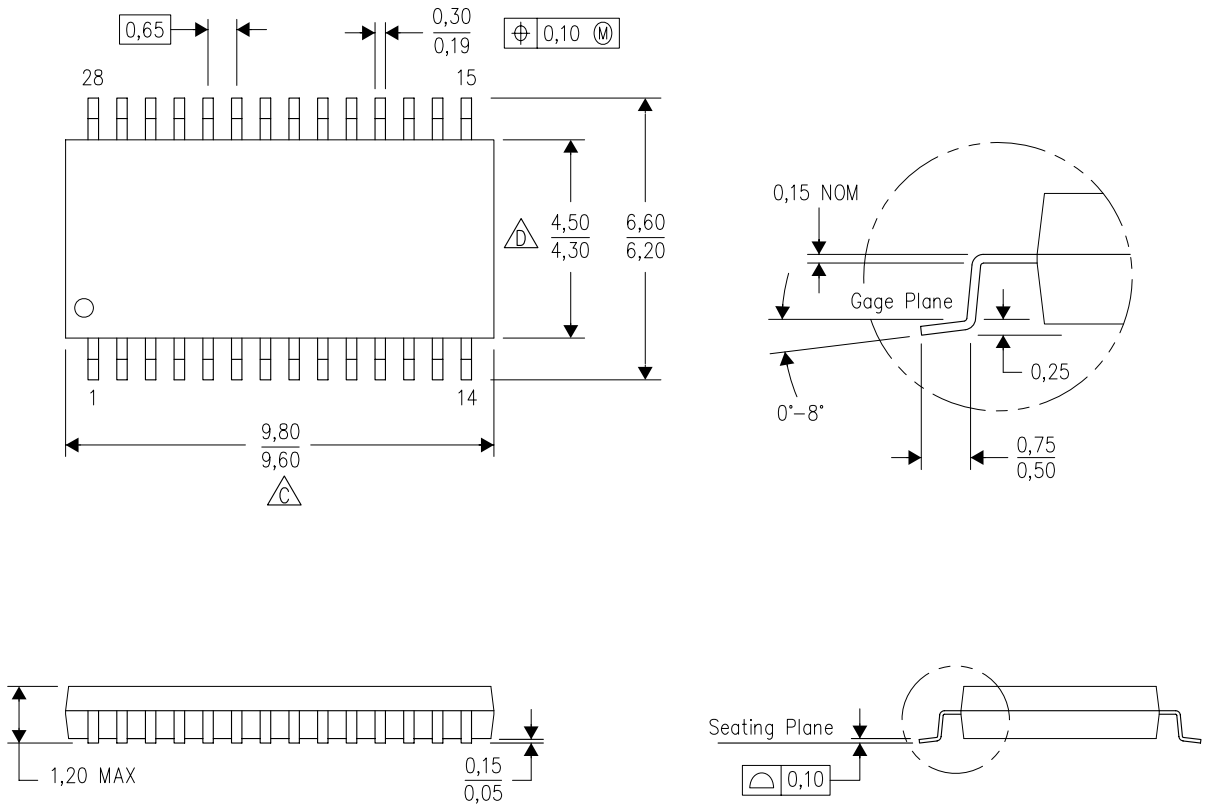
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1262IPWR	TSSOP	PW	28	2000	367.0	367.0	38.0

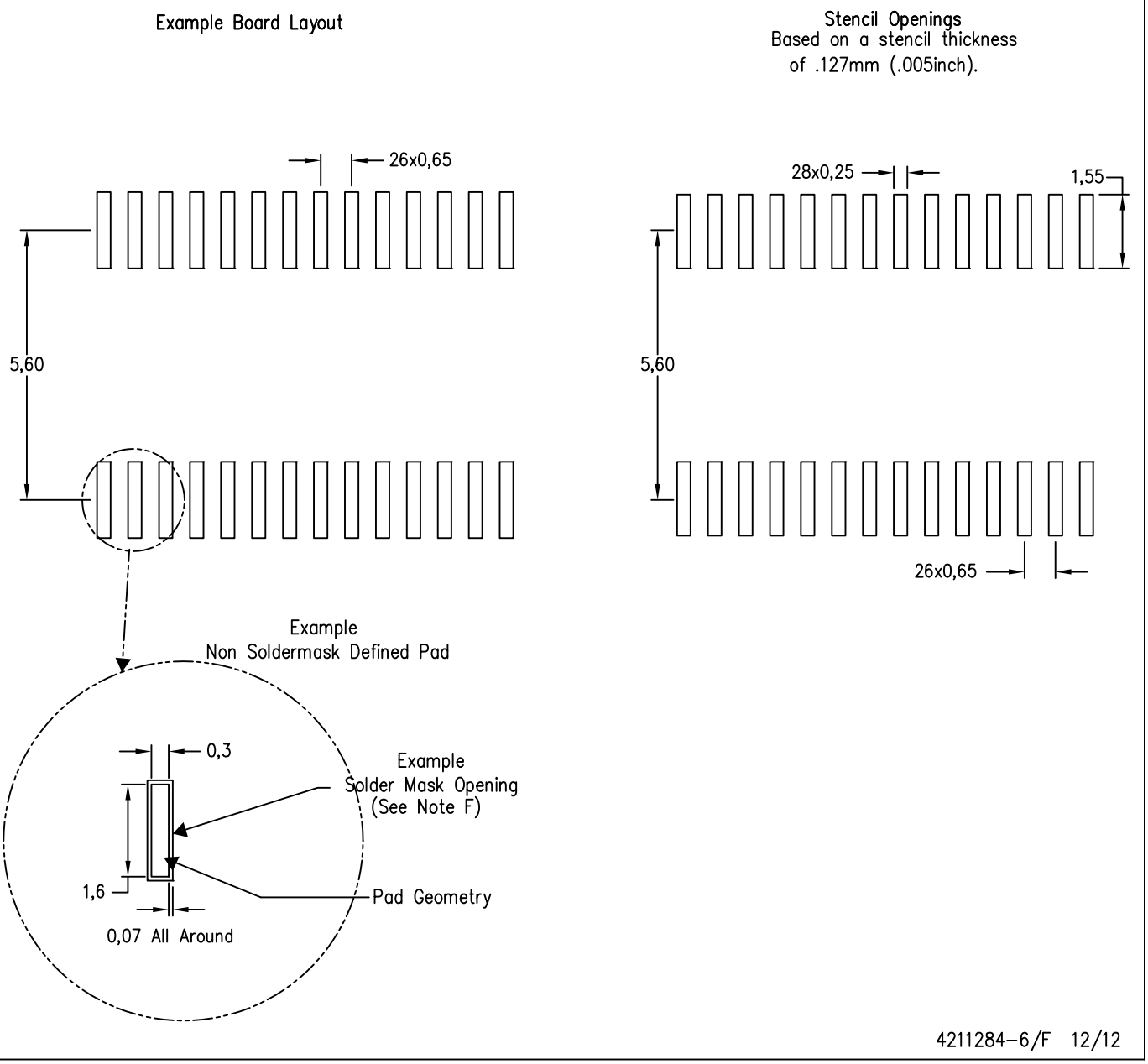
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

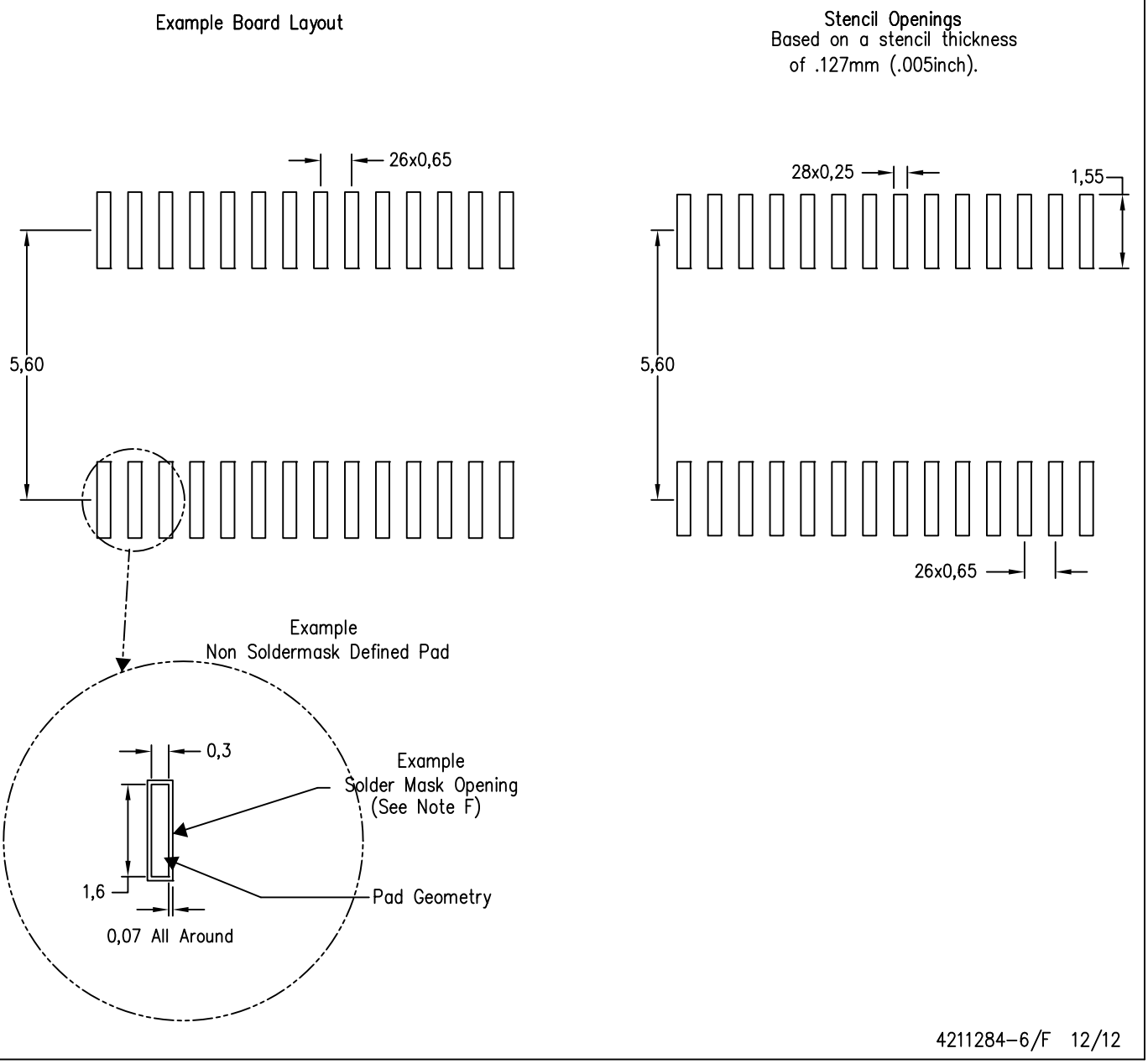
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
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E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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