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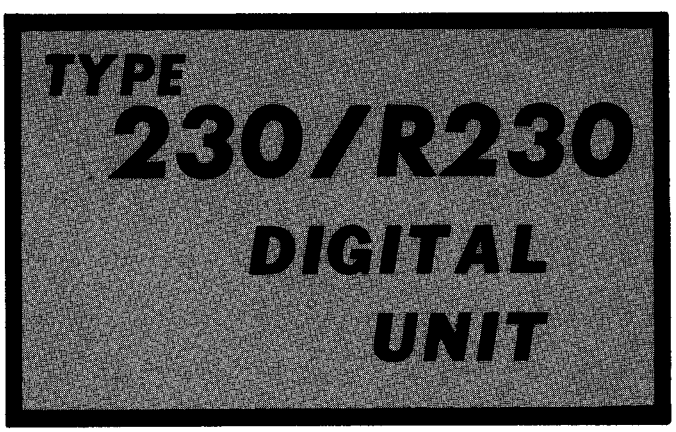
INSTRUCTION MANUAL

Serial Number _____



Tektronix, Inc.
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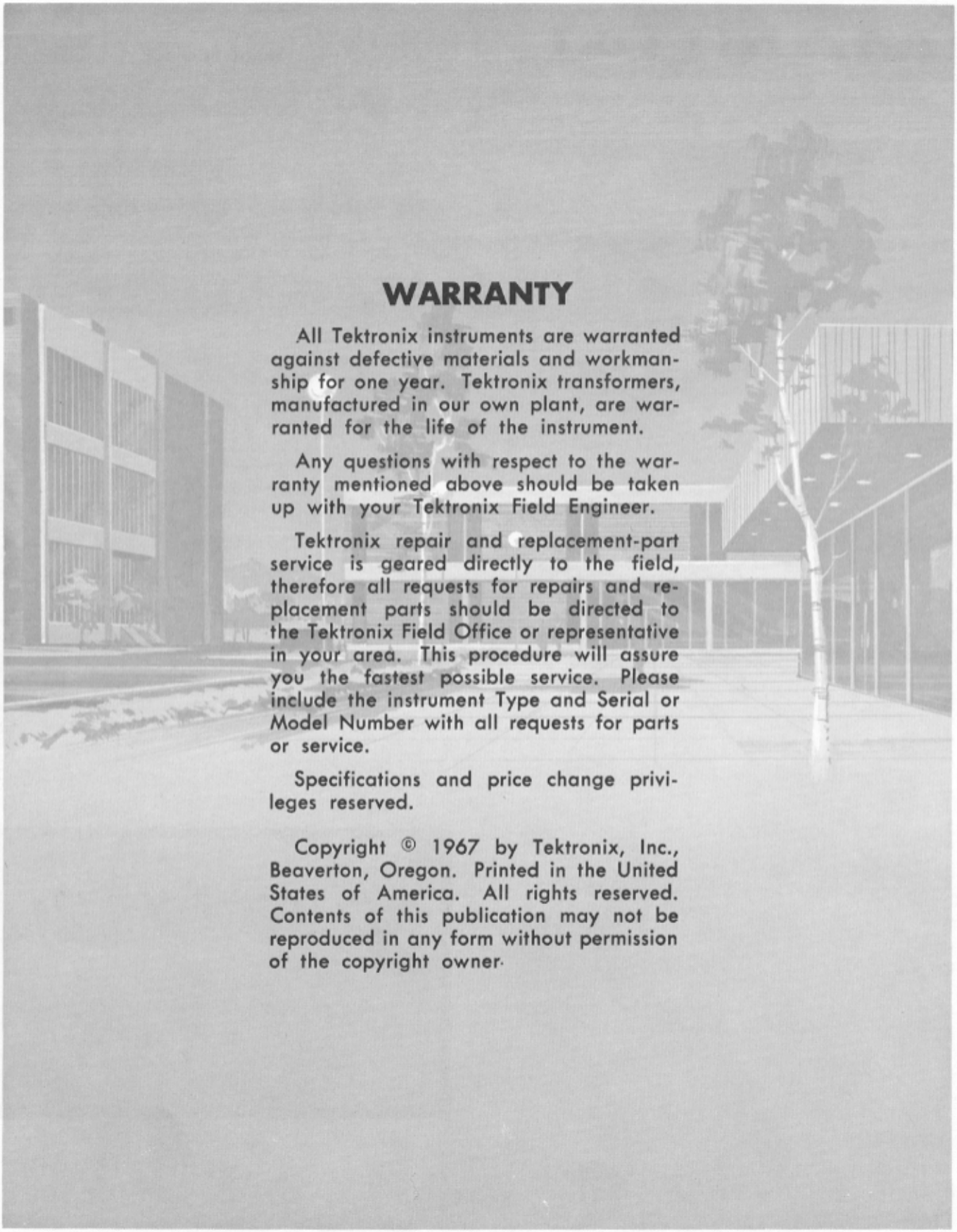
070-0635-00



WARRANTY

All Tektronix instruments are warranted against defective materials and workmanship for one year. Tektronix transformers, manufactured in our own plant, are warranted for the life of the instrument.

Any questions with respect to the warranty mentioned above should be taken up with your Tektronix Field Engineer.

Tektronix repair and replacement-part service is geared directly to the field, therefore all requests for repairs and replacement parts should be directed to the Tektronix Field Office or representative in your area. This procedure will assure you the fastest possible service. Please include the instrument Type and Serial or Model Number with all requests for parts or service.

Specifications and price change privileges reserved.

CONTENTS

Abbreviations and symbols used in this manual are based on or taken directly from IEEE Standard 260 "Standard Symbols for Units", MIL-STD-12B and other standards of the electronics industry. The logic symbology is based on MIL-STD-806. Change information, if any, is located at the rear of this manual.

Fig. 1-1. The Type 230 Digital Unit.

SECTION 1
CHARACTERISTICS

General Information

The Type 230/R230 Digital Unit is designed for use with the Tektronix Type 568 Oscilloscope as part of a digital readout system for making automatic digital measurements of voltage, time between percentage points, and time between pulses on one or two waveforms. All functions of the Type 230 are programmable, making the instrument appropriate for applications requiring a variety of measurements that can be changed in rapid sequence. The Type 230 may also be operated from the front panel controls, although the functions of the instrument are limited as compared to those available with external programming. The Type 230 provides front panel readouts including + or —, unit of measure, and a 4-digit numerical readout. Go-no-go limits are also indicated. Rear panel connectors provide inputs for external programming, and binary-coded-decimal outputs of the front panel information.

The instrument is designed to operate over an ambient temperature range of 0° C to +60° C. Performance specifications given in this section apply over this temperature range after a 5-minute warmup period, provided the instrument has been calibrated at +25° C ±5° C. Additional information describing some characteristics and features is also included where needed in this portion of the manual. Characteristics given under Operational Information are not specifications in themselves and are not necessarily checked in the performance check or calibration procedure.

Information given in this instruction manual applies to both the Type 230 and Type R230 unless otherwise specified. The Type R230 is electrically identical to the Type 230, but is equipped with front panel pull handles and slide-out tracks for rackmounting in a standard 19-inch rack. Rackmounting instructions, a mechanical parts list and a dimensional drawing of the Type R230 are provided in Section 8.

Thoughout the text, each plug-in circuit card is referred to either by the circuit number of the plug (which constitutes the edge of the card) or by the circuit number of the jack into which the card is plugged. For example, the Buffer may be referred to either as P5 or J5. When reading the text, consider that these plug and jack circuit numbers are interchangeable.

OPERATING CHARACTERISTICS

Characteristics	Operating Information	
Input	External from a Tektronix Type 568 Oscilloscope.	
Units of Measure[1]		
Volts	Readout in millivolts (MV) and volts (V).	
Time	Readout in nanoseconds (NS), microseconds (μS), milliseconds (MS), and seconds (S).	
Numerical Range[1]	Readout from —3999 to +3999.	
Display Time[1]	Variable from 0.01 second to 10 seconds,	
Preset Limits Range[1]		
Upper	From —3999 to +3999	
Lower	From —3999 to +3999	
	Externally Programmed	Front Panel Operation
Time Measurement Start and Stop Point Range		
% Between Zones	0% to 159%	0% to 99%
Vertical Millimeters Offset	0 mm to 159 mm above or below the reference zone	0 mm to 99 mm above the 0% zone, 0 mm to 99 mm below the 100% zone.
	No more than 80 mm of offset is usable, since only 80 mm of vertical display is available.	
Horizontal Millimeters Offset	1 mm to 159 mm from sweep start. No more than 105 mm is usable.	1 mm to 99 mm from sweep start.

ELECTRICAL CHARACTERISTICS

Characteristics	Performance Specification
Zone Generators, Ch A and Ch B, 0% and 100%, P1 and P2.	
Zone Position	Horizontal increments of 0.5 major division from sweep start.
Accuracy	Within 1 minor division of position programmed.
Zone Width	0.3 cm, 2 cm, 4 cm or 10 cm (to end of sweep) from start of zone.

[1]Digital readout from Nixie tubes on Type 230. All references to major or minor divisions of display refer to Analog readout from Type 568 CRT. Nixie Trademark Burroughs Corporation.

Characteristics	Performance Specification
Accuracy	Within 1 mm when programmed for 0.3 cm width; within 10% when programmed for 2 cm or 4 cm width.
Memories, Ch A and Ch B, 0% and 100%, P3 and P4.	
Memory Output Level	−0.6 V to +5.4 V.
Accuracy	Within 6 mV of input voltage.
Leak Down	30 mV or less in 10 seconds.
Peak Charge Time	15 μs of zone or peak signal time.
Buffer, P5	
Ch A and Ch B Signal Gain	0.5 V/div output for 1.0 V/div input.
Output Level	+2.15 V ±0.10 V output for +10.0 V DC input.
5 V RAMP	
Gain	0.5 V/div ±0.5% for 5 V/div input; adjustable to 0.5 V/div ±0.2%.
Linearity	Within 1% of input linearity.
DC Level	0.0 V ±20 mV for 0.0 V input; adjustable to 0.0 V ±1 mV.
50 V RAMP	
Gain	Adjustable to give proper zone position at 9th graticule line.[2]
VOLTMETER RAMP	Adjustable, 5 mV/μs, 2.5 mV/μs, and 10 mV/μs.
Linearity	Within 0.25%.
Comparators, P6 and P7	
Signal Input Range	At least −1.0 V to +5.0 V.
Offset Voltage Out	±50 mV to ±4.95 V.
Accuracy	Within 0.25% ±2 mV of programmed offset.
Offset Tracking Accuracy	Within 1 mV of input reference, from +0.15 V to +4.15 V.
% Offset Gain	0% to 99% of voltage difference between 0% and 100% memory levels.
Accuracy	Within 0.25% ±2 mV of programmed voltage.
External Control	
Plus Trigger (J204-Pin 29)	Positive step of 4 volts or more, having a ristime of 1 microsecond or less.
Minus Trigger (J204-Pin 30)	Negative step of 4 volts or more, having a negative-going risetime of 1 microsecond or less.

ENVIRONMENTAL CHARACTERISTICS

Characteristics	Performance Specification
Ambient Temperature Range	
Operating	0° C to +60° C
Non-operating	−40° C to +65° C
Maximum Altitude	
Operating	15,000 feet
Non-operating	50,000 feet
Vibration (Operating)	Performs within specifications after being vibrated for 15 minutes along each axis at frequencies from 10 c/s to 50 c/s and accelerations up to 1.9 g.
Shock (Non-operating)	Performs within specifications after being subjected to guillotine type shocks of 30 g's one-half sine, 11 millisecond duration. One shock each direction along each axis (total of 6 shocks).
Transportation (Non-operating) Vibration	Performs within specifications after transportation package has been vibrated for 1 hour at accelerations up to 1 g.
Drop Test	Performs within specifications after transportation package has been dropped from a height of 30 inches on one corner, on each edge radiating from that corner and on each flat side of the package.

[2]**Model 1 not independently adjustable.**

MECHANICAL CHARACTERISTICS

Characteristics	Description
Construction	
Chassis and cabinet	Aluminum alloy
Front panel	Anodized aluminum alloy
Circuit cards	Epoxy laminate with etched wiring
Approximate Dimensions	
Type 230	
Height	8 inches, including feet
Width	16⅞ inches
Depth	22 inches, including knobs and rear-panel feet
Type R230	
Height	7 inches
Width	16⅞ inches; fits into a standard 19 inch rack
Depth	22¾ inches, including handles and rear-panel feet
Connectors	
Input, programming and readout (rear panel)	Microribbon type 36-terminal jacks (total of 6)
Ventilation	Forced filtered air; overheat protection by means of thermal relay.

POWER SOURCE ELECTRICAL REQUIREMENTS

Characteristic	AC RMS Operating Range	Operational Information
Line Voltage		Power connection changed by means of rear-panel line-selector assembly; normally set for 115 VAC. Medium operating range when shipped from the factory.
Low		
100 VAC Nominal	90 volts to 110 volts	
200 VAC Nominal	180 volts to 220 volts	
Medium		
115 VAC Nominal	104 volts to 126 volts	
230 VAC Nominal	208 volts to 252 volts	
High		
124 VAC Nominal	112 volts to 136 volts	
248 VAC Nominal	224 volts to 272 volts	
Line Frequency	48 to 66 Hz	
Power Consumption		130 W maximum

NOTES

SECTION 2
OPERATING INSTRUCTIONS

General Information

This section of the manual provides the basic information required for operating the Type 230. Instructions are included for installing the instrument, using the front-panel controls and connecting the input and output signals from the indicator oscilloscope. For remote operation, refer to Section 3 Programming Instructions.

Rackmounting

Instructions for rackmounting the Type 230 are given in the Rackmounting foldout pages of Section 11. After the slide-out tracks have been installed in the rack, the Type 230 may be removed or re-inserted at any time as described in the Rackmounting section.

Operating Voltage

The Type 230 may be operated from either a 115-volt or 230-volt nominal line voltage source. The LINE VOLTAGE SELECTOR assembly, located on the rear panel, converts the instrument from one operating range to the other (115 or 230 volts). This assembly also allows selection of one of three regulating ranges and contains the two line fuses. When the instrument is converted from one nominal line voltage source to the other, the assembly connects or disconnects one of the fuses to provide the proper protection for the power transformer.

Use the following procedure to convert this instrument between line voltages or regulating ranges:

1. Disconnect the instrument from the power source.

2. Remove the two captive screws which hold the cover to the assembly and remove the cover.

3. To convert to a different line voltage, pull out the Voltage Selector switch bar (Fig. 2-3), turn it around 180° and plug it into the opposite set of holes. The Voltage Selector switch bar will be in the upper position for 115-volt operation and in the lower position for 230-volt operation.

4. To change regulating ranges, pull out the Range Selector switch bar (Fig. 2-1), slide it to the desired range and plug it back in. Select a range which is centered about the average line voltage to be applied (see Table 2-1).

5. Re-install the cover and the two captive screws. Be sure the cover fits firmly against the rear panel. This ensures that the line fuses are installed correctly.

6. Before applying power to the instrument, check that the indicating tabs on the switch bars protrude through the proper holes of the cover for the correct line voltage and regulating ranges.

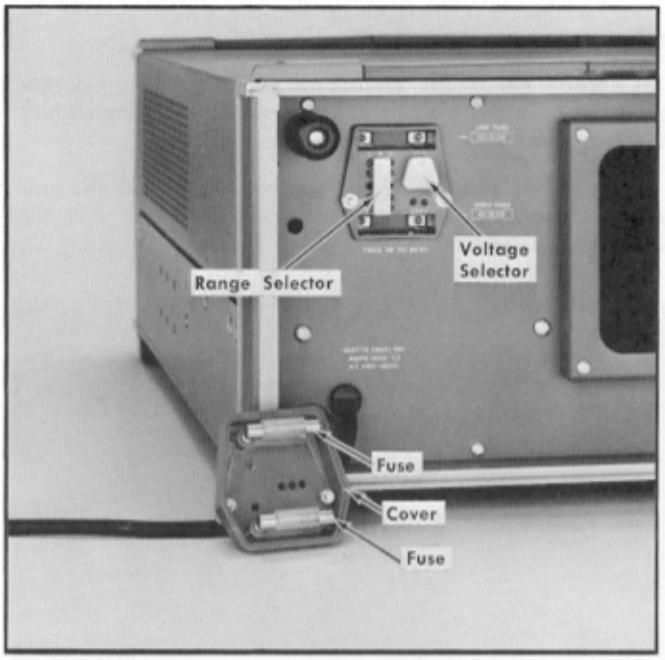


Fig. 2-1. Line Voltage Selector assembly with cover removed. Shown set for 115-Volt medium-range operation.

CAUTION

The Type 230 should not be operated with the Voltage Selector or Range Selector switches in the wrong position for the line voltage applied. Operation of the instrument with either switch in the wrong position will provide incorrect operation or damage the instrument.

TABLE 2-1

Regulating Ranges

Range Selector Switch Positions	Regulating Ranges
LO (switch bar in left position)	90 to 110 volts (180 to 220 volts)
M (switch bar in center position)	104 to 126 volts (208 to 252 volts)
HI (switch bar in right position)	112 to 136 volts (224 to 272 volts)

It may be necessary to use a 115-volt to 230-volt adapter to match the power plug to the power-source receptacle, or the power cord and plug may be changed. Use the following procedure to change the power cord.

a. Disconnect the power plug from the power source.

b. Unsolder the ground wire (green) from the ground lug (see Fig. 2-2).

c. Unsolder the black wire and the white wire from the ceramic strip. If you are not familiar with soldering techniques used on ceramic strips refer to Soldering Techniques in the maintenance section.

d. Compress the strain relief and pull the power cord out through the rear panel.

e. Cut and strip the leads on the new power cord to the same length as those on the old cord.

f. Install the power cord through the hole in the rear panel and solder the leads to the same terminals from which the previous cord was removed; (see Fig. 2-2).

g. Place the strain relief on the power cord near the rear panel, compress the strain relief and re-install it into the hole in the rear panel.

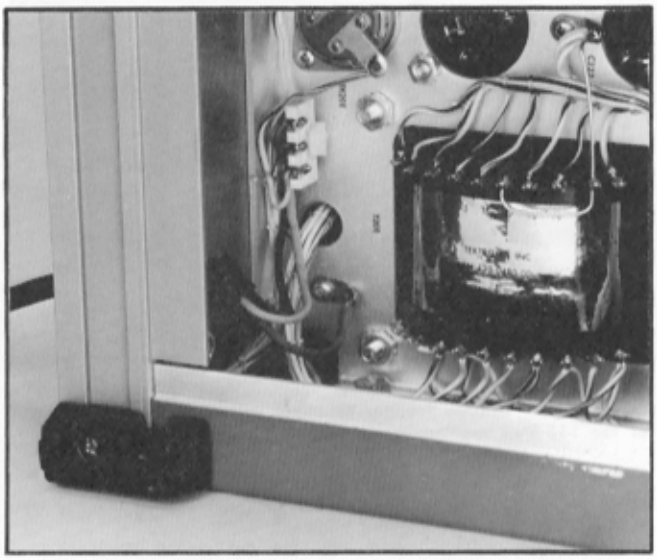


Fig. 2-2. Bottom view of the Type 230 showing the location of the ground lug and input connections required for changing the power cord.

Definition of Terms

Some terms are used throughout this manual that may appear confusing to an operator unfamiliar with Tektronix digital readout terminology.

ZONES. The Type 230 produces three intensified zones on Channel A and/or Channel B trace of the Type 568 Oscilloscope; the 0% zone, the 100% zone and the time measurement zone. Each zone appears as a brightened portion of the trace (Fig. 2-3).

The 0% and 100% zone position and width are determined by the setting of the REF ZONE-POSITION and WIDTH controls.

The time measurement zone is only produced on a time measurement. Its width and position depend on the setting of the TIME MEASUREMENT START and STOP POINT controls. The time measurement zone intensifies the portion of the display being measured.

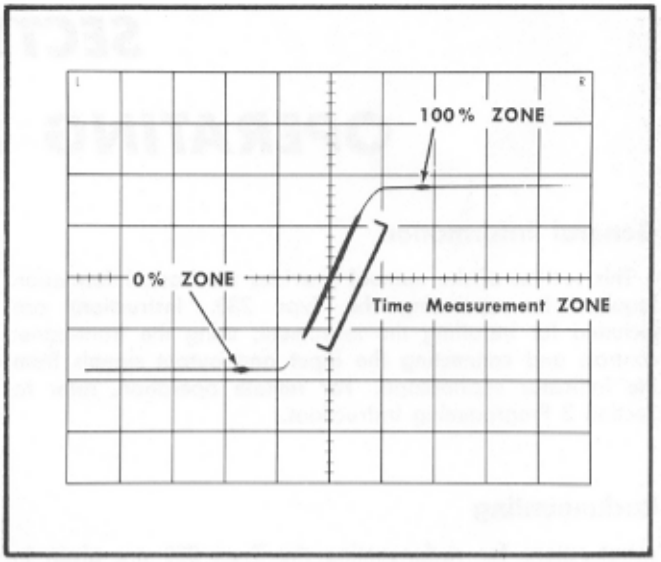


Fig. 2-3. Three types of intensified zones.

SLOPE. Refers to the rising or falling portion of a pulse or waveform which is being presented on the CRT of the Type 568 Oscilloscope. Two types of slopes will be referred to; a positive slope (rising) and a negative slope (falling). See Fig. 2-4 for pulse slope definitions.

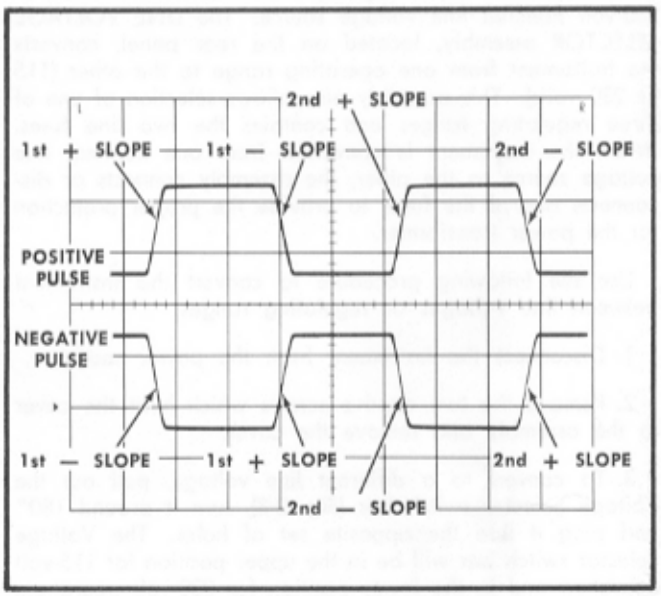


Fig. 2-4. Pulse slope definitions.

FUNCTION OF FRONT PANEL CONTROLS, SWITCHES AND INDICATORS

MEASUREMENT MODE Switch — Selects operating mode of instrument for the type of measurement to be made.

TIME—Used for all time measurements.

A VOLTS—Used for voltage measurements of the waveform on channel A of the vertical plug-in unit in the Type 568.

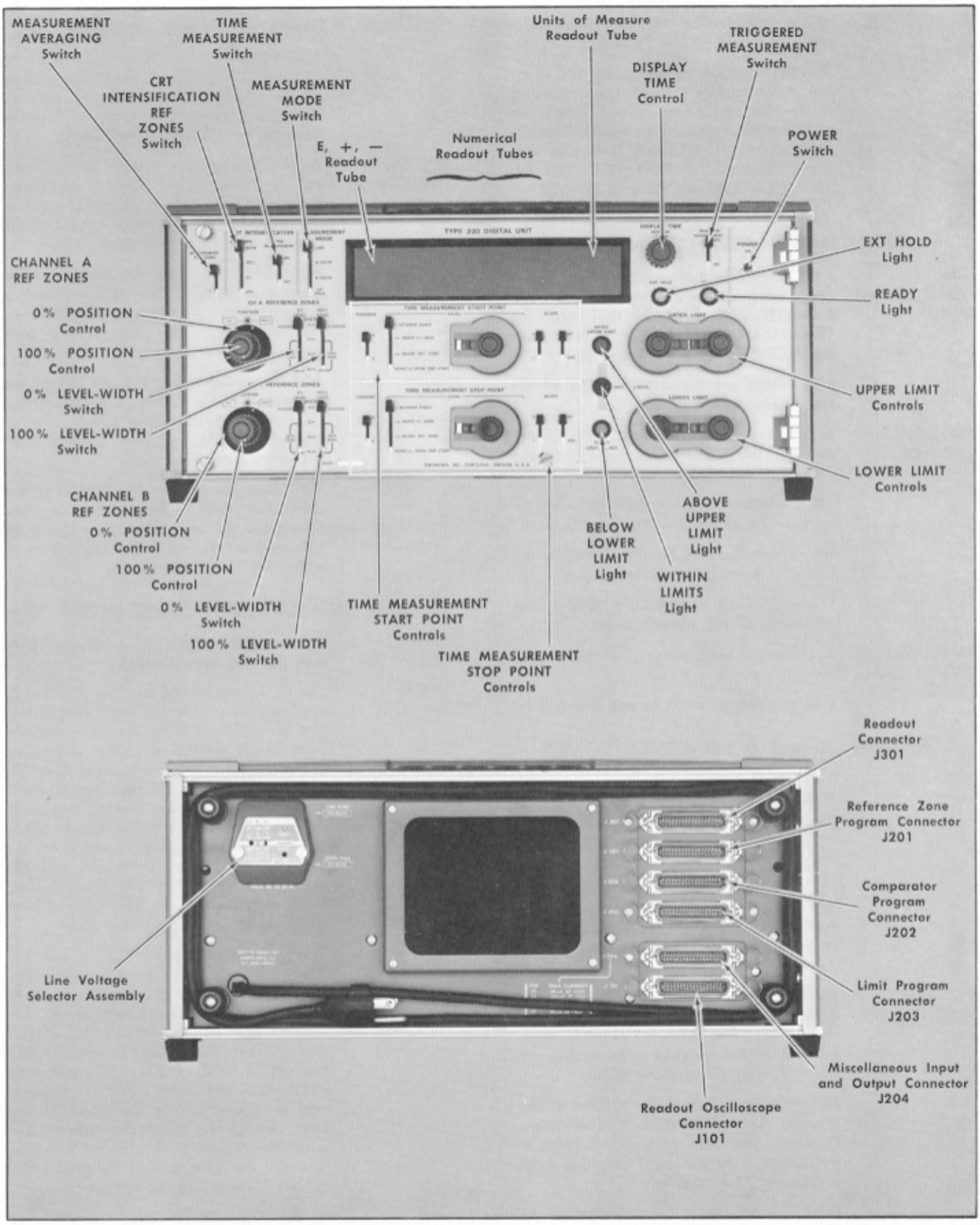


Fig. 2-5. Front- and rear-panel controls and connectors on the Type 230.

B VOLTS—Used for voltage measurements of the waveform on channel B of the vertical plug-in unit in the Type 568.

EXT PROG—Sets up instrument for external programming through the connectors at the rear of the instrument. Disconnects all front-panel controls except TRIGGERED MEASUREMENT, DISPLAY TIME and CRT MEASUREMENT, DISPLAY TIME, CRT INTENSIFICATION, MODE and POWER.

CRT INTENSIFICATION CONTROLS

TIME MEASUREMENT Switch

ON—Intensifies that portion of the waveform being measured between the TIME MEASUREMENT START POINT and the TIME MEASUREMENT STOP POINT when the MODE switch is set to TIME.

OFF—Turns off the intensification of the time measurement.

REF ZONES Switch

BOTH—Intensifies both the 0% ZONE and the 100% ZONE on the CRT of the indicator oscilloscope.

100%—Intensifies only the 100% ZONE on the CRT of the indicator oscilloscope.

0%—Intensifies only the 0% ZONE on the CRT of the indicator oscilloscope.

OFF—Turns off both the 0% ZONE and the 100% ZONE intensifications.

MEASUREMENT AVERAGING Switch

8—Averages measurement of eight consecutive sweeps.

1—Measurement made on one sweep only.

CHANNEL A and B REFERENCE ZONES

POSITION Switch

0% (Outer Knob)—Positions the 0% ZONE on the channel A waveform. Moves the starting point of the intensified zone in ½ centimeter steps across the face of the CRT.

100% (Center Knob)—Positions the 100% ZONE on the channel A waveform. Moves the starting point of the intensified zone in ½ centimeter steps across the face of the CRT.

0% LEVEL-WIDTH

AVERAGE—Sets the WIDTH of the channel A 0% ZONE to 0.3 centimeters. References the start or stopping point of measurement to the average level of the signal within the 0.3 cm zone width.

NEG PEAK-2 cm—Sets the WIDTH of the channel A 0% ZONE to 2 centimeters. References the start or stopping point of measurement to the most negative peak within the 2 cm zone width.

NEG PEAK-4 cm—Sets the WIDTH of the channel A 0% ZONE to 4 centimeters. References the start or stopping point of the measurement to the most negative peak within the 4 cm zone width.

NEG PEAK-10 cm—Sets the WIDTH of the channel A 0% ZONE to 10 centimeters. References the start or stopping point of the measurement to the most negative peak within the 10 cm zone width.

100% LEVEL-WIDTH Switch

AVERAGE—Sets the WIDTH of the channel A 100% ZONE to 0.3 centimeter. References the start or stopping point of measurement to the average level of the signal within the 0.3 cm zone width.

POS PEAK-2 cm—Sets the WIDTH of the channel A 100% ZONE to 2 centimeters. References the start or stopping point of measurement to the most positive peak within the 2 cm zone width.

POS PEAK-4 cm—Sets the WIDTH of the channel A 100% ZONE to 4 centimeters. References the start or stopping point of measurement to the most positive peak within the 4 cm zone width.

POS PEAK-10 cm—Sets the WIDTH of the channel A 100% ZONE to 10 centimeters. References the start or stopping point of measurement to the most positive peak within the 10 cm zone width.

TIME MEASUREMENT START POINT

CHANNEL Switch

Selects either channel A or channel B to start the time measurement.

SLOPE Switch

The +, — switch and the 1ST, 2ND switch are used in conjunction with each other. The +, — switch allows the time measurement to be started on either a positive (+) or negative (—) going slope. The 1ST, 2ND switch allows the time measurement to be started on either the first or second positive slope, or the first or second negative slope, depending upon where the +, — switch is set. As an example, with the +, — switch set at + and the 1ST, 2ND switch set at 1ST, the time measurement will start on the first positive slope.

LEVEL Switches

Two switches are labled LEVEL—one is a rotary type, the other a lever switch. The lever switch selects one of four ways of starting the time measurement; % BETWEEN ZONES, mm ABOVE 0% ZONE, mm BELOW 100% ZONE and HORIZ mm FROM SWP START. The offset dials (rotary switches) select either the percentage or millimeters as indicated by the lever switch. The offset dials are always read directly; the outer control indicates tens and the inner control indicates units, for either percentage or millimeters.

% BETWEEN ONES—Used for measuring a specified percentage (as set by the offset dials) between the 0% zone and the

100% ZONE. As an example, for rise-time measurements, the lever switch is set at % BETWEEN ZONES and the offset dials are set at 1 and 0. The time measurement will start at the ten percent point of the waveform being measured.

mm ABOVE 0% ZONE—Used to start the time measurement a specified number of millimeters (as set by the offset dials) above the reference level of the 0% ZONE. As an example; with the lever switch set at % BETWEEN ZONES and the offset dials set at 1 and 0, the time measurement will start ten millimeters (or one centimeter) above the reference level of the 0% ZONE.

mm BELOW 100% ZONE—Used to start the time measurement a specified number of millimeters (as set by the offset dials) below the reference level of the 100% ZONE. As an example; with the lever switch set at mm BELOW 100% ZONE and the offset dials set at 1 and 0, the time measurement will start ten millimeters (or one centimeter) below the reference level of the 100% ZONE.

HORIZ mm FROM SWP START—Used to start the time measurement a specified number of millimeters after the start of the sweep. As an example; with the lever switch set at HORIZ mm FROM SWP START and the offset dials set at 15, the time measurement will start 15 millimeters (or 1½ centimeters) after the start of the sweep.

TIME MEASUREMENT STOP POINT

These controls perform the same functions as those just described under Time Measurement Start Point. However, this group of controls is concerned with the end of the time measurement.

LIMIT CONTROLS

UPPER LIMIT Switches — Sets the upper acceptable limit for either voltage or time measurements. These controls are read directly. They correspond to the readout tubes as they are read from left to right. The left inner control (+0, —0, etc.) corresponds to the left hand indicator tube (+, —) and to the first number tube. The remaining three controls correspond directly to the remaining three number tubes.

LOWER LIMIT Switches — Sets the lower acceptable limit for either voltage or time measurements. These controls are read directly. They correspond to the readout tubes as they are read from left to right. The left inner control (+0, —0, etc.) corresponds to the left hand (+, —) indicator tube and to the first number tube. The remaining three controls correspond directly to the remaining three number tubes.

ABOVE UPPER LIMIT Indicator — Lights if the number on the readout tubes is above that set on the UPPER LIMIT switches. This information is also available at the Readout connector (J301 and the Program and Control connector (J204) at the rear of the instrument.

WITHIN LIMITS Indicator Lamp — Lights if the number on the readout tubes is equal to or between the limits set on the UPPER LIMIT and LOWER LIMIT switches. This information is also available at the Readout connector (J301, and the Program and Control connector (J204) at the rear if the instrument.

BELOW LOWER LIMIT Indicator Lamp — Lights if the number on the Readout tubes is lower than that set on the LOWER LIMIT switches. This information is also present at the Readout connector, (J301) and the Program and Control connector (J204) at the rear of the instrument.

READY Indicator Lamp — Lights when the instrument has completed a count and is ready to accept a new program. The light extinguishes during measurement time.

EXT HOLD Indicator Lamp — Lights when an external recorder is recording the last measurement taken by the Type 230, and is holding. No change in display will be made until the external recorder has completed its cycle. The Type 230 may make the next measurement during this period.

DISPLAY TIME — Varies the time from one readout display to the next. During this period the readout holds the last number counted, and no further count will be transferred into the storage register (readout) until the display period ends. Variable from 0.01 seconds to 15 seconds.

TRIGGERED MEASUREMENT Switch — Used only when externally programmed. Sets up instrument to require an external trigger to start a measurement when a new program is applied.

+, — and E Indicators (Left Nixie tube) — On a voltage measurement, this tube indicates the Polarity of voltage referenced from the 0% zone to the 100% zone.

On a time measurement, this tube normally indicates a + time; e.g., the time measurement start point occurs before the stop point. However, if the start point occurs later in time than the stop point a — will be indicated.

If an average measurement of eight sweeps is being made (MEASUREMENT AVERAGE switch set at 8) it is possible for the tube to indicate both + and —, indicating that the stop occurred both before (—) and after (+) the start or reference point.

	E (error) is indicated whenever the 3 is lighted in the thousands indicator (left hand number tube). This is only a warning that the thousands indicator readout may be in error. Since the largest number the thousands indicator will read out is 3, it is never certain whether the count is actually 3, or larger than 3. The readout on the three remaining number indicators is always valid.
NUMBER Indicators	These four indicator tubes are read directly.
Units of Measure Indicator	Indicates the unit of measure in ns, μs, ms, s, mV and V. This tube is turned off if the Type 568 plug-in unit's Time/Div or Volts/Div Variable controls are not in the Calibrated position unless the Type 230 MEASUREMENT MODE switch is at EXT PROG.
Decimal Point Indicators	The decimal point is placed in the proper position by the time-base or vertical amplifier plug-in units. When programming externally, interpolation is sometimes necessary.

FIRST TIME OPERATION

The following procedure illustrates the use of the front-panel controls in the various measurement modes to familiarize the operator with the instrument. It is recommended that the operator follow this procedure completely for the first time operation. Since external programming is very close to duplicating front-panel operation, it will not be demonstrated here. Section 3 of this manual describes the methods of external programming.

In addition to the Type 230, the following equipment will be required for this operation.

a. Tektronix Type 568 Oscilloscope with two sampling plug-in units installed (Tektronix Type 3S3 and 3T4 recommended).

b. Fast rise pulse generator, such as a Tektronix Type 111.

c. Various cables and attenuators.

Procedure

1. Connect the 012-0119-01 cable between J101 of the Type 230 and J101 of the Type 568.

2. Connect the Pulse Output connector of the Type 111 to the Type 3S3 Probe A input connector through a GR 50 Ω 2× attenuator, a GR 50 Ω 10× attenuator, a GR to P6038 Probe adapter, and a P6038 Probe.

3. Connect the Pretrigger Output of the Type 111 to the Trigger - External Input of the Type 3T4 through a 10× attenuator and a 50 Ω cable.

4. Connect a 5 ns length of 50 Ω cable to the Charge Line connector of the Type 111.

5. Connect the Type 230, the Type 568, and the Type 111 to a power source that meets the voltage and frequency requirements of the instruments. Turn on all power switches.

6. While the instruments are warming up, set the front-panel controls as follows:

Type 230

MEASUREMENT MODE	A-VOLTS
CRT INTENSIFICATION	
TIME MEASUREMENT	OFF
REF ZONES	OFF
MEASUREMENT AVERAGING	1
CH A REFERENCE ZONES	
POSITION, 0%	White dot at top center
POSITION, 100%	White dot at top center
0% LEVEL - WIDTH	NEG PEAK 2 cm
100% LEVEL - WIDTH	NEG PEAK 2 cm
CH B REFERENCE ZONES	
POSITION, 0%	White dot at top center
POSITION, 100%	White dot at top center
0% LEVEL - WIDTH	NEG PEAK 2 cm
100% LEVEL - WIDTH	NEG PEAK 2 cm
TIME MEASUREMENT START POINT	
CHANNEL	A
LEVEL	% BETWEEN ZONES
Offset Dials	0 and 0
SLOPE	+ and 1st
TIME MEASUREMENT STOP POINT	
CHANNEL	A
LEVEL	% BETWEEN ZONES
Offset Dials	0 and 0
SLOPE	+ and 1st
LOWER LIMIT	+0000
UPPER LIMIT	+0000
TRIGGERED MEASUREMENT	OFF
DISPLAY TIME	Midrange

Type 568 Vertical Unit

Mode	Channel A
mV/Div	100
Variable	Calibrated
Position	Centered
Low Noise - Fast RT	Fast RT
DC Offset	Midrange
Smoothing	Counterclockwise

Type 568 Time Base Unit

Sweep Rate	5 nSEC
Variable	Calibrated
Delay	1.00
Sweep Mode	Normal
Trigger Level	Fully Clockwise

Triggering	+ External
Recovery Time	As desired
Samples/Sweep	×1 (1000)
Position	Centered

Type 568

Intensity	Normal or lower
Focus	As desired
Scale Illumination	As desired
Calibrator	Off

Type 111

Pulse Generator	
Repetition Rate	Maximum
Polarity	+
Range	10 KC
Trigger To Pulse Time Difference	
Variable	Max
Fixed Increment	0

7. Adjust the Type 3T4 Trigger Level control for a stable display. Using the Type 3T4 position control, position the trace to start at the left side of the graticule. Position the trace at the center horizontal graticule line with the Type 3S3 A Position control.

8. Set the CRT INTENSIFICATION-REF ZONES switch to 0%. Note that the zone is intensified on the CRT at the start of the trace and is 2 cm wide. Set the Ch A 0% LEVEL-WIDTH switch to NEG PEAK-4 cm; note that the 0% zone width is now four centimeters. Set the Ch A 0% LEVEL-WIDTH switch to 10 cm and again note the change in the 0% zone width. Reset the switch to AVERAGE .3 cm.

9. Turn the Ch A 0% POSITION control clockwise one position at a time. Note that the 0% zone steps across the CRT 0.5 centimeters for each position of the 0% POSITION control.

10. Set the CRT INTENSIFICATION-REF ZONES switch to 100%. Note that only the 100% zone is intensified and is 2 centimeters wide. Manipulate the Ch A 100% LEVEL-WIDTH switch and the Ch A 100% POSITION control as described in Steps 8 and 9 for the 0% zone, and note that they perform the same functions as the 0% zone controls. Reset the Ch A 100% LEVEL-WIDTH switch to AVERAGE .3 cm.

11. Set the CRT INTENSIFICATION-REF ZONES switch to BOTH. Turn the Ch A 0% and 100% POSITION controls. Note that both the 0% and 100% zones are now intensified.

12. Change the Type 3T4 Time/Div switch to 1 nSEC. Turn the Type 111 Trigger to Pulse Time Difference - Variable control until the pulse leading edge is centered on the CRT screen. Adjust the Type 3S3 mV/Div switch to give about 4 or 5 cm of vertical deflection.

13. Using the Ch A 0% and 100 POSITION controls, position the 0% zone on the baseline ½ cm from the pulse leading edge and the 100% zone on the most positive point on the pulse. Note that the readout on the Type 230 agrees with the CRT display amplitude. Set the Ch A 0% and 100% LEVEL-WIDTH switches to 2 cm and note that the readout increases slightly. The voltage measurement is referenced to the average voltage level within the zones when the LEVEL-WIDTH switches are set at AVERAGE, and to the most negative peak of the 0% zone and the most positive peak of the 100% zone when the respective LEVEL-WIDTH switches are set at either 2 cm, 4 cm, or 10 cm widths.

14. Turn the time-base Delay control slowly clockwise. Notice that the Type 230 readout does not change as long as the 0% zone remains on the baseline and the 100% zone remains on the pulse top. Re-position the display with the Delay control so the 0% zone is on the pulse top and the 100% zone is on the baseline. Note that the polarity readout changes from + to —.

15. Position the display so the 0% zone is again on the baseline and the 100% zone on the most positive point of the pulse. Set the MEASUREMENT AVERAGING switch to 8 and note the average value of the readout. Set the UPPER LIMIT switches to read one count greater than the average value of the readout. Set the LOWER LIMIT switches to read one count less than the average value of the readout. Turn the DISPLAY TIME control counterclockwise to speed up the measurement cycle. Return the MEASUREMENT AVERAGING switch to 1 and watch the three Limit lamps. Whenever the readout exceeds the average value, the ABOVE UPPER LIMIT lamp lights. If the readout equals the average value, the WITHIN LIMITS lamp lights, and if the readout is less than the average value, the BELOW LOWER LIMIT lamp lights.

16. Turn the vertical plug-in unit mV/Div variable control out of the calibrated (detent) position. Note that the readout is uncalibrated, the decimal point has moved and the "units of measure" indicator lamp is extinguished. The "number" indicator tubes read out the measurement, but not in V or mV. Return the mV/Div variable control to the calibrated position.

17. Reset the following Type 230 controls:

MEASUREMENT MODE	TIME
CHANNEL A REF ZONES	
0% LEVEL	AVERAGE
100% LEVEL	AVERAGE
TIME MEASUREMENT START POINT	
LEVEL	% BETWEEN ZONES
Offset Switches	5-0
SLOPE	+, 1ST
TIME MEASUREMENT STOP POINT	
LEVEL	% BETWEEN ZONES
Offset Switches	5-0
SLOPE	—, 1ST

18. Using the Ch A 0% POSITION control, position the 0% zone on the baseline preceding the pulse. Using the Ch A 100% POSITION control, position the 100% zone on the pulse top.

19. Set the CRT INTENSIFICATION-TIME MEASUREMENT switch to ON. There is now a third intensified zone on the waveform. This intensified pulse portion of the trace is the time measurement zone, which extends from the leading edge 50% point to the trailing edge 50% point. The time measurement is read directly from the Type 230 readout. This is standard pulse-width measurement.

20. Reset the following Type 230 controls:

CRT INTENSIFICATION
- TIME MEASUREMENT — OFF

TIME MEASUREMENT START POINT
- Offset switches — 1-0
- SLOPE — +, 1 ST

TIME MEASUREMENT STOP POINT
- Offset switches — 9-0
- SLOPE — +, 1 ST

21. Using the Ch A 0% POSITION control, position the 0% zone on the flat portion of the display just before the positive-going leading edge of the pulse.

22. Using the ChA 100% POSITION control, position the 100% zone on the peak of the pulse.

23. Set the CRT INTENSIFICATION-TIME MEASUREMENT switch to ON. Notice that the type of measurement being made is a risetime measurement, from the 10% point to the 90% point of the positive slope as shown by the measurement zone.

24. Set the CRT INTENSIFICATION-TIME MEASUREMENT switch to OFF. Position the 0% zone at the peak of the pulse with the Ch A 0% POSITION control. Using the CH A 100% POSITION control, position the 100% zone on the flat portion of the display just after the negative-going edge of the pulse. Set both SLOPE switches to —.

25. Set the CRT INTENSIFICATION-TIME MEASUREMENT switch to ON. The measurement being made is now a fall-time measurement between the 90% point and the 10% point of the first negative slope. The measurement zone is indicated by the intensification zone between the 0% zone and the 100% zone.

26. Reset the following Type 230 controls:

CRT INTENSIFICATION
- TIME MEASUREMENT — OFF
- REF ZONES — 0%

TIME MEASUREMENT START POINT
- LEVEL — mm ABOVE 0% ZONE
- Offset switches — 0-5
- SLOPE — +, 1 ST

TIME MEASUREMENT STOP POINT
- LEVEL — mm ABOVE 0% ZONE
- Offset switches — 3-0
- SLOPE — +, 1 ST

27. Position the 0% zone on the baseline ½ cm to the left of the start of the pulse rise.

28. Set the CRT INTENSIFICATION-TIME MEASUREMENT switch to ON. The intensified measurement zone is from 5 mm above the 0% zone reference level to 30 mm above this level. The readout corresponds to the time interval between the start and the stop of the intensified zone.

29. The mm BELOW 100% ZONE position of the TIME MEASUREMENT START POINT and TIME MEASUREMENT STOP POINT-LEVEL switches works in the same manner as the mm ABOVE 0% ZONE position, with the measurement being referenced to a selected point below the 100% ZONE.

30. Turn the time-base Time/Div variable control out of the calibrated (detent) position. The readout is uncalibrated, the decimal point has moved and the "unit of measure" indicator tube is extinguished. The "number" indicator tubes read out the measurement, but not in mS, μS, etc. Return the Time/Div variable control to the calibrated position.

31. Vary the DISPLAY TIME control from the midrange position and notice the change in length of time the readout is displayed. This can be noticed most easily by observing either the READY lamp or the time measurement intensified zone on the CRT. Both of these are extinguished during measurement time, which occurs at the end of each display time period.

SECTION 3
TYPE 230 PROGRAMMING INSTRUCTIONS

General Information

The 230 has a total of 105 programming inputs available at the external connections located at the rear of the instrument. There are also 52 readout lines available. The characteristics of the external program input lines are as follows:

TRUE

For a TRUE indication, the program inputs are particularly adapted to saturated transistor collector inputs, and will easily function with ground closures by relays. To ensure that no feedback or "sneak path" occurs, a series diode should be inserted at each program input in use. The ideal logic level which constitutes a logical ONE is ground; the most positive level which constitutes a logical ONE is +2 volts.

FALSE

To program a ZERO (FALSE), any program line may be left open. If a line is held at a specific level when programmed FALSE, the holding level must be more positive than +6 volts to constitute a logical ZERO. Pullup on any program line should not exceed +12 volts. A line providing +12 volts at 350 mA is available at J204 pin 23.

Jacks J201, J202, and J203 are located on the Type 230 rear panel for external program inputs. Jack J204 contains program inputs, Type 230 power supply voltages for external use, and controlling outputs from the Type 230. Jack J301 provides measurement results or readout to external devices. Jack J101 provides the necessary interconnections from the Type 230 to the Type 568 and vice-versa. (For physical location of the jacks see Fig. 3-1).

Program Common Lines

Pins 17, 18, 35, and 36 of J201, J202, and J203 are program common outputs. J204 pin 17 is also a program common output. All of the 13 program common lines join at the Type 230 front panel MEASUREMENT MODE switch. Only when the MEASUREMENT MODE switch is in the EXT PROG position will the program common lines enable the external program inputs.

Effective with serial number B13050 and above, all Type 230/R230 instruments are equipped with keyed rear panel connectors. This change is to prevent damage to the instrument. The cables used on instruments serial numbered below B130540 will not fit modified instruments, but keyed cables will fit unmodified instruments. Keyed cables for modified Type 230/R230 are available under the following Tektronix part numbers:

Cables for J201-J202-J203-J301	012-0131-00
Cable for J204	012-0131-01
Cable for J101	012-0119-01

EXTERNAL PROGRAM LINES

Table 3-1 lists all of the 105 external program inputs. Since some of the lines provide a program function in either TRUE or FALSE condition, each line will be examined in each condition. Special notations are provided where combinations of lines program an additional function.

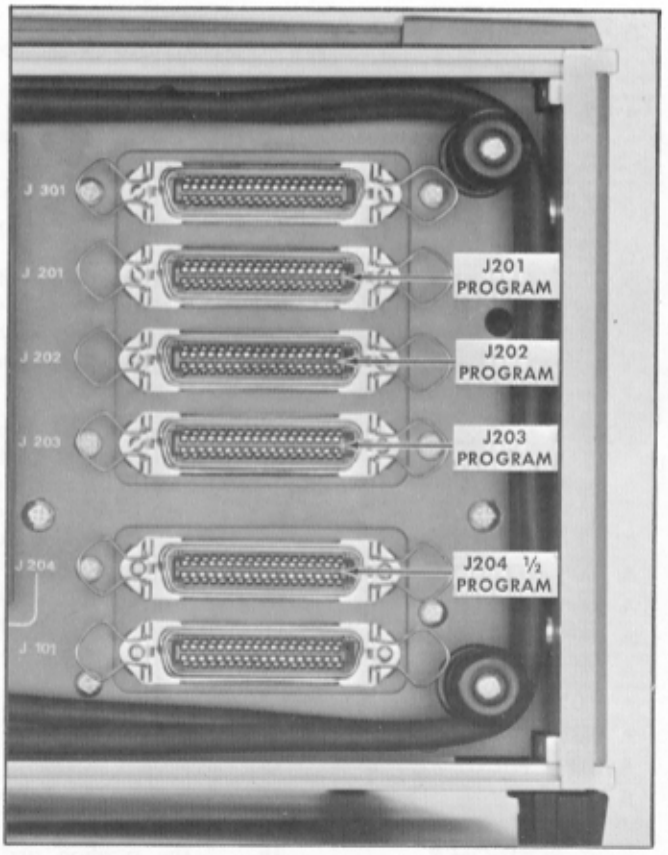


Fig. 3-1. Type 230 external connectors.

TABLE 3-1
External Program Inputs

TITLE	PIN NO. (J201)	TRUE	FALSE
A 0% POSITION 8	1	Provides 8 cm position command to the A 0% Zone Generator.	No program
A 0% POSITION 4	2	Provides 4 cm position command to the A 0% Zone Generator.	No program

TABLE 3-1 *(cont)*

TITLE	PIN NO. (J201)	TRUE	FALSE
A 0% POSITION 2	3	Provides 2 cm position command to the A 0% Zone Generator.	No program
A 0% POSITION 1	4	Provides 1 cm position command to the A 0% Zone Generator.	No program
A 0% POSITION .5	5	Provides .5 cm position command to the A 0% Zone Generator.	No program

NOTE

Although only 9.5 cm of zone position may be programmed from the front panel, externally the zone can be programmed to 15.5 cm. Any programmed position of 12 (8 cm +4 cm) through 15.5 cm (8 cm + 4 cm + 2 cm + 1 cm + .5 cm) will Cause the previous memory information to be retained subsequent measurement. If the zone position is programmed past the sweep end and before position 12, measurement cycles will no longer occur since the memories cannot assume a charge.

A 0% WIDTH 4 cm	6	Shifts the A 0% Memory from AVERAGE to PEAK; zone width changes to 4 cm.	Programs the A 0% memory to AVERAGE; zone width is .3 cm.
A 0% WIDTH 2 cm	7	Shifts the A 0% Memory from AVERAGE to PEAK; zone width changes to 2 cm.	Programs the A 0% memory to AVERAGE; zone width is .3 cm.

NOTE

If both 4 cm and 2 cm are programmed TRUE, the remainder of the sweep intensifies from the start position of the zone. If either one of the two are programmed TRUE, the sweep is intensified from the programmed zone position for the programmed width or to the end of the sweep, whichever occurs first.

VOLTS	8	Programs the Type 230 to a voltage measurement mode, disables the horizontal decimals and units plug-in common lines; enables the vertical decimals and units plug-in common lines.	Programs the Type 230 to a time measurement mode; enables the horizontal decimals and units plug-in common lines; disables the vertical decimals and units plug-in lines.
A 100% POSITION 8	9	The position and width programs for the A 100% zone perform the same function as the position and width program lines for the A 0% zone.	
A 100% POSITION 4	10		
A 100% POSITION 2	11		
A 100% POSITION 1	12		
A 100% POSITION .5	13		
A 100% WIDTH 4 cm	14		
A 100% WIDTH 2 cm	15		
A CHOP	16	Enables A chopper drive for external chopper synchronization.	
B 0% POSITION 8	19	The position and width programs for the B 0% and B 100% zones perform the same function as the position and width program lines for the A 0% and A 100% zones.	
B 0% POSITION 4	20		
B 0% POSITION 2	21		
B 0% POSITION 1	22		
B 0% POSITION .5	23		
B 0% WIDTH 4 cm	24		
B 0% WIDTH 2 cm	25		
MEASURE AVERAGE	26	Programs a readout equal to the average value of eight consecutive measurements. Used for noisy signals to reduce error.	Programs the readout to indicate the value of one measurement.

TABLE 3-1 *(cont)*

TITLE	PIN NO. (J201)	TRUE	FALSE
B 100% POSITION 8	27	See B 0% POSITION for B 100% position and width characteristics.	
B 100% POSITION 4	28		
B 100% POSITION 2	29		
B 100% POSITION 1	30		
B 100% POSITION .5	31		
B 100% WIDTH 4 cm	32		
B 100% WIDTH 2 cm	33		
B CHOP	34	Enables B chopper drive for external chopper synchronization.	

TITLE	PIN NO. (J202)	TRUE	FALSE
(START) B CHANNEL	1	Start point on B channel.	Start point on A channel.
(START) HORIZONTAL mm	2	Start Comparator fires at OFFSET mm from sweep start. (Independent of signal).	Start comparator fires as a function of the signal.
(START) % BETWEEN	3	Start Comparator fires at the signal level expressed as percentage.	Start comparator fires on the signal level in offset mm vertically displaced from the memory.
(START) mm BELOW	4	Start Comparator fires at the amount of programmed start offset below the selected reference zone.	Start Comparator fires at the amount of programmed start offset above the selected reference zone.
(START) OFFSET 100	5	References the Start Comparator offset from the 100% zone.	References the Start Comparator offset from the 0% zone.
(START) MINUS SLOPE	6	Start Comparator fires on a minus slope of the analog display.	Start Comparator fires on a plus slope of the analog display.
(START) SECOND SLOPE	7	Start Comparator fires on a 2nd slope of the analog display (either plus or minus 2nd slope as programmed).	Start Comparator fires on a 1st slope of the analog display (either plus or minus 1st slope as programmed).
COUNTER RESET INHIBIT	8	Programs the Type 230 counter to accumulate a series of measurements without resetting or clearing the previous measurement information. Additive readout will still occur at the end of each measurement.	Normal operation
(START) OFFSET 80	9	Start Comparator fires at one of three references: a. Signal—offset mm or offset % may be selected. b. Voltmeter ramp—offset mm or offset % may be selected. c. Sweep ramp (Horizontal mm)—only offset mm may be used.	No program

NOTE

OFFSET program lines are additive. It is possible to program 159 increments (% or mm) through the external programming inputs. Since the Type 230 is not designed to measure out-of-graticule information, no more than a maximum of 80 mm would be useful. The offset percentage above 100% is useful for the measurement of overshoot. Although the sum of the offset lines is greater than 159, the first decade of the offset is constructed to provide no more than nine.

(START) OFFSET 40	10	Programs 40% or 40 mm	No program
(START) OFFSET 20	11	Programs 20% or 20 mm	No program
(START) OFFSET 10	12	Programs 10% or 10 mm	No program

TABLE 3-1 *(cont)*

TITLE	PIN NO. (J202)	TRUE	FALSE
(START) OFFSET 8	13	Programs 8% or 8 mm	No program
(START) OFFSET 4	14	Programs 4% or 4 mm	No program
(START) OFFSET 2	15	Programs 2% or 2 mm	No program
(START) OFFSET 1	16	Programs 1% or 1 mm	No program
(STOP) B CHANNEL	19	Pins 19 through 25 perform the same programming functions that pins 1 through 7 perform, with the exception that pins 19 through 25 control the Stop Comparator.	
(STOP) HORIZONTAL mm	20		
(STOP) % BETWEEN	21		
(STOP) mm BELOW	22		
(STOP) OFFSET 100	23		
(STOP) MINUS SLOPE	24		
(STOP) SECOND SLOPE	25		
EXTERNAL SCALE	26	Disables internal scaling (See J204)	Enables internal scaling

NOTE

If EXT SCALE is TRUE, the front panel readout will not indicate the correct scaling for the measurement. Programming of the decimals and units externally is required.

(STOP) OFFSET 80	27	Pins 27 through 34 program functions identical to those of pins 9 through 16, with the exception that pins 27 through 34 program the Stop Comparator.
(STOP) OFFSET 40	28	
(STOP) OFFSET 20	29	
(STOP) OFFSET 10	30	
(STOP) OFFSET 8	31	
(STOP) OFFSET 4	32	
(STOP) OFFSET 2	33	
(STOP) OFFSET 1	34	

TITLE	PIN NO. (J203)	TRUE	FALSE
EXTERNAL HORIZONTAL ÷ 2	1	Divides readout by two (See J204).	Programs normal clock rate.
UPPER MINUS	2	Programs the upper limit level to be a negative number.	Programs the upper limit level to be a positive number.
UPPER LIMIT 2000	3	Programs the upper limit level to an algebraic value of 2000.	No program
UPPER LIMIT 1000	4	Programs 1000	No program
UPPER LIMIT 800	5	Programs 800	No program
UPPER LIMIT 400	6	Programs 400	No program
UPPER LIMIT 200	7	Programs 200	No program
UPPER LIMIT 100	8	Programs 100	No program
UPPER LIMIT 80	9	Programs 80	No program
UPPER LIMIT 40	10	Programs 40	No program
UPPER LIMIT 20	11	Programs 20	No program
UPPER LIMIT 10	12	Programs 10	No program
UPPER LIMIT 8	13	Programs 8	No program
UPPER LIMIT 4	14	Programs 4	No program
UPPER LIMIT 2	15	Programs 2	No program
UPPER LIMIT 1	16	Programs 1	No program

TABLE 3-1 *(cont)*

TITLE	PIN NO. (J203)	TRUE	FALSE

NOTE

The limit level inputs are additive so that a limit of + or — 3999 may be programmed. Care must be taken to avoid programming any decade of either the upper or lower limits to a value greater than 9. For example, the combination of 800 plus 100 is permissible, but the combination of 800 plus 200, 800 plus 400, or any combination totalling over 900 will result in an erroneous limit readout.

EXTERNAL HORIZONTAL ÷ 5	19	Multiplies readout by two; shifts readout decimal to left one place. (See J204).	Programs normal count and decimal position.
LOWER MINUS	20	Programs the lower limit level to be a negative number.	Programs a positive number.
LOWER LIMIT 2000	21	Programs the lower limit level to lower an algebraic value of 2000.	No program
LOWER LIMIT 1000	22	Programs 1000	No program
LOWER LIMIT 800	23	Programs 800	No program
LOWER LIMIT 400	24	Programs 400	No program
LOWER LIMIT 200	25	Programs 200	No program
LOWER LIMIT 100	26	Programs 100	No program
LOWER LIMIT 80	27	Programs 80	No program
LOWER LIMIT 40	28	Programs 40	No program
LOWER LIMIT 20	29	Programs 20	No program
LOWER LIMIT 10	30	Programs 10	No program
LOWER LIMIT 8	31	Programs 8	No program
LOWER LIMIT 4	32	Programs 4	No program
LOWER LIMIT 2	33	Programs 2	No program
LOWER LIMIT 1	34	Programs 1	No program

NOTE

The limit level circuits are constructed to be sensitive to polarity differences as well as differences in absolute value. This means that it is possible and sometimes desirable to program a +0000 or a —0000. It should be noted that the circuit views a + 0000 as being greater in algebraic value than a — 0000. Any count that occurs without a polarity sign is treated as plus, and if the Type 230 is in a cumulative measurement mode (average-of-eight; counter reset inhibit) the counter adds all numbers arithmetically regardless of polarity. When this mode is present, enough jitter may be present to cause the equipment to indicate a readout of ±. The limit circuit sees ± as —, so the entire readout will be meaningless for that measurement.

TITLE	PIN NO. (J204)	TRUE	FALSE
DECIMAL 2	1	Programs the 2nd readout decimal from the left to light.	When DECIMAL 2, DECIMAL 3, and DECIMAL 4 are all FALSE, the fifth decimal light from the left will be programmed ON (except as noted below).
DECIMAL 3	2	Programs the 3rd readout decimal from the left to light.	
DECIMAL 4	3	Programs the 4th readout decimal from the left to light.	

TABLE 3-1 *(cont)*

TITLE	PIN NO. (J204)	TRUE	FALSE
		NOTE Scaling the readout of the Type 230 by external programming is done by programming the decimal and units nixies with the following exceptions, variations, or conditions: When EXT SCALE is FALSE, the vertical and horizontal plug-ins in the Type 568 control the scaling of the readout, but do not forbid or inhibit additional scaling from the external program inputs. In most cases additional scaling would not be desired, but if attenuators were placed between the vertical input and the signal source the external scaling could be used to compensate the readout. When EXT SCALE is TRUE, internal scaling is disabled. Without some external scaling provided, the readout will indicate an accumulation of measurement without any decimals or units to indicate magnitude of measurement. EXT ÷ 5 is used to multiply the readout by two. This enables the programmer to compensate for a change in a plug-in attenuator or sweep range. EXT ÷ 5 also shifts the decimal one place to the left when TRUE. In order to compensate for this characteristic, programming the decimal point position should be adjusted if necessary to provide the correct decimal readout. EXT ÷ 2 divides the readout by two, so scaling should also compensate for the division if needed. The decimal scaling of the Type 230 has an inhibiting function so that no two decimals may appear. The units scaling has no inhibiting function, and it is possible for all units to be energized at once. The operator should note this when programming the instrument and avoid programming multiple unit lines unless so specified by the program.	
NIXIE 'v'	4	Programs front panel readout nixie 'v' ON	No program
NIXIE 's'	5	Programs front panel readout nixie 's' ON	No program
NIXIE 'm'	6	Programs front panel readout nixie 'm' ON	No program
NIXIE 'μ'	7	Programs front panel readout nixie 'μ' ON	No program
NIXIE 'N'	8	Programs front panel readout nixie 'N' ON	No program
		NOTE If either units or decimals are to be programmed externally, EXT SCALE should be programmed TRUE to prevent multiple display of units or decimals.	
HIGH SPEED PROGRAM	9	Reduces time between measurements.	Normal measurement speed.
A CHOP[1]	15	Enables A chopper drive for external chopper synchronization.	Disables A chopper drive.
B CHOP[1]	16	Enables B chopper drive for external chopper synchronization.	Disables B chopper drive.

The remainder of J204 is composed of external control outputs. Jacks J101, J301, and the remainder of J204 will be discussed after the programming instructions.

FIRST-TIME PROGRAMMING

Since the majority of the external functions are controllable from the front panel of the Type 230, an easy way to set up the first program is to "front-panel program" the instrument to perform a desired measurement. After determining that the measurement succeeds on a front panel basis, the operator can then proceed with externally programming the Type 230. Table 3-2 lists all front panel functions and their external program counterparts. This will allow the operator to cross-reference a front panel setup to an external program.

TABLE 3-2

Program Line Equivalents of Front Panel Settings

FRONT PANEL	CORRESPONDING PROGRAM LINE
MEASUREMENT AVERAGING 1:8	MEASURE AVERAGE: J201-26
CRT INTENSIFICATION	No External Counterparts

[1]**This line used only on instruments SN 360 and up.**

TABLE 3-2 *(cont)*

FRONT PANEL	CORRESPONDING PROGRAM LINE
MEASUREMENT MODE:	
TIME	VOLTS FALSE: J201-8
A VOLTS	VOLTS: J201-8. B CHANNEL FALSE: J202-1
B VOLTS	VOLTS: J201-8. B CHANNEL: J202-1
EXT PROG	No Counterpart

NOTE

Offset is used in External Program Volts, but not in Front Panel Volts.

DISPLAY TIME	No Counterpart
TRIGGERED MEASUREMENT	No Counterpart
CH A REFERENCE ZONES	
POSITION 0%	A 0% Position 8, 4, 2, 1, .5: J201-1, 2, 3, 4, 5
POSITION 100%	A 100% Position 8, 4, 2, 1,.5: J201-9, 10, 11, 12, 13
0% LEVEL	
AVERAGE .3 cm	No Program: J201-6, 7 FALSE
NEG PEAK 2 cm	A 0% Width 2 cm: J201-7
NEG PEAK 4 cm	A 0% Width 4 cm: J201-6
NEG PEAK 10 cm	A 0% Width 2 cm, 4 cm: J201-7, 6
100% LEVEL	
AVERAGE .3 cm	No Program: J201-14, 15 FALSE
POS PEAK 2 cm	A 100% Width 2 cm: J201-15
POS PEAK 4 cm	A 100% Width 4 cm: J201-14
POS PEAK 10 cm	A 100% Width 2 cm, 4 cm: J201-15, 14
CH B REFERENCE ZONES	
POSITION 0%	B 0% Position 8, 4, 2, 1, .5: J201-19, 20, 21, 22, 23
POSITION 100%	B 100% Position 8, 4, 2, 1, .5: J201-27, 28, 29, 30, 31
0% LEVEL	
AVERAGE .3 cm	No Program: J201-24, 25 FALSE
NEG PEAK 2 cm	B 0% Width 2 cm: J201-25
NEG PEAK 4 cm	B 0% Width 4 cm: J201-24
NEG PEAK 10 cm	B 0% Width 2 cm, 4 cm: J201-25, 24
100% LEVEL	
AVERAGE .3 cm	No Program: J201-32, 33 FALSE
POS PEAK 2 cm	B 100% Width 2 cm: J201-33
POS PEAK 4 cm	B 100% Width 4 cm: J201-32
POS PEAK 10 cm	B 100% Width 2 cm, 4 cm: J201-33, 32
TIME MEASUREMENT START POINT	
CHANNEL	
A	B CHANNEL FALSE: J202-1
B	B CHANNEL: J202-1
LEVEL	
% BETWEEN ZONES	% BETWEEN: J202-3
mm ABOVE 0% ZONE	mm BELOW FALSE: J202-4
mm BELOW 100% ZONE	mm BELOW: J202-4 (OFFSET from 100% zone)
HORIZ mm FROM SWP START	HORIZ mm: J202-2 (normally first plus slope)
OFFSET DIALS (0-99)	OFFSET 80 through 1: J202-9 through 16
SLOPE +	MINUS SLOPE FALSE: J202-6
—	MINUS SLOPE: J202-6
1st	2nd SLOPE FALSE: J202-7
2nd	2nd SLOPE: J202-7

TABLE 3-2 *(cont)*

FRONT PANEL	CORRESPONDING PROGRAM LINE
TIME MEASUREMENT STOP POINT	
CHANNEL	
A	B CHANNEL FALSE: J202-19
B	B CHANNEL: J202-19
LEVEL	
% BETWEEN ZONES	% BETWEEN: J202-21
mm ABOVE 0% ZONE	mm BELOW FALSE: J202-22
mm BELOW 100% ZONE	mm BELOW: J202-22
HORIZ mm FROM SWP START	HORIZ mm: J202-20
OFFSET DIALS (0-99)	OFFSET 80 through 1: J202-27 through 34
SLOPE +	MINUS SLOPE FALSE: J202-24
—	MINUS SLOPE: J202-24
1st	2nd SLOPE FALSE: J202-25
2nd	2nd SLOPE: J202-25
UPPER LIMIT DIALS	UPPER MINUS and UPPER 2000 through 1: J203-2 through 16
LOWER LIMIT DIALS	LOWER MINUS and LOWER 2000 through 1: J203-20 through 34

NOTE

Whenever the Type 230 is operated with the MEASUREMENT MODE switch in the EXT PROG position, it is advisable to position the TRIGGERED MEASUREMENT switch ON. This will help in preventing lockup of the measurement cycle. When the TRIGGERED MEASUREMENT switch is ON, a plus or minus trigger must be applied through rear-panel jack J204 to initiate a measurement. This trigger must be synchronized with the programming device so that a change in program does not occur until after PRINT COMMAND from the Type 230 moves high and returns low, signifying the end of measurement and readiness for a new program.

SAMPLE PROGRAMS

The following pages show a group of example programs to aid the operator in first-time programming of the Type 230. All of the program input lines have been conveniently arranged in an 8-4-2-1 order. Each four-bit (line) segment is called a character. Since there are 105 bits (lines) programmable, there are 27 characters in the program chart below (Notice that the 27th character has only one bit; bit eight). The entire group of characters is called a word. In addition to the three program examples mentioned above, a blank program chart is included for convenient reproduction (see Fig. 3-7). The blank program is arranged in the same fashion as the example program charts. The character number is at the far left of the chart. Moving right, the eight, four, two, and one bits are tabulated. The two columns to the right of the bit spaces are for the programs, two to each worksheet. At the far right the program input lines appear in the same order as the bits. For example, if the operator did not wish to program the other three bits in character 6 TRUE, he would write 0001 in the program space adjacent to Character 6. Moving to the right at the Character 6 level, the program input line corresponding to Gharacter 6, Bit 1 is Jack J201, pin 26.

Example Program One (See Fig. 3-4)

The first example deals with a voltage measurement of channel A information. Refer to Fig. 3-2 for a pictorial representation of the information to be measured. The Type 568 vertical plug-in has been set to display about 6 divisions of signal vertical deflection on channel A only. The Type 568 horizontal plug-in has been triggered on the plus slope of the signal, and the TIME/DIV has been set to cause the display as shown in Fig. 3-2. Since the display rises from 0% to 100% amplitude from the fifth to the seventh division, the program input may be only concerned with the 5th to 7th division area. The program for this measurement is as follows: (See example program chart No. 1, Fig. 3-3).

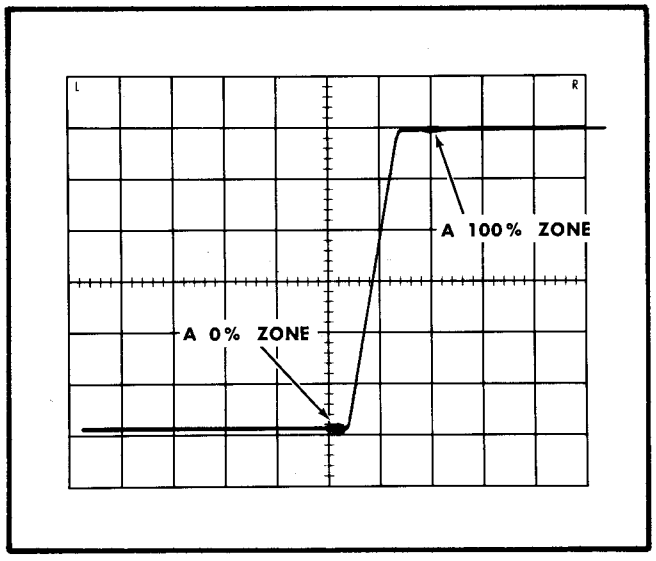


Fig. 3-2. Information to be measured in Example Program 1.

Character 1:	0101	This places the A 0% zone and the start of measurement at the fifth graticule division.
Character 2:	0001	Since we wish the memories to charge to average, bits 4 and 2 are FALSE. A voltage measurement is desired, so bit 1 is TRUE.

CHARACTER	8	4	2	1	PROGRAM 1	PROGRAM 2	J201 PINS 8	4	2	1
1	A 0% POS. 8	4	2	1	0101	0001	1	2	3	4
2	A 0% POS. .5	A 0% Wid. 4 cm	2 cm	VOLTS	0001	0000	5	6	7	8
3	A 100% POS. 8	4	2	1	0111	0101	9	10	11	12
4	A 100% POS. .5	A 100% Wid. 4 cm	2 cm	A CHOP	0000	0000	13	14	15	16
5	B 0% POS. 8	4	2	1	0000	0000	19	20	21	22
6	B 0% POS. .5	B 0% Wid. 4 cm	2 cm	MEASURE AVE.	0000	0000	23	24	25	26
7	B 100% POS. 8	4	2	1	0000	0000	27	28	29	30
8	B 100% POS. .5	B 100% Wid. 4 cm	2 cm	B CHOP	0000	0000	31	32	33	34
							J202			
9	(START) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW	0000	0010	1	2	3	4
10	(START) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	COUNTER RESET INHIBIT	0000	0000	5	6	7	8
11	(START) OFFSET 80	40	20	10	0000	0001	9	10	11	12
12	OFFSET 8	4	2	1	0000	0000	13	14	15	16
13	(STOP) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW	0000	1001	19	20	21	22
14	(STOP) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	EXT SCALE	1000	1100	23	24	25	26
15	(STOP) OFFSET 80	40	20	10	0000	0001	27	28	29	30
16	(STOP) OFFSET 8	4	2	1	0000	0101	31	32	33	34
							J203			
17	EXT HORIZ ÷ 2	UPPER MINUS	UPPER LIMIT 2000	1000	0000	0000	1	2	3	4
18	800	400	200	100	0110	0011	5	6	7	8
19	80	40	20	10	0011	1000	9	10	11	12
20	8	4	2	1	0000	0101	13	14	15	16
21	EXT HORIZ ÷ 5	LOWER MINUS	LOWER LIMIT 2000	1000	0000	0000	19	20	21	22
22	800	400	200	100	0101	0011	23	24	25	26
23	80	40	20	10	0111	0001	27	28	29	30
24	8	4	2	1	0000	0101	31	32	33	34
							J204			
25	PROG DEC 2	3	4	NIXIE 'V'	0000	0000	1	2	3	4
26	NIXIE S	NIXIE M	NIXIE 'μ'	NIXIE 'N'	0000	0000	5	6	7	8
27	HIGH SPEED PGM		A CHOP[2]	B CHOP[2]	0000	0000	9		15	16

NOTE: GROUND CLOSURE OF A PROGRAM LINE CONSTITUTES A LOGICAL ONE (TRUE); ANY OPEN LINE IS A LOGICAL ZERO (FALSE).

[2]Below SN 360 these bits are not used.

Fig. 3-3. Example Programs 1 and 2.

Character 3:	0111	Character 3, Bits 4, 2, and 1 position the A 100% Zone at the 7th display cm; the A 100% memory charges to the average value of the signal during the ZONE.
Character 4:	0000	No program desired.
Character 5:	0000	No Program.
Character 6:	0000	No program desired. (Bit 1, MEASURE AVERAGE is usually used for an unstable display. Since no problem exists, Bit 1 is left FALSE).
Character 7:	0000	No program. Characters 5 and 7 are programmed 0000 to allow the B memories to charge and discharge with each measurement cycle of the instrument. If more than ten centimeters of zone position is programmed, and a memory is not allowed to charge on a previous cycle, the measurement cycle may lock up.
Character 8:	0000	No program desired.
Character 9:	0000	Programming Bit 8 FALSE causes the Start Comparator to fire on the A channel information. The other three bits concern time measurement programming.
Character 10:	0000	No program desired.
Character 11:	0000	No program desired.
Character 12:	0000	No program desired.
Character 13:	0000	Programming Bit 8 FALSE causes the stop comparator to fire on the A channel information. The other three bits concern time measurement programming.
Character 14:	1000	Bit 8 is programmed TRUE to fire the stop Comparator at the offset % from the 100% zone. Bit 1 is programmed FALSE to enable plug-in commons and allow the plug-ins to control the readout decimals and units.
Character 15:	0000	No program desired.
Character 16:	0000	No program desired.
Character 17:	0000	Programming Bit 4 FALSE causes the upper limit level to be a positive number.
Character 18:	0110	Since the display is to read out approximately +06.00 V, assume that a tolerance of ±5% is imposed on the measurement. The sum of Character 18, Bits 4 and 2; Character 19, Bits 2 and 1 equals 0630. +0630 is the maximum value of measurement that may occur without an indication of above upper limit level.
Character 19:	0011	
Character 20:	0000	
Character 21:	0000	Programming Bit 4 FALSE causes the lower limit level to be a positive number.
Character 22:	0101	Note the explanation for Characters 18, 19, and 20. The desired measurement should not exceed 5% from + 06.00 V, so the lower limit level is programmed to + 0570.
Character 23:	0111	
Character 24:	0000	
Character 25:	0000	No program desired.
Character 26:	0000	No program desired.
Character 27:	0000	No program desired.

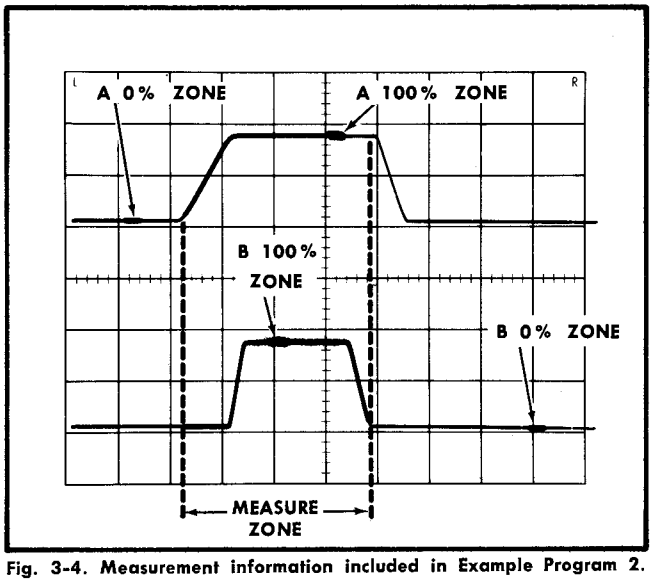


Fig. 3-4. Measurement information included in Example Program 2.

Example Program Two

The second example shows how to set up a time measurement program. In addition to this explanation, the second column of sample program chart No. 1 (Fig. 3-3) shows the program setup. Refer also to Fig. 3-4 for a photograph of the signal being measured. This program is a time measurement between two events; one on channel A, the other on channel B. The Type 568 vertical plug-in is set at A and B with the Type 568 display as shown in Fig. 3-4. The Type 568 horizontal plug-in is set for 100 dots per division to display the events shown in Fig. 3-4. The objective of this measurement is to measure the time difference between 10% up on the A channel event to 15 mm down from the top of the B channel event. In other words, we wish to measure from the start of the A channel event to the end of the B channel event. Note that the A channel event begins its rise at the 2nd centimeter of display, and begins to fall at about 6.5 cm of display. The B channel event begins its rise at the 3 cm point, and starts to fall at the 5 cm point. This information should be used for programming zone positioning. The program word by characters is as follows:

Character 1:	0001	Bit 1 is TRUE to place the A 0% zone at the first cm of display on the A trace.
Character 2:	0000	No program desired.
Character 3:	0101	Bits 4 and 1 are TRUE to place the A 100% zone at the fifth cm of display on the A trace.
Character 4:	0000	No program desired.
Character 5:	1001	Bits 8 and 1 position the B 0% zone at the ninth cm of display on the B trace.

Character 6:	0000	No program desired.
Character 7:	0100	Bit 4 positions the B 100% zone at the fourth cm of the B trace.
Character 8:	0000	No program desired.
Character 9:	0010	Bit 8 FALSE fires the start comparison on the A channel; Bit 2 TRUE places the comparison at a percentage of the position between zones as determined by OFFSET (characters 11 and 12).
Character 10:	0000	Bits 4 and 2 FALSE cause the start comparison point to occur on the first plus slope.
Character 11:	0001	Bit 1 TRUE causes the start comparison to occur at 10% above the 0% zone.
Character 12:	0000	No program desired.
Character 13:	1001	Bit 8 TRUE selects B channel for the stop comparison point, Bit 1 TRUE places the stop comparison point at Offset mm below the reference zone.
Character 14:	1100	Bit 8 TRUE selects the 100% zone as the stop offset reference; Bit 4 TRUE and Bit 2 FALSE selects the first minus slope for the stop comparison point.
Character 15:	0001	Character 15, Bit 1 and Character 16, Bits 4 and 1 TRUE make a sum of 15 mm offset which causes the stop comparison point to occur 15 mm down the first minus slope.
Character 16:	0101	
Character 17:	0000	Bit 4 FALSE causes a plus upper limit.
Character 18:	0011	Assuming a tolerance of plus or minus 10% for this measurement, the TRUE bits in characters 18, 19, and 20 sum up to an upper limit level of +0385, since the approximate length of the desired measurement is 350 microseconds (100 dots/cm, 3.5 cm, and therefore 350 dots).
Character 19:	1000	
Character 20:	0101	
Character 21:	0000	Bit 4 FALSE selects a positive lower limit level.
Character 22:	0011	The TRUE bits in Characters 22, 23, and 24 sum the lower limit level to +0315, which equals the desired measurement minus the 10% tolerance.
Character 23:	0001	
Character 24:	0101	
Character 25:	0000	No program desired for characters 25, 26 and 27 since external scaling is not used for this measurement. Although an equivalent-time sampling plug-in unit is being used for this measurement, no need for speedup of the sweep is indicated in this program.
Character 26:	0000	
Character 27:	0000	

Example Program Three

The third example program illustrates how a pair of consecutive measurements may be made to determine the exact time of a peak amplitude occurrence. Referring to Fig. 3-5, a pulse-type signal is shown with its peak occurring at about the fifth cm of display. The time (horizontal mm) from the sweep start to the 90% point on the rise of the signal is measured on the first program. The time from the sweep start to the 90% point on the fall of the signal is measured on the second program. By accumulating the count from both measurements and dividing them by two, the time position of the peak from the start of the sweep may be determined. The second measurement is pictured in Fig. 3-5b. The external program is shown in example program number three (Fig. 3-6). An explanation of the measurement programs by character follows:

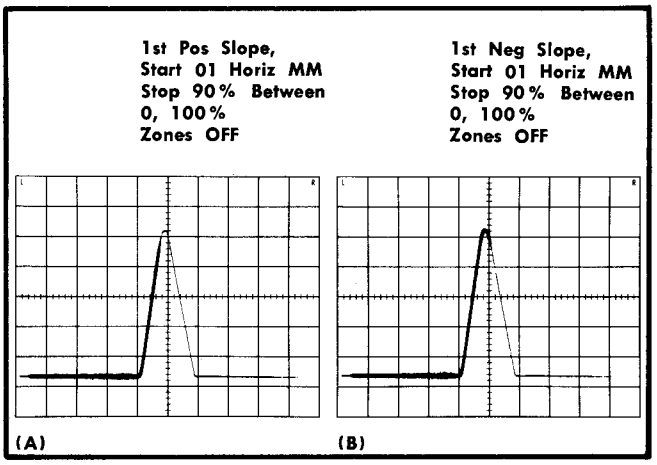


Fig. 3-5. Measurement information included in (A) Example Program 3 and (B) Example Program 4.

Character 1:	0000	No program desired.
Character 2:	1000	A 0% (Average) zone positioned at the .5 cm point on the display.
Character 3:	0001	Characters 3 and 4 program the A 100% memory to charge to the maximum positive peak of the display from the 1.5 cm position to the end of the sweep.
Character 4:	1110	
Character 5:	0000	No program desired.
Character 6:	0000	No program desired.
Character 7:	0000	No program desired.
Character 8:	0000	No program desired.
Character 9:	0100	Selects start comparison on Horizontal mm from sweep start.
Character 10:	0000	Selects start comparison at first plus slope of the signal.
Character 11:	0000	No program desired.
Character 12:	0001	Programs 1 mm from sweep start.
Character 13:	0010	Selects stop comparison point on A channel and % between the zones.
Character 14:	0001	Selects stop point at the first plus slope; disables internal scaling.
Character 15:	1001	Selects stop point to 90% level.
Character 16:	0000	No program desired.

CHARACTER	8	4	2	1	PROGRAM	PROGRAM	J201 PINS 8	4	2	1
1	A 0% POS. 8	4	2	1			1	2	3	4
2	A 0% POS. .5	A 0% Wid. 4 cm	2 cm	VOLTS			5	6	7	8
3	A 100% POS. 8	4	2	1			9	10	11	12
4	A 100% POS. .5	A 100% Wid. 4 cm	2 cm	A CHOP			13	14	15	16
5	B 0% POS. 8	4	2	1			19	20	21	22
6	B 0% POS. .5	B 0% Wid. 4 cm	2 cm	MEASURE AVE.			23	24	25	26
7	B 100% POS. 8	4	2	1			27	28	29	30
8	B 100% POS. .5	B 100% Wid. 4 cm	2 cm	B CHOP			31	32	33	34
							J202			
9	(START) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW			1	2	3	4
10	(START) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	COUNTER RESET INHIBIT			5	6	7	8
11	(START) OFFSET 80	40	20	10			9	10	11	12
12	OFFSET 8	4	2	1			13	14	15	16
13	(STOP) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW			19	20	21	22
14	(STOP) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	EXT SCALE			23	24	25	26
15	(STOP) OFFSET 80	40	20	10			27	28	29	30
16	(STOP) OFFSET 8	4	2	1			31	32	33	34
							J203			
17	EXT HORIZ ÷ 2	UPPER MINUS	UPPER LIMIT 2000	1000			1	2	3	4
18	800	400	200	100			5	6	7	8
19	80	40	20	10			9	10	11	12
20	8	4	2	1			13	14	15	16
21	EXT HORIZ ÷ 5	LOWER MINUS	LOWER LIMIT 2000	1000			19	20	21	22
22	800	400	200	100			23	24	25	26
23	80	40	20	10			27	28	29	30
24	8	4	2	1			31	32	33	34
							J204			
25	PROG DEC 2	3	4	NIXIE 'V'			1	2	3	4
26	NIXIE S	NIXIE M	NIXIE 'μ'	NIXIE 'N'			5	6	7	8
27	HIGH SPEED PGM		A CHOP[3]	B CHOP[3]			9		15	16

NOTE: GROUND CLOSURE OF A PROGRAM LINE CONSTITUTES A LOGICAL ONE (TRUE); ANY OPEN LINE IS A LOGICAL ZERO (FALSE).

[3]These bits are not used on instruments below SN 360.

Fig. 3-6. Example Programs 3 and 4.

CHARACTER	8	4	2	1	PROGRAM 3	PROGRAM 4	J201 PINS 8	4	2	1
1	A 0% POS. 8	4	2	1	0000	1100	1	2	3	4
2	A 0% POS. .5	A 0% Wid. 4 cm	2 cm	VOLTS	1000	1000	5	6	7	8
3	A 100% POS. 8	4	2	1	0001	1100	9	10	11	12
4	A 100% POS. .5	A 100% Wid. 4 cm	2 cm	A CHOP	1110	1110	13	14	15	16
5	B 0% POS. 8	4	2	1	0000	1100	19	20	21	22
6	B 0% POS. .5	B 0% Wid. 4 cm	2 cm	MEASURE AVE.	0000	0000	23	24	25	26
7	B 100% POS. 8	4	2	1	0000	1100	27	28	29	30
8	B 100% POS. .5	B 100% Wid. 4 cm	2 cm	B CHOP	0000	0000	31	32	33	34
							J202			
9	(START) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW	0100	0100	1	2	3	4
10	(START) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	COUNTER RESET INHIBIT	0000	0001	5	6	7	8
11	(START) OFFSET 80	40	20	10	0000	0000	9	10	11	12
12	OFFSET 8	4	2	1	0001	0001	13	14	15	16
13	(STOP) B CHANNEL	HORIZ MM	% BETWEEN	MM BELOW	0010	0010	19	20	21	22
14	(STOP) OFFSET FROM 100%	MINUS SLOPE	2nd SLOPE	EXT SCALE	0001	0101	23	24	25	26
15	(STOP) OFFSET 80	40	20	10	1001	1001	27	28	29	30
16	(STOP) OFFSET 8	4	2	1	0000	0000	31	32	33	34
							J203			
17	EXT HORIZ ÷ 2	UPPER MINUS	UPPER LIMIT 2000	1000	1011	1000	1	2	3	4
18	800	400	200	100	1001	0101	5	6	7	8
19	80	40	20	10	1001	0000	9	10	11	12
20	8	4	2	1	1001	0000	13	14	15	16
21	EXT HORIZ ÷ 5	LOWER MINUS	LOWER LIMIT 2000	1000	0000	0000	19	20	21	22
22	800	400	200	100	0000	0100	23	24	25	26
23	80	40	20	10	0000	1000	27	28	29	30
24	8	4	2	1	0000	0000	31	32	33	34
							J204			
25	PROG DEC 2	3	4	NIXIE 'V'	0000	0000	1	2	3	4
26	NIXIE S	NIXIE M	NIXIE 'μ'	NIXIE 'N'	0000	1010	5	6	7	8
27	HIGH SPEED PGM		A CHOP[4]	B CHOP[4]	0000	0000	9		15	16

NOTE: GROUND CLOSURE OF A PROGRAM LINE CONSTITUTES A LOGICAL ONE (TRUE); ANY OPEN LINE IS A LOGICAL ZERO (FALSE).

[4]These bits are not used on instruments below SN 360.

Fig. 3-7. Blank External Program worksheet.

Character 17:	1011	Divides the count (readout) by two so that the accumulation of the two measurements will read out the actual time to the amplitude peak; plus upper limit level. Care must be taken that the horizontal plug-in is not set in a ÷ 5 sweep rate function or erroneous readout will occur.
Character 18:	1001	Characters 17, 18, 19, and 20 are programmed for an Upper Limit level of +3999 so that no out-of-limits indication will occur on the first section of this measurement series.
Character 19:	1001	See character 18.
Character 20:	1001	See character 18.
Character 21:	0000	Characters 21, 22, 23, and 24 are programmed for +0000 so that only when the count reaches some negative value will the Lower Limit Level indicate an out-of-limits condition.
Character 22:	0000	
Character 23:	0000	
Character 24:	0000	See Character 21.
Character 25:	0000	No scaling of the readout is needed until the end of the second measurement.
Character 26:	0000	See Character 25.
Character 27:	0000	No program desired.

Since the two measurements are so alike, only the characters that differ will be listed for explanation. Assuming that the distance from sweep start to the peak of the waveform is about +490 μs and the tolerance is ±2%, the limit levels and scaling program will be set accordingly.

Character 1:	1100	Characters 1, 3, 5, and 7 are programmed to the 12 cm position to cause both A and B Memories to remain charged. This is possible since the peak amplitude to be "remembered" is the same in both words of the program. Keeping both of the memories charged allows the Type 230 to make both measurements on only one memory charging sweep, thus saving cycle time.
Character 3:	1100	
Character 5:	1100	
Character 7:	1100	
Character 10:	0001	Counter Reset Inhibit is TRUE to allow accumulation of the two measurements.
Character 14:	0101	Selects first minus slope for start point; still inhibits internal scaling.
Character 18:	0101	Characters 18, 19, and 20 form the upper limit level for the measurement, a total of +0500.
Character 19:	0000	
Character 20:	0000	
Character 22:	0100	The sum of the TRUE bits in characters 22, 23, and 24 form the lower limit level for this measurement, a total of +0480.
Character 23:	1000	
Character 24:	0000	
Character 25:	0000	The fifth decimal lamp from the right will illuminate.
Character 26:	1010	Lights the μ and s symbols in the units nixie.

The total readout should be +0490 μs.

EXTERNAL PROGRAMMING

The external programming functions may be easily checked for proper performance by any programming device which will provide the proper logic levels to the Type 230 (See the first page of the programming instructions). The need may arise to check the programming performance of the Type 230 when there is no programming device readily available. A substitute for an automatic programmer may be constructed with 105 SPST switches connected to program common on one side. The remaining pole of each switch should be connected through an inexpensive diode to a programming input. Closure of any switch will activate a single program function, and any proper measurement program can be set up readily.

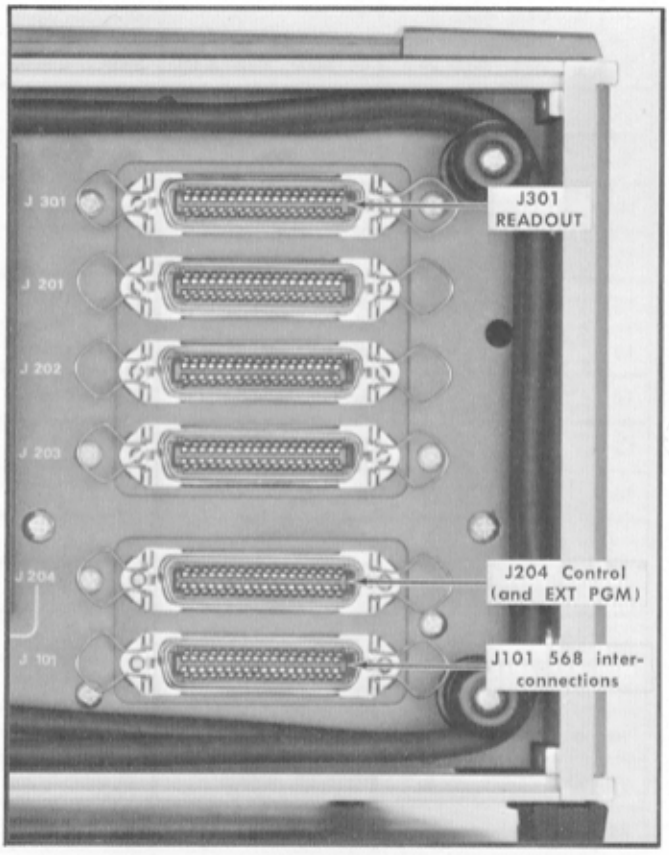


Fig. 3-8. Type 230 external connectors.

Type 230 Control Outputs

As was mentioned earlier in this text, J204 (See Fig. 3-1 or Fig. 3-8 for J204 location) is used for some external program inputs (pins 1 through 9). The majority of the remainder of the pins on J204 are used for external control outputs from the Type 230 for controlling external devices. Fig. 3-9 illustrates the connectors of J204. The following list by pin number explains the purpose of each line.

J204 Pin 17 As mentioned earlier, this is a program ground enabled by the MEASUREMENT MODE switch on the front panel.

Pin 18 Ground to the Type 230 chassis.

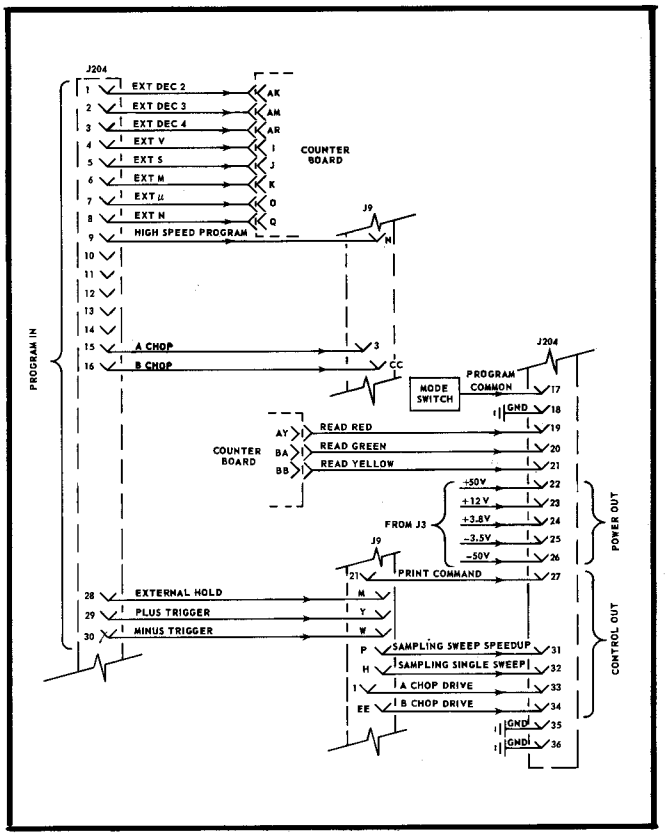


Fig. 3-9. J204 wiring diagram.

Pin 19 READ RED: This output from the Limit Lamp Driver circuitry on the Counter and Readout board is low when the measurement exceeds the Upper Limit Level. This and the outputs from pins 20 and 21 can be used to control an external device which would stop further measurements by the Type 230 on a device under test.

Pin 20 READ GREEN: Indicates the measurement is within limits. See J204 pin 19.

Pin 21 READ YELLOW: Indicates that the measurement has exceeded the Lower Limit level. See J204 pin 19.

Pin 22 +50 volts (±1% at 50 mA maximum) available for powering external controlling units.

Pin 23 +12 volts (±1% at 350 mA maximum; see pin 22.

Pin 24 +3.8 volts (±1% at 200 mA maximum); see pin 22.

Pin 25 —3.5 volts (±1% at 200 mA maximum); see pin 22.

Pin 26 —50 volts (±1% at 25 mA maximum); see pin 22.

Pin 27 PRINT COMMAND: This line is used to signal an external device that a measurement has been completed and the measurement information has been shifted into the storage registers of the Type 230. Normally, the PRINT COMMAND negative step will occur 150 μs after the storage registers are set.

Pin 28 EXTERNAL HOLD: This line is essentially a control input to the Type 230. When EXTERNAL HOLD is TRUE, it keeps the storage registers from resetting. EXTERNAL HOLD, in conjunction with the readout section (J301), may be used to stop the measurement cycles when an out-of-limits situation occurs.

Pin 29 PLUS TRIGGER: Used to synchronize the speed and occurrence of measurement cycles with some external source.

Pin 30 MINUS TRIGGER: See pin 29.

Pin 31 SWEEP SPEEDUP: This line is a control from the Type 230 to the Type 568 horizontal plug-in unit to speed up the repetition rate of measurement cycles by decreasing the total sweep time.

Pin 32 SWEEP RESET (SINGLE SWEEP): This line is a control from the Type 230 to the Type 568 horizontal plug-in unit (Type 3T5 or 3T6) to speed up the repetition rate of measurement cycles by resetting the sweep when the memories are charged or the measurement is complete[5]. With a Type 3T4 plug-in unit, this line causes the unit to permit only one measurement cycle for each triggering pulse.

Pin 33 A CHOP DRIVE: Provides a synchronizing signal to an external signal chopper for the Type 568 vertical plug-in A channel input.

Pin 34 B CHOP DRIVE: Same as pin 33 except for B channel.

Pins 35 and 36 Chassis ground.

Readout Connector J301

Jack J301 (See Fig. 3-8 for physical location of J301) provides an external readout of measurement information from the Type 230 to an external recording device. Fig. 3-10 is a wiring diagram of the Type 230 internal connections to J301. On each line in use, the descriptive label indicates the function of the individual line when TRUE. For example, READ PLUS at J301, pin 1 comes from pin AH on the Counter and Readout board. When TRUE, READ PLUS indicates that the measurement is positive. With the exception of open pins 17 and 18, pins 1 through 29 are information outputs from the Counter and Readout section of the Type 230. Pin 31 (PRINT COMMAND) provides an indication to an external receiver that the measurement is complete and may be recorded.

J301 Pin 30 EXTERNAL HOLD: This line permits an external recorder to prevent clearing the measurement data in the registers.

Signal Connector J101

Jack J101 provides interconnection between the Type 230 and the Type 568 (See Fig. 3-9 for the physical location of J101). Fig. 3-8 shows the internal connections from J101 to

[5]**Does not apply to Synchronizer Circuit Card Series F, Model 1 and 2.**

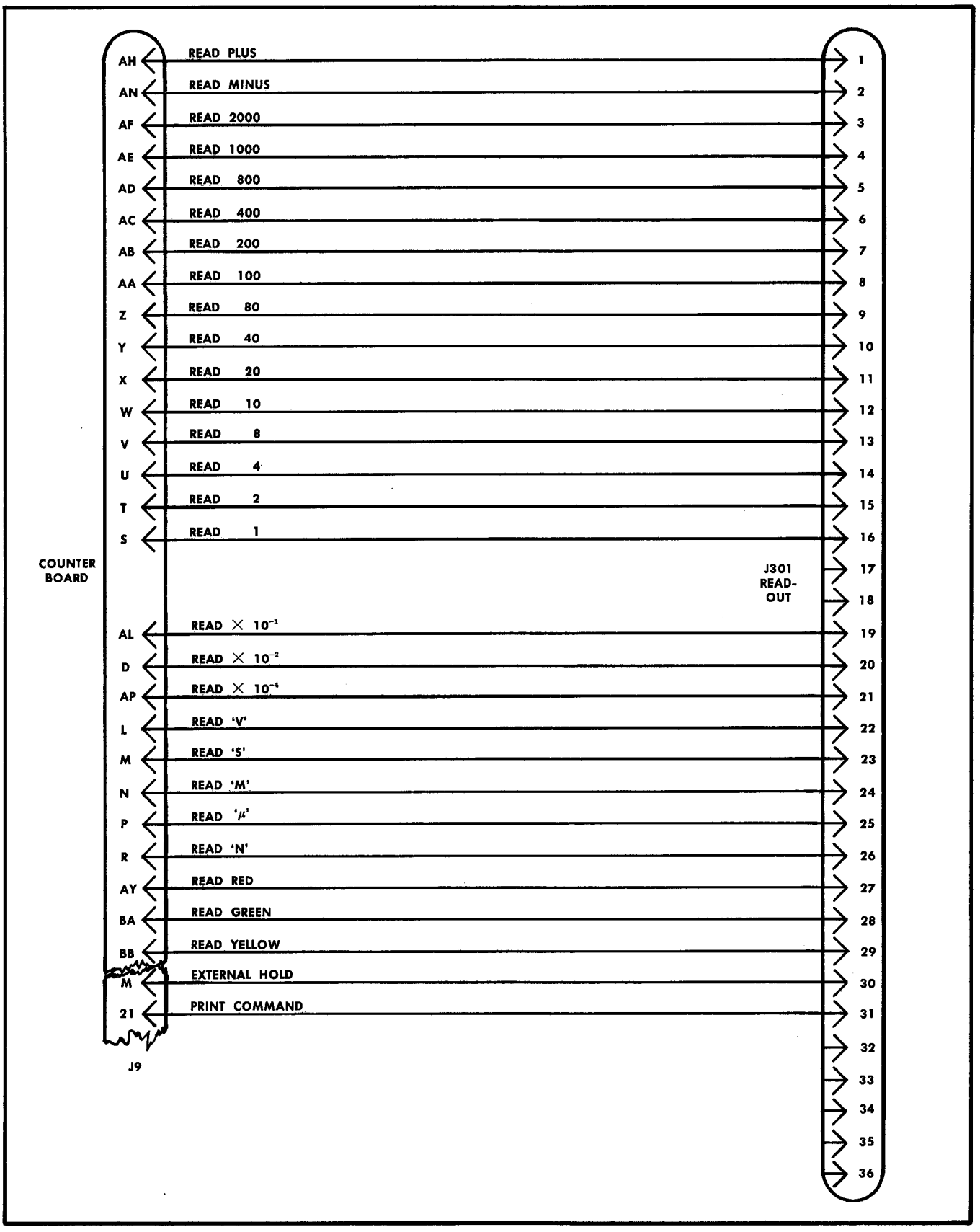


Fig. 3-10. J301 wiring diagram.

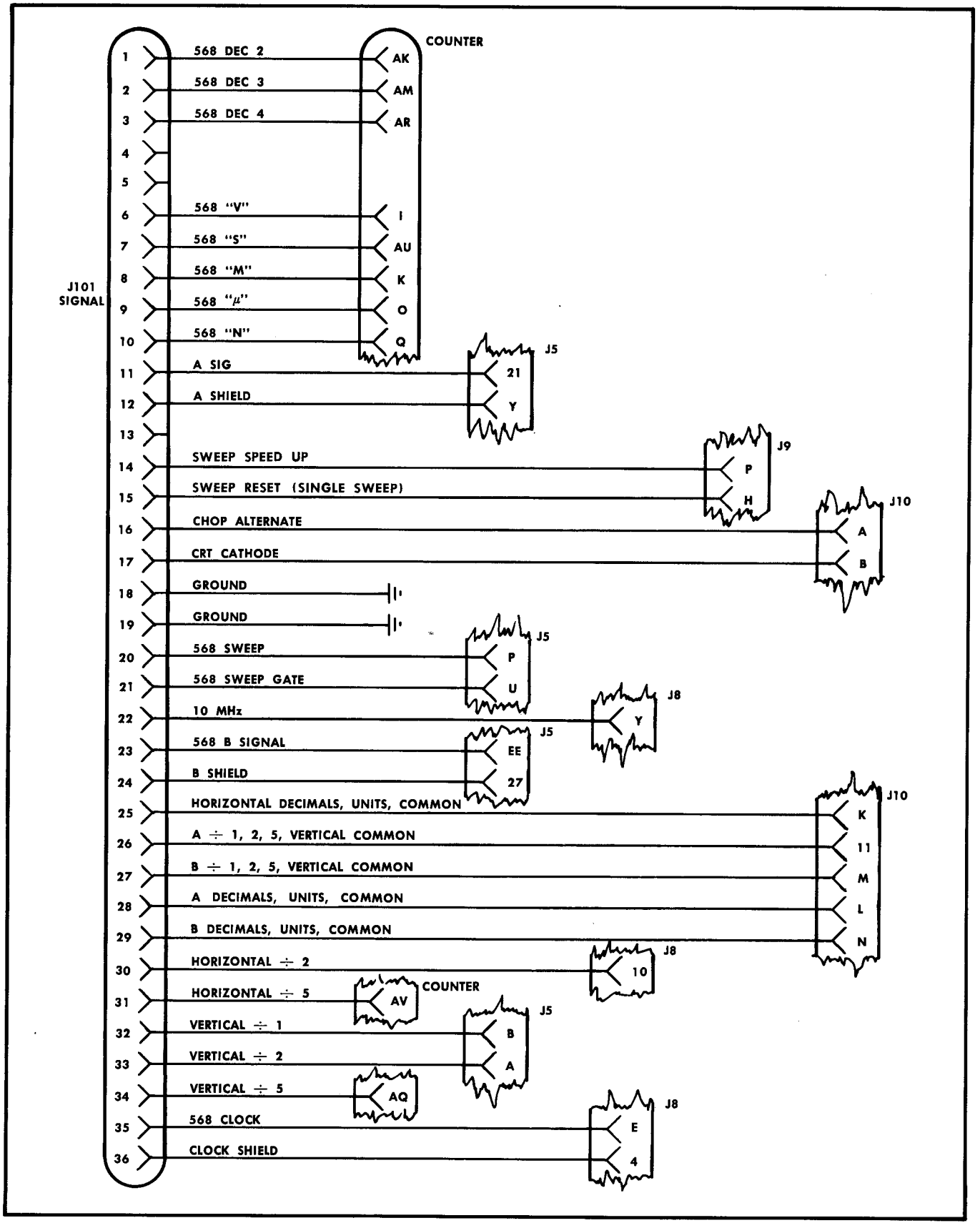


Fig. 3-11. J101 wiring diagram.

the various cards in the Type 230. An explanation of the lines by pin number follows:

J101 pins 1, 2, and 3 are the decimal position commands from either the vertical or horizontal plug-in. Pins 6, 7, 8, 9, and 10 control the unit symbols on the front panel readout. This may be accomplished by either the vertical or the horizontal plug-in.

Pin 11 A SIGNAL: This conveys the A channel signal from the vertical plug-in. This signal is connected to the Buffer card.

Pin 12 The shield for the A channel signal line.

Pin 14 SAMPLING TIME-BASE SPEED-UP: An internal command line from the Type 230 synchronizer card to the Type 568 horizontal plug-in. This line causes the time-base unit to speed up the sweep during non-measure time, thereby increasing the number of measurements available per second.

Pin 15 SAMPLING TIME-BASE SINGLE SWEEP: This is also a command line from the Synchronizer card to the horizontal plug-in. It will, when TRUE, shift the plug-in to a single sweep mode.

Pin 16 CHOP ALTERNATE: This is from the vertical plug-in to the CRT Intensification card. When the plug-in is in a multi-trace mode, this line synchronizes the display intensification to the proper channel.

Pin 17 CRT CATHODE: This comes from the CRT Intensification card to the Type 568 Z axis input. All of the Type 230 display intensification commands emanate from this source.

Pins 18 and 19 Chassis ground.

Pins 20 and 21 568 SWEEP and 568 SWEEP GATE (respectively): Input lines to the Type 230 Buffer card. Both inputs come from the Type 568 horizontal plug-in.

Pin 22 10 MHz CLOCK: An enabling line to the 10 MHz clock generator in the Type 230. This provides the proper digital resolution for certain real-time horizontal plug-ins.

Pin 23 568 B SIGNAL: The B channel from the vertical plug-in appears at pin 23.

Pin 24 The shield for the B channel line.

Pins 25, 26, 27, 28, and 29 Plug-in common lines. The selection of one or more of these common lines is made in the scaling logic section of the CRT Intensification card.

Pin 30 HORIZONTAL ÷ 2: This is selected by the horizontal plug-in to cause the clock generator to reduce its frequency by a factor of two.

Pin 31 HORIZONTAL ÷ 5: This is selected by the horizontal plug-in to cause the readout to be multiplied by 2.

Pin 32 VERTICAL ÷ 1: Comes from the vertical plug-in to change the rate of rise of the voltmeter ramp in the Buffer card.

Pin 33 VERTICAL ÷ 2: See Pin 32.

Pin 34 VERTICAL ÷ 5: This goes to the decimal section of the Counter and Readout board. When the vertical plug-in is in factor-of-two position (2 V/cm, 2 mV/cm, etc.), this line shifts the decimal one place left.

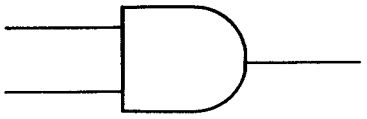
Pin 35 568 CLOCK: The clock from the horizontal plug-in is sent from this pin to the Type 230 clock card.

Pin 36 A shield for pin 35 information.

GLOSSARY OF TERMS

Activated — A circuit is said to be activated if it is performing its indicated logical function. This does not necessarily mean conduction.

AND — An AND gate is a device having two or more inputs. In order for an AND gate to be activated, all inputs must be activated.



Bit — Abbreviated form of the word binary digit used to denote one element of binary information.

Buffer — a. A device used between two circuits to reduce loading of one upon the other.

b. A device used to increase the fanout of a preceding circuit.

Carry — The term used to describe the output which occurs as an overflow from a counter.

Character — A group of bits ordinarily presented in parallel form.

Clear — To reset a circuit. To cause a bistable device to return to a ready state in which it will accept an activating pulse or level.

Clock — An oscillator or generator which times or synchronizes the computing process. The clock speed usually limits the counting or computation speed of the entire system.

Complement — The opposite state. To cause an opposite state to occur. In a bistable device there are two voltage levels available at the inputs or outputs, one level is the complement of the other, and vice versa. The vinculum, a line drawn above a term, is used to indicate the complement of that term. Example:

High = High 1 = 0 True = True;
True = False, High = Low, 1 = 0

Counter — A computing unit which produces the sums of digital numbers or indicates the totals of numbers entered.

Decade Counter — An electronics counter which automatically resets to zero at the count of ten.

Decoder — A device used to convert from one number system to another. Two most commonly used types are the Binary-to-Decimal, and the Decimal-to-Binary. The Binary-to-Decimal decoder is often used at the output of a digital device to convert binary information into the more readily distinguishable decimal information.

Don't Care — The case in logic where certain input combinations cannot or will not occur. Hence they may be ignored. Example: Ordinarily a four-binary counter will produce any of sixteen combinations. If converted to a decade counter, binary numbers ten through sixteen will not appear at the output. They have no effect on the next circuit and can be ignored or called don't cares.

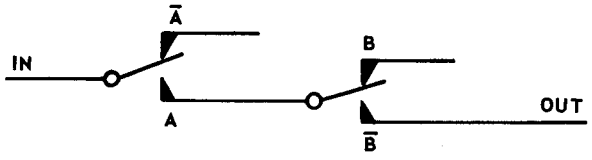
Enable — The occurrence of a pulse or level at one input of a device. This pulse or occurrence will enable the circuit to accept an activating level at another input.

FALSE — The state of a device which occurs when it is not activated. One or more of its inputs are not activated, hence its output line indicates a "false" condition.

High — A logical state or level. A high state may be assigned as a logical one or zero, depending upon whether positive or negative logic methods are used. High is usually designated as the more positive of two logic levels.

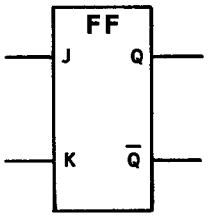
Inhibitor — A device which negates the passage of a signal at one input by the presence of a signal at another input.

Example:



JK flipflop — The JK flipflop is essentially the same device as an RS flipflop, with one exception: a JK flipflop will accept the presence of any combination of inputs, whereas the RS will not. When a one is placed at both inputs, the JK will toggle or complement, instead of reverting to an undefined output.

There are some variations to the basic configuration of the JK flipflop. It may have a clock input, and if neither the J nor K are in the one input condition the clock will toggle the flipflop at the clock rate. The logic symbol and truth table for a JK flipflop are shown following:



J	K	Q	$\bar{Q}$
0	0	no chonge	
1	0	0	1
1	1	toggle	

Logic Diagram — A diagram that depicts by logic symbols and supplementary notations the details of signal flow and control, but not necessarily the point-to-point wiring, existing in a system of two-state devices.

Logic Function — A combinational, storage, delay, or sequential function expressing a relationship between signal input(s) to a system or device and the resultant output(s).

Logic Levels — Levels of voltage which are assigned a logical meaning. They are usually consistant in meaning throughout a system. For instance, 0 V or ground might be a logical one, and +4 V a logical zero. The chief criteria for logic level values is that they can activate or de-activate the particular devices.

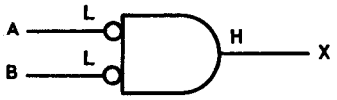
Low — The more negative or less positive of two logic levels. It may be assigned either a logical 0 or 1 depending upon whether negative or positive logic is specified.

Majority Logic — Majority Logic refers to a logic circuit which delivers a level at its output which is governed by the majority of its input levels. A majority circuit must have three or more inputs. The inverted output of a majority circuit is identical to the output of a minority circuit.

Minority Logic — Minority Logic describes a logic circuit which has three or more inputs and delivers an output level governed by the logic state of a minority of its inputs. The inverted output of a minority circuit is identical to the output of a majority circuit.

NAND — A logic circuit having two or more inputs. It is activated only when all input levels are of the opposite state in comparison to the activated output.

Example:

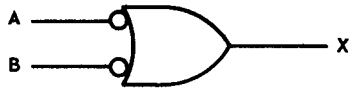


X will only be High when A and B are low. Any other combination of input levels will produce a low at the output.

Negative Logic — If the less positive potential (current) is consistently selected as the 1-state, the resultant system, or device, is said to have negative logic.

NOR — A modification of the basic OR circuit where the activated output requires the existance of its logical opposite on any of one or more inputs.

Example:

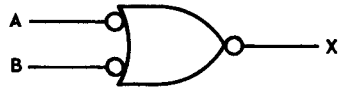


The presence of a low level at A or B or both A and B will produce a high at X.

ONE — An assignment symbol used to relate to one or the other of two states of a bistable device. A ONE may represent either a high or a low level.

OR — A circuit which delivers an activated output whenever any one of its two or more inputs are at the same logic level as its output.

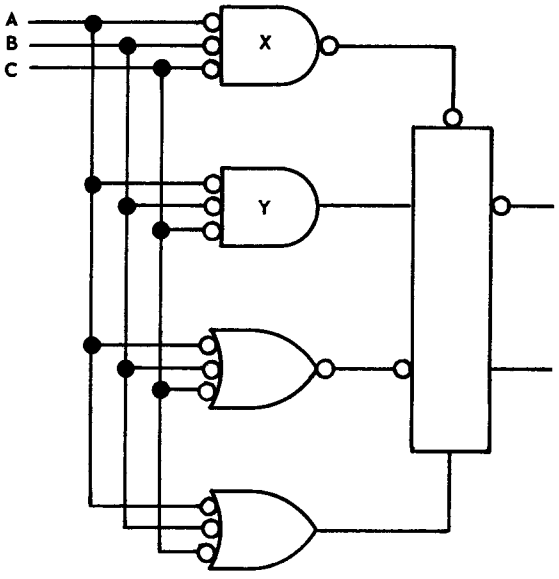
Example:



Either A or B or both in a low state will produce a low state at X.

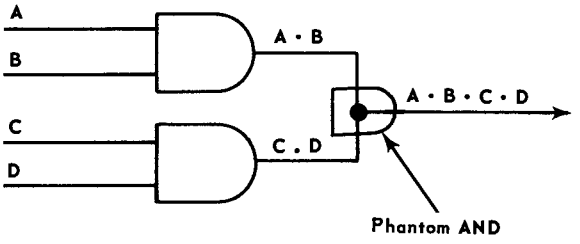
Parallel — The case where a group of numbers or pulses are delivered simultaneously.

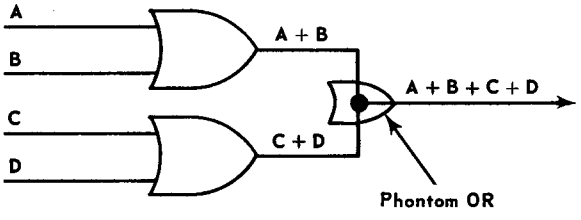
Example:



Phantom AND, Phantom OR — The connection of two logic device outputs which exhibits a logic function at their junction.

Example:





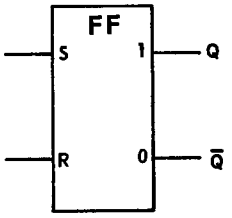
Positive Logic — If all signal line terminals in a logic diagram of a system or device have the same pair of physical states, and if both are electric potentials (currents), and if the more positive potential (current) is con-

sistently selected as the 1-state, the resultant system, or device, is said to have positive logic.

Register — Consists of a group of flipflops in parallel to constitute a single register. Its purpose is to store a group of binary digits or levels.

RESET — To cause a flipflop or register to revert to its ready or zero state.

RS flipflop — A bistable device which, when triggered, will change its output level(s) from one stable state to the other stable state. Ordinarily, the RS flipflop has two inputs, labeled SET and RESET (or CLEAR). The application of a one to both inputs will cause the flipflop to revert to an undefined state. The application of a one to the RESET input will cause the flipflop to exhibit a zero at its output. If a one is then applied to the SET input, the flipflop will then change to a one at its output. Most RS flipflops have two outputs labeled Q and Q. With proper input conditions, the outputs will always be the complement of one another. The logic symbol and truth table for an RS flipflop are shown below:



S	R	Q	Q̄
0	0	no change	
0	1	0	1
1	0	1	0
1	1	undefined	

Serial — Connecting devices in a series arrangement such that all information is processed consecutively. This is opposite to Parallel, which accepts the different bits of information simultaneously.

SET — To cause a flipflop or register to shift to the one state, or opposite to reset.

Shift Register — A circuit which will shift a digit or a group of digits (levels) to the left or to the right. It is often used to convert information from parallel to serial or vice versa.

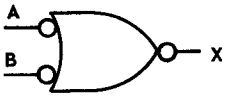
States in Binary Logic — The two physical states on each terminal of each signal line shall be referred to as the 0-state and the 1-state. The 0-state may be called the reference (inactive, antifiducial) state, and the 1-state the significant (active, fiducial) state. The above must not be construed as implying that the 1-state requires more power, contains more energy, or is at a higher potential than the 0-state. The state designations are purely arbitary as far as the physical interpretation is concerned.

Store — To cause a group of digits to be placed in a device (register, memory, etc.) from whence it may be delivered at a later time.

Toggle — To cause a flipflop to change its output condition from one logic state to the other. If the output is a one before the flipflop is toggled, it will be at the zero condition after it is toggled once.

TRUE — The case in logic where a device is fulfilling its active function.

Example:

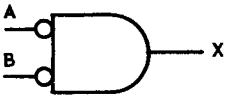


H = High
L = Low

A	B	X
H	H	H = FALSE
H	L	L = TRUE
L	H	L = TRUE
L	L	L = TRUE

Truth Table — A table listing all of the input possibilities of a device along with the output condition of each set of possible conditions. The truth table may use highs and lows or ones and zeros.

Example:



A	B	X	A	B	X
0	0	1	H	H	L
0	1	1	H	L	L
1	0	1	L	H	L
1	1	0	L	L	H

Word — A set of characters that occupies one storage location as is transported as a unit.

ZERO — An assignment symbol used to relate to one or the other of the two states of a bistable device. Zero may either equal a high or low level, but is must represent the opposite state of a logical one.

NOTES

SECTION 4
CIRCUIT DESCRIPTION

Introduction

The Type 230 Digital Unit is a programmable time and voltage measurement unit. External program connectors on the rear panel provide for interconnections to a programming device. Front panel controls, switches, and readouts permit manual control of most programmable functions. The signal processing circuitry of the unit is contained on 11 plug-in circuit cards and one circuit board. This section of the manual describes the operation of the Type 230; first in block diagram terms and then on an individual circuit card basis.

On the block diagram level, overall descriptions are given of instrument operation when making time measurements and when making voltage measurements. Block diagrams are included within the text to show the difference between the two modes of operation. An overall block diagram, located in the Diagrams section, shows the relationship between the major circuits of the instrument.

Following the block diagram description, this section contains a description of each circuit in the Type 230. In general, where a circuit functions as an analog or linear device, a conventional circuit description is given. If a circuit performs a logic function, a logic description is given. In the Type 230, the activated logic state is provided by a low voltage level (0 to +2 volts) and corresponds to the true logic state or a logical one. The non-activated logic state is provided by a high voltage level (+6 to +12 volts) and corresponds to the false logic state or a logical zero. Any logic line that is not connected to a low logic level automatically assumes the false (high) state. The "high" and "low" convention will be used as a general rule in this description.

Block diagrams, logic diagrams, and waveform illustrations are included within the text to support and clarify the description. Overall logic diagrams of some of the more complex circuit cards are included in the Diagrams section. Complete circuit card diagrams are also included in the Diagrams section. The circuit diagrams should be referred to for electrical values and those circuit elements not given on the logic diagrams.

BLOCK DIAGRAM DESCRIPTION

Time Measurements

The usual way to measure time with an oscilloscope is to count the horizontal divisions on the CRT between the measurement limits. This distance multiplied by the sweep rate equals the elapsed time. With the Type 230, the elapsed time between two points on a waveform display is measured with a counter and presented as a digital readout. To make a time measurement, the Type 230 needs specific information from the vertical amplifier and the time-base plug-in units. The required information is applied via an interconnecting cable from the Type 568 Oscilloscope and includes the following:

1. Horizontal sweep waveform
2. Sweep gate waveform
3. Clock pulses
4. Unit of measure (ns, μs, etc.)
5. Decimal point position information
6. Signal to be measured

Figure 4-1 shows the time relationship between a typical signal and the horizontal waveform. The intensified 0% and 100% zones (points A and B on the signal waveform) can be moved to any of 20 positions on the display by turning the 0% and 100% controls on the front panel (0.5 cm zone movement between switch positions). In the description that follows, the 0% intensified zone of the CRT is set for the most negative point of the signal, and the 100% zone is set for the most positive point.

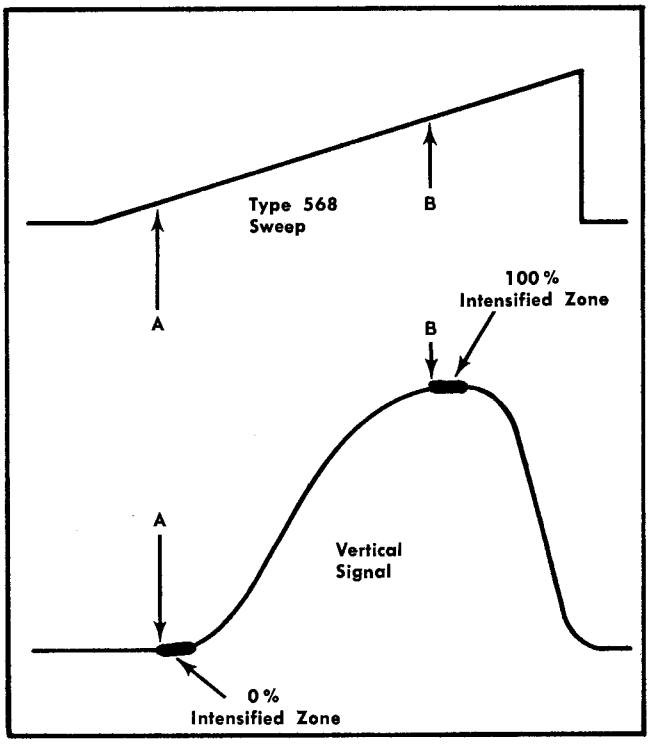


Fig. 4-1. Time relationship of Type 568 sweep, signal, and intensified zones.

The horizontal sweep, after passing through a buffer stage, is applied to the 0% and 100% zone generator circuits (see Fig. 4-2). The horizontal sweep voltage is combined with the voltage from each zone generator circuit to form gate pulses that are delayed a preset amount of time from the sweep start. These gate pulses are applied to memory circuits.

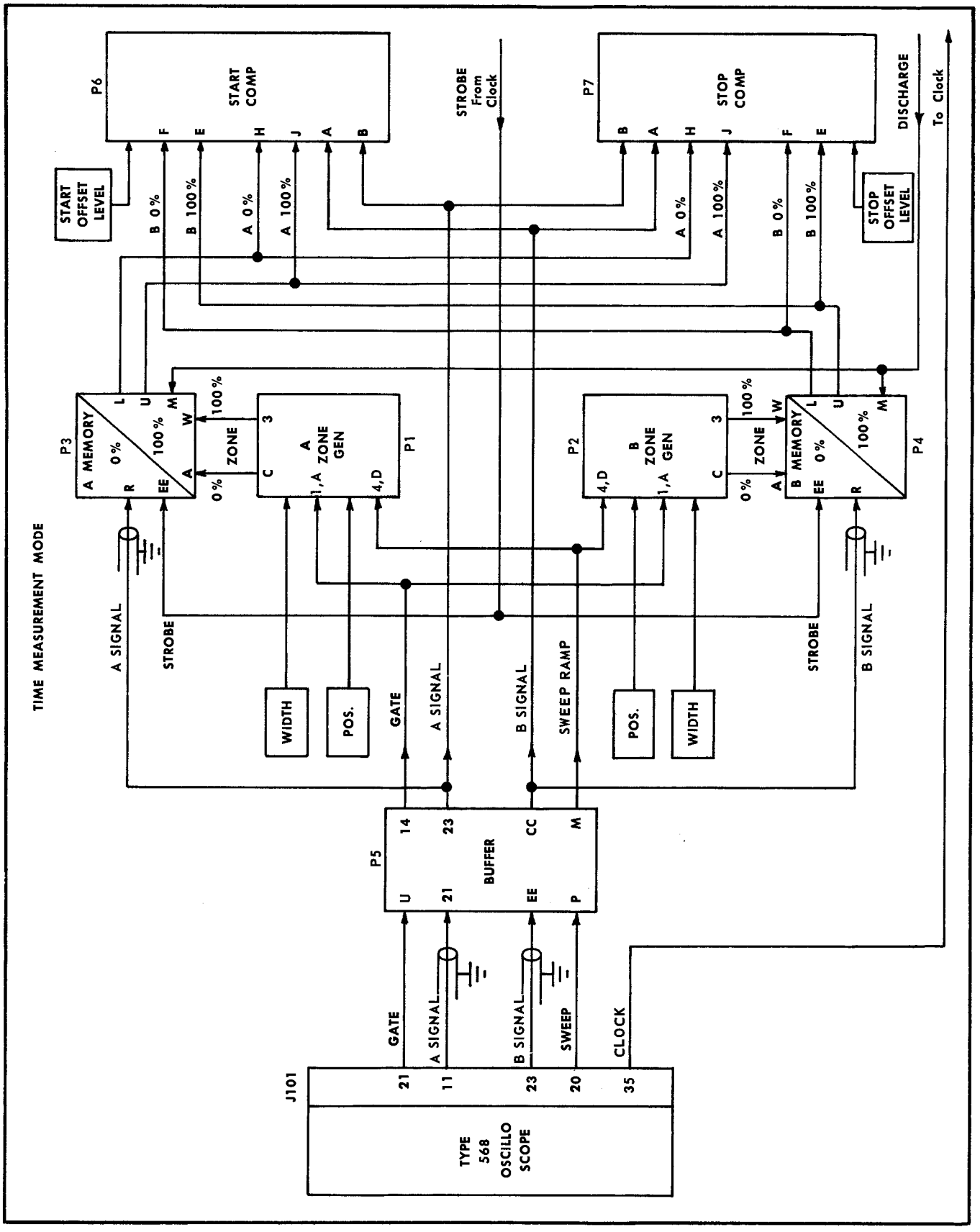


Fig. 4-2. Block diagram showing signal flow to start and stop comparators, time measurement mode.

There are two memory circuit cards, one for Channel A and one for Channel B. The use of two memory circuits provides the Type 230 with the capability of starting a measurement on one trace of a dual-trace display and ending the measurement on the other trace. For example, the time difference between pulses on two different signal lines can be measured.

When the 0% gate pulse is generated as previously explained, the 0% memory samples the vertical signal voltage at point A of Figure 4-1. This sample is stored in the 0% memory circuit. The output of the 0% memory circuit is applied to one input on each of two differential comparator circuits (the start and stop comparators). Each memory circuit takes a sample of the vertical signal and its output automatically adjusts to the signal voltage with every sweep.

When the horizontal sweep reaches point B in Figure 4-1, the sweep voltage and the voltage from the 100% zone generator combine to form a gate pulse that activates the 100% memory circuit. The 100% memory circuit samples the vertical signal at point B and stores it. The output of the 100% memory circuit is applied to a second input of the differential comparator circuits.

Each comparator needs two inputs:

1. A pre-selected DC voltage level that sets the point of comparison (start or stop point of measurement).

2. The signal from the vertical amplifier plug-in or the sweep waveform. (The START SLOPE and STOP SLOPE switches on the front panel are set to the polarity of the waveform slope being measured, plus or minus slope, and 1st slope or 2nd slope. In programmed operation, the selections are made by programming inputs).

The DC voltage level referred to in (1) above can be a percentage of the voltage between the two memories, a voltage offset from either of the memories, or a selected DC offset voltage referenced to ground as in the case of "Horiz mm" offset. The signal in (2) above can be from either the A Channel or B Channel of the vertical plug-in unit.

Figure 4-3 shows the comparators and the time relationship between the reference and signal voltage. To illustrate the operation, the instrument is set to make a 10% to 90% time measurement as follows:

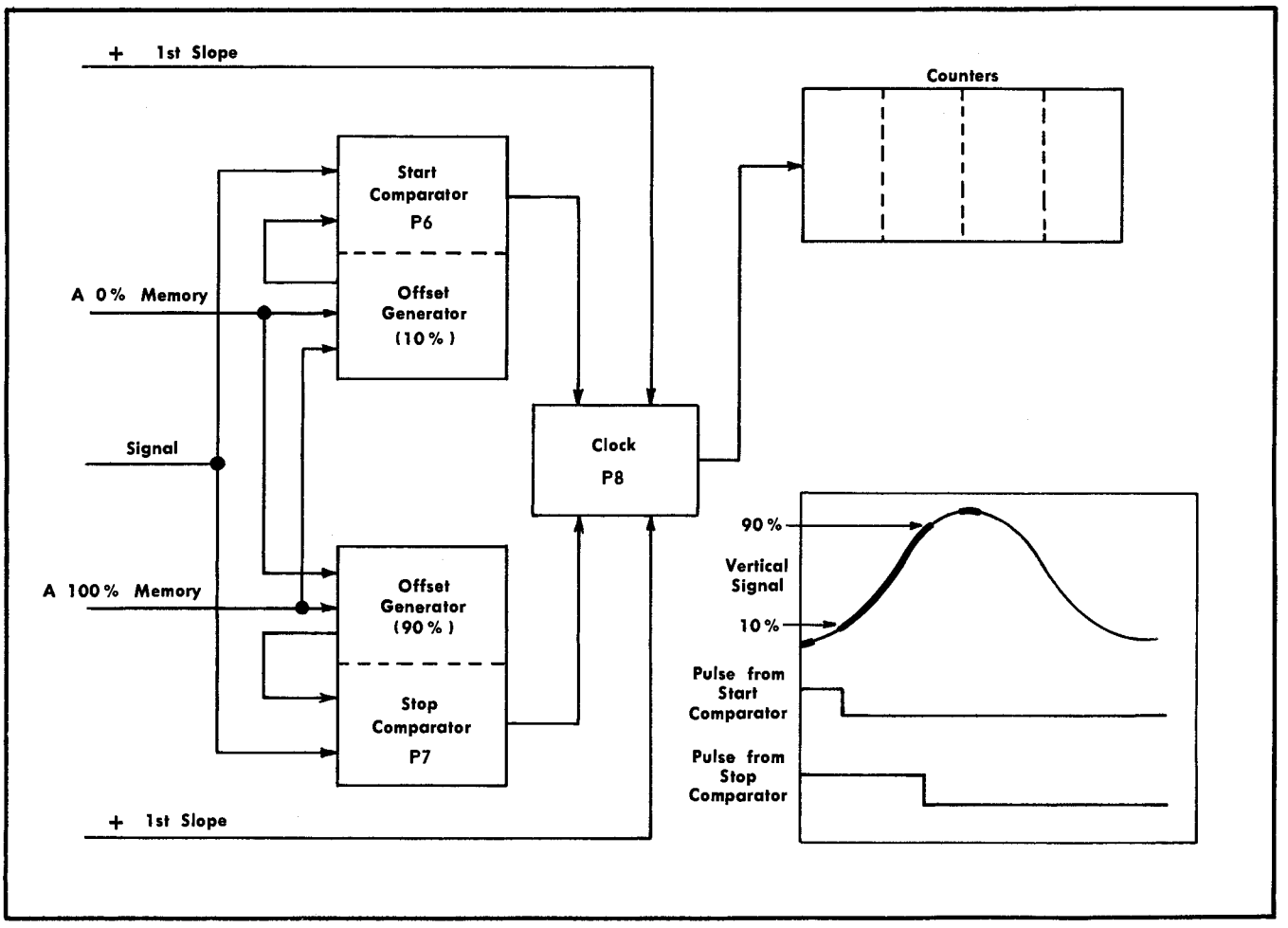


Fig. 4-3. Block diagram showing start and stop comparator pulse generation.

1. Both the 0% and 100% memory levels are applied to the offset generator (mounted on the Start Comparator circuit card) whose output is a voltage level selected to be 10% of the voltage between the 0% and 100% memory levels. This 10% voltage is applied to one side of the start comparator.

2. In an identical manner to that explained above, a 90% voltage level is generated by the offset generator on the Stop Comparator circuit card and is applied to one side of the stop comparator.

The other input of each differential comparator receives the vertical signal from the buffer stage. When the vertical signal rises to 10% of its amplitude, the start comparator switches and sends a pulse to the clock gate, allowing clock pulses to pass to a counter. When the signal voltage reaches 90% of its amplitude, the stop comparator fires and ends the pulse to the clock gate. Thus between the firing of the start comparator and the firing of the stop comparator, clock pulses are passed to the counters. As a result, the number shown on the readout is the time between the 10% and 90% voltage points of the vertical signal.

Voltage Measurements

Figure 4-4 shows the connections to the comparators when making voltage measurements. For simplification, only one signal, one zone generator and one memory are shown. Note that the front panel START and STOP functions are not used when making voltage measurements.

When making voltage measurements, the reference voltages for the comparators are the memory outputs (derived from the vertical signal). The other input to the differential comparators is a voltmeter ramp voltage generated on the Buffer circuit card. As the voltmeter ramp voltage rises through the 0% memory voltage the start comparator fires. This sends a pulse to the clock gate and gates a 1 MHz clock (generated on the Clock circuit card) to the counters. When the voltmeter ramp voltage rises through the 100% memory voltage, the stop comparator fires and sends a pulse to the counter. The voltage between the 0% and 100% levels is equal to the number of 1 MHz clock pulses times the voltmeter ramp rate of rise.

There are three linear voltmeter ramps generated on the Buffer circuit card. The voltmeter ramp applied to the comparators for a particular measurement is determined by the setting of the volts/div switch of the vertical plug-in unit. The rate of rise for the voltmeter ramp for a particular setting of the volts/div switch is as follows: (a) 2.5 mV/μs for any "2" setting of the volts/div switch (÷5), (b) 5 mV/μs in any "1" setting of the volts/div switch (÷1), and (c) 10 mV/μs in any "5" setting of the volts/div circuitry (÷2). Likewise, the position of the decimal point and the unit of measure are determined by the input attenuator switching of the vertical plug-in unit (volts/div).

The foregoing discussion briefly outlines the two basic operating modes of the Type 230. The functions of the synchronizer, counter, and limit comparator circuits are basically the same for both modes of operation. The synchro-

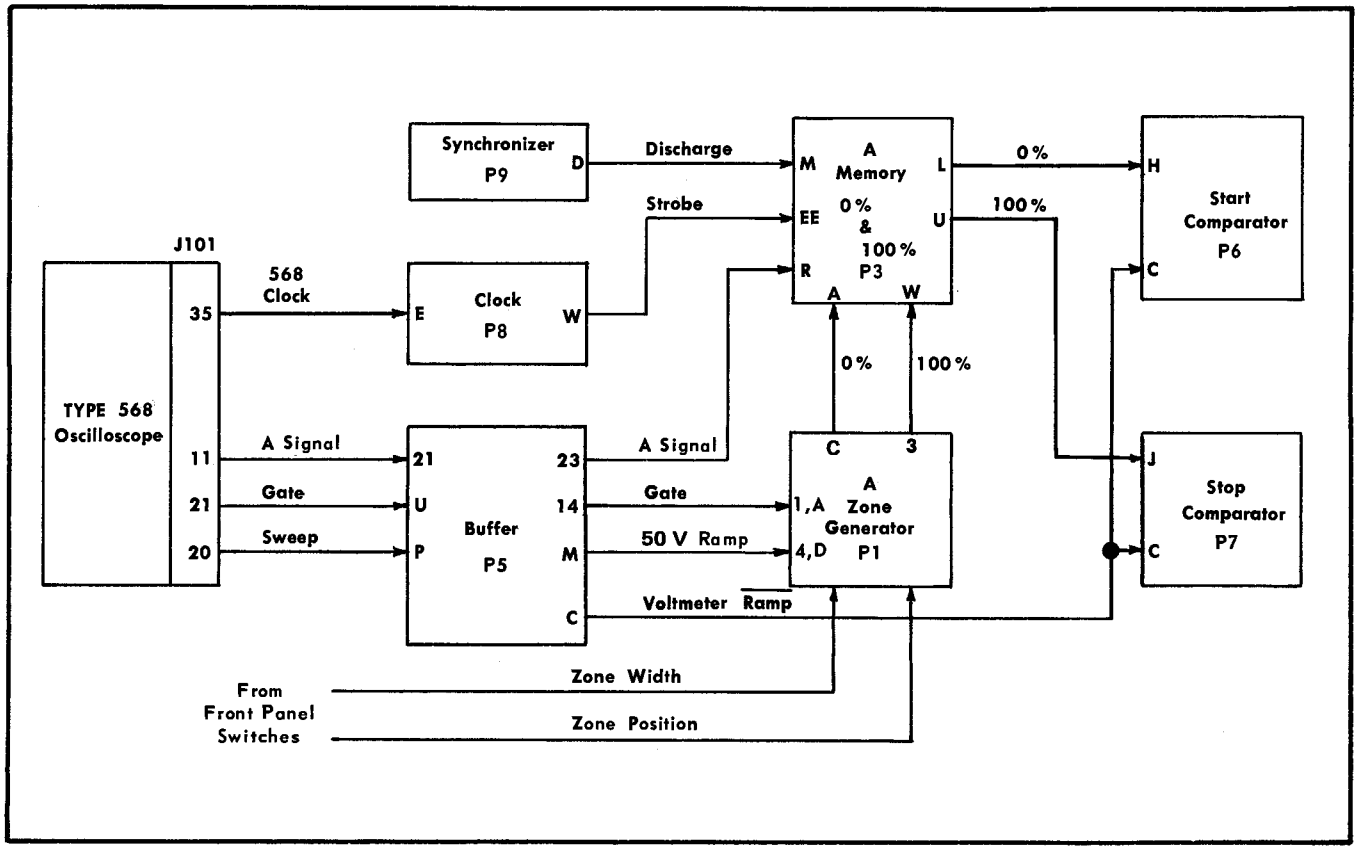


Fig. 4-4. Block diagram of signal flow to the start and stop comparator circuits, volts mode.

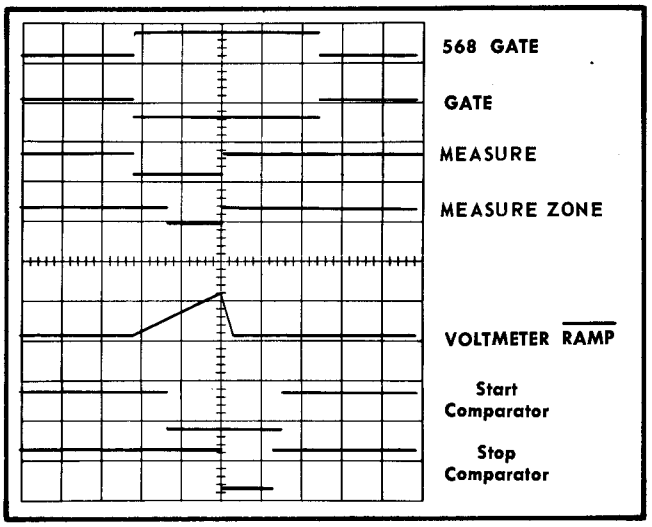


Fig. 4-5. Waveform diagram showing major signals used in volts mode.

nizer is the heart of the whole system in that it directs the system to perform all of its functions in their proper sequence. The synchronizer is comprised of a delay generator, logic gates, and flip-flops. The delay generator generates the DELAY pulse which starts the measurement cycle. Other pulses derived from the DELAY pulse discharge the memories, reset the clock and counters, and tell the circuitry when to measure (see Fig. 4-5). The counter counts and stores the gated clock pulses (digitized measurement) from the clock circuit. The limit comparators take the binary information from the register and compare it with preset limits (either front-panel or externally programmed) and read out the comparison results.

A detailed analysis of the operation of the various circuits in the Type 230 is given in the following circuit card descriptions. Refer to the end of Section 3 for a definition of terms.

CIRCUIT ANALYSIS
BUFFER CIRCUIT CARD

The Buffer circuit card provides the interface between external equipment and the circuits within the Type 230 proper. Circuits on the Buffer circuit card are presently comprised of gating circuits, a ramp generator circuit, and two operational amplifiers. The Buffer circuit card has been kept uncomplicated for easy re-design if future external equipment changes cause interface problems.

GATE and $\overline{\text{GATE}}$ Generator Circuit. The signal on connector P5 pin U (see Fig. 4-6) is actually the plus gate from the time base plug-in unit. Throughout this description this particular signal is referred to as the 568 GATE since it arrives via the Type 568. The 568 GATE goes high at the start of the sweep, then goes low as the sweep ends.

From P5 pin U the 568 GATE is applied to transistor Q611. The inverted output at the collector of Q611, now called SWEEP GATE, is applied to two circuits; to the Zone Generator circuit card via P5 pin W, and to the base of transistor Q613. The SWEEP GATE output from the collector of Q613 is applied to pin 6 of three-input NAND gate M614. When the 568 GATE goes high at the start of a sweep, the output of M614 pin 5 goes low, causing flipflop M618 to toggle. The output on M618 pin 5 goes low and starts the GATE pulse. Simultaneously, the output on M618 pin 7 goes high and generates the $\overline{\text{GATE}}$ pulse. The high $\overline{\text{GATE}}$ signal, through capacitor C621, resets flipflop M620 and the resulting high output on M620 pin 4 starts the voltmeter ramp generator (transistors Q652, Q663, Q666 and associated circuitry).

The high output of M620 pin 4 is also applied to M614 pin 7 and holds the output of M614 pin 5 low. Thus the 568 $\overline{\text{GATE}}$ cannot end GATE and $\overline{\text{GATE}}$ until the VOLTMETER $\overline{\text{RAMP}}$ is ended.

The MEASURE signal on P5 pin K goes low at the start of the measure sweep. When MEASURE goes high, M620 switches and the resulting low output on M620 pin 4 biases Q652 into conduction and ends the VOLTMETER $\overline{\text{RAMP}}$. As VOLTMETER $\overline{\text{RAMP}}$ goes low, transistor Q617 is biased into conduction and applies a low to M614 pin 8. The 568 GATE goes low at the end of the sweep. With all three of its inputs low, M614 pin 5 applies a high to M618 pin 6. Flipflop M618 sets, ending GATE and $\overline{\text{GATE}}$. If for some reason MEASURE does not go high, the VOLTMETER $\overline{\text{RAMP}}$ continues to run up until the current through resistor R625 switches M620. In this case, capacitor C624 speeds up the switching process. The switching of M620 ends VOLTMETER $\overline{\text{RAMP}}$ as previously explained.

Voltmeter Ramp Generator. The voltmeter ramp generator is an integrating Miller run-up circuit comprised of transistors Q663 and Q666 and associated circuitry. The rate of linear rise is controlled by capacitor C665 and resistor R661 in series with variable resistor R660. Operation of the voltmeter ramp generator is as follows:

The output of M620 pin 4 is coupled to the base of inhibitor transistor Q652. Transistor Q652 forms a current shunt through diode D653 to prevent the generation of a VOLTMETER $\overline{\text{RAMP}}$ until $\overline{\text{GATE}}$ goes high and resets M620. With M620 reset by $\overline{\text{GATE}}$ as previously explained, the output of M620 pin 4 goes high and reverse biases Q652. Diode D653 is now reverse biased. Timing current from resistor R660 is allowed to flow into timing capacitor C665 and the VOLTMETER $\overline{\text{RAMP}}$ starts to run up.

Transistor Q663 and Q666 form an operational amplifier. As the current through R660 is diverted into C665, the voltage at the base of Q663 tries to go negative; the voltage at Q663 collector goes positive, decreasing the current through Q666. As the current through Q666 decreases, Q666 emitter goes positive and applies degenerative feedback to the base of Q663. The result is a linear voltage ramp at the emitter of Q666. The VOLTMETER $\overline{\text{RAMP}}$ thus generated is used by the start and stop comparators when making voltage measurements.

The rate of rise of the VOLTMETER $\overline{\text{RAMP}}$ can be changed by enabling either VERT ÷ 1 or VERT ÷2 (P5 pins B and A respectively). As an example, grounding pin A reverse biases transistor Q632, and thereby reverse biases diode D633. With D633 reverse biased, additional current through R634 and R635 is made available for charging timing capacitor C665. Since programming pins A and B simultaneously is not permitted, three choices of ramp rise are available. The three ramps correspond to the "1", "2" and "5" positions of the Volts/Div switch on the vertical plug-in

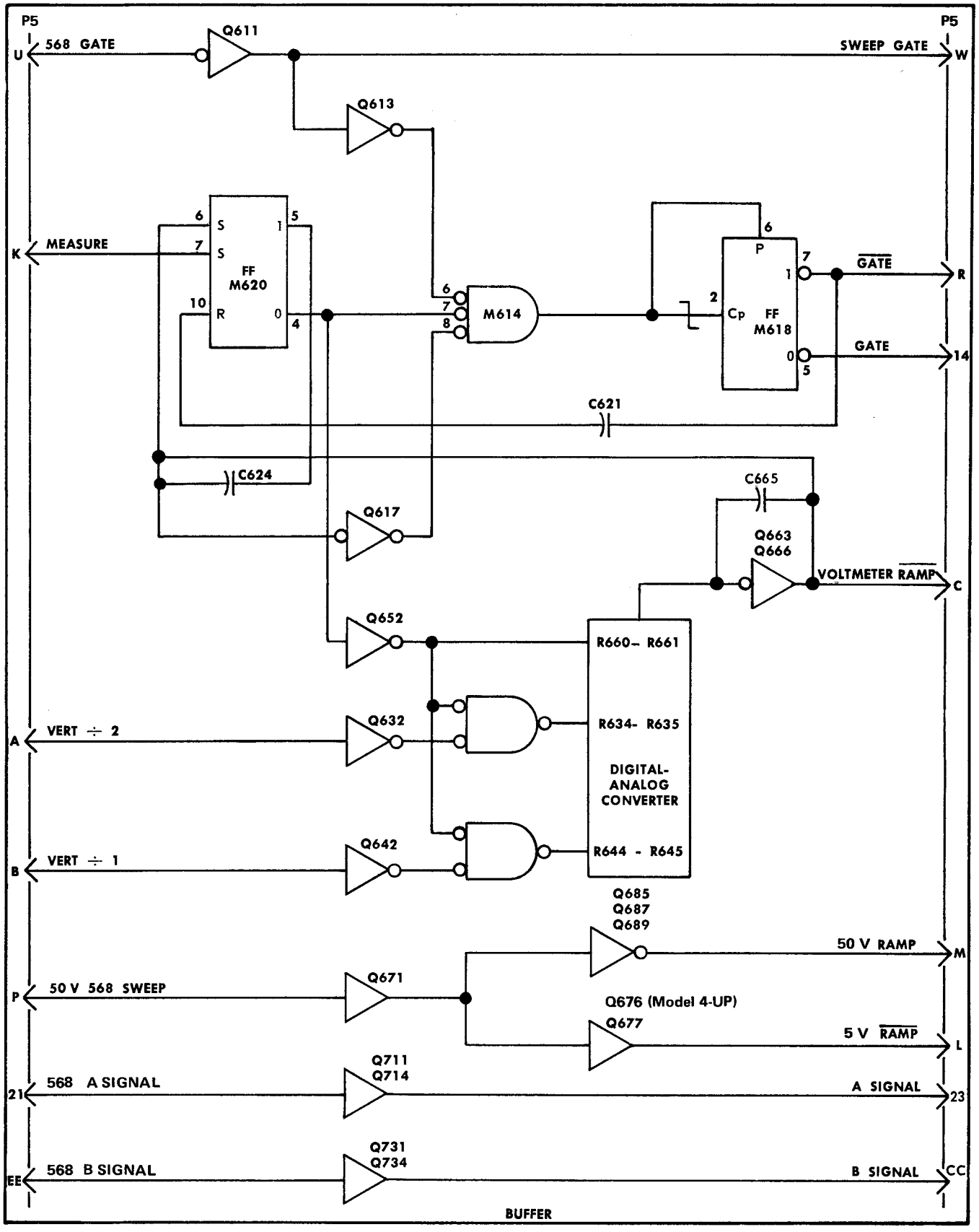


Fig. 4-6. Buffer circuits logic diagram.

unit and are enabled by connecting one of two common lines (A ÷ 1, 2, 5 COMMON or B ÷ 1, 2, 5 COMMON) to P5 pin A or B or leaving both open. Selection of the proper VOLTMETER RAMP can best be understood by looking at a composite of all the circuits related to the voltmeter ramp generator as shown on the simplified voltmeter ramp function foldout diagram in the Diagrams section of this manual. The common line selected by the vertical plug-in unit Volts/Div switch is provided from the CRT Intensification card (P10) in the Type 230, and its logic level depends on the state of NAND gates Q123 and Q113 as controlled by the front-panel MEASUREMENT MODE switch.

When the MEASUREMENT MODE switch is set to B VOLTS, P10 pin 12 (B SIGNAL) on the CRT intensification card is grounded through D524 and the switch, and P10 pin 9 is held low by current through D2051 on the Clock card when P8 pin 7 is grounded through D521 and the MEASUREMENT MODE switch. This results in a low on the B ÷ 1, 2, 5 COMMON line which is then connected by the Channel B Volts/Div switch of the vertical plug-in unit to select the proper VOLTMETER RAMP for the Volts/Div setting. When the Channel B Volts/Div switch is set to one of the "2" positions, P5 pins A and B are both open and the VOLTMETER RAMP rate is 2.5 mV/μs. When the switch is set to one of the "1" positions, P5 pin B (÷1) is held low and the ramp is 5 mV/μs. When the switch is set to one of the "5" positions, P5 pin A (÷2) is held low and the ramp rate is 10 mV/μs.

When the MEASUREMENT MODE switch is set to A VOLTS, P10 pin 9 (VOLTS) is held low by the connection to P8 pin M, but P10 pin 12 (B SIGNAL) is not connected and is therefore high. This results in a low on the A ÷ 1, 2, 5 COMMON line which selects the proper VOLTMETER RAMP to correspond with the deflection factor set by the Channel A Volts /Div switch.

If the MEASUREMENT MODE switch is set to TIME P10 pin 9 is high, causing both ÷ 1, 2, 5 COMMON lines to be high and no lows applied to P5 pin A or B. This is true regardless of the logic level on P10 pin 12, since inhibitor Q103 on the CRT Intensification card applies a low to the inputs of NAND gates Q113 and Q123. In this measurement mode the VOLTMETER RAMP runs in the ÷5 mode during each sweep (when the 568 GATE is low) but the ramp is disconnected in the Type 230 and is not used.

50 V Ramp Inverter (Models 1, 2, 3). The inverter circuit consisting of transistors Q671, Q685, Q687 and Q689 forms a buffer and inverting operational amplifier circuit with a gain of approximately —1. The input is the positive-going 568 SWEEP (50 volts) on P5 pin P. The output is a negative-going 50-volt ramp which is applied to the Zone Generator Circuit card for use in deriving the ZONE pulses.

In operation, the 568 SWEEP ramp is applied through diode D671 to the base of emitter follower Q671. The voltage at the junction of emitter resistors R670 and R672 rises, increasing the conduction through Q687. As the current through Q687 increases, the voltage drop across resistor R685 increases and in turn lowers the base voltage of Q685. Since Q685 is another emitter follower, decreasing its base voltage causes a corresponding decrease in its emitter voltage. Feedback resistor R683 applies negative feedback to the base of Q687 and ensures a linear output, which is taken as 50V RAMP from P5 pin M.

Note that the output of emitter follower Q671 has a voltage divider circuit in its emitter. The voltage at the junction of emitter resistor R672 and R673 is tapped off and applied to the base of transistor Q677, another emitter follower. The output of Q677 is a positive-going ramp of five volts amplitude, the DC level of which is adjustable by resistor R675. This 5V RAMP is applied through P5 pin L to the Start and Stop Comparator circuit cards. On the Comparator cards, the ramp is used as one input to a comparator when offsetting the start or stop point from the sweep start in making time measurements (HORIZ mm FROM SWEEP START).

50 V RAMP Inverter (Model 4-up). In operation, the 568 SWEEP is applied through SW671 and D671 to the base of emitter-follower Q671. A portion of the voltage rise at the emitter of Q671 is taken off at the junction of R672 and R673 and coupled through emitter-followers Q676 and Q677 (see Buffer diagram) to the output at P5 pin L. This positive-going 5V RAMP output is adjusted by R670 (5V RAMP GAIN) to 5 volts for use as a comparison ramp in the start and stop comparators while making time measurements in HORIZ mm FROM SWEEP START mode. Switch SW 671 at the input is used while adjusting the amplitude and DC level of the 5V RAMP output.

The input 568 SWEEP ramp signal is also taken directly from the emitter of Q671 and inverted by Q687, then applied through emitter-follower Q685 to the output at P5 pin M as 50V RAMP, a negative-going ramp to be used by the zone generators. Negative feedback from the output to the base of Q687 ensures a linear output of the ramp. The amplitude of 50V RAMP is adjusted by R680 (50V RAMP GAIN) for proper zone positioning across the CRT.

Vertical Signal Buffers. The vertical signal inputs at P5 pins 21 and EE are applied to two identical operational amplifier circuits, each having an overall gain of 0.5. Since the circuits are identical, only the amplifier for Channel A is described.

The input signal on P5 pin 21 is applied to a voltage divider consisting of resistor R702 in series with the series parallel combination of resistors R704, R705, and R709. The resistance of the series-parallel network is equal to that of R702. The input signal is thus attenuated by one half and is applied to the base of emitter follower Q711. Resistor R716, the emitter load resistor of Q711, is long-tailed to transistor Q714 which functions as an impedance transformer to match a high impedance input to a low impedance output. The attenuation of the input signal is necessary to make the signal levels compatible with the input capabilities of the integrated-circuit comparator on the Start and Stop Comparator circuit cards.

ZONE GENERATOR CIRCUIT CARDS

The two Zone Generator circuit cards generate the time and width-variable 0% and 100% zone memory-gate pulses. The time locations of the four zones are indicated by trace brightening on the Type 568 CRT. The operator has an option of twenty zone positions and four zone widths, all controllable from the front panel or programmable at the appropriate program inputs. The zone positions are variable in 0.5 cm steps; the widths available are 0.3 cm, 2 cm, 4 cm, and 10 cm.

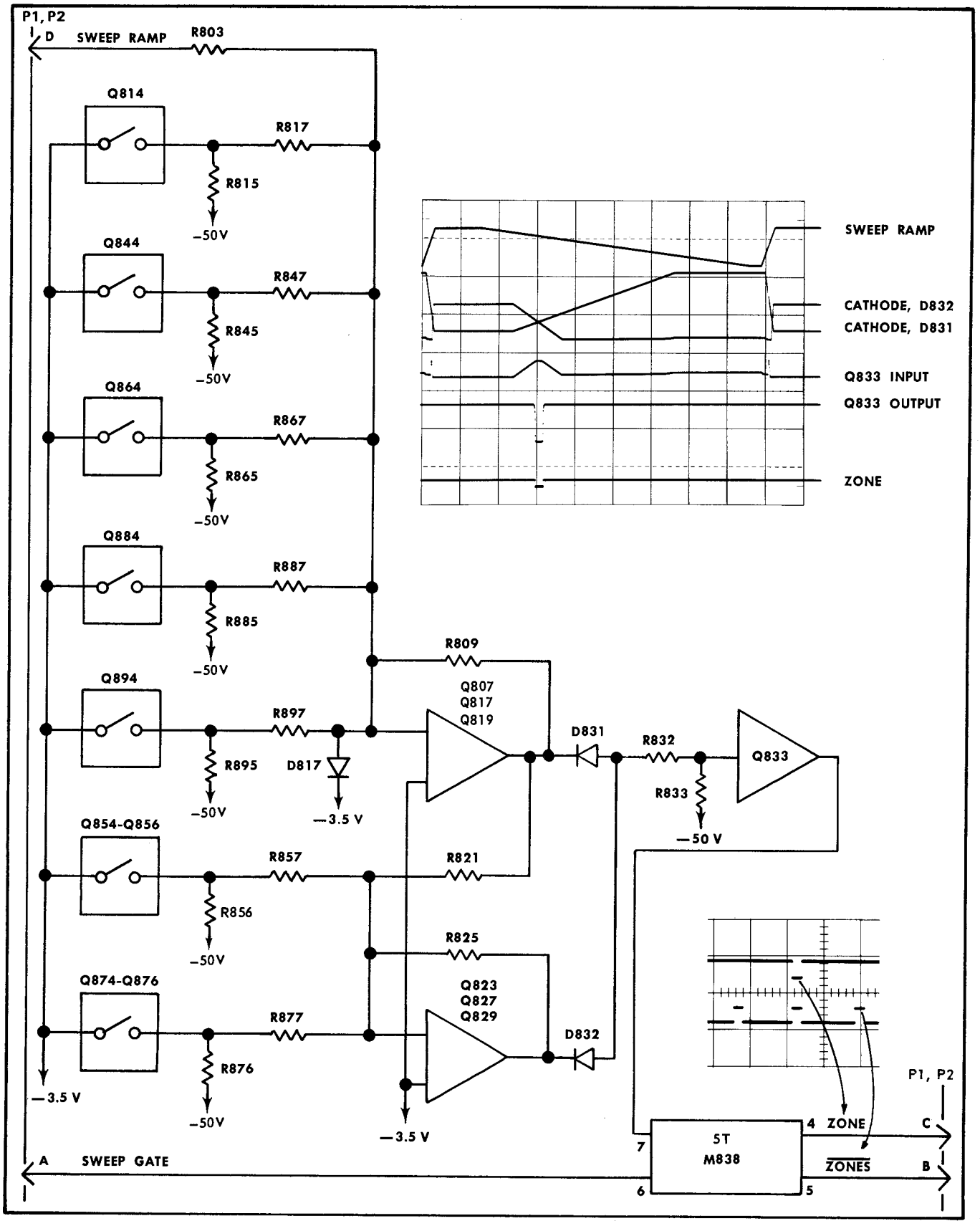


Fig. 4-7. Block diagram showing zone generation.

The intensified memory zones are generated by two identical Zone Generator circuit cards; the "A" Zone Generator circuit card and the "B" Zone Generator circuit card. Each of the two Zone Generator cards contains two zone generator circuits which are identical except for the circuit numbers assigned. Since the four zone generator circuits are alike, only the "A" 0% zone generator is described.

Each zone generator circuit can be further divided into three circuits: the positioning circuit, the width circuit, and the squaring circuit. In the following description, the zone positioning circuitry is explained, then the width circuitry, and finally the generation of the zone pulse by the squaring circuit.

The inputs to the zone generators (see circuit diagram) are the SWEEP GATE pulse and the 50 V RAMP from the Buffer circuit card, and position and width logic inputs controllable from either the front-panel REFERENCE ZONES switches or from the programming connectors. The outputs of each zone generator are (1) ZONE, (2) $\overline{\text{ZONE}}$, (3) AVERAGE, and (4) $\overline{\text{TWELVE}}$. The $\overline{\text{ZONE}}$ output on pin B is applied to the Synchronizer circuit card. The ZONE, AVERAGE, and $\overline{\text{TWELVE}}$ outputs are applied to the Memory circuit cards.

Positioning Circuit

In operation, zone positioning is controlled by applying low levels to the bases of transistors Q814, Q844, Q864, Q884, and Q894. These transistors control the current into the input of an inverting operational amplifier consisting of transistors Q807, Q817, and Q819 and associated circuitry. The current control transistors and operational amplifiers actually make up a digital-to-analog converter, the analog output being taken from the emitter of Q807.

The 50 V RAMP which starts at approximately +50 volts, is applied through R803 to the base of Q817. At the start of the sweep the base of Q817 is clamped at about —3.0 volts by D817. Assuming that all the current control transistors are cut off due to highs on their inputs, the voltage on the emitter of Q807 is about 0 volts. Transistor Q819 is near cutoff due to the conduction of Q817. These are the conditions at the start of the sweep when all the zone positioning inputs are high (positioned at start of sweep).

As the 50 V RAMP starts running down, the decreasing voltage results in decreasing current flow through R803. Clamp diode D817 starts giving up its current to compensate for the decrease in current through R803. With all the current control transistors cut off, D817 soon runs out of current. Transistor Q817 now starts to give up its base current, with the result that its collector current decreases and its collector voltage starts to rise. The rise in Q817 collector voltage increases the drive to Q807 base. Emitter-follower Q807 increases its conduction and the ramp output as its emitter starts to rise (see Fig. 4-7). As the ramp output of Q807 rises, increasing current flow through R809 applies a feedback voltage to the base of Q817 which keeps Q817 from being immediately cut off. Eventually the voltage at the collector of Q817 reaches about +12 volts and Q807 is saturated. With no further increase in feedback available through R809, Q817 is cut off by the falling 50 V RAMP. The voltage at the base of Q817 reaches about —8 volts by the time the sweep ends.

For purpose of further explanation, assume that a low is applied to pin Y or W. (Zone position: 4th centimeter from sweep start). Transistor Q884 saturates and takes all the current flowing through resistor R885. This current is subtracted from the total available at the base of Q817. Diode D817 now conducts harder and makes up most of the current difference necessary to hold Q817 base voltage at —3.5 volts. The increased current flow through D817 increases the voltage drop across the diode slightly and Q817 increases its conduction to the point where the voltage on the emitter of Q807 rests at about —3.5 volts. These are the conditions at the start of the sweep.

As the 50 V RAMP starts running down, the circuit operates as previously explained except that now D817 does not run out of current as soon. The 50 V RAMP must run down much farther before D817 is reverse biased and Q817 starts giving up its base current. The increased distance the 50 V RAMP must run down before the Q807 emitter starts rising represents 4 cm of zone position displacement on the CRT trace. Switching the current control transistors on and off changes the amount of current which D817 must pass and changes the zone position.

When externally programming the Type 230, it is possible to program both the 4 cm and 8 cm position inputs. This is detected by circuit connected to the base of Q899, and Q899 is turned off. The $\overline{\text{TWELVE}}$ signal output of Q899 is applied to pin 27 and thence to the memories. The use of this signal will be described in the memory circuit description.

Width Circuitry

The width circuitry consists of Q823, Q827, Q829, Q833, Q854, Q856, Q874, Q876, D831, and D832. Transistors Q823, Q827, and Q829 form another inverting operational amplifier; Q833 operates as an inverter. For purposes of explanation, assume that the width inputs (pins R, U, M, and N) are high (the zone width is 0.3 cm). Assume also that one or more of the position inputs is low.

At the start of the sweep the voltage at the base of Q827 is resting at about —3.6 volts. Q829 is conducting, which biases Q827 to a collector current of about 1 mA. The conduction of Q827 biases Q823 to where it also passes about 1 mA and the voltage on Q823 emitter is about +2 volts. The voltage at the junction of diodes D831 and D832 is about —2 volts, that at the base of Q833 about —4 volts. Diode D831 is forward biased and conducting; D832 is reverse biased.

When the 50 V RAMP starts running down, nothing happens in the width circuit until D817 runs out of current and the ramp out of Q807 starts running up as previously explained. At the point where Q807 ramp starts to run up, two things start to happen; the forward bias on D831 starts to decrease and the voltage on the base of Q827 tries to move positive. As the base voltage of Q827 starts to rise, Q827 increases its conduction and decreases the bias on Q823 base. Transistor Q823 decreases conduction, Q823 emitter voltage starts to fall, and the falling emitter voltage is coupled through R825 to Q827 base where it opposes the rising ramp voltage.

As the ramp output of Q807 continues to rise the current through D831 decreases toward zero. The voltage at the

base of Q833 starts positive and Q833 is biased into conduction. The rising ramp voltage of Q833 base quickly drives the transistor into saturation and its collector voltage bottoms out at about —3.5 volts. This is the start of the ZONE pulse.

Meanwhile, the ramp voltage on Q823 emitter is running down. When the ramp output of Q823 emitter falls to the point where D832 becomes forward biased, the conduction of D832 starts pulling the Q833 base negative again. Transistor Q833 collector voltage rises rapidly to about +2 volts as Q833 is driven into cutoff. This is the end of the zone pulse. The waveform output of Q833 collector is that of an inverted, truncated triangle whose leading edge is generated from the Q807 emitter ramp and whose trailing edge is generated from the Q823 emitter ramp (see Fig. 4-7).

The zone width is increased from 0.3 cm to 2 cm by applying a low to either pin R or U. A low at either of these inputs biases transistor Q854 into conduction. The conduction of Q854 biases Q856 into cutoff and the current through R856 is now diverted through R857 to R821 and the base of Q827. Transistor Q827 decreases conduction, its collector voltage rises, and the resting voltage at Q823 now emitter rises. Since the negative-going ramp output of Q823 now starts from a higher positive level the time between the point where D831 is reverse biased and the point where D832 becomes forward biased is increased. Transistor Q833 remains in conduction for a period equal to 2 cm of CRT trace.

Note the values of R876 and R856 in the 4 cm and 2 cm width circuits respectively. It can be seen that if 4 cm width is programmed instead of 2 cm, the resting point of Q823 emitter is moved more positive and Q823 emitter ramp must run down from the higher level. The output pulse from Q833 is now 4 cm wide instead of 2 cm. With both the 2 cm and the 4 cm WIDTH inputs low, the resting potential to Q823 emitter is so high that D832 never becomes forward biased before the sweep ends. Once the ZONE pulse moves low, it does not return to the high level until the end of the SWEEP GATE Pulse. Before leaving the width circuits, the function of AND gate diodes D855 and D875 should be noted. If neither the 2 cm width circuit nor the 4 cm width circuit is receiving a low input, both D855 and D875 are reverse biased and the AVERAGE signal output on pin P is low. If either or both of the two width circuits are receiving a low, the corresponding diode(s) is forward biased and the AVERAGE signal is high. The AVERAGE signal output on pin P is used to signal the memory whether an average charge or a peak charge is to be made. This will be discussed again in the Memory circuit card description.

Squaring Circuit

Integrated circuit M838 is used as a Schmitt circuit whose purpose is to square up the pulse output of Q833. Between sweeps the SWEEP GATE input on pin A is high and inhibits M838. At the start of the sweep, pin A goes low and M838 is enabled. When Q833 collector voltage goes negative at the start of a ZONE pulse as previously explained, the circuitry inside M838 changes state. The $\overline{\text{ZONE}}$ output on pin B goes high, the ZONE output on pin C goes low. Switching action is rapid and the pulse shows a square shape. At the end of the negative pulse from Q833, M838 resets. If 10 cm zone width is programmed, M838 is reset by the end of SWEEP GATE. Thus M838 is reset by either the end of the negative pulse from Q833 or the end of SWEEP GATE,whichever occurs first.

MEMORY CIRCUIT CARDS

The Type 230 contains two Memory circuit cards, one for Channel A and one for Channel B. The two cards are identical; each contains a 0% memory circuit and a 100% memory circuit.

The inputs to each Memory circuit card (see circuit diagram) are the 0% ZONE, 100% ZONE, AVERAGE, and $\overline{\text{TWELVE}}$ signals from the Synchronizer circuit card, the signal output of the vertical plug-in unit received via the Buffer circuit card, and the STROBE signal from the Clock circuit card. The outputs from each of the two cards are memory voltage levels corresponding to the signal voltage at the intensified zones and signals that indicate when the memories are properly charged. The memory voltage levels are applied to the Start and Stop Comparator circuit cards for use as one of the reference voltages in each of the two comparators. The memory status signals are sent to the Synchonizer circuit card where they enable a measurement sweep if the memories are properly charged.

0% Memory Circuit

For purposes of explanation, assume that the AVERAGE, $\overline{\text{TWELVE}}$, and STROBE signals are low, that DISCHARGE AND 0% ZONE are high, and that there is a signal present at pin R. Assume also that flipflop M1022 is in the reset state, providing a low state of 0% CHARGED, indicating to the synchronizer that the 0% memory is charged (see Fig. 4-8). Under these conditions the high 0% ZONE signal on NAND gate M1012 pin 7 causes a low on M1012 pin 5. The low on M1012 pin 5 biases transistor Q1015 off, Q1015 collector voltage rises and biases Q1018 off. The high DISCHARGE signal on NAND gate M1020B pin 9 causes its output to go low, biasing transistors Q1031 and Q1036 off. The high 0% ZONE signal from pin A to NAND gates M1040A pin 8 and M1040B pin 9 cause both inputs to NAND gate M1042B (pins 9 and 10) to be low. The output of M1042B goes high and biases transistor Q1046 off. Turning off Q1046 biases transistor Q1053 off also. At this point diodes D1062, D1063, D1065, and D1066 are all reverse biased. The charge on memory capacitor C1063 cannot change under these circumstances.

When the Synchronizer circuit starts a measurement cycle, the memory DISCHARGE pulse is generated by the $\overline{\text{DELAY}}$ pulse and $\overline{\text{GATE}}$. The negative-going DISCHARGE pulse is applied to M1020B pin 9 and the output of M1020B goes high (TWELVE, the other input, is low). The high output of M1020B sets flipflop M1022, causing the output on M1022 pin 5 to go high and the output on pin 4 (Model 4-up) to go low. The high output from M1022 pin 5 goes to the Synchronizer card to indicate that the 0% memory is not charged. In Memory Model 4-up, M1022 Pin 4 is connected to M1040A pin 7. The low at pin 7 enables M1040A to act when 0% ZONE moves low. The high output at M1022 pin 5 also is applied to pin 7 of AND/NAND gate M1026, causing the output at M1026 pin 4 to go high and the output at pin 5 to go low. The low at M1026 pin 5 turns off Q1043, which enables Q1057. The high signal from M1020B pins 4 and 5 is also applied to Q1031, biasing it into con-

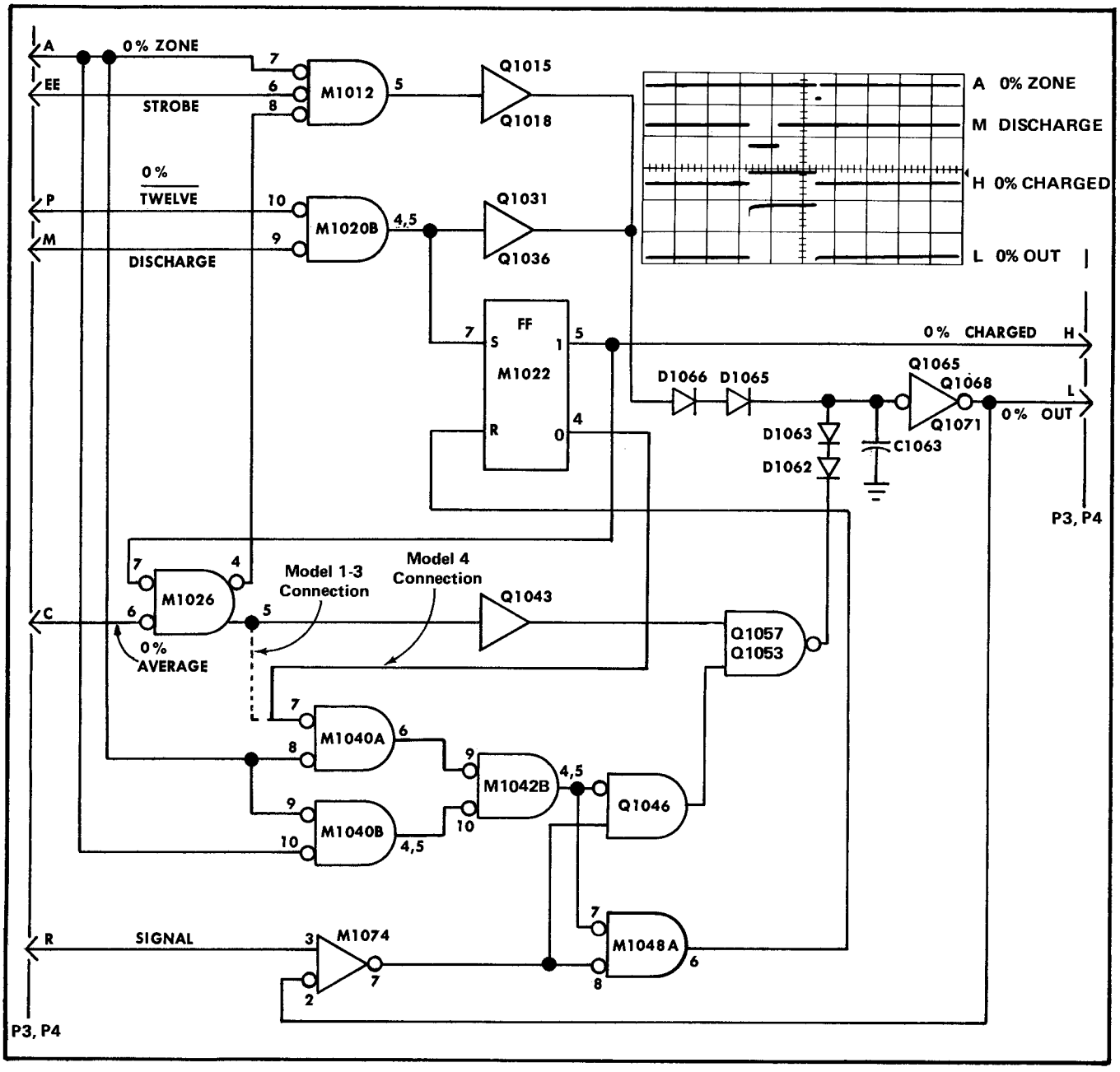


Fig. 4-8. 0% memory circuit logic diagram.

duction. The conduction of Q1031 turns on Q1036, which completes a current path for memory capacitor C1063 through D1065, D1066, and Q1036. Capacitor C1063 now charges to about +6 volts. This is considered to be the discharged state of C1063. As the DISCHARGE pulse ends and again goes high, Q1036 cuts off, disconnecting the discharge path for C1063.

The 0% memory circuit now waits until the 0% ZONE pulse from the Zone generator circuit moves low. The low 0% ZONE pulse is applied to NAND gate M1040B pin 9 and to NAND GATE M1040A pin 8. Since the input to M1040A pin 7 is receiving a low from M1022 pin 4 (Model 4-up), the output at M1040A pin 6 goes high. The high output of M1040A is applied to M1042B pin 9 causing the output at M1024B pins 4 and 5 to go low. The low output from M1042B is connected to M1048A pin 7, permitting M1074 to control the gate via the pin 8 input. The low output of M1042B also is applied to the base of Q1046, and enables the transistor. Thus, the 0% ZONE pulse has enabled the memory charging circuit. Whether the charge in C1063 gets changed or not is now dependent upon the output of the differential comparator, M1074. The low output of M1042B enables input pin 7 of NAND gate M1048A, allowing M1074 to control the gate.

NOTE

In Memory circuit cards Models 1, 2, and 3, pin 7 of M1040A is connected to pin 5 of M1026 instead of M1022 pin 4 as in Model 4 and up. The earlier configuration caused the state of M1040A to be dependent upon the condition of the AVERAGE signal. Models 4-up are no longer dependent upon this condition.

The signal input on pin R is applied to the inverting input (pin 3) of M1074. The memory output is applied via resistor R1073 to the non-inverting input (pin 2). Now, if the voltage across C1063 is greater than the signal voltage, the output of M1074 goes positive and turns on Q1046 through resistor R1046. The conduction of Q1046 biases Q1053 into conduction, closing the charge path from −3.5 volts through Q1057, Q1053, D1062, D1063 and R1063. High current through this path very quickly reduces the positive charge in C1063 and the memory output follows the change in C1063 voltage. When the voltage across C1063 reaches the signal input voltage, M1074 pin 7 immediately goes low and cuts off Q1046. The voltage across C1063 is now a close approximation of the signal voltage at this instant (the beginning of the 0% ZONE). The low output of M1074 pin 7 activates NAND gate M1048A, M1048A resets flipflop M1022, and M1022 sends a signal (via pin H) to the Synchronizer circuit that the 0% memory is charged.

Switching M1022 also applies a low to M1026 pin 7. The output on M1026 pin goes high (AVERAGE is assumed to be low). The output of M1026 pin 4 is applied through resistor R1011 to M1012 pin 8. Since both 0% ZONE and STROBE are already low, the output of M1012 pin 5 goes high after about 1 microsecond of delay caused by R1011 and C1011. The high output from M1012 pin 5 biases on transistors Q1015 and Q1018. A small amount of current now flows through the path consisting of R1063, D1065, D1066, Q1018, and R1018, pulling the voltage on C1063 positive.

In Model 4-up, pin 4 output of M1022 goes high, and after about 1 microsecond of delay caused by R1041 and C1041, M1040A pin 7 goes high and output pin 6 goes low, enabling pin 9 of NAND gate M1042B. The high output on M1026 pin 5 is applied through R1042 to the base of Q1043, causing Q1043 to conduct and Q1057 to cut off.

In Models 1-3, the high output of M1026 pin 5 is applied through R1041 to M1040A pin 7 and to Q1043 base. After about one microsecond delay caused by R1041 and C1041, Q1043 is biased into conduction and cuts off Q1057. The high also causes that output of M1040A pin 6 to go low, enabling M1042B pin 9. Since both 0% ZONE and STROBE are low, the output of M1040B is high and causes the output of M1042B to be low. The output of M1042B is applied as enabling bias to Q1046 base.

As the current through Q1018 pulls the voltage on C1063 positive, the 0% memory output voltage rises also (all models). When the 0% memory output voltage equals the signal voltage, M1074 switches and its output on M1074 pin 7 goes high. The high from M1074 pin 7 is applied to Q1046 emitter and Q1046 now conducts and biases Q1053 on. The conduction of Q1053 through R1059 starts pulling the voltage on C1063 slowly negative again. Differential comparator M1074 now switches rapidly back and forth, constantly balancing the voltage on C1063 with the signal voltage. Flipflop M1022 continues to send a 0% memory charged signal to the synchronizer, since it does not set again until DISCHARGE occurs.

At the end of the 0% ZONE pulse, M1012 pin 7 goes high, M1012 pin 5 goes low, transistor Q1015 turns off, and the path from C1063 to the +50-volt supply opens. The input to M1040B pin 9 and M1040A pin 8 goes high and both NAND gates deliver low outputs. NAND gate M1042B now delivers a high on its output pins 4 and 5 and applies cutoff bias to the base of Q1046. Turning off Q1046 biases Q1053 off also, opening the path from C1063 to the −50-volt supply. Memory capacitor C1063 is now disconnected from any charge or discharge path and retains its charge until the DISCHARGE pulse or another 0% ZONE pulse occurs.

At the start of the foregoing description it was assumed that STROBE remained low. The assumption was made in order to simplify the explanation. In actual practice, the only time that STROBE remains low is when the Type 3B2 is used as the horizontal plug-in unit. At clock rates of 100 kHz and below, as in equivalent-time sampling, the STROBE pulse is delayed for about two microseconds following each clock pulse, then is low for a period of about six microseconds.

Strobing the memories with 6 μs pulses provides for better averaging. Without strobing, it would be possible for the memories to contain a voltage representing a noise spike or misplaced sample at the time ZONE goes high. With strobing, the memory voltage is permitted to move 10 mV during each 6 μs strobe pulse, thus averaging out misplaced samples or noise spikes. The fact that STROBE is switching between high and low does not invalidate the foregoing explanation; the action is merely broken up into 6 μs periods as the STROBE pulses switch NAND gates M1012 and M1040B.

Likewise in the description it was assumed that $\overline{\text{TWELVE}}$ was low. This is always so in front-panel operation. With $\overline{\text{TWELVE}}$ low, the memories are discharged at the beginning of each memory sweep. However, when making programmed measurements, it is frequently advantageous to discharge the memories, charge them during the zones, then make a whole series of voltage and time measurements before again discharging the memories. This saves the time normally spent on first discharging, then charging, the memories on separate memory sweeps for each measurement. As an example, after making a memory charging sweep, it is possible to program a measurement series consisting of A volts, B volts, A risetime, B risetime, Time between A and B, and so on.

When programming the $\overline{\text{TWELVE}}$ function, certain other program inputs and conditions are required also. These are as follows:

1. The Type 230 must be set for triggered measurement and must receive a trigger from the readout equipment or other source.

2. The time-base unit must be synchronized with the Type 230. This can be accomplished by programming HIGH SPEED.

3. The series of measurements must be made on a repetitive input waveform (or waveforms when using both A and B channels).

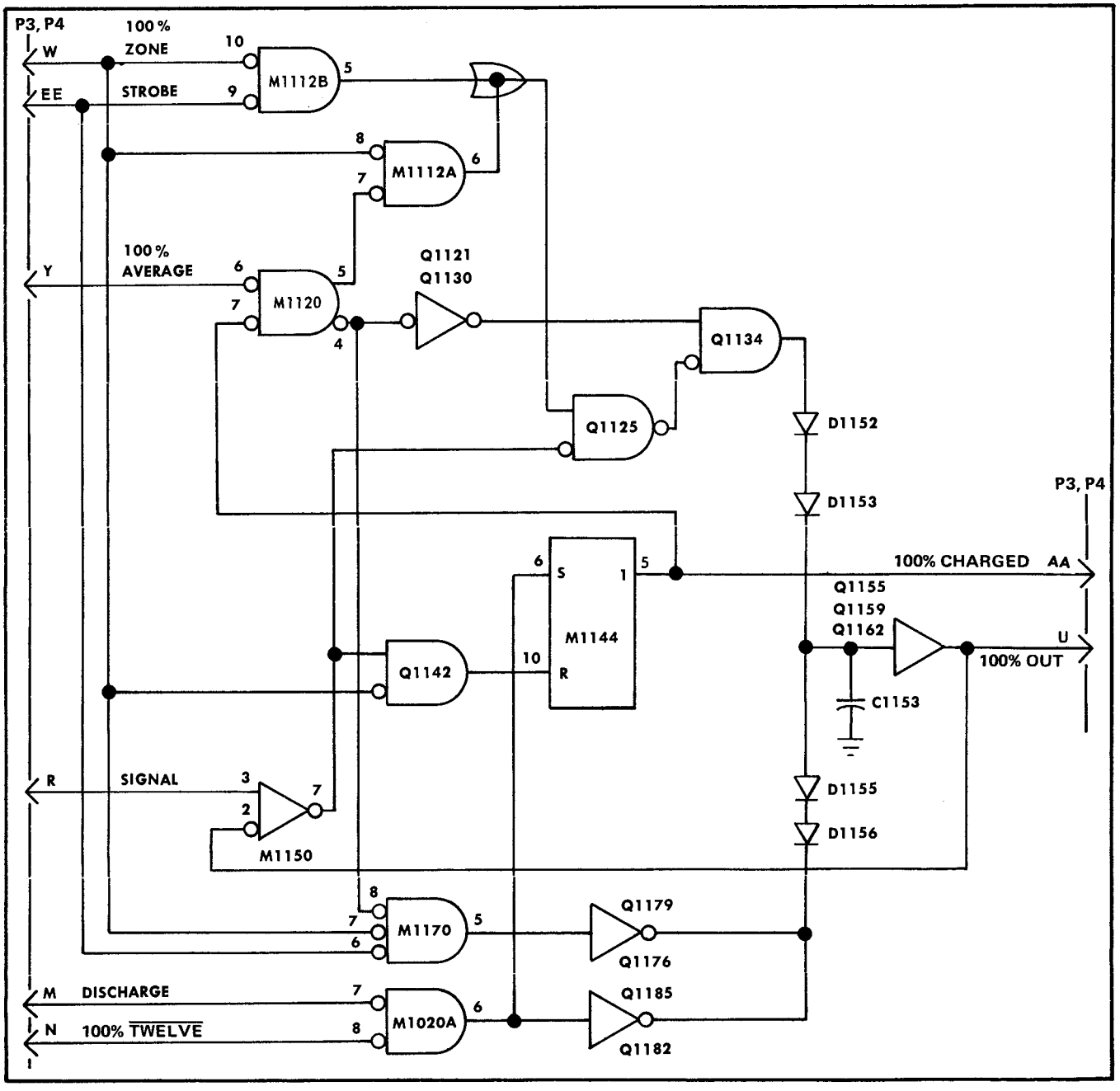


Fig. 4-9. 100% memory circuit logic diagram.

4. The first measurement in the series should be made before TWELVE is programmed.

5. The vertical sensitivity, offset, trace position and signal must remain the same throughout the measurement series. For further information concerning the programming of the TWELVE function, see the Programming section of this manual.

Operation of the Type 230 in any of the peak modes causes AVERAGE to go high. The 0% memory changes its operation as explained in the following paragraphs.

The high AVERAGE signal applied to M1026 pin 6 causes a high output at M1026 pin 4. The high from M1026 pin 4 to M1012 pin 8 inhibits M1012, turning off Q1015 and Q1018. Current flow through Q1036 provides discharge current for C1063 during DISCHARGE time.

In Models 1 through 3, the high AVERAGE signal applied to M1026 pin 6 causes the output of M1026 pin 5 to go low, enabling M1040A pin 7. The other input, M1040A pin 8, is activated by the now widened 0% ZONE pulse (ZONE is widened because of the uncertainty as to where the peak signal actually occurs). The low output of M1026 pin 5

also biases Q1043 and Q1057 into conduction, providing additional current to charge C1063 at a faster rate.

In Model 4-up, the low output at M1022 pin 4 enables pin 7 of M1040A. The other input, M1040A pin 8, is activated by the now widened 0% ZONE pulse (ZONE is widened because of the uncertainty as to where the peak signal actually occurs). The high AVERAGE signal applied to M1026 pin 6 causes the output of M1026 to go low, turning off transistor Q1043 and enabling the base of Q1057.

The 0% memory circuit (all models) is now able to follow rapid negative increases in signal level, but since Q1018 is biased off, positive-going excursions of the signal are ignored. The 0% memory circuit output now represents the most negative peak that occurs during the low state of 0% ZONE.

100% Memory Circuit

The 100% memory circuit is similar in operation to the 0% memory circuit except that where the 0% memory capacitor is discharged positively to +6 volts and charged to +2 volts (with the trace centered), the 100% memory capacitor is discharged to −2 volts and charged to +2 volts. The reason for the circuit differences between the two memories is that 0% memory must charge quickly in the negative direction while the 100% memory must charge positive rapidly, when in peak mode.

For purposes of explanation, assume that 100% AVERAGE, STROBE, and $\overline{\text{TWELVE}}$ are low (see circuit diagram). Assume also that the 100% ZONE and DISCHARGE inputs are high and that a signal is applied to pin R. Under these conditions the high 100% ZONE signal on NAND gate M1112B pin 10 causes a low on M1112B pin 5. The low on M1112B pin 5 is applied through a phantom OR gate (see Fig. 4-9) to the base of transistor Q1125, biasing it off. Turning off Q1125 biases off transistor Q1134 and thereby reverse biases diodes D1152 and D1153. The high 100% DISCHARGE signal on NAND gate M1020A pin 7 causes a low output on M1020A pin 6, biasing off transistors Q1182 and Q1185. Diodes D1155 and D1156 are consequently reverse biased by the path through resistor R1178 to +50 volts. With D1152, D1153, D1155, and D1156 all reverse biased, the charge on memory capacitor C1153 cannot change.

The negative-going DISCHARGE pulse is applied to M1020A pin 7. The 100% $\overline{\text{TWELVE}}$ signal at M1020A pin 8 is also low, so the output on C1020A pin 6 goes high. The high output of M1020A pin 6 sets flipflop M1144 and the output on M1144 pin 5 goes high. The high output of M1144 pin 5 is applied to the Synchronizer card and signals that the 100% memory is not charged. The high signal from M1020A also biases Q1182 and Q1185 into conduction, discharging C1153 to −2 volts. This is the discharged state of the 100% memory capacitor. As the DISCHARGE pulse ends and again goes high, M1020A pin 6 goes low, cutting off Q1182 and Q1185 and disconnecting the discharge path for C1153.

The 100% memory circuit now waits until the 100% ZONE pulse from the Zone generator circuit card arrives at pin W. The negative-going 100% ZONE pulse is applied to NAND gate M1112B pin 10. With both inputs low, M1112B pin 5 goes high and turns on transistors Q1125 and Q1134. The high output of flipflop M1144 pin 5 causes AND/NAND gate M1120 pin 4 to go high and turn on transistors Q1121 and Q1130. The current flow through Q1134 and Q1130 forward biases D1152 and D1153 and applies a heavy charge current to C1153. As the voltage across C1153 quickly goes positive, the operational amplifier consisting of Q1155, Q1159 and Q1162 follows the change and delivers a positive-going signal to differential comparator M1150 pin 2. When the memory output voltage equals the signal voltage, M1150 switches and applies a high to Q1125 emitter, cutting it off. The high output of M1150 pin 7 is also applied to Q1152 emitter. With 100% ZONE low, Q1142 turns on and switches flipflop M1144 via M1144 pin 10. The output M1144 pin 5 goes low, signaling the Synchronizer card that the 100% memory is charged. The voltage in C1153 is now a close approximation of the signal voltage at this instant (the beginning of the 100% ZONE).

Switching M1144 also applies a low to M1120 pin 7. The output on M1120 pin 4 goes low and turns off transistors Q1121 and Q1130, opening the high-current charge path to C1153. The low output on M1120 pin 4 is also applied to M1170 pin 8. The input to M1170 pin 7 is the 100% ZONE pulse, the input to pin 6 is the STROBE signal. The output of M1170 pin 5 now goes high and low at the STROBE rate, turning Q1176 and Q1179 off and on. Turning the two transistors off and on starts removing the charge from C1153. When the charge on C1153 falls slightly below the signal level, M1150 switches and turns Q1125 back on. Turning on Q1125 again biases Q1134 back into conduction and starts recharging C1153. The charging current is turned off and on in accordance with the STROBE signal applied to M112B pin 9. When the charge in C1153 again exceeds the signal voltage, M1150 once again switches and starts the discharge process. The switching of M1150 is very rapid and the charge on C1153 is held very close to the signal level for the duration of the 100% ZONE pulse.

Operation of the Type 230 in any of the peak modes causes AVERAGE to go high as previously explained. The 100% memory changes its operation as explained in the following paragraphs.

The high AVERAGE signal applied to M1120 pin 6 causes a high output at M1120 pin 4. The high from M1120 pin 4 to Q1121 base turns on Q1121 and Q1130. The conduction of Q1121 and Q1130 provides additional current through Q1134 to charge C1153. The high from M1120 pin 4 is also applied to M1170 pin 8. The output on M1170 pin 5 goes low and biases Q1176 and Q1179 off, opening the discharge path for C1153. With the charge path controlled by the operation of M1150, M1120, M1112B, Q1121, Q1130, Q1125, and Q1134, the memory circuit is now able to follow rapid increases in signal level. However, with Q1176 and Q1182 cut off, decreases in signal level are ignored. The memory circuit output now represents the highest peak that occurs during the 100% ZONE pulse. As in the case of the 0% memory, the 100% ZONE pulse is widened because of the uncertainty as to where the peak signal actually occurs.

Operation of the 100% memory circuit with $\overline{\text{TWELVE}}$ programmed high is similar to the operation of the 0% Memory circuit with similar programming. The $\overline{\text{TWELVE}}$ signal is programmed high before the second measurement and causes the output of M1020A pin 6 to remain low, disabling the path for the DISCHARGE signal.

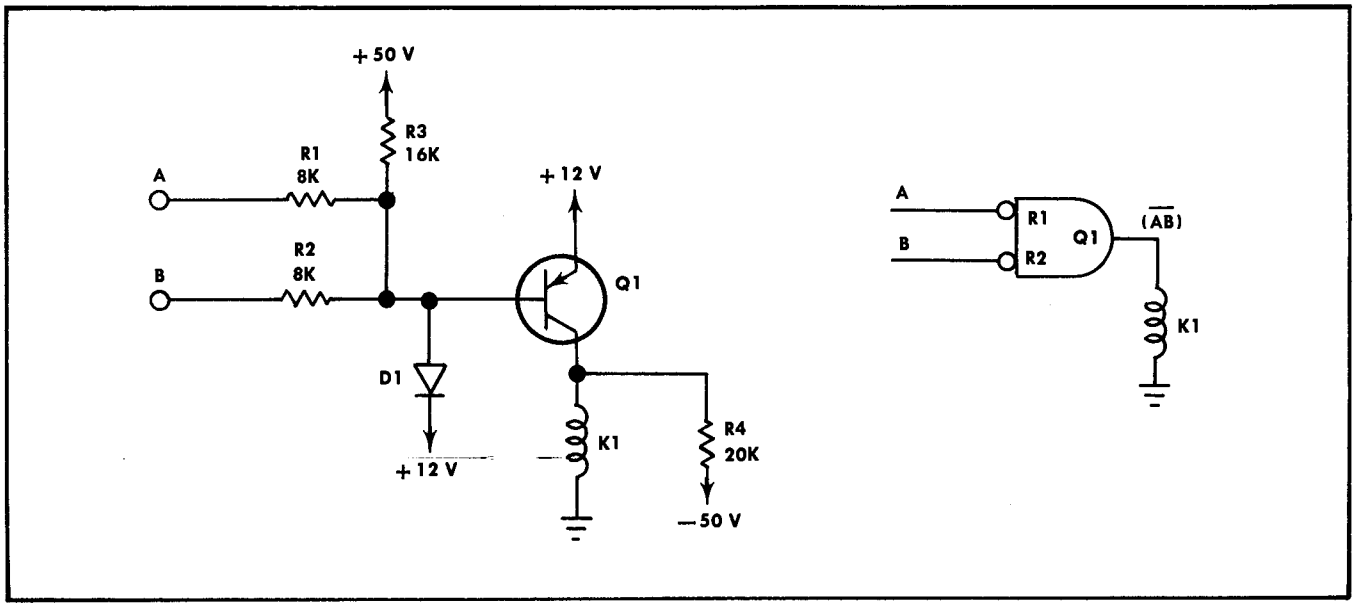


Fig. 4-10. Basic RTL circuit and logic symbol.

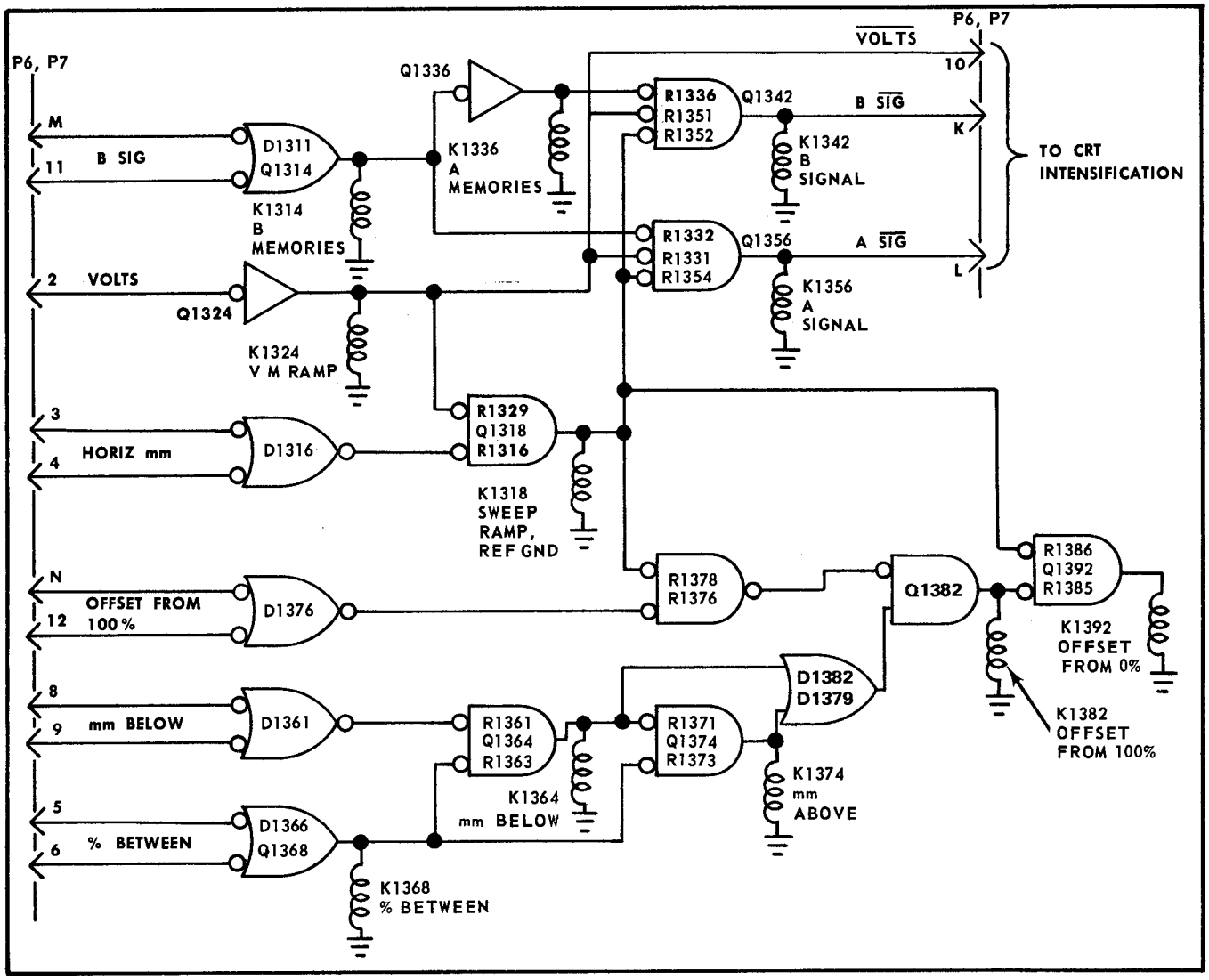


Fig. 4-11. Comparator function logic diagram.

START AND STOP COMPARATORS

The Type 230 has two Comparator cards, a start comparator for (P6) and a stop comparator (P7). As described previously, the function of these cards is to gate the clock on and off when appropriate logic levels and signals are received. Reed switches on the cards are controlled from the front-panel on the Type 230 or via rear-panel programming. Since the two cards are identical both physically and electrically, only the switching logic of the start comparator will be explained in detail. Operation of the offset generator section will be described for both cards to explain the various measurement modes.

The comparator circuitry may be separated into three major sections: the differential comparator, M1472; the function logic section, Q1314 through Q1392; and the offset generator section, Q1421A through Q1472 and Q1513 through Q1583 (see circuit diagrams).

Differential Comparator

The output function of the comparator card is provided by differential comparator M1472, an integrated circuit device. Comparison is made between a selected reference level and a selected input or ramp signal to generate the start (or stop) of the measurement. The reference level is either ground or one of the four memory outputs, or a selected offset from one of these. The signal for comparison may be either A SIGNAL, B SIGNAL, the VOLTMETER $\overline{\text{RAMP}}$ or the 5V $\overline{\text{RAMP}}$. These signals all come from the Buffer card. The maximum usable amplitude of either ramp signal out of the Buffer card is +5 volts. The level of A signal or B signal will normally be between ground and +5 volts.

When the voltage on the positive-going transition of the selected input signal matches the selected comparison voltage, differential comparator M1472 fires, sending a negative-going step through P6 pin 7 to be used for gating the clock circuit. When the signal voltage again returns below the comparison level, the comparator resets to its ready state.

Function Logic Section

The function logic circuitry consists primarily of resistor-transistor logic gates (RTL)[1] which control the relays that select the comparison level and the signal to be applied to the differential comparator. A basic resistor-transistor NAND gate is illustrated in Fig. 4-10. Input resistors R1 and R2 form part of the voltage divider that determines the state of the gate. A ground closure at either A or B is considered a logical one (low). When no ones (lows) are present at A or B, diode D1 clamps the base of transistor Q1 at approximately +12.6 volts. This voltage holds Q1 in cutoff with its emitter-base junction reverse biased.

If only resistor R1 were grounded through the A input, the voltage at the base of Q1 would still not be below the clamp voltage of D1, and Q1 would remain cut off. The same would occur if only resistor R2 were grounded through input B. If both A and B were grounded, however, current through R1 and R2 would be sufficient to drop the base voltage of Q1 and bias the transistor into conduction. With Q1 turned on, relay K1 is energized, and provides the activated function of NAND gate R1-R2-Q1.

Fig 4-11 is a logic diagram of the function logic section of the Comparator card. The way this logic relates to the selection of the signal and the comparison level may be seen in Fig. 4-12.

Either mm or % from the memory level may be selected for the comparison reference when A or B SIGNAL or the VOLTMETER $\overline{\text{RAMP}}$ is used for the comparison signal. When the SWEEP $\overline{\text{RAMP}}$ is used for comparison, only mm may be selected as the reference by the function logic. See Table 4-1 for the logic used in the various measurement modes.

B Signal

The logic lines that program B SIGNAL (and A $\overline{\text{SIGNAL}}$) enter the Comparator card at pins 11 and M. Pin M is the external program input from J202; pin 11 is the internal program input from the MEASUREMENT MODE selector on the front panel of the Type 230. These two inputs form a NOR gate with transistor Q1314. When either pin M or pin 11 is low, the output of the B Memories NOR gate (at the collector of Q1314) is high, energizing relay K1314 which selects the B 0% and 100% memories for setting the comparison level reference. The high at the output of the B Memories NOR gate is also applied to the A memory inverter (Q1336) and to one input of the three-input A Signal NAND gate (R1332-R1331-R1354-R1356). The high at the base of Q1336 holds that transistor in the non-conduction state, inhibiting relay K1336 to prevent any comparison being made with the A 0% or 100% memories. The low at the output of the A memory inverter (Q1336) enables one input of the three-input B Signal NAND gate (R1336-R1351, R1352-Q1342). For the purpose of this discussion, assume that the levels at P6 pins 2, 3 and 4 (VOLTS and HORIZ mm) are all high, causing the second and third inputs of the B Signal NAND gate to be enabled (low). With all three inputs low, the output of this NAND gate is high and relay K1342 is energized, selecting the B input signal for the comparison signal. Even though two of the inputs to the A Signal NAND gate (R1332-R1331-R1354-Q1356) are low, being connected in parallel with two inputs of the B Signal NAND gate, the A Signal NAND gate is inhibited by the high third input from the B Memories NOR gate. With the A Signal NAND gate inhibited, K1356 is not energized and the A signal is not connected. The outputs of the B Signal and A Signal NAND gates are also applied to the CRT intensification circuit through P6 pins K and L to permit intensification of the trace during the measurement period if other circuits are programmed for intensification.

When the HORIZ mm and VOLTS inputs are high, as previously assumed, if both B SIGNAL logic inputs (P6 pins 11 and M) are also high, the B memories and B signal will be inhibited by the B Memories NOR gate and the B Signal NAND gate, respectively, and the A memories and A signal will be activated by the A memories inverter and A Signal NAND gate, respectively. Under these conditions the A signal will be applied to one side of the differential comparator (M1472) and the A 0% and/or 100% memories (depending on measurement mode) will determine the reference level at the other side of the comparator.

[1] **An explanation of RTL logic gates may be found in the text: Digital Computer Fundamentals, Thomas C. Bartee, McGraw-Hill, 1966, pp. 108-110.**

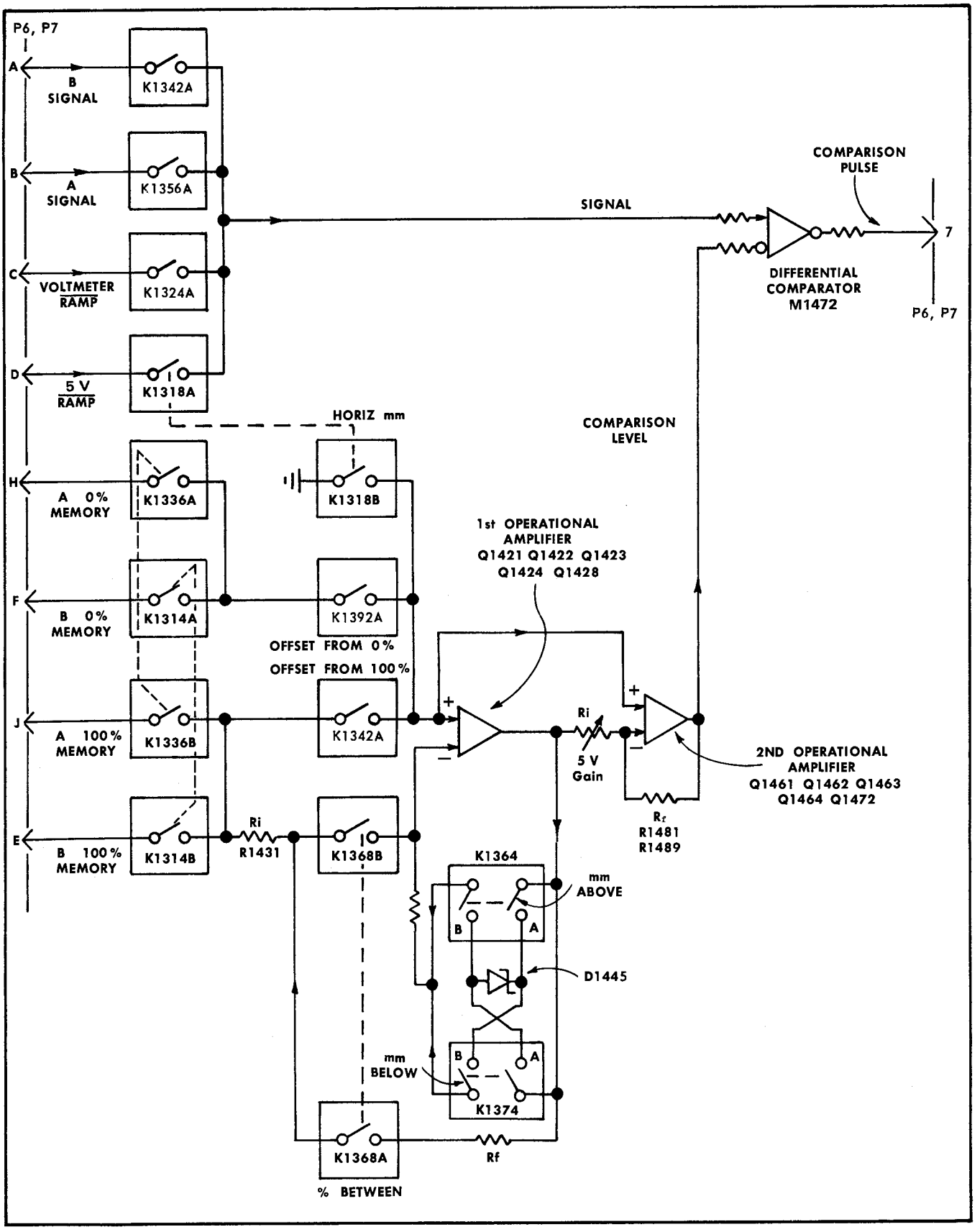


Fig. 4-12. Comparator signal and reference level selection.

TABLE 4-1

Function Logic for Various Measurement Modes

	K1342 B SIGNAL	K1356 A SIGNAL	K1324 VOLTMETER RAMP	K1318A SWEEP RAMP K1318B REF. GROUND	K1336 A MEMORIES	K1314 B MEMORIES	K1368 % BETWEEN	K1374 mm ABOVE	K1364 mm BELOW	K1392 OFFSET FROM 0%	K1382 OFFSET FROM 100%
A VOLTS	0	0	1	0	1	0	ϕ	ϕ	ϕ	ϕ	ϕ
B VOLTS	0	0	1	0	0	1	ϕ	ϕ	ϕ	ϕ	ϕ
A% Between Zones	0	1	0	0	1	0	1	0	0	1	0
B% Between Zones	1	0	0	0	0	1	1	0	0	1	0
A mm Above 0%	0	1	0	0	1	0	0	1	0	1	0
A mm Below 0%	0	1	0	0	1	0	0	0	1	1	0
B mm Above 0%	1	0	0	0	0	1	0	1	0	1	0
B mm Below 0%	1	0	0	0	0	1	0	0	1	1	0
A mm Above 100%	0	1	0	0	1	0	0	1	0	0	1
A mm Below 100%	0	1	0	0	1	0	0	0	1	0	1
B mm Above 100%	1	0	0	0	0	1	0	1	0	0	1
B mm Below 100%	1	0	0	0	0	1	0	0	1	0	1
Horiz mm From Sweep Start	0	0	0	1	0	0	0	ϕ	ϕ	0	0

0—Open

1—Closed

ϕ—Don't Care. Reed may be open or closed, depending on other program information.

Volts

The VOLTS program from either the external program input or the MEASUREMENT MODE switch enters the Comparator card at P6 pin 2. The external input is directly from 201 pin 8. For internal operation, P6 pin 2 and P7 pin 2 are held low by current through D2051 on the Clock card when P8 pin 7 is grounded through D521 and the MEASUREMENT MODE switch. (See the fold-out Simplified Voltmeter Ramp Function diagram in the Diagrams section of this manual.) Q1324 inverts the input VOLTS level to $\overline{\text{VOLTS}}$. When the voltage at pin 2 is low, the high output of the inverter energizes relay K1324, connecting the VOLTMETER $\overline{\text{RAMP}}$ to the signal side of the differential comparator. The high output of Q1324 also inhibits the functions of the B Signal, A Signal and Sweep Ramp NAND gates, preventing any of these signals from being connected to the differential comparator.

When the voltage at pin 2 is high, the VOLTMETER $\overline{\text{RAMP}}$ is inhibited from being connected to the differential comparator. In this case, Q1324 does not inhibit either the SWEEP $\overline{\text{RAMP}}$, A SIGNAL or B SIGNAL.

Horiz mm

HORIZ mm enters the Comparator card at P6 pins 3 and 4. Pin 4 is the input from external program connector J202; pin 3 is the internal input from the TIME MEASUREMENT START POINT (or STOP POINT) switch on the front panel of the Type 230. These two inputs form the Horiz mm OR gate which controls one input of the Sweep Ramp NAND gate (R1316-R1329-Q1318). When the VOLTS program at P6 pin 2 is high and the HORIZ mm program at P6 pin 3 or 4 is low, the output of the Sweep Ramp NAND gate is high, energizing relay K1318. When K1318 is energized it connects the SWEEP RAMP to one side of differential comparator M1472 and connects ground as reference to the offset generator.

The output of the Sweep Ramp NAND gate is also connected to one input of the Offset from 100% NAND gate (R1376-R1378) and one input of the Offset from 0% NAND gate (R1386-R1385-Q1392). When the SWEEP RAMP is enabled by K1318, the high inputs to the Offset from 0% and the Offset from 100% gates inhibit the offset generator from comparing against the 0% or 100% memories of either channel. As mentioned earlier, the B Signal and A Signal NAND gates are also inhibited when the Sweep Ramp NAND gate output is high.

Offset from 100%; Offset from 0%

The Offset from 100% OR gate consists of program inputs P6 pins N and 12. Pin N is the external programming

input; pin 12 is from the front panel TIME MEASUREMENT START POINT (or STOP POINT) switch. The output of this OR gate is applied to the Offset from 100% AND gate composed of resistors R1378 and R1376. For this AND gate to function the output of the Offset from 100% OR gate and the output from the Sweep Ramp NAND gate must both be low. This is the case when Offset from 100% is programmed. The low output from the Offset from 100% AND gate is then sent to the base of inhibitor transistor Q1382. The emitter of Q1382 is controlled by the output of the mm Below NAND gate and mm Above NAND gate (to be described later). The output of the inhibitor controls the Offset from 100% relay K1382. In order for K1382 to be energized, the inhibitor emitter must be high. When K1382 is energized, the offset generator is referenced to the 100% memory (A or B, whichever is selected). The inhibitor output is also applied to one input of the Offset from 0% NAND gate (R1386-R1385-Q1392). If relay K1318 (Sweep Ramp) and relay K1382 (Offset from 100%) are not energized, the two lows applied to the Offset from 0% NAND gate activate the gate, energizing relay K1392. This causes the offset generator to be referenced to the 0% memory (A or B, whichever is selected).

mm Below and mm Above

The internal and external program inputs for mm Below (and mm Above) enter the comparator card at P6 pins 8 and 9, respectively. Internal programming is selected by the TIME MEASUREMENT START POINT (or STOP POINT) switch. These two inputs form the mm Below OR gate which controls one input of the mm Below NAND gate (R1361-R1363-Q1364). The other input to this NAND gate is controlled by the % Between NOR gate (Q1368). If both inputs to the mm Below NAND gate are low (mm Below activated, % Between inhibited), the output of the NAND gate is high, energizing relay K1364. When K1364 is energized, the offset generator provides offset below the selected reference in mm increments on the CRT display. The output of this NAND gate, when high, also inhibits one input of the mm Above NAND gate, (R1371-R1373-Q1374), preventing it from energizing relay K1374 (mm Above). If both inputs to the mm Above NAND gate are low (mm Below and % Between inhibited), the output of the NAND gate is high, energizing K1374 to provide offset above the selected reference in mm increments on the CRT display.

% Between

The program lines for % Between enter the Comparator card at P6 pins 6 and 5 respectively, for the internal and external inputs. The front-panel TIME MEASUREMENT START POINT (or STOP POINT) switch selects this mode internally. These two inputs and transistor Q1368 form the % Between NOR gate which controls relay K1368 (% Between) and one input each of the mm Above and mm Below NAND gates, as mentioned before. When either of the two inputs to the % Between NOR gate is true (low), K1368 is energized and the comparison voltage to be applied to the differential comparator will be some selected percentage of the voltage between the 0% and 100% zones (A or B, as selected). The high output of the % Between NOR gate also inhibits both the mm Below and mm Above functions, which in turn inhibit the Offset from 100% and Offset from 0% functions.

Program Logic

The following table shows the program inputs required to be true to energize any particular relay of the function logic:

Relay	Function	Program Lines Low to Energize Relay (Lines not mentioned are high)
K1356	A Signal	None
K1342	B Signal	11 or M
K1324	Voltmeter Ramp	2
K1318	Sweep Ramp	3 or 4
K1336	A Memories	None
K1314	B Memories	11 or M
K1368	% Between	5 or 6
K1364	mm Below	8 or 9
K1374	mm Above	None
K1392	Offset From 0%	None
K1382	Offset From 100%	12 or N

Notice that when no inputs are programmed low, the function logic will select A Signal and Offset mm Above the 0% zone.

Offset Generator

The offset generator, which consists of two operational amplifiers, provides voltage offset (% or mm) from the selected reference level for comparison with the selected signal. The reference (ground or one of the memory levels) is applied to two or more inputs of the operational amplifiers, depending on the measurement mode (see Fig. 4-13 and 4-15 through 17). The offset gain logic (Fig. 4-14) programs the feedback resistance of the second operational amplifier to set the amount of offset from the reference.

Percent Between Zones

General. The first operational amplifier of the offset generator consists of Q1421B, Q1421A, Q1424, Q1422, and Q1428. When the Type 230 is set for one of the % Between Zones modes, K1392 and K1368A and B are closed, connecting the 0% memory level (either A or B, as selected to the + input of both operational amplifiers (bases of Q1421A and Q1461B), and the 100% memory level of the same channel to the — input of the first amplifier. In this mode, the input resistance (R_i) to amplifier 1 is R1431 and the feedback resistance (R_f) from the amplifier output to the — input is composed of R1433, R1434 and R1435. The gain of this amplifier is adjusted with R1435 (to about 1.24) so that at the input 5-volt (maximum) difference between memory levels will be amplified to match the approximate 6.2-volt zener diode reference voltage used in the offset mm modes. Transistor Q1423 provides constant current for the amplifier. The voltage level at the collector of Q1421A is proportional to the difference between the 0% memory level at the base of Q1421A and the 100% memory level applied to the base of Q1421B. Emitter follower Q1422 connects this voltage to output transistor Q1428, which amplifies the voltage and inverts it.

Offset Gain Logic. The output of the first operational amplifier is applied through input resistors R1455, R1456, and

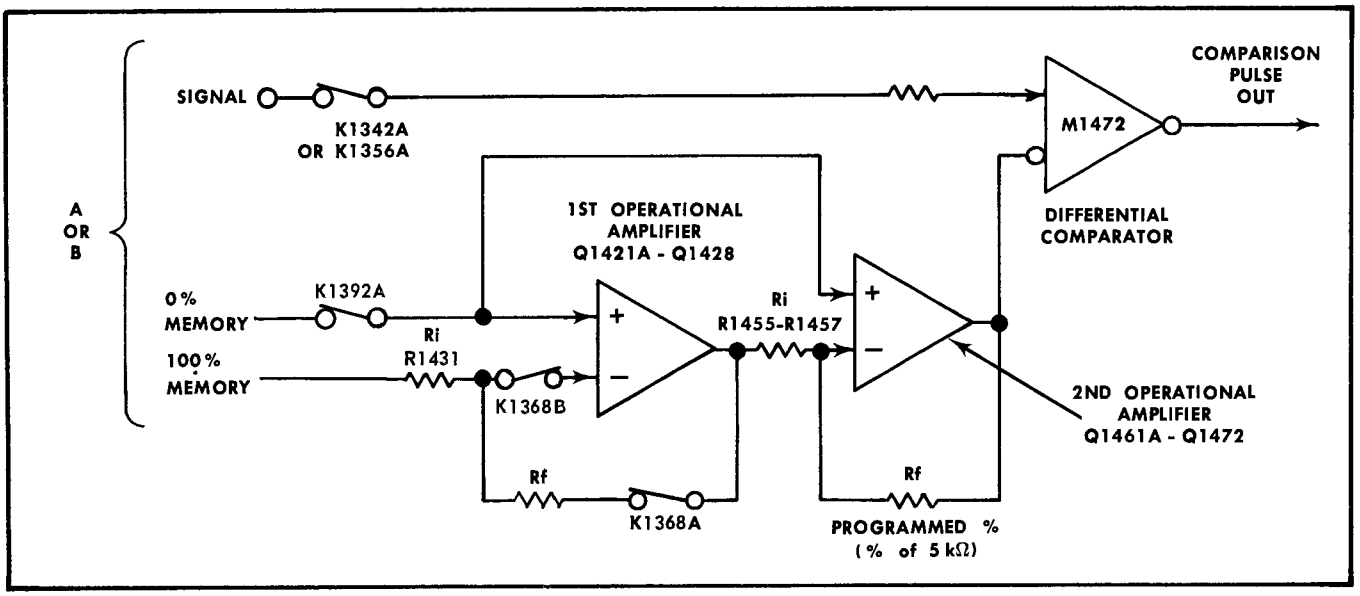


Fig. 4-13. Offset generator operation: time measurement mode, percent between zones.

R1457 to the — input of the second operational amplifier (Q1461B, Q1461A, Q1462, Q1464 and Q1472). The feedback resistance (R1481 through R1489) is selected by a 2-decade digital-to-analog converter (Q1513 through Q1583) operated by the front-panel TIME MEASUREMENT START POINT (or STOP POINT) switches or by remote program. The amount of feedback resistance connected back to the — input of the second operational amplifier determines the amount of offset from the reference level to be applied to differential comparator M1472. The D-A converter consists of a series of OR gates, inverters and inhibitors and the selectable feedback resistors that are enabled or inhibited by relays K1513 through K1583 (see Fig. 4-14). A combination of 1-2-4-2' and 1-2-4-8 logic is used by the converter to provide 2 decades of feedback resistance in 50-ohm increments from zero to 4.95 kΩ for front-panel operation or up to 7.65 kΩ for externally programmed operation. When all of the input program lines to the OR gates are high, all of the relays in the D-A converter are actuated and the programmed feedback resistance is zero ohms, providing a gain of zero for the second operational amplifier, and thus zero offset from the selected reference.

The first decade of the feedback resistors (R1481 through R1485) provide offset selection from zero to 9 increments. These increments represent percentage of the voltage between memory levels in the % Between mode. Diodes D1530 and D1540 are part of the 1-2-4-2' logic configuration of the first decade. When P6 pin 21 or Y is low, OR gates D1530 and D1540 cause relays K1523 and K1533 to be inhibited, in addition to K1543 which is inhibited directly by the input OR gate. This operation selects resistors R1482 through R1485 to provide increment 8.

The second decade (R1486 through R1489) provides increments of 10, 20, 30, . ., 150. Since both decades can be programmed together, 160 increments of offset, from zero through 159 (% or mm), may be selected. However, this total amount is available only through external programming, since the front-panel switches can only total up to 99. When SW1585 is set to the CALIBRATE position, inhibitors Q1563 and Q1583 cause relays K1563 and K1583 to be inhibited, selecting the 1 kΩ and 4 kΩ values of feedback resistance for an overall gain of one for the two operational amplifiers. The input resistance adjustment (R1455, 5 V GAIN) of the second amplifier is normally adjusted when SW1585 is set to CALIBRATE position so that its output is offset 5 volts from the reference input.

Volts (A or B) Mode

When either the A or B VOLTS measurement mode is selected (see Fig. 4-15), the operation of the Start and Stop Comparators is similar to that used in the % Between Zones mode just described. The main logic difference between these two modes is selection of the VOLTMETER RAMP by K1324 as the comparison signal and programming is second operational amplifier feedback resistance to be a fixed value of zero ohms. Normally this sets the start comparator for zero mm offset above the 0% memory and the stop comparator for zero mm offset above the 100% memory.

When the instrument is ready to measure, the VOLTMETER RAMP starts rising at a rate determined by the vertical plug-in unit. When the ramp reaches the 0% memory level of the offset generator on the Start Comparator card, the comparator fires, starting the operation of the clock. When the VOLTMETER RAMP reaches the 100% memory level of the offset generator on the Stop Comparator card, that comparator fires, stopping the clock. The number of clock pulses passed during the excursion of the VOLTMETER RAMP is proportional to the voltage between the two memory levels and is read out as voltage by the Type 230. If the 0% memory level is set to be more positive than the 100% level, the voltage readout is negative (—).

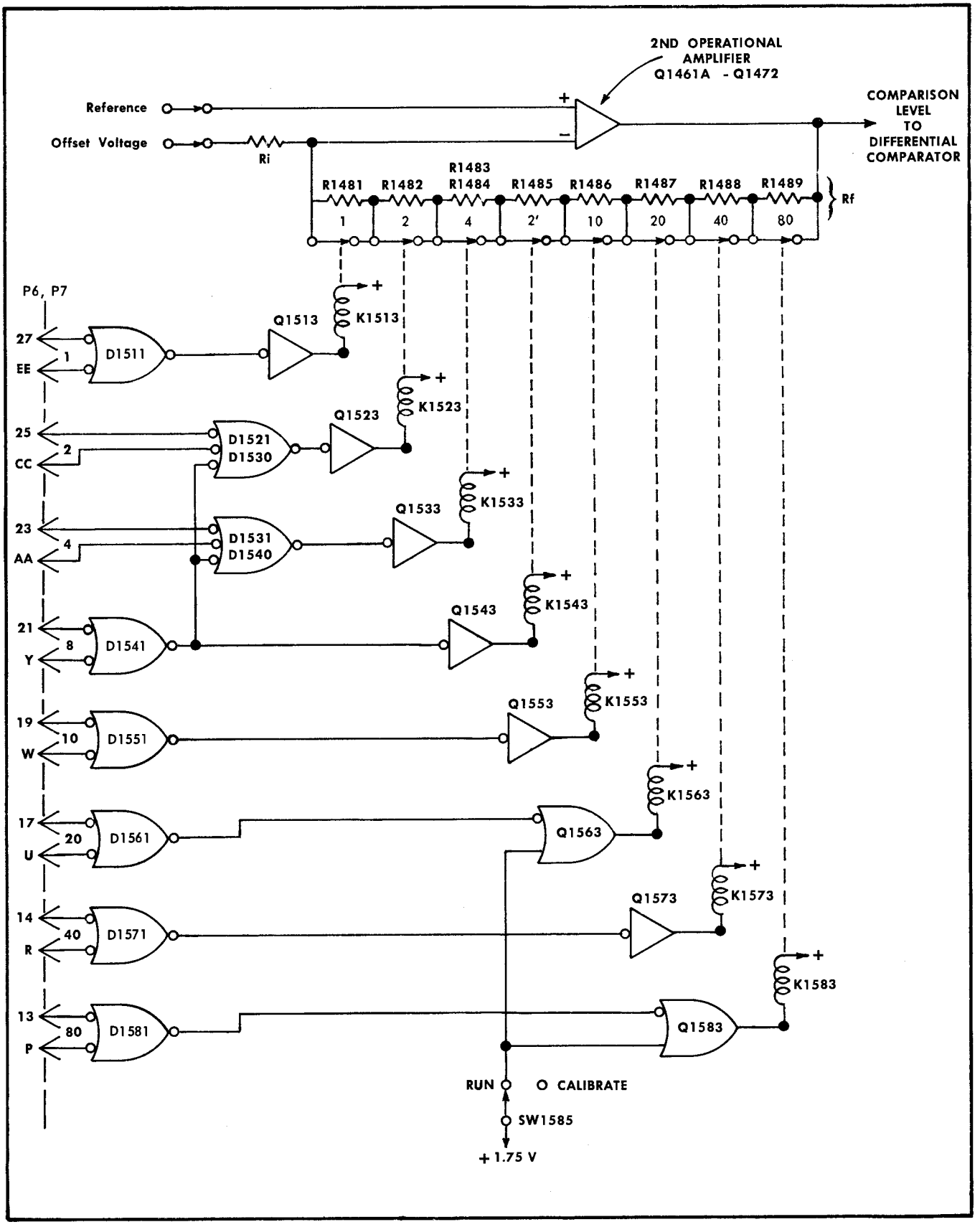


Fig. 4-14. Comparator offset generator control.

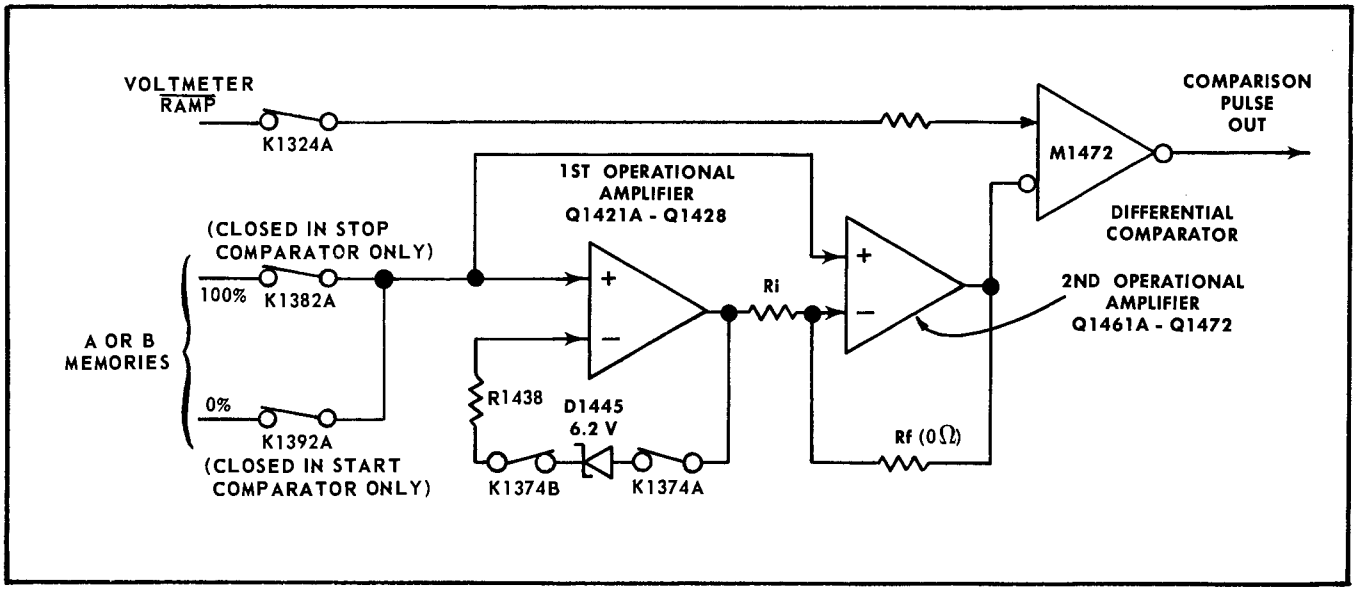


Fig. 4-15. Offset generator operation: A or B volts measurement mode.

mm Above or Below

When the Type 230 is set for a Time Measurement mode using mm Above or Below the 0% or 100% zone, the feedback element to the —side of the first operational amplifier is zener diode D1445. Transistors Q1442 and Q1449 provide constant current for the zener diode.

Either the 0% memory level or the 100% memory level of the selected signal is used for the reference at the + input to both amplifiers. Offset is provided by D1445, either above or below the reference level as selected by relays K1364 (mm Below) or K1374 (mm Above). The selected feedback of the second operational amplifier then sets the offset in mm of the CRT display, with 1 mm change being produced by a resistance change of 50 ohms. Only mm Above 0% and mm Below 100% are selectable from the front panel of the Type 230, but mm Below 0% and mm Above 100% may be obtained by means of external programming. The operation of the start and stop comparators in these four modes is shown in Fig. 4-16.

When the instrument is ready to make a measurement, the signal excursion through the comparison level (mm from one of the memories) on the start comparator starts the operation of the clock circuit and the signal excursion through the comparison level on the stop comparator stops the clock. The number of output pulses made by the clock during this interval is proportional to the time the signal takes to move between the two levels, and is presented as time on the front-panel readout.

Horiz mm From Sweep Start

Selecting the HORIZ mm FROM SWEEP START mode of the Type 230 actuates relays K1318 and K1374 on the Start and Stop Comparator cards. Relay K1318 selects the 5V $\overline{\text{RAMP}}$ as the comparison signal and connects ground as the reference level to the offset generator. Relay K1374 provides + offset from ground, by means of D1445, to be compared to the positive-going 5V $\overline{\text{RAMP}}$ (see Fig. 4-17). The programmed feedback resistance of the offset generator is proportional to mm of horizontal displacement from the left edge of the CRT display. When the 5V $\overline{\text{RAMP}}$ voltage runs up to the comparison voltage set by the start comparator (time measurement start point), the differential comparator starts the operation of the clock circuit. When the 5V RAMP reaches the comparison voltage of the stop comparator (time measurement stop point), that differential comparator stops the clock. The number of pulses produced while the clock is running is proportional to the elapsed sweep time and is presented as time on the front-panel readout.

SYNCHRONIZER CIRCUIT CARD (Model 1, 2)

The Synchronizer circuit card controls the sequence of events in the measurement cycle. Gates and flipflops on the card monitor the operations of the various elements in the program, and as each step is completed, the fact is detected by a gate or flipflop, which then initiates the next step. The Synchronizer circuit card also generates the internal trigger ($\overline{\text{DELAY}}$) which starts the measurement program if the Type 230 is operating in the self-triggered mode. The following logic description of the Synchronizer circuit card explains when and how the various control signals are generated.

$\overline{\text{Delay}}$ Pulse

The source of the $\overline{\text{DELAY}}$ pulse is the delay generator circuit on the Synchronizer circuit card (see Fig. 4-18). While the repetition rate of the $\overline{\text{DELAY}}$ pulse can be varied from the front panel (by DISPLAY TIME control R505), the width can be varied by internal adjustment R1780 only. Once a $\overline{\text{DELAY}}$ pulse is generated, the measurement cycle must be completed and all the logic gates satisfied before a second pulse can be generated.

In operation, the delay generator (transistors Q1774, Q1777, Q1785, and Q1787 and associated circuitry) can be inhibited

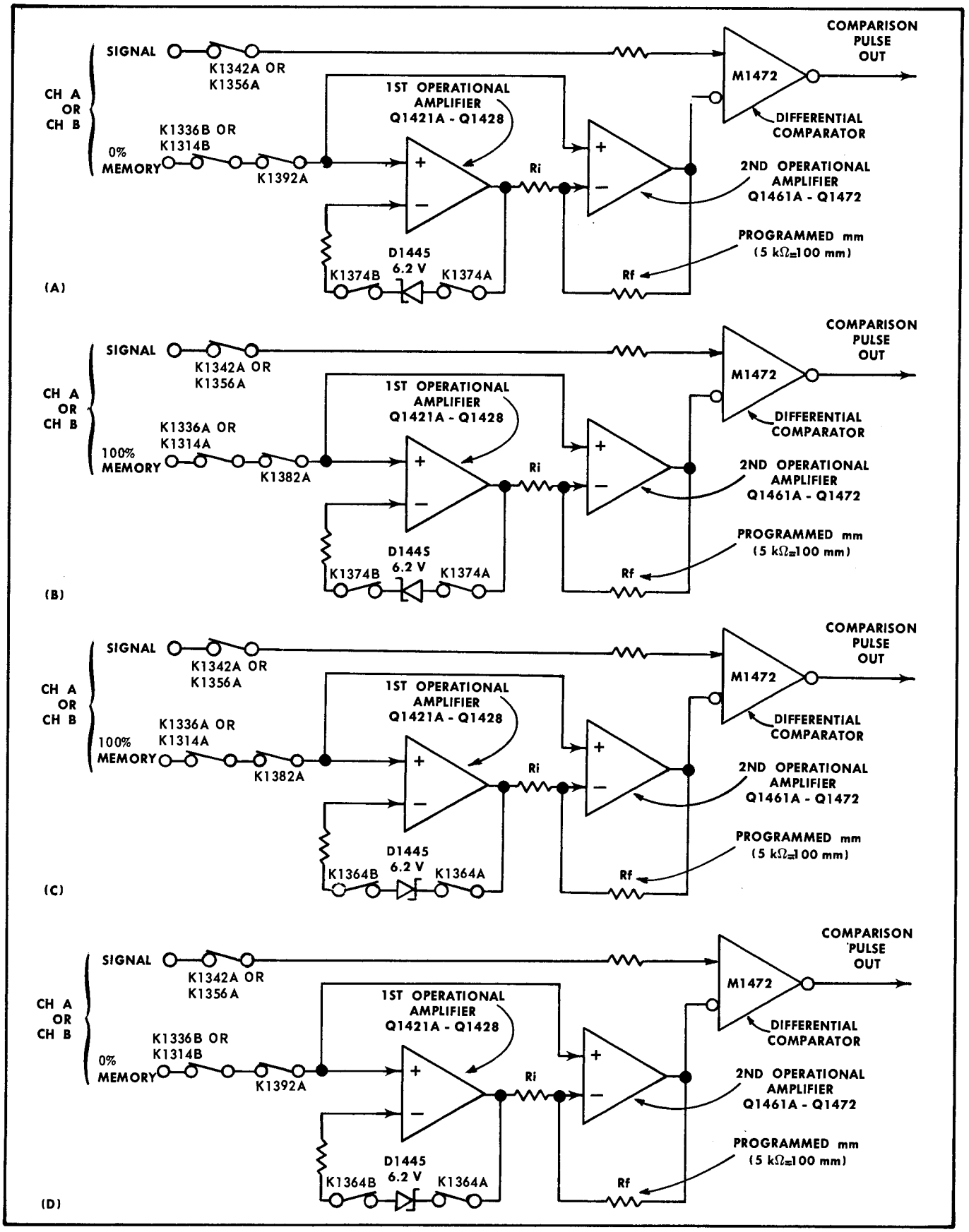


Fig. 4-16. Offset generator operation: (A) mm above 0% zone; (B) mm above 100% zone (externally programmed only); (C) mm below 100% zone; (D) mm below 0% zone (externally programmed only).

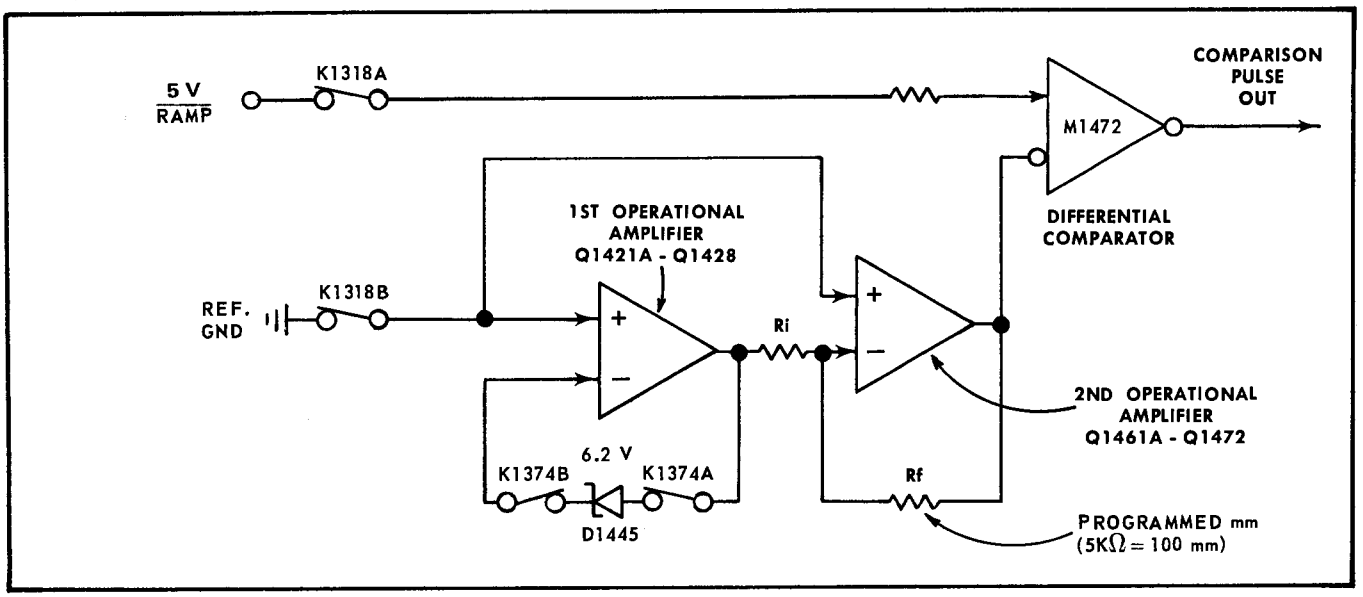


Fig. 4-17. Offset generator operation: time measurement mode, horiz mm from sweep start.

from two sources. The first source, LOCKOUT, (pin 6 of NAND gate M1770 through resistor R1768) ensures that a trigger pulse cannot be generated while a measurement cycle is in process. The second source (pin 6 of bistable M1724 through TRIGGERED MEASUREMENT switch SW502 and resistor R1769, see circuit diagram) permits the timing of the Type 230 to be controlled by external programming equipment. A positive voltage through either R1768 or R1769 biases Q1785 into conduction and locks the delay generator in its low state.

For purposes of explanation, assume that SW502 is ON and that positive trigger pulses from an external source are applied to pin Y. Assume also that a measurement cycle has been completed and that the output on pin 6 of M1770 is low.

The externally applied, positive-going trigger pulse is applied to M1724 pin 3. Flipflop M1724 sets. The low on M1724 pin 6 turns off transistor Q1785. With Q1785 turned off, the voltage on the anode of diode D1785 rises and transistor Q1777 is biased into conduction. The conduction of Q1777 turns on Q1774, which further increases the drive to Q1777. As a result of the foregoing regenerative action, switching is very rapid and a fast rising positive pulse is coupled out through resistor R1774.

The positive pulse at the collector of Q1774 is also coupled out through resistor R1780 (DELAY) and R1781 to diode D1781. Diode D1781 conducts and connects the pulse to capacitor C1787 and to the gate of FET Q1787. The time constant provided by R1780, R1781 and C1787 controls the width of the internally generated trigger pulse (DELAY). Since the other synchronizer circuits in the Type 230 are activated by the negative-going edge of the pulse on the collector of Q1774, the pulse width provides a delay between the application of the externally applied trigger pulse and the start of a measurement cycle. This delay permits the reed switches and other external circuitry to switch and settle down before the measurement cycle commences.

As the voltage on the gate of Q1787 goes positive, Q1787 starts drawing current through resistor R1787 and Q1787 drain voltage starts decreasing. The decrease is coupled through resistor R1784 and R1783 to the base of Q1777. From one to 8 milliseconds after the start of the pulse (this time is adjustable by Delay Control R1780) Q1787 cuts off Q1777. Cutting off Q1777 also cuts off Q1774 and the voltage on the collector of Q1774 drops, ending the pulse. When the pulse ends, D1781 becomes back biased, and the only way C1787 can discharge and turn off Q1787 is through DISPLAY TIME control R505. As C1787 discharges, Q1787 decreases conduction. The voltage on Q1787 drain starts to rise, but meanwhile Q1785 has been biased back into conduction by M1770. The conduction of Q1785 prevents another pulse from being generated until the end of the measurement cycle as explained in the following paragraph.

When DELAY goes positive, the positive pulse coupled out through R1774 is applied to clock reset flipflop M1762 pin 3. Since MEASURE is low at this time, M1762 sets and its output pin 7 goes high. The high on M1762 pin 7 is connected to M1770 pin 2. The high on M1770 pin 2 causes the output on M1770 pin 7 to go low. Now, as soon as DELAY ends and goes low, M1770 pin 3 and 5 both have low inputs and the output on pin 6 goes high. The high output on pin 6 biases Q1785 back into conduction and locks up the delay generator until MEASURE sets M1762, then ends.

At the start of the next MEASURE pulse, M1724 resets, causing M1724 pin 6 to go high. This holds Q1785 on and locks out the delay generator until the next externally applied trigger is received. When Q1785 is conducting it holds off Q1777 and DELAY is held low. This does not inhibit the display time function of C1787/R505; the time between DELAY pulses is determined by the external trigger rate.

Going back to the time when DELAY ended, the end of DELAY triggers the remaining part of the measurement cycle into operation. The first step is to discharge the memories and reset the counters. These actions are accomplished as explained in the following paragraphs.

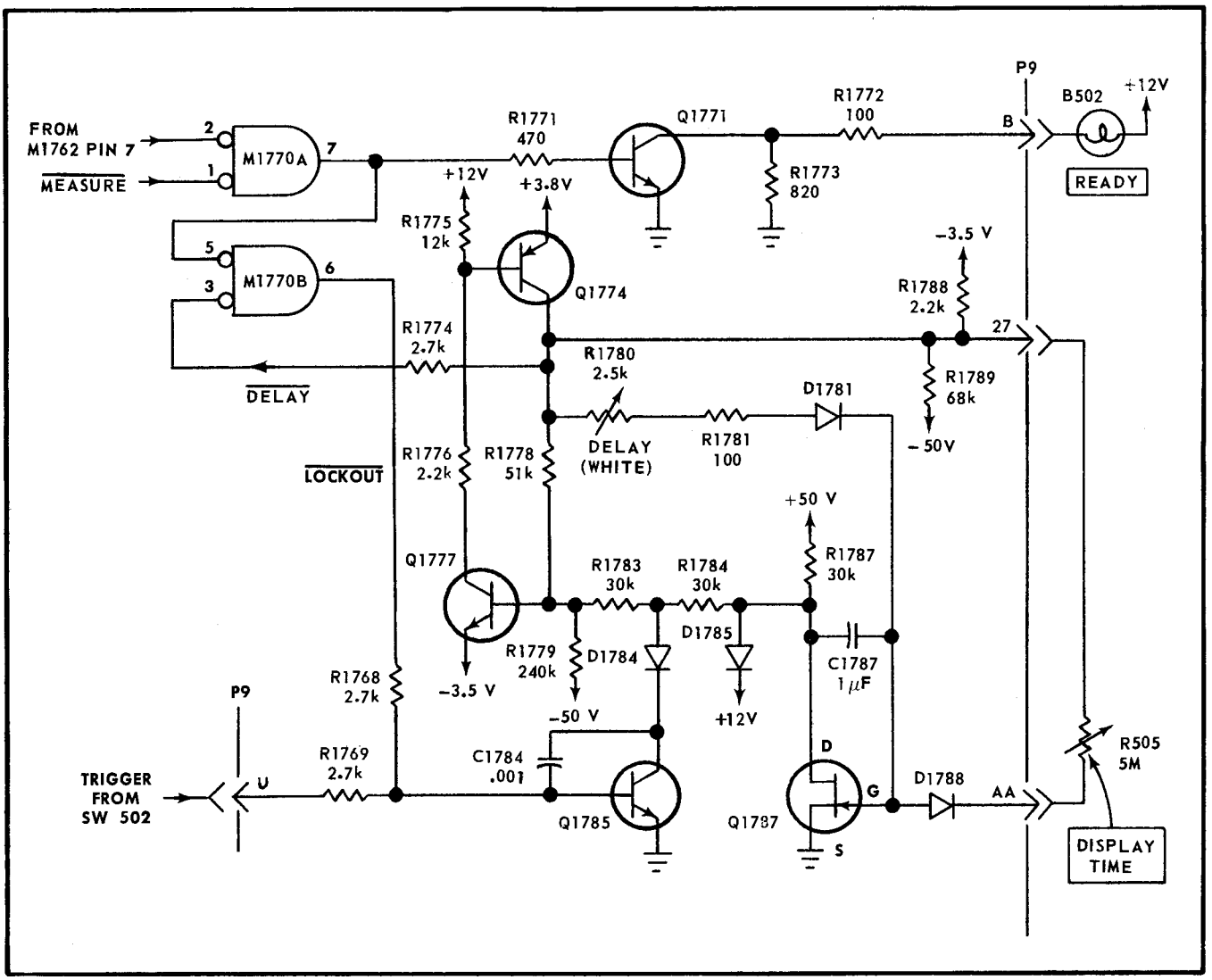


Fig. 4-18. DELAY generation (synchronizer models 1 and 2).

Memory Discharge Pulse

The positive DELAY pulse generated by Q1774 and Q1777 is coupled through R1774 to pin 3 of discharge flipflop M1804 (see Fig. 4-19). The pulse resets the flipflop and the output on M1804 pin 6 goes low. The low from pin 6 is applied to pin 5 of NAND gate M1748B. The circuit waits until GATE goes positive at the start of a sweep (there is no fixed relationship between DELAY and GATE). When GATE goes negative, both inputs to M1748B (pins 3 and 5) are low and the output on M1748B pin 6 goes high, reverse biasing transistor Q1806. When Q1806 cuts off, its collector goes negative, and the negative-going signal is coupled out through resistor R1808 to the Memory circuit card, discharging the memories.

When GATE once again goes positive at the start of the sweep, the positive-going transition is coupled through capacitor C1801 to M1804 pin 2, setting the flipflop and removing the enabling input to M1748B pin 5. Transistor Q1806 again conducts, ending the DISCHARGE pulse. Normally, no further DISCHARGE pulses can be generated until the delay circuit generates another positive pulse; but if the delay time is set longer than the time per sweep, it is possible to get more than one DISCHARGE pulse for one DELAY.

Counter Reset and Reset Pulses

The COUNTER RESET pulse is nothing more than the DISCHARGE pulse which is coupled out through resistor R1794. The COUNTER RESET pulse is generated from the COUNTER RESET pulse by inverter transistor Q1795. Both pulses can be inhibited by applying a low input to P9 pin 9. The COUNTER RESET INHIBIT line is provided in the event the operator wants to accumulate a count in the counter to perform a summing operation.

Measure Pulse

Average-Of-One-Mode. At the start of the memory sweep, the memory DISCHARGE pulse has discharged the

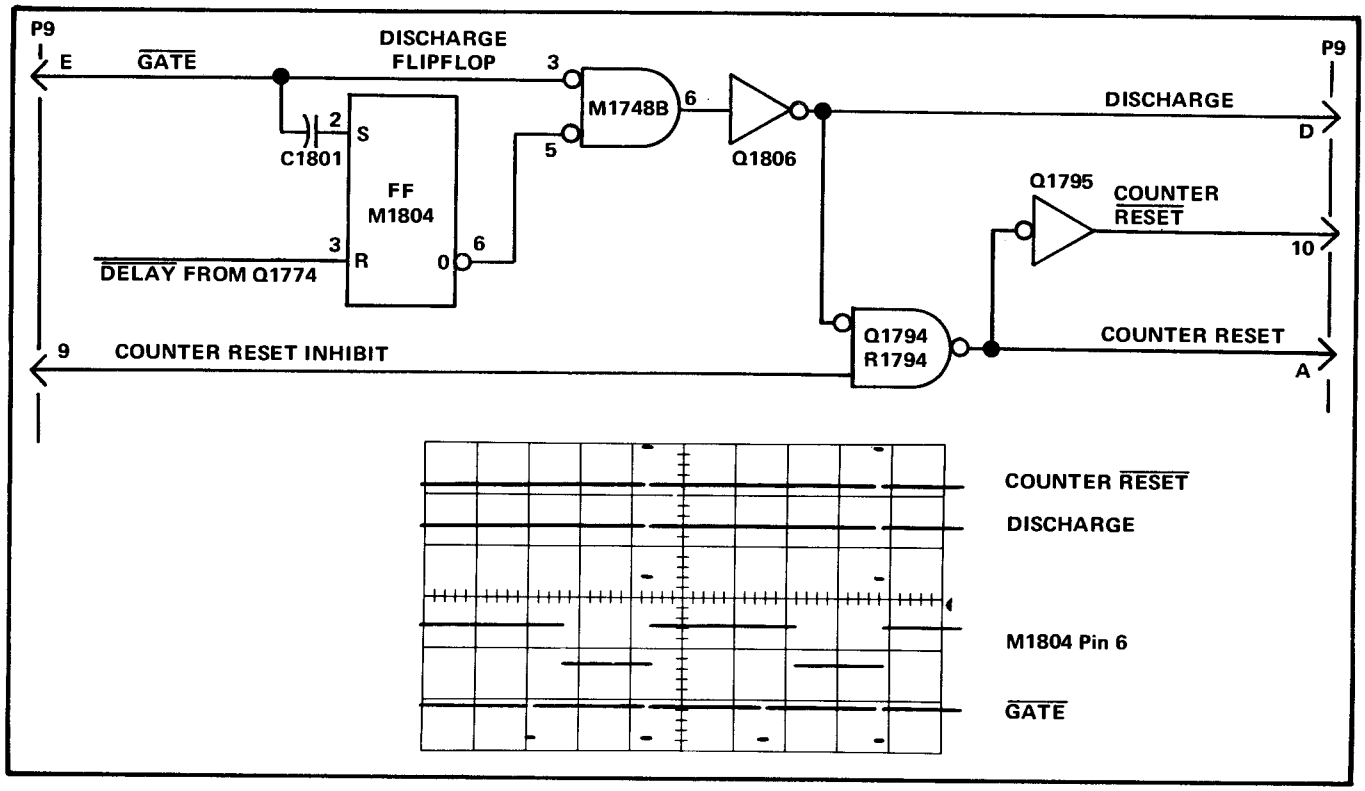


Fig. 4-19. DISCHARGE, COUNTER RESET and COUNTER RESET pulses (synchronizer models 1 and 2).

memories and the COUNTER RESET and COUNTER RESET pulses have reset the counters. As the sweep runs up, the memories are recharged. In the event the memories do not get properly charged on one sweep, more memory sweeps are made until the proper charge is obtained. The fact that the memories are charged is noted, and the Type 230 then makes a measurement sweep. The events that take place during the measurement sweep are largely controlled by the MEASURE and MEASURE pulses.

At the start of the memory sweep, M1804 is reset and has a low output on pin 7 (see Fig. 4-20). Likewise, DELAY has gone low. The DELAY signal is applied to four-input NAND gate M1760 pin 2 and the low output of M1804 pin 7 is applied to M1760 pin 5. GATE signal on M1760 pin 1 is low. It is now necessary to show that M1760 pin 3, the fourth input, is also low. When the DELAY pulse occurs and MEASURE on M1762 pin 2 is low, the flipflop resets and the output on M1762 pin 7 goes high. The low output on M1762 pin 6 is coupled to M1760 pin 3. All four inputs to M1760 are thus low and the output on pins 6 and 7 is high. This output is applied to the junction of diode D1718 and capacitor C1719.

The cathode side of D1718 is connected to four-input NAND gate M1718. Until the memories are charged, the output of M1718 is low and through D1718, M1718 clamps the output of M1760 low. All four memories must be charged before M1718 can go high and release the clamp that is holding on the output of M1760 through D1718.

Assuming that the memories become charged on the first memory sweep, the output of M1718 goes high. However, since the measurement circuitry must not be activated during the memory sweep, and RC circuit consisting of resistor R1718 and C1718 releases the clamp on M1760 slowly. The voltage must rise slowly to prevent capacitor C1719 from passing a trigger pulse to Measure flipflop M1720 at this time. However, circuit conditions are now such that M1720 can be triggered on the next (measurement) sweep.

At the end of the memory sweep, GATE goes positive and puts a high input on NAND gate M1760 pin 1. The output on M1760 pins 6 and 7 goes low, reverse biasing D1718 (the cathode side of D1718 is receiving a high signal from M1718 since the memories are charged). When GATE goes low at the start of the measurement sweep, M1760 pin 1 goes low again and the output on pins 6 and 7 goes high. Since D1718 is reverse biased, the output rise of M1760 is not slowed down by C1718, and a differentiated spike is coupled through C1719 to M1720 pin 6. Since pin 6 is the present input, M1720 resets with the outputs on M1720 pin 5 going high and pin 7 going low. The outputs of M1720 are inverted in M1722, making the MEASURE line to P9 pin 2 low and the MEASURE line to clock reset flipflop M1762 pin 2 high.

When the measurement sweep is completed, the Clock circuit card generates an END pulse which is applied to P9 pin 4 on the Synchronizer circuit card. The positive-going END signal is applied to the base of transistor Q1741 and biases Q1741 into conduction. The resulting low output of Q1741 is applied to NAND gate M1746 pin 2. Assuming that the Type

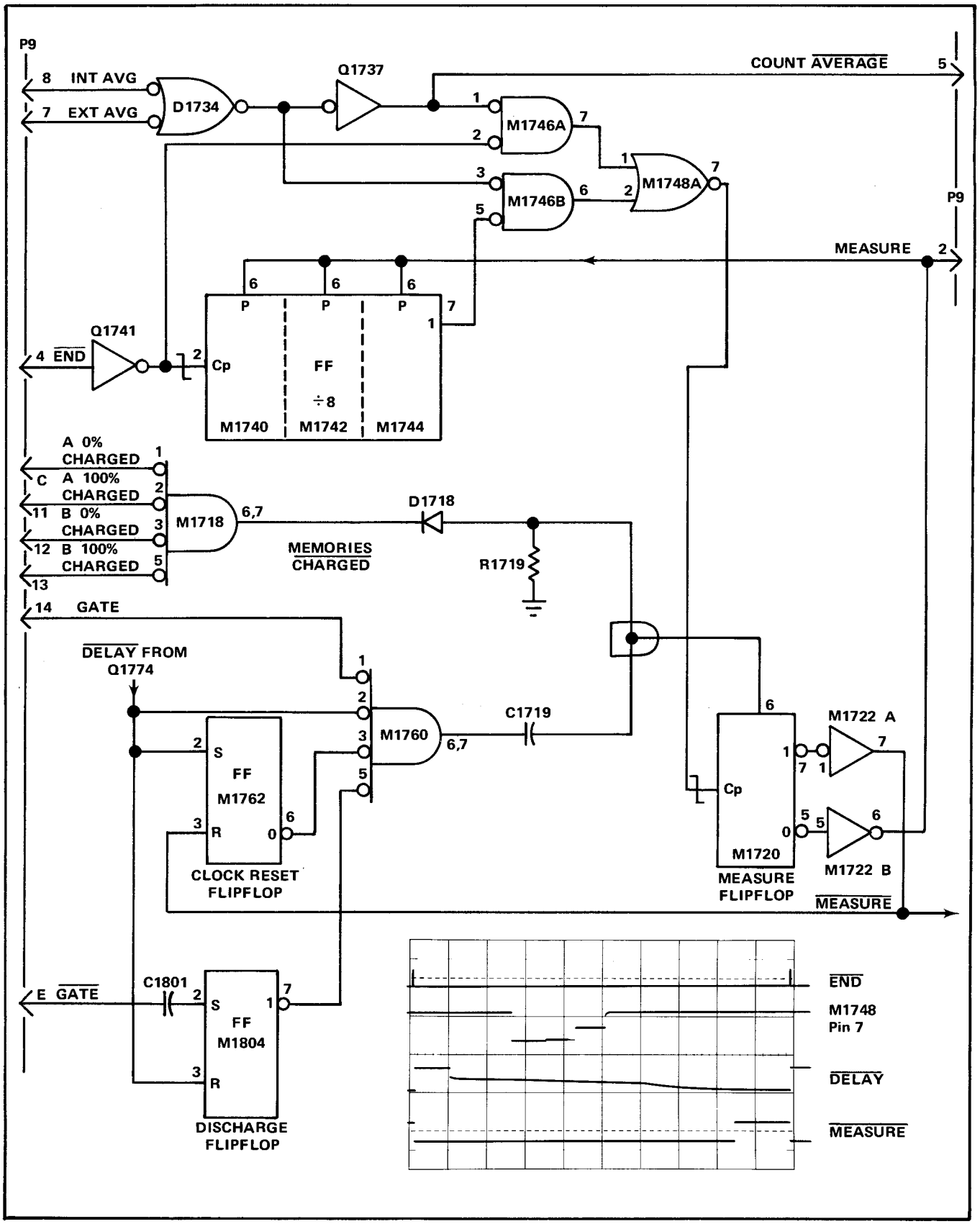


Fig. 4-20. MEASURE pulse generation (synchronizer models 1 and 2).

230 is operating in the average-of-one mode, the output to M1746A pin 1 is low also. The two lows on M1746 pins 1 and 2 result in a high output on M1746A pin 7. This high is inverted in M1748A, and the low output from M1748A is applied to pin 2 of measure flipflop M1720. The application of a negative-going signal to M1720 pin 2 sets the measure flipflop and thereby ends the positive MEASURE signal.

Average-Of-Eight Mode. The MEASUREMENT AVERAGE switch on the Type 230 front panel provides a means of averaging variations in signal measurements. With the MEASUREMENT AVERAGE switch set to 8, the gated clock pulses are divided by eight on the Clock circuit card and MEASURE stays high until the divide-by-eight counter (M1740, M1742, and M1744) on the Synchronizer circuit card has counted eight END pulses. After eight END pulses have been counted, M1720 is set and ends MEASURE.

In the average-of-eight mode, a low level is applied to either pin 7 or 8 of P9. The low signal shuts off transistor Q1737 and the output at Q1737 collector goes high. The high output of Q1737 is applied to NAND gate M1746A pin 1 and keeps the output on M1746A pin 7 low. The positive MEASURE signal presets the counter to zero and the output line from M1744 pin 7 to M1746B pin 5 is low. With low inputs on both pins 3 and 5 of M1746B (remember, P9 pin 7 or 8 is low), the output of NAND gate M1746B pin 6 goes high. The high output from M1746B pin 6 is inverted in M1748A and appears as low on M1748A pin 7. Since M1720 has pin 1 tied to a positive voltage through resistor R1720, the negative-going output of M1748A cannot toggle M1720.

GATE occurs and starts the measurement sweep. Since the memories are presumably charged from the memory sweep, the end of GATE causes the output of M1760 to go high and set measure flipflop M1720 as described before. MEASURE now goes high and remains so until eight END pulses have been counted by the counter.

As the END pulses arrive, they advance the counter until the count reaches 1-1-1 (decimal 7). At this point, the output on M1744 pin 7 goes high, the output of M1746B pin 6 goes low, and the output of M1748A goes high. Now, when the count advances to 0-0-0 on the next END pulse, M1744 pin 7 goes low, M1746 pin 6 goes high, and M1748A pin 7 goes low. The negative-going output of M1748A clocks measure flipflop M1720 and it resets to high, ending the MEASURE pulse as previously explained.

Ending the positive MEASURE signal applies a low input to M1762 pin 2, but the clock reset flipflop remains set. The low output from M1762 pin 7 is applied to M1756B pin 5, and since M1756B pin 3 is also low, the output on pin 6 is high. The high output on M1756B keeps Q1766 cut off and the CLOCK RESET remains low until either a DELAY pulse is generated or a GATE pulse is applied to P9 pin 14.

Clock Reset Pulse

As described in the preceding paragraphs, when MEASURE goes high, M1762 pin 2 receives the high input and the flipflop sets. Pin 7 goes low and pin 6 goes high. The low output from pin 7 is applied to NOR gate M1756B (see Fig. 4-21) whose output now goes high. The high output of M1756B turns off transistor Q1766. Turning off Q1766 permits the CLOCK RESET signal on P9 pin F to go low. The low output on P9 pin F is applied to the Clock circuit card, where it releases the clock gating circuits. The CLOCK RESET signal does not go high again until either a DELAY pulse is received by M1762 pin 3 or the GATE input at M1756B pin 3 goes positive.

Register Set Pulse

Now that the measurement has been made, it is necessary to transfer the count in the counters to the registers where it is held until the end of the next measurement sweep. The control signal which permits the registers to accept information contained in the counters is the REGISTER SET pulse.

The REGISTER SET pulse is derived through inverting the high REGISTER SET pulse, the inverting being done by inverter line-driver M1768. The REGISTER SET pulse is generated at the instant MEASURE goes negative at the end of the measurement sweep. The negative-going edge of MEASURE is applied through capacitor C1758 to M1758 pin 1 in the register set single-shot (see Fig. 4-22).

The register set single-shot (M1758 and M1756A) is a monostable circuit. With no pulse inputs, M1758 resets with the output on pin 7 low and the output on pin 6 high. The high output on pin 6 is applied to M1756A pin 1, causing a low output on M1756A pin 7. The low output on M1756A is applied back to M1758 pin 2. This is the stable state of the register set single-shot.

When MEASURE goes negative at the end of the measurement sweep, the negative-going edge of the pulse is coupled through C1758 to M1758 pin 1. Since M1758 pin 2 is receiving a low from M1756A pin 7, the conditions are now such that M1758 switches and pin 7 goes high. The high output on pin 7 is coupled back to M1758 pin 5, and the output on pin 6 goes low. The low output on M1758 pin 6 is applied to M1756A, causing M1756A pin 7 to go high and deliver a positive pulse to the REGISTER SET line. The high output is also applied through resistor R1757 to M1758 pin 2 and to capacitor C1757. The time constant of R1757 and C1757 keeps M1758 from returning to quiescence for about 10 microseconds, but at the end of that time the voltage on M1758 pin 2 has risen to the point where M1758 switches back to its stable state with pin 7 going low and pin 6 going high. When M1758 switches back to its stable state, the high output on pin 6 is coupled back to M1756A pin 2 and ends the REGISTER SET pulse. As REGISTER SET goes low, the signal is inverted by inverter line-driver M1768 and the REGISTER SET pulse goes high.

NOTE

When MEASURE goes low the output at M1762 pin 7 is low and both pins 1 and 2 of M1770A are low. The output on M1770A pin 7 goes high and makes the output on M1770B pin 6 low. The low signal at this point turns off Q1785 (assuming the TRIGGERED MEASUREMENT switch SW502 is OFF) and permits a new DELAY pulse to be generated at the end of the display time. This happens at the same moment that REGISTER SET pulse goes high. Since the DELAY pulse is one millisecond or more long and REGISTER SET is about 10 microseconds, the count is set into the counters long before DELAY enables the new measurement cycle.

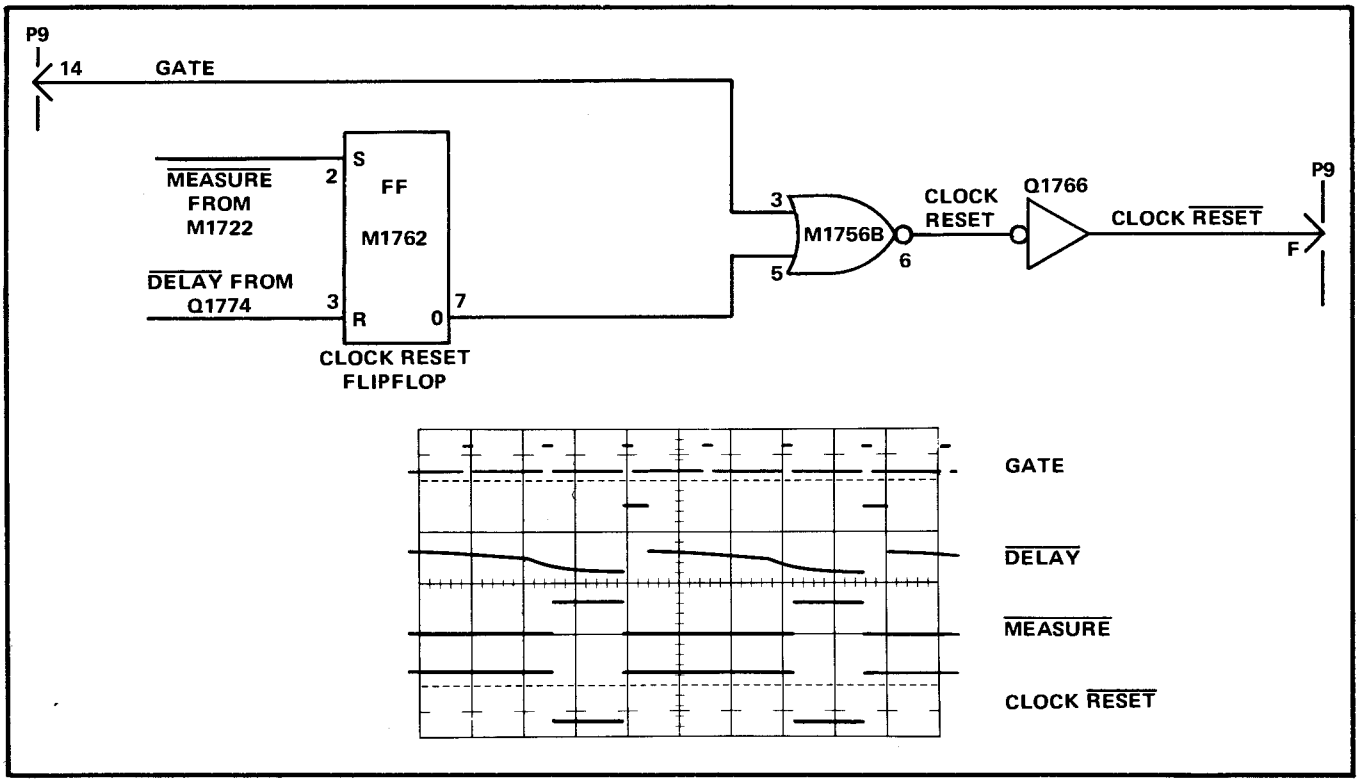


Fig. 4-21. CLOCK $\overline{\text{RESET}}$ pulse generation (synchronizer models 1 and 2).

If for some reason the external readout equipment (such as a printer) is unable to keep up with the Type 230, the readout equipment can direct the Type 230 to hold the count in the registers until the printer or other device has finished. The hold signal is connected to the EXT HOLD line on P9 pin M. A low on P9 pin M biases transistor Q1752 into conduction. The conduction of Q1752 applies a high to M1756A pin 2 and holds the REGISTER $\overline{\text{SET}}$ output on M1756A pin 7 low. Holding pin 7 low keeps the registers from accepting a new count and prevents the PRINT COMMAND from being generated. However, the rest of the measurement cycle is not interrupted, and the Type 230 continues to make measurements while waiting for the readout equipment to catch up.

Print Command Pulse

Assuming that the external readout equipment (printer, etc.) has not signaled via EXT HOLD line P9 pin M, the Synchronizer circuit card now generates the PRINT COMMAND PULSE. The conditions necessary for the generation of this pulse are as explained in the following paragraphs.

Print command single-shot M1728 is monostable. Pin 1 of M1728 is connected to +3.8 volts and with no signal inputs, the single-shot stays quiescent with a low output on pin 7. The low on pin 7 is applied back to pin 5, and since pin 3 is connected to ground through resistor R1726, pin 3 is also low. The two lows on the reset side of the flipflop cause a high output on pin 6, which biases transistor Q1729 into conduction and the output on P9 pin 21 is normally low.

When REGISTER $\overline{\text{SET}}$ goes positive for 10 μs as previously explained, the positive-going pulse is coupled through capacitor C1726 to M1728 pin 3. The differentiated positive spike causes the output on M1728 pin 6 to go low. The edge of the negative-going output on pin 6 is coupled through capacitor C1727 to M1728 pin 1 (causing pin 7 to go high) and through resistor R1728 to the base of transistor Q1729 biasing it into cutoff. With Q1729 cut off, PRINT COMMAND goes positive. The positive PRINT COMMAND is a signal that the count is being changed in the registers and is actually an inhibit signal provided to lock out the printer (or other readout device) while the count is being changed. After an RC time determined by C1727 and resistor R1727, M1728 pin 1 again goes high, pin 7 goes low, and pin 6 goes high (pin 3 has already gone low since the time constant of C1726 and R1726 is less than $\approx$150 μs time constant of C1727 and R1727). When pin 6 goes high, Q1729 starts to conduct and PRINT COMMAND goes negative, freeing the readout device for operation. The count in the registers can be used any time **except** when PRINT COMMAND is positive.

Chopper Drive Signals

In measurement systems where the signal inputs to the vertical plug-in unit include signal choppers, some means must be included to switch the choppers from signal to reference and back again at the right times. The choppers switch the vertical inputs to ground (or other reference) at the end of the GATE pulse (see Fig. 4-23), then switch the inputs back to the signal at the end of the first zone (A 0%, B 0%, A 100%, B 100%). Generally the zones will be set so that one of the 0% zones occurs first, but it makes no difference to the Type 230; it will always notify the choppers to switch back to the signal at the end of the first zone.

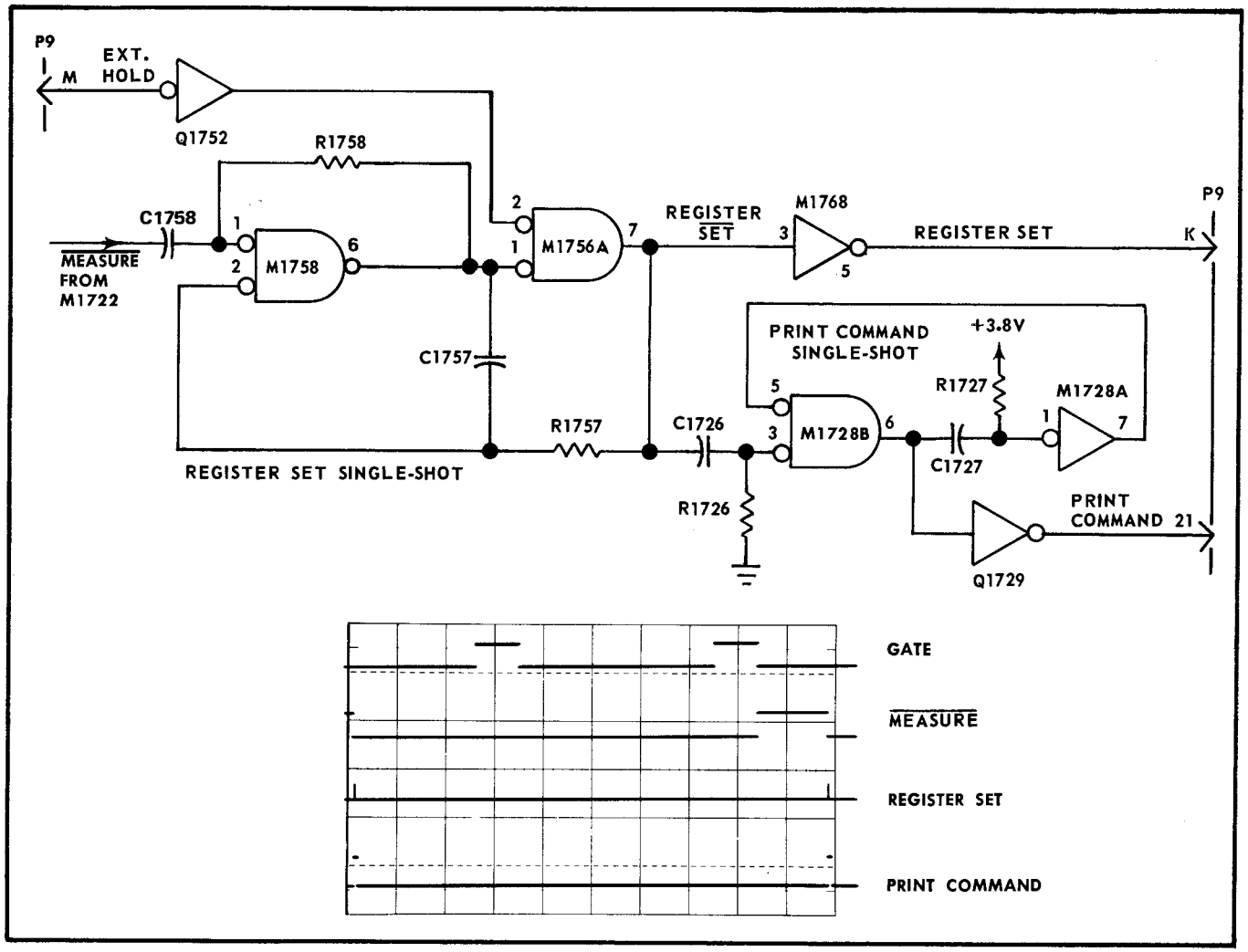


Fig. 4-22. REGISTER SET and PRINT COMMAND pulse generation (synchronizer models 1 and 2).

In operation, the GATE signal from the buffer (which is started by the Type 568 + GATE and ends at the end of MEASURE or when the VOLTMETER RAMP reaches 15 volts) is applied to flipflop M1812 pin 2. When GATE goes positive between sweeps, M1812 sets and pin 6 goes high. If transistors Q1817 and Q1827 are held off by programming inputs on P9 pins 3 and CC, the high on M1812 pin 6 biases transistors Q1815 and Q1825 into conduction. When Q1815 and Q1817 conduct, the CHOPPER DRIVE signals go low, switching the choppers.

When the first zone occurs, the $\overline{\text{ZONE}}$ bus (P9 pin L) goes high. The $\overline{\text{ZONE}}$ pulse is applied to M1810 pin 1, which then causes M1810 pin 7 to go low. At the end of the $\overline{\text{ZONE}}$ pulse (the bus has a positive pulse corresponding to each of the four zones) the output on M1810 pin 7 goes high. The positive-going output of M1810 pin 7 is differentiated by capacitor C1811 and is applied as a spike to M1812 pin 3. The positive spike resets the flipflop and pin 6 goes low. The flipflop remains reset until the GATE pulse again sets it.

Transistors Q1817 and Q1827 in the chopper drive circuit provide a means of externally programming the operation of the choppers. Control signals in the form of ground closures or a saturated transistor can be applied to P9 pins 3 and CC to enable "A" or "B" CHOPPER DRIVE signals as desired.

Sweep Speed-Up Signal

When using the Type 230 in a system that employs equivalent-time sampling techniques, the time between measurement can be shortened by speeding up those portions of the sweep that occur outside the zones of interest. The 0% memories charge during the 0% zones, the 100% memories during the 100% zones. The rest of the memory sweep is necessary only for proper smoothing. During the measurement sweep the time before the measurement starts and the time after the measurement is finished is unused. While the unused portions of the sweep cannot be completely eliminated, they can be speeded up.

The sweep is speeded up by applying a logical low to the sampling time base unit through P9 pin P (see Fig. 4-24). In normal operation, P9 pin N is open and transistor Q1744 is cut off, making the output on P9 pin P negative. When P9 pin N (HIGH SPEED PROGRAM) is grounded, Q1844 will conduct and ground P9 pin P any time the output of M1823B goes high.

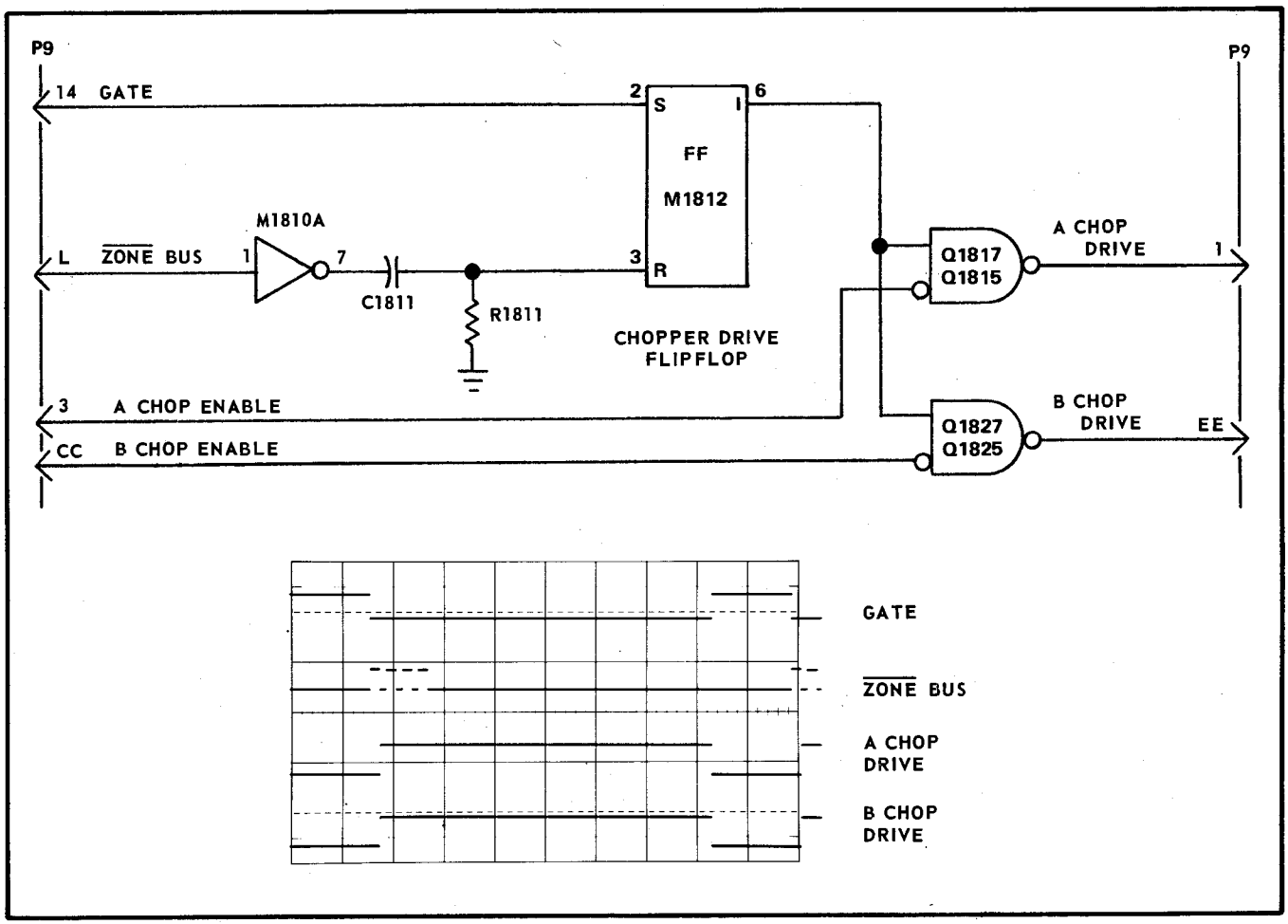


Fig. 4-23. CHOPPER DRIVE signal generation (synchronizer models 1 and 2).

During the memory sweep, ZONE on pin L of P9 goes positive each time a zone occurs. The high signal is applied to M1810A pin 1 and causes a low output of M1810A pin 7. Since the input on M1810B pin 5 is low during the memory sweep, coupling the low on M1810A pin 7 to M1810B pin 3 causes the output on M1810B pin 6 to go high. The high output of M1810B pin 6 is applied to M1832B pin 3 and the output on M1832B pin 6 goes low, turning off Q1844. The output on P9 pin P goes negative and the sweep returns to 100 dots per division during the zones. When the sweep is outside the memory zones, the high ZONE pulses are absent and M1810A delivers a high on pin 7. The high output from M1810A pin 7 is coupled around to M1810B pin 3 and causes a low output on M1810B pin 6. Since MEASURE is low during the memory sweep, both pins 3 and 5 of M1832B are now receiving a low and the output on M1832B goes high, turning on Q1844. The conduction of Q1844 grounds P9 pin P and the time-base unit switches to a 10-dots-per-division sweep. During the measurement sweep, M1832B delivers a low output and cuts off Q1844 when MEASURE goes high. When the END pulse from the Clock circuit card terminates the high MEASURE signal, the two lows on pins 3 and 5 of M1832B cause a high output on M1832B pin 6. Transistor Q1844 now conducts, grounds P9 pin P, and thereby speeds up the sweep.

Single Sweep Signal

The sweep from the time-base unit (Type 3T4 for example) is not normally synchronized with the DELAY pulse of the Type 230. This results in considerable lost time if DELAY occurs just after the time-base unit has started a sweep. Since the Type 230 actually starts the measurement cycle on the first GATE pulse which occurs after a DELAY pulse and since the GATE pulse is derived from the time base unit's + GATE, the time between DELAY and the generation of GATE can sometimes become intolerably long. The Tektronix Type 3T4 Programmable Sampling Sweep Unit has a programming input called SINGLE SWEEP which can be used for synchronizing the sweep of the Type 3T4 with the DELAY pulse, thus eliminating most of the instances where one piece of equipment must wait for the other to finish an operation.

Grounding P9 pin N (HIGH SPEED PROGRAM) on the Synchronizer circuit card not only activates the sweep speed-up circuit but makes synchronizing pulses available on P9 pin H also. With P9 pin N grounded, M1832A pin 2 is held low. Now, each time MEASURE goes low, the output on M1832A pin 7 goes high and a differentiated positive spike is coupled through capacitor C1833 to input pin 2 of flipflop M1836. The positive spike to M1836 pin 2 sets the flipflop and the output on pin 7 goes low. The flipflop remains set

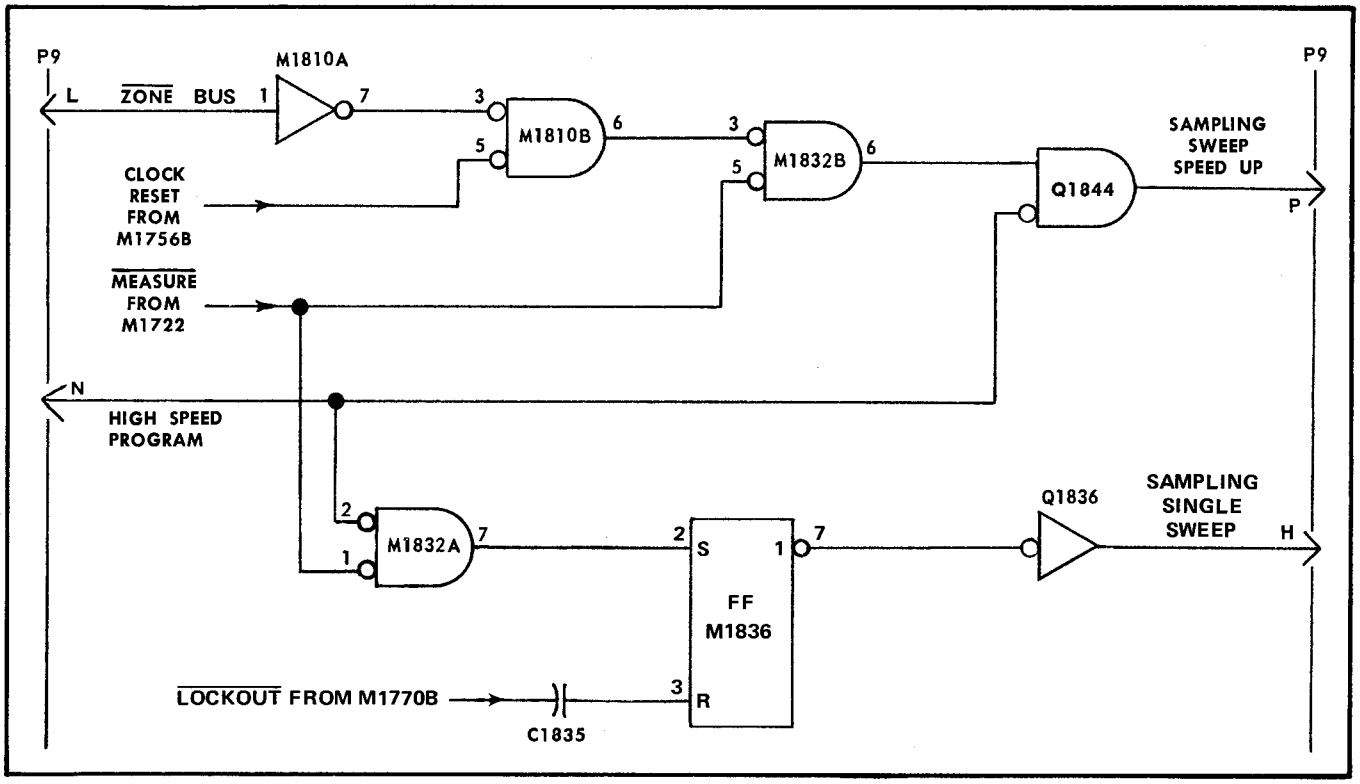


Fig. 4-24. SWEEP SPEEDUP and SINGLE SWEEP signal generation (synchronizer models 1 and 2).

until DELAY goes negative and resets the flipflop through M1770 and capacitor C1835. When M1836 is reset by the ending of MEASURE, the low output on M1836 pin 7 biases transistor Q1836 into conduction, effectively grounding P9 pin H. With the ground (actually saturation resistance of Q1836) on P9 pin H, the sweep circuit in the Type 3T4 is locked up. When DELAY goes negative the flipflop resets and the output on M1836 pin 7 goes high. Transistor Q1836 is now turned off and the Type 3T4 sweep circuit is unlocked. When the next triggering event occurs and starts the sweep in the Type 3T4, GATE ends and a memory sweep is made. After the memories are charged, a measurement sweep is made. Upon completion of the measurement, MEASURE goes low and again locks the sweep on the Type 3T4 until the next DELAY pulse occurs.

SYNCHRONIZER CIRCUIT CARD MODEL 3-UP

The Synchronizer circuit card generates most of the control signals which determine the sequence of events in the measurement cycle. The term "measurement", as used in this discussion, is the time interval corresponding to the Type 230 measurement zone, during which the Type 230 is counting clock pulses (proportional to time or voltage). "Measurement" may also refer to the results obtained from the count. The term "measurement cycle" is defined as the time interval from the end of the previous measurement (the end of the measurement zone in the previous measurement sweep) to the end of the readout of the present measurement. Due to the sequential nature of operations in the Type 230, there is some overlap between adjacent measurement cycles, because each new measurement cycle is started before the previous measurement is read out. The term "display time" means the time interval during which the readout Nixies[2] on the Type 230 front panel are displaying the measurement reading. Since the previous measurement readout is held only until the new measurement is read into the registers, the duration of the display time is approximately equal to the interval between measurements, but lags one measurement behind.

Each measurement cycle includes a memory-charging event, a measurement event, and the measurement readout. Usually there is one memory-charging sweep and one measurement sweep in each measurement cycle, but there may be more than one of either type of sweep under certain conditions.

The synchronizer resets the clock, discharges the memories and resets the counters, then monitors the state of the memories while they are changed to match the levels of the incoming signals. After the memories have reached full charge, the synchronizer starts the measurement and releases the clock reset. After the measurement count has been taken, the synchronizer sets the new count into the registers and initiates readout. For high-speed programming, the synchronizer also controls the dot density and reset point of each sweep.

Timing Diagram

Fig. 4-25 shows the basic timing sequence of signals through the synchronizer when using minimum delay holdoff and a sampling sweep rate of 100 ns/division. The synchronizer is operated in free-running mode (non-triggered) for

[2]Trademark Burroughs Corp.

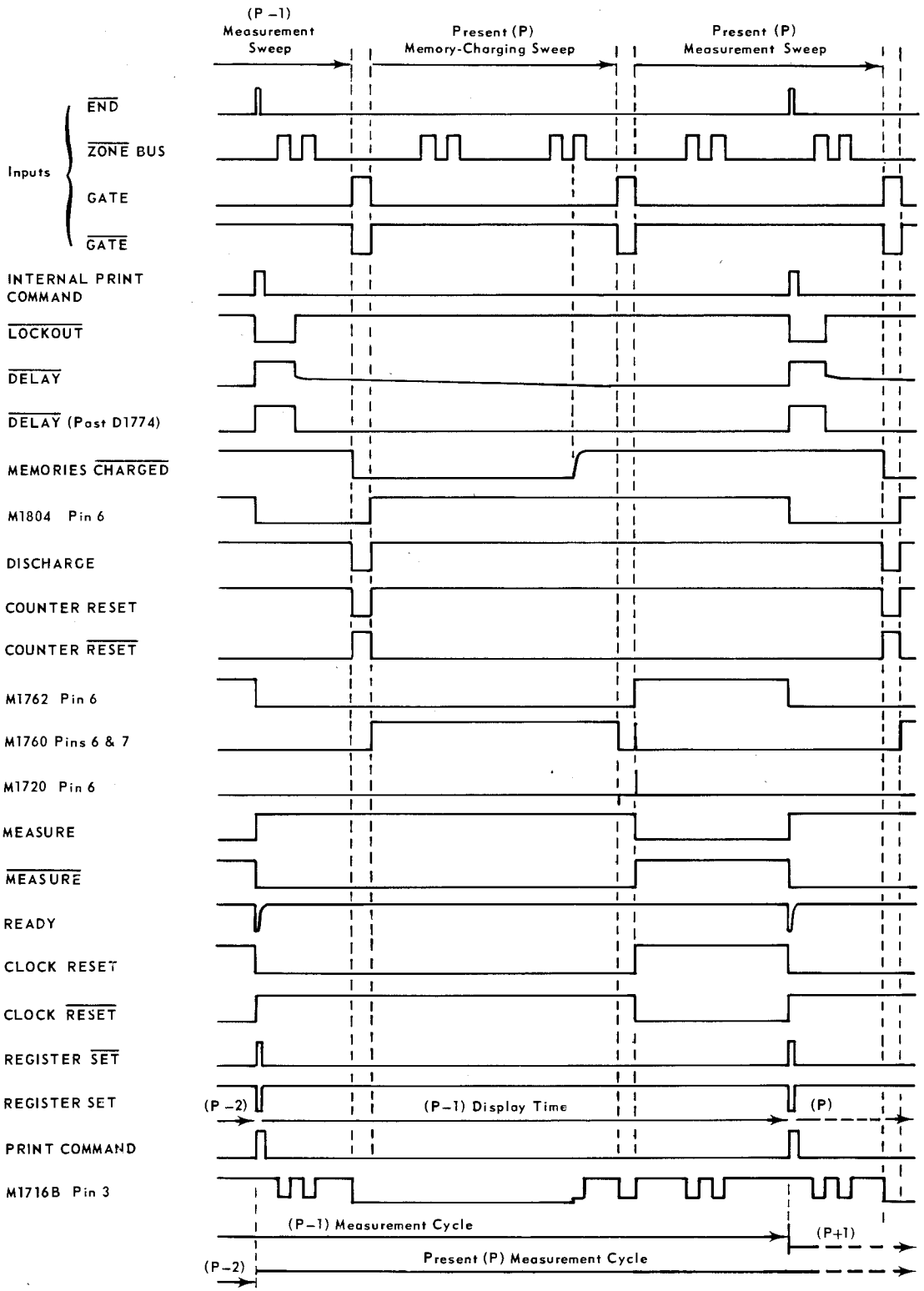


Fig. 4-25. Timing diagram of synchronizer signals (synchronizer model 3-up).

these waveforms, and none of the input enable or inhibit lines (such as HIGH SPEED PROGRAM) are programmed. Exceptions to this timing sequence are discussed wherever appropriate in the text.

DELAY and LOCKOUT

The DELAY pulse is an internal trigger signal that is generated and used by the synchronizer to activate the measurement circuitry. The source of the DELAY pulse is the delay generator shown in Fig. 4-26. After one DELAY pulse has been generated, the measurement must be completed and the delay generator must have completed its holdoff period before another DELAY pulse can be produced.

In free-running (non-triggered) mode, DELAY starts automatically at the beginning of the measurement cycle if the delay generator holdoff period (set by the front-panel DISPLAY TIME control) is set to end before the end of the measurement, or at the end of the delay holdoff if it is set to end later than the end of the measurement. In this mode, the repetition rate of DELAY (and of the measurement cycles), can be varied by means of the DISPLAY TIME control. If the DISPLAY TIME control had been turned away from the fully counterclockwise position (higher resistance of R505) for the waveforms in Fig. 4-25, the start of the DELAY pulse would have occurred some time after the beginning of the measurement cycle (at the end of the previous measurement).

In triggered measurement mode, DELAY starts at the arrival of the first external trigger after the start of a measurement cycle (if the delay holdoff has ended). Therefore, the repetition rate of DELAY in this mode is controlled by the external triggering signal. However, if the trigger occurs after the start of the previous measurement but before the end of the delay holdoff, DELAY occurs automatically at the end of the measurement or the end of the delay holdoff (whichever is later) and is not actually triggered. The external control equipment usually provides a trigger following the desired delay holdoff, thus avoiding this non-triggered operation.

The delay generator is inhibited by either or both of two signals, the output from external trigger flipflop M1724 (through the TRIGGERED MEASUREMENT switch), or the output from lockout flipflop M1764. The inhibit signal from pin 6 of M1724 permits the start of the measurement to be controlled by an external triggering signal; the inhibit from pin 7 of M1764 (LOCKOUT) prevents the delay generator from producing more than one DELAY pulse for each measurement cycle. A high level from either source to the base of Q1785 holds the transistor in saturation and locks DELAY at its low level.

To understand the operation of the circuit, assume that a measurement has just been completed. Under the conditions given for Fig. 4-25, the lockout flipflop has just been preset by INTERNAL PRINT COMMAND, causing pin 7 (LOCKOUT) of M1764 to go low. Since the inhibit input to Q1785 from the external trigger flipflop (through the TRIGGERED MEASUREMENT switch) is open, the negative-going transition of LOCKOUT turns off Q1785, releasing D1784 and allowing the voltage at the base of Q1777 to go positive (assuming that the delay holdoff has ended). This turns on Q1777 which also turns on Q1774, and the regenerative action through R1778 causes a fast-rising pulse at the collector of Q1774. This is the start of the DELAY pulse.

To make sure that all of the synchronizer circuits function properly following instrument turn-on or momentary power failure, the +50-volt and +12-volt power supplies are connected to initiate one measurement cycle at turn-on. As power is applied, the +12-volt supply presets M1764 through R1761 and C1761. At the same time, the +50-volt supply presets M1724 through C1701, R1701 and D1702, and pulls up on the base of Q1785 through D1703, momentarily turning on Q1785. When C1701 becomes charged, Q1785 turns off (because LOCKOUT is also low), initiating a DELAY pulse. One measurement must then be completed before the instrument is ready to start into a normal measurement operation.

The positive-going transition of DELAY at the collector of Q1774 is coupled through R1780 (DELAY), R1781 and D1781 to the gate of FET Q1787. As the gate voltage moves positive, turn-on of the transistor is slow due to negative feedback through C1787 and the time constant of C1787, R1781 and R1780. In about 1 ms to 8 ms (depending on the setting of R1780), the drain voltage of Q1787 becomes negative enough to turn off Q1777. As Q1777 turns off, Q1774 also turns off, ending the DELAY pulse. Since the gates that start a measurement are activated by the negative-going edge of DELAY, the width of the pulse provides a delay between the application of the trigger pulse and the start of the measurement. This delay, adjusted by the operator to suit the requirements of the system, permits reed switches and other circuitry to operate and settle down before the measurement begins.

The negative-going transition at the end of DELAY clocks M1764, causing pin 7 (LOCKOUT) to go high. The high level of LOCKOUT turns on Q1785, preventing the generation of another DELAY pulse until M1764 has again been preset by INTERNAL PRINT COMMAND at the end of the measurement.

At the end of the DELAY pulse, D1781 becomes reverse biased, so the only way that C1787 can discharge and allow Q1787 to turn off is through D1788 and DISPLAY TIME control R505. This permits the setting of R505 to determine the duration of the delay generator holdoff and thus control the interval between DELAY pulses. The rate of rise at the drain of Q1787 is slowed, as C1787 discharges and Q1787 turns off, due to the negative feedback through C1787 and the long time constant of C1787-R505. The delay holdoff period ends when Q1787 turns off, enabling the delay generator to be able to generate another DELAY pulse following the release of LOCKOUT at the completion of the measurement.

If the synchronizer had been operated in triggered mode, instead of free-running mode as assumed in the foregoing description, operation of the external trigger circuit and delay generator would be as follows:

In triggered mode, TRIGGERED MEASUREMENT switch SW502 is set to the ON position, connecting the output of external trigger flipflop M1724 to the base of Q1785. Following completion of a measurement, M1724 is in the reset condition (pin 6 high, pin 7 low), having been reset by the positive-going edge of MEASURE at the beginning of the measurement sweep. Since M1764 was preset by the end of the previous measurement, LOCKOUT is low, but Q1785 is held in conduction by the high output from M1724 pin 6.

An external minus trigger applied from the control equipment through rear-panel connector J204 to pin W of P9 is

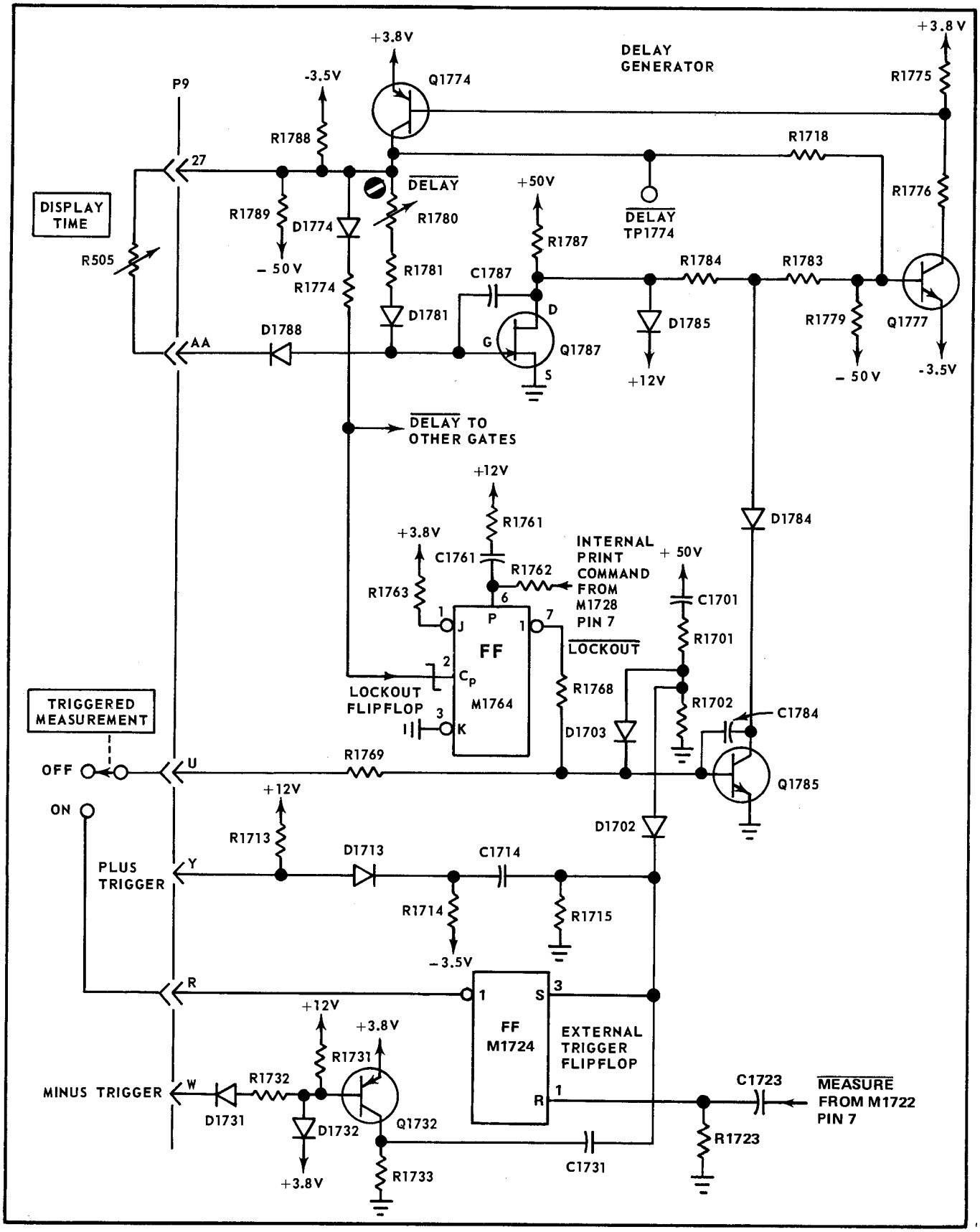


Fig. 4-26. Partial synchronizer circuit showing delay generator and external trigger circuits (synchronizer model 3-up).

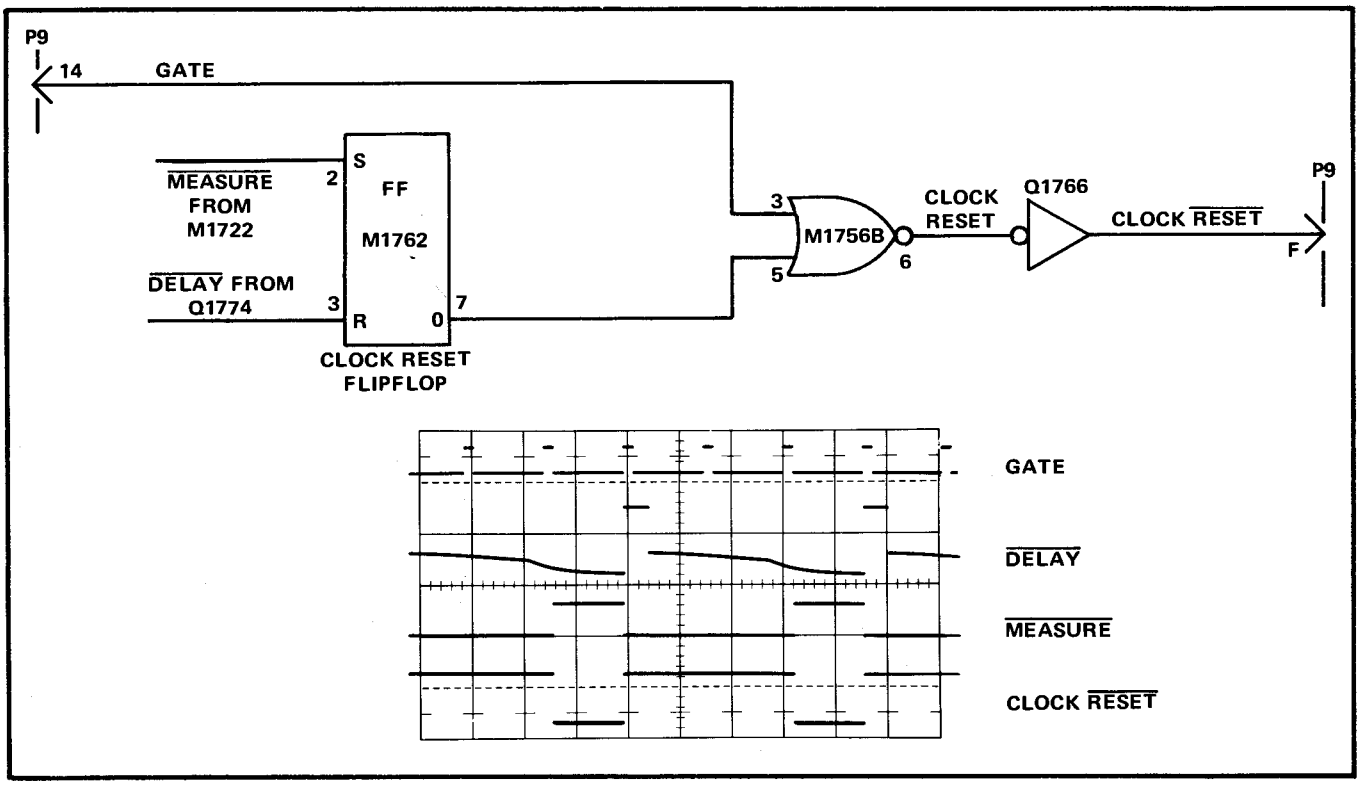


Fig. 4-27. CLOCK RESET pulse generation (synchronizer model 3-up).

inverted by Q1732, differentiated, and applied to pin 3 of M1724. (Alternatively, an external plus trigger applied to pin Y would be differentiated and applied directly to pin 3 of M1724.) The positive-going spike at M1724 pin 3 causes pin 6 to move low, turning off Q1785 to start the DELAY pulse. The remainder of the delay circuitry operates the same whether in triggered or free-running mode.

CLOCK RESET

Clock reset flipflop M1762 is set by DELAY at the start of the DELAY pulse (see Fig. 4-27), giving a high at M1762A pin 7. The high from M1762 causes the output of M1756B (CLOCK RESET) to move low and the output of inverter Q1766 (CLOCK RESET) to go high. The high level of CLOCK RESET resets the clock circuit and holds it in the reset condition until time to make the measurement.

At the start of the measurement sweep, the positive level of MEASURE resets M1762, causing M1756B pin 5 to go low. Since GATE is also low during the sweep, the output of M1756B moves high. CLOCK RESET at the output of Q1766 then goes low, releasing the clock circuit to make the measurement.

After the measurement has been completed, CLOCK RESET is restored to its high level either by DELAY or GATE (whichever comes first), resetting the clock in preparation for the next measurement.

DISCHARGE and COUNTER RESET

At the start of the DELAY pulse, discharge flipflop M1804 (see Fig. 4-28) was also placed in the set condition by the positive level of DELAY. The low output at pin 6 of M1804 enables pin 5 of M1748B, and the discharge circuit then awaits the arrival of GATE at the end of the measurement sweep. (There is usually no fixed relationship between DELAY and GATE.) When GATE goes negative, the pin 3 input of M1748B goes low and the output on pin 6 goes high. The high from pin 6 is inverted by Q1806 and the DISCHARGE pulse is coupled out through P9 pin D to the Memory circuit cards to discharge the memories.

When GATE then goes positive at the start of the memory-charging sweep, the positive level at pin 3 of M1748B causes pin 6 to go low, and the inversion through Q1806 ends the DISCHARGE pulse. The positive-going GATE transition also resets M1804, through C1801, inhibiting the pin 5 input of M1748B. DISCHARGE then remains high until the next measurement cycle.

The COUNTER RESET pulse, coupled out through R1794 and P9 pin A, is the same as the DISCHARGE pulse, except that COUNTER RESET can be inhibited by applying a low to the COUNTER RESET INHIBIT input (P9 pin 9) through rear-panel connector J202. This permits the operator to accumulate a count in the counter to perform a summing operation. COUNTER RESET INHIBIT is inverted by Q1794, keeping COUNTER RESET high, even while DISCHARGE is low. COUNTER RESET, inverted from COUNTER RESET by Q1795, resets the ÷ 8 counter and the + and − flipflops in the clock circuit at the start of the memory-charging sweep.

MEASURE, MEASURE and READY

During the memory-charging sweep, the low level of MEMORIES CHARGED through D1718 from M1718 (see Fig. 4-29)

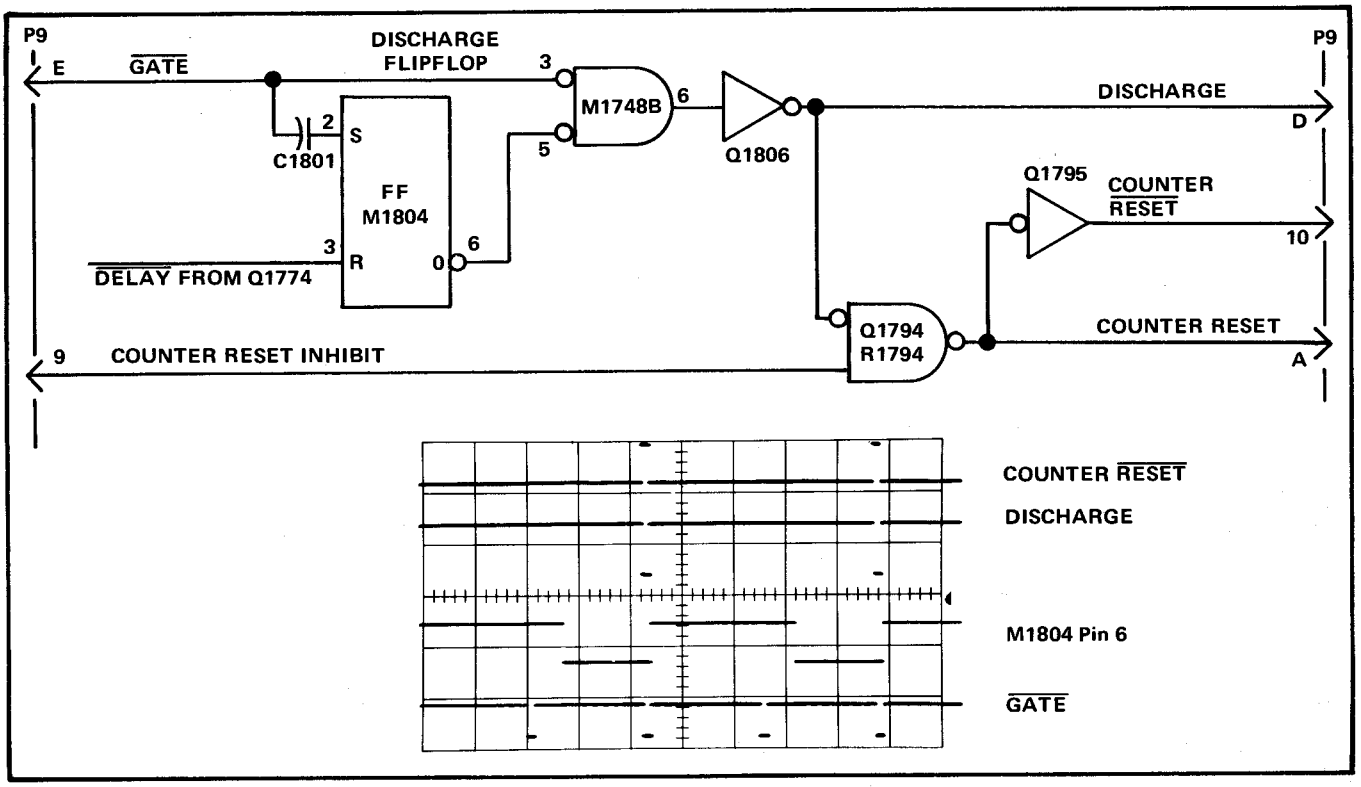


Fig. 4-28. DISCHARGE, COUNTER RESET and COUNTER RESET pulse generation (synchronizer model 3-up).

inhibits the preset input (pin 6) of measure flipflop M1720 so that M1760 cannot preset M1720 until the memories are fully charged. As the fourth memory becomes charged during the last zone, the output at pins 6 and 7 of memories charged NAND gate M1718 goes positive, reverse biasing D1718 and releasing the preset input of M1720. To prevent the positive-going transition of MEMORIES CHARGED from presetting M1720 during the memory-charging sweep, the transition is slowed down by RC circuit R1718-C1718.

Since M1762 is in the set condition and M1804 is in the reset condition at the end of the memory-charging sweep, input pins 3 and 5 of M1760 are enabled by the low outputs from the flipflops. The pin 2 input of M1760 is also enabled by the low state of DELAY at this time, so the GATE input signal at M1760 pin 1 controls the output level of M1760.

GATE is low during the memory-charging sweep, holding the output of M1760 at the high level. When GATE goes high at the end of the sweep, the output of M1760 moves low but this has no effect on the subsequent circuitry. When GATE then moves low at the start of the measurement sweep, the output of M1760 moves high momentarily, and since the preset input of measure flipflop M1720 is not inhibited by MEMORIES CHARGED at this time, the positive-going transition from M1760 through C1719 presets M1720. As M1720 is preset, its 1 output (pin 7) goes low and its 0 output (pin 5) goes high. These outputs are inverted by M1722A and B, providing the high state of MEASURE and the low state of MEASURE. The high MEASURE level, applied back to pin 2 of M1762, resets M1762, causing pin 6 to go high. This high, applied to pin 3 of M1760, causes the output of M1760 to drop back to the low level. Thus the duration of the positive output level of M1760, from the end of GATE to the reset of M1762 is very short and appears only as a spike on the waveform in Fig. 4-25.

When the measurement zone is completed (during the measurement sweep), the clock circuit generates an END pulse which is applied through P9 pin 4 to the base of Q1741 in the synchronizer circuit. The positive-going END signal is inverted by Q1741 and the low is applied to M1746A pin 1 (assuming that the Type 230 is operating in average-of-one mode). Since the pin 2 input of M1746A is also low, the output at pin 7 goes high. Pin 2 of M1748A is also low in average-of-one mode, so the high applied to M1748A pin 1 causes M1748A pin 7 to go low. The negative-going transition from M1748A clocks M1720, ending the MEASURE and MEASURE pulses.

READY (see Synchronizer schematic). When MEASURE went high at the beginning of the measurement sweep, it caused clock reset flipflop M1762 to reset, and the low output from pin 7 of M1762 enables the pin 1 input of M1770A. Since MEASURE remains high until the end of the measurement, the second input to M1770A is inhibited during the measurement, causing M1770A pin 7 to be low, and the READY lamp circuit remains inactive.

At the end of the measurement, when MEASURE goes low, the output of M1770A moves high, causing Q1771 to start to turn on the READY lamp (indicating that the Type 230 has completed the measurement). However, under the free-running conditions described previously, DELAY occurs immediately and sets M1762, causing M1762 pin 7 to go high. This high, applied to M1770A pin 1, causes M1770A pin 7 to return to the low level and end the READY signal.

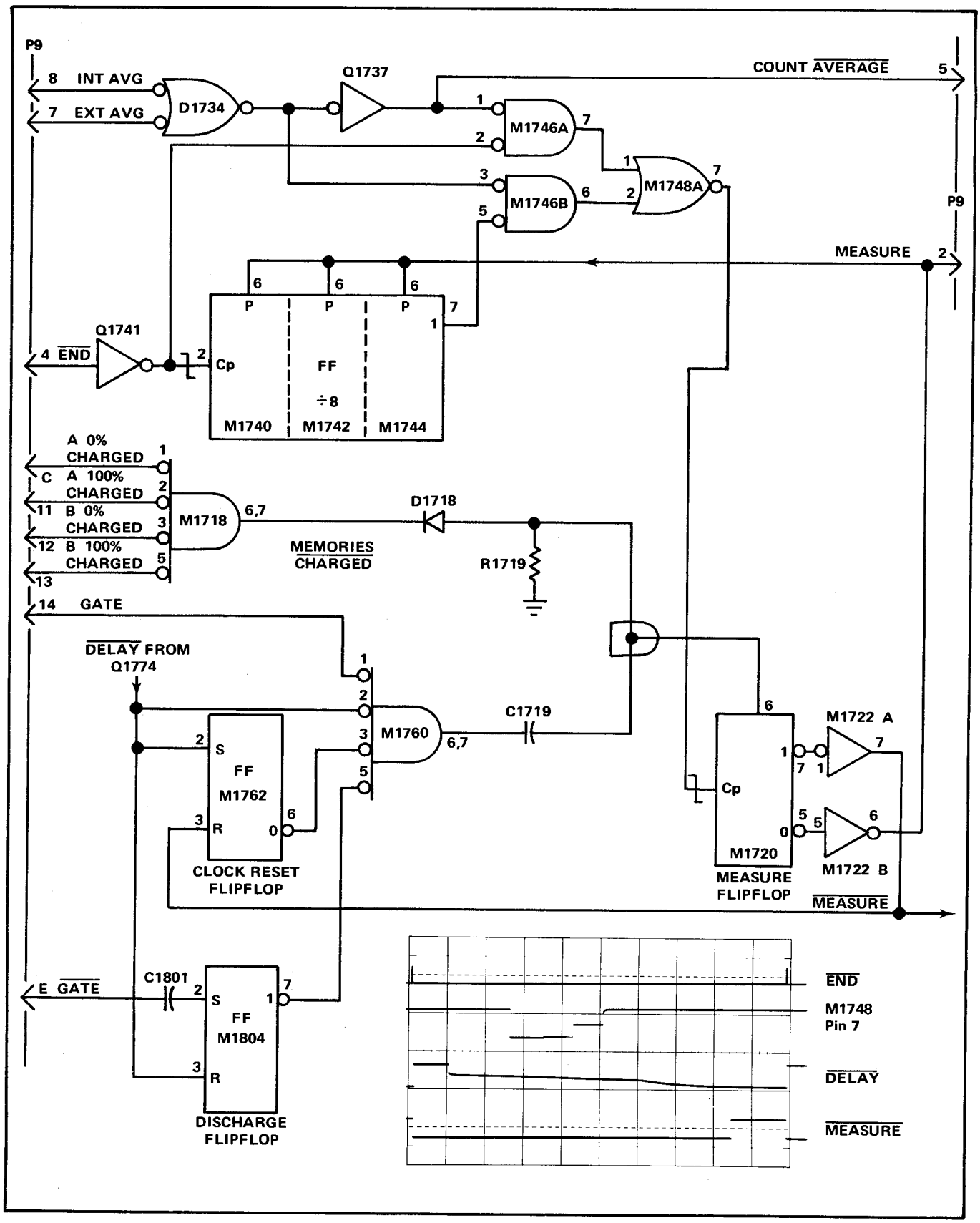


Fig. 4-29. MEASURE pulse generation (synchronizer model 3-up).

In triggered mode, or when the measurement rate is slowed down with the DISPLAY TIME control, the READY lamp remains illuminated from the end of MEASURE until the time that DELAY occurs and sets M1762.

Average-of-Eight Mode. The MEASUREMENT AVERAGING switch on the front panel of the Type 230, and a corresponding rear-panel program line, provide a means of averaging the readout of eight consecutive measurements (see Fig. 4-29). With the switch set to the 1 position (or the program line open), operation of the MEASURE pulse circuit is as previously described. In average-of-one mode, even though ÷8 counter M1740, M1742 and M1744 is clocked by each inverted END pulse, the counter is again preset by each MEASURE pulse, so that no change is ever seen at the counter output. With the switch set to the 8 position or EXT AVERAGE is programmed, the END pulses are divided by eight before MEASURE and MEASURE are generated, and eight measurements are made before the counter is preset. At the same time, the gated clock pulses are divided by eight in the clock circuit so that the measurement is divided by eight before being read out.

A low level at P9 pin 7 or 8 is applied to the pin 3 input of M1746B and is also inverted by Q1737 and applied as a high to the pin 2 input of M1746A. The high input to M1746B holds M1746B pin 7 low, inhibiting the passage of inverted END pulses through that gate. The low input to M1746B pin 3, however, enables M1746B so that the inverted END pulses routed through the ÷ 8 counter are used to clock the measure flipflop.

The positive level of MEASURE that holds the divide-by-eight counter in the preset condition prior to the beginning of measurement sweep causes output pin 7 of M1744 to be initially at the low level. When measure flipflop M1720 is preset by GATE at the start of the measurement sweep, MEASURE goes low, releasing the ÷8 counter and which starts counting inverted END pulses. At the fourth count, pin 7 of M1744 goes high, pin 6 of M1746B goes low and pin 7 of M1748A goes high. Since M1720 requires a negative-going edge for clocking, the positive-going transition from M1748A has no effect on M1720. When the count of END pulses reaches 8, the counter resets to 0 and pin 7 of M1744 goes low again. Pin 6 of M1746B then goes high and pin 7 of M1748A goes low, clocking the measure flipflop and ending the MEASURE and MEASURE pulses.

The remainder of the measurement cycle, after the end of MEASURE and MEASURE, is the same as for average-of-one mode. A single readout is provided for the averaged measurement.

REGISTER SET and PRINT COMMAND

After the measurement has been made, the count in the counters is transferred to the registers where it is held until the end of the next measurement. The control signal which commands the registers to accept the information contained in the counters is the REGISTER SET pulse.

The register set single-shot circuit consists of flipflop M1758 and NAND gate M1756A (see Fig. 4-30). The stable state of the single-shot is the reset state, in which M1758A pin 7 is low, M1758B pin 6 is high, and M1756A pin 7 (REGISTER SET) is low. The low at M1756A pin 7 is coupled back through R1757 to pin 2, enabling the flipflop. When MEASURE goes low, the negative-going edge of the pulse is coupled through C1758 to M1758A pin 1, causing pin 7 to go high and M1758B pin 6 to go low. The low at pin 1 of M1756A causes M1756A pin 7 to go high, starting the REGISTER SET pulse. REGISTER SET is inverted by M1768, providing the low level of REGISTER SET which sets the count into the registers at the end of MEASURE.

The high output at M1756A pin 7, connected back through R1757 to M1758A pin 2 and through C1757 to M1758B pin 6, resets M1758, returning the single-shot to its stable state. The time constant of R1757 and C1757 delays the reset of M1758 for about 10 μs after MEASURE goes high. M1758A pin 7 then goes low, M1758B pin 6 goes high, and M1756A pin 7 goes low, ending the REGISTER SET and REGISTER SET PULSES.

NOTE

Since the duration of DELAY is at least 1 ms and the duration of REGISTER SET is only about 10 μs, the count is set into the registers long before the DELAY pulse can start the new measurement.

The positive-going transition of REGISTER SET at the output of M1756A also triggers the print command single-shot circuit to start the PRINT COMMAND pulse, indicating that the count is being changed in the registers. (The count can be used any time that PRINT COMMAND is not high.) The PRINT COMMAND signal is used to inhibit the operation of a printer or other readout device while the count is being changed.

With pin 1 of M1728A connected to +3.8 volts and pin 3 of M1728B connected to ground, the stable state of the single-shot is the set condition, pin 7 being low and pin 6 being high. The high output at M1728B pin 6 is inverted by Q1729, holding PRINT COMMAND at the low level.

The positive-going edge of REGISTER SET is coupled through C1726 to M1728B pin 3, causing pin 6 to go low. This transition at pin 6, inverted by Q1729, is the start of the positive-going PRINT COMMAND pulse. INTERNAL PRINT COMMAND from M1728A pin 7 is connected to the preset input (pin 6) of lockout flipflop M1764, presetting the flipflop to enable the start of another DELAY pulse as previously described.

The negative-going edge at M1728B pin 6 is also applied through C1727 to pin 1 of M1728A, causing pin 7 to move high, and placing the single-shot temporarily in the reset condition.

After a delay of about 200 μs, determined by C1727 and R1727, pin 1 of M1728A returns to the high level, causing pin 7 to go low. Since the time constant of R1726 and C1726 is much less than that of R1727 and C1727, M1728B pin 3 is low at that time and M1728B pin 6 goes high, returning PRINT COMMAND to the low level.

External Hold. If the external readout equipment (such as a printer) does not operate as fast as the Type 230, the readout equipment can command the Type 230 to hold the count in the registers until the printer is ready for it. The hold signal is applied from the readout device to the EXT HOLD line at pin M of the synchronizer (see Fig. 4-30) through rear-panel connector J204. A low on P9 pin M is inverted by Q1752 and applied as a high to M1756A pin 2. This inhibits REGISTER SET by holding M1756A pin 7 at

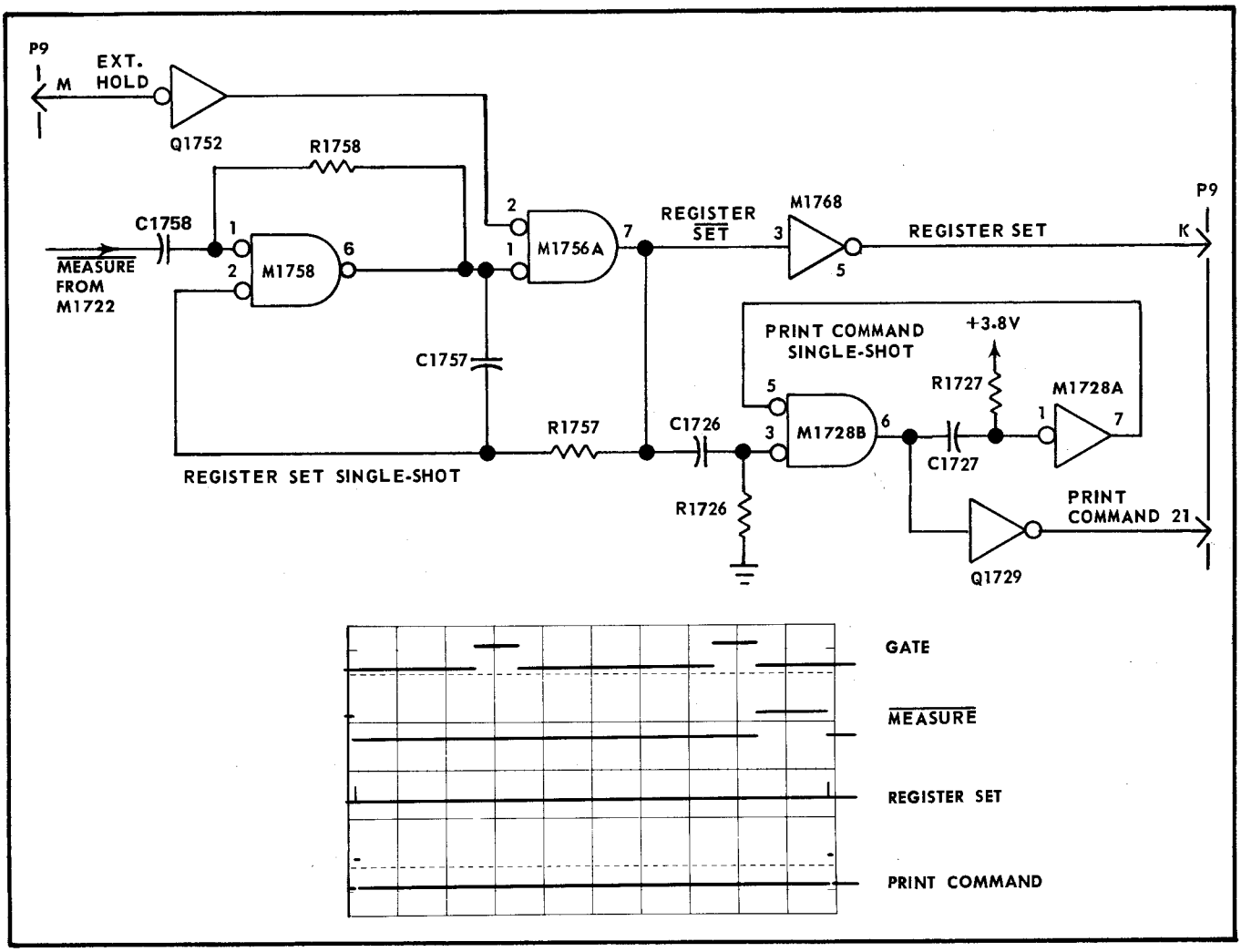


Fig. 4-30. REGISTER SET and PRINT COMMAND pulse generation (synchronizer model 3-up).

the low level, thus keeping the registers from accepting a new count and preventing PRINT COMMAND from being generated.

By inhibiting the INTERNAL PRINT COMMAND to M1764, the EXT HOLD signal also inhibits the rest of the measurement circuitry by keeping LOCKOUT high. This permits the Type 230 to be ready to proceed to the next measurement as soon as the readout equipment completes its operation. When EXT HOLD is then released, pin 2 of M1756A goes low, and if the register set single-shot has returned to its stable state, M1756A pin 7 goes high, starting REGISTER SET, REGISTER SET and PRINT COMMAND. The count in the registers can then be read out as the system proceeds to the next measurement.

High Speed Program

When using the Type 230 in a system that employs a Type 3T5 or 3T6 Sampling Sweep Unit, the time between measurements can be shortened considerably by speeding up those portions of the sweep that occur outside the zones of interest (in equivalent-time mode) and by resetting the sweep whenever its function has been accomplished.

NOTE

The Type 3T4 Sampling Sweep Unit does not have the sweep reset feature, but the unit does speed up the sweep after the sweep function has been completed.

Sweep speedup is achieved by running the sweep at a dot density of 100 dots/division during the zones of interest, then changing to 10 dots/division outside of those zones. Since the time per dot is the same in either case, the sweep runs 10 times as fast at 10 dots/division.

On the memory-charging sweep, only the memory zones are of interest; therefore, the sweep can be speeded up before the first zone and between zones, then reset after all four memories have been charged. During the measurement sweep, only the measurement zone is of interest, so the sweep can be reset as soon as the measurement is completed. Additional time is gained by holding off the sweep whenever it is not needed, thus time is not lost waiting for an unused sweep to be completed.

In order to use the high-speed functions to full advantage, the delay holdoff period should be set to minimum with the DISPLAY TIME control, and the Type 230 should be operated

in triggered mode using a trigger from the control equipment. The memory zones should be short (0.3 cm) and should be superimposed wherever posssible. A sweep rate that has the least possible holdoff time between displayed dots should be used (see the sampling-sweep unit manual for trigger holdoff), and the zones should be positioned to use minimum sweep time. If the readout equipment is not able to keep up with the Type 230 measurement rate in high-speed mode, EXTERNAL HOLD should be controlled by the readout equipment.

The high-speed program functions are selected by applying a low level to P9 pin N of the synchronizer (see Fig. 4-31) by way of rear-panel connector J204. The SWEEP SPEEDUP and SWEEP RESET control signals that results are sent to the sampling-sweep unit through P9 pins P and H. When using the Type 3T5 or 3T6 plug-in units, pins P and H are high except when the high-speed function (sweep speedup or reset) is active. When using the Type 3T4, pins P and H are negative (—12 volts) except when the high speed function is active. Buffers Q1778-Q1779 and Q1738-Q1739 act as inverters with the Type 3T5 or 3T6, and as non-inverting level-changing circuits with the Type 3T4.

Since the sweep of the sampling-sweep unit is reset at the end of the measurement zone, the start of GATE and GATE is coincident with the start of PRINT COMMAND, END, DELAY, etc. In other words, the start of the sweep holdoff period prior to the memory-charging sweep in Fig. 4-25 is moved to coincide with the start of END and DELAY, and the start of the sweep holdoff period preceding the measurement sweep is moved to coincide with the end of the last zone. The time difference is the amount of time that is saved by sweep reset. The memory-charging sweep, however, does not start until the DELAY pulse has ended, so the sweep holdoff at the start of the memory-charging sweep is extended slightly. In addition to the time saved by sweep reset, the time scale before the first zone and between zones on the memory-charging sweep in Fig. 4-25 is divided by a factor of 10 due to sweep speedup.

When using a Type 3T4 Sampling Sweep Unit, the sweep can not be reset by the synchronizer, but time can still be saved by using sweep speedup. The sweep speedup (single sweep) circuit holds off the Type 3T4 memory-charging sweep until the DELAY pulse has ended, and holds off the measurement sweep for the usual sweep holdoff period. Following each sweep holdoff, the sweep reset circuit triggers the Type 3T4 to start a single sweep.

Sweep Speedup. When not operated in high-speed mode, the high level of the HIGH SPEED PROGRAM line is inverted by M1794A and connected through D1770 to inhibit operation of sweep speedup buffer Q1778-Q1779. At this time, the dot density of the sweep is 100 dots/division. When HIGH SPEED PROGRAM is selected, the low at the input is inverted by M1794A, releasing the input of the sweep speedup buffer and allowing M1770B to control the sweep dot density.

During the memory-charging sweep, ZONE BUS at pin L of P9 goes high each time a zone occurs, and is low between the zones. ZONE is inverted by M1810A, and any time a zone is not present a high is applied to M1810B pin 3. The high causes M1810B pin 6 to move low, and since MEASURE at pin 5 of M1770B is low during the memory-charging sweep, the output at M1770B pin 6 goes high, activating the sweep speedup buffer to speed the sweep to 10 dots/division.

During the zones of the memory-charging sweep, M1810B has a low level applied to pin 3, and since CLOCK RESET at M1810B pin 5 is low at that time, pin 6 of M1810B is high. The high at M1770B pin 3 causes pin 6 to be low, disabling the sweep speedup buffer and allowing the sweep to slow to 100 dots/division. Since all four zones must be charged for each measurement, about half of the memory-charging time can be saved by superimposing the two 0% zones and the two 100% zones.

When the sweep is reset at the end of the last zone of the memory-charging sweep, the sweep speedup buffer is activated in the same way as it is between zones, but the sweep holdoff time is the same as for normal operation.

At the beginning of the measurement sweep, MEASURE at M1770B pin 5 goes high, allowing pin 6 to go low and slow down the sweep to 100 dots/division until the measurement is completed. The part of the measurement sweep prior to the measurement zone is not speeded up due to the uncertainty as to where the measurement zone will start and the loss of resolution that would result by starting the measurement at 10 dots/division.

At the end of the measurement, the sweep is again reset, MEASURE moves low and the SWEEP SPEEDUP line to the sampling sweep unit is again activated for the memory-charging sweep.

Circuit operation of the sweep speedup buffer is as follows: When using a Type 3T5 or 3T6 Sampling Sweep unit, the positive voltage in the plug-in unit holds P9 pin P at the high level whenever the sweep speedup buffer is not activated. At this time, both transistors and all three diodes in the buffer are turned off (see Synchronizer schematic). When pin 6 of M1770B goes high between zones on the ZONE BUS, the base-emitter junction of Q1778 becomes forward biased, Q1779 turns on, and D1777 becomes forward biased. Q1779 does not go into saturation, however, because of current through D1777 which holds the emitter of Q1778 only one junction more positive than the collector of Q1779. Current through the transistors is thus self-regulating. D1779 remains off, but D1778 is forward biased by current through Q1779, and pulls the output level at pin P down near ground level to produce speedup of the sweep (10 dots/division).

If a Type 3T4 Sampling Sweep Unit is used, the plug-in unit holds pin P negative whenever HIGH SPEED PROGRAM is not selected. When M1770B pin 6 goes high to cause sweep speedup, Q1778 and Q1779 turn on and D1777 becomes forward biased as described previously. D1778 is reverse biased by the negative voltage on its anode, disconnecting Q1779 from the output, but current through D1779 and Q1778 pulls the output level at pin P up near ground level to produce speedup of the sweep (10 dots/division).

Sweep Reset (Single Sweep). Instrument turn-on presets sweep reset flipflop M1790 through C1790 so that output pin 5 is high. This is the state of the flipflop for normal (not high-speed) operation. If HIGH SPEED PROGRAM is **not** selected, the high at P9 pin N is applied to pin 3, the K input of M1790, and a low is applied by inverter M1794A to pin 1, the J input of M1790 (see Fig. 4-31). When DELAY occurs, the negative-going edge at the end of DELAY is applied to

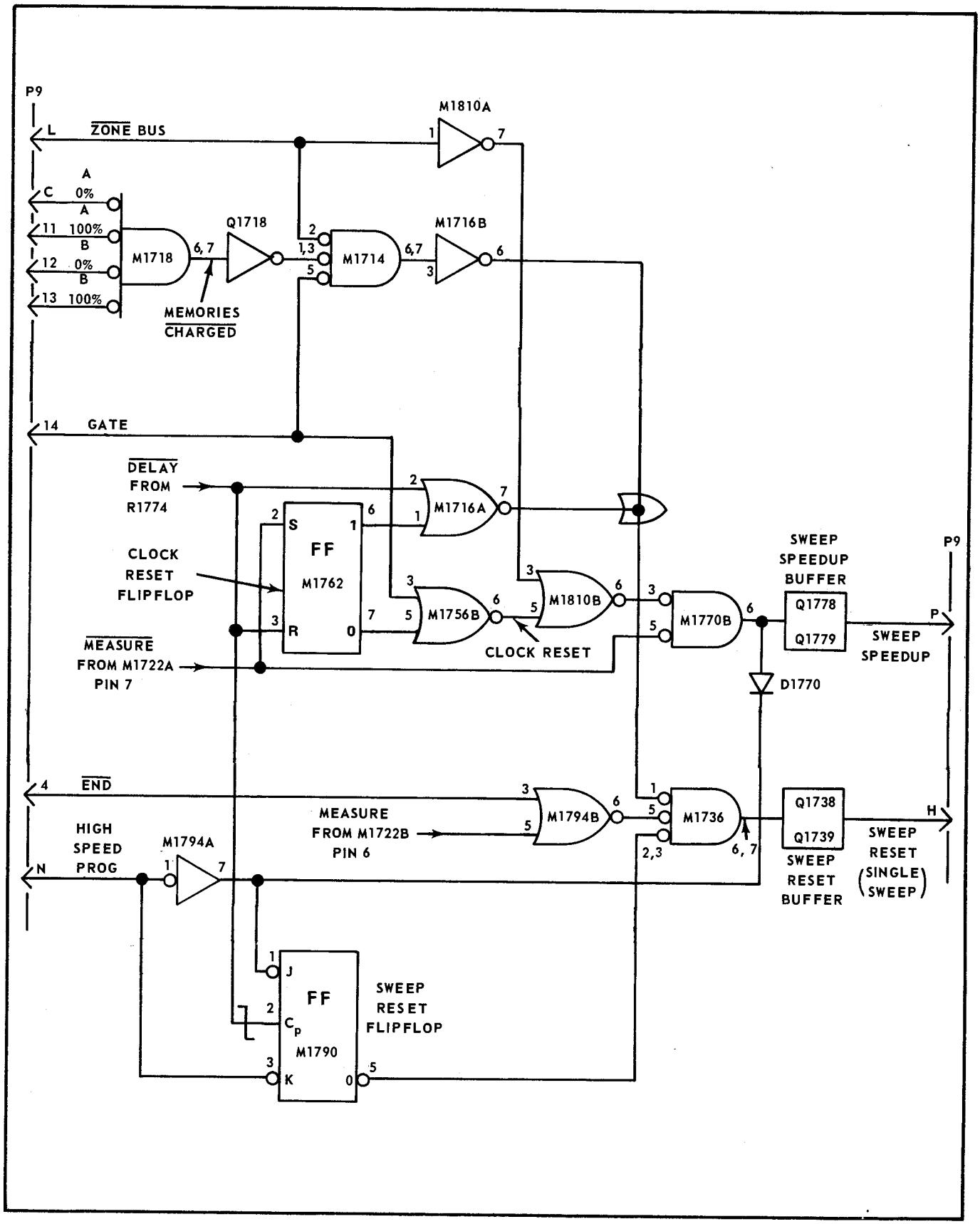


Fig. 4-31. SWEEP SPEEDUP and SWEEP RESET signal generation (synchronizer model 3-up).

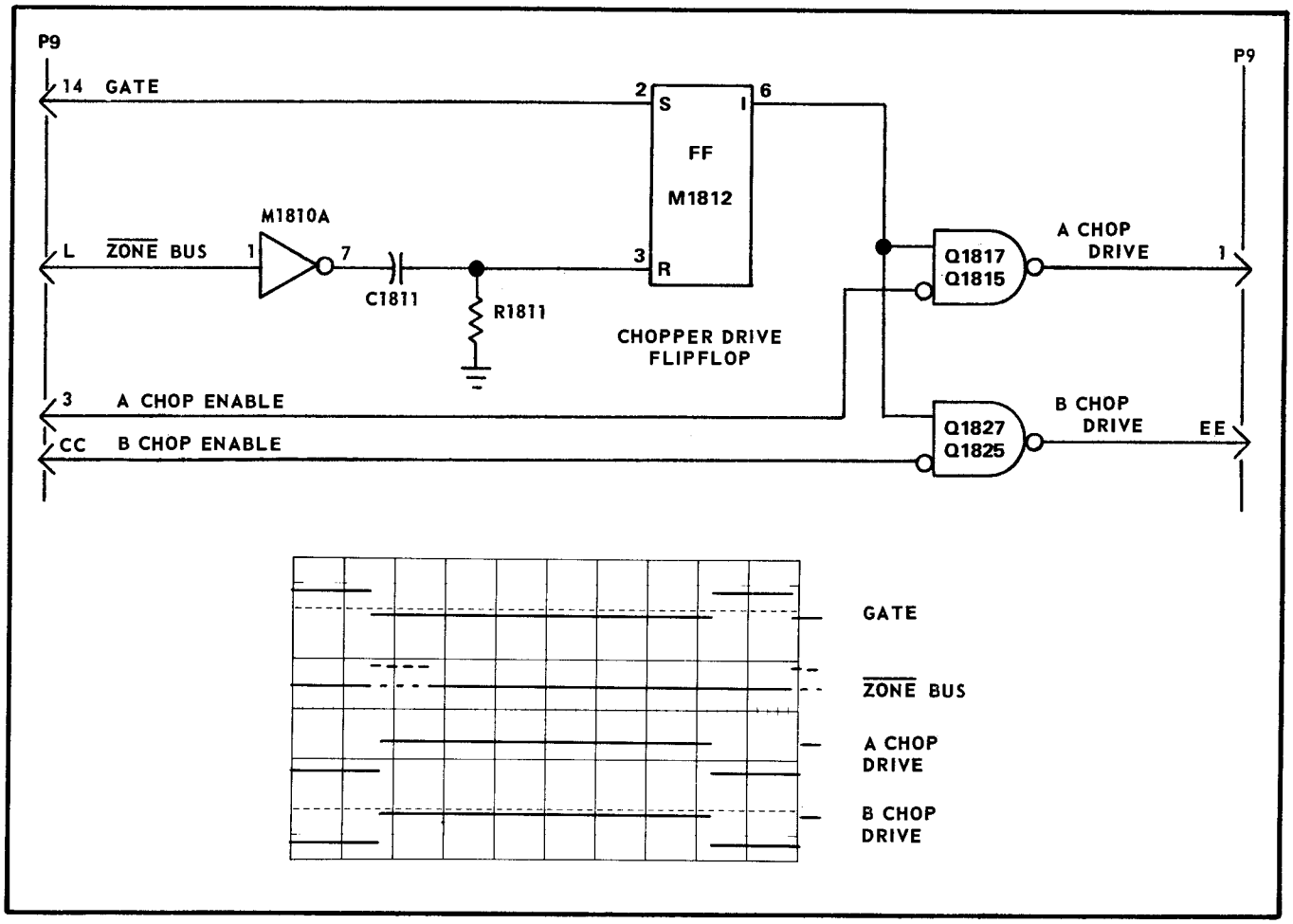


Fig. 4-32. A CHOP DRIVE and B CHOP DRIVE signal generation (synchronizer model 3-up).

the clock pulse input of M1790 but does not change the state of the flipflop, since the J input is low and the K input is high. (DELAY would have clocked the flipflop to the set condition, pin 5 going high, if the HIGH SPEED PROGRAM line had just been released after having previously been activated.) The high output of M1790 is applied to pins 2 and 3 of M1736, causing a low at M1736 pins 6 and 7 to inhibit the sweep reset buffer during normal sweep operation. The output at P9 pin H is therefore at the level set by the sampling sweep unit.

When HIGH SPEED PROGRAM is selected, a low is applied to the K input of M1790 and a high is applied to the J input. The end of the first DELAY pulse, following the end of a measurement or the arrival of an external trigger, clocks the flipflop and pin 5 moves low, enabling input pins 2 and 3 of M1736. The sweep reset flipflop then remains in the set condition, enabling pins 2 and 3 of M1736, until the HIGH SPEED PROGRAM line is released. If a measurement is in progress when the high-speed program is activated, the cycle continues until MEASURE and MEASURE end at the end of the measurement zone. The high level of MEASURE had previously reset Clock Reset flipflop M1762, thus pin 6 is high and pin 7 of M1716A is low, enabling the pin 1 input of M1736. The high level of MEASURE, applied to M1794B pin 5, causes pin 6 to move low and enable the pin 5 input of M1736. With all four inputs at the low level, pins 6 and 7 of M1736 move high, activating the sweep reset buffer to reset the sweep (at the start of MEASURE). Circuit operation of the sweep reset buffer is identical to that described for the sweep speedup buffer, except for the nature of the inputs and the purpose of the output.

When the next DELAY pulse starts, either at the end of the measurement or after the arrival of an external trigger, the memories are discharged and MEMORIES CHARGED goes low, causing a high at the output of inverter Q1718. The high, applied to pin 3 of M1714 causes pin 6 to be low, and pin 6 of M1716B to be high, releasing control of the sweep reset function to M1716A.

Clock reset flipflop M1762, which was set by the start of DELAY, has a low at output pin 6, but the low does not affect the output of M1716A because of the high level of DELAY at M1716A pin 2. When M1716A pin 2 moves low at the end of DELAY, pin 7 moves high, and the high input to M1736 pin 1 causes M1736 pins 6 and 7 to move low, releasing the sweep reset buffer and allowing the memory-charging sweep to start.

As GATE goes low at the start of the sweep, pin 5 of M1714 is enabled, and when MEMORIES CHARGED moves

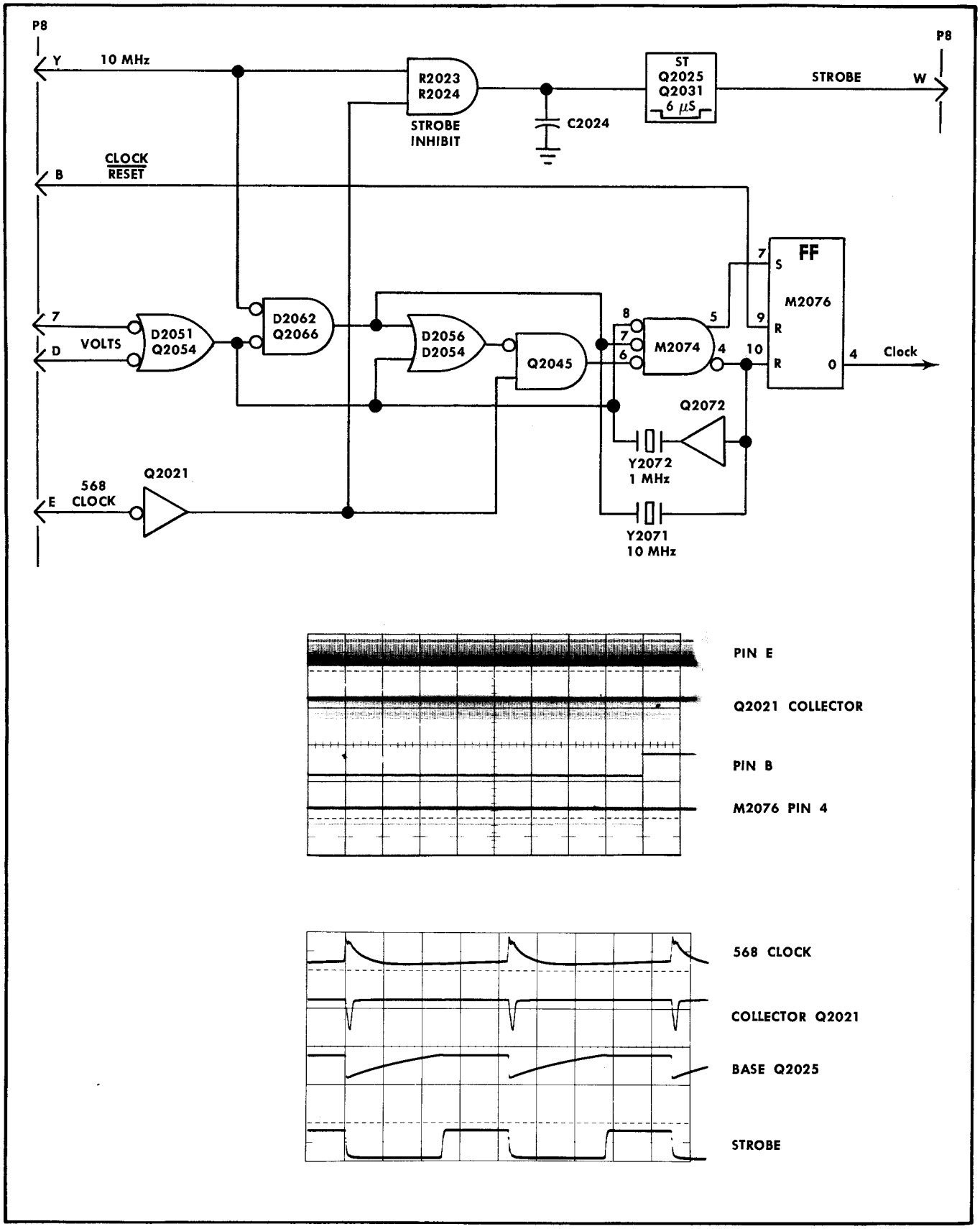


Fig. 4-33. STROBE and CLOCK pulse generation (clock models 1 and 2).

high during the last zone, pins 1 and 3 of M1714 are enabled. The sweep is not reset, however, until the end of the zone when ZONE BUS moves low. The low from ZONE BUS at M1714 pin 2 then causes pins 6 and 7 to move high and pin 6 of M1716B to move low, enabling pin 1 of M1736. This activates the sweep reset buffer and the sweep resets.

As soon as the sweep holdoff time is finished, the measure flipflop is preset by GATE and MEASURE goes low. Since END is also low at this time, the output of M1794B is high, and this high, applied to the pin 5 input of M1736, causes pin 6 to go low, inhibiting the sweep reset buffer and allowing the measurement sweep to start.

At the end of the measurement, MEASURE goes high again and the output of M1794B goes low, enabling the pin 5 input of M1736. Since the output of M1716B is still low, the output of M1736 goes high, activating the sweep reset buffer to reset the sweep. The instrument then is ready to start another measurement cycle.

A CHOP DRIVE and B CHOP DRIVE

The chopper drive circuits in the synchronizer are designed for use with measurement sytems that include signal choppers at the inputs to the vertical plug-in unit. The choppers switch the vertical inputs to ground (or other reference) at the start of the GATE pulse (see Fig. 4-32) then back to the input signals at the end of the first zone (A 0%, B 0%, A 100% or B 100%), regardless of which zone occurs first.

To enable either (or both) of the chopper drive circuits, a low is applied through rear-panel connector J204 or J201 to P9 pin 3 (A CHOP ENABLE). The low inputs enable the output chopper drivers so that they can be switched by chopper drive flipflop M1812.

When GATE goes high between sweeps, the high at pin 2 of M1812 causes the flipflop to move to set condition, with pin 7 going low and pin 6 going high. The high at pin 6 is applied to both of the output chopper drivers so that the driver that is enabled provides a low output through P9 pin 1 or pin EE and rear-panel connector J204 to the chopper drive unit, switching the input to the reference level.

When the first zone occurs, the high on ZONE BUS is inverted by M1810A, but has no effect on M1812B. At the end of the first ZONE pulse, the output on M1810 pin 7 goes high and the differentiated positive-going pulse resets M1812. Pin 6 of M1812 goes low, causing the chopper driver outputs to move high, and the chopper drive unit switches the input back to the signal. M1812 then remains in the reset state and the input remains connected to the signal until the next GATE pulse arrives.

CLOCK CIRCUIT CARD

The Clock circuit card receives start and stop information from the start and stop comparators. When the start comparator makes a comparison, the Clock circuit card gates the clock pulses on. The stop comparator comparison ends the gate, shutting off the clock pulses. Since the number of clock pulses that occur during the gated time is proportional to the time between the start and the finish of the measurement, the clock pulses can be counted to digitize the measurement.

The Clock circuit card provides the digital measurement information to the counters in the form of a burst of clock pulses. When the Type 230 is used in an equivalent-time sampling system and is set to make time measurements, the clock pulses are derived from the time base unit's slewed sampling strobe pulse. When the Type 230 is used in a real-time sampling system and is set to make time measurements, the clock pulse burst is derived from the clock output of the time base unit or from a crystal-controlled 10 MHz oscillator on the Clock circuit card. If the Type 230 is set to make a voltage measurement, the clock pulse burst are derived from the crystal-controlled 1 MHz oscillator on the Clock circuit card.

In addition to providing a clock burst output to the Counter circuit board, circuits on the Clock circuit card determine whether a measurement result is positive or negative and provide this information to the readout circuitry. The card also provides a MEASURE ZONE signal to the CRT intensification circuitry which causes the trace to be intensified over the portion of the trace in which the time measurement takes place. The Clock circuit card also generates strobe pulses which are applied to the Memory circuit card, and the END signal which informs the Synchronizer circuit card that the measurement has ended.

Clock Generator and Memory Strobe Circuits

The Type 230 makes a measurement by counting the number of clock pulses that occur in a given interval of time. When making a time measurement the clock pulses are translated directly into a time reading. In making a voltage measurement the number of clock pulses that occur during the time it takes a linear voltage ramp to rise from the measurement start point to the measurement stop point translated into a voltage reading. The clock generator circuit on the Clock circuit card provides the required type of clock signal for the various operating modes of the Type 230/568 measurement system.

The possible operating modes of the clock generator circuit are as follows:

1. When using a sampling time-base unit such as the Type 3T4 for making time measurements, the slewed pulse is used as the clock. The clock generator circuits merely shape the clock signal from connector P8 pin E and route it to the other circuits.

2. When using the Type 3B2 real-time time-base unit for time measurements, the clock from the Type 3B2 is used on the ranges where a clock is available. When the Type 3B2 Digital Resolution switch is in the .1 μs position, the 10 MHz clock is generated on the Clock circuit card by the clock generator circuits.

3. When the measurement program calls for a voltage measurement, a ground to either P8 pin 7 or pin D causes the Clock circuit card clock oscillator to generate a 1 MHz clock signal.

Models 1 and 2

Time Measurement, Equivalent Time Mode. In this mode of operation, P8 pins 7, D, and Y are left floating (see Fig. 4-33). The output of transistor Q2054 is low, as is the output of the NAND gate consisting of diode D2062 and transistor Q2066. The two low outputs disable both the os-

cillator feedback paths (pins 7 and 8) of M2074. The low outputs are also applied through OR gate diodes D2054 and D2056 and AND gate transistor Q2045, biasing it off.

When making time measurements with an equivalent-time sampling system, the clock pulse (slewed pulse) from the time-base unit is applied to P8 pin E. From pin E, the clock pulse is applied to transistor Q2021 which inverts and amplifies the clock signal input. The output of Q2021 is applied through R2045 to M2074 pin 6. Q2045 is cut off and does not inhibit signal passage. The single-ended input into M2074 is converted into a push-pull output which drives squaring flipflop M2076. The CLOCK $\overline{\text{RESET}}$ signal applied to M2076 pin 9 inhibits the clock pulses until the GATE signal has reset the three-dot delay circuits. Once the CLOCK $\overline{\text{RESET}}$ pulse ends, M2076 starts passing constant amplitude, properly shaped clock pulses to clock NAND gate M2078, whose other inputs will be described later.

Time Measurements, Real-Time Mode. When making time measurements in a real-time system, a clock signal generated in the time-base unit is applied through the Type 568 to P8 pin E in the Type 230. When the clock rate is 1 MHz or less, operation of the clock generator circuit is the same as for equivalent-time sampling.

If the Type 3B2 is used as the time base unit and the Type 3B2 Digital Resolution switch is set to .1 μs, no clock signal is sent from the Type 3B2. In this situation the .1 μs position of the Digital Resolution switch applies a negative voltage to P8 pin Y. The voltage on pin Y is anded in the NAND gate consisting of diode D2062 and transistor Q2066 with the output of the NOR gate consisting of diode D2051 and transistor Q2054. Since both pins D and 7 are high, the output of the NOR gate is low. With both of its inputs low, the output of the NAND gate goes high. The high output from the NAND gate unclamps the feedback path from M2074 pin 4 through 10-MHz crystal Y2071 and M2074 pin 7. Integrated circuit M2074 now becomes a 10 MHz oscillator. The output of M2074 is squared up by M2076 and the internally generated clock pulse is used for time measurements.

Voltage Measurement Mode. Setting the Type 230 to make a voltage measurement applies ground to P8 pin 7 (or D when externally programmed). With a ground on pin 7, the output of the NOR gate consisting of diode D2051 and transistor Q2054 goes high. The high output of the NOR gate causes the output of NAND gate consisting of diode D2062 and transistor Q2066 to go low and inhibit the 10 MHz feedback path of M2074. At the same time, the high output of the NOR gate removes the clamp from the 1 MHz feedback path from M2074 pin 8 (transistor Q2072 provides fast turn-on time for Y2072). The 1 MHz output of M2074 is applied to squaring flipflop M2076 and thence to the user circuits as previously explained.

Strobe Generator

When making time measurements where the clock input to P8 pin E is 100 kHz or less, the Clock circuit card generates a 6 μs-wide strobe pulse which is applied to the memories. The input clock signal is applied to the input of a Schmitt Trigger circuit consisting of transistors Q2025 and Q2031 and associated circuit elements. At clock rates above 100 kHz, the circuit locks up and delivers a low voltage level to the memories at J8 pin W.

Model 3-up

Time Measurement, Equivalent Time Mode. In this mode of operation, P8 pins 7, D, and Y are left floating (see Fig. 4-34). The output of Q2054 is low, as is the output of the NAND gate consisting of diode D2062 and transistor Q2066. The two low outputs disable both of the oscillator feedback paths (pins 7 and 8) of M2074. The low outputs are also applied through OR gate diodes D2054 and D2056 to AND gate M2045, enabling one of its inputs. The other inputs to M2045 are 568 CLOCK and STROBE from the collector of transistor Q2031. The clock input to M2045 is enabled for the negative duration of 568 CLOCK. The strobe from Q2031 activates M2045 approximately 2 microseconds after each clock pulse, as explained in the following paragraphs.

When making time measurements with an equivalent-time sampling system, 568 CLOCK (slewed pulse from the time-base unit) is applied to P8 pin E. From pin E, the clock pulse is applied to the base of transistor Q2021 which inverts and amplifies the pulse. The negative pulse from the collector of Q2021 is coupled through capacitor C2022, and clipped by diodes D2022 and D2021 to provide a pulse ranging from +0.6 V to −4.1 V in total excursion. The pulse from the clipping diodes is applied to the cathodes of diodes D2023 and D2024. Both diodes become forward-biased momentarily, charging capacitors C2023 and C2026 in negative direction. The negative charge on the two capacitors simultaneously cuts off transistors Q2025 and Q2029, both previously held in conduction. The positive level at the collector of Q2025 enables the base of transistor Q2031. Transistor Q2029 remains cut off for about 2 microseconds, the time for C2026 to discharge through resistor R2026. When Q2029 regains conduction, its collector forward biases Q2031, whose collector begins the negative excursion of STROBE.

Due to the larger values of C2023 and R2023 at the base of Q2025, it takes about 7 microseconds for C2023 to discharge sufficiently for Q2025 to regain conduction. When Q2025 returns to conduction, its collector disables the base of Q2031, whose collector returns positive, ending the negative excursion of STROBE. The output of Q2031 is connected to M2045 to activate that gate, and also leaves the Clock circuit card at J8, pin W, to control the memories. Transistor Q2035 is cut off and does not affect STROBE except during real-time operation (Type 3B2).

The delayed clock output of M2045 is differentiated and applied to M2074 pin 6. The single-ended input into M2074 is converted into a push-pull output which drives squaring flipflop M2076. The CLOCK $\overline{\text{RESET}}$ signal applied to M2076 pin 6 inhibits the clock pulses until the GATE signal has reset the three-dot delay circuits. Once the CLOCK $\overline{\text{RESET}}$ pulse ends, M2076 starts passing constant amplitude, properly shaped clock pulses to NAND gate M2078 and to the three-dot delay circuits.

Time Measurement, Real-Time Mode (TYPE 3B2). If the Type 3B2 is used as the time-base unit, the 10 MHz ENABLE input at P8 pin Y holds the STROBE output at P8 pin W low for all modes of operation of the Type 3B2. When the Type 3B2 Digital Resolution switch is set to any position except .1 μs, the Type 230 receives clock pulses at P8 pin E, and a positive level at P8 pin Y holds transistor Q2035 in conduction. The collector of Q2305 holds STROBE low. The positive level from pin Y also holds transistor Q2066 cut off, which enables one input of M2045. Another input to M2045

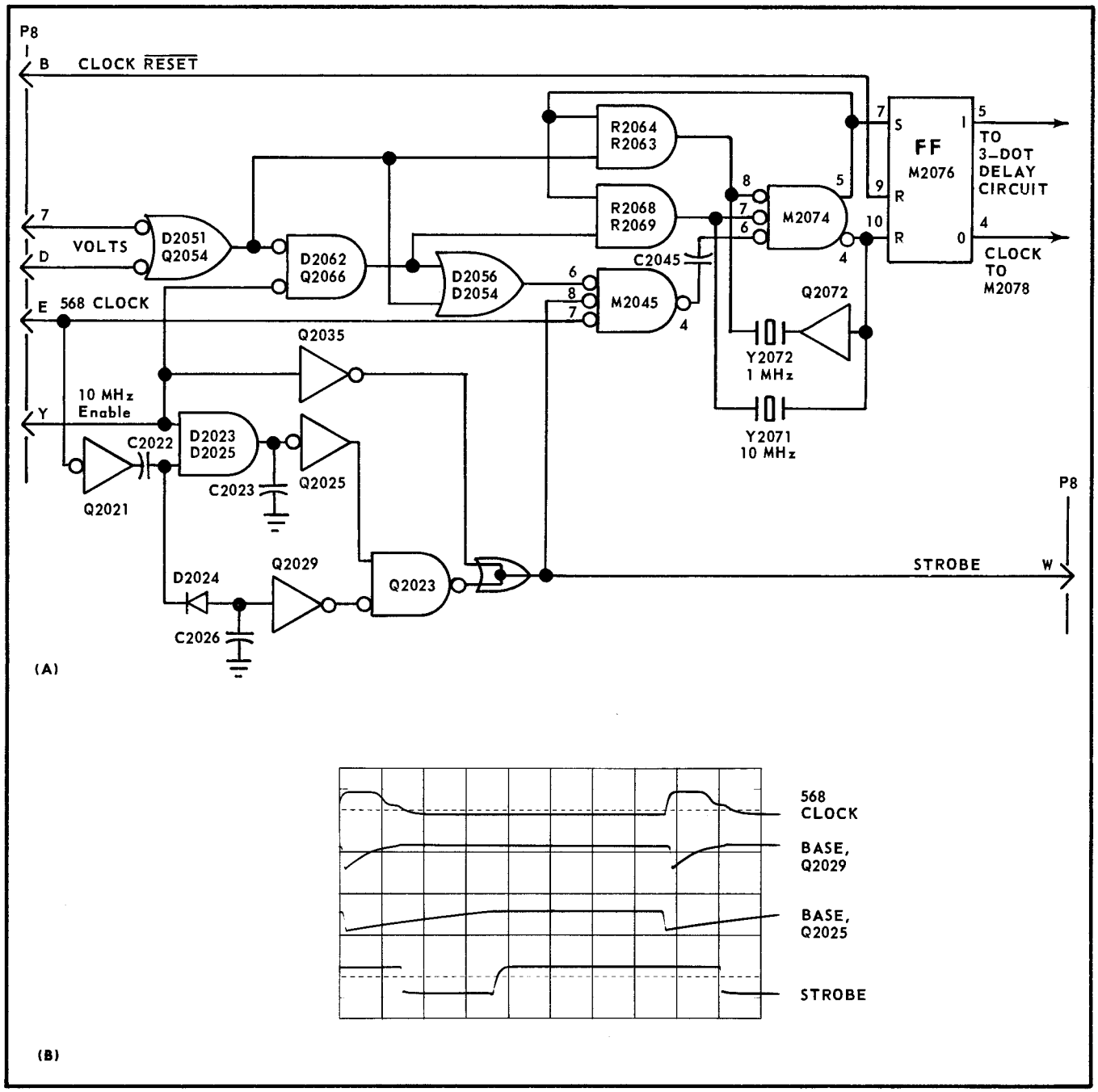


Fig. 4-34. STROBE and CLOCK pulse generation (clock model 3-up).

is enabled by the constant low from STROBE, so 568 CLOCK is allowed to control the gate. The low from the collector of Q2066 also disables M2076 pin 7, the 10 MHz feedback line for the internal clock. The other unused feedback line to M2074 (pin 8) is held low through diode D2063 by the off condition of transistor Q2054.

When the Type 3B2 Digital Resolution switch is placed in the .1 μs position, 568 CLOCK is disconnected and P8 pin Y moves from a positive voltage to about —10 volts. A 1 MHz clock signal is superimposed on the negative level at pin Y, but the signal is not used by the Type 230. The negative level from pin Y cuts off Q2035 and Q2025, and STROBE is still held in the low state. Transistor Q2066 is turned on by the low from P8 pin Y, and its collector moves high, locking out pin 6 of M2045. This inhibits any stray noise from the open 568 CLOCK line. The high at the collector of Q2066 also enables pin 7 of M2074, setting the internal 10 MHz clock generator into operation. Integrated circuit M2074 now delivers a 10 MHz signal to M2076 for time measurements.

Voltage Measurement Mode. Setting the Type 230 to make a voltage measurement applies ground to P8 pin 7 (or D when externally programmed). With a ground at pin 7, the output of NOR gate D2051 and Q2054 goes high, in-

hibiting M2045 through OR gate diode D2054 to lock 568 CLOCK out of the Type 230 clock generator circuit. The high output of the NOR gate causes the output of NAND gate D2062 and Q2066 to go low and inhibit the 10 MHz feedback path of M2074. At the same time, the high output of the NOR gate removes the clamp from the 1 MHz feedback path from M2074 pin 8. (Transistor Q2072 provides fast turn-on for Y2072.) The 1 MHz output of M2074 is applied to squaring flipflop M2076 and thence to the user circuits as previously explained. For voltage measurements as for time measurements, 568 CLOCK still generates STROBE for equivalent time operation, and STROBE is still low during Type 3B2 real time operation.

Three Dot Delay Circuits

Since the comparators can be triggered by noise spikes whose amplitude is equal to or greater than the comparison voltage, some means must be provided for negating comparisons made on noise. The Clock circuit card contains two three-dot delay circuits (one for each comparator) which enable the Type 230 to distinguish between comparisons made on signals and those made on noise or a misplaced sample. The three-dot delay circuits prevent the clock burst from being sent to the counters until three consecutive comparisons, coincident with clock pulses, have been made. Noise spikes or misplaced samples are generally of random spacing; thus, the three-dot delay circuits almost eliminate the chance of a clock burst being gated on by a comparison made on noise. The operation of the two delay circuits is similar; therefore, only the start comparator's delay circuit will be described.

Start First + Slope Mode. For purposes of explanation assume that the Type 230 is set to start the measurement on the first positive slope of the displayed waveform. In this mode of operation P8 pins A, C, 1 and 3 are high (see Fig. 4-35). The outputs of OR gate diodes D2091 and D2111 are high. Between sweeps the GATE signal goes positive and sets the three-stage shift register consisting of JK flipflops M2100, M2102, and M2108. All three flipflops have highs on their pin 5 outputs, lows on their pin 4 outputs. Whenever GATE goes high, CLOCK $\overline{\text{RESET}}$ also goes high and prevents flipflop M2076 from passing clock pulses until the start of the measurement sweep. The input from the start comparator on P8 pin 2 is high until a comparison is made. The high from P8 pin 2 and the high from D2091 are inverted by M2090B and Q2095, appearing as lows at the inputs of NAND gate M2098A. The output of M2098A goes high and is applied as an inhibiting input to M2100 pin 10. The high output of M2098A is also inverted by inverter M2094B and is applied as a low to negative-logic AND gate M2104 pin 6. The other two inputs to M2104 are the lows from M2100 and M2102 pins 4, so the output of M2104 goes low, removing the inhibiting voltage from flipflop M2108 pin 10. These are the conditions that exist at the beginning of the measurement sweep. The count in three-dot delay circuits is 0-0-0.

When the GATE signal ends and MEASURE goes positive, CLOCK $\overline{\text{RESET}}$ goes negative and removes the inhibiting input from M2076 pin 9. Flipflop M2076 starts passing clock pulses to the flipflop in the three-dot delay counter. Flipflop M2100 and M2102 cannot toggle on the clock pulses since they have been set by the positive portion of the GATE pulse and they are receiving highs on pin 10 which inhibits any signal applied to pin 9. However, M2108 pin 10 is receiving a low from M2104, so M2108 toggles. The output on M2108 pin 4 goes high and the output of M2090A now goes low. The count in the three-dot delay circuit counter is now 1-0-0 (digital 4).

The clock pulses from M2076 have no further effect until the start comparator makes a comparison. When the start comparator makes a comparison, the input on P8 pin 2 goes low. The low on P8 pin 2 is inverted by M2090B which causes the output of M2098A to go low. The low output of M2098A removes the inhibiting input from M2100 pin 10 and M2100 switches on the next clock pulse. At the same time, the low output of M2098A is inverted by M2094B. The high output of M2094B pin 5 applies an inhibiting voltage to M2100 pin 7 and removes the activating input from M2104 pin 6. The output of M2104 pin 4 goes high and applies an inhibiting input to M2103 pin 10. Since the output of M2106 is also high, M2108 is inhibited on both its J and K inputs. When M2100 switches on the first clock pulse following the firing of the start comparator, its output on pin 5 goes low, removing the inhibiting input from M2102 pin 10. The count in the counter is now 1-0-1 and the circuit is ready for the next clock pulse.

On the second clock pulse after the firing of the start comparator M2102 toggles. The output of M2101 pin 5 goes low. Since M2106 is now receiving lows from M2098A pin 6, M2100 pin 5, and M2102 pin 5, the output of M2106 goes low and removes the inhibiting input from M2108 pin 7. The second clock pulse from M2076 has changed the count in the counter to 1-1-1.

With the arrival of the third clock pulse, M2108 toggles. The output on M2108 pin 4 goes low and the output on M2108 pin 5 goes high. The count in the counter has changed to 0-1-1. Since M2110 is being held in set by the output of D2111, it cannot toggle. However, the low output from M2108 pin 4 again activates NAND gate M2090A. The output of M2090A goes high and toggles flipflop M2120.

The operation of the three-dot circuit just described assumes that the start comparator made a comparison on a valid signal. If the comparison was made on a noise pulse less than three clock pulses long, the start comparator switches back and applies a high input to P8 pin 2. NAND gate M2098A again delivers a high input to M2100 pin 10 and the clock pulses toggle the flipflops back to a count of 1-0-0. The start comparator must remain fired for at least three clock pulses before the three-dot delay counter will deliver a usable output pulse.

Start Second + Slope Mode. If the measurement is set to start on the second slope, the output from OR gate diode D2111 is low. The low output from D2111 removes the set input from flipflop M2110 and M2110 is reset by the CLOCK $\overline{\text{RESET}}$ pulse which occurs at the beginning of the measurement sweep. With M2110 reset, its output on pin 4 is high, the output of pin 5 is low. As previously explained, M2108 toggles with M2108 pin 5 going high when a valid comparison has been made on the first positive slope. The positive-going output on M2108 pin 5 toggles M2110 since the inhibit signal from D2111 is removed in second slope operation. When M2110 toggles, its output on pin 4 goes low. When the start comparator again makes a valid comparison on the second slope of the displayed signal, M2108 again toggles and in turn toggles M2110. The output on M2110 pin 4 goes high and toggles M2120.

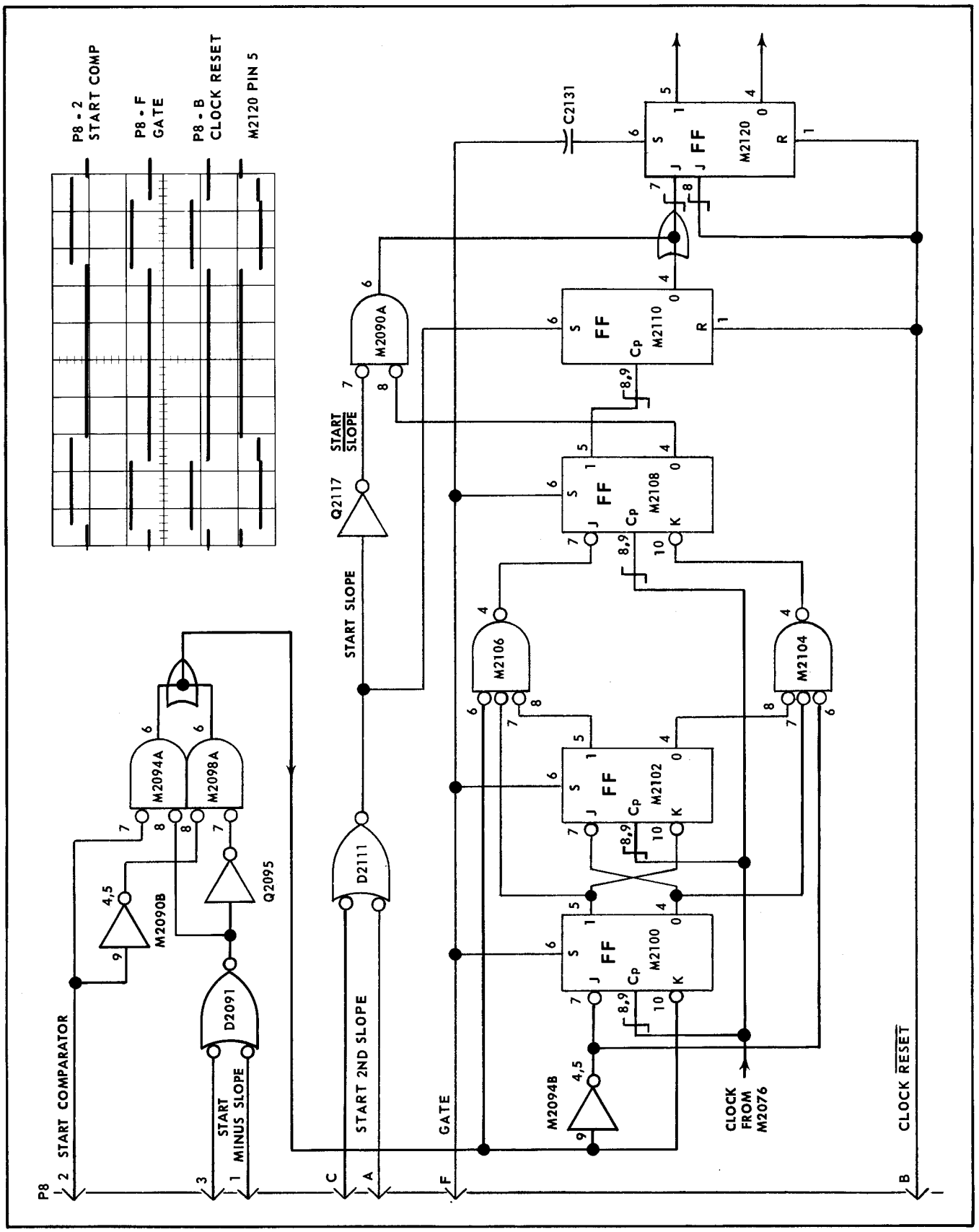


Fig. 4-35. 3 dot delay circuit logic.

Plus or Minus Slope Gating Circuits

Since the polarity of the signal input from the comparators on P8 pins 2 and 21 can be either positive or negative, the Clock circuit card contains inverters and gates to provide the three-dot delay circuits with the required inputs regardless of the input polarity. Taking the start comparator input on P8 pin 2 as an example, the gates and inverters operate as explained in the following paragraphs.

Assuming that the start comparator is set to switch on the first positive slope, the input on P8 pin 2 is high prior to the time the first comparison is made. The high input on P8 pin 2 is inverted in M2090B and is applied as a low to NAND gate M2098A pin 8. Since neither pins 1 or 3 of P8 are grounded in this mode of operation, there is a high at the base of inverter transistor Q2095 and it also delivers a low to M2098A pin 7. With two lows on its input, M2098A delivers a high to the phantom OR gate at its output. The high at the output of the phantom OR gate is applied to flipflop M2100 pin 10 and to inverter M2094B pin 9. The low output of M2094B is applied to M2100 pin 7.

If the start comparator is set to switch on the first negative slope, the input on P8 pin 2 is low prior to the time the first comparison is made. The low input on P8 pin 2 is applied to NAND gate M2094A pin 7. Since either pin 1 or pin 3 of P8 is grounded in this mode of operation, there is a low at the output of OR gate diode D2091. The low output of D2091 is applied to M2094A pin 8. With two lows on its inputs, M2094A delivers a high to the phantom OR gate at its output as previously explained. Now, when the start comparator makes a comparison, its output goes high. The high input on P8 pin 2 turns off M2094A. Since M2098A is already held off by the output of Q2095, the outputs of M2094A and M2098A to the phantom OR gate are low. The three-dot delay circuit now operates as previously explained.

Clock Gating Circuits

Assuming the start comparator holds the comparison for 3 consecutive clock pulses on the first positive slope, M2108 toggles on the third clock pulse as previously explained. The output on M2108 pin 4 goes low, activating NAND gate M2082B. Each time the clock pulse goes high, the positive-going transition is applied to M2120 pin 7, causing the flipflop to toggle. The output on M2120 pin 5 goes high. When M2120 pin 5 goes high, it applies a high to M2172 pin 8 and causes the MEASURE ZONE signal to go low. The low MEASURE ZONE signal is applied to M2078 pin 6, and assuming that all the other inputs to M2078 and Q2079 are low, M2078 starts passing the clock pulses to NAND gate M2082B. Each time the clock pulse goes high, the output of M2078 pin 5 goes low, enabling NAND gate M2082B pin 9. If P8 pin 13 (COUNTER $\overline{\text{AVERAGE}}$) is low, M2082B is activated and passes clock pulses to flipflop M2018 pins 8 and 9. If either pin 10 or pin 19 of P8 is grounded (HORIZ ÷ 2), M2018 operates as a flipflop and gives one clock pulse output for each two clock pulses in. If both P8 pin 10 and pin 19 are ungrounded, the feedback path from M2018 pin 5 to M2018 pin 1 through resistor R2018 converts M2018 into a single-shot. In single-shot operation, M2018 resets itself between clock pulses, then switches on each clock pulse, delivering one clock pulse out for every clock pulse in.

Plus and Minus Indicator Drive Circuits

At the same time that M2078 pin 4 goes low (as described in the preceding paragraph), NAND gate M2124B is receiving a low from M2120 pin 4. The two lows on its input cause M2124B pin 5 to go high. The high output from M2124B pin 5 sets flipflop M2126. The output of M2126 pin 6 goes low and is applied to the + register flipflop on the Counter and Readout circuit board.

If the stop comparator fires before the start comparator, M2172 still delivers a low output to M2078 pin 6. Assuming all other inputs to M2078 are satisfied, M2078 starts passing clock pulses out through M2078 pin 4. Since M2120 has not yet been toggled by the start comparator, its output on pin 5 is low and enables NAND gate M2124A. When M2078 pin 4 goes low on the first gated clock pulse, the output of M2124A pin 6 goes high and sets flipflop M2128[3], sending a low to the − (minus) storage register on the Counter and Readout circuit board. Now, when the start comparator fires and switches M2120, the high output on M2120 pin 5 ends the MEASURE ZONE and thereby closes NAND gate M2078. Pin 4 of M2078 goes high and removes the enabling input from NAND gate M2124B.

Measure Zone Start and Stop Flipflops

Between sweeps, measure zone start flipflop M2120 (see Fig. 4-36) and measure zone stop flipflop M2170 are set by the positive-going edge of the GATE pulse applied through capacitor C2131 to pin 6 of the flipflops. At the end of the positive portion of the GATE pulse, the CLOCK $\overline{\text{RESET}}$ pulse (generated by the Synchronizer circuit card) is applied to pins 1 and 8 of the two flipflops. The CLOCK $\overline{\text{RESET}}$ pulse resets the flipflops, causing their output pins 5 to go low and pins 4 to go high. During the memory sweep CLOCK $\overline{\text{RESET}}$ stays high and the flipflops remain reset. When CLOCK $\overline{\text{RESET}}$ goes negative at the start of the measurement sweep, the positive voltage is removed from pins 1 and 8 of the flipflops and M2120 and M2170 are free to toggle when they receive a positive-going input on pin 7.

With the measure zone start and stop flipflops reset as explained in the preceding paragraph, the low outputs from M2120 and M2170 pins 5 enable both inputs to NAND gate M2172A. The output of M2172A goes high, generating the positive portion of the MEASURE ZONE signal. The output of M2172A on pin 6 goes high and is applied as an inhibit signal to NAND gate M2078 pin 6. No clock pulses can pass through M2078 until this inhibit signal is removed.

When the start comparator's three-dot delay circuit delivers a high output as previously explained, the positive-going edge applied to M2120 pin 7 toggles the flipflop. The output on M2120 pin 5 goes high. The high output from M2120 pin 5 is applied to M2172 pin 8 and causes the output of M2172A pin 6 to go low. Since M2172B pin 10 is receiving a high from M2170 pin 4, both inputs to the phantom OR gate at the output of M2172 are low and MEASURE ZONE is thus low. The low MEASURE ZONE is applied to NAND gate M2078 pin 6 and gates on the clock burst. The clock burst lasts until the stop comparator's three-dot delay circuit toggles M2170.

[3]Flipflops M2126 and M2128 are rated as 2 MHz devices. Capacitors C2126 and C2128 serve to integrate the 10 MHz clock and permit M2126 and M2128 to switch to 10 MHz signals.

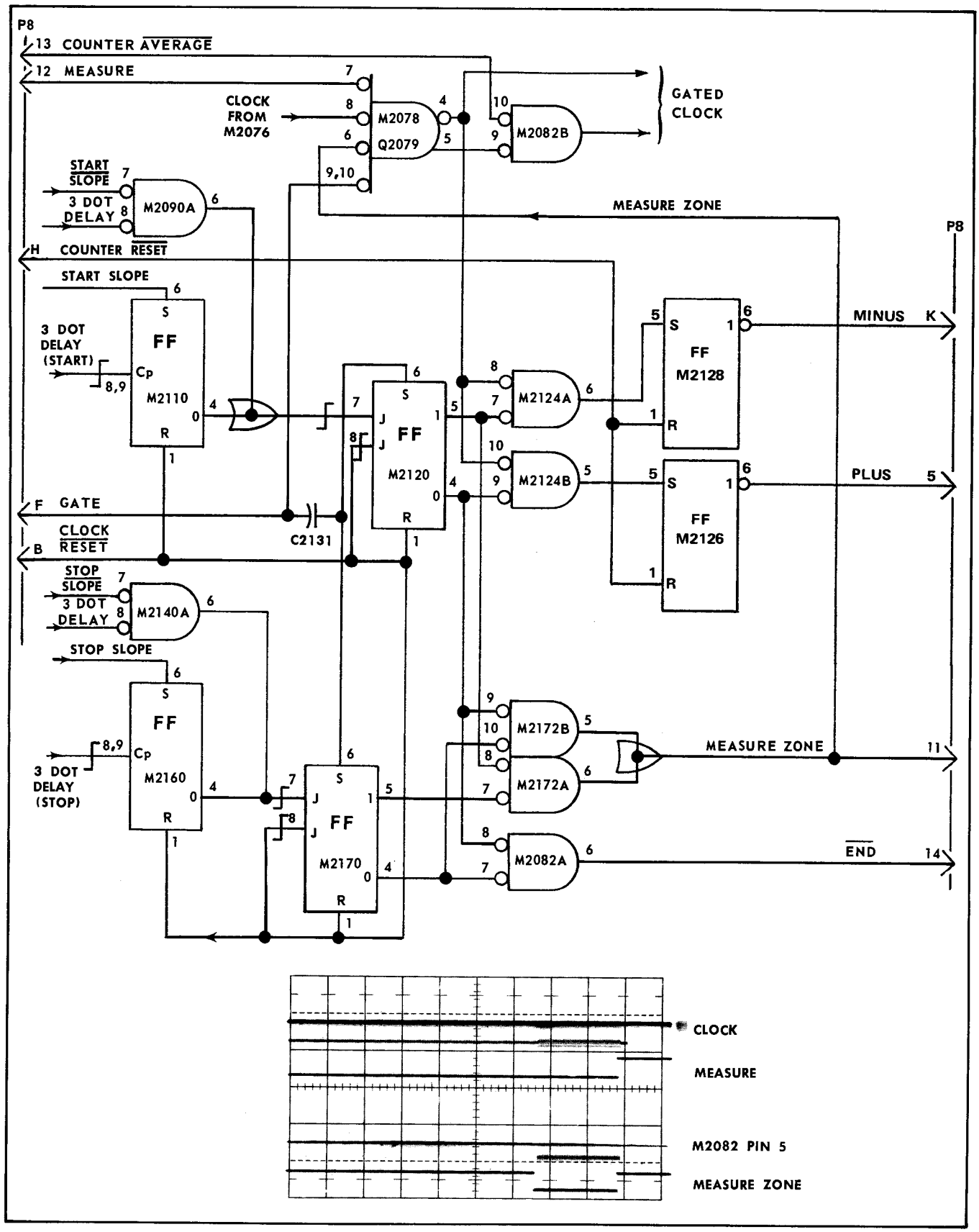


Fig. 4-36. MEASURE ZONE, $\overline{\text{END}}$, GATED CLOCK, PLUS and MINUS signal generation.

After the stop comparator has remained fired for three consecutive clock pulses, the stop comparator's three-dot delay circuit delivers a high output pulse to M2170. Flipflop M2170 toggles and its output on pin 4 goes low. The low from M2170 pin 4 is anded in NAND gate M2172B with the low from M2120 pin 4. The output of M2172B goes high and ends the negative portion of MEASURE ZONE. The now positive MEASURE ZONE is applied to M2078 pin 6 and ends the clock pulse burst. If for some reason the stop comparator does not fire, the clock burst is terminated when GATE sets the three-dot delay circuit counters.

Generation of $\overline{\text{End}}$ Pulse

At the time when M2120 is toggled by the output of the start comparator's three-dot delay circuit, M2120 pin 4 goes low. This low is applied to NAND gate M2182A pin 8. When the stop comparator's three-dot delay circuit toggles M2170, M2082A pin 7 also receives a low input. The output of M2082A pin 6 goes high, creating the $\overline{\text{END}}$ pulse. The END pulse lasts until CLOCK RESET resets M2120 and M2170. With the flipflops reset, they both have highs on pin 4, causing the output of M2082A to go low and terminate the $\overline{\text{END}}$ pulse.

Divide-By-Eight Logic

When the Type 230 is set for Average-Of-Eight mode, P8 pin 13 (see Fig. 4-37) is high (COUNTER $\overline{\text{AVERAGE}}$). The high biases off NAND gate M2082B. At the same time, the COUNTER AVERAGE signal on P8 pin 6 grounds pins 7 and 10 of flipflop M2080 in the divide-by-eight counter (M2080, M2084, and M2086). When the start comparator switches and enables M2078, the clock pulses from M2078 pin 4 to M2080 pins 8 and 9 cause M2080 to toggle. The counter delivers 1 clock pulse out for every eight clock pulses passed by NAND gate M2078. Another divide-by-eight counter on the Synchronizer circuit card causes the Type 230 to make eight measurement sweeps before the count in the counters is transferred into the storage registers.

COUNTER CIRCUIT BOARD

The Counter circuit board (mounted on the back of the front panel) carries the counters, registers, binary-to-decimal decoders, buffer-inverters, and visual indicators necessary to provide the visual and electrical readouts of the Type 230. The counters and binary-to-decimal decoders make extensive use of integrated circuits. The logic of the various circuits shown on the counter and readout diagrams is explained in the following paragraphs.

Input Signals

COUNTER RESET Pulse. The negative COUNTER RESET

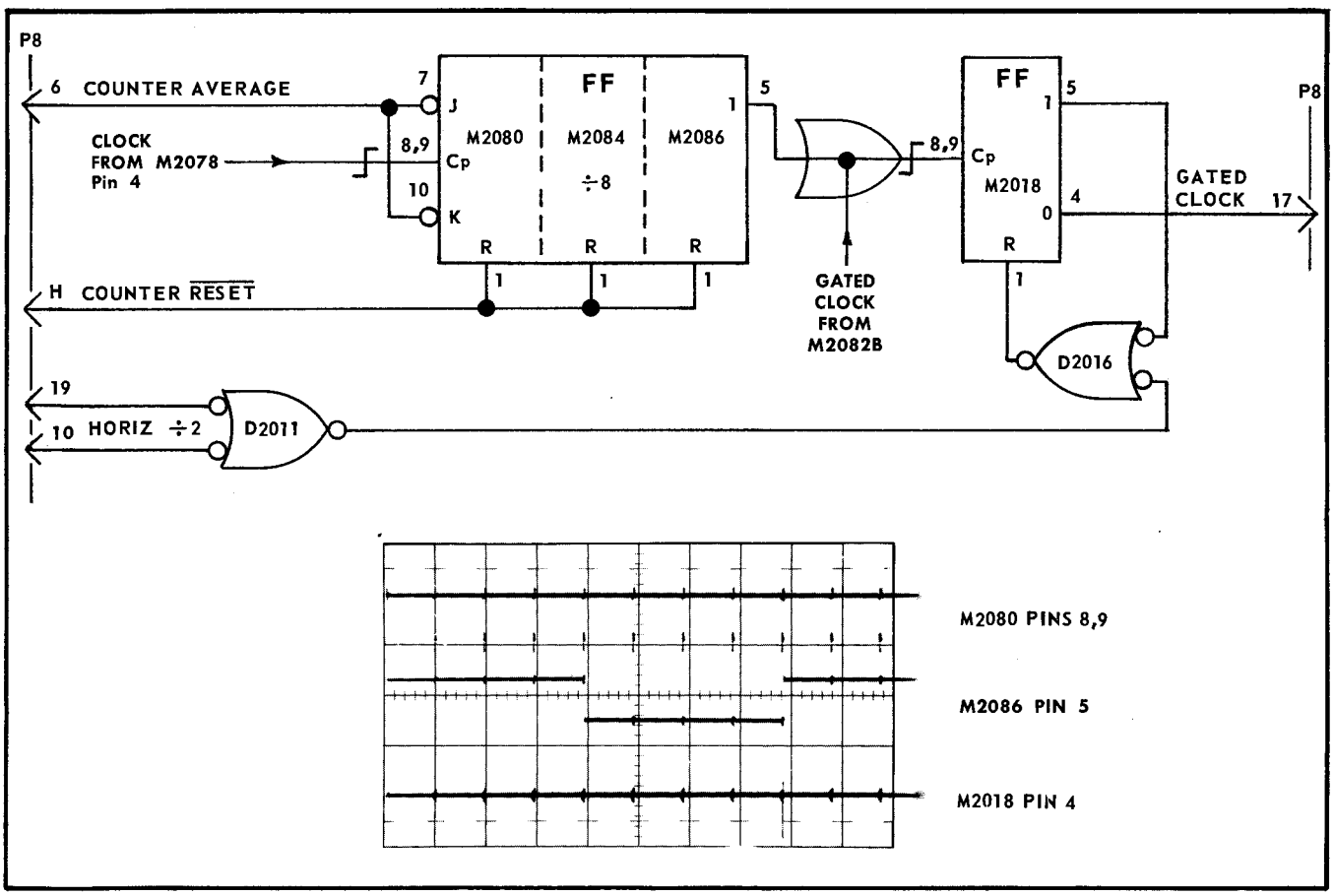
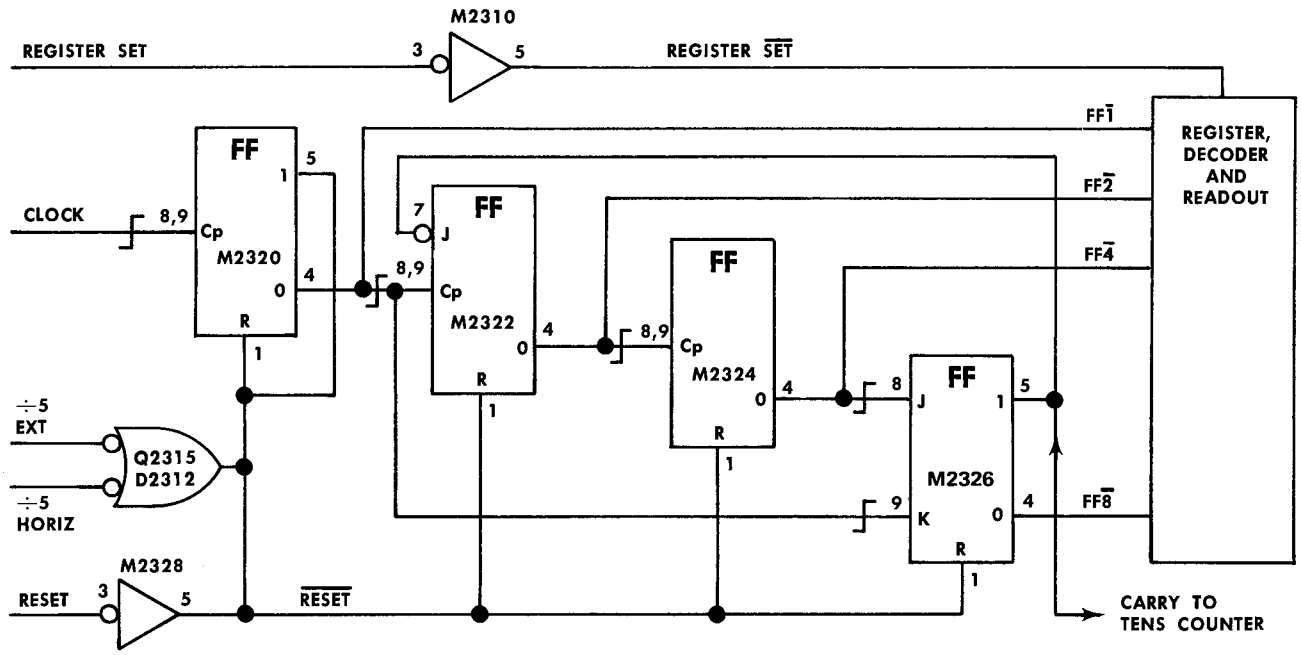
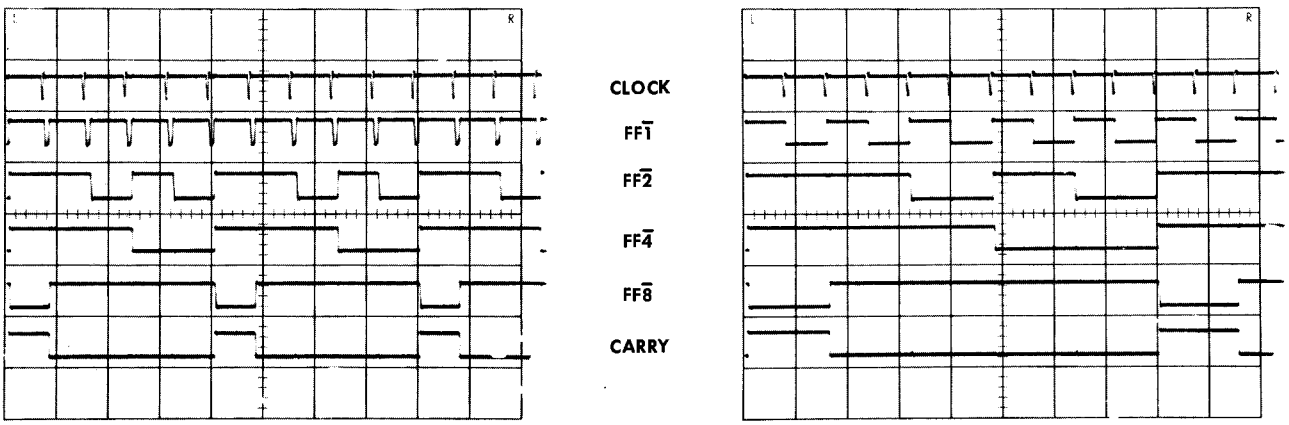


Fig. 4-37. Clock divider circuits.





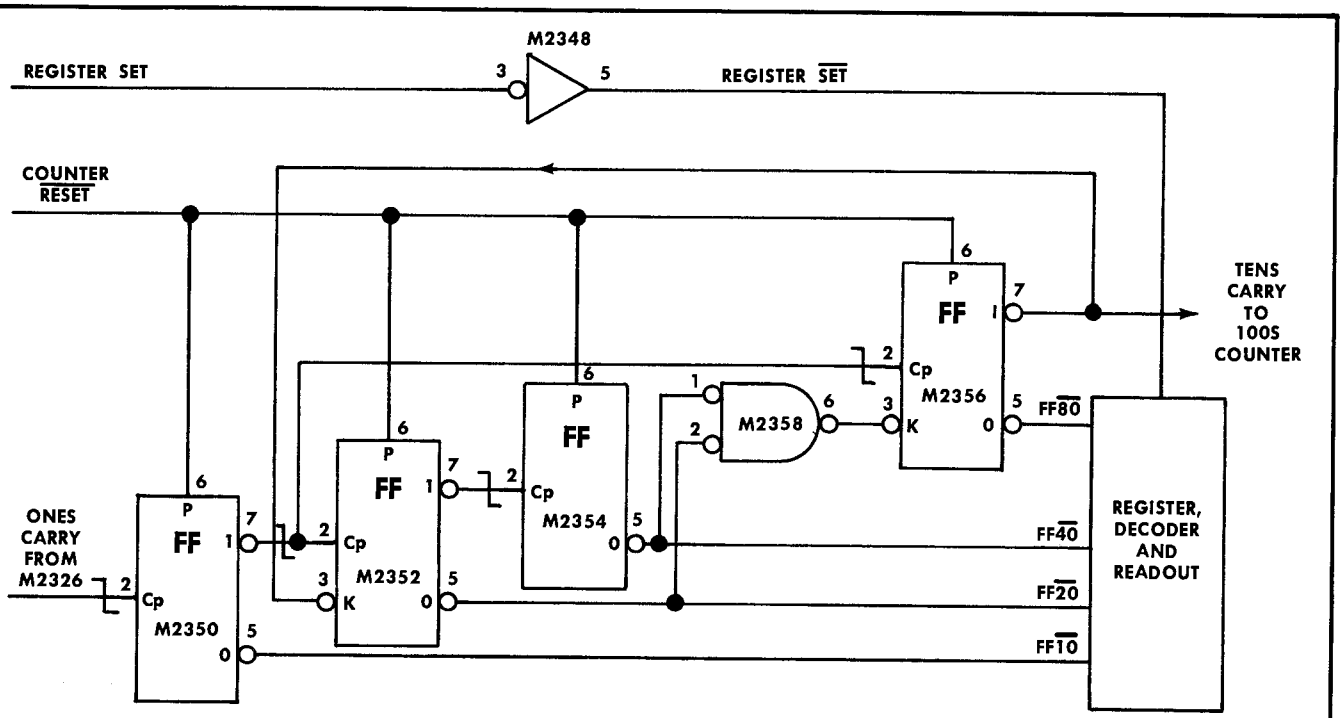
÷10 TRUTH TABLE

Clock	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
FF1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
FF2	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0
FF4	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0
FF8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Carry	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1
Dec. No.	0	1		2		3		4		5		6		7		8		9		10	

÷5 TRUTH TABLE

1	0	1	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0	0	0	0
0	0	0	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	1	1	0	0
1	1	1	1	1	1	1	0	0	1	1
0	1		2		3		4		0	

Fig. 4-38. One's Counter.



TRUTH TABLE

ONES CARRY	0	1	2	3	4	5	6	7	8	9	10
FF$\overline{10}$	0	1	0	1	0	1	0	1	0	1	0
FF$\overline{20}$	0	0	1	1	0	0	1	1	0	0	0
FF$\overline{40}$	0	0	0	0	1	1	1	1	0	0	0
FF$\overline{80}$	0	0	0	0	0	0	0	0	1	1	0
TENS CARRY	1	1	1	1	1	1	1	1	0	0	1

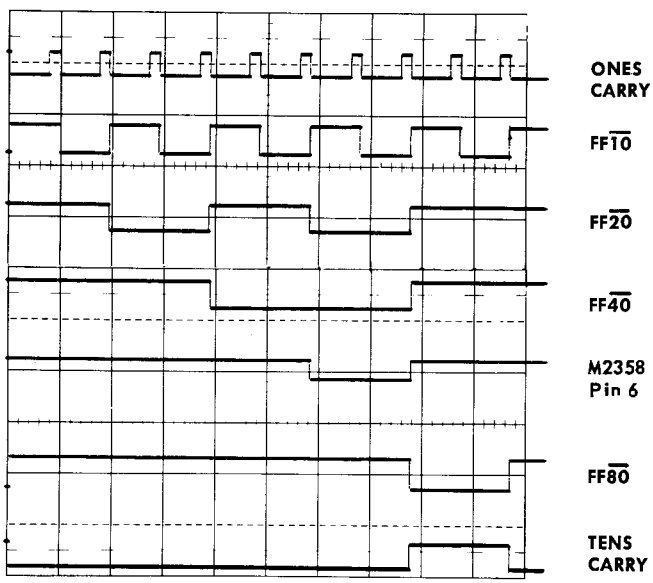


Fig. 4-39. Ten's Counter.

pulse from the Synchronizer circuit card is applied to the circuits on the Counter board (see circuit diagram) prior to the start of a measurement. The COUNTER RESET pulse is inverted in inverter line-driver M2328, becoming the positive-going COUNTER $\overline{\text{RESET}}$ pulse. The pulse resets all four counters to zero before the start of a measurement.

÷ 5 EXT and ÷ 5 HORIZ. The ÷ 5 EXT input is used when counter scaling is controlled by an external programmer. The ÷ 5 HORIZ input is normally connected to the time-base unit. Whenever the time-base unit time per division is in a 2-series range and a time measurement is being made, the ÷5 HORIZ input is low. A low level to either of the ÷5 inputs changes the first flipflop (M2320) in the ones counter from a divide-by-two counter to a divide-by-one counter. This causes the ones counter to send a carry pulse output to the tens counter on every fifth CLOCK pulse. This has the effect of multiplying the CLOCK pulse by two, i.e., 100 dots/cm × 2 = 200 counts/cm. In this mode of operation all output readings are even numbers.

REGISTER SET Pulse. This negative pulse is received from the Synchronizer card at the end of a measurement. When the pulse is received, the information in the counters is transferred to the registers. Note that inverter line-drivers M2310 and M2348 invert the pulse before it is applied to the integrated circuits in the registers.

CLOCK Pulse. The CLOCK pulses are received from the Clock circuit card. When the sampling sweep unit is set to any 5-series timing range, the Clock circuits divide the CLOCK pulses by two before they are applied to the counters.

Output Signals

The outputs of the Counter circuit board are the visual readouts (ones, tens, hundreds, thousands, decimal point, +, —, and unit-of-measure) and electrical readout lines from the registers. Except for the decimal point outputs, all electrical outputs are driven by inverter-buffer transistors.

Logic Description

Ones Counter. The Ones Counter (see Fig. 4-38) is made up of four flipflops (M2320, M2322, M2324, and M2326), the first three of which normally operate as "T" flipflops. The ones counter is basically a binary ripple-through BCD counter. The flipflops switch on the positive-going edge of the CLOCK pulse input. The $\overline{\text{RESET}}$ pulse, applied between measurements, resets all the counters to zero prior to the start of a count.

Disregard for the moment the feedback path from M2320 pin 5 to the collector of transistor Q2315.

With the flipflops reset to zero, the first CLOCK pulse applied to the Cp input of M2320 sets the flipflop to 1 (the output on pin 4 goes low). The output on pin 4 is applied to the pins 8 and 9 of M2322 (Cp) and to pin 9 (K) of M2326. Since the flipflops switch only on the positive-going transition of a pulse, M2322 and M2326 do not reset. The count in the ones counter is now 0-0-0-1. (See the truth table in Fig. 4-38).

The second CLOCK pulse resets M2320 and the positive excursion of the output sets M2322. Flipflop M2326 remains reset since the pulse from M2320 pin 4 is applied to pin 9, the reset input of M2326. The count in the counter is 0-0-1-0.

On the third CLOCK pulse, M2320 sets to 1 and pin 4 goes low. Since the flipflops switch only on the positive-going transition of a pulse, M2322 does not change at this time. The count in the counter is now 0-0-1-1.

The fourth CLOCK pulse resets M2320. The positive-going output (pin 4) of M2320 resets. The positive-going output of M2322 sets M2324. The count in the counter is now 0-1-0-0.

On the fifth CLOCK pulse, M2320 sets to 1. The second and third flipflops do not change. The count in the counter is now 0-1-0-1.

The sixth CLOCK pulse resets M2320, M2322 sets to 1, and M2324 remains in the set (1) state. The count in the counter is now 0-1-1-0.

On the seventh CLOCK pulse, M2320 sets to 1, the second and the third flipflops remain in their 1 state. Note that inputs to both pins 8 and 9 of M2326 are low. The count in the counter is now 0-1-1-1.

The eighth CLOCK pulse resets M2320. Resetting M2320 resets M2322, then M2324. Resetting M2320 also applies a positive-going signal to pin 9 of M2326 but since this is the reset input and M2326 is at this moment already reset, the pulse has no effect. However, almost immediately a positive-going pulse caused by the resetting of M2324 arrives at M2326 pin 8 and causes it to set. With M2326 set to 1, the carry line is high, and pin 7 of M2322 is inhibited. M2322 cannot switch again until the carry line goes low. The count in the counter is now 1-0-0-0.

The ninth CLOCK pulse sets M2320 to 1; the other three flipflops do not change. The count in the counter is 1-0-0-1.

On the tenth CLOCK pulse, M2320 resets and applies a positive-going voltage to the Cp input of M2322 and the K input of M2326. Since the J input (pin 7) to M2322 is held by the 0 output (carry line) from M2326, the second and third flipflops remain reset. The positive-going output of M2320 resets M2326 through its K input (pin 9). The count in the four flipflops is now 0-0-0-0. Resetting the fourth M2326 changes the output on pin 5 of M2326 from high to low, removing the inhibiting input from pin 7 of M2322 and readying it for the next count. The carry line switches from high to low and provides the negative-going CARRY pulse required by the tens counter.

Next, notice the feedback path from pin 5 of M2320 to the collector of transistor Q2315. With no ÷5 input, Q2315 is normally conducting and grounds the feedback. If the time-base unit is set to one of its 2-series timing ranges (20 ns per division, for instance), the ground signal applied to the base circuit of Q2315 through diode D2312 cuts Q2315 off. With the clamp thereby removed from the feedback path, M2320 provides a switch pulse to M2322 for every CLOCK pulse input received. This converts the ones counter from a divide-by-ten counter to a divide-by-five counter. The ones counter now provides a CARRY pulse output for every five CLOCK pulses received.

Whenever the time-base unit is set to one of its 5-series timing ranges (50 μs per division for instance), the CLOCK signal is divided by two on the Clock circuit card.

In this case the ones counter operates as a divide-by-ten counter as previously explained.

Tens Counter. Operation of the tens counter (see Fig. 4-39) is similar to that of the ones counter except that the flipflops switch on the negative-going trailing edge of a positive pulse.

The Tens Counter receives the negative-going carry pulse from the ones counter and the $\overline{\text{RESET}}$ pulse from inverter line-driver M2328. The outputs of the tens counter are BCD signals to the tens register (M2370, M2372, M2374 and M2376) and a negative-going carry pulse to the hundreds counter. Like the ones counter the tens counter is basically a four-flipflop ripple-through counter with gating to reset at the count of ten. The output code is 1-2-4-8. The $\overline{\text{RESET}}$ pulse applied between measurements resets the flipflops to zero prior to the start of a count.

Each time M2326 (in the ones counter) resets to zero, the negative-going pulse from M2326 pin 5 switches the first flipflop in the tens counter (M2350). Assuming that all the counters have been reset by the $\overline{\text{RESET}}$ pulse, the tens counter operates as follows:

On the first carry pulse from the ones counter, the negative-going pulse from M2326 pin 5 sets M2350 to 1. The output on M2350 pin 5 goes low and the output on M2350 pin 7 goes high. The count in the tens counter is now 0-0-0-1.

The second carry pulse from the ones counter resets M2350. The negative-going output from M2350 pin 7 sets M2352 to 1. The negative-going output from M2350 pin 7 is also applied to M2356, but M2356 is receiving a high signal from AND gate M2358 on pin 3 and cannot switch at this time. The count in the tens counter is now 0-0-1-0.

On the third carry pulse, M2350 sets with the output on pin 5 going low, the output on pin 7 going high. Since the flipflop is insensitive to the positive-going edge of a positive pulse, M2352 does not switch on the third carry pulse. The count in the counter is now 0-0-1-1.

The fourth carry pulse resets M2350. The negative-going output from M2350 pin 7 resets M2352. Resetting M2352 generates a negative-going signal on M2352 pin 7 which sets M2354. The count in the tens counter is now 0-1-0-0.

On the fifth carry pulse, M2350 sets (pin 5 goes low and pin 7 goes high). Flipflop M2352 stays reset and M2354 stays set. The count in the counter is now 0-1-0-1.

The sixth carry pulse resets M2350, and the negative-going output on M2350 pin 7 sets M2352. Flipflop M2354 remains set from the fourth carry pulse. The count in the counter is now 0-1-1-0.

On the seventh carry pulse, M2350 sets and M2352 and M2354 remain set. The count in the counter is now 0-1-1-1.

At this point, note the inputs to M2356 and M2358. The output from M2350 pin 7 to pins 2 of M2352 and M2356 is high. The output from pin 5 of M2352 to input pin 1 of M2358 is low, as is the output from pin 5 of M2354 to input pin 1 of M2358. This makes the output of M2358 pin 7 high, which is applied to M2358 pin 5. Under these conditions, the output of M2358 pin 6 is low. The low output from M2358 pin 6 is applied to input pin 3 of M2356. Conditions are now such that M2356 will switch the next time a negative-going pulse is applied to M2356 pin 2.

On the eighth carry pulse, M2350 resets. The negative-going output from M2350 pin 7 causes M2356 to set and M2352 to reset. Resetting M2352 applies a negative-going pulse to M2354 pin 2, and M2354 also resets. The count in the counter is now 1-0-0-0.

The ninth carry pulse sets M2350, with M2350 pin 5 going low and M2350 pin 7 going high. The transition on pin 7 is the wrong polarity to switch M2352, M2354, and M2356. The count in the counter is now 1-0-0-1.

On the tenth carry pulse, M2350 resets and the negative-going output on pin 7 resets M2356. The resetting of M2356 removes the inhibit from pin 3 of M2352 and the negative-going signal from M2356 pin 7 is applied as a carry pulse to the hundreds counter.

Hundreds Counter. Except for circuit numbers, the hundreds counter is the same as the tens counter. The logic description of the tens counter applies to the hundreds counter as well.

Thousands Counter. Since the overall counting operation does not require the counter to count above decimal 3999, the thousands counter (see Fig. 4-40) consists of two flipflops. Flipflops M2400 and M2404 operate as a two-stage ripple-through counter until a binary count of three (1-1) is accumulated. On the count of three, a feedback loop from the reset side (pin 7) of M2404 locks up the two flipflops until a $\overline{\text{RESET}}$ pulse is received.

Following the output of the thousands counter through registers M2406 and M2408, it can be seen that any time the number 3 in Nixie tube V2429 is lighted, the E (error) symbol in Nixie tube V2439 is also lighted. This does not necessarily indicate that a counting error has been made, but the operator must realize that if the total count should exceed decimal 3999, the counters will not provide the proper readout. Anytime the count reaches decimal 3000 or more, the reading may be suspected of being incorrect.

Registers. The registers consist of 24 JK flipflops which store the output information from the various logic circuitry to which they are connected. Note that all flipflops in the registers have their clock and reset inputs (pins 2 and 6) tied together and their K inputs (pin 3) connected to the information to be stored. When the REGISTER $\overline{\text{SET}}$ pulse from M2310, M2348 and M2402 is applied to pins 2 and 6, the information to be stored is clocked into the registers.

Taking integrated circuit M2330 as an example, the operation of the registers is as follows:

1. Assume that the "1" (set) is being received from M2320 on pin 3. The circuit cannot switch until a clock (REGISTER $\overline{\text{SET}}$) is applied.

2. When the REGISTER $\overline{\text{SET}}$ pulse from the Synchronizer card arrives, it is inverted to REGISTER $\overline{\text{SET}}$ by M2310. The positive level of the REGISTER $\overline{\text{SET}}$ pulse resets M2330 to 0 and the negative-going trailing edge clocks in the state of M2320.

Since all the remaining register cells on the Counter circuit board operate in a manner similar to that given above for M2330, no further explanation is provided.

Binary-To-Decimal Decoder—Nixie Drivers. The integrated circuits decode the 1-2-4-8 BCD outputs of the registers and supply decimal information to the ones, tens and hundreds Nixie indicator tubes. The binary-to-decimal decoders require either ground-closure or saturated-transistor inputs. The outputs are the output resistance of a saturated transistor which, to the Nixie tubes, looks like ground closures to the Nixie element to be lighted.

The binary-to-decimal decoder for the thousands Nixie consists of Q2421, Q2423, Q2425, and Q2427 (see circuit diagram). Circuit operation is as follows:

1. With a zero in the thousands register (M2406 and M2408), the outputs on pin 5 of both units are high, the outputs on pin 7 low. The high output of M2406 pin 5 applies enabling bias to the bases of Q2421 and Q2425. Transistor Q2425 cannot conduct because of the high output of M2408 applied to its emitter. The low output of M2408 is applied to the emitter of Q2421. Under these conditions, Q2421 conducts and lights the "0" in the thousands Nixie.

2. When the thousands register contains a binary 1 (0-1), the high output of M2406 pin 7 applies enabling bias to the bases of Q2423 and Q2427. Transistor Q2427 is prevented from conducting by the high output of M2408 pin 5, but the low output of M2407 pin 7 is applied to the emitter of Q2423, permitting Q2423 to conduct and light the "1" in the thousands Nixie.

3. A binary 2 (1-0) in the register sets M2406 to 0 and M2408 to 1. The high output on pin 5 of M2406 applies enabling bias to the bases of Q2421 and Q2425 as previously explained. However, the low output of M2408 pin 5 enables the emitter circuit of Q2425 only, so the "2" element of V2429 is lighted.

4. A binary 3 (1-1) in the register sets both M2406 and M2408 to 1. The high output on pin 7 of M2406 applies enabling bias to the bases of Q2423 and Q2427, but the low output of M2408 pin 5 enables Q2427 only. The "3" in the thousands Nixies is lighted, and through R2437, the E (error) in Nixie V2439.

Decimal Point Decoder. The Decimal Point Decoder uses a binary-to-decimal decoder with special connections for properly positioning the decimal point. The inputs are decimal point information and a ÷ 5 level from the time-base unit, the vertical amplifier, or from external equipment. To gain digital resolution, the ÷5 operation is actually a "multiply by two and move the decimal point" operation. The circuit operates as follows:

1. Assume that the decimal point is to be in the fifth place to the right (10 to the zero power). In this situation, there are high inputs into the decimal register (M2440, M2444, and M2448). The outputs from the flipflops in the register are all high. M2450 decodes this condition as a zero and delivers an output on M2450 pin 9, lighting the fifth neon lamp (B515).

2. Next assume that the ÷5 line is held low. As previously explained, this is actually a "multiply by two and move the decimal point" operation. The low ÷5 input to M2440 causes the flipflop to set to 1 and the output on pin 5 goes low. This is decoded by M2450 as a 1. The output on pin 5 of M2450 goes low and lights B516, the fourth neon lamp (10^{-1}).

3. When the external input requires the decimal point to be moved to the fourth position, the output of M2448 goes low. This is decoded by M2450 as a 2 and the output on pin 10 of M2450 goes low. Since pins 5 and 10 on M2450 are connected together, B516 lights again (10^{-1} again).

4. While holding M2448 pin 3 low (10^{-1}), apply a low level ÷5 to pin 3 of M2440. The low outputs from M2440 and M2448 are decoded by M2450 as a 3. The output on Pin 4 of M2450 goes low, lighting B517 (10^{-2}).

5. The third neon lamp is also lighted by a low input on the EXT 3 line to pin 3 of M2444. With an input on this line only, the output of M2444 is decoded by M2450 as a 4. The output of M2450 pin 11 goes low, and since pins 4 and 11 are connected in parallel, B517 again lights (10^{-2}).

6. When the external input requires the decimal point to be moved to the second position, the inputs to M2444 and M2448 are connected in parallel through D2444 and D2447. Applying a low level to pin AK sets both M2444 and M2448 to 1. Decoder M2450 decodes the two inputs as a 6, which makes the output on pin 12 of M2450 low and turns on B518 (10^{-3}).

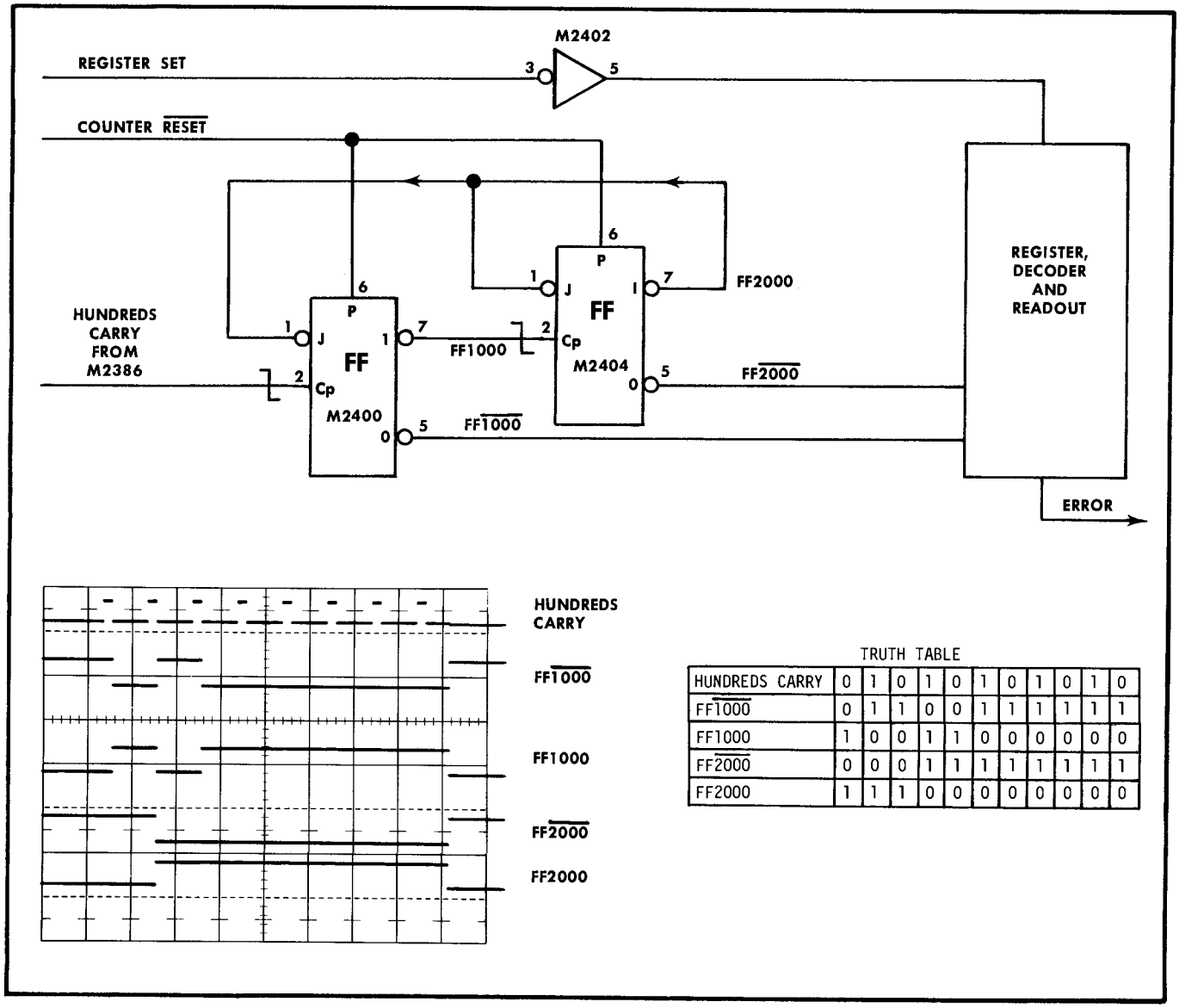
7. With conditions as given in the preceding paragraph, assume that the ÷5 line is also low. Decoder M2450 reads the three low input as a 7 and the output on pin 2 of M2450 goes low. Neon lamp B519 is lighted (10^{-4}).

After the decimal point information has been decoded and applied to the neon lamp which indicates the decimal point, it is still necessary to provide the decimal point location to external equipment. The information is re-encoded into binary by D2455, D2456, D2457 and D2458 as follows. When B515 is lighted, there is no output (0-0), when B516 is lighted, D2457 holds pin AL low (10^{-1}). Likewise, when the line to B517 is low (10^{-2}), D2455 holds pin D low (10^{-2}). When B518 is lighted, the line to pin AJ and the cathodes D2456 and D2458 is low. Diodes D2456 and D2458 hold both the 10^{-1} and the 10^{-2} lines low, giving a binary 3 (10^{-3}). The 10^{-4} line is held low by D2459 whenever B519 is lighted.

Units-Of-Measure Circuit. The units-of-measure circuit consists of a five-bit register, five buffer-inverters, and a Nixie readout tube. The inputs to the register are the unit-of-measure information received from the sampling sweep unit and the vertical amplifier. This information is transferred into the register when the REGISTER $\overline{\text{SET}}$ pulse moves high, then returns low. The information stored in the register is taken from the outputs, then amplified and inverted by the buffer-inverter transistors (Q2481, Q2483, Q2485, Q2487 and Q2489) and applied to the appropriate element or elements in the Nixie tube. The outputs of the buffer-inverter transistors are also made available to external lines via D2480, D2482, D2484, D2486 and D2488.

Limit Lamp Storage. The limit storage circuit (see Fig. 4-41) has the function of delaying and transferring the upper and lower limit comparator output information to the readout lamps located on the front panel. It is composed of a single-shot multivibrator, storage flipflops for both the upper and lower limit information, a NAND gate, and three limit lamp drivers.

GREATER information from the upper limit comparator comes into the circuit through pin AZ to pin 3 of flipflop



TRUTH TABLE

HUNDREDS CARRY	0	1	0	1	0	1	0	1	0	1	0
FF1000	0	1	1	0	0	1	1	1	1	1	1
FF1000	1	0	0	1	1	0	0	0	0	0	0
FF2000	0	0	0	1	1	1	1	1	1	1	1
FF2000	1	1	1	0	0	0	0	0	0	0	0

Fig. 4-40. 1000s Counter.

M2512. The information seen at pin 3 of M2512 may be either a low to indicate GREATER, or a high to indicate GREATER. LESS information enters the circuit through pin BC on the Counter and Readout board to pin 3 of flipflop M2522. The LESS information, a low or a high, comes from the lower limit comparator.

The negative REGISTER SET pulse comes through differentiator C2501-R2501 to pin 2 of integrated circuit M2502, which is two NAND gates connected as a single-shot. The negative transition the REGISTER SET pulse has no noticeable effect on pin 2 of M2502, since this pin is maintained in a low state by R2501. When REGISTER SET returns high, pin 7 goes low, causing pin 6 to go high. Pin 6 of M2502 is connected to pins 6 and 2 of flipflop M2512, and to pins 6 and 2 of flipflop M2522. The high at pin 6 of single-shot M2502 lasts about 20 μs, due to the RC time constant of C2505 and associated circuitry. The 20 μs is used to wait for a stable Limit circuit output.

This causes both of the storage flipflops to set on the positive level of the single-shot output. When the output of the single-shot returns negative, pins 2 of both storage flipflops are activated by the negative edge, and the limit information is transferred into the flipflops. Following is a truth table of the input and output combinations of the storage flipflops.

TRUTH TABLE

M2512 pin 3	M2522 pin 3	M2512 pin 7	M2522 pin 7
H (0)	H (0)	L (1)	L (1)
H (0)	L (1)	L (1)	H (0)
L (1)	H (0)	H (0)	L (1)
L (1)	L (1)	H (0)	H (0)

As the foregoing truth table illustrates, when the limit information to both storage flipflops is high, the flipflops go to a set condition and do not reset when pin 2 is pulled low. The two lows at the output (pin 7) of the flipflops go to M2532A. The two lows at the inputs (pin 1 and 2) of the NAND gate cause its output (pin 7) to go high. The high at M2532A pin 7 goes to the base of limit lamp driver transistor Q2533 and turns it on. The conduction of Q2533 energizes the WITHIN LIMITS lamp on the Type 230 front panel.

When the LESS information from the lower limit comparator is low, indicating a count less than the limits, flipflop M2522 has a low at its reset input. The negative edge from M2502 enables the flipflop, which sends a high from pin 7 to the base of Q2523 and to pin 2 of M2532A. The high at pin 2 of M2532A holds its output pin 7 low, which turns Q2533 off and de-energizes the WITHIN LIMITS lamp. The same high turns Q2523 on and energizes the BELOW LOWER LIMIT lamp on the Type 230 front panel. This indicates to the operator that the count is less than the lower limits.

When the GREATER information from the upper limit comparator is low (indicating a count greater than the upper limit), pin 3 of M2512 is low. When the negative edge from M2502 occurs, the flipflop is reset, sending a high to Q2513. The high from pin 7 of M2512 is also sent to M2532A pin 1, holding its output (pin 7) low. The low at the output of M2532A turns Q2533 off, de-energizing the WITHIN LIMITS lamp. The high at the base of Q2513 turns it on, energizing the ABOVE UPPER LIMIT lamp on the front panel of the Type 230. This indicates to the operator that the count has exceeded the upper limit.

When both LESS and GREATER inputs from the limit comparators are low, both of the storage flipflops will be reset when the negative edge of the single-shot gate occurs. This will cause both flipflop outputs to send a high to the transistor drivers (Q2513 and Q2523). The highs at the bases of the two transistors turns them both on, and the front panel limit lamps will indicate that the count is both above and below the limits.

The collectors of Q2513, Q2533, and Q2523 are connected to J301, pins 27, 28 and 29 respectively. These external pins are for external readout and recording purposes. The collectors are also connected to J204 pin 19, 20 and 21 respectively. The J204 pins may be used for the same purposes.

LIMIT COMPARATOR

The limit comparator sections essentially function as majority[4] circuits. This means that each of the transistors is sensitive to whether the input has a majority of lows or a majority of highs. The state of the transistor's collector will be opposite to the nature of the majority, since the transistor is an inverter. According to the author listed in the footnote below, if a majority is inverted (complemented) it becomes a minority. In accordance with the footnote this discussion will treat each of the limit comparators as a series of minority gates, except where specifically excluded.

The Limit circuit card (Model 2-up) is provided with two unique voltage supplies, each derived from standard voltages supplied by the Type 230 power supply. These two supplies provide the closely regulated voltages required for operation of the Limit Comparators.

[4]**Digital Computer Design Fundamentals; Yohan Chu; McGraw-Hill; 1962. See Pages 130-132.**

—4.9-Volt Supply

A resistive divider (R2773-R2775) connected from the −50 volt supply to ground furnishes the stable reference point for the operation of this supply. The base of transistor Q2775 is connected to the junction of the divider resistors, where the operating voltage is approximately —4.2 volts. The collector of Q2775 is returned to −50 volts through R2779 and P11-BB. Resistor R2779 provides protection for the transistor, plus additional power-handling capability for the circuit. The emitter of Q2775 is the —4.9 volt output to all the limit circuitry which requires this voltage.

+16.9-Volt Supply

A resistive divider (R2753-R2755) connected between +12 volts and +50 volts furnishes a constant +17.6 volts from which transistor Q2755 can reference its operation. The collector of Q2755 is returned directly to +50 volts through P11-V to provide sufficient current for the demands of the limit circuitry using +16.9 volts.

Limit Comparator

The Limit card, in conjunction with the limit lamp storage section of the Counter board, provides "Go-No-Go" front panel readout for the operator of the Type 230. There are three limit lamps located on the right-hand side of the Type 230 front panel. These three lamps indicate to the operator whether a measurement exceeds the limits preset by the operator. The Limit Set knobs located near the limit lamps on the front panel enable the operator to set the measurement range.

The Limit circuit is essentially a pair of binary comparators. The programmed limits and counter information are delivered to the Limit circuits as logic levels. A logical one (low) is approximately ground potential. A logical zero (high) is approximately +12 volts. When the Type 230 transfers the accumulated count to the decoders in the Counter board, this information is also transferred to the Limit card counter inputs for comparison with the upper and lower programmed limits.

Each of the two limit comparators consists of a series of logical "minority" circuits. These minority gate compare the incoming counter and limit inputs. If the inputs to a minority gate are a minority of lows and a majority of highs, the output of the minority gate is low. If the inputs to the minority gate are a minority of highs and a majority of lows, the output of the minority gate is high. Excepting the output gates of the limit comparators, all of the circuitry in the limit comparators can be segmented into three-input minority gates.

The truth table for a minority gate in the Limit card is illustrated in Fig. 4-42, with the logic symbol for a minority gate.

All of the "C" inputs to the Limit card are from the Counter board. All of the "U" inputs comes from the UPPER LIMIT switch of the Type 230, or externally programmed limits from J203. The MEASUREMENT MODE switch selects either the front panel Upper Limit switch information or limit information from programmed inputs at J203. The "L" inputs

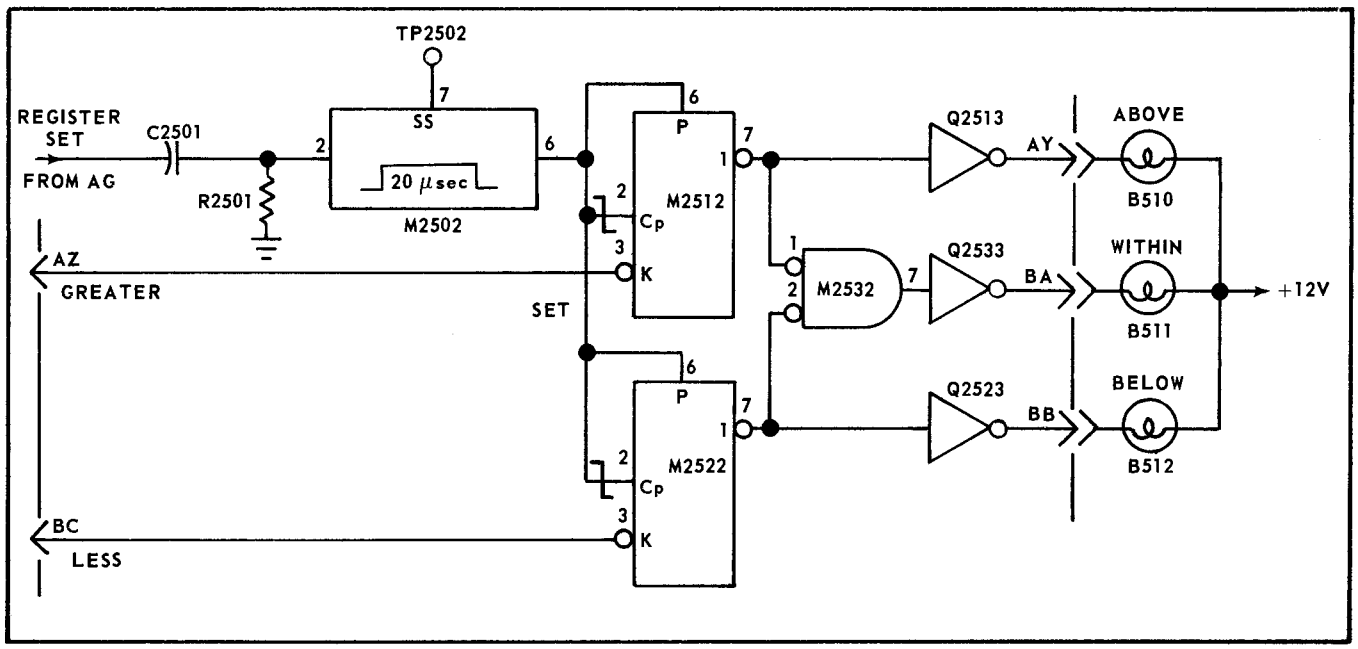


Fig. 4-41. Limit storage logic.

come from the Lower Limit switch of the Type 230, or externally programmed limits from J203. The MEASUREMENT MODE switch selects either the front panel Lower Limit switch information or programming information from J203.

The circuit operation of the limit comparators is best explained by analyzing the operation of a typical minority gate, and then by viewing the overall operation of the two limit comparators as a series of minority gates.

Fig. 4-43 is a schematic diagram of the first two minority gates in the upper limit comparator. These gates are typical for both the upper and lower limit comparators. When referring to a minority gate in this description, the output transistor of that minority gate will be mentioned as the minority gate designator. For example, Q2620, R2612, R2616 R2618 and R2619 are the components for a minority gate; the reference will be made to minority gate Q2620.

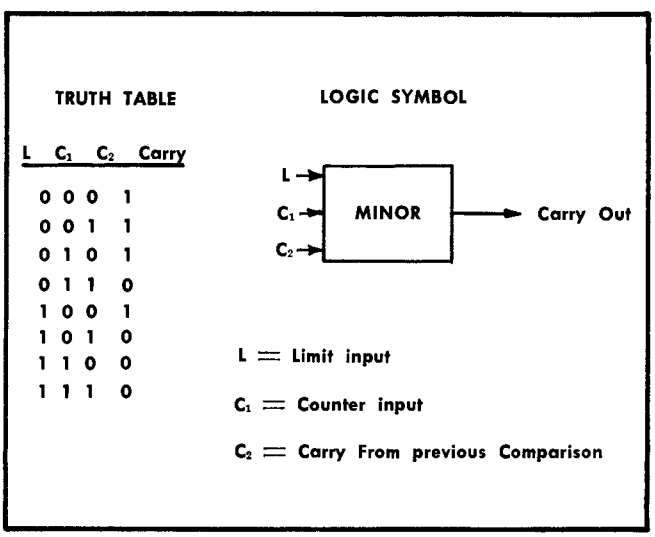


Fig. 4-42. Minority logic and truth table.

1. Counter MINUS information at P11 pin 5 is inverted by Q2977 and applied as Counter $\overline{\text{MINUS}}$ to resistor R2618.

2. Counter 1 information from P11 pin 17 is inverted by Q2817 and sent as Counter $\overline{1}$ to R2616.

3. Upper 1 information comes from P11 pin CC through R2611 to the emitter of Q2613. Since Q2613 is in a common base configuration, the Upper 1 information is not inverted by Q2613 and it goes from the collector of Q2613 to R2612.

Resistors R2612, R2616, R2618, and R2619 are tied to the base of Q2620. The other end of R2619 is returned to +16.9 volts.[5] The emitter of Q2620 is returned to +12 volts. Whenever two or more of the three input resistors are returned to a high, the voltage at the base of Q2620 is more positive than that of its emitter, and Q2620 is in an off condition. The off condition of Q2620 sends a low to R2620, one of the input resistors of the next minority gate. If two or more of the three resistors at Q2620 base (R2612, R2616, and R2618) are returned to a low, the voltage at the base of Q1620 will be more negative than its emitter, turning the transistor on. An on condition sends a high to R2620.

Transistor Q2631 has the following three inputs:

1. The Ones information from the collector of Q2620 through R2620.

2. Upper 2 information from P11 pin 26 is sent to R2622. R2622 is connected to R2624 and the base of Q2624. The other end of R2624 is returned to +12 volts. The upper 2 information at the base of Q2624 is inverted by Q2624 to Upper $\overline{2}$ information at the collector of Q2624. From the col-

[5] +50 V is used in Limit card Model 1.

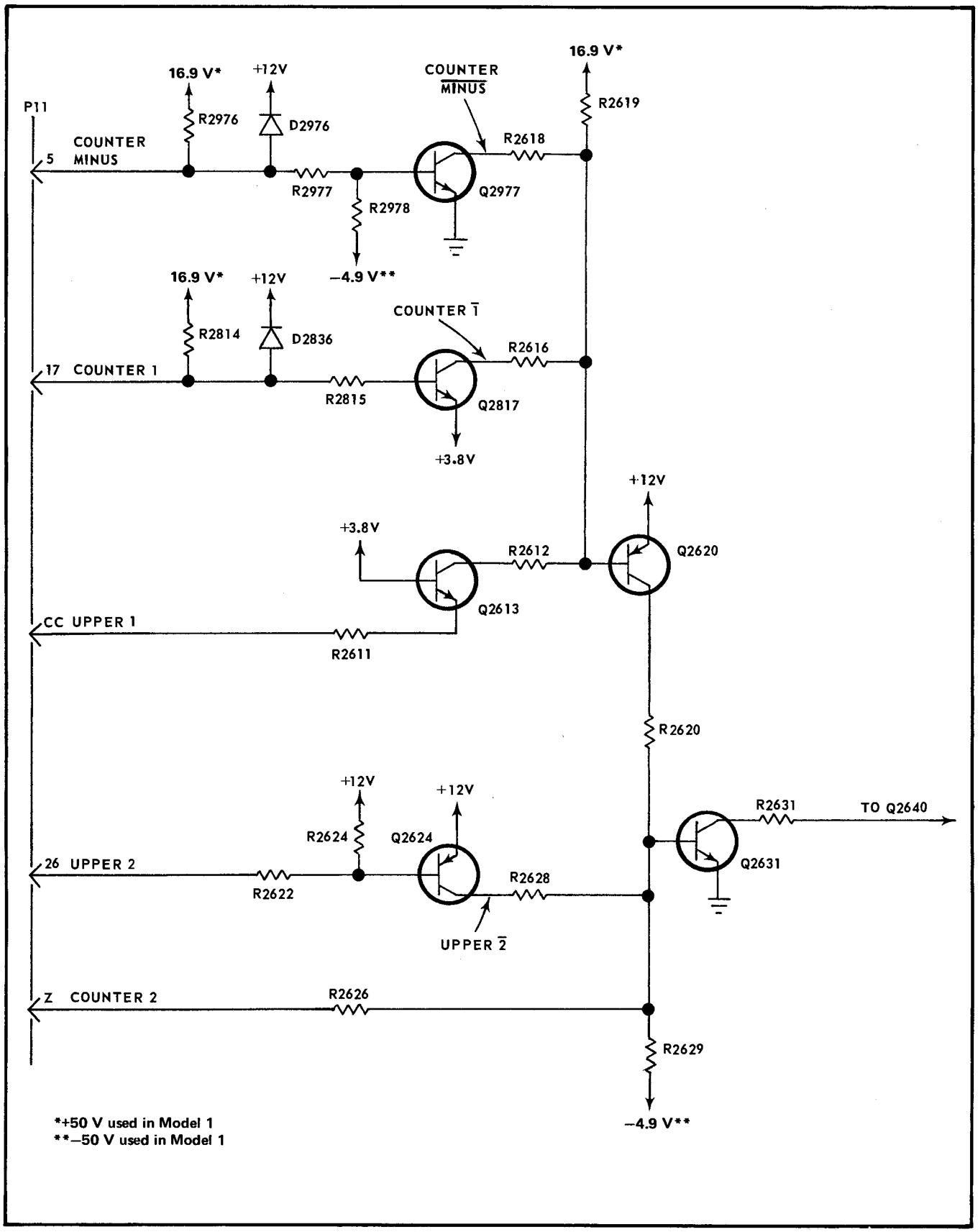


Fig. 4-43. Circuit diagram illustrating minority logic.

lector of Q2624 Upper $\overline{2}$ goes to R2628, the second input to minority gate Q2631.

3. Counter 2 information enters at P11 pin Z, and is sent directly to R2626, the third input to minority gate Q2631.

R2629 is returned at one end of —4.9 volts[6]. The other end of R2629 connects to the junction of R2626, R2628, R2620, and the base of Q2631. The emitter of Q2631 is at ground, and the collector connects to R2631, one of the inputs to the next minority gate Q2640. When two or more of the inputs to the minority resistors (R2620, R2624, and R2628) are low, the voltage at the base of Q2631 is more negative than its emitter. The off condition of Q2631 sends the minority, a high, to R2631. If two or more inputs to the minority resistors are high, Q2631's base is more positive than its emitter, turning it on. The on condition of Q2631 causes a low to be sent to R2631.

Upper Limit Comparator

To further the understanding of the upper limit comparator, four examples will be given.

Example One

Upper Limit Setting ..... +1234

Nixie Readout ..... ±1232

In this case, the following inputs to P11 are low:

Upper	P11 Pin	Counter	P11 Pin
4	DD	2	Z
10	EE	10	11
20	19	20	21
200	P	200	12
1000	R	1000	F

The remainder of the Upper and Counter inputs to P11 are high, as shown in Fig 4-44.

The first comparison is at minority gate Q2620 and associated components. The minority gate has three inputs: Counter $\overline{1}$, a low ($\overline{C1}$ is the Counter 1 information inverted by Q2817); C MINUS, a low, from the collector of Q2977; Upper 1 from P11 pin CC, which is high. The low-low-high input to the minority gate turns Q2620 on and passes a high to the next minority gate (Q2631 and associated components).

The high at R2620 is the first input to minority gate Q2631. Upper 2 at P11, pin 26, is high. After passing through divider R2622 and R2624, Upper 2 is inverted to a low by Q2624. This low to R2628 is the second minority input to Q2631. The third input is a low from P11 pin Z, the Counter 2 information. Counter 2 comes through R2626 to the base of Q2631. The input of high-low-low at the base of Q2631 turns it off, sending a high to R2631.

Resistor R2631 is one input to the next minority gate (Q2640 and associated components). The second input comes from P11, pin DD, the Upper 4 information. Upper 4, a low, is sent through R2633 to the emitter of Q2633 whose base is returned to +3.8 volts. At the collector of Q2633 the low goes to the second minority resistors, R2634. The third information is sent from P11 pin 14, the Counter 4 input. Counter 4 is high, held to +12 volts by D2836, whose anode is connected to Counter 4 and whose cathode is returned to +12 volts. When Counter 4 input is released by the transistor driver in the Counter board, R2836 pulls up on the Counter 4 input line. The Counter 4 line stops going up at about +12 volts when D2836 turns on. The Counter 4 high is passed through R2837 to the base of Q2837. The high at the base of Q2837 is inverted to Counter $\overline{4}$, a low, and sent to R2638. The high-low-low input to Q2640 turns it on, sending a high to R2640. R2640 is the first input to the next minority gate (Q2651 and associated components).

Counter 8 is high and comes from P11 pin Y. The Counter 8 input goes to R2646, the second input to the minority gate. Upper 8 comes from P11, pin 23, through R2642 and R2644, to the base of Q2644. Transistor Q2644 inverts Upper 8 to a low which is applied to R2648. A high-high-low to the base of Q2651 turns it on, sending a low to the next minority gate (Q2660 and associated components). The Upper 10 information at P11 pin EE is low, and passes through R2653 to the base of Q2653. The low at the base of Q2653 is not inverted by the transistor, and the low appears at one end of R2654 as the second input to minority gate Q2660. Counter 10 information at P11, pin 11, is a low. The Counter 10 is inverted to a high by Q2857, and is sent to R2658 as the third input to minority gate Q2660. The low-low-high at the base of Q2660 turns it on, sending a high to R2660, part of minority gate Q2671.

Upper 20 information, a low, appears at P11 pin 19 and goes to voltage divider R2662-R2664. From the junction of the voltage divider the Upper 20 information goes to the base of transistor Q2664, which inverts the low to a high. This high goes to R2668, the second input to the minority gate. The third input, Counter 20, is low, and comes from P11 pin 21 to R2666. The high-high-low at the base of Q2671 turns it on, sending a low through R2671, an input to the next minority gate (Q2680 and associated components).

Upper 40 information from P11 pin 27 is sent through R2673 to the emitter of Q2673. The high at the emitter of Q2673 is not inverted, and appears at the collector of Q2673 as a high. The high is sent to R2674, the second input to minority gate Q2680. Counter 40 information at P11 pin 9 is high. This high goes to the base of Q2877 for inversion to a low. The low at the collector of Q2877 is sent through R2678, the third input to the minority gate. The low-high-low information at the base of Q2680 turns it on, sending a high from its collector to R2680, an input to the next minority gate (transistor Q2691 and associated components).

Upper 80 information, a high, comes from P11 pin 15, and is sent through voltage divider R2682-R2684 to the base of Q2684. A low at the collector of Q2684 is sent through the second input of the minority gate, R2688. Counter 80 information at P11 pin U is a high. The high goes to the third input of the minority gate through R2686. A high-low-high at the base of Q2691 turns on the device, delivering a low to the next minority gate (Q2700 and associated components) through R2691.

The Upper 100 information at P11 pin 16, a high, is fed through R2693 to the emitter of Q2693. The high at the col-

[6]—50 V used in Model 1.

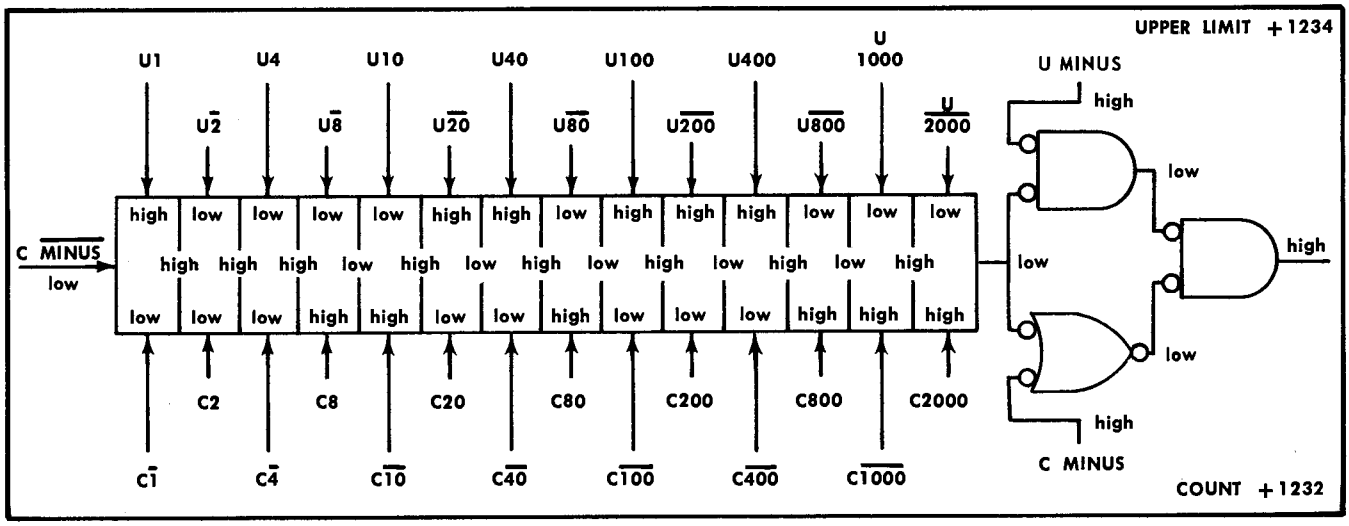


Fig. 4-44. Example 1. Comparison of +1234 upper limit with +1232 count.

lector of Q2693 is sent to R2694, the second input to the minority gate. Counter 100, a high, appears at P11 pin 8. This Counter 100 information is sent through R2897 to the base of Q2897, where the high is inverted to a low at the collector of Q2897. The Counter $\overline{100}$ at the collector of Q2897 is sent through R2698, the third input to the minority gate. The low-high-low at the base of Q2700 turns the transistor on, sending a high to the next minority gate through R2700.

Upper 200 information at P11 pin P is a low. The Upper 200 information is fed through voltage divider R2702-R2704 to the base of Q2704, is inverted by Q2704, and sent as a high to R2708, the second input to the minority gate. The third input to the minority gate, Counter 200, comes from P11 pin 12. The Counter 200 information is a low, and is fed through R2706 to the base of Q2711. The high-high-low at the base of Q2711 turns it on, and a low at its collector is sent to R2711, one input to the next minority gate (Q2720 and associated components).

The Upper 400 information at P11 pin S is a high and is sent through R2713 to the emitter of Q2713. No inversion occurs between emitter and collector of Q2713, so a high is sent through R2714, the second input to the minority gate. Counter 400 information is high, and comes into the Limits card at P11, pin 7. The high information (Counter 400) goes through current-limiting R2917 to the base of Q2917. The Counter 400 is inverted to Counter $\overline{400}$ at the collector of Q2917, and is sent as a low to R2718, the third input to the base of Q2720. The low-high-low at the base of Q2720 turns it on, sending a high to the next minority gate (Q2731 and associated components) through R2720.

Upper 800 information at P11 pin N is a high and goes through voltage divider R2722-R2724 to the base of Q2724. The low at the collector of Q2724 is fed through R2728, the second input to the minority gate. Counter 800 information at P11 pin L is a high, and goes through R2726 as the third input to the base of Q2731. The high-low-high at the base of Q2731 turns it on, sending a low through R2731, one input to the next minority gate (Q2740 and associated components).

Upper 1000 information from P11 pin R is a low and goes through R2733 to the emitter of Q2733. The low at the collector of Q2733 is sent through R2734 as one input to the minority gate. Counter 1000 at P11 pin F is a low and goes through R2937 to the base of Q2937. The Counter $\overline{1000}$ at the collector of Q2937 is a high, and is fed through R2738 as the third input to the minority gate. The low-low-high at the base of Q2740 turns it on, sending a high through R2740 as one input to the next minority gate (Q2751 and associated components).

Upper 2000 at P11 pin H is a high and goes through voltage divider R2742-R2744 to the base of Q2744. The low at the collector of Q2744 is sent through R2748, the second input to the minority gate. Counter 2000 information comes from P11 pin J through R2746 as the third input to the minority gate. The high-low-high at the base of Q2751 turns it on, sending a low through R2751, one input to a NAND gate composed of R2751, R2754, R2759, and Q2760. The low at the collector of Q2751 also goes to the cathode of D2753, which is part of an OR gate composed of D2753 and D2778.

The Upper MINUS at P11 pin 6 is a high, and goes through R2753 to the emitter of Q2753. The high at the collector of Q2753 goes through R2754, the other input to NAND gate R2751-R2754-R2779-R2760. This NAND gate requires a low-low input in order for Q2760 to conduct and deliver a high output. The information at the NAND gate's input is low-high and Q2760 is turned off, sending a low through R2760. Resistors R2760-R2761-R2771-R2772 form a two-input AND gate.

Since Counter MINUS from P11 pin 5 is a high, the collector of Q2751 is a low, the OR gate (D2753-D2778) has a high-low applied, and is sending a low to the AND gate (R2760-R2761-R2771-R2772). The other input to the AND gate is a low-low, which sends a low to Q2771's base. The low-low turns Q2771 off, sending a high from the collector of Q2771 to P11 pin 2. A high at P11 pin 2 indicates that the Counter input is not greater than the Upper Limit setting. This information is sent to the limit lamp storage section of the Counter board.

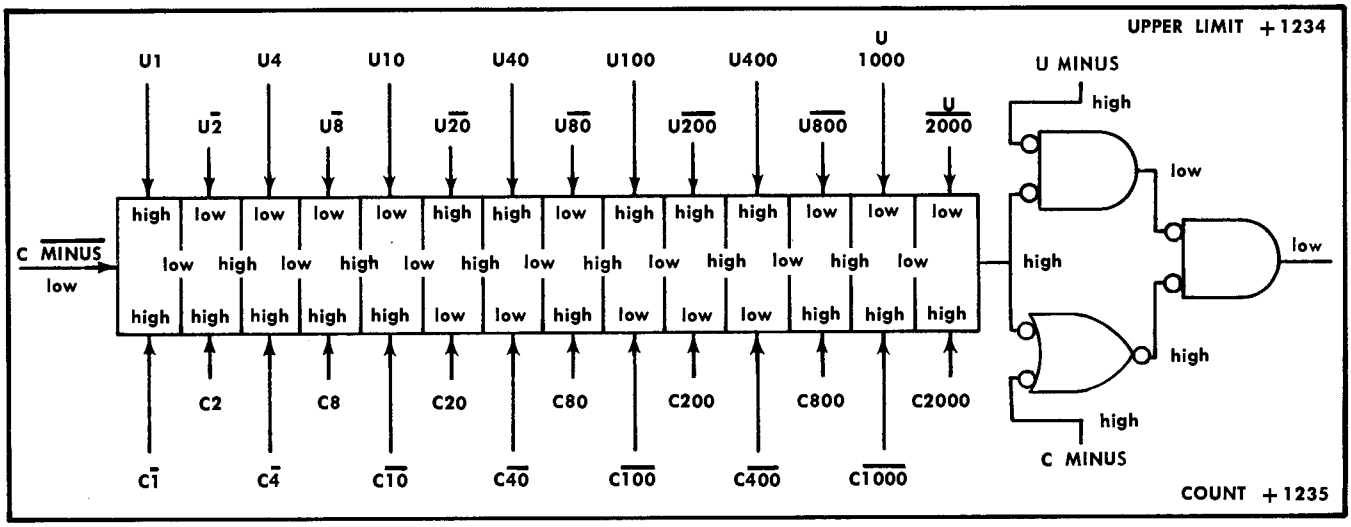


Fig. 4-45. Example 2. Comparison of +1234 upper limit with +1235 count.

Example Two

Upper Limit Setting ..... +1234

Nixie Readout ..... +1235

The illustration in Fig. 4-45 is a simplified logic diagram of the upper limit comparator. The binary inputs are such that the Count input is exceeding the Upper Limit setting. All of the lines coming into the top of the comparator string are Upper Limit information lines. Each of the odd inputs to the comparator string is inverted, such as Counter $\overline{1}$, Upper $\overline{2}$, etc. The diagram shows that the Counter and Upper Limit inputs after comparison cause a low (GREATER) to be sent to the limit lamp storage circuits for readout.

Example Three

Upper Limit Setting ..... +0001

Nixie Readout ..... —0002

The illustration in Fig. 4-46 is another logic diagram of the upper limit comparator. The binary inputs are such that although the Count exceeds the Upper Limit in numerical quantity, the negative Count is considered to be algebraically less than the positive Limit. The output of the upper limit comparator is therefore a high signifying $\overline{\text{GREATER}}$ to the limit lamp storage section.

Example Four

Upper Limit Setting ..... —1234

Nixie Readout ..... —1232

The illustration in Fig. 4-47 is a logic diagram of the upper limit comparator. The binary inputs are such that both the Count and Upper Limit are negative. Although the absolute value of the Upper Limit is greater than the absolute value of the Count, the negative Upper Limit is considered algebraically less than the negative Count. The upper limit comparator sends an output of a low indicating to the lamp storage section that the Count is exceeding the Upper Limit.

Lower Limit Comparator

The lower limit comparator functions exactly as the upper limit comparator, with the exception of the output section. This discussion will cover an explanation of the output section of the lower limit comparator and one example of a lower limit comparison.

The output of the 2000's minority gate is seen at the collector of transistor Q2951. This information is fed to a NOR gate composed of resistors R2951, R2958, R2959, and transistor Q2960. The other information to the NOR gate is Counter MINUS coming in at R2958. A low at either input to the NOR gate is sufficient to turn Q2960 on, which would send a high through resistor R2960 to a majority gate composed of R2960, R2962, R2974, R2971 and R2972.

The output of the 2000's minority gate is also fed directly to the cathode of D2953 to form one input to a two-input OR gate. The other input to the OR gate comes through D2978 as Counter $\overline{\text{MINUS}}$. Counter MINUS information from P11 pin 5 is sent directly to R2958 of the NOR gate mentioned in the previous paragraph, and is also sent through voltage divider R2977-R2978 to the base of Q2977, where it is inverted to become Counter $\overline{\text{MINUS}}$. The Counter $\overline{\text{MINUS}}$ information and the output of the 2000's minority gate combine in the OR gate and send information through R2971 as the second input to the majority gate. Lower MINUS information from P11 pin 4 comes through D2973 to the emitter of Q2974. The information at the collector of Q2974 is sent through R2974 to form the third input of the majority gate. The majority gate will pass the majority of the input information (e.g., a high-high-low would cause a high; a low-low-high would cause a low) to Q2971, the output transistor for the lower limit comparator. The information at the collector of Q2971 is sent to the limit lamp storage circuit on the Counter board. A high at the collector of Q2971 indicates that the Count does not exceed the Lower Limit. A low

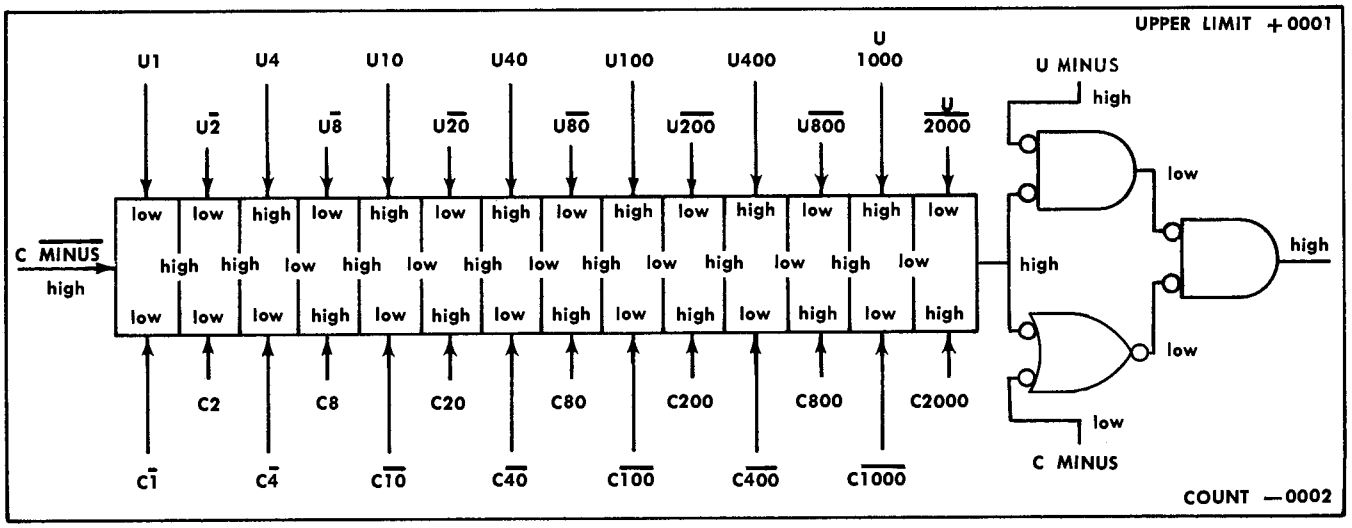


Fig. 4-46. Example 3. Comparison of +0001 upper limit with —002 count.

at the collector of Q2971 indicates that the Count does exceed or is lower than the Lower Limit.

Example Five

Lower Limit Setting ..... +1201

Nixie Readout ..... —2512

The illustration in Fig. 4-48 is a logic diagram of the lower limit comparator. The binary information inputs are such that although the Count is numerically greater (not less) than the Lower Limit setting, the opposite polarities of the two quantities causes a low at the output of the comparator. The low indicates that the Count is less than the Lower Limit.

CRT INTENSIFICATION CIRCUIT

The CRT Intensification card is composed of two separate sections; the intensification section and the scaling logic section.

Intensification Section

The intensification section (see Fig. 4-49) furnishes the CRT Z axis section of the Type 568 with intensification commands in the form of logic levels. As in the other parts of the Type 230, a logical "one" is a low or less positive level, and a logical "zero" is a high or more positive level.

The intensification command goes to the Type 568 from P10 pin B (see circuit diagram). P10 pin B is controlled by a six-input OR gate composed of Q26-Q36-Q46-Q56-Q66-Q76. When all six of the transistors are in the off condition, their output will be high. If any of the transistors are on, a low is sent to the CRT cathode to cause more trace intensity. The six inputs to the OR gate are separately controlled by AND gates. These will be discussed in the following paragraphs.

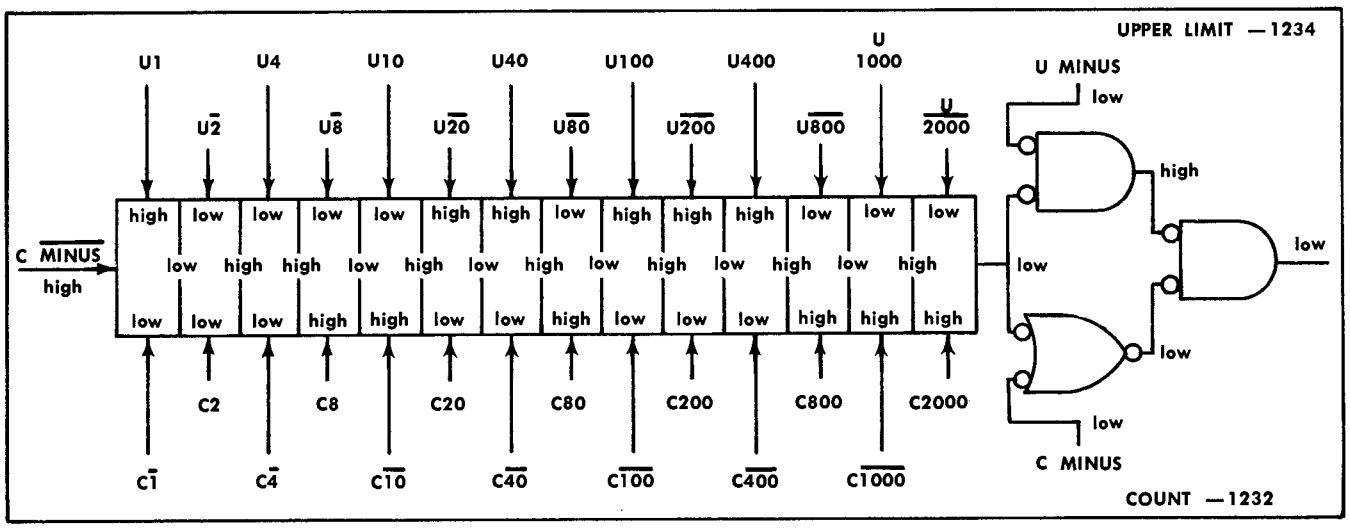


Fig. 4-47. Example 4. Comparison of —1234 upper limit with —1232 count.

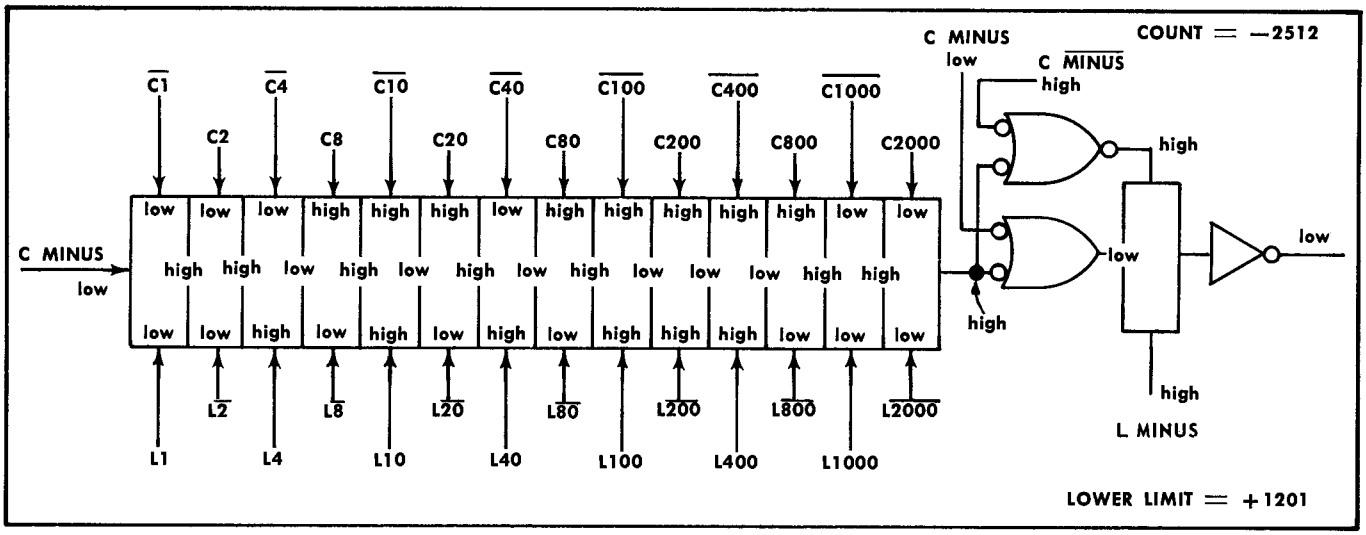


Fig. 4-48. Comparison of +1201 lower limit with —2512 count.

The alternate information at P10 pin A is high when the vertical plug-in is switched to channel A, low when the vertical plug-in is switched to channel B. or alternately high and low for channel A and B when the vertical plug-in is in the alternate or chopped mode. If the information at P10 pin A is high, it turns Q13 on, which sends a low to one input of the AND gate composed of D25, D23, and Q21. The second input to the AND gate is D23, which receives 0% BRIGHTEN information from P10 pin 1. The 0% BRIGHTEN information is controlled by the REFERENCE ZONES selector on the Type 230 front panel. The third input to the AND gate is the A 0% ZONE pulse from the Zone Generator circuit. The 0% ZONE pulse enters at P10 pin C and goes to the base of Q21, whose emitter is tied to D23 and D25 cathodes. In order for the A 0% ZONE to be displayed as an intensified portion of the Type 568 display, there must be a low at the inputs of Q21, D23 anode, and D25 anode. This condition causes the AND gate to send a low to the OR gate, turning Q26 on, which intensifies the trace for the duration of the A 0% ZONE pulse.

The second input to the six input OR gate is at the base of Q36, which is tied to the emitter of Q31 and the cathodes of D35 and D33. If the information at P10 pin A (ALTERNATE) is high, Q13 is on, sending a ow to the anode of D35. This enables one input of AND gate D35-D33-Q31. The second input to the AND gate comes from the Type 230 front panel REFERENCE ZONES selector through P10 pin 2 as 100% BRIGHTEN information. This information at P10 pin 2 is sent to the anode of D33 and must be low in order for the AND gate to enable 100% ZONE information. The 100% ZONE information comes from the 100% Zone Generator, enters P10 at pin D and goes to the base of Q31. When the 100% zone occurs, a low is put on the base of Q31 which enables the third input of the AND gate controlling Q36. If the AND gate sends a low to Q36, it will turn on and intensify the trace for the duration of the 100% ZONE.

The third input to the six-input OR gate is at the base of Q46, which is controlled by D45, D43, and Q41. These three components comprise a three-input AND gate. The ALTERNATE information from P10 pin A, after buffering is applied to the anode of D45. When the B channel of the vertical plug-in is selected, P10 pin A is low, which enables the D45 input to the AND gate. The 0% BRIGHTEN level at P10 pin 1 is sent to the anode of D43. If this level is low, it enables the D43 input to the AND gate. The third input is the B 0% ZONE pulse from the B Zone Generator card. B 0% ZONE comes into P10 at pin E to the base of Q41. If all three of the inputs to the AND gate are low, the AND gate sends a low to the base of Q46, turning it on. The on condition of Q46 will intensify the Type 568 trace for the duration of the B 0% ZONE pulse.

The fourth input to the six-input OR gate is at the base of Q56, which is controlled by an AND gate comprised of D55, D53, and Q51. The ALTERNATE level from J10 pin A, after buffering is applied to the anode of D55. When the B channel of the vertical plug-in is selected, P10 pin A is low, which enables the D55 input of the AND gate (D55-D53-Q51). The 100% BRIGHTEN level at P10 pin 2 is sent to the anode of D53. If this level is low, it enables the D53 input to the AND gate. The third input to the AND gate is the B 100% ZONE, which enters P10 via pin F to the base of Q51. If the B 100% ZONE pulse is present (low), the AND gate's third input is enabled. When all three of the inputs are low, the AND gate sends a low to the base of Q56, turning it on. Thus the Type 568 trace will be intensified for the duration of the B 100% ZONE.

The fifth input to the six-input OR gate (Q26-Q36-Q46-Q56 -Q66-Q76) is at the base of Q66, which is controlled by a five-input AND gate composed of D67, D66, D65, Q63 and Q61. ALTERNATE information at P10 pin A is inverted by transistor Q13 and goes to the anode of D67 to form the first input of the five-input AND gate. If P10 pin A is high, Q13's collector will be low, enabling the D67 input to the AND gate. MEASURE BRIGHTEN level at P10 pin 3 is low when the Type 230 front panel TIME MEASUREMENT switch is ON. This level is sent to the anode of D66 to enable the second input to the AND gate. The $\overline{\text{VOLTS}}$ input at P10 pin

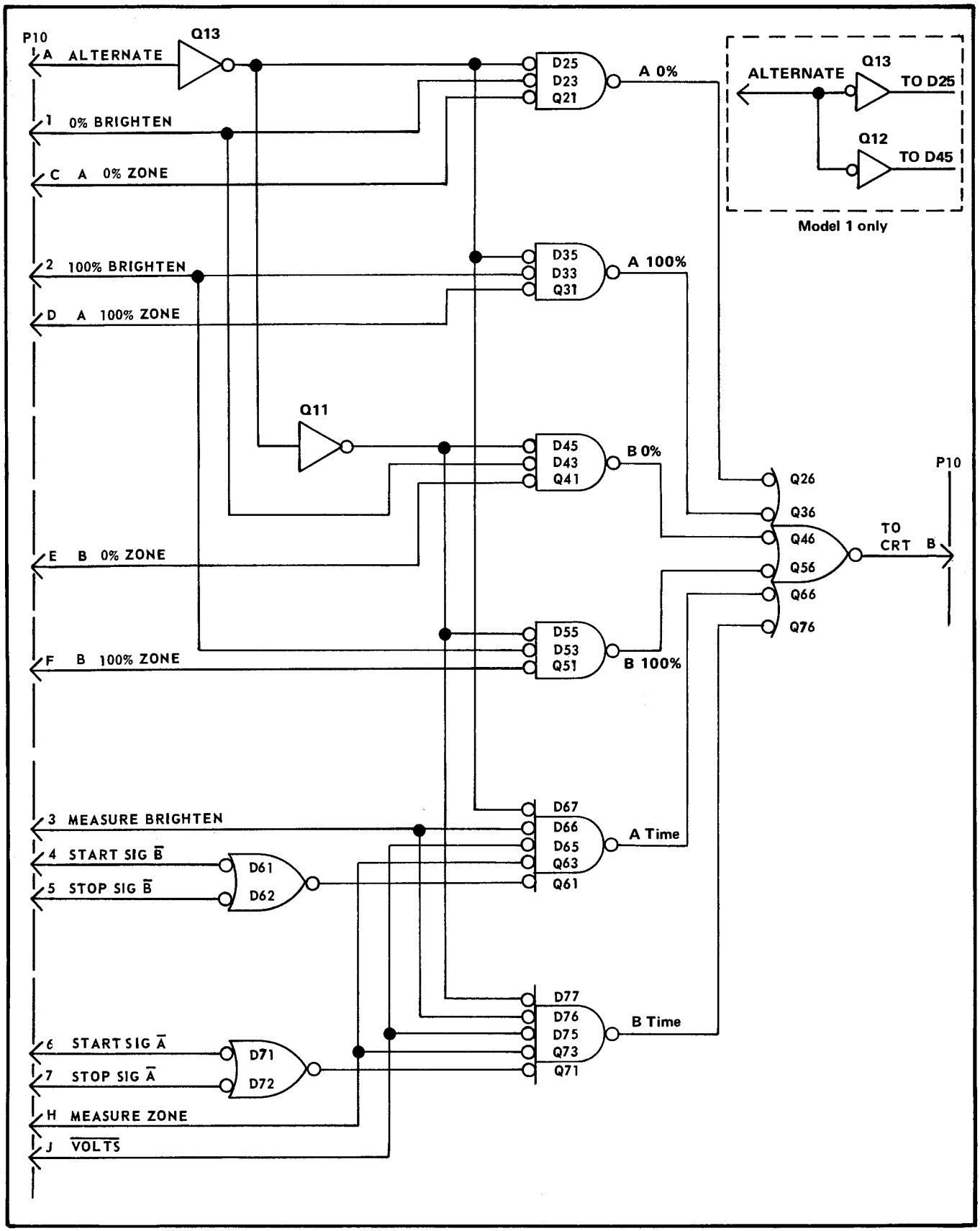
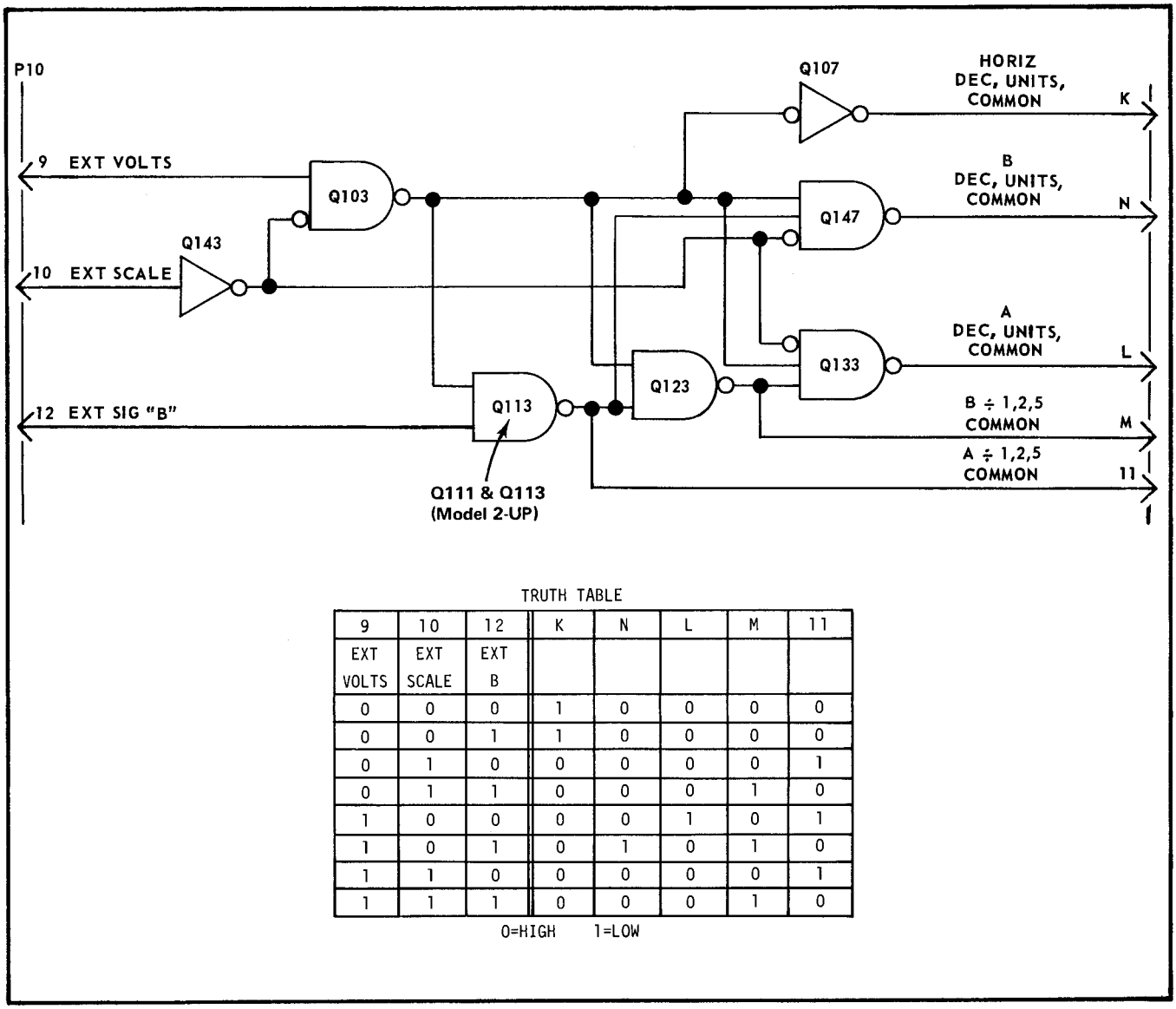


Fig. 4-49. CRT intensification logic diagram.



TRUTH TABLE

9 EXT VOLTS	10 EXT SCALE	12 EXT B	K	N	L	M	11
0	0	0	1	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	1	0	0	0	1	0
1	0	0	0	0	1	0	1
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	1
1	1	1	0	0	0	1	0

0=HIGH 1=LOW

Fig. 4-50. Scaling logic diagram.

J comes from the start and stop comparators. In order for P10 pin J to be low, the Type 230 must be in either internal time measurement mode or externally programmed for time measurement. If the Type 230 is in a time measurement mode, the D65 input to the AND gate will be enabled. MEASURE ZONE from the Clock card comes from P10 pin H to the base of Q63 to form the fourth input to the AND gate. The fifth input at the base of Q61 is controlled by a two-input OR gate composed of D61 and D62. The inputs to the two diodes are at P10 pins 4 and 5. Both pins are furnished information by the $\overline{B}$ SIGNAL outputs of the start comparator and the stop comparator. Whenever measurements are being made of the A signal, the $\overline{B}$ SIGNAL inputs will be low, enabling the intensification of the time measurement of the A signal. Conversely, if the time measurement is of the B signal, P10 pins 4 and 5 will both be high, and intensification of the Channel A trace is inhibited. When all five inputs to the AND gate are low, the AND gate will send a low to the Q66 input of the six-input OR gate, which will then intensify the trace for the length specified by the MEASURE ZONE waveform.

The sixth input to the OR gate is at the base of Q76. The base of Q76 is controlled by a five-input AND gate. This AND gate is composed of D77, D76, D75, Q73, and Q71. The ALTERNATE information from P10 pin A, after buffering, is applied to the anode of D77. P10 pin A must be in a low state (channel B) in order to enable the D77 input to the AND gate. MEASURE BRIGHTEN at P10 pin 3 comes into the AND gate at the anode of D76. MEASURE BRIGHTEN must also be low to enable the second input to the AND gate (D76 anode). $\overline{\text{VOLTS}}$ from P10 pin J comes into the AND gate at the anode of D75. When $\overline{\text{VOLTS}}$ is low, the D75 input to the AND gate is enabled. MEASURE ZONE at P10 pin H to the base of Q73 is the fourth input to the AND gate. It also must be low to enable the AND gate. The fifth input to the AND gate is at the base of Q71. It is controlled by a two-input OR gate comprised of D71 and D72. The $\overline{A}$

TRUTH TABLE

P10 Pins

1	2	3	4	5	6	7	A	C	D	E	F	H	J	Intensified Area
1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	0	1	ϕ	ϕ	ϕ	ϕ	ϕ	A 0% Zone
ϕ	1	ϕ	ϕ	ϕ	ϕ	ϕ	0	0	1	ϕ	ϕ	ϕ	ϕ	A 100% Zone
1	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	1	ϕ	ϕ	1	ϕ	ϕ	ϕ	B 0% Zone
ϕ	1	ϕ	ϕ	ϕ	ϕ	ϕ	1	ϕ	ϕ	ϕ	1	ϕ	ϕ	B 100% Zone
ϕ	ϕ	1	1	ϕ	ϕ	ϕ	0	ϕ	ϕ	ϕ	ϕ	1	1	A Measure Zone Start
ϕ	ϕ	1	ϕ	1	ϕ	ϕ	0	ϕ	ϕ	ϕ	ϕ	1	1	A Measure Zone Stop
ϕ	ϕ	1	ϕ	ϕ	1	ϕ	1	ϕ	ϕ	ϕ	ϕ	1	1	B Measure Zone Start
ϕ	ϕ	1	ϕ	ϕ	ϕ	1	1	ϕ	ϕ	ϕ	ϕ	1	1	B Measure Zone Stop

SIGNAL from the start comparator comes in at P10 pin 6 to the cathode of D71. The $\bar{A}$ SIGNAL from the stop comparator enters at P10 pin 7 and goes to the cathode of D72. Either of P10 pins 6 or 7 low will send a low to the AND gate, enabling the Q71 input. This in turn will (if all five inputs are low) turn Q76 on and intensify the trace for the time duration of MEASURE ZONE.

The following table is a list of input combinations which will intensify the Type 568 trace. As far as this circuit's logic is concerned, it is possible for the trace to be intensified by more than one combination simultaneously. In the table below, a 1 signal is equal to a low, a 0 is equal to a high. The symbol ϕ signifies "don't care." Each horizontal line and its binary combination represents one case where intensification will occur.

Scaling Section

The scaling logic section of the CRT Intensification card is a group of logic gates which enable the correct "common" lines to the vertical and the horizontal plug-in units. Enabling one of the plug-in "commons" allows it to control the scale factor of the front panel readout.

Fig. 4-50 shows the logic diagram of the scaling logic section of the CRT Intensification circuit and a truth table illustrating the input conditions required to attain a particular enabling output. As in the remainder of the instrument, a logical one is a low level, a logical zero is a high level.

The EXTERNAL SCALE input at P10 pin 10 comes from the external programming input (J202 pin 26). When P10 pin 10 is low, Q143 is off. Turning Q143 off disconnects the emitters of Q103, Q147 and Q133. Disconnecting the emitter of Q103 causes it to be off, and a high is at the collector of Q103. This high is sent to five places:

1. A high at the emitter of Q107 will turn it off, and its collector moves high. The high at Q107's collector is passed to P10 pin K (HORIZONTAL DECIMALS and UNITS COMMON) and disables the horizontal plug-in's capability to control the time measurement scale factor.

(Model 2-up). 2. The second input from the collector of Q103 is a two-input NAND gate composed of R114 (from the collector of Q103) and Q111 and Q113. In order for Q113 to be on, the input end of R114 must be high and P10 pin 12 (EXTERNAL SIGNAL B) must be high, holding Q111 in conduction. Both inputs are applied to the base of Q113.

(Model 1). 2. The second input from the collector of Q103 is a two-input NAND gate composed of R111, R112, R113 and Q114. In order for Q113 to be on, the input end of R114 must be high and P10 pin 12 (EXTERNAL SIGNAL B) must be high. The input to P10 pin 12 comes through D111 and voltage divider R111-R112-R113 to the base of Q113.

3. The third input from the collector of Q103 is to a two-input NAND gate composed of R118 (from the collector of Q113), R119 (from the collector of Q103), and Q123. The collectors of Q103 and Q113 must be both high in order to turn Q123 on and send a low to P10 pin M, the B ÷ 1, 2, 5 enabling output.

4. The fourth input from the collector of Q103 is to the three input gate composed of R113 (from the collector of Q103, R131 (from the collector of Q123), and Q133. The emitter of Q133 is inhibited by an off condition of Q143 which is off when the EXTERNAL SCALE input at P10 pin 10 is low. In addition to Q133's emitter being low, the collectors of Q103 and Q123 must be high for Q133 to be on. When Q133 is on, its collector sends a low to P10 pin L to enable the A DECIMAL, UNITS, COMMON in the vertical plug-in.

5. The fifth input from the collector of Q103 is a three input gate composed of R148 (from the collector of Q103), R146 (from the collector of Q113) and Q147. The emitter of Q147 is inhibited by an off condition of Q143 when the EXTERNAL SCALE input at P10 pin 10 is low. In order for Q147 to go on, EXTERNAL SCALE must be high, which pulls Q143's collector low, and enables the emitter of Q147. In addition to an enabled emitter, Q147 must have a high at the collectors of Q103 and Q113. When Q147 is turned on, its collector is low, and P10 pin N is low. The low at P10 pin N enables the B DECIMALS, UNITS, COMMON in the vertical plug-in.

LOW VOLTAGE POWER SUPPLY

General

The low-voltage power supply circuit provides the operating power for this instrument from six regulated supplies. Electronic regulation is used to provide stable, low-ripple output voltages. Each regulated supply contains a short-protection circuit to prevent instrument damage if a supply

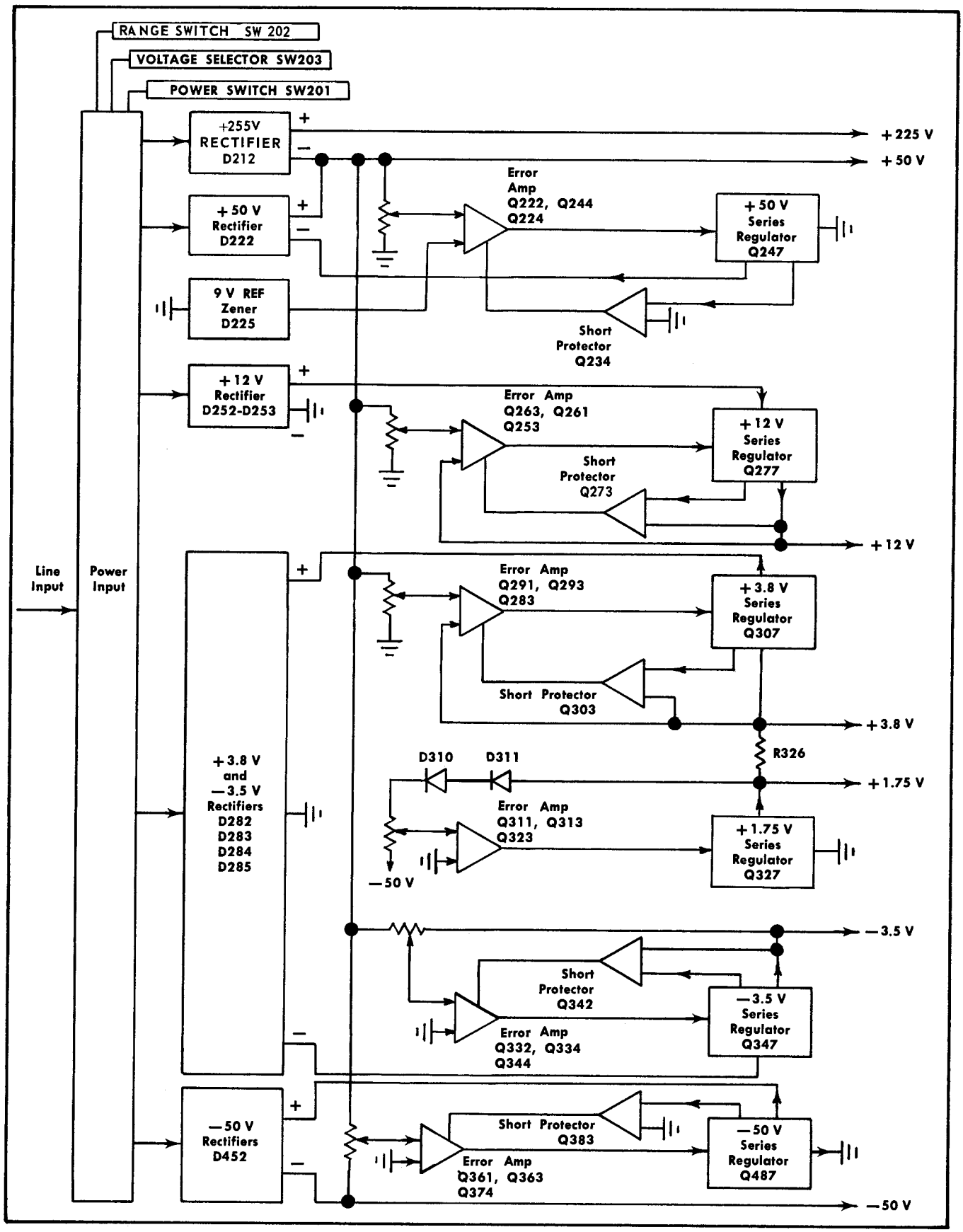


Fig. 4-51. Power supply and regulator block diagram.

is inadvertently shorted to ground. The power input stage includes the Voltage Selector assembly. This assembly allows selection of the nominal operating voltage regulating range for the instrument. Fig. 4-52 shows a detailed block diagram of the power supply circuit. A schematic of this circuit is shown at the rear of this manual.

Power Input

Power is applied to the primary of T201 through the 115V line fuse F201, POWER switch SW201, thermal cutout TK201, Voltage Selector switch SW 202 and Range Selector switch SW203. Voltage Selector switch SW 202 connects the split primaries of T201 in parallel for 115-volt nominal operation, or in series for 230-volt nominal operation. A second line fuse, F202 is connected into the circuit when the Voltage Selector switch is set to the 230-volt position to provide the correct protection for 230-volt operation. For 230-volt operation F202 current rating is one-half of F201 and although F201 is still in series with the primary, F202 takes protection precedence over F201.

The fan is connected across one half of the split-primary winding so it always has about 115 volts applied to it. The Range Selector switch, SW 203, allows the instrument to regulate correctly on higher or lower than normal line voltages. Each half of the primary has taps above and below the 115-volt (230) nominal point. As the Range Selector switch, SW230 is switched from LO to HI, the turns ratio is decreased. This provides a fairly constant voltage in the secondary of T201 even though the primary voltage has increased. Thermal cutout TK201 provides thermal protection for this instrument. If the internal temperature of the instrument exceeds a safe operating level, TK201 opens to interrupt the applied power. When the temperature returns to a safe level, TK201 automatically closes to re-apply the power.

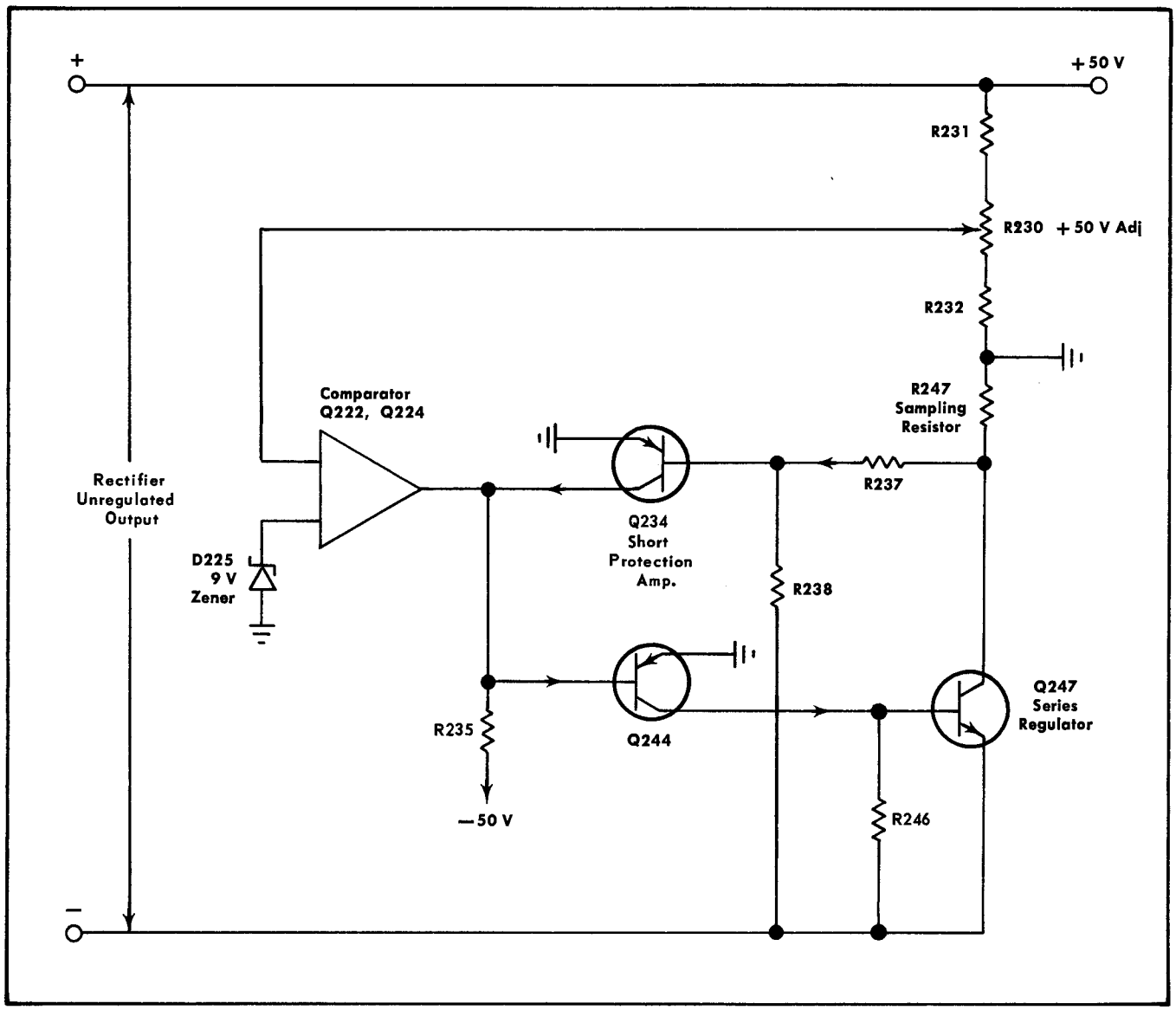


Fig. 4-52. +50-volt regulator simplified diagram.

+50-Volt Power Supply

The +50-Volt Supply (see Fig. 4-52) is the prime reference supply since it provides the reference voltage for the other supplies. The output from the secondary of T201 is rectified by bridge rectifier D222. This voltage is filtered by C222 and then applied to the +50-volt series regulator stage to provide a stable output voltage. The series regulator can be compared to a variable resistance which is changed to control the output current. The current through the series regulator stage is controlled by the error amplifier to provide the correct regulated output voltage. Reference voltage for the comparator is provided by zener diode D225 which sets the base of Q222 at about +9 volts. The base level of Q224 is determined by voltage divider R230-R231-R232 between the output of this supply and ground. R230 is adjustable to set the output voltage of this supply to +50 volts. Q222-Q224 of the comparator responds to the change that R230 presents to the base of Q222 allowing the output current of the error amplifier stage to control the conduction of the series regulator stage. This output current changes to maintain equal voltages at the bases of Q222 and Q224. This occurs as follows: If the +50 Volts adjustment (R230) is turned clockwise, Q224 base and Q222-Q224 emitters tend to go more positive than the base of Q222, and the current through Q222 increases. Increased current through Q222 produces more voltage drop across R235 and the base of Q224 goes positive. This results in a decrease in current through Q224, allowing the base of Q247 to go more negative. The base of Q247 going more negative decreases current through Q247 and the load, thereby decreasing the output voltage. This reduces the voltage across divider R230-R231-R232 and the divider action returns the base of Q224 to about +9 volts. A similar but opposite action takes place when R230 is turned counterclockwise so the base of Q224 is more negative than the base of Q222. The +50-Volt adjustment, R230, is set to provide a +50-volt level at the output of this supply.

The output voltage is regulated to provide a constant voltage to the load by feeding a sample of the output back to the series regulator, Q247. For example, assume that the

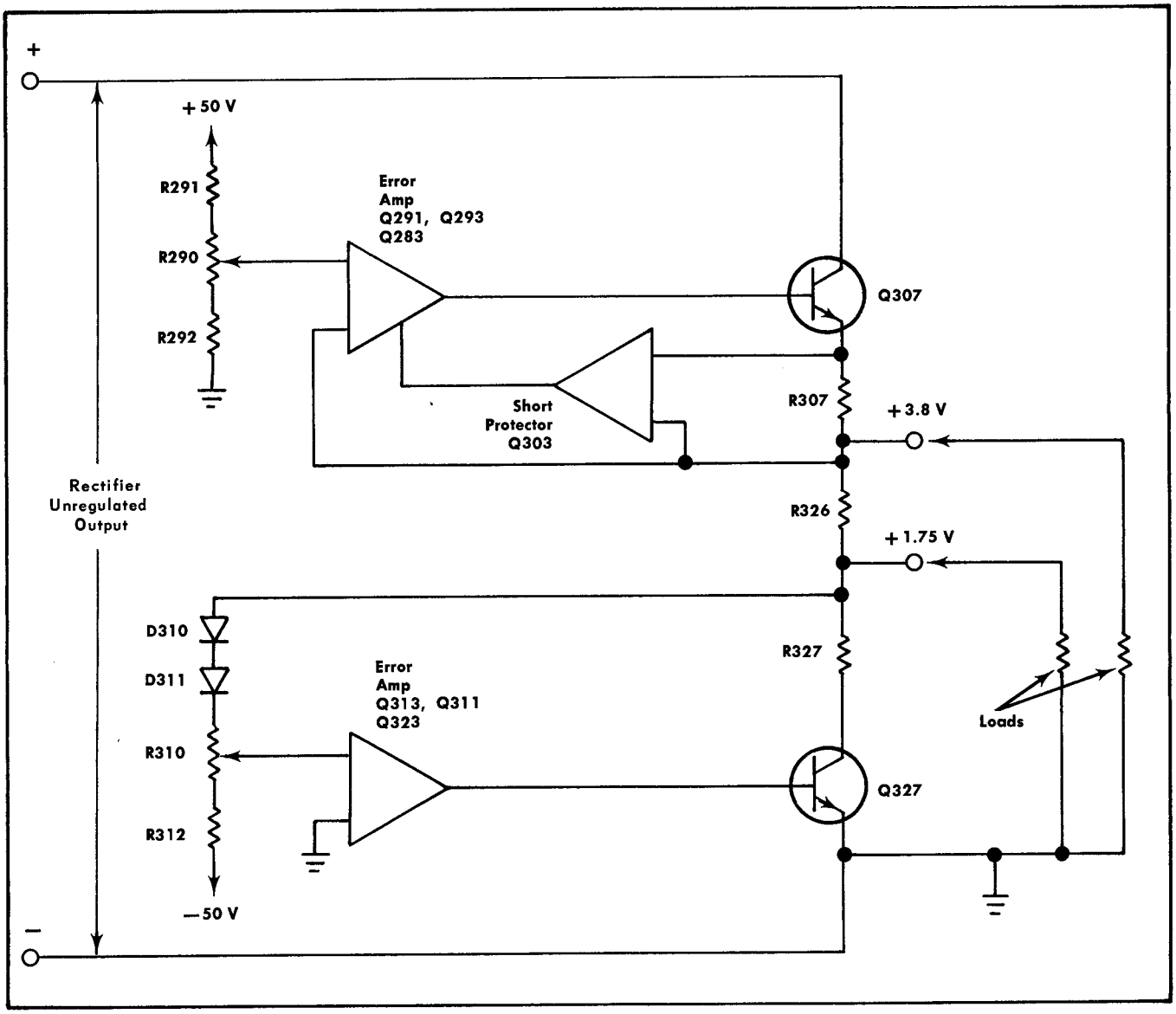


Fig. 4-53. Simplified diagram of the +3.8 volt and +1.75 volt regulators.

output voltage increases (more positive) because of a change in load or an increase in line voltage. This positive-going level at the output is applied across voltage divider R230-R231-R232 and the base of Q224 goes positive also. This reduces the current flow through Q224. Increasing current through Q222 causes its collector to go positive. When the collector of Q222 goes positive, the bias on Q224 is decreased allowing the base of Q247 to go more negative. Reduced current through Q247 also means that there is less current through the load and the output voltage decreases (less positive). In a similar manner, the series regulator and error amplifier stages compensate for the output changes due to ripple.

The short-protection amplifier stage, Q234, protects the +50-Volt Supply if the output is shorted. For normal operation, the emitter-base voltage of Q234 is not enough to bias it on. However, when the output is shorted, high current flows through R247. The voltage drop across R247 becomes sufficient to forward bias Q234 and its collector current produces an increased voltage drop across R227. The increased voltage drop across R227 reduces the current flow of both Q244 and Q247 to limit the output current. Further limiting of the output current is provided by voltage divider R237 and R238 which senses the increase in unregulated voltage across Q247, and adds to the increasing base current of Q234. This results in a further decrease of current through R247 and Q247.

+12-Volt Supply

Full wave rectified voltage for operation of the +12-Volt Supply is provided by D252-D253. The voltage is filtered by C253 and connected to the +12-volt series regulator stage to provide a stable output voltage in a manner similar to that described for the +50-Volt Supply. For example, assume that the output voltage increases (more positive) because of a change in load or an increase in line voltage. This positive-going level is applied to the base of Q261 through R268. The current in the differential amplifier (Q263-Q261) is shifted so that more current flows through Q261 than through Q263. The current through R267 also increases, which causes the base of emitter follower Q253 to go more negative. This in turn causes the emitter of series regulator transistor Q277 to go more negative. This action restores the +12-Volt Supply back to the preset value determined by voltage divider R260-R261-R262.

Shorting protection is provided by R276-R277-R273-R257 and Q273. R257 and R273 are provided to sense the line voltage relative to the +12-Volt Supply. It is desired to limit the current at a lower value at high line voltage than at low line voltage. This provides protection for Q277. R276-R277 sense the current flowing through Q277. Voltage divider R273-R257 contributes a small positive voltage in addition to the voltage drop across R276-R277 at the base of Q273. The higher the line voltage the greater the voltage contribution from R273-R257 to the base of Q273. When sufficient current is drawn from the supply, Q273 will be turned on and the supply voltage will collapse, because Q273 has depleted the current available to Q253 to maintain the supply at +12 volts.

+3.8-Volt, +1.75-Volt and —3.5-Volt Supplies

Power for these supplies is taken from one source. The output from the secondary to T201 is rectified by two separrate full wave rectifiers D282-D283 and D284-D285. D282-D283 rectifiers supply a positive voltage which is filtered by C283 and then applied to the +3.8-volt series regulator stage. D284-D285 supplies a negative voltage which is filtered by C284 and then applied to —3.5-volt series regulator stage. Both the +3.8-Volt and 3.5-Volt Supply regulator circuits operate in a manner similar to the supplies described previously.

Operation of the +1.75-Volt Supply is as follows:

The rectified voltage from D282-D283 is applied to series regulator and current sensing resistor R307 and shunt regulator Q327 to produce a +3.8-Volt Supply. The +1.75-Volt Supply is derived from a voltage divider across the +3.8-Volt Supply (see Fig. 4-44). The voltage divider consisting of R326-R327-Q327 connected between the +3.8-Volt Supply and ground drops the +3.8 volts to +1.75 volts. To maintain a constant voltage drop across R326, a sample of the 1.75 volts is referred to the error amplifier, allowing shunt current regulator Q327 to adjust the current through R326 to a constant value. This provides a constant +1.75 volt output with varying load. R290 (+3.8 Volts) and R310 (+1.75 Volts) are controls to set the output voltages of these supplies to their required values. As this supply is derived from the +3.8-Volt Supply, any excessive current of the +1.75-Volt Supply will flow through the short circuit protection sampling resistor, R307, which provides the same protection to the +1.75-Volt Supply as to the +3.8-Volt Supply. D310-D311 are temperature compensating diodes used to maintain the voltage output constant, resulting in constant logic levels from the integrated circuits using this voltage supply.

—50-Volt Supply

Bridge-rectifier D452 provides the rectified voltage which is connected to the —50-volt series regulator. Reference voltage for this supply is provided by voltage divider R360-R361-R362 between the regulated +50 volts and the output of this supply. Since the +50 volts is held stable by the +50-volt regulator circuit, any change at the base of error amplifier Q363-Q361-Q374 and series regulator Q347 is compensated in a manner similar to that described for the +50-Volt Supply. The —50-Volts adjustment, R360, sets the quiescent conduction level of the error amplifier stage to provide an output level of —50 volts.

Shorting protection is provided by Q383 and R487 in a manner similar to the other supplies.

+255-Volt Supply

Half wave rectification for operation of the +255-Volt Supply is provided by D212 in conjunction with the regulated +50-Volt Supply as a "booster" voltage. The voltage is filtered by an RC type network composed of C212A-C212B-R212-R215 and connected to an emitter follower type regulator (Q2343), located on the Counter circuit board. This circuit provides partial regulation of +200 volts by the use of the regulated +50-Volt Supply and neon B2341.

NOTES

SECTION 5
MAINTENANCE

Introduction

This section of the manual provides information on preventive maintenance for servicing the Type 230, troubleshooting procedures for locating trouble, and corrective maintenance for repairing the instrument. Preventive maintenance performed on a regular basis helps prevent instrument failure and improves the mechanical and electrical reliability of the instrument. If trouble should occur in the instrument, corrective maintenance should be performed immediately to prevent additional damage and to restore the instrument to its proper operation.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, lubrication, visual inspection and recalibration. The Type 230 should be checked every 1000 hours of operation or every six months, whichever occurs first. If the instrument is subjected to adverse environmental conditions such as excessive dust, high temperature or high humidity the frequency of the checks should be increased.

Access to the Interior

The top and bottom dust covers of the Type 230 can be easily removed for access to the internal circuitry. The covers are secured to the frame with slotted-head fasteners that can be releasd by turning each fastener 1/4 turn counterclockwise. The covers should be re-installed on the instrument for normal operation to keep out dust and provide proper distribution of the air flow.

The front panel is hinged and can be opened for access to the circuit cards, front panel switches, etc. To open the front panel, unscrew the two slotted thumbscrews at the left side of the front panel and swing the front panel out and to the right.

Cleaning

Clean the instrument often enough to prevent accumulation of dirt. Dirt on the components acts as a thermal insulating blanket preventing heat dissipation and it may provide electrical conducting paths.

Air Filter. Under normal operating conditions the air filter should be checked every few weeks and cleaned if dirty. More frequent cleaning may be required if the instrument is used in a smoky or dusty environment. Remove the filter by pulling it out of the frame on the rear of the instrument. To clean the filter, wash it thoroughy in a mild detergent solution. Rinse the filter in clear water and let it dry; then coat it with an air-filter adhesive available from air-conditioner suppliers or from Tektronix (Part No. 066-0058-00). Let the adhesive dry thoroughly before re-installing the filter.

Exterior. The outside of the instrument can be cleaned by wiping with a soft cloth. A small paint brush is useful in removing dust from the front-panel controls. Hardened dirt or grease may be removed with a soft cloth dampened in a water and mild detergent solution. Abrasive cleaners should not be used.

Interior. Clean the interior of the instrument by loosening the accumulated dust with a dry, soft paint brush. Remove the loosened dust by vacuum or by blowing it out with a low-velocity stream of air. Any remaining dirt may be removed with a small cloth or a cotton-tipped applicator dampened with a solution of water and mild detergent. The plug-in circuit cards should be removed for individual cleaning. After cleaning the interior, allow the instrument to dry thoroughly before turning it on.

Lubrication of Switches and Shaft Bushings. The life of selector switches and other moving parts can be lengthened by keeping them properly lubricated. Use a cleaning type lubricant (such as Cramoline) on shaft bushing, interconnecting plug contacts, and switch contacts. Use a heavier grease (Beacon grease No. 325 or equivalent) on switch detents. Do not over lubricate. The necessary materials and instructions for proper lubrication of Tektronix instruments are contained in a component lubrication kit available from Tektronix. Tektronix Part No. 003-0342-00.

Fan Oiling. During periodic servicing, the fan motor should be lubricated with a few drops of light machine oil (Anderol L826 available from Lehigh Company or Roton Distributors is recommended). An industrial hypodermic needle and syringe is used to insert the oil through the rubber seal, as shown in Fig. 5-1. Hold the syringe at a 45° angle, pierce the rubber seal, then insert the needle about 1/4 inch and depress the plunger far enough to inject 3 or 4 drops of oil into the bearing. If a syringe and needle cannot be obtained locally, they may be ordered from Tektronix (Tektronix Part No. 003-0282-00 for the syringe; 003-0285-00 for the needle).

Visual Inspection

After cleaning, the instrument should be carefully checked for such defects as poor connections, damaged parts, and improperly seated transistors and integrated circuits. The remedy for most visible defects is obvious; however, if heat-damaged parts are discovered, determine the cause of overheating before the damaged parts are replaced. Otherwise the damage may be repeated.

Transistor and Integrated Circuit Checks

Periodic checks of the transistors and integrated circuits used in the Type 230 are not recommended. The best determination of performance is the actual operation of the component in the circuit. Performance of the circuits is thoroughly

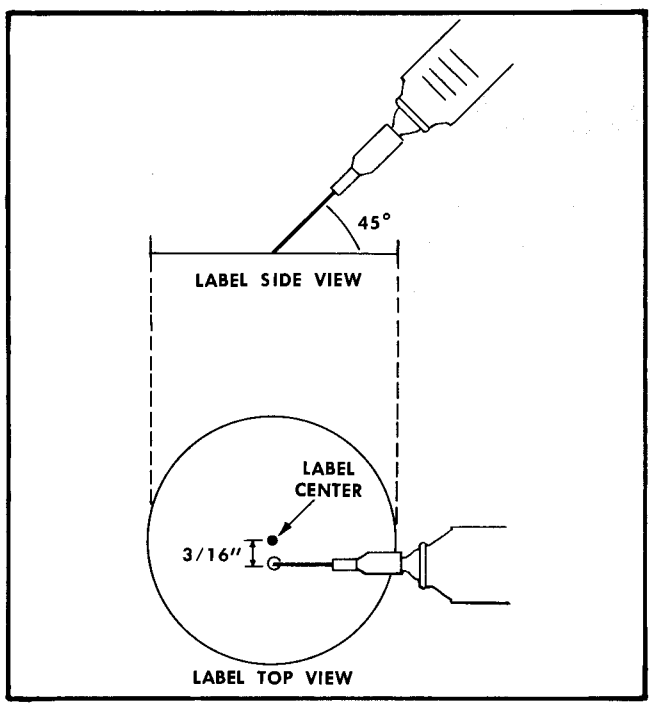


Fig. 5-1. Oiling the fan with a hypodermic.

checked during recalibration; substandard transistors and integrated circuits will usually be detected at that time.

Recalibration

To insure correct and accurate measurements, the instrument calibrated should be checked each 1000 hours of operation or at least every 6 months. Performance Check and Calibration procedures are given in separate sections of this manual.

The calibration procedure can be helpful in isolating major troubles in the instrument. In some cases, minor troubles not apparent during normal operation may be revealed and corrected during calibration.

CORRECTIVE MAINTENANCE

General

Corrective maintenance consists of component replacement and instrument repair. Special techniques or procedures required to replace components in this instrument are described here.

Obtaining Replacement Parts

Standard Parts. All electrical and mechanical part replacements for the Type 230 can be obtained through your local Tektronix Field Office or representative. However, many of the standard electronic components can be obtained locally in less time than is required to order them from Tektronix, Inc. Before purchasing or ordering replacement parts, consult the Parts List for value, tolerance and rating.

NOTE

When selecting replacement parts, it is important to remember that the physical size and shape of a component may affect its performance at high frequencies. All replacement parts should be direct replacements unless it is known that a different component will not adversely affect instrument performance.

Special Parts. In addition to the standard electronic components, some special parts are used in the Type 230. These parts are manufactured or selected by Tektronix, Inc. to meet specific performance requirements, or are manufactured for Tektronix, Inc. in accordance with our specifications. These special parts are indicated in the Parts List by an asterisk preceding the part number. Most of the mechanical parts used in this instrument have been manufactured by Tektronix, Inc. Order all special parts directly from your Tektronix Field Office or representative.

Ordering Parts. When ordering replacement parts from Tektronix, include the following information:

1. Instrument Type.

2. A description of the part (if electrical, include circuit number).

3. Tektronix Part Number.

4. Instrument Serial Number.

Soldering Techniques

CAUTION

Disconnect the instrument from the power source before soldering.

Circuit Card Soldering. It is best to remove the card from the instrument and place it in a holder in a position where both sides of the board are accessible. Use ordinary 60/40 tin-lead solder with a 35- to 40-watt pencil-type soldering iron. A higher wattage soldering iron will separate the etched wiring from the base material. The tip of the iron should be clean and properly tinned for quick heat transfer to the solder connection.

The following technique is suggested for replacing a component on a circuit card.

1. Grip one lead of the component with a pair of needle-nose pliers. If the component is known to be defective, the leads may be cut near the component body for individual removal.

2. Touch the tip of the soldering iron to the connection at the back of the board, then gently pull the lead out of the board and remove the soldering iron.

3. A clean hole should be left in the board when the lead is removed. If not, clean the hole out by reheating the connection, and insert a sharp non-metallic object such as a toothpick into the hole.

4. Remove each of the other leads and clean the holes in the same manner.

5. Clean the leads of the new component and bend them to fit the holes in the circuit card.

6. Insert the leads into the holes, making certain the component seats on the card in the same manner as the original. If it does not, reheat the connection and press the component into place.

7. Apply the soldering iron and a small amount of solder to the connection at the back of the card. Use only the amount of solder required to form a good electrical connection.

8. Check the front (component side) of the card to insure that the solder has wicked through the hole and onto the lead. On some cards it may be necessary to solder the lead on the component side of the card. If this is required, use a procedure similar to that described in step 7.

9. Clip off excess leads extending beyond the solder connection and clean the card with flux-remover solvent.

Ceramic Terminal Strip Soldering. Solder containing about 3% silver should be used for soldering on ceramic terminal strips. Occasional use of ordinary 60/40 tin-lead solder is permissible, but its repeated use or the application of excessive heat will break the silver-to-ceramic bond in the terminal notch. Silver-bearing solder is available locally from electronic distributors or may be purchased in 1-pound rolls from your Tektronix Field Office. Order by Tektronix Part Number 251-0514-00.

Use the following technique when soldering on a ceramic terminal strip.

1. Use a 40 to 75-watt soldering iron with a chisel-shaped tip.

2. Clean and tin the tip of the iron with silver-bearing solder.

3. Apply heat to the solder connection by touching the soldering iron tip to the side and base of the connection (Fig. 5-2). Do not apply pressure with the iron or insert the tip into the notch, as this may break or chip the ceramic strip.

4. Use the minimum amount of heat required to make the solder flow freely.

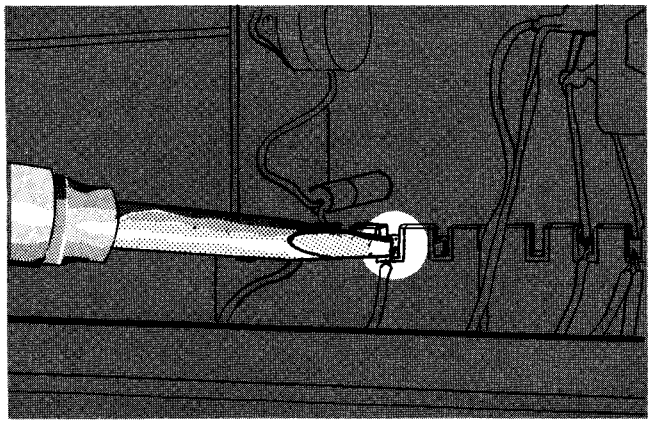


Fig. 5-2. Correct method of applying heat when soldering to a ceramic terminal strip.

5. Apply only enough solder to cover the leads; do not attempt to fill the notch with solder.

6. Cut off any excess lead length extending beyond the connection and clean the ceramic strip with a flux-removing solvent.

Metal Terminal Soldering. Use ordinary 60/40 tin-lead solder for soldering to metal terminals such as switch or connector terminals. A soldering iron with a 40 to 75 watt rating should be used and the tip of the iron should be properly cleaned and tinned.

To remove a lead or solder a lead to a metal terminal use the following techniques:

1. Hold the lead with a pair of long nose pliers. If the lead is insulated, be careful not to damage the insulation.

2. Apply the soldering tip directly to the connection until the solder begins to melt. Do not apply excessive heat.

3. Pre-tin all leads to be soldered to a connector terminal. Pre-tin by heating the lead and coating it with a small amount of solder.

4. Use the minimum amount of solder required to form a good electrical connection. Excessive solder may impair the operation of the component or form a cold solder joint.

Other Soldering Considerations. When soldering to a switch terminal, do not let the solder flow beyond or around the rivet holding the terminal on the switch wafer. The spring tension of the switch terminal may be destroyed and it will not make a good electrical connection.

When soldering a short-lead component, heat shunt the lead (Fig. 5-3) between the soldering iron tip and the component using a pair of long nose pliers.

After soldering any connection, cut off the excess length of the soldered lead. Be sure that these loose ends are not dropped into the instrument where they could cause electrical shorting.

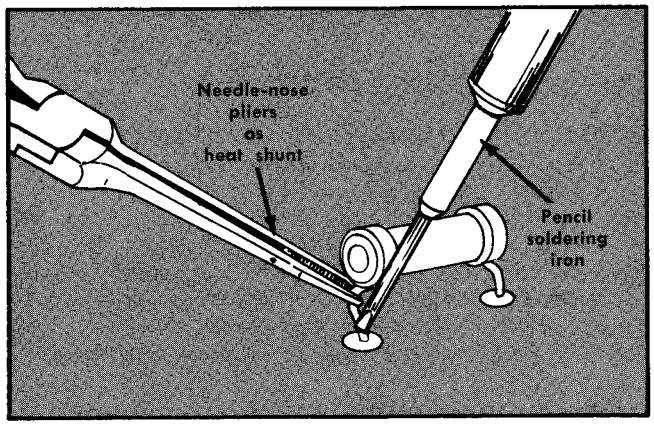


Fig. 5-3. Use of heat shunt to protect components during soldering.

Replacement Procedures

Ceramic Strip Replacement. To replace a damaged ceramic terminal strip, first unsolder all connections, then

pry the mounting studs attached to the strip out of the chassis. If prying is not satisfactory, remove the studs by tapping on the ends protruding from the reverse side of the chassis. Still another way to remove a ceramic strip is to use diagonal cutters and cut off one side of each stud. The remainder of the studs can then be pulled out after the strip has been removed.

If the nylon spacers do not come out with the studs, they may be left in the chassis or pulled out separately. The spacers, if not damaged, can be used with the new ceramic strip assembly. Replacement strips are supplied with mounting studs attached, so it is not necessary to salvage the old studs.

When the damaged strip and stud assembly have been removed, place the spacers into the mounting holes in the chassis and press the mounting studs of the new strip assembly into the spacers. It may be necessary to tap lightly or apply some pressure to the ceramic strip to make the studs seat all the way down into the spacers. To avoid damage to the terminal strip use a soft-tipped tool for tapping, and apply force only to the portion of the strip directly above the mounting studs. Fig. 5-4 shows the assembled terminal strip. Cut off the excess length of the mounting studs extending beyond the ends of the spacers. Resolder all components and wires in place as they were previously arranged (Note the soldering techniques described earlier).

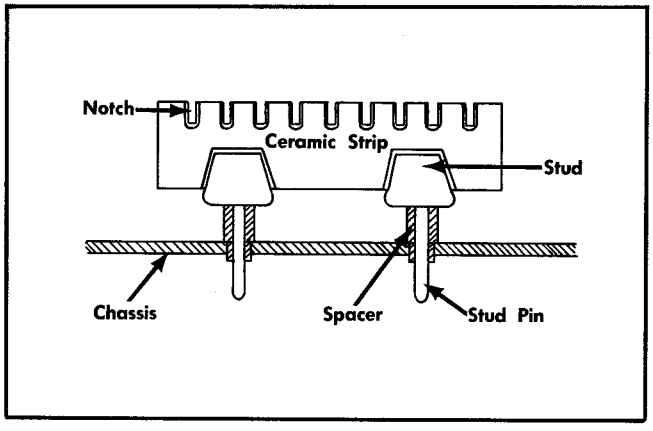


Fig. 5-4. Ceramic terminal strip assembly.

Circuit Card Replacement. If the Counter circuit board or any of the plug-in circuit cards are damaged and cannot be repaired, the damaged card should be replaced with a new card. Replacement cards may be ordered either with or without circuit components wired in place. The Tektronix part numbers are given in the Mechanical Parts List Section of this manual. To obtain a replacement card with the components soldered in place, order the circuit card assembly. (An assembly does not include socket-mounted components.)

If the Counter circuit board should need replacing, use the following procedure for removal and installation:

1. Remove the two screws which secure the plug-in circuit card retainer bar to the front-panel swing-out.

2. Disconnect all wires from the square-pin connectors. These wires may be tagged with the pin number for replacement, or the illustrations at the rear of this section may be referred to.

3. Remove the six screws securing the Counter circuit board to front-panel swing-out support spacers and remove the circuit board.

4. Remove the four nuts securing the Readout tube cover to the circuit board.

5. Remove the Readout tube cover by sliding the decimal indicator wires out through the hole in the Counter circuit board.

6. Reverse the procedure of removal for installing a new circuit board.

Switch Replacement. Individual parts of either a rotary switch or a lever switch are not normally replaceable. If one section of a switch is defective, the entire unit should be replaced. Replacement switches may be ordered either wired or unwired. Refer to the Electrical Parts List for the appropriate part number. When replacing a switch, tag the leads and switch contacts with corresponding tags. Use the old switch as a sample for wiring the new one, using the soldering techniques described earlier.

Transistor and Integrated Circuit Replacement. Transistors and ICs should not be replaced unless they are actually defective. Unnecessary replacement or switching of components may affect the calibration of the instrument. If a transistor or integrated circuit is removed during routine maintenance, be sure it is returned to its original socket.

Any replacement component should be of the original type or a direct replacement. Bend the leads to fit the socket correctly and cut off the leads the same length as the original component. Note the electrode configurations shown in Fig. 5-5.

Some of the chassis-mounted power-supply transistors use silicone grease to increase heat transfer. Replace the silicone grease when replacing these transistors.

WARNING

Silicone grease should be handled with care and should be kept away from the eyes. Wash your hands thoroughly after using it.

After any component is replaced, check the operation of that part of the circuit which may be affected.

Indicator Lamp Replacement. The EXT HOLD, READY and LIMIT lamps on the front panel may be replaced. To remove the lamps, grip the lamp just behind the lens with the fingernails of two fingers or the thumb and middle finger. To replace the lamp, align the connectors with the socket and push the lamp into place. Refer to the Parts List for the appropriate part numbers.

The plug-in relay assemblies are polarized and should be installed so that the plastic locating pin is aligned with the corresponding hole in the board. The assembly will not seat properly if installed backward. Use care in handling the assemblies, for they are delicate and should not be subjected to excessive shock. To replace a reed switch.

a. Using a tube puller, lift straight up on the defective assembly. Take care not to bend the clips on the parent board.

b. Using a toothpick or sharp instrument, push the reed switch out either end of the coil. The reed and holding block will slide out of the other end. (See Fig. 5-6.)

c. Slide the replacement reed switch into the opened end of the assembly and replace the holding block.

d. Re-install the repaired assembly on the parent board.

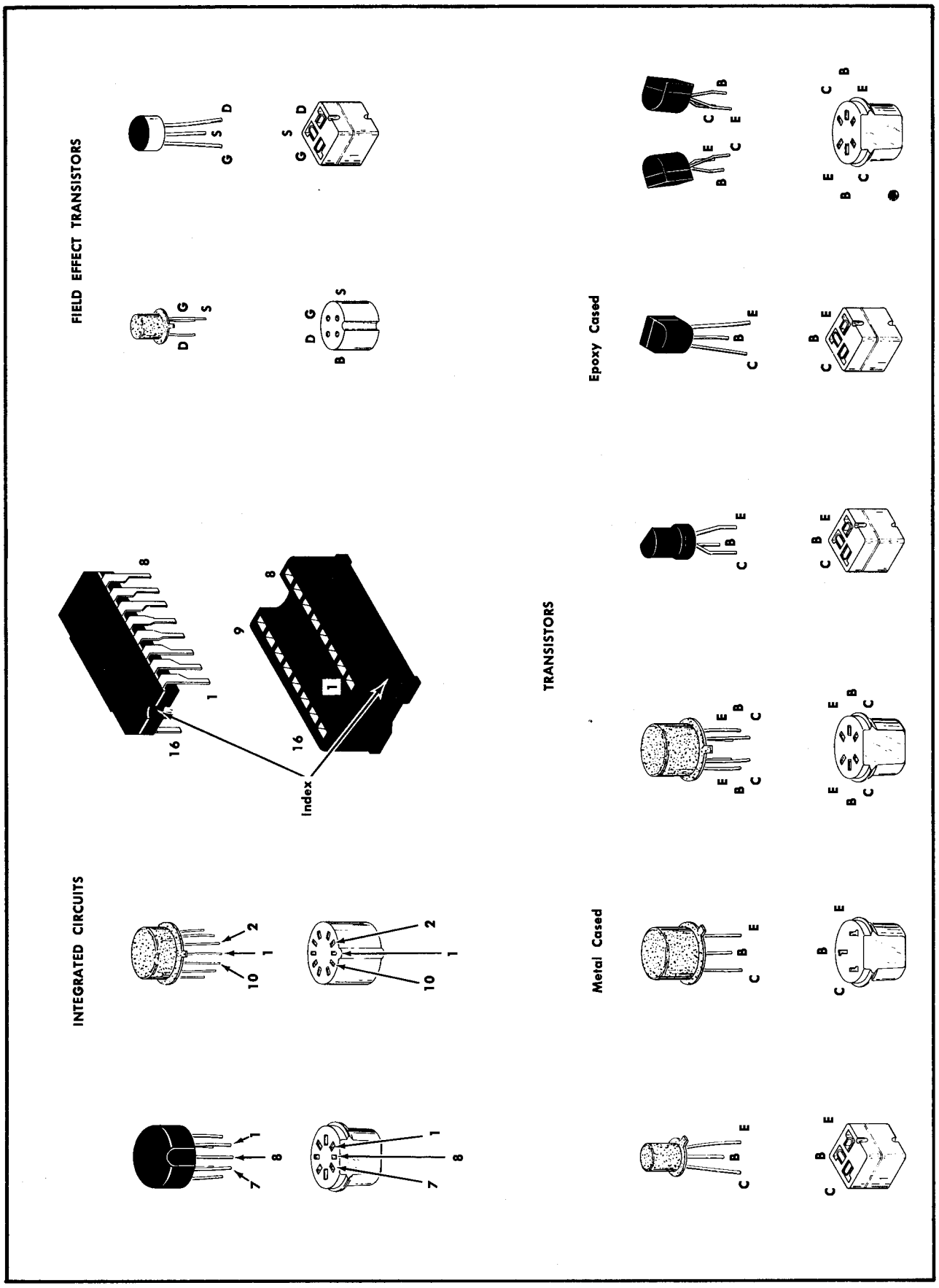


Fig. 5-5. Electrode configuration for socket-mounted transistors and Integrated Circuits, top view.

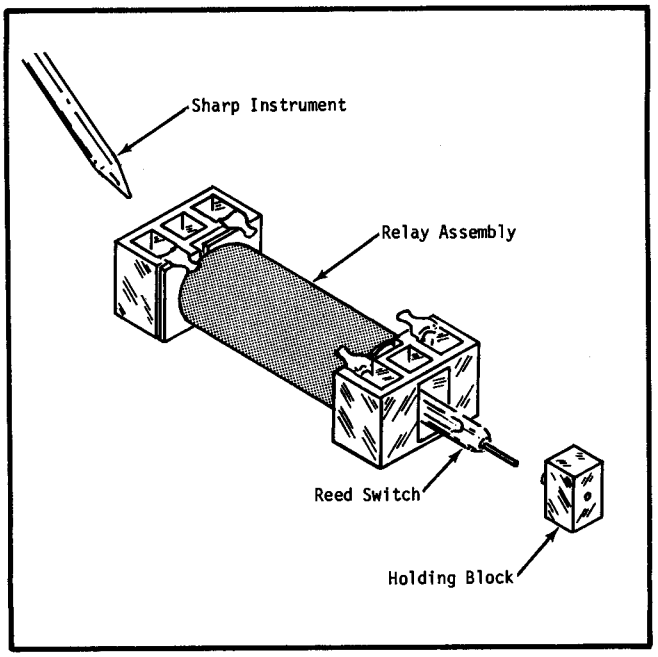


Fig. 5-6. Removal of Reed Switch.

To replace the single reed switch, insert the switch into the coil. Center the switch in the coil and solder the two axial leads to the pin connectors on the circuit board.

Power Transformer Replacement. If a complete check of the instrument shows that the power transformer requires replacement, notify your local Tektronix Field Office or representative for a warranty replacement (see the warranty note in the front of this manual). Be sure to use only the correct replacement for the power transformer.

Fuse Replacement. Both line fuses are contained in plastic holders in the cover of the LINE SELECTOR ASSEMBLY at the rear of the instrument. To remove the fuses, disconnect the line cord from the power source and remove the cover of the assembly. Push on the end of the fuse to be removed and slide it out of the holder. Replace the fuse in a similar manner, being sure the cover fits snugly against the rear panel of the instrument.

Use only the correct value replacement fuse. A smaller value will tend to blow out; a larger value will not provide adequate protection for the instrument. Only the upper fuse within the assembly (1.6-A) is used for 115-volt operation. However, for 230-volt operation both the upper fuse and lower fuse (0.8-A) must be installed.

TROUBLESHOOTING

Introduction

The following information is provided to aid in locating and correcting trouble in the Type 230. Information in the Circuit Description, Calibration and Diagrams sections is also helpful when troubleshooting the instrument.

Troubleshooting Aids

Diagrams. Circuit diagrams are given in foldout pages in Section 10. The circuit numbers and electrical values of components, as well as significant voltages and waveforms are shown on the diagrams. All front-panel and internal controls are given and all input and output connections are indicated.

Circuit Boards. The figures at the rear of this section show the circuit boards used in the Type 230. Each electrical component is identified by its circuit number, and test points are indicated. The circuit boards are also outlined on the diagrams with a blue line. The use of these illustrations along with the diagrams will aid in locating test points and components mounted on the circuit boards.

Switch Wafer Identification. Switch wafers shown on the diagrams are coded to illustrate the position of the wafer in the complete switch assembly. Rotary switch wafers are numbered from the front or mounting end of the switch, toward the rear. The letters "F" and "R" indicate whether the front or the rear of the wafer performs the particular switching function.

Wiring Color Code. All insulated wire in the Type 230 is color-coded according to the EIA standard color-code (as used for resistors) to aid in circuit tracing. The widest color stripe denotes the first color of the code. Power-supply voltage can be identified by the background color and three color stripes. A white background color indicates a positive voltage; a tan background, a negative voltage.

TABLE 5-1

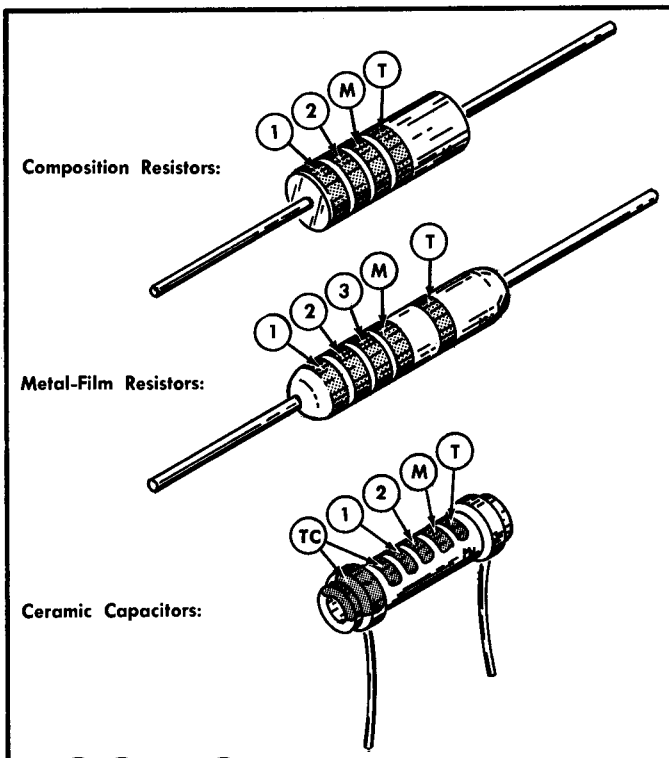
Power Supply Wiring Color Code

Supply	Background Color	1st Stripe	2nd Stripe	3rd Stripe
+250 Volt	White	Orange	Black	Brown
+50 Volt	White	Brown	Green	Black
+12 Volt	White	Brown	Red	Black
+3.8 Volt	White	Orange	Green	Brown
+1.75 Volt	White	Violet	Red	Black
−3.5 Volt	Tan	Brown	Red	Black
−50 Volt	Tan	Brown	Green	Black

Resistor Color-Code. In addition to the brown composition resistors, metal film resistors (identifiable by their grey or light blue color) are used in the Type 230. The resistance value of composition and metal film resistors is color-coded on the components with the standard EIA color-code. The color-code is read starting with the stripe nearest the end of the resistor. Composition resistors have four stripes consisting of two significant figures, a multiplier and a tolerance value. Metal-film resistors have five stripes which consist of three significant figures, a multiplier and a tolerance value. (See Fig. 5-7).

Capacitor Markings. The capacitance value of common disc capacitors and small electrolytics are marked in microfarads on the side of the component body. The white ceramic capacitors used in the Type 230 are color-coded in picofarads using a modified EIA code (see Fig. 5-7).

Diode Color-Code. The cathode end of each glass-enclosed diode is indicated by a stripe, a series of stripes, or a dot. For metal-encased diodes, the anode and cathode are indicated by the direction in which the diode symbol is marked on the case. When the diode is a JEDEC registered device, aseries of stripes indicates the diode type number using the EIA color-code system. On diodes manufactured especially for Tektronix, a four-band color code system is used, the first band of which is either blue or pink. On the latter type of diodes, the last three bands identify the diode



(1) (2) and (3) —1st, 2nd and 3rd significant figures;
(M) —multiplier; (T) —tolerance;
(TC) —temperature coefficient.

Resistor and Capacitor Color Code

Color	Significant Figures	Multiplier		Tolerance	
		Resistors	Capacitors	Resistors	Capacitors
Silver	---	10^{-2}	---	±10%	---
Gold	---	10^{-1}	---	±5%	---
Black	0	1	1	---	±20% or 2 pF*
Brown	1	10	10	±1%	±1% or 0.1 pF*
Red	2	10^2	10^2	±2%	±2%
Orange	3	10^3	10^3	±3%	±3%
Yellow	4	10^4	10^4	±4%	+100% —0%
Green	5	10^5	10^5	±0.5%	±5% or 0.5 pF*
Blue	6	10^6	10^6	---	---
Violet	7	---	---	---	---
Gray	8	---	10^{-2}	---	+80% —20% or 0.25 pF*
White	9	---	10^{-1}	---	±10% or 1 pF*
(none)	---	---	---	±20%	±10% or 1 pF*

*For capacitance of 10 pF or less.

NOTE: (T) and/or (TC) color code for capacitors depends upon manufacturer and capacitor type. May not be present in some cases.

Fig. 5-7. Standard EIA color coding for resistors and capacitors.

within a class of part numbers (e.g., a diode color-coded blue-brown-grey-green probably indicates Tektronix Part Number 152-0185-00). When in doubt, consult the Parts List.

Troubleshooting, External

Familiarity with the normal operation of the instrument is of great assistance in locating trouble. Often an apparent malfunction is the result of improper or inadequate external connections to associated equipment. If apparent trouble occurs in the Type 230, consider the following preliminary checks before proceeding with extensive troubleshooting.

Settings. Incorrect control settings of either the Type 230 or the Readout Oscilloscope can give an indication of trouble that does not exist. Operate the front-panel controls to see if any operational problems are apparent. If there is doubt about the correct use of a control or the relationship between controls, refer to the Operating Instructions section of this manual.

Check Associated Equipment. Be sure the equipment used with the Type 230 is operating correctly. Check that the rear panel cables are connected properly and that they are not defective.

Check Front-Panel Indicators. When operating the Type 230 in a programmable measurement system, the front-panel EXT HOLD and READY lamps can sometimes provide clues as to the nature of trouble. If the external hold feature is used and the EXT HOLD lamp is lighted, the trouble is probably in the external equipment. If an external trigger is used and the READY lamp remains lighted as the DISPLAY TIME control is turned throughout its range, the external trigger is not reaching the Synchronizer Circuit Card.

The READY lamp can in some cases be used for trouble isolation when the Type 230 is used without an external programmer. If the READY lamp does not light and the Nixie tubes indicate that measurements are not being made, open the front panel and pull out the Memory Circuit Cards.

CAUTION

The POWER switch should be turned off before removing or replacing a plug-in circuit card.

If the READY lamp does not light, check that the TRIGGERED MEASUREMENT switch is set for internal operation (down). If the READY lamp comes on when the Memory Circuit Cards are pulled, the trouble is probably on the Memory Circuit Cards or between the cards and the vertical plug-in unit.

Troubleshooting, Internal

The following procedure is provided to aid in isolating a trouble to a particular circuit card and to locate the trouble within the circuit on the card. If a component is found to be defective, it should be replaced following the replacement procedure given under Corrective Maintenance earlier in this section. The calibration of the circuit should be checked after any component has been replaced.

[1]Pins BB, V, X, and 18 on the Limit Circuit Card in J11. Also check pin Z of J9 (+3.8 V) and N of J5 (+225 V).

TABLE 5-2

Inter-Circuit Relationships

	Power Supplies	Zone Generators Ch A 0%	Ch A 100%	Ch B 0%	Ch B 100%	Memories Ch A 0%	Ch A 100%	Ch B 0%	Ch B 100%	Buffer Gate circuit	Sweep circuit	Volt Meter Ramp	Ch A Signal	Ch B Signal	Start Comparator	Stop Comparator	Clock	Synchronizer	CRT Intensification	D, U, ÷ 1, 2, 5, Common	Counter	Storage Register and Readout	Limit Light Storage	Limits
Power Supplies	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
Zone Generators	●									●	●							●						
Ch A 0%	●					●				●	●							●	●					
Ch A 100%	●						●			●	●							●	●					
Ch B 0%	●							●		●	●							●	●					
Ch B 100%	●								●	●	●							●	●					
Memories	●																							
Ch A 0%	●												●		●	●	●	●						
Ch A 100%	●												●		●	●	●	●						
Ch B 0%	●													●	●	●	●	●						
Ch B 100%	●													●	●	●	●	●						
Buffer	●														●	●	●	●						
Gate circuit	●	●	●	●	●												●	●						
Sweep circuit	●	●	●	●	●										●	●								
Volt Meter Ramp	●														●	●								
Ch A Signal	●					●	●								●	●								
Ch B Signal	●							●	●						●	●								
Start Comparator	●					●	●	●	●		●	●	●	●						●				
Stop Comparator	●					●	●	●	●		●	●	●	●						●				
Clock	●									●					●	●		●						
Synchronizer	●					●	●	●	●	●							●		●			●	●	
CRT Intensification	●	●													●	●	●	●						
D, U, ÷ 1, 2, 5, Common	●																●				●	●		
Counter	●																●	●						●
Storage Register and Readout	●																		●					●
Limit Light Storage	●																	●						●
Limits	●																				●		●	

CAUTION

Due to the component density on the circuit cards, care should be taken with meter leads and probe tips. Shorting of the leads can cause abnormal voltages or transients which may destroy many components.

Voltage Checks. The voltages on pins 26, 18, 20, 16 and 24 of the suspected card(s)[1] should be checked with an accurate (±3%) 20,000 Ω/volt DC voltmeter. The plug-in circuit cards may be put on the extender cards for easy access to the circuitry. The extender card has test points for all connections to the circuit card. Test conditions and voltages are given on the apron of the circuit diagram foldouts.

Card Substitution Check. Some of the plug-in circuit cards are duplicated. In cases where there are two identical cards, a defective circuit can often be identified by substitution. As an example, if the Channel A Zone Generator is suspected, exchange the positions of the Channel A and Channel B Zone Generator Circuit cards. If the Channel B is now inoperative, the malfunction is in the original Channel A Zone Generator card.

Waveform Checks. Waveform checks should be made with a test oscilloscope having at least a 40 MHz capability. Significant waveforms are shown on the circuit diagram foldouts and on the diagrams in the Circuit Logic Description section.

Table 5-2 shows how each circuit is directly related to other circuits. To use this table, find the circuit(s) affected in the row across the top of the table. Check that the proper output logic levels (or pulses) are present from the circuit indicated in the left column. After the trouble has been isolated to a particular circuit, a visual inspection may reveal the source of trouble. Check the circuit for poor connections, damaged components, broken wires, etc.

The Buffer Circuit Card is probably the best place to start a waveform check if the trouble cannot be isolated by the use of Table 5-2. If the input and output waveforms on the Buffer Circuit Card all appear to be correct, the next card to check is the Synchronizer. Since some of the circuits on the Synchronizer Circuit Card form loops with circuits on other cards, trouble on the Synchronizer Circuit Card may cause some of the input waveforms to be incorrect. Trouble on the Synchronizer Circuit Card can be isolated by taking waveforms in the following manner:

1. Turn the TRIGGERED MEASUREMENT switch off. Turn the DISPLAY TIME control fully counterclockwise. Place the Synchronizer Circuit Card in the extender card and connect the test oscilloscope to integrated circuit M1770 pin 3. If the DELAY pulse is absent, pull out the Memory Circuit Cards. If the pulse is still absent, remove transistor Q1785 from its socket. The delay generator should now free-run. Should the delay generator start to free-run when the Memory Circuit Cards are removed, check the DISCHARGE pulse on J9 pin D. If the DISCHARGE pulse appears normal, the trouble is probably on the Memory Circuit Cards.

2. If the delay generator starts to free-run when Q1785 is removed from its socket, check Q1785. If the transistor is good, leave the delay generator free-running and trace the END pulse (this is a narrow pulse; see the Synchronizer Circuit Card description) through transistor Q1741 and the integrated circuits M1746 and M1748A. If the END pulse is absent at J9 pin 4, check the input and output waveforms on the Clock Circuit Card. Make sure the MEASUREMENT AVERAGING switch is in the "1" position when tracing END through M1746 and M1748A.

3. Check both inputs to integrated circuit M1720 (pins 2 and 6). Check both outputs of integrated circuit M1722. If everything appears normal at this point, check the inputs and outputs of integrated circuit M1770. When the proper output has been obtained from M1770, replace Q1785 in its socket. The delay generator should operate normally. Re-install the Memory Circuit Cards; if the delay generator now locks up, check back through the Memory Circuit Cards and Buffer Circuit Card.

Semiconductor Tests

Most circuit failures result from the failure of a transistor, diode, or integrated circuit due to normal aging and use. The following paragraphs detail various methods of checking semiconductor devices.

Transistor Checks. Transistor defects usually take the form of the transistor opening, shorting, or developing excessive leakage. The best method of checking transistors is by direct substitution. Be sure the voltage conditions of the circuit are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic tester (such as a Tektronix Type 575).

Static-type testers are not recommended since they do not check the device under operating conditions. However, if no other tester is immediately available, an ohmmeter will usually detect catastrophic failures in a transistor. As a general rule, use the R × 1 k range where the current is usually limited to less than 2 mA and the internal voltage is usually 1½ volts. Check the current and voltage of the ohmmeter by inserting a multimeter between the ohmmeter leads and measureing the current and voltage of the various ranges. When it has been determined which ohmmeter ranges will not harm the transistor, then use those ranges to measure the transistor's resistance. Check the resistance in both directions through the junctions as listed in Table 5-2.

TABLE 5-3
Transistor Resistance Checks

Ohmmeter Connections[2]	Resistance Readings That Can Be Expected Using the R × 1 k Range
Emitter-Collector	High readings both ways (about 60 kΩ to around 500 kΩ).
Emitter-Base	High reading one way (about 200 kΩ or more). Low reading the other way (about 400 Ω to 2.5 kΩ).
Base-Collector	High reading one way (about 500 kΩ or more). Low reading the other way (about 400 Ω to 2.5 kΩ).

[2]**Test prods from the ohmmeter are first connected one way to the transistor leads and then the test prods are reversed (connected the other way). Thus, the effects of the polarity reversal of the voltage applied from the ohmmeter to the transistor can be observed.**

Integrated Circuit Checks. Integrated circuits are best checked by direct substitution. Where a replacement is not available, use any of the test methods listed for transistors that can be safely used for integrated circuits.

Diode Checks. Diodes (except for tunnel diodes) can easily be checked for an open or shorted condition by measuring the resistance between the terminals after unsoldering one end of the component. Use a resistance scale with an internal voltage between 800 mV and 3 volts. The resistance should measure very high (in megohm range) in one direction and low in the other.

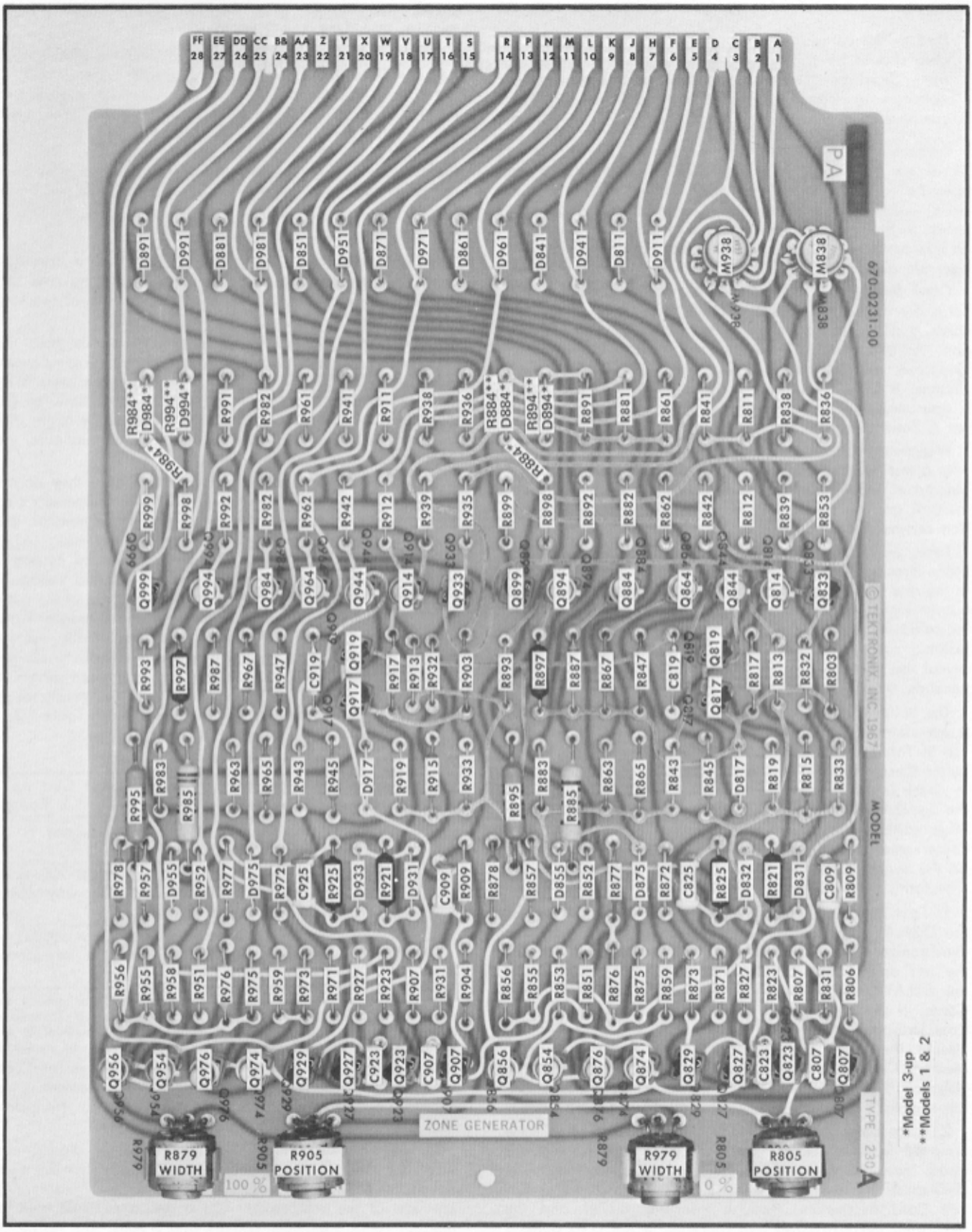


Fig. 5-8. Component locations on the Ch A or Ch B Zone Generator card.

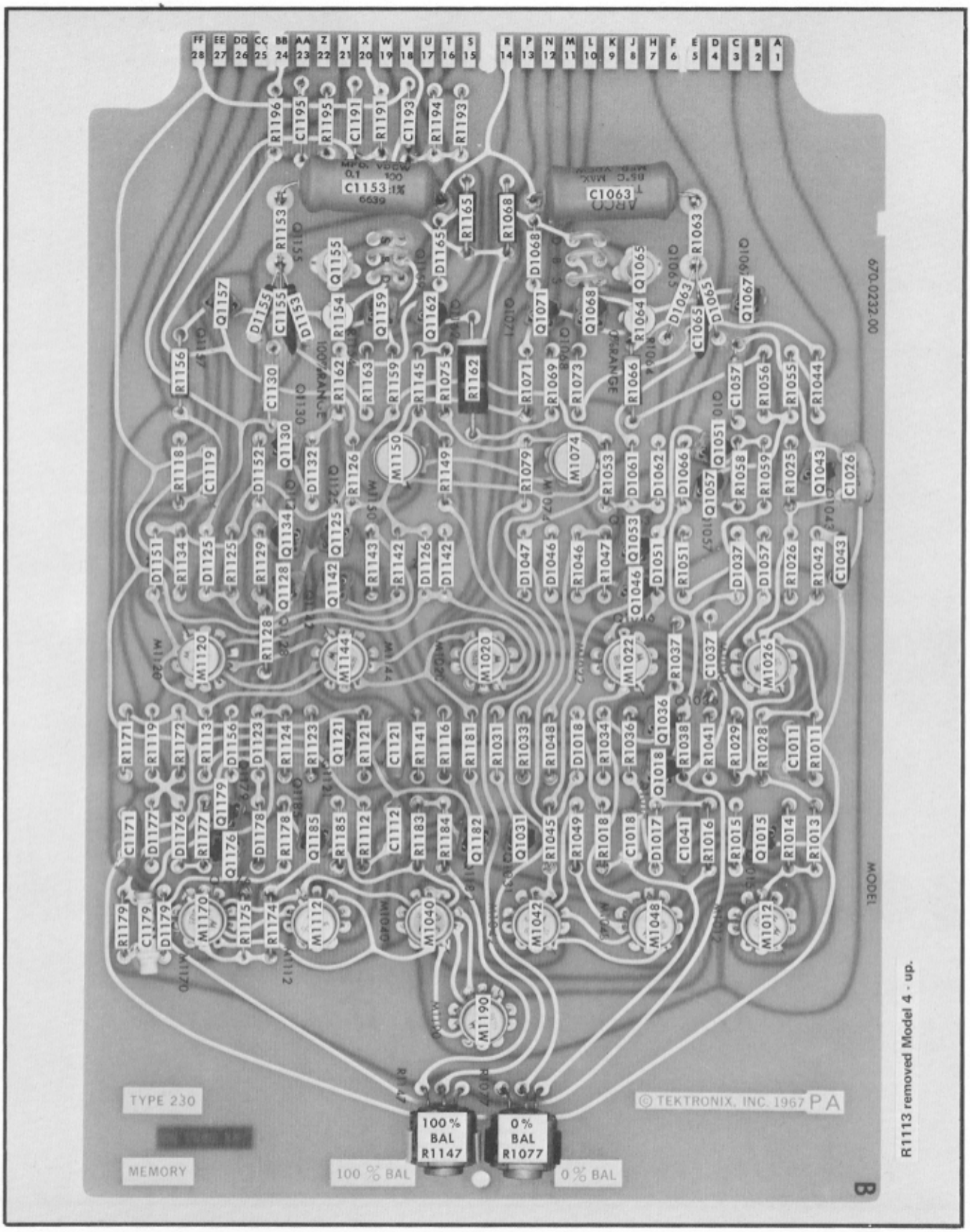


Fig. 5-9. Component locations on the Ch A or Ch B Memory card.

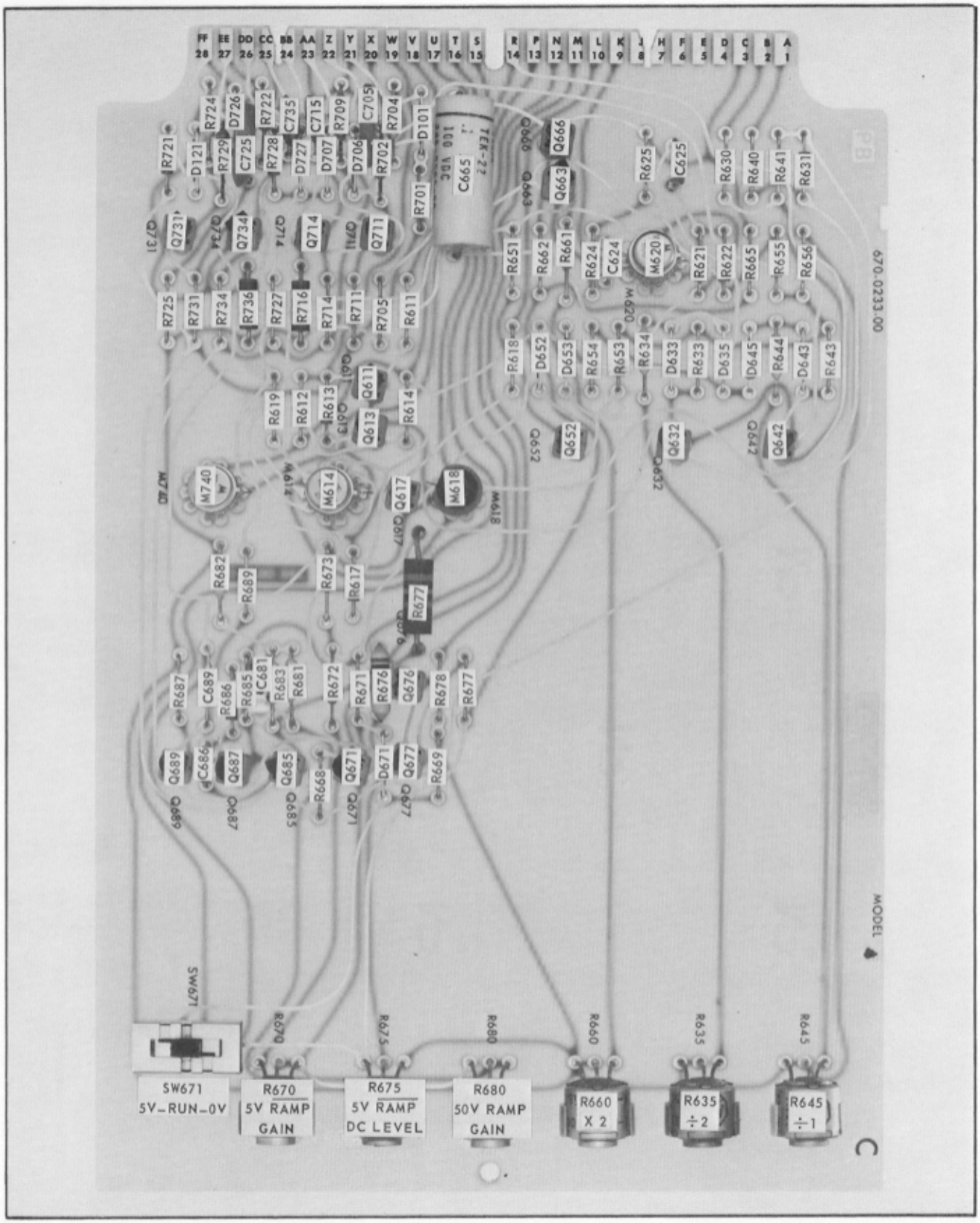


Fig. 5-10. Component locations on the Buffer card (Model 4-up).

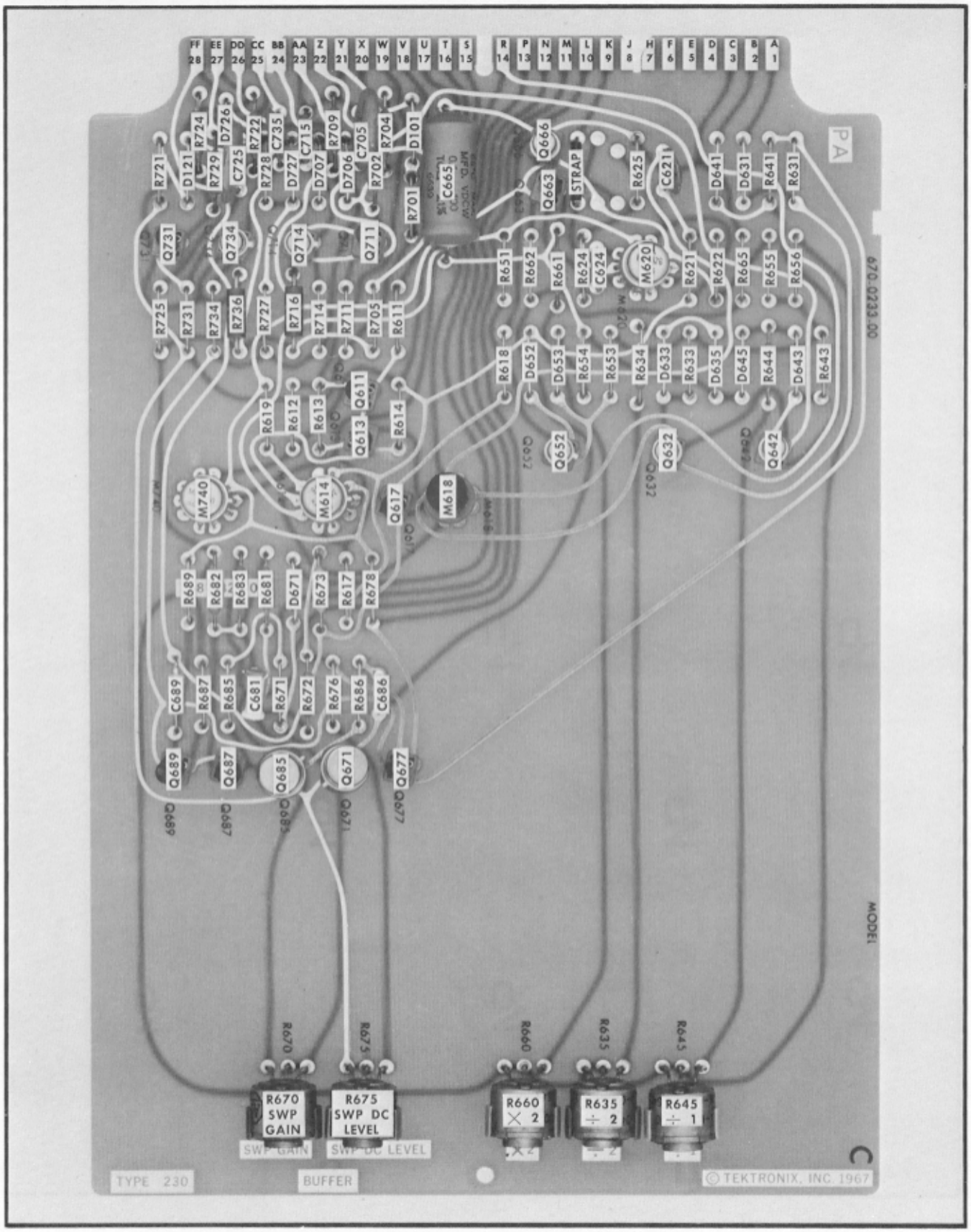


Fig. 5-11. Component locations on the Buffer card (Models 1-3).

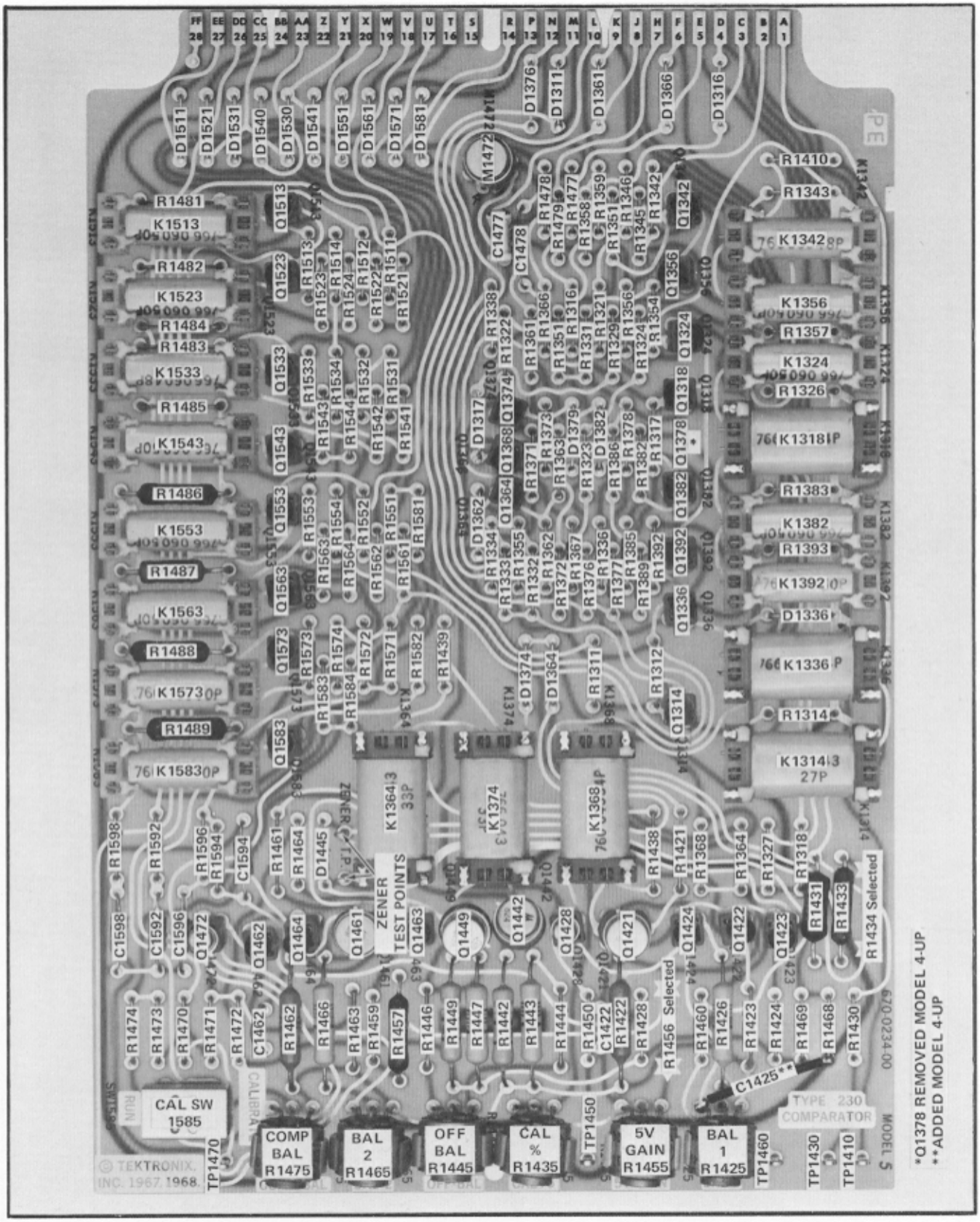


Fig. 5-12. Component locations on the Start or Stop Comparator card.

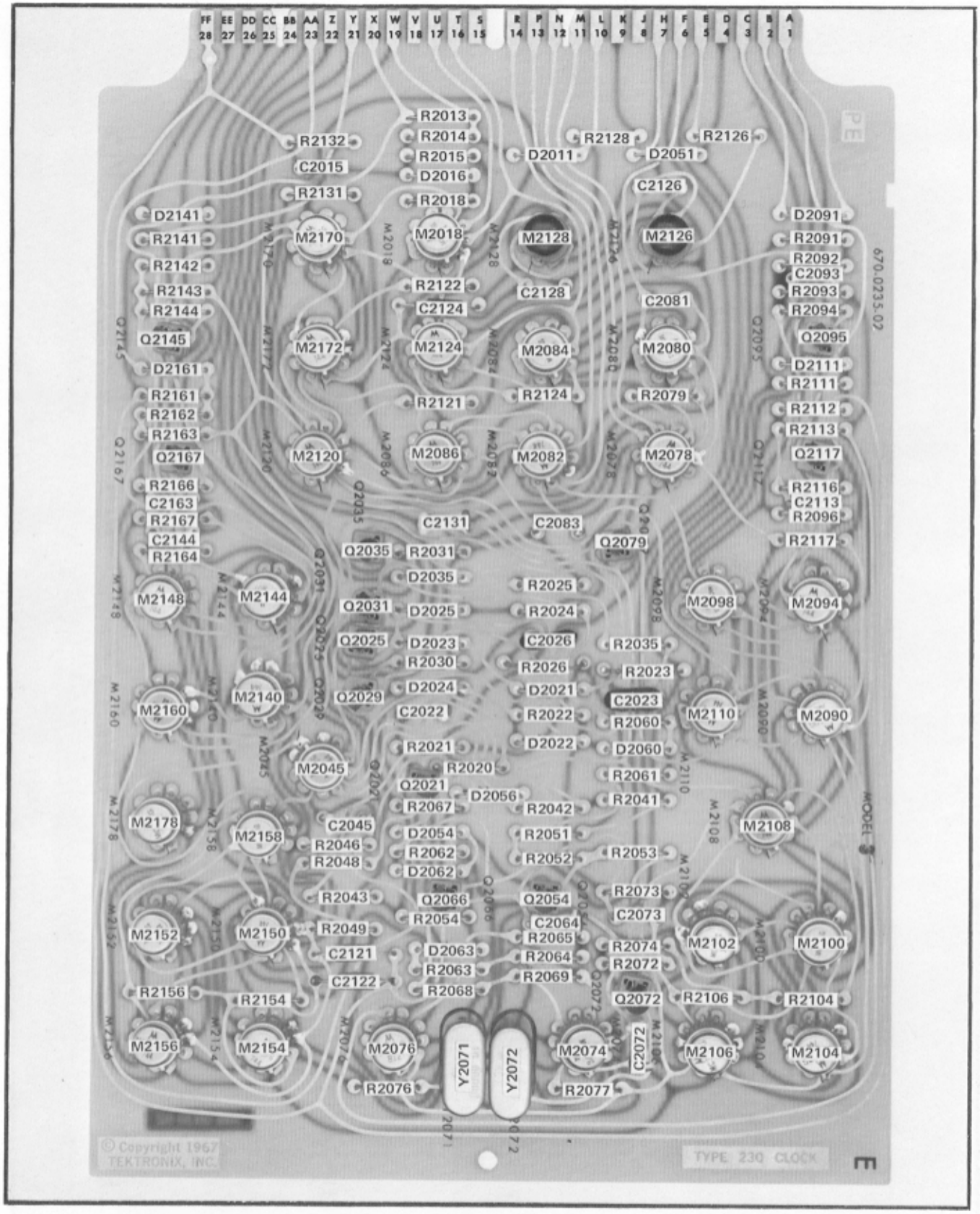


Fig. 5-13. Component locations on the Clock Card (Model 3-up).

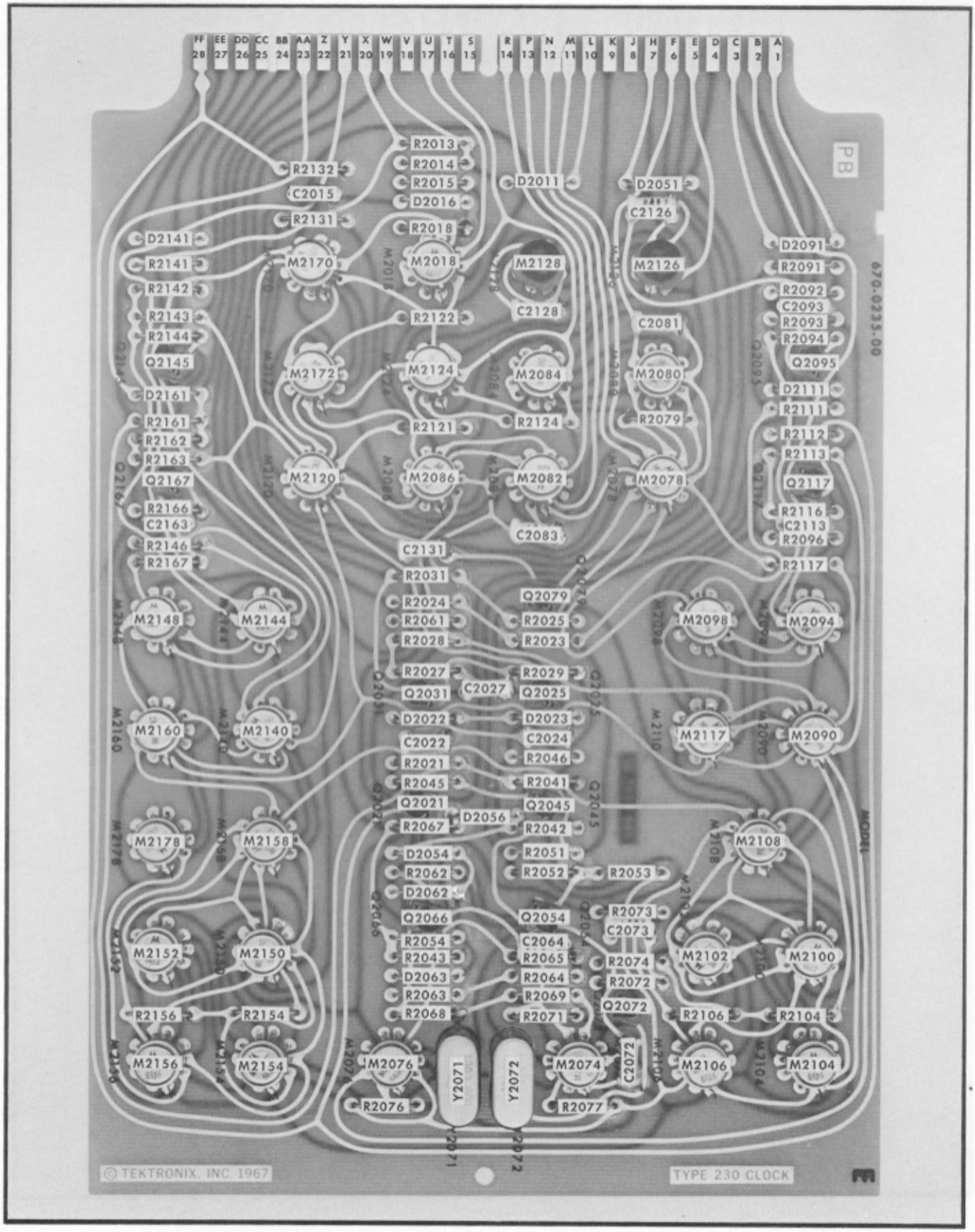


Fig. 5-14. Component locations on the Clock Card (Model 1 and 2).

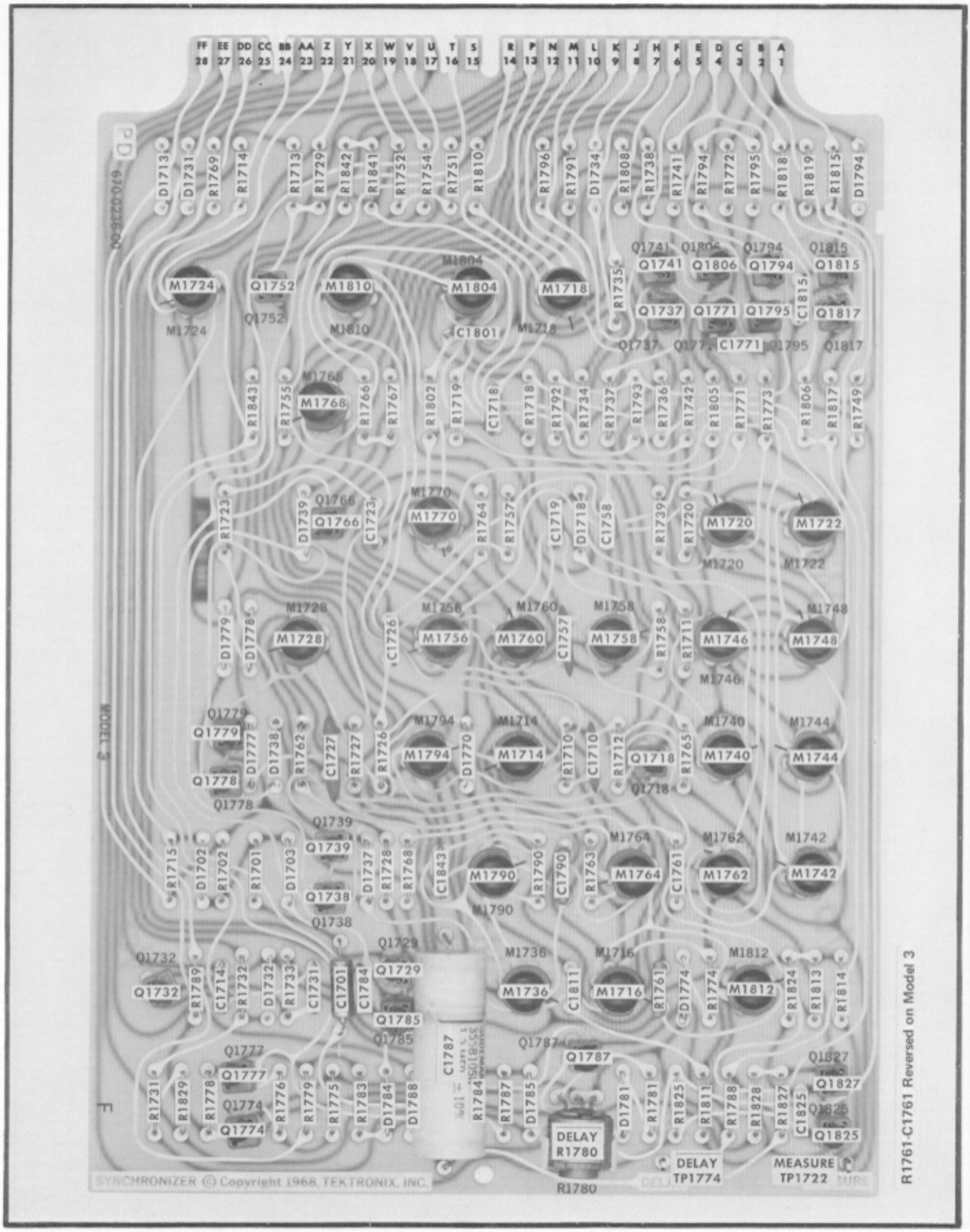


Fig. 5-15. Component locations on the Synchronizer card (Model 3-up).

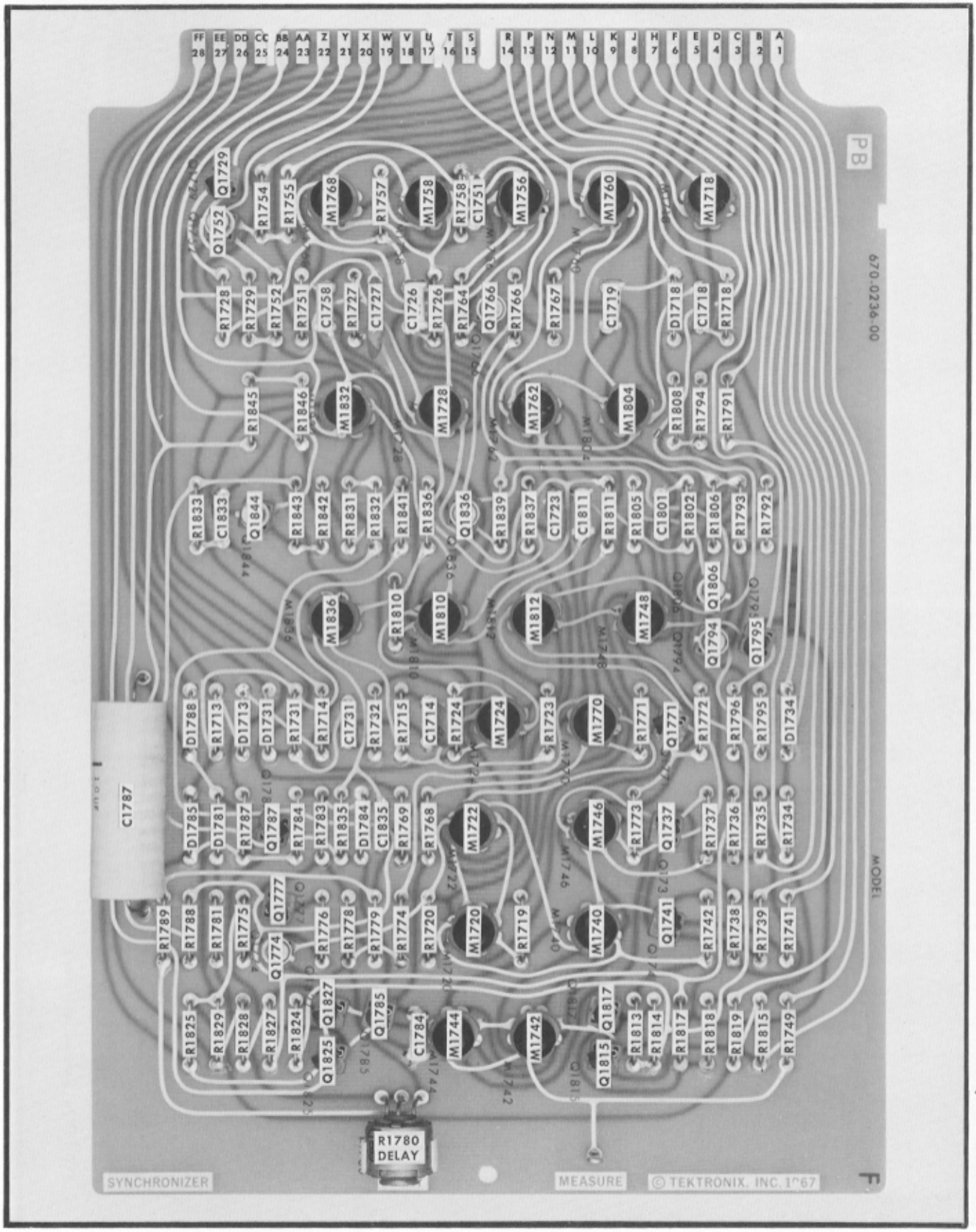


Fig. 5-16. Component locations on the Synchronizer card (Model 1 and 2).

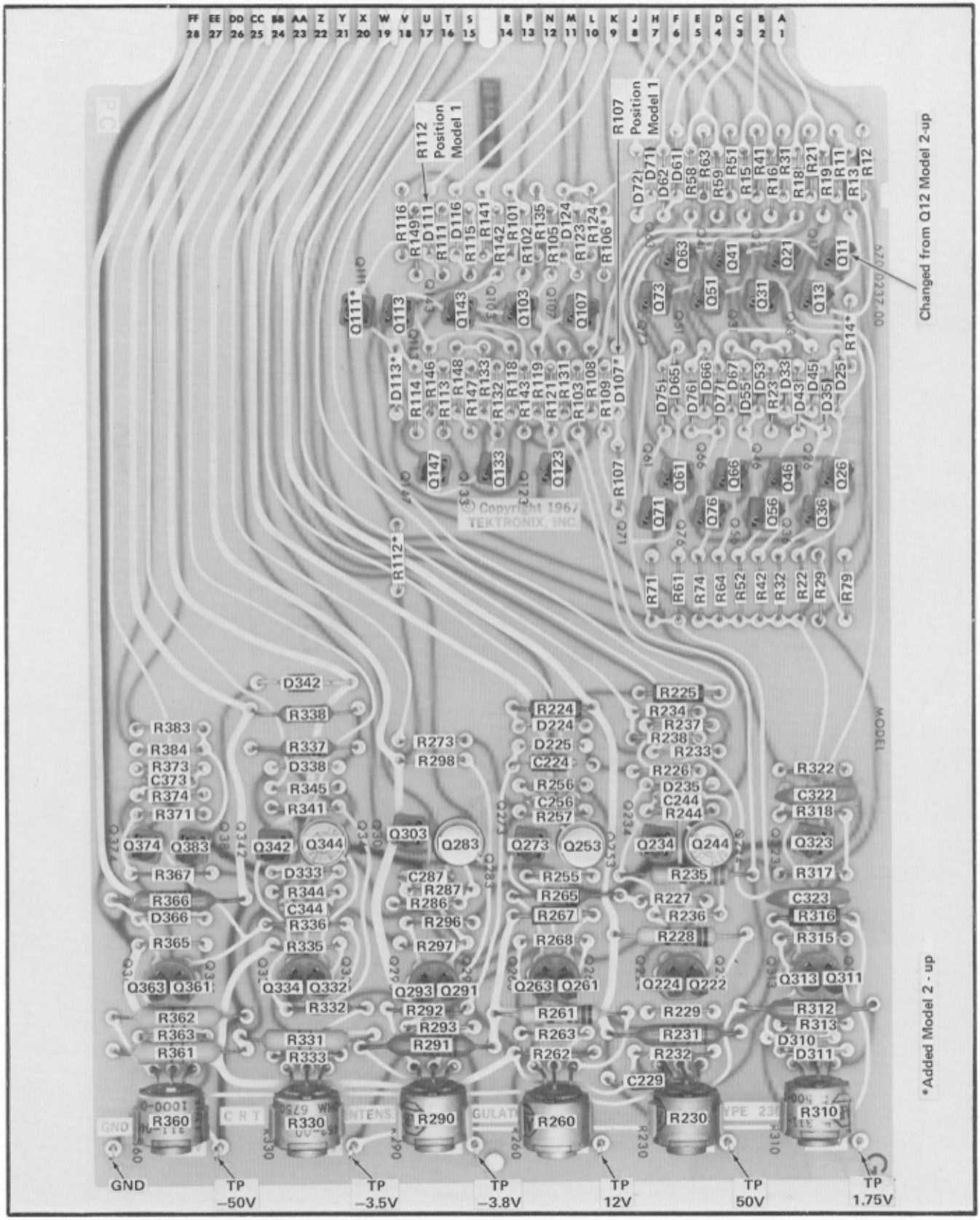


Fig. 5-17. Component locations on the CRT INTEN/Regulator card.

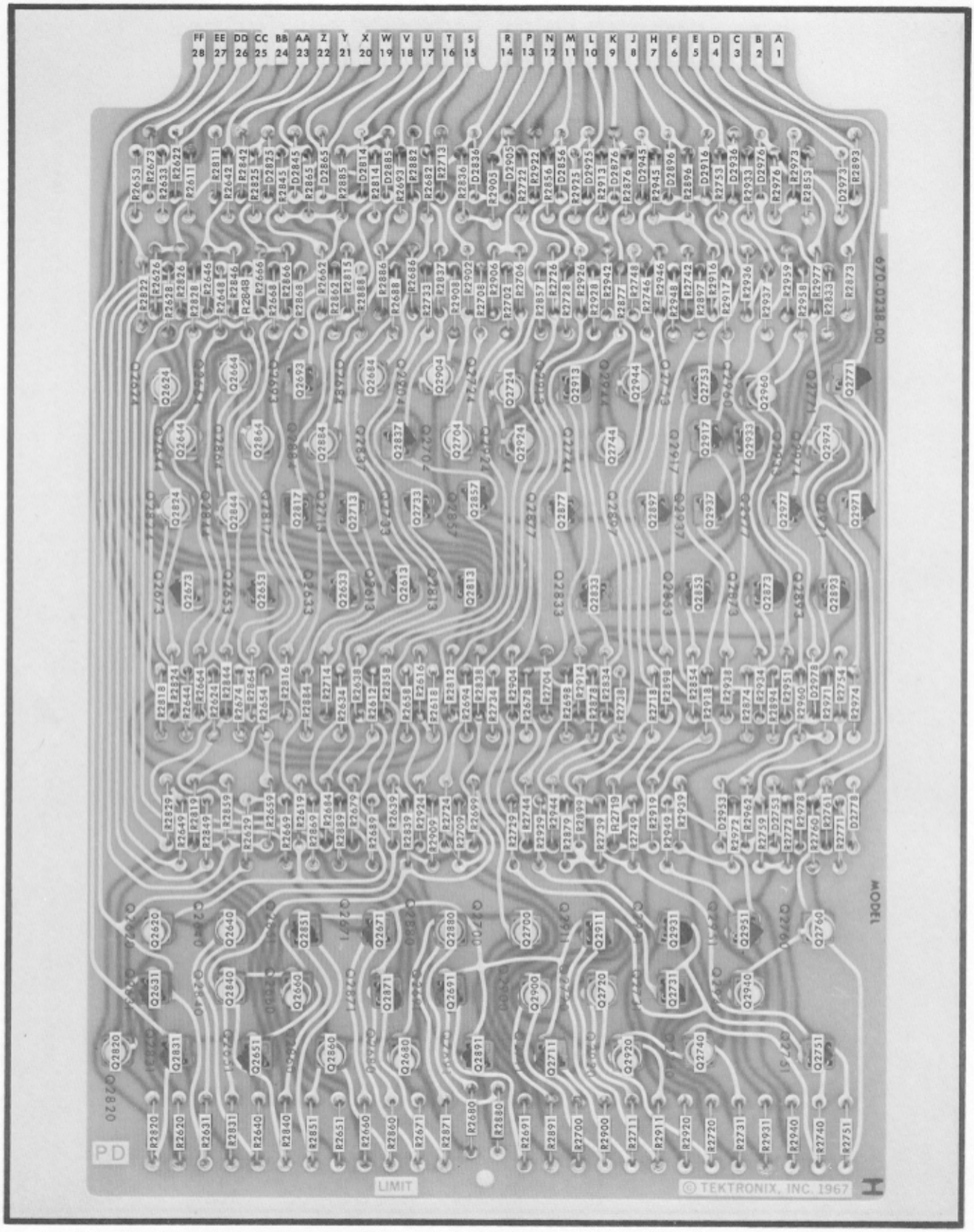


Fig. 5-18. Component locations on the Limit card (Model 1).

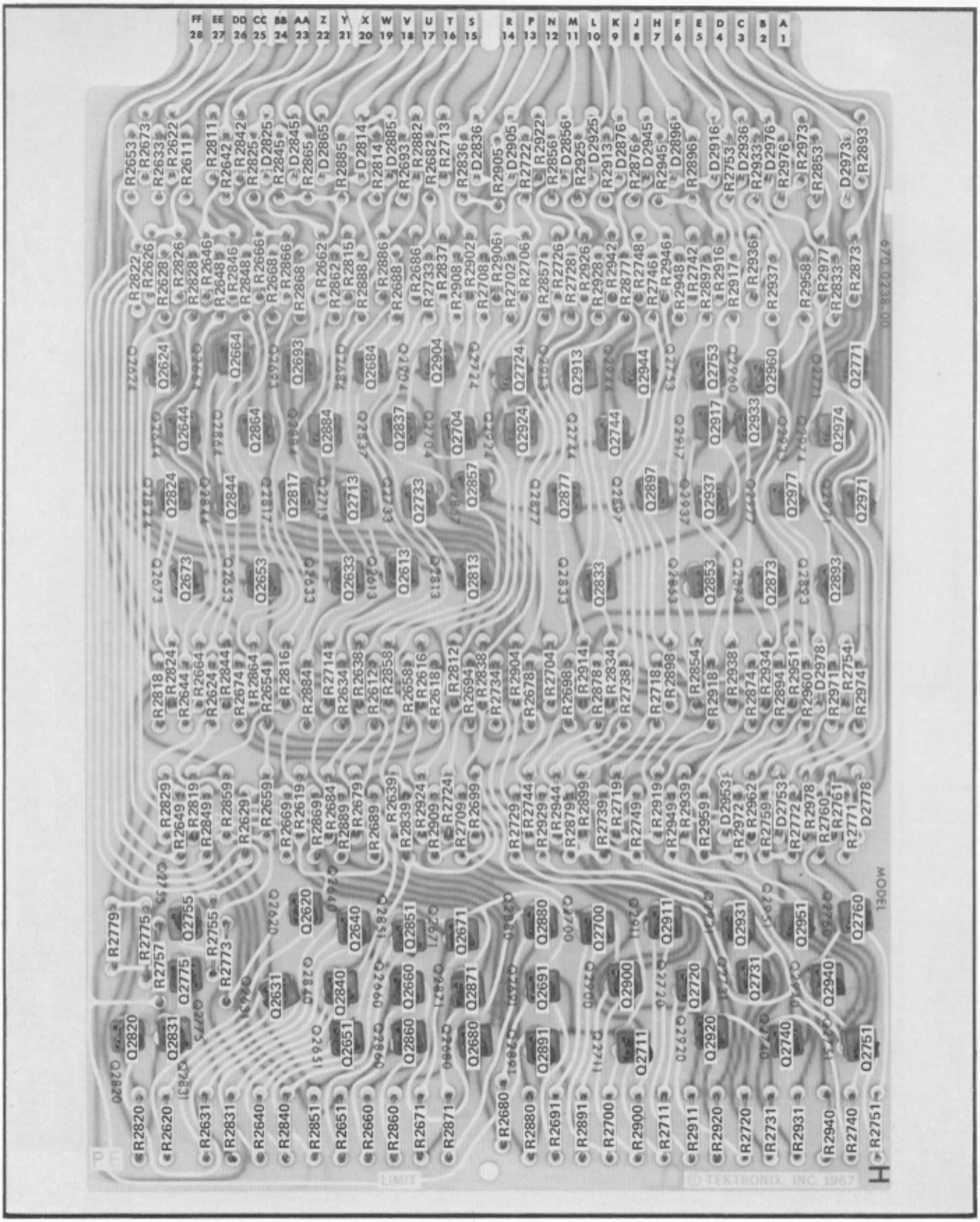


Fig. 5-19. Component locations on the Limit card (Model 2-up).

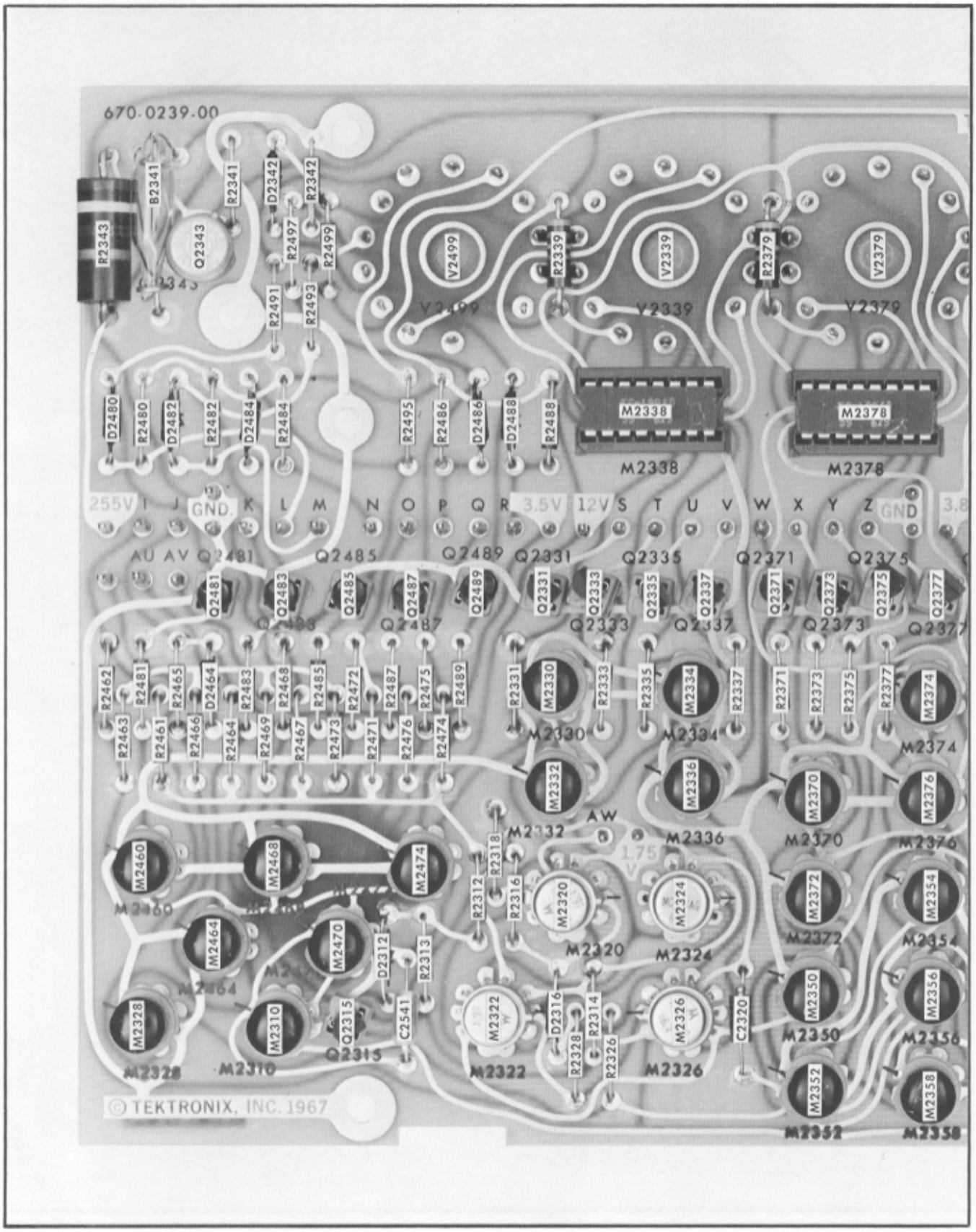


Fig. 5-20. (A and B) Pin connection locations on the Counter circuit board.

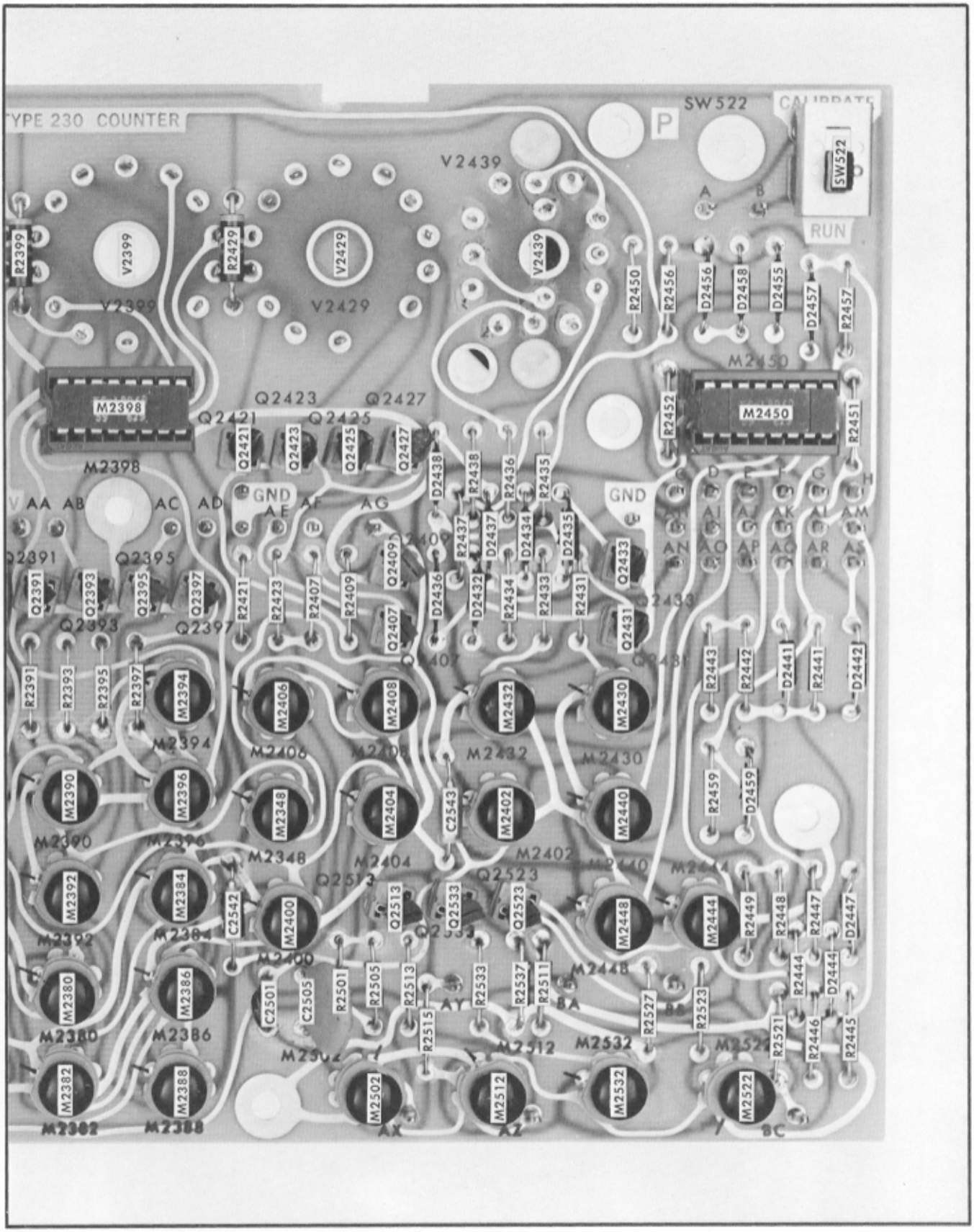

TYPE 230 COUNTER
SW522
CALIBRATE
RUN
P
V2439
V2399
V2429
M2398
M2450
Q2423
Q2427
Q2421
Q2425
GND
M2394
M2406
M2408
M2432
M2430
M2390
M2396
M2348
M2404
M2402
M2440
M2392
M2384
M2400
M2444
M2380
M2386
M2448
M2382
M2388
M2502
M2512
M2532
M2522
Q2513
Q2523
Q2533
AX
AY
AZ
BA
BC

Fig. 5-20B.

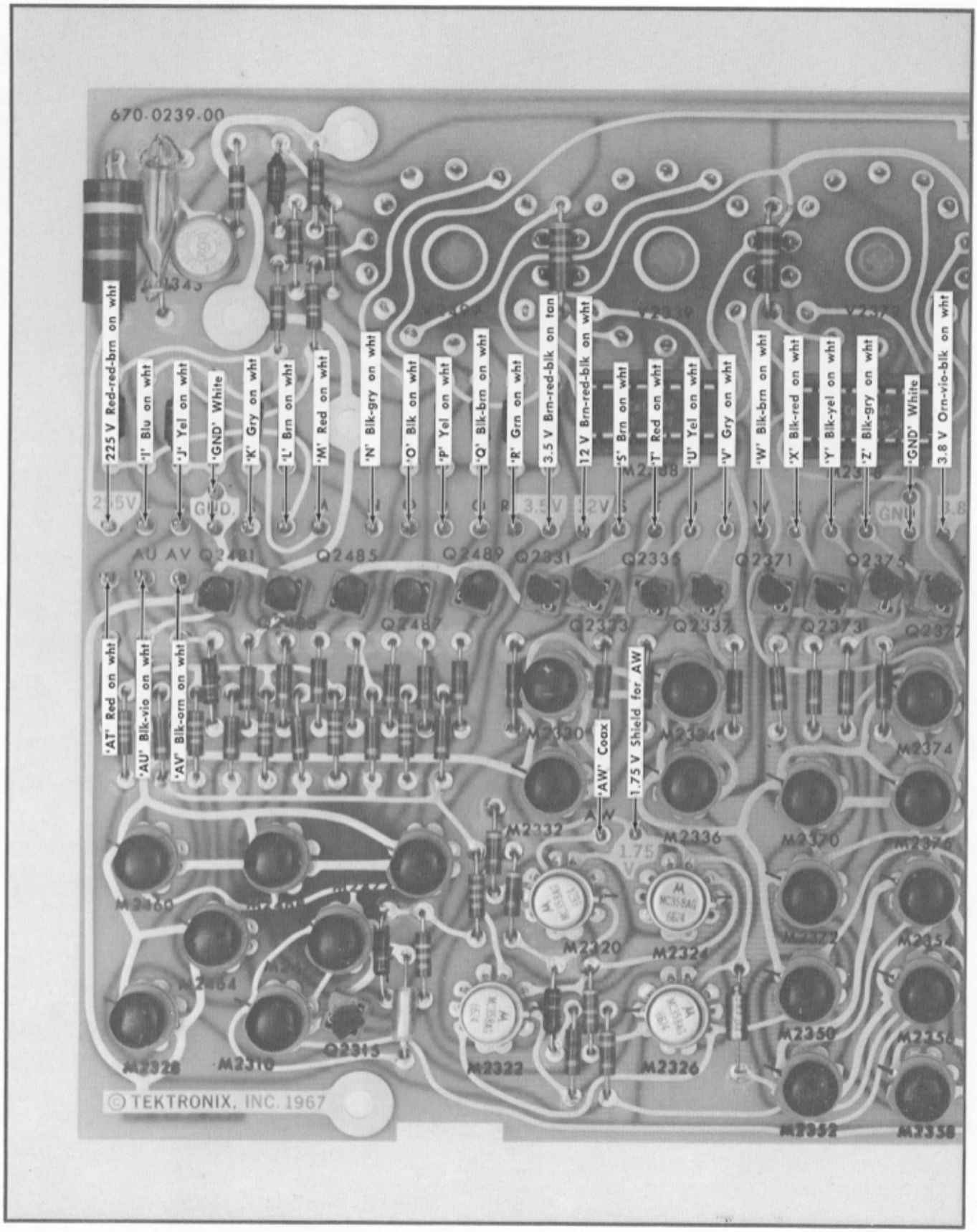


Fig. 5-21. (A and B) Pin connection locations on the Counter circuit card board.

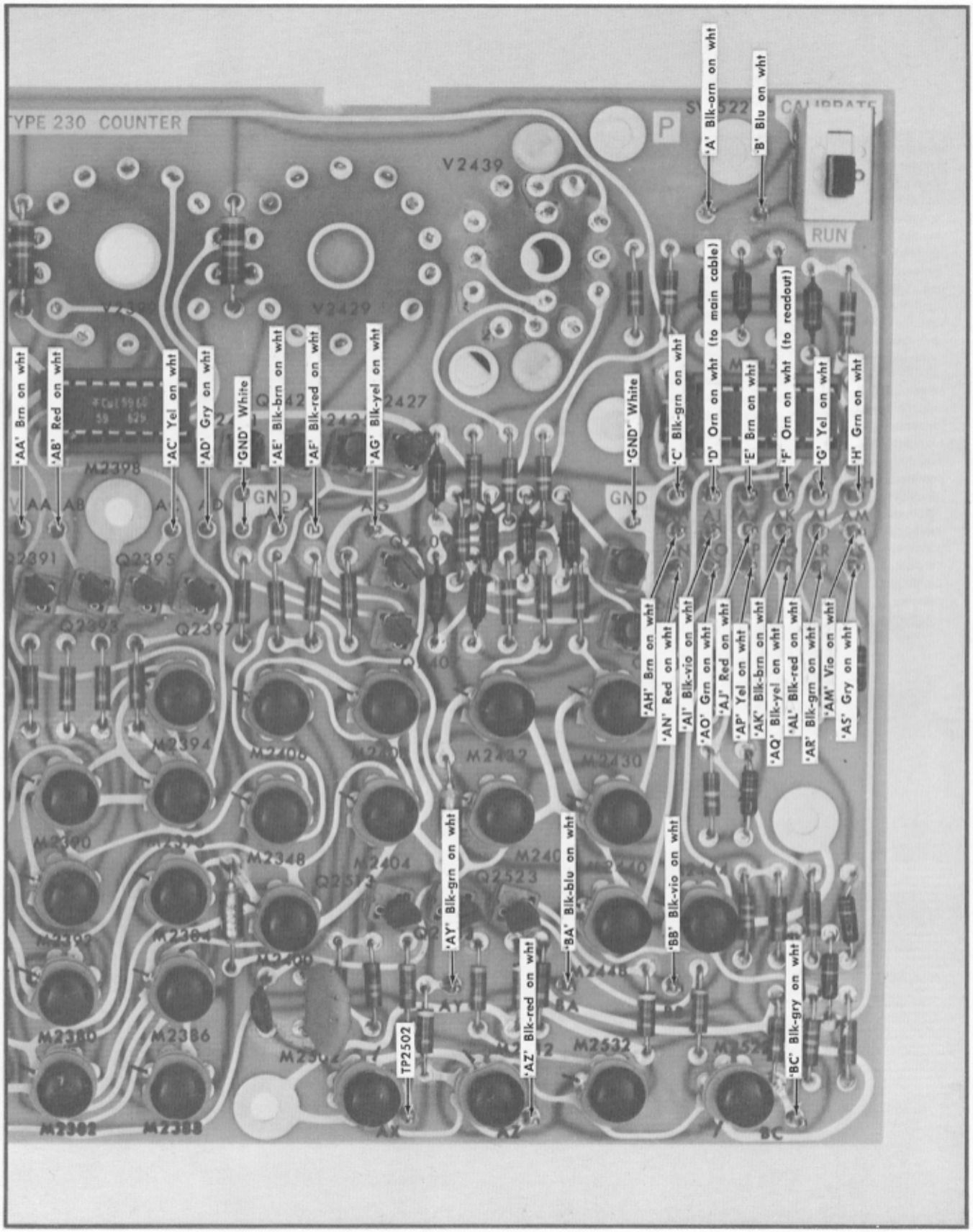

TYPE 230 COUNTER
V2439
V2429
'A' Blk-orn on wht
'B' Blu on wht
RUN
'AA' Brn on wht
'AB' Red on wht
'AC' Yel on wht
'AD' Gry on wht
'GND' White
'AE' Blk-brn on wht
'AF' Blk-red on wht
'AG' Blk-yel on wht
'GND' White
'C' Blk-grn on wht
'D' Orn on wht (to main cable)
'E' Brn on wht
'F' Orn on wht (to readout)
'G' Yel on wht
'H' Grn on wht
'AH' Brn on wht
'AN' Red on wht
'AI' Blk-vio on wht
'AO' Grn on wht
'AJ' Red on wht
'AP' Yel on wht
'AK' Blk-brn on wht
'AQ' Blk-yel on wht
'AL' Blk-red on wht
'AR' Blk-grn on wht
'AM' Vio on wht
'AS' Gry on wht
'AY' Blk-grn on wht
'BA' Blk-blu on wht
'BB' Blk-vio on wht
'AZ' Blk-red on wht
'BC' Blk-gry on wht
TP2502
M2398
M2394
M2348
M2380
M2386
M2382
M2388
M2432
M2430
M2448
M2532
M2522
Q2391
Q2395
Q2393
Q2397
Q2523
GND

Fig. 5-21B.

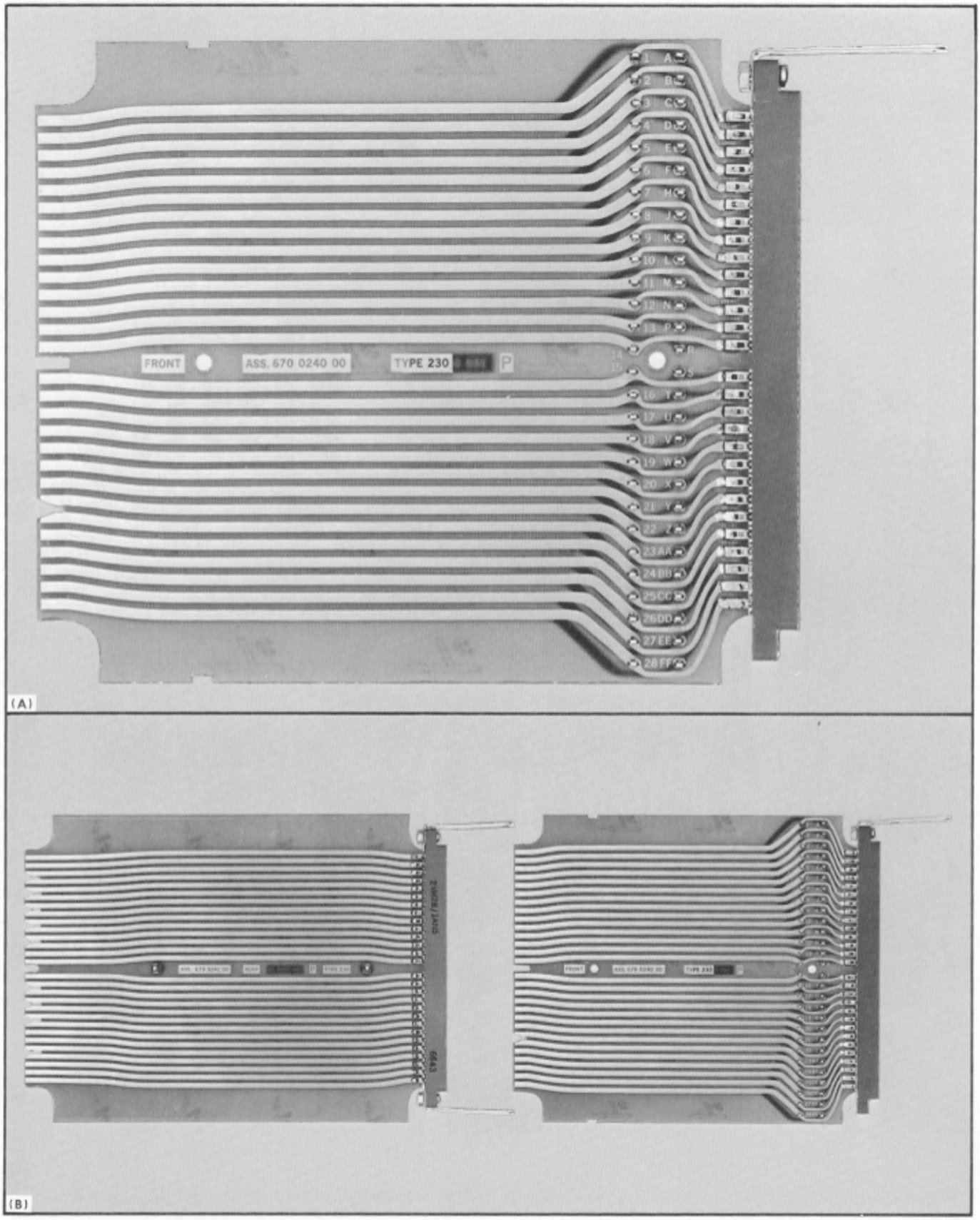


Fig. 5-22. (A) Test points location on the front extender card, (B) Proper alignment of extender cards to provide to test points and component parts for each individual circuit cards.

SECTION 6

PERFORMANCE CHECK

General Information

This section of the manual provides a procedure for rapidly checking the performance of the Type 230. The procedure is intended to check the operation of the instrument to the requirements given in the Characteristics section without performing a complete calibration procedure and without adjusting any internal controls.

Performance of the Type 230 should be checked after each 1000 hours of operation at least once every 6 months to assure that it is operating properly and accurately. Failure to meet the performance requirements given in this procedure indicates the need for internal adjustments and checks as given in the Calibration section.

EQUIPMENT REQUIRED

The following (or equivalent) items of equipment are required for a complete performance check of the Type 230. Equipment requirements given here are the minimum requirements for proper calibration of the Type 230. All items are assumed to be calibrated and operating within their rated specifications. If substitute equipment is used, it must equal or exceed the given requirements in order to check the Type 230 to the given accuracy.

1. Oscillocope to provide measurement information to the Type 230. Tektronix Type 568 with sampling plug-in units, such as the Type 3S3 vertical unit and Type 3T4 Time base unit recommended.

2. 36-pin interconnecting cable, Tektronix Part No. 012-0119-00.

3. (Optional) Real Time vertical and Time base plug-in units to be used with the Type 568 if real time measurements are normally made with the Type 230. Tektronix Type 3A2 vertical unit and Type 3B2 Time-base unit recommended.

PERFORMANCE CHECK PROCEDURE

Equipment used in the following procedure is that listed under Equipment Required. If substitute equipment is used, connections and control settings may need to be changed to correspond to the characteristics of the equipment used.

Preliminary Procedure

1. Connect the 36-pin interconnecting cable (012-0119-00) between J101 of the Type 568 and J101 of the Type 230.

2. Insert the sampling vertical and horizontal plug-in units into the Type 568.

3. Check that the voltage selector and range selector switch bars in the LINE VOLTAGE SELECTOR assembly on the rear of the Type 230 are set to correspond to the proper applied line voltage.

4. Connect the Type 230, Type 568 and other test equipment to a suitable power source and turn on all of the equipment.

5. Set the front panel controls of the Type 230, Type 568 and other test equipment as follows:

Control Settings

Type 230

TRIGGERED MEASUREMENT	OFF
DISPLAY TIME	centered
MEASUREMENT MODE	TIME
CRT INTENSIFICATION	
TIME MEASUREMENT	ON
REF ZONES	OFF
MEASUREMENT AVERAGING	1
CHANNEL A REF ZONES	
0% POSITION	White dot at top center
100% POSITION	White dot at top center
0% LEVEL-WIDTH	.3 CM
100% LEVEL-WIDTH	.3 CM
CHANNEL B REF ZONES	
0% POSITION	White dot at top center
100% POSITION	White dot at top center
0% LEVEL-WIDTH	.3 CM
100% LEVEL-WIDTH	.3 CM
TIME MEASUREMENT START POINT	
CHANNEL	A
LEVEL	HORIZ mm FROM SWP START
Offset dials	1 and 0
SLOPE	+, 1st
LIMITS	As desired

Type 568

Intensity	Normal Brightness
Astig	As is
Focus	Adjust for a well focused trace
Scale Illum	As desired
Calibrator	Off
CRT Cathode Selector	Ext CRT Cathode

Vertical Sampling Unit

Input Signal	None
Mode	Channel A
mV/Div (Ch A)	100
Variable	Calib
Norm-Inv (Ch A and B)	Norm
Position	Centered
DC Offset	Full ccw
Smoothing (Ch A and B)	Full ccw
Low Noise-Fast Risetime	Fast RT

Time Base Sampling Unit

Time/Div	.1 μs
Variable	Calibration
Triggering	+, Int
Trigger Level	Free running trace
Delay	1.0
Position	Centered
Sweep Mode	Normal
Samples/Sweep	1000 (X1)
Manual Scan or Ext Atten	Centered
Recovery Time	Centered

Control Settings for Optional Real-Time plug-in units

Vertical Unit

Input signal	none
Mode	A
Volts/Div	2
Input Coupling	AC
Position	Centered

Time-Base Unit

Sweep Rate	1 ms
Resolution	10 μs
Triggering	AC, +, Int
Trigger level	Free Run
Position	Centered

1a. Check Buffer Sweep Gain Using Sampling Plug-in Units

a. Check—Type 230 readout of 0.800 μS, ±0.001 μs.

b. Change the Type 568 time base unit Time/Div switch to 50 ns.

c. Check—Type 230 readout of 0.400 μS, ±0.001 μs.

d. Change the Type 568 time base unit Time/Div switch to .2 μs.

e. Check—Type 230 readout of 1.600 μS, ±0.002 μs.

f. Return the Type 568 time base unit Time/Div switch to .1 μs.

1b. Check Buffer Sweep Gain Using Real Time Plug-in Units

a. Check—Type 230 readout of 08.00 MS, ±00.01 mS.

b. Change the Type 568 time base unit Time/Div switch to .5 mS.

c. Check—Type 230 readout of 04.00 mS, ±00.01 ms (±3% of sweep calibration).

d. Change the Type 568 time base unit Time/Div switch to 2 ms.

e. Check—Type 230 readout of 16.00 MS, ±00.10 ms.

f. Return the Type 568 time base Time/Div switch to 1 ms.

2. Check Buffer Sweep DC Level

a. Change the Type 230 controls as follows:

CRT INTENSIFICATION

TIME MEASUREMENT	OFF

TIME MEASUREMENT START POINT

Offset dials	0 and 1

b. Check that the trace starts at the extreme left vertical graticule line on the Type 568.

c. Set the Type 230 CRT INTENSIFICATION-TIME MEASUREMENT switch to ON.

d. Check—The Type 568 CRT display; intensified zone should start at the extreme left vertical graticule line (start of sweep), and is erratic with TIME MEASUREMENT START POINT Offset Dials at 0 and 0.

e. Set the Type 230 TIME MEASUREMENT START POINT—Offset dials to 1 and 0.

f. Check—Type 568 CRT display; intensified zone should be 8.0 cm long, ±0.5 minor div.

3a. Check Buffer Voltmeter $\overline{\text{Ramps}}$ Using Sampling Plug-in Units

a. Change the following front panel controls:

Type 230

TIME MEASUREMENT START POINT

LEVEL	mm ABOVE 0% ZONE
Offset dials	0 and 0

TIME MEASUREMENT STOP POINT

LEVEL	mm ABOVE 0% ZONE
Offset dials	8 and 0

b. Set the Type 230 Run/Calibrate switch to Calibrate (located on counter circuit board; Fig. 6-1).

c. Position the trace on the Type 568 at the bottom horizontal graticule line.

d. Check—Type 230 readout of 0800. MV, ±0001 mV.

e. Set the Type 568 vertical unit mV/Div switch to 50.

f. Position the trace at the bottom horizontal graticule line.

g. Check—Type 230 readout of 0400. MV, ±0001 mV.

h. Set the Type 568 vertical unit mV/Div switch to 20.

i. Position the trace at the bottom horizontal graticule line.

j. Check—Type 230 readout of 160.0 MV, ±000.2 mV.

k. Return the Type 568 vertical mV/Div switch to 100.

3b. Check Buffer Voltmeter Ramps Using Real Time Plug-in Units

a. Change the following front panel controls:

Type 230

TIME MEASUREMENT START POINT

LEVEL	mm ABOVE 0% ZONE
Offset dials	0 and 0

TIME MEASUREMENT STOP POINT

LEVEL	mm ABOVE 0% ZONE
Offset dials	8 and 0

b. Set the Type 230 Run/Calibrate switch to Calibrate. (located on Counter Circuit board, Fig. 6-1).

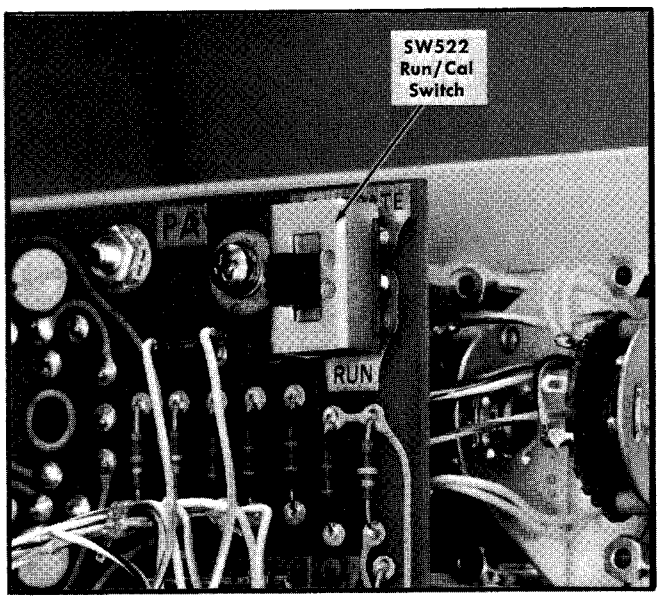


Fig. 6-1. Location of Run/Calibrate switch on the Counter circuit board.

c. Position the trace on the Type 568 at the bottom graticule line.

d. Check—Type 230 readout of 16.00 V, ±00.01 V.

e. Set the Type 568 Vertical Unit Volts/Div switch to 1.

f. Check—Type 230 readout of 08.00 V, ±00.01 V.

g. Set the Type 568 Vertical Unit Volts//Div switch to .5.

h. Check—Type 230 Readout of 04.00 V, ±00.01 V.

i. Return the Type 568 Vertical Volts/Div switch to .2.

j. Change the Run/Calibrate switch on the Counter circuit card to Run.

4. Check Channel A Zone Generator 0% Zone Position and 100% Zone Position

a. Change the following front panel controls:

CRT INTENSIFICATION

TIME MEASUREMENT	OFF
REF ZONES	0%

b. Check that the Type 568 trace starts at the extreme left vertical graticule line.

c. Position the start of the 0% zone at the 5th cm vertical graticule line with the 0% ZONE POSITION control. (Fig. 6-2).

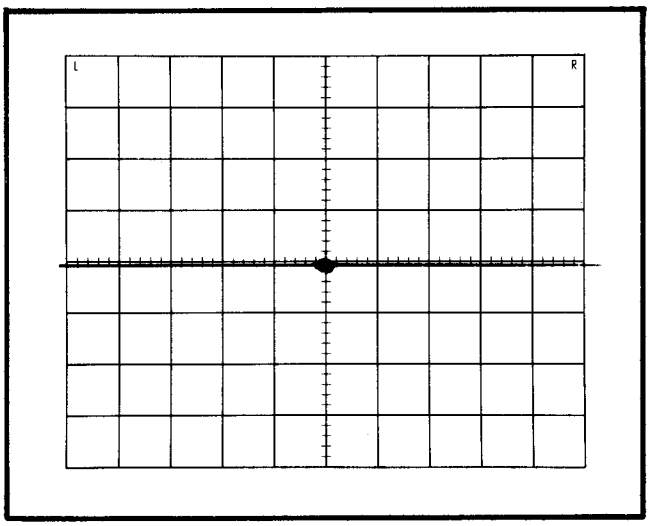


Fig. 6-2. Definition of vertical graticule lines.

d. Check—Type 568 CRT display intensified zone should start at the 5th cm vertical graticule line.

e. While observing the Type 568 CRT display, turn the 0% ZONE POSITION control throughout its range.

f. Check—Type 568 CRT display; start of intensified zone should move across the CRT in 0.5 cm steps.

g. Position the intensified zone at the 9th cm vertical graticule line.

h. Check—Start of intensified zone within 1 minor div of the 9th cm vertical graticule line.

i. Position the intensified zone at the start of sweep.

j. Check—Start of 0% Zone within 1 minor div of sweep start.

k. Set the CRT INTENSIFICATION—REF ZONE switch to 100%.

l. Position the start of the 100% zone at the 5th cm (center) vertical graticule line with the 100% ZONE POSITION control.

m. Check—Type 568 CRT display, intensified zone should start at the center (5th cm) vertical graticule line.

n. While observing the Type 568 CRT display, turn the 100% ZONE POSITION control throughout its range.

o. Check—Type 568 CRT display; intensified zone should move across the CRT in 0.5 cm steps.

p. Position the intensified zone at the 9th cm vertical graticule line.

q. Check—Start of intensified zone within 1 minor div of the 9th cm vertical graticule line.

r. Position the intensified zone at the start of sweep.

s. Check—Type 568 CRT display; start of intensified zone within 1 minor div of start of sweep.

5. Check Channel B Zone Generator 0% Zone Position and 100% Zone Position

a. Set the Type 568 Vertical Mode switch to Channel B.

b. Set the CRT INTENSIFICATION-REF ZONE switch to 0%.

c. Repeat parts b through s of step 3 for checking of the Channel B 0% Zone position and 100% Zone position. All control settings of Type 230 are the same with the exception that all references should be made to Channel B.

6. Check Channel B Zone Generator 0% Zone Width and 100% Zone Width

a. Position the 100% intensified zone on the Type 568 trace to the center vertical graticule line.

b. Check that both Channel B LEVEL—WIDTH switches are set at 0.3 CM.

c. Check—Type 568 CRT display; width of intensified zone should be 0.3 cm (1.5 minor div).

d. Position the intensified zone on the Type 568 trace to the extreme left vertical graticule line.

e. Set the Channel B 100% LEVEL—WIDTH switch successively to 2 CM, 4 CM and 10 CM.

f. Check—For correct width of intensified zone within (±0.5 minor div) for each setting of the LEVEL—WIDTH switch. In the 10 CM position of the 0% and 100% Zone LEVEL—WIDTH switches, with the 0% Zone Position set at sweep start the entire length of the sweep is normally intensified (approx 10.5 cm).

g. Set the CRT INTENSIFICATION-REF ZONE switch to 0%.

h. Postion the intensified zone on the Type 568 display to the center vertical graticule line.

i. Check—Type 568 CRT display; width of intensified zone should be 0.3 cm (1.5 minor div).

j. Set the 0% LEVEL—WIDTH switch successively to 2 CM, 4 CM and 10 CM.

k. Check—Type 568 CRT display for correct width of the intensified zone within ±10% for each setting of the LEVEL-WIDTH switch.

7. Check Channel A Zone Generator 0% Zone Width and 100% Zone Width

a. Set the Type 568 Vertical Mode switch to Channel A.

b. Return the CRT INTENSIFICATION—REF ZONE Switch to 100%.

c. Repeat step 6 for checking of the Channel A 0% Zone Width and 100% Zone Width. All control settings of the Type 230 are the same, with the exception that all references should be made to Channel A.

8. Check Channel A Memory Tracking

a. Change the following Type 230 controls:

MEASUREMENT MODE	A VOLTS
CRT INTENSIFICATION REF ZONES	BOTH
CHANNEL A REF ZONES	
0% POSITION	Start of sweep
100% POSITION	Start of sweep
0% LEVEL—WIDTH	0.3 CM
100% LEVEL—WIDTH	0.3 CM
CHANNEL B REF ZONES	
0% POSITION	Start of sweep
100% POSITION	Start of sweep
0% LEVEL—WIDTH	0.3 CM
100% LEVEL—WIDTH	0.3 CM
TIME MEASUREMENT START POINT	
LEVEL	% BETWEEN ZONES
Offset dials	0 and 0
TIME MEASUREMENT STOP POINT	
LEVEL	% BEWEEN ZONES
Offset dials	0 and 0

b. Set the trace on the Type 568 CRT at the center horizontal graticule line with the Channel A Vertical Position control.

c. Check—Type 230 readout of 0000. MV, ±0001 mV.

d. Position the trace on the Type 568 CRT at the top horizontal graticule line.

e. Check—Type 230 readout of 0000. MV, ±0003 mV.

f. Postion the Trace on the Type 568 CRT at the bottom horizontal graticule line.

g. Check—Type 230 readout of 0000. MV, ±0003 mV.

h. Position the trace on the Type 568 at the center horizontal graticule line.

NOTE

If Real Time Plug-ins are used for this step, the numerical readouts will be the same, but the Units of Measure will read out in Volts.

9a. Check Channel A Memory Leak Down (Sampling Plug-in Units)

a. Set the Sampling Time Base Unit Time/Div switch to the 50 nSEC position. Free-run the sweep.

b. Position the 0% Zone at the start of the sweep and the 100% Zone 9.5 divisions from the start of the sweep with the Channel A ZONE POSITION controls.

c. Set the MEASUREMENT AVERAGING switch to 8. Note the average readout of approximately a half-dozen measurements. Set the MEASUREMENT AVERAGING switch to 1.

d. Change the Sampling Time Base Unit Time/Div switch to the slowest equivalent-time sweep position (0.2 ms for the Type 3T4). Check the time for one sweep with a watch or stop-watch.

e. Check—the leakdown should not exceed 12 counts in 10 seconds (or 1.2 counts per second if the sweep lasts less than 10 seconds).

9b. Check Channel A Memory Leak Down (Real Time Plug-in Units)

a. Set the Time Base Unit Time/Div switch to 10 ms.

b. Position the 0% Zone at the start of the sweep, and the 100% Zone 9.5 divisions from the start of the sweep with the Channel A ZONE POSITION controls.

c. Check—Type 230 readout of 0.000 V, ±0.002 V.

d. Set the Time Base Unit Time/Div switch to 1.

e. Check—After three sweeps on the Type 568, check the Type 230 readout for 0.000 V, ±0.008 V.

f. Position the 100% Zone at the start of the sweep, and the 0% Zone 9.5 cm from the start of the sweep with the Channel A ZONE POSITION controls.

g. Check—After three sweeps on the Type 568, check the Type 230 readout for 0.000 V, ±0.008 V.

h. Set the Time Base Unit Time/Div switch to 10 ms.

i. Check—Type 230 readout of 0.000 V, ±0.002 V.

10. Check Channel B Memory Tracking

a. Set the Vertical Sampling Plug-In Mode switch to Channel B.

b. Set the MEASUREMENT MODE switch to B VOLTS.

c. Repeat parts b through h of Step 6 for checking the Channel B Memory Tracking. All control settings are the same, with the exception that all references should be made to Channel B.

11. Check Channel B Memory Leak Down

Repeat steps 7a and b for checking Channel B Memory leakdown. All control settings are the same with the exception that all references should be made to Channel B.

12. Check—Upper Limits (+ Count)

a. Set the Time-Base Sampling Plug-In for a slow sweep rate.

b. Set the TIME MEASUREMENT START and STOP POINT-LEVEL switches at HORIZ mm FROM SWP START.

c. Set the MEASUREMENT MODE switch to TIME.

d. Obtain a + four digit readout on the Type 230 by adjusting the LEVEL—Offset dials. A readout with no zeros or nines present is best, such as +1.812 MS.

e. Set the LOWER LIMIT dials to any number lower than the readout. Any (—) number is lower.

f. Set the UPPER LIMIT dials to the same number as obtained in the readout.

g. Check—WITHIN LIMIT Lamp (green) should be on, ABOVE UPPER AND BELOW LOWER LIMIT lamps should be off.

h. Set the UPPER LIMIT units dial one number smaller than the readout.

i. Check—WITHIN LIMITS lamp should turn off and ABOVE UPPER LIMIT lamp (red) should turn on after two sweeps.

j. Return the UPPER LIMIT units dial to the original number.

k. Check—WITHIN LIMITS lamp turns on and ABOVE UPPER LIMIT lamp turns off.

l. Continue this procedure as outlined in parts h through k with the UPPER LIMIT tens, hundreds, and thousands dials. The ABOVE UPPER LIMIT lamp should turn on when any one of the three dials is set to a number smaller than the readout.

13. Check Lower Limit (+ Count)

a. Set the UPPER LIMIT dials to a number larger than the readout.

b. Set the LOWER LIMITS dials to the same number as in the readout.

c. Check—WITHIN LIMITS lamp turns on, BELOW LOWER LIMIT lamp turns off.

d. Set the LOWER LIMIT units dials one number larger than the readout.

e. Check—WITHIN LIMITS lamp should turn off and BELOW LOWER LIMIT lamp should turn on.

f. Return the LOWER LIMIT units dial to the original number.

g. Check—WITHIN LIMITS lamp should turn on and BELOW LOWER LIMIT lamp should turn off.

h. Continue this procedure with the LOWER LIMIT tens, hundreds and thousands dials. The BELOW LOWER LIMIT lamp should light when any one of the three dials is set to a larger number than the readout.

14. Check Upper Limit (— Count)

a. Obtain a (—) four digit readout on the Type 230. This is accomplished most easily by reversing the settings of the TIME MEASUREMENT START and STOP POINT Offset dials.

b. Set the LOWER LIMIT dials to a more negative number than the readout.

c. Set the UPPER LIMIT dials to the same number as in the readout.

d. Check—WITHIN LIMITS lamp turns on, and ABOVE UPPER LIMIT lamp turns off.

e. Set the UPPER LIMIT units dial one number larger than the readout.

f. Check—WITHIN LIMITS lamp turns off and ABOVE UPPER LIMITS lamp turns on.

g. Return the UPPER LIMIT units dial to the original number.

h. Continue this procedure with the UPPER LIMITS tens, hundreds and thousands dials. The ABOVE UPPER LIMIT lamp should turn on if any of the three dials are set to a number larger than the readout.

15. Check Lower Limit (— Count)

a. Set the UPPER LIMIT thousands dial to + 1.

b. Set the LOWER LIMIT dials to the same number as in the readout.

c. Check—WITHIN LIMITS lamp turns on and BELOW LOWER LIMIT lamp turns off.

d. Set the LOWER LIMIT units dial one number smaller than the readout.

e. Check—WITHIN LIMITS lamp turns off and BELOW LOWER LIMIT lamp turns on.

f. Return the LOWER LIMIT units dial to the original number.

g. Continue with this procedure with the LOWER LIMIT tens, hundreds and thousands dial. The BELOW LOWER LIMIT lamp should turn on whenever any one of the three dials is set to a number smaller than the readout.

This completes the performance check for the Type 230. Turn off all equipment.

SECTION 7
CALIBRATION

General Information

Performance and/or calibration of the Type R230 should be checked after each 1000 hours of operation and at least once every 6 months to assure that the instrument is operating correctly and accurately. Recalibration of the instrument may be performed periodically as part of a regular preventive maintenance schedule, or may be done whenever the need is indicated by the performance check procedure. In addition, portions of the instrument will require recalibration if components have been replaced or other electrical repairs have been made in the circuitry.

Any needed maintenance should be performed before proceeding with the calibration. Trouble which becomes apparent during calibration should be corrected using the techniques given in the Maintenance section of this manual.

The calibration procedure given in this section is a combined verification and adjustment procedure that permits the instrument to be adjusted for best performance.

A calibration index is included at the beginning of the calibration procedure for use as a calibration guide and checklist.

The procedure is arranged in a sequence which allows the instrument to be calibrated with the least interaction of adjustments and reconnection of equipment. If desired, the steps may be performed out of sequence or a step may be done individually. However, it will be necessary to check any subsequent steps that might be affected by adjustments that are made. Power supply adjustments will affect the entire instrument.

When doing a complete recalibration of the instrument, best overall performance is obtained if each adjustment is made to the exact setting, even if the observed performance is within the allowable tolerance.

Throughout this procedure, each adjustment is designated by its circuit number (e.g., R635) and the color of the bracket holding the adjustment (e.g., red).

NOTE

This procedure is written for a Type 230 equipped with Buffer circuit card Model 4-up. Changes in this procedure for adjusting earlier models of the Buffer circuit card are located at the end of this procedure. Substitute the changed steps if adjusting Buffer Models 1-3.

RECOMMENDED EQUIPMENT

The following (or equivalent) equipment is recommended for complete calibration of this instrument (see Fig. 7-1). Specifications given are the minimum necessary for accurate calibration. All test equipment is assumed to be correctly calibrated and operating within the original specification, as are the Type 568 Oscilloscope and associated plug-in units used with the Type 230. If equipment is substituted, it must meet or exceed the requirements listed for the recommended equipment.

1. Precision differential DC voltmeter. Accuracy within ±0.05%; measurement resolution, 1 mV; range, 0.001 volt to 250 volts. John Fluke Model 825A recommended. Steps 1-6, 10-12, 14-15, 17-21.

2. Test oscilloscope. Bandwidth from DC to 40 MHz; deflection factor from 0.005 volt/div to 2 volts/div; sweep rates of 1 ms/div, 2 ms/div and 5 ms/div; Tektronix Type 453 Oscilloscope recommended. Steps 6-9, 12, 13, 16, 21.

3. 1× probe with BNC connector. Tektronix P6011 Probe, Part No. 010-0193-00, recommended. Steps 6-9, 12, 13, 16, 21.

4. Variable autotransformer. Output voltage variable from 104 to 126 volts AC RMS for 115-volt nominal operation or from 208 to 252 volts AC RMS for 230-volt nominal operation; output power 340 watts minimum. If a monitor voltmeter is not included, a separate AC voltmeter is required with an accuracy within 3% over the required range. General Radio W10MT3W Variac autotransformer recommended for 115-volt nominal operation; W10HMT3W for 230-volt nominal operation. All steps.

5. Oscilloscope to provide measurement information to the Type 230. Tektronix Type 568 with sampling plug-in units such as a Type 3S5 or 3S6 Vertical Unit, with two Type S-1 Sampling Heads and a Type 3T5 or 3T6 Sampling Sweep Unit recommended. All steps.

6. BNC female to GR connector adapter. Tektronix Part No. 017-0063-00. Step 19 and 21.

7. Two 42-inch 50 Ω coaxial cables with BNC connectors. Tektronix Part No. 012-0057-01 recommended. Step 19 and 21.

8. Shorting strap constructed of insulated copper wire and two alligator clips. Step 13 and 21.

9. Shorting strap constructed of insulated copper wire and three alligator clips. Steps 13-18, 21.

10. 36-pin J101 interconnecting cable, Tektronix Part No. 012-0119-01. All steps.

11. Pocket-type screwdriver with blade width less than 1/8th inch. All steps except 7.

12. 33 kΩ, 1/2 watt, 5% resistor with alligator clip soldered at each step. Steps 10-12.

13. Extender card, Tektronix Part No. 670-0240-00 and 670-0241-00 (both required, furnished with Type 230). Steps 8-16, 21.

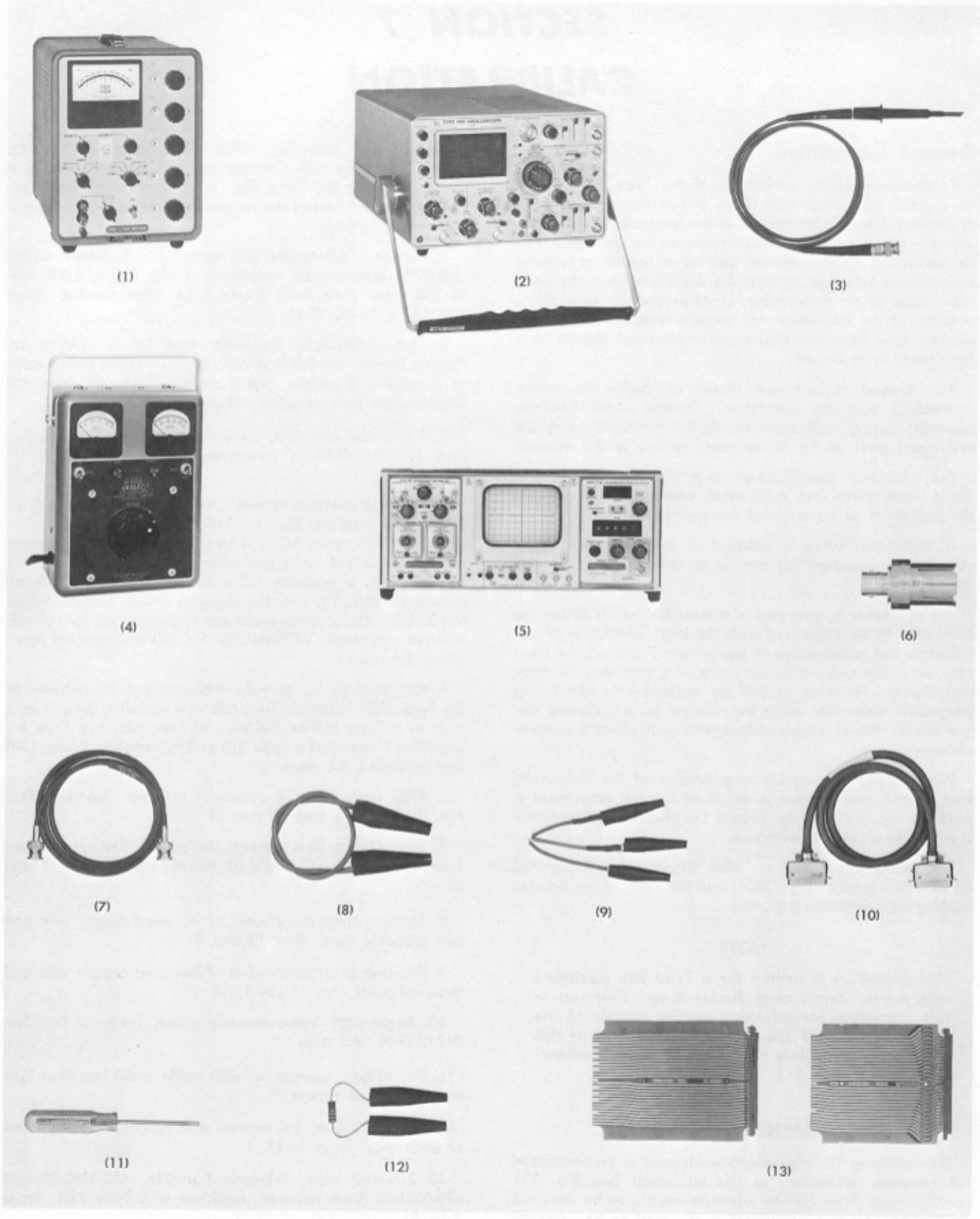


Fig. 7-1. Test equipment and accessories required for steps 1-29.

CALIBRATION INDEX AND RECORD PROCEDURE

This outline is provided to serve as a verification and calibration record. It may be reproduced for that purpose or for use as a calibration guide for calibrators who are familiar with the procedure.

Type 230 Serial Number _____

Calibration Date _____

Test Engineer _____

PROCEDURE

In the following procedure, complete control settings are listed for each major group of adjustments or checks. If only a partial calibration is to be performed, start with the setup preceding the desired portion of the procedure.

When connecting the precision differential DC voltmeter, unless otherwise specified, the positive lead is to be connected to the first test point mentioned and the negative lead is to be connected to the second test point mentioned.

CAUTION

If a null-type meter is used, always set the null to the VTVM (or lowest sensitivity) range before connecting the meter to a test point or before changing control settings of any instrument to which the meter is connected. Ensure that both inputs to the null-type meter are ungrounded.

Preliminary Procedure

1. Check that the voltage selector and range selector switch bars in the Line Voltage Selector assembly on the rear of the Type 230 and the Type 568 Oscilloscope are set to correspond to the autotransformer output voltage.

2. Connect the autotransformer, test equipment and Type 568 to a suitable power source.

3. Connect the Type 230 to the autotransformer.

4. Connect the 36-pin interconnecting cable between J101 of the Type 568 and J101 of the Type 230.

5. Turn on all equipment and set the autotransformer output for the nominal line voltage to be used (115 volts or 230 volts).

6. Allow at least 20 minutes warmup time at an ambient air temperature of between +20° C and +30° C (+68° F to +86° F) before making any checks or adjustments.

7. During the warmup period set the Type 230 and test instrument controls as follows:

Type 230

Triggered Measurement	Off
Display Time	Fully clockwise
Measurement Mode	Time
CRT Intensification	
Time Measurement	Off
Ref Zones	Off
Measurement Averaging	1
Ch A Reference Zones	
0% Position	2 switch positions clockwise from straight up
100% Position	4 switch positions clockwise from straight up
0% Level—Width	Average .3 CM
100% Level—Width	Average .3 CM
Ch B Reference Zones	
0% Position	2 switch positions clockwise from straight up
100% Position	4 switch positions clockwise from straight up
0%Level—Width	Average .3 CM
100% Level—Width	Average .3 CM
Time Measurement Start Point	
Channel	A
Level	% Between Zones
Offset dials	0-0
Slope	+, 1st
Time Measurement Stop Point	
Channel	A
Level	% Between Zones
Offset dials	0-0
Slope	+, 1st
Upper Limit	+3999
Lower Limit	—3999

Sampling Sweep Unit

Program Selector	Int
Horiz Pos	As is
Time/Div	100 ns
Samples/Sweep	1000
Delay	0000
Triggering	+, Ext
Sensitivity	Fully counterclockwise
Recovery Time	Centered

Type 568

Inten	Fully counterclockwise
Calibrator	Off
CRT Cathode Selector (rear panel)	Chopped Blanking
Others	As desired

Sampling Vertical Unit

Input Signal	None
Mode	Dual-Trace
Channels A and B	
Units/div	100
Variable	Cal
Invert	Pushed in
DC Offset Dials	000

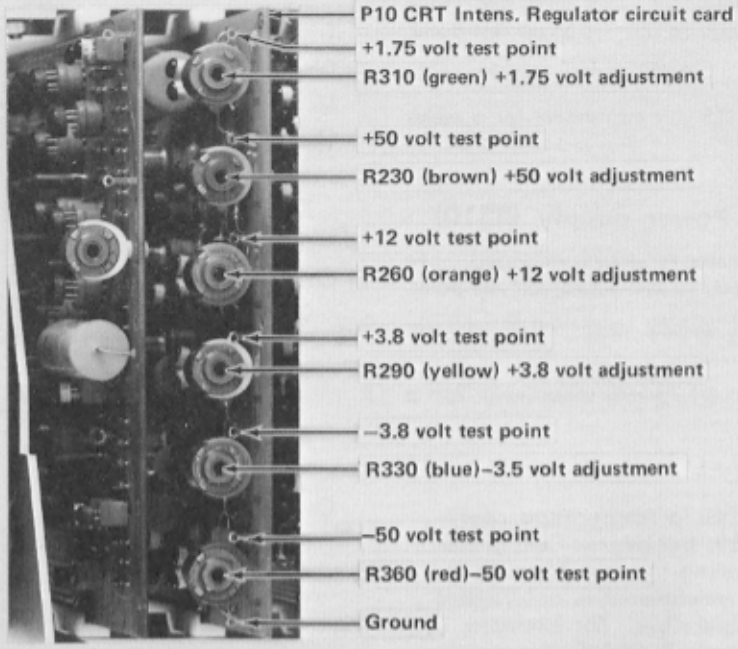


Fig. 7-2. Adjustment and test point locations for steps 1 through 9.

Test Oscilloscope

Horizontal Display	A
Time/Div	5 ms (calibrated)
Triggering	Auto, +, AC, Line
Vertical Mode	Ch 1
Channel 1	
Input Selector	AC
Volts/Div	5 mV (calibrated)
Position	Centered trace

1. Adjust +50-Volt Power Supply (R230)

a. Open the Type 230 front panel for access to the circuit cards.

b. Set the precision differential voltmeter to +50 volts.

c. Connect the negative lead of the voltmeter to the Gnd test point and the positive lead to the +50-volt test point on the CRT Intens/Regulator circuit card (see Fig. 7-2).

d. CHECK—Meter reading: +50.0 volts ±0.5 volt.

e. ADJUST—Resistor R230 (brown), +50-volt adjustment on the Regulator card for a meter reading of +50.0 volts.

2. Adjust —50-Volt Power Supply (R360)

a. Disconnect the positive lead of the voltmeter from the +50-volt test point and set the voltmeter polarity to —.

b. Connect the positive lead of the voltmeter to the —50-volt test point (see Fig. 7-2).

c. CHECK—Meter reading: —50.0 volts ±0.5 volt.

d. ADJUST—R360 (red), —50-volt adjustment for a meter reading of —50.0 volts.

3. Adjust +12-Volt Power Supply (R260)

a. Disconnect the positive lead of the differential voltmeter from the —50-volt test point and set the voltmeter to +12 volts.

b. Connect the positive lead of the voltmeter to the +12-volt test point (see Fig. 7-2).

c. CHECK—Meter reading: +12.00 volts ±0.12 volt.

d. ADJUST—R260 (orange), +12-volt adjustment for a meter reading of +12.00 volts.

4. Adjust +3.8-Volt Power Supply (R290)

a. Set the differential voltmeter to +3.8 volts and move the positive lead of the voltmeter to the +3.8-volt test point (Fig. 7-2).

b. CHECK—Meter reading: +3.800 volts ±0.038 volt.

c. ADJUST—R290 (yellow), +3.8-volt adjustment (Fig. 7-2) for a meter reading of +3.800 volts.

5. Adjust —3.5-Volt Power Supply (R330)

a. Set the differential voltmeter to —3.5 volts and move the positive lead of the voltmeter to the —3.5-volt test point.

b. CHECK—Meter reading: —3.500 volts ±0.035 volt.

c. ADJUST—R330 (blue), —3.5-volt adjustment for a meter reading of —3.500 volts.

6. Adjust +1.75-Volt Power Supply (R310)

a. Set the differential voltmeter to +1.75 volts and move the positive lead of the voltmeter to the +1.75-volt test point.

b. CHECK—Meter reading: +1.75 volts ±0.07 volt (at +25° C ±2° C).

c. ADJUST—R310 (green), +1.75-volt adjustment for a meter reading of +1.75 volts.

NOTE

The +1.75-volt supply has a temperature coefficient of about —4 millivolts per degree Centigrade. When checking and adjusting the +1.75-volt supply, change the voltage requirement in accordance with the ambient air temperature. For example, if the ambient air temperature is 20° C, the supply voltage should be +1.77 volts ±0.07 volt.

d. Remove the voltmeter leads from the test points.

7. Check Power Supply Ripple

a. Install the 1× probe on the Channel 1 input connector of the test oscilloscope.

b. Connect the test probe ground clip to the Ground test point on the CRT Intens/Regulator circuit card.

c. Connect the test probe successively to each of the test points given in Table 7-1. With the probe connected to each test point, observe the oscilloscope display while varying the autotransformer output between 104 and 126 volts AC RMS (208 and 252 volts AC RMS for 230-volt operation).

d. CHECK—Test oscilloscope display: Power supply ripple amplitudes not exceeding the maximum values given in Table 7-1.

e. Remove the probe from the Type 230.

f. Reset the autotransformer to the nominal line voltage (115 volts or 230 volts).

TABLE 7-1

Power Supply Regulation and Ripple

Voltage Test Point (See Fig. 7-2)	Maximum Ripple at twice line frequency Peak-to-Peak Voltage
+50 volts	±3 mV
—50 volts	±3 mV
+12 volts	±3 mV
+3.8 volts	±2 mV
—3.5 volts	±2 mV
+1.75 volts	±4 mV

Control Settings

Type 230

Triggered Measurement	Off
Display Time	**Fully counterclockwise**
Measurement Mode	Time
CRT Intensification	
Time Measurement	Off
Ref Zones	**Both**
Measurement Averaging	1
Ch A Reference Zones	
0% Position	2 switch positions clockwise from straight up
100% Position	4 switch positions clockwise from straight up
0% Level—Width	Average .3 CM
100% Level—Width	Average .3 CM
Ch B Reference Zones	
0% Position	2 switch positions clockwise from straight up
100% Position	4 switch positions clockwise from straight up
0% Level—Width	Average .3 CM
100% Level—Width	Average .3 CM
Time Measurement Start Point	
Channel	A
Level	% Between Zones
Offset dials	0-0
Slope	+, 1st
Time Measurement Stop Point	
Channel	A
Level	% Between Zones
Offset dials	0-0
Slope	+, 1st
Upper Limit	+3999
Lower Limit	—3999

Sampling Sweep Unit

Program Selector	Int
Time/Div	100 ns
Samples/Sweep	1000
Delay	0000
Triggering	+, Ext
Sensitivity	**Clockwise**
Recovery Time	Centered
Horiz Pos	**As is**

Type 568

Inten	**Normal brightness**
Focus	**Adjusted for well-focused trace**
Calibrator	Off
CRT Cathode Selector	Chopped Blanking
Others	As desired

Sampling Vertical Unit

Input Signal	None
Mode	Dual-Trace
Channels A and B	
Units/div	100
Variable	Calib
Invert	Pushed in
Ch A DC Offset Dial	**Trace just above CRT center**
Ch B DC Offset Dial	**Trace just below CRT center**

Test Oscilloscope

Horizontal Display	A
Time/Div	**1 ms (calibrated)**
Triggering	**Auto, +, AC, Int**
Vertical Mode	Channel 1
Channel 1	
Input Selector	**DC**
Volts/Div	**2 (calibrated)**
Position	**Centered Trace**

8. Adjust Ch A Memory 0% Range (R1064)

a. Turn off the Type 230 Power switch and remove the Ch A Memory circuit card.

b. Remove the circuit card extender from the holding slot next to the Limit circuit card. Connect the front and rear sections of the extender card together.

c. Insert the extender card in the Ch A Memory card jack and insert the Ch A Memory card in the extender.

d. Turn on the Type 230 Power switch and allow about 1 minute for warmup.

e. Check that all four intensified zones are visible on the Type 568 CRT.

f. Set the test oscilloscope Channel 1 Input Coupling switch to Gnd.

g. Position the test oscilloscope trace 1 division below the center horizontal graticule line.

h. Attach the 1× test probe to pin L of the extender card (Fig. 7-3).

i. Change the test oscilloscope Input Coupling switch to DC and trigger the test oscilloscope to obtain a stable display.

j. CHECK—Test oscilloscope display (see Fig. 7-4): Channel A 0% Memory discharged level 6.0 volts ±0.5 volt above the ground reference set up in part g of this step.

k. ADJUST—R1064, 0% Range adjustment on the Ch A Memory circuit card (Fig. 7-3) for a memory discharged level +6.0 volts above the ground reference.

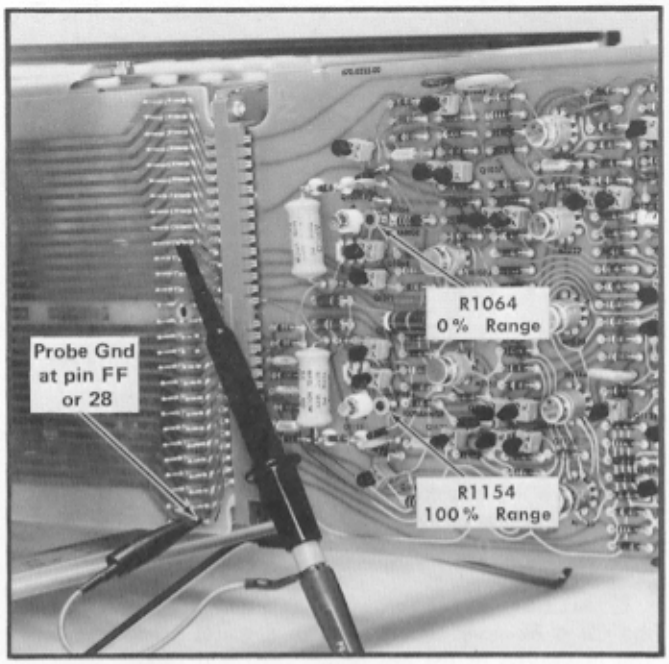


Fig. 7-3. Memory circuit card extended and the 1× probe connected to Pin L.

9. Adjust Ch A Memory 100% Range (R1154)

a. Move the 1× test probe to pin U of the extender card.

b. Set the test oscilloscope Triggering Slope switch to — and trigger the test oscilloscope display.

c. CHECK—Test oscilloscope display (see Fig. 7-4): 100% Memory discharged level 2.0 volts ±0.5 volt below the ground reference level.

d. ADJUST—R1154, 100% Range adjustment on the Ch A Memory circuit card (Fig. 7-3) for a memory discharged level 2.0 volts below the ground reference level.

e. Disconnect the test probe from the extender card.

10. Adjust Ch A Memory 0% Balance (R1077)

a. Turn off the Type 568 Power switch and remove the Sampling plug-in unit.

b. Turn off the Type 230 Power switch.

c. Remove the Ch A Memory circuit card, disconnect it from the extender card, and re-insert the memory circuit card into its jack.

d. Extend the Buffer circuit card.

e. Connect the 33 kΩ resistor across pins 21 and Y of the extender card.

f. Set the Type 230 Triggered Measurement switch to On, then turn on the Type 230 and Type 568 Power switches.

g. Set the differential voltmeter to 0 volts.

h. Connect the differential voltmeter between test points 1410 and 1460 on the Start Comparator circuit card (Fig. 7-5).

i. CHECK—Meter reading: 0.000 volt ±0.006 volt.

j. ADJUST—R1077 (black), 0% Balance adjustment on the Ch A Memory circuit card for a meter reading of 0.000 volt (Fig. 7-5).

11. Adjust Ch A Memory 100% Balance (R1147)

a. Move the negative lead of the voltmeter from test point 1460 to test point 1430 (Fig. 7-5).

b. CHECK—Meter reading: 0.000 volt ±0.006 volt.

c. ADJUST—R1147 (brown), 100% Balance adjustment on the Ch A Memory circuit card for a meter reading of 0.000 volt (measured across test points 1410 and 1430).

d. Remove the voltmeter leads from the test points.

e. Return the test oscilloscope Triggering Slope switch to +.

f. Turn off the Type 230 and Type 568 Power switches.

g. Remove the 33 kΩ resistor, disconnect the extender card, and re-insert the Buffer circuit card into the Type 230.

h. Re-install the Sampling plug-in unit in the Type 568.

i. Turn on the Type 230 and Type 568 Power switches.

12. Adjust and Check Ch B Memory Circuit

a. Turn off the Type 230 Power switch and extend the Ch B Memory circuit card.

b. Turn on the Type 230 Power switch and allow about 1 minute warmup.

c. Reset the following controls:

	Type 230
Triggered Measurement	Off
Time Measurement Start Point	
Channel	B
Time Measurement Stop Point	
Channel	B

d. Repeat steps 8 through 11, starting at step 8f, to adjust and check the Ch B Memory circuit card. All references to Ch A should be interpreted as Ch B. At step 10e, connect the 33 kΩ resistor across pins 27 and EE instead of 21 and Y.

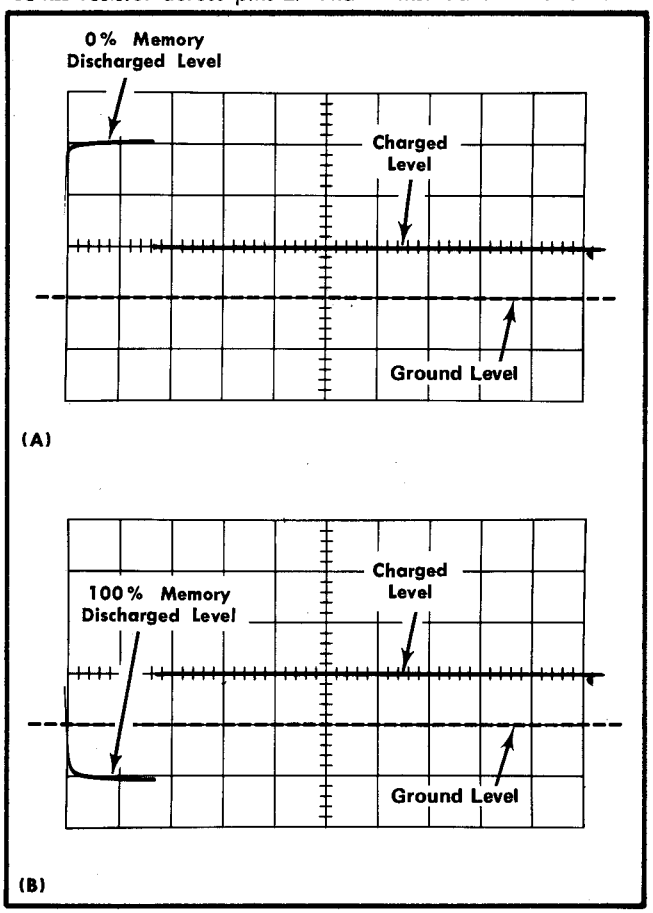


Fig. 7-4. Test oscilloscope display of (A) output of 0% Memory and (B) output of 100% memory.

NOTES

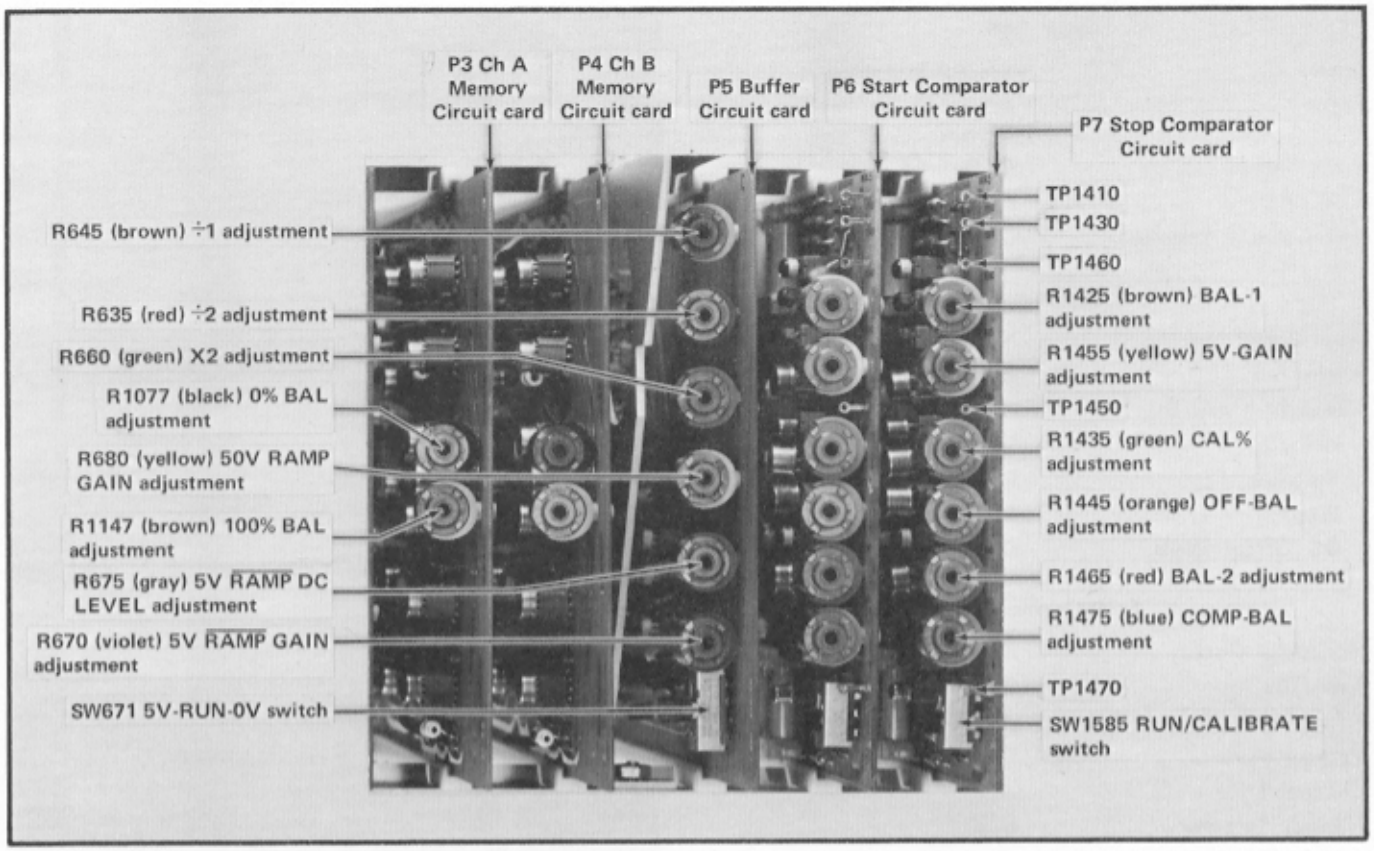


Fig. 7-5. Adjustment and test point locations for steps 11 through 27.

Control Settings

Type 230

Triggered Measurement	**Off**
Display Time	Fully counterclockwise
Measurement Mode	Time
CRT Intensification	
Time Measurement	Off
Ref Zones	Both
Measurement Averaging	1
Ch A Reference Zones	
0% Position	**Index dot straight up**
100% Position	**Index dot straight up**
0% Level—Width	Average .3 CM
100% Level—Width	Average .3 CM
Ch B Reference Zones	
0% Position	**Index dot straight up**
100% Position	**Index dot straight up**
0% Level—Width	Average .3 CM
100% Level—Width	Average .3 CM
Time Measurement Start Point	
Channel	**A**
Level	% Between Zones
Offset dials	0-0
Slope	+, 1st
Time Measurement Stop Point	
Channel	**A**
Level	% Between Zones
Offset dials	0-0
Slope	+, 1st
Upper Limit	+3999
Lower Limit	—3999

Sampling Sweep Unit

Program Selector	Int
Time/Div	100 ns
Samples/Sweep	1000
Delay	0000
Triggering	+, Ext
Sensitivity	Clockwise
Recovery Time	Centered
Horiz Pos	**Trace start at graticule left edge**

Type 568

Inten	Normal brightness
Focus	Adjusted for well-focused trace
Scale Illum	As Desired
Calibrator	Off
CRT Cathode Selector	Chopped Blanking

Sampling Unit

Input Signal	None
Mode	Dual-Trace
Channels A and B	
Units/Div	100
Variable	Cal
Invert	Pushed In
DC Offset Dials	**000**

Test Oscilloscope

Horizontal Display	A
Time/Div	**2 ms (calibrated)**
Triggering	Auto, +, AC, Int
Vertical Mode	Channel 1
Channel 1	
Input Selector	**GND**
Volts/Div	**.5 (calibrated)**
Position	Centered Trace

13. Adjust Start Comparator Offset Bal (R1445)

a. Set the front-panel controls as given following step 12.

b. Turn off the Type 230 Power switch, remove the extender card, and remove both Memory circuit cards. Note the positions of these cards, so that each may be re-installed in its original place.

c. Extend the Start Comparator circuit card on the extender card.

d. Connect the two-ended shorting strap across D1445 on the Start Comparator card (see Fig. 7-6A).

e. Connect the three-ended shorting strap to pins B, H and J of the extender card (see Fig. 7-6B).

f. Turn on the Type 230 Power switch and allow about 1 minute for warmup.

g. Connect the test oscilloscope probe ground lead to pin 1 of the extender card (reference ground) and connect the probe tip to either end of D1445 (see Fig. 7-6A).

h. Set the test oscilloscope Input Coupling switch to DC.

i. CHECK—Test oscilloscope trace position: Centered trace ±1 major division (0 volts ±0.5 volt). It may be necessary to increase the Volts/Div setting to initially locate the trace position.

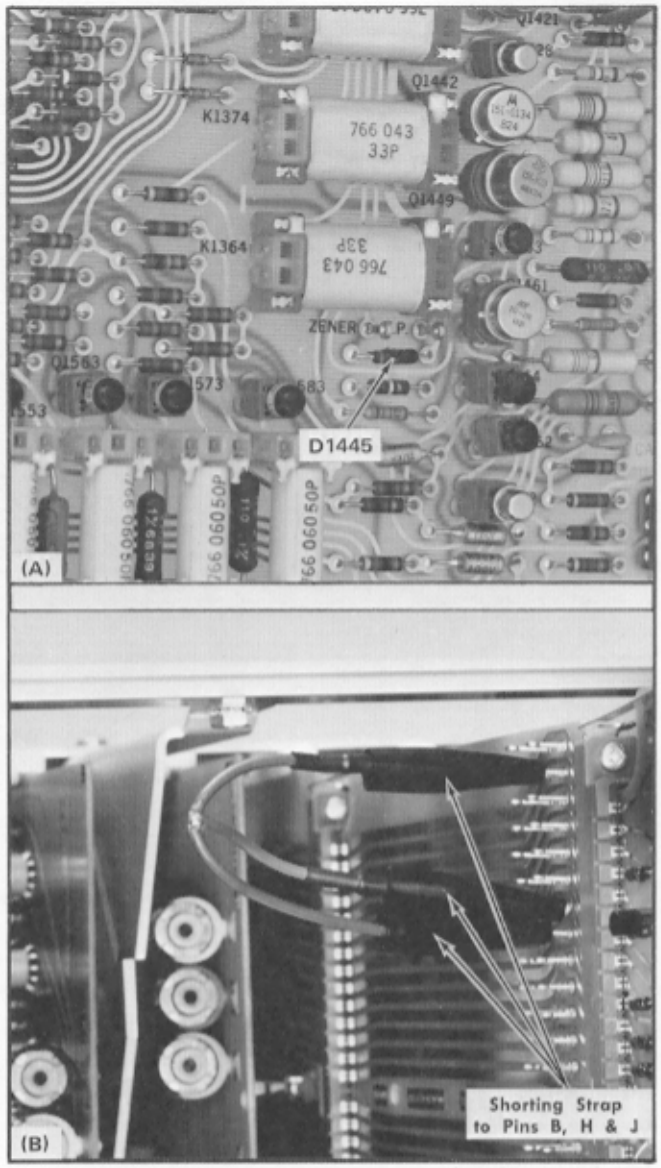


Fig. 7-6. Start Comparator circuit card with (A) location of D1445 and (B) special shorting strap connected.

j. ADJUST—R1445 (orange), Off Bal adjustment (located on the Start Comparator circuit card, Fig. 7-5) for a centered trace on the test oscilloscope display. Wait for 1 minute, then readjust if drift has occurred.

k. Turn off the Type 230 Power switch.

l. Remove the probe, ground lead, and the two-ended shorting strap from the Type 230.

m. Turn on the Type 230 Power switch and allow about 1 minute for warmup.

14. Adjust Start Comparator Bal 1 (R1425)

a. Connect the differential voltmeter between test points 1450 (positive lead) and 1460 (negative lead) on the Start Comparator circuit card (see Fig. 7-5).

b. CHECK—Meter reading: 0.000 volt ±1 mV.

c. ADJUST—R1425 (brown), Bal 1 adjustment on the Start Comparator circuit card (Fig. 7-5) for a meter reading of 0.000 volt.

15. Pre-adjust Start Comparator Bal 2 (R1465)

a. Move the positive lead of the differential voltmeter from test point 1450 to test point 1470 (see Fig. 7-5).

b. CHECK—Meter reading: 0.000 volt ±2 mV.

c. ADJUST—R1465 (red), Bal 2 adjustment on the Start Comparator circuit card (Fig. 7-5) for a meter reading of 0.000 volt.

d. Leave the voltmeter leads connected for a later step in this procedure.

16. Adjust Start Comparator Comp Bal (R1475)

a. Connect the test probe ground lead to pin FF and the 1× test probe tip to pin 7 of the extender card.

b. Set the test oscilloscope Triggering Level control for a free-running display.

c. Position the display so that it is centered on the center horizontal graticule line of the test oscilloscope CRT.

d. Set the Type 568 Samping Sweep Time/Div control to 10 μs.

e. CHECK—Test oscilloscope display. Noise waveform similar to that shown in Fig. 7-7.

f. ADJUST—R1475 (blue), Comp Bal adjustment on the Start Comparator circuit card (Fig. 7-5) so that the maximum intensity portion of the noise display is at the center of the display excursion.

g. Remove the test probe from the extender card.

17. Adjust Start Comparator 5 V Gain (R1455)

a. Set the Run/Calibrate switch (see Fig. 7-5) to the Calibrate position.

b. Set the voltmeter to +5.000 volts.

c. Set the Type 230 Time Measurement Start Point Level switch to mm Above 0% Zone.

d. CHECK—Meter reading +5.000 volts ±14.5 mV, with the voltmeter connected between test points 1470 and 1460 on the Start Comparator circuit card.

e. ADJUST—R1455 (yellow), 5 V gain adjustment (Fig. 7-5) for a meter reading of +5.000 volts.

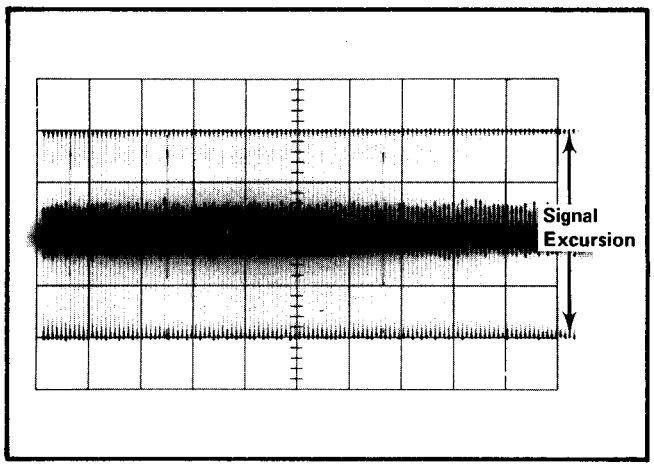


Fig. 7-7. Typical test Oscilloscope display when adjusting Start Comparator Comp. Bal.

18. Adjust Start Comparator Bal 2 (R1465)

a. Set the voltmeter polarity to —.

b. Set the Type 230 Time Measurement Start Point Level switch to mm Below 100% Zone.

c. CHECK—Meter reading: —5.000 volts ±2 mV.

d. ADJUST—R1465 (red), Bal 2 adjustment (Fig. 7-5), for one-half the error from 5.000 volts if the voltage does not meet the ±2 mV tolerance.

e. Repeat steps 17b through 18d until both voltages are within tolerance.

f. Set the voltmeter polarity to +.

g. Set the Type 230 Measurement Start Point Level switch to Horiz mm From Swp Start.

h. CHECK—Meter reading: +5.000 volts ±14.5 mV.

i. Set the voltmeter to 0.000 volt.

j. Set the Type 230 Time Measurement Start Point Level switch to mm Below 100% Zone.

k. Set the Start Comparator Run/Calibrate switch to the Run position.

l. CHECK—Meter reading: 0.000 volt ±2 mV.

m. Remove the voltmeter leads from the Start Comparator circuit card.

n. Turn off the Type 230 Power switch.

o. Remove the special shorting strap from pins B, H and J of the extender card and insert the two Memory circuit cards into the Type 230. Remove the extender card and insert the Comparator card into the Type 230.

p. Turn on the Type 230 Power switch and allow about 1 minute for warmup.

Control Settings

Type 230

Triggered Measurement	**On**
Display Time	Fully counterclockwise
Measurement Mode	Time
CRT Intensification	
Time Measurement	Off
Ref Zones	Both
Measurement Averaging	1
Ch A Reference Zones	
0% Position	Index dot straight up
100% Position	Index dot straight up
0% Level—Width	Average .3 CM
100% Level—Width	Average .3 CM
Ch B Reference Zones	
0% Position	Index dot straight up
100% Position	Index dot straight up
0% Level—Width	Average .3 CM
100% Level—Width	Average .3 CM
Time Measurement Start Point	
Channel	A
Level	**% Between Zones**
Offset dials	0-0
Slope	+, 1st
Time Measurement Stop Point	
Channel	A
Level	% Between Zones
Offset dials	0-0
Slope	+, 1st
Upper Limit	+3999
Lower Limit	—3999

Sampling Sweep

Program Selector	Int
Time/Div	**1 μs**[1]
Samples/Sweep	1000
Delay	0000
Triggering	+, Ext
Sensitivity	Clockwise
Recovery Time	Centered
Horiz Pos	Trace start at graticule left edge

Type 568

Inten	Normal brightness
Focus	Adjusted for a well-focused trace
Scale Illum	As desired
Calibrator	**100 kHz**[1]
CRT Cathode Selector	Chopped blanking

Sampling Unit

Mode	**Ch A**
Channel A	
Units/Div	100
Variable	Cal
Invert	Pushed in
DC Offset dial	000

Differential Voltmeter

Polarity	+

[1]On earlier models of the Type 568, set the Calibrator switch to 20 kHz and the Time/Div switch to 5 μS.

19. Adjust Start Comparator Cal % (R1435)

a. Set the front-panel controls as given following step 18.

b. Connect the Type 568 Calibrator 5 V output via a 50 Ω BNC cable through a BNC to GR adapter to the sampling head input (Channel A).

c. Connect the Type 568 + Pretrigger output via a 50 Ω BNC cable to the sampling sweep Ext trigger input.

d. Trigger the display with the Type 568 sampling sweep Sensitivity control. Adjust the sampling sweep Recovery Time control for an optimum display. Vertically center the display.

e. With the Type 230 Ch A Reference Zones Position controls, position the Channel A 0% zone just before the first positive-going segment of the square-wave signal, and the Ch A 100% zone just after the first positive-going segment of the display.

f. Set the Start Comparator Run/Calibrate switch to Calibrate.

g. Connect the differential voltmeter between test points 1430 and 1470 on the Start Comparator circuit card (see Fig. 7-5).

h. CHECK—Meter reading: 0.000 volt ±14.5 mV.

i. ADJUST—R1435 (green), Cal % adjustment (located on the Start Comparator circuit card, Fig. 7-5) for a meter reading of 0.000 volt.

j. Disconnect the voltmeter leads.

k. Remove the coaxial cables from the Type 568 Calibrator outputs.

20. Check Start Comparator Offset Voltage Out

a. Change the sampling sweep controls as follows:

Trigger Sensitivity	Fully counterclockwise
Time/Div	100 ns

b. Set the Start Comparator Run/Calibrate switch to Run (Fig. 7-5).

c. Set the Type 230 Time Measurement Start Point Level switch to mm Above 0% Zone.

d. Connect the differential voltmeter between test points 1470 (positive lead) and 1460 (negative lead) on the Start Comparator circuit card.

e. Set the Time Measurement Start Point Level Offset dials as given in Table 7-2.

f. CHECK—Meter readings within the tolerance specified in the table.

TABLE 7-2

Comparator Offset Check

Offset Dial Setting	Voltage Between TP1470 and TP1460	Tolerance: ±(0.25% + 2 mV)
0-0	0 mV	±2.0 mV
0-1	50 mV	±2.1 mV
0-2	100 mV	±2.3 mV
0-4	200 mV	±2.5 mV
0-8	400 mV	±3.0 mV
1-0	500 mV	±3.3 mV
2-0	1.0 volt	±4.5 mV
4-0	2.0 volts	±7.0 mV
8-0	4.0 volts	±12.0 mV
9-9	4.95 volts	±14.4 mV

g. Disconnect the voltmeter leads.

21. Adjust and Check Stop Comparator Circuit

a. Repeat steps 13 through 20 of this procedure to calibrate the Stop Comparator circuit card. The calibration procedure is exactly the same as for the Start Comparator circuit card. The illustrations and control settings used in conjunction with steps 13 through 20 should be used with this procedure, except that "Time Measurement Start Point" should be interpreted as "Time Measurement Stop Point" and "Start Comparator circuit card" should be interpreted as "Stop Comparator circuit card".

Control Settings

Type 230

Triggered Measurement	**Off**
Display Time	**Centered**
Measurement Mode	Time
CRT Intensification	
Time Measurement	**On**
Ref Zones	**Off**
Measurement Averaging	1
Ch A Reference Zones	
0% Position	**Index dot straight up**
100% Position	**index dot straight up**
0% Level—Width	Average .3 CM
100% Level—Width	Average .3 CM
Ch B Reference Zones	
0% Position	Index dot straight up
100% Position	Index dot straight up
0% Level—Width	Average .3 CM
100% Level—Width	Average .3 CM
Time Measurement Start Point	
Channel	A
Level	**Horiz mm From Swp Start**
Offset dials	**1-0**
Slope	+, 1st
Time Measurement Stop Point	
Channel	A
Level	**Horiz mm From Swp Start**
Offset dials	**9-0**
Slope	+, 1st
Upper Limit	+3999
Lower Limit	—3999

Sampling Sweep

Program Selector	Int
Time/Div	**1 μS**
Samples/Sweep	1000
Delay	0000
Triggering	+, Ext
Sensitivity	Free-running trace
Recovery Time	Centered
Horiz Pos	Trace start at graticule left edge.

Type 568

Inten	Normal Brightness
Focus	Adjusted for a well-focused trace
Scale Illum	As desired
Calibrator	**Off**
CRT Cathode Selector	Chopped Blanking

	Sampling Unit
Input Signal	None
Mode	Ch A
Channel A	
Units/Div	100
Variable	Cal
Invert	Pushed in
DC Offset dial	000

22. Adjust Buffer 5 V RAMP DC Level (R675) Model 4-up

a. Set the 5 V-RUN-0 V switch on the Buffer circuit card to the 0 V position (Fig. 7-5).

b. Connect the differential voltmeter between test points 1410 and 1460 on the Start Comparator circuit card.

c. CHECK—Meter reading: 0.000 volts ±0.020 volt.

d. ADJUST—R675 (gray) 5 V RAMP DC Level adjustment (on the Buffer circuit card) for a meter reading of 0.000 volts.

23. Adjust Buffer 5 V $\overline{\text{RAMP}}$ Gain (R670) Model 4-up

a. Set the differential voltmeter to +5 volts.

b. Set the 5 V-RUN-0 V switch to the 5 V position.

c. CHECK—Meter reading: 1/10 the 50 V supply reading ±0.025 volt.

d. ADJUST—R670 (violet), 5 V $\overline{\text{RAMP}}$ Gain adjustment on the Buffer card for a meter reading of 1/10 the +50 V supply reading.

e. If adjustment of R670 was required, recheck the 5 V RAMP DC Level adjustment as described in step 22.

f. Remove the meter leads from the test points.

g. Set the 5 V-RUN-0 V switch to the RUN position.

h. CHECK—Type 230 readout: +08.00μS. Typically, the readout will not vary more than ±5 counts.

i. Adjust the Type 568 Inten control so that only the intensified zone is displayed.

j. CHECK—Type 568 display: Intensified zone length of 8.0 major divisions ±½ minor division.

k. Adjust the Sampling Sweep front-panel Horiz Gain adjustment, if necessary, to obtain an intensified zone length of 8.0 major divisions.

24. Adjust Buffer Voltmeter Ramps (R645, R635, R660)

a. Change the following front panel controls:

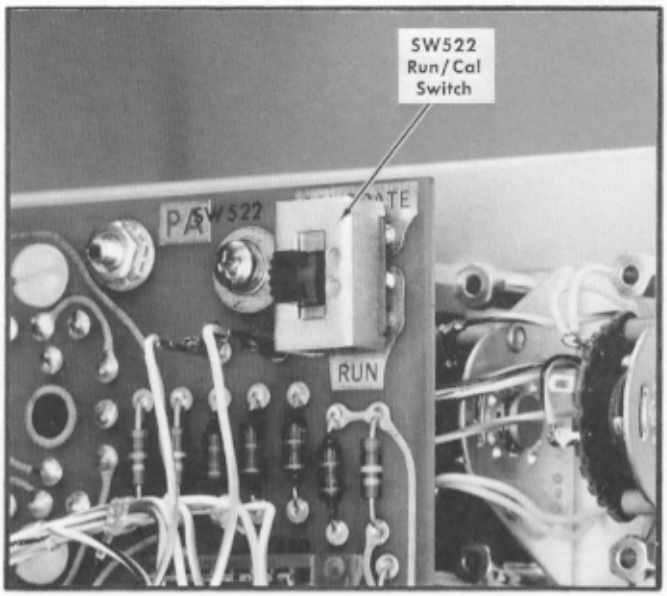


Fig. 7-8. Location of Run/Calibrate switch on the Counter circuit card.

	Type 230
Time Measurement Start Point	
Level	mm Above 0% Zone
Offset dials	0-0
Time Measurement Stop Point	
Level	mm Above 0% Zone
Offset dials	8-0
Measurement Averaging	8

b. Set the Type 230 RUN/Calibrate switch to Calibrate (located on the counter circuit board; Fig. 7-8).

c. Set the Sampling Plug in Units/Div switch to 200.

d. Position the Type 568 trace at the bottom horizontal graticule line.

e. CHECK—Type 230 readout: +1.600 V ±0.008 V.

f. ADJUST—R660 (green) ×2 adjustment on the Buffer circuit card, (see Fig. 7-5) for a Type 230 readout of +1.600 V.

g. Set the Sampling Plug in Units/Div switch to 100.

h. Position the Type 568 trace to the bottom horizontal graticule line.

i. CHECK—Type 230 readout: +0800. MV ±0004. MV.

j. ADJUST—R645 (brown) ÷ 1 adjustment on the Buffer circuit card, (Fig. 7-5) for a Type 230 readout of +0800. MV.

k. Set the Sampling Plug in Units/Div switch to 50.

l. Position the Type 568 trace to the bottom horizontal graticule line.

m. CHECK—Type 230 readout: +0400. MV ±0002. MV.

n. ADJUST—R635 (red), ÷ 2 adjustment on the Buffer circuit card (see Fig. 7-5) for a Type 230 readout of +0400 MV.

o. Return the Sampling Plug in Units/Div switch to 100.

p. Return the Run/Calibrate switch (on the Counter board) to Run.

25. Adjust Ch A Zone Generator 0% Position (R805) and 100% Position (R905)

a. Reset the following front-panel controls:

Type 230

CRT Intensification	
Ref Zones	0%
Time Measurement	Off

b. Position the Channel A trace slightly above the center horizontal graticule line.

c. Check that the Type 568 sweep starts at the extreme left vertical graticule line. Adjust the Sampling Sweep Horiz Pos control if necessary.

d. Turn the Ch A Reference Zones 0% Position control to set the index dot on the knob 2 positions clockwise from the straight-up position.

e. CHECK—Type 568 display: Channel A 0% intensified zone starts within ½ minor division of the 1-cm vertical graticule line (1 cm in from the extreme left vertical line).

f. ADJUST—R805 (black), the 0% Position adjustment on the Ch A Zone Generator circuit card (Fig. 7-9), so that the intensified zone starts at the 1-cm vertical graticule line.

g. Set the CRT Intensification Ref Zones switch to 100%.

h. Turn the Ch A Reference Zones 100% Position control 2 positions clockwise from the straight-up position of the index dot.

i. CHECK—Type 568 display: Channel A 100% intensified zone starts within ½ minor division of the 1-cm vertical graticule line.

j. ADJUST—R905 (brown), the 100% Position adjustment on the Ch A Zone Generator circuit card (Fig. 7-9) so that the intensified zone starts at the 1-cm vertical graticule line.

26. Adjust Ch B Zone Generator 0% Position (R805) and 100% Position (R905)

a. Set the Sampling Unit Mode switch to Ch B.

b. Repeat step 25 for calibration of the Ch B Zone Generator 0% Position and 100% Position adjustment. References to Channel A should be interpreted as Channel B.

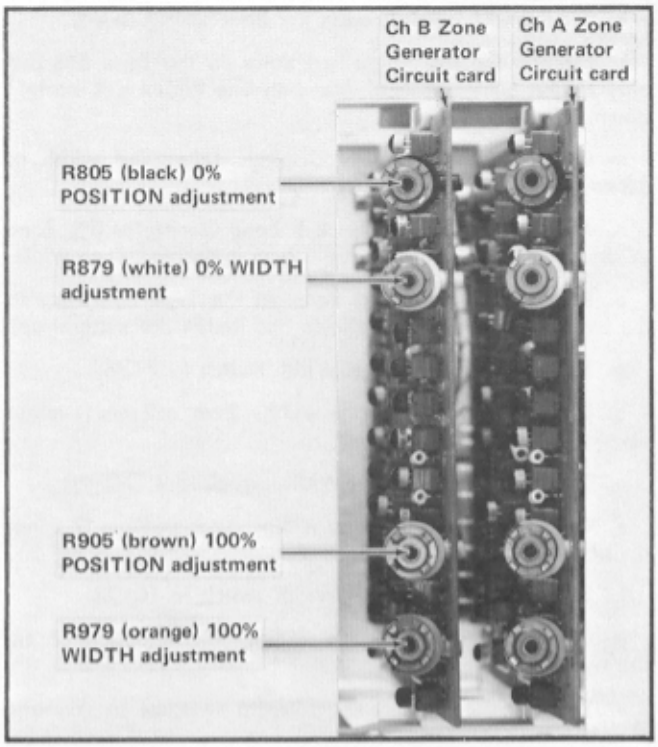


Fig. 7-9. Adjustment locations for steps 28-31.

27. Adjust Ch B Zone Generator 0% Zone Width (R879) and 100% Zone Width (R979)

a. Position the 100% intensified zone on the Type 568 trace to the center vertical graticule line (Index dot straight down).

b. CHECK—Type 568 CRT display: Intensified zone width of 0.3 cm ±0.1 cm.

c. ADJUST—R979 (orange), Ch B Zone Generator 100% Zone Width adjustment (Fig. 7-9) for 0.3 cm intensified zone width.

d. Position the 100% intensified zone on the Type 568 trace to the extreme left vertical graticule line (Index dot straight up).

e. Set the Ch B 100% Level-Width switch to 2 CM.

f. CHECK—Intensified zone width: 2 cm ±2 mm (1 minor division).

g. Set the Ch B 100% Level-Width switch to 4 CM.

h. CHECK—Intensified zone width: 4 cm ±4 mm (2 minor divisions).

i. Set the Ch B 100% Level-Width switch to 10 CM.

j. CHECK—Intensified zone width: Intensification of entire sweep.

k. Set the CRT Intensification Ref Zone switch to 0%.

l. Position the 0% intensified zone on the Type 568 display to the center vertical graticule line (Index dot straight down).

m. CHECK—Type 568 CRT display: Intensified width of 0.3 cm ±0.1 cm.

n. ADJUST—R879 (white), Ch B Zone Generator 0% Zone Width adjustment (Fig. 7-9) for 0.3 cm intensified zone width.

o. Position the intensified zone on the Type 568 trace to the extreme left vertical graticule line (Index dot straight up).

p. Set the Ch B 0% Level-Width switch to 2 CM.

q. CHECK—Intensified zone width: 2 cm ±2 mm (1 minor division).

r. Set the Ch B 0% Level-Width switch to 4 CM.

s. CHECK—Intensified zone width: 4 cm ±4 mm (2 minor divisions).

t. Set the Ch B 0% Level-Width switch to 10 CM.

u. CHECK—Intensified zone width: Intensification of entire sweep.

v. Set both Channel B Level-Width switches to Average .3 CM.

28. Adjust Ch A Zone Generator 0% Zone Width (R879) and 100% Zone Width (R979)

a. Set the Sampling Unit Mode switch to Ch A.

b. Set the CRT Intensification Ref Zones switch to 100%.

c. Repeat step 27. All references to Channel B should be interpreted as Channel A.

29. Adjust Buffer 50 V $\overline{\text{RAMP}}$ Gain (R680)

a. Set the Sampling Unit Mode switch to Dual-Trace.

b. Position the Channel A trace slightly above the center horizontal graticule line and the Channel B trace slightly below the center horizontal graticule line.

c. Turn the Ch A and Ch B Reference Zones 0% Position controls 2 positions counterclockwise from the straight-up position.

d. CHECK—Type 568 display: Channel A and Channel B 0% intensified zones start within ½ minor division of the 9-cm vertical graticule line (1 cm to the left of the extreme right graticule line).

e. ADJUST—R680 (yellow), the 50 V RAMP Gain adjustment on the Buffer circuit card (see Fig. 7-5), to position the start of the intensified zones at the 9-cm vertical graticule line. If adjustment of R680 is required, repeat steps 22, 23, 25, 26, 27, 28 and 29.

f. Set the CRT Intens Ref zones switch to 100%.

g. With the Ch A and Ch B Reference Zones 100% Position controls, position both intensified zones at the 9-cm vertical graticule line.

h. CHECK—Type 568 display: Channel A and Channel B 100% intensified zones start within ½ minor division of the 9-cm vertical graticule line. If not correct, readjust R680 (50 V RAMP Gain adjustment) for a compromise setting so that both the 0% and 100% intensified zone positions are within tolerance as described in parts d and h of this step.

NOTES

PROCEDURE CHANGES FOR TYPE 230 EQUIPPED WITH BUFFER CIRCUIT CARD MODELS 1 THROUGH 3

Do not follow steps 22, 23 and 29 in the main procedure. Instead, substitute the following steps in place of steps 22 and 23:

22. Adjust Buffer Sweep DC Level (R675)

a. Set the controls as given following step 21 with the following exceptions:

	Type 568
Power	Off

	Type 230
Power	Off
Triggered Measurement	On

b. Remove the Sampling Sweep Unit from the Type 568.

c. Set the Differential Voltmeter to 0 Volt.

d. Extend the Buffer circuit card.

e. Connect the two-ended shorting strap across pins P and FF of the extender card.

f. Turn on the Type 230 Power switch.

g. Connect the positive meter lead to pin L and the negative lead to pin FF of the extender card.

h. CHECK—Buffer Sweep DC Level: 0.000 volt ±0.020 volt.

i. ADJUST—R675 (gray), SWP DC LEVEL adjustment for a voltmeter reading of 0.000 volt (Fig. 7-10).

j. Turn off the Type 230 Power switch and remove the meter leads.

23. Adjust Buffer Sweep Gain (R670)

a. Connect the two-ended shorting strap across pins P and V of the extender card.

b. Set the Differential Voltmeter to +50.00 volts.

c. Turn on the Type 230 Power switch.

d. Connect the positive meter lead to pin V (+50 volts) and the negative lead to pin FF (ground) of the extender card.

e. Record the meter reading; it should be +50 volts ±0.5 volt.

f. Disconnect the positive lead from pin V and set the meter to +5.000 volts.

g. Connect the positive meter lead to pin L of the extender card.

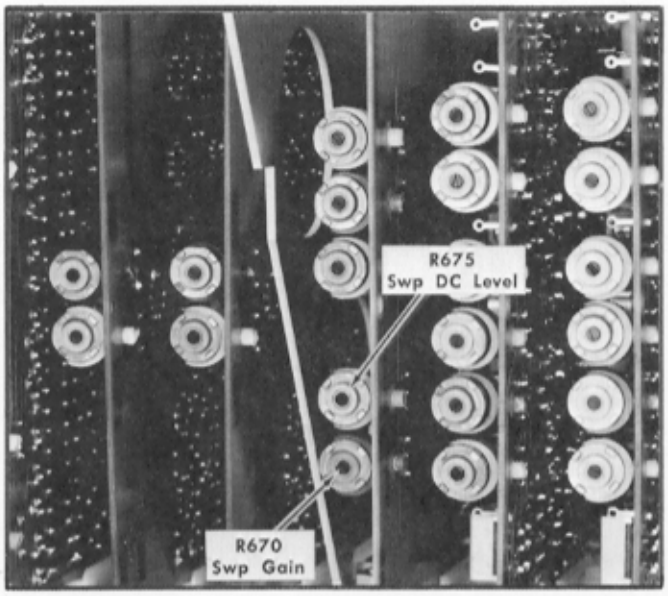


Fig. 7-10. Location of Sweep Gain and Sweep DC Level adjustments on the Buffer circuit card. (Models 1-3).

h. CHECK—Buffer Sweep Gain: Meter reading of one-tenth the voltage recorded in part e, ±0.025 volt.

i. ADJUST—R670 (violet), SWP GAIN adjustment for one-tenth the voltage recorded in part e (Fig. 7-10).

j. Turn off the Type 230 Power switch.

k. Disconnect the meter leads and shorting strap from the extender card.

l. Remove the Buffer circuit card and the extender card, then re-install the Buffer card in its jack (J5).

m. Re-install the Sampling Sweep Unit into the Type 568.

This completes the calibration procedure for the Type 230. Turn off and disconnect all test equipment. Replace the extender circuit cards into their holder and secure the front-panel.

NOTES

SECTION 8
RACKMOUNTING

Introduction

The Tektronix Type R230 is designed to be mounted in a standard 19-inch-wide rack with universal hole spacing[1]. When mounted with the ruggedizing hardware as described below, and when properly calibrated, this instrument will meet all electrical and environmental specifications given in Section 1.

General Information

The slide-out tracks provided with the Type R230 permit it to be extended out of the rack for troubleshooting or servicing (see Fig. 8-1). When not extended, the instrument is held into the rack with four securing screws.

The chassis sections of the slide-out tracks are installed on the chassis at the factory, and the stationary sections are to be attached to the mounting rails of the racks. When installed, the intermediate sections slide freely between the chassis and stationary sections as the instrument is pulled out or pushed into the rack.

[1] **Universal hole spacing is: 5/8", 5/8", 1/2", 5/8", 5/8", 1/2", · · · · Racks with other hole spacing may need to have additional holes drilled and tapped in the support rails at the locations indicated in Figs. 8-5 and 8-9.**

The mounting hardware provided with the Type R230 is intended to make the tracks adaptable to a variety of racks and installation methods. Not all of the hardware will be needed for any particular installation, so only the parts that are required for the specific mounting method should be used.

In order to operate the Type R230 in the extended position, the instrument must be mounted close enough to its companion instruments to permit the interconnecting cables to reach between instruments, and the input power connection must be located close enough for the power cord to reach.

Mounting Considerations

A wide variety of mounting methods are available for installing the slide-out tracks in the rack. The following factors should be taken into consideration when choosing the mounting method for a particular installation:

1. Depth of the rack.

2. Degree of mechanical stability required.

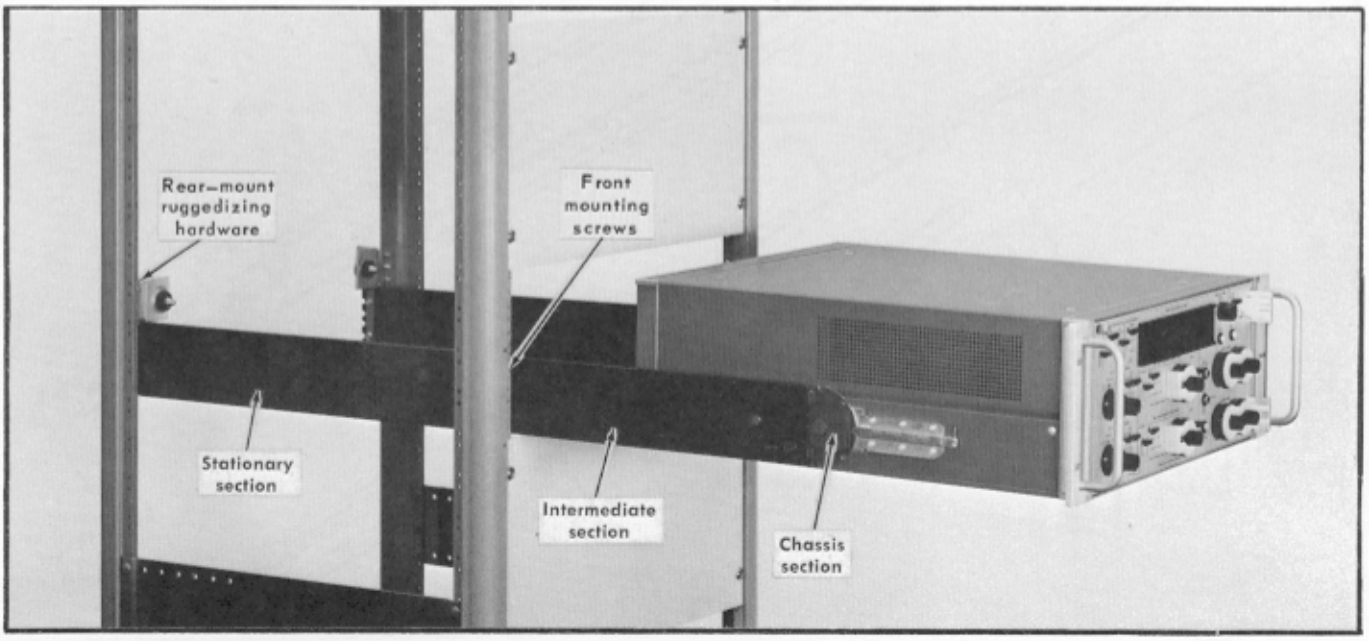


Fig. 8-1. The Type R230 extended on slide-out tracks. Shown with rack sides removed.

3. Mounting method used for other instruments in the rack.

4. Type of mounting holes in the supporting rails; that is, whether they are tapped, untapped, or countersunk.

5. Whether or not the rear support rails are movable, whether they can be positioned at any location or moved only in discrete increments.

6. Relative thicknesses of the front panels of the various instruments in the rack.

7. General appearance desired for the completed rack assembly.

8. Length of the stationary sections of the slide-out tracks.

Serial Number Range	Stationary/Intermediate Sections		Chassis Sections		(Group)
	Length	Tek. Part No.	Length	Tek. Part No.	
B010100-B030209	22 in.	351-0086-00	11 3/4 in.	351-0027-00	A
B040210-B050322	20 in.	351-0085-00	11 3/4 in.	351-0027-00	B
B050323 and up	22 in.	351-0086-00	13 1/4 in.	351-0082-00	C

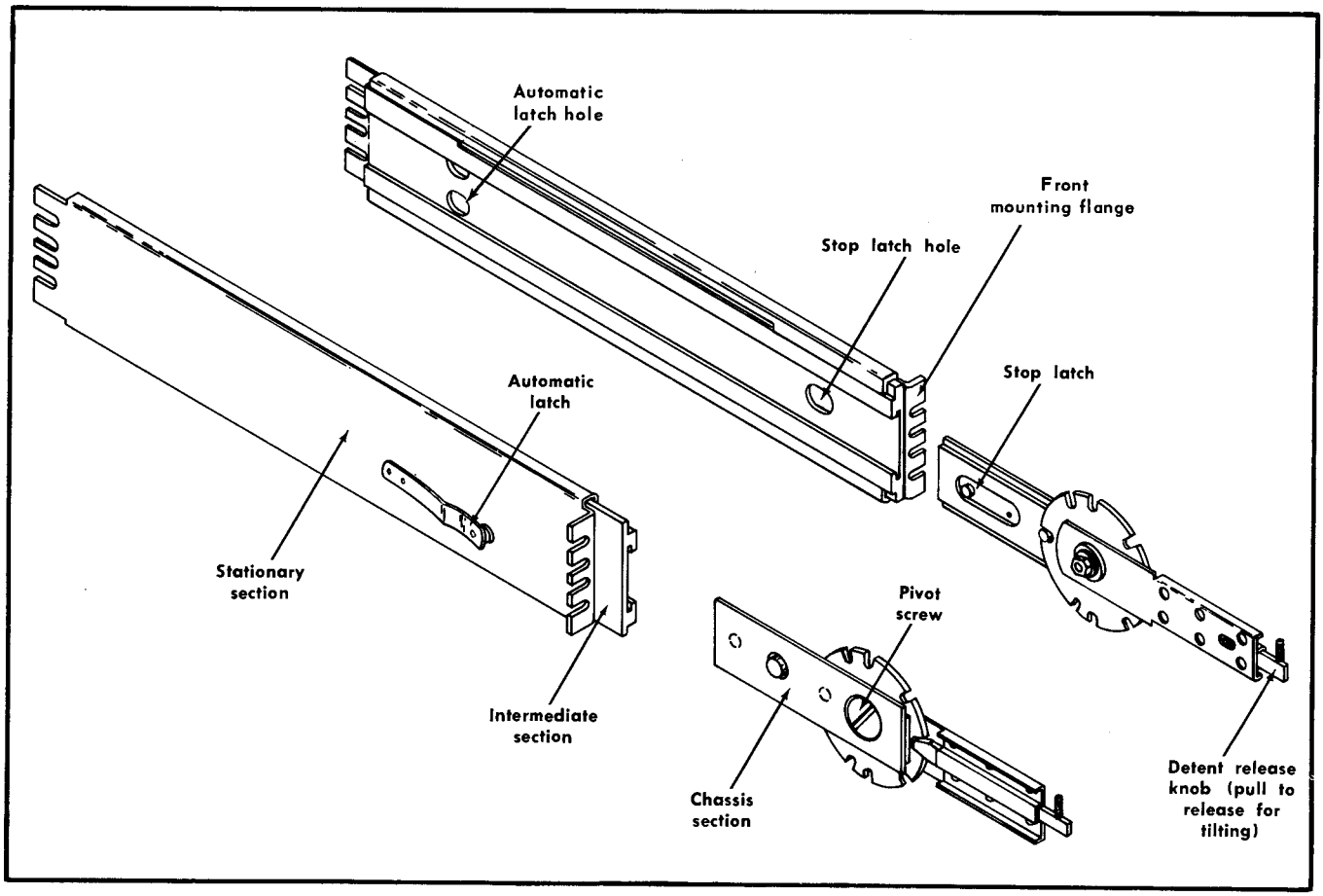


Fig. 8-2. Slideout track assemblies.

These factors will usually determine whether the front mounting flanges of the stationary sections are to be mounted in front of the rails or behind them, whether or not the ruggedizing rear-support hardware is to be used, etc.

Different lengths of slide-out tracks (Fig. 8-2) have been shipped with different Serial Numbers of Type 230's. These are as follows:

NOTE

These Serial Number ranges are provided as a general guide, but do not apply to all instruments. The primary criteria to be used for mounting purposes are the actual lengths of the slide-out track sections supplied with the instrument. Hereafter, these three combinations will be referred to as "Group A", "Group B" and "Group C".

Front-End Mounting with Tapped Front Rails. If the mounting holes in the front rails of the rack are tapped for 10-32 screws, the easiest method of attaching the front ends of the stationary sections to the rack is to mount the front flanges in front of the front rails (see Fig. 8-6A and B). When mounted in this position, 10-32 pan-head screws may be used directly to attach the front flanges to the rails, or 10-32 flat-head screws may be used with countersunk shim material to clamp the front flanges to the rails. The use of countersunk shim material provides better support for the front flanges and also permits depth adjustment of the front panel. If the various instruments in the rack have different panel thicknesses, different thicknesses of shim material can be used to make the front surfaces of all panels flush with each other. The shim material should be approximately 1/2-inch wide and have a minimum thickness of approximately 1/8 inch to accommodate the countersunk screw heads. Each strip should be at least as long (vertical dimension in the rack) as the width of the front flanges of the stationary sections (3 1/8 inches). Since the dimensions of the shim material are determined entirely by the dimensions of the rack installation, no shim material is provided with the mounting hardware.

NOTE

When the flanges are mounted in front of the front rails or when shim material exceeding 1/8-inch in thickness is used, special adjustment of the ruggedizing rear-mount hardware may be required (see Standard Rear-End Mounting below).

Front-End Mounting with Untapped Front Rails. If the mounting holes in the front rails are not tapped, bar nuts (Fig. 8-3) must be used behind the rails to accommodate the mounting screws. All of the options previously described for tapped front rails also apply to the untapped rails when used with bar nuts. In addition, the untapped front rails (with bar nuts) permit the front mounting flanges to be attached to the rear sides of the front rails (see Fig. 8-6C). When mounted in this position, the flanges are clamped between the bar nuts and the front rails. Either 10-32 pan-head screws or 10-32 flat-head screws with shim

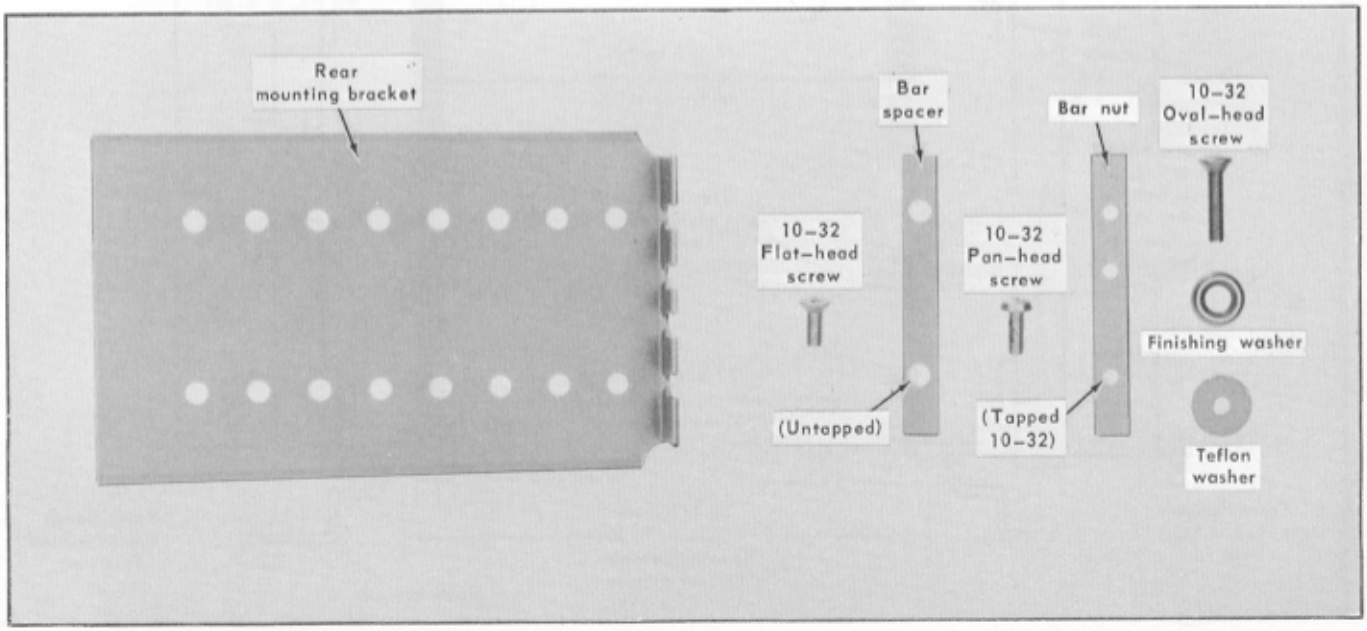


Fig. 8-3. Identification of mounting hardware provided with the Type R230. (Shim material described in the text is not provided.)

material may be used as described for tapped front rails, or 10-32 flat-head mounting screws may be countersunk into the front rails.

Standard Rear-End Mounting. To provide an adequate shock-mounted installation, the rear end of each stationary section must be mounted firmly to a rear-support rail using the ruggedizing hardware. If the rack does not have a strong supporting member located the correct distance from the front rails (Fig. 8-4), an additional support must be provided. The instrument will not meet the environmental specifications unless firmly supported at this point. Use the 10-32 round-head screws provided in the ruggedizing kit (see Fig. 8-7) to mount the rear bar supports to the rear rails, and use 10-32 pan-head screws to attach the stationary sections of the tracks to the bar supports. If the mounting holes in the rear rails are not tapped, bar nuts must also be used for mounting the bar supports. For instruments equipped with 20-inch stationary sections (Group B), an additional rear mounting bracket (Fig. 8-3) is required between each stationary section and the rear mount.

NOTE

If the front flanges of the stationary sections are mounted in front of the front rails, or if more than 1/8-inch of shim thickness is used for mounting the front flanges, or if the support rails are located at fixed positions such that the distance from the front surface of the front rail to the rear surface of the rear rail is slightly greater than 21 inches, additional washers and possibly longer support-pin and/or securing bushing screws (Fig. 8-7) may be needed to make the ruggedizing support fit securely. No more than about 1/2 inch of washer thickness can be added to each rear-support mounting without deteriorating the ruggedizing capability of the installation.

Non-Ruggedizing Rear-End Mounting. If the rear support rails cannot be positioned so that the distance from the front surface of the front rails to the rear surface of the rear rails is between 21 and 21 1/2 inches, the rear-mount ruggedizing hardware cannot be used. Also, if the particular installation does not require a high degree of physical rigidity, the use of ruggedizing hardware may be omitted. In either of these cases, an alternative method of supporting the rear ends of the stationary sections is required. Fig. 8-11 illustrates two alternative mounting methods using the rear-mounting brackets and not the ruggedizing hardware. The depth between the front and rear rails of the rack will determine which of these configurations should be used.

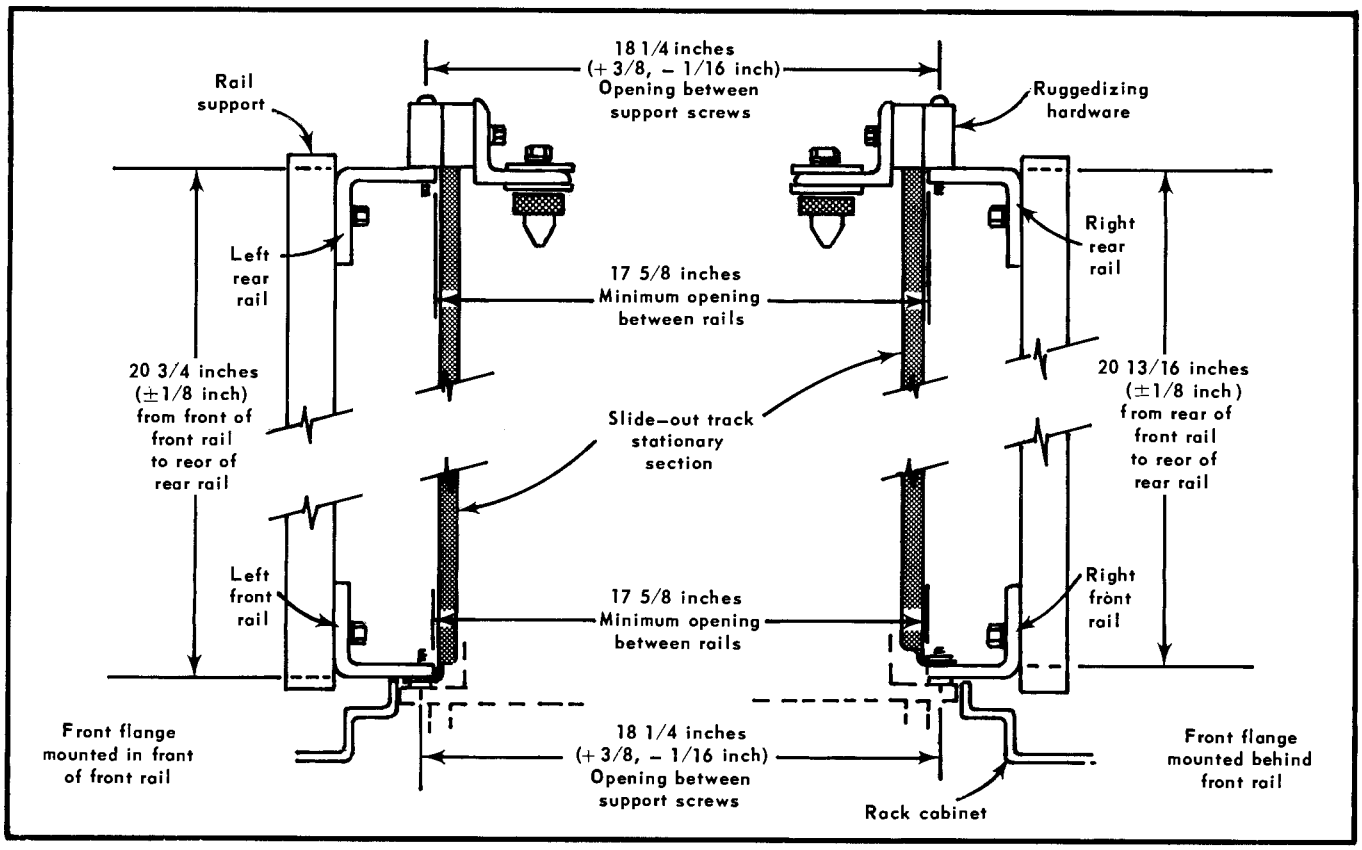


Fig. 8-4. Required spacing of support rails for mounting stationary sections of slide-out tracks.

CAUTION

Although the alternative mounting methods shown in Fig. 8-11 provide adequate support under normal operating conditions, they do not provide the solid rear-mount support required to meet the environmental specifications of the instrument. If mounted without the ruggedizing hardware, the instrument may be damaged by severe vibration or shock.

Rack Dimensions

Fig. 8-4 shows the maximum and minimum dimensions required between support rails to provide adequate support for the Type R230 and proper operation of the slide-out tracks. Minimum overall depth of the rack from the front surface of the front rails must be at least 22 1/2 inches to accommodate the rear-mount ruggedizing hardware, power cord and interconnecting cables, and to provide enough space for air circulation. (If 20-inch stationary sections are used with rear mounting brackets, the overall rack depth must be at least 23 1/8 inches.)

Mounting Procedure

The following mounting and alignment procedures use the rear-support ruggedizing hardware for attaching the rear end of each stationary section to the rear support rail. If the ruggedizing hardware is not to be utilized, refer to the procedure exceptions given under Non-Ruggedized Mounting which follows the Alignment Procedure.

The stationary and intermediate sections of the slide-out tracks are shipped as matched pairs and should not be separated. To distinguish between the right and left stationary/intermediate assemblies, note the position of the automatic latch (see Fig. 8-2) in each assembly. The automatic latch should be located near the bottom of the assembly when it is installed in the rack.

Use the following procedure to install the stationary sections of the slide-out tracks and the Type 230 in the rack:

1. Referring to Fig. 8-5, select the proper front-rail mounting holes for the stationary sections.

2a. If the front flanges of the stationary sections are to be mounted in front of the front rails, mount the front of each stationary section as shown in Fig. 8-6A or B.

2b. If the front flanges are to be mounted behind the front rails, mount the front end of each stationary section as shown in Fig. 8-6C.

3. With the front end of each stationary section attached to the front rail, hold the track in a level position in the rack and locate the proper rear-rail mounting holes for the ruggedizing hardware (see Fig. 8-9).

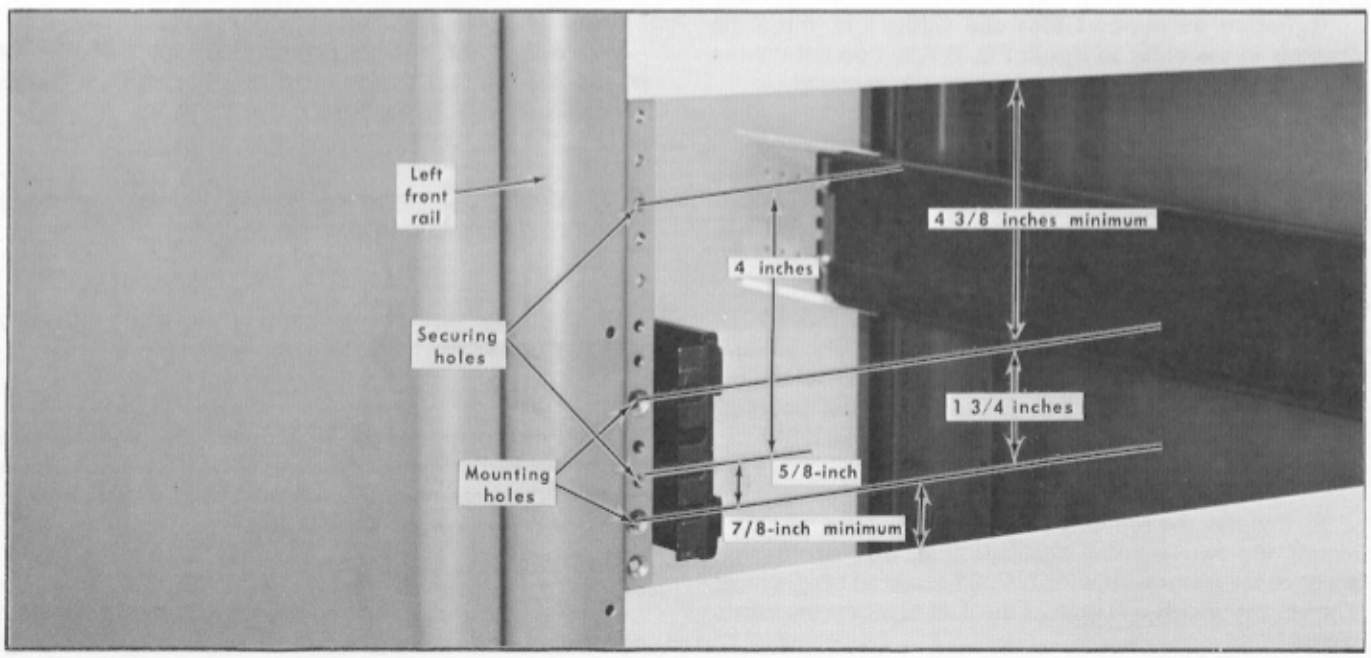


Fig. 8-5. Vertical mounting position for front end of slide-out tracks. Left stationary section (only) is shown.

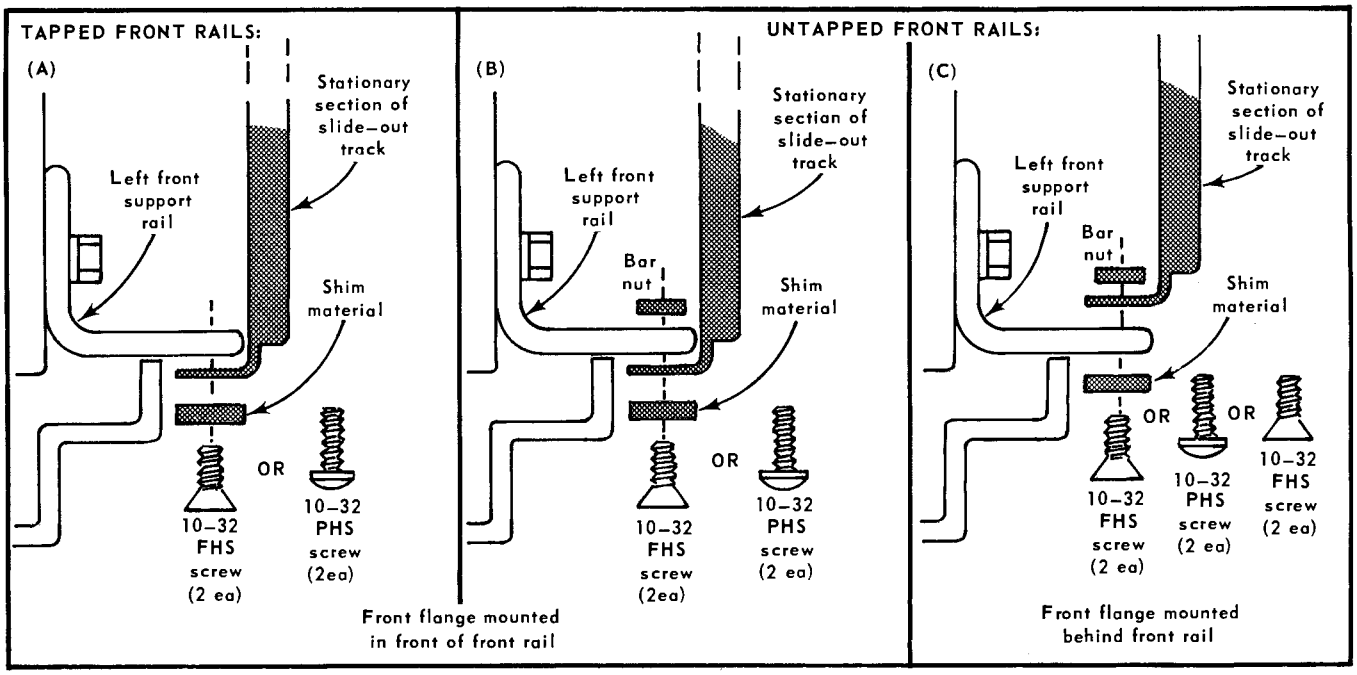


Fig. 8-6. Methods for mounting front end of stationary sections as described in the text. Thickness of optional shim material is selected to compensate for differences in front-panel thickness of various instruments in rack. (Shim material is not provided with hardware.)

4. Attach the bar supports (Fig. 8-7) to the rear support rails with the 10-32 round-head screws, using at least two mounting screws for each bar support.

5. Mount the angle brackets and spacer blocks on the bar supports as shown in Fig. 8-7, but do not tighten the screws.

6. Fasten the support pins and washers to the angle brackets in the order shown in Fig. 8-7, but do not tighten the screws. Be sure the spacers are properly centered.

7a. If the instrument has 22-inch stationary sections (Group A or C), attach the rear end of each stationary section to the correspoinding bar support using at least two 10-32 pan-head screws and a bar spacer.

7b. If the instrument has 20-inch stationary sections (Group B), attach each rear mounting bracket to the bar support with two pan-head screws and fasten the mounting bracket to the stationary section as shown in Fig. 8-8.

8. Remove the top dust cover from the Type R230 and mount the two securing bushings (Fig. 8-7) on the rear panel of the instrument with 1/4-20 hexagonal-head screws. Tighten the screws and replace the dust cover on the instrument.

9. Referring to Fig. 8-12, insert the instrument into the rack. Do not connect the power cord or interconnecting cables and do not install the securing screws.

Alignment Procedure

Use the following procedure to adjust the instrument alignment in the rack:

1. Position the instrument approximately half-way out of the rack so that the point of rotation on each chassis section is adjacent to the front rail of the rack.

2. Loosen the mounting screws holding the front mounting flanges to the front rails.

3. Hold the instrument in the center of its mounting space and re-tighten the front mounting screws.

4. Push the instrument all the way into the rack and check the vertical and horizontal alignment of the front panel of the instrument. If necessary, readjust the positioning as described in steps 2 and 3.

5. Push the instrument all the way into the rack again and install one securing screw on each side of the front

panel using a finishing washer and teflon washer with each securing screw as shown in Fig. 8-12. If the front rails are not tapped for the 10-32 securing screws, some other means of securing the instrument into the rack must be provided.

NOTE

If the instrument does not slide all the way into the rack easily, check the fit of the rear-support ruggedizing hardware before installing the securing screws. If necessary, move the inside support-pin washer to the outside of the angle bracket (Fig. 8-7).

6. Press each securing bushing over the support pin and check alignment of the ruggedizing hardware.

7a. If the securing bushings and support pins fit tightly, with the neoprene washers seated against the securing bushings, hold each angle bracket firmly in place and tighten the angle-bracket screws and the support-pin screw. Fig. 8-10 shows the completed installation of the left rear support.

7b. If the securing bushing and support pin do not fit tightly together, determine what adjustment is necessary; i.e., whether one or more additional washers are required for a tight fit, etc. Remove the securing screws, extend the instrument part way out of the rack and make the necessary changes in the ruggedizing hardware, then repeat steps 5, 6 and 7a.

8. Secure the front panel of the Type R230 to the front rails of the rack with the four securing screws (Fig. 8-12).

NOTE

The securing screws are an important part of the shock-mounted installation.

9. After all adjustments have been made and all hardware has been tightened securely, connect the power cord to a suitable power source and connect the program cables to the proper connectors on the rear panel of the instrument.

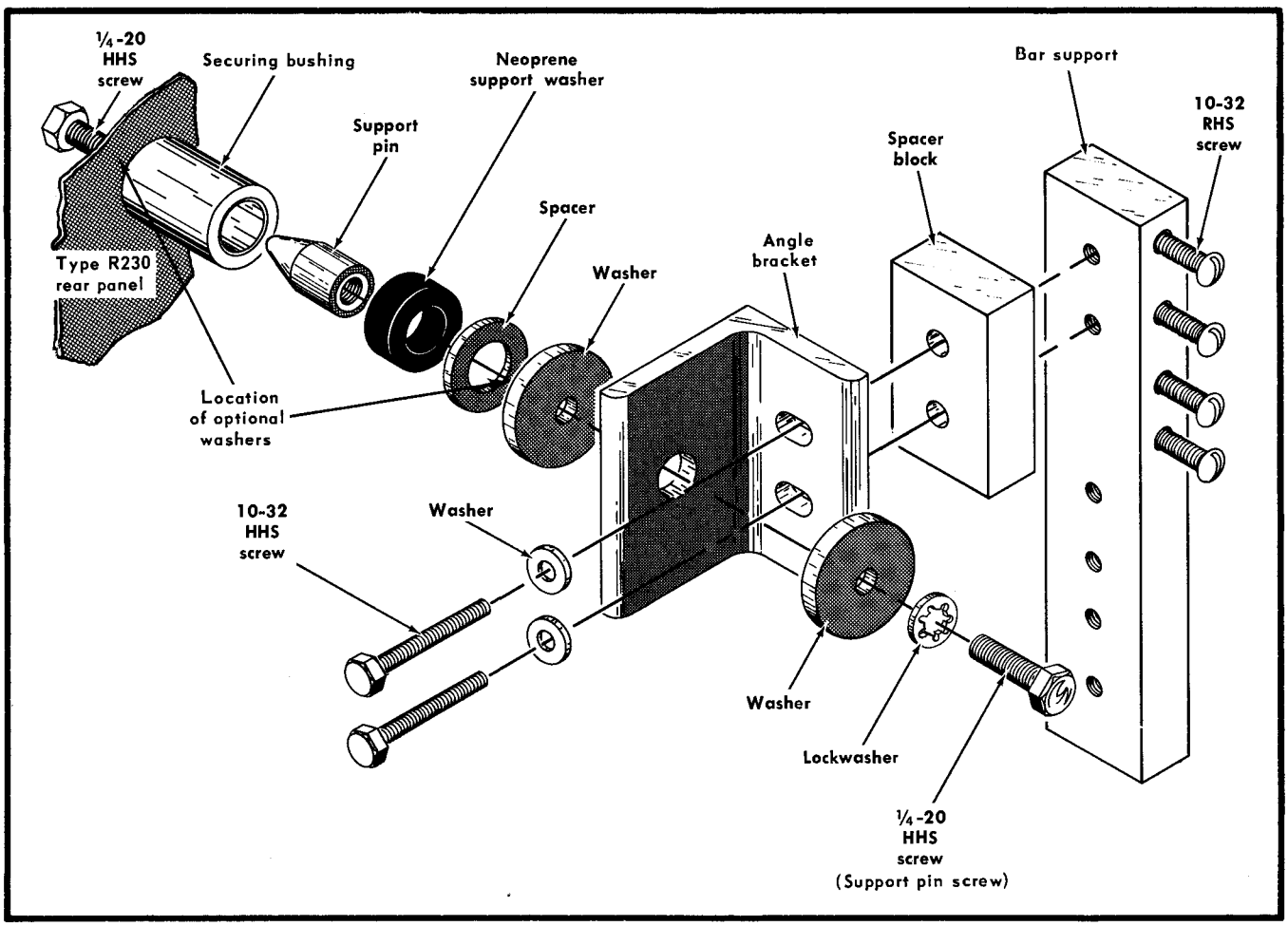


Fig. 8-7. Rear-support ruggedizing hardware. Optional washers (Tektronix Part Number 210-0866-00) are for depth adjustment, if required, as described in the text. Optional washers are not provided with the mounting hardware.

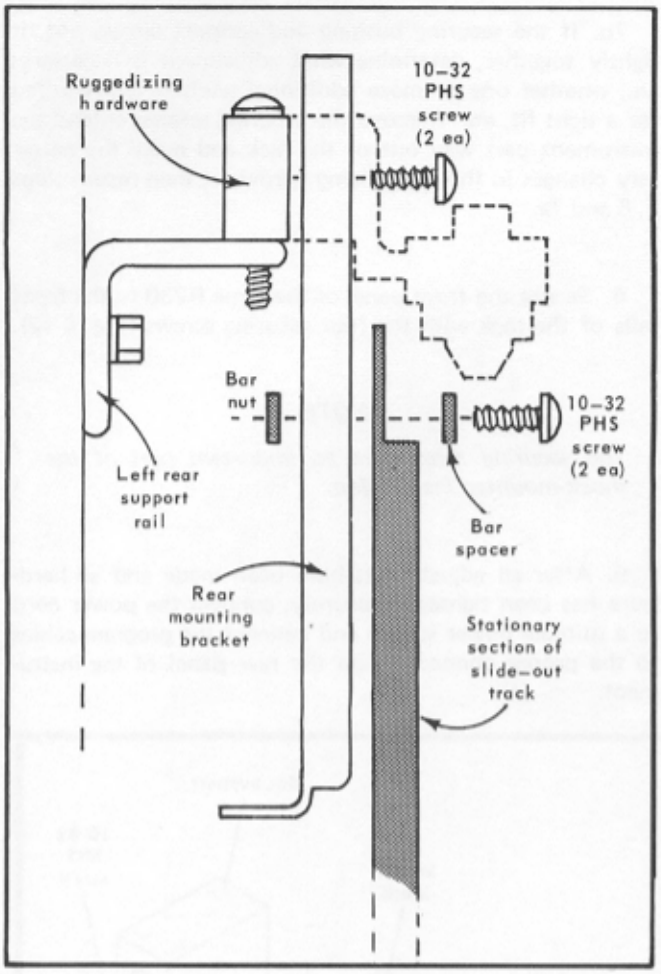


Fig. 8-8. Method of mounting rear end of 20-inch stationary section (Group B only).

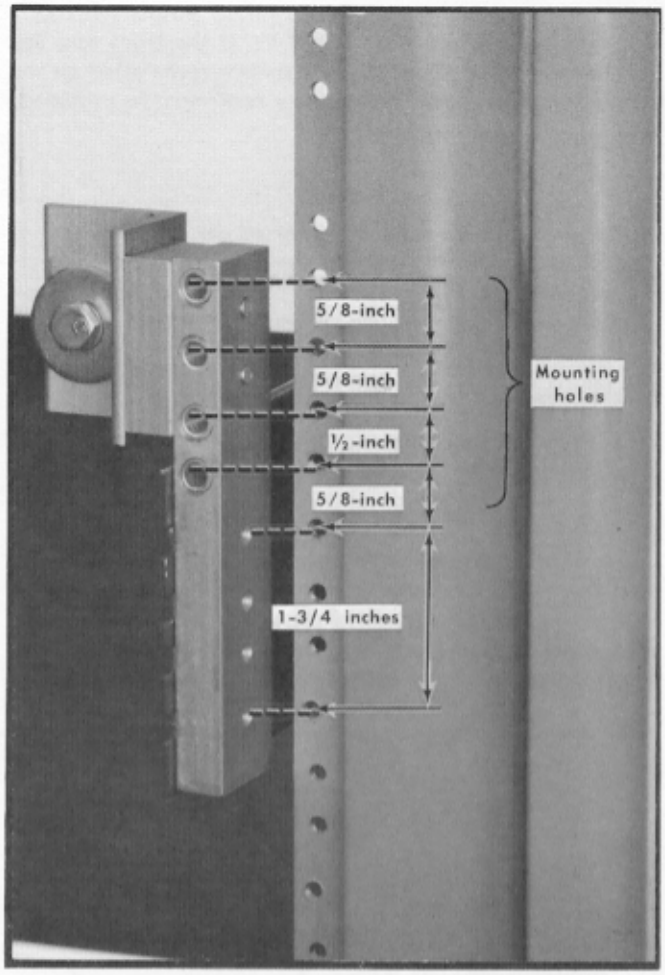


Fig. 8-9. Vertical mounting position for rear end of slide-out tracks. Left stationary section (only) is shown.

Non-Ruggedized Mounting

If the ruggedizing hardware is not to be used, refer to Fig. 8-11 for mounting the rear end of each stationary section and use the standard Mounting and Alignment procedures as a guide. Omit the steps that apply only to the ruggedizing hardware and substitute the following steps for the corresponding steps given in the procedures:

Mounting Procedure step 4. Attach the rear support brackets to the rear support rails as shown in Fig. 8-11 and tighten the screws securely.

Adjustment Procedure 6. Loosen the screws that hold the rear support brackets to the support rails and allow the rear ends of the stationary sections to seek their normal positions. Tighten the rear mounting bracket screws while holding up on the rear of the instrument so that the weight is removed from the brackets.

Slide-Out Track Lubrication

The special finish on the sliding surfaces of the slide-out tracks provides permanent lubrication. However, if the tracks do not slide smoothly even after being properly adjusted, a thin coating of paraffin may be rubbed onto the sliding surfaces for additional lubrication.

Removal and Re-insertion

After the initial installation and adjustment of the slide-out tracks, the Type 230 may be removed or re-inserted in the rack by following the instructions given in Fig. 8-12. Under normal circumstances, no further adjustments are required.

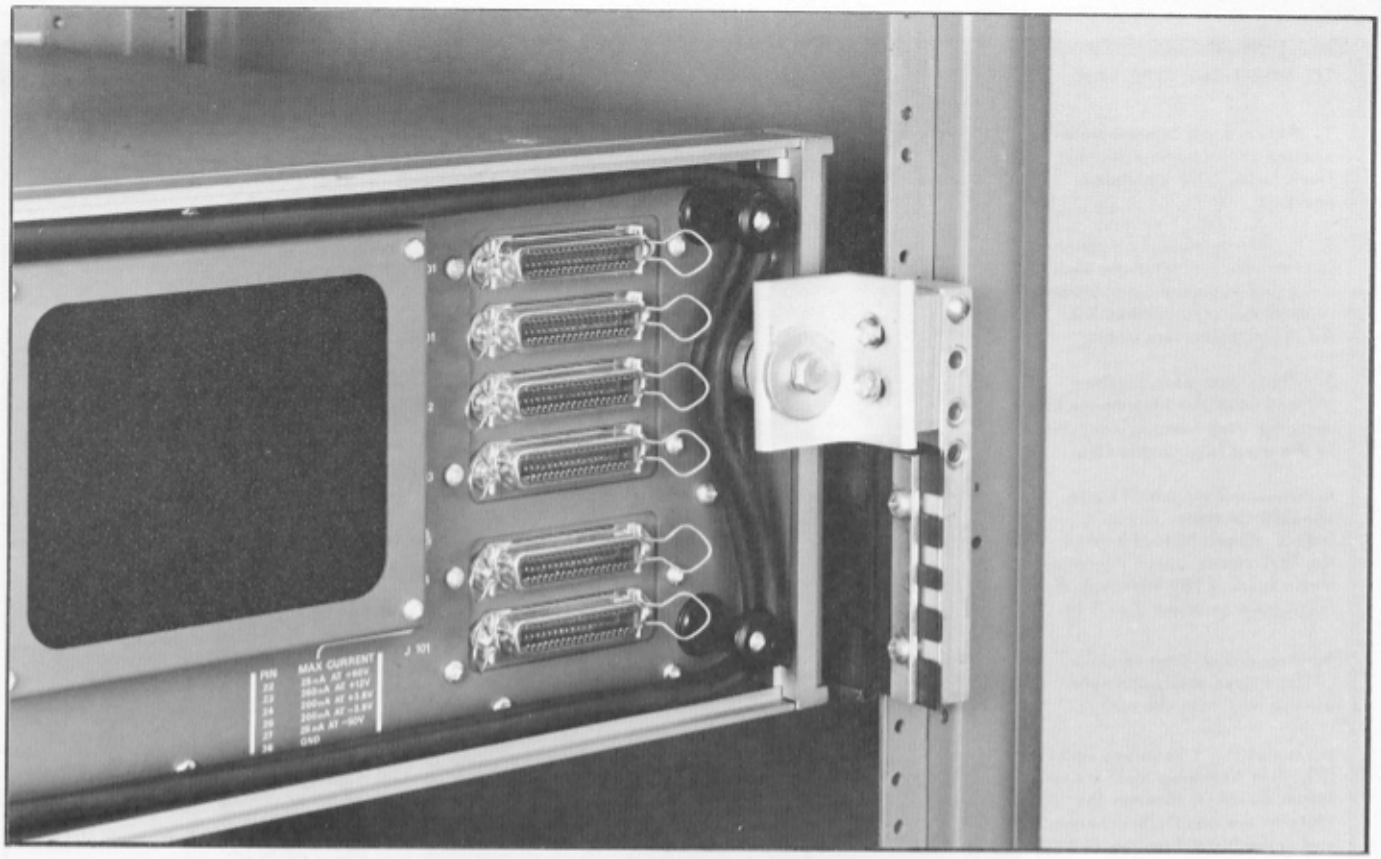


Fig. 8-10. Completed installation of left rear support. Mounting with 22-inch stationary section (Groups A and C) is shown.

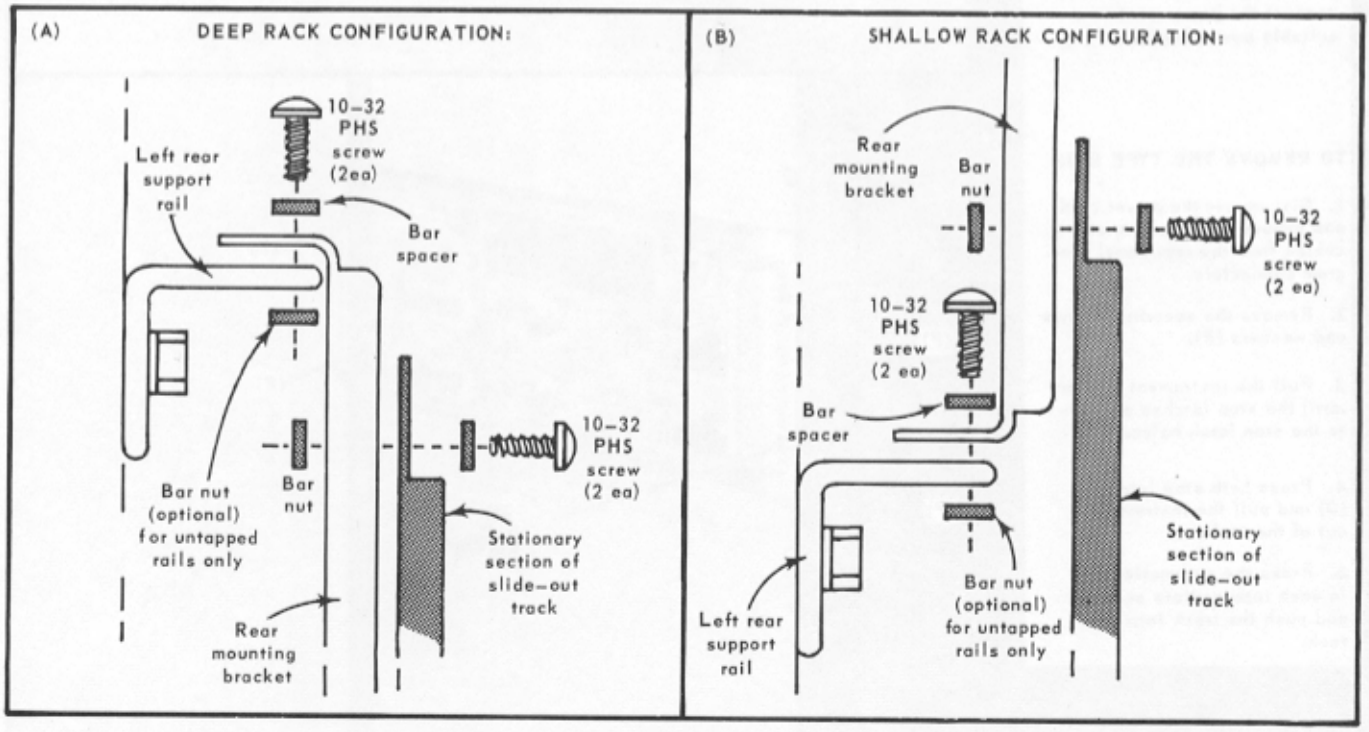


Fig. 8-11. Non-ruggedized mounting: (A) For use with 20-inch stationary sections or racks deeper than 21 inches from the front of the front rail to the rear of the rear rail; (B) For use with racks shallower than 21 inches.

TO INSERT THE TYPE R230

1. Pull out the intermediate section (A) of each slide-out track to its fully extended position.

2. Insert the chassis sections (B) into the intermediate sections and push the instrument in until the stop latches hit the intermediate sections.

3. Press both stop latches (C) and push the instrument in until the stop latches snap into the stop latch holes (D).

4. (Instruments with 11¾-in. chassis sections, Group A only): Reach in just behind the instrument, press the automatic latches (E) and push the instrument in about 2 or 3 in.

5. Press both stop latches (D) and push the instrument all the way into the rack.

6. Insert the 4 securing screws (F), with finishing washers and teflon washers, through the slots in the handle brackets and screw them into the front rails of the rack.

7. Connect the proper interconnecting cables to the rear-panel program connectors and connect the power cord to a suitable power source.

TO REMOVE THE TYPE R230

1. Disconnect the power cord and remove the interconnecting cables from the rear-panel program connectors.

2. Remove the securing screws and washers (F).

3. Pull the instrument outward until the stop latches snap into the stop latch holes.

4. Press both stop latches (D) and pull the instrument out of the rack.

5. Press the automatic latch in each intermediate section and push the track into the rack.

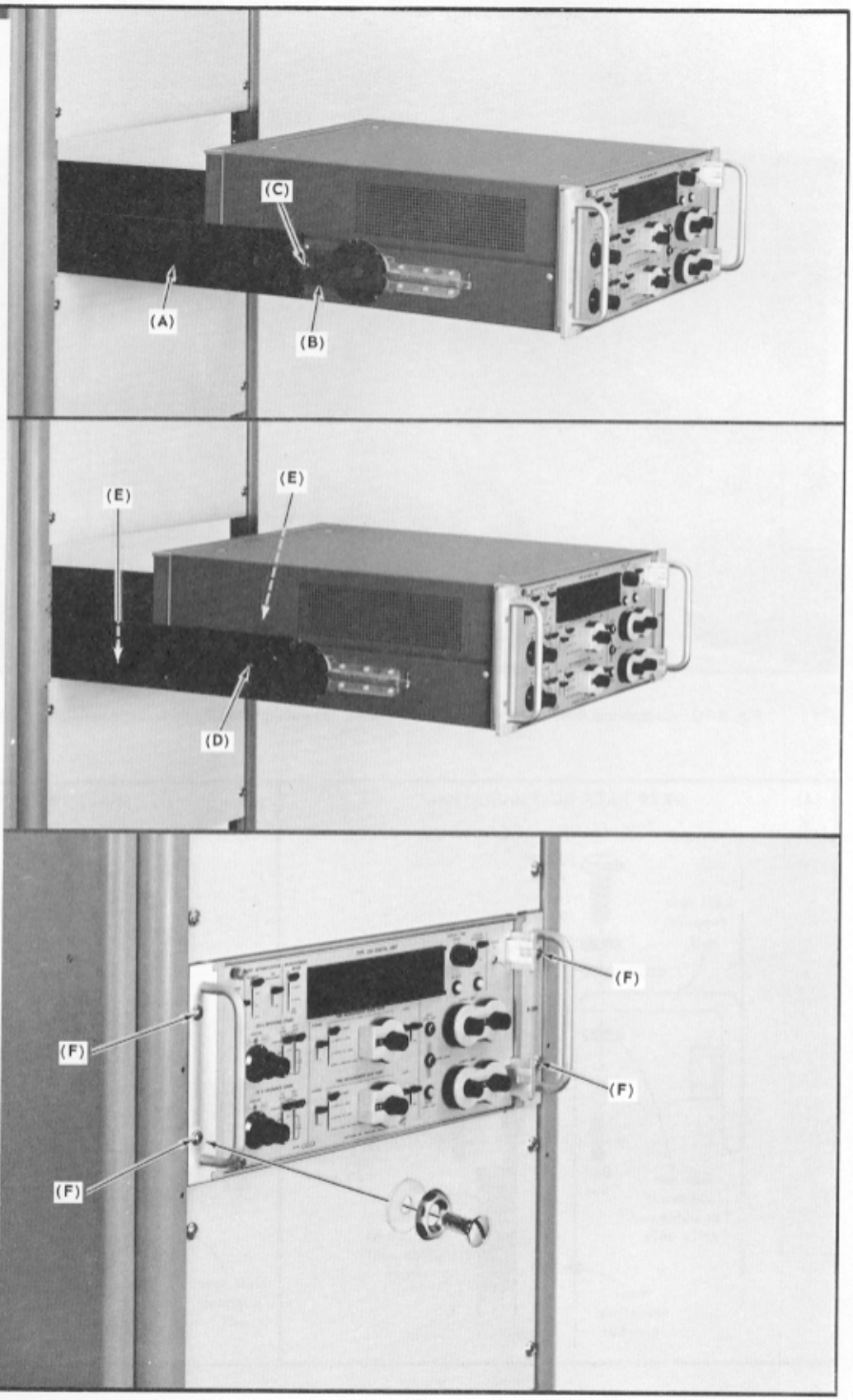
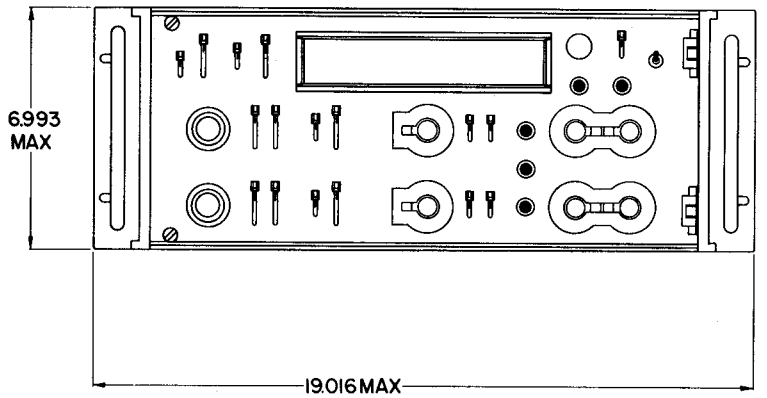
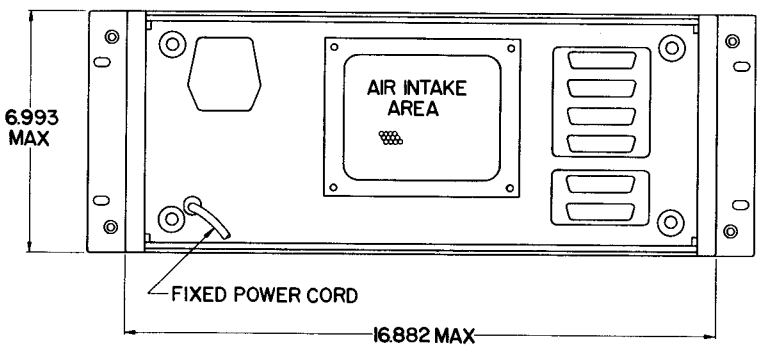


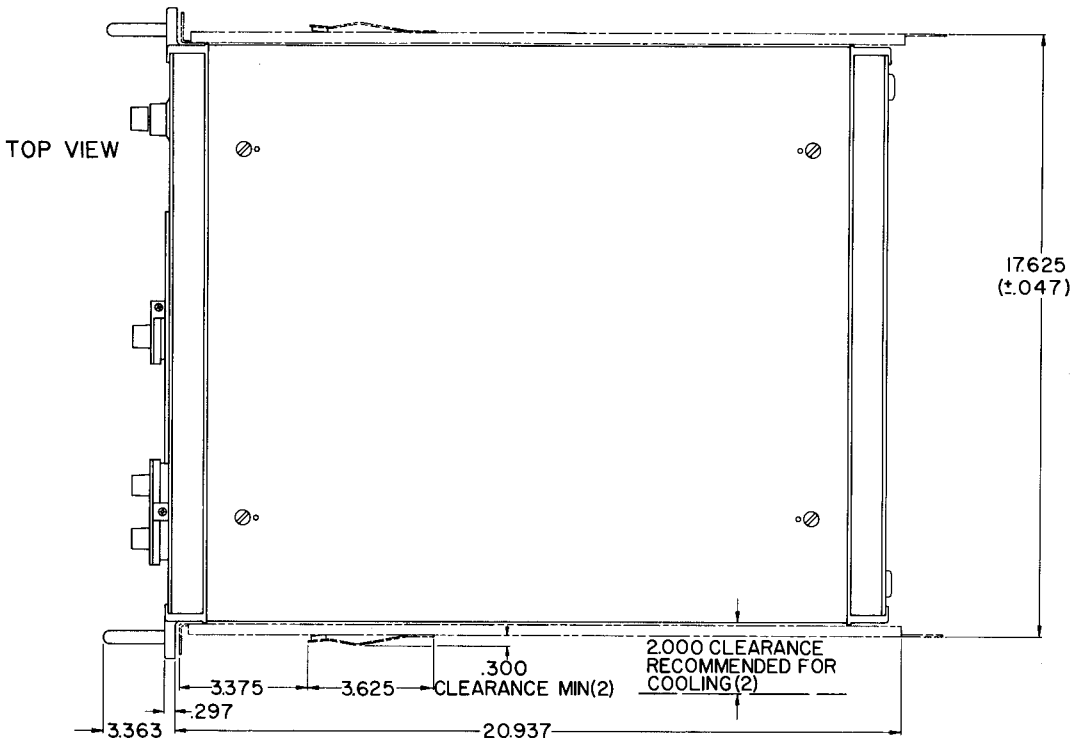
Fig. 8-12. Insertion and removal of the Type R230 after the slide-out tracks have been installed.

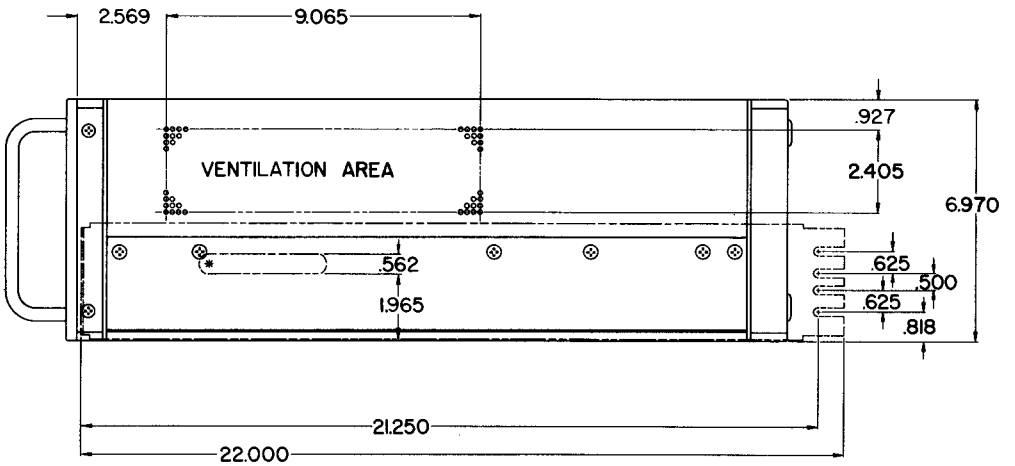


FRONT VIEW

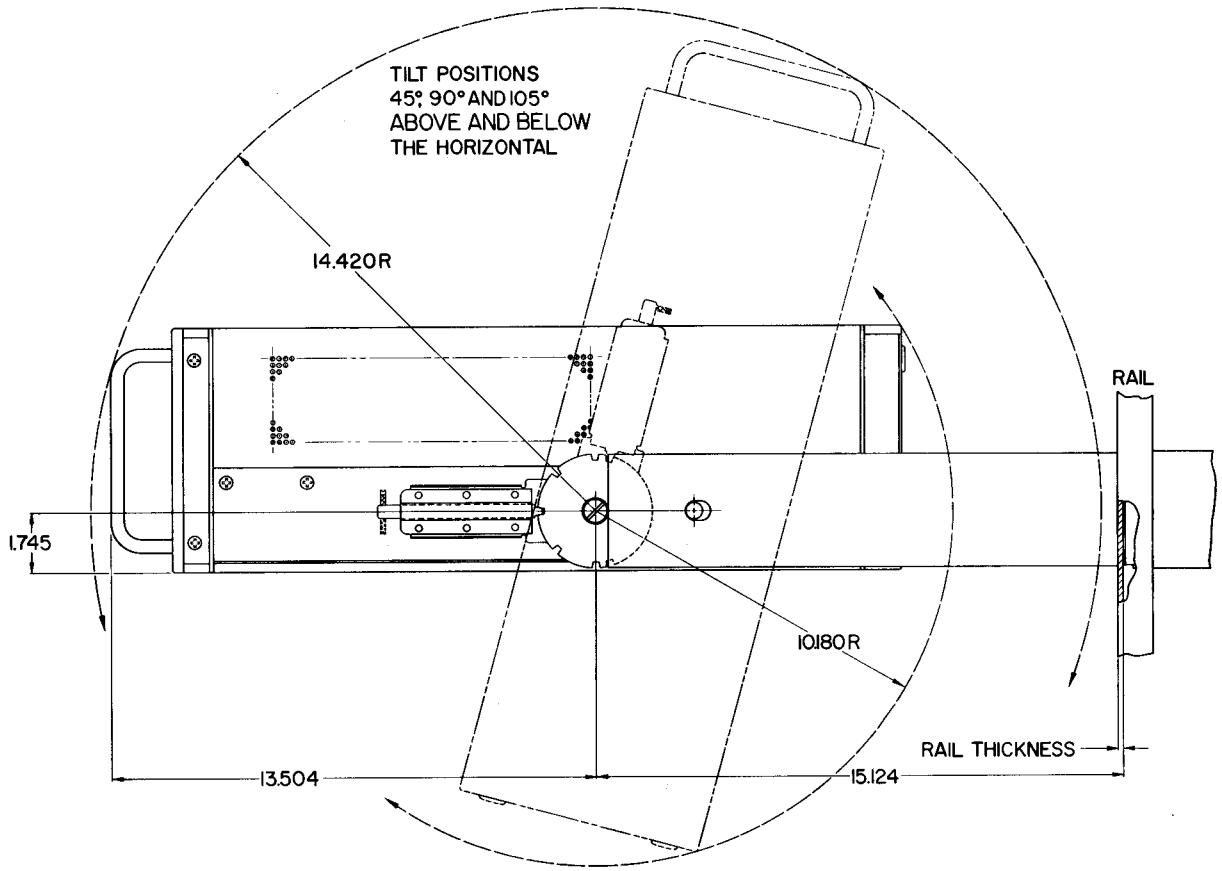


REAR VIEW


TOP VIEW
17.625
(±.047)
.300
CLEARANCE MIN(2)
2.000 CLEARANCE
RECOMMENDED FOR
COOLING(2)
3.375
3.625
.297
3.363
20.937


2.569
9.065
.927
VENTILATION AREA
2.405
6.970
.562
1.965
.625
.500
.625
.818
21.250
22.000

SIDE VIEW


TILT POSITIONS
45°, 90° AND 105°
ABOVE AND BELOW
THE HORIZONTAL
14.420R
RAIL
1.745
10.180R
RAIL THICKNESS
13.504
15.124

NOTES

PARTS LIST ABBREVIATIONS

BHB	binding head brass
BHS	binding head steel
cap.	capacitor
cer	ceramic
comp	composition
conn	connector
CRT	cathode-ray tube
csk	countersunk
DE	double end
dia	diameter
div	division
elect.	electrolytic
EMC	electrolytic, metal cased
EMT	electrolytic, metal tubular
ext	external
F & I	focus and intensity
FHB	flat head brass
FHS	flat head steel
Fil HB	fillister head brass
Fil HS	fillister head steel
h	height or high
hex.	hexagonal
HHB	hex head brass
HHS	hex head steel
HSB	hex socket brass
HSS	hex socket steel
ID	inside diameter
incd	incandescent
int	internal
lg	length or long
met.	metal
mtg hdw	mounting hardware
OD	outside diameter
OHB	oval head brass
OHS	oval head steel
PHB	pan head brass
PHS	pan head steel
plstc	plastic
PMC	paper, metal cased
poly	polystyrene
prec	precision
PT	paper, tubular
PTM	paper or plastic, tubular, molded
RHB	round head brass
RHS	round head steel
SE	single end
SN or S/N	serial number
SW	switch
TC	temperature compensated
THB	truss head brass
thk	thick
THS	truss head steel
tub.	tubular
var	variable
w	wide or width
WW	wire-wound

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial or model number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

SPECIAL NOTES AND SYMBOLS

×000	Part first added at this serial number
00×	Part removed after this serial number
*000-0000-00	Asterisk preceding Tektronix Part Number indicates manufactured by or for Tektronix, Inc., or reworked or checked components.
Use 000-0000-00	Part number indicated is direct replacement.
◐	Screwdriver adjustment.
▭	Control, adjustment or connector.

INDEX OF ELECTRICAL PARTS LIST

SECTION 9
ELECTRICAL PARTS LIST

Values are fixed unless marked Variable.

CHASSIS AND COUNTER BOARD

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
				Bulbs			
B501	150-0043-00			Incandescent, Assembly			
B502	150-0043-00			Incandescent, Assembly			
B510	150-0066-00			Incandescent, Red Lens			
B511	150-0065-00			Incandescent, Green Lens			
B512	150-0064-00			Incandescent, Amber Lens			
B515	150-0050-00			Neon, NE-2H			
B516	150-0050-00			Neon, NE-2H			
B517	150-0050-00			Neon, NE-2H			
B518	150-0050-00			Neon, NE-2H			
B519	150-0050-00			Neon, NE-2H			
B2341	150-0021-00			Neon, NE-76			
				Capacitors			
Tolerance ±20% unless otherwise indicated.							
C212A,B	290-0007-00			2 x 15 μF	Elect.	450 V	
C222	290-0322-00			550 μF	Elect.	100 V	+75%—10%
C249	290-0273-00			68 μF	Elect.	60 V	10%
C253	290-0320-00			4500 μF	Elect.	40 V	+100%—10%
C279	290-0296-00			100 μF	Elect.	20 V	
C283	290-0321-00			11000 μF	Elect.	15 V	+100%—10%
C284	290-0321-00			11000 μF	Elect.	15 V	+100%—10%
C309	290-0138-00			330 μF	Elect.	6 V	
C329	290-0138-00			330 μF	Elect.	6 V	
C349	290-0138-00			330 μF	Elect.	6 V	
C389	290-0273-00			68 μF	Elect.	60 V	10%
C452	290-0322-00			550 μF	Elect.	100 V	+75%—10%
C2320	290-0263-00			2.7 μF	Elect.	15 V	
C2501	283-0065-00			0.001 μF	Cer	100 V	5%
C2505	283-0010-00	B010100	B179999	0.05 μF	Cer	50 V	
C2505	283-0167-00	B180000		0.1 μF	Cer	100 V	10%
C2541	290-0136-00			2.2 μF	Elect.	20 V	
C2542	290-0136-00			2.2 μF	Elect.	20 V	
C2543	290-0136-00			2.2 μF	Elect.	20 V	

CHASSIS AND COUNTER BOARD (cont)

Diodes

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
D212	*152-0107-00			Silicon	Replaceable by 1N647
D222	152-0199-00			Rectifier Bridge	MDA 962-3 (Motorola)
D252	152-0198-00			Silicon	MR1032A (Motorola)
D253	152-0198-00			Silicon	MR1032A (Motorola)
D282	152-0198-00			Silicon	MR1032A (Motorola)
D283	152-0198-00			Silicon	MR1032A (Motorola)
D284	152-0198-00			Silicon	MR1032A (Motorola)
D285	152-0198-00			Silicon	MR1032A (Motorola)
D328	152-0066-00			Silicon	1N3194
D452	152-0199-00			Rectifier Bridge	MDA 962-3 (Motorola)
D521	*152-0185-00			Silicon	Replaceable by 1N4152
D522	*152-0185-00			Silicon	Replaceable by 1N4152
D524	*152-0185-00			Silicon	Replaceable by 1N4152
D525	*152-0185-00			Silicon	Replaceable by 1N4152
D531	*152-0185-00			Silicon	Replaceable by 1N4152
D532	*152-0185-00			Silicon	Replaceable by 1N4152
D533	*152-0185-00			Silicon	Replaceable by 1N4152
D534	*152-0185-00			Silicon	Replaceable by 1N4152
D536	*152-0185-00			Silicon	Replaceable by 1N4152
D537	*152-0185-00			Silicon	Replaceable by 1N4152
D538	*152-0185-00			Silicon	Replaceable by 1N4152
D539	*152-0185-00			Silicon	Replaceable by 1N4152
D541	*152-0185-00			Silicon	Replaceable by 1N4152
D542	*152-0185-00			Silicon	Replaceable by 1N4152
D543	*152-0185-00			Silicon	Replaceable by 1N4152
D544	*152-0185-00			Silicon	Replaceable by 1N4152
D546	*152-0185-00			Silicon	Replaceable by 1N4152
D547	*152-0185-00			Silicon	Replaceable by 1N4152
D548	*152-0185-00			Silicon	Replaceable by 1N4152
D551	*152-0185-00			Silicon	Replaceable by 1N4152
D552	*152-0185-00			Silicon	Replaceable by 1N4152
D553	*152-0185-00			Silicon	Replaceable by 1N4152
D554	*152-0185-00			Silicon	Replaceable by 1N4152
D556	*152-0185-00			Silicon	Replaceable by 1N4152
D557	*152-0185-00			Silicon	Replaceable by 1N4152
D558	*152-0185-00			Silicon	Replaceable by 1N4152
D559	*152-0185-00			Silicon	Replaceable by 1N4152
D561	*152-0185-00			Silicon	Replaceable by 1N4152
D562	*152-0185-00			Silicon	Replaceable by 1N4152
D563	*152-0185-00			Silicon	Replaceable by 1N4152
D564	*152-0185-00			Silicon	Replaceable by 1N4152
D566	*152-0185-00			Silicon	Replaceable by 1N4152
D567	*152-0185-00			Silicon	Replaceable by 1N4152
D568	*152-0185-00			Silicon	Replaceable by 1N4152
D2312	*152-0185-00			Silicon	Replaceable by 1N4152
D2316	*152-0185-00	B010100	B169999	Silicon	Replaceable by 1N4152
D2316	*152-0322-00	B170000		Silicon	Tek Spec
D2342	*152-0107-00			Silicon	Replaceable by 1N647

CHASSIS AND COUNTER BOARD (cont)

Diodes *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
D2432	*152-0107-00			Silicon Replaceable by 1N647
D2434	*152-0107-00			Silicon Replaceable by 1N647
D2435	*152-0107-00			Silicon Replaceable by 1N647
D2436	*152-0107-00			Silicon Replaceable by 1N647
D2437	*152-0107-00			Silicon Replaceable by 1N647
D2438	*152-0107-00			Silicon Replaceable by 1N647
D2441	*152-0185-00			Silicon Replaceable by 1N4152
D2442	*152-0185-00			Silicon Replaceable by 1N4152
D2444	*152-0185-00			Silicon Replaceable by 1N4152
D2447	*152-0185-00			Silicon Replaceable by 1N4152
D2455	*152-0107-00			Silicon Replaceable by 1N647
D2456	*152-0107-00			Silicon Replaceable by 1N647
D2457	*152-0107-00			Silicon Replaceable by 1N647
D2458	*152-0107-00			Silicon Replaceable by 1N647
D2459	*152-0185-00			Silicon Replaceable by 1N4152
D2464	*152-0185-00			Silicon Replaceable by 1N4152
D2480	*152-0185-00			Silicon Replaceable by 1N4152
D2482	*152-0107-00			Silicon Replaceable by 1N647
D2484	*152-0107-00			Silicon Replaceable by 1N647
D2486	*152-0107-00			Silicon Replaceable by 1N647
D2488	*152-0107-00			Silicon Replaceable by 1N647

Fuses

F201	159-0034-00			1.6 A 3AG Slo-Blo
F202	159-0018-00			0.8 A 3AG Slo-Blo

Connectors

J1	131-0292-01			56 pin contact
J2	131-0292-01			56 pin contact
J3	131-0292-01			56 pin contact
J4	131-0292-01			56 pin contact
J5	131-0292-01			56 pin contact
J6	131-0292-01			56 pin contact
J7	131-0292-01			56 pin contact
J8	131-0292-01			56 pin contact
J9	131-0292-01			56 pin contact
J10	131-0292-01			56 pin contact
J11	131-0292-01			56 pin contact
J101	131-0294-00	B010100	B129999	36 pin contact
J101	131-0294-01	B130000		36 pin contact
J201	131-0294-00	B010100	B129999	36 pin contact
J201	131-0294-06	B130000		36 pin contact
J202	131-0294-00	B010100	B129999	36 pin contact
J202	131-0294-06	B130000		36 pin contact
J203	131-0294-00	B010100	B129999	36 pin contact
J203	131-0294-06	B130000		36 pin contact
J204	131-0294-00	B010100	B129999	36 pin contact
J204	131-0294-05	B130000		36 pin contact
J301	131-0294-00	B010100	B129999	36 pin contact
J301	131-0294-06	B130000		36 pin contact

CHASSIS AND COUNTER BOARD (cont)

Integrated Circuits

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
M2310	156-0010-00			Buffer-Inverter	Replaceable by Fairchild μL900
M2320	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2322	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2324	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2326	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2328	156-0010-00			Buffer-Inverter	Replaceable by Fairchild μL900
M2330	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2332	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2334	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2336	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2338	156-0001-00			Decimal Decoder-Driver	Replaceable by Fairchild CμL960
M2348	156-0010-00			Buffer-Inverter	Replaceable by Fairchild μL900
M2350	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2352	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2354	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2356	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2358	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M2370	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2372	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2374	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2376	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2378	156-0001-00			Decimal Decoder-Driver	Replaceable by Fairchild CμL960
M2380	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2382	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2384	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2386	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2388	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M2390	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2392	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2394	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2396	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2398	156-0001-00			Decimal Decoder-Driver	Replaceable by Fairchild CμL960
M2400	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2402	156-0010-00			Buffer-Inverter	Replaceable by Fairchild μL900
M2404	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2406	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2408	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2430	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2432	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2440	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2444	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2448	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923

CHASSIS AND COUNTER BOARD (cont)

Integrated Circuits (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
M2450	156-0001-00			Decimal Decoder-Driver	Replaceable by Fairchild CμL960
M2460	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2464	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2468	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2470	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2474	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2502	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M2512	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2522	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M2532	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914

Transistors

Q247	*151-0140-00			Silicon	Selected from 2N3055
Q277	*151-0140-00			Silicon	Selected from 2N3055
Q307	*151-0140-00			Silicon	Selected from 2N3055
Q327	*151-0140-00			Silicon	Selected from 2N3055
Q347	*151-0140-00			Silicon	Selected from 2N3055
Q487	*151-0140-00			Silicon	Selected from 2N3055
Q2315	151-0190-00	B010100	B119999	Silicon	2N3904
Q2315	*151-0190-01	B120000		Silicon	Tek Spec
Q2331	151-0190-00	B010100	B119999	Silicon	2N3904
Q2331	*151-0190-01	B120000		Silicon	Tek Spec
Q2333	151-0190-00	B010100	B119999	Silicon	2N3904
Q2333	*151-0190-01	B120000		Silicon	Tek Spec
Q2335	151-0190-00	B010100	B119999	Silicon	2N3904
Q2335	*151-0190-01	B120000		Silicon	Tek Spec
Q2337	151-0190-00	B010100	B119999	Silicon	2N3904
Q2337	*151-0190-01	B120000		Silicon	Tek Spec
Q2343	151-0150-00			Silicon	2N3440
Q2371	151-0190-00	B010100	B119999	Silicon	2N3904
Q2371	*151-0190-01	B120000		Silicon	Tek Spec
Q2373	151-0190-00	B010100	B119999	Silicon	2N3904
Q2373	*151-0190-01	B120000		Silicon	Tek Spec
Q2375	151-0190-00	B010100	B119999	Silicon	2N3904
Q2375	*151-0190-01	B120000		Silicon	Tek Spec
Q2377	151-0190-00	B010100	B119999	Silicon	2N3904
Q2377	*151-0190-01	B120000		Silicon	Tek Spec
Q2391	151-0190-00	B010100	B119999	Silicon	2N3904
Q2391	*151-0190-01	B120000		Silicon	Tek Spec
Q2393	151-0190-00	B010100	B119999	Silicon	2N3904
Q2393	*151-0190-01	B120000		Silicon	Tek Spec
Q2395	151-0190-00	B010100	B119999	Silicon	2N3904
Q2395	*151-0190-01	B120000		Silicon	Tek Spec
Q2397	151-0190-00	B010100	B119999	Silicon	2N3904

CHASSIS AND COUNTER BOARD (cont)

Transistors (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
Q2397	*151-0190-01	B120000		Silicon Tek Spec
Q2407	151-0190-00	B010100	B119999	Silicon 2N3904
Q2407	*151-0190-01	B120000		Silicon Tek Spec
Q2409	151-0190-00	B010100	B119999	Silicon 2N3904
Q2409	*151-0190-01	B120000		Silicon Tek Spec
Q2421	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2421	151-0272-00	B190000		Silicon Dual
Q2423	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2423	151-0272-00	B190000		Silicon Dual
Q2425	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2425	151-0272-00	B190000		Silicon Dual
Q2427	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2427	151-0272-00	B190000		Silicon Dual
Q2431	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2431	151-0272-00	B190000		Silicon Dual
Q2433	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2433	151-0272-00	B190000		Silicon Dual
Q2481	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2481	151-0272-00	B190000		Silicon Dual
Q2483	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2483	151-0272-00	B190000		Silicon Dual
Q2485	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2485	151-0272-00	B190000		Silicon Dual
Q2487	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2487	151-0272-00	B190000		Silicon Dual
Q2489	151-0179-00	B010100	B189999	Silicon 2N3877A
Q2489	151-0272-00	B190000		Silicon Dual
Q2513	151-0190-00	B010100	B119999	Silicon 2N3904
Q2513	151-0207-00	B120000		Silicon 2N3415
Q2523	151-0190-00	B010100	B119999	Silicon 2N3904
Q2523	151-0207-00	B120000		Silicon 2N3415
Q2533	151-0190-00	B010100	B119999	Silicon 2N3904
Q2533	151-0207-00	B120000		Silicon 2N3415

Resistors

Resistors are fixed, composition, ±10% unless otherwise indicated.

R211	316-0100-00			10 Ω	¼ W		
R212	315-0271-00			270 Ω	¼ W		5%
R213	317-0201-00	B010100	B149999X	200 Ω	⅛ W		5%
R215	302-0184-00			180 kΩ	½ W		
R221	307-0093-00			1.2 Ω	½ W		5%
R222	301-0273-00			27 kΩ	½ W		5%
R246	302-0181-00			180 Ω	½ W		
R247	*308-0141-00			1 Ω	½ W	WW	5%
R251	*308-0090-00			0.25 Ω	1 W	WW	
R252	*308-0090-00			0.25 Ω	1 W	WW	

CHASSIS AND COUNTER BOARD (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R253	302-0562-00			5.6 kΩ	½ W	
R274	302-0181-00			180 Ω	½ W	
R276	308-0245-00			0.6 Ω	2 W	WW 5%
R277	308-0244-00			0.3 Ω	0.2 W	WW
R281	*308-0090-00			0.25 Ω	1 W	WW
R282	*308-0090-00			0.25 Ω	1 W	WW
R283	301-0202-00			2 kΩ	½ W	5%
R284	301-0202-00			2 kΩ	½ W	5%
R304	302-0181-00			180 Ω	½ W	
R307	*308-0090-00	B010100	B189999	0.25 Ω	1 W	WW
R307	308-0590-00	B190000		0.25 Ω	3 W	WW 5%
R326	308-0441-00			3 Ω	3 W	WW 5%
R327	308-0245-00			0.6 Ω	2 W	WW 5%
R346	302-0181-00			180 Ω	½ W	
R347	*308-0087-00			0.5 Ω	1 W	WW 1%
R451	307-0093-00			1.2 Ω	½ W	5%
R452	301-0273-00			27 kΩ	½ W	5%
R486	302-0181-00			180 Ω	½ W	
R487	*308-0141-00			1 Ω	½ W	WW 5%
R505	311-0673-00			5 MΩ, Var		
R510	301-0390-00			39 Ω	½ W	5%
R512	301-0390-00			39 Ω	½ W	5%
R515	315-0471-00			470 Ω	¼ W	5%
R516	315-0471-00			470 Ω	¼ W	5%
R518	315-0471-00			470 Ω	¼ W	5%
R519	315-0471-00			470 Ω	¼ W	5%
R2312	315-0333-00			33 kΩ	¼ W	5%
R2313	315-0243-00			24 kΩ	¼ W	5%
R2314	315-0473-00			47 kΩ	¼ W	5%
R2316	315-0472-00			4.7 kΩ	¼ W	5%
R2318	315-0472-00			4.7 kΩ	¼ W	5%
R2326	315-0332-00	B010100	B059999	3.3 kΩ	¼ W	5%
R2326	315-0102-00	B060000		1 kΩ	¼ W	5%
R2328	315-0202-00	B010100	B059999	2 kΩ	¼ W	5%
R2328	315-0332-00	B060000		3.3 kΩ	¼ W	5%
R2331	315-0272-00			2.7 kΩ	¼ W	5%
R2333	315-0272-00			2.7 kΩ	¼ W	5%
R2335	315-0272-00			2.7 kΩ	¼ W	5%
R2337	315-0272-00			2.7 kΩ	¼ W	5%
R2339	301-0363-00			36 kΩ	½ W	5%
R2341	315-0104-00	B010100	B149999	100 kΩ	¼ W	5%
R2341	315-0393-00	B150000		39 kΩ	¼ W	5%
R2342	315-0106-00			10 MΩ	¼ W	5%
R2343	305-0242-00	B010100	B149999	2.4 kΩ	2 W	5%
R2343	301-0101-00	B150000		100 Ω	½ W	5%
R2371	315-0272-00			2.7 kΩ	¼ W	5%
R2373	315-0272-00			2.7 kΩ	¼ W	5%
R2375	315-0272-00			2.7 kΩ	¼ W	5%
R2377	315-0272-00			2.7 kΩ	¼ W	5%

CHASSIS AND COUNTER BOARD (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R2379	301-0303-00			30 kΩ	½ W	5%
R2391	315-0272-00			2.7 kΩ	¼ W	5%
R2393	315-0272-00			2.7 kΩ	¼ W	5%
R2395	315-0272-00			2.7 kΩ	¼ W	5%
R2397	315-0272-00			2.7 kΩ	¼ W	5%
R2399	301-0303-00			30 kΩ	½ W	5%
R2407	315-0272-00			2.7 kΩ	¼ W	5%
R2409	315-0272-00			2.7 kΩ	¼ W	5%
R2421	315-0272-00			2.7 kΩ	¼ W	5%
R2423	315-0272-00			2.7 kΩ	¼ W	5%
R2429	301-0303-00			30 kΩ	½ W	5%
R2431	315-0272-00			2.7 kΩ	¼ W	5%
R2433	315-0272-00			2.7 kΩ	¼ W	5%
R2434	315-0242-00			2.4 kΩ	¼ W	5%
R2435	315-0154-00	B010100	B149999	150 kΩ	¼ W	5%
R2435	315-0753-00	B150000		75 kΩ	¼ W	5%
R2436	315-0154-00	B010100	B149999	150 kΩ	¼ W	5%
R2436	315-0753-00	B150000		75 kΩ	¼ W	5%
R2437	315-0513-00	B010100	B149999	51 kΩ	¼ W	5%
R2437	315-0273-00	B150000		27 kΩ	¼ W	5%
R2438	315-0623-00	B010100	B149999	62 kΩ	¼ W	5%
R2438	315-0393-00	B150000		39 kΩ	⅛ W	5%
R2441	315-0113-00			11 kΩ	¼ W	5%
R2442	315-0912-00			9.1 kΩ	¼ W	5%
R2443	315-0133-00			13 kΩ	¼ W	5%
R2444	315-0113-00			11 kΩ	¼ W	5%
R2445	315-0912-00			9.1 kΩ	¼ W	5%
R2446	315-0133-00			13 kΩ	¼ W	5%
R2447	315-0113-00			11 kΩ	¼ W	5%
R2448	315-0912-00			9.1 kΩ	¼ W	5%
R2449	315-0133-00			13 kΩ	¼ W	5%
R2450	315-0753-00			75 kΩ	¼ W	5%
R2451	315-0622-00			6.2 kΩ	¼ W	5%
R2452	315-0472-00			4.7 kΩ	¼ W	5%
R2456	315-0124-00			120 kΩ	¼ W	5%
R2457	315-0124-00			120 kΩ	¼ W	5%
R2459	315-0124-00			120 kΩ	¼ W	5%
R2461	315-0113-00			11 kΩ	¼ W	5%
R2462	315-0912-00			9.1 kΩ	¼ W	5%
R2463	315-0133-00			13 kΩ	¼ W	5%
R2464	315-0113-00			11 kΩ	¼ W	5%
R2465	315-0912-00			9.1 kΩ	¼ W	5%
R2466	315-0133-00			13 kΩ	¼ W	5%
R2467	315-0113-00			11 kΩ	¼ W	5%
R2468	315-0912-00			9.1 kΩ	¼ W	5%
R2469	315-0133-00			13 kΩ	¼ W	5%
R2471	315-0113-00			11 kΩ	¼ W	5%
R2472	315-0912-00			9.1 kΩ	¼ W	5%

CHASSIS AND COUNTER BOARD (cont)

Capacitors (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R2473	315-0133-00			13 kΩ	1/4 W	5%
R2474	315-0113-00			11 kΩ	1/4 W	5%
R2475	315-0912-00			9.1 kΩ	1/4 W	5%
R2476	315-0133-00			13 kΩ	1/4 W	5%
R2480	315-0242-00			2.4 kΩ	1/4 W	5%
R2481	315-0272-00			2.7 kΩ	1/4 W	5%
R2482	315-0242-00			2.4 kΩ	1/4 W	5%
R2483	315-0272-00			2.7 kΩ	1/4 W	5%
R2484	315-0242-00			2.4 kΩ	1/4 W	5%
R2485	315-0272-00			2.7 kΩ	1/4 W	5%
R2486	315-0242-00			2.4 kΩ	1/4 W	5%
R2487	315-0272-00			2.7 kΩ	1/4 W	5%
R2488	315-0242-00			2.4 kΩ	1/4 W	5%
R2489	315-0272-00			2.7 kΩ	1/4 W	5%
R2491	315-0623-00	B010100	B149999	62 kΩ	1/4 W	5%
R2491	315-0393-00	B150000		39 kΩ	1/4 W	5%
R2493	315-0623-00	B010100	B149999	62 kΩ	1/4 W	5%
R2493	315-0393-00	B150000		39 kΩ	1/4 W	5%
R2495	315-0623-00	B010100	B149999	62 kΩ	1/4 W	5%
R2495	315-0393-00	B150000		39 kΩ	1/4 W	5%
R2497	315-0623-00	B010100	B149999	62 kΩ	1/4 W	5%
R2497	315-0393-00	B150000		39 kΩ	1/4 W	5%
R2499	315-0623-00	B010100	B149999	62 kΩ	1/4 W	5%
R2499	315-0393-00	B150000		39 kΩ	1/4 W	5%
R2501	315-0222-00			2.2 kΩ	1/4 W	5%
R2505	315-0103-00			10 kΩ	1/4 W	5%
R2511	315-0102-00			1 kΩ	1/4 W	5%
R2513	315-0471-00	B010100	B119999	470 Ω	1/4 W	5%
R2513	315-0151-00	B120000		150 Ω	1/4 W	5%
R2515	315-0911-00			910 Ω	1/4 W	5%
R2521	315-0102-00			1 kΩ	1/4 W	5%
R2523	315-0471-00	B010100	B119999	470 Ω	1/4 W	5%
R2523	315-0151-00	B120000		150 Ω	1/4 W	5%
R2527	315-0911-00			910 Ω	1/4 W	5%
R2533	315-0471-00			470 Ω	1/4 W	5%
R2537	315-0911-00			910 Ω	1/4 W	5%

Switches

	Unwired or Wired	Tektronix Part No.	Serial/Model No. Eff	Disc		
SW201		260-0834-00	B010100	B139999	Toggle	POWER
SW201		260-0276-00	B140000		Toggle	POWER
SW500		260-0473-00			Lever	MEASUREMENT AVERAGING
SW502		260-0473-00			Lever	TRIGGER MEASUREMENT
SW506		260-0849-00			Lever	REF ZONES
SW509		260-0473-00			Lever	TIME MEASUREMENT
SW520		260-0847-00			Lever	MEASUREMENT MODE
SW522		260-0723-00			Slide	CAL RUN
SW530A	wired	*262-0807-00			Rotary	LOWER LIMIT (TENS)
SW530B		260-0844-00				LOWER LIMIT (UNITS)
SW540A	wired	*262-0808-00			Rotary	LOWER LIMIT (HUNDREDS)
SW504B		260-0845-00				LOWER LIMIT (THOUSANDS)

CHASSIS AND COUNTER BOARD (cont)

Switches (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
SW550A	wired *262-0807-00		Rotary	UPPER LIMIT (TENS)
SW550B	260-0844-00			UPPER LIMIT (UNITS)
SW560A	wired *262-0808-00		Rotary	UPPER LIMIT (HUNDREDS)
SW560B	260-0845-00			UPPER LIMIT (THOUSANDS)
SW570A	260-0846-00		Rotary	CH A 0% POSITION
SW570B				CH A 100% POSITION
SW571	260-0849-00		Lever	CH A 0% LEVEL
SW572	260-0849-00		Lever	CH A 100% LEVEL
SW575	260-0848-00		Lever	LEVEL START
SW576	260-0473-00		Lever	SLOPE START
SW577	260-0473-00		Lever	SLOPE START
SW579A	260-0844-00		Rotary	START LEVEL (UNITS)
SW579B				START LEVEL (TENS)
SW580A	260-0846-00		Rotary	CH B 0% POSITION
SW580B				CH B 100% POSITION
SW581	260-0849-00		Lever	CH B 0% LEVEL
SW582	260-0849-00		Lever	CH B 100% LEVEL
SW585	260-0848-00		Lever	LEVEL STOP
SW586	260-0473-00		Lever	SLOPE STOP
SW587	260-0473-00		Lever	SLOPE STOP
SW589A	260-0844-00		Rotary	STOP LEVEL (UNITS)
SW589B				STOP LEVEL (TENS)
SW590	260-0473-00		Lever	CHANNEL START
SW591	260-0473-00		Lever	CHANNEL STOP

Thermal Cutout

TK201	260-0413-00		175°F ±5°F

Test Point

TP2502	*214-0579-00	Pin, Test Point

Transformer

T201	*120-0480-00	Power

Electron Tubes

V2339	154-0327-00	B5092 (Numbers)
V2379	154-0327-00	B5092 (Numbers)
V2399	154-0327-00	B5092 (Numbers)
V2429	154-0327-00	B5092 (Numbers)
V2439	154-0509-00	B5971 (Alpha Numeric)
V2499	154-0326-00	B5094 (Units)

ZONE GENERATOR CARDS (2) Series A

	*670-0231-00	Complete Card

Capacitors

Tolerance ±20% unless otherwise indicated.

C807	281-0651-00	47 pF	Cer		5%
C809	281-0509-00	15 pF	Cer	500 V	10%
C819	290-0136-00	2.2 μF	Elect.	20 V	
C823	281-0651-00	47 pF	Cer		5%
C825	281-0523-00	100 pF	Cer	350 V	

ZONE GENERATOR CARDS (2) Series A (cont)

Capacitors (Cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Description		
C907	281-0651-00			47 pF	Cer	5%
C909	281-0509-00			15 pF	Cer 500 V	10%
C919	290-0136-00			2.2 μF	Elect. 20 V	
C923	281-0651-00			47 pF	Cer	5%
C925	281-0523-00			100 pF	Cer 350 V	

Diodes

D811	*152-0185-00			Silicon	Replaceable by 1N4152
D817	*152-0185-00			Silicon	Replaceable by 1N4152
D831	*152-0185-00			Silicon	Replaceable by 1N4152
D832	*152-0185-00			Silicon	Replaceable by 1N4152
D841	*152-0185-00			Silicon	Replaceable by 1N4152
D851	*152-0185-00			Silicon	Replaceable by 1N4152
D855	*152-0185-00			Silicon	Replaceable by 1N4152
D861	*152-0185-00			Silicon	Replaceable by 1N4152
D871	*152-0185-00			Silicon	Replaceable by 1N4152
D875	*152-0185-00			Silicon	Replaceable by 1N4152
D881	*152-0185-00			Silicon	Replaceable by 1N4152
D884	*152-0185-00	X3		Silicon	Replaceable by 1N4152
D891	*152-0185-00			Silicon	Replaceable by 1N4152
R894	*152-0185-00	X3		Silicon	Replaceable by 1N4152
D911	*152-0185-00			Silicon	Replaceable by 1N4152
D917	*152-0185-00			Silicon	Replaceable by 1N4152
D931	*152-0185-00			Silicon	Replaceable by 1N4152
D932	*152-0185-00			Silicon	Replaceable by 1N4152
D941	*152-0185-00			Silicon	Replaceable by 1N4152
D951	*152-0185-00			Silicon	Replaceable by 1N4152
D955	*152-0185-00			Silicon	Replaceable by 1N4152
D961	*152-0185-00			Silicon	Replaceable by 1N4152
D971	*152-0185-00			Silicon	Replaceable by 1N4152
D975	*152-0185-00			Silicon	Replaceable by 1N4152
D981	*152-0185-00			Silicon	Replaceable by 1N4152
D984	*152-0185-00	X3		Silicon	Replaceable by 1N4152
D991	*152-0185-00			Silicon	Replaceable by 1N4152
D994	*152-0185-00	X3		Silicon	Replaceable by 1N4152

Integrated Circuits

M838	156-0003-00			3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M938	156-0003-00			3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G

Transistors

Q807	151-0190-00	1		Silicon	2N3904
Q807	*151-0190-01	2		Silicon	Tek Spec
Q814	151-0188-00	1		Silicon	2N3906
Q814	151-0220-00	2		Silicon	2N4122
Q817	151-0190-00	1		Silicon	2N3904

ZONE GENERATOR CARDS (2) Series A (cont)

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
Q817	*151-0190-01	2	Silicon	Tek Spec
Q819	151-0190-00	1	Silicon	2N3904
Q819	*151-0190-01	2	Silicon	Tek Spec
Q823	151-0190-00	1	Silicon	2N3904
Q823	*151-0190-01	2	Silicon	Tek Spec
Q827	151-0190-00	1	Silicon	2N3904
Q827	*151-0190-01	2	Silicon	Tek Spec
Q829	151-0190-00	1	Silicon	2N3904
Q829	*151-0190-01	2	Silicon	Tek Spec
Q833	151-0190-00	1	Silicon	2N3904
Q833	*151-0190-01	2	Silicon	Tek Spec
Q844	151-0188-00	1	Silicon	2N3906
Q844	151-0220-00	2	Silicon	2N4122
Q854	151-0188-00	1	Silicon	2N3906
Q854	151-0220-00	2	Silicon	2N4122
Q856	151-0188-00	1	Silicon	2N3906
Q856	151-0220-00	2	Silicon	2N4122
Q864	151-0188-00	1	Silicon	2N3906
Q864	151-0220-00	2	Silicon	2N4122
Q874	151-0188-00	1	Silicon	2N3906
Q874	151-0220-00	2	Silicon	2N4122
Q876	151-0188-00	1	Silicon	2N3906
Q876	151-0220-00	2	Silicon	2N4122
Q884	151-0188-00	1	Silicon	2N3906
Q884	151-0220-00	2	Silicon	2N4122
Q894	151-0188-00	1	Silicon	2N3906
Q894	151-0220-00	2	Silicon	2N4122
Q899	151-0190-00	1	Silicon	2N3904
Q899	*151-0190-01	2	Silicon	Tek Spec
Q907	151-0190-00	1	Silicon	2N3904
Q907	*151-0190-01	2	Silicon	Tek Spec
Q914	151-0188-00	1	Silicon	2N3906
Q914	151-0220-00	2	Silicon	2N4122
Q917	151-0190-00	1	Silicon	2N3904
Q917	*151-0190-01	2	Silicon	Tek Spec
Q919	151-0190-00	1	Silicon	2N3904
Q919	*151-0190-01	2	Silicon	Tek Spec
Q923	151-0190-00	1	Silicon	2N3904
Q923	*151-0190-01	2	Silicon	Tek Spec
Q927	151-0190-00	1	Silicon	2N3904
Q927	*151-0190-01	2	Silicon	Tek Spec
Q929	151-0190-00	1	Silicon	2N3904
Q929	*151-0190-01	2	Silicon	Tek Spec
Q933	151-0190-00	1	Silicon	2N3904
Q933	*151-0190-01	2	Silicon	Tek Spec
Q944	151-0188-00	1	Silicon	2N3906
Q944	151-0220-00	2	Silicon	2N4122
Q954	151-0188-00	1	Silicon	2N3906
Q954	151-0220-00	2	Silicon	2N4122

ZONE GENERATOR CARDS (2) Series A (cont)

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
Q956	151-0188-00	1		Silicon 2N3906
Q956	151-0220-00	2		Silicon 2N4122
Q964	151-0188-00	1		Silicon 2N3906
Q964	151-0220-00	2		Silicon 2N4122
Q974	151-0188-00	1		Silicon 2N3906
Q974	151-0220-00	2		Silicon 2N4122
Q976	151-0188-00	1		Silicon 2N3906
Q976	151-0220-00	2		Silicon 2N4122
Q984	151-0188-00	1		Silicon 2N3906
Q984	151-0220-00	2		Silicon 2N4122
Q994	151-0188-00	1		Silicon 2N3906
Q994	151-0220-00	2		Silicon 2N4122
Q999	151-0190-00	1		Silicon 2N3904
Q999	*151-0190-01	2		Silicon Tek Spec

Resistors

Resistors are fixed, composition, ±10% unless otherwise indicated.

R803	321-0287-00			9.53 kΩ	1/8 W	Prec	1%
R805	311-0510-00			10 kΩ, Var			
R806	321-0320-00			21 kΩ	1/8 W	Prec	1%
R807	315-0473-00			47 kΩ	1/4 W		5%
R809	321-0259-00			4.87 kΩ	1/8 W	Prec	1%
R811	315-0472-00	1	2	4.7 kΩ	1/4 W		5%
R811	315-0153-00	3		15 kΩ	1/4 W		5%
R812	315-0682-00	1	2	6.8 kΩ	1/4 W		5%
R812	315-0273-00	3		27 kΩ	1/4 W		5%
R813	315-0363-00	1	2	36 kΩ	1/4 W		5%
R813	315-0154-00	3		150 kΩ	1/4 W		5%
R815	321-0385-00			100 kΩ	1/8 W	Prec	1%
R817	321-0376-00			80.6 kΩ	1/8 W	Prec	1%
R819	315-0153-00			15 kΩ	1/4 W		5%
R821	321-0260-00			4.99 kΩ	1/8 W	Prec	1%
R823	315-0473-00			47 kΩ	1/4 W		5%
R825	321-0260-00			4.99 kΩ	1/8 W	Prec	1%
R827	315-0153-00			15 kΩ	1/4 W		5%
R831	315-0433-00			43 kΩ	1/4 W		5%
R832	315-0202-00			2 kΩ	1/4 W		5%
R833	315-0433-00			43 kΩ	1/4 W		5%
R835	315-0202-00			2 kΩ	1/4 W		5%
R836	315-0163-00			16 kΩ	1/4 W		5%
R838	315-0122-00			1.2 kΩ	1/4 W		5%
R839	315-0472-00			4.7 kΩ	1/4 W		5%
R841	315-0472-00	1	2	4.7 kΩ	1/4 W		5%
R841	315-0752-00	3		7.5 kΩ	1/4 W		5%
R842	315-0682-00	1	2	6.8 kΩ	1/4 W		5%
R842	315-0133-00	3		13 kΩ	1/4 W		5%
R843	315-0363-00	1	2	36 kΩ	1/4 W		5%
R843	315-0753-00	3		75 kΩ	1/4 W		5%
R845	321-0356-00			49.9 kΩ	1/8 W	Prec	1%
R847	321-0347-00			40.2 kΩ	1/8 W	Prec	1%
R851	315-0133-00			13 kΩ	1/4 W		5%

ZONE GENERATOR CARDS (2) Series A (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
R852	315-0752-00			7.5 kΩ	1/4 W		5%
R853	315-0153-00			15 kΩ	1/4 W		5%
R855	315-0104-00			100 kΩ	1/4 W		5%
R856	321-0341-00			34.8 kΩ	1/8 W	Prec	1%
R857	321-0318-00			20 kΩ	1/8 W	Prec	1%
R859	315-0433-00			43 kΩ	1/4 W		5%
R861	315-0472-00	1	2	4.7 kΩ	1/4 W		5%
R861	315-0752-00	3		7.5 kΩ	1/4 W		5%
R862	315-0682-00	1	2	6.8 kΩ	1/4 W		5%
R862	315-0133-00	3		13 kΩ	1/4 W		5%
R863	315-0363-00	1	2	36 kΩ	1/4 W		5%
R863	315-0753-00	3		75 kΩ	1/4 W		5%
R865	321-0327-00			24.9 kΩ	1/8 W	Prec	1%
R867	321-0318-00			20 kΩ	1/8 W	Prec	1%
R871	315-0133-00			13 kΩ	1/4 W		5%
R872	315-0752-00			7.5 kΩ	1/4 W		5%
R873	315-0153-00			15 kΩ	1/4 W		5%
R875	315-0104-00			100 kΩ	1/4 W		5%
R876	321-0306-00			15 kΩ	1/8 W	Prec	1%
R877	321-0289-00			10 kΩ	1/8 W	Prec	1%
R878	321-0338-00			32.4 kΩ	1/8 W	Prec	1%
R879	311-0541-00			20 kΩ, Var			
R881	315-0472-00	1	2	4.7 kΩ	1/4 W		5%
R881	315-0362-00	3		3.6 kΩ	1/4 W		5%
R882	315-0682-00			6.8 kΩ	1/4 W		5%
R883	315-0363-00			36 kΩ	1/4 W		5%
R884	315-0243-00	1	2	24 kΩ	1/4 W		5%
R884	315-0303-00	3		30 kΩ	1/4 W		5%
R885	323-0298-00			12.4 kΩ	1/2 W	Prec	1%
R887	321-0289-00			10 kΩ	1/8 W	Prec	1%
R891	315-0472-00	1	2	4.7 kΩ	1/4 W		5%
R891	315-0362-00	3		3.6 kΩ	1/4 W		5%
R892	315-0682-00			6.8 kΩ	1/4 W		5%
R893	315-0363-00			36 kΩ	1/4 W		5%
R894	315-0243-00	1	2X	24 kΩ	1/4 W		5%
R895	323-0269-00			6.19 kΩ	1/2 W	Prec	1%
R897	321-0260-00			4.99 kΩ	1/8 W	Prec	1%
R898	315-0393-00			39 kΩ	1/4 W		5%
R899	315-0152-00			1.5 kΩ	1/4 W		5%
R903	321-0287-00			9.53 kΩ	1/8 W	Prec	1%
R905	311-0510-00			10 kΩ, Var			
R906	321-0320-00			21 kΩ	1/8 W	Prec	1%
R907	315-0473-00			47 kΩ	1/4 W		5%
R909	321-0259-00			4.87 kΩ	1/8 W	Prec	1%
R911	315-0472-00	1	2	4.7 kΩ	1/4 W		5%
R911	315-0153-00	3		15 kΩ	1/4 W		5%
R912	315-0682-00	1	2	6.8 kΩ	1/4 W		5%
R912	315-0273-00	3		27 kΩ	1/4 W		5%

ZONE GENERATOR CARDS (2) Series A (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
R913	315-0363-00	1	2	36 kΩ	1/4 W		5%
R913	315-0154-00	3		150 kΩ	1/4 W		5%
R915	321-0385-00			100 kΩ	1/8 W	Prec	1%
R917	321-0376-00			80.6 kΩ	1/8 W	Prec	1%
R919	315-0153-00			15 kΩ	1/4 W		5%
R921	321-0260-00			4.99 kΩ	1/8 W	Prec	1%
R923	315-0473-00			47 kΩ	1/4 W		5%
R925	321-0260-00			4.99 kΩ	1/8 W	Prec	1%
R927	315-0153-00			15 kΩ	1/4 W		5%
R931	315-0433-00			43 kΩ	1/4 W		5%
R932	315-0202-00			2 kΩ	1/4 W		5%
R933	315-0433-00			43 kΩ	1/4 W		5%
R935	315-0202-00			2 kΩ	1/4 W		5%
R936	315-0163-00			16 kΩ	1/4 W		5%
R938	315-0122-00			1.2 kΩ	1/4 W		5%
R939	315-0472-00			4.7 kΩ	1/4 W		5%
R941	315-0472-00	1	2	4.7 kΩ	1/4 W		5%
R941	315-0752-00	3		7.5 kΩ	1/4 W		5%
R942	315-0682-00	1	2	6.8 kΩ	1/4 W		5%
R942	315-0133-00	3		13 kΩ	1/4 W		5%
R943	315-0363-00	1	2	36 kΩ	1/4 W		5%
R943	315-0753-00	3		75 kΩ	1/4 W		5%
R945	321-0356-00			49.9 kΩ	1/8 W	Prec	1%
R947	321-0347-00			40.2 kΩ	1/8 W	Prec	1%
R951	315-0133-00			13 kΩ	1/4 W		5%
R952	315-0752-00			7.5 kΩ	1/4 W		5%
R953	315-0153-00			15 kΩ	1/4 W		5%
R955	315-0104-00			100 kΩ	1/4 W		5%
R956	321-0341-00			34.8 kΩ	1/8 W	Prec	1%
R957	321-0318-00			20 kΩ	1/8 W	Prec	1%
R959	315-0433-00			43 kΩ	1/4 W		5%
R961	315-0472-00	1	2	4.7 kΩ	1/4 W		5%
R961	315-0752-00	3		7.5 kΩ	1/4 W		5%
R962	315-0682-00	1	2	6.8 kΩ	1/4 W		5%
R962	315-0133-00	3		13 kΩ	1/4 W		5%
R963	315-0363-00	1	2	36 kΩ	1/4 W		5%
R963	315-0753-00	3		75 kΩ	1/4 W		5%
R965	321-0327-00			24.9 kΩ	1/8 W	Prec	1%
R967	321-0318-00			20 kΩ	1/8 W	Prec	1%
R971	315-0133-00			13 kΩ	1/4 W		5%
R972	315-0752-00			7.5 kΩ	1/4 W		5%
R973	315-0153-00			15 kΩ	1/4 W		5%
R975	315-0104-00			100 kΩ	1/4 W		5%
R976	321-0306-00			15 kΩ	1/8 W	Prec	1%
R977	321-0289-00			10 kΩ	1/8 W	Prec	1%
R978	321-0338-00			32.4 kΩ	1/8 W	Prec	1%
R979	311-0541-00			20 kΩ, Var			
R981	315-0472-00	1	2	4.7 kΩ	1/4 W		5%
R981	315-0362-00	3		3.6 kΩ	1/4 W		5%

ZONE GENERATOR CARDS (2) Series A (cont)

Resistors (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
R982	315-0682-00			6.8 kΩ	1/4 W		5%
R983	315-0363-00			36 kΩ	1/4 W		5%
R984	315-0243-00	1	2	24 kΩ	1/4 W		5%
R984	315-0303-00	3		30 kΩ	1/4 W		5%
R985	323-0298-00			12.4 kΩ	1/2 W	Prec	1%
R987	321-0289-00			10 kΩ	1/8 W	Prec	1%
R991	315-0472-00	1	2	4.7 kΩ	1/4 W		5%
R991	315-0362-00	3		3.6 kΩ	1/4 W		5%
R992	315-0682-00			6.8 kΩ	1/4 W		5%
R993	315-0363-00			36 kΩ	1/4 W		5%
R994	315-0243-00	1	2X	24 kΩ	1/4 W		5%
R995	323-0269-00			6.19 kΩ	1/2 W	Prec	1%
R997	321-0260-00			4.99 kΩ	1/8 W	Prec	1%
R998	315-0393-00			39 kΩ	1/4 W		5%
R999	315-0152-00			1.5 kΩ	1/4 W		5%

MEMORY CARDS (2) Series B

	*670-0232-00			Complete Card			

Capacitors

Tolerance ±20% unless otherwise indicated.

C1011	283-0001-00			0.005 μF	Cer	500 V	
C1018	281-0549-00	1	5X	68 pF	Cer	500 V	10%
C1026	283-0001-00			0.005 μF	Cer	500 V	
C1037	290-0136-00			2.2 μF	Elect.	20 V	
C1041	283-0001-00			0.005 μF	Cer	500 V	
C1043	283-0002-00			0.01 μF	Cer	500 V	
C1057	290-0136-00			2.2 μF	Elect.	20 V	
C1063	285-0595-00			0.1 μF	PTM	100 V	1%
C1065	283-0060-00	1		100 pF	Cer	200 V	5%
C1065	283-0599-00	2		98 pF	Mica	500 V	5%
C1112	283-0001-00			0.005 μF	Cer	500 V	
C1119	283-0001-00			0.005 μF	Cer	500 V	
C1121	283-0010-00			0.05 μF	Cer	50 V	
C1153	285-0595-00			0.1 μF	PTM	100 V	1%
C1155	283-0060-00	1		100 pF	Cer	200 V	5%
C1155	283-0599-00	2		98 pF	Mica	500 V	5%
C1171	283-0001-00			0.005 μF	Cer	500 V	
C1179	281-0633-00	1	5X	910 pF	Cer	500 V	5%
C1191	290-0167-00			10 μF	Elect.	15 V	
C1193	290-0183-00			1 μF	Elect.	35 V	10%
C1195	290-0183-00			1 μF	Elect.	35 V	10%

Diodes

D1017	*152-0185-00			Silicon	Replaceable by 1N4152
D1018	*152-0185-00			Silicon	Replaceable by 1N4152
D1037	*152-0185-00			Silicon	Replaceable by 1N4152
D1046	*152-0185-00			Silicon	Replaceable by 1N4152
D1047	*152-0185-00			Silicon	Replaceable by 1N4152
D1051	*152-0185-00			Silicon	Replaceable by 1N4152

MEMORY CARDS (2) Series B (cont)

Diodes *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
D1057	*152-0185-00		Silicon	Replaceable by 1N4152
D1061	*152-0185-00		Silicon	Replaceable by 1N4152
D1062	*152-0185-00		Silicon	Replaceable by 1N4152
D1063	*152-0323-00	1	Silicon	Tek Spec
D1063	*152-0165-00	2	Silicon	Selected from 1N3579
D1063[1]	*152-0321-00	3	Silicon	Dual, Tek Spec
D1065	*152-0323-00	1	Silicon	Tek Spec
D1065	*152-0165-00	2	Silicon	Selected from 1N3579
D1065[1]	*152-0321-00	3	Silicon	Dual, Tek Spec
D1066	*152-0185-00		Silicon	Replaceable by 1N4152
D1068	152-0168-00		Zener	1N963A 400 mW, 12 V, 20%
D1123	*152-0185-00		Silicon	Replaceable by 1N4152
D1125	*152-0185-00		Silicon	Replaceable by 1N4152
D1126	*152-0185-00		Silicon	Replaceable by 1N4152
D1132	*152-0185-00		Silicon	Replaceable by 1N4152
D1142	*152-0185-00		Silicon	Replaceable by 1N4152
D1151	*152-0185-00		Silicon	Replaceable by 1N4152
D1152	*152-0185-00		Silicon	Replaceable by 1N4152
D1153	*152-0323-00	1	Silicon	Tek Spec
D1153	*152-0165-00	2	Silicon	Selected from 1N3579
D1153[2]	*152-0321-00	3	Silicon	Dual, Tek Spec
D1155	*152-0323-00	1	Silicon	Tek Spec
D1155	*152-0165-00	2	Silicon	Selected from 1N3579
D1155[2]	152-0321-00	3	Silicon	Dual, Tek Spec
D1156	*152-0185-00		Silicon	Replaceable by 1N4152
D1165	152-0168-00		Zener	1N963A 400 mW, 12 V, 20%
D1176	*152-0185-00		Silicon	Replaceable by 1N4152
D1177	*152-0185-00		Silicon	Replaceable by 1N4152
D1178	*152-0185-00		Silicon	Replaceable by 1N4152
D1179	*152-0185-00		Silicon	Replaceable by 1N4152

Integrated Circuits

M1012	156-0003-00		3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M1020	156-0006-00		Dual 2-Input NAND/NOR Gate	Replaceable by Motorola MC360G
M1022	156-0007-00		R-S Flipflop	Replaceable by Motorola MC352G
M1026	156-0003-00		3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M1040	156-0006-00		Dual 2-Input NAND/NOR Gate	Replaceable by Motorola MC360G
M1042	156-0006-00		Dual 2-Input NAND/NOR Gate	Replaceable by Motorola MC360G
M1048	156-0006-00		Dual 2-Input NAND/NOR Gate	Replaceable by Motorola MC360G
M1074	156-0013-00		Differential Comparator	Replaceable by Fairchild μA710C
M1112	156-0006-00		Dual 2-Input NAND/NOR Gate	Replaceable by Motorola MC360G
M1120	156-0003-00		3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G

[1]D1063 and D1065 model 3-up furnished as a pair.
[2]D1153 and D1155 model 3-up furnished as a pair.

MEMORY CARDS (2) Series B (cont)

Integrated Circuit (Cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
M1144	156-0007-00			R-S Flipflop	Replaceable by Motorola MC352G
M1150	156-0013-00			Differential Comparator	Replaceable by Fairchild μA710C
M1170	156-0003-00			3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M1190	156-0004-00			Bias Driver	Replaceable by Motorola MC354G

Transistors

Q1015	151-0190-00	1	4	Silicon	2N3904
Q1015	*151-0190-01	5		Silicon	Tek Spec
Q1018	151-0188-00	1	4	Silicon	2N3906
Q1018	151-0220-00	5		Silicon	2N4122
Q1031	151-0190-00	1	4	Silicon	2N3904
Q1031	*151-0190-01	5		Silicon	Tek Spec
Q1036	151-0188-00	1	4	Silicon	2N3906
Q1036	151-0220-00	5		Silicon	2N4122
Q1043	151-0190-00	1	4	Silicon	2N3904
Q1043	*151-0190-01	5		Silicon	Tek Spec
Q1046	151-0188-00	1	4	Silicon	2N3906
Q1046	151-0220-00	5		Silicon	2N4122
Q1051	151-0190-00	1	4	Silicon	2N3904
Q1051	*151-0190-01	5		Silicon	Tek Spec
Q1053	151-0190-00	1	4	Silicon	2N3904
Q1053	*151-0190-01	5		Silicon	Tek Spec
Q1057	151-0190-00	1	4	Silicon	2N3904
Q1057	*151-0190-01	5		Silicon	Tek Spec
Q1065	151-1002-00			Silicon	FET
Q1067	151-0190-00	1	4	Silicon	2N3904
Q1067	*151-0190-01	5		Silicon	Tek Spec
Q1068	151-0188-00	1	4	Silicon	2N3906
Q1068	151-0220-00	5		Silicon	2N4122
Q1071	151-0190-00	1	4	Silicon	2N3904
Q1071	*151-0190-01	5		Silicon	Tek Spec
Q1121	151-0190-00	1	4	Silicon	2N3904
Q1121	*151-0190-01	5		Silicon	Tek Spec
Q1125	151-0190-00	1	4	Silicon	2N3904
Q1125	*151-0190-01	5		Silicon	Tek Spec
Q1128	151-0188-00	1	4	Silicon	2N3906
Q1128	151-0220-00	5		Silicon	2N4122
Q1130	151-0188-00	1	4	Silicon	2N3906
Q1130	151-0220-00	5		Silicon	2N4122
Q1134	151-0188-00	1	4	Silicon	2N3906
Q1134	151-0220-00	5		Silicon	2N4122
Q1142	151-0188-00	1	4	Silicon	2N3906
Q1142	151-0220-00	5		Silicon	2N4122
Q1155	151-1002-00			Silicon	FET
Q1157	151-0190-00	1	4	Silicon	2N3904
Q1157	*151-0190-01	5		Silicon	Tek Spec

MEMORY CARDS (2) Series B (cont)

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc		Description
Q1159	151-0190-00	1	4	Silicon	2N3904
Q1159	*151-0190-01	5		Silicon	Tek Spec
Q1162	151-0188-00	1	4	Silicon	2N3906
Q1162	151-0220-00	5		Silicon	2N4122
Q1176	151-0188-00	1	4	Silicon	2N3906
Q1176	151-0220-00	5		Silicon	2N4122
Q1179	151-0190-00	1	4	Silicon	2N3904
Q1179	*151-0190-01	5		Silicon	Tek Spec
Q1182	151-0188-00	1	4	Silicon	2N3906
Q1182	151-0220-00	5		Silicon	2N4122
Q1185	151-0190-00	1	4	Silicon	2N3904
Q1185	*151-0190-01	5		Silicon	Tek Spec

Resistors

Resistors are fixed, composition, ±10% unless otherwise indicated.

R1011	315-0102-00	1 kΩ	¼ W	5%
R1013	315-0242-00	2.4 kΩ	¼ W	5%
R1014	315-0391-00	390 Ω	¼ W	5%
R1015	315-0622-00	6.2 kΩ	¼ W	5%
R1016	315-0433-00	43 kΩ	¼ W	5%
R1018	315-0134-00	130 kΩ	¼ W	5%
R1025	315-0102-00	1 kΩ	¼ W	5%
R1026	315-0433-00	43 kΩ	¼ W	5%
R1028	315-0242-00	2.4 kΩ	¼ W	5%
R1029	315-0242-00	2.4 kΩ	¼ W	5%
R1031	315-0391-00	390 Ω	¼ W	5%
R1033	315-0392-00	3.9 kΩ	¼ W	5%
R1034	315-0302-00	3 kΩ	¼ W	5%
R1036	315-0202-00	2 kΩ	¼ W	5%
R1037	315-0392-00	3.9 kΩ	¼ W	5%
R1038	315-0474-00	470 kΩ	¼ W	5%
R1041	315-0102-00	1 kΩ	¼ W	5%
R1042	315-0391-00	390 Ω	¼ W	5%
R1044	315-0272-00	2.7 kΩ	¼ W	5%
R1045	315-0391-00	390 Ω	¼ W	5%
R1046	315-0102-00	1 kΩ	¼ W	5%
R1047	315-0392-00	3.9 kΩ	¼ W	5%
R1048	315-0472-00	4.7 kΩ	¼ W	5%
R1049	315-0203-00	20 kΩ	¼ W	5%
R1051	315-0104-00	100 kΩ	¼ W	5%
R1053	315-0474-00	470 kΩ	¼ W	5%
R1055	315-0752-00	7.5 kΩ	¼ W	5%
R1056	315-0104-00	100 kΩ	¼ W	5%
R1058	315-0132-00	1.3 kΩ	¼ W	5%
R1059	315-0913-00	91 kΩ	¼ W	5%

MEMORY CARDS (2) Series B (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R1063	315-0100-00			10 Ω	1/4 W	5%
R1064	311-0633-00			5 kΩ, Var		
R1066	301-0473-00			47 kΩ	1/2 W	5%
R1068	301-0752-00			7.5 kΩ	1/2 W	5%
R1069	315-0473-00			47 kΩ	1/4 W	5%
R1071	315-0101-00			100 Ω	1/4 W	5%
R1073	315-0102-00			1 kΩ	1/4 W	5%
R1075	315-0102-00			1 kΩ	1/4 W	5%
R1077	311-0465-00			100 kΩ, Var		
R1078	315-0302-00	X6		3 kΩ	1/4 W	5%
R1079	315-0105-00	1	5	1 MΩ	1/4 W	5%
R1079	315-0205-00	6		2 MΩ	1/4 W	5%
R1112	315-0102-00			1 kΩ	1/4 W	5%
R1113	315-0272-00	1	3X	2.7 kΩ	1/4 W	5%
R1116	315-0391-00			390 Ω	1/4 W	5%
R1118	315-0102-00			1 kΩ	1/4 W	5%
R1119	315-0433-00			43 kΩ	1/4 W	5%
R1121	315-0391-00			390 Ω	1/4 W	5%
R1123	315-0272-00			2.7 kΩ	1/4 W	5%
R1124	315-0433-00			43 kΩ	1/4 W	5%
R1125	315-0473-00			47 kΩ	1/4 W	5%
R1126	315-0182-00			1.8 kΩ	1/4 W	5%
R1128	315-0753-00			75 kΩ	1/4 W	5%
R1129	315-0102-00			1 kΩ	1/4 W	5%
R1134	315-0474-00			470 kΩ	1/4 W	5%
R1141	315-0391-00			390 Ω	1/4 W	5%
R1142	315-0132-00			1.3 kΩ	1/4 W	5%
R1143	315-0242-00			2.4 kΩ	1/4 W	5%
R1145	315-0102-00			1 kΩ	1/4 W	5%
R1147	311-0465-00			100 kΩ, Var		
R1149	315-0205-00	1		2 MΩ	1/4 W	5%
R1149	315-0105-00	2	5	1 MΩ	1/4 W	5%
R1149	315-0205-00	6		2 MΩ	1/4 W	5%
R1150	315-0302-00	X6		3 kΩ	1/4 W	5%
R1153	315-0100-00			10 Ω	1/4 W	5%
R1154	311-0633-00			5 kΩ, Var		
R1156	301-0473-00			47 kΩ	1/2 W	5%
R1159	315-0393-00			39 kΩ	1/4 W	5%
R1161	315-0101-00			100 Ω	1/4 W	5%
R1162	303-0912-00	1	5	9.1 kΩ	1 W	5%
R1162	303-0752-00	6		7.5 kΩ	1 W	5%
R1163	315-0102-00			1 kΩ	1/4 W	5%
R1165	301-0123-00			12 kΩ	1/2 W	5%
R1171	315-0102-00			1 kΩ	1/4 W	5%
R1172	315-0242-00			2.4 kΩ	1/4 W	5%
R1174	315-0242-00			2.4 kΩ	1/4 W	5%
R1175	315-0391-00			390 Ω	1/4 W	5%
R1177	315-0224-00			220 kΩ	1/4 W	5%
R1178	315-0474-00			470 kΩ	1/4 W	5%
R1179	315-0154-00			150 kΩ	1/4 W	5%

MEMORY CARDS (2) Series B (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R1181	315-0391-00			390 Ω	1/4 W	5%
R1183	315-0622-00			6.2 kΩ	1/4 W	5%
R1184	315-0204-00			200 kΩ	1/4 W	5%
R1185	315-0101-00			100 Ω	1/4 W	5%
R1191	307-0110-00			3 Ω	1/4 W	5%
R1193	307-0110-00			3 Ω	1/4 W	5%
R1194	307-0110-00			3 Ω	1/4 W	5%
R1195	307-0110-00			3 Ω	1/4 W	5%
R1196	307-0110-00			3 Ω	1/4 W	5%

BUFFER CARD Series C

	*670-0233-00			Complete Card		

Capacitors

Tolerance ±20% unless otherwise indicated.

C621	283-0060-00			100 pF	Cer	200 V	5%
C624	283-0000-00			0.001 μF	Cer	500 V	
C665	285-0595-00			0.1 μF	PTM	100 V	1%
C681	281-0540-00	1	3	51 pF	Cer		5%
C681	281-0509-00	4		15 pF	Cer	500 V	
C686	283-0000-00	1		0.001 μF	Cer	500 V	
C686	283-0065-00	2		0.001 μF	Cer	100 V	5%
C689	290-0136-00			2.2 μF	Elect.	20 V	
C705	283-0111-00			0.1 μF	Cer	50 V	
C715	283-0003-00			0.01 μF	Cer	150 V	
C725	283-0111-00			0.1 μF	Cer	50 V	
C735	283-0003-00			0.01 μF	Cer	150 V	

Diodes

D631	*152-0185-00	1	3X	Silicon	Replaceable by 1N4152
D633	*152-0185-00			Silicon	Replaceable by 1N4152
D635	152-0246-00			Silicon	Low leakage 0.25 W, 40 V
D641	*152-0185-00	1	3X	Silicon	Replaceable by 1N4152
D643	*152-0185-00			Silicon	Replaceable by 1N4152
D645	152-0246-00			Silicon	Low leakage 0.25 W, 40 V
D652	*152-0185-00			Silicon	Replaceable by 1N4152
D653	152-0246-00			Silicon	Low leakage 0.25 W, 40 V
D671	*152-0185-00	1	6	Silicon	Replaceable by 1N4152
D671	*152-0242-00	7		Silicon	Selected from 1N486A
D701	*152-0185-00			Silicon	Replaceable by 1N4152
D706	*152-0185-00			Silicon	Replaceable by 1N4152
D707	*152-0185-00			Silicon	Replaceable by 1N4152
D721	*152-0185-00			Silicon	Replaceable by 1N4152
D726	*152-0185-00			Silicon	Replaceable by 1N4152
D727	*152-0185-00			Silicon	Replaceable by 1N4152

BUFFER CARD Series C (cont)

Integrated Circuits

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
M614	156-0003-00			3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M618	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M620	156-0007-00			R-S Flipflop	Replaceable by Motorola MC352G
M740	156-0004-00			Bias Driver	Replaceable by Motorola MC354G

Transistors

Q611	151-0190-00	1	4	Silicon	2N3904
Q611	*151-0190-01	5		Silicon	Tek Spec
Q613	151-0190-00	1	4	Silicon	2N3904
Q613	*151-0190-01	5		Silicon	Tek Spec
Q617	151-0190-00	1	4	Silicon	2N3904
Q617	*151-0190-01	5		Silicon	Tek Spec
Q632	151-0188-00	1	4	Silicon	2N3906
Q632	151-0220-00	5		Silicon	2N4122
Q642	151-0188-00	1	4	Silicon	2N3906
Q642	151-0220-00	5		Silicon	2N4122
Q652	151-0188-00	1	4	Silicon	2N3906
Q652	151-0220-00	5		Silicon	2N4122
Q663	151-0190-00	1	4	Silicon	2N3904
Q663	*151-0190-01	5		Silicon	Tek Spec
Q666	151-0188-00	1	4	Silicon	2N3906
Q666	151-0220-00	5		Silicon	2N4122
Q671	*151-0136-00	1	3	Silicon	Replaceable by 2N3053
Q671	151-0190-00	4		Silicon	2N3904
Q671	*151-0190-01	5		Silicon	Tek Spec
Q676	151-0188-00	X4		Silicon	2N3906
Q676	151-0220-00	5		Silicon	2N4122
Q677	151-0190-00	1	4	Silicon	2N3904
Q677	*151-0190-01	5		Silicon	Tek Spec
Q685	*151-0136-00	1	3	Silicon	Replaceable by 2N3053
Q685	151-0190-00	4		Silicon	2N3904
Q685	*151-0190-01	5		Silicon	Tek Spec
Q687	151-0179-00			Silicon	2N3877A
Q689	151-0179-00			Silicon	2N3877A
Q711	151-0190-00	1	4	Silicon	2N3904
Q711	*151-0190-01	5		Silicon	Tek Spec
Q714	151-0188-00	1	4	Silicon	2N3906
Q714	151-0220-00	5		Silicon	2N4122
Q731	151-0190-00	1	4	Silicon	2N3904
Q731	*151-0190-01	5		Silicon	Tek Spec
Q734	151-0188-00	1	4	Silicon	2N3906
Q734	151-0220-00	5		Silicon	2N4122

BUFFER CARD Series C (cont)

Resistors

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
Resistors are fixed, composition, ±10% unless otherwise indicated.						
R611	315-0102-00			1 kΩ	1/4 W	5%
R612	315-0821-00			820 Ω	1/4 W	5%
R613	315-0621-00			620 Ω	1/4 W	5%
R614	315-0202-00			2 kΩ	1/4 W	5%
R617	315-0103-00			10 kΩ	1/4 W	5%
R618	315-0103-00			10 kΩ	1/4 W	5%
R619	315-0472-00			4.7 kΩ	1/4 W	5%
R621	315-0153-00			15 kΩ	1/4 W	5%
R622	315-0393-00			39 kΩ	1/4 W	5%
R624	315-0363-00			36 kΩ	1/4 W	5%
R625	315-0433-00			43 kΩ	1/4 W	5%
R630	315-0122-00	X4		1.2 kΩ	1/4 W	5%
R631	315-0562-00			5.6 kΩ	1/4 W	5%
R633	315-0823-00			82 kΩ	1/4 W	5%
R634	321-0363-00			59 kΩ	1/8 W Prec	1%
R635	311-0463-00			5 kΩ, Var		
R640	315-0202-00	X4		2 kΩ	1/4 W	5%
R641	315-0103-00			10 kΩ	1/4 W	5%
R643	315-0823-00			82 kΩ	1/4 W	5%
R644	321-0408-00			174 kΩ	1/8 W Prec	1%
R645	311-0541-00			20 kΩ, Var		
R651	315-0221-00			220 Ω	1/4 W	5%
R653	315-0202-00			2 kΩ	1/4 W	5%
R654	315-0821-00			820 Ω	1/4 W	5%
R655	315-0182-00			1.8 kΩ	1/4 W	5%
R656	315-0223-00			22 kΩ	1/4 W	5%
R660	311-0541-00			20 kΩ, Var		
R661	321-0409-00			178 kΩ	1/8 W Prec	1%
R662	315-0244-00			240 kΩ	1/4 W	5%
R665	315-0243-00			24 kΩ	1/4 W	5%
R667	303-0563-00	X4		56 kΩ	1 W	5%
R668	315-0102-00	X4		1 kΩ	1/4 W	5%
R669	315-0624-00	X3		620 kΩ	1/4 W	5%
R670	311-0510-00			10 kΩ, Var		
R671	316-0275-00			2.7 MΩ	1/4 W	
R672	321-0338-00	1	3	32.4 kΩ	1/8 W Prec	1%
R672	321-0347-00	4		40.2 kΩ	1/8 W Prec	1%
R673	321-0261-00			5.11 kΩ	1/8 W Prec	1%
R675	311-0465-00			100 kΩ, Var		
R676	315-0274-00	1	3	270 kΩ	1/4 W	5%
R676	322-0481-00	4		1 MΩ	1/4 W Prec	1%
R677	315-0474-00	X4		470 kΩ	1/4 W	5%
R678	315-0332-00	1	3	3.3 kΩ	1/4 W	5%
R678	315-0273-00	4		27 kΩ	1/4 W	5%
R680	311-0510-00	X4		10 kΩ		

BUFFER CARD Series C (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
R681	321-0346-00	1	3	39.2 kΩ	1/8 W	Prec	1%
R681	321-0353-00	4		46.4 kΩ	1/8 W	Prec	1%
R682	321-0349-00	1	5	42.2 kΩ	1/8 W	Prec	1%
R682	321-0350-00	6		43.2 kΩ	1/8 W	Prec	1%
R683	321-0357-00			51.1 kΩ	1/8 W	Prec	1%
R685	315-0184-00			180 kΩ	1/4 W		5%
R686	315-0511-00			510 Ω	1/4 W		5%
R687	315-0113-00			11 kΩ	1/4 W		5%
R689	315-0101-00			100 Ω	1/4 W		5%
R701	315-0363-00	1	6	36 kΩ	1/4 W		5%
R701	315-0513-00	7		51 kΩ	1/4 W		5%
R702	321-0289-03			10 kΩ	1/8 W	Prec	0.25%
R704	321-0389-00			110 kΩ	1/8 W	Prec	1%
R705	315-0102-00			1 kΩ	1/4 W		5%
R709	321-0293-03			11 kΩ	1/8 W	Prec	0.25%
R711	315-0244-00			240 kΩ	1/4 W		5%
R714	315-0471-00			470 Ω	1/4 W		5%
R716	301-0103-00			10 kΩ	1/2 W		5%
R721	315-0363-00	1	6	36 kΩ	1/4 W		5%
R721	315-0513-00	7		51 kΩ	1/4 W		5%
R722	321-0289-00			10 kΩ	1/8 W	Prec	0.25%
R724	321-0389-00			110 kΩ	1/8 W	Prec	1%
R725	315-0102-00			1 kΩ	1/4 W		5%
R727	315-0821-00			820 Ω	1/4 W		5%
R728	315-0621-00	1		620 Ω	1/4 W		5%
R728	315-0821-00	2		820 Ω	1/4 W		5%
R729	321-0293-03			11 kΩ	1/8 W	Prec	0.25%
R731	315-0244-00			240 kΩ	1/4 W		5%
R734	315-0471-00			470 Ω	1/4 W		5%
R736	301-0103-00			10 kΩ	1/2 W		5%

Switch

	Unwired or Wired				
SW671	260-0984-00	X4	Slide	CAL RUN	

COMPARATOR CARDS (2) Series D

	*670-0234-00	Complete Card

Capacitors

Tolerance ±20% unless otherwise indicated.

C1422	283-0054-00		150 pF	Cer	200 V	5%
C1425	283-0065-00	X5	0.001 μF	Cer	100 V	5%
C1462	283-0000-00		0.001 μF	Cer	500 V	
C1477	281-0525-00		470 pF	Cer	500 V	
C1478	290-0136-00		2.2 μF	Elect.	20 V	

COMPARATOR CARDS (2) Series D (cont)

Capacitors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
C1592	290-0327-00			0.56 μF	Elect.	100 V	
C1594	290-0183-00			1 μF	Elect.	35 V	10%
C1596	290-0183-00			1 μF	Elect.	35 V	10%
C1598	290-0327-00			0.56 μF	Elect.	100 V	

Diodes

D1311	*152-0185-00			Silicon	Replaceable by 1N4152
D1316	*152-0185-00			Silicon	Replaceable by 1N4152
D1317	*152-0185-00			Silicon	Replaceable by 1N4152
D1336	*152-0185-00			Silicon	Replaceable by 1N4152
D1361	*152-0185-00			Silicon	Replaceable by 1N4152
D1362	*152-0185-00			Silicon	Replaceable by 1N4152
D1364	*152-0185-00			Silicon	Replaceable by 1N4152
D1366	*152-0185-00			Silicon	Replaceable by 1N4152
D1374	*152-0185-00			Silicon	Replaceable by 1N4152
D1376	*152-0185-00			Silicon	Replaceable by 1N4152
D1379	*152-0185-00			Silicon	Replaceable by 1N4152
D1382	*152-0185-00			Silicon	Replaceable by 1N4152
D1445[3]	*153-0033-00	1	5	Matched Resistors and Diode assembly	
D1445[4]	*153-0033-01	6		Matched Resistors and Diode assembly	
D1511	*152-0185-00			Silicon	Replaceable by 1N4152
D1521	*152-0185-00			Silicon	Replaceable by 1N4152
D1530	*152-0185-00			Silicon	Replaceable by 1N4152
D1531	*152-0185-00			Silicon	Replaceable by 1N4152
D1540	*152-0185-00			Silicon	Replaceable by 1N4152
D1541	*152-0185-00			Silicon	Replaceable by 1N4152
D1551	*152-0185-00			Silicon	Replaceable by 1N4152
D1561	*152-0185-00			Silicon	Replaceable by 1N4152
D1571	*152-0185-00			Silicon	Replaceable by 1N4152
D1581	*152-0185-00			Silicon	Replaceable by 1N4152

Relays

K1314	*108-0340-00	1	3	Coil, Reed (double)	
K1314A	260-0877-00	1		Reed	
K1314A	260-0877-01	2	3	Reed	
K1314B	260-0877-00	1		Reed	
K1314B	260-0877-01	2	3	Reed	
K1314 K1314A K1314B	148-0041-00	4		Reed (double)	
K1318	*108-0340-00	1	3	Coil, Reed (double)	
K1318A	260-0877-00	1		Reed	
K1318A	260-0877-01	2	3	Reed	
K1318B	260-0877-00	1		Reed	
K1318B	260-0877-01	2	3	Reed	
K1318 K1318A K1318B	148-0041-00	4		Reed (double)	

[3]Furnished as a unit with R1434 and R1456.

[4]Furnished as a unit with R1433, R1434, R1456 and R1457 mod 6-up.

COMPARATOR CARDS (2) Series D (cont)

Relays *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
K1324	*108-0355-00	1	3	Coil, Reed
K1324A	260-0877-00	1		Reed
K1324A	260-0877-01	2	3	Reed
K1324 K1324A	148-0039-00	4		Reed (single)
K1336	*108-0340-00	1	3	Coil, Reed (double)
K1336A	260-0877-00	1		Reed
K1336A	260-0877-01	2	3	Reed
K1336B	260-0877-00	1		Reed
K1336B	260-0877-01	2	3	Reed
K1336 K1336A K1336B	148-0041-00	4		Reed (double)
K1342	*108-0355-00	1	3	Coil, Reed
K1342A	260-0877-00	1		Reed
K1342A	260-0877-01	2	3	Reed
K1342 K1342A	148-0039-00	4		Reed (single)
K1356	*108-0355-00	1	3	Coil, Reed
K1356A	260-0877-00	1		Reed
K1356A	260-0877-01	2	3	Reed
K1356 K1356A	148-0039-00	4		Reed (single)
K1364	*108-0340-00	1	3	Coil, Reed (double)
K1364A	260-0877-00	1		Reed
K1364A	260-0877-01	2	3	Reed
K1364B	260-0877-00	1		Reed
K1364B	260-0877-01	2	3	Reed
K1364 K1364A K1364B	148-0041-00	4		Reed (double)
K1368	*108-0340-00	1	3	Coil, Reed (double)
K1368A	260-0877-00	1		Reed
K1368A	260-0877-01	2	3	Reed
K1368B	260-0877-00	1		Reed
K1368B	260-0877-01	2	3	Reed
K1368 K1368A K1368B	148-0041-00	4		Reed (double)
K1374	*108-0340-00	1	3	Coil, Reed (double)
K1374A	260-0877-00	1		Reed

COMPARATOR CARDS (2) Series D (cont)

Relays *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
K1374A	260-0877-01	2	3	Reed
K1374B	260-0877-00	1		Reed
K1374B	260-0877-01	2	3	Reed
K1374 K1374A K1374B	148-0041-00	4		Reed (double)
K1382	*108-0355-00	1	3	Coil, Reed
K1382A	260-0877-00	1		Reed
K1382A	260-0877-01	2	3	Reed
K1382 K1382A	148-0039-00	4		Reed (single)
K1392	*108-0355-00	1	3	Coil, Reed
K1392A	260-0877-00	1		Reed
K1392A	260-0877-01	2	3	Reed
K1392 K1392A	148-0039-00	4		Reed (single)
K1513	*108-0355-00	1	3	Coil, Reed
K1513A	260-0877-00	1		Reed
K1513A	260-0877-01	2	3	Reed
K1513 K1513A	148-0039-00	4		Reed (single)
K1523	*108-0355-00	1	3	Coil, Reed
K1523A	260-0877-00	1		Reed
K1523A	260-0877-01	2	3	Reed
K1523 K1523A	148-0039-00	4		Reed (single)
K1533	*108-0355-00	1	3	Coil, Reed
K1533A	260-0877-00	1		Reed
K1533A	260-0877-01	2	3	Reed
K1533 K1533A	148-0039-00	4		Reed (single)
K1543	*108-0355-00	1	3	Coil, Reed
K1543A	260-0877-00	1		Reed
K1543A	260-0877-01	2	3	Reed
K1543 K1543A	148-0039-00	4		Reed (single)
K1553	*108-0355-00	1	3	Coil, Reed
K1553A	260-0877-00	1		Reed
K1553A	260-0877-01	2	3	Reed
K1553 K1553A	148-0039-00	4		Reed (single)

COMPARATOR CARDS (2) Series D (cont)

Relays *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
K1563	*108-0355-00	1	3	Coil, Reed
K1563A	260-0877-00	1		Reed
K1563A	260-0877-01	2	3	Reed
K1563 } K1563A }	148-0039-00	4		Reed (single)
K1573	*108-0355-00	1	3	Coil, Reed
K1573A	260-0877-00	1		Reed
K1573A	260-0877-01	2	3	Reed
K1573 } K1573A }	148-0039-00	4		Reed (single)
K1583	*108-0355-00	1	3	Coil, Reed
K1583A	260-0877-00	1		Reed
K1583A	260-0877-01	2	3	Reed
K1583 } K1583A }	148-0039-00	4		Reed (single)

Integrated Circuit

M1472	156-0013-00			Differential Comparator	Replaceable by Fairchild μA710C

Transistors

Q1314	151-0188-00	1	2	Silicon	2N3906
Q1314	151-0220-00	3		Silicon	2N4122
Q1318	151-0188-00	1	2	Silicon	2N3906
Q1318	151-0220-00	3		Silicon	2N4122
Q1324	151-0188-00	1	2	Silicon	2N3906
Q1324	151-0220-00	3		Silicon	2N4122
Q1336	151-0188-00	1	2	Silicon	2N3906
Q1336	151-0220-00	3		Silicon	2N4122
Q1342	151-0188-00	1	2	Silicon	2N3906
Q1342	151-0220-00	3		Silicon	2N4122
Q1356	151-0188-00	1	2	Silicon	2N3906
Q1356	151-0220-00	3		Silicon	2N4122
Q1364	151-0188-00	1	2	Silicon	2N3906
Q1364	151-0220-00	3		Silicon	2N4122
Q1368	151-0188-00	1	2	Silicon	2N3906
Q1368	151-0220-00	3		Silicon	2N4122
Q1374	151-0188-00	1	2	Silicon	2N3906
Q1374	151-0220-00	3		Silicon	2N4122
Q1378	151-0188-00	1	2	Silicon	2N3906
Q1378	151-0220-00	3	3X	Silicon	2N4122
Q1382	151-0188-00	1	2	Silicon	2N3906
Q1382	151-0220-00	3		Silicon	2N4122
Q1392	151-0188-00	1	2	Silicon	2N3906
Q1392	151-0220-00	3		Silicon	2N4122
Q1421	*151-0104-00			Silicon	Replaceable by 2N2913

COMPARATOR CARDS (2) Series D (cont)

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc		Description
Q1422	151-0188-00	1	2	Silicon	2N3906
Q1422	151-0220-00	3		Silicon	2N4122
Q1423	151-0190-00	1	2	Silicon	2N3904
Q1423	*151-0190-01	3		Silicon	Tek Spec
Q1424	151-0188-00	1	2	Silicon	2N3906
Q1424	151-0220-00	3		Silicon	2N4122
Q1428	*151-0133-00			Silicon	Selected from 2N3251
Q1442	*151-0134-00			Silicon	Replaceable by 2N2905
Q1449	*151-0103-00			Silicon	Replaceable by 2N2219
Q1461	*151-0104-00			Silicon	Replaceable by 2N2913
Q1462	151-0188-00	1	2	Silicon	2N3906
Q1462	151-0220-00	3		Silicon	2N4122
Q1463	151-0190-00	1	2	Silicon	2N3904
Q1463	*151-0190-01	3		Silicon	Tek Spec
Q1464	151-0188-00	1	2	Silicon	2N3906
Q1464	151-0220-00	3		Silicon	2N4122
Q1472	*151-0133-00			Silicon	Selected from 2N3251
Q1513	151-0190-00	1	2	Silicon	2N3904
Q1513	*151-0190-01	3		Silicon	Tek Spec
Q1523	151-0190-00	1	2	Silicon	2N3904
Q1523	*151-0190-01	3		Silicon	Tek Spec
Q1533	151-0190-00	1	2	Silicon	2N3904
Q1533	*151-0190-01	3		Silicon	Tek Spec
Q1543	151-0190-00	1	2	Silicon	2N3904
Q1543	*151-0190-01	3		Silicon	Tek Spec
Q1553	151-0190-00	1	2	Silicon	2N3904
Q1553	*151-0190-01	3		Silicon	Tek Spec
Q1563	151-0190-00	1	2	Silicon	2N3904
Q1563	*151-0190-01	3		Silicon	Tek Spec
Q1573	151-0190-00	1	2	Silicon	2N3904
Q1573	*151-0190-01	3		Silicon	Tek Spec
Q1583	151-0190-00	1	2	Silicon	2N3904
Q1583	*151-0190-01	3		Silicon	Tek Spec

Resistors

Resistors are fixed, composition, ±10% unless otherwise indicated.

R1311	315-0202-00		2 kΩ	¼ W	5%
R1312	315-0241-00		240 Ω	¼ W	5%
R1314	315-0182-00		1.8 kΩ	¼ W	5%
R1316	315-0332-00		3.3 kΩ	¼ W	5%
R1317	315-0113-00		11 kΩ	¼ W	5%
R1318	315-0223-00	1	3 22 kΩ	¼ W	5%
R1318	315-0203-00	4	20 kΩ	¼ W	5%
R1321	315-0202-00		2 kΩ	¼ W	5%
R1322	315-0241-00		240 Ω	¼ W	5%
R1323	315-0562-00		5.6 kΩ	¼ W	5%

COMPARATOR CARDS (2) Series D (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R1324	315-0241-00	1	3	240 Ω	1/4 W	5%
R1324	315-0181-00	4		180 Ω	1/4 W	5%
R1326	315-0332-00			3.3 kΩ	1/4 W	5%
R1327	315-0473-00			47 kΩ	1/4 W	5%
R1329	315-0682-00			6.8 kΩ	1/4 W	5%
R1331	315-0912-00			9.1 kΩ	1/4 W	5%
R1332	315-0912-00			9.1 kΩ	1/4 W	5%
R1333	315-0752-00			7.5 kΩ	1/4 W	5%
R1334	315-0222-00			2.2 kΩ	1/4 W	5%
R1336	315-0912-00			9.1 kΩ	1/4 W	5%
R1338	315-0163-00			16 kΩ	1/4 W	5%
R1342	315-0241-00	1	3	240 Ω	1/4 W	5%
R1342	315-0181-00	4		180 Ω	1/4 W	5%
R1343	315-0272-00			2.7 kΩ	1/4 W	5%
R1345	315-0123-00			12 kΩ	1/4 W	5%
R1346	315-0682-00			6.8 kΩ	1/4 W	5%
R1351	315-0912-00			9.1 kΩ	1/4 W	5%
R1352	315-0912-00			9.1 kΩ	1/4 W	5%
R1354	315-0912-00			9.1 kΩ	1/4 W	5%
R1355	315-0163-00			16 kΩ	1/4 W	5%
R1356	315-0241-00	1	3	240 Ω	1/4 W	5%
R1356	315-0181-00	4		180 Ω	1/4 W	5%
R1357	315-0272-00			2.7 kΩ	1/4 W	5%
R1358	315-0123-00			12 kΩ	1/4 W	5%
R1359	315-0682-00			6.8 kΩ	1/4 W	5%
R1361	315-0302-00			3 kΩ	1/4 W	5%
R1362	315-0103-00			10 kΩ	1/4 W	5%
R1363	315-0622-00			6.2 kΩ	1/4 W	5%
R1364	315-0473-00			47 kΩ	1/4 W	5%
R1366	315-0202-00			2 kΩ	1/4 W	5%
R1367	315-0241-00			240 Ω	1/4 W	5%
R1368	315-0303-00			30 kΩ	1/4 W	5%
R1371	315-0512-00			5.1 kΩ	1/4 W	5%
R1372	315-0183-00	1	5	18 kΩ	1/4 W	5%
R1372	315-0163-00	6		16 kΩ	1/4 W	5%
R1373	315-0512-00			5.1 kΩ	1/4 W	5%
R1376	315-0512-00			5.1 kΩ	1/4 W	5%
R1377	315-0183-00			18 kΩ	1/4 W	5%
R1378	315-0822-00			8.2 kΩ	1/4 W	5%
R1382	315-0241-00	1	3	240 Ω	1/4 W	5%
R1382	315-0181-00	4		180 Ω	1/4 W	5%
R1383	315-0272-00			2.7 kΩ	1/4 W	5%
R1385	315-0822-00			8.2 kΩ	1/4 W	5%
R1386	315-0822-00			8.2 kΩ	1/4 W	5%
R1389	315-0273-00	1	5	27 kΩ	1/4 W	5%
R1389	315-0223-00	6		22 kΩ	1/4 W	5%
R1392	315-0241-00	1	3	240 Ω	1/4 W	5%

COMPARATOR CARDS (2) Series D (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
R1392	315-0181-00	4		180 Ω	1/4 W		5%
R1393	315-0182-00	1	3	1.8 kΩ	1/4 W		5%
R1393	315-0272-00	4		2.7 kΩ	1/4 W		5%
R1410	315-0103-00			10 kΩ	1/4 W		5%
R1421	321-0235-00			2.74 kΩ	1/8 W	Prec	1%
R1422	323-0491-00			1.27 MΩ	1/2 W	Prec	1%
R1423	321-0441-00			383 kΩ	1/8 W	Prec	1%
R1424	315-0114-00			110 kΩ	1/4 W		5%
R1425	311-0464-00			25 kΩ, Var			
R1426	323-0462-00			634 kΩ	1/2 W	Prec	1%
R1428	315-0153-00			15 kΩ	1/4 W		5%
R1430	315-0103-00			10 kΩ	1/4 W		5%
R1431	308-0438-00	1	6	5 kΩ	3 W	WW	0.5%
R1431	308-0586-00	7		5 kΩ	3 W	WW	0.25%
R1433	308-0439-00	1	5	5.83 kΩ	3 W	WW	0.5%
R1433[5]	*153-0033-01	6		Matched Resistors and Diode assembly			
R1434[6]	*153-0033-00	1	5	Matched Resistors and Diode assembly			
R1434[5]	*153-0033-01	6		Matched Resistors and Diode assembly			
R1435	311-0433-00			100 Ω, Var			
R1438	321-0235-00			2.74 kΩ	1/8 W	Prec	1%
R1439	315-0470-00			47 Ω	1/4 W		5%
R1442	323-0260-00			4.99 kΩ	1/2 W	Prec	1%
R1443	323-0310-00	1	5	16.5 kΩ	1/2 W	Prec	1%
R1443	323-0318-00	6		20 kΩ	1/2 W	Prec	1%
R1444	321-0269-00			6.19 kΩ	1/8 W	Prec	1%
R1445	311-0462-00			1 kΩ, Var			
R1446	321-0269-00			6.19 kΩ	1/8 W	Prec	1%
R1447	323-0310-00	1	5	16.5 kΩ	1/2 W	Prec	1%
R1447	323-0318-00	6		20 kΩ	1/2 W	Prec	1%
R1449	323-0260-00			4.99 kΩ	1/2 W	Prec	1%
R1450	315-0103-00			10 kΩ	1/4 W		5%
R1455	311-0433-00			100 Ω, Var			
R1456[7]	*153-0033-00	1	5	Matched Resistors and Diode assembly			
R1456[5]	*153-0033-01	6		Matched Resistors and Diode assembly			
R1457	308-0439-00	1	5	5.83 kΩ	3 W	WW	0.5%
R1457[5]	*153-0033-01	6		Matched Resistors and Diode assembly			
R1459	315-0152-00			1.5 kΩ	1/4 W		5%
R1460	315-0103-00			10 kΩ	1/4 W		5%
R1461	321-0239-00			3.01 kΩ	1/8 W	Prec	1%
R1462	323-0491-00			1.27 MΩ	1/2 W	Prec	1%
R1463	321-0441-00			383 kΩ	1/8 W	Prec	1%
R1464	315-0114-00			110 kΩ	1/4 W		5%
R1465	311-0464-00			25 kΩ, Var			
R1466	323-0462-00			634 kΩ	1/2 W	Prec	1%
R1468	315-0102-00			1 kΩ	1/4 W		5%
R1469	315-0133-00			13 kΩ	1/4 W		5%
R1470	315-0103-00			10 kΩ	1/4 W		5%

[5]R1433, R1434, R1456, R1457 and D1455 model 6-up furnished as a unit.

[6]Furnished as a unit with D1445 and R1456.

[7]Furnished as a unit with D1445 and R1434.

COMPARATOR CARDS (2) Series D (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R1471	315-0471-00			470 Ω	¼ W	5%
R1472	315-0153-00			15 kΩ	¼ W	5%
R1473	315-0471-00			470 Ω	¼ W	5%
R1474	316-0225-00			2.2 MΩ	¼ W	
R1475	311-0465-00			100 kΩ, Var		
R1477	315-0471-00			470 Ω	¼ W	5%
R1478	315-0101-00			100 Ω	¼ W	5%
R1479	315-0471-00			470 Ω	¼ W	5%
R1481	321-0068-00			49.9 Ω	⅛ W Prec	1%
R1482	321-0636-00			100 Ω	⅛ W Prec	0.5%
R1483	321-0636-00			100 Ω	⅛ W Prec	0.5%
R1484	321-0636-00			100 Ω	⅛ W Prec	0.5%
R1485	321-0636-00			100 Ω	⅛ W Prec	0.5%
R1486	308-0434-00			500 Ω	3 W WW	0.25%
R1487	308-0435-00			1 kΩ	3 W WW	0.25%
R1488	308-0436-00			2 kΩ	3 W WW	0.1%
R1489	308-0437-00			4 kΩ	3 W WW	0.1%
R1511	315-0103-00			10 kΩ	¼ W	5%
R1512	315-0562-00			5.6 kΩ	¼ W	5%
R1513	315-0182-00			1.8 kΩ	¼ W	5%
R1514	315-0161-00			160 Ω	¼ W	5%
R1521	315-0103-00			10 kΩ	¼ W	5%
R1522	315-0562-00			5.6 kΩ	¼ W	5%
R1523	315-0182-00			1.8 kΩ	¼ W	5%
R1524	315-0161-00			160 Ω	¼ W	5%
R1531	315-0103-00			10 kΩ	¼ W	5%
R1532	315-0562-00			5.6 kΩ	¼ W	5%
R1533	315-0182-00			1.8 kΩ	¼ W	5%
R1534	315-0161-00			160 Ω	¼ W	5%
R1541	315-0103-00			10 kΩ	¼ W	5%
R1542	315-0562-00			5.6 kΩ	¼ W	5%
R1543	315-0182-00			1.8 kΩ	¼ W	5%
R1544	315-0161-00			160 Ω	¼ W	5%
R1551	315-0103-00			10 kΩ	¼ W	5%
R1552	315-0562-00			5.6 kΩ	¼ W	5%
R1553	315-0182-00			1.8 kΩ	¼ W	5%
R1554	315-0161-00			160 Ω	¼ W	5%
R1561	315-0103-00			10 kΩ	¼ W	5%
R1562	315-0562-00			5.6 kΩ	¼ W	5%
R1563	315-0182-00			1.8 kΩ	¼ W	5%
R1564	315-0161-00			160 Ω	¼ W	5%
R1571	315-0103-00			10 kΩ	¼ W	5%
R1572	315-0562-00			5.6 kΩ	¼ W	5%
R1573	315-0182-00			1.8 kΩ	¼ W	5%
R1574	315-0161-00			160 Ω	¼ W	5%

COMPARATOR CARDS (2) Series D (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R1581	315-0103-00			10 kΩ	1/4 W	5%
R1582	315-0562-00			5.6 kΩ	1/4 W	5%
R1583	315-0182-00			1.8 kΩ	1/4 W	5%
R1584	315-0161-00			160 Ω	1/4 W	5%
R1592	315-0470-00			47 Ω	1/4 W	5%
R1594	315-0101-00			100 Ω	1/4 W	5%
R1596	315-0101-00			100 Ω	1/4 W	5%
R1598	315-0470-00			47 Ω	1/4 W	5%

Switch

Ckt. No.	Unwired or Wired Tektronix Part No.	Serial/Model No. Eff	Disc	Description
SW1585	260-0723-00			Slide CALIBRATE RUN

Test Points

TP1410	*214-0579-00			Pin, Test Point
TP1430	*214-0579-00			Pin, Test Point
TP1450	*214-0579-00			Pin, Test Point
TP1460	*214-0579-00			Pin, Test Point
TP1470	*214-0579-00			Pin, Test Point

CLOCK CARD Series E

	*670-0235-00	1	2	Complete Card		
	*670-0235-02	3		Complete Card		

Capacitors

Tolerance ±20% unless otherwise indicated.

C2015	283-0110-00			0.005 μF	Cer	150 V	
C2022	281-0543-00	1	2	270 pF	Cer	500 V	10%
C2022	281-0536-00	3		1000 pF	Cer	500 V	10%
C2023	283-0605-00	X3		678 pF	Mica	300 V	1%
C2024	281-0524-00	1	2X	150 pF	Cer	500 V	
C2026	283-0640-00	X3		160 pF	Mica	100 V	1%
C2027	281-0536-00	1	2X	1000 pF	Cer	500 V	10%
C2045	281-0605-00	X3		200 pF	Cer	500 V	
C2064	281-0525-00			470 pF	Cer	500 V	
C2072	281-0525-00			470 pF	Cer	500 V	
C2073	281-0536-00			1000 pF	Cer	500 V	10%
C2081	281-0536-00			1000 pF	Cer	500 V	10%
C2083	281-0536-00			1000 pF	Cer	500 V	10%
C2093	283-0110-00			0.005 μF	Cer	150 V	
C2113	283-0110-00			0.005 μF	Cer	150 V	

CLOCK CARD Series E (cont)

Capacitors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
C2121	290-0267-00	X3		1 μF	Elect.	35 V	
C2122	290-0267-00	X3		1 μF	Elect.	35 V	
C2124	290-0267-00	X2		1 μf	Elect.	35 V	
C2126	281-0536-00	1	2	1000 pF	Cer	500 V	10%
C2126	281-0523-00	3		100 pF	Cer	350 V	
C2128	281-0536-00	1	2	1000 pF	Cer	500 V	10%
C2128	281-0523-00	3		100 pF	Cer	350 V	
C2131	281-0518-00			47 pF	Cer	500 V	
C2144	283-0110-00	X3		0.005 μF	Cer	150 V	
C2163	283-0110-00			0.005 μF	Cer	150 V	

Diodes

D2011	*152-0185-00		Silicon	Replaceable by 1N4152
D2016	*152-0185-00		Silicon	Replaceable by 1N4152
D2021	*152-0185-00	X3	Silicon	Replaceable by 1N4152
D2022	*152-0185-00		Silicon	Replaceable by 1N4152
D2023	*152-0185-00		Silicon	Replaceable by 1N4152
D2024	*152-0185-00	X3	Silicon	Replaceable by 1N4152
D2025	*152-0185-00	X3	Silicon	Replaceable by 1N4152
D2035	*152-0185-00	X3	Silicon	Replaceable by 1N4152
D2051	*152-0185-00		Silicon	Replaceable by 1N4152
D2054	*152-0185-00		Silicon	Replaceable by 1N4152
D2056	*152-0185-00		Silicon	Replaceable by 1N4152
D2060	*152-0185-00	X3	Silicon	Replaceable by 1N4152
D2062	*152-0185-00		Silicon	Replaceable by 1N4152
D2063	*152-0185-00		Silicon	Replaceable by 1N4152
D2091	*152-0185-00		Silicon	Replaceable by 1N4152
D2111	*152-0185-00		Silicon	Replaceable by 1N4152
D2141	*152-0185-00		Silicon	Replaceable by 1N4152
D2161	*152-0185-00		Silicon	Replaceable by 1N4152

Integrated Circuits

M2018	156-0002-00		J-K Flipflop	Replaceable by Motorola MC358AG
M2045	156-0003-00	X3	3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M2074	156-0003-00		3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M2076	156-0007-00		R-S Flipflop	Replaceable by Motorola MC352G
M2078	156-0003-00		3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G

CLOCK CARD Series E (cont)

Integrated Circuits *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
M2080	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2082	156-0006-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Motorola MC360G
M2084	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2086	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2090	156-0006-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Motorola MC360G
M2094	156-0006-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Motorola MC360G
M2098	156-0006-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Motorola MC360G
M2100	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2102	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2104	156-0003-00			3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M2106	156-0003-00			3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M2108	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2110	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2120	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2124	156-0006-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Motorola MC360G
M2126	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M2128	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M2140	156-0006-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Motorola MC360G
M2144	156-0006-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Motorola MC360G
M2148	156-0006-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Motorola MC360G
M2150	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2152	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2154	156-0003-00			3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M2156	156-0003-00			3-Input AND/NAND-OR/NOR Gate	Replaceable by Motorola MC357G
M2158	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG

CLOCK CARD Series E (cont)

Integrated Circuits *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
M2160	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2170	156-0002-00			J-K Flipflop	Replaceable by Motorola MC358AG
M2172	156-0006-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Motorola MC360G
M2178	156-0004-00			Bias Driver	Replaceable by Motorola MC354G

Transistors

Q2021	151-0190-00	1	5	Silicon	2N3904
Q2021	*151-0190-01	6		Silicon	Tek Spec
Q2025	151-0190-00	1	5	Silicon	2N3904
Q2025	*151-0190-01	6		Silicon	Tek Spec
Q2029	151-0190-00	X3	5	Silicon	2N3904
Q2029	*151-0190-01	6		Silicon	Tek Spec
Q2031	151-0190-00	1	5	Silicon	2N3904
Q2031	*151-0190-01	6		Silicon	Tek Spec
Q2035	151-0190-00	X3	5	Silicon	2N3904
Q2035	*151-0190-01	6		Silicon	Tek Spec
Q2045	151-0190-00	1	2X	Silicon	2N3904
Q2054	151-0188-00	1	5	Silicon	2N3906
Q2054	151-0220-00	6		Silicon	2N4122
Q2066	151-0188-00	1	5	Silicon	2N3906
Q2066	151-0220-00	6		Silicon	2N4122
Q2072	151-0188-00	1	5	Silicon	2N3906
Q2072	151-0220-00	6		Silicon	2N4122
Q2079	151-0190-00	1	5	Silicon	2N3904
Q2079	*151-0190-01	6		Silicon	Tek Spec
Q2095	151-0190-00	1	5	Silicon	2N3904
Q2095	*151-0190-01	6		Silicon	Tek Spec
Q2117	151-0190-00	1	5	Silicon	2N3904
Q2117	*151-0190-01	6		Silicon	Tek Spec
Q2145	151-0190-00	1	5	Silicon	2N3904
Q2145	*151-0190-01	6		Silicon	Tek Spec
Q2167	151-0190-00	1	5	Silicon	2N3904
Q2167	*151-0190-01	6		Silicon	Tek Spec

Resistors

Resistors are fixed, composition, ±10% unless otherwise indicated.

R2013	315-0432-00		4.3 kΩ	1/4 W	5%
R2014	315-0362-00		3.6 kΩ	1/4 W	5%
R2015	315-0302-00		3 kΩ	1/4 W	5%
R2018	315-0472-00		4.7 kΩ	1/4 W	5%
R2020	315-0471-00	X3	470 Ω	1/4 W	5%

CLOCK CARD Series E (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R2021	315-0242-00			2.4 kΩ	1/4 W	5%
R2022	315-0102-00	X3		1 kΩ	1/4 W	5%
R2023	315-0823-00	1	2	82 kΩ	1/4 W	5%
R2023	321-0334-00	3		29.4 kΩ	1/8 W Prec	1%
R2024	315-0563-00	1	2	56 kΩ	1/4 W	5%
R2024	315-0203-00	3		20 kΩ	1/4 W	5%
R2025	315-0361-00	1	2	360 Ω	1/4 W	5%
R2025	315-0182-00	3		1.8 kΩ	1/4 W	5%
R2026	321-0335-00	X3		30.1 kΩ	1/8 W Prec	1%
R2027	315-0391-00	1	2X	390 Ω	1/4 W	5%
R2028	315-0103-00	1	2X	10 kΩ	1/4 W	5%
R2029	315-0621-00	1	2X	620 Ω	1/4 W	5%
R2030	315-0182-00	X3		1.8 kΩ	1/4 W	5%
R2031	315-0431-00	1	2	430 Ω	1/4 W	5%
R2031	315-0122-00	3		1.2 kΩ	1/4 W	5%
R2035	315-0103-00	X3		10 kΩ	1/4 W	5%
R2041	315-0623-00			62 kΩ	1/4 W	5%
R2042	315-0183-00			18 kΩ	1/4 W	5%
R2043	315-0154-00	1	6	150 kΩ	1/4 W	5%
R2043	321-0414-00	7		200 kΩ	1/8 W Prec	1%
R2045	315-0103-00	1	2X	10 kΩ	1/4 W	5%
R2046	315-0203-00	1	2	20 kΩ	1/4 W	5%
R2046	315-0122-00	3		1.2 kΩ	1/4 W	5%
R2048	315-0102-00	X3		1 kΩ	1/4 W	5%
R2049	315-0472-00	X3		4.7 kΩ	1/4 W	5%
R2051	315-0512-00			5.1 kΩ	1/4 W	5%
R2052	315-0302-00			3 kΩ	1/4 W	5%
R2053	315-0432-00			4.3 kΩ	1/4 W	5%
R2054	315-0563-00			56 kΩ	1/4 W	5%
R2060	315-0203-00	X3		20 kΩ	1/4 W	5%
R2061	315-0563-00	1	2	56 kΩ	1/4 W	5%
R2061	315-0363-00	3		36 kΩ	1/4 W	5%
R2062	315-0363-00			36 kΩ	1/4 W	5%
R2063	315-0203-00			20 kΩ	1/4 W	5%
R2064	315-0242-00			2.4 kΩ	1/4 W	5%
R2065	315-0242-00			2.4 kΩ	1/4 W	5%
R2067	315-0563-00	1	3	56 kΩ	1/4 W	5%
R2067	315-0303-00	4		30 kΩ	1/4 W	5%
R2068	315-0203-00	1	3	20 kΩ	1/4 W	5%
R2068	315-0123-00	4		12 kΩ	1/4 W	5%
R2069	315-0102-00			1 kΩ	1/4 W	5%
R2071	315-0202-00	1	2X	2 kΩ	1/4 W	5%
R2072	315-0393-00			39 kΩ	1/4 W	5%
R2073	315-0272-00			2.7 kΩ	1/4 W	5%
R2074	315-0362-00			3.6 kΩ	1/4 W	5%
R2076	315-0392-00			3.9 kΩ	1/4 W	5%

CLOCK CARD Series E (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R2077	315-0242-00			2.4 kΩ	1/4 W	5%
R2079	315-0272-00			2.7 kΩ	1/4 W	5%
R2091	315-0682-00			6.8 kΩ	1/4 W	5%
R2092	315-0303-00			30 kΩ	1/4 W	5%
R2093	315-0393-00			39 kΩ	1/4 W	5%
R2094	315-0392-00			3.9 kΩ	1/4 W	5%
R2096	315-0562-00			5.6 kΩ	1/4 W	5%
R2104	315-0272-00			2.7 kΩ	1/4 W	5%
R2106	315-0272-00			2.7 kΩ	1/4 W	5%
R2111	315-0512-00			5.1 kΩ	1/4 W	5%
R2112	315-0302-00			3 kΩ	1/4 W	5%
R2113	315-0432-00			4.3 kΩ	1/4 W	5%
R2116	315-0392-00			3.9 kΩ	1/4 W	5%
R2117	315-0562-00			5.6 kΩ	1/4 W	5%
R2121	315-0102-00			1 kΩ	1/4 W	5%
R2122	315-0102-00			1 kΩ	1/4 W	5%
R2124	315-0272-00	1		2.7 kΩ	1/4 W	5%
R2124	315-0222-00	2		2.2 kΩ	1/4 W	5%
R2126	315-0201-00	X3		200 Ω	1/4 W	5%
R2128	315-0201-00	X3		200 Ω	1/4 W	5%
R2131	315-0393-00			39 kΩ	1/4 W	5%
R2132	315-0393-00			39 kΩ	1/4 W	5%
R2141	315-0682-00			6.8 kΩ	1/4 W	5%
R2142	315-0303-00			30 kΩ	1/4 W	5%
R2143	315-0393-00			39 kΩ	1/4 W	5%
R2144	315-0392-00			3.9 kΩ	1/4 W	5%
R2146	315-0562-00			5.6 kΩ	1/4 W	5%
R2154	315-0272-00			2.7 kΩ	1/4 W	5%
R2156	315-0272-00			2.7 kΩ	1/4 W	5%
R2161	315-0512-00			5.1 kΩ	1/4 W	5%
R2162	315-0302-00			3 kΩ	1/4 W	5%
R2163	315-0432-00			4.3 kΩ	1/4 W	5%
R2166	315-0392-00			3.9 kΩ	1/4 W	5%
R2167	315-0562-00			5.6 kΩ	1/4 W	5%

Crystals

Y2071	158-0031-00	1	4	10 MHz
Y2071	158-0031-01	5		10 MHz
Y2072	158-0025-00	1	2	1 MHz
Y2072	158-0014-00	3		10 kHz

SYNCHRONIZER CARD Series F

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
	*670-0236-00			Complete Card			
				Capacitors			
Tolerance ±20% unless otherwise indicated.							
C1701	290-0284-00	X3	5	4.7 μF	Elect.	35 V	10%
C1701	290-0395-00	6		4.7 μF	Elect.	50 V	
C1710	283-0079-00	X3		0.01 μF	Cer	250 V	
C1714	283-0110-00			0.005 μF	Cer	150 V	
C1718	283-0110-00			0.005 μF	Cer	150 V	
C1719	281-0523-00	1	2	100 pF	Cer	350 V	
C1719	283-0060-00	3		100 pF	Cer	200 V	5%
C1723	283-0110-00			0.005 μF	Cer	150 V	
C1726	281-0536-00	1	2	1000 pF	Cer	500 V	10%
C1726	283-0001-00	3		0.005 μF	Cer	500 V	
C1727	283-0111-00	1	2	0.1 μF	Cer	50 V	
C1727	283-0081-00	3		0.1 μF	Cer	25 V	+80%--20%
C1731	283-0110-00			0.005 μF	Cer	150 V	
C1757	283-0003-00	1	2	0.01 μF	Cer	150 V	
C1757	283-0079-00	3		0.01 μF	Cer	250 V	
C1758	281-0523-00	1		100 pF	Cer	350 V	
C1758	281-0525-00	2		470 pF	Cer	500 V	
C1758	283-0032-00	3		470 pF	Cer	500 V	5%
C1761	283-0059-00	X3		1 μF	Cer	25 V	
C1771	283-0079-00	X3		0.1 μF	Cer	250 V	
C1784	281-0536-00	1	2	1000 pF	Cer	500 V	10%
C1784	283-0067-00	3		0.001 μF	Cer	200 V	10%
C1787	285-0576-00			1 μF	PTM	100 V	10%
C1790	283-0059-00	X3		1 μF	Cer	25 V	
C1801	283-0110-00			0.005 μF	Cer	150 V	
C1811	281-0536-00	1	2	1000 pF	Cer	500 V	10%
C1811	283-0067-00	3		0.001 μF	Cer	200 V	10%
C1815	283-0067-00	X3		0.001 μF	Cer	200 V	10%
C1825	283-0067-00	X3		0.001 μF	Cer	200 V	10%
C1833	283-0110-00	1	2X	0.005 μF	Cer	150 V	
C1835	283-0003-00	1	2X	0.01 μF	Cer	150 V	
C1843	283-0110-00	X3		0.005 μF	Cer	150 V	
				Diodes			
D1702	*152-0322-00	X3		Silicon	Tek Spec		
D1703	*152-0185-00	X3		Silicon	Replaceable by 1N4152		
D1713	*152-0185-00			Silicon	Replaceable by 1N4152		
D1718	*152-0185-00	1	2	Silicon	Replaceable by 1N4152		
D1718	*152-0322-00	3		Silicon	Tek Spec		
D1731	*152-0185-00			Silicon	Replaceable by 1N4152		
D1732	*152-0185-00	X3		Silicon	Replaceable by 1N4152		
D1734	*152-0185-00			Silicon	Replaceable by 1N4152		
D1737	*152-0185-00	X3		Silicon	Replaceable by 1N4152		
D1738	*152-0185-00	X3		Silicon	Replaceable by 1N4152		

SYNCHRONIZER CARD Series F (cont)

Diodes *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
D1739	*152-0185-00	X3		Silicon	Replaceable by 1N4152
D1770	*152-0322-00	X3		Silicon	Tek Spec
D1774	*152-0185-00	X3		Silicon	Replaceable by 1N4152
D1777	*152-0185-00	X3		Silicon	Replaceable by 1N4152
D1778	*152-0185-00	X3		Silicon	Replaceable by 1N4152
D1779	*152-0185-00	X3		Silicon	Replaceable by 1N4152
D1781	*152-0185-00			Silicon	Replaceable by 1N4152
D1784	*152-0185-00			Silicon	Replaceable by 1N4152
D1785	*152-0185-00			Silicon	Replaceable by 1N4152
D1788	*152-0185-00			Silicon	Replaceable by 1N4152
D1794	*152-0185-00	X3		Silicon	Replaceable by 1N4152

Integrated Circuits

M1714	156-0011-00	X3		Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1716	156-0011-00	X3		Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1718	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1720	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M1722	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1724	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1728	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1736	156-0011-00	X3		Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1740	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M1742	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M1744	156-0012-00			Clocked J-K Flipflop	Replaceable by Fairchild μL923
M1746	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1748	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1756	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1758	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1760	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1762	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1764	156-0012-00	X3		Clocked J-K Flipflop	Replaceable by Fairchild μL923
M1768	156-0010-00			Buffer-Inverter	Replaceable by Fairchild μL900
M1770	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914

SYNCHRONIZER CARD Series F (cont)

Integrated Circuits *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
M1790	156-0012-00	X3		Clocked J-K Flipflop	Replaceable by Fairchild μL923
M1794	156-0011-00	X3		Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1804	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1810	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1812	156-0011-00			Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1832	156-0011-00	1	2X	Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914
M1836	156-0011-00	1	2X	Dual 2-Input NAND/ NOR Gate	Replaceable by Fairchild μL914

Transistors

Q1718	151-0188-00	X3	4	Silicon	2N3906
Q1718	151-0220-00	5		Silicon	2N4122
Q1729	151-0190-00	1	4	Silicon	2N3904
Q1729	*151-0190-01	5		Silicon	Tek Spec
Q1732	151-0188-00	X3	4	Silicon	2N3906
Q1732	151-0220-00	5		Silicon	2N4122
Q1737	151-0190-00	1	4	Silicon	2N3904
Q1737	*151-0190-01	5		Silicon	Tek Spec
Q1738	151-0188-00	X3	4	Silicon	2N3906
Q1738	151-0220-00	5		Silicon	2N4122
Q1739	151-0190-00	X3	4	Silicon	2N3904
Q1739	*151-0190-01	5		Silicon	Tek Spec
Q1741	151-0190-00	1	4	Silicon	2N3904
Q1741	*151-0190-01	5		Silicon	Tek Spec
Q1752	151-0188-00	1	4	Silicon	2N3906
Q1752	151-0220-00	5		Silicon	2N4122
Q1766	151-0188-00	1	4	Silicon	2N3906
Q1766	151-0220-00	5		Silicon	2N4122
Q1771	151-0190-00	1	4	Silicon	2N3904
Q1771	*151-0190-01	5		Silicon	Tek Spec
Q1774	151-0188-00	1	4	Silicon	2N3906
Q1774	151-0220-00	5		Silicon	2N4122
Q1777	151-0190-00	1	4	Silicon	2N3904
Q1777	*151-0190-01	5		Silicon	Tek Spec
Q1778	151-0188-00	X3	4	Silicon	2N3906
Q1778	151-0220-00	5		Silicon	2N4122
Q1779	151-0190-00	X3	4	Silicon	2N3904
Q1779	*151-0190-01	5		Silicon	Tek Spec
Q1785	151-0190-00	1	4	Silicon	2N3904
Q1785	*151-0190-01	5		Silicon	Tek Spec

SYNCHRONIZER CARD Series F (cont)

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc		Description
Q1787	151-1005-00	1	6	Silicon	FET
Q1787	151-1004-00	7		Silicon	FET
Q1794	151-0188-00	1	4	Silicon	2N3906
Q1794	151-0220-00	5		Silicon	2N4122
Q1795	151-0190-00	1	4	Silicon	2N3904
Q1795	*151-0190-01	5		Silicon	Tek Spec
Q1806	151-0188-00	1	4	Silicon	2N3906
Q1806	151-0220-00	5		Silicon	2N4122
Q1815	151-0190-00	1	4	Silicon	2N3904
Q1815	*151-0190-01	5		Silicon	Tek Spec
Q1817	151-0190-00	1	4	Silicon	2N3904
Q1817	*151-0190-01	5		Silicon	Tek Spec
Q1825	151-0190-00	1	4	Silicon	2N3904
Q1825	*151-0190-01	5		Silicon	Tek Spec
Q1827	151-0190-00	1	4	Silicon	2N3904
Q1827	*151-0190-01	5		Silicon	Tek Spec
Q1836	151-0188-00	1	2X	Silicon	2N3906
Q1844	151-0188-00	1	2X	Silicon	2N3906

Resistors

Resistors are fixed, composition, ±10% unless otherwise indicated.

R1701	315-0123-00	X3		12 kΩ	1/4 W	5%
R1702	315-0472-00	X3		4.7 kΩ	1/4 W	5%
R1710	315-0562-00	X3		5.6 kΩ	1/4 W	5%
R1711	315-0202-00	X3		2 kΩ	1/4 W	5%
R1712	315-0751-00	X3		750 Ω	1/4 W	5%
R1713	315-0123-00			12 kΩ	1/4 W	5%
R1714	315-0104-00	1	2	100 kΩ	1/4 W	5%
R1714	315-0243-00	3		24 kΩ	1/4 W	5%
R1715	315-0272-00	1	2	2.7 kΩ	1/4 W	5%
R1715	315-0392-00	3		3.9 kΩ	1/4 W	5%
R1718	315-0103-00			10 kΩ	1/4 W	5%
R1719	315-0102-00			1 kΩ	1/4 W	5%
R1720	315-0622-00	1	7	6.2 kΩ	1/4 W	5%
R1720	315-0472-00	8		4.7 kΩ	1/4 W	5%
R1722	315-0102-00	X8		1 kΩ	1/4 W	5%
R1723	315-0392-00			3.9 kΩ	1/4 W	5%
R1724	315-0562-00	1	2X	5.6 kΩ	1/4 W	5%
R1726	315-0102-00	1	2	1 kΩ	1/4 W	5%
R1726	315-0562-00	3		5.6 kΩ	1/4 W	5%
R1727	315-0332-00			3.3 kΩ	1/4 W	5%
R1728	315-0102-00			1 kΩ	1/4 W	5%
R1729	315-0302-00			3 kΩ	1/4 W	5%
R1731	315-0104-00	1	2	100 kΩ	1/4 W	5%
R1731	315-0123-00	3		12 kΩ	1/4 W	5%
R1732	315-0392-00	1	2	3.9 kΩ	1/4 W	5%
R1732	315-0201-00	3		200 Ω	1/4 W	5%
R1733	315-0243-00	X3		24 kΩ	1/4 W	5%

SYNCHRONIZER CARD Series F (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R1734	315-0302-00			3 kΩ	1/4 W	5%
R1735	315-0222-00			2.2 kΩ	1/4 W	5%
R1736	315-0392-00			3.9 kΩ	1/4 W	5%
R1737	315-0751-00			750 Ω	1/4 W	5%
R1738	315-0361-00			360 Ω	1/4 W	5%
R1739	315-0102-00			1 kΩ	1/4 W	5%
R1741	315-0391-00			390 Ω	1/4 W	5%
R1742	315-0102-00			1 kΩ	1/4 W	5%
R1749	315-0102-00			1 kΩ	1/4 W	5%
R1751	315-0392-00			3.9 kΩ	1/4 W	5%
R1752	315-0102-00			1 kΩ	1/4 W	5%
R1754	315-0101-00			100 Ω	1/4 W	5%
R1755	315-0622-00			6.2 kΩ	1/4 W	5%
R1757	315-0102-00			1 kΩ	1/4 W	5%
R1758	315-0102-00			1 kΩ	1/4 W	5%
R1761	315-0102-00	X3		1 kΩ	1/4 W	5%
R1762	315-0471-00	X3		470 Ω	1/4 W	5%
R1763	315-0202-00	X3		2 kΩ	1/4 W	5%
R1764	315-0222-00			2.2 kΩ	1/4 W	5%
R1765	315-0202-00	X3		2 kΩ	1/4 W	5%
R1766	315-0392-00			3.9 kΩ	1/4 W	5%
R1767	315-0102-00			1 kΩ	1/4 W	5%
R1768	315-0272-00			2.7 kΩ	1/4 W	5%
R1769	315-0272-00			2.7 kΩ	1/4 W	5%
R1771	315-0471-00	1	2	470 Ω	1/4 W	5%
R1771	315-0272-00	3		2.7 kΩ	1/4 W	5%
R1772	315-0101-00			100 Ω	1/4 W	5%
R1773	315-0821-00			820 Ω	1/4 W	5%
R1774	315-0272-00	1	2	2.7 kΩ	1/4 W	5%
R1774	315-0471-00	3		470 Ω	1/4 W	5%
R1775	315-0123-00			12 kΩ	1/4 W	5%
R1776	315-0222-00			2.2 kΩ	1/4 W	5%
R1778	315-0513-00			51 kΩ	1/4 W	5%
R1779	315-0244-00			240 kΩ	1/4 W	5%
R1780	311-0496-00			2.5 kΩ, Var		
R1781	315-0101-00			100 Ω	1/4 W	5%
R1783	315-0303-00			30 kΩ	1/4 W	5%
R1784	315-0303-00			30 kΩ	1/4 W	5%
R1787	315-0303-00			30 kΩ	1/4 W	5%
R1788	315-0222-00			2.2 kΩ	1/4 W	5%
R1789	315-0683-00			68 kΩ	1/4 W	5%
R1790	315-0222-00	X3		2.2 kΩ	1/4 W	5%
R1791	315-0622-00			6.2 kΩ	1/4 W	5%
R1792	315-0272-00			2.7 kΩ	1/4 W	5%
R1793	315-0472-00			4.7 kΩ	1/4 W	5%

SYNCHRONIZER CARD Series F (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R1794	315-0471-00			470 Ω	1/4 W	5%
R1795	315-0272-00			2.7 kΩ	1/4 W	5%
R1796	315-0102-00			1 kΩ	1/4 W	5%
R1802	315-0102-00			1 kΩ	1/4 W	5%
R1805	315-0102-00			1 kΩ	1/4 W	5%
R1806	315-0102-00			1 kΩ	1/4 W	5%
R1808	315-0222-00			2.2 kΩ	1/4 W	5%
R1810	315-0392-00			3.9 kΩ	1/4 W	5%
R1811	315-0102-00			1 kΩ	1/4 W	5%
R1813	315-0681-00			680 Ω	1/4 W	5%
R1814	315-0471-00			470 Ω	1/4 W	5%
R1815	315-0123-00			12 kΩ	1/4 W	5%
R1817	315-0473-00			47 kΩ	1/4 W	5%
R1818	315-0243-00			24 kΩ	1/4 W	5%
R1819	315-0333-00			33 kΩ	1/4 W	5%
R1824	315-0471-00			470 Ω	1/4 W	5%
R1825	315-0123-00			12 kΩ	1/4 W	5%
R1827	315-0473-00			47 kΩ	1/4 W	5%
R1828	315-0243-00			24 kΩ	1/4 W	5%
R1829	315-0333-00			33 kΩ	1/4 W	5%
R1831	315-0272-00	1	2X	2.7 kΩ	1/4 W	5%
R1832	315-0682-00	1	2X	6.8 kΩ	1/4 W	5%
R1833	315-0102-00	1	2X	1 kΩ	1/4 W	5%
R1835	315-0123-00	1	2X	12 kΩ	1/4 W	5%
R1836	315-0472-00	1	2X	4.7 kΩ	1/4 W	5%
R1837	315-0394-00	1	2X	390 kΩ	1/4 W	5%
R1839	315-0823-00	1	2X	82 kΩ	1/4 W	5%
R1841	315-0272-00	1	2	2.7 kΩ	1/4 W	5%
R1841	315-0202-00	3		2 kΩ	1/4 W	5%
R1842	315-0751-00	1	2	750 Ω	1/4 W	5%
R1842	315-0122-00	3		1.2 kΩ	1/4 W	5%
R1843	315-0392-00	1	2	3.9 kΩ	1/4 W	5%
R1843	315-0242-00	3		2.4 kΩ	1/4 W	5%
R1845	315-0394-00	1	2X	390 kΩ	1/4 W	5%
R1846	315-0823-00	1	2X	82 kΩ	1/4 W	5%

CRT INTENS/REGULATOR CARD Series G

*670-0237-00	Complete Card	

Capacitors

Tolerance ±20% unless otherwise indicated.

C224	290-0245-00	1.5 μF	Elect.	10 V	10%
C229	290-0177-00	1 μF	Elect.	50 V	
C244	283-0003-00	0.01 μF	Cer	150 V	
C256	283-0003-00	0.01 μF	Cer	150 V	
C287	283-0003-00	0.01 μF	Cer	150 V	

CRT INTENS/REGULATOR CARD Series G (cont)

Capacitors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
C322	283-0111-00			0.1 μF Cer 50 V
C323	283-0111-00			0.1 μF Cer 50 V
C344	283-0003-00			0.01 μF Cer 150 V
C373	283-0003-00			0.01 μF Cer 150 V

Diodes

D23	*152-0185-00			Silicon Replaceable by 1N4152
D25	*152-0185-00			Silicon Replaceable by 1N4152
D33	*152-0185-00			Silicon Replaceable by 1N4152
D35	*152-0185-00			Silicon Replaceable by 1N4152
D43	*152-0185-00			Silicon Replaceable by 1N4152
D45	*152-0185-00			Silicon Replaceable by 1N4152
D53	*152-0185-00			Silicon Replaceable by 1N4152
D55	*152-0185-00			Silicon Replaceable by 1N4152
D61	*152-0185-00			Silicon Replaceable by 1N4152
D62	*152-0185-00			Silicon Replaceable by 1N4152
D65	*152-0185-00			Silicon Replaceable by 1N4152
D66	*152-0185-00			Silicon Replaceable by 1N4152
D67	*152-0185-00			Silicon Replaceable by 1N4152
D71	*152-0185-00			Silicon Replaceable by 1N4152
D72	*152-0185-00			Silicon Replaceable by 1N4152
D75	*152-0185-00			Silicon Replaceable by 1N4152
D76	*152-0185-00			Silicon Replaceable by 1N4152
D77	*152-0185-00			Silicon Replaceable by 1N4152
D107	*152-0185-00	X2		Silicon Replaceable by 1N4152
D111	*152-0185-00			Silicon Replaceable by 1N4152
D113	*152-0185-00	X2		Silicon Replaceable by 1N4152
D116	*152-0185-00			Silicon Replaceable by 1N4152
D124	*152-0185-00			Silicon Replaceable by 1N4152
D224	*152-0185-00			Silicon Replaceable by 1N4152
D225	152-0212-00			Zener 1N936 9 V, 5%, TC
D235	*152-0061-00			Silicon Tek Spec
D310	*152-0185-00			Silicon Replaceable by 1N4152
D311	*152-0185-00			Silicon Replaceable by 1N4152
D333	*152-0185-00			Silicon Replaceable by 1N4152
D338	*152-0185-00			Silicon Replaceable by 1N4152
D342	152-0066-00			Silicon 1N3194
D366	*152-0185-00			Silicon Replaceable by 1N4152

Transistors

Q11	151-0190-00	X2		Silicon 2N3904
Q11	*151-0190-01	3		Silicon Tek Spec
Q12	151-0188-00		1X	Silicon 2N3906
Q13	151-0190-00	1	2	Silicon 2N3904
Q13	*151-0190-01	3		Silicon Tek Spec

CRT INTENS/REGULATOR CARD Series G (cont)

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc		Description
Q21	151-0190-00	1	2	Silicon	2N3904
Q21	*151-0190-01	3		Silicon	Tek Spec
Q26	151-0188-00	1	2	Silicon	2N3906
Q26	151-0220-00	3		Silicon	2N4122
Q31	151-0190-00	1	2	Silicon	2N3904
Q31	*151-0190-01	3		Silicon	Tek Spec
Q36	151-0188-00	1	2	Silicon	2N3906
Q36	151-0220-00	3		Silicon	2N4122
Q41	151-0190-00	1	2	Silicon	2N3904
Q41	*151-0190-01	3		Silicon	Tek Spec
Q46	151-0188-00	1	2	Silicon	2N3906
Q46	151-0220-00	3		Silicon	2N4122
Q51	151-0190-00	1	2	Silicon	2N3904
Q51	*151-0190-01	3		Silicon	Tek Spec
Q56	151-0188-00	1	2	Silicon	2N3906
Q56	151-0220-00	3		Silicon	2N4122
Q61	151-0190-00	1	2	Silicon	2N3904
Q61	*151-0190-01	3		Silicon	Tek Spec
Q63	151-0190-00	1	2	Silicon	2N3904
Q63	*151-0190-01	3		Silicon	Tek Spec
Q66	151-0188-00	1	2	Silicon	2N3906
Q66	151-0220-00	3		Silicon	2N4122
Q71	151-0190-00	1	2	Silicon	2N3904
Q71	*151-0190-01	3		Silicon	Tek Spec
Q73	151-0190-00	1	2	Silicon	2N3904
Q73	*151-0190-01	3		Silicon	Tek Spec
Q76	151-0188-00	1	2	Silicon	2N3906
Q76	151-0220-00	3		Silicon	2N4122
Q103	151-0190-00	1	2	Silicon	2N3904
Q103	*151-0190-01	3		Silicon	Tek Spec
Q107	151-0190-00	1	2	Silicon	2N3904
Q107	*151-0190-01	3		Silicon	Tek Spec
Q111	151-0188-00	X2		Silicon	2N3906
Q111	151-0220-00	3		Silicon	2N4122
Q113	151-0190-00	1	2	Silicon	2N3904
Q113	*151-0190-01	3		Silicon	Tek Spec
Q123	151-0190-00	1	2	Silicon	2N3904
Q123	*151-0190-01	3		Silicon	Tek Spec
Q133	151-0190-00	1	2	Silicon	2N3904
Q133	*151-0190-01	3		Silicon	Tek Spec
Q143	151-0190-00	1	2	Silicon	2N3904
Q143	*151-0190-01	3		Silicon	Tek Spec
Q147	151-0190-00	1	2	Silicon	2N3904
Q147	*151-0190-01	3		Silicon	Tek Spec
Q222	151-0188-00	1	2	Silicon	2N3906

CRT INTENS/REGULATOR CARD Seires G (cont)

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc		Description
Q222	151-0220-00	3		Silicon	2N4122
Q224	151-0188-00	1	2	Silicon	2N3906
Q224	151-0220-00	3		Silicon	2N4122
Q234	151-0188-00	1	2	Silicon	2N3906
Q234	151-0220-00	3		Silicon	2N4122
Q244	151-0208-00			Silicon	2N4036
Q253	*151-0136-00			Silicon	Replaceable by 2N3053
Q261	151-0190-00	1	2	Silicon	2N3904
Q261	*151-0190-01	3		Silicon	Tek Spec
Q263	151-0190-00	1	2	Silicon	2N3904
Q263	*151-0190-01	3		Silicon	Tek Spec
Q273	151-0190-00	1	2	Silicon	2N3904
Q273	*151-0190-01	3		Silicon	Tek Spec
Q283	*151-0136-00			Silicon	Replaceable by 2N3053
Q291	151-0190-00	1	2	Silicon	2N3904
Q291	*151-0190-01	3		Silicon	Tek Spec
Q293	151-0190-00	1	2	Silicon	2N3904
Q293	*151-0190-01	3		Silicon	Tek Spec
Q303	151-0190-00	1	2	Silicon	2N3904
Q303	*151-0190-01	3		Silicon	Tek Spec
Q311	151-0190-00	1	2	Silicon	2N3904
Q311	*151-0190-01	3		Silicon	Tek Spec
Q313	151-0190-00	1	2	Silicon	2N3904
Q313	*151-0190-01	3		Silicon	Tek Spec
Q323	151-0190-00	1	2	Silicon	2N3904
Q323	*151-0190-01	3		Silicon	Tek Spec
Q332	151-0188-00	1	2	Silicon	2N3906
Q332	151-0220-00	3		Silicon	2N4122
Q334	151-0188-00	1	2	Silicon	2N3906
Q334	151-0220-00	3		Silicon	2N4122
Q342	151-0188-00	1	2	Silicon	2N3906
Q342	151-0220-00	3		Silicon	2N4122
Q344	151-0208-00			Silicon	2N4036
Q361	151-0190-00	1	2	Silicon	2N3904
Q361	*151-0190-01	3		Silicon	Tek Spec
Q363	151-0190-00	1	2	Silicon	2N3904
Q363	*151-0190-01	3		Silicon	Tek Spec
Q374	151-0188-00	1	2	Silicon	2N3906
Q374	151-0220-00	3		Silicon	2N4122
Q383	151-0190-00	1	2	Silicon	2N3904
Q383	*151-0190-01	3		Silicon	Tek Spec

CRT INTENS/REGULATOR CARD Series G (cont)

Resistors

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
Resistors are fixed, composition, ±10% unless otherwise indicated.						
R11	315-0272-00			2.7 kΩ	1/4 W	5%
R12	315-0202-00	1		2 kΩ	1/4 W	5%
R12	315-0102-00	2		1 kΩ	1/4 W	5%
R13	315-0272-00			2.7 kΩ	1/4 W	5%
R14	315-0103-00	X2		10 kΩ	1/4 W	5%
R15	315-0243-00			24 kΩ	1/4 W	5%
R16	315-0472-00			4.7 kΩ	1/4 W	5%
R18	315-0243-00			24 kΩ	1/4 W	5%
R19	315-0472-00			4.7 kΩ	1/4 W	5%
R21	315-0104-00			100 kΩ	1/4 W	5%
R22	315-0472-00			4.7 kΩ	1/4 W	5%
R29	315-0243-00			24 kΩ	1/4 W	5%
R31	315-0104-00			100 kΩ	1/4 W	5%
R32	315-0472-00			4.7 kΩ	1/4 W	5%
R41	315-0104-00			100 kΩ	1/4 W	5%
R42	315-0472-00			4.7 kΩ	1/4 W	5%
R51	315-0104-00			100 kΩ	1/4 W	5%
R52	315-0472-00			4.7 kΩ	1/4 W	5%
R58	315-0243-00			24 kΩ	1/4 W	5%
R59	315-0472-00			4.7 kΩ	1/4 W	5%
R61	315-0183-00			18 kΩ	1/4 W	5%
R63	315-0104-00			100 kΩ	1/4 W	5%
R64	315-0472-00			4.7 kΩ	1/4 W	5%
R71	315-0183-00			18 kΩ	1/4 W	5%
R74	315-0472-00			4.7 kΩ	1/4 W	5%
R79	315-0271-00			270 Ω	1/4 W	5%
R101	315-0682-00			6.8 kΩ	1/4 W	5%
R102	315-0103-00			10 kΩ	1/4 W	5%
R103	315-0823-00			82 kΩ	1/4 W	5%
R105	315-0392-00			3.9 kΩ	1/4 W	5%
R106	315-0512-00	X2		5.1 kΩ	1/4 W	5%
R107	315-0103-00			10 kΩ	1/4 W	5%
R108	315-0474-00			470 kΩ	1/4 W	5%
R109	315-0474-00			470 kΩ	1/4 W	5%
R111	315-0682-00	1		6.8 kΩ	1/4 W	5%
R111	315-0303-00	2		30 kΩ	1/4 W	5%
R112	315-0113-00	1		11 kΩ	1/4 W	5%
R112	315-0470-00	2		47 Ω	1/4 W	5%
R113	315-0513-00	1		51 kΩ	1/4 W	5%
R113	315-0124-00	2	3	120 kΩ	1/4 W	5%
R113	315-0114-00	4		110 kΩ	1/4 W	5%
R114	315-0333-00			33 kΩ	1/4 W	5%
R115	315-0392-00			3.9 kΩ	1/4 W	5%
R116	315-0243-00			24 kΩ	1/4 W	5%
R118	315-0333-00			33 kΩ	1/4 W	5%
R119	315-0333-00			33 kΩ	1/4 W	5%

CRT INTENS/REGULATOR CARD Series G (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
R121	315-0124-00	1	3	120 kΩ	1/4 W		5%
R121	315-0114-00	4		110 kΩ	1/4 W		5%
R123	315-0392-00			3.9 kΩ	1/4 W		5%
R124	315-0243-00			24 kΩ	1/4 W		5%
R131	315-0333-00			33 kΩ	1/4 W		5%
R132	315-0124-00	1	3	120 kΩ	1/4 W		5%
R132	315-0114-00	4		110 kΩ	1/4 W		5%
R133	315-0333-00			33 kΩ	1/4 W		5%
R135	315-0243-00			24 kΩ	1/4 W		5%
R141	315-0682-00			6.8 kΩ	1/4 W		5%
R142	315-0103-00			10 kΩ	1/4 W		5%
R143	315-0823-00			82 kΩ	1/4 W		5%
R146	315-0333-00			33 kΩ	1/4 W		5%
R147	315-0124-00	1	3	120 kΩ	1/4 W		5%
R147	315-0114-00	4		110 kΩ	1/4 W		5%
R148	315-0333-00			33 kΩ	1/4 W		5%
R149	315-0243-00			24 kΩ	1/4 W		5%
R224	301-0512-00			5.1 kΩ	1/2 W		5%
R225	301-0275-00			2.7 MΩ	1/2 W		5%
R226	315-0470-00			47 Ω	1/4 W		5%
R227	315-0222-00			2.2 kΩ	1/4 W		5%
R228	323-0315-00			18.7 kΩ	1/2 W	Prec	1%
R229	315-0470-00			47 Ω	1/4 W		5%
R230	311-0462-00			1 kΩ, Var			
R231	323-0330-00			26.7 kΩ	1/2 W	Prec	1%
R232	321-0264-00			5.49 kΩ	1/8 W	Prec	1%
R233	315-0273-00			27 kΩ	1/4 W		5%
R234	315-0273-00			27 kΩ	1/4 W		5%
R235	323-0339-00			33.2 kΩ	1/2 W	Prec	1%
R236	315-0101-00			100 Ω	1/4 W		5%
R237	315-0301-00			300 Ω	1/4 W		5%
R238	315-0513-00			51 kΩ	1/4 W		5%
R244	315-0511-00			510 Ω	1/4 W		5%
R255	315-0101-00			100 Ω	1/4 W		5%
R256	315-0101-00			100 Ω	1/4 W		5%
R257	315-0103-00			10 kΩ	1/4 W		5%
R260	311-0480-00			500 Ω, Var			
R261	323-0315-00			18.7 kΩ	1/2 W	Prec	1%
R262	321-0266-00			5.76 kΩ	1/8 W	Prec	1%
R263	315-0470-00			47 Ω	1/4 W		5%
R265	322-0222-00			2 kΩ	1/4 W	Prec	1%
R267	301-0912-00			9.1 kΩ	1/2 W		5%
R268	315-0470-00			47 Ω	1/4 W		5%
R273	315-0151-00			150 Ω	1/4 W		5%
R286	315-0101-00			100 Ω	1/4 W		5%
R287	315-0511-00			510 Ω	1/4 W		5%
R290	311-0480-00			500 Ω, Var			
R291	323-0323-00			22.6 kΩ	1/2 W	Prec	1%

CRT INTENS/REGULATOR CARD Series G (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R292	321-0215-00			1.69 kΩ	1/8 W	Prec 1%
R293	315-0470-00			47 Ω	1/4 W	5%
R296	315-0821-00			820 Ω	1/4 W	5%
R297	315-0222-00			2.2 kΩ	1/4 W	5%
R298	315-0470-00			47 Ω	1/4 W	5%
R310	311-0480-00			500 Ω, Var		
R312	323-0327-00			24.9 kΩ	1/2 W	Prec 1%
R313	315-0470-00			47 Ω	1/4 W	5%
R315	315-0470-00			47 Ω	1/4 W	5%
R316	301-0751-00			750 Ω	1/2 W	5%
R317	315-0132-00			1.3 kΩ	1/4 W	5%
R318	315-0122-00			1.2 kΩ	1/4 W	5%
R322	315-0101-00			100 Ω	1/4 W	5%
R330	311-0462-00			1 kΩ, Var		
R331	323-0356-00			49.9 kΩ	1/2 W	Prec 1%
R332	321-0239-00			3.01 kΩ	1/8 W	Prec 1%
R333	315-0470-00			47 Ω	1/4 W	5%
R335	315-0470-00			47 Ω	1/4 W	5%
R336	321-0239-00			3.01 kΩ	1/8 W	Prec 1%
R337	322-0289-00			10 kΩ	1/4 W	Prec 1%
R338	322-0289-00			10 kΩ	1/4 W	Prec 1%
R341	315-0101-00			100 Ω	1/4 W	5%
R344	315-0511-00			510 Ω	1/4 W	5%
R345	315-0750-00			75 Ω	1/4 W	5%
R360	311-0462-00			1 kΩ, Var		
R361	323-0356-00			49.9 kΩ	1/2 W	Prec 1%
R362	323-0356-00			49.9 kΩ	1/2 W	Prec 1%
R363	315-0101-00			100 Ω	1/4 W	5%
R365	315-0101-00			100 Ω	1/4 W	5%
R366	323-0310-00			16.5 kΩ	1/2 W	Prec 1%
R367	321-0345-00			38.3 kΩ	1/8 W	Prec 1%
R371	315-0101-00			100 Ω	1/4 W	5%
R373	315-0511-00			510 Ω	1/4 W	5%
R374	315-0681-00			680 Ω	1/4 W	5%
R383	315-0513-00			51 kΩ	1/4 W	5%
R384	315-0301-00			300 Ω	1/4 W	5%

LIMIT CARD Series H

	*670-0238-00		Complete Card	

Diodes

D2753	*152-0185-00	Silicon	Replaceable by 1N4152
D2778	*152-0185-00	Silicon	Replaceable by 1N4152
D2814	*152-0185-00	Silicon	Replaceable by 1N4152
D2825	*152-0185-00	Silicon	Replaceable by 1N4152
D2836	*152-0185-00	Silicon	Replaceable by 1N4152

LIMIT CARD Series H (cont)

Diodes *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc		Description
D2845	*152-0185-00			Silicon	Replaceable by 1N4152
D2856	*152-0185-00			Silicon	Replaceable by 1N4152
D2865	*152-0185-00			Silicon	Replaceable by 1N4152
D2876	*152-0185-00			Silicon	Replaceable by 1N4152
D2885	*152-0185-00			Silicon	Replaceable by 1N4152
D2896	*152-0185-00			Silicon	Replaceable by 1N4152
D2905	*152-0185-00			Silicon	Replaceable by 1N4152
D2916	*152-0185-00			Silicon	Replaceable by 1N4152
D2925	*152-0185-00			Silicon	Replaceable by 1N4152
D2936	*152-0185-00			Silicon	Replaceable by 1N4152
D2945	*152-0185-00			Silicon	Replaceable by 1N4152
D2953	*152-0185-00			Silicon	Replaceable by 1N4152
D2973	*152-0185-00			Silicon	Replaceable by 1N4152
D2976	*152-0185-00			Silicon	Replaceable by 1N4152
D2978	*152-0185-00			Silicon	Replaceable by 1N4152

Transistors

Q2613	151-0190-00	1	2	Silicon	2N3904
Q2613	*151-0190-01	3		Silicon	Tek Spec
Q2620	151-0188-00	1	2	Silicon	2N3906
Q2620	151-0220-00	3		Silicon	2N4122
Q2624	151-0188-00	1	2	Silicon	2N3906
Q2624	151-0220-00	3		Silicon	2N4122
Q2631	151-0190-00	1	2	Silicon	2N3904
Q2631	*151-0190-01	3		Silicon	Tek Spec
Q2633	151-0190-00	1	2	Silicon	2N3904
Q2633	*151-0190-01	3		Silicon	Tek Spec
Q2640	151-0188-00	1	2	Silicon	2N3906
Q2640	151-0220-00	3		Silicon	2N4122
Q2644	151-0188-00	1	2	Silicon	2N3906
Q2644	151-0220-00	3		Silicon	2N4122
Q2651	151-0190-00	1	2	Silicon	2N3904
Q2651	*151-0190-01	3		Silicon	Tek Spec
Q2653	151-0190-00	1	2	Silicon	2N3904
Q2653	*151-0190-01	3		Silicon	Tek Spec
Q2660	151-0188-00	1	2	Silicon	2N3906
Q2660	151-0220-00	3		Silicon	2N4122
Q2664	151-0188-00	1	2	Silicon	2N3906
Q2664	151-0220-00	3		Silicon	2N4122
Q2671	151-0190-00	1	2	Silicon	2N3904
Q2671	*151-0190-01	3		Silicon	Tek Spec
Q2673	151-0190-00	1	2	Silicon	2N3904
Q2673	*151-0190-01	3		Silicon	Tek Spec
Q2680	151-0188-00	1	2	Silicon	2N3906
Q2680	151-0220-00	3		Silicon	2N4122
Q2684	151-0188-00	1	2	Silicon	2N3906
Q2684	151-0220-00	3		Silicon	2N4122

LIMIT CARD Series H (cont)

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc		Description
Q2691	151-0190-00	1	2	Silicon	2N3904
Q2691	*151-0190-01	3		Silicon	Tek Spec
Q2693	151-0190-00	1	2	Silicon	2N3904
Q2693	*151-0190-01	3		Silicon	Tek Spec
Q2700	151-0188-00	1	2	Silicon	2N3906
Q2700	151-0220-00	3		Silicon	2N4122
Q2704	151-0188-00	1	2	Silicon	2N3906
Q2704	151-0220-00	3		Silicon	2N4122
Q2711	151-0190-00	1	2	Silicon	2N3904
Q2711	*151-0190-01	3		Silicon	Tek Spec
Q2713	151-0190-00	1	2	Silicon	2N3904
Q2713	*151-0190-01	3		Silicon	Tek Spec
Q2720	151-0188-00	1	2	Silicon	2N3906
Q2720	151-0220-00	3		Silicon	2N4122
Q2724	151-0188-00	1	2	Silicon	2N3906
Q2724	151-0220-00	3		Silicon	2N4122
Q2731	151-0190-00	1	2	Silicon	2N3904
Q2731	*151-0190-01	3		Silicon	Tek Spec
Q2733	151-0190-00	1	2	Silicon	2N3904
Q2733	*151-0190-01	3		Silicon	Tek Spec
Q2740	151-0188-00	1	2	Silicon	2N3906
Q2740	151-0220-00	3		Silicon	2N4122
Q2744	151-0188-00	1	2	Silicon	2N3906
Q2744	151-0220-00	3		Silicon	2N4122
Q2751	151-0190-00	1	2	Silicon	2N3904
Q2751	*151-0190-01	3		Silicon	Tek Spec
Q2753	151-0190-00	1	2	Silicon	2N3904
Q2753	*151-0190-01	3		Silicon	Tek Spec
Q2755	151-0190-00	X2		Silicon	2N3904
Q2755	*151-0190-01	3		Silicon	Tek Spec
Q2760	151-0188-00	1	2	Silicon	2N3906
Q2760	151-0220-00	3		Silicon	2N4122
Q2771	151-0190-00	1	2	Silicon	2N3904
Q2771	*151-0190-01	3		Silicon	Tek Spec
Q2775	151-0188-00	X2		Silicon	2N3906
Q2775	151-0220-00	3		Silicon	2N4122
Q2813	151-0190-00	1	2	Silicon	2N3904
Q2813	*151-0190-01	3		Silicon	Tek Spec
Q2817	151-0190-00	1	2	Silicon	2N3904
Q2817	*151-0190-01	3		Silicon	Tek Spec
Q2820	151-0188-00	1	2	Silicon	2N3906
Q2820	151-0220-00	3		Silicon	2N4122
Q2824	151-0188-00	1	2	Silicon	2N3906
Q2824	151-0220-00	3		Silicon	2N4122
Q2831	151-0190-00	1	2	Silicon	2N3904

LIMIT CARD Series H (cont)

Transistors (cont)

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc		Description
Q2831	*151-0190-01	3		Silicon	Tek Spec
Q2833	151-0190-00	1	2	Silicon	2N3904
Q2833	*151-0190-01	3		Silicon	Tek Spec
Q2837	151-0190-00	1	2	Silicon	2N3904
Q2837	*151-0190-01	3		Silicon	Tek Spec
Q2840	151-0188-00	1	2	Silicon	2N3906
Q2840	151-0220-00	3		Silicon	2N4122
Q2844	151-0188-00	1	2	Silicon	2N3906
Q2844	151-0220-00	3		Silicon	2N4122
Q2851	151-0190-00	1	2	Silicon	2N3904
Q2851	*151-0190-01	3		Silicon	Tek Spec
Q2853	151-0190-00	1	2	Silicon	2N3904
Q2853	*151-0190-01	3		Silicon	Tek Spec
Q2857	151-0190-00	1	2	Silicon	2N3904
Q2857	*151-0190-01	3		Silicon	Tek Spec
Q2860	151-0188-00	1	2	Silicon	2N3906
Q2860	151-0220-00	3		Silicon	2N4122
Q2864	151-0188-00	1	2	Silicon	2N3906
Q2864	151-0220-00	3		Silicon	2N4122
Q2871	151-0190-00	1	2	Silicon	2N3904
Q2871	*151-0190-01	3		Silicon	Tek Spec
Q2873	151-0190-00	1	2	Silicon	2N3904
Q2873	*151-0190-01	3		Silicon	Tek Spec
Q2877	151-0190-00	1	2	Silicon	2N3904
Q2877	*151-0190-01	3		Silicon	Tek Spec
Q2880	151-0188-00	1	2	Silicon	2N3906
Q2880	151-0220-00	3		Silicon	2N4122
Q2884	151-0188-00	1	2	Silicon	2N3906
Q2884	151-0220-00	3		Silicon	2N4122
Q2891	151-0190-00	1	2	Silicon	2N3904
Q2891	*151-0190-01	3		Silicon	Tek Spec
Q2893	151-0190-00	1	2	Silicon	2N3904
Q2893	*151-0190-01	3		Silicon	Tek Spec
Q2897	151-0190-00	1	2	Silicon	2N3904
Q2897	*151-0190-01	3		Silicon	Tek Spec
Q2900	151-0188-00	1	2	Silicon	2N3906
Q2900	151-0220-00	3		Silicon	2N4122
Q2904	151-0188-00	1	2	Silicon	2N3906
Q2904	151-0220-00	3		Silicon	2N4122
Q2911	151-0190-00	1	2	Silicon	2N3904
Q2911	*151-0190-01	3		Silicon	Tek Spec
Q2913	151-0190-00	1	2	Silicon	2N3904
Q2913	*151-0190-01	3		Silicon	Tek Spec
Q2917	151-0190-00	1	2	Silicon	2N3904

LIMIT CARD Series H (cont)

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
Q2917	*151-0190-01	3		Silicon Tek Spec
Q2920	151-0188-00	1	2	Silicon 2N3906
Q2920	151-0220-00	3		Silicon 2N4122
Q2924	151-0188-00	1	2	Silicon 2N3906
Q2924	151-0220-00	3		Silicon 2N4122
Q2931	151-0190-00	1	2	Silicon 2N3904
Q2931	*151-0190-01	3		Silicon Tek Spec
Q2933	151-0190-00	1	2	Silicon 2N3904
Q2933	*151-0190-01	3		Silicon Tek Spec
Q2937	151-0190-00	1	2	Silicon 2N3904
Q2937	*151-0190-01	3		Silicon Tek Spec
Q2940	151-0188-00	1	2	Silicon 2N3906
Q2940	151-0220-00	3		Silicon 2N4122
Q2944	151-0188-00	1	2	Silicon 2N3906
Q2944	151-0220-00	3		Silicon 2N4122
Q2951	151-0190-00	1	2	Silicon 2N3904
Q2951	*151-0190-01	3		Silicon Tek Spec
Q2960	151-0188-00	1	2	Silicon 2N3906
Q2960	151-0220-00	3		Silicon 2N4122
Q2971	151-0190-00	1	2	Silicon 2N3904
Q2971	*151-0190-01	3		Silicon Tek Spec
Q2974	151-0188-00	1	2	Silicon 2N3906
Q2974	151-0220-00	3		Silicon 2N4122
Q2977	151-0190-00	1	2	Silicon 2N3904
Q2977	*151-0190-01	3		Silicon Tek Spec

Resistors

Resistors are fixed, composition, ±10% unless otherwise indicated.

R2611	315-0182-00		1.8 kΩ	1/4 W	5%
R2612	315-0563-00		56 kΩ	1/4 W	5%
R2616	315-0753-00	1	75 kΩ	1/4 W	5%
R2616	315-0513-00	2	51 kΩ	1/4 W	5%
R2618	315-0823-00		82 kΩ	1/4 W	5%
R2619	315-0184-00	1	180 kΩ	1/4 W	5%
R2619	315-0273-00	2	27 kΩ	1/4 W	5%
R2620	315-0823-00		82 kΩ	1/4 W	5%
R2622	315-0103-00		10 kΩ	1/4 W	5%
R2624	315-0102-00		1 kΩ	1/4 W	5%
R2626	315-0823-00		82 kΩ	1/4 W	5%
R2628	315-0823-00		82 kΩ	1/4 W	5%
R2629	315-0244-00	1	240 kΩ	1/4 W	5%
R2629	315-0273-00	2	27 kΩ	1/4 W	5%
R2631	315-0823-00		82 kΩ	1/4 W	5%
R2633	315-0182-00		1.8 kΩ	1/4 W	5%
R2634	315-0563-00		56 kΩ	1/4 W	5%
R2638	315-0753-00	1	75 kΩ	1/4 W	5%
R2638	315-0513-00	2	51 kΩ	1/4 W	5%
R2639	315-0224-00	1	220 kΩ	1/4 W	5%

LIMIT CARD Series H (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description	
R2639	315-0273-00	2		27 kΩ	1/4 W 5%
R2640	315-0823-00			82 kΩ	1/4 W 5%
R2642	315-0103-00			10 kΩ	1/4 W 5%
R2644	315-0102-00			1 kΩ	1/4 W 5%
R2646	315-0823-00			82 kΩ	1/4 W 5%
R2648	315-0823-00			82 kΩ	1/4 W 5%
R2649	315-0244-00	1		240 kΩ	1/4 W 5%
R2649	315-0273-00	2		27 kΩ	1/4 W 5%
R2651	315-0823-00			82 kΩ	1/4 W 5%
R2653	315-0182-00			1.8 kΩ	1/4 W 5%
R2654	315-0563-00			56 kΩ	1/4 W 5%
R2658	315-0753-00	1		75 kΩ	1/4 W 5%
R2658	315-0513-00	2		51 kΩ	1/4 W 5%
R2659	315-0224-00	1		220 kΩ	1/4 W 5%
R2659	315-0273-00	2		27 kΩ	1/4 W 5%
R2660	315-0823-00			82 kΩ	1/4 W 5%
R2662	315-0103-00			10 kΩ	1/4 W 5%
R2664	315-0102-00			1 kΩ	1/4 W 5%
R2666	315-0823-00			82 kΩ	1/4 W 5%
R2668	315-0823-00			82 kΩ	1/4 W 5%
R2669	315-0244-00	1		240 kΩ	1/4 W 5%
R2669	315-0273-00	2		27 kΩ	1/4 W 5%
R2671	315-0823-00			82 kΩ	1/4 W 5%
R2673	315-0182-00			1.8 kΩ	1/4 W 5%
R2674	315-0563-00			56 kΩ	1/4 W 5%
R2678	315-0753-00	1		75 kΩ	1/4 W 5%
R2678	315-0513-00	2		51 kΩ	1/4 W 5%
R2679	315-0224-00	1		220 kΩ	1/4 W 5%
R2679	315-0273-00	2		27 kΩ	1/4 W 5%
R2680	315-0823-00			82 kΩ	1/4 W 5%
R2682	315-0103-00			10 kΩ	1/4 W 5%
R2684	315-0102-00			1 kΩ	1/4 W 5%
R2686	315-0823-00			82 kΩ	1/4 W 5%
R2688	315-0823-00			82 kΩ	1/4 W 5%
R2689	315-0244-00	1		240 kΩ	1/4 W 5%
R2689	315-0273-00	2		27 kΩ	1/4 W 5%
R2691	315-0823-00			82 kΩ	1/4 W 5%
R2693	315-0182-00			1.8 kΩ	1/4 W 5%
R2694	315-0563-00			56 kΩ	1/4 W 5%
R2698	315-0753-00	1		75 kΩ	1/4 W 5%
R2698	315-0513-00	2		51 kΩ	1/4 W 5%
R2699	315-0224-00	1		220 kΩ	1/4 W 5%
R2699	315-0273-00	2		27 kΩ	1/4 W 5%
R2700	315-0823-00			82 kΩ	1/4 W 5%
R2702	315-0103-00			10 kΩ	1/4 W 5%

LIMIT CARD Series H (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R2704	315-0102-00			1 kΩ	¼ W	5%
R2706	315-0823-00			82 kΩ	¼ W	5%
R2708	315-0823-00			82 kΩ	¼ W	5%
R2709	315-0244-00	1		240 kΩ	¼ W	5%
R2709	315-0273-00	2		27 kΩ	¼ W	5%
R2711	315-0823-00			82 kΩ	¼ W	5%
R2713	315-0182-00			1.8 kΩ	¼ W	5%
R2714	315-0563-00			56 kΩ	¼ W	5%
R2718	315-0753-00	1		75 kΩ	¼ W	5%
R2718	315-0513-00	2		51 kΩ	¼ W	5%
R2719	315-0224-00	1		220 kΩ	¼ W	5%
R2719	315-0273-00	2		27 kΩ	¼ W	5%
R2720	315-0823-00			82 kΩ	¼ W	5%
R2722	315-0103-00			10 kΩ	¼ W	5%
R2724	315-0102-00			1 kΩ	¼ W	5%
R2726	315-0823-00			82 kΩ	¼ W	5%
R2728	315-0823-00			82 kΩ	¼ W	5%
R2729	315-0244-00	1		240 kΩ	¼ W	5%
R2729	315-0273-00	2		27 kΩ	¼ W	5%
R2731	315-0823-00			82 kΩ	¼ W	5%
R2733	315-0182-00			1.8 kΩ	¼ W	5%
R2734	315-0563-00			56 kΩ	¼ W	5%
R2738	315-0753-00	1		75 kΩ	¼ W	5%
R2738	315-0513-00	2		51 k	¼ W	5%
R2739	315-0224-00	1		220 kΩ	¼ W	5%
R2739	315-0273-00	2		27 kΩ	¼ W	5%
R2740	315-0823-00			82 kΩ	¼ W	5%
R2742	315-0103-00			10 kΩ	¼ W	5%
R2744	315-0102-00			1 kΩ	¼ W	5%
R2746	315-0823-00			82 kΩ	¼ W	5%
R2748	315-0823-00			82 kΩ	¼ W	5%
R2749	315-0244-00	1		240 kΩ	¼ W	5%
R2749	315-0273-00	2		27 kΩ	¼ W	5%
R2751	315-0823-00			82 kΩ	¼ W	5%
R2753	315-0182-00			1.8 kΩ	¼ W	5%
R2754	315-0563-00			56 kΩ	¼ W	5%
R2755	321-0326-00	X2		24.3 kΩ	⅛ W	Prec 1%
R2757	321-0252-00	X2		4.12 kΩ	⅛ W	Prec 1%
R2759	315-0224-00	1		220 kΩ	¼ W	5%
R2759	315-0273-00	2		27 kΩ	¼ W	5%
R2760	315-0823-00			82 kΩ	¼ W	5%
R2761	315-0754-00	1		750 kΩ	¼ W	5%
R2761	315-0823-00	2		82 kΩ	¼ W	5%
R2771	315-0433-00			43 kΩ	¼ W	5%
R2772	315-0274-00	1		270 kΩ	¼ W	5%

LIMIT CARD Series H (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R2772	315-0753-00	2		75 kΩ	1/4 W	5%
R2773	321-0252-00	X2		4.12 kΩ	1/8 W	Prec 1%
R2775	321-0339-00	X2		33.2 kΩ	1/8 W	Prec 1%
R2779	315-0103-00	X2		10 kΩ	1/4 W	5%
R2811	315-0182-00			1.8 kΩ	1/4 W	5%
R2812	315-0563-00			56 kΩ	1/4 W	5%
R2814	315-0243-00			24 kΩ	1/4 W	5%
R2815	315-0273-00			27 kΩ	1/4 W	5%
R2816	315-0753-00	1		75 kΩ	1/4 W	5%
R2816	315-0513-00	2		51 kΩ	1/4 W	5%
R2818	315-0823-00			82 kΩ	1/4 W	5%
R2819	315-0224-00	1		220 kΩ	1/4 W	5%
R2819	315-0273-00	2		27 kΩ	1/4 W	5%
R2820	315-0823-00			82 kΩ	1/4 W	5%
R2822	315-0103-00			10 kΩ	1/4 W	5%
R2824	315-0102-00			1 kΩ	1/4 W	5%
R2825	315-0393-00			39 kΩ	1/4 W	5%
R2826	315-0823-00			82 kΩ	1/4 W	5%
R2828	315-0823-00			82 kΩ	1/4 W	5%
R2829	315-0244-00	1		240 kΩ	1/4 W	5%
R2829	315-0273-00	2		27 kΩ	1/4 W	5%
R2831	315-0823-00			82 kΩ	1/4 W	5%
R2833	315-0182-00			1.8 kΩ	1/4 W	5%
R2834	315-0563-00			56 kΩ	1/4 W	5%
R2836	315-0243-00			24 kΩ	1/4 W	5%
R2837	315-0273-00			27 kΩ	1/4 W	5%
R2838	315-0753-00	1		75 kΩ	1/4 W	5%
R2838	315-0513-00	2		51 kΩ	1/4 W	5%
R2839	315-0224-00	1		220 kΩ	1/4 W	5%
R2839	315-0273-00	2		27 kΩ	1/4 W	5%
R2840	315-0823-00			82 kΩ	1/4 W	5%
R2842	315-0103-00			10 kΩ	1/4 W	5%
R2844	315-0102-00			1 kΩ	1/4 W	5%
R2845	315-0393-00			39 kΩ	1/4 W	5%
R2846	315-0823-00			82 kΩ	1/4 W	5%
R2848	315-0823-00			82 kΩ	1/4 W	5%
R2849	315-0244-00	1		240 kΩ	1/4 W	5%
R2849	315-0273-00	2		27 kΩ	1/4 W	5%
R2851	315-0823-00			82 kΩ	1/4 W	5%
R2853	315-0182-00			1.8 kΩ	1/4 W	5%
R2854	315-0563-00			56 kΩ	1/4 W	5%
R2856	315-0243-00			24 kΩ	1/4 W	5%
R2857	315-0273-00			27 kΩ	1/4 W	5%
R2858	315-0753-00	1		75 kΩ	1/4 W	5%
R2858	315-0513-00	2		51 k	1/4 W	5%

LIMIT CARD Series H (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R2859	315-0513-00	1		220 kΩ	1/4 W	5%
R2859	315-0273-00	2		27 kΩ	1/4 W	5%
R2860	315-0823-00			82 kΩ	1/4 W	5%
R2862	315-0103-00			10 kΩ	1/4 W	5%
R2864	315-0102-00			1 kΩ	1/4 W	5%
R2865	315-0393-00			39 kΩ	1/4 W	5%
R2866	315-0823-00			82 kΩ	1/4 W	5%
R2868	315-0823-00			82 kΩ	1/4 W	5%
R2869	315-0244-00	1		240 kΩ	1/4 W	5%
R2869	315-0273-00	2		27 kΩ	1/4 W	5%
R2871	315-0823-00			82 kΩ	1/4 W	5%
R2873	315-0182-00			1.8 kΩ	1/4 W	5%
R2874	315-0563-00			56 kΩ	1/4 W	5%
R2876	315-0243-00			24 kΩ	1/4 W	5%
R2877	315-0273-00			27 kΩ	1/4 W	5%
R2878	315-0753-00	1		75 kΩ	1/4 W	5%
R2878	315-0513-00	2		51 kΩ	1/4 W	5%
R2879	315-0224-00	1		220 kΩ	1/4 W	5%
R2879	315-0273-00	2		27 kΩ	1/4 W	5%
R2880	315-0823-00			82 kΩ	1/4 W	5%
R2882	315-0103-00			10 kΩ	1/4 W	5%
R2884	315-0102-00			1 kΩ	1/4 W	5%
R2885	315-0393-00			39 kΩ	1/4 W	5%
R2886	315-0823-00			82 kΩ	1/4 W	5%
R2888	315-0823-00			82 kΩ	1/4 W	5%
R2889	315-0224-00	1		240 kΩ	1/4 W	5%
R2889	315-0273-00	2		27 kΩ	1/4 W	5%
R2891	315-0823-00			82 kΩ	1/4 W	5%
R2893	315-0182-00			1.8 kΩ	1/4 W	5%
R2894	315-0563-00			56 kΩ	1/4 W	5%
R2896	315-0243-00			24 kΩ	1/4 W	5%
R2897	315-0273-00			27 kΩ	1/4 W	5%
R2898	315-0753-00	1		75 kΩ	1/4 W	5%
R2898	315-0513-00	2		51 kΩ	1/4 W	5%
R2899	315-0224-00	1		220 kΩ	1/4 W	5%
R2899	315-0273-00	2		27 kΩ	1/4 W	5%
R2900	315-0823-00			82 kΩ	1/4 W	5%
R2902	315-0103-00			10 kΩ	1/4 W	5%
R2904	315-0102-00			1 kΩ	1/4 W	5%
R2905	315-0393-00			39 kΩ	1/4 W	5%
R2906	315-0823-00			82 kΩ	1/4 W	5%
R2908	315-0823-00			82 kΩ	1/4 W	5%
R2909	315-0244-00	1		240 kΩ	1/4 W	5%
R2909	315-0273-00	2		27 kΩ	1/4 W	5%
R2911	315-0823-00			82 kΩ	1/4 W	5%

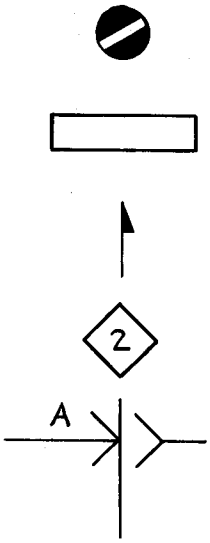
LIMIT CARD Series H (cont)

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R2913	315-0182-00			1.8 kΩ	1/4 W	5%
R2914	315-0563-00			56 kΩ	1/4 W	5%
R2916	315-0243-00			24 kΩ	1/4 W	5%
R2917	315-0273-00			27 kΩ	1/4 W	5%
R2918	315-0753-00	1		75 kΩ	1/4 W	5%
R2918	315-0513-00	2		51 kΩ	1/4 W	5%
R2919	315-0224-00	1		220 kΩ	1/4 W	5%
R2919	315-0273-00	2		27 kΩ	1/4 W	5%
R2920	315-0823-00			82 kΩ	1/4 W	5%
R2922	315-0103-00			10 kΩ	1/4 W	5%
R2924	315-0102-00			1 kΩ	1/4 W	5%
R2925	315-0393-00			39 kΩ	1/4 W	5%
R2926	315-0823-00			82 kΩ	1/4 W	5%
R2928	315-0823-00			82 kΩ	1/4 W	5%
R2929	315-0244-00	1		240 kΩ	1/4 W	5%
R2929	315-0273-00	2		27 kΩ	1/4 W	5%
R2931	315-0823-00			82 kΩ	1/4 W	5%
R2933	315-0182-00			1.8 kΩ	1/4 W	5%
R2934	315-0563-00			56 kΩ	1/4 W	5%
R2936	315-0243-00			24 kΩ	1/4 W	5%
R2937	315-0273-00			27 kΩ	1/4 W	5%
R2938	315-0753-00	1		75 kΩ	1/4 W	5%
R2938	315-0513-00	2		51 kΩ	1/4 W	5%
R2939	315-0224-00	1		220 kΩ	1/4 W	5%
R2939	315-0273-00	2		27 kΩ	1/4 W	5%
R2940	315-0823-00			82 kΩ	1/4 W	5%
R2942	315-0103-00			10 kΩ	1/4 W	5%
R2944	315-0102-00			1 kΩ	1/4 W	5%
R2945	315-0393-00			39 kΩ	1/4 W	5%
R2946	315-0823-00			82 kΩ	1/4 W	5%
R2948	315-0823-00			82 kΩ	1/4 W	5%
R2949	315-0244-00	1		240 kΩ	1/4 W	5%
R2949	315-0273-00	2		27 kΩ	1/4 W	5%
R2951	315-0823-00			82 kΩ	1/4 W	5%
R2958	315-0823-00			82 kΩ	1/4 W	5%
R2959	316-0564-00	1		560 kΩ	1/4 W	
R2959	315-0823-00	2		82 kΩ	1/4 W	5%
R2960	315-0823-00			82 kΩ	1/4 W	5%
R2962	315-0244-00	1		240 kΩ	1/4 W	5%
R2962	315-0273-00	2		27 kΩ	1/4 W	5%
R2971	315-0433-00			43 kΩ	1/4 W	5%
R2972	315-0274-00	1		270 kΩ	1/4 W	5%
R2972	315-0753-00	2		75 kΩ	1/4 W	5%
R2973	315-0563-00			56 kΩ	1/4 W	5%
R2974	315-0273-00			27 kΩ	1/4 W	5%
R2976	315-0243-00			24 kΩ	1/4 W	5%
R2977	315-0273-00			27 kΩ	1/4 W	5%
R2978	315-0474-00	1		470 kΩ	1/4 W	5%
R2978	315-0683-00	2		68 kΩ	1/4 W	5%

SECTION 10
DIAGRAMS
and
MECHANICAL PARTS ILLUSTRATIONS

The following symbols are used on the diagrams:



Screwdriver adjustment

Front-, side- or rear-panel control or connector

Clockwise control rotation in direction of arrow

Refer to indicated diagram

Connection to circuit board made with pin connector at indicated pin

Blue line encloses components located on circuit board

TYPE 230

VOLTAGE AND WAVEFORM CONDITIONS

Circuit voltages were measured with an infinite resistance voltmeter. Voltages were measured with respect to ground with the Type 568 sweep disabled and the Type 230 in TIME MEASUREMENT mode and TRIGGERED MEASUREMENT—OFF. Exceptions to this are given at the end of this note.

The voltages and waveforms shown in blue on the schematic diagrams are not absolute and may vary between instruments. Any apparent differences between the voltage levels measured with the oscilloscope and those shown on the waveforms are due to causes such as different operating conditions, or measurement resolution.

Waveforms shown are actual photographs taken with a Tektronix camera equipped with a projected graticule.

(Cont on next diagram)

VOLTAGE AND WAVEFORM CONDITIONS

(Cont from previous diagram)

To obtain the waveforms, the Type 230 was connected to a Tektronix Type 568 Oscilloscope through an interconnecting cable. The test oscilloscope was a Tektronix Type 547 with Type 1A2 Dual Trace Amplifier.

Waveforms were obtained under the following conditions:

Type 568 Oscilloscope and Plug-in Units

Sweep Mode	Free Running
Sweep Rate	As necessary
Vertical Mode	Dual-Trace or Alternate
Vertical Input Signal	None

Type 230 Digital Unit

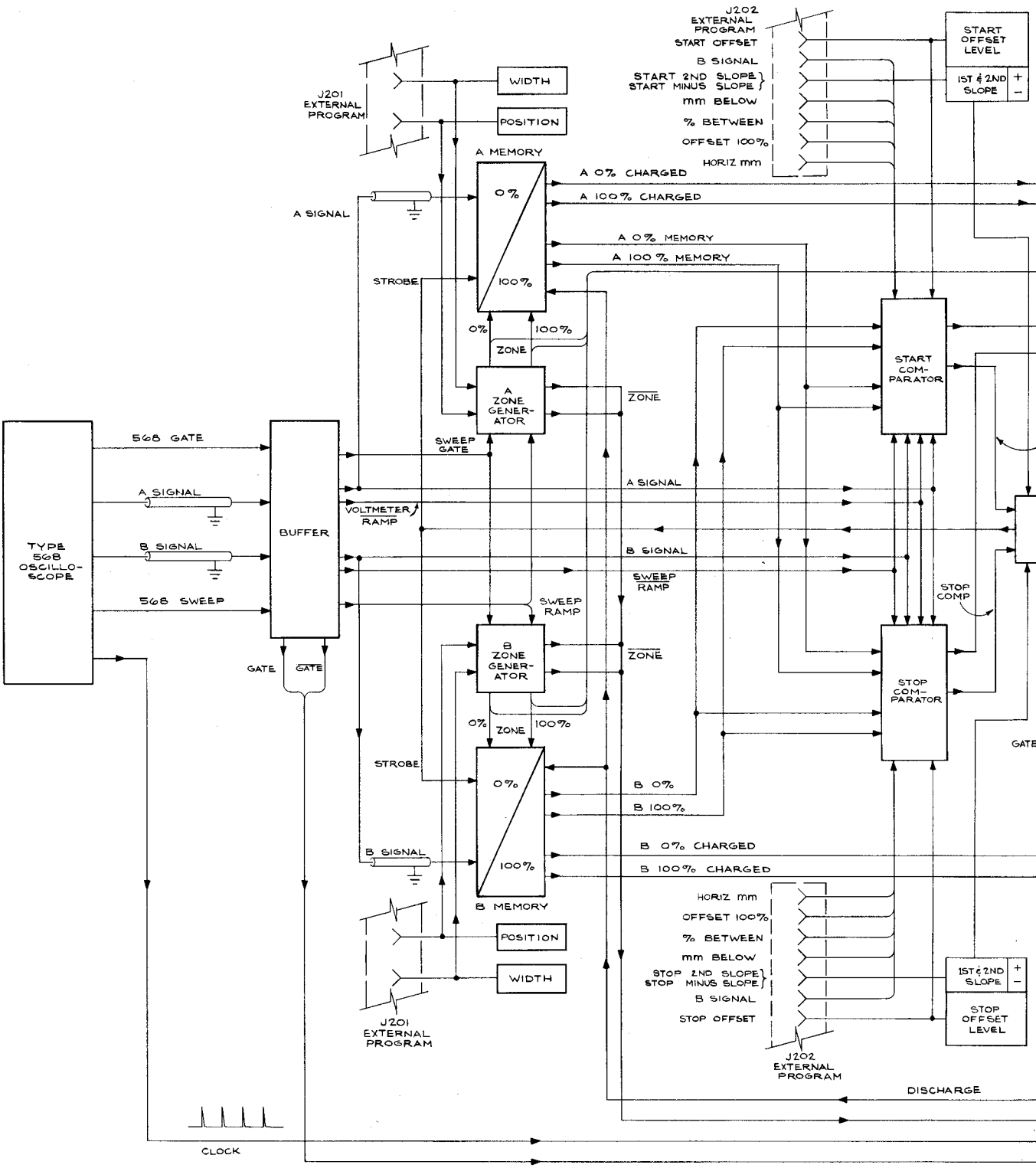
TRIGGERED MEASUREMENT	OFF
DISPLAY TIME	Counterclockwise

Test Oscilloscope

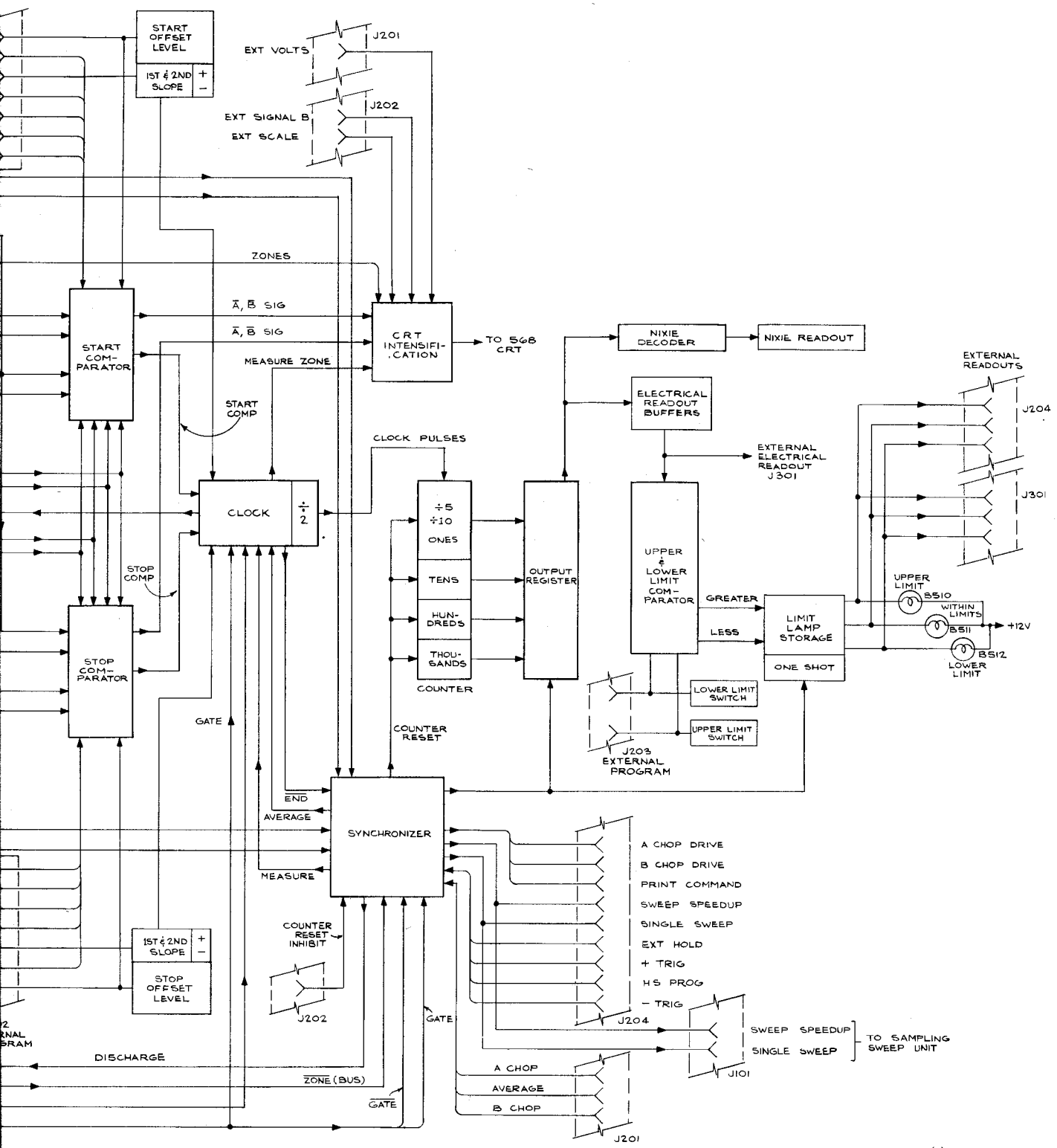
Horizontal Display	A Dly'd
Time-base A	
Time/cm	As noted on waveforms
Triggering	Auto, ±, Int
Plug-In Volts/cm	As noted on waveforms

EXCEPTIONS TO BASIC VOLTAGE READING CONDITIONS:

Voltages shown on the Counter board, the Limit card and the CRT Intensification circuit diagrams were taken with the Type 568 sweep enabled and the Type 230 DISPLAY TIME control set fully counterclockwise.



TYPE 230 DIGITAL UNIT

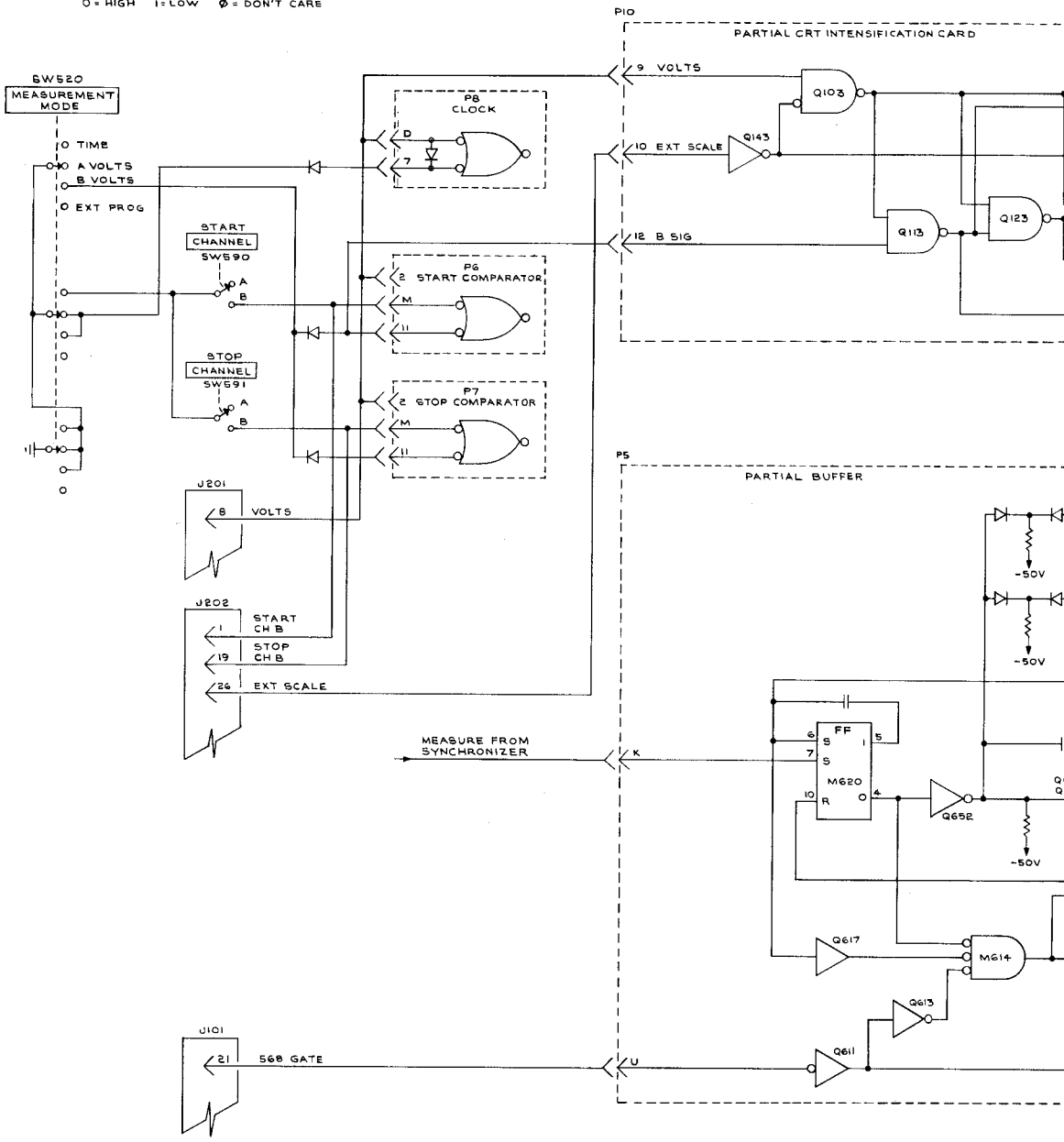


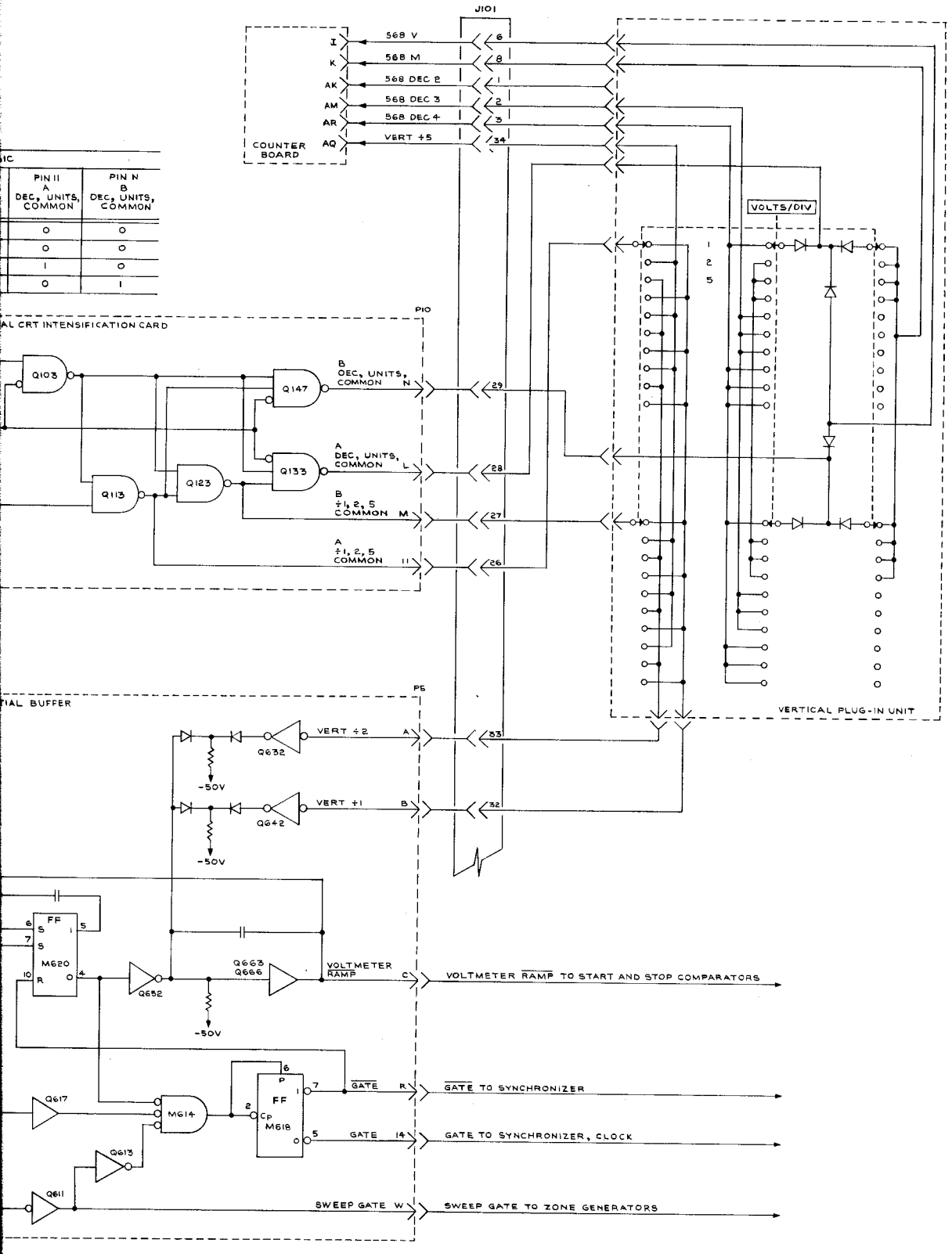
667

BLOCK DIAGRAM

MEASUREMENT MODE	P10 INPUT LOGIC			P10 OUTPUT LOGIC				
	PIN 9 VOLTS	PIN 10 B SIGNAL	PIN 12 EXT SCALE	PIN K HORIZ DEC, UNITS, COMMON	PIN M B ÷1, 2, 5 COMMON	PIN L A ÷1, 2, 5 COMMON	PIN H A DEC, UNITS, COMMON	PIN N B DEC, UNITS, COMMON
TIME -- CHANNEL A	0	0	0	1	0	0	0	0
TIME -- CHANNEL B	0	Ø	0	1	0	0	0	0
A VOLTS	1	0	0	0	0	1	1	0
B VOLTS	1	1	0	0	1	0	0	1

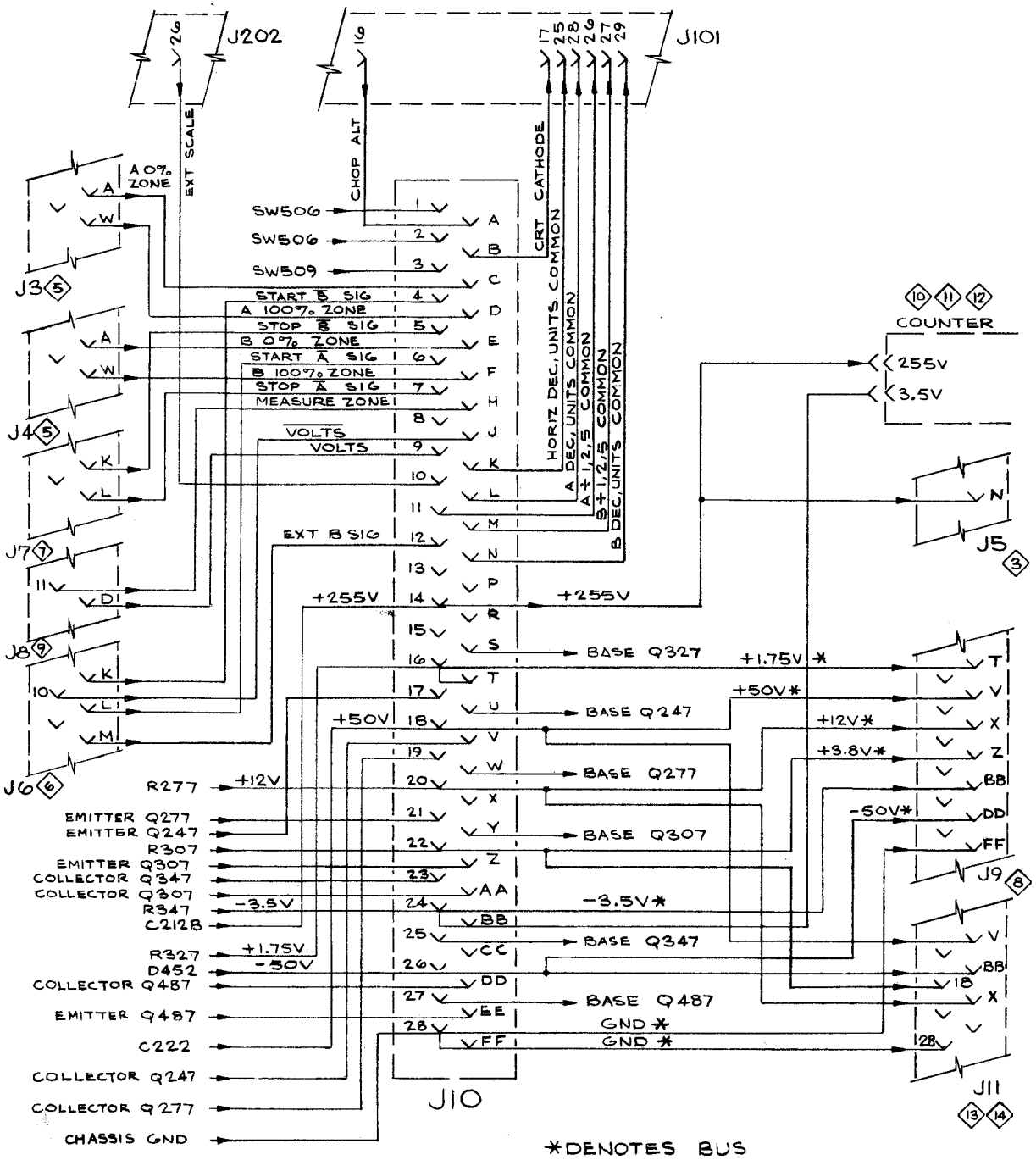
0 = HIGH 1 = LOW Ø = DON'T CARE

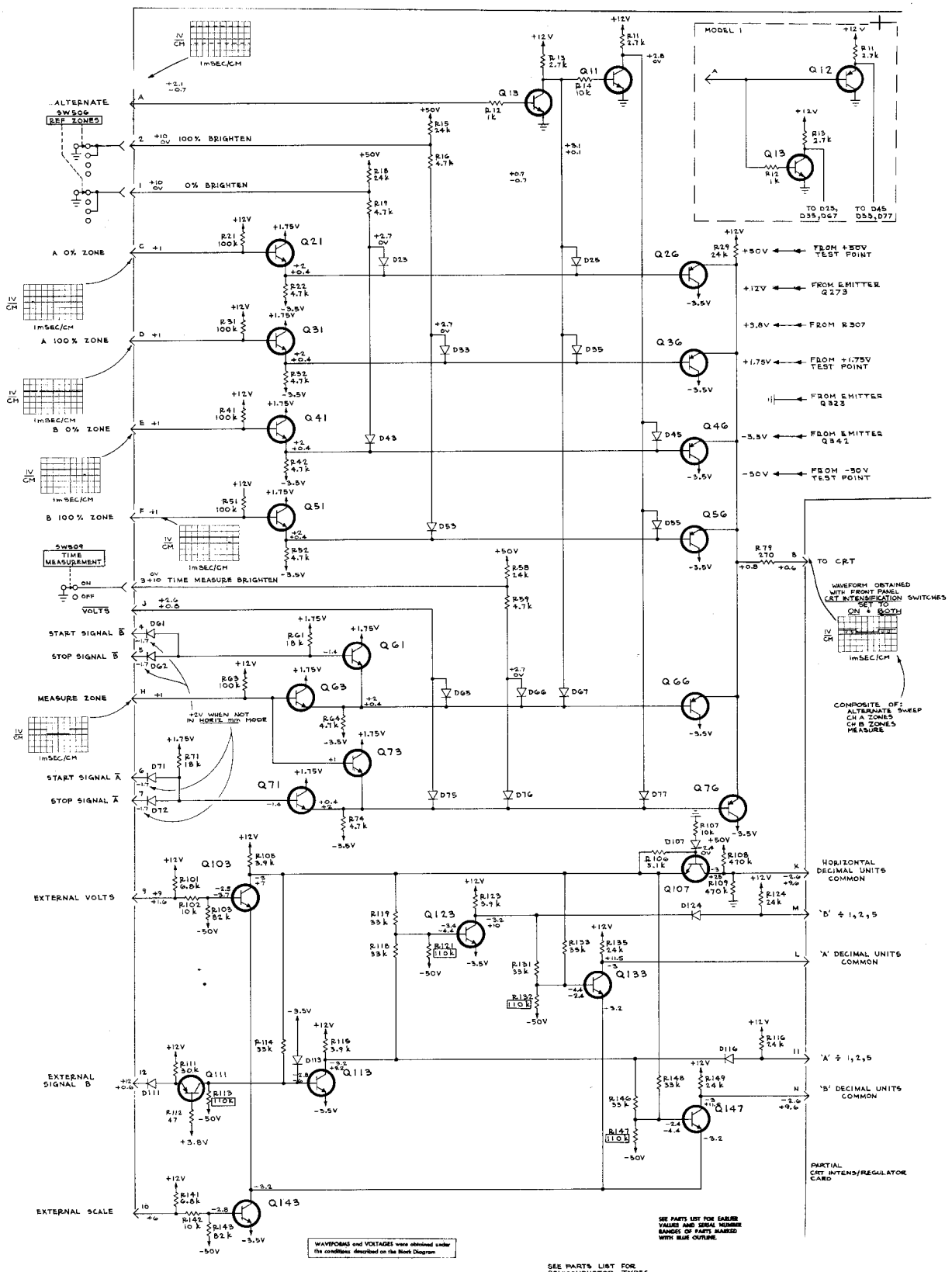




PIN II A DEC, UNITS, COMMON	PIN N B DEC, UNITS, COMMON
0	0
0	0
1	0
0	1

SIMPLIFIED VOLTMETER RAMP FUNCTION 667 EKP


J202
J101
EXT SCALE
CHOP ALT
CRT CATHODE
HORIZ DEC, UNITS COMMON
A DEC, UNITS COMMON
A ÷ 1,2,5 COMMON
B ÷ 1,2,5 COMMON
B DEC, UNITS COMMON
A 0% ZONE
J3
J4
J6
J7
J8
SW506
SW506
SW509
START B SIG
A 100% ZONE
STOP B SIG
B 0% ZONE
START A SIG
B 100% ZONE
STOP A SIG
MEASURE ZONE
VOLTS
VOLTS
EXT B SIG
+255V
+255V
BASE Q327
BASE Q247
BASE Q277
BASE Q307
BASE Q347
BASE Q487
GND *
GND *
COUNTER
255V
3.5V
J5
J9
J11
+1.75V *
+50V*
+12V*
+3.8V*
-50V*
-3.5V*
R277
EMITTER Q277
EMITTER Q247
R307
EMITTER Q307
COLLECTOR Q347
COLLECTOR Q307
R347
C2128
R327
D452
COLLECTOR Q487
EMITTER Q487
C222
COLLECTOR Q247
COLLECTOR Q277
CHASSIS GND
+12V
-3.5V
+1.75V
-50V
+50V
J10
*DENOTES BUS



CRT INTENSIFICATION
PIO (PARTIAL)
SERIES G, MODEL 1-UP

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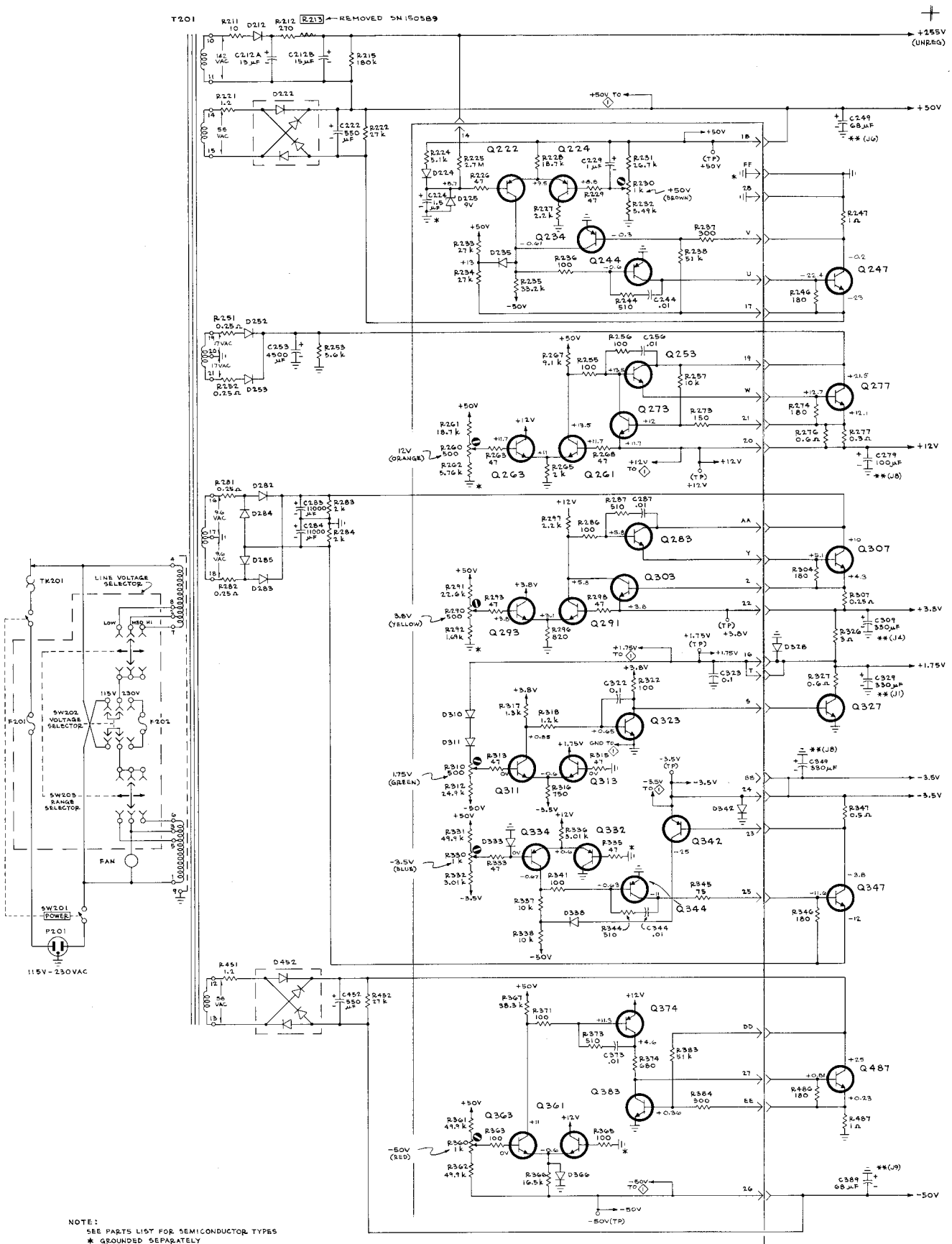
TYPE 230 DIGITAL

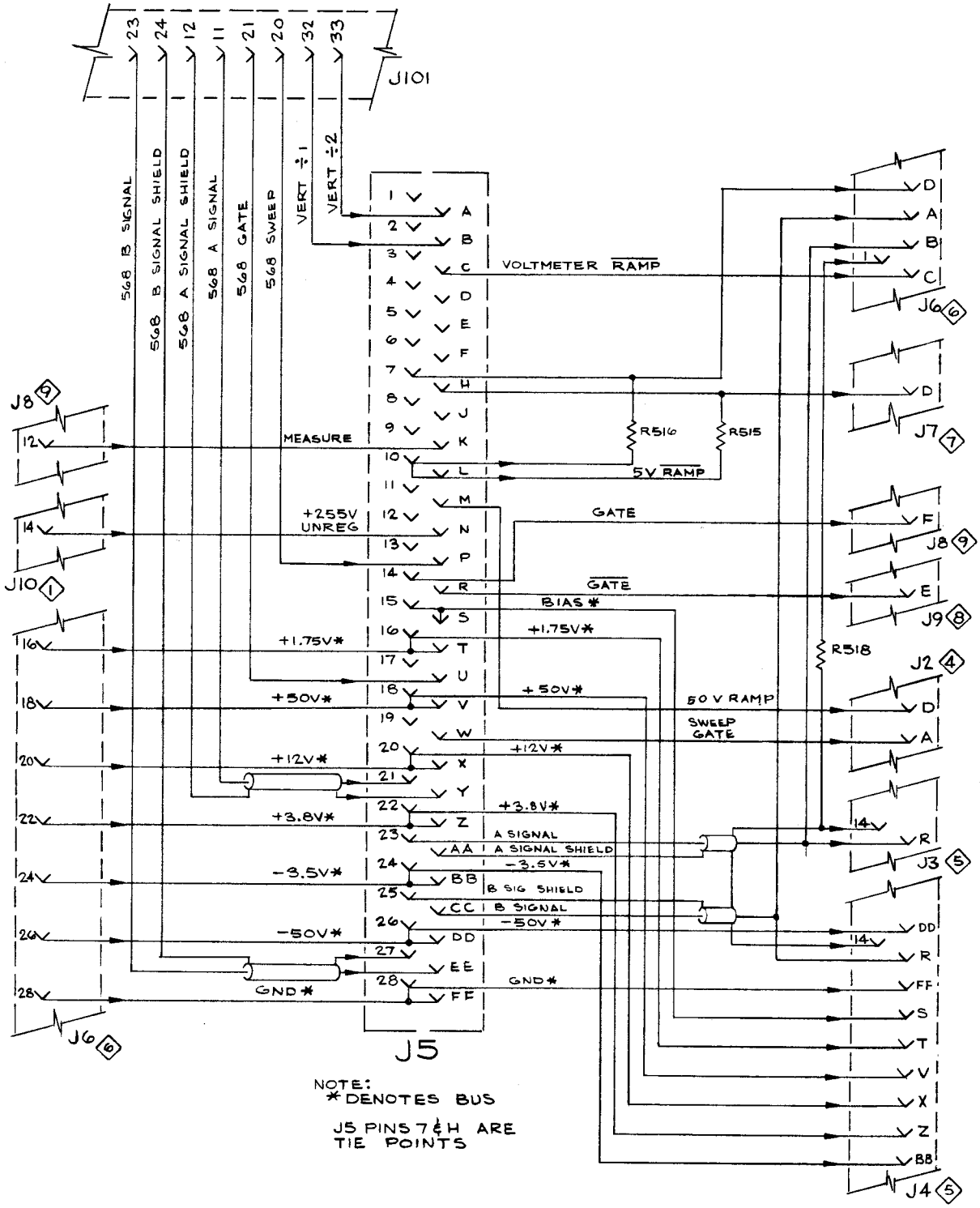


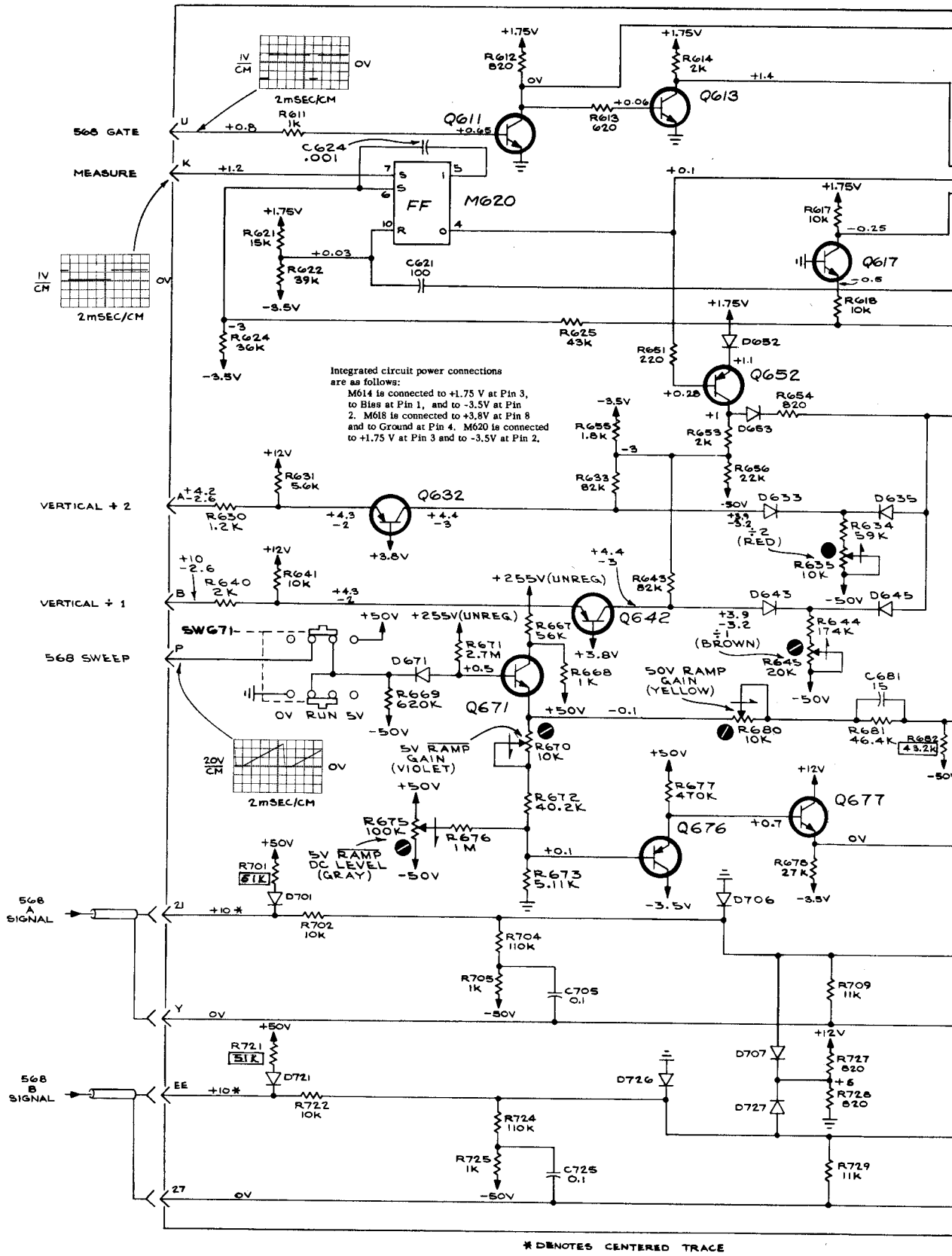
NOTE:
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
* GROUNDED SEPARATELY
**DENOTES ACTUAL CAPACITOR LOCATION

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

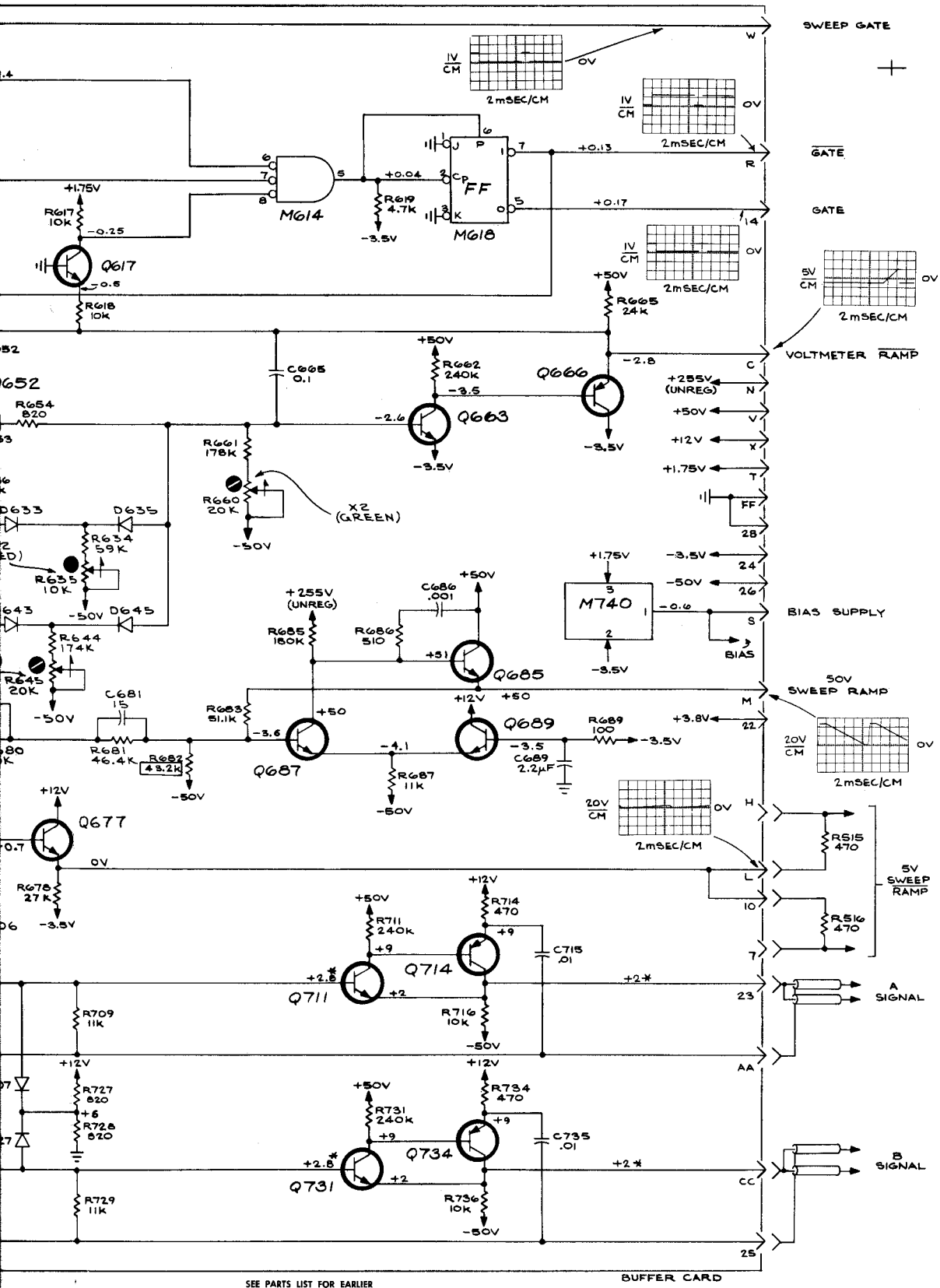
PARTIAL CRT INTENS/REGULATOR CARD

VOLTAGES were taken under conditions given on Block Diagram.


J101
23
24
12
11
21
20
32
33
568 B SIGNAL
568 B SIGNAL SHIELD
568 A SIGNAL SHIELD
568 A SIGNAL
568 GATE
568 SWEEP
VERT ÷1
VERT ÷2
VOLTMETER RAMP
MEASURE
+255V UNREG
+1.75V*
+50V*
+12V*
+3.8V*
-3.5V*
-50V*
GND*
R516
R515
5V RAMP
GATE
BIAS*
50 V RAMP
SWEEP GATE
R518
A SIGNAL
A SIGNAL SHIELD
B SIG SHIELD
B SIGNAL
J8
J10
J6
J5
J7
J9
J2
J3
J4
NOTE:
*DENOTES BUS
J5 PINS 7 & H ARE TIE POINTS



TYPE 230 DIGITAL UNIT



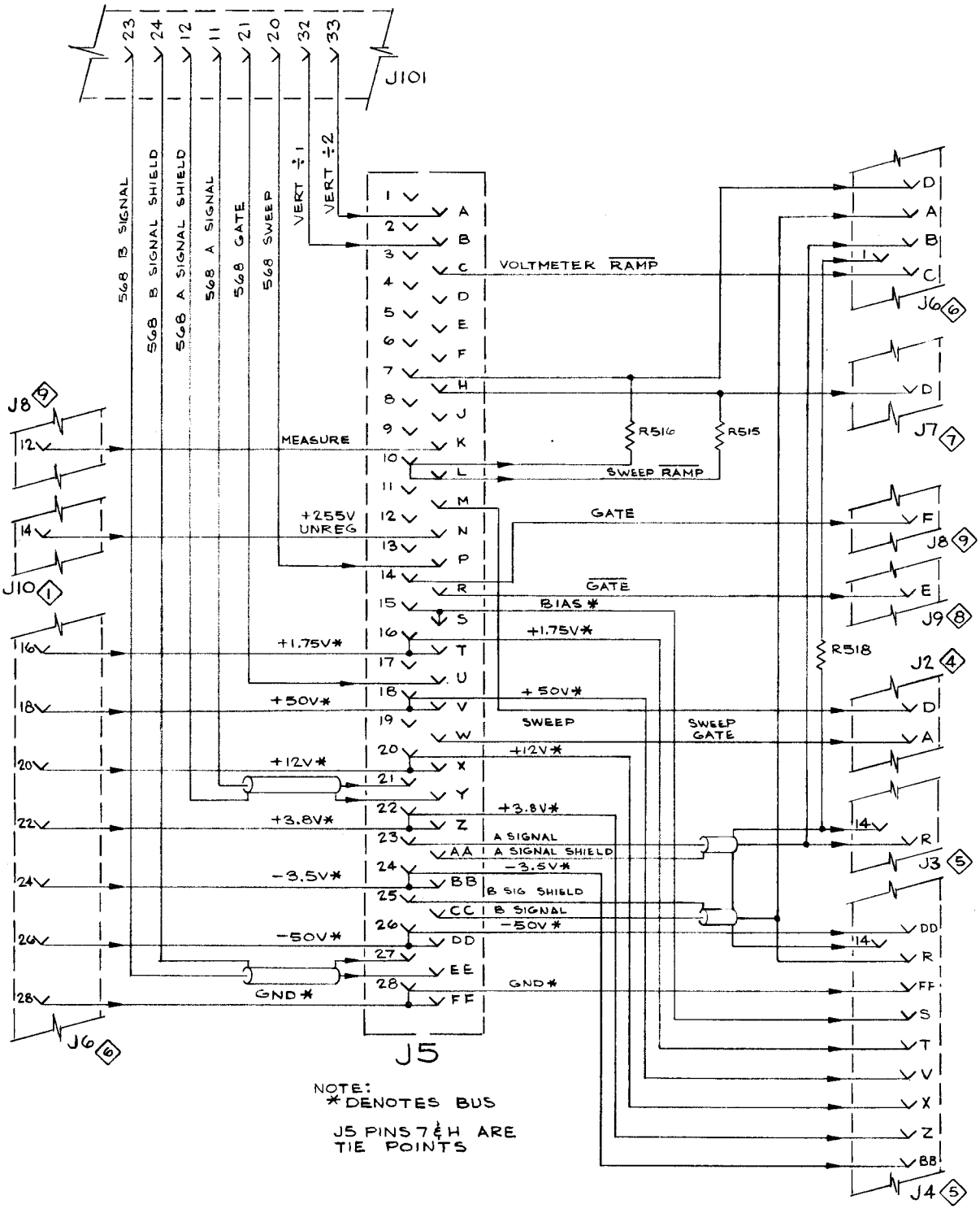
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

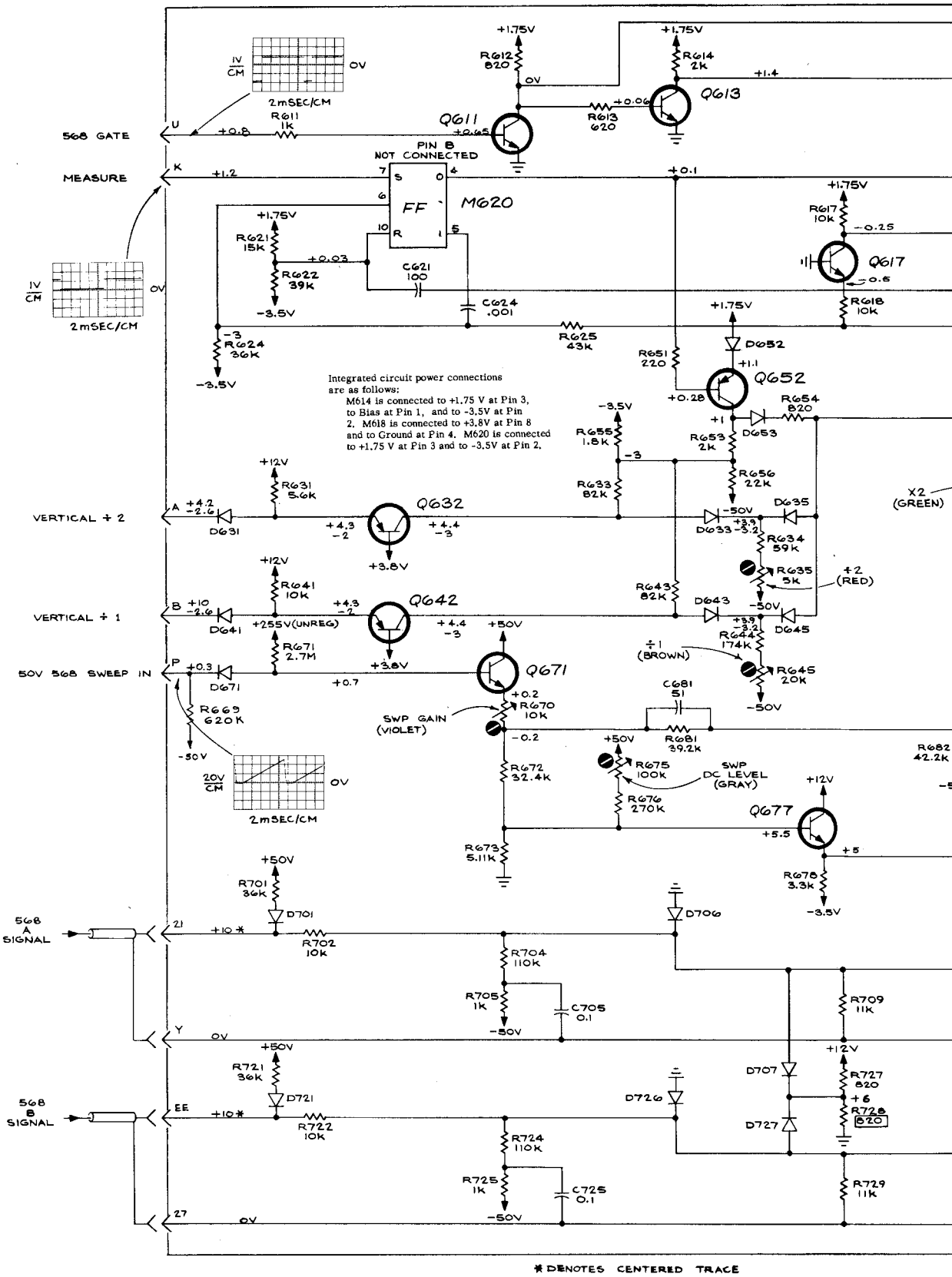
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

369

P5 – BUFFER ③

(SERIES C, MODEL 4-UP)

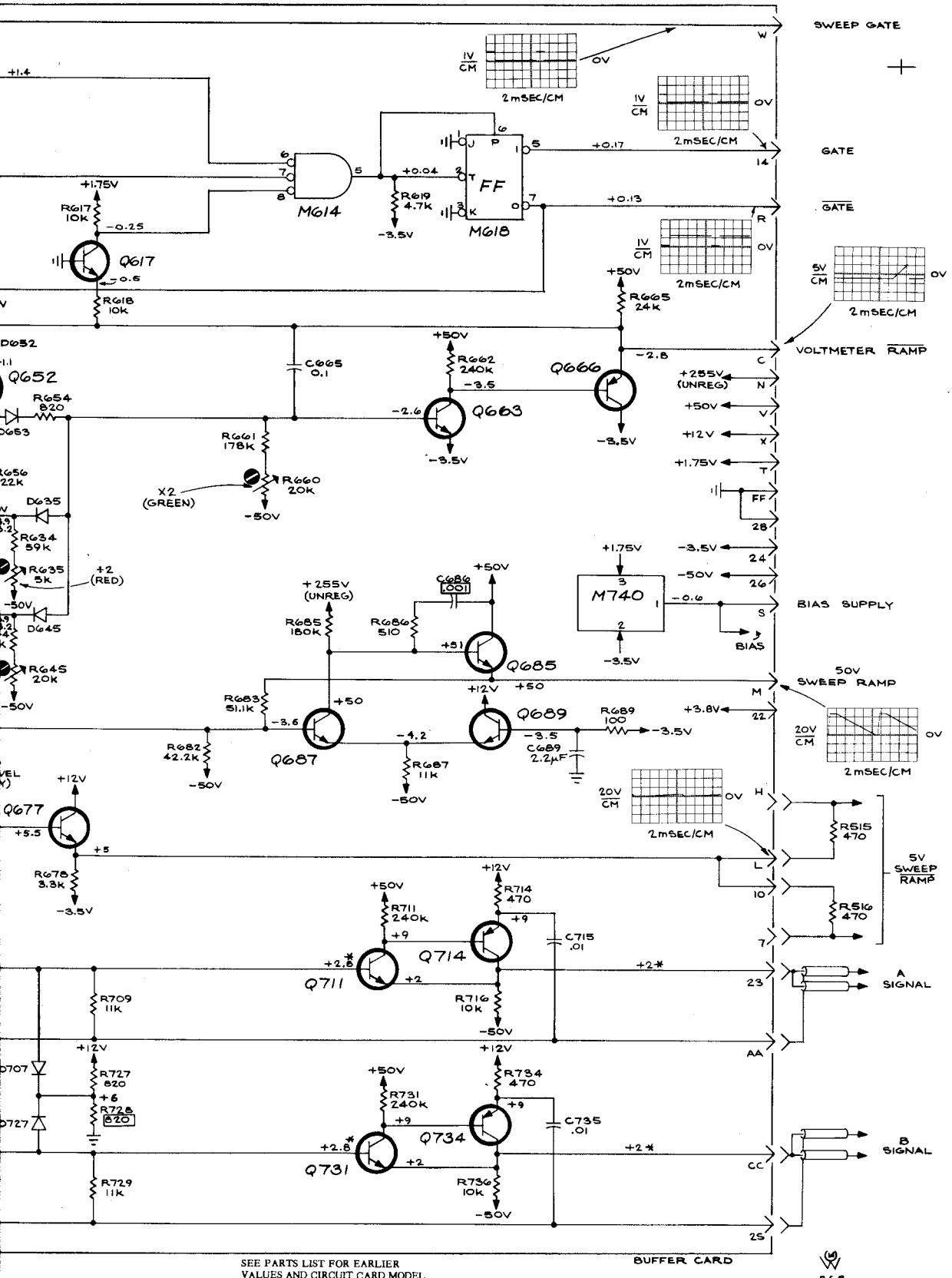

J101
23
24
12
11
21
20
32
33
568 B SIGNAL
568 B SIGNAL SHIELD
568 A SIGNAL SHIELD
568 A SIGNAL
568 GATE
568 SWEEP
VERT ÷1
VERT ÷2
VOLTMETER RAMP
MEASURE
+255V UNREG
+1.75V*
+50V*
+12V*
+3.8V*
-3.5V*
-50V*
GND*
R516
R515
SWEEP RAMP
GATE
BIAS*
SWEEP
SWEEP GATE
A SIGNAL
A SIGNAL SHIELD
B SIG SHIELD
B SIGNAL
R518
J8
J10
J6
J5
J7
J9
J2
J3
J4
NOTE:
*DENOTES BUS
J5 PINS 7 & H ARE TIE POINTS



TYPE 230 DIGITAL UNIT

VOLTAGES and WAVEFORMS were obtained under conditions given on Block Diagram.

D1



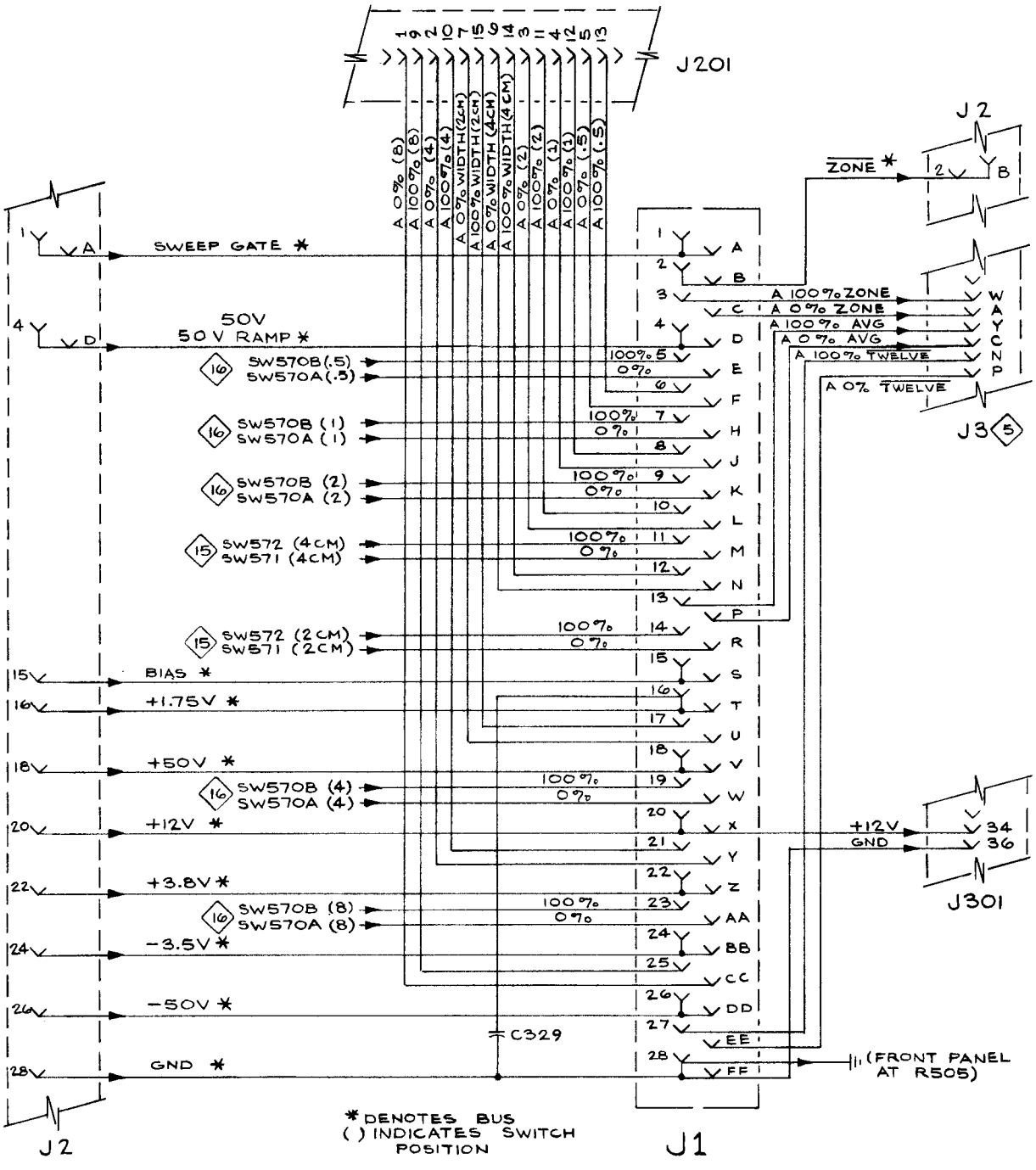
SEE PARTS LIST FOR EARLIER VALUES AND CIRCUIT CARD MODEL NUMBERS OF PARTS MARKED WITH BLUE OUTLINE.

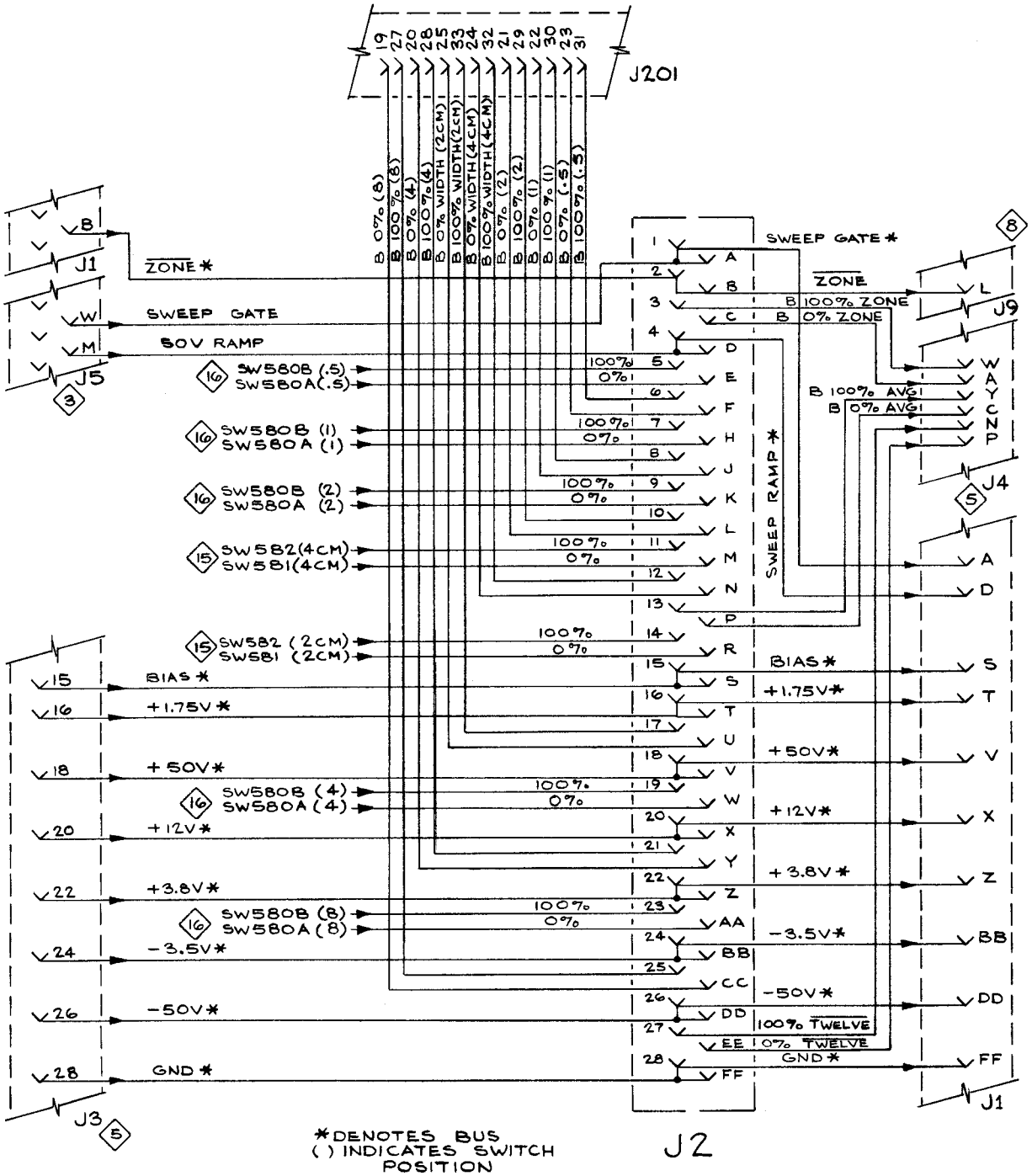
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

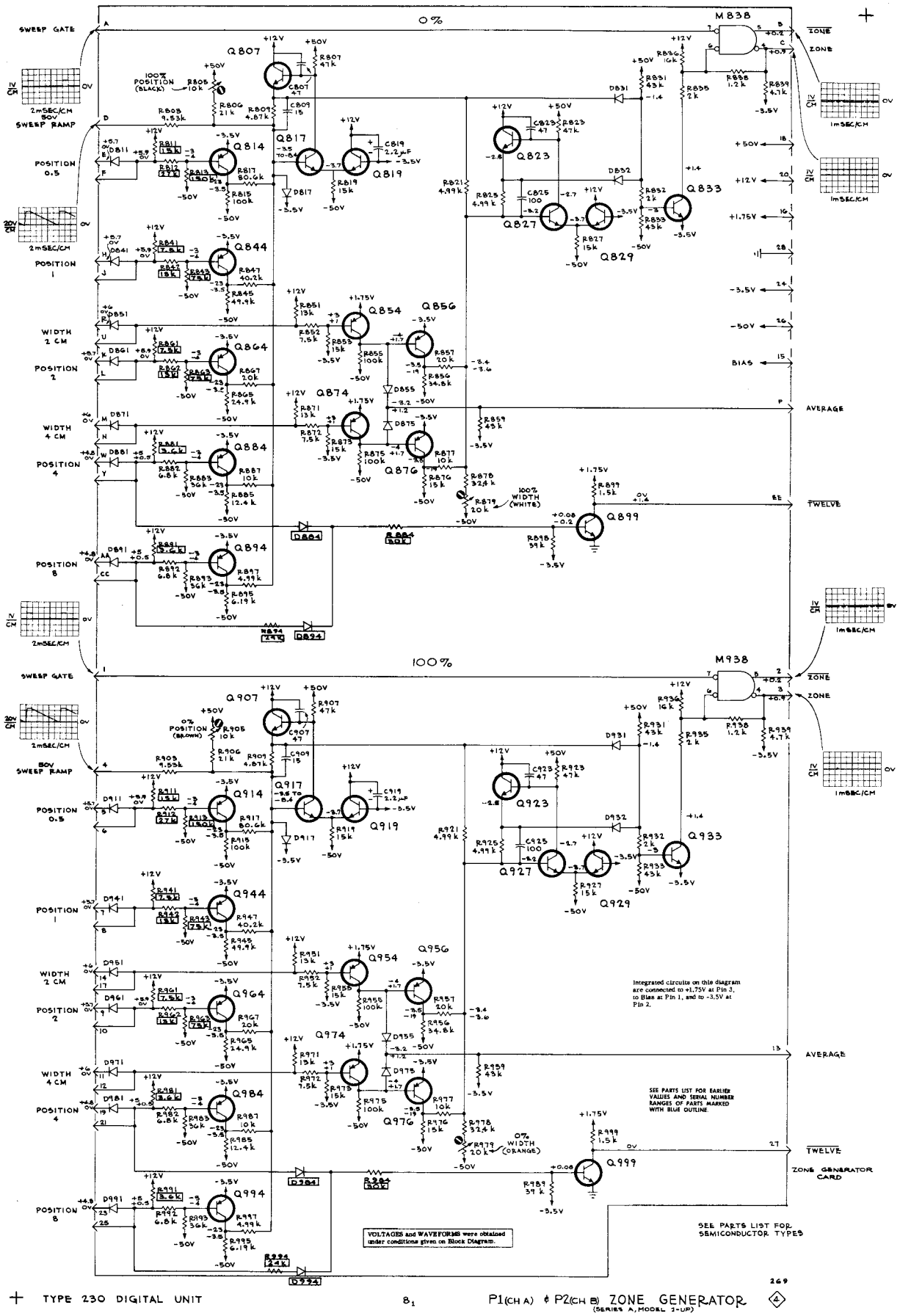
868

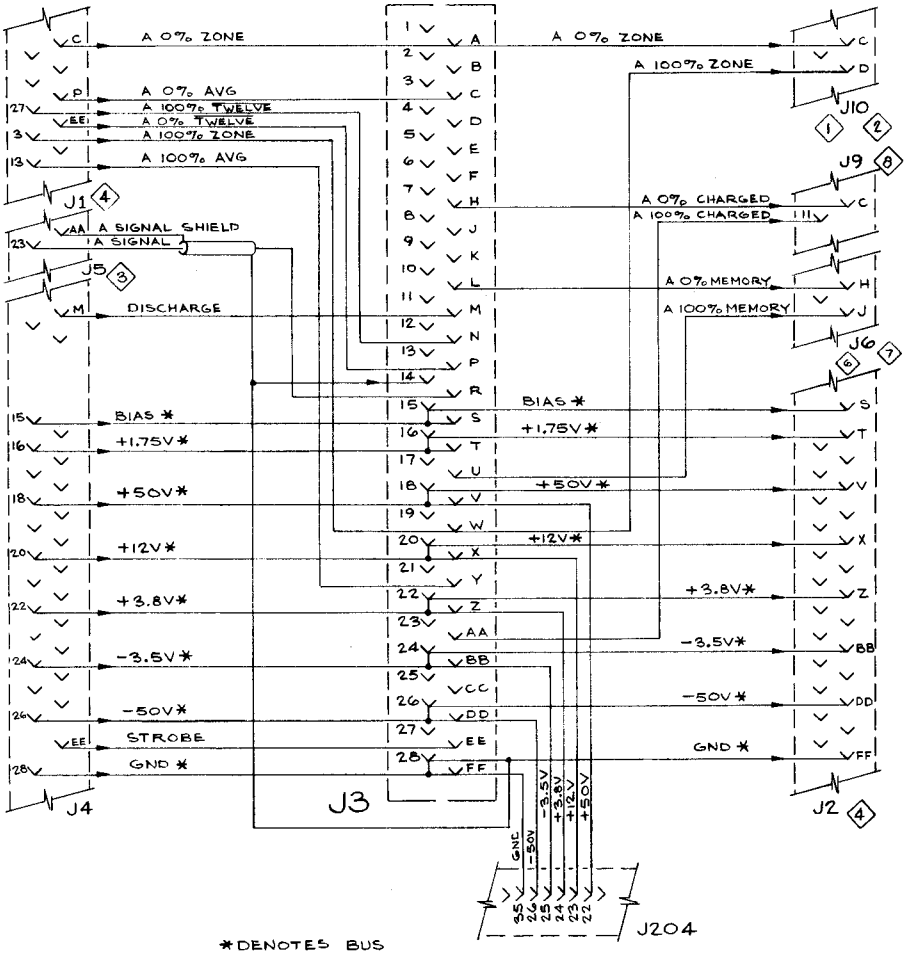
P5 – BUFFER ◇3

(SERIES C, MODELS 1, 2, 3)

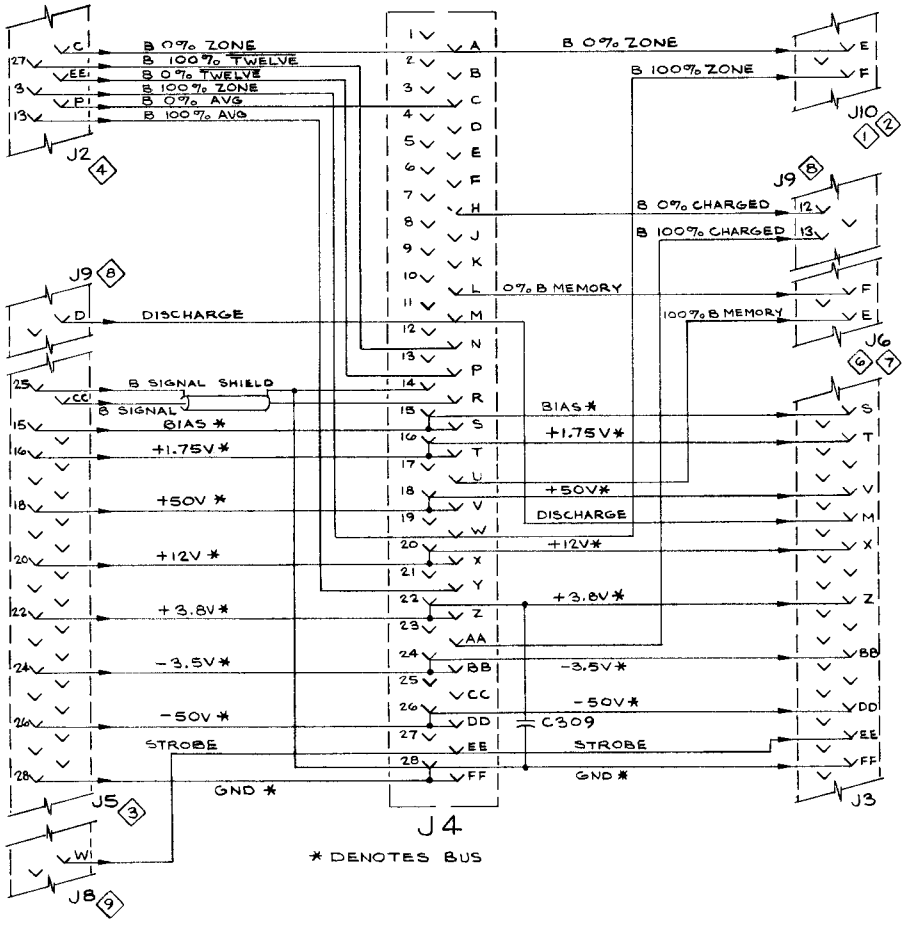

J201
A 0% (8)
A 100% (8)
A 0% (4)
A 100% (4)
A 0% WIDTH (2CM)
A 100% WIDTH (2CM)
A 0% WIDTH (4CM)
A 100% WIDTH (4CM)
A 0% (2)
A 100% (2)
A 0% (1)
A 100% (1)
A 0% (.5)
A 100% (.5)
J2
SWEEP GATE *
50V
50 V RAMP *
SW570B (.5)
SW570A (.5)
SW570B (1)
SW570A (1)
SW570B (2)
SW570A (2)
SW572 (4CM)
SW571 (4CM)
SW572 (2CM)
SW571 (2CM)
BIAS *
+1.75V *
+50V *
SW570B (4)
SW570A (4)
+12V *
+3.8V *
SW570B (8)
SW570A (8)
-3.5V *
-50V *
GND *
C329
100%
0%
ZONE *
A 100% ZONE
A 0% ZONE
A 100% AVG
A 0% AVG
A 100% TWELVE
A 0% TWELVE
J3
WAYCNP
+12V
GND
J301
(FRONT PANEL AT R505)
* DENOTES BUS
( ) INDICATES SWITCH POSITION
J1


J201
19 27 20 28 25 33 24 32 21 29 22 30 23 31
B 0% (8)
B 100% (8)
B 0% (4)
B 100% (4)
B 0% WIDTH (2CM)
B 100% WIDTH (2CM)
B 0% WIDTH (4CM)
B 100% WIDTH (4CM)
B 0% (2)
B 100% (2)
B 0% (1)
B 100% (1)
B 0% (.5)
B 100% (.5)
J1
B
ZONE*
W
SWEEP GATE
M
50V RAMP
J5
3
16 SW580B (.5)
SW580A (.5)
16 SW580B (1)
SW580A (1)
16 SW580B (2)
SW580A (2)
15 SW582 (4CM)
SW581 (4CM)
15 SW582 (2CM)
SW581 (2CM)
16 SW580B (4)
SW580A (4)
16 SW580B (8)
SW580A (8)
15 BIAS*
16 +1.75V*
18 +50V*
20 +12V*
22 +3.8V*
24 -3.5V*
26 -50V*
28 GND*
J3
5
100% 0%
SWEEP GATE*
SWEEP RAMP*
ZONE
B 100% ZONE
B 0% ZONE
B 100% AVG
B 0% AVG
100% TWELVE
0% TWELVE
GND*
BIAS*
+1.75V*
+50V*
+12V*
+3.8V*
-3.5V*
-50V*
8
J9
L
W
A
Y
C
N
P
J4
5
A
D
S
T
V
X
Z
BB
DD
FF
J1
J2
*DENOTES BUS
( ) INDICATES SWITCH POSITION

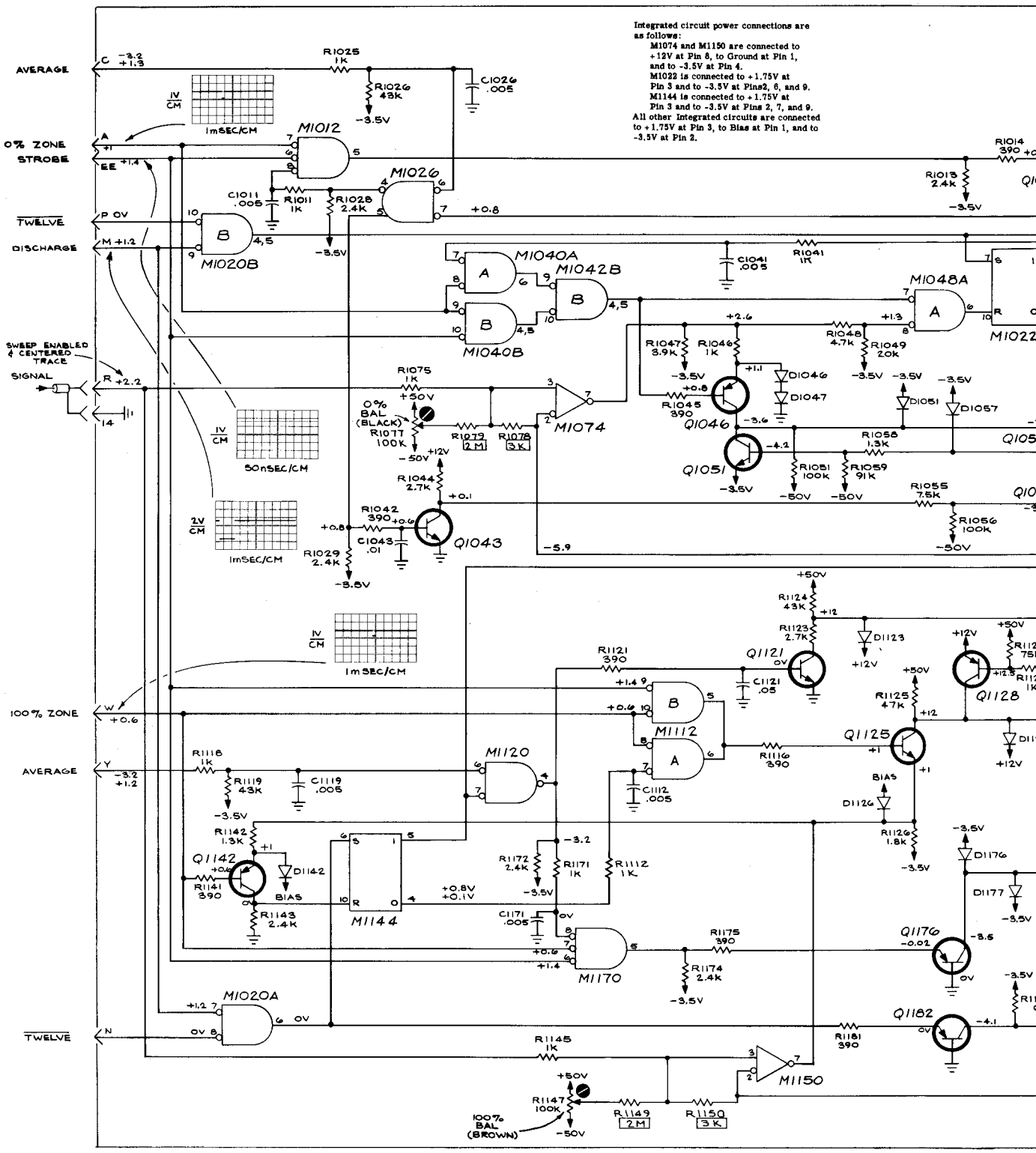

0%
100%
M838
M938
SWEEP GATE
ZONE
ZONE
AVERAGE
TWELVE
BIAS
WIDTH 2 CM
WIDTH 4 CM
POSITION 0.5
POSITION 1
POSITION 2
POSITION 4
POSITION 8
2mSEC/CM
1mSEC/CM
50V SWEEP RAMP
100% POSITION (BLACK)
0% POSITION (BRN-own)
100% WIDTH (WHITE)
0% WIDTH (ORANGE)
Integrated circuits on this diagram are connected to +1.75V at Pin 3, to Bias at Pin 1, and to -3.5V at Pin 2.
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
VOLTAGES and WAVEFORMS were obtained under conditions given on Block Diagram.
ZONE GENERATOR CARD



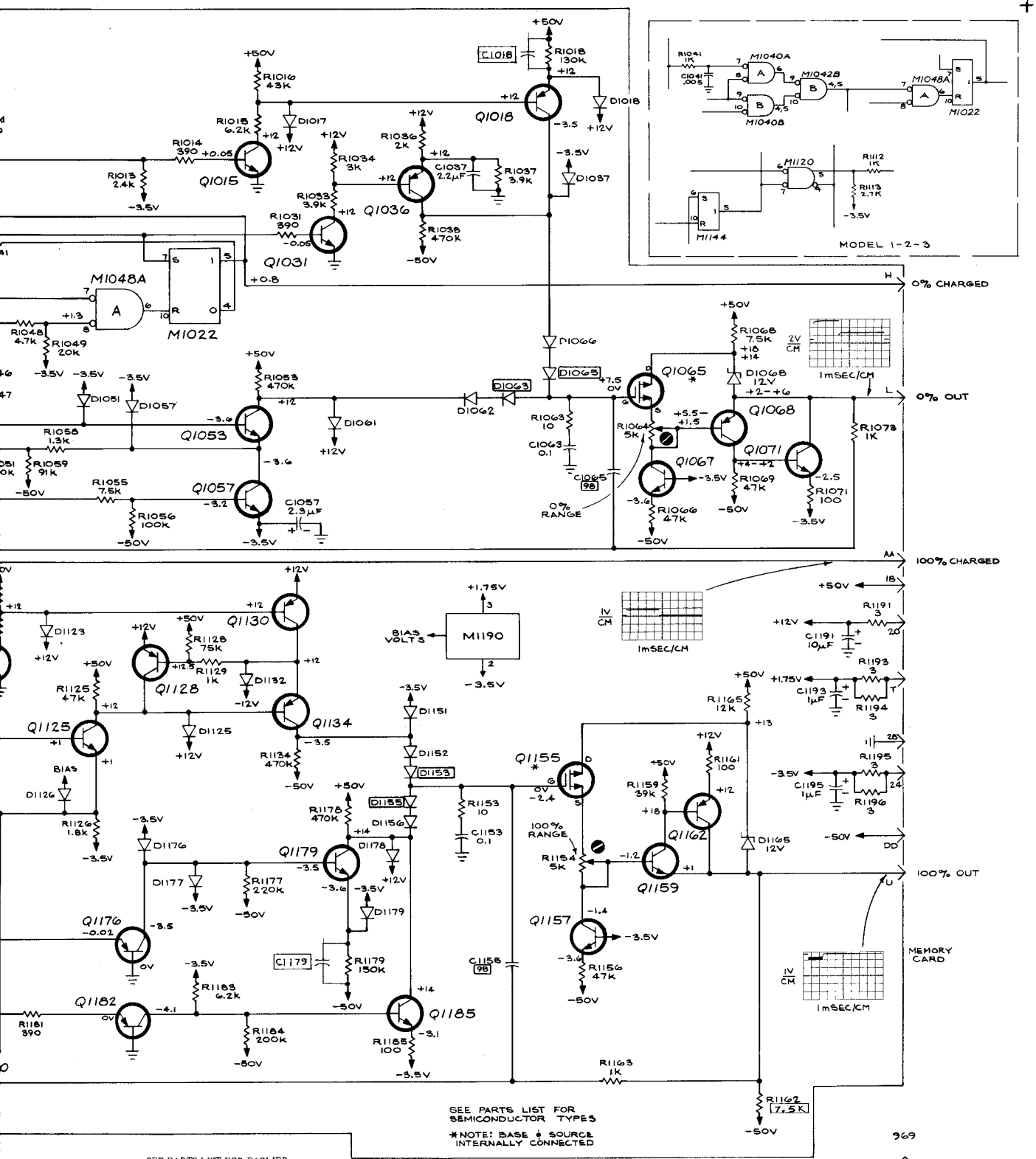
*DENOTES BUS



*DENOTES BUS



TYPE 230 DIGITAL UNIT

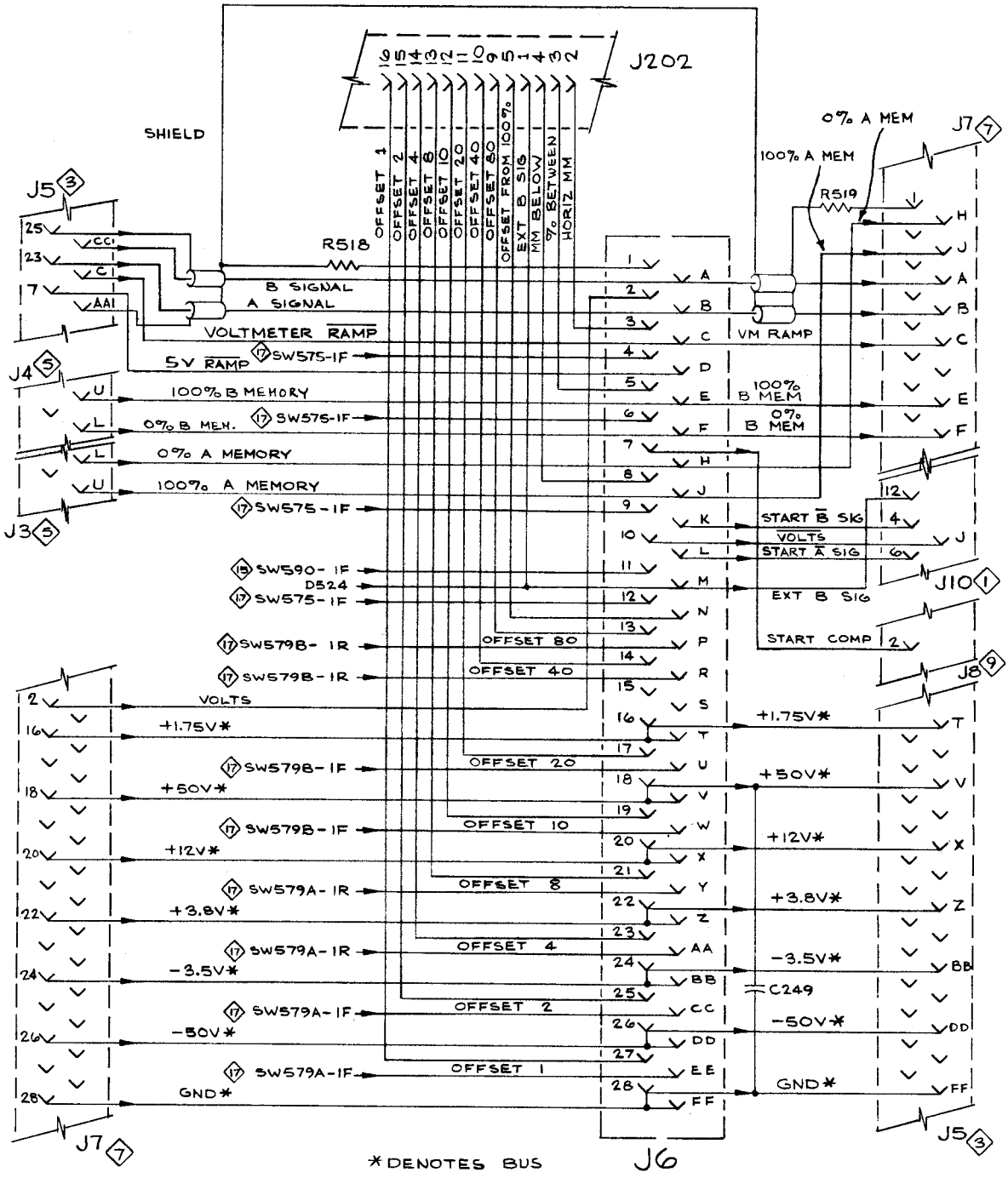


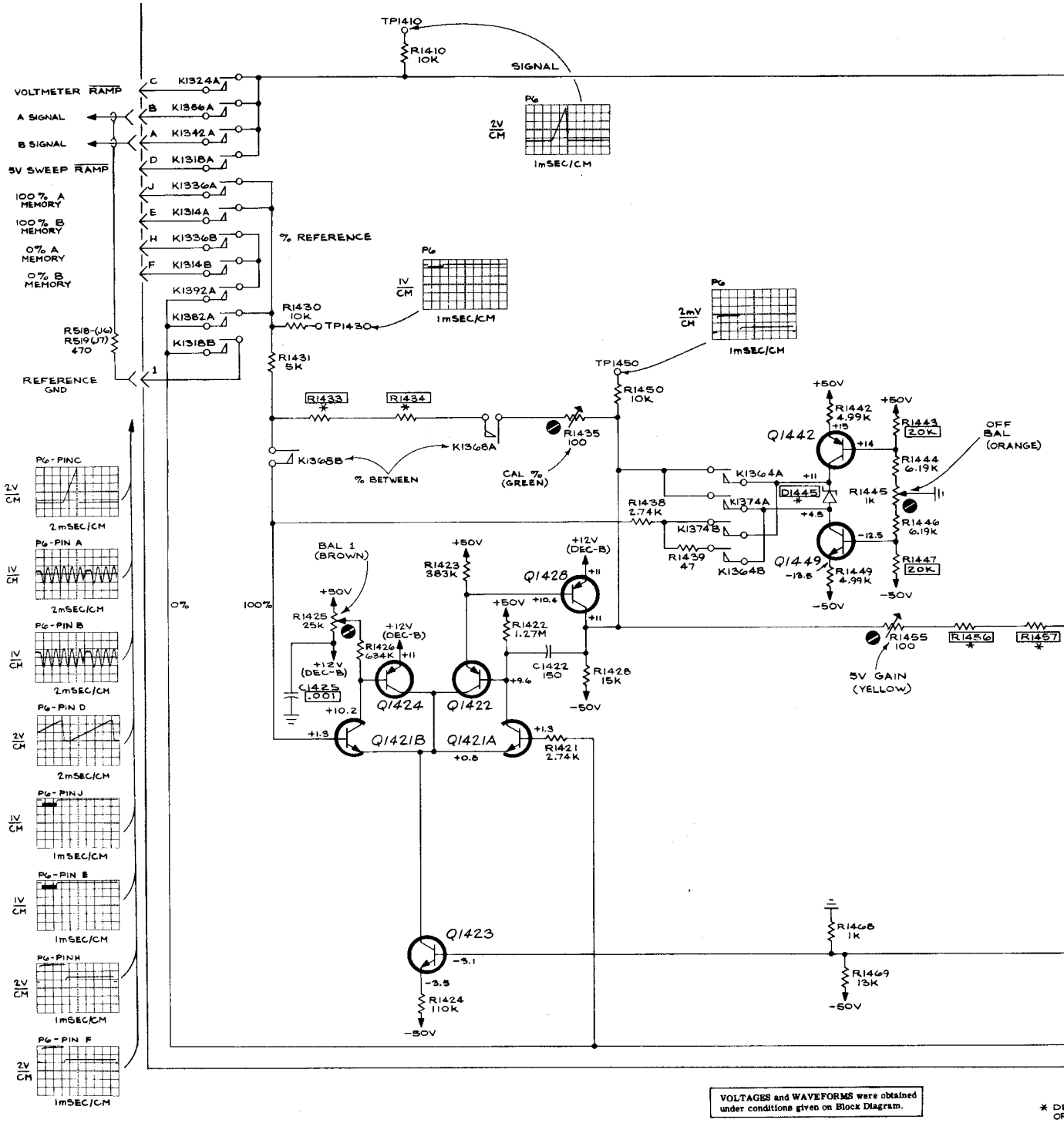
D SEE PARTS LIST FOR EARLIER VALUES AND CIRCUIT CARD MODEL NUMBERS OF PARTS MARKED WITH BLUE OUTLINE.

P3(A) & P4(B) MEMORY

(SERIES B, MODEL 1-UP)

5

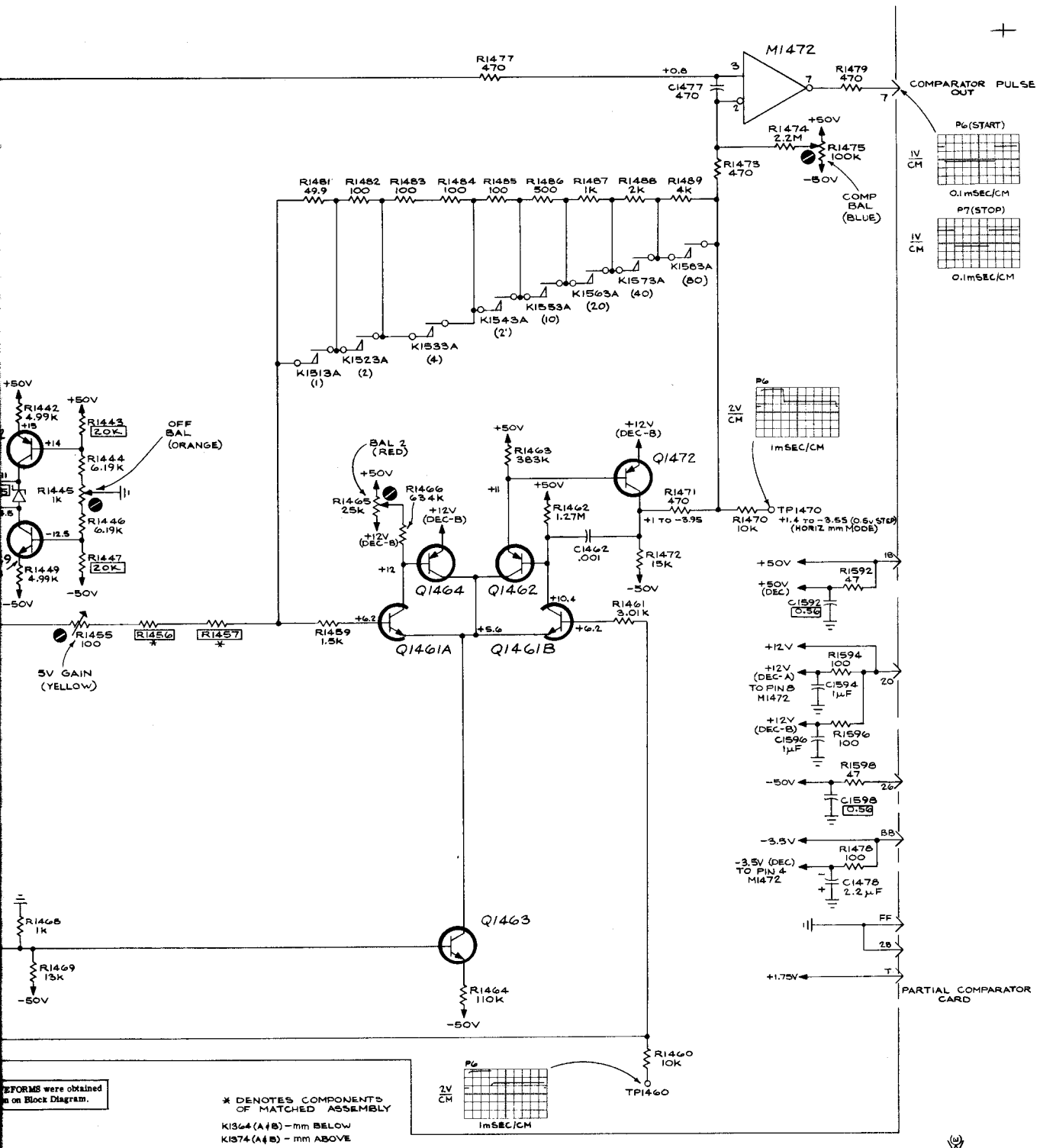

J202
SHIELD
J5
J4
J3
R518
B SIGNAL
A SIGNAL
VOLTMETER RAMP
5V RAMP
100% B MEMORY
0% B MEM.
0% A MEMORY
100% A MEMORY
SW575-1F
SW590-1F
D524
SW579B-1R
SW579B-1F
SW579A-1R
SW579A-1F
VOLTS
+1.75V*
+50V*
+12V*
+3.8V*
-3.5V*
-50V*
GND*
OFFSET 80
OFFSET 40
OFFSET 20
OFFSET 10
OFFSET 8
OFFSET 4
OFFSET 2
OFFSET 1
OFFSET FROM 100%
EXT B SIG
MM BELOW
% BETWEEN
HORIZ MM
J7
R519
0% A MEM
100% A MEM
VM RAMP
100% B MEM
0% B MEM
START B SIG
VOLTS
START A SIG
EXT B SIG
J10
START COMP
J8
C249
J5
J6
*DENOTES BUS



VOLTAGES and WAVEFORMS were obtained under conditions given on Block Diagram.

SEE PARTS LIST FOR EARLIER VALUES AND CIRCUIT CARD MODEL NUMBERS OF PARTS MARKED WITH BLUE OUTLINE.

TYPE 230 DIGITAL UNIT



* DENOTES COMPONENTS OF MATCHED ASSEMBLY

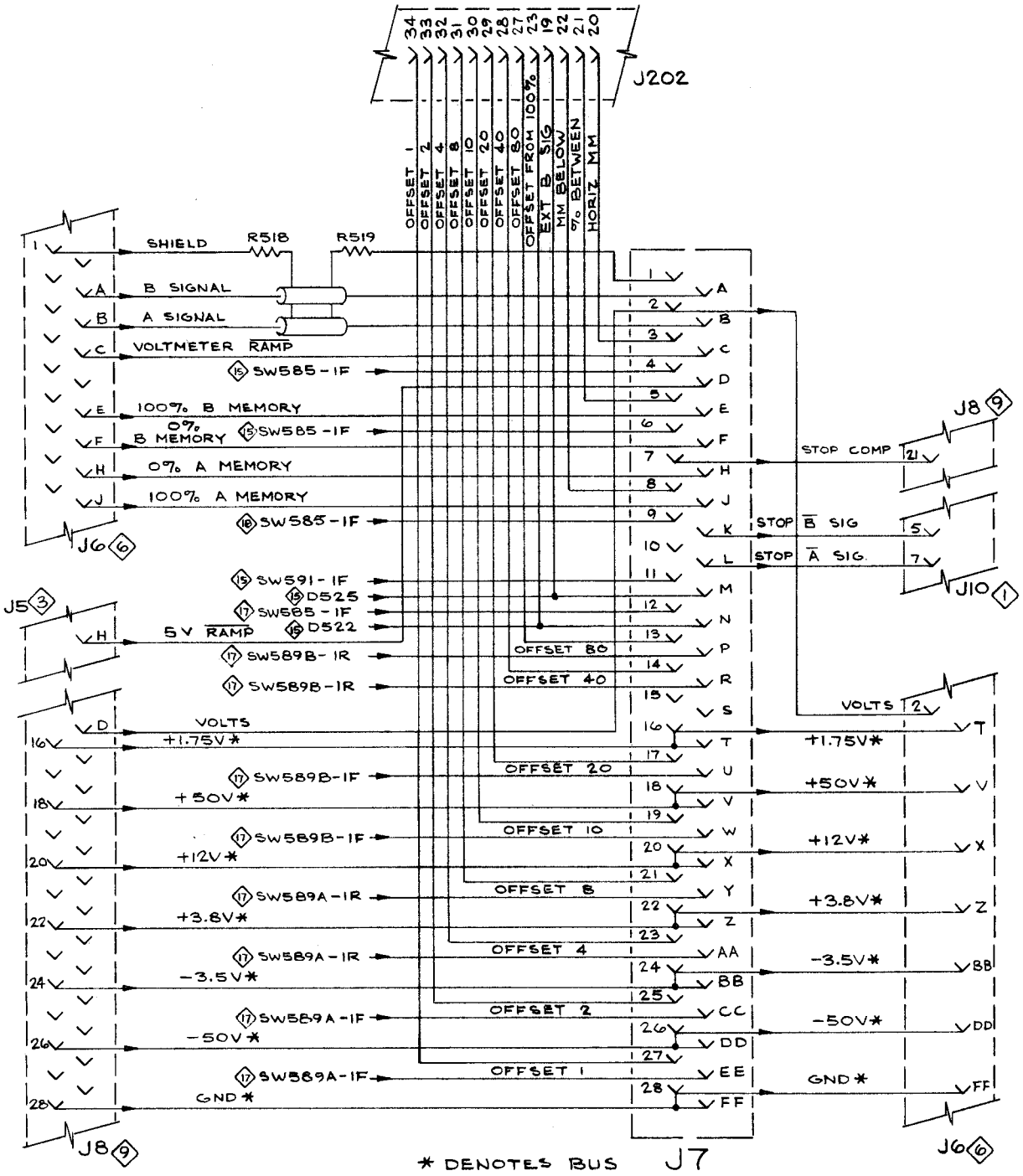
K1364 (A&B) – mm BELOW
K1374 (A&B) – mm ABOVE

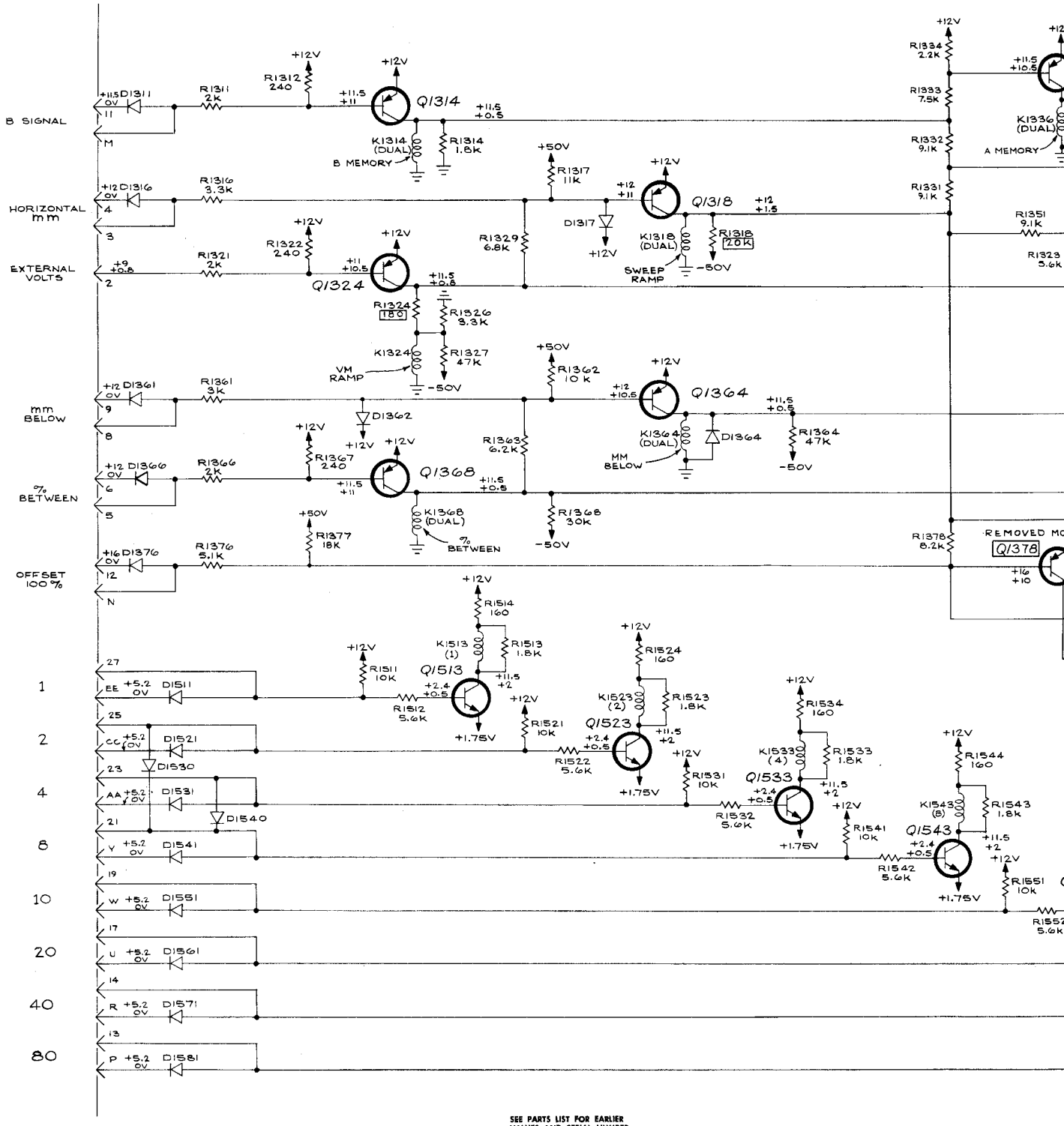
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

669

P6(START) & P7(STOP) - COMPARATOR ⑥
— OFFSET GENERATOR —

(SERIES D, MODEL 1 - UP)

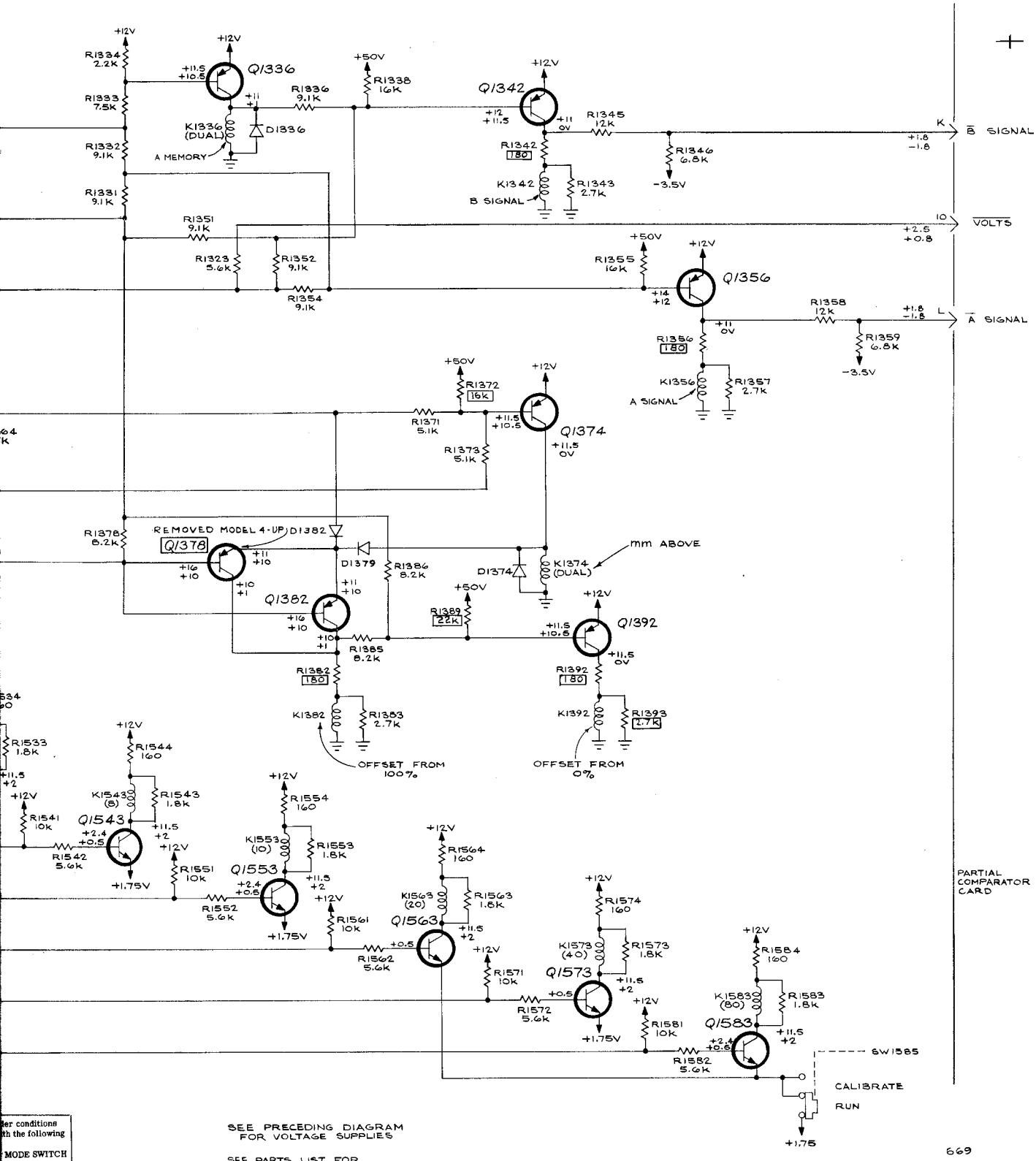

J202
34 33 32 31 30 29 28 27 23 19 22 21 20
OFFSET 1
OFFSET 2
OFFSET 4
OFFSET 8
OFFSET 10
OFFSET 20
OFFSET 40
OFFSET 80
OFFSET FROM 100%
EXT B SIG
MM BELOW
% BETWEEN
HORIZ MM
SHIELD
R518
R519
B SIGNAL
A SIGNAL
VOLTMETER RAMP
SW585-1F
100% B MEMORY
0% B MEMORY
SW585-1F
0% A MEMORY
100% A MEMORY
SW585-1F
J6
SW591-1F
D525
SW585-1F
5V RAMP
D522
SW589B-1R
SW589B-1R
J5
VOLTS +1.75V*
SW589B-1F
+50V*
SW589B-1F
+12V*
SW589A-1R
+3.8V*
SW589A-1R
-3.5V*
SW589A-1F
-50V*
SW589A-1F
GND*
J8
OFFSET 80
OFFSET 40
OFFSET 20
OFFSET 10
OFFSET 8
OFFSET 4
OFFSET 2
OFFSET 1
J7
STOP COMP
STOP B SIG
STOP A SIG
J8
J10
VOLTS
+1.75V*
+50V*
+12V*
+3.8V*
-3.5V*
-50V*
GND*
J6
* DENOTES BUS



SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

VOLTAGES were taken under conditions given on Block Diagram with the following additions:
Type 230 MEASUREMENT MODE SWITCH set to TIME.

TYPE 230 DIGITAL UNIT



der conditions
th the following
MODE SWITCH

SEE PRECEDING DIAGRAM FOR VOLTAGE SUPPLIES

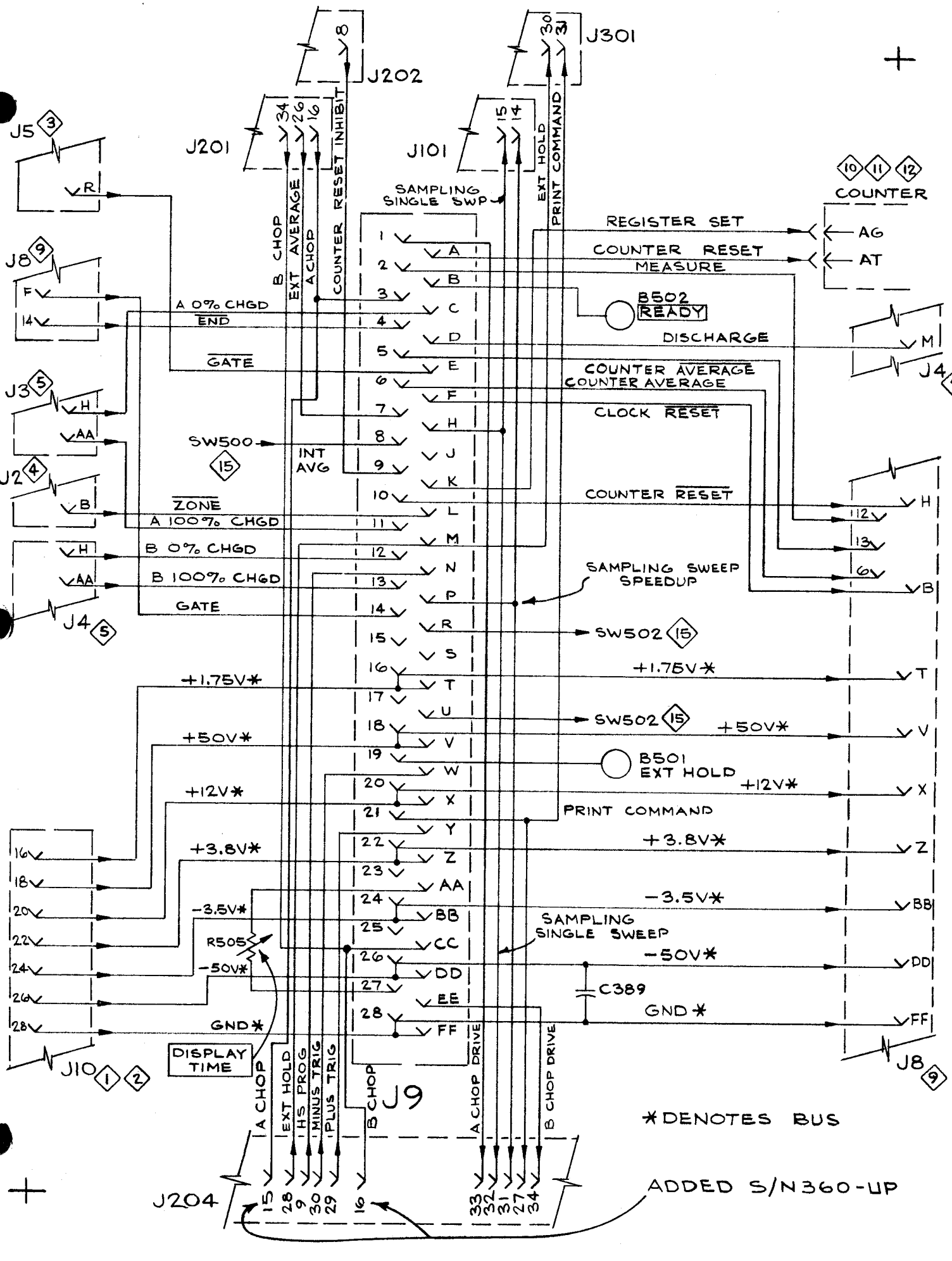
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

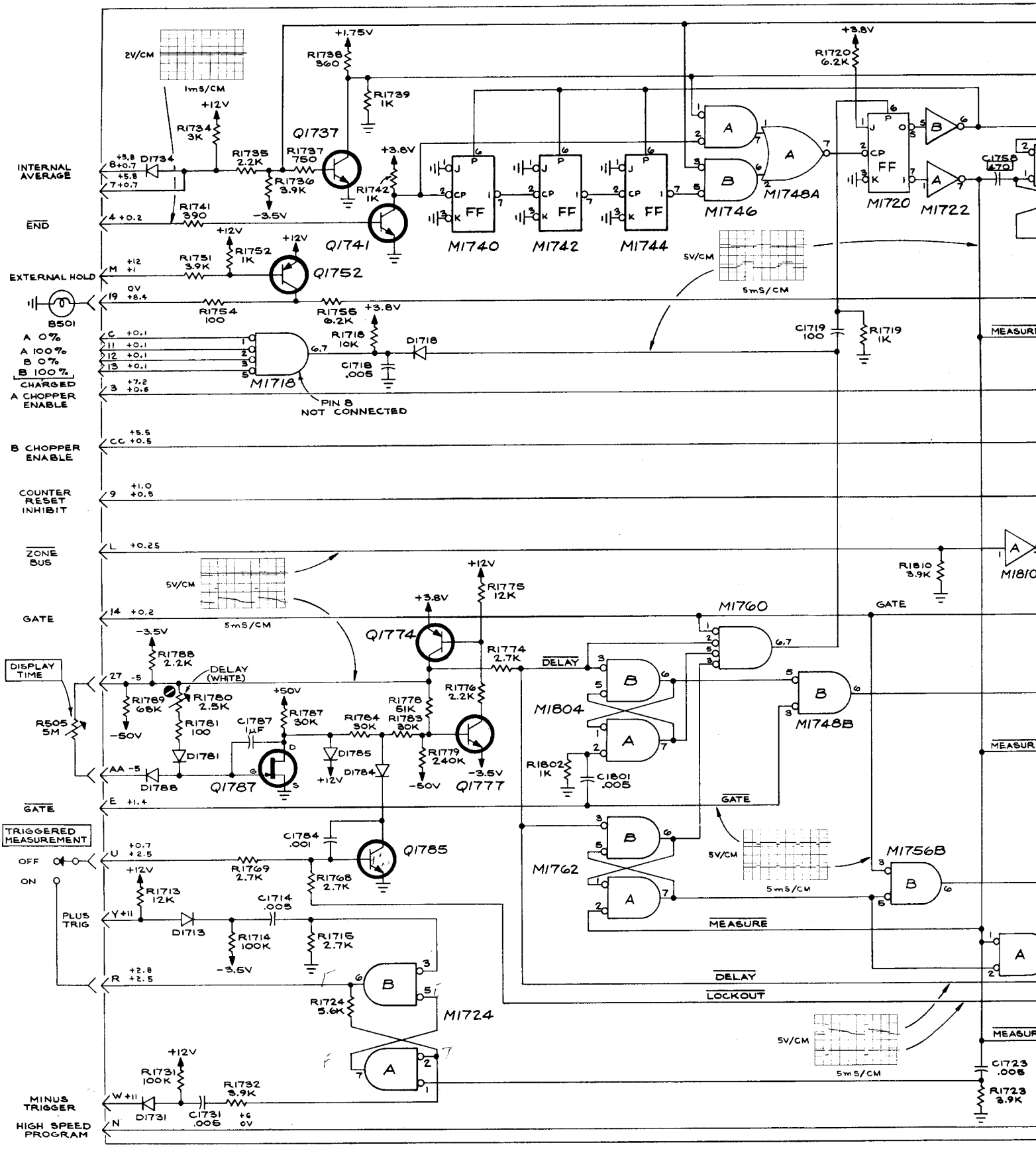
669

P6 (START) & P7 (STOP) — COMPARATOR ⟨7⟩

— PROGRAM LOGIC —

(SERIES D, MODEL 1 — UP)

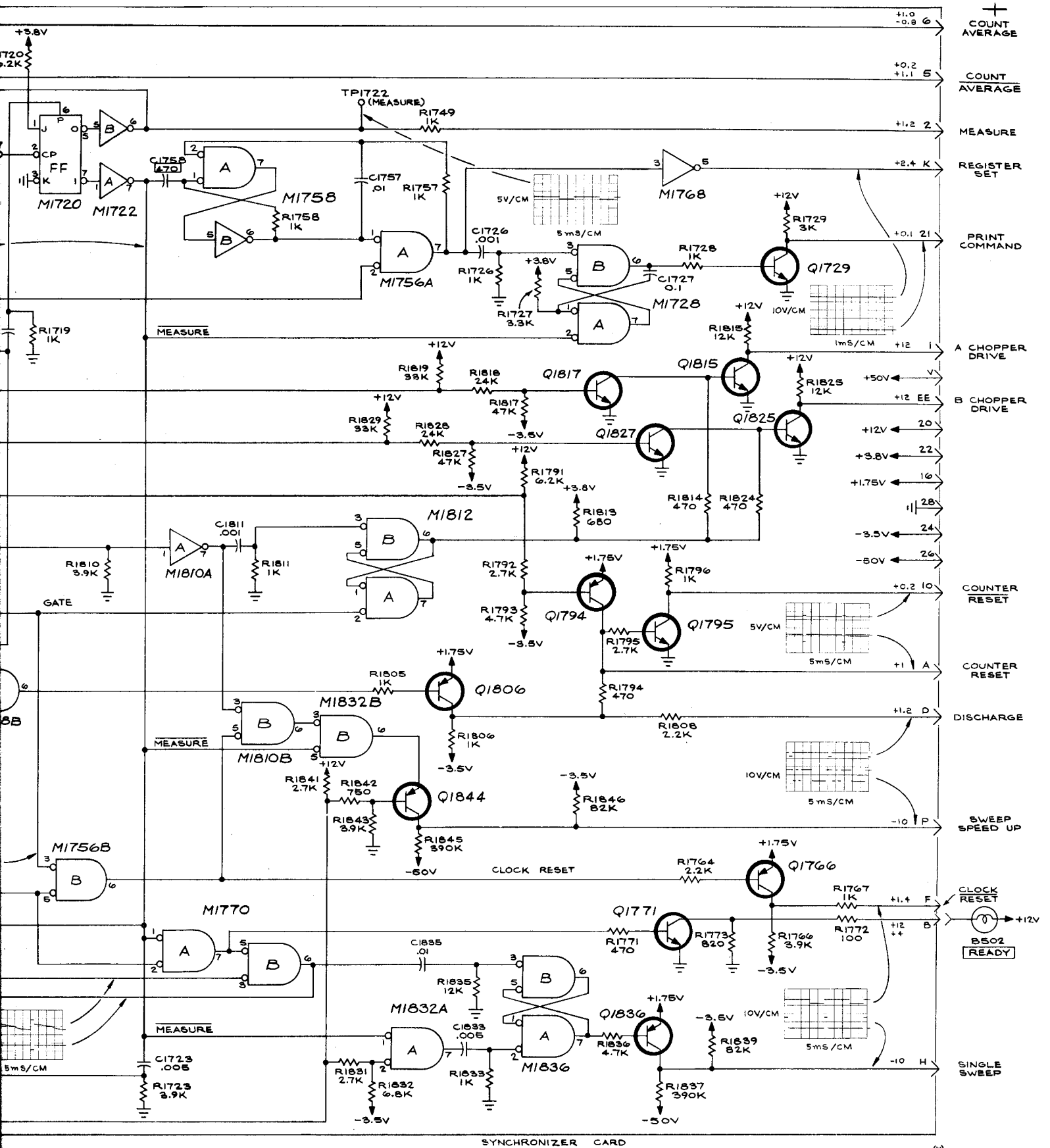

J202
J301
J201
J101
J5
J8
J3
J2
J4
J10
J204
J9
SAMPLING SINGLE SWP
EXT HOLD
PRINT COMMAND
B CHOP
EXT AVERAGE
A CHOP
COUNTER RESET INHIBIT
COUNTER
REGISTER SET
AG
COUNTER RESET
MEASURE
AT
B502 READY
A 0% CHGD
END
GATE
DISCHARGE
COUNTER AVERAGE
COUNTER AVERAGE
CLOCK RESET
SW500
INT AVG
ZONE
A 100% CHGD
B 0% CHGD
B 100% CHGD
GATE
COUNTER RESET
SAMPLING SWEEP SPEEDUP
SW502
+1.75V*
+50V*
B501 EXT HOLD
+12V*
PRINT COMMAND
+3.8V*
-3.5V*
R505
SAMPLING SINGLE SWEEP
-50V*
C389
GND*
DISPLAY TIME
A CHOP
EXT HOLD
HS PROG
MINUS TRIG
PLUS TRIG
B CHOP
A CHOP DRIVE
B CHOP DRIVE
*DENOTES BUS
ADDED S/N360-UP



TYPE 230 DIGITAL UNIT

SEE PARTS LIST FOR EARLIER VALUES AND CIRCUIT CARD MODEL NUMBERS OF PARTS MARKED WITH BLUE OUTLINE.

D1



SYNCHRONIZER CARD

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

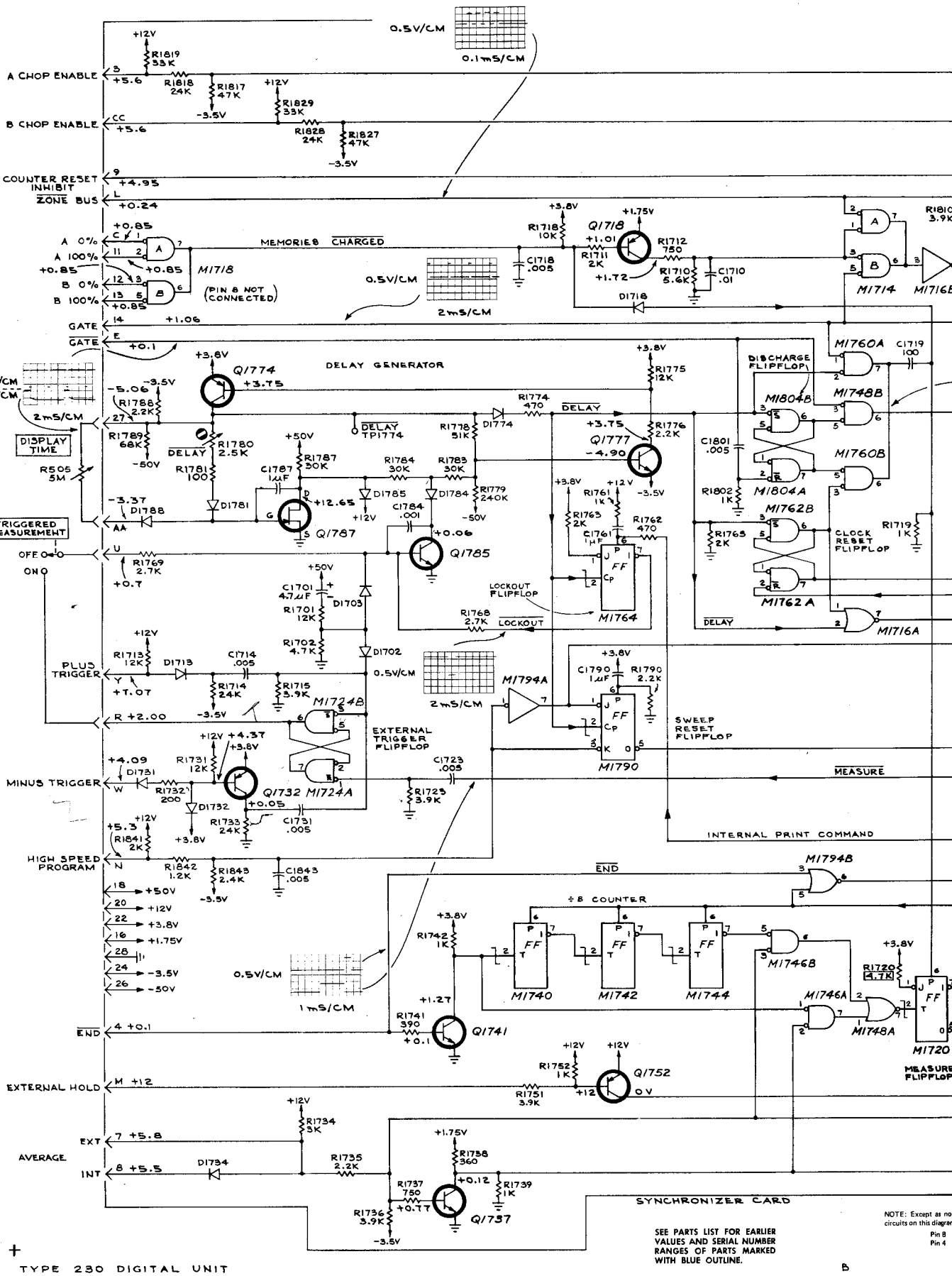
NOTE: Except as noted on specific devices, all integrated circuits on this diagram have these power connections:
Pin 8 - +3.8V
Pin 4 - Gnd

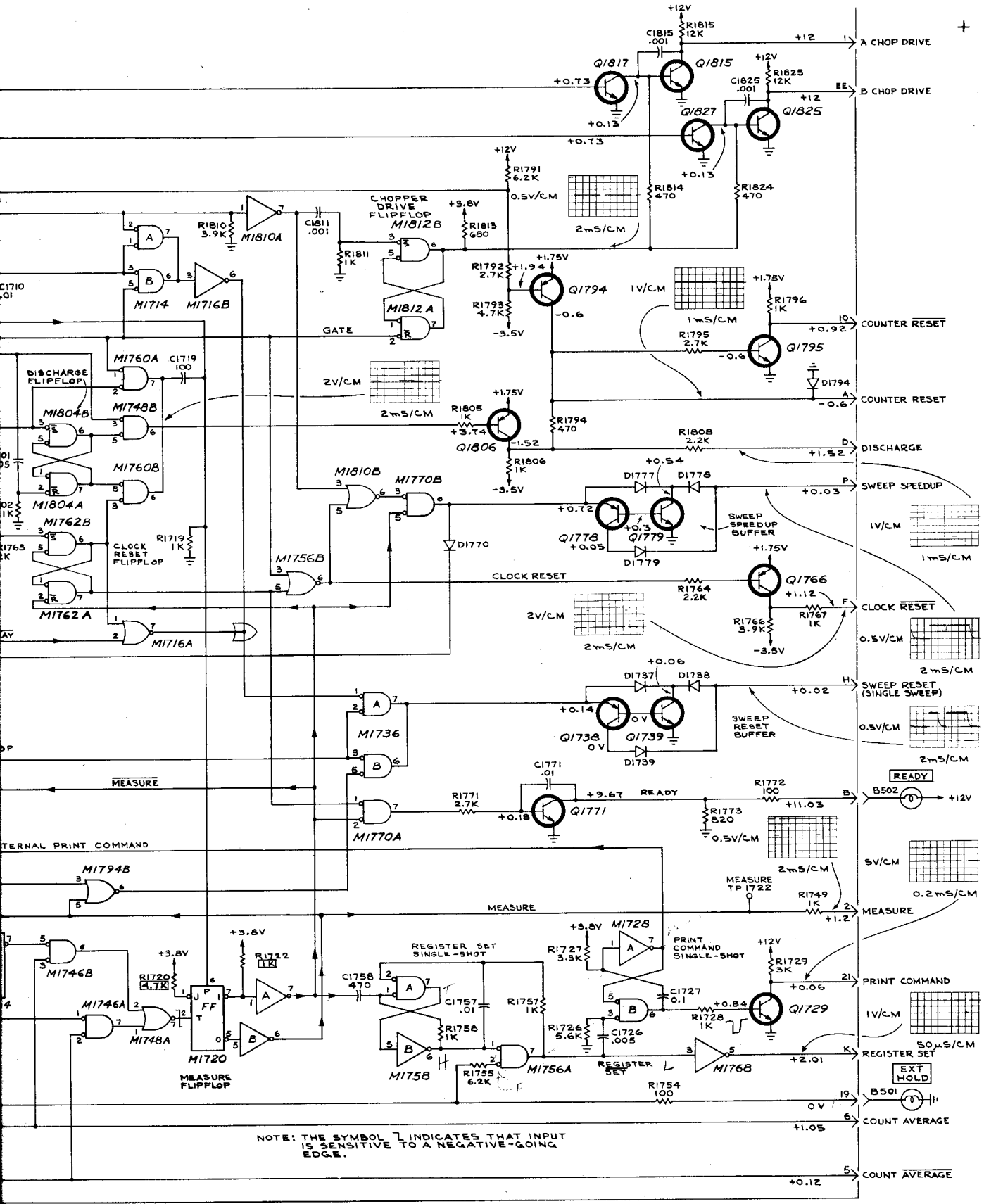
669

P9 SYNCHRONIZER (8)

(SERIES F, MODEL 1 & 2)

D1


A CHOP ENABLE
B CHOP ENABLE
COUNTER RESET INHIBIT
ZONE BUS
A 0%
A 100%
B 0%
B 100%
MEMORIES CHARGED
M1718
(PIN 8 NOT CONNECTED)
GATE
DELAY GENERATOR
Q1774
Q1777
Q1787
Q1785
DISPLAY TIME
TRIGGERED MEASUREMENT
OFF
ON
PLUS TRIGGER
MINUS TRIGGER
HIGH SPEED PROGRAM
EXTERNAL HOLD
AVERAGE
EXT
INT
EXTERNAL TRIGGER FLIPFLOP
M1724A
LOCKOUT FLIPFLOP
M1764
SWEEP RESET FLIPFLOP
M1790
DISCHARGE FLIPFLOP
M1760A
M1748B
M1760B
M1804A
M1762B
CLOCK RESET FLIPFLOP
M1762A
M1716A
÷8 COUNTER
M1740
M1742
M1744
M1746B
M1746A
M1748A
M1720
MEASURE FLIPFLOP
M1794A
M1794B
Q1732
Q1741
Q1752
Q1737
MEASURE
END
INTERNAL PRINT COMMAND
SYNCHRONIZER CARD
0.5V/CM
0.1mS/CM
2mS/CM
1mS/CM
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.
NOTE: Except as no
circuits on this diagra
Pin 8
Pin 4
TYPE 230 DIGITAL UNIT
B



NOTE: Except as noted on specific devices, all integrated circuits on this diagram have these power connections:
Pin 8 - +3.8V
Pin 4 - Gnd

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

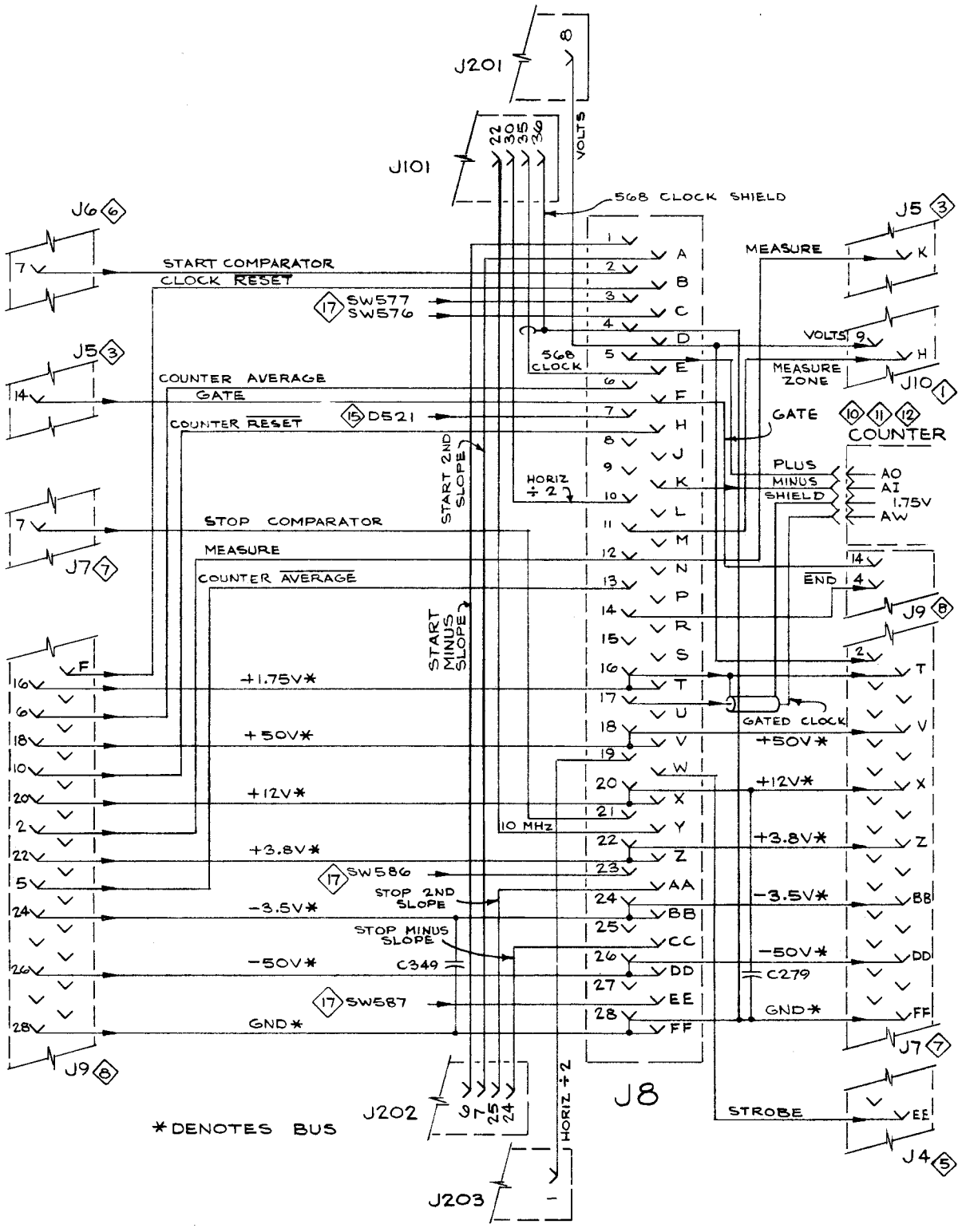
NOTE: ALL UNUSED I.C. INPUT PINS ARE GROUNDED.

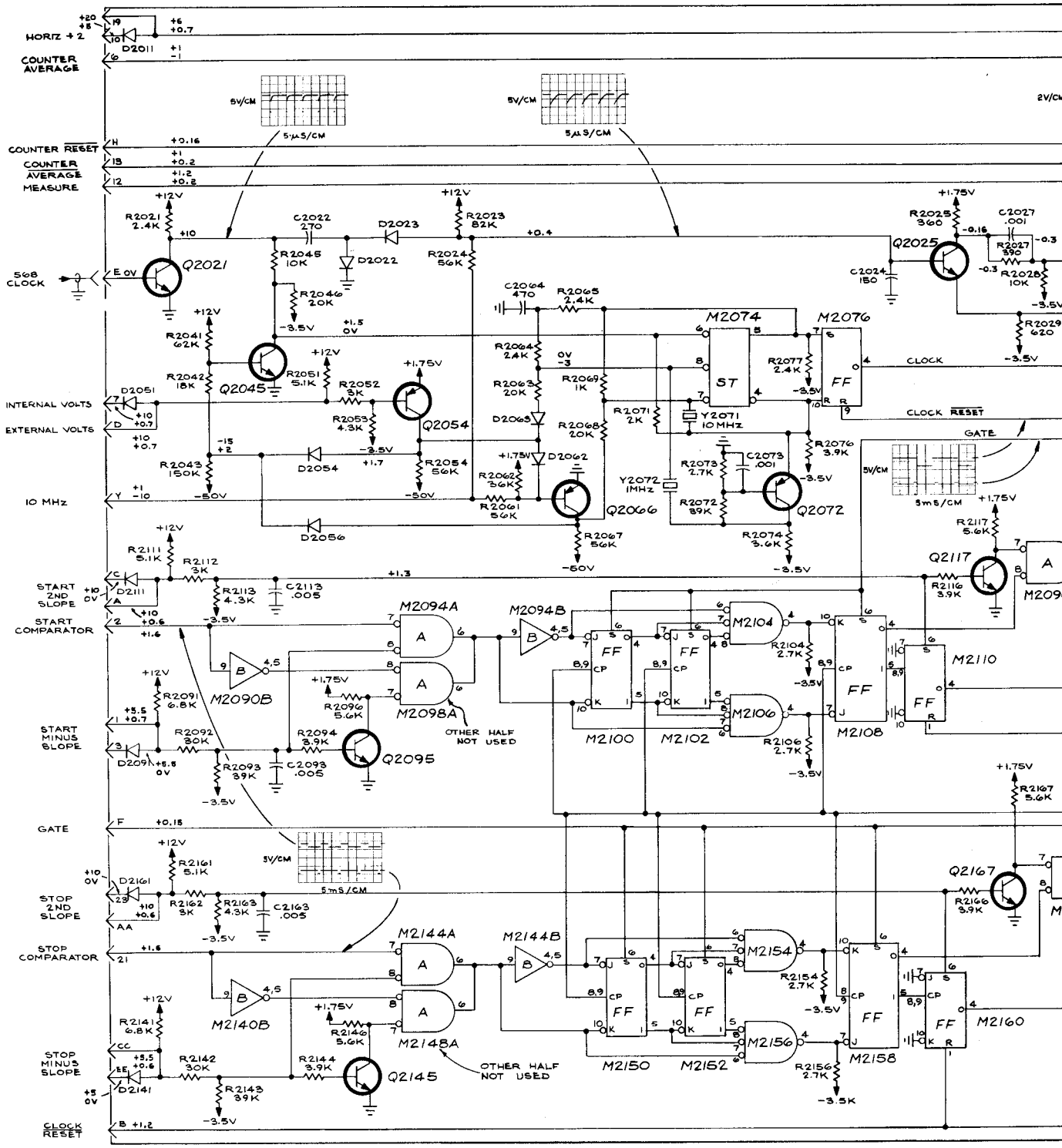
ZER CARD

FOR EARLIER RIAL NUMBER ARTS MARKED TLINE.

B

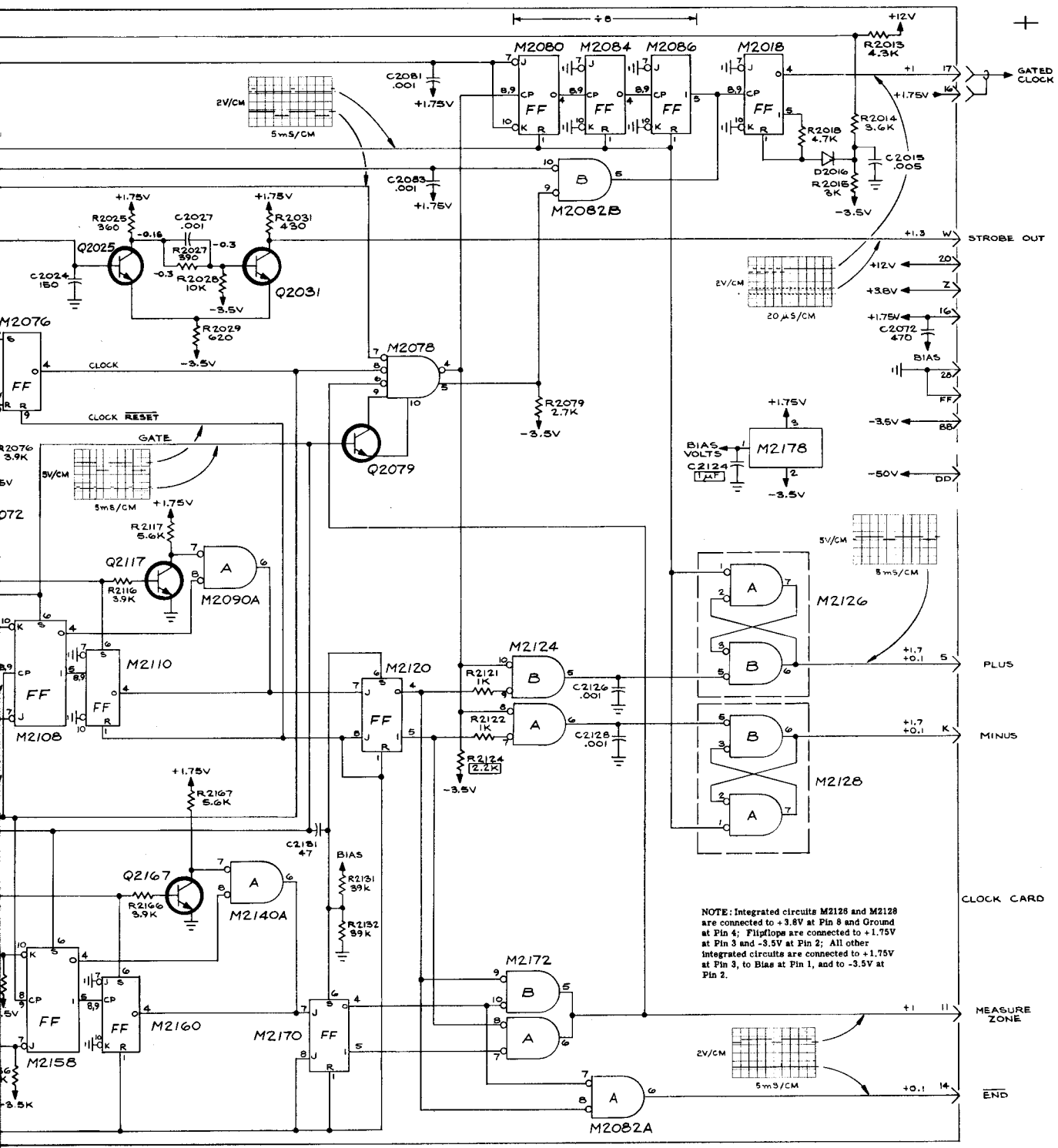
P9 SYNCHRONIZER (8)
(SERIES F, MODEL 3-UP)


J201
J101
22
30
35
36
VOLTS
568 CLOCK SHIELD
J6 6
J5 3
J7 7
J9 8
J8
J202
J203
J4 5
J10 1
J5 3
START COMPARATOR
CLOCK RESET
17 SW577
SW576
COUNTER AVERAGE GATE
COUNTER RESET
15 D521
STOP COMPARATOR
MEASURE
COUNTER AVERAGE
START 2ND SLOPE
START MINUS SLOPE
HORIZ ÷2
+1.75V*
+50V*
+12V*
+3.8V*
-3.5V*
-50V*
GND*
10 MHz
17 SW586
STOP 2ND SLOPE
STOP MINUS SLOPE
C349
17 SW587
568 CLOCK
MEASURE
VOLTS
MEASURE ZONE
GATE
10 11 12 COUNTER
PLUS
MINUS
SHIELD
AO
AI
1.75V
AW
END
GATED CLOCK
+50V*
+12V*
+3.8V*
-3.5V*
-50V*
C279
GND*
STROBE
*DENOTES BUS



TYPE 230 DIGITAL UNIT

SEE PA
VALUES
NUMBE
BLUE O



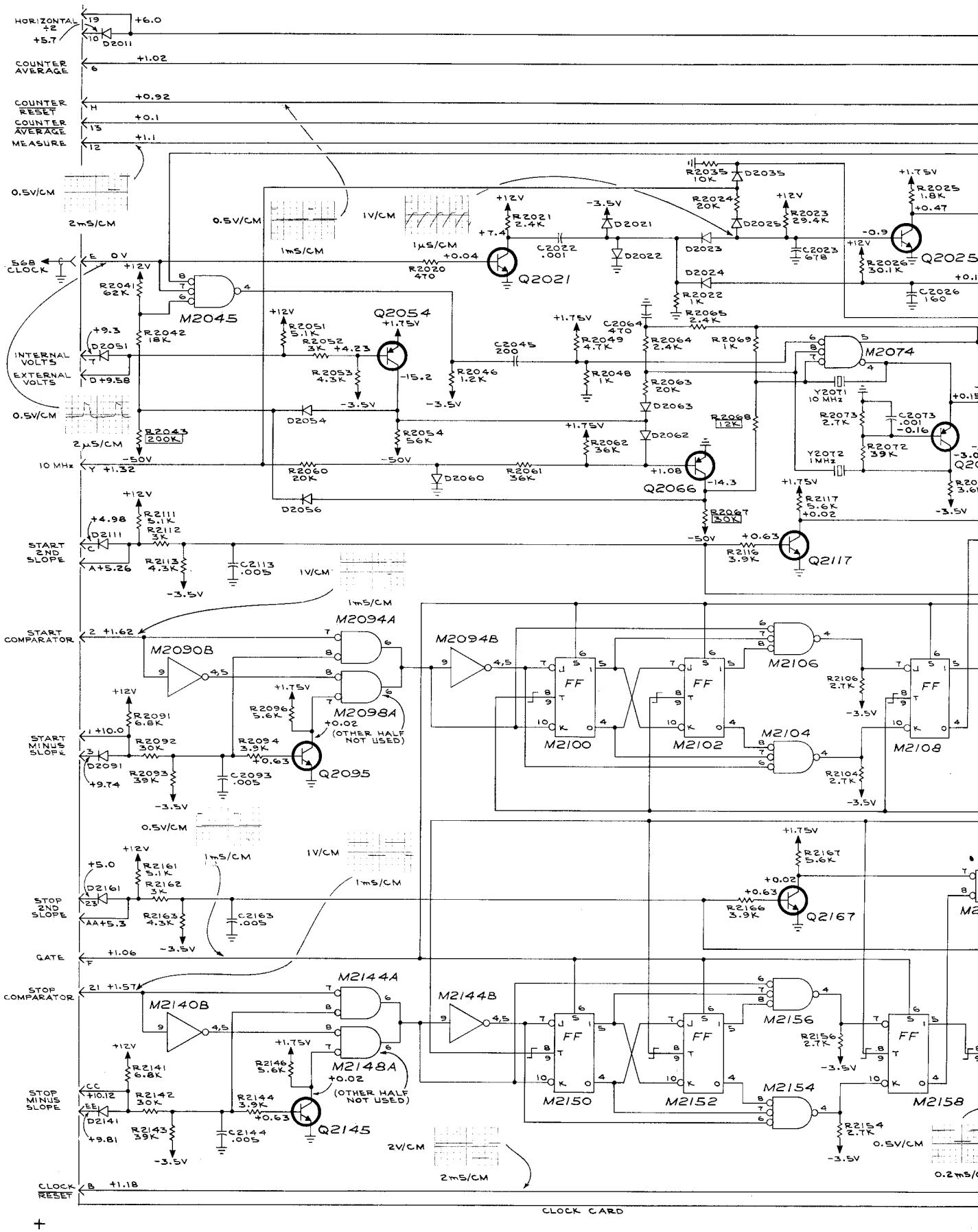
669

SEE PARTS LIST FOR EARLIER VALUES AND CIRCUIT CARD MODEL NUMBERS OF PARTS MARKED WITH BLUE OUTLINE.

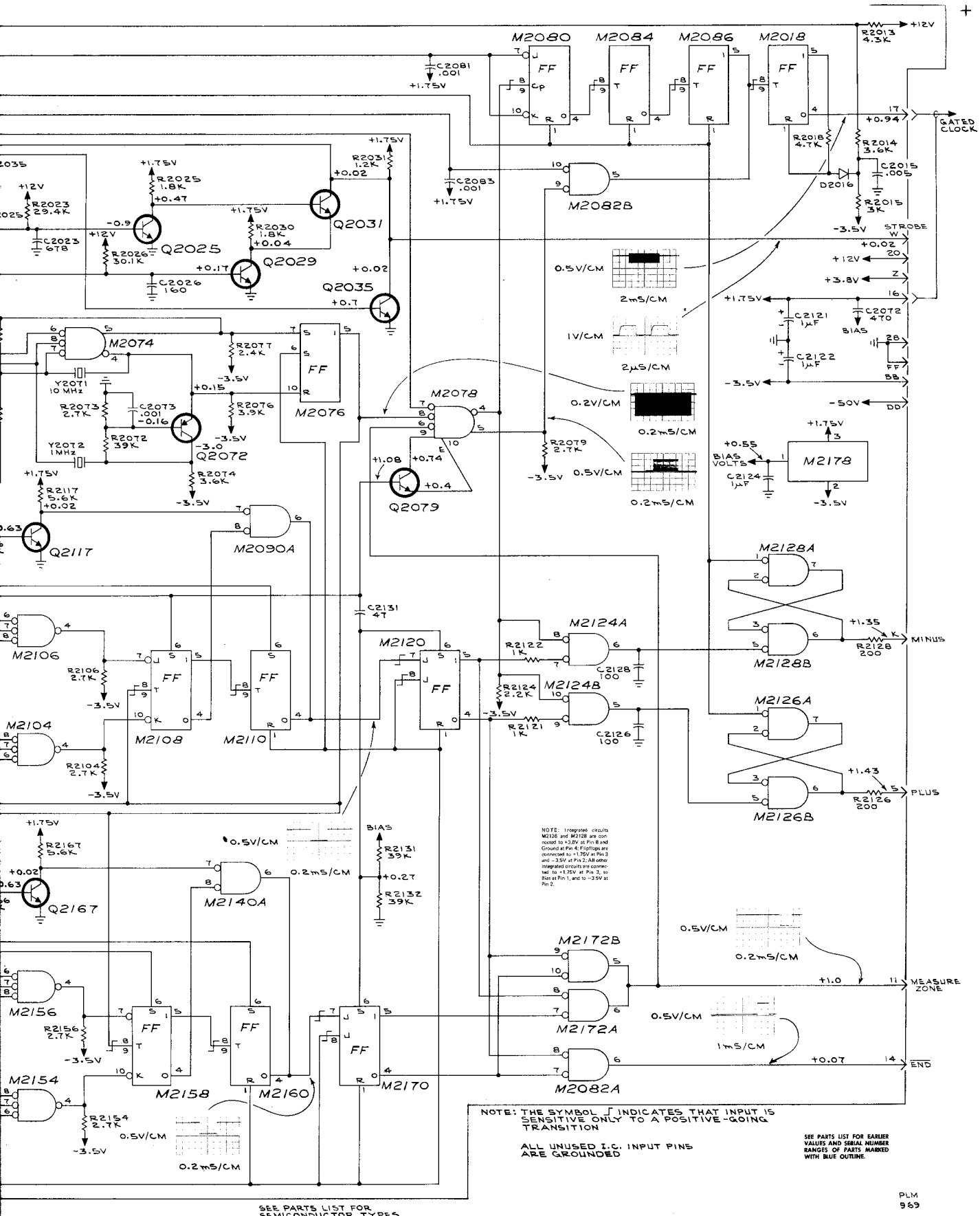
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

P8 CLOCK 9

(SERIES F, MODEL 1 & 2)

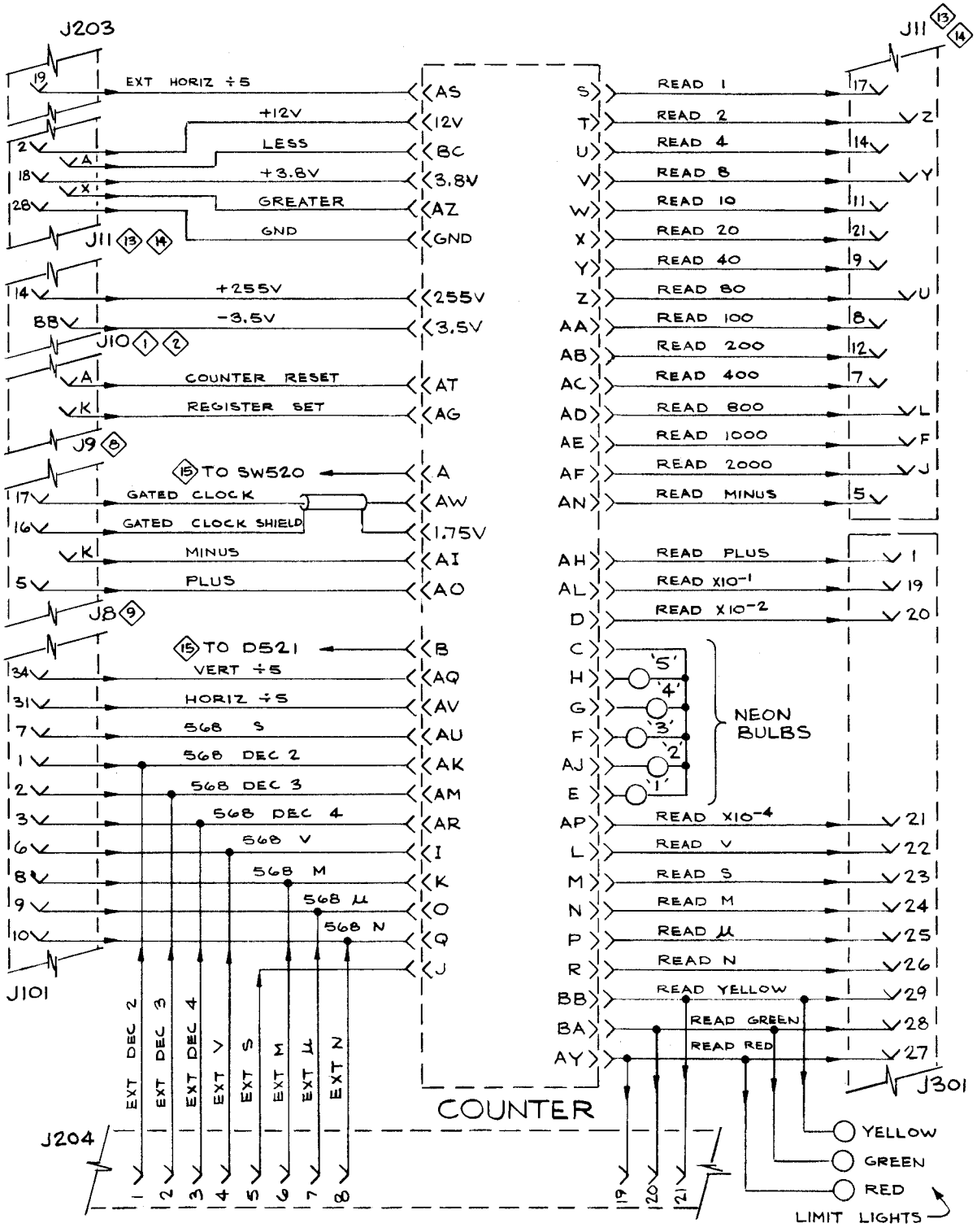


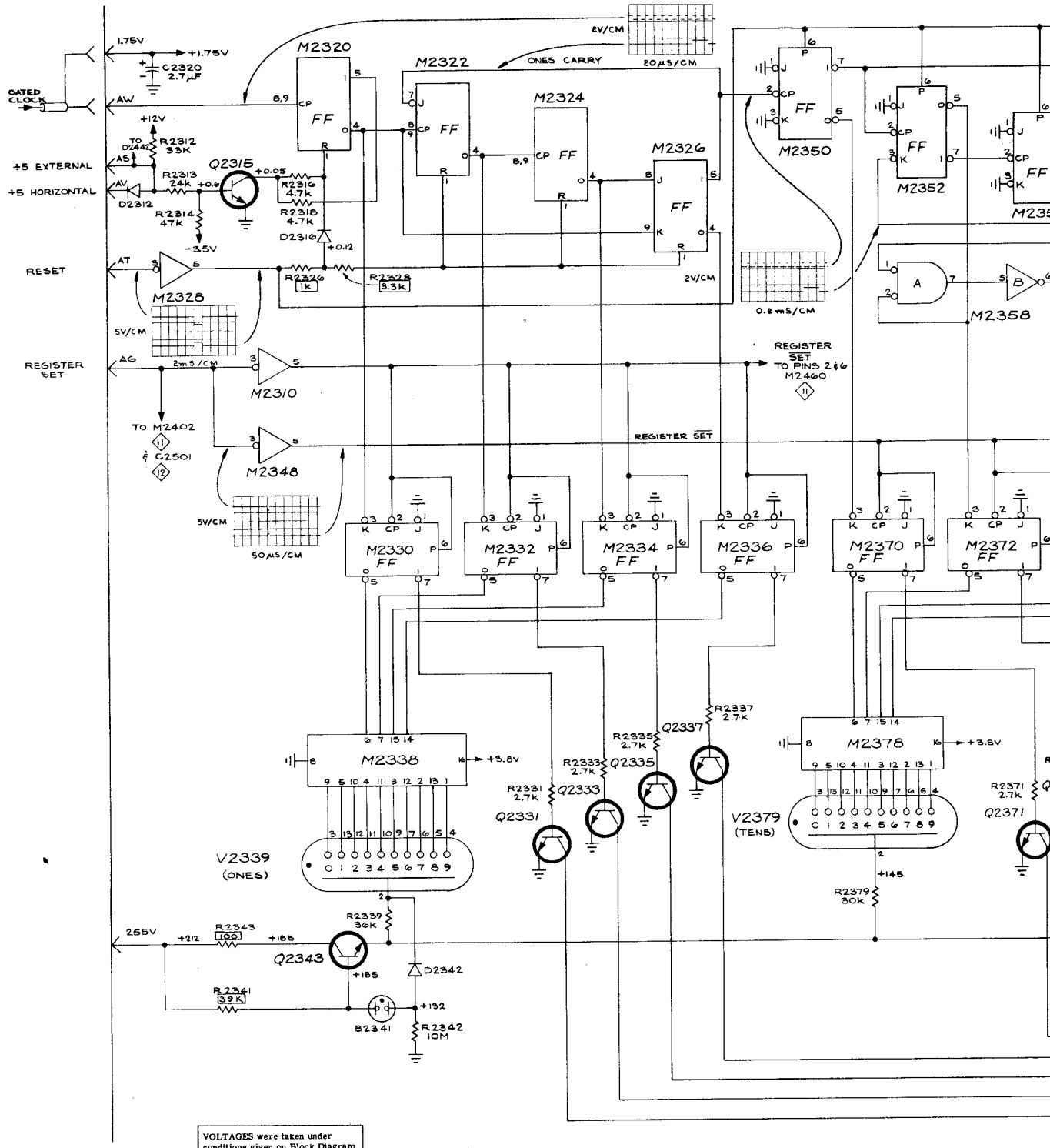
TYPE 230 DIGITAL UNIT



PLM
969

P8 CLOCK SERIES E MODEL 3-UP (9)


J203
EXT HORIZ ÷5
+12V
LESS
+3.8V
GREATER
GND
J11
+255V
-3.5V
J10
COUNTER RESET
REGISTER SET
J9
TO SW520
GATED CLOCK
GATED CLOCK SHIELD
MINUS
PLUS
J8
TO D521
VERT ÷5
HORIZ ÷5
568 S
568 DEC 2
568 DEC 3
568 DEC 4
568 V
568 M
568 μ
568 N
J101
AS
12V
BC
3.8V
AZ
GND
255V
3.5V
AT
AG
A
AW
1.75V
AI
AO
B
AQ
AV
AU
AK
AM
AR
I
K
O
Q
J
READ 1
READ 2
READ 4
READ 8
READ 10
READ 20
READ 40
READ 80
READ 100
READ 200
READ 400
READ 800
READ 1000
READ 2000
READ MINUS
READ PLUS
READ X10⁻¹
READ X10⁻²
NEON BULBS
READ X10⁻⁴
READ V
READ S
READ M
READ μ
READ N
READ YELLOW
READ GREEN
READ RED
J301
COUNTER
EXT DEC 2
EXT DEC 3
EXT DEC 4
EXT V
EXT S
EXT M
EXT μ
EXT N
J204
YELLOW
GREEN
RED
LIMIT LIGHTS



VOLTAGES were taken under conditions given on Block Diagram.

NOTE: Integrated circuits M2320, M2322, M2324, and M2326 are connected to -3.5V at Pin 2 and +1.75V at Pin 3; All other integrated circuits on this diagram (excluding M2338, M2378, and M2398) are connected to ground at Pin 4 and+3.8V at Pin 8.

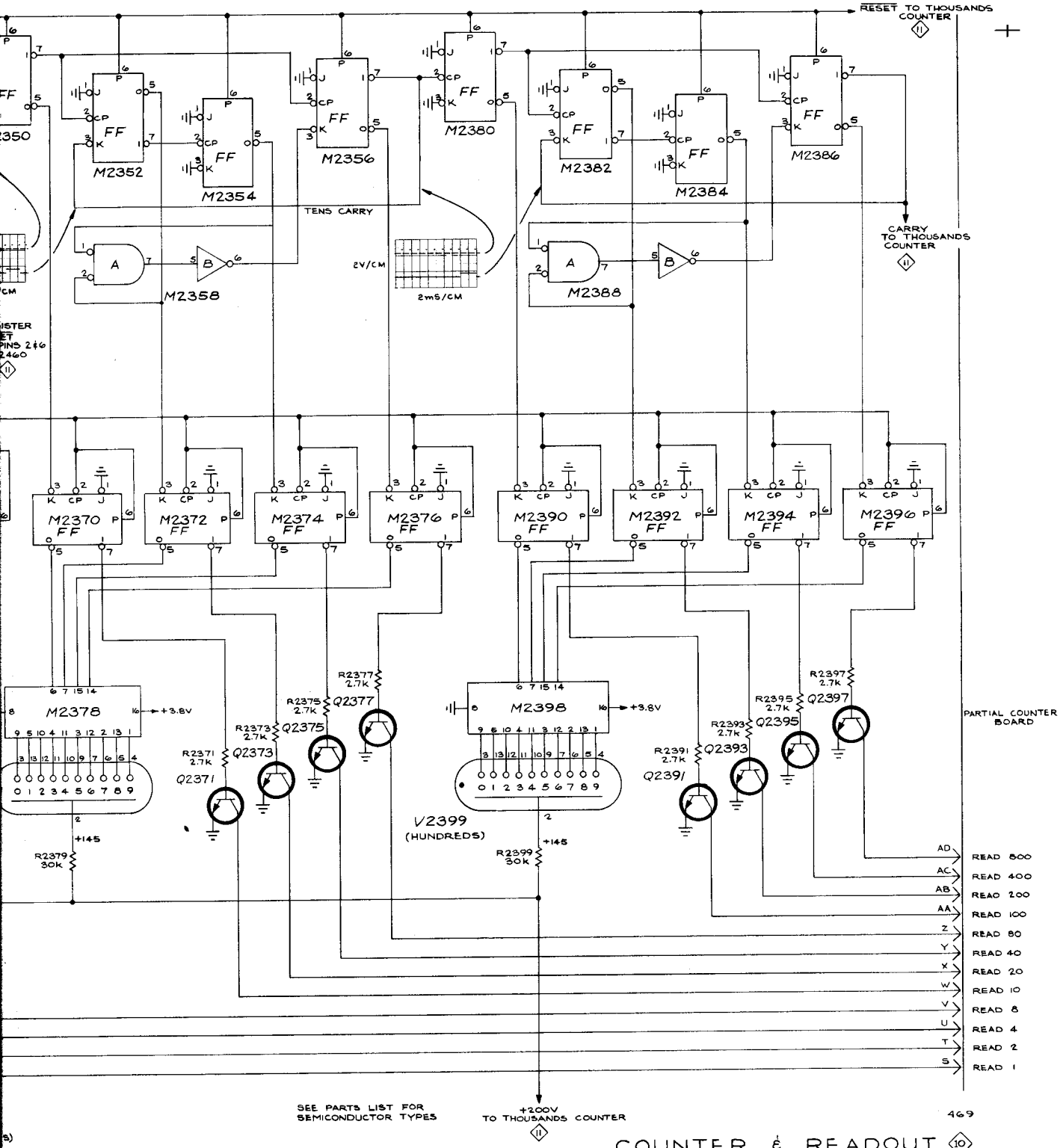
REFERENCE DIAGRAMS

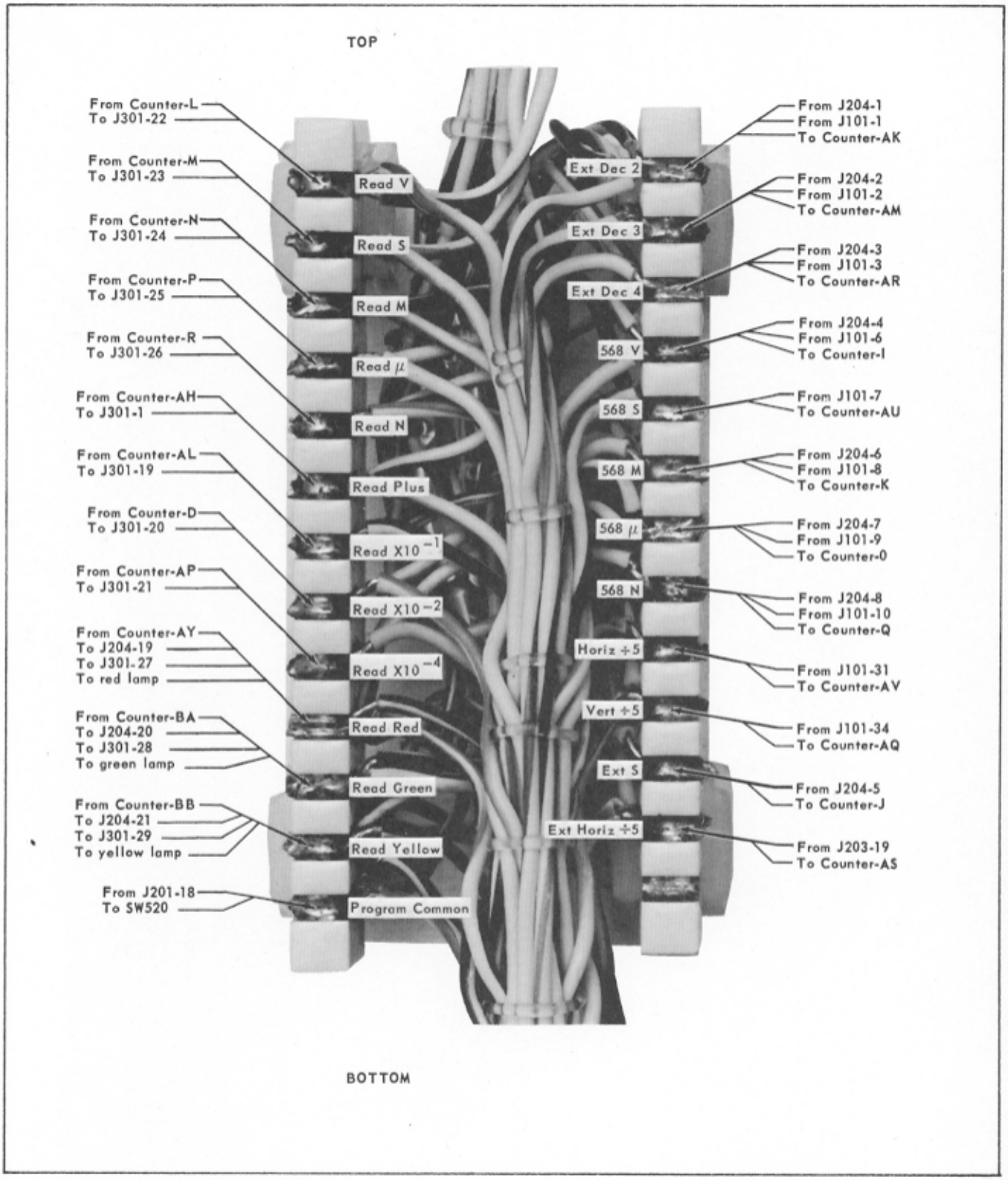
(11) COUNTER & READOUT (THOUSANDS-UNITS)

(12) COUNTER & READOUT (DECIMALS-LIMIT STORAGE)

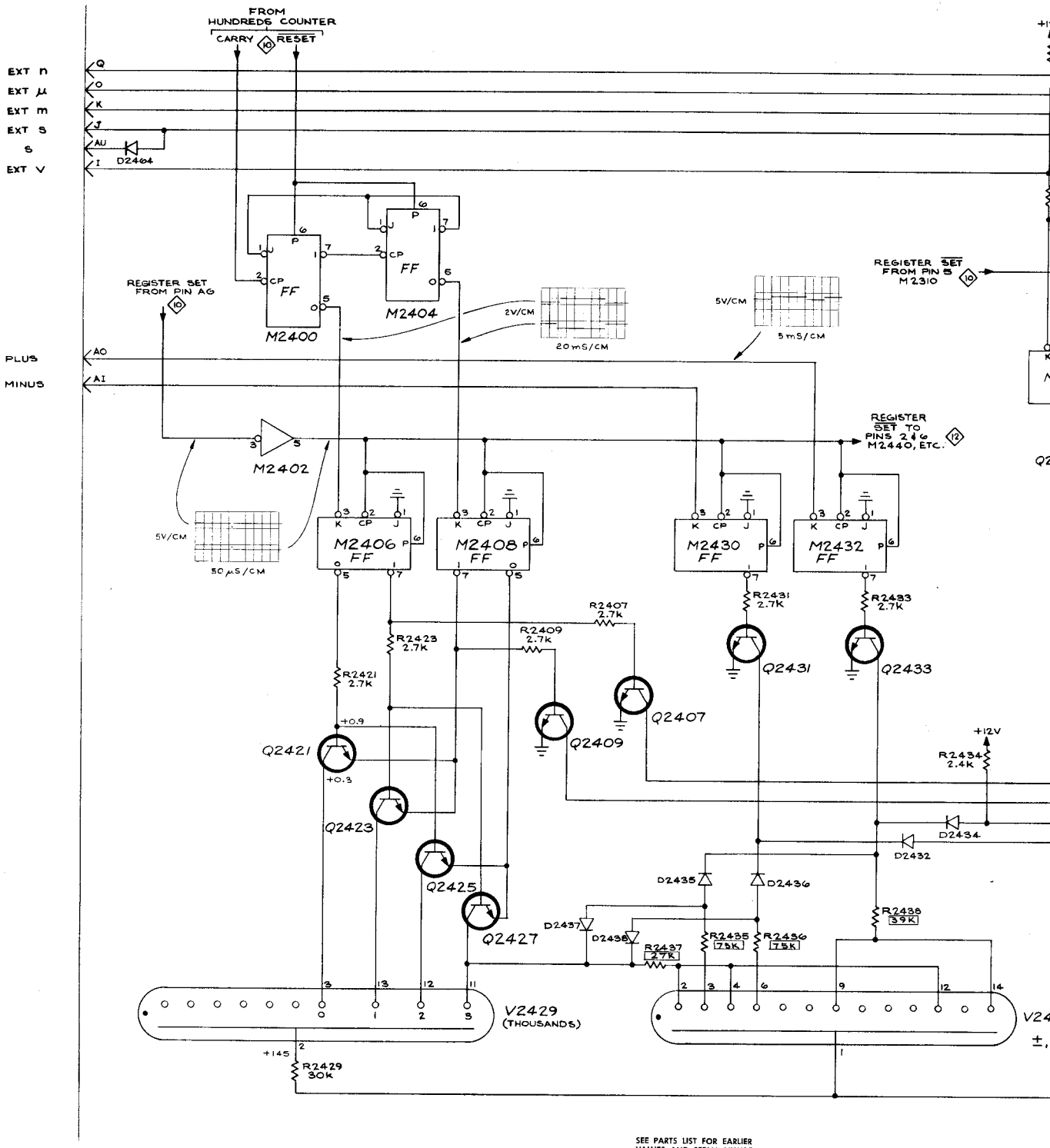
TYPE 230 DIGITAL UNIT

SEE PARTS VALUES A RANGES WITH BLU


RESET TO THOUSANDS COUNTER
M2352
M2354
M2356
M2380
M2382
M2384
M2386
TENS CARRY
CARRY TO THOUSANDS COUNTER
M2358
2V/CM
2mS/CM
M2388
M2370 FF
M2372 FF
M2374 FF
M2376 FF
M2390 FF
M2392 FF
M2394 FF
M2396 FF
M2378
M2398
+3.8V
R2371 2.7k
R2373 2.7k
R2375 2.7k
R2377 2.7k
R2391 2.7k
R2393 2.7k
R2395 2.7k
R2397 2.7k
Q2371
Q2373
Q2375
Q2377
Q2391
Q2393
Q2395
Q2397
V2399 (HUNDREDS)
+145
R2379 30k
R2399 30k
PARTIAL COUNTER BOARD
AD READ 800
AC READ 400
AB READ 200
AA READ 100
Z READ 80
Y READ 40
X READ 20
W READ 10
V READ 8
U READ 4
T READ 2
S READ 1
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
+200V TO THOUSANDS COUNTER
469
COUNTER & READOUT (10)
(ONES - TENS - HUNDREDS)
STORAGE)
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.



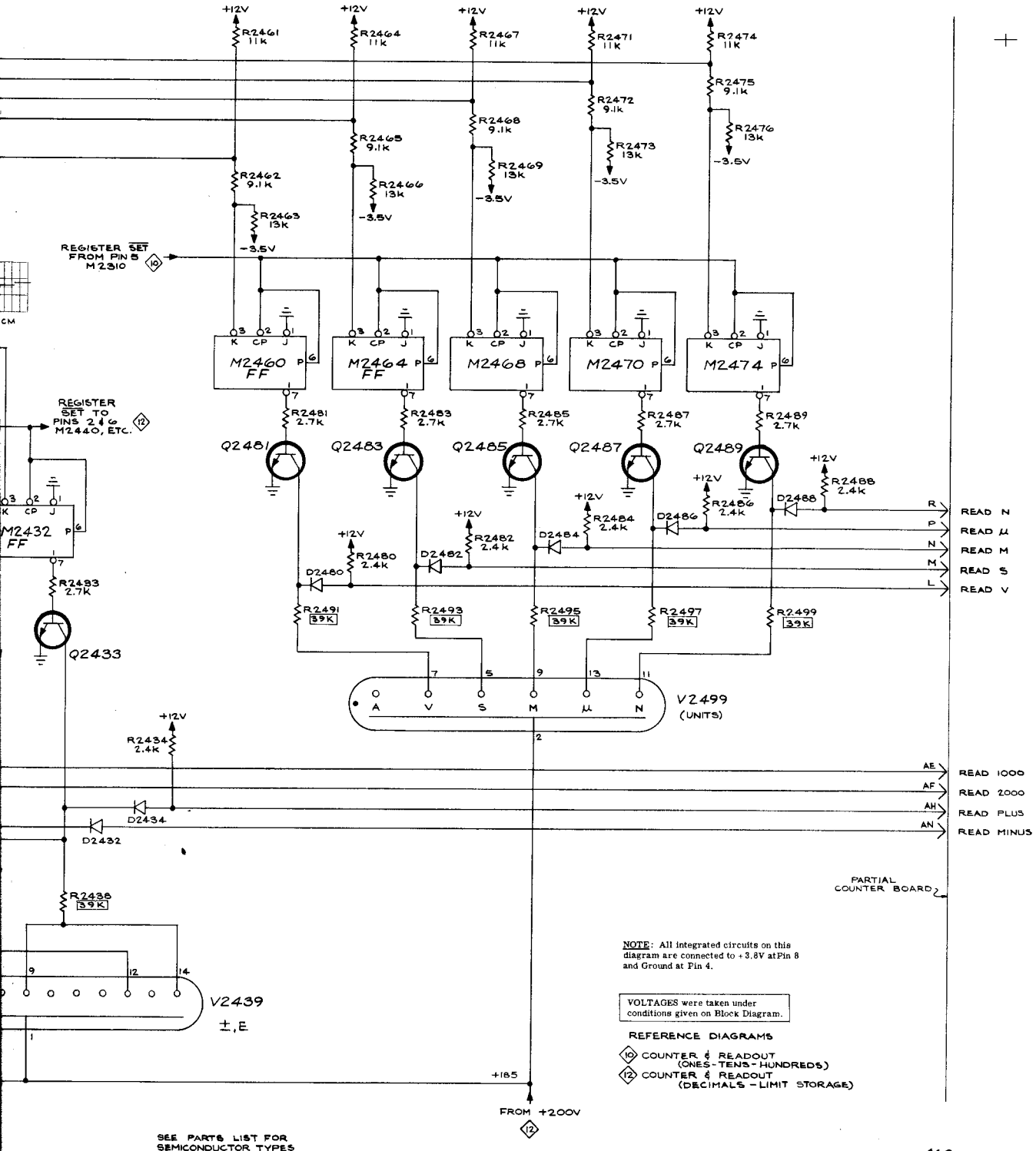
Counter and external program wiring connections located on rear of connector-mounting bulkhead.



SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

SEE PARTS L
SEMICONDUCTO

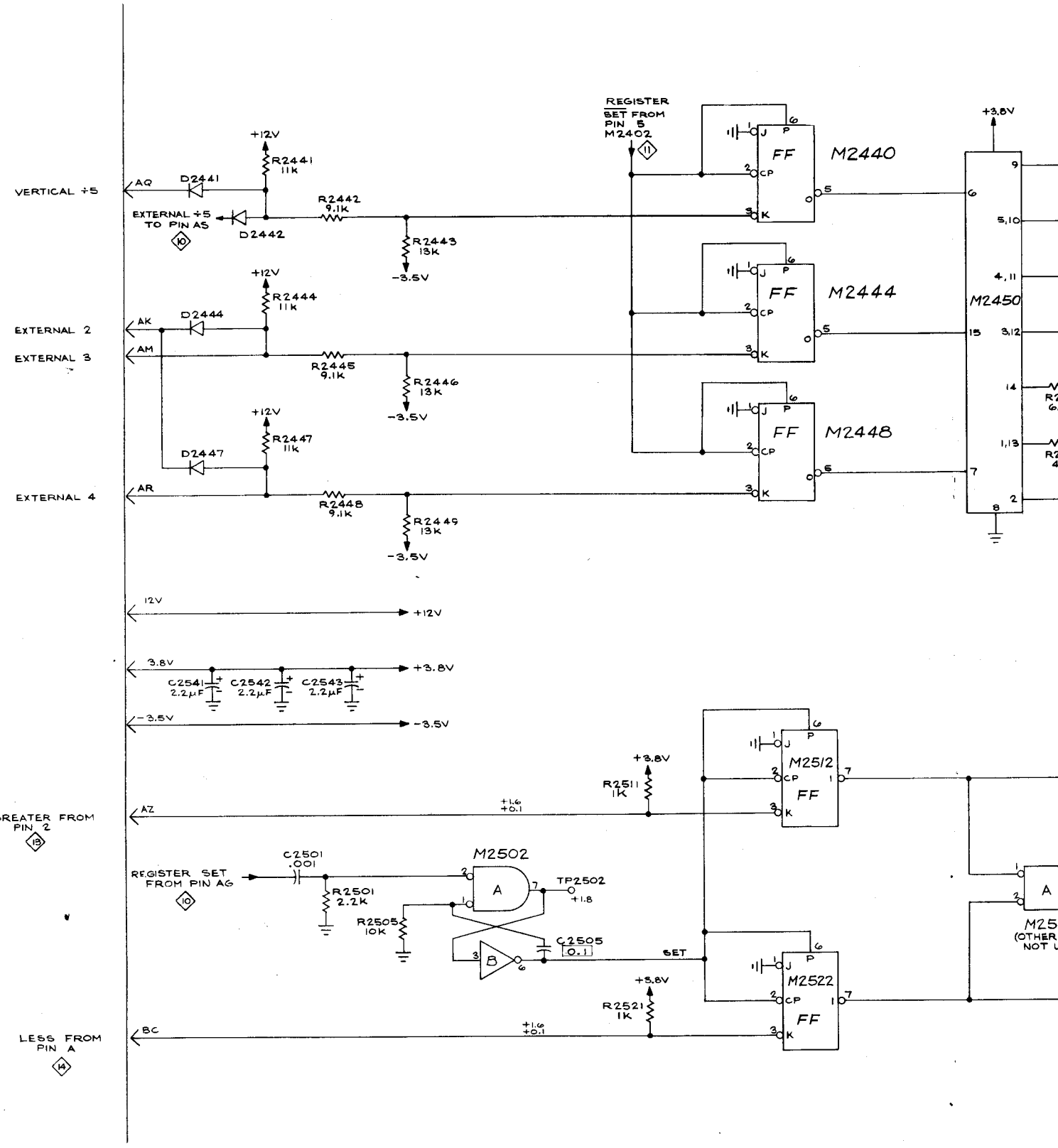
TYPE 230 DIGITAL UNIT

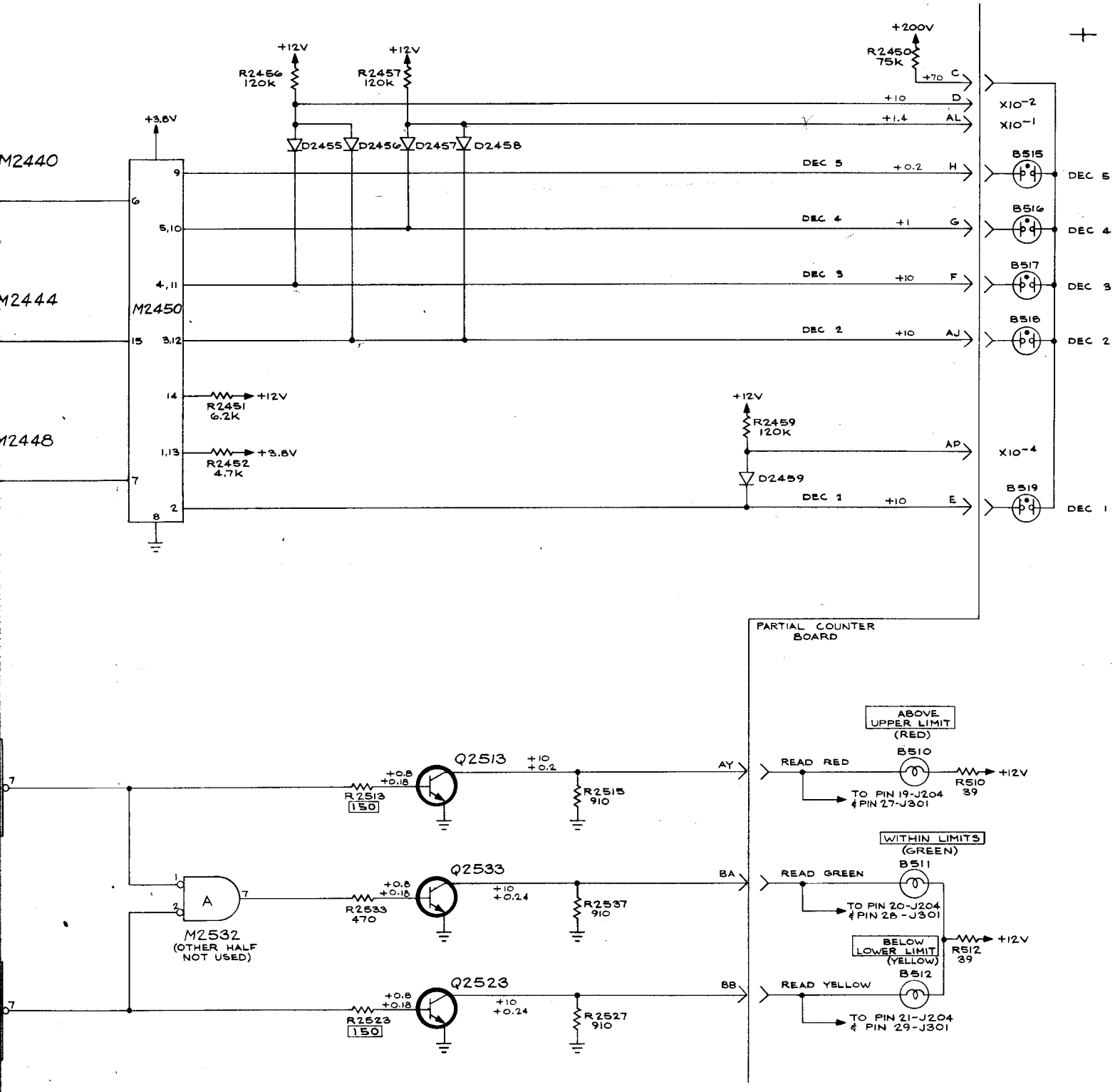


469

COUNTER & READOUT 11

(THOUSANDS - UNITS)


VERTICAL ÷5
EXTERNAL 2
EXTERNAL 3
EXTERNAL 4
GREATER FROM PIN 2
LESS FROM PIN A
REGISTER SET FROM PIN 5 M2402
EXTERNAL ÷5 TO PIN A5
REGISTER SET FROM PIN A6
+12V
-3.5V
+3.8V
R2441 11k
R2442 9.1k
R2443 13k
R2444 11k
R2445 9.1k
R2446 13k
R2447 11k
R2448 9.1k
R2449 13k
D2441
D2442
D2444
D2447
M2440
M2444
M2448
M2450
M2512
M2522
FF
C2541 2.2µF
C2542 2.2µF
C2543 2.2µF
C2501 .001
R2501 2.2k
R2505 10K
C2505 0.1
M2502
TP2502 +1.8
R2511 1K
R2521 1K
+1.6 +0.1
SET



SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS MARKED WITH BLUE OUTLINE.

NOTE: All integrated circuits on this diagram are connected to +3.8V at Pin 8 and Ground at Pin 4 (excluding M2450).

VOLTAGES were taken under conditions given on Block Diagram.

REFERENCE DIAGRAMS

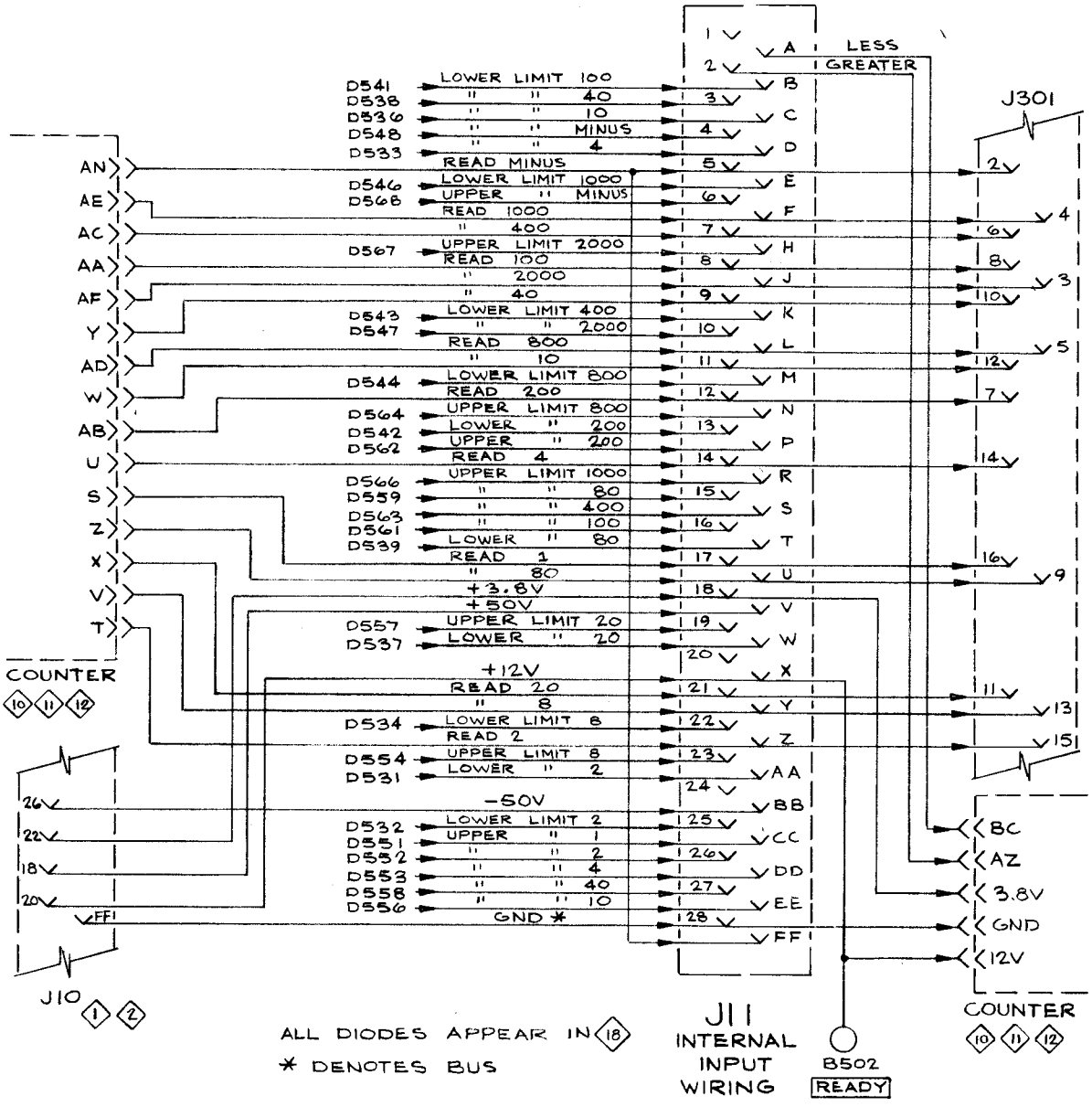
- 10 COUNTER & READOUT (ONES-TENS-HUNDREDS)
- 11 COUNTER & READOUT (THOUSANDS-UNITS)
- 13 UPPER LIMIT
- 14 LOWER LIMIT

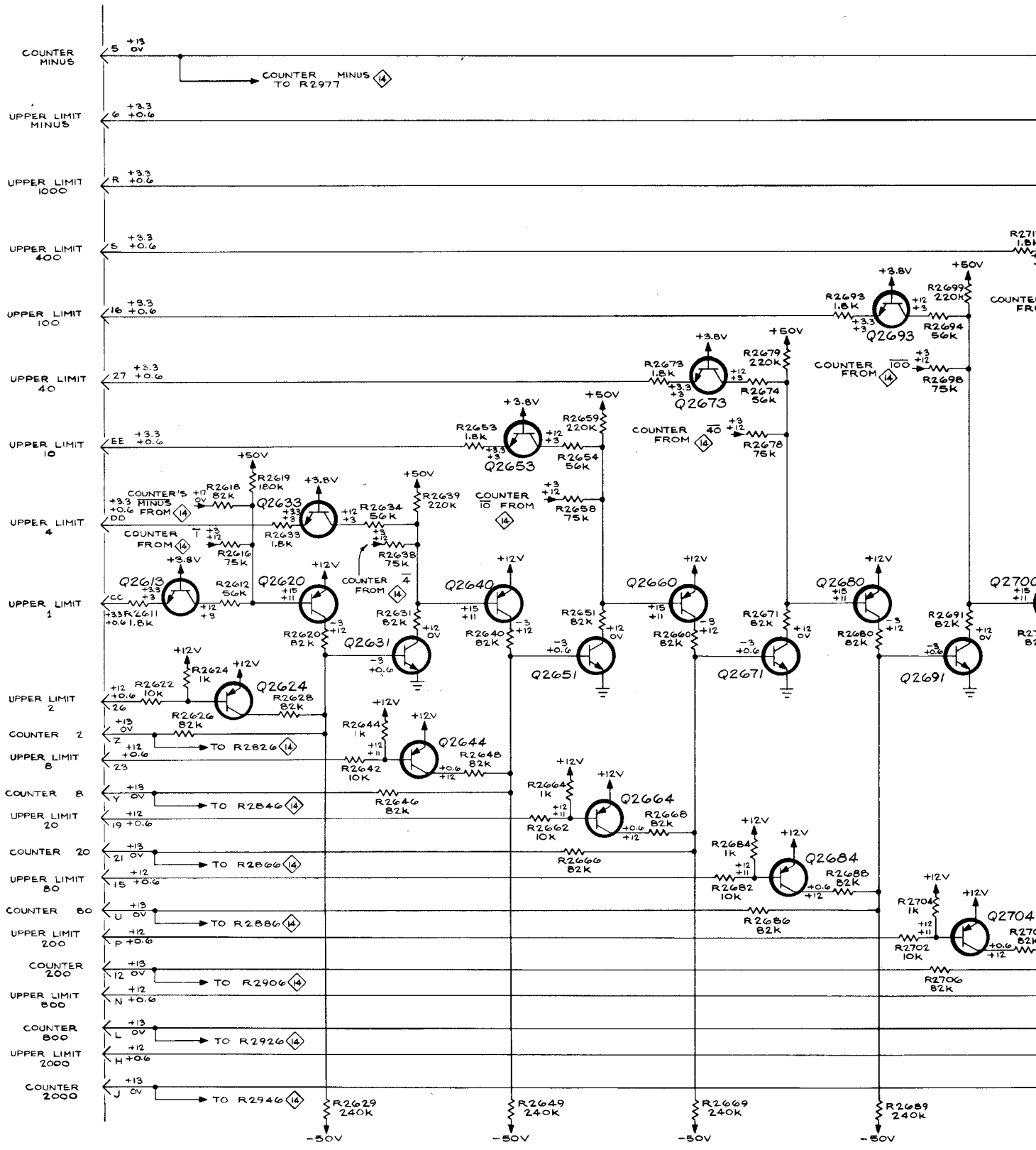
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

1069

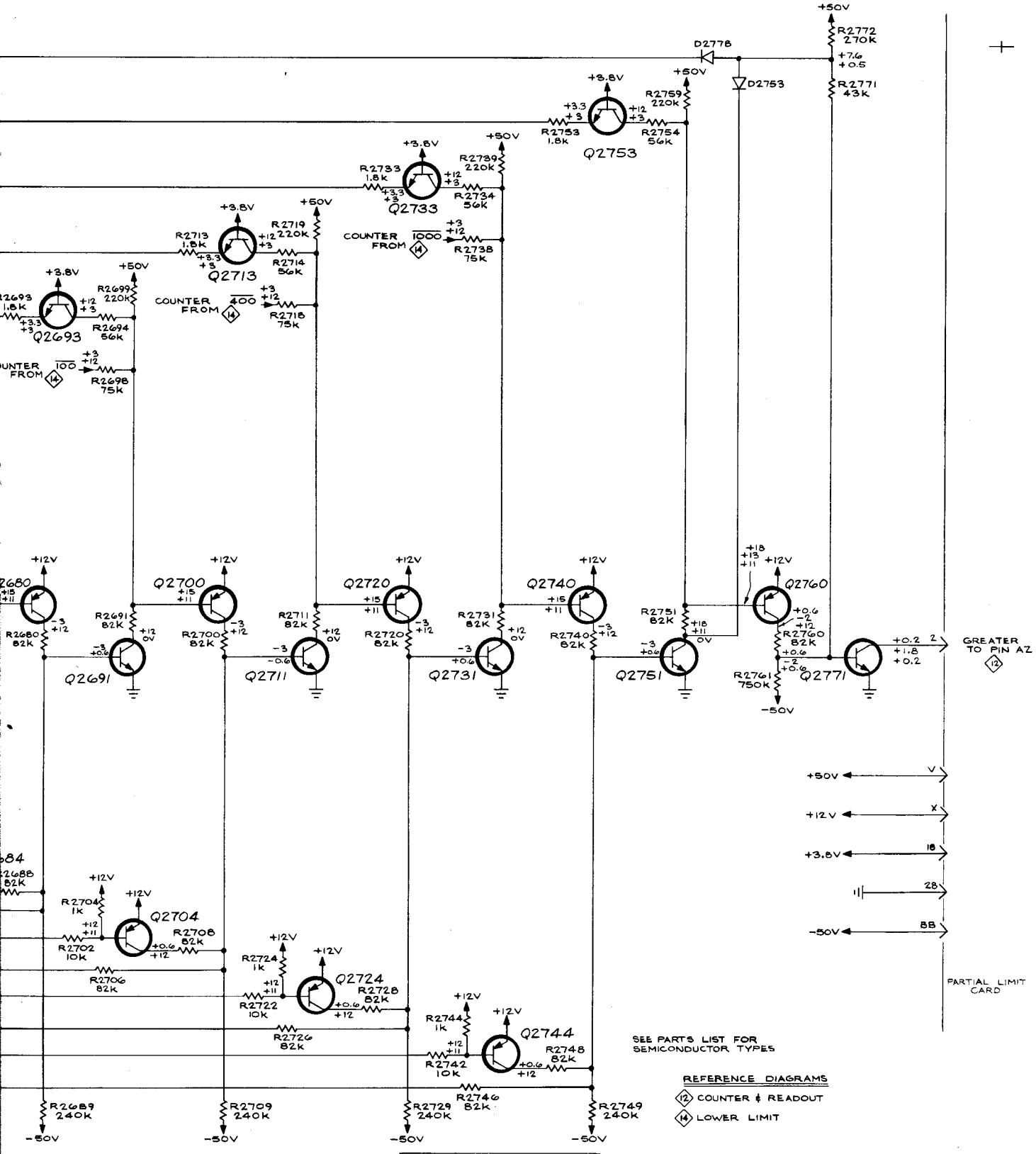
COUNTER & READOUT 12

(DECIMALS - LIMIT STORAGE)


LESS
GREATER
J301
D541 LOWER LIMIT 100
D538 " " 40
D536 " " 10
D548 " " MINUS
D533 " " 4
READ MINUS
D546 LOWER LIMIT 1000
D568 UPPER " MINUS
READ 1000
" 400
D567 UPPER LIMIT 2000
READ 100
" 2000
" 40
D543 LOWER LIMIT 400
D547 " " 2000
READ 800
" 10
D544 LOWER LIMIT 800
READ 200
D564 UPPER LIMIT 800
D542 LOWER " 200
D562 UPPER " 200
READ 4
D566 UPPER LIMIT 1000
D559 " " 80
D563 " " 400
D561 " " 100
D539 LOWER " 80
READ 1
" 80
+3.8V
+50V
D557 UPPER LIMIT 20
D537 LOWER " 20
+12V
READ 20
" 8
D534 LOWER LIMIT 8
READ 2
D554 UPPER LIMIT 8
D531 LOWER " 2
-50V
D532 LOWER LIMIT 2
D551 UPPER " 1
D552 " " 2
D553 " " 4
D558 " " 40
D556 " " 10
GND *
AN
AE
AC
AA
AF
Y
AD
W
AB
U
S
Z
X
V
T
FF
COUNTER
10 11 12
26
22
18
20
FF
J10
1 2
A B C D E F H J K L M N P R S T U V W X Y Z AA BB CC DD EE FF
J11
INTERNAL
INPUT
WIRING
BC
AZ
3.8V
GND
12V
COUNTER
10 11 12
B502
READY
ALL DIODES APPEAR IN 18
* DENOTES BUS



TYPE 230 DIGITAL UNIT

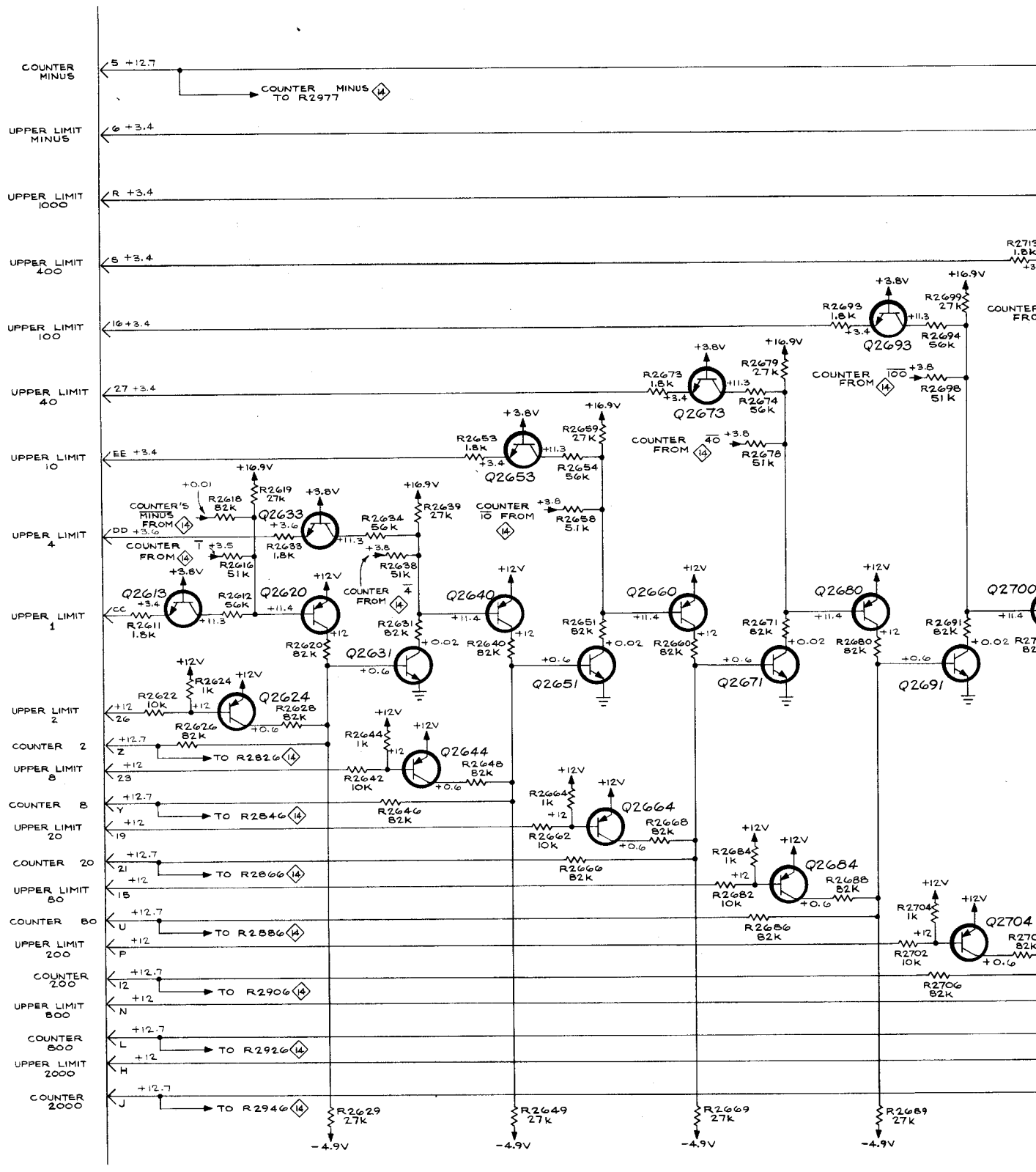


VOLTAGES were taken under conditions given on Block Diagram with the following additions:
Type 230 READOUT.....+0001
Type 230 UPPER LIMIT LEVEL.....
+0000 (upper reading)
-0001 (lower reading)

269

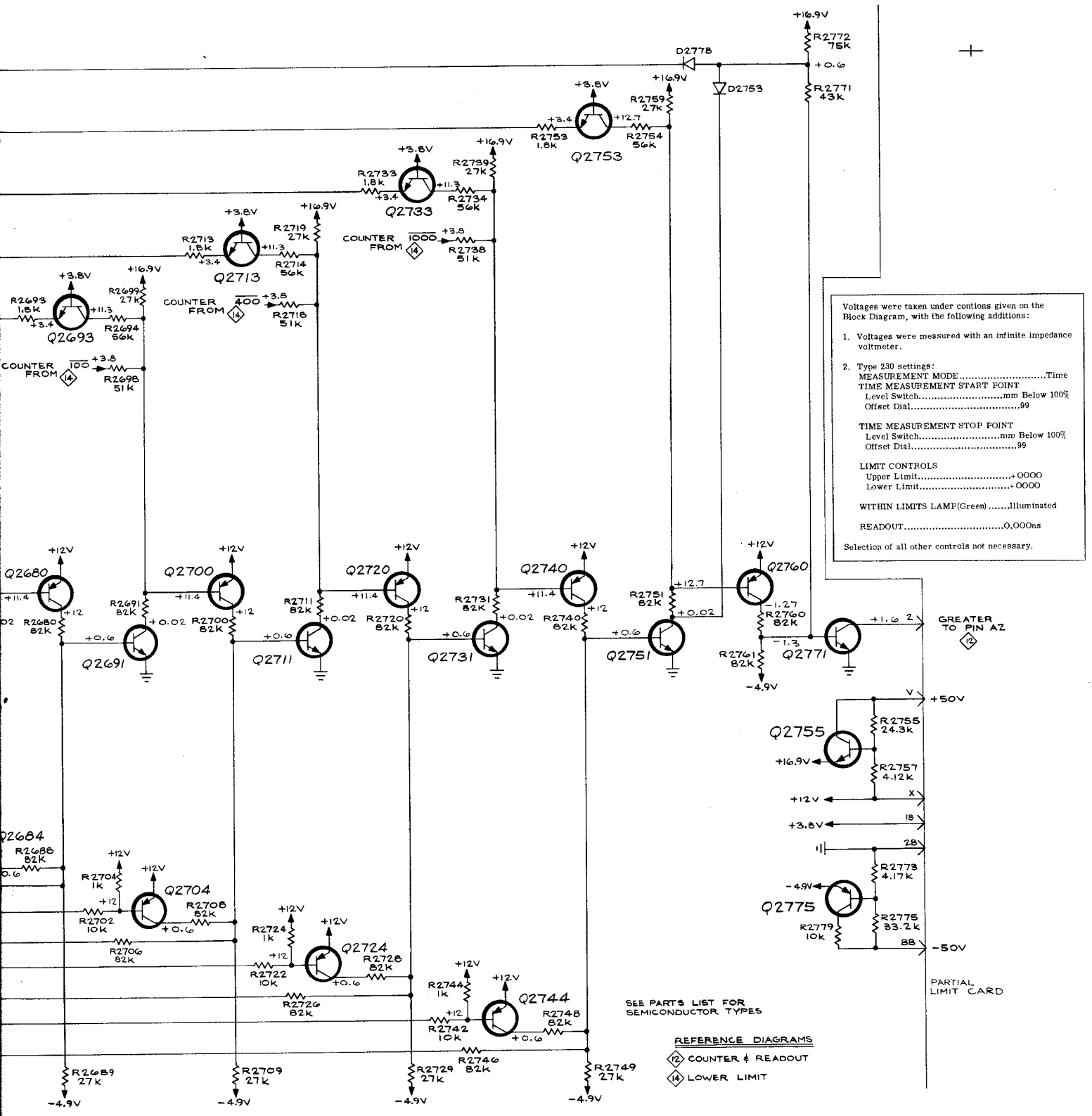
P11 — UPPER LIMIT (13)

(SERIES H, MODEL 1)



TYPE 230 DIGITAL UNIT

A



Voltages were taken under contions given on the Block Diagram, with the following additions:

1. Voltages were measured with an infinite impedance voltmeter.

2. Type 230 settings:
   MEASUREMENT MODE.....Time
   TIME MEASUREMENT START POINT
   Level Switch.....mm Below 100%
   Offset Dial.....99

   TIME MEASUREMENT STOP POINT
   Level Switch.....mm Below 100%
   Offset Dial.....99

   LIMIT CONTROLS
   Upper Limit.....+0000
   Lower Limit.....+0000

   WITHIN LIMITS LAMP(Green).....Illuminated

   READOUT.....0.000ns

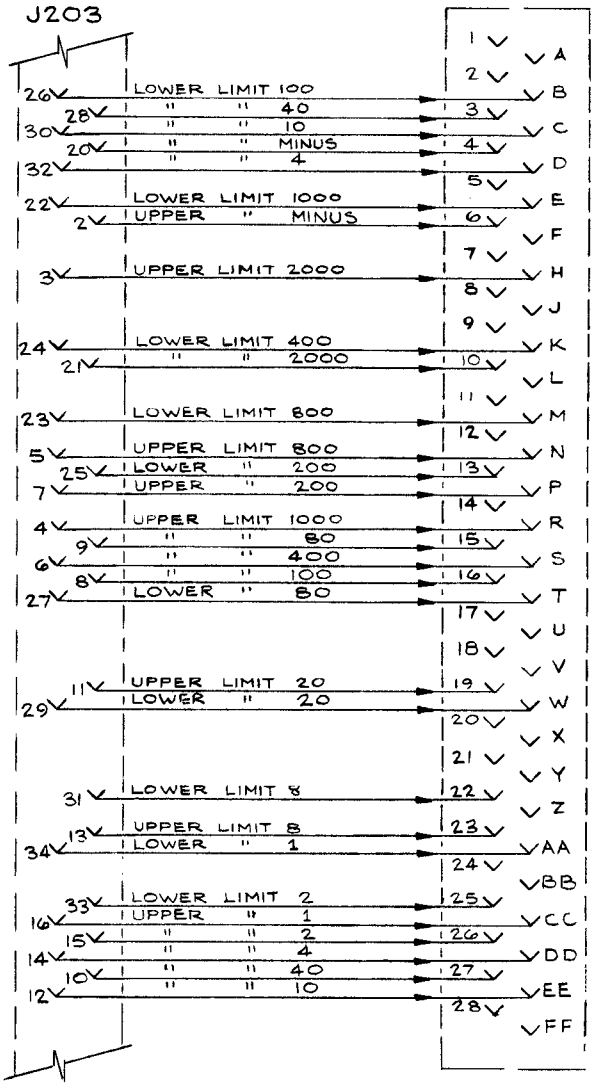
Selection of all other controls not necessary.

269

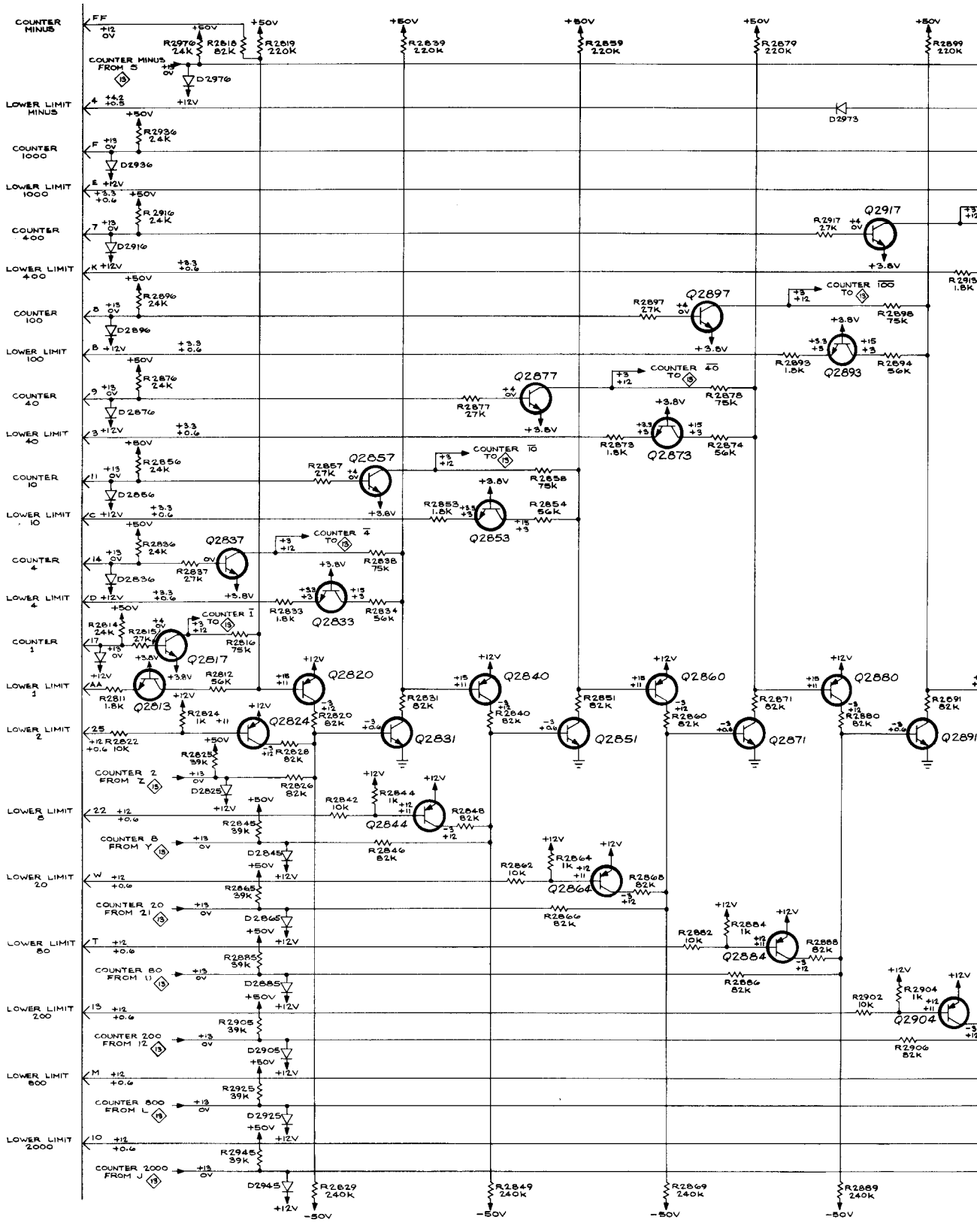
P11 – UPPER LIMIT 13

(SERIES H, MODEL 2-UP)

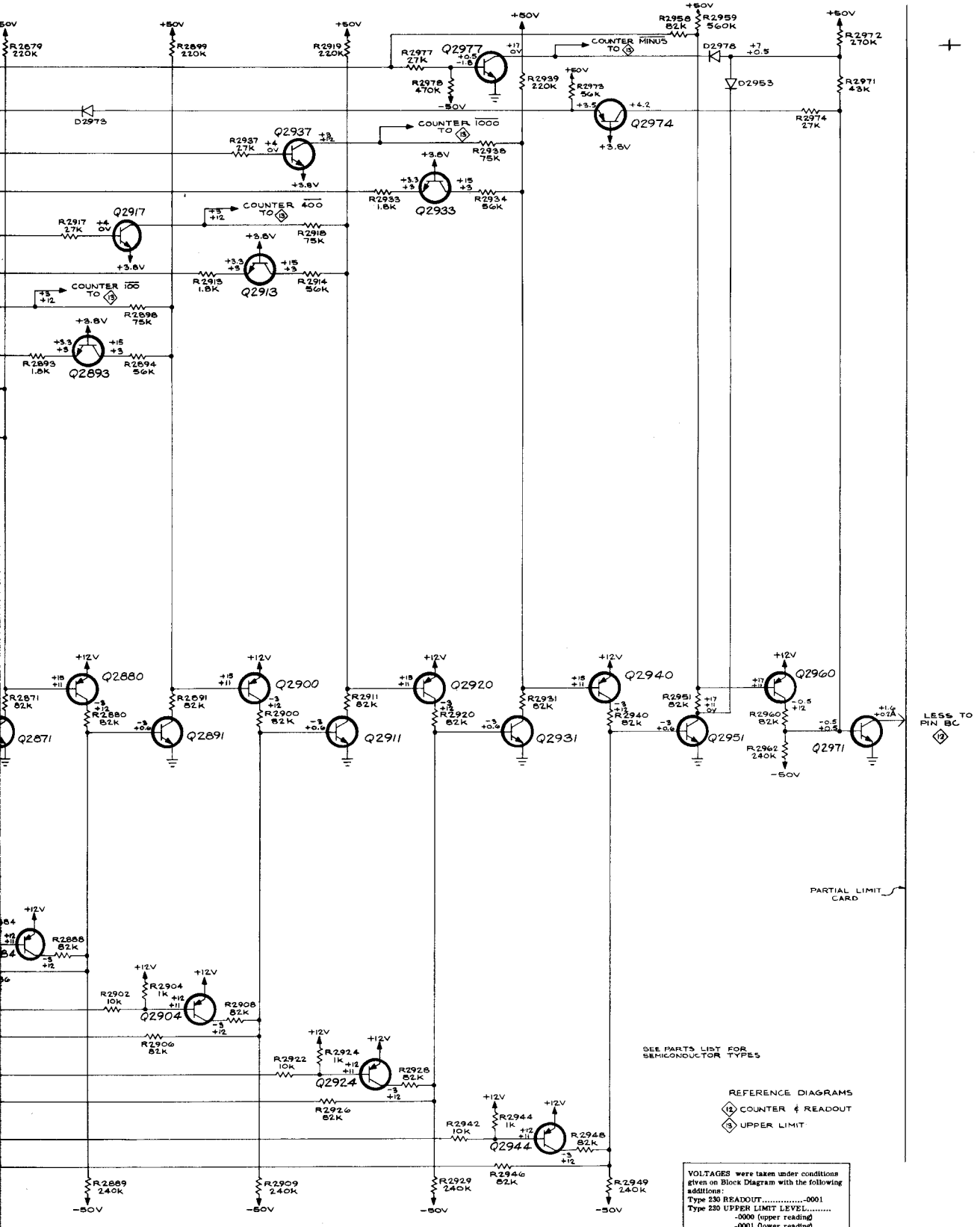
A



EXTERNAL INPUT WIRING



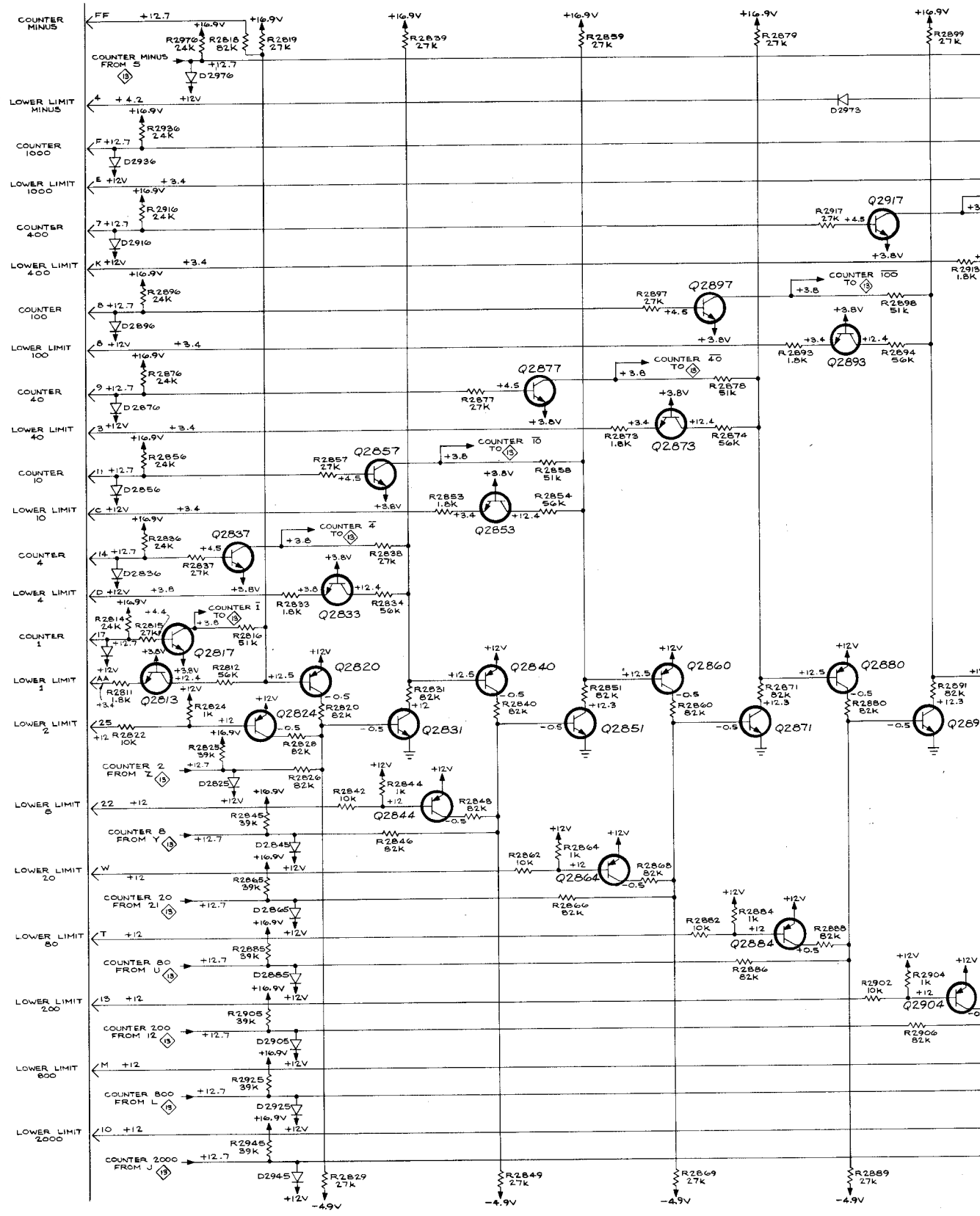
TYPE 230 DIGITAL UNIT



VOLTAGES were taken under conditions given on Block Diagram with the following additions:
Type 230 READOUT.....-0001
Type 230 UPPER LIMIT LEVEL.....
-0000 (upper reading)
-0001 (lower reading)

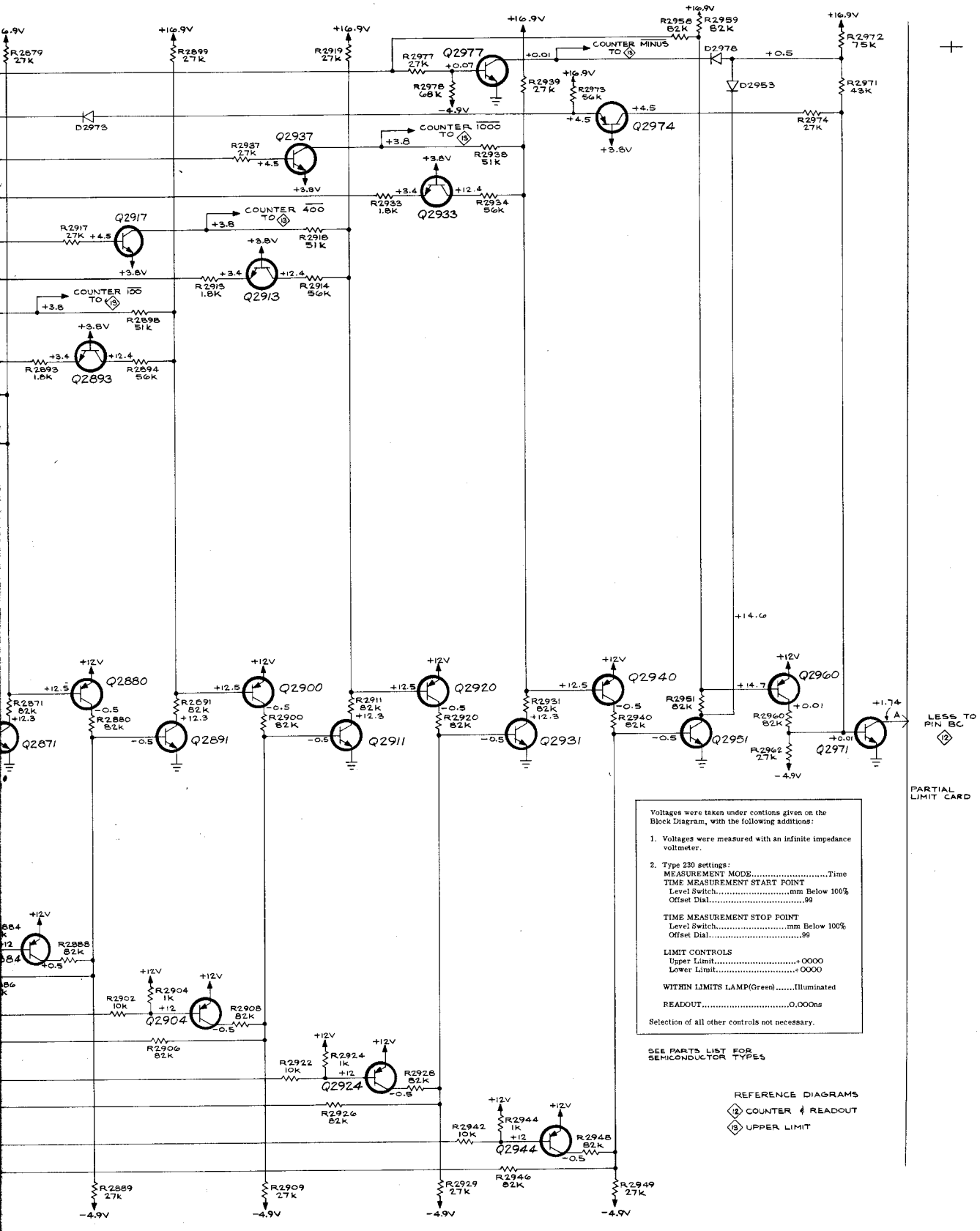
P11 - LOWER LIMIT 14

(SERIES H, MODEL 1)



TYPE 230 DIGITAL UNIT

A



Voltages were taken under contions given on the Block Diagram, with the following additions:

1. Voltages were measured with an infinite impedance voltmeter.
2. Type 230 settings:
   - MEASUREMENT MODE.....Time
   - TIME MEASUREMENT START POINT
     - Level Switch.....mm Below 100%
     - Offset Dial.....99
   - TIME MEASUREMENT STOP POINT
     - Level Switch.....mm Below 100%
     - Offset Dial.....99
   - LIMIT CONTROLS
     - Upper Limit.....+0000
     - Lower Limit.....+0000
   - WITHIN LIMITS LAMP(Green).....Illuminated
   - READOUT.....0.000ns

Selection of all other controls not necessary.

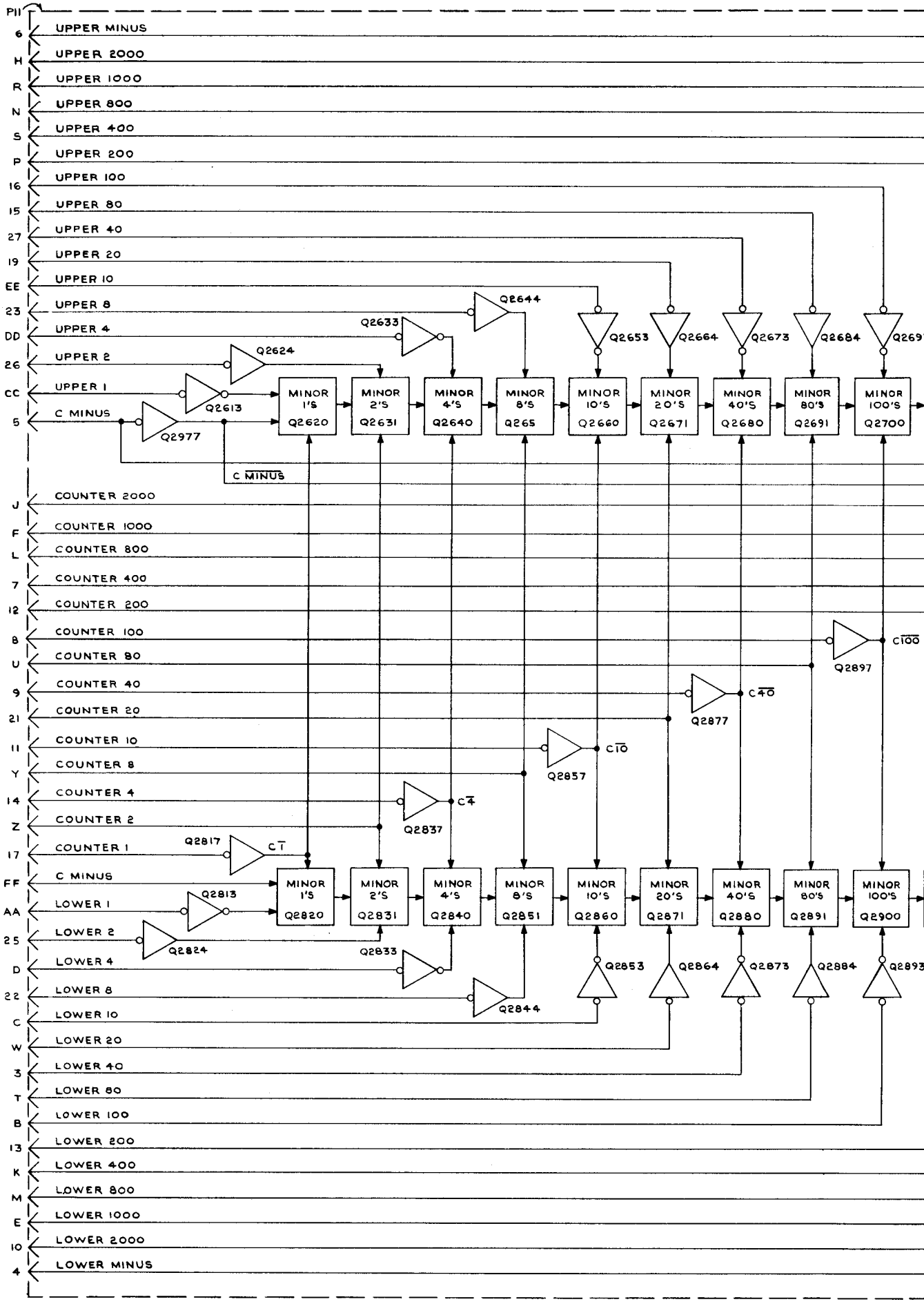
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

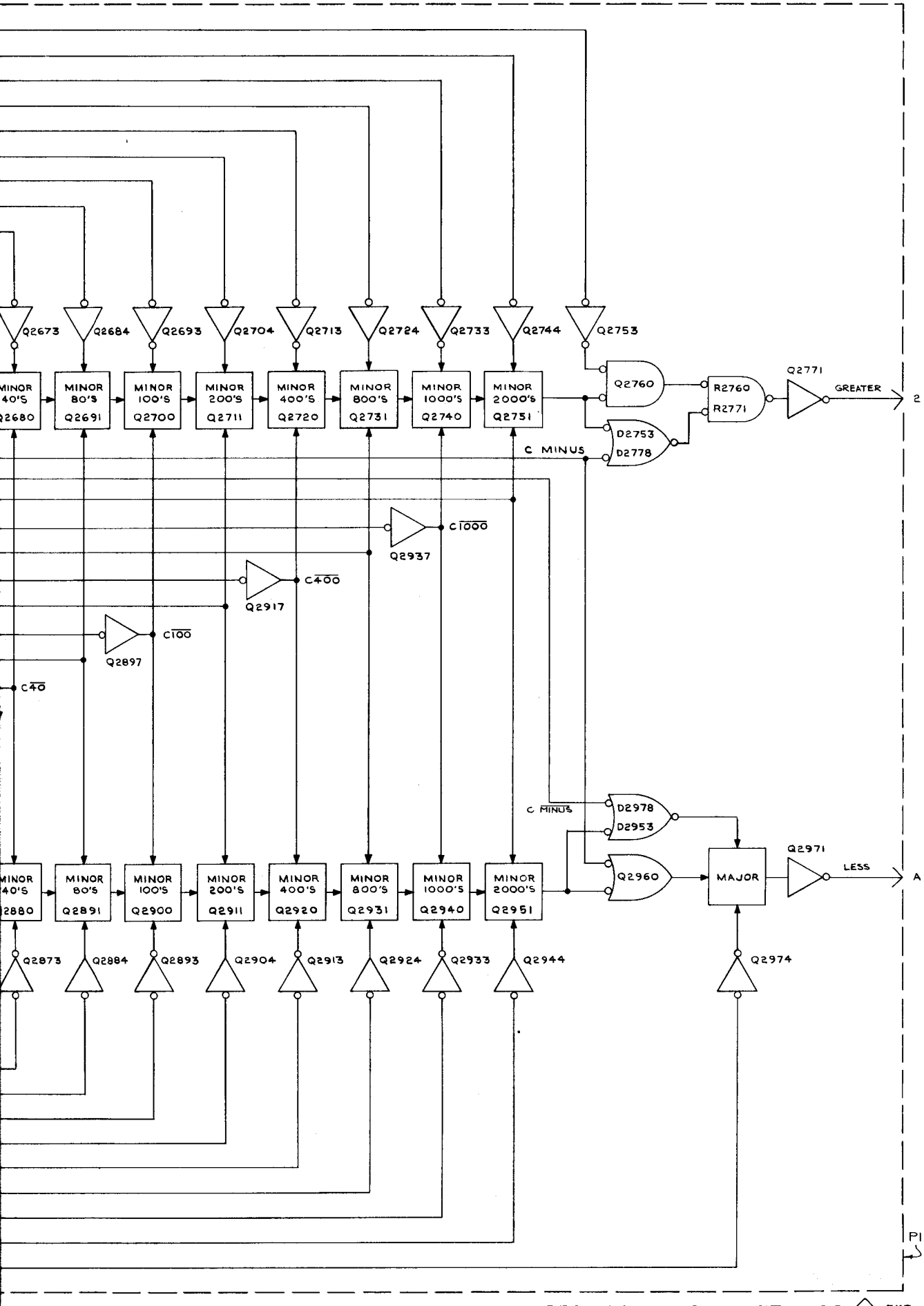
REFERENCE DIAGRAMS
- 12 COUNTER & READOUT
- 13 UPPER LIMIT

P11 - LOWER LIMIT 14

(SERIES H, MODEL 2-UP)

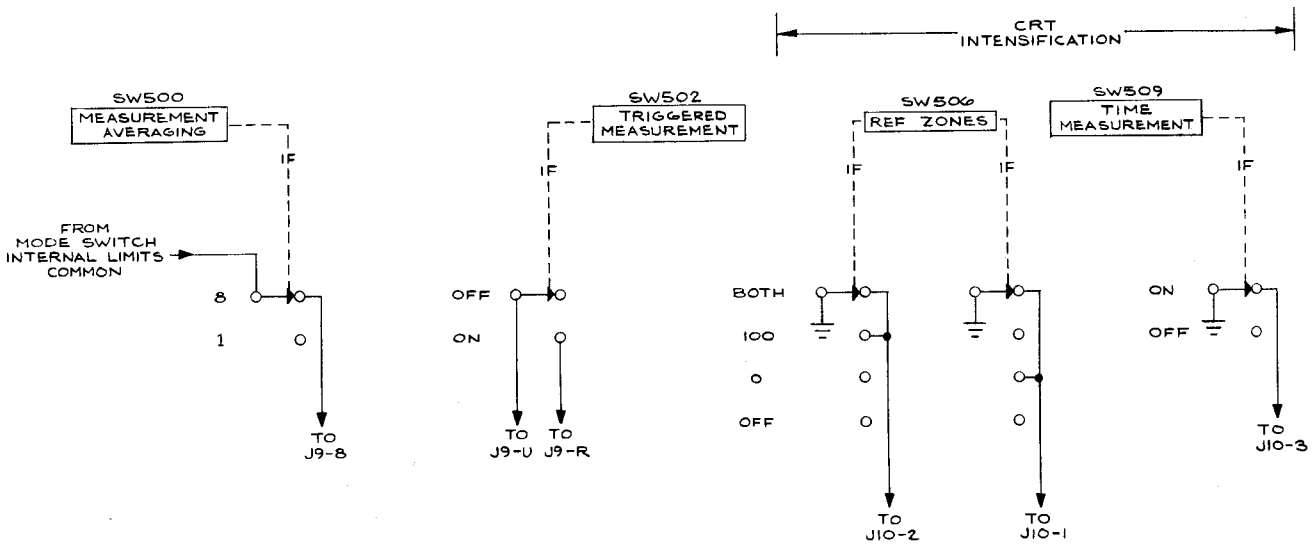
A

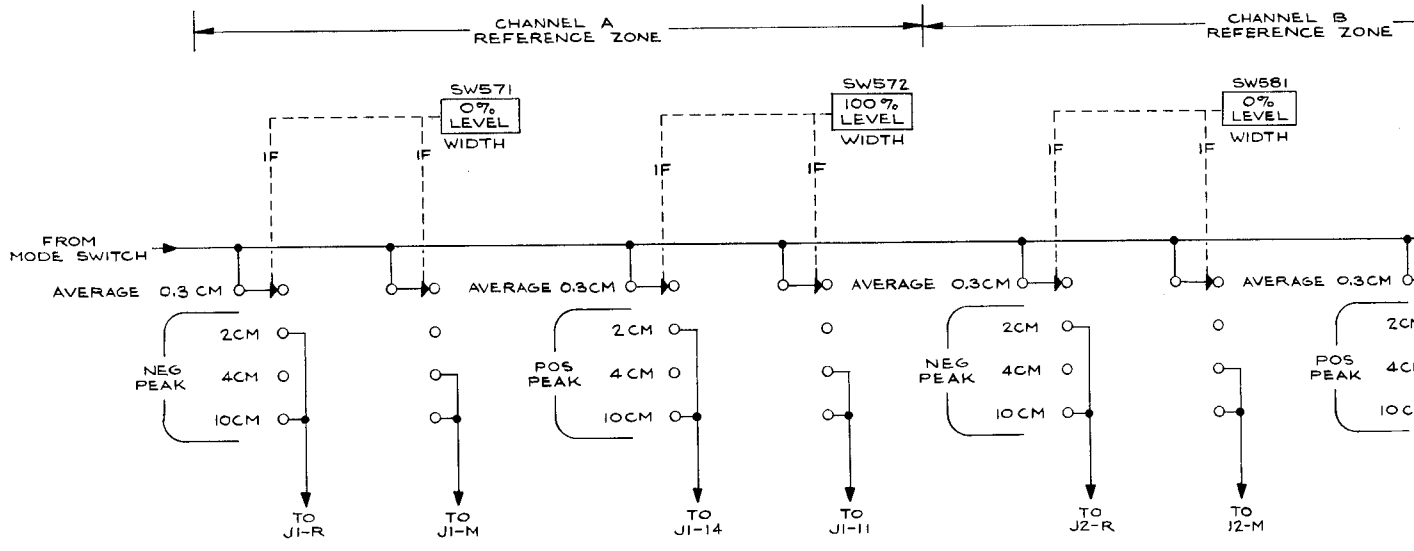

P11
6 UPPER MINUS
H UPPER 2000
R UPPER 1000
N UPPER 800
S UPPER 400
P UPPER 200
16 UPPER 100
15 UPPER 80
27 UPPER 40
19 UPPER 20
EE UPPER 10
23 UPPER 8
DD UPPER 4
26 UPPER 2
CC UPPER 1
5 C MINUS
J COUNTER 2000
F COUNTER 1000
L COUNTER 800
7 COUNTER 400
12 COUNTER 200
8 COUNTER 100
U COUNTER 80
9 COUNTER 40
21 COUNTER 20
11 COUNTER 10
Y COUNTER 8
14 COUNTER 4
Z COUNTER 2
17 COUNTER 1
FF C MINUS
AA LOWER 1
25 LOWER 2
D LOWER 4
22 LOWER 8
C LOWER 10
W LOWER 20
3 LOWER 40
T LOWER 80
B LOWER 100
13 LOWER 200
K LOWER 400
M LOWER 800
E LOWER 1000
10 LOWER 2000
4 LOWER MINUS
Q2644
Q2633
Q2624
Q2613
Q2977
C MINUS
Q2653
Q2664
Q2673
Q2684
MINOR 1'S Q2620
MINOR 2'S Q2631
MINOR 4'S Q2640
MINOR 8'S Q265
MINOR 10'S Q2660
MINOR 20'S Q2671
MINOR 40'S Q2680
MINOR 80'S Q2691
MINOR 100'S Q2700
Q2897
Q2877
Q2857
Q2837
Q2817
Q2813
Q2824
Q2833
Q2844
Q2853
Q2864
Q2873
Q2884
MINOR 1'S Q2820
MINOR 2'S Q2831
MINOR 4'S Q2840
MINOR 8'S Q2851
MINOR 10'S Q2860
MINOR 20'S Q2871
MINOR 40'S Q2880
MINOR 80'S Q2891
MINOR 100'S Q2900

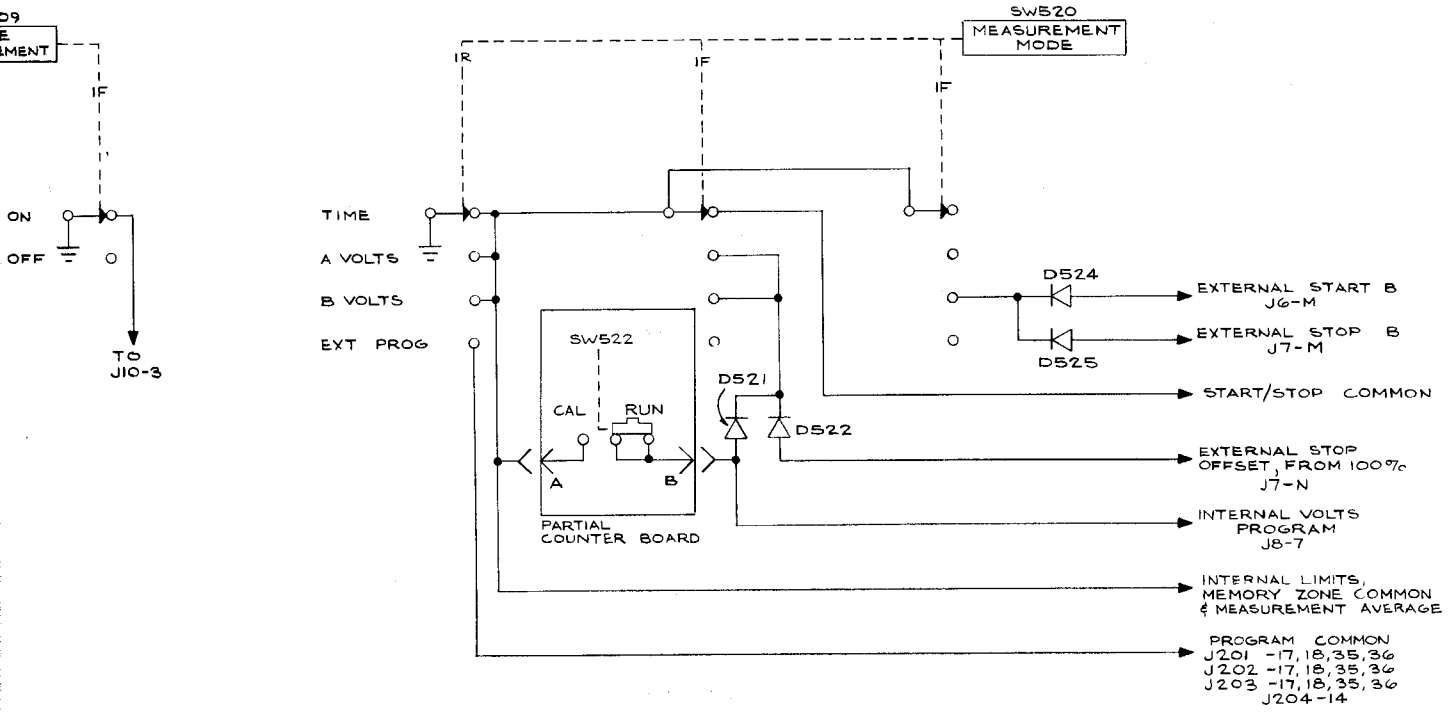


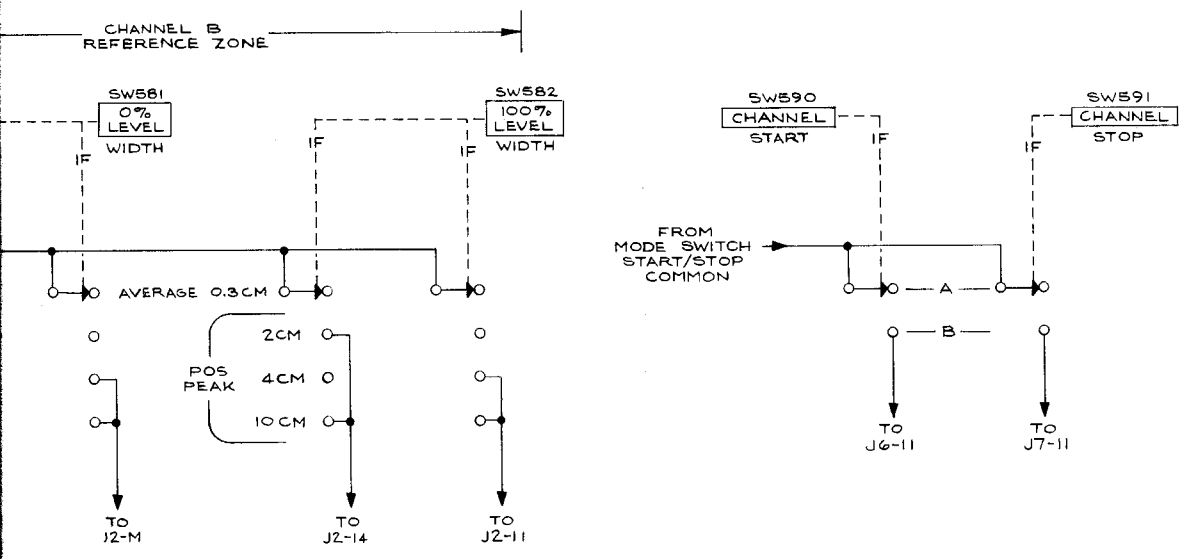
P11 UPPER AND LOWER LIMIT CARD 15 EKP 667

A1

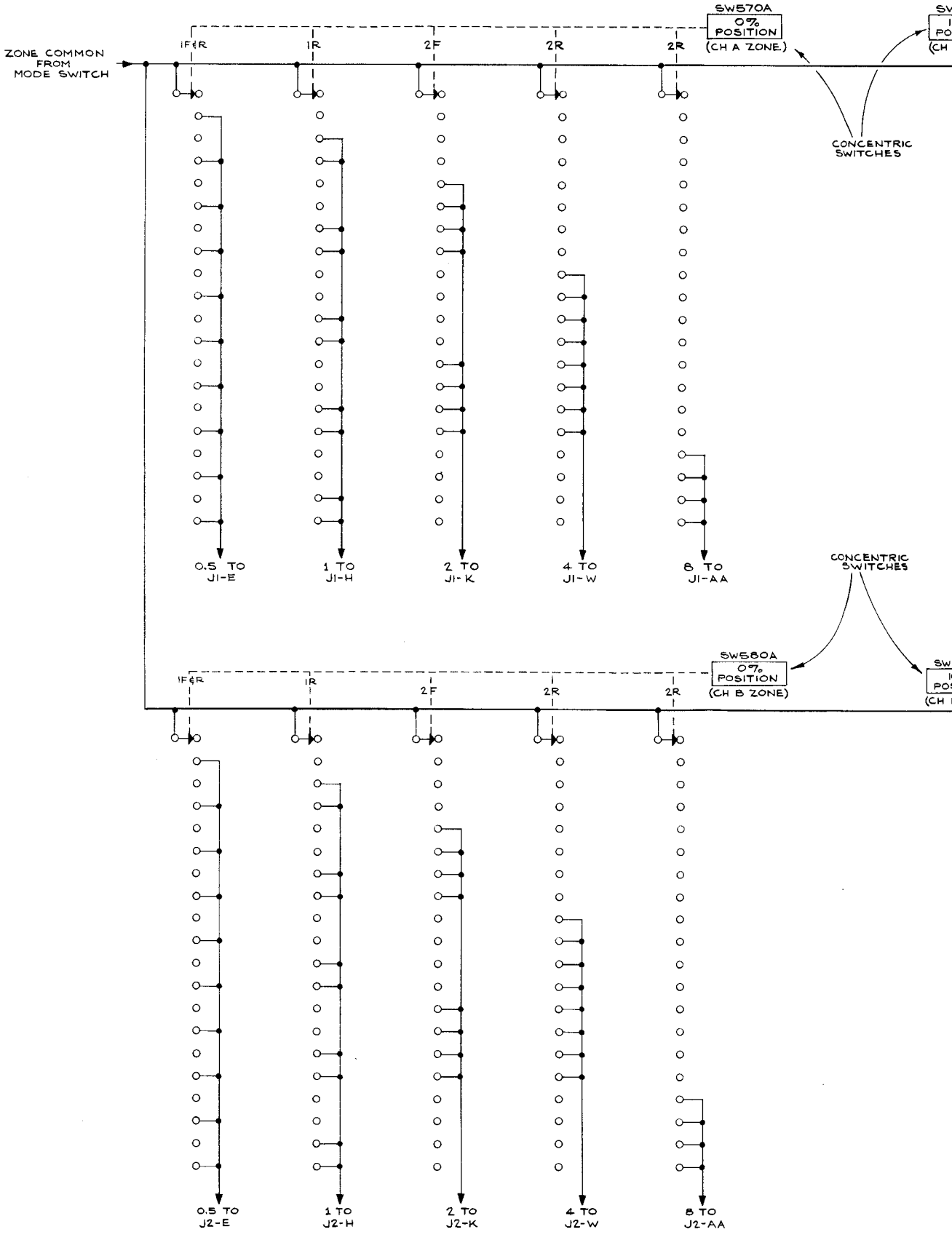

CRT
INTENSIFICATION
SW500
MEASUREMENT
AVERAGING
IF
FROM
MODE SWITCH
INTERNAL LIMITS
COMMON
8
1
0
TO
J9-8
SW502
TRIGGERED
MEASUREMENT
IF
OFF
ON
TO
J9-U
TO
J9-R
SW506
REF ZONES
IF
IF
BOTH
100
0
OFF
TO
J10-2
TO
J10-1
SW509
TIME
MEASUREMENT
IF
ON
OFF
TO
J10-3

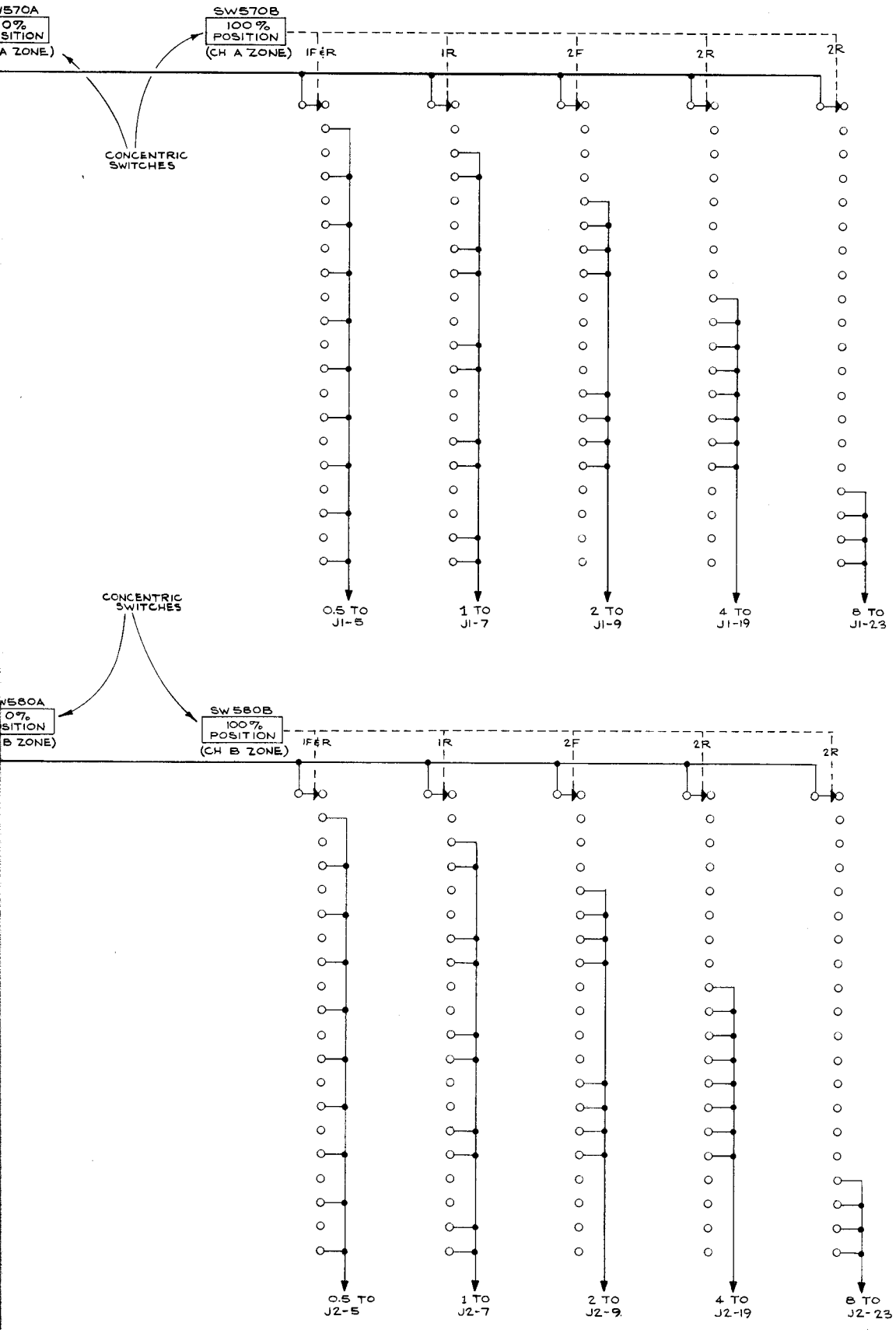

CHANNEL A
REFERENCE ZONE
CHANNEL B
REFERENCE ZONE
SW571
0%
LEVEL
WIDTH
SW572
100%
LEVEL
WIDTH
SW581
0%
LEVEL
WIDTH
IF
FROM
MODE SWITCH
AVERAGE 0.3 CM
AVERAGE 0.3CM
AVERAGE 0.3CM
AVERAGE 0.3CM
NEG
PEAK
POS
PEAK
2CM
4CM
10CM
TO
J1-R
TO
J1-M
TO
J1-14
TO
J1-11
TO
J2-R
TO
J2-M





SEE PARTS LIST FOR SEMICONDUCTOR TYPES


ZONE COMMON FROM MODE SWITCH
1F&R
1R
2F
2R
2R
SW570A
0% POSITION
(CH A ZONE)
CONCENTRIC SWITCHES
0.5 TO J1-E
1 TO J1-H
2 TO J1-K
4 TO J1-W
8 TO J1-AA
CONCENTRIC SWITCHES
SW580A
0% POSITION
(CH B ZONE)
1F&R
1R
2F
2R
2R
0.5 TO J2-E
1 TO J2-H
2 TO J2-K
4 TO J2-W
8 TO J2-AA

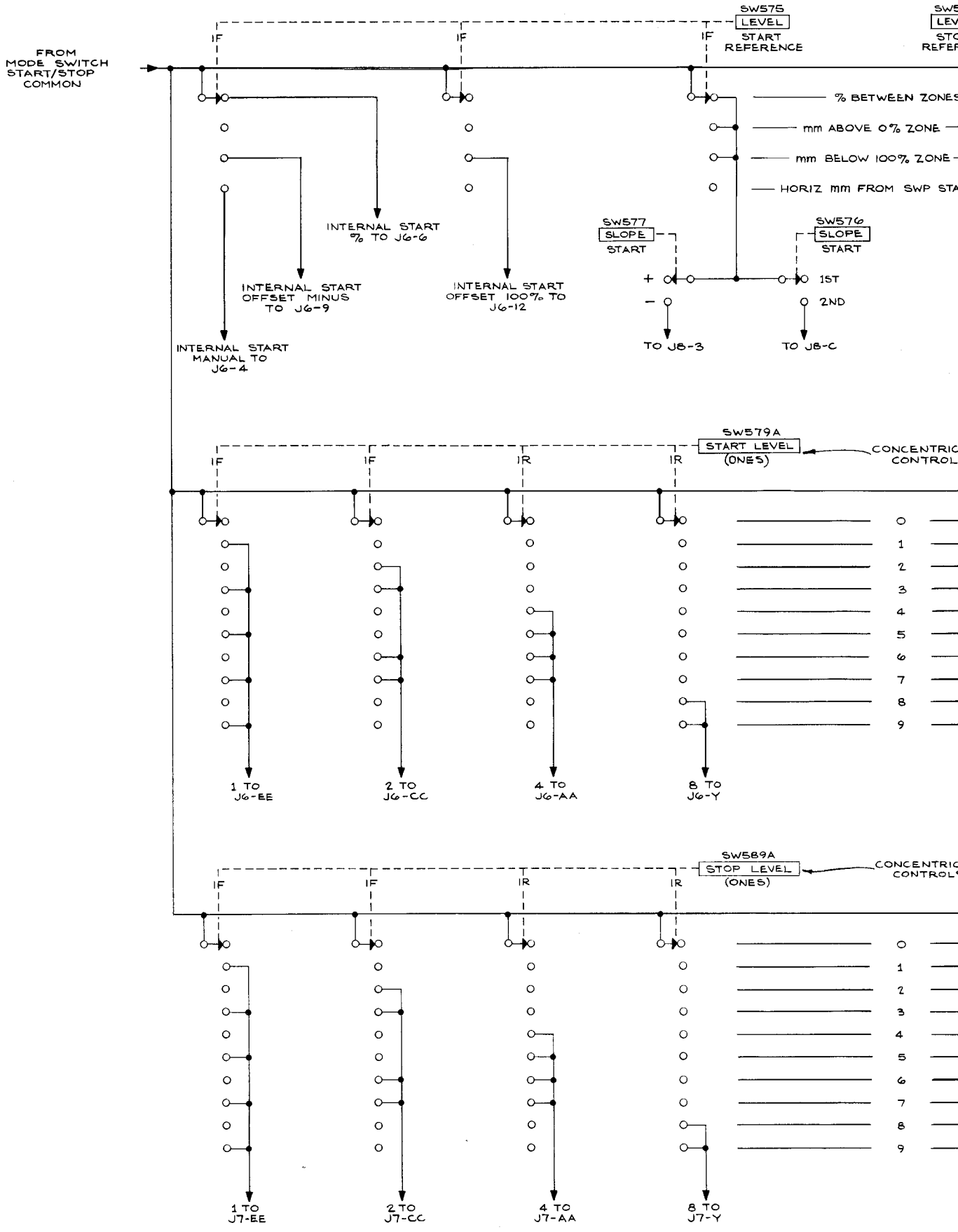


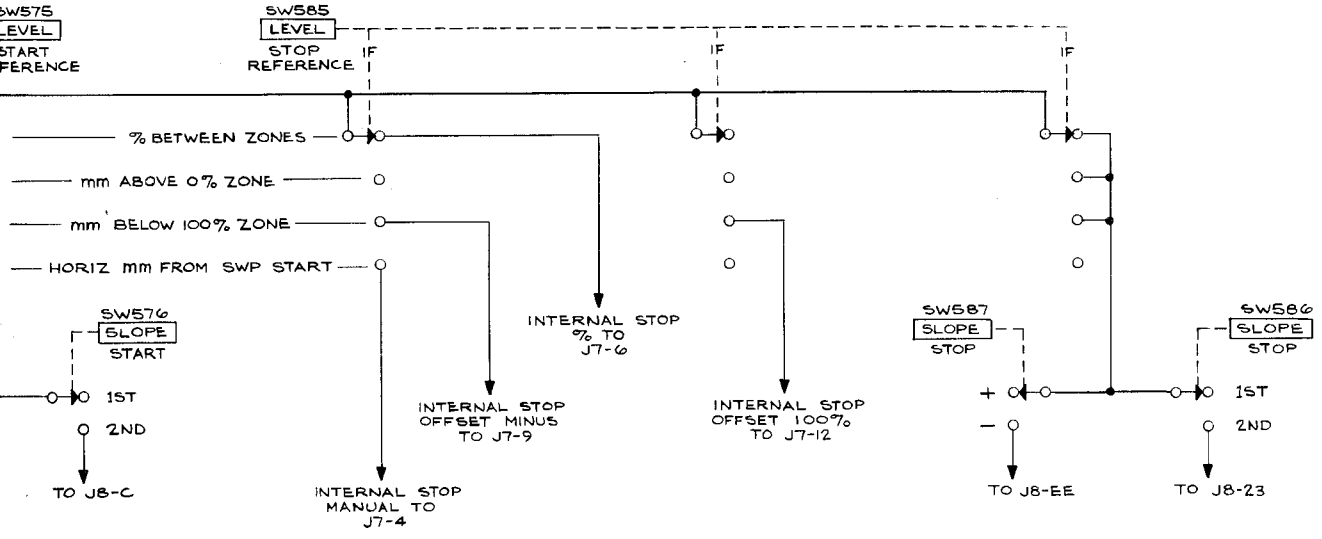
667

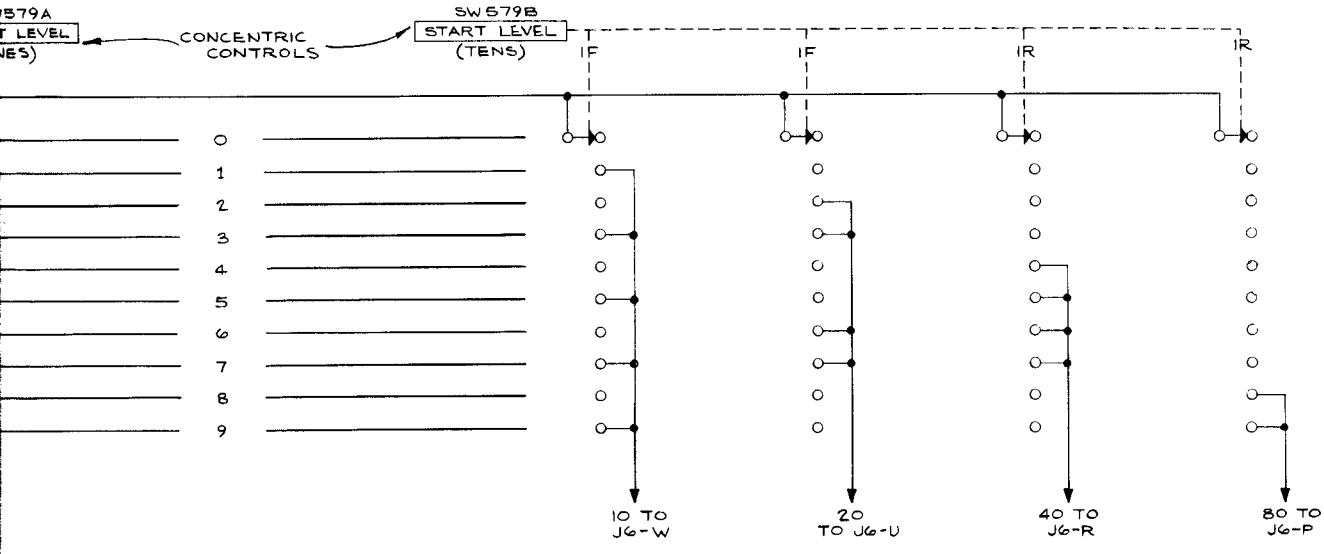
REFERENCE
ZONE POSITION SWITCHES (17)

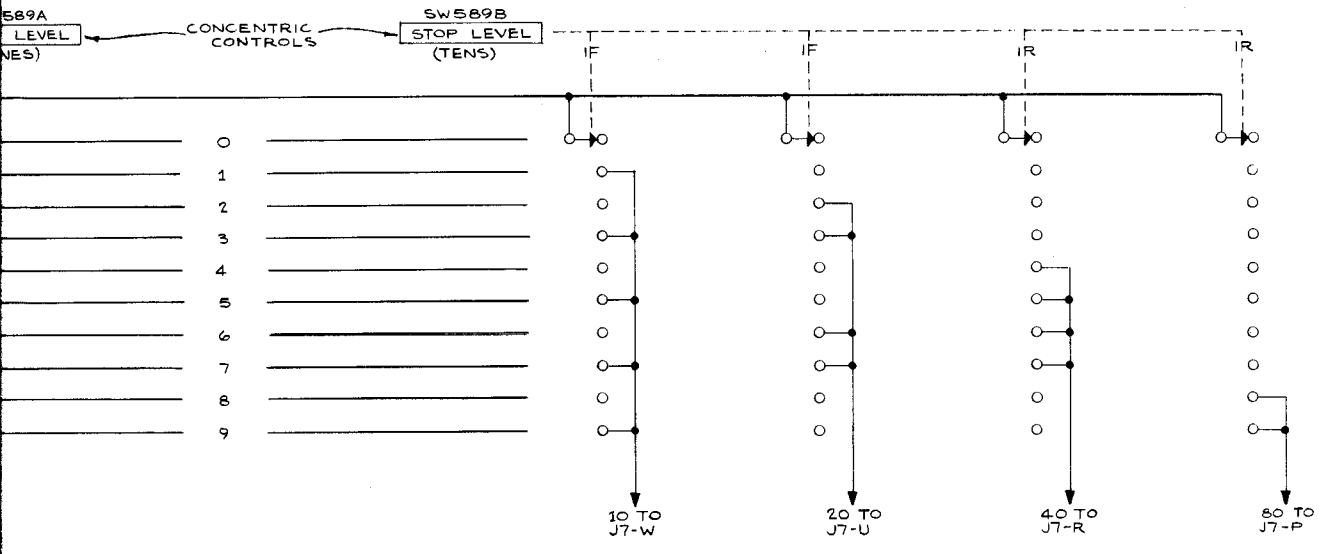
A2

SWITCHES


FROM MODE SWITCH START/STOP COMMON
SW575
LEVEL
START REFERENCE
IF
IF
IF
% BETWEEN ZONES
mm ABOVE 0% ZONE
mm BELOW 100% ZONE
HORIZ mm FROM SWP STA
INTERNAL START % TO J6-6
INTERNAL START OFFSET MINUS TO J6-9
INTERNAL START OFFSET 100% TO J6-12
INTERNAL START MANUAL TO J6-4
SW577
SLOPE
START
SW576
SLOPE
START
+
−
1ST
2ND
TO J8-3
TO J8-C
SW579A
START LEVEL
(ONES)
CONCENTRIC CONTROL
IF
IF
IR
IR
0
1
2
3
4
5
6
7
8
9
1 TO J6-EE
2 TO J6-CC
4 TO J6-AA
8 TO J6-Y
SW589A
STOP LEVEL
(ONES)
CONCENTRIC CONTROL
IF
IF
IR
IR
0
1
2
3
4
5
6
7
8
9
1 TO J7-EE
2 TO J7-CC
4 TO J7-AA
8 TO J7-Y



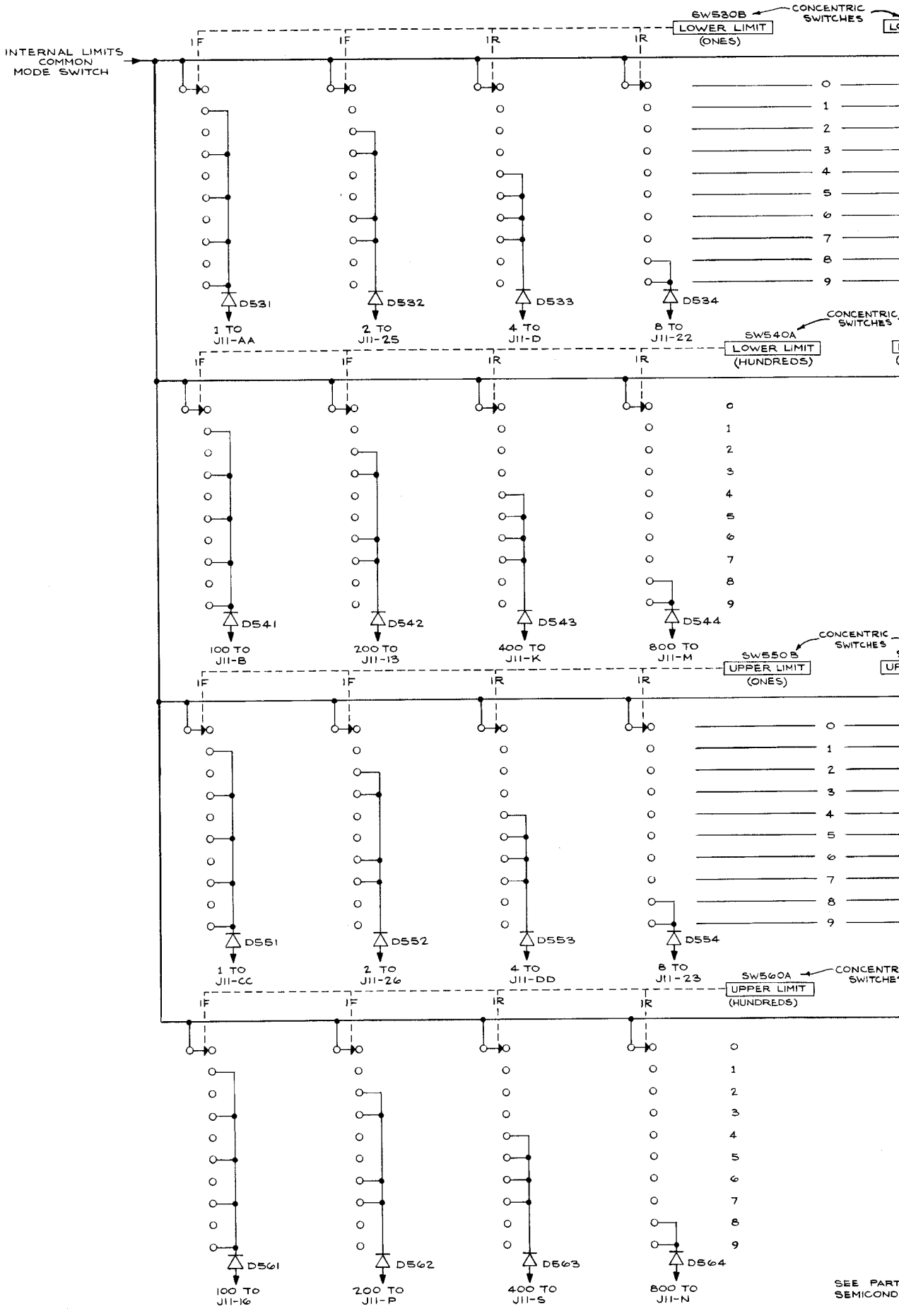


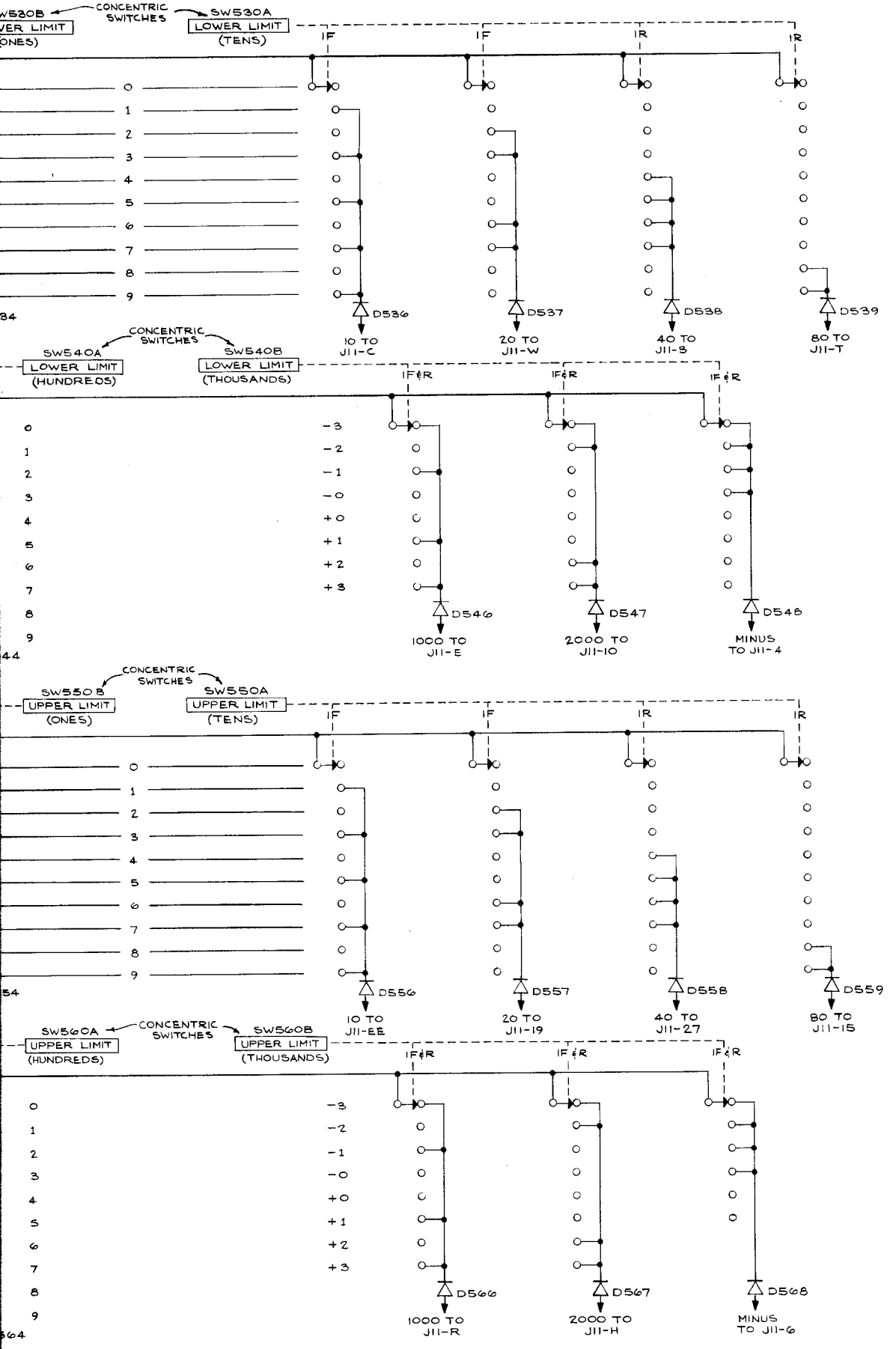


667

A2

START & STOP SWITCHES 18


INTERNAL LIMITS COMMON MODE SWITCH
IF
IF
IR
IR
SW530B
CONCENTRIC SWITCHES
LOWER LIMIT
(ONES)
0
1
2
3
4
5
6
7
8
9
D531
D532
D533
D534
1 TO J11-AA
2 TO J11-25
4 TO J11-D
8 TO J11-22
SW540A
LOWER LIMIT
(HUNDREDS)
D541
D542
D543
D544
100 TO J11-B
200 TO J11-13
400 TO J11-K
800 TO J11-M
SW550B
UPPER LIMIT
(ONES)
D551
D552
D553
D554
1 TO J11-CC
2 TO J11-26
4 TO J11-DD
8 TO J11-23
SW560A
UPPER LIMIT
(HUNDREDS)
D561
D562
D563
D564
100 TO J11-16
200 TO J11-P
400 TO J11-S
800 TO J11-N



SEE PARTS LIST FOR SEMICONDUCTOR TYPES

667

LIMIT SWITCHES 19

A1

J101

	FUNCTION	CNTR ⟨12⟩ ⟨11⟩ ⟨10⟩	J5 ⟨3⟩	J8 ⟨9⟩	J9 ⟨8⟩	J10 ⟨1⟩	TIE STRIP (CSC) ⟨11⟩	J204
1	DECIMAL 2	AK					13	1
2	DECIMAL 3	AM					12	2
3	DECIMAL 4	AR					11	3
4								
5	A (UNITS)							
6	V (UNITS)	I					10	4
7	S (UNITS)	AV					9	
8	M (UNITS)	K					8	6
9	μ (UNITS)	O					7	7
10	N (UNITS)	Q					6	8
11	CH A SIGNAL		21					
12	Shield		Y					
13								
14	SWEEP SPEEDUP				P			31
15	SWEEP RESET				H			32
16	INTENS ZONE ENABLE					A		
17	CRT CATHODE					B		
18	GROUND							
19	GROUND							
20	SWEEP		P					
21	SWEEP GATE		U					
22	10 MHz ENABLE			Y				
23	CH B Signal		EE					
24	Shield		27					
25	HORIZ D, U, ÷ GND					K		
26	CH A ÷ GND					11		
27	CH B ÷ GND					M		
28	CH A D & U GND					L		
29	CH B D & U GND					N		
30	HORIZ ÷2			10				
31	HORIZ ÷5	AV					5	
32	VERTICAL ÷1		B					
33	VERTICAL ÷2		A					
34	VERTICAL ÷5	AQ					4	
35	CLOCK			E				
36	Shield			4				

J201

	FUNCTION	J1 ⟨4⟩	J2 ⟨4⟩	J6 ⟨7⟩	J7 ⟨7⟩	J8 ⟨9⟩	J9 ⟨8⟩	J10 ⟨1⟩	J204	TIE STRIP (CSD) ⟨11⟩	SW 520 (MODE) ⟨16⟩
1	A 0% POSITION 8	CC									
2	A 0% POSITION 4	Y									
3	A 0% POSITION 2	L									
4	A 0% POSITION 1	J									
5	A 0% POSITION 0.5	F									
6	A 0% PEAK 4 cm	N									
7	A 0% PEAK 2 cm	U									
8	VOLTS			2	2	D		9			
9	A 100% POSITION 8	25									
10	A 100% POSITION 4	21									
11	A 100% POSITION 2	10									
12	A 100% POSITION 1	8									
13	A 100% POSITION 0.5	6									
14	A 100% PEAK 4 cm	12									
15	A 100% PEAK 2 cm	17									
16	A CHOP						3		15		
17	PROGRAM COMMON									1	✓
18	PROGRAM COMMON									1	✓
19	B 0% POSITION 8		CC								
20	B 0% POSITION 4		Y								
21	B 0% POSITION 2		L								
22	B 0% POSITION 1		J								
23	B 0% POSITION 0.5		F								
24	B 0% PEAK 4 cm		N								
25	B 0% PEAK 2 cm		U								
26	MEASURE AVERAGE						7				
27	B 100% POSITION 8		25								
28	B 100% POSITION 4		21								
29	B 100% POSITION 2		10								
30	B 100% POSITION 1		8								
31	B 100% POSITION 0.5		6								
32	B 100% PEAK 4 cm		12								
33	B 100% PEAK 2 cm		17								
34	B CHOP						CC		16		
35	PROGRAM COMMON									1	✓
36	PROGRAM COMMON									1	✓

J202

	FUNCTION	J6 ◇7	J7 ◇7	J8 ◇9	J9 ◇8	J10 ◇1	SW 520 (MODE) ◇16	TIE STRIP (CSD) ◇11
1	B CHANNEL	M				12		
2	HORIZ MM	3						
3	% BETWEEN	5						
4	MM BELOW	8						
5	OFFSET FROM 100%	N						
6	MINUS SLOPE			I				
7	2 nd SLOPE			A				
8	RESET INHIBIT				9			
9	OFFSET 80	13						
10	OFFSET 40	14						
11	OFFSET 20	17						
12	OFFSET 10	19						
13	OFFSET 8	21						
14	OFFSET 4	23						
15	OFFSET 2	25						
16	OFFSET 1	27						
17	PROGRAM COMMON						✓	1
18	PROGRAM COMMON						✓	1
19	B CHANNEL		M					
20	HORIZ MM		3					
21	% BETWEEN		5					
22	MM BELOW		8					
23	OFFSET FROM 100%		N				✓	
24	MINUS SLOPE			CC				
25	2 nd SLOPE			AA				
26	EXT SCALE				10			
27	OFFSET 80		13					
28	OFFSET 40		14					
29	OFFSET 20		17					
30	OFFSET 10		19					
31	OFFSET 8		21					
32	OFFSET 4		23					
33	OFFSET 2		25					
34	OFFSET 1		27					
35	PROGRAM COMMON						✓	1
36	PROGRAM COMMON						✓	1

J203

	FUNCTION	COUNTER BOARD ◇10 ◇12	J8 ◇9	J11 ◇13 ◇14	SW520 (MODE) ◇16	SW560 (LIMIT) ◇19	SW550 (LIMIT) ◇19	SW540 (LIMIT) ◇19	SW530 (LIMIT) ◇19	TIE STRIP (CSD) ◇11
1	EXT ÷ 2		19							
2	UPPER MINUS			6		✓				
3	UPPER LIMIT 2000			H		✓				
4	UPPER LIMIT 1000			R		✓				
5	UPPER LIMIT 800			N		✓				
6	UPPER LIMIT 400			S		✓				
7	UPPER LIMIT 200			P		✓				
8	UPPER LIMIT 100			16		✓				
9	UPPER LIMIT 80			15			✓			
10	UPPER LIMIT 40			27			✓			
11	UPPER LIMIT 20			19			✓			
12	UPPER LIMIT 10			EE			✓			
13	UPPER LIMIT 8			23			✓			
14	UPPER LIMIT 4			DD			✓			
15	UPPER LIMIT 2			26			✓			
16	UPPER LIMIT 1			CC			✓			
17	PROGRAM COMMON				✓					1
18	PROGRAM COMMON				✓					1
19	EXT ÷ 5	AS								
20	LOWER MINUS			4				✓		
21	LOWER LIMIT 2000			10				✓		
22	LOWER LIMIT 1000			E				✓		
23	LOWER LIMIT 800			M				✓		
24	LOWER LIMIT 400			K				✓		
25	LOWER LIMIT 200			13				✓		
26	LOWER LIMIT 100			B				✓		
27	LOWER LIMIT 80			T					✓	
28	LOWER LIMIT 40			3					✓	
29	LOWER LIMIT 20			W					✓	
30	LOWER LIMIT 10			C					✓	
31	LOWER LIMIT 8			22					✓	
32	LOWER LIMIT 4			D					✓	
33	LOWER LIMIT 2			25					✓	
34	LOWER LIMIT 1			AA					✓	
35	PROGRAM COMMON				✓					1
36	PROGRAM COMMON				✓					1

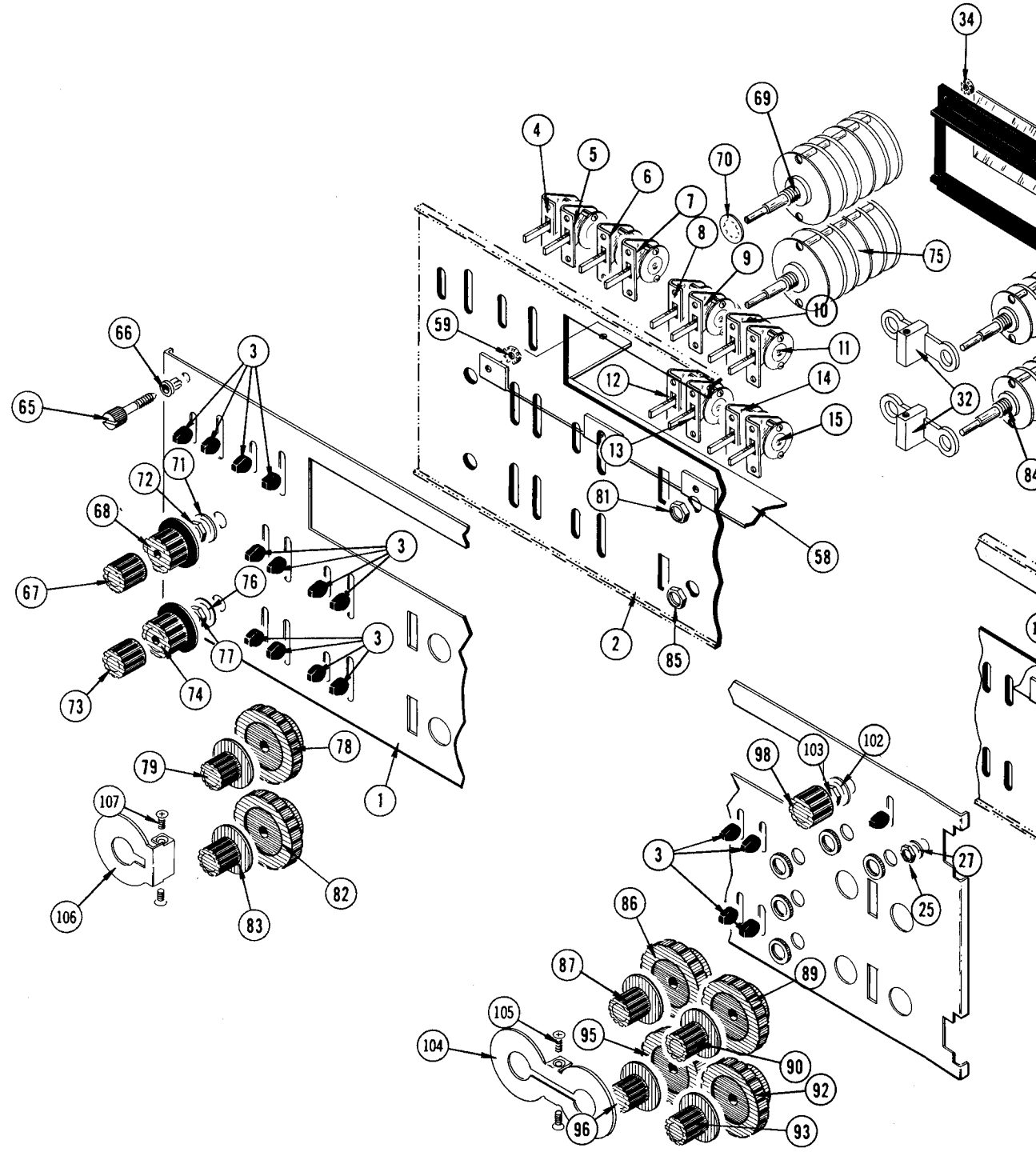
J204

	FUNCTION	COUNTER BOARD ◇12 ◇17	J3 ◇5	J9 ◇8	TIE STRIP (CSC) ◇11	TIE STRIP (CSD) ◇11	J101	SW520 (MODE) ◇16	J301
1	DECIMAL 2	AK			13		1		
2	DECIMAL 3	AM			12		2		
3	DECIMAL 4	AR			11		3		
4	V (UNITS)	I			10		6		
5	S (UNITS)	J			3				
6	M (UNITS)	K			8		8		
7	μ (UNITS)	O			7		9		
8	N (UNITS)	Q			6		10		
9	HIGH SPEED PROGRAM			N					
10									
11									
12									
13									
14									
15									
16									
17	PROGRAM COMMON				1			✓	
18	GND								
19	READ RED	AY				4			27
20	READ GREEN	BA				3			28
21	READ YELLOW	BB				2			29
22	+50V		V						
23	+12V		X						
24	+3.8V		Z						
25	−3.5V		BB						
26	−50V		DD						
27	PRINT COMMAND			21					31
28	EXT HOLD			M					30
29	PLUG TRIGGER			Y					
30	MINUS TRIGGER			W					
31	SWEEP SPEEDUP			P					
32	SWEEP RESET			H					
33	A CHOP DRIVE			I					
34	B CHOP DRIVE			EE					
35	GND		FF						
36	GND						19		

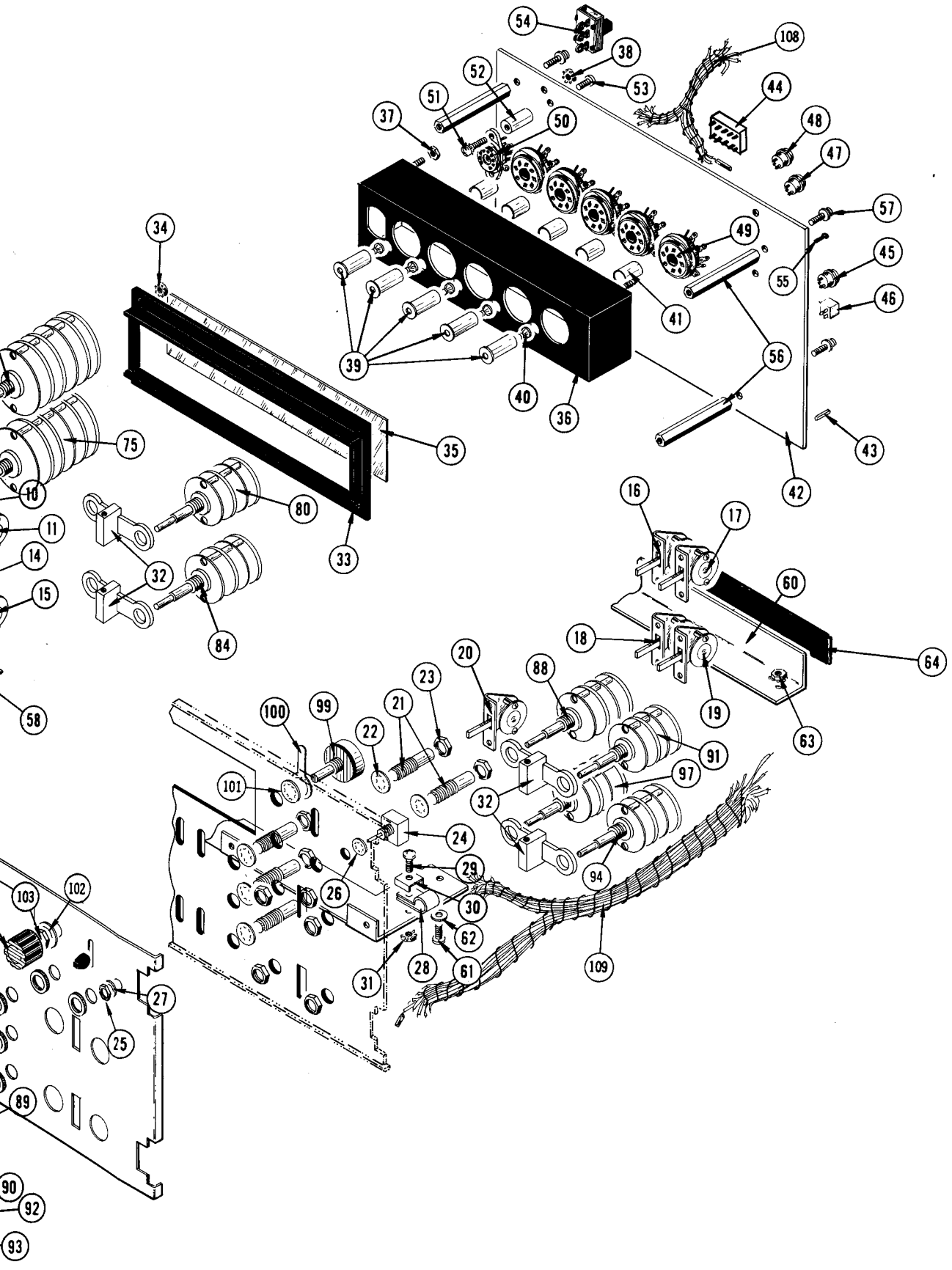
J301

	FUNCTION	J1 ◇4	J9 ◇8	J11 ◇13 ◇14	J204	CNTR ◇10 ◇11 ◇12	TIE STRIP (CSD) ◇11
1	READ PLUS					AH	8
2	READ MINUS			5. FF		AN	
3	READ 2000			J		AF	
4	READ 1000			F		AE	
5	READ 800			L		AD	
6	READ 400			7		AC	
7	READ 200			12		AB	
8	READ 100			8		AA	
9	READ 80			U		Z	
10	READ 40			9		Y	
11	READ 20			21		X	
12	READ 10			11		W	
13	READ 8			Y		V	
14	READ 4			H		U	
15	READ 2			Z		T	
16	READ 1			17		S	
17							
18							
19	READ $X10^{-1}$						7
20	READ $X10^{-2}$						6
21	READ $X10^{-4}$						5
22	READ V (UNITS)						13
23	READ S (UNITS)						12
24	READ M (UNITS)						11
25	READ μ (UNITS)						10
26	READ N (UNITS)						9
27	READ RED				19		4
28	READ GREEN				20		3
29	READ YELLOW				21		2
30	EXTERNAL HOLD		M		28		
31	PRINT COMMAND		21		27		
32							
33							
34	+12 V	X					
35							
36	GND	FF					

TYPE 230 INTERCONNECTION TABLES



TYPE 230 DIGITAL UNIT


54
38
53
52
51
37
50
108
44
48
47
57
49
45
55
46
41
56
39
40
36
43
42
34
35
75
10
11
14
15
58
80
33
32
84
16
17
60
18
64
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20
88
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21
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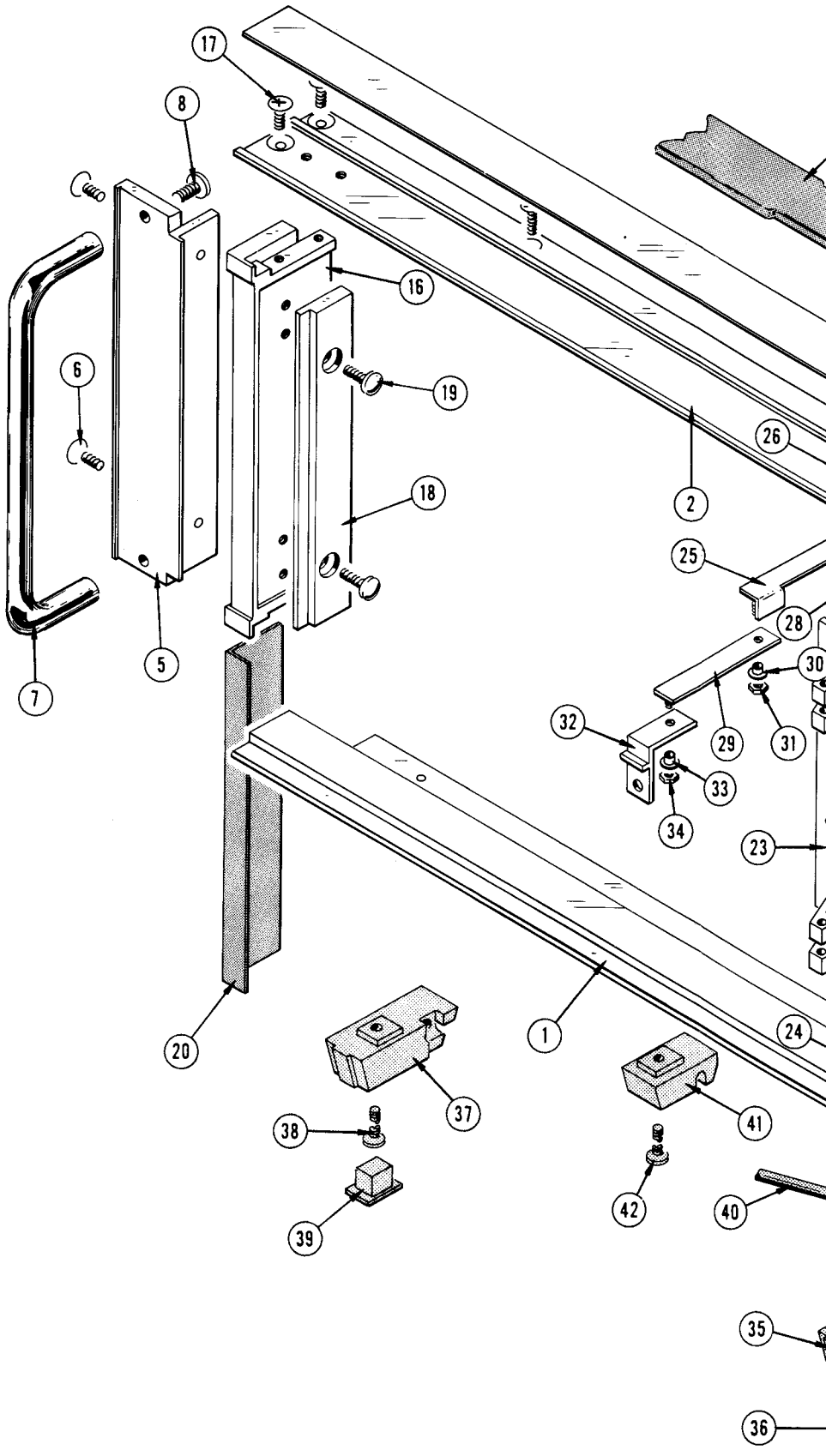
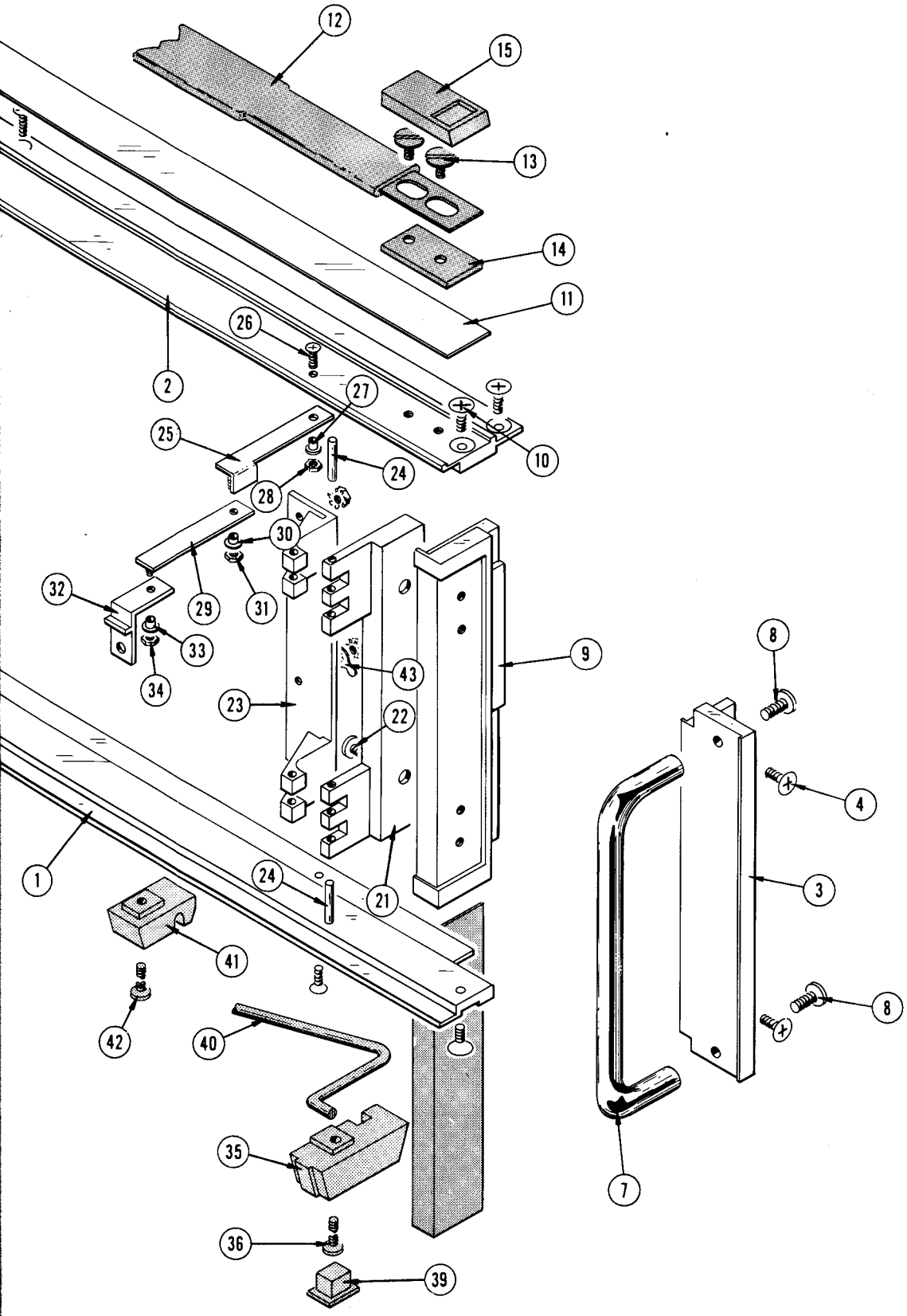
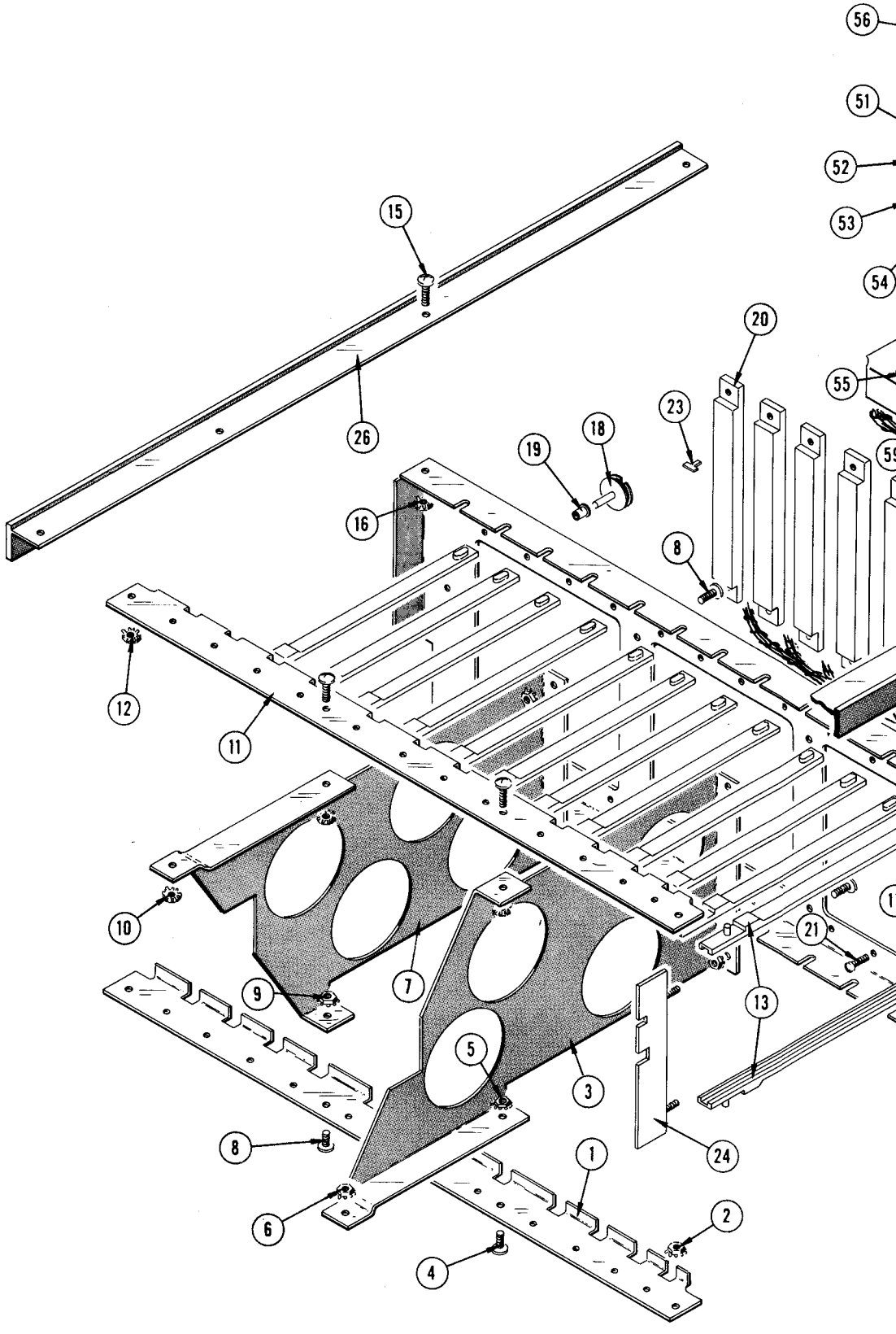
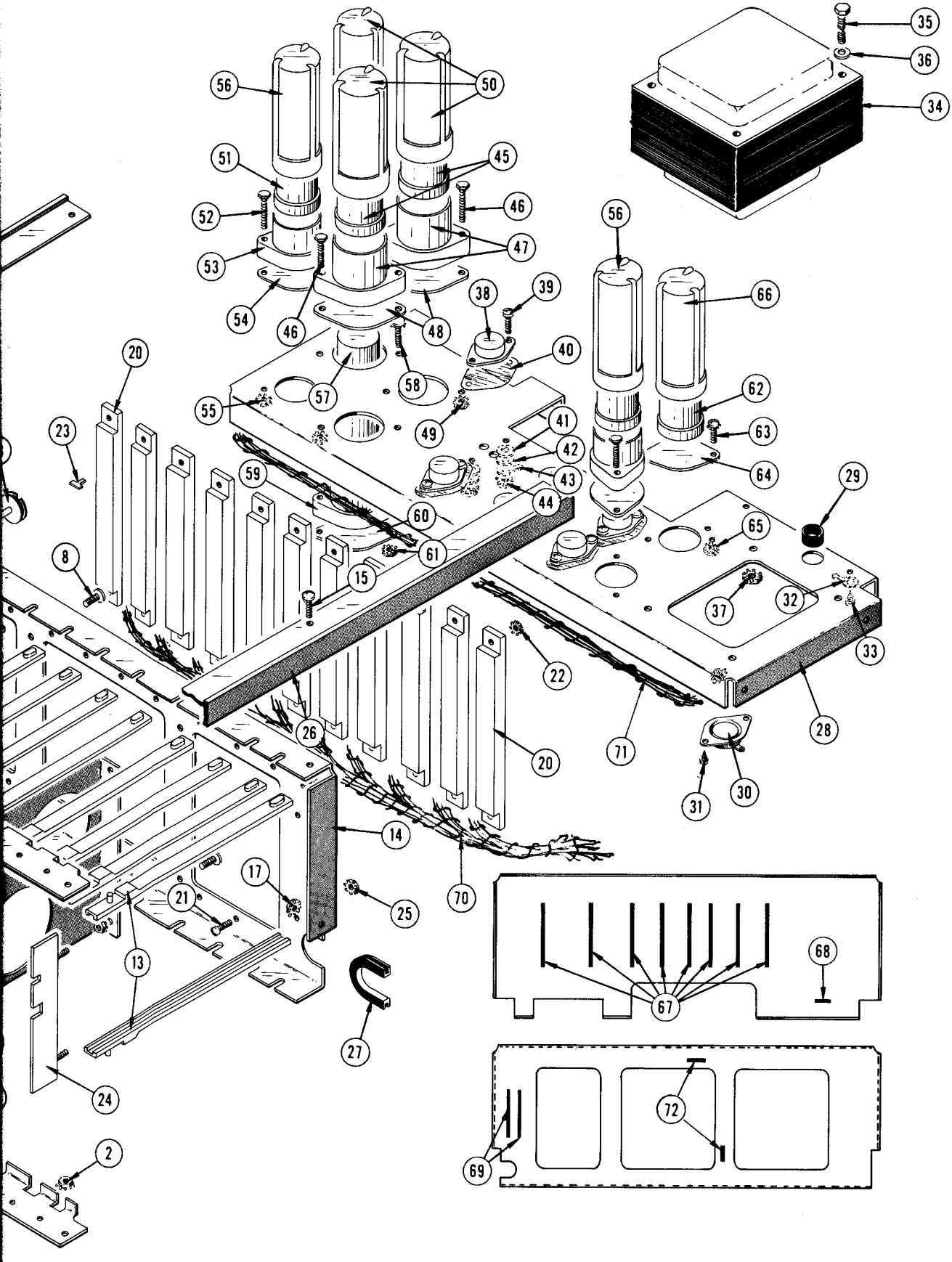
99
100
91
97
101
32
24
29
26
30
62
28
61
31
94
109
103
102
27
25
89
90
92
93


17
8
16
6
19
26
18
2
25
28
30
32
29
31
33
34
23
5
7
20
1
24
37
41
38
42
40
39
35
36


12
15
13
14
11
26
2
27
25
10
24
28
30
32
29
31
33
34
9
43
23
22
1
24
21
41
42
40
35
36
39
8
4
3
8
7



TYPE 230 DIGITAL UNIT


35
36
34
56
50
51
45
52
46
53
47
54
46
48
38
39
40
57
58
55
49
56
66
62
63
64
41
42
43
44
59
60
61
20
23
8
15
29
65
37
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26
71
28
20
31
30
14
17
21
25
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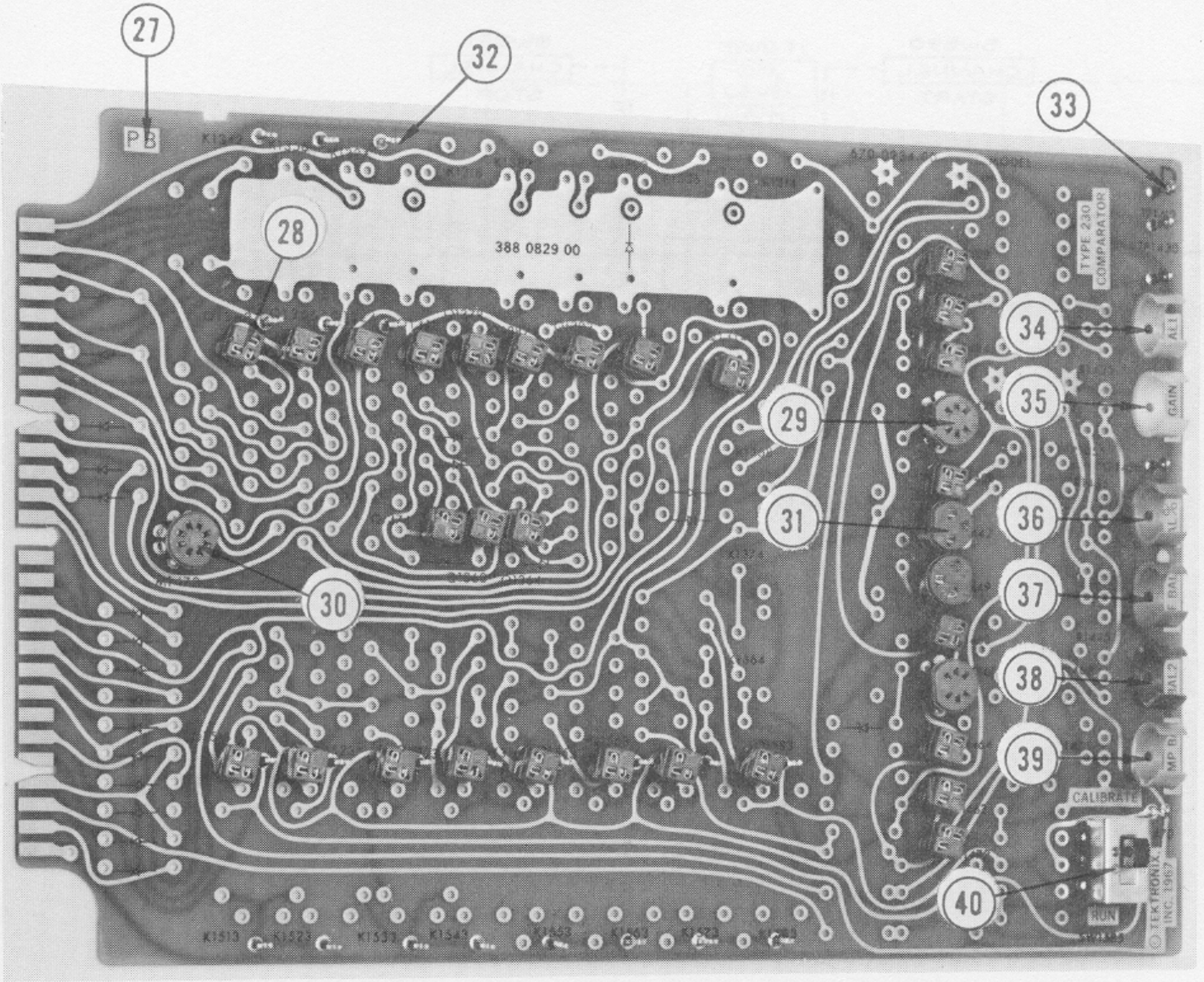
COMPARATOR


27
32
33
28
388 0829 00
TYPE 230
COMPARATOR
34
35
29
31
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30
37
38
39
CALIBRATE
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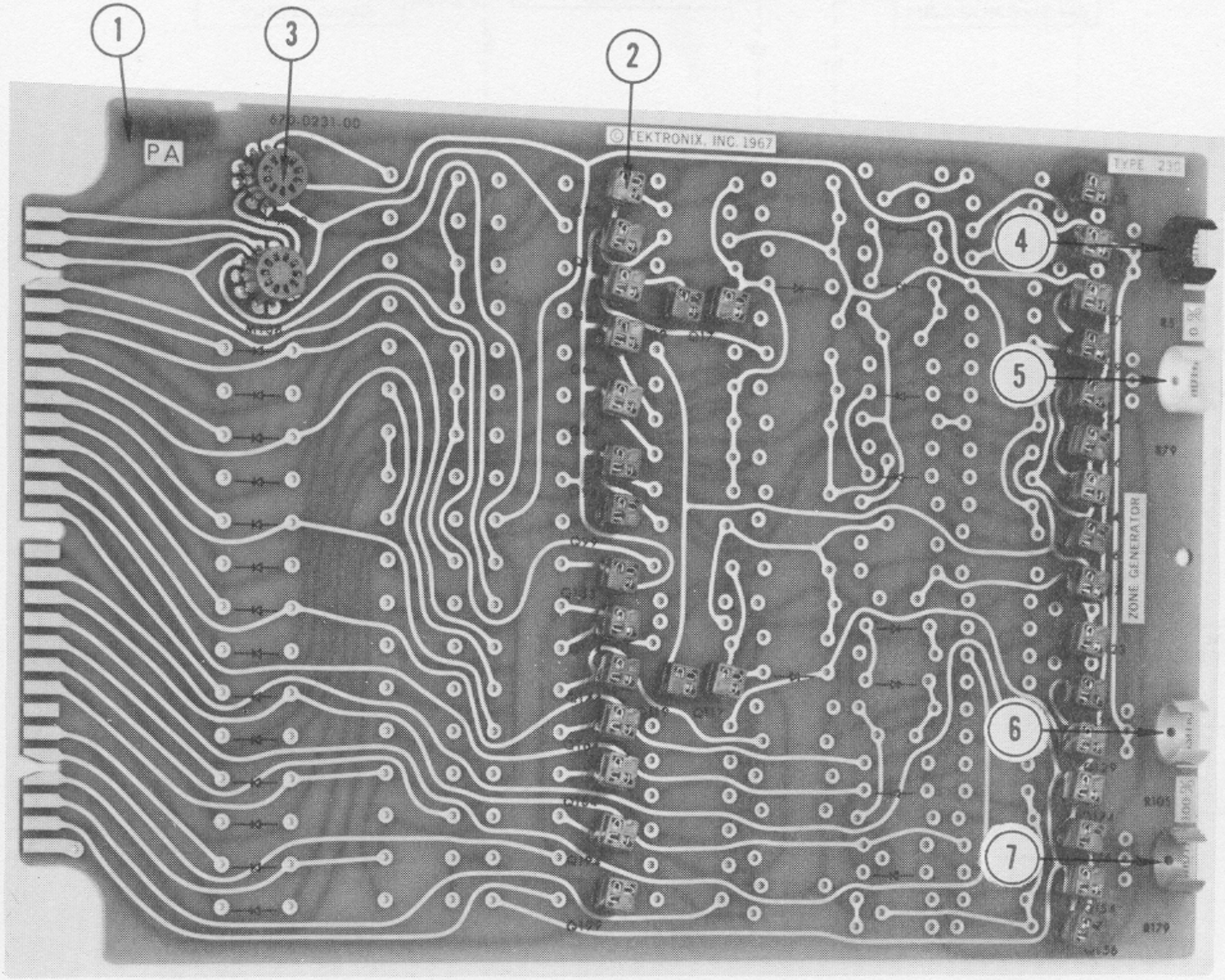
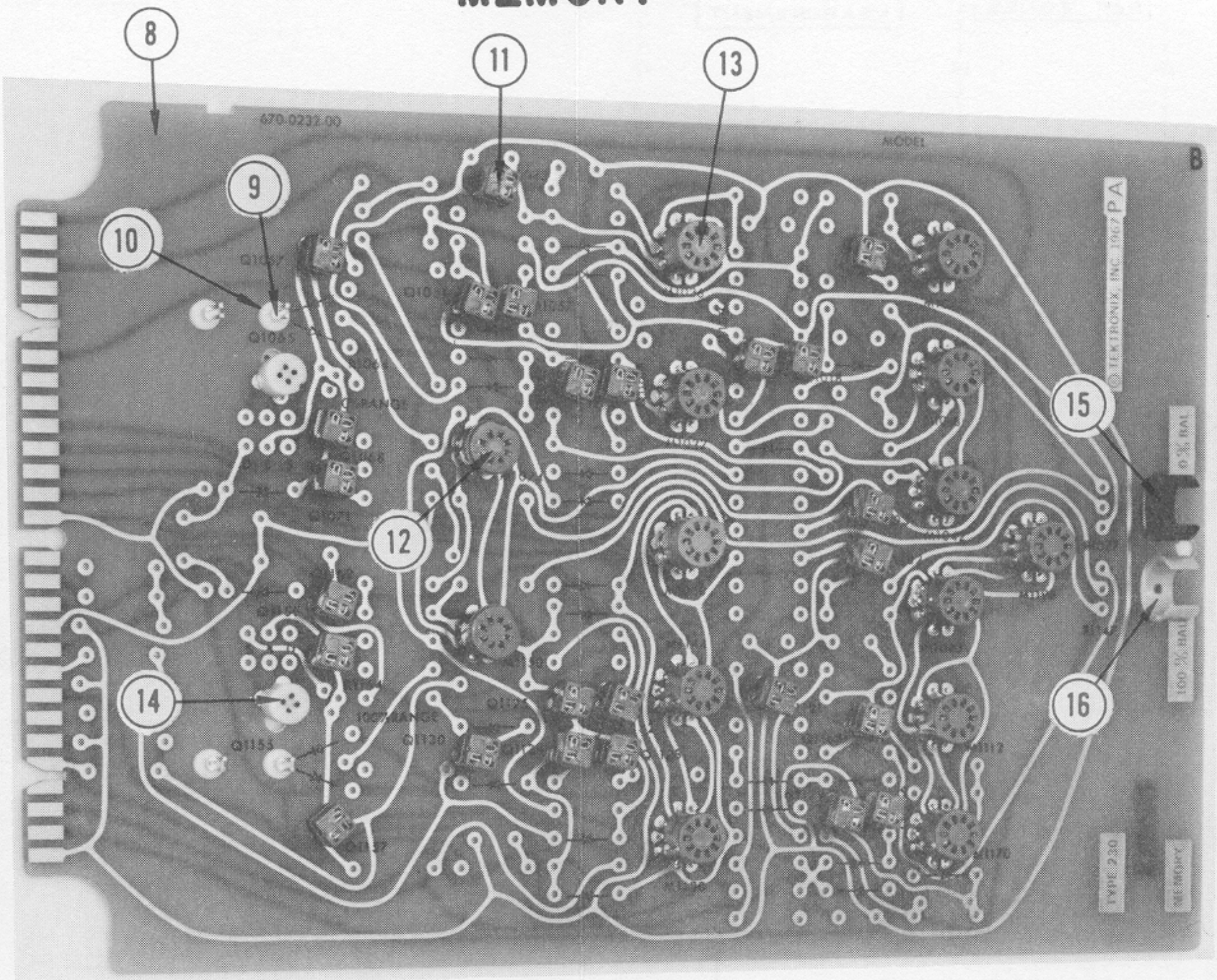
RUN
TEKTRONIX
INC. 1967

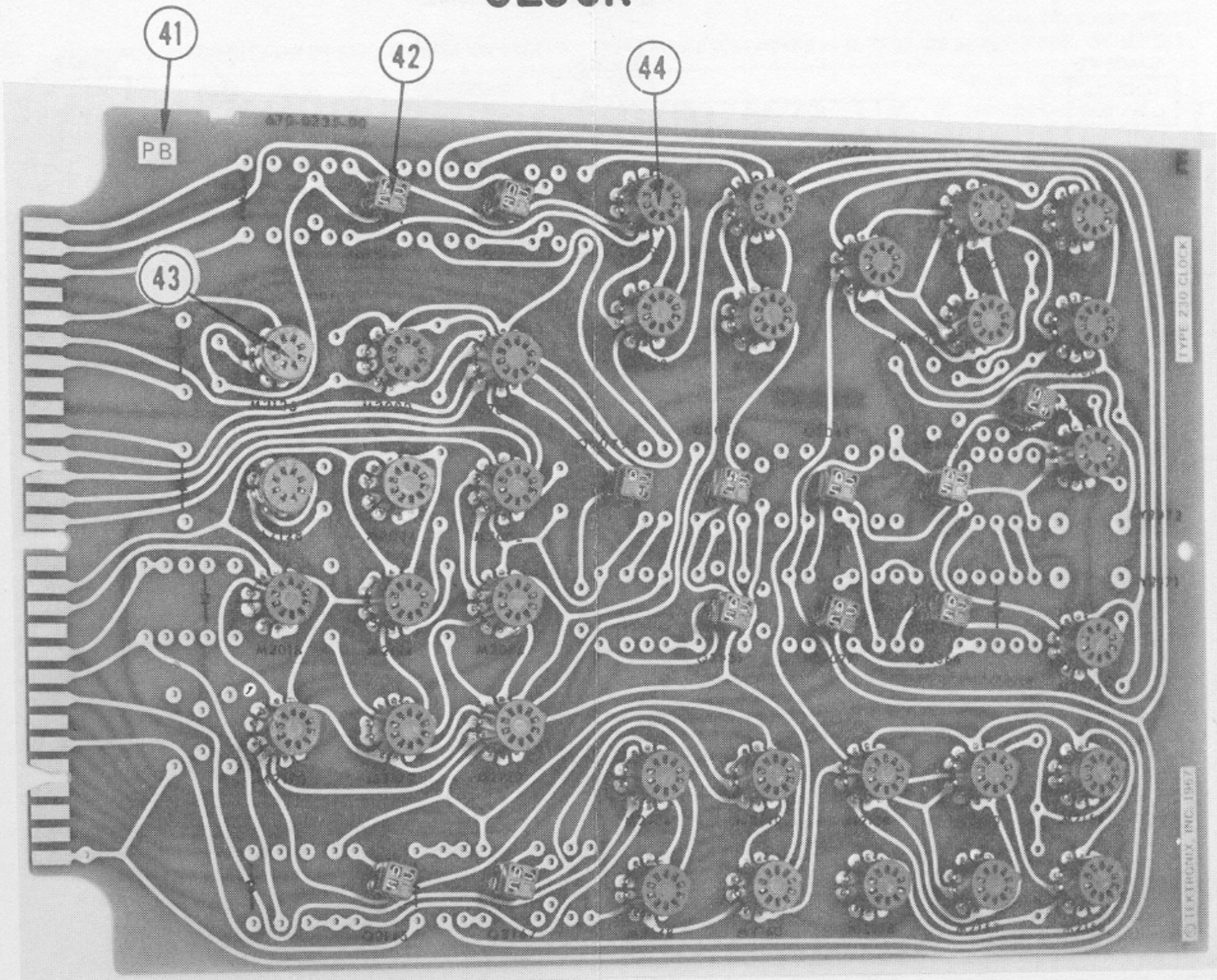
ZONE GENERATOR



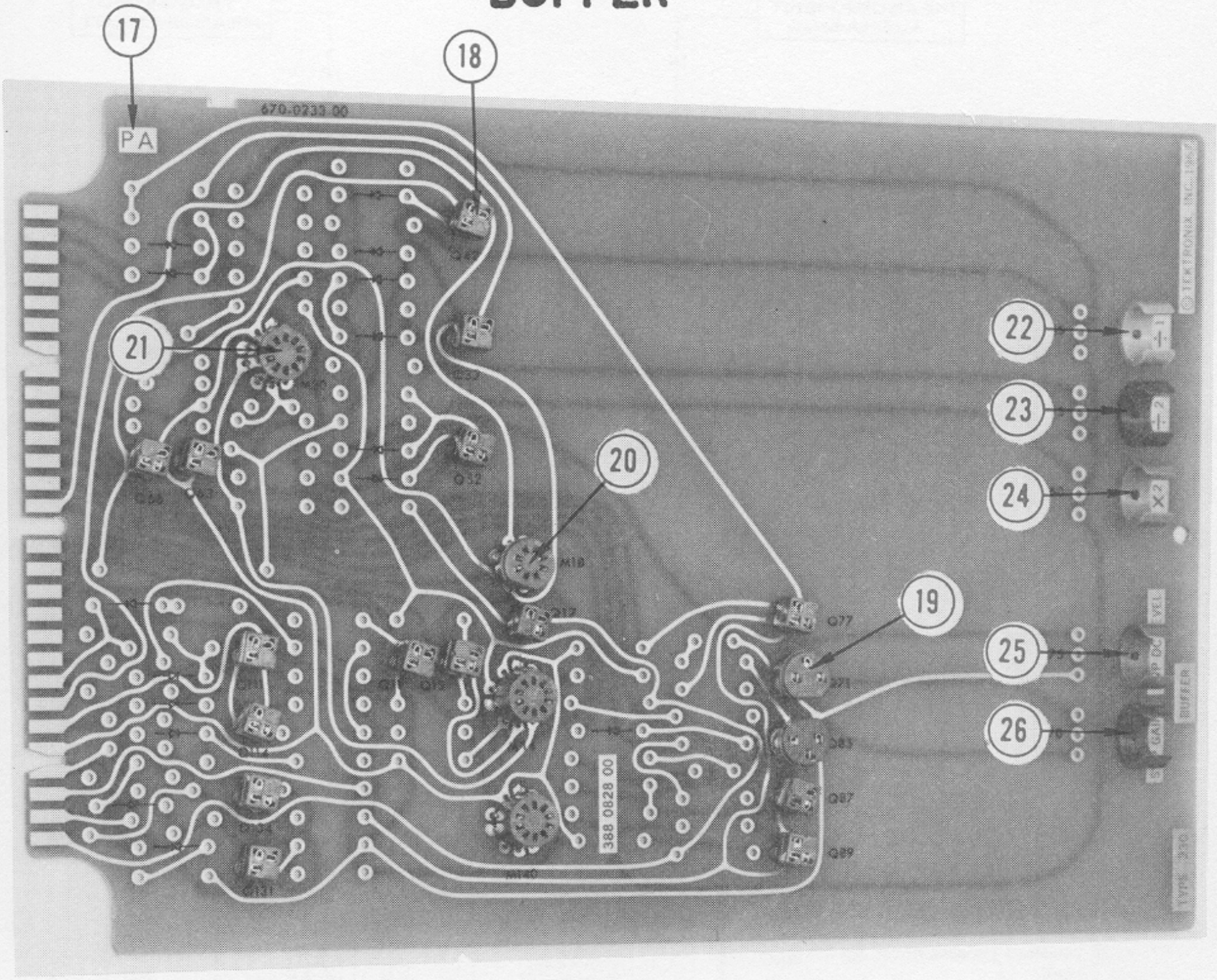
MEMORY



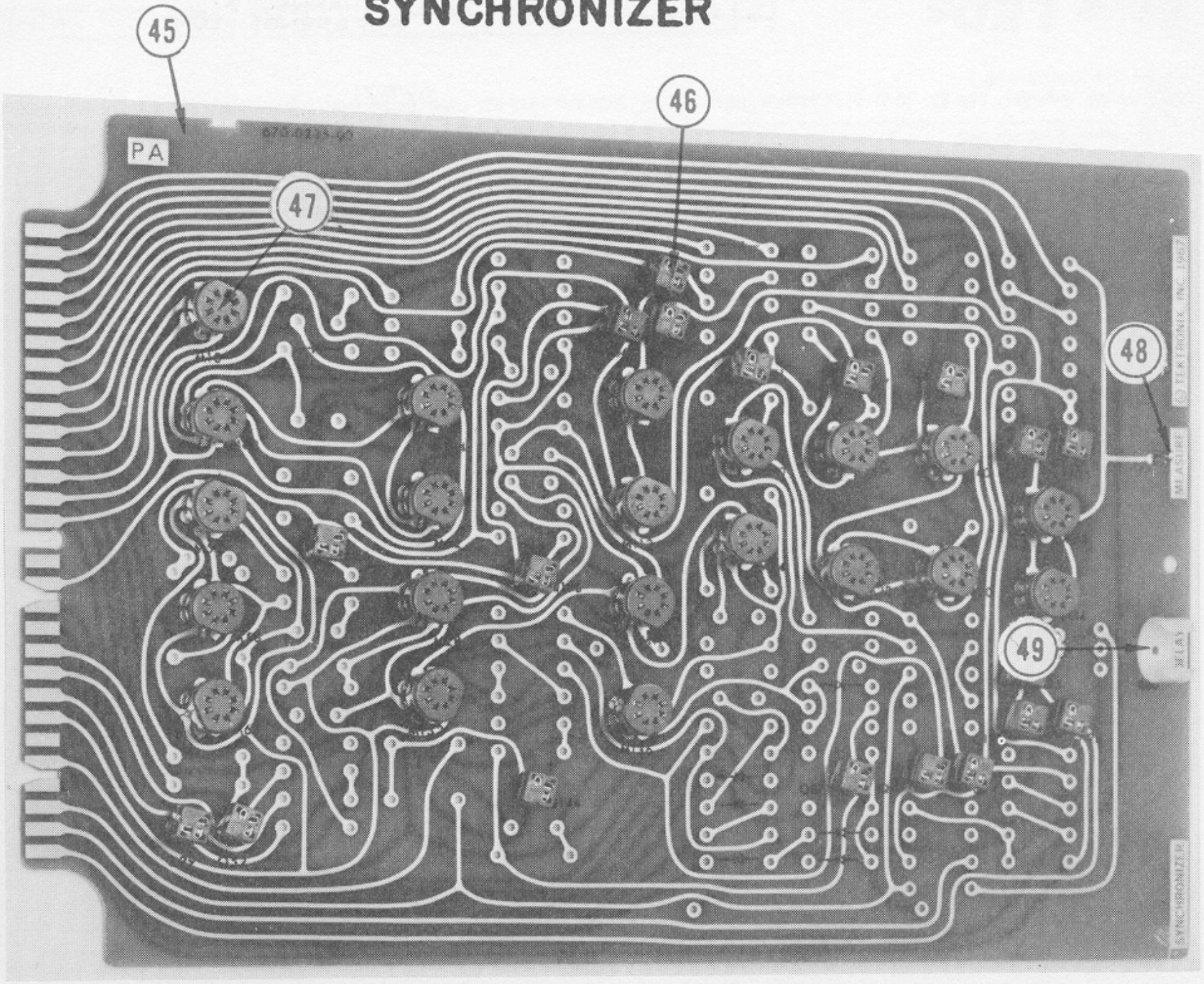
CLOCK



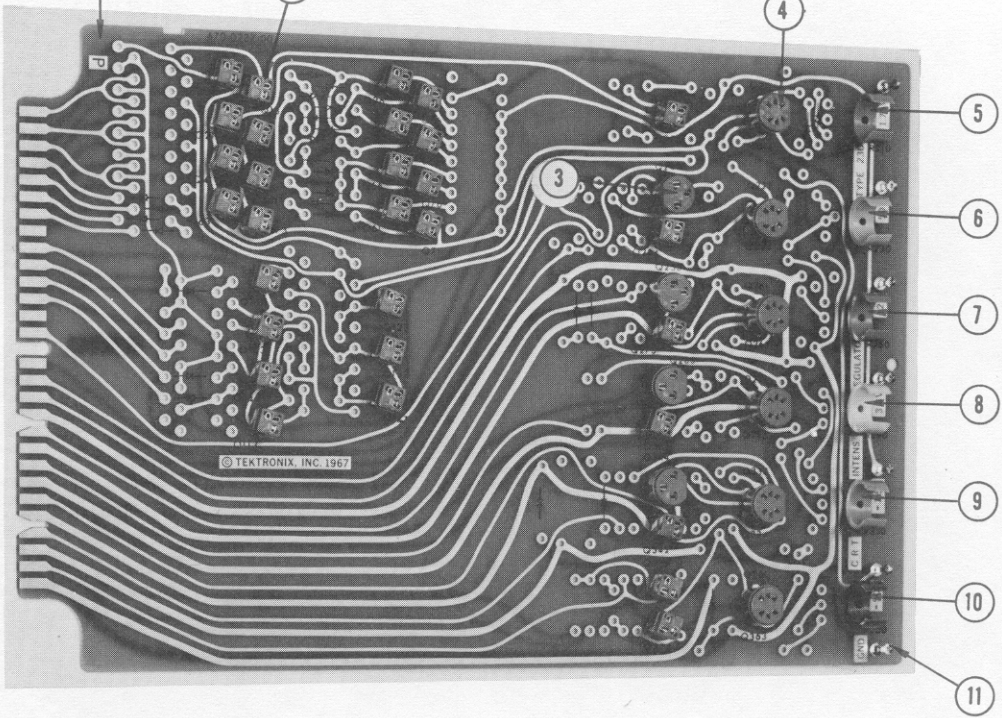
BUFFER



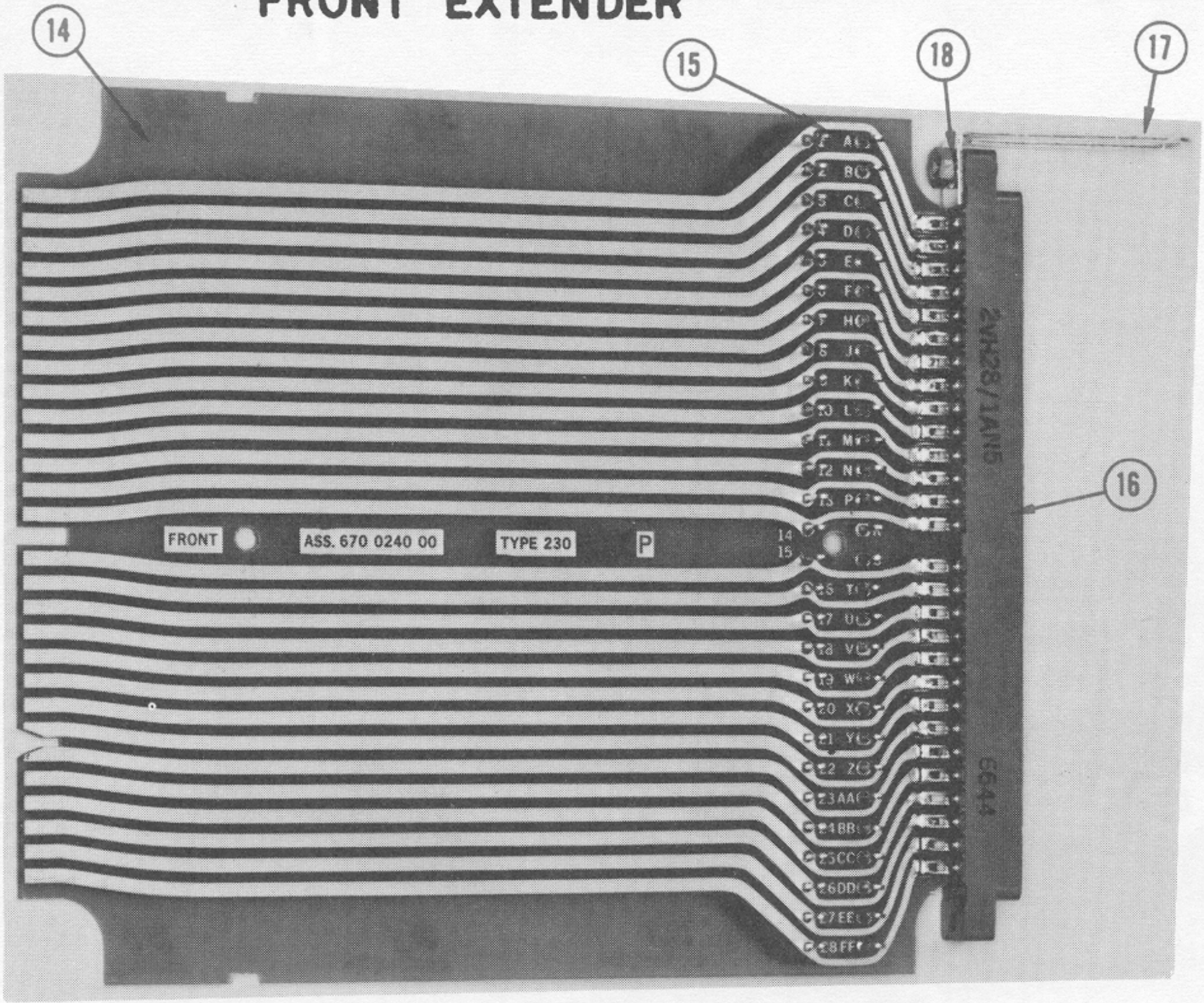
SYNCHRONIZER



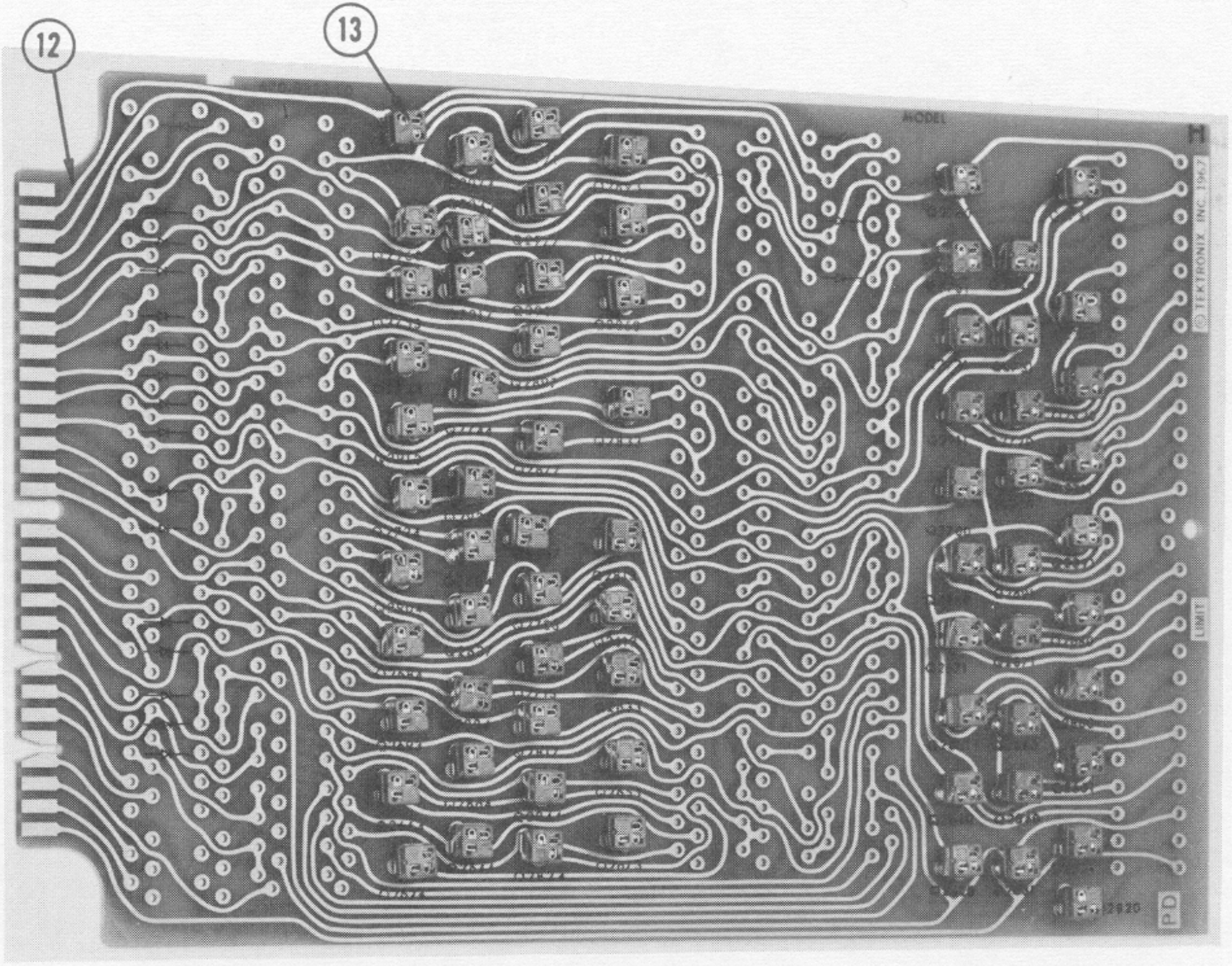
INTENS. REGULATOR



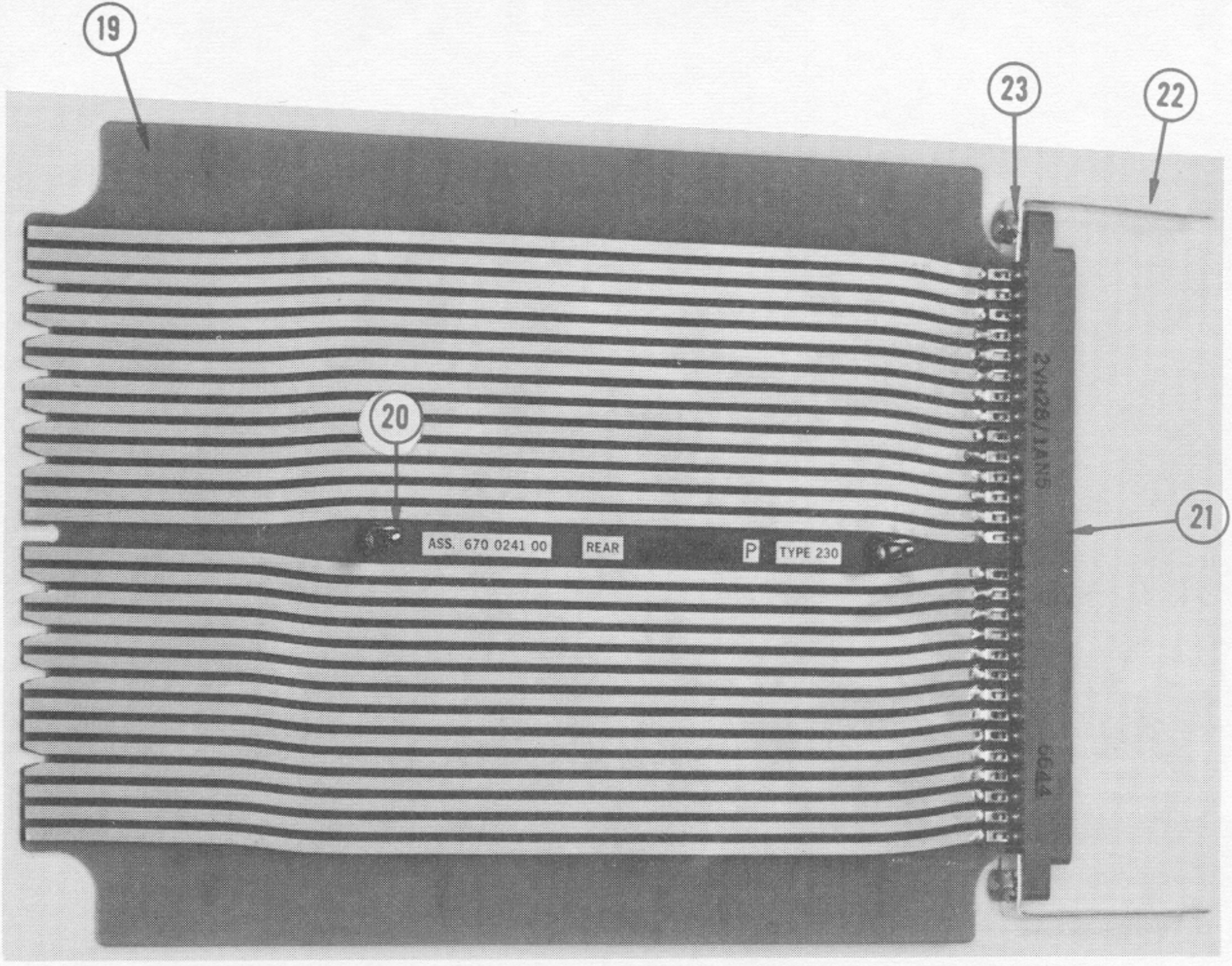
FRONT EXTENDER

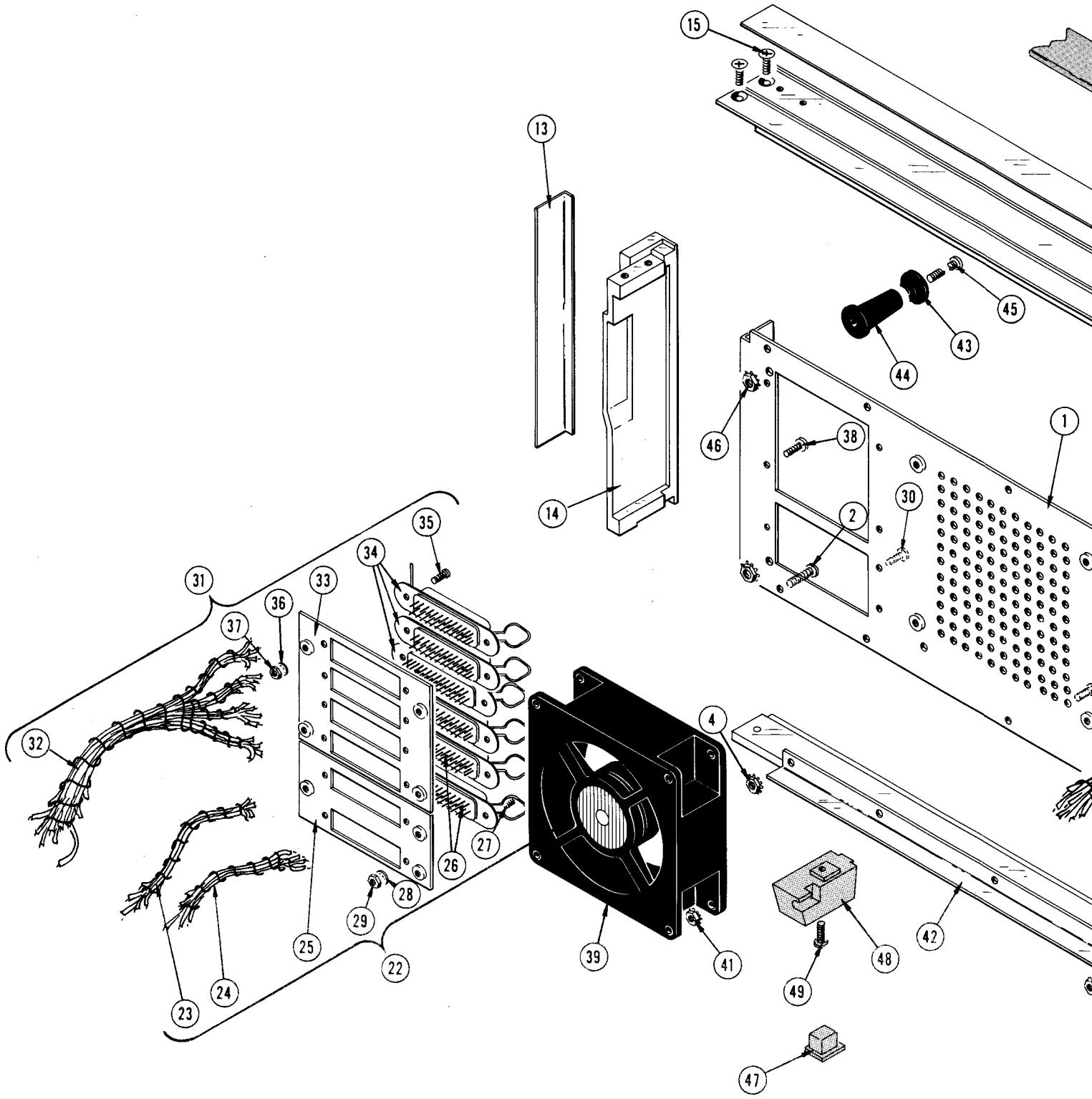


LIMIT

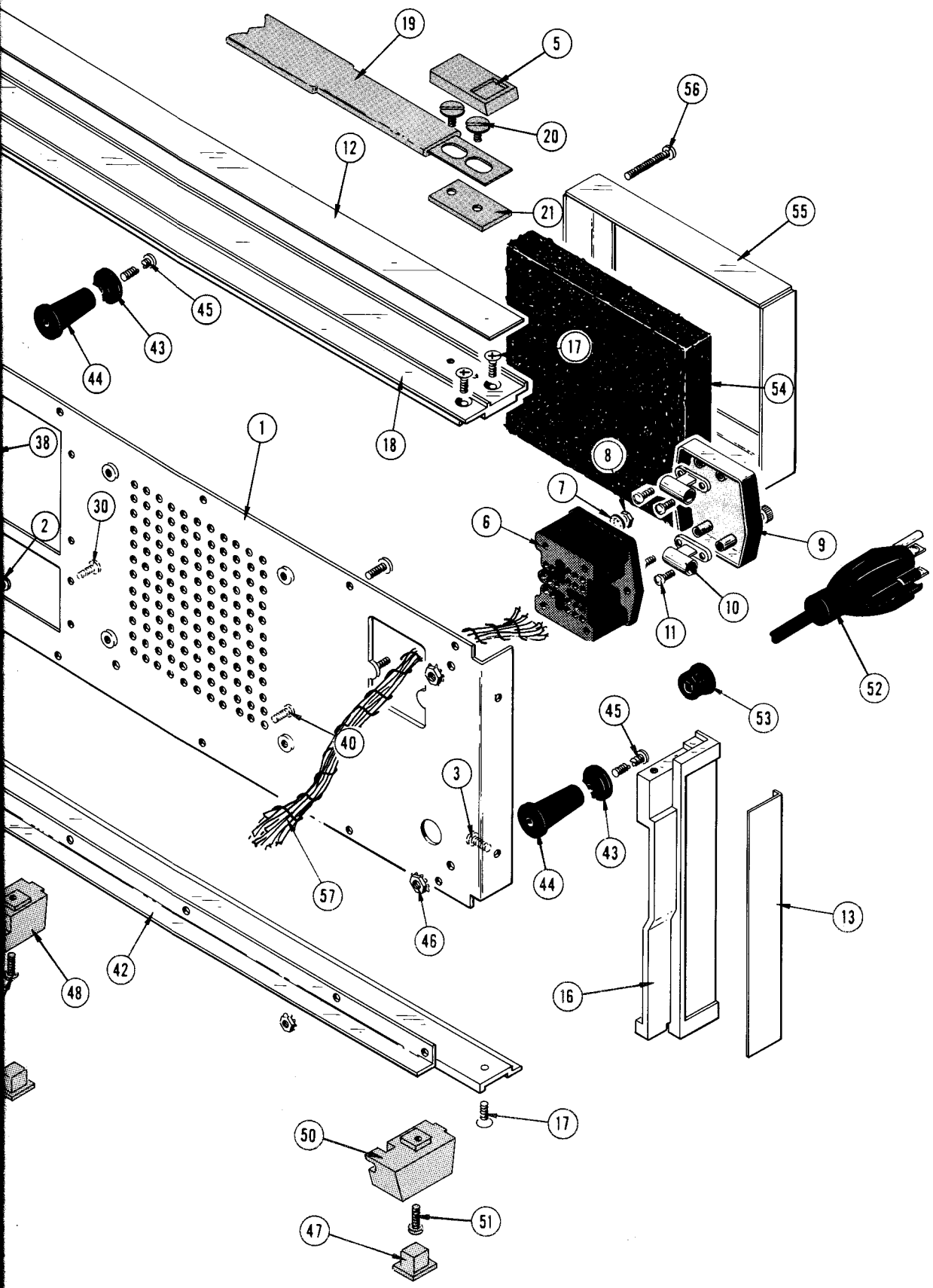


REAR EXTENDER





TYPE 230 DIGITAL UNIT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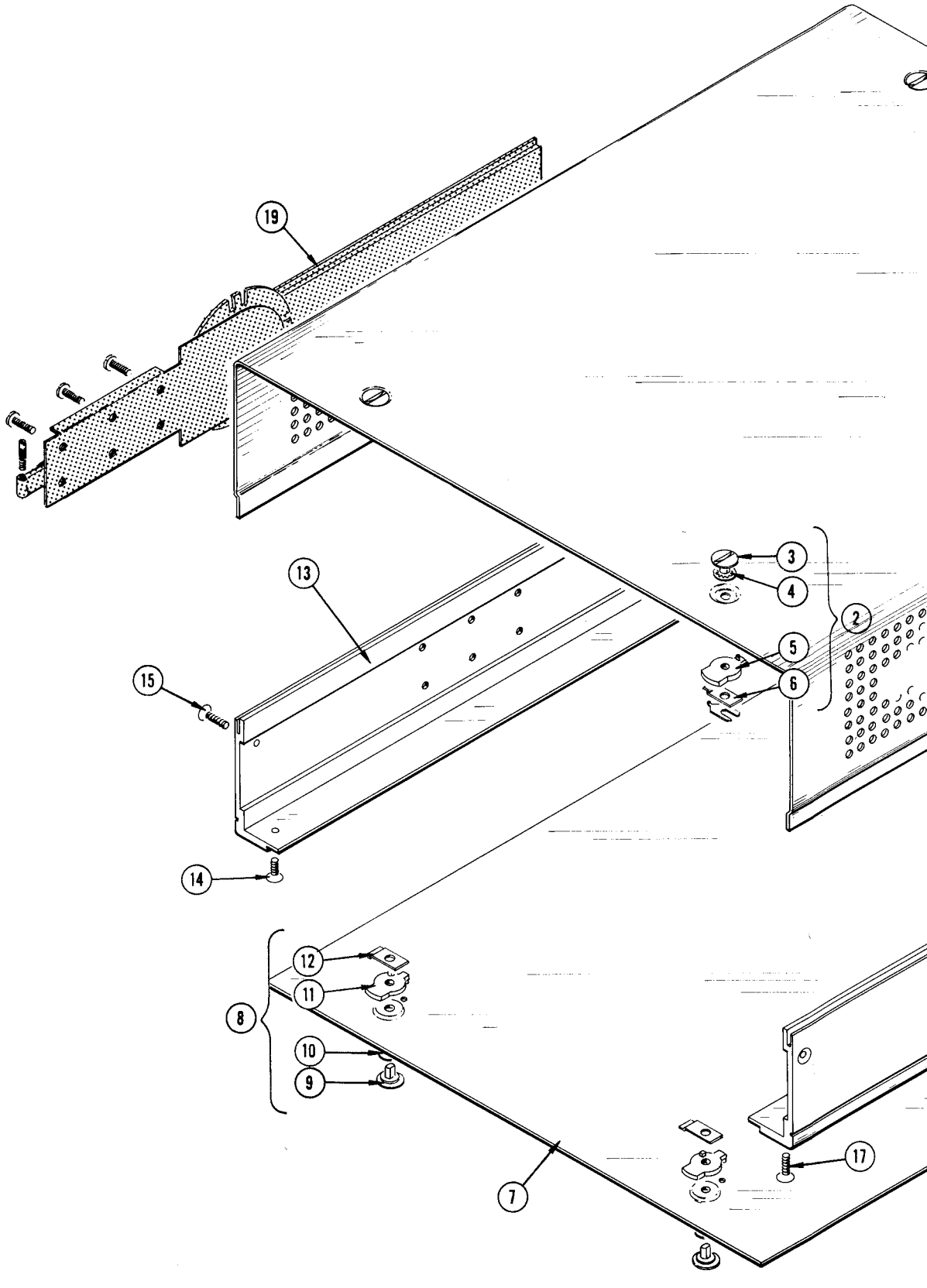
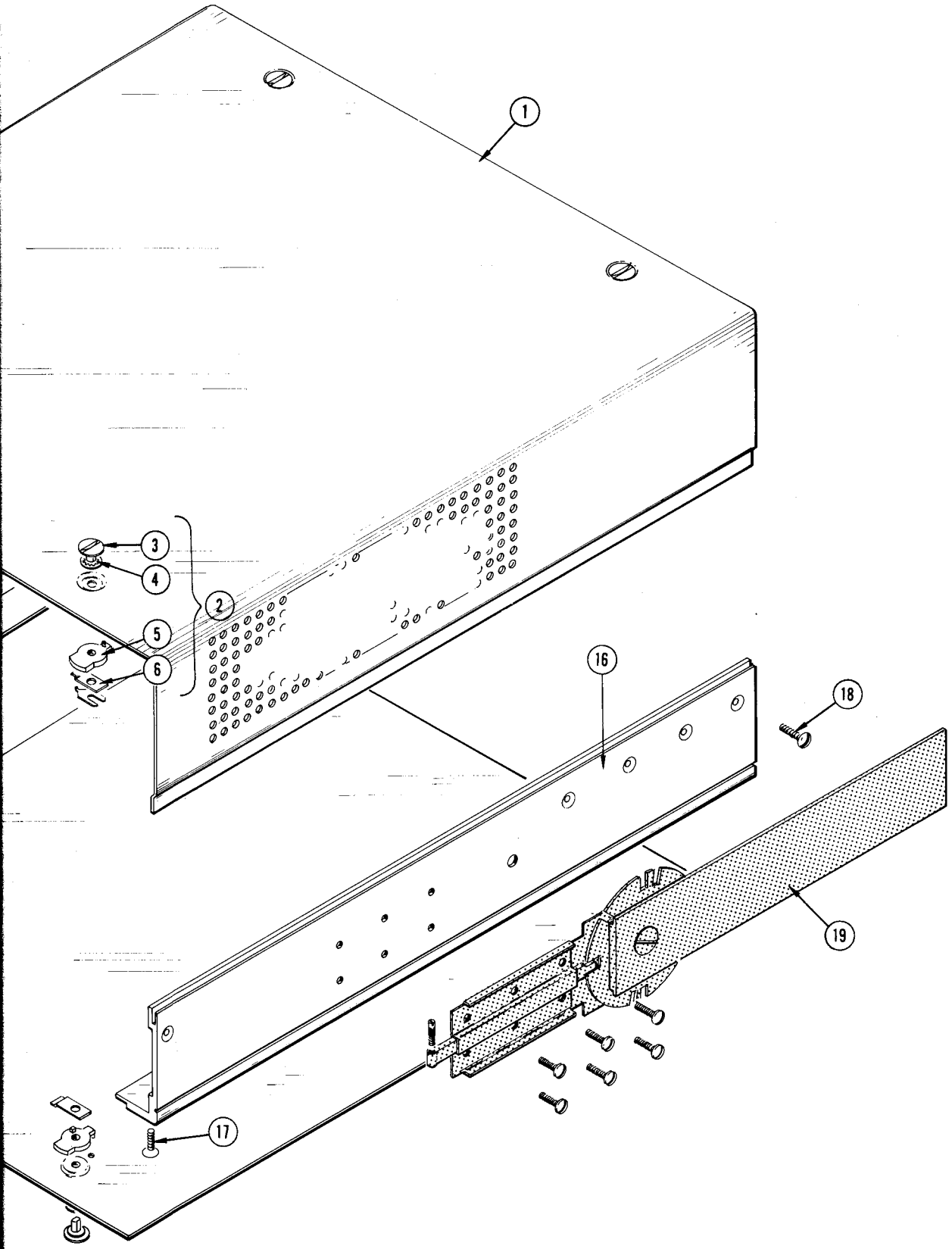


TYPE 230 DIGITAL UNIT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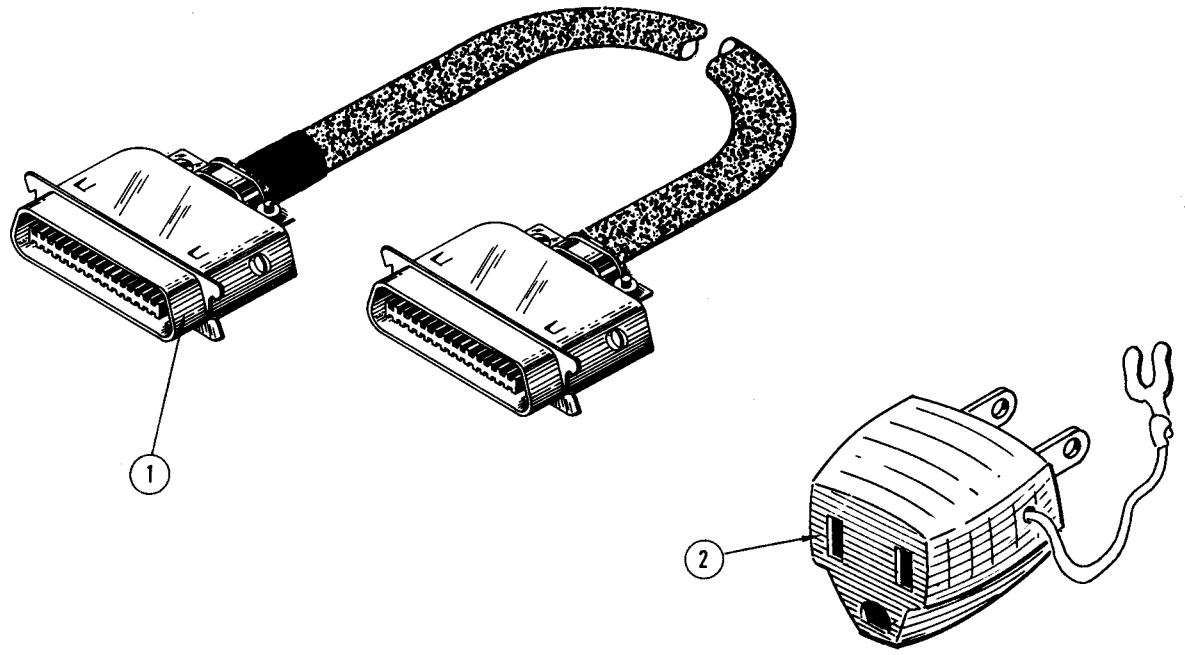

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty 1 2 3 4 5	Description
8-1	012-0119-01			1	CABLE, inter-connection
-2	103-0013-00			1	ADAPTER, power cord, 3 wire to 2 wire
	070-0635-00			2	MANUAL, instruction (not shown)
		OTHER PARTS FURNISHED WITH TYPE R230 ONLY			
	016-0097-00			1	KIT, ruggedizing hardware (not shown)
	016-0099-00			1	KIT, rackmounting hardware (not shown)
	351-0086-00	B010100	B040209	1	TRACK, slide, stationary & inter-section (pair, not shown)
	351-0085-00	B040210	B049999	1	TRACK, slide, stationary & inter-section (pair, not shown)
	351-0086-00	B050000		1	TRACK, slide, stationary & inter-section (pair, not shown)

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations which appear either on the back of the diagrams or on pullout pages immediately following the diagrams of the instruction manual.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the Description column.

Assembly and/or Component
Detail Part of Assembly and/or Component
mounting hardware for Detail Part
Parts of Detail Part
mounting hardware for Parts of Detail Part
mounting hardware for Assembly and/or Component

Mounting hardware always appears in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation.

Mounting hardware must be purchased separately, unless otherwise specified.

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial or model number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ABBREVIATIONS AND SYMBOLS

For an explanation of the abbreviations and symbols used in this section, please refer to the page immediately preceding the Electrical Parts List in this instruction manual.

INDEX OF MECHANICAL PARTS ILLUSTRATIONS

SECTION 11

MECHANICAL PARTS LIST

FIG. 1 FRONT

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty	1 2 3 4 5	Description
1-1	333-0972-01			1		PANEL, front
-2	386-1172-00			1		PLATE, sub-panel, front
-3	366-0215-01			17		KNOB, charcoal, LEVER
-4	260-0473-00			1		SWITCH, lever—MEASUREMENT AVERAGING 8—1
	- - - - - -			-		mounting hardware: (not included w/switch)
	220-0413-00			2		NUT, hex., 4-40 x 3/16 x 0.562 inch long
-5	260-0846-00			1		SWITCH, lever—REF ZONES
	- - - - - -			-		mounting hardware: (not included w/switch)
	220-0413-00			2		NUT, hex., 4-40 x 3/16 x 0.562 inch long
-6	260-0473-00			1		SWITCH, lever—TIME MEASUREMENT
	- - - - - -			-		mounting hardware: (not included w/switch)
	220-0413-00			2		NUT, hex., 4-40 x 3/16 x 0.562 inch long
-7	260-0847-00			1		SWITCH, lever—MEASUREMENT MODE
	- - - - - -			-		mounting hardware: (not included w/switch)
	220-0413-00			2		NUT, hex., 4-40 x 3/16 x 0.562 inch long
-8	260-0849-00			1		SWITCH, lever, CH A 0% level
	- - - - - -			-		mounting hardware: (not included w/switch)
	220-0413-00			2		NUT, hex., 4-40 x 3/16 x 0.562 inch long
-9	260-0849-00			1		SWITCH, lever, CH A 100% level
	- - - - - -			-		mounting hardware: (not included w/switch)
	220-0413-00			2		NUT, hex., 4-40 x 3/16 x 0.562 inch long
-10	260-0473-00			1		SWITCH, lever—CHANNEL AB (start point)
	- - - - - -			-		mounting hardware: (not included w/switch)
	220-0413-00			2		NUT, hex., 4-40 x 3/16 x 0.562 inch long
-11	260-0848-00			1		SWITCH, lever—% BETWEEN ZONES (start point)
	- - - - - -			-		mounting hardware: (not included w/switch)
	220-0413-00			2		NUT, hex., 4-40 x 3/16 x 0.562 inch long
-12	260-0849-00			1		SWITCH, lever—CH B 0% level
	- - - - - -			-		mounting hardware: (not included w/switch)
	220-0413-00			2		NUT, hex., 4-40 x 3/16 x 0.562 inch long

FIG. 1 FRONT *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description
1-13	260-0849-00			1	SWITCH, lever, CH B 100% level
	- - - - - -			-	mounting hardware: (not included w/switch)
	220-0413-00			2	NUT, hex., 4-40 x 3/16 x 0.562 inch long
-14	260-0473-00			1	SWITCH, lever—CHANNEL AB (stop point)
	- - - - - -			-	mounting hardware: (not included w/switch)
	220-0413-00			2	NUT, hex., 4-40 x 3/16 x 0.562 inch long
-15	260-0849-00			1	SWITCH, lever—% BETWEEN ZONES (stop point)
	- - - - - -			-	mounting hardware: (not included w/switch)
	220-0413-00			2	NUT, hex., 4-40 x 3/16 x 0.562 inch long
-16	260-0473-00			1	SWITCH, lever—SLOPE + — (start point)
	- - - - - -			-	mounting hardware: (not included w/switch)
	220-0413-00			2	NUT, hex., 4-40 x 3/16 x 0.562 inch long
-17	260-0473-00			1	SWITCH, lever—SLOPE 1st 2nd (start point)
	- - - - - -			-	mounting hardware: (not included w/switch)
	220-0413-00			2	NUT, hex., 4-40 x 3/16 x 0.562 inch long
-18	260-0473-00			1	SWITCH, lever—SLOPE + — (stop point)
	- - - - - -			-	mounting hardware: (not included w/switch)
	220-0413-00			2	NUT, hex., 4-40 x 3/16 x 0.562 inch long
-19	260-0473-00			1	SWITCH, lever—SLOPE 1st 2nd (stop point)
	- - - - - -			-	mounting hardware: (not included w/switch)
	220-0413-00			2	NUT, hex., 4-40 x 3/16 x 0.562 inch long
-20	260-0473-00			1	SWITCH, lever—TRIGGERED MEASUREMENT
	- - - - - -			-	mounting hardware: (not included w/switch)
	220-0413-00			2	NUT, hex., 4-40 x 3/16 x 0.562 inch long
-21	- - - - - -			5	ASSEMBLY, bulb
	- - - - - -			-	mounting hardware for each: (not included w/assembly)
-22	210-0012-00			1	LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
-23	210-0590-00			1	NUT, hex., 3/8-32 x 7/16 inch
-24	260-0834-00			1	SWITCH, toggle—POWER
	- - - - - -			-	mounting hardware: (not included w/switch)
-25	210-0562-00			2	NUT, hex., 1/4-40 x 5/16 inch
-26	210-0046-00			1	LOCKWASHER, internal, 0.261 ID x 0.400 inch OD
-27	210-0940-00			1	WASHER, flat, 1/4 ID x 3/8 inch OD

FIG. 1 FRONT *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
1-28	343-0006-00			1		CLAMP, cable, plastic, 1/2 inch
	- - - - - -			-		mounting hardware: (not included w/clamp)
-29	212-0023-00			1		SCREW, 8-32 x 3/8 inch, PHS
-30	210-0863-00			1		WASHER, "D" type
-31	210-0458-00			1		NUT, keps, 8-32 x 11/32 inch
-32	406-0757-00			4		BRACKET, spacer, switch
-33	426-0351-00			1		FRAME, readout
	- - - - - -			-		mounting hardware: (not included w/frame)
-34	210-0586-00			6		NUT, keps, 4-40 x 1/4 inch
-35	378-0579-00			1		FILTER, light, chromatic
-36	380-0117-00			1		HOUSING, readout
	- - - - - -			-		mounting hardware: (not included w/housing)
-37	210-0406-00			4		NUT, hex., 4-40 x 1/4 inch
-38	210-0586-00			4		NUT, keps, 4-40 x 1/4 inch
-39	352-0084-00			5		HOLDER, plastic, neon single
-40	378-0541-00			5		FILTER, lens, clear
-41	200-0643-00			5		COVER, plastic neon holder
-42	670-0239-00			1		ASSEMBLY, circuit board—COUNTER
	- - - - - -			-		assembly includes:
	388-0834-00			1		BOARD, circuit
-43	214-0506-00			66		PIN, connector, straight, male
	214-0579-00			1		PIN, test point
-44	136-0260-00			4		SOCKET, 16 pin
-45	136-0183-00			1		SOCKET, 3 pin
-46	136-0220-00			29		SOCKET, 3 pin
-47	136-0237-00			44		SOCKET, 8 pin
-48	136-0241-00			4		SOCKET, 10 pin
-49	136-0250-00			5		SOCKET, 13 pin
-50	136-0251-00			1		SOCKET, 14 pin
	- - - - - -			-		mounting hardware: (not included w/socket)
-51	211-0534-00			2		SCREW, sems, 6-32 x 5/16 inch, PHS
-52	385-0100-00			2		ROD, plastic, 5/16 x 1/2 inch
-53	211-0558-00			2		SCREW, plastic, 6-32 x 1/4 inch
-54	260-0723-00			1		SWITCH, slide
-55	343-0043-00			1		CLAMP, neon
	- - - - - -			-		mounting hardware: (not included w/assembly)
-56	129-0114-00			6		POST, hex., 1/4 x 1 5/8 inches
-57	211-0116-00			6		SCREW, sems, 4-40 x 5/16 inch
-58	386-1218-00			1		PLATE, support
	- - - - - -			-		mounting hardware: (not included w/plate)
-59	210-0457-00			6		NUT, keps, 6-32 x 5/16 inch

FIG. 1 FRONT *(cont)*

Fig. & Index No.	Part No. Tektronix	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
1-60	214-0905-00			1		RETAINER, circuit board
	- - - - - -			-		mounting hardware: (not included w/retainer)
-61	212-0023-00			2		SCREW, 8-32 x 3/8 inch, PHS
-62	210-0804-00			2		WASHER, flat, 0.170 ID x 3/8 inch OD
-63	210-0458-00			2		NUT, keps, 8-32 x 11/32 inch
-64	348-0102-00			1		PAD, cushioning, 14 inches long
-65	214-0553-00			2		LATCH SCREW, 1.388 inches long
-66	358-0255-00			2		BUSHING, plastic, latch
-67	366-0149-00			1		KNOB, charcoal—CH A 0%—100%
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-68	366-0142-00			1		KNOB, charcoal—CH A POSITION
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-69	260-0846-00			1		SWITCH, unwired—CH A POSITION
	- - - - - -			-		mounting hardware: (not included w/switch)
-70	210-0012-00			1		LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
-71	210-0840-00			1		WASHER, flat, 0.390 ID x 1/2 inch OD
-72	210-0413-00			1		NUT, hex., 3/8-32 x 1/2 inch
-73	366-0149-00			1		KNOB, charcoal—CH B 0%—100%
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-74	366-0142-00			1		KNOB, charcoal, CH B POSITION
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-75	260-0846-00			1		SWITCH, unwired—CH B POSITION
	- - - - - -			-		mounting hardware: (not included w/switch)
	210-0012-00			1		LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
-76	210-0840-00			1		WASHER, flat, 0.390 ID x 1/2 inch OD
-77	210-0413-00			1		NUT, hex., 3/8-32 x 1/2 inch
-78	366-0167-03			1		KNOB, charcoal—START POINT
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-79	366-0164-02			1		KNOB, charcoal—START POINT
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-80	260-0844-00			1		SWITCH, unwired—START POINT
	- - - - - -			-		mounting hardware: (not included w/switch)
-81	210-0413-00			1		NUT, hex., 3/8-32 x 1/2 inch
-82	366-0167-03			1		KNOB, charcoal—STOP POINT
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-83	366-0164-02			1		KNOB, charcoal—STOP POINT
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS

FIG. 1 FRONT *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
1-84	260-0844-00			1		SWITCH, unwired—STOP POINT
	- - - - - -			-		mounting hardware: (not included w/switch)
-85	210-0413-00			1		NUT, hex., $^3/_8$-32 x $^1/_2$ inch
-86	366-0167-02			1		KNOB, charcoal—UPPER LIMIT (left)
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x $^3/_{16}$ inch, HSS
-87	366-0164-01			1		KNOB, charcoal—UPPER LIMIT (left)
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x $^3/_{16}$ inch, HSS
-88	262-0807-00			1		SWITCH, wired—UNITS/TENS
	- - - - - -			-		switch includes:
	260-0844-00			1		SWITCH, unwired
	- - - - - -			-		mounting hardware: (not included w/switch)
	210-0413-00			1		NUT, hex., $^3/_8$-32 x $^1/_2$ inch
-89	366-0167-03			1		KNOB, charcoal—UPPER LIMIT (right)
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x $^3/_{16}$ inch, HSS
-90	366-0164-02			1		KNOB, charcoal—UPPER LIMIT (right)
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x $^3/_{16}$ inch, HSS
-91	262-0808-00			1		SWITCH, wired—HUNDREDS/THOUSANDS
	- - - - - -			-		switch includes:
	260-0845-00			1		SWITCH, unwired
	- - - - - -			-		mounting hardware: (not included w/switch)
	210-0413-00			1		NUT, hex., $^3/_8$-32 x $^1/_2$ inch
-92	366-0167-03			1		KNOB, charcoal—LOWER LIMIT (right)
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x $^3/_{16}$ inch, HSS
-93	366-0164-02			1		KNOB, charcoal—LOWER LIMIT (right)
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x $^3/_{16}$ inch, HSS
-94	262-0808-00			1		SWITCH, wired—HUNDREDS/THOUSANDS
	- - - - - -			-		switch includes:
	260-0845-00			1		SWITCH, unwired
	- - - - - -			-		mounting hardware: (not included w/switch)
	210-0413-00			1		NUT, hex., $^3/_8$-32 x $^1/_2$ inch

FIG. 1 FRONT *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description
1-95	366-0167-02			1	KNOB, charcoal—LOWER LIMIT (left)
	- - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set, 6-32 x 3/16 inch, HSS
-96	366-0164-01			1	KNOB, charcoal—LOWER LIMIT (left)
	- - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set, 6-32 x 3/16 inch, HSS
-97	262-0807-00			1	SWITCH, wired—UNITS/TENS
	- - - - - -			-	switch includes:
	260-0844-00			1	SWITCH, unwired
	- - - - - -			-	mounting hardware: (not included w/switch)
	210-0413-00			1	NUT, hex., 3/8-32 x 1/2 inch
-98	366-0113-00			1	KNOB, charcoal—DISPLAY TIME
	- - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set, 6-32 x 3/16 inch, HSS
-99	- - - - - -			1	RESISTOR, variable
	- - - - - -			-	mounting hardware: (not included w/resistor)
-100	210-0207-00			1	LUG, solder, 3/8 ID x 5/8 inch OD, SE
-101	210-0012-00			1	LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
-102	210-0840-00			1	WASHER, flat, 0.390 ID x 1/2 inch OD
-103	210-0413-00			1	NUT, hex., 3/8-32 x 1/2 inch
-104	200-0368-01			4	FRAME, knob window (dual)
	- - - - - -			-	mounting hardware for each: (not included w/frame)
-105	211-0541-00			1	SCREW, 6-32 x 1/4 inch, FHS
-106	426-0360-01			2	FRAME, knob window (single)
	- - - - - -			-	mounting hardware for each: (not included w/frame)
-107	211-0541-00			2	SCREW, 6-32 x 1/4 inch, FHS
-108	179-1189-00			1	CABLE HARNESS, readout
	- - - - - -			-	cable harness includes:
	131-0371-00			6	CONNECTOR, single contact, female
-109	179-1182-00			1	CABLE HARNESS, sub-panel
	- - - - - -			-	cable harness includes:
	131-0371-00			61	CONNECTOR, single contact, female

FIG. 2 FRONT FRAME PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty 1 2 3 4 5	Description
2-1	426-0343-00			1	FRAME, section, digital unit, bottom
-2	426-0344-00			1	FRAME, section, digital unit, top
-3	407-0296-03			1	BRACKET, angle, right (Type R230 only)
	- - - - - -			-	mounting hardware: (not included w/bracket)
-4	212-0574-00			2	SCREW, 10-32 x 0.434 inch FHS (Type R230 only)
-5	407-0296-00			1	BRACKET, angle, left (Type R230 only)
	- - - - - -			-	mounting hardware: (not included w/bracket)
-6	212-0574-00			2	SCREW, 10-32 x 0.434 inch FHS (Type R230 only)
-7	367-0076-00			2	HANDLE (Type R230 only)
	- - - - - -			-	mounting hardware for each: (not included w/handle)
-8	212-0562-00			2	SCREW, 10-32 x 7/8 inch FHS (Type R230 only)
-9	426-0326-01			1	FRAME, section, right front & left rear
	- - - - - -			-	mounting hardware: (not included w/frame)
-10	212-0574-00			2	SCREW, 10-32 x 0.434 inch, FHS
-11	124-0188-00			1	STRIP, trim, 16.3 x 0.876 inch (Type R230 only)
-12	367-0073-00	B010100	B159999	1	HANDLE (Type 230 only)
	367-0073-01	B160000		1	HANDLE (Type 230 only)
	- - - - - -			-	mounting hardware: (not included w/handle)
-13	213-0155-00			2	SCREW, 10-32 x 0.40 inch (Type 230 only)
-14	386-1176-00	B010100	B039999	2	PLATE, (Type 230 only)
	386-1352-00	B040000		2	PLATE, (Type 230 only)
-15	200-0728-00			1	COVER, handle end
-16	426-0325-01			1	FRAME, section, left front & right rear
	- - - - - -			-	mounting hardware: (not included w/frame)
-17	212-0574-00			2	SCREW, 10-32 x 0.434 inch, FHS
-18	377-0151-00			1	INSERT, corner frame section
	- - - - - -			-	mounting hardware: (not included w/frame)
-19	212-0518-00			2	SCREW, 10-32 x 5/16 inch, BHS
-20	124-0189-00			2	STRIP, trim, 0.995 x 6.45 inches (Type 230 only)
-21	214-0866-00			1	HINGE, outer half
	- - - - - -			-	mounting hardware: (not included w/hinge)
-22	212-0518-00			2	SCREW, 10-32 x 5/16 inch, BHS
-23	214-0865-00			1	HINGE, inner half
	- - - - - -			-	mounting hardware: (not included w/hinge)
-24	214-0864-00			2	PIN, hinge
	213-0159-00			2	SCREW, 3-48 x 1/8 inch, PHS

FIG. 2 FRONT FRAME PARTS *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description (1 2 3 4 5)
2-25	214-0925-00			1	SUPPORT, arm, door
	- - - - - -			-	mounting hardware: (not included w/support)
-26	211-0025-00	B010100	B030279	1	SCREW, 4-40 x 3/8 inch, FHS
	211-0102-00	B030280		1	SCREW, 4-40 x 1/2 inch, 100° csk, FHS
-27	361-0158-00			1	SPACER, sleeve
	210-0054-00	B010100	B030279X	1	LOCKWASHER, split, #4
	210-0851-00			1	WASHER, flat, 0.119 ID x 3/8 OD
	210-0948-00			1	WASHER, plastic
-28	210-0405-00	B010100	B030279	1	NUT, hex., 4-40 x 3/16 inch
	210-0589-00	B030280		1	NUT, locking, 4-40 x 1/4 inch
-29	214-0926-00			1	SUPPORT, arm, door
	- - - - - -			-	mounting hardware: (not included w/support)
-30	361-0158-00			1	SPACER, sleeve
	210-0054-00	B010100	B030279X	1	LOCKWASHER, split, #4
	210-0851-00			1	WASHER, flat, 0.119 ID x 3/8 OD
	210-0948-00			1	WASHER, plastic
-31	210-0405-00	B010100	B030279	1	NUT, hex., 4-40 x 3/16 inch
	210-0589-00	B030280		1	NUT, locking, 4-40 x 1/4 inch
-32	407-0373-00			1	BRACKET, angle, door stop
	- - - - - -			-	mounting hardware: (not included w/bracket)
-33	361-0158-00			1	SPACER, sleeve
	210-0054-00			1	LOCKWASHER, split, #4
	210-0851-00			1	WASHER, flat, 0.119 ID x 3/8 OD
	210-0948-00			1	WASHER, plastic
-34	210-0405-00	B010100	B030279	1	NUT, hex., 4-40 x 3/16 inch
	210-0589-00	B030280		1	NUT, locking, 4-40 x 1/4 inch
	210-0457-00			1	NUT, keps, 6-32 x 5/16 inch (not shown)
-35	348-0096-01			1	FOOT, cabinet, right front (Type 230 only)
	- - - - - -			-	mounting hardware: (not included w/foot)
-36	212-0541-00			1	SCREW, 10-32 x 5/8 inch, RHS (Type 230 only)
-37	348-0098-01			1	FOOT, cabinet, left front (Type 230 only)
	- - - - - -			-	mounting hardware: (not included w/foot)
-38	212-0541-00			1	SCREW, 10-32 x 5/8 inch, RHS (Type 230 only)
-39	348-0097-00			2	PAD, cabinet foot (Type 230 only)
-40	348-0095-01			1	FLIPSTAND, cabinet (Type 230 only)
-41	214-0846-01			1	RETAINER, flipstand, (Type 230 only)
	- - - - - -			-	mounting hardware: (not included w/retainer)
-42	212-0509-00			1	SCREW, 10-32 x 5/8 inch (Type 230 only)
-43	210-0202-00			1	LUG, solder, SE #6
	- - - - - -			-	mounting hardware: (not included w/lug)
	210-0457-00			1	NUT, keps, 6-32 x 5/16 inch

FIG. 3 CIRCUIT CARD SUPPORTS, BULKHEAD & POWER CHASSIS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
3-1	407-0319-00			1		BRACKET, circuit card guide
	- - - - - -			-		mounting hardware: (not included w/bracket)
	212-0040-00			2		SCREW, 8-32 x 3/8 inch, FHS
-2	210-0458-00			2		NUT, keps, 8-32 x 11/32 inch
-3	386-1219-00			1		SUPPORT, bracket
	- - - - - -			-		mounting hardware: (not included w/support)
-4	212-0023-00			4		SCREW, 8-32 x 3/8 inch, PHS
-5	210-0458-00			4		NUT, keps, 8-32 x 11/32 inch
	211-0538-00			1		SCREW, 6-32 x 5/16 inch, FHS
-6	210-0457-00			1		NUT, keps, 6-32 x 5/16 inch
-7	386-1173-00			1		SUPPORT, bracket
	- - - - - -			-		mounting hardware: (not included w/support)
-8	212-0023-00			4		SCREW, 8-32 x 3/8 inch, PHS
-9	210-0458-00			4		NUT, keps, 8-32 x 11/32 inch
	211-0538-00			1		SCREW, 6-32 x 5/16 inch, FHS
-10	210-0457-00			1		NUT, keps, 6-32 x 5/16 inch
-11	407-0318-00			1		BRACKET, circuit card guide
	- - - - - -			-		mounting hardware: (not included w/bracket)
	212-0040-00			2		SCREW, 8-32 x 3/8 inch, FHS
-12	210-0458-00			2		NUT, keps, 8-32 x 11/32 inch
-13	351-0113-00			24		GUIDE, plastic, circuit card
-14	441-0710-00			1		CHASSIS, bulkhead
	- - - - - -			-		mounting hardware: (not included w/chassis)
-15	212-0040-00			4		SCREW, 8-32 x 3/8 inch, PHS
-16	210-0458-00			4		NUT, keps, 8-32 x 11/32 inch
	212-0574-00			2		SCREW, 10-32 x 0.434 inch, FHS
-17	220-0410-00			2		NUT, keps, 10-32 x 3/8 inch
-18	214-0210-00			1		ASSEMBLY, solder spool
	- - - - - -			-		assembly includes:
	214-0209-00			1		SPOOL, w/o solder
	- - - - - -			-		mounting hardware: (not included w/assembly)
-19	361-0007-00			1		SPACER, plastic, 0.188 inch long
-20	131-0292-01	B010100	B050339	11		CONNECTOR, 56 pin, female
	131-0549-00	B050340		11		CONNECTOR, 56 pin, female
	- - - - - -			-		mounting hardware for each: (not included w/connector)
-21	211-0014-00	B010100	B050339	2		SCREW, 4-40 x 1/2 inch, PHS
-22	210-0586-00	B010100	B050399	2		NUT, keps, 4-40 x 1/4 inch
	211-0097-00	B050340		2		SCREW, 4-40 x 5/16 inch, PHS
-23	214-0702-00			22		KEY, plastic, polarized
-24	352-0124-00			1		HOLDER, circuit card extender
	- - - - - -			-		mounting hardware: (not included w/holder)
-25	210-0457-00			2		NUT, keps, 6-32 x 5/16 inch

FIG. 3 CIRCUIT CARD SUPPORTS, BULKHEAD & POWER CHASSIS *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
3-26	426-0349-00			2		FRAME, section, left & right
	- - - - - -			-		mounting hardware for each: (not included w/frame)
	212-0574-00			2		SCREW, 10-32 x 0.434 inch, FHS
-27	358-0166-00			1		BUSHING, plastic
-28	441-0711-00			1		CHASSIS, power
	- - - - - -			-		mounting hardware: (not included w/chassis)
	212-0585-00			4		SCREW, 10-32 x 1/2 inch, OHS
	220-0410-00			4		NUT, keps, 10-32 x 3/8 inch
	212-0023-00			4		SCREW, 8-32 x 3/8 inch, PHS
	210-0458-00			4		NUT, keps, 8-32 x 11/32 inch
-29	348-0063-00			1		GROMMET, plastic, 1/2 inch diameter
-30	- - - - - -			1		THERMAL CUTOUT
	- - - - - -			-		mounting hardware: (not included w/thermal cutout)
-31	213-0044-00			2		SCREW, thread forming, 5-32 x 3/16 inch, PHS
-32	210-0201-00			4		LUG, solder, SE #4
	- - - - - -			-		mounting hardware for each: (not included w/lug)
-33	213-0044-00			1		SCREW, thread forming, 5-32 x 3/16 inch, PHS
-34	- - - - - -			1		TRANSFORMER
	- - - - - -			-		mounting hardware: (not included w/transformer)
-35	212-0516-00			4		SCREW, 10-32 x 2 inches, HHS
-36	210-0812-00			4		WASHER, fiber, 0.19 x 0.38 inch OD
-37	220-0410-00			4		NUT, keps, 10-32 x 3/8 inch
-38	- - - - - -			6		TRANSISTOR
	- - - - - -			-		mounting hardware for each: (not included w/transistor)
-39	211-0511-00			2		SCREW, 6-32 x 1/2 inch, PHS
-40	386-0978-00			1		PLATE, mica, insulating
-41	210-0935-00			2		WASHER, fiber, shouldered
-42	210-0803-00			2		WASHER, flat, 0.150 ID x 3/8 inch OD
-43	210-0202-00			1		LUG, solder, SE #6
-44	210-0457-00			2		NUT, keps, 6-32 x 5/16 inch
-45	- - - - - -			2		CAPACITOR
	- - - - - -			-		mounting hardware for each: (not included w/capacitor)
-46	211-0588-00			2		SCREW, 6-32 x 3/4 inch, HHS
-47	432-0048-00			1		BASE, plastic, large capacitor mounting
-48	386-0254-00			1		PLATE, fiber, large capacitor mounting
-49	210-0457-00			2		NUT, keps, 6-32 x 5/16 inch

FIG. 3 CIRCUIT CARD SUPPORTS, BULKHEAD & POWER CHASSIS *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
3-50	200-0293-00			3		COVER, plastic, 1.365 ID x 2 9/16 inches long
-51	- - - - - -			2		CAPACITOR
	- - - - - -			-		mounting hardware for each: (not included w/capacitor)
-52	211-0588-00			2		SCREW, 6-32 x 3/4 inch, HHS
-53	432-0047-00			1		BASE, plastic, small capacitor mounting
-54	386-0252-00			1		PLATE, fiber small capacitor mounting
-55	210-0457-00			2		NUT, keps, 6-32 x 5/16 inch
-56	200-0256-00			2		COVER, plastic, 1 ID x 2 1/32 inches long
-57	- - - - - -			1		CAPACITOR
	- - - - - -			-		mounting hardware: (not included w/capacitor)
-58	211-0516-00			2		SCREW, 6-32 x 7/8 inch, PHS
-59	432-0048-00			1		BASE, plastic, large capacitor mounting
-60	386-0254-00			1		PLATE, fiber, large capacitor mounting
-61	210-0457-00			2		NUT, keps, 6-32 x 5/16 inch
-62	- - - - - -			1		CAPACITOR
	- - - - - -			-		mounting hardware: (not included w/capacitor)
-63	211-0534-00			2		SCREW, sems, 6-32 x 5/16 inch, PHS
-64	386-0252-00			1		PLATE, fiber, small capacitor mounting
-65	210-0457-00			2		NUT, keps, 6-32 x 5/16 inch
-66	200-0257-00			1		COVER, plastic, 1 ID x 2 17/32 inches long
-67	124-0106-00			8		STRIP, ceramic, 7/16 inch h, w/11 notches
	- - - - - -			-		each strip includes:
	355-0046-00			2		STUD, plastic
	- - - - - -			-		mounting hardware for each: (not included w/strip)
	361-0008-00			2		SPACER, plastic, 0.281 inch long
-68	124-0092-00			1		STRIP, ceramic, 7/16 inch h, w/3 notches
	- - - - - -			-		strip includes:
	355-0046-00			1		STUD, plastic
	- - - - - -			-		mounting hardware: (not included w/strip)
	361-0008-00			1		SPACER, plastic, 0.281 inch long
-69	124-0147-00			2		STRIP, ceramic, 7/16 inch h, w/13 notches
	- - - - - -			-		each strip includes:
	355-0046-00			2		STUD, plastic
	- - - - - -			-		mounting hardware for each: (not included w/strip)
	361-0008-00			2		SPACER, plastic, 0.281 inch long
-70	179-1185-00			1		CABLE HARNESS, interconnector
-71	179-1184-00			1		CABLE HARNESS, power
-72	124-0119-00			2		STRIP, ceramic, 7/16 inch h, w/2 notches
	- - - - - -			-		each strip includes:
	355-0046-00			1		STUD, plastic
	- - - - - -			-		mounting hardware for each: (not included w/strip)
	361-0009-00			1		SPACER, plastic, 0.406 inch long

FIG. 4 CIRCUIT CARDS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description
4-1	670-0231-00			2	ASSEMBLY, circuit card—ZONE GENERATOR (CH A & B)
	- - - - - -			-	each assembly includes:
	388-0826-00	B010100	B129999	1	CARD, circuit
	388-0826-01	B130000		1	CARD, circuit
-2	136-0220-00			34	SOCKET, transistor, 3 pin
-3	136-0241-00			2	SOCKET, transistor, 10 pin
-4	352-0120-00			1	HOLDER, variable resistor, black
-5	352-0112-00			1	HOLDER, variable resistor, white
-6	352-0119-00			1	HOLDER, variable resistor, brown
-7	352-0117-00			1	HOLDER, variable resistor, orange
-8	670-0232-00			2	ASSEMBLY, circuit card—MEMORY (CH A & B)
	- - - - - -			-	each assembly includes:
	388-0827-00			1	CARD, circuit
-9	131-0344-00			4	CONNECTOR, terminal feed thru
	- - - - - -			-	mounting hardware for each: (not included w/connector)
-10	358-0136-00			1	BUSHING, plastic
-11	136-0220-00			25	SOCKET, transistor, 3 pin
-12	136-0237-00			2	SOCKET, transistor, 8 pin
-13	136-0241-00			12	SOCKET, transistor, 10 pin
-14	136-0257-00			2	SOCKET, transistor, 4 pin
-15	352-0120-00			1	HOLDER, variable resistor, black
-16	352-0119-00			1	HOLDER, variable resistor, brown
-17	670-0233-00			1	ASSEMBLY, circuit card—BUFFER
	- - - - - -			-	assembly includes:
	388-0828-00	B010100	B059999	1	CARD, circuit
	388-0828-01	B060000		1	CARD, circuit
	260-0984-00	XB060000		1	SWITCH, slide
-18	136-0220-00			15	SOCKET, transistor, 3 pin
-19	136-0183-00	B010100	B059999	2	SOCKET, transistor, 3 pin
	136-0220-00	B060000		3	SOCKET, transistor, 3 pin
-20	136-0237-00			1	SOCKET, transistor, 8 pin
-21	136-0241-00			3	SOCKET, transistor, 10 pin
-22	352-0119-00			1	HOLDER, variable resistor, brown
-23	352-0114-00			1	HOLDER, variable resistor, red
-24	352-0116-00			1	HOLDER, variable resistor, green
-25	352-0113-00			1	HOLDER, variable resistor, grey
-26	352-0115-00			1	HOLDER, variable resistor, violet

FIG. 4 CIRCUIT CARDS *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty 1 2 3 4 5	Description
4-27	670-0234-00			2	ASSEMBLY, circuit card—COMPARATOR (CH A & B)
	- - - - - -			-	each assembly includes:
	388-0829-00			1	CARD, circuit
	260-0877-00	B010100	B049999	25	SWITCH, reed
	260-0877-01	B050000		25	SWITCH, reed
	214-0579-00			5	CONNECTOR, test point
-28	136-0220-00			28	SOCKET, transistor, 3 pin
-29	136-0235-00			2	SOCKET, transistor, 6 pin
-30	136-0237-00			1	SOCKET, transistor, 8 pin
-31	136-0183-00			2	SOCKET, transistor, 3 pin
-32	131-0505-00			26	CONNECTOR, terminal stud
-33	131-0525-00			24	TERMINAL, stud, w/half loop
-34	352-0119-00			1	HOLDER, variable resistor, brown
-35	352-0121-00			1	HOLDER, variable resistor, yellow
-36	352-0116-00			1	HOLDER, variable resistor, green
-37	352-0017-00			1	HOLDER, variable resistor, orange
-38	352-0114-00			1	HOLDER, variable resistor, red
-39	352-0118-00			1	HOLDER, variable resistor, blue
-40	260-0723-00			1	SWITCH, slide—CALIBRATE—RUN
-41	670-0235-00			1	ASSEMBLY, circuit card—CLOCK
	- - - - - -			-	assembly includes:
	388-0830-00	B010100	B089999	1	CARD, circuit
	388-0831-01	B090000		1	CARD, circuit
-42	136-0220-00			12	SOCKET, transistor, 3 pin
-43	136-0237-00			2	SOCKET, transistor, 8 pin
-44	136-0241-00			31	SOCKET, transistor, 10 pin
-45	670-0236-00			1	ASSEMBLY, circuit card—SYNCHRONIZER
	- - - - - -			-	assembly includes:
	388-0831-00			1	CARD, circuit
-46	136-0220-00			19	SOCKET, transistor, 3 pin
-47	136-0237-00			21	SOCKET, transistor, 8 pin
-48	214-0579-00			1	CONNECTOR, test point
-49	352-0112-00			1	HOLDER, variable resistor, white

FIG. 5 CIRCUIT CARDS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5 Description
5-1	670-0237-00			1	ASSEMBLY, circuit card—INTENSIFICATION REGULATOR
	- - - - - -			-	assembly includes:
	388-0832-00	B010100	B099999	1	CARD, circuit
	388-0832-01	B100000		1	CARD, circuit
-2	136-0220-00			30	SOCKET, transistor, 3 pin
-3	136-0183-00			4	SOCKET, transistor, 3 pin
-4	136-0235-00			6	SOCKET, transistor, 6 pin
-5	352-0116-00			1	HOLDER, variable resistor, green
-6	352-0119-00			1	HOLDER, variable resistor, brown
-7	352-0117-00			1	HOLDER, variable resistor, orange
-8	352-0121-00			1	HOLDER, variable resistor, yellow
-9	352-0118-00			1	HOLDER, variable resistor, blue
-10	352-0114-00			1	HOLDER, variable resistor, red
-11	214-0579-00			7	PIN, test point
-12	670-0238-00			1	ASSEMBLY, circuit card—LIMIT
	- - - - - -			-	assembly includes:
	388-0833-00	B010100	B049999	1	CARD, circuit
	388-0833-01	B050000		1	CARD, circuit
-13	136-0220-00			70	SOCKET, transistor, 3 pin
-14	670-0240-00			1	ASSEMBLY, circuit card—FRONT EXTENDER
	- - - - - -			-	assembly includes:
	388-0824-00			1	CARD, circuit
-15	214-0579-00			56	PIN, test point
-16	131-0292-01			1	CONNECTOR, female, 56 pin
-17	344-0141-00			1	CLIP, circuit card retainer
	- - - - - -			-	mounting hardware: (not included w/clip)
	211-0012-00			1	SCREW, 4-40 x 3/8 inch, PHS
-18	210-0586-00			1	NUT, keps, 4-40 x 1/4 inch
	214-0702-00			1	KEY, plastic, polarized
-19	670-0241-00			1	ASSEMBLY, circuit card—REAR EXTENDER
	- - - - - -			-	assembly includes:
	388-0825-00			1	CARD, circuit
-20	134-0066-00			2	PLUG, banana, male
	- - - - - -				mounting hardware for each: (not included w/plug)
	211-0108-00			1	SCREW, 2-56 x 5/32 inch, RHS
	210-0850-00			1	WASHER, flat, 0.093 ID x 0.281 inch OD
	210-0053-00			1	LOCKWASHER, split, #2
-21	131-0292-01			1	CONNECTOR, female, 56 pin
-22	344-0141-00			2	CLIP, circuit card retainer
	- - - - - -			-	mounting hardware for each: (not included w/clip)
	211-0012-00			1	SCREW, 4-40 x 3/8 inch, PHS
-23	210-0586-00			1	NUT, keps, 4-40 x 1/4 inch

FIG. 6 REAR

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Qty 1 2 3 4 5	Description
6-1	386-1171-00			1	PANEL, rear
	- - - - - -			-	mounting hardware: (not included w/panel)
-2	211-0510-00			10	SCREW, 6-32 x 3/8 inch, PHS
-3	212-0507-00			4	SCREW, 10-32 x 3/8 inch, BHS
-4	210-0457-00			10	NUT, keps, 6-32 x 5/16 inch
-5	200-0728-00			2	COVER, handle end (Type 230 only)
-6	204-0279-00			1	ASSEMBLY, line voltage selector
	- - - - - -			-	mounting hardware: (not included w/assembly)
-7	210-0006-00			2	LOCKWASHER, internal, #6
-8	210-0407-00			2	NUT, hex., 6-32 x 1/4 inch
-9	200-0762-00			1	COVER, line voltage selector
	- - - - - -			-	cover includes
-10	352-0102-00			2	HOLDER, fuse
	- - - - - -			-	mounting hardware for each: (not included w/holder)
-11	213-0088-00			1	SCREW, thread cutting, 4-40 x 1/4 inch
-12	124-0188-00			1	STRIP, trim, 16.3 x 0.876 inch (Type 230 only)
-13	124-0201-00			2	STRIP, trim, 6.45 x 1.009 inches
-14	426-0325-01			1	FRAME, section, left rear
	- - - - - -			-	mounting hardware: (not included w/frame)
-15	212-0574-00			2	SCREW, 10-32 x 0.434 inch, FHS
-16	426-0326-01			1	FRAME, section, left rear
	- - - - - -			-	mounting hardware: (not included w/frame)
-17	212-0574-00			2	SCREW, 10-32 x 0.434 inch, FHS
-18	426-0330-00			1	FRAME, section, rear top
-19	367-0073-00			1	HANDLE (Type 230 only)
	- - - - - -			-	mounting hardware: (not included w/handle)
-20	213-0155-00			2	SCREW, 10-32 x 0.40 inch (Type 230 only)
-21	386-1176-00	B010100	B039999	2	PLATE, (Type 230 only)
	386-1352-00	B040000		2	PLATE, (Type 230 only)
-22	630-0217-00	B010100	B059999	1	ASSEMBLY, connector
	630-0217-01	B060000		1	ASSEMBLY, connector
	- - - - - -			-	assembly includes:
-23	179-1187-00			1	CABLE HARNESS, external programming
-24	179-1188-00	B010100	B059999	1	CABLE HARNESS, external programming
	179-1188-01	B060000		1	CABLE HARNESS, external programming
-25	386-1245-00			1	PLATE, connector mounting
-26	131-0294-00			2	CONNECTOR, 36 contact, female
	- - - - - -			-	mounting hardware for each: (not included w/connector)
-27	211-0062-00			2	SCREW, 2-56 x 5/16 inch, PHS
-28	210-0001-00			2	LOCKWASHER, internal, #2
-29	210-0405-00			2	NUT, hex., 2-56 x 3/16 inch
	- - - - - -			-	mounting hardware: (not included w/assembly)
-30	211-0507-00			3	SCREW, 6-32 x 5/16 inch, PHS

FIG. 6 REAR *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
6-31	630-0218-00			1		ASSEMBLY, connector
	- - - - - -			-		assembly includes:
-32	179-1186-00			1		CABLE HARNESS, external programming (main)
-33	386-1244-00			1		PLATE, connector mounting
-34	131-0294-00			4		CONNECTOR, 36 pin, female
	- - - - - -			-		mounting hardware for each: (not included w/connector)
-35	211-0062-00			2		SCREW, 2-56 x 5/16 inch, PHS
-36	210-0001-00			2		LOCKWASHER, internal, #2
-37	210-0405-00			2		NUT, hex., 2-56 x 3/16 inch
	- - - - - -			-		mounting hardware: (not included w/assembly)
-38	211-0510-00			4		SCREW, 6-32 x 3/8 inch, PHS
-39	119-0031-00			1		ASSEMBLY, blower
	- - - - - -			-		mounting hardware: (not includea w/assembly)
-40	211-0511-00			4		SCREW, 6-32 x 1/2 inch, PHS
-41	210-0457-00			4		NUT, keps, 6-32 x 5/16 inch
-42	426-0329-00			1		FRAME, section, bottom rear
-43	348-0078-00	B010100	B149999X	4		FOOT, plastic, cap
-44	348-0079-00	B010100	B149999	4		FOOT, plastic
	348-0191-00	B150000		4		FOOT, plastic
	- - - - - -			-		mounting hardware for each: (not included w/foot)
-45	212-0082-00			1		SCREW, 8-32 x 1 1/4 inches, PHS
-46	210-0458-00			1		NUT, keps, 8-32 x 11/32 inch
-47	348-0097-00			2		PAD, cabinet foot (Type 230 only)
-48	348-0096-01			1		FOOT, cabinet (Type 230 only)
	- - - - - -			-		mounting hardware: (not included w/foot)
-49	212-0541-00			1		SCREW, 10-32 x 5/8 inch, RHS (Type 230 only)
-50	348-0098-01			1		FOOT, cabinet (Type 230 only)
	- - - - - -			-		mounting hardware: (not included w/foot)
-51	212-0541-00			1		SCREW, 10-32 x 5/8 inch, RHS (Type 230 only)
-52	161-0033-00			1		CORD, power, 3 conductor
	343-0170-00	XB110490		1		RETAINER, cable to cable (not shown)
-53	358-0161-00			1		BUSHING, plastic, strain relief
-54	378-0029-00			1		FILTER, air, plastic foam
-55	380-0119-00			1		HOUSING, air filter
	- - - - - -			-		mounting hardware: (not included w/housing)
-56	211-0516-00			4		SCREW, 6-32 x 7/8 inch, PHS
-57	179-1190-00			1		CABLE HARNESS, line voltage selector

FIG. 7 CABINET & SIDE FRAMES

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty 1 2 3 4 5	Description
7-1	386-1139-00			1	CABINET, top
	- - - - - -			-	cabinet includes:
-2	214-0812-00			4	ASSEMBLY, latch
	- - - - - -			-	each assembly includes:
-3	214-0603-01			1	PIN, securing
-4	214-0604-00			1	SPRING
-5	386-0227-00			1	PLATE, plastic, index
-6	386-0226-00			1	PLATE, locking
-7	386-1138-00			1	CABINET, bottom
	- - - - - -			-	cabinet includes:
-8	214-0812-00			4	ASSEMBLY, latch
	- - - - - -			-	each assembly includes:
-9	214-0603-01			1	PIN, securing
-10	214-0604-00			1	SPRING
-11	386-0227-00			1	PLATE, plastic, index
-12	386-0226-00			1	PLATE, locking
-13	426-0347-00			1	FRAME, section, bottom left
	- - - - - -			-	mounting hardware: (not included w/frame)
-14	212-0574-00			2	SCREW, 10-32 x 0.434 inch, FHS
-15	212-0585-00			2	SCREW, 10-32 x 0.50 inch, FHS
	220-0410-00			1	NUT, keps, 10-32 x 3/8 inch
-16	426-0348-00			1	FRAME, section, bottom right
	- - - - - -			-	mounting hardware: (not included w/frame)
-17	212-0574-00			2	SCREW, 10-32 x 0.434 inch, FHS
-18	212-0585-00			2	SCREW, 10-32 x 0.50 inch, FHS
	220-0410-00			1	NUT, keps, 10-32 x 3/8 inch
-19	351-0027-00	B010100	B049999	1	TRACK, slideout (pair, Type R230 only)
	351-0082-00	B050000		1	TRACK, slideout (pair, Type R230 only)

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Sections of the manual are often printed at different times, so some of the information on the change pages may already be in your manual. Since the change information sheets are carried in the manual until ALL changes are permanently entered, some duplication may occur. If no such change pages appear in this section, your manual is correct as printed.

TEXT CORRECTION

Section 6 Performance Check

Page 6-1 EQUIPMENT REQUIRED

REPLACE: items 1, 2 and 3 with the following:

1. Type 568 oscilloscope with sampling and sampling sweep units, such as Type 3S5 (with two Sampling Heads) and Type 3T5.

2. Interconnecting cable, Tektronix Part Number 012-0119-01 (Included as standard accessory with the Type 230).

Page 6-1 Control Settings

ADD: the following controls after SLOPE:

TIME MEASUREMENT STOP POINT	
CHANNEL	A
LEVEL	HORIZ mm FROM SWP START
Offset dials	1 and 0

Page 6-2

REPLACE: the control settings in column 1 with the following:

Sampling Sweep Unit	
Samples/Sweep	1000
Time/Div	(100 ns)
Decade	7
Multiplier	1
Delay	1000
Program Selector	Int
Trigger	
Sensitivity	fully cw
Recovery Time	fully cw
Mode	+, Int
Horiz Pos	Centered
Sampling Unit	
Mode	Ch A
Channels A and B	
Units/Div	100
Cal/Variable	Cal
Invert	Pushed In (normal)
DC Offset Dials	0-0
Normal/Smooth	Normal

TEXT CORRECTION

Section 1 Characteristics

Page 1-3

ADD: the following information to the end of the present text:

Characteristic		Performance Requirement	
J 101 From Type 568		True	False
Pin	Indicates		
1	Decimal 2	≤ +2 V, ≤ 2.8 mA	≥ +6 V, ≥ 0.0 mA
2	Decimal 3	≤ +2 V, ≤ 3 mA	≥ +6 V, ≥ -0.15 mA
3	Decimal 4		
4	Not Used		
5	Not Used		
6	Letter V	≤ +2 V, ≤ 1.5 mA	≥ +6 V, ≥ -0.15 mA
7	Letter m		
9	Letter μ		
10	Letter n	≤ +2 V, ≤ 1.5 mA	≥ +6 V, ≥ -0.15 mA
11	Ch A Signal In	1 V/div ±3% at +10 V center screen. Z_{in} ≥ 10 kΩ	
12	A Signal Shield		
13	not used		
14	3T4 Speed up	≥ +1 V at ≤ 2.5 mA	≥ -11 V at 68 kΩ ±10%
15	3T4 Single Sweep		
16	Chop/Alternate	≥ -1.0 V low to ≥ 1.0 V high, ≤ 1 kΩ	
17	CRT Intensity(output)	≥ +0.8 V at 270 Ω ±10%	≤ 0.2 V at 270 Ω ±10%
18	Ground		
19	Ground		
20	Sweep	5 V/div ±3% starting at 0 V ±0.5 V	
21	Sweep Gate	≥ +1.0 V at 3 kΩ ±5%	≥ -0.5 V at 3 kΩ ±5%
22	10 MHz	≥ -9.3 V, 0.17 mA	≤ -3.1 V, 0.06 mA
23	Ch B Signal In	1 V/div ±3% +10 V center screen. Z_{in} ≥ 10 kΩ	
24	B Signal Shield		
25	Horiz Decimal Units, Common	≥ -.25 V at ≤ 5 mA	≥ +23 V at 235 kΩ ±10%
26	A ÷ 1,2,5	≥ -2.5 V at ≤ 5 mA	+12 V at 24 kΩ ±10%
27	B ÷ 1,2,5		
28	A Decimal Units Common	≥ -3.0 V at ≤ 5 mA	+12 V at 24 kΩ ±10%
29	B Decimal Units Common		
30	Horiz ÷ 2	≤ +2 V, ≤ 2.4 mA	≥ +6 V, ≤ 0.5 mA
31	Horiz ÷ 5	≤ +2 V, ≤ 0.4 mA	≥ +6 V, 0.0 mA
32	Vert ÷ 1	≤ +2 V, ≤ 2.4 mA	≥ +6 V, 0.0 mA
33	Vert ÷ 2	≤ +2 V, ≤ 1.4 mA	≥ +6 V, 0.0 mA
34	Vert ÷ 5	≤ +2 V, ≤ 5.5 mA	≥ +6 V, 0.0 mA
35	Sweep Clock Risetime/Falltime Frequency Pulse Width Amplitude	 ≤ 150 ns ≤ 1 MHz 0.7 μs to 1.3 μs ≥ -0.5 V to +1 V at ≥ 0.5 mA	 ≥ 0.5 mA
36	Clock Shield		

Characteristic		Performance Requirement	
J 201 Reference Zone Program		True	False
Pin	Program		
1	A 0% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
2	A 0% Position 4		
3	A 0% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
4	A 0% Position 1		
5	A 0% Position 0.5		
6	A 0% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
7	A 0% Width 2		
8	External Volts	≤ +2 V, ≤ 6 mA	≥ +6 V, ≤ 2.9 mA
9	A 100% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
10	A 100% Position 4		
11	A 100% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
12	A 100% Position 1		
13	A 100% Position 0.5		
14	A 100% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
15	A 100% Width 2		
16	A Chopped	≤ +2 V, ≤ 0.4 mA	≥ +6 V, ≤ 0.1 mA
17	Program Common		
18	Program Common		
19	B 0% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
20	B 0% Position 4		
21	B 0% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
22	B 0% Position 1		
23	B 0% Position 0.5		
24	B 0% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
25	B 0% Width 2		
26	Measurement Average	≤ +2 V, ≤ 3.7 mA	≥ +6 V, ≥ -2.4 mA
27	B 100% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
28	B 100% Position 4		
29	B 100% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
30	B 100% Position 1		
31	B 100% Position 0.5		
32	B 100% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
33	B 100% Width 2		
34	B Chopped	≤ +2 V, ≤ 0.4 mA	≥ +6 V, ≤ 0.03 mA
35	Program Common	≤ +24 V, ≤ 500 mA	
36	Program Common		

Characteristic		Performance Requirement	
J 201 Reference Zone Program		True	False
Pin	Program		
1	A 0% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
2	A 0% Position 4		
3	A 0% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
4	A 0% Position 1		
5	A 0% Position 0.5		
6	A 0% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
7	A 0% Width 2		
8	External Volts	≤ +2 V, ≤ 6 mA	≥ +6 V, ≤ 2.9 mA
9	A 100% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
10	A 100% Position 4		
11	A 100% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
12	A 100% Position 1		
13	A 100% Position 0.5		
14	A 100% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
15	A 100% Width 2		
16	A Chopped	≤ +2 V, ≤ 0.4 mA	≥ +6 V, ≤ 0.1 mA
17	Program Common		
18	Program Common		
19	B 0% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
20	B 0% Position 4		
21	B 0% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
22	B 0% Position 1		
23	B 0% Position 0.5		
24	B 0% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
25	B 0% Width 2		
26	Measurement Average	≤ +2 V, ≤ 3.7 mA	≥ +6 V, ≥ -2.4 mA
27	B 100% Position 8	≤ +2 V, ≤ 2.3 mA	≥ +6 V, ≤ 0.25 mA
28	B 100% Position 4		
29	B 100% Position 2	≤ +2 V, ≤ 2.1 mA	≥ +6 V, ≤ 0.1 mA
30	B 100% Position 1		
31	B 100% Position 0.5		
32	B 100% Width 4	≤ +2 V, ≤ 0.7 mA	≥ +6 V, ≤ 0.1 mA
33	B 100% Width 2		
34	B Chopped	≤ +2 V, ≤ 0.4 mA	≥ +6 V, ≤ 0.03 mA
35	Program Common	≤ +24 V, ≤ 500 mA	
36	Program Common		

Characteristic		Performance Requirement	
J 202 Comparator Program		True	False
Pin	Program		
1	Start B Channel	≤ +2 V, ≤ 7.1 mA	≥ +6 V, ≤ 2.9 mA
2	Start HORIZ mm	≤ +2 V, ≤ 4 mA	≥ +6 V, ≤ 2.7 mA
3	Start Percent Between	≤ +2 V, ≤ 5.9 mA	≥ +6 V, ≤ 2.9 mA
4	Start mm BELOW Reference Zone	≤ +2 V, ≤ 2.9 mA	≥ +6 V, ≤ 3.7 mA
5	Start Offset from 100%	≤ +2 V, ≤ 3.7 mA	≥ +6 V, ≤ 2.9 mA
6	Start Minus Slope	≤ +2 V, ≤ 1.4 mA	≥ +6 V, ≤ 0.8 mA
7	Start Second Slope		
8	Counter Reset Inhibit	≤ +2 V, ≤ 2.5 mA	≥ +6 V, ≥ -0.5 mA
9	Start Offset 80	≤ +2 V, ≤ 1.3 mA	≥ +6 V, ≥ -0.1 mA
10	Start Offset 40		
11	Start Offset 20		
12	Start Offset 10		
13	Start Offset 8	≤ +2 V, ≤ 3.7 mA	≥ +6 V, 0.0 mA
14	Start Offset 4	≤ +2 V, ≤ 1.3 mA	≥ +6 V, ≥ -0.1 mA
15	Start Offset 2		
16	Start Offset 1		
17	Program Common		
18	Program Common		
19	Stop B Channel	≤ +2 V, ≤ 7.1 mA	≥ +6 V, ≤ 2.9 mA
20	Stop HORIZ mm	≤ +2 V, ≤ 4.0 mA	≥ +6 V, ≤ 2.7 mA
21	Stop Percent Between	≤ +2 V, ≤ 5.9 mA	≥ +6 V, ≤ 2.9 mA
22	Stop mm BELOW Reference Zone	≤ +2 V, ≤ 4.9 mA	≥ +6 V, ≤ 3.7 mA
23	Stop Offset from 100%	≤ +2 V, ≤ 3.7 mA	≥ +6 V, ≤ 2.9 mA
24	Stop Minus Slope	≤ +2 V, ≤ 1.4 mA	≥ +6 V, ≤ 0.8 mA
25	Stop Second Slope		
26	External Scale	≤ +2 V, ≤ 1.4 mA	≥ +6 V, ≤ 0.1 mA
27	Stop Offset 80	≤ +2 V, ≤ 1.3 mA	≥ +6 V, ≥ -0.1 mA
28	Stop Offset 40		
29	Stop Offset 20		
30	Stop Offset 10		
31	Stop Offset 8	≤ +2 V, ≤ 3.7 mA	≥ +6V, 0.0 mA
32	Stop Offset 4	≤ +2 V, ≤ 1.3 mA	≥ +6 V, ≥ -0.1 mA
33	Stop Offset 2		
34	Stop Offset 1		
35	Program Common		
36	Program Common		

Characteristic		Performance Requirement	
J 203 Limit Program		True	False
Pin	Program		
1	External ÷ 2	≤ +2 V, ≤ 2.4 mA	≥ +6 V, ≤ 0.5 mA
2	Upper Minus	≤ +2 V, ≤ 1.9 mA	≥ +6 V, 0.0 mA
4	Upper 1000		
6	Upper 400		
8	Upper 100		
10	Upper 40		
12	Upper 10		
14	Upper 4		
16	Upper 1		
3	Upper 2000	≤ +2 V, ≤ 1.2 mA	≥ +6 V, ≤ 0.5 mA
5	Upper 800		
7	Upper 200		
9	Upper 80		
11	Upper 20		
13	Upper 8		
15	Upper 2		
17	Program Common		
18	Program Common		
19	Ext ÷ 5	≤ +2 V, ≤ 0.4 mA	≥ +6 V, ≥ -0.4 mA
20	Lower Minus	≤ +2 V, ≤ 1.0 mA	≥ +6 V, 0.0 mA
21	Lower 2000	≤ +2 V, ≤ 1.2 mA	≥ +6 V, ≤ 0.5 mA
23	Lower 800		
25	Lower 200		
27	Lower 80		
29	Lower 20		
31	Lower 8		
33	Lower 2		
22	Lower 1000	≤ +2 V, ≤ 1.9 mA	≥ +6 V, 0.0 mA
24	Lower 400		
26	Lower 100		
28	Lower 40		
30	Lower 10		
32	Lower 4	≤ +2 V, ≤ 1.9 mA	≥ +6 V, 0.0 mA
34	Lower 1		
35	Lower 1		
36	Program Common		

Characteristic		Performance Requirement	
J 204 Miscillaneous Inputs and Outputs			
		True	False
Pin	Indicates		
1	Print Command	≤ +2 V, at ≤ 20 mA	+12 V at 3 kΩ ±10%
2	External Hold		
	Hold	≤ +2 V, ≤ 6 mA	
	Release	≥ +7 V, ≤ 2.4 mA	
3	Red Light	≤ +2 V at ≤ 20 mA	≥ +10 V at ≤ 100 Ω
4	Green Light		
5	Yellow Light		
6	+ Trigger		
	Risetime	≤1 μs	
	Amplitude	≥ 3 V (positive step)	
7	- Trigger		
	Risetime	≤ 1 μs	
	Amplitude	≥ 3 V (negative step)	
8	Program 3T4 H.S.	≤ +2 V, ≤ 4.4 mA	≥ +6 V, ≥ -1.7 mA
9	3T4 Speed Up	≥ +1 V, ≤ 2.5 mA	≥ -11 V at 68 kΩ ±10%
10	3T4 Single Sweep		
11	A Chopper Drive	≤ +1 V, ≤ 20 mA	+12 V at 12 kΩ ±10%
12	B Chopper Drive		
13	Ext Decimal 2	≤ +2 V, ≤ 2.8 mA	≥ +6 V, 0.0 mA
14	Ext Decimal 3	≤ +2 V, ≤ 1.5 mA	≥ +6 V, ≤ 0.05 mA
15	Ext Decimal 4		
16	not used		
17	Ext Letter V	≤ +2 V, ≤ 1.5 mA	≥ +6 V, ≥ -0.14 mA
18	Ext Letter s		
19	Ext Letter m		
20	Ext Letter μ		
21	Ext Letter n		
22	+50 V	±1% at ≤ 25 mA	
23	+12 V	±1% at ≤ 350 mA	
24	+3.8 V	±1% at ≤ 200 mA	
25	-50 V	±1% at ≤ 25 mA	
26	not used		
27	not used		
28	not used		
29	not used		
30	not used		
31	not used		
32	not used		
33	not used		
34	not used		
35	Program Common		
36	Ground		

Characteristic		Performance Requirement	
J 301 Readout Connector		True	False
Pin	Indicates		
1	+	≤ 2 V at ≤ 20 mA	+12 V at 2.4 kΩ ±10%
2	-		
3	2000	≤ +2 V, ≤ +20 mA	≥ +12 V at ≤ 1 mA
4	1000		
5	800		
6	400		
7	200		
8	100		
9	80		
10	40		
11	20		
12	10		
13	8		
14	4		
15	2	≤ +2 V, ≤ +20 mA	≥ +12 V at ≤ 1 mA
16	1		
17	not used		
18	not used		
19	X 10^{-1}	≤ +5 V at ≤ 1 mA	+12 V at 120 kΩ ±15%
20	X 10^{-2}		
21	X 10^{-4}		
22	V	≤ 2 V at ≤ 20 mA	+12 V at 2.4 kΩ ±10%
23	S		
24	m		
25	μ		
26	n		
27	Red	≤ 2 V at ≤ 20 mA	≥ +10 V at ≤ 100 Ω
28	Green		
29	Yellow		
30	External Hold	Hold ≤ +2 V at ≤ 6 mA, Release ≥ +7 V at ≤ 2.4 mA	
31	Print Command	≤ 2 V at ≤ 20 mA	+12 V at 6.2 kΩ ±5%
32	not used		
33	+12 V Out	±1% at ≤ 350 mA	Ripple ≤ 5 mV
34	not used		
35	not used		
36	Ground		

TYPE 230/R230 TENT SN B190910

ELECTRICAL PARTS LIST CORRECTION

CHANGE TO:

Q2421	151-0292-00	Silicon	Nixie Driver
Q2423	151-0292-00	Silicon	Nixie Driver
Q2425	151-0292-00	Silicon	Nixie Driver
Q2427	151-0292-00	Silicon	Nixie Driver
Q2431	151-0292-00	Silicon	Nixie Driver
Q2433	151-0292-00	Silicon	Nixie Driver
Q2481	151-0292-00	Silicon	Nixie Driver
Q2483	151-0292-00	Silicon	Nixie Driver
Q2485	151-0292-00	Silicon	Nixie Driver
Q2487	151-0292-00	Silicon	Nixie Driver
Q2489	151-0292-00	Silicon	Nixie Driver

M15,364/969

TYPE 230/R230

ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTIONS

SYNCHRONIZER CARD - Series F

CHANGE TO:

R1778	315-0753-00	75 kΩ	1/4 W	5%	Model 9-up

ELECTRICAL PARTS LIST AND SCHEMATIC CORRECTIONS

SYNCHRONIZER CARD Series F

CHANGE TO:

R1790	315-0103-00	10 kΩ	1/4 W	5%	Model 10-up