DETAILED CIRCUIT DESCRIPTION

SYSTEM PROCESSOR

The System Processor (diagram 1) is the control center of all operations in the scope. It consists of an 8-bit microprocessor (μP), an 8-bit data bus, a 16-bit address bus, a prioritizing interrupt system, hardware address decoding, nonvolatile RAM space, and 272K bytes of bank-switched ROM.

The System Processor circuitry also coordinates the functions of the two other microprocessors in the 2430, the Waveform Processor and the Front Panel Processor.

System μP

System μP U640 executes instructions stored in the System ROM in order to initiate and control the various functions of this scope. Internally, the microprocessor has 16-bit data paths; externally it has an 8-bit data bus for communication and a separate 16-bit address bus. No address/data bus demultiplexing is necessary. The μP is driven by an external 8-MHz clock that is divided by four internally for a 2-MHz cycle rate. The number of cycles per instruction varies from a minimum of 2 to a maximum of 20, with the average being about 4 cycles per instruction. The μP executes, on the average, 1/2 MIP (Million Instructions Per second).

System μP U640 generates three signals used to control the communication activities of external circuitry. Of these signals, E and Q are for timing purposes. The rising edge of Q signals that the address on the bus is valid; data to the μP is latched on the falling edge of E. The third signal generated is the R/W signal. It is valid the same time the address is valid, and its state (LO or HI) determines whether an addressed device is written to or read from.

The E signal (U640 pin 34) and the Q signal (U640 pin 35) are ORed together by U840D to generate the HVMA (Host Valid Memory Address) signal. When HVMA at U840D pin 11 is HI, the address on the bus is valid. Once the external circuitry receives a valid address signal, it proceeds with the specified memory access. The signals used to enable and time these accesses are $\overline{RD}$ (read) and $\overline{WR}$ (write).

The $\overline{RD}$ signal is derived from U844A, which NANDs the HVMA signal with the μP R/$\overline{W}$ signal. Inverting buffer U572C provides added driving power to the R/$\overline{W}$ signal, and inverting buffer U884B reinverts it back to its original polarity before it is applied to NAND-gate U844A. The output of U844A is the $\overline{RD}$ signal, whose falling edge indicates the start of a read cycle. The rising edge of $\overline{RD}$ is coincident with the latching of the data read into μP U640.

The $\overline{WR}$ signal is derived from an inverted version of the μP R/$\overline{W}$ signal (via U572C) with a buffered μP Q signal (via U880D) NANDed by U844B. The output of this NAND-gate is a signal with a falling edge that indicates the start of a write cycle to the addressed device and a rising edge that latches data from the μP into the addressed device. The Q signal is used here instead of HVMA (as was used to generate $\overline{RD}$ to produce a data hold time of more than 100 ns as needed by the oscilloscope Time Base Controller circuitry.

Data Bus Buffer

Data Bus Buffer U650 provides buffering of the data bus lines. It is bidirectional to enable two-way communication between the System μP and the data bus. In normal operation, jumper J126 will connect the chip-enable pin to ground, and the buffer is enabled to transfer data. The direction of the transfer is controlled by the R/$\overline{W}$ signal from the System μP via inverting buffer U572C.

Moving test jumper J126 to its "KERNEL" position disables buffer U650 and forces it to its tri-state (high-impedance output) mode. The pull-up and pull-down resistors on the data bus lines, R742, R746, and R744, place an instruction byte on the μP data bus that causes the μP to repeatedly increment the addresses placed on its address bus lines through their entire range. This procedure is a troubleshooting aid that exercises a good portion of the address-decoding and chip-select circuitry.

Address Buffers

Address Buffers U632 and U730 provide buffering of the System μP address lines to the various addressable devices. The buffer chips are permanently enabled and provide both current buffering and electrical isolation for the address lines. Test point TP840 is provided as a source of an oscilloscope trigger signal when checking the incrementing address lines in the forced "KERNEL" troubleshooting mode described in the "Data Bus Buffer" description.

System ROM

The System ROM (read-only memory) stores the commands and data used by System μP U640 to execute its control functions. The System ROM is made up of one 16K byte × 8-bit memory device, U670, that contains the System μP operating system, and four page-switched, 64K byte × 8-bit memory devices, U680, U682, U690, and U692 used for storage of all the additional operating routines. This gives a total of 272K bytes of ROM space. Each ROM is individually enabled by the ROM Select circuitry, and the addressed data will only appear on the system data bus when the $\overline{\text{RD}}$ (read) signal goes LO. Since μP U640 has the capability to address only 64K locations and has to address other things besides ROM, the System ROM is split into 17 pages. Address decoders U890A, U890B, and part of PC Register U860, select the page of ROM to be read from to allow the System μP to access the entire 272K byte ROM space.

Immediately after the power-up reset ends, μP U640 automatically tries to fetch the reset vector (the location of the first program instruction) from locations FFFE(hex) and FFFF(hex) in its address space. Anytime the System μP tries to access memory, the HVMA (host valid memory address) signal from U840D will be HI during the time the address is guaranteed to be valid. Addresses FFFE and FFFF have bits AE and AF (the two MSBs of the address bus) set HI; therefore, with the HVMA signal HI, NAND-gate U870D outputs a LO that enables U890A, and a $\overline{\text{ROM1}}$ select output is obtained from U890A for both addresses. The $\overline{\text{ROM1}}$ applied to the chip-enable input of ROM U670, along with the LO $\overline{\text{RD}}$ applied to its output enable, outputs the two 8-bit data bytes from location FFFE and location FFFF onto the system data bus via bus transceiver U660. The address contained in these bytes directs the μP to the start of its program, and the program is started.

When the μP needs information from one of the other System ROMs, it writes four bits of select data into register U860. Of these bits, PAGE-BIT0 and PAGE-BIT1, applied to 1-of-4 Decoder U890B, select which ROM chip of ROM0 is enabled. PAGE-BIT2 and PAGE-BIT3 are the most significant bits of the ROM addresses and determine which page of the enabled ROM is addressed.

Power-Up Reset

The Power-Up Reset circuit keeps the System μP reset until all instrument power supplies are sure to be operating properly and for the 100 ms delay needed by μP U640. This delay time is enough that the processor will begin the operating program with all electrical components in valid (defined) states after the instrument is turned on.

The Power-Up Reset circuit consists of an RC-integrator formed by R936 and C938 and a comparator circuit formed by U940B and associated components. Capacitor C938 begins charging when the PWRUP (power-up) signal goes HI, and the comparator detects when this charging level crosses a predefined threshold voltage (set by R944, R943, and R942). Positive feedback through R942 separates the turn-on and turn-off thresholds of comparator U940B to ensure that switching of the comparator is positive when the threshold level is reached. The turn-on circuit delay of approximately 100 ms allows all electrical components to stabilize before attempting any circuit operations.

On power-down, the PWRUP line is immediately pulled LO, and capacitor C938 begins discharging via R938 and diode CR936. At the time this discharge is initiated, the $\overline{\text{NMI}}$ (nonmaskable interrupt) is asserted, and the processor branches to the power-down routine. In the power-down period before the power supplies are discharged, the μP does the housekeeping activities that ensure the data stored in Nonvolatile (NV) RAM is correct and turns off any asserted 50-ohm input coupling. After approximately 10 ms of discharging, the $\overline{\text{RESET}}$ line is asserted to hold the μP reset while the power supplies finish their discharge. If power to the System μP is not lost but merely reduced, approximately 260 ms after $\overline{\text{NMI}}$ goes LO, the System μP will fetch its reset vector and restart as though the power was actually cycled off and then back on.

Interrupt Logic

The Interrupt Logic circuit provides a means by which other sub-systems may interrupt the normal program execution being done by the μP to request service. Three levels of interrupts are available in μP U640. The $\overline{\text{NMI}}$ (nonmaskable interrupt) that occurs at power-down has priority over the other two interrupt levels. If either of the other interrupts is present at the same time as the $\overline{\text{NMI}}$, the μP gives preference to the $\overline{\text{NMI}}$ and immediately branches to the power-down routine. The power-down routine performs the operations necessary for an orderly shut-down of the scope. A cyclical-redundancy checksum of the data stored in Nonvolatile RAM is calculated and stored back into that RAM. On power-up, that checksum is used to verify the validity of the parameters and settings stored in the Nonvolatile RAM. To prevent a possible 50-ohm overload of the Channel 1 or Channel 2 input circuitry during times that the instrument is off, part of the power-down routine is to make certain that input coupling is set to a high-impedance state.

The next interrupt in priority after the $\overline{\text{NMI}}$ is the $\overline{\text{FIRQ}}$ (fast-interrupt request). It is produced by flip-flop U894A in response to a 2 ms clock signal from the Time Base circuit (diagram 8). The 2 ms clock sets the $\overline{\text{FIRQ}}$ line LO every 2 ms to signal μP U640 that it is time to do the time-critical tasks like updating the DAC System. When the fast-interrupt request has been serviced, the μP clears the $\overline{\text{FIRQ}}$ latched into U894A by outputting address 6012h. This address is decoded by 1-of-8 Decoder U884 to generate a $\overline{\text{CLRFIRQ}}$ (clear fast-interrupt request) signal that resets flip-flop U894A. Servicing of a fast-interrupt request differs from other interrupt requests in that the contents of only two μP registers are pushed to an internal stack (instead of all the μP registers), allowing the μP to respond faster.

The lowest priority is given to the combined signal forming the $\overline{\text{IRQ}}$ (interrupt request). This interrupt allows various sub-systems to get attention from the System μP. NOR-gate U850B outputs a LO when any of the five conditions occur. Inputs to NOR-gate U850B are from: the GPIB (General Purpose Interface Bus), the Display circuitry, the Front Panel, the Waveform μP, and the Trigger System. Of these, the latter three interrupts may be masked off (disabled) by the μP by writing LO mask bits into register U760 which are then applied to AND-gates U880A, U880B, and U880C. A LO input to one input of an AND-gate holds the associated output pin LO and prevents an interrupt signal from being gated through to NOR-gate U850B. The Waveform μP may mask the Display System interrupt (DISDN) from the System μP by placing a LO on pin 5 (MDISDN) of AND-gate U580B from register U550 (diagram 2). The Waveform μP thereby can gain first access to the Display System if it needs to do display updates before the System μP sees that the Display System is finished with its last task. When the Waveform μP is done, it writes the MDISDN interrupt HI to let the System μP know that it is finished with the Display System and the Display System is ready to be restarted.

When an $\overline{\text{IRQ}}$ interrupt is detected, the μP executes a read of location 6010h which is the address of Interrupt Register U654 (an octal buffer). That address is decoded by 1-of-8 Decoder U884 to set $\overline{\text{INTREG}}$ LO and enable U654. The enabled buffer passes the status of the various interrupt lines at its inputs to the data bus for the μP to read. From the status bits read, the μP determines which circuit caused the interrupt and branches to the called for interrupt service routine. If more than one interrupt is pending, the System μP IRQ interrupt handling routine decides which one needs to be (or can be) handled first. The order in which it handles these interrupts depends on the current activity of the System μP.

Besides interrupt status, three other status bits are read from the Interrupt Register. These are the DCOK (dc ok) signal from the power supply (check during the calibration routine register checks), BUSGRANT from the Waveform μP, and $\overline{\text{FPDNRD}}$. DCOK signifies that the various power supply voltages are within proper limits; BUSGRANT indicates that the Waveform μP has relinquished bus control in its operating space and that those addresses are now mapped into the System μP address space. $\overline{\text{FPDNRD}}$ indicates that the Front Panel μP has read the data sent to it from the System μP.

System Address Decode Circuit

The System Address Decode circuit uses several of the system address bits, along with other control signals, to connect the System Data Bus (via the Memory Buffer) to System RAM and ROM (called System Memory, collectively) for those addresses that map to those memories. It also isolates the System Data Bus from System Memory when the System μP output addresses that map to other memory devices or certain input/output registers. Some control signals are routed from this decode circuit to other circuits and are used to decode enables for those circuits.

MEMORY BUFFER. U660, a bi-directional buffer, connects or isolates the System Data Bus from System Memory depending on whether enabled or disabled by the output of AND-gate U580A. Direction of data transfer is controlled by $\overline{\text{WR}}$ (write) line from the system processor. When devices other than System ROM or System RAM are addressed, the buffer outputs are switched to a high-impedance state to isolate the memory devices from the data bus.

MEMORY MAP. Figure 3-2 is a memory map showing the different memory areas and the address blocks they occupy on the System Processor and the Waveform Processor Data Bus. Addresses output by the System Processor and/or the Waveform Processor access the memory indicated in the address block depending on how those addresses are decoded. Refer to Figure 3-2 as the address blocks are discussed (both here and later for the Waveform RAM).

As indicated by the memory map, addresses from 0000h-7FFFh are overlapping addresses; that is, if they are originated by the System Processor, they may map to (access) memory locations or registers connected to either

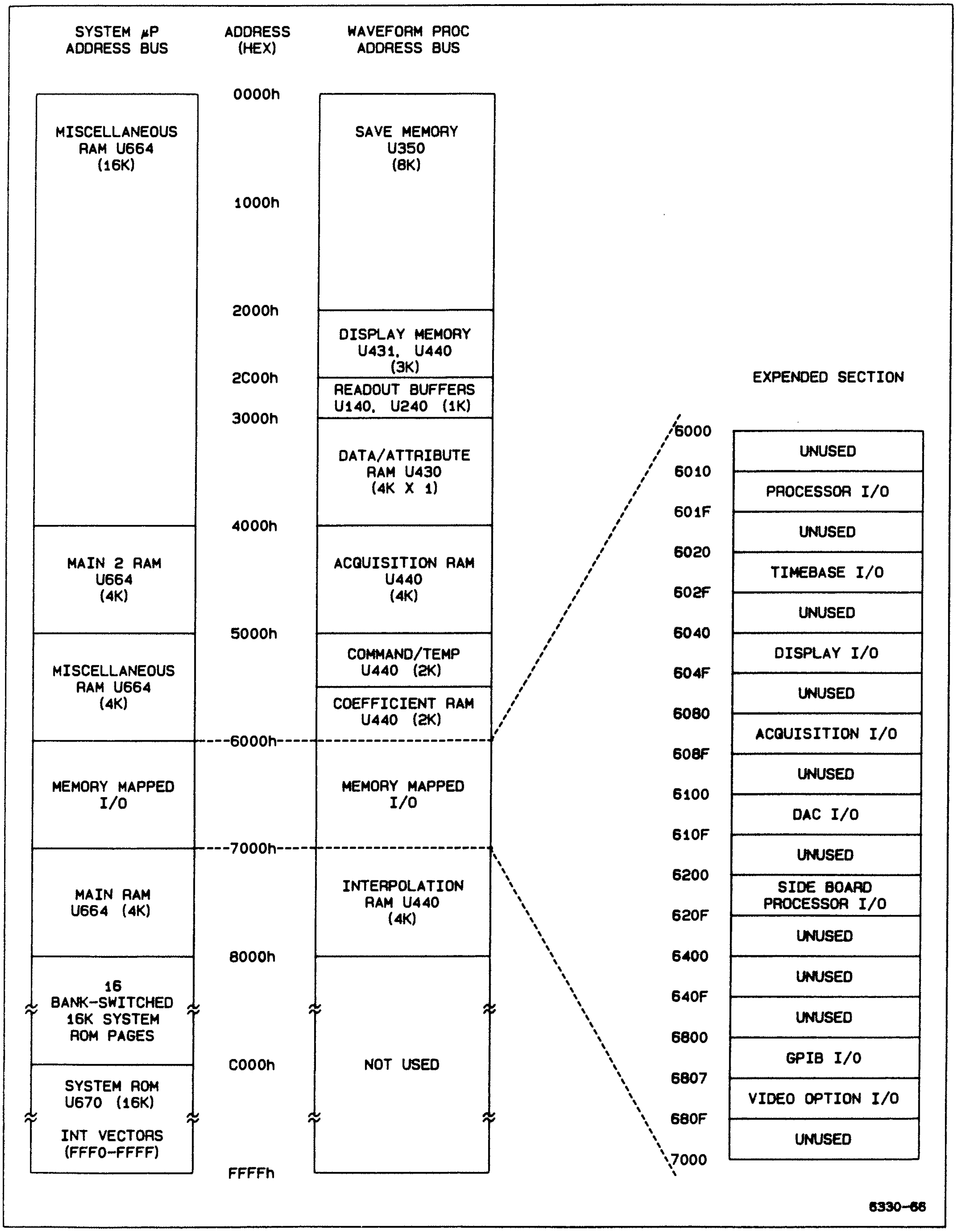


Figure 3-2. Simplified Memory Map

the System Data Bus or the Waveform Processor Data bus. If they are originated by the Waveform Processor, they access the memories indicated on the Waveform Processor Bus. The following description of the address decoding is for System Processor addresses and how the System Address Circuit outputs control signals to the Memory Buffer and to the address decoding circuit for the Waveform Processor (diagram 2). For information on how the Waveform Processor's address decoding circuitry uses these signals, see "Waveform Processor Operation" in this section.

ADDRESSES 8000h-FFFFh. All addresses from 8000h-FFFFh have AF set HI. This HI is AF is inverted (via U866C) and routed to U580A. With the inverted AF bit holding the input of AND-gate U580A LO, the output of the gate holds the Memory Buffer U660 enabled (LO). As shown in the memory map, all addresses in this range are System ROM accesses and require System Data Bus connection to the System Memory Data Bus. Locations 8000h-FFFFh are not used to address any other memory devices outside System memory (decoding for the paged System ROM was discussed under "System ROM" in this section).

ADDRESSES 0000h-7FFFh. All addresses in this range have the AF bit set LO. With AF LO, the inverted AF signal holds a HI at one input to the dual-input AND-gate U580A. The output of this AND-gate (and the enabling of U660) is then controlled by the output of OR-gate U332A.

When the System Processor wants these address ranges to map to the Waveform Processor Data Bus (i. e., wants the System Data Bus and the Waveform Data Bus connected) , it either asserts BUSREQ to the Waveform μP to receive BUSGRANT, or it asserts BUSTAKE to force BUSGRANT. BUSGRANT at the input of OR-GATE U250D forces a HI to the input of AND-gate U862B. If this is not a $\overline{\text{MAIN}}$ or $\overline{\text{MAIN2}}$ memory access, $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$ from 1-of-8 Decoder U668 are both HI and U862B output is driven HI by the BUSGRANT. This HI is coupled through U332A and U580A to disable the U660 Memory Buffer and disconnect the System Data Bus from System Memory. $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$ are routed to decoding circuitry and used to connect the System Data Bus to the Waveform Data Bus (see "System μP Access" under "Waveform Processor Operation" in this section).

If either of the host RAM enables $\overline{\text{MAIN}}$ or $\overline{\text{MAIN2}}$ are LO, the 1-of-8 decoder U668 has decoded address lines AC, AD, and AE to determine that the addresses range from 4000h-4FFFh or from 7000h-7FFFh. In these address ranges, the LO host RAM enable holds off the BUSGRANT-forced HI at the output of U250D from driving the output of AND-gate U862B HI. If the System Processor is accessing these locations in Waveform Processor RAM, it asserts WFRAM HI (Waveform RAM) at the input to OR-gate U332A. This HI is coupled through U332A and AND-gate U580 to disable U660 regardless of BUSGRANT, $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$. BUSGRANT and WFRAM are routed to decoding circuitry to connect the System DATA Bus to the Waveform Data Bus.

If the System Processor is NOT accessing Waveform Processor RAM for the 4000h-4FFFh or 7000h-7FFFh address space, WFRAM is disabled LO. With either $\overline{\text{MAIN}}$ or $\overline{\text{MAIN2}}$ enabled LO, the output of U862B is driven LO. This LO lets OR-gate U332A, and then AND-gate U580A, switch LO and enables Memory Buffer U660 to connect the System Data Bus to the System Memory Bus. The $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$ memories are then accessed.

If the System Processor is NOT accessing Waveform Processor RAM or a MAIN-section of System RAM, BUSGRANT and WFRAM are NOT asserted HI and $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$ are not asserted LO. In this case, the output of four-input AND-gate U862A controls the enabling/disabling of the Memory Buffer. U862A combines with AND-gate U432B to form a five-input AND-gate function, with output Y0-Y3 and Y5 connected to the five inputs. If the address is in the range of 0000h-4FFFh or 5000h-5FFFh, 1-of-8 decoder U668 decodes a LO output to one of the five ANDed inputs. U862A outputs a LO which is ORed (by U250D) with the disabled BUSGRANT (LO) to hold off AND-gate U862B. The LO at the output of U862B is passed through U332A (WPRAM is LO) and U580A to enable the Memory Buffer and connect the System Data Bus to the System Memory. The LO output of U322A, $\overline{\text{CYSYS}}$, also enables the System RAM for this Miscellaneous RAM access.

ADDRESSES 6000h-6FFFh. Addresses in this range either access devices on the Waveform Processor bus or directly access devices on the System Data Bus. If the address is in this range, U668 decodes Y6, $\overline{\text{HMMIO}}$ LO.

Since Y6 is LO, all other outputs, including those driving the five inputs to AND-function U862A/U432B, are HI. With the five inputs to AND-function U862A/U432B all HI, its output is HI to U862. With the remaining two decoder outputs U862B, $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$, set HI, AND-gate U862B outputs a HI that holds the Memory Buffer disabled for ALL HMMIO accesses. $\overline{\text{HMMIO}}$ is inverted via U866B and is routed, along with address bits A3 and A4, to decoding circuitry (Diagram 2) to determine when the System Data Bus connects to the Waveform Data Bus for HMMIO accesses.

Host Memory-Mapped I/O

To permit the System μP to control the hardware functions of the scope, several control registers have been assigned to unique addresses within the μP address space (memory-mapped). These registers appear as blocks of read-only, write-only, or read-write memory to the System μP. The data bits handled by these registers control specific hardware functions, and the commands written will not violate any hardware restrictions.

As mentioned in "System Address Decode Circuit", the block of addresses from 6000h to 6FFFh corresponds to the host memory-mapped input/output ($\overline{\text{HMMIO}}$) block. Addresses within this block are decoded to produce a LO $\overline{\text{HMMIO}}$ signal to 1-of-8 Decoder U884 and Octal buffer U830. The three MSBs of the I/O address block and the HVMA (host valid memory address) are decoded by 1-of-8 decoder U668 to decode the I/O addresses between 6000h and 6FFFh.

One-of-eight Decoder U884 uses the $\overline{\text{HMMIO}}$ line and address bits A3 and A4 as enabling signals. Address lines A0 and A1 and the R/$\overline{\text{W}}$ line from the processor (via inverter U572C), select one of the eight outputs of U884 to go LO when the Decoder is enabled. Table 3-1 shows the registers accessed by this decoding.

Inverting buffer U830, enabled by $\overline{\text{HMMIO}}$ for I/O operations, applies the inverted middle bits of the address bus to various functional modules as selects. The firmware routines will allow only one of these select bits to be set LO at a time. In the selected circuit, further address decoding is enabled. Figure 3-2 illustrates the System μP address memory map and shows the blocks assigned for memory-mapped I/O. Each of the memory-mapped I/O blocks consists of 16 consecutive addresses from 6000h to 7000h with various functions assigned to specific addresses. These functions include clocks, chip enables, and circuit enables. Each is explained in the descriptions of the circuits they affect.

System RAM

The System RAM provides temporary storage of data used in execution of the various control functions of the System μP. In addition, long-term power-off storage of system-calibration constants and front-panel settings is provided, allowing the instrument to power on in the same state it was in when it was turned off.

The System RAM consists of a single memory device. It is nonvolatile RAM, that is, a battery-backup circuit is used to maintain data when power is off. The μP U640 controls the direction of data flow via the $\overline{\text{WR}}$ (write) and $\overline{\text{RD}}$ (read) control lines.

NOTE

Although all the data in this memory device is backed up and is, therefore, nonvolatile, that part of the System RAM reserved for data that NEEDS to be backed up (such as the calibration constants and front-panel settings) is referred to as NVRAM throughout this section. Parts of System RAM that do NOT NEED backing up are referred to as volatile RAM or just RAM.

Table 3-1
Host Memory-Mapped I/O

W/R	A1	A0	Output Signal
LO	LO	LO	INTREG (read Interrupt Register)
LO	LO	HI	PMISCIN (Processor miscellaneous inputs)
LO	HI	LO	CLRFIRQ (clears FIRQ flip-flop)[a]
LO	HI	HI	NC
HI	LO	LO	PCREG (write Processsor Control Register)
HI	LO	HI	PMISCOUT (write Misc Register)
HI	HI	LO	TVREG (write Video Option Register)
HI	HI	HI	WDREG (write Word Probe and GPIB LED Register)

[a]To clear the Fast-Interrupt Request, the μP does a read of the assigned address even through an actual register does not exist. The decoded output performs the reset function and no data is transferred.

The chip-select circuit for System RAM U664 consists of Q842, Q960, CR944, and associated components. With instrument power off, no bias current for Q960 is available, and the transistor is off. Power for maintaining the stored contents of the RAM is applied to U664 from the Battery circuit; with Q960 off, the chip enable input of U664 is also pulled HI via R764 to switch the I/O pins to their high-impedance state. This is the "low-power standby mode," and the contents of U664 are maintained as long as the Vb_{cc} supply and CE (chip enable) pins are held above +2 volts.

When instrument power is applied, a switching circuit in the Battery stage supplies power for the RAM, and the normal power supplies provide bias currents for the chip-select string between U332A and U664. As the power supplies are coming up, operations on the address bus are undefined, which could cause U332A to try to enable U664. To prevent this, the $\overline{\text{RESET}}$ signal from the Power-Up Reset stage is applied to the base circuit of Q960 through diode CR944. This LO keeps the transistor biased off until the power-up $\overline{\text{RESET}}$ signal returns HI; at which time the data on the address bus is stable.

With normal power on, when OR-gate U332A decodes a System RAM access, its output goes LO to turn off Q842. R956 then pulls up on the base of Q960, turning that transistor on and pulling the chip-enable pin of U664 LO to enable the System RAM. The RAM enable is removed when the output of U332A goes HI, turning Q842 back on and robbing the base current from Q960. With Q960 off, R764 pulls the the chip-enable input of U664 HI to disable the RAM.

Miscellaneous Registers

The Miscellaneous Registers allow the System μP to initiate and control various processes by writing control words to two address-decoded locations. The Miscellaneous Registers also contain an address-decoded buffer used to read certain bits of instrument status.

The $\overline{\text{RESET}}$ line holds all of the outputs of Processor Control Register U860 LO until the Power-Up Reset goes HI, ensuring that the functions controlled by the PC register outputs start in known states. To load U860 the System μP writes data to location 6014h, generating an address-decoded $\overline{\text{PCREG}}$ clock. This rising edge of the $\overline{\text{PCREG}}$ clock when the clock returns HI causes the data on the data bus to be written into the register. Table 3-2 illustrates the select functions of the PC Register output bits.

Table 3-2
Processor Control Register Functions

Bit	Output Name	Output Function
0 1	PAGE-BIT0 PAGE-BIT1	ROM enable selection signals for Bank-Switched System ROM.
2 3	PAGE-BIT2 PAGE-BIT3	Select a page in Bank-Switched System ROM.
4	WPRESET	Resets Waveform μP.
5	WPKERNEL	Places the Waveform μP in "Kernel" mode for diagnostics.
6	BUSREQ	System μP requests to take control of the Waveform μP busses.
7	BUSTAKE	System μP takes control of the Waveform μP address and data busses.
8	DIAGO	Diagnostic bit 0—verifies that data can be written to the PC register.

Operation of U760, the Processor Miscellaneous Register (PMREG), is similar to U860 just described. Data is written into the register with the $\overline{\text{PMISCOUT}}$ (processor miscellaneous outputs) clock when address 6015h is decoded by U884. Table 3-3 explains register functions.

The Processor Miscellaneous buffer (PMBUF), U854, at address 6011h, allows the System μP to monitor the activities of various other circuits. By reading the data byte from location 6011h, the System μP can check for the presence of a Word-Trigger probe and for Waveform μP and Front Panel μP interrupts. For diagnostic routines and self-check, correct operation of registers U760, U860, and U754 is verified by writing known values to the diagnostic bits (DIAG0, DIAG1, and DIAG2) then reading them back. If both HI'S and LO'S can be written to and read from these diagnostic locations, fairly high confidence may be placed in the addressing and selection of the registers and their data paths.

Battery

The Battery circuit supplies standby power to the System RAM that allows instrument calibration constants and front-panel settings to remain stored for long periods of time (greater than three years) when instrument power is turned off. A switching circuit turns off the battery (BT800) current source while normal instrument power is applied. A battery monitor circuit warns the Front Panel μP (and thereby the user) of a low-voltage condition (indicating that

Table 3-3
Processor Miscellaneous Register (PMREG) Output Functions

Bit	Output Name	Output Functionss
0	MWPDN	Masks off (disables) Waveform Processor Done interrupt.
1	MSYNTRIG	Masks off Synchronous Trigger interrupt.
2	MFPINT	Masks off Front-Panel interrupt.
3	STEP COMP	Indicates the AutoStep Sequencer has completed a sequence step.
4	SEQOUT	Indicates the AutoStep Sequencer has completed a sequence.
6	BELL	Indicates an event occurred which normally rings instrument's internal warning bell.

it is time to change the battery) or an over-voltage condition (indicating that reverse current is attempting to charge the lithium battery).

With normal instrument power applied, transistor Q806 will be turned on by the base-bias voltage-divider circuit formed by R812 and R815. Base current is then supplied through Q806 and R800 to turn on Q804. This is the normal operating mode, and operating current for Nonvolatile RAM U664 is supplied via Q804 from the +5 V_D supply. During normal operation, capacitor C904 is held charged through CR902 but isolated from the RAM power source by reverse-biased diode CR900.

With instrument power turned off, transistors Q806 and Q804 are both turned off. The positive charge potential stored by capacitor C904 forward biases CR900 and pulls the chip-enable pin of U664 HI through R764. This disables RAM U664 and switches its I/O ports to high-impedance states. Operation in this state is the "standby" mode in which data in U664 is maintained using minimal supply current.

The eventual charge loss from capacitor C904 causes its output voltage to drop below that of Backup Battery BT800 (a lithium battery), and diode CR900 again becomes reverse biased. The standby current for U664 is then supplied from the battery via CR802 (and R900 in the return path). Diode CR802 acts as the current switch and prevents reverse current through the lithium battery during normal power-on operation. Resistor R900 provides reverse-current limiting in the event that CR802 becomes shorted.

BATTERY WARNING CIRCUIT. Operational amplifier U940A is a very high impedance buffer to limit current drain of the battery. Its buffered output voltage is applied to the Front Panel μP (diagram 3) to monitor for both low-voltage and over-voltage conditions of the lithium backup battery. A battery-error condition found at power-on or with the Extended Diagnostics will cause the BATT-STATUS test to fail. That test may then be selected to run at the next lower level in the test hierarchy to determine if the battery is undervoltage or overvoltage. The warning circuit is operational only when normal instrument power is applied. Resistor R802 provides additional circuit impedance that prevents any appreciable discharging of the battery by the voltage-sensing circuit.

WAVEFORM PROCESSOR SYSTEM

The Waveform Processor System (diagram 2) performs the high-speed data-handling operations needed to produce and update displays of acquired data points on the crt including averaging, enveloping, adding, multiplying, and interpolation of the waveform data. It accepts task information from the System μP and then carries out the assigned tasks without further need of the System μP. When that task list has been completed, it sends an interrupt to the System μP to inform it that another list of tasks can be accepted.

The Waveform μP memory space is accessible by the System μP, allowing the System μP to send commands to the Waveform μP and to read any desired result or data location especially for the GPIB I/O functions.

Waveform μP

Waveform μP U470 is a specially designed, high-speed microprocessor with a 16-bit multiplexed data and address bus and separate 12-bit instruction-address and 16-bit instruction-data busses. The Waveform μP is clocked at 2.5 MHz and executes one instruction each clock cycle. Internally the Waveform μP uses a 32-bit wide instruction word. Therefore, to enable it to obtain a complete instruction for execution with each μP cycle, instructions are "double-prefetched." Two 16-bit halves of the instruction are fetched from the instruction bus with each cycle at a 5 MHz rate, so that the instruction words are 32 bits wide.

Initially, with power-on, $\overline{\text{WPRESET}}$ (Waveform μP reset) from Processor Controlled Register U860 (diagram 1) will be LO, holding the processor reset via U270C. This reset remains in effect until the System μP writes a HI bit to the $\overline{\text{WPRESET}}$ output of U860 to remove the reset and enable the Waveform μP. The System μP also holds the Waveform μP reset while it is updating the command list in RAM of the next task that the Waveform μP is to perform. This reset occurs at the completion of each set of tasks given to the Waveform μP and is released when the new task list is in place in the Waveform μP Command RAM, U440.

Upon release of $\overline{\text{WPRESET}}$, the Waveform μP fetches the first two 16-bit words from its instruction ROMs, U480 and U490, at a 5 MHz rate and forms them into a 32-bit instruction word. Waveform μP U470 then executes the first instruction and at the same time it "prefetches" the next 32-bit word from the instruction ROM (the next instruction). The Waveform μP continues fetching instructions to carry out its internal initialization routine until that is completed, and it then looks in Command RAM at a vectored location to find the first task in the task list.

The first instruction in the task list tells the Waveform μP what is to be done. The μP then switches to the routine in ROM to get the instructions that do that job. Part of that routine might be to get the arguments for the task. When the arguments are in place, the Waveform μP then finishes the task routine. When done with the first task, the Waveform μP looks at the task list for the next task. It keeps doing the commands and arguments for each task until the entire task list is done. The last task of every task list is the WPDN task (Waveform Processor Done). Upon receiving that task, the Waveform μP sets the WPDN bit to the System μP Interrupt circuit HI, informing the System μP that it is finished. It then enters a "loop forever" state to wait for its next set of instructions. When the System μP checks the interrupt register and finds WPDN HI, it resets the Waveform μP and writes a new list of tasks to the Waveform μP Command RAM.

WAVEFORM μP OPERATION. When the Waveform μP gains control of the waveform bus, it sequentially moves the 1024 data points for each channel (512 min/max pairs in envelope) from the Acquisition Memory (diagram 8) to the Save Memory (U350). When the Waveform μP does a display update, it selects the required data points needed for each waveform display requested (according to the mode selected) from Save Memory and moves them to the Display Memory (diagram 16). At the end of the display update, DISDN (display done) from the Display Control (diagram 17) goes HI to interrupt the Waveform μP (and the System μP if the Waveform μP is also done and permits the signal to be gated to the System μP via AND-gate U580B, diagram 1). This tells the Waveform μP that the current display cycle has completed and the next update to Display Memory may be started.

When in ENVELOPE acquisition mode with more than a one acquisition accumulation to be displayed, the data bytes stored in Save Memory are not automatically overwritten with each acquisition. As the data bytes are being transferred from Acquisition Memory to Save Memory, they are compared by the Waveform μP. If the new data byte does not exceed the current maximum or minimum value in Save Memory location that it is being compared with, that Save Memory location is not overwritten (until the envelope acquisition is reset to start a new accumulation).

In AVG acquisition mode, data from the Acquisition Memory is averaged with the waveform data in the Save Memory, and the Save Memory is then rewritten with the averaged waveform data. Waveform adds, multiplies, expansions, and interpolations are performed by the Waveform μP on the Save Memory data prior to transfer to the Display Memory for display.

WAVEFORM μP ADDRESS ENABLING. The 2.5 MHz System Clock signal CLK1 from the Clock Divider U710 (diagram 7) is inverted by U866E and ORed with the skewed 2.5 MHz CLK3 signal by OR-gate U264B. The timing of this ORed signal is such that the output of U264B goes HI when the address on the input pins of Waveform Address Registers U562 and U364 is guaranteed to be valid. Inverter U270B inverts the output from the OR-gate (WVMA—waveform valid-memory address), and when that output again goes LO, the rising edge of the inverted WVMA signal on the clock input of the Waveform Address Registers latches the 16-bit address from the Waveform μP into the registers.

ADDRESS LATCH. U366, a dual 4-to-1 multiplexer, and Address Latches U364 and U562 couple a modified version of the 16-bit address output by the Waveform μP (DAD0-DADF) to the Waveform Processor Address Bus (WA0-WAF). Addresses latched to the Waveform Processor Address Bus remain on that bus for the entire Waveform μP cycle.

Due to its architecture, the Waveform μP outputs different address blocks than those required to access the various memories on the Waveform Processor Data Bus (see Figure 3-2). U366 selects either address bit DADC or DADB for output to address WAB of the Waveform Processor Data Bus, depending on the condition of its three most-significant address bits, DADC, DADE, and DADF. AND-gate U276B detects when these bits are all HI and outputs a HI to the "A" select input of the multiplexer.

With the "B" select input held HI for all Waveform μP accesses by $\overline{\text{BUSCONNECT}}$, U366 routes DADB to address bit WB via address latch U562.

If any of the three most-significant Waveform μP address bits are low, DADC is coupled to address bit WB. This action translates the addresses output by the Waveform μP to those required on the Waveform Processor Bus.

If $\overline{\text{BUSCONNECT}}$ is LO, the access is a System Processor access and BUSGRANT is HI. BUSGRANT disables the Address Latches and the decoding action of U366 does not affect the address on the Waveform Processor Bus. BUSGRANT is inverted via U254B enables the Bus Connect Address Buffers to connect the System Address Bus to the Waveform Processor Bus.

Test point TP562 on address line WAA provides a trigger source for an external test oscilloscope when examining address waveforms in the Waveform μP "KERNEL" mode. As the KERNEL mode exercises address lines WA0-WAA, WAA is used as the trigger point.

WAVEFORM μP READ/WRITE ENABLING. Once latched, the address is removed from the bus and, depending on whether μP U470 is supposed to be reading or writing, data will be read into the processor from data bus buffers U360 and U560 or written to the WD (waveform data) bus via U360, a bidirectional data bus buffer. To read data into the processor, the HI R/$\overline{\text{W}}$ (read-write) signal is applied to NAND-gate U870C where it is NANDed with $\overline{\text{CLK1}}$. During the half period that $\overline{\text{CLK1}}$ is HI (CLK1 is LO), the gated output from U870C is the $\overline{\text{WRD}}$ (waveform processor read) in its LO (asserted) state. The LO is applied to the direction-enabling input of bidirectional buffer U360 via U542B. This LO enables U360 for a read from the WD (waveform data) bus, and the addressed 8-bit word on the WD bus is applied to the center eight lines of the processor 16-bit address/data bus.

The four least significant bits (LSB) and the four most significant bits (MSB) of the data applied to the WD bus come from buffer U560, which is enabled via U250B and U250A for processor reads. The four LSBs are always LO (guard bits), while the four MSBs will be set to the same level as the WD7 bit (sign-extended) of the center eight bits. This placement of the 8-bit data in the center of the 16-bit bus provides a reasonable tradeoff between dynamic range (12 bits) and guard bits (4 bits).

To write data out of the Waveform μP to the WD bus, the $\overline{\text{WRD}}$ level applied to the direction-enabling pin of U360 will be HI. The center eight bits of the Waveform μP data bus will then be buffered onto the WD (waveform data) bus by U360 and written to the currently addressed location. During writes to the WD bus, the HI level of $\overline{\text{WRD}}$ disables buffer U560, via U250B and U250A, to isolate it from the Waveform μP address/data bus.

SYSTEM μP ACCESS. When the System μP needs to do an access in the Waveform μP address space, it checks its software copy of PCREG to see if the Waveform μP is reset. If it is not reset, the System μP asserts BUSREQ (bus request) to the Waveform μP and waits until the Waveform μP outputs a BUSACK (bus acknowledge) to OR-gate U332D. The output of U332D is the BUSGRANT signal that, when HI, disables the Waveform μP data buffers, address registers, and memory control lines.

When Waveform μP U470 is being held reset (inactive) and cannot possibly respond to a BUSREQ, the System μP instead asserts BUSTAKE to OR-gate U332D when it needs to take control of the Waveform μP address space. The System μP can also assert BUSTAKE during diagnostics in the event of a Waveform μP failure to release the bus after a BUSREQ is given.

With BUSGRANT asserted HI, the inverted BUSGRANT, $\overline{\text{BUSGRANT}}$ is output by inverter U254B and enables Bus Connect Address Buffers U262, U260, and U564. The enabled buffers connect the System μP address bus and control signal lines to their counterparts from the Waveform μP. The Bus Connect Data Buffer U552, a bidirectional device, is then enabled and directed by control signals from the System μP for data transfers to and from the Waveform μP data bus.

Decoding circultry uses the signals WFRAM, $\overline{\text{MAIN}}$, $\overline{\text{MAIN2}}$, and HMMIO; System-Address bits A3, A4, and AF; and BUSTAKE/BUSGRANT to determine when to enable U552 and connect the System Data Bus to the Waveform Data Bus. The addresses that produce accesses to the Waveform RAM (and require U552 to be enabled) are shown as are noted on the memory map, Figure 3.2. (Also, see "System Address Decode", appearing earlier in this section.)

The Bus Connect Data Buffer is enabled when the output of the dual-input AND-gate U432D steps HI and the output of U254D steps LO. With BUSGRANT asserted HI, the output state of U850A depends on the state of its other input which is controlled by the output of OR-gate U850A. Any HI on U850A's inputs drives its output LO. This LO output holds the output of U432D LO and U552 disabled HI via U254D.

One input to U850A is $\overline{\text{BUSGRANT}}$. Since BUSGRANT is HI, $\overline{\text{BUSGRANT}}$ is LO a few nanoseconds after BUSGRANT enables. While HI, $\overline{\text{BUSGRANT}}$ holds U850A's output LO, preventing transients from enabling the Bus Connect Data Buffer. After the few nanoseconds $\overline{\text{BUSGRANT}}$ has no effect on decoder operation.

If the address-bit AF is HI at the input to NOR-gate U850A, the address on the System Address Bus is between 8000h-FFFFh. These addresses map only to System ROM; therefore, the access cannot be a Waveform Processor access. The HI AF-bit at the input to U850A holds its output LO and, via inverter U254D, the Bus Connect Data Buffer is disabled.

If either $\overline{\text{MAIN}}$ or $\overline{\text{MAIN2}}$ are LO, the System Processor is accessing the 4000h-4FFFh or 7000h-7FFFh address space, and WFRAM determines whether the access is to the Waveform RAM space. If WFRAM is disabled LO at the inputs to OR gates U840A and U840B, one of the outputs of those gates will be LO, depending on which signal, $\overline{\text{MAIN}}$ or $\overline{\text{MAIN2}}$, is also LO. The LO output will be inverted HI by either U254C or U254F, and the output of NOR-gate U850A will be LO. Again via inverter U254D, the Bus Connect Data Buffer is disabled.

If WFRAM is enabled HI, the outputs of both U840A and U840B are HI and are inverted LO by UU254F and U254C, respectively. Since this is not a System ROM (AF-bit) or a HMMIO access, the rest of the inputs of U850A will be LO and the output of U850A will go HI. The Bus Connect Data Buffer will be enabled by the LO at the output of inverter U254A.

If HMMIO is HI at the input to U874B, the access is for the 6000h-6FFFh address space. Whether or not the access connects the System Processor the the Waveform Data Bus depends on System Address Bits A3 and A4.

For 6000h-6FFFh addresses in the eight upper ranges (6018h-601Fh, 6038h- 603Fh, etc.), both bits are HI; for the eight lower address ranges (6000h-6017h, 6020h-6037h, etc.), at least one of the bits will be LO. With one or both of the A3 and A4 bits LO at NAND-gate U874D, its output must be HI. This HI is coupled to one input of NAND-gate U874B (the other input of U874B is held HI by HMMIO) and its output is forced LO. This output is connected to the input of U874A, an inverter-configured NAND-gate, and holds the output of the device and the input to NOR-gate U850A HI. The Bus Connect Data Buffer is held disabled as previously described.

If both A3 and A4 are HI, NAND-gate U874D's output goes LO. This LO drives the output of of NAND-gate U874B HI and the output of U874A LO. With the other inputs to U850A LO, its output goes HI and enables the Bus Connect Buffer via U254D.

To summarize, the conditions that must be present for the decoding circuitry to produce an enable to the Bus Connect Data Buffer are:

1. $\overline{\text{BUSGRANT}}$ LO—Waveform μP has relinquished the busses;

2. $\overline{\text{MAIN}}$ and $\overline{\text{MAIN2}}$ HI—This is not a "System RAM" Main Memory access;

3. Address bit AF is LO—This is not a "System ROM" access, and either:

   a. HMMIO is LO—The address is not a System μP memory-mapped I/O location, or

   b. It is a memory-mapped I/O location and address bits A3 and A4 are HI (the address is within the top eight I/O addresses ranges of the System μP).

Addresses residing in the System μP memory space should not access the Waveform μP memory space, and are thus excluded from access by U850A and the associated input logic gates. Addresses not excluded will cause a System μP access into the Waveform μP memory space.

Waveform μP ROM

The Waveform μP ROM consists of two 8K-×-8-bit ROM devices connected in parallel to form an 8K-×-16-bit storage memory for Waveform μP waveform data handling commands. The Waveform μP "double-fetches" data from this ROM space by reading in two 16-bit bytes of command data during each Waveform μP clock cycle. This method of reading the commands makes the Waveform μP command memory space look like a 4K-×-32-bit ROM. The 32-bit instruction word formed by the two fetches adequately defines any Waveform μP operation and allows the Waveform μP to execute one instruction for each 2.5 MHz clock cycle.

The chip-select pins of Waveform μP ROMs, U480 and U490, are both connected to a +5-V supply through

R376. During normal operation, Waveform KERNEL jumper (P128) is installed, and the chip selects of both ROMs are shorted to ground and are constantly enabled.

The addresses of instructions to be read are determined by the 12 instruction-address bits output from the Waveform μP and by the state of the 5-MHz clock. The 12 address bits from U470 are the most significant address bits for any given instruction. The 5-MHz clock applied to ROM address inputs A0 through delay line DL580 and associated components delays the least significant address bit enough delay to provide the needed data-hold time. The state of the 5-MHz clock will be LO to access the first 16 bits of an instruction word. The state of the A0 address line then goes HI, and the second half of the 32-bit instruction is obtained from the next higher memory location. This address selection scheme is the "double-fetch" of instruction data mentioned previously in the Waveform μP description.

Removing jumper P128 disables the Waveform ROMs and places their outputs into the high-impedance state. The pull-up and pull-down resistors within resistor packs R474 and R590 place a "NOP" (no-operation) instruction byte on the instruction bus. A NOP command causes the Waveform μP to increment through the first 12 bits of its address range on the 16-bit DAD bus and through all the addresses of its IA bus. This "KERNEL" mode allows the Waveform μP address bus and address decoding to be exercised for troubleshooting and diagnostic purposes.

Address Decode

The Address Decode circuit monitors the Waveform μP address bus to develop the appropriate enabling signals to the memory or I/O device that is to be accessed.

Block decoding is done by one-of-eight decoder U570, which uses address lines WAC-WAF to separate the addresses below 32K into eight 4K blocks. Decoder U570 is enabled when a valid address (WVMA HI) below 32K (address bit WAF LO) is placed on the memory address bus by either the Waveform μP or the System μP. The next three lower address lines (WAE, WAD, and WAC) determine which one of the eight outputs of the Decoder will be selected. Table 3-4 illustrates this address decoding.

ADDRESSES 0000h-1FFFh. Accesses in this 8k Block are mapped to U350, the Save RAM. fHU570, a 1-of-8 decoder, outputs a LO at either Y0 or Y1 for all addresses within this block and HIs on Y2-Y7. A LO at either Y0 or Y1 causes AND-gate U580C (functioning as a negative-logic OR gate) to output a LO $\overline{\text{SAVE}}$ enable. This LO is inverted twice via Q244 and Q332 and holds the chip-select input of Save RAM U350 enabled LO. Since this address block is the only block that accesses the SAVE memory, when other address blocks are decoded by U570 (in the descriptions to follow), Y0 and Y1 are HI and U350 disabled via Q244 and Q332.

NOTE

The chip-select circuit between the $\overline{\text{SAVE}}$ output of U580C and RAM U350 is identical to that for the System μP RAM (U664, diagram 1). The circuit determines chip selection during normal operation and isolates the Save RAM chip-select input when power is off. See the descriptions in "Battery" and in "Battery-Backup for Save Memory" for more information.

Writing to or reading from any of the Waveform μP RAM space is done via bidirectional Bus Buffer U352. When Save RAM U350 is selected by the $\overline{\text{SAVE}}$ line going LO, U352 is also enabled via AND-gate U580D. The state of the $\overline{\text{WWR}}$ (waveform write) control line determines the direction of the data transfer.

ADDRESSES 2000h-4FFFh and 6000h-6FFFh. Addresses in these ranges select either Y2 ($\overline{\text{DISP}}$), Y3 ($\overline{\text{DATT}}$), Y4 ($\overline{\text{ACQ}}$), or Y6 ($\overline{\text{WHMMIO}}$). $\overline{\text{DISP}}$, $\overline{\text{DATT}}$, and $\overline{\text{ACQ}}$, are used to select the Display and Display Attribute Memories (diagram 16) and the Acquisition Memory (diagram 8) respectively. WMMIO (Waveform Memory-Mapped I/O) is used to select the Register Decoding Circuitry.

With the output of U580C HI for all accesses in this group, Y0 and Y1 hold Save RAM U350 disabled (see "ADDRESSES 0000h-1FFFh" discussion). The HI $\overline{\text{SAVE}}$ also holds the input to U580D HI; the other input to U580D is held HI by the output of U432A. The output of U432A is HI because one of its inputs is held HI by Y5 and the other held HI by Y7 (via OR-gate U132C). The HIs at both inputs to U580D hold the Waveform Data Buffer disabled for all accesses in this group.

When WMMIO (6000h-6FFFh) is decoded LO, decoder U540 is enabled. U540 operates similarly to U570 and uses address lines WA0-WA4 to produce its various I/O enabling outputs. Address bits WA3 and WA4 are used as chip selects and cause the output of U540 to fall into the eight locations immediately above those of Decoder U884 (diagram 1) for System μP memory-mapped I/O.

Table 3-4
Waveform μP Address Decoding

ADDRESS BITS			OUTPUT SIGNAL (Active LO)
WAE	WAD	WAC	
LO	LO	LO	(Y0 or Y1) SAVE from NAND-gate
LO	LO	HI	U580C to enable the SAVE memory.
LO	HI	LO	(Y2) DISP—Selects display memory.
LO	HI	HI	(Y3) DATT—Selects attribute memory.
HI	LO	LO	(Y4) ACQ—Selects acquisition memory.
HI	LO	HI	(Y5) WPCMDN/COEFF—Selects either the command or the coefficient memory.
HI	HI	LO	(Y6) WMMIO—Enables Waveform μP memory-mapped I/O Decoder U540.
HI	HI	HI	(Y7) WPRAM2—Decoded to enable waveform processor RAM U440.

The outputs of U540 allow the accessing processor to read the display status ($\overline{\text{SSREG}}$), to read the two-byte address of the last-acquired point ($\overline{\text{RDMAR0}}$ and $\overline{\text{RDMAR1}}$), or to latch the present interrupt status ($\overline{\text{COMREG}}$). (See the "Display Status Register" and "Interrupt Latch" descriptions for further explanation.)

ADDRESSES 5000h-5FFFh. This 4K block of addresses is decoded as an access to the Waveform Processor Coefficient-Temp Memory in RAM U440. With a 5XXXh address, U570 decodes WPCMDN COEPF LO and sets its other 7 outputs HI. The LO at the input to AND-gate U432A holds its output LO, and this LO holds U440 enabled for access. (The HI $\overline{\text{SAVE}}$ disables U350 as previously described).

The LO at the output of U432A is also coupled to the input of U580D. With a LO at the input to this AND-gate, its output is LO and U352, the Waveform Data Buffer, is enabled to connect the Waveform Data Bus to the Waveform Processor RAM.

ADDRESSES 7000h-7FFFh. Addresses in this range select WFRAM2 LO. Assuming BUSGRANT and WFRAM are both LO at the inputs to XOR-gate U130A, both inputs to OR-gate U132C are LO and its output is also LO. This LO forces the output of U432A LO and enables U440 RAM. The same LO also enables the Waveform Data Buffer via U580D to connect the Waveform Data Bus to the Waveform Processor RAM.

The System Processor can also access this address bus by asserting BUSGRANT and WPRAM HI. The two HI inputs to XOR-gate U130A produce a LO at its output. The Waveform Data Buffer is enabled and the Waveform Data Buffer are enabled as was just described for the Waveform Processor access for this address group. BUSGRANT disables the Address Latches for the Waveform Processor and is inverted to enable the Bus Connect Circuitry to connect the System Address Bus to the Waveform Address Bus. The Bus Connect Data Buffer is enabled to connect the System Data Bus to the Waveform Data Bus.

Waveform μP RAM

The Waveform μP RAM is used for storage and manipulation of waveform-display data. The RAM space is divided up into four memories consisting of the 8K-×-8-bit "Save Memory" RAM space, the 2K-×-8-bit "Command-temp" RAM space, the 2K-×-8-bit "Coefficient" RAM space, and the "Interpolation" RAM space.

The 8K-×-8-bit Save Memory, U350, is where the Waveform μP places acquired waveform data that should be retained with power off. Waveforms stored in the Save RAM are retained for up to three years at room temperature with the power off by the Battery Backup System (see "Battery" in this section.

The 8K-×-8-bit RAM, U350, is where the Command-Temp, Coefficient, and Interpolation RAM spaces reside. The Waveform μP uses the Commmand-Temp RAM space for storage of commands to the Waveform μP from the System μP and for temporary scratch-pad storage of display calculations in process. The Coefficient RAM space is used only for further scratch-pad storage. Interpolation RAM is used for storing interpolation calculation used for the MEASURE feature of this scope.

Reading from and writing to the Waveform μP RAM selected by the Address Decode circuit are controlled by the $\overline{WRD}$ (waveform read) and $\overline{WWR}$ (waveform write) signals respectively.

RAM Buffer

The RAM Buffer U352 allows data transfers to and from the Waveform μP RAM to take place. The buffer is enabled by U580D when any of the Waveform μP RAM locations are addressed. Buffer direction is determined by the $\overline{WWR}$ level.

Battery-Backup for Save Memory

The waveforms stored in Save Memory U350 are maintained when the power is off. The Battery-backup Circuit previously described provides supplies power to Save RAM U350, as well as System RAM while power is off. For operation of this circuit see "Battery" in this section for more information.

As was true for the chip-select circuitry for System ROM, undefined operations on the address bus can cause the chip-select circuit enable U350 as the power supplies are brought up at power-on. To prevent this, the base circuit of Q332 through diode CR244. This LO keeps the transistor biased off and U350 is disabled until the power-up $\overline{RESET}$ signal returns HI; at which time the data on the address bus is stable.

Display Status Register

Display Status Register U542A allows the controlling processor (System μP or Waveform μP) to read the status of the Display System operations. The address-decoded $\overline{SSREG}$ (sub-system status register) line from Decoder U540 enables buffer U542A to place the DISDN (display done) and ACQDN (acquisition done) signals on the WD bus where they may be read. These status bits are used by the reading μP to determine when to execute the next phase of a display or acquisition sequence.

Interrupt Latch

The Interrupt Latch (U550) allows the Waveform μP operations to interrupt the System μP for servicing and, when servicing is completed, allows the System μP to reset the interrupt.

To write data into the latch, the controlling μP addresses location 6019h, causing the $\overline{COMREG}$ line from U540 to enable U550. Data from the WD bus is written into the latch on the rising edge of the $\overline{WWR}$ pulse. The Q output from pin 2 (MDISDN) of the latch is applied to AND-gate U580B (diagram 1) where it either masks the DISDN (display done) interrupt from the System μP when it occurs or lets the interrupt pass. Masking the DISDN interrupt from the System μP permits the Waveform μP to have first access to the Display System for display updates before the System μP sees that the Display System is finished with its last task. The next bit is unused. The Q output bit on pin 10 is the WPDN (waveform processor done) interrupt and provides the Waveform μP with a way of telling the System μP that it is done with its assigned task and is ready to accept another. The output bit on pin 10 is applied to Display Status Register U542A and is used for write-readback verification of U550 and U542A during the self-check and other diagnostic routines.

FRONT PANEL PROCESSOR

The Front Panel Processor (diagram 3) monitors the settings of the pots and switches of the Front Panel (diagram 4) and the Auxiliary Front Panel (diagram 6). The Front Panel μP allows quick system response to changes in front-panel settings without excessive use of time by the System μP. The Front Panel Processor system consists of the microprocessor integrated circuit with a built-in RAM, ROM, and A/D converter (for digitizing the potentiometer wiper voltages); the handshake logic between the System μP and the Front Panel μP (to synchronize data transfer between processors); and the data bus interface to provide the actual data transfers between busses.

Front Panel μP

Front Panel μP U700 does the reading of the front-panel pots and switches. It continuously scans the front-panel control settings and compares them against the values stored in its internal RAM. When a change is detected, the Front Panel μP issues an interrupt to the System μP. The System μP then handles the interrupt and reads the changed data from the Front Panel μP to update its control-setting values. The Front Panel μP also updates the current value list stored in its RAM for further use.

Front Panel μP U700 is externally clocked by the 4 MHz system clock applied to the external clock input (EXTAL). Initially, the LO state of $\overline{FPRESET}$ on the INT_2 input (pin 18) will clear all the internal registers of the Front Panel μP. When $\overline{FPRESET}$ goes HI, the μP executes the power-up self-test instructions stored in ROM space within the μP integrated circuit. When the self test has completed, the Front Panel μP sends the diagnostic result byte to the System μP and branches to its main program. The main program routine sets up the data direction for the various port lines, sets the AN0-AN3 (analog inputs 0-3) to their analog input mode, and receives the eight front-panel configuration bytes from the System μP that define the manner in which the various front-panel switches and pots operate. It then begins scanning the front-panel pots and switches for their initial settings. After the initial values are determined and stored, the Front Panel μP sends those coded values back to the System μP in an 11-byte message (10 data bytes plus an end-of-message byte) to update the front-panel information held by the System μP. It then begins scanning the front-panel controls for changes from the currently stored front-panel values.

To read front-panel pot settings, the internal A/D converter of the Front Panel μP performs an 8-bit, successive-approximation conversion of the analog levels applied to the AN0 and AN2 inputs by a selected potentiometer. These analog input signals come from 8-input analog multiplexers U902 on the Front Panel (diagram 4) and U600 on the Auxiliary Front Panel (diagram 6). A specific pot to be read is selected by the multiplexer under control of the MUXSEL0, MUXSEL1, MUXSEL2, and MUXINH (multiplexer inhibit) output lines from the Front Panel μP. These select signals, in combination with the selected A/D (AN0 or AN2) input, define the pot being read. The voltages monitored on the AN1 and AN3 analog inputs are also digitized by the internal A/D converter to detect Main board temperature (MBTEMP) changes (not used at this time) and if lithium backup battery BT800 (diagram 1) is either low (needing replacement) or being charged (not allowed).

To read the front-panel switches, the Front Panel μP first sets one of the front-panel switch-matrix rows LO, using the MUXSEL0-MUXSEL2 outputs. It then sets its $S/\overline{L}$ (shift/load) output on pin 29 LO. The LO does a parallel load of the switch-closure data into shift registers U904 (diagram 4) and U700 (diagram 6). The shift/load line is then set HI (shift mode), and eight shift clocks (SHCLK) are generated to move the switch-closure data serially onto the SW OUT (front-panel switch data out) or the SW OUT A (auxiliary front-panel switch data out) lines, where it is read by the Front Panel μP. This cycle is then repeated for the seven remaining rows of the matrix to read all the switches.

When the Front Panel μP detects a change in either a switch or a pot setting from its currently stored values, it places a code identifying which control setting changed on its PA0-PA7 outputs, and it then sets the WRTOHOST (write to host) signal HI to clock Handshake Logic flip-flop U861B. The resulting HI on the Q output of the flip-flop is the front-panel interrupt (FPINT) to the System μP, telling it that the front-panel settings have been changed.

The System μP handles the interrupt by reading the byte from the Front Panel μP; and then, via the Handshake Logic, it resets flip-flop U861B to remove the interrupt and set HOSTDNRD (host done reading) HI. This signals the Front Panel μP that the System μP has read the code identifying the changed control. The Front Panel μP then places the new control-setting value on its output bus and reasserts the front-panel interrupt using the WRTOHOST line to again clock flip-flop U861B.

The System μP then reads the changed-data bytes for the identified control(s) (either three bytes or five bytes depending on whether one or two control changes are being sent) and reasserts HOSTDNRD. Changes of up to two controls are remembered by Front Panel μP U700 so that if the System μP is busy, the control changes are not lost while the Front Panel μP is waiting to make the transfers. If more than two controls are changed before the System μP has time to read the changes, the oldest change is written over and lost.

The $\overline{\text{WRTOFP}}$ (write to front-panel processor) input to U700 at pin 3 is set LO (via the Handshake Logic) when the System μP wants to input data to the Front Panel μP. The Front Panel μP then reads one byte of data from the System μP in a manner similar to that just described for transfers from the Front Panel μP to the System μP. This mode allows the System μP to change the current control configuration list stored in the limited RAM space of the Front Panel μP. This list defines how the operation of pots and switches is to be interpreted (for example, momentary contact or toggle switches).

Jumper J155, connected to the PC_7 and PD_7 inputs, is used to enable diagnostic test routines that verify functionality of U700. The test routines may also be used to troubleshoot the Front Panel Processor system. These tests are explained in the Diagnostics portion of the "Maintenance" section of this manual.

Handshake Logic

The Handshake Logic circuit, formed by NOR-gates U862A, B, C, and D and flip-flops U861A and B, controls and synchronizes data transfers between the System μP and the Front Panel μP.

Data transfers between the two processors are initiated by interrupts that signal the destination processor that service is requested. When the Front Panel μP has changed-value data to give to the System μP, it will place the data bytes to be given to the System μP on its PA_0-PA_7 (port A—bits 0 through 7) outputs. It then asserts WRTOHOST (write to host) HI, clocking the FPINT (front-panel interrupt) at the Q output of U861B HI.

Depending on what the System μP is doing, it may either service the interrupt request immediately, or it may wait for time to be available. When it responds to the interrupt, it does a read of the Front Panel "register" at address 6209h. The decoded $\overline{\text{FPREG}}$ signal from Trigger Holdoff Decoder U781 (diagram 12) allows OR-gates U862B and U862C to pass the $\overline{\text{WR}}$ or $\overline{\text{RD}}$ signals. For a read, both input pins to U862B are LO, causing the output of U862A to go LO. This enables buffer U751, placing the data from the Front Panel μP on the System μP data bus (FP0-FP7) and, at the same time, resets flip-flop U861B. Resetting U861B removes the front-panel interrupt and sets HOSTDNRD (host done reading) to U700 HI.

When the System μP needs to write to the Front Panel μP, it writes data to address 6209h. This latches data from the System μP data bus into register U742. The enable to U742 is via U862C. The latch enable also resets the Q output of flip-flop U861A LO via U862D to produce the $\overline{\text{WRTOFP}}$ (write to front-panel) interrupt to U700. Latching data into U742 immediately frees the System μP to resume other tasks, since it doesn't have to wait for the Front Panel μP to service the interrupt.

When U700 services the interrupt by the System μP, it sets $\overline{\text{FPRD}}$ (front-panel reading) LO and enables the latched data in register U742 onto the Front Panel data bus. It then reads the data into its internal registers and asserts FPDNRD (front-panel done reading). FPDNRD going HI clocks the $\overline{\text{FPDNRD}}$ status bit from flip-flop U861A pin 6 HI to signal the System μP that it is done reading the byte and removes the $\overline{\text{WRTOFP}}$ interrupt present on U861A pin 5. Each data byte transfer from the System μP to the Front Panel μP and vice versa is done using the two handshake routines just described.

Trigger Status Indicators

The Front Panel Trigger Status Indicators provide visual information regarding trigger slope and trigger status to the user. Data written to LED Register U741 from the System μP turns on the LED that reflects the current trigger status. A LO output from U741 turns on the associated LED. The LED Register is enabled by a System μP write to address 6208h. Trigger Holdoff Decoder U781 (diagram 12) produces the decoded $\overline{\text{LEDREG}}$ signal that enables data at the input pins to be latched when the $\overline{\text{WR}}$ clock goes HI.

FRONT PANEL CONTROLS

The Front Panel is the operator's interface for controlling the user-selectable oscilloscope functions.

All of the Front Panel controls (diagram 4) are "soft" controls in that they are not connected directly into the signal path. Therefore, associated circuits are not influenced by the physical parameters (such as capacitance, resistance, and inductance) of the controls. In addition, converting the analog output levels of the potentiometers to digital equivalent values allows the System μP and the Front Panel μP to handle the data in ways that enhance control operation.

The variables defining the current settings of the control pots and the front-panel switches are stored and continually updated in Nonvolatile RAM U664 (diagram 1) by the System μP. The data remains stored when the oscilloscope is turned off so that when the scope is turned on again the System μP returns to the same front-panel setup that was present when the scope was turned off.

Front-Panel Switch Scanner

The Front Panel switches are arranged in an electrical array of eight rows and six columns. Switches are placed at row-column intersections, and when a switch is closed, one of the row lines is connected to one of the column lines through an isolation diode. Checking for switch conditions (open or closed) is done by setting a single row line LO and then sequentially checking the six columns to determine if a LO is present on any of the column lines. After each column line in a row is checked, the current row line is reset HI and the next row line is set LO to check the next six columns. A complete check of the front-panel switches consists of setting all eight row lines LO in order and performing a six-column scan for each column to check for a LO.

A row is selected for checking by the Front Panel μP (U700, diagram 3) when it switches the MUXSEL lines (0-2) applied to multiplexer U903 to set a row line LO. To check the columns, the processor pulses its S/$\overline{\text{L}}$ (shift/load) select line to shift register U904 first LO and then HI. This causes a parallel load of the six column-line bits (plus the seventh and eighth bits tied HI by R934) into the shift register. The processor then generates eight shift clocks (SHCLK) to U904, serially shifting the switch data out on the SWOUT (switch data out) line. The serial data bits are applied to the PB0 input (pin 25) of the Front Panel μP to be checked. Any LO bits in the column-line data tell the μP that a switch is closed. Since the Front Panel μP knows which row line it set LO, it can determine from the position of the LO bits in the serial data string which of the switches are closed.

In addition to the front-panel push-button and continuous-rotation switches connected in the switch array, there is a rate switch associated with the Horizontal Position, the CH 1 Vertical Position, the CH 2 Vertical Position, and the Cursor Position potentiometers. These switches are normally closed in the center positioning range of the associated pot. When the pot is rotated in either direction out of this range, the rate switch opens. The open switch signals the Front Panel μP that the associated control function has changed from normal (absolute) positioning to a faster, rate-change positioning mode. Rotating the pot still further into the rate region causes the associated on-screen display position to change at a still faster rate. When the pot position is returned to its center range (rate switch closed), further positioning of the associated display occurs from where the rate function positioning left off.

Pot Scanning

The Pot Scanning circuitry, working together with the A/D converter internal to Front Panel μP U700, produces digital values for the wiper voltages of the front-panel potentiometers and for the voltages monitored by the auxiliary front-panel circuitry. Analog multiplexer U902 selects which of the eight front-panel pots are read. (Trigger Level control R902 and Holdoff control R901 are continuous-rotation potentiometers made up of two separate resistive elements each.) Analog multiplexer U600 (diagram 6) selects the auxiliary front-panel value to be read.

Three MUXSEL control lines to multiplexers U902 and U600 select the pot or value to be read. The analog voltage level at the wiper of the pot selected by U902 is output at pin 3 (AOUT0) and is applied to the Front Panel μP at pin 21 (analog input AN0). Analog voltages selected by multiplexer U600 are applied to analog input AN2. The voltage levels at these inputs are digitized, and the amount and direction of changes from the previously stored values are calculated. Changed values are stored in the internal RAM of U700 for comparison during future scans, and the change data is then relayed to the System μP. That change data is used by the System μP to update its current control settings and pot values list and to update the front-panel variables in Nonvolatile RAM U664.

SYSTEM DAC AND ACQUISITION CONTROL REGISTERS

The System DAC and Acquisition Control Registers circuitry (diagram 5) is used to set various analog reference voltages throughout the instrument and controls such things as preamplifier gain, vertical position and centering, trigger levels, holdoff time, common-mode rejection, graticule illumination, and CCD offsets.

The System DAC portion of the circuitry consists of a data latch that stores the digital value to be converted, a D/A converter that does the actual conversion, a multiplexer system to route the resulting analog voltage to the proper control circuit, and a sample-and-hold system that stores the analog levels between updates. Much of the multiplexing and sample-and-hold circuitry is shown in diagram 6, System DAC (cont) and Auxiliary Front Panel.

The other portion of diagram 5 is the Acquisition Control Registers circuitry, used by the System μP to set up the acquisition and triggering modes. The System DAC portion is described first.

D/A Converter

The D/A Converter stage, U860, converts the digital value written into registers U850 and U851 by the System μP into two complementary output currents. (Complementary in this case means that the sum of the two currents equals a predefined value.) The digital data bits to be converted are serially clocked into the shift register from data bus line D7 (via U280). Sixteen data bits are sequentially placed on data bus line D7 and clocked into the shift register on the rising edges of 16 $\overline{\text{WR}}$ pulses (clock is via U280A and U280B). As the bits are being loaded into the registers, the DAC output current does not correspond to any useful value, but the multiplexers used to direct that output to the following stages are not enabled during loading. After all 16 bits have been clocked into the register, the inputs to DAC U860 will be at their proper levels and the DAC outputs will be valid levels. One of the multiplexers may then be enabled by the System μP using the DAC MUX enables via register U272.

Only the first 12 bits (DAC0 through DAC11) of the 16 bits loaded into the registers for are used for conversion data. The next three higher bits are used as 1-of-8 select bits to the four analog multiplexers that route the DAC output voltage to the proper Sample-and-Hold circuit. And finally, the MSB of shift register U851 is used in a write-readback operation that allows the operation of registers U850 and U851 to be checked by the System μP during self checks and diagnostics.

The magnitude (range) of the DAC output currents is set by the voltages applied to pins 14 and 15 of U860. Pin 15 V_{REF-} is tied to ground through R761. The reference voltage to pin 14 is applied via a voltage divider (R760 and R860) between the +10 V_{REF} supply and the output of the DAC Gain Sample-and-Hold, U660. The System μP enables self-calibration of the gain of U860 via this Sample-and-Hold circuit. Gain changes are explained in the discussion of the DAC Gain Self-Calibration circuit.

DAC I-TO-E CONVERTER. This circuit changes the differential output currents from DAC U860 into a single-ended output voltage that is routed to a selected Sample-and-Hold circuit via one of the analog multiplexers.

The output currents from DAC U860 develop a voltage drop across the resistive networks at the inputs to operational amplifier U661C. The equivalent input impedance at both inputs is approximately 200 ohms; so, when both currents are equal (middle range of the DAC), the output voltage of operational amplifier U661C will be close to zero volts. An offset current is added to the non-inverting input node via R666 to precisely set the midrange value to zero volts. The gain of U661C is set by the ratio of R663 to R664, and the (calibrated) output voltage ranges from −1.36 V to +1.36 V.

DAC OFFSET. The DAC Offset level is self-adjusting and is updated via DAC Offset Sample-and-Hold U650 each time the DAC System cycles through its DAC channels to update its control levels.

At the beginning of each DAC-update cycle, the System μP writes 0800h to DAC input shift registers U850 and U851; this corresponds to zero volts (center of the DAC range). The DAC output currents representing zero volts are converted by the DAC I-to-E Converter U661C to a voltage that is applied to U650 via multiplexer U651. Any deviation from the desired zero-volt level causes the output of U650 (configured as an inverting integrator) to shift slightly. This applies an offsetting voltage to DAC I-to-E Converter U661C via R666 and R665 to bring its output level back to precisely zero volts.

Capacitor C655 holds the offset level constant between update cycles (every 64 ms) to keep the proper offset for the entire DAC cycle. By updating the offset every 64 milliseconds, offset variations that would otherwise occur over time and temperature changes are eliminated.

DAC GAIN. The DAC Gain is set during each DAC-update cycle immediately after DAC Offset is set and keeps DAC gain constant with time and temperature changes.

To set the DAC Gain, the System μP loads 0F59h into DAC input registers U850 and U851 and routes the resulting output voltage to DAC Gain Sample-and-Hold U660 via multiplexer U651 pin 2. A digital input of 0F59h to the DAC is supposed to produce an output of +1.25 V from U661C. The resulting DAC output is compared to a +1.25 volt reference by operational amplifier U660. Any deviation from the correct +1.25 V level produces a gain-correction voltage applied to the DAC via R760. Capacitor C662 maintains the correction voltage between DAC update cycles.

Multiplexer Select

The Multiplexer Select circuit, composed of addressable latch U272 and the associated decoding gates, provides the enabling signal that selects one of the four 1-of-8 multiplexers to route the DAC output voltage to the Sample-and-Hold circuits. Data applied to the D input of U272 from data bus bit $\overline{\text{D7}}$ (via U280D) is latched to the addressed output pin as determined by the logic levels on the A, B, and C select lines (A0 through A2). The input data is written to the addressed output on the falling edge of the enable signal at pin 14 (via U280A and U280C). The logic state written to the output remains latched when the enable signal returns HI. The states of the unaddressed outputs remain unchanged. To enable the latch, NOR-gate U280A (functioning as a negative-logic NAND-gate) needs the $\overline{\text{DACSEL}}$ (DAC select) line LO to produce a HI output. That HI is inverted by U280C to enable the Multiplexer Select register to be written into. That same LO $\overline{\text{DACSEL}}$ is applied to NOR-gate U280D to enable it to pass the data on the D7 line to the D input of U272 and to the DAC input register, formed by U850 and U851.

Multiplexer U651, when enabled by Multiplexer Select Latch U272, routes the analog output voltage from DAC I-to-E Converter U661C to one of eight Sample-and-Hold circuits, depending on the output specified by the logic states on the its select inputs. Selection is determined by three bits clocked into DAC Register U851 as described in the preceding D/A Converter discussion. One of three other multiplexers, shown in diagram 6, may be enabled instead of U651 to pass the DAC output to one of the Sample-and-Hold circuits on their outputs (also shown in diagram 6).

Sample-and-Hold

The eight Sample-and-Hold circuits shown on diagram 5 (formed by U641A through U641D, U650, U660, U661A, U661B and their associated components) store and buffer the analog voltage levels directed to them by multiplexer U651. Each of the operational-amplifier circuits selectable by U651 (except the DAC Offset and DAC Gain operational amplifiers, U650 and U660 respectively) has a hold capacitor on one input that is charged up to the DAC output voltage level through the selected multiplexer channel. When the multiplexer channel is then deselected, the capacitor holds the voltage at a fixed level so that the associated Sample-and-Hold circuit provides a steady voltage level to the circuit it controls. Voltage gain of the Sample-and-Hold operational amplifiers range from more than 4.5 in the CH 1 and CH 2 Gain-Cal circuits down to 2 in the

Jit 1 Gain and Jit 2 Gain amplifiers and down to about 1 for the CH 1 and CH 2-BAL voltage followers. The Jitter Gain circuits (formed by U661A and U661B) produce a negative 5 V dc offset voltage at their output pins as their gain-setting resistors are referenced to the +5 V supply. The DAC Offset and DAC Gain Sample-and-Hold circuit operations are described in the previous D/A Converter discussion.

Acquisition Control Registers

Mode control of the analog acquisition system and trigger circuitry is controlled by the System μP via shift registers and a decoder. The System μP, through its address decoding circuitry, enables Decoder U271 to produce a shift register clock at one of its eight outputs. These clock signals are used to move serial data from the ACD (acquisition control data) line, U272 pin 5, into one of the various Acquisition Control Registers, of which three are shown in diagram 5. They are Peak Detector Control Register U530, Gate Array Control Register U270, and Trigger Source Control Register U140. Other registers clocked are the Channel 1 and Channel 2 Control Registers (U510 and U220 on diagram 9), the internal control registers of the CH 1 and CH 2 Preamplifiers (U420 and U320 on diagram 9), and the internal control registers in the A/B Trigger Generator (U150, diagram 11).

The ACD line is shared by all the Acquisition Control Registers; the selected clock determines which register will be loaded with the data being written by the System μP. Decoder U271 is enabled when the $\overline{\text{ACQSEL}}$ and $\overline{\text{WR}}$ lines are LO and address line A3 is HI. Address lines A0, A1, A2 determine which of the output lines produces the clock signal. A data bit present on the ACD line (previously written to latch U272 in a DAC write cycle) is loaded into the clocked register on the rising edge of the $\overline{\text{WR}}$ signal as U271 becomes unenabled and its selected LO output goes HI. Each bit to be loaded must be successively written to U272 then moved into a register by the output clock from U271.

SYSTEM DAC (cont) AND AUXILIARY FRONT PANEL

The DAC multiplexing and sample-and-hold circuits included in diagram 6 operate similarly to those described in the DAC System (diagram 5) discussion. The analog voltage output from the DAC I-to-E Converter is routed through one of the three additional multiplexers (shown in diagram 6) to several types of hold circuits.

DAC Multiplexers

DAC Multiplexers U821, U830, and U831 route the analog output voltage from DAC I-to-E Converter U661C (diagram 5) to the various Sample-and-Hold circuits. Operation of each multiplexer is identical to that of Multiplexer U651, previously described in the System DAC circuit discussion. Each multiplexer is individually enabled by a bit from Multiplexer Select Latch U272, and signal routing through the enabled device is controlled by the three select bits applied to it from the three most significant bit outputs of DAC Register U851.

Sample-and-Hold

A separate Sample-and-Hold circuit is associated with each of the multiplexer outputs. An analog voltage routed from the DAC I-to-E Converter through the selected multiplexer channel charges up the hold capacitor at the input of an operational amplifier in the selected Sample-and-Hold circuit. When that multiplexer channel is deselected, the voltage level is held on the capacitor because of the high-impedance discharge paths presented by the multiplexer output and the operational amplifier input. The individual operational amplifiers are configured as buffers with voltage gains varying from −0.47 to +10, depending on the requirements of the function that is being controlled. The CH 1 and CH 2 Position Sample-and-Hold circuits also provide a dc offset of their output levels to properly bias the inputs they drive.

Cal Signal Amplifier

The Cal Signal Amplifier (U610) operates in a manner similar to the Sample-and-Hold circuits just described. It is used to supply test signals to the CAL inputs of the CH 1 and CH 2 Peak Detectors (U440 and U340, diagram 10) for Self Calibration of the acquisition system. The test signal level, stored on capacitor C733, is applied to the input of an amplifier internal to U610 which has dual-differential outputs. The complementary-current outputs for each channel are approximately 6 mA ±1.25 mA.

Z-Axis Control

The Z-Axis Control stage consists of Q810, U811, U810A, U810B, five-transistor array U812, and associated components. Multiplexer U811 selects one of three intensity-control voltages—normal, intensified, or readout (output from Sample-and-Hold buffers U820B, U820C, or U820D) and routes it to a current source composed of U810A, U810B, and Q810. The amount of current passed by Q810 controls the display intensity. The transistors in array U812 form an automatic gain compensation circuit for Z-Axis Amplifier U227 (diagram 19).

Selecting an input to pass through multiplexer U811 is done by two active input signals, BRIGHTZ and RO. (The third select input is a permanent LO, so one of the first four inputs only can be selected.) For normal-intensity waveform displays, all select bits will be LO to select input 0 to switch through U811. If the waveform display should be intensified at any time, the BRIGHTZ input will go HI, selecting input 1. When readout is to be displayed, the RO input will go HI, selecting either input 3 or input 4, depending on the setting of the BRIGHTZ bit. Since inputs 3 and 4 are both connected to the INT-RO (readout intensity) control voltage level, the readout displays are not intensified.

The selected intensity control voltage is applied to U810B, configured as an inverting buffer with a gain of −1. The output voltage is offset −4.06 V by the voltage divider at pins 3 and 5 of U810 (R814 and R815) and resistor R816 at pin 6. The resulting inverted and shifted output is converted to a current by R812 and applied to the emitter of Q810.

The circuitry of operational amplifier U810A and transistor Q810 is arranged so that the transistor is on with its emitter held at −2.7 V. The −2.7 V level at the emitter is set by the bias on input pin 3 of operational amplifier U810A. The voltage developed at the output of U810B causes a current to flow in R812 and sets the current drive level for the Z-Axis circuit (diagram 19). This Z-INT drive current supplied via U812E from pin 14 may vary from 0 mA to 4 mA (−1.36 V to +1.36 V respectively at the output pin of multiplexer U811).

When the intensity of the selected display is at minimum, the output control voltage from multiplexer U811 will be below −1.36 V. This causes the output of U810B to go to approximately −2.7 V, reducing the emitter current to Q810 to approximately zero. Diode CR810 limits the reverse-bias voltage across the base-emitter junction of Q810 to about 0.6 volts and protects the base-emitter junction from excessive voltage.

Automatic compensation of the Z-Axis Amplifier gain is carried out in five-transistor array U812. Transistors U812B and U812C form the bias network for U812D, one-half of the Z-Drive compensation amplifier. Biasing for the other transistor of the differential pair is supplied by U812A, R817, and a resistor internal to the Z-Axis Amplifier that is tied to the $+5\ V_D$ supply. The differential amplifier pair is biased so that the total current is divided between the two sides. The resistance value of the internal resistor in the Z-Axis Amplifier is an indication of the gain of that device. Changes in that value that occur between different Z-Axis Amplifiers shift the biasing level of U812E to either increase or decrease the share of the total current through that transistor by a small amount. The change in current is in the appropriate direction to make the display intensity of different instruments comparable with exactly the same Intensity control settings. Capacitor C817 bypasses high-frequency noise present on the ZGAIN signal line.

The SPOTWOB (spot wobble) signal line, at the output of Operational Amplifier U810B, picks off the various intensity levels. Those levels are used in the Horizontal and Vertical Output Amplifiers (diagram 18) to dynamically correct intensity-related position shifts on the crt (described in the Display Output circuitry discussion).

Graticule Illumination

The Graticule Illumination circuit, composed of U820A, U520G, and associated components, sets the brightness of the three lamps used to light up the graticule lines etched on the crt faceplate.

Operational amplifier U820A is configured as an inverting integrator. Inverting buffer U520G may be thought of simply as an open-collector transistor following operational amplifier U820. The circuit appears this way because the negative feedback around the loop via U820 and voltage divider R824-R825 keeps U520G in its linear operating range. Gain around the loop (11) is set by the ratio of R822 to R823 plus 1. The DAC control voltage applied to pin 2 of U820A causes the integrator output to slowly ramp in the opposite direction. This output is inverted by U520G, and it sets the current in the graticule lamps. Between DAC-updates no integration takes place, and the charge held on C822 holds the output of the inverting buffer, and thereby the graticule lighting, constant.

Auxiliary Front Panel

The Auxiliary Front Panel circuitry provides a means of reading the front-panel bezel push buttons, located directly below the crt, as well as several analog voltages associated with the front-panel BNC input connectors. The circuit consist of analog multiplexer U600 (used to route the various analog voltages to the A/D converter), parallel-loading shift register U700 (used to relay switch-closure data to the Front Panel μP, shown in diagram 3), and associated components.

Analog multiplexer U600 routes one of the eight input levels to the A/D converter internal to Front Panel μP U700 (diagram 3), depending on the three-bit code applied to its select inputs. The selected signal may be one of the four probe-coding voltages (developed by the voltage divider formed by the encoding resistance of the probe attached to the input connectors and the associated pull-up resistor within R601), the CH1 OVL (overload) or CH2

OVL levels (used to indicate when an excessive voltage is applied to the input connector), or one of the two, 180 degree out-of-phase wipers on the Intensity control (a continuous-rotation pot).

Auxiliary Switch Register U700 performs a parallel load of the status of all of its input bits whenever the Front Panel μP puts out a SHCLK (shift clock) with the $S/\overline{L}$ (shift/load) select input of the register set LO. Once loaded, the $S/\overline{L}$ input is set HI, and the eight bits of switch-closure data are clocked out to the Front Panel μP on the SWOUTA (switch data out-auxiliary Front Panel) line with eight more clocks applied to the clock input of the Auxiliary Switch Register. Switches read include the five menu select switches on the lower edge of the crt bezel, the Intensity Control SELECT switch, the STATUS switch, and the MENU OFF/EXTENDED MENU switch.

SYSTEM CLOCKS

The System Clocks circuitry (diagram 7) produces the fixed-frequency System clocks signals used throughout the oscilloscope. These clocks are developed from a 40 MHz master clock frequency, and they are used to drive state machines that produce other special-purpose clocks that control the waveform acquisition processes.

Master Clock

The Master Clock circuit produces 20 MHz and 8 MHz clocks ($\overline{\text{C20M}}$ and C8M) by dividing down the output from the 40 MHz crystal oscillator circuit, Y611. The oscillator circuit drives both the divide-by-two flip-flop (U612A) and the divide-by-five circuit (flip-flops U612B, U615A, and U615B) in parallel via inverter U513A. The 20 MHz clock is obtained from flip-flop U612A. With its Set, Clear, J, and K inputs all held permanently HI, the flip-flop toggles on each negative-going 40 MHz clock edge to divide the input clock frequency by two.

The divide-by-five circuit is a state machine formed by J-K flip-flops U612B, U615A, and U615B. With the two feedback signals to the J and K inputs of U612B, the flip-flop chain sets logic level on the J and K inputs of U615B that allows its Q output to change states only every five 40 MHz input clocks to produce the 8 MHz clock.

Jumper J132 allows an external clock signal to be substituted for the 40 MHz clock signal to aid in testing and troubleshooting.

Secondary Clocks

The Secondary Clocks circuit further divides the 20 MHz clock to produce other system clock rates. The flip-flops within U710, along with logic gates U711A, U711B, U711C, and U712B, produce 10 MHz, 5 MHz, and 2.5 MHz clocks.

Flip-flop U710D and exclusive-OR gate U711C generate the 2.5 MHz clock (CLK3A) that is delayed 3/8 of a cycle (150 ns) with respect to the 2.5 MHz clock at the 3Q output (CLK1A). CLK1A, CLK2A, and CLK3A are used for control-clock generation in the Waveform Processor system (diagram 2). The 10 MHz clock output at J133 is provided as a trigger signal when troubleshooting the Waveform Processor system with a logic analyzer or test oscilloscope.

The CLK1A, CLK2A, and CLK3A clocks are buffered by U712A, U712C, and U712D to the Waveform μP. Buffering these clocks ensures that a fault on the buffered side will not halt operation of the Secondary Clock Generator circuit. Series-damping resistors R713, R715, and R716 reduce ringing in the interconnection cable. The 5 MHz clock is applied to multiplexer U722A, where it is available for selection (along with the $\overline{\text{4MHz}}$ clock) as the reference signal to Phase Clock Array phase-locked loop circuit (U381, diagram 11). The 5 MHz clock is also used in the Display Control circuitry, diagram 17.

Minimum-Delay 1 MHz Clock

The Minimum-Delay 1 MHz Clock circuit produces a 1 MHz clock (2XPC) whose transitions very nearly coincide with those of the 20 MHz clock. The requirements of the clock timing dictate that the delay between a rising edge of the 20 MHz clock (C20M2 on U720A pin 3) and the 2 MHz $\overline{\text{TTL4C}}$ (TTL-compatible phase 4 clock, originating from Phase Clock Array U470—diagram 11) transitions be less than 50 ns. Since the propagation delay (2XPC-to-$\overline{\text{TTL4C}}$ delay) through the Phase-Clock Array is a significant portion of the 50 ns allowed, the phase of the 2XPC (two-times CCD "C" register clock rate) clock relative to the 20 MHz clock must be optimized for minimum delay.

To obtain minimum delay, U622, U523B, and their associated logic gating are configured as a divide-by-20 counter whose output is synchronized to the 20 MHz clock (plus propagation delay through U523B). Counter U622 and NAND-gate U620C provide division by ten, producing a 2 MHz clock (4XPC) at pin 11 of U622. This clock is inverted by U513F and is used in the A/D Converter and Acquisition Latches circuit (diagram 15). The uninverted 4XPC clock is used as the SR (shift right) data input for shift register U642 to produce two delayed 4XPC clocks ($D_1$4XPC and $D_2$4XPC).

After one run through the counting cycle at power-on, any unknown counter states in divide-by-ten counter U622 are resolved, and the circuit counts in the following manner: If the circuit does not start in the Load condition, it will be in the Count mode (a HI on pin 9 from the output of NAND-gate U620C) and the 20 MHz clocks cause the counter output to increment until it reaches 1100 (binary). At this point the output of U620C will go LO, causing the counter to load the count 0011 (binary) from its inputs with the next clock. Once the counter is loaded, the output of U620C will return HI, and normal counting from a known state commences. When the counter reaches 1100 again, the load-count sequence will be repeated, requiring ten 20 MHz clocks to complete the cycle.

AND-gate U623C watches the three lowest bits of the counter outputs (Q_A, Q_B, and Q_C). The output of U623C (pin 8) will be HI during the "7" state (0111 binary) of each 10-count cycle and will stay HI for one 20 MHz clock cycle (50 ns). This HI is applied to the K input and the J input (via OR-gate U522B) of flip-flop U523B. With the K and J inputs both HI, the flip-flop toggles when the next 20 MHz clock arrives. Assuming the Q output of the flip-flop was LO, toggling to a HI applies a HI to the J input via OR-gate U522B. When the output of U623C returns LO (next 20 MHz clock), the J and K input states of the flip-flop will keep the Q output HI with subsequent 20 MHz clocks.

The Q output of U523B will stay HI until the next seven (0111) state from AND-gate U623C arrives, at which time the J and K inputs are again set HI. On the rising edge of the next 20 MHz clock the Q output of flip-flop U523B toggles LO. When the 50 ns pulse from U623C returns LO, the J and K input states will both be LO, and further 20 MHz clocks are prevented from changing the Q output state of the flip-flop. The output remains LO until the next HI state from U623C starts the divide sequence over again. Note that transitions of the 1 MHz signal (2XPC) at pin 9 of U523B are delayed from the $\overline{\text{C20M}}$ (20 MHz clock) clock rising-edge transitions by only the propagation delay through the flip-flop (about 7 ns).

CCD Output-Sample Clocks

The CCD (charge-couple devices) Output-Sample Clocks stage controls signal transfers from the Acquisition CCD-Clock Drivers (diagram 10) to the external CCD Output circuitry (diagram 14). It consists of a state machine synchronized to the 20 MHz clock (and thus the CCD events) and produces clocks to: (1) move sampled data out of the CH1 CCD array, (2) move sampled data out of the CH2 CCD array, (3) reset both the CH1 and CH2 CCD array output-charge wells in preparation for the next transfer, and (4) phase-lock the CCD-Data Clock stage. Figure 3-3 illustrates the timing of these clocks and other clocks in the System Clock Generator; it may be of use in following the discussion of circuit operation.

When acquired samples are to be shifted out of the CH1 and CH2 CCD array, the TTL version of the Phase-Clock 04 output ($\overline{\text{TTL4C}}$ from Phase Clock Array U470) will be toggling at 500 kHz. Transitions of the $\overline{\text{TTL4C}}$ clock are resynchronized to the 20 MHz clock (C20M2) by flip-flop U720A to correct the phase between the $\overline{\text{TTL4C}}$ clock and the state machine outputs. This correction closely synchronizes charge transfers within the CCD (relative to the 2XPC clock) with the signal transfers out of the CCD.

When the $\overline{\text{SYNC4C}}$ (synchronized phase-4 clock) is LO (pin 5 of flip-flop U720A), the LOAD signal applied to shift registers U730 and U830 (via AND-gate U623B and inverter U513E) will be HI. This HI, along with the HI SYNC4C signal from pin 6 of flip-flop U720A, causes both shift registers to do a parallel load of the fixed logic levels applied to their D input pins. The levels loaded set the $\overline{\text{OS1}}$ (sample CH1-CCD outputs), $\overline{\text{OS2}}$ (sample CH2-CCD outputs), and the $\overline{\text{RST}}$ (reset CCD output wells) outputs from U730, and the $\overline{\text{SYNC}}$ (sync data clocks) output from U830 all HI. The HI $\overline{\text{RST}}$ level applied back to U621 and the HI output from NAND-gate U620B will be loaded into counter U621 as 0101 binary because of the LO $\overline{\text{LOAD}}$ output of U623B applied to the CT/$\overline{\text{LD}}$ input pin. This state then stays as is for the remainder of the LO state of the $\overline{\text{SYNC4C}}$ signal.

When the $\overline{\text{SYNC4C}}$ output of flip-flop U720A returns HI, counter U621 is enabled by the HI from AND-gate U623B to count for three, 20 MHz clock cycles (150 ns), reaching the count of 0111 binary. The next clock toggles the Q_C output of U621 LO (count goes to 1000 binary), and the $\overline{\text{LOAD}}$ output from AND-gate U623B is forced LO. The HI LOAD signal output obtained from inverter U513E, along with the LO SYNC4C from flip-flop U720A pin 6, sets up shift registers U730 and U830 to shift right. The next 20 MHz clock (250 ns after the 2XPC clock toggled) shifts a LO to the $\overline{\text{OS1}}$ output of U730 (pin 14) and loads a binary 0100 into counter U621 (since the output of NAND-gate U620B is now LO). The fixed HI applied to the SR data input of U730 is shifted to the Q_A output.

After 0100 is loaded into counter U621, the $\overline{\text{LOAD}}$ output of U623B returns HI (since pin 12 of U621 has been set HI by the inputs loaded into the counter). This once again produces a LO LOAD output from inverter U513E and prevents U730 and U830 from shifting. Counter U621 counts four cycles of the 20 MHz clock (200 ns), reaching count 0111. The next 20 MHz clock toggles the Q_C output of U621 LO and sets the $\overline{\text{LOAD}}$ line LO once again, enabling shift registers U730 and U830. The next clock (250 ns) shifts the previously loaded LO from the $\overline{\text{OS1}}$ output right to the $\overline{\text{OS2}}$ output of U730 and moves a HI from the SR data input into the $\overline{\text{OS1}}$ output. At the same time, counter U621 is reloaded to 0100 binary to again restart its count.

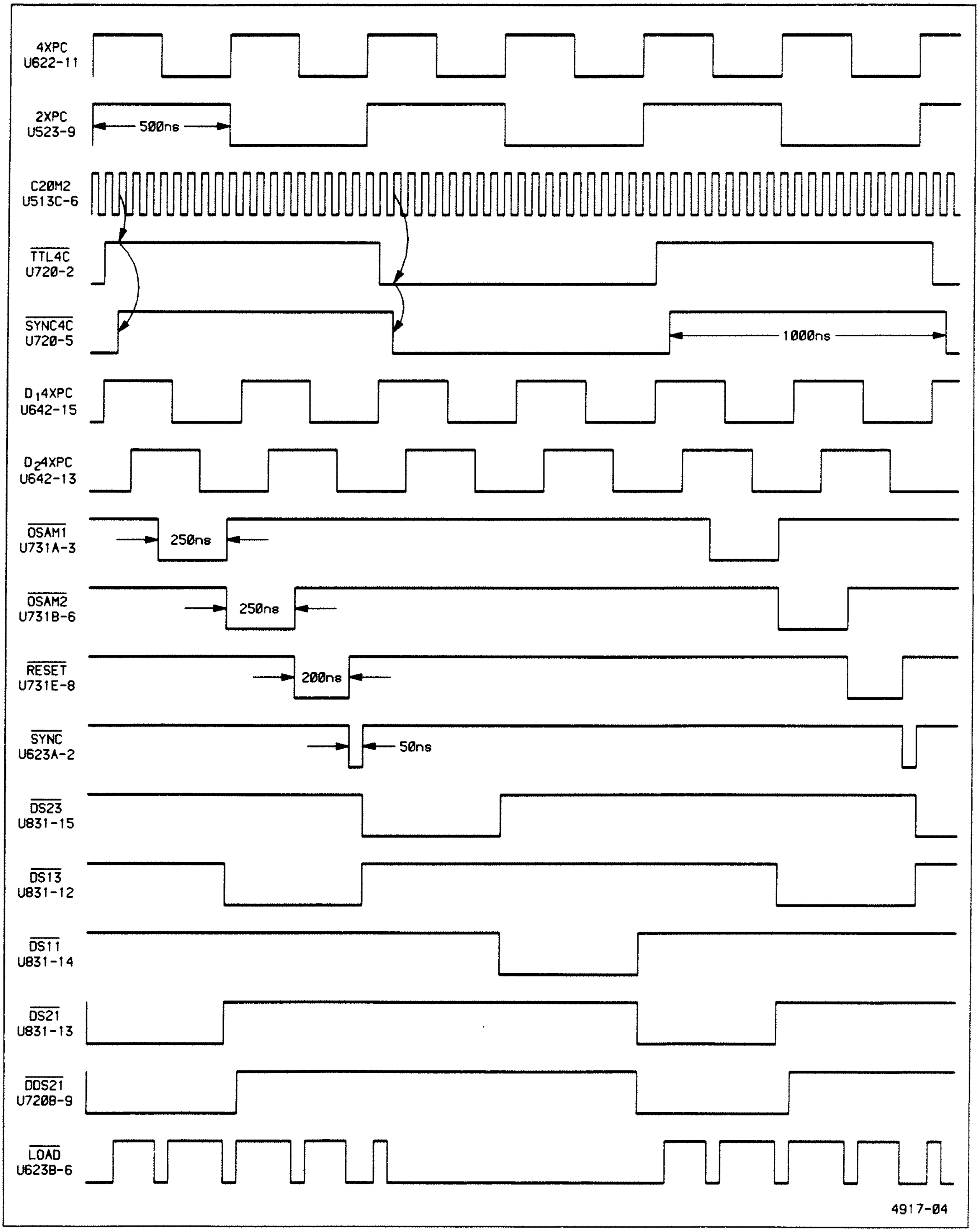


Figure 3-3. System Clock waveforms.

A similar 250 ns cycle occurs for the $\overline{\text{OS2}}$ LO state, ending with the LO being shifted to the Q_D output of U730. However, when the load is done to U621 this time, the $\overline{\text{OS2}}$ output to NAND-gate U620B is LO, and counter U621 is loaded with 0101 binary (the D_A) input from U620B is HI).

Since U621 now needs one less clock to count to 0111, $\overline{\text{RST}}$ (and thus $\overline{\text{RESET}}$ remains LO for 200 ns (rather than 250 ns as for $\overline{\text{OS1}}$ and $\overline{\text{OS2}}$), after which time the next load of U621 will occur. At the end of the reset time, both $\overline{\text{RST}}$ and the DA output of U620B are both LO, so counter U621 loads to 0000 binary. On the same 20 MHz clock, the LO $\overline{\text{RST}}$ level present on the SR data input of U830 is shifted right to the Q_A ($\overline{\text{SYNC}}$) output. This state (with $\overline{\text{SYNC}}$ LO) lasts one clock cycle (50 ns) only, because Q_C is still LO, causing LOAD to go HI and, therefore, causing the shift register to again shift right, resulting in SYNC going HI. On the next 20 MHz clock pulse, the $\overline{\text{TTL4C}}$ input is LO, causing $\overline{\text{SYNC4C}}$ to go LO on the clock edge. This starts the whole process over, and it is repeated until all samples have been moved out of the CCD arrays.

AND-gates U731A, U731B, and U731C buffer the outputs of counter U730 and ensure that the counter and the clock circuit will keep running even if a short occurs on the buffered $\overline{\text{OSAM1}}$, $\overline{\text{OSAM2}}$, or $\overline{\text{RESET}}$ lines.

CCD Data Clocks

The CCD Data Clocks ($\overline{\text{DS11}}$, $\overline{\text{DS13}}$, $\overline{\text{DS21}}$, and $\overline{\text{DS23}}$), generated by counter U721, shift register U831, and the associated logic gating, are responsible for multiplexing the four CCD array output levels (CH 1-1, CH 1-3, CH 2-1, and CH 2-3) onto the CCD DATA line for digitization by the A/D Converter. Figure 3-3 (shown previously) illustrates timing of the stage.

When the $\overline{\text{SYNC}}$ output from U830 pin 15 goes LO (for 50 ns at the end of the $\overline{\text{TTL4C}}$ cycle), the outputs of NAND-gate U620A and inverter U513D go HI, and the output of AND-gate U623A goes LO. This places counter U721 and shift register U831 in their parallel load mode, and the next 20 MHz clock rising edge (start of next $\overline{\text{TTL4C}}$) loads in the fixed logic levels at their D inputs. The data bits (1000 binary) loaded into shift register U831 set the DS23 (data select CH2 phase-3) output bit (pin 15) HI, with all other output bits LO. The LO $\overline{\text{DS23}}$ output from inverter U832D is applied to Q880 (diagram 14) to switch the CCD output data from the CH2 CCD array phase-3 output onto the CCD DATA line, where it is applied to A/D Converter U560 (diagram 15).

That same 20 MHz clock loads counter U721 with 0111 binary and clocks $\overline{\text{SYNC}}$ from pin 15 of U830 HI. With $\overline{\text{SYNC}}$ HI, shift register U831 is in hold mode, and counter U721 is enabled to count via AND-gate U623A. Counter U721 increments from the beginning count of 0111 to 0000 (nine, 20 MHz clocks—450 ns), at which time the $\overline{\text{SHIFT}}$ output from OR-gate U522A goes LO. This sets up shift register U831 (via U620A) to shift and via U623A places U721 in load mode. The next 20 MHz clock (at 500 ns) shifts a new LO from the SR data input of U831 into the Q_A output and shifts the HI from the Q_A output to the Q_B output (DS11). Counter U721 is also reloaded with 0111 binary for the next count cycle.

Similar 500 ns count cycles shift the HI bit to each output of shift register U831 in succession until, during the last 50 ns of the HI state of the DS13 signal (U831 pin 15), $\overline{\text{SYNC}}$ goes LO again. The LO sets up U721 and U831 to load on the next 20 MHz clock. The next clock (concurrent with $\overline{\text{TTL4C}}$ going LO) loads both U721 and U831 and starts the cycle over again. The arrival of the $\overline{\text{SYNC}}$ signal ensures that the presetting load of U721 and U831 always occurs concurrently with $\overline{\text{TTL4C}}$ going LO. The four data-select clocks (and their inverted outputs) are thereby synchronized to CCD array output cycles.

The DS21 signal is also applied to a circuit formed by flip-flop U720B and exclusive-OR gate U711D. One input of U711D is held permanently HI so the gate acts as an inverter for the DS21 signal on the other input. When the DS21 logic level goes HI, the output of U711D goes LO and flip-flop U720B become set with the Q output (pin 9) HI. At the end of the HI logic level, the DS21 signal goes LO, but the Q output remains HI until the next rising edge of the $D_1$4XPC clock (4XPC delayed by one 20 MHz clock cycle) clocks the LO on the D input through the flip-flop. This circuit action has the effect of stretching the DS21 signal by 50 ns. The resulting DDS21 signal is applied to Time Base Controller U670 (diagram 8).

The delayed $D_1$4XPC and $D_2$4XPC clocks are produced by using the 4XPC clock as the data source for the shift-right input to register U162 and clocking that data right to the shift register outputs with the 20 MHz clock (C20M1). The first output signal (Q_A) is delayed from the input clock by 50 ns and the second (Q_C) by 150 ns. $D_2$4XPC is applied to NAND-gate U650B (diagram 8) for use is controlling the timing of the $\overline{\text{SAVEACQ}}$ signal to the Acquisition Memory. The time delay ensures that the data written to Memory has stabilized at the output of the A/D Converter.

Reference Frequency Selector

The PLL (phase-locked loop) Reference Frequency Selector, U722A, selects either a 4 MHz or a 5 MHz clock signal as the reference frequency to the Phase-Locked Loop (PLL) circuit (U381, diagram 11). The Phase-Clock Oscillator in the PLL circuit runs at 50 times the selected reference frequency, so sampling clocks to Phase Clock Array U470 are generated at a rate of either 200 MHz or 250 MHz. The two choices of signal frequencies provide the correct input frequency to the internal dividers of the Phase Clock Array needed to generate the clocks for each SEC/DIV setting sample rate.

Flip-flop U523A is configured as a divide-by-two circuit that divides the 8 MHz (C8M) clock to produce a $\overline{\text{4MHz}}$ clock at its $\overline{Q}$ output (pin 6). The SEL4/5 (select 4 MHz/5 MHz) signal on pin 14 of U722A selects whether this 4 MHz clock or the 5 MHz clock from U710 will appear at the REF4/5 output pin. The signal inputs to the multiplexer are connected so that when SEL4/5 is HI, the 5 MHz clock is selected (no matter what state the other select input, shown with U722B, is in); when it is LO, the 4 MHz clock is selected. The $\overline{\text{4MHz}}$ signal is inverted by U832F and applied to the Front-Panel μP (U700, diagram 3) as the clocking frequency.

TIME BASE CONTROLLER AND ACQUISITION MEMORY

Time Base Controller (U670, diagram 8) and its associated gating circuitry generates the control signals and clocks to cause acquisitions in the various modes to occur. It keeps track of how the acquisition is progressing, starts the digitization of the samples by the A/D Converter when the correct number of data points have been acquired, and moves the digitized samples to Acquisition Memory (U600). The Acquisition Memory provides temporary storage of the converted data to permit the Waveform μP to access the data as it is needed to update the display.

Time Base Controller

Time Base Controller U670 monitors and controls the various acquisition functions. Two different operating modes of the CCD (charge-coupled devices) arrays must be controlled by U670; these are the FISO mode (fast-in, slow-out) and the Short-Pipe mode (slow-in, slow-out). FISO mode is used at sweep speeds faster than 100 μs/div when the analog sampling must occur at the fastest possible rate. The Short-Pipe mode is used for lower frequency signals when the A/D conversion rate is much faster than the signals being sampled.

The major Time Base Controller functions in FISO (fast-in, slow-out) mode are:

- Ensure that enough samples are in the CCD array "B" register to fill the "pretrigger" requirements.
- Ensure that the proper number of "post-trigger" samples are moved into the "B" register after triggering occurs.
- Discard the proper number of unneeded samples at the start of "slow-out" conversion.
- Ensure that exactly 1024 samples are moved to the Acquisition Memory during the "slow-out" conversion process.

Major functions in Short-Pipe mode are:

- Ensure that valid data has made it through the "short-pipe" path of the CCD arrays.
- Synthesize the proper sample rate called for by the SEC/DIV setting.
- Ensure that enough samples have been saved in the Acquisition Memory to fill pretrigger requirements before enabling the Triggers.
- Ensure that the proper number of post-trigger samples are stored into the Acquisition Memory after the trigger event.

The instruction registers within Time Base Controller U670 are enabled when $\overline{\text{TBSEL}}$ from the System μP is LO. A register is selected for writing to or reading from by address lines A0, A1, and A2. Setup data from the System μP data bus is buffered to the selected register via bidirectional buffer U641 and written into the selected internal register by the $\overline{\text{WR}}$ (write) signal applied to pin 14. Acquisition mode, SEC/DIV setting, trigger position, and several other functions are controlled by the System μP via the commands written to the instruction registers within U670. Status data and register contents may be read out of the Time Base Controller registers by the System μP in a similar manner using the $\overline{\text{RD}}$ (read) signal to reverse the data paths in buffer U641 and the internal circuitry of U670.

The FISO (fast-in, slow-out, pin 36), ROLL (pin 2), SEL4/5 (select reference—4 MHz/5 MHz, pin 28), and ENVL (envelope, pin 39) outputs are set indirectly by System μP writes to the internal control registers at the start of each acquisition cycle. Control signals are then output by an internal state machine of the Time Base Controller to dynamically control the acquisition circuitry in the required mode and signal acquisition rate (set by a combination of FISO and SEL4/5). Writing to these "register" locations also allows the System μP to generate several strobes for internal latching and control functions.

A state machine internal to Time Base Controller U670 runs the acquisition process from start to finish. When all internal registers are properly loaded, the System μP writes to location 6022(h), generating a strobe that switches acquisition control to the Time Base Controller. This starts the acquisition system, and samples are taken in the defined mode. For FISO operations, the following occurs.

A counter internal to U670 begins counting $\overline{\text{TTL1B}}$ (TTL version—Phase 1B) clocks to determine when at least enough samples have been transferred into the "B" register of the CCD arrays to fill "pretrigger" requirements. Samples will then continue to be placed in the B register, but no output samples will be saved until the record trigger occurs. (All 1054 locations in the two sides of 16 $\times$ 33 B register will fill if a record trigger does not occur before that many samples have been taken.) Each $\overline{\text{TTL1B}}$ clock represents 32 analog samples (two, 16-sample sides) transferred into the CCD array B register. When the proper number of pretrigger samples have been loaded, U670 will set its EPTHO (end of pretrigger holdoff) line HI. This signal enables Trigger Logic Array U370 (diagram 11), and the state machine in Time Base Controller U670 starts watching the SYNTRIG (synchronized trigger) input (pin 30) from the Phase Clock Array (U470, diagram 11) for the "record" trigger. In the meantime, the Trigger Logic Array will be counting delay clocks (DELCLK) to fulfill any specified delay requirements before a record trigger is permitted to be generated.

When the delay requirements are met, the SYNTRIG is allowed to occur when a trigger event occurs. The counter then watches $\overline{\text{TTL1B}}$ to determine when the proper number of post-trigger samples have been moved to the B register to fill the post-trigger requirements, then it sets SO (slow-out, pin 38) HI. This stops the sampling process and starts A/D conversion of the analog samples stored in the CCD array B register.

Since the trigger event can occur at any one of the 32 analog samples that are taken between each TTL1B clock, and since the Time Base Controller only keeps track of the number of pretrigger and post-trigger samples in terms of these 32-sample records, there are usually some samples at the beginning of those in the CCD array B register that are extra. When the analog samples are serially moved out of the CCD array for digitization, these extra samples must be ignored in order to maintain proper trigger location within the complete record. The CCD Phase Clock Array (U470) knows where the record trigger occurred relative to the $\overline{\text{TTL1B}}$ pulse (1-of-32 position) and sends this information to U670 on the TL0-TL4 (trigger location bits 0 through 4) lines. This trigger-location number is loaded into the counter and, as the samples are moved out of the CCD array, that number of samples is essentially discarded. Those samples are A/D converted but will not be stored because U650B is not yet enabled to gate the $\overline{\text{SAVEACQ}}$ signal used to write the data into the Acquisition Memory.

Once the extra samples have been counted, the ACQUIRE output is set HI, enabling U650B. Since the instrument is in FISO mode, the output of U512C will be HI and the $\overline{\text{SAVEACQ}}$ signal used to save waveform data into the Acquisition Memory (via U501) is controlled by the output of U642 (diagram 7). This input to NAND-gate U650B is a delayed version of the 4XPC (2 MHz) clock ($D_2$4XPC). The 150 ns delay provided ensures that the A/D Converter output byte has settled before being written to the Acquisition Memory.

When the Time Base Controller is in control of writing data to the Acquisition Memory, the $\overline{\text{SAVEACQ}}$ clock is routed through U501 of the Mode Control Logic and becomes the $\overline{\text{WE}}$ (write enable) clock used to write waveform data into Acquisition Memory U600. That data is obtained from the Acquisition Latches (diagram 15) via buffer U613. The $\overline{\text{WE}}$ signal is also used to increment the Memory Address Counter (U300, U400, and U401) the result being that digitized samples from the Acquisition Latches are saved interleaved in consecutive memory locations. Each address is latched into the Record-Start Address Latches (U502 and U601) as the data-write ends, so that the address of the last-stored sample is always available. This information is used as a pointer when generating waveform displays.

As the digitized samples are moved to Acquisition Memory, an internal counter in Time Base Controller U670 watches the DS21 and DS23 clocks (pins 6 and 17) to determine when 1024 points (or 512 max/min pairs in Envelope mode) from each CCD array (CH 1 and CH 2) have been stored. When 2048 samples have been saved, the Time Base Controller will set ACQUIRE (pin 24) LO, disabling memory saves, and it will set its ACQDN (acquisition done) status line (pin 25) HI. The Waveform μP (U470, diagram 2) then takes over for transfer of the acquired waveforms to the Waveform μP Save Memory.

When the Waveform μP (U470, diagram 2) reads the HI ACQDN status via U542 (diagram 2), it reads the address of the last-saved point from the Record-End Latch (U502 and U601). Since the Acquisition Memory addresses are circular (incrementing the Address Counter from its last address goes back to the first address), it knows the record begins at the next address. With TB2MEM LO, the $\overline{\text{ACQ}}$ signal is routed through Mode Logic Switch U501 to become the $\overline{\text{WP2MEM}}$ signal. The $\overline{\text{ACQ}}$ signal going LO from the Waveform μP via address decoder U570 enables data buffer U610 to permit the Waveform μP to access the waveform data stored in the Acquisition Memory (see "Waveform Processor System" description).

SHORT-PIPE OPERATION. Short-Pipe operation is similar to FISO in the way mode and setup data is loaded and the way the internal counter is used to keep track of various events. The major differences are: Short-Pipe mode moves input samples directly from the CCD array "A" register input, down the first "B" register channel and out of the CCD array through the "C" register. Short-Pipe mode must also synthesize the sample clock rate.

To synthesize the sample rate for the Short-Pipe mode, FISO (from U670 pin 36) is set LO by the System μP, thereby enabling the CE2B/N (clock enable 2B divided by N) input to U512C. The CE2B/N clock (along with the $D_2$4XPC clock) then controls saving the waveform data into the Acquisition Memory. In Short-Pipe mode, CCD sampling occurs at a continuous 1 MHz rate, but due to SEC/DIV setting data written to an internal counter in U670, the synthesized $\overline{\text{CE2B/N}}$ clock will only allow every "Nth" point to be saved in Acquisition memory to produce only 50 data points per division in the display. Samples between the saved Nth points are ignored. The synthesized $\overline{\text{CE2B/N}}$ clock will only enable U650B long enough to save either two or four points and is dependent on the sweep-rate division factor written to the internal counter. This allows effective sample rates down to 1 sample every 2 μs (100 μs/div) to be achieved. The SDC (slow-delay clock, U670—pin 29) runs at this effective sample rate and allows the Trigger circuits to count delay periods in terms of sample intervals.

Since CCD array samples are moved directly from the input to the output via the first B register and since stored samples may occur at a rate different than the sample rate, pretrigger and post-trigger counting is done relative to samples actually stored into the Acquisition Memory. When enough valid pretrigger points have been saved, EPTHO enables the Triggers. Data is saved in bursts of two points (four points in ENVELOPE acquisition mode), one for CH 1 and one for CH 2, at the synthesized rate. When the trigger event occurs, the Trigger location bits are set relative to the synthesized clock and allow a data correction algorithm to correct already-acquired data points relative to the trigger event. Post-trigger sampling occurs at the defined rate, and since A/D converted data already is stored in Acquisition Memory, ACQDN is set. Waveform data bytes are moved to the Save Memory by the Waveform μP and control is given back to the System μP.

LOAD LATCHES FLIP-FLOP. In Envelope Mode, Load Latches flip-flop U651A puts out a signal at the beginning of each envelope sampling interval that is HI for four acquisition cycles. That HI LOAD LATCHES signal loads the first four acquired data points (two min-max pairs) into the Acquisition Latches to be used for min-max comparison to the following waveform samples in that Envelope sampling interval.

The Set input of U651A is HI during Envelope, the output of the flip-flop is controlled by the DS23 clock and the CE2B/N clock (on the D input). The CE2B/N clock is a divided down DS23 clock, with the division factor depending on the SEC/DIV setting. The division factor determines how many waveform samples will be compared for new max and new min during each envelope sampling interval. Only the maximum and minimum waveform data point values that occur during the envelope sampling interval are transferred to the Acquisition Memory.

For non-envelope acquisitions, ENVL is LO. The Set input of flip-flop U651A is therefore asserted, and U651A will be held in the Set state with the Q output (LOAD LATCHES) held HI. That constant HI signal applied to the Acquisition Latch Switching circuitry causes each data point acquired to be loaded into the Acquisition Latches and transferred into Acquisition Memory.

ROLL LOGIC. In ROLL mode the display is constantly being updated as new data points are available. A means is provided to tell the Waveform μP when new data points are available. An interrupt to the Waveform μP is generated by the Roll Logic flip-flop, U651B. When the ACQUIRE signal from Time Base Controller U670 goes HI, new waveform data points are acquired. The HI state of that signal is clocked to the Q output of flip-flop U651B on the rising edge of the $\overline{\text{CE2B/N}}$ signal; the same signal that causes the sample data to be saved into the Acquisition Memory in Short-Pipe mode. The PTAVAIL signal at the Q output is an interrupt to the Waveform μP. When the Waveform μP services the interrupt request, it sets $\overline{\text{PTACK}}$ (point acknowledge) LO via U500B and U500C to reset the flip-flop in preparation for the next new data points. The saved points are also moved to the Save Memory and then to the Display Memory for a display update.

In NORMAL mode, the ROLL signal is LO, and NAND-gate U500B outputs a continuous logic HI that holds the Roll Logic flip-flop in the Reset state (with the Q output LO).

Memory Mode Control

The Memory Mode Control circuit is made up primarily of Mode Selector Switch U501, a quad 2-to-1 multiplexer that switches control signals between those of Time Base Controller U670 and those of the Waveform μP. Selection is done by the TB2MEM signal from AND-gate U731D pin 11.

The $\overline{\text{WE}}$ (write enable) output from Mode Selector Switch U501, pin 12, controls both writing into the Acquisition Memory and incrementing of the Address Counter. With TB2MEM set LO, the $\overline{\text{WWR}}$ (Waveform μP write) signal gated through OR-gate U512D to the 4A input (pin 13) of U501 controls writing to the Acquisition Memory. The $\overline{\text{OE}}$ (output enable) derived from the Waveform μP $\overline{\text{WRD}}$ (Waveform μP read signal), controls the output of Acquisition Memory data. It is asserted LO only when the Waveform μP is trying to read Acquisition Memory locations.

With TB2MEM HI, the $\overline{\text{SAVEACQ}}$ signal from NAND-gate U650B, is selected as the $\overline{\text{WE}}$ signal, and the $\overline{\text{OE}}$ is set HI to disable the Acquisition Memory from outputting data. Data buffer U613 is enabled by the LO level of the $\overline{\text{EOE}}$ signal from pin 7 of the Mode Select Switch to connect the the Envelope Logic Latch bus to the input bus of the Acquisition Memory.

When the Waveform μP wants to access the Acquisition Memory, it will set the $\overline{\text{ACQ}}$ line LO to enable its control signals to the inputs of Mode Logic Switch U501 and wait for the ACQUIRE signal from Time Base Controller U670 (diagram 8) to go LO (indicating that the Time Base Controller is finished acquiring). When ACQUIRE goes LO, the output of AND-gate U731D (TB2MEM) goes LO and the Mode Logic Switch select the Waveform μP signals to control the Acquisition Memory. The LO TB2MEM signal also sets the Address Counters to their Load state, and the counter outputs then follow the WA0-WAA (Waveform μP address bits 0-A) lines, giving direct access to Acquisition Memory data locations by the Waveform μP.

Address Counter

The Address Counter increments the Acquisition Memory address as each point is saved. Each write into Acquisition Memory ends with the $\overline{\text{WE}}$ (write enable) signal going HI, clocking the counter to address the next sequential Acquisition Memory location.

The TB2MEM signal from AND-gate U731D controls the mode of the Acquisition Memory Address Counter (composed of binary counters U300, U400, and U401). When the the TB2MEM signal goes LO, the counters become "transparent." This connects the Waveform μP address bus to the address inputs of the Acquisition Memory so that the Address Counter output follows the WA0-WAA (Waveform μP address bits 0-A) lines. When the TB2MEM signal is HI, the Time Base Controller is in control of the Acquisition Memory, and counter will be in its count mode as the acquired signals are being stored into the Acquisition Memory.

Acquisition Memory

Acquisition Memory U600 is a random-access memory device (RAM) that provides temporary storage of acquired data points before they are moved into Save Memory. Analog waveform samples from the CH 1 and CH 2 CCD arrays are digitized and moved into Acquisition Memory under control of the Time Base Controller (diagram 8), alternating CH 1 data with CH 2 data. The Waveform μP reads the data out of Acquisition Memory via buffer U610, unscrambles it, and moves it to proper Save Memory locations.

MEMORY INPUT BUFFER. Memory Input Buffer U613 applies the time-multiplexed waveform data bytes from the Acquisition Latches (diagram 15) to the data inputs of the Acquisition Memory inputs at all times except when the Waveform μP is accessing the Memory. Inverter U620D inverts the most-significant bit of the sample data so that range center of the A/D Converter output corresponds to 00 hex (center screen value), thereby creating bipolar data referenced to center screen.

Record-End Latch

The Record End Latch composed of U502 and U601 continually latches the address of the last Acquisition memory location that was written. The latch is clocked on the rising edge of the $\overline{\text{WE}}$ clock (from the $\overline{\text{SAVEACQ}}$ signal or the Waveform μP $\overline{\text{WWR}}$ signal via Mode Logic Switch U501) and provides the Waveform μP with the last address written (the end of the record for a full acquisition) by the Time Base Controller or read by the Waveform μP. Since the Acquisition Memory addresses are circular, the start of a FISO record will always be the Record End address plus one. In Short-Pipe mode, the Waveform μP will read those (two for normal, four for envelope) points immediately preceding (and including) the Record End address. The latched address (plus the trigger location data) is placed on the Waveform μP data bus by asserting $\overline{\text{RDMAR0}}$ and $\overline{\text{RDMAR1}}$ (read memory address) lines.

Two-to-one multiplexer U722B applies either trigger-location bit 4 (TL4) or the Time Base Controller TBTRIG (time base triggered) status bit to latch U502, depending on whether FISO or Short-Pipe mode is called for. The TBTRIG bit used in Short-Pipe mode tells the Waveform μP when the Time Base Controller detected Record Triggering.

ATTENUATORS AND PREAMPLIFIERS

The Attenuator and Preamplifier circuitry (diagram 9) allows the operator to select the vertical deflection factors. The Front Panel μP monitors the Channel VOLTS/DIV switches and VOLTS/DIV VAR controls and passes changes to the settings to the System μP which then digitally switches the attenuators and sets the Preamplifier gains accordingly. Vertical Couplings are similarly controlled.

Channel 1 and Channel 2 Attenuators

The Channel 1 and Channel 2 Attenuators are identical in operation, with corresponding circuitry in each channel performing the same function. Therefore, only the Channel 1 circuitry is described.

An input signal from the Channel 1 input connector is routed through an attenuator network by four pairs of magnetic-latch relay contacts. The position of the relays is set by data placed into Attenuator Control Register U511 by the System μP. Relay buffers U510 and U520A and ATTEN CLK circuitry, U520D, Q620, and Q621 provide the necessary drive current to the relay coils.

Four input coupling modes (1 MΩ AC, GND, 1 MΩ DC, and 50 Ω DC) and three attenuation factors (1X, 10X, and 100X) may be selected by closing different combinations of relay contacts. The relay contacts are magnetically latched and, once set, remain in position until new attenuator settings are loaded into the Attenuator Control Register and clocked by the ATTEN CLK circuitry. (See the "Attenuator Control Register" description for a discussion of the relay-latching procedure.) The three attenuation factors, along with the programmable and variable gain factors of the Vertical Preamplifier, are used to the obtain complete range of vertical deflection factors.

The 50 Ω termination resistor has a thermal sensor associated with it that produces a dc voltage (CH 1 OVL) proportional to the input power. Should the input power exceed the normal safe operating level for the 50 Ω DC input, the output voltage from the thermal sensor will exceed the normal operating limit. The amplitude of this dc level is periodically checked by the Front Panel μP to detect if an overload condition is present. If an overload occurs, the System μP switches the input coupling to the 1 MΩ position to prevent damage to the attenuator, and the error message "50 Ω OVERLOAD" is displayed on the crt. At power-off, the input coupling is automatically switched to the 1 MΩ position to prevent an unmonitored overload condition from accidently occurring.

Compensating capacitor C414 is manually adjusted at the time of calibration to normalize input capacitance of the preamplifier to the attenuator.

A probe-coding ring around the BNC input connector passes probe-coding information (a resistance value to ground) to the Front Panel μP for detection of probe attenuation factors. The readout scale factors are then set to reflect the attenuation factor of the attached probe.

Attenuator Control Register and Attenuator Clock

The Attenuator Control Register, composed of shift registers U511 and U221, allows the System μP to control the settings of the input coupling and attenuation factors. To set the input coupling mode and attenuation factors for Channel 1 and Channel 2, a series of eight 16-bit control words are serially clocked into U221 and U511 (eight bits in each register). Each control word is used to set the position of one of the eight attenuator and coupling relays (four relays are in each attenuator assembly). Each control word will have only the bit corresponding to the specific relay contact to be closed set HI. Relay buffers U510 and U520A (for Channel 1) and U220 and U520B (for Channel 2) are open-collector drivers that invert the polarities of all bits. This results in a LO being applied to only the coil lead associated with the contact to be closed; all other coil leads are held HI.

ATTENUATOR CLK CIRCUIT. To set a relay once the control word is loaded, the System μP generates an ATTN CLK (attenuator clock) to U520D pin 4 via R530 and C530. The strobe pulses the output of U520D LO for a short time. This output pulse attempts to turn on both Q620 and Q621 (relay drivers) via their identical base-bias networks. Due to the lower level from the turned on Darlington relay buffer (coupled through the associated coil diode and either CR610 or CR622 to one of the bias networks), one transistor will turn on harder as the ATTN CLK pulse begins to forward bias the transistors. The more positive collector voltage of the transistor turning on harder is fed through the bias diode (again either CR610 or CR622) to further turn off the opposite transistor. This action results in one transistor being fully on and the other one being fully off. The saturated transistor supplies a current path through the two stacked relay coils to the LO output of either U221 or U511 to close the selected contacts. Once set, the magnetic-latch feature will hold the relay set to this position until opposing data is clocked into the Attenuator Control Register and strobed into the relay. All coil leads for the remaining relays are set HI, and only the selected relay will be set.

To set the seven remaining Attenuator and coupling relays, the sequence just described is repeated seven more times. Whenever the System μP is informed by the Front Panel μP that the attenuation factor or input coupling has changed, the entire relay-setting procedure is repeated for all eight relays.

The MSB (most-significant bit) of the Attenuator Control Register, ATD15, is routed back to the System μP via CR287 and U380A (diagram 5), allowing diagnostic read-back of the register contents.

Channel 1 Preamplifier

Preamplifier U420 converts the single-ended input signal from the Channel 1 Attenuator to a differential output signal used to drive the Channel 1 Peak Detector (U440, diagram 10). The device provides amplification in predefined increments, depending on the control data written to it from the System μP. The Preamplifier also has provisions for signal inversion, variable gain, vertical positioning, trigger signal pickoff, and balance control.

The Channel 1 vertical input signal is applied to pin A of Channel 1 Preamplifier U420 via C1005, R1005, and R1015. Resistor R1015 is a damping resistor, and the two series diodes to the −8 V supply, CR410 and CR411, protect the Preamplifier input from excessive negative voltages. The differential Preamplifier signal outputs (+OUT and −OUT) sink 12 mA of common-mode current from the Channel 1 Peak Detector inputs and drive those 75 Ω inputs with a 0.25 mA per division output signal.

Control data from the System μP is clocked into the internal control register of U420 via pin 22 (CD) by the clock signal applied to pin 23 ($\overline{CC}$). This data causes the Preamplifier either to multiply the normalized gain (5 mV/div) by 2.5 or 1 or to divide the normalized gain by 2, 4, or 10. The resulting sensitivities are 2 mV/div, 5 mV/div, 10 mV/div, 20 mV/div, and 50 mV/div respectively.

Three analog control voltages set by the DAC System circuitry (diagrams 5 and 6) modify the differential output signal at pins 9 and 10 of the Preamplifier. CH1-BAL (Channel 1 Balance) is applied to U420 pin 2 from the sample-and-hold circuit formed by U641B and C648 (diagram 5). This signal is a dc-offset level determined during the auto-calibration procedure. The offset value is stored as a calibration constant in nonvolatile memory and, like the other DAC System outputs, is updated approximately every 64 ms, holding the Preamplifier in a dc-balanced condition.

The voltage level of the CH1-PA-POS (Channel 1 Preamplifier Position) signal, from the circuit which includes U630A and U630B (diagram 6), vertically positions the channel 1 trace. When the CH1 VERT POS control on the Front Panel is turned, the Front Panel μP detects the change and reports it to the System μP. The System μP incorporates the change and causes subsequent DAC System updates to reflect the new value in the analog voltage level of the CH1-PA-POS signal.

A user may change the Channel 1 variable gain by pressing the CH1 VARIABLE button and pressing the appropriate menu choice buttons. The Front Panel μP detects these switch closures and reports them to the System μP. The System μP modifies the memory value that is sent to the DAC System to reflect the user-defined variable gain factor in the CH1-GAIN-CAL signal. The memory value that is modified is the calibrated value derived at the time of instrument self-calibration and stored in nonvolatile memory. Selecting the CAL menu choice, removes the variable gain modification and returns the calibrated gain setting.

A pickoff amplifier internal to U420 conditions the trigger signal and provides the proper signal level at pin 15 to drive the A/B Trigger Generator (U150, diagram 11). The pickoff point for the trigger signal is prior to the addition of the vertical-position offset, so the position of the signal on the crt has no effect on the trigger operation. However, the pickoff point is after the Preamplifier balance and variable gain have been added to the signal, so both of these functions affect trigger operation.

Common-mode signals are rejected from the trigger signal by the circuitry composed of operational amplifier U230B and associated components. The inverting input of U230B (pin 6) is connected to the common-mode point between +PICK (pin 12) and −PICK (pin 15) of U420. Any common-mode signals present are inverted and applied to a common-mode point between R133 and R235 to cancel the signals from the differential output. A filter network composed of LR421 and a built-in circuit board capacitor reduces trigger noise susceptibility.

The drain voltage for the input FET of the Preamplifier is provided by the circuit composed of VR420, R512, R515, and R516. Resistors R516 and R515 are part of the self-calibration circuitry and are used to match the gain of the CH1-BAL signal (pin 2) with that of the output of the attenuator.

Channel 2 Preamplifier

Operation of Channel 2 Preamplifier U320 is nearly identical to that of the Channel 1 Preamplifier just described. The exceptions are that the signal obtained from the pickoff reverse-termination return (pin 11) is used to drive the rear-panel CH 2 OUT connector and that the signal from the positive trigger pickoff (pin 12) is used to drive the Video Option Back-Porch Clamp circuit (diagram 21). The output of that clamp circuit is an offset signal, applied to the Channel 2 Preamplifier at pin 3, that is used to remove ac power-supply hum from the display of a video signal applied to the Channel 2 input when the Video option is in use.

The amplified Channel 2 +PRTR signal from U320 pin 11 provides an accurate representation of the Channel 2 signal at the rear-panel CH 2 OUT connector. The +PRTR pickoff signal is applied to the emitter of Q240B via a voltage divider formed by R234, R241, and R240. Transistor Q240B, configured as a diode, provides thermal compensation for the bias voltage of Q240A and reduces dc level shifts with varying temperature. Emitter-follower Q240A provides the drive and impedance matching to the CH 2 OUT connector and removes the diode drop added by Q240B. Clamp diodes CR140 and CR141 protect Q240A should a drive signal be accidentally applied to the CH 2 OUT connector.

External Trigger Preamplifier

The functions provided by External Trigger Preamplifier U100 are similar to those provided by the Channel 1 and Channel 2 Preamplifiers. The single-ended EXT TRIG 1 and EXT TRIG 2 input signals are buffered by U100 and routed to A/B Trigger Generator U150 (diagram 11) where they are available for selection as the trigger source for either the A or B trigger signal.

External trigger signal sensitivities may be set by the user to allow triggering ranges of either ±0.9 volts (EXT ÷ 1) or ±4.5 volts (EXT ÷ 5). Larger applied voltages on the external trigger inputs will exceed the control ranges of the Trigger System. The logic levels of control bits applied to U100 pin 30 (GA3) and pin 31 (GA4) from Source Select Control Register U140 (diagram 5) set the gain of the EXT 1 and EXT 2 Preamplifiers respectively.

Dc offsets in the output signal due to any tracking differences between the +5 V and the −5 V supply to U100 are reduced by the Tracking-Regulator circuit composed of U120, Q110, and associated components. Operational amplifier U120 and Q110 is configured so that the output voltage at the emitter of Q110 follows the −5 V supply applied to R210. This tracking arrangement ensures that the supply voltages are of equal magnitude to minimize dc offsets in the output signals.

PEAK DETECTORS AND CCD/CLOCK DRIVERS

The Peak Detectors and CCD/Clock Driver arrays (diagram 10) form what is essentially a very fast analog shift register. Waveform samples from each Preamplifier (U320 and U420, diagram 9) are loaded into the shift register array at a selected sample rate up to 10 ns per division and clocked out of the array at a slower fixed rate for digitization by the A/D Converter (diagram 15).

Peak Detectors U340 and U440 are hybrid devices having two modes of operation: "track" and "peak detect." For NORMAL and AVG (average) acquisition modes, the Peak Detectors track the input signal and provide signal gain from the Preamplifiers to the CCD arrays. In the peak detect mode used for ENVELOPE acquisitions, the Peak Detectors detect and hold the most positive and the most negative amplitude value of the input signal that occurs during each sampling interval. The peak values are amplified as in the NORMAL and AVG modes and applied to the input registers of the CCD arrays in such a manner as to produce a composite waveform of the most positive and most negative waveform amplitudes.

CCD/Clock Drivers U350 and U450 are hybrid devices containing a charge-coupled device (CCD) integrated circuit and a Clock Driver integrated circuit. The charge-coupled devices are very fast analog shift registers. Differential signal level applied to the inputs of the CCD from the Peak Detectors are sequentially clocked into the CCD registers at the processor-selected sample rate as determined by the SEC/DIV switch setting. Movement of the analog samples through the CCD arrays is controlled by the Clock Driver circuitry of the devices. Shifting the sâmples out of the CCD to be digitized in done with the combined clocking action of the internal Clock Drivers and the clock signals supplied externally to the CCD via Q450, Q460, Q550, Q551, and Q560. All control logic for the CCD/Clock Drivers, with the exception of the $\overline{\text{RESET}}$ signal from the System Clock circuitry (diagram 7), is derived from Phase Clock Array U470 (diagram 11).

Signal samples from both vertical channels are continuously loaded into and shifted through the CCD arrays until a trigger event occurs. The Time Base Controller (U670, diagram 8) then allows a specific number of further analog samples to be shifted into the arrays depending on the number of post-trigger samples needed to fill the waveform record. That number is determined by the TRIG POSITION setting for the acquisition. When the necessary samples have been loaded into the arrays, sampling is halted. The differential analog samples stored in the CCD arrays are then shifted out of the CCD to the CCD Output circuitry (diagram 14) where they are conditioned and multiplexed to the A/D Converter to be digitized.

Peak Detectors

The Peak Detectors provide peak detection, gain, and buffering of the CH 1 and CH 2 signals. Peak detect is enabled for ENVELOPE mode acquisitions only, but signal buffering is provided for all modes. Operation of both Peak Detectors is the same; therefore, the description is limited to the CH 1 circuitry. A simplified block diagram of the Peak Detector is shown in Figure 3-4.

Two user-selectable bandwidth limiters provide bandwidth reductions to either 20 MHz or 50 MHz for the signal through the Peak Detectors. With the Video Option installed, one of the 20 MHz limiter coils (L531 for CH 1) is adjustable to optimize the 20 MHz response for video signal operation. Without the option, both 20 MHz bandwidth limit coils for each Peak Detector are fixed values. Fifty megahertz bandwidth is adjusted by C431 for CH 1. The input stage of the Peak Detector is where bandwidth limiting is switched. Three bandwidth-select bits (FULL, BW50, and BW20) applied from the Peak Detector Control register (U530, diagram 5) control the bandwidth. Only one control bit at a time is set HI, and that bit controls the input amplifier bandwidth accordingly.

The differential signal from the CH 1 Preamplifier is applied to the CH 1 Peak Detector (U440) on input pins 4 and 6. In ENVELOPE acquisition mode, two sets of two fast-peak detectors following the input stage are used to permit continuous peak detection of negative and positive peaks of the input signal. While the PDA fast-peak detector is peak detecting the positive peak, the PDB peak detector is holding the last peak or resetting and vice versa (see table in Figure 3-4). Each of fast-peak detectors is followed by a slow-peak detector to increase the peak-hold time to the CCD input register. The outputs of the positive peak detectors are multiplexed to the differential OUT1 pins (pins 26 and 28) while the outputs of the negative peak detectors are multiplexed to the differential OUT3 pins (pins 33 and 35).

For NORMAL and AVERAGE acquisition modes, the Peak Detector operates in the track mode. To track the input signal and supply buffering only to the input signal, pin 21 ($\overline{\text{PD}}$) is set HI and pin 22 (SLOW/$\overline{\text{FAST}}$ is set LO, and the differential peak-detector clock signals (PD1 and PD2) are held at fixed levels (PD1 LO and PD2 HI). These control state levels set up one of the fast-peak detectors in the positive- and negative-peak detectors to follow the input signal in the track mode. The differential outputs at OUT1 and OUT3 follow the input signal at a signal level of 400 mV/division with a dc common-mode voltage of about 9 V. The CCD/Clock Driver SIG1 and SIG3 inputs are high impedance, so output loading of the Peak Detectors is provided by the Common-Mode Adjust circuits (discussed later).

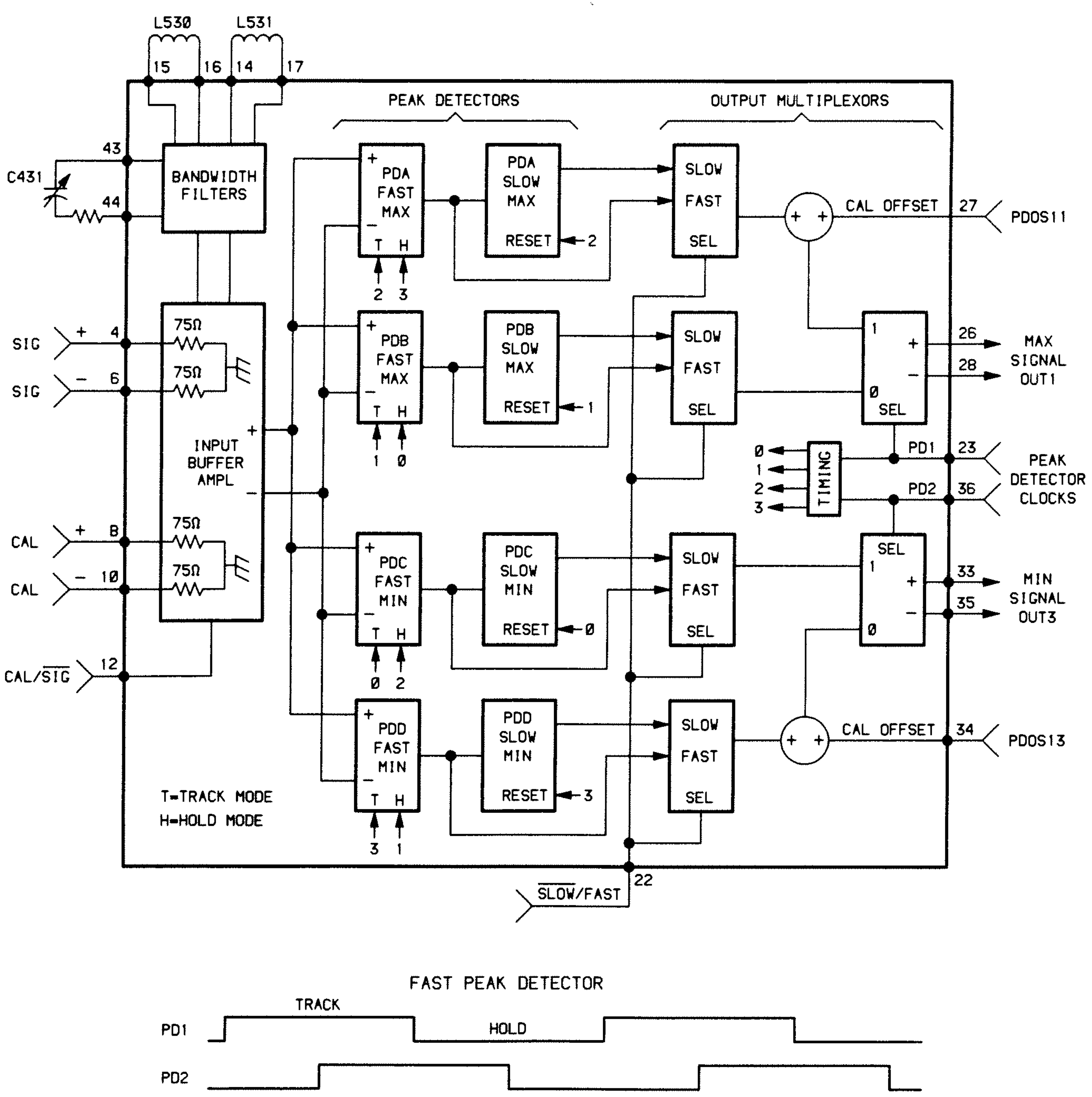
Peak detect mode for ENVELOPE acquisitions is turned on by setting $\overline{\text{PD}}$ LO at pin 21 and SLOW/$\overline{\text{FAST}}$ HI at pin 22 of Peak Detector U440. The differential ECL peak-detector clock signals (PD1 and PD2) toggle under control of the Phase Clock Array (U470, diagram 11) to control the internal peak detector switching and multiplexing of the positive and negative peaks to the OUT1 and OUT3 stages. The table in Figure 3-4 shows timing of the peak detector clocks and illustrates how alternate peaks are applied to the SIG1 and SIG3 inputs of the CCD.

DC offsets between the internal peak detectors of U440 are nulled out by voltage levels applied from the DAC System (diagram 6) to pins 27 and 34. Bias current for the input stage of U440 is set by R430 on pin 47, and output stage bias is set by R440 on pin 32.

The +CAL and −CAL inputs at pins 8 and 10 are identical to the signal inputs, but they are used only for the application of test signals during calibration or diagnostic testing. Selection of the inputs is controlled by the CAL/$\overline{\text{SIG}}$ signal. The test signals applied to pins 8 and 10 from the DAC System are used for testing and calibrating the Peak Detectors, the CCD/Clock Drivers, the CCD Output circuits, and the A/D Converter.

Common-Mode Adjust

The Common-Mode Adjust circuits (U540A and B, Q540, Q640, and associated components) allow varying, under control of the System μP, the common-mode voltage levels at the output of the CH 1 Peak Detector. (Similar circuitry performs the same task for the CH 2 Peak Detector.) Adjusting these dc levels changes the gain of the CCD and is done during self-calibration to control the overall gain of the Peak Detector-CCD subsystem. The CH 1—OUT1 Common-Mode Adjust circuit is described; the remaining Common-Mode Adjust circuits operate identically.



MAX	A	PD / DISPLAY	HOLD / DISPLAY	TRACK	PD	PD / DISPLAY	HOLD / DISPLAY	TRACK
MAX	B	TRACK	PD	PD / DISPLAY	HOLD / DISPLAY	TRACK	PD	PD / DISPLAY
MIN	C	PD	PD / DISPLAY	HOLD / DISPLAY	TRACK	PD	PD / DISPLAY	HOLD / DISPLAY
MIN	D	HOLD / DISPLAY	TRACK	PD	PD / DISPLAY	HOLD / DISPLAY	TRACK	PD

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Figure 3-4. Simplified Peak Detector block diagram.

The OUT1+ and OUT1− common voltage is level shifted and attenuated, then applied to U540A pin 3. Operational amplifier U540A compares the common-mode level with the attenuated CM11 level from the DAC System. The output of U540A drives Q640 to supply more or less current to the collector circuit thus raising or lowering the voltage on pin 25 of U440. Common-mode current is drawn by pins 26 and 28 via R540C and R450D to complete the feedback loop to the operational amplifier. Additional current is drawn by VCC1 (pin 25), part of which is supplied via R651 to reduce the stress on Q640. Emitter resistor R647 provides protection to Q640 against excessive current demand in the event of a short or overload. Resistors R647 and R651 also limit the voltage gain of Q640 to stabilize the feedback loop of the Common-Mode Adjust circuit.

Charge-Coupled Devices (CCD)

The CCD portion of the CCD/Clock Driver hybrid is a MOS-type integrated circuit that functions as a very fast analog shift register. A signal applied to the input is sampled by being converted to charge packets. These charge packets are then shifted through the CCD registers by MOS-circuit gating at intervals determined by the clock rates applied by the Clock Driver integrated circuit portion of the hybrid. The internal arrangement of the CCD analog shift registers and the total amount of storage space permits the input signal to be sampled at a high clock rate when necessary for the higher frequency signals. The charge packet samples are temporarily stored and then shifted out of the CCD at a much slower rate than the sampling rate. An inexpensive A/D Converter can be used to digitize the signal and slower memory circuits used to store the digitized samples. This type of operation is called Fast-In-Slow-Out (FISO) and is used at SEC/DIV settings of 50 µs and faster. At SEC/DIV settings of 100 µs and slower, the CCD runs with a constant clock rate of 500 kHz in a mode called Short Pipeline (discussed later).

A simplified diagram of one-half of one CCD is shown in Figure 3-5. The half shown, the SIG1 side or Side 1, is nearly identical to the SIG3 side (Side 3) of the CCD. Each side provides temporary storage of 528 analog samples for a total storage of 1056 samples of a single channel. The extra samples above that needed for the 1024-byte waveform record are needed for proper clock switching between the Fast-In and Slow-Out portions of the FISO cycle. The CCD has a Serial-Parallel-Serial (S-P-S) architecture. Each side has a 16 sample serial input "A" register, a 16 × 33 sample parallel storage "B" register, and a 16 sample serial output "C" register. Two such SPS sections are shown in Figure 3-5.

All the registers require four-phase gate clocking to move the sample charge packets through the CCD. Hence, there are four "A" register clocks, four "B" register clocks, and four "C" register clocks. There is also a Transfer In (TI) clock to shift samples from the serial A register into the B register and a Transfer Out (TO) clock to move them from the B register to the C register. The $\overline{\text{RESET}}$ clock discharges the output wells between output sample intervals so that charge does not accumulate at the input to the source-follower output amplifier. The S1 Sample clock samples the analog input signal at the side one inputs. Sampling occurs on the falling edge of S1, and the charge packet representing the instantaneous analog signal value is initially formed under the first "1A" gate (the first gate that is driven by the A register Phase 1 clock).

An extra input gate is added to Side 3, the other side of the CH 1 CCD array (not shown in Figure 3-5) to accept the Side 3 charge packets and permit their movement through the CCD to be synchronized with the Side 1 samples. The S3 Sample clock (opposite in polarity to the S1 Sample clock) performs the sampling function of the SIG3 signal. This sampling scheme doubles the effective sample rate of the CCD. Thus, the 100 megasample per second sampling rate is achieved with 50 MHz "A" register clocks. All register gates are driven with bipolar square-wave signals of +5 V to −5 V. The $\overline{\text{RESET}}$ clock signal also switches between +5 V and −5 V, but it is HI for only 200 ns of the total 2 µs period.

In FISO mode, 16 samples are shifted down the serial input A register at a clock period equal to 0.04 times the SEC/DIV setting. On every sixteenth clock cycle, the positive 2A clock pulse is replaced by a single positive pulse that moves all the charge packets into a transfer-in register at the head of the B register array. The A register is then empty and ready to accept new serial-in samples. The B register clocks run at 1/16 the speed of the A register clock rate so that the A register will be filled prior to each B register clock. In this way, the B register is filled with samples that are moved in parallel through the array. During this Fast-In portion of the input cycle, unneeded charges that arrive at the output C register due to the way that the input signal is continually sampled (until a trigger occurs) are emptied from the CCD through the output diffusion (OD1). When the Time Base Controller determines that the proper number of samples have been stored in the CCD after the trigger occurs, the mode changes to Slow-Out. The C register and RESET clocks then toggle at a constant 500 kHz rate to shift samples out of the CCD to be digitized.

The Short Pipe mode of the CCD is in effect at SEC/DIV settings of 100 µs and slower. The CCD is operated at a continuous 500 kHz rate. Samples are

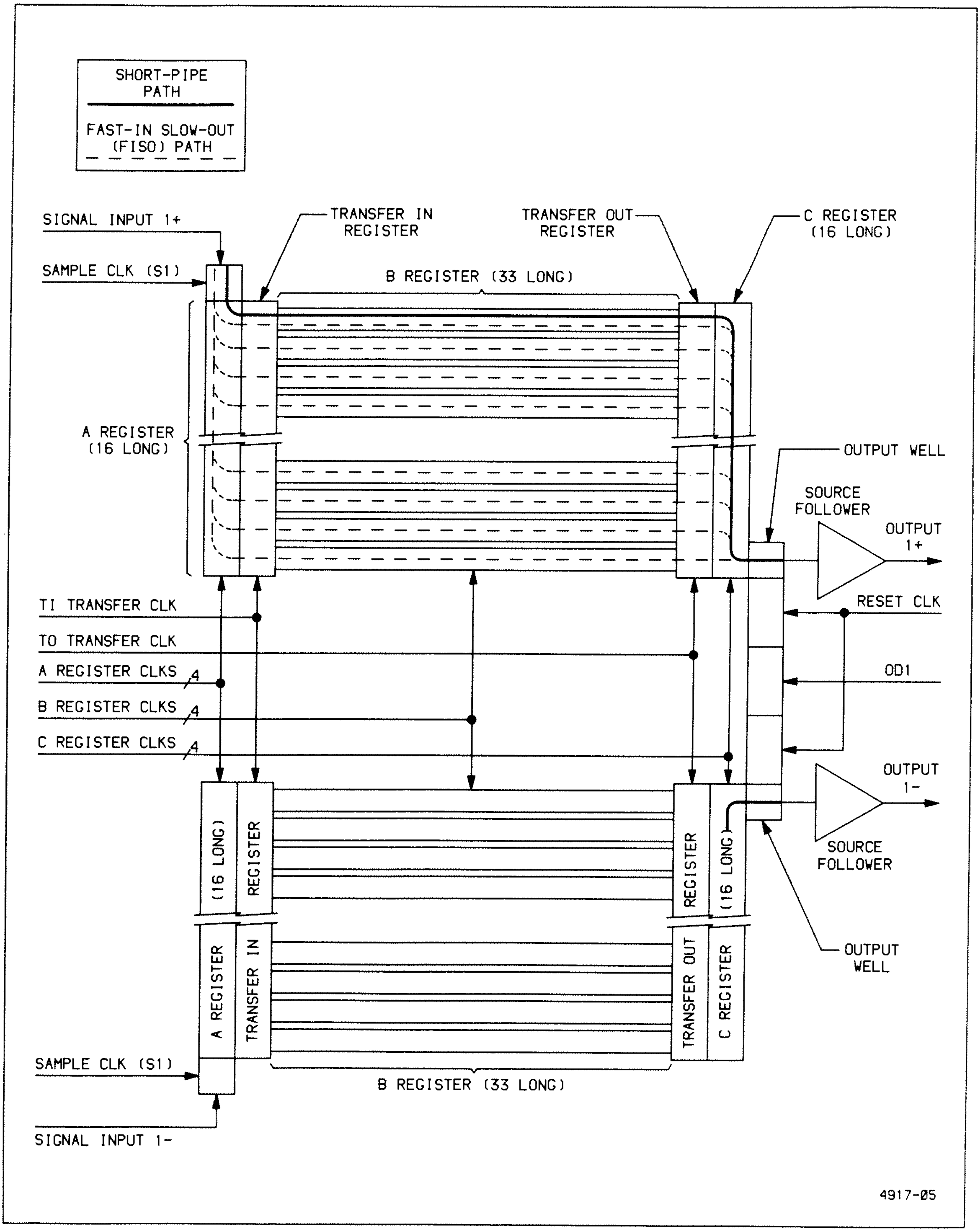

Figure 3-5. Simplified CCD architecture.

shifted serially through the CCD via one B register channel only. The TI clock toggles continuously to move the sample charge packets from the first A register position into the active B register channel, shown in Figure 3-5 as the Short-Pipe (slow-in, slow-out) path.

The output diffusions for sides 1 and 3 (OD1 and OD3) are independently driven from the DAC system. Varying the voltages on these nodes varies the gain of the CCD. These adjustments are used in conjunction with the Common-Mode Adjustments to calibrate the gains of the Peak Detector and CCD/Clock Driver subsystem. Gain increases with increasing OD voltage and decreasing Common-mode voltage; therefore, the calibration firmware moves these voltages in opposite directions to effect calibration.

Clock Drivers

The Clock Driver integrated circuits internal to the CCD/Clock Driver hybrids develop the four "A" register clocks, the four "B" register clocks, the two sample clocks, and the transfer input (TI) clock for the CCD. The high-speed Sample A Register and TI drivers are differential class A drivers through thick-film load resistors on the hybrid. The B Register drivers are slower with active pull-up and pull-down totem-pole outputs similar to conventional TTL driver outputs.

The 1A and 3A high-speed clocks are accessible at probe pins 21 and 20 of the hybrid devices. These pins (P1A and P3A) are isolated from the actual CCD gates by internal 875-ohm series resistors. Terminate the signals into 50 ohms to view them. Using the standard 10 MΩ probe will cause the signals to have a displayed rise time of about 30 ns; the actual rise time internally is about 2 ns.

Channel 1 CCD bias current for the high-speed drivers is set by the feedback circuit of U360A and Q375. The drivers are biased by injecting current into the IS input (pin 29). Increasing the current makes the LO level of the high-speed clocks more negative; decreasing the current raises the LO level. The HI level of the clocks is always within a few hundred millivolts of the +5 V supply to the hybrid. For controlling the negative clock level, the common-mode level of the 1A and 3A clocks at the P1A and P3A outputs is applied to the input of U360A. This level is compared to the midpoint between the +5 V and −5 V supplies. Operational amplifier U360A drives the base of Q375 to a level such that the current injected into IS sets the common-mode level of P1A and P3A equal to the voltage at pin 3 of U360A (the voltage supply midpoint value). Since the HI clock levels at P1A and P3A are approximately at the +5 V supply level, the LO levels of the clocks then are set to approximately the −5 V supply level. Bias stability is thereby maintained over temperature and component variations.

Each Clock Driver integrated circuit has only two B register drivers. Therefore, the B register drive task is shared between the two CCD/Clock Driver hybrids. The Clock Drivers in U450 drive the 1B and 3B gates of both CCD arrays, and the ones in U350 drive the 2B and 4B gates of both CCD arrays (see diagram 10). The Transfer Out (TO) gate timing has to match the 4B gate timing; therefore, the TO gate inputs of each CCD are tied to the 4B gate signal through R345.

Since the B register drivers have totem-pole outputs with emitter-followers for pull-ups, their HI state outputs are reduced from the +5 V supply by approximately 1 V. Resistors R466, R465, R366, and R365 reduce the transient current flow into the B register gates when the B drivers change state.

Resistor array R470 provides proper termination for the ECL logic inputs to the CH 1 Clock Drivers.

"C" CLOCK DRIVERS. These are external clock drivers consisting of Q450, Q550, Q460, Q560, and associated components. They provide the necessary −5 V to +5 V clock swings for the CCD "C" register gates. Each driver is simply an inverting buffer which accepts TTL inputs from the Phase Clock Array. During the Fast-In portion of the FISO acquisition cycle, the outputs of all four drivers are held HI by the Phase Clock Array. During the Slow-Out portion of the cycle, and at SEC/DIV settings of 100 μs and slower, the C Clock Drivers toggle at a 500 kHz rate in the normal four-phase sequence.

RESET DRIVER. This driver consisting of Q551 is identical to the C Clock Driver states. It takes the $\overline{\text{RESET}}$ signal input from U731C in the System Clocks circuitry (diagram 7). Like the C Clock Drivers, the Reset driver is driven HI during Fast-in and toggles at other times. The Reset driver output is held HI for only 200 ns of the 2 μs clock period.

−2 V Regulator

A −2 V supply needed to terminate all of the high-speed ECL signals on the Main circuit board is formed by U580B and Q580. The circuit is a simple series-pass regulator with R585 and R586 developing the −2 V reference for operational amplifier U580B from the −5 V supply. Feedback is through R587. Collector load resistors R486, R487, and R488 limit the power dissipation of Q580 and protect it from possible short circuits of the −2 V supply.

TRIGGERS AND PHASE CLOCKS

In this scope, the acquisition system continuously acquires input samples. When the user-specified number of "pretrigger" samples have been moved into the CCD arrays, the trigger system is allowed to recognize trigger events. Sampling of the signal input to the CCD arrays continues (with new samples pushing out old samples) until a trigger occurs. After the trigger, the number of "post-trigger" samples needed to fill the waveform record are moved into the CCD arrays and sampling is stopped. The acquired samples are then moved out of the CCD arrays, digitized, stored to memory, and displayed. The acquisition system then begins again to fill the "pretrigger window" for the next acquisition; and, when that has been done, the trigger system is enabled to look for the next trigger event.

The Trigger circuits (diagram 11) detect when the user-defined triggering conditions are met and then allow the acquisition to be completed. When the triggering signal limits defined by the user for slope, level, and variable holdoff are detected by A/B Trigger Generator U150, the resulting trigger output is applied to Trigger Logic Array U370, where triggering conditions of delay mode, delay time or delay events count, and optional trigger sources are taken into consideration. The Trigger Logic Array outputs several trigger-recognition and acquisition-control signals that cause the acquisition system to finish the "post-trigger" portion of the acquisition.

The Phase Locked Loop and CCD Phase Clock circuits (diagram 11) control sampling and shifting operations of the CCD/Clock Driver hybrid. The Phase Locked Loop synthesizes the 200/250 MHz sample clock driving the CCD Phase Clock Array. The CCD Phase Clock Array uses this "master" clock to generate other CCD clocks in accordance with mode data written to it from the System μP.

A/B Trigger Generator

The A/B Trigger Generator circuit, composed of U150 and associated components, provides for selection and analog-type trigger detection from five input signals for each of the A and B triggers. These are the CH 1 and CH 2 vertical inputs, the EXT 1 and EXT 2 trigger inputs, and the line-trigger input (A trigger only). Two multiplexers internal to U150 select one of these signals as the trigger source for A Trigger and one (excluding the LINE signal) for B Trigger. Source selection depends on the states of the $\overline{\text{SR0A}}$, $\overline{\text{SR1A}}$, and $\overline{\text{SR2A}}$ (source select—A trigger) lines for the A Trigger and on $\overline{\text{SR0B}}$, $\overline{\text{SR1B}}$, and $\overline{\text{SR2B}}$ for B Trigger. The appropriate select bits are written into register U140 by the System μP whenever the operator makes a triggering condition change using the trigger source menus.

Control data from the System μP defining trigger mode, trigger coupling, and trigger slope are clocked serially (one bit at a time) from the CD (control data) line into two storage registers internal to U150. Clocking the $\overline{\text{CCA}}$ (control clock A) line moves the setup data to the A control register, while clocking $\overline{\text{CCB}}$ moves data to the B control register. When the control data has been loaded, each trigger circuit begins comparing its selected input signal to the user-defined trigger level for that trigger channel.

When the defined triggering criteria are met for either A or B, the associated trigger outputs (ATG, $\overline{\text{ATG}}$ for A Trigger; BTG, $\overline{\text{BTG}}$ for B Trigger) will go to their asserted (true) states. The exception is when the A Trigger holdoff has not finished (ATHO is still HI). When the holdoff ends, however, the next trigger event on the selected A Trigger input will assert the A Trigger output gates.

Each differential trigger gate is inverted and current buffered by a pair of differential transistors that allow quick response to the trigger edges by Trigger Logic Array U370.

Trigger Logic

The Trigger Logic circuit consists primarily of Trigger Logic Array U370. The Trigger Logic Array provides final trigger-source selection; trigger-point delays, delayed either by a specified amount of time or by a specified number of events; and ramp-control signals to the Jitter-Correction circuitry for resolving trigger-point ambiguities. The Trigger Logic Array also produces the trigger and external clock signals necessary to control operations of the CCD Phase Clock circuit.

The three enable inputs to U370, E1B (A3), E2B ($\overline{\text{WR}}$), and E3B ($\overline{\text{ACQSEL}}$), are all set LO whenever writing to addresses between 6080h and 6087h to enable the address inputs (A0, A1, and A2). The choice of eight addresses between 6080h and 6087h provides for different operating requirements of the Trigger Logic Array.

Depending on the address written to, one of the following actions may occur:

Mode control data may be loaded into the internal mode register.

The internal events and delay counter low-byte or high-byte of the number of events to be counted or delay may be loaded.

Various strobes used for internal control of the Trigger Logic Array may be generated.

Table 3-5 shows the action taken for each address selected.

Table 3-5

Trigger Logic Array Addresses (6080h-6087h)

Address Bits			Circuit Operation Initiated
A2	A1	A0	
0	0	0	Restart Acquisition
0	0	1	Force Manual Trigger
0	1	0	Load Mode Control Data from M0-M7
0	1	1	Latch Delay Counter Low-Byte from M0-M7
1	0	0	Latch Delay Counter High-Byte from M0-M7
1	0	1	Load Delay Counter from Delay Latches
1	1	0	Not Used
1	1	1	Reset All Latches

As previously mentioned, U370 provides final trigger-mode and source selection, dependent on data written from the System μP to a control register within U370 at address 6082h. The mode control data byte loaded from the M0-M7 input bus is built by the System μP and applied to the M0-M7 (mode) inputs from serial-input register U270 (diagram 5) via the GAD0-GAD7 bus lines. The data byte defines the A Trigger source, B Trigger source, Record Trigger source, Jitter Trigger source, and whether a single event or multiple events are needed to produce a trigger. Bit definition is shown in Figure 3-6.

After the control data byte is loaded and the acquisition is restarted, Trigger Logic Array U370 waits for EPTHO (end of pretrigger holdoff) to go HI at pin 28, indicating that the acquisition system has sampled the "pretrigger" points and is ready to complete the acquisition. With EPTHO set HI, the trigger logic begins watching the trigger source (as defined by the control data byte), waiting for a trigger event to occur.

Operation of the Trigger Logic Array is very sequential in the way it functions in the various trigger modes. An example is illustrated in the sequence of events for B RUNS AFTER trigger mode.

1. The System μP loads the "delay count" and "control mode" registers, then starts the acquisition (indicated by setting RSTACQ HI at TP370).

2. The Trigger Logic Array watches for EPTHO at pin 28 to go HI; signaling that the defined number of pretrigger points have been sampled.

3. With EPTHO HI, the Trigger Logic Array watches MTG and $\overline{\text{MTG}}$ (main trigger gate) for an A trigger event to start the delay counter. When a trigger occurs, JTRIG (jitter trigger) is generated, starting the jitter-correction circuits (via the RAMP and $\overline{\text{RAMP}}$ signals).

4. The defined delay count is decremented to zero by the DELCLK (delay clock) signal on pin 67 from Phase Clock Array U470. If the mode were A Delayed by B Events, the B Trigger events would be used to decrement the delay counter.

5. In this example, when the internal Delay count reaches 0, a RTRIG (record trigger) is generated for B RUNS AFTER. RTRIG is the "record trigger" point on the displayed waveform. If the mode were B TRIG AFTER, the Trigger Logic Array would begin watching for a B Trigger to occur on the DTG and $\overline{\text{DTG}}$ input pins (Delay Trigger Gate).

6. Time Base Controller U670 (diagram 8) counts the post-trigger samples as they are acquired. When the required count is reached to complete the acquisition, it resets EPTHO to LO and further triggers from the Trigger Logic Array are prevented from being generated.

The Time Base Controller then starts moving digitized samples to the Acquisition Memory and, when finished, tells the System μP that the acquisition is done. The System μP may then restart the whole process again for the next acquisition by writing appropriate data to the various trigger registers.

In external clock mode, the differential EXTCK and $\overline{\text{EXTCK}}$ (external clock) signals to the Phase Clock circuit replace the normal master-clock ($\overline{\text{MCLK}}$) signal and allows the B trigger events to be used as the events delay source.

CONTROL DATA BYTE

M7	M6	M5	M4	M3	M2	M1	MØ
JT1	JTØ	RT1	RTØ	ONEVNT	BTØ	AT1	ATØ

JITTER TRIGGER BITS

JT1	JTØ	SOURCE
Ø	Ø	A TRIGGER
Ø	1	B TRIGGER
1	Ø	END EVENTS
1	1	B TRIGGER

RECORD TRIGGER BITS

RT1	RTØ	SOURCE
Ø	Ø	A TRIGGER
Ø	1	END DELAY TIME
1	Ø	END DELAY EVENTS
1	1	B TRIGGER

ONE EVENT BITS

ONEVNT	EVENTS=1
Ø	NO
1	YES

B TRIGGER BIT

BTØ	SOURCE
Ø	DELAYED INST. TRIGGER
1	WORD TRIGGER OPTION

A TRIGGER BITS

AT1	ATØ	SOURCE
Ø	Ø	MAIN INST. TRIGGER
Ø	1	VIDEO TRIGGER OPTION
1	Ø	WORD TRIGGER OPTION
1	1	A*B TRIGGER

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Figure 3-6. Trigger Logic Array Control Data Byte.

The $\overline{\text{A TRIG}}$ and $\overline{\text{B TRIG}}$ outputs from Q287 and Q288 are TTL-buffered versions of the corresponding trigger signals and are routed to rear-panel BNC connectors.

Phase Locked Loop

The Phase Locked Loop circuit synthesizes the 200/250 MHz clock used by the Acquisition System. It consists of Phase/Frequency comparator U381 amplifier U580A, a voltage-tuned tank circuit, and a divide-by-50 counter internal to Phase Clock Array U470. The tank-circuit resonant frequency is set by the value of voltage-controlled capacitor CR580. The resulting clock is divided by 50 by the counter and is applied to the phase-frequency detector U381 on the FIV4 line. The FIV4 signal is compared to the reference clock REF4/5, and any phase or frequency error appears at the output of U381 as variable width pulses. These pulses are integrated by U580A to produce a dc voltage that represents the phase difference (fast or slow) and magnitude of error between the REF4/5 clock and the divided down master clock. This is the frequency-control voltage and varies the capacitance of varactor diode CR580, part of the tank circuit formed by the circuit board delay line and CR580. The tank is tuned by the control voltage so that the master clock frequency is precisely 50 times the reference frequency. Depending on the user-defined sweep rate and acquisition mode, the reference (REF4/5) will be either 4 MHz or 5 MHz, resulting in a 200 MHz or 250 MHz master clock (see Table 3-6).

Table 3-6

REF4/5 Frequency for Each SEC/DIV Setting

SEC/DIV Setting	REF4/5 Frequency	Phase Clock Array Clock Frequency
EXT CLK	Don't Care	EXT CLK
200 ns and faster	5 MHz	250 MHz
500 ns	4 MHz	200 MHz
1 μs	4 MHz	200 MHz
2 μs	5 MHz	250 MHz
5 μs	4 MHz	200 MHz
10 μs	5 MHz	250 MHz
20 μs	5 MHz	250 MHz
50 μs	Don't Care	1 MHz
100 μs	Don't Care	1 MHz

CCD Phase Clock

The CCD Phase Clock generates properly phased and frequency-related clocks that control most of the Acquisition system. These functions include moving samples into the CCD arrays, shifting within the arrays, jitter-correction control, peak-detection control, and trigger-delay clock generation. These clocks are derived from the 200/250 MHz master clock generated by the internal oscillator and the Phase Locked Loop circuit.

Two operating modes exist for the CCD arrays; FISO (fast-in, slow-out) and Short-Pipe. The Phase Clock circuit is set up to generate proper clocking signals for either mode by loading data into Gate Array Control Register U270 (diagram 5). This data is applied to U470 on the CC0-CC3 (chip control 0-3) lines and on the PD_{OFF} (peak detector off) line. The PD_{OFF} line enables/disables the peak-detector output lines (PD1, $\overline{\text{PD1}}$, PD2, and $\overline{\text{PD2}}$) and thus peak detection mode (see that description). The CC0-CC3 inputs control operating mode and clock selection as shown in Table 3-7.

FISO MODE. As explained in the CCD description, each CCD is made up of two identical differential channels using a serial-parallel-serial (SPS) structure. Samples are moved into and shifted within the CCD arrays using properly phased, overlapping clocks. Figure 3-5 shows a basic CCD structure (see CCD description, diagram 10).

Depending on whether the Side 1 channel or Side 3 channel is being acquired, the corresponding sample gate (SAM1 or SAM3) will go HI. This moves the present level of the input signal into the input well of the CCD arrays. Before the sample gate returns LO, the ϕ1A (phase 1-A register) clock goes HI and the charge is shared by the adjacent cells (input and ϕ1). When the sample gate returns LO, all charge moves to the ϕ1 cell. The ϕ2A clock then goes HI and charge is distributed into both the ϕ1 and ϕ2 cells. When ϕ1 returns LO, all charge will move into the ϕ2 cell. Similar shifts occur using the ϕ3A and ϕ4A clocks until ϕ1 occurs again, completing the cycle.

When 16 samples have been acquired in the A register, the TI (transfer into B) clock moves all 16 samples from the ϕ1A cells in parallel into the B register. The four phases of the B clocks shift samples down the 16 parallel B registers in a manner similar to that just described for the A register but at 1/16th the rate. The $\overline{\text{TTL1B}}$ clock (TTL-version of B clock ϕ1) is output to the Time Base Controller and allows it to keep track of how many samples have been acquired (in multiples of 32). This allows the Time Base Controller to know when the proper number of "pretrigger" points have been acquired and when to enable the Trigger Logic Array.

Table 3-7

Phase Clock Array Control Lines (CC3 through CC0)

SEC/DIV Setting	Control Bits				Mode
	CC3	CC2	CC1	CC0	
EXT CLK	0	0	0	0	
200 ns and faster	0	0	1	0	FISO
500 ns	0	1	0	0	FISO
1 μs	0	1	1	0	FISO
2 μs	1	0	0	0	FISO
5 μs	1	0	1	0	FISO
10 μs	1	1	0	0	FISO
20 μs	1	1	1	0	FISO
50 μs	x	x	0	1	FISO (Short-Pipe)
100 μs and slower	x	x	1	1	Short-Pipe

Once enabled, the Trigger Logic Array begins counting its predefined delay while samples continue to be acquired. The DELCLK (delay clock) output to the Trigger Logic runs at one-half the sample-clock rate, allowing the Trigger Logic to complete any defined delay. When delay is done, the JTRIG and RTRIG signals may be generated. When the JTRIG occurs, the RAMP and $\overline{\text{RAMP}}$ signals from the Trigger Logic start the Jitter-Correction Ramps. The JTRIG signal to U470 causes the TL0 (trigger location-bit 0) bit to latch the phase (HI or LO) of the master clock, defining which half of the cycle the trigger event occurred. The internal slow-ramp logic circuitry of U470 becomes enabled and, on the next two edges of the master clock, asserts the two pairs of slow-ramp (SLRMP) outputs. These outputs reverse the charge direction of the Jitter-Correction Ramp circuits (diagram 12) and start the Jitter-Correction Counters (diagram 13) on opposite edges of the master clock. See those descriptions for further information on trigger-jitter correction.

Depending on trigger mode, the RTRIG (record trigger) line will be asserted some time after JTRIG occurs. RTRIG is synchronized to the B-register clock and is output to the Time Base Controller on the SYNTRIG (synchronous trigger) line, telling it to start counting post-trigger samples. The RTRIG also loads a register internal to U470 with the present sample count to locate the trigger event (explained later). When the Time Base Controller has completed the post-trigger count, it will set SO (slow out) HI, switching the Phase Clock Array mode from "Fast In" to "Slow Out" mode. The various phase clocks are now derived from the 1 MHz 2XPC clock (from the Time Base Controller) instead of the 200/250 MHz master clock, and samples are shifted out of the CCD arrays at the A/D conversion rate.

Outputs TL0-TL4 (trigger location bits 0 through 4) define the trigger location within ±1/2 of a sample interval and allow the extra samples taken at the beginning and end of the CCD sample array contents to be discarded. Defining and discarding these samples is done because the trigger event may occur at any of 32 locations within the two A registers. Outputs TL1-TL4 locate the trigger at one of these 32 sample positions, allowing samples before the start of the waveform to be discarded. Output TL0 defines trigger position within the sample interval to either half of the interval (phase 1 side or phase 3 side) by sampling the phase of the master clock when the trigger occurred.

SHORT-PIPE MODE. A second acquisition mode, Short-Pipe mode, is used at SEC/DIV settings 100 μs/div and slower. In Short-Pipe mode, the ϕ2A clock that transfers samples down the input (A) register is disabled; and instead, the TI (transfer into B array) clock shifts samples straight down the first register of the B array to the output well. Sampling occurs at 1 MHz in Short-Pipe mode (500 kHz each side of the CCD array) as the various phase clocks are derived from the 2XPC clock. Trigger delays are generated at the SDC (slow-delay clock) rate since Short-Pipe mode connects the DELCLK output to the SDC input. Since sampling is occurring at a 1 MHz rate and the SEC/DIV is set so that a sample rate slower than this is required, some of the samples must be discarded. The discrepancy is resolved by Time Base Controller by counting and discarding the proper number of samples between those it allows to be saved. This allows effective sample rates much lower than the actual 1 MHz rate and, by routing the SDC signal to DELCLK, allows the trigger delays to be counted in terms of effective sample events.

In FISO mode, the $\overline{\text{TTL1B}}$ (TTL-level phase 1B) signal runs at 1/16 of the A-register clock rate and is used by the Time Base Controller to keep track of how many FISO samples have been taken. Each $\overline{\text{TTL1B}}$ clock indicates that 16 sample intervals have occurred. In Short-Pipe mode, the $\overline{\text{TTL1B}}$ clock runs at the A-register clock rate. By using the $\overline{\text{TTL1B}}$ count and the TL0-TL4 data, the Time Base Controller (U670, diagram 8) can precisely determine when the acquisition is finished.

TTL4C is a TTL version of the phase 4 clock for the C (output) register and runs at all times except during RESET. This is one of the signals required by the System Clock Generators for producing correctly timed Output Sample Clocks to the CCD Output circuitry (diagram 14) and the $\overline{\text{RESET}}$ clock to the CCD arrays.

JITTER CORRECTION RAMPS

The Jitter Correction Ramps located on diagram 12 are a portion of two dual-ramp timing circuits used to detect and measure the time difference between a trigger event and the sample clock. This information is needed when doing acquisitions at SEC/DIV settings greater that 500 ns to correctly place the data points obtained on different trigger events. The Jitter Correction Counters are located on diagram 13.

Jitter Correction Ramps

Operation of the RAMP1 and RAMP2 circuits is identical; therefore, only the RAMP1 Jitter Correction circuit will be described. Both Jitter Correction Ramps are initiated by the same trigger event, but they are switched to their slow-discharge mode on opposite edges of the sample clock. By switching on opposite edges, the trigger point has two distinct references which define the trigger point, allowing the System µP to detect and correct for metastable states of the trigger recognition logic.

The ramp generator consists of a constant current source used to rapidly charge an integration capacitor when the trigger event occurs and a second current source used to discharge the capacitor (more slowly) after the proper edge of the sample clock occurs. The fast-charge time is the actual time from the trigger event to the appropriate sample-clock edge. The time it takes the slow-discharge mode to discharge C491 gives a numerical representation (counted) of how high the ramp level reached when C491 was fast charging; and therefore, the time of the fast ramp.

Fast charging rate is determined by the constant current source formed by U590A, Q493, and associated components. The charging current is nominally 20 milliamperes through R590 and Q493. The voltage drop across R590 balances the +7.5 volt reference at pin 2 of U590A and keeps Q493 turned on just enough to maintain the balance at the operational amplifier inputs.

This charge current is switched through either Q491 or Q492, depending on whether the ramp should be ramping down slowly or ramping up quickly. When waiting for a trigger to occur, the SLRMP1 (slow-ramp 1) will be LO, turning Q491 on. Charging current from Q491, which would normally charge integration capacitor C491 (and the 50 pF circuit-board capacitor), is shunted to −5 volts by Q490, which is turned on by a HI $\overline{\text{RAMP}}$ (fast ramp) signal applied to its base.

RAMP CLAMPING. The clamping circuit made up of U590B, CR490, and associated components, holds the ramp summing-node voltage (collector of Q490) at zero volts while the circuit is waiting for a trigger to occur (signaled when RAMP and $\overline{\text{RAMP}}$ go to their true states). The summing-node voltage is applied to U590B on pin 6 where it is compared to the zero-volt clamp level (ground) on pin 5. When the summing node attempts to go below ground while Q490 is on, U590B will conduct more to maintain the balance at the input pins, thereby clamping the summing node at zero volts via R592 and CR490.

Transistor Q380 and its associated components clamp the positive peaks of both ramps at +3.2 volts via CR491. This clamping takes place at SEC/DIV settings slower than 500 ns/div because the SLRMP signal doesn't occur soon enough after the RAMP signal starts the ramp to reverse the ramp slope before the +3.2 V level is reached.

RAMP SWITCHING. When Trigger Logic Array U370 (diagram 11) detects that a trigger event has occurred, it sets the RAMP and $\overline{\text{RAMP}}$ signals to their active (true) states. The LO $\overline{\text{RAMP}}$ signal turns Q490 off to allow the integration capacitor to begin a fast charge, and the HI RAMP signal turns Q392 on to reverse bias CR490 and remove the clamp circuit from the summing node.

The charging current now linearly charges C491 and the circuit board capacitance positive (holding STOP1 LO through U490) until the proper edge of the next sample clock occurs (see Figure 3-7). This switches the SLRMP1 and $\overline{\text{SLRMP1}}$ signals to their true states, turning off Q491 and turning Q492 on.

With Q492 on, the charging current is routed through R497, producing a HI START1 signal and enabling the RAMP1 Jitter Correction Counter circuit (diagram 13).

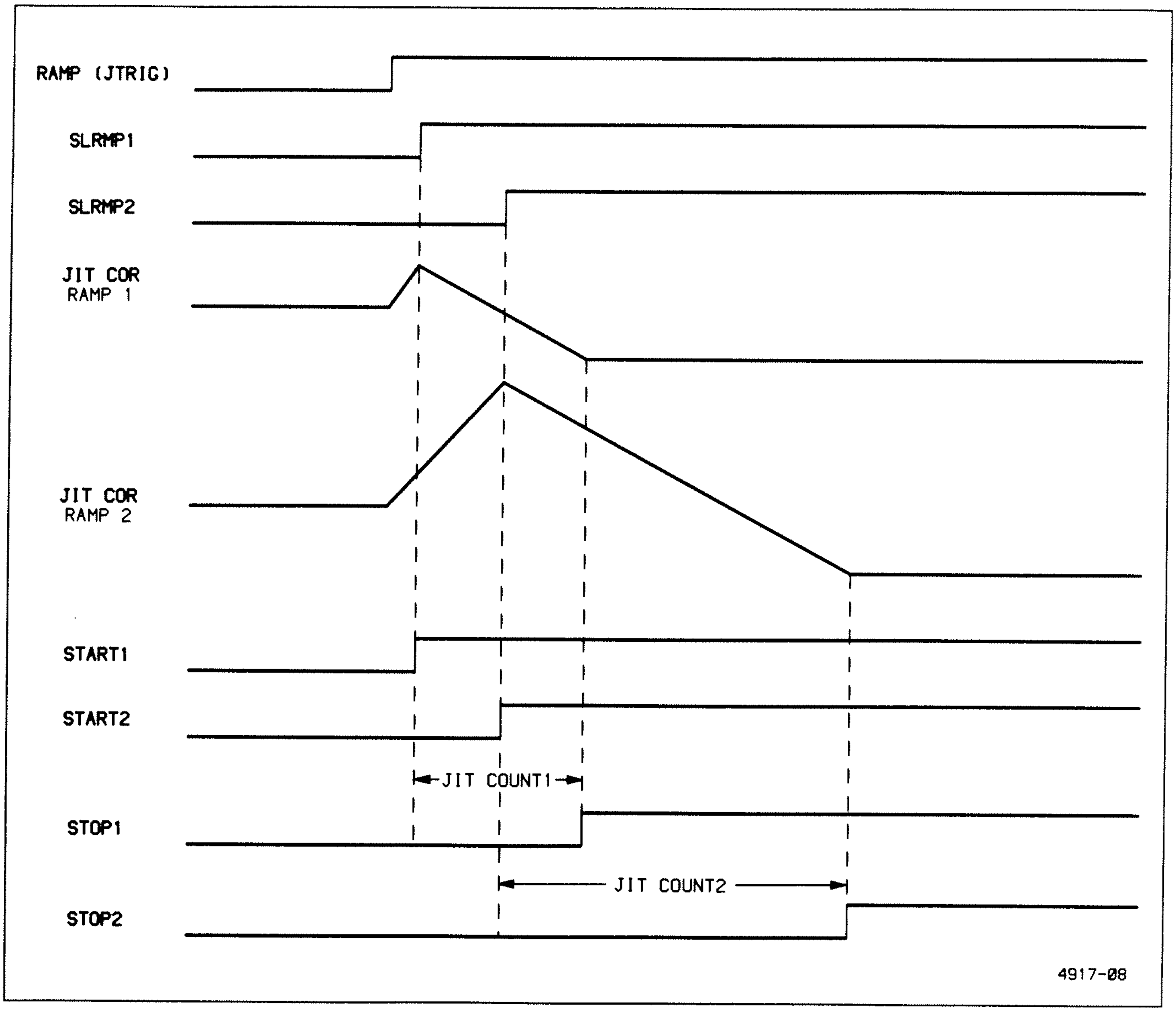

Figure 3-7. Jitter correction waveforms.

Since Q491 is now off, C491 begins the slow-ramp discharge through Q495 and R493. When the voltage held on C491 crosses the switching threshold of U490, STOP1 is switched HI to turn off RAMP1 Jitter Correction Counter at the proper count.

At the time of calibration, the JIT1 GAIN (jitter gain—ramp 1) value is set to the base of the discharge current source transistor, Q495, so that the ratio between charging rate and discharging rate is 1250:1 (approximately 20 mA from the charging current source to approximately 16 μA discharge current from Q495). The slow discharge time of C491 allows the RAMP1 Jitter Correction Counter to convert the peak amplitude of RAMP1 (dependent on the time that C491 was allowed to fast charge) into a count relating trigger-event position to the sample-clock edge.

After the Jitter Counter has been read, the RAMP, $\overline{\text{RAMP}}$, SLRMP1, and $\overline{\text{SLRMP1}}$ signals will be reset to their inactive states. This again clamps the summing-node voltage at zero volts and reapplies the charging current to the node in preparation for the next trigger event.

RAMP2. As mentioned earlier, the RAMP2 Jitter Correction circuit is running simultaneously, referenced to the opposite edge of the sample clock. The RAMP2 Jitter Correction Counter produces a count defining the trigger point relative to the opposite edge of the sample clock. Since both ramps have a possibility of an error in their slow-ramp starting times (due to metastable switching of the SLRMP1 and SLRMP2 signals) there will always be a chance of error present in the trigger-position count. The count from both ramps is checked, and the value closest to the nominal midrange count will be used by the System μP when placing the repetitively sampled data points. If both counts are in error, that acquisition is discarded.

TRIGGER HOLDOFF, JITTER COUNTERS, AND CALIBRATOR

Circuitry shown in diagram 13 performs a variety of functions.

The Trigger Holdoff circuits allow a delay to occur between the occurrence of a triggering event and when the A/B Trigger Generator is allowed to recognize another trigger event. Variable Holdoff can help the user prevent double triggering on aperiodic signals (such as complex digital words).

The RAMP1 and RAMP2 Jitter Correction Counters measure the time difference between the asynchronous trigger event and the actual sampling point of the waveform data. That information is needed by the System μP to place the random samples taken in REPET acquisition mode correctly with respect to data points taken in the previous acquisitions to fill the waveform record.

The Calibrator circuit generates a square-wave output having precise amplitude and frequency characteristics. The CALIBRATOR signal provided at the front-panel connector is useful for adjusting probe compensation and verifying VOLTS/DIV and SEC/DIV calibration.

The Side Board Address Decoder included in the circuitry is used by the System μP to enable the appropriate register or buffer on the Side board to read the Jitter Correction Counters, select the Holdoff Time, and communicate with the Front Panel μP.

Trigger Holdoff

The Trigger Holdoff circuit consists of a trigger-enabled, constant current source (actually one of three selectable sources added to a small permanent source) used to linearly charge a capacitor (one-of-two selectable cap values). The resulting integrator output is a linear ramp whose slope depends on the current-source and integration-capacitor selection. The ramp is applied to the Holdoff Comparator where it is compared to the user-definable (front-panel pot) holdoff-reference level. When the charging ramp crosses that level, the ramp rapidly discharges (resets) and ends the holdoff condition.

Holdoff Select

The Holdoff Select circuit, under System μP control, determines which of the Holdoff Current Sources and which of the integration capacitors will be used to produce the holdoff ramp. Its outputs are set by the microprocessor by writing data into Holdoff Register U762, residing at address 620Ch. Output bits HO0 through HO2 (holdoff control bits 0-2) enable their corresponding current-source transistor when HI. Bit HO3 is used for selection of the integration capacitor. The $\overline{\text{FPRESET}}$ bit allows the system processor to reset the Front Panel μP (diagram 3).

Buffer U761, residing at read location 602Ch, allows the System μP to check the holdoff circuit setup and to monitor the status of the A Trigger (ATG) and trigger holdoff (ATHO) bits.

Holdoff Current Sources

The Holdoff Current Sources provide the constant currents used to charge the integration capacitors (producing a linear ramp). The circuit consists of four transistor current sources, three of which may be turned on or off under control of the Holdoff Select circuit.

The bases of the four current-source transistors, Q761, Q771, Q772, and Q773, are held one diode-drop below +5 volts by CR772 and R773. This results in precisely +5 volts being present on the emitter of any conducting current-source transistor. The amount of current is set by the value of emitter resistor(s). Transistor Q773 will always be on while the other three current-source transistors can be turned on or off by the HO control bit via the the associated emitter diodes. A LO at the cathode of one of these diodes will disable the associated current source by reverse biasing the transistor junction; a HI at the cathode of a diode enables the charging-current source via the associated emitter resistor.

Charging Capacitor Selection

The Charging Capacitor Selection circuit composed of Q783, Q782, and associated components, selects the integrating capacitance. The magnitude of the charging current from the selected current source, in combination with the capacitance value, of the integration capacitor, determines charge rate (slope) of the holdoff ramp; and thereby, the holdoff time. Table 3-8 illustrates the holdoff time as a function of the selected current source and charging capacitor.

Charging current is stored on capacitor C882 when holdoff intervals less than or equal to 10 μs are desired. For longer holdoff periods, capacitor C881 and C885 are placed in parallel with C882 by turning Q782 on. Transistor Q782 turns on when HO3 (holdoff select 3) is LO, turning Q783 off. This pulls the gate of Q782 high and turns it on, placing the parallel combination of C881 and C885 in parallel with C882. Due to the relative capacitance ratios (1000:1), C881 is the dominant integrating element in the three-capacitor parallel combination.

Holdoff-Ramp Comparators

Two Holdoff-Ramp Comparators, U871 and U881, watch the holdoff ramp. Comparator U871 compares the ramp level to the user-defined reference level while U871 compares it to a predefined "end-of-holdoff" level.

Initially, a HI on the $\overline{Q}$ output of Holdoff Logic flip-flop U872A keeps Q781 turned on. The integration capacitors are discharged, and all the charging current is being shunted away from the capacitors through Q781. The user-definable holdoff reference applied to U871 pin 2 via R863 will always be more positive than this discharged level, so the output of U871 applied to the Holdoff Logic will be HI. This removes the reset from the Holdoff Logic flip-flop U872A and enables the occurrence of a trigger event (ATG going HI) to clock it.

When a trigger event occurs, discharge transistor Q781 turns off, allowing the selected integrating capacitors to charge. When the charging ramp reaches the user-defined HOREF (holdoff reference) level, the output of ramp comparator U871 will go LO. This resets flip-flop U872A of the Holdoff Logic which, in turn, turns Q781 back on.

The low-impedance path through Q781 discharges the integration capacitor very rapidly. When this discharging ramp crosses the −4.6 volt level (defined by R887 and R888), the output of U881 will go LO, resetting the Holdoff Logic circuit. This ends the holdoff pulse and allows the next trigger to be accepted.

Transistor Q781 remains on until the next trigger event, at which time the cycle repeats itself. Propagation delays through the Analog Trigger and the Record Trigger devices ensure that the discharging ramp will always reach the −5 V level before another trigger event can start the next holdoff ramp.

Table 3-8

Holdoff Delay Range for Current Source vs Charging Capacitor Combinations

Charging Capacitor	Holdoff Delay Range			
	909 μA Current Source	90.0 μA Current Source	9.09 μA Current Source	827 μA Current Source
1000 pF	10 ns - 100 ns	100 ns - 1 μs	1 μs - 10 μs	
1.1 μF	10 μs - 100 μs	100 μs - 1 ms	1 ms - 10 ms	10 ms - 100 ms

Holdoff Logic

The Holdoff Logic initiates and controls the holdoff ramp and produces the holdoff pulse controlling the delay between one trigger event and the next. It starts the holdoff ramp when a trigger event is detected, begins ramp discharge when the user-defined HOREF level is reached, and ends the holdoff pulse when the ramp crosses the "end-of-holdoff" level.

Initially, the Set and Reset inputs of U872A will be HI, allowing the flip-flop to watch the ATG (analog trigger) line for a trigger event. While it is waiting, its $\overline{Q}$ output will be HI, keeping Q781 on and the integration capacitors discharged.

When an ATG occurs, the HI level at the input of the flip-flop is clocked to the Q output while the $\overline{Q}$ output goes LO. This LO turns Q781 off and allows the selected current source(s) to charge the capacitors. At the same time, the LO is applied to pin 10 of U872B, forcing its Q output HI. This is the ATHO (analog trigger holdoff) signal and indicates that an analog trigger has occurred. This signal is applied to A/B Trigger Generator U150 (diagram 11) to prevent it from recognizing another trigger until the holdoff time ends.

As the charging ramp reaches the user-defined (front-panel Holdoff pot) reference level, the output from comparator U871 will go LO. This $\overline{\text{CROSS}}$ (reference crossing) level is applied to U872A and resets the flip-flop. The $\overline{Q}$ output, now HI, turns Q781 on and begins discharging the ramp at a rapid rate. The HI $\overline{Q}$ output from U872A removes the Set level from U872B and allows the ENDHO (end of holdoff) level from U881 to reset the ATHO level LO when the discharging ramp reaches −4.6 volts.

As mentioned earlier, propagation delays in the A/B Trigger Generator and the Trigger Logic Array ensure that another trigger (ATG) will not occur until Q781 has discharged the integration capacitors fully to −5 V. This ensures that holdoff ramps always start from a known point, and thus maintains holdoff stability.

The width of the ATHO pulse represents the time from which one analog trigger event was accepted to when the next trigger event is allowed (next acquisition record). By varying this time (front-panel Holdoff control) the displayed waveform may be adjusted to exclude undesired trigger events (which may cause display instability).

Jitter Correction Counters

The RAMP1 and RAMP2 Jitter Correction Counters convert the discharge time of their associated Jitter Correction Ramps to binary numbers relating trigger-event positions to the edges of the sample clock. Since operation of both Jitter Correction Counters is identical, only the RAMP1 Jitter Correction Counter will be described.

The RAMP1 Jitter Correction Counter is an eight-bit counter that is started and stopped by signals from the RAMP1 Jitter Correction circuit. It counts the 8 MHz clock pulses over the interval when the Jitter Correction Ramp is discharging, thus converting the peak value of the ramp to a binary number. Since that value is directly proportional to the time difference between a trigger event and the next sample-clock edge, the number derived by the counter gives a precise time measurement of where the trigger occurred with respect to the sampled data. That information is used by the System μP to correctly place the random-sampled data points obtained in REPET acquisition mode with respect to the previously acquired random data points as the waveform record is filled.

Initially, the RAMP1 Counter (composed of U852A and U852B) is held reset by the HI from pin 6 of U841A. When the START1 (start counter 1) input goes HI (signaling start of the slow discharge of integration capacitor C491, located on diagram 12), the rising edge of the next 8 MHz clock pulse will enable the counter by clocking the $\overline{Q}$ output of U841A LO. The Q output of the "stop" flip-flop U841B is LO and enables U851B to pass falling-edge clock pulses to U852A at an 8 MHz rate.

The counter increments until the RAMP1 Jitter Correction circuit detects the discharge threshold has been crossed. When this occurs, STOP1 (stop counter 1) applied to U841B will go HI. The next rising edge of the 8 MHz clock disables U851B via U841B and stops the counter.

The System μP may then read the counter contents via U752 at address-decoded location 620Fh. Counter contents for the B Jitter Correction Counter may be read at location 620Eh.

When the jitter ramps are reinitiated (in preparation for the next trigger event), the START1 and STOP1 signals will return LO. The next rising edge of the 8 MHz clock will reset the Jitter Correction Counter by clocking pin 6 of U841A HI.

Address Decoder

Address Decoder U781 monitors the address bus to determine when various buffers and registers on the Side board are to be enabled for communication with the System μP. Table 3-9 illustrates this decoding.

Table 3-9

Side Board Address Decoding

Address (hex)	Selects or Enables
6208	LED Register
6209	Front-Panel Register
620A	No connection
620B	No connection
620C	Write/Read Holdoff Register
620D	Set Holdoff Flip-Flop
620E	Read Jitter Correction Counter 1
620F	Read Jitter Correction Counter 2

Calibrator

The Calibrator circuit is composed of U731, U831, Q831, and associated components. Output frequency is set by the CALCLK signal from the Time Base Controller (diagram 8). The output frequency follows the SEC/DIV setting from 50 ns/div to 20 ms/div and is set to display from 2.5 to 10 calibrator cycles across the ten graticule divisions over those settings. This feature allows quick and easy verification of the acquisition time base rates. The Calibrator circuitry is essentially a voltage regulator that is switched off and on, producing a square-wave output signal at the CALIBRATOR loop.

When the CALCLK (calibrator clock) signal, at the base of U831D (applied via R885) is LO, U831C (configured as a diode) is forward biased. This shunts bias current away from Q831, keeping it turned off. When Q831 is off, the front-panel CALIBRATOR output is pulled to ground potential, through R831, thereby setting the lower limit of the CALIBRATOR square-wave signal.

As the CALCLK signal goes from LO to HI, the base of U831D is pulled HI, reverse biasing U831C. Bias current for Q831 now flows through R834 and R835, turning it on. The voltage at the emitter of Q831 rises to a level of +2.4 volts, determined by the voltage regulator composed of U731, U831A, U831B, Q831, and associated components. This regulated level is divided down to +400 mV p-p, by the resistive divider formed by R832 and R831, and applied to the front-panel CALIBRATOR loop at an effective output impedance of 50 ohms.

CCD OUTPUT

The CCD Output circuits (diagram 14) convert the two differential output signals from each CCD into single-ended signals for subsequent A/D conversion. The single-ended analog voltages are applied to Track-and-Hold circuits where they are held until the time-multiplexed A/D Converter digitizes the stored samples.

Single-Ending Amplifiers

There are four identical Single-Ending Amplifiers used to convert the four differential CCD array outputs to single-ended signals for A/D conversion. Operation of the Channel 1—Side 1 Single-Ending Amplifier is described.

Side 1 signal outputs from U450 are applied through R876A and R876B to the bases of U775A and U775B. Transistors U775A and U775B form a differential transconductance amplifier that provides high-impedance loading of the CCD array outputs. The collectors of the two transistors are connected to operational amplifier U770A which is configured as a differential-input, single-ended output transresistance amplifier. The connection of R771 to the +7.5 V supply causes the output of U770A to be level shifted to +7.5 V. The resulting output at pin 1 of U770A is a level-shifted, attenuated, single-ended replica of the differential CCD array output signal with most common-mode interference removed.

Track-and-Hold Amplifiers and Multiplexers

The Track-and-Hold Amplifiers and Multiplexers allow a single A/D Converter to digitize all the analog samples from both CCD arrays by time-multiplexing the output samples to the single converter. The four Track-and-Hold circuits are identical; and, for brevity, only the CH 1—Side 1 circuitry will be described.

The output from U770A is applied directly to sampling switch U560A, an enhancement-mode MOS-FET device. The switch gate is controlled via Q660 by the $\overline{\text{OSAM1}}$ (Output Sample from Channel 1) logic signal, and is closed when the data being shifted out of the CCD is stable. When $\overline{\text{OSAM1}}$ is LO, the switch is on, and hold capacitor C561 charges to the signal level of U770A. When $\overline{\text{OSAM1}}$ is HI, the switch is off, and C561 holds its voltage level. Figure 3-3 (shown previously in the "System Clocks" description) shows the timing of $\overline{\text{OSAM1}}$ and $\overline{\text{OSAM2}}$ during the Slow-Out and Short-Pipe modes of CCD operation. During Fast-In mode, $\overline{\text{OSAM1}}$ and $\overline{\text{OSAM2}}$ are both held LO.

The level stored on Hold capacitor C561 is buffered by operational amplifier U770B. The operational amplifier, along with Q771, converts the applied input sample voltage to output current.

Selection of the CH 1—Side 1 current signal to be digitized by the A/D Converter is controlled by the $\overline{\text{DS11}}$ (Data Select-Channel 1—Side 1) line. As shown in Figure 3-3, only one of the four DS signals will be LO at any time. A LO $\overline{\text{DS11}}$ signal applied to the base of Q770 will turn that transistor off. The other transistor of CH 1 (Q870) and both of the CH 2 transistors (Q780 and Q880) are on to shunt their associated signal currents to ground. Each of the four shunting transistors will be turned off in sequence to allow its associated signal current to pass to the CCD DATA node via a series common-base transistor (Q772 for Channel 1—Side 1). The resulting CCD DATA signal is a time-multiplexed combination of all four CCD output channels (two from CH 1 and two from CH 2).

Precise current matching of the Side 1 and Side 3 signal offsets is achieved by setting the DAC-generated CENTER 1 voltage at the time of calibration. Similar offset matching for CH 2 is done with the CENTER 2 signal.

Secondary Supplies

The Secondary Supplies circuit, composed of U861A, U861B, U861C, U861D, and associated components, provides operating voltages used by the CCD Output circuitry. The voltage level of the A2D REF (−0.5 V analog-to-digital reference) is determined by the current through R861 from operational amplifier U861C and is set by the resistive divider string formed by R762, R763, and R764 from the +10 V_{REF} supply. The other voltage outputs (+7.5 V and +9 V_{RA} and +9 V_{RB}) are set by the various taps on the resistive voltage divider and buffered by operational amplifiers.

A/D CONVERTER AND ACQUISITION LATCHES

The A/D Converter and Acquisition Latches (diagram 15) circuit consists of eight-bit A/D Converter U560, eight-bit Min-Max Comparator U740 and U732 (for ENVELOPE acquisitions), Acquisition Latches U631, U632, U630, and U640, and latch switching circuitry to direct and latch the acquired data point values.

A/D Converter

A/D Converter U560 is an 8-bit flash converter that digitizes the analog samples from the CCD arrays at an overall conversion rate of 2 MHz. (See the partial diagram 15 in the Diagrams section for instruments with serial numbers below B011146.)

The A2D REF voltage (−0.5 volt) is amplified and inverted by U880 to produce the 2 V reference voltage used by the A/D Converter. Noise and ripple are filtered from the amplified reference voltage by L770, C560, and C776. The negative side of the reference is tied to ground; therefore, input voltages for conversion may range from 0 V to +2 V. The time-multiplexed CCD Data signal current develops a voltage across R880 that is offset by the A2D REF and then amplified and inverted by U780 to produce an input signal to the A/D Converter within the 0 V to +2 V range needed. The amplified signal is applied to the analog input of U560 after being filtered by L780 and C770.

The input sample is converted on the falling edge of $D_2$4XPC, a 2 MHz clock signal. A valid data byte representing the analog input voltage appears on the A/D Converter output approximately 20 ns later. That data byte is applied to the 8-bit Magnitude Comparator formed by U740 and U732, with the four LSB going to U740 and the four MSB of the byte going to U732.

Envelope Min-Max Comparator

For ENVELOPE Mode acquisitions, glitch-catching at the slow SEC/DIV settings is done by the Envelope Min-Max Comparator circuit formed by four-bit comparators U740 and U732. At SEC/DIV settings slower than 50 μs, analog Peak Detectors U440 and U340 provide more samples than needed to fill the required 50 data points (25 min-max pairs) per division, so not all are saved. During each envelope sampling interval (1/50 of the SEC/DIV setting at 50 μs and slower), the Min-Max Comparator compares every Peak Detector min/max value from A/D Converter U560 to the last-latched maximum or minimum byte to determine which sample will be saved. If the new byte value is greater than the latched byte value, the MAX output of Comparator U732 (pin 5) will go HI; if less than the latched value, MIN at pin 7 will go HI. If the A/D output value is equal to the latched value, both connected outputs of Magnitude Comparator U732 will remain LO. The final min byte and max byte obtained from each channel during an envelope sampling interval are saved to the Acquisition Memory as part of the envelope waveform record.

Since the input to the A/D Converter is time multiplexed between CH1 maximum, CH2 maximum, CH1 minimum, and CH2 minimum values from the Peak Detectors, the latched data applied to the Magnitude Comparator from the Max/Min Latches must also be time multiplexed to maintain the correct relationship for making the comparisons (CH1 maximum against CH1 maximum, CH1 minimum against CH1 minimum, etc.). The necessary time multiplexing is done by the Envelope Latching Logic circuitry.

Acquisition Latch Switching

NORMAL MODE ACQUISITIONS. In non-envelope mode, the LOAD LATCHES signal from the Time Base Controller remains in its HI state. With LOAD LATCHES HI at one of the inputs of OR-gates U512A and U512B, the MIN and MAX signals from the Envelope Min-Max Comparators are ignored, and the outputs from the gates are held HI. This causes each sample from the A/D Converter to be clocked directly through the Acquisition Latches.

Output enabling of the four Acquisition Latches is controlled by the DS11, DS13, DS21, and DS23 data select lines, which also control the multiplexing of the CCD analog samples to A/D Converter U560. The states of these select lines, only one of which may be HI at a time, are latched into the four flip-flops of U520 and U521 by the 20 MHz system clock (C20M1). The $\overline{Q}$ outputs of the flip-flops control output enabling of the four Acquisition Latches. One at a time, their outputs are enabled to apply the acquired data point to the output bus for transfer to the Acquisition Memory input buffer (U613, diagram 8). Two hundred and fifty nanoseconds after one of the Acquisition Latches has been enabled, the rising edge of the $\overline{4XPC}$ signal clocks the HI state present on the D inputs of the flip-flops of U510 and U511 to the Q output of the enabled flip-flop. That rising edge then clocks the data byte from the A/D Converter through the enabled Acquisition Latch to the input buffer of the Acquisition Memory.

ENVELOPE MODE ACQUISITIONS. In ENVELOPE MODE, the LOAD LATCHES signal input to U512A and U512B (from the Time Base Controller, diagram 8) forces each clock flip-flop in turn to clock the A/D Converter output data byte into its associated latch by holding their D inputs HI during the first four data point conversions in each envelope sampling interval. These first four samples (one byte in each Acquisition Latch) initialize the min/max data in the latches for comparison to the remaining data samples that occur in the envelope sampling interval.

The Acquisition Latch Switching circuitry multiplexes the latched CH 1 and CH 2 maximum and minimum data bytes to the inputs of the Envelope Min-Max Comparator so that each digitized sample from the A/D Converter is compared to the correct previous sample (CH 1 Min to the previous CH 1 Min, etc.). It also provides the proper enabling and clocking to direct a new maximum or minimum data bytes into the correct Acquisition Latch.

As in NORMAL Mode acquisitions, output enabling of the four latches is controlled by the DS11, DS13, DS21, and DS23 data select lines. The $\overline{Q}$ outputs of the flip-flops control output enabling of the four latches, causing the Acquisition Latch corresponding with the selected CCD output (CH 1 or CH 2, maximum or minimum) to apply the previously latched data byte to the inputs of the Envelope Min-Max Comparator. A/D Converter output data is thus always being compared to the proper maximum or minimum data value.

When the Envelope Min-Max Comparator detects that the A/D Converter output byte value is either above or below the latched byte value, the MAX or MIN output of U732 will go HI respectively. The HI is passed through U512A (MIN) or U512B (MAX) to the D inputs of flip-flops U510 and U511. Since the A/D Converter output byte value could represent any of the four CCD array channels, the data select lines that determine what sample is currently being output from the CCD arrays are applied to the reset inputs of U510 (A and B) and U511 (A and B). Only that clocking flip-flop corresponding to the selected data sample is enabled by a HI data select line; all others remain in the RESET state.

When the $\overline{4XPC}$ (2 MHz) clock occurs, the enabled clocking flip-flop transfers the level at its D input to its Q output. If that level is a HI (a new max has been found), the current A/D Converter output data byte (the new max) will be latched into the associated Max Latch (either U632 or U631, depending on whether it is CH 1 or CH 2 data), where it then becomes the new comparison level. MIN clocks are produced by U510B and U511A in a similar fashion, latching the new MIN values into either U640 or U630.

Acquisition Latches

During Envelope Mode, the Acquisition Latches perform as Min-Max latches (U631 and U632 Max; U630 and U640 Min) to hold the maximum and minimum data point values being compared during the sampling interval. These values are compared to each newly converted waveform sample to determine when new maximums or minimums occur. Output enabling and data latching are controlled by the Acquisition Latch Switching as previously described.

DISPLAY AND ATTRIBUTES MEMORY

The Display and Attributes Memory (diagram 16) is where the Waveform Processor stores waveform and readout data that is to be displayed on the crt. Digital-to-Analog converters (DAC), under control of the Display Control circuits, convert this stored data to the vertical- and horizontal-deflection signal currents that drive the Display Output amplifiers.

Vertical Display RAM

Vertical Display RAM U431 stores the vertical-deflection data for four 512-point waveforms. Data points to be displayed are written from the Save Memory into the RAM by the Waveform μP (diagram 2) on the WD bus (waveform data bus) via bus transceiver U322. The stored waveform display bytes are read sequentially out of the Vertical Display RAM in blocks under control of the Display Counter (diagram 17) and applied to Vertical DAC U142 to produce the analog vertical deflection signal of the displayed waveform.

To write data into the Vertical Display RAM, the Waveform μP puts the data byte to be written onto its WD bus and sets its $\overline{\text{WRD}}$ (waveform read) bit HI. This HI enables bus transceiver U322, and the vertical data is applied to I/O (in/out) pins of the RAM. At the same time, the $\overline{\text{DISP}}$ signal is address decoded LO (from decoder U570, diagram 2) for addresses between 8K and 12K, and the WAB address bit applied to U323B selects the Vertical RAM U431 via U421A. When the Waveform μP generates its write pulse ($\overline{\text{WWR}}$), it is transmitted through U422A and U422D, writing data into the Vertical Display RAM. This process occurs for each data byte (point) of waveform information.

To display the stored data points, the System μP loads the starting address of the data block to be displayed into the Display Counter and selects the Display Counter to address the Vertical Display RAM (via the Address Multiplexer). The System μP also sets the $\overline{\text{YON}}$ (vertical display on) bit applied to U421A and U421B LO, selecting the Vertical Display RAM and enabling its outputs. As the Display Counter increments, the selected block of data is sequentially clocked out onto the DY bus (vertical-display data bus) and applied to Vertical DAC U142 to produce the vertical deflection signal current to the Vertical Output Amplifiers.

If the Waveform μP needs to read data from the Vertical Display RAM, it outputs an address within 8K to 10K address space of the RAM. This address block is decoded by U323B to enable both the Vertical Display RAM (via U421A) and bus transceiver U322. Since the Waveform μP is trying to read data, its $\overline{\text{WRD}}$ (waveform processor read) line will be set LO. This enables the RAM outputs via U323C and U421B and causes buffer U322 to direct the data onto the Waveform μP data bus.

Horizontal Display RAM

Operation of Horizontal Display RAM U440 is identical to that of the Vertical Display RAM just described. The Horizontal RAM chip select ($\overline{\text{CSX}}$) is gated through U323D for addresses between 10K and 12K when $\overline{\text{DISP}}$ is LO. Data that may be stored in the Horizontal Display RAM includes two 512-point waveforms and 1K $\times$ 8 of readout information. During a waveform display, the data output from the Horizontal RAM may be routed to either the Vertical DAC or Horizontal DAC, providing for either two more YT displays or two XY displays.

Attributes RAM

Attributes RAM U430 contains 4K $\times$ 1 points of data that tell the Z-Axis system (using the BRIGHTZ signal) whether or not a data point read from either the Vertical Display RAM or the Horizontal Display RAM should be intensified. Operation of the RAM is similar to that just described for the Vertical and Horizontal RAMs except that the data path is only one bit wide.

The write enable of the Attribute RAM ($\overline{\text{WRA}}$) is gated by U422C between 12K and 14K when $\overline{\text{DATT}}$ is LO from decoder U570 (diagram 17). $\overline{\text{WRA}}$ going LO enables the data from bit WD7 of the data bus to be written to the addressed location. Gate U422A prevents the $\overline{\text{WWR}}$ clock from being gated to U422C if the Display Counter is selected (Waveform μP not in control of the address bus).

To read attribute data out of the RAM, the Waveform μP sets $\overline{\text{WRD}}$ LO. This LO, along with the address-decoded $\overline{\text{DATT}}$ (attribute data) line, enables buffer U423A and places the addressed output bit from the D0 output of U430 onto bit WD7 of the data bus.

When displaying data from either (or both) the Vertical RAM or Horizontal RAM (the addresses applied to all three RAM chips are the same), the attribute data for each data point will be applied to the Z-Axis circuit to determine the intensity of each point. A HI bit from the D0 output of U430 will intensify the displayed point.

Horizontal Data Buffers

The Horizontal Data Buffers, U320 and U321, are used to route the data from the Horizontal RAM to either the Horizontal DAC or the Vertical DAC, depending on the type of display being produced.

For normal waveform displays, vertical deflection data may come from either the Vertical or the Horizontal Display RAM. To route data from the Horizontal RAM to the Vertical DAC, the outputs of the Vertical RAM will be disabled ($\overline{\text{OEY}}$), the outputs of the Horizontal RAM will be enabled ($\overline{\text{OEX}}$ goes LO), and buffer U320 will be enabled ($\overline{\text{XTOVERT}}$ goes LO). These three signals are all controlled by the System μP by writing bits XON and XTOVERT HI into Mode Control Register U541 (diagram 17) and writing a LO to the YON output of the register. Now, data addressed in the Horizontal RAM is applied to the Vertical DAC to produce vertical waveform deflections.

For XY displays, Mode-Control bits XON, YON, and XY are set HI while XTOVERT is set LO. This applies addressed data from the Vertical RAM to the Vertical DAC and applies the addressed data from the Horizontal RAM to the Horizontal DAC via now-enabled buffer U321. A waveform versus waveform (XY) display results.

During readout displays, both U320 and U321 will be disabled, along with the Vertical RAM. Since the readout character-code data is stored in the Horizontal RAM, it will be enabled. Character-code data from the Horizontal RAM is output to the Readout State Machine, where it is converted to the appropriate horizontal- and vertical-deflection codes.

Readout Buffers

Readout buffers U240 and U140 direct the ten least significant bits (LSB) from the Display Counter to the Horizontal DAC and the Vertical DAC during readout displays. **The buffers are enabled by a LO $\overline{\mathrm{RO}}$ signal at their enable inputs.**

Four of these bits, Q6-Q9, are applied to the four most significant bits (MSB) of the Vertical DAC input through U140A and are used to select one of the 16 available readout lines for the selected character to be displayed on.

The six LSBs are applied to the six MSBs of the Horizontal DAC and are used to select one of the 64 possible character positions on the selected readout line. Since a maximum of only 40 characters will actually be displayed on any given line, the gain of the Horizontal Output Amplifier increases when readout is being displayed. The center 40 character positions then fill the display horizontally. This action is more fully explained in the Horizontal Output Amplifier description.

Ramp Buffers

Ramp Buffers U130 and U140 apply the ten LSBs of the Display Counter address (via Address Multiplexer U210, U212, and U221 on diagram 17) to the Horizontal DAC during YT waveform (non-XY) displays. Since the Display Counter address is merely incrementing for waveform displays, a horizontal ramp results at the Horizontal DAC outputs. Each sequentially acquired data point is thus displayed at its corresponding horizontal (time-dependent) address on the crt. The buffers are enabled by the $\overline{\mathrm{COUNTEN}}$ (counter enable) bit from the Mode-Control Register.

Volts Cursor Register

Volts Cursor Register U241 is an address-decoded memory location where the System μP writes the eight MSBs of the vertical-position data for volts-cursor displays. Data written into this register, along with two bits written into the Misc Register U540, define the vertical position of the Volts cursor. Since volts-cursor displays have two cursors, the microprocessor alternately writes the position data for each cursor into the registers just before it is displayed. Data is written into the register on the rising edge of the address-decoded $\overline{\mathrm{VCURS}}$ clock pulse.

Volts-cursor displays are a special type of "waveform" display wherein the vertical deflection data from the Vertical Display RAM is disabled (by turning off the RAM chip select), and the data bits in Volts Cursor Register U241 (and the DY0-DY1 bits from the Misc Register U540, diagram 17) are applied to Vertical DAC U142 instead. Cursor display is automatically selected by the Z-Axis logic when neither WFM nor $\overline{\mathrm{RO}}$ are asserted (not a waveform display and not a readout display). To start the display, the System μP asserts the START bit in the Display Control Register as it would for a waveform display, starting the Display State Machine. The result is a horizontal line displayed on the screen at the level set by the data from the Volts Cursor Register. When displaying cursors on a waveform, the two LSBs from the Misc Register are set to 0, decreasing the resolution from 1024 levels to 256 levels.

Time Cursor Register

Time Cursor Register U441 provides a function similar to the Volts Cursor Register. Time-cursor data is written to the register from the system processor on the rising edge of the address-decoded $\overline{\mathrm{TCURS}}$ clock (time-cursor clock). This data is applied to Horizontal DAC U250 (along with the DX0-DX1 bits from the Misc Register) to define the horizontal position of the cursor. A software ramp previously written into Vertical RAM U431 is applied to Vertical DAC U142 as the Display State Machine runs (started in the same way as the volts-cursor display).

For "directed-beam" cursors, such as the "+" made up of individual microprocessor-directed points displayed on screen, both cursor registers are enabled after the System μP writes one dot of XY position data into the registers. To display the addressed point, the processor sets the HZON (host z-axis on) bit in the Misc Register LO, then HI. The processor then calculates the next point of the "+", writes the position data to the cursor registers, enables the registers, and sets $\overline{\mathrm{HZON}}$ LO to display that point. This cycle continues until the entire "+" is drawn.

Vertical DAC

Vertical DAC U142 generates complementary vertical-deflection currents used to drive the vertical deflection system from the digital data applied to its inputs. The data that appears at the DAC inputs is selected by the microprocessor via the Mode-Control Register and determines what type of display will be generated. The exclusive-OR gate U350A inverts bit DY9 during "non-readout" displays to create "bipolar" data relative to the vertical (graticule) center of the crt.

Horizontal DAC

Operation of Horizontal DAC U250 is identical to that of the Vertical DAC and produces the horizontal-deflection signal currents that drive the Horizontal Output Amplifier.

Diagnostic Buffers

The Diagnostic Buffers, U141 (vertical) and U243 (horizontal), allow the System μP to monitor the data being applied to the Vertical DAC and Horizontal DAC respectively. By forcing known data patterns through the various data paths and observing the data arriving at the DAC inputs, the diagnostic routines can verify functionality of much of the display system hardware. The buffers are enabled during diagnostics via the address-decoded Register Select logic.

DISPLAY CONTROL

The Display Control System (diagram 17) produces the crt waveform and readout displays from data stored in the Display RAM. The data, originally stored by the Waveform μP or the System μP, is read out of the RAM and is used to produce the individual dots that make up both waveform and readout displays. The Display System has two "state machines" for converting the stored data into the horizontal and vertical deflections that produce the waveform dots and readout characters.

For YT waveform displays, the Display State Machine generates 512 linearly spaced points across the face of the crt (horizontally). Each of these points may be displayed at any of 256 vertical positions on the crt. For XY displays, each of the 512 points that make up a waveform may be placed anywhere on the screen in a 256 × 256 matrix.

For readout displays, the face of the crt is vertically divided into 16 character lines each having 40 horizontal character positions on the line. Each of these character positions corresponds to a specific location in the readout memory space (stored in the Horizontal RAM). To display the readout, the Readout State Machine sequentially reads through the readout memory and displays the required character at the corresponding (memory-mapped) location on the crt screen. Each displayed character consists of a sequence of individual dots produced by the Readout State Machine.

Each of these display types is controlled and initiated by the System μP. The acquired waveform data points are written into the Display RAMs by the Waveform μP and the readout data is written in by the System μP. Display of this stored data is controlled by the System μP through data latched into the several display registers. The data written to the registers determines what type of display should be produced, how long (number of data points) it should be, and when it should start.

Register Select

The Register Select stage, composed of U550 and U450D (along with the System μP address decoding), address decodes the three LSBs of the System μP address bus to enable any of eight display "registers" for a read or write. These registers control such things as display mode (how the stored data is displayed, either XY or YT), which waveforms are displayed, and whether or not cursors and readout are to be displayed.

The enable inputs for U550 are controlled by the System μP. The $\overline{\text{DISPSEL}}$ (display select) is an address-decoded signal produced on the Processor board when any of the display memory addresses are output by the System μP. Negative OR gate U450D provides an enable to U550 whenever the System μP is trying to read or write. Address bit A3 provides the final enable when it is HI.

Once enabled, the three lowest address bits are used to select one of the eight outputs from U550. These outputs, when LO, enable or load one of the eight display registers. Enabling of these individual registers is explained in more detail in the specific register descriptions.

Mode Control Register

Mode Control Register U541 and associated gating circuits composed of U340, U442, U423B, and U350C, control the operating modes of the various display state machines.

Data from the processor data bus is written into data latch U541 when the $\overline{\text{MODECON}}$ (mode control) bit from U550 returns HI (after the PWRUP reset goes HI). These latched bits are used as enables to other portions of the display circuitry and control the overall function of the display.

NAND gates U340C and U340D do not allow the $\overline{\text{YON}}$ and $\overline{\text{XON}}$ enables (controlling the vertical and horizontal RAMs respectively) unless the display counter is running (PRESTART + DISPLAY is HI). Exclusive-OR gate U350C and tristate buffer U423B are used to enable horizontal-deflection bit DX1 only when the time cursor is being displayed (both RO and COUNTEN are LO). The remaining bits from the mode-control register are NANDed with the $\overline{\text{DISP}}$ (display running) signal and only affect their associated functions while the Display State Machine is running.

Buffer U542 provides a way for the System μP to read back the data written to the Mode Control Register U541.

Display Control Register

The operation of Display Control Register U530 is similar to that just described for the Mode Control Register. When enabled (by $\overline{\text{DISCON}}$), data from the data bus is written into U530 on the rising edge of the System μP $\overline{\text{WR}}$ (write) clock. These data bits determine how many data points are displayed, whether the display is to be read from memory in envelope mode (ENV), and whether the intensity of each dot should be bright or dim (DOTS).

The buffer U531 provides a way for the System μP to read back the contents of the Display Control Register.

Miscellaneous Register

Operation of the Miscellaneous Register is identical to that of the Display Control Register just described. The output bits control miscellaneous circuit functions, as the register name implies. The function of each bit is explained in the description of the associated circuitry.

Buffer U540 allows the System μP to read back the contents of the Miscellaneous Register.

Display Clocks

The state machines of the Display System run on clocks derived from the 5 MHz clock of the Secondary Clock Generator U710 (diagram 7). The Display Clocks circuit provides the signal frequency division and gating logic to properly condition clocks for the Display System circuitry.

The 5 MHz clock signal from the Time Base Controller circuit is buffered and inverted by U413C and is used to drive the Readout State Machine.

The 5 MHz clock is also applied to the counter made up of decade counters U410A and U410B, producing several intermediate clocks at their outputs. The 1 MHz 2QC clock, the 500 kHz 2QA clock, and the 250 kHz clock from U410B are gated together by U411A and produce the $\overline{\text{SAMPLE}}$ clock, having a LO duty cycle of 12.5%.

Buffer U413A inverts the 250 kHz clock used for the Z-Axis and Display State Machines.

Gates U411C, U412C, and U412D make up a clock-steering circuit that selects the source for clocks to the counters, depending on display mode. When displaying waveforms, readout, or cursors, the DISPLAY bit applied to U411C is HI. The RO and $\overline{\text{RO}}$ signals, applied to U412C and U412D respectively, do clock selection depending on whether readout or waveform data is to be displayed.

For waveform displays, RO applied to U412C is LO, holding its output to U411C HI. This HI, along with the HI DISPLAY bit, enables U411C, and the output of U411C follows the 250 kHz signal applied to U412D (since $\overline{\text{RO}}$ is HI). For readout displays, RO and $\overline{\text{RO}}$ are HI and LO respectively. This holds the output of U412D HI, and the output of U411C follows the $\overline{\text{CLKRAM}}$ (clock RAM) signal from the Readout State Machine. To completely disable the Counter clocks, the Display State Machine sets the DISPLAY bit applied to U411C LO.

Display Counter

The Display Counter stage, made up of U211, U220, and U222, generates the sequential addressing that the Display and Readout State Machines use to read the stored waveform and character data out of the display RAM. Depending on the type of information to be read from RAM (waveform or readout), clocks to the counter are selected by logic to produce waveform and readout displays at the proper refresh rates.

To display stored data, the System μP writes the eight MSBs of the 12-bit starting RAM address into U211 and U220 over the data bus by generating a LO $\overline{\text{LDCOUNT}}$ from the Register Select stage. The 4 LSBs of the address (all LO) are also loaded at the same time into U222. The counter then starts counting at the selected rate. When the count in U222 reaches 15, its $\overline{\text{RCO}}$ (ripple-carry output) goes LO for the last half of the clock cycle and enables U220. Due to a two-gate propagation delay through U222 to the $\overline{\text{RCO}}$ output, U220 will still be enabled on the rising edge of the next clock. This clocks U220, which is then disabled until U222 counts another 16 clocks. Counting continues, and eventually the $\overline{\text{RCO}}$ output of U220 enables U211, causing it to increment in a similar fashion. Counting continues until the Display State Machine determines that the desired display is complete, at which time it shuts off clocks to the counter.

The outputs of the counters change synchronously and are applied to the Multiplexer stage, which selects between these counter outputs and the microprocessor address bus for Display RAM addresses. The MAX output from U222 (occurring on count 15) is used in the Readout State Machine.

Address Multiplexer

The Address Multiplexer stage, under control of the Display State Machine, selects the address source for the various display RAMs from either the Waveform μP address bus or the Display Counter.

When the Waveform μP is writing acquired data into the display RAMs (Horizontal or Vertical), the Display State Machine selects the Waveform μP address bus (WA0-WAB) as the source for RAM addresses by setting the COUNTSEL (counter select) line LO. When displaying the stored data, COUNTSEL is HI, and the outputs from the Display Counter are routed to the various RAM address lines.

Exclusive-OR gate U350B is used to invert counter bit DC0 when displaying envelope data (ENV is HI). This causes data pairs (max-min) to be read out in reverse (relative to how they were stored) and produces an envelope display that always starts with a MIN point.

Display State Machine

The Display State Machine determines when display of stored data should start and stop, depending on other conditions in the Display System.

To start a display, the System μP writes a HI for the START bit into Display Control Register U530. This HI is applied to the D input of flip-flop U415A and clocked to its Q output on the falling edge of the 250 kHz clock (rising edge of the $\overline{\text{250 kHz}}$ clock). This latched STARTDIS bit (HI) is then applied to the D input of U414A and to pin 9 of U313. Since the Display Counter has not reached its final value (this is the starting point), the output level of the three lower AND gates within U313 are LO, thereby enabling the output AND gate (it has inverting inputs). With the previous display cycle finished (as it is for this discussion), the DISDN (display done) bit applied to pin 10 of U313 is also HI. The 250 kHz clock applied to this enabled AND gate causes the output of U313 to go HI on the falling edge to clock the HI STARTDIS bit to the Q output of U414A. This latched signal is the DISPLAY bit that enables the Display Counter clocks (via U411C).

The DISPLAY bit is delayed slightly by the propagation delays of the START bit through the flip-flops and gates. Therefore, the PRESTART bit is written HI to cause the output of U323A to be HI until the DISPLAY bit is latched into flip-flop U414A. The HI PRESTART + DISPLAY bit from U323A selects the counter outputs to address the Display RAMs (via the Address Multiplexer stage). After the DISPLAY bit is latched into U414A, the System μP sets the START and PRESTART bits from the Display Control Register LO. The LO START bit is clocked to the Q output of U415A, disabling the 250 kHz clocks through U313 to U414A, and the LO PRESTART bit allows the DISPLAY signal to control OR-gate U323A.

With the DISPLAY bit to U411C set HI, clocks from either U412C or U412D clock the Display Counter. Which one does the clocking depends on whether the data to be displayed is readout or waveform information. If readout information is being displayed, the $\overline{\text{RO}}$ bit (from the Mode Control Register) applied to U412D will be LO, disabling the 250 kHz clock (output of U412D is held HI). At the same time, R/O applied to U412C is HI, enabling the $\overline{\text{CLKRAM}}$ (clock RAM) signal from the Readout State Machine to clock the address counters.

If waveform data is to be displayed, $\overline{\text{RO}}$ from the Mode Control Register is HI and RO is LO. The LO RO level applied to U412C closes the $\overline{\text{CLKRAM}}$ path (output of U412C is held HI) while the HI $\overline{\text{RO}}$ level applied to U412D opens the 250 kHz clock path through U412D and U411C.

The two display-control bits, STOP512 and STOP1024, applied to U313 determine how many data bytes are read from the selected display RAM (Horizontal, Vertical, and Attribute) before stopping the current display cycle. Only one of these two bits is HI at any time. The outputs of the unselected AND gates within U313 are LO, and along with the LO caused by the LO STARTDIS bit, enable the output gate of U313. The selected AND gate watches its appropriate counter bit and, on the falling edge of the bit, causes a clock at the output of U313. This clocks the now LO STARTDIS bit to the Q output of U414A, disabling U411C (and thus clocks to the Display Counter), and resets the DISDN at the $\overline{\text{Q}}$ output HI in preparation for the next display cycle.

The DISDN signal is also sent to the System μP Interrupt Logic to tell it when the currently assigned display task is complete. When the processor detects the HI DISDN, it writes data out to the display register to start the next display cycle. The System μP, knowing how much waveform and readout data needs to be displayed, does the writing at a rate that keeps the overall display-refresh rate constant.

Displaying a single waveform requires 512 data points be read from RAM, so STOP512 is set HI. A two-waveform display or a single-waveform envelope display will require STOP1024 to be HI. Readout displays may also consist of up to 16 lines of readout, in which case STOP1024 would be set. This is further explained in the Readout State Machine description.

The $\overline{\text{STOPDIS}}$ bit applied to the reset inputs of U414A and U415A provides the System μP with a way to stop any display in process.

Z-Axis Logic

The Z-Axis Logic determines when to turn the display beam on or off for each of the various display modes. These displays are readout, waveform, cursor-normal, cursor-dashed, and diagnostic (host-forced) Z-Axis on.

To enable readout or waveform displays, the Display State Machine sets its DISPLAY output HI. This enables U415B, U414B, and U312C.

During readout displays, the $\overline{\text{RZON}}$ (readout Z-Axis on) signal from the Readout State Machine is LO for each point that should be turned on and HI when the display should be blanked. The level of this signal is sampled by U415B at a 5 MHz rate. The Q output of U415B controls the Z-Axis through U450B and U223C, and since it is synchronized to the 5 MHz clock used to clock the Readout State Machine, the intensity of each dot is not the same.

For waveform displays, the DOTS bit from Display Control Register U530 will be set HI by the System μP. This HI, along with the HI DISPLAY signal from the Display State Machine, enables U312C. As long as a waveform display is taking place, the 250 kHz clock turns the display dots on and off with a 50% duty cycle via U312C and U223C. When the Display State Machine determines that the waveform display is over, it sets its DISPLAY bit LO, disabling U312C. For nonwaveform displays, the DOTS bit is LO, also disabling U312C.

For cursor displays, the HI DISPLAY signal enables D flip-flop U414B, and the $\overline{\text{250 kHz}}$ clock begins clocking the data from the output of U312B to the Q output of U414B. Since a cursor display is neither a waveform nor a readout display, the DOTS signal applied to inverter U413D is LO while the $\overline{\text{RO}}$ signal applied to NAND-gate U312B is HI. This enables U312B, and the output of U412A then controls the D input signal to flip-flop U414B. That signal is clocked to the Q output and applied to U223C to control the Z-Axis signal $\overline{\text{ZON}}$.

When displaying the inactive cursor (the one not selected for control by the cursor pot), the ACTIVELC (active line cursor) bit from the Misc Register to pin 2 of U412A is set LO. This causes the output of U412A to be HI, and the Z-Axis remains on as long as that particular cursor is being displayed.

When the other (active) cursor is to be displayed, the System μP sets the ACTIVELC bit HI. The output of U412A is then dependent on the DC3 signal from the Display Counter. The DC3 signal has a 50% duty cycle and changes states every eight characters (for cursors, the character is a single dot), so the resultant cursor display appears as a dashed line.

The $\overline{\text{HZON}}$ (host Z-Axis on) bit applied to U450B from the Misc Register (U540) allows the System μP to turn the Z-Axis on during diagnostics and allows verification of Z-Axis functionality. When set LO, $\overline{\text{HZON}}$ produces a LO at the output of U450B output, and thus at the $\overline{\text{ZON}}$ (Z-Axis on) output of U223C. This keeps the Z-Axis turned on until the $\overline{\text{HZON}}$ bit is reset HI by the processor.

Readout State Machine

The Readout State Machine produces the alphanumeric readout on the crt from character-code data stored in the Horizontal RAM. For readout displays, the face of the crt is vertically divided into 16 character lines each having 40 horizontal character positions on the line. Each of these character positions corresponds to a specific location in the readout memory space (stored in the Horizontal RAM). To display the readout, the Readout State Machine sequentially reads through the readout memory and displays the required character at the corresponding (memory-mapped) location on the crt screen. Each displayed character consists of a sequence of individual dots produced by the Readout State Machine.

Since the position of the character on the screen is related directly to the RAM location, the LSBs of the Display Counter are used to position the character on the crt screen. The six LSBs of the counter are applied to the Horizontal DAC and select 1-of-64 character locations on a line (only the center 40 are displayed) and the next four LSBs are applied to the Vertical DAC to select 1-of-16 display lines.

Once this rough positioning is done, the Readout State Machine displays a sequence of dots that make up the addressed character, each dot being positioned relative to the rough display position.

Character codes, sequentially read from the Horizontal RAM, are applied to seven address lines of a character ROM (U420). These select the block of dot-position data within the ROM corresponding to that character code. Five more address bits are generated by an incrementing Dot Counter (U416B and U416A) and sequentially clock the XY dot-position data from the selected ROM block. The horizontal and vertical dot-position data is applied to the Horizontal and Vertical DACs and is used to deflect the crt beam relative to the selected on-screen character position.

The operation of the Readout State Machine is ROM based; it proceeds through a sequence of states based on data loaded from a ROM.

Initially, when power is first applied, both the PWRUP (power up) and DISPLAY signals applied to U450A are LO. These states cause a LO at the reset input of presettable counter U231 that resets its output count to zero. The reset state will remain until the instrument power comes up (PWRUP goes HI) and the system processor determines that a display should be produced (it starts the Display State Machine and DISPLAY goes HI).

With the reset removed, presettable counter U231 is enabled to either count (up) or do a parallel load from the four MSBs output from the addressed location within U232 on the next rising edge of the $\overline{\text{5 MHz}}$ clock. The COUNT/$\overline{\text{LOAD}}$ select line from the data selector U230 determines whether counting or loading will occur.

The LOAD/$\overline{\text{DECIDE}}$ bit output from the addressed ROM location within U232 is applied to the enable input of U230 and determines whether the COUNT/$\overline{\text{LOAD}}$ line is forced LO (U230 disabled by LOAD/$\overline{\text{DECIDE}}$ being HI) or whether one of the decision inputs is selected (via select inputs A, B and C of U230). When the LOAD/$\overline{\text{DECIDE}}$ bit from U232 is LO, it indicates that the state machine is at a decision point as to whether counter U231 should count or load (instead of just automatically loading the next state). The condition tested to make this decision is selected by the select inputs to U230 and are as follows:

D0—R/O (readout) goes HI when a readout display should start.

D2—AND gate U233A watches for the 12th character address (11).

D3—$\overline{\text{EOCH}}$ (end of character) goes LO on the last character dot and causes the next state to be loaded.

D4—EOL (end of line—X9 bit U440, diagram 16) goes HI when readout line is over.

D5—AND gate U223B watches for the 64th character address (63) to indicate that the next character is the beginning of a new line.

ROM U330, addressed in parallel with U232, outputs three bits unique to the state selected and is used to clock the dot counter (U416B and U416A), clock the Display Counter, and to turn on the Z-Axis for readout dots.

The flow chart in Figure 3-8 illustrates operation of the Readout State Machine.

As the state machine runs, the counter outputs of U231 (the "current-state") are first reset to state "0." The data output from the O4-O7 (outputs 4-7) lines of U232 contain the "next-state" data, O1-O3 (outputs 1-3) hold the select data for the data selector U230, and output O0 (output 0) is the LOAD/$\overline{\text{DECIDE}}$ bit. In addition, the outputs from U330, used to turn on the Z-Axis if appropriate ($\overline{\text{RZON}}$), increment the character ROM dot counter U416B-U416A ($\overline{\text{CKDOTCTC}}$), and clock the Display Counter ($\overline{\text{CLKRAM}}$) to address the next character, are now at their state 0 condition (all HI).

The COUNT/$\overline{\text{LOAD}}$ signal from U232 determines what action counter U231 takes when the next $\overline{\text{5 MHz}}$ clock occurs. If LO, the data from outputs O4-O7 of U232 is loaded to the counter outputs; if HI, the counter increments.

The LOAD/$\overline{\text{DECIDE}}$ line, along with the three channel-select inputs to U230, gives the state machine the ability to determine when certain events have occurred. When the LOAD/$\overline{\text{DECIDE}}$ bit from ROM U232 is HI, indicating that no decisions need be made in the present state, data selector U230 is disabled and the COUNT/$\overline{\text{LOAD}}$ output to U231 are forced LO. On the next $\overline{\text{5 MHz}}$ clock, the "next-state" data from U232 (outputs O4-O7) is merely loaded into counter U231.

If the "present-state" data output from U232 has the LOAD/$\overline{\text{DECIDE}}$ bit set LO, indicating that some circuit condition needs to be tested to determine what to do next,

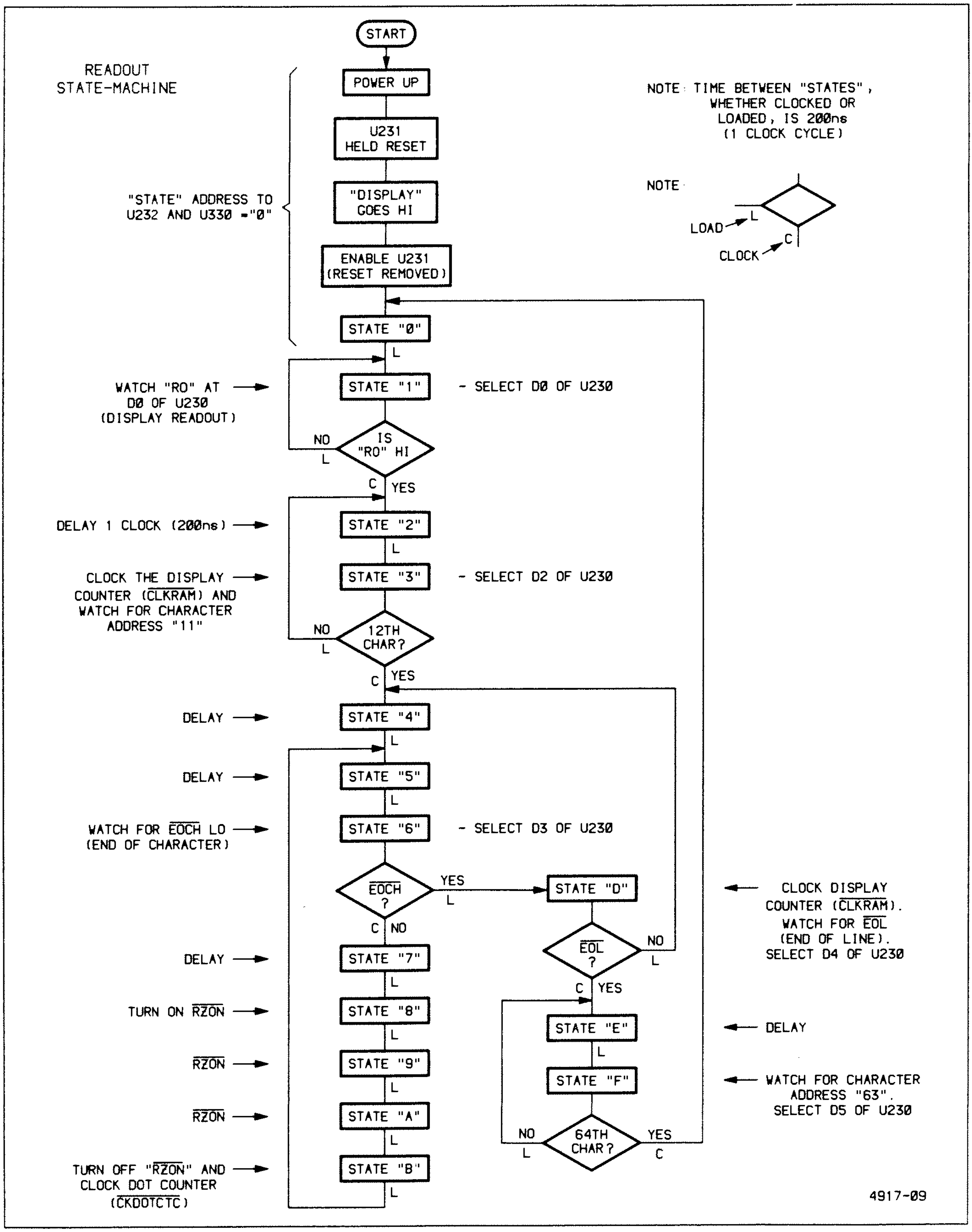

Figure 3-8. Readout State Machine flow chart.

data selector U230 is enabled. The three data bits (O1 through 03) from U232 define which condition needs to be tested and selects one of the D inputs of U230 to route to U231 via the COUNT/$\overline{\text{LOAD}}$ line. Whether or not the condition being tested for is present at the selected D input determines whether counter U231 counts or loads.

To go from state "0" to state "1," data from U232 is loaded into U231.

The state 1 data from U232 has the LOAD/$\overline{\text{DECIDE}}$ signal set LO, and the next three bits select input D0 of U230 to watch. This is the R/O (readout) line, and it is set HI by the System μP when it wants to start a readout display. If R/O is LO (don't start yet), COUNT/$\overline{\text{LOAD}}$ is also LO and the "next-state" data from U232 is loaded into counter U231. For state 1, the next-state data is also 1, so the state machine just cycles in state 1 until R/O goes HI.

When R/O goes HI, the COUNT/$\overline{\text{LOAD}}$ line follows and the next 5 MHz clock increments the counter to state "2." State 2 has the LOAD/$\overline{\text{DECIDE}}$ bit set HI, so the next clock merely loads the next-state data (which happens to be 3) into U231.

State "3" clocks the display RAM (using $\overline{\text{CLKRAM}}$ from U330), enables U230, and selects its D2 input. AND gate U223A, producing the D2 input level, monitors the Display Counter address lines, looking for address 11. Address 11 corresponds to the twelfth character (remember character 0) and the first character displayed on the crt. (See Display Output description for further explanation.) If address 11 has not been encountered yet, the next-state data from U232 will be loaded into U231.

This next-state data is 2. Returning to state 2 resets the $\overline{\text{CLKRAM}}$ bit from U330 HI so the next state 3 will clock the Display Counter again. This loop between states 2 and 3 continues to clock the Display Counter until U223A detects address 11. When this occurs, COUNT/$\overline{\text{LOAD}}$ goes HI and the next 5 MHz clock increments the state to "4."

State "4" resets $\overline{\text{CLKRAM}}$ HI and disables U230. The next clock loads state "5," a 200 ns delay, into U231. The next clock loads state "6."

State "6" data from U232 enables U230 and selects its D3 input. This is the $\overline{\text{EOCH}}$ (end of character) bit from the character ROM U420 and will only be LO for the last dot of any given character. As long as $\overline{\text{EOCH}}$ is HI (not the last dot), U231 will increment to state "7" on the next clock. State 7 disables U230, terminating the test condition.

State "8" is loaded from state 7 and turns on the Z-Axis via $\overline{\text{RZON}}$ (readout Z-Axis on) from U330. States "9" and "A" (hex) are sequentially loaded from the previous state and also have $\overline{\text{RZON}}$ asserted. These three cycles in sequence turn the Z-Axis on for 600 ns for each readout dot to be displayed.

State "B" is loaded from state "A" and does two things. It turns $\overline{\text{RZON}}$ off (HI) and sets $\overline{\text{CKDOTCTC}}$ (clock dot counter) LO, incrementing the dot counter made up of U416B and U416A. This addresses the next byte of XY deflection data within U420 in preparation for the next dot display cycle.

The next 5 MHz clock loads state 5 from state B and resets the $\overline{\text{CKDOTCTC}}$ from U330 HI. State 6 is next loaded from state 5 and is once again checking for $\overline{\text{EOCH}}$ (described earlier).

If $\overline{\text{EOCH}}$ is set LO this time (signaling the last dot), counter U231 will be loaded to state "D" (instead of clocked to state 7 as described earlier). State D clocks the Display Counter via $\overline{\text{CLKRAM}}$, enables U230 and selects its D4 input. This input monitors the EOL signal (X9 bit) from the Horizontal RAM which will be set HI when the last character of a given line of readout information has been displayed. When EOL (end of line) is detected, U231 increments to state "E." If it is not detected, state 4 will be reloaded from state D data and the next character will be displayed as described before.

State "E" resets the $\overline{\text{CLKRAM}}$ signal from U330 and disables U230. The next 5 MHz clock loads state "F" from state E data.

State "F" data clocks the Display Counter via $\overline{\text{CLKRAM}}$, enables U230 and selects its D5 input. AND gate U223B watches for Display Counter address 63; i.e., the 64th character. If the 64th character is not detected, state E is loaded from the state F data, resetting $\overline{\text{CLKRAM}}$ HI in preparation for the next state F and the associated $\overline{\text{CLKRAM}}$ pulse. The looping between states E and F continues to increment the Display Counter until U223B detects address 63 (the 64th character).

The 64th character is significant in that the next character is the start of the next line. When address 63 is detected, U231 is clocked from state F to state 0. The routine is now back to where it started, and the next line may be displayed in a similar manner.

DISPLAY OUTPUT

The Display Output circuits (diagram 18) convert the current outputs from the Horizontal and Vertical digital-to-analog converters (DACs) to the voltage levels used to drive the crt deflection plates. The Display Output circuit includes a vector-generation function that allows the individual dots of a waveform display to be translated into smooth lines connecting the waveform points (vectors on). A Display Mode switching circuit under control of the System μP selects which type of signal is applied to the output amplifiers for the various display types (envelope, dots, vectors, or readout).

Vertical and Horizontal Input Buffers

Operation of the Vertical and Horizontal Input Buffers is identical; so for brevity, only the Vertical Input Buffer circuit operation is described.

The Vertical Input Buffer, JFET operational amplifier U170 and its associated components, translates the complementary output currents from the Vertical DAC (U142, diagram 16) to an output voltage. Complementary, in this case, means that the sum of the currents is a fixed value; if one current increases, the other decreases by the same amount.

Current from the Vertical DAC output connected to pin 3 of U170 develops a voltage across R163. This voltage causes the output of U170 to move in the same direction until the feedback current through R164 applies an equal voltage to pin 2 of U170. The output voltage of the Input Buffer at pin 6 is the (signed) sum of voltages across R163 (+) and R164 (−). The gain of the stage is 1 V per mA (differential).

Vertical and Horizontal Vector Generators

Operation of the Vertical and Horizontal Vector Generators is similar. For brevity, only the Vertical Vector Generator is described in detail, and the differences in the two Vector Generators pointed out. Each Vector Generator consists of a High-Current Difference Amplifier, a Sample-and-Hold circuit, and an Integrator circuit that transforms the step voltages output from the Sample-and-Hold circuit to smooth transitions (vectors). See Figure 3-9 for a simplified diagram.

The step transitions from Vertical Input Buffer U170 are applied to the High-Current Difference Amplifier, made up of U281, Q182, Q181, and associated components, through R172. Initially (before the first integration occurs), input pin 3 of U281 is referenced to ground through R161; deviation from this ground reference seen at the other

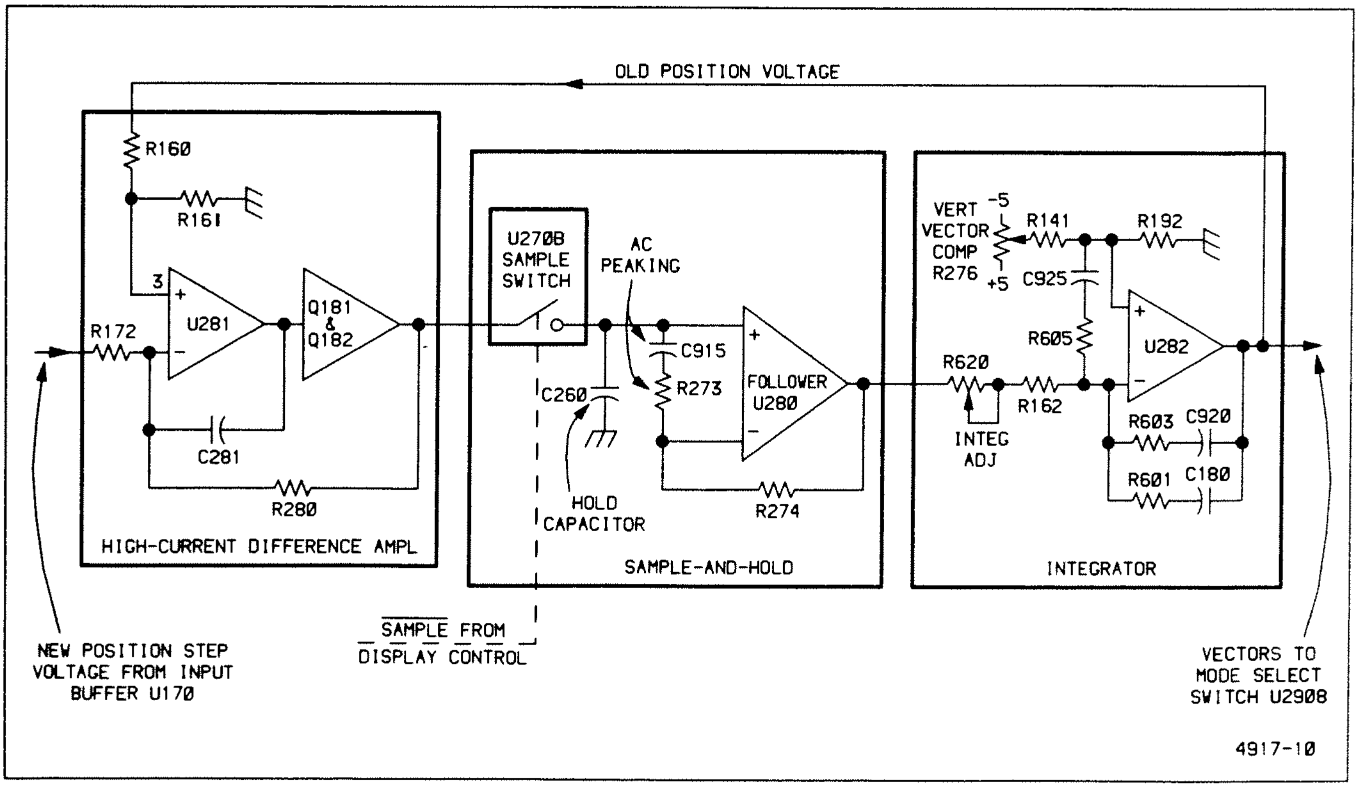

Figure 3-9. Vertical Vector Generator.

input (pin 2) causes the output (pin 6) of U281 to move in the opposite direction. This voltage change is applied to the base of Q181 (via R145) and to the base of Q182 (via series diodes CR193 and CR194 from R145). These transistors are biased in their linear region and act as emitter followers for the signals at their bases. Two series diodes between the bases of the transistors separate the base voltages by 1.2 volts, so the emitters of both transistors are at about the same potential. Negative feedback from the amplifier output (junction of R194-R196) is via R280. The resistance ratio of R280 to R172 sets the voltage gain of the amplifier at −1. Capacitor C281, from the output of U281 back to the input at R172, provides a fast feedback path to smooth transition spikes.

Sample Switch U270B, Hold Capacitor C260, and Voltage Follower U280 form a sample-and-hold circuit. The output of the High-Current Difference Amplifier at the junction of R194 and R196 is allowed enough time to settle to its new level before the 250 kHz $\overline{\text{SAMPLE}}$ pulse goes LO. At that time, the output of the Difference Amplifier is applied to the input of Voltage Follower U280A, and C260 is charged rapidly to that output voltage level. The $\overline{\text{SAMPLE}}$ pulse returns HI, and the BX output of the data selector goes to its high-impedance state to start the hold time. Voltage Follower U280 has high-impedance FET inputs; therefore, Hold Capacitor C260 discharges very little during the hold time.

The output of Voltage Follower U280 is held at the voltage level across C260; that level causes some value of current to flow through the series combination of R620 and R162 to the input of Integrator U282 (pin 2, the inverting input). The output of Integrator U282 at pin 6 ramps linearly for the duration of the hold cycle. (Actually, it ramps for almost the whole cycle, since the charge on Hold Capacitor C260 reaches the final level slightly before the sample switch is opened to start the hold time.) The time constants of the integrating network composed of R162 and of the series combination of R601 and C180 in parallel with R603 and C470 are such that the output of Integrator U282 reaches the new point position just as the next $\overline{\text{SAMPLE}}$ gate to U270B occurs. (A step change of 1 volt at the input causes a ramp of −1/4 V per μs (or −1 volt over the 4 μs cycle hold time.)

The feedback of this "new" point position to U281 through R160 modifies the reference at pin 3 of Difference Amplifier U281 (new reference is one-half the output voltage at U282 pin 6). The next voltage from Input Buffer U170 is applied to the input (pin 2 of U281) of the Difference Amplifier which now amplifies the difference between the present point position on screen (represented by the voltage at pin 3 of U281A) and the new position (applied to pin 2 of U281A). This difference voltage is sampled and stored on Hold Capacitor C260 where it sets a new current level through R162 and R620 from the output of Voltage Follower U280 to the input (pin 2) of Integrator U282A.

This cycle just described of comparing the old position to the new one, sampling the difference, and ramping to the new position continues for each point of a vector waveform display.

The adjustment associated with Voltage Follower U280 is INT ADJ potentiometer R620. This pot (the integrator adjustment) is used to compensate for charge current introduced from analog switch U270B. A corresponding adjustment is not present in the Horizontal Vector Generator circuit. A VECTOR COMP adjustment is present in both the Vertical and Horizontal Integrator circuits. The pots (R276 vertical and R376 horizontal) are used to adjust for minimum vertical and horizontal offset between the vector and dot displays.

Mode Select

The Mode Select Switch consists of data selector U290A (horizontal) and U290B (vertical). The switches route the various X-Axis and Y-Axis signal sources to the Horizontal and Vertical Output Amplifiers. The select signals to U290 coming from Miscellaneous Display Register U540 (diagram 17) allow the System μP to switch to the various display modes (Envelope, vectors, dots, and readout). The System μP does this by writing control bits to the 1Q and 2Q output of Display Register U540 (AMP1 and AMP0 respectively) which are applied to select input SEL_B (pin 9) of U290B and to SEL_A (pin 10) of U290A.

An envelope waveform display is produced by selecting the X0 and Y0 inputs of U290 to be switched to the Output Amplifiers. The signal applied to the Horizontal Output Amplifier for YT displays is the incrementing count from the Display Counter, and it moves the electron beam horizontally across the face of the crt. In the Vertical circuitry, a sample-and-hold circuit formed by Data Selector U270A and Hold Capacitor C912 bypasses the Vertical Vector Generator circuitry. The 250 kHz signal driving the data selector, derived from the same Clock Divider circuit that supplies the $\overline{\text{SAMPLE}}$ signal (U410A and B, diagram 17), is delayed slightly by the rc combination of R607 and C900. The delay allows the analog signal at the output of the Vertical DAC to settle before the sample from Input Buffer Amplifier U170 is taken. The voltage on C912 is applied to the rc integrator made up of R165 and C166 to produce a min-max envelope with shaded vectors between the successive dots.

To produce a vector display of a waveform, the System μP selects the X1 and Y1 inputs of U290. This routes the outputs from the Vector Generators (previously described) to the Horizontal and Vertical Output Amplifiers.

For non-vector waveform displays, the X2 and Y2 inputs are routed to the outputs of U290. These signal lines, V DOTS and H DOTS, come directly from the output of the Vertical and Horizontal Input Buffers (U170 and U370B), bypassing the Vector Generators. Since the data applied to the Horizontal DAC in YT mode is from the incrementing Display Counter, the Y-Axis vertical deflections are displayed versus a linear X-Axis ramp (horizontal time axis). If XY mode is in effect, the data applied to the Horizontal DAC is the digitized waveform data used to provide the X-Axis deflection signal. In either YT mode with vectors off or XY mode, a dot waveform display is seen on the crt.

To display readout, the H READOUT and V READOUT signals at the Y3 and X3 inputs are switched to the outputs of U290. The resistive divider formed by R171 and R282 slightly decreases the amplitude of the signal from the Vertical DAC to ensure that all the Readout vertical data points are limited to eight vertical graticule divisions and will appear on screen. Operational amplifier U392B and its associated resistors perform the opposite function on the H READOUT signal from the Horizontal DAC, increasing the gain of that signal. This horizontal expansion causes the center 40 characters of a displayed readout line (out of a possible 64) to horizontally fill the screen. (See the Readout State Machine description for further details.)

Horizontal and Vertical Output Amplifiers

Operation and circuitry of the Horizontal and Vertical Output Amplifiers is nearly identical. Therefore, only the Horizontal Output Amplifier circuit operation is described.

The selected horizontal signal from U290A is applied to operational amplifier U392A configured with a variable gain set by R586. (The corresponding buffer in the Vertical Output Amplifier has a slightly different variable gain range.) Operational amplifier U392D is an inverting amplifier having a gain of about two. Horizontal offset is adjusted with R587.

The output of U392D drives the negative horizontal-deflection plate (H−) of the crt and operational amplifier U392C. Operational amplifier U392C is configured as an inverting buffer with unity gain, and its output drives the positive horizontal-deflection plate (H+).

Spot-Wobble Correction

The Spot-Wobble Correction circuit provides a dynamic correction of spot-shift on the crt caused by signal intensity changes (crt electron-beam current changes). Correction is accomplished by injecting offsetting currents that vary linearly with beam-current changes into the Vertical and Horizontal Output Amplifiers.

The beam-current control voltage is inverted by U460A and applied to one end of R583 and R584 while the other end of both potentiometers is connected to the noninverted control signal. Each potentiometer is adjusted over this "differential" range to minimize the associated spot wobble while viewing a special calibration display provided with the Extended Calibration function.

HIGH-VOLTAGE SUPPLY AND CRT

The High-Voltage Power Supply and CRT circuit (diagram 19) provides the voltage levels and control circuitry for operation of the cathode-ray tube (crt). The circuitry consists of the High-Voltage Oscillator, the High-Voltage Regulator, the +61 V Supply, the Cathode Supply, the Anode Multiplier, the DC Restorer, Focus and Z-Axis Amplifiers, the Auto Focus Buffer, the CRT, and the various CRT Control circuits.

High-Voltage Oscillator

The High-Voltage Oscillator transforms power obtained from the −15 V unregulated supply into the various ac levels necessary for the operation of the crt circuitry. The circuit consists primarily of transformer T525 and switching transistor Q628 connected in a power oscillator configuration. Sinusoidal low-voltage oscillations set up in the primary winding of T525 are raised by transformer action to high-voltage levels in the secondary windings. These ac secondary voltages are applied to the +61 V Supply, the DC Restorer, the Cathode Supply, and the Anode Multiplier circuits that provide the necessary crt operating potentials.

Oscillation occurs due to the positive feedback from the primary winding (pin 4 to pin 5) to the smaller base-drive winding (pin 3 to pin 6) used to provide base drive to switching transistor Q628. The frequency of oscillation is approximately 50 kHz and is determined primarily by the parallel resonance frequency of the transformer.

OSCILLATION START UP. Initially, when power is applied, the High-Voltage Regulator circuit detects that the crt cathode voltage is too positive and pulls pin 3 of transformer T525 negative. The negative level is applied to the base of switching transistor Q628 through the transformer winding and forward biases it. Charge begins to flow in the primary winding through the transistor collector circuit and produces a magnetic field around the transformer primary winding. The increasing magnetic field induces an in-phase voltage in the base-drive winding that further supports the base-emitter voltage bias of the transistor. This in-phase feedback causes Q628 to remain on and continue supplying energy to the parallel resonant circuit formed by the winding inductance and interwinding capacitance of the transformer. As the primary voltage peaks, then begins falling, the induced magnetic field begins to decay. This decreases the base-drive voltage through the base-connected winding and begins to turn Q628 off.

As Q628 turns off, the magnetic field around the primary winding continues to collapse, and a voltage of opposite polarity is induced in the base-drive winding. This turns the switching transistor completely off. Once again, as the magnetic field builds and then reverses, the voltage induced in the base-drive winding changes direction, forward biasing Q628. At that point, the primary winding current starts increasing again, and the switching transistor is again turned on hard by the feedback supplied to the base-drive winding. This sequence of events occurs repetitively as the circuit continues to oscillate.

The oscillating magnetic field couples power from the primary winding into the secondary windings of the transformer. The amplitudes of the voltages induced in the secondary windings are a function of the turns ratios of the transformer windings.

High-Voltage Regulator

The High-Voltage Regulator consists of U168A and associated components. It monitors the crt Cathode Supply voltage and varies the bias point of the switching transistor in the High-Voltage Oscillator to hold the Cathode Supply voltage at the nominal level. Since the output voltages at the other secondary winding taps are related by turns ratios to the Cathode Supply voltage, all voltages are held in regulation.

When the Cathode Supply voltage is at the proper level (−1900 V), the current through R263 and the 19 MΩ resistor internal to High-Voltage Module CR565 holds the voltage developed across C260 at zero volts. This is the balanced condition and sets the output of integrator U168A at a level providing correct base drive for Q628 to hold the secondary voltages at their proper levels.

If the Cathode Supply voltage level tends too positive, a slightly positive voltage will develop across C260. This voltage causes the output of integrator U168A to move negative. The negative shift charges capacitor C717 to a different level around which the induced feedback voltage at the base-drive winding will swing. The added negative bias causes Q628 to turn on earlier in the oscillation cycle, delivering more energy per cycle to the resonant transformer. The increased energy in the resonant circuit increases the secondary voltages until the Cathode Supply voltage returns to the balanced condition (zero volts across C260). Opposite action occurs should the Cathode Supply voltage tend too negative.

+61 Volt Supply

The +61 Volt Supply circuit provides power to several other circuits on the High-Voltage board. Diode CR411 provides half-wave rectification of the first-tap voltage from the secondary of T525 and stores that charge on C317. Transistor Q215, zener diode VR210 and the associated components form a buffered zener regulator. Diode CR315 protects the base-emitter junction of Q215 should a failure reverse-bias the junction. Capacitor C218 stores a relatively large charge at the regulated level and supplies operating current to the load during current surges.

Cathode Supply

The Cathode Supply circuit is composed of a voltage-doubler and an rc filter network contained within High-Voltage Module CR565. This supply produces the −1900 V accelerating potential to the CRT cathode and the −900 V slot lens voltage. The −1900 V supply is monitored by the High-Voltage Regulator to maintain the regulation of all voltages from the High-Voltage Oscillator.

The alternating voltage from pin 10 of transformer T525 (950 V peak) is applied to a conventional voltage-doubler circuit at pin 7 of the High Voltage Module. On the positive half cycle, the input capacitor of the voltage doubler (0.006 μF) is charged to −950 V through the forward-biased diode connected to ground at pin 9 of the module. The following negative half cycle adds its ac component (−950 V peak) to this stored dc value and produces a total peak voltage of −1900 V across the capacitor. This charges the 0.006 μF storage capacitor (connected across the two doubler diodes) through the second diode (now the forward-biased diode) to −1900 V. Two rc filters follow the voltage doubler to smooth out the ac ripple. A resistive voltage divider across the output of the filter network provides the −900 V slot lens potential.

Anode Multiplier

The Anode Multiplier circuit (also contained in High-Voltage Module CR565) uses voltage multiplication to produce the +14 kV CRT anode potential. Circuit operation is similar to that of the voltage-doubler circuit of the Cathode Supply.

The first negative half cycle charges the 0.001 μF input capacitor (connected to pin 8 of the High Voltage Module) to a positive peak value of +2.33 kV. The following positive half cycle adds its positive peak amplitude to the voltage stored on the input capacitor and boosts the charge on the second capacitor of the multiplier (and those following) to +4.66 kV. Following cycles continue to boost up succeeding capacitors to values +2.33 kV higher than the preceding capacitor until all six capacitors are fully charged. This places the output of the last capacitor in the multiplier at +14 kV above ground potential. Once the multiplier reaches operating potential, succeeding cycles replenish charge drawn from the Anode Multiplier by the crt beam. The 1 MΩ resistor in series with the output protects the multiplier by limiting the anode current to a safe value.

Focus Amplifier

The Focus Amplifier, in conjunction with the auto-focus circuitry, provides optimum focus of the crt beam for all settings of the front-panel INTENSITY control. The Focus Amplifier itself consists of two shunt-feedback amplifiers composed of Q145, Q152, and their associated components. The outputs of these amplifiers set the operating points of a horizontally converging quadrapole lens and a vertically converging quadrapole lens within the crt. The convergence strength of each lens is dependent on the electric field set up between the lens elements.

Since the bases of Q145 and Q152 are held at constant voltages set by their emitter potentials, changing the position of the wiper arms of the ASTIG and FOCUS pots changes the current in the base resistors, R261 and R145. This changes the feedback currents in R245 and R246 and produces different output levels from the Focus Amplifiers; that in turn, changes the convergence characteristic of the quadrapole lenses.

Initially, at the time of adjustment, the FOCUS and ASTIG potentiometers are set for optimum focus of the crt beam at low intensity. After that initial adjustment, the ASTIG pot normally remains as set, and the FOCUS control is positioned by the user as required when viewing the displays. When using the FOCUS control, transistor Q152 is controlled as described above; however, an additional current is also supplied to the base node of Q145 from the FOCUS pot through R262. This additional current varies the base-drive current to Q145 and provides tracking between the two lenses as the FOCUS control is adjusted during use of the instrument.

Auto Focus Buffer

The convergence strengths of the quadrapole lenses also dynamically track changes in the display intensity. The VQ signal, applied to the crt at pins 5 and 6, is linearly related to the VZ (intensity) signal driving the crt control grid, and increases the strength of the lenses at higher crt beam currents. (A higher beam current requires a stronger lens to cause an equal convergence of the beam.) The emitter follower Q500 buffers the VZ signal (offset 15 volts by VR316) to the first and second quadrapole lenses. A linear relationship (as opposed to the "ideal" exponential relationship) between the Z-Axis drive (VZ) and quadrapole voltage (VQ) provides adequate dynamic focusing for low to medium Z-Axis drive. The High-Drive Focus adjustment R400 sets the attenuation factor at the output of buffer Q500. Capacitors C409 and C295 compensate for the capacitive loading of the quadrapole elements.

Z-Axis Amplifier

The high-voltage, high-speed transresistance amplifier U227 produces VZ, the Z-Axis drive signal. The amplifier has two signal inputs: ZINT—a current input that determines the output voltage VZ, and $\overline{\text{ZON}}$—a TTL gating signal that causes VZ to go to its lowest value (approximately 8 V) when HI. Capacitor C139 supplies current to U227 during VZ transitions, R137 is a current limiter, and C234 is a bootstrap capacitor to speed up VZ edges.

DC Restorer

The DC Restorer provides crt control-grid bias and couples both the dc and the low-frequency components of the Z-Axis drive signal to the crt control grid. This circuit allows the Z-Axis Amplifier to control the display intensity by coupling the low-voltage Z-Axis drive signal (VZ) to the elevated crt control grid potential (about −1.9 kV). Refer to Figure 3-10 for the following description.

The DC Restorer circuit operates by clipping an ac voltage waveform at the grid bias and the Z-Axis drive levels. The shaped ac waveform is then coupled to the crt control grid through a coupling capacitor that restores the dc components of the signal.

GRID BIAS LEVEL. An ac drive voltage of approximately 300 V peak-to-peak is applied to the DC Restorer circuit from pin 7 of transformer T525. The negative half-cycle of the sinusoidal waveform is clipped by CR541, and

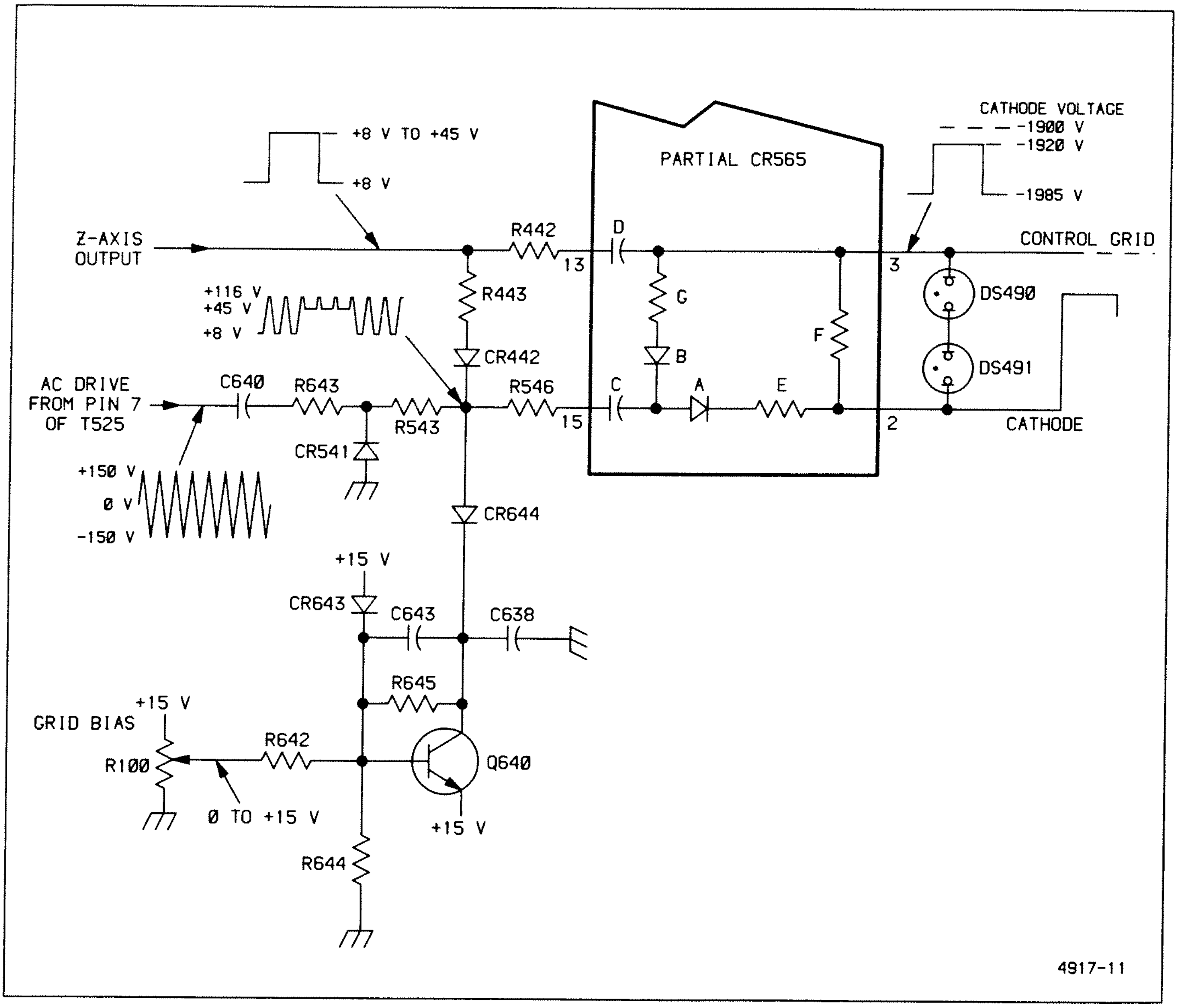

Figure 3-10. DC Restorer.

the positive half-cycle (150 V peak) is applied to the junction of CR442, CR644, and R546 via R643 and R543. Transistor Q640 and associated components form a voltage clamp circuit that limits the positive swing of the ac waveform at the junction.

Transistor Q640 is configured as a shunt-feedback amplifier with C643 and R645 as the feedback elements. The feedback current through R645 develops a voltage across the resistor that is positive with respect to the +15.6 V on the base of the transistor. The value of this additive voltage plus the diode drop across CR644 sets the clamping threshold. Grid Bias potentiometer R100 varies the voltage across base resistor divider R642 and R644 and thus sets the feedback current through R645. The adjustment range of the pot can set the nominal clamping level between +45 V and +75 V.

When the amplitude of the ac waveform is below the clamping threshold, diode CR644 will be reverse biased and the ac waveform is not clamped. During the time the diode is reverse biased, transistor Q640 is kept biased in the active region by the charge retained on C643 from the previous cycle. As the amplitude of the ac waveform at the junction of CR442 and CR644 exceeds the voltage at the collector of Q640, diode CR644 becomes forward biased, and the ac waveform is clamped at that level. Any current greater than that required to maintain the clamp voltage will be shunted to the +15 V supply by transistor Q640.

Z-AXIS DRIVE LEVEL. The variable Z-Axis signal (VZ) establishes the lower clamping level of the ac waveform applied to the High Voltage Module. When the amplitude of the waveform drops below the Z-Axis signal level, CR442 becomes forward biased, and the ac waveform is clamped to the Z-Axis signal level. The VZ level may vary between +8 V and +50 V, depending on the setting of the front-panel INTENSITY control.

The ac waveform, now carrying both the grid-bias information and the Z-Axis drive information, is applied to a DC Restorer circuit in the in the High-Voltage Module where it is lowered to the voltage level of the crt control grid (approximately −2 kV).

DC RESTORATION. The DC Restorer circuit in the High-Voltage Module is referenced to the crt cathode voltage via a connection within CR565. Capacitor C (labeling shown in Figure 3-10), connected to pin 15 of CR565, initially charges to a level determined by the difference between the Z-Axis signal level and the crt cathode potential. The Z-Axis signal sets the level on the positive plate of capacitor C through R443, CR442, and R546; the level on the negative plate is set by the crt cathode voltage through resistor E and diode A. Capacitor D is charged to a similar dc level through resistor F and R442.

When the ac waveform applied to pin 15 begins its transition from the lower clamped level (set by the Z-Axis signal) towards the upper clamped level (set by the Grid Bias potentiometer), the charge on capacitor C increases. The additional charge is proportional to the voltage difference between the two clamped voltage levels.

When the ac waveform begins its transition from the upper clamped level back to the lower clamped level, diode A becomes reverse biased. Diode B becomes forward biased, and an additional charge proportional to the negative excursion of the ac waveform (difference between the upper clamped level and the lower clamped level) is added to capacitor D through diode B and resistor G. The amount of charge added to capacitor D depends on the setting of the front-panel INTENSITY control, as it sets the lower clamping level of the ac waveform. This added charge determines the potential of the control grid with respect to the crt cathode.

The potential difference between the control grid and the cathode controls electron-beam current (the display intensity). With no Z-Axis signal applied (INTENSITY control off), capacitor D will be charged to its maximum negative value since the difference between the two clamped voltage levels is at its maximum value. This is the minimum intensity condition and reflects the setting of the Grid Bias potentiometer. During calibration, the Grid Bias pot is adjusted so that the difference between the upper clamping level (set by the Grid Bias pot) and the "no signal" level of the Z-Axis drive signal (VZ) produces a control grid bias that barely shuts off the crt electron beam.

As the INTENSITY control is advanced, the amplitude of the square-wave Z-Axis signal increases accordingly. This increased signal amplitude decreases the difference between the upper and lower clamped levels of the ac waveform, and less charge is added to capacitor D. The decreased voltage across capacitor D decreases the potential difference between the control grid and the cathode, and more crt beam current is present. Increased beam current increases the crt display intensity.

During the periods that capacitor C is charging and discharging, the control grid voltage is held stable by the long-time-constant discharge path of capacitor D through resistor F. Any charge removed from capacitor D during the positive transitions of the ac waveform will be replaced on the negative transitions.

The fast-rise and fast-fall transitions of the Z-Axis signal are coupled to the crt control grid through capacitor D. This ac-coupled fast-path signal sends the crt electron beam to the new intensity level, then the slower DC Restorer path "catches up" to handle the dc and low-frequency components of the Z-Axis drive signal.

Neon lamps DS490 and DS491 prevent arcing inside the crt by preventing the control grid and cathode from becoming too widely separated in voltage.

Other CRT Control Circuits

The CRT Control Circuits produce the voltages and current levels necessary for the crt to operate. Operational amplifier U168B, transistor Q269, and associated components form an Edge-Focus circuit that establishes the voltages for the elements of the third quadrapole lens. The positive lens element is set to its operating potential by Edge Focus adjustment pot R300 (via R393). This voltage is also divided by R278 and R277 and applied to the noninverting input of U168B to control the voltage on the other element of the third lens.

The operational amplifier and transistor of the Edge-Focus circuit are arranged as a feedback amplifier with R279 and R179 setting the stage gain. Gain of the amplifier is equal to the attenuation factor of divider network R278 and R277; so, total overall gain of the stage from the wiper of R300 to the collector of Q269 is equal to unity. The offset voltage between lens elements is set by the ratio of R279 and R179 and the +10 V reference applied to R179. This arrangement causes the two voltages applied to the third quadrapole lens to track each other over the entire range of Edge Focus adjustment R300.

Other adjustable level-setting circuits include "Orthogonality" Alignment pot R305, used to rotate the beam alignment after vertical deflection. This adjustment controls the amount of current through the Y-Axis alignment coil around the neck of the crt and is set to produce precise perpendicular alignment between the X- and Y-Axis deflections. The TRACE ROTATION adjustment pot, R1077, is a front-panel control. The effect of the adjustment is similar to the Y-Axis Alignment pot, but when adjusted, it rotates both the X-Axis and the Y-Axis deflections on the face of the crt. A final adjustable level-setting control is the Geometry pot R200, adjusted to optimize display geometry.

SYSTEM I/O

The System I/O circuits (diagram 20) provide methods of getting various types of signals or voltages into and out of the scope. These include a GPIB interface, an interface to the AutoStep Sequencer, Word-Trigger interface, an audio bell, and the probe-power connectors used to supply power to active probes.

GPIB

The GPIB interface provides an electrical interface adherent to the IEEE 488-1980 Standard using protocols defined in the Tektronix GPIB Codes and Formats Standard.

GPIB data transfers are done under control of U630, a GPIB Controller integrated circuit. The controller automatically produces proper handshaking and data direction control. Data is transferred to and from the GPIB bus through bidirectional buffer U624. Handshaking signals are transferred to and from the GPIB bus via the handshaking bidirectional buffer, U720. Data transfers between the GPIB Controller and the System μP are through bidirectional buffer U532.

When power is first applied, the $\overline{\text{GPIBRESET}}$ signal from register U754 holds GPIB Controller U630 in its reset state. The System μP then removes the reset and begins to initialize the internal registers of the GPIB Controller. To write data into the registers, the System μP writes data to the memory-mapped addresses between 6800h and 6807h. These addresses produce a LO $\overline{\text{GPIBSEL}}$ and a LO address bit A3 applied to U332B and enable the GPIB Controller. Data is written to the internal register defined by address bits A0-A2.

The GPIB Controller is now initialized and begins watching the handshake lines on the GPIB bus, looking for a data transfer to be initiated by another GPIB device on the bus. Data transfer may also be initiated by the System μP by writing data into the GPIB Controller data register. In either case, activity on the GPIB bus follows the sequences presented in Figures 3-11 and 3-12.

When data has been read into the controller from the GPIB bus, the $\overline{\text{GPIBINT}}$ (GPIB interrupt) request is asserted, telling the System μP that GPIB data is available. To receive the data, the System μP reads the GPIB Controller internal data register, automatically resetting the interrupt request.

Status of the GPIB operations is displayed on the three front-panel GPIB Status LEDs. These LEDs are turned on or off by the System μP by writing three control bits into Word Probe and GPIB LED Register U754.

See the Programmers Reference Guide included with this instrument for the GPIB commands and functions implemented in this scope.

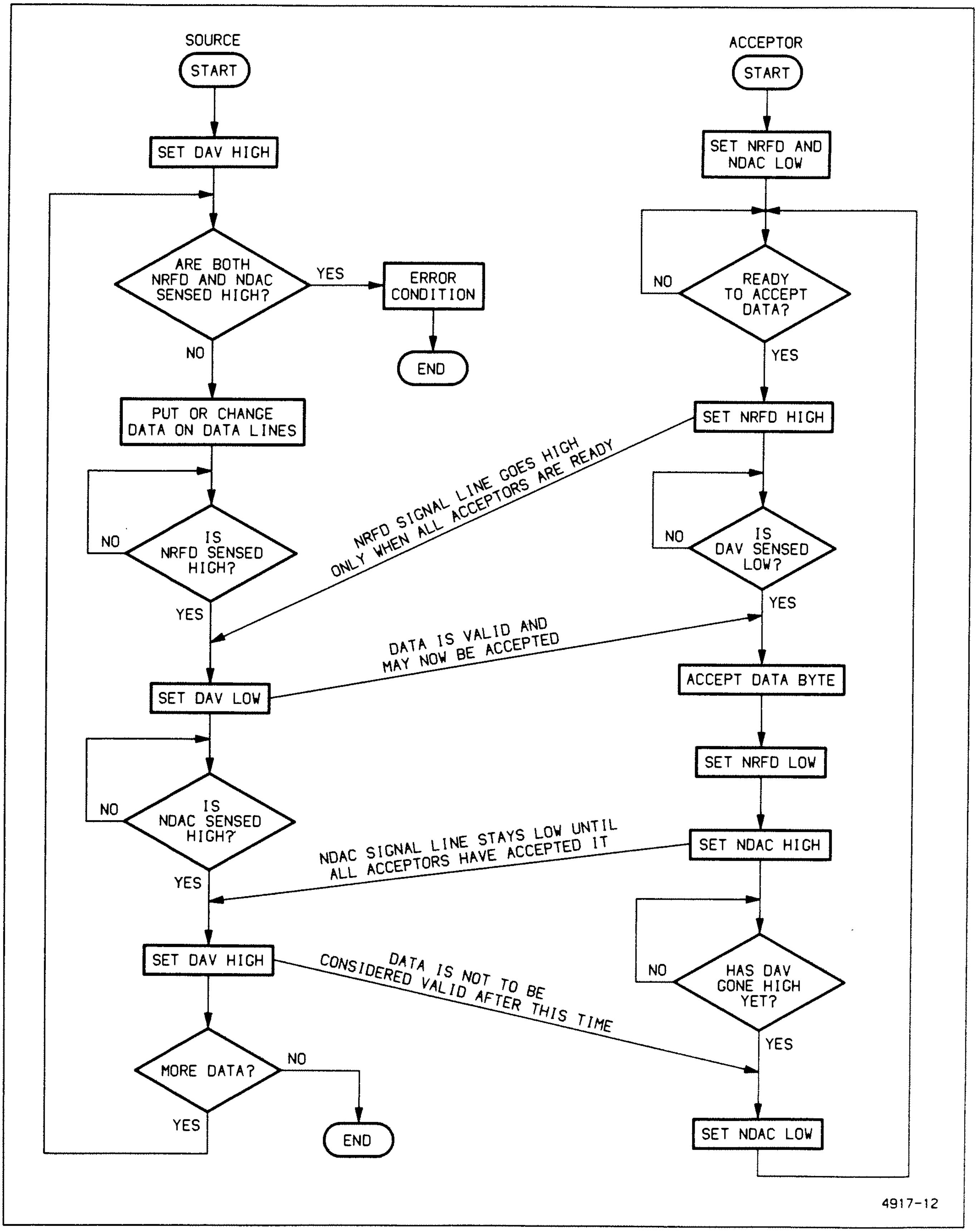

Figure 3-11. GPIB data flow diagram.

The GPIB may be set up to operate with a ThinkJet® printer or any plotter using the Hewlett-Packard Graphic Language® as a listen-only device on the bus. No controller may be used, and the printer/plotter should be the only device other than the 2430A on the bus.

Sequencer Output Circuit

The Sequencer Output circuit drives two output BNC connectors and accepts input from a third BNC connector. The outputs/input are called SEQUENCE OUT, STEP COMPLETE, and SEQUENCE IN, respectively. SEQUENCE OUT steps LO (TTL level) to indicate when a sequence completes execution; STEP COMPLETE steps LO to indicate when a step in a sequence completes. A TTL step from HI to LO (or grounding the input) to SEQUENCE IN restarts a temporarily halted sequence. See the Operators Manual included with this instrument for more information.

The System μP controls the SEQUENCE OUT and STEP COMPLETE output levels via Miscellaneous Register U760 (diagram 1). When a sequence and/or step is complete, the System μP sets SEQOUT and/or STEP COMP HI out of the Miscellaneous Register.

SEQOUT is coupled to Q104 via R300, a 1kΩ resistor. A TTL HI voltage level, dropped across the R330 and the base/emitter of Q104, is great enough to saturate Q104 and provides a LO SEQUENCE OUT at J1903. When SEQOUT is LO, Q104 is off. SEQUENCE OUT at J1903 is pulled up to about +3V via R108. (The +5 Volt supply is zener-regulated by R105 and VR 105 to provide the +3 Volt collector supplies for Q104 and Q107.)

The circuit action of Q107 and its surrounding circuitry is identical to the Q104 stage with STEP COMP driving the base of Q107 via R108 to provide STEP COMPLETE at J1904. CR104/CR107 provide output protection for Q104/Q107.

To read the SEQUENCE IN at J1905, the System μP periodically sets $\overline{\text{SEQINCS}}$ (Sequence In Chip Select) LO via Miscellaneous Register U884 (diagram 1). SEQINCS is routed to one input of OR-gates U250C and U132A; the other input of OR-gate U250C is connected to the System μP $\overline{\text{WR}}$ (write) line, and the other input of U132A is connected to the System μP $\overline{\text{RD}}$ line. With SEQINCS LO, the $\overline{\text{WR}}$ and/or $\overline{\text{RD}}$ can drive the output of their respective OR-gate LO, when they are asserted.

After setting SEQINCS LO, the System μp next asserts $\overline{\text{WR}}$ LO. This LO drives the output of OR-gate U250C LO to RESET the Q output of D-type Flip-Flop U894B LO. NEXT, $\overline{\text{RD}}$ is asserted LO ($\overline{\text{WR}}$ goes HI) to drive the out-

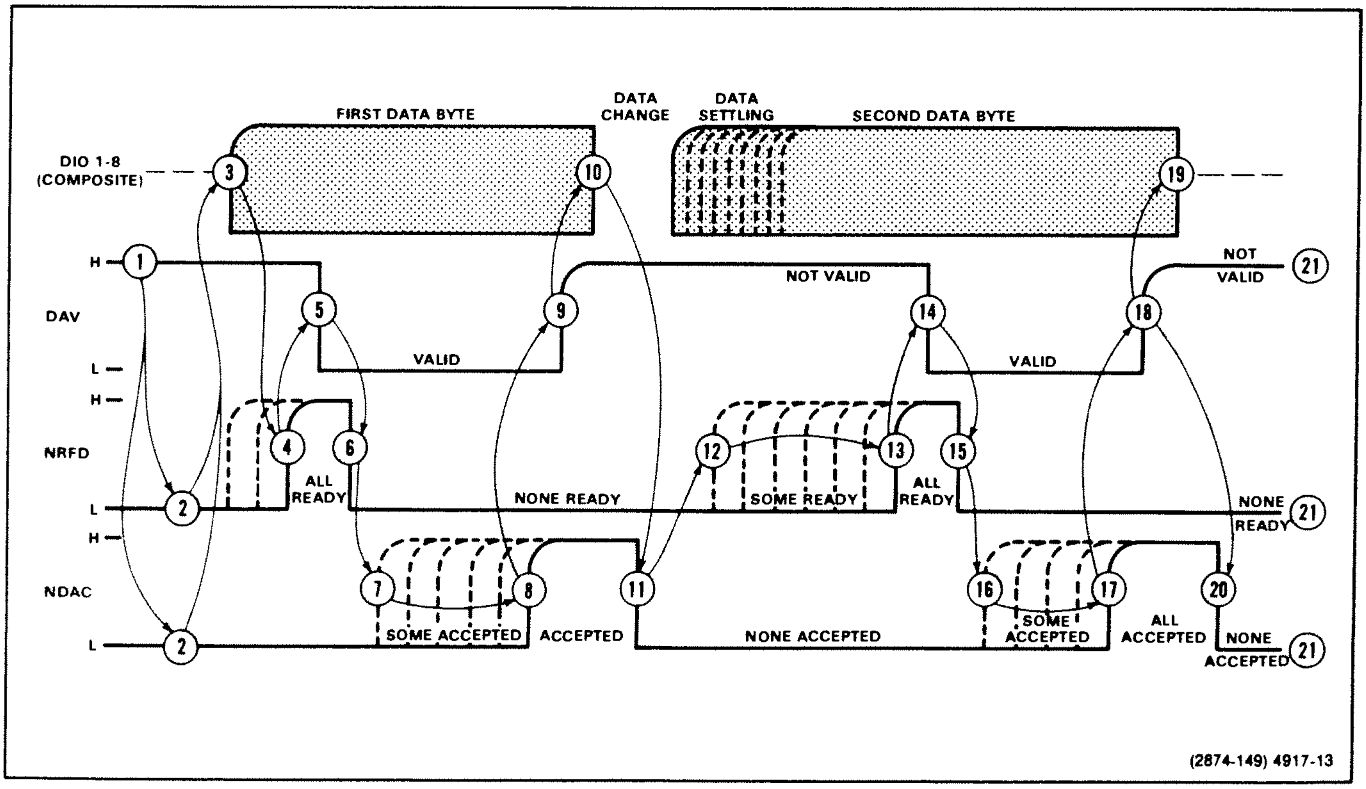

Figure 3-12. GPIB three-wire handshake state diagram.

put of OR-gate U132A LO. This LO enables the upper-four buffers of the Octal Buffer U120. With the Q-output of Flip-Flop U894B connected to the input of one of the enabled buffers, that reset-forced LO obtained at $\overline{WR}$ is coupled to the D0 line of the System μP Data Bus. The System μP monitors the D0 bit as long as $\overline{RD}$ and SEQINCS are asserted.

The input to inverter U424E is normally pulled up to +5 volts by R120. This HI is inverted LO by U424E and routed to the positive-triggered clock input of Flip-Flop U894B. If, during the time $\overline{RD}$ is asserted, SEQUENCE IN steps LO at J1905, it drives the clock input of U894B HI and the +5 volts hardwired to the D-input of the flip-flop latches to the Q output. With the Quad Buffer still enabled by $\overline{RD}$, the System μP reads the transition via data bit D0 and restarts the temporarily-halted sequence.

Word Trigger and GPIB Status Control Register

The Word Trigger circuit provides interface and control of the external Word Trigger Probe. Two bits from Control Register U754 are used to set the recognition mode of the Word Trigger Probe. Forty bits of serial data are applied to the W DATA (word data) line and clocked into the serial shift register in the word probe by toggling the W CLOCK (word clock) line. Once loaded, the Word Trigger Probe outputs a trigger pulse each time (and as long as) the set conditions are met.

The $\overline{WDTTL}$ output is applied to the trigger circuits where, if selected as the trigger source, it produces a scope trigger event. The trigger signal is buffered to the rear panel by U844D, Q720, and the associated components. Output levels are TTL compatible, with the maximum HI level being set by R716 and VR717. Output impedances are 47 ohms LO and 227 ohms HI. Diode CR722, zener VR717, and resistors R717 and R718 provide protection of the output circuit should an out-of-range voltage be applied to the output connector.

The remaining inputs and outputs of Control Register U754 are used to control the GPIB Status LEDs and to reset GPIB Controller U630.

Bell

The Bell circuit allows the scope to produce an audio tone to draw the operator's attention to certain warning and error conditions. The circuit consists of a free-running oscillator whose signal is gated through the output speaker.

The oscillator consists of timer U274, configured as an astable multivibrator (oscillator), and output transistor Q594, used to buffer the oscillator output. Current flowing in R274 and R276 charges C372 up until it crosses the trigger level at pin 2 of U274. This sets the output applied to the base of Q594 LO, turning the transistor off, and sets the discharge output at pin 7 to ground potential. Capacitor C372 now discharges through R276 until the threshold level at pin 6 is reached, at which time the output at pin 3 goes HI and the discharge pin goes to a high-impedance state. Capacitor C372 begins to charge through R274 and R276 again, completing the cycle. The cycle continues as long as instrument power is applied, alternately turning Q594 off and on with an approximate 50% duty cycle.

The BELL line from the Miscellaneous Register (U760, diagram 1) is used to gate this oscillator signal through the speaker to produce the audio output. As long as BELL is LO, transistors Q596, Q558, and Q592 are off, and current is cut off to speaker LS498.

When BELL goes HI, transistor Q596 turns on, which in turn, turns on Q588. With Q588 on, the base of Darlington transistor Q592 is pulled HI. Now, whenever the oscillator transistor Q594 is on, proper biasing conditions for Q592 are established and current flows from the +5 V_D supply to ground through Darlington Q592, the speaker LS498, and transistor Q594. When Q594 turns off, current flow is interrupted until the oscillator turns Q594 back on.

Since LS498 is inductive, the current decay portion of its cycle (Q594 off) tends to force pin 1 of the speaker above the +5 V_D supply level. Diode CR594 becomes forward biased in this case and shunts the decay current back to the +5 V_D supply, protecting transistor Q594 from overvoltage conditions.

As long as the BELL line remains HI, the speaker produces an approximate 2 kHz tone. In practice, the System μP sets the BELL line HI for a short time ($\simeq$4 ms), turning Q588 on, starting the tone and rapidly charging C590. When BELL returns LO, C590 gradually discharges through R594. As the capacitor discharges, bias on Q592, and thus current through the speaker, is reduced, causing the sound to gradually fade out in a pleasing "bell-like" tone.

Probe Power

The Probe Power outputs on the rear panel provide access to three of the instrument power-supply voltages and may be used to power approved voltage- and current-probe accessories. Contact your Tektronix sales representative for a list of approved probe accessories.

Video Option Control Register

The Video Option Control Register (U750 on diagram 20) is written to by the System Processor (address-decoded location 6012h) to control operational setup of the Video Option. The Video Option Control Register is initialized on power-up and provides for control of the following functions:

1. Selection of trigger field (Field1 or Field2).

2. Choice of triggering on positive- or negative-sync input signals (NEG-SYNC).

3. Selection of correct polarity of the offset signal via the CH2 INV signal.

4. Control of the display functions (VIDEO CLAMP and FAST CLAMP).

5. Enabling the Video Trigger Circuit to trigger the scope.

6. Selection of TV Line Coupling—allowing all lines to produce a trigger signal to the main Trigger circuit of the scope.

VIDEO OPTION

The Video Option (diagram 21) consists of additional hardware and firmware installed in the host instrument to enhance triggering on and viewing of composite video signals. The Video Option block diagram located in the tabbed foldout pages in the rear of the manual may be an aid in following the Video Option circuit descriptions.

The Video Option circuitry contains both video-signal processing and trigger-generation circuits. The video-signal processing circuits stabilize the input signal and separate the television synchronization signals (horizontal and vertical sync pulses) from the composite video signal. The trigger-generation circuits then count these separated sync pulses to determine when a TV Trigger signal is to be produced.

In the video-signal processing circuits, the gain of the AGC (automatic gain control) Amplifier is automatically adjusted to produce the correct signal amplitude to the Sync Pickoff Comparator for proper sync separation over a wide range of input signal levels. The Trigger Back-Porch Clamp adjusts the back-porch level of the input signal through the Fixed-Gain Amplifier on each sync pulse. The feedback to the Fixed Gain Amplifier compensates for level shifting caused by any power-line ripple riding on the composite video signal. The Sync-Tip Clamp circuit monitors the horizontal-sync pulse amplitude and produces the automatic-gain-control voltage that sets the gain of the AGC Amplifier. Sync pulses are separated from the composite video signal by the Sync Pickoff Comparator. The horizontal- and vertical-sync pulses are further separated by the Pulse Stretcher and Field Generator circuits for use in producing the horizontal clock and field-sync signals needed by the Trigger Generation circuitry.

To set up the Video Option operating modes, the System Processor writes control settings to the Video Mode Option Register (diagram 20) in the System I/O circuitry. The latched setting in the register is held until a different mode is needed. Programmable counters, also under System processor control, count the extracted horizontal sync pulses (lines) until the line number for the selected trigger point is reached. At that point, if the main trigger circuit is finished with holdoff, the TV Trigger Generator circuit produces a TV Trigger to the A/B Trigger Generator to trigger the next storage acquisition.

An additional display function added to Channel 2 is the TV CLAMP feature. When enabled, the circuitry holds the back-porch level of the displayed signal on Channel 2 at ground level. The Channel 2 Vertical Display Clamp circuit checks the back-porch levels of the incoming TV signal on Channel 2 and produces offsetting voltages to the Channel 2 Preamplifier to bring those levels back to ground reference. The circuit action produces a stable vertical signal display of a TV signal by removing power supply ripple that may be present. Either inverted or noninverted signals may be displayed with the TV CLAMP feature.

Video Signal Processing Circuitry

AGC AMPLIFIER. The AGC (automatic gain control) Amplifier, Q514, U612, and U710B, amplifies the composite-video input signal from the selected trigger channel. Stage gain is controlled by feedback that is derived from the amplitude of the incoming horizontal sync pulses. The amplifier itself is formed by two cross-connected differential amplifier pairs in U612 that permit normal or inverted amplification of the signal. The front-panel SLOPE/SYNC switch selects whether the amplifier is inverting or noninverting to match the required signal polarity for the sync-separation circuits. For correct operation of the sync separation circuit, the composite-video signal must be sync-negative; therefore, if a "noninverted" signal display has positive sync, the SLOPE/SYNC switch may be pressed to invert the signal (+ SLOPE LED is on for positive-sync input display). Inversion only occurs in the trigger Sync Separator path; the display polarity remains unaffected.

Gain of the AGC Amplifier is controlled by the action of the Trigger Back-Porch Clamp, the Sync-Tip Clamp, and the Automatic Gain-Control circuitry working together to set the channel resistance of FET Q514 and thereby the gain of AGC Amplifier U612. Amplifier gain is automatically adjusted to maintain the sync-tip level at a known point relative to the back-porch amplitude of the signal. This action provides an accurate and stable pickoff point on the signal to the Sync Pickoff Comparator circuit (Q504 and Q510) with input video signals of different or varying amplitudes. The minimum gain of the circuit is decreased (to permits the application of higher amplitude signals) by the use of constant-current diodes CR526 and CR620 as the current sources for the differential amplifiers.

When power is first applied, the operating level of the AGC Amplifier is established by feedback only. With no signal applied, the channel resistance of Q514 is minimum, setting the gain of the AGC Amplifier to maximum. With maximum gain and no signal, the feedback loops of the Back-Porch Clamp and the Sync-Tip Clamp set the circuit gain as if an average "ground" signal were being received.

The composite-video input signal is applied to one input of the differential AGC Amplifier at pin 3 of U612 and to Dc-Offset Amplifier U710B via a low-pass filter composed of R714 and C714. The low-pass filter averages the signal at the input of U710B so that only the average (dc) signal level appears at the output of U710B and on pin 11 of U612. Since the input signal swings about this average level, the AGC Amplifier output signal will be centered in its linear amplification region.

The base-emitter bias of the differential output transistors within U612 are controlled by the NEG-SYNC signal from Video Option Control Register U750 (diagram 20). When the NEG-SYNC bin is set HI, the transistors connected to pins 2 and 9 will be biased on, with those at pins 6 and 13 biased off. When NEG-SYNC is set LO, the conducting transistors are switched, and the polarity of the output signal driving transistor Q612 is inverted. Common-base transistor Q612 level shifts the output signal from the AGC Amplifier and provides voltage gain to drive U610D.

FIXED GAIN AMPLIFIER. The Fixed Gain Amplifier circuit, formed by U610A, B, and C, Q502, and U710C, provides additional gain to the video signal from the AGC Amplifier. The Trigger Back-Porch Clamp circuit monitors the back-porch level of the resulting signal and injects an offsetting dc level into the Fixed Gain Amplifier via U710C to shift that level to approximately +4.5 V.

Emitter-follower U610D drives one input of a differential amplifier made up of U610A and U610B, while the other input is driven by the output signal of U710C. Transistor U610C and its associated components form the current source for the amplifier. The collector output of U610B drives the input of the Sync Pickoff Comparator.

Transistor Q502 and its associated circuitry act as a start-up circuit that monitors the dc output level of U610B and applies an offset voltage to pin 10 of U710C should that level go below zero volts. This occurs when going from a "no-signal" or low-signal condition to a strong signal. If the dc output level goes below ground, diode CR612 will become forward biased, shutting off Q502. With Q502 off, the −15 V supply applied via resistor R506 will forward bias CR606 to charge C713 negatively. This pulls the output voltage of U710C negative and decreases base drive to U610B. Reducing base drive reduces the collector current so that the collector voltage of U610B returns positive until the above zero-volt output level is restored and CR612 becomes biased off.

SYNC PICKOFF COMPARATOR. The Sync-Pickoff Comparator, composed of Q504 and Q510, switches when the amplitude of a sync pulse crosses the comparator threshold level. The switching threshold is set by the biasing resistors of Q510, R408 and R409, to about 50% of the sync level to eliminate any video information. The output signal from the collector of Q510 is the composite of all detected sync pulses, and the output of Q504 is an inverted replica of that signal.

SYNC-TIP CLAMP AND AUTOMATIC GAIN CONTROL. Transconductance Amplifier U510, in conjunction with the AGC Amplifier, is used to clamp the sync-tip level. Amplifier U510 is enabled by the bias current supplied by Q512 when sync tips turn that transistor on. This amplifier acts as a weak operational amplifier to set the sync-tip level constant when Q512 is conducting to supply bias current to pin 5 of U510.

The Sync-Tip Clamp holds the negative-sync tips at about +0.5 V, so the resulting sync pulses are approximately 4 V in amplitude. Anytime the negative-sync tips at the collector of U610B go below about +0.5 V, input pin 3 of U510 will go below the ground reference at the other input. This causes the output of U510 to go low when enabled, and C512 begins discharging slowly toward −15 V. This decreasing voltage is applied to the gate of FET Q514 to increase the channel resistance and decrease the gain of the AGC Amplifier. Since U510 is a transconductance amplifier, it can change the voltage across C514 only a small amount during each sync pulse, and a few horizontal-line cycles are needed to reduce the gain of the AGC Amplifier to the new operating level. Between sync tips, when amplifier U510 is disabled, the long time constant of R610 and C512 holds the bias for Q514 (and thus gain of the AGC Amplifier) nearly constant.

Diode CR502 acts to reduce AGC Amplifier gain quickly if the negative-sync-tip amplitude at the collector of U610B drops below −0.8 V. If the diode becomes forward biased, as it might should the signal amplitude go suddenly negative, Q510 will be turned on for a longer time until the signal amplitude returns to a lower level. Amplifier U510 can then increase the channel resistance of Q514 more quickly to reduce gain of the AGC Amplifier and return the sync-tip amplitude to the correct level.

TRIGGER BACK-PORCH CLAMP. The Trigger Back-Porch Clamp circuit formed by U504, U410A, and associated components, is enabled for a short time during each horizontal-sync pulse immediately following the sync tip (during the back-porch time). The output of the Trigger Back-Porch Clamp is used to hold the back-porch level of the composite-video signal to a predetermined dc level. This, in combination with the action of the Sync-Tip Clamp, produces sync pulses that are approximately 4 V in amplitude.

Transconductance Amplifier U504 is enabled by turning transistor U410A off on the falling (trailing) edge of the inverted sync pulse from Q504 (via C308). Bias current to turn on U504 is then supplied through R403. The amplifier will stay enabled until the current supplied by resistor R214 charges C308 back positive enough to bias U410A back on (in approximately 1 μs). During the time that U504 is enabled, it senses the back-porch level of the composite-video waveform applied to pin 3 via resistive divider R613, R602, and R604. Depending on whether the sensed level is above or below the ground reference level on pin 2, the amplifier output will either charge or discharge capacitor C713 to a new voltage level. This will slightly change the offset voltage applied to pin 4 of U610B (via U710C), shifting the entire composite-video waveform in the direction required to hold the back-porch level at +4.5 volts (zero volts on pin 3 of U504). During the period between back porches, C713 acts as a hold capacitor to maintain the offset bias on U610B.

PULSE STRETCHER. The Pulse Stretcher lengthens the horizontal-sync pulse width to produce a more symmetrical, faster rise-time clocking pulse. It also removes alternate equalizing and serrated pulses that occur during the NTSC TV signal vertical-sync block from the composite-sync waveform in order to maintain the correct horizontal clock rate.

Transistors U420B, U420C, and associated components form a monostable multivibrator used to stretch the width of the horizontal-sync pulses. The leading edge of each horizontal-sync pulse turns on U420C which, in turn, reverse biases diode CR224 via C325 to turn off U420B. The resulting HI at the collector of U420B keeps U420C biased on (via R421). The output at the collector of U420B remains HI until C325 charges to about +1 volt via R224; then, CR224 becomes forward biased to once again turn U420B on. The collector voltage of transistor U420B then drops to about +0.4 V, at which point diode CR329 conducts to clamp the output at one diode drop above ground. This stretched output pulse from the monostable multivibrator is level-shifted down one diode drop through CR328 to produce the TTL-compatible HORIZCLK signal used to generate trigger signals to the main Trigger circuit of the oscilloscope.

Since the equalizing and serration pulses in the vertical-sync block occur at twice the horizontal-sync rate (see Figures 3-13 and 3-14), every other one must be prevented from triggering the monostable multivibrator to keep the line count correct. The DLY'D HCLK (delayed Horizontal clock) applied to the base of U420B (via R210) holds that transistor on for a period of time between the normal horizontal line-sync pulses. This action effectively removes the unwanted pulses from the HORIZCLK output by preventing them from triggering the multivibrator circuit.

CLOCK FREE RUN. If non-NTSC standard television signals are being used, the vertical-sync block may not be serrated. To maintain the proper horizontal-sync rate during the absence of signal-supplied horizontal pulses, the Clock Free-Run circuit produces "artificial" clock pulses. Therefore, the line count will continue and be correct when the next horizontal-sync pulse does arrive. The signal used as the self-generated HORIZCLK signal is derived from the VCO (voltage-controlled oscillator) output (2XH) of the Phase-Locked Loop circuit. That signal, at twice the horizontal-sync rate, is divided by two at the Q output of flip-flop U220B. It is then wire-ORed into the HORIZCLK signal line via R334 and CR332. If a horizontal-sync pulse is not present to trigger the monostable multivibrator, CR332 will be biased on by the HI HCLK to pass that pulse to the HORIZCLK signal line. When the Phase-Locked Loop (PLL) circuit is locked (synchronized) with the incoming horizontal sync, the HCLK rising edge will slightly lag the incoming sync pulse to prevent jitter of the HORIZCLK signal to U524B.

PHASE-LOCKED LOOP (PLL). Phase-Locked Loop U314 locks onto the horizontal-sync signal to produce a synchronized clock at twice the horizontal-sync rate (2XH). The 2XH clock is used to extract the various sync- and field-identification signals from the composite-sync waveform. It is also divided and delayed to obtain the DLY'D HCLK (see Figure 3-13) signal used in eliminating alternate equalizing and serration pulses from the HORIZCLK signal and the input to the PLL Phase Comparator inputs.

The 2XH VCO (voltage-controlled oscillator) output is divided by two by flip-flop U220B to produce both the HCLK and $\overline{\text{HORIZCLK}}$ signals at the horizontal-line rate. Horizontal sync from the input signal is applied to the Phase Comparator input of U314 at pin 14 via U308B. The $\overline{\text{HORIZCLK}}$ from the $\overline{\text{Q}}$ output of U220B is applied to U314 at pin 3 through U308C.

Phase Comparator output 2 (PC2 OUT at pin 13) of PLL U314, outputs the PLL ERROR signal whenever the leading edges of the $\overline{\text{HORIZCLK}}$ signal on pin 3 and the horizontal-sync pulses on pin 14 do not coincide. The error signal output is integrated by R322, R320, and C322 to produce a voltage (applied to pin 9) used to correct the operating frequency of the VCO. When either no phase errors exist or no signals are present to compare (both phase-comparator inputs at the same level), pin 13 goes to a high-impedance state, and the voltage on C322 maintains the operating frequency of the VCO. Resistors R323 and R324 and capacitor C324 set the operating frequency range of the PLL circuit. A bleeder resistor, R327, reduces the charge on C322 slightly between each error signal output so that the $\overline{\text{HORIZCLK}}$ signal will always lag the horizontal-sync of the input signal by a small amount. This

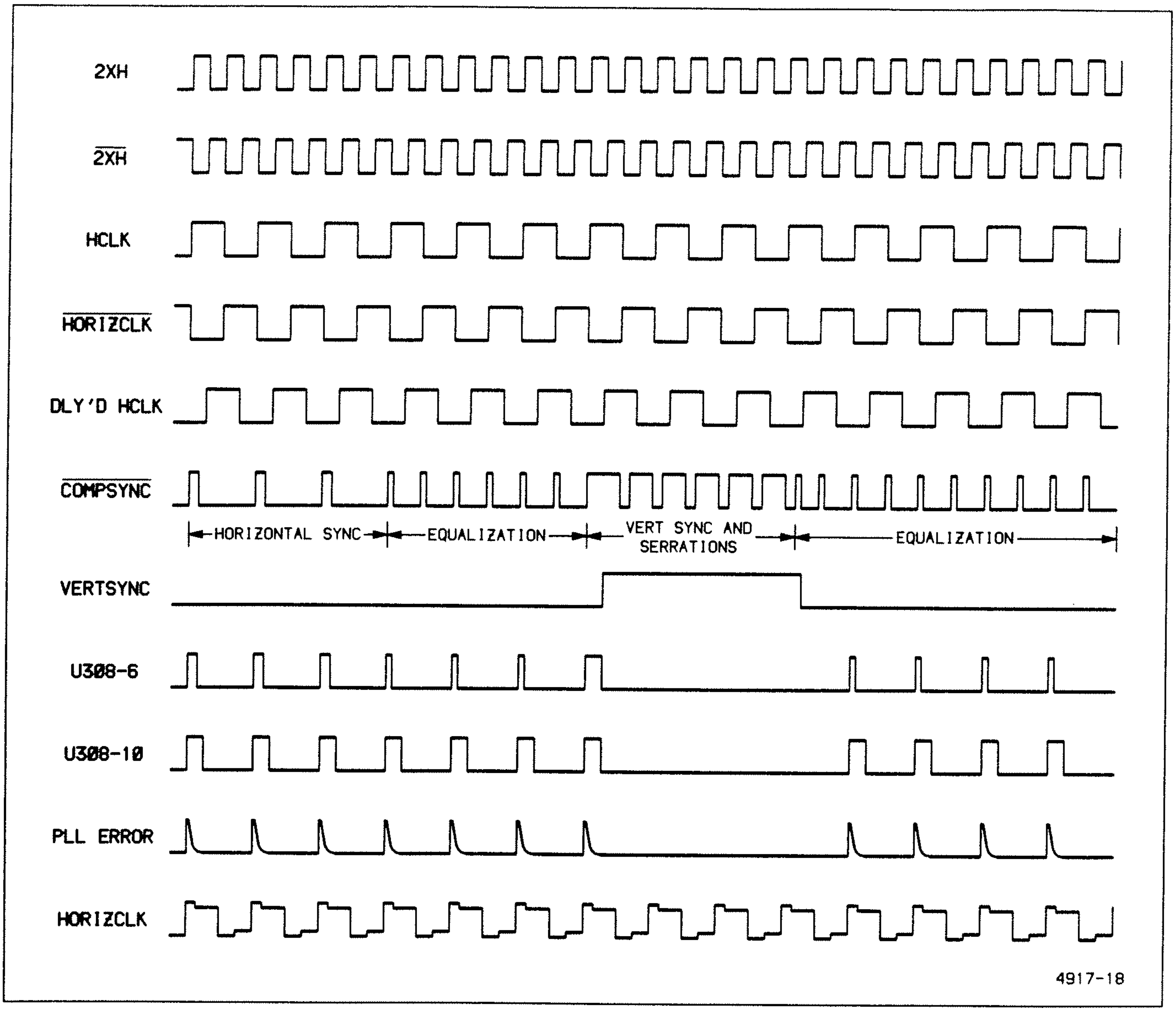

Figure 3-13. Video Option waveforms.

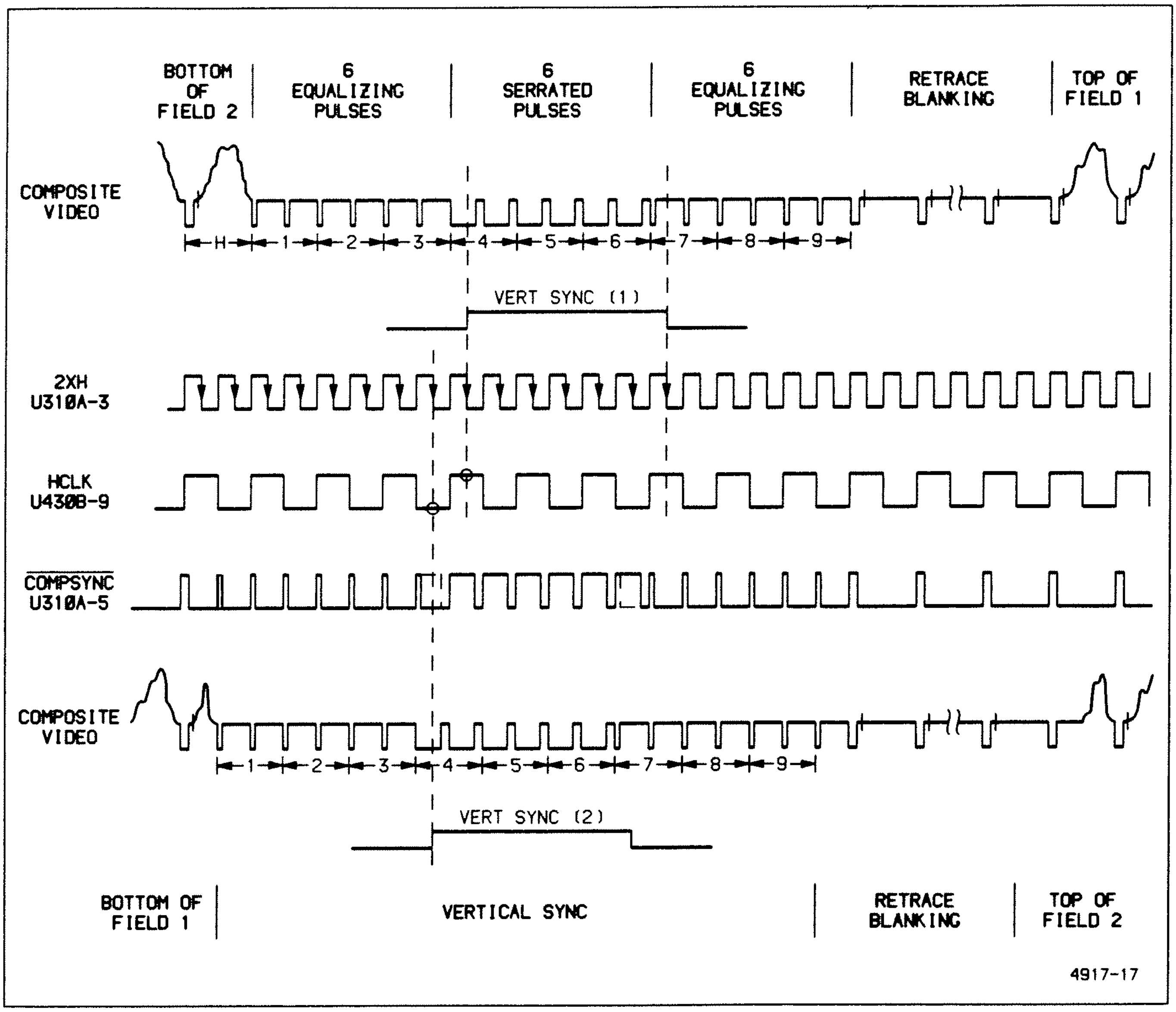

Figure 3-14. Video Option field-sync identification.

slight lag prevents the possibility of jitter in the HORIZCLK signal going to clock TV Trigger flip-flop U524B.

A similar signal (PLL LOCK) from pin 1 of the Phase Comparator is integrated by R326 and C330. If the PLL is not locked onto the input signal, the PLL LOCK output remains in the LO state long enough to be sensed by the PLL Unlock Detector. The long LO state of the PLL LOCK signal discharges C330 negative enough with respect to the emitter voltage of Q330, that the transistor becomes biased on. The collector voltage of Q330 will then go high, and Vertical Sync flip-flop U310A and Delayed Horizontal Clock flip-flop U220A will both be reset by the HI UNLOCKED signal. With U220A and U310A both reset, the DLY'D HCLK and VERTSYNC signals are held LO, and the equalizing pulses and vertical-sync serrations are no longer prevented from passing through NOR-gate U308B. The PLL Phase Comparator then sees the entire input signal during attempts to lock on so that locking will occur in the proper range. While the unlocked condition exists, the Channel 2 Vertical Display Clamp circuit is held disabled (via R328) by the HI state of $\overline{\text{TVCLAMP}}$ to prevent an invalid offset from being sent to the Channel 2 Vertical Preamplifier.

When lock is achieved, the phase difference between the two input signals becomes very small. The PLL LOCK pulse output level remains in the HI state (no error) long enough that C330 is allowed to charge positive and turn off transistor Q330. UNLOCK then goes LO to remove the resets from flip-flops U310A and U220A, allowing them operate, and $\overline{\text{TVCLAMP}}$ goes LO to enable the Channel 2 Vertical Display Clamp circuit. Unwanted equalizing pulses and the vertical-sync serrations are now prevented from passing to PLL Phase Comparator inputs by the DLY'D HCLK (delayed horizontal clock) and VERTSYNC signals applied to the PLL Phase Comparator Input NOR-gates, U308B and U308C (see Figure 3-13).

The DLY'D HCLK is shifted one-quarter HCLK cycle. When the DLY'D HCLK is HI, the outputs of both NOR-gates at the inputs to the PLL Phase Comparator are held LO, and the alternate equalizing pulses of composite-sync signal are prevented from passing to the PLL Phase Comparator. The vertical-sync serrations are prevented from passing through NOR-gate U308B by the HI VERTSYNC signal applied during vertical-sync times. Both types of unwanted pulses are thereby eliminated from the Phase Comparator inputs. The remaining sync pulses to be compared with the $\overline{\text{HORIZCLK}}$ signal are then only at the horizontal-sync frequency, and the VCO output frequency shifts slightly as necessary to bring that frequency to precisely twice the horizontal-sync rate (2XH). The charge on capacitor C322 holds the VCO to that output frequency throughout the vertical-sync period when all serration pulses are disabled from the Phase Comparator input and no comparisons are being made.

DELAYED HORIZONTAL CLOCK. The Delayed Horizontal Clock (DLY'D HCLK) is used to remove alternate equalizing pulses and serration pulses from the composite-sync waveform in order to maintain precise sync for horizontal line counting. The PLL-generated HCLK signal from the Q output of U220B is clocked into U220A by the $\overline{\text{2XH}}$ pulse from NOR-gate U308A (acting as an inverter). The inversion of the two-times clock delays the Q output of flip-flop U220A by one-quarter of a horizontal clock (HCLK) cycle. The quarter-cycle delay enables the HI portion of the output (applied to U420B via R210) to mask the alternate, unwanted equalization and serration pulses (occurring at twice the horizontal-sync rate) from the HORIZCLK output by preventing U420B, in the Pulse Stretcher circuit, from switching during those time periods. The same signal masks the unwanted equalization pulses from the PLL inputs by disabling NOR-gates U308B and U308C from passing signals to compare during the DLY'D HCLK HI state. All the vertical-sync serration pulses are eliminated from the PLL Phase Comparator input by the HI state of the VERTSYNC signal applied to the input NOR-gates.

VERTICAL SYNC. The Vertical Sync circuitry outputs pulses for both the Field 1 and the Field 2 vertical-sync times. These VERTSYNC pulses are used to toggle the Field Sync Generator. The VERTSYNC signal is produced by clocking the level of the $\overline{\text{COMPSYNC}}$ signal on the D input (pin 5) of U310A into that flip-flop using the inverted two-times horizontal clock $\overline{\text{2XH}}$. Figure 3-14 shows that only during a vertical-sync interval will the $\overline{\text{COMPSYNC}}$ signal be HI on the rising edge of the $\overline{\text{2XH}}$ clock. At all other (non-vertical sync) times, the $\overline{\text{COMPSYNC}}$ signal will be LO on the rising edge of the 2XH clock. Thus, the Q output of flip-flop U310A will be clocked HI during vertical-sync intervals for VERTSYNC, and it will be clocked LO during the rest of the field.

FIELD-SYNC GENERATOR. The Field-Sync Generator produces the FIELD signal used in identifying the individual fields of picture information. For interlaced-scan signals, the signal identifies which field a given line of picture information belongs to (exceptions are explained in the Line Counter description); while, for non-interlaced-scan signals, it toggles to indicate vertical sync. The circuit consists of an Interlace/non-Interlace Detector, a Vertical-Sync Latch (interlaced), and a Vertical-Sync flip-flop (non-interlaced).

To detect whether a signal is interlaced (two vertical-sync pulses per frame) or non-interlaced (only one vertical-sync pulse per frame), flip-flop U310B is clocked to transfer the level of the HCLK signal on the D input to the $\overline{Q}$ output by the VERTSYNC clock at the start of a vertical-sync period. For non-interlaced displays, the vertical-sync rising edge always occurs during a HI portion of the HCLK signal, and the $\overline{Q}$ output of U310B will be clocked HI; while, for interlaced displays, the $\overline{Q}$ output will alternate between HI and LO.

The $\overline{Q}$ from pin 12 of U310B controls two other flip-flops U430A and U430B, through the circuit action of transistors U420A and Q422. If the output of U310B is not toggling (non-interlaced signals), transistor U420A will be turned off by pull-down resistor R426. This allows the base bias voltage of Q422 to go positive as C426 charges through R429 and R428. Soon, Q422 is biased off and flip-flop U430B becomes reset. The reset on U430B from C426 holds the $\overline{Q}$ output HI to reverse bias CR334 and isolate the $\overline{Q}$ output from the FIELD signal line. At the same time, the LO TVINTERLACED signal applied to the set input of U430A from the collector of Q422 enables that flip-flop to toggle on the rising edges of the vertical-sync pulses applied to the clock input (pin 3). This toggling is required to reinitialize the counters after they have counted their last lines. The TVINTERLACED signal is also applied to the Processor Miscellaneous Buffer (U854, diagram 1) where it may be read by the System μP to determine whether the video signal is interlaced or non-interlaced. The System μP must be able to determine this information to properly control the line counting.

For interlaced displays, the output from U310B will toggle. This will alternately turn transistor U420A on and off at the vertical-field rate. The first time U420A gets turned on by an interlaced-system signal, it discharges C426 and turns Q422 on. Capacitor C426 will charge positive through R429 and R428 when U420A turns off, but the long time constant of the charging path prevents the charge from getting positive enough to reassert the reset to U430B before the next toggle cycle once again discharges the capacitor. Flip-flop U430A is held set by the HI TVINTERLACED (interlaced) signal asserted from the collector of Q422, and CR336 is reverse biased to isolate U430A from the FIELD signal line. The resulting FIELD signal, as a result of the output of flip-flop U430B, will be HI for all lines in Field 1 and LO for all lines in Field 2 (with a few exceptions that are explained in the Line Counters description).

LINE COUNTERS. Line Counter U530 contains three programmable counters (at decoded addresses 6808h through 680Fh) that are set by the System Processor to determine when the chosen line number in the field selected for triggering is reached. The various control registers of the counter are set up to count horizontal clock pulses (lines) to determine line location in the field.

The Line Counter is enabled whenever its address block is decoded by the system Address Decode circuitry. To differentiate it from the GPIB circuitry (which also answers for the same block of decoded addresses), the Video Option uses address bit A3 as a second chip select. Specific registers within the Line Counter are addressed using address lines A0-A2 applied to the register-select inputs. Reading and writing of the selected register is controlled by the System μP using the $\overline{WR}$ select line while the E (enable) clock synchronizes transfers to the System μP rate.

Once the proper setup data (defining counter mode and line number) is written to the Line Counter, the enabled counter will begin counting horizontal clock pulses (lines). Counters are alternately started as the FIELD signal toggles, and counters 1 and 2 produce a LO output when their predefined counts are reached. Counter 3 is used to determine the number of LINES in a FIELD (of FIELD 2 if in an interlaced system). The System μP checks the "previous field" line count by reading the counter contents via the data bus.

LINE COUNT ADJUSTMENTS. Depending on the type of signal being triggered upon (System M or non-System M) and the desired line for trigger, the System μP adjusts both the numbers preloaded to the counters and the field to which the assigned line-count relates. These line-count and relative-field adjustments are required for the following reasons.

1. The HORIZCLK coincident with a switch in the FIELD indicator does not produce a count. Since the FIELD change doesn't enable the opposite counter in time to catch the rising edge of the HORIZCLK (responsible for the change), the preloaded line count must be reduced by one.

2. The counters cannot produce a "zero-count" delay; i.e., the counter output goes LO one count (line) after the counter reaches zero. Even when set to zero, a count must still occur; so the line count must be reduced by one again.

3. The counter outputs merely arm the trigger circuit, with the next line sync producing the actual trigger; therefore, line count must be reduced again by one.

RELATIVE FIELD ADJUSTMENTS. For non-System M television signals (line one coincident with the FIELD sync pulse), the line-adjustment requirements described above require that the first three lines of either field be counted relative to the previous FIELD pulse.

Since, by definition, System-M fields begin numbering lines three lines before the vertical field-sync occurs, and due to the line-adjustment requirements described above, the first six lines of System-M fields must be counted relative to the previous FIELD pulse.

As stated in the "Line Count Adjustments," the trigger arming pulse occurs one line count prior to reaching the selected trigger line. Depending on whether the System Processor has selected the arming pulse relative to Field 1 or Field 2, either NAND-gate U541C or NAND-gate U541D will be enabled by a control bit (FLD1 or FLD2) from Video Option Control Register U750. The selected pulse, when it occurs, is passed through the enabled gate, through U541A and U424D, and appears as a clock pulse at the trigger-arm flip-flop, U524A.

TV TRIGGER GENERATOR. The TV Trigger Generator circuit produces the signal to trigger the Oscilloscope at the designated horizontal line. The output from the Line Counter arms the TV Trigger Generator circuit, enabling a trigger to be produced on the next line-sync pulse. Generation of a TV trigger from the circuit is enabled by a HI TVENA (TV-enable) bit from Video Option Control Register U750 (diagram 20).

In the Video Option, as in the main Trigger Generator a trigger signal is inhibited from being produced during trigger holdoff. For the holdoff period, the ATHO (A-trigger holdoff) signal applied to U424C is HI to hold arming flip-flop U524A reset which, in turn, holds trigger flip-flop U524A reset. When the holdoff processing cycle is completed, the ATHO signal goes LO to remove the reset from U524A and enable triggering.

Assuming TV Line Coupling mode is not active, the LINECPL (line coupling) bit applied to U541B pin 5 will be LO, and arming flip-flop U524A will be enabled. When the Line Counter has counted the proper number of lines relative to the Processor-selected field, flip-flop U524A will be clocked. This produces a HI "armed" level applied to the reset input of trigger flip-flop U524A that releases the reset condition of the flip-flop. The next HORIZCLK pulse (line) then clocks a LO to the $\overline{Q}$ output, $\overline{TVTG}$, that defines the trigger point in the acquisition record. The $\overline{TVTG}$ output is reset HI when trigger holdoff (ATHO) goes HI to reset the flip-flop via U424C and U524A.

When TV Line Coupling mode is selected, the LINECPL bit from the Video Option Control Register will be set HI. This causes flip-flop U524A to be immediately armed when A trigger holdoff ends by forcing a set signal to pin 4 of that flip-flop through NAND-gate U541B. In this mode, a trigger will occur on the first line sync following the end of each holdoff interval. The resulting display will be stable with respect to horizontal sync pulses but will not be stable with respect to the vertical sync pulses.

CH2 VERTICAL DISPLAY CLAMP. The Channel 2 Display Clamp circuit clamps the back-porch level of the triggered-display signal near the on-screen zero-volt reference. This allows automatic positioning of the display on the crt when probing various points with differing dc levels and removes vertical jitter that would be caused by 60-Hz hum riding on the television signal.

The Channel 2 Pickoff (CH2 PO) signal from the Channel 2 Preamplifier is applied through a low-pass filter formed by R524 and C514. The filter removes all the high-frequency components from the composite video signal, but its purpose is to specifically remove the color-burst modulation from the back-porch of the sync pulses. The filtered sync pulse is then amplified with respect to ground during its back-porch interval either by operational amplifier U514 or by operational amplifier U520, depending on the display polarity chosen by the operator. The selected comparator, when gated on (via U410A and either R410 or R411) during the back-porch interval, produces a dc-offset voltage used to shift the back-porch level of the displayed channel 2 signal to zero volts. Capacitor C522 acts as a hold capacitor to maintain a constant dc offset to the Channel 2 Vertical Preamplifier between back-porch samples. Operational amplifier U710D buffers the offset signal to the Channel 2 Preamplifier.

Offset gain of Channel 2 Preamplifier U320 is set higher when the CH2 VOLTS/DIV switch is set to 2 mV, 5 mV, 10 mV, 100 mV, or 1 V/Div. At those VOLTS/DIV settings, the FASTCLAMP bit is set LO to turn on U420E. This turns FET Q419 on and places C520 in parallel with C522 thus increasing the size of the hold capacitance. This slows down the loop response at the "more sensitive" offset gain setting of the Channel 2 Preamplifier to prevent oscillation.

CLAMP SWITCHING. The Clamp Switching circuit enables and disables the effect of the Channel 2 Vertical Display Clamp. The clamp circuit operation may be switched to provide correct clamping for either inverted or noninverted video signals.

When display clamping of the Channel 2 signal is not enabled, BCLAMPENA will be set LO, turning U420D on. The HI on the collector of U420D turns on U410B, U410C, and Q420 and turns off Q710 via U710A. Any enabling currents to offset amplifiers U514 or U520 are shunted through U410B and U410C respectively. With FET Q420 on, the input to U710D will be grounded. This disables the

Offset Buffer. With FET Q710 turned off via U710A, the offset line to the Channel 2 Vertical Preamplifier is open circuited, so no trace offsetting can occur.

When the Channel 2 Vertical Display Clamp is enabled, BCLAMPENA will be HI, turning U420D off. The LO on the collector of U420D turns Q420 off, enabling Offset Buffer Amplifier U710D to track the offset level output from the active Offset Amplifier, and the offset signal line to the Channel 2 Vertical Preamplifier is connected to the Offset Buffer by turning on Q710 via U710A.

Selection of either U514 or U520 is controlled by the CH2 INV signal and is dependent on the setting of the invert function in the associated COUPLING/INVERT menu. Since signal offsetting in the Channel 2 Preamplifier is done before the signal is inverted, offset voltages for inverted- and normal-signal displays must be of opposite polarity. Switching between these two offset amplifiers provides the required polarity change and allows the back porch of either display type to be clamped at the ground reference. Depending on the polarity of the CH2 INV (Channel 2 Invert) signal, either U410E or U410D will be on, turning off either U410B or U410C. U410B will be off when CH2 INV is HI and U410C will be off when it is LO. Bias current from the Trigger Back-Porch Clamp circuit to the offset amplifiers (U514 and U520) is not shunted away by the "off" transistor, and the offset amplifier associated with the off transistor will be biased on during the sync pulse back-porch interval.

Biasing current to enable the selected Offset Amplifier is produced during the back-porch interval when U410A (in the Trigger Back-Porch Clamp circuit) is turned off. Bias current through either R411 or R410 (depending on whether U410B or U410C is off) is supplied via R403. The other offset amplifier will be disabled since its bias current is being shunted through the "on" transistor. The amount of bias current permitted by Transconductance Amplifier U504 to the "on" amplifier provides a signal to the Channel 2 Preamplifier (after buffering by U710D) that vertically offsets the displayed signal on Channel 2.

Since the offset voltage must be maintained throughout the entire horizontal interval, capacitor C522 (and C520 in parallel if FASTCLAMP is not enabled) serves as a hold capacitor between back-porch samples. At some VOLTS/DIV settings the Channel 2 Preamplifier is set for higher offset gain. Transistor Q419 will be turned on for those settings, placing C520 in parallel with C522 to slow down the loop response. This prevents oscillation in the Channel 2 Preamplifier at the more sensitive gain settings.

Offset Buffer Amplifier U710D applies this "stored" offset level to the Channel 2 Preamplifier (via Q710), shifting the back porch of the displayed signal to near the on-screen ground reference (as set with the Vertical POSITION control).

Any time the Phase-Locked Loop is not locked (indicating that a proper TV Trigger signal is not present), the Channel 2 Vertical Display Clamp is turned off via R328 by a HI $\overline{\text{TVCLAMP}}$ signal from the PLL Unlock Detector to prevent sending invalid offsets to the Channel 2 Preamplifier. During the unlocked state of the PLL, FET Q420 is biased on to pull the input to Offset Buffer Amplifier U710D to ground, and FET Q710 is biased off via U710A (acting as an inverter to the $\overline{\text{TVCLAMP}}$ signal) to open circuit the offset signal line to the Channel 2 Preamplifier.

LOW-VOLTAGE POWER SUPPLY

The low voltages required by the scope are produced by a high-efficiency, switching power supply (diagram 22). This type of supply directly rectifies and stores charge from the ac line supply; then the stored charge is switched through a special transformer at a high rate, generating the various supply voltages.

AC Power Input

LINE SWITCHING AND LINE RECTIFIER. Ac line voltages of either 115 V or 230 V may provide the primary power for the instrument, depending on the setting of the LINE VOLTAGE SELECTOR switch S1000 (located on the instrument rear panel). POWER Switch S1350 applies the selected line voltage to the power supply rectifier (CR510).

With the selector switch in the 115 V position, the rectifier and storage capacitors C105 and C305 operate as a full-wave voltage doubler. When operating in this configuration, each capacitor is charged on opposite half cycles of the ac input, and the voltages across the two capacitors in series approximates the peak-to-peak values of the source voltage. For 230 V operation, switch S1000 connects the rectifier as a conventional bridge rectifier. Both capacitors charge on both input half cycles, and the voltage across C105 and C305 in series approximates the peak value of the rectified source voltage. For either configuration (with proper line voltage), the dc voltage supplied to the power supply inverter is the same.

SURGE PROTECTION. Thermistors RT717 and RT805 limit the surge current when the power supply is first turned on. As current warms the thermistors, their resistances decrease and have little effect on circuit operation.

Spark-gap electrodes E609 and E616 are surge voltage protectors. If excessive source voltage is applied to the instrument, the spark-gaps conduct, and the extra current quickly exceeds the rating of F1000. The fuse then opens to protect the power supply.

EMI FILTER. A sealed line filter, FL1000, is packaged with the line cord connector. It is effective in reducing noise with frequency components at and beyond 1 MHz. A differential mode filter is made up of R809, C816, R815, L715, L709, R808, R713, and C706 and is effective in reducing switch-mode noise up to 1 MHz. Resistor R1000 ensures that the capacitors in the line filter become discharged a short time after removal of the line cord so as to not present a shock hazard at the line cord connector. A combination common-mode and differential-mode filter is made up of T117, R217, R117, C218, C225, and C328. The line-rectification energy-storage capacitors (C105 and C305) also aid in the operation of this filter circuit. Resistors R410 and R400 bleed charge from the line-rectification capacitors to guarantee that they are discharged within a definite time after power is removed (turned off).

THERMAL SWITCH. Thermal Switch S1020 opens if the temperature of the power supply heatsink becomes abnormally high. High temperatures may indicate blocked ventilation holes or failed components. Opening the switch removes ac-line power from the supply to prevent any further damage from occurring. When the heatsink cools to its normal limits, the switch recloses. Opening of S1020 immediately shuts off the power supply, and the System μP does not perform its normal shutdown routine. Waveforms and front-panel settings are not saved on a thermal shutdown.

Control Power Supply

The control circuits for the power supply require a separate power supply circuit to operate. This independent power source is made up of Q148, Q240, Q836, and associated components.

Initially, when instrument power is applied, the positive plate of capacitor C244 is charged toward the value of the positive rectified-line voltage through R223. The voltage at the base of Q148 follows at a level determined by the voltage divider composed of R436, R244, CR239, R245, R640, Q836 and the load resistance placed on the supply. When the voltage across C244 reaches about +27 V, the base voltage of Q148 reaches +12.6 V and Q148 turns on, saturating Q240. The +27 V on the emitter of Q240 appears at its collector and establishes the positive voltage supply for the +12 V regulator stage formed by Q836, VR929, R245, and R640. With Q240 on, R244 is placed in parallel with R436 and both Q148 and Q240 remain saturated.

The +27 V level begins to drain down as the +12 V Regulator draws charge from C244. If the main power supply doesn't start (and thus recharge C244 via T335 and CR245) by the time the voltage across C244 reaches about +14 V, Q240 turns off. With Q240 off, resistor R244 pulls the base of Q148 low and turns it off also. (Capacitor C244 would only discharge low enough to turn off the transistors under a fault condition.) In this event, C244 would then charge again to +27 V, and the start sequence would repeat. Normally, the main power converter is delivering adequate power before the +14 V level is reached, and the current drawn through T335 via Q421 and Q423 induces a current in the secondary winding of T335 that charges C244 positive via diode CR245. The turns ratio of T335 sets the secondary voltage to approximately +17 V and, as long as the supply is being properly regulated, C244 is charged to that level and held there.

Power Conversion

The power converter consists of a buck-type switching Preregulator, producing width-regulated voltage pulses that are filtered to produce a preregulated dc current, and an Inverter stage that chops this preregulated current into ac to drive a power transformer. The transformer has output windings that provide multiple unregulated dc voltages after rectification has taken place. The main Preregulator components are Q421, Q423, CR426, C328, T335, T620, and U233. The fundamental Inverter components are Q521, Q721, T639, and U829B (see Figure 3-15).

PREREGULATOR. The Preregulator control circuit monitors the drive voltage reflected from the secondary to the primary of the Inverter output transformer T639 and holds it at the level that produces proper supply voltages at each of the secondary windings.

The Preregulator control circuit consists primarily of control IC U233, gate drive transformer T620, and the associated bias and feedback circuit elements. The voltage at the primary center tap of T639 is attenuated and applied to the voltage-sense input of control IC U233. This IC varies the "on time" of a series switch, depending on whether the sensed voltage is too high or too low. Transistors Q421 and Q423 form this "series switch," and are each active during alternate switching cycles. The on-time duty cycle of the series switch is inversely proportional to the rectified line voltage on C328. In normal operation, the series switch is on about one-half of the time. When the series switch is off, current to T639 is through CR426.

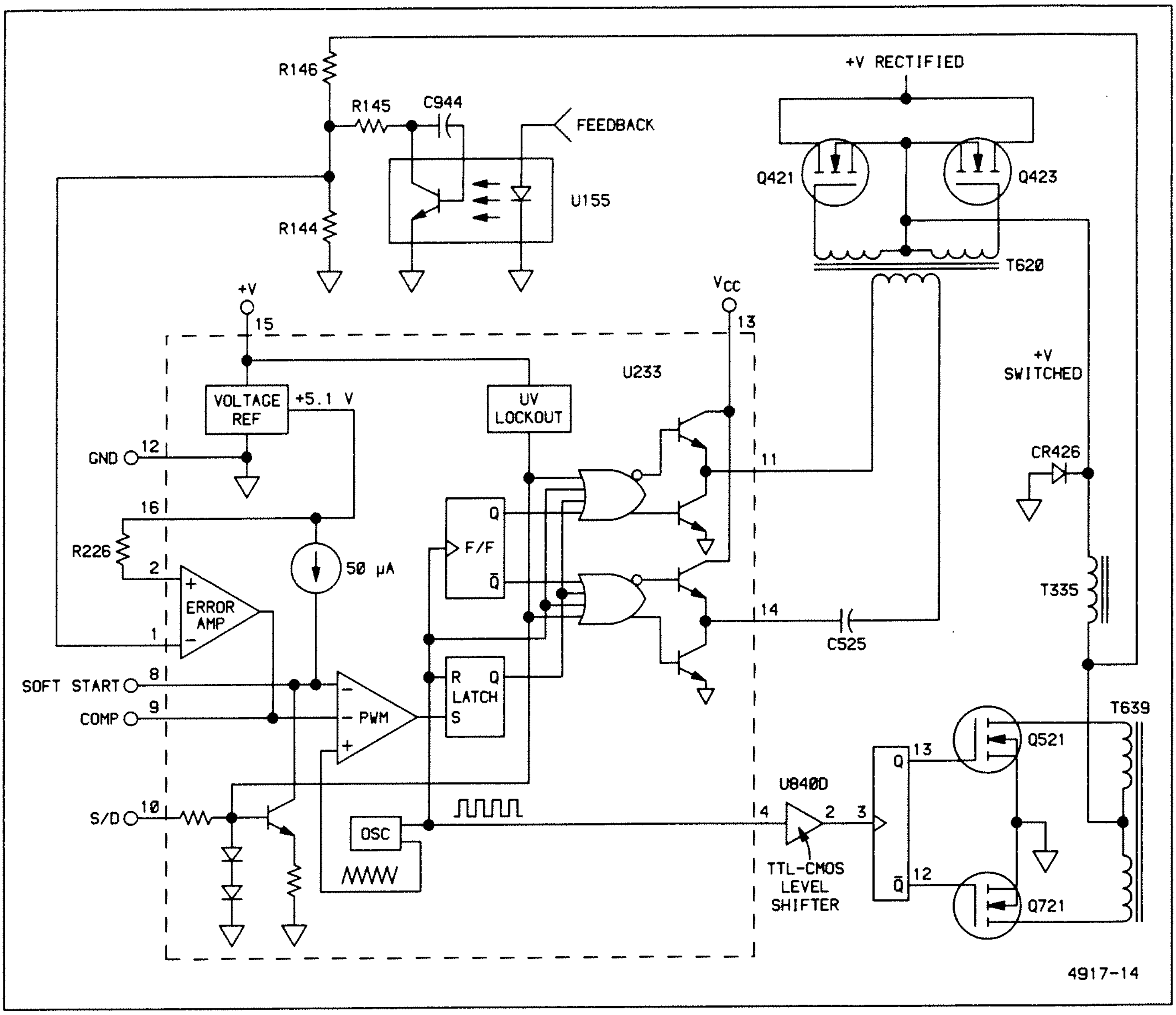

Figure 3-15. PWM Regulator and Inverter.

PREREGULATOR START-UP. As the supply for the Preregulator control IC is established, an internal oscillator begins to run. The oscillator generates a repetitive triangular wave (as shown in Figure 3-16) at a frequency determined primarily by R228 and C227 (with R227 having a minor effect since it controls the discharge time of timing capacitor C227).

As the control power supply turns on, a 50 μA current source internal to U233 begins to charge capacitor C128 positive. This charging level, applied to one of the negative inputs of the PWM comparator, allows drive pulses of greater and greater duty cycle to be generated. These pulses drive the series switching transistors (Q421 and Q423), and their slow progression from narrow to wide causes the various secondary supplies to gradually build up to their final operating levels. This slow buildup prevents a turn-on current surge that would cause the current-limit circuitry to shut down the supply.

PREREGULATION. Once the initial charging at power-up is accomplished (as just described), the voltage-sensing circuitry begins controlling the Inverter switching action. The voltage level at the primary center tap of T639 is divided by sense string R146-R144, and the resulting voltage is applied to the error amplifier internal to U233 at pin 1. The +5.1 V reference generated by U233 is applied to pin 2 of U233, the other input of the error amplifier. If the sensed level at pin 1 is lower than the reference level at pin 2 (as it always is for the first few switching cycles), the output of the error amplifier is high. This high level is applied to a negative input of the PWM comparator; the other negative input is applied from the soft-start capacitor (described previously).

The lower of the two negative input levels determines the actual negative comparison point of the PWM comparator; and this level determines the point at which the positive-going ramp, applied to the positive input, switches the PWM comparator to initiate the off state of the PWM switch. The PWM series switch is turned on at the beginning of each clock cycle; turn-off occurs when the positive-going ramp crosses the threshold level of the PWM comparator. The lower the level at the controlling (negative) input, the shorter the PWM switch "on time." Depending on the output level sensed, the duty cycle of the drive signal changes (sensed level rises or falls with respect to the triangular waveform applied to the positive PWM comparator input) to hold the secondary supplies at their proper levels.

Optoisolator U155 and resistor R145 form a control network that allows a voltage sensed at the FEEDBACK input to slightly alter the voltage-sense reference applied to pin 1 of U233. The FEEDBACK signal is generated by the +5 V Inverter Feedback amplifier (U189, diagram 23) and is directly related to the level of the +5 V_D supply line. If the FEEDBACK signal goes above its nominal level (+5 V_D is too low), base drive to the shunt transistor (in optoisolator U155) increases. This increase causes additional current to be shunted around R144 (via R145 and phototransistor of U155) and changes the ratio of the sensing divider. The voltage at the center tap of T639 must increase to balance out the changed sense ratio and maintain balance in the error amplifier. Since the output of the error amplifier controls the current to the primary winding of the output transformer, and since the error amplifier sensing depends on a balanced condition, the voltage at the transformer primary increases.

With a higher current applied to the transformer primary, higher voltages appear across the secondary windings of T639 with each cycle. This causes the secondary voltages to return to their nominal levels. As the +5 V_D line returns to its nominal level, base drive to the shunt transistor stabilizes at a level that keeps the sensed +5 V_D level in regulation. Should the FEEDBACK signal level tend too high, opposite control responses occur. Further information about the FEEDBACK signal is given in the +5 V Inverter Feedback description.

INVERTER. The Inverter circuit alternately switches current through each leg of the primary winding of output transformer T639. The circuit is made up of Q521, Q721, U840D, U829B, and associated components.

A clock pulse from U233 is applied to a TTL-CMOS level shifting buffer (U840D) at the beginning of every switching cycle. The level-shifted clock pulse at the output of U840 clocks U829B, a CMOS D-type flip-flop (configured to toggle with each clock). The Inverter switch transistors, Q521 and Q721, are alternately turned on and off by the flip-flop outputs and are connected to opposite ends of the primary winding of the output transformer. Driving the inverter switches in alternate fashion produces ac currents in the secondary windings of the output transformer that are rectified, providing the various unregulated dc supply voltages.

Primary Fault Sensing

Primary current, primary regulated voltage, and primary unregulated voltage are monitored by circuitry to prevent catastrophic failure. Should conditions arise that cause an excessive primary current or an excessive primary regulated voltage, limiting occurs. The excessive primary current and primary regulated voltage functions share much common circuitry, while the low unregulated primary voltage circuitry is entirely independent of the first two fault-sensing circuits.

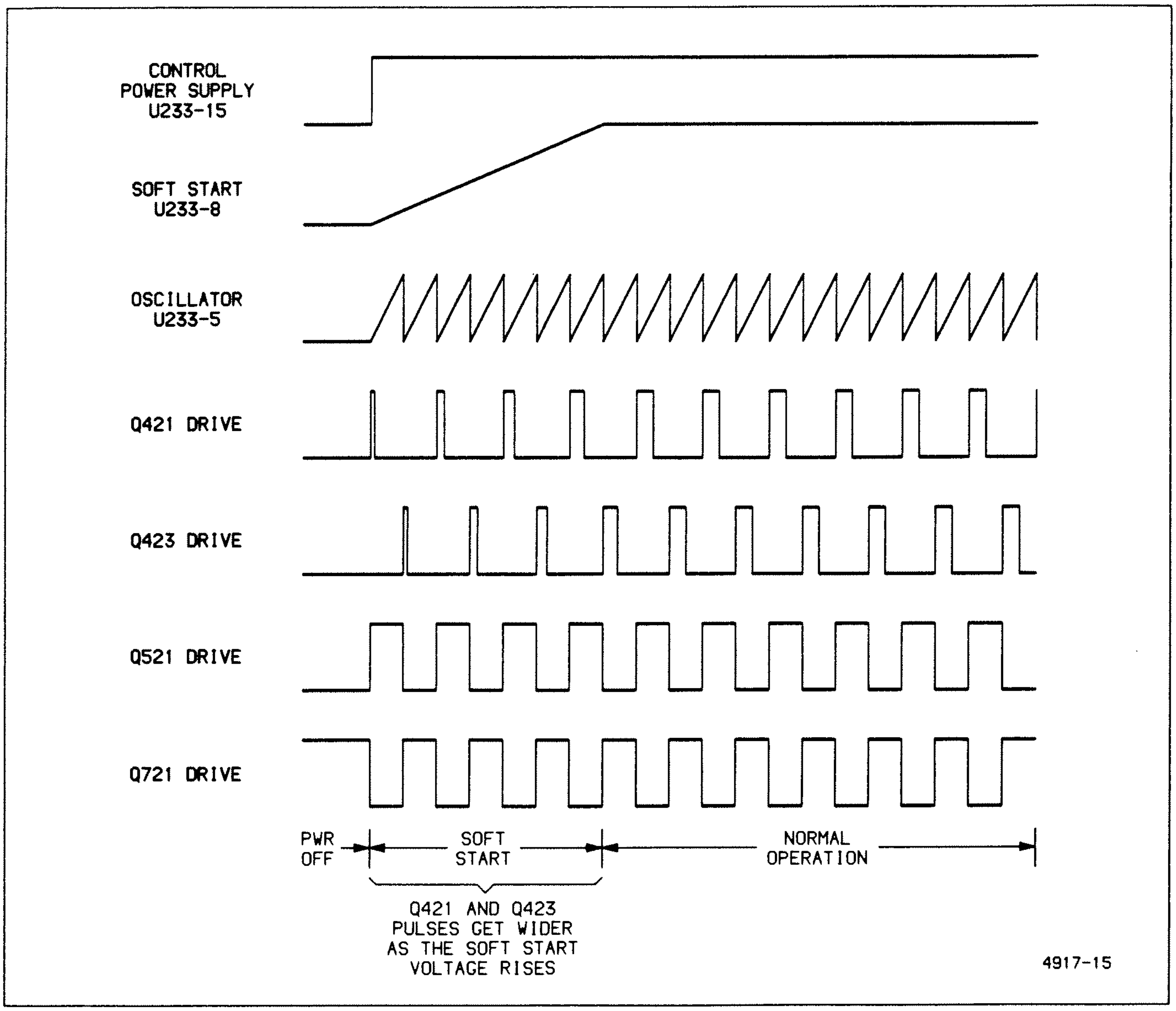

Figure 3-16. PWM switching waveforms.

PRIMARY OVER-CURRENT SENSING. The primary current of T639 through R727 produces a voltage signal that is filtered by R728 and C728 to remove high-frequency switching spikes. The filtered signal is applied to the inverting input of U840C. The noninverting input of the comparator is set at a level defined by the +5.1 V reference from U233 and voltage divider R935-R836. If an excessive-current condition exists (to the point that the inverting input of U840C goes more positive than the noninverting input), the comparator output goes low. The open-collector output of the comparator is "wire-ORed" with the open-collector output of the regulated primary over-voltage comparator (U840B) and drives U840A, connected as an inverting buffer. Buffer U840A drives the clock input of a CMOS flip-flop in U829, configured as a monostable flip-flop, used to shut down supply operation.

PRIMARY OVER-VOLTAGE SENSING. The regulated primary voltage is sensed by the voltage divider R129-R128, with C528 providing low-pass filtering to remove high-frequency switching spikes. The attenuated signal is applied to comparator U840B at the inverting input, while the noninverting input is connected to the +5.1 V reference from U233. Should the regulated primary voltage become high enough to raise the inverting input of the comparator more positive than the noninverting input, the comparator output goes to a low level. As previously stated, the output of this comparator is wire-ORed to the output of U840C and drives an inverting clock buffer U840A. This buffer in turn drives the clock input of the monostable flip-flop circuit used to shut down supply operation.

SHUTDOWN TIMER. The Shutdown Timer ensures that the preregulator series switch remains off long enough for energy stored in C128 (the soft-start capacitor) and C244 (the Control Power Supply energy-storage capacitor) to drain down via normal circuit loading should an over-current or over-voltage fault occur. Shutdown of the series switch (Q421 and Q423) occurs when the S/D (shutdown) input (pin 10) of U233 goes high. The Shutdown Timer, made up of U829A, R824, C829, R934, CR730, and CR824, controls this input.

Prior to being clocked, U829A (configured as a monostable flip-flop) is in a reset state with its Q output set low. This is the normal operating mode and allows the series switch to be controlled by the regulating functions of U233. Capacitor C829 charges to the Control Power Supply voltage via R824 and CR824 (diode CR824 shunts R934 when charging C829 to provide a relatively fast charging path). When the flip-flop is clocked (indicating a fault-sense from the voltage- or current-sense circuits), the Q output goes high and C829 begins to discharge. With Q high, CR824 becomes reverse biased so that discharge of C829 is through R934, providing a relatively slow discharge compared to the charging time. This ensures that the Q output of U829A is held high long enough for soft-start capacitor C128 and Control Power Supply capacitor C244 to fully discharge.

The high Q output of U829A, connected to the shutdown input to U233, turns off the PWM switch (Q421 and Q423) immediately and keeps it off until Q returns low (when the Control Power Supply decays and turns U829 off). However, the PWM clock continues to run and the Inverter switches (Q521 and Q721) continue to operate. Since the PWM switch is not operating, energy is not transferred to the Control Power Supply via T335, and C244 discharges below the minimum voltage level required by the Control Power Supply circuit (through the normal circuit load). When this minimum level is reached, the Control Power Supply regulator disconnects from C244, interrupting the power to the control circuitry and stopping the Inverter switches.

Monostable U829A is designed to remain active long enough for the Control Power supply to decay and disconnect. The disconnect level is approximately half of the Control Power Supply voltage and, once disconnected, supply voltage is reestablished in 0.5 to 2 seconds. The time it takes C244 to charge from the "disconnect threshold" to the Control Power Supply "turn-on threshold" is the dominate factor in determining the power supply restarting time when recovering from an over-current or over-voltage fault condition.

Capacitor C829 is once again charged through R824 and CR824 with a relatively short time constant, allowing U829A to be triggered again (if the fault persists) by the time the Control Power Supply restarts.

LINE UP. The Line Up circuit, composed of U834B, U265, and associated components, senses the level of the rectified line voltage and relays its status through the PWRUP circuit to the System μP. The signal from voltage divider R325-R835 is low-pass filtered by C835 and is applied to the inverting input of comparator U834B. The noninverting input of the comparator is referenced to the +5.1 V reference from U233. The output of the comparator drives the light-emitting diode of optoisolator U265, so whenever the rectified line-input voltage is below the normal operating level (approximately +178 V), the light-emitting diode (LED) is off. With the LED off, the output phototransistor of U265 is biased off.

At instrument turn-on, after the rectified line voltage comes up, the control power supply begins supplying power to the control circuitry. At that time, the output of comparator U834 goes LO at pin 7 to turn on the LED in optoisolator U265. This action biases on the output transistor of the optoisolator and switches the LINE UP signal HI. Through the PWRUP signal circuitry, a HI LINE UP signal tells the System μP that ample line voltage is available for normal instrument operation.

When instrument power is turned off, the rectified line voltage begins dropping. At about 178 V, comparator U834 switches off the LED in U264, and the LINE UP signal goes LO. A LO output tells the System μP that power is dropping, and the μP begins shutting the instrument down in an orderly fashion before the secondary voltages go out of regulation.

Line Trigger

The Line Trigger circuit, made up of T415, U170A, and the associated components, provides a representation of the input line signal to the Trigger stage that is isolated from the power-line environment.

Since resistors R516 and R518 are large compared to the impedance of the primary winding in T415, the transformer operates in a current-driven mode. The secondary winding of T415 is connected to a transresistance amplifier stage consisting of U170A, C483, and R483. This amplifier presents a very low impedance to the output of the transformer and maintains the integrity of the line voltage signal representation. Capacitor C483 provides a negative-feedback path to high frequencies (relative to 60 Hz) and reduces noise on the line-frequency signal. The output of the transresistance amplifier drives the oscilloscope trigger circuitry.

Rectifiers

The Rectifiers convert the alternating currents from the secondary windings of the Inverter output transformer to the various unregulated dc voltages required by the instrument. Rectification is done by conventional diode rectifier circuits, and filtering is done by conventional LC networks.

LOW-VOLTAGE REGULATORS

The Low-Voltage Regulators (diagram 23) remove ac voltage noise and ripple from the various unregulated dc supply voltages. Each regulator output is automatically current limited if the output current exceeds the requirements of a normally functioning instrument. This limiting prevents any further component damage.

+10 V and −5 V References

Each of the power supply regulators controls its respective output by comparing the output voltage to a known reference level. In order to maintain a stable supply voltage, the reference voltage must itself be highly stable. The circuit composed of U180, U170B, U900, and associated components produces the two reference levels used by the regulator circuits.

Resistor R556 and capacitor C664 form an RC filter network that smooths the unregulated +15 V_A supply before it is applied to voltage-reference IC U180. The +10 volt output from pin 6 of U180 feeds a low-pass filter composed of R900 and C900. The output of this filter in turn feeds unity-gain buffer amplifier U900, the output of which is the source of the +10 V reference used by the various positive regulators. Low-pass filter R900-C900 provides filtering for the IC voltage reference and provides for a well-defined voltage rise of the +10 V_{REF} voltage at power-up.

Operational amplifier U170B and its associated components make up a −5 V Reference circuit used as the reference for the negative regulators. It is configured as an inverting amplifier with a gain of 1/2 and converts the +10 V_{REF} input to a precision −5 V_{REF} output.

+15 V Regulator

The +15 V Regulator uses three-terminal regulator U579 and operational amplifier U570A (arranged as the voltage sensor) to achieve regulation of the +15 V supply). The three-terminal regulator holds its output voltage on pin 2 at 1.25 V more positive than the reference input level applied to pin 1. The voltage at the reference pin is established by current in diode CR575 and is controlled by voltage sensor U570A.

Resistors R576 and R575 at the regulator output divide the +15 V level down for comparison to the +10 V reference applied to pin 3 of operational amplifier U570A. At initial power up, when the input voltage at pin 2 (from the divider) is lower than the +10 V reference, the output of amplifier U570A is high, and the output voltage is allowed to rise. As the regulator output reaches +15 V, the amplifier begins sinking current away from the reference pin of the three-terminal regulator via diode CR575. This sets the voltage on the reference pin at its nominal level and holds the output at +15 volts.

Current limiting for the +15 V supply is provided by the internal circuitry of the three-terminal regulator. Diodes CR576 and CR583 protect U570A from transient voltage reversals.

+8 V Regulator

The +8 V Regulator is composed of Q465, Q479, U470A, U470B, and the associated components. The circuit regulates the voltage and limits the supply current.

Initially, as power is applied, the voltage at pin 6 of U470B via R476 is lower than the +8 V reference level applied to pin 5 via divider R465 and R466. The output of U470B is forced HI, reverse biasing diode CR466. With CR466 (and CR465) off, all the current through R565 is supplied as base current to Q465, turning it on. This turns on the pass transistor Q479 at maximum current. This current charges up the various loads on the supply line and the output level moves positive.

As the regulator output rises toward +8 V, this positive-going voltage is applied to the inverting input of U470B through R476. When the output voltage reaches +8 V, the inverting input equals the reference at the noninverting input set by R465 and R466. Then, the output at pin 7 of U470B goes negative, forward biasing diode CR466 and shunting base-drive current away from Q465. This reduces the currents through Q465 and Q479 to levels that maintain a +8 V output. Since base drive source for Q465 is the +15 V supply, via R565, proper relative polarity between the two supplies is assured (preventing component damage in case of a failure on the +15 V supply line).

The over-current limiting circuit is of foldback design and is performed by operational amplifier U470A and its associated components. Under normal current demand conditions, the output of U470A is HI, keeping diode CR465 reverse biased. If the regulator output current exceeds approximately 1.3 A (as it might if a component fails), the voltage drop across R473 (added onto the +8 V output voltage) causes the inverting input of U470A to exceed the +8 V level at the noninverting input, and the output at pin 1 will go LO. This forward biases diode CR465 and reduces the forward bias on Q465 and thereby decreases the bias current to Q479. This in turn reduces the regulator output current through Q479 to decrease the output voltage. As the output voltage drops (applied to U470A pin 3), the output current required to cause limiting also decreases, causing both voltage and current to drop to low values as Q465 becomes biased off.

Pin 2 of U470A is pulled down through R477 to the $-8\ V_A$ supply so that the output of the foldback circuit becomes immediately HI at power-on. This initial HI holds CR465 biased off thereby preventing a false overcurrent sense and subsequent latchup at start-up as the +8 V regulated output seen on pin 3 of U470A rises from zero volts to its normal operating level.

+5 V Regulator

Regulation of the +5 V supply is provided by a circuit similar to that of the +8 V Regulator. As long as the relative polarity between the +8 V supply and the +5 V supply is maintained, base drive to Q870 is supplied through R864. The current through Q870 provides base drive for the series-pass transistor Q879.

When voltage-sense amplifier U870B detects that the +5 V remote-sense voltage has reached +5 V, it begins shunting base-drive current away from Q870 via diode CR866 and holds the output voltage constant.

Current limiting for the +5 V supply is done by U870A and associated components. Under normal current demand conditions, the output of U870A is high and diode CR865 is reverse biased. However, should the current through current-sense resistor R873 reach approximately 3 amperes, the voltage developed across R873 (added to the regulated +5 V output) raises the voltage at pin 2 of U870A (via divider R876 and R875) to a level equal to that at pin 3. This causes the output of U870A to go low, forward biasing CR865. Base drive current is then shunted away from Q870, and the output current in Q879 is reduced. Resistor R874 allows the supply to maintain regulation with the remote-sense line disconnected. Resistors R885 and R886 provide enough initial current to the load to prevent an excessive-current latchup of U470A as the power comes up.

−15 V Regulator

Operation of the −15 V Regulator, composed of U679, U570B and their associated components, is similar to that of the +15 V Regulator already described. The regulator is referenced to −5 V to allow sensing of the negative output level. Zener diode VR870 allows operational amplifier U570B to operate in its active region. Capacitor C873 is a speed-up capacitor that allows the regulator to respond more quickly to current surges and other transients and provides filtering of zener noise produced by VR870.

−8 V Regulator

Operation of the −8 V regulator is nearly identical to that of the +8 V Regulator, except that it is referenced to −5 V to allow sensing of negative voltages. Zener diode VR380 allows operational amplifiers U270A and U270B to operate in their linear regions.

The −8 V Sense input provides for remote sensing of the supply level on the Main board where regulation is the most critical. Since the −8 V level is remotely sensed, the IR drop caused by the impedance in the supply bus lines going to the main board and a small series resistor in the line (R121 on the Main board) causes the actual output level from the supply regulator to be closer to −8.4 V. (This is the voltage actually required by some of the −8 V load circuits.) Resistor R388 allows the supply to maintain regulation with the remote sense line disconnected. Current limiting of the combined −8 V and −8.3 V supplies occurs at about 3 amperes.

−5 V Regulator

Operation of the −5 V Regulator is similar to that of the +5 V Regulator. Current limiting of the −5 V supply occurs at about 3.1 amperes.

+5 V Inverter Feedback

Operational amplifier U189 and associated components are configured as a frequency-compensated voltage-sensing network. The circuit monitors the +5 V digital power supply line from the rectifiers and provides feedback to the Preregulator Control IC (U233) via optoisolator U155 (both on diagram 22). The feedback is used to trim the +5 V_D level by controlling the Preregulator. The FEEDBACK signal slightly varies the voltage to the Inverter output transformer and holds the output of the 5 V secondary windings at an optimum level. Output levels of the other secondary windings are related by turns ratio to the +5 V_D level and are also held at their optimum levels. This technique minimizes power losses in the series-pass transistors and increases regulator reliability.

Power-Up

The Power-Up circuit, composed of U189A, Q295 and the associated components, provides buffering and level shifting of the LINE UP signal to the System Processor.

Operational amplifier U189A is configured as a comparator referenced to +10 V_{REF}. When adequate power-line input voltage is available, the LINE UP signal will be HI. The output of the comparator will be LO, turning off transistor Q295. This results in a HI PWRUP signal to the System μP, indicating that the power supplies are stable. When adequate power-line voltage is not available, the LINE UP signal from the Preregulator circuit goes LO, the output level of U189A goes HI and turns Q295 on, resulting in a LO PWRUP signal to the System μP. This indicates that the various supply voltages may go out of regulation in about 10 ms.

Capacitor C195 provides a negative-feedback path for high-frequency signals and stabilizes operation of U189A.

DC-OK Sense

The output of the DC-OK Sense circuit is checked by the System Processor after it receives the PWR UP signal to verify that power supply voltages are within tolerance.

By itself, the resistive summing network made up of R794, R795, R797, R686, R688 and R796 would produce a voltage near zero volts if all supplies were within tolerance. This voltage may vary ±0.19 V, depending on slight variations in the individual supply output levels. The current in resistor R396 is, however, added into the summing node and shifts its operating point approximately 0.19 V positive.

The resulting voltage is compared to ground by comparator U395B and to +0.37 V by comparator U395A, establishing the tolerance window. Both open-collector outputs of the comparator are off, and the DCOK signal is HI, as long as the summing-node voltage falls within this window. Should the summing-node voltage exceed either limit, the associated comparator turns on its output transistor and pulls the DCOK signal LO, indicating that at least one of the power supplies is not operating properly.