Tektronix®
COMMITTED TO EXCELLENCE

5223 Option 10 (GPIB) DIGITIZING OSCILLOSCOPE

SERVICE

For Qualified Service Personnel Only.

INSTRUCTION MANUAL

Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THIS MANUAL CONTAINS SERVICING INSTRUCTIONS FOR USE BY QUALIFIED SERVICE PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING UNLESS YOU ARE QUALIFIED TO DO SO.

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LIST OF TABLES

SAFETY SUMMARY

The general safety information contained in this summary is for servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL


Static-Sensitive Devices.

This symbol indicates where applicable cautionary or other information is to be found.

AS MARKED ON EQUIPMENT


DANGER—High voltage.


Protective ground (earth) terminal.


ATTENTION—refer to manual.

WARNINGS

POWER SOURCE

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product. Use only a power cord that is in good condition.

For detailed information on power cords, refer to Section 1 General Information.

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating), can render an electric shock.

USE THE PROPER FUSE

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating, and current rating.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

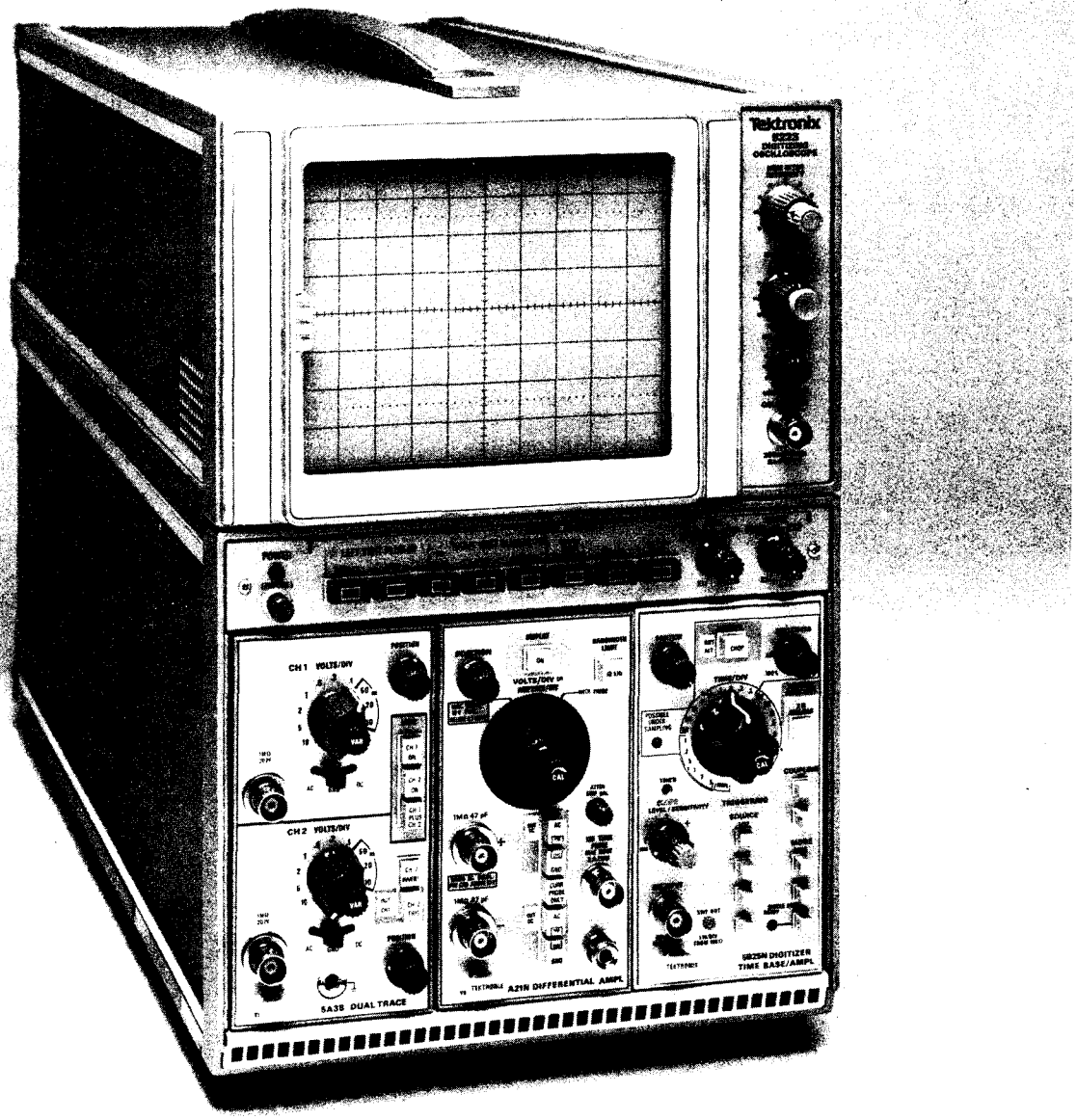
Disconnect power before removing protective panels, soldering, or replacing components.

CRT HANDLING

Use care when handling a crt. Breakage of the crt causes a high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses should be worn. Avoid striking the crt on any object which might cause it to crack or implode. When storing a crt, place it in a protective carton or set it face down in a protected location on a smooth surface with a soft mat under the faceplate.

SILICONE GREASE HANDLING

Handle silicone grease with care. Avoid getting the silicone grease in your eyes. Wash hands thoroughly after use.



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5223 DESCRIPTION

The TEKTRONIX 5223 Digitizing Oscilloscope is a digital storage instrument with a real-time bandwidth of 10 megahertz. The 5223 is capable of displaying real-time and stored waveforms simultaneously (four real-time waveforms and four stored waveforms, if dual channel amplifier units are used); the real-time waveforms need not be related to the stored waveforms. Stored waveforms can be expanded vertically and horizontally by a factor of 10, using front-panel controls. The left and right stored vertical signals can be displayed against each other in the X-Y mode, using the L VS R front-panel display function. The roll mode is useful when viewing low-frequency signals. Rear-panel connectors provide access to the internal analog and controls signals to record stored waveforms using associated equipment (i.e., X-Y plotter). The 5223 accepts most 5000-series plug-in units; the flexibility of the plug-in feature, and variety of plug-in units available, allows the system to be used for many measurement applications.

In addition, the 5223 Option 10 allows remote programming of the 5223 MEMORY CONTENTS switches, and the transfer of waveform data between the 5223 and other GPIB compatible instruments.

GENERAL INFORMATION

This section contains a basic content description of both the Operators and Service manuals, information on instrument installation, power requirements, packaging for shipment, instrument conversion, rackmount information and specifications. The specification portion consists of three tables; Electrical, Environmental, and Physical Characteristics.

A Standard Accessories list and full-page instrument dimensional drawing of both the bench and rackmount models are also contained in this section.

OPERATORS MANUAL

The Operators Manual is divided into the following four sections:

Section 1—General Information contains instrument description, electrical specifications, environmental characteristics, standard accessories, installation, and packaging for shipment instructions.

Section 2—Operating Instructions contain information relative to operating and checking the instrument operation.

Section 3—GPIB Information contains instructions and descriptions of the GPIB commands used by the 5223 Option 10.

Section 4—Applications contains information useful in making basic oscilloscope measurements.

Section 5—Instrument Options contains a description of available options and gives the location of the incorporated information for those options.

SERVICE MANUAL

WARNING

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Section 1—General Information, Section 2—Operating Instructions, and Section 3—GPIB Information contain information which is covered in the Operators Manual.

Section 4—Theory of Operation contains basic and general circuit analysis that may be useful for servicing or operating the instrument.

Section 5—Maintenance provides conventional troubleshooting charts, signature analysis based troubleshooting routines, and maintenance procedures with detailed instructions for replacing assemblies, subassemblies and individual components.

Section 6—Calibration contains procedures to check the operational performance and electrical characteristics of the instrument. Procedures also include methods for adjustment of the instrument to meet specifications.

Section 7—Instrument Options contains a description of available options and locations of incorporated information for those options.

Section 8—Replaceable Electrical Parts contains information necessary to order replaceable parts and assemblies related to the electrical functions of the instrument.

Section 9—Diagrams and Circuit Board Illustrations includes detailed circuit schematics, locations of assembled boards within the instrument, voltage and waveform information, circuit board component locators, and locations of adjustments to aid in performing the Adjustment and Performance Check portion of the Calibration procedure.

Section 10—Replaceable Mechanical Parts includes information necessary to order replaceable mechanical parts and shows exploded drawings which identify assemblies.

INSTALLATION

INITIAL INSPECTION

This instrument was inspected both mechanically and electrically before shipment. It should be free of mars or scratches and should meet or exceed all electrical specifications. To confirm this, inspect the instrument for physical damage incurred in transit and test the electrical performance by following the Checkout Procedure in Section 2, Operating Instructions. Verify Performance Requirements by referring to the Calibration section of this manual. If there is damage or deficiency, contact your local Tektronix Field Office representative.

POWER CORD INFORMATION

WARNING

AC POWER SOURCE AND CONNECTION. This instrument operates from a single-phase power source. It has a three-wire power cord and a two-pole, three-terminal grounding-type plug. The voltage to ground (earth) from either pole of the power source must not exceed the maximum rated operating voltage, 250 volts.

Before making connection to the power source, determine that the instrument is adjusted to match the voltage of the power source (see Fig. 1-2), and has a suitable two-pole, three-terminal grounding-type plug. Refer any changes to qualified service personnel.

GROUNDING. This instrument is safety class I equipment (IEC designation). All accessible conductive parts are directly connected through the grounding conductor of the power cord to the grounding contact of the power plug.

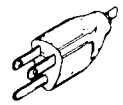
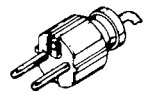
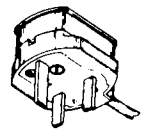
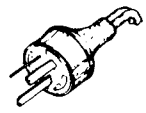
WARNING

The power input plug must only be inserted in a mating receptacle with a grounding contact. Do not defeat the grounding connection. Any interruption of the grounding connection can create an electric shock hazard.

For electric shock protection, the grounding connection must be made before making connection to the instrument's input or output terminals.

TABLE 1-1
Power-Cord Conductor Identification

Conductor	Color	Alternate Color
Ungrounded (Line)	Brown	Black
Grounded (Neutral)	Blue	White
Protective Grounding (Earthing)	Green-Yellow	Green-Yellow

Plug Configuration	Usage	Nominal Line-Voltage (AC)	Reference Standards	Option #
	North American 120V/15A	120 V	[1]ANSI C73.11 [2]NEMA 5-15-P [3]IEC 83	STANDARD
	Universal Euro 250V/10-16A	240 V	[4]CEE (7), II, IV, VII [3]IEC 83	A1
	UK 240V/13A	240 V	[5]BS 1363 [3]IEC 83	A2
	Australian 240V/10A	240 V	[6]AS C112	A3
	North American 240V/15A	240 V	[1]ANSI C73.20 [2]NEMA 6-15-P [3]IEC 83	A4

[1]ANSI—American National Standards Institute
[2]NEMA—National Electrical Manufacturer's Association
[3]IEC—International Electrotechnical Commission
[4]CEE—International Commission on Rules for the Approval of Electrical Equipment
[5]BS—British Standards Institution
[6]AS—Standards Association of Australia

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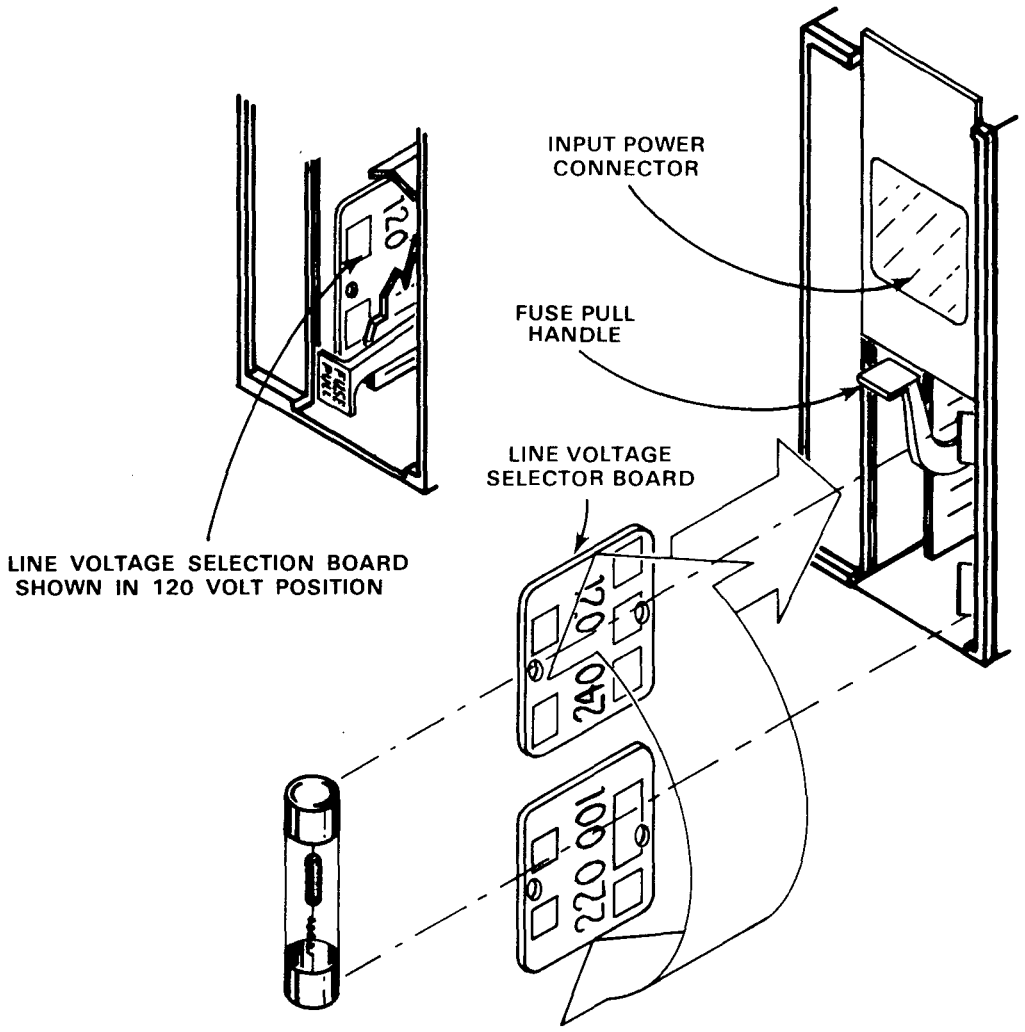
Figure 1-1. Power cord and plug identification information.



Line Voltage Selection/Fuse Replacement Procedure

1. Disconnect input power cable from instrument.
2. Slide plastic fuse cover up over power cord connector area.
3. Pull out on FUSE PULL handle and remove fuse.
4. Insert a scribe into the hole in the Line Voltage Selector Board and remove.
5. Position Line Voltage Selector Board for desired operation voltage (selected operating voltage range will be displayed at top of Line Voltage Selector Board whene installed. See drawing above).
6. Push Line Voltage Selector Board firmly into Input Power Connector slot.
7. Return FUSE PULL handle to normal position.
8. See table on instrument rear panel. To select proper fuse and install in fuse holder.
9. Slide plastic fuse cover over fuse area.
10. Connect line power cord to instrument.
11. Set POWER switch to ON.

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Figure 1-2. Line voltage range selection.

The power-cord plug required depends upon the ac input voltage and the country in which the instrument is to be used. Should you require a power-cord plug other than that supplied with your instrument, refer to the Reference Standards listed in Figure 1-1.

LINE VOLTAGE AND REGULATING-RANGE SELECTION

CAUTION

To prevent damage to the instrument, always check the Line Voltage Selector Board (see Fig. 1-2) located on the rear of the instrument before connecting the instrument to the supply circuit.

The Line Voltage Selector Board allows selection of four line voltage ranges. To convert from one range to another, change the power cord and plug to match the power-source receptacle, then insert a scribe into the hole in the Line Voltage Selector Board and remove. Select the desired voltage range using the table printed on the rear of the instrument and insert the line voltage selector Board as shown in Figure 1-2.

OPERATING TEMPERATURE

The 5223 can be operated where the ambient air temperature is between 0° and +50° C and can be stored in ambient temperatures from −55° to +75° C. After storage at temperatures outside the operating limits, allow the chassis temperature to reach a safe operating limit before applying power.

The 5223 is cooled by air exhausted by the fan and drawn in through holes in the side, and bottom panels; additional air is drawn in through the top panel in the rackmount configuration. To ensure proper cooling of the instrument, maintain the clearance provided by the feet on the bottom and allow at least 2 inches clearance (more if possible) at the top, sides, and rear of the instrument.

OPERATING POSITION

A stand, mounted on the bottom of the instrument, permits the instrument to be tilted up about 10° for more convenient crt viewing.

INSTRUMENT DIMENSIONS

A drawing showing the major bench model and rackmount model dimensions of the instrument is shown in Figure 1-3 and 1-4.

PACKAGING FOR SHIPMENT

If this instrument is to be shipped for long distances by commercial transportation, it is recommended that the instrument be packaged in the original manner. The carton and packaging material in which your instrument was shipped should be saved and used for this purpose.

Also, if this instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the following: Owner of the instrument (with address), the name of a person at your firm who can be contacted, complete instrument type and serial number, and a description of the service required.

If the original packaging is unfit for use or not available, package the instrument as follows:

1. Obtain a corrugated cardboard shipping carton having inside dimensions at least six inches greater than the instrument dimensions; refer to Table 1-2 for carton test srength requirements.

TABLE 1-2
Shipping Carton Test Strength

Gross Weight (lb)	Carton Test Strength (lb)
0-10	200
10-30	275
30-120	375
120-140	500

2. Enclose the instrument with polyethylene sheeting or equivalent to protect the finish of the instrument.

3. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing three inches on each side.

4. Seal the carton with shipping tape or with an industrial stapler.

5. Mark the address of the Tektronix Service Center and your return address on the carton in one or more prominent locations.

PANEL COVER REMOVAL

WARNING

Dangerous potentials exist at several points throughout the oscilloscope. When the instrument must be operated with the cabinet panels removed, do not touch exposed connections or components. Some transistors have voltage present on their cases. To prevent shock hazard disconnect power before cleaning the instrument or replacing parts.

The panel covers are held in place by fasteners on the rear of the instrument. To remove the panel covers loosen the screws and rotate the fasteners so that the

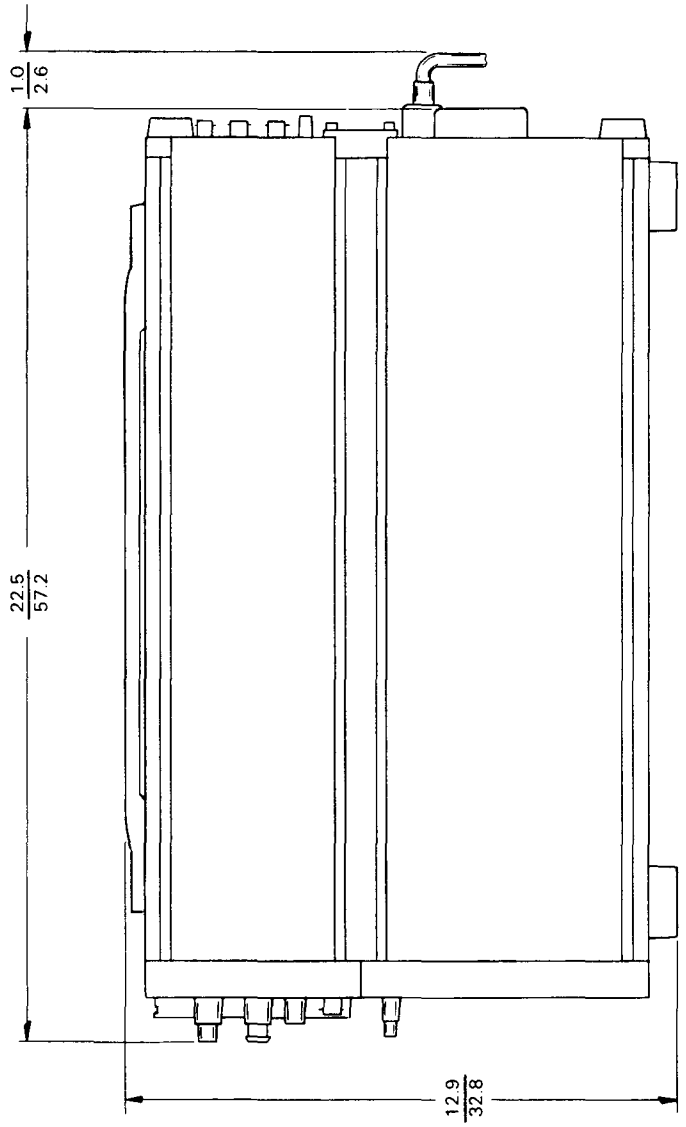

Figure 1-3. 5223 dimensional drawing.

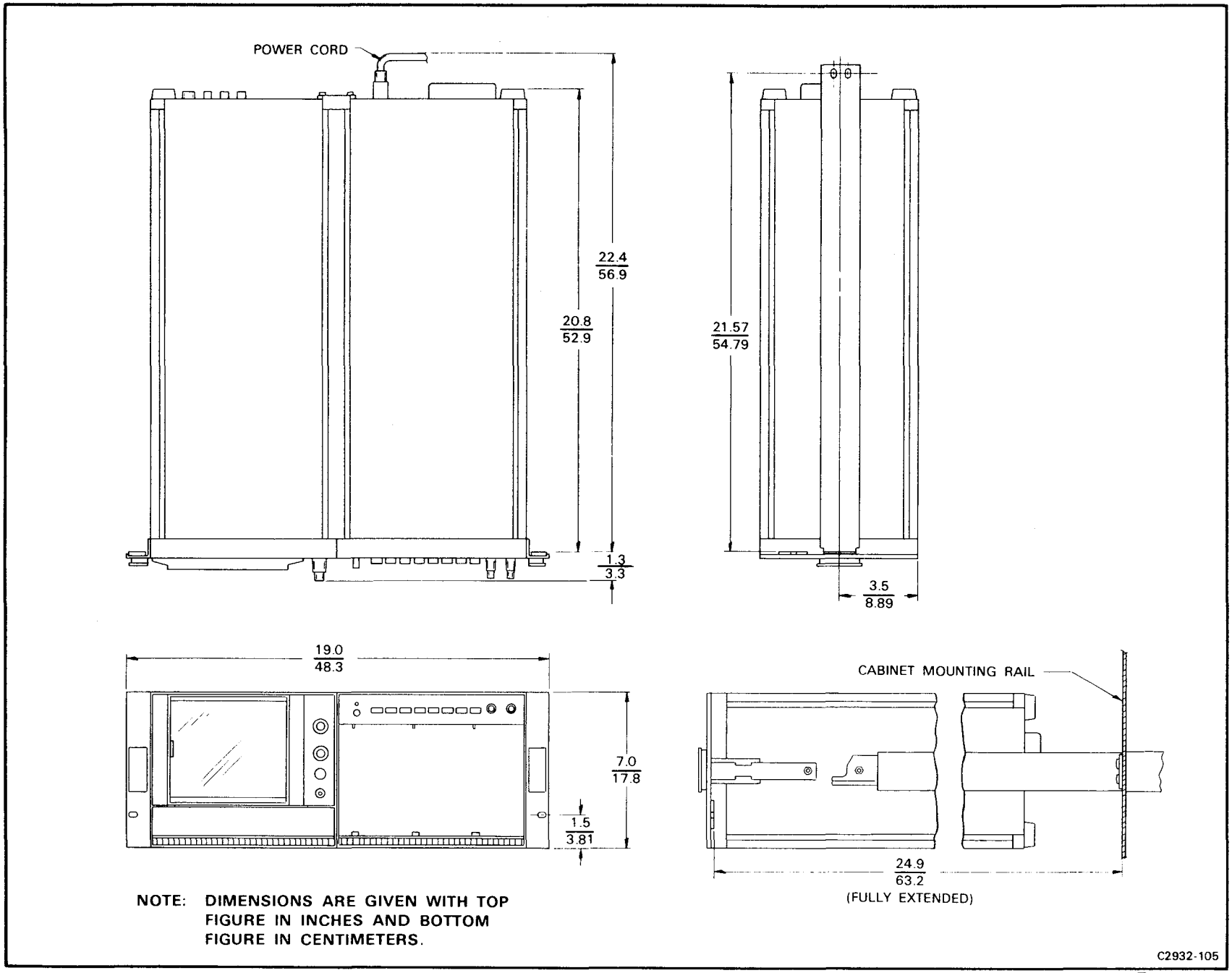

Figure 1-4. 5223 rackmount dimensional drawing.

panel can be slid out the rear of the instrument. The instrument should be operated with the panels in place to protect the interior from dust, to eliminate shock hazard, and ensure proper air circulation.

INSTRUMENT CONVERSION

The 5223 acquisition module and the display module can be fastened together stacked or side by side; this permits operation as a bench oscilloscope, or in a standard 19-inch rack. The two modules can be converted from a bench model to a rackmount model or vise versa. Field conversion kits, including the necessary parts, and instructions are available from Tektronix, Inc. Order: 040-0976-00, Bench-to-rack conversion; 040-0975-00, Rack-to-bench conversion.

NOTE

Before attempting to operate the instrument, make sure the module wiring interconnections are correct.

RACKMOUNT INFORMATION

The 5223 is designed to be installed in a standard 19-inch rack with Universal hole spacing. If a rack with other than Universal hole spacing is used, additional mounting holes may need to be drilled.

The rear mounting brackets allow this instrument to be mounted in racks with 20 to 27 inches between the front and rear rails. The 5223 must be properly supported at the rear; improper support may result in instrument damage.

RACK DIMENSIONS

A drawing showing the major dimensions of the rackmount 5223 is shown in Figure 1-4.

HEIGHT. At least 7 inches of vertical space is required to mount this instrument in a rack. This gives enough clearance for adjacent instruments and panels. Additional height may be required if an oscilloscope camera is to be used with this instrument.

WIDTH. Minimum space between the front rails of the rack is 17-5/8 inches. This space allows the slide-out tracks to operate freely, permitting the 5223 to move in and out of the rack.

DEPTH. Total depth required to mount this instrument in an enclosed-cabinet rack is 22.4 inches. This allows enough space for air circulation, signal connections, and the power cord.

SLIDE-OUT TRACKS

The slide-out tracks provided with this instrument permit it to be extended out of the rack for maintenance and calibration without removing it from the rack. Be sure the power cord and signal cables are long enough to allow operation in the extended position.

The slide-out tracks consist of two assemblies, one for the left side of the instrument and one for the right side. Figure 1-5 shows the slide-out track assembly. The stationary section of each assembly attaches to the front and rear rails of the rack. The chassis sections allow the instrument to be extended out of the rack.

The hardware needed to mount the tracks to the rack is shown in Figure 1-5. Since enough hardware is supplied to make the tracks compatible with a variety of racks and installation methods, some of it may not be needed.

MOUNTING PROCEDURE

1. Select the proper front-rail mounting holes for the stationary sections using the measurements shown in Figure 1-6.

2. Mount the front flanges of the stationary sections to the front rails of the rack with a bar nut and two pan-head screws (see Fig. 1-7).

NOTE

If the rails of the rack are tapped, either drill out the holes with a 0.196 inch (5 mm) drill or mount the front flanges in front of the rails.

3. Mount the rear of the stationary sections to the rear rail using the method shown in Figure 1-7 A or B. Be sure that the tracks are level.

4. Refer to Figure 1-8 to install the instrument into the rack.

5. See Figure 1-9 to adjust the alignment of the stationary sections.

6. After the tracks operate smoothly, connect the power cord and all necessary cables to the rear-panel connectors. Push the instrument all the way into the rack to secure the release latches.

REMOVING OR INSTALLING THE INSTRUMENT

After initial installation and adjustment of the slide-out tracks, the instrument can be removed or installed by following the instructions given in Figure 1-8. No further adjustments are required under normal conditions.

SLIDE-OUT TRACK LUBRICATION

The special finish on the sliding surfaces of the tracks provides permanent lubrication. However, if the tracks require additional lubrication, a thin coat of paraffin can be rubbed onto the sliding surfaces.

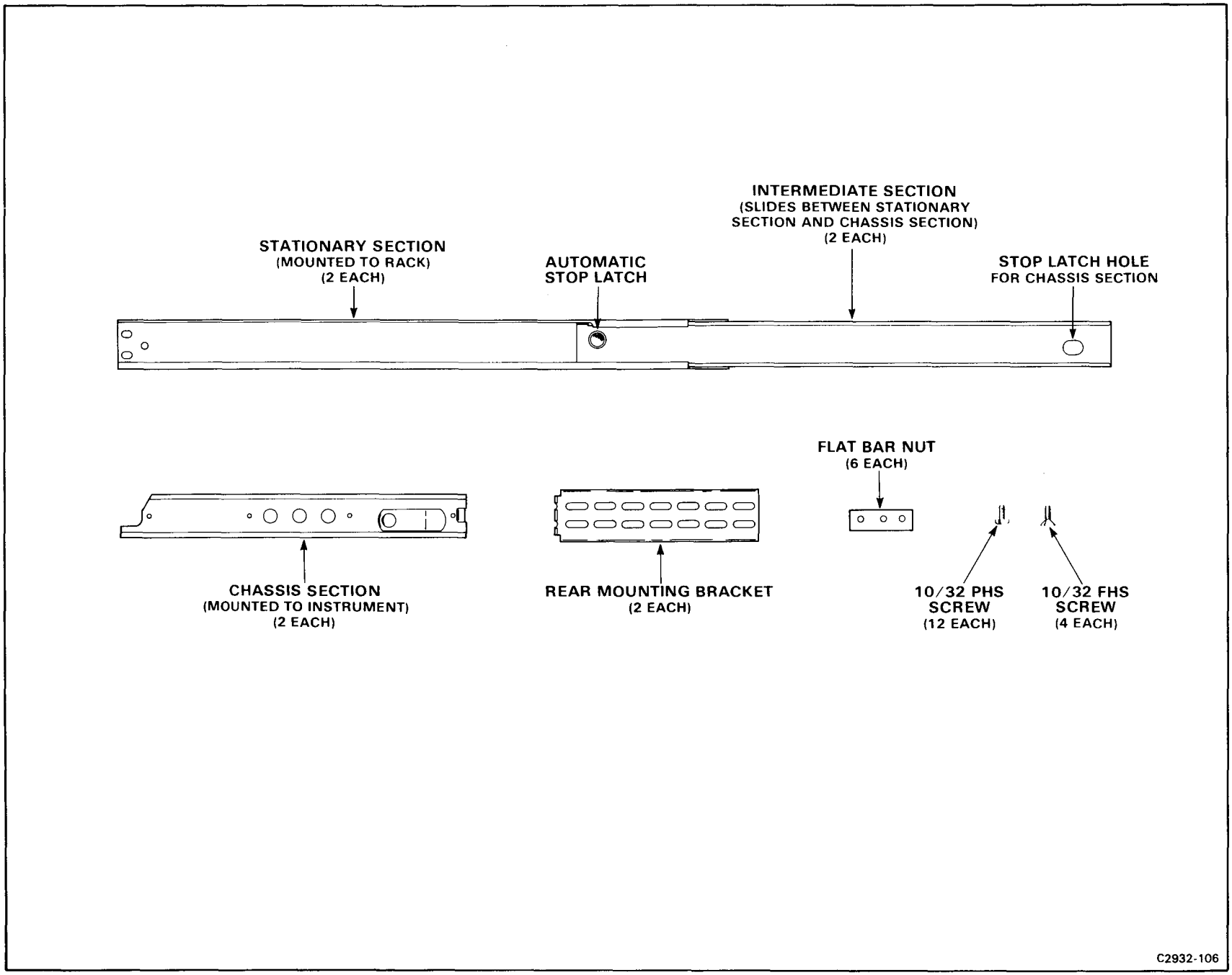

Figure 1-5. Slide-out track assembly.

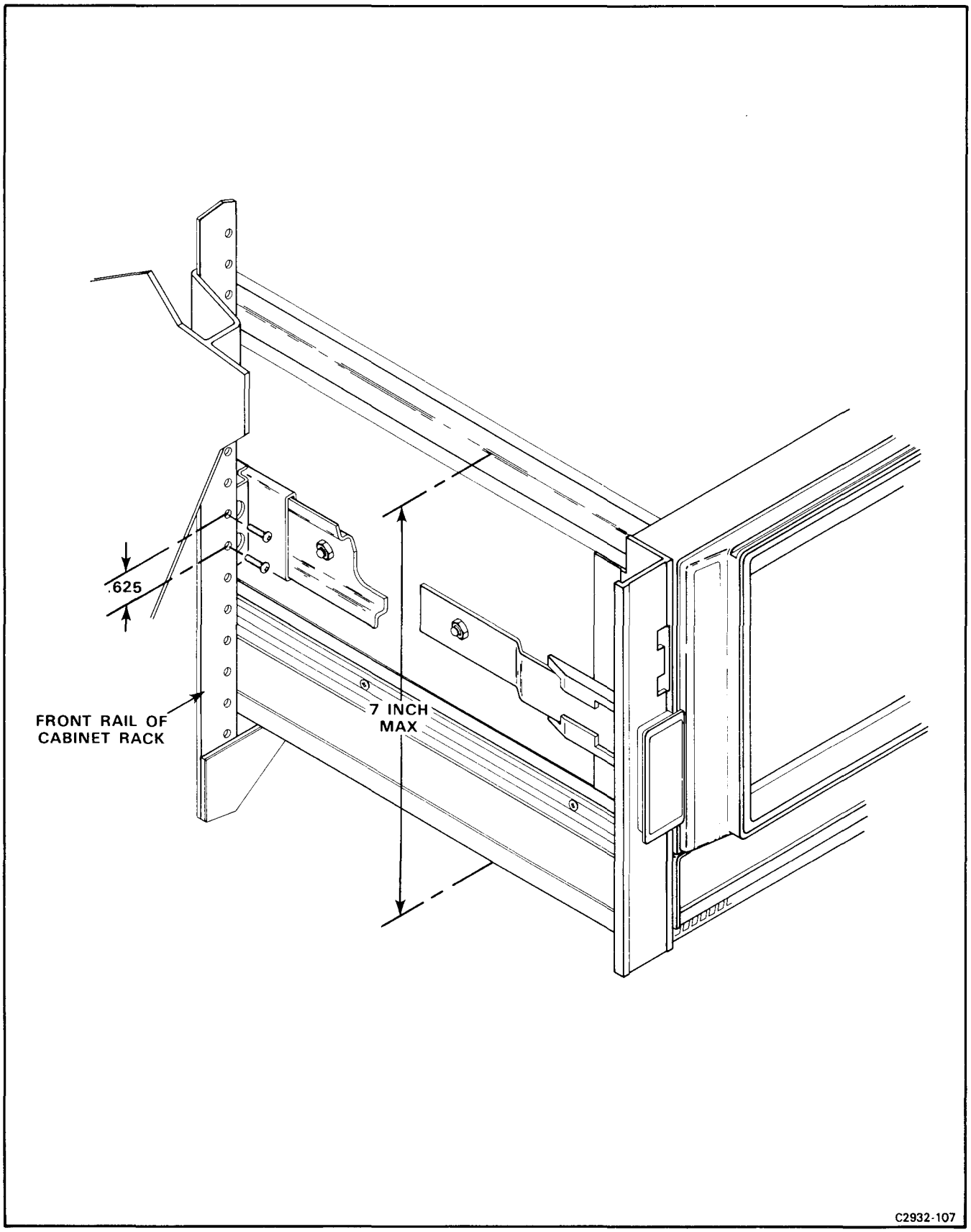

Figure 1-6. Vertical mounting position of the left stationary section, and location of securing screw holes.

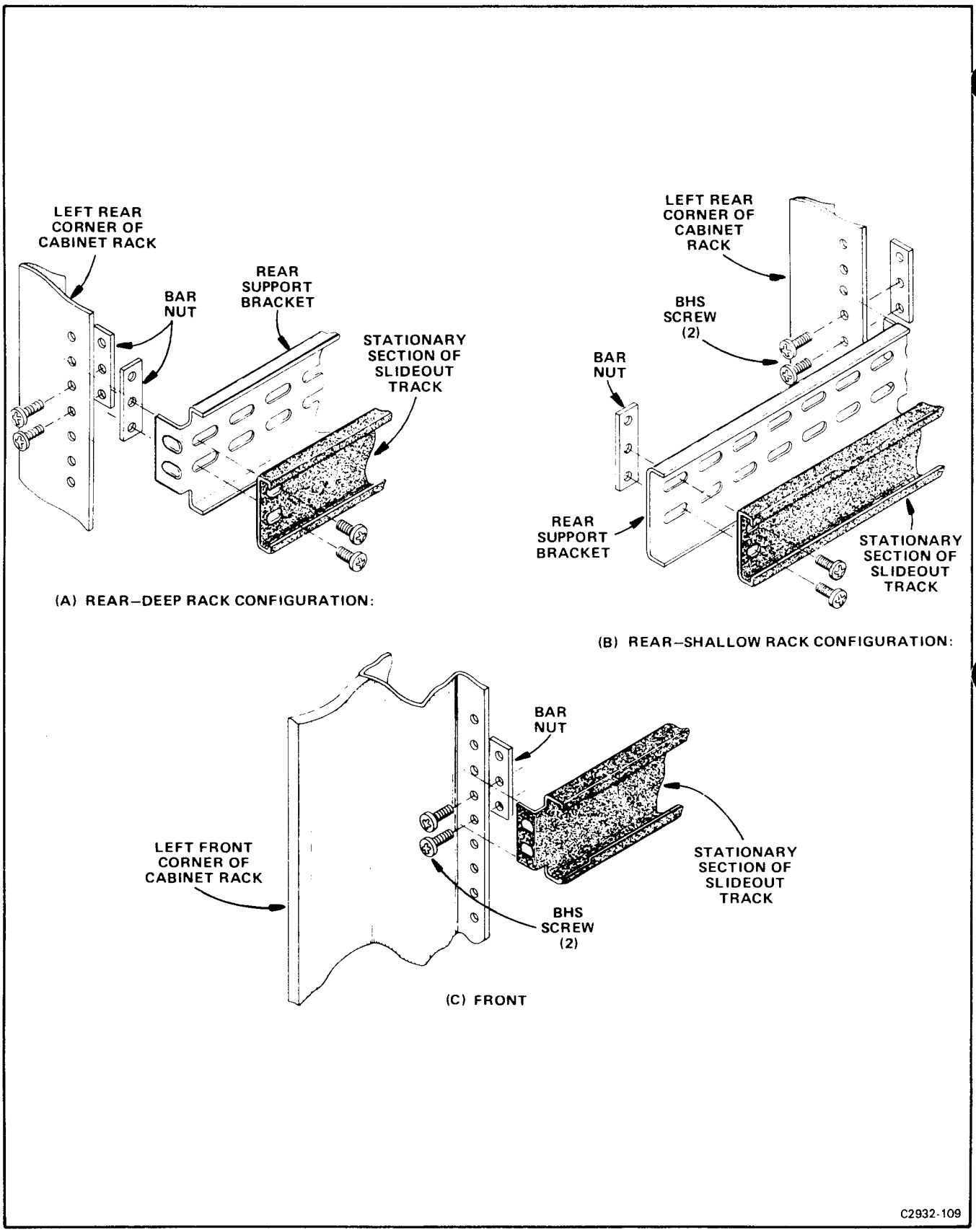

Figure 1-7. Details for mounting stationary sections.

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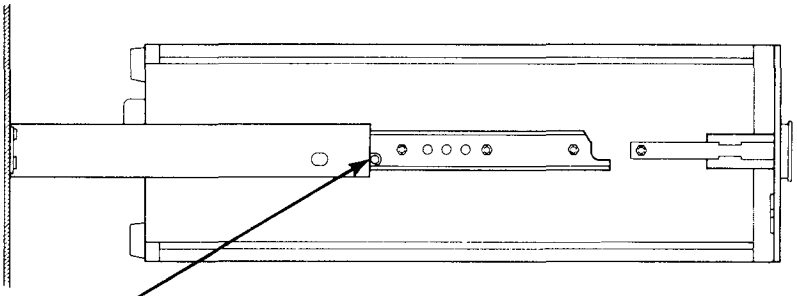

TO INSTALL

1. PULL THE SLIDEOUT TRACK INTERMEDIATE SECTIONS OUT TO THE FULLY EXTENDED POSITION.
2. INSERT THE INSTRUMENT CHASSIS SECTIONS INTO THE INTERMEDIATE SECTIONS.
3. PRESS STOP LATCHES AND PUSH INSTRUMENT TOWARD RACK UNTIL THE LATCHES SNAP INTO THEIR HOLES.
4. AGAIN PRESS STOP LATCHES AND PUSH INSTRUMENT INTO RACK UNTIL RELEASE LATCHES ARE SECURED.

TO REMOVE

1. PULL OUTWARD ON THE RELEASE LATCH HANDLES.
2. PULL THE INSTRUMENT OUTWARD UNTIL THE STOP LATCHES SNAP INTO THE HOLES.
3. PRESS STOP LATCHES AND REMOVE THE INSTRUMENT.

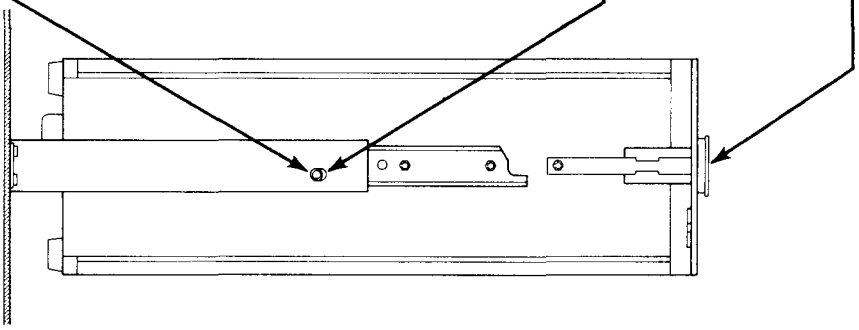

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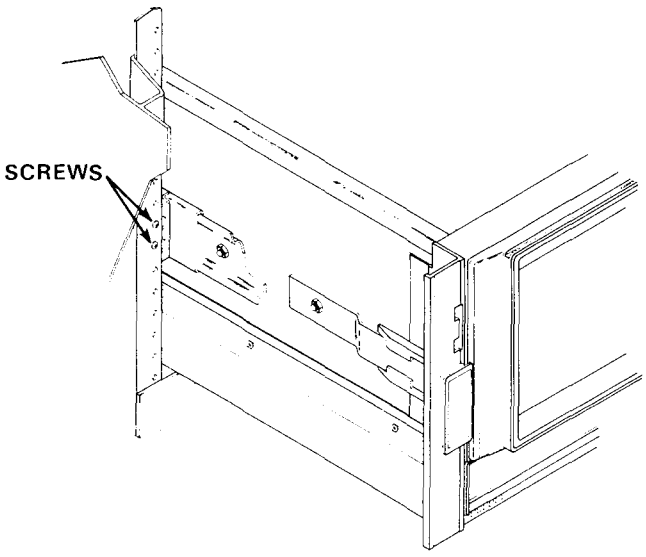
Figure 1-8. Installing and removing the instrument.



1. LOOSEN SCREWS ON BOTH SIDES (LEFT SIDE SHOWN).
2. ALLOW SLIDES TO SEEK PROPER WIDTH.
3. CENTER INSTRUMENT.
4. RETIGHTEN SCREWS.
5. PUSH THE INSTRUMENT ALL THE WAY INTO THE RACK. IF TRACKS DO NOT SLIDE SMOOTHLY, CHECK FOR CORRECT SPACING BETWEEN THE REAR SUPPORTS.

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Figure 1-9. Adjusting the slide-out tracks for smooth sliding action.

SPECIFICATION

The electrical characteristics listed in Table 1-3 apply when the following conditions are met: (1) Calibration of the instrument must have taken place at an ambient temperature between +20° and +30° C, (2) the instrument must be allowed a 20-minute warm-up period, (3) all specifications are valid at an ambient temperature of 0° to +50° C, unless otherwise stated, (4) the instrument must be in an environment that meets the limits described in Table 1-4.

Any applicable conditions not listed above are expressly stated as part of that characteristic. Environmental characteristics are listed in Table 1-4 and Physical characteristics are listed in Table 1-5. See Figures 1-3 and 1-4 for dimensional drawing.

TABLE 1-3
Electrical Characteristics

Characteristic	Performance Requirement
VERTICAL AND HORIZONTAL	
Bandwidth (With 067-0680-00 Calibration Fixture)	
Vertical	
Real Time and Stored	Dc to at least 12 MHz, with 8 div reference.
Horizontal	
Real Time	Dc to at least 7 MHz, with 8 div reference.
Maximum Horizontal Calibrated Sweep Rate	
Real Time	20 ns/div.

TABLE 1-3 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement
VERTICAL AND HORIZONTAL (Cont)	
Vertical Aberrations	
Real Time and Stored	3% or less, peak-to-peak with display centered. (Both + and −5 division steps from 067-0680-00 Calibration Fixture).
Signal Accuracy (with 067-0680-00 Calibration Fixture)	
Real Time	±1%.
Stored	
Interface to crt	±3%.
Interface to GPIB	±1%.
GPIB to crt	±2%.
Chart Output	200 mV/div.
Interface to Chart Output	±5%.
GPIB to Chart Output	±4%.
DC Gain Match	
Real Time vs Stored Vertically	Within ±2%.
Real Time vs Stored Horizontally (With Calibrated 5B25N at 0.5 ms/div)	Within ±3%.
Left Vert vs Right Vert Real Time	Within ±1%.
Vertical Low Frequency Linearity	
Real Time, Stored and Chart Output	±0.2 div or less error over any two divisions of the graticule area (measured with 067-0680-00 in "Gain" position).
Horizontal Low Frequency Linearity	
Real Time	±0.15 div or less over any one division of center 8 divisions of the graticule area, when adjusted for no error on second and tenth graticule lines (measured with 067-0680-00).
Vertical Dynamic Range	
Right Vertical Stored	At least ±5 div.
Left Vertical Stored	At least ±4 div.
Vertical Delay Line	
Real Time	Permits viewing leading edge of displayed waveform.
X-Y Operation	
Real Time	Less than 2 degrees phase shift, dc to 20 kHz, between horizontal compartment and either vertical compartment.

TABLE 1-3 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement
VERTICAL AND HORIZONTAL (Cont)	
Left Vert vs Right Vert	
Stored (Single Channel only; except at 100 μs/div) with two 5A38's, 5A45's or 5A48's	Less than 5 degrees phase shift between vertical compartments at 10 MHz.
Vertical	
Digitizer Resolution	0.01 division (10 bits).
Maximum Digitizing Rate	1 mega-sample per second, for one vertical compartment only. 1/2 mega-sample per second, for both vertical compartments.
Real Time Channel Switching	
With 5B25N Time Base set to 0.1 ms/div range or slower	
Chop Switching Rate	Time/division ÷ 100. Chop clock is trailing edge (positive-going) of sample pulse.
Chop Blanking Duration	450 to 600 ns.
Alternate Switching Rate	Channel switches at end of each sweep.
With 5B25N Time Base at 50 μ/div range or faster in Chop or Alternate	Channel switches at end of each real-time sweep.
Without Digitizer Time Base or with 5B25N in Amplifier Mode	
Chop Switching Rate	300 kHz ±25%.
Chop Blanking Duration	Less than 50%.
Alternate Switching Rate	Channel switches at end of each sweep.
Vertical Switching Sequence (Chop or Alt)	Each vertical plug-in compartment (in chop or alternate) is allocated two segments for display. Thus, if two dual-channel plug-ins are installed, the display sequence is left CH 1, right CH 1, left CH 2, right CH 2. If a single channel plug-in is installed, or selected, the display defaults to all the segments allocated to that plug-in.
Horizontal Channel Switching (Chop or Alt)	The channel switch for the horizontal plug-in compartment operates at the same rate as the left/right vertical channel switch. When using a dual-channel plug-in (amplifier or time-base), the display sequence is A, B, A, B...(CH 1, CH 2, CH 1, CH 2). Thus time base A (or CH 1) is slaved to Left Vertical compartment and time base B (or CH 2) is slaved to Right Vertical compartment.
Z-AXIS AMPLIFIER	
External Input	
Input Voltage	A voltage swing of 5 V (dynamic range + to −5 V) will fully modulate beam, dc to 1 MHz with intensity control set as necessary.

TABLE 1-3 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement
Z-AXIS AMPLIFIER (Cont)	
External Input (cont)	
Usable Frequency Range	Dc to 5 MHz.
Input Impedance	Resistance, 10 k ±10%. Capacitance, 50 pF maximum.
Maximum Safe Input	40 V (dc + peak ac).
CRT DISPLAY	
Geometry	Bowing or tilt ≤0.1 division.
Orthogonality	±0.2 division total variation over 8 divisions.
Linearity	With a normal 8 × 10 div square raster or time markers, max deviation from straight line: horizontal, 0.1 division; vertical, 0.1 division.
Phosphor	P31.
Deflection	Electrostatic with mesh magnification.
Acceleration Potential	15 kV overall.
Graticule	
Scale	8 × 10 divisions with 1.22 cm/division.
Scale Color and Type	Orange internal-graticule lines, with 5-division risetime markings.
Beamfinder	Brings trace within graticule area and increase trace intensity to a visible level.
MEMORY	
Memory length	1 K data points per vertical compartment, shared by multiple trace plug-ins.
Pretrigger Marker	Waveform is intensified prior to trigger point.
ROLL MODE	Operative at 100 ms/div and slower.
DISPLAY OUTPUTS (Chart Output)	
Maximum Clock Rate	220 Hz ±30%.
Minimum Clock Rate	14 Hz ±20%.
Output Impedance	1 KΩ ±10%.
Amplitude	200 mV/div ±5%.

TABLE 1-3 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement
MEMORY (Cont)	
PEN LIFT	
Normally Open	Relay closes during each MEMORY waveform output.
Duration	300 ms minimum, 1.5 s maximum.
Maximum Voltage	30 V, dc or peak ac.
Maximum Current	200 mA, dc or peak ac.
Maximum VA	5.
POWER SUPPLY	
Line Voltage Ranges (RMS)	90-117 V. 102-132 V. 191-249 V. 204-250 V maximum.
CALIBRATOR	
Voltage	300 mV, ±1%.
Current	3 mA, ±1%.
Frequency	1 kHz, ±1%.
Duty Cycle	50%, ±2%.
Output Iimpedance	100 Ω, ±1%.
CONNECTORS	
Camera Power	Three-contact connector compatible with TEKTRONIX C59 camera.
PLUG-IN OUTPUTS	
Amplitude	50 mV/div ±5%.
Bandwidth	
Vertical	At least 15 MHz.
Horizontal	At least 7.0 MHz.
Output Impedance	50 Ω ±10%.
Offset	±100 mV (no load).

TABLE 1-3 (CONT)
Electrical Characteristics

Characteristic	Performance Requirement
CONNECTORS (Cont)	
PLUG-IN OUTPUTS (cont)	
Noise and Crosstalk Between Any Plug-In Combination (Reference 8 Div Input)	Less than 5 mV (dc to 5 MHz). Less than 10 mV (dc to 20 MHz). Less than 25 mV (dc to 100 MHz).
SS RESET INPUT Single-Sweeep Reset)	Rear panel connector and camera bezel connector. Closure to ground causes reset.
A GATE OUT OR SAMPLE CLK OUT	
Amplitude	0.8 V max low to 2.4 V min high.
Rise Time	
From 0.8 V to 2.0 V with 50 pF and 1 M Ω Load	
SAMPLE CLK OUT	50 ns.
A GATE OUT	100 ns max.
GPIB INTERFACE	
Functions Implemented (As per IEEE 488-1978)	Description
SH1	Complete Source Handshake Capability.
AH1	Complete Acceptor Handshake Capability.
T5	Complete Talk Function.
L4	Listen Function w/o Listen Only mode.
SR1	Complete Service Request Capability.
RL2	Remote/Local Function w/o Local Lockout.
PPØ	No Parallel Poll Capability.
DC1	Complete Device Clear Capability.
DTØ	No Device Trigger Capability.
CØ	No Control Capability.
E1	Open Collector Bus Drivers.

TABLE 1-4
Environmental Characteristics

Characteristic	Performance Requirement
Temperature	
Operating	0° to 50° C.
Storage	-55° to +75° C.
Altitude	
Operating	To 15,000 feet (4,500 m).
Storage	To 50,000 feet (15,000 m).
Vibration	
Operating and Nonoperating	Tested to MIL-28800B SECT. 4.5.5.3.1 Type 2, Class 5, Style E & F.
Shock	
Nonoperating	Tested to MIL-T-28800B SECT. 4.5.5.4.1 Type 2, Class 5, Style E & F.
Bench Handling	Tested to MIL-T-28800B SECT. 4.5.5.4.4 Type 2, Class 5, Style E & F.
Transportation	National Safe Transit Assoc., Pre-Shipment Test procedure.
Vibration of Packaged Prorduct	NSTA. Project 1 A-B-1.
Drop of Packaged Product	NSTA. Project 1 A-B-2.
EMC	Tektronix Product Design Standard 062-2866-00.

TABLE 1-5
Physical Characteristics

Characteristic	Information
Ventilation	Safe operating temperature maintained by ac fan. Automatic resetting thermal cutout protects instrument.
Finish	Anodized front- and rear-panel with blue-vinyl painted aluminum cabinet.
Cabinet Version	
Net Weight, With Feet and Handle	37-1/2 lbs. (16.19 kg).
Outside Dimensions	See Figure 1-3.
Rackmount Version	
Net Weight	42 lbs. (19.1 kg).
Outside Dimensions	See Figure 1-4.

SYSTEM ELECTRICAL SPECIFICATION

Your Tektronix 5223 Digitizing Oscilloscope system provides exceptional flexibility in operation with a wide choice of general- and special-purpose plug-in units. The type number of a particular plug-in unit identifies its usage as follows:

The first digit (5) denotes the oscilloscope system for which the plug-in is designed (5000-series).

The second letter describes the purpose of the plug-in unit:

A—Amplifier unit
B—"Real time" time-base unit
C—Curve tracer
L—Spectrum analyzer
S—Sampling unit

The third and fourth digits of the plug-in type number do not carry any special connotation.

A "N" suffix letter added to the normal four-digit type number identifies a unit not equipped with the circuitry necessary to encode data for the 5000-series readout system (available in 5400 series only).

Table 1-6 lists the vertical specifications which are system dependent. For more complete specifications on plug-in units for the 5000-series oscilloscope system, refer to the Tektronix Products catalog.

Table 1-7 lists the horizontal specifications which are system dependent. For more complete specifications on plug-in units for the 5000-series oscilloscope system, refer to the Tektronix Products catalog.

Table 1-8 lists some special purpose plug-in units available for use with the 5223 Oscilloscope.

Some system incompatibilities exist between the 5223 Digitizing Oscilloscope and various plug-in units. Table 1-9 lists these incompatibilities and their effect on the operation of the system.

STANDARD ACCESSORIES

1 ea ..... Operators Manual
1 ea ..... Service Manual
1 ea ..... Faceplate Filter (installed)
1 ea ..... Power Cord
1 ea ..... GPIB Cable

For more detailed information, refer to the Tabbed Accessories page at the rear of this manual.

TABLE 1-6
5223 Oscilloscope Vertical System Specification

Product	Type	Minimum Deflection Factor	Bandwidth -3 dB	CMRR
5A13N	Single Differential/ Comparator	1 mV/div	2 MHz	10,000:1
5A15N	Single	1 mV/div	2 MHz	
5A18N	Dual	1 mV/div	2 MHz	
5A19N	Single Differential	1 mV/div	2 MHz	1,000:1
5A21N	Single Differential (voltage and current)	50 μV/div	1 MHz	100,000:1

TABLE 1-6 (CONT)
5223 Oscilloscope Vertical System Specification

Product	Type	Minimum Deflection Factor	Bandwidth -3 dB	CMRR
5A22N	Single Differential	10 μV/div	1 MHz	100,000:1
5A24N	Single	50 mV/div	2 MHz	
5A26	Dual Differential	50 μV/div	1 MHz	100,000:1
5A38	Dual	10 mV/div	10 MHz	
5A45	Single	1 mV/div	10 MHz	
5A48	Dual	1 mV/div	10 MHz	

TABLE 1-7
5223 Oscilloscope Horizontal System Specification

Product	Type	Sweep Rate	Mag	Single Sweep	Volts/Div Ext Mode
5B25N	Digitizer	0.2 μs to 5 s	10X	Yes	50 mV
5B10N	Single	1 μs to 5 s	10X	Yes	50 mV and 500 mV
5B12N	Dual Delaying	A, 1 μs to 5 s; B, 2 μs to 5 s	10X	Yes	50 mV and 500 mV
5B40	Single	0.1 μs to 5 s	10X	Yes	50 mV
5B42	Dual Delaying	A, 0.1 μs to 5 s; B, 0.1 μs to 0.5 s	10X 10X	Yes	50 mV

TABLE 1-8
Special Purpose Plug-In Units

Product	Description
5CT1N	Semiconductor Curve Tracer
5L4N	100 KHz Spectrum Analyzer
5S14N	1 GHz Sampling

TABLE 1-9
5223 Plug-In Incompatibilities

Plug-In Unit Type	Operating Conditions	Symptom	Cause
5A14N	More than one trace displayed from plug-in unit and 5223 operating in memory mode (digitizer time-base unit installed in horizontal compartment).	Memory display is incoherent and/or distorted; real-time display is distorted at time-base unit sweep rates of 0.5, 0.2 and 0.1 milli-second/division.	Plug-in channel switch settling time too slow, 5223 not designed to accommodate more than two channels in one memory.
5A18N (with Serial Numbers below B128131)	5223 operating in memory mode (digitizer time-base unit installed in horizontal compartment), and 5A18N operating in chop mode.	Memory and real-time displays are distorted at time-base unit sweep rates of 0.5, 0.2 and 0.1 milliseconds/division.	Channel switch settling time too slow; for solution of problem install 040-0963-XX kit in 5A18N.
5A26N (with Serial Numbers below B051662)	When 5223 is operating in memory mode (digitizer time-base unit installed in horizontal compartment), and 5A26N is operated in chop mode.	Memory and real-time displays are distorted at time-base unit sweep rates of 0.5, 0.2 and 0.1 milliseconds/division.	Channel switch settling time too slow; for solution of problem install 040-0964-XX kit in 5A26N.
5A48 (with Serial Numbers below B101046	When 5223 is operating in memory mode (digitizer time-base unit installed in horizontal compartment), and 5A48 is operated in chop mode.	Memory and real-time displays are distorted at time-base unit sweep rates of 0.5, 0.2 and 0.1 milliseconds/division.	Channel switch settling time too slow; for solution of problem install 040-0958-XX kit in 5A48.
5L4N (with Serial Numbers below B07XXXX)	Physically locked out of 5223 when installed in both vertical compartments. When installed in 5223 right vertical and horizontal compartments, unit operates in real-time mode without memory capability.		For solution of problem contact your local Tektronix field office.
5S14N	Physically locked out of 5223 when installed in both vertical compartments. When installed in 5223 right vertical and horizontal compartments unit operates in real-time mode without memory capability.		Mechanical interference of post against internal components. 5S14N can be operated in 5223 if post is removed; however 5L4N with Serial Numbers below B07XXXX will be damaged when operated in 5223 with post removed.

TABLE 1-9 (CONT)
5223 Plug-In Incompatibilities

Plug-In Unit Type	Operating Conditions	Symptom	Cause
5B10N 5B12N	Sweep rates of 1 microsecond/division and faster.	Leading edge of pulse(s) not displayed.	Trigger circuitry too slow.
5B10N 5B12N	Composite trigger mode.	Will only trigger off signal from left vertical plug-in unit.	5223 will not allow composite trigger mode operation of these plug-in units.

OPERATING INSTRUCTIONS

To operate this instrument effectively, the user must become familiar with the operation and capabilities of the instrument. This section describes the use of front- and rear-panel controls and connectors.

NOTE

Detailed operating information for a specific plug-in is given in the instruction manual for that unit.

WARNING

To avoid electric-shock hazard, see Installation in the General Information section of this manual before operating this instrument.

STANDARD OPERATION

OPERATING MODES

The 5223 Option 10 oscilloscope has two non-standard modes of operation. These are the Talk Only and Test modes which are selected by the rear-panel GPIB Address Selection switch. If the 5223 Option 10 is in either of these modes, normal operation of the oscilloscope cannot be obtained. For standard operation of the 5223 Option 10 oscilloscope, these switch sections must be set as shown in Figure 2-1.

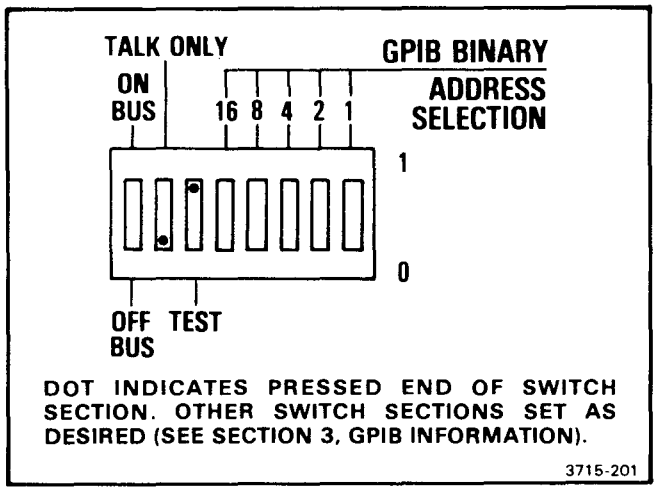


Figure 2-1. Standard operating mode.

POWER-UP SELF-TEST

The 5223 Option 10 Digitizing Oscilloscope automatically performs a self-test each time power is applied to the instrument. At power-on, a Reset signal is generated which initiates the running of a series of internal routines that verify the proper operation of the GPIB-board ROM, GPIB-board RAM, GPIB-board to Memory-board data path, the waveform memory, and the GPIB-Board to Driver-board data path.

Results of the self-test are displayed by the LEDs in the MEMORY CONTENTS switches on the front panel of the instrument. Self-test fault conditions are indicated by blinking LEDs.

If the instrument successfully passes its self-test, none of the LED's will blink or stay illuminated unless they are pressed.

Should any self-test produce a fault indication, all subsequent tests are suspended. Refer service personnel to the Maintenance section of the 5223 Option 10 Service manual.

LED assignments for fault indications are listed below:

LED	FAULT LOCATION
DISPLAY LEFT	Lower ROM.
SAVE LEFT	Upper ROM.
L VS R	RAM.
SAVE RIGHT	CPU-board to Memory-board data path.
DISPLAY RIGHT	Waveform memory.
VECTOR MODE	CPU-board to Back-Panel board data path.

A fault condition warning can be ignored by pressing the OUTPUT SAVED DISPLAY button. This will extinguish the flashing LED and step the instrument to the next item in the self-test sequence. Depending on the severity of the fault, you may be able to step the instrument through all remaining tests and into normal operation in this manner.

The following circumstances may cause apparent fault conditiions. These conditions should be checked before requesting service.

1. If the rear panel TALK ONLY switch is on, none of the MEMORY CONTENTS switches will operate normally following the self-test.

2. If the rear panel TEST switch is in the ON position when power is applied, the instrument will not complete its self-test but will branch instead to one of the signature analysis routines.

3. If a 5B25N Digitizing Time Base/Amplifier unit is not installed, or if it is set to "AMPL", both SAVE lights will illuminate and stay lit at the conclusion of the self-test. This is true regardless of whether or not the SAVE buttons are pressed but it DOES NOT indicate a fault condition.

4. The ROLL pushbutton will not light when pressed if the time-base sweep speed is set faster than 0.1 second per division.

5. If the L VS R button and one of the SAVE buttons are pressed, the other SAVE button will be lit whether it is pressed or not.

Graticule Pattern Display

At the conclusion of the Waveform Memory test, a calibrated graticule pattern is loaded into the left and right memory compartments. This pattern will be displayed if both SAVE buttons, the L VS R button, and both DISPLAY buttons are pressed at power-on.

The displayed graticule will have one dot on each minor division. The dots are arranged in such a way that, if the graticule is output to an X-Y plotter, a continuous curve is plotted.

The graticule display can be erased by releasing the SAVE buttons.

PLUG-IN UNITS

The 5223 accepts up to three Tektronix 5000-series plug-in units. This plug-in feature allows a variety of display combinations and also allows selection of bandwidth, sensitivity, display mode, etc., to meet many measurement requirements. In addition, it allows the oscilloscope system to be expanded to meet future measurement requirements. The overall capabilities of the resultant system are, in large part, determined by the characteristics of the plug-ins selected[1].

INSTALLATION

To install a plug-in unit into one of the plug-in compartments, align the slots in the top and bottom of the plug-in with the associated guides in the plug-in compartment. Push the plug-in unit firmly into the plug-in compartment until it locks into place. To remove a plug-in, pull the release latch on the plug-in unit to disengage it and pull the unit out of the plug-in compartment. It is not necessary that all of the plug-in compartments be filled to operate the instrument, the only plug-ins needed are those required for the measurement to be made. Blank plug-ins or front panels should be used to ensure proper airflow through the instrument. When the instrument is adjusted in accordance with the adjustment procedure given in the service manual, the vertical and horizontal gain are standardized. This allows calibrated plug-in units to be changed from one plug-in compartment to another without readjustment. However, the basic adjustment of the individual plug-in units should be checked when they are installed in this system to verify their measurement accuracy. See the plug-in service manual for verification procedure.

PLUG-IN SELECTION[1]

The plug-in versatility of the 5223 oscilloscope allows a variety of display modes with many different plug-ins. The following information is provided here to aid in plug-in selection.

To produce a single-trace display, install a single-channel vertical unit (or dual-channel unit set for single-channel operation) in either of the vertical (left or right) compartments. For dual-trace displays, either install a dual-channel vertical unit in one of the vertical compartments or install a single-channel vertical unit in each vertical compartment. A combination of a single-channel and a dual-channel vertical unit allows a three-trace display; likewise, a combination of two dual-channel vertical units allows a four-trace display. The 5223 does allow the operation of a plug-in unit with more than two channels (e.g. 5A14N), but in the real-time mode only.

To obtain a vertical sweep with the input signal displayed horizontally, insert a time-base unit into one of the vertical compartments and a amplifier unit in the horizontal compartment. If a vertical sweep is used, there is no retrace blanking and the time-base unit triggering must be accomplished externally.

For X-Y displays, either a 5A-series amplifier unit or a 5B-series time-base unit having an amplifier channel can be installed in the horizontal compartment to accept the X signal. The Y signal is connected to a 5A-series amplifier unit installed in a vertical compartment.

[1] Refer to Table 1-9, 5223 Plug-In Incompatibilities in this manual for operating restrictions concerning a particular plug-in unit, when used in the 5223 Digitizing Oscilloscope.

Special purpose plug-in units may have specific restrictions regarding the compartments in which they can be installed. This information will be given in the instruction manuals for these plug-ins.

CONTROLS AND CONNECTORS

The 5223 Digitizing Oscilloscope front- and rear-panel controls and connectors are shown in Figure 2-2 and Figure 2-3. A brief, functional description of each control and connector is included in the illustration. Refer to Detailed Operating Information for additional information.

OPERATING INFORMATION

DISPLAY SWITCHING LOGIC

The electronic switching for time-shared displays is produced at the plug-in interface within the mainframe; however, the switching logic is selected in the plug-in units. The system allows several combinations of plug-ins and Display switch settings. Refer to the individual plug-in manuals for specific capabilities and operating procedures[1].

Switching Sequence

Four display time slots are provided on a time-sharing basis. When two vertical plug-ins are active, each receives two time slots, so the switching sequence is: left, right, left, right, etc. The two time slots alloted to each plug-in are divided between amplifier channels in a dual-trace unit; if two dual-trace plug-ins are active, then the switching sequence is: left Channel 1, right Channel 1, left Channel 2, right Channel 2, etc. If only one vertical plug-in is active, it receives all four time slots. The switching sequence is the same for both the alternate and chopped display modes[1].

VERTICAL DISPLAY MODE

Display On

To display a signal, the Display button of the applicable vertical plug-in unit must be pushed in to activate the unit. If two plug-ins are installed in the vertical compartments and the signal from only one of the units is desired, set the Display switch of the unwanted unit to Off (button out). If neither plug-in is activated, the signal from the left unit is displayed. Both plug-ins can be activated for multi-trace displays[1].

Alternate Mode

The alternate position of the time-base unit Chop/Alt switch produces a display that alternates between activated plug-ins and amplifier channels with each sweep of the time base. The switching sequence is described under Display Switching Logic in this section. Although the Alternate mode can be used at all sweep rates, the Chop mode may provide a more satisfactory display at sweep rates from about one millisecond/division to five seconds/division. At these slower sweep rates, alternate-mode switching becomes difficult to view.

Chopped Mode

The Chop position of a nondigitizer time-base unit Display switch produces a display that is electronically switched between channels at a 300-kilohertz rate. The switching sequence is discussed earlier. In general, the Chop mode provides the best display at sweep rates slower than about one millisecond/division or whenever dual-trace, single-shot phenomena are to be displayed. At faster sweep rates, the chopped switching becomes apparent and may interfere with the display.

The 5B25N chopped switching rate can be determined by dividing the Time/Division switch setting by 100 at sweep rates of 0.1 millisecond/division and slower; at sweep rates of 50 microseconds/division and faster the channel switching occurs at the end of each sweep, i.e., it operates in alternate mode only.

Dual-Sweep Displays

When a dual-sweep time-base unit is operated in the horizontal compartment, the alternate and chopped time-shared switching for either the A or B sweep is identical to that for a single time-base unit. However, if both the A and B sweeps are operating, the 5223 operates in the independent pairs mode. Under this condition, the left vertical unit is always displayed at the sweep rate of the A time base and the right vertical unit is displayed at the sweep rate of the B time base (nondelayed sweep only). This results in two displays that have completely independent vertical deflection and chopped or alternate sweep switching[1].

X-Y OPERATION

In some applications, it is desirable to display one signal versus another (X-Y) rather than against an internal sweep. The flexibility of the plug-in units available for use with the 5223 provides a means for applying a signal to the horizontal deflection system for this type of display. Some of the 5B-series time-base units can be operated as amplifiers, in addition to their normal use as time-base generators. For more information on X-Y displays, see the discussion on L VS R in this section of the manual.

RASTER DISPLAY

A raster-type display can be used to effectively increase the apparent sweep length. For this type of display, the trace is deflected both vertically and horizontally by

[1] Refer to Table 1-9, 5223 Plug-In Incompatibilities in this manual for operating restrictions concerning a particular plug-in unit, when used in the 5223 Digitizing Oscilloscope.

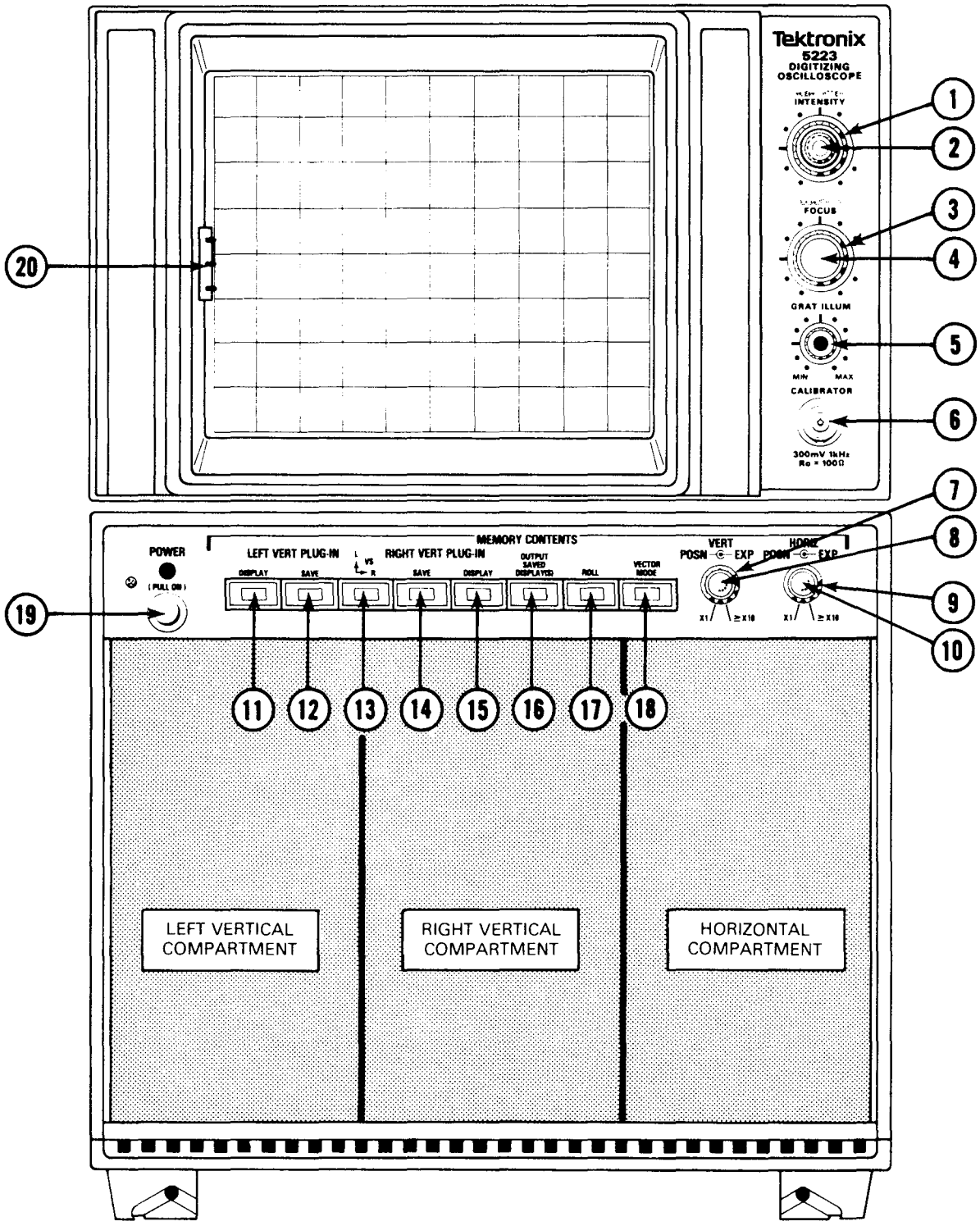


Figure 2-2. Front-panel controls, connectors and indicators.

(1) **INTENSITY**—Controls brightness of real-time display.

(2) **MEM INTEN**—Controls brightness of memory display.

(3) **FOCUS**—Control to optimize crt display definition.

(4) **BEAMFINDER**—Switch, when pressed, compresses and intensifies display so that it is visible within the graticule area.

(5) **GRAT ILLUM**—Control varies level of graticule illumination.

(6) **CALIBRATOR**—Connector provides a 300 mV, 1 kHz, square-wave voltage for calibrating amaplifiers or compensating probes.

(7) **VERT POSN**—Control positions the memory display vertically.

(8) **VERT EXP**—Control expands the memory display vertically.

(9) **HORIZ POSN**—Control positions the memory display horizontally.

(10) **HORIZ EXP**—Control expands the memory display horizontally.

(11) **DISPLAY**—Switch produces a digitized display of the left vertical plug-in signal(s) on the crt.

(12) **SAVE**—Switch causes the left vertical digitized waveform to be saved (memory cannot be updated until button is released).

(13) **L VS R**—Switch causes the left memory to be displayed on the Y axis (vertical) and the right memory to be displayed on the X axis (horizontal).

(14) **SAVE**—Switch causes the right vertical digitized waveform to be saved (memory cannot be updated until this button is released).

(15) **DISPLAY**—Switch produces a digitized display of the right vertical plug-in signal(s) on the crt.

(16) **OUTPUT SAVED DISPLAY(S)**—Switch makes available a voltage analog of the saved memory display(s) at the rear-panel MEMORY Y and X connectors.

(17) **ROLL**—Switch causes the memory display(s) to move from right to left on the crt (in a Y-T mode). Thus the most recently acquired data is at the right of the display(s) operational with digitizer time-base only and sweep rates equal to or slower than 0.1 second/div).

(18) **VECTOR MODE**—Switch joins dots in the memory display.

(19) **POWER (Switch and Indicator)**—Switch controls power to instrument. Indicator illuminates when power is applied to instrument.

(20) **Camera Power Connector (not labeled)**—Three pin connector provides power for camera operation and receives single-sweep-reset signal from compatible camera systems.

C2932-201B

Figure 2-2 (cont). Front-panel controls, connectors and indicators.

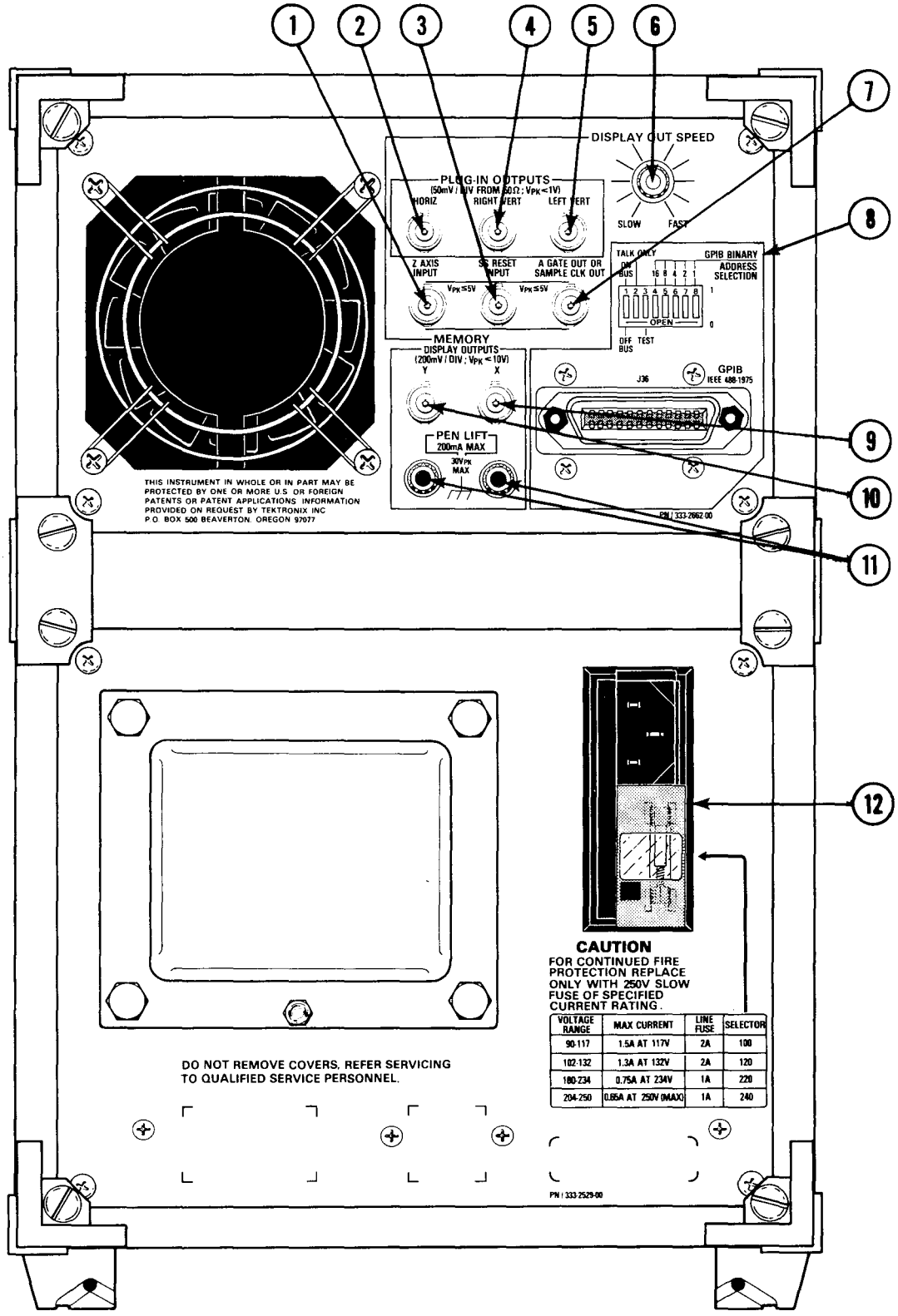


Figure 2-3. Rear-panel controls and connectors.

REAR-PANEL DESCRIPTIONS

(1) **Z-AXIS INPUT**—Connector for external input to intensity modulate the display(s).

(2) **HORIZ**—Connector makes available the horizontal plug-in signal(s).

(3) **SS RESET INPUT**—Connector for input of remote single-sweep reset.

(4) **RIGHT VERT**—Connector makes available the right-vertical plug-in signal(s).

(5) **LEFT VERT**—Connector makes available the left-vertical plug-in signal(s).

(6) **DISPLAY OUT SPEED**—Controls the rate at which the saved memory display(s) is converted to an analog voltage and made available at the MEMORY X and Y connectors.

(7) **A GATE OUT OR SAMPLE CLK OUT**—Connector makes available the time-base gate.

(8) See Section 3, GPIB Information for description of GPIB controls.

(9) **MEMORY X**—Connector provides a voltage analog of the memory vertical signal(s).

(10) **MEMORY Y**—Connector provides a voltage analog of the memory vertical signal(s).

(11) **PEN LIFT**—Connectors provide control to auxiliary equipment (i.e., X-Y plotter) when front-panel OUTPUT DISPLAY cycle is activated.

(12) **Line-Voltage Selector, Power Cord Connector and Fuse Holder**—Board insert to select line source voltage.

3715-203B

Figure 2-3 (cont). Rear-panel controls and connectors.

sawtooth signals, and is accomplished by installing a 5B-series time-base unit in the left vertical compartment, as well as one in the horizontal compartment. Normally, the unit in the vertical compartment should be set to a slower sweep rate than the time-base unit in the horizontal compartment; the number of horizontal traces in the raster depends upon the ratio between the two rates.

Information can be displayed on the raster using the Z-AXIS INPUT to provide intensity modulation of the display. This type of raster display can be used to provide a television-type display.

GRATICULE

The graticule is marked on the inside of the crt faceplate, providing accurate, parallax-free measurements. The graticule is divided into eight vertical and ten horizontal divisions. Each divison is a 1.22 centimeter square divided into five minor divisions along each axis. The vertical gain and horizontal timing of the plug-in units are calibrated to the graticule so that accurate measurements can be made from the crt. The illumination of the graticule lines can be varied with the GRAT ILLUM control.

Figure 2-4 shows the graticule and defines the various measurement lines. The terminology defined here will be used in all discussions involving measurements from the graticule. The markings: 0%, 10%, 90%, and 100% on the left side of the graticule are for accurate rise-time measurements.

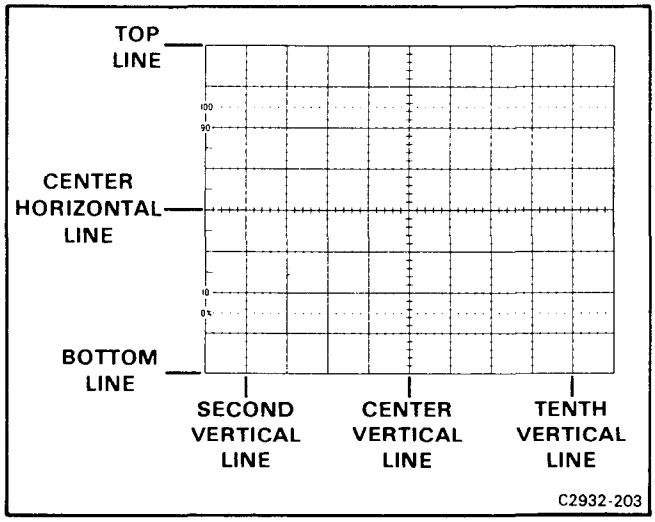


Figure 2-4. Definition of graticule measurement lines.

LIGHT FILTER

The tinted face-plate filter minimizes light reflections from the face of the crt to improve contrast when viewing the display under high-ambient-light conditions. This filter may be removed for waveform photographs or for viewing high-writing-rate displays. To remove the filter, pull outward on the bottom of the plastic crt mask and remove it from the crt bezel. Remove the tinted filter; leave the clear plastic faceplate-protector (implosion shield) installed and replace the mask. The face-plate protector should be left in place at all times to protect the crt face from scratches and the operator from crt implosion.

WARNING

Do not remove the clear plastic implosion shield covering the crt face plate; the implosion shield provides protection to the operator from crt implosion.

INTENSITY CONTROLS

The INTENSITY control determines the brightness of the real-time display. The MEM INTEN determines the brightness of the stored display. This control is operational only when either the MEMORY CONTENTS LEFT or RIGHT VERT PLUG-IN DISPLAY switch(s) is set to the in position.

BEAMFINDER

The BEAMFINDER helps to locate a display that overscans the crt viewing area vertically and/or horizontally. When the BEAMFINDER button is pressed, the display is compressed and intensified within the graticule area. To locate and reposition an overscanned display, use the following procedure:

1. Press the BEAMFINDER switch; while the display is compressed adjust the vertical and horizontal position controls to center the display. Change the vertical and horizontal deflection factors until the vertical deflection is about four divisions high and the horizontal deflection is about six divisions wide. (The horizontal deflection needs to be reduced only when operating in an X-Y mode.)

2. Release the BEAMFINDER switch; the display should remain within the graticule area.

MEMORY CONTENTS

The 5223 with a digitizer time-base unit installed in the horizontal compartment has the capability of storing real-time waveforms in memory and then displaying the stored waveform. The MEMORY CONTENTS switches and controls are used to perform this function. After obtaining a real-time display with the MEMORY CONTENTS switches in the out position, press the DISPLAY switch for the appropriate vertical plug-in unit, a duplicate waveform will be displayed (the MEM INT, VERT POSN, and HORIZ POSN controls may need adjusting to position the waveform onto the crt display area). In the DISPLAY mode the redisplayed waveform is constantly being updated. This can be demonstrated by grounding the input signal; the memory display will then be an updated base line along with the real-time display, if the digitizer time-base unit is in the auto mode.

However, when the appropriate SAVE switch is pressed, the memory waveform is saved in the 5223 memory. To demonstrate the SAVE function, obtain a real-time display with the time-base unit in Auto mode. Press the DISPLAY switch, press the SAVE switch and disconnect the input signal. The real-time display will change to a base line and the saved memory display will remain unchanged.

The MEMORY CONTENTS VERT POSN and VERT EXP controls can be used to position and expand the stored waveform vertically. The MEMORY CONTENTS HORIZ POSN and HORIZ EXP controls can be used to position and expand the stored waveform horizontally.

L VS R

The L VS R mode allows X-Y comparisons of two signals. The L VS R mode allows a signal applied to the Left Vertical plug-in unit to be displayed against a signal applied to the Right Vertical plug-in unit. For X-Y Comparisons the left vertical plug-in unit provides the Y axis and the Right Vertical plug-in provides the X axis. Acquisition of both vertical compartments occurs simultaneously; this feature allows X-Y displays of frequencies from dc to 10 megahertz with less than 5 degrees phase shift. Optimum performance is provided when identical plug-in units are used (e.g., 5A38, 5A45, or 5A48) and are operated in the single channel mode. For the best display, one cycle only of the slowest signal should be displayed. The storage capabilities of the 5223 are such that these signals do not have to occur at the same time. To demonstrate this capability, apply a signal to the left vertical unit and press the MEMORY CONTENTS LEFT VERT PLUG-IN SAVE switch, then apply a signal to the right vertical unit and press the MEMORY CONTENTS RIGHT VERT PLUG-IN SAVE switch. Press the L VS R switch; the left vertical signal is displayed on the Y axis and the right vertical signal is displayed on the X axis.

ROLL MODE

The Roll mode is operational with a digitizer time-base unit only, at sweep rates of 0.1 seconds and slower. In this mode, the signal is digitized and recorded on the right-hand side of the display; the recorded digitized signal moves across the crt from the right to the left much like a strip chart recorder.

To demonstrate the Roll mode, use the following procedure:

1. Install a digitizer time-base unit in the right horizontal compartment, and an amplifier unit in the left vertical compartment.

2. Set all of the 5223 MEMORY CONTENTS switches to the out position. Press the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY switch.

3. Set the VERT POSN and HORIZ POSN controls to midrange.

4. Set The VERT EXP and HORIZ EXP controls fully counterclockwise.

5. Set the digitizing time-base unit sweep rate to 0.5 seconds/division, and the triggering mode to auto.

6. Rotate the left amplifier plug-in unit position control and notice that the memory display is updated at the end of the real-time sweep.

7. Press the MEMORY CONTENTS ROLL switch and notice that the real-time sweep disappears.

8. Rotate the left amplifier plug-in unit position control and notice that the stored display is updated at the right hand side of the crt screen.

9. Rotate the left amplifier plug-in position control and at the same time press the MEMORY CONTENTS LEFT PLUG-IN SAVE switch; notice that the display is now stationary.

VECTOR MODE

The MEMORY CONTENTS VECTOR MODE switch is used to reduce the effect of perceptual aliasing. Perceptual aliasing is a type of optical illusion inherent in dot displays. When stored data are displayed as points, the eye tends to visually connect adjacent points; however, the closest dots in screen position, may not be the next in sequence. In addition to perceptual aliasing, dot displays can also show an "envelope error" that occurs when the dots do not fall on the peaks of the signal. See Figure 2-5.

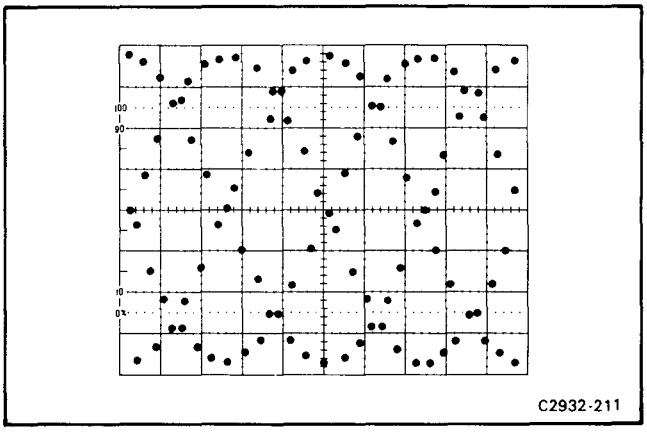


Figure 2-5. Perceptual aliasing illustrated.

Perceptual aliasing is easily remedied by adding vectors to the display as shown in Figure 2-6. But the envelope error can still persist because the vectors are straight lines joining the data points. The actual signal could still lie outside the waveform traced by the vectors, if the digitizer did not sample the peak points of the waveform. Each type of display construction (dots or vectors) yields a

different useful storage bandwidth. Dot displays will need more samples-per-cycle on the crt screen to help alleviate perceptual aliasing and envelope errors. Vector displays need less samples-per-cycle since the vectors help reduce the effect of perceptual aliasing. To estimate the useful storage bandwidth for single-shot storage of sine waves, use the following rules-of-thumb:

1) $\text{Approximate Useful Bandwidth for Dot Displays} \approx \frac{\text{maximum sampling rate}}{25}$

2) $\text{Approximate Useful Bandwidth for Vector Displays} \approx \frac{\text{maximum sampling rate}}{10}$

(Envelope Error is approximately 5% with formula 2)

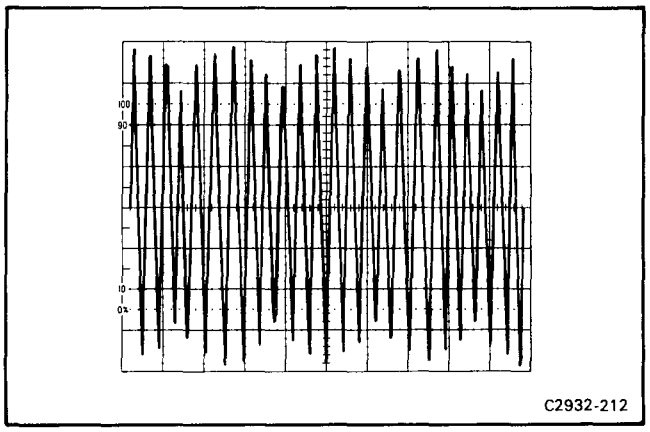


Figure 2-6. Vector Mode display.

CALIBRATOR OUTPUT

The CALIBRATOR provides a convenient signal for checking basic vertical gain and sweep timing. The calibrator signal is also very useful for adjusting probe compensation as described in probe instruction manuals. In addition,the calibrator can be used as a convenient signal source for application to external equipment.

Voltage

The CALIBRATOR provides an accurate voltage of 300 millivolts, into a high impedance load.

Repetition Rate

The repetition rate of the CALIBRATOR is 1 kilohertz. The CALIBRATOR circuit uses frequency-stable components to maintain accurate frequency and a constant duty factor. Thus, the CALIBRATOR can be used for checking the basic sweep timing of time-base units (1-kilohertz rate only).

Wave Shape

The square-wave output signal of the CALIBRATOR can be used as a reference wave shape when checking or adjusting the compensation of passive, high-resistance probes. The square-wave output from the CALIBRATOR has a flat top; so that any distortion in the displayed waveform is due to improper probe compensation.

DISPLAY PHOTOGRAPHY

A permanent record of the crt display can be obtained with an oscilloscope camera system. The instruction manual for the Tektronix oscilloscope cameras include complete instructions for obtaining waveform photographs.

The 5223 crt bezel provides integral mounting for Tektronix oscilloscope cameras. The three pins located on the left side of the crt bezel connect power to compatible camera systems. Control signals are also received from Tektronix automatic cameras to allow camera-controlled single-shot photography (see camera manual for further information).

INPUT/OUTPUT SIGNALS (Rear-Panel)

A Gate Out or Sample Clock Out

One of two signals can be selected to be available at the A GATE OUT/SAMPLE CLK OUT connector. The source of this signal is the time-base unit installed in the horizontal compartment. The A Gate is a positive-going rectangular pulse. The duration of the A Gate signal is the same as the duration of the respective time-base sweep.

Refer Selection of SAMPLE CLK OUT signal to qualified service personnel only.

Plug-In Outputs

Signals from the left and right vertical plug-in units are available at the LEFT VERT and RIGHT VERT rear-panel connectors. Likewise, the horizontal signal is available at the HORIZ connector. These outputs are provided as a convenient signal source of the vertical and horizontal deflection signals.

Intensity Modulation

Intensity (Z-axis) modulation can be used to relate a third item of electrical phenomena to the vertical (Y-axis) and the horizontal (X-axis) coordinates without affecting the waveshape of the displayed signal. This is accomplished by changing the intensity of the displayed waveform to provide a "grey scale" display.

The voltage amplitude required for visible trace modulation depends on the setting of the INTENSITY and MEM INTEN controls. A 5 volt peak-to-peak signal will completely modulate the display at the appropriate intensity setting; lower amplitude signals can be used to change the relative trace brightness. Negative-going signals decrease display intensity and positive-going

signals increase the display intensity. Refer to the General Information section in this manual for specifications on Z-axis signal requirements.

Time markers applied to the rear-panel Z-AXIS INPUT connector provide a direct time reference on the display. With an uncalibrated horizontal sweep, or with X-Y mode operation, the time markers provide a means of reading time directly from the display. If the markers are not time-related to the display waveform, use a single-sweep display.

Remote Single-Sweep Reset

An external single-sweep-reset signal can be applied to a time-base unit installed in the horizontal plug-in compartment through the rear-panel SS RESET INPUT connector. This remote reset function is a duplication of the manually-operated single-sweep reset function (pushbutton) located on the front panel of the 5B-series time-base units[1]. The signal source for the external single-sweep reset function can be either active (pulse generator, logic circuit, etc.) or passive (switch or relay); closure to ground causes reset.

Memory Display Outputs

The X and Y MEMORY DISPLAY OUTPUTS signals can be used by associated equipment (i.e., X-Y plotter) to make a permanent record of the waveform information stored in the 5223 memories. When the front-panel OUTPUT SAVED DISPLAY(S) switch is pressed a voltage analog of the appropriate memory information is made available on a one shot basis at a rate determined by the DISPLAY OUT SPEED control. To insure proper operation, the front-panel DISPLAY and SAVE switches should be set to their in position. During this cycle the crt display defaults to real-time operation after which the stored display returns to the crt.

Pen Lift

The PEN LIFT function is used in conjunction with the X-Y plotter to cause the writing pen to engage the paper. The function can be set, when activated, to cause a switch closure or opening. Refer selection to qualified service personnel only.

IEEE-488 (GPIB) Connector

The GPIB connector and Address Selection switch are described in Section 3, GPIB Information.

OPERATORS CHECKOUT PROCEDURE

The Operators Checkout Procedure may be used to verify proper operation of the front-panel controls and for familiarization with the instrument. Only instrument functions (not measurement quantities or specifications) are checked in the procedure; therefore, a minimum amount of test equipment is required. If performing the Operators Checkout Procedure reveals improper performance or instrument malfunction, check the operation of associated equipment; then refer to qualified service personnel for repair or adjustment of the instrument.

TEST EQUIPMENT REQUIRED

The test equipment listed below was used in preparing the Operators Checkout Procedure. Other test equipment which meets these requirements may be substituted. When other equipment is substituted, the control settings or setup may need to be altered.

a. Tektronix 5B25N Digitizer Time-Base unit, 5A45 Amplifier unit, and a 5A48 or 5A38 Dual Trace Amplifier unit.

b. Cables (2 Required)

Description: Length, 42 inches; connectors, bnc.

Type Used: Type RG-58/U, 50-ohm coaxial, Tektronix part 012-0057-01.

c. T Connector

Description: Connectors, bnc to bnc.

Type Used: Bnc to bnc connector, Tektronix Part 103-0030-00.

PRELIMINARY SETUP

1. Set the front-panel controls as follows:

INTENSITY	2 o'clock
FOCUS	midrange
MEM INTEN	counterclockwise
GRAT ILLUM	counterclockwise
POWER	(pushbutton in)
MEMORY CONTENTS	all pushbuttons out
VERT POSN	midrange
HORIZ POSN	midrange
VERT EXP	X1 (counterclockwise)
HORIZ EXP	X1 (counterclockwise)

2. Check that the instrument rear-panel Line Voltage Selector setting (see Fig. 2-3) corresponds to the power available (both voltage and frequency), and connect the 5223 to the power source. (For more information, see Operating Power Information in the General Information section of this manual.)

[1] Refer to Table 1-9, 5223 Plug-In Incompatibilities in this manual for operating restrictions concerning a particular plug-in unit, when used in the 5223 Digitizing Oscilloscope.

3. Install 5A-series amplifier units in the left and right vertical plug-in compartments. Install a 5B-series digitizer time-base unit in the horizontal plug-in compartment.

4. Pull the POWER switch out.

5. Set the time-base unit to 1 millisecond/division (magnifier to X1) and triggering to auto mode with ac coupling from the right source.

6. Set the left and right vertical plug-in unit display switches in. If plug-in is a dual-trace unit, select only one channel.

7. Press the BEAMFINDER switch and position the displayed traces to the center of the crt graticule with the left, right, and time-base plug-in units' position controls. Release the BEAMFINDER switch.

8. Rotate the INTENSITY control until the display is at a desirable viewing level.

9. Connect a bnc cable from the CALIBRATOR output to the input of the right vertical plug-in unit, and set the deflection factor to 0.1 volts/division (for a three division display).

10. Set the time-base unit triggering slope to +, from the right source, and adjust trigger level for a stable display.

Display Focus

11. Rotate the FOCUS control and observe the square-wave display. Notice that the thickness of the trace varies. Set the FOCUS control for a well-defined trace.

Graticule Illumination

12. Rotate the GRAT ILLUM control throughout its range and notice that the graticule lines are illuminated as the control is turned clockwise.

Vertical Deflection System

13. Connect the CALIBRATOR output to the input connectors of both amplifier units with two bnc cables and a bnc T connector. Set the deflection factor of the left amplifier unit to display about 3 divisions of signal on the crt.

14. Position the displayed waveform to the upper half of the graticule, with the left amplifier unit position control.

15. Position the displayed waveform to the lower half of the graticule, with the right amplifier position control.

16. Set the time-base unit Display switch to ALT. Two traces should be displayed on the crt. The top trace is produced by the left amplifier unit and the bottom trace is produced by the right amplifier unit; the sweep for both traces is produced by the time-base unit. Set the sweep rate of the time-base unit to 50 milliseconds/division; notice the display alternates between the left and right amplifier plug-in units, after each sweep. Turn the time-base sweep rate switch throughout its range; notice that the display alternates between amplifier units at all sweep rates.

17. Set the time-base unit Display switch to CHOP. Rotate the time-base unit sweep rate switch throughout its range. A dual-trace display should be presented at all sweep rates. Notice that both amplifier units are displayed by the time-base unit on a time-sharing basis. Set the time-base unit sweep rate to 1 millisecond/division.

18. Position the start of the traces to the left graticule line with the time-base unit position control.

Triggering

19. Set the time-base unit triggering source switch to left and adjust the triggering slope control for a stable display. Disconnect the input signal from the right amplifier unit input connector. Notice that the remaining display is stable.

20. Set the time-base unit Triggering Source switch to Right. Notice that the display is unstable.

21. Remove the calibrator signal from the left amplifier unit and connect it to the input of the right amplifier unit. Notice that the display is again stable.

Memory Contents

22. Set the MEMORY CONTENTS RIGHT VERT PLUG-IN DISPLAY switch to the in position, notice that the switch is illuminated and that there are two square-waves displayed on the crt. (The MEMORY CONTENTS VERT POSN and MEM INTEN control may have to be rotated to obtain a memory display on the crt.)

23. Set the time-base unit sweep rate to 0.1 millisecond/division and notice that one cycle is displayed for 10 divisions.

24. Set the MEMORY CONTENTS RIGHT VERT PLUG-IN SAVE switch to the in position.

25. Set the time-base unit sweep rate to 1 millisecond/division and notice that the memory display remains the same while the real-time display changes to one cycle/division.

26. Disconnect the bnc cable from the input of the right amplifier plug-in unit and notice that the memory display is retained even through the real-time signal is removed.

27. Set the MEMORY CONTENTS RIGHT VERT PLUG-IN DISPLAY switch to the out position and notice the stored display disappears.

28. Set the MEMORY CONTENTS RIGHT VERT PLUG-IN DISPLAY switch to the in position and notice that the stored display reappears.

29. Press the MEMORY CONTENTS OUTPUT SAVED DISPLAY(S) switch and notice that the stored display disappears and then reappears after a period of time determined by the DISPLAY OUT SPEED control (see Fig. 2-3).

30. Set the MEM INTEN control fully clockwise. Set the MEMORY CONTENTS VECTOR MODE switch to the in position and notice that the rising and falling edges of the signal brighten.

31. Set the time-base unit sweep rate to 0.5 seconds/division.

32. Set the MEMORY CONTENTS RIGHT VERT PLUG-IN SAVE switch to the out position.

33. Rotate the right vertical plug-in unit position control so the dot moves up and then down approximately two divisions as the spot crosses the crt. Notice that the stored display is updated after the dot reaches the right side of the crt.

34. Set the MEMORY CONTENTS ROLL switch in. Rotate the right vertical plug-in unit position control so the dot moves up and then down approximately two divisions and notice that the display is continually updated at the right side of the crt while the display moves from right to left.

35. Set all of the MEMORY CONTENTS switches to the out position.

36. Connect the calibrator signal to the input of the left amplifier unit.

37. Set the time-base unit sweep rate to 0.1 millisecond/division and triggering for ac coupling from the left source.

38. Set the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY switch to the in position, notice that the switch is illuminated and that there are two square-waves displayed on the crt. (The MEMORY CONTENTS VERT POSN and MEM INTEN controls may have to be rotated to obtain a memory display on the crt).

39. Set the MEMORY CONTENTS LEFT VERT PLUG-IN SAVE switch to the in position.

40. Set the time-base unit sweep rate to 1 millisecond/division and notice that the memory display remains the same while the real-time display changes to one cycle/division.

41. Disconnect the bnc cable from the input of the left amplifier plug-in unit and notice that the memory display is retained even though the real-time signal is removed.

42. Set the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY switch to the out position and notice that the stored display disappears.

43. Set the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY switch to the in position and notice that the stored display reappears.

44. Press the MEMORY CONTENTS OUTPUT SAVED DISPLAY(S) switch and notice that the stored display disappears and then reappears, after a period of time determined by DISPLAY OUT SPEED control.

45. Set the time-base unit sweep rate to 0.5 seconds/division.

46. Set the MEMORY CONTENTS LEFT PLUG-IN SAVE switch to the out position.

47. Rotate the left vertical plug-in unit position control so the dot moves up and then down approximately two divisions as the spot crosses the crt. Notice that the stored display is updated after the dot reaches the right side of the crt.

48. Set the MEMORY CONTENTS ROLL switch in.

49. Rotate the left vertical plug-in unit position control so the dot moves up and then down approximately two divisions as the spot crosses the crt. Notice that the display is continually updated at the right side of the crt and that the display moves from right to left.

50. Set the time-base unit sweep rate to 1 millisecond/division.

51. Set the MEMORY CONTENTS L VS R switch to the in position. Notice that the left plug-in amplifier unit position control positions the dot vertically and the right amplifier plug-in unit position control positions the dot horizontally.

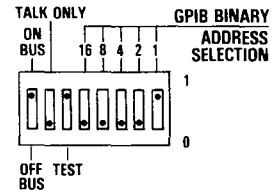
GPIB

52. Turn off the power to the 5223 and connect the 5223 to a Tektronix 4050-series GPIB controller using a GPIB cable.

53. Set the 5223 rear-panel GPIB Address Selection switches as shown in Figure 2-7.

54. Enter the program shown in Figure 2-7 into the 4050-series controller.

55. Set all MEMORY CONTENTS switches to the out position.




```
100 POLL A1,A2;1
110 DIM A$(5500)
120 PRINT @1:"ACCESS LEFT;ASCII;CURVE?"
130 INPUT @1:A$
140 PRINT @1:"WFMPRE WFID:R;";A$
150 END
```

3715-207

Figure 2-7. Operators GPIB checkout setup and program.

56. Connect the calibrator signal to the left amplifier unit.

57. Pull the POWER switch out.

58. Press the LEFT VERT PLUG-IN SAVE and DISPLAY buttons.

59. Turn the INTENSITY control fully counter-clockwise and adjust the MEM INTEN control for a usable display.

60. Execute the program (entered in step 54) by typing the RUN command.

61. Observe that the RIGHT VERT PLUG-IN SAVE button is illuminated.

62. Set the LEFT VERT PLUG-IN DISPLAY button to the out position.

63. Press the RIGHT VERT PLUG-IN DISPLAY button and observe that the display returns.

64. Press the LEFT VERT PLUG-IN DISPLAY button and observe that the two displayed waveformrs match.

65. Press the POWER switch in.

This completes the Operators Checkout procedure.

BASIC OSCILLOSCOPE MEASUREMENT TECHNIQUES

The oscilloscope is a unique and versatile measuring device in that it allows you to view the signals you are measuring. Certain measurement techniques basic to oscilloscope use are described in the following pages. However, these measurement techniques are not described in detail since each application must be adapted to the requirements of the individual measurement. Also, the 5223 Digitizing Oscilloscope is host to a variety of plug-in units; you will find specific applications for these plug-in units described in the instruction manuals for these units. Contact your local Tektronix Field Office or representative for additional assistance.

For a more comprehensive study of oscilloscope measurement techniques, we suggest the following books that describe oscilloscope measurement techniques which can be adapted for use with this instrument.

Robert G. Middleton, *Scope Waveform Analysis*, Howard W. Sams & Co. Inc., The Bobbs-Merrill Company Inc., Indianapolis, 1961.

Robert G. Middleton and L. Donald Payne, *Using the Oscilloscope in Industrial Electronics*, Howard W. Sams & Co., Inc., The Bobbs-Merrill Company Inc., Indianapolis, 1961.

John F. Rider and Seymour D. Uslan, *Encyclopedia of Cathode-Ray Oscilloscopes and Their Uses*, John F. Rider Publisher Inc., New York, 1959.

John F. Rider, *Obtaining and Interpreting Test Scope Traces*, John F. Rider Publisher Inc., New York, 1959.

Rufus P. Turner, *Practical Oscilloscope Handbook*, Volumes 1 and 2, John F. Rider Publisher Inc., New York, 1964.

PEAK-TO-PEAK VOLTAGE MEASUREMENTS—AC

The oscilloscope allows you to make very accurate peak-to-peak voltage measurements. The following procedure takes you step-by-step through the measurement process.

1. Set the input coupling on the vertical plug-in unit to Gnd and connect the signal to the input connector.

2. Set the input coupling to AC and set the Volts/Div switch to display about 5 or 6 vertical divisions of the waveform. Check that the variable Volts/Div control (red knob) is in the Cal position.

3. Adjust the time-base triggering controls for a stable display and set the Time/Div switch to display several cycles of the waveform.

4. Turn the vertical Position control so that the lower portion of the waveform coincides with one of the graticule lines below the center horizontal line, and the top of the waveform is in the viewing area. Move the

display with the horizontal Position control so that one of the upper peaks is aligned with the center vertical reference line (see Fig. 2-8).

5. Measure the vertical deflection from peak-to-peak (divisions).

NOTE

This technique may also be used to make measurements between two points of the waveform, rather than peak-to-peak.

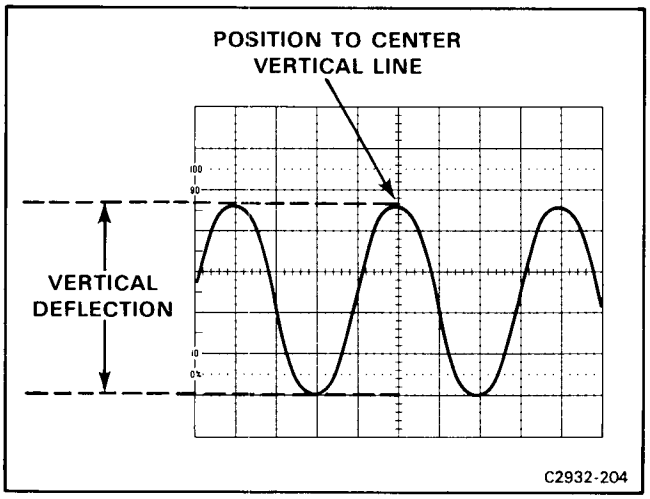


Figure 2-8. Measuring peak-to-peak voltage of a waveform.

6. Multiply the distance (in divisions) measured in step 5 by the Volts/Div switch setting. Also include the attenuation factor of the probe, if applicable.

EXAMPLE: Assume a peak-to-peak vertical deflection of 4.6 divisions and a Volts/Div switch setting of 5 V.

$$\underset{\text{(divisions)}}{4.6} \times \underset{\text{(Volts/Div setting)}}{5} = \underset{\text{peak-to-peak}}{23 \text{ volts}}$$

NOTE

If an attenuator probe is used that cannot change the scale factor readout (Volts/Div), multiply the right side of the above equation by the attenuation factor.

INSTANTANEOUS VOLTAGE MEASUREMENT—DC

The oscilloscope simplifies the task of determining the dc level at any particular point on a waveform. This measurement is accomplished as described below:

1. Set the input coupling of the vertical plug-in unit to Gnd and position the trace to one division above the bottom line of the graticule (or other selected reference line). If the voltage to be measured is negative with respect to ground, position the trace one division below the top line of the graticule. Do not move the vertical Position control after this reference has been established.

NOTE

To measure a voltage level with respect to a voltage other than ground, make the following changes to step 1: Set the input coupling switch to dc and apply the reference voltage to the input connector; then position the trace to the reference line.

2. Connect the signal to the input connector. Set the input coupling to dc (the ground reference can be checked at any time by setting the input coupling to Gnd).

3. Set the Volts/Div switch to display about 5 or 6 vertical divisions of the waveform. Check that the variable Volts/Div control (red knob) is in the Cal position. Adjust the time-base triggering controls for a stable display.

4. Measure the distance in divisions between the reference line and the point on the waveform at which the dc level is to be measured. For example, in Figure 2-9 the measurement is made between the reference line and point A.

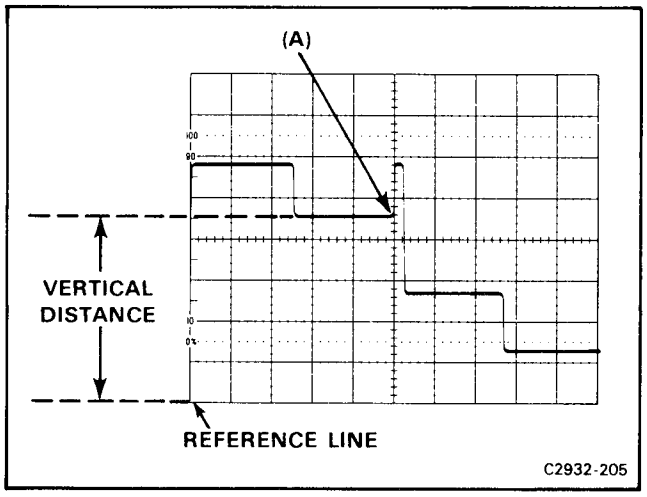


Figure 2-9. Measuring instantaneous dc voltage with respect to a reference voltage.

5. Establish the polarity; the voltage is positive if the signal is applied to the + input connector and the waveform is above the reference line.

6. Multiply the distance measured in step 4 by the Volts/Div switch setting. Include the attenuation factor of the probe, if applicable (see the note following the Peak-to-Peak Voltage Measurement example given previously).

EXAMPLE: Assume that the vertical distance measured is 4.6 divisions, the polarity is positive, and the Volts/Div switch setting is 2 V.

$$\underset{\text{(divisions)}}{4.6} \times \underset{\text{(Volts/Div)}}{2} = \underset{\text{instantaneous}}{+9.2 \text{ volts}}$$

COMPARISON MEASUREMENTS

In some applications, you may need to establish a set of deflection factors other than those indicated by the Volts/Div or Time/Div switches. This is useful for comparing signals to a reference voltage amplitude or period. To establish a new set of deflection factors based upon a specific amplitude or period, proceed as follows:

Vertical Deflection Factor

1. Apply a reference signal of known amplitude to the vertical connector. Using the Volts/Div switch and variable Volts/Div control, adjust the display for an exact number of divisions. Do not move the variable Volts/Div control after obtaining the desired deflection.

2. Divide the amplitude of the reference signal (volts) by the product of the deflection in divisions (established in step 1) and the Volts/Div switch setting. This is the Deflection Conversion Factor.

$$\text{Deflection Conversion Factor} = \frac{\text{reference signal amplitude (volts)}}{\text{deflection (divisions)} \times \text{Volts/Div setting}}$$

3. To determine the peak-to-peak amplitude of a signal compared to a reference, disconnect the reference and apply the signal to the input connector.

4. Set the Volts/Div switch to a setting that provides sufficient deflection to make the measurement. Do not readjust the variable Volts/Div control.

5. To establish a modified deflection factor at any setting of the Volts/Div switch, multiply the Volts/Div switch setting by the Deflection Conversion Factor established in step 2.

$$\text{Modified Deflection Factor} = \text{Volts/Div setting} \times \text{Deflection Conversion Factor}$$

6. Measure the vertical deflection in divisions and determine the amplitude by the following formula:

$$\text{Signal amplitude} = \text{Modified Deflection Factor} \times \text{Deflection (divisions)}$$

EXAMPLE: Assume a reference signal amplitude of 30 volts, a Volts/Div switch setting of 5 V and a deflection of four divisions. Substituting these values in the Deflection Conversion Factor formula (step 2):

$$\frac{30 \text{ V}}{(4)(5 \text{ V})} = 1.5$$

Then, with a Volts/Div switch setting of 2 V, the Modified Deflection Factor (step 5) is:

$$(2 \text{ V})(1.5) = 3 \text{ volts/division}$$

To determine the peak-to-peak amplitude of an applied signal that produces a vertical deflection of five divisions with the above conditions, use the Signal Amplitude formula (step 6):

$$(3 \text{ V})(5) = 15 \text{ volts}$$

Sweep Rate

1. Apply a reference signal of know frequency to the vertical input connector. Using the Time/Div switch and variable Time/Div control, adjust the display so that one cycle of the signal covers an exact number of horizontal divisions. Do not change the variable Time/Div control after obtaining the desired deflection.

2. Divide the period of the reference signal (seconds) by the product of the horizontal deflection in divisions (established in step 1) and the setting of the Time/Div switch. This is the Deflection Conversion Factor.

$$\text{Deflection Conversion Factor} = \frac{\text{reference signal period (seconds)}}{\text{horizontal deflection (divisions)} \times \text{Time/Div switch setting}}$$

3. To determine the period of an unknown signal, disconnect the reference and apply the unknown signal.

4. Set the Time/Div switch to a setting that provides sufficient horizontal deflection to make an accurate measurement. Do not readjust the variable Time/Div control.

5. To establish a Modified Deflection Factor at any setting of the Time/Div switch, multiply the Time/Div switch setting by the Deflection Conversion Factor established in step 2.

$$\text{Modified Deflection Factor} = \text{Time/Div switch setting} \times \text{Deflection Conversion Factor}$$

6. Measure the horizontal deflection in divisions and determine the period by the following formula:

$$\text{Period} = \text{Modified Deflection Factor} \times \text{horizontal deflection (divisions)}$$

EXAMPLE: Assume a reference signal frequency of 455 hertz (period 2.2 milliseconds), a Time/Div switch setting of 0.2 millisecond, and a horizontal deflection of eight divisions. Substituting these values in the Deflection Conversion Factor formula (step 2):

$$\frac{2.2 \text{ ms}}{(8)(0.2 \text{ ms})} = 1.375$$

@

Then, with a Time/Div switch setting of 50 ms, the Modified Deflection Factor (step 5) is:

(50 ms) (1.375) = 68.75 milliseconds/division

To determine the time period of an applied signal which completes one cycle in seven horizontal divisions, use the Period formula (step 6):

(68.75 ms) (7) = 481 milliseconds

This product can be converted to frequency by taking the reciprocal of the period (see application of Determining Frequency).

TIME PERIOD MEASUREMENT

The oscilloscope provides you with an easy way to determine the time (period) between two points on a waveform. Follow the procedure given below:

1. Connect the signal to the vertical input connector, select either AC or DC input coupling, and set the Volts/Div switch to display about four divisions of the waveform.

2. Set the time-base triggering controls to obtain a stable display. Set the Time/Div switch to the fastest sweep rate that will permit displaying one cycle of the waveform in less than eight divisions (some nonlinearity may occur in the first and last graticule divisions of display). Refer to Figure 2-10.

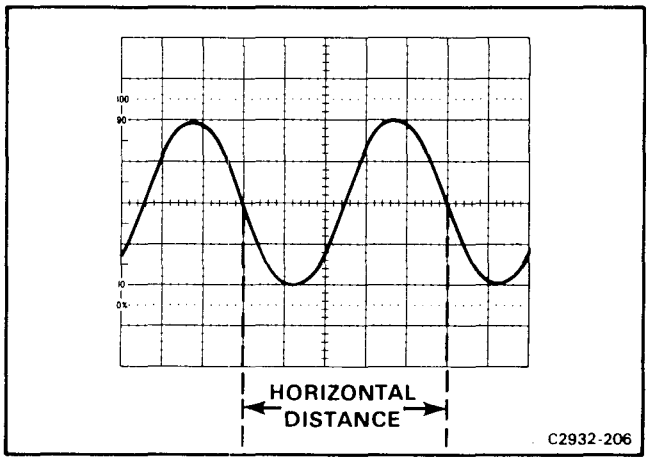


Figure 2-10. Measuring time duration (period) between points on a waveform.

3. Rotate the vertical Position control to center the displayed waveform on the center horizontal graticule line. Adjust the horizontal Position control to center the time-measurement points within the center eight divisions of the graticule.

4. Measure the horizontal distance between the time measurement points. Be sure the variable Time/Div control is in the Cal position.

5. Multiply the distance measured in step 4 by the setting of the Time/Div switch.

EXAMPLE: Assume that the horizontal distance between the time-measurement points is five divisions and the Time/Div switch is set to 0.1 millisecond. Using the formula:

$$\text{horizontal distance (divisions)} \times \text{Time/Div switch setting} = (5)\,(0.1\text{ ms}) = 0.5\text{ ms}$$

The period is 0.5 millisecond.

DETERMINING FREQUENCY

The time measurement technique can also be used to determine the frequency of a signal. The frequency of a periodically recurrent signal is the reciprocal of the time duration (period) of one cycle. Use the following procedure:

1. Measure the period of one cycle of the waveform as described in the previous application.

2. Take the reciprocal of the period to determine the frequency.

EXAMPLE: The frequency of the signal shown previously in Figure 2-10, which has a period of 0.5 millisecond, is:

$$\frac{1}{\text{period}} = \frac{1}{0.5\text{ ms}} = 2\text{ kilohertz}$$

RISE-TIME MEASUREMENT

Rise-time measurements employ basically the same techniques as the time-period measurements. The main difference is the points between which the measurement is made. The following procedure gives the basic method of measuring rise-time between the 10% and 90% points of the waveform.

1. Connect the signal to the input connector.

2. Set the Volts/Div switch and variable Volts/Div control to produce a display exactly five divisions in amplitude.

3. Center the display about the center horizontal graticule line with the vertical Positions control.

4. Set the time-base triggering controls to obtain a stable display. Set the Time/Div switch to the fastest sweep rate that will display less than eight divisions between the 10% and 90% points on the waveform (see Fig. 2-11).

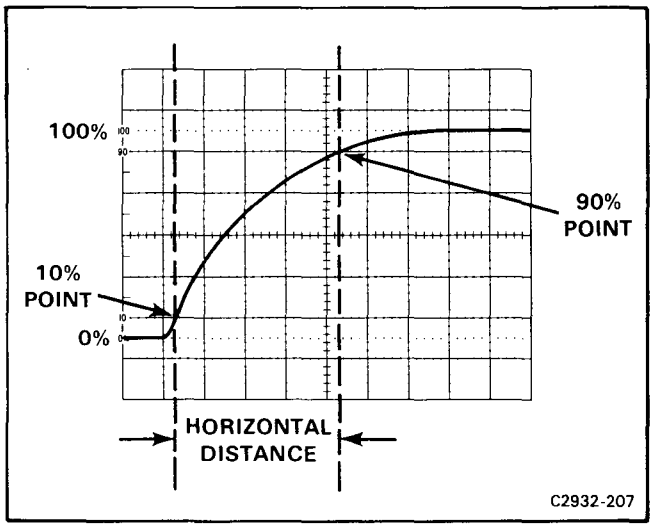


Figure 2-11. Measuring risetime.

5. Adjust the horizontal Position control to move the 10% point of the waveform near the second vertical line of the graticule.

6. Measure the horizontal distance between the 10% and 90% points. Be sure the variable Time/Div control is in the Cal position.

7. Multiply the distance measured in step 6 by the setting of the Time/Div switch.

EXAMPLE: Assume that the horizontal distance between the 10% and 90% points is four divisions and the Time/Div switch is set to 1 ms.

Using the period formula to find rise time:

horizontal distance (division)	×	Time/Div switch setting	=	(4) (1 ms) = 4 ms

The rise time is 4 milliseconds.

TIME DIFFERENCE MEASUREMENTS

When used in conjuction with a calibrated time-base plug-in unit, the multi-trace feature of the 5223 Digitizing Oscilloscope allows you to measure the time difference between two or more separate events. (For information on X-Y measurements refer to the L VS R discussion in Section 2 of this manual.) To measure time difference, use the following procedure:

1. Set the input coupling switches of the amplifier channels to either AC or DC.

2. Set the Display switch on the time-base unit to either Chop or Alt. In general, Chop is more suitable for low-frequency signals. More information on determining the mode is given under Vertical Display Mode in Section 2 of this manual.

3. Set the vertical plug-in triggering switches to trigger the display on channel 1 (or left plug-in).

4. Connect the reference signal to the channel 1 input connector and the comparison signal to the channel 2 (or center plug-in) input connector. The reference signal should precede the comparison signal in time. Use coaxial cables or probes which have similar time-delay characteristics to connect the signal to the input connectors. Trigger the time base on the reference signal.

5. If the signals are of oppostie polarity, invert the channel 2 (or center plug-in) display. (Signals may be of opposite polarity due to 180 degree phase difference; if so, take this into account in the final calculation.)

6. Set the Volts/Div switches to produce about four divisions of displayed waveform.

7. Set the time-base triggering controls for a stable display. Set the Time/Div switch for a sweep rate which shows three or more divisions between the measurement points, if possible; make sure that the Variable Time/Div control is in the Cal position.

8. Adjust the vertical Position controls to bring the measurement points to the center horizontal reference line.

9. Adjust the horizontal Position control so the channel 1 (or left plug-in) waveform (reference) crosses the center horizontal line at a vertical graticule line.

10. Measure the horizontal distance between the two measurement points (see Fig. 2-12).

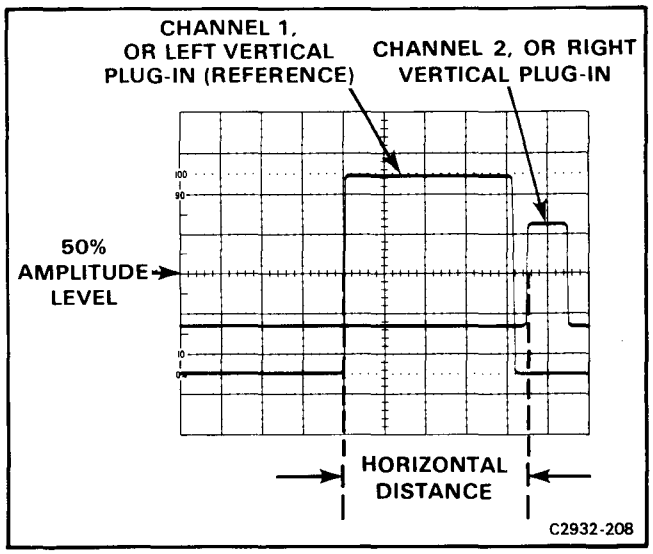


Figure 2-12. Measuring time difference between two pulses.

11. Multiply the measured distance by the setting of the Time/Div switch.

EXAMPLE: Assume that the Time/Div switch is set to 50 ms and the horizontal distance between measurement points is four divisions. Using the formula:

Time/Div switch setting × horizontal distance (divisions) = (50 ms) (4.5) = 200 ms

The time delay is 200 milliseconds.

MULTI-TRACE PHASE DIFFERENCE MEASUREMENT

With the oscilloscope you can easily make phase comparisons between two or more signals of the same frequency. For this you will need an input for each signal (use either a dual-trace plug-in or two single trace plug-ins). This method of phase difference measurements can be used up to the frequency limit of the vertical system. To make the comparison, use the following procedure:

1. Set the input coupling switches of the amplifier channels to either AC or DC.

2. Set the Display switch on the time-base unit to either Chop or Alt. In general, Chop is more suitable for low-frequency signals and the Alt position is more suitable for high-frequency signals. More information on determining the mode is given under Vertical Display Mode in Section 2 of this manual.

3. Set the vertical plug-in triggering switches to trigger the display on channel 1 (or left plug-in).

4. Connect the reference signal to the channel 1 input connector and comparison signal to the channel 2 (or center plug in) input connector. The reference signal should precede the comparison signal in time. Use coaxial cables or probes which have similar time-delay characteristics to connect the signals to the input connectors.

5. If the signals are of opposite polarity invert channel 2 (or center plug-in) display. (Signals may be of opposite polarity due to 180 degree phase difference; if so, take this into account in the final calculation.)

6. Set the Volts/Div switches and the variable Volts/Div controls so the displays are equal and about five divisions in amplitude.

7. Set the time-base triggering controls to obtain a stable display. Set the Time/Div switch to a sweep rate which displays about one cycle of the waveform.

8. Move the waveforms to the center of the graticule with the vertical Position controls.

9. Turn the variable Time/Div control until one cycle of the reference signal (channel 1, or left plug-in) occupies exactly eight divisions between the second and tenth vertical lines of the graticule (see Fig. 2-13).

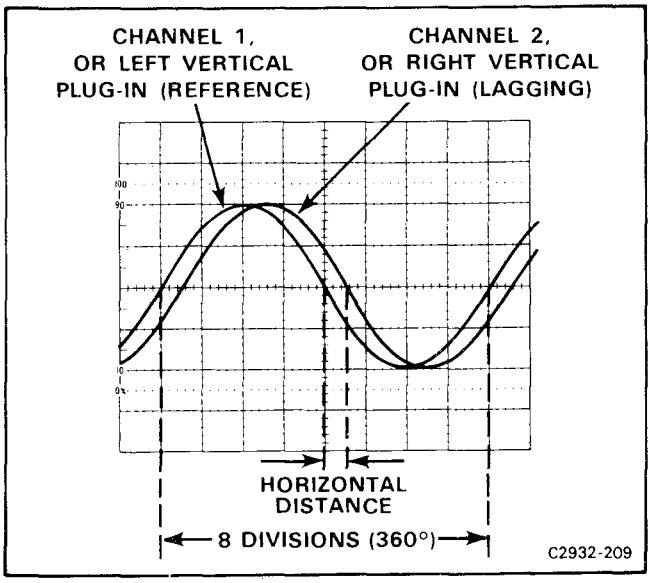


Figure 2-13. Measuring phase difference.

Each division of the graticule represents 45 degrees of the cycle (360 degrees divided by 8 divisions = 45 degrees/division). The sweep rate can be stated in terms of degrees as 45 degree/division.

10. Measure the horizontal difference (in divisions) between corresponding points on the waveforms.

11. Multiply the measured distance (in divisions) by 45 degrees/division (sweep rate) to obtain the exact amount of phase difference.

EXAMPLE: Assume a horizontal difference of 0.6 division with a sweep rate of 45 degrees/division as shown in Figure 2-13. Use the formula:

horizontal difference (divisions) × sweep rate (degrees/ divisions) = (0.6) (45 degrees) = 27 degrees

The phase difference is 27 degrees.

HIGH RESOLUTION PHASE MEASUREMENT

More accurate dual-trace phase measurements can be made by increasing the sweep rate (without changing the variable Time/Div control setting). One of the easiest ways to increase the sweep rate is with the sweep magnifier (X10) button on the time-base unit. The magnified sweep rate is automatically indicated by the knob-skirt scale-factor readout.

EXAMPLE: If the sweep rate were increased 10 times with the magnifier, the magnifier sweep rate should be 45 degrees/division divided by 10 = 4.5 degrees/division. Figure 2-14 shows the same signals as used in Figure 2-13, but with the sweep magnifier button pushed in. With a horizontal difference of six divisions the phase difference is:

$$\text{horizontal difference (divisions)} \times \text{magnified sweep rate (degrees/divisions)} = \frac{(6)}{(4.5 \text{ degrees})} = 27 \text{ degrees}$$

The phase difference is 27 degrees.

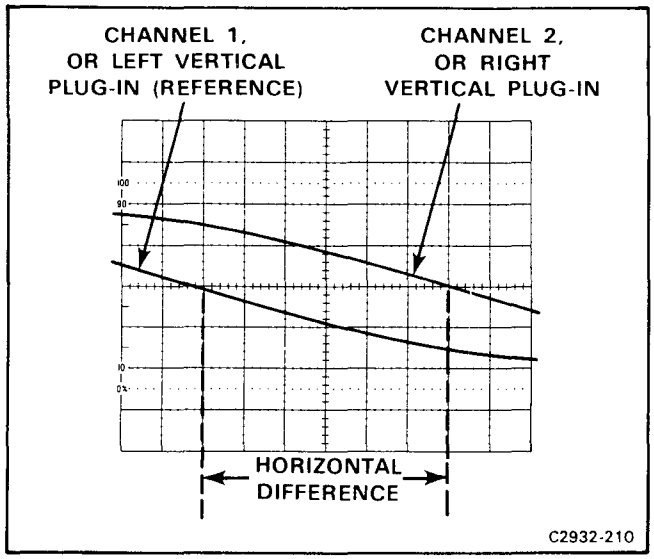


Figure 2-14. High-resolution phase difference measurement with increased sweep rate.

PERMANENT WAVEFORM RECORDS USING AN X-Y PLOTTER

Permanent waveform records are easily made when you connect your 5223 Digitizing Oscilloscope to an external X-Y plotter. Analog voltages, which represent the X and Y components of the 5223 memory contents, are output from connectors on the rear panel of the instrument when you press the OUTPUT SAVED DISPLAY button. By connecting an X-Y plotter to these outputs as described in the procedure below, you can make a permanent copy of any stored waveform simply by pressing the OUTPUT SAVED DISPLAY button. To use this feature of your 5223 Digitizing Oscilloscope, first perform the setup shown in Figure 2-15, then proceed with the numbered instructions.

1. Use the Position controls of the left and center amplifiers to center the two waveforms on the 5223 graticule area.

2. Press the 5223 MEMORY CONTENTS LEFT PLUG-IN DISPLAY switch and the L VS R switch.

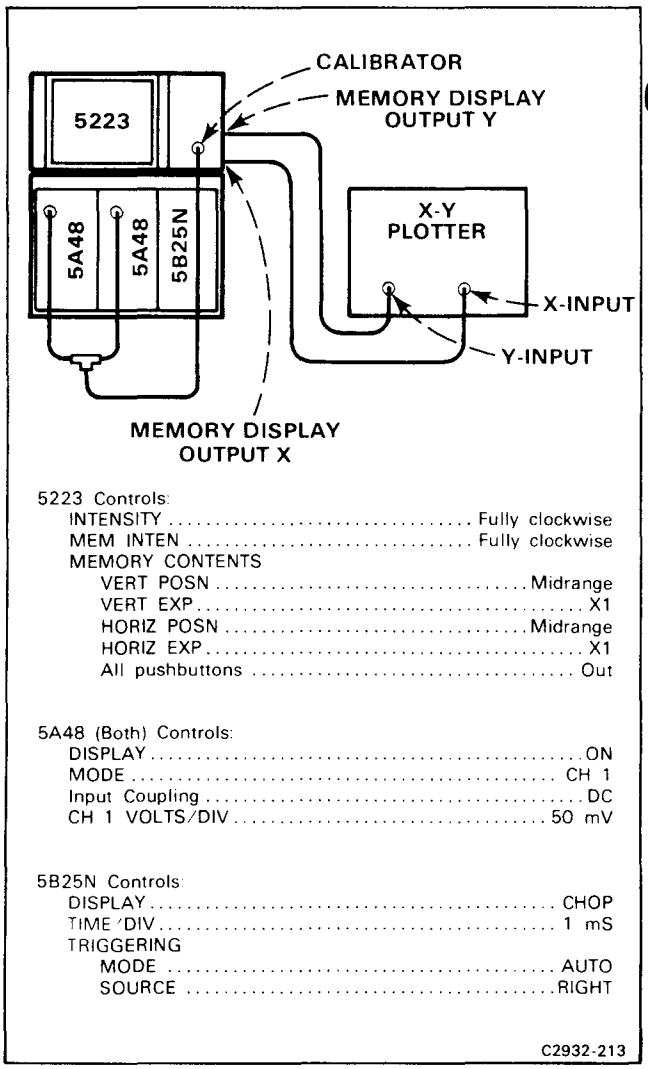


Figure 2-15. Setup for operation of an X-Y Plotter with the 5223.

3. Rotate the 5223 INTENSITY control fully counterclockwise.

4. Place graph paper on the X-Y plotter.

5. Use the 5223 MEMORY CONTENTS HORIZ POSN control to horizontally center the two dots displayed on the crt.

6. Use the 5223 MEMORY CONTENTS VERT POSN control to position the two displayed dots three divisions below the center graticule line.

7. Press the 5223 MEMORY CONTENTS LEFT PLUG-IN SAVE switch, then press the MEMORY CONTENTS OUTPUT SAVED DISPLAY(S) switch and set the X-Y plotter controls for desired "X" deflection of the pen movement.

8. Press and release the MEMORY CONTENTS LEFT PLUG-IN DISPLAY and SAVE switches.

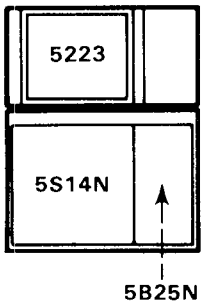
9. Disconnect the bnc cable from the right amplifier input and connect it to the left amplifier input.

10. Press the 5223 MEMORY CONTENTS RIGHT PLUG-IN SAVE switch, then press the MEMORY CONTENTS OUTPUT SAVED DISPLAY(S) switch and set the X-Y plotter controls desired "Y" deflection of the pen movement.

11. See the information in Section 2 of this manual on PEN LIFT operation and refer to the X-Y plotter instruction manual for additional operating information.

HOW TO STORE THE DISPLAY OF A 5S14N SAMPLER UNIT

The 5S14N Dual Trace Delayed Sweep Sampler is a two-wide plug-in unit that normally operates in the center (vertical) and right (horizontal) plug-in compartments of Tektronix 5000-Series mainframes. However, the 5223 Digitizing Oscilloscope requires the installation of a 5B25N Time Base unit in the right (horizontal) compartment in order to store a display in memory. Both these requirements are met in the following special setup procedure which explains how you can use the 5S14N plug-in unit in the left and center compartments of the 5223. And, because a 5B25N is installed in the right horizontal compartment, the display can be saved in memory.



5223 Controls:
- INTENSITY ..... Fully counterclockwise
- MEM INTEN ..... Fully clockwise
- MEMORY CONTENTS
  - LEFT VERT PLUG-IN DISPLAY ..... In
  - All other pushbuttons ..... Out
  - VERT POSN ..... Midrange
  - HORIZ POSN ..... Midrange
  - VERT EXP X1
  - HORIZ EXP X1

5B25N Controls:
- DISPLAY ..... CHOP
- TRIGGERING
  - MODE ..... AUTO
- TIME/DIV ..... 5 ms
  - CAL ..... In detent position

5S14N Controls:
- CHANNEL 1
  - VOLTS/DIV ..... 0.5 V
  - DC OFFSET ..... Midrange
- TIME/DIV ..... 1 μs
  - CAL ..... In detent position
- SCAN
  - EXT Pushbutton ..... In
- SWP Pushbutton ..... IN:DELAYING
- TRIGGERING ..... AUTO TRIG

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Figure 2-16. Setup for operating the 5S14N with the 5223.

1. Perform the setup as shown in Figure 2-16.

2. Press the 5223 MEMORY CONTENTS L VS R switch in.

3. Set the 5223 MEM INTEN control for desired viewing and rotate the 5S14 HORIZ POS control to align the displayed dot on the left-most graticule line.

4. Press the 5S14 SCAN MAN button and rotate the SCAN control to align the dot on the center graticule line.

5. Rotate the 5223 MEMORY CONTENTS VERT POSN CONTROL to align the trace on the center graticule line.

6. Connect a wire from the 5B25N SWP OUT pin connector to 5S14N SCAN EXT input pin connector.

7. Press the 5S14N EXT switch in and rotate the SCAN control so that the trace is 10 divisions in length horizontally.

NOTE

Misadjustment of the 5S14N HORIZ POS control will show a bright spot on either end of the trace; set the 5S14N HORIZ POS control in conjunction with the 5223 MEMORY CONTENTS HORIZ POSN control to eliminate the bright spot at either end of the trace.

8. The 5S14N can now be used normally if the following precautions are observed:

a. The sweep rate of the 5B25N must be adjusted according to Table 2-1, depending upon the Delaying Sweep rate of the 5S14N.

b. Even though the 5S14N is selected for a single trace display the 5223 stores the 5S14N waveforms as dual trace waveforms. This may cause some degradation in the appearance of the display in VECTOR MODE, and will cause the Chart Recorder Output to trace the displayed waveform twice for each output sequence.

c. It may be convenient to select ROLL on the 5223 while setting up the controls on the 5S14N, but the ROLL function should not be used after the setup is completed, or when waveforms are being acquired and saved.

TABLE 2-1
5S14N Sweep Rate vs 5B25N Sweep Rate

Delaying Sweep Rate on 5S14N	Fastest Recommended Sweep Rate on 5B25N[1]
1 μs and Faster	5 ms/div
10 μs to 2 μs	0.1 s/div
100 μs to 20 μs	0.5 s/div

[1]Slower by a factor of 10 if the Lo Noise function of the 5S14N is used; A reduction in sweep rate on 5B25N produces a more usable display on the 5S14N.

d. The 5S14N two-dot time measurement function is inoperable when using the 5S14N in the vertical compartments of the 5223 Digitizing Oscilloscope.

HOW TO STORE THE DISPLAY OF 5L4N SPECTRUM ANALYZER

As in the preceeding application, the 5L4N Spectrum Analyzer is also a two-wide plug-in unit that normally operates in the center (vertical) and right (horizontal) compartments of Tektronix 5000-Series mainframes. And, because display storage in the 5223 mainframe requires that a 5B25N Time Base unit be installed in the right plug-in compartment, a special setup procedure is necessary for storing the 5L4N display. This procedure explains how you can use the 5L4N Spectrum Analyzer installed in the left and center plug-in compartment of the 5223 mainframe, which then allows you to use the 5B25N Time Base unit in the right (horizontal) compartment and threrby store the 5L4N display. The setup procedure for doing this is given below.

1. Perform the setup as shown in Figure 2-17.

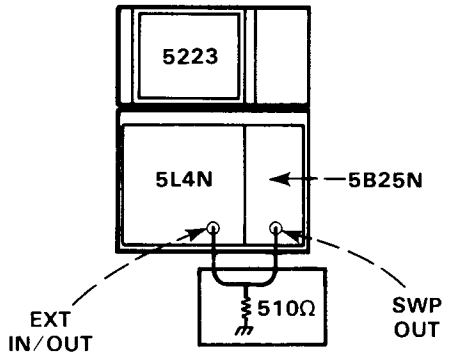
2. Use the 5L4N vertical POSITION control to align the real-time trace with the bottom graticule line.

3. Use the 5B25N POSITION control to align the peak of the start spur waveform on the real-time trace with the left-most graticule line.

4. Use the 5223 VERT POSN control to align the stored trace with the bottom graticule line.

5. Use the 5L4N horizontal POSITION control to set the peak of the start spur waveform (on the stored trace) as close to the left end of the trace as possible, without distorting the start spur waveform.

6. Use the 5223 MEMORY CONTENTS HORIZ POSN control to overlay the stored start spur waveform on the real-time start spur waveform.



5223 Controls:
- INTENSITY ..... Fully clockwise
- MEM INTEN ..... Fully clockwise
- MEMORY CONTENTS
  - LEFT VERT PLUG-IN DISPLAY ..... In
  - RIGHT VERT PLUG-IN DISPLAY ..... In
  - L VS R ..... In
  - VECTOR MODE ..... In
  - All other switches ..... Out
  - VERT POSN ..... Midrange
  - HORIZ POSN ..... Fully clockwise
  - VERT EXP X1
  - HORIZ EXP X1

5L4N Controls:
- 10 dB/DIV ..... In
- dBm 600 Ω ..... In
- FREQUENCY 000
- DSPL ON ..... In
- 5K Hz FREQ COMB ..... In
- LOG REF ..... -10
- SCAN/DIV ..... 10 K
- RESOLUTION ..... AUTO
- FREQ MKR ..... In
- 50 mV/DIV ..... In
- Horizontal POSITION ..... Fully clockwise
- SPAN ..... Fully clockwise
- MULTR/MNL ..... Fully clockwise
- All other switches ..... Out

5B25N Controls:
- DISPLAY ..... CHOP
- TIME/DIV ..... 20 ms
- TRIGGERING
  - SOURCE ..... LEFT
  - COUPLING ..... AC
  - MODE ..... AUTO

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Figure 2-17. Setup for operating the 5L4N with the 5223.

NOTE

The 5223 VERT POSN and HORIZ POSN control settings now are properly set; take care to not disturb them.

7. Rotate the 5223 INTENSITY control fully counterclockwise.

8. Connect a bnc cable from the 5L4N ZO=600 Ω (comb generator) connector to the 5L4N INPUT 1 V MAX connector.

9. Use the 5L4N SPAN control to adjust for two comb lines per division on the 5223 graticule and at the same time use the 5L4N horizontal POSITION control to keep the start spur aligned with the left-most graticule line.

10. Rotate the 5223 MEM INTEN control fully counterclockwise and the 5223 INTENSITY control fully clockwise.

11. Use the 5L4N MULTR/MNL control to adjust for two comb lines per division on the 5223 graticule, and at the same time use the 5B25N POSITION control to keep the start spur waveform aligned with the left-most graticule line.

12. Rotate the 5223 MEM INTEN control fully clockwise and check that the two displays overlay each other.

13. The 5L4N/5B25N/5223 system is now operational. For further operating information refer to the operators manual of each instrument.

NOTE

To position the stored display use the 5L4N horizontal POSITION control. To position the real-time display use the 5B25N POSITION control.

APPLICATION OF TALK ONLY MODE

The TALK-ONLY feature of the 5223 Option 10 allows you to use it as a 10-bit, 4-channel, analog-to-digital converter. The 5223 will transmit a continuous stream of data (up to 50 ms/div dual compartment, and 20 ms/div using one compartment) to a controller or a listener such as a mass memory device.

This particular application uses the graphic display of a Tektronix 4052 calculator to serve as the memory unit. The program given below is optimized for recording a single channel of information to a length of 6000 data points. If you esire to record more than one channel, program line 290 must be changed to draw dots only instead of vectors. However, when more channels are plotted the data rate is reduced significantly because of the speed limitations of the 4052.

Operation

Figure 2-18 illustrates how to set-up the 5223 Option 10 for this application. When the rear-panel switch is set to the "ON BUS" position, the digitizers display is disabled so only the real-time display remains. When the 4052 program is executed, it will begin graphing data as it is generated by the 5223. After the screen is full (6000 points plotted) the program repeats.

Program

The program for this application is as follows:

```
100 REM **** DATA LOGGING FROM 5223 TO 4052 DISPLAY ****
110 GOSUB 400
120 ON SRQ THEN 400
130 PAGE
140 N=2000
150 PRINT "I          Vectored Data Display"
160 PRINT "I       ";N;" Points Horizontally"
170 GOSUB 500
180 V=70
190 WINDOW 0,N,-128,128
200 ON EOI THEN 230
210 RBYTE A
220 GO TO 210
230 FOR I=1 TO 3
240 VIEWPORT 10,120,V,V+20
250 MOVE 0,V
260 FOR X=1 TO N
270 RBYTE A,B
280 Y=A-256*(A>127)
290 DRAW X,Y
300 NEXT X
310 V=V-30
320 NEXT I
330 GO TO 120
```

```
400 REM **** SERIAL POLL ROUTINE ****
410 POLL L,S;2
420 RETURN
500 REM **** GENERATE AXES ROUTINE ****
510 WINDOW 0,N,-128,128
520 V=70
530 FOR J=1 TO 3
540 VIEWPORT 10,120,V,V+20
550 V=V-30
560 AXIS N/10,25.6,0,0
570 NEXT J
580 RETURN
```

COMMENTS

This example program is intended to illustrate how the 5223 may be used for continuous data logging via TALK-ONLY. When executed, the 4052 will draw three horizontal graphs plotting a new point as its value is sampled and transfered from the 5223. The 5223 in effect becomes an A-to-D converter for the 4052.

Each plot is a continuation of the previous graph. After all three plots are completed, the program will erase the 4052 screen and start plotting data again.

When used with a 4052, a single channel may graphed at sweep speeds as fast as 1 sec/div at the 5223/5B25N.

The 5223/5b25N however is capable of output speeds comparable to sweeping as fast as 50 msec/div without an overrun condition.

Line 140: 'N' sets the number of data points to be graphed on each horizontal axis.

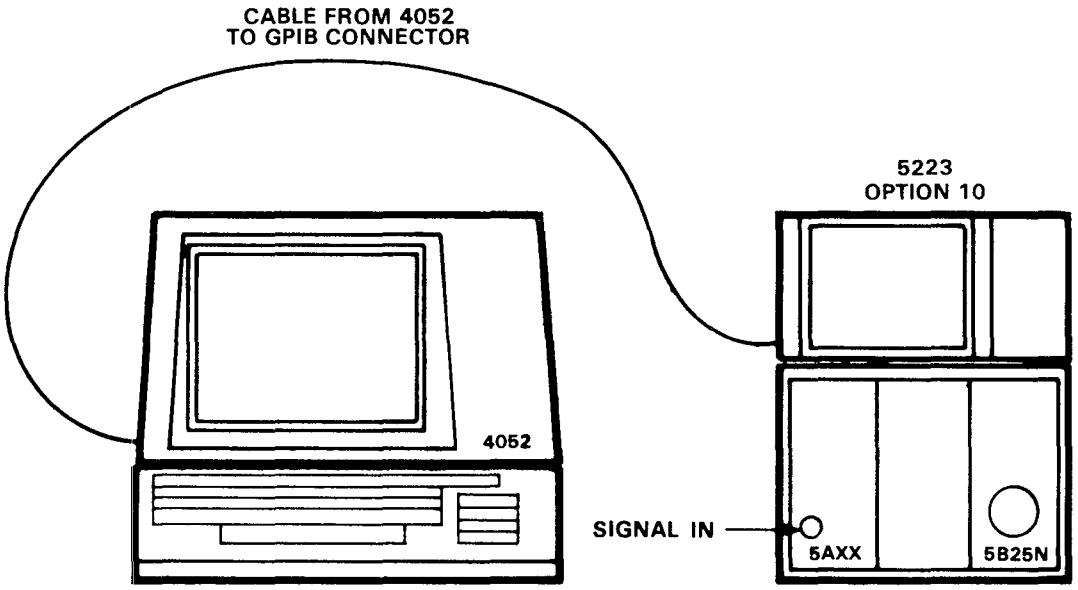
Lines 200-220: Reads data bytes until an EOI is detected to synchronize the byte pairs for each point.

Lines 230-320: Plots the most significant 8-bits of the byte pair A and B.

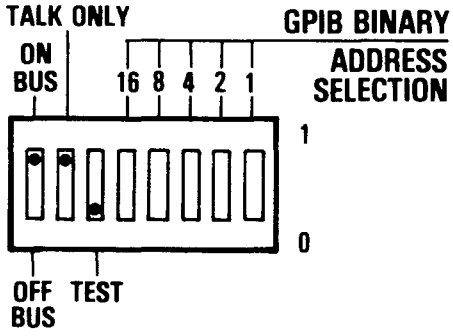
Line 270: Reads in both bytes A and B of the data point.

Line 280: Converts the two's compliment variable A to an offset variable of range + or - 128.

Line 410: Serial Poll of the 5223 at device address 2.



REAR PANEL SWITCH SETTING:



DISPLAY: ..... LEFT

5AXX AMPLIFIER: ..... SELECT SINGLE CHANNEL DISPLAY

5B25N TIMEBASE:
TIME/DIV ..... 1.0 SEC/DIV OR SLOWER

3715-78

Figure 2-18. TEST setup for TALK-ONLY application.

GPIB INFORMATION

The 5223 Option 10 Oscilloscope is equipped with an interface which conforms to **IEEE Standard 488-1978 Digital Interface for Programmable Instrumentation,** commonly referred to as a General Purpose Interface Bus, or GPIB.

The GPIB (Option 10) allows remote operation of the 5223 and waveform-data transfers to and from the 5223.

DESCRIPTION

The GPIB is an interface system using sixteen signal lines; eight data lines, three handshake lines, and five bus management lines. Information is transferred over the bus in a bit-parallel, byte-serial format using an asynchronous "handshake" procedure. This handshake allows communication between instruments with different transfer rates if they conform to the handshake state diagrams and other protocols defined in the IEEE standard. The data transfer rate is effectively limited by the slowest active instrument (talker or listener) on the bus. This ensures the accurate transfer of data to and from all active instruments.

A minimum GPIB system for the 5223 Option 10 Oscilloscope would consist of the 5223 (Option 10) and a GPIB controller (e.g., a Tektronix 4050-series graphic system). The controller directs all command and data transfers on the GPIB.

A larger GPIB system may consist of up to 15 instruments distributed over a total cable length of up to 20 metres. These instruments may include, in addition to the 5223 and controller, other talkers (e.g., counter, digital multimeter, etc.) and other listeners (e.g., line printer, tape drive, programmable signal generator, etc.).

The GPIB system can be connected in either a star or linear configuration, or a combination of both (see Fig. 3-1). To maintain the electrical characteristics of the bus, a device load must be connected for each two metres of cable, and at least half of the devices connected to the bus must be powered up.

GPIB FUNCTIONS

The IEEE Standard 488-1978 defines the GPIB interface functions and the allowed subsets of those functions. The subsets that apply to the 5223 are listed in Table 3-1.

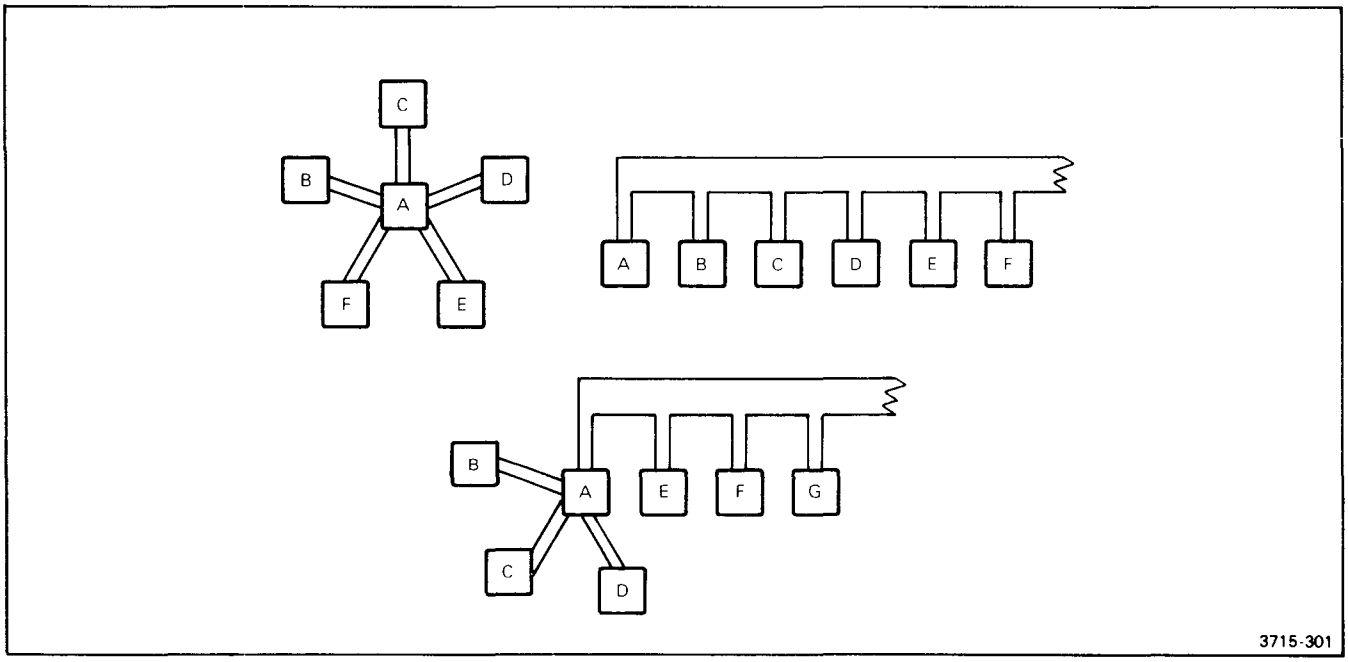


Figure 3-1. GPIB system configuration.

TABLE 3-1
5223 GPIB Interface Functions

Function	Subset	Capability
Source Handshake	SH1	Complete.
Acceptor Handshake	AH1	Complete.
Talker	T5	Complete.
Listener	L4	No Listen Only Mode.
Service Request	SR1	Complete.
Remote/Local	RL2	No Local Lockout.
Parallel Poll	PPØ	None.
Device Clear	DC1	Complete.
Device Trigger	DTØ	None.
Controller	CØ	None.
Bus Drivers	E1	Open Collector Drivers.

ADDRESS SELECTION

The primary GPIB address of the 5223 is set by using the Address selection switches located on the rear panel of the 5223 (see Fig. 3-2). To set the primary GPIB address of the 5223, use a pen or other pointed object to set the binary equivalent of the desired primary address. Any primary address between and including 0 decimal (00000 binary) and 30 decimal (11110 binary) may be used. Do not set 31 decimal (11111 binary) as the primary address; 31 is reserved for use by the controller to "untalk" or "unlisten" a device. (Tektronix 4050-series graphic systems also reserve 0 decimal for another function.)

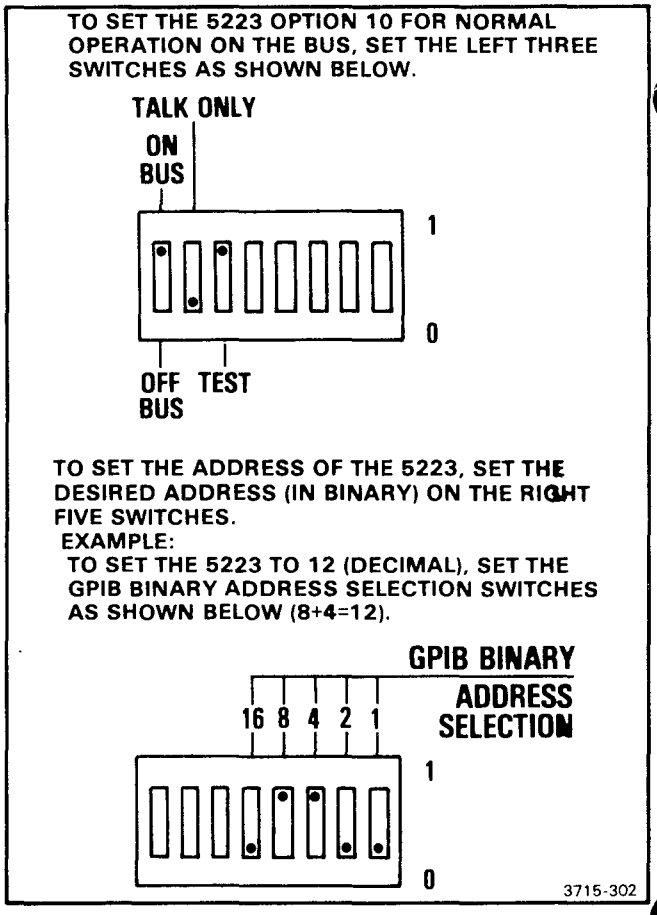


Figure 3-2. Address and Mode Selection.

The remaining three switches select the operating mode of the 5223. The switch section to the left (ON BUS/OFF BUS) connects or disconnects the 5223 from the bus. (One device load is presented to the bus even when the 5223 is OFF BUS.) The other two switch sections allow the 5223 to be used in Talk Only or Test mode. The TALK ONLY switch allows the 5223 to be used as an unaddressed talker in a system without a controller. The TEST switch sets the 5223 into a self-test mode. The TEST function is described in the Maintenance section of this manual.

POWER-UP AND RESET STATES

When the 5223 Option 10 is turned on (with the rear-panel ON BUS/OFF BUS switch in the ON BUS position), a self-test procedure is started to check the 5223 circuitry (See Power-Up Self-Test in Operating Instructions section). On completion of the self test, the 5223 asserts SRQ (Service ReQuest) on the GPIB and sets the On Bus and Powered status byte. (See Service Request in this section.) This SRQ can be cleared by a serial poll.

On completion of the power-up sequence, the 5223 Option 10 defaults are set as if the following commands had been received;

```
WFMPRE WFID:L,NR.PT:1Ø16,PT.OFF:Ø
BINARY
ACCESS LEFT
```

(See the WFMPRE, BINARY, and ACCESS command descriptions for an explaination of these codes.)

The 5223 responds to either a DCL (Device CLear) or SDC (Selected Device Clear) message by aborting any command in progress, and clearing all SRQ's (except Power-on). If an external input command is in progress, the partially filled data area is cleared. If an external output command is in progress, it is terminated.

The IFC (InterFace Clear) message interrupts any data input or output. If the 5223 is talking, it will continue from that point when it is again addressed as a talker. If the 5223 is listening, it will continue inputting data when it is again addressed as a listener.

MESSAGES

All of the many possible messages that may be sent over the GPIB can be split into two major classifications; interface messages or device-dependent messages. Interface messages are sent by the GPIB controller to the other instruments on the bus to control the functions of each instrument's GPIB interface. Device-dependent messages (e.g., instrument commands, data, etc.) may be sent by any instrument on the bus, to any other instrument(s) on the bus as determined by the GPIB controller. (See Fig. 3-3.)

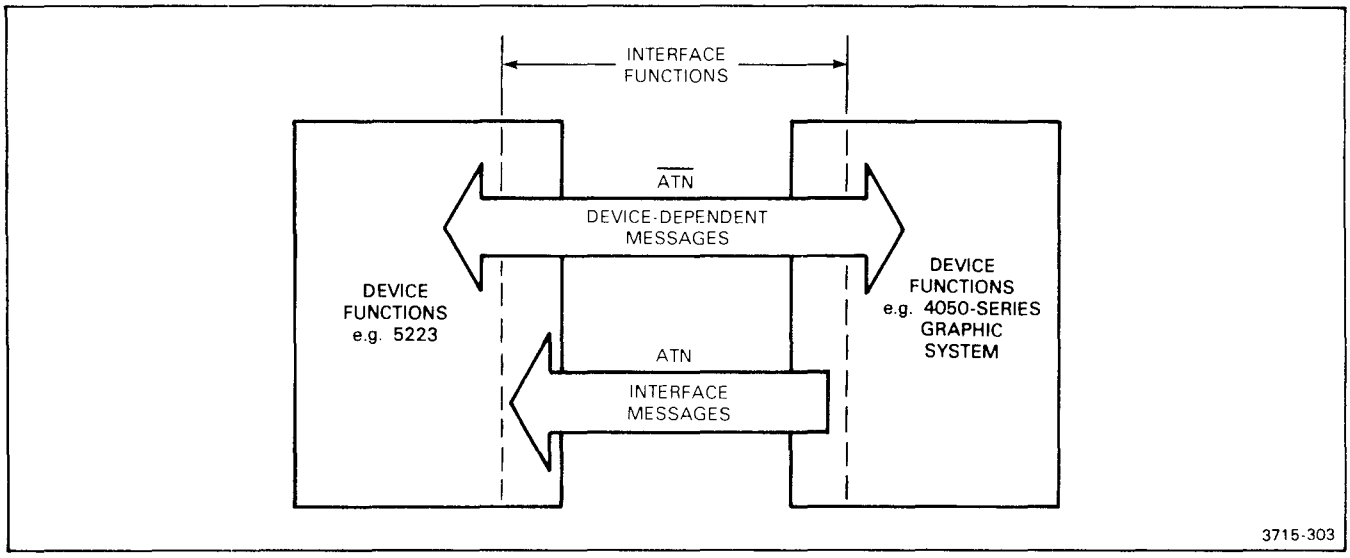


Figure 3-3. Device-Dependent messages vs. interface messages.

GPIB INTERFACE MESSAGES

Interface messages are used by the controller to manage the bus (e.g., designate talkers and listeners, etc.). All instruments on the bus listen to every interface message.

The interface messages that constitute the controller's vocabulary are defined by the standard. They can be thought of as Ascii codes given a new meaning when sent by the controller with the ATtentioN (ATN) line asserted.

Two of the interface messages are the talk and listen addresses. When a device sees its talk address (called My Talk Address or MTA) and ATN simultaneously, it must become a talker. When the controller removes ATN, the device begins the source handshake to transmit its data. Similarly, My Listen Address (MLA) and ATN tells a device to listen to the data sent by a talker.

The controller uses other kinds of interface messages for other tasks. One is the Serial Poll Enable message (SPE) used with the service request function. Suppose an instrument is designed to assert SRQ when it has acquired some data. The controller must poll the devices to find the interrupting device since any one, or more than one, can assert SRQ. To conduct the serial poll, the controller sends SPE, a universal message, then addresses each device in turn as a talker and reads a status byte from each. Any device asserting SRQ also asserts bit 7 (DIO7) of the status byte to tell the controller that it is actively requesting service. The remainder of the status byte tells the controller why it is requesting service. (See Service Request later in this section.)

The controller issues the Device CLear (DCL) or Selected Device Clear (SDC) message to initialize internal functions of devices on the bus. DCL applies to all devices, SDC only affects the addressed device(s). The effects of these messages on each instrument is decided by the designer, who can choose to initialize any device function to any state that suits the purpose of the instrument. Their effects in the 5223 are described under Power-Up And Reset States earlier in this section.

The Go To Local (GTL) and Local Lock-Out (LLO) messages disable the addressed device's GPIB interface or front panel, respectively.

The UnTalk and UnListen messages apply to all instruments on the bus.

The Group Execute Trigger (GET), Parallel Poll Configure (PPC), Parallel Poll Unconfigure (PPU), and Take ConTrol (TCT) messages are ignored by the 5223 because the 5223 does not have device trigger, parallel poll, or controller capability.

DEVICE-DEPENDENT MESSAGES

Device-dependent messages (e.g., 5223 commands, data, etc.) are transferred from any one instrument (talker) to one or more other instruments (listeners) on the bus. Device-dependent messages may affect the functions of the instruments (e.g., commands), but they do not directly affect the actual GPIB interface.

Device-dependent messages sent to the 5223 can contain both upper- and lower-case Ascii characters. Lower-case characters are converted to upper-case when received by the 5223. (The 5223 sends only upper-case characters over the GPIB.)

Multiple commands can be sent as one message if they are separated by semi-colons.

The 5223 device-dependent messages can be separated into three sub-catagories; instrument control, waveform transfer, and information request commands.

INSTRUMENT CONTROL COMMANDS

Instrument control commands allow remote control of many of the 5223 functions. Many of these commands and their arguments can be abbreviated, if desired. In the following command descriptions, the minimum abbreviations of a command or argument is shown in bold. Either a comma or a space can be used as a separator between a command and its argument(s), and between multiple arguments (where allowed).

ACQUIRE Command

This command is used to initiate an Acquire process in one or both memory compartments.

The command format is:

ACQUIRE <argument>

where <argument> is one or both of the following;

LEFT — for the Left compartment,
RIGHT — for the Right compartment,

Multiple arguments can be separated by spaces or commas, and can be in any order.

An ACQUIRE process causes the appropriate compartment(s)' SAVE function to be turned off, and the front-panel button-scanning routines to be replaced with a special Acquire routine. The Acquire routine monitors the Address Select signal from the memory board, waiting for a transition in the signal, which indicates that a page change has resulted from a complete record being loaded into that compartment's memory. When such a transition occurs in a compartment which was specified in the ACQUIRE command, that compartment's SAVE function is turned on, and an Acquisition Complete SRQ is generated. This monitoring program executes often enough to be sure of running at least four times during any one sweep, so that it will catch the first new waveform available.

An Improper Command SRQ will be generated if the ACQUIRE command is issued while the 5223 is in the Local state, a PLOT process is running, or the ROLL function is on.

PLOT Command

This command is used to initiate a PLOT process via the GPIB.

The command format is:

PLOT

This command has no arguments.

The PLOT process consists of turning the OUTPUT SAVED DISPLAY(S) function on, and then waiting for the memory board to terminate it. During the PLOT process, commands which affect the front panel buttons or the memory board are not allowed. At the conclusion of the PLOT process, a Plotter Done SRQ will be generated.

A PLOT process may also be initiated or ended (if the 5223 is in the Local state) by pressing the OUTPUT SAVED DISPLAY(S) button on the front panel.

RELEASE Command

This command turns off selected memory control functions, and leaves the others unaffected.

The command format is:

RELEASE <argument>

where <argument> is one or more of the following;

DISP.L — DISPLAY LEFT
SAVE.L — SAVE LEFT
L.VS.R — L VS R
DISP.R — DISPLAY RIGHT
SAVE.R — SAVE RIGHT
ROLL — ROLL
VECTOR — VECTOR
ALL — all of the above

Multiple arguments can be separated by spaces or commas, and can be in any order.

This command must only be used while the 5223 is in the Remote state, and the PLOT and ACQUIRE processes are inactive. If it is issued at any other time, an Improper Command SRQ will be generated.

SELECT Command

This command turns on specified memory control functions, and leaves the others unaffected.

The command format is:

SELECT <argument>

where <argument> is one or more of the following;

DISP.L	— DISPLAY LEFT
SAVE.L	— SAVE LEFT
L.VS.R	— L VS R
DISP.R	— DISPLAY RIGHT
SAVE.R	— SAVE RIGHT
ROLL	— ROLL
VECTOR	— VECTOR
ALL	— all of the above

Multiple arguments can be separated by spaces or commas, and can be in any order.

This command must only be used while the 5223 is in the Remote state, and the PLOT and ACQUIRE processes are inactive. If it is issued at any other time, an Improper Command SRQ will be generated.

SET Command

The set command turns on specified memory control functions, and turns off all others.

The command format is:

SET <argument>

where <argument> is one or more of the following;

DISP.L	— DISPLAY LEFT
SAVE.L	— SAVE LEFT
L.VS.R	— L VS R
DISP.R	— DISPLAY RIGHT
SAVE.R	— SAVE RIGHT
ROLL	— ROLL
VECTOR	— VECTOR
ALL	— all of the above

Multiple arguments can be separated by spaces or commas, and can be in any order.

This command must only be used while the 5223 is in the Remote state, and the PLOT and ACQUIRE processes are inactive. If it is issued at any other time, an Improper Command SRQ will be generated.

If no <argument> is specified, all of the above memory functions will be turned off.

STOP Command

This command may be used to cancel OUTPUT SAVED DISPLAY(S) and ACQUIRE processes. No service request will be generated as a result of the termination.

The command format is:

STOP

This command has no arguments.

If no process is active, the STOP command has no affect.

WAVEFORM TRANSFER COMMANDS

Waveform transfer commands directly control or affect the transfer of waveform data. Many of these commands can be abbreviated, if desired. In the following command descriptions, the minimum abbreviation of a command or argument is shown in bold. Either a comma or a space can be used as a separator between a command and its argument(s), and between multiple arguments (where allowed).

General Waveform Transfer Information

The transmit mode of the 5223 (ASCII or BINARY) should be selected based on the particular application. If the waveform data is going to be processed or inspected by the controller, then Ascii data will be much easier to work with. If the waveform data is just going to be stored and later reloaded into the 5223 for viewing or visual comparison with other waveforms, then Binary data will usually transfer faster over the GPIB and require less storage space (two bytes per point for Binary data, up to five bytes per point for Ascii data).

NOTE

Unless transmission speed or storage space is a major consideration, you may prefer to use Ascii coding for all waveform data transmissions.

The waveform data is transmitted in a 'Y-only' format. Implicit in the 'Y-only' format is the assumption that the y-values in the data stream represent instantaneous values of the digitized waveform, sampled at evenly spaced intervals.

However, due to the channel-switching of the 5223, a waveform stored in memory may not always meet this requirement. Waveforms acquired in the CHOP mode are sampled at regular but non-uniform intervals. In order to resolve this inconsistency, an interpolation algorithm is used to generate points to fill in the waveform and make the intervals evenly spaced again.

Interpolated waveforms are transmitted as a series of 254 groups of points. Each group is four points long; the

first two points are "real" points, that is, they were actually sampled by the digitizer, and the last two points are interpolated values.

The interpolation algorithm is shown graphically in Figure 3-4.

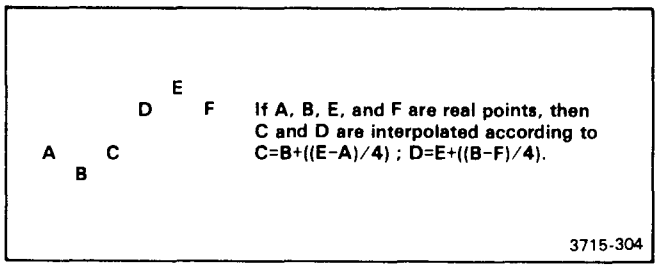


Figure 3-4. Waveform data interpolation.

The operating conditions that cause the 5223 to interpolate are shown in Table 3-2.

The length of the transmitted waveform (number of transmitted points) is also affected by the combinations of plug-in settings shown in Table 3-2.

TABLE 3-2
Plug-In Settings and Waveform Points

Single/ Dual Channel	Alt/ Chop Format	L*R*100μs Format	# of Points Transmitted	Inter-polation ?
SINGLE	N/A	NO	1016	NO
SINGLE	N/A	YES	508	NO
DUAL	ALT	NO	508	NO
DUAL	ALT	YES	508	NO
DUAL	CHOP	NO	1016	YES
DUAL	CHOP	YES	254	NO

(L*R*100 μS Format is Left and Right compartments active at 100 μS sweep rate.)

The waveform data is normalized in terms of the displayed waveform. Neither the waveform data nor the waveform preamble contain any scaling information. Horizontally, the data is to be interpreted as being evenly distributed over the interval of one real-time sweep (i.e., 10.16 divisions of sweep).

Vertically, the data represents the displacement from zero (center screen) of the input waveform, normalized to ±5.12 divisions of deflection.

ACCESS Command

This command is used to set the value of a group of internal software flags collectively called the Access Code. This code determines which waveform record the 5223 will transmit in response to a CURVE? query.

The command format is:

ACCESS <argument>

where <argument> is one of the following;

LEFT	— Left compartment, single channel
LEFT1	— Left compartment, channel 1
LEFT2	— Left compartment, channel 2
RIGHT	— Right compartment, single channel
RIGHT1	— Right compartment, channel 1
RIGHT2	— Right compartment, channel 2

Upon power-up of the system, the access code defaults to LEFT.

If the single/dual channel nature of the accessed compartment conflicts with the Access Code when a CURVE? query is answered, the transmitted waveform may not agree with the Access Code. In these cases, the WFID argument of the WFMPRE? query response will correctly identify the waveform. Table 3-3 illustrates this for the left compartment (right compartment is similar).

TABLE 3-3
Access Code vs. Transmitted Waveform

Access Code	Left Compartment Single/Dual Channel	Transmitted Waveform
L	SINGLE	L
L	DUAL	L1
L1	SINGLE	L
L1	DUAL	L1
L2	SINGLE	L
L2	DUAL	L2

The decoding routine used to process the argument ignores all characters except 1, 2, L, and R. These characters may appear in any order, however, it is not legal to specify more than one channel or compartment at a time. If this is attempted, a Command Error SRQ will be generated.

ASCII Command

This command places the waveform transmission function of the 5223 in the ASCII mode.

The command format is:

ASCII

This command has no arguments.

The 5223 defaults to the binary transmit mode on power-up.

BINARY Command

This command places the waveform transmission function of the 5223 in the BINARY mode.

The command format is:

BINARY

This command has no arguments.

The 5223 defaults to the binary transmit mode on power-up.

CURVE Command

This command loads a waveform into the compartment and channel specified by the most recent WFMPRE command sent to the 5223.

The command format is:

CURVE <waveform>

where <waveform> is either Ascii Data or Binary Data.

Ascii Data Format. Ascii data consist of a series of signed integer numbers in the range of -512 to +511. Each number represents the vertical position of a point of the waveform. The actual vertical position of the point (in graticule divisions) is the transmitted value divided by 100, where 0 is the center graticule line (e.g., -200 is two divisions below graticule center).

Each transmitted value must be separated by a comma or a space.

Positive values do not need a plus sign (+).

Binary Data Format. Binary data has the following format:

%<byte count><waveform data><checksum>

The percent sign (%) tells the 5223 that the following data is in binary format.

The <byte count> is a two-byte binary integer (most significant byte first) specifying the number of <waveform data> bytes (2 X number of points) plus the <checksum> byte. (The only legal values are 509, 1017, and 2033.)

The <waveform data> is a series of binary data bytes. Each waveform point is represented by a two-byte, binary number (most significant byte first), in the following format:

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
<msbyte>	<s>	<b8>	<b6>	<b7>	<b5>	<b4>	<b3>	<b2>
<lsbyte>	<b1>	<bØ>	<x>	<x>	<x>	<x>	<x>	<x>

where
<msbyte> is the most-significant byte,
<lsbyte> is the least-significant byte,
<s> is the sign bit (1 if negative, 0 if zero or positive),
<bØ> — <b8> are data bits Ø through 8, and
<x> bits are ignored.

There are two ways to interpret <bØ> through <b8> and <s>:

One interpretation is that <bØ> through <b8> and <s> represent a left-justified, two's-complement, signed binary fraction with an implied radix point (equivalent to a decimal point) between <s> and <b8>. This results in a fraction between -1 and +1.

The other interpretation is that <bØ> through <b8> and <s> represent a left-justified, two's-complement, signed binary integer in the range of -512 to +511.

The actual displayed vertical position of each point (in graticule divisions from crt center) is the fraction value times 5.12 or the integer value divided by 100.

In either case, any number of data bits (up to 15) can be sent to the 5223 and the displayed waveform will always be within ±5.12 divisions of graticule center as long as the binary data is sent left-justified following the sign bit.

The <checksum> is a single-byte binary integer whose value is the two's complement of the modulo-256 sum of the <bytecount> bytes and the <waveform data> bytes (but not the "%"). If the transmitted <checksum> byte does not agree with the checksum calculated by the 5223 when the waveform is received, a Checksum Error SRQ will be generated.

If a binary waveform's block length is an illegal value, or doesn't match the value specified by the NR.PTS argument of the most recent WFMPRE command, a Command Error SRQ will be generated, and the waveform data will be ignored.

If more points than were specified in the block length or the most recent preamble are sent to the 5223, a Command Error SRQ will be generated. (It is highly unlikely that the "extra" waveform points will constitute valid command strings, so they will be interpreted as misspelled commands.)

If fewer points are transmitted to the 5223 than were specified, the remaining points are set to zero.

If the waveform has a legal number of points, but doesn't match the space available for the accessed memory channel, it is compressed or expanded as required. For example, if a waveform that is 254 points long is loaded into a single-channel memory, which has an available space of 1016 points, straight-line interpolation is used to fill in three points between each transmitted point, bringing the waveform size up to 1016 points.

Conversely, if a single-channel waveform of 1016 points is loaded into the 508-point space of a dual-channel record, alternate points are discarded to make the waveform fit.

If a dual-channel waveform is loaded into a compartment that previously contained a single channel waveform, half of the original waveform's points are retained, and marked as the other channel.

After the waveform is loaded, the compartment into which it was loaded is Saved, and the other memory control functions return to the settings they had prior to the transfer.

If an attempt is made to load a waveform while the 5223 is in the Local mode, or an OUTPUT SAVED DISPLAY(S) or ACQUIRE process is active, an Improper Command SRQ will be generated, and the waveform data will be ignored.

CURVE? Command

This command causes the 5223 to transmit the waveform selected by the last ACCESS command.

The command format is:

CURVE?

The 5223 responds to this command with:

CURVE <waveform>

where <waveform> is either Ascii data or Binary data (see the description for the CURVE command above).

Whether the 5223 transmits Ascii data or Binary data depends on the transmit mode (set by the ASCII or BINARY commands above).

If a waveform transmission is requested when the 5223 is in the Local state, or when a PLOT or ACQUIRE process is running, an Improper Command SRQ will be generated.

WFMPRE Command

This command is used to set up the 5223 for the reception of waveform data. Waveform parameters which do not appear in the CURVE data, such as the number of points in the curve, the trigger position, and the channel into which the curve is to be loaded, are specified by the WFMPRE command.

The command format is:

WFMPRE <argument>

where <argument> is one or more of the following;

WFID:<destination>
NR.PT:<points>
PT.OFF:<trigger position>

<destination> is **L, L1, L2, R, R1,** or **R2** (see ACCESS command description).

<points> is the number of points per waveform (**254, 508,** or **1016**).

<trigger position> is the ordinal position of the triggering event in the waveform.

The waveform preamble arguments defined above may appear in any order in the WFMPRE command, and may even be repeated. If they are repeated, however, it is the last one which will take effect.

Any argument other than those defined above will be ignored.

Waveform parameters, once specified by a WFMPRE command, retain their values until they are altered by another WFMPRE command.

Multiple arguments can be separated by spaces or commas, and can be in any order.

WFMPRE? Command

This is a standard command among Tektronix waveform-handling GPIB instruments intended to allow the controller to determine the characteristics of a waveform. The form of this command is:

WFMPRE?

The 5223 responds to this command with:

WFMPRE WFID:<destination>,NR.PT:<points>, PT.OFF:<trigger>,<mode>

where <destination>, <points>, and <trigger> are as described in the WFMPRE command above, and <mode> is either of the following;

ENCDG:ASC or
ENCDG:BIN,BYT/NR:2,BN.FMT:LF,BIT/NR:10

INFORMATION REQUEST COMMANDS

Information request commands allow the GPIB controller to keep track of the current status of the 5223. Many of these commands can be abbreviated, if desired. In the following command descriptions, the minimum abbreviation of each command is shown in bold.

HEALTH? Command

This command allows the controller to test the performance of the 5223's waveform storage and retrieval processes. In response to this command, the 5223 repeats its power-on memory board RAM test, and reports its findings via the GPIB. At the conclusion of the test, both compartments are loaded with the power-on graticule pattern, and the DISPLAY LEFT, SAVE LEFT, L VS R, SAVE RIGHT, and DISPLAY RIGHT functions are forced On; all other functions are forced Off.

The command format is:

HEALTH?

The 5223 responds to this command with:

HEALTH OK or
HEALTH SICK

ID? Command

This command is standard among Tektronix GPIB instruments, and is used to identify the instrument over the bus.

The command format is:

ID?

The 5223 responds to this command with:

ID TEK/5223 V79.1,<lo rom><hi rom><8291 type>

<lo rom> is a single-digit code identifying the version of the currently-installed lower ROM.

<hi rom> is a single-digit code identifying the version of the currently-installed upper ROM.

<8291 type> is null if the GPIB chip is an 8291, or A if the GPIB chip is an 8291A.

SET? Command

This command returns enough information to completely define the current state of all the GPIB-programmable features of the 5223, in such a form that, if the response is "echoed" back to the 5223, the states of all those features will return to the values they had at the time of the SET? command. The information reported consists of the front-panel button settings, the encoding mode for waveform transmissions (ASCII or BINARY), and the access code for waveform transmissions.

The command format is:

SET?

The 5223 responds to this command with:

SET <button>;ACCESS <access code>;<mode>

where <button> is as many of the following as apply;

DISP.L (If DISPLAY LEFT button active)
SAVE.L (If SAVE LEFT button active)
L.VS.R (If L VS R button active)
SAVE.R (If SAVE RIGHT button active)
DISP.R (If DISPLAY RIGHT button active)
ROLL (If ROLL button active)
VECTOR (If VECTOR button active)

<access code> is L, L1, L2, R, R1, or R2 (see ACCESS command)

<mode> is either ASCII or BINARY

Multiple <button> arguments are separated by commas.

SERVICE REQUEST

The service request function allows the 5223 to keep the GPIB controller informed of its status. This is done by asserting the Service ReQuest (SRQ) line and then sending a status byte to the controller when polled. The status byte is an eight-bit binary number which represents the status of the 5223. Any service request can be cleared by performing a serial poll of the 5223.

Status Bytes

The status bytes which are sent by the 5223 and their meanings are listed in Table 3-4.

TABLE 3-4
5223 Status Bytes

Condition	Status Byte*
On Bus and Powered	65 or 81
Command Error	97
Improper Command	98 or 114
Checksum Error	101
Transmission Aborted	192 or 208
Plotter Done	194 or 210
Acquisition Complete (RIGHT)	193 or 209
Acquisition Complete (LEFT)	196 or 212
Acquisition Complete (Both)	197 or 213

*The second status byte value will be returned if the 5223 is Busy.

Any other status byte values indicate normal operation of the 5223.

TALK ONLY MODE

The TALK ONLY mode of the 5223 Option 10 allows the user to amass large amounts of continuous data. In this mode, all memory control functions are disabled, and the waveform displays from both compartments are turned off. The front-panel buttons are re-defined so that the DISPLAY LEFT and DISPLAY RIGHT buttons serve to enable (when pushed in) or disable (when released) the transmission of the digitized data from the LEFT and RIGHT compartments, respectively. All other buttons are electrically inoperative.

The digitized data from the selected channels is continuously transmitted at the sample rate (determined by the timebase), or the data transfer speed of the listener, or the data transmission speed of the 5223, whichever is slowest.

The maximum data transmission speed of the 5223 corresponds to a timebase setting of 50 ms/div if two compartments' outputs are being transmitted, and 20 ms/div if only one compartment's output is being transmitted.

TALK ONLY mode data is transmitted in the following format:

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
<msbyte>	<s>	<b8>	<b7>	<b6>	<b5>	<b4>	<b3>	<b2>
<lsbyte>	<b1>	<bØ>	<s/d>	<t>	<or>	<l/r>	<ch>	<Ø>

where
<msbyte> is the most-significant byte,
<lsbyte> is the least-significant byte (sent with EOI),
<s> is the sign bit (1 if negative, 0 if zero or positive),
<bØ> — <b8> are data bits Ø through 8,
<s/d> indicates the number of channels (1 if single, 0 if dual).
<t> indicates triggered status of sweep (1 if triggered, 0 if not),
<t> indicates triggered status of sweep (1 if triggered, 0 if not),
<or> indicates data overrun (1 if 5223 is generating data faster than GPIB is transferring it, 0 if not),
<l/r> indicates compartment (1 if Left, 0 if Right), and
<ch> indicates channel of dual-channel waveform (1 if channel 1, 0 if channel 2).

SAMPLE PROGRAMS

The following sample programs were written using a Tektronix 4050-series graphic system as the GPIB-system controller. Other controllers may require some program modifications to work properly.

All of the sample programs use variable A3 as the address of the 5223. The sample programs set the value of A3 to 10. If your 5223 is set for some other address, those statements must be changed to match the actual 5223 address.

To avoid duplication, the sample programs use subroutines to perform three tasks; request an access code, get a waveform preamble from the 5223 and extract the waveform length from it, and poll the 5223.

All of the sample programs use these subroutines, therefore, they must be included for the programs to work properly.

The sample programs are written so that they can be combined into one program without changing any line-numbers.

Subroutines

The Access Code subroutine performs the following steps:

1. Requests the access code (lines 10010 and 10020).
2. Assigns access code to Q$ (line 10030).
3. Checks that 1 and 2 do not both exist in Q$ (line 10050).
4. Checks that L and R do not both exist in Q$ (line 10060).
5. Checks that L or R does exist in Q$ (line 10070).
6. Returns to main program (line 10090).

```
10000 REM SUBROUTINE TO ASSIGN ACCESS CODE TO Q$
10010 PRINT "ENTER DESIRED ACCESS CODE"
10020 PRINT "(L, L1, L2, R, R1, or R2): ";
10030 INPUT Q$
10040 REM check that Q$ is a valid access code
10050 IF POS(Q$,"1",1)>0 AND POS(Q$,"2",1)>0 THEN 10010
10060 IF POS(Q$,"L",1)>0 AND POS(Q$,"R",1)>0 THEN 10010
10070 IF POS(Q$,"L",1)=0 AND POS(Q$,"R",1)=0 THEN 10010
10080 REM access code is valid
10090 RETURN
```

The Wfmpre? subroutine performs the following steps:

1. Saves Left and Right compartments and requests waveform preamble from 5223 (line 11040).
2. Assigns waveform preamble to W$ (line 11050).
3. Extracts waveform length* from W$ (line 11060).
4. Converts length information from string to numeric data (line 11070).
5. Returns to main program (line 11080).

```
11000 REM WFMPRE? EXTRACTION SUBROUTINE
11010 REM waveform preamble to W$
11020 REM length to L
11030 REM A3 = 5223 address
11040 PRINT @A3:"SELECT SAVE.L,SAVE.R;WFMPRE?"
11050 INPUT @A3:W$
11060 L$=SEG(W$,POS(W$,"NR.PT:",1)+6,4)
11070 L=VAL(L$)
11080 RETURN
```

The Serial Poll subroutine performs the following steps:

1. Clears SRQ and assigns the status byte value to variable S1 using the 4050-series serial poll command (line 12030).
2. Returns to main program (line 12040).

```
12000 REM POLL SUBROUTINE
12010 REM status byte to S1
12020 REM A3 = 5223 address
12030 POLL A1,S1;A3
12040 RETURN
```

*Other information can also be extracted from W$ in the same manner.

Ascii Data To 4050 String

This program performs the following steps:

1. Enables the Serial Poll subroutine (line 1010).
2. Assigns variable A3 a value of 10 for the 5223 address (line 1020).
3. Branches to Access Code subroutine (line 1030).
4. Sends an ACCESS command with the desired access code to the 5223 (line 1040).
5. Branches to the Wfmpre? subroutine (line 1050).
6. Clears any previous value of A$ and dimensions A$ (lines 1060 and 1070).
7. Requests an Ascii curve from the 5223 and stores it as A$ (lines 1080 and 1090).

This program should be used when the waveform data is only going to be stored on tape. Both W$ (the waveform preamble) and A$ (the curve) should be stored together on tape.

```
1000 REM ASCII DATA TO 4050 STRING
1010 ON SRQ THEN 12000
1020 A3=10
1030 GOSUB 10000
1040 PRINT @A3:"ACCESS ";Q$
1050 GOSUB 11000
1060 DELETE A$
1070 DIM A$(7+L*5)
1080 PRINT @A3:"ASCII;CURVE?"
1090 INPUT @A3:A$
1100 REM A$ now contains the curve data
1110 PRINT "TRANSFER COMPLETE"
1120 RETURN
```

Ascii String Data To 5223

This program performs the following steps:

1. Enables the Serial Poll subroutine (line 1530).
2. Assigns variable A3 a value of 10 for the 5223 address (line 1540).
3. Branches to Access Code subroutine (line 1550).
4. Sends the waveform preamble to the 5223 (line 1560).
5. Sends new waveform identification to the 5223 (line 1580).
6. Sends the curve data to the 5223 (line 1590).

```
1500 REM ASCII STRING DATA TO 5223
1510 REM W$ = Waveform Preamble
1520 REM A$ = curve data string
1530 ON SRQ THEN 12000
1540 A3=10
1550 GOSUB 10000
1560 PRINT @A3:W$
1570 REM change WFID if desired
1580 PRINT @A3:"WFMPRE WFID:";Q$
1590 PRINT @A3:A$
1600 PRINT "TRANSFER COMPLETE"
1610 RETURN
```

Ascii Data To 4050 Array

This program performs the following steps:

1. Enables the Serial Poll subroutine (line 2010).
2. Assigns variable A3 a value of 10 for the 5223 address (line 2020).
3. Branches to Access Code subroutine (line 2030).
4. Sends an ASCII command and an ACCESS command with the desired access code to the 5223 (line 2040).
5. Branches to Wfmpre? subroutine (line 2050).
6. Clears and dimensions array B (lines 2060 and 2070).
7. Requests a curve from the 5223 and stores it in array B (lines 2080 and 2090).

This program should be used when the waveform data is going to be processed by the controller, in that each point of the waveform is stored as an individual value in the array. (e.g., The 238th point of the waveform is stored as B(238).)

```
2000 REM ASCII DATA TO 4050 ARRAY
2010 ON SRQ THEN 12000
2020 A3=10
2030 GOSUB 10000
2040 PRINT @A3:"ASCII;ACCESS ";Q$
2050 GOSUB 11000
2060 DELETE B
2070 DIM B(L)
2080 PRINT @A3:"CURVE?"
2090 INPUT @A3:B
2100 REM array B now contains the curve data
2110 PRINT "TRANSFER COMPLETE"
2120 RETURN
```

Ascii Array Data To 5223

This program performs the following steps:

1. Enables the Serial Poll subroutine (line 2530).
2. Assigns variable A3 a value of 10 for the 5223 address (line 2540).
3. Branches to Access Code subroutine (line 2550).
4. Sends waveform preamble to 5223 (line 2560).
5. Sends new waveform identification to the 5223 (line 2580).
6. Sends CURVE command and curve data to the 5223 (line 2590).

```
2500 REM ASCII ARRAY DATA TO 5223
2510 REM W$ = waveform preamble
2520 REM B = curve data array
2530 ON SRQ THEN 12000
2540 A3=10
2550 GOSUB 10000
2560 PRINT @A3:W$
2570 REM change WFID if desired
2580 PRINT @A3:"WFMPRE WFID:";Q$
2590 PRINT @A3:"CURVE ";B;
2600 REM the trailing ; is important. If omitted, the
2610 REM array will be sent without delimiters.
2620 PRINT "TRANSFER COMPLETE"
2630 RETURN
```

Binary Data To 4050 Arrays

This program performs the following steps:

1. Enables the Serial Poll subroutine (line 3010).
2. Assigns variable A3 a value of 10 for the 5223 address (line 3020).
3. Branches to Access Code subroutine (line 3030).
4. Sends a BINARY command and an ACCESS command with the desired access code to the 5223 (line 3040).
5. Branches to the Wfmpre? subroutine (line 3050).
6. Clears and dimensions arrays A, B, and C (lines 3060 and 3100).
7. Requests curve from the 5223 (line 3110).
8. Sends 5223's Talk Address (line 3120).
9. Reads curve data from 5223 (line 3130).
10. Sends Untalk message (line 3140).

@

This program has no real advantage over Ascii transmission when using a 4050-series controller. (Ascii data is much easier to work with.)

```
3000 REM BINARY DATA TO 4050 ARRAYS
3010 ON SRQ THEN 12000
3020 A3=10
3030 GOSUB 10000
3040 PRINT @A3:"BINARY;ACCESS ";Q$
3050 GOSUB 11000
3060 DELETE A,B,C
3070 REM array A will contain 'CURVE %<bytecount>'
3080 REM array B will contain the waveform points
3090 REM array C will contain <checksum><linefeed>
3100 DIM A(9),B(2*L),C(2)
3110 PRINT @A3:"CURVE?"
3120 WBYTE @A3+64:
3130 RBYTE A,B,C
3140 WBYTE @95:
3150 PRINT "TRANSFER COMPLETE"
3160 RETURN
```

Binary Data To 5223

This program performs the following steps:

1. Enables the Serial Poll subroutine (line 3530).
2. Assigns variable A3 a value of 10 for the 5223 address (line 3540).
3. Branches to Access Code subroutine (line 3550).
4. Sends waveform preamble to 5223 (line 3560).
5. Sends new waveform identification to 5223 (line 3580).
6. Sends curve data to 5223's Listen address (line 3590).
7. Sends Unlisten message (line 3600).

```
3500 REM BINARY DATA TO 5223
3510 REM W$ = waveform preamble
3520 REM arrays A, B, and C, contain curve data
3530 ON SRQ THEN 12000
3540 A3=10
3550 GOSUB 10000
3560 PRINT @A3:W$
3570 REM change WFID if desired
3580 PRINT @A3:"WFMPRE WFID:";Q$
3590 WBYTE @A3+32:A,B,C
3600 WBYTE @63:
3610 PRINT "TRANSFER COMPLETE"
3620 RETURN
```

ASCII & IEEE 488 (GPIB) CODE CHART

B7 B6 B5 / BITS / B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL 0 0	20 DLE 10 16	40 SP 20 32	60 0 30 48	100 @ 40 64	120 P 50 80	140 ` 60 96	160 p 70 112
0 0 0 1	1 GTL SOH 1 1	21 LLO DC1 11 17	41 ! 21 33	61 1 31 49	101 A 41 65	121 Q 51 81	141 a 61 97	161 q 71 113
0 0 1 0	2 STX 2 2	22 DC2 12 18	42 " 22 34	62 2 32 50	102 B 42 66	122 R 52 82	142 b 62 98	162 r 72 114
0 0 1 1	3 ETX 3 3	23 DC3 13 19	43 # 23 35	63 3 33 51	103 C 43 67	123 S 53 83	143 c 63 99	163 s 73 115
0 1 0 0	4 SDC EOT 4 4	24 DCL DC4 14 20	44 $ 24 36	64 4 34 52	104 D 44 68	124 T 54 84	144 d 64 100	164 t 74 116
0 1 0 1	5 PPC ENQ 5 5	25 PPU NAK 15 21	45 % 25 37	65 5 35 53	105 E 45 69	125 U 55 85	145 e 65 101	165 u 75 117
0 1 1 0	6 ACK 6 6	26 SYN 16 22	46 & 26 38	66 6 36 54	106 F 46 70	126 V 56 86	146 f 66 102	166 v 76 118
0 1 1 1	7 BEL 7 7	27 ETB 17 23	47 ' 27 39	67 7 37 55	107 G 47 71	127 W 57 87	147 g 67 103	167 w 77 119
1 0 0 0	10 GET BS 8 8	30 SPE CAN 18 24	50 (28 40	70 8 38 56	110 H 48 72	130 X 58 88	150 h 68 104	170 x 78 120
1 0 0 1	11 TCT HT 9 9	31 SPD EM 19 25	51) 29 41	71 9 39 57	111 I 49 73	131 Y 59 89	151 i 69 105	171 y 79 121
1 0 1 0	12 LF A 10	32 SUB 1A 26	52 * 2A 42	72 : 3A 58	112 J 4A 74	132 Z 5A 90	152 j 6A 106	172 z 7A 122
1 0 1 1	13 VT B 11	33 ESC 1B 27	53 + 2B 43	73 ; 3B 59	113 K 4B 75	133 [5B 91	153 k 6B 107	173 { 7B 123
1 1 0 0	14 FF C 12	34 FS 1C 28	54 , 2C 44	74 < 3C 60	114 L 4C 76	134 \ 5C 92	154 l 6C 108	174 ¦ 7C 124
1 1 0 1	15 CR D 13	35 GS 1D 29	55 - 2D 45	75 = 3D 61	115 M 4D 77	135] 5D 93	155 m 6D 109	175 } 7D 125
1 1 1 0	16 SO E 14	36 RS 1E 30	56 . 2E 46	76 > 3E 62	116 N 4E 78	136 ^ 5E 94	156 n 6E 110	176 ~ 7E 126
1 1 1 1	17 SI F 15	37 US 1F 31	57 / 2F 47	77 UNL ? 3F 63	117 O 4F 79	137 UNT _ 5F 95	157 o 6F 111	177 RUBOUT (DEL) 7F 127
	ADDRESSED COMMANDS	UNIVERSAL COMMANDS	LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES OR COMMANDS	

KEY

octal 25 PPU — GPIB code
NAK — ASCII character
hex 15 21 — decimal

THEORY OF OPERATION

This section of the manual describes the circuitry in the 5223 Digitizing Oscilloscope Option 10 (GPIB). The description starts with a Block Diagram Description, using the diagram shown in Figure 4-1, and goes into the more involved areas in the Detailed Circuit Description. Detailed schematic diagrams are located at the back of this manual. Refer to these diagrams when reading the descriptions.

BLOCK DIAGRAM DESCRIPTION

The following description presents an overview of the operation of the 5223. Figure 4-1 shows a block diagram of the 5223 system. The number within the diamond in each block refers to the diagram of the same number in the Diagrams and Circuit Board Illustrations section.

SAMPLING PRINCIPLES

In order to perform its digitizing operation, the 5223 Digitizing Oscilloscope Option 10 (GPIB) "takes a sample" of its input signal. A sample is the voltage of the input signal at a specific instant in time. The 5223 then produces a 10-bit number (it digitizes the sample) that represents the voltage of that sample. To store a complete waveform, the 5223 takes a series of 1024 samples.

Two types of sampling are used in the 5223. Real-time sampling is used at sweep speeds up to 0.1 ms/division. At sweep speeds of 50 μs/division and faster, sequential sampling is employed. The following discussion describes real-time and sequential sampling.

REAL-TIME SAMPLING

Real-time sampling is so named because all the samples needed to store a waveform are taken during a single real-time sweep of that signal. The time represented by the horizontal axis of the display is the actual time needed to take all the samples for this waveform. Because all the samples must be taken in the time of one horizontal sweep, real-time sampling is suited to slower signals.

In the 5223, the system uses real-time sampling when the sweep speed is set to 0.1 ms/division or slower. At these sweep speeds, the time base generates 1024 sample pulses during each sweep.

SEQUENTIAL (EQUIVALENT-TIME) SAMPLING

When the signal to be sampled is occurring at a rate that does not allow 1024 conversions per real-time sweep (as in real-time sampling), sequential sampling is used. The 5223 uses sequential sampling when the sweep speed is set to 50 μs/division or faster. In sequential sampling, the time base produces one sample pulse per real-time sweep. Each sample pulse is timed to occur slightly later in relation to the trigger point of each sweep. After 1024 sweeps of the input signal, the 5223 system has stored a complete record of the waveform and, when the MEMORY CONTENTS DISPLAY button is pressed, can display a single facsimile of the input. Because each sample was taken in sequence from a different cycle of the input signal, the process is termed "sequential sampling."

Because the time needed to collect enough samples to display the input signal, e.g. a pulse, is much greater than the pulse itself, sequential sampling is known as "equivalent-time" sampling. Figure 4-2 shows a display of a waveform constructed by equivalent-time sampling. The equivalent time between dots is determined by the fixed point on the signal where the real-time sweep triggers and the point where the sample is taken. Figure 4-3 shows the relationship between real-time and equivalent-time displays.

SIGNAL NAMES ON 5223 SYSTEM BLOCK DIAGRAM

1. A Gate
2. Analog Output Off
3. Analog Ramp
4. Analog Signal
5. Analog Vertical
6. Chart Clock

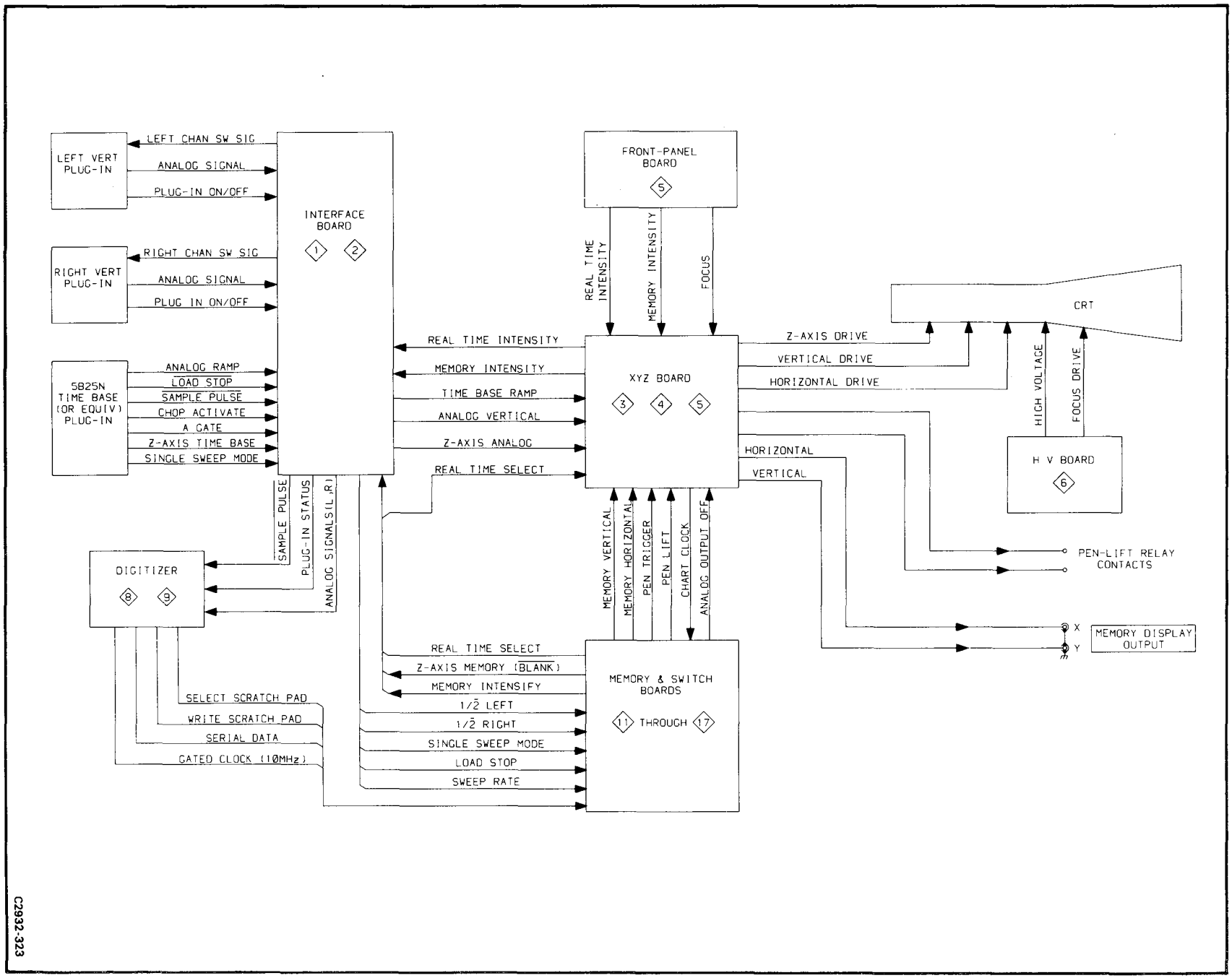


Figure 4-1. 5223 System block diagram.

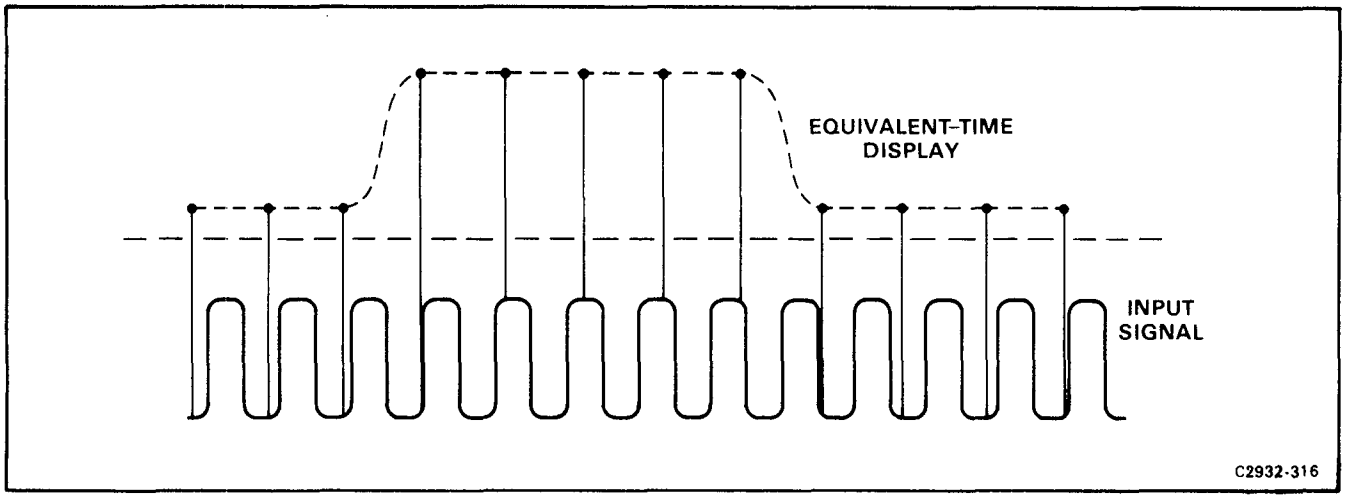


Figure 4-2. How a repetitive real-time signal is reconstructed in an equivalent-time display via sequential sampling.

7. Chop Activate
8. Focus
9. Focus Drive
10. Gated Clock (10 MHz)
11. High Voltage
12. Horizontal (X) Memory Display Output
13. Horizontal Drive
14. Left Chan Sw Sig
15. $\overline{\text{Load Stop}}$
16. Memory Horizontal
17. Memory Intensify
18. Memory Intensity
19. Memory Vertical
20. Pen Lift
21. Pen-Lift Relay Contacts
22. Pen Trigger
23. Plug-In On/Off
24. Plug-In Status
25. Right Chan Sw Sig
26. Real Time Intensity
27. Real Time Select
28. $\overline{\text{Sample Pulse}}$
29. Select Scratch Pad
30. Serial Data
31. Single Sweep Mode
32. Sweep Rate
33. Time Base Ramp
34. Vertical (Y) Memory Display Output
35. Vertical Drive
36. Write Scratch Pad
37. Z-Axis Analog
38. Z-Axis Drive
39. Z-Axis Memory ($\overline{\text{Blank}}$)
40. Z-Axis Time Base
41. $1/\overline{2}$ Left
42. $1/\overline{2}$ Right

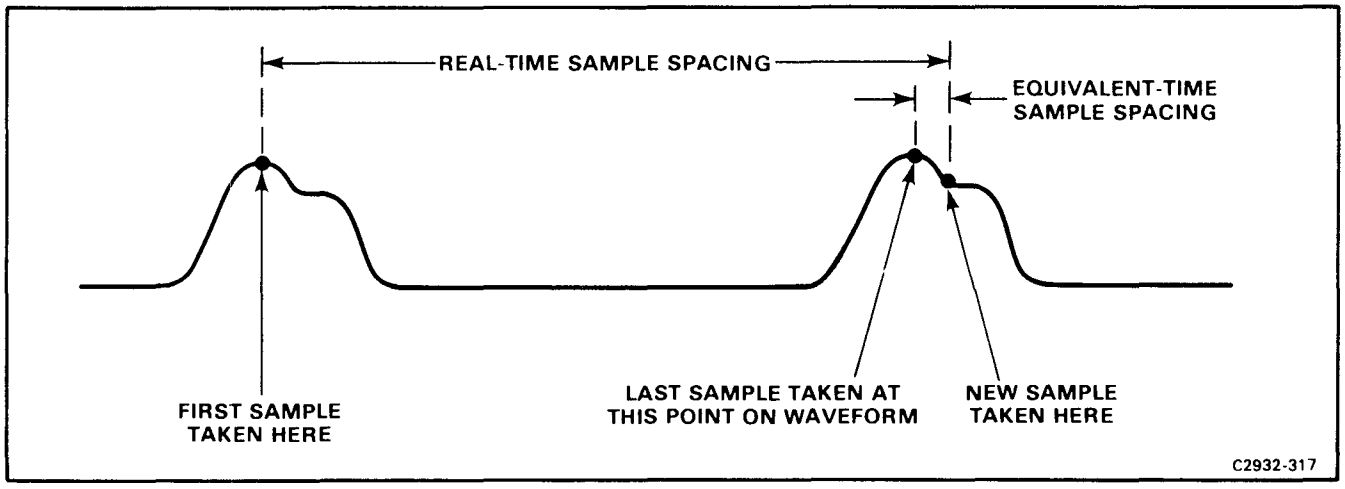


Figure 4-3. Relationship between real-time and equivalent-time.

1. A Gate. A high-logic level on the A Gate line from the 5B25N Time Base indicates that an analog sweep is in progress. The A Gate signal is a TTL-level signal.

2. Analog Output Off. A low-logic level on the Analog Output Off line indicates that a chart-output sequence is in progress. (A chart-output sequence is a serial presentation of the words in the memory, presented in an analog manner, at a speed suitable for a chart recorder.) The Analog Output Off signal disconnects the memory signal from the Memory Display Outputs, and causes a high-logic level on the Real-Time Select line, which prevents a memory display during a chart-output sequence (see item 27).

3. Analog Ramp. The Analog Ramp signal has a selectable, constant delta V per unit time. The Analog Ramp produces horizontal deflection on the crt. In other literature, the Analog Ramp may be called sweep or sweep output. The 5B25N Time Base produces the Analog Ramp.

4. Analog Signal. The Analog Signal is a differential signal from the amplifier plug-ins. The differential signal is proportional to the magnitude of the input signal; its dc voltage is proportional to the setting of the amplifier plug-in's position control.

5. Analog Vertical. The Analog Vertical signal consists of buffered and selected Analog Signals from the left and right vertical plug-ins. Buffered left and right Analog Signals are applied to the inputs of the channel switch, on the A9-Interface Board, whose output is Analog Vertical. During a real-time display, Analog Vertical becomes Vertical Drive to the crt.

6. Chart Clock. The Chart Clock signal is generated on the A3-XYZ Board and used to control the rate at which data from the memory will be presented to the MEMORY DISPLAY OUTPUT connectors on the rear panel. The frequency of the Chart Clock signal is adjustable from 29 to 425 Hz with the DISPLAY OUT SPEED control, which causes data to reach the connectors at 14 to 212 Hz when a chart out sequence has been initiated. (A flip-flop divides the chart clock signal by two.)

7. Chop Activate. A switch closure in the 5B25N Time Base connects a signal from the A9-Interface Board to the Chop Activate line via the internal Chop Sense line. The A9-Interface-Board generated Chop Activate signal, if present, occurs as a result of switch closures in the plug-in amplifiers (combinations of "Display On" and "Ch 1 - Ch 2 On"). When the time-base Chop button is pressed, the Chop Activate signal has a +5 V dc level.

NOTE

Under certain circumstances, the memory system will activate the Chop Activate line on the Interface Board.

8. Focus. The Focus signal, which comes from the A2-Front Panel Board, controls the level of focus voltage to the crt. The Focus signal controls both displays—real-time and memory.

9. Focus Drive. The Focus Drive signal controls the crt focus grid. The A5-Focus DC Restorer Board generates the Focus Drive signal.

10. Gated Clock (10 MHz). The Gated Clock signal, which originates on the A8-Digitizer Board, steps the serial data shift register on the A11-Memory Board. This serial shift register converts serial data to parallel data.

11. High Voltage. Post-accelerating voltage (12 kV) generated by a high-voltage power supply module.

12. Horizontal (X) Memory Display Output. The Horizontal (X) Memory Display Output signal comes from the horizontal memory via slew-rate-limited amplifiers on the A3-XYZ Board. The slew rate can be adjusted with the DISPLAY OUT SPEED control on the rear panel.

13. Horizontal Drive. Output of the Horizontal Amplifier on the A3-XYZ Board. Causes horizontal deflection on the crt.

14. Left Chan Sw Sig. The Left Chan Sw Sig selects either Channel 1 or Channel 2 of the left plug-in to be sent to the A9-Interface Board, via the Analog Signal line. The A9-Interface Board generates the TTL-level Left Chan Sw Sig and its counterpart, Right Chan Sw Sig. Left leads Right by 90°. The left plug-in amplifier will use Left Chan Sw Sig if it is a dual-channel model. Figure 4-4 shows the relation of the Left Chan Sw Sig to its associated signals.

15. $\overline{\text{Load Stop}}$. The $\overline{\text{Load Stop}}$ pulse, from the 5B25N Time Base, signifies the end of the digitized record. The $\overline{\text{Load Stop}}$ pulse passes through the A9-Interface Board to the Memory system.

16. Memory Horizontal. The D/A Converter on the A11-Memory Board converts the 10-bit words from the horizontal section of memory to the analog Memory Horizontal signal. The signal can be modified by the MEMORY CONTENTS HORIZ POSN, EXP and VECTOR MODE controls.

17. Memory Intensify. The memory system generates the Memory Intensify pulse to signify the amount of stored record that was acquired previous to the trigger point of the real-time display. A high-logic level means normal intensity, and a low-logic level means "intensify."

18. Memory Intensity. A signal from the front-panel MEM INTEN control that governs the brightness of the memory display.

19. Memory Vertical. A D/A Converter on the A11-Memory Board converts the 10-bit words from the vertical section of the memory to the analog Memory Vertical signal. The Memory Vertical signal can be modified with the MEMORY CONTENTS VERT POSN, EXP and VECTOR MODE controls.

20. Pen Lift. A TTL signal generated by the Memory and used by the A3-XYZ Board to drive the pen-lift relay.

21. Pen-Lift Relay Contacts. The Pen-Lift Relay Contacts provide a switch closure or opening (selectable by a jumper on the A3-XYZ Board) to operate the pen-lift feature of a chart recorder.

22. Pen Trigger. A TTL signal from the A11-Memory Board. The Pen Trigger signal initiates a one-second pen lift and data-output-holdoff period.

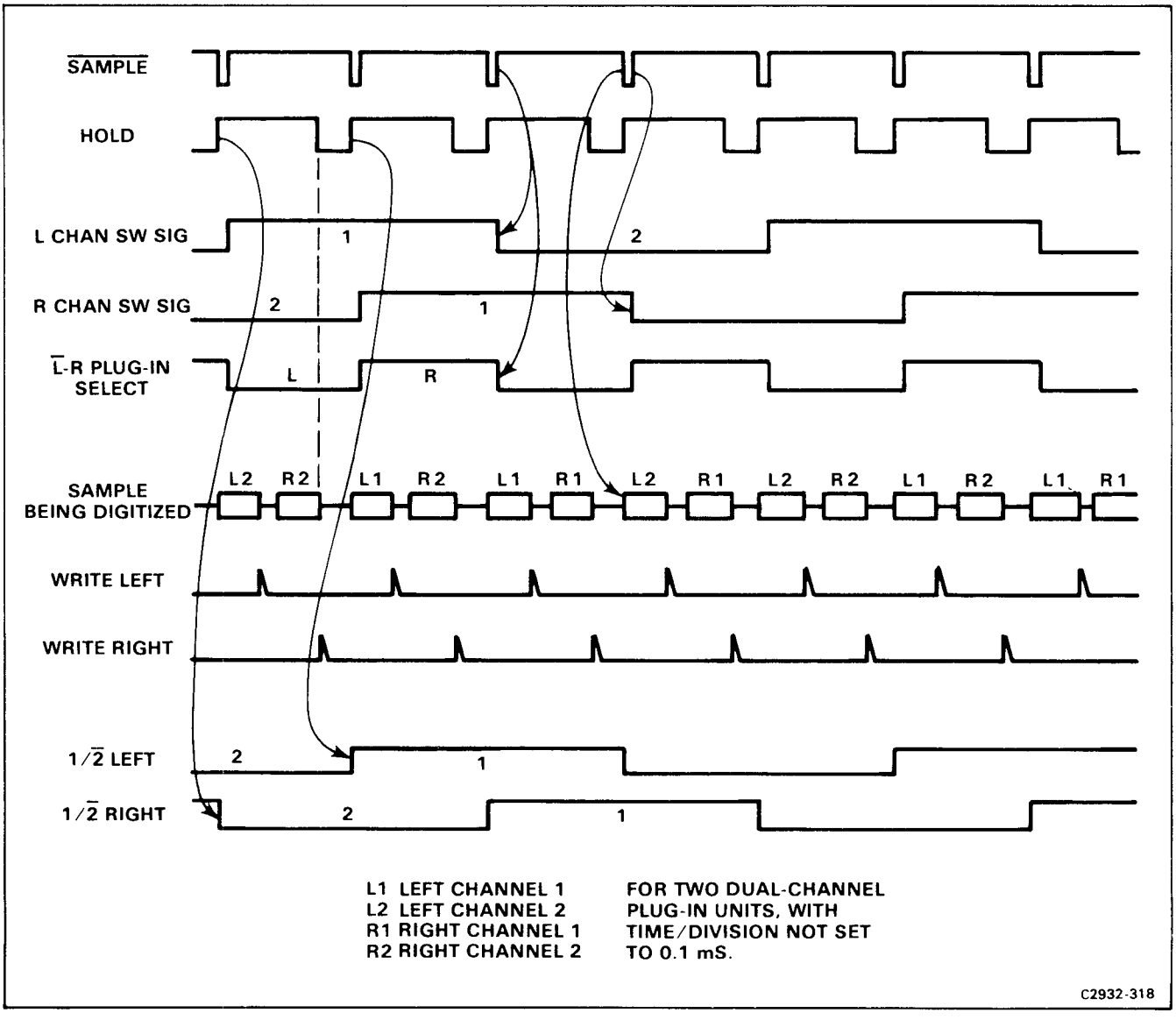


Figure 4-4. Relation of Sample, Channel-Switch and Write signals.

23. Plug-In On/Off. A switch closure from the vertical plug-in that will be used by the A9-Interface Board to determine whether the associated plug-in output is to be used for vertical deflection.

24. Plug-In Status. A signal from the A9-Interface Board to the A8-Digitizer Board to determine if a "double" write command (in the Left and Right and 0.1 ms/division mode) will be sent to the Memory.

25. Right Chan Sw Sig. The Right Chan Sw Sig selects either Channel 1 or Channel 2 of the right plug-in to be sent to the A9-Interface Board, via the Analog Signal line. The A9-Interface Board generates the TTL-level Right Chan Sw Sig and its counterpart, Left Chan Sw Sig. Right lags Left by 90°. The right plug-in amplifier will use Right Chan Sw Sig if it is a dual-channel model. Figure 4-4 shows the relation of the Right Chan Sw Sig to its associated signals.

26. Real Time Intensity. The Real Time Intensity signal is a dc level produced by the front-panel INTENSITY control. The Real Time Intensity signal goes from the A2-Front Panel Board to the A9-Interface board via the A3-XYZ Board. The A9-Interface Board converts the Real Time Intensity level to a weighted current. If the Real Time Select line is a logical 1, this weighted current reaches the Z Axis Analog output of the A9-Interface Board.

27. Real Time Select. A TTL signal from the A11-Memory Board that time-shares memory and real-time signals to the crt. A logic 1 (high) on Real Time Select means real-time, and a logic 0 (low) means memory signals. The type of display is selected by the MEMORY CONTENTS DISPLAY and the Display buttons on the plug-in amplifiers.

If only the real-time display is selected, the Real Time Select line stays at a logic 1 (high).

If only the memory display is selected, the Real Time Select line stays at a logic 0 (low).

If no display is selected (no MEMORY CONTENTS DISPLAY button and no Display buttons on the plug-in units pressed), the 5223 display defaults to the real-time display of the signal from the Left plug-in compartment.

If both the MEMORY CONTENTS DISPLAY and the vertical plug-in units Display buttons are pressed, and the 5B25N Time Base is set from 5 s to 0.1 ms/division, the Real Time Select signal "chops" between logic 1 and logic 0, allowing 5 μs for real-time display and 5 μs for memory, and so forth. When the 5B25N Time Base is set from 50 μs to 0.2 μs/division, the memory information is displayed during the time base's holdoff period.

Because the holdoff period is not defined, the reading of the memory is inhibited when the sweep is running. This ensures that the entire memory waveforms will be read—hence no systematic portions of memory record are passed over and not displayed.

Table 4-1 lists these conditions.

TABLE 4-1
Display vs. Real Time Select Conditions
[Roll and Output Saved Display(s) not operating]

Real-Time Display	Memory Display	Time/Div Setting	Real Time Select	Display
Off	Off	Any	High	Left real-time vertical.
On	Off	Any	High	Selected vertical.
Off	On	Any (except Amp)	Low	Selected memory display.
On	On	0.1 ms/div or slower (except Amp)	50%	Chops between selected displays—5 μs segments.
On	On	50 μs/div or faster	High during sweep; low during holdoff.	Displays portions of the memory during time base holdoff period.
On	On	Amp	High.	Selected vertical.

28. Sample Pulse. A TTL signal generated by the 5B25N Time Base to notify the 5223 mainframe when to sample the analog outputs of the left and right vertical plug-in amplifiers. With the 5B25N Variable Time/Division in the Calibrated position and the Time/Division set from 5 s to 0.1 ms, the repetition rate of the Sample Pulse is such that the Digitizer takes 100 samples per horizontal crt division. When the 5B25N Time/Div is set from 50 μs to 0.2 μs, one Sample Pulse occurs for each full real-time sweep and its associated holdoff period. This mode is called sequential-sweep mode; only repetitive waveforms can be stored and displayed properly.

29. Select Scratch Pad. A TTL signal from the A8-Digitizer Board that notifies the A11-Memory Board of the origin of a loaded serial byte. It identifies the byte as originating in the left or the right vertical sampler.

30. Serial Data. The principal output of the A8-Digitizer Board is Serial Data. A single serial byte is 10 bits in length (the MSB is the first bit in the series; the LSB is the last) whose value (a binary weighted fraction) represents the vertical signal position as captured and stored by the sampler. The serial byte is stepped into a shift register (see definition 10), then loaded in parallel into a scratch pad by the application of the Write Scratch Pad signal to the A11-Memory Board.

31. Single Sweep Mode. When the 5B25N Time Base is set to single-sweep, it causes a +5 V level on the Single Sweep Mode line. The Single Sweep Mode line goes via the Interface to the Memory, where it defeats the "full record" circuitry.

32. Sweep Rate. The dc level on the Sweep Rate line informs the Memory of the 5B25N Time Base's mode of operation. The dc levels on the Sweep Rate line, and their meanings, are:

DC Levels	Mode	Time/Div Setting
+4.35 to +5.0 V	Amplifier mode (memory off).	Ampl
+2.88 to +4.34 V	Enable roll mode.	5 s to 0.1 s
+0.7 to +2.87 V	Real-time sampled data.	5 s to 0.1 ms
0 to +0.69 V	Equivalent-time sampled data.	50 μs to 0.2 μs

33. Time Base Ramp. The buffered analog ramp from the A9-Interface to the A3-XYZ Board.

34. Vertical (Y) Memory Display Output. The Vertical (Y) Memory Display Output signal comes from the vertical memory via slew-rate-limited amplifiers on the A3-XYZ Board. The slew rate can be adjusted with the DISPLAY OUT SPEED control on the rear panel.

35. Vertical Drive. A relatively high-voltage (about 50 V) signal that represents the memory or analog vertical information. The Vertical Drive signal is selected by the Real Time Select signal, and used to drive the vertical deflection plates of the crt.

36. Write Scratch Pad. A TTL signal from the A8-Digitizer Board that causes the A11-Memory Board to load serial data, stored in a shift register, into a scratch pad latch. Gating signals on the A11-Memory Board route the Write Scratch Pad signal to the correct scratch pad, and generate write commands that cause the memory controllers to load the memory.

37. Z-Axis Analog. A signal the A9-Interface Board generates in response to Memory Intensify, Z-Axis Memory (Blank), Real Time Select, Z-Axis Time Base, Real Time Intensity, and Memory Intensity. The resulting signal (Z-Axis Analog) is sent to the A3-XYZ Board, providing type and amount of Z-Axis Drive information.

38. Z-Axis Drive. A relatively high-voltage (about 60 V) signal that represents the Z-Axis Analog signal, and provides on-off control of the crt beam.

39. Z-Axis Memory (Blank). A TTL signal from the A11-Memory Board that provides for interdot, intertrace, intervector, and end-of-record blanking. The Z-Axis Memory Blank signal is necessary to prevent the multiplexed crt display from having spurious lines when switching between displays.

40. Z-Axis Time Base. A TTL signal from the 5B25N Time Base that notifies the A9-Interface Board that the time base ramp is running (ramping up) and that the crt beam should be on to present the real-time display.

41. 1/$\overline{2}$ Left. A TTL signal from the A9-Interface Board for the A11-Memory Board. When a digital word is written in memory, the level on the 1/2 Left line indicates the state of the left plug-in channel switch at the time the sample was taken (except at 0.1 ms/division with two vertical plug-in units turned on). This identifies the origin of the digital word. See Figure 4-4.

42. 1/$\overline{2}$ Right. A TTL signal from the A9-Interface Board for the Memory Board. When a digital word is written in memory, the level on the 1/2 Right line indicates the state of the right plug-in channel switch at the time the sample was taken (except at 0.1 ms/division with two vertical plug-in units turned on). This identifies the origin of the digital word. See Figure 4-4.

CIRCUIT BOARD FUNCTIONS

INTERFACE BOARD

The Interface Board is the means by which plug-in units connect to the 5223 mainframe. The Interface Board selects Channel 1 or Channel 2 of the operating vertical plug-in unit(s) with the Left and Right Chan Sw Signals. The Interface receives Plug-In On/Off information from each plug-in unit, and an analog signal(s) from the one(s) that are on.

The Interface transfers:

1. analog signals from the vertical plug-in units to the XYZ Board,

2. control signals from the time base to the Digitizer and the Memory system, and

3. control signals from the vertical plug-in units to the Memory system.

DIGITIZER BOARD

The Digitizer samples the analog signals from the left and right vertical amplifiers and converts each sample to a serial 10-bit word. The Digitizer sends its data to the Memory system.

XYZ BOARD

The XYZ Board contains deflection amplifiers for the left and right vertical plug-in units (Y), the horizontal plug-in unit (X, time base) and intensity (Z) signals. The outputs of the XYZ Board go to the crt to produce the display.

HV BOARD

The HV Board produces high voltages and focus control for the cathode-ray tube.

FRONT PANEL BOARD

The Front Panel Board contains the graticule illumination circuit and the CALIBRATOR signal generator.

MEMORY & SWITCH BOARDS

The Memory and Switch Boards form the Memory System, which stores data from the Digitizer and upon command, displays that data.

5223 MEMORY SYSTEM

STRUCTURE

The 5223 memory has two separate systems—one for data from the left vertical plug-in compartment and one for data from the right vertical plug-in compartment.

Each compartment of memory is divided into two "pages" of 1024 words. Using this two-page arrangement permits the system to write data into one page while reading data for display purposes from the other page. This scheme of readout provides a flicker-free display because one of the pages may always be accessed for display. Once a complete display cycle has occurred, the pages will interchange their functions if the "acquisition" memory has been fully loaded.

Figure 4-5 shows a simplified block diagram of the memory system. Refer to Figure 4-5 when reading the following description.

The 10 MHz Clock from the Digitizer enters serial data from the Digitizer Board into the Serial-to-Parallel Converter on the Memory Board. The Scratch Pad Select and Write Scratch Pad signals, from the Digitizer Board, select the Scratch Pad (Left or Right), where the data will go and enter the data into that Scratch Pad.

The outlined circuitry, called Right Memory, shows the functions that enable the alternate read-write operations in the two memory pages. The Right Memory includes the following blocks:

- Control Functions
- Gated Buffers
- Write Address Counter
- Read Address Counter
- Address Multiplexers
- Start Sweep Register
- Read-Write Format Control
- Page A and Page B Memories

Control Functions, Gated Buffers and Address Multiplexers

The Control Functions block receives the Write Scratch Pad and $\overline{\text{Load Stop}}$ signals, and produces four outputs as follows:

a. The Write Clock signal, which increments the Write Address Counter and starts a memory-load sequence.

b. A Load signal, that occurs when the memory page receiving data is full, causes the Start Sweep Register to store the address where the last data was stored (this identifies the start of the waveform for display purposes).

c. The Address Select signal, which causes the Address Multiplexers to switch the read and write addresses to the appropriate memory page, depending on which page is being written to and which page is being read for display.

d. The control signals that turn on the Gated Buffers to route data to the written page and from the page being read to the output D/A Converters.

Write Address Counter

The Write Address Counter contains a number that relates the data words being written to their locations in memory. Each time a new word is stored in memory, the write address is incremented by one. The memory-load sequence continues until at least 1024 words have been loaded into the memory page. The P0, P1 Control line arranges bits P0 and P1 of the write address to match the sequence in which the Digitizer Board samples the input signals.

Read Address and Horizontal Position Counters

The Read Address Counter provides a sequence of addresses to cause an orderly readout of memory data. At the start of a memory-read sequence, the Read Address Counter receives a "start address" from the Start Sweep Register and the Horizontal Position Counter resets to zero. Read Clock pulses then increment both counters. The memory-read sequence proceeds repetitively at the Read Clock rate (220 kHz when the readout is to be displayed on the crt, or between 29 and 425 Hz when the readout is for an external chart recorder) until the other page is full. Then the Address Multiplexers "flip" the pages and start writing into this page and reading the other page.

Page A and Page B Memories

The Page A and Page B Memories receive data from the Scratch Pad via the Gated Buffers. Only two of the Gated Buffers (in the Right Memory block) are on at any time—one input and one output. For example, if the Page A Memory is being written and the Page B Memory is being read, the input buffer for Page A will be gated on and the input buffer for Page B will be gated off. Similarly, the output buffer for Page A will be gated off and the output buffer for Page B will be gated on.

Read-Write Format Control

The Read-Write Format Control produces two signals that (a) determine whether the two least-significant bits of the write address (P0, P1) will be in normal or reversed order, and (b) selects either bit Q0 of the read address or the Mem Ch 1/$\overline{\text{Ch 2}}$ Select signal as the least significant bit of the read address.

RECORD INTENSIFIER

The Record Intensifier receives the A Gate, $\overline{\text{Load Stop}}$ and $\overline{\text{Roll}}$ signals. When the A Gate line is active, the Record Intensifier sets Bit 11 high. Bit 11 stays high until the $\overline{\text{Load Stop}}$ pulse occurs. The memory stores Bit 11 with incoming data. When the memory is being read out, Bit 11 is sent to the Z-Axis Control circuit on the Interface Board. The Z-Axis Control intensifies the memory data that was stored while Bit 11 was low. The effect of this is to intensify the part of the memory display that occurred before the real-time sweep was triggered.

A low $\overline{\text{Roll}}$ signal will also set Bit 11 high. The pretrigger function is not used in Roll mode.

ROLL MODE

In the Roll mode the memory display is updated at the same rate that the input signal is being digitized. This means the user doe not have to wait for the entire memory to be filled before a memory display is available. Roll mode is available at sweep speeds of 0.1 ms/division and slower.

In Roll mode the Start-Sweep Register increments with every Write Clock rather than waiting for a $\overline{\text{Load Stop}}$ as in normal mode. The memory then receives data at a rate set by the sample rate of the time base, and reads out continuously at 220 kHz between sample pulses. Only the Page A Memory is used in the Roll mode.

CHART OUT OPERATION

Data about waveforms that are both displayed and saved will be applied to the rear-panel MEMORY DISPLAY OUTPUTS (X and Y) when the OUTPUT SAVED DISPLAY(S) button is pressed. The data will be read out at a slow rate to accommodate a chart recorder. The rate of readout is adjustable from 14 to 212 Hz with the rear-panel DISPLAY OUT SPEED control.

LEFT VS RIGHT OPERATION

The 5223 will produce a Left Vs Right display by applying the outputs of the Left and Right Memories to the Vertical and Horizontal D/A Converters and Amplifiers,

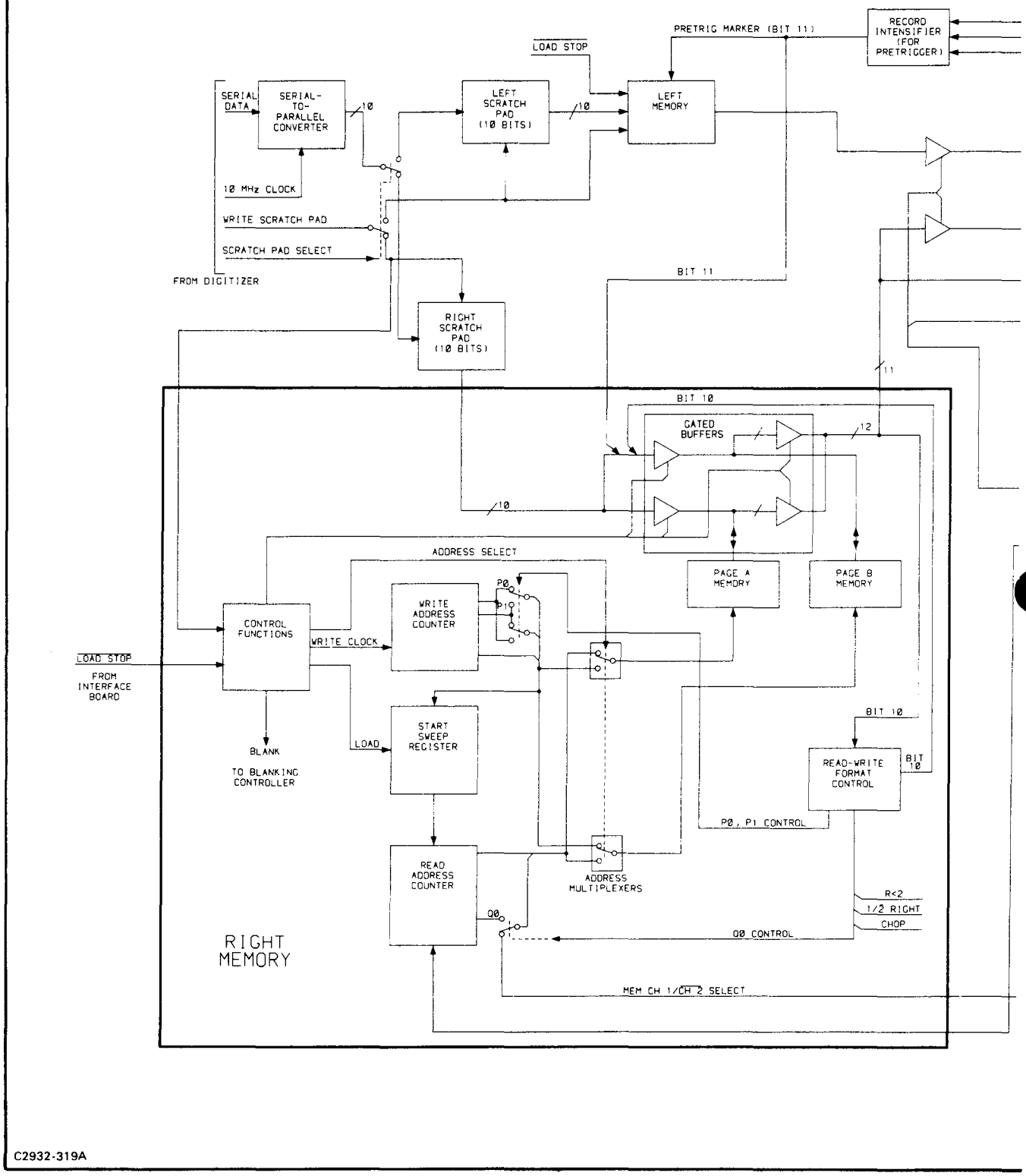


Figure 4-5. Simplified block diagram of Memory System.

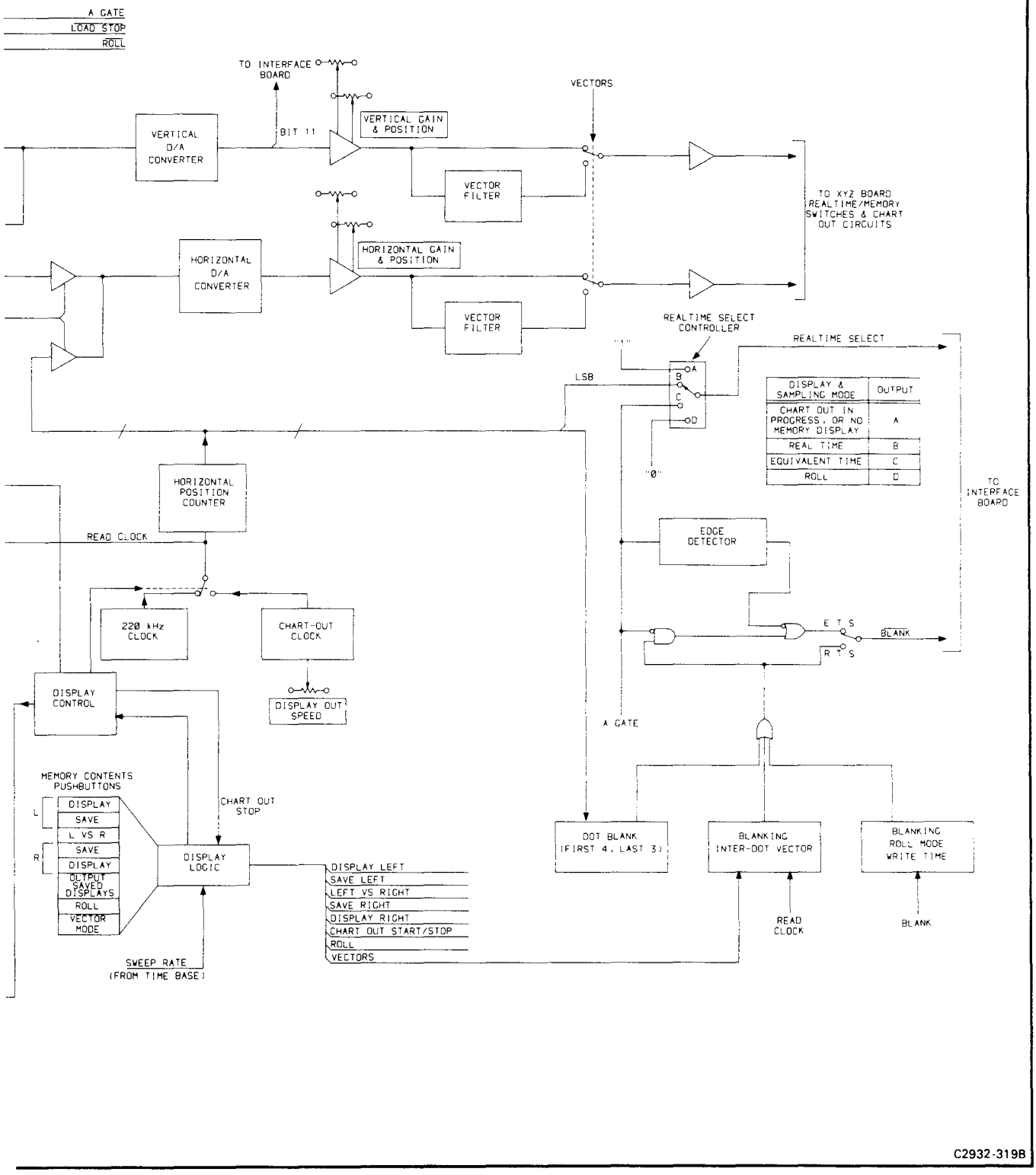


Figure 4-5 (cont). Simplified block diagram of Memory System.

respectively. This differs from a normal memory display (Y versus Time), in which the Horizontal D/A Converter receives the output of the Horizontal Position Counter.

PRETRIGGER DISPLAY

When the system is operating in real-time sampling mode (0.1 ms/division and slower), the 5B25N's Pretrigger control permits the operator to select, with respect to the trigger point of the real-time display, the part of the input signal that the memory will store and display. The part of the memory display that occurs before the trigger point of the real-time display will be intensified. The result is as follows:

a. When the Pretrigger control is set to 0%, the memory display is the same as the real-time display. None of the display is intensified.

b. When the Pretrigger control is set to 50%, the trigger point of the real-time display appears at the middle of the memory display. The first part of the memory display shows the signal that preceded the real-time trigger point; this part of the display is intensified. The second part of the memory display, from the real-time trigger point at mid-screen to the end of the display, shows the signal that followed the trigger event.

When the Pretrigger control is set to some other point between 0% and 100%, the trigger point of the real-time display will appear at the appropriate point to show the corresponding percentage of the pretrigger signal.

c. When the Pretrigger control is set to 100%, the trigger point of the real-time display appears at the right end of the memory display. The memory display then consists entirely of signals that preceded the trigger point of the real time display.

The pretrigger portion of the memory display is governed by the relationship between the Load Stop pulse and the point where the real-time sweep triggers, which is selected by the setting of the Pretrigger control on the 5B25N Time Base. The Load Stop pulse tells the memory to stop loading data words from the Digitizer, and the start-sweep register stores the address where the last word was stored. When this page of memory is displayed, the display ends at the memory address where the Load Stop occurred. Figure 4-6 shows the relation between the input signal, the real-time sweep, the setting of the Pretrigger control, the Load Stop pulse and the memory display.

OVERVIEW OF MEMORY OPERATION

This description gives an overview of the operation of the 5223 Memory System, as shown on diagram 19 in the foldout section. Each block has a name, an identifying code and a number that tells which schematic diagram shows the circuitry in that block. For example, at the bottom left of the Block Diagram we see the Left Memory Load Controller, block DD, with a number 13 in a diamond. The number 13 in the diamond means that diagram 13 shows the circuitry of the Left Memory Load Controller, block DD.

The names on the lines that connect the blocks are sometimes actual signal names used on the schematic diagrams, and sometimes names that describe a function. This description uses the names from the Block Diagram.

The circuitry shown on diagrams 10 through 18 forms the 5223 Memory System. Diagrams 10 and 18 depict circuitry located on the Switch Board, and the circuits shown on diagrams 11 through 17 are located on the Memory Board.

The Serial-to-Parallel Converter (SPC, block HH on diagram 11) converts serial data from the Digitizer to 10-bit data bytes. The Gated Clock from the Digitizer clocks data into the SPC. The Digitizer also activates the Write and Select lines. These signals are used by the Scratch Pad Controller to produce write commands, for the Left and Right Write-Command Controllers, and Write signals. The Write signal goes to the Converter Scratch Pad.

The Converter Scratch Pad (CSP, block II on diagram 11) temporarily stores the 10-bit byte from the Serial-to-Parallel Converter. The Write signal from the Scratch Pad Controller activates the CSP. When activated, the CSP applies parallel data to the Page A and Page B Buffered Memories in the left and right memories.

The Load Stop Buffer (block P on diagram 12) buffers the time base's Load Stop signal. If complete records exist, a Buffered Load Stop is sent to the Left and Right Memory Record-Full Detectors to stop loading data into memory records. Buffered Load Stop also goes to the Record Intensify Generator, block WW on diagram 11.

The Record Intensify Generator (block WW on diagram 11) uses the A Gate signal from the Interface Board and Buffered Load Stop to generate Memory Intensify. The Memory Intensify signal is normally stored in memory with the appropriate record. The stored record can then be displayed with an intensified part. The intensified part was stored in memory before the real-time trigger, i.e., pre-trigger view.

The Sweep Rate line from the Interface board is applied to the Digitizer Time-Base Detector and to the Equivalent-Time Detector.

The Digitizer Time-Base Detector (block LLL on diagram 10) monitors the Sweep Rate line to decide whether the memory display indicators should be enabled (Display Enable output to blocks NNN and HHH), and whether the Roll mode should be enabled (Roll Disable output to block III). If the time base is not a digitizer unit, or if the digitizer time base is in the amplifier mode, the memory buffered display indicators and the display functions of the 5223 are shut off. If the digitizer time base is set to 50 ms/div or faster, the Roll Disable function is activated, which prevents Roll mode.

The Equivalent-Time Detector (ETD, block Q on diagram 12) also monitors the Sweep Rate line and, if both memory and real-time displays are selected, decides whether to "chop between memory and real-time," or "display memory during the real-time sweep's hold-off time." The ETD produces the Display Memory During Holdoff signal for the Real-Time Select Controller (block H on diagram 12).

The Debounced Switch Control (DSC, block FFF on diagram 10) converts the mechanical positions of the MEMORY CONTENTS pushbuttons to "debounced" electrical signals. Signals representing Display Left, Save Left, Left vs. Right, Save Right, and Display Right are sent from the DSC to the Control Output Normalizer Left vs. Right (block GGG on diagram 10). The Dots Joined signal goes from the DSC to the Tri-State Test Port on block HHH. The Roll signal goes from the DSC to the Roll Command Modifier on block III. The Chart Out signal goes from the DSC to the Chart Out Toggle on block KKK.

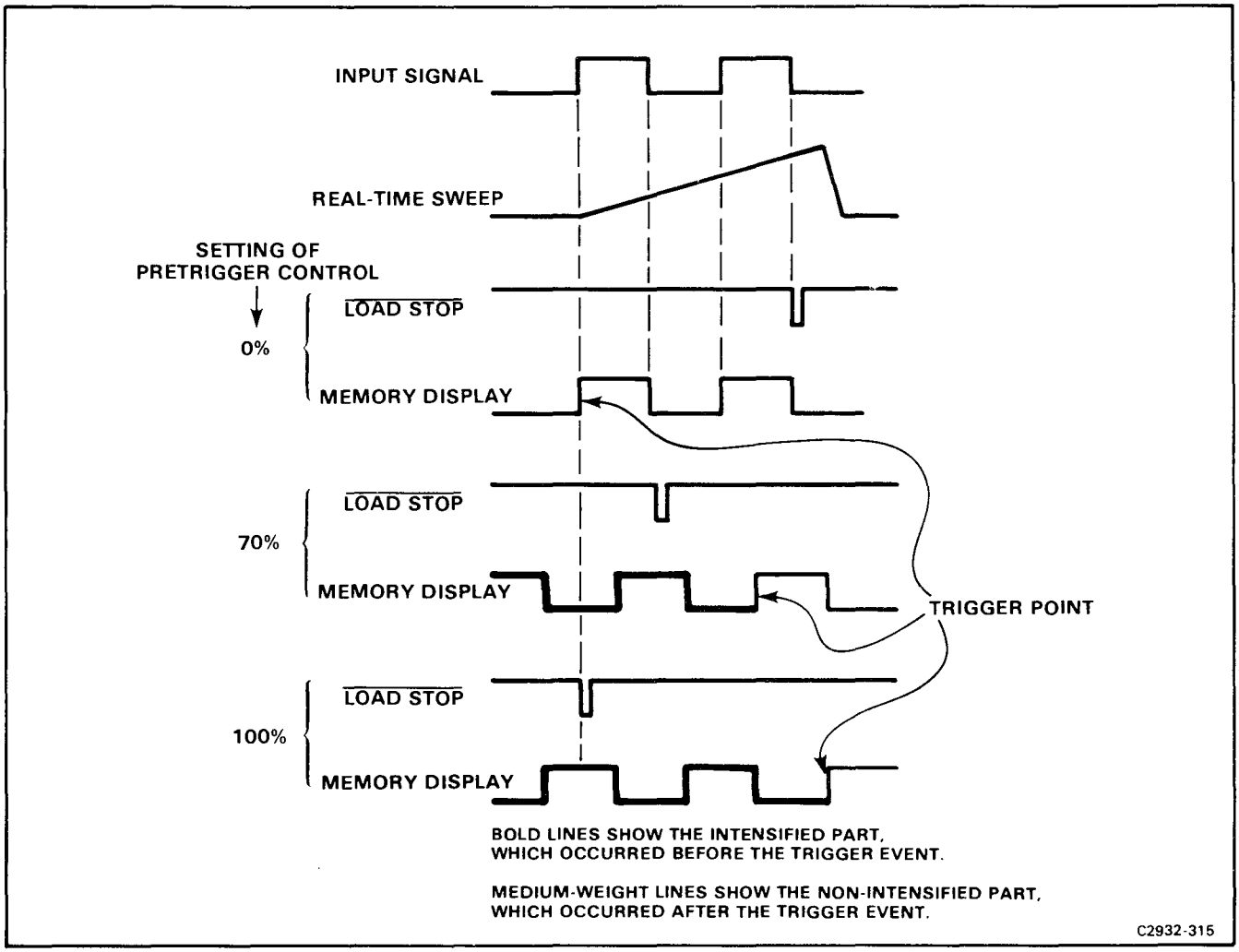


Figure 4-6. Relation of input signal, real-time sweep, Pretrigger control, Load Stop and memory display.

The outputs of the Control Output Normalizer Left vs Right (on block GGG of diagram 10) are called Display functions. The Display functions are sent to the Left On or Right On Detector (block JJJ on diagram 10), the Tri-State Test Port (block HHH on diagram 10), the Output Status Detector (block MMM on diagram 10), and the Buffered Display Indicators (block NNN on diagram 10).

The Left On or Right On Detectors monitor the display functions. If either or both Display Left or Display Right are active, the Left + Right On output will be active and sent to the Roll Command Modifier, block III.

The Roll Command Modifier (block III on diagram 10) receives the Roll input from the front-panel ROLL button, the Left + Right On and the Roll Disable signals from the Digitizer Time-Base Detector and generates Roll for the Tri-State Test Port.

The Output Status Detector (block MMM on diagram 10) monitors display functions and, if Display Left and Save Left have been enabled, or if Display Right and Save Right have been enabled, produces a signal that resets the Chart Out Toggle.

If the Chart Out Toggle (block KKK on diagram 10) has been reset by the Output Status Detector, the Chart Out pulse from the Debounced Switch Control will set the Chart Out Toggle. The Chart Out Toggle will then produce the Chart Out Start signal, which connects to the Tri-State Test Port. The Chart Out Toggle is normally reset by the Chart Out Reset signal; however, it can also be reset if the enable from the Output Status Detector is defeated.

The Chart Out Start/Stop Decoder (block D on diagram 12) monitors the status of displayed memories and the output of the Memory Record Timeshare Generator (block L) to detect the end of an output sequence of memory records. The Chart Out Start/Stop Decoder generates the Chart Out Reset signal, which goes to the Chart Out Toggle (block KKK on diagram 10) circuit via the Output Status Detector (block MMM on diagram 10); and the "start location" signal for the Memory Record Timeshare Generator (block L on diagram 12).

The Tri-State Test Port (TSTP, block HHH on diagram 10) interfaces the Memory Board to the Switch Board. For test purposes, a high-logic level on pin 8 of J15 will disable all control outputs from the Switch Board and thereby allow the control lines to the Memory Board to be exercised independently. The TSTP has three groups of outputs, Display, Chart Out Start, and Display Mode. Display consists of Display Left, Display Right, and Left vs Right. The Display signals are sent to the D/A Converter Data Controller (block A on diagram 17). The Chart Out Start signal is sent to the Pen-Lift Detector and the Read Clock Controller (blocks G and N on diagram 12). Lastly, the Display Mode signals are sent to the Chart Out Start/Stop Decoder, so that chart out start and stop locations can be determined, and to the Display Function Generator.

The Memory Record Timeshare Generator (MRTG, block L on diagram 12) serves as the source for timesharing the displayed memory records. The output from this block goes to the Chart Out Start/Stop Decoder, the D/A Converter Data Controller and the Pen-Lift Detector (blocks D, A, and G on diagram 12, respectively).

The Display Function Generator (DFG, block E on diagram 12) monitors the Display Mode lines from the Tri-State Test Port. If either Display Left or Display Right for the memory is on, a Memory On signal will be generated. If Display Left or Display Right for real time is on, a Real Time On signal will also be generated. These two signals go to the Blanking Source Generator and Blanking Output (blocks J and I on diagram 12).

The Pen-Lift Detector (block G on diagram 12) generates a Chart On pulse when Chart Out Enable is active. The Chart On Pulse goes to the Chart Out Initializing circuit (block F, diagram 12). The Pen-Lift Detector also triggers the pen-lift hold-off timer on the XYZ Board.

The D/A Converter Data Controller (block A, diagram 17) monitors the Display Mode and Left/Right Mux signals to generate the Buffer Select signals for the Buffered Vertical D/A Converter and the Buffered Horizontal D/A Converter (blocks B and C on diagram 17). The Buffer Select signals determine which pairs of data input buffers will be activated.

The Buffered Vertical D/A Converter (block B, diagram 17) receives Left Record Data and Right Record Data from the left and right memory systems. Depending on the status of the Buffer Select lines, the Buffered Vertical D/A Converter generates a scaled output current for the Switch Board.

The Buffered Horizontal D/A Converter (block C, diagram 17), receives Right Record Data from the right memory system and Horizontal Data from the Horizontal Position Counter. The Buffered Horizontal D/A Converter produces a scaled output current for the Switch Board. Depending on which input buffer is enabled, that current will represent the Right Record or the horizontal position.

The Adjustable Low-Speed Clock comes from the XYZ Board to the Read Clock Source Controller (block N, diagram 12). The DISPLAY OUT SPEED control governs

the repetition rate of the Adjustable Low-Speed Clock.

The Read Master Oscillator (block M, diagram 12) generates a 440 kHz reference signal for the Read Clock Source Controller.

The Read Clock Source Controller (Block N, diagram 12) selects one of two sources for its output clock, which it sends to the Read Clock Delay circuit (block TT, diagram 11). The rate of the Clock pulse determines the speed at which memory data is fetched out of the Left and Right Buffered Memories.

The Horizontal Position Counter (HPC block 000, diagram 17) generates horizontal data for the Buffered Horizontal D/A Converter (block C, diagram 17) and the End-of-Sweep Detector (block S, diagram 12). The horizontal data is a binary weighted ramp that starts at "0" and is incremented to "1023." At position 1023 the HPC generates an End-of-Sweep pulse that goes to the Memory Sweep Reset circuit (block R, diagram 16). The HPC also produces Position #4, which is sent to the Pen-Lift Output Control to let the pen drop to the chart paper, and to the Blanking Source Generators (block J, diagram 12) which allows memory record traces to be displayed.

The End-of-Sweep Detector (block S, diagram 12) determines when position #1021 has occurred, at which time a Pre-End-of-Sweep Trigger is generated and sent to the Pen-Lift Output Control and the Blanking Source Generators (blocks O and J on diagram 12).

The Blanking Source Generators (BSG, block J on diagram 12) produce blanking signals that provide for dot-to-dot, record-to-record, vector-to-vector, and roll-mode update movements. The BSGs produce the Blank pulse for the Blanking Controller.

The A Gate signal from the Interface Board is applied to the Blanking Output and the Real-Time Select Controller (blocks H and I on diagram 12). A high-logic level on A Gate indicates the real-time sweep is operating.

The Real-Time Select Controller (block H, diagram 12) generates the Real-Time Select and $\overline{\text{Early Real-Time Select}}$ signals. The Real-Time Select signal causes the XYZ Board to select the analog signals for display on the crt (memory and real-time). The Real-Time Select to the Interface Board selects the Memory Intensity or the Real-Time Intensity control as the input to the Z-Axis circuit. If the 5223 system is in an equivalent-time sampling mode the $\overline{\text{Early Real-Time Select}}$ signal goes to the Blanking Controller, which causes the memory contents to be displayed during real-time sweep hold off, that is, when A Gate is low.

The Blanking Controller (block K on diagram 12) uses the Blank pulse to generate Blank Control which goes to the Blanking Output circuit. Blanking control can be pre-empted upon receipt of $\overline{\text{Early Real-Time Select}}$.

The Blanking Output circuit (block I, diagram 12) monitors the Blank Control, Memory On, Real Time On, and A Gate signals. Depending on the status of these signals, the Blanking Output circuit generates $\overline{\text{Blank}}$, which goes to the Interface Board. Real-time and equivalent-time sampling cause two different operations, as follows:

Case #1: If the 5223 acquisition system is in real-time sampling mode, the Blanking Output circuit buffers Blank Control to form $\overline{\text{Blank}}$.

Case #2: If the 5223 acquisition system is in equivalent-time sampling mode, the Blanking Output circuit generates a $\overline{\text{Blank}}$ signal to shut off the crt beam during the transition from memory to real-time and from real-time to memory.

The Chart Out Initializing Circuit (block F, diagram 12) monitors the Chart On pulse and generates the Sweep Reset and Chart Load signals. Sweep Reset goes to the Memory Sweep Reset circuit, where it causes an Address Load, a Clear Pulse, and a Flip Page Pulse to be generated. The Chart Load signal goes to the Memory Record Timeshare Generator, which sets up the memory system so that the proper sequence of memory output will occur.

The Memory Sweep Reset circuit (MSR, block R, diagram 12) generates the following outputs:

1. Page Pulse, which goes to the Horizontal Position Counter (block 000),

2. Address Load, which goes to the Left Read counter and the Right Read Counter, and

3. Flip Page Pulse, which goes to the Sequencer Buffer-Selectors. The Page Pulse sets the Horizontal Position Counter to location zero regardless of its previous location. The Address Load signals will force the Left and Right Read Counters to load the start-sweep addresses at their inputs. Flip Page Pulse is for the Memory Sequencers.

The Pen-Lift Output Control (block O, diagram 12) generates Pen-Lift/N.O. or N.C. by opening a set of relay contacts that are normally closed or closing a set of contacts that are normally open. This occurs if the system is in a "chart out" mode. The Pen Lift signal starts

upon receipt of the Pre-End of Sweep signal and ends upon receipt of position #4.

The Left Page A Buffered Memory (block JJ, diagram 15) stores waveform record information. Depending on the state of the Buffer Select control lines, waveform record information will be loaded or sent to the Buffered Vertical D/A Converter as Left Record Data. The Buffer Select signal is supplied to both Left Page A and Left Page B Buffered Memories from the Sequencer Buffer-Selector. The locations where waveform record bytes are stored will be determined by the Address signal from the Left Page A Address Multiplexer.

The Left Page B Buffered Memory (block KK, diagram 15) stores waveform record information just as Page "A" does. The locations where waveform record bytes are stored will be determined by the Address signal from the Left Page B Address Multiplexer.

The Left Page A and Left Page B Address Multiplexers (block MM and NN, diagram 15) use the Buffer Select signal from the Sequencer Buffer-Selector to determine which address, write or read, will be passed to the Left Page A and Page B Buffered Memories as Address.

The Left Write Counter (LWC, block PPP, diagram 15) generates Write Address and sends it to the Left Page A and Page B Address Multiplexers and the Left Start Sweep Register. The Write Address provides storage location information. The Write Clock signal from the Sequencer Buffer-Selector increments the LWC. The LWC also receives special information from the Left Write-Address Normalizer - the Mix Address signal.

The Left Write-Address Normalizer (block RR, diagram 15) receives the Chop Format Active signal from the Chop Transceiver (block XX). If the Chop Format Active signal is present and the memory is to be loaded as a dual record, the Mix Address signal is activated and sent to the Left Write Counter.

The Chop Transceiver (block XX, diagram 11) monitors the Chop Format Active line to the Interface Board and determines the status of chop mode. When the 5223 is in roll mode or equivalent-time sampled mode, the transceiver sends a Chop command to the Interface Board.

The Sequencer Buffer-Selector (SBS, block U, diagram 13) generates the Write Clock pulse from State Control, and sends it to the Left Memory Record-Full Detector (LMRFD, block FF) and the Left Write Counter. The SBS produces the Write Left Adrs signal for the Left Memory Load Controller. The LMRFD keeps track of the number of write commands used per record. After 1024 write commands have occurred, the LMRFD will allow the next Load Stop to pass as Gated Stop. Gated Stop is then passed on to the SBS.

The Left Ch 1/Ch2 Hold-Off Generator (block X, diagram 13) is used in dual-channel alternate operation only. For example, as the 5223 is digitizing and displaying Left Ch 1, a Load Stop may occur before the end of the real-time sweep. When this Load Stop occurs, loading of the memory must stop until the Ch 1/Ch 2 marker has changed from Ch 1 (for this example) to Ch 2. The hold off generator produces the Hold Off signal and sends it to the Left Write-Command Controller (block AA, diagram 13).

The Left Memory Load Controller (LMLC, block DD, diagram 13) receives the Write Left Adrs signal which is used to generate the Left Page Full, End-of-Record, and Page-Flip Enable signals. End-of-Record is generated each time Write Left Adrs is active. (Write Left Adrs means "write the left start sweep location in the register," at block 00.) The Page-Flip Enable and Left Page Full signals mean that the last written page of memory is now full and ready to be flipped into the reading mode. Left Page Full is sent to the Left Write Command Controller (block AA) to prevent further write commands to the Left Memory Sequencer. The End-of-Record signal is sent to the Left Register Controller (block QQ).

The Left Write Command Controller (LWCC, block AA, diagram 13) gates the Write Left signal from the Scratch Pad Controller. The signals used for gating are Hold Off, from the Left Ch 1/Ch 2 Hold-Off Generator, and Left Page Full from the Left Memory Load Controller. The output of the LWCC is the Write Start signal which goes to the Left Memory Sequencer (Block T, diagram 13).

The Left Power-Up Sequencer Reset circuit (LPUSR, block Z, diagram 13) provides the Left Reset signal to the Left Memory Sequencer (block T). The Left Reset signal will be activated when the LPUSR circuit determines that the Left Memory Sequencer is in a faulty reset state.

The Left Memory Sequencer (LMS, block T, diagram 13) provides the State Control signals to the Sequencer Buffer-Selector (block U) so that the selector can cycle the memory properly when loading record information. State Control is activated upon receipt of the Write Start signal.

When it receives the End-of-Record signal, the Left Register Controller (LRC, block QQ, diagram 15) generates the Load signal for the Left Start-Sweep

Register (LSSR). The Load signal provides the necessary timing and, in conjunction with U1320 and U1450D, causes the LSSR control signals to cycle the LSSR. The LSSR serves to store record-start-sweep locations, which is necessary because of pretrigger view properties of the 5223. Upon receipt of the Load signal, the LSSR will load and retain the arbitrary location of the Write Address signal. The Record Start Address signal is sent to the Left Read Counter (block PP on diagram 15).

When two record waveforms have been stored, the Left Record Sorting circuit (LRS, block SS, diagram 15) sorts Channel 1 record information from Channel 2 record information in memory. The sorting takes place only when two records are stored in memory and marked as such. The LRS circuit sends the L Ch 1/Ch 2 Marker to the Left Read Counter (LRC), where it becomes the LSB of the Read Address. When the LSB is a 1 it indicates that Ch 1 data is being read from memory; and when the LSB is a 0 it indicates that Ch 2 data is being read from memory. The LRC also generates the Read Address for the Left Page A and Page B Address Multiplexers. The Read Address will be used to address locations in memory so that the stored records will be called back in the same order in which they were stored. The Record-Start Address signal gives the LRC a starting place.

The Read Clock Delay circuit (RCD, block TT, diagram 11) delays the Clock signal from Block N. This permits the crt to be blanked before changing the displayed record information. The Delayed Read Clock signal goes to the Left and Right Read Counters and the Horizontal Position Counter.

The Right Page A Buffered Memory (RPABM, block UU, diagram 16) stores waveform record information. Depending on the state of Buffer Select, waveform record information will be loaded from parallel data or sent to the Buffered Vertical and Horizontal D/A Converters as right record data. The Buffer Select signals are supplied to both Right Page A and Right Page B Buffered Memories from the Sequencer Buffer-Selector. The location where waveform record bytes are stored will be determined by the Address data supplied by the Right Page A Address Multiplexer (block YY, diagram 16).

The Right Page B Buffered Memory stores waveform record information, just as Page A does. The locations where waveform record bytes are stored will be determined by Address data supplied by the Right Page B Address Multiplexer (block ZZ, diagram 16).

The Right Page A and Page B Address Multiplexers (blocks YY and ZZ on diagram 16) use the Buffer Select signal from the Sequencer Buffer-Selector to determine which address, write or read, will be passed as Address data to the Right Page A and Page B Buffered Memories.

The Right Write Counter (RWC, block QQQ, diagram 16) generates the Write Address and sends it to the Right Page A and Page B Address Multiplexers and the Right Start Sweep Register. The Write Address provides the storage location information. The RWC is incremented by the Write Clock signal from the Sequencer Buffer-Selector, block W. The RWC also receives the Mix Address signal from the Right Write-Address Normalizer, block DDD.

The Right Write Address Normalizer (block DDD, diagram 16) receives the Chop Format Active signal from the Chop Transceiver (block XX). If chop is active and memory is to be loaded as a dual record, the Mix Address signal is activated and sent to the Right Write Counter.

The Sequencer Buffer-Selector (SBS, block W, diagram 14) generates the Write Clock from State Control, and sends it to the Right Memory Record Full Detector (RMRFD) and the Right Write Counter (blocks GG and QQQ). The Write Right Adrs signal goes to the Right Memory Load Controller. The RMRFD (block GG) keeps track of the number of write commands used per record. After 1024 write commands have occurred, the RMRFD will allow the next Load Stop to pass to the SBS as Gated Stop.

The Right Ch 1/Ch 2 Hold-Off Generator (block Y, diagram 14) is used in dual-channel alternate operation only. As the 5223 is digitizing and displaying Right Ch 1, a Load Stop may (probably will) occur before the end of the real-time sweep. When this Load Stop occurs, loading of the memory must stop until the Ch 1/Ch 2 marker has changed from one channel to the other. The Hold-Off Generator produces Hold-Off and sends it to the Right Write Command Controller (block BB, diagram 14).

The Right Memory Load Controller (block EE, diagram 14) receives Write Address, which is used to generate the Right Page Full, End-of-Record, and Page-Flip Enable signals. End-of-Record is generated each time Write Right Adrs is active (which means "write the right start-sweep location in the register," block AAA, diagram 16). The Page-Flip Enable and Right Page Full signals mean that the last written page of memory is now full and ready to be flipped into the reading mode. Right Page Full goes to the Right Write Command Controller (block BB, diagram 14) to prevent further Write Commands to the Right Memory Sequencer. The End-of-Record signal goes to the Right Register Controller (block CCC, diagram 16).

The Right Write Command Controller (RWCC, block BB, diagram 14) gates the Write Right signal from the Scratch Pad Controller. The signals used for gating are $\overline{\text{Hold-Off}}$ from the Right Ch 1/Ch 2 Hold-Off Generator, and Right Page Full, from the Right Memory Load Controller. The output of the RWCC is the Write Start signal which goes to the Right Memory Sequencer (block V, diagram 14).

The Right Power-Up Sequencer Reset (RPUSR, block CC, diagram 14) provides the Right Reset signal to the Right Memory Sequencer (block V). Right Reset will activate any time the RPUSR determines that the Right Memory Sequencer is in a faulty reset state.

The Right Memory Sequencer (block V, diagram 14) provides the State Control signal to the Sequencer Buffer-Selector (SBS) so that the SBS can cycle memory properly when loading record information. The State Control line is activated upon receipt of Write Start.

When it receives the End-of-Record signal, the Right Register Controller (block CCC, diagram 16) generates the Load signal for the Right Start Sweep Register (block AAA). The Load signal provides the necessary timing and, in conjunction with U1691A and U1495C, causes block AAA control signals to cycle the Start Sweep Register.

The Right Start Sweep Register (RSSR, block AAA, diagram 16) stores record-start-sweep locations. This is necessary because of pretrigger-view properties of the 5223. When the Load signal occurs, the RSSR will load and retain the arbitrary location of the Write Address signal. The Record Start Address signal goes to the Right Read Counter (block BBB).

When two waveform records have been stored, the Right Record Sorting circuit (RRS, block EEE, diagram 16) sorts Channel 1 record information from Channel 2 record information in memory. The sorting takes place only when two records are stored in memory and marked as such. The RRS circuit sends the R Ch 1/Ch 2 Marker to the Right Read Counter (block BBB) output, where it becomes the LSB of the Read Address. When the LSB is a 1 it indicates that Ch 1 data is being read from memory; and when the LSB is a 0 it indicates that Ch 2 data is being read from memory.

The Right Read Counter (RRC, block BBB, diagram 16) generates the Read Address for the Right Page A and Page B Address Multiplexers. The Read Address will be used to address locations in memory so that the stored records will be called back in the same order in which they were stored. The Record Start Address gives the RRC a starting place.

DETAILED CIRCUIT OPERATION

This part of the Theory of Operation section provides a detailed description of the electrical operation, and relationship of the circuits in the 5223. The theory of operation for circuits unique to this instrument is described in detail in this discussion. Circuits commonly used in the electronics industry are not described in detail.

Complete schematic diagrams are provided in Section 9, Diagrams and Circuit Board Illustrations. For diagrams 1 through 18, the number inside the diamond preceding a heading in the following discussion refers to the schematic diagram for that circuit. The schematic diagrams contain shaded borders around the major stages of the circuits to conveniently locate the components mentioned in the following discussions. The name of each stage is given in a shaded box on the diagram, and as a sub-heading in the discussion of that schematic diagram.

Diagrams 21 through 24 depict the GPIB/Memory Board Interface. Because the firmware will diagnose the circuitry on diagrams 21 through 24, no detailed description is included. Instead, an overview describes the circuitry of diagrams 21 through 24.

Diagrams 10 through 18 depict, and diagram 19 is a block diagram of, the Memory System. In diagram 19, each block has a name, an identifying code, and a number that tells which diagram shows its circuitry. For example, at the lower right of the Block Diagram we find the Right Memory Load Controller, block EE, with the number 14 in a diamond. The number 14 means that the circuitry of the Right Memory Load Controller is shown on diagram 14.

TEKTRONIX DRAFTING CONVENTION

Logic symbols on the schematics are drawn according to the function performed by the device in its particular application. By so doing, some deviations from the manufacturer's assigned symbology occur (although device electrical function is identical). An example of this would be an AND gate (all inputs high—output high; any input low—output low) drawn as an OR gate for low inputs (any input low—output low; all inputs high—output high). For operational characteristics of individual devices, refer to the manufacturer's data book.

◇1 MAIN INTERFACE

The Main Interface is the means by which the plug-in units connect to and "communicate with" the 5223 mainframe. This discussion concerns the 10 groups of circuitry on the Main Interface board, as follows:

1. Vertical Signal Buffers
2. Horizontal Signal Buffer
3. Left and Right Trigger Buffers
4. Z-Axis Control Signal Generator
5. Single Sweep Reset Generator
6. Sweep Gate or Sample Pulse Selector
7. Chop-Alternate Logic
8. Channel-Switch Logic
9. Vertical Channel Switch Control
10. Multi-Channel Plug-In Detectors

VERTICAL SIGNAL BUFFERS

A pair of emitter followers at each vertical plug-in connector supplies the plug-in output signals to the Digitizer board. Q250 and Q251 transfer the signal from the left vertical plug-in connector and Q441 and Q442 transfer the signal from the right vertical plug-in connector to the Digitizer board via P1 and P3 respectively. The diodes on the emitters of the four transistors limit the signal amplitude and the RC networks in the output leads optimize the transient response.

HORIZONTAL SIGNAL BUFFER

Emitter-followers Q740 and Q840 transmit the output signals from the horizontal plug-in connector to the XYZ board.

LEFT AND RIGHT TRIGGER BUFFERS

Emitter-followers at each vertical plug-in connector transmit the Trigger signals to the horizontal plug-in connector. Because the emitter-followers are similar, only the left one is described here. The left vertical plug-in produces a Trigger signal that is 250 mV in amplitude per division of crt deflection. Diode CR360 level-shifts the signal about 0.6 V positive, and Q350 shifts its level about 0.6 V negative. Because of this, the signal leaves Q350 at the same dc level and at practically the same amplitude as it entered. The left Trigger signal connects to pins A3 and B4 of the horizontal plug-in connector. The amplitude of the Trigger signal at the input to the horizontal plug-in depends on the input impedance of the

time base in use. The 5B10, 5B12, and 5B13 have high input impedance which does not attenuate the Trigger signal—it stays at 250 mV per division of crt deflection. Other 5B-series time bases have 63-ohm impedance which results in a nominal signal amplitude of 50 mV/division of crt deflection.

The right vertical trigger amplifier is similar to the left one. The right trigger signal is connected to pin A4 of the horizontal plug-in connector.

Z-AXIS CONTROL SIGNAL GENERATOR

Circuitry on the Interface board combines the following signals:

1. The Intensify signals from the three plug-in compartments,

2. The Chan Switch/Chop Blank signal from U630D,

3. The levels from the front-panel INTENSITY and MEM INTEN controls,

4. The sum of the A Swp Z-Axis and B Swp Z-Axis signals, and

5. Signals from the Memory board.

Circuitry on the Interface board uses these signals to produce an output current called Z-Axis. The Z-Axis current controls the Z-Axis Amplifier so that an increase in current brightens the display.

In real-time operation, the A and B Swp Z-Axis signals, the Intensify signals from the three plug-in compartments, the Real-time Intensity and the Chop Blank signals are summed into the emitter of Q641. Transistor Q641 supplies the Z-Axis signal current to the Z-Axis Amplifier (diagram 5). Diode CR633 limits the voltage excursion at the emitter of Q641.

In memory operation, the Memory Intensity signal, the $\overline{\text{Memory Intensify}}$ signal, and the $\overline{\text{Blank}}$ signal from the Memory board combine to drive transistor Q640. The output current of Q640 combines with the output current of Q641 to form the Z-Axis drive current.

Gates U700B, U700C, U630A and U630B form the blanking logic circuit. This circuit accepts the Chop Blank, Realtime Select, and memory $\overline{\text{Blank}}$ signals.

The Real Time Select line controls gates U700C and U630A. A high-logic level on Real Time Select causes U700B to apply a low-logic level to pin 8 of U700C, thus enabling it to respond to the Chop Blank signal. The same high-logic level on the Real Time Select line disables U630A so it cannot respond to inputs on the memory $\overline{\text{Blank}}$ line.

When U630B is activated, its high-logic level output cuts off conduction in Q641, which causes the Z-Axis Amplifier to blank the Real Time display. Any of three conditions will activate U630B, as follows:

1. A high-logic level on the Chan Switch/Chop Blank line,

2. A low-logic level on the Real Time Select line, or

3. A low-logic level on the $\overline{\text{Blank}}$ line.

When U630A is activated, its high-logic level output cuts off conduction in Q640, which causes the Z-Axis Amplifier to blank the memory display. Either of two conditions will activate U630A, as follows:

1. A high-logic level on the Real Time Select line, or

2. A low-logic level on the $\overline{\text{Blank}}$ line.

SINGLE SWEEP RESET GENERATOR

Transistor Q920 applies the SS Reset signal to pin B17 of the horizontal plug-in connector. Pin 2 of the camera connector (on the crt bezel) and the rear panel SS RESET INPUT connector are connected together so that grounding either point will cause Q920 to saturate briefly. The saturation time is about 1 ms as determined by C910 and R910. While saturated, Q920 conducts current into the time base via pin B17 of the horizontal plug-in connector. The current activates the single-sweep reset function in the time base.

SWEEP GATE OR SAMPLE PULSE SELECTOR

Connector J94 on the rear panel provides either the Sweep Gate or the Sample clock as selected by the position of jumper P940. The selected signal reaches J94 via Q960.

CHOP-ALTERNATE LOGIC

The circuitry made up of Q731, U630C, Q720, Q730, U630D, U720A, Q810, and Q811 generates the Chan Switch/Chop Blank signal. The logic circuitry has three modes of operation: Chop, Free-Run; Chop, Driven By The 5B25N; and Alternate Drive. Table 4-2 relates the types of vertical and horizontal plug-in units and their control settings to the settings of the 5223 mainframe and shows the resulting operating mode of the chop-alternate logic.

TABLE 4-2
Chop-Alternate Logic

Horizontal Compartment			Vertical Plug-In and Mainframe Conditions	Operating Mode
Plug-In	Time/Div	Chop/Alt		
5B25N	0.2 μs-50 μs	X		Chop, driven
5B25N	0.1 ms-5 s	Chop	Two vertical displays on.	Chop, driven
5B25N	0.1 ms-5 s	Chop	Either vertical set to dual-trace operation.	Chop, driven
5B25N	0.1 ms-5 s	X	Roll.	Chop, driven
5B25N	0.1 ms-5 s	Chop	Only one display on; no dual-trace; no roll.	Alternate
5B25N	0.1 ms-5 s	Alt	No roll.	Alternate
5B25N	Ampl	Chop	X	Chop, free-run
5B25N	Ampl	Alt	X	Alternate
not a 5B25N	X	Alt*	X	Alternate
not a 5B25N	X	Chop*	Neither vertical in dual-trace; not more than one vertical display being presented.	Alternate
not a 5B25N	X	Chop*	Two vertical displays on.	Chop, free-run
not a 5B25N	X	Chop*	One or both vertical plug-in units in dual-trace.	Chop, free-run

X means don't care
*** Except for the 5S14, any plug-in without a Chop/Alt control is internally wired to operate in Chop mode.**

Chop, Free-Run

Transistors Q720 and Q730 form an emitter-coupled astable multivibrator. This multivibrator generates the Chan Switch/Chop Blank signal when the 5B25N is in Ampl mode or when a time base other than a 5B25N is used and multiple traces are displayed. When the 5B25N is in Ampl mode, the Sweep Rate line will be at +5 V, which will turn Q731 off. The Chop Activate line will activate U630C, whose low-logic level output will permit the multivibrator to operate.

When the 5B25N is in Ampl mode (or another time base is in use) and U720A is in its cleared condition, the pin 6 output of U720A enables U630D. Flip-flop U720A stays in cleared condition because:

1. no Sample pulses occur,

2. the Chop Activate line prevents low levels from occurring (via Q810 and CR800) on U720A's set input, and,

3. U720A and Q811 form a one-shot multivibrator.

The emitter-coupled multivibrator operates at about 300 kHz, and U630D passes the signal from the multivibrator to the Chan Switch/Chop Blank line. The positive-going edge of the Chan Switch/Chop Blank signal causes the channel switching to change states; and the high-logic level causes the crt blanking to operate. Figure 4-7 shows the active paths and timing for chop, free-run operation.

Chop, Driven by the 5B25N

The 5B25N causes U630D to generate the Chop Blank part of the Chan Switch/Chop Blank signal when:

1. The 5B25N Time/Div control is not set to Ampl position and the 5B25N is in chop mode,

   a. Traces from both vertical plug-in units are displayed, and

   b. Either vertical plug-in unit has dual-trace mode selected, or

2. The Memory board forces chop mode.

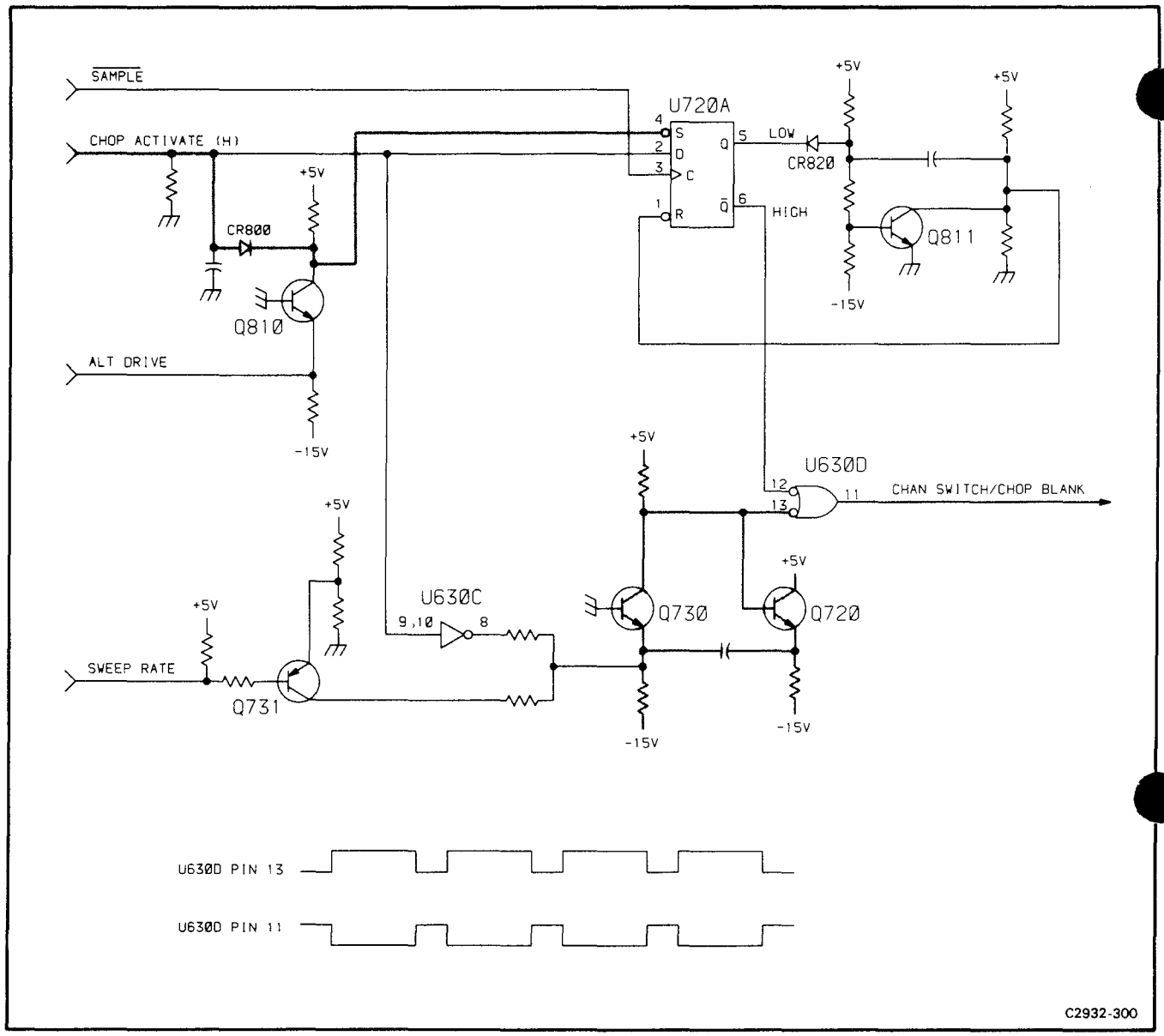


Figure 4-7. Active paths and timing in "chop, free-run" operation.

The Memory board forces chop mode if the 5B25N is in equivalent-time sampling mode (Time/Div from 50 μs to 0.2 μs/Div), or if the front-panel ROLL button and one or both DISPLAY buttons are pressed in.

When the 5B25N is operating as a time base the Sweep Rate line saturates Q731. The current in Q731 causes the voltage on R730 to reverse-bias Q730, which prevents the multivibrator from operating.

When the previously mentioned conditions exist, the Chop Blank pulses are synchronous with the Sample Pulse from the 5B25N. When the Chop Activate line is at a high-logic level, a positive-going transition on the Sample Pulse line clocks U720A, the input to the blanking timer.

Together, U720A, CR820, and Q811 form the blanking timer, which operates when the 5B25N is not in Ampl mode. When U720A pin 5 goes to a high-logic level it turns off CR820, which allows the bias network on Q811's base to turn it on. The voltage at Q811's collector goes toward ground from +4 V at a rate set by the RC combination of C820, R820, R821, and R822. When the collector voltage of Q811 reaches about +1 V, it clears U720A. Flip-flop U720A then changes states; its pin 5 output becomes a low-logic level that turns on CR82[illegible] and turns off Q811. While the pin 5 output of U720A wa[illegible]

a high-logic level, the pin 6 output was a low-logic level, of about 500 ns in duration, that caused U630D to produce the Chop Blank part of the Chan Switch/Chop Blank signal. Gate U630D is enabled by the high-logic level from the disabled chop multivibrator transistor, Q730. Figure 4-8 shows the active paths and timing in chop, driven by 5B25N operation.

Alternate Drive

When the time base is set to Alt mode, the Chop Activate line will be at a low-logic level and CR800 will be reverse-biased. Because CR800 is turned off, Q810 can function. Alt Drive pulses from the time base cause Q810 to produce negative-going pulses that set U720A so that its Q output is at a high-logic level. The blanking timer generates a negative-going pulse of about 500 ns duration which activates U630D to produce the Chop Blank part of the Chan Switch/Chop Blank signal. Gate U630D is enabled by the high-logic level from the disabled chop multivibrator transistor, Q730. Figure 4-9 shows the active paths and timing in alternate operation.

CHANNEL SWITCH LOGIC

The Channel Switch Logic circuitry is located on the top right of diagram 1, and consists of U610A, U610B, U710A, U710B, and U720B.

The channel switch for the vertical plug-in compartments consists of U610A and B. It changes state on the positive-going edge of the Chan Switch/Chop Blank pulse. Flip-flops U610A and B are connected as a ring counter. Together, the A and B sections of U610 generate two quadrature signals (they're separated by 90°) at a rate one-quarter of the channel-switch rate. The signals, called Left and Right Chan Sw Sig, connect to pins B21 of the left and right vertical plug-in connectors, respectively. Multi-trace plug-in units set to multi-trace modes use the Chan Sw Sig to drive their channel-switch circuits. The Q output of U720B connects, via gates U700A and D, to the vertical real-time channel switch, U410 on diagram 2; and the $\overline{Q}$ output connects to pin B21 of the horizontal plug-in compartment to provide sweep switching.

The Left and Right Chan Sw Signals also drive FF's U710A and B, the left and right sampled plug-in channel switch. The Hold signal from the Digitizer board clocks U710A and B. The positive-going edge of the Hold signal latches the channel-switch information into FF's U710A and B at the same time that the Digitizer board samples the analog signal from the plug-in units. The Memory board stores the output of the Digitizer. That is, the Digitizer stores the analog signal information and, if it is a multi-trace display, the two FF's (U710A and B) store the source identification information. This method matches the signal and its source in the Memory board.

VERTICAL CHANNEL SWITCH CONTROL

When two plug-in units are producing signals to be displayed, the mainframe time-shares their outputs by switching the vertical channel switch (U410, diagram 2).

The $\overline{\text{Right On}}$ and $\overline{\text{Left On}}$ lines from the plug-in compartments indicate whether a plug-in's output is being displayed. A -30 V level on a $\overline{\text{Right On}}$ or $\overline{\text{Left On}}$ line means that the Display button is pressed in on the corresponding plug-in unit. Gates U700A and D monitor the $\overline{\text{Right On}}$ and $\overline{\text{Left On}}$ lines.

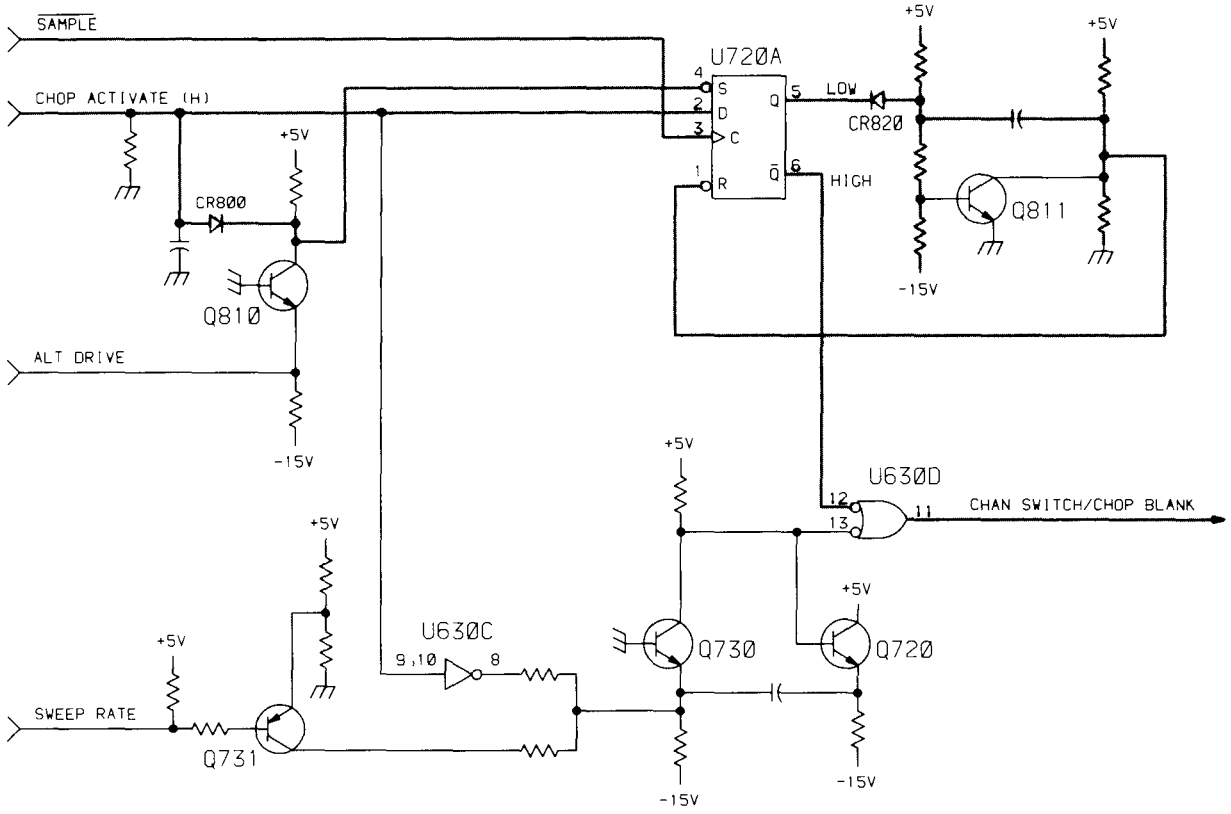
When only the left plug-in Display button is pressed in, the high-logic level on the $\overline{\text{Right On}}$ line disables U700D, which produces a low-logic level on the L-R Plugin Select line. This causes U410, the vertical channel switch, to connect the signal from the left plug-in to the vertical amplifier. This condition also exists when neither plug-in Display button is pressed in.

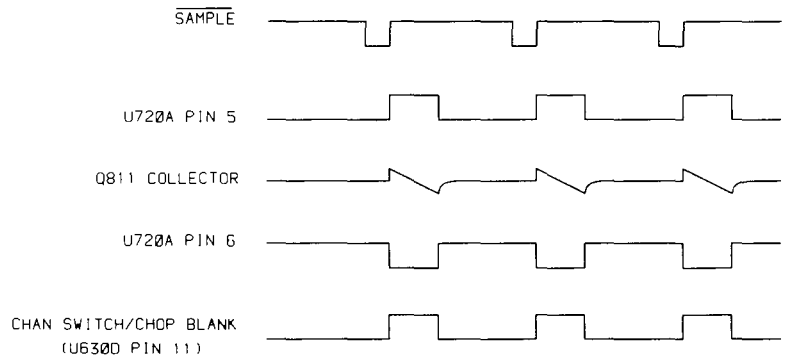
When only the right plug-in Display button is pressed in, the low-logic level on the $\overline{\text{Right On}}$ line reaches pin 12 of U700D. The high-logic level on the $\overline{\text{Left On}}$ line disables U700A, which produces a low-logic level that activates U700D to produce a high-logic level on the L-R Plugin Select line. The high-logic level on L-R Plugin Select causes U410 (diagram 2) to connect the signal from the right plug-in to the vertical amplifier.

When both plug-in unit's Display buttons are pressed in, the low-logic level on the $\overline{\text{Left On}}$ line will enable U700A and the low-logic level on the $\overline{\text{Right On}}$ line will enable U700D. When the $\overline{\text{Horiz Chan Sw Sig}}$ line is at a low-logic level it will activate U700A. When activated, U700A produces a high-logic level that disables U700D, which then asserts a low-logic level on the L-R Plugin Select line. This causes U410 to connect the signal from the left plug-in to the vertical amplifier. When the $\overline{\text{Horiz Chan Sw Sig}}$ line changes to a high-logic level it disables U700A, whose low-logic level output activates U700D to produce a high-logic level on the L-R Plugin Select line. This causes U410 to connect the signal from the right plug-in to the vertical amplifier. This switching sequence continues as determined by the Chan Switch/Chop Blank signal.

MULTI-CHANNEL PLUG-IN DETECTORS

Each vertical plug-in compartment has a Chop Sense line that indicates whether the plug-in is in a dual-trace mode. When a plug-in unit's dual-trace display is





C2932-301

Figure 4-8. Active paths and timing in "chop, driven by 5B25N" operation.

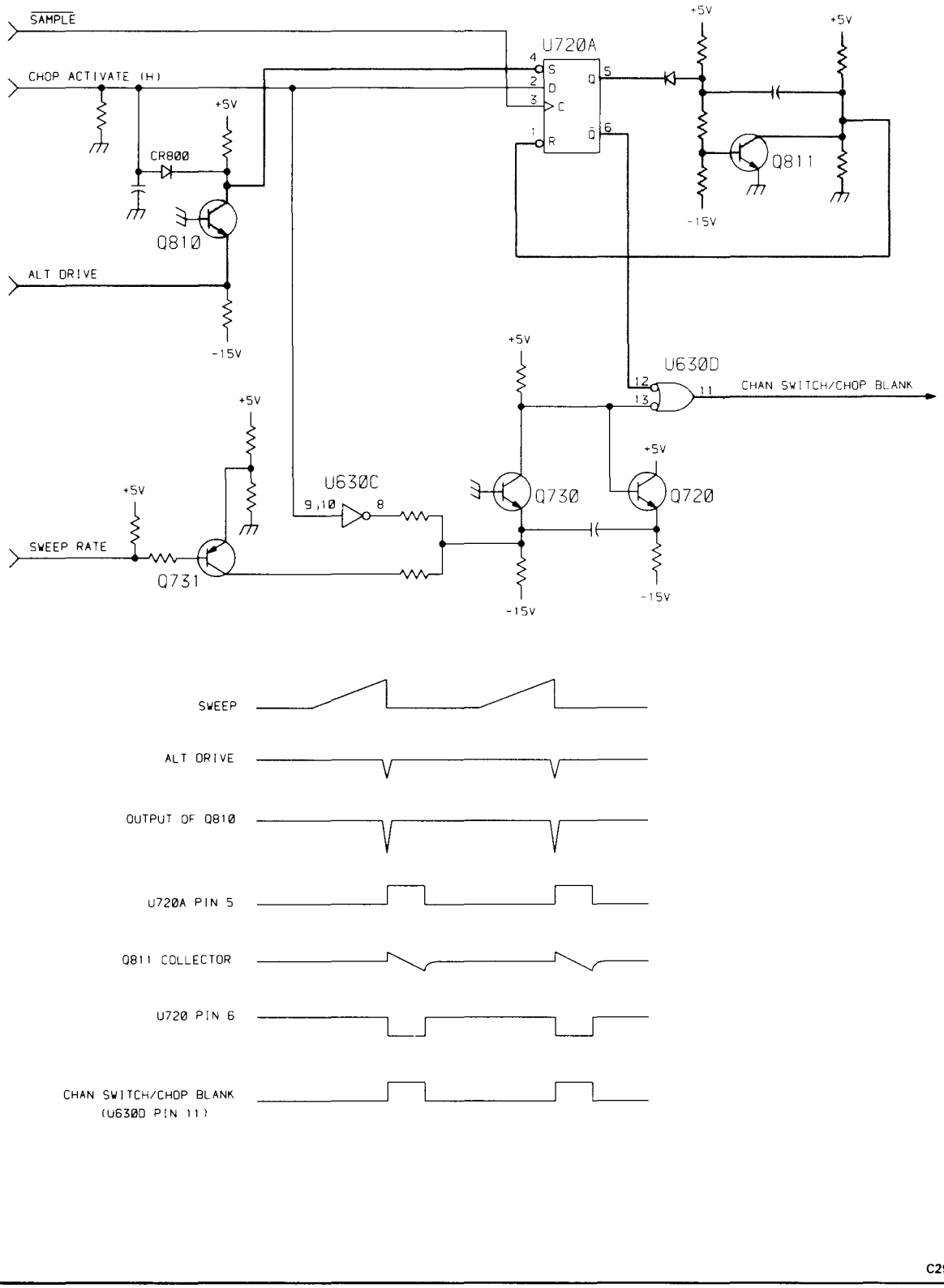


Figure 4-9. Active paths and timing in alternate operation.

selected, the Chop Sense line will be above +2.2 V. If the plug-in unit is in single-trace operation or if no plug-in is installed, the Chop Sense line will be at zero volts.

Comparators U130A and B compare the levels on the Chop Sense (L) and (R) lines with a +1.5 V reference. When the Chop Sense (L) line is at a low-logic level, U130A asserts a high-logic level on the L < 2 line. This means that the left plug-in unit is displaying fewer than two traces (for example, one). Conversely, a high-logic level on Chop Sense (L) causes U130A to apply a low-logic level to the L < 2 line, which means that the left plug-in unit is displaying two traces.

The right channel plug-in detector works similarly.

A low-logic level on the L < 2 or the R < 2 line will turn on Q600, which applies a high level to the Chop Sense line.

2 CHANNEL SWITCHING

Diagram 2 shows the part of the Interface Board's circuitry that is not shown on diagram 1. The Channel Switch selects the signal from the left or right plug-in compartment for display on the crt. The Vertical Signal Output Amplifiers provide samples of the signals from the left and right plug-in compartments to the PLUG-IN OUTPUT connectors (J91 and J92) on the rear panel.

CHANNEL SWITCH

Emitter-followers Q430, Q332, Q530, and Q431 provide a high impedance for the output of the vertical plug-in units and drive the channel switch, U410. Channel switch U410 connects one of the two vertical plug-in signals to pass to the display unit via the delay line. The L-R Plugin Select signal controls U410; a low-logic level on the L-R Plugin Select line causes U410 to connect the left channel to its output.

Resistors R321 and R516, in the emitter circuits of the Left and Right Input stages, establish the gain of the vertical amplifier part of U410. Those resistors connect to pins 1 and 16 (left) and pins 8 and 9 (right) of U410. The output of U410 from pins 12 and 13 goes to a shunt-feedback amplifier, Q300 and Q301, and Q400 and Q500. The shunt-feedback amplifier changes the dc level and amplitude of the vertical output signal to be compatible with the input requirement of the Vertical Amplifier. The shunt-feedback amp also has the low output impedance that the delay line requires for proper drive, and transient-response compensation.

When a dual time base is in use, the time base furnishes trace-separation information (a square wave whose amplitude is proportional to the desired trace separation) to pin B16 of the horizontal plug-in connector (diagram 1). The Trace Separation signal enters the vertical display through Q410.

LEFT AND RIGHT SIGNAL OUTPUT AMP

The Vertical Signal Output Amplifiers are differential to single-ended converters that have impedance reduction and gain. These amplifiers apply the signals from the left and right vertical plug-in compartments to the Plug-In Output connectors on the rear panel (J92, RIGHT VERT; and J91, LEFT VERT). Because the left and right amplifiers operate identically, only the left one is described here. The signals from the emitters of U410 connect to differential amplifier Q330 and Q331. The output current of Q330 drives shunt feedback amplifier Q240. The output current of Q331 flows through common-base stage Q231, generating a voltage drop across R240. The voltage on R240 and the voltage developed at the output of Q231 are additive, that is, in phase. This output voltage drives emitter-follower Q140. The RC network in the output lead is for transient-response compensation.

3 VERTICAL AMPLIFIER

The Vertical Amplifier receives inputs from the vertical plug-in units via the Interface, and from the vertical section of the Memory via the Switch board. Diagram 3 shows the Vertical Amplifier.

The Vertical Amplifier drives the vertical deflection plates of the crt. Depending on the state of the Real Time Select control line, the output of the Vertical Amplifier will come from the vertical plug-in(s) or from the vertical section of the memory.

Another amplifier supplies an integrated (smoothed) version of the memory display, for a chart recorder or other slow-responding instrument, to the MEMORY DISPLAY OUTPUT (Y) connector (J98) on the rear panel.

VERTICAL DISPLAY CHANNEL

The real-time signal comes from the Interface to the vertical channel switch, U330, via R432 and R433. Potentiometer R336 (RT Gain) and R434 determine the gain of the real-time channel. Transistor Q335 and its associated parts form a constant-current source for the real-time section of U330. The constant-current source minimizes the common-mode signal at the output of th

Vertical Amplifier. Adjustments C336, C439, R437 and R438 optimize the transient response of the real-time section of channel switch U330.

The memory signal, which comes from the Switch Board in the form of differential currents, develops differential voltages on R526 and R527. These differential voltages reach the input of the memory section of U330 via R425 and R426.

The Real Time Select line controls channel switch U330. A high-logic level on the Real Time Select line selects the real-time output.

With no signals applied to the Vertical Amplifier, the current through feedback resistors R124 and R230 determines the voltage at pin 13 of U230 (the upper vertical deflection plate voltage). That current is the sum of the current in R330 and U330's pin 12 output. U330's pin 12 current is half the sum of the currents in R324, R325 and R335, which is about 12 mA. The current through R330 is set by the Vert CM (common mode) adjustment,R225, via Q225. This current determines the voltage at the crt's upper deflection plate. Adjusting R225 will also vary the voltage at the lower deflection plate a similar amount, and in the same direction, by changing the current in R333. The vertical amplifier is relatively sensitive to the common-mode output voltage, and an incorrect adjustment of R225 can cause a number of seemingly unrelated symptoms. Refer to Section 6, Calibration, for information on how to set the Vert CM adjustment correctly.

The Vert Cent potentiometer, R326, varies the ratio of currents in R330 and R333, which causes a differential change in deflection plate voltages.

The common-mode input voltage at U330 pins 10, 7, 2 and 15 is about +9 V because of current drawn by circuitry on the inputs.

Resistors R124-R230 and R131-R231 are the feedback elements for U230. Adjustment C230 optimizes the transient response of the output amplifier. Transistor Q130 operates with active devices in U230 to decrease U230's supply voltage if the deflection plate leads accidentally contact ground.

MEMORY DISPLAY OUTPUT AMPLIFIER

Operational amplifier U811 and its related parts form a variable-rate integrator that furnishes a smoothed version of the memory signal to J98, the MEMORY DISPLAY OUTPUT (Y) connector. When the OUTPUT SAVED DISPLAY(S) button is pressed, circuitry on the Memory board causes a low-logic level on the ANALOG OUTPUT OFF line for the duration of the output cycle. This turns on Q810, which causes a high-logic level on the Signal line. The high-logic level on the Signal line causes the four switches in U810 to close—switches U810C and U810D connect U811 to the memory output from the Switch board. Potentiometer R47A varies the charge rate of the integrator to suit the external device receiving the signal.

BEAMFINDER

When the BEAMFINDER button is pressed, CR223 and R216 divert current from Q225. This causes output amplifier U230 to conduct more current and raise the common-mode voltage. The greater common-mode voltage reduces the dynamic range of amplifier U230. This ensures that the display will be on-screen regardless of the amplitude of the input signal.

4 HORIZONTAL AMPLIFIER

The Horizontal Amplifier receives inputs from the horizontal plug-in, via the Interface, and from the horizontal section of the Memory via the Switch Board. Diagram 4 shows the Horizontal Amplifier.

The Horizontal Amplifier drives the horizontal deflection plates of the crt. Depending on the state of the RT Select control line, the input of the Horizontal Amplifier will come from the horizontal plug-in (real-time) or from the horizontal section of the memory.

A separate amplifier provides a sample of the horizontal plug-in signal to the HORIZ PLUG-IN OUTPUT connector (J93) on the rear panel.

A third amplifier supplies an integrated (smoothed) version of the memory display for a chart recorder or other slow-responding instrument.

HORIZONTAL DISPLAY CHANNEL

The Horizontal Amplifier is identical to the Vertical Amplifier except as follows:

1. The common-mode voltages at the inputs (P7) are about −0.6 V instead of +9 V as in the Vertical.

2. Level-shifters Q306 and Q307 accommodate the different common-mode voltage.

3. Diodes CR200 and CR201 limit signal excursions. In the Vertical Amplifier, channel switch U330 performs the limiting.

4. To accommodate the difference in the crt's horizontal and vertical deflection sensitivities, the transconductance of channel-switch U400 is 20% lower than its counterpart in the Vertical Amplifier, U330. This makes the Horizontal Amplifier more sensitive.

5. A high-logic level at U400 pin 4 selects the real-time display, rather than a low-logic level as with U330 in the Vertical Amplifier.

The Horizontal Amplifier is sensitive to the common-mode output voltage, and an incorrect adjustment of R317 (Horiz CM) can cause a number of seemingly unrelated symptoms. Refer to Section 6, Calibration, for information about how to set the Horizontal CM adjustment correctly.

When the BEAMFINDER control is pushed in, CR314 and R215 divert current from Q316. This causes output amplifier U200 to conduct more current and raise the common-mode output voltage. The greater common-mode output voltage reduces the dynamic range of amplifier U200, and ensures that the display will be on-screen regardless of the amplitude of the input signal.

MEMORY DISPLAY OUTPUT AMPLIFIER

Operational amplifier U820 and its related parts forms a variable-rate integrator that furnishes a smoothed version of the memory signal to J97, the MEMORY DISPLAY OUTPUT (X) connector. When the OUTPUT SAVED DISPLAY(S) button is pressed, the circuitry on the Memory board causes a low-logic level on the ANALOG OUTPUT OFF line on the Vertical Amplifier, diagram 3, for the duration of the output cycle. This turns on Q810, which causes a high-logic level on the Signal line. The high-logic level on Signal causes the four switches in U810 to close—switches U810A and U810B connect U820 to the memory output from the Switch Board. Potentiometer R47B varies the charge rate of the integrator to suit the external device receiving the signal.

HORIZONTAL SIGNAL OUTPUT AMPLIFIER

Transistors Q500, Q501, Q502, Q503, and Q510 form a differential to single-ended converter for the HORIZ PLUG-IN OUTPUT signal. The output sensitivity is 50 mV/division of deflection on the crt. Because the horizontal dimension of the crt is 10 divisions, the signal at J93 need vary only + and − 250 mV to contain 10 divisions worth of information, i.e., a full display. Diodes CR510 and CR511 protect Q510 against high voltages from external equipment connected to J93.

5
Z-AXIS AMPLIFIER AND FRONT PANEL

Z-AXIS AMPLIFIER

The Z-Axis Amplifier is a current-driven operational amplifier that controls the intensity of the crt display via the control-grid supply. Diagram 5 shows the Z-Axis Amplifier, which consists of Q700, Q702, Q703 and related parts. Transistors Q702 and Q703 form a collector-coupled complementary amplifier; their collectors are the output. The output voltage is fed back to the summing node of the amplifier via R705.

The Z-Axis Amplifier has three inputs: (1) the output of the Interface Board (which responds to the Intensify and Z-Axis inputs from the horizontal plug-in compartment, and the front-panel real-time INTENSITY and MEM INTEN controls), (2) the external Z AXIS INPUT connector, and (3) the BEAMFINDER. These inputs reach the input of the Z-Axis Amplifier, the base of Q700, via a diode gate (CR605, CR704, CR606, and CR700). The inputs are current-sensitive; more current causes a brighter display.

Principles of Operation

The input circuit consists of:

1. Active devices Q600, Q603, Q610 and Q701,

2. Five current sources, as follows:

Q600 and Q603	≈2.3 mA
R611	≈0.2 mA
R605, Q701 & R702	≈0.2 mA
R700	≈1.9 to 2.1 mA
R606, CR620	≈2.5 mA (only when the BEAMFINDER button is pressed)

Figure 4-10 shows the diode current-switching gate and the current sources.

3. Diode current-switching gate CR605, CR606, CR700 and CR704.

The diode current-switching gate limits the range of currents into the summing node to between ≈0.2 mA and ≈2.0 mA. Because the amplifier's output current flows through feedback resistor R705, this range of input currents sets the range of output voltages to between ≈+10 and ≈+62 V.

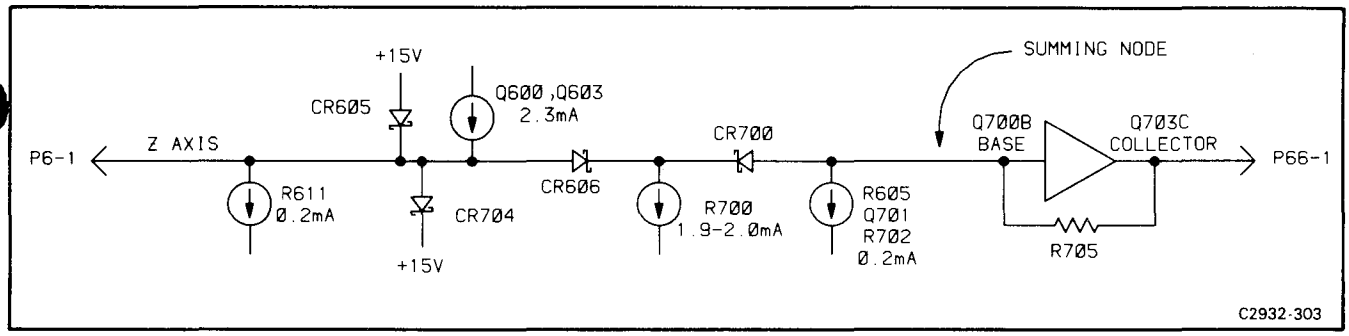


Figure 4-10. Current sources and diode current-switching gate in Z-Axis Amplifier.

Input from Interface Board

When no current flows in the Z Axis line (P6 pin 1), diode CR606 and CR704 conduct; CR605 and CR700 are off. Because CR700 is off the current in the summing node is 0.2 mA, which sets the output voltage to about +10 V. This is the blanked condition.

When between 0.1 mA and 2.1 mA flow in the Z Axis line (P6 pin 1), diodes CR606 and CR700 conduct; CR605 and CR704 are off. Because Q610 and Q701 have current gains of nearly unity, the current in the summing node is practically the same as the Z Axis input current. The output voltage increases with input current, to a maximum of about +62 V with a 2.1 mA input current.

When more than 2.1 mA flows in the Z-Axis input (P6 pin 1), diodes CR605 and CR700 conduct; CR606 and CR704 are turned off. Because CR606 is turned off, the current at the summing node is limited to the 2.1 mA total drawn by R700 and the R605, Q701, R702 current source. Diode CR605 conducts the extra input current.

Input from External Z AXIS INPUT Connector (J96)

With no external signal applied, Q600 sets the base voltage of Q603 at about +24.3 V, which puts about 5 V across emitter resistor R604. This establishes the quiescent current of ≈2.3 mA in the collector of Q603. Because the voltage gain from J96 to the base of Q603 is about unity, and because the transconductance of Q603 to a voltage input is about 0.5 mA/Volt, an input that ranges from zero to -4.2 V will cause Q603's output current to increase 2.1 mA (from 2.3 to 4.4 mA). This current change will affect the output voltage the same as a reduction in input current from the Interface Board. The opposite effect will occur if a positive voltage is applied to J96.

Input from BEAMFINDER

When the BEAMFINDER button is pressed, a current of about 2.5 mA flows in CR620 and R606. Because this current exceeds the maximum-intensity current of 2.1 mA, the output of the Z-Axis Amplifier is +62 V.

CALIBRATOR

Transistors Q111, Q112 and related parts form an emitter-coupled multivibrator. The multivibrator operates at 1 kHz and produces a 300 mV square wave (100 mV into 50 Ω). Potentiometer R204, Freq Trim, adjusts the operating frequency.

GRATICULE ILLUMINATOR

Transistors Q210, Q310 and GRAT ILLUM control R200 permit the operator to vary the voltage on the graticule lamps from zero to -15 V.

6
CRT CIRCUIT

The CRT Circuit provides high voltages to operate the crt. The crt requires -2960 V for its cathode, a negative voltage of about -3040 V for the control grid, +12,000 V for the anode, 6.3 V ac for the filament, and about -2100 V for the focus electrode.

To generate these potentials, the CRT Circuit has:

1. an oscillator,

2. a regulator that controls the oscillator,

3. a half-wave rectifier that furnishes -2960 V,

4. a voltage-quadrupler that furnishes +12,000 V,

5. a control-grid bias circuit,

6. a 6.3 V ac source, that can be elevated to -2960 V, for the crt filament, and

7. control circuits that permit adjustments to the focus, astigmatism, geometry, and trace rotation of the display.

OSCILLATOR

Transistor Q62 and transformer T120 form the high-voltage oscillator.

The oscillator operates between 35 and 45 kHz at an amplitude governed by the regulator (Q300, Q400, Q401 and associated parts). The regulator senses the -2960 V output and controls the amplitude of oscillation by varying the base current to the oscillator transistor.

When power is applied to the oscilloscope the -2960 V line is at zero volts. Via R202 and R220A, the +86 V forward-biases Q401, whose output turns on Q400. The output of Q400 turns on Q300 which furnishes maximum current to the base of oscillator transistor Q62 via the base feedback winding of T120. At this point Q62 will conduct, beginning oscillation, which occurs as follows:

Its collector current will cause a corresponding current increase in the base-feedback winding that drives its own base. When the voltage at pin 2 of T120 stops increasing, the magnetic field around T120 starts collapsing, inducing currents in the base-feedback windings which will turn Q62 off, while the collapsing field drives the collector voltage to a higher value. The current changes in the collector of Q62 drive the primary winding of T120, and T120's secondary winding furnishes high-voltage ac to the -2960 V half-wave rectifier and the +12,000 V voltage quadrupler.

Transistor Q60 acts as a voltage limiter for the oscillator's supply voltage. It ensures that the supply voltage will not go more positive than about +19.3 V under all input voltage conditions. Zener diode VR800, on the XYZ Board (diagram 5), sets Q60's base voltage to +20 V. Transistor Q60's collector is connected to the unregulated +20V. When Q60's collector is more positive than +20 V, Q60 operates as an emitter-follower and supplies about +19.3 V to transformer T120 via L222. If the +20 V Unreg falls below +20 V, Q60's collector-base junction will become forward-biased and the emitter voltage will vary with the +20 V Unreg.

REGULATOR

A sample of the -2960 V reaches the regulator via R220B. Transistors Q401 and Q400 form an error amplifier which senses changes in the -2960 V output voltage.

If the -2960 V voltage goes positive, part of the positive-going change reaches the base of Q401 via R220B. The positive-going voltage forward-biases Q401, whose output turns on Q400. Q400's output causes Q300 to increase the current to the base of oscillator transistor Q62, which will respond by producing greater collector current to T120. The secondary voltage of T120 increases and the -2960 V output becomes more negative.

A negative-going change on the -2960 V line will be regulated in the opposite fashion to that just described.

-2960 V SUPPLY

Diode CR120 forms a half-wave rectifier. Components C120, R120, C110, and R110 filter the rectified output to provide -2960 V. The -2960 V serves as the negative accelerating potential for the crt cathode.

+12,000 V SUPPLY

Hybrid circuit U220 rectifies its ac input from T120 and multiplies it to +12,000 V. Because the +12,000 V and the -2960 V both originate from the same ac source, regulating the -2960 V also regulates the +12,000 V.

The +12,000 V serves as the accelerating potential for the crt anode.

CONTROL-GRID BIAS CIRCUIT

Diodes CR101, CR102, CR103, CR210, and VR210 provide the negative voltage for the crt control grid. The Intensity Preset adjustment, R411, sets the output level of this supply. About 300 V, p-p, from the secondary of T120 reaches the Control-Grid Bias Circuit via C211 and R211. Diodes CR101 and CR210 clip the ac signal to determine the operating level at the control grid. CR103 limits the negative excursion of the signal. Quiescently, when the crt is blanked by signals from the Z-Axis Amplifier, the anode of CR101 is set at about 10 V by the Z-Axis Amplifier. Intensity Preset adjustment R411 sets the positive clipping level at the cathode of CR210 to bias the control grid of the crt just negative enough to blank the trace when the Z-Axis Amplifier is at +20 V. The quiescent level of the Z-Axis output signal (at P66 pin 1) is about +10 V, which is about 10 V below crt cutoff. In this state, the grid is 65-70 V more negative than the cathode.

The negative voltage at the crt cathode (-2960 V) is connected, via R104, to the cathode of CR102. The clipped voltage developed by diodes CR101 and CR210 is peak-to-peak rectified by diodes CR102 and CR103 and

superimposed on this negative voltage to result in a level at the grid that is more negative than the crt cathode. The unblanking gate from the Z-Axis Amplifier reaches the anode of CR101 via R105. The fast-rising and -falling parts of this signal are coupled directly to the control grid via C100. The unblanking gate further clips the negative excursions, thereby reducing the voltage difference between grid and cathode of the crt. This allows the cathode current of the crt to pass to the anode to present a display.

CRT CONTROL CIRCUITRY

The FOCUS control, R300, determines the focus of the crt display. The network of CR110, CR111, CR112, CR200, and VR101 provide a negative voltage for the crt's focus grid. About 300 V p-p from the secondary winding of T120 reaches the focus-grid supply via C210 and R210. The setting of the Focus control determines the negative clipping level at the cathode of CR200, which in conjunction with the Focus Preset control, governs the operating level of the focus grid. Under normal operating conditions the voltage at the focus grid is more positive than the control grid or the cathode of the crt.

The Trace Rot adjustment, R220, provides a means of adjusting current in trace-rotation coil L51 so that the trace aligns with the horizontal graticule lines.

The Geom and Astig adjustments, R901 and R900, provide voltages to the horizontal-deflection-plate shield and grid #5. These voltages provide a well-defined display.

7 LV POWER SUPPLY

The Low-Voltage Power Supply provides operating power for the entire oscilloscope. Electronic regulation produces stable, low-ripple output voltages.

The main power input from the power line reaches the primary of transformer T25 via the Fuse, Line Filter, POWER switch, thermal cutout, and Line-Voltage Selector. The Line-Voltage Selector has a circuit board which may be inserted in four different ways to accommodate nominal line voltages of 100, 120, 220, and 240 volts. The operating voltage ranges for each of these settings, the current consumptions, and the correct value for the main fuse are marked on the rear panel of the instrument. The primary voltage connections from the power-inlet module also have connections for fan power. Because the fan is connected across one of the primary transformer windings it always receives a nominal 120 volts, whether or not the 5223 is set and connected for another line voltage. Autotransformer action of the primary circuit of the transformer accomplishes this regulation.

The secondary windings, their full-wave bridge rectifiers and filter capacitors provide filtered, unregulated dc voltages.

-30 V REGULATOR

The -30 V Regulator provides power for various parts of the 5223 and serves as the reference voltage for the -15 and +30 V regulators. The -30 V regulator is a feedback-amplifier system which operates between ground and the unregulated -38 V. Output current from the -30 V supply reaches the load via series-pass transistor Q120. The output voltage of the regulator is set by the voltage at the wiper of -30 V adjustment R521. Transistor Q421 compares the voltage from R521 with the voltage at the anode of VR430. The feedback path is through Q421, Q420 and Q320 to the base of the two driver transistors, Q230-Q231, and to the base of series-pass transistor Q120. Any variation in output voltage reaches the base of Q421 and is nullified by a change in Q120's conduction, thus maintaining a steady output. Transistor Q121 and sensing resistor R224 limit the current through Q120 when the voltage drop across R224 exceeds about 0.6 V. This protects the regulator from excessive power dissipation when a short circuit or other problem exists. Components R120, VR230, and R222 provide fold-back current limiting, which reduces the maximum current the supply will deliver as the difference between the unregulated voltage and the output voltage increases.

-15 V REGULATOR

The -15 V regulator consists of series-pass transistor Q1200 and error-sensing transistors Q1000 and Q1001. Transistor Q1200 delivers current to the load. The regulator establishes the output voltage by comparing its output voltage with the reference voltage at the base of Q1000. Differences between voltages at the bases of Q1000 and 1001 cause a change in Q1001's collector current. The resulting voltage change is applied to the base of Q910, whose output changes the conduction of Q1200 to correct for any output error. If the output gets short circuited, Q1100 limits the current through Q1200. During normal operation Q1100 does not conduct. The -15 V regulator also has fold-back current-limiting, implemented by CR1100, R1101, and R1203, and conventional current-limiting implemented by R1202 and Q1100.

+15 V REGULATOR

The +15 V regulator consists of error-sensing transistors Q810 and Q811, error amplifier Q710, and series-pass transistor Q600. This regulator operates like the -15 V regulator.

+30 V REGULATOR

The +30 V regulator furnishes power for the instrument and serves as reference voltage for the +86, +15 and +5 V regulators. The regulator consists of error-sensing transistor Q411, error amplifier Q410-Q400, and series-pass transistor Q500. The feedback amplifier system is similar to the one described for the -30 V supply. The +30 adjustment R522 permits the output voltage to be set to exactly +30 V. Components Q300, R302, R301, R300 and VR400 provide fold-back current limiting. The voltage across R302 turns limiting-transistor Q300 on when the output current exceeds about 500 mA.

+86 V REGULATOR

Error amplifier Q1020-Q1120 compares the +30 V reference with the voltage at the base of Q1020. Voltage divider R1120-R1013 senses the +86 V; its output drives the base of Q1020. The output current of Q1120 drives Q1220, the input device of Darlington stage Q1220-Q1320. Components R1211 and Q1210 provide short-circuit protection.

+5 V REGULATOR

The regulator for the +5 V supply achieves its regulation by switching its series-pass transistors between "on" and "off" states rather than by continuously varying their conduction. Because of this it is known as a switching regulator. The regulator consists of:

1. switching circuitry,
2. voltage-regulating circuitry,
3. a triangle generator,
4. current-limiting circuitry, and
5. over-voltage protection.

Figure 4-11 is a simplified block diagram of the +5 V regulating circuit.

The switching circuit connects current from the +25 V source to the output and to storage capacitor C503. The triangle generator and voltage regulator set the rate and duty factor, respectively, of the switching action. The voltage regulator senses the ripple on the output and the dc level at the A9 Interface board, and automatically adjusts the duty factor of the switching circuit to establish the correct output voltage. The current-limiting circuit senses the output current and, if it exceeds about

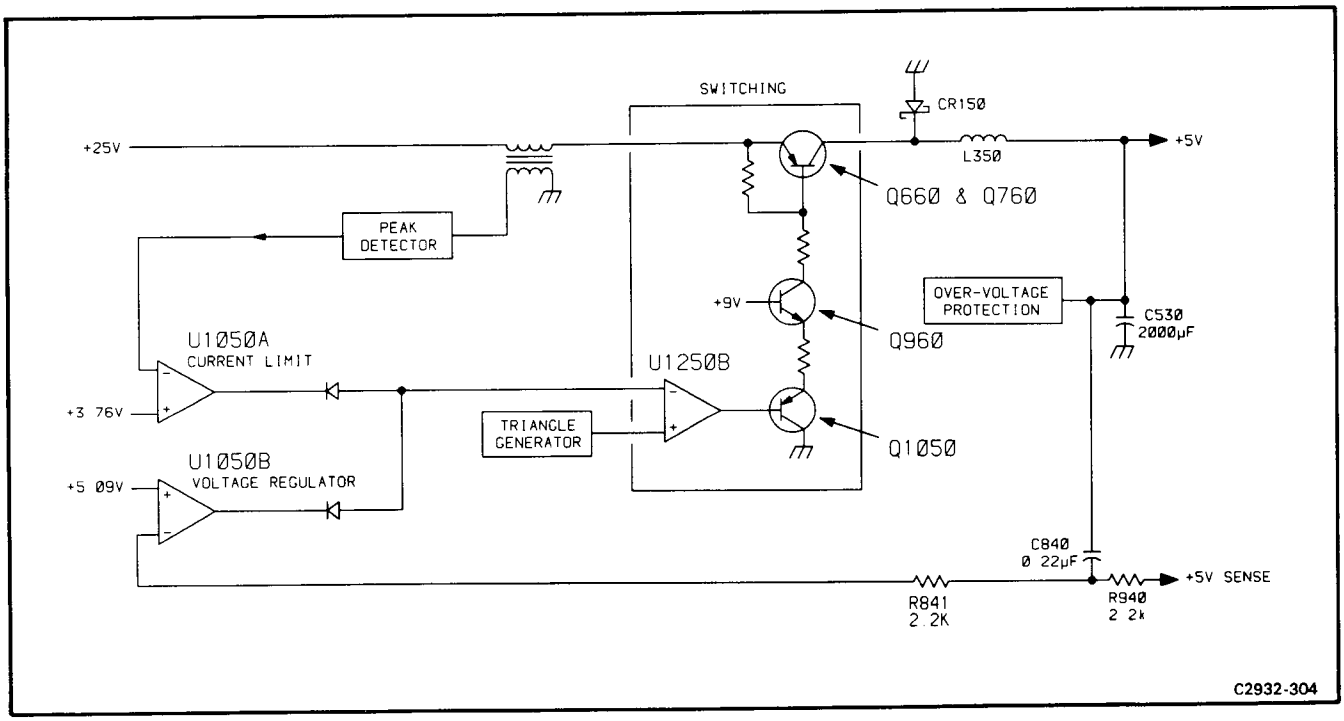


Figure 4-11. Simplified block diagram of +5 V switching regulator.

8.5 amperes, reduces the duty factor of the switching circuit to decrease the output voltage. The overvoltage protection circuit senses the actual output voltage and, if the output exceeds +6.2 V, shuts off the regulator and shorts the output line to ground.

The outputs of the voltage regulator, U1050B, and the current regulator, U1050A, connect to the input of switching comparator U1250B via diode gate CR1050-CR1150. The gate ensures that only one of the regulators is connected to the switching comparator at any time. The regulator whose output voltage is lower will be connected to U1250B.

The switching circuitry consists of comparator U1250B, driver stage Q1050 and Q960, and switching transistors Q660 and Q760. In normal operation, comparator U1250B receives a 25 kHz triangle wave on its + input and a dc level from U1050B on its minus input. (In current-limit operation, the dc level from U1050A serves as the reference level for comparator U1250B.) The amplitude of the triangle wave is about 2.2 V on a dc level of about 4.5 V (its valley is 3.4 V and its peak is 5.6 V). U1250B produces a square wave in response to these inputs. Each time the triangle wave crosses the voltage level at U1250's minus input (the output of U1050B), U1250B switches. The dc level from U1050B determines the voltage where U1250B will switch—so the dc output of U1050B governs the duty factor of U1250B's square-wave output. Emitter follower Q1050 provides a high impedance for U1250B to drive, and with common-base stage Q960 and R1050-R1060, provides the current needed to drive Q660 and Q760.

When Q660 and Q760 conduct they furnish current to the load via L350. When Q660 and Q760 are turned off, L350 maintains current flow via "catch diode" CR150. Figure 4-12 is a simplified diagram that shows current paths in open- and closed-switch conditions.

When they switch, Q660 and Q760 generate transients that could damage them. To protect Q660 and Q760 from

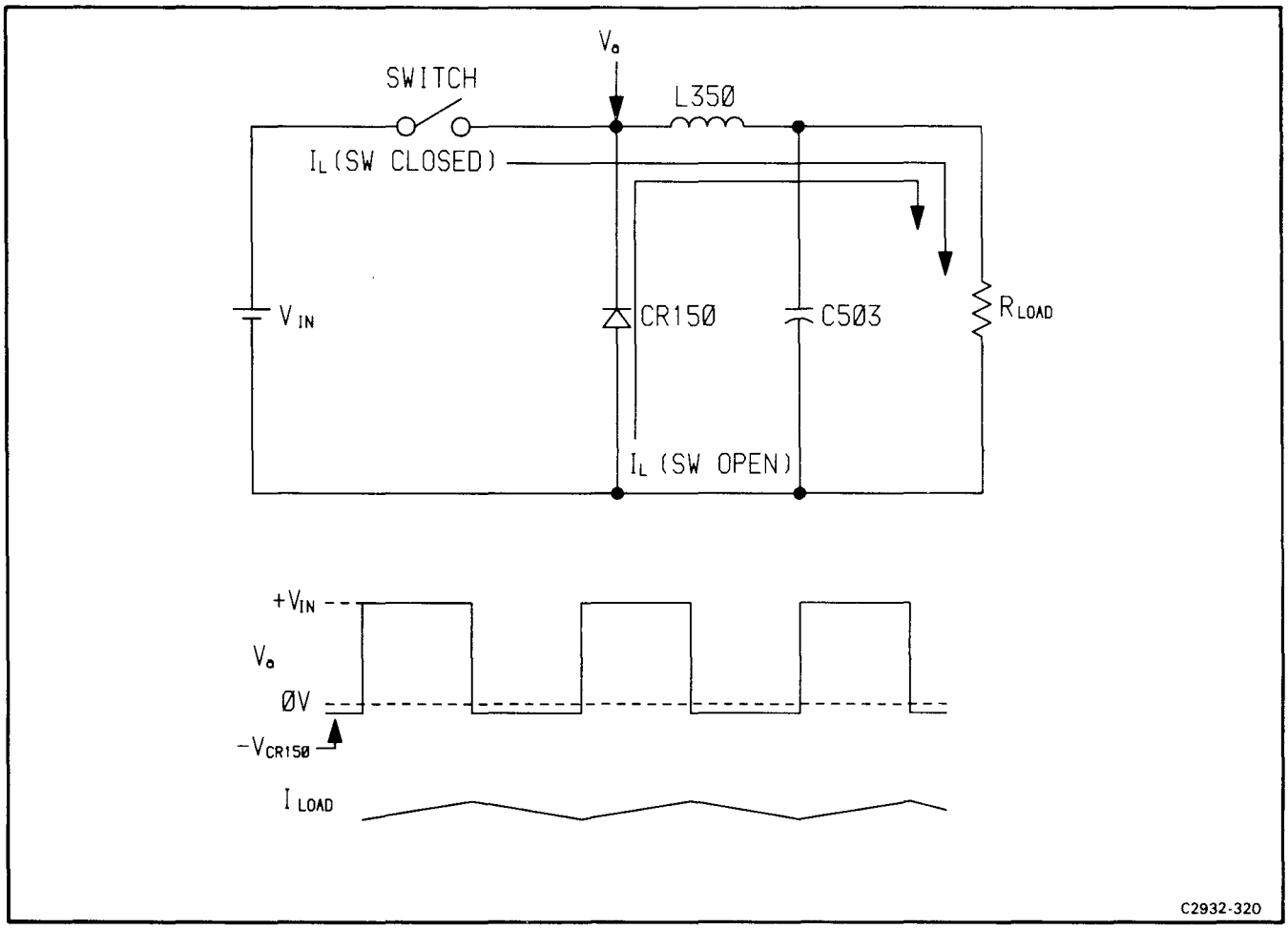


Figure 4-12. Current paths through the switching and regulating components in open- and closed-switch conditions.

these transients, we have circuits that minimize the effects of the transients. Saturable reactor L651, CR560, and R560 protect Q660 and Q760 during turn-on. Diode CR650, L650, R340, and C140 protect Q660 and Q760 during turn-off.

Three LC filters, L830-C1140, L1040-C1130, and L1140-C1230 reduce ripple on the output voltage.

Amplifier U1050B receives two inputs. One input is the sum of the ripple voltage from storage capacitor C503 and the output dc level, and the other is a reference voltage of +5.09 V. When the +5 V output voltage is less than its nominal value, the output of U1050B provides a more-positive reference voltage to the input of switching comparator U1250B. The higher reference causes U1250B to change the duty factor of its output to have a longer negative part than before. Because the negative part of U1250B's output controls the on-time of switching transistors Q660 and Q760, they conduct for a longer part of the switching cycle. The output voltage then rises to its proper value. The reverse of this sequence takes place if the +5 V output is above its nominal value; U1050B produces a less-positive reference for switching comparator U1250B, which then changes the duty factor of its output to have a shorter negative period than before. Because the negative part of U1250B's output controls the on-time of switching transistors Q660 and Q760, they conduct for a shorter part of the switching cycle. The output voltage returns to its proper value.

Comparator U1250A and its related parts form a triangle-wave generator that produces a 25 kHz, 2.2 V triangle wave. The triangle wave drives switching comparator U1250B.

Transformer T540, amplifier U1050A and related parts form the current-limiting circuit. T540 senses the current flowing in the switching transistors. Diode CR740 and C841 form a peak detector. When the output of the peak detector exceeds about +3.75 V, CR740 conducts and charges C841. The minus input of U1050A senses this more-positive voltage and applies a more-negative voltage to the input of U1250B via CR1050. The more-negative reference causes U1250B to shorten the negative part of its output signal. Because the negative part of U1250B's output establishes the on-time of switching transistors Q660 and Q760, they conduct for a shorter part of the switching cycle. This reduces the output voltage.

Transistor Q1350 and controlled-rectifiers Q1341 and Q1340 form an over-voltage protection circuit. Zener diode VR951 sets Q1350's base voltage at about +5.6 V. If the +5 V output voltage rises above about +6.2 V it will turn Q1350 on. The output of Q1350 will turn Q1341 on, and Q1341's output will turn on Q1340. When Q1341 is turned on, it grounds the +9 V line via R1340 and Q1340. The absence of +9 V then shuts off the triangle generator, the current-limit comparator, the switching comparator, and the switch-drive transistor Q960. Any failure in the regulator itself could cause the output to rise above +5 V. The failures that do not affect Q660 and Q760 can be protected against by the action of Q1341, which effectively shuts off switching transistors Q660 and Q760. However, if the failure is a short circuit in Q660, Q760, Q960 or Q1050, or related parts, there is no control of the output and the +25 V will be connected directly to the +5 V output. In this situation, Q1340 clamps the +5 V output to ground and F340 blows to protect the load circuitry.

UNREGULATED VOLTAGES

There are five unregulated voltages, +200 V, +38 V, +20 V, -20 V, and -38 V. The +200 V reaches the Interface Board via fuse F930, and the +20 V reaches the crt circuit via fuse F620.

LINE TRIGGER SOURCE

The trigger circuits in time bases need an ac signal for their line trigger function. Components R311, C210, R310, and R820 filter and attenuate the ac signal from lead 7 of T25. The output, called Line Trig, goes to the Interface Board so time bases can use it.

8
DIGITIZER SAMPLER

In order to make an accurate conversion, the Digitizer A/D Converter requires a constant voltage at its input. The Digitizer Sampler (DS) samples the signal from the plug-in unit and presents a constant-voltage sample to the Digitizer A/D Converter (diagram 9). The DS consists of a Sample-Hold circuit, a Transconductance Amplifier, a Channel Switch, the Sample-Gate Drivers and Control Logic.

SAMPLE-HOLD

The Sample-Hold (S-H) circuit connects the left and right input signals to capacitors which "hold" those voltages for the Digitizer A/D Converter (diagram 9). Each S-H circuit consists of two diode bridges for the differential input signal, two differential current switches for each diode bridge, clamp diodes, transient response compensation, and two storage capacitors. Because the plus and minus sides of the left and right channels

operate similarly, only the plus side of the right channel will be described here.

Differential current switches Q370, Q371, Q372 and Q373 control diode bridge U460. When Q370 and Q373 are turned on, they conduct current through the four diodes of U460 (Q371 and Q372 are reverse-biased). The conducting bridge connects the input signal from emitter-follower Q470 to storage capacitor C461. This is the "sample" state. When Q371 and Q372 are turned on and Q370 and Q373 are reverse-biased, Q371 and Q372 conduct current through CR471, R471, ground, R470, and CR470. This current develops about -1 V at the anodes of U460 (pins 1 and 12) and about +1 V at the cathodes of U460 (pins 6 and 7), which reverse-biases U460's diodes. This is the "hold" condition—C461 maintains its charge because of the high impedance of reverse-biased U460 and Q460A in the next stage. Figure 4-13 shows the current paths in the + side of the right channel for the sample and hold conditions. The - side of the right channel, and the left channel, works the same. The diode in U460 whose cathode connects to U460 pins 8 and 11 prevents that point from going more than one diode voltage drop (about 0.6 V) below ground. Schottky diodes CR570 and CR472 keep the + and - input voltges from going more than one diode voltage drop from each other.

SAMPLE-GATE DRIVERS

The Sample-Gate Drivers (SGD) produce signals that operate the Sample-Hold circuits. The SGD consists of Q360, Q361, Q362 and Q363 and related components.

When a sampling sequence is to begin the Hold line will be at a high-logic level. This high-logic level will turn on Q362 and turn Q363 off; the low-logic level on $\overline{\text{Hold}}$ will turn Q360 on and Q361 off. The NPN transistors, Q361 and Q362, have collector voltages of +5.0 and +4.6 V, respectively, which operate the PNP differential current switches in the Sample-Hold circuit. The PNP transistors, Q360 and Q363, have collector voltages of -4.6 and -5.0, respectively, which operate the NPN differential current switches in the Sample-Hold circuit. These operating voltages turn on transistors Q372 and Q371 because the Hold line is at a high-logic level. The current path will be through R481, Q372, CR470, R470, circuit ground, R471, CR471, Q371 and R480. This current flow develops voltages of -1.0 V at CR470's cathode and +1.0 V at CR471's anode, which keeps bridge U460 reverse-biased. It presents a high impedance to C461, which "holds" its voltage.

When the Hold line is at a low-logic level it will turn on Q363 and turn Q362 off. The complementary $\overline{\text{Hold}}$ signal will be at a high-logic level, turning on Q361 and turning off Q360. This causes the output voltages of NPN transistors Q361 and Q362 to be +4.6 and +5.0 V, respectively. The PNP transistors, Q360 and Q363, now have collector voltages of -5.0 and -4.6 V, respectively. These voltages, because the Hold line is at a low-logic level, turn on Q370 and Q373 in the Sample-Hold circuit. The current path is through R481, Q373, the four diodes in U460, Q370 and R480. The impedance of U460 is low when it conducts, so the input voltage is effectively connected to storage capacitor C461.

TRANSCONDUCTANCE AMPLIFIER

The Transconductance Amplifier (TA) presents a high impedance to storage capacitors C461 and C561, and provides an output signal from the right channel to the Channel Switch stage. The right TA, described here, consists of source-followers Q460A and Q460B and paraphase amplifier Q450 and Q451.

Source-followers Q460A and B transfer the voltage from storage capacitors C461 and C561 to paraphase amplifier Q450 and Q451. Potentiometer R560 (Right Center) balances the amplifier to center the display, and R350 (Right Gain) adjusts the gain of the stage.

CHANNEL SWITCH

The Channel Switch (CS) controls the output of both Transconductance Amplifiers—it connects the left channel to the Digitizer A/D Converter and turns off the right channel, or vice versa. The CS consists of U540 and U640.

Because both channels of the CS function similarly only the right channel will be described here.

Transistors U540A, B, C and D are connected as common-base stages. Two signal lines control their switching. The bases of U540A and D (the "innerbase") receive the "off" signal, and the bases of U540B and C (the "outerbase") receive the "on" signal. The signal line with the lower voltage turns off its transistor pair, and the other line turns on its transistor pair. When the innerbase line is at the higher level, U540A and D conduct the signal to +5 V via R551—and the right channel is off. When the outerbase line is at the higher level, U540B and C conduct the + and - signals to the + and - Analog Signal lines.

CONTROL LOGIC

The Control Logic (CL) circuitry generates signals that control the Sample-Gate Drivers, the Channel Switch,

and the Extra Write gate on diagram 9. The CL consists of U270A; U280A and B; U180A, B, C and D; U130D; and U170A, B and C.

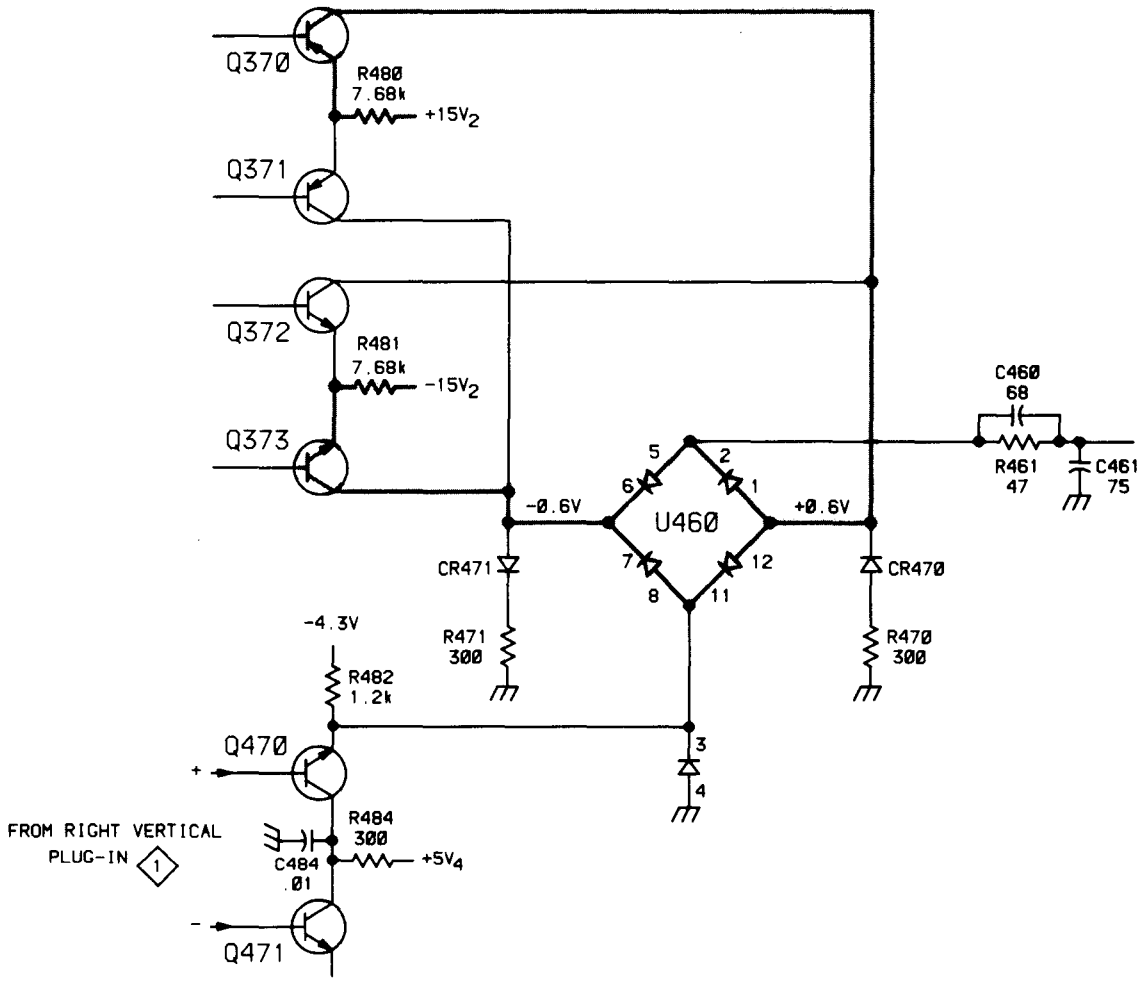
Sample-Gate Flip-Flop

Flip-flop U280B and related components produce the complementary Hold signals which control the Sample-Gate Drivers. It has three modes of operation, as follows:

1. 5B25N Time/Div not set to 0.1 ms. In this situation the Sample pulses occur more than 2 μs apart, which is sufficient to make two A-D conversions (left sampled data, then right sampled data) that take 1 μs each.

2. 5B25N Time/Div set to 0.1 ms and one vertical plug-in unit in use. When the Time/Div control is set to 0.1 ms, Sample pulses occur at 1 μs intervals. This allows time for only one A-D conversion per Sample pulse.

3. 5B25N Time/Div set to 0.1 ms and two vertical plug-in units in use. When the Time/Div control is set to 0.1 ms, Sample pulses occur at 1 μs intervals. Only one A-D conversion can occur per Sample pulse. Because two



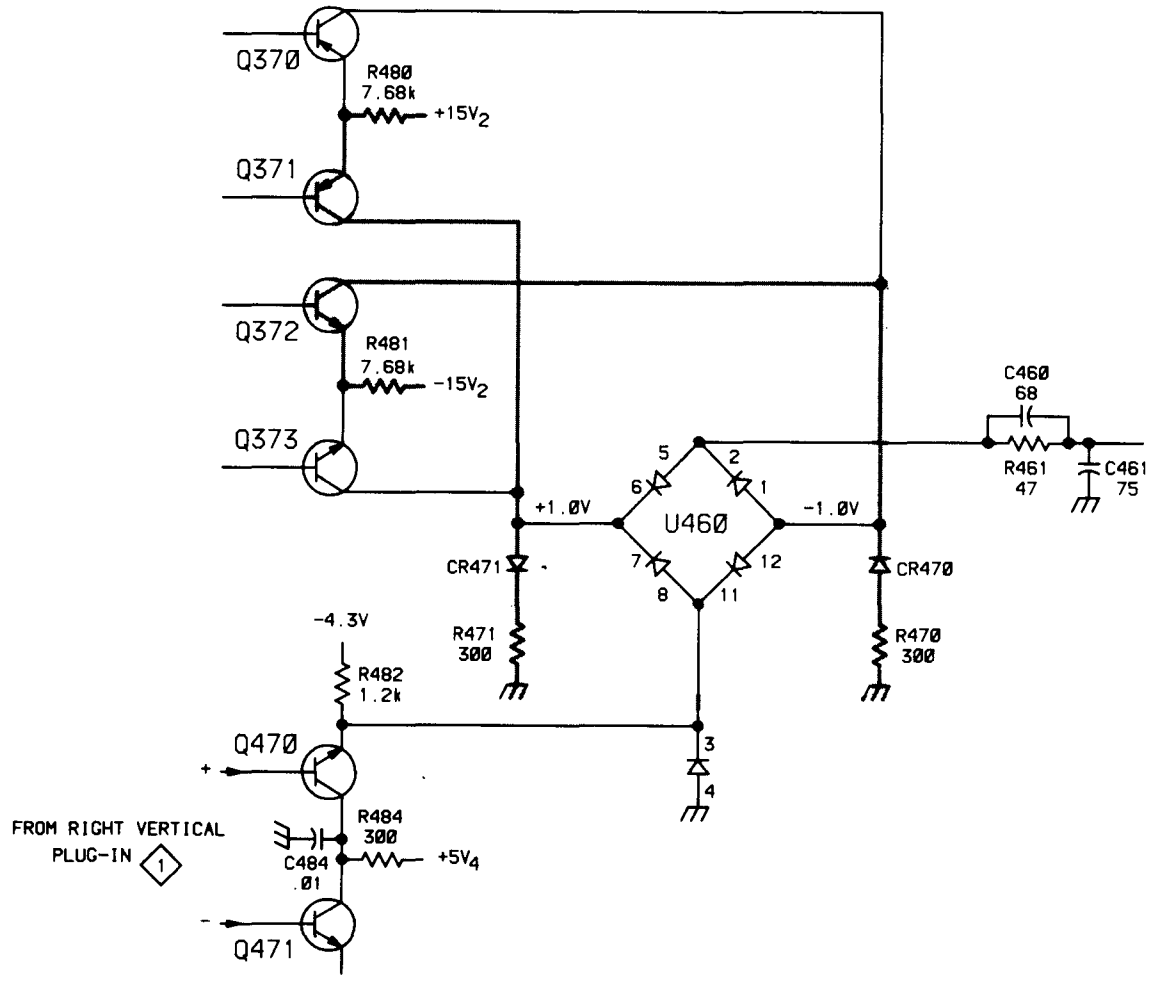
A. DURING SAMPLE, THE CONDUCTING DIODE BRIDGE (U460) CONNECTS THE INPUT TO THE STORAGE CAPACITOR (C461)

C2932-305A

Figure 4-13. Operation of sample-hold gate.

vertical plug-in units are in use, the actual digitizing rate is half the sampling rate. Each sample is stored in two memory locations to fill the memory.

5B25N Not at 0.1 ms/Division. When the $\overline{100\ \mu s}$ line is at a high-logic level (5B25N not at 0.1 ms/division), Q181 will be off and the Left On•Right On•100 μs line will apply a low-logic level to the J input of U270A. The first $\overline{\text{Sample}}$ pulse clocks U270A and U280B; U270A applies a high-logic level to U280B's K input. The coincidence of the high-logic level on its K input and the $\overline{\text{Sample}}$ pulse on the Clock input resets U280B, which asserts a high-logic level on the Hold line and a low-logic level on its pin 9 output. The low-logic level from U280B pin 9 disables U170A and B. In this "not in 0.1 ms" mode, the high-logic level on $\overline{100\ \mu s}$ disables U180B, which via U180C, also disables U180A and enables U170D. When enabled, U170D inverts the Left signal and applies it to U130D, enabling U130D to respond to the second End signal and set U280B. When set, U280B asserts a low-logic level on the Hold line. Figure 4-14 shows the timing of these events, and Table 4-3 shows their truth table.



B. DURING HOLD THE REVERSE-BIASED DIODE BRIDGE (U460) DISCONNECTS THE INPUT FROM THE STORAGE CAPACITOR (C461).

C2932-305B

Figure 4-13 (cont). Operation of sample-hold gate.

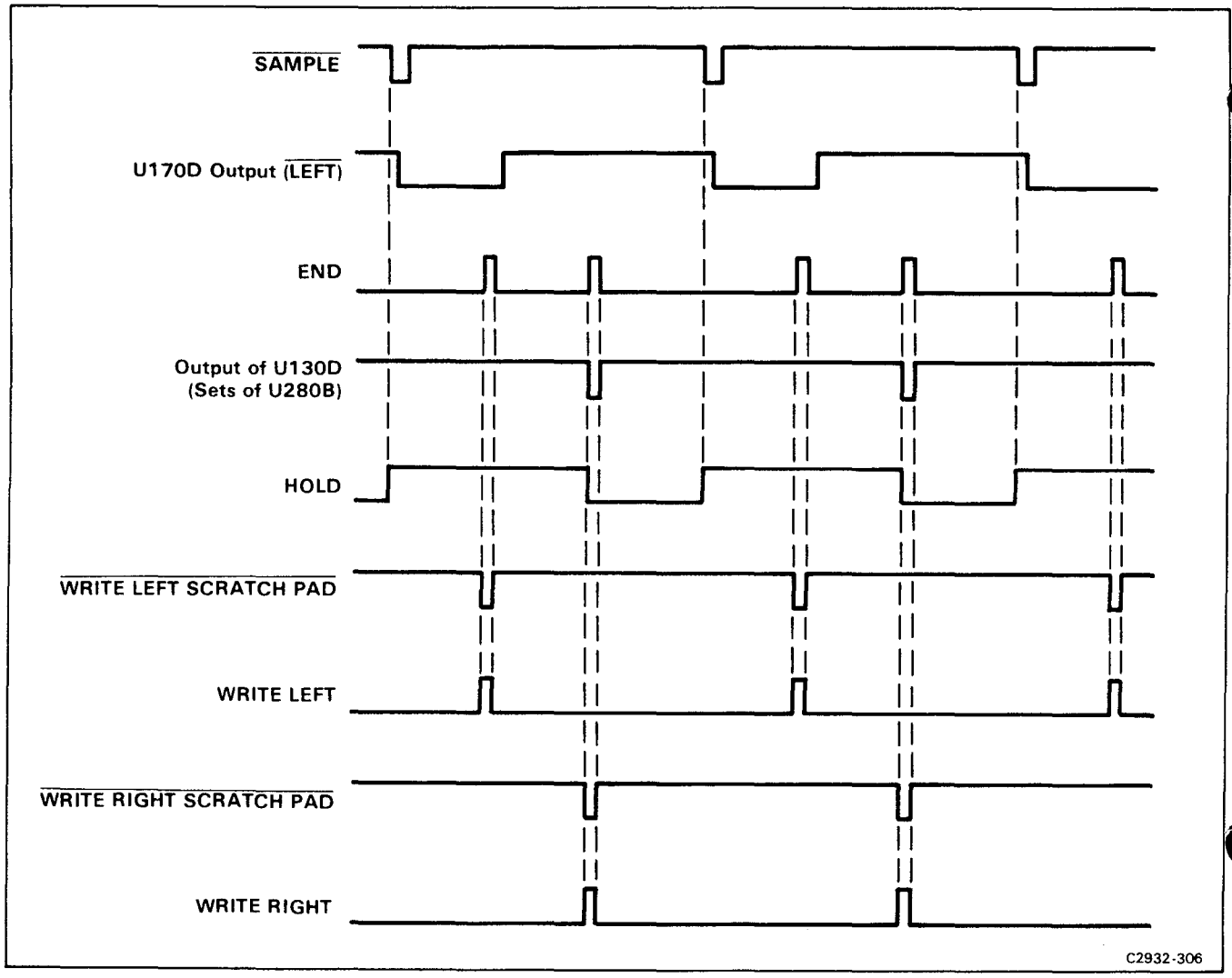


Figure 4-14. Sample-hold control logic. 5B25N Time/Div not set to 0.1 ms.

TABLE 4-3
Truth Table of Digitizer Mode-Control Functions

Plug-In Controls			Interface Logic Levels			Control Logic Levels				
Display								Chan Sw Preset Enable		
LEFT VERT	RIGHT VERT	HORIZ TIME/DIV	LEFT ON• RIGHT ON	RIGHT ON	100 μs	LEFT ON• RIGHT ON• 100 μs (Q181)	SINGLE (U180C-10)	RIGHT (U170B-5)	LEFT (U170A-1)	Waveform Shown in Figure
Off	Off	not .1 ms	L	H	H	L	H	L	H	3-14
On	Off	not .1 ms	L	H	H	L	H	L	H	3-14
Off	On	not .1 ms	L	L	H	L	H	L	H	3-14
On	On	not .1 ms	H	L	H	L	H	L	H	3-14
Off	Off	.1 ms	L	H	L	L	L	L	H	3-16
On	Off	.1 ms	L	H	L	L	L	L	H	3-16
Off	On	.1 ms	L	L	L	L	L	H	L	3-16
On	On	.1 ms	H	L	L	H	H	L	H	3-15

5B25N at 0.1 ms/Division and Only One Vertical Plug-In in Use. When the 5B25N is set to 0.1 ms/division and only one vertical plug-in is in use, FF U280B is reset by the $\overline{\text{Sample}}$ pulse and set by the End pulse. Flip-flop U280B generates the Hold pulse.

In this condition, the $\overline{100\,\mu s}$ and Left On•Right On lines are at low-logic levels. This activates U180B, which activates U170D via U180C. The high-logic level output of U170D enables U130D so that the End pulse can set U280B.

Figure 4-15 shows the time relationships of these signals. Table 4-3 shows their truth table.

5B25N at 0.1 ms/Division, L & R Vertical Plug-Ins "On". When the 5B25N is set to 0.1 ms/division and both vertical plug-in Display buttons are pressed in, the $\overline{100\,\mu s}$ line will be at a low-logic level and the Left On•Right On line will be at a high-logic level. Transistor Q181 will be on and the Left On•Right On•100 μs line will apply a high-logic level to U270A's J input. $\overline{\text{Sample}}$ pulses will now cause U270A to toggle and apply alternate low- and high-logic levels to U280B's K input. The first $\overline{\text{Sample}}$ pulse resets U280B (because its J and K inputs are at low- and high-logic levels, respectively), which produces a high-logic level on the Hold line. The high-logic level on Hold lasts until the second End pulse

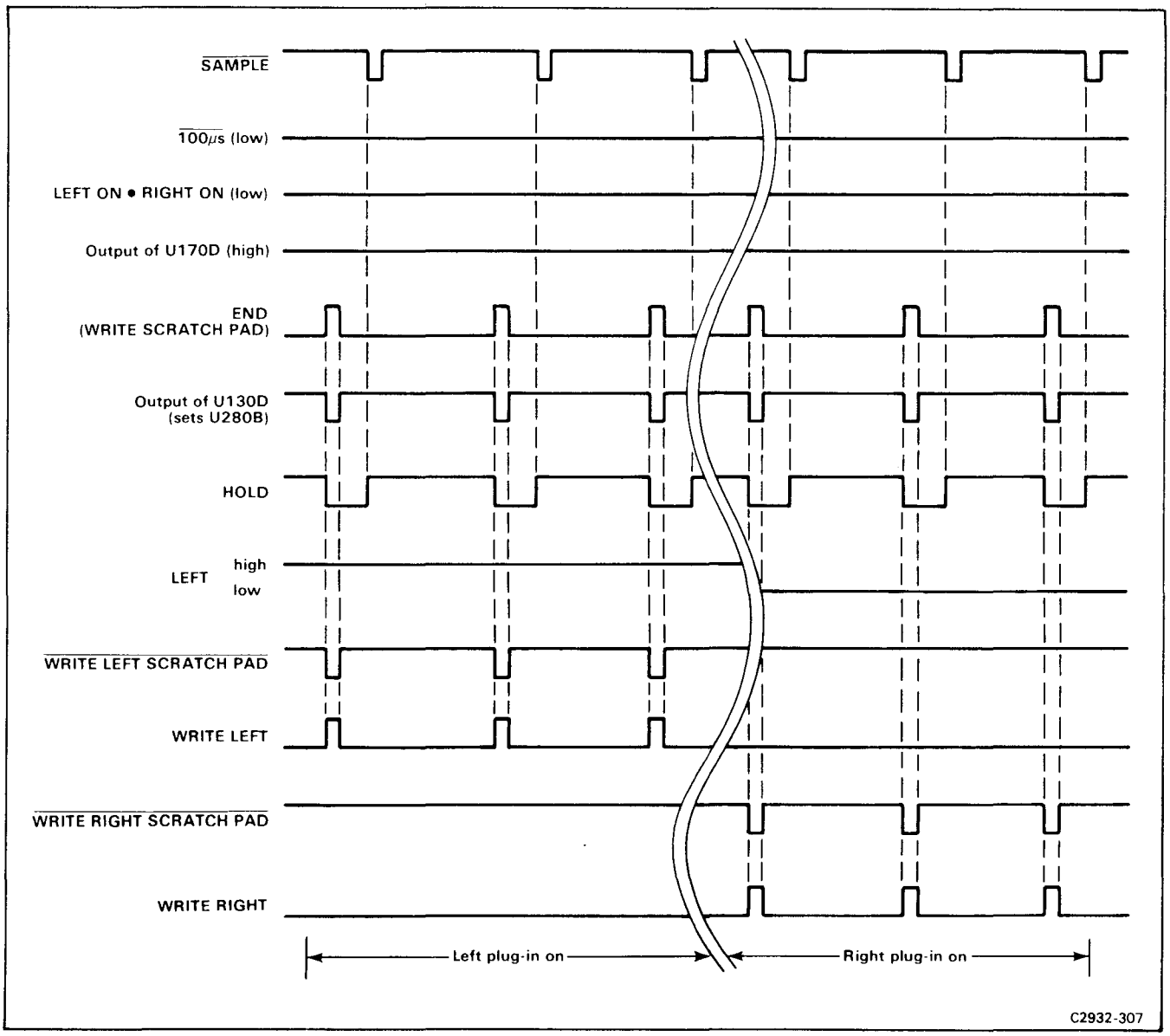


Figure 4-15. Sample-hold control logic, 5B25N Time/Div set to 0.1 ms; only one vertical "on".

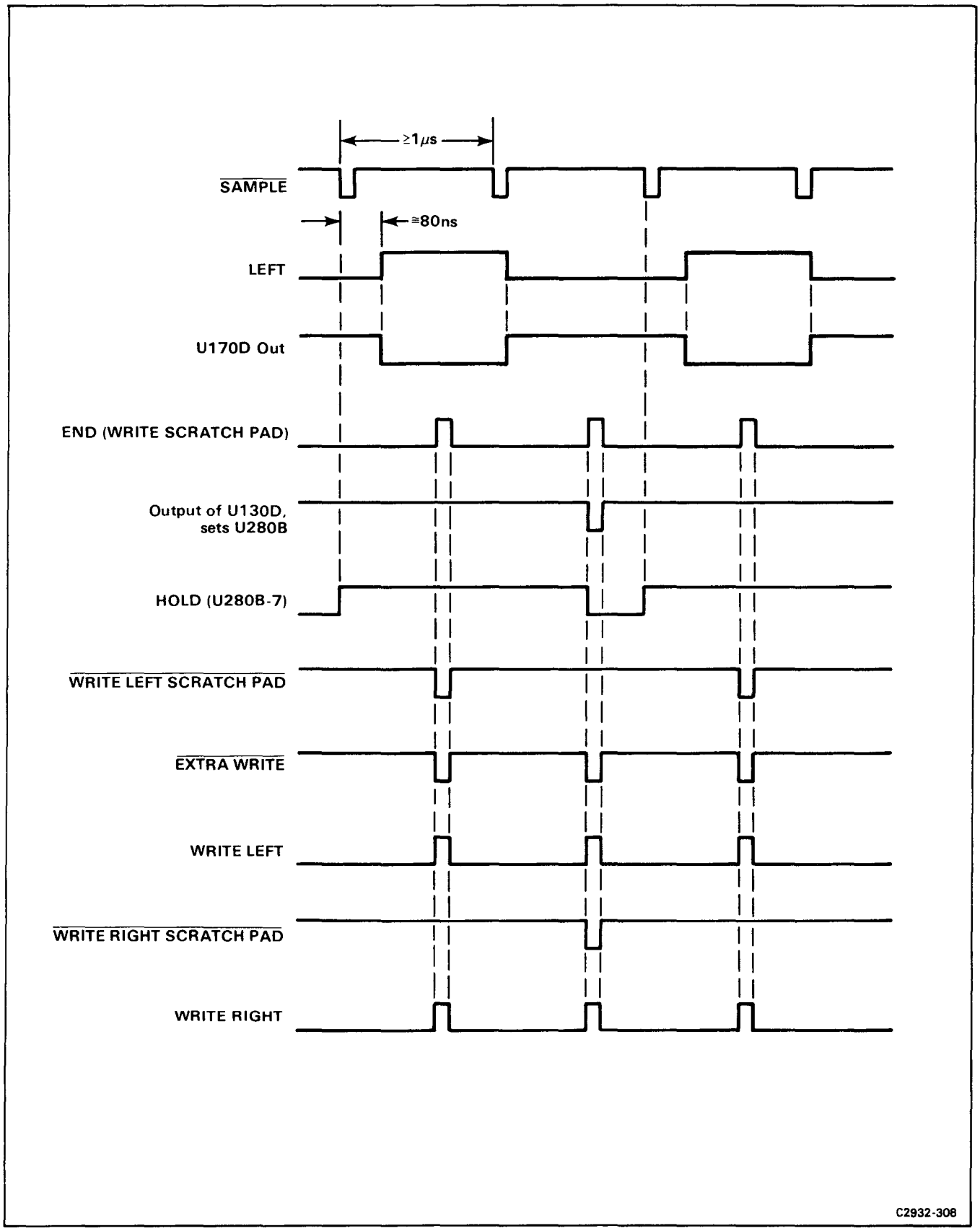


Figure 4-16. Sample-hold control logic, 5B25N Time/Div set to 0.1 ms, left and right vertical "on".

activates U130D to set U280B (U130D is enabled by the high-logic level from U170D when Left is at a low-logic level). The second Sample pulse has no effect on U280B because its J and K inputs are at low-logic levels. In this mode, U270A and U280B effectively divide the Sample frequency by two. Sample pulse #3 resets U280B to repeat the operation.

Gates U1291C and D, on diagram 11, combine the Write Scratch Pad signal (another name for the End signal) and the Left and Right signals to form the Write Left Scratch Pad and Write Right Scratch Pad signals. Gates U1291A and B, also on diagram 11, produce the Write Right and Write Left signals in response to the appropriate Write Scratch Pad signal or the Extra Write signal.

Figure 4-16 shows the timing relationship of these signals. Table 4-4 shows their truth table.

TABLE 4-4
Channel Switch Logic

100 μs	Left On•Right On	U180C Pin 10	
L	L	L	Condition 1
L	H	H	Condition 2
H	L	H	
H	H	H	

CHANNEL SWITCH

Flip-flop U280A produces the signals that control the Channel Switch circuit. Just prior to the beginning of a digitizing sequence, the high-logic level from U280B pin 9 enables U170A and B. The levels on the Right On, 100 μs and Left On•Right On lines determine which section of U170 will be activated.

When the 100 μs and Left On•Right On lines are in Condition 1 (see Table 4-4), U180B is activated. Via U180C, gate U180B then causes a low-logic level at U180A's pin 2 input. In this condition a low-logic level on Right On will activate U180A, which will apply a high-logic level to U170B and, via U180D, a low-logic level to U170A. If the Hold line is at a high-logic level, the high-logic level from U180A will activate U170B, which will apply a low-logic level to the set input of FF U280A. When set, U280A will assert a high-logic level on its pin 5 output. The high-logic level from U280A pin 5 will turn on the right Channel Switch and turn off the left Channel Switch. If the Right On line is at a high-logic level, U180A will be disabled regardless of the condition of the 100 μs and Left On•Right On lines. If the Hold line is at a high-logic level, the low-logic level output of U180A will activate U170A (via U180D), which will reset FF U280A. When reset, U280A will assert a high-logic level on its pin 6 output that will turn on the left Channel Switch and turn off the right Channel Switch.

All other combinations of inputs on the 100 μs and Left On•Right On lines will disable U180B. See Table 4-4. When U180B is disabled it will apply a high-logic level, via U180C, to U180A's pin 2 input. This high-logic level will disable U180A, which will then ignore the level on the Right On Line and apply a low-logic level to U170B and, via U180D, a high-logic level to U170A. The high-logic level will activate U170A, which will assert a low-logic level on the reset input of U280A. When reset, U280A will assert a high-logic level on its pin 6 output. The high-logic level from U280A pin 6 will turn on the left channel switch and turn off the right channel switch.

While a digitizing sequence is in process, the Clock signal that occurs when the Carry line is at a high-logic level will cause U280A to toggle. This causes the digitizing sequence to be left, then right when two plug-in units are turned on. In single-plug-in mode when the time base is set to 0.1 ms/division, FF U280A also toggles when the Carry line is at a high-logic level. However, in this mode U170D will be active, enabling U130D. In this situation, the End pulse will set U280B, which will produce a high-logic level on the Hold line that will activate either U170A or B. The activated gate will set or reset U280A, returning it to its previous state and providing single-channel digitizing.

9
DIGITIZER A/D CONVERTER

The Digitizer A/D Converter (DADC) produces a 10-bit word that represents the voltage of each sample from the Digitizer Sampler (diagram 8). The DADC consists of a Clock Generator, a Timing-Counter/Decoder, a Successive-Approximation Register, a D/A Converter and a Comparator.

CLOCK GENERATOR

The Clock Generator (CG) produces groups of 10 clock pulses for the Timing Counter/Decoder and the Control Logic section of the Digitizer Sampler (diagram 8). The CG consists of an oscillator (Q143, Q142), a gate that turns the oscillator on and off (Q140, Q141) and a gate to control the output clock pulses (U130B).

Transistors Q143 and Q142 form a Bose oscillator whose operating period is about 81 ns. Transistors Q140 and Q141 are arranged as a negative-input OR gate which stops the oscillator when a low-logic level occurs on the $\overline{\text{End}}$ or the Hold line. The Timing Counter/Decoder counts pulses from the oscillator and when the first 10 pulses have occurred, produces a low-logic level on the $\overline{\text{End}}$ line. The low-logic level on $\overline{\text{End}}$ turns on Q141 (for 50 ns), whose collector voltage goes positive to -3.7 V which is more positive than the operating range of Q143's emitter. Figure 4-17 shows details of this timing and voltage. The oscillator is off while the Channel Switch in the Digitizer Sampler (diagram 8) switches from the left plug-in signal to the right plug-in signal. When the $\overline{\text{End}}$ line returns to a high-logic level the oscillator generates a second group of 10 pulses, and again a low-logic level on $\overline{\text{End}}$ stops the oscillator. Shortly after the $\overline{\text{End}}$ pulse starts, a low-logic level occurs on the Hold line—it stays low and holds the oscillator off until the 5B25N produces another $\overline{\text{Sample}}$ pulse that starts another Hold pulse. During one sample time period the Clock Generator has produced two groups of 10 pulses that initiate A/D conversions of both left and right channel information (except when the time base is set to 0.1 ms/div or when only one plug-in is in use.)

While the oscillator is operating, a high-logic level on the $\overline{\text{End}}$ line enables it to pass pulses to the $\overline{\text{Clock}}$, and via inverter U130C, the Clock lines.

Transistor Q150 prevents the collector voltage of gate Q140-Q141 from going more positive than -3.7 V.

TIMING COUNTER/DECODER

The Timing Counter/Decoder (TCD) receives Clock pulses and produces: (a) nine "time-slot" signals for the Successive-Approximation Register, (b) the End and Carry signals for the Digitizer Sampler (diagram 8), and (c) the $\overline{\text{Extra Write}}$ and Write Scratch Pad signals for the Memory, via diagram 11. The TCD circuit consists of decade counter U230, binary-to-decimal decoder U220-U310D, pulse generator Q430-U420D, FF U270B, gate U170C and inverter U130A. Figure 4-17 shows the timing of events in the TCD.

$\overline{\text{Clock}}$ pulses increment counter U230, which produces a binary version of the number of $\overline{\text{Clock}}$ pulses it has received. The ninth $\overline{\text{Clock}}$ pulse causes U230 to produce a high-logic level on the Carry line, which connects to U270B's K input and to the Digitizer Sampler (diagram 8). The tenth $\overline{\text{Clock}}$ pulse causes FF U270B to assert a high-logic level on the End line for about 50 ns, which signifies that an analog sample has been digitized and the A/D conversion cycle is complete. Flip-flop U270B reverts to its set state after 50 ns because it is wired as a one-shot. The End pulse goes directly to the Memory as Write Scratch Pad. When the Left On•Right On•100 μs line is at a high-logic level, the End pulse activates U170C to produce the $\overline{\text{Extra Write}}$ signal for the Memory. Inverter U130A applies the complement of the End signal to the Successive-Approximation Register and the Clock Generator.

Decoder U220-U310D receives the four-line binary output of counter U230 and produces a low-logic level on the output line of the equivalent decimal value. Transistor Q430 and gate U420D produce the $\overline{\text{Enable}}$ pulse, for decoder U220, in response to the Clock pulse. The emitter voltage of Q430 will go negative faster than it will go positive because of C520. The charge time of C520 delays the leading edge of the Enable pulse about 13 ns from the leading edge of the Clock pulse to allow the comparator to "settle" after Clock pulses. The $\overline{\text{Enable}}$ pulse enables U310D to produce the Timeslot 8 signal—which occurs when U230 asserts a high-logic level on its pin 11 output. The other output of U420D, Enable, enables decoder U220 to decode the input from counter U230. When enabled, U220 asserts a low-logic level on the appropriate output line for "Timeslots" 0 through 7. When the ninth clock pulse causes counter U230's output to be 1000, the 1 is a high-logic level on U230 pin 11 and the three zeros are low-logic levels on U230 pins 12, 13, and 14. The high-logic level from U230 pin 11 and the high-logic level on the Enable line from U420D pin 9 activate U310D, which asserts a low-logic level on the Timeslot 8 line.

SUCCESSIVE-APPROXIMATION REGISTER

The Successive-Approximation Register (SAR) produces 10 successive digital codes that signify 10 possible voltage values of a signal being sampled. The 10-bit code goes to the D/A Converter which produces weighted dc currents for each input code. The Comparator will balance the dc currents from the SAR against dc currents from the Digitizer Sampler (diagram 8) to make a "greater" or "less" decision. The series of 10 "decisions" constitutes a 10-bit word that represents the voltage at a particular horizontal location. The SAR consists of initial-setup driver Q210; latching gates U300A, B, C and D, U310A, B, C, U320B, C and D; steering gates U400A, B, C, D, U410A, B, C, D and U420C.

The latching gates are AND gates with their outputs wired to one of their inputs (a). When the other input (b) is at a high-logic level, the gate will "latch" when it receives a high-logic level on the (a) input because the high-logic level on the output will hold the (b) input at a high-logic level even though the high input level may end.

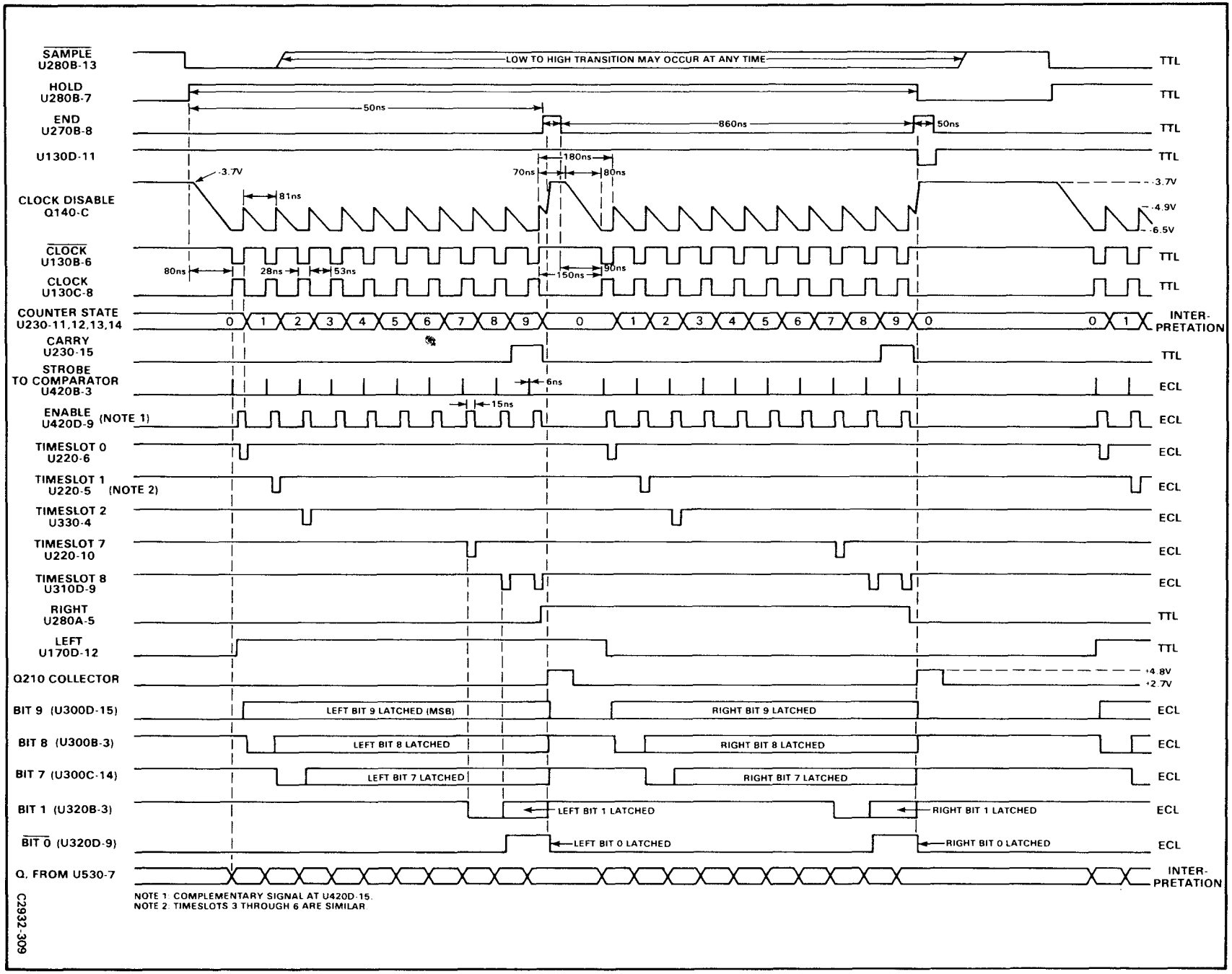
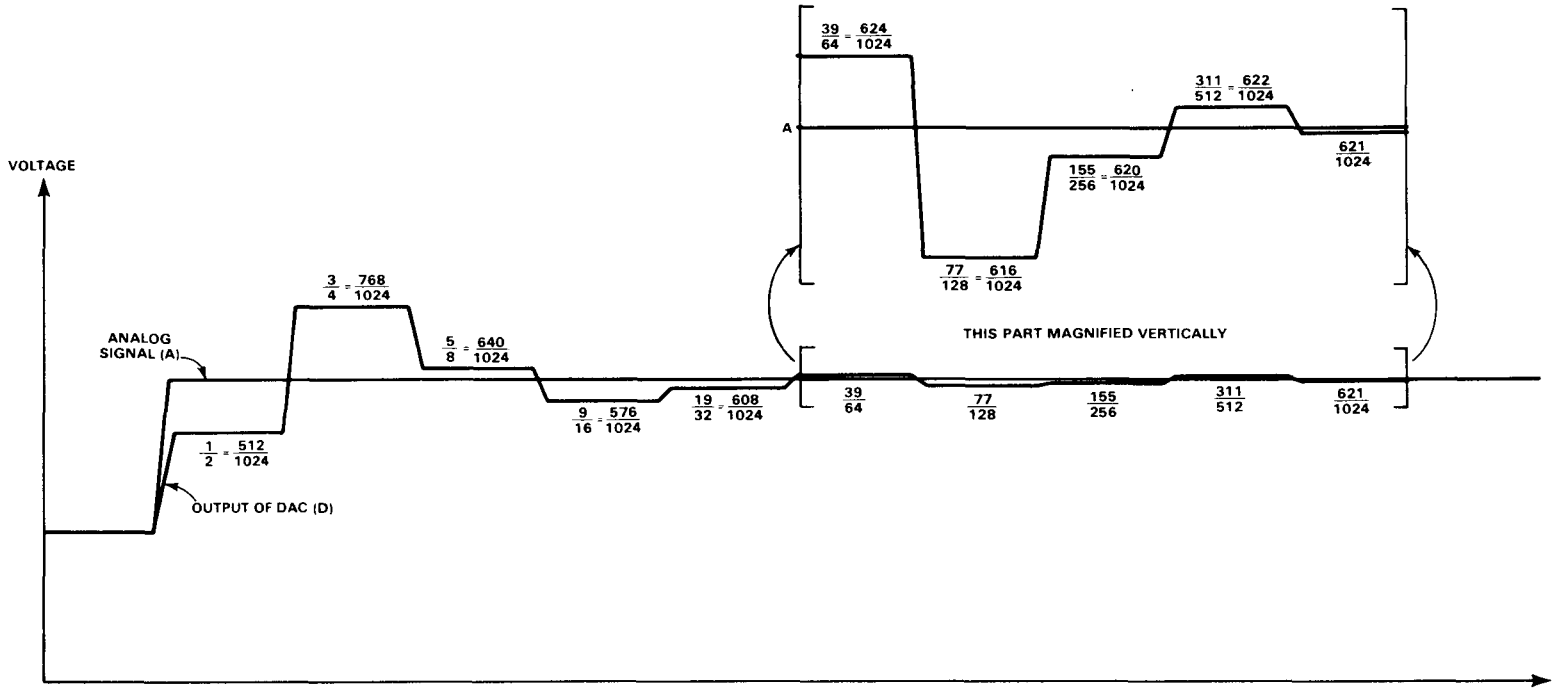


Figure 4-17. Timing of events in Digitizer A/D Converter.



		START	1	2	3	4	5	6	7	8	9	10		DATA TO MEMORY (FROM Q110)
COMPARATOR STROBE														
COMPARATOR INPUT			D<A	D>A	D>A	D<A	D<A	D>A	D<A	D<A	D>A	D<A		
COMPARATOR OUTPUT (U530-7)			L	H	H	L	L	H	L	L	H	L		
MSB	BIT 1 (U300D-15)	L	H[1]	H	H	H	H	H	H	H	H	H	H	512
	BIT 2 (U300B-3)	H	L[2]	L[1]	L	L	L	L	L	L	L	L	L	
	BIT 3 (U300C-14)	H	H	L[2]	L	L	L	L	L	L	L	L	L	
	BIT 4 (U300A-2)	H	H	H	L	H	H	H	H	H	H	H	H	64
	BIT 5 (U310C-14)	H	H	H	H	L	H	H	H	H	H	H	H	32
	BIT 6 (U310A-2)	H	H	H	H	H	L	L	L	L	L	L	L	
	BIT 7 (U310B-3)	H	H	H	H	H	H	L	H	H	H	H	H	8
	BIT 8 (U320C-14)	H	H	H	H	H	H	H	L	H	H	H	H	4
	BIT 9 (U320B-3)	H	H	H	H	H	H	H	H	L	L	L	L	
LSB	BIT 10 (U320D-15)	H	H	H	H	H	H	H	H	H	L	H	H	1/621

NOTES: 1. RESULT OF COMPARISON DETERMINES NEXT STATE: D·A· STAYS L; D·A·L CHANGES TO H.
2. H TO L TRANSITION SETS NEXT BIT FOR TEST.

C2932-314

Figure 4-18. Output of Successive-Approximation Register during A/D conversion.

To start a successive-approximation cycle, a low-logic level on the $\overline{\text{End}}$ line:

a. Clears latch U300D, which asserts a low-logic level on its output, the MSB line, and

b. turns on Q210, which produces a high-logic level that "sets" the other nine latching gates because their other inputs are held at a high-logic level by the timeslot lines.

The Clock Generator produces 10 clock pulses that cause the Timing Counter/Decoder to generate negative-going 15 ns pulses on the 0 through 8 time-slot lines. Timeslots 0 through 7 come from U220; 8 comes from U310D.

We'll describe the operation of the SAR during an A/D conversion. Figure 4-18 is a graphic representation of the process, with an arbitrary input voltage from the sampler.

Before the A/D conversion starts, a low-logic level on the $\overline{\text{End}}$ line clears U300D, which drives the Bit 9 line (it's the MSB), and Q210 sets the other nine latches to high-logic levels. (The data on the 10 lines is now 01111 11111.) The D/A Converter now furnishes a reference voltage of half full-scale (512/1024) to comparator U530.

When the first $\overline{\text{Clock}}$ pulse occurs, two things happen:

a. U530 produces a low-logic level on the Q line because the reference voltage is less than the unknown voltage, and

b. U220 asserts a low-logic level on the Timeslot 0 line, which enables U400C and clears latch U300B, which asserts a low-logic level on the Bit 8 line.

The low-logic level on Q activates steering gate U400C, whose output sets U300D. Latch U300D then holds the Bit 9 line at a high-logic level. Because only the Bit 8 line is at a low-logic level, the D/A Converter applies a reference voltage of 3/4 full-scale (768/1024) to comparator U530.

The second $\overline{\text{Clock}}$ pulse causes:

a. Comparator U530 to produce a high-logic level on the Q line because the reference voltage (768/1024) is greater than the unknown voltage, and

b. U220 to produce a low-logic level on the Timeslot 1 line.

The low-logic level on Timeslot 1 clears latch U300C, which asserts a low-logic level on the Bit 7 line. The high-logic level on the Q line has no effect on steering gate U400A, so latch U300B stays cleared and applies a low-logic level to the Bit 8 line. Because the Bit 8 and Bit 7 lines are now at low-logic levels and the other lines are at high-logic levels, the D/A Converter furnishes a reference voltage of 5/8 full-scale (640/1024) to comparator U530.

The third $\overline{\text{Clock}}$ pulse causes:

a. Comparator U530 to produce a high-logic level on the Q line because the reference voltage (640/1024) is greater than the unknown voltage, and

b. U220 to assert a low-logic level on the Timeslot 2 line.

The high-logic level on the Q line does not affect steering gate U400D, so U300C stays cleared and applies a low-logic level to the Bit 7 line. The low-logic level on the Timeslot 2 line clears latch U300A, which asserts a low-logic level on the Bit 6 line. The D/A Converter now applies a reference voltage of 9/16 full-scale (576/1024) to comparator U530.

The fourth $\overline{\text{Clock}}$ pulse causes:

a. Comparator U530 to produce a low-logic level on the Q line because the reference voltage (576/1024) is less than the unknown voltage, and

b. U220 to assert a low-logic level on the Timeslot 3 line.

The low-logic level on Q activates U400B, whose output sets latch U300A to apply a high-logic level to the Bit 6 line. The low-logic level on Timeslot 3 clears latch U310C, which asserts a low-logic level on the Bit 5 line. The D/A converter now applies a reference voltage of 19/32 full-scale (608/1024) to comparator U530.

The fifth $\overline{\text{Clock}}$ pulse causes:

a. comparator U530 to produce a low-logic level on the Q line because the reference voltage (608/1024) is less than the unknown voltage, and

b. U220 to assert a low-logic level on the Timeslot 4 line.

The low-logic level on Q activates U410D, whose output sets latch U310C (the high-logic level on Timeslot 3 enables U310C). Latch U310C now applies a high-logic level to the Bit 5 line. The low-logic level on the Timeslot 4 line clears latch U310A, which asserts a low-logic level

on the Bit 4 line. The D/A Converter now applies a reference voltage of 39/64 full-scale (624/1024) to comparator U530.

The sixth $\overline{\text{Clock}}$ pulse causes:

a. Comparator U530 to produce a high-logic level on the Q line because the reference voltage (624/1024) is greater than the unknown voltage, and

b. U220 to assert a low-logic level on the Timeslot 5 line.

The high-logic level on Q does not affect steering gate U410C, so latch U310A stays cleared and applies a low-logic level to the Bit 4 line. The low-logic level on the Timeslot 5 line clears latch U310B, which asserts a low-logic level on Bit 3 line. The D/A Converter now applies a reference voltage of 77/128 full-scale (616/1024) to comparator U530.

The seventh $\overline{\text{Clock}}$ pulse causes:

a. Comparator U530 to produce a low-logic level on the Q line because the reference voltage (616/1024) is less than the unknown voltage, and

b. U220 to assert a low-logic level on the Timeslot 6 line.

The low-logic level on Q activates steering gate U410A, whose output sets latch U310B (the high-logic level on Timeslot 5 enables U310B). Latch U310B now applies a high-logic level to the Bit 3 line. The low-logic level on the Timeslot 6 line clears latch U320C, which asserts a low-logic level on the Bit 2 line. The D/A Converter now applies a reference voltage of 155/256 full-scale (620/1024) to comparator U530.

The eighth $\overline{\text{Clock}}$ pulse causes:

a. Comparator U530 to produce a low-logic level on the Q line because the reference voltage is less than the unknown voltage, and

b. U220 to assert a low-logic level on the Timeslot 7 line.

The low-logic level on Q activates steering gate U410B, whose output sets latch U320C (the high-logic level on Timeslot 6 enables U320C). Latch U320C now applies a high-logic level to the Bit 2 line. The low-logic level on the Timeslot 7 line clears latch U320B, which asserts a low-logic level on the Bit 1 line. The D/A Converter now applies a reference voltage of 311/512 full-scale (622/1024) to comparator U530.

The ninth $\overline{\text{Clock}}$ pulse causes:

a. Comparator U530 to produce a high-logic level on the Q line because the reference voltage is greater than the unknown voltage, and

b. U310D to assert a low-logic level on the Timeslot 8 line.

The high-logic level on Q does not affect steering gate U420C, so latch U320B stays cleared and applies a low-logic level to the Bit 1 line. The low-logic level on the Timeslot 8 line clears latch U320D, which asserts a low-logic level on the Bit 0 line. The D/A Converter now applies a reference voltage of 622/1024 full-scale to comparator U530.

The tenth $\overline{\text{Clock}}$ pulse causes:

a. Comparator U530 to produce a low-logic level on the Q line because the reference voltage is less than the unknown voltage, and

b. flip-flop U270B to produce the End pulse (because of the Carry output from U230), which resets the SAR preparatory to another approximation sequence.

The low-logic level on Q affects no other circuitry—it is the last serial bit sent to the Memory.

D/A CONVERTER

The D/A Converter (DAC) converts the digitally coded outputs of the Successive-Approximation Register (SAR) to proportional differential voltages. These voltages serve as reference voltages for the Comparator. The DAC consists of two five-bit converters- one for the most-significant five bits (U520), one for the least significant five bits (U600, 610 and Q720), and a voltage regulator (U730).

The 10 sections of the DAC control currents which, depending on the input from the SAR, add to or subtract from the composite output current. The currents are weighted to values proportional to their place in the 10-bit word; i.e. the MSB current is twice the magnitude of the MSB-1 current, and so forth.

Resistors R623 through R626 attenuate the current from the U600, U610, Q720 DAC so that its outputs relate to the outputs of U520 in a correct proportion to form a contiguous 10-bit converter.

Amplifiers U730A & B establish a reference voltage for the transistors, in U520, that set the five weighted currents. Operational amplifier U730A sets the reference voltage to U730B 3.01 V below the +7.5 V reference for U520. This occurs because the R_i-R_f combination conducts 1 mA (30V/30k = 1 mA; 1 mA (3.01 k) = 3.01 V) and because U730A's minus input is at the same voltage as its plus input - zero volts. The +3.01 V across R734 sets U730B's input to a value such that its output voltage will be a level that will cause about 6.2 mA in the 480 Ω resistor that connects between pins 3 and 4 of U520. The voltage at the pin 1, 15 and 16 inputs (≈1.6 V) is the reference voltage for the five current-setting transistors in U520.

COMPARATOR

The Comparator "decides" whether the Analog signal from the Digitizer Sampler (diagram 8) is greater or less than the reference signal from the D/A converter, and produces the Serial Data output to the Memory. The Comparator consists of U530, U420A and B, Q110, Q330 and Q331.

Resistors R620, R630 and R631 sense the Analog current from the Digitizer Sampler. The output current from the DAC passes through R620. The sum of these voltages reaches pins 2 and 3 of U530.

Comparator U530 latches its outputs when its pin 4 input is at a low-logic level. When U530 pin 4 is at a high-logic level, its outputs change depending on its inputs. When a low-logic level occurs on the Clock line, gates U420A and B produce a positive-going pulse of about 6 ns duration. This happens because U420B pin 6 receives the Clock pulse directly, and activates U420B because its pin 7 input is initially at a low-logic level. The output of U420B now goes to a high-logic level. A few nanoseconds later, the positive-going output of U420A reaches U420B pin 7 (it was delayed by R430 & C431) and disables U420B, whose output returns to a low-logic level. Figure 3-17 shows these pulses and their timing.

When a strobe pulse, from U420B, occurs while U530's pin 2 input is more positive than pin 3, U530 pin 7 causes a high-logic level on the Q output. (U530 pin 8, its complement, then goes negative.) These outputs forward-bias Q331 and reserve-bias Q330, which turns on Q110. Transistor Q110 asserts a low-logic level on the Serial Data line.

-5 V AND -4.3 V SUPPLIES

Amplifier U340A is a unity-gain voltage follower which produces a -5 V output because its pin 3 input is connected to a -5 V reference, and because its feedback is not attenuated.

Transistor Q580 is an emitter-follower that provides a -4.3 V output because it is referenced to the -5 V.

+11 V SUPPLY

Amplifier U340B is a unity-gain voltage follower referenced to +5 V. The ratio of feedback to input resistors (R341/R342, 16.5 K/13.7 K) establishes a gain of about 1.2, which causes the output of Q741 to be 6 V (5 times 1.2) above the reference voltage, or +11 V.

Transistor Q741 is an emitter follower and Q721 is a current amplifier.

Transistor Q740, R738 and R737 form a foldback current-limiting circuit. If the current through R723 is high enough to produce a voltage that forward-biases Q740 (about +13.2 V), Q740 will conduct and reduce the output voltage.

MEMORY CONTENTS CONTROLLER

The Memory Contents Controller (MCC) produces 10 control signals for the memory circuits, and operates the lights in the MEMORY CONTENTS pushbuttons. The MCC consists of the following circuits:

1. Partial Blanking Source Generator, Block J
2. Debounced Switch Control, Block FFF
3. Chart Out Toggle, Block KKK
4. Digitizer Time-Base Detector, Block LLL
5. Buffered Display Indicators, Block NNN
6. Miscellaneous, Blocks RRR and AAAA

BLANKING SOURCE GENERATOR (PARTIAL), BLOCK J

The Blanking Source Generator (BSG) causes the Read Clock one-shot (U250A, diagram 12) to generate a shorter pulse when the VECTOR MODE button is pressed.

When the VECTOR MODE button is pressed, U420 pin 7 produces a low-logic which, via U300 and U410C, saturates Q320. Transistor Q320 then applies a high-logic level to the $\overline{\text{Dots}}$ line. The high-logic level on $\overline{\text{Dots}}$ effectively reduces the resistive part of U205A's (diagram 12) timing components so that its output pulse changes from 2 μs to about 300 ns in duration.

DEBOUNCED SWITCH CONTROL, BLOCK FFF

The Debounced Switch Control (DSC) produces bounce-free drive signals for other circuits in the Memory Contents Controller. The DSC consists of U320, U420 and switches S210, S220, S230, S240, S250, S260, S270 and S280.

The eight MEMORY CONTENTS controls (LEFT DISPLAY and SAVE, L VS R, RIGHT SAVE and DISPLAY, OUTPUT SAVED DISPLAY(S), ROLL and VECTOR MODE) are connected to the inputs of multiplexers U320 and U420 via the pushbutton switches mentioned above. The microprocessor calculates and writes bounce-free drive signals to latches U300 and U400A. The calculations, which are done periodically, are based on the logic levels of the pushbuttons switch contacts, which the microprocessor reads via multiplexers U320 and U420.

CHART-OUT TOGGLE, BLOCK KKK

The Chart-Out Toggle (COT) circuit produces the Chart Out Start signal for the Read Clock Source Controller (block N, diagram 12). The COT consists of flip-flop U400A.

The microprocessor may set the Chart Out Start signal high or low by writing to latch U400 at the appropriate time, as determined by its reading of the OUTPUT SAVED DISPLAY(S) button. The Memory Board may preclude this action with a low level on the Chart Out Reset line, which forces the Chart Out Start line low regardless of the microprocessor's actions. Filter R338-C400 prevents glitches from the Chart Out Reset circuitry from clearing U400A prematurely.

DIGITIZER TIME-BASE DETECTOR, BLOCK LLL

The Digitizer Time-Base Detector (DTBD) monitors the Sweep Rate line and controls the Roll Enable and $\overline{5B25}$ lines. The DTBD consists of U200A and U200B.

Comparators U200A and U200B monitor the voltage on the Sweep Rate line. U200A is referenced to +2.44 V and U200B is referenced to +3.05 V.

When the time base in use is a 5B25N with its Time/Div control not set to AMPL position, the Sweep Rate line will be below +3.05 V and U200B will assert a low-logic level on the $\overline{5B25}$ line. When the 5B25N Time/Div is set to AMPL or when a non-5B25N time base is in use, the Sweep Rate line will be above +3.05 V and U200B will assert a high-logic level on the $\overline{5B25}$ line.

When the time base in use is a 5B25N, and the Time/Div control is set anywhere from 0.1 s to 5 s, the Sweep Rate line will be above the +2.44 V reference voltage of U200A. Comparator U200A then asserts a high-logic level on the Roll Enable line. When the 5B25N Time/Div control is set to times outside the 0.1 s to 5 s range, the voltage on the Sweep Rate line will be below U200A's +2.44 V reference voltage and U200A will assert a low-logic level on the Roll Disable line.

BUFFERED DISPLAY INDICATORS, BLOCK NNN

The name "Buffered Display Indicators" (BDI) refers collectively to the LED's that light the MEMORY CONTENTS pushbuttons and the buffer that drives them. A lighted pushbutton indicates a selected function. The BDI consists of buffer U310 and LED's DS110 through DS180.

Flip-flop U300 on the Switch Board applies eight signals to U310. The signals are:

1. Display Left
2. Save Left
3. Left vs Right
4. Save Right
5. Display Right
6. Chart Out Start—OUTPUT SAVED
7. $\overline{\text{Roll}}$
8. $\overline{\text{Dots Joined}}$—VECTOR MODE

Except for number 6, Chart Out Start, which lights the OUTPUT SAVED DISPLAY(S) indicator; and number 8, $\overline{\text{Dots Joined}}$, which lights the VECTOR MODE indicator; the signals light indicators of the same name. Buffer U310 will invert a high-logic level on any of the signal lines to a low-logic level that will illuminate the appropriate indicator.

MISCELLANEOUS, BLOCKS AAAA AND RRR

In block AAAA, a low level from U410C turns off U450A, which then causes a high-logic level on the Gate Control line.

In block RRR, U450B and E form a comparator which responds to the output of U410C by producing complementary Dots Joined signals to drive switches U720A, B, C and D on diagram 18.

EXTERNAL INTERFACE PORT

Diagram 11 shows connectors J11 and J12 and part of the circuitry on the Memory Board. The memory circuits shown on Diagram 11 are:

1. Serial-to-Parallel Converter, Block HH
2. Converter Scratch Pad, Block II
3. Scratch Pad Controller, Block LL
4. Read Clock Delay, Block TT
5. Record Intensify Generator, Block WW
6. Chop Transceiver, Block XX

Connectors J11 and J12 have two functions. First, when the 5223 operates without a peripheral GPIB device, memory-shorting boards are installed in J11 and J12. The shorting boards provide direct connection between the top and bottom pins of J11 and J12. Pins 1 through 14 and 23 through 36 are connected; pins 15 through 22 are not connected.

Second, when a GPIB peripheral is used with the 5223, it connects to J11 and J12 instead of the memory shorting boards.

SERIAL-TO-PARALLEL CONVERTER, BLOCK HH

The Serial-to-Parallel Converter (SPC) accepts serial data from the Digitizer A/D Converter and produces 10-bit parallel data words. The SPC consists of U1090 and U1290B.

Clock pulses from the Digitizer A/D Converter enter Serial Data into shift register U1090. When eight bits have been entered into U1090, the next bit causes the most significant bit to "overflow" U1090—it is entered into U1290B. The byte that enters the scratch pad (block II) consists of the LSB on the Serial Data line, the output of U1090 (the LSB + 1 through the MSB - 1) and the output of U1090 (the MSB).

CONVERTER SCRATCH PAD, BLOCK II

The Converter Scratch Pad (CSP) serves as a storage register for the output of the Serial-to-Parallel Converter. The CSP has left and right sections, and consists of hex flip-flops U960, U970, U980 and U990.

The 10-bit output of the Serial-to-Parallel Converter is connected to the input of the left CSP (U960, U980) and the right CSP (U970, U990). The output of the Serial-to-Parallel Converter changes as it receives serial data from the D/A Converter. When the Serial-to-Parallel Converter has received 10 serial data bits, the data on its 10 output lines will be valid. The Write Left S P or the Write Right S P signal will enter the data into the appropriate section of the CSP. The CSP applies its data to Data Bus A for the Left Memory and Data Bus B for the Right Memory.

SCRATCH PAD CONTROLLER, BLOCK LL

The Scratch Pad Controller (SCP) circuit clocks data from the Serial-to-Parallel Converter into the Converter Scratch Pad. The SCP consists of U1290A and U1291A, B, C and D.

Clock pulses from the Digitizer A/D Converter trigger FF U1290A and the Serial-to-Parallel Converter Simultaneously. The low-logic levels on U1290A's Q and $\overline{Q}$ outputs are determined by the Right signal from the Digitizer Sampler. When Right is at a high-logic level U1290A pin 5 will be at a high-logic level, and activate U1291D if the Write Scratch Pad line is at a high-logic level. The trailing, positive-going edge of U1291D's output will clock data from the Serial-to-Parallel Converter into the right Converter Scratch Pad.

When the Right line is at a low-logic level and the Write Scratch Pad line is at a high-logic level, the $\overline{Q}$ output of U1290A will activate U1291C. The trailing, positive-going edge of U1291C's output will clock data into the left Converter Scratch Pad.

When the $\overline{\text{Extra Write}}$ line is at a high-logic level it enables U1291B and U1291A to produce the Write Right and Write Left signals, respectively. (The $\overline{\text{Extra Write}}$ signal compensates for the Digitizer's format change when the time base is at 0.1 ms/division and both left and right plug-ins are turned on.

When the $\overline{\text{Extra Write}}$ line is at a low-logic level it activates either U1291B or U1291A, whichever has a high-logic level on its other input. The activated gate produces a high-logic level on either Write Right or Write Left.

READ CLOCK DELAY, BLOCK TT

The Read Clock Delay circuit delays positive transitions of the Read Clock signal about 50 ns and delays negative transitions about 200 ns. This occurs because of the delay of C260 and the threshold of U450A. Delaying the Read Clock signal allows the $\overline{\text{Blank}}$ pulse to turn off the crt beam before presenting a memory display.

RECORD INTENSIFY GENERATOR, BLOCK WW

Flip-flop U1691B produces high-logic levels on the A11 and B11 lines, of Address Buses A and B, that cause the 5223 to intensify only those samples taken between the last Load Stop and the next A Gate. This intensified part is the part that occurred before the trigger event that started the real-time sweep.

The positive-going transition on the A Gate line clocks U1691B which asserts a high-logic level on the A11 and B11 lines. A low-logic level on the Load Stop line will set U1691B and end its high-logic level output. Flip-flop U1691B will also produce a high-logic level on the A11 and B11 lines when a low-logic level occurs on the Roll line.

The A11 and B11 lines go through the Left and Right Buffered Memories respectively (on diagrams 15 and 16), to data buses D and C, where they are called D11 and C11. They are stored in memory with their appropriate data. The buffers in the Buffered Vertical DAC, block B on diagram 11, apply bit C11 or D11 to the V bus as bit V11. Bit V11 goes to the Z-Axis Control Signal Generator (diagram 1), via P12 pin 30, as Memory Intensify.

Storing data and using bit 11 for the Memory Intensify signal permits the stored record to be displayed with an intensified part. The intensified part will be the part that was acquired before the real-time trigger.

CHOP TRANSCEIVER, BLOCK XX

The Chop Transceiver (CT) transmits the Chop signal to the Left and Right Memories. When the system is in roll mode (0.1 s/division or slower), the chop mode is used so they can be viewed at the same time without flicker.

In equivalent-time sampling mode (50 μs/division or faster), chop mode is used to ensure that the samples are stored in chop format. The CT consists of VR1181, VR1182, Q1190, Q1191 and U1280D.

When the GPIB Z Axis line is at a high-logic level, the Chop signal from the time base will activate U1280D via Q1191. Gate U1280D will pass the Chop signal to the Left and Right Memories.

A low-logic level on the Roll or Equiv Sampled line will activate Q1190, whose high-logic level output applies a high-logic level to the Chop line to the Interface board. This high-logic level also activates U1280D, via Q1191. The Chop mode can be deactivated by the GPIB board via J12 pin 31.

12 CHART OUT AND DISPLAY CONTROLLERS

The Chart Out & Display Controllers (CODC) produce the Chart Out Reset, Blank, Real Time Select and Analog Output Off signals, and control the rate of transferring display data to an external recorder. The CODC includes the following circuits:

1. Chart Out Start/Stop Decoder, Block D
2. Display Function Generator, Block E
3. Chart Out Initializing, Block F
4. Pen-Lift Detector, Block G
5. Real Time Select Controller, Block H
6. Blanking Output, Block I
7. Blanking Source Generators, Block J
8. Blanking Controller, Block K
9. Memory Record Timeshare Generator, Block L
10. Read Master Oscillator, Block M
11. Read Clock Source Controller, Block N
12. Pen-Lift Output Control, Block O
13. Load Stop Buffer, Block P
14. Equivalent Time Detector, Block Q
15. Memory Sweep Reset, Block R
16. End-Of-Sweep Detector, Block S

CHART OUT START/STOP DECODER, BLOCK D

The Chart Out Start/Stop Decoder generates the Chart Out Reset signal and furnishes a "start location" to the memory-record timeshare generator (block L).

The decoder has six inputs, as follows:

1. Display Left.

2. Display Right.

3. Bit C10 [single- (high-logic level) or dual-channel (low-logic level) from right memory].

4. Bit D10 [single- (high-logic level) or dual-channel (low-logic level) from left memory].

5. A three-line BCD output from U160, the memory-record timeshare generator in block L. The three outputs of U160 signify:

   a. The L-$\overline{R}$ output is the memory select line; a low-logic level means right and a high-logic level means left. The Q_A output of U160 serves as the L-$\overline{R}$ signal.

b. The Mem CH 1/$\overline{\text{CH 2}}$ Select output is the channel select line; a low-logic level means CH 2 and a high-logic level means CH 1. The Q_B output of U160 serves as the Mem CH 1/$\overline{\text{CH 2}}$ Select signal.

c. The Q_C output of U160 is the "memory shutoff" line for the Chart Out Decoder.

6. A control signal from U240A, the Read Clock Source Controller, in block N.

Gate U220C monitors the Display Left, Display Right, and inverted Bit D10 line. If both left and right memories are displaying signals and the left memory contains data for a dual-channel display, U220C asserts a high-logic level at the D_A input of counter U160 in the Memory Record Timeshare Generator. For all other display combinations, U220C applies a low-logic level to U160's D_A input. The output of U220A determines the start location (left or right) for a "chart-out" sequence.

The 5223 can provide eight combinations of left-right display vs. single- or dual-channel operation, as follows:

1. Memory display ..... Left
   Left memory ..... Single-channel stored.

In this situation high-logic levels exist on pins 9, 10, and 11 of U130 because of: left memory selected (Display Left at high-logic level); right memory not selected (Display Right at low-logic level; inverted by U210D); and left memory displaying single channel (D10 at high-logic level). Gate U130 causes a low-logic level on U240F pin 13; U240 applies a high-logic level to U140 pin 13, activating U140 (because its pin 12 input is held at a high-logic level by the Mem CH 1/$\overline{\text{CH 2}}$ Select line) to apply a low-logic level to U340D. Gate U340D asserts a high-logic level on the $\overline{\text{Chart Out Reset}}$ line. (A high-logic level on Chart Out Start and a low-logic level on $\overline{\text{Saved Left}}$ cause U340C to produce a low-logic level which U240A presents as a high-logic level to U340D pin 12.) When the end of the 1024-bit recorded sweep is displayed. U470 (diagram 17) produces a high-logic level on the h_{10} line which activates U1500D. (The high-logic level on h_{10} means 2^{10} bits have been displayed.) The output of U1500D triggers one-shot U500B to generate a Page Pulse, which decrements the number in U160 (the Memory Record Timeshare Generator) from 1110 (on 2^3, 2^2, 2^1, and 2^0 outputs) to 1101. Because U140 pin 12 is monitoring the 2^1 bit, the Mem CH 1/$\overline{\text{CH 2}}$ Select line, the low-logic level there disables U140 and U340D asserts a low-logic level on the $\overline{\text{Chart Out Reset}}$ line.

2. Memory Display ..... Right
   Right Memory ..... Single channel stored.

This combination of inputs causes high-logic levels on pins 3, 4, & 5 of U130 because of: right memory selected (Display Right at high-logic level), left memory not selected (Display Left at low-logic level inverted by U210E), and left memory single channel (C 10 at a high-logic level). Gate U130 causes a low-logic level on U240F pin 13; U240F applies a high-logic level to U140 pin 13, which activates U140 (because its pin 12 is held at a high-logic level by the Mem CH 1/$\overline{\text{CH 2}}$ Select line) to apply a low-logic level to U340D pin 13. Gate U340D asserts a high-logic level on the $\overline{\text{Chart Out Reset}}$ line. (U340D is enabled by a high-logic level from U240A, which is caused by high-logic level on Chart Out Start and a low-logic level on $\overline{\text{Saved Right}}$ via U340A and U340C.) When the end of the 1024-bit recorded sweep is displayed, U470 (on diagram 17) produces a high-logic level on the h_{10} line which activates U1500D. (The high-logic level on h_{10} means 2^{10} bits have been displayed.) The output of U1500D triggers one-shot U500B to generate a Page Pulse, which decrements the number in U160 (the Memory Record Timeshare Generator) from 1110 (on the 2^3, 2^2, 2^1, and 2^0 outputs) to 1101. Because U140 pin 12 is monitoring the 2^1 bit (the Mem CH 1/$\overline{\text{CH 2}}$ Select line), the low-logic level there disables U140 and U340D asserts a low-logic level on the $\overline{\text{Chart Out Reset}}$ line.

3. Memory display ..... Left, Right
   Both memories ..... Single channel stored

This display sequence causes high-logic levels on pins 9, 10, and 11 of U230 because right memory is selected (Display Right at high-logic level) and left memory is selected (Display Left at high-logic level), and right plug-in is displaying a single channel (C10 at high-logic level). These three high-logic levels activate U230, which, via U240E, appplies a high-logic level to U140 pin 1. Because U160 is asserting a high-logic level on the Mem CH 1/$\overline{\text{CH 2}}$ Select line, U220D is active; it applies a high-logic level to U140 pin 2. This activates U140, which disables U340D by applying a low-logic level to pin 13. The pin 1- pin 2 gate in U140 now awaits a negative-going transition on its pin 2 input to disable it and cause a low-logic level on the $\overline{\text{Chart Out Reset}}$ line. The negative-going transition takes place after two 1024-bit sweeps have been displayed because U160 starts with a count of 1110 (on its 2^3, 2^2, 2^1, and 2^0 outputs) and is decremented once for every 1024 read commands. The first 1024 read commands cause the 5223 to output the right memory record—then U160 is decremented from 1110 to 1101. The second 1024 read commands cause the 5223 to output the left memory record—then U160 is decremented from 1101 to 1100. The two zeros represent low-logic levels on the pin 3 and pin 2 outputs of U160, which disable U200D. Gate U200D applies a

low-logic level to U140 pin 2, disabling it. U140 now applies a high-logic level to U340D pin 13, and U340D asserts a low-logic level on the Chart Out Reset line.

4. Memory Display ..... Left, Right
   Left Memory ..... Dual-channel
   Right Memory ..... Single-channel

This display sequence is practically the same as #3, except that it has three displays per sequence rather than two. Except for U220C, which is active and loads a high-logic level into the A section of U160 so that it contains 1111, the inputs are the same as those in sequence #3. As in sequence #3, U340D is disabled by a low-logic level from U140, and U140 awaits a 00 condition on the 2^0 and 2^1 outputs of U160 to disable U200D and cause U140 to activate U340D. Gate U340D will then generate a Chart Out Reset signal. Because U160 is set to 1111 at the start of this operation, and because it must decrement to 1100 to disable U200D and produce the Chart Out Reset signal, U160 must decrement 1111_2-1100_2=0011_2=3_{10} times. The first 1024 read commands output the information in left channel 1 memory. The second 1024 read commands output the information in the right memory and the third 1024 read commands output the information in left channel 2 memory. After the third 1024-bit group of read commands, the 2^0 and 2^1 outputs of U160 are at low-logic levels, disabling U200D and, via U240 and U340D, causing a low-logic level on the Chart Out Reset line.

5. Memory Display ..... Left, Right
   Left Memory ..... Single-channel
   Right Memory ..... Dual-channel

This situation causes high-logic levels on pins 3, 4, and 5 of U220B because:

a. Display Left is active,

b. Display Right is active, and

c. The low-logic level on the C10 line (dual-channel, right memory) is inverted by U210C.

Because the left memory is set to single channel, the D10 line is at a high-logic level. Inverter U210B applies a low-logic level to U220C pin 9, disabling U220C. Gate U220C now applies a low-logic level to U160 pin 15, causing U160 to contain 1110. Gate U220B applies a high-logic level to U140 pin 9, U160 applies a high-logic level to U140's pin 10 & 11 inputs because U160 is set to 1110.

Gate U140 is active, causing U340D to produce a high-logic level on the Chart Out Reset line. Gate U140 requires a low-logic level on its pin 9-10 input to enable U340D to assert a low-logic level on the Chart Out Reset line—the output of Memory Record Timeshare Gen U160 will then be 1011 because that is the first number, in a descending series from 1110, that contains a zero on the 2^2 output (1110, 1101, 1100, 1011). The first 1024 read commands will output right memory channel 1. The horizontal position counter then produces a high-logic level on the h_{10} line, which, via U1500D, triggers one-shot U500B. The Memory Record Timeshare Generator now decrements to 1101, and the second set of 1024 read commands will output the left memory contents. Now the Memory Record Timeshare Generator decrements to 1100, and the third set of 1024 read commands will output right memory, channel 2. The Memory Record Timeshare Generator is now decremented to 1011, which disables U140 and activates U340D to assert a low-logic level on Chart Out Reset that ends the data output process.

6. Memory display ..... Left, Right
   Left Memory ..... Dual-channel
   Right Memory ..... Dual-channel

The display settings cause high-logic levels on the Display Left and Display Right lines and low-logic levels on the C10 and D10 lines. Except for the low-logic level on D10, this situation is the same as #5. The low-logic level on D10 causes a high-logic level on U220C pin 9 which activates U220C to load a "1" into the U160's 2^0 location—U160 will contain 1111. Also as in case #5, the high-logic levels on Display Right and Display Left and the output of U210C activate U220B, which enables U140 with a high-logic level at its pin 9 input. the 2^2 output of U160 activates U140—which, as in case 5, awaits a low-logic level on its pin 9 & 10 inputs to activate U340D and cause a low-logic level on the Chart Out Reset line. After 1024 read commands the horizontal position counter produces a high-logic level on the h_{10} line. This high-logic level triggers one-shot U500B via U1500D.

The output of U500B decrements U160. The sequence of events is:

a. The first 1024 read commands will output channel 1 of the left memory.

b. Bit h_{10} decrements U160 from 1111 to 1110.

c. The second 1024 read commands will output channel 1 of the right memory.

d. Bit h_{10} decrements U160 from 1110 to 1101.

e. The third 1024 read commands will output channel 2 of the left memory.

f. Bit h_{10} decrements U160 from 1101 to 1100.

g. The fourth 1024 read commands will output channel 2 of the right memory.

h. Bit h_{10} decrements U160 from 1100 to 1011.

i. The low-logic level on U160's 2^2 output disables U140, whose high-logic level output activates U340D to produce a low-logic level on the Chart Out Reset line—this ends the data output process.

7. Memory Display..... Left
   Left Memory..... Dual-channel

The display settings cause low-logic levels on the Display Right and D10 lines and a high-logic level on the Display Left line. Inverters U210D (Display Right) and U210B (D10) supply high-logic levels to the pin 2 and 13 inputs of U220A, and the high-logic level on Display Left activates U220A. The output of U220 activates U130, which, via U240E, applies a high-logic level to U140 pin 1. The Memory Record Timeshare Generator contains 1110 because U220C applied a low-logic level to U160's pin 15 input (the low-logic level on Display Right disabled U220C). The pin 2 input of U140 is the controlling input.

Gate U200D senses the 2^0 and 2^1 outputs of U160—when they are both at low-logic levels, U200D will disable U140 and cause a low-logic level on the Chart Out Reset line.

The sequence of events is:

a. The first 1024 read commands will output channel 1 of the left memory.

b. Bit h_{10} decrements U160 from 1110 to 1101.

c. The second 1024 read commands will output channel 2 of the left memory.

d. Bit h_{10} decrements U160 from 1101 to 1100.

e. The low-logic levels on the 2^0 and 2^1 outputs of U160 disable U200D, which applies a low-logic level to the pin 2 input of U140. This low-logic level disables U140, whose high-logic level output activates U340D to assert a low-logic level on the Chart Out Reset line—this ends the data output process.

8. Display..... Right
   Right Memory..... Dual-channel

The display settings cause low-logic levels on the Display Left and C10 lines and a high-logic level on Display Right. Inverters U210E (Display Left) and U210C (C10) supply high-logic levels to pins 3 and 4 of U230; the high-logic level on Display Right activates U230. The output of U230, via U240E, applies a high-logic level to U140 pin 1. The Memory Record Timeshare Generator contains 1110 because U220C applied a low-logic level to U160's pin 15 input (the low-logic level on Display Left disabled U220C). Gate U200D senses the 2^0 and 2^1 outputs of U160—when they are both at high-logic levels, U200D will disable U140 and cause a low-logic level on the Chart Out Reset line. The sequence of events is the same as that described in #7, except that this sequence is for the right memory, not the left.

Table 4-5 describes the various sequences of output saved displays.

DISPLAY FUNCTION GENERATOR, BLOCK E

The Display Function Generator (DFG) produces signals that influence the Pen-Lift Control, the Blanking Source Generator, the Real-Time Select and the Blanking Output circuits. The DFG consists of gates U110D, U200A, U330C, U410D, and U1280A and B.

When the Chart Out Start line is at a high-logic level and either Saved Left or Saved Right is at a low-logic level, U340C (End-of-Sweep Detector, Block S) will be active and produce a low-logic level that disables U110D. The low-logic level output of U110D has two effects, as follows: a. It sets U320B and resets U250A (both in the Blanking Source Controller, Block J) which prevents Blank pulses, and b. disables U1400D and U1670C, which cause the Real-Time Select circuit (Block H), to produce the Real Time Select signal. This eliminates the memory display.

If the Chart Out Start line is at a low-logic level or if both Saved Left and Saved Right are at high-logic levels, U340C will be disabled. Its high-logic level output will enable U110D. A high-logic level on Display Left or Display Right will activate U200A, and U200A's output will then activate U110D. When active, the high-logic level output of U110D enables U1400D and U1670D in the Real-Time Select circuit, and in the Blanking Source Generator, permits FF U320B and one-shot U250A to function.

TABLE 4-5
Output Saved Displays(s)

Displayed Waveform Acquisition Conditions		Output Sequence
Left Vertical Plug-In	**Right Vertical Plug-In**	**Y Outputs (X Output is a Ramp)**
Single	Single	Right, Left
Single	Dual	Right Channel 1, Left, Right Channel 2
Dual	Single	Left Channel 1, Right, Left Channel 2
Dual	Dual	Left Channel 1, Right Channel 1, Left Channel 2, Right Channel 2
Dual	Off	Left Channel 1, Left Channel 2
Off	Dual	Right Channel 1, Right Channel 2
		L Vs R Outputs
Single	Single	2 Plots L/R
Single	Dual	2 Plots of L/R_2, 1 Plot L/R_1
Dual	Single	2 Plots of L_1/R, 1 Plot L_2/R
Dual	Dual	2 Plots of L_1/R_1, 2 Plots L_2/R_2

CHART OUT INITIALIZING, BLOCK F

The Chart Out Initializing (COI) circuit generates two signals—one that triggers the Memory Sweep Reset circuit, and one the loads the Memory Record Timeshare Generator. The COI circuit consists of gate U1500D and inverter U240B.

Gate U1500D has two inputs, the h_{10} line from the Horizontal Position Counter (diagram 17 block 000), and the output of U530D in the Pen-Lift Detector, block G. Exclusive-OR gate U530D is normally disabled, and its output is at a low-logic level that enables U1500D. When the Horizontal Position Counter receives the 1024th read command, it asserts a high-logic level on the h_{10} line. This high-logic level activates U1500D, which produces a low-logic level that triggers one-shot U500B in the Memory Sweep Reset circuit. When U530D, in the Pen-Lift Detector, is activated it produces a high-logic level that activates U1500D. Gate U530D will be activated briefly when U240A applies a low-logic level to U530D pin 12. Via inverter U240B, the high-logic level output of U530D does two things, as follows:

1. It loads the Memory Record Timeshare Generator, block L, and

2. It causes the End-of-Sweep Detector, block S, to generate a signal that; (a) starts block J producing blanking, and, (b) initiates the pen-lift operation via block O.

PEN-LIFT DETECTOR, BLOCK G

The Pen-Lift Detector produces a signal that:

1. when at a low-logic level, stops the Chart Out Oscillator, or

2. when at a high-logic level, permits the output of the Chart Out Oscillator to reach the Read Clock Source Controller.

The Pen-Lift Detector consists of gates U310D, U530C and D, and one-shot U250B.

Gates U310D and U530D sense the output of U240A, which is at a high-logic level when a "chart-out" sequence is occurring. The high-logic level has two effects, as follows:

1. it enables U310D and

2. it disables exclusive-OR gate U530D.

Because U310D is enabled, a high-logic level from U160 on the L-$\overline{R}$ line will activate U310D. The low-logic level output of U310D reaches U530C's pin 10 input before it reaches the pin 9 input because of the delay caused by R620-C630. Exclusive-OR gate U530C will be activated while its inputs are at different levels, and via U200C, will produce a short positive-going pulse that will trigger one-shot U250B. One-shot U250B produces the Pen-Lift Detector's output signal, a negative-going pulse.

If a low-logic level occurs on the output of U240A, it will activate U530D (in the manner described for U530C in the preceding paragraph), which will produce a short positive-going pulse. This output pulse has two applications, as follows:

1. it will trigger one-shot U250B to produce an output signal, and

2. it reaches the Chart Out Initialize circuit, block F, where U240B inverts it to a negative-going pulse that loads data into U160 in the Memory Record Timeshare Generator.

The positive-going pulse from U530D also activates U1500D to trigger one-shot U500B. The Page Pulse output of U500B would decrement U160 if U160 were not being simultaneously loaded by the low-logic level from U240B, which has priority over the decrement input signal.

REAL TIME SELECT CONTROLLER, BLOCK H

The Real Time Select Controller circuitry generates two signals, the Real Time Select signal for the vertical and horizontal channel switches and the Z-Axis Amplifier, and the "Early Real Time Select" signal for the Blanking and Read Clock Source Controllers. The Real Time Select circuit consists of U1670A, U1640F, U1400D, U1670C, U1395A, U1495A, Q1295, and associated components.

A low-logic level on Left On will disable U1280A, and a low-logic level on Right On will disable U1280B. A low-logic level from either of these gates will activate U410D. When active, U410D asserts a high-logic level on the Real Time On line which enables U330C. If the Roll line is at a high-logic level, U330C is active and it applies a high-logic level to U1670C pin 10. Of U1670C's other two inputs, one (pin 9) is connected to the output of U110D, which is at a high-logic level when the memory display is enabled, and the other (pin 11) is connected to the inverted output of Q340. (The low-logic level on Equiv Sampled keeps U1670A disabled and U1400D active.) When the Chart Out Start line is at a low-logic level it disables U340C which applies a high-logic level to the pin 13 input of U110D. A high-logic level on the Display Left or Display Right line will cause U200A to activate U110D. If U1670A is disabled, U1640F will apply a high-logic level to U1400D pin 12, and the high-logic level output of U110D then activates U1400D. When active, U1400D applies a high-logic level to exclusive-OR gate U1495A. If U1495A's other input is at a low-logic level, it causes a high-logic level on the Real Time Select line. A low-logic level on the Sweep Rate line cause the Q340-U240C combination to apply a high-logic level (Display Memory During Holdoff) to U1670C pin 11, activating it. Gate U1670C now enables U1395A, and an A Gate will activate U1395A to produce the "Early Real Time Select" signal for the Blanking Controller, Block K, and the Read Clock Source Controller, Block N. If the 5223 is in equivalent-time sampling mode, the Early Real Time Select signal will cause the memory display to occur during real-time holdoff, that is, while the A Gate is at a low-logic level. When activated, U1395A's low-logic level output reaches T-filter L1395-L1495-C1496-C1495 via CR1395, CR1294, and Q1295. The T-filter delays the Real Time Select signal from the A Gate. In situations when U1640F disables U1400D and U110D is active, the output of the T-filter will activate U1495 to produce a Real Time Select signal.

BLANKING OUTPUT, BLOCK I

The Blanking Output circuit generates the Blank signal, which drives the Z-Axis Amplifier via the Interface board. A low-logic level on Blank causes the Z-Axis Amplifier to turn off the crt display. The Blanking Output circuit consists of U440C, U1395C, U1395D and U1495D.

When the 5223 is operating in equivalent-time sampling mode (50 μs/division or faster), it presents the memory display during the holdoff time between real-time sweeps. The Blanking Output circuit uses the A Gate signal from the time base to produce two Blank pulses, one at the beginning and one at the end of the holdoff period, to turn off the crt beam while the display is being switched from real-time to memory and back.

The A Gate from the 5B25N Time Base will cause $\overline{\text{Blank}}$ pulses because a high-logic level on the Display Memory During Holdoff line will activate U440C, which enables U1395D. (A low-logic level on Sweep Rate, via Q340, causes U240C to assert a high-logic level on Display Memory During Holdoff.)

A high-logic level on the A Gate line activates U1395D, which applies a low-logic level to U1495D pin 13, disabling it and causing a low-logic level on the $\overline{\text{Blank}}$ line. The low-logic level from U1395D also reaches the pin 9 input of U1395C via delay network L1291-C1291, disabling U1395C. The high-logic level output of U1395C activates U1495D, because its inputs are again at different levels, and causes a high-logic level on the $\overline{\text{Blank}}$ line. This $\overline{\text{Blank}}$ pulse turns off the crt while the display is being switched from memory to real time.

A reverse sequence of events takes place at the end of the A Gate pulse, when the low-logic level on the A Gate line disables U1395D. The high-logic level from U1395D then disables U1495D, which asserts a low-logic level on the $\overline{\text{Blank}}$ line. The high-logic level from U1395D reaches the pin 9 input of U1395C via delay network L1291-C1291, and activates U1395C. The low-logic level output of U1395C activates U1495D, which ends the $\overline{\text{Blank}}$ pulse by asserting a high-logic level on the $\overline{\text{Blank}}$ line. This $\overline{\text{Blank}}$ pulse turns off the crt while the display is being switched from real-time to memory.

When the A Gate line is at a low-logic level or when U440C is disabled by the Sweep Rate signal (via Q340 and U240C), the Blanking Controller, Block K, can cause $\overline{\text{Blank}}$ pulses. When the Blanking Controller causes $\overline{\text{Blank}}$ pulses, they have the same duration as the input pulses from U430A—as contrasted to the situation where A Gate causes a short $\overline{\text{Blank}}$ pulse at the leading and trailing edges of A Gate. Gate U430A produces a low-logic level that disables U1395C if U1395C's other input is at a high-logic level. Gate U1395C now applies a high-logic level to U1495D which produces a low-logic level on the $\overline{\text{Blank}}$ line because U1395D is applying a high-logic level to U1495D's pin 13 input. The output of U1395D will be at a high-logic level because the low-logic level from U430A disables U440C.

BLANKING SOURCE GENERATORS, BLOCK J

The Blanking Source Generators provide inputs to the Blanking Controller, block K. A flip-flop (U320B) and two one-shots (U250A and U1620B) comprise the Blanking Source Generator.

Flip-flop U320B will produce a high-logic level output when:

1. a high-logic level occurs on the h_2 line (which ends memory sweep-to-sweep blanking), or

2. a low-logic level from U110D sets U320B (which prevents blanking when no memory is being displayed).

When the sweep ends, the End-of-Sweep Detector, block S, produces a low-logic level that resets FF U320B. Flip-flop U320B then produces a low-logic level that causes the $\overline{\text{Blank}}$ signal and starts sweep-to-sweep blanking.

When a high-logic level occurs on the Read Clock line, one-shot U250A produces a negative pulse of 2 μs duration. A low-logic level from U110D will reset U250A—this will have no effect unless it is presently generating an output. Gate U110D, in the Display Function Generator, block E, will be disabled and generate a low-logic level to reset U250A when:

1. both Display Left and Display Right are at low-logic levels (because no memory is being displayed),

2. $\overline{\text{Saved Left}}$ or $\overline{\text{Saved Right}}$ is at a low-logic level and the Chart out Start line is at a high-logic level (because a "chart out sequence" is in progress).

A high-logic level on the Qualified Write Cmd line from the right or left Memory Sequencer will activate U1500C, whose low-logic level output will trigger one-shot U1620B to produce a negative-going pulse of 10 μs duration. This blanks the display while updating the memory when the system is in roll mode. A high-logic level on the $\overline{\text{Roll}}$ line will reset U1620B.

A low-logic level from any of these generators is a "blanking" signal for block K, the Blanking Controller.

BLANKING CONTROLLER, BLOCK K

The Blanking Controller (BC) produces an input signal for the Blanking Output circuit. The BC consists of U350 and U430A.

Gate U350 receives inputs from:

1. Flip-flop U320B, which produces a high-logic level output from the third point of a digitized sweep until four points before the end;

2. One-shot U250A, which produces a negative 2 μs pulse every time the Read Clock pulse occurs;

3. One-shot U1620B, which produces a negative 10 μs pulse when a left or right Qualified Write Cmd occurs;

These four inputs cause U350 to produce a low-logic level output, with 2 μs positive pulse when Read Clock pulses occur and with 10 μs positive pulses when a left or right Qualified Write Cmd pulse takes place. If the Real-Time Select Controller is applying a high-logic level to U430A pin 2, the outputs of U350 will pass through U430A to the Blanking Output circuit.

MEMORY RECORD TIMESHARE GENERATOR, BLOCK L

The Memory Record Timeshare Generator (MRTG) generates three outputs for use in the Chart Out Start/Stop Decoder, the Pen-Lift Decoder, the Real-Time Select Controller, and the External Interface Port. The MRTG consists of four-bit down-counter U160.

The MRTG has four data inputs, a decrement input and a load input. Three of the data inputs are wired to +5 V and the other receives the "start location" bit from U220C in block D. At the start of a memory readout sequence, a low-logic level on the pin 11 input will load 111X into U160—111 in the D, C, and B sections and X (either a 1 or a 0 as the start location bit) in the A section. Only the C, B, and A outputs are used; they are labeled 2^2, 2^1, and 2^0 on the schematic. During a memory readout operation the Horizontal Position Counter (block 000 on diagram 17) produces a high-logic level on the h_{10} line when 1024 bits of data have been transmitted. A high-logic level on h_{10} activates U1500D, whose output triggers one-shot U500B. The output pulse from U500B decrements the number in U160. A low-logic level on the 2^2 output indicates that a complete sequence of data, to a chart recorder, has occurred and shuts off the Decoder for Chart Out Reset. A complete sequence is four 1024-bit data groups, which would represent left memory channel 1, right memory channel 1, left memory channel 2, and right memory channel 2.

The 2^1 output of U160 is the Memory Ch 1/$\overline{\text{Ch 2}}$ Select line; it selects memory channels when dual-trace plug in units are used in both left and right compartments of the 5223. A high-logic level selects channel 1. This bit is pertinent only when dual-channel plug-in units are in use.

The 2^0 output of U160 is the L-$\overline{\text{R}}$ line which timeshares the left and right memories. A high-logic level selects the left memory. This bit is significant only when both memory displays are in use.

When a memory readout sequence is to start, a high-logic level on the Chart Out Start line activates U340C. (A low-logic level on $\overline{\text{Saved Left}}$ or $\overline{\text{Saved Right}}$ enables U340C via U340A.) The output of U340C, via U240A, activates exclusive-OR gate U530D because the high-logic level from U240A reaches pin 12 first; C523 must charge before pin 13 is again at the same voltage as pin 12. When active, U530D produces a high-logic level that:

1. loads the MRTG, and

2. via U1500D, triggers one-shot U500B, which generates the $\overline{\text{Page Pulse}}$ signal. The output of U500B would decrement U160 except that U160 is being loaded at the same time, and the load operation has priority.

READ MASTER OSCILLATOR, BLOCK M

The Read Master Oscillator produces a 440 kHz square wave for the Read Clock Source Controller.

Inverter U400B, C520, R422 and R423 form an RC oscillator, which operates at 440 kHz. Potentiometer R422 adjusts the frequency of operation.

READ CLOCK SOURCE CONTROLLER, BLOCK N

The Read Clock Source Controller (RCSC) produces the Read Clock signal, which is used to increment the Left and Right Read Counters and the Horizontal Position Counter. The RCSC consists of gates U340A, B, and C, U310A and B, and U410A; inverter U240A; and FF U260B.

When the Chart Out Start line is at a high-logic level and $\overline{\text{Saved Left}}$ or $\overline{\text{Saved Right}}$ is at a low-logic level, U340C will be active and apply a low-logic level to inverter U240A and the pin 5 input of U340B. Inverter U240A applies a high-logic level to U320's pin 1 input which enables it to pass pulses from the Chart Out Oscillator via U310B. The low-logic level from U340C activates U340B so that pulses from the Read Master Oscillator have no effect. The high-logic level output of U340B enables U410A, permitting U310A's pulses to activate

U410A. The output of U410A clocks FF U260B, which will generate Read Clock pulses in response to the Chart Out Oscillator pulses if its J input (pin 7) is at a high-logic level. (If U260B's J input is at a low-logic level, the first clock pulse will reset it and it will not respond after that.)

When the Chart Out Start line is at a low-logic level or $\overline{\text{Saved Left}}$ and $\overline{\text{Saved Right}}$ are at high-logic levels, U340C will be disabled and apply a high-logic level to inverter U240A and the pin 5 input of U340B. Inverter U240A then applies a low-logic level to U310A, activating it and preventing it from passing Chart Out Oscillator pulses. The high-logic level from U340C enables U340B so that it will pass pulses from the Read Master Oscillator to U410A, which is enabled by the high-logic level from U310A.

Gate U410A passes Read Master Oscilator pulses to FF U260B, which generates Read Clock pulses if its J input is at a high-logic level. (If U260B's J input is at a low-logic level, the first clock pulse will reset it and it will not respond after that.)

PEN-LIFT OUTPUT CONTROL, BLOCK O

The Pen-Lift Output control (PLOC) produces an output that controls the pen of an external chart recorder. The PLOC consists of FF U300B, gate U450D and inverter U540A.

Signals from the Horizontal Position Counter, block 000 on diagram 17, turn the PLOC on and off. This causes the output signal to have one state from counts 3 to 1021, and the other state from counts 1022 to 2.

In order to produce the pen-lift output, U450D must be enabled by U340C. Gate U340C will be activated by a low-logic level on $\overline{\text{Saved Left}}$ or $\overline{\text{Saved Right}}$ and a high-logic level on Chart Out Start. If Display Left or Display Right is at a high-logic level, a high-logic level on the h_2 line will clock U300B. The output of U300B will then activate U450D, whose output will energize pen-lift relay K910. When the Horizontal Position Counter reaches count 1021, the End-of-Sweep Detector produces a low-logic level that resets U300B and ends the pen-lift output.

Some recorders require open circuits to actuate their pens; others need closed circuits. By selecting the position of jumper P929, either requirement can be satisfied.

$\overline{\text{LOAD STOP}}$ BUFFER, BLOCK P

The $\overline{\text{Load Stop}}$ Buffer provides normal and inverted $\overline{\text{Load Stop}}$ signals. It consists of Q1192 and U240D.

Transistor Q1192 inverts the $\overline{\text{Load Stop}}$ signal, which then goes to the Left and Right Memory Sequencers as G Stop Left and G Stop Right via P11 on diagram 11.

The output of U240D is again $\overline{\text{Load Stop}}$ which, when asserted, disables U500B in the Memory Sweep Reset circuit, and sets U1691B on diagram 11. When set, FF U1691B asserts a low-logic level on the A11 and B11 lines for the Left and Right Memories.

EQUIVALENT-TIME DETECTOR, BLOCK Q

The Equivalent-Time Detector produces the $\overline{\text{Equiv Sampled}}$ signal for the Real-Time Select circuit and the Chop Transceiver. The Equivalent-Time Detector consists of Q430 and U240C.

Transistor Q340 is connected to the Sweep Rate line from the 5B25N Time Base. When the 5B25N's Time/Div control is set to 50 μs or faster, the Sweep Rate line will be at about 0 V, which will cause Q340's emitter voltage (the $\overline{\text{Equiv Sampled}}$ line) to be at about +0.7 V. To U240C, +0.7 V is a low-logic level, which it inverts to a high-logic level that enables U440C and U1670C in the Real-Time Select circuit. The low-logic level on the $\overline{\text{Equiv Sampled}}$ line disables U1670A in the Real-Time Select circuit, and enables the Chop Transceiver in block XX, which asserts a high-logic level on the Chop line for the Left and Right Write Address Normalizers.

When the Sweep Rate line is above +0.7 V, Q340 puts the $\overline{\text{Equiv Sampled}}$ line above the limit of a TTL low-logic level. Inverter U240C then asserts a low-logic level on the Display Memory During Holdoff line.

MEMORY SWEEP RESET, BLOCK R

The Memory Sweep Reset circuit produces the $\overline{\text{Page Pulse}}$ signal which loads the Read Counters with the current sweep location. When a memory readout operation is in process, the Page Pulse output has two effects. If a memory page is full, Page Pulse toggles the page FF (left, U820B; right, U620A), and decrements the Memory Record Timeshare Generator. One-shot U500B and associated parts form the Memory Sweep Reset circuit.

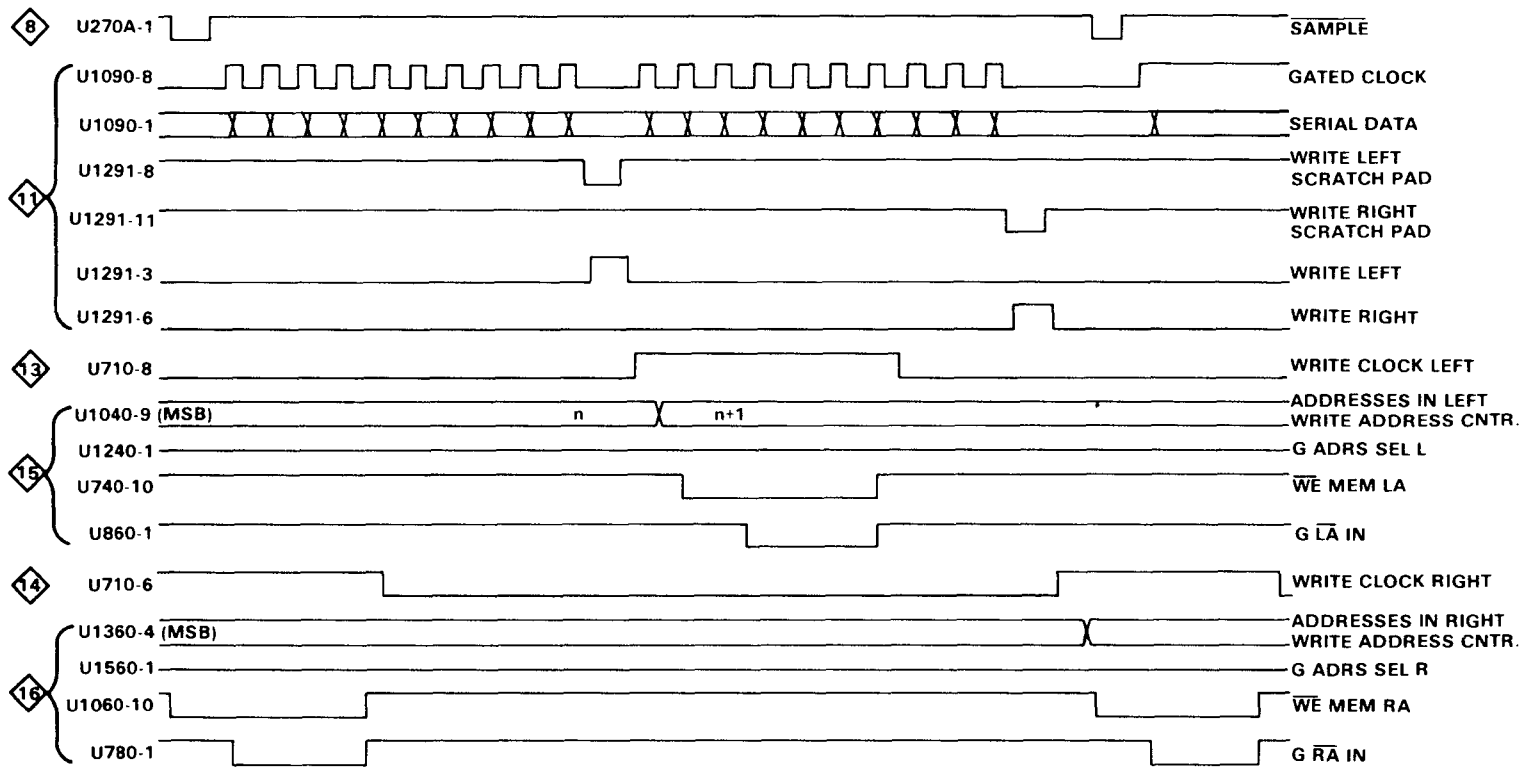


Figure 4-19. Timing of typical write-data-to-memory cycle.

A low-logic level from U1500D (in block R) while U500B's pin 10 input is at a high-logic level will trigger U500B. When it is triggered, U500B generates the Page Pulse signal. (A low-logic level on the Load Stop line, U500B's pin 10 input, will disable U500B. The negative-going edge of that low-logic level will reset U500B, which then ends its Page Pulse output signals.) The Page Pulse signal enables U110A, on diagram 11, to produce the G Adrs Load L and G Adrs Load R signals that load the Read Counters on diagrams 15 and 16. The Page Pulse signal from U500B activates U310C, on diagram 11, which clocks U600A. When U600A receives a clock pulse while the Roll line is at a high-logic level, U600A activates U110A (diagram 11) to produce the G Adrs Load L and G Adrs Load R signals that load the Read Counters on diagrams 15 and 16.

When a memory readout sequence is in process, a high-logic level on the Page Pulse line decrements the Memory Record Timeshare Generator.

END-OF-SWEEP DETECTOR, BLOCK S

The End-Of-Sweep Detector generates a pulse to reset flip-flops in the Pen-Lift Output Control Circuit and the Blanking Source Generator. Gates U330B, U460 and inverter U540C form the End-Of-Sweep Detector.

Gate U460 receives the 10 output bits of the Horizontal Position Counter; nine directly and the other via inverter U540C. Because U460 receives bit h_1 inverted, U460 will be activated at a position count of 1021 instead of 1023 as it would if bit h_1 were not inverted. Count 1021 occurs three counts before count 1024, where the sweep ends. When active, U460 applies a low-logic level to U330B, activating it (U330B's other input is held at a high-logic level by the U240B-disabled U530D combination) to produce a low-logic level that resets FF's U300B and U320B.

LEFT MEMORY SEQUENCER

The Left Memory Sequencer (LMS) produces gate pulses that control the sequence of data transfers in the Left Memory (diagram 15). The LMS and its counterpart, the Right Memory Sequencer, control the operation of the entire 5223 memory. Figure 4-19 shows the timing of a typical write-data-to-memory cycle. The LMS consists of the following circuitry:

1. Left Memory Sequencer, Block T
2. Sequencer Buffer-Selector, Block U
3. Left CH 1/CH 2 Hold Off Generator, Block X
4. Power-Up Left Sequencer Reset, Block Z
5. Left Write-Command Controller, Block AA
6. Left Memory-Load Controller, Block DD
7. Left Memory Record-Full Detector, Block FF

LEFT MEMORY SEQUENCER, BLOCK T

The Left Memory Sequencer (LMS) produces gate pulses that control the sequence of data transfers in the Left Memory. The LMS consists of a gated oscillator, U1320B and U400C; an up-counter, U700; decoding logic, U1100; a control gate, U1000; an RS FF, U900; and a circuit that produces the Write Clock Left pulse, U800A, B, C, D and U710B.

A high-logic level on the Qualified Write Cmd Left line clocks a high-logic level into FF U1320B. The high-logic level on the Left Controller Active line enables oscillator U400C, which operates at about 10 MHz. Oscillations from U400C increment binary counter U700. Three outputs of the counter and the oscillator waveform operate the decoding logic, U1100, which sends its output to FF U900 via control gate U1000. After oscillator U400C has generated five cycles, U700's 2^2 output activates U1100D, which in turn activates U1000C. The output of U1000C resets section 4 of quad FF U900, which asserts a low-logic level on its 4Q output. This low-logic level, from U900 pin 13, causes three events:

1. It sets the 3Q, 2Q, and 1Q stages of U900 to high-logic level outputs.

2. It disables control gate U1000, and

3. It resets FF U1320B and counter U700.

Figure 4-20 illustrates this timing.

As soon as C1110 discharges to +1.3 V the Q_A section of U900 is set, and the sequence ends.

While U700 is counting between one and five, one of its output lines is always at a high-logic level. Via U800A, B, C, and D, U710B is always active and asserting a high-logic level on the Write Clock line. When U900 resets counter U700, its four output lines are all at low-logic levels and U710B is disabled—it then produces a low-logic level on the Write Clock Left line.

Variable capacitor C801 adjusts the operating frequency of oscillator U400C. The correct operating frequency is one that causes the duration of the Write Clock Left pulse to be 560 ns.

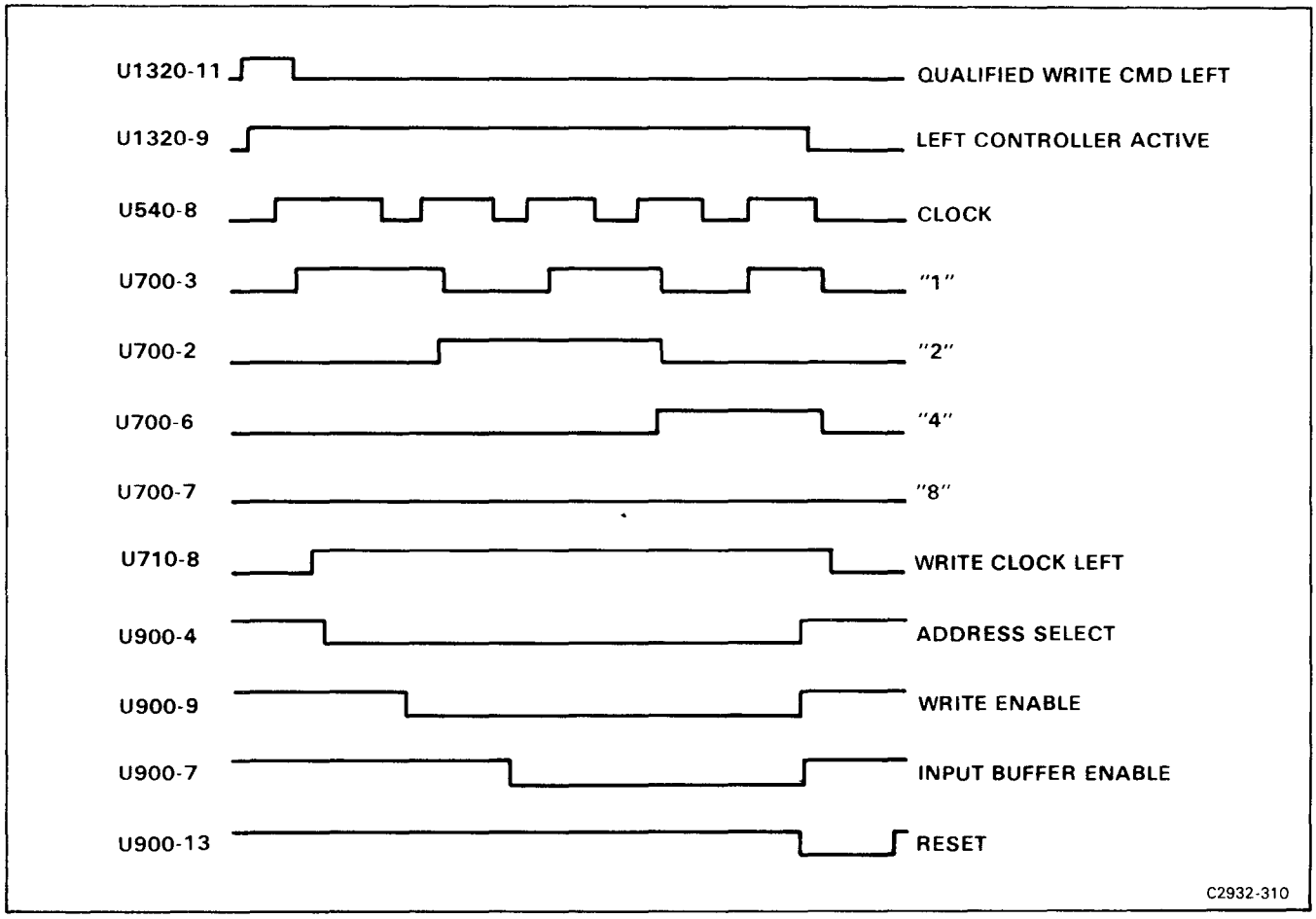


Figure 4-20. Timing of Left Memory Sequencer.

SEQUENCER BUFFER-SELECTOR, BLOCK U

The Sequencer Buffer-Selector (SBS) generates signals that control the memory's input and output buffers (blocks JJ and KK on diagram 15) and gates address data to the memories. The SBS consists of U440A, U820A, U920 and U930.

When the Save Left line is at low-logic level U800F applies a high-logic level to the pin 13 input of U440A. The pin 1 and 2 inputs of U440A receive the "qualified" Page Pulse, via FF U1300A (on pin 1), and Page Pulse directly (on pin 2). The "qualified" Page Pulse is the high-logic level that U1300A produces at its pin 6 output if its D input is at a low-logic level (Left Page Full) when Page Pulse clocks it. Because the Page Pulse signal is about 270 ns duration, the output of U1300A will reach and activate U440A. The high-logic level output of U440A clocks FF U820A, which responds by changing states. (Flip-flop U820B is the "page flip-flop," whose output determines whether the SBS will cause the left page A memory to receive data (write) while data from left page B is being read, or vice versa.) The Q output of U820A goes to the B inputs of sections 2 and 4 of multiplexer U920 and to U930B and C. The $\overline{Q}$ output of U820A goes to the B input of section 3 of U920 and to U930A and D. The Q output of FF U600B controls multiplexer U920; a high-logic level selects the B inputs when the 5223 is in normal operation. When the 5223 is in Roll mode the low-logic level from U600B selects U920A's A inputs. That is, Roll involves only page A of the memory. Multiplexer U920 produces the $\overline{LA}$ Out, $\overline{LB}$ Out, and Adrs Sel L signals and U930 produces the $\overline{LA}$ In, $\overline{LB}$ In, $\overline{WE}$ Mem LA and $\overline{WE}$ Mem LB signals. The $\overline{LA}$ and $\overline{LB}$ In and Out signals activate the left page A and B memory input and output buffers. The $\overline{WE}$ Mem LA and LB signals are Write Enable signals for pages A and B of the left memory.

LEFT CH 1/CH 2 HOLD OFF GENERATOR, BLOCK X

The Left Channel 1/Channel 2 Holdoff Generator produces the L $\overline{Holdoff}$ signal for the Left Write-

Command Controller, block AA. The generator consists of gates U1010A, U830C and D; inverter U1210D; and FF U810A.

In dual-channel-alternate operation, two complete real-time sweeps are needed to fill one page of memory. After the first sweep, Gated Stop L clocks FF U810A, whose $\overline{Q}$ output disables U1110A. When disabled, U1110A does not produce Qualified Write Cmd Left pulses. The next transition of the G 1/$\overline{2}$ Left Mux signal will reset FF U810A, which will enable U1110A and permit a second series of Qualified Write Cmd Left pulses. When a page of the memory is full, U1200B (block DD) causes a low-logic level on the Left Page Full line, which sets FF U810A and starts the L Holdoff signal.

Gate U830D will pass the L Holdoff signal only when its pin 13 input is at a low-logic level, which requires:

1. a low-logic level on GA10, and

2. a low-logic level on the SS Mode line.

If the time base is set to single-sweep mode, it will cause a high-logic level on the SS Mode line. This high-logic level will activate U830C, whose output will activate U830D and disable the holdoff circuit.

POWER-UP LEFT SEQUENCER RESET, BLOCK Z

The Left Power-Up Sequencer Reset circuit is intended to reset the Left Memory Sequencer when the 5223 is turned on. It consists of FF U810B.

If counter U700, in the Left Memory Sequencer, stops at any count except 0000 (low-logic levels on its four outputs) it will activate U710B. In this case U710B will assert a high-logic level on the Write Clock Left line, which is connected to U810B's D input. A high-logic level on the G Write Left line will clock the high-logic level from Write Clock Left into U810B, which will produce a low-logic level on its $\overline{Q}$ output (Left Reset). The low-logic level on Left Reset will activate U1200D, whose output will reset counter U700 in the Left Memory Sequencer.

LEFT WRITE-COMMAND CONTROLLER, BLOCK AA

The Left Write-Command Controller (LWCC) produces the Qualified Write Cmd Left signal for the Left Memory Sequencer (block T) and the Blanking Source Generator (block J). Any of three conditions will disable Qualified Write Cmd Left signals, as follows:

1. when the memory page is full, or

2. when the holdoff circuit is active, or

3. if the system is in roll mode and a display is saved.

The LWCC consists of U1110A.

LEFT MEMORY-LOAD CONTROLLER, BLOCK DD

The Left Memory-Load Controller (LMLC) produces control signals for the Left Register Controller (L Ch 1 + L Ch 2 Left), the Sequencer Buffer-Selector, and the Left Write-Command Controller. The LMLC consists of gates U1020C, U1010B, U360A and B, U1500A and U1200B; and FFs U1310A and B, and U1300A.

In conventional (non-Roll-mode) operation, the LMLC will determine when a memory page is full and will produce the Left Page Full pulse. When the next Page Pulse occurs, FF U1300A will produce a high-logic level on its pin 6 output. The high-logic level from U1300A and the Page Pulse will activate U440A (if the Saved Left line is at a high-logic level), which will clock FF U820B.

If the system is in dual-channel-alternate mode, two real-time sweeps are needed to fill a page of memory. In this mode, the A10 line will be at a high-logic level and two Write Left Adrs pulses must occur before the LMLC produces a Left Page Full pulse.

When the system is in dual-channel-chop mode, only one real-time sweep is needed to fill a memory page. The A10 line will be at a low-logic level and the first Write Left Adrs pulse will cause the LMLC to produce a Left Page Full pulse.

In Roll mode, U920 produces a Write Left Adrs pulse for each Qualified Write Cmd Left pulse. This means that, in Roll mode, there will be one L Ch 1 + L Ch 2 Left pulse for each Qualified Write Cmd Left pulse. Page FF U820B is held reset, selecting only Page A control signals for the memory. A low-logic level from U600B pin 9 disables the left page full FFs, U1310A and B.

LEFT MEMORY RECORD-FULL DETECTOR, BLOCK FF

The Left Memory Record-Full Detector (LMRFD) produces a Gated Stop L signal for the Sequencer Buffer-Selector, block U. The LMRFD consists of counter U1610, FF U1410B, and gates U450B and U330A.

Write Clock Left pulses increment counter U1610. When the number in U1610 reaches 1024 (2^{10}), U1610 produces a high-logic level on its 2^{10} output which clocks FF U1410B. The output of U1410B resets U1610 and activates U450B. Gate U450B's output enables U330A. A G Stop Left pulse can now activate U330A, whose output, via blocks U and DD, produces a low-logic level at the "Reset" input of U1410B. Flip-flop U1410B resets in response to this negative going input, producing a low-logic level that: a. allows U1610 to resume incrementing in response to Write Clock Left pulses, and b. turns off U450B, which disables U330A.

If the time base is in single-sweep mode, it will assert a high-logic level on the SS Mode line. The high-logic level on SS Mode will activate U450B, whose output will enable U330A. The next G Stop Left will activate U330A and cause a Gated Stop L signal.

RIGHT MEMORY SEQUENCER

The Right Memory Sequencer (RMS) produces gate pulses that control the sequence of data transfers in the Right Memory (diagram 15). The RMS consists of the following circuitry:

1. Right Memory Sequencer, Block V
2. Sequencer Buffer-Selector, Block W
3. Right CH 1/CH 2 Hold Off Generator, Block Y
4. Right Write Command Controller, Block BB
5. Power-Up Right Sequencer Reset, Block CC
6. Right Memory Load Controller, Block EE
7. Right Memory Record Full Detector, Block GG

RIGHT MEMORY SEQUENCER, BLOCK V

The Right Memory Sequencer (RMS) produces gate pulses that control the sequence of data transfers in the Right Memory.

The RMS consists of a gated oscillator, U820A and U400A; an up-counter, U510; decoding logic, U720; a control gate, U730; an RS FF, U640; and a circuit that produces the Write Clock Right pulse, U610A, B. C, D, and U710A.

A high-logic level on the Qualified Write Cmd Right line clocks a high-logic level into FF U820A. The high-logic level on the Right Controller Active line enables oscillator U400A, which operates at about 10 MHz. Oscillations from U400A increment binary counter U510. Three outputs of the counter and the oscillator waveform operate the decoding logic, U720, which sends its output to FF U640 via control gate U730. After oscillator U400A has generated five cycles, U510's 2^2 output activates U720B, which in turn activates U730B. The output of U730B resets section 2 of quad FF U640, which asserts a low-logic level on its 2Q output. This low-logic level, from U640 pin 7, causes three events:

1. It sets the 1Q, 3Q, and 4Q stages of U640 to high-logic levels.

2. It disables control gate U730, and

3. It resets FF U820A and counter U510.

Figure 4-21 illustrates this timing.

As soon as C550 discharges to +1.3 V the 2Q section of U640 is set, and the sequence ends.

While U510 is counting between one and five, one of its output lines is always at a high-logic level. Via U610A, B, C, and D, U710A is always active and asserting a high-logic level on the Write Clock Right line. When U640 resets counter U510, its four output lines are all at low-logic levels and U710A is disabled—it then produces a low-logic level on the Write Clock Right line.

Variable capacitor C800 adjusts the operating frequency of oscillator U400A. The correct operating frequency is one that causes the duration of the Write Clock Right pulse to be 560 ns.

SEQUENCER BUFFER-SELECTOR, BLOCK W

The Sequencer Buffer-Selector (SBS) generates signals that control the memory's input and output buffers (blocks UU and VV on diagram 16) and gates address data to the memories. The SBS consists of U440B, U620A, U630 and U650.

When the Save Right line is at low-logic level U210A applies a high-logic level to the pin 5 input of U440B. The pin 4 and 3 inputs of U440B receive the "qualified" Page Pulse via FF U1300B (on pin 4) and Page Pulse directly (on pin 3). The "qualified" Page Pulse is the high-logic level that U1300B produces at its pin 8 output if its D input is at a low-logic level ($\overline{\text{Right Page Full}}$) when Page Pulse clocks it. Because the Page Pulse signal is about 270 ns in duration, the output of U1300B will reach and activate U440B. The high-logic level output of U440B clocks FF U620A, which responds by changing states. (Flip-flop U620B is the "page flip-flop", whose output determines whether the SBS will cause the right page A memory to receive data (write) while data is being read

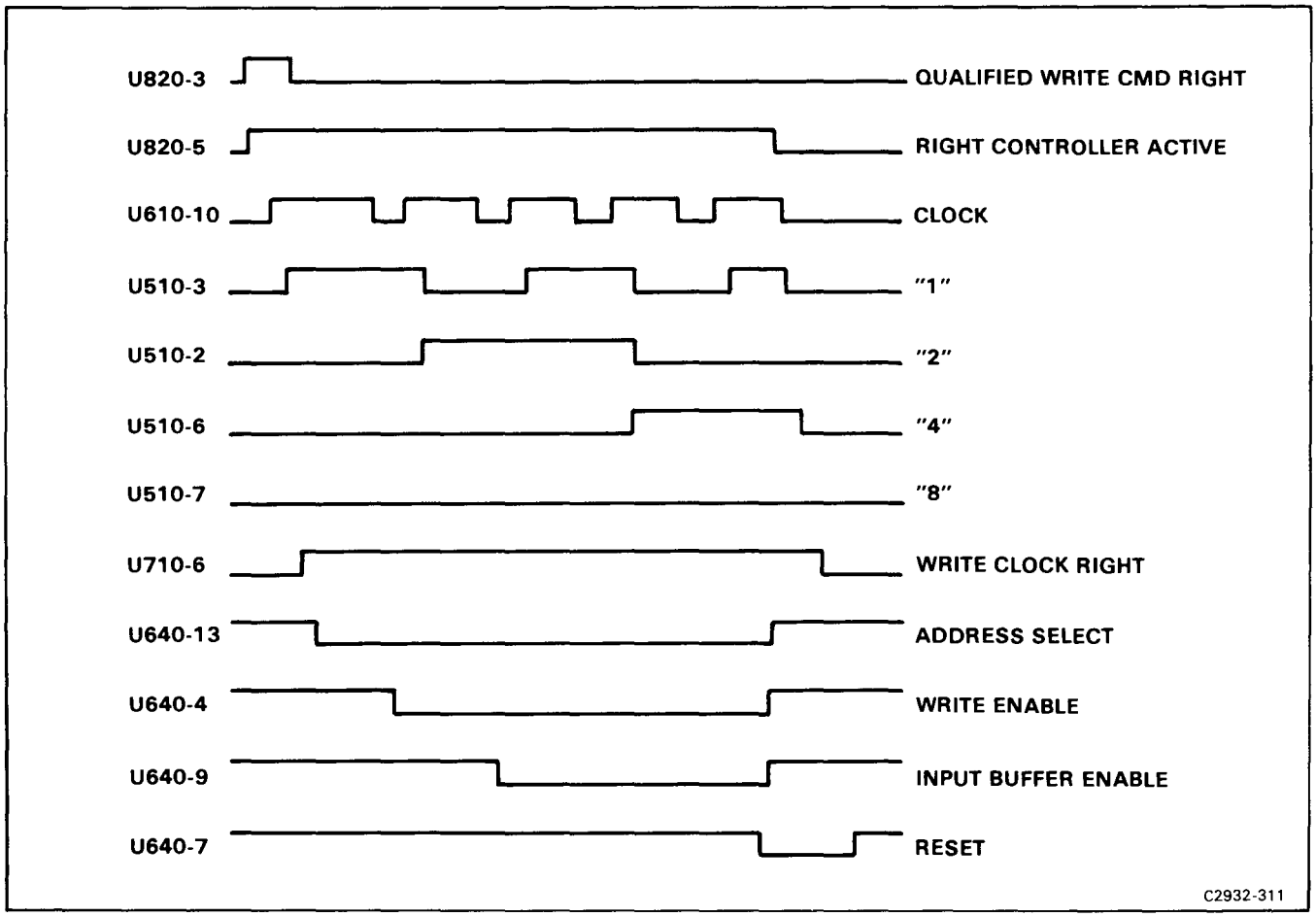


Figure 4-21. Timing of Right Memory Sequencer.

from the right page B memory, or vice versa.) The Q output of U620A goes to the B inputs of sections 2 and 4 of multiplexer U630 and to U650D and C. The $\overline{Q}$ output of U620A goes to the B input of section 3 of U630 and to U650A and B. The Q output of FF U300A controls multiplexer U630; a high-logic level selects the B inputs when the 5223 is in normal operation. When the 5223 is in Roll mode the low-logic level from U300A selects U630's A inputs. That is, Roll involves only page A of the memory.

Multiplexer U630 produces the $\overline{RA}$ Out, $\overline{RB}$ Out, and Adrs Sel R signals and U650 produces the $\overline{RA}$ In, $\overline{RB}$ In, $\overline{WE}$ Mem RA and $\overline{WE}$ Mem RB signals. The $\overline{RA}$ and $\overline{RB}$ In and Out signals activate the Right page A and B memory input and output buffers. The $\overline{WE}$ Mem RA and RB signals are Write Enable signals for pages A and B of the Right memory.

RIGHT CH 1/CH 2 HOLD OFF GENERATOR, BLOCK Y

The Right Ch 1/Ch 2 Hold Off Generator produces the R Holdoff signal for the Right Write-Command Controller, block BB. The generator consists of gates U1450B, U830A and B; inverter U540F; and FF U320A.

In dual-channel-alternate operation, two complete real-time sweeps are needed to fill one page of memory. After the first sweep. Gated Stop R clocks FF U320A, whose $\overline{Q}$ output disables U1110B. When disabled, U1110B does not produce Qualified Write Cmd Right pulses. The next transition of the G $1/\overline{2}$ Right Mux signal will reset FF U320A, which will enable U1110B, and permit a second series of Qualified Write Cmd Right pulses. When a page of the memory is full, U1200C (block EE) causes a low-logic level on the $\overline{\text{Right Page Full}}$ line, which sets FF U320A and starts the R $\overline{\text{Holdoff}}$ signal.

Gate U830B will pass the R $\overline{\text{Holdoff}}$ signal only when its pin 4 input is at a low-logic level, which requires:

1. a low-logic level on GB10, and

2. a low-logic level on the SS Mode line.

If the time base is set to single-sweep mode, it will cause a high-logic level on the SS Mode line. This high-logic level will activate U830A, whose output will activate U830B and disable the holdoff circuit.

RIGHT WRITE COMMAND CONTROLLER, BLOCK BB

The Right Write-Command Controller (RWCC) produces the Qualified Write Cmd Right for the Right Memory Sequencer (block V) and the Blanking Source Generator (block J). Any of three conditions will stop Qualified Write Cmd Right signals, as follows:

1. when the memory page is full, or,

2. when the holdoff circuit is active, or

3. if the system is in roll mode and a display is saved.

The LWCC consists of U1110B.

POWER-UP RIGHT SEQUENCER RESET, BLOCK CC

The Right Power-Up Sequencer Reset circuit is intended to reset the Right Memory Sequencer when the 5223 is turned on. It consists of FF U620B.

If counter U510, in the Right Memory Sequencer, stops at any count except 0000 (low-logic levels on its four outputs) it will activate U710A. In this case U710A will assert a high-logic level on the Write Clock Right line, which is connected to U620B's D input. A high-logic level on the G Write Right line will clock the high-logic level from Write Clock Right into U620B, which will produce a low-logic level on its $\overline{Q}$ output ($\overline{\text{Right Reset}}$). The low-logic level on $\overline{\text{Right Reset}}$ will activate U410C, whose output will reset counter U510 in the Right Memory Sequencer.

RIGHT MEMORY LOAD CONTROLLER, BLOCK EE

The Right Memory-Load Controller (RMLC) produces control signals for the Right Register Controller ($\overline{\text{L Ch 1 + L Ch 2 Right}}$), the Sequencer Buffer-Selector, and the Right Write-Command Controller. The RMLC consists of gates U1400B and C, U495B, U1200C, U1500B, U1550A; and FFs U910A and B, and U1300B.

In conventional (non-Roll-mode) operation, the RMCC will determine when a memory page is full and will produce the $\overline{\text{Right Page Full}}$ pulse. When the next Page Pulse occurs, FF U1300B will produce a high-logic level on its pin 8 output. The high-logic level from U1300B and the Page Pulse will activate U440B (if the $\overline{\text{Saved Right}}$ line is at a high-logic level), which will clock FF U620A.

If the system is in dual-channel-alternate operation, two real-time sweeps are needed to fill a page of memory. In this mode, the $\overline{\text{B10}}$ line will be at a high-logic level and two Write Right Adrs pulses must occur before the RMLC produces a $\overline{\text{Right Page Full}}$ pulse.

When the system is in dual-channel-chop mode, only one real-time sweep is needed to fill a memory page. The $\overline{\text{B10}}$ line will be at a low-logic level and the first Write Right Adrs pulse will cause the RMLC to produce a $\overline{\text{Right Page Full}}$ pulse.

In Roll mode, U630 produces a Write Right Adrs pulse for each Qualified Write Cmd Right pulse. This means that, in Roll mode, there will be one $\overline{\text{L Ch 1 + L Ch 2 Right}}$ pulse for each Qualified Write Cmd Right pulse. Page FF U620A is held reset, selecting only Page A control signals for the memory. A low-logic level from U300A pin 5 disables the left page full FFs, U910A and B.

RIGHT MEMORY RECORD FULL DETECTOR, BLOCK GG

The Right Memory Record-Full Detector (RMRFD) produces a Gated Stop R signal for the Sequencer Buffer-Selector, block W. The RMRFD consists of counter U1510, FF U1410A, and gates U450C and U330D.

Write Clock Right pulses increment counter U1510. When the number in U1510 reaches 1024 (2^{10}), U1510 produces a high-logic level on its 2^{10} output which clocks FF U1410A. The output of U1410A resets U1510 and activates U450C. Gate U450C's output enables U330D. A G Stop Right pulse can now activate U330D, whose output, via blocks W and EE, produces a low-logic level at the "Reset" input of U1410A. Flip-flop U1410A resets in response to the negative-going input, producing a low-logic level that: a. allows U1510 to resume incrementing in response to Write Clock Right pulses, and b. turns off U450C, which disables U330D.

If the time base is in single-sweep mode, it will assert a high-logic level on the SS Mode line. A high-logic level on SS Mode will activate U450C, whose output will enable U330D. The next G Stop Right will activate U330D and cause a Gated Stop R signal.

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LEFT MEMORY

The Left Memory (LM) stores data that represents the crt display from the left plug-in. The LM consists of the following circuits:

1. Left Page A Buffered Memory, Block JJ
2. Left Page B Buffered Memory, Block KK
3. Left Page A Address Multiplexer, Block MM
4. Left Page B Address Multiplexer, Block NN
5. Left Start-Sweep Register, Block OO
6. Left Read Counter, Block PP
7. Left Register Controller, Block QQ
8. Left Write Address Normalizer, Block RR
9. Left Record Sorting, Block SS
10. Left Write Counter, Block PPP

LEFT PAGE A BUFFERED MEMORY, BLOCK JJ

The Left Page A Buffered Memory (LPABM) can store data from Data Bus GA and transfer data from memory to Data Bus D. The LPABM consists of U560, U660, U740, U840, U940, U760 and U860.

The 10 bits on Address Bus J specify the memory locations where data will be "written to" or "read from" in memory elements U740, U840 and U940. The CS and WE inputs (Chip Select and Write Enable) control the memory as follows:

CS and WE both at low-logic levels—memory receives data ("write"),

CS at a low-logic level and WE at a high-logic level—memory sends data ("read").

This shows that the $\overline{WE}$ Mem LA line controls the write-read action of the memory.

The G Adrs Sel L line controls the Page A and B Address Multiplexers and Buffered Memories.

When G Adrs Sel L is at a low-logic level, it causes both Page A and Page B Address Multiplexers to route data from their A inputs to their outputs. The Page A Address Multiplexer then selects the write address from Address Bus N, and applies it to the Page A Buffered Memory via Address Bus J. The Page B Address Multiplexer selects the read address from Address Bus O, and applies it to the Page B Buffered Memory via address Bus K. Synopsis: When G Adrs Sel L is at a low-logic level, Page A writes new data and Page B reads data out.

When G Adrs Sel L is at a high-logic level, the Page A and Page B Address Multiplexers route data from their B inputs to their outputs. In this situation Page A reads data out, and Page B writes new data.

When data from Data Bus GA is to be stored in memory (written), a low-logic level on G $\overline{LA}$ In activates buffers U760 and U860, which pass the data from the GA bus to the I/O terminals of memories U740, U840 and U940. Low-logic levels on $\overline{G\ Chip\ Sel\ L}$ and $\overline{WE}$ Mem LA will store the GA bus data in the location specified by Address Bus J.

When the memory data is to be read out, the $\overline{WE}$ Mem LA line will be at a high-logic level, which will cause the memory to place data, from the location specified by Address bus J, on its output. A low-logic level on the G $\overline{LA}$ Out line will enable buffers U560 and U660 to place the memory data on Data Bus D.

LEFT PAGE B BUFFERED MEMORY, BLOCK KK

The Page B Buffered Memory (PBBM) can store data from Data Bus GA and transfer data from memory to Data Bus D. The PBBM consists of U570, U670, U770, U870, U750, U850 and U950.

The 10 bits on Address Bus K specify the memory locations where data will be "written to" or "read from" in memory elements U750, U850 and U950. The CS and WE inputs control the memory as follows:

CS and WE both at low-logic levels—receive data ("write"),

CS at a low-logic level and WE at a high-logic level—send data ("read").

This shows that the $\overline{WE}$ Mem LB line controls the write-read action of the memory.

The G Adrs Sel L line controls the Page A and B Address Multiplexers and Buffered Memories.

When G Adrs Sel L is at a low-logic level, it causes both Page A and Page B Address Multiplexers to route data from their A inputs to their outputs. The Page A Address Multiplexer then selects the write address from Address Bus N, and applies it to the Page A Buffered Memory via Address Bus J. The Page B Address Multiplexer selects the read address from Address Bus O, and applies it to the Page B Buffered Memory via address Bus K. Synopsis: When G Adrs Sel L is at a low-logic level, Page A writes new data and Page B reads data out.

When G Adrs Sel L is at a high-logic level, the Page A and Page B Address Multiplexers route data from their B inputs to their outputs. In this situation Page A reads data out, and Page B writes new data.

When data from Data Bus GA is to be stored in memory ("written"), a low-logic level on G $\overline{LB}$ In activates buffers U770 and U870, which pass the data from the GA bus to

the I/O terminals of memories U750, U850 and U950. A low-logic level on $\overline{WE}$ Mem LB will store the GA bus data in the location specified by Address Bus K.

When the memory data is to be read, the $\overline{WE}$ Mem LB line will be at a high-logic level. This will cause the memory (U750, U850 and U950) to place data, from a location specified by Address Bus K, on its output. A low-logic level on the G $\overline{LB}$ Out line will enable buffers U570 and U670 to place the memory data on Data Bus D.

LEFT PAGE A ADDRESS MULTIPLEXER, BLOCK MM

The Page A Address Multiplexer (PAAM) selects an address from Address Bus N or Address Bus O and places it on Address Bus J. The PAAM consists of U1040, U1140 and U1240.

The 10 bits on Address Bus N connect to the A inputs of multiplexers U1040, U1140 and U1240, and Address bus O's 10 bits connect to the B inputs. The G Adrs Sel L line controls U1040, U1140 and U1240; a low-logic level there selects the A inputs (Address Bus N) and a high-logic level selects the B inputs (Address Bus O).

LEFT PAGE B ADDRESS MULTIPLEXER, BLOCK NN

The Page B Address Multiplexer (PBAM) selects an address from Address Bus N or Address Bus O and places it on Address Bus K. The PBAM consists of U1050, U1150 and U1250.

The 10 bits of Address Bus N connect to the B input of U1050, U1150 and U1250; and Address Bus O's 10 bits connect to their A inputs. The G Adrs Sel L line controls U1050, U1150 and U1250; a low-logic level there selects the A inputs (Address bus O) and a high-logic level selects the B inputs (Address Bus N).

LEFT START-SWEEP REGISTER, BLOCK OO

The Left Start-Sweep Register (LSSR) will store up to four 10-bit words from address Bus N. The words represent the memory locations where the memory sweep ended. It also stores the Left $\overline{\text{Format Scrambled}}$ and Left $\overline{\text{Format L•R•100}}$ μsec bits for Option 10. The LSSR consists of U1340, U1440, U1540, U540E and U1640E.

The storage elements in the LSSR, U1340, U1440 and U1540, are 4 × 4 register files. The four sets of four cells in each element can each accept and store address data (be "written") and have those addresses "read" out. The write and read operations can take place simultaneously. Both write and read sections have three control lines, $\overline{Enable}$, Address 1 and Address 2. A low-logic level on the $\overline{Enable}$ input allows the section to accept or send addresses. The four combinations of the two address lines designate the specified cell to be written or read.

The write $\overline{Enable}$ inputs receive 50 ns Load L pulses from U1210C. The write address lines (A_1 and A_2) receive the $\overline{\text{G Adrs Sel L}}$ line from U1640E (which selects pairs of addresses for page A or B) and the output of U1450D (which selects Ch 1 or Ch 2 within the pair), respectively.

The read $\overline{Enable}$ inputs are connected to ground, causing the register to immediately place designated addresses on address Bus W. The A_1 and A_2 read address lines are the G Mem Ch 1/Ch 2 Sel Line and G Adrs Sel L lines, respectively. Figure 4-22 shows the timing of a memory-write operation, with the 5223 in Roll mode and using a dual-channel amplifier.

LEFT READ COUNTER, BLOCK PP

The Left Read Counter (LRC) accepts a 10-bit number from address Bus W, counts G Read Clock pulses and supplies data to Address Bus O. The LRC consists of U1030, U1130 and U1230.

A low-logic level on the $\overline{\text{G Adrs Load L}}$ line loads data from the W0 through W9 lines into counters U1030, U1130 and U1230. Positive transitions on the G Read Clock line cause the counter to increment. A high-logic level on the G Read Adrs Ctr Clr L line resets the counter to zero for test purposes. The contents of the LRC is the input to Address Bus O, which is used to read the Left Page A or B Buffered Memory.

LEFT REGISTER CONTROLLER, BLOCK QQ

The Left Register Controller (LRC) produces control signals for the write enable and write select A_2 inputs of the Left Start Sweep Register. The LRC consists of U1020D, U1520C, U1450A, U1210C, U1220B, U1320A and U1450D.

Gate U1020D, inverter U1520C and associated parts form a one-shot that generates a 200 ns pulse in response to the input trigger pulse ($\overline{\text{L Ch 1 + L Ch 2 Left}}$). The transitions of the pulse from U1520C activate exclusive-OR gate U1450A, which generates a positive-going 50 ns pulse for each transition of the input pulse. Inverter U1210C applies negative-going 50 ns pulses to the clock input of FF U1320A and to the write enable inputs of the Left Start-Sweep Register.

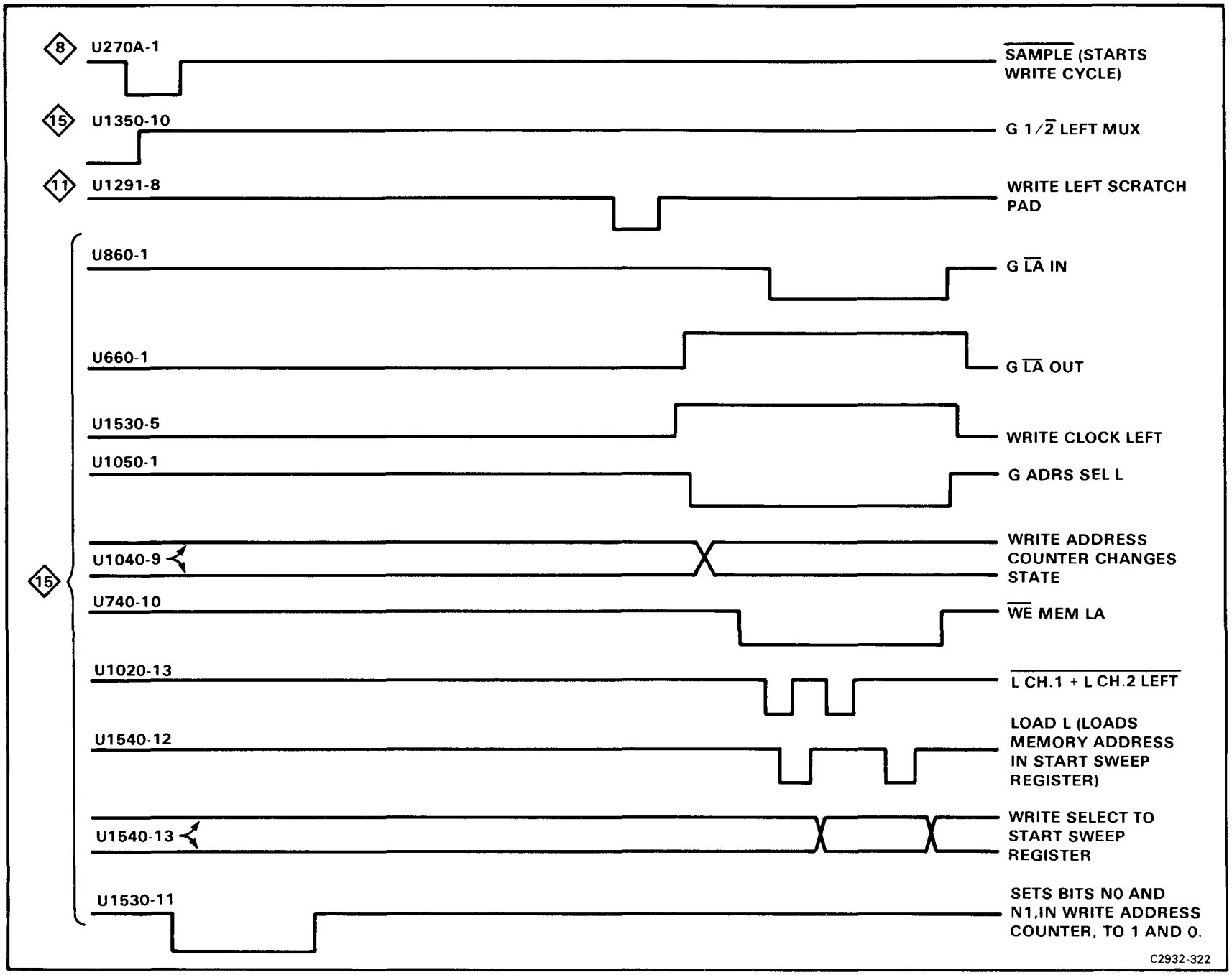

Figure 4-22. Timing of write-data-to-memory operation using a dual-channel amplifier in the left plug-in compartment, with 5223 Roll mode.

When the system is in dual-channel-alternate mode, two distinct addresses will be stored in the Channel 1 and Channel 2 locations of the Start Sweep Register.

When the system is in dual-channel-chop or single-channel mode, the same address will be stored in the Channel 1 and Channel 2 locations of the Start Sweep Register.

The positive-going trailing edges of the 50 ns pulses clock FF U1320A. Gate U1220B controls the operation of U1320A; a high-logic level at U1220B's pin 4 input (from U1120A) permits U1320A to operate in "toggle" mode. Gate U1120A will assert a high-logic level on U1220B pin 4 when GA10 or Chop is at a high-logic level. The high-logic level that enables U1220B causes a high-logic level, via U1210A and U1120C, at the pin 12 input of exclusive-OR gate U1450D. Gate U1450D then inverts the output of U1320A and applies it to the A_2 write address inputs of the Left Start-Sweep Register. If U1120A is not applying a high-logic level to U1220B, the output of FF U1320A stays at a high-logic level.

The negative-going 50 ns pulses from U1210C enable the write inputs of the Left Start-Sweep Register.

LEFT WRITE ADDRESS NORMALIZER, BLOCK RR

The Left Write-Address Normalizer (LWAN) controls the two least-significant bits of the write-address bus (bits N0 and N1) so that they match the Interface Board's sequence of sampling. The LWAN consists of U1350B; U1420; U1120A, B, C, and D; U1020B; and U1210A, B, and F.

Multiplexer U1420 receives the N0 and N1 bits from U1530 and the output of one-shot U1350B. Gate U1020B controls U1420. Either a low-logic level on Chop or a high-logic level on GA10 activates U1020B, whose high-logic level output causes U1420 to connect its B inputs to its outputs. This puts the 2^0 and 2^1 outputs of U1530 on Address Bus N in their original order (N0=2^0 and and N1=2^1).

When the 5B25N is in Chopped mode and a dual-channel vertical plug-in is in use, the GA 10 line will be at a low-logic level and the Chop line will be at a high-logic level. Inverter U1210F applies a high-logic level to U1020B pin 5, which, with the high-logic level on the Chop line, disables U1020B.

When disabled, U1020B applies a low-logic level to the pin 1 input of U1420, causing it to connect its A inputs to its outputs. Section 2 of U1420 now puts U1530's 2^0 output on the N1 line of address Bus N and section 3 applies U1530's 2^1 output to the N0 line via U1120D and U1120B. (A high-logic level from U1120A, activated by the $\overline{\text{Chop}}$ signal from U1210B, enables U1120D and U1120B.)

Also, when the operating mode is chopped, dual-channel, a positive-going transition on the G $1/\overline{2}$ Left Mux line will trigger one-shot U1350B. The negative-going output of U1350B will pass through the "1" section of U1420 and load the Left Write Counter to 2^3, nc; 2^2, nc; 2^1, 0; and 2^0, 1; which means that the 2^3 and 2^2 outputs do not change, the 2^1 output is 0 (a low-logic level), and the 2^0 output is 1 (a high-logic level).

When the 5B25N is in Chopped mode and a dual-channel vertical plug-in is in use, the output sequence of counter U1530 is normalized by U1420 so that the addressed locations to memory are as shown in Figure 4-23 with reference to the sampled data and markers coming into the memory.

The normalization process causes the Channel 1 data to be loaded into odd memory locations and Channel 2 data to be loaded into even memory locations.

When U1120A is activated, by a high-logic level on GA 10 or Chop, its high-logic level output has three effects, as follows:

1. It enables U1120D, which passes the output of U1420 section 3 to the N0 line.

2. Via U1210A, it asserts a low-logic level on the $\overline{\text{A10}}$ line.

3. It enables U1220B in the Left Register Controller, so that the address generated by U1220B, U1320A and U1450D will be alternated to the Left Start Sweep Register.

LEFT RECORD SORTING, BLOCK SS

The Left Record Sorting (LRS) circuit determines whether bit W0 or G Mem Ch $1/\overline{\text{Ch 2}}$ Sel L will be bit O0 on Address Bus O. The LRS consists of U1210E and U1220A, C and D.

Bit D10 indicates whether the data is stored as a single- or dual-channel record. A high-logic level on D10 means single-channel.

Bit D10 controls the LRS circuit. A high-logic level on D10 will enable U1220D, which will then pass the 2^0 output of U1230 to the O0 line of Address Bus O via

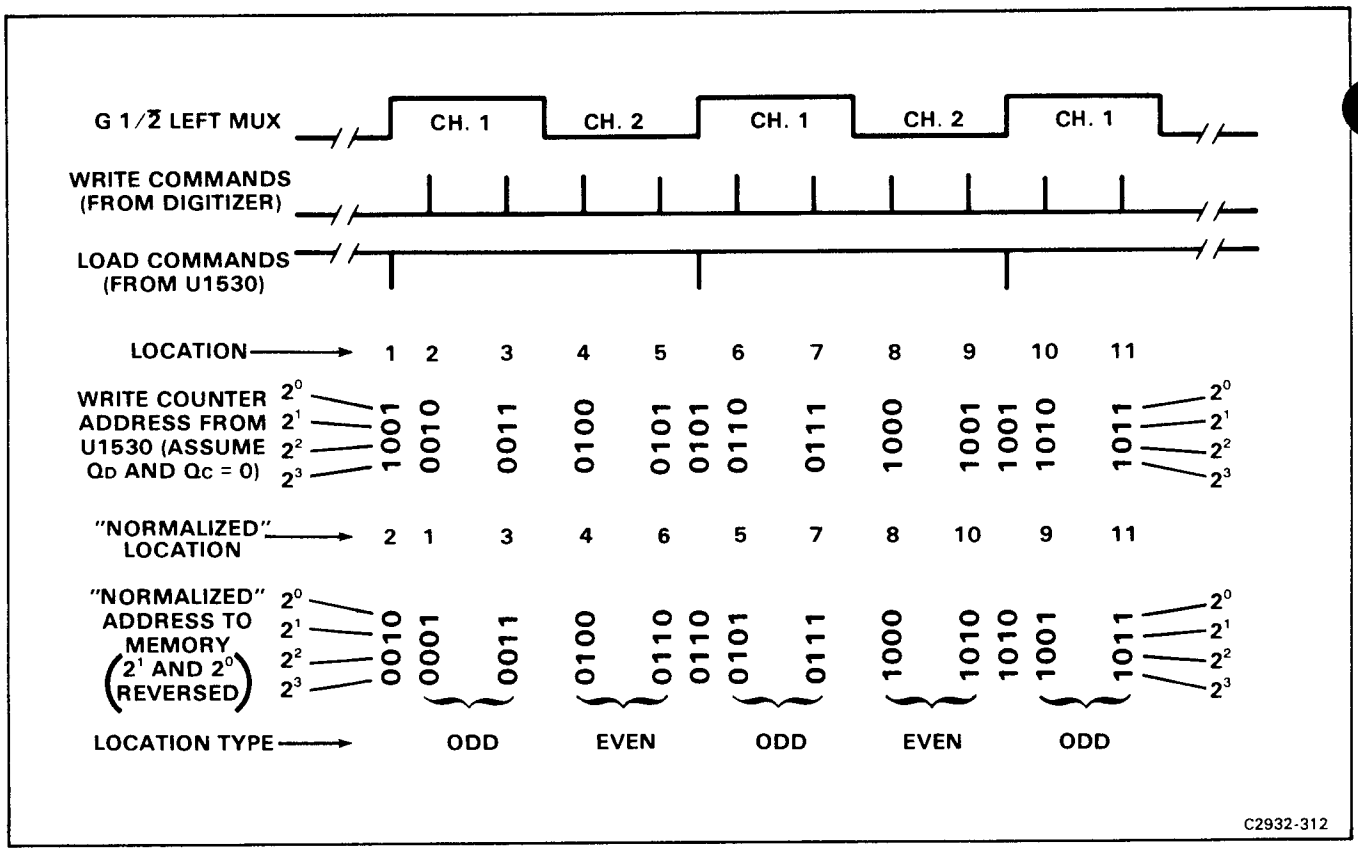

Figure 4-23. Reversal of 2^0 and 2^1 outputs of U1530 to "normalize" memory addresses when operating in "chop, dual-channel" mode.

U1220A. (The pin 2 input of U1220A is at a high-logic level because the high-logic level on D10 activated U1210E and U1220C.)

A low-logic level on D10 disables U1220D and enables U1220C, via U1210E, to pass the G Mem Ch 1/$\overline{\text{Ch 2}}$ Sel L signal to the O0 line of Address Bus O.

LEFT WRITE COUNTER, BLOCK PPP

The Left Write Counter (LWC) counts Write Clock Left pulses and supplies a 10-bit number to the Left Start Sweep Register and to the Page A and Page B Address Multiplexers via Address Bus N. The LWC consists of U1330, U1430 and U1530.

Write Clock Left pulses from the Left Memory Sequencer increment the LWC. The 10 sections of U1530, U1430 and U1330 furnish the N0 through N9 bits to Address Bus N.

When the 5223 has a dual-channel vertical amplifier and the time-base is in chopped mode, U1420 will connect its A inputs to the output. If a high-logic level occurs on G 1/2 Left Mux line, it will trigger one-shot U1350B. Via section 1 of U1420, U1350B's output will load U1530. Counter U1530 will be loaded as follows:

bit N0 - high,

bit N1 - low,

bit N2 - same as before load (Q_C^{-1}), and

bit N3 - same as before load (Q_D^{-1}).

For more details see Left Write-Address Normalizer discussion.

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RIGHT MEMORY

The Right Memory (RM) stores data that represents the crt display from the right plug-in. The RM consists of the following circuits:

1. Right Page A Buffered Memory, Block UU
2. Right Page B Buffered Memory, Block VV
3. Right Page A Address Multiplexer, Block YY
4. Right Page B Address Multiplexer, Block ZZ
5. Right Start-Sweep Register, Block AAA
6. Right Read Counter, Block BBB
7. Right Register Controller, Block CCC
8. Right Write Address Normalizer, Block DDD
9. Right Record Sorting, Block EEE
10. Right Write Counter, Block QQQ

RIGHT PAGE A BUFFERED MEMORY, BLOCK UU

The Right Page A Buffered Memory (RPABM) can store data from Data Bus GB and transfer data from memory to Data Bus C. The RPABM consists of U580, U680, U780, U880,U1060, U1160, and U1260.

The 10 bits on Address Bus L specify the memory locations where data will be "written to" or "read from" in memory elements U1060, U1160 and U1260. The CS and WE inputs (Chip Select and Write Enable) control the memory as follows:

CS and WE both at low-logic levels—receive data ("write"),

CS at a low-logic level and WE at a high-logic level—send data ("read").

This shows how the $\overline{WE}$ Mem RB line controls the write-read action of the memory.

The G Adrs Sel R line controls the Page A and B Address Multiplexers and Buffered Memories.

When G Adrs Sel R is at a low-logic level, it causes both Page A and Page B Address Multiplexers to route data from their A inputs to their outputs. The Page A Address Multiplexer then selects the write address from Address Bus N, and applies it to the Page A Buffered Memory via Address Bus L. The Page B Address Multiplexer selects the read address from Address Bus O, and applies it to the Page B Buffered Memory via Address Bus M. Synopsis: When G Adrs Sel R is at a low-logic level, Page A writes new data and Page B reads data out.

When G Adrs Sel R is at a high-logic level, the Page A and Page B Address Multiplexers route data from their B inputs to their outputs. In this situation Page A reads data out, and Page B writes new data.

When data from Data Bus GB is to be stored in memory (written), a low-logic level on G $\overline{RA}$ In activates buffers U780 and U880, which pass the data from the GB bus to the I/O terminals of memories U1060, U1160 and U1260. A low-logic level on the $\overline{WE}$ Mem RA line will store the GB Bus data in the location specified by Address Bus L.

When the memory data is to be read out, the WE Mem RB line will be at high-logic level, which will cause the memory to place data, from the location specified by Address bus L, on its output. A low-logic level on the G $\overline{RA}$ Out line will enable buffers U580 and U680 to place the memory data on Data Bus C.

RIGHT PAGE B BUFFERED MEMORY, BLOCK VV

The Right Page B Buffered Memory (RPBBM) can store data from Data Bus GB and transfer data from memory to Data Bus C. The RPBBM consists of U590, U690, U790, U890, U1070, U1170 and U1270.

The 10 bits on Address Bus M specify the memory locations where data will be "written to" or "read from" in memory elements U1070, U1170 and U1270. The CS and WE inputs control the memory as follows:

CS and WE both at low-logic levels—receive data ("write")

CS at a low-logic level and WE at a high-logic level—send data ("read").

This shows now the $\overline{WE}$ Mem LB line controls the write-read action of the memory.

When data from Data Bus GB is to be stored in memory ("written"), a low-logic level on G $\overline{RB}$ In activates buffers U790 and U890, which pass the data from the GB bus to the I/O terminals of memories U1070, U1170 and U1270. A low-logic level on $\overline{WE}$ Mem RB will store the GB Bus Data in the location specified by Address Bus M.

When the memory data is to be read, the $\overline{WE}$ Mem RB line will be at a high-logic level. This will cause the memory (U1070, U1170 and U1270) to place data, from a location specified by Address Bus M, on its output. A low-logic level on the G $\overline{RB}$ Out line will enable buffers U590 and U690 to place the memory data on Data Bus C.

RIGHT PAGE A ADDRESS MULTIPLEXER, BLOCK YY

The Right Page A Address Multiplexer (RPAAM) selects an address from Address Bus P or Address Bus Q and places it on Address Bus L. The RPAAM consists of U1360, U1460 and U1560.

The 10 bits on Address Bus P connect to the A inputs of multiplexers U1360, U1460 and U1560, and Address Bus Q's 10 bits connect to the B inputs. The G Adrs Sel R line controls U1360, U1460 and U1560; a low-logic level there selects the A inputs (Address Bus P) and a high-logic level selects the B inputs (Address Bus Q).

RIGHT PAGE B ADDRESS MULTIPLEXER, BLOCK ZZ

The Right Page B Address Multiplexer (RPBAM) selects an address from Address Bus P or Address Bus Q and places it on Address Bus M. The RPBAM consists of U1370, U1470 and U1570.

The 10 bits of Address Bus P connect to the B input of U1370, U1470 and U1570; and Address Bus Q's 10 bits connect to their A inputs. The G Adrs Sel R line controls U1370, U1470 and U1570; a low-logic level there selects the A inputs (Address Bus Q) and a high-logic level selects the B inputs (Address Bus P).

RIGHT START-SWEEP REGISTER, BLOCK AAA

The Right Start-Sweep Register (RSSR) will store up to four 10-bit words from address Bus P. The words represent the memory locations where the memory sweep ended. It also stores the Right $\overline{\text{Format Scrambled}}$ and Right $\overline{\text{Format}}$• L•R•100 μsec bits for Option 10. The RSSR consists of U1380, U1480, U1580, and U1640D.

The storage elements in the RSSR, U1380, U1480 and U1580, are 4 x 4 register files. The four sets of four cells in each element can each accept and store address data (be "written") and have those addresses "read" out. The write and read operations can take place simultaneously. Both write and read sections have three control lines, $\overline{\text{Enable}}$, Address 1 and Address 2. A low-logic level on the $\overline{\text{Enable}}$ input allows the section to accept or send addresses. The four combinations of the two address lines designate the specified cell to be written or read.

The write $\overline{\text{Enable}}$ inputs receive 50 ns Load R pulses from U1690B. The write address lines (A_1 and A_2) receive the $\overline{\text{G Adrs Sel R}}$ line from U1640D (which selects pairs of addresses for page A or B) and the output of U1495C (which selects Ch 1 or Ch 2 within the pair), respectively.

The read $\overline{\text{Enable}}$ inputs are connected to ground, causing the register to immediately place designated addresses on address Bus Z. The A_1 and A_2 read address lines are the G Mem Ch 1/$\overline{\text{Ch 2}}$ Sel R line and G Adrs Sel R lines, respectively.

RIGHT READ COUNTER, BLOCK BBB

The Right Read Counter (RRC) accepts a 10-bit number from Address Bus Z, counts G Read Clock pulses and supplies data to Address Bus Q. The RRC consists of U1391, U1491 and U1591.

A low-logic level on the $\overline{\text{G Adrs Load R}}$ line loads data from the Z0 through Z9 lines into counters U1391, U1491 and U1591. Positive transitions on the G Read Clock line cause the counter to increment. A high-logic level on the G Read Adrs Ctr Clr R line resets the counter to zero for test purposes. The contents of the RRC is the input to Address Bus Q, which is used to read the Right Page A or Page B Buffered Memory.

RIGHT REGISTER CONTROLLER, BLOCK CCC

The Right Register Controller (RRC) produces control signals for the write enable and write select A_2 inputs of the Right Start Sweep Register. The RRC consists of U1690D, U1640A, U1450C, U1690B, U1690A, U1691A and U1495C.

Gate U1690D, inverter U1640A and associated parts form a one-shot that generates a 200 ns pulse in response to the input trigger pulse ($\overline{\text{L Ch 1 + L Ch 2 Right}}$). The transitions of the pulse from U1640A activate exclusive-OR gate U1450C, which generates a positive-going 50 ns pulse for each transition of the input pulse. Inverter U1690B applies negative-going 50 ns pulses to the clock input of FF U1691A and to the write enable inputs of the Right Start-Sweep Register.

When the system is in dual-channel-alternate operation, two distinct addresses will be stored in the Channel 1 and Channel 2 locations of the Start-Sweep Register.

When the system is in dual-channel-chop or single-channel mode, the same address will be stored in the Channel 1 and Channel 2 locations of the Start Sweep Register.

The positive-going trailing edges of the 50 ns pulses clock FF U1691A. Gate U1690A controls the operation of U1691A; a high-logic level at U1690A's pin 2 input (from U1695A) permits U1691A to operate in "toggle" mode. Gate U1120A will assert a high-logic level on U1220B pin 4 when GB10 or Chop is at a high-logic level. The high-logic level that enables U1690A causes a high-logic level, via U1520A and U1695B, at the pin 9 input of exclusive-OR gate U1495C. Gate U1495C then inverts the output of U1691A and applies it to the A_2 write address inputs of the Right Start-Sweep Register. If U1695A is not applying a high-logic level to U1690A, the output of FF U1691A stays at a high-logic level.

The negative-going 50 ns pulses from U1690B enable the write inputs of the Right Start-Sweep Register.

RIGHT WRITE ADDRESS NORMALIZER, BLOCK DDD

The Right Write-Address Normalizer (RWAN) controls the two least-significant bits of the write-address bus (bits P0 and P1) so that they match the Interface Board's sequence of sampling. The RWAN consists of U1350A, U1680; U1690C; U1695A, B, C and D; U1520A, and U1640B.

Multiplexer U1680 receives the P0 and P1 bits from U1590 and the output of one-shot U1350A. Gate U1690C controls U1680. Either a low-logic level on Chop or a high-logic level on GB10 activates U1690C, whose high-logic level output causes U1680 to connect its B inputs to its outputs. This puts the 2^0 and 2^1 outputs of U1590 on Address Bus P in their original order (P0=2^0 an and P1=2^1).

When the 5B25N is in Chopped mode and a dual-channel vertical plug-in is in use, the GB10 line will be at a low-logic level and the Chop line will be at a high-logic level. Inverter U1640B applies a high-logic level to U1690C pin 10, which, with the high-logic level on the Chop line, disables U1690C

When disabled, U1690C applies a low-logic level to pin 1 of U1680, causing it to connect its A inputs to its outputs. Section 2 of U1620 now puts U1590's 2^0 output on the P1 line of address Bus P and section 3 applies U1590's 2^1 output to the P0 line via U1695D and U1695C. (A high-logic level from U1695A, activated by the Chop signal, enables U1695D and U1695C.)

Also, when the operating mode is chopped, dual-channel, a positive-going transition on the G $1/\overline{2}$ Right Mux line will trigger one-shot U1350A. The negative-going output of U1350A will pass through the "1" section of U1680 and load the Right Write Counter 2^3, nc; 2^2, nc; 2^1, 0; and 2^0 is connected to the $\overline{\text{L•R•100}}$ μs line. 1; which means that the 2^3 and 2^2 outputs do not change, the 2^1 output is 0 (a low-logic level), and 2^0 output will be determined by the $\overline{\text{L•R•100}}$ μs line.

When the 5B25N is in Chopped mode and a dual-channel vertical plug-in is in use, the output sequence of counter U1590 is normalized by U1680 so that the addressed locations to memory are as shown in Figure 4-24 with reference to the sampled data and markers coming into the memory:

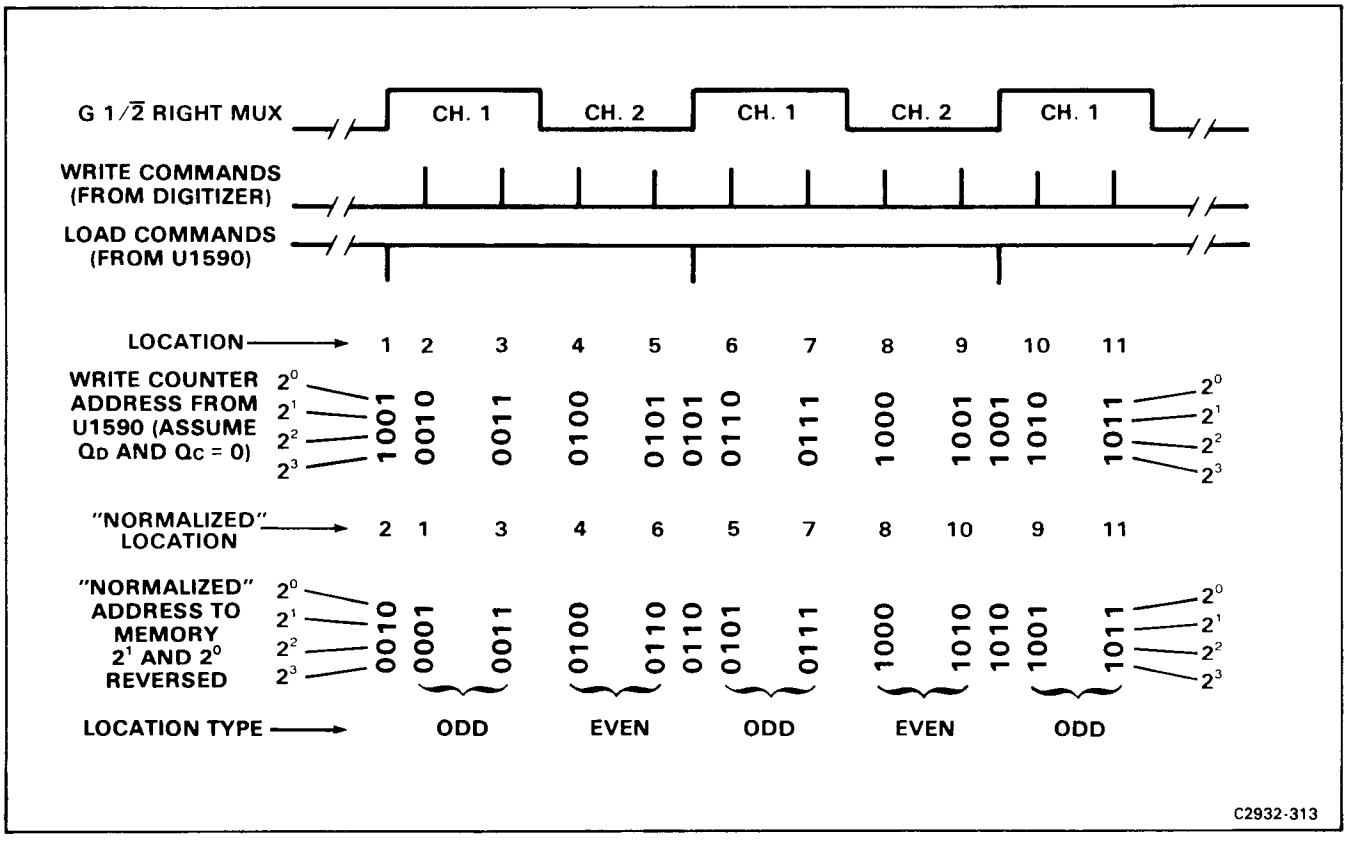


Figure 4-24. Reversal of 2^0 and 2^1 outputs of U1590 to "normalize" memory addresses when operating in "chop, dual-channel"mode.

The normalization process causes the Channel 1 data to be loaded into odd memory locations and Channel 2 data to be loaded into even memory locations.

When U1695A is activated, by a high-logic level on GB10 or Chop, its high-logic level output has three effects, as follows:

1. It enables U1695D, which passes the output of U1680 section 3 to the P0 line.

2. Via U1520A, it asserts a low-logic level on the $\overline{B10}$ line.

3. It enables U1690A in the Right Register Controller, so that the address generated by U1690A, U1691A and U1495C will be alternated to the Right Start Sweep Register.

RIGHT RECORD SORTING, BLOCK EEE

The Right Record Sorting (RRS) circuit determines whether bit Z0 or G Mem Ch 1/$\overline{\text{Ch 2}}$ Sel R will be bit Q0 on Address Bus Q. The RRS consists of U1640C and U1550B, C and D.

Bit C10 indicates whether the data is stored as a single- or dual-channel record. A high-logic level on C10 means single-channel.

Bit C10 controls the RRS circuit. A high-logic level on C10 will enable U1550D, which will then pass the 2^0 output of U1591 to the Q0 line of Address Bus Q via U1550C. (The pin 9 input of U1550C is at a high-logic level because the high-logic level on C10 activated U1640C and U1550B.

A low-logic level on C10 disables U1550D and enables U1550B, via U1640C, to pass the G Mem Ch 1/$\overline{\text{Ch 2}}$ Sel R signal to the Q0 line of Address Bus Q.

RIGHT WRITE COUNTER, BLOCK QQQ

The Right Write Counter (RWC) counts Write Clock Right pulses and supplies a 10-bit number to the Right Start Sweep Register and to The Page A and Page B Address Multiplexers via Address Bus P. The RWC consists of U1390, U1490 and U1590.

Write Clock Right pulses from the Right Memory Sequencer increment the RWC. The 10 sections of U1590, U1490 and U1390 furnish the P0 through P9 bits to Address Bus R.

When the 5223 has a dual-channel vertical amplifier and the time-base is in chopped mode, U1680 will connect its A inputs to the output. If a high-logic level occurs on G 1/$\overline{2}$ Right Mux line, it will trigger one-shot U1350A. Via section 1 of U1680, U1350A's output will load U1590. Counter U1590 will be loaded as follows:

bit N0 - high,

bit N1 - low,

bit N2 - same as before load (Q_C^{-1}), and

bit N3 - same as before load (Q_D^{-1}).

For more details see Right Write-Address Normalizer discussion.

17 MEMORY DISPLAY MULTIPLEXERS & DAC'S

The Memory Display Multiplexers (MDM) and DAC's multiplex data from the two memories to the Memory Buffer Amplifiers via the DAC's. The following circuits comprise the MDM & DAC's:

1. DAC Data Controller, Block A
2. Buffered Vertical DAC, Block B
3. Buffered Horizontal DAC, Block C
4. Horizontal Position Counter, Block OOO

DAC DATA CONTROLLER, BLOCK A

The DAC Data Controller (DAC DC) activates the buffers that transfer data to the vertical and horizontal D/A converters. The DAC DC consists of U110C, U210F, U100A, B, C, and D; and U170.

Gates U110C, U100A through D, and inverter U210F form a logic circuit that provides the A inputs to sections 1 and 4 of multiplexer U170. Multiplexer U170 serves as a mode-changing device that selects L VS R or a conventional memory display. Table 4-6 is a truth table that shows how U100A and B respond to the Display Left, Display Right and L-$\overline{R}$ inputs.

TABLE 4-6
How U100A and B Respond to The Display Left, Display Right and L-R Inputs

Display Left	Display Right	L-R	U100 A	U100 B
0	0	0	1	1
0	0	1	1	1
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

The Left Vs Right line controls U170; a low-logic level on Left Vs Right causes U170 to connect its A inputs to its outputs. If Left Vs Right is at a low-logic level, U170's 4Y and 1Y outputs will follow the outputs of U100B and A, as listed in Table 4-6 which shows that either, but not both, sets of buffers can be enabled. (A low-logic level enables the buffers.) The 2Y and 3Y outputs will be at a high-logic level and a low-logic level respectively. The high-logic level on 2Y will disable buffers U380 and U390, and the low-logic level on 1Y will enable buffers U180 and U190.

When the front-panel L VS R button is pressed the Left Vs Right line will be at a high-logic level, which will cause U170 to connect its B inputs to its outputs. Now the 4Y, 1Y, 2Y and 3Y outputs will be low-, high-, low-, and high-logic levels, respectively, enabling buffers U480 and U490 (left memory) and U380 and U390 (right memory). Data from the left and right memories goes to the vertical and horizontal D/A converters, respectively, on diagram 17.

BUFFERED VERTICAL DAC, BLOCK B

The Buffered Vertical DAC (BV DAC) converts digital input from the left or right plug-in compartment to a representative output current. The output current goes to the vertical Memory Buffer Amplifier on diagram 18. The BV DAC consists of buffers U480, U490, U280, U290, and D/A converter U291.

Two lines from the DAC Data Controller enable the C- and D-bus buffers. When enabled, the buffer applies its input data, via the V-bus, to the input of D/A converter U291. Converter U291 produces a dc current between zero and 4 mA, which is proportional to the digital number at its input. Resistors R293 and R292 establish a +5 V reference voltage for U291.

BUFFERED HORIZONTAL DAC, BLOCK C

The Buffered Horizontal DAC (BH DAC) converts digital input from the Horizontal Position Counter or the right plug-in compartment to a representative output current. The output current goes to the horizontal Memory Buffer Amplifier on diagram 18. The BH DAC consists of buffers U180, U190, U380 and D/A converter U191.

Two lines from the DAC Data Controller enable the horizontal-position buffers and C-bus buffers. When enabled, the buffer applies its input data, via the H-bus, to the input of D/A converter U191. Converter U191 produces a dc current between zero and 4 mA, which is proportional to the digital number at its input. Resistors R193-R192 establish a +5 V reference voltage for U191.

HORIZONTAL POSITION COUNTER, BLOCK OOO

The Horizontal Position Counter (HPC) responds to Read Clock pulses, from block N on diagram 17, and provides an 11-bit digital code representing the number of Read Clock pulses, to the h bus. The HPC consists of U270, U370 and U470.

Counters U270, U370 and U470 form an 11-bit up-counter. G Read Clock pulses increment the counter. The 1,024th G Read Clock pulse causes U470 to assert a high-logic level on the h10 output, which triggers one-shot U500B (in block R on diagram 12) to generate Page Pulse. The Page Pulse resets the HPC, increments the Memory Timeshare Generator, and tests to see if the A or B memory pages should be flipped. The $\overline{\text{Page Pulse}}$ loads the read counters with appropriate addresses via U110A (diagram 11).

MEMORY BUFFER AMPLIFIERS

The Memory Buffer Amplifiers (MBA) produce the horizontal and vertical memory signals for the deflection amplifiers. The MBA consists of the following circuits:

1. Voltage Reference, Block SSS
2. Vertical and Horizontal Position Set, Block TTT
3. Transresistance Amplifiers, Blocks UUU and XXX
4. Signal Shapers, Blocks VVV and YYY
5. Buffered Differential Output Amplifiers, Blocks WWW and ZZZ

VOLTAGE REFERENCE, BLOCK SSS

The Voltage Reference consists of a voltage divider and two voltage followers, U280A and B, that establish reference voltages for the Transresistance Amplifiers. The reference voltage is +8.2 V.

VERTICAL AND HORIZONTAL POSITION SET, BLOCK TTT

These circuits consist of a voltage divider that includes the VERT and HORIZ POSN SET controls, and two voltage followers (U290B and U290A) that apply the respective voltages to the reference inputs of the vertical and horizontal Buffered Differential Amplifiers.

TRANSRESISTANCE AMPLIFIERS, BLOCKS UUU AND XXX

The Transresistance Amplifier (TA) receives a current from the Memory DAC and converts it to a voltage for the Buffered Differential Output Amplifier. The horizontal TA, described here, consists of Q361, Q370, Q180, Q371 and Q362. The vertical TA, shown in block XXX, works similarly.

A maximum 4 mA current flows between the Memory DAC and the emitter of Q361. Because Q361 conducts the DAC's current, the HORIZ POSN control, R190A, adjust Q180's conduction so that the display will be horizontally centered (the voltage at Q361's collector will be about +8.2 V). Resistors R375 and R190B, HORIZ EXP, set the gain of Q361. Emitter-follower Q362 buffers the output signal to the Signal Shaper. When the VECTOR MODE button is pressed a high-logic level on the Gate Control line turns on Q371, which completes a negative feedback loop via Q370. The feedback produces smooth transitions betwen display points instead of sudden jumps.

SIGNAL SHAPERS, BLOCKS VVV AND YYY

The Vertical and Horizontal Shapers each contain two circuits that connect the signal from the Transresistance Amplifier to the Buffered Differential Amplifier. The Dots Joined and Dots Joined signals control switches U350A and U350B in the horizontal channel. When Dots Joined is at a high-logic level, U350A connects the horizontal signal from Q362's output to Q461 via R363. This takes place when the VECTOR MODE button is released. When Dots Joined is at a high-logic level (the VECTOR MODE button is pressed), U350B connects Q362's output to Q461 via filter network R377, L370, R378, C372, C373, R470, L360, C362 and C361. The Vertical Signal Shaper works similarly.

BUFFERED DIFFERENTIAL OUTPUT AMPLIFIERS, BLOCKS WWW AND ZZZ

The Buffered Differential Output Amplifiers (BDOA) provide the vertical and horizontal memory signals for the Vertical and Horizontal Amplifiers. The Horizontal BDOA consists of U350A and B, Q461, Q462, Q470 and U450C.

Switches U350A or B connect the input to amplifier Q461, which drives Q462, the input to the differential stage. Transistors Q462 and Q470 provide the Horiz Mem Signal to the Horizontal Amplifier, shown on diagram 4.

Transistor U450C is a current source (about 6.5 mA) for differential amplifier stage Q462-Q470. The HORIZ POSN SET control, R296, and voltage follower U290B provide a variable reference voltage for Q470, so the user can move the display horizontally.

The Vertical BDOA works similarly.

GPIB/MEMORY BOARD INTERFACE SYSTEM

Microprocessor U700 (diagram 23) is the heart of the GPIB/Memory Board Interface System. It receives a clock signal, an interrupt signal from the GPIB Driver, and eight bits of data from the system data bus. The Microprocessor produces 16 bits of data on the address bus. Bits A0-A11 address the ROMs, A0-A9 address the RAM, and A12-A15 go to an address decoder. The address decoder will activate the ROMs, the RAM, the General Purpose Interface Adapter, the Data Bus Buffer, or the Address Decoder for the Memory Board to Microprocessor Control Signal Multiplexer. Figure 4-25 is a block diagram of the GPIB/Memory Board Interface System.

When Buffer C and the Line Transceivers are enabled, the General Purpose Interface Adapter completes a communication path between the system Data Bus and the external General Purpose Interface Bus.

The Microprocessor (μP) senses the levels that the Rear-Panel Switches set on the system Data Bus, and "decides" what operations it will perform.

Under control of the Microprocessor, the L/R Memory Board Output Multiplexer will connect data from the Left or Right Memory Systems to the system Data Bus.

Via the system Data Bus, data can be loaded into the 5223 Memory Board from the Microprocessor or from the Digitizer.

The Microprocessor can control the Memory Board by setting data into the μP-Memory Board Control Signal Latch. Data from the Latch goes to the Memory Board as control signals.

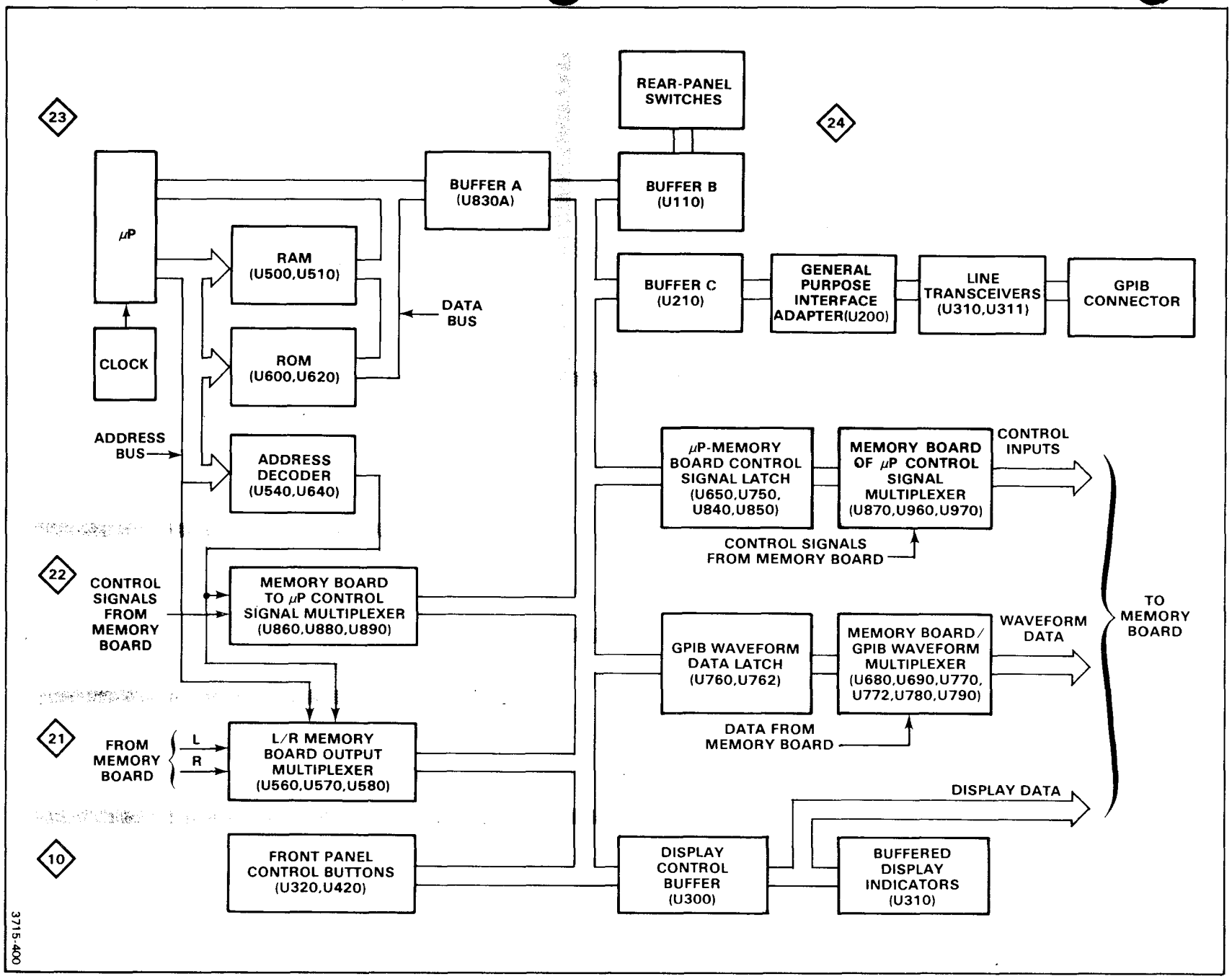


Figure 4-25. Block Diagram of 5223 GPIB/Memory Board Interface System.

The Memory Board or μP Control Signal Multiplexer works with the Memory Board/μP Enable Gates to select either the Memory Board's own control signals or signals from the Microprocessor via the μP-Memory Board Control Signal Latch.

The Memory Board-μP Control Signal Multiplexer permits the Microprocessor to read the control signals for the Left or Right Memories.

The Memory Contents Controller responds to commands from the MEMORY CONTENTS pushbuttons by producing control signals for the 5223 memory system. It also illuminates those MEMORY CONTENTS pushbuttons whose operations are active.

The Memory Buffer Amplifiers produce the horizontal and vertical memory signals for the deflection amplifiers.

Microprocessor to Memory Board Control Signal Latch

Gates U740A, B, C, and D provide output ports U840 and U850 (diagram 22) with the capability of producing latched level outputs or pulse outputs. The U740B-U850 combination operates as follows:

When the pin 5 input of U740B is at a high level, its output asserts a low level on the Enable input of U850. The outputs of U850 will remain in the low-impedance drive mode, at the levels they last contained.

When the pin 5 input of U740B is at a low level, U740B will be activated only during a microprocessor write operation to the latch U850. At all other times U850's outputs will be in the high-impedance mode, and their levels will be established by R750, R751 and U830. This results in the output lines of U850 "pulsing" away from their pulled-down or pulled-up levels only while the microprocessor "writes" a one or a zero, respectively, to U850.

MAINTENANCE

This section contains information for performing preventive maintenance, troubleshooting, and corrective maintenance for the 5223 Option 10 (GPIB) Digitizing Oscilloscope mainframe.

PREVENTIVE MAINTENANCE

Preventive maintenance, when performed on a regular basis, can prevent instrument breakdown and may improve the instruments reliability. The severity of the environment to which the instrument is subjected will determine the frequency of maintenance. A convenient time to perform preventive maintenance is preceding electrical adjustment of the instrument.

CABINET PANEL REMOVAL

WARNING

Dangerous potentials exist at several points throughout this instrument. When the instrument is operated with the covers removed, do not touch exposed connections or components. Some transistors have voltages present on their cases. Disconnect the power before cleaning the instrument or replacing parts.

The side, top, and bottom cabinet panels provide protection from operating potentials present within the instrument. In addition, they reduce radiation of electromagnetic interference from the instrument. The cabinet panels are held in place by grooves in the frame rails. To remove the panels, first loosen the securing screws of the the appropriate rear cabinet feet and/or corner retainer then pivot the feet/retainers till the panel clears. Slide the panel to the rear. See the exploded view drawing in Section 10 Replaceable Mechanical Parts, for additional information. Operate the instrument with the panels in place to protect the interior from dust.

CLEANING

The 5223 should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation. It also provides an electrical conduction path which can result in instrument failure. The cabinet side panels reduce the amount of dust reaching the interior of the instrument. Operation without the panels in place necessitates more frequent cleaning.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a nonresidue type of cleaner, preferably isopropyl alcohol or totally denatured ethyl alcohol. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

EXTERIOR

Loose dust accumulated on the outside of the instrument can be removed with a soft cloth or small brush. The brush is particularly useful for dislodging dirt on and around the front-panel controls. Dirt which remains can be removed with a soft cloth dampened in a mild solution of detergent and water. Abrasive cleaners should not be used.

CRT

Clean the plastic light filter, implosion shield, and the crt faceplate with a soft, lint-free cloth dampened with denatured alcohol.

INTERIOR

Cleaning the interior of the instrument should only be occasionally necessary. The best way to clean the interior is to blow off the accumulated dust with dry, low-velocity air (approximately 5 lb/in^2). Remove any dirt which remains with a soft brush or a cloth dampened with a mild solution of detergent and water. A cotton-tipped applicator is useful for cleaning in narrow spaces, or for cleaning more delicate circuit components.

CAUTION

Circuit boards and components must be dry before applying power to prevent damage from electrical arcing.

The high-voltage circuits should receive special attention. Excessive dirt in this area may cause high-voltage arcing and result in improper instrument operation.

VISUAL INSPECTION

The 5223 should be inspected occasionally for such defects as broken connections, improperly seated semiconductors, damaged or improperly installed circuit boards, and heat-damaged parts. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged parts are found. Overheating usually indicates other trouble in the instrument; therefore, correcting the cause of overheating is important to prevent recurrence of the damage.

SEMICONDUCTOR CHECKS

Periodic checks of semiconductors are not recommended. The best check of semiconductor performance is actual operation in the instrument. More details on semiconductors are given under Troubleshooting later in this section.

PERIODIC ELECTRICAL ADJUSTMENT

To ensure accurate measurements, check the electrical adjustment of this instrument after each 1000 hours of operation, or every six months if used infrequently. In addition, replacement of components may necessitate adjustment of the affected circuits. Complete adjustment instructions are given in Section 6, Calibration. This procedure can be helpful in localizing certain troubles in the instrument, and in some cases, may correct them.

TROUBLESHOOTING

The following information is provided to facilitate troubleshooting of the 5223 Option 10 Digitizing Oscilloscope mainframe. Information contained in other sections of this manual should be used in conjunction with the following data to aid in locating a defective component. An understanding of the circuit operation is helpful in locating troubles. See Section 4, Theory of Operation, for this information.

GPIB TROUBLESHOOTING

Option 10 adds microprocessor controlled GPIB (General Purpose Interface Bus) capability to the standard 5223 Digitizing Oscilloscope mainframe. Because problems in microprocessor controlled circuits are very difficult to find using conventional troubleshooting methods, a special troubleshooting technique called "signature analysis" is used for locating problems in this circuitry. Signature analysis troubleshooting and the instrument self-test are explained in detail later in this section, however, brief descriptions are given below.

SELF TEST

A self-test feature designed into the 5223 Option 10 is used to determine the need for signature analysis troubleshooting. Each time the 5223 Option 10 is powered-up, an internal RESET causes the instrument to perform a self-test of the microprocessor controlled GPIB circuitry. Instrument problems not detected by the self-test are likely not related to the GPIB circuitry. In which case, the conventional troubleshooting methods discussed below should be used to locate and correct the problem. The self-test and how to interpret its results are explained in detail later in this section.

SIGNATURE ANALYSIS

Signature analysis troubleshooting greatly simplifies the task of locating problems in microprocessor controlled circuits. In signature analysis, the microprocessor circuit generates repetitive signal patterns from internal instructions. These patterns form the "signatures" which occur at various points (nodes) within the circuit. Reading these signatures can often lead directly to the location of a circuit problem.

The Self-Test and Signature Analysis Troubleshooting portion of this section contains a background discussion of signature analysis troubleshooting. It also provides detailed instructions for performing signature analysis troubleshooting on the 5223.

CONVENTIONAL TROUBLESHOOTING AIDS

DIAGRAMS

Complete schematic diagrams are given on the foldout pages in Section 9, Diagrams and Circuit Board Illustrations. The component circuit number and electrical value of each component in this instrument are

shown on these diagrams. (See the first page of the Diagrams and Circuit Board Illustrations section for definitions of the reference designators and symbols used to identify components in this instrument.) Important voltages and numbered waveform test points are also shown on the diagrams. Important waveforms, and the numbered test points where they were obtained, are located adjacent to each diagram. The portions of circuits mounted on circuit boards are enclosed with heavy, solid-black lines. Each schematic diagram is divided into functional stage blocks, as indicated by the wide shaded lines. These functional blocks are described in detail in Section 4, Theory of Operation.

CIRCUIT BOARD ILLUSTRATIONS

To aid in locating circuit boards, an illustration showing the circuit board location appears on the back of the foldout page facing the schematic diagram. An illustration of the circuit board(s) is also included here to identify the physical location of components and waveform test points that appear on the respective schematic diagram. Each circuit board illustration and diagram are arranged in a grid locator with an index to facilitate rapid location of components contained in the corresponding schematic diagram.

TROUBLESHOOTING CHARTS (Appendix A)

The troubleshooting charts contained in Appendix A at the rear of this manual are provided to aid in locating circuit troubles in the A11-Memory board. These troubleshooting charts will direct you to the probable faulty circuit and suggest an appropriate remedy for the problem.

Troubleshooting Hints

From our experience with development and manufacture of the 5223 Digitizing Oscilloscope, we've compiled a few service "hints" which may prove helpful in troubleshooting the instrument. These service "hints" supplement the fold-out troubleshooting charts and are located at the beginning of Appendix A.

MEMORY BOARD EXTENDER KIT

An extender board kit is available to allow access to component pins and test points mentioned in the Troubleshooting Chart foldouts in Appendix A at the rear of this manual (see Calibration Fixture in Troubleshooting Equipment list). The extender board set mounts the A11-Memory Board perpendicular to the A18-GPIB Board. All circuits function in a normal fashion. Refer to Figure 5-1 for proper mounting configuration.

ADJUSTMENT AND TEST POINT LOCATIONS

To aid in locating test points and adjustable components called out in the various sections of the Calibration procedure, the Adjustment and Test Point Locations foldout pages are provided in Section 9, Diagrams and Circuit Board Illustrations.

COMPONENT COLOR CODING

This instrument contains brown composition resistors, some metal-film resistors, and some wire-wound resistors. The resistance values of wire-wound resistors are usually printed on the component body. The resistance values of composition resistors and metal-film resistors are color coded on the components using the EIA color code (some metal-film resistors may have the value printed on the body). The color code is read starting with the stripe nearest the end of the resistor. Composition resistors have four stripes, which consist of two significant figures, a multiplier, and a tolerance value (see Fig. 5-2). Metal-film resistors have five stripes consisting of three significant figures, a multiplier, and a tolerance value.

The values of common disc capacitors and small electrolytics are marked on the side of the component body. The white ceramic and epoxy-coated tantalum capacitors used in the instrument are color coded using a modified EIA code (see Fig. 5-2).

The cathode end of glass-encased diodes is indicated by a stripe, a series of stripes, or a dot. The cathode and anode ends of metal-encased diodes can be identified by the diode symbol marked on the body.

SEMICONDUCTOR LEAD CONFIGURATIONS

Lead configurations and index locators for semiconductor devices used in the 5223 Option 10 Digitizing Oscilloscope are shown in Figure 5-3.

STATIC-SENSITIVE DEVICES

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 5-1 for relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common to unprotected environments.

Observe the following precautions to avoid damage.

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or conductive foam. Label any package that contains static-sensitive assemblies or components.

3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.

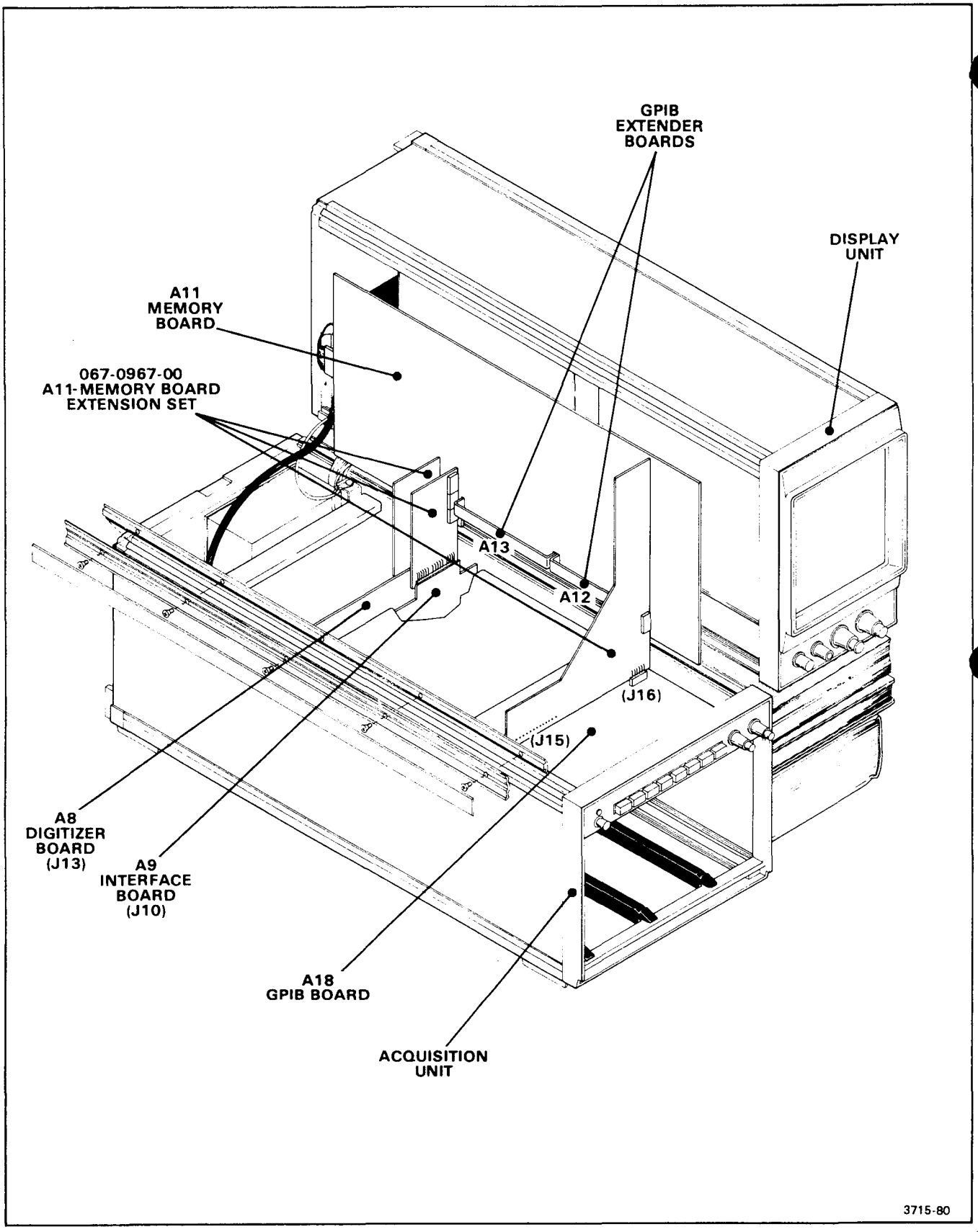
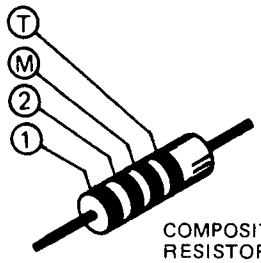
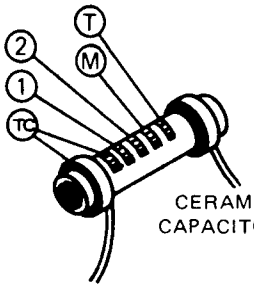


Figure 5-1. Using the A11-Memory board extender kit.

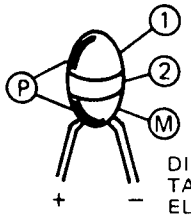
COLOR CODE



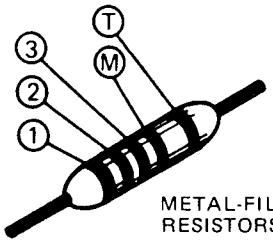
COMPOSITION RESISTORS



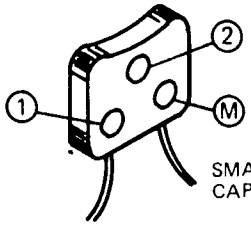
CERAMIC CAPACITORS



DIPPED TANTALUM ELECTROLYTICS



METAL-FILM RESISTORS



SMALL DISC CAPACITORS

(1) (2) and (3) - 1ST, 2ND, AND 3RD SIGNIFICANT FIGS. (T) AND/OR (TC) COLOR CODE MAY NOT BE PRESENT ON SOME CAPACITORS;

(M) - MULTIPLIER (T) - TOLERANCE;

(TC) - TEMPERATURE COEFFICIENT. (P) - POLARITY AND VOLTAGE RATING

COLOR	SIGNIFICANT FIGURES	RESISTORS		CAPACITORS			DIPPED TANTALUM VOLTAGE RATING
		MULTIPLIER (OHMS)	TOLERANCE	MULTIPLIER (pF)	TOLERANCE		
					OVER 10pF	UNDER 10pF	
BLACK	0	1	---	1	±20%	± 2pF	4VDC
BROWN	1	10	±1%	10	±1%	±0.1pF	6VDC
RED	2	10^2 or 100	±2%	10^2or 100	±2%	---	10VDC
ORANGE	3	10^3or 1 K	±3%	10^3 or 1000	±3%	---	15VDC
YELLOW	4	10^4 or 10K	±4%	10^4 or 10,000	+100% −0%	---	20VDC
GREEN	5	10^5 or 100 K	±1/2%	10^5or 100,000	±5%	±0.5pF	25VDC
BLUE	6	10^6 or 1 M	±1/4%	10^6 or 1,000,000	---	---	35VDC
VIOLET	7	---	±1/10%	10^7 or 10,000,000	---	---	50VDC
GRAY	8	---	---	10^{-2} or 0.01	+80% −20%	±0.25pF	---
WHITE	9	---	---	10^{-1} or 0.1	±10%	±1pF	3VDC
GOLD	---	10^{-1} or 0.1	±5%	---	---	---	---
SILVER	---	10^{-2} or 0.01	±10%	---	---	---	---
NONE	---	---	±20%	---	±10%	±1pF	---

C1862-74

Figure 5-2. Color code for resistors and capacitors.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by the body, never by the leads.

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only special antistatic vacuum type desoldering tools such as the Pace model PC10.

TABLE 5-1
Relative Susceptibility to Static Discharge Damage

Semiconductor Classes	Relative Susceptibility Levels[1]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear Microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[1]Voltage equivalent for levels:

1 = 100 to 500 V
2 = 200 to 500 V
3 = 250 V
4 = 500 V
5 = 400 to 600 V
6 = 600 to 800 V
7 = 400 to 1000 V (est.)
8 = 900 V
9 = 1200 V

(Voltage discharged from a 100 pF capacitor through a resistance of 100 ohms.)

MULTI-PIN CONNECTOR IDENTIFICATION

Pin 1 on multi-pin connectors is designated with a triangle. A triangle, dot or square printed on circuit boards denotes pin 1. When a connection is made to a circuit board, the orientation of the triangle on the multi-pin holder is determined by the index (triangle, dot or square) printed on the circuit board (see Fig. 5-4).

Some multi-pin connectors are equipped with a locking mechanism to more readily secure the connector to the circuit board. To remove these connectors, grasp the connector body and pull parallel to the pin. These connectors should not be removed by pulling on the wire leads; this causes the locking mechanism to clamp onto the circuit board pins.

TROUBLESHOOTING EQUIPMENT

The following equipment is useful for troubleshooting the 5223 Digitizing Oscilloscope mainframe:

1. Transistor Tester

Description: Dynamic-type tester.

Purpose: Test semiconductors.

Recommended type: TEKTRONIX 577/177 Curve Tracer, TEKTRONIX 576 Curve Tracer, 7CT1N Curve Tracer plug-in unit and a 7000-series oscilloscope system, or a 5CT1N Curve Tracer plug-in unit and a 5000-series oscilloscope system.

2. Digital Multimeter

Description: 10 megohm input impedance and 0 to 1 kilovolt range, ac and dc; ohmmeter, accuracy, within 0.1%. Test probes must be insulated to prevent accidental shorting.

Purpose: Check voltages and resistances.

Recommended type: TEKTRONIX DM 501A Digital Multimeter.

3. Test Oscilloscope (Storage)

Description: Frequency response, dc to 100 megaherts minimum; deflection factor, 5 millivolts to 5 volts/division and 1 milliampere to 1 ampere/division. at 10X, 10-megohm voltage probe should be used to reduce circuit loading for voltage measurements. For current waveforms, use a TEKTRONIX P6021 Current Probe with passive termination, or the equivalent.

Purpose: Check operating waveforms.

Recommended type: TEKTRONIX 466 Portable Storage Oscilloscope System. Refer to the Tektronix Products catalog for other applicable oscilloscope systems.

@

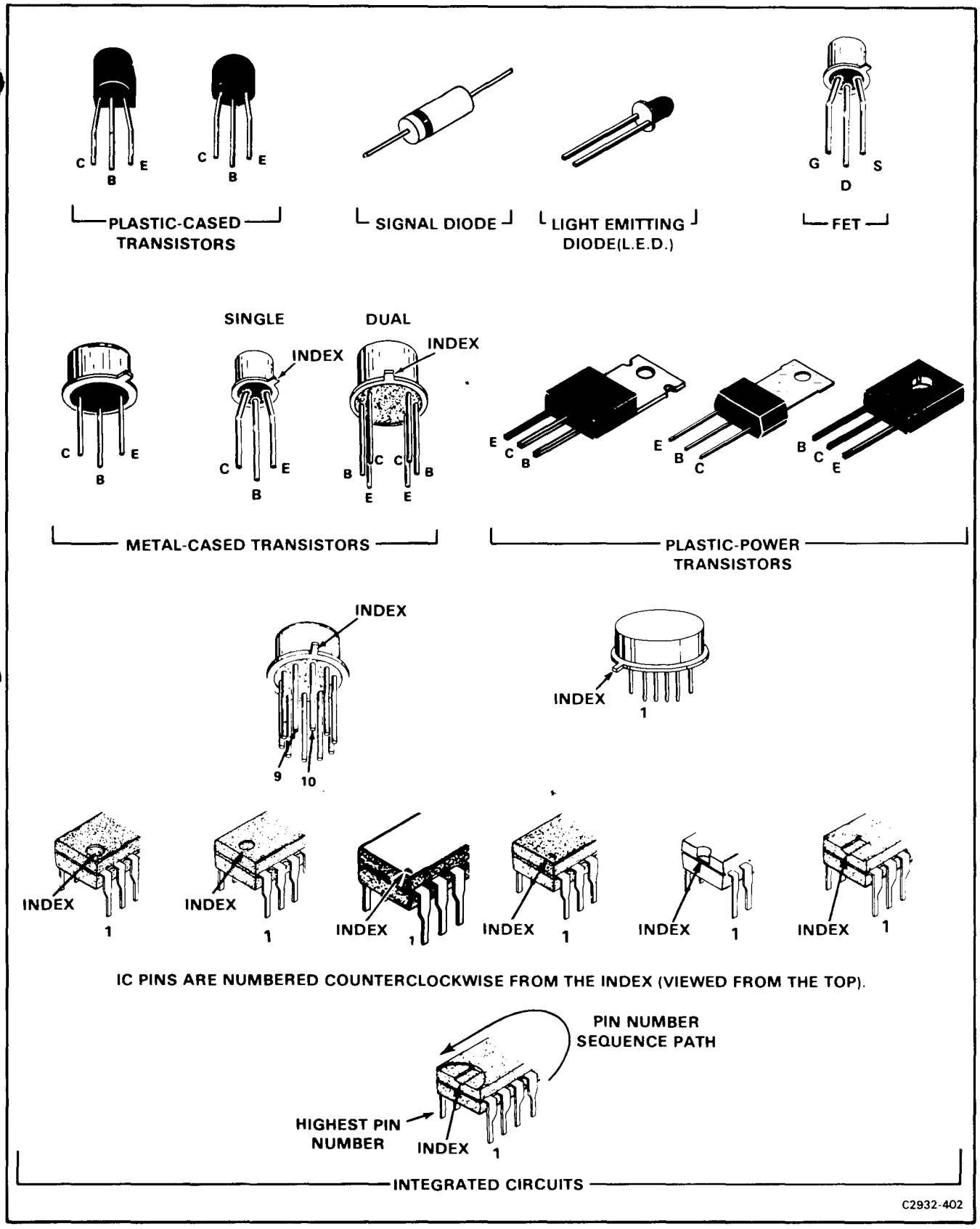


Figure 5-3. Semiconductor lead configurations.

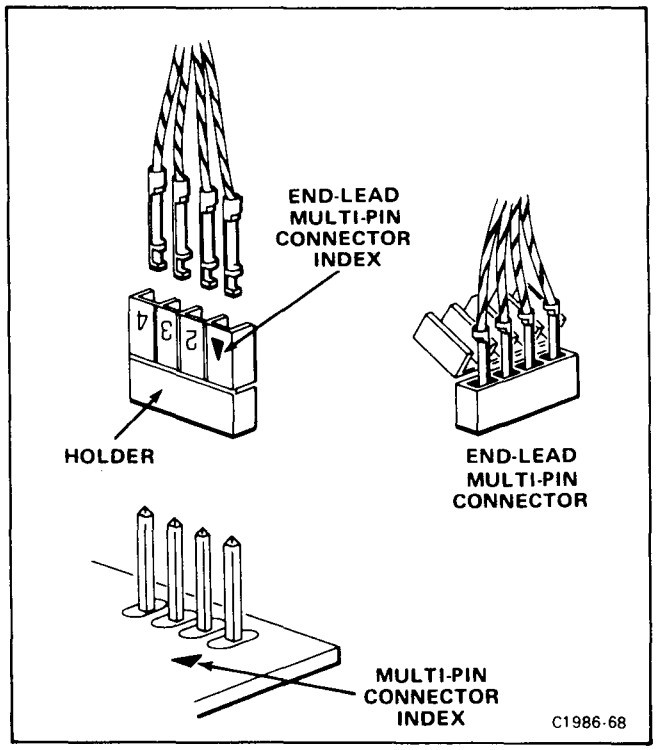


Figure 5-4. Orientation of multi-pin connectors.

4. Variable Autotransformer

   Description: Output variable from 0 to 140 volts, 10 amperes minimum rating. Must have three-wire power cord, plug, and receptacle.

   Purpose: Vary input line voltage when troubleshooting in the power-supply unit.

   Recommended type: General Radio W10MT3W Variac Autotransformer.

5. Isolation Transformer

   Description: 1:1 turns ratio, 500 volt-amperes minimum rating, 50-60 cycle. Must have three-wire power cord, plug, and receptacle with ground connection carried through from input to output.

   Purpose: To isolate the 5223 from line potential when troubleshooting power supply.

   Recommended type: Stancor #P6298 (for 115-volt line only) modified to include three-wire power cord, plug, and receptacle.

6. Digital Tester

   Description: Time Measurements, Logic level indicator.

   Purpose: Troubleshooting the A11-Memory board and A10-Switch board.

   Recommended type: TEKTRONIX 851 Digital Tester.

7. Calibration Fixture

   Purpose: Troubleshooting the A10-Switch and A11-Memory board.

   Recommended type: Tektronix 067-0967-00 Memory Board Extension Board Set.

8. Signature Analyzer

   Purpose: Troubleshooting the GPIB circuitry.

   Recommended type: SONY/TEKTRONIX 308 Data Analyzer with pull-up resistor option.

9. Calibration Fixture

   Purpose: Signature analysis troubleshooting.

   Recommended type: Tektronix 067-0966-00 Loop-through board set.

TROUBLESHOOTING TECHNIQUES

This troubleshooting procedure is arranged to check the simple trouble possibilities before proceeding with extensive troubleshooting. The first few checks ensure proper connection, operation, and adjustment. If the trouble is not located by these checks, the remaining steps aid in locating the defective component. When the defective component is located, replace it following the replacement procedures given under Corrective Maintenance.

1. CHECK CONTROL SETTINGS

Incorrect control settings can indicate a trouble that does not exist. If there is any question about the correct function or operation of any control on the 5223, refer to Section 2, Operating Instructions.

2. CHECK ASSOCIATED EQUIPMENT

Before proceeding with troubleshooting, check that the equipment used with this instrument is operating correctly. Also, check that the input signals are properly connected and that the interconnecting cables are not defective. Check the line-voltage source.

3. VISUAL CHECK

Visually check that portion of the instrument in which the trouble is located. Many troubles can be found by visible indications, such as unsoldered connections, loose cable connections, broken wires, damaged circuit boards, and damaged components.

4. CHECK INSTRUMENT ADJUSTMENT

Check the electrical adjustment of this instrument, or the affected circuit if the trouble appears in one circuit. The apparent trouble may only be a result of misadjustment. Complete adjustment instructions are given in Section 6, Calibration.

5. ISOLATE TROUBLE TO A CIRCUIT

To isolate trouble to a particular circuit, note the trouble symptom. The symptom often identifies the circuit in which the trouble is located. When trouble symptoms appear in more than one circuit, check the affected circuits by taking voltage and waveform measurements. Also check for the correct output signals at the front- and rear-panel output connectors with a test oscilloscope. If the signal is correct, the circuit is working correctly up to that point.

Incorrect operation of all circuits often indicates trouble in the power supply. However, a defective component elsewhere in the instrument can appear as a power-supply trouble and may also affect the operation of other circuits.

Locating test points and components on the A8-Digitizer board and A18-GPIB board is extremely difficult due to the physical location of the boards in the mainframe.

For access to components and test points shown on the schematics and associated dollies use the mounting configuration (A18-GPIB board, A11-Memory board) and board placement (A8-Digitizer board) as shown in Figure 5-1 and Figure 5-5 respectively.

The 5223 Troubleshooting Charts, in Appendix A provide a guide for locating defective circuits in the A11-Memory board. First, identify the trouble symptom, then start at the top left of the appropriate chart (Refer to Index of Symptoms) and perform the checks given across the top of the page until a step is found that does not produce the indicated results. Further checks, on the circuit in which the trouble is probably located, are listed below the step. These charts do not include checks for all possible defects; use steps 6 and 7 in such cases.

6. CHECK VOLTAGES AND WAVEFORMS

Often the defective component can be located by checking for the correct voltages or waveforms in the circuit. Typical voltages and waveforms are given in Section 9, Diagrams and Circuit Board Illustrations.

NOTE

Voltages and waveforms given in Section 9, Diagrams and Circuit Board Illustrations, are not absolute and may vary slightly between 5223 Digitizing Oscilloscope Mainframes. To obtain operating conditions used to take these readings, see the Voltage and Waveform Conditions adjacent to the schematic.

7. CHECK INDIVIDUAL COMPONENTS

The following procedures describe methods of checking individual components in the 5223. Components which are soldered in place (excluding Integrated Circuits) are best checked by first disconnecting one end. This isolates the measurement from the effects of surrounding circuitry.

WARNING

To avoid electric-shock hazard, always disconnect the 5223 from the power source before removing or replacing components.

Fuses

Check for open fuses by checking continuity with an ohmmeter.

Transistors

A good check of transistor operation is actual performance under operating conditions. A transistor can most effectively be checked by substituting a new component for it (or one which has been previously checked). However, be sure that circuit conditions are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic tester. Static-type testers are not recommended, since they do not check operation under simulated operating conditions.

Integrated Circuits

Integrated circuits can be checked with a test oscilloscope, digital tester or by direct substitution.

CAUTION

Direct substitution must not be attempted with soldered in integrated circuits. The I.C., circuit board or both could be damaged due to the heat required to melt the solder from the connections. Refer to Soldering Techniques later in this section. Use care when checking voltages and waveforms around the integrated circuits so that adjacent leads are not shorted together. The integrated circuit test clip provides a convenient means of clipping a test probe to the in-line, multi-pin integrated circuits.

A good understanding of the circuit operation is essential to troubleshooting circuits using integrated circuits. Operating waveforms, logic levels, and other operating information for the integrated ciruits are given in Section 4, Theory of Operation and Section 9, Diagrams and Circuit Board Illustrations.

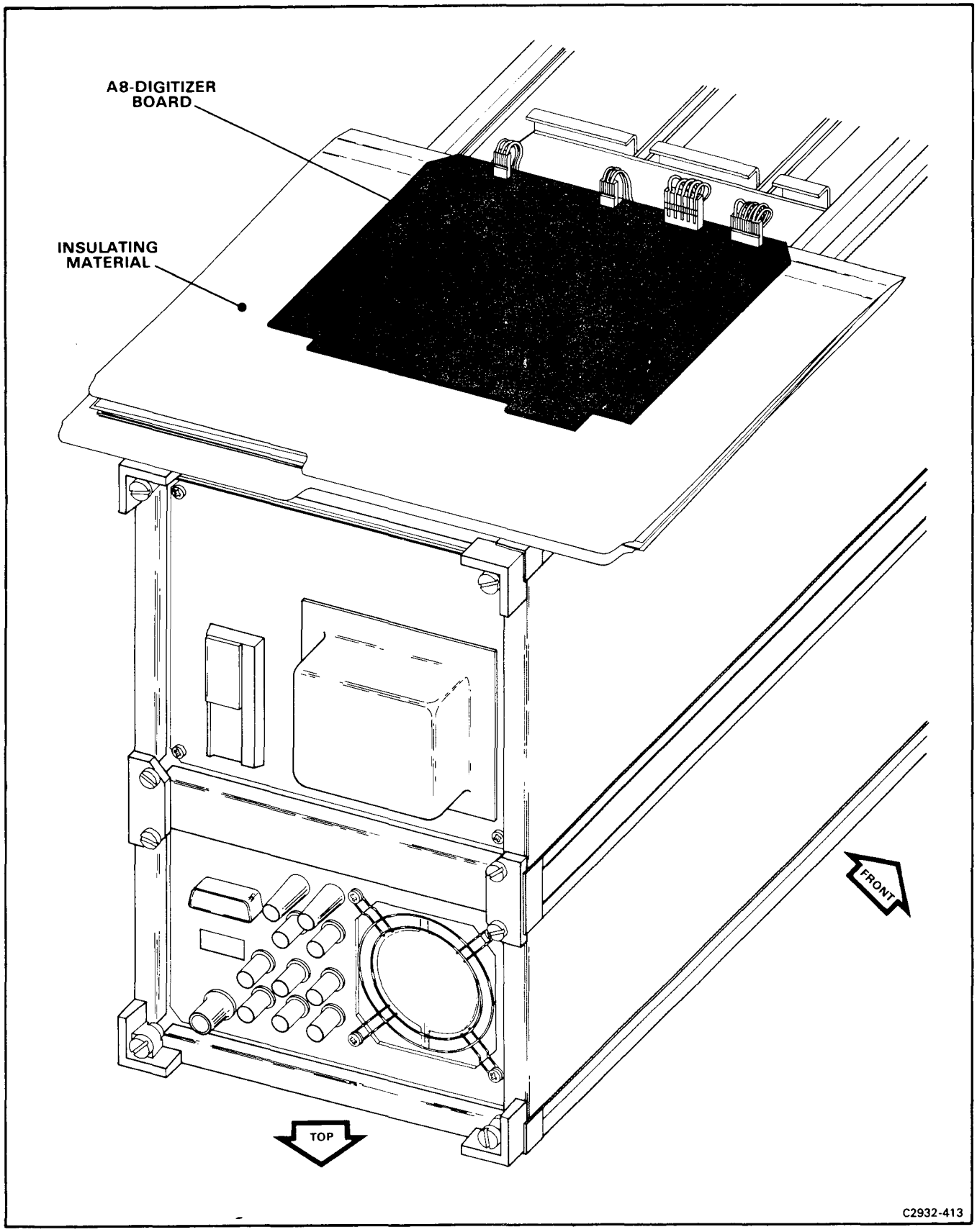


Figure 5-5. A8-Digitizer board placement for troubleshooting.

Diodes

A diode can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter on a scale having a low internal source current, such as the R X 1k scale. The resistance should be very high in one direction and very low when the meter leads are reversed.

CAUTION

When checking diodes, do not use an ohmmeter scale that has a high internal current, since high currents may damage the diodes under test.

Resistors

Check the resistors with an ohmmeter. Resistor tolerances are given in Section 8, Replaceable Electrical Parts. Normally, resistors do not need to be replaced unless the measured value varies widely from the specified value.

Capacitors

A leaky or shorted capacitor can best be detected by checking resistance with an ohmmeter on the highest scale. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after initial charge of the capacitor. An open capacitor can best be detected with a capacitance meter or by checking if the capacitor passes ac signals.

8. REPAIR AND ADJUST THE CIRCUIT

If any defective parts are located, follow the replacement procedures given under Component Replacement in this section. Check the performance of any circuit that has been repaired or that has had any electrical components replaced. Adjustment of the circuit may be necessary.

SELF-TEST AND SIGNATURE ANALYSIS TROUBLESHOOTING

The GPIB circuitry in the 5223 Option 10 Digitizing Oscilloscope is microprocessor controlled and, therefore, lends itself to the use of a troubleshooting technique called "signature analysis". Signature analysis is used to troubleshoot the GPIB portion of the 5223 Option 10 (this is in addition to the standard troubleshooting information). Another feature made possible with microprocessor control is the inclusion of an instrument "self-test" routine which is automatically performed every time the instrument is powered-up.

The first step to troubleshooting the 5223 Option 10 is the performance of the power-up self-test. This is done with the protective covers still on the instrument. Should the instrument pass self-test there is likely no need to use signature analysis for troubleshooting. However, should the self-test indicate a fault condition, Table 5-2 will refer you to the appropriate portion of the signature analysis troubleshooting flow charts (in Appendix B) to begin checking for the problem.

POWER-UP SELF-TEST

The 5223 Option 10 Digitizing Oscilloscope automatically performs a self-test each time power is applied to the instrument. At power-on, a RESET signal is generated which initiates the running of a series of internal routines that verify the proper operation of the GPIB board ROM, GPIB board RAM, GPIB board-Memory board data path, the waveform memory, and the GPIB Board-Driver board data path respectively.

LED	FAULT LOCATION
DISPLAY LEFT	Lower ROM.
SAVE LEFT	Upper ROM.
LEFT VS RIGHT	RAM.
SAVE RIGHT	CPU board-Memory board data path.
DISPLAY RIGHT	Waveform memory.
VECTOR MODE	CPU board-Back Panel board data path.

If the instrument successfully passes its self-test none of the LED's will blink or stay illuminated unless they are pressed.

SELF-TEST SETUP CONDITIONS

The self-test should be performed with the protective panels in place, the rear panel TEST switch in the OFF position (see Fig. 5-6), and with a 5B25N Digitizer Time Base/Amplifier installed in the right plug-in compartment.

TABLE 5-2
5223 Option 10 Self-Test Failure Table

Symptom	Possible Cause	Action
1. All switches illuminate on power up and stay lit.	Test switch on the GPIB selector is in the TEST position.	
2. DISP L or SAVE L lights blinks on power-up.	ROM test failure. Bad ROM, bad address lines to ROM—use signature analysis to determine and correct the problem	Perform Signature Analysis Set-up then start at trouble-shooting chart 1
3. L VS R light blinks on power-up.	RAM test failure. Bad RAM, open DATA or ADDRESS lines to RAM, or possibly a bad address decoder. Use signature analysis to determine and correct this problem. NOTE: ADDRESS and DATA shorts would be detected by the ROM test.	Perform Signature Analysis Set-up then start at trouble-shooting chart 10
4. SAVE R light blinks on power-up.	Buffer test failure. Bad memory board, bad connector from GPIB board to memory board, or bad IC on GPIB board. Bad GPIB board IC's could include U760, U762, U680, U690, U770, U780, U790, U772, U580, U570, and U560. Use signature analysis to determine and correct the problem.	Perform Signature Analysis Set-up then start at trouble-shooting chart 14
5. DISP R light blinks on power-up.	Memory board RAM failure. Bad memory board, bad IC's as in Buffer test above, or U650, U750, U840, or U850 could be bad. Use signature analysis to determine and correct the problem.	Perform Signature Analysis Set-up then start at trouble-shooting chart 18
6. VECTOR light blinks on power-up.	Back Panel board test failed. Could be cabling problem, bad U200 or U210 on Back Panel board. Use signature analysis to determine and correct the problem.	
7. The 5223 Option 10 does not operate with	1. The GPIB ON/OFF switch is OFF. 2. The GPIB address switches are not set correctly.	

TABLE 5-2 (CONT)
5223 Option 10 Self-Test Failure Table

Symptom	Possible Cause	Action
regards to GPIB activity but the self tests pass and the oscilloscope appears to operate normally otherwise.	3. The TEST and TALK ONLY switches are on. 4. U200 is defective. 5. The bus drivers are defective. 6. Defective cabling between the GPIB board and the Back Panel board. 7. The switch buffer on the Back Panel board is defective. 8. A connection from the GPIB cable connector to the Back Panel board is shorted or open.	
8. The switches will not illuminate on power-up.	The TALK ONLY switch on the GPIB selector is in the TALK ONLY position.	
9. On power-up, DISP L, DISP R, L VS R, and VECTOR switches work properly but the SAVE switches stay illuminated.	No 5B25N Time Base installed or the AMP MODE is selected. There could also be a problem with the sweep rate circuit.	
10. The MEMORY BOARD RAM test does not fail on power-up but the calibrated graticule fails to appear	The MEMORY BOARD RAM test was not executed, which is caused by the failure of the microprocessor data bus to go HI when no device is selected. Use signature analysis to determine and correct the problem.	
11. Nothing happens that makes any sense.	Use signature analysis to determine and correct the situation.	

OTHER CONSIDERATIONS

At this point there are several considerations to take into account. They are:

If the rear panel TEST switch is in the ON position when power is applied, the instrument will not complete its self-test but will branch instead to one of the signature analysis routines.

If a 5B25N Digitizing Time Base/Amplifier unit is not installed, or if it is set to "AMPL", both SAVE lights will illuminate and stay lit at the conclusion of the self-test. This is true regardless of whether or not the SAVE buttons are pressed but it DOES NOT indicate a fault condition.

The ROLL pushbutton will not light when pressed if the time-base sweep speed is set faster than 0.1 second per division.

Left vs Right slaving will override the status (out position or pressed in) of the SAVE buttons. For example, if the Left SAVE and Left vs Right buttons are pressed, the right SAVE button will be lit regardless of whether it is pressed or not.

The CPU-Back Panel data path self-test is performed only when the GPIB ON/OFF switch is in the ON position.

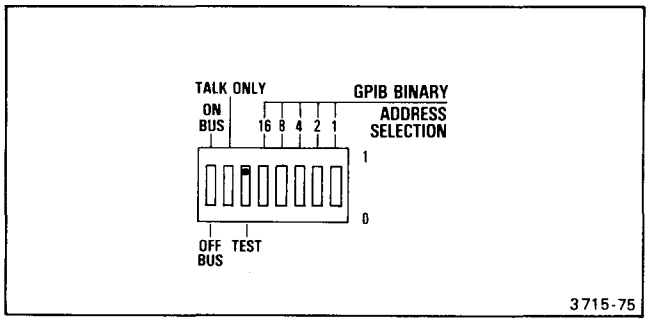


Figure 5-6. GPIB test switch shown in the OFF position.

GRATICULE PATTERN DISPLAY

At the conclusion of the Waveform Memory test, a calibrated graticule pattern is loaded into the left and right memory compartments. This pattern can be displayed if both SAVE buttons, the Left vs Right button, and either DISPLAY button are pressed at power-on.

The displayed graticule will have one dot on each minor division. The dots are arranged in such a way that, if the graticule is output to an X-Y plotter, a continuous curve is plotted. Waveform Y-values at the center of the graticule are precisely 1/2 scale; if output over the GPIB, they have a value of zero.

SELF-TEST FAULT CONDITIONS

Should any self-test produce a fault indication, all subsequent tests are suspended. Refer to Table 5-2 for the possible cause and appropriate action to take.

Step Through Fault Conditions

A fault condition warning can be ignored by pressing the OUTPUT SAVED DISPLAY button. This will extinguish the flashing LED and step the instrument to the next item in the self-test sequence. Depending on the severity of the fault, you may be able to step the instrument through all remaining tests and into normal operation in this manner.

SIGNATURE ANALYSIS TROUBLESHOOTING

When the power-up self test indicates a need to use signature analysis to troubleshoot a problem, the following information will guide you into and through the process. Though it might cause apprehension in those unfamiliar with it, signature analysis is really a simple-to-use troubleshooting method that will speed you through what would otherwise be a tedious, if not impossible task—tracing a problem in a microprocessor controlled circuit. This information begins with a general discussion of signature analysis troubleshooting followed by a description of the stimulation routines designed into the 5223 Option 10 firmware, an overview of the signature analysis tests, a list of test equipment required, and information for preparing the 5223 Option 10 for signature analysis troubleshooting. Signature analysis troubleshooting flow charts and Signature sets are contained in Appendix B at the rear of this manual.

SIGNATURE ANALYSIS BACKGROUND INFORMATION

Signature analysis is a troubleshooting method for isolating faults, usually to the component level, in complex logic circuits. Signature analysis testing relys on exercising or "wiggling" points in the circuit (nodes) in a repeatable and somewhat predictable fashion. The manner in which the circuit nodes are exercised is relatively unimportant, as long as the events at the node under test are repeatable. For example, a microprocessor system can easily be made to repeatedly increment (loop) through its address fields, exercising a good portion of the instrument's circuitry. Or, as in most cases, exercise routines are stored in ROM and can be easily retrieved and run to exercise circuitry in the instrument.

Once a means of exercising the circuitry has been implemented, actual signatures at circuit nodes can be taken. Individual signatures are taken over a specific number of system clock cycles (gate time), determined by how the signature analyzer is electrically connected into the system. The actual signature is presented to the user as a 4-digit hexadecimal type number that is a numerical representation of the generally complex sequence of events occurring at the node under test. Individual signatures may be composed of the characters 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, C, F, H, P and U.

The signatures taken at various nodes are compared to "signature sets" containing known good signatures for each particular test node. (All signatures for these procedures were taken with a SONY/TEKTRONIX 308 Data Analyzer. Use of other signature analyzers may result in meaningless signatures.) An incorrect signature indicates a problem. Bad signatures can be traced back (in terms of data flow) to the point of error in much the same way a bad waveform can be traced back to its source in analog circuitry.

However, an important difference in analog signal tracing and digital signature tracing should be noted. In analog signal tracing, many clues to a fault can be picked up by watching for deviations from the desired waveshape (clipping, oscillations, power supply noise, etc.). In signature tracing, however, subtle differences in signatures from those desired mean nothing. A wrong signature is wrong and that's generally all that can be determined from it.

There are several cases where certain wrong signatures may provide clues, though. A signature of 0000 may be an indicaton that a test node is shorted to ground (0000 is the "ground" signature). Likewise, a node with a faulty signature the same as the V_{cc} signature may be shorted to the positive supply. When two or more nodes have the same bad signature, they may also be shorted together.

Signature analysis may be used in configurations other than that described above, but are not used differently with the 5223 Option 10 Digitizing Oscilloscope. Many technical articles are available on the subject of Signature Analysis and should be referred to if you desire more specific information.

STIMULATION ROUTINES

The 5223 Option 10 firmware contains a set of stimulation routines. Some of these routines are used for signature analysis troubleshooting and others are used for special troubleshooting situations. All of the stimulation routines are described below. The signature analysis routines generate repetitive signals at various nodes on the GPIB board and produce the signatures required for troubleshooting with the Signature Sets and flow-charts in Appendix B.

Stimulation routines are selected by means of the GPIB Address Selector switches in conjunction with the TEST switch on the rear panel of the instrument (refer to Fig. 5-7). With the TEST switch in the ON position at power-up, the 5223 Option 10 will complete its ROM self-test then branch to which ever stimulation routine is selected. This will also happen if the A14-Driver board is disconnected or otherwise disabled, in which case stimulation routine 0 is automatically entered. Each of the stimulation routines is a "dead-end" as far as the firmware is concerned, and once entered they run repetitively until the microprocessor is reset.

To select a stimulation routine press the TEST switch to the ON (down) position and set up the binary number of the desired routine on swtiches 4 through 8. For example, when switches 8 and 7 are pressed, binary number 3 is set up and selects stimulation routine 3. Other stimulation routines are selected in the same manner. The following are descriptions of the 5223 Option 10 stimulation routines:

Stimulation Routine 0—Kernel Stimulation

This routine repetitively executes the CPU's RAM test which includes read and write operations on the GPIB address selector switches. This is a signature analysis routine and allows testing of the following features:

RAM - U500 and U510
MOS to TTL bus buffer
TTL data bus bit uniqueness
Address selector switch function

Stimulation Routine 1—Self-Test Cycling

This routine causes the 5223 Option 10 to continuously cycle through its power-up self-test routines (except the rear panel self test). During each cycle, the graticule is displayed for approximately 5 seconds, and both SAVE and DISPLAY buttons will illuminate under each of the four possible combinations for the Left vs. Right and VECTOR MODE buttons. The OUTPUT SAVED DISPLAY function is then initiated, and the cycle begins again. This routine is not used in signature analysis troubleshooting.

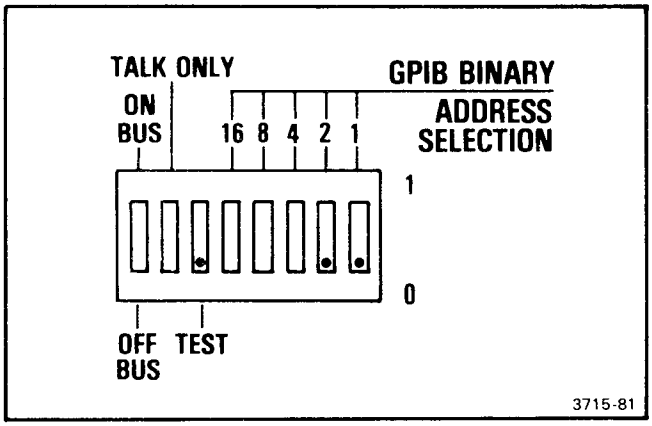


Figure 5-7. GPIB address selection switch. Shows GPIB TEST switch in the ON position and stimulation routine 3 selected.

Stimulation Routine 2—Input Port Test

This routine continuously samples an input port and displays the contents on the front panel LEDs. An input port is selected for sampling by the front panel pushbuttons in the following way: The DISPLAY LEFT, SAVE LEFT, LEFT VS RIGHT, and SAVE RIGHT pushbuttons generate bits 3 through 0, respectively, of an address. The remaining 12 bits of the address are set to hexidecimal 480X.

If this routine is run with the A11-Memory board installed, the DATA OUT RESET signal from the Memory board will prevent the OUTPUT SAVED DISPLAY lamp from illuminating and the XYZ board's pen-lift relay may be overdriven. This routine is not used for signature analysis troubleshooting.

Stimulation Routine 3—Digital-to-Analog Converter Stimulation

This routine is useful when troubleshooting the analog circuitry of the GPIB board and the Chart Out signal path of the XYZ board (with the memory board installed on extenders). This routine has two modes of operation; DC mode and AC mode:

The DC mode (selected when the VECTOR MODE button is in the OUT position) repetitively copies the settings of the remmaining seven (7) front-panel switches to the 7 most significant bits of both the horizontal and vertical digital-to-analog converters on the memory board. Buttons pressed IN copy ones, buttons in the OUT position copy zeros. The DISPLAY LEFT button is copied to the DAC's most significant bits, and each button to the right, up to and including the ROLL button, is copied to a bit of succesively lesser significance. The remaining DAC bits are zeroed.

The AC mode (selected when the VECTOR MODE button is pressed in) applies numbers corresponding to a plus and minus 5-division signal to the DAC inputs, alternating at approximately 100 Hz.

During the operation of this routine, the SAVE LEFT, SAVE RIGHT, LEFT VS RIGHT, and OUTPUT SAVED DISPLAY functions are held ON to activate the Chart Out signal path.

Stimulation Routine 4—Signature Analysis Loop

This routine repetitively generates a sequence of test patterns on all the output ports of the CPU board and performs read operations on input ports 0, 1, and 2. The output patterns are such that, when the Loop-Through board set is installed, all gate inputs on the CPU board, which are not hard-wired to constant levels, are fully exercised with every possible combination of inputs at least once during the loop. Start and Stop pulses are also provided in the loop.

Stimulation Routine 5—Input Port 0 Stimulus

This routine is the same as Stimulation Routine 4, except that input port 0 is the only port read by the processor. All output port signatures remain identical to those for routine 4.

Stimulation Routine 6—Input Port 1 Stimulus

This routine is the same as routine 5, except that input port 1 is read instead of port 0.

Stimulation Routine 7—Input Port 1 Stimulus

This routine is the same as routine 5, except that input port 2 is read instead of port 0.

Stimulation Routine 8—Input Port 1 Stimulus

This routine is the same as routine 5, except that input port 4 is read instead of port 0.

Stimulation Routine 9—Front-Panel Button Stimulus

This routine does not generate patterns on all the output ports. It merely reads the inputs of port 5, which are connected to the front-panel controls, and copies the normally closed contacts to the front panel LEDs. This is done repetitively, along with the generation of start and stop pulses. This separates the signature analysis of the front-panel input port from the rest of the circuitry so the signatues for routines 4 through 8 are not affected by the position of the front-panel buttons.

Stimulation Routine 10—8291 Stimulus

This routine repetitively outputs a "walking one" pattern to the 8291's SRQ Status register, and echoes the data back after each write. Start and Stop pulses are generated for each complete set of output patterns.

Because the GPIB ON/OFF SWITCH applies a hardware RESET to the 8291, it should be in the ON position when this routine is running. Normal oscilloscope operation should not be attempted after this loop is run without completely powering down.

SIGNATURE ANALYSIS TESTS

Signature analysis troubleshooting in the 5223 Option 10 is divided into four parts or tests: "kernel", "RAM", "INPUT/OUTPUT", and "LED-Pushbuttons." Troubleshooting flow-charts (in Appendix B) 1 through 9 comprise the kernel test, 10 through 17 are the RAM test, 18 through 20 are the INPUT/OUTPUT tests, and flow-chart 21 checks the LED-Pushbuttons. The purpose of each of these tests is outlined below.

1. KERNEL TEST (Troubleshooting flow-charts 1-9)—The Kernel test verifies:

a. Power supply voltages.

b. System clock operation.

c. RESET and WAIT operation.

d. That the microprocessor is capable of stepping through its address space (like a 16-bit binary counter) and that there are no faults on A0-A15.

e. That signature analysis CLOCK and START/STOP are functioning properly.

f. Operation of the primary address decoder (U820).

g. That the data bus to the two ROMs is free of faults, the data bus is connected between the ROMs, and that the ROM control signals and contents are correct.

2. RAM TEST (Troubleshooting flow-charts 10-17)—The RAM test verifies:

a. That the microprocessor is able to execute ROM instructions.

b. Proper RAM operation.

c. That there are no shorted address or data lines.

d. That the system data bus is free of faults.

e. That U830 can drive the system data bus.

f. That U110 can drive the system data bus.

g. That U830 can drive the data bus from the system data bus.

3. INPUT/OUTPUT TESTS (Troubleshooting flow-charts 18-20)—The Input/Output test verifies:

a. That outputs can source data.

b. The multiplexers and logic work properly.

c. That the inputs can receive data.

4. LED-PUSHBUTTON TEST (Troubleshooting flow-chart 21)—This test verifies that the LED-pushbuttons operate properly and that the LEDs are functioning.

TEST EQUIPMENT REQUIRED

The following is a list of test equipment required to perform signature analysis troubleshooting on the 5223 Option 10 Digitizing Oscilloscope:

1. SONY/TEKTRONIX 308 Data Analyzer with pull-up resistor options.

2. Digital Voltmeter.

3. Test Oscilloscope.

4. Loop-through board set (067-0966-00).

5. Memory board extender kit (067-0967-00)

CONTROL SIGNALS, TEST POINTS, AND JUMPERS

Signature Analyzer Start, Stop, and Clock control signals are provided on the GPIB board on square pins labeled B, F, and A, respectively. Unless otherwise specified in the signature set tables, the signature analyzer should be set to sample on the negative edge of the clock and have active low levels for the start and stop signals. Test points are also provided for +5 V and GND.

Jumpers which are used in signature analysis troubleshooting are C, D, E, G, and H. When these jumpers are removed; C disables RAM, D and E disable the input and output ports, and G and H disable the interrupts. U710 is an 8-wide strap that connects the microprocessor data bus to the ROMs. Removing U710 causes the microprocessor to free-run (operation code 00).

SET-UP

Once the need to use signature analysis is established, certain steps must be taken to prepare the instrument. Briefly, the A11-Memory board must be removed from the 5223 Option 10 instrument and replaced with the Loop-Through board set. The appropriate signature analysis stimulation routine can then be selected on the GPIB Address selection switches on the rear panel of the instrument. Directions for setting up the instrument for signature analysis is discussed in detail below and should be followed carefully to ensure accurate results.

Remove Memory board—Remove the A11-Memory board and install the Loop-Through board Memory board as follows:

1. Disconnect power—always disconnect power from the instrument before removing and replacing circuit boards.

2. Bench model only (Rackmount procedure begins at step 6)—Remove the protective cabinet panels from the Display unit (see Cabinet Panel Removal at the beginning of this section) then proceed with the following instructions (refer to illustration in Component Removal and Replacement, Fig. 5-13)

3. Slide out the two trim strips to expose the interlock securing hardware.

4. Remove the interlock hardware and remove the interlock (outer).

5. Separate the Display and Acquisition units.

6. Rackmount model only—remove the protective cover from the side and top of the Acquisition Unit.

7. Disconnect all wires and pin connectors which connect the A11-Memory board to other parts in the instrument.

8. Remove the two GPIB Interconnect boards, A16 and A17 from the A11-Memory board edge pins.

9. Remove the board mounting hardware.

10. Separate the interboard pin connectors, then remove the board from the instrument.

11. Install the edge pin extender boards (part of the Tektronix 067-0967-00 memory board Extender kit) to the edge pin connectors on the GPIB board.

12. Install the GPIB Loop-Through board into the extender boards as shown in Figure 5-8.

13. Connect the power leads to the GPIB Loop-Through board, being careful to observe polarity and connect the Loop-Through board cable plug to J15 pins on the GPIB board.

14. Set the rear-panel TEST switch to the ON position (see Fig. 5-7) and select the appropriate signature analysis stimulation routine.

15. Reverse the above instructions to replace the A11-Memory board upon completion of signature analysis troubleshooting. Take care to match the index arrow on the pin connectors to the correspoinding arrow on the circuit board. Correct location of the pin connectors is shown on the circuit board illustrations. Care must also be exercised to align the interboard pin connectors.

Once the 5223 Option 10 is prepared as outlined above, turn to Appendix B to begin signature analysis troubleshooting.

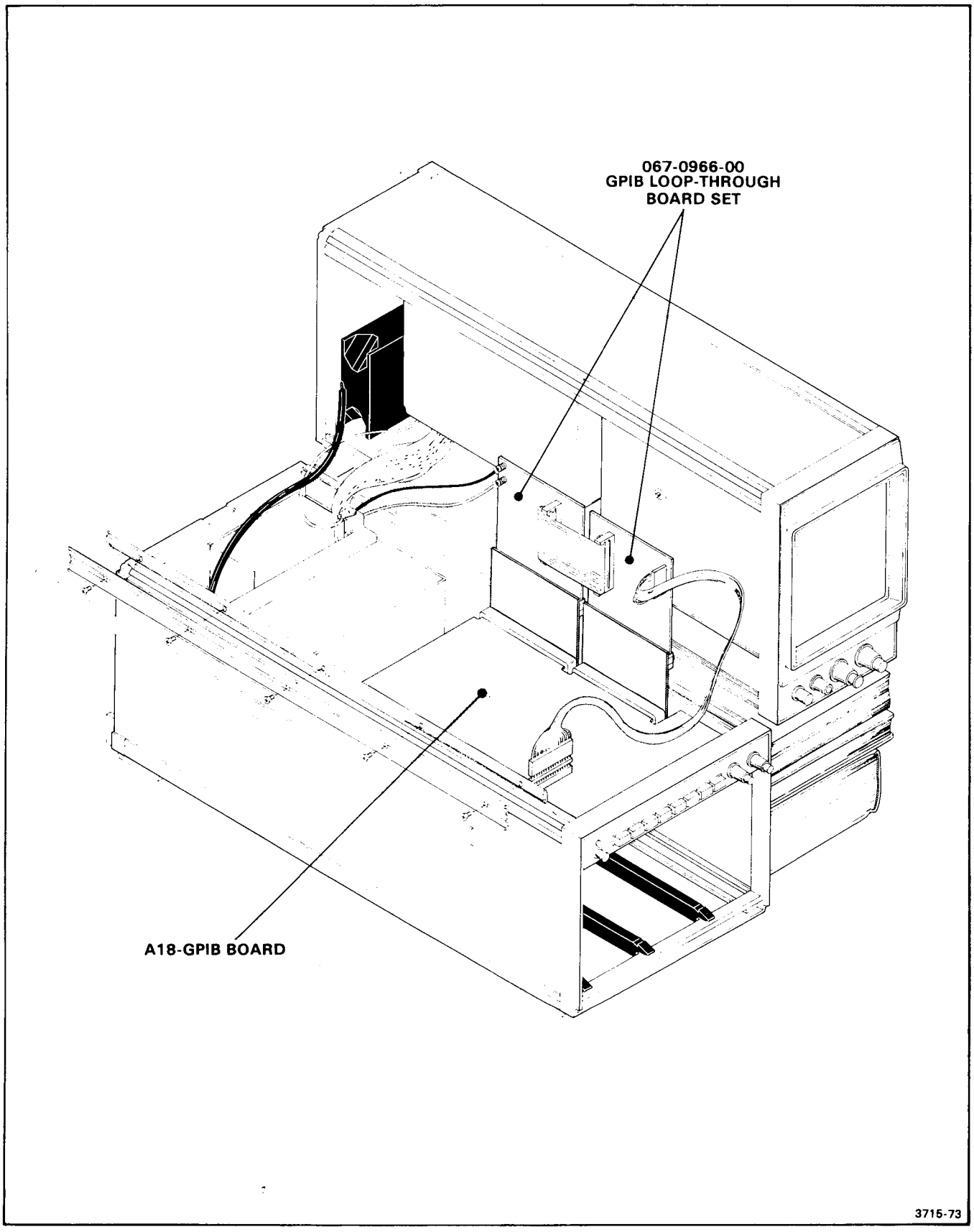


Figure 5-8. GPIB Loop-Through board installed.

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CORRECTIVE MAINTENANCE

Corrective Maintenance consists of component replacement and instrument repair. Special techniques required to replace components in the 5223 Option 10 Digitizing Oscilloscope mainframe are given here.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical part replacements for the 5223 can be obtained through your Tektronix Field Office or representative. However, many of the standard electronic components can be obtained locally.

Some parts are manufactured or selected by Tektronix, Inc. to satisfy particular requirements, or are manufactured for Tektronix, Inc. to our specifications.

Before purchasing a part from a source other than Tektronix, Inc. check the parts list for value, tolerance, rating, and description.

NOTE

When selecting replacement parts, remember that the physical size and shape of a component may affect its performance in the instrument. All replacement parts should be direct replacements unless you know that a different component will not adversly affect instrument performance.

Most of the mechanical parts used in this instrument have been manufactured by Tektronix, Inc. To determine manufacturer of parts, refer to Parts List, Cross Index Mfr. Code Number to Manufacturer.

When ordering replacement parts from Tektronix, Inc., include the following information:

1. Instrument type.

2. Instrument serial number.

3. A description of the part (if electrical, include circuit number).

4. Tektronix part number.

SOLDERING TECHNIQUES

WARNING

To avoid electric-shock hazard, disconnect the instrument from the power source before soldering.

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used when repairing or replacing parts.

The desoldering and removal of parts is especially critical and should be done only with a vacuum solder extractor; further, one approved by a Tektronix, Inc., Service Center.

Use wire solder with rosin core, 63% tin, 37% lead. Contact your local Tektronix, Inc. representative of field office for approved solders.

Several of the circuit boards in this instrument have as many as six (6) layers. Conductive paths between the top and bottom board layers may connect with one or any number of inner layers. Once this inner conductive path is broken (due mainly to poor soldering practices) between the top and bottom layer, the board is unuseable and must be replaced. Damage can void warranty.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum type desoldering equipment, should attempt repair of any board in this instrument. The following multi-layer board assemblies are particularly susceptable to heat damage: A8, A9, A11, A18. Damage can void warranty.

When soldering on circuit boards or small wiring, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron can cause the etched circuit wiring to separate from the board base material, and melt the insulation from small wiring. Always keep the soldering-iron tip properly tinned to ensure the best heat transfer to the solder joint. Apply only enough heat to make a good solder joint. To protect heat-sensitive components, hold the component lead with a pair of long-nose pliers between the component body and the solder joint.

The following technique should be used to replace a component on any of the circuit boards. Most components cannot be removed without first removing the board from the instrument. See the appropriate board removal procedure later in this section.

1. Touch the tip of the vacuum desoldering tool directly to the solder to be removed.

CAUTION

Excessive heat can cause the etched circuit wiring to separate from the board base material.

Never allow the solder extractor to remain on the board for more than three (3) seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for multi-pin components) must not be used. Damage can void warranty.

NOTE

Some components are difficult to remove from the circuit boards due to a bend placed in each lead during machine insertion of the component. The purpose of the bent leads is to hold the component in position during a flow-solder manufacturing process which solders all components at once. To make removal of machine inserted components easier, straighten the leads of the component on the back of the circuit board, using a small screwdriver or pliers.

When removing multi-pin components i.e., IC's, do not heat adjacent conductors consecutively (see Fig. 5-9). Allow a moment for the circuit board to cool before proceeding to the next pin.

CAUTION

Do not allow solder or solder flux to flow under circuit board switches. The printed circuit board is an integral part of the switch and intermittent operation can occur if contaminated.

2. Bend the leads of the replacement components to fit the holes in the circuit board. If the component is replaced while the board is mounted in the instrument, cut the leads so they will just protrude through the board. Insert the leads into the holes in the board so that the component is firmly seated against the board, or as originally positioned.

3. Touch the iron to the connection and apply enough solder to make a firm solder joint.

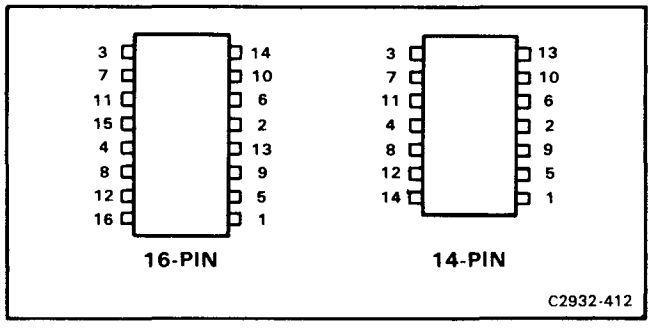

Figure 5-9. Recommended desoldering sequence for multi-pin devices.

4. Cut off any excess lead protruding through the board (if not clipped in step 2).

5. Clean the area around the solder connection with a flux removing solvent. Be careful not to remove information printed on the circuit board.

COMPONENT REMOVAL AND REPLACEMENT

WARNING

To avoid electric-shock hazard, always disconnect the instrument from the power source before removing or replacing components or plug-in units.

The exploded-view drawings associated with the Replaceable Mechanical Parts list (located at the rear of this manual) may be helpful in the removal or disassembly of individual components or sub-assemblies.

POWER-SUPPLY UNIT REMOVAL

The power-supply can be slid out the rear of the 5223 as a unit.

Remove and replace the Power Supply Unit as follows:

1. Remove the power cord.

2. Follow the instructions under Cabinet Panel Removal, (at the beginning of the Maintenance section) then proceed with the following instructions.

3. Separate the Power on switch from the extender shaft.

4. Remove the screws securing the two cable harness clamps to the Power Supply Unit.

5. Disconnect all wires and pin connectors which connect the Power Supply Unit and the A7-Power Supply board to other parts in the instrument.

6. Remove 6 screws (see Fig. 5-10); 4 that hold the Power Supply Unit to the rear frame, and 2 that secure the front of the unit to the frame rails.

7. Remove the Power Supply Unit from the mainframe.

Replace the Power Supply Unit in the reverse order of removal. Match the index arrow on the multi-pin connectors to the corresponding arrow on the A7-Power Supply board. Correct location of the pin connectors is shown on the circuit board illustration in Section 9 Diagrams and Circuit-Board Illustrations.

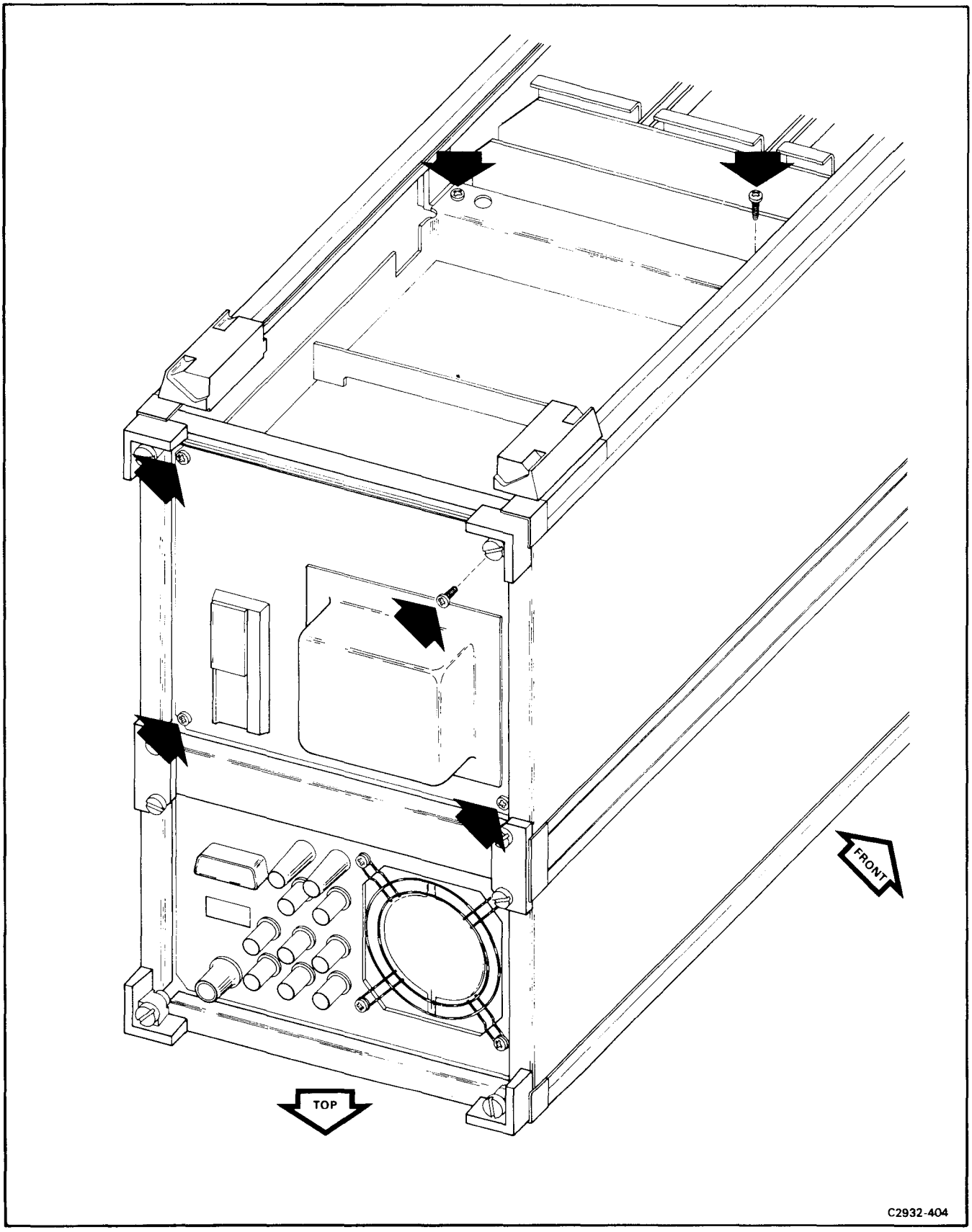

Figure 5-10. Location of screws for Power Supply Unit removal.

CATHODE-RAY TUBE REMOVAL

Remove the cathode-ray tube (crt) as follows (refer to Fig. 5-11):

WARNING

The crt may retain a dangerous electrical charge. Before removing the crt, the anode must be fully discharged by shorting the anode lead from the crt to the chassis. Wait approximately ten minutes and again firmly short this lead to the chassis. Then proceed with the following instructions.

Use care when handling a crt. Breakage of the crt causes a high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses should be worn. Avoid striking the crt on any object which might cause it to crack or implode. When storing a crt, place it in a protective carton or set it face down in a protected location on a smooth surface with a soft mat under the faceplate.

1. Remove the protective panels from the top and side of the Display Unit. The rackmount 5223 requires the bottom panel removed in addition to the top and side panels.

2. Remove the crt base-pin socket and four individual neck pin connectors. Note the location of each.

3. Remove the 4 screws shown in Figure 5-12. Then pull out the H.V. Assembly, locate the focus neck pin and disconnect it from the crt.

4. Remove the plastic opening covers to gain access to the bezel and crt clamp screws.

5. Remove the multi-pin wire connector-to-camera connector.

6. Remove the graticule light assembly (light reflector, spring retainer and A1-Grat Illum board.

7. Loosen each clamp screw 1/4 turn. Then, loosen each clamp screw approximately 2 more turns.

8. Remove the four screws securing the crt bezel to the front panel. Remove the bezel, implosion shield, light filter and camera connector.

9. Hold one hand on the crt faceplate and gently push forward on the crt base with the other. Slowly pull the crt out from the front of the instrument while guiding the crt anode lead through the hole in the crt shield.

CATHODE-RAY TUBE REPLACEMENT

Replace the cathode-ray tube (crt) as follows (refer to Fig. 5-11):

1. Insert the crt into the shield, guiding the crt anode plug through the hole in the crt shield. Assure that the crt clamps are properly aligned.

2. Clean the crt implosion shield, light filter and faceplate with denatured alcohol.

3. Hold the implosion shield in position and replace the crt bezel and camera connector. Firmly tighten the four screws making sure that the implosion shield is properly aligned.

4. Snug up the crt clamp screws. Assure the crt screen is centered before final tightening.

5. Replace the graticule light assembly (light reflector, spring retainer and A1-Grat Illum board).

6. Replace the opening covers, light filter and frame mask.

7. Place the crt base-pin socket on the crt base pins.

8. Reconnect the crt anode plug.

9. Carefully reconnect all cables and crt neck-pin connectors.

10. Replace the H.V. assembly.

11. Replace all protective panels. (Side, top, bottom).

NOTE

Replacement of the crt necessitates re-adjustment of the instrument. Refer to Section 6, Calibration.

CIRCUIT BOARDS

If a circuit board is damaged beyond repair, replace the entire board assembly. Part numbers for completely wired boards are given in Section 8, Replaceable Electrical Parts.

Most of the circuit boards in this instrument are mounted on the chassis; pin connectors are used for electrical interconnection with chassis mounted components and other circuit boards.

The pin connectors, except for coaxial-type connectors, used for interconnection between circuit boards are color-coded to aid in identification and circuit tracing. The color of the connector body matches the resistor color-

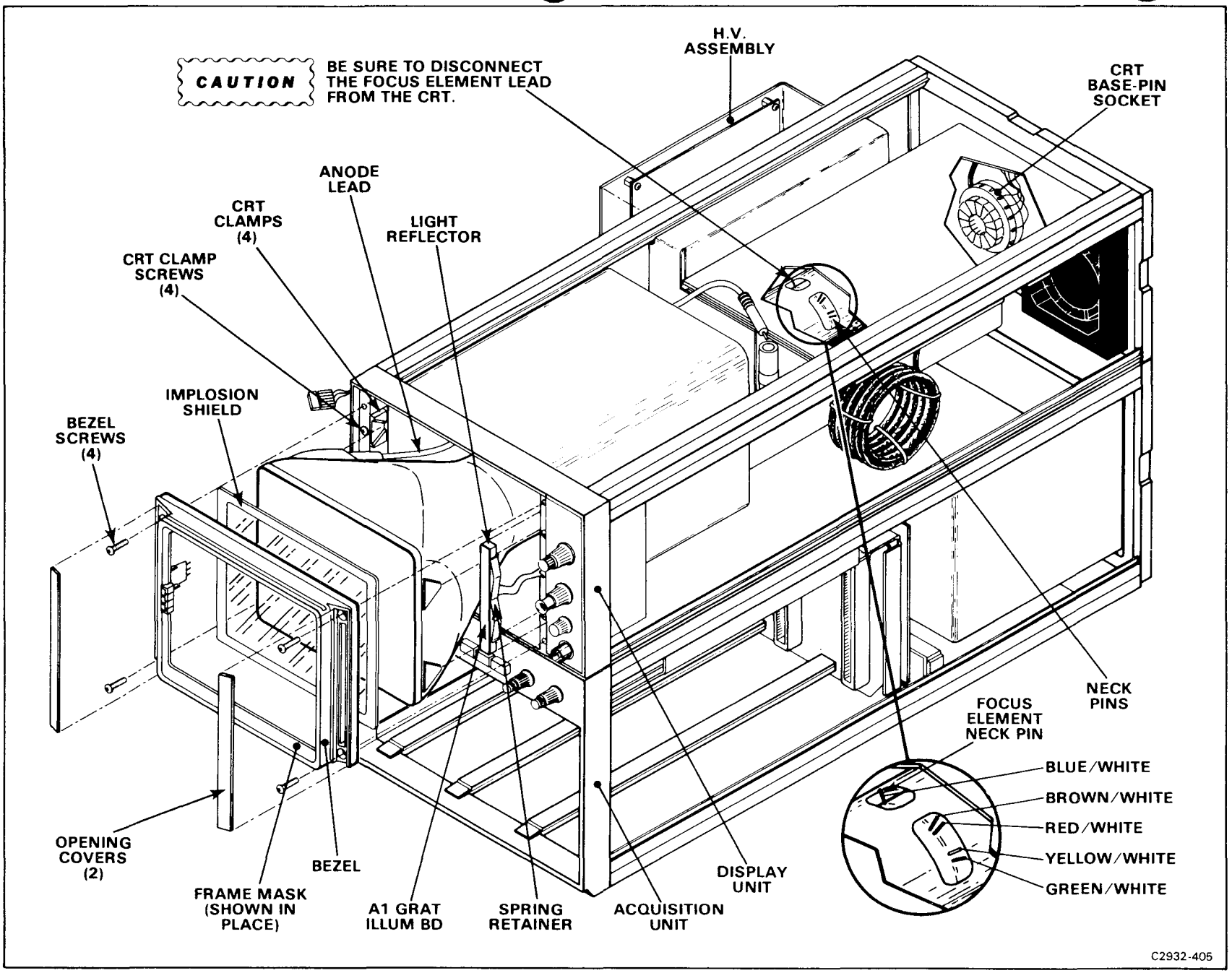

Figure 5-11. Cathode-ray-tube removal and replacement.

code for the last digit of the connector circuit number; e.g., P602 is red, P603 is orange, etc. The exception is the orange harmonica connected to P1 on the A8-Digitizer and A9-Interface board.

NOTE

When removing wires from the circuit board always tag the wire and the corresponding connection point on the circuit board.

A1-GRAT ILLUM BOARD

Remove and replace the A1-Grat Illum board as follows:

1. Remove the power cord from the mainframe.

2. Remove the right (top, if rackmount) display unit protective panel (see Cabinet Panel Removal).

3. Unplug the two wires that connect the A1-Grat Illum board to the A2-Front Panel board (at the A2-Front Panel board end).

4. Remove the right opening cover.

5. Remove the spring retainer (see Fig. 5-11).

6. Pry out the A1-Grat Illum board (including light reflector) with a thin blade screwdriver.

NOTE

The lamps are easily replaced without removing the board. See Soldering Techniques.

Replace the A1-Grat Illum board by reversing the order of removal.

Align the lamps with the appropriate holes in the plastic light reflector. Ensure the unmasked side of the light reflector is towards the crt.

A2-FRONT PANEL BOARD

Remove and replace the A2-Front Panel board as follows:

1. Remove the power cord from the mainframe.

2. Remove the right (top, if rackmount) display unit protective panel from the Display Unit to expose the A2-Front Panel board.

3. Remove the control knobs and mounting hardware from the INTENSITY, FOCUS and GRAT ILLUM pots.

4. Bench model only—remove the plastic cable clamp, then unplug all pin connectors which connect the board to other parts in the instrument.

5. Rackmount model only—Unplug the orange 2-pin harmonica. (The other connectors will be removed in step 7.)

6. Remove the securing hardware, then remove the board from the instrument.

7. Rackmount model only—Remove the plastic cable clamp, then unplug the pin connectors.

Replace the A2-Front Panel board by reversing the order of removal. Match the index arrow on the pin connectors to the coresponding arrow on the board. Correct location of the pin connectors is shown on the circuit board illustration in Section 9, Diagrams and Circuit Board Illustrations.

A3-XYZ BOARD

Remove and replace the A3-XYZ board as follows:

1. Remove the power cord from the mainframe.

2. Remove all protective panels from the Display Unit. If rackmount, also remove the bottom cover of the Acquisition Unit. (See Cabinet Panel Removal).

3. Disengage all pin connectors that connect the A3-XYZ board to other parts in the instrument.

4. Unsolder the delay line leads and remove the associated end connector mounting screw.

5. Remove the securing hardware, then slide the board towards the rear of the instrument.

6. Remove the 4 crt neck pin connectors.

Replace the A3-XYZ board by reversing the order of removal. Match the index arrow on the pin connectors to the corresponding arrow on the board. Correct location of the pin connectors is shown on the circuit board illustration in Section 9, Diagrams and Circuit Board Illustrations.

A4-H.V. BOARD

Remove and replace the A4-H.V. board as follows:

1. Disconnect the power cord from the mainframe.

2. Remove the protective panels from the Display Unit (see Cabinet Panel Removal).

WARNING

To avoid electric shock, always ground the anode lead to the chassis to dissipate any stored charge in the crt and H.V. multiplier.

3. Unplug the anode lead at the coupling on the right side of the Display Unit. Ground the anode lead and H.V. multiplier to the chassis.

4. Remove the screws shown in Figure 5-12; then remove the mounting plate with A4-H.V. board attached.

5. Disengage all pin connectors that connect the A4-H.V. board to other parts in the instrument. Unsolder the 3 wires connected to the power transistor (Q60).

6. Remove the board securing hardware, then separate the A4-H.V. board from the mounting plate.

NOTE

If the A4-H.V. board is to be replaced, the A5 and A6 D.C. Restorer boards must be removed. Follow the procedure for A5 and A6 D.C. Restorer board removal given later in this section.

7. Replace the board by reversing the order of removal. Match the index arrow on the pin connectors to the corresponding arrow on the A3-XYZ board. Correct location of the pin connectors is shown on the circuit board illustration in Section 9, Diagrams and Circuit Board Illustrations.

A5, A6-DC RESTORER BOARDS

Remove and replace the DC Restorer boards as follows:

1. Follow the procedure for A4-H.V. board removal then proceed with the following instructions.

2. Locate the appropriate board mounting pins (on the back side of the A4-H.V. board) then remove the solder and clean the circuit board pads. Follow the procedure given under Soldering Techniques earlier in this section.

3. Disengage the defective board from the mounting holes in the A4-H.V. board.

4. Replace the boards by reversing the order of removal.

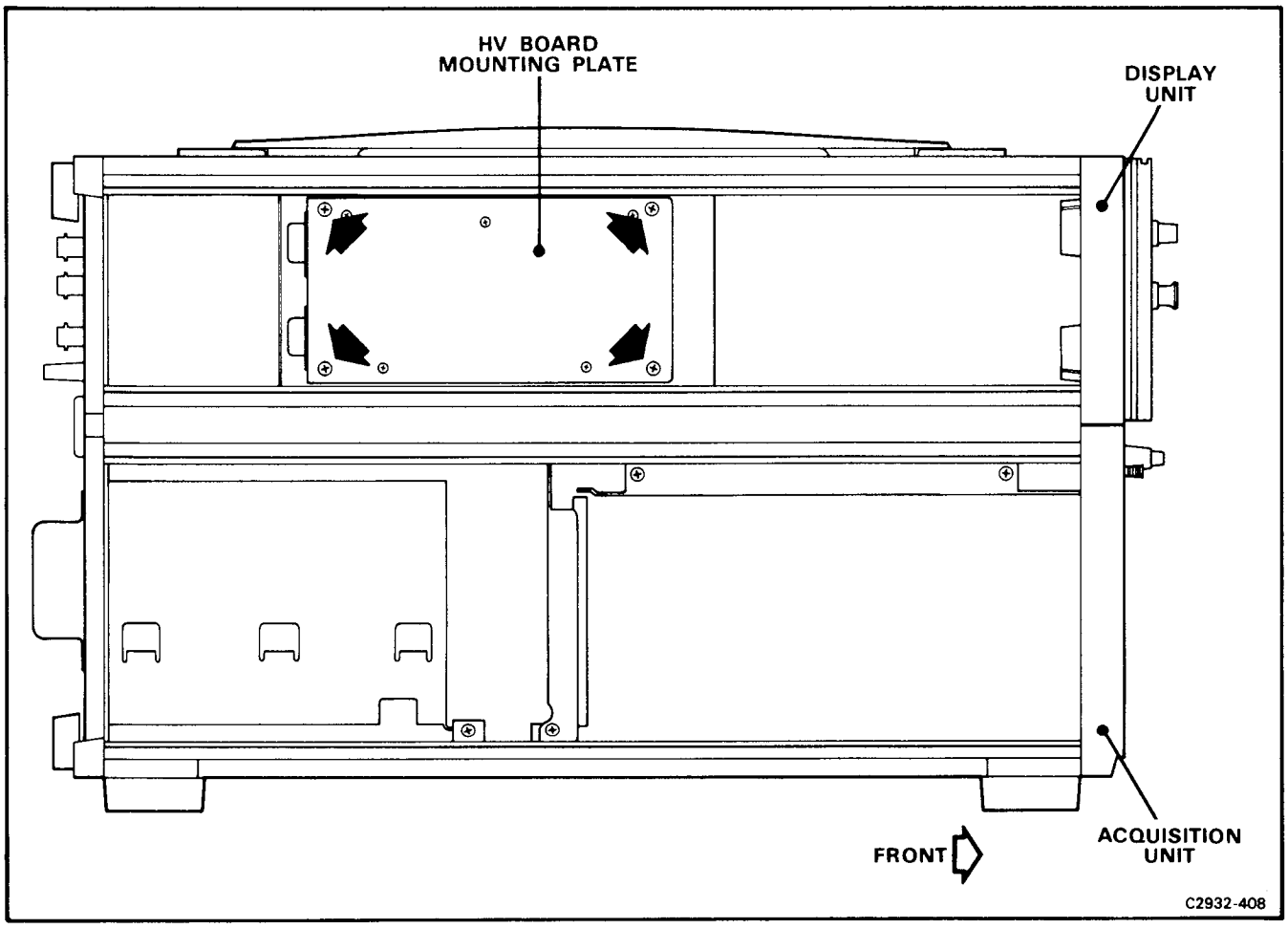

Figure 5-12. Screw locations for A4-H.V. board removal.

A7-POWER SUPPLY BOARD

Replace the A7-Power Supply Board as follows:

1. Follow the Power Supply Unit Removal procedure then proceed with the following instructions.

2. Remove the securing hardware of all transistors and diodes mounted to the chassis (heatsink).

3. Remove the 7 securing screws and lift the board with attached diodes and power transistors from the chassis.

4. Disconnect all wires which connect the board to other components in the Power Supply Unit.

NOTE

When removing wires or components from the circuit board, always tag the wire or component and the corresponding connection point on the circuit board.

5. The transistors and diodes that were mounted to the chassis (their mounting hardware was removed in step 2) must now be unsoldered from the A7-Power Supply board. Follow the procedure given under Soldering Techniques earlier in this section.

NOTE

The chassis mounted diodes and transistors are not part of the A7-Power Supply board. If any chassis mounted component is needed it must be ordered separately.

6. Remove the circuit board stiffener from the board.

Install the A7-Power Supply board as follows:

1. Install the circuit board stiffener. Align the 2 chassis mounting holes before tightening the center screw.

2. Connect all wires that connect the board to other components in the Power Supply Unit.

3. Install the board in the unit. Replace and tighten the securing hardware.

4. Install the chassis mounted transistors and diodes. Check that the power transistors are aligned with their mounting screws and that the insulating washers and heat conductive film (used instead of silicone grease) are in place between the transistor cases and the chassis (heatsink).

5. Solder the diodes and transistors installed in step 4.

6. Check the A7-Power Supply board for correct operation under load. Connect the +5 V sense terminal to the +5 V output and check the regulation of the individual supplies. Use the variable auto-transformer as described in Troubleshooting Equipment earlier in this section.

7. Install the Power Supply Unit in the mainframe.

8. Connect all wires and multi-pin connectors to the board. Match the index arrow on the pin connectors to the corresponding arrow on the board. Correct location of the pin connectors is shown in the circuit board illustration in Section 9, Diagrams and Circuit Board Illustrations.

A8-DIGITIZER BOARD

Remove and replace the A8-Digitizer board as follows:

1. Disconnect all pin connectors which connect the A8-Digitizer board to other parts in the instrument.

2. Remove the 2 mounting screws.

3. Slide the A8-Digitizer board downwards to disengage the pins from the A11-Memory board.

4. Disengage the board from the 2 mounting clips.

5. Remove the board through the right side of the instrument.

Replace the board by reversing the order of removal. Match the index arrow on the pin connectors to the corresponding arrow on the board. Correct location of the pin connectors is shown on the circuit board illustration in Section 9, Diagrams and Circuit Board Illustrations.

A9-INTERFACE BOARD

Remove and replace the A9-Interface board as follows:

1. Remove all plug-ins from the Acquisition Unit.

2. Remove the front grill.

3. Remove the 3 plug-in guides (see Fig. 5-13).

4. Remove the interface board shield (8 screws).

5. Unsolder the delay line cable and remove the associated end-clamp hardware.

6. Disconnect all pin connectors which connect the A9-Interface board to other parts in the instrument.

7. Remove the securing hardware (3/16 socket).

8. Slide the A9-Interface board downwards to disengage the interboard pin connector, then remove the board.

9. Replace the board by reversing the order of removal. Match the index arrow on the pin connectors to the corresponding arrow on the board. Correct location of the pin connectors is shown on the circuit board illustration in Section 9, Diagrams and Circuit Board Illustrations.

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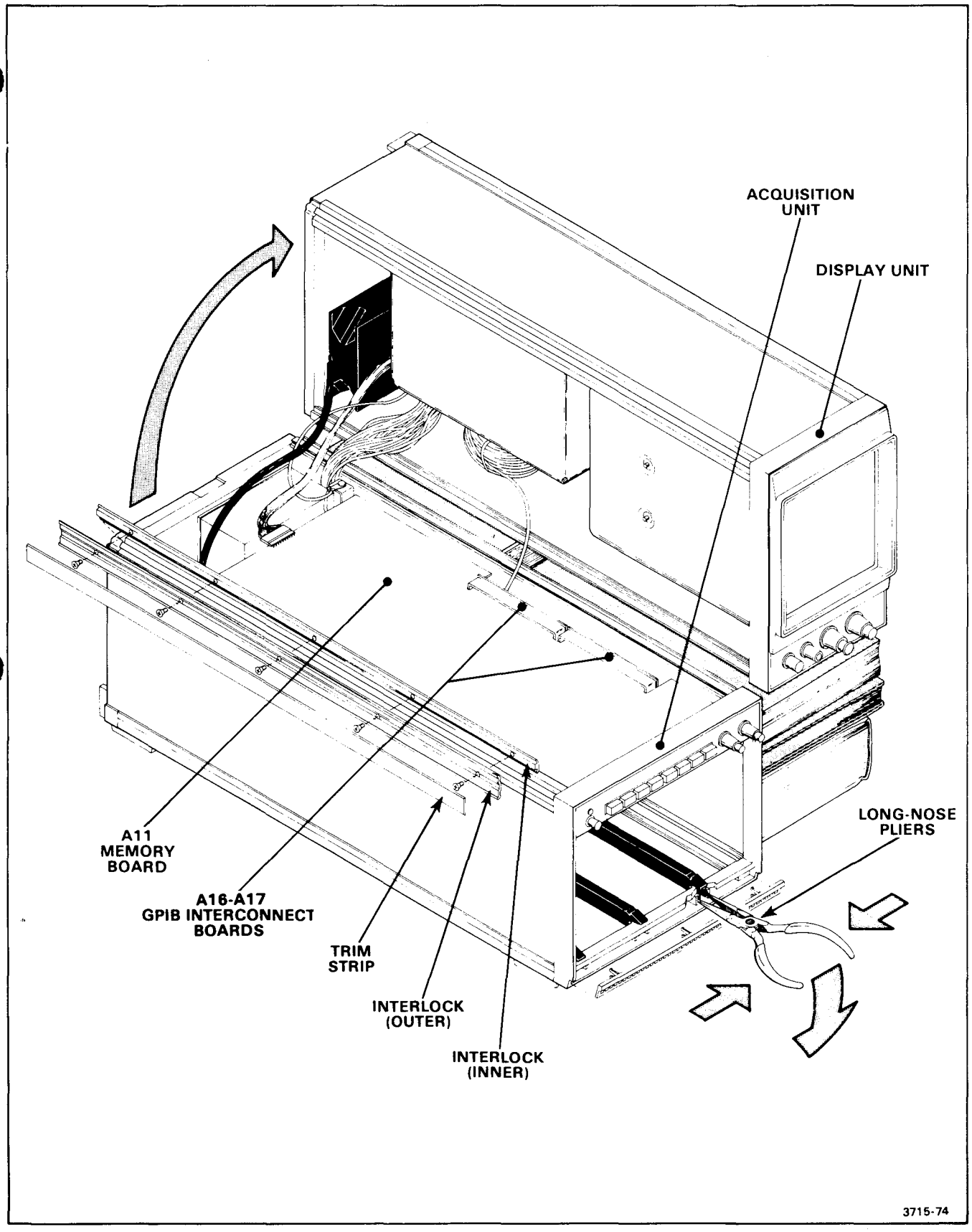


Figure 5-13. A11-Memory board and plug-in guide removal.

A11-MEMORY BOARD

Remove and replace the A11-Memory board as follows:

1. Bench model only (Rackmount procedure begins at step 5)—remove the protective cabinet panels from the Display unit (see Cabinet Panel Removal) then proceed with the following instructions (refer to Fig. 5-13).

2. Slide out the two trim strips to expose the interlock securing hardware.

3. Remove the interlock hardware and remove the interlocks (outer).

4. Separate the Display and Acquisition Units as shown in Figure 5-13.

5. Rackmount model only—remove the protective cover from the side and top of the Acquisition Unit.

6. Disconnect all wires and pin connectors which connect the A11-Memory board to other parts in the instrument.

7. Remove the two GPIB interconnect boards, A16 and A17 from the A11-Memory board edge pins.

8. Remove the board mounting hardware.

9. Separate the interboard pin connectors then remove the board from the instrument.

10. Replace the A11-Memory board by reversing the order of removal. Match the index arrow on the pin connectors to the corresponding arrow on the board. Correct location of the pin connectors is shown on the circuit board illustration in Section 9, Diagrams and Circuit Board Illustrations. Care must be excercised to align the interboard pin connectors.

A14-DRIVER BOARD

Remove and replace the A14-Driver board and the A14-Rear Panel board as follows:

1. Remove the protective cabinet panels from the top and side of the display unit.

2. Remove the securing screw from the A14-Driver board. Pull the circuit board toward the front of the instrument to disengage it from the A15-Rear Panel board connector pins. Disconnect the pin connectors from the A14-Driver board to free it from the instrument.

3. Replace the A14-Driver board by reversing the order of removal. Match the index arrow on the pin connectors to the corresponding arrow on the board. Connect location of the pin connectors is shown on the circuit board illustration in Section 9, Diagrams and Circuit Board Illustrations.

A15-REAR PANEL BOARD

Remove the A15-Rear Panel board as follows:

1. Follow the first 2 steps of the A-14 Driver board removal procedure then proceed with the following instructions.

2. Remove the four (4) securing screws located at the corners of the GPIB connector plug on the rear panel. This frees the A15-Rear Panel board for removal.

3. Replace the A15-Rear Panel board by reversing the order of removal.

A16, A17-GPIB INTERCONNECT BOARDS

Remove and replace the A16, A17 GPIB Interconnect boards as follows:

1. Follow the first 5 steps of the A11-Memory board removal procedure then proceed with the following instructions.

2. Carefully pry (use your fingers) the board from the A11-Memory board edge-pin connectors.

3. Replace the A16, A17 GPIB Interconnect boards by reversing the order of removal.

A18-GPIB BOARD

Remove and replace the A18-GPIB board as follows:

1. Follow the procedure for A11-Memory board removal, then proceed with the following instructions.

2. Remove the vertical and horizontal position control knobs.

3. Disconnect all wires and connectors which connect the A18-GPIB board to other parts of the instrument.

4. Remove the mounting hardware. The mounting hardware is accessible through the plug-in compartment.

5. Replace the A18-GPIB board by reversing the order of removal.

SEMICONDUCTORS

Semiconductors should not be replaced unless actually defective. If removed from their sockets during routine maintenance, return them to their original sockets. Unnecessary replacement of semiconductors may affect the adjustment of the instrument. When semiconductors are replaced, check the operation of circuits which may be affected.

WARNING

To avoid electric shock hazard, always disconnect the 5223 from the power source before removing or replacing components.

Replacement semiconductors should be of the original type or a direct replacement. Lead configurations of the semiconductors used in this instrument are shown in Figure 5-3. Some plastic case transistors have lead configurations which do not agree with those shown. If a replacement transistor is made by a different manufacturer than the original, check the manufacturer's basing diagram. Transistor sockets in this instrument are wired for standard basing as used for metal-cased transistors. When removing soldered-on transistors, follow the procedure given in Soldering Techniques earlier in this section.

To replace one of the Power transistors mounted on the heatsink (chassis) of the Power-Supply Unit, first remove the mounting hardware. Then, unsolder and remove the defective transistor. When replacing the transistor, be sure to install the insulating washer and the heat conductive silicone washer between the transistor and the heatsink. Tighten the mounting nut just tight enough to hold the transistor in place. Then solder the replacement transistor leads to the circuit board.

An extracting tool should be used to remove the in-line integrated circuits to prevent damaging the pins. This tool is available from Tektronix, Inc.; order Tektronix Part 003-0619-00. If an extracting tool is not available, use care to avoid damaging the pins. Pull slowly and evenly on both ends of the integrated circuit. Try to avoid disengaging one end from the socket before the other end.

INTERCONNECTING PINS

Two methods of interconnection are used in this instrument to electrically connect the circuit boards with other boards and components. When the interconnection is made with a coaxial cable, a special end-lead connector plugs into a socket on the board. Other interconnections are made with a pin soldered into the board. Two types of mating connectors are used for these interconnecting pins. If the mating connector is mounted on a plug-on circuit board, a special socket is soldered into the board. If the mating connector is on the end of a lead, an end-lead pin connector is used which mates with the interconnecting pin. The following information provides the removal and replacement procedure for the various types of interconnecting methods.

CAUTION

Do not proceed with the following instructions until the information in Soldering Techniques has been read. Negligence can void warranty.

Coaxial-Type End-Lead Connectors

Replacement of the coaxial-type end-lead connectors requires special tools and techniques; only experienced maintenance personnel should attempt to remove or replace these connectors. We recommend that the damaged cable or wiring harness be replaced as a unit. For cable or wiring harness part numbers, see Section 11, Replaceable Mechanical Parts. An alternative solution is to refer the replacement of the defective connector to your local Tektronix Field Office or representative. Figure 5-14 gives an exploded view of a coaxial end-lead connector assembly.

Circuit-Board Pins

A circuit-board pin replacement kit (including necessary tools, instructions, and replacement pins with attached ferrules) is available from Tektronix, Inc. Order Tektronix Part 040-0542-00. Replacing circuit-board pins on multi-layer boards is not recommended. (The multi-layer boards in this instrument are listed under Soldering Techniques in this section.)

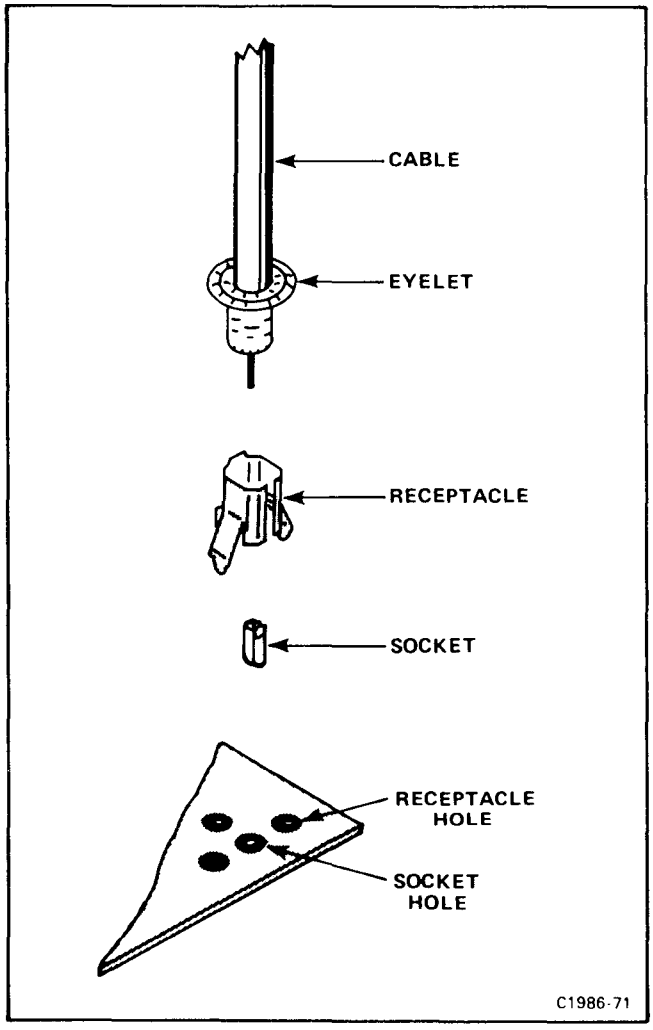


Figure 5-14. Coaxial end-lead connector assembly.

To replace a damaged pin, first disconnect any pin connectors. Then unsolder the damaged pin and pull it from the board with a pair of pliers, leaving the ferrule (see Fig. 5-15) in the circuit board if possible. If the ferrule remains in the circuit board, remove the spare ferrule from the replacement pin and press the new pin into the hole in the circuit board. If the ferrule is removed with the damaged pin, clean out the hole then press the replacement pin, with attached spare ferrule, into the circuit board. Position the replacement pin in the same manner as the original. Solder the pin to the circuit board on each side of the board. If the original pin was bent at an angle to mate with a connector, carefully bend the new pin to the same angle. Replace the pin connector.

Circuit-Board Pin Sockets

The pin sockets on the circuit boards are soldered to the back of the board. To remove or replace one of these sockets, first unsolder the pin (use a vacuum-type desoldering tool to remove excess solder). Then straighten the tabs on the socket and remove the socket from the board. Place the new socket in the circuit board hole and press the tabs down against the board. Solder the tabs of the socket to the circuit boards; be careful not to get solder inside the socket.

NOTE

The spring tension of the pin sockets ensures a good connection between the circuit board and the pin. This spring tension can be destroyed by using the pin sockets as a connecting point for spring-loaded probe tips, alligator clips, etc.

Multi-Pin Connectors

The pin connectors used to connect the wires to the interconnecting pins are clamped to the ends of the associated leads. To remove or replace damaged multi-pin connectors, remove the old pin connector from the end of the lead and clamp the replacement connector to the lead.

NOTE

Some multi-pin connectors are equipped with a special locking mechanism. These connectors cannot be removed by pulling on the wire(s). To remove the connectors from the pin(s) grasp the plastic holder and pull.

To remove an individual wire from the holder insert a scribe in the hole on the side of the holder and slide the extended portion under the holder. This will allow the wire to be removed from the holder.

Some of the pin connectors are grouped together and mounted in a plastic holder; the overall result is that these connectors are removed and installed as a multi-pin connector (see Troubleshooting Aids). If the individual end-lead pin connectors are removed from the plastic holder, note the order of the individual wires for correct replacement in the holder.

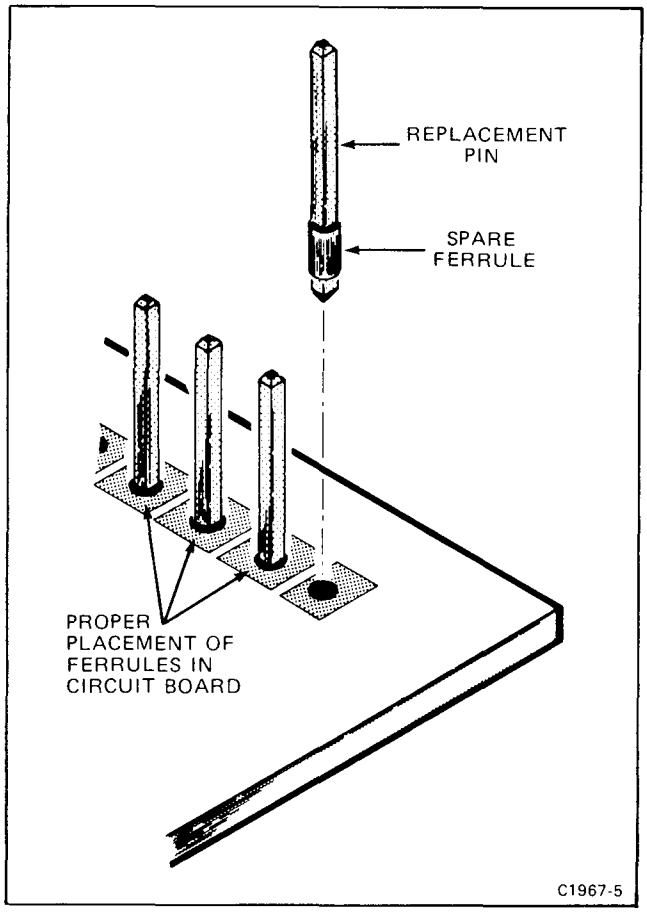


Figure 5-15. Exploded view of circuit-board pin and ferrule.

PUSHBUTTON SWITCHES

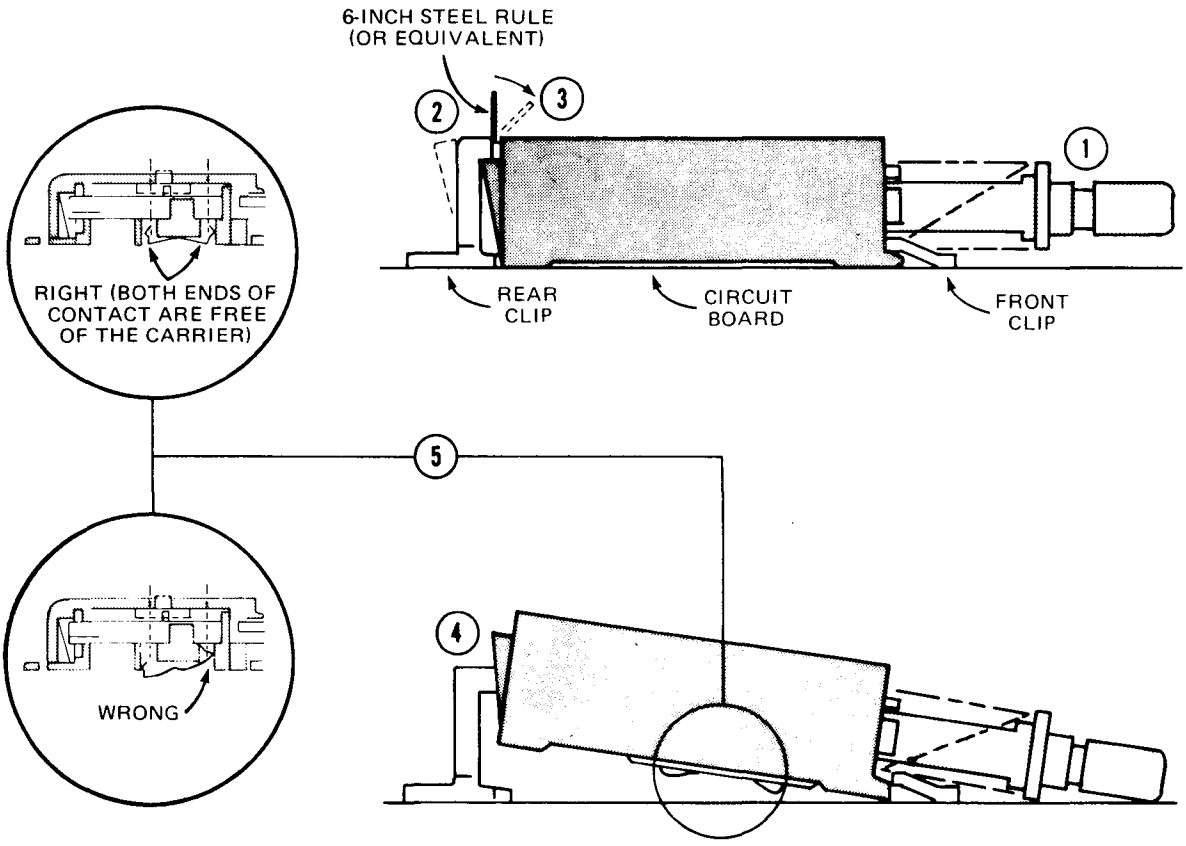
CAUTION

Use only denatured alcohol to clean switch contacts.

The pushbutton switches used on the 5223 Digitizing Oscilloscope mainframe are circuit board mounted. First remove the associated circuit board following the procedure given under Circuit Boards in this section. Figure 5-16 gives removal and replacement instructions for the pushbutton switches.

ADJUSTMENT AFTER REPAIR

After any electrical component has been replaced, the adjustment of that particular circuit should be checked, as well as the adjustment of any closely related circuits. Since the low-voltage supplies affect all circuits, adjustment of the entire instrument should be checked if component replacements have been made in these supplies or if the power transformer has been replaced. See Section 6, Calibration, for a complete adjustment procedure.



(1) Make sure that all switch shafts are in the OUT position to clear the rear clip.

(2) Place the long edge of a six-inch rule or similar thin straight edge between the top edge of the rear clip and the switch body.

(3) Carefully pry the rear clip back just far enough to push the steel rule down between the clip and switch body.

CAUTION

When the switch is removed, the contacts may drop free and be damaged or lost. Body salts or acids can contaminate the switch contacts. Wear cotton gloves to prevent touching the contacts in the switch or on the board with bare hands.

(4) Pull the rear of the switch up, remove the steel rule, and pull the switch out of the front clip.

(5) To replace the switch, first check that the slide contacts are properly installed in the carrier. Then, place the front of the switch into the front clip and push the rear of the switch down until the rear clip catches and holds the switch in place.

C1967-3

Figure 5-16. Removal procedure for pushbutton switches.

CALIBRATION

This section provides procedures for calibrating this instrument. These procedures are designed to compare the performance of this instrument with measurement instruments of known accuracy to detect, correlate, or eliminate by adjustment, any variation from the electrical specifications. These procedures also verify that the controls function properly.

This section is divided into two parts: Part I—Performance Check is provided for those who wish to verify that this instrument meets the applicable electrical specifications in section 1 without making internal adjustments. Part II—Adjustment and Performance Check provides a complete calibration procedure that includes adjustments and performance checks in addition to verifying that the controls function properly. The procedures in Part I and Part II are written so that the entire instrument, or any major circuit or part of a circuit, can be checked or adjusted.

Table 6-1, Calibration Procedure Electives, lists the choices available and instructions for performing complete or partial calibration procedures. Also refer to page 6-2, Using These Procedures, for more detailed information.

TABLE 6-1
Calibration Procedure Electives

Electives	Procedures
Functional Check	1. A functional check only is provided in the Checkout Procedure in the Operators Manual, and in section 1 of this manual.
	2. Also, a functional check is accomplished by performing Part II—Adjustment and Performance Check.
Performance Check Only	Perform Part I—Performance Check.
Complete Calibration	Perform Part II—Adjustment and Performance Check.
Partial Procedures	Proceed to the desired step(s) (e.g., A2, A3, B2, B3, etc,; as listed in the Index to Part I—Performance Check or Index to Part II—Adjustment and Performance Check). **NOTE** *When adjustments are made, it is recommended that the entire, major functional circuit procedure be performed.*

USING THESE PROCEDURES

NOTE

In these procedures, capital letters are used within the body of the text to identify front-panel controls, indicators, and connectors on the 5223 (e.g., INTENSITY). Initial capitalization is used to identify all the associated test equipment and their controls, indicators, and connectors (e.g., Triggering) used in the procedures. Initial capitalization is also used to identify adjustments internal to the 5223 (e.g., Geometry).

These procedures are divided into subsections by major functional circuits (e.g. A. Power Supply, B. Real-Time Display, etc.). The order in which the subsections and procedures appear is the recommended sequence for a complete performance check or calibration of the instrument.

The first step in each subsection (A1, B1, C1, etc.) contains reference information and Setup Conditions that must be performed before proceeding.

The Setup Conditions provide equipment connection information and control settings for both this instrument and any associated test equipment. Also, the Setup Conditions are written so that if desired, each subsection (A, B, C, etc.) or step (A2, A3, B2, B3, etc.) can be performed independently.

The alphabetical instructions under each step (a, b, c, etc.) may contain CHECK, EXAMINE, ADJUST, or INTERACTION as the first word of the instruction. These terms are defined as follows:

1. **CHECK**—indicates the instruction accomplishes an electrical specification check. Each electrical specification checked is listed in Table 6-2, Performance Check Summary (see the Performance Check Summary discussion for more information).

2. **EXAMINE**—usually precedes an ADJUST instruction and indicates that the instruction determines whether adjustment is necessary. If no ADJUST instruction appears in the same step, the EXAMINE instruction concerns measurement limits that do not have a related adjustment. Measurement limits following the word EXAMINE are not to be interpreted as electrical specifications. They are provided as indicators of a properly functioning instrument and to aid in the adjustment process.

3. **ADJUST**—describes which adjustment to make and the desired result. It is recommended that adjustments not be made if a previous CHECK or EXAMINE instruction indicates that no adjustment is necessary.

4. **INTERACTION**—indicates that the adjustment described in the preceding instruction interacts with other circuits. The nature of the interaction is described and reference is made to the step(s) affected.

PERFORMANCE CHECK SUMMARY

Table 6-2, Performance Check Summary, lists the electrical specifications that are checked in Part I and Part II of this section. Table 6-2 is intended to provide a convenient means for locating the procedures in Part I and Part II that check and/or adjust the instrument to meet the applicable electrical specifications. For example: if the Vertical Amplifier had been repaired, use Table 6-2 to locate the electrical specifications affected by the repair. Then, note the title of the procedure in Part I or Part II in which those specifications are checked and/or adjusted. Use the index provided at the front of Part I and Part II to determine the page number of the desired procedures.

TABLE 6-2
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
VERTICAL AND HORIZONTAL			
Bandwidth (With 067-0680-00 Calibration Fixture)			
Vertical			
Real Time and Stored	Dc to at least 12 MHz, with 8 div reference.	A6. Check Vertical Amplifier 12 Megahertz Gain. B5. Check Digitizer Bandwidth.	B8. Check Vertical Amplifier 12 Megahertz Gain. C8. Check Digitizer Bandwidth.
Horizontal			
Real Time	Dc to at least 7 MHz, with 8 div reference.	A8. Check Horizontal Bandwidth.	B10. Check Horizontal Bandwidth.
Maximum Horizontal Calibrated Sweep Rate			
Real Time	20 ns/div	A7. Check Horizontal Timing.	B9. Check Horizontal Timing.
Vertical Aberrations			
Real Time and Stored	3% or less, peak-to-peak with display centered. (Both + and −5 division steps from 067-0680-00 Calibration Fixture.)	A5. Check Vertical Amplifier Step Response. B6. Check Digitizer Aberrations and Blowby.	B7. Check/Adjust Vertical Amplifier Step Response. C9. Check Digitizer Aberrations and Blowby.
Vertical Signal Accuracy (With 067-0680-00 Calibration Fixture)			
Real Time	±1%.	A4. Check Vertical and Horizontal Real-Time Gain, Low Frequency Linearity, and Beamfinder.	B6. Check/Adjust Vertical Real-Time Gain, and Beamfinder.
Stored	±3%.	B3. Check Digitizer Gain, Centering and Monotonicity.	C6. Check/Adjust Digitizer Gain, Left and Right Centering and Monotonicity.
Interface—GPIB	0.5 mV/code ±1%.	Verified at the factory.	C10. Examine GPIB Operation.
GPIB—CRT	0.01 div/code or address ±2%.		

TABLE 6-2 (CONT)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
VERTICAL AND HORIZONTAL (Cont)			
Chart Output	200 mV/div ±5%.	C4. Check Right Vertical, Left Vertical, Horizontal, A Gate Out or Sample Clock Out and Memory X and Y Display Outputs.	D5. Check Right Vertical Left Vertical, Horizontal, A Gate Out or Sample Clock Out and Memory X and Y Display Outputs.
GPIB—Chart Output	2 mV/code or address ±4%.		
DC Gain Match			
Real Time vs Stored Horizontally	Within ±2%.	B2. Check Memory Display Out Gain.	C4. Check/Adjust Memory Display Out
Real Time vs Stored (With Calibrated 5B25N at 0.5 ms/div)	Within ±3%.	B3. Check Digitizer Gain, Centering and Monotonicity.	C6. Check/Adjust Digitizer Gain, Left and Right Centering and Monotonicity.
Left Vert vs Right Vert Real Time	Within ±1%.	B2. Check Memory Display Out Gain.	C4. Check/Adjust Memory Display Out Gain.
Vertical Low Frequency Linearity			
Real Time, Stored and Chart Output	±0.2 div or less error over any two divisions of the graticule area (measured with 067-0680-00 in "Gain" position).	A4. Check Vertical Real-Time Gain, Low Frequency Linearity, and Beamfinder.	B6. Check/Adjust Vertical Real-Time Gain, Low Frequency Linearity and Beamfinder.
Horizontal Low Frequency Linearity			
Real Time	±0.15 div or less over any one division of center 8 divisions of the graticule area, when adjusted for no error on second and tenth graticule lines (measured with 067-0680-00).	A3. Check Geometry, Horizontal Real-Time Gain and Low Frequency Linearity.	B5. Check/Adjust Geometry, Horizontal Real-Time Gain and Low Frequency Linearity.
Vertical Dynamic Range			
Right Vertical Stored	At least ±5 div.	B3. Check Digitizer Gain, Centering and Monotonicity.	C6. Check/Adjust Digitizer Gain, Left and Right Centering, and Monotonicity.

TABLE 6-2 (CONT)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
VERTICAL AND HORIZONTAL (Cont)			
Left Vertical Stored	At least ±4 div.	B3. Check Digitizer Gain, Centering and Monotonicity.	C6. Check/Adjust Digitizer Gain, Left and Right Centering, and Monotonicity.
Vertical Delay Line Real Time	Permits viewing leading edge of displayed waveform.	A5. Check Vertical Amplifier Step Response.	B7 Examine/Adjust Vertical Amplifier Step Response.
XY Operation Real Time	Less than 2 degrees phase shift, dc to 20 kHz, between horizontal commpartment and either vertical compartment.	A9. Check XY Operation.	B11. Check XY Operation.
Left Vert vs Right Vert Stored (Single Channel only; except at 100 μs/div) with two 5A38's, 5A45's or 5A48's	Less than 5 degrees phase shift between vertical compartments at 10 MHz.	Verified at the factory.	
Vertical Digitizer Resolution	0.01 division (10 bits).		
Maximum Digitizing Rate	1 mega-sample per second, for one vertical compartment only. 1/2 mega-sample per second, for both vertical compartments.		
Real Time Channel Switching With 5B25N Time Base set to 0.1 ms/div range or slower Chop Switching Rate	Time/Division ÷ 100 Chop clock is trailing edge (positive-going) of sample pulse.		
Chop Blanking Duration	450 to 600 ns.		

TABLE 6-2 (CONT)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
VERTICAL AND HORIZONTAL (Cont)			
Real Time Channel Switching (cont)			
Alternate Swiching Rate	Channel switches at end of each sweep.	Verified at the factory.	
With 5B25N Time Base at 50 μs/div range or faster in Chop or Alternate	Channel switches at end		
Without Digitizer Time Base or with 5B25N in Amplifier Mode			
Chop Switching Rate	300 kHz ±25%.		
Chop Blanking Duration	Less than 50%.		
Alternate Switching Rate	Channel switches at end of each sweep.		
Vertical Switching Sequence (Chop or Alt)	Each vertical plug-in compartment (in chop or alternate) is allocated two segments for display. Thus, if two dual-channel plug-ins are installed, the display sequence is left CH 1, right CH 1, left CH 2, right CH 2. If a single channel plug-in is installed, or selected, the display defaults to all the segments allocated to that plug-in.		
Horizontal Channel Switching (Chop or Alt)	The channel switch for the horizontal plug-in compartment operates at the same rate as the left/right vertical channel		

TABLE 6-2 (CONT)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
VERTICAL AND HORIZONTAL (Cont)			
Horizontal Channel Switching (cont)	switch. When using a dual-channel plug-in (amplifier or time-base), the display sequence is A, B, A, B... (CH 1, CH 2, CH 1, CH 2). is slaved to Left Vertical compartment and time base B (or CH 2) is slaved to Right Vertical compartment.	Verified at the factory.	
Z-AXIS AMPLIFIER			
External Input			
Input Voltage	A voltage swing of 5 V (dynamic range + to −5 V) will fully modulate beam, dc to 1 MHz with intensity control set as necessary.	C5. Check Z-Axis, SS Reset and Pin Lift Outputs.	D6. Check Z-Axis, SS Reset and Pin Lift Outputs.
Useable Frequency Range	Dc to 5 MHz.	Verified at the factory.	
Input Impedance	Resistance, 10 k ±10%. Capacitance, 50 pF maximum.		
Maximum Safe Input	40 V (dc + peak ac).		
CRT DISPLAY			
Geometry	Bowing or tilt ≤0.1 division.	A3. Check Geometry, Horizontal Real-Time Gain and Low Frequency Linearity.	B5. Check/Adjust Geometry, Horizontal Real-Time Gain, and Low Frequency Linearity.
Orthogonality	±0.2 division total variation over 8 divisions.		
Linearity	With a normal 8 × 10 div raster or time markers, max deviation from straight line: horizontal 0.1 division; vertical 0.1 division.		
Phosphor	P31.	Verified at the factory.	
Deflection	Electrostatic with mesh magnification.		

TABLE 6-2 (CONT)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
CRT DISPLAY (Cont)			
Acceleration Potential	15 kV overall.	Verified at the factory.	
Graticule			
Scale	8 × 10 divisions with 1.22 cm/division.		
Scale Color and Type	Orange internal-graticule lines, with 5-division risetime markings.		
Beamfinder	Brings trace within graticule area and increase trace intensity to a visible level.	A4. Check Vertical Real-Time Gain, Low Frequency Linearity and Beamfinder.	B6. Check/Adjust Vertical Real-Time Gain, Low Frequency Linearity and Beamfinder.
MEMORY			
Memory Length	1 K data points per vertical compartment, shared by multiple trace plug-ins.	Verified at the factory.	
Pretrigger Marker	Waveform is intensified prior to trigger point.		
ROLL MODE	Operative at 100 ms/div and slower.		
DISPLAY OUTPUTS (Chart Output)			
Maximum Clock Rate	220 Hz ±30%.		
Minimum Clock Rate	14 Hz ±20%.		
Impedance	1 kΩ ±10%.		
Amplitude	200 mV/div ±5%.		
PEN LIFT			
Normally Open	Relay closes during each MEMORY waveform output.	C5. Check Z-Axis, SS Reset and Pen Lift Outputs.	D6. Check Z-Axis, SS Reset and Pen Lift Outputs.
Duration	300 ms minimum, 1.5 s maximum.	Verified at the factory.	
Maximum Voltage	30 V, dc or peak ac.		

TABLE 6-2 (CONT)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
MEMORY (Cont)			
PEN LIFT (cont)			
Maximum Current	200 mA, dc or peak ac.	Verified at the factory.	
Maximum VA	5.		
POWER SUPPLY			
Line Voltage Ranges (RMS)	90-117 V. 102-132 V. 191-249 V. 204-250 V maximum.	Verified at the factory.	
CALIBRATOR			
Voltage	300 mV, ±1%.	Requires performing step D2 of Part II-Adjustment and Performance Check.	D2. Check Calibrator Output Voltage.
Current	3 mA, ±1%.	Verified at the factory.	
Frequency	1 kHz, ±1%.	C2. Check Calibrator 1 kHz Repetition Rate.	D3. Check/Adjust Calibrator 1 kHz Repetition Rate.
Duty Cycle	50%, ±2%.	C3. Check Calibrator Duty Cycle.	D4. Check Calibrator Duty Cycle.
Output Impedance	100 Ω, ±1%.	Verified at the factory.	
CONNECTORS			
Camera Power	Three-contact connector compatible with TEKTRONIX C59 camera.	C5. Check Z-Axis, SS Reset and Pen Lift Outputs	D6. Check Z-Axis, SS Reset and Pen Lift Outputs.
PLUG-IN OUTPUTS			
Amplitude	50 mV/div ±5%.	B2. Check Memory Display Out Gain.	C4. Check/Adjust Memory Display Out Gain.
Bandwidth		Verified at the factory.	
Vertical	At least 15 MHz.		
Horizontal	At least 7.0 MHz.		
Output Impedance	50 Ω ±10%.		
Offset	±100 mV (no load).		

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TABLE 6-2 (CONT)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
CONNECTORS (Cont)			
Output Impedance (cont)			
Noise and Crosstalk Between Any Plug-In Combination (Reference 8 Div Input)	Less than 5 mV (dc to 5 MHz). Less than 10 mV (dc to 20 MHz). Less than 25 mV (dc to 100 MHz).	Verified at the factory.	
SS RESET INPUT (Single-Sweep Reset)	Rear panel connector and camera bezel connector. Closure to ground causes reset.	C5. Check Z-Axis, SS Reset and Pen Lift Outputs.	D6. Check Z-Axis, SS Reset and Pen Lift Outputs.
A GATE OUT OR SAMPLE CLK OUT			
Amplitude	0.8 V max low to 2.4 V.	C4. Check Right Vertical, Left Vertical, Horizontal, A Gate Out or Sample Clock Out and Memory X and Y Display Outputs.	D5. Check Right Vertical, Left Vertical, Horizontal, A Gate Out or Sample Clock Out and Memory X and Y Display Outputs.
Rise Time		C4. Check-Right Vertical, Left Vertical, Horizontal A Gate Out or Sample Clock Out and Memory X and Y Display Outputs.	D5. Check Right Vertical, Left Vertical, Horizontal, A Gate Out or Sample Clock Out and Memory X and Y Display Outputs.
From 0.8 V to 2.0 V with 50 pF and 1 MΩ Load			
SAMPLE CLK OUT	50 ns.		
A GATE OUT	100 ns max.		
GPIB INTERFACE			
Functions Implemented (As per IEEE 488-1978)	Description	Verified at the factory.	
SH1	Complete Source Handshake Capability.		
AH1	Complete Acceptor Handshake Capability		
T5	Complete Talk Function.		
L4	Listen Function w/o Listen Only Mode.		

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TABLE 6-2 (CONT)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
GPIB INTERFACE (Cont)			
SR1	Complete Service Request Capability.	Verified at the factory.	
RL2	Remote/Local Function w/o Local Lockout.		
PP0	No Parallel Poll Capability.		
DC1	Complete Device Clear Capability.		
DT0	No Device Trigger Capability.		
C0	No Controller Capability.		
E1	Open Collector Bus Drivers.		

ADJUSTMENT INTERVAL

To maintain instrument accuracy, check performance every 1000 hours of operation, or every 6 months if used infrequently. Before complete adjustment, thoroughly clean and inspect this instrument as outlined in the Maintenance section.

TEKTRONIX FIELD SERVICE

Tektronix Field Service Centers and the Factory Service Center provide instrument repair and adjustment services. Contact your Tektronix Field Office or representative for further information.

TEST EQUIPMENT REQUIRED

The test equipment listed in Table 6-3 is required for a complete Adjustment and Performance Check of the instrument. If only a Performance Check is to be performed, the items required for Adjustment are not required, and are indicated by footnote 1. The remaining test equipment is common to both procedures.

The specifications for test equipment, given in Table 6-3, are the minimum required to meet the performance requirements. Detailed operating instructions for test equipment are omitted in these procedures. Refer to the test equipment instruction manual if more information is needed.

SPECIAL FIXTURES

Special fixtures are used only where they facilitate instrument adjustment. These fixtures are available from Tektronix, Inc. Order by part number from Tektronix Field Offices or representatives.

TEST EQUIPMENT ALTERNATIVES

All of the listed test equipment is required to completely calibrate this instrument. However, complete checking or adjusting may not always be necesary or desirable. You may be satisfied with checking only selected characteristics, thereby reducing the amount of test equipment actually required.

The calibration procedures in Part I and Part II are based on the first item of equipment given as an example. When other equipment is substituted, control settings or setups may need to be altered. If the exact item of equipment given as an example in Table 6-3 is not available, first check the Minimum Specifications column carefully to see if any other equipment might suffice. Then check the Purpose column to see what this item is used for. If used for a performance check or adjustment that is of little or no importance for your measurement requirements, the item and corresponding step(s) can be deleted.

TABLE 6-3
Test Equipment

Description	Minimum Specifications	Purpose	Examples of Applicable Test Equipment
1. Test Oscilloscope	Bandwidth, dc to 50 megahertz, minimum deflection factor 10 millivolts/division; accuracy, within 3%. Dual-channel with an inverting input and both added and alternate vertical modes.	Used throughout calibration procedure.	a. TEKTRONIX 5440 Oscilloscope System with 5A48 Amplifier; 5B40 Time Base, and P6008 Probe. b. TEKTRONIX 475 Oscilloscope with P6053B Probe. c. Refer to the Tektronix Products catalog for compatible oscilloscope system.
2. Amplifier Unit (Two Required)	Tektronix 5A-series plug-in unit.	Used throughout procedure to provide vertical input to the instrument under adjustment.	a. TEKTRONIX 5A48 Amplifier.
3. Time-Base Unit	Sweep rate 0.2 microseconds/division.	Used throughout procedure to provide sweep.	a. TEKTRONIX 5B25N Time Base.
4. Signal Standardizer	Produces gain-check and pulse-response waveforms.	Used throughout procedure to standardize instrument so plug-in units can be interchanged without complete readjustment, and to adjust crt geometry.	a. Tektronix Calibration Fixture 067-0680-00. b. 5000-series plug-in units with suitable signal sources may be substituted if lower performance is acceptable.
5. DMM (Digital Multimeter)	Range, −75 to +200 volts; accuracy, within 0.1%.	Check and adjustment of calibrator output accuracy, Z-axis display voltages.	a. TEKTRONIX DM 501A Option 02 Digital Multimeter with power module. b. Fluke Model 825A Differential DC Voltmeter.
6. Time-Mark Generator	Marker outputs; 20 nanosecond to 0.1 second; marker accuracy, within 0.1%; trigger output, 1 millisecond.	Check and adjustment of horizontal timing, and calibrator frequency.	a. TEKTRONIX TG 501 Time-Mark Generator with power module.
7. Sine-Wave Generator	Frequency, 250 kilohertz to 25 megahertz, reference frequency ≈ 50 kHz; output amplitude, variable from 50 millivolts to 3 volts into 50 ohms.	Check vertical bandwidth and external Z-axis input.	a. TEKTRONIX SG 503 Leveled Sine-Wave Generator with power module. b. General Radio 1310-B Oscillator.
8. Function Generator	Waveform outputs; sine-wave, squarewave and triangular from 6 Hz to 3 MHz.	Used throughout procedure for signal source.	a. TEKTRONIX FG 503, with power module.

TABLE 6-3 (CONT)
Test Equipment

Description	Minimum Specifications	Purpose	Examples of Applicable Test Equipment
9. Coaxial Cable (Two of Each Length Required)	Impedance, 50 ohms; type, RG-58/U; length, 18 and 42 inches; connectors, bnc.	Signal interconnection.	a. Tektronix Part 012-0076-00 (18 inches) and Tektronix Part 012-0057-01 (42 inches).
10. 50-ohm Terminator	Impedance, 50 ohms; accuracy, within 2%. Connectors, bnc.	Output termination for signal generators, if amplifier unit is not 50-ohm input impedance.	a. Tektronix Part 011-0049-01.
11. T Connector	Bnc-to-bnc.	Used to check external Z-Axis operation and X-Y compensation.	a. Tektronix Part 103-0030-00.
12. Low-Capacitance Screwdriver[1]	1-inch shaft.	Used throughout adjustment procedure to adjust variable components.	a. Tektronix Part 003-0000-00.
13. Screwdriver[1]	Three-inch shaft, 3/32-inch bit.	Used throughout procedure to adjust variable resistors.	a. Xcelite R3323.
14. GPIB Controller	IEEE—488 GPIB Compatible Controller.	Exercise GPIB functions.	a. TEKTRONIX 4051 Graphic Computer System.

[1]**Used for Part II—Adjustment and Performance Check only; NOT used for Part I—Performance Check.**

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PART I—PERFORMANCE CHECK

The following procedure (Part I—Performance Check) verifies electrical specifications without removing instrument covers or making internal adjustments. All tolerances given are as specified in the Performance Check Summary Table 6-2.

Part II—Adjustment and Performance Check provides the information necessary to: (1) verify that the instrument meets the electrical specifications, (2) verify that the controls function properly, and (3) perform all internal adjustments.

A separate Checkout Procedure is provided in section 2 of this manual to provide instrument familiarization and also to verify that the controls function properly.

See Table 6-1, Calibration Procedure Electives, at the beginning of this section, for information on performing a Partial Part I—Performance Check procedure.

INDEX TO PART I PERFORMANCE CHECK

PERFORMANCE CHECK INITIAL SETUP PROCEDURE

NOTE

The performance of this instrument can be checked at any ambient temperature from 0° to +50° C unless otherwise stated.

1. Check that the Line Voltage Selector switch is set for the correct input line voltage; also check that a suitable power cord and plug has been attached. Refer to Installation in Section 1 for specific details.

2. Set the rear-panel GPIB Selector switch as shown in Figure 6-1.

3. Connect the instrument to the power source.

4. Pull the POWER switch out and allow at least 20 minutes warmup before proceeding.

CAUTION

To prevent instrument damage, turn off the 5223 POWER before installing or removing plug-in units.

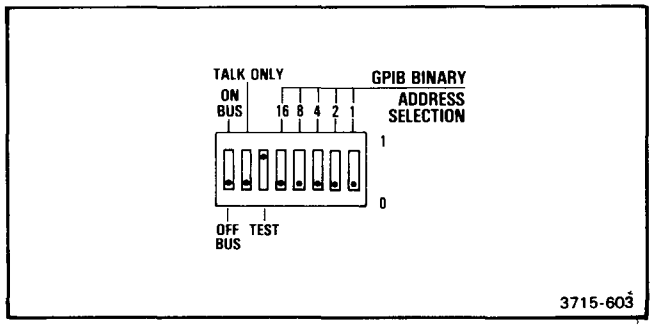

Figure 6-1. GPIB selector switch setting.

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A. REAL-TIME DISPLAY

Equipment Required: (Numbers correspond to those listed in Table 6-3, Test Equipment.)

2. Amplifier Unit (2 required)
3. Time-Base Unit
4. Signal Standardizer
6. Time-Mark Generator
7. Sine-Wave Generator
8. Function Generator
9. Coaxial cable (two 18 inch, one 42 inch)
10. 50-ohm Terminator
11. T Connector

Shaded lines identify Performance Requirement CHECK.

A1. REAL-TIME DISPLAY PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure given at the beginning of Part I—Performance Check.

b. Refer to Section 7, Instrument Options, and the Change Information at the rear of this manual for any modifications which may affect this procedure.

c. Set 5223 Digitizing Oscilloscope controls as follows:

POWER ..... ON
INTENSITY ..... Counterclockwise
FOCUS ..... 1 o'clock
GRAT ILLUM ..... Midrange
MEM INTEN ..... Counterclockwise
MEMORY CONTENTS ..... All pushbuttons out
VERT EXP X1
HORIZ EXP X1
VERT POSN ..... Midrange
HORIZ POSN ..... Midrange

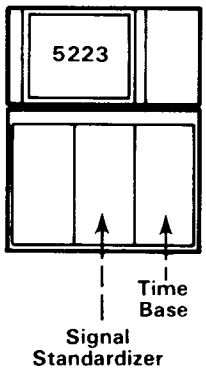
A2. CHECK TRACE ALIGNMENT, VERTICAL AND HORIZONTAL REAL-TIME CENTERING

NOTE

First perform step A1, then proceed.

A2. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Signal Standardizer
Amplitude ..... Midrange
Position ..... Midrange
Test ..... Vert or Horiz Aux In

Time Base
Sweep Rate ..... 1 ms/Div
Triggering
Coupling ..... AC
Source ..... Right
Mode ..... Auto

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a. Set the INTENSITY control for a visible trace.

b. Use the signal standardizer Position control to align the displayed trace with the center graticule line.

c. **CHECK**—Trace parallels the center graticule line within 0.1 division.

d. Set the signal standardizer Test selector switch to Vert or Horiz Com Mode.

e. **CHECK**—That the trace is within 0.05 division of the center graticule line.

f. Move the signal standardizer to the horizontal compartment and the time-base unit to the right vertical compartment.

g. **CHECK**—That the trace aligns with the center graticule line within 0.1 division.

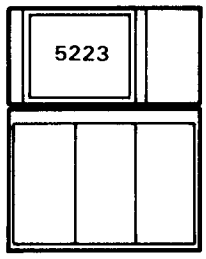
A3. CHECK GEOMETRY, HORIZONTAL AND VERTICAL MEMORY GAIN, AND LOW FREQUENCY LINEARITY

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A3. SETUP CONDITIONS

5223 Controls:
- MEMORY CONTENTS
  - LEFT VERT PLUG-IN DISPLAY ..... In
  - L VS R ..... In
  - VECTOR MODE ..... In
  - LEFT VERT PLUG-IN SAVE ..... In
  - All other pushbuttons ..... Out
- POWER ..... Off



3715-605

a. Pull POWER switch ON.

b. Set the MEM ITEN control for a visible display.

c. Use the MEMORY CONTENTS VERT POSN and HORIZ POSN controls to align the displayed grid pattern with the graticule lines.

d. **CHECK**—That the traces parallel the graticule lines within 0.1 divisions.

e. **CHECK**—For 8 divisions of deflection between the second vertical trace and the tenth vertical trace, within 0.16 division, and that the deflection between any two vertical traces does not exceed 0.2 division.

f. **CHECK**—For 6 divisions of deflection between the second and eight horizontal trace within 0.12 division and that its deflection between any two horizontal traces does not exceed 0.15 division.

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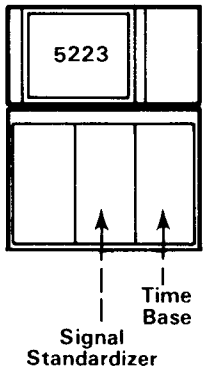
A4. CHECK VERTICAL AND HORIZONTAL REAL-TIME GAIN, LOW FREQUENCY LINEARITY, AND BEAMFINDER

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A4. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Signal Standardizer
Rep Rate ..... 1 kHz
Test ..... Vert or Horiz Gain

Time Base
Sweep Rate ..... 10 μs/Div
Triggering
Mode ..... Auto

C2932-532

a. Set the INTENSITY control for a visible display of nine horizontal traces.

b. Use the signal standardizer Position control to align the bright center trace with the graticule center line.

c. **CHECK**—For one trace per graticule division, with six divisions of deflection between the third trace above and the third trace below the center bright trace, within 0.06 division.

d. **CHECK**—For less than 0.2 division error in any two divisions of deflection anywhere on the crt screen.

e. Move the signal standardizer to the left vertical compartment.

f. **CHECK**—For one trace per graticule division, with six divisions of deflection between the third trace above and the third trace below the bright center trace, within 0.06 division.

g. Set the INTENSITY control fully counterclockwise.

h. **CHECK**—Press the BEAMFINDER pushbutton and check that a trace is visible and cannot be positioned off the crt screen with the signal standardizer and time-base Position controls.

i. Move the signal standardizer to the horizontal compartment and the time-base unit to the center compartment.

j. **CHECK**—For 8 divisions of deflection between the second vertical trace and the tenth vertical trace, within 0.08 division, and that the deflection between any two vertical trace does not exceed 0.1 division.

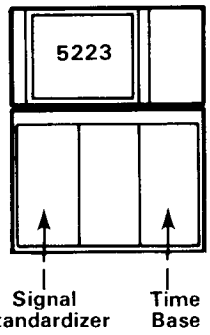
A5. CHECK VERTICAL AMPLIFIER STEP RESPONSE

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A5. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Signal Standardizer
Rep Rate ..... 100 kHz
Test ..... Vert or Horiz + Step Response

Time Base
Sweep Rate ..... 2 μs/Div
Triggering
Mode ..... Auto
Slope ..... +
Source ..... Left

C2932-533

a. Set the INTENSITY control for desired viewing.

b. Set the signal standardizer Position and Amplitude controls for a 6-division display centered on the graticule area.

c. Set the time-base unit triggering controls for a stable display.

d. **CHECK**—Displayed pulse for a flat top and square corner that does not deviate more than 0.18 division, with the signal standardizer Rep Rate and time-base unit sweep rates given in Table 6-4.

e. Move the signal standardizer to the center vertical compartment.

f. Set the signal standardizer Rep Rate switch to 100 kilohertz. Set the Amplitude and Position controls for a six-division display, centered on the graticule area.

TABLE 6-4
Frequency Compensation
(Signal Rep Rate vs. Sweep Rate)

Signal Standardizer Rep Rate	Sweep Rate
100 kHz	2 μs
1 MHz	0.2 μs

g. Set the time-base sweep rate to 2 microseconds/division and triggering to Right.

h. **EXAMINE**—Displayed pulse for a flat top and square corner that does not deviate more than 0.18 division with the signal standardizer Rep Rate and the time-base unit sweep rates given in Table 6-4.

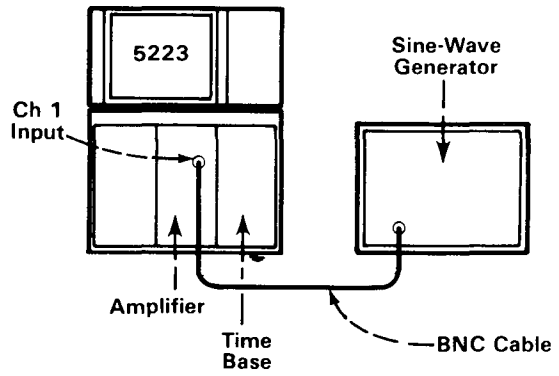
A6. CHECK VERTICAL AMPLIFIER 12 MEGAHERTZ GAIN

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A6. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Amplifier
Channel 1 Deflection Factor ..... 20 mV/Div
Input Coupling ..... DC
Mode ..... Ch 1

Sine-Wave Generator
Frequency Range ..... Ref ≈.05 MHz

Time Base
Sweep Rate ..... 1 ms/Div
Triggering
Mode ..... Auto
Source ..... Right
Coupling ..... AC

C2932-534

a. Set the INTENSITY control for a visible display.

b. Set the sine-wave generator controls and amplifier Position control for a 6-division display centered on the graticule.

c. Without changing the sine-wave generator output amplitude, increase the sine-wave generator frequency until the displayed amplitude is reduced to 4.2 divisions.

d. **CHECK**—Sine-wave generator frequency is at least 12 megahertz.

e. Move the amplifier to the left vertical compartment (leave signal connected).

f. **CHECK**—Return the sine-wave generator Frequency Range to Ref ≈0.5 MHz, and repeat parts b through d for the left vertical compartment.

A7. CHECK HORIZONTAL TIMING

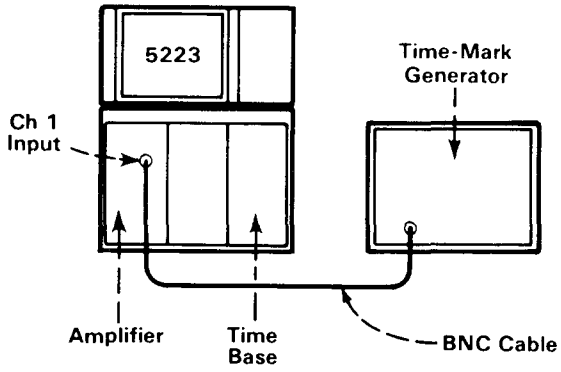
This step verifies that the 5223/time-base system will meet the sweep timing specifications of the time base being used.

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A7. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Amplifier
Channel 1 Input Coupling ..... DC
Mode ..... Ch 1
Trigger ..... Ch 1

Time Base
Sweep Rate ..... 0.5 ms/Div
Triggering
Coupling ..... AC
Mode ..... Auto
Source ..... Left

C2932-535

a. Connect 1-millisecond markers from the time-mark generator to the amplifier unit input and adjust the amplifier unit deflection factor for about 2 divisions of display. Set the INTENSITY control for desired viewing.

b. Set the time-base unit triggering controls for a stable display.

c. Position the first marker to the extreme left graticule line.

d. Set the time-base unit sweep calibration control for 1 marker at each major graticule division between the second and tenth graticule lines (center 8 divisions).

e. **CHECK**—Refer to the instruction manual Timing Specifications, for the time base being used, to check the systems high-frequency timing and linearity.

f. Return the time-base unit sweep calibration control to the calibrated position.

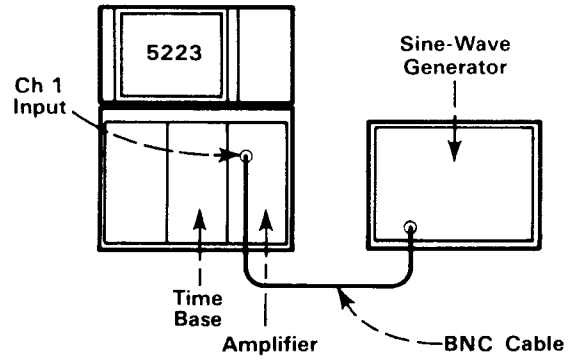
A8. CHECK HORIZONTAL BANDWIDTH

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A8. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Amplifier
Channel 1 Deflection Factor ..... 20 mV/Div
Channel 1 Input Coupling ..... DC
Mode ..... Ch 1

Sine-Wave Generator
Frequency Range ..... Ref ≈.05 MHz

Time Base
Sweep Rate ..... 1 ms/Div
Triggering
Mode ..... Auto

C2932-536

a. Set the INTENSITY controls for desired viewing.

b. Set the sine-wave generator for 8 divisions of the 50 kilohertz signal centered on the 5223 crt.

c. Set the sine-wave generator output frequency to 7 megahertz.

d. **CHECK**—That the amplitude of the displayed 7 megahertz signal is at least 5.7 divisions.

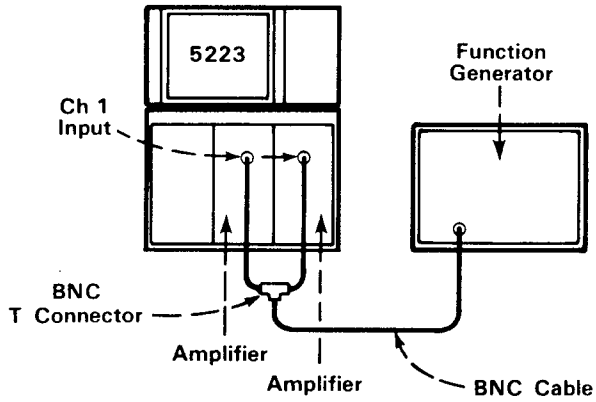
A9. CHECK XY OPERATION

NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A9. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Amplifiers (Both)
Channel 1 Deflection Factor ..... 1 V/Div
Channel 1 Input Coupling ..... DC
Mode ..... Ch 1

Function Generator
Function ..... Sine wave

C2932-537

a. Set the INTENSITY control for desired viewing.

b. Set the function generator Amplitude and Frequency controls to display 8 divisions of 20 kilohertz on the vertical and horizontal axis (diagonally).

c. **CHECK**—That the opening at the center of the displayed ellipse is not more than 0.35 divisions vertically.

B. MEMORY

Equipment Required: (Numbers correspond to those listed in Table 6-3, Test Equipment.)

1. Test Oscilloscope
2. Amplifier Unit (two required)
3. Time-base Unit
4. Signal Standardizer
6. Time-Mark Generator
7. Sine-Wave Generator
8. Function Generator
9. Coaxial Cable (two 18 inch, two 42 inch)
10. 50-Ohm Terminator
11. T Connector

Shaded lines identify Performance Requirement CHECK.

B1. MEMORY PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure given at the beginning of Part I—Performance Check.

b. Refer to Section 7, Instrument Options, and the Change Information at the rear of this manual for any modifications which may affect this procedure.

c. Set the 5223 Digitizing Oscilloscope controls as follows:

POWER ..... ON
INTENSITY ..... Counterclockwise
FOCUS ..... Midrange
GRAT ILLUM ..... Midrange
MEM INTEN ..... Counterclockwise
MEMORY CONTENTS .....All pushbuttons out
VERT EXP X1
HORIZ EXP X1
VERT POSN ..... Midrange
HORIZ POSN ..... Midrange

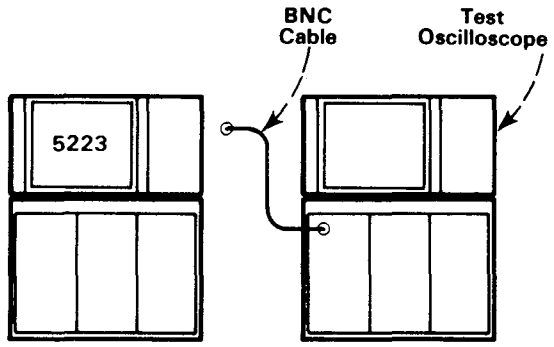
B2. CHECK MEMORY DISPLAY OUT GAIN

NOTE

First perform B1, then proceed.

B2. SETUP CONDITIONS

5223 Controls:
MEMORY CONTENTS
VECTOR MODE ..... IN
VERT EXP X1
HORIZ EXP X1
POWER ..... Off



Test Equipment Controls:
Test Oscilloscope
Deflection Factor ..... 0.5 V/Div
Sweep Rate ..... 5 ms/Div
Input Coupling ..... DC

3715-606

a. Perform B2. Setup Conditions.

b. Set the rear-panel GPIB switch to Test 3, see Figure 6-2.

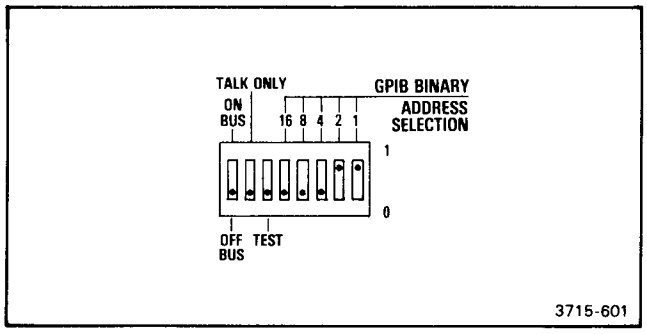


Figure 6-2. GPIB switch Test 3 selection.

c. Pull POWER switch ON.

d. Connect a bnc cable from the test oscilloscope vertical input to the MEMORY DISPLAY OUTPUTS Y connector on the rear-panel of 5223.

e. Set the DISPLAY OUT SPEED control to FAST (rear-panel).

f. **CHECK**—Observe test oscilloscope display for a signal amplitude of 2 volts (make sure test oscilloscope vertical deflection factor is accurate).

g. Remove the bnc cable from the MEMORY DISPLAY Y connector and connect it to the MEMORY DISPLAY X connector.

h. **CHECK**—Observe a signal transition of 2 volts on the test oscilloscope display.

i. Turn POWER switch OFF and set the rear-panel GPIB selector switch as shown in Figure 6-1, page 6-14. Then, turn POWER switch ON.

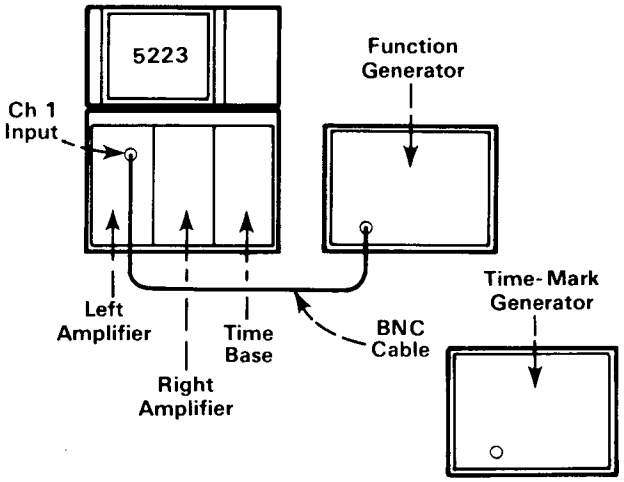
B3. CHECK DIGITIZER GAIN

NOTE

If the preceding step was not performed, first perform B1, then proceed.

B3. SETUP CONDITIONS

5223 Controls:
- MEMORY CONTENTS
  - LEFT VERT PLUG-IN DISPLAY ..... In
  - All other pushbuttons ..... Out
  - VERT EXP X1
  - HORIZ EXP X1



Test Equipment Controls:
- Function Generator ..... 2 kHz Square Wave

Left Amplifier
- Display ..... On
- Channel 1 Deflection Factor ..... 1 V/Div
- Mode ..... Ch 1

Right Amplifier
- Display ..... Off
- Channel 1 Deflection Factor ..... 1 V/Div
- Mode ..... Ch 1

Time Base
- Sweep Rate ..... 0.1 ms/Div
- Triggering
  - Coupling ..... AC
  - Source ..... Left
  - Mode ..... Auto

C2932-540

a. Perform B3. Setup Conditions.

b. Set the MEM INTEN control fully counterclockwise and the INTENSITY control for desired viewing.

c. Apply a 6 division square-wave signal from the function generator to the input of the left-amplifier unit channel 1 input and set the time-base unit triggering controls for a stable display.

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d. Set the MEM INTEN control for desired viewing.

e. **CHECK**—That the real-time gain matches the memory gain within 0.12 division.

f. Disconnect the square-wave signal from the left amplifier unit and connect it to the right amplifier unit Channel 1 input.

g. Set the right amplifier unit Display switch to On and Channel 1 deflection factor to 1 volt. Press and release the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY switch.

h. Press the MEMORY CONTENTS RIGHT VERT PLUG-IN DISPLAY switch in and set the time-base unit triggering source to right and trigger level for a stable display.

i. **CHECK**—That the real-time gain matches the memory gain within 0.12 divisions.

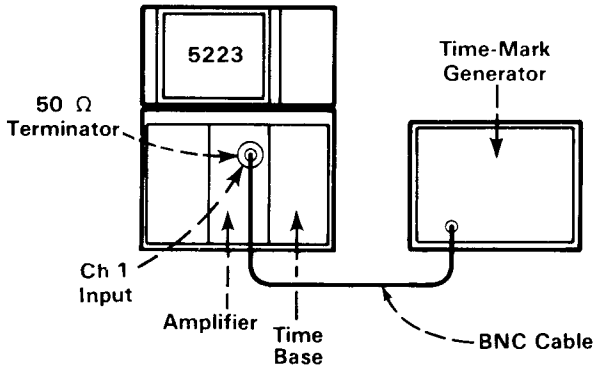
B4. CHECK REAL TIME AND MEMORY TIMING MATCH

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B4. SETUP CONDITIONS

5223 Controls:
- MEMORY CONTENTS
  - RIGHT VERT PLUG-IN DISPLAY ..... In
  - All other pushbuttons ..... Out



Test Equipment Controls:
- Amplifier
  - Channel 1 Deflection Factor ..... 1 V/Div
  - Mode ..... Ch 1
  - Trigger ..... Ch 1
- Time-Mark Generator ..... 0.5 ms Markers
- Time Base
  - Sweep Rate ..... 0.5 ms/Div
  - Triggering
    - Source ..... Right
    - Coupling ..... AC
    - Mode ..... Auto

C2932-538

a. Connect the output of time-mark generator to the input of the vertical amplifier unit through a 50Ω terminator.

b. Set the time-mark generator to 0.5 milliseconds markers.

c. Set the INTENSITY and MEM INTEN controls for desired viewing.

d. Set the time-base unit triggering control for a stable display.

e. Align the second time mark with the second left-most graticule line.

f. **CHECK**—That the memory display matches the real-time display within 0.24 division at the tenth graticule line; if not within 0.24 division see digitizer time-base calibration procedure.

g. Rotate the MEM INTEN control fully counterclockwise.

h. Rotate the time-base unit Position control to equalize errors at the second and tenth time markers with the second and tenth graticule lines.

i. **CHECK**—That the sixth (center) time marker aligns with the graticule center line within 0.2 divisions.

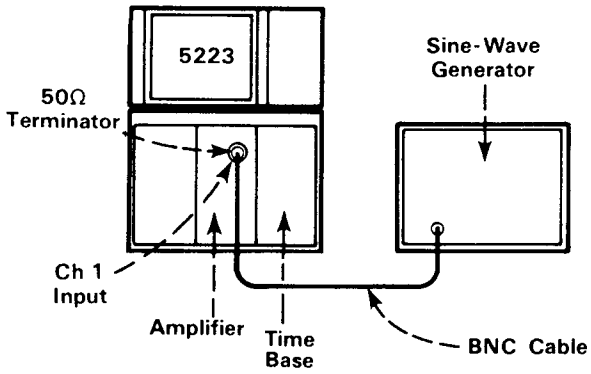
B5. CHECK DIGITIZER BANDWIDTH

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B5. SETUP CONDITIONS

5223 Controls:
INTENSITY ..... Fully counterclockwise



Test Equipment Controls:
Amplifier
Channel 1 Deflection Factor ..... 0.5 V/Div
Display ..... On
Position ..... Midrange

Time Base
Sweep Rate ..... 10 μs/Div
Triggering ..... Auto

Sine-Wave Generator ..... Ref ≈.05 MHz

C2932-541

a. Set the MEM INTEN control for desired viewing.

b. Set the sine-wave generator to display 6 divisions of the 50 kilohertz signal centered on the crt.

c. Set the time-base unit sweep rate to 0.2 microseconds/divisions and the sine-wave generator frequency to 10 megahertz.

d. **CHECK**—Memory display for at least 4.2 divisions of signal.

e. Move the amplifier unit to the left vertical compartment (leave cable connected).

f. Press the MEMORY CONTENTS LEFT VERT-PLUG-IN DISPLAY switch in, and press and release the MEMORY CONTENTS RIGHT VERT PLUG-IN DISPLAY switch.

g. Set the sine-wave generator to display 6 divisions of the 50 kilohertz signal centered on the crt.

h. Set the sine-wave generator to 10 megahertz and the time-base unit Triggering to Left.

i. **CHECK**—Memory display for at least 4.2 divisions of displayed signal.

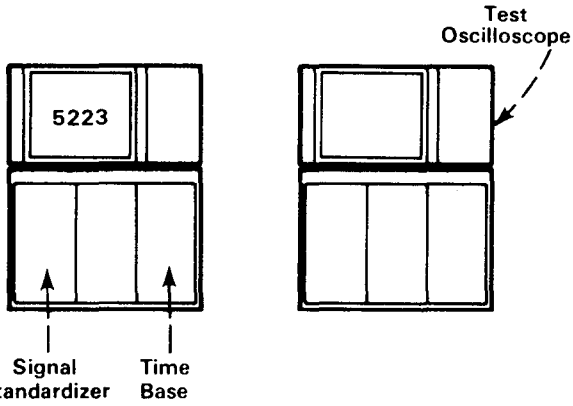
B6. CHECK DIGITIZER ABERRATIONS AND BLOWBY

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B6. SETUP CONDITIONS

5223 Controls:
- INTENSITY ..... For desired viewing
- MEMORY CONTENTS
  - LEFT PLUG-IN DISPLAY ..... In
  - RIGHT PLUG-IN DISPLAY ..... In
  - All other pushbuttons ..... Out



Test Equpment Controls:
- Signal Standardizer
  - Test Selector switch ..... Vert or Horiz + Step Resp
  - Rep Rate ..... 1 MHz
- Time Base
  - Sweep Rate ..... 0.2 μs/Div
  - Triggering
    - Coupling ..... AC
    - Source ..... Left
    - Mode ..... Auto
- Test Oscilloscope
  - Vertical Deflection Factor ..... 50 mV/Div
  - Sweep Rate ..... 0.1 μs/Div

C2932-542

a. Set the signal standardizer Amplitude and Position controls for 5 division pulses centered on the crt.

b. Set the MEM INTEN control for desired viewing.

c. **CHECK**—That the flat top of the memory display matches the real-time display within 0.05 division.

d. **CHECK**—Memory display aberrations are less than 0.15 division.

e. Remove the signal standardizer from the left vertical compartment and install it in the right vertical compartment.

f. Set the time-base unit triggering source switch to Right.

g. Press the MEMORY CONTENTS RIGHT VERT PLUG-IN DISPLAY switch in, and press and release the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY switch.

h. **CHECK**—Repeat parts a and d for the right vertical memory display.

C. CALIBRATOR AND INPUT/OUTPUT SIGNALS

Equipment Required: (Numbers correspond to those listed in Table 6-3, Test Equipment.)

1. Test Oscilloscope
2. Amplifier Unit (two required)
3. Time-Base Unit
4. Signal Standardizer
5. DMM (digital multimeter)
6. Time-Mark Generator
7. Sine-Wave Generator
9. Coaxial Cable (two 18 inch, one 42-inch required)
11. T Connector

Shaded lines identify Performance Requirement CHECK.

C1. CALIBRATOR AND INPUT/OUTPUT SIGNALS PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup Procedure given at the beginning of Part I—Performance Check.

b. Refer to Section 7, Instrument Options, and the Change Information at the rear of this manual for any modifications which may affect this procedure.

c. Set 5223 Digitizing Oscilloscope controls as follows:

POWER ..... ON
INTENSITY ..... Counterclockwise
FOCUS ..... Midrange
GRAT ILLUM ..... Midrange
MEM INTEN ..... Counterclockwise
MEMORY CONTENTS .....All pushbuttons out
VERT EXP X1
HORIZ EXP X1
VERT POSN ..... Midrange
HORIZ POSN ..... Midrange

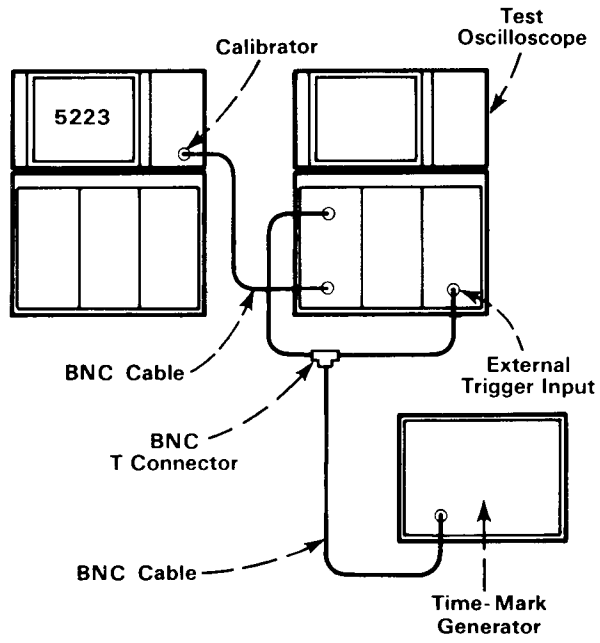
C2. CHECK CALIBRATOR 1 kHz REPETITION RATE

NOTE

First perform step C1, then proceed.

C2. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Test Oscilloscope
Triggering ..... Auto, Ac, External
Input Coupling ..... DC
Sweep Rate ..... 0.5 ms/Div
Vertical Mode ..... Add

C2932-543

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NOTE

A frequency counter with an accuracy of at least 0.1% may be used to check the CALIBRATOR repetition rate.

a. Use a bnc T-connector to apply 1-millisecond time-markers to the test oscilloscope external trigger input and the channel 1 vertical input. Connect the 5223 CALIBRATOR output to the Channel 2 vertical input of the test oscilloscope.

b. Set the test oscilloscope vertical deflection factors to display 2 divisions of CALIBRATOR signal, and 1 division of time-marker signal.

c. Set the test oscilloscope triggering level for a stable time-mark display.

d. Set the test oscilloscope sweep rate for 0.5 second/division.

e. **CHECK**—The time required for the 1-millisecond time marks to drift from the positive level of the CALIBRATOR signal to the negative level, and back to the positive level, must be more than 1.0 second (2 divisions). This time can be measured directly from the display by observing the number of divisions that the markers move across the display area before, it returns to the positive level, in one second.

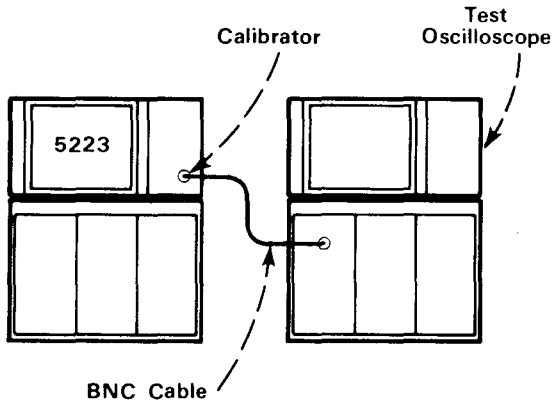
C3. CHECK CALIBRATOR DUTY CYCLE

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C3. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Test Oscilloscope
Vertical Deflection ..... 100 mV/Div
Sweep Rate ..... 1 ms/Div
Triggering
Slope ..... +
Coupling ..... AC
Mode ..... Auto
Source ..... Left
Vertical Mode ..... Ch 1

C2932-544

a. Set the test oscilloscope triggering for positive slope and auto mode with ac coupling from the internal source at a sweep rate of 0.1 millisecond/division. Set the triggering controls so that the display starts at the 50% point on the rising edge of the waveform.

b. Set the test oscilloscope sweep magnifier to X10. Then, position the display horizontally so the falling edge of the waveform aligns with the center vertical graticule line.

c. Set the test oscilloscope triggering to negative slope.

d. **CHECK**—The 50% point on the rising edge of the waveform now displayed is within 2.0 divisions horizontally of the center line. (Indicates duty cycle of 50%, within 2%.)

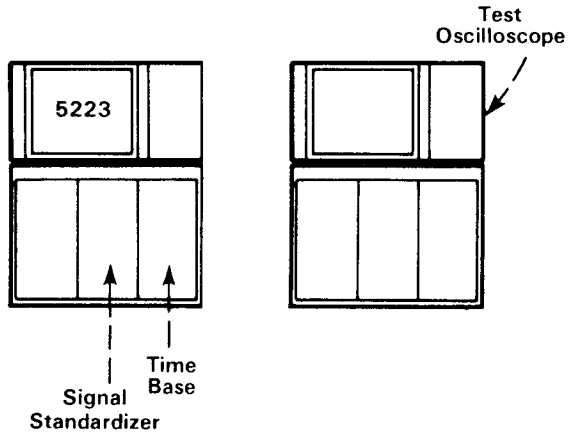
C4. CHECK RIGHT VERTICAL, LEFT VERTICAL, HORIZONTAL, A GATE OUT OR SAMPLE OUT CLOCK AND MEMORY X AND Y DISPLAY OUTPUTS

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C4. SETUP CONDITIONS

5223 Controls:
MEMORY CONTENTS
All pushbuttons ..... Out



Test Equipment Controls:
Signal Standardizer
Test Selector switch ..... Vert or Horiz Gain
Rep Rate ..... 100 kHz

Test Oscilloscope
Sweep Rate ..... 0.5 ms/Div
Vertical Deflection Factor ..... 50 mV/Div

Time Base
Sweep Rate ..... 1 ms/Div

C2932-545

a. Connect the input of the test oscilloscope to the PLUG-IN OUTPUTS RIGHT VERT connector (located on the 5223 rear-panel) with a bnc cable, and position the bright trace (test oscilloscope) to the center graticule line.

b. **CHECK**—That there is 6 divisions of deflection between the third trace above and below the center graticule line on the test oscilloscope display, within 0.3 division.

c. Remove the signal standardizer from the right vertical compartment and install it in the left vertical compartment.

d. Disconnect the bnc cable from the PLUG-IN OUTPUTS RIGHT VERT connector and connect it to the PLUG-IN OUTPUTS LEFT VERT connector. Position the bright trace to the center graticule line.

e. **CHECK**—That there is 6 divisions of deflection between the third trace above and below the center graticule line on the test oscilloscope display, within 0.3 division.

f. Set the signal standardizer Test selector switch to Vert or Horiz + Step Resp, Rep Rate to 1 kilohertz, and the Amplitude control for a 4 division display on the 5223 crt.

g. Use a bnc cable to connect the MEMORY DISPLAY OUTPUT Y connector (rear panel) to the test oscilloscope vertical input.

h. Set the test oscilloscope vertical deflection factor to 0.5 volts, and the sweep rate to 0.1 seconds.

i. Set the rear-panel DISPLAY OUT SPEED control to FAST.

j. Press the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY and SAVE switches in.

k. **CHECK**—Press the MEMORY CONTENTS OUTPUT SAVED DISPLAY(S) switch in and observe test oscilloscope display for a square-wave signal.

l. Move the bnc cable to the MEMORY DISPLAYS OUTPUT X connector, and set the test oscilloscope sweep rate to 1 second/division.

m. **CHECK**—Press the MEMORY CONTENTS OUTPUT SAVED DISPLAY(S) switch and observe the test oscilloscope display for one sawtooth cycle.

n. Remove the signal standardizer from the left vertical compartment, and install amplifier units in the left and right vertical compartments.

o. Set the time-base sweep unit rate to 0.5 milliseconds/division, and move the bnc cable from the MEMORY DISPLAY OUTPUTS connector to the A GATE OUT OR SAMPLE CLK OUT connector.

p. Set the test oscilloscope deflection factor to 1 volt/divison.

q. **CHECK**—For an A Gate signal on the test oscilloscope that is TTL compatible; rectangular waveform with the positive excursion greater than +2.4 volts and a baseline of +0.8 volt or less; The instrument under test may be set to output the Sample Clock signal, see Part II—Adjustment and Performance Check to verify the A Gate signal.

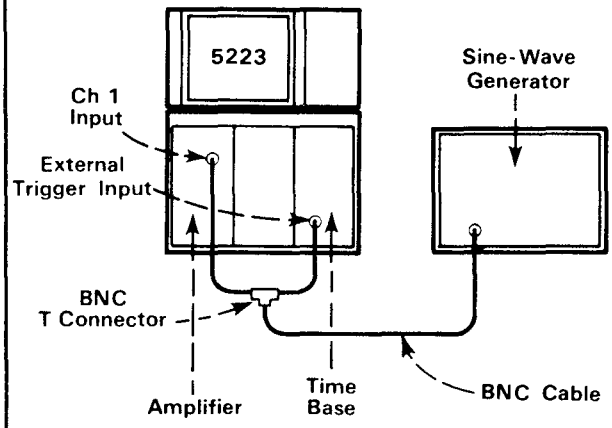
C5. CHECK Z-AXIS, SS RESET AND PEN LIFT OUTPUTS

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C5. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Amplifier
Channel 1 Deflection Factor ..... 1 V/Div

Sine-Wave Generator ..... 1 MHz

Time Base
Sweep Rate ..... 0.2 μs/Div
Triggering
Coupling ..... AC
Source ..... External
Mode ..... Auto

C2932-546

a. Set the signal generator Amplitude control and time-base unit Triggering controls for a 5 division stable display on the 5223 crt.

b. Disconnect the bnc cable from the amplifier input connector and connect it to the rear-panel Z-AXIS INPUT connector.

c. **CHECK**—Rotate the INTENSITY control and check that the displayed trace intensity is modulated by the 1 megahertz signal.

d. Set the time-base unit sweep rate to 5 milliseconds/division.

e. Set the INTENSITY control for desired viewing.

f. Press the Single-Sweep Reset pushbutton on the time-base unit.

g. **CHECK**—While shorting the center conductor on the rear panel SS RESET connector to ground, observe one sweep of the crt.

h. Connect the DMM (digital multimeter) leads between ground and the middle pin on the camera power connector.

i. **CHECK**—While shorting the center conductor on the rear panel SS RESET connector to ground, notice that the meter reading changes to zero.

j. Press the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY and SAVE switches in.

k. Connect the DMM, set to measure resistance, between the two PEN LIFT banana plug connectors (located on the rear panel).

l. **CHECK**—Press the MEMORY CONTENTS OUTPUT SAVED DISPLAY(S) switch and notice that the meter reading indicates approximately zero ohms; if the meter reading indicates a high resistance, see the Part II—Adjustment and Performance Check Procedure.

This concludes the Part I—Performance Check procedure.

PART II—ADJUSTMENT AND PERFORMANCE CHECK

The following procedure (Part II—Adjustment and Performance Check) provides the information necessary to: (1) verify that the instrument meets the electrical specifications, (2) verify that the controls function properly, and (3) perform all internal adjustments.

Part I—Performance Check verifies that the instrument meets the electrical specifications without making internal adjustments. All tolerances given are as specified in the Specification tables (section 1) in this manual.

A separate Checkout Procedure is provided in section 2 for instrument familiarization and also to verify that the controls function properly.

See Table 6-1, Calibration Procedure Electives, at the beginning of this section, for information on performing a Partial Part II—Adjustment and Performance Check procedure.

INDEX TO PART II—ADJUSTMENT AND PERFORMANCE CHECK

@

ADJUSTMENT AND PERFORMANCE CHECK INITIAL SETUP PROCEDURE

NOTE

The performance of this instrument can be checked at any ambient temperature from 0° to +50° C unless otherwise stated. Adjustments must be performed at an ambient temperature between +20° and +30° C for specified accuracies.

1. Remove the panel covers from the 5223 (refer to panel cover removal in section 1 of this manual).

2. Check that the Line Voltage Selector board is set for the correct input line voltage (refer to line voltage selection in section 1 of this manual).

3. Set the rear-panel GPIB selector switch as shown in Figure 6-3.

CAUTION

To avoid instrument damage, it is recommended that the POWER switch be turned off before removing or replacing plug-in units.

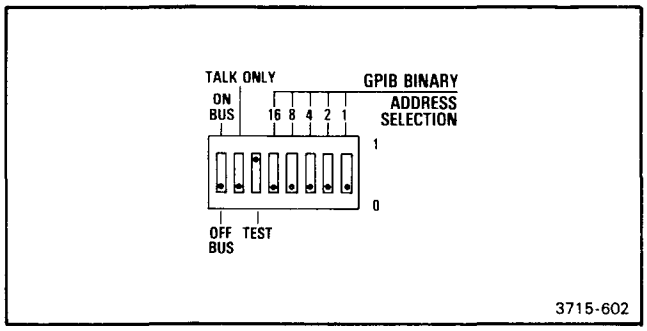


Figure 6-3. GPIB selector switch setting.

4. Install a 5B25N Time-Base unit in the 5223 Digitizing Oscilloscope horizontal compartment.

5. Connect the 5223 Digitizing Oscilloscope to a suitable power source. Set the POWER switch to ON and allow at least 20 minutes warmup.

A. POWER SUPPLY

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

5. DMM (digital multimeter)
13. Screwdriver

Shaded lines identify Performance Requirement CHECK.

A1. POWER SUPPLY PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup Procedure given at the beginning of Part II—Adjustment and Performance Check.

b. Refer to Section 7, Instrument Options, and the Change Information at the rear of this manual for any modifications which may affect this procedure.

c. See **TEST POINT AND ADJUSTMENT LOCATIONS A** foldout page in Section 9, Diagrams and Circuit Board Illustrations.

d. Set 5223 Digitizing Oscilloscope controls as follows:

POWER ..... ON
INTENSITY ..... Counterclockwise
FOCUS ..... Midrange
GRAT ILLUM ..... Midrange
MEM INTEN ..... Counterclockwise
MEMORY CONTENTS ..... All Pushbuttons Out
VERT EXP X1
HORIZ EXP X1
VERT POSN ..... Midrange
HORIZ POSN ..... Midrange

e. Lay the instrument on its right side as viewed from front panel.

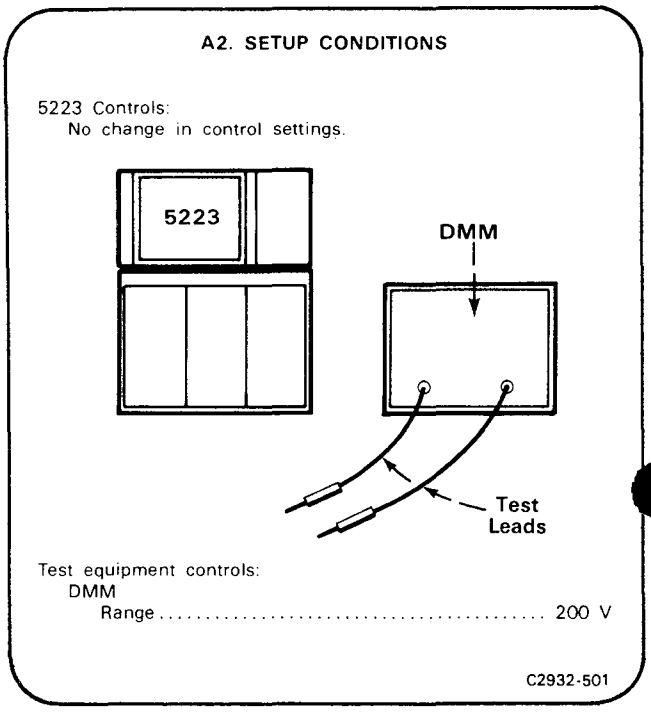
A2. ADJUST +30 VOLT AND -30 VOLT POWER SUPPLIES (A7R521 AND A7R522)

NOTE

First, perform step A1, then proceed.

WARNING

Extreme caution must be used when operating the 5223 with the panel covers removed due to the line voltage, high voltage, and high current potentials present.



a. Connect the DMM (digital multimeter) between TP910 (-30 V) and TP930 (Gnd) on the Power Supply circuit board.

b. **EXAMINE**—The DMM reading for -30 volts, within the limits of -29.99 to -30.01 volts.

c. **ADJUST**—The -30 Volt adjustment (R521) (located on A7 Power Supply board) for a meter reading between -29.99 and -30.01 volts.

d. Connect the DMM between TP510 (+30 V) and TP930 (Gnd).

e. **EXAMINE**—Meter reading for +30 volts within the limits of +29.99 to +30.01 volts.

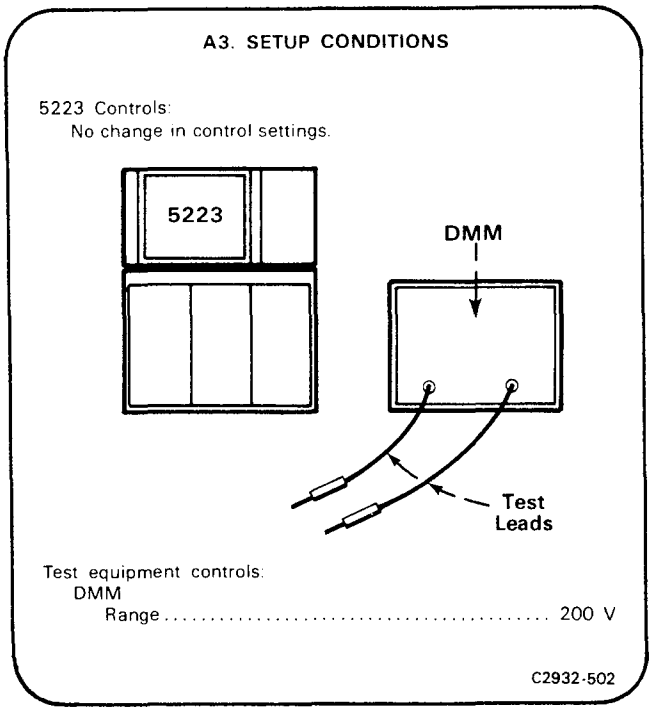
f. **ADJUST**—The +30 Volt adjustment (R522) (located on A7 Power Supply board) for a meter reading between +29.99 and +30.01 volts.

g. **INTERACTION**—Any change in the setting of R521 will affect the setting of R522, and may affect the operation of all circuits in the instrument.

A3. EXAMINE POWER-SUPPLY VOLTAGES

NOTE

If the preceding step was not performed, first perform step A1, then proceed.



a. **EXAMINE**—Table 6-5 lists the low-voltage power supplies in this instrument. Connect DMM common lead to TP930 (Gnd) and check each supply for output voltages within the given tolerance.

b. **INTERACTION**—If the power supplies are not within the tolerances given in Table 6-5, perform step A2.

TABLE 6-5
Power Supply Tolerance

Power Supply	Output Voltage Limits	DMM Voltage Range
TP910 (-30 V)	-29.99 to -30.01 volts	200
TP1010 (-15 V)	-14.860 to -15.140 volts	20
TP940 (+5 V)	+4.803 to +5.197 volts (nominal 5.1 V)	20
TP820 (+15 V)	+14.860 to +15.140 volts	20
TP510 (+30 V)	+29.99 to +30.01 volts	200
TP1230 (+86 V)	+84.34 to +87.65 volts	200

c. Disconnect the DMM test leads.

B. REAL-TIME DISPLAY

Equipment Required: (Numbers correspond to those listed in Table 6-3, Test Equipment.)

1. Test Oscilloscope
2. Amplifier Unit (two required)
3. Time-Base Unit
4. Signal Standardizer
5. DMM (digital multimeter)
6. Time-Mark Generator
7. Sine-Wave Generator
8. Function Generator
9. Coaxial Cable (two required)
11. T Connector
12. Low-Capacitance Screwdriver
13. Screwdriver

Shaded lines identify Performance Requirement CHECK.

B1. REAL-TIME DISPLAY PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup Procedure given at the beginning of Part II—Adjustment and Performance Check.

b. Refer to Section 7, Instrument Options, and the Change Information at the rear of this manual for any modifications which may affect this procedure.

c. See **TEST POINT AND ADJUSTMENT LOCATIONS B** foldout page in Section 9, Diagrams and Circuit Board Illustrations.

d. Set 5223 Digitizing Oscilloscope controls as follows:

POWER ..... ON
INTENSITY ..... Counterclockwise
FOCUS ..... 1 o'clock
GRAT ILLUM ..... Midrange
MEM INTEN ..... Counterclockwise
MEMORY CONTENTS .....All pushbuttons out
  VERT EXP X1
  HORIZ EXP X1
  VERT POSN ..... Midrange
  HORIZ POSN ..... Midrange

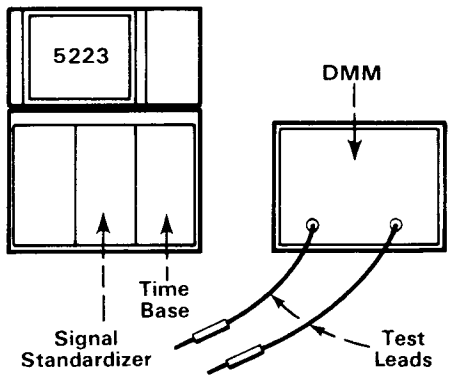
B2. CHECK/ADJUST TRACE ALIGNMENT (A3R220), VERTICAL CENTERING (A3R326), VERTICAL COMMON MODE (A3R225), HORIZONTAL CENTERING (A3R313), AND HORIZONTAL COMMON MODE (A3R317)

NOTE

First perform step B1, then proceed.

B2. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:

DMM
  Range ..... 200 V

Signal Standardizer
  Amplitude ..... Midrange
  Position ..... Midrange
  Test ..... Vert or Horiz Aux In

Time Base
  Sweep Rate ..... 1 ms/Div
  Triggering
    Coupling ..... Right
    Source ..... AC
    Mode ..... Auto

C2932-503

a. Set the INTENSITY control for a visible trace.

b. Use the signal standardizer Position control to align the displayed trace with the center graticule line.

c. **CHECK**—Trace parallels the center graticule line, within 0.1 division.

d. **ADJUST**—Trace Rotation adjustment (R220) to align the trace with the center graticule line.

e. Set the signal standardizer Test selector switch to Vert or Horiz Com Mode.

f. **CHECK**—That the trace is within 0.05 division of the center graticule line.

g. **ADJUST**—Vertical Centering adjustment (R326) to overlay the displayed trace with the center graticule line.

h. Set the signal standardizer Test selector switch to Vert or Horiz Aux In.

i. Connect the DMM (digital multimeter) test leads between TP L130 and TP L123 (located on A3, XYZ board). Use the signal standardizer Position control to set the DMM reading to 0 volts, within 0.1 volt.

j. Connect the DMM meter leads between TP L130 and chassis ground.

k. **EXAMINE**—DMM reading for 55 volts, within 0.2 volts.

l. **ADJUST**—Vertical Common Mode adjustment (R225) for DVM reading of 55 volts, within 0.2 volts.

m. **INTERACTION**—If either R225 or R326 were adjusted in this step, repeat parts e through l.

n. Move the signal standardizer to the horizontal compartment and the time-base unit to the right vertical compartment.

o. Set the signal standardizer Test selector switch to Vert or Horiz Com Mode.

p. **CHECK**—That the trace aligns with the center graticule line within 0.1 division.

q. **ADJUST**—The Horizontal Centering adjustment (R313) to align the trace with the center graticule line.

r. Set the signal standardizer Test selector switch to Vert or Horiz Aux In.

s. Connect the DMM meter leads between TP L110 and TP L100 (located on A3, XYZ board).

t. Use the signal standardizer Position control to set the DMM reading to 0 volts within 0.1 volt.

u. Connect the DMM meter leads between TP L100 and chassis ground.

v. **ADJUST**—The Horizontal Common Mode adjustment (R317) for a DMM meter reading of 55 volts within 0.2 volts.

w. **INTERACTION**—If either R317 or R313 were adjusted in this step, repeat parts n through v.

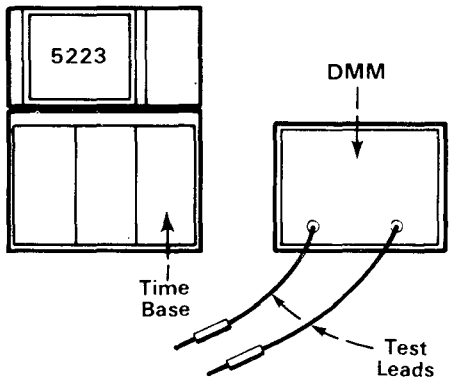
B3. EXAMINE/ADJUST CRT GRID BIAS (A4R411)

NOTE

If the preceding step was not performed, first perform B1, then proceed.

B3. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
DMM
Range ..... 200 V

Time Base
Sweep Rate ..... Amplifier Mode

C2932-504

a. Connect the DMM between test point P66, pin 1, and chassis ground.

b. Rotate the INTENSITY control clockwise to obtain a visible dot, then rotate the INTENSITY control counterclockwise so that the dot is just extinguished.

c. **EXAMINE**—DMM reading should be 19 to 21 volts.

d. **ADJUST**—Set the INTENSITY control for a DMM reading of 20 volts, and set the Preset Intensity adjustment (R411) so that the dot display on the crt is just extinguished.

NOTE

The instrument has to be on for at least 20 minutes to allow for stabilization of the crt grid cutoff voltage.

e. Disconnect the DMM test leads.

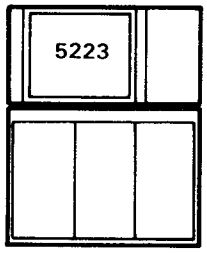
B4. CHECK/ADJUST PRESET FOCUS (A4R420), ASTIGMATISM (A3R900) GEOMETRY (A3R901), LOW FREQUENCY VERTICAL AND HORIZONTAL LINEARITY

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B4. SETUP CONDITIONS

5223 Controls:
- MEMORY CONTENTS
  - LEFT VERT PLUG-IN DISPLAY ..... In
  - L VS R ..... In
  - VECTOR MODE ..... In
  - LEFT VERT PLUG-IN SAVE ..... In
  - All other pushbuttons ..... Out
- POWER ..... Off



3715-607

a. Pull POWER switch ON.

b. Set the MEM INTEN control for a visible display.

c. Make sure the FOCUS control is still set to 1 o'clock.

d. Use the MEMORY CONTENTS VERT POSN and HORIZ POSN control to align the grid pattern with the graticule lines.

e. **CHECK**—Displayed grid pattern should be sharply focused and well defined.

f. **ADJUST**—Preset Focus adjustment (R420) and Astigmatism adjustment R900 for a well defined grid pattern.

g. **CHECK**—That the traces parallel the graticule lines within 0.1 division.

h. **ADJUST**—The Geometry adjustment (R901) so that the traces parallel the graticule lines, within 0.1 division.

i. **CHECK**—For 6 divisions of deflection between the second and eighth horizontal traces within 0.12 division and that the deflection between any two horizontal traces does not exceed 0.15 division.

j. **CHECK**—For 8 divisions of deflection between the second and tenth vertical traces within 0.08 division and that the deflection between any two vertical traces does not exceed 0.15 division.

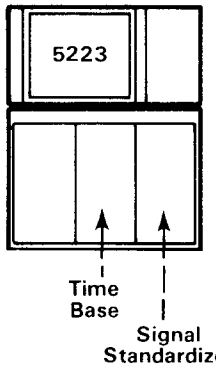
B5. CHECK/ADJUST HORIZONTAL REAL-TIME GAIN (A3R309)

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B5. SETUP CONDITIONS

5223 Controls:
POWER ..... Off
MEMORY CONTENTS
All pushbuttons ..... Out



Test Equipment Controls:
Signal Standardizer
Rep Rate ..... 1 kHz
Test ..... Vert or Horiz Gain

Time Base
Sweep Rate ..... 10 μs/Div
Triggering
Mode ..... Auto

C2932-506

a. Pull POWER switch ON.

b. Set the INTENSITY control for a visible display of eleven vertical traces.

c. Using the signal standardizer Position control, align the second vertical trace with the second graticule line.

d. **CHECK**—For 8 divisions of deflection between the second vertical trace and the tenth vertical trace, within 0.08 division, and that the deflection between any two vertical traces does not exceed 0.1 division.

e. **ADJUST**—Horizontal Real-Time Gain adjustment (R309) for 8 divisions of deflection between the second vertical trace and the tenth vertical trace, within 0.08 division, making sure that the deflection between any two vertical traces does not exceed 0.1 division.

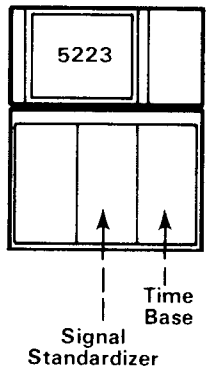
B6. CHECK/ADJUST VERTICAL REAL-TIME GAIN (A3R336), AND BEAMFINDER

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B6. SETUP CONDITIONS

5223 Controls:
No change in control settings



Test Equipment Controls:
Signal Standardizer
Rep Rate ..... 1 kHz
Test ..... Vert or Horiz Gain

Time Base
Sweep Rate ..... 10 μs/Div
Triggering
Mode ..... Auto

C2932-507

a. Set the INTENSITY control for a visible display of eleven horizontal traces.

b. Use the signal standardizer Position control to align the bright center trace with the graticule center line.

c. **CHECK**—For one trace per graticule division with six divisions of deflection between the third trace above and the third trace below the center bright trace, within 0.06 division.

d. **ADJUST**—Vertical Real-Time Gain adjustment (R336) for six divisions of deflection between the third trace above, and the third trace below, the center bright trace.

e. **CHECK**—For less than 0.2 division error in any two divisions of deflection anywhere on the crt screen.

f. Move the signal standardizer to the left vertical compartment.

g. **CHECK**—For one trace per graticule division with six divisions of deflection between the third trace above and the third trace below the bright center trace, within 0.06 division.

h. Set signal standardizer Test selector switch to Vert or Horiz Com Mode.

i. **EXAMINE**—The displayed trace should be within 1 division of the center graticule line.

j. Set the signal standardizer Test selector switch to Vert or Horiz Aux In.

k. Set the INTENSITY control fully counterclockwise.

l. **CHECK**—Press the BEAMFINDER pushbutton and check that a trace is visible and cannot be positioned off the crt screen with the signal standardizer and time-base Position controls.

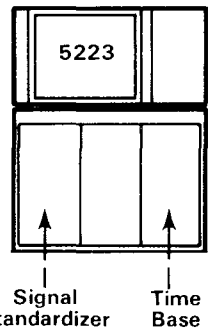
B7. EXAMINE/ADJUST VERTICAL AMPLIFIER STEP RESPONSE (A3C336, A3R437, A3C439, A3R438, AND A3C230)

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B7. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Signal Standardizer
Rep Rate ..... 100 kHz
Test ..... Vert or Horiz + Step Response

Time Base
Sweep Rate ..... 2 μs Div
Triggering
Mode ..... Auto
Slope ..... +
Source ..... Left

C2932-508

a. Set the signal standardizer Position and Amplitude controls for a 6-division display centered on the graticule area.

b. Set the time-base unit triggering controls for a stable display.

c. **EXAMINE**—Displayed pulse for a flat top and square corner that does not deviate more than 0.18 division, with the signal standardizer Rep Rate and time-base unit sweep rates given in Table 6-6.

d. **ADJUST**—Compensation adjustments #1, #2, #3, #4, and #5 (located on A3, XYZ board) as given in Table 6-6 for optimum flat top and square corner on the displayed waveform.

e. Move the signal standardizer to the center vertical compartment.

f. Set the signal standardizer Rep Rate switch to 100 kilohertz. Set the Amplitude and Position controls for a six-division display, centered on the graticule area.

TABLE 6-6
Frequency Compensation
(Signal Rep Rate vs. Sweep Rate)

Signal Standardizer Rep Rate	Sweep Rate	Adjustment
100 kHz	2.0 μs	Comp #1 (C336) Comp #2 (R437)
1 MHz	0.2 μs	Comp #3 (C439) Comp #4 (R438) Comp #5 (C230)

g. Set the time base sweep rate to 2 microseconds/division and triggering to right.

h. **EXAMINE**—Displayed pulse for a flat top and square corner that does not deviate more than 0.18 division with the signal standardizer Rep Rate and the time-base unit sweep rates given in Table 6-6.

i. **ADJUST**—If necessary, compromise the compensation adjustments #1, #2, #3, #4 and #5 as given in Table 6-6 for optimum flat top and square corner on the displayed pulse for the left and center vertical compartments.

B8. CHECK VERTICAL AMPLIFIER 12 MEGAHERTZ GAIN (A3C200)

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

a. Set the INTENSITY control for a visible display.

b. Set the sine-wave generator controls and amplifier Position control for a 6-division display centered on the graticule.

c. Without changing the sine-wave generator output amplitude, increase the sine-wave generator frequency until the displayed amplitude is reduced to 4.2 divisions.

d. **CHECK**—Sine-wave generator frequency is at least 12 megahertz.

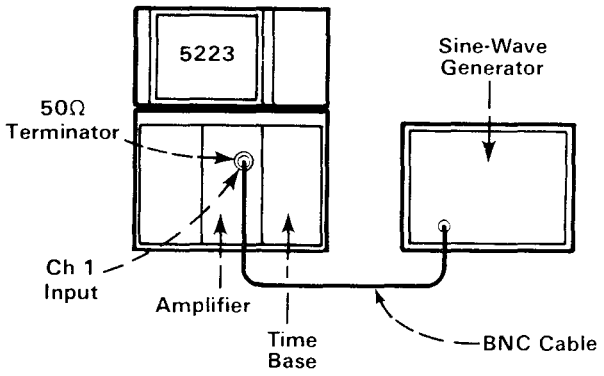
e. Move the signal standardizer to the left vertical compartment (leave signal connected).

f. **CHECK**—Repeat parts d through e for the left vertical compartment.

g. **ADJUST**—If the specifications of steps d or f were not met, perform step B7.

B8. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls
Amplifier
Channel 1 Deflection Factor ..... 20 mV/Div
Input Coupling ..... DC
Mode ..... Ch 1

Sine Wave Generator
Frequency Range ..... Ref 0.5 MHz

Time Base
Sweep Rate ..... 1 ms/Div
Triggering
Mode ..... Auto
Source ..... Right
Coupling ..... AC

C2932-509

h. Set the sine-wave generator to display a 2 division 10 megahertz signal.

i. Press the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY switch in.

j. Rotate the INTENSITY and MEM INTEN controls fully clockwise.

k. Set the time-base unit sweep rate to 0.2 microseconds/division and triggering controls for a stable 10 megahertz display.

l. Use the VERT POSN and HORIZ POSN to center the memory display vertically and horizontally on the crt.

m. Rotate the HORIZ EXP control fully clockwise and the MEM INTEN control fully counterclockwise.

n. **EXAMINE**—The extreme left portion of the displayed trace should appear normal with no distortion of the first sine-wave cycle.

o. **ADJUST**—The Horizontal HF Comp adjustment (C200) to minimize distortion of the first sine-wave cycle.

B9. CHECK HORIZONTAL TIMING

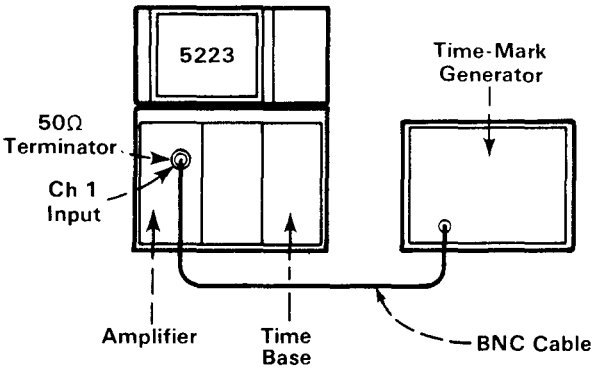
This step verifies that the 5223/time-base system will meet the sweep timing specifications of the time base being used.

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B9. SETUP CONDITIONS

5223 Controls:
Memory Contents
All Pushbuttons ..... Out



Test Equipment Controls:
Amplifier
Channel 1 Input Coupling ..... DC
Mode ..... Ch 1
Trigger ..... Ch 1

Time Base
Sweep Rate ..... 0.5 ms/Div
Triggering
Coupling ..... AC
Mode ..... Auto
Source ..... Left

C2932-510

a. Connect 1-millisecond markers from the time-mark generator to the amplifier unit input, and adjust the amplifier unit deflection factor for about 2 divisions of display. Set the INTENSITY control for desired viewing.

b. Set the time-base unit triggering controls for a stable display.

c. Position the first marker to the extreme left graticule line.

d. Set the time-base unit sweep calibration control for 1 marker at each major graticule division between the second and tenth graticule lines (center 8 divisions).

e. **CHECK**—Refer to the instruction manual Timing Specifications, for the time base being used, to check the systems high-frequency timing and linearity.

f. Return the time-base unit sweep calibration control to the calibrated position.

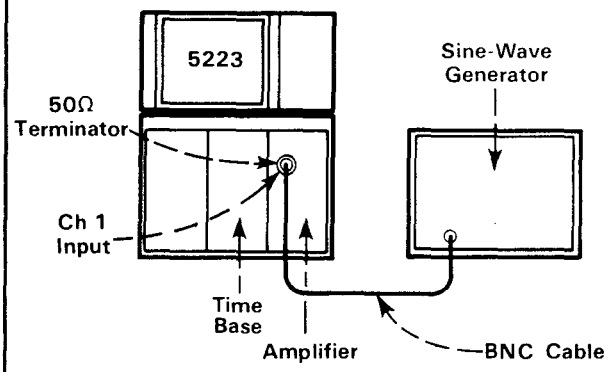
B10. CHECK HORIZONTAL BANDWIDTH

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B10. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Amplifier
Channel 1 Deflection Factor ..... 20 mV/Div
Channel 1 Input Coupling ..... DC
Mode ..... Ch 1

Sine-Wave Generator
Frequency Range ..... Ref ≈ .05 MHz

Time Base
Sweep Rate ..... 1 ms/Div
Triggering
Mode ..... Auto

C2932-511

a. Set the INTENSITY control for desired viewing.

b. Set the sine-wave generator for 8 divisions of 50 kilohertz signal centered on the 5223 crt.

c. Set the sine-wave generator output frequency to 7 megahertz.

d. **CHECK**—That the amplitude of the displayed 7 megahertz signal is at least 5.7 divisions.

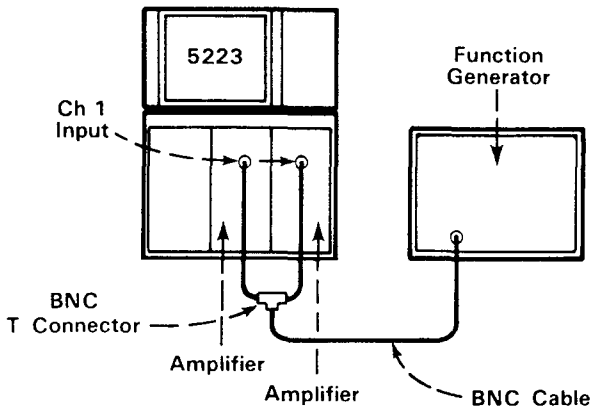
B11. CHECK XY OPERATION

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B11. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Amplifiers (Both)
Channel 1 Deflection Factor ..... 1 V/Div
Channel 1 Input Coupling ..... DC
Mode ..... Ch 1

Function Generator
Function ..... Sine Wave

C2932-512

a. Set the INTENSITY control for desired viewing.

b. Set the function generator Amplitude and Frequency controls to display 8 divisions of 20 kilohertz on the vertical and horizontal axis (diagonally).

c. **CHECK**—That the opening at the center of the displayed ellipse is not more than 0.35 divisions vertically.

C. MEMORY

Equipment Required: (Numbers correspond to those listed in Table 6-3, Test Equipment.)

1. Test Oscilloscope
2. Amplifier Unit (two required)
3. Time-base Unit
4. Signal Standardizer
6. Time-Mark Generator
7. Sine-Wave Generator
8. Function Generator
9. Coaxial Cable (two 18 inch, two 42 inch)
10. 50-Ohm Terminator
11. T Connector
12. Low-Capacitance Screwdriver
13. Screwdriver
14. GPIB Controller

Shaded lines identify Performance Requirement CHECK.

C1. MEMORY PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup Procedure given at the beginning of Part II—Adjustment and Performance Check.

b. Refer to Section 7, Instrument Options, and the Change Information at the rear of this manual for any modifications which may affect this procedure.

c. See **TEST POINT AND ADJUSTMENT LOCATIONS C** foldout page in Section 9, Diagrams and Circuit Board Illustrations.

d. Set the 5223 Digitizing Oscilloscope controls as follows:

POWER ..... ON
INTENSITY ..... Counterclockwise
FOCUS ..... Midrange
GRAT ILLUM ..... Midrange
MEM INTEN ..... Counterclockwise
MEMORY CONTENTS .....All pushbuttons out
  VERT EXP X1
  HORIZ EXP X1
  VERT POSN ..... Midrange
  HORIZ POSN ..... Midrange

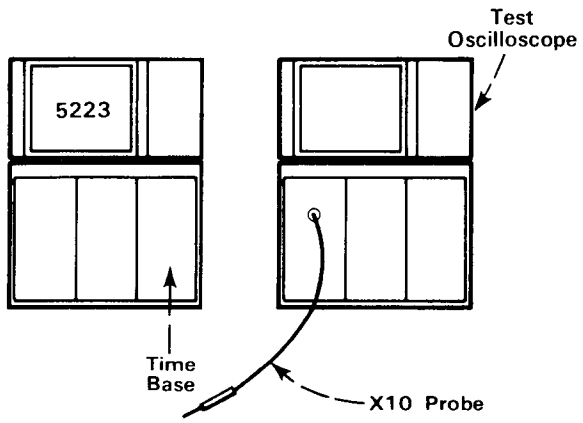
C2. EXAMINE/ADJUST MEMORY SEQUENCER CLOCK (A11C800, A11C801) AND READ CLOCK (A11R422)

NOTE

First perform step C1, then proceed.

C2. SETUP CONDITIONS

5223 Controls:
  MEMORY CONTENTS
    LEFT VERT PLUG-IN DISPLAY ..... In
    ROLL ..... In



Test Equipment Controls:
  Test Oscilloscope
    Vertical Deflection Factor ..... 1 V (including X10 probe)
    Sweep Rate ..... 0.2 µs/Div

  Time Base
    Sweep Rate ..... 0.1 s/Div
    Triggering
      Mode ..... Auto

C2932-513

a. Connect the test oscilloscope probe tip to pin 6 of J11, on the A11 Memory Board, which is accessible from the right side of the 5223 (see Test Point and Adjustment Locations C).

b. Set the test oscilloscope triggering controls to trigger on the positive going portion of the pulse.

c. **EXAMINE**—The test oscilloscope displayed pulse width must be within the limits of 535 to 585 nanoseconds.

NOTE

To gain access to adjustments in part d, g, and j, the 5223 (non-rackmount version) acquisition unit and display unit need to be separated; refer to the maintenance section in this manual for procedure.

d. **ADJUST**—Left Write Clock adjustment (C801), A11 Memory board, for a pulse width of 560 nanoseconds, on the test oscilloscope displayed pulse.

e. Move the test oscilloscope probe tip to pin 23 of J11.

f. **EXAMINE**—The test oscilloscope displayed pulse width must be within the limits of 535 to 585 nanoseconds.

g. **ADJUST**—Right Write Clock adjustment (C800) for a pulse width of 560 nanoseconds, on the test oscilloscope displayed pulse.

h. Connect the test oscilloscope probe tip to pin 3 of J11, and set the sweep rate to 1 microsecond/division.

i. **EXAMINE**—The test oscilloscope displayed pulse width must be within the limits of 4.05 to 4.95 microseconds.

j. **ADJUST**—Read Clock adjustment (R422) for a pulse period of 4.5 microseconds on the test oscilloscope displayed pulse.

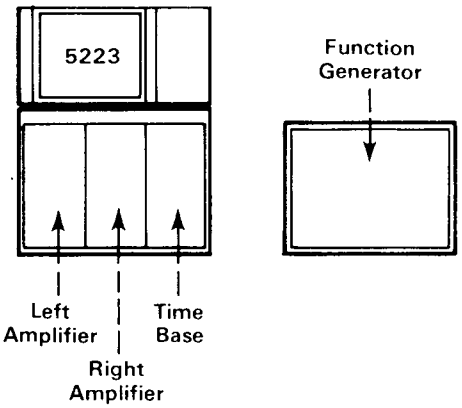
C3. EXAMINE/ADJUST VERTICAL AND HORIZONTAL POSITION SET (A18R295, A18R296)

NOTE

If the preceding step was not performed, first perform C1, then proceed.

C3. SETUP CONDITIONS

5223 Controls:
MEMORY CONTENTS
LEFT VERT PLUG-IN DISPLAY ..... Out
RIGHT VERT PLUG-IN DISPLAY ..... In



Test Equipment Controls
Left Amplifier
Display ..... On
Channel 1 Deflection Factor ..... 1 V/Div
Mode ..... Ch 1
Position ..... Midrange

Right Amplifier
Display ..... On
Channel 1 Deflection Factor ..... 1 V/Div
Mode ..... Ch 1
Position ..... Midrange

Function Generator
Frequency ..... 2 kHz

Time Base
Sweep Rate ..... 0.1 ms/Div
Triggering
Coupling ..... AC
Mode ..... Auto
Source ..... Left

C2932-514

a. Set the MEM INTEN control for a visible memory trace.

b. Use the VERT POSN control to position the displayed memory trace to a location on the crt where rotating the VERT EXP control does not cause the memory trace to move. Take care to not disturb the setting of the VERT POSN or VERT EXP controls until Step C4 is completed.

c. **EXAMINE**—The memory trace, must be within 0.5 divisions of the center graticule line.

d. **ADJUST**—Vertical Position Set adjustment (R295) to align the trace with the center graticule line (R295 is accessible on the right side of the 5223).

e. Set the INTENSITY control for desired viewing of the two real-time traces.

f. From the function generator apply an 8 division, 2 kilohertz sine-wave signal, to the left amplifier unit Channel 1 input.

g. Press the MEMORY CONTENTS LEFT PLUG-IN DISPLAY and MEMORY CONTENTS L VS R switches in.

h. Set the INTENSITY control fully counterclockwise.

i. Use the HORIZ POSN control to position the displayed memory trace to a location on the crt where rotating the HORIZ EXP control does not cause the displayed memory trace to move. Take care to not disturb the setting of the HORIZ POSN or HORIZ EXP controls until Step C4 is completed.

j. **EXAMINE**—The displayed trace must be within 0.1 division of the center graticule lines.

k. **ADJUST**—Horizontal Position Set adjustment (R296) to move the trace to the center graticule line (R296 is accessible on the right side of the 5223).

C4. CHECK/ADJUST MEMORY DISPLAY OUT GAIN (A3R630, A3R516)

NOTE

If the preceding step was not performed, first perform C1, then proceed.

a. Set the rear-panel GPIB switch to Test 3, see Figure 6-4.

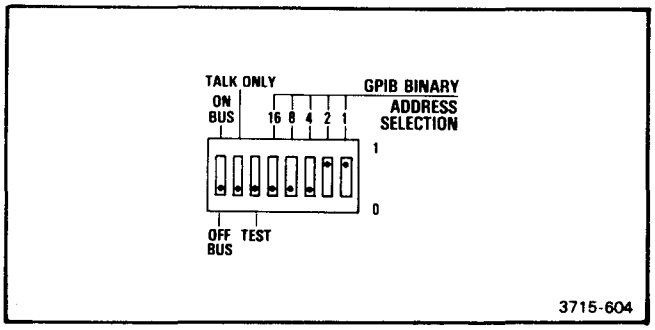
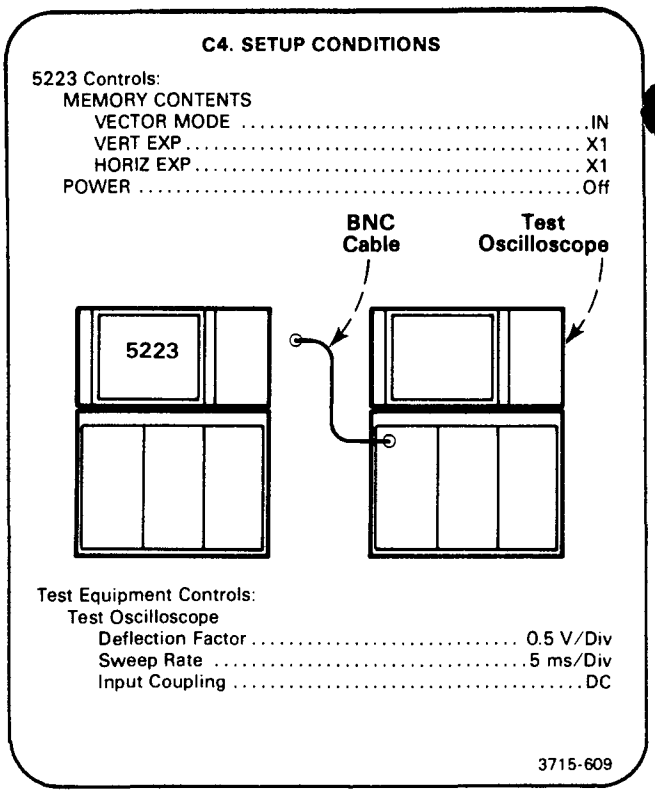


Figure 6-4. GPIB switch Test 3 selection.



b. Pull POWER switch ON.

c. Connect a bnc cable from the test oscilloscope vertical input to the MEMORY DISPLAY OUTPUTS Y connector on the rear-panel of 5223.

d. Set the DISPLAY OUT SPEED control to FAST (rear-panel).

e. **CHECK**—Observe test oscilloscope display for a signal transition of 2 volts (make sure test oscilloscope vertical deflection factor is accurate).

f. **ADJUST**—Set Y Display Out Gain adjustment (R630) for a 2 volt signal transition on the test oscilloscope.

g. Use the test oscilloscope position control to center the displayed waveform at the center graticule line.

h. Disconnect the bnc cable from the MEMORY DISPLAY OUTPUTS Y connector.

i. **CHECK**—The test oscilloscope displayed trace should be within 0.5 volts of the center graticule line. Before troubleshooting make sure the MEMORY CONTENTS VERT and HORIZ POSN controls were not disturbed from their settings in Step C3.

j. Connect the bnc cable from the test oscilloscope to the MEMORY DISPLAY X connector.

k. **CHECK**—Observe a signal transition of 2 volts on the test oscilloscope display.

l. **ADJUST**—Set the X Display Out Gain adjustment (R516) for a 2 volt display on the test oscilloscope.

m. Use the test oscilloscope Position control to center the displayed waveform at the center graticule line.

n. Disconnect the bnc cable from the MEMORY DISPLAY OUTPUTS X connector.

o. **CHECK**—The test oscilloscope displayed trace should be within 0.5 volts of the center graticule line. Before troubleshooting make sure the MEMORY CONTENTS VERT and HORIZ POSN controls were not disturbed from their settings in step C3.

p. Set the rear-panel GPIB selector switch as shown in Figure 6-3, page 6-31.

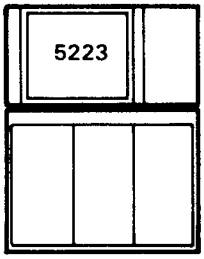
C5. EXAMINE/ADJUST—MEMORY GAIN (A4R420, A3R417)

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C5. SETUP CONDITIONS

5223 Controls:
- POWER ..... In
- INTENSITY ..... Fully counterclockwise
- MEM INTEN ..... Midrange
- MEMORY CONTENTS
  - LEFT VERT PLUG-IN DISPLAY ..... In
  - L VS R ..... In
  - VECTOR MODE ..... In
  - LEFT VERT PLUG-IN SAVE ..... In



3715-610

a. Pull the POWER switch ON.

b. Use the MEMORY CONTENTS VERT POSN and HORIZ POSN controls to align the displayed grid pattern with the vertical and horizontal graticule lines.

c. **EXAMINE**—For one trace per graticule division with six divisions of deflection between the third trace above and the third trace below the center vertical graticule line, within 0.1 division.

d. **ADJUST**—Vertical Memory Gain adjustment (R420) for six divisions of deflection between the third trace above and the third trace below the center graticule line.

e. **EXAMINE**—For one trace per graticule division with eight divisions of deflection between the second and tenth vertical traces, within 0.1 division.

f. **ADJUST**—Horizontal Memory Gain adjustment (R417) for eight divisions of deflection between the second and tenth traces.

g. Set the POWER switch off. Set all the MEMORY CONTENTS switches out and pull the POWER switch out.

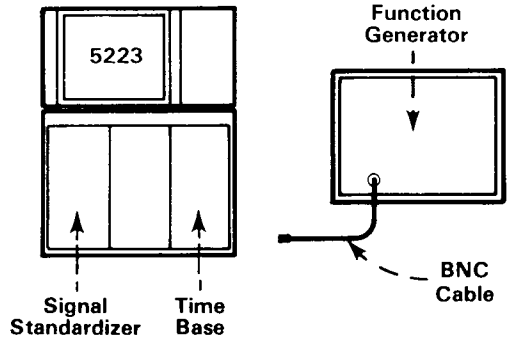
C6. CHECK/ADJUST DIGITIZER GAIN (A8R750, A8R350), LEFT AND RIGHT CENTERING (A8R560, A8R660), AND MONOTONICITY (A8R730)

NOTE

If the preceding step was not performed, first perform C1, then proceed.

C6. SETUP CONDITONS

5223 Controls:
- MEMORY CONTENTS
  - LEFT VERT PLUG-IN DISPLAY ..... In
  - All other pushbuttons ..... Out
  - VERT EXP X1
  - HORIZ EXP X1



Test Equipment Controls:
- Signal Standardizer
  - Test Vert or Horiz ..... Gain
  - Rep Rate ..... 1 KHz
- Timebase
  - Sweep Rate ..... 0.1 ms/Div
  - Triggering
    - Coupling ..... AC
    - Source ..... Left
    - Mode ..... Auto

3715-611

a. Set the INTENSITY control fully counterclockwise.

b. Set the MEM INTEN control for desired viewing.

c. Use the signal standardizer position control to align the bright trace with the center graticule line.

d. **CHECK**—For 6 divisions of deflection between the third trace above and the third trace below the center graticule line, within 0.18 division.

e. **ADJUST**—The Left Digitizer Gain adjustment (R750) for 6 divisions of deflection between the third trace above and the third trace below the center graticule line, within 0.1 division (accessible from the bottom of the 5223).

f. Move the signal standardizer to the center plug-in compartment. Press and release the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY switch.

g. Press the MEMORY CONTENTS RIGHT VERT PLUG-IN DISPLAY switch in and set the time-base unit triggering source to right and trigger level for a stable display.

h. **CHECK**—For 6 divisions of deflection between the third trace above and the third trace below the center graticule line, within 0.18 division.

i. **ADJUST**—The Right Digitizer Gain adjustment (R350) for 6 divisions of deflection between the third trace above and the third trace below the center graticule line, within 0.1 division. (accessible from the bottom of the 5223).

j. Set the signal standardizer Test selector switch to Vert or Horiz Com Mode, and the INTENSITY control for desired viewing.

k. **EXAMINE**—The displayed memory trace should align with the real-time trace, within 0.2 division.

l. **ADJUST**—Right Center adjustment (R560) to exactly overlay the memory displayed trace with the right vertical real-time trace.

m. Move the signal standardizer to the left vertical compartment.

n. Set the MEMORY CONTENT(S) LEFT VERT PLUG-IN DISPLAY switch in and the MEMORY CONTENT(S) RIGHT VERT PLUG-IN DISPLAY switch out.

o. **EXAMINE**—The displayed traces should align with the center graticule line, within one division.

p. **ADJUST**—Left Center adjustment (R660) to exactly overlay the left-vertical memory displayed trace with the left vertical real-time trace.

q. Set the signal standardizer Test selector switch to Aux In.

r. Set the VERT POSN, VERT EXP. HORIZ POSN. and HORIZ EXP controls to midrange.

s. Connect the function generator to the signal standardizer Aux In input and set the Amplitude to display six divisions of the triangular waveform on the 5223 crt.

t. Set the Intensity control fully counterclockwise, and the time-base Triggering Source to Left.

u. **EXAMINE**—The triangular waveform for smooth straight slopes.

v. **ADJUST**—The Monotonicity adjustment (R370) for optimum smooth straight slopes on the triangular waveform.

@

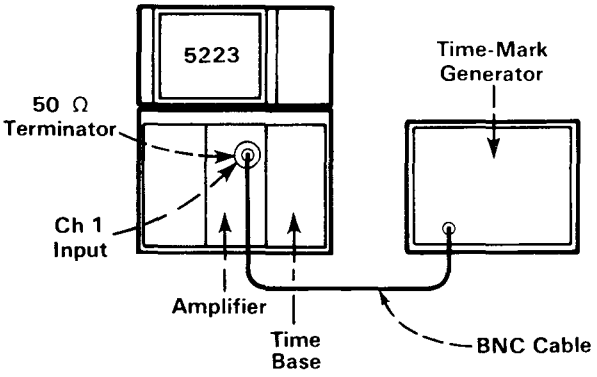
C7. CHECK REAL-TIME MATCH AND MEMORY TIMING MATCH

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C7. SETUP CONDITIONS

5223 Controls:
- MEMORY CONTENTS
  - RIGHT VERT PLUG-IN DISPLAY ..... In
  - All other pushbuttons ..... Out
  - VERT EXP X1
  - HORIZ EXP X1



Test Equipment Controls:
- Amplifier
  - Channel 1 Deflection Factor ..... 1 V/Div
  - Mode ..... Ch 1
  - Trigger ..... Ch 1
- Time-Mark Generator ..... 0.5 ms Markers
- Time Base
  - Sweep Rate ..... 0.5 ms/Div
  - Triggering
    - Source ..... Right
    - Coupling ..... AC
    - Mode ..... Auto

C2932-518

a. Connect the output of the time-mark generator to the input of the vertical amplifier unit through a 50Ω terminator.

b. Set the INTENSITY and MEM INTEN controls for desired viewing.

c. Set the time-base unit triggering control for a stable display.

d. Align both memory and real-time second time markers with the second left-most graticule line.

e. **CHECK**—That the memory display matches the real-time display within 0.24 division at the tenth graticule line; if not within 0.24 division, see digitizer time-base calibration procedure. C5

f. Rotate the MEM INTEN control fully counterclockwise.

g. Rotate the time-base unit Position control to equalize errors at the second and tenth time markers with the second and tenth graticule lines.

h. **CHECK**—That the sixth (center) time mark aligns with the graticule center line, within 0.2 divisions.

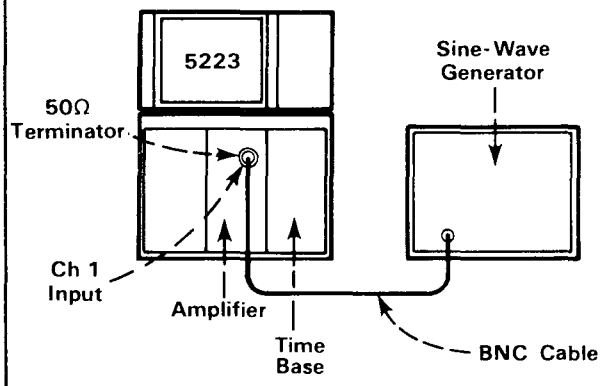
C8. CHECK DIGITIZER BANDWIDTH

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C8. SETUP CONDITIONS

5223 Controls:
- INTENSITY ..... Fully counterclockwise



Test Equipment Controls:
- Amplifier
  - Channel 1 Deflection Factor ..... 0.5 V/Div
  - Display ..... On
  - Position ..... Midrange
- Time Base
  - Sweep Rate ..... 10 μs/Div
  - Triggering ..... Auto
- Sine-Wave Generator ..... Ref ≈ .05 MHz

C2932-519

a. Set the MEM INTEN control for desired viewing.

b. Set the sine-wave generator to display 6 divisions of the 50 kilohertz signal, centered on the crt.

c. Set the time-base unit sweep rate to 0.2 microseconds/division and the sine-wave generator frequency to 10 megahertz.

d. **CHECK**—Memory display for at least 4.2 divisions of signal.

e. Move the amplifier unit to the left vertical compartment.

f. Press the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY switch in, and press and release the MEMORY CONTENTS RIGHT DISPLAY switch.

g. Set the sine-wave generator to display 6 divisions of 50 kilohertz signal centered on the crt.

h. Set the sine-wave generator to 10 megahertz and the time-base unit Triggering to Left.

i. **CHECK**—Memory display for at least 4.2 divisions of displayed signal.

C9. CHECK DIGITIZER ABERRATIONS AND BLOWBY

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

a. Set the signal standardizer Amplitude and Position controls for 5 division pulses centered on the crt.

b. **CHECK**—That the flat top of the memory display matches the real-time display within 0.05 division.

c. **CHECK**—That the memory display aberrations are less than 0.15 division.

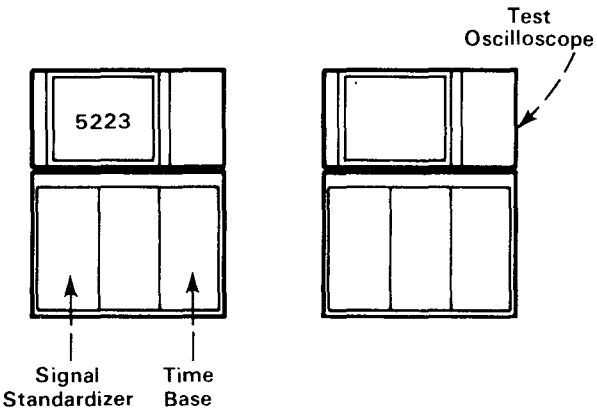
d. Remove the signal standardizer from the left vertical compartment and install it in the right vertical compartment.

e. Set the time-base unit triggering source switch to Right.

f. **CHECK**—Repeat parts b and c for the right vertical memory display.

C9. SETUP CONDITIONS

5223 Controls:
- INTENSITY ..... For desired viewing
- MEM INTEN ..... For desired viewing
- MEMORY CONTENTS
  - LEFT PLUG—IN DISPLAY ..... In
  - RIGHT PLUG-IN DISPLAY ..... In
  - All other pushbuttons ..... Out



Test Equpment Controls:
- Signal Standardizer
  - Test Selector switch ..... Vert or Horiz + Step Resp
  - Rep Rate ..... 1 MHz
- Time Base
  - Sweep Rate ..... 0.2 μs/Div
  - Triggering
    - Coupling ..... AC
    - Source ..... Left
    - Mode ..... Auto
- Test Oscilloscope
  - Vertical Deflection Factor ..... 50 mV/Div
  - Sweep Rate ..... 0.2 μs/Div

C2932-520

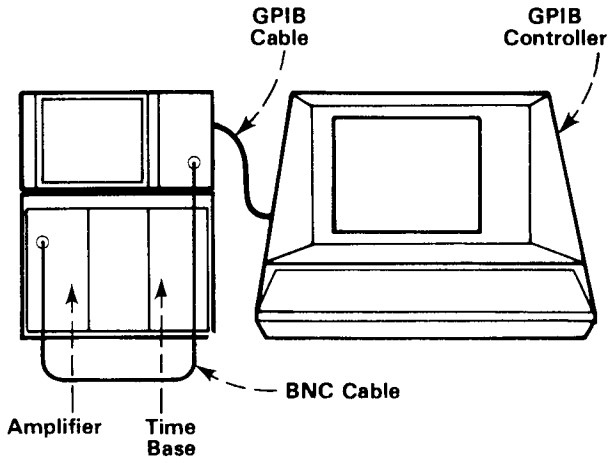
C10. EXAMINE GPIB OPERATION

NOTE

If the preceding step was not performed, first perform step C1, then proceed.

C10. SETUP CONDITIONS

5223 Controls:
- MEMORY CONTENTS
  - All pushbuttons ..... Out
  - VERT POSN ..... Midrange
  - HORIZ POSN ..... Midrange
  - VERT EXT X1
  - HORIZ EXT X1
- INTENSITY ..... Clockwise
- MEM INTEN ..... Clockwise



Test Equipment:
- Amplifier
  - Deflection Factor ..... 0.2 V/Div
  - Coupling ..... DC
- Time Base
  - Sweep Rate ..... 0.5 ms/Div
  - Triggering
    - Mode ..... Auto
    - Source ..... Left

3715-613

a. Set the rear-panel GPIB selector switch as shown in Figure 6-5.

b. Use the Amplifier Position control align the display waveform with center graticule line.

c. Enter the program, on page 6-50, into the 4050-series GPIB Controller:

d. Initiate the GPIB Controller program by executing the RUN command.

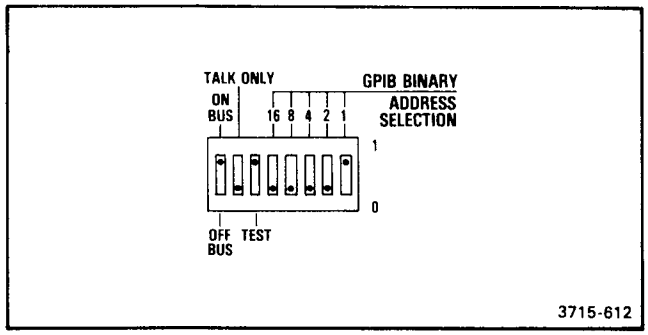


Figure 6-5. Address 1 selected for 5223.

```
100 POLL A1,A2;1
110 ON SRQ THEN 560
120 PRINT @1:"ID?"
130 INPUT @1:A$
140 PRINT "ID QUERY RESPONSE : ";A$
150 REM REMOTE ENABLE FUNCTION TEST
160 E1=0
170 PRINT @1:"SEL DISP.L"
180 GOSUB 630
190 IF NOT(E1) THEN 210
200 PRINT "ERROR ** 5223 DID NOT RESPOND TO REMOTE ENABLE ";
210 E1=0
220 WBYTE @33,1:ASC("R"),ASC("E"),ASC("L"),32
230 WBYTE @63:
240 GOSUB 630
250 IF E1 THEN 280
260 PRINT "ERROR ** 5223 DID NOT RESPOND TO 'GO TO LOCAL' COMMAND "
270 REM TEST TALKED-WITH-NOTHING-TO-SAY
280 PRINT @1:"ID?"
290 WBYTE @20,65:
300 RBYTE B1
310 IF B1=255 THEN 350
320 PRINT "ERROR ** TALKED-WITH-NOTHING-TO-SAY DID NOT WORK"
330 STOP
340 REM TEST INTERFACE CLEAR
350 WBYTE @20:
360 POLL A1,A2;1
370 IF NOT(A2) THEN 390
380 PRINT "ERROR ** DEVICE CLEAR DID NOT CLEAR STATUS BYTE "
390 WBYTE @24:
400 INIT
410 WBYTE @65:
420 RBYTE B1
430 IF B1 THEN 470
440 PRINT "ERROR ** INTERFACE CLEAR DID NOT RETURN SERIAL POLL"
450 PRINT "                FUNCTION TO IDLE STATE"
460 GO TO 480
470 IF B1<>255 THEN 320
480 WBYTE @95,20:
490 REM WAVEFORM TRANSFER TEST
500 DIM W$(6000)
510 PRINT @1:"ACCESS LEFT;ASCII;CURVE?"
520 INPUT @1:W$
530 PRINT @1:"WFMPRE WFID:R;";W$
540 WBYTE @35,1:
550 END
560 REM SERIAL POLL ROUTINE
570 POLL A1,A2;1
580 IF A2<>98 AND A2<>114 THEN 610
590 E1=1
600 RETURN
610 PRINT"UNEXPECTED SRQ OF ";A2
620 RETURN
630 REM TIME-DELAY PROGRAM
640 FOR I9=1 TO 50
650 PRINT " H";
660 NEXT I9
670 RETURN
```

D. CALIBRATOR AND INPUT/OUTPUT SIGNALS

Equipment Required: (Numbers correspond to those listed in Table 6-3, Test Equipment.)

1. Test Oscilloscope
2. Amplifier Unit (Two required)
3. Time-Base Unit
4. Signal Standardizer
5. DMM (digital multimeter)
6. Time-Mark Generator
7. Sine-Wave Generator
9. Coaxial Cable (two 18 inch, one 42-inch required)
11. T Connector
13. Screwdriver

Shaded lines identify Performance Requirement CHECK.

D1. CALIBRATOR AND INPUT/OUTPUT SIGNALS PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup Procedure given at the beginning of Part II-Adjustment and Performance Check.

b. Refer to Section 7, Instrument Options, and the Change Information at the rear of this manual for any modifications which may affect this procedure.

c. See **TEST POINT AND ADJUSTMENT LOCATIONS D** foldout page in Section 9, Diagrams and Circuit Board Illustrations.

d. Set 5223 Digitizing Oscilloscope controls as follows:

POWER ..... ON
INTENSITY ..... Counterclockwise
FOCUS ..... Midrange
GRAT ILLUM ..... Midrange
MEM INTEN ..... Counterclockwise
MEMORY CONTENTS .....All pushbuttons out
VERT EXP X1
HORIZ EXP X1
VERT POSN ..... Midrange
HORIZ POSN ..... Midrange

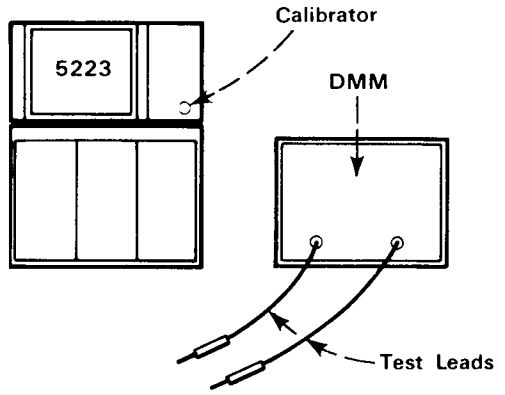
D2. CHECK CALIBRATOR OUTPUT VOLTAGE

NOTE

First perform step D1, then proceed.

D2. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls
DMM
Voltage Range ..... 2 V

C2932-521

a. Remove Q112 from the A2 Front-Panel board.

b. Connect the precision dc voltmeter to the CALIBRATOR output connector.

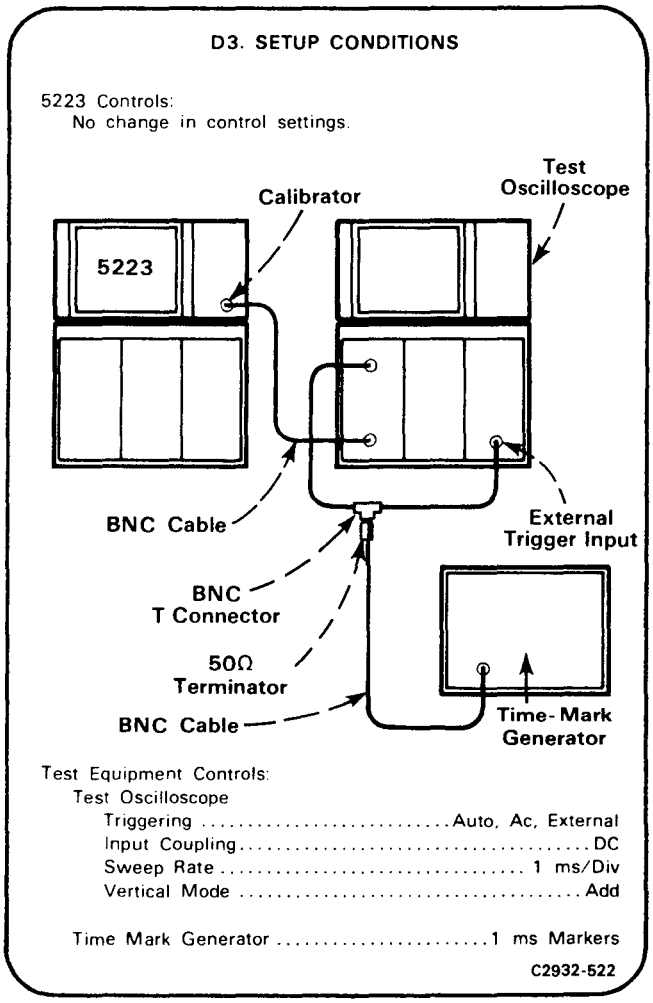
c. **CHECK**—Meter reading for 300 millivolts, within the limits of 298 to 302 millivolts.

d. Replace Q112 in the A2 Front-Panel board.

D3. CHECK/ADJUST CALIBRATOR 1 kHz REPETITION RATE (A2R204)

NOTE

If the preceding step was not performed, first perform step D1, then proceed.



NOTE

A frequency counter with an accuracy of at least 0.1% may be used to adjust the CALIBRATOR repetition rate.

a. Use a bnc T-connector to apply 1 millisecond time-markers to the test oscilloscope external trigger input and the channel 1 vertical input. Connect the 5223 CALIBRATOR output to the Channel 2 vertical input of the test oscilloscope.

b. Set the test oscilloscope triggering level for a stable time-mark display.

c. Set the test oscilloscope vertical deflection factors to display 2 divisions of CALIBRATOR signal and 1 division of time-marker signal.

d. Set the test oscilloscope sweep rate for 0.5 second/division.

e. **CHECK**—The time required for the 1 millisecond time marks to drift from the positive level of the CALIBRATOR signal to the negative level, and back to the positive level must be more than 1.0 second (2 divisions). This time can be measured directly from the display by observing the number of divisions that the markers move across the display area, before it returns to the positive level, in one second.

f. **ADJUST**—Freq Trim adjustment (R204) for minimum drift.

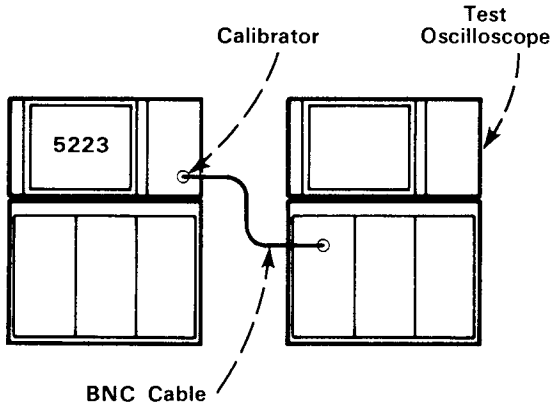
D4. CHECK CALIBRATOR DUTY CYCLE

NOTE

If the preceding step was not performed, first perform step D1, then proceed.

D4. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Test Oscilloscope
Vertical Deflection ..... 100 mV/Div
Sweep Rate ..... 1 ms/Div
Triggering
Slope ..... +
Coupling ..... AC
Mode ..... Auto
Source ..... Left

C2932-523

a. Set the test oscilloscope triggering for positive slope and auto mode with ac coupling from the internal source at a sweep rate of 0.1 millisecond/division. Set the triggering controls so that the display starts at the 50% point on the rising edge of the waveform.

b. Set the test oscilloscope sweep magnifier to X10. Then, position the display horizontally so the falling edge of the waveform aligns with the center vertical graticule line.

c. Set the test oscilloscope triggering to negative slope.

d. **CHECK**—The 50% point on the rising edge of the waveform now displayed is within 2.0 divisions horizontally of the center line. (Indicates duty cycle of 50% within 2%.)

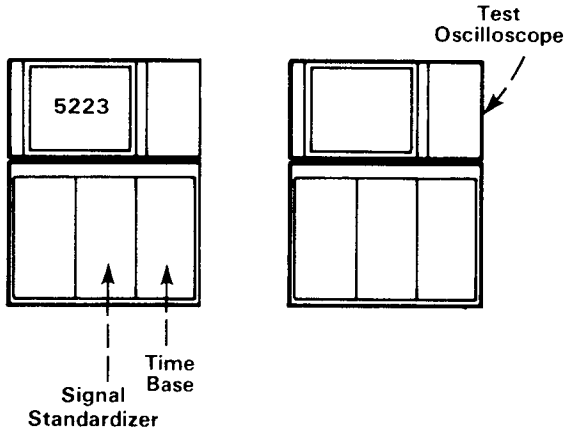
D5. CHECK RIGHT VERTICAL, LEFT VERTICAL, HORIZONTAL, A GATE OUT OR SAMPLE CLOCK OUT AND MEMORY X AND Y DISPLAY OUTPUTS

NOTE

If the preceding step was not performed, first perform step D1, then proceed.

D5. SETUP CONDITIONS

5223 Controls:
MEMORY CONTENTS
All pushbuttons ..... Out



Test Equipment Controls:
Signal Standardizer
Test Selector switch ..... Vert or Horiz Gain
Rep Rate ..... 100 kHz

Test Oscilloscope
Sweep Rate ..... 0.5 ms/Div
Vertical Deflection Factor ..... 50 mV/Div

Time Base
Sweep Rate ..... 1 ms/Div

C2932-524

a. Connect the input of the test oscilloscope to the PLUG-IN OUTPUTS RIGHT VERT connector (located on the 5223 rear-panel) with a bnc cable and position the bright trace (test oscilloscope) to the center graticule line.

b. **CHECK**—That there is 6 divisions of deflection between the third trace above and below the center graticule line on the test oscilloscope display, within 0.3 division.

c. Remove the signal standardizer from the right vertical compartment and install it in the left vertical compartment.

d. Disconnect the bnc cable from the PLUG-IN OUTPUTS RIGHT VERT connector and connect it to the PLUG-IN OUTPUTS LEFT VERT connector. Position the bright trace to the center graticule line.

e. **CHECK**—That there is 6 divisions of deflection between the third trace above and below the center graticule line on the the test oscilloscope display, within 0.3 division.

f. Set the signal standardizer Test selector switch to Vert or Horiz + step Resp, Rep Rate to 1 kilohertz, and the Amplitude control for a 4 division display on the 5223 crt.

g. Use a bnc cable to connect the MEMORY DISPLAY OUTPUT Y connector (rear panel) to the test oscilloscope vertical input.

h. Set the test oscilloscope vertical deflection factor to 0.5 volts, and the sweep rate to 0.1 seconds.

i. Set the rear-panel DISPLAY OUT SPEED control to FAST.

j. Press the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY and SAVE switches in.

k. **CHECK**—Press the MEMORY CONTENTS OUTPUT SAVED DISPLAY(S) switch in and observe the test oscilloscope display for a square-wave signal.

l. Move the bnc cable to the MEMORY DISPLAYS OUTPUT X connector, and set the test oscilloscope sweep rate to 1 second/division.

m. **CHECK**—Press the MEMORY CONTENTS OUTPUT SAVED DISPLAY(S) switch and observe the test oscilloscope display for one sawtooth cycle.

n. Remove the signal standardizer from the left vertical compartment, and install amplifier units in the left and right vertical compartments.

o. Set the time-base sweep unit rate to 0.5 millisecond/division, and move the bnc cable from the MEMORY DISPLAY OUTPUTS connector to the A GATE OUT OR SAMPLE CLK OUT connector.

p. Set the test oscilloscope deflection factor to 1 volt/division.

q. **CHECK**—For an A Gate signal on the test oscilloscope that is TTL compatible; rectangular waveform with the positive excursion greater than +2.4 volts and a baseline of +0.8 volt or less. If the instrument under test is set to output the CLK (Sample Clock) signal, move shorting plug on P940, located on A9 Interface board, to select the A Gate signal as shown on Test Point and Adjustment Locations C.

r. Move the shorting plug on P940, located on A9 Interface board, back to the CLK (Sample Clock) position. (See Test Point and Adjustment Locations C.)

s. Set the test oscillosocpe sweep rate to 5 microseconds/division.

t. **CHECK**—That a Sample Clock pulse is TTL compatible and occurs every 5 microseconds.

u. Move the shorting plug on P940 to the A GATE position.

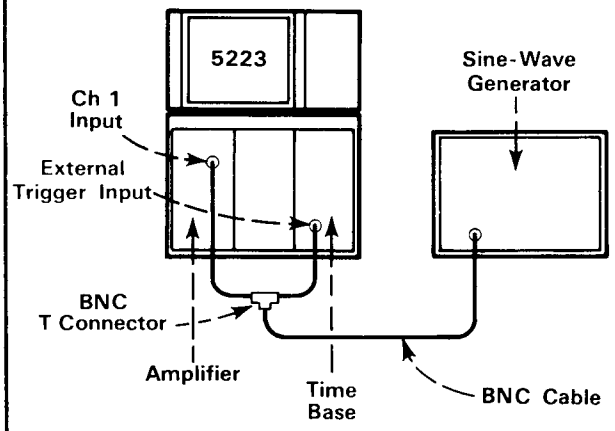
D6. CHECK Z-AXIS, SS RESET AND PEN LIFT OUTPUTS

NOTE

If the preceding step was not performed, perform step D1, then proceed.

D6. SETUP CONDITIONS

5223 Controls:
No change in control settings.



Test Equipment Controls:
Amplifier
Channel 1 Deflection Factor ..... 1 V/Div

Sine-Wave Generator ..... 1 MHz

Time Base
Sweep Rate ..... 1 ms/Div
Triggering
Coupling ..... AC
Source ..... Right
Mode ..... Auto

C2932-525

a. Set the signal generator Amplitude control and time-base unit Triggering controls for a 5 division stable display on the 5223 crt.

b. Disconnect the bnc cable from the amplifier input connector and connect it to the rear-panel Z-AXIS INPUT connector.

c. **CHECK**—Rotate the INTENSITY control and check that the displayed trace intensity is modulated by the one megahertz signal.

d. Set the time-base unit sweep rate to 5 milliseconds/division.

e. Set the INTENSITY control for desired viewing.

f. Press the Single-Sweep Reset pushbutton on the time-base unit.

g. **CHECK**—While shorting the center conductor on the rear panel SS RESET connector to ground, observe one sweep of the crt.

h. Connect the DMM (digital multimeter) leads between ground and the middle pin on the camera power connector.

i. **CHECK**—While shorting the center conductor on the rear panel SS RESET connector to ground, notice that the meter reading changes to zero.

j. Press the MEMORY CONTENTS LEFT VERT PLUG-IN DISPLAY and SAVE switches in.

k. Connect the DMM set to measure resistance between the two PEN LIFT banana plug connectors (located on the rear panel).

l. Make sure the shorting strap plug on P929 is on pins 1 and 2.

m. **CHECK**—Press the MEMORY CONTENTS OUTPUT SAVED DISPLAY(S) switch and notice that the meter reading indicates approximately zero ohms.

n. Move shorting strap plug on P929 to pins 2 and 3.

o. **CHECK**—Press the MEMORY CONTENTS SAVED DISPLAY(S) switch and notice that the DMM reading changes from zero to >20 megohms.

This concludes Part II—Adjustment and Performance Check.

INSTRUMENT OPTIONS

Your instrument may be equipped with one or more instrument options. A brief description of each available option is given in the following discussion. Option information is incorporated into the appropriate sections of the manual. Refer to Table 7-1 and the Table of Contents for location of option information. For further information on instrument options, see your Tektronix Products catalog or contact your Tektronix Field Office.

LIST OF OPTIONS

OPTION 05

Allow the Instrument to operate from a 48 to 440 Hz line frequency. Option 05 is available for the rackmount 5223 only (not available on the bench model) and is installed at the factory.

OPTION 10

Provides GPIB compatibility and is factory installed. A separate Operators and Service manual is available for the 5223 Option 10 (GPIB) instrument.

OPTION A1

The standard power cord is replaced with the Universal European 240-volt type power cord (Tektronix Part 161-0066-09).

OPTION A2

The standard power cord is replaced with the United Kingdom 240-volt type power cord (Tektronix Part 161-0066-10).

OPTION A3

The standard power cord is replaced with the Australian 240-volt type power cord (Tektronix Part 161-0066-11).

OPTION A4

The standard power cord is replaced with the North American 240-volt type power cord (Tektronix Part 161-0066-12).

INSTRUMENT OPTION IDENTIFICATION

OPTION 05

Nomenclature on the rear panel will indicate if Option 05 is installed. ed.

OPTION 10

The 5223 Option 10 instrument is equipped with a GPIB connector and Address Selector switch on the rear panel.

OPTION A1, A2, A3, AND A4

Refer to Figure 1-1 in this manual to determine type of cord used with your instrument.

TABLE 7-1
Option Information Locator

Option	Location in Manual		Information
	Section	Heading	
05	7 Instrument Options	Option 05	Gives a brief description of Option 05.
10	All Sections		Option 10 information is included throughout this manual.
A1	1 General Information	Power Cord Information Figure 1-1.	Lists details of Option A1.
	7 Instrument Options	Option A1	Gives a brief description of Option A1.
A2	1 General Informmation	Power Cord Information Figure 1-1	Lists details of Option A2.
	7 Instrument Options	Option A2	Gives a brief description of Option A2.
A3	1 General Information	Power Cord Information Figure 1-1.	Lists details of Option A3.
	7 Instrument Options	Option A3	Gives a brief description of Option A3.
A4	1 General Information	Power Cord Information Figure 1-1	Lists details of Option A4.
	7 Instrument Options	Option A4	Gives a brief description of Option A4.

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REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

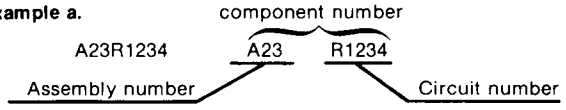
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

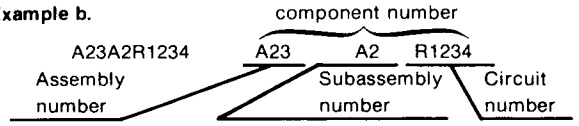
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00213	NYTRONICS, COMPONENTS GROUP, INC., SUBSIDIARY OF NYTRONICS, INC.	ORANGE STREET	DARLINGTON, SC 29532
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01281	TRW ELECTRONIC COMPONENTS, SEMICONDUCTOR OPERATIONS	14520 AVIATION BLVD.	LAWNDALE, CA 90260
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
01995	THONET-WISCONSIN INC.	911 N 11TH ST.	SHEBOYGAN, WI 53081
02111	SPECTROL ELECTRONICS CORPORATION	17070 EAST GALE AVENUE	CITY OF INDUSTRY, CA 91745
02735	RCA CORPORATION, SOLID STATE DIVISION	ROUTE 202	SOMERVILLE, NY 08876
02777	HOPKINS ENGINEERING COMPANY	12900 FOOTHILL BLVD.	SAN FERNANDO, CA 91342
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
03888	KDI PYROFILM CORPORATION	60 S JEFFERSON ROAD	WHIPPANY, NJ 07981
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
08806	GENERAL ELECTRIC CO., MINIATURE LAMP PRODUCTS DEPARTMENT	NELA PARK	CLEVELAND, OH 44112
09023	CORNELL-DUBILIER ELECTRONIC DIVISION FEDERAL PACIFIC ELECTRIC CO.	2652 DALRYMPLE ST.	SANFORD, NC 27330
12697	CLAROSTAT MFG. CO., INC.	LOWER WASHINGTON STREET	DOVER, NH 03820
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
14552	MICRO SEMICONDUCTOR CORP.	2830 F FAIRVIEW ST.	SANTA ANA, CA 92704
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
14859	TEXAS INSTRUMENTS INC., CONTROL DIV.	300 NORTH MAIN	VERSAILLES, KY 40383
14936	GENERAL INSTRUMENT CORP., SEMICONDUCTOR PRODUCTS GROUP	P.O. BOX 600,600 W. JOHN ST.	HICKSVILLE, NY 11802
15454	RODAN INDUSTRIES, INC.	2905 BLUE STAR ST.	ANAHEIM, CA 92806
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
23936	PAMOTOR DIV., WILLIAM J PURDY COMPANY	770 AIRPORT BLVD.	BURLINGAME, CA 94010
24546	CORNING GLASS WORKS, ELECTRONIC COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
50157	MIDWEST COMPONENTS INC.	P. O. BOX 787 1981 PORT CITY BLVD.	MUSKEGON, MI 49443
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
52648	PLESSEY SEMICONDUCTORS	1641 KAISER	IRVINE, CA 92714
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
54590	RCA CORP., ELECTRONIC COMPONENTS DIV.	415 S. 5TH STREET	HARRISON, NJ 07029
55210	GETTIG ENG. AND MFG. COMPANY	PO BOX 85, OFF ROUTE 45	SPRING MILLS, PA 16875
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
73899	JFD ELECTRONICS COMPONENTS CORP.	PINETREE ROAD	OXFORD, NC 27565
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
76493	BELL INDUSTRIES, INC., MILLER, J. W., DIV.	19070 REYES AVE., P O BOX 5825	COMPTON, CA 90224
76854	OAK INDUSTRIES, INC., SWITCH DIV.	S. MAIN ST.	CRYSTAL LAKE, IL 60014
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80031	ELECTRA-MIDLAND CORP., MEPCO DIV.	22 COLUMBIA ROAD	MORRISTOWN, NJ 07960
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E. WASHINGTON STREET P. O. BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
91929	HONEYWELL, INC., MICRO SWITCH DIV.	CHICAGO & SPRING STS.	FREEPORT, IL 61032
95348	GORDOS CORPORATION	250 GLENWOOD AVENUE	BLOOMFIELD, NJ 07003

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-5961-00			CKT BOARD ASSY:GRATICULE ILLUMINATION	80009	670-5961-00
A2	670-5943-00			CKT BOARD ASSY:FRONT PANEL	80009	670-5943-00
A3	670-5944-00			CKT BOARD ASSY:XYZ AMPLIFIER	80009	670-5944-00
A4	670-2128-10			CKT BOARD ASSY:HI VOLTAGE	80009	670-2128-10
A5	670-4856-02			CKT BOARD ASSY:FOCUS D.C.RESTORER	80009	670-4856-02
A6	670-4856-03			CKT BOARD ASSY:Z AXIS D.C.RESTORER	80009	670-4856-03
A7	670-5948-00			CKT BOARD ASSY:POWER SUPPLY	80009	670-5948-00
A8	670-5949-00			CKT BOARD ASSY:DIGITIZER	80009	670-5949-00
A9	670-5947-00			CKT BOARD ASSY:INTERFACE	80009	670-5947-00
A11	670-5946-00			CKT BOARD ASSY:MEMORY	80009	670-5946-00
A14	670-6311-00			CKT BOARD ASSY:CONNECTOR (OPTION 10 ONLY)	80009	670-6311-00
A15	670-6312-00			CKT BOARD ASSY:REAR PANEL (OPTION 10 ONLY)	80009	670-6312-00
A16	670-6314-00			CKT BOARD ASSY:GPIB INTERCONNECT	80009	670-6314-00
	----- -----			(NO ELECTRICAL PARTS)(OPTION 10 ONLY)		
A17	670-6314-00			CKT BOARD ASSY:GPIB INTERCONNECT	80009	670-6314-00
	----- -----			(NO ELECTRICAL PARTS) (OPTION 10 ONLY)		
A18	670-5951-00			CKT BOARD ASSY:GPIB (OPTION 10 ONLY)	80009	670-5951-00
A1	----- -----			CKT BOARD ASSY:GRATICULE ILLUMINATION		
A1DS	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,SEL	76854	17AS15
A1W365	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	----- -----			CKT BOARD ASSY:FRONT PANEL		
A2C110	285-0808-00			CAP.,FXD,PLSTC:0.1UF,10%,50V	56289	LP66A1A104K004
A2C111	290-0778-00			CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A2C112	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C113	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C210	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A2CR210	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2Q110	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A2Q111	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2Q112	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2Q210	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
A2Q310	151-0462-00			TRANSISTOR:SILICON,PNP	80009	151-0462-00
A2R103	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A2R110	321-0830-03			RES.,FXD,FILM:2.41K OHM,0.25%,0.125W	91637	MFF1816D24100C
A2R111	321-1296-03			RES.,FXD,FILM:12K OHM,0.25%,0.125W	91637	MFF1816D12001C
A2R112	321-1097-03			RES.,FXD,FILM:101 OHM,0.25%,0.125W	91637	MFF1816D101R0C
A2R113	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A2R200	311-1375-00			RES.,VAR,NONWIR:PNL,10K OHM,1W	01121	73M1G040L103M
A2R204	311-1563-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	73138	91-85-0
A2R209	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R210	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R211	321-1602-04			RES.,FXD,FILM:29.27K OHM,0.1%,0.125W	91637	MFF1816D29271B
A2R212	321-1655-03			RES.,FXD,FILM:32K OHM,0.25%,0.125W	91637	MFF1816D32001C
A2R213	321-0924-02			RES.,FXD,FILM:40K OHM,0.5%,0.125W	24546	NC55C4002D
A2R300	311-2045-00			RES.,VAR,NONWIR:PNL,50K OHM,20%,0.5W	01121	19M250
A2R400	311-2042-00			RES.,VAR,NONWIR:PNL,2X20K OHM,20%,0.5W	01121	19M251
A2S300	311-2045-00			RES.,VAR,NONWIR:PNL,50K OHM,20%,0.5W	01121	19M250
A2S400	311-2042-00			RES.,VAR,NONWIR:PNL,2X20K OHM,20%,0.5W	01121	19M251

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3	----- -----			CKT BOARD ASSY:XYZ AMPLIFIER		
A3C100	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C110	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A3C112	283-0178-00			CAP.,FXD,CER DI:0.1UF,+80-20%,100V	72982	8131N145651 104Z
A3C120	283-0178-00			CAP.,FXD,CER DI:0.1UF,+80-20%,100V	72982	8131N145651 104Z
A3C132	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A3C200	281-0178-00			CAP.,VAR,PLSTC:1-3.5PF,500V	80031	2805D013R5BH02F0
A3C201	281-0529-00			CAP.,FXD,CER DI:1.5PF,+/-0.25PF,500V	72982	301-000C0K0159C
A3C206	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C210	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A3C211	281-0529-00			CAP.,FXD,CER DI:1.5PF,+/-0.25PF,500V	72982	301-000C0K0159C
A3C214	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C221	281-0529-00			CAP.,FXD,CER DI:1.5PF,+/-0.25PF,500V	72982	301-000C0K0159C
A3C222	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C223	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C224	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C230	281-0178-00			CAP.,VAR,PLSTC:1-3.5PF,500V	80031	2805D013R5BH02F0
A3C232	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A3C233	281-0529-00			CAP.,FXD,CER DI:1.5PF,+/-0.25PF,500V	72982	301-000C0K0159C
A3C234	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A3C303	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C313	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C314	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C315	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C322	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C334	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C336	281-0205-00			CAP.,VAR,PLSTC:4-65PF,100V	80031	2810C5R565QJ02F0
A3C413	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C414	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C418	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C422	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C430	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C438	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	72982	8035D9AADC0G270M
A3C439	281-0205-00			CAP.,VAR,PLSTC:4-65PF,100V	80031	2810C5R565QJ02F0
A3C510	281-0792-00			CAP.,FXD,CER DI:82PF,10%,100V	72982	8035D2AADC0G820K
A3C511	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A3C520	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C536	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A3C605	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C610	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C611	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C612	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C613	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C624	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C625	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C701	283-0110-00			CAP.,FXD,CER DI:0.005UF,+80-20%,150V	56289	19C242B
A3C703	290-0758-00			CAP.,FXD,ELCTLT:2.2UF,+50-10%,160V	56289	502D227
A3C714	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C715	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C724	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C800	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C801	290-0758-00			CAP.,FXD,ELCTLT:2.2UF,+50-10%,160V	56289	502D227
A3C805	283-0178-00			CAP.,FXD,CER DI:0.1UF,+80-20%,100V	72982	8131N145651 104Z
A3C815	281-0760-00			CAP.,FXD,CER DI:22PF,10%,500V	72982	0314021 C0G0220K
A3C820	285-1067-00			CAP.,FXD,PLSTC:0.5UF,1%,200V	14752	230B1C504F
A3C821	281-0760-00			CAP.,FXD,CER DI:22PF,10%,500V	72982	0314021 C0G0220K
A3C822	285-1067-00			CAP.,FXD,PLSTC:0.5UF,1%,200V	14752	230B1C504F

A3 XYZ AMPLIFIER (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3C830	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A3C832	290-0134-00			CAP.,FXD,ELCTLT:22UF,20%,15V	56289	150D226X0015B2
A3C902	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A3C903	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C930	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A3C934	285-1075-00			CAP.,FXD,PLSTC:0.1UF,5%,100V	14752	230B1B104J
A3CR200	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A3CR201	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A3CR223	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR313	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR314	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR423	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR510	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR511	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR522	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR523	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR524	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR530	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR600	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR601	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR605	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A3CR606	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A3CR620	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR700	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A3CR701	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR704	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A3CR801	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A3CR910	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR930	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	03508	DE140
A3K910	148-0076-00			RELAY,REED:1 FORM A,5V,0.25A,100V	95348	F81-1447
A3L100	108-0736-00			COIL,RF:810NH	80009	108-0736-00
A3L110	108-0736-00			COIL,RF:810NH	80009	108-0736-00
A3L123	108-0736-00			COIL,RF:810NH	80009	108-0736-00
A3L130	108-0736-00			COIL,RF:810NH	80009	108-0736-00
A3L206	108-0271-00			COIL,RF:0.025UH	80009	108-0271-00
A3L222	108-0408-00			COIL,RF:100NH	80009	108-0408-00
A3Q100	151-0407-00			TRANSISTOR:SILICON,NPN	04713	SS2456
A3Q110	151-0350-00			TRANSISTOR:SILICON,PNP	04713	SPS6700
A3Q120	151-0350-00			TRANSISTOR:SILICON,PNP	04713	SPS6700
A3Q130	151-0407-00			TRANSISTOR:SILICON,NPN	04713	SS2456
A3Q225	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q300	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q306	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q316	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q335	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q500	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q501	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q502	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q503	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q510	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q522	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q600	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q603	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q610	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q700	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q701	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q702	151-0406-00			TRANSISTOR:SILICON,PNP	01295	SGC7282

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A3 XYZ AMPLIFIER (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3Q703	151-0407-00			TRANSISTOR:SILICON,NPN	04713	SS2456
A3Q810	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q930	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3R100	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A3R105	322-0331-00			RES.,FXD,FILM:27.4K OHM,1%,0.25W	01121	OBD
A3R110	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A3R112	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A3R113	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A3R114	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A3R115	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A3R116	315-0623-00			RES.,FXD,CMPSN:62K OHM,5%,0.25W	01121	CB6235
A3R120	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A3R121	303-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,1W	01121	GB3625
A3R123	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A3R124	323-0272-00			RES.,FXD,FILM:6.65K OHM,1%,0.50W	75042	CECTO-6651F
A3R125	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A3R126	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A3R127	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A3R130	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A3R131	323-0272-00			RES.,FXD,FILM:6.65K OHM,1%,0.50W	75042	CECTO-6651F
A3R133	303-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,1W	01121	GB3625
A3R201	323-0272-00			RES.,FXD,FILM:6.65K OHM,1%,0.50W	75042	CECTO-6651F
A3R202	317-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.125W	01121	BB1025
A3R203	323-0272-00			RES.,FXD,FILM:6.65K OHM,1%,0.50W	75042	CECTO-6651F
A3R204	317-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.125W	01121	BB1025
A3R205	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A3R206	303-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,1W	01121	GB3625
A3R210	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R212	303-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,1W	01121	GB3625
A3R213	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R214	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A3R215	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A3R216	315-0912-00			RES.,FXD,CMPSN:9.1K OHM,5%,0.25W	01121	CB9125
A3R217	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R220	311-1558-00			RES.,VAR,NONWIR:20K OHM,20%,0.50W	73138	91-80-0
A3R221	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A3R222	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A3R223	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3R224	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A3R225	311-1565-00			RES.,VAR,NONWIR:250 OHM,20%,0.50W	73138	91-87-0
A3R230	317-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.125W	01121	BB1025
A3R231	317-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.125W	01121	BB1025
A3R232	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R234	317-0394-00			RES.,FXD,CMPSN:390K OHM,5%,0.125W	01121	BB3945
A3R235	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R236	315-0623-00			RES.,FXD,CMPSN:62K OHM,5%,0.25W	01121	CB6235
A3R300	321-0150-00			RES.,FXD,FILM:357 OHM,1%,0.125W	91637	MFF1816G357R0F
A3R301	321-0260-00			RES.,FXD,FILM:4.99K OHM,1%,0.125W	91637	MFF1816G49900F
A3R302	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A3R303	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A3R304	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R305	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A3R307	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R308	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A3R309	311-0622-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3326H-G48-101
A3R310	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A3R312	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515

A3 XYZ AMPLIFIER (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3R313	311-1564-00			RES.,VAR,NONWIR:TRMR,500 OHM,0.5W	73138	91-86-0
A3R314	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A3R315	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
A3R316	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A3R317	311-1565-00			RES.,VAR,NONWIR:250 OHM,20%,0.50W	73138	91-87-0
A3R318	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A3R319	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R320	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
A3R321	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A3R322	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R323	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A3R324	322-0249-00			RES.,FXD,FILM:3.83K OHM,1%,0.25W	75042	CEBT0-3831F
A3R325	322-0249-00			RES.,FXD,FILM:3.83K OHM,1%,0.25W	75042	CEBT0-3831F
A3R326	311-1564-00			RES.,VAR,NONWIR:TRMR,500 OHM,0.5W	73138	91-86-0
A3R329	315-0912-00			RES.,FXD,CMPSN:9.1K OHM,5%,0.25W	01121	CB9125
A3R330	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A3R333	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A3R334	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R335	321-0150-00			RES.,FXD,FILM:357 OHM,1%,0.125W	91637	MFF1816G357R0F
A3R336	311-0605-01			RES.,VAR,NONWIR:200 OHM,10%,0.50W	73138	82P-3-0-201
A3R337	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A3R400	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A3R401	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A3R402	321-0088-00			RES.,FXD,FILM:80.6 OHM,1%,0.125W	91637	MFF1816G80R60F
A3R403	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A3R404	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A3R406	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A3R407	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R408	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R409	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R410	321-0227-00			RES.,FXD,FILM:2.26K OHM,1%,0.125W	91637	MFF1816G22600F
A3R411	321-0227-00			RES.,FXD,FILM:2.26K OHM,1%,0.125W	91637	MFF1816G22600F
A3R412	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A3R413	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A3R414	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R415	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R416	321-0115-00			RES.,FXD,FILM:154 OHM,1%,0.125W	91637	MFF1816G154R0F
A3R417	311-1567-00			RES.,VAR,NONWIR:TRMR,100 OHM,0.50W	73138	91-89-0
A3R418	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A3R420	311-1567-00			RES.,VAR,NONWIR:TRMR,100 OHM,0.50W	73138	91-89-0
A3R421	321-0103-00			RES.,FXD,FILM:115 OHM,1%,0.125W	91637	MFF1816G115R0F
A3R422	315-0912-00			RES.,FXD,CMPSN:9.1K OHM,5%,0.25W	01121	CB9125
A3R424	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A3R425	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A3R426	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A3R427	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3R432	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A3R433	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A3R434	321-0116-00			RES.,FXD,FILM:158 OHM,1%,0.125W	91637	MFF1816G158R0F
A3R435	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A3R436	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A3R437	311-0613-00			RES.,VAR,NONWIR:100K OHM,10%,0.50W	73138	82-27-0
A3R438	311-0635-00			RES.,VAR,NONWIR:1K OHM,10%,0.50W	73138	82-32-0
A3R439	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R500	321-0325-00			RES.,FXD,FILM:23.7K OHM,1%,0.125W	91637	MFF1816G23701F
A3R501	321-0180-00			RES.,FXD,FILM:732 OHM,1%,0.125W	91637	MFF1816G732R0F
A3R502	321-0325-00			RES.,FXD,FILM:23.7K OHM,1%,0.125W	91637	MFF1816G23701F

A3 XYZ AMPLIFIER (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3R504	321-0164-00			RES.,FXD,FILM:499 OHM,1%,0.125W	91637	MFF1816G499R0F
A3R505	321-0164-00			RES.,FXD,FILM:499 OHM,1%,0.125W	91637	MFF1816G499R0F
A3R510	315-0430-00			RES.,FXD,CMPSN:43 OHM,5%,0.25W	01121	CB4305
A3R512	321-0176-00			RES.,FXD,FILM:665 OHM,1%,0.125W	91637	MFF1816G665R0F
A3R513	321-0176-00			RES.,FXD,FILM:665 OHM,1%,0.125W	91637	MFF1816G665R0F
A3R514	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A3R515	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R516	311-1564-00			RES.,VAR,NONWIR:TRMR,500 OHM,0.5W	73138	91-86-0
A3R517	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A3R520	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A3R521	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A3R522	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A3R523	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A3R524	321-0172-00			RES.,FXD,FILM:604 OHM,1%,0.125W	91637	MFF1816G604R0F
A3R526	321-0225-00			RES.,FXD,FILM:2.15K OHM,1%,0.125W	91637	MFF1816G21500F
A3R527	321-0225-00			RES.,FXD,FILM:2.15K OHM,1%,0.125W	91637	MFF1816G21500F
A3R528	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R529	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R530	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R531	307-0364-00			RES.,THERMAL:50 OHM,5%,0.125W	15454	DG125500J
A3R532	321-0142-00			RES.,FXD,FILM:294 OHM,1%,0.125W	91637	MFF1816G294R0F
A3R534	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A3R535	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A3R536	321-0108-00			RES.,FXD,FILM:130 OHM,1%,0.125W	91637	MFF1816G130R0F
A3R537	321-0108-00			RES.,FXD,FILM:130 OHM,1%,0.125W	91637	MFF1816G130R0F
A3R538	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R600	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A3R601	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R602	321-0329-00			RES.,FXD,FILM:26.1K OHM,1%,0.125W	91637	MFF1816G26101F
A3R603	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A3R604	321-0223-00			RES.,FXD,FILM:2.05K OHM,1%,0.125W	91637	MFF1816G20500F
A3R605	321-0272-00			RES.,FXD,FILM:6.65K OHM,1%,0.125W	91637	MFF1816G66500F
A3R606	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A3R610	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A3R611	321-0378-00			RES.,FXD,FILM:84.5K OHM,1%,0.125W	91637	MFF1816G84501F
A3R620	321-0356-00			RES.,FXD,FILM:49.9K OHM,1%,0.125W	91637	MFF1816G49901F
A3R621	321-0356-00			RES.,FXD,FILM:49.9K OHM,1%,0.125W	91637	MFF1816G49901F
A3R622	321-0356-00			RES.,FXD,FILM:49.9K OHM,1%,0.125W	91637	MFF1816G49901F
A3R623	321-0356-00			RES.,FXD,FILM:49.9K OHM,1%,0.125W	91637	MFF1816G49901F
A3R624	321-0189-00			RES.,FXD,FILM:909 OHM,1%,0.125W	91637	MFF1816G909R0F
A3R630	311-1566-00			RES.,VAR,NONWIR:200 OHM,20%,0.50W	73138	91-88-0
A3R700	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A3R701	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A3R702	321-0280-00			RES.,FXD,FILM:8.06K OHM,1%,0.125W	91637	MFF1816G80600F
A3R705	322-0331-00			RES.,FXD,FILM:27.4K OHM,1%,0.25W	01121	OBD
A3R706	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3R710	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A3R711	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A3R715	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A3R716	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A3R720	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A3R721	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A3R722	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A3R723	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A3R800	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A3R801	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A3R803	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	01121	CB3335

A3 XYZ AMPLIFIER (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3R804	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A3R809	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A3R810	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R811	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A3R812	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A3R813	321-0235-00			RES.,FXD,FILM:2.74K OHM,1%,0.125W	91637	MFF1816G27400F
A3R814	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A3R815	321-1449-00			RES.,FXD,FILM:470K OHM,1%,0.125W	91637	MFF1816G47002F
A3R816	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A3R820	321-0235-00			RES.,FXD,FILM:2.74K OHM,1%,0.125W	91637	MFF1816G27400F
A3R821	321-1449-00			RES.,FXD,FILM:470K OHM,1%,0.125W	91637	MFF1816G47002F
A3R822	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A3R823	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A3R830	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	01121	CB3335
A3R833	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A3R900	311-1552-00			RES.,VAR,NONWIR:500K OHM,20%,0.50W	73138	91-74-0
A3R901	311-1552-00			RES.,VAR,NONWIR:500K OHM,20%,0.50W	73138	91-74-0
A3R902	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A3R910	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R911	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A3R912	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3R913	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3R920	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	01121	CB3635
A3R921	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A3R922	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	01121	CB3635
A3R923	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A3R930	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A3R931	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R932	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	01121	CB3335
A3R933	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A3R934	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A3U200	155-0207-00			MICROCIRCUIT,LI:HORIZONTAL AMPLIFIER	80009	155-0207-00
A3U230	155-0207-00			MICROCIRCUIT,LI:HORIZONTAL AMPLIFIER	80009	155-0207-00
A3U330	155-0022-00			MICROCIRCUIT,DI:ML,CHANNEL SWITCH	80009	155-0022-00
A3U400	155-0022-00			MICROCIRCUIT,DI:ML,CHANNEL SWITCH	80009	155-0022-00
A3U610	156-0158-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	MC1458V
A3U810	156-0644-03			MICROCIRCUIT,DI:QUAD BILATERAL SWITCH	80009	156-0644-03
A3U811	156-0158-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	MC1458V
A3U820	156-0158-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	MC1458V
A3U830	156-0402-00			MICROCIRCUIT,LI:TIMER	27014	SL34829
A3U930	156-0402-00			MICROCIRCUIT,LI:TIMER	27014	SL34829
A3VR210	152-0405-00			SEMICOND DEVICE:ZENER,1W,15V,5%	80009	152-0405-00
A3VR232	152-0405-00			SEMICOND DEVICE:ZENER,1W,15V,5%	80009	152-0405-00
A3VR431	152-0227-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ13903
A3VR730	152-0481-00			SEMICOND DEVICE:ZENER,1W,5.1V,5%	80009	152-0481-00
A3VR731	152-0481-00			SEMICOND DEVICE:ZENER,1W,5.1V,5%	80009	152-0481-00
A3VR732	152-0481-00			SEMICOND DEVICE:ZENER,1W,5.1V,5%	80009	152-0481-00
A3VR733	152-0481-00			SEMICOND DEVICE:ZENER,1W,5.1V,5%	80009	152-0481-00
A3VR902	152-0147-00			SEMICOND DEVICE:ZENER,0.4W,27V,5%	04713	SZ50622RL
A3VR920	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738
A3VR921	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738
A3VR922	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738
A3VR923	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738
A3W610	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A4	----- -----			CKT BOARD ASSY:HI VOLTAGE		
A4C110	283-0261-00			CAP.,FXD,CER DI:0.01UF,20%,4000V	56289	575C1A1
A4C120	283-0082-00			CAP.,FXD,CER DI:0.01UF,+80-20%,4000V	56289	112C29
A4C121	281-0638-00			CAP.,FXD,CER DI:240PF,5%,500V	72982	301000Z5D241J
A4C122	283-0034-00			CAP.,FXD,CER DI:0.005UF,20%,4000V	56289	41C107A
A4C130	290-0798-00			CAP.,FXD,ELCTLT:180UF,+100-10%,40V	56289	672D187H040DM5C
A4C210	281-0513-00			CAP.,FXD,CER DI:27PF,+/-5.4PF,500V	72982	301-000P2G0270M
A4C211	281-0513-00			CAP.,FXD,CER DI:27PF,+/-5.4PF,500V	72982	301-000P2G0270M
A4C220	283-0221-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N087X7R0474M
A4C300	290-0164-00			CAP.,FXD,ELCTLT:1UF,+50-10%,150V	56289	500D105F150BA7
A4C301	283-0341-00			CAP.,FXD,CER DI:0.047UF,10%,100V	72982	8121N153X7R0473K
A4C310	290-0768-00			CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A4C311	290-0766-00			CAP.,FXD,ELCTLT:2.2UF,+50-10%,160V	56289	502D232
A4C312	283-0188-00			CAP.,FXD,CER DI:0.001UF,20%,6000V	72982	8486KVX5T0102M
A4C410	283-0188-00			CAP.,FXD,CER DI:0.001UF,20%,6000V	72982	8486KVX5T0102M
A4CR100	152-0586-00			SEMICOND DEVICE:SILICON,600V,500MA	14936	RGP10J
A4CR120	152-0409-00			SEMICOND DEVICE:SILICON,12,000V,5MA	80009	152-0409-00
A4CR200	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A4CR201	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A4CR210	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A4CR220	152-0495-00			SEMICOND DEVICE:V MULTR,6KV IN,12KV OUT	80009	152-0495-00
A4CR300	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A4CR400	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A4DS100	150-0030-00			LAMP,GLOW:NEON,T-2,60 TO 90 VOLTS	08806	A2B-T
A4DS101	150-0030-00			LAMP,GLOW:NEON,T-2,60 TO 90 VOLTS	08806	A2B-T
A4DS110	150-0030-00			LAMP,GLOW:NEON,T-2,60 TO 90 VOLTS	08806	A2B-T
A4DS120	150-0030-00			LAMP,GLOW:NEON,T-2,60 TO 90 VOLTS	08806	A2B-T
A4DS511	150-0030-00			LAMP,GLOW:NEON,T-2,60 TO 90 VOLTS	08806	A2B-T
A4L222	108-0422-00			COIL,RF:FIXED,82UH	80009	108-0422-00
A4Q60	151-0140-00			TRANSISTOR:SILICON,NPN	80009	151-0140-00
A4Q62	151-0140-00			TRANSISTOR:SILICON,NPN	80009	151-0140-00
A4Q300	151-0126-00			TRANSISTOR:SILICON,NPN	04713	ST1046
A4Q400	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A4Q401	151-0136-00			TRANSISTOR:SILICON,NPN	02735	35495
A4R100	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A4R101	315-0392-03			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A4R110	315-0470-03			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A4R120	315-0472-03			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A4R121	315-0134-03			RES.,FXD,CMPSN:130K OHM,5%,0.25W,AB ONLY	01121	CB1345
A4R130	315-0161-02			RES.,FXD,CMPSN:160 OHM,5%,0.25W	01121	CB1615
A4R200	315-0103-03			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R201	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A4R202	315-0364-00			RES.,FXD,CMPSN:360K OHM,5%,0.25W	01121	CB3645
A4R210	315-0754-00			RES.,FXD,CMPSN:750K OHM,5%,0.25W	01121	CB7545
A4R211	315-0754-00			RES.,FXD,CMPSN:750K OHM,5%,0.25W	01121	CB7545
A4R212	315-0103-03			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R213	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A4R220	307-0290-09			RES.,FXD,FILM:250K OHM	80009	307-0290-09
A4R300	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A4R301	315-0470-03			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A4R302	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
A4R310	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A4R400	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A4R401	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A4R402	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A4R404	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A4R405	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025

A4 HI VOLTAGE (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A4R410	315-0103-03			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R411	311-1232-00			RES.,VAR,NONWIR:50K OHM,20%,0.50W	32997	3386F-T04-503
A4R420	311-1256-00			RES.,VAR,NONWIR:2.5M OHM,20%,0.50W	73138	72-78-0
A4R430	301-0435-00			RES.,FXD,CMPSN:4.3M OHM,5%,0.50W	01121	EB4355
A4T120	120-1087-00			XFMR,PWR,SDN&SU:HIGH VOLTAGE	80009	120-1087-00
A4VR100	152-0357-00			SEMICOND DEVICE:ZENER,0.4W,82V,5%	04713	SZ12461KRL
A4VR101	152-0287-00			SEMICOND DEVICE:ZENER,0.4W,110V,5%	04713	1N986B
A4VR210	152-0168-00			SEMICOND DEVICE:ZENER,0.4W,12V,5%	04713	SZG35009K4
A4W100	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A4W200	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A5	----- -----			CKT BOARD ASSY:FOCUS D.C.RESTORER		
A5C111	283-0402-00			CAP.,FXD,CER,DI:0.001UF,+80-20%,4000V	72982	3904BF200Z5U102Z
A5C112	283-0402-00			CAP.,FXD,CER,DI:0.001UF,+80-20%,4000V	72982	3904BF200Z5U102Z
A5CR110	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A5CR111	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A4CR112	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A5R111	315-0103-03			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R112	315-0206-01			RES.,FXD,CMPSN:20M OHM,5%,0.25W	01121	CB2065
A5R113	315-0243-03			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A5R114	315-0103-03			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A6	----- -----			CKT BOARD ASSY:Z AXIS D.C.RESTORER		
A6C100	283-0402-00			CAP.,FXD,CER,DI:0.001UF,+80-20%,4000V	72982	3904BF200Z5U102Z
A6C101	283-0402-00			CAP.,FXD,CER,DI:0.001UF,+80-20%,4000V	72982	3904BF200Z5U102Z
A6C102	283-0402-00			CAP.,FXD,CER,DI:0.001UF,+80-20%,4000V	72982	3904BF200Z5U102Z
A6CR101	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A6CR102	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A6CR103	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A6R102	315-0824-02			RES.,FXD,CMPSN:820K OHM,5%,0.25W	01121	CB8245
A6R103	315-0206-01			RES.,FXD,CMPSN:20M OHM,5%,0.25W	01121	CB2065
A6R104	315-0243-03			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A6R105	315-0103-03			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A7	----- -----			CKT BOARD ASSY:POWER SUPPLY		
A7C110	283-0008-00			CAP.,FXD,CER DI:0.1UF,20%,500V	56289	275C8
A7C140	285-0808-00			CAP.,FXD,PLSTC:0.1UF,10%,50V	56289	LP66A1A104K004
A7C210	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A7C220	290-0509-00			CAP.,FXD,ELCTLT:3000UF,+100-10%,50V	56289	68D10454
A7C301	290-0509-00			CAP.,FXD,ELCTLT:3000UF,+100-10%,50V	56289	68D10454
A7C320	281-0788-00			CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K
A7C340	290-0506-00			CAP.,FXD,ELCTLT:9600UF,+100-10%,25V	56289	68D10471
A7C410	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A7C430	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	72982	8035D9AADC0G150K
A7C431	290-0517-00			CAP.,FXD,ELCTLT:6.8UF,20%,35V	56289	196D685X0035KA1
A7C503	290-0702-00			CAP.,FXD,ELCTLT:2000UF,+100-0%,50V	56289	68D10715
A7C520	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A7C530	290-0779-00			CAP.,FXD,ELCTLT:10UF,+50-10%,50VDC	56289	502D237
A7C710	290-0506-00			CAP.,FXD,ELCTLT:9600UF,+100-10%,25V	56289	68D10471
A7C720	290-0779-00			CAP.,FXD,ELCTLT:10UF,+50-10%,50VDC	56289	502D237
A7C740	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A7C810	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A7C811	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	72982	8035D9AADC1G470K
A7C820	290-0779-00			CAP.,FXD,ELCTLT:10UF,+50-10%,50VDC	56289	502D237
A7C840	290-0269-00			CAP.,FXD,ELCTLT:0.22UF,5%,35V	56289	162D224X5035BC2
A7C841	290-0282-00			CAP.,FXD,ELCTLT:0.047UF,10%,35V	56289	162D473X9035BC2
A7C850	290-0177-00			CAP.,FXD,ELCTLT:1UF,20%,50V	56289	162D105X0050CD2
A7C950	290-0282-00			CAP.,FXD,ELCTLT:0.047UF,10%,35V	56289	162D473X9035BC2
A7C951	290-0177-00			CAP.,FXD,ELCTLT:1UF,20%,50V	56289	162D105X0050CD2
A7C1000	290-0506-00			CAP.,FXD,ELCTLT:9600UF,+100-10%,25V	56289	68D10471
A7C1010	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A7C1060	290-0177-00			CAP.,FXD,ELCTLT:1UF,20%,50V	56289	162D105X0050CD2
A7C1100	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	72982	8035D9AADC1G470K
A7C1110	290-0779-00			CAP.,FXD,ELCTLT:10UF,+50-10%,50VDC	56289	502D237
A7C1111	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	72982	8035D9AADC0G150K
A7C1130	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	502D230
A7C1140	290-0177-00			CAP.,FXD,ELCTLT:1UF,20%,50V	56289	162D105X0050CD2
A7C1150	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A7C1220	290-0468-00			CAP.,FXD,ELCTLT:250UF,+75-10%,150V	56289	68D10470
A7C1230	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	502D230
A7C1240	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A7C1250	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A7C1251	281-0788-00			CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K
A7C1310	290-0670-00			CAP.,FXD,ELCTLT:550UF,+75-10%,100V	56289	68D10512
A7C1330	290-0767-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,160V	56289	502D228
A7CR110	152-0462-00			SEMICOND DEVICE:RECT,SI,200V,2.5A	04713	SDA10228
A7CR140	152-0668-00			SEMICOND DEVICE:RECT BRIDGE,SI,200V,6A	80009	152-0668-00
A7CR210	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR430	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR510	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR511	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A7CR520	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR530	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR560	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A7CR610	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A7CR650	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
A7CR710	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A7CR720	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A7CR740	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR800	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR801	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R

A7 POWER SUPPLY (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A7CR810	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR841	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR860	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR900	152-0668-00			SEMICOND DEVICE:RECT BRIDGE,SI,200V,6A	80009	152-0668-00
A7CR910	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A7CR950	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR951	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR952	152-0141-02	XB010131		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR1000	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR1001	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR1012	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR1050	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR1100	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR1101	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A7CR1110	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A7CR1111	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR1120	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A7CR1150	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR1151	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR1210	152-0585-00			SEMICOND DEVICE:SILICON,BRIDGE,200V,1A	80009	152-0585-00
A7CR1220	152-0585-00			SEMICOND DEVICE:SILICON,BRIDGE,200V,1A	80009	152-0585-00
A7CR1250	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7CR1300	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A7CR1340	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A7F340	159-0011-00			FUSE,CARTRIDGE:3AG,6.25A,125V,5SEC	75915	3136.25
A7F620	159-0025-00			FUSE,CARTRIDGE:3AG,0.5A,250V,FAST-BLOW	71400	AGC 1/2
A7F950	159-0024-00			FUSE,CARTRIDGE:3AG,0.062A,250V,0.3 SEC	71400	AGC 1/16
A7L350	108-1009-00			COIL,RF:FIXED,371MH	80009	108-1009-00
A7L650	108-1005-00			COIL,RF:FIXED,1.7MH	80009	108-1005-00
A7L651	108-1008-00			COIL,RF:FIXED,850MH	80009	108-1008-00
A7L830	108-1007-00			COIL,RF:FIXED,5.6MH	80009	108-1007-00
A7L1040	108-1006-00			COIL,RF:FIXED,28.8MH	80009	108-1006-00
A7L1140	108-1006-00			COIL,RF:FIXED,28.8MH	80009	108-1006-00
A7Q121	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A7Q230	151-0432-00			TRANSISTOR:SILICON,NPN	80009	151-0432-00
A7Q231	151-0432-00			TRANSISTOR:SILICON,NPN	80009	151-0432-00
A7Q300	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A7Q320	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A7Q400	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A7Q410	151-0432-00			TRANSISTOR:SILICON,NPN	80009	151-0432-00
A7Q411	151-0432-00			TRANSISTOR:SILICON,NPN	80009	151-0432-00
A7Q420	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A7Q421	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A7Q501	151-0208-02			TRANSISTOR:SILICON,PNP	80009	151-0208-02
A7Q510	151-0432-00			TRANSISTOR:SILICON,NPN	80009	151-0432-00
A7Q610	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A7Q710	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A7Q810	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A7Q811	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A7Q910	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A7Q960	151-0260-00			TRANSISTOR:SILICON,NPN	80009	151-0260-00
A7Q1000	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A7Q1001	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A7Q1020	151-0347-00			TRANSISTOR:SILICON,NPN	56289	2N5551
A7Q1050	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A7Q1100	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A7Q1120	151-0347-00			TRANSISTOR:SILICON,NPN	56289	2N5551

A7 POWER SUPPLY (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A7Q1210	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A7Q1220	151-0350-00			TRANSISTOR:SILICON,PNP	04713	SPS6700
A7Q1341	151-0503-00			SCR:SILICON,TO-92	04713	SCR5138
A7Q1350	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A7R120	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A7R200	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A7R201	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A7R221	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A7R222	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A7R223	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A7R224	308-0685-00			RES.,FXD,WW:1.5 OHM,5%,1W	75042	BW20-1R500J
A7R225	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A7R226	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A7R230	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A7R300	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A7R301	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A7R302	308-0767-00			RES.,FXD,WW:1.1 OHM,5%,1W	75042	BW20-1R100J
A7R310	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A7R311	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A7R320	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A7R321	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A7R330	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A7R340	308-0555-00			RES.,FXD,WW:5 OHM,5%,3W	00213	1200S-5R000J
A7R400	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A7R410	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A7R411	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A7R420	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A7R421	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A7R422	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A7R430	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A7R500	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A7R501	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A7R510	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A7R511	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A7R512	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A7R513	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A7R514	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A7R520	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A7R521	311-1223-00			RES.,VAR,NONWIR:TRMR,250 OHM,0.5W	02111	63M251T602
A7R522	311-1224-00			RES.,VAR,NONWIR:500 OHM,20%,0.50W	32997	3386F-T04-501
A7R523	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	MFF1816G12400F
A7R524	321-0256-00			RES.,FXD,FILM:4.53K OHM,1%,0.125W	91637	MFF1816G45300F
A7R560	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A7R600	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A7R610	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A7R611	308-0793-00			RES.,FXD,WW:0.51 OHM,5%,0.50W	75042	BW20 .51 OHM 5%
A7R613	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A7R650	308-0680-00			RES.,FXD,WW:0.045 OHM,10%,3W	91637	RS2B-R0450K
A7R651	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A7R700	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A7R710	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A7R711	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A7R712	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A7R741	321-0042-00			RES.,FXD,FILM:26.7 OHM,1%,0.125W	91637	MFF1816G26R70F
A7R742	321-0042-00			RES.,FXD,FILM:26.7 OHM,1%,0.125W	91637	MFF1816G26R70F
A7R743	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A7R750	308-0680-00			RES.,FXD,WW:0.045 OHM,10%,3W	91637	RS2B-R0450K

A7 POWER SUPPLY (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A7R751	301-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.50W	01121	EB2005
A7R800	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A7R810	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A7R811	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A7R812	321-0603-00			RES.,FXD,FILM:15K OHM,0.25%,0.125W	91637	MFF1816D15001C
A7R813	321-0603-00			RES.,FXD,FILM:15K OHM,0.25%,0.125W	91637	MFF1816D15001C
A7R814	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A7R820	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A7R841	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A7R850	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	01121	CB2045
A7R851	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A7R852	301-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.50W	01121	EB2005
A7R853	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A7R900	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A7R910	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A7R912	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A7R913	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A7R940	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A7R950	321-0309-00			RES.,FXD,FILM:16.2K OHM,1%,0.125W	91637	MFF1816G16201F
A7R951	321-0390-00			RES.,FXD,FILM:113K OHM,1%,0.125W	91637	MFF1816G11302F
A7R952	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	01121	CB2045
A7R953	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A7R954	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A7R955	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A7R1000	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A7R1010	321-0603-00			RES.,FXD,FILM:15K OHM,0.25%,0.125W	91637	MFF1816D15001C
A7R1011	321-0603-00			RES.,FXD,FILM:15K OHM,0.25%,0.125W	91637	MFF1816D15001C
A7R1012	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A7R1013	321-0364-00			RES.,FXD,FILM:60.4K OHM,1%,0.125W	91637	MFF1816G60401F
A7R1014	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A7R1015	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A7R1020	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A7R1040	308-0710-00			RES.,FXD,WW:0.27 OHM,10%,1W	75042	BW20-R2700J
A7R1050	301-0150-00			RES.,FXD,CMPSN:15 OHM,5%,0.50W	01121	EB1505
A7R1051	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A7R1060	301-0150-00			RES.,FXD,CMPSN:15 OHM,5%,0.50W	01121	EB1505
A7R1061	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A7R1100	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A7R1101	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A7R1110	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A7R1111	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A7R1112	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A7R1120	321-0390-00			RES.,FXD,FILM:113K OHM,1%,0.125W	91637	MFF1816G11302F
A7R1121	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A7R1122	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A7R1140	308-0710-00			RES.,FXD,WW:0.27 OHM,10%,1W	75042	BW20-R2700J
A7R1150	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A7R1151	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A7R1152	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A7R1160	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A7R1161	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A7R1162	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A7R1163	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A7R1200	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A7R1201	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A7R1202	308-0793-00			RES.,FXD,WW:0.51 OHM,5%,0.50W	75042	BW20 .51 OHM 5%
A7R1203	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715

A7 POWER SUPPLY (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A7R1210	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A7R1211	307-0113-00			RES.,FXD,CMPSN:5.1 OHM,5%,0.25W	01121	CB51G5
A7R1241	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A7R1242	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A7R1250	321-0689-00			RES.,FXD,FILM:24.9K OHM,0.5%,0.125W	91637	MFF1816G24901D
A7R1251	321-0764-01			RES.,FXD,FILM:5.09K OHM,0.5%,0.125W	91637	MFF1816G50900D
A7R1252	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A7R1253	315-0474-00	XB010131		RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A7R1260	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
A7R1261	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A7R1320	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A7R1340	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A7R1341	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A7T540	108-0493-00			COIL,RF:625UH	80009	108-0493-00
A7U1050	156-0853-00	B010100	B010130	MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER,DUAL	27014	LM358N
A7U1050	156-1272-00	B010131		MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	NE5532-FE-IIB
A7U1250	156-1225-00			MICROCIRCUIT,LI:DUAL COMPARATOR,8 DIP	27014	LM393N
A7VR230	152-0243-00			SEMICOND DEVICE:ZENER,0.4W,15V,5%	14552	1N965B
A7VR400	152-0243-00			SEMICOND DEVICE:ZENER,0.4W,15V,5%	14552	1N965B
A7VR430	152-0227-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ13903
A7VR850	152-0306-00			SEMICOND DEVICE:ZENER,0.4W,9.1V,5%	14433	1N960B
A7VR951	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG35008

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A8	----- -----			CKT BOARD ASSY:DIGITIZER		
A8C130	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C140	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C150	283-0633-00			CAP.,FXD,MICA D:77PF,1%,100V	00853	D151E770F0
A8C160	281-0788-00			CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K
A8C162	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C163	290-0534-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1
A8C164	290-0512-00			CAP.,FXD,ELCTLT:22UF,20%,15V	56289	196D226X0015KA1
A8C210	290-0512-00			CAP.,FXD,ELCTLT:22UF,20%,15V	56289	196D226X0015KA1
A8C212	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	72982	8035D9AADC0G150K
A8C220	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A8C240	290-0534-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1
A8C260	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C331	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	72982	8035D9AADC0G150K
A8C332	290-0267-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	162D105X0035CD2
A8C340	290-0534-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1
A8C341	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A8C380	290-0512-00			CAP.,FXD,ELCTLT:22UF,20%,15V	56289	196D226X0015KA1
A8C382	290-0534-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1
A8C431	281-0811-00			CAP.,FXD,CER DI:10PF,10%,100V	72982	8035D2AADC1G100K
A8C433	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C460	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	72982	8035D2AADC0G680K
A8C461	283-0616-00			CAP.,FXD,MICA D:75PF,5%,500V	00853	D155E750J0
A8C484	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C486	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C510	290-0512-00			CAP.,FXD,ELCTLT:22UF,20%,15V	56289	196D226X0015KA1
A8C511	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C520	281-0811-00			CAP.,FXD,CER DI:10PF,10%,100V	72982	8035D2AADC1G100K
A8C530	290-0512-00			CAP.,FXD,ELCTLT:22UF,20%,15V	56289	196D226X0015KA1
A8C531	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C560	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	72982	8035D2AADC0G680K
A8C561	283-0616-00			CAP.,FXD,MICA D:75PF,5%,500V	00853	D155E750J0
A8C660	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	72982	8035D2AADC0G680K
A8C661	283-0616-00			CAP.,FXD,MICA D:75PF,5%,500V	00853	D155E750J0
A8C680	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C681	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C685	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C720	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A8C735	290-0512-00			CAP.,FXD,ELCTLT:22UF,20%,15V	56289	196D226X0015KA1
A8C738	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	72982	8035D9AADC0G150K
A8C742	290-0512-00			CAP.,FXD,ELCTLT:22UF,20%,15V	56289	196D226X0015KA1
A8C750	290-0534-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1
A8C760	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	72982	8035D2AADC0G680K
A8C761	283-0616-00			CAP.,FXD,MICA D:75PF,5%,500V	00853	D155E750J0
A8CR112	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR140	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A8CR150	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR151	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR152	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR213	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR260	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR261	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR331	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR360	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR361	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR430	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR470	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R

A8 DIGITIZER (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A8CR471	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR472	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A8CR501	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR502	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR503	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR504	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR505	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR506	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR507	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR508	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR509	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR510	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR540	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A8CR541	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A8CR570	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A8CR571	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR572	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR631	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR670	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR671	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR672	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A8CR700	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR716	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR770	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR771	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A8CR772	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A8L110	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A8L164	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A8L240	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A8L280	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A8L360	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A8L380	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A8L510	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A8L530	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A8Q110	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q140	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q141	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q142	151-0198-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS8802-1
A8Q143	151-0198-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS8802-1
A8Q150	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q181	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q210	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q330	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q331	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q360	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q361	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q362	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q363	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q370	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q371	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q372	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q373	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q430	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q450	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q451	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q460	151-1057-00			TRANSISTOR:SILICON,FE,N-CHANNEL,DUAL	80009	151-1057-00
A8Q470	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677

A8 DIGITIZER (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A8Q471	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q550	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q551	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q500	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q571	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q572	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q573	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q580	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A8Q670	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q671	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q672	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q673	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q674	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q675	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q720	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q721	151-0208-02			TRANSISTOR:SILICON,PNP	80009	151-0208-02
A8Q740	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q741	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q750	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q751	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q760	151-1057-00			TRANSISTOR:SILICON,FE,N-CHANNEL,DUAL	80009	151-1057-00
A8Q770	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q771	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A8Q772	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8Q773	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A8R110	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A8R111	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A8R112	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A8R113	315-0161-00			RES.,FXD,CMPSN:160 OHM,5%,0.25W	01121	CB1615
A8R114	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A8R130	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8R140	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R150	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A8R151	321-0230-00			RES.,FXD,FILM:2.43K OHM,1%,0.125W	91637	MFF1816G24300F
A8R152	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A8R153	321-0213-00			RES.,FXD,FILM:1.62K OHM,1%,0.125W	91637	MFF1816G16200F
A8R154	321-0142-00			RES.,FXD,FILM:294 OHM,1%,0.125W	91637	MFF1816G294R0F
A8R160	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A8R161	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8R162	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R163	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A8R170	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R180	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A8R181	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A8R182	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A8R183	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A8R210	307-0526-00			RES NTWK,THK FI:5,510 OHM,10%,0.125W	32997	4306R-101-511J
A8R211	307-0651-00			RES NTWK,FXD,FI:5,3.3K OHM,5%,0.150W	01121	206A332
A8R212	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R213	315-0910-00			RES.,FXD,CMPSN:91 OHM,5%,0.25W	01121	CB9105
A8R214	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A8R220	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8R221	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8R222	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8R223	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8R230	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8R240	321-0323-00			RES.,FXD,FILM:22.6K OHM,1%,0.125W	91637	MFF1816G22601F

A8 DIGITIZER (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A8R241	321-0294-00			RES.,FXD,FILM:11.3K OHM,1%,0.125W	91637	MFF1816G11301F
A8R242	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A8R243	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8R250	321-0192-00			RES.,FXD,FILM:976 OHM,1%,0.125W	91637	MFF1816G976R0F
A8R251	321-0192-00			RES.,FXD,FILM:976 OHM,1%,0.125W	91637	MFF1816G976R0F
A8R252	321-0175-00			RES.,FXD,FILM:649 OHM,1%,0.125W	91637	MFF1816G649R0F
A8R253	321-0187-00			RES.,FXD,FILM:866 OHM,1%,0.125W	91637	MFF1816G866R0F
A8R254	321-0175-00			RES.,FXD,FILM:649 OHM,1%,0.125W	91637	MFF1816G649R0F
A8R255	321-0187-00			RES.,FXD,FILM:866 OHM,1%,0.125W	91637	MFF1816G866R0F
A8R261	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A8R280	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8R281	315-0161-00			RES.,FXD,CMPSN:160 OHM,5%,0.25W	01121	CB1615
A8R300	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	01121	206A102
A8R320	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G
A8R330	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A8R331	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A8R332	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A8R334	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A8R335	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A8R340	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A8R341	321-0310-00			RES.,FXD,FILM:16.5K OHM,1%,0.125W	91637	MFF1816G16501F
A8R342	321-0302-00			RES.,FXD,FILM:13.7K OHM,1%,0.125W	91637	MFF1816G13701F
A8R350	311-1936-00			RES.,VAR,NONWIR:CKT BD,50 OHM,20%,0.5W	73138	MODEL 72X
A8R351	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A8R352	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A8R353	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A8R354	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A8R355	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A8R356	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
A8R361	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R362	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R370	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R371	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R382	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R430	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A8R431	321-0294-00			RES.,FXD,FILM:11.3K OHM,1%,0.125W	91637	MFF1816G11301F
A8R432	321-0323-00			RES.,FXD,FILM:22.6K OHM,1%,0.125W	91637	MFF1816G22601F
A8R433	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A8R440	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A8R442	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A8R442	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A8R443	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A8R450	307-0127-00			RES.,THERMAL:1K OHM,10%	50157	2D1596
A8R451	321-0109-00			RES.,FXD,FILM:133 OHM,1%,0.125W	91637	MFF1816G133R0F
A8R452	321-0224-00			RES.,FXD,FILM:2.1K OHM,1%,0.125W	91637	MFF1816G21000F
A8R453	321-0289-03			RES.,FXD,FILM:10K OHM,0.25%,0.125W	91637	MFF1816D10001C
A8R461	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R470	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R471	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R480	321-0278-00			RES.,FXD,FILM:7.68K OHM,1%,0.125W	91637	MFF1816G76800F
A8R481	321-0278-00			RES.,FXD,FILM:7.68K OHM,1%,0.125W	91637	MFF1816G76800F
A8R482	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A8R483	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A8R484	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R485	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A8R486	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R500	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G

A8 DIGITIZER (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A8R520	307-0541-00			RES,NTWK,THK FI:(7)1K OHM,10%,1W	91637	MSP08A01-102G
A8R530	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	01121	206A102
A8R531	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A8R532	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A8R540	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A8R541	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A8R550	321-0294-00			RES.,FXD,FILM:11.3K OHM,1%,0.125W	91637	MFF1816G11301F
A8R551	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A8R552	321-0196-00			RES.,FXD,FILM:1.07K OHM,1%,0.125W	91637	MFF1816G10700F
A8R554	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	MFF1816G549R0F
A8R555	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	MFF1816G549R0F
A8R560	311-1244-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3386X-T07-101
A8R561	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A8R562	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R571	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R572	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R581	321-0278-00			RES.,FXD,FILM:7.68K OHM,1%,0.125W	91637	MFF1816G76800F
A8R582	321-0278-00			RES.,FXD,FILM:7.68K OHM,1%,0.125W	91637	MFF1816G76800F
A8R583	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A8R610	307-0527-00			RES NTWK,FXD,FI:(5)39 OHM,20%,0.125W	01121	206A390
A8R620	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	MFF1816G549R0F
A8R621	321-1133-02			RES.,FXD,FILM:240 OHM,0.5%,0.125W	91637	MFF1816D240R0D
A8R622	321-1133-02			RES.,FXD,FILM:240 OHM,0.5%,0.125W	91637	MFF1816D240R0D
A8R623	321-1211-09			RES.,FXD,FILM:1.56K OHM,1%,0.125W	91637	MFF1816C15600F
A8R624	321-1211-09			RES.,FXD,FILM:1.56K OHM,1%,0.125W	91637	MFF1816C15600F
A8R625	321-0137-00			RES.,FXD,FILM:261 OHM,1%,0.125W	91637	MFF1816G261R0F
A8R626	321-0137-00			RES.,FXD,FILM:261 OHM,1%,0.125W	91637	MFF1816G261R0F
A8R630	321-0171-00			RES.,FXD,FILM:590 OHM,1%,0.125W	91637	MFF1816G590R0F
A8R631	321-0171-00			RES.,FXD,FILM:590 OHM,1%,0.125W	91637	MFF1816G590R0F
A8R632	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A8R633	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A8R634	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A8R650	321-0196-00			RES.,FXD,FILM:1.07K OHM,1%,0.125W	91637	MFF1816G10700F
A8R651	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	MFF1816G549R0F
A8R652	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	MFF1816G549R0F
A8R660	311-1244-00			RES.,VAR,NONWIR:100 OHM,10%,0.50W	32997	3386X-T07-101
A8R661	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R670	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R671	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R681	321-0278-00			RES.,FXD,FILM:7.68K OHM,1%,0.125W	91637	MFF1816G76800F
A8R682	321-0278-00			RES.,FXD,FILM:7.68K OHM,1%,0.125W	91637	MFF1816G76800F
A8R683	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A8R684	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A8R685	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R686	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A8R710	321-0289-03			RES.,FXD,FILM:10K OHM,0.25%,0.125W	91637	MFF1816D10001C
A8R711	321-0318-03			RES.,FXD,FILM:20K OHM,0.25%,0.125W	24546	NC55C2002C
A8R712	321-0347-00			RES.,FXD,FILM:40.2K OHM,1%,0.125W	91637	MFF1816G40201F
A8R713	321-0376-00			RES.,FXD,FILM:80.6K OHM,1%,0.125W	91637	MFF1816G80601F
A8R714	321-0381-00			RES.,FXD,FILM:90.9K OHM,1%,0.125W	91637	MFF1816G90901F
A8R715	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8R716	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R720	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A8R722	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A8R723	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A8R724	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A8R730	311-1248-00			RES.,VAR,NONWIR:500 OHM,10%,0.50W	73138	72X-23-0-501K

A8 DIGITIZER (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A8R731	321-0604-00			RES.,FXD,FILM:30K OHM,0.25%,0.125W	91637	MFF1816D30001C
A8R732	321-0256-00			RES.,FXD,FILM:4.53K OHM,1%,0.125W	91637	MFF1816G45300F
A8R733	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A8R734	321-0239-07			RES.,FXD,FILM:3.01K OHM,0.1%,0.125W	91637	MFF1816C30100B
A8R735	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A8R737	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A8R738	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A8R739	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A8R740	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A8R741	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A8R742	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A8R750	311-1936-00			RES.,VAR,NONWIR:CKT BD,50 OHM,20%,0.5W	73138	MODEL 72X
A8R751	321-0294-00			RES.,FXD,FILM:11.3K OHM,1%,0.125W	91637	MFF1816G11301F
A8R752	307-0127-00			RES.,THERMAL:1K OHM,10%	50157	2D1596
A8R753	321-0224-00			RES.,FXD,FILM:2.1K OHM,1%,0.125W	91637	MFF1816G21000F
A8R754	321-0109-00			RES.,FXD,FILM:133 OHM,1%,0.125W	91637	MFF1816G133R0F
A8R755	321-0294-00			RES.,FXD,FILM:11.3K OHM,1%,0.125W	91637	MFF1816G11301F
A8R761	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R770	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R771	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A8R781	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A8R782	321-0278-00			RES.,FXD,FILM:7.68K OHM,1%,0.125W	91637	MFF1816G76800F
A8R783	321-0278-00			RES.,FXD,FILM:7.68K OHM,1%,0.125W	91637	MFF1816G76800F
A8U130	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A8U170	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A8U180	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A8U220	156-0920-00			MICROCIRCUIT,DI:BIN TO 1-8 DECODER	80009	156-0920-00
A8U230	156-0788-01			MICROCIRCUIT,DI:SYN 4-BIT CNTR,W/SYN CLEAR	01295	SN74LS162
A8U270	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG FF	80009	156-0567-02
A8U280	156-0118-03			MICROCIRCUIT,DI:1 DUAL J-K FF,BURN-IN	80009	156-0118-03
A8U300	156-0458-00			MICROCIRCUIT,DI:QUAD AND GATE,2-INP	04713	MC10104L
A8U310	156-0458-00			MICROCIRCUIT,DI:QUAD AND GATE,2-INP	04713	MC10104L
A8U320	156-0458-00			MICROCIRCUIT,DI:QUAD AND GATE,2-INP	04713	MC10104L
A8U340	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	MLM358U
A8U400	156-0205-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	80009	156-0205-02
A8U410	156-0205-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	80009	156-0205-02
A8U420	156-0205-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	80009	156-0205-02
A8U460	156-0106-00			MICROCIRCUIT,LI:MONOLITHIC,6-DIODE ARRAY	54590	CA3039
A8U520	155-0167-01			MICROCIRCUIT,LI:4BIT D/A CONVERTER	80009	155-0167-01
A8U530	156-0362-00			MICROCIRCUIT,LI:ECL COMPARATOR	34335	AM685HL
A8U540	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A8U560	156-0106-00			MICROCIRCUIT,LI:MONOLITHIC,6-DIODE ARRAY	54590	CA3039
A8U600	156-0534-01			MICROCIRCUIT,LI:DUAL DIFF AMPL	80009	156-0534-01
A8U610	156-0534-01			MICROCIRCUIT,LI:DUAL DIFF AMPL	80009	156-0534-01
A8U640	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A8U660	156-0106-00			MICROCIRCUIT,LI:MONOLITHIC,6-DIODE ARRAY	54590	CA3039
A8U730	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	MLM358U
A8U760	156-0106-00			MICROCIRCUIT,LI:MONOLITHIC,6-DIODE ARRAY	54590	CA3039

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A9	----- -----			CKT BOARD ASSY:INTERFACE		
A9C130	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A9C131	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	72982	1035D2ADC0G569D
A9C140	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	72982	8035D2AADX5P151K
A9C160	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	72982	8035D9AADC0G270M
A9C250	290-0267-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	162D105X0035CD2
A9C251	290-0706-00			CAP.,FXD,ELCTLT:22UF,20%,50V	90201	TDC226M050WLD
A9C260	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	72982	8035D9AADC0G270M
A9C261	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A9C301	283-0618-00			CAP.,FXD,MICA D:130PF,2%,400V	00853	D155E131G0
A9C314	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	72982	8035D9AADC1G220K
A9C340	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A9C352	290-0267-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	162D105X0035CD2
A9C353	290-0267-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	162D105X0035CD2
A9C401	281-0765-00			CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710100X5P101J
A9C402	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	72982	8035D9AADC0G150K
A9C420	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A9C440	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	72982	1035D2ADC0G569D
A9C461	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A9C462	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	72982	8035D9AADC0G270M
A9C463	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	72982	8035D9AADC0G270M
A9C464	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	72982	8035D2AADX5P151K
A9C516	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	72982	8035D9AADC1G220K
A9C560	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A9C610	290-0135-00			CAP.,FXD,ELCTLT:15UF,20%,20V	56289	150D156X0020B2
A9C660	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A9C720	281-0768-00			CAP.,FXD,CER DI:470PF,20%,100V	72982	8035D9AADW5R471M
A9C750	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	72982	1035D2ADC0G569D
A9C800	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A9C820	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	72982	8035D2AADX5P151K
A9C830	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A9C860	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	72982	1035D2ADC0G569D
A9C861	290-0219-00			CAP.,FXD,ELCTLT:5UF,+75-10%,25V	56289	30D505G025BA9
A9C862	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A9C910	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A9CR140	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR141	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR160	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR231	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR261	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR360	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR450	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR451	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR452	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR530	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR531	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR550	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR560	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR633	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A9CR630	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A9CR655	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR800	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR820	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR840	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9CR960	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A9L732	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A9Q140	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677

A9 INTERFACE (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A9Q231	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q240	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q250	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A9Q251	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A9Q300	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q301	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q330	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q331	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q332	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q340	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q350	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q400	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q410	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q430	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q431	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q432	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q440	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q441	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A9Q442	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A9Q500	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q530	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q531	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q532	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q550	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q600	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A9Q640	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q641	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q720	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q730	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q731	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A9Q740	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q811	151-0195-00			TRANSISTOR:SILICON,NPN	80009	151-0195-00
A9Q810	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A9Q840	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9Q920	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A9Q960	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A9R110	321-0082-00			RES.,FXD,FILM:69.8 OHM,1%,0.125W	91637	MFF1816G69R80F
A9R111	321-0082-00			RES.,FXD,FILM:69.8 OHM,1%,0.125W	91637	MFF1816G69R80F
A9R120	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A9R130	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A9R131	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A9R132	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A9R133	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A9R134	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A9R140	315-0430-00			RES.,FXD,CMPSN:43 OHM,5%,0.25W	01121	CB4305
A9R141	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A9R142	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A9R160	315-0910-00			RES.,FXD,CMPSN:91 OHM,5%,0.25W	01121	CB9105
A9R161	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R210	322-0139-00			RES.,FXD,FILM:274 OHM,1%,0.25W	91637	MFF1421G274R0F
A9R211	322-0139-00			RES.,FXD,FILM:274 OHM,1%,0.25W	91637	MFF1421G274R0F
A9R220	323-0101-00			RES.,FXD,FILM:110 OHM,1%,0.50W	75042	CECT0-1100F
A9R230	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A9R240	321-0164-00			RES.,FXD,FILM:499 OHM,1%,0.125W	91637	MFF1816G499R0F
A9R241	321-0164-00			RES.,FXD,FILM:499 OHM,1%,0.125W	91637	MFF1816G499R0F
A9R242	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R243	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205

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A9 INTERFACE (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A9R260	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R261	315-0910-00			RES.,FXD,CMPSN:91 OHM,5%,0.25W	01121	CB9105
A9R301	321-0301-00			RES.,FXD,FILM:13.3K OHM,1%,0.125W	91637	MFF1816G13301F
A9R310	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A9R311	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A9R312	321-0236-00			RES.,FXD,FILM:2.8K OHM,1%,0.125W	91637	MFF1816G28000F
A9R313	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A9R315	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A9R320	321-0236-00			RES.,FXD,FILM:2.8K OHM,1%,0.125W	91637	MFF1816G28000F
A9R322	321-0325-00			RES.,FXD,FILM:23.7K OHM,1%,0.125W	91637	MFF1816G23701F
A9R323	321-0325-00			RES.,FXD,FILM:23.7K OHM,1%,0.125W	91637	MFF1816G23701F
A9R324	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A9R325	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A9R326	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R327	315-0430-00			RES.,FXD,CMPSN:43 OHM,5%,0.25W	01121	CB4305
A9R328	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R330	321-0183-00			RES.,FXD,FILM:787 OHM,1%,0.125W	91637	MFF1816G787R0F
A9R331	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R332	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R341	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A9R342	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A9R343	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A9R350	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A9R351	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A9R352	321-0133-00			RES.,FXD,FILM:237 OHM,1%,0.125W	91637	MFF1816G237R0F
A9R353	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R360	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A9R361	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A9R401	321-0272-00			RES.,FXD,FILM:6.65K OHM,1%,0.125W	91637	MFF1816G66500F
A9R402	321-0278-00			RES.,FXD,FILM:7.68K OHM,1%,0.125W	91637	MFF1816G76800F
A9R403	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A9R404	321-0236-00			RES.,FXD,FILM:2.8K OHM,1%,0.125W	91637	MFF1816G28000F
A9R410	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A9R420	315-0430-00			RES.,FXD,CMPSN:43 OHM,5%,0.25W	01121	CB4305
A9R422	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A9R423	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R424	315-0430-00			RES.,FXD,CMPSN:43 OHM,5%,0.25W	01121	CB4305
A9R425	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R430	321-0164-00			RES.,FXD,FILM:499 OHM,1%,0.125W	91637	MFF1816G499R0F
A9R431	315-0164-00			RES.,FXD,CMPSN:160K OHM,5%,0.25W	01121	CB1645
A9R432	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A9R433	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A9R450	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A9R452	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R461	315-0910-00			RES.,FXD,CMPSN:91 OHM,5%,0.25W	01121	CB9105
A9R463	315-0430-00			RES.,FXD,CMPSN:43 OHM,5%,0.25W	01121	CB4305
A9R503	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A9R504	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A9R505	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A9R506	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A9R510	321-0236-00			RES.,FXD,FILM:2.8K OHM,1%,0.125W	91637	MFF1816G28000F
A9R511	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A9R512	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A9R513	321-0236-00			RES.,FXD,FILM:2.8K OHM,1%,0.125W	91637	MFF1816G28000F
A9R514	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A9R515	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A9R516	321-0126-03			RES.,FXD,FILM:200 OHM,0.25%,0.125W	91637	MFF1816D200R0C

A9 INTERFACE (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A9R520	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
A9R521	321-0236-00			RES.,FXD,FILM:2.8K OHM,1%,0.125W	91637	MFF1816G28000F
A9R522	315-0430-00			RES.,FXD,CMPSN:43 OHM,5%,0.25W	01121	CB4305
A9R523	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R524	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A9R525	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A9R527	321-0325-00			RES.,FXD,FILM:23.7K OHM,1%,0.125W	91637	MFF1816G23701F
A9R528	321-0325-00			RES.,FXD,FILM:23.7K OHM,1%,0.125W	91637	MFF1816G23701F
A9R530	321-0183-00			RES.,FXD,FILM:787 OHM,1%,0.125W	91637	MFF1816G787R0F
A9R531	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R540	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R541	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R542	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A9R543	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A9R544	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R550	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A9R551	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A9R552	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R553	321-0133-00			RES.,FXD,FILM:237 OHM,1%,0.125W	91637	MFF1816G237R0F
A9R560	315-0910-00			RES.,FXD,CMPSN:91 OHM,5%,0.25W	01121	CB9105
A9R561	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R562	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A9R563	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A9R600	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A9R602	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A9R603	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A9R604	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A9R610	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A9R620	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A9R631	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A9R632	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A9R633	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A9R635	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A9R640	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R641	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R642	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A9R643	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A9R650	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A9R652	315-0334-00			RES.,FXD,CMPSN:330K OHM,5%,0.25W	01121	CB3345
A9R653	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A9R654	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A9R656	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A9R701	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A9R710	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	01121	206A102
A9R720	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A9R721	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A9R722	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A9R723	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A9R730	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A9R731	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A9R740	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R741	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A9R742	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A9R754	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A9R755	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R800	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A9R801	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A9R803	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A9R810	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A9R820	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A9R821	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A9R822	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A9R830	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A9R831	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A9R832	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A9R840	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A9R841	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R842	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R850	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R851	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A9R852	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A9R860	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A9R900	315-0563-00			RES.,FXD,CMPSN:56K OHM,5%,0.25W	01121	CB5635
A9R901	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A9R910	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A9R920	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A9R921	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A9R940	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R941	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A9U130	156-1225-00			MICROCIRCUIT,LI:DUAL COMPARATOR,8 DIP	27014	LM393N
A9U410	155-0022-00			MICROCIRCUIT,DI:ML,CHANNEL SWITCH	80009	155-0022-00
A9U610	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A9U630	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A9U700	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A9U710	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A9U720	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A9W421	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A9W630	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A9W750	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A9W751	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A9W752	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A9W753	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11	----- -----			CKT BOARD ASSY:MEMORY		
A11C123	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C150	281-0809-00			CAP.,FXD,CER DI:200PF,5%,100V	72982	8013T2ADDC1G201J
A11C151	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A11C160	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C191	290-0778-00			CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A11C192	290-0778-00			CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A11C250	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C260	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A11C270	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C320	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C340	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C450	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C510	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A11C520	281-0826-00			CAP.,FXD,CER DI:2200PF,5%,100V	04222	CA101C222KAA
A11C523	281-0820-00			CAP.,FXD,CER DI:680PF,10%,50V	12969	CGB681KDX
A11C540	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C550	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	72982	8035D9AADC1G470K
A11C570	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C630	281-0820-00			CAP.,FXD,CER DI:680PF,10%,50V	12969	CGB681KDX
A11C710	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C720	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C740	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C770	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C800	281-0158-00			CAP.,VAR,CER DI:7-45PF,50V	73899	DVJ-5006
A11C801	281-0158-00			CAP.,VAR,CER DI:7-45PF,50V	73899	DVJ-5006
A11C830	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C860	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C930	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A11C940	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1000	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A11C1080	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1110	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	72982	8035D9AADC1G470K
A11C1120	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1170	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1194	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	72982	1035D2ADC0G569D
A11C1200	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1230	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1291	283-0789-00			CAP.,FXD,MICA D:600PF,1%,500V	09023	CD15ED601F0
A11C1340	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A11C1350	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1380	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1390	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1395	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1450	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A11C1500	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1501	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A11C1550	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A11C1551	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A11C1570	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1591	283-0666-00			CAP.,FXD,MICA D:890PF,2%,100V	00853	D151F891G0
A11C1661	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A11C1662	281-0809-00			CAP.,FXD,CER DI:200PF,5%,100V	72982	8013T2ADDC1G201J
A11C1630	281-0809-00			CAP.,FXD,CER DI:200PF,5%,100V	72982	8013T2ADDC1G201J
A11C1639	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11C1690	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A11CR1194	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672

A11 MEMORY (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11CR1294	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A11CR1395	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A11L1291	108-0249-00			COIL,RF:12UH	76493	B-4992
A11L1395	108-0509-00			COIL,RF:2.45UH	80009	108-0509-00
A11L1495	108-0509-00			COIL,RF:2.45UH	80009	108-0509-00
A11Q340	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A11Q1190	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A11Q1191	151-0195-00			TRANSISTOR:SILICON,NPN	80009	151-0195-00
A11Q1192	151-0195-00			TRANSISTOR:SILICON,NPN	80009	151-0195-00
A11Q1295	151-0424-00			TRANSISTOR:SILICON,NPN	04713	SPS8246
A11R122	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R123	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A11R150	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A11R151	315-0333-00			RES.,FXD,CMPSN:33K OHM,5%,0.25W	01121	CB3335
A11R191	321-0231-00			RES.,FXD,FILM:2.49K OHM,1%,0.125W	91637	MFF1816G24900F
A11R192	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A11R193	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A11R194	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A11R195	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A11R240	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A11R250	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A11R251	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A11R260	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A11R291	321-0231-00			RES.,FXD,FILM:2.49K OHM,1%,0.125W	91637	MFF1816G24900F
A11R292	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A11R293	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A11R300	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R301	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R310	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R421	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A11R422	311-1263-00			RES.,VAR,NONWIR:1K OHM,10%,0.50W	32997	3329P-L58-102
A11R423	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A11R470	307-0502-00			RES,NTWK,THK FI:1.8 OHM,20%,(9) RES	91637	MSP10A01-182M
A11R501	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A11R510	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R520	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A11R522	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R523	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A11R550	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R552	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A11R615	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A11R620	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A11R710	307-0502-00			RES,NTWK,THK FI:1.8 OHM,20%,(9) RES	91637	MSP10A01-182M
A11R720	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R730	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R731	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R810	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A11R830	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R870	307-0502-00			RES,NTWK,THK FI:1.8 OHM,20%,(9) RES	91637	MSP10A01-182M
A11R930	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A11R1000	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A11R1100	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R1180	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A11R1181	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A11R1190	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A11R1192	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A11R1193	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225

A11 MEMORY (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11R1195	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A11R1280	307-0502-00			RES,NTWK,THK FI:1.8 OHM,20%,(9) RES	91637	MSP10A01-182M
A11R1285	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R1290	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R1291	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A11R1292	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A11R1293	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A11R1294	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	01121	CB1125
A11R1295	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A11R1300	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R1310	307-0502-00			RES,NTWK,THK FI:1.8 OHM,20%,(9) RES	91637	MSP10A01-182M
A11R1350	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R1395	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A11R1396	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A11R1420	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R1450	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A11R1500	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R1501	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A11R1550	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A11R1551	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A11R1591	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A11R1630	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A11R1631	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A11R1632	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A11R1660	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A11R1661	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A11R1662	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A11R1663	315-0751-00			RES.,FXD,CMPSN:750'OHM,5%,0.25W	01121	CB7515
A11U100	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U110	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A11U130	156-0452-00			MICROCIRCUIT,DI:4-WIDE 2-INP AND-OR-INVERT	80009	156-0452-00
A11U140	156-0452-00			MICROCIRCUIT,DI:4-WIDE 2-INP AND-OR-INVERT	80009	156-0452-00
A11U160	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U170	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01995	SN74LS257
A11U180	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U190	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U191	156-0927-02			MICROCIRCUIT,LI:DIGITAL/ANALOG CONVERTER	80009	156-0927-02
A11U200	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A11U210	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A11U220	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A11U230	156-0452-00			MICROCIRCUIT,DI:4-WIDE 2-INP AND-OR-INVERT	80009	156-0452-00
A11U240	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A11U250	156-0733-02			MICROCIRCUIT,DI:DUAL MONOSTABLE MV W/ST INP	80009	156-0733-02
A11U260	156-0387-02			MICROCIRCUIT,DI:DUAL J-K FF,BURN IN	80009	156-0387-02
A11U270	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U280	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U290	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U291	156-0927-02			MICROCIRCUIT,LI:DIGITAL/ANALOG CONVERTER	80009	156-0927-02
A11U300	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U310	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U320	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U330	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A11U340	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U350	156-0465-02			MICROCIRCUIT,DI:8 INP NAND GATE	01295	SN74LS30NP3
A11U360	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A11U370	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U380	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02

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A11 MEMORY (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11U390	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U400	156-0721-02			MICROCIRCUIT,DI:QUAD 2-IN NAND SCHMITT TRIG	80009	156-0721-02
A11U410	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U430	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U440	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A11U450	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A11U460	156-0866-00			MICROCIRCUIT,DI:13 INP NAND GATES	04713	SN74LS133
A11U470	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U480	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U490	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U500	156-0733-02			MICROCIRCUIT,DI:DUAL MONOSTABLE MV W/ST INP	80009	156-0733-02
A11U510	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U530	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A11U540	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A11U560	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U570	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U580	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U590	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U600	156-0387-02			MICROCIRCUIT,DI:DUAL J-K FF,BURN IN	80009	156-0387-02
A11U610	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A11U620	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U630	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U640	156-0804-00			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH	07263	74LS279PC
A11U650	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A11U660	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U670	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U680	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U690	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U700	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U710	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	80009	156-0464-02
A11U720	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A11U730	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U740	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U750	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U760	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U770	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U780	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U790	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U800	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A11U810	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U820	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U830	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A11U840	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U850	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U860	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U870	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U880	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U890	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	80009	156-0852-02
A11U900	156-0804-00			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH	07263	74LS279PC
A11U910	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U920	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U930	156-0478-02			MICROCIRCUIT,DI:DUAL 4 INP & GATE,BURN-IN	01295	SN74LS21NP3
A11U940	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U950	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U960	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	80009	156-0391-02
A11U970	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	80009	156-0391-02
A11U980	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	80009	156-0391-02

A11 MEMORY (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11U990	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	80009	156-0391-02
A11U1000	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U1010	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A11U1020	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U1030	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN DNTR	01295	SN74LS193
A11U1040	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U1050	156-0651-02			MICROCIRCUIT,DI:8-BIT PRL-OUT SER SHF RGTR	80009	156-0651-02
A11U1060	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U1070	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U1090	156-0651-02			MICROCIRCUIT,DI:8-BIT PRL-OUT SER SHF RGTR	80009	156-0651-02
A11U1100	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A11U1110	156-0478-02			MICROCIRCUIT,DI:DUAL 4 INP & GATE,BURN-IN	01295	SN74LS21NP3
A11U1120	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U1130	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U1140	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U1150	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U1160	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U1170	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U1200	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
A11U1210	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A11U1220	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U1230	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U1240	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U1250	156-0651-02			MICROCIRCUIT,DI:8-BIT PRL-OUT SER SHF RGTR	80009	156-0651-02
A11U1260	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U1270	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A11U1280	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A11U1290	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U1291	156-0707-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	01295	SN74S86N
A11U1300	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U1310	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U1320	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U1330	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U1340	156-0989-02			MICROCIRCUIT,DI:4X4 RGTR FILE W/3 STATE OUT	80009	156-0989-02
A11U1350	156-0733-02			MICROCIRCUIT,DI:DUAL MONOSTABLE MV W/ST INP	80009	156-0733-02
A11U1360	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U1370	156-0529-00			MICROCIRCUIT,DI:DATA SELECTOR,16 PIN DIP	01295	SN74LS257N
A11U1380	156-0989-02			MICROCIRCUIT,DI:4X4 RGTR FILE W/3 STATE OUT	80009	156-0989-02
A11U1390	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U1391	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U1395	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A11U1400	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A11U1410	156-0387-02			MICROCIRCUIT,DI:DUAL J-K FF,BURN IN	80009	156-0387-02
A11U1420	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U1430	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U1440	156-0989-02			MICROCIRCUIT,DI:4X4 RGTR FILE W/3 STATE OUT	80009	156-0989-02
A11U1450	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A11U1460	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U1470	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U1480	156-0989-02			MICROCIRCUIT,DI:4X4 RGTR FILE W/3 STATE OUT	80009	156-0989-02
A11U1490	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U1491	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U1495	156-0707-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	01295	SN74S86N
A11U1500	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-00
A11U1510	156-0895-01			MICROCIRCUIT,DI:14-BIT BINARY COUNTER	80009	156-0895-01
A11U1520	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A11U1530	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193

A11 MEMORY (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11U1540	156-0989-02			MICROCIRCUIT,DI:4X4 RGTR FILE W/3 STATE OUT	80009	156-0989-02
A11U1550	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U1560	156-0529-00			MICROCIRCUIT,DI:DATA SELECTOR,16 PIN DIP	01295	SN74LS257N
A11U1570	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U1580	156-0989-02			MICROCIRCUIT,DI:4X4 RGTR FILE W/3 STATE OUT	80009	156-0989-02
A11U1590	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U1591	156-0412-02			MICROCIRCUIT,DI:SYN 4-BIT UP/DOWN CNTR	01295	SN74LS193
A11U1610	156-0895-01			MICROCIRCUIT,DI:14-BIT BINARY COUNTER	80009	156-0895-01
A11U1620	156-0172-02			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	01295	SN74123
A11U1640	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A11U1670	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A11U1680	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A11U1690	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11U1691	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A11U1695	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A11VR1181	156-0278-00			MICROCIRCUIT,DI:DIVIDED BY 10 COUNTER	52648	SP8630B
A11VR1182	156-0278-00			MICROCIRCUIT,DI:DIVIDED BY 10 COUNTER	52648	SP8630B

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A14	670-6311-00			CKT BOARD ASSY:CONNECTOR	80009	670-6311-00
A14C110	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A14C220	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A14C310	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A14C410	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
A14R110	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A14U100	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A14U110	156-0916-00			MICROCIRCUIT,DI:EIGHT 2-INP 3-STATE BFR	80009	156-0916-00
A14U210	156-1111-01			MICROCIRCUIT,DI:OCTAL BUS XCVR W/3 ST OUT	80009	156-1111-01
A14U200	156-1257-00			MICROCIRCUIT,DI:GPIB TALKER/LISTENER	34649	D8291
A14U310	156-1414-00			MICROCIRCUIT,DI:OCTAL GPIB XCVR DATA BUS	01295	SN75160
A14U311	156-1415-00			MICROCIRCUIT,DI:OCTAL GPIB XCVR MGT BUS	01295	SN75161
A14W410	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	55210	L-2007-1
A15	670-6312-00			CKT BOARD ASSY:REAR PANEL	80009	670-6312-00
A15S300	260-1721-00			SWITCH,ROCKER:8,SPST,125MA,30VDC	00779	435166-5

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A18	670-5951-00			CKT BOARD ASSY:GPIB	80009	670-5951-00
A18C180	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A18C290	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A18C334	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	72982	8005H9AADW5R472K
A18C336	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	72982	8035D9AADC1G220K
A18C340	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A18C341	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A18C342	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A18C350	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C360	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C361	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	72982	8035D2AADX5R271K
A18C362	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A18C371	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A18C372	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	72982	8035D2AADC0G680K
A18C373	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	72982	8035D9AADC1G220K
A18C374	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	56289	503D475G035AS
A18C375	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	72982	8005H9AADW5R472K
A18C400	281-0809-00			CAP.,FXD,CER DI:200PF,5%,100V	72982	8013T2ADDC1G201J
A18C430	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	72982	8035D2AADC0G680K
A18C431	290-0525-00			CAP.,FXD,ELCTLT:4.7UF,20%,50V	56289	196D475X0050KA1
A18C440	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	56289	503D475G035AS
A18C450	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A18C470	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A18C500	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C520	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C550	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C600	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C660	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C730	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C780	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C800	283-0788-00			CAP.,FXD,MICA D:267PF,1%,500V	09023	CD15F0(267)F03
A18C820	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C851	281-0798-00			CAP.,FXD,CER DI:51PF,1%,100V	04222	MC101A510G
A18C853	281-0798-00			CAP.,FXD,CER DI:51PF,1%,100V	04222	MC101A510G
A18C860	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C890	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A18C900	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A18CR180	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR190	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR334	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR340	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR341	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR342	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR343	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR344	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR360	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR361	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR362	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR363	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR370	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR371	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR900	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR910	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18CR911	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A18L340	108-0240-00			COIL,RF:FIXED,820UH	76493	B5147
A18L360	108-0240-00			COIL,RF:FIXED,820UH	76493	B5147
A18L370	108-0240-00			COIL,RF:FIXED,820UH	76493	B5147

A18 GPIB (CONT)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A18L430	108-0240-00			COIL,RF:FIXED,820UH	76493	B5147
A18Q180	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A18Q181	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A18Q290	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A18Q320	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A18Q330	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A18Q331	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A18Q332	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A18Q360	151-1042-00			SEMICOND DVC SE:MATCHED PAIR FET	27014	SF50031
A18Q361	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A18Q362	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A18Q370	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A18Q371	151-1042-00			SEMICOND DVC SE:MATCHED PAIR FET	27014	SF50031
A18Q430	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A18Q450	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A18Q460	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A18Q461	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A18Q462	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A18Q470	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A18Q800	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A18Q900	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A18R100	315-0270-00			RES.,FXD,CMPSN:27 OHM,5%,0.25W	01121	CB2705
A18R180A,B	311-2046-00			RES.,VAR,NONWW:PNL,DUAL 10K OHM & 2.5K OHM	12697	CM41748
A18R190A,B	311-2046-00			RES.,VAR,NONWW:PNL,DUAL 10K OHM & 2.5K OHM	12697	CM41748
A18R200	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A18R201	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A18R202	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A18R203	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A18R220	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A18R221	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A18R230	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A18R231	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A18R250	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A18R251	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A18R260	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A18R261	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A18R280	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A18R281	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A18R282	321-0613-00			RES.,FXD,FILM:5.03K OHM,1%,0.125W	91637	MFF1816G50300F
A18R283	321-0268-00			RES.,FXD,FILM:6.04K OHM,1%,0.125W	91637	MFF1816G60400F
A18R284	321-1676-03			RES.,FXD,FILM:230.7 OHM,0.25%,0.125W	91637	MFF1816D230R7C
A18R285	321-0242-00			RES.,FXD,FILM:3.24K OHM,1%,0.125W	91637	MFF1816G32400F
A18R286	321-0247-00			RES.,FXD,FILM:3.65K OHM,1%,0.125W	91637	MFF1816G36500F
A18R287	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A18R288	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A18R290	321-0325-00			RES.,FXD,FILM:23.7K OHM,1%,0.125W	91637	MFF1816G23701F
A18R291	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A18R292	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A18R293	321-0255-00			RES.,FXD,FILM:4.42K OHM,1%,0.125W	91637	MFF1816G44200F
A18R294	321-1296-07			RES.,FXD,FILM:12K OHM,0.1%,0.125W	91637	MFF1816C12001B
A18R295	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A18R296	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A18R300	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A18R310	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A18R330	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A18R331	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A18R332	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A18R333	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A18R334	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A18R335	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A18R336	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A18R337	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A18R338	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A18R340	321-0186-00			RES.,FXD,FILM:845 OHM,1%,0.125W	91637	MFF1816G845R0F
A18R341	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A18R350	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A18R360	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A18R361	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A18R362	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A18R363	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A18R370	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A18R371	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A18R372	321-0186-00			RES.,FXD,FILM:845 OHM,1%,0.125W	91637	MFF1816G845R0F
A18R373	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A18R374	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A18R375	321-1676-03			RES.,FXD,FILM:230.7 OHM,0.25%,0.125W	91637	MFF1816D230R7C
A18R376	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A18R377	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A18R378	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A18R379	307-0103-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A18R390	321-0243-00			RES.,FXD,FILM:3.32K OHM,1%,0.125W	91637	MFF1816G33200F
A18R391	321-0242-00			RES.,FXD,FILM:3.24K OHM,1%,0.125W	91637	MFF1816G32400F
A18R392	321-0247-00			RES.,FXD,FILM:3.65K OHM,1%,0.125W	91637	MFF1816G36500F
A18R430	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A18R431	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A18R432	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A18R433	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A18R434	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A18R435	321-0258-00			RES.,FXD,FILM:4.75K OHM,1%,0.125W	91637	MFF1816G47500F
A18R436	321-0201-00			RES.,FXD,FILM:1.21K OHM,1%,0.125W	91637	MFF1816G12100F
A18R437	321-0212-00			RES.,FXD,FILM:1.58K OHM,1%,0.125W	91637	MFF1816G15800F
A18R440	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A18R441	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A18R442	321-0223-00			RES.,FXD,FILM:2.05K OHM,1%,0.125W	91637	MFF1816G20500F
A18R443	321-0126-00			RES.,FXD,FILM:200 OHM,1%,0.125W	91637	MFF1816G200R0F
A18R444	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A18R445	321-0209-00			RES.,FXD,FILM:1.47K OHM,1%,0.125W	91637	MFF1816G14700F
A18R446	307-0103-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A18R450	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A18R452	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A18R460	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A18R461	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A18R462	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A18R463	321-0214-00			RES.,FXD,FILM:1.65K OHM,1%,0.125W	91637	MFF1816G16500F
A18R464	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A18R465	321-0258-00			RES.,FXD,FILM:4.75K OHM,1%,0.125W	91637	MFF1816G47500F
A18R466	321-0223-00			RES.,FXD,FILM:2.05K OHM,1%,0.125W	91637	MFF1816G20500F
A18R470	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A18R471	321-0201-00			RES.,FXD,FILM:1.21K OHM,1%,0.125W	91637	MFF1816G12100F
A18R472	321-0212-00			RES.,FXD,FILM:1.58K OHM,1%,0.125W	91637	MFF1816G15800F
A18R473	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A18R474	321-0132-00			RES.,FXD,FILM:232 OHM,1%,0.125W	91637	MFF1816G232R0F
A18R601	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A18R650	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A18R700	307-0586-00			RES NTWK,FXD FI:9.39K OHM,2%,1.25W	32997	4310R-101-393G
A18R710	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A18R710	307-1137-00			RES,NTWK,FXD,FI:8,5M OHM,50%,0.125W	03888	A3UT17
A18R750	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	91637	MSP06A01-103J
A18R751	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	01121	206A102
A18R800	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A18R810	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A18R830	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A18R850	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A18R851	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A18R853	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A18R900	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A18R901	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A18R910	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A18R911	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	MFF1816G549R0F
A18R912	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	MFF1816G549R0F
A18R913	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A18R914	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A18R940	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A18S210	263-0010-00			SWITCH PB ASSY:1 PUSH,7.5MM,W/2 CONTACTS	80009	263-0010-00
A18S220	263-0010-00			SWITCH PB ASSY:1 PUSH,7.5MM,W/2 CONTACTS	80009	263-0010-00
A18S230	263-0010-00			SWITCH PB ASSY:1 PUSH,7.5MM,W/2 CONTACTS	80009	263-0010-00
A18S240	263-0010-00			SWITCH PB ASSY:1 PUSH,7.5MM,W/2 CONTACTS	80009	263-0010-00
A18S250	263-0010-00			SWITCH PB ASSY:1 PUSH,7.5MM,W/2 CONTACTS	80009	263-0010-00
A18S260	263-0033-00			SWITCH,PB ASSY:1 MOMENTARY,7.5MM,2 CONTACT	80009	263-0033-00
A18S270	263-0010-00			SWITCH PB ASSY:1 PUSH,7.5MM,W/2 CONTACTS	80009	263-0010-00
A18S280	263-0010-00			SWITCH PB ASSY:1 PUSH,7.5MM,W/2 CONTACTS	80009	263-0010-00
A18U200	156-1225-00			MICROCIRCUIT,LI:DUAL COMPARATOR,8 DIP	27014	LM393N
A18U280	156-1272-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	LM393N
A18U290	156-0158-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	MC1458V
A18U300	156-0982-00			MICROCIRCUIT,DI:OCTAL D EDGE TRIG F-F	80009	156-0982-00
A18U310	156-0914-00			MICROCIRCUIT,DI:OCT ST BFR W/3-STATE OUT	01295	SN74LS240
A18U320	156-0529-00			MICROCIRCUIT,DI:DATA SELECTOR,16 PIN DIP	01295	SN74LS257N
A18U350	156-0644-00			MICROCIRCUIT,DI:QUAD BILATERAL SWITCH	80009	156-0644-00
A18U400	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	80009	156-0388-00
A18U410	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00(N OR J)
A18U420	156-0529-00			MICROCIRCUIT,DI:DATA SELECTOR,16 PIN DIP	01295	SN74LS257N
A18U450	156-0259-01			MICROCIRCUIT,DI:3-LINE TO 8-LINE DCDR	80009	156-0259-01
A18U500	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A18U510	156-1127-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1127-01
A18U520	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A18U530	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A18U540	156-0469-01			MICROCIRCUIT,DI:3-LINE TO 8-LINE DCDR	80009	156-0469-01
A18U550	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A18U560	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS25
A18U570	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS25
A18U580	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS25
A18U600	160-0731-00			MICROCIRCUIT,DI:4096 X 8 E PROM	80009	160-0731-00
A18U620	160-1026-00			MICROCIRCUIT,DI:2048 X 8 E PROM	80009	160-1026-00
A18U640	156-0469-01			MICROCIRCUIT,DI:3-LINE TO 8-LINE DCDR	80009	156-0469-01
A18U650	156-0982-01			MICROCIRCUIT,DI:OCTAL D EDGE TRIG FLIP FLOP	80009	156-0982-01
A18U660	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A18U670	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A18U680	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18U690	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18U700	156-0983-00			MICROCIRCUIT,DI:MICROPROCESSOR EIGHT BIT	80009	156-0983-00
A18U710	307-1137-00			RES,NTWK,FXD,FI:8,5M OHM,50%,0.125W	03888	A3UT17

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Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A18U730	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A18U740	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	80009	156-0383-02
A18U750	156-0982-01			MICROCIRCUIT,DI:OCATL D EDGE,TRIG FLIP FLOP	80009	156-0982-01
A18U760	156-0392-02			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	80009	156-0392-02
A18U762	156-0982-01			MICROCIRCUIT,DI:OCTAL D EDGE TRIG FLIP FLOP	80009	156-0982-01
A18U770	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18U772	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18U780	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18U790	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18U810	156-0955-00			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	07263	74LS241 PC OR DC
A18U820	156-0469-01			MICROCIRCUIT,DI:3-LINE TO 8-LINE DCDR	80009	156-0469-01
A18U830	156-1111-01			MICROCIRCUIT,DI:OCTAL BUS XCVR W/3 ST OUT	80009	156-1111-01
A18U840	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373
A18U850	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373
A18U860	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18U870	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18U880	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18U890	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	012955	SN74LS257
A18U920	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A18U930	156-0804-01			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH	80009	156-0804-01
A18U950	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED FF	80009	156-1059-00
A18U960	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18U970	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR	01295	SN74LS257
A18VR440	152-0306-00			SEMICOND DEVICE:ZENER,0.4W,9.1V,5%	14433	1N960B
A18VR460	152-0306-00			SEMICOND DEVICE:ZENER,0.4W,9.1V,5%	14433	1N960B

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
B25	119-0215-06			FAN,TUBEAXIAL:115V,13W	23936	8500C
C52	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	72982	831-516E102P
CR140	152-0668-00			SEMICOND DEVICE:RECT BRIDGE,SI,200V,6A	80009	152-0668-00
CR150	152-0640-00			SEMICOND DEVICE:SILICON,35V,30A,DO-4	01281	SD-4101
CR900	152-0068-00			SEMICOND DVC,DI:RECT BRIDGE,SI,200V,6A	80009	152-0668-00
DS22	150-0121-04			LAMP,CARTRIDGE:5V,0.06A	80009	150-0121-04
DS100	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,SEL	76854	17AS15
DS200	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,SEL	76854	17AS15
DS300	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,SEL	76854	17AS15
DL90	119-0773-02			DELAY LINE,ELEC:500 PSEC,150 OHM,COIL	80009	119-0733-02
F20	159-0023-00			FUSE,CARTRIDGE:3AG,2A,250V,5SEC	71400	MDX-2
F26	159-0044-00			FUSE,CARTRIDGE:3AG,0.2A,250V,SLOW-BLOW	71400	MDL 2/10
F28	159-0044-00			FUSE,CARTRIDGE:3AG,0.2A,250V,SLOW-BLOW	71400	MDL 2/10
F30	159-0160-00			FUSE,CARTRIDGE:3AG,1.5 A,250V,18 SEC,UL	71400	MDX 1-1/2
F32	159-0027-00			FUSE,CARTRIDGE:3AG,4A,125V,SLOW-BLOW	71400	MDX4
F33	159-0027-00			FUSE,CARTRIDGE:3AG,4A,125V,SLOW-BLOW	71400	MDX4
F34	159-0160-00			FUSE,CARTRIDGE:3AG,1.5 A,250V,18 SEC,UL	71400	MDX 1-1/2
FL20	119-0813-00			SELECTOR,VOLTS:W/LINE FLTR RCPT & FUSE	02777	F65003
L51	108-1010-00			COIL,TUBE DEFL:TRACE ROTATOR	80009	108-1010-00
Q60	151-0140-00			TRANSISTOR:SILICON,NPN	80009	151-0140-00
Q62	151-0140-00			TRANSISTOR:SILICON,NPN	80009	151-0140-00
Q120	151-0464-00			TRANSISTOR:SILICON,NPN	80009	151-0464-00
Q500	151-0482-00			TRANSISTOR:SILICON,PNP	80009	151-0482-00
Q600	151-0405-00			TRANSISTOR:SILICON,NPN	04713	SJE943
Q660	151-0625-00			TRANSISTOR:SILICON,PNP	03508	D45H11
Q760	151-0625-00			TRANSISTOR:SILICON,PNP	03508	D45H11
Q1200	151-0429-00			TRANSISTOR:SILICON,PNP	04713	SJE957
Q1320	151-0482-00			TRANSISTOR:SILICON,PNP	80009	151-0482-00
Q1340	151-0528-00			TRANSISTOR:SILICON,50V,16A	04713	2N6400
R47	311-2044-00			RES.,VAR,NONWW:PNL,500K OHM,5%,1.0W	01121	70F1G040L504X
S21	260-0724-01			SWITCH,THRMSTC:NC,OPEN 83.3,CL 66.7,10V	14859	20704-L67-322
S22	260-1222-00			SWITCH,PUSH-PUL:10A,250VAC	91929	2DM301
T25	120-1291-00			XFMR,PWR,STPDN:LF	80009	120-1291-00
V51	154-0827-00			ELECTRON TUBE:CRT,P31,INT SCALE	80009	154-0827-00

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966 Drafting Practices.
Y14.2, 1973 Line Conventions and Lettering.
Y10.5, 1968 Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

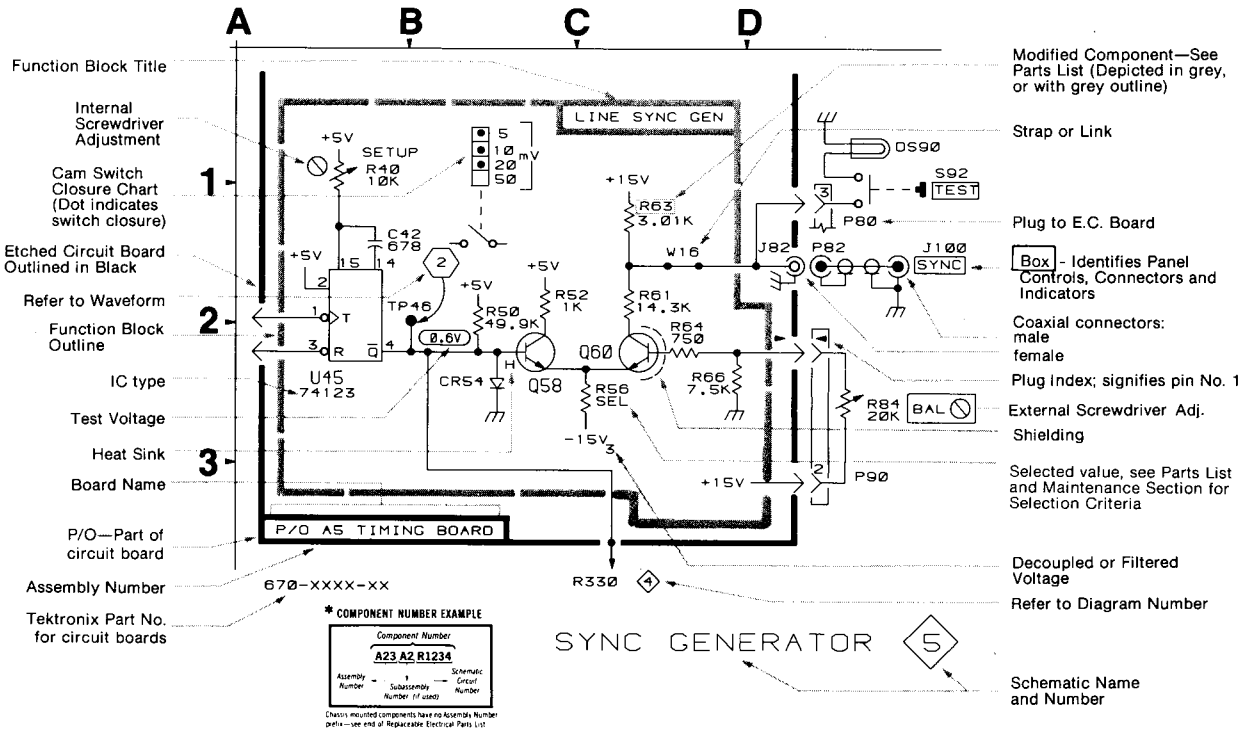
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



@

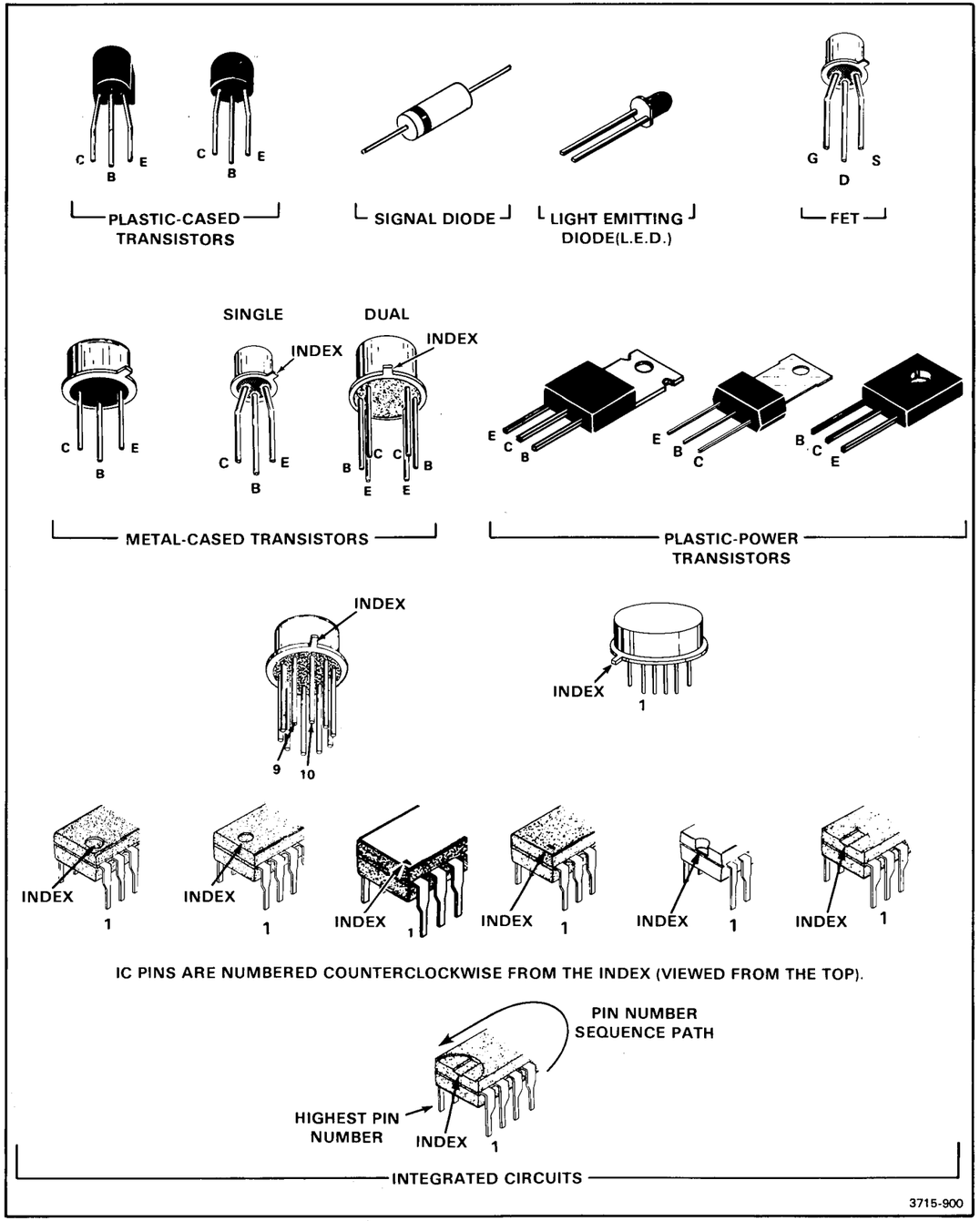
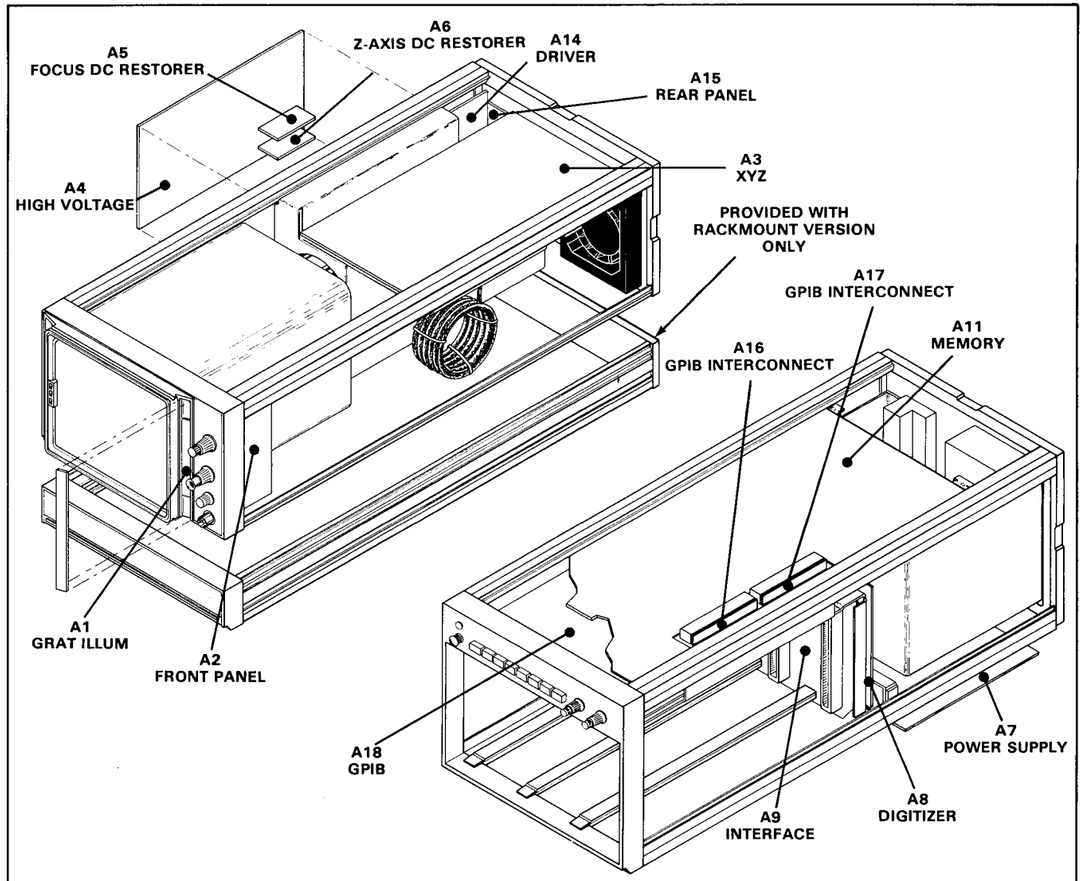


Figure 9-1. Semiconductor Lead Configurations.



BOARD LOCATOR BY ASSEMBLY NUMBER			BOARD LOCATOR BY BOARD NAME		
Assembly Number	Board Name	Schematic Location	Board Name	Assembly Number	Schematic Location
A1	Grat Illum.	5	Focus DC Restorer	A5	6
A2	Front Panel	5	Z-Axis DC Restorer	A6	6
A3	XYZ	3,4,6,12	Digitizer	A8	8,9,11
A4	HV	6	Driver	A14	20,24
A5	Focus DC Restorer	6	Front Panel	A2	5
A6	Z-Axis DC Restorer	6	GPIB	A18	7,10,11,18,20,
A7	Power Supply	7			21,22,23
A8	Digitizer	8,9,11	GPIB Intercon.	A16	11,21,22
A9	Interface	1,2,12	GPIB Intercon.	A17	11,21,22
A11	Memory	5,9,10,11,12,13	Grat Illum.	A1	5
		14,15,16,17,18	H.V.	A4	6
A14	Driver	20,24	Interface	A9	1,2,12
A15	Rear Panel	20,24	Memory	A11	5,9,10,11,12,13
A16	GPIB Intercon.	11,21,22			14,15,16,17,18
A17	GPIB Intercon.	11,21,22	Power Supply	A7	7
A18	GPIB	7,10,11,18,20	Rear Panel	A15	20,24
		21,22,23	XYZ	A3	3,4,6,12

3715-79

Figure 9-2. 5223 Option 10 Circuit Board Locations.

5223 Option 10

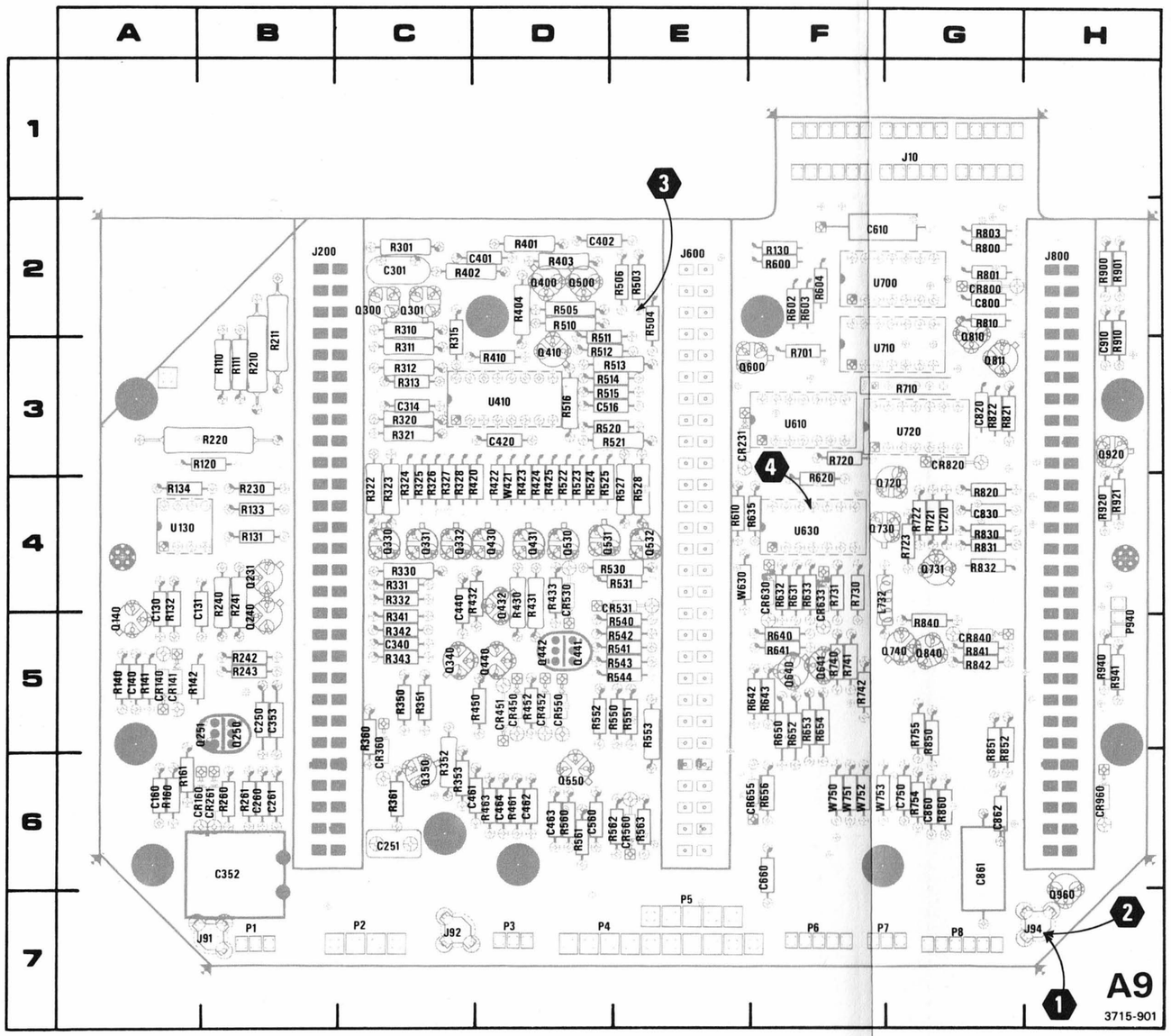


Figure 9-3. A9-Interface circuit board assembly.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CI NU
C160	A5	A6	J1
C250	B6	B5	J9
C251	A6	C6	J2
C260	A5	B6	J6
C261	B5	B6	J8
C352	B6	B6	
C353	B6	B5	L7
C461	B5	C6	
C462	B6	D6	P1
C463	C6	D6	P2
C560	D5	D6	P3
C610	B5	F2	P4
C660	C5	F6	P5
C720	F4	G4	P6
C750	D6	G6	P6
C800	E3	G2	P7
C820	G3	G3	P8
C830	F3	G4	P8
C860	D6	G6	P8
C861	B6	G6	P9
C862	E5	G6	
C910	D3	H3	Q2
			Q2
CR160	A4	A6	Q3
CR231	A1	E3	Q4
CR261	A4	B6	Q4
CR360	B5	C6	Q5
CR452	C4	D5	Q6
CR550	C4	D5	Q6
CR560	C5	E6	Q6
CR630	G5	F4	Q7
CR633	G5	F4	Q7
CR655	G5	E6	Q7
CR800	F3	G2	Q7
CR820	F3	G3	Q8
CR840	D4	G5	Q8
CR960	E5	H6	Q8
			Q9
J10	B1	G1	Q9
J10	F6	G1	

Partial A9 also shown on diagrams 2 and

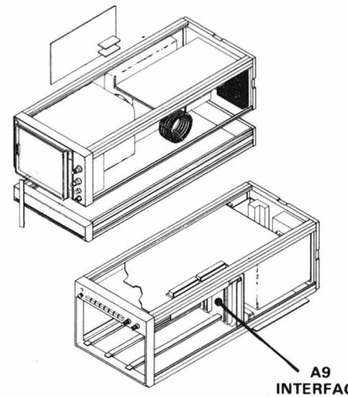
ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CI NU
P10	B1	H4	P1

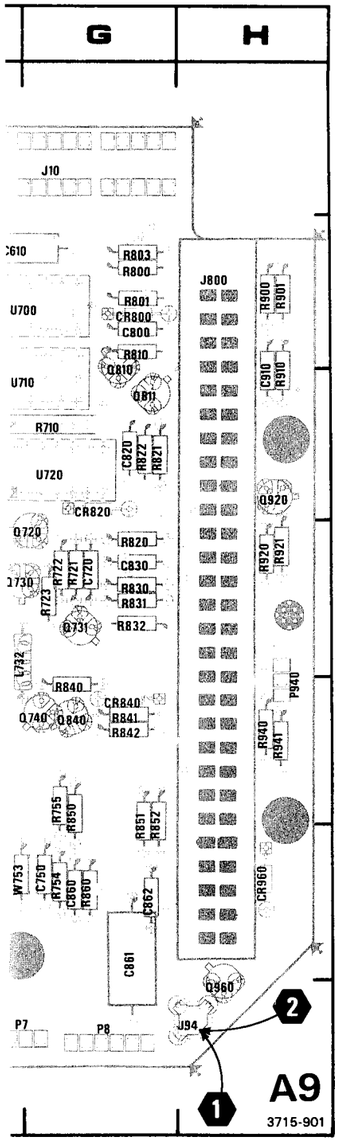
Partial A11 also shown on diagrams 5, 8,

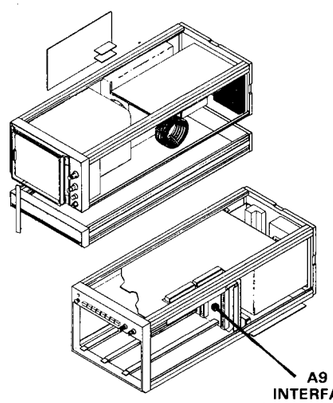
CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CI NU
J94	F6	CHASSIS	P9



A9 INTERFACE
Shown on Diag. 1 & 2





MAIN INTERFACE DIAGRAM ①

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C160	A5	A6	J10	E1	G1	R120	B1	B3	R604	B1	F2	R830	F2	G4
C250	B6	B5	J94	F6	H7	R130	B1	F2	R610	B2	E4	R831	F2	G4
C251	A6	C6	J200	A2	B2	R131	B1	B4	R620	F3	F4	R832	F3	G4
C260	A5	B6	J600	C2	E2	R133	B1	B4	R631	G5	F4	R840	D4	G5
C261	B5	B6	J800	E2	H2	R134	B1	A4	R632	G5	F4	R841	D4	G5
C352	B6	B6				R160	A5	A6	R633	G5	F4	R842	D4	G5
C353	B6	B5	L732	B6	F4	R161	A4	A6	R635	A1	E4	R850	D5	G5
C461	B5	C6				R230	B1	B4	R640	F5	F5	R851	E4	G5
C462	B6	D6	P1	A6	B7	R242	A4	B5	R641	F4	F5	R852	D4	G5
C463	C6	D6	P2	E6	C7	R243	A4	B5	R642	F4	F5	R860	D6	G6
C560	D5	D6	P3	B6	D7	R260	A4	B6	R643	F5	F5	R900	D3	H2
C610	B5	F2	P4	A6	D7	R341	B4	C5	R650	G5	F5	R901	D3	H2
C660	C5	F6	P5	C6	E7	R342	B4	C5	R652	G5	F5	R910	D3	H3
C720	F4	G4	P6	H4	F7	R350	B5	C5	R653	G5	F5	R920	D3	H4
C750	D6	G6	P6	D6	F7	R351	B5	C5	R654	G5	F5	R921	F5	H4
C800	E3	G2	P7	D6	F7	R352	B5	C6	R656	G5	F6	R940	E4	H5
C820	G3	G3	P8	A1	G7	R353	B5	C6	R701	B2	F3	R941	E5	H5
C830	F3	G4	P8	G1	G7	R360	B5	C5	R710A	F1	G3			
C860	D6	G6	P8	D1	G7	R361	B5	C6	R710B	G1	G3	U130A	B1	A4
C861	B6	G6	P940	E5	H5	R452	B4	D5	R710C	B5	G3	U130B	B1	A4
C862	E5	G6				R461	B6	D6	R710D	G3	G3	U610A	G1	F3
C910	D3	H3	Q250	A4	B5	R503	D2	E2	R710E	F2	G3	U610B	F2	F3
			Q251	A4	B5	R504	D2	E2	R720	F3	F3	U630A	G5	F4
CR160	A4	A6	Q350	B5	C6	R506	B1	E2	R721	F3	G4	U630B	G5	F4
CR231	A1	E3	Q441	C5	D5	R515	D2	D3	R722	F3	G4	U630C	F3	F4
CR261	A4	B6	Q442	C4	D5	R541	C4	E5	R723	F3	G4	U630D	F3	F4
CR360	B5	C6	Q550	D5	D6	R542	C4	E5	R730	F4	F4	U700A	C2	F2
CR452	C4	D5	Q600	A1	E3	R543	C4	E5	R731	F4	F4	U700B	F5	F2
CR550	C4	D5	Q640	G5	F5	R544	C4	E5	R740	F4	F5	U700C	G5	F2
CR560	C5	E6	Q641	G5	F5	R550	D5	E5	R741	F4	F5	U700D	D2	F2
CR630	G5	F4	Q720	F3	G4	R551	D5	E5	R742	F4	F5	U710A	F1	G3
CR633	G5	F4	Q730	F3	F4	R552	C4	D5	R754	D6	G6	U710B	F1	G3
CR655	G5	E6	Q731	F2	G4	R553	D5	E5	R755	D4	G5	U720A	F3	G3
CR800	F3	G2	Q740	D4	G5	R560	C6	D6	R800	E3	G2	U720B	E2	G3
CR820	F3	G3	Q810	E3	G3	R561	D5	D6	R801	F3	G2			
CR840	D4	G5	Q811	G3	G3	R562	C5	E6	R803	F5	G2	W630	D4	E4
CR960	E5	H6	Q840	D4	G5	R563	C5	E6	R810	E4	G2	W750	H5	F6
			Q920	D3	H3	R600	B1	F2	R820	F3	G4	W751	H5	F6
J10	B1	G1	Q960	E5	H7	R602	C2	F2	R821	G3	G3	W752	H4	F6
J10	F6	G1				R603	C2	F2	R822	F3	G3	W753	B6	F6

Partial A9 also shown on diagrams 2 and 12.

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION		
P10	B1	H4	P10	F6	H4	P10	E1	H4		

Partial A11 also shown on diagrams 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, and 17.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION			
J94	F6	CHASSIS	P94	F6	CHASSIS			

VOLTAGE AND WAVEFORM CONDITIONS

Voltage Conditions. The test voltages (circled numbers) on the schematic were taken using a digital multimeter with 10 MΩ input impedance (TEKTRONIX DM501A Digital Multimeter installed in a TM501 Power Module or a TEKTRONIX 7D13 Digital Multimeter used with a readout equipped 7000-series oscilloscope).

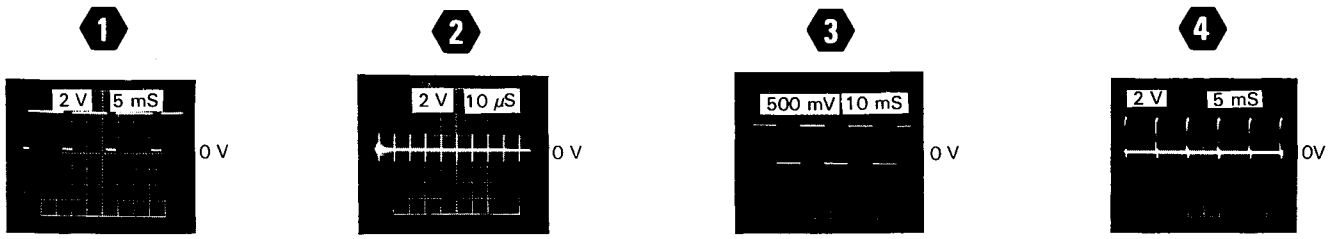
No plug-in units were installed.

Waveform Conditions. A 5B25N Digitizer Time Base/Ampl with controls set as follows: Time/Div (1 ms), Chop (In), Triggering (AC, Auto, Left) and two 5000 series vertical amplifiers with controls set as follows: Volts/Div (1V), Display (On) were installed in the appropriate compartments of the 5223. A 1 volt, 1 kHz square-wave was applied to both vertical amplifier inputs.

The 5223 controls were set as follows: Memory Contents pushbuttons—Display (both in) Vector Mode (in), Display Speed Out (fully cw). All other buttons (out).

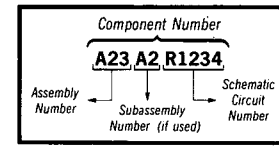
The waveforms were monitored using a test oscilloscope system with 10 MΩ input impedance, at least 60 MHz bandwidth and 10X probe (TEKTRONIX 7603 Oscilloscope, 7B92A Time Base, 7A13 Differential Comparator and P6062B Probe).

Refer to the individual waveform photos for deflection factor and sweep rate settings.

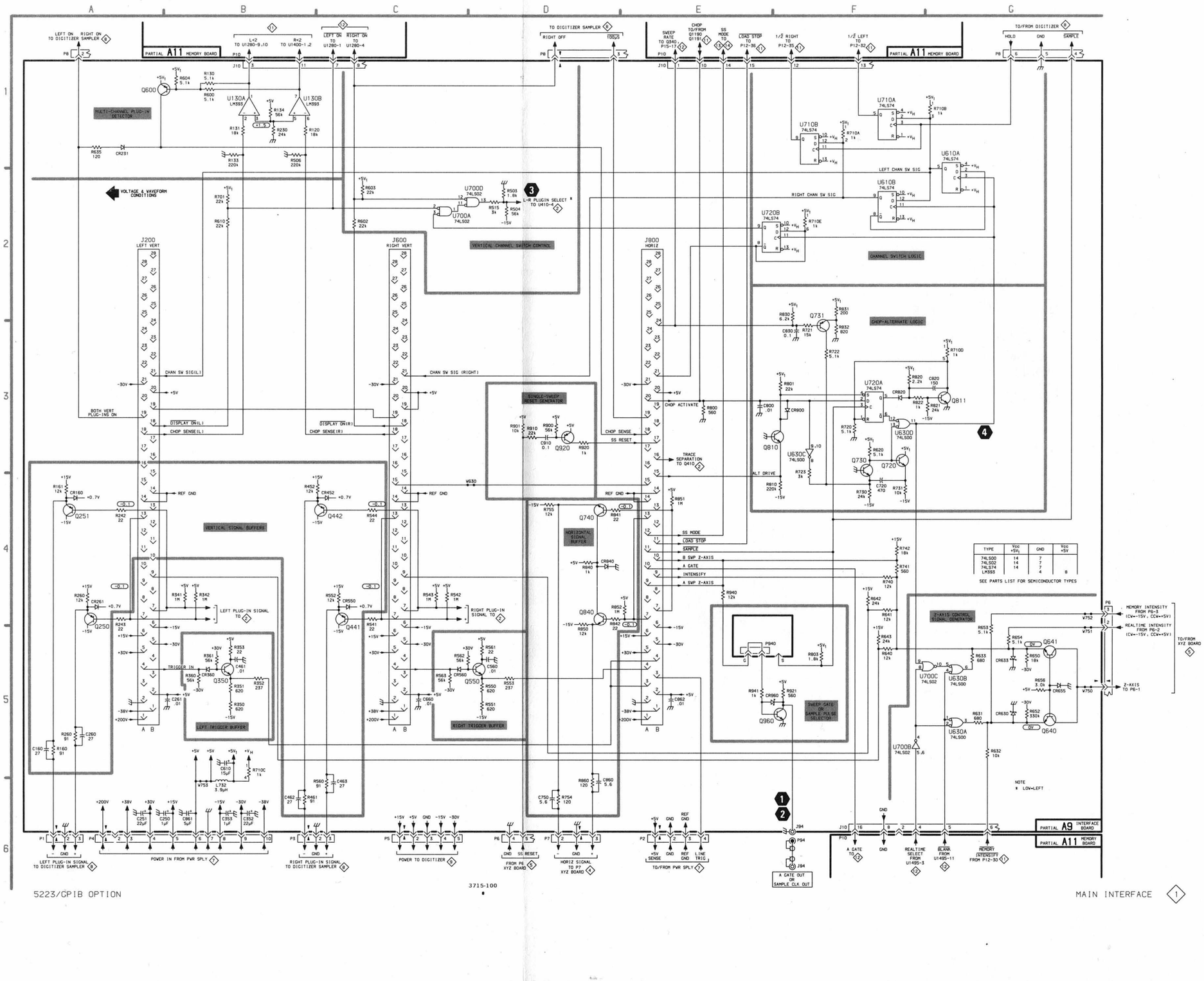


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



5223/GPIB OPTION

3715-100

MAIN INTERFACE 1

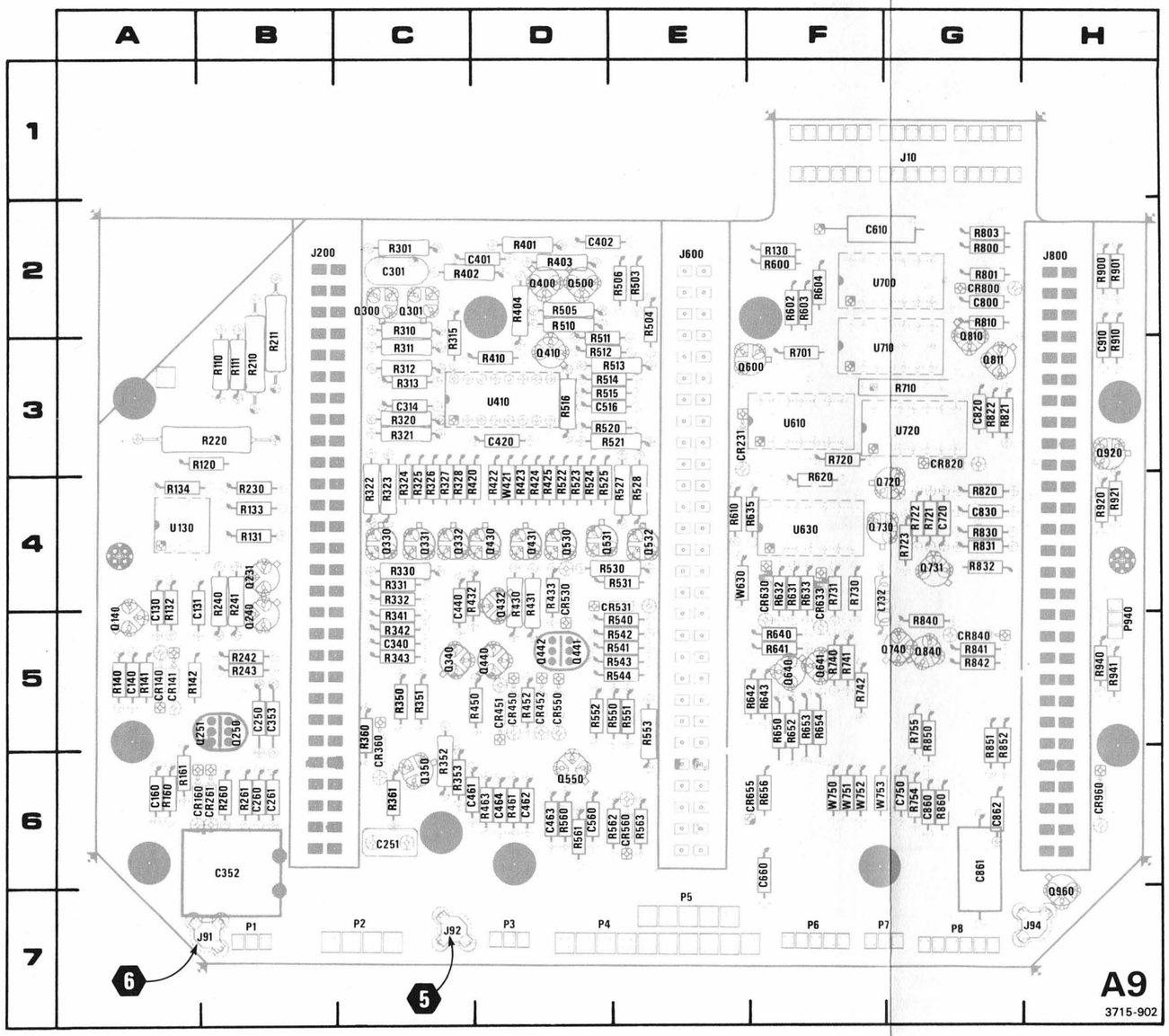


Figure 9-4. A9-Interface circuit board assembly.

Static Sensitive Devices
See Maintenance Section

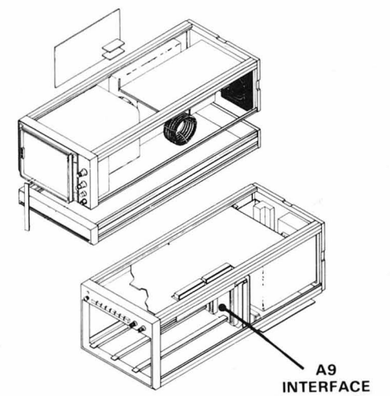
COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



A9
INTERFACE
Shown on Diag. 1 & 2

CHANNEL SWITCHING DIAGRAM ◇2

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C130	D5	A4	Q440	C1	D5	R402	D3	C2
C131	D5	A4	Q500	D3	D2	R403	D3	D2
C140	D5	A5	Q530	A2	D4	R404	D4	D2
C301	D3	C2	Q531	C1	D4	R410	C4	D3
C314	B3	C3	Q532	C2	E4	R420	B3	C4
C340	D1	C5				R422	A3	D4
C401	D3	D2	R110	E4	B3	R423	C2	D4
C402	D3	D2	R111	E3	B3	R424	B3	D4
C420	C2	D3	R132	D5	A4	R425	B3	D4
C440	D1	C4	R140	D5	A5	R430	C1	D4
C464	D1	D6	R141	D5	A5	R431	C1	D4
C516	B2	D3	R142	C5	A5	R432	C1	C4
			R210	E4	B3	R433	A2	D4
CR140	D5	A5	R211	E2	B3	R450	D1	D5
CR141	D5	A5	R220	E3	B3	R463	D1	D6
CR450	D1	D5	R240	C5	B4	R505	D3	D2
CR451	D1	D5	R241	C5	B4	R510	D2	D2
CR530	A2	D4	R301	D3	C2	R511	D2	D3
CR531	A3	E4	R310	D4	C2	R512	D2	D3
			R311	D3	C3	R513	B2	D3
J91	E5	B7	R312	B4	C3	R514	C4	D3
J92	E1	C7	R313	B3	C3	R516	B2	D3
			R315	C4	C3	R520	B2	D3
Q140	D5	A5	R320	B3	C3	R521	B3	D3
Q231	D5	B4	R321	B3	C3	R522	B2	D4
Q240	C5	B5	R322	C5	C4	R523	B2	D4
Q300	D4	C2	R323	C5	C4	R524	C1	D4
Q301	E4	C2	R324	C5	C4	R525	C1	D4
Q330	C5	C4	R325	C5	C4	R527	C1	E4
Q331	C5	C4	R326	B4	C4	R528	C1	E4
Q332	A4	C4	R327	B4	C4	R530	C1	E4
Q340	D1	C5	R328	B3	C4	R531	A2	E4
Q400	E2	D2	R330	C5	C4	R540	A3	E5
Q410	D2	D3	R331	A3	C4			
Q430	A3	D4	R332	A4	C4	U410	C3	D3
Q431	A3	D4	R343	D1	C5			
Q432	D2	D4	R401	D3	D2	W421	A3	D4

Partial A9 also shown on diagrams 1 and 12.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DL90	E3	CHASSIS	J91	E5	CHASSIS
			J92	E1	CHASSIS

VOLTAGE AND WAVEFORM CONDITIONS

Voltage Conditions. The test voltages (circled numbers) on the schematic were taken using a digital multimeter with 10 MΩ input impedance (TEKTRONIX DM501A Digital Multimeter installed in a TM501 Power Module or a TEKTRONIX 7D13 Digital Multimeter used with a readout equipped 7000-series oscilloscope).

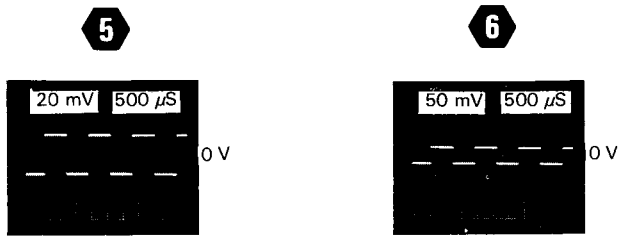
No plug-in units were installed.

Waveform Conditions. A 5B25N Digitizer Time Base/Ampl with controls set as follows: Time/Div (1 ms), Chop (In), Triggering (AC, Auto, Left) and two 5000 series vertical amplifiers with controls set as follows: Volts/Div (1V), Display (On) were installed in the appropriate compartments of the 5223. A 1 volt, 1 kHz square-wave was applied to both vertical amplifier inputs.

The 5223 controls were set as follows: Memory Contents pushbuttons—Display (both in), Vector Mode (in), Display Speed Out (fully cw). All other buttons (out).

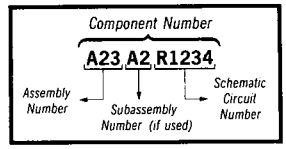
The waveforms were monitored using a test oscilloscope system with 10 MΩ input impedance, at least 60 MHz bandwidth and 10X probe (Tektronix 7603 Oscilloscope, 7B92A Time Base, 7A13 Differential Comparator and P6062B Probe).

Refer to the individual waveform photos for deflection factor and sweep rate settings.

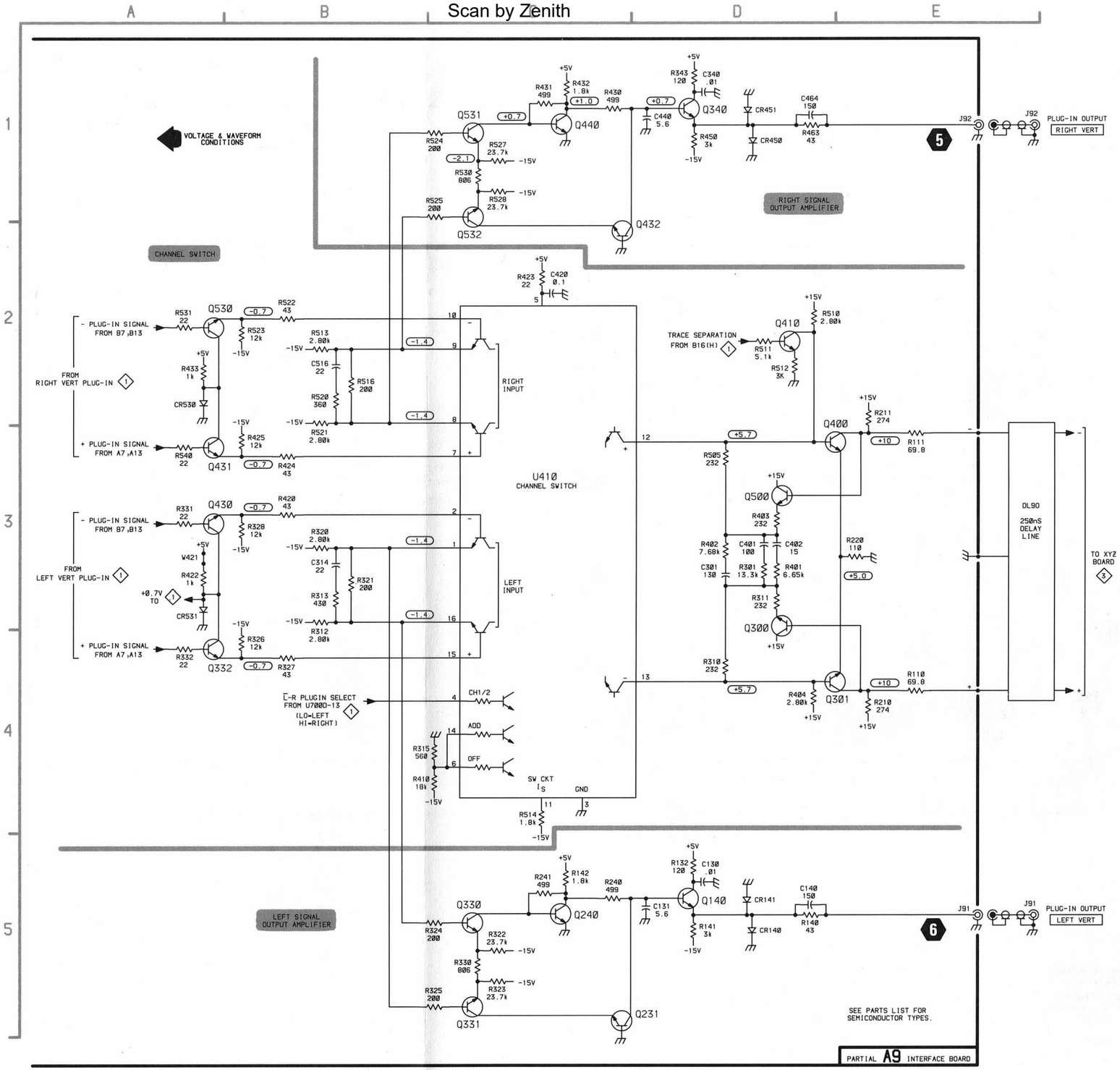


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



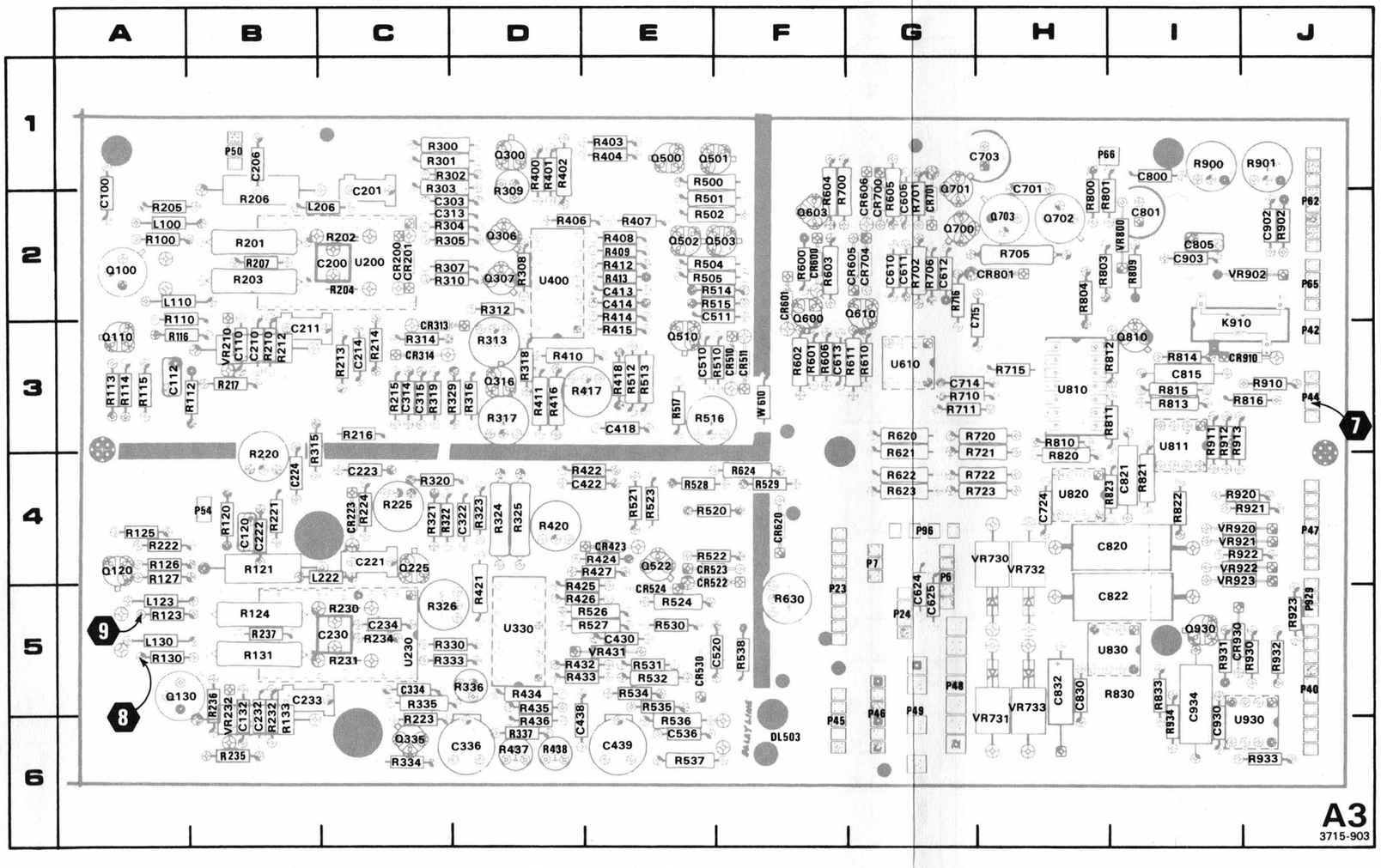
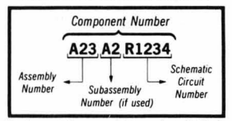


Figure 9-5. A3-XYZ circuit board assembly.

A3—XYZ
Circuit Bd Assembly

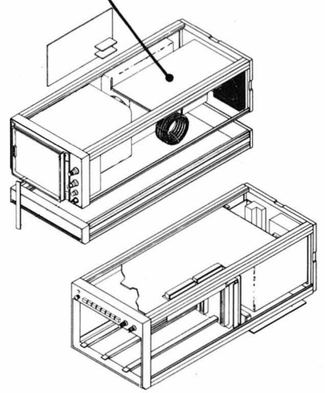
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

A3
XYZ
Shown on Diag. 3,4,5,& 12



VERTICAL AMPLIFIER DIAGRAM 3

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C132	E3	B5
C221	F5	C4
C222	E4	B4
C230	G4	C5
C232	E4	B5
C233	F2	B5
C234	G4	C5
C322	E5	D4
C334	B4	C5
C336	C4	D6
C430	D2	E5
C438	B4	D6
C439	C4	E6
C536	A4	E6
C815	C1	I3
C822	E2	I5
CR223	D5	C4
CR423	B5	E4
CR522	B5	E4
CR523	B5	E4
CR524	A2	E5
CR530	A3	E5
L123	G4	A5
L130	G3	A5
LR222	E4	C4
P23	A2	F5
P40	A5	J5
P40	A1	J5
P44	E1	J3
P45	D5	F6
P47	D1	J4
Q120	E3	A4
Q130	E3	A5
Q225	E5	C4
Q335	B4	C6
Q522	B5	E4
Q810	C1	I3
R121	F4	B4
R123	G4	A5
R124	F5	B5
R125	E3	A4
R126	E3	A4
R127	E3	A4
R130	G3	A5
R131	F2	B5
R133	F3	B5
R216	D5	C3
R222	E3	A4
R223	F5	C6
R224	D5	C4
R225	D5	C4
R230	F5	C5
R231	F2	C5
R232	E4	B5
R234	G3	C5
R235	E4	B6
R236	E4	B5
R237	E3	B5
R320	E5	C4
R322	E5	C4
R323	C5	D4
R324	C2	D4
R325	C3	D4
R326	D4	C5
R330	D4	C5
R333	D3	C5
R334	B4	C6
R335	B4	C5
R336	B4	D5
R337	B4	D6
R420	C3	D4
R421	C3	D5
R422	E5	D4
R424	B4	E4
R425	B2	D5
R426	B3	D5
R427	D5	E4
R432	C3	D5
R433	C4	D5
R434	B4	D5
R435	B3	D5
R436	B4	D6
R437	C4	D6
R438	B4	D6
R521	B5	E4
R523	B5	E4
R524	B2	E5
R526	B3	E5
R527	B2	E5
R530	A5	E5
R532	B4	E5
R534	C5	E5
R535	C5	E5
R536	A3	E6
R537	A4	E6
R538	A5	F5
R622	A2	G4
R623	A1	G4
R630	B3	F5
R722	B2	G4
R723	A1	G4
R810	B1	H3
R811	C1	H3
R812	C1	H3
R813	C1	I3
R814	B1	I3
R815	C1	I3
R816	C2	J3
R910	E2	J3
R911	D2	I3
R912	E1	I3
R920	E2	I4
R921	D1	I4
R923	B1	J5
RT531	B3	E5
U230	F3	C5
U330	D3	D5
U610B	B1	G3
U810C	C1	H3
U810D	C1	H3
U810	B1	H3
U811A	C2	I3
U811B	E1	I3
VR232	E4	B5
VR431	C5	E5
VR732	E2	H4
VR733	E2	H5
VR920	D2	I4
VR921	D2	I4

Partial A3 also shown on diagrams 4, 5, 6 and 12.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J98	F1	CHASSIS
R47A	D2	CHASSIS

VOLTAGE AND WAVEFORM CONDITIONS

Voltage Conditions. The test voltages (circled numbers) on the schematic were taken using a digital multimeter with 10 MΩ input impedance (Tektronix DM501A Digital Multimeter installed in a TM501 Power Module or a Tektronix 7D13 Digital Multimeter used with a readout equipped 7000-series oscilloscope.

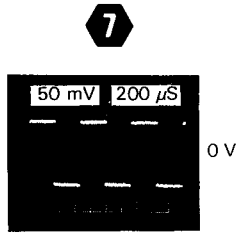
No plug-in units were installed.

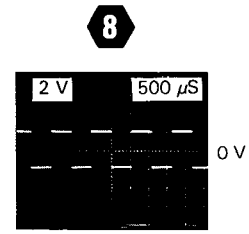
Waveform Conditions. A 5B25N Digitizer Time Base/Ampl with controls set as follows: Time/Div (1 ms), Chop (In), Triggering (AC, Auto, Left) and two 5000-series vertical amplifiers with controls set as follows: Volts/Div (1V), Display (On) were installed in the appropriate compartments of the 5223. A 1 volt, 1 kHz square wave was applied to both vertical amplifier inputs.

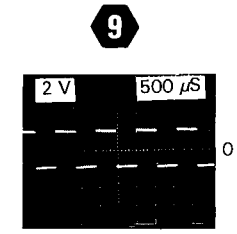
The 5223 controls were set as follows: Memory Contents pushbuttons—Display (both-in) Vector Mode (In), Display Speed Out (full cw). All other buttons (out). Waveforms 8 and 9—All Memory Contents pushbuttons (out).

The waveforms were monitored using a test oscilloscope system with 10 MΩ input impedance, at least 60 MHz bandwidth and 10X probe (Tektronix 7603 Oscilloscope, 7B92A Time Base, 7A13 Differential Comparator and P6062B Probe).

Refer to the individual waveform photos for deflection factor and sweep rate settings.

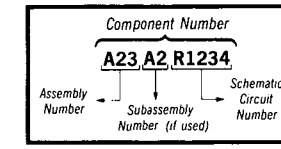




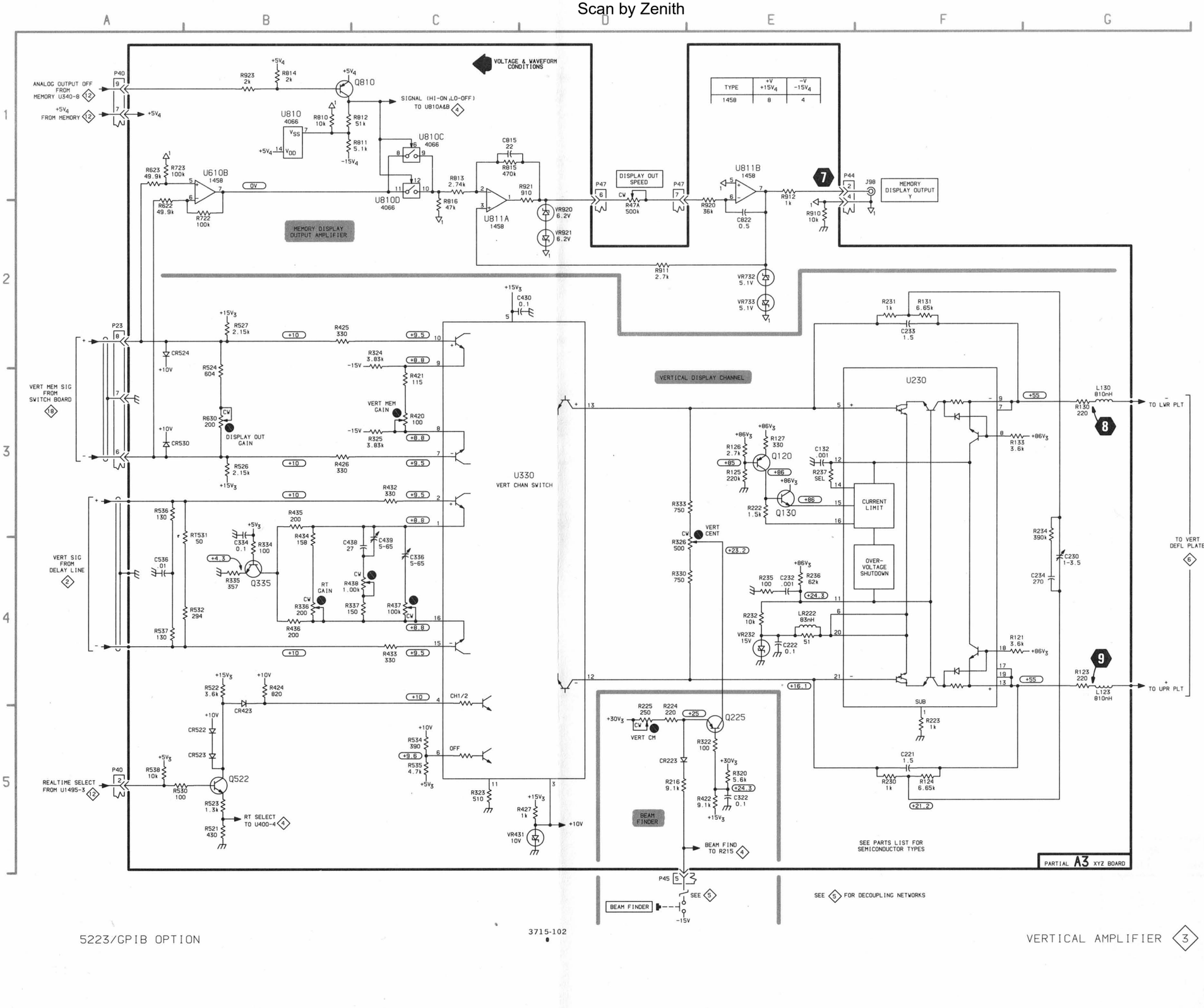


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List



5223/GPIB OPTION

3715-102

VERTICAL AMPLIFIER 3

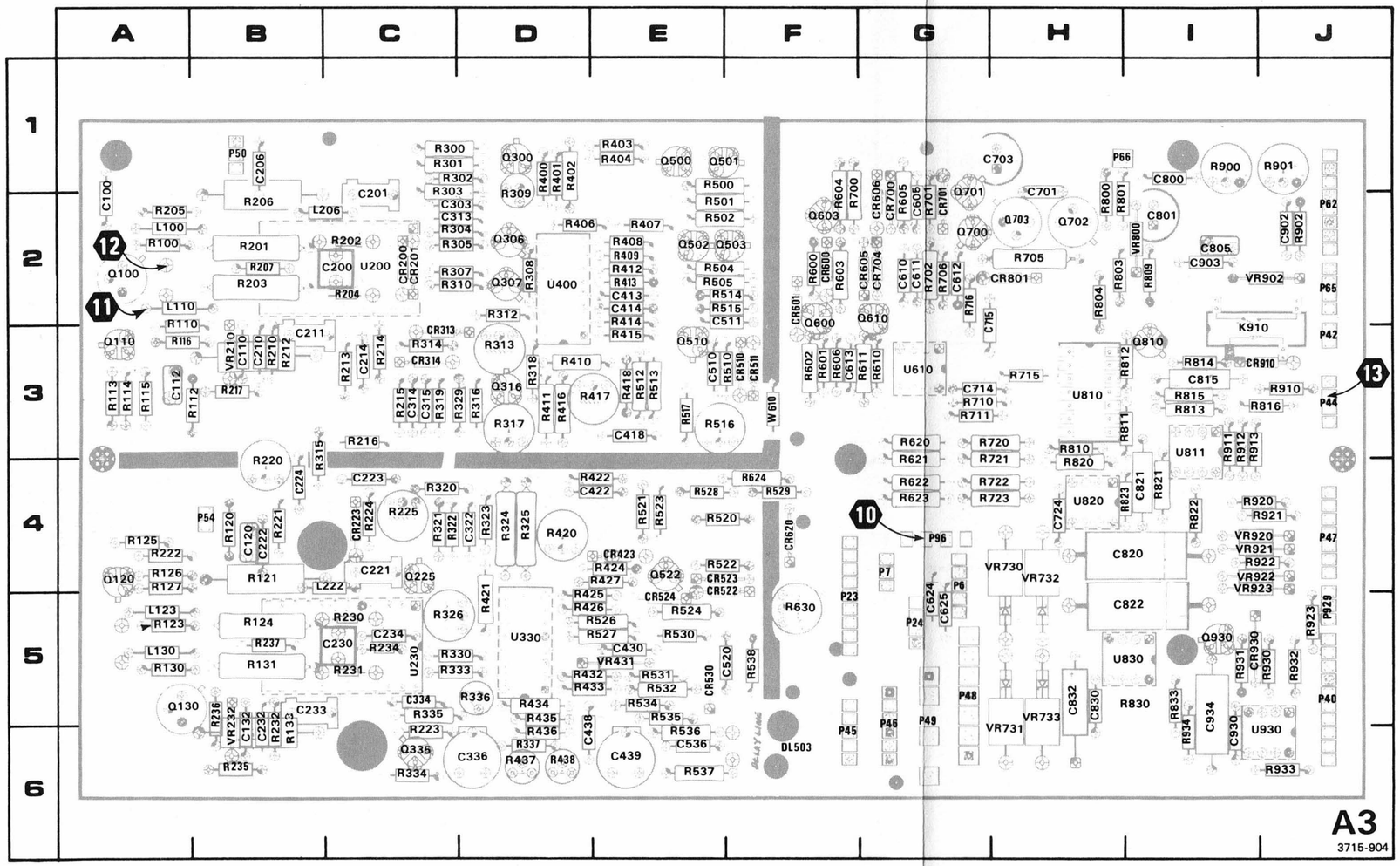


Figure 9-6. A3-XYZ circuit board assembly.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

HORIZONTAL AMPLIFIER DIAGRAM 4

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	F2	B3
C200	G3	C2
C201	F4	C1
C206	E4	B1
C210	E3	B3
C211	F2	B3
C303	B2	C2
C313	E3	C2
C315	E5	C3
C413	C2	E2
C510	E1	E3
C511	D1	E2
C820	E5	H4
C821	C5	I4
CR200	E3	C2
CR201	E3	C2
CR313	D3	C3
CR314	D4	C3
CR510	E1	F3
CR511	E1	F3
L100	G4	A2
L110	G2	A2
LR206	F3	C2
P7	A2	G4
P23	A3	F5
P44	E5	J3
P47	D5	J4
P96	E1	G4
Q100	E3	A2
Q110	E3	A3
Q300	B3	D1
Q306	E4	D2
Q307	E2	D2
Q316	E4	D3
Q500	C2	E1
Q501	C1	E1
Q502	D2	E2
Q503	D1	E2
Q510	D1	E3
R100	G4	A2
R110	G2	A2
R113	E2	A3
R114	E2	A3
R115	E3	A3
R116	F3	A3
R127	E3	A4
R201	F4	B2
R202	F4	C2
R203	F2	B2
R204	F2	C2
R205	E3	A2
R206	G4	B2
R207	F3	B2
R210	E3	B3
R212	G2	B3
R213	F4	C3
R215	D4	C3
R300	B3	C1
R301	B2	C1
R302	B2	C1
R303	B2	C1
R304	E4	C2
R305	E4	C2
R307	E2	C2
R308	D4	D2
R309	B2	D1
R310	E2	C2
R312	D2	D2
R313	D3	D3
R314	D3	C3
R315	E4	B3
R316	D4	D3
R317	D4	D3
R318	C5	D3
R319	D4	C3
R329	D5	D3
R400	B2	D1
R401	B3	D1
R402	B3	D1
R403	C1	E1
R404	C1	E1
R406	C4	D2
R407	E1	E2
R408	B2	E2
R409	B3	E2
R410	C3	D3
R411	C4	D3
R412	C4	E2
R413	C2	E2
R414	B3	E2
R415	B4	E3
R416	C4	D3
R417	C3	D3
R500	C1	E1
R501	C1	E2
R502	C1	E2
R504	C1	E2
R505	D1	E2
R510	E1	F3
R512	B3	E3
R513	B4	E3
R514	D1	E2
R515	D1	E2
R516	B3	E3
R517	D1	E3
R528	B4	E4
R529	B3	F4
R620	B5	G3
R621	B5	G3
R624	B4	F4
R715	C5	H3
R720	B5	G3
R721	B5	G3
R820	C5	H4
R821	C5	I4
R822	C5	I4
R823	D5	H4
R913	E5	I3
R922	E5	I4
U200	F2	C2
U400	C2	D2
U610A	B5	G3
U810A	C5	H3
U810B	C5	H3
U820A	C5	H4
U820B	E5	H4
VR210	E4	B3
VR730	E5	H4
VR731	E5	H6
VR922	D5	I4
VR923	D5	I4

Partial A3 also shown on diagrams 3, 5, 6 and 12.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J93	F1	CHASSIS
J97	F5	CHASSIS
R47B	D5	CHASSIS

VOLTAGE AND WAVEFORM CONDITIONS

Voltage Conditions. The test voltages (circled numbers) on the schematic were taken using a digital multimeter with 10 MΩ input impedance (TEKTRONIX DM501A Digital Multimeter installed in a TM501 Power Module or a TEKTRONIX 7D13 Digital Multimeter used with a readout equipped 7000-series oscilloscope).

No plug-in units were installed.

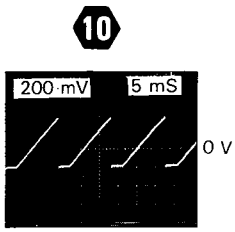
Waveform Conditions. A 5B25N Digitizer Time Base/Ampl with controls set as follows: Time/Div (1 ms), Chop (In), Triggering (AC, Auto, Left) was installed in the horizontal plug-in compartment of the 5223.

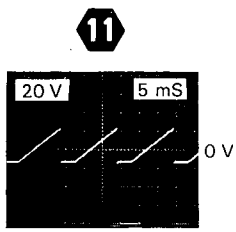
For waveform 11, Slope (-).

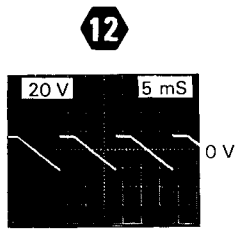
For waveform 12, Slope (+).

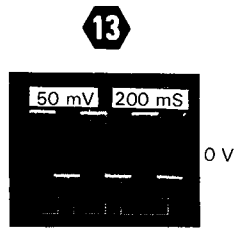
The 5223 controls were set as follows: Memory Contents pushbuttons—Display (both in), Vector Mode (in), Display Speed Out (full cw). All other buttons (out).

The waveforms were monitored using a test oscilloscope system with 10 MΩ input impedance, at least 60 MHz bandwidth and 10X probe (TEKTRONIX 7603 Oscilloscope, 7B92A Time Base, 7A13 Differential Comparator and P6062B Probe. Refer to the individual waveform photos for deflection factor and sweep rate settings.



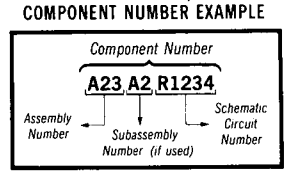






Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

VOLTAGE & WAVEFORM CONDITIONS

HORIZONTAL SIGNAL OUTPUT AMPLIFIER

HORIZONTAL DISPLAY CHANNEL

MEMORY DISPLAY OUTPUT AMPLIFIER

HORIZ INPUT FROM INTERFACE 1

HORIZ MEMORY SIGNAL FROM SWITCH BOARD 18

FROM P23 18

RT SELECT FROM Q521 3

BEAM FIND FROM P45-5 3

SIGNAL (HI-ON, LO-OFF) FROM Q810 3

PLUG-IN OUTPUT HORIZ

TO RIGHT PLT

TO LEFT PLT

TO HORIZ DEFL PLTS 6

MEMORY DISPLAY OUTPUT X

PARTIAL A3 XYZ BOARD

SEE 5 FOR DECOUPLING NETWORKS

TYPE	+V +15V4	-V -15V4
1458	8	4

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

5223/GPIB OPTION

3715-103

HORIZONTAL AMPLIFIER 4

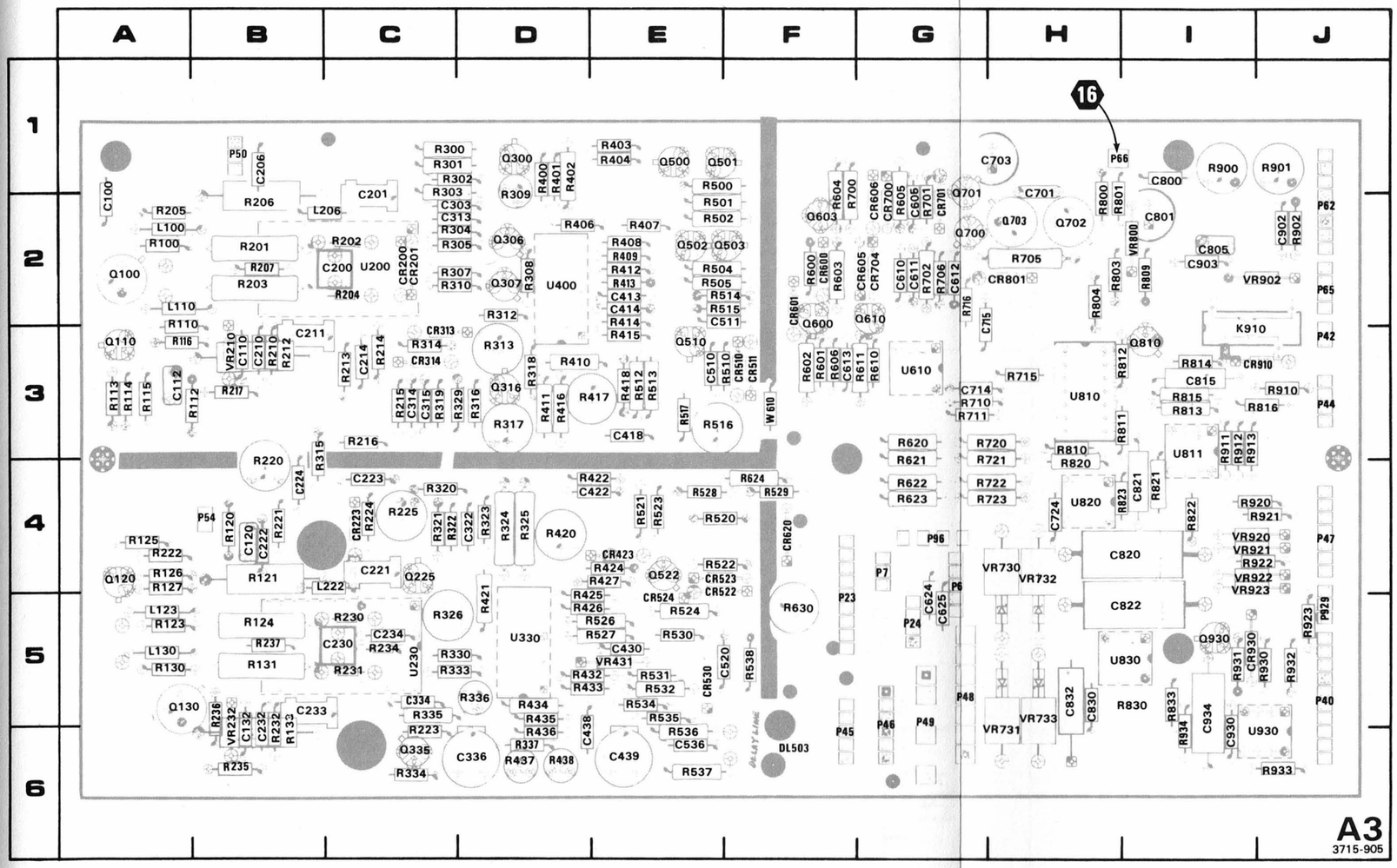


Figure 9-7. A3-XYZ circuit board assembly.

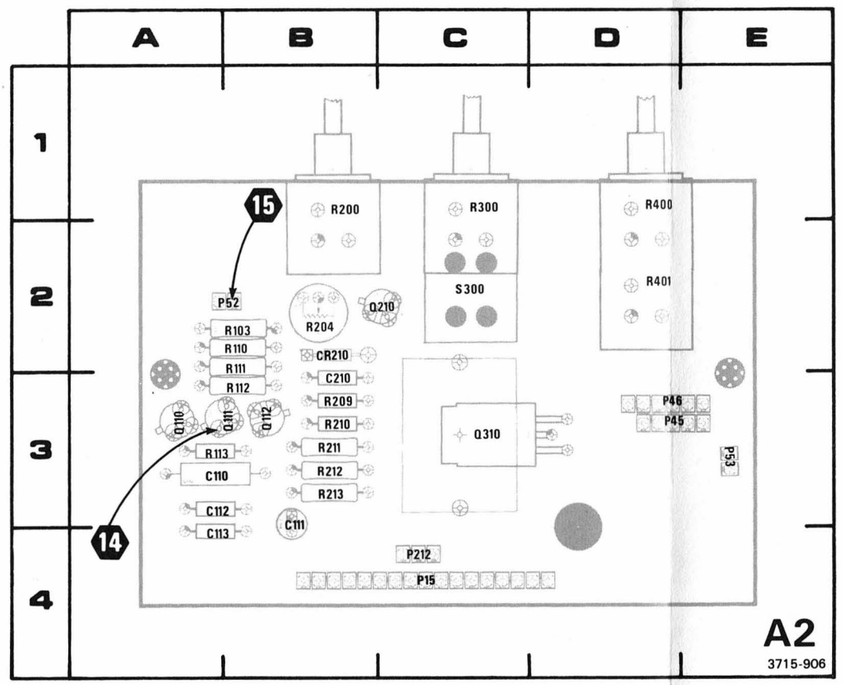
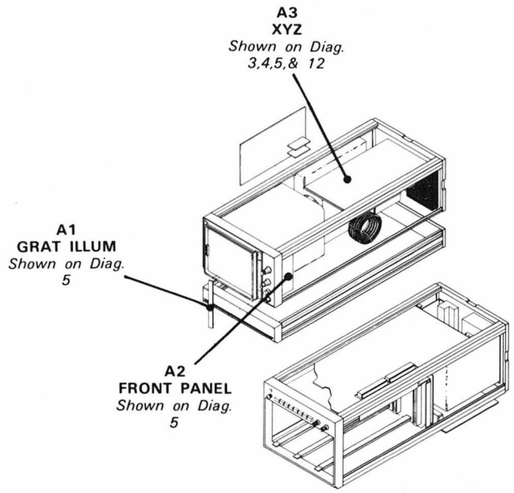
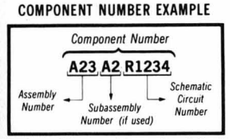


Figure 9-8. A1-Graticule Illum circuit board assembly.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

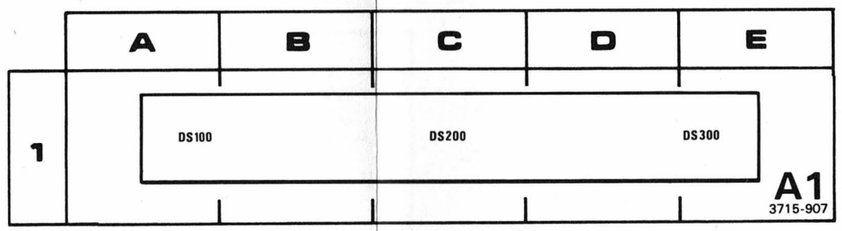
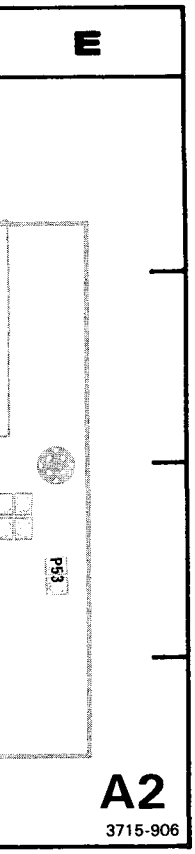


Figure 9-9. A2-Front Panel circuit board assembly.



Z-AXIS AMPLIFIER AND FRONT PANEL DIAGRAM 5

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DS100	C2	A1	DS200	C2	C1	DS300	C2	E1

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	A1	A3	P212	A5	C4	R200	A2	B1
C111	A1	B4				R204	A1	B2
C112	B4	A3	Q110	B1	A3	R209	A2	B3
C113	B3	A4	Q111	B1	B3	R210	B2	B3
C210	B4	B3	Q112	A1	B3	R211	A1	B3
			Q210	B2	C2	R212	B1	B3
CR210	B2	B2	Q310	B2	C3	R213	A1	B3
						R300	A3	C1
P15	A5	C4	R103	B1	B2	R400	A3	D1
P45	B3	D3	R110	A1	B2	R401	A3	D2
P46	B4	D3	R111	A1	B2			
P52	B1	B2	R112	B1	B3	S300	B3	C2
P53	B2	E3	R113	B1	A3			

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	E4	A2	CR605	E2	G2	R214	D4	C3
C112	D4	A3	CR606	E2	G2	R321	E4	C4
C120	E4	B4	CR620	E2	F4	R418	D4	E3
C214	D4	C3	CR700	E2	G2	R520	E4	E4
C223	E4	C4	CR701	E1	G2	R600	E1	F2
C224	E4	B4	CR704	E2	G2	R601	D1	F3
C314	E3	C3	CR801	F1	H2	R602	D1	F3
C414	D4	E2				R603	E1	F2
C418	E4	E3	P6	D2	G4	R604	E1	F2
C422	E4	D4	P24	F5	G5	R605	E2	G2
C520	E4	E5	P44	D3	J3	R606	E2	F3
C605	E1	G2	P45	D3	F6	R610	D2	G3
C610	D4	G2	P46	C4	G5	R611	D2	G3
C611	C4	G2	P48	C4	G5	R700	E2	F2
C612	D4	G2	P49	C5	G5	R701	F1	G2
C613	D3	F3	P50	D2	B1	R702	F2	G2
C624	D3	G5	P62	F3	J2	R705	F2	H2
C625	D3	G5	P66	F1	H1	R706	F1	G2
C701	F1	H1	P96	D1	G4	R710	F4	G3
C703	F2	H1				R711	F4	G3
C714	F4	G3	Q600	E1	F2	R716	E1	G2
C715	D1	G2	Q603	E1	F2	R800	F1	H2
C724	F4	H4	Q610	E2	G2	R801	F1	H2
C800	D4	I1	Q700	F2	G2	R803	F1	H2
C801	F1	I2	Q701	E2	G1	R804	F1	H2
C805	C4	I2	Q702	F1	H2	R809	F4	I2
C903	C4	I2	Q703	F1	H2			
						VR800	F4	I2
CR600	D1	F2	R112	D4	A3			
CR601	D1	F2	R120	E4	B4			

Partial A3 also shown on diagrams 3, 4, 6 and 12.

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION			
P15	B5	B1			

Partial A11 also shown on diagrams 1, 8, 9, 10, 11, 12, 13, 14, 15, 16, and 17.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C52	B1	CHASSIS	J52	B1	CHASSIS	P50	D2	CHASSIS
			J95	D3	CHASSIS			
J50	D2	CHASSIS	J96	D1	CHASSIS			

VOLTAGE AND WAVEFORM CONDITIONS

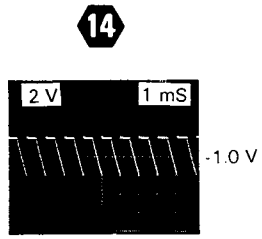
Voltage Conditions. The test voltages (circled numbers) on the schematic were taken using a digital multimeter with 10 MΩ input impedance (TEKTRONIX DM501A Digital Multimeter installed in a TM501 Power Module or a TEKTRONIX 7D13 Digital Multimeter used with a readout equipped 7000-series oscilloscope).

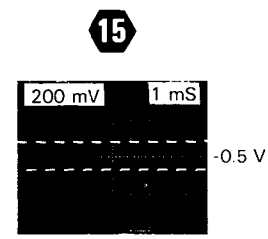
No plug-in units were installed.

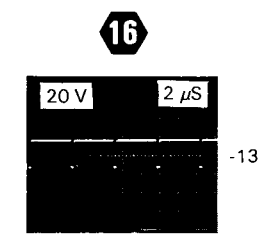
Waveform Conditions. A 5B25N Digitzer Time Base/Ampl with controls set as follows: Time/Div (1 ms), Chop (In), Triggering (AC, Auto, Left) was installed in the horizontal plug-in compartment of the 5223. For waveform 16, the INTENSITY was set approx. 3/4 turn clockwise, and either Display pushbutton pressed.

The waveforms were monitored using a test oscilloscope system with 10 MΩ input impedance, at least 60 MHz bandwidth and 10X probe (TEKTRONIX 7603 oscilloscope, 7B92A Time Base, 7A13 Differential Comparator and P6062B probe).

Refer to the individual waveform photos for deflection factor and sweep rate settings.

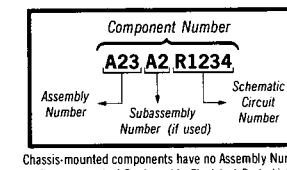




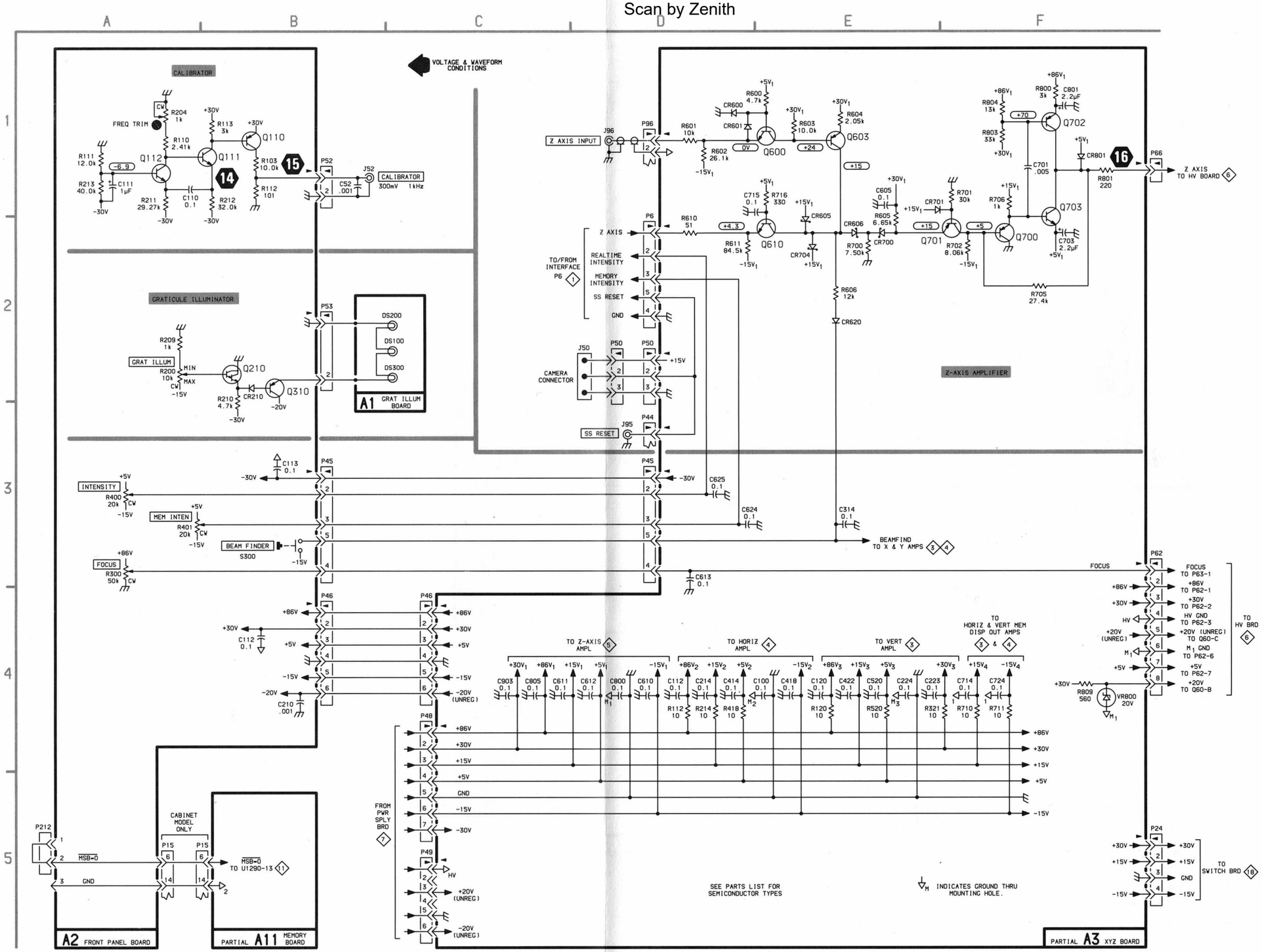


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



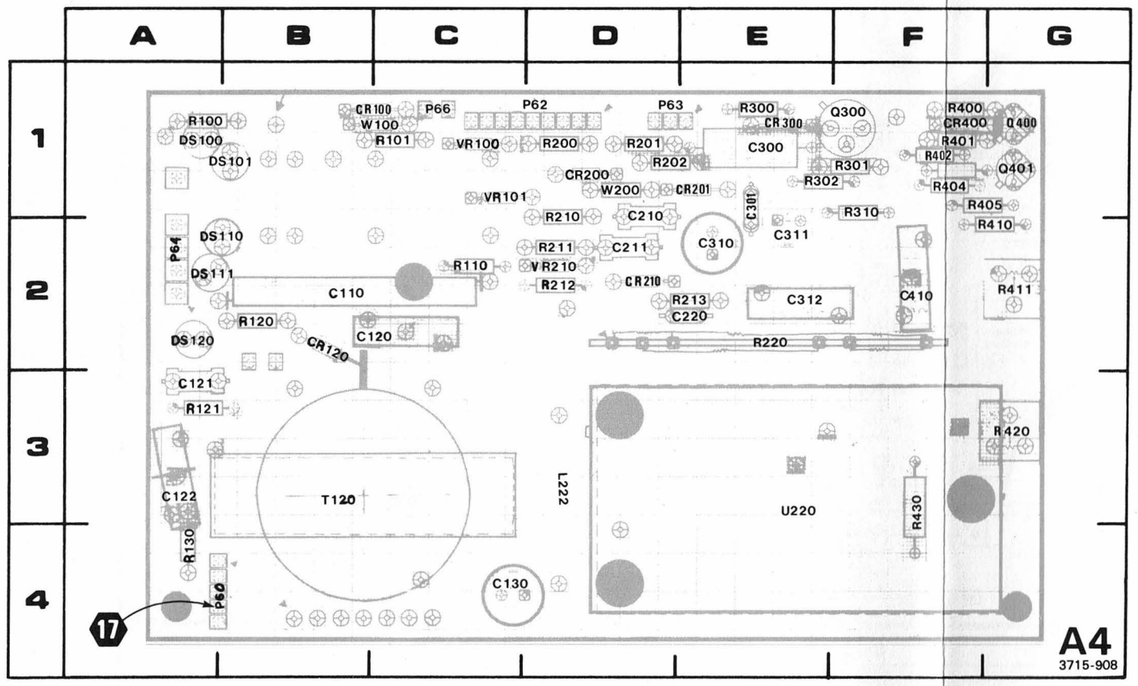


Figure 9-10. A4-High Voltage circuit board assembly.

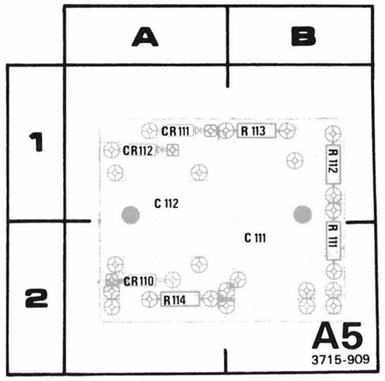


Figure 9-11. A5-Focus DC Restorer circuit board assembly.

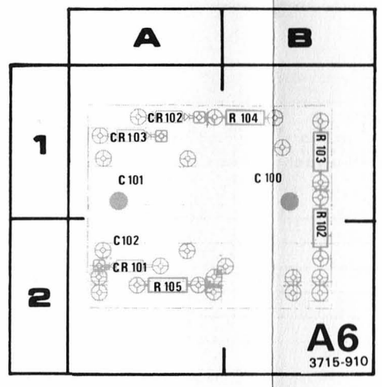
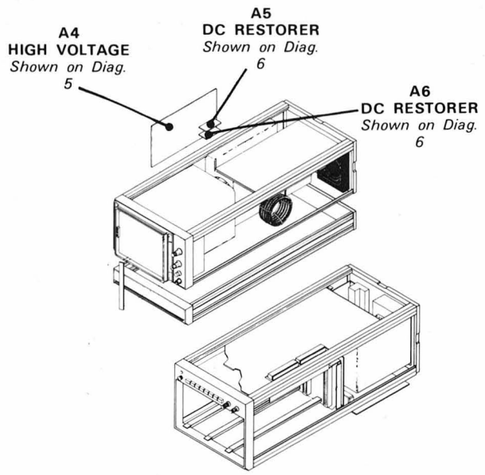
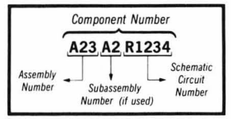


Figure 9-12. A6-Z-Axis DC Restorer circuit board assembly.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

CRT CIRCUIT DIAGRAM 6

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C902	F3	J2	R220	F1	B3	R902	F2	J2
			R221	F1	B4			
P54	F1	B4	R900	F3	I1	VR902	F2	J2
P65	F2	J2	R901	F3	J1			

Partial A3 also shown on diagrams 3, 4, 5 and 12.

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	D1	B2	DS120	D4	B2	R220A	D2	E2
C120	D1	C2				R220B	D2	E2
C121	D4	A3	L222	A1	D3	R220C	D3	E2
C122	D4	A3				R220D	D3	E2
C130	A1	C4	P60	A1	B4	R300	B2	E1
C210	C3	D2	P62	A3	D1	R301	B2	F1
C211	C3	D2	P62	A1	D1	R302	B2	E1
C220	C2	E2	P63	A3	D1	R310	B4	F1
C300	B3	E1	P66	A4	C1	R400	B2	F1
C301	B2	E1				R401	B2	F1
C310	C2	E2	Q300	B2	F1	R404	B2	F1
C311	C4	E2	Q400	B2	G1	R405	B2	F1
C312	D3	E2	Q401	C2	G1	R410	C2	G2
C410	D2	F2				R411	B4	G2
			R100	D4	A1	R420	D3	G3
CR100	B4	C1	R101	B3	C1	R430	D3	F3
CR120	C1	B2	R110	D1	C2			
CR200	B3	D1	R120	D1	B2	T120	B1	B3
CR201	D2	E1	R121	D4	A3			
CR210	C4	D2	R130	D4	A4	VR100	B3	C1
CR300	B2	E1	R200	C3	D1	VR101	C3	C1
CR400	B2	F1	R201	B3	D1	VR210	C4	D2
			R202	D2	D1			
DS100	D4	A1	R210	C3	D1	W100	B3	C1
DS101	D4	B1	R211	C3	D2	W200	D2	D1
DS110	D4	B2	R212	C4	D2			
DS111	D4	A2	R213	D2	E2			

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C111	D3	B2	CR111	D3	A1	R112	D3	B1
C112	C3	A1	CR112	D3	A1	R113	D3	B1
						R114	C3	A2
CR110	C3	A2	R111	D3	B2			

ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	D4	B1	CR101	C4	A2	R102	D4	B1
C101	C4	A1	CR102	D4	A1	R103	D4	B1
C102	C4	A2	CR103	D4	A1	R104	D4	B1
						R105	C4	A2

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L51	F1	CHASSIS	Q62	A2	CHASSIS	V51	F1	CHASSIS
Q60	A1	CHASSIS	R300	A3	CHASSIS			

VOLTAGE AND WAVEFORM CONDITIONS

Voltage Conditions. The test voltages (circled numbers) on the schematic were taken using a digital multimeter with 10 MΩ input impedance (Tektronix DM501A Digital Multimeter installed in a TM501 Power Module or a Tektronix 7D13 Digital Multimeter used with a readout equipped 7000-series oscilloscope). The voltages on the crt were taken with a high voltage probe compatible with the digital multimeter described above.

Waveform Conditions. A 5B25N Digitizer Time Base/Ampl with controls set as follows: Time/Div (1 ms), Chop (In), Triggering (AC, Auto, Left) was installed in the horizontal plug-in compartment of the 5223.

The waveforms were monitored using a test oscilloscope system with 10 MΩ input impedance, at least 60 MHz bandwidth and 10X probe (Tektronix 7603 Oscilloscope, 7B92A Time Base, 7A13 Differential Comparator and P6062B Probe).

Refer to waveform photo for deflection factor and sweep rate setting.

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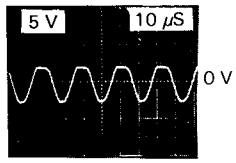
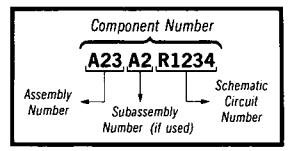
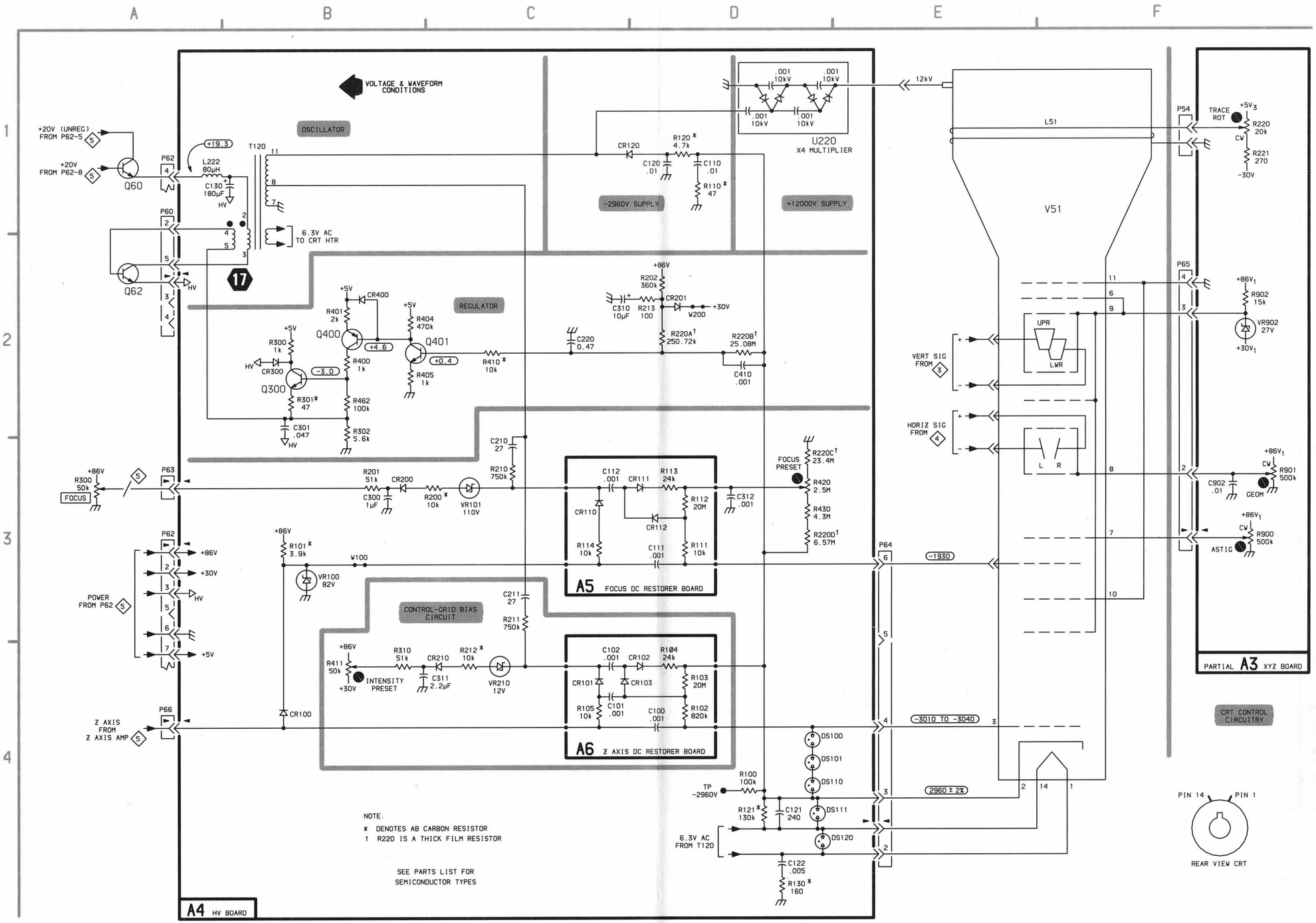


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



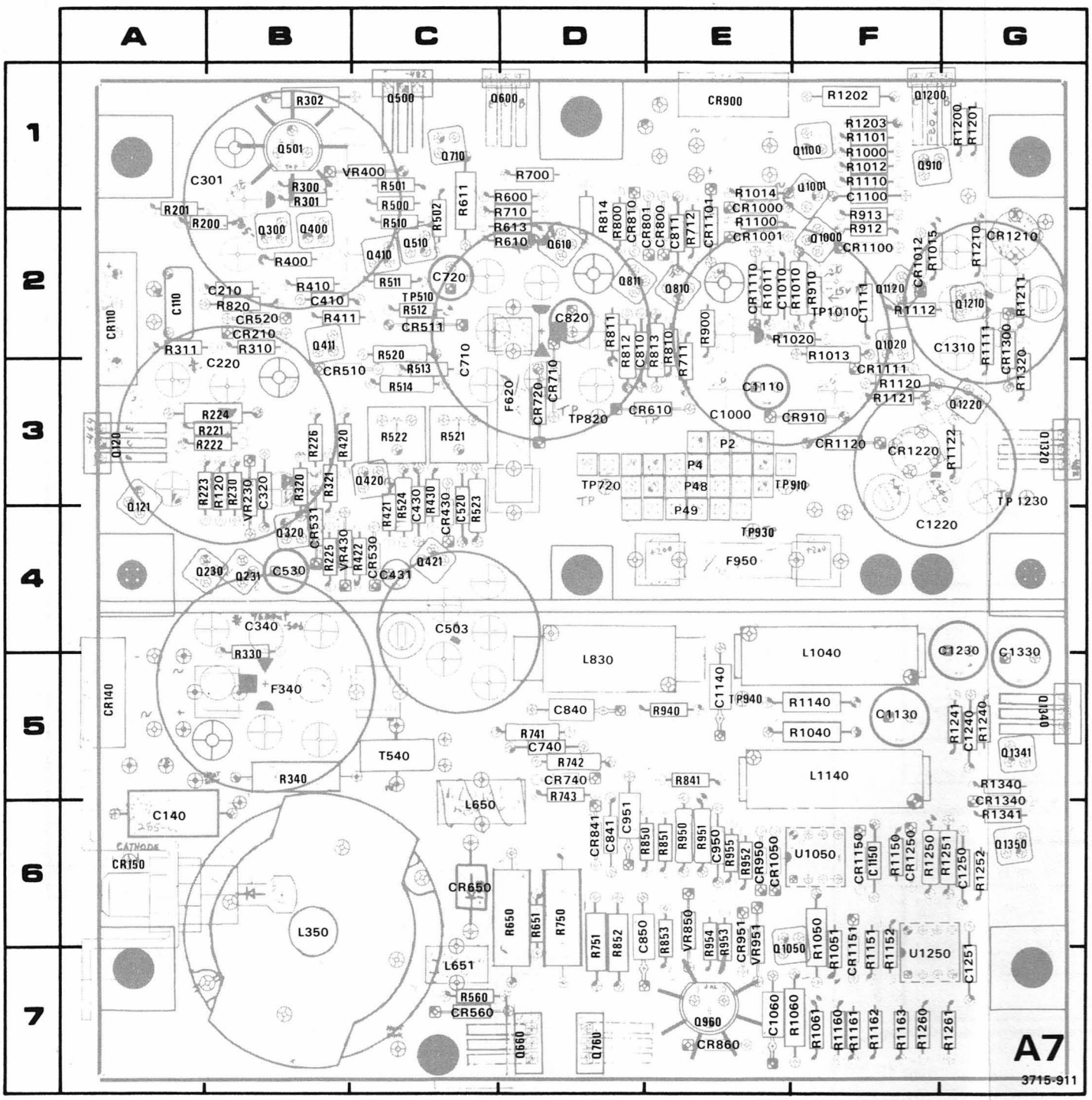


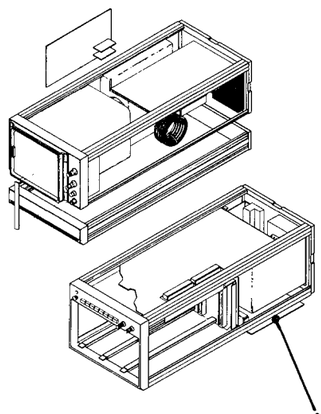
Figure 9-13. A7-Power Supply circuit board assembly.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



A7
POWER SUPPLY
Shown on Diag. 7

LV POWER SUPPLY DIAGRAM 7

ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	B3	A2	CR511	G2	C2	P4	G2	E3	R224	G4	B3	R750	E4	D6	R1150	D5	F6
C140	E5	A6	CR520	F2	B2	P48	G4	E3	R225	F3	B4	R751	E4	D7	R1151	D4	F6
C210	C3	B2	CR530	G3	C4	P49	G5	E4	R226	C3	B3	R800	D3	D2	R1152	D5	F6
C220	C3	B3	CR531	G3	B4				R230	G3	B3	R810	D2	E2	R1160	F4	F7
C301	C2	A1	CR560	E5	C7	Q120	G3	A3	R300	F2	B1	R811	D2	D2	R1161	D5	F7
C320	F3	B3	CR610	E2	D3	Q121	F4	A4	R301	F2	B1	R812	C2	D2	R1162	D5	F7
C340	C4	B4	CR650	E5	C6	Q230	F3	B4	R302	G2	B1	R813	C2	E2	R1163	D5	F7
C410	F2	B2	CR710	E2	D3	Q231	F3	B4	R310	C3	B2	R814	D2	D2	R1200	E3	G1
C430	F3	C4	CR720	G2	D3	Q300	F2	B2	R311	C3	A2	R820	C4	B2	R1201	E3	G1
C431	F3	C4	CR740	E4	D5	Q320	F4	B4	R320	F4	B3	R841	E5	E5	R1202	E3	F1
C503	E5	C4	CR800	D2	E2	Q400	F2	B2	R321	F3	B3	R850	C4	E6	R1203	D3	F1
C520	F3	C4	CR801	D2	D2	Q410	F2	C2	R330	C4	B5	R851	C4	E6	R1210	C1	G2
C530	G3	B4	CR810	D2	D2	Q411	F2	B2	R340	E5	B5	R852	E5	D7	R1211	D1	G2
C710	C2	C3	CR841	D4	D6	Q420	F3	C3	R400	F2	B2	R853	E4	E6	R1241	E5	G5
C720	G2	C2	CR860	E4	E7	Q421	F3	C4	R410	F2	B2	R900	C3	E2	R1250	C5	F6
C740	E4	D5	CR900	C2	E1	Q500	G2	C1	R411	F2	B2	R910	D3	F2	R1251	C5	G6
C810	D2	D2	CR910	G3	F3	Q501	G2	B1	R420	F3	B3	R912	E3	F2	R1252	D5	G6
C811	D2	E2	CR950	C4	E6	Q510	F2	C2	R421	F3	C4	R913	E3	F2	R1260	D5	F7
C820	E2	D2	CR951	D4	E6	Q600	E2	D1	R422	F3	C4	R940	E5	E5	R1261	D5	G7
C840	E5	D5	CR1000	D3	E2	Q610	E2	D2	R430	F3	C4	R950	C5	E6	R1320	D1	G3
C841	E4	D6	CR1001	D3	E2	Q610	D2	D2	R500	G2	C1	R951	C4	E6	R1340	E5	G5
C850	E4	D7	CR1012	D1	F2	Q660	E4	D7	R501	G2	C1	R952	C4	E6	R1341	E5	G6
C950	C4	E6	CR1050	D5	E6	Q710	E2	C1	R502	E2	C2	R953	D4	E6			
C951	G4	D6	CR1100	D3	F2	Q760	E4	D7	R510	F2	C2	R954	C5	E6	T540	E4	C5
C1000	C3	E3	CR1101	E3	E2	Q810	D2	E2	R511	F2	C2	R1000	D3	F1			
C1010	D3	E2	CR1110	E3	E2	Q811	D2	D2	R512	F2	C2	R1010	C3	E2	TP510	G2	C2
C1060	F4	E7	CR1111	D1	F3	Q910	D3	F1	R513	F2	C3	R1011	C3	E2	TP720	C1	D3
C1100	D3	F1	CR1120	E1	F3	Q960	E5	E7	R514	G2	C3	R1012	D3	F1	TP910	G3	F3
C1110	E3	E3	CR1151	D5	F6	Q1000	D3	F2	R520	G2	C2	R1013	D1	F2	TP930	F5	E4
C1111	D1	F2	CR1210	B1	G2	Q1001	D3	F1	R521	G3	C3	R1014	D3	E1	TP940	F5	E5
C1130	F5	F5	CR1220	B1	F3	Q1001	D3	F1	R522	G2	C3	R1015	D1	F2	TP1010	E3	F2
C1140	E5	E5	CR1250	D5	F6	Q1020	D1	F2	R523	G3	C4	R1020	D1	E2	TP1010	E2	F2
C1150	D5	F6	CR1300	D1	G2	Q1050	D5	E7	R524	G3	C4	R1040	F5	F5	TP1230	E1	G3
C1220	C1	F4	CR1340	E5	G6	Q1120	D1	F2	R560	E5	C7	R1050	D4	F6			
C1230	F5	G5				Q1200	E3	F1	R600	E2	D1	R1051	F4	F6	U1050A	C5	F6
C1240	E5	G5	F340	C4	B5	Q1210	D1	G2	R610	D2	D2	R1060	E5	F7	U1050B	D5	F6
C1250	C5	G6	F620	E2	D3	Q1220	D1	G3	R611	E2	C1	R1061	F4	F7	U1050	F4	F6
C1251	D5	G7	F950	C1	E4	Q1320	D1	G3	R613	E2	D2	R1100	D3	E2	U1250A	D5	F7
C1310	C1	G2				Q1340	E5	G5	R650	E4	D6	R1100	D3	E2	U1250B	D4	F7
C1330	E1	G5	L350	E5	B6	Q1341	E5	G5	R651	E4	D6	R1101	D3	F1	U1250	F4	F7
			L650	E5	C6	Q1350	D5	G6	R700	C2	D1	R1110	D3	F1			
CR110	C2	A2	L651	E5	C7				R710	D2	D2	R1111	D1	G2	VR230	F3	B3
CR140	B4	A5	L830	E5	D5	R200	C2	A2	R711	D2	E3	R1112	D1	F2	VR400	F2	C1
CR150	F5	A6	L1040	F5	F5	R201	B4	A2	R712	D2	E2	R1120	D1	F3	VR430	F3	B4
CR210	F2	B2	L1140	F5	F5	R221	G3	B3	R741	E4	D5	R1121	D1	F3	VR850	F4	E6
CR430	F3	C4				R222	F3	B3	R742	E4	D5	R1122	C1	G3	VR951	C5	E6
CR510	F2	B3	P2	G1	E3	R223	G3	A3	R743	D4	D5	R1140	F5	F5			

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P160	A5	A5	R150	A5	A5

Partial A10 also shown on diagrams 10, 12, 17 and 18.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
B25	B3	CHASSIS	F20	A4	CHASSIS	F32	B2	CHASSIS	FL20	A4	CHASSIS	S21	A3	CHASSIS
			F26	B1	CHASSIS	F33	B3	CHASSIS				S22	B3	CHASSIS
DS22	A5	CHASSIS	F28	B1	CHASSIS	F34	B3	CHASSIS	J20	A4	CHASSIS			
			F30	B2	CHASSIS							T25	B1	CHASSIS

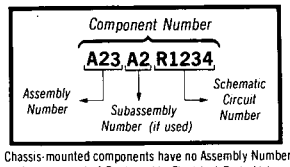
VOLTAGE CONDITIONS

Voltage Conditions. The test voltages (circled numbers) on the schematic were taken using a digital multimeter with 10 MΩ input impedance (TEKTRONIX DM501A Digital Multimeter installed in a TM501 Power Module or a TEKTRONIX 7D13 Digital Multimeter used with a readout equipped 7000-series oscilloscope).

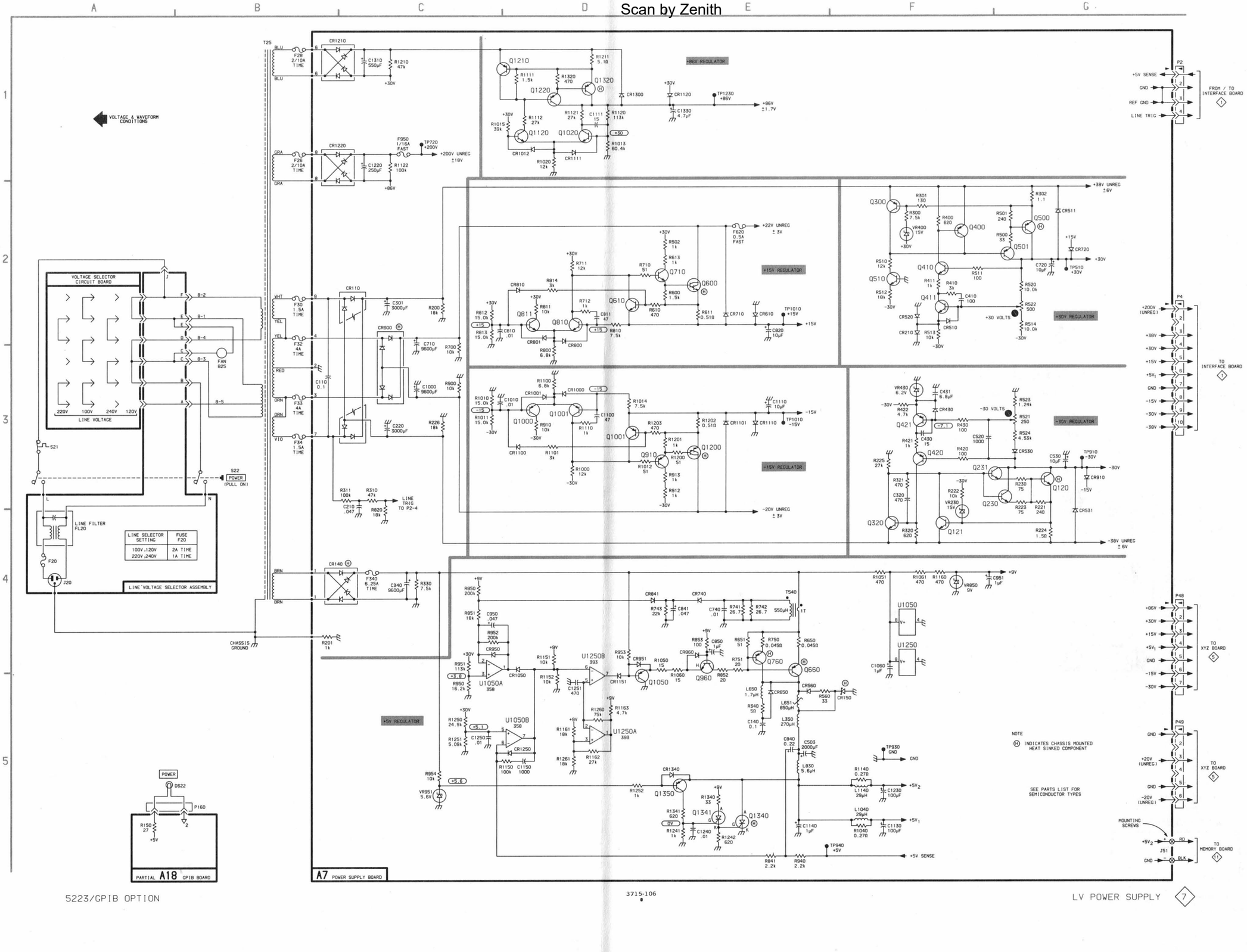
No plug-in units were installed.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



5223/GPIB OPTION

LV POWER SUPPLY 7

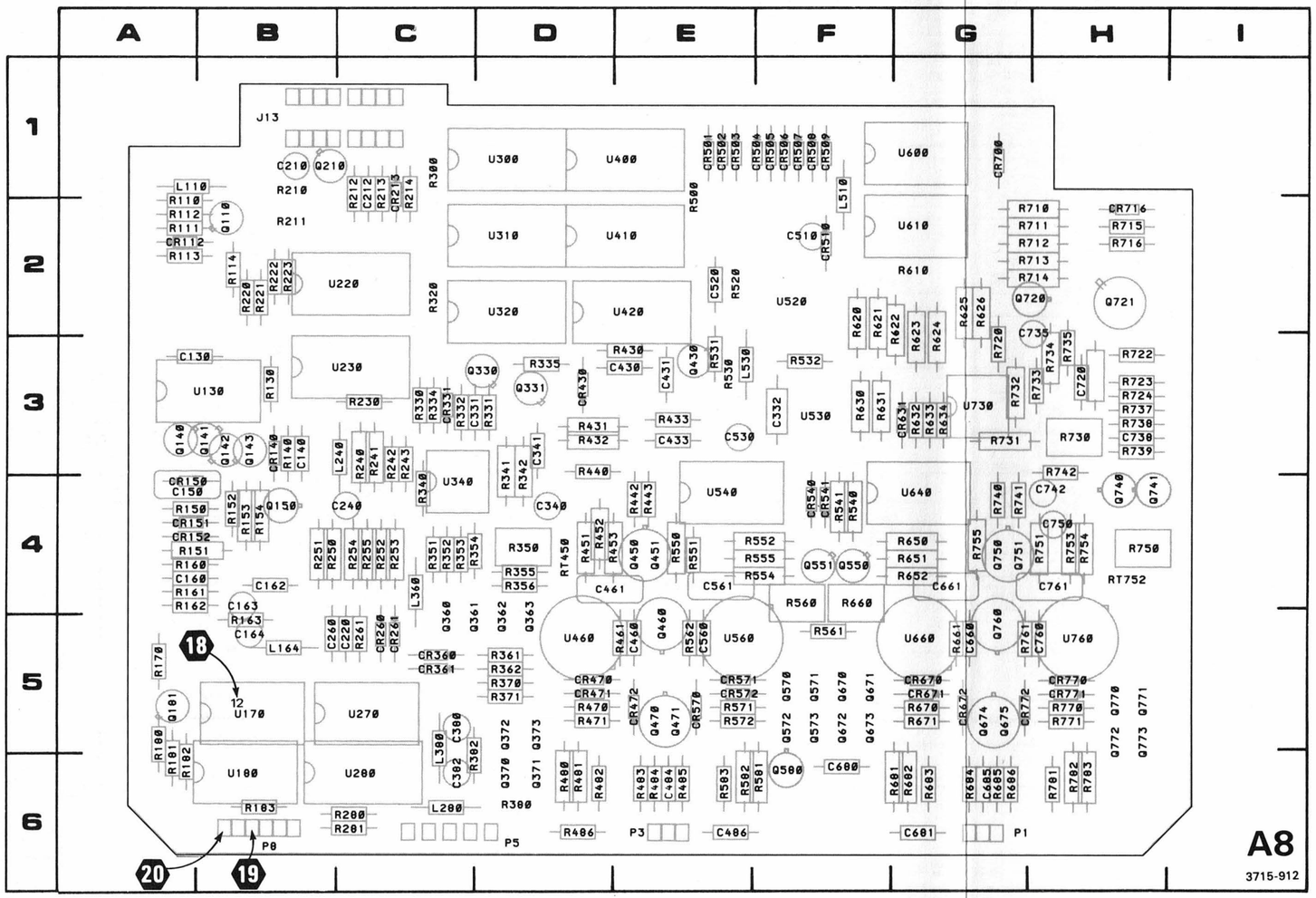
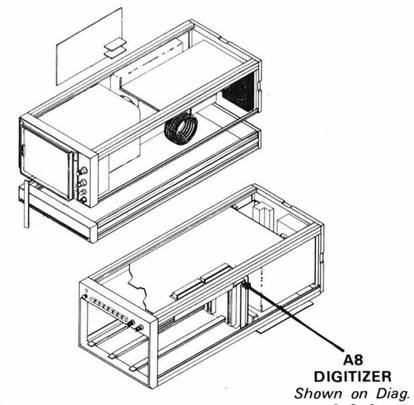


Figure 9-14. A8-Digitizer circuit board assembly.



A8—Digitizer Circuit Bd Assembly

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

DIGITIZER SAMPLER DIAGRAM 8

ASSEMBLY A8

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C460	E3	E5	Q451	F4	E4	R356	C2	D4	R684	C6	G6
C461	E3	E4	Q460A	F3	E5	R361	D2	D5	R685	C6	G6
C484	C3	E6	Q460B	F4	E5	R362	D1	D5	R686	C6	G6
C560	E4	E5	Q470	C3	E5	R370	D2	D5	R740	F5	G4
C561	E4	E4	Q471	C4	E5	R371	D3	D5	R741	F6	G4
C660	E5	G5	Q550	F6	F4	R440	F3	D3	R742	F6	H3
C661	E5	G4	Q551	F3	F4	R442	F3	E4	R750	F6	H4
C685	C6	G6	Q570	D4	F5	R443	F4	E4	R751	F6	H4
C760	E6	H5	Q571	D4	F5	R451	F4	D4	R753	F6	H4
C761	E6	H4	Q572	D4	F5	R452	F3	D4	R754	F6	H4
			Q573	D4	F5	R453	F3	E4	R755	F5	G4
CR260	F1	C5	Q670	D5	F5	R461	E3	E5	R761	E6	H5
CR261	F1	C5	Q671	D5	F5	R470	E3	D5	R770	E6	H5
CR360	C2	C5	Q672	D5	F5	R471	D3	D5	R771	D6	H5
CR361	C2	C5	Q673	D5	F5	R480	D2	D6	R781	C6	H6
CR470	E3	D5	Q674	C6	G5	R481	D3	D6	R782	D6	H6
CR471	D3	D5	Q675	C6	G5	R482	C3	D6	R783	D6	H6
CR472	D3	E5	Q750	F5	G4	R483	C3	E6			
CR540	G4	F4	Q751	F6	G4	R484	C3	E6	RT450	F4	D4
CR541	G5	F4	Q760A	F5	G5	R485	C4	E6	RT752	F6	H4
CR570	D3	E5	Q760B	F6	G5	R540	G4	F4			
CR571	E4	E5	Q770	D6	H5	R541	G5	F4	U130D	C2	B3
CR572	D4	E5	Q771	D6	H5	R550	F4	E4	U170A	C1	B5
CR670	D5	G5	Q772	D6	H5	R551	G5	E4	U170B	C1	B5
CR671	E5	G5	Q773	D6	H5	R552	F3	F4	U170D	B1	B5
CR672	D6	G5				R554	F3	F4	U180A	B1	B6
CR770	E6	H5	R170	A2	A5	R555	F4	F4	U180B	B1	B6
CR771	D6	H5	R180	A2	A5	R560	F3	F4	U180C	B1	B6
CR772	D6	H5	R181	A2	A6	R560	E4	F4	U180D	C1	B6
			R182	A1	A6	R562	E4	E5	U270A	B1	C5
J13	G1	B1	R183	A1	B6	R571	E4	E5	U280A	F1	C6
			R250	F1	B4	R572	D4	E5	U280B	C2	C6
P3	C3	E6	R251	F1	B4	R581	D4	F6	U460	E3	D5
P8	A1	B6	R252	G1	C4	R582	D4	E6	U540A	G3	E4
			R253	G1	C4	R583	C4	E6	U540B	G2	E4
Q181	B1	A5	R254	G1	C4	R650	F6	G4	U540C	G4	E4
Q360	C3	C5	R255	G1	C4	R651	F5	G4	U540D	G4	E4
Q361	C1	D5	R280	B1	C6	R652	F6	G4	U640A	G5	G4
Q362	C2	D5	R281	A2	C6	R660	F6	F4	U640B	G5	G4
Q363	C2	D5	R350	F3	D4	R661	E5	G5	U640C	G6	G4
Q370	D2	D6	R351	C2	C4	R670	D5	G5	U640D	G7	G4
Q371	D2	D6	R352	C2	C4	R671	E5	G5	U660	E5	G5
Q372	D3	D5	R353	C2	C4	R681	D5	G6	U760	E6	H5
Q373	D3	D5	R354	C2	D4	R682	D5	G6			
Q450	F3	E4	R355	D2	D4	R683	C6	G6			

Partial A8 also shown on diagrams 9 and 11.

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P13	A1	H4	P13	G1	H4

Partial A11 also shown on diagrams 1, 5, 9, 10, 11, 12, 13, 14, 15, 16, and 17.

VOLTAGE AND WAVEFORM CONDITIONS

Voltage Conditions. The test voltages (circled numbers) on the schematic were taken using a digital multimeter with 10 MΩ input impedance (TEKTRONIX DM501A Digital Multimeter installed in a TM501 Power Module or a TEKTRONIX 7D13 Digital Multimeter used with a readout equipped 7000-series oscilloscope).

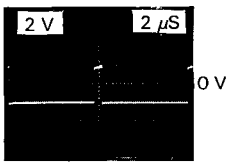
No plug-in units were installed.

Waveform Conditions. A 5B25N Digitizer Time Base/Ampl with controls set as follows: Time/Div (1 ms), Chop (In), Triggering (AC, Auto, Left) was installed in the horizontal plug-in compartment of the 5223.

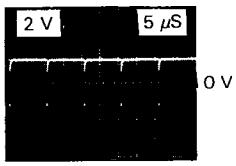
The waveforms were monitored using a test oscilloscope system with 10 MΩ input impedance, at least 60 MHz bandwidth and 10X probe (TEKTRONIX 7603 Oscilloscope, 7B92A Time Base, 7A13 Differential Comparator and P6062B Probe.

Refer to the individual waveform photos for deflection factor and sweep rate settings.

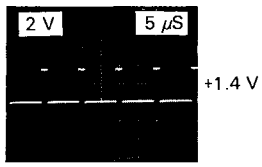
18



19

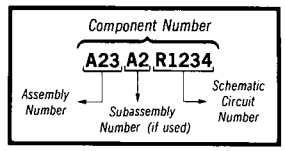


20

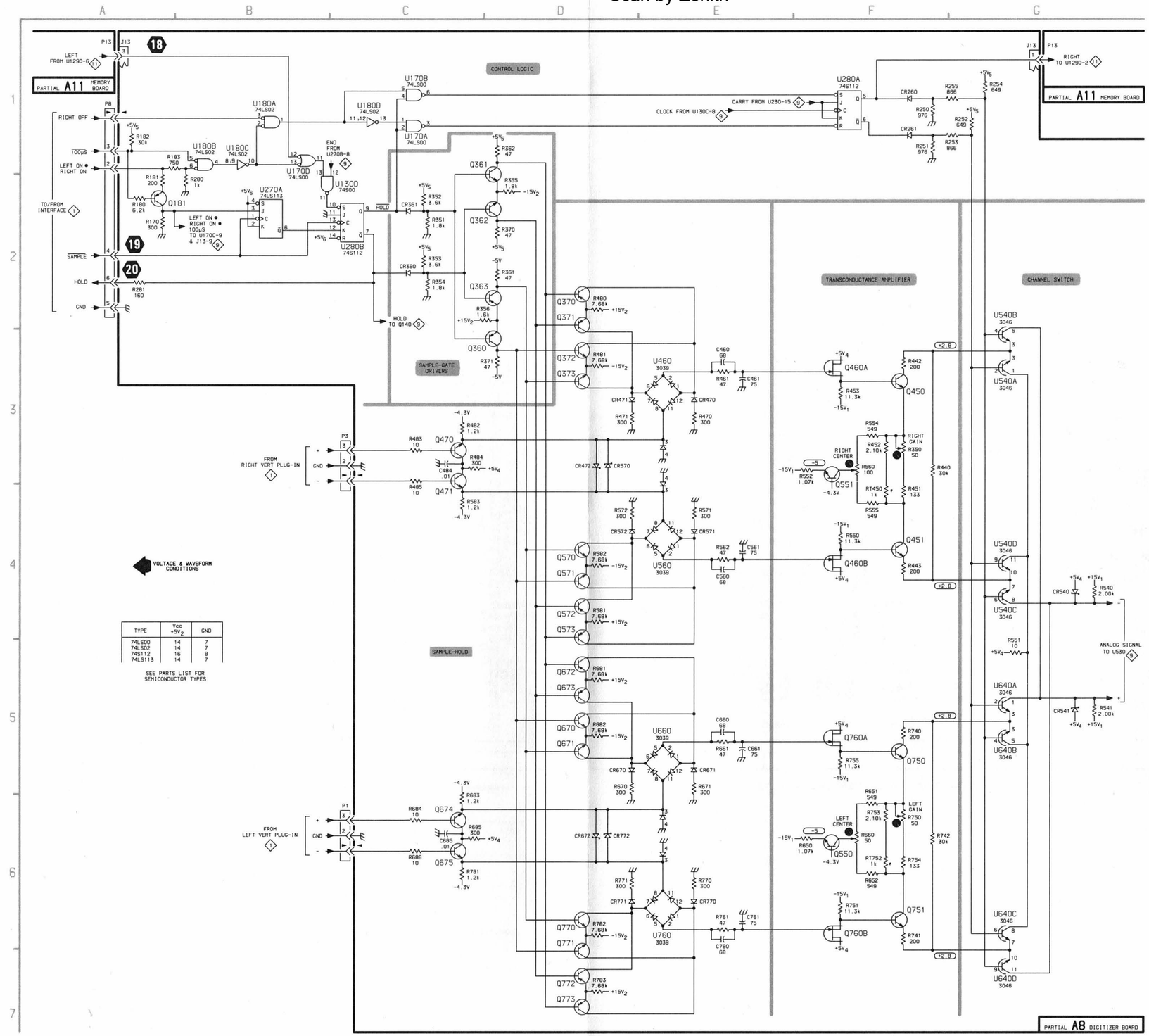


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



TYPE	Vcc +5V$_2$	GND
74LS00	14	7
74LS02	14	7
74S112	16	8
74LS113	14	7

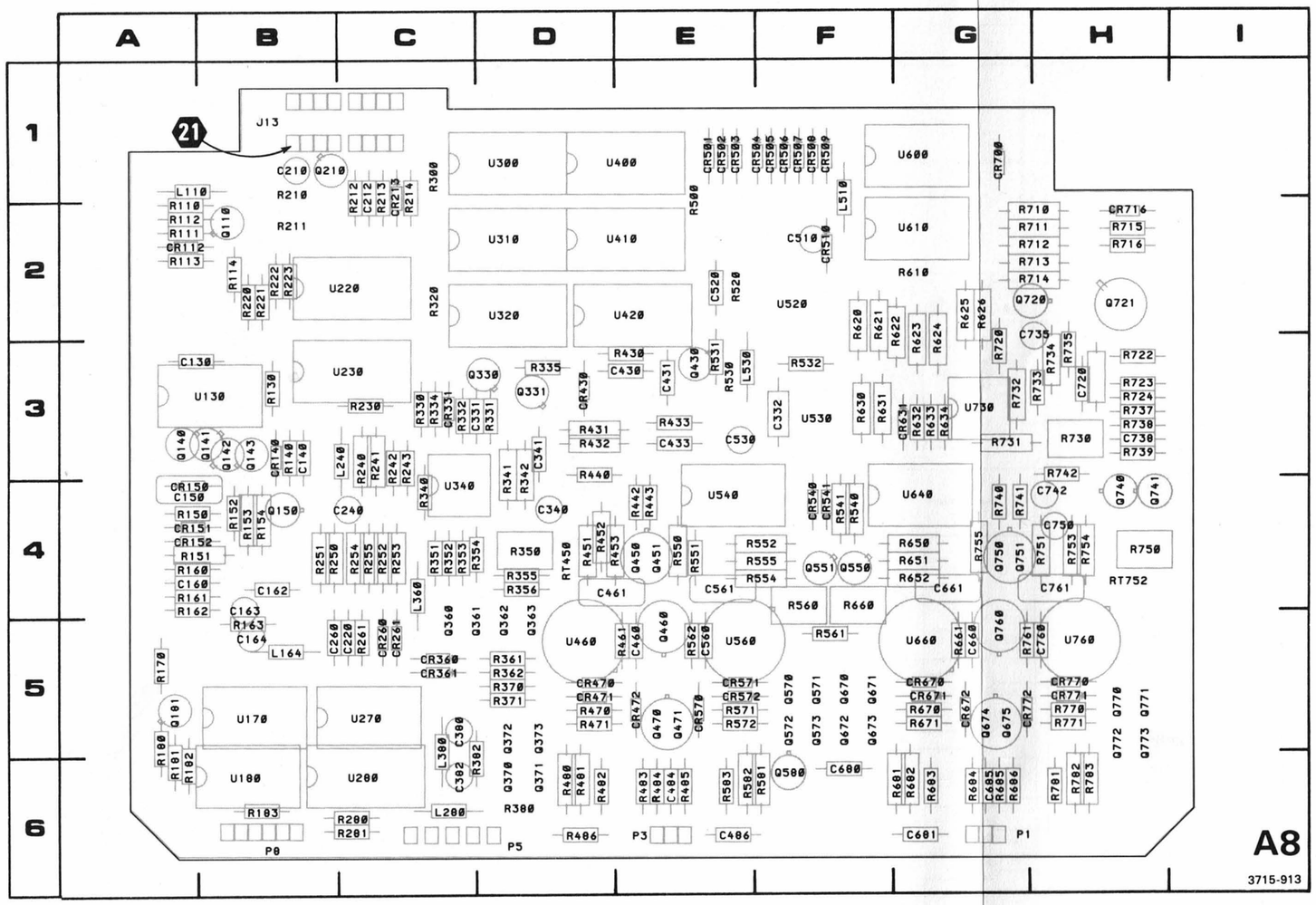


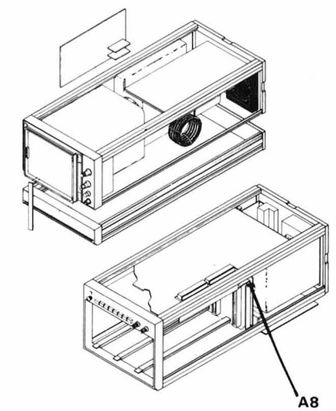
Figure 9-15. A8-Digitizer circuit board assembly.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



A8 DIGITIZER
Shown on Diag. 8 & 9

ASSEMBLY

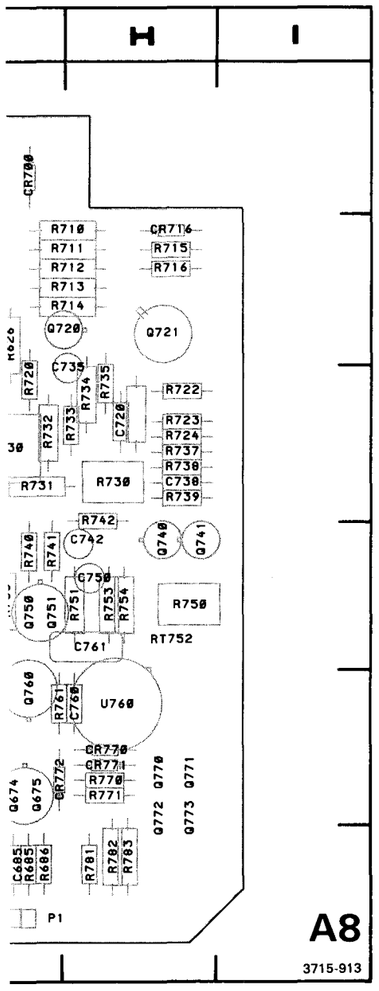
CIRCUIT NUMBER	LO
C130	
C140	
C150	
C160	
C162	
C163	
C164	
C210	
C212	
C220	
C240	
C260	
C331	
C332	
C340	
C341	
C380	
C382	
C431	
C433	
C486	
C510	
C520	
C530	
C680	
C681	
C720	
C735	
C738	
C742	
C750	
CR112	
CR140	
CR150	
CR151	
CR152	
CR213	
CR331	
CR430	
CR501	
CR502	
CR503	
CR504	
CR505	
CR506	
CR507	
CR508	
CR509	

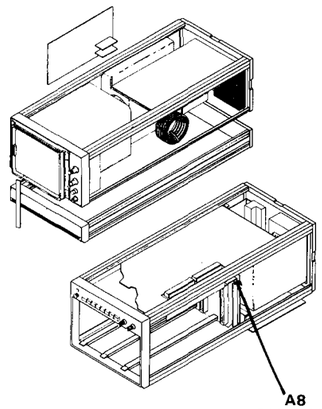
Partial A8 also

ASSEMBLY

CIRCUIT NUMBER	S
P13	

Partial A11 als and 17.





A8
DIGITIZER
Shown on Diag. 8 & 9

DIGITIZER A/D CONVERTER DIAGRAM 9

ASSEMBLY A8

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C130	G5	B3	CR510	G1	F2	R162	I6	A4	R486	I6	D6	R724	G4	H3
C140	A1	B3	CR631	G4	G3	R163	A1	B5	R500A	D4	E1	R730	E6	H3
C150	B1	A4	CR700	E6	G1	R210A	D2	B1	R500B	D4	E1	R731	G2	G3
C160	A1	A4	CR716	E6	H2	R210B	C4	B1	R500C	D4	E1	R732	G1	G3
C162	B2	B4				R210C	C3	B1	R500D	D3	E1	R733	G1	H3
C163	I6	B4	J13	H3	B1	R210D	C3	B1	R500E	D3	E1	R734	G1	H3
C164	G5	B5	J13	C1	B1	R210E	C3	B1	R500F	D2	E1	R735	G1	H3
C210	G5	B1				R211A	B4	B2	R500G	D3	E1	R737	G5	H3
C212	D2	C1	L110	G5	A1	R211B	C3	B2	R520A	C5	E2	R738	G4	H3
C220	C2	C5	L164	G5	B5	R211C	C3	B2	R520B	D6	E2	R739	H4	H3
C240	G6	C4	L240	H6	C3	R211D	C3	B2	R520C	B5	E2			
C260	G5	C5	L280	G4	C6	R211E	B5	B2	R520D	C5	E2	U130A	C2	B3
C331	G3	D3	L360	H5	C4	R212	D2	C1	R520E	D5	E2	U130B	B1	B3
C332	G4	F3	L380	H5	C5	R213	D2	C1	R520F	D5	E2	U130C	B1	B3
C340	H6	D4	L510	H5	F1	R214	D2	C1	R520G	D5	E2	U170C	B5	B5
C341	H5	D3	L530	I5	E3	R220	B3	B2	R530A	H3	E3	U220	C2	C2
C380	H5	C5				R221	B3	B2	R530B	H2	E3	U230	B2	C3
C382	G4	C6	P5	I4	D6	R222	B3	B2	R530C	G3	E3	U270B	B5	C5
C431	G3	E3				R223	B4	B2	R530D	G3	E3	U300A	D3	D1
C433	B5	E3	Q110	H3	B2	R230	G5	C3	R531	B5	E3	U300B	D2	D1
C486	I6	E6	Q140	A1	A3	R240	H6	C3	R532	F1	F3	U300C	D3	D1
C510	H5	F2	Q141	A2	B3	R241	H6	C3	R561	G6	F5	U300D	D2	D1
C520	B5	E2	Q142	B1	B3	R242	G6	C3	R610A	E5	G2	U310A	D4	D2
C530	I5	E3	Q143	B1	B3	R243	G6	C3	R610B	E4	G2	U310B	D4	D2
C680	G5	F6	Q150	A1	B4	R261	C2	C5	R610C	E5	G2	U310C	D3	D2
C681	I4	G6	Q210	D2	B1	R300A	C3	C1	R610D	E5	G2	U310D	C5	D2
C720	I6	H3	Q330	H3	D3	R300B	C3	C1	R610E	E4	G2	U320B	D5	D2
C735	G1	H2	Q331	H2	D3	R300C	C2	C1	R620	F2	F2	U320C	D5	D2
C738	G4	H3	Q430	B5	E3	R300D	C3	C1	R621	F2	F2	U320D	D5	D2
C742	H5	H4	Q580	G6	F6	R300E	D2	C1	R622	F2	G2	U340A	H6	C4
C750	H6	H4	Q720	E6	H2	R320A	G3	C2	R623	F4	G2	U340B	H4	C4
			Q721	G4	H2	R320B	B5	C2	R624	F4	G2	U400A	D3	E1
CR112	H3	A2	Q740	H4	H4	R320C	C5	C2	R625	F4	G2	U400B	D3	E1
CR140	B1	B3	Q741	G4	H4	R320D	C4	C2	R626	F4	G2	U400C	D2	E1
CR150	B1	A4				R320E	C4	C2	R630	F2	F3	U400D	D3	E1
CR151	B1	A4	R110	C2	A2	R320F	C5	C2	R631	F3	F3	U410A	D4	E2
CR152	B1	A4	R111	H3	A2	R320G	C5	C2	R632	G1	G3	U410B	D5	E2
CR213	D2	C1	R112	H3	A2	R330	B5	C3	R633	G1	G3	U410C	D4	E2
CR331	F3	C3	R113	H3	A2	R331	F3	D3	R634	G1	G3	U410D	D4	E2
CR430	H4	D3	R114	H3	B2	R332	G3	C3	R710	E4	H2	U420A	G3	E2
CR501	D3	E1	R130	B1	B3	R334	G3	C3	R711	E4	H2	U420B	G3	E2
CR502	D3	E1	R140	B1	B3	R335	H2	D3	R712	E5	H2	U420C	D5	E2
CR503	D3	E1	R150	A2	A4	R340	G6	C4	R713	E5	H2	U420D	B5	E2
CR504	D3	F1	R151	B1	A4	R341	H5	D4	R714	E5	H2	U520	E1	F2
CR505	D4	F1	R152	B1	B4	R342	H5	D4	R715	E6	H2	U530	G2	F3
CR506	D4	F1	R153	B1	B4	R430	G3	E3	R716	E6	H2	U600	E4	G1
CR507	D5	F1	R154	B1	B4	R431	H4	D3	R720	F1	G3	U610	E5	G2
CR508	D5	F1	R160	A1	A4	R432	H4	D3	R722	G4	H3	U730A	G1	G3
CR509	D5	F1	R161	A1	A4	R433	B5	E3	R723	G4	H3	U730B	F1	G3

Partial A8 also shown on diagrams 8 and 11.

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P13	D1	H4	P13	H3	H4

Partial A11 also shown on diagrams 1, 5, 8, 10, 11, 12, 13, 14, 15, 16, and 17.

VOLTAGE AND WAVEFORM CONDITIONS

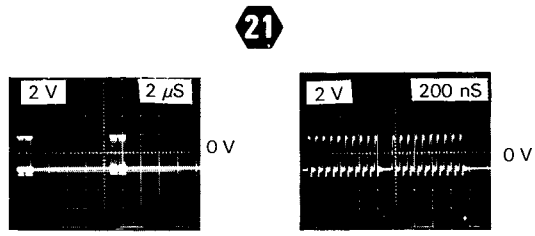
Voltage Conditions. The test voltages (circled numbers) on the schematic were taken using a digital multimeter with 10 MΩ input impedance (TEKTRONIX DM501A Digital Multimeter installed in a TM501, Power Module or a TEKTRONIX 7D13 Digital Multimeter used with a readout equipped 7000-series oscilloscope).

No plug-in units were installed.

Waveform Conditions. A 5B25N Digitizer Time Base/Ampl with controls set as follows: Time Div (1 ms), Chop (In), Triggering (AC, Auto, Left) was installed in the horizontal plug-in compartment of the 5223.

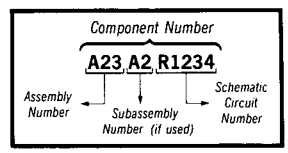
The waveforms were monitored using a test oscilloscope system with 10 MΩ input impedance, at least 60 MHz bandwidth and 10X probe (TEKTRONIX 7603 Oscilloscope, 7B92A Time Base, 7A13 Differential Comparator and P6062B Probe.

Refer to the waveform photos for deflections factor and sweep rate settings.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

CLOCK GENERATOR

TIMING COUNTER/DECODER

VOLTAGE & WAVEFORM CONDITIONS

PARTIAL A11 MEMORY BOARD

D/A CONVERTER

COMPARATOR

+11V,-5V,-4.3V SUPPLIES

SUCCESSIVE-APPROXIMATION REGISTER

PARTIAL A8 DIGITIZER BOARD

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

POWER FROM INTERFACE 7

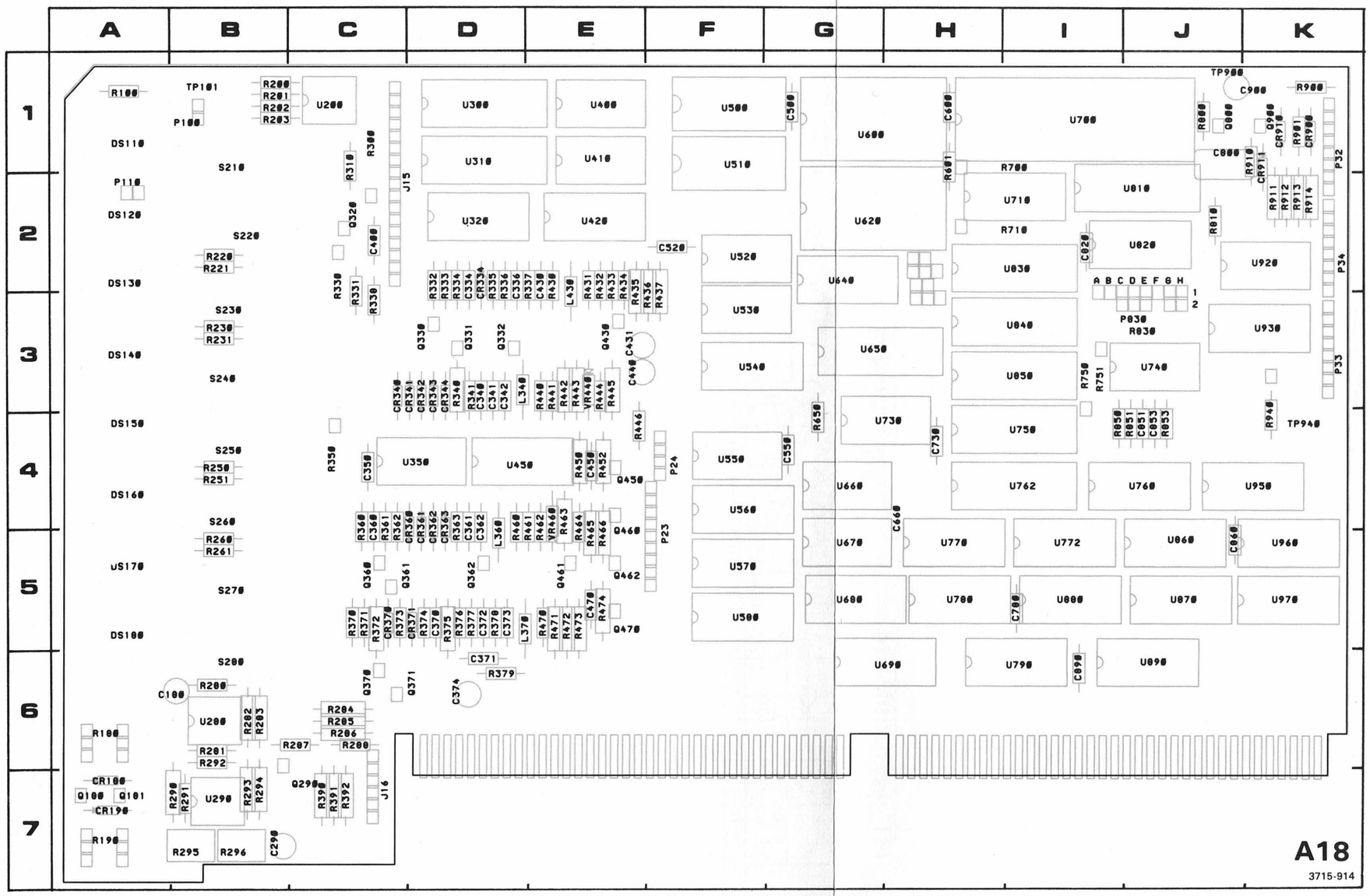


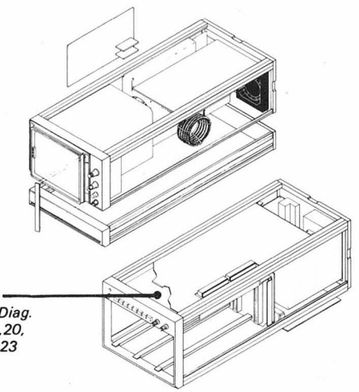
Figure 9-16. A18-GPIB circuit board assembly.

MEMORY CONTENTS CONTRO

ASSEMBLY A18

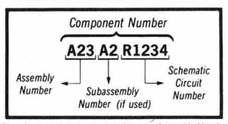
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C400	C5	C2
DS110	G1	A1
DS120	G1	A2
DS130	G1	A2
DS140	G2	A3
DS150	G2	A4
DS160	G2	A4
DS170	G2	A5
DS180	G2	A5
J15	A4	C2
J15	G3	C2
Q320	F4	C2
R200	B5	B1
R201	B5	B1
R202	B5	B1
R203	B5	B1
R220	F1	B2
R221	F1	B2
R230	F1	B3
R231	F2	B3
R250	F2	B4
R251	F2	B4
R260	F2	B5
R261	F3	B5
R288	F4	C6
R300A	E4	C1
R300B	E3	C1
R300C	E4	
R300D	E3	
R300E	E3	
R300F	E3	
R300G	E3	
R300H	E4	
R300J	B5	
R310	B5	
R330A	B1	
R330B	B2	
R330C	B2	
R330D	B2	
R330E	B2	
R330F	B2	
R330G	B2	
R330H	B2	
R330J	B3	
R331	F4	
R332	F4	
R338	B5	
R350A	B3	
R350B	B3	
R350C	B3	
R350D	B3	
R350E	B4	
R350F	B4	
R350G	B4	
R431	E5	
R432	F4	
R433	E5	
R434	F4	

Partial A18 also shown on diagrams 18, 21, 22 and 23.

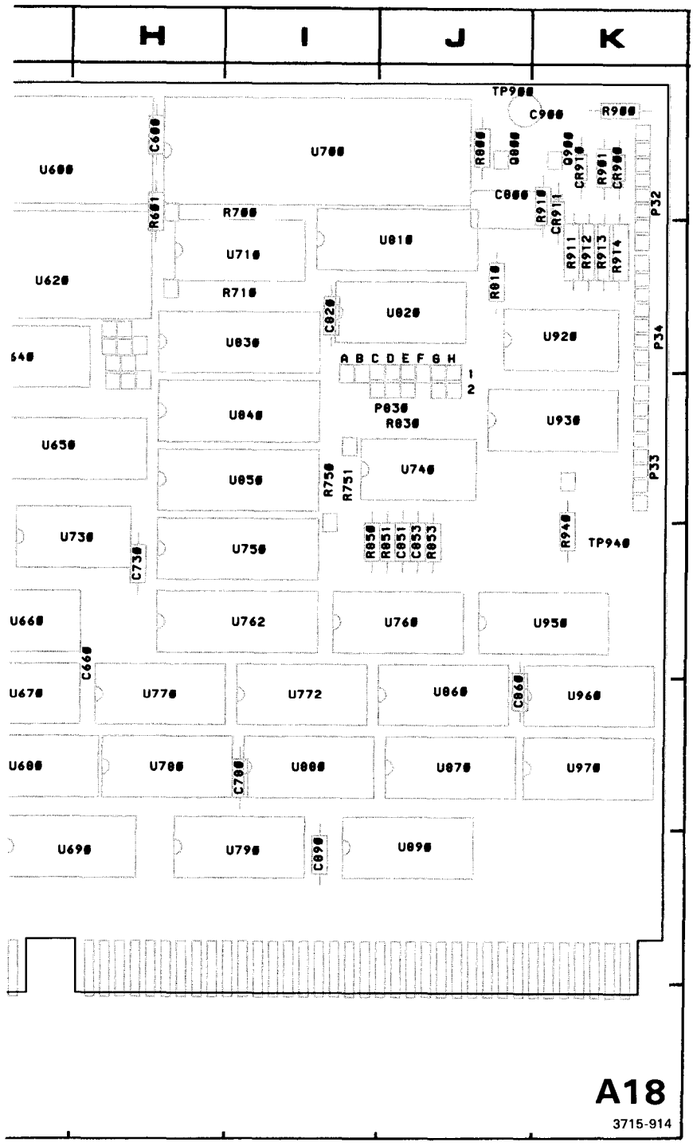


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

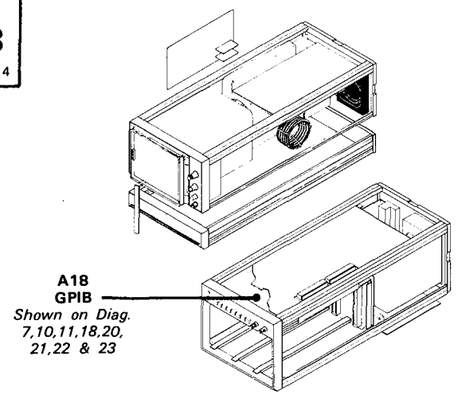


MEMORY CONTENTS CONTROLLER DIAGRAM 10

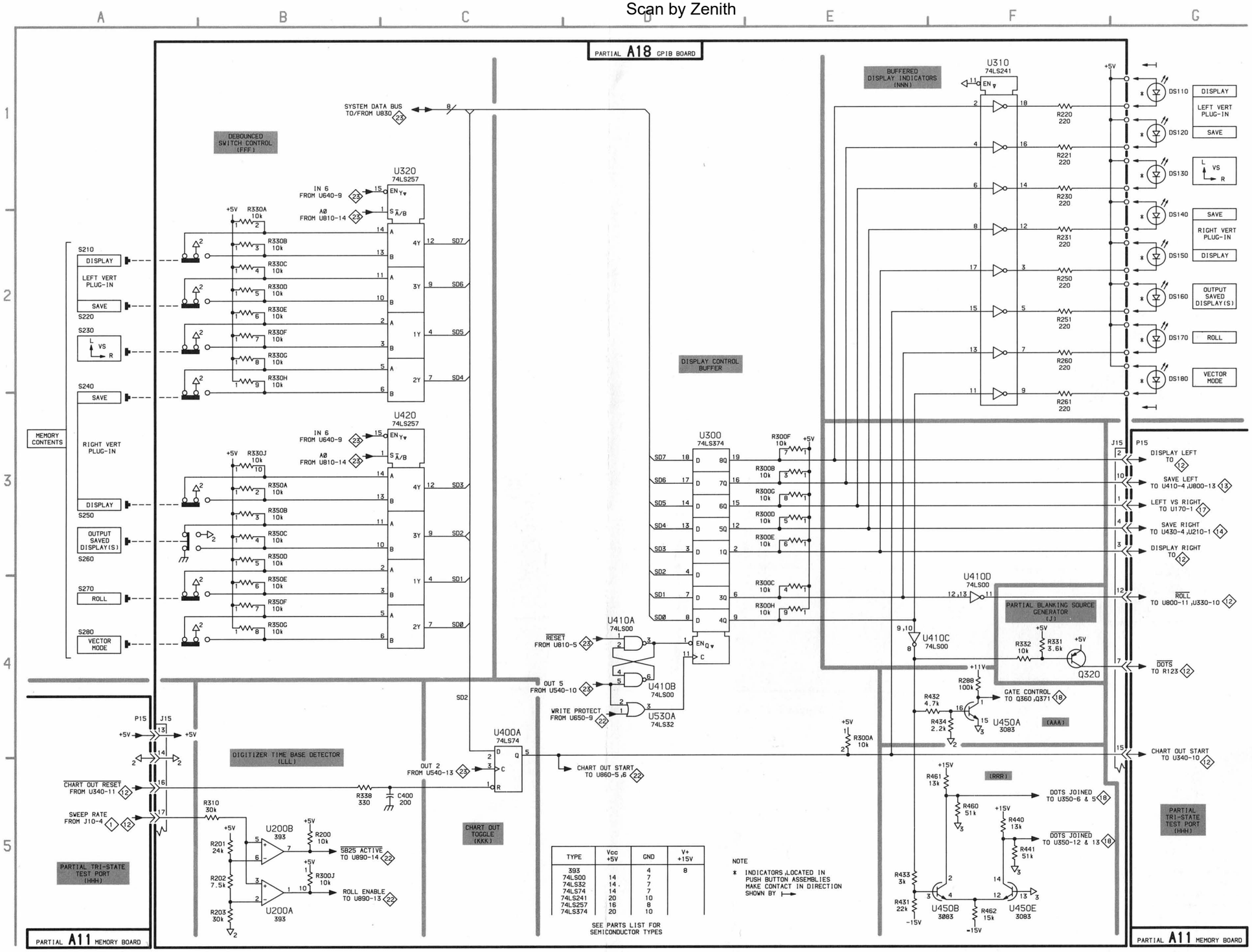
ASSEMBLY A18

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C400	C5	C2
DS110	G1	A1
DS120	G1	A2
DS130	G1	A2
DS140	G2	A3
DS150	G2	A4
DS160	G2	A4
DS170	G2	A5
DS180	G2	A5
J15	A4	C2
J15	G3	C2
Q320	F4	C2
R200	B5	B1
R201	B5	B1
R202	B5	B1
R203	B5	B1
R220	F1	B2
R221	F1	B2
R230	F1	B3
R231	F2	B3
R250	F2	B4
R251	F2	B4
R260	F2	B5
R261	F3	B5
R288	F4	C6
R300A	E4	C1
R300B	E3	C1
R300C	E4	C1
R300D	E3	C1
R300E	E3	C1
R300F	E3	C1
R300G	E3	C1
R300H	E4	C1
R300J	B5	C1
R310	B5	C1
R330A	B1	C2
R330B	B2	C2
R330C	B2	C2
R330D	B2	C2
R330E	B2	C2
R330F	B2	C2
R330G	B2	C2
R330H	B2	C2
R330J	B3	C2
R331	F4	C2
R332	F4	D2
R338	B5	C3
R350A	B3	C4
R350B	B3	C4
R350C	B3	C4
R350D	B3	C4
R350E	B4	C4
R350F	B4	C4
R350G	B4	C4
R431	E5	E2
R432	F4	E2
R433	E5	E2
R434	F4	E2
R440	F5	E3
R441	F5	E3
R460	F5	D4
R461	F5	D4
R462	F5	E4
S210	A2	B1
S220	A2	B2
S230	A2	B3
S240	A2	B3
S250	A3	B4
S260	A3	B4
S270	A4	B5
S280	A4	B6
U200A	B5	C1
U200B	B5	C1
U300	D3	D1
U310	F1	D1
U320	C1	D2
U400A	C4	E1
U410A	D4	E1
U410B	D4	E1
U410C	F4	E1
U410D	F4	E1
U420	C3	E2
U450A	F4	D4
U450B	F5	D4
U450E	F5	D4
U530A	D4	F3

Partial A18 also shown on diagrams 18, 21, 22 and 23.



A18
GPIB
Shown on Diag. 7,10,11,18,20, 21,22 & 23



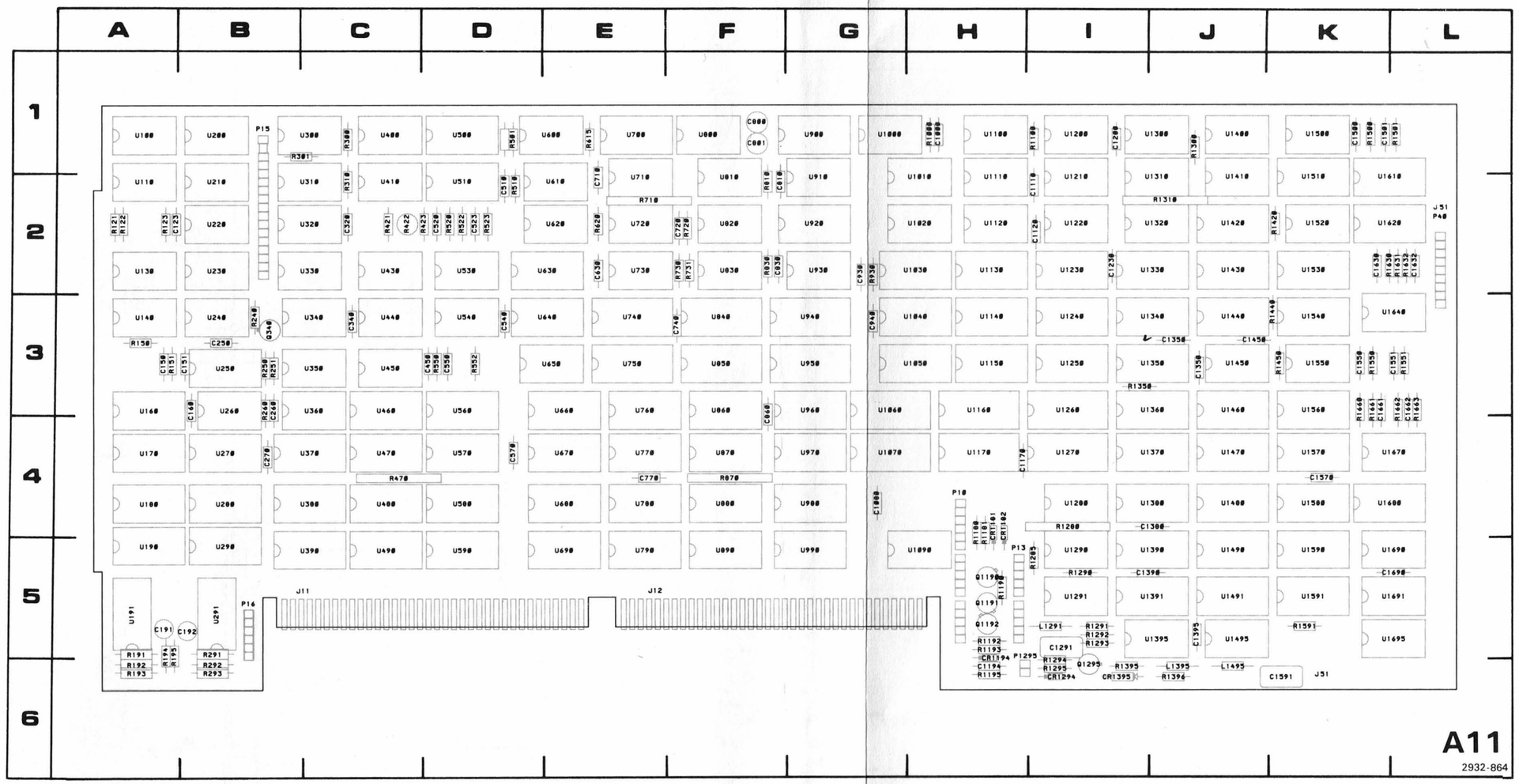


Figure 9-17. A11-Memory circuit board assembly.

A11—Memory Circuit Bd Assembly

Static Sensitive Devices
See Maintenance Section

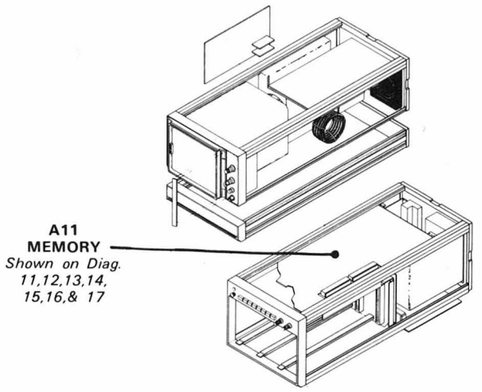
COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



A11
MEMORY
Shown on Diag. 11,12,13,14, 15,16,& 17

EXTERNAL INTERFACE PORT DIAGRAM 11

ASSEMBLY A8

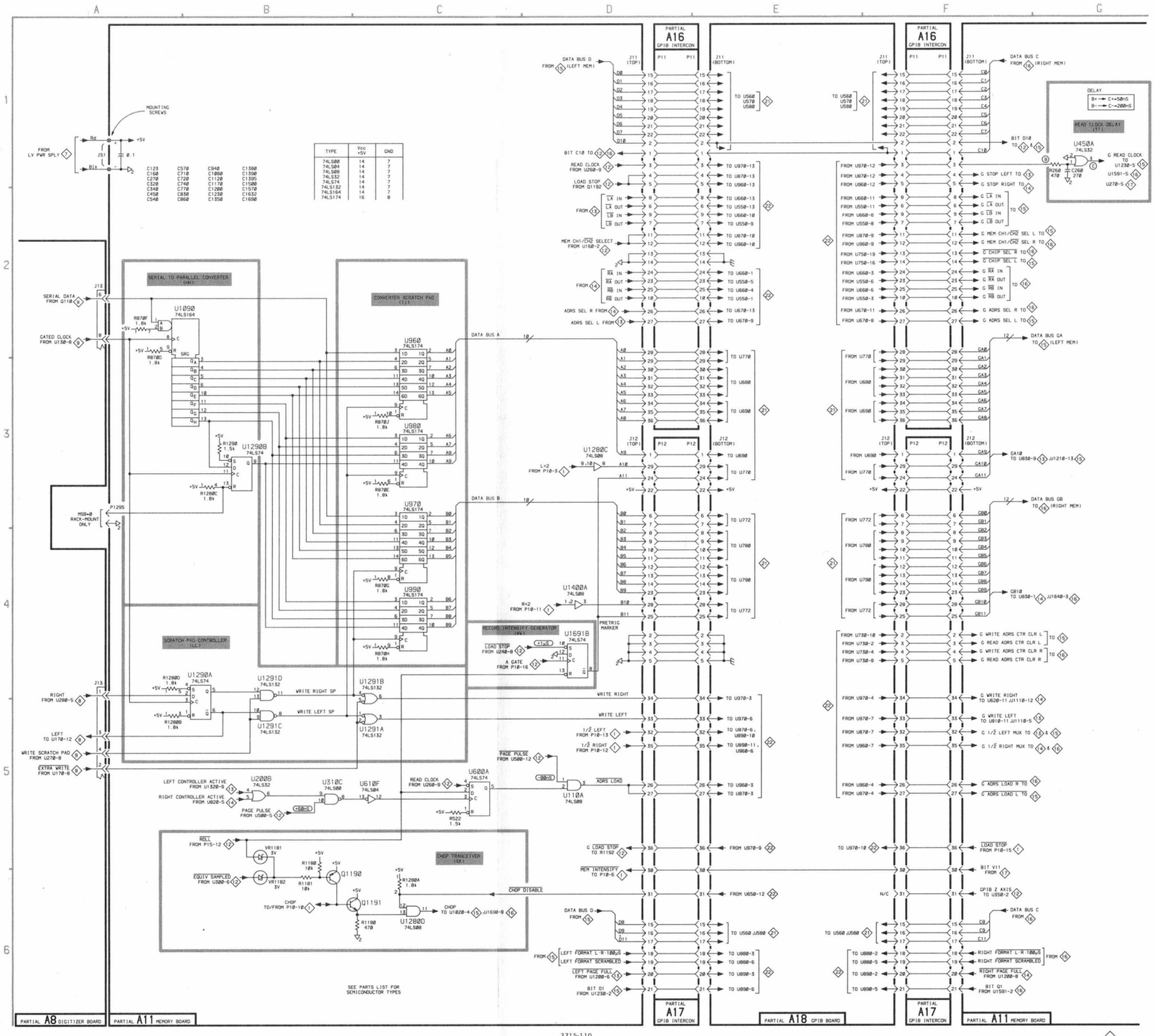
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J13	A2	B1	J13	A4	B1

Partial A8 also shown on diagrams 8 and 9.

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C123	A1	A2	R522	C5	D2
C160	A1	B3	R870D	A2	F4
C260	E1	B3	R870E	C3	F4
C270	A1	B4	R870F	A2	F4
C320	A1	C2	R870G	C4	F4
C340	A1	C3	R870H	C4	F4
C450	A1	D3	R870J	C3	F4
C540	A1	D3	R1180	B5	H4
C570	B1	D4	R1181	B5	H4
C710	B1	E2	R1190	C6	H5
C720	B1	F2	R1280A	C5	I4
C740	B1	F3	R1280B	A5	I4
C770	B1	E4	R1280C	B3	I4
C830	B1	F2	R1280D	A4	I4
C860	B1	F3	R1290	B3	I5
C940	B1	G3			
C1080	B1	G4	U110A	D5	A2
C1120	B1	I2	U200B	B5	B1
C1170	B1	H4	U310C	B5	C2
C1200	B1	I1	U450A	E1	C3
C1230	B1	I2	U600A	C5	E4
C1350	B1	J3	U610F	C5	E2
C1380	B1	J4	U960	C2	G3
C1390	B1	J5	U970	C3	G4
C1395	B1	J5	U980	C3	G4
C1500	B1	K1	U990	C4	G5
C1570	B1	K4	U1090	B2	H5
C1632	B1	L2	U1280C	D3	I4
C1690	B1	L5	U1280D	C6	I4
			U1290A	B4	I5
J11	D1	C5	U1290B	B3	I5
J12	D3	E5	U1291A	C5	I5
J51	A1	L2	U1291B	C4	I5
			U1291C	B5	I5
P1295	A3	H5	U1291D	B4	I5
			U1400A	D4	J1
Q1190	C5	H5	U1691B	D4	L5
Q1191	C6	H5			
			VR1181	B5	H4
R260	E1	B3	VR1182	B5	H4

Partial A11 also shown on diagrams 1, 5, 8, 9, 10, 12, 13, 14, 15, 16, and 17.



5223 GPIB OPTION

3715-110

EXTERNAL INTERFACE PORT 11

5223 Option 10

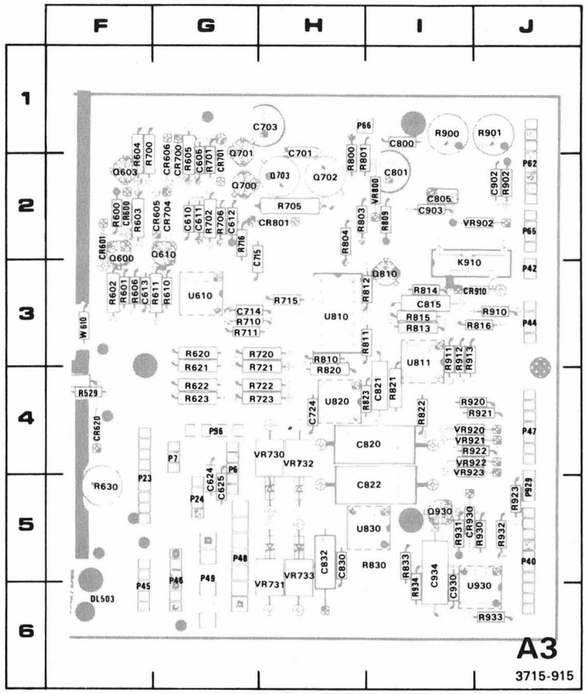


Figure 9-18. A3-Partial XYZ circuit board assembly.

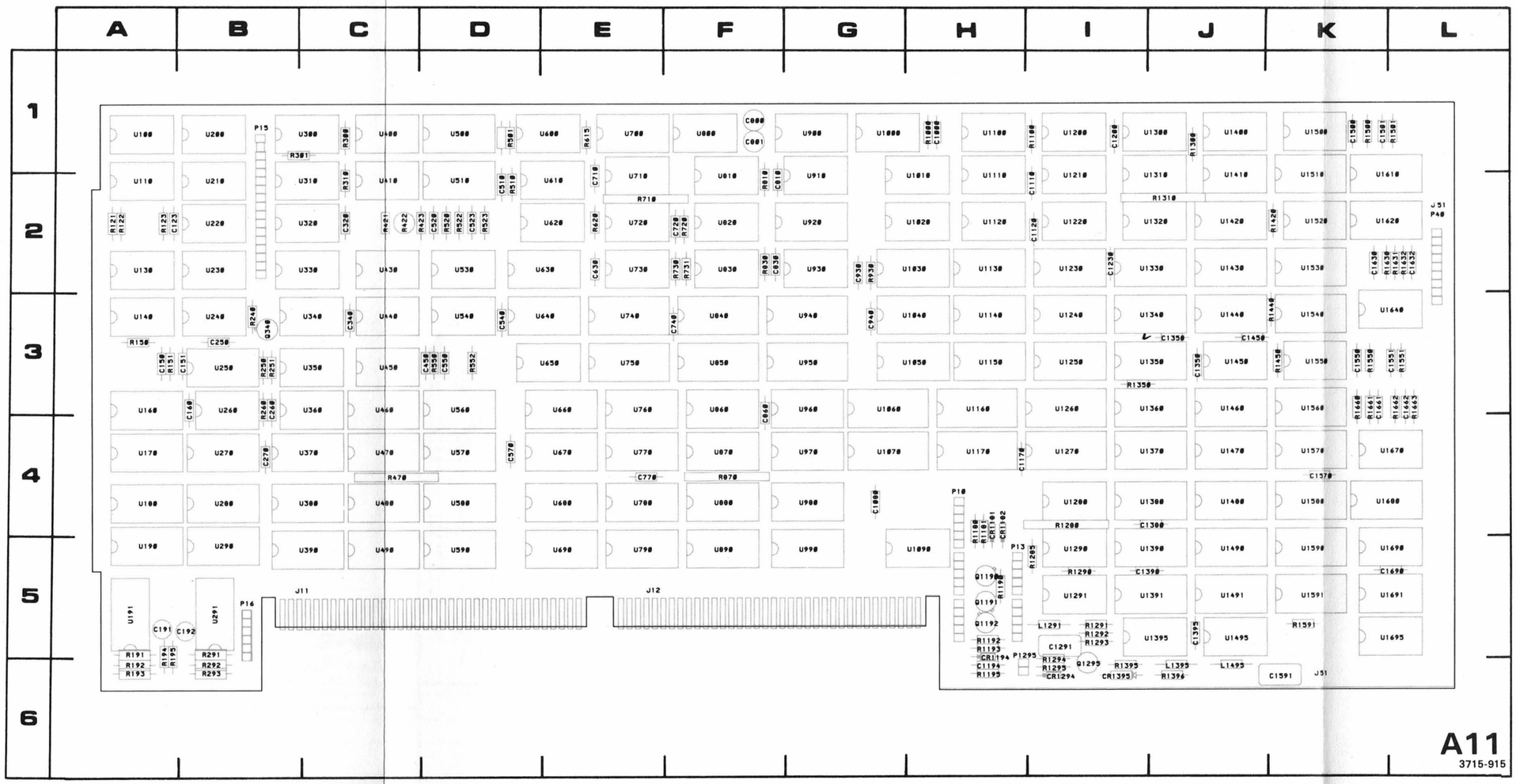
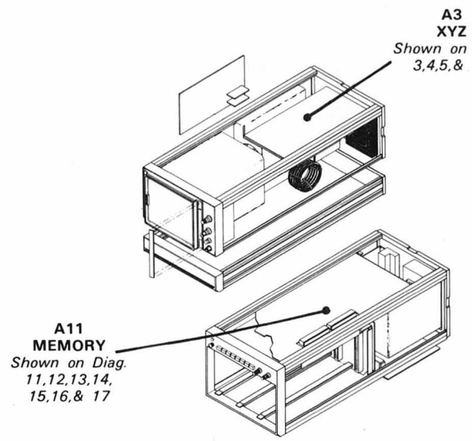
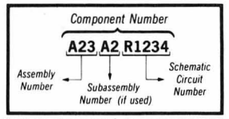


Figure 9-19. A11-Memory circuit board assembly.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

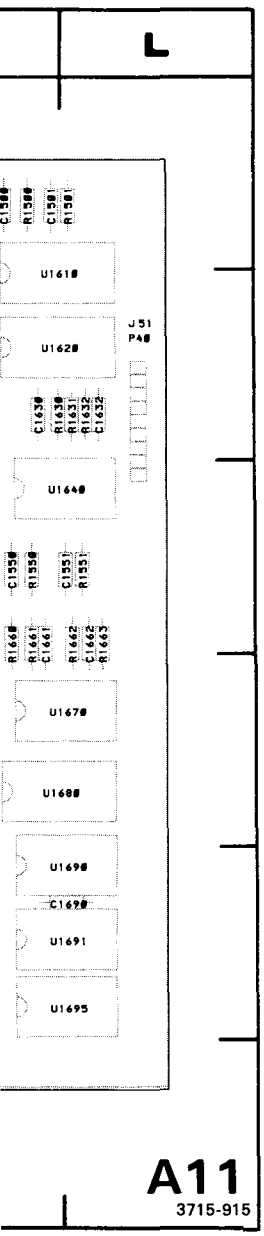


CHART OUT AND DISPLAY CONTROLLERS DIAGRAM 12

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C830	F2	H5	P40	F2	J5	R930	G2	J5
C832	G2	H5	P40	H3	J5	R931	G2	I5
C930	H2	I6	P42	H3	J3	R932	H2	J5
C934	G2	I5	P47	H2	J4	R933	H2	J6
CR910	H3	I2	P929	H3	J5	R934	H2	I6
CR930	G2	I5	Q930	G2	I5	U830	F2	I5
						U930	H2	J6
K910	H3	I3	R830	G2	I5			
			R833	G2	I5			

Partial A3 also shown on diagrams 3, 4, 5 and 6.

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J10	H4	G1	J10	C4	G1

Partial A9 also shown on diagrams 1 and 2.

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J15	A4	B3	J15	E5	B3
J15	A1	B3	J15	D1	B3

Partial A10 also shown on diagrams 7, 10, 17 and 18.

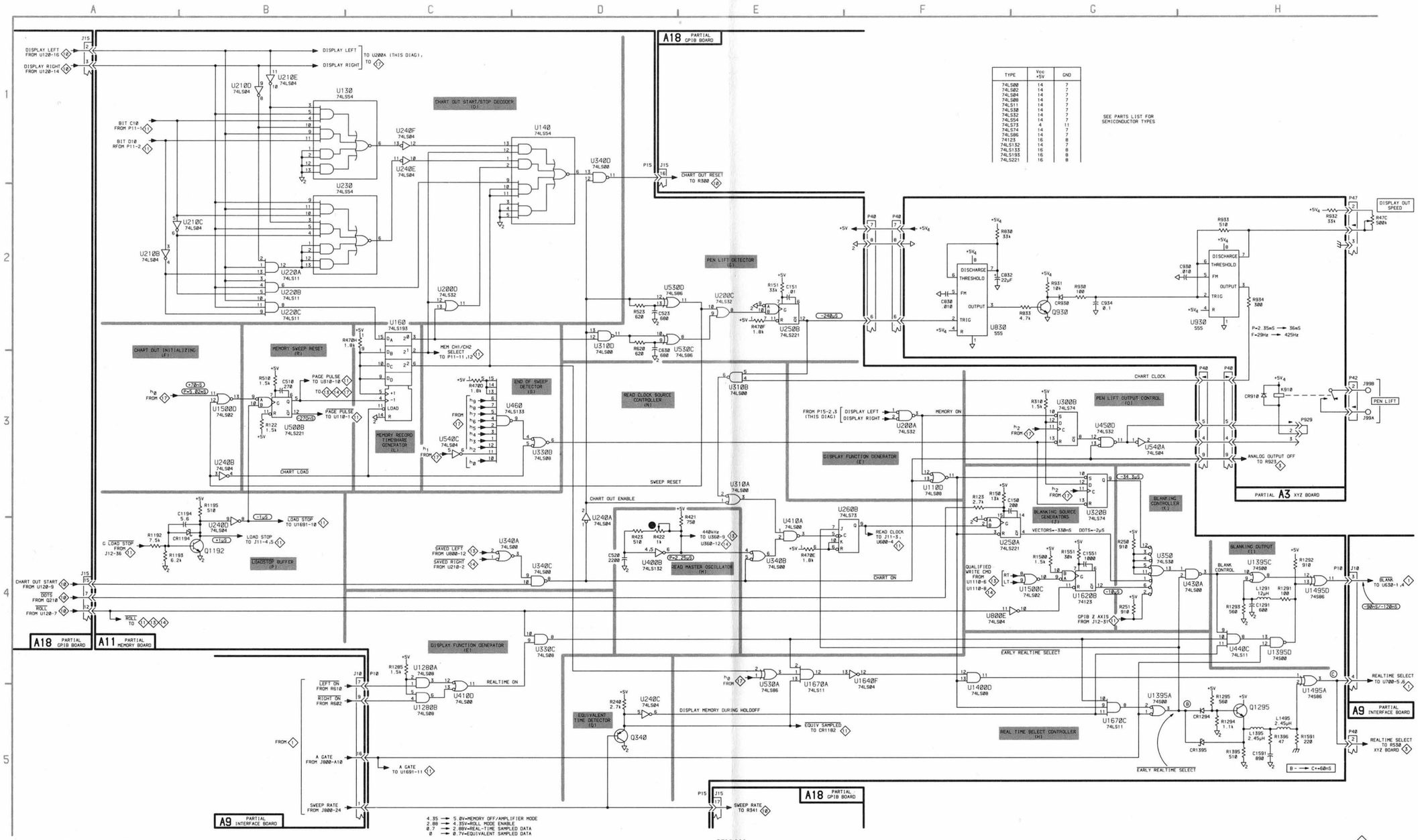
ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C150	G3	A3	R470E	E4	C4	U260B	F3	B3
C151	E2	B3	R470F	E2	C4	U300B	G3	C1
C510	B3	D2	R470H	C2	C4	U310A	E3	C2
C520	D4	D2	R510	B3	D2	U310B	E3	C2
C523	D2	D2	R523	D2	D2	U310D	D2	C2
C630	D2	E2	R620	D2	E2	U320B	G3	C2
C1194	B3	H6	R1192	A4	H5	U330B	D3	C2
C1291	H4	I5	R1193	B4	HC	U330C	D4	C2
C1551	G4	L3	R1195	B3	H6	U340A	D4	C3
C1591	H5	K6	R1285	C4	I5	U340B	E4	C3
			R1291	H4	I5	U340C	D4	C3
CR1194	B4	H5	R1292	H4	I5	U340D	D1	C3
CR1294	H5	I6	R1293	H4	I5	U350	G4	C3
CR1395	H5	I6	R1294	H5	I6	U400B	D4	C1
			R1295	H5	I6	U410A	E4	C2
L1291	H4	I5	R1395	H5	I6	U410D	C5	C2
L1395	H5	J6	R1500	G4	K1	U430A	H4	C2
L1495	H5	J6	R1551	G4	L3	U440C	H4	C3
			R1591	H5	K5	U450D	G3	C3
P10	C4	H4				U460	D3	C3
P10	H4	H4	U110D	F3	A2	U500B	B3	D1
P15	D1	B1	U130	C1	A2	U530A	E4	D2
P15	E5	B1	U140	D1	A3	U530C	E2	D2
P40	H5	L2	U160	C2	A3	U530D	E2	D2
P40	F2	L2	U200A	F3	B1	U540A	G3	D3
P40	H3	L2	U200C	E2	B1	U540C	C3	D3
			U200D	C2	B1	U800E	F4	F1
Q340	D5	B3	U210B	A2	B2	U1280A	C4	I4
Q1192	B4	H5	U210C	B2	B2	U1280B	C5	I4
Q1295	H5	I6	U210D	B1	B2	U1395A	G5	J5
			U210E	B1	B2	U1395C	H4	J5
R122	B3	A2	U220A	B2	B2	U1395D	H4	J5
R123	F3	A2	U220B	B2	B2	U1400D	F5	J1
R150	F3	A3	U220C	B2	B2	U1495A	H5	J5
R151	E2	A3	U230	C1	B2	U1495D	H4	J5
R240	D5	B3	U240A	D3	B3	U1500C	G4	K1
R250	G4	B3	U240B	B3	B3	U1500D	B3	K1
R251	G4	B3	U240C	D5	B3	U1620B	G4	K2
R310	G3	C2	U240D	B4	B3	U1640F	F4	L3
R421	E3	C2	U240E	C1	B3	U1670A	E4	L4
R422	D4	C2	U240F	C1	B3	U1670C	G5	L4
R423	D4	C2	U250A	G4	B3			
R470D	C3	C4	U250B	E2	B3			

Partial A11 also shown on diagrams 1, 5, 8, 9, 10, 11, 13, 14, 15, 16, and 17.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J99A	H3	CHASSIS	R47C	H2	CHASSIS
J99B	H3	CHASSIS			



TYPE	Vcc +5V	GND
74LS00	14	7
74LS02	14	7
74LS04	14	7
74LS08	14	7
74LS11	14	7
74LS30	14	7
74LS32	14	7
74LS54	14	7
74LS75	4	11
74LS74	14	7
74LS86	14	7
74123	16	8
74LS132	14	7
74LS133	16	8
74LS193	16	8
74LS221	16	8

A11—Memory
Circuit Bd Assembly

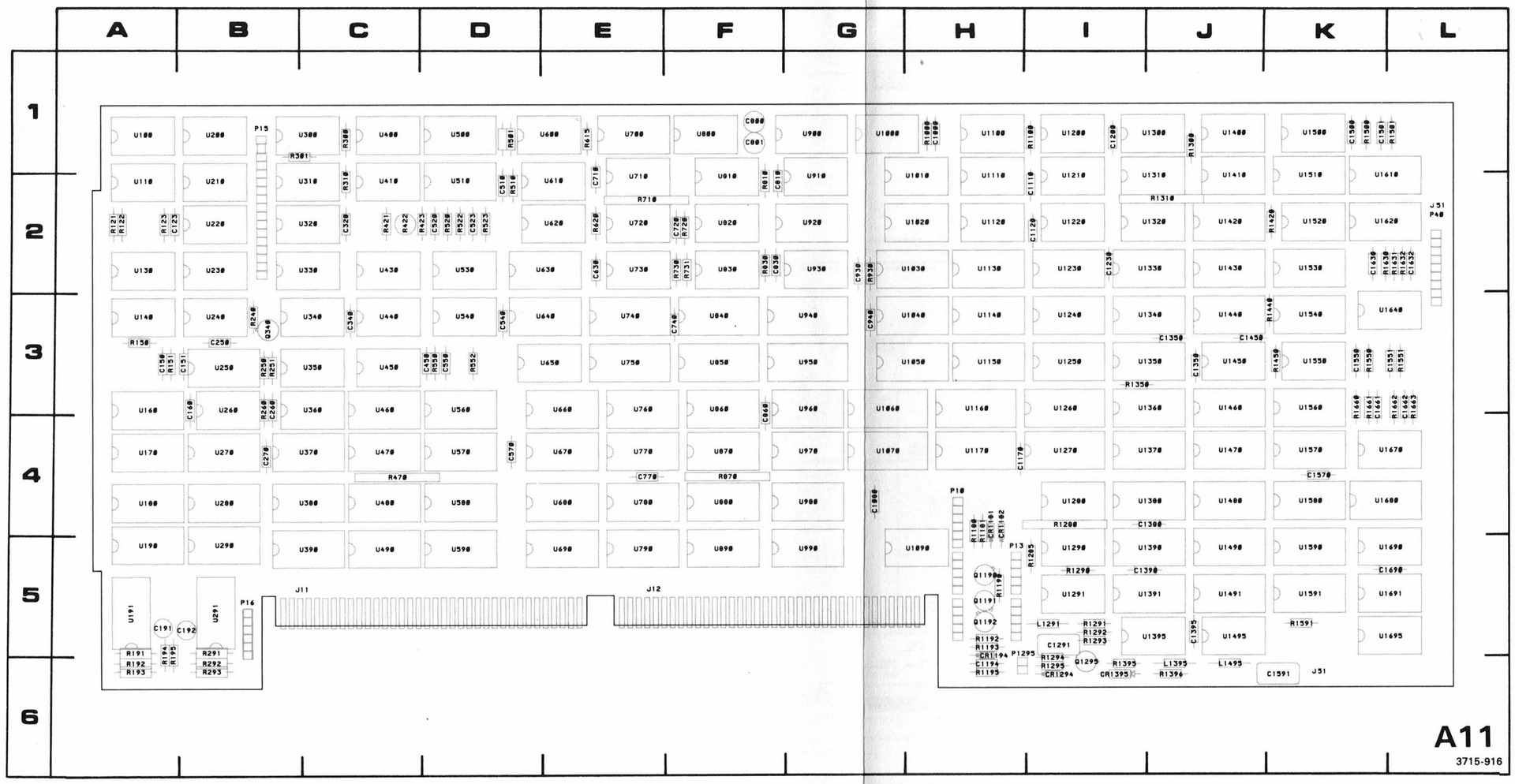


Figure 9-20. A11-Memory circuit board assembly.

Static Sensitive Devices
See Maintenance Section

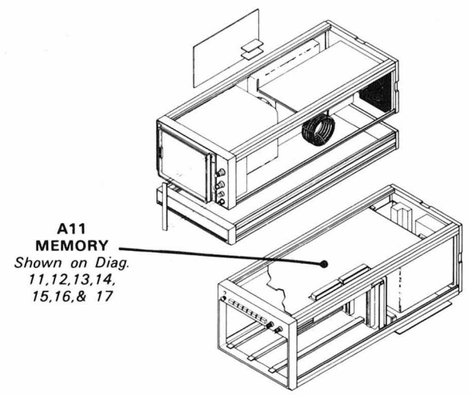
COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

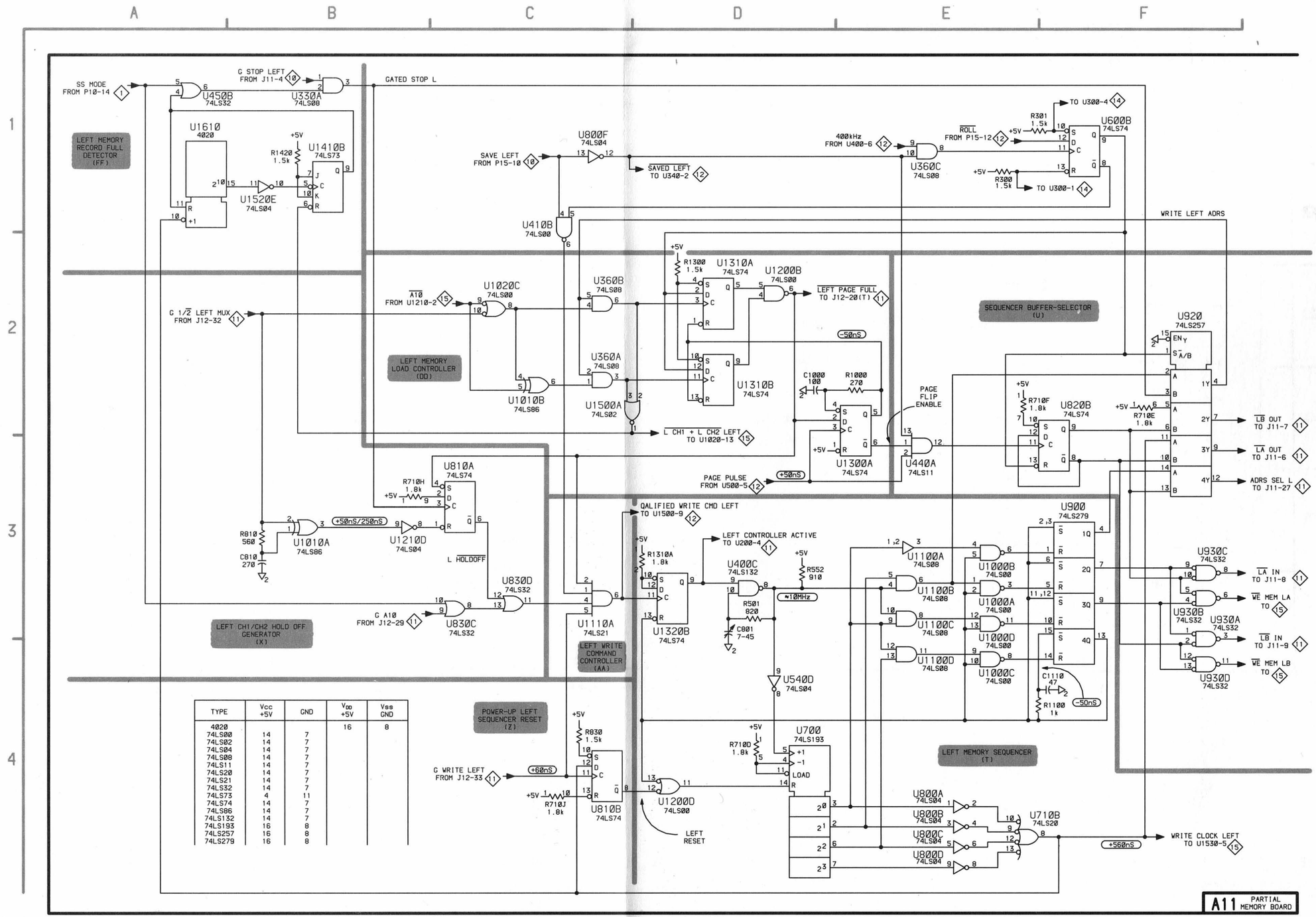


LEFT MEMORY SEQUENCER DIAGRAM 13

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C801	D3	F1	U800D	E4	F1
C810	B3	F2	U800F	C1	F1
C1000	D2	H1	U810A	C3	F2
C1110	F4	I2	U810B	C4	F2
			U820B	F2	F2
R300	E1	C1	U830C	C3	F2
R301	E1	C1	U830D	C3	F2
R501	D3	D1	U900	F3	G1
R552	D3	D3	U920	F2	G2
R710D	D4	E2	U930A	F3	G2
R710E	F2	E2	U930B	F3	G2
R710F	E2	E2	U930C	F3	G2
R710H	B3	E2	U930D	F4	G2
R710J	C4	E2	U1000A	E3	G1
R810	B3	F2	U1000B	E3	G1
R830	C4	F2	U1000C	E4	G1
R1000	E2	H1	U1000D	E3	G1
R1100	F4	I1	U1010A	B3	H2
R1300	D2	J1	U1010B	C2	H2
R1310	D3	J2	U1020C	C2	H2
R1420	B1	K2	U1100A	E3	H1
			U1100B	E3	H1
U330A	B1	C2	U1100C	E3	H1
U360A	C2	C3	U1100D	E4	H1
U360B	C2	C3	U1110A	C3	H2
U360C	E1	C3	U1200B	D2	I1
U400C	D3	C1	U1200D	D4	I1
U410B	C1	C2	U1210D	B3	I2
U440A	E3	C3	U1300A	E3	J1
U450B	A1	C3	U1310A	D2	J2
U540D	D4	D3	U1310B	D2	J2
U600B	F1	E4	U1320B	D3	J2
U700	D4	E1	U1410B	B1	J2
U710B	F4	E2	U1500A	C2	K1
U800A	E4	F1	U1520E	B1	K2
U800B	E4	F1	U1610	A1	K2
U800C	E4	F1			

Partial A11 also shown on diagrams 1, 5, 8, 9, 10, 11, 12, 14, 15, 16, and 17.



TYPE	Vcc +5V	GND	VDD +5V	Vss GND
4020		7	16	8
74LS00	14	7		
74LS02	14	7		
74LS04	14	7		
74LS08	14	7		
74LS11	14	7		
74LS20	14	7		
74LS21	14	7		
74LS32	14	7		
74LS73	4	11		
74LS74	14	7		
74LS86	14	7		
74LS132	14	7		
74LS193	16	8		
74LS257	16	8		
74LS279	16	8		

A11—Memory
Circuit Bd Assembly

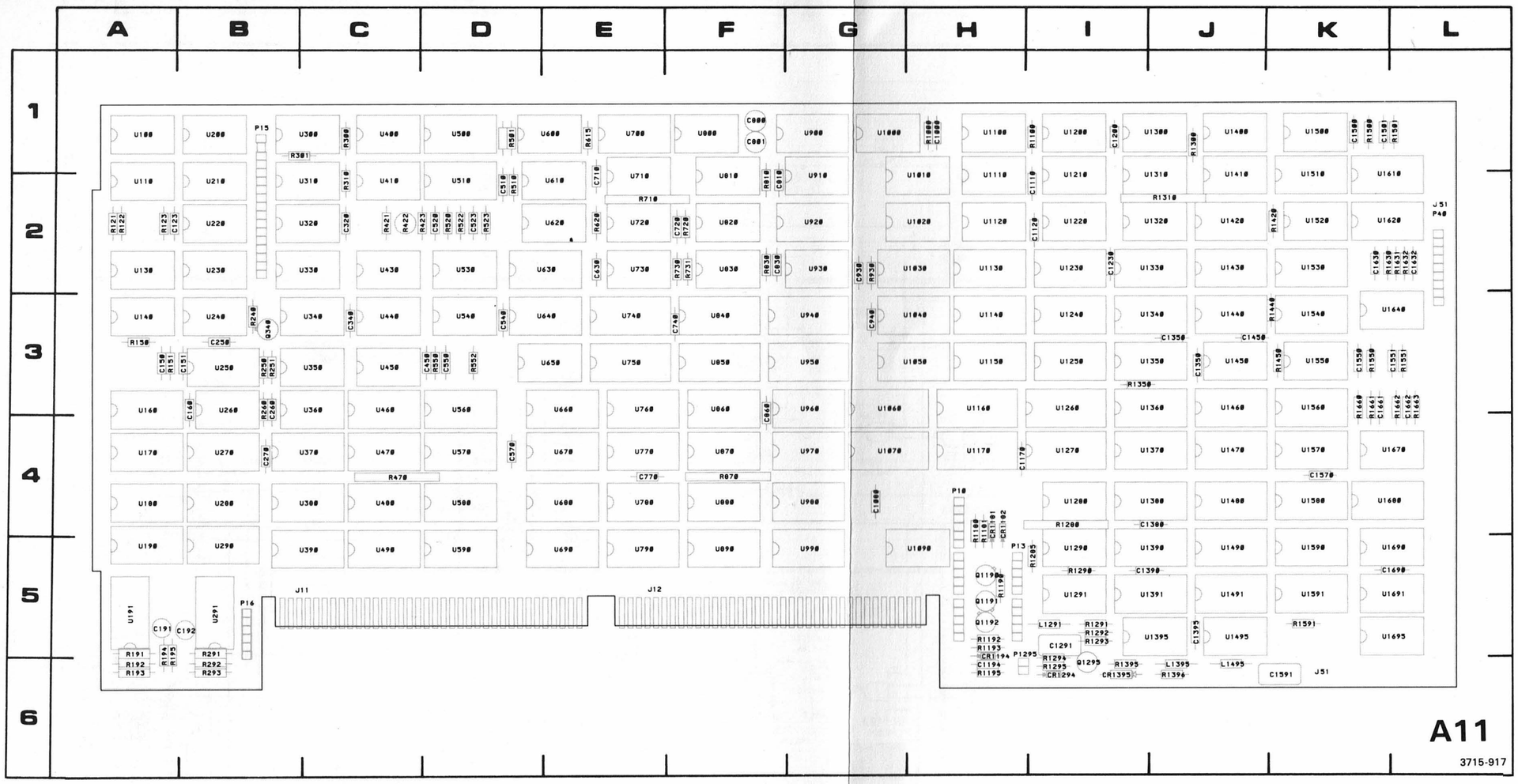


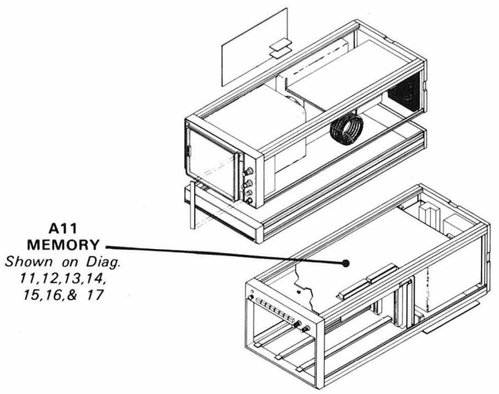
Figure 9-21. A11-Memory circuit board assembly.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

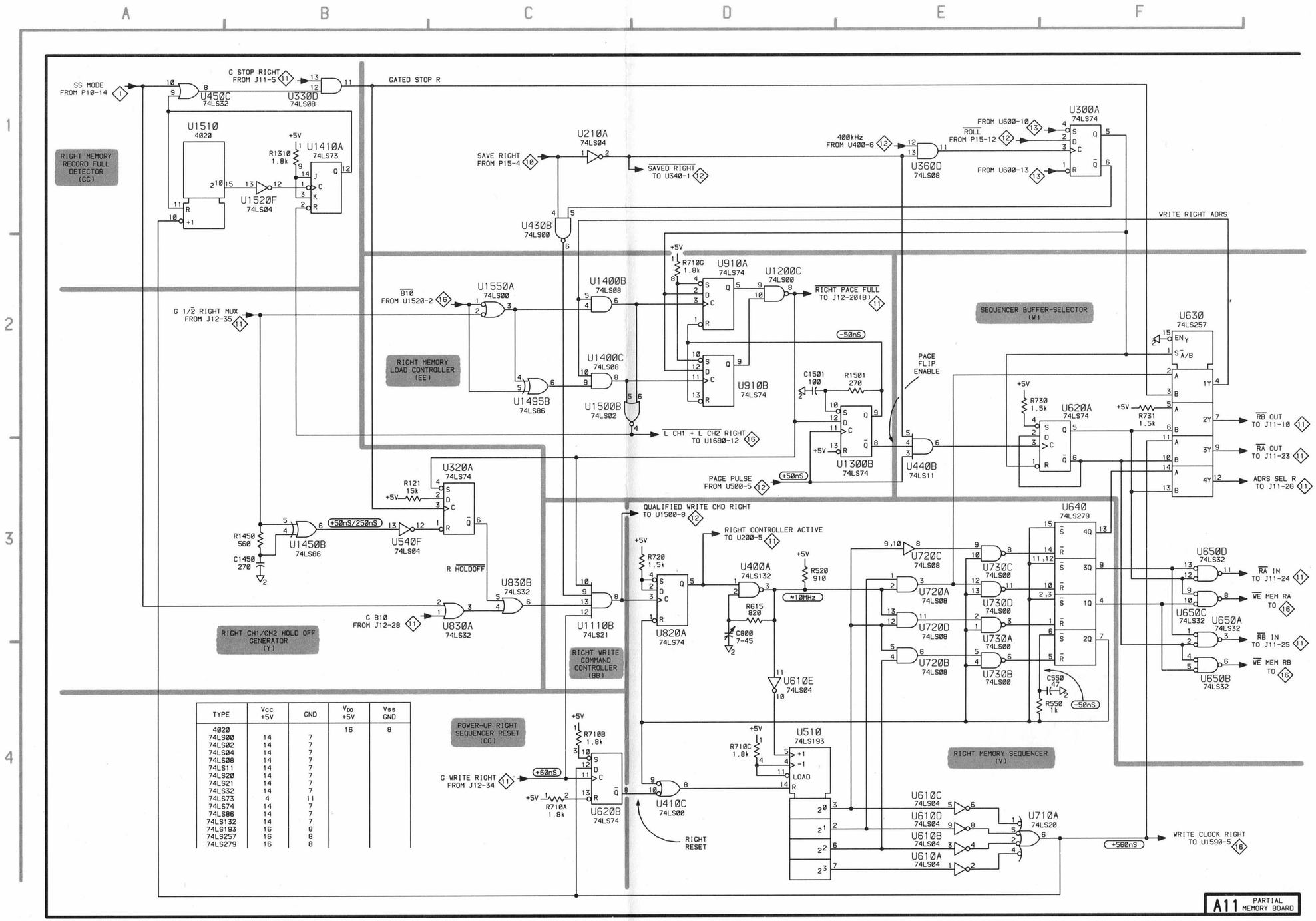


RIGHT MEMORY SEQUENCER DIAGRAM 14

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C550	F4	D3	U610E	D4	E2
C800	D3	F1	U620A	F2	E2
C1450	B3	J3	U620B	C4	E2
C1501	D2	K1	U630	F2	E2
			U640	F3	E3
R121	B3	A2	U650A	F3	E3
R520	D3	D2	U650B	F4	E3
R550	F4	D3	U650C	F3	E3
R615	D3	E1	U650D	F3	E3
R710A	C4	E2	U710A	F4	E2
R710B	C4	E2	U720A	E3	E2
R710C	D4	E2	U720B	E4	E2
R710G	D2	E2	U720C	E3	E2
R720	D3	F2	U720D	E3	E2
R730	E2	F2	U730A	E3	E2
R731	F2	F2	U730B	E4	E2
R1310	B1	J2	U730C	E3	E2
R1450	B3	K3	U730D	E3	E2
R1501	E2	L1	U820A	D3	F2
			U830A	C3	F2
U210A	C1	B2	U830B	C3	F2
U300A	F1	C1	U910A	D2	G2
U320A	C3	C2	U910B	D2	G2
U330D	B1	C2	U1110B	C3	H2
U360D	E1	C3	U1200C	D2	I1
U400A	D3	C1	U1300B	E3	J1
U410C	D4	C2	U1400B	C2	J1
U430B	C1	C2	U1400C	C2	J1
U440B	E3	C3	U1410A	B1	J2
U450C	A1	C3	U1450B	B3	J3
U510	D4	D2	U1495B	C2	J5
U540F	B3	D3	U1500B	C2	K1
U610A	E4	E2	U1510	A1	K1
U610B	E4	E2	U1520F	B1	K2
U610C	E4	E2	U1550A	C2	K3
U610D	E4	E2			

Partial A11 also shown on diagrams 1, 5, 8, 9, 10, 11, 12, 13, 15, 16, and 17.



TYPE	Vcc +5V	GND	V$_{DD}$ +5V	Vss GND
4020			16	8
74LS00	14	7		
74LS02	14	7		
74LS04	14	7		
74LS08	14	7		
74LS11	14	7		
74LS20	14	7		
74LS21	14	7		
74LS32	14	7		
74LS73	4	11		
74LS74	14	7		
74LS86	14	7		
74LS132	14	7		
74LS193	16	8		
74LS257	16	8		
74LS279	16	8		

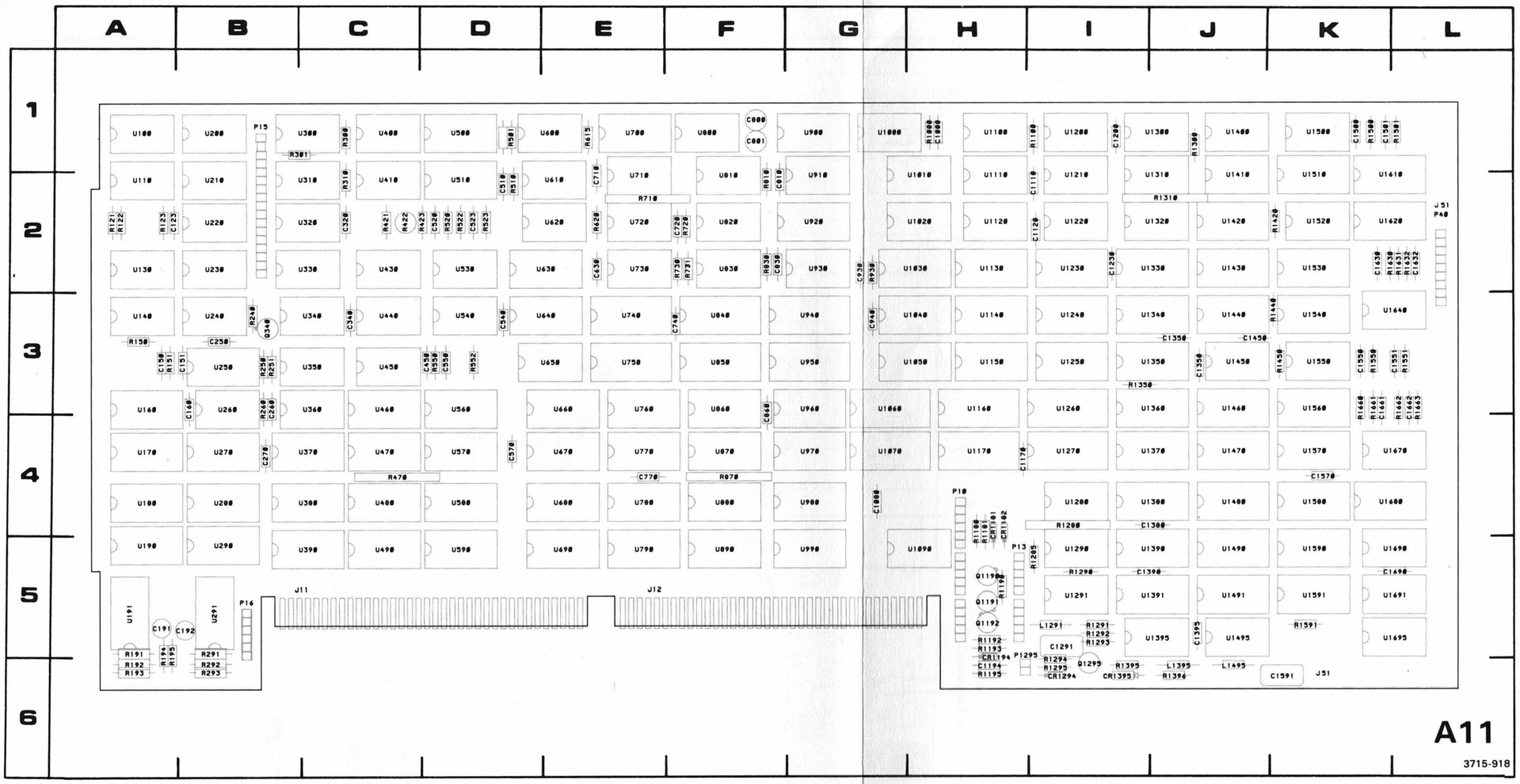


Figure 9-22. A11-Memory circuit board assembly.

Static Sensitive Devices
See Maintenance Section

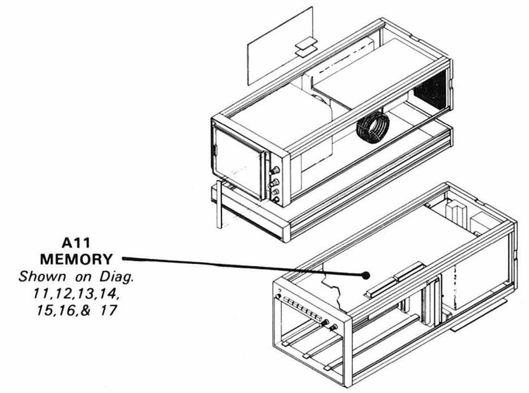
COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



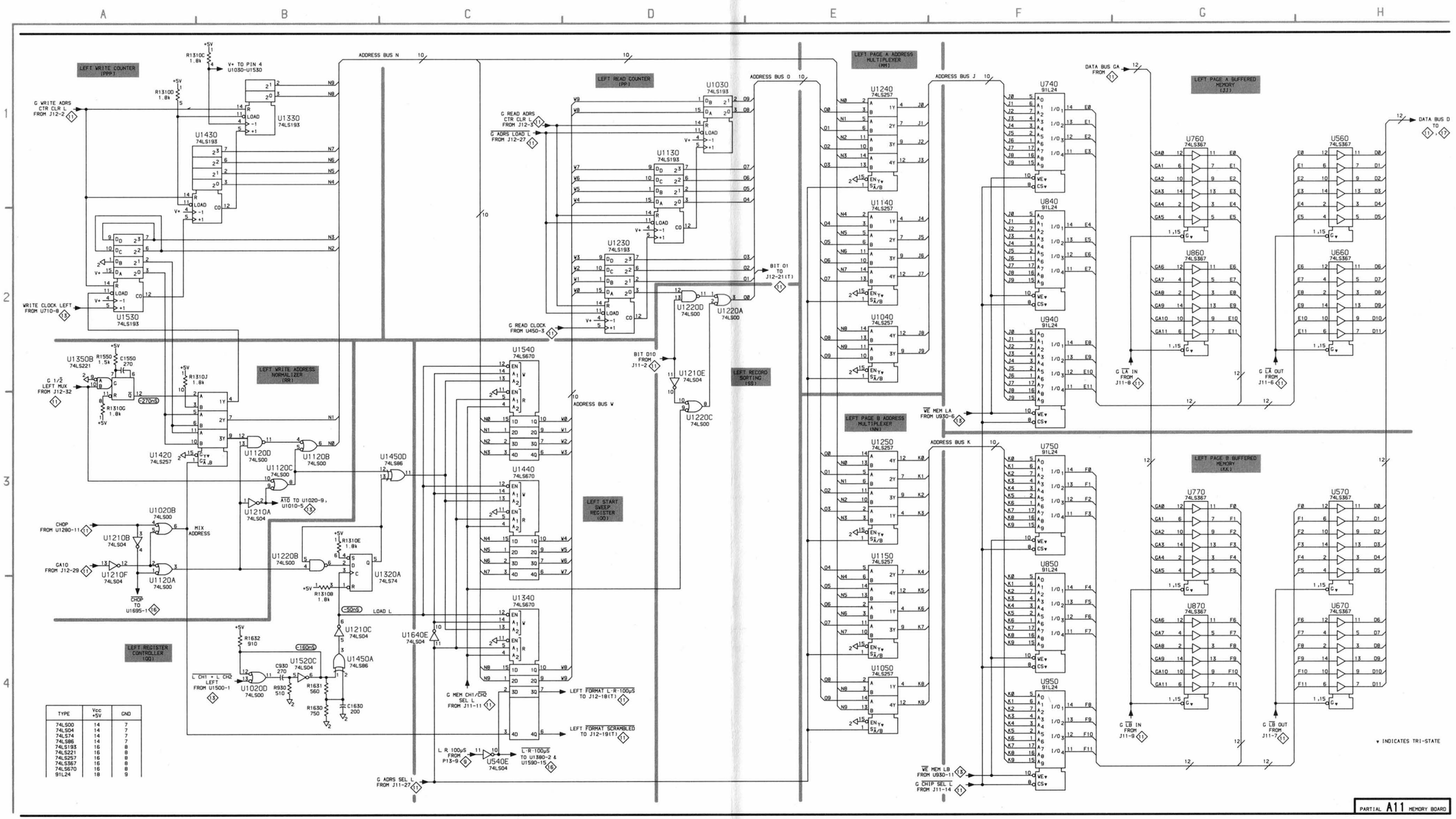
A11
MEMORY
Shown on Diag. 11,12,13,14, 15,16,& 17

LEFT MEMORY DIAGRAM 15

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C930	B4	G2	U1040	E2	H3
C1550	A2	K3	U1050	E4	H3
C1630	B4	K2	U1120A	A4	H2
			U1120B	B3	H2
R930	B4	G2	U1120C	B3	H2
R1310B	B4	J2	U1120D	B3	H2
R1310C	B1	J2	U1130	D1	H2
R1310D	A1	J2	U1140	31	H3
R1310E	B3	J2	U1150	E3	H3
R1310G	A3	J2	U1210A	B3	I2
R1310J	A2	J2	U1210B	A3	I2
R1550	A2	K3	U1210C	B4	I2
R1630	B4	K2	U1210E	D2	I2
R1631	B4	L2	U1210F	A3	I2
R1632	B4	L2	U1220A	D2	I2
			U1220B	B3	I2
U540E	C4	D3	U1220C	D3	I2
U560	H1	D3	U1220D	D2	I2
U570	H3	D4	U1230	D2	I2
U660	H2	E3	U1240	31	I3
U670	H4	E4	U1250	E3	I3
U740	F1	E3	U1320A	C3	J2
U750	F3	E3	U1330	B1	J2
U760	G1	E3	U1340	C4	J3
U770	G3	E4	U1350B	A2	J3
U840	F1	F3	U1420	A3	J2
U850	F3	F3	U1430	B1	J2
U860	G2	F3	U1440	C3	J3
U870	G4	F4	U1450A	B4	J3
U940	F2	G3	U1450D	C3	J3
U950	F4	G3	U1520C	B4	K2
U1020B	A3	H2	U1530	A2	K2
U1020D	B4	H2	U1540	C2	K3
U1030	D1	H2	U1640E	C4	L3

Partial A11 also shown on diagrams 1, 5, 8, 9, 10, 11, 12, 13, 14, 16, and 17.



TYPE	Vcc +5V	GND
74LS00	14	7
74LS04	14	7
74LS74	14	7
74LS86	14	7
74LS193	16	8
74LS221	16	8
74LS257	16	8
74LS367	16	8
74LS670	16	8
91L24	18	9

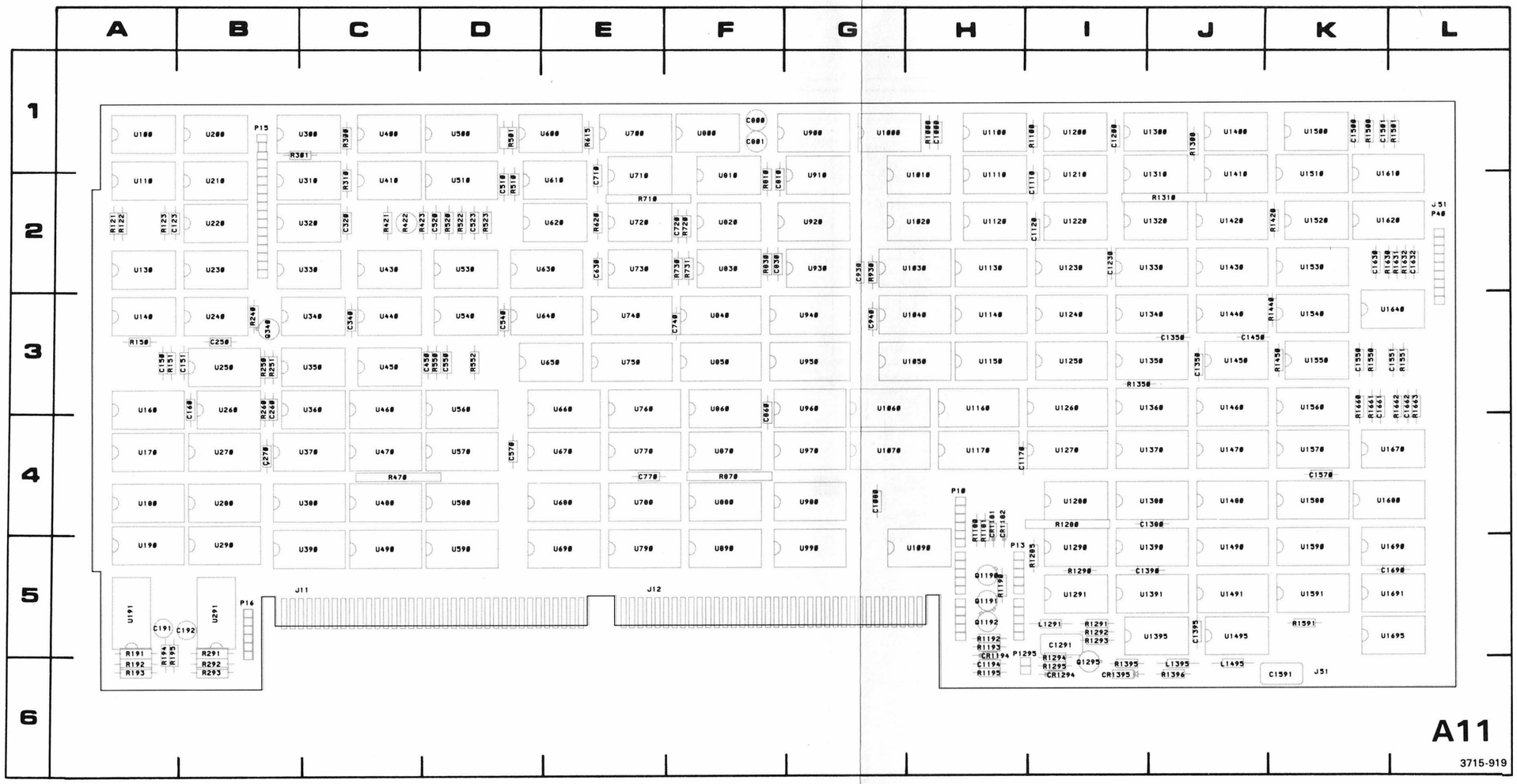


Figure 9-23. A11-Memory circuit board assembly.

A11-Memory
Circuit Bd Assembly

Static Sensitive Devices
See Maintenance Section

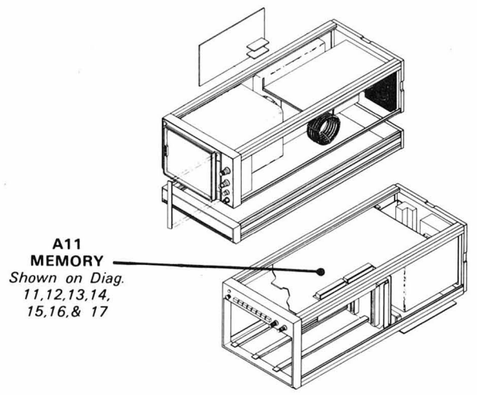
COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



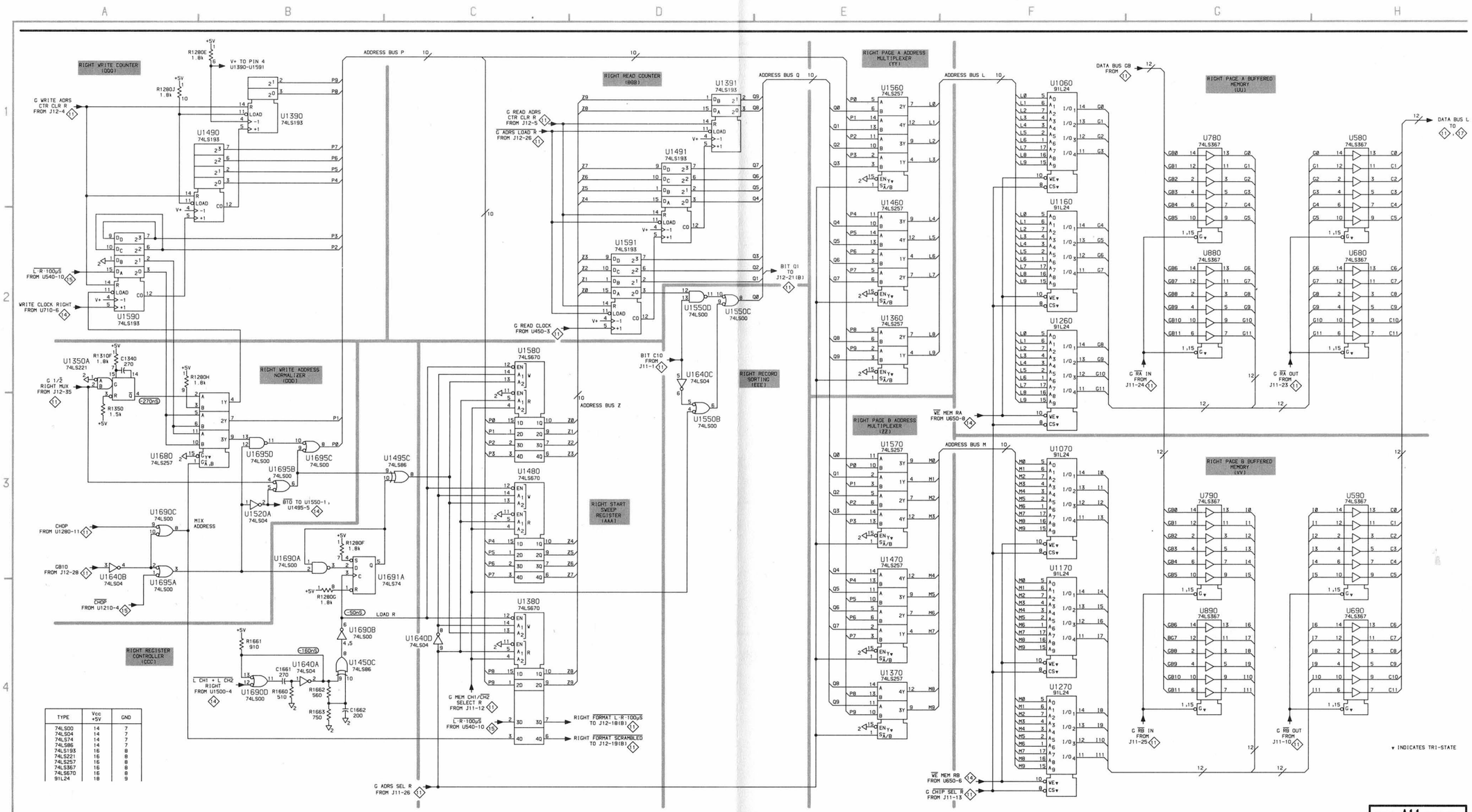
A11
MEMORY
Shown on Diag. 11,12,13,14, 15,16,& 17

RIGHT MEMORY DIAGRAM 16

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1661	B4	K3	U1390	B1	J5
C1662	B4	L3	U1391	D1	J5
			U1450C	B4	J3
R1280E	A1	I4	U1470	E3	J4
R1280F	B3	I4	U1480	C3	J4
R1280G	B4	I4	U1490	B1	J5
R1280H	A2	I4	U1491	D1	J5
R1280J	A1	I4	U1495C	C3	J5
R1310F	A2	J2	U1520A	B3	K2
R1350	A3	I3	U1550B	D3	K3
R1660	B4	K3	U1550C	D2	K3
R1661	B4	K3	U1550D	D2	K3
R1662	B4	L3	U1560	E1	K3
R1663	B4	L3	U1570	E3	K4
			U1580	C2	K4
U580	H1	D4	U1590	A2	K5
U590	H3	D5	U1591	D2	K5
U680	H2	E1	U1640A	B4	L3
U690	H4	E5	U1640B	A3	L3
U780	G1	E4	U1640C	D2	L3
U790	G3	E5	U1640D	C4	L3
U800	G2	F1	U1640	E1	L3
U890	G4	F5	U1680	A3	L4
U1060	F1	G3	U1690A	B3	L5
U1070	F3	G4	U1690B	B4	L5
U1160	F1	H3	U1690C	A3	L5
U1170	F3	H4	U1690D	B4	L5
U1260	F2	I3	U1691A	C3	L5
U1270	E4	I4	U1695A	A4	L5
U1350A	A2	J3	U1695B	B3	L5
U1360	E2	J3	U1695C	B3	L5
U1370	E4	J4	U1695D	B3	L5
U1380	C4	J4			

Partial A11 also shown on diagrams 1, 5, 8, 9, 10, 11, 12, 13, 14, 15, and 17.



TYPE	Vcc +5V	GND
74LS00	14	7
74LS04	14	7
74LS74	14	7
74LS86	14	7
74LS193	16	8
74LS221	16	8
74LS257	16	8
74LS367	16	8
74LS670	16	8
91L24	18	9

5223 Option 10

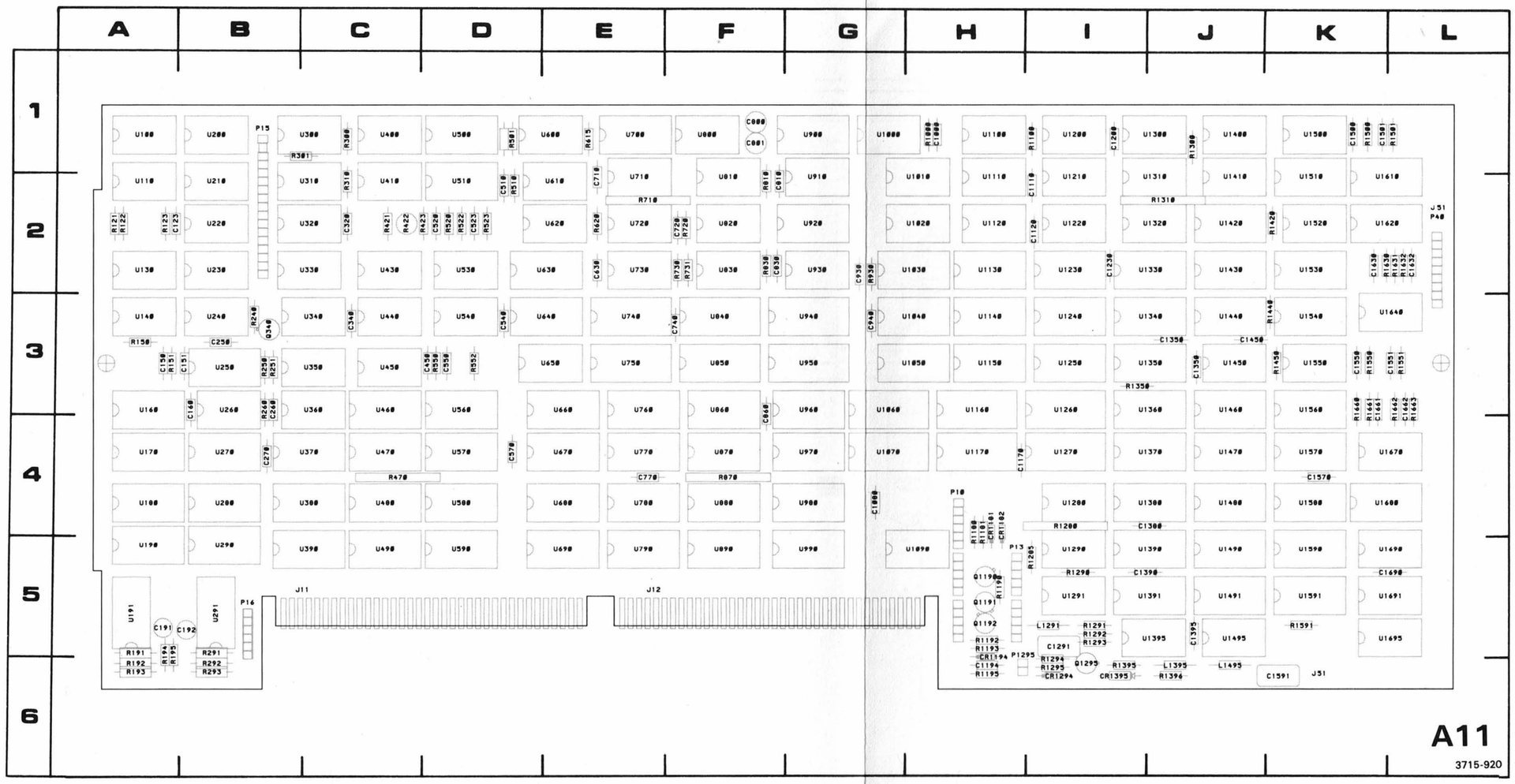


Figure 9-24. A11-Memory circuit board assembly.

Static Sensitive Devices
See Maintenance Section

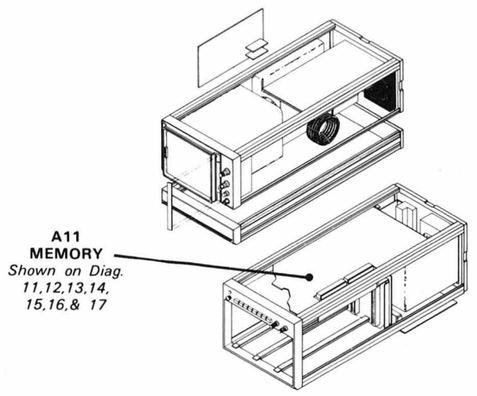
COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



A11
MEMORY
Shown on Diag. 11,12,13,14, 15,16,& 17

MEMORY DISPLAY MULTIPLEXERS AND DAC'S

DIAGRAM 17

ASSEMBLY A10

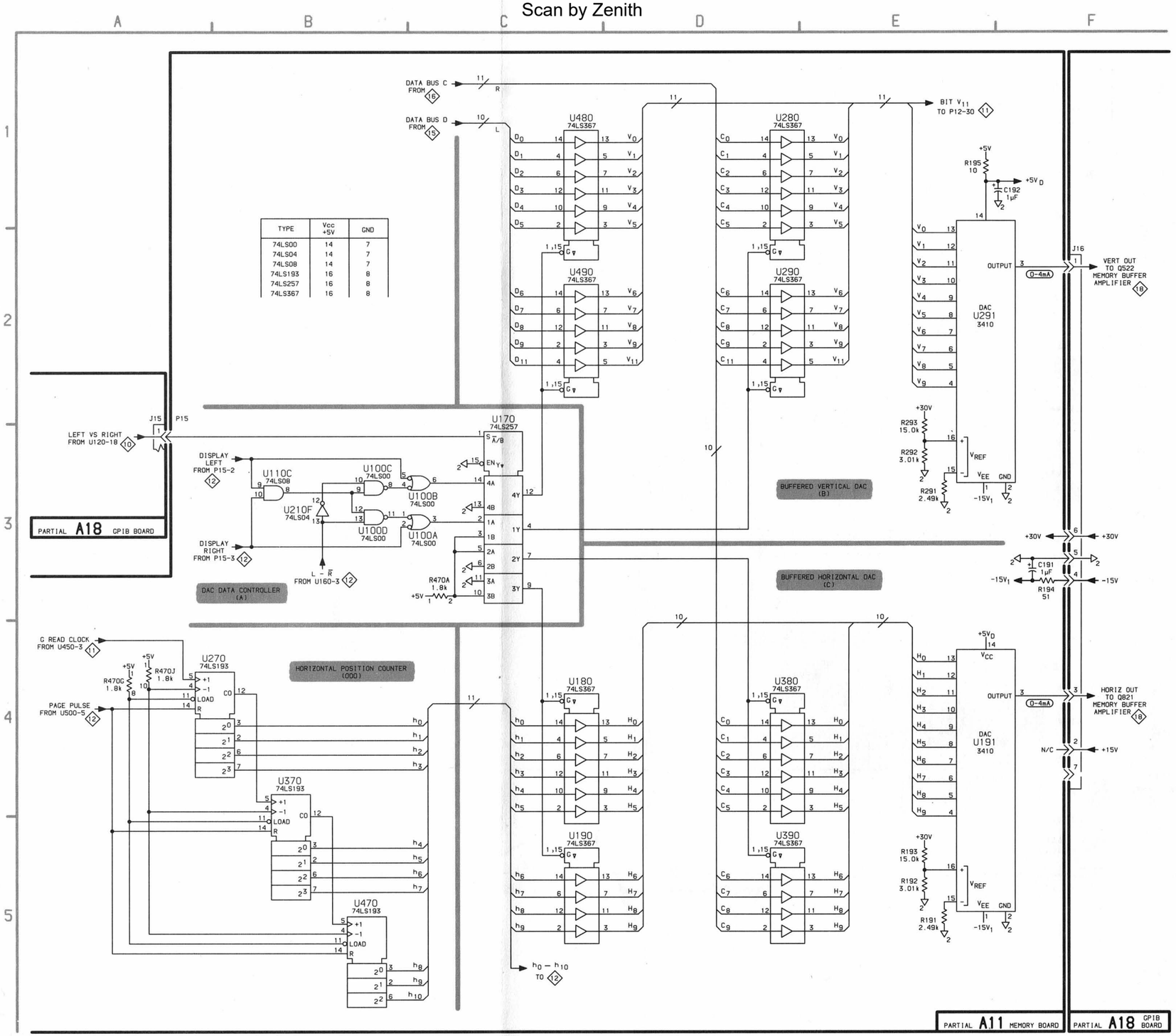
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J15	A2	B3	J16	F2	G4

Partial A10 also shown on diagrams 7, 10, 12 and 18.

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C191	F3	A5	U100C	B3	A4
C192	F1	B5	U100D	B3	A4
			U110C	B3	A2
P15	A2	B1	U170	C2	A4
			U180	C4	A1
R191	E5	A5	U190	C5	A5
R192	E5	A6	U191	E4	A5
R193	E5	A6	U210F	B3	B2
R194	F3	A5	U270	B4	B4
R195	E1	A5	U280	D1	B4
R291	E3	B5	U290	D2	B5
R292	E3	B6	U291	E2	B5
R293	E2	B6	U370	B4	C4
R470A	C3	C4	U380	D4	C4
R470G	A4	C4	U390	D5	C5
R470J	A4	C4	U470	B5	C4
			U480	C1	C4
U100A	C3	A4	U490	C2	C5
U100B	C3	A4			

Partial A11 also shown on diagrams 1, 5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.



TYPE	Vcc +5V	GND
74LS00	14	7
74LS04	14	7
74LS08	14	7
74LS193	16	8
74LS257	16	8
74LS367	16	8

A18—GPIB
Circuit Bd Assembly

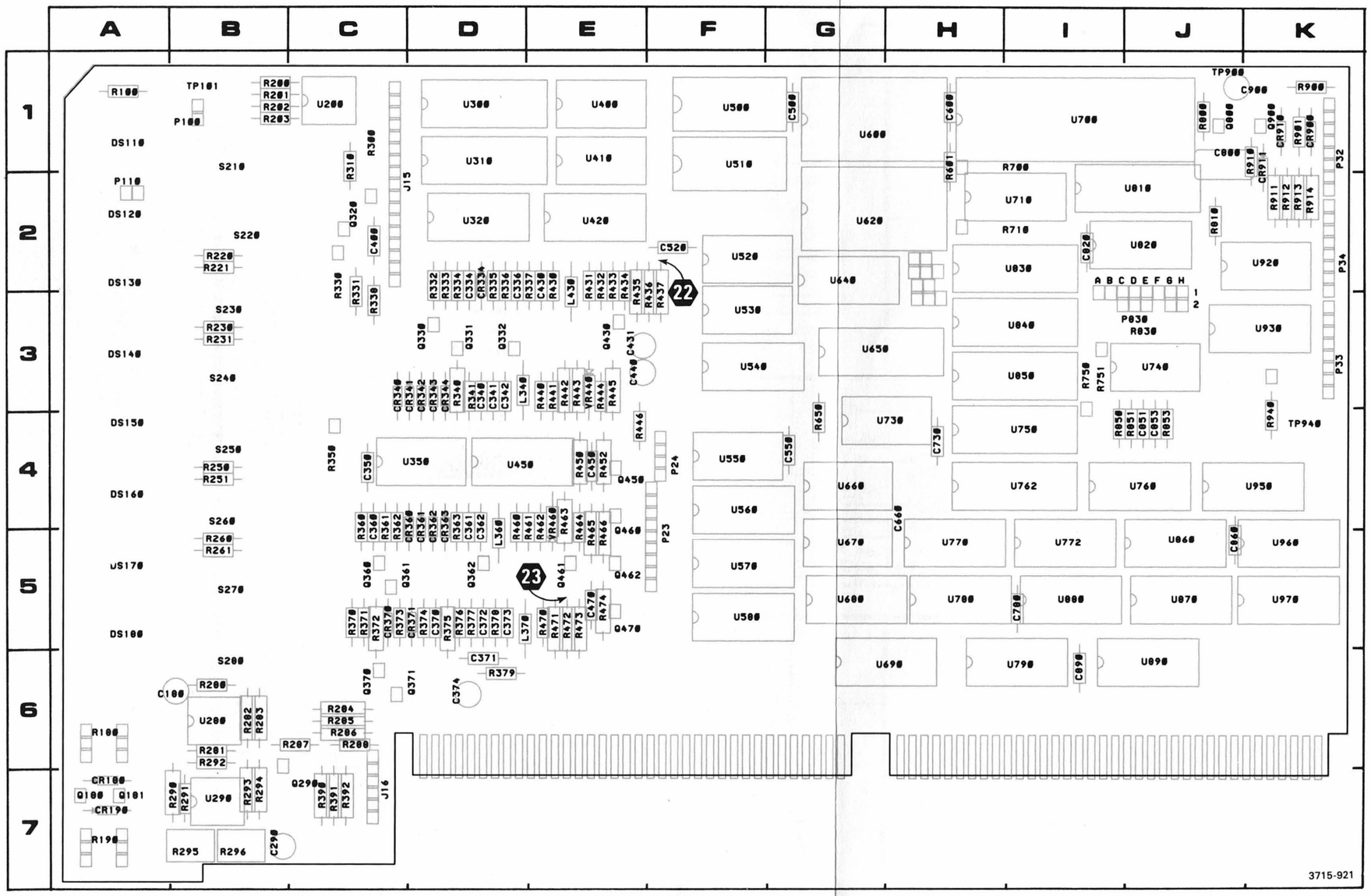


Figure 9-25. A18-GPIB circuit board assembly.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

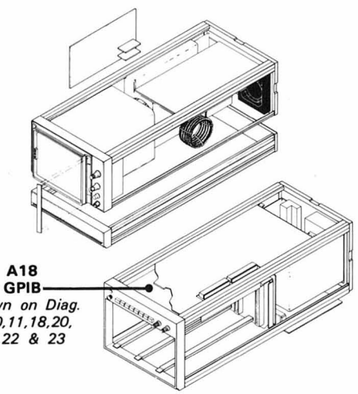
@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

MEMORY BUFFER A

ASSEMBLY A18

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C180	E2	A6
C2:0	E3	B7
C334	B1	D2
C336	C2	D2
C340	C1	D3
C341	D2	D3
C342	D1	D3
C350	C5	C4
C360	C5	C4
C361	D4	D4
C362	D4	D4
C370	B4	D5
C371	C3	D6
C372	C4	D5
C373	C4	D5
C374	A4	D6
C430	C2	E2
C431	B5	E3
C440	A5	E3
C450	E2	E4
C470	E3	E5
CR180	B2	A7
CR190	B4	A7
CR334	B1	D2
CR340	B2	C3
CR341	B1	D3
CR342	B1	D3
CR343	B1	D3
CR344	B1	D3
CR360	B3	D4
CR361	B3	D4
CR362	B3	D4
CR363	B3	D4
CR370	B4	C5
CR371	B4	D5
J16	A1	C7
L340	D1	D3
L360	D4	D4
L370	C4	D5
L430	C1	E2
P23	F1	F4
P24	A4	F4
Q180	C4	A7
Q181	C4	A7
Q290	C3	B7
Q330	B1	D2
Q331	C1	D2
Q332	C1	D3
Q360	D2	D3
Q361	D1	D3
Q362	C5	C4
Q370	C5	C4
Q371	D4	D4
Q430	D4	D4
Q450	B4	D5
Q460	C3	D6
Q461	C4	D5
Q462	C4	D5
Q470	A4	D6
	C2	E2
R180A	B5	E3
R180B	A5	E3
R190A	E2	E4
R190B	E3	E5
R280	B2	A7
R281	B4	A7
R282	B1	D2
R283	B2	C3
R284	B1	D3
R285	B1	D3
R286	B1	D3
R287	B1	D3
R290	B3	D4
R291	B3	D4
R292	B3	D4
R293	B3	D4
R294	B4	C5
R295	B4	D5
R296		
R333		
R334		
R335		
R336		
R337		
R340		
R341		
R360		
R361		
R362		
R363		
R370		

Partial A18 also shown on diagrams 10, 21, 22 and 2



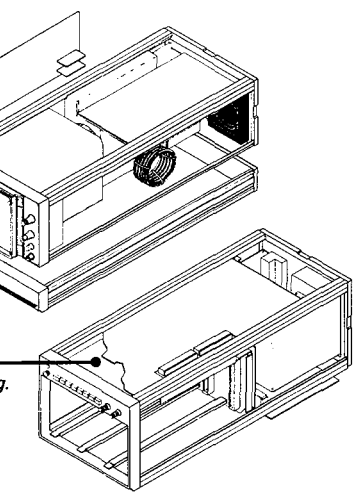
A18
GPIB
Shown on Diag. 7,10,11,18,20, 21,22 & 23

MEMORY BUFFER AMPLIFIERS DIAGRAM 18

ASSEMBLY A18

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C180	E2	A6
C2;0	E3	B7
C334	B1	D2
C336	C2	D2
C340	C1	D3
C341	D2	D3
C342	D1	D3
C350	C5	C4
C360	C5	C4
C361	D4	D4
C362	D4	D4
C370	B4	D5
C371	C3	D6
C372	C4	D5
C373	C4	D5
C374	A4	D6
C430	C2	E2
C431	B5	E3
C440	A5	E3
C450	E2	E4
C470	E3	E5
CR180	B2	A7
CR190	B4	A7
CR334	B1	D2
CR340	B2	C3
CR341	B1	D3
CR342	B1	D3
CR343	B1	D3
CR344	B1	D3
CR360	B3	D4
CR361	B3	D4
CR362	B3	D4
CR363	B3	D4
CR370	B4	C5
CR371	B4	D5
J16	A1	C7
L340	D1	D3
L360	D4	D4
L370	C4	D5
L430	C1	E2
P23	F1	F4
P24	A4	F4
Q180	C4	A7
Q181	C2	A7
Q290	A5	C7
Q330	C1	D3
Q331	B1	D3
Q332	C1	D3
Q360	C1	C5
Q361	C4	C5
Q362	C3	D5
Q370	B3	C6
Q371	C3	D6
Q430	D1	E3
Q450	E2	E4
Q460	E1	E4
Q461	D4	E5
Q462	E4	E5
Q470	E3	E5
R180A	B2	A6
R180B	B1	A6
R190A	B4	A7
R190B	B3	A7
R280	B1	B6
R281	B4	B6
R282	B2	B6
R283	B3	B6
R284	B1	C6
R285	C2	C6
R286	C1	C6
R287	B5	C6
R290	D2	B7
R291	E2	B7
R292	E3	B6
R293	D2	B7
R294	A5	B7
R295	D2	B7
R296	D3	B7
R333	B1	D2
R334	B1	D2
R335	C1	D2
R336	C1	D2
R337	C1	E2
R340	C1	D3
R341	C1	D3
R360	C5	C4
R361	C5	C4
R362	C5	C4
R363	C3	D4
R370	C1	C5
R371	C3	C5
R372	C3	C5
R373	B4	C5
R374	B4	D5
R375	B3	D5
R376	C4	D5
R377	C4	D5
R378	C4	D5
R379	A4	D6
R390	A5	C7
R391	C4	C7
R392	C4	C7
R430	C2	E2
R435	D1	E2
R436	D1	F2
R437	E1	F2
R442	D1	E3
R443	E2	E3
R444	E2	E3
R445	E2	E3
R446	A5	E4
R450	E1	E4
R452	E2	E4
R463	E3	E4
R464	E3	E4
R465	D3	E4
R466	D4	E4
R470	C4	E5
R471	D3	E5
R472	E3	E5
R473	E3	E5
R474	E3	E5
U280A	B4	B6
U280B	B1	B6
U290A	E2	B7
U290B	E3	B7
U350A	D3	D4
U350B	D4	D4
U350C	D1	D4
U350D	D1	D4
U350	C5	D4
U450C	E3	D4
U450D	E2	D4
U450	E4	D4
VR440	E2	E3
VR460	E3	E4

Partial A18 also shown on diagrams 10, 21, 22 and 23.



VOLTAGE AND WAVEFORM CONDITIONS

Voltage Conditions. The test voltages (circled numbers) on the schematic were taken using a digital multimeter with 10 MΩ input impedance (TEKTRONIX DM501A Digital Multimeter installed in a TM501 Power Module or a TEKTRONIX 7D13 Digital Multimeter used with a readout equipped 7000-series oscilloscope).

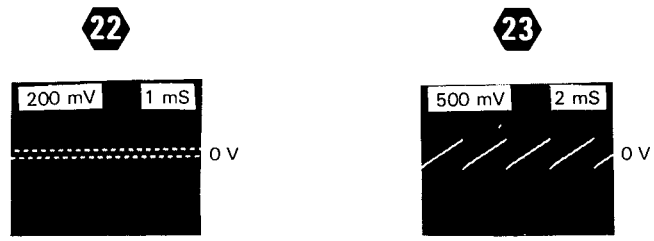
No plug-in units were installed.

Waveform Conditions. A 5B25N Digitizer Time Base/Ampl with controls set as follows: Time/Div (1 ms), Chop (In), Triggering (AC, Auto, Left) and two 5000-series vertical amplifiers with controls set as follows: Volts/Div (1V), Display (On) were installed in the appropriate compartments of the 5223.

The 5223 controls were set as follows: Memory Contents pushbuttons—Display, either left or right (in) Vert Mode (in). All other buttons (out).

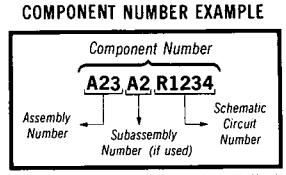
The waveforms were monitored using a test oscilloscope system with 10 MΩ input impedance, at least 60 MHz bandwidth and 10X probe (TEKTRONIX 7603 Oscilloscope, 7B92A Time Base, 7A13 Differential Comparator and P6062B Probe).

Refer to the individual waveform photos for deflection factor and sweep rate settings.

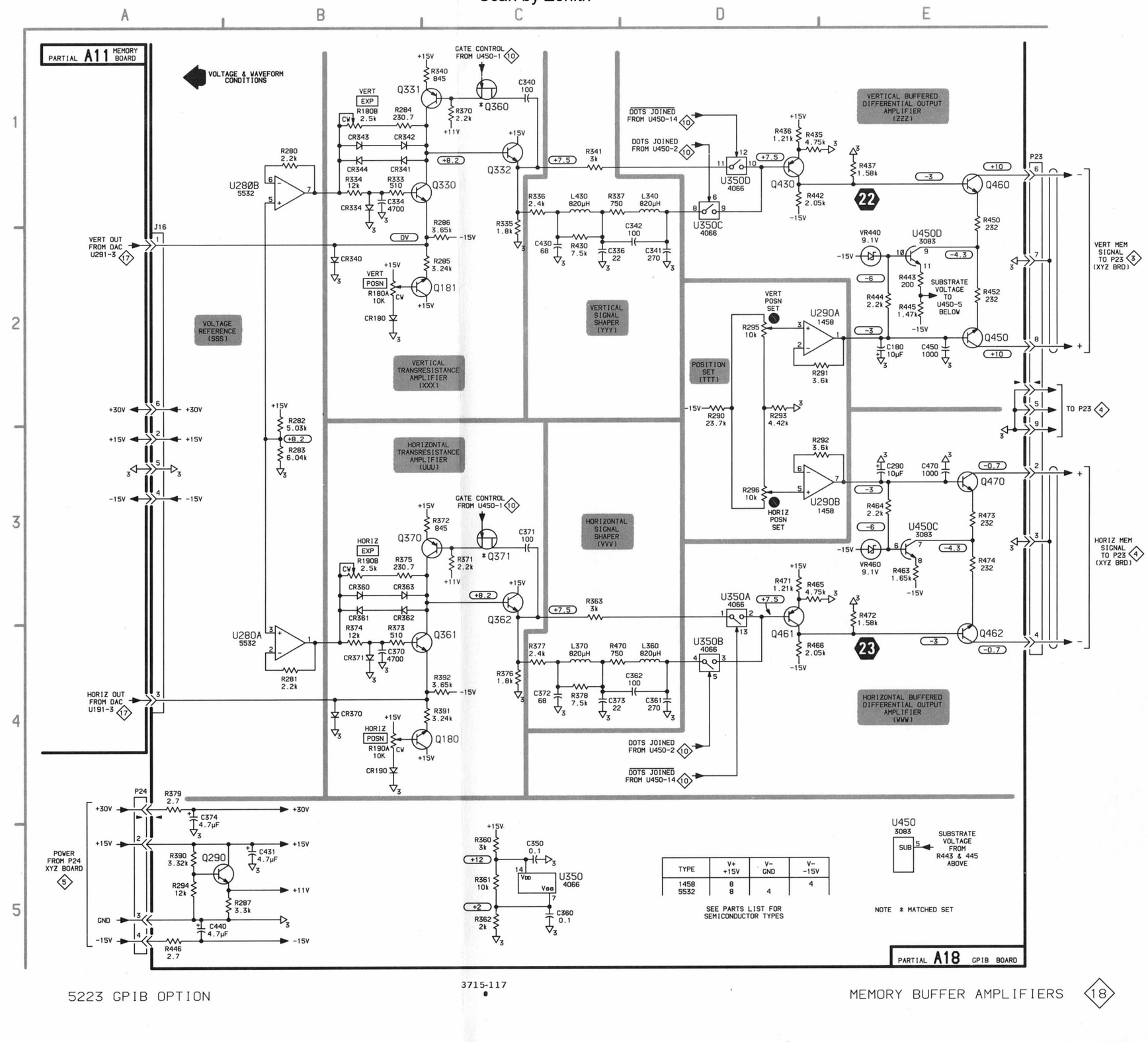


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



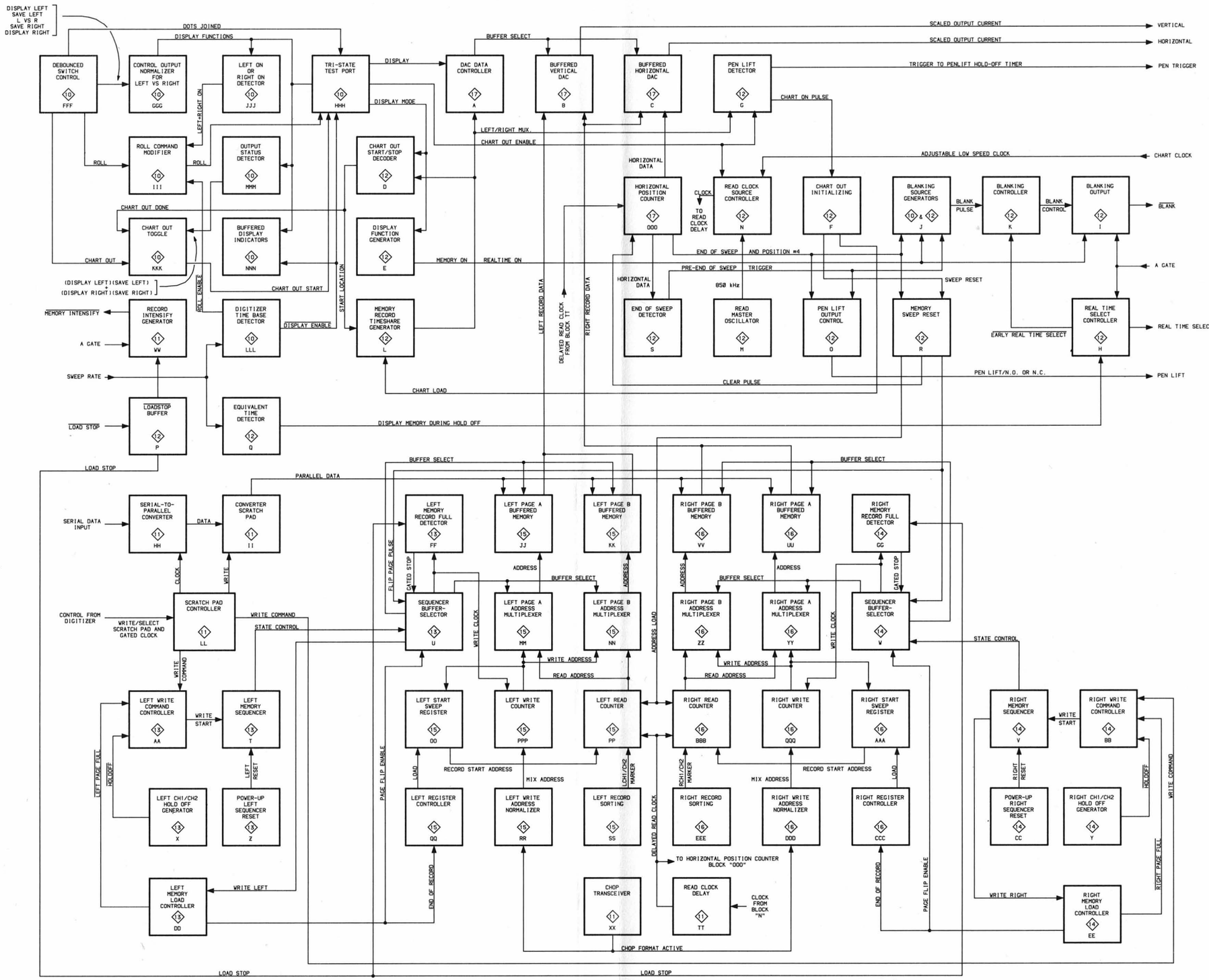
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

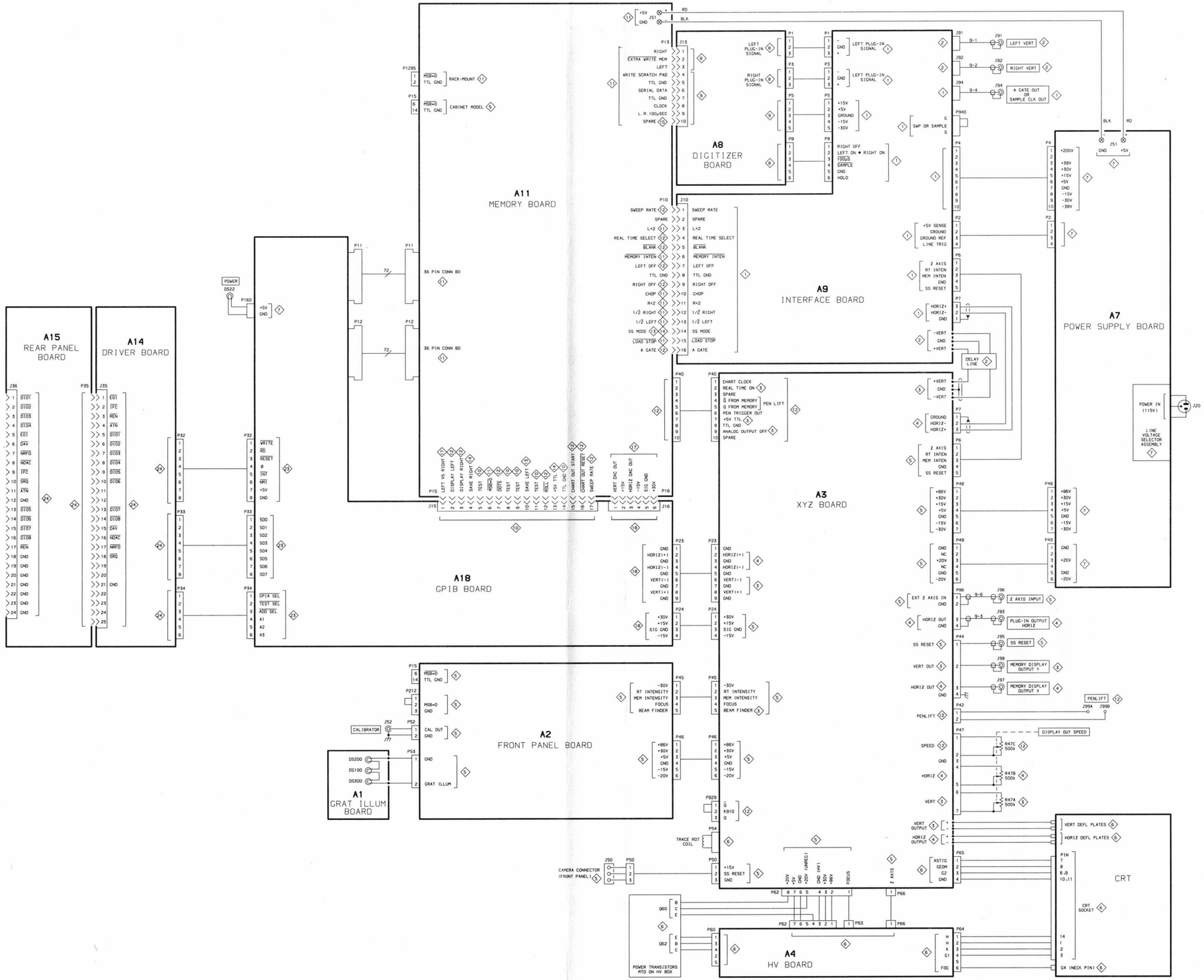


TYPE	V+ +15V	V- GND	V- -15V
1458	8		
5532	8	4	4

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

NOTE * MATCHED SET





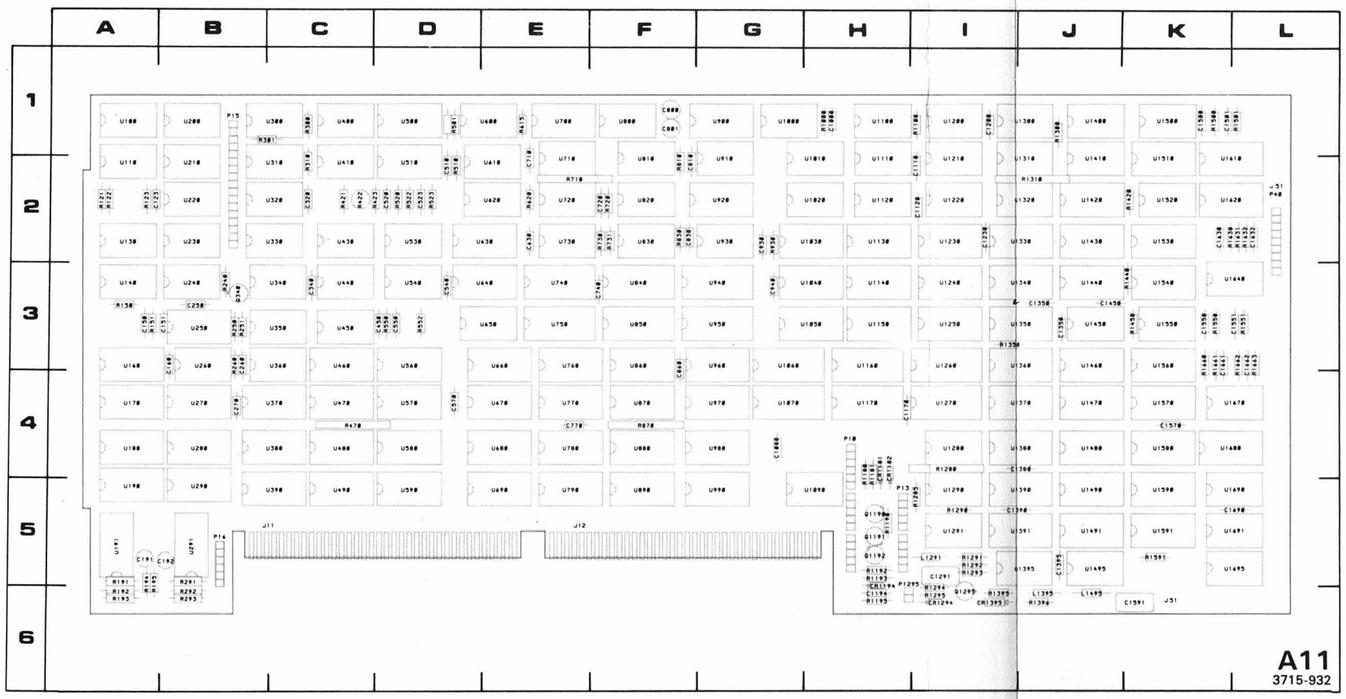
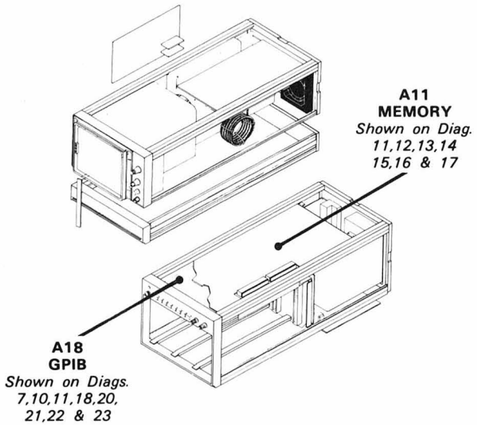


Figure 9-26. A11-Memory circuit board assembly.



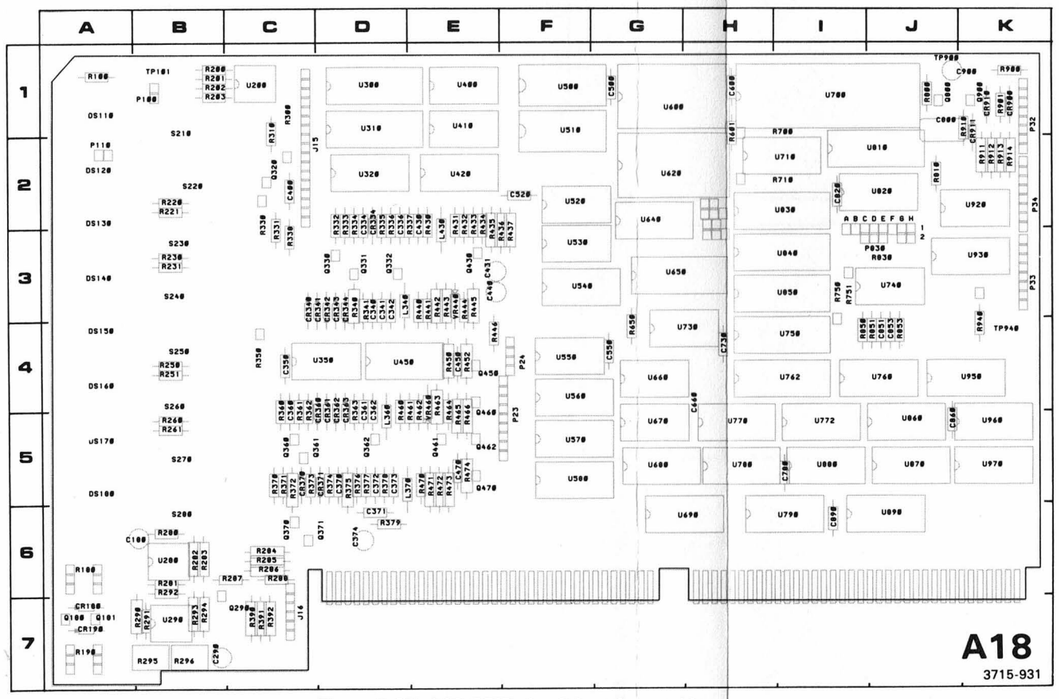


Figure 9-27. A18-GPIB circuit board assembly.

GPIB DATA BUS / MEMORY BOARD INTERFACE DIAGRAM 21

ASSEMBLY A18

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R850	C2	I4
U560	C4	F4
U570	C3	F5
U580	C2	F5
U670A	B2	G5
U670B	C2	G5
U680	G2	G5
U690	G1	H6
U730C	D1	H4
U760	D2	J4
U762	D1	I4
U770	G2	H5
U772	G5	I5
U780	G4	H5
U790	G3	I6

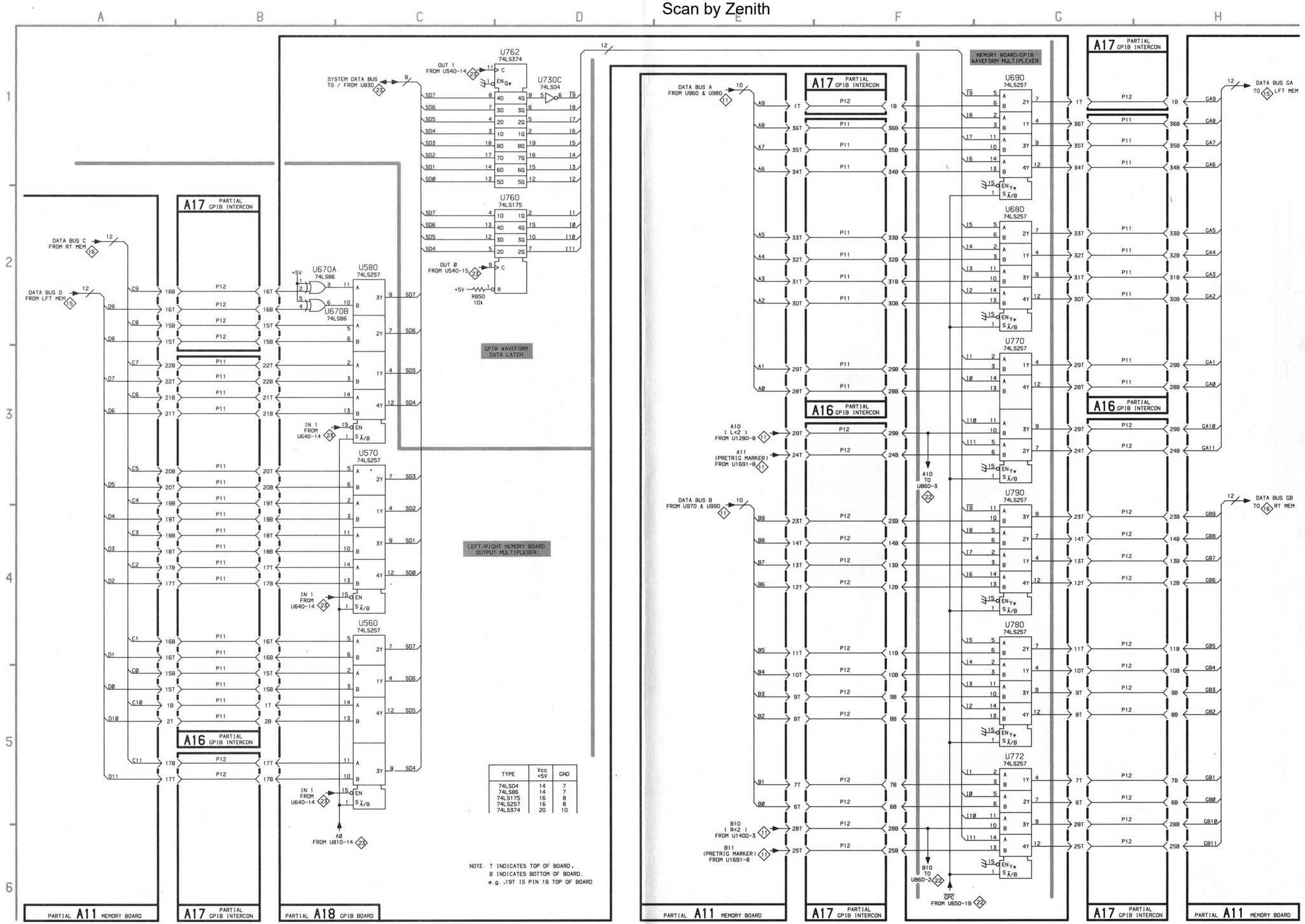
Partial A18 also shown on diagrams 10, 18, 22 and 23.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



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5223 GPIB OPTION

GPIB DATA BUS/MEMORY BOARD INTERFACE 21

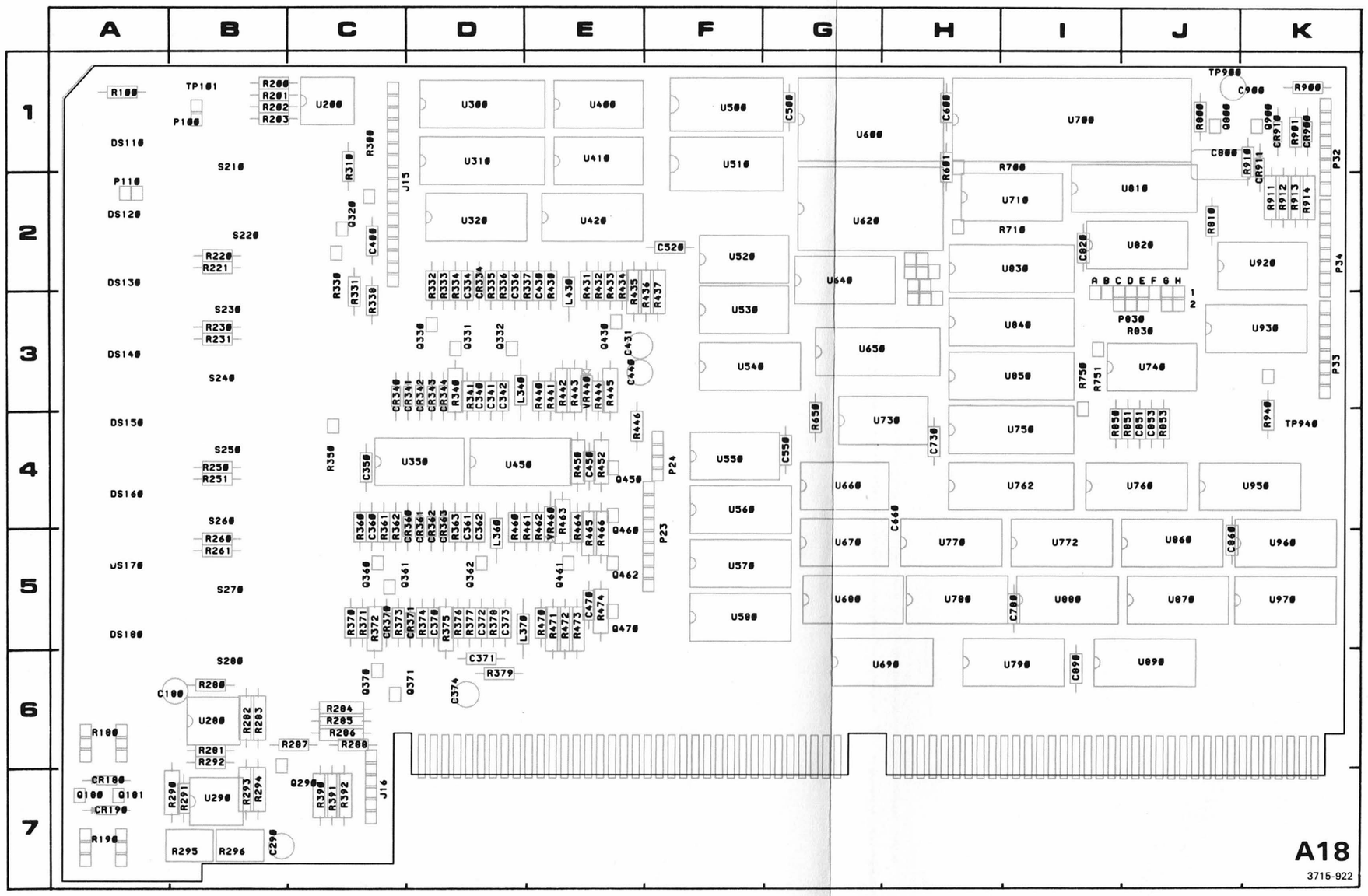


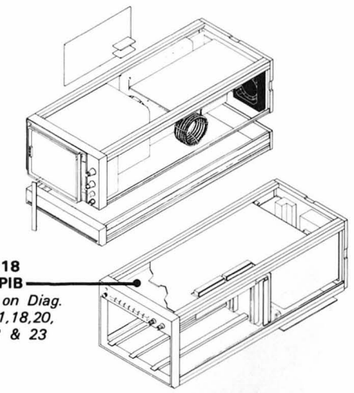
Figure 9-28. A18-GPIB circuit board assembly.

GPIB BOARD / MEMORY BOARD INTERFACE DIA

ASSEMBLY A18

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C851	E4	J4	U660D	D2	G4
C853	E4	J4	U670C	C1	G5
			U670D	C1	G5
R650	G5	G4	U730A	G4	H4
R750A	E5	I3	U730B	G4	H4
R750B	E4	I3	U730D	G5	H4
R750C	G5	I3	U730E	G4	H4
R750D	G4	I3	U740A	D4	J3
R750E	E5	I3	U740B	E4	J3
R751A	F3	I3	U740C	D4	J3
R751D	F3	I3	U740D	D4	J3
R830E	G4	J3	U750	C3	I4
R830F	E3	J3	U840	E3	I3
R851	E4	J4	U850	E4	I3
R853	E4	J4	U860	B2	J5
R940	B5	K4	U870	G1	J5
			U880	B4	I5
U550A	C1	F4	U890	B3	J6
U550B	C1	F4	U920B	B5	K2
U550C	D1	F4	U920C	F1	K2
U550D	D1	F4	U930A	F3	K3
U650	C2	G3	U950A	B5	K4
U660A	D2	G4	U960	G2	K5
U660B	D2	G4	U970	G1	K5
U660C	D2	G4			

Partial A18 also shown on diagrams 10, 18, 21 and 23.



Static Sensitive Devices
See Maintenance Section

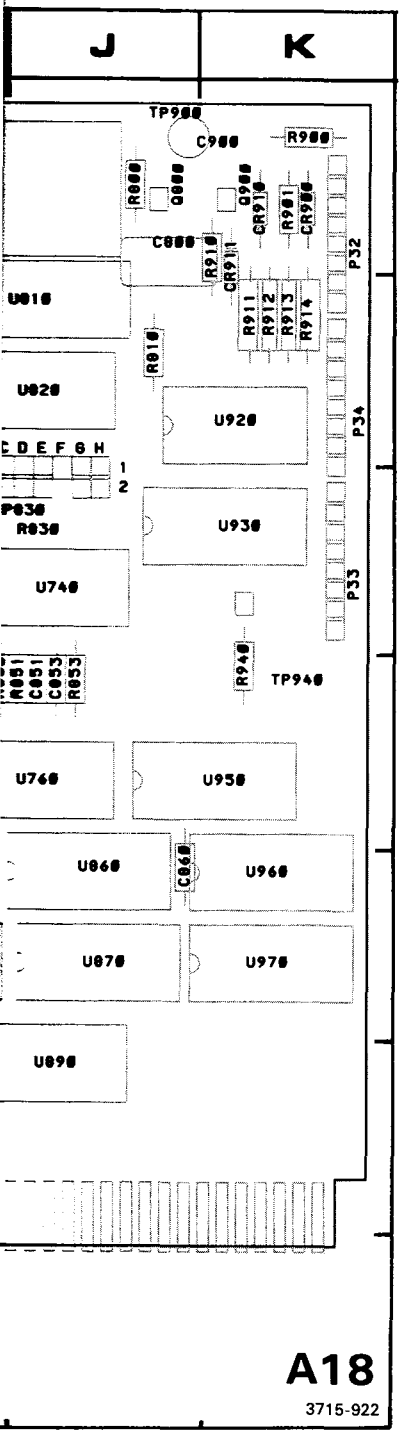
COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

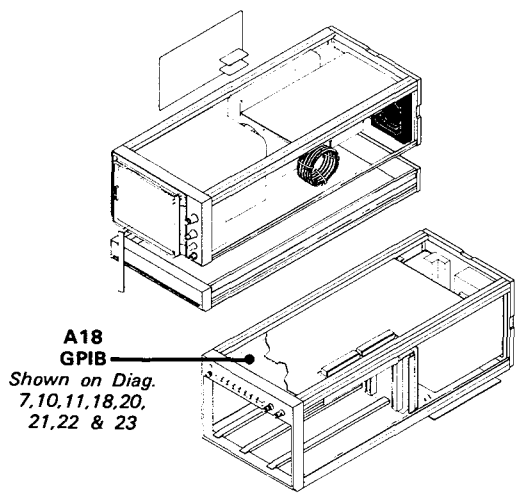


GPIB BOARD / MEMORY BOARD INTERFACE DIAGRAM 22

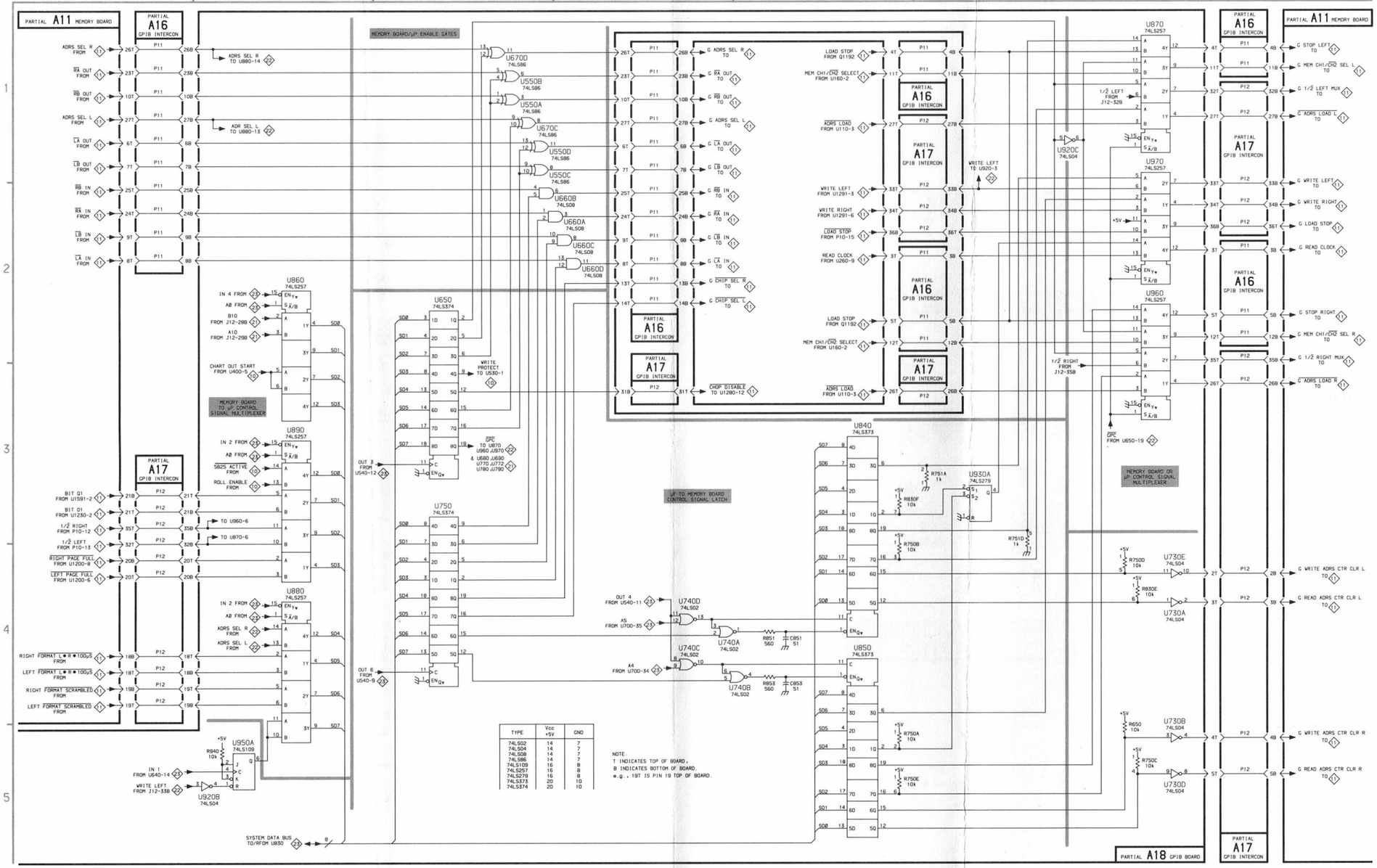
ASSEMBLY A18

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C851	E4	J4	U660D	D2	G4
C853	E4	J4	U670C	C1	G5
			U670D	C1	G5
R650	G5	G4	U730A	G4	H4
R750A	E5	I3	U730B	G4	H4
R750B	E4	I3	U730D	G5	H4
R750C	G5	I3	U730E	G4	H4
R750D	G4	I3	U740A	D4	J3
R750E	E5	I3	U740B	E4	J3
R751A	F3	I3	U740C	D4	J3
R751D	F3	I3	U740D	D4	J3
R830E	G4	J3	U750	C3	I4
R830F	E3	J3	U840	E3	I3
R851	E4	J4	U850	E4	I3
R853	E4	J4	U860	B2	J5
R940	B5	K4	U870	G1	J5
			U880	B4	I5
U550A	C1	F4	U890	B3	J6
U550B	C1	F4	U920B	B5	K2
U550C	D1	F4	U920C	F1	K2
U550D	D1	F4	U930A	F3	K3
U650	C2	G3	U950A	B5	K4
U660A	D2	G4	U960	G2	K5
U660B	D2	G4	U970	G1	K5
U660C	D2	G4			

Partial A18 also shown on diagrams 10, 18, 21 and 23.



A18
GPIB
Shown on Diag. 7,10,11,18,20, 21,22 & 23



5223 GPIB OPTION

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GPIB BD/MEMORY BD INTERFACE 22

22 GPIB Bd/Memory Bd Interface | Reverse Side A18

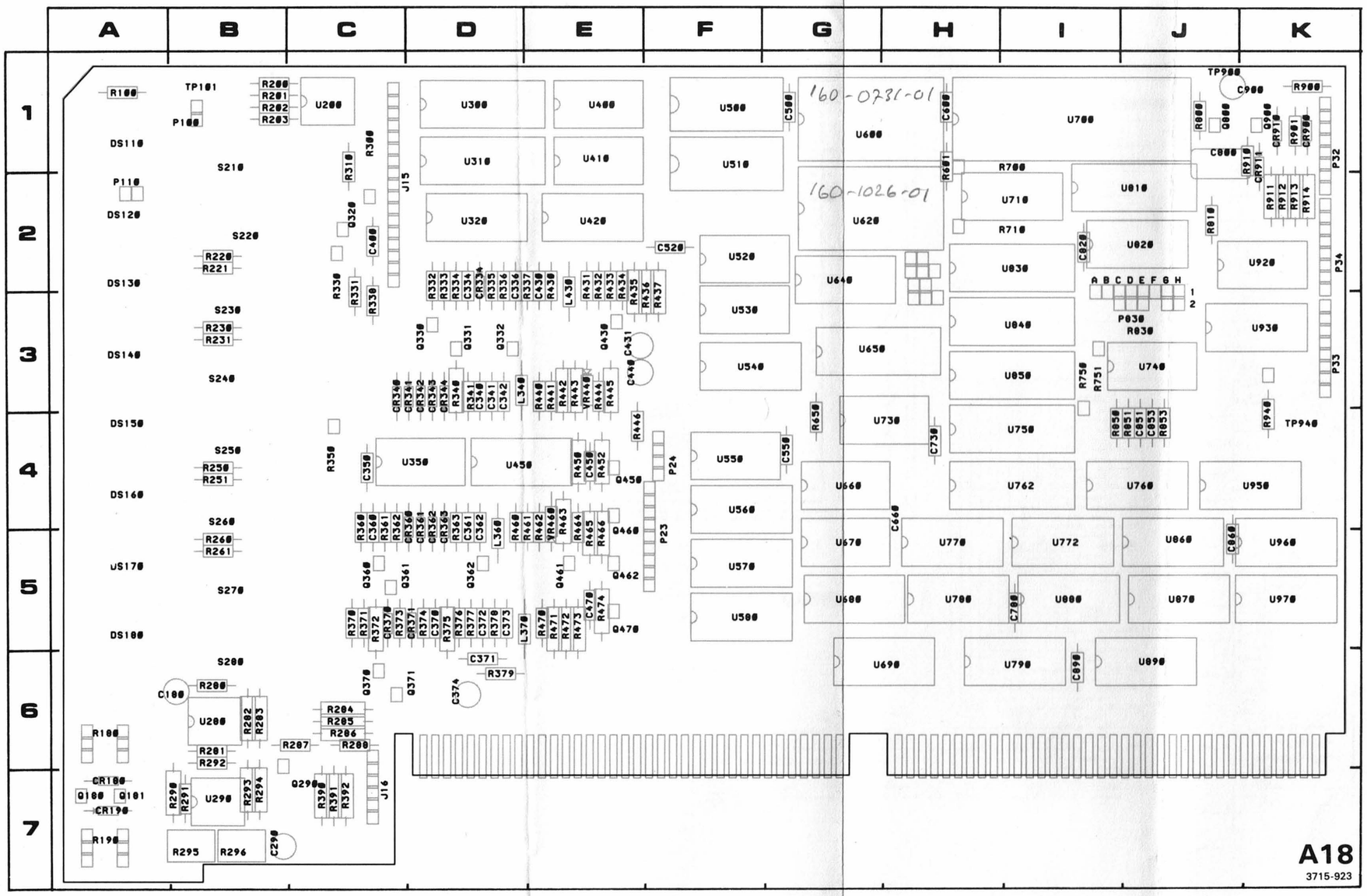


Figure 9-29. A18-GPIB circuit board assembly.

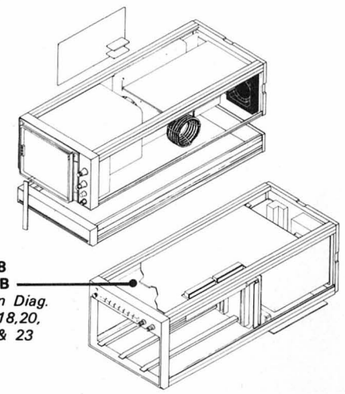
A18—GPIB Circuit Bd Assembly

CENTRAL PROCESSING UNIT DIAGRAM

ASSEMBLY A18

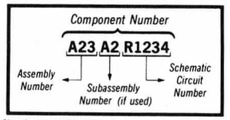
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C600	B1	H1
C800	A4	J1
C900	B4	K1
CR900	B4	K1
CR910	A2	K1
CR911	A2	K1
P32	F6	K1
P33	F1	K3
P34	F2	K2
P110	B4	A2
Q800	A4	J1
Q900	A4	K1
R601	A2	H1
R700	C1	I1
R710	D1	I2
R800	B4	J1
R810	B1	J2
R830A	B2	J3
R830G	D6	J3
R830J	D6	J3
R830	D2	J3
R900	B4	K1
R901	F6	K1
R910	A2	K1
R911	A4	K2
R912	A4	K2
R913	A4	K2
R914	A4	K2
U400B	A2	E1
U500	E5	F1
U510	E5	F1
U520C	D5	F2
U520D	E2	F2
U530C	D5	F3
U530D	E2	F3
U540	F4	F3
U600	D3	G1
U620	D4	G2
U640	F3	G2
U700		
U710		
U810A		
U810B		
U810C		
U810D		
U810E		
U810F		
U810G		
U810H		
U820		
U830		
U920A		
U920D		
U920E		
U920F		
U930B		
U930C		
U930D		
U950B		

Partial A18 also shown on diagrams 10, 18, 21 and 22.

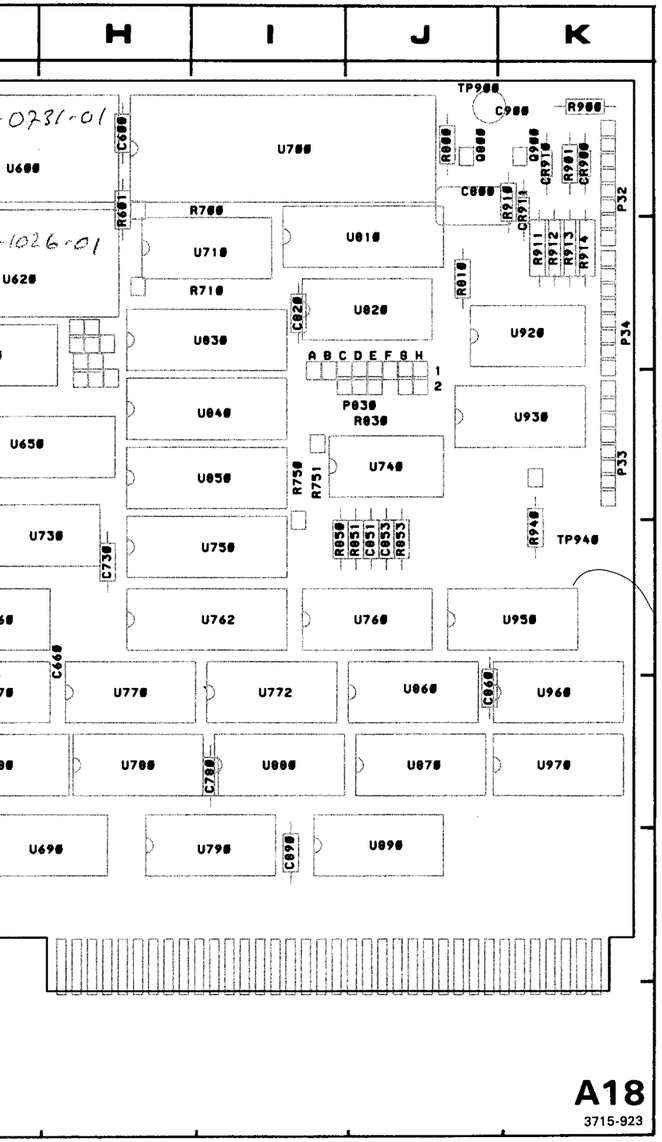


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

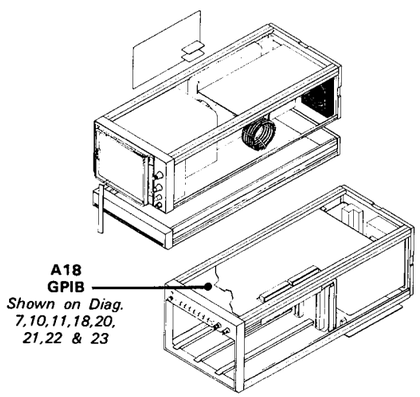


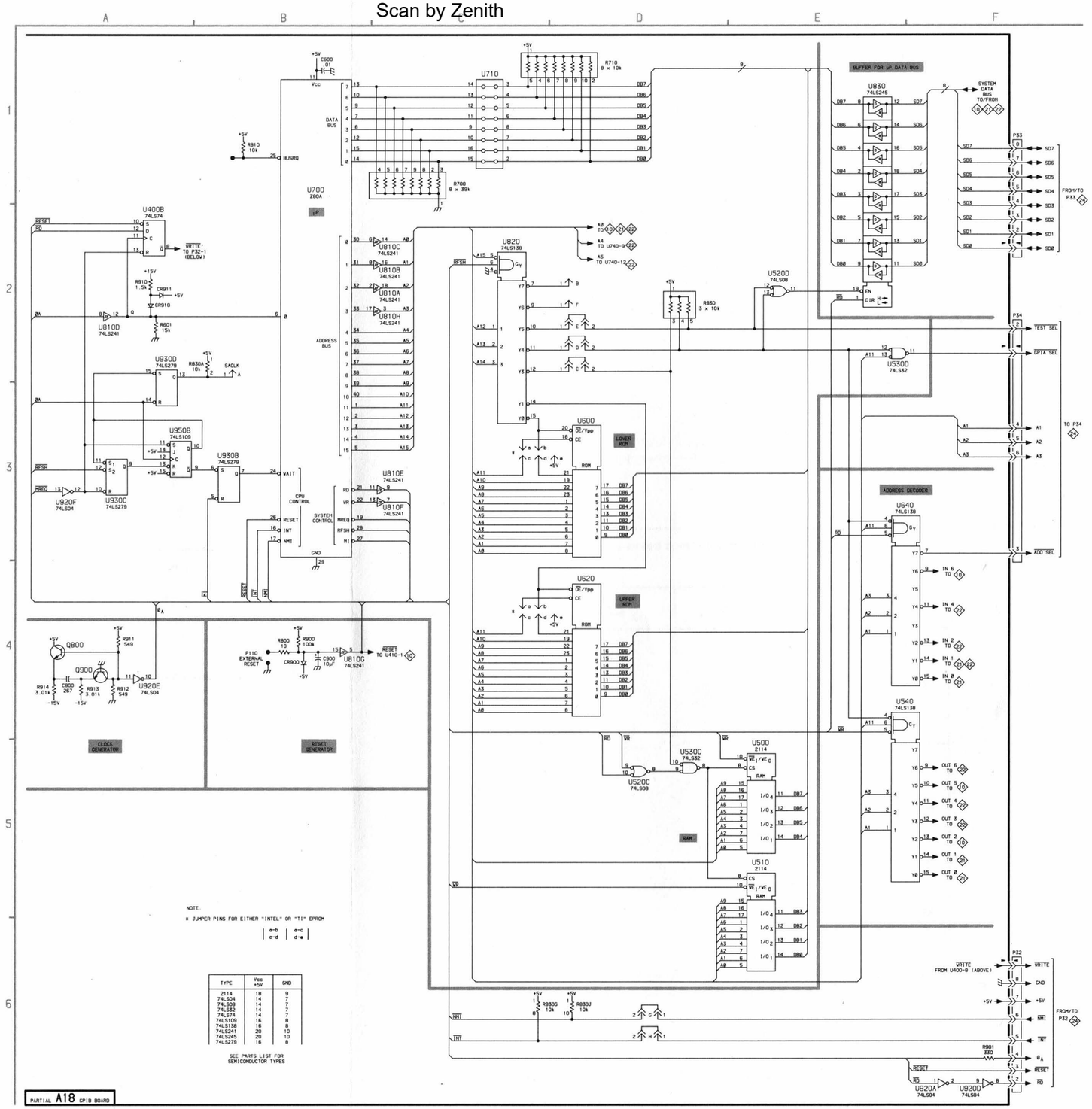
CENTRAL PROCESSING UNIT DIAGRAM 23

ASSEMBLY A18

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C600	B1	H1
C800	A4	J1
C900	B4	K1
CR900	B4	K1
CR910	A2	K1
CR911	A2	K1
P32	F6	K1
P33	F1	K3
P34	F2	K2
P110	B4	A2
Q800	A4	J1
Q900	A4	K1
R601	A2	H1
R700	C1	I1
R710	D1	I2
R800	B4	J1
R810	B1	J2
R830A	B2	J3
R830G	D6	J3
R830J	D6	J3
R830	D2	J3
R900	B4	K1
R901	F6	K1
R910	A2	K1
R911	A4	K2
R912	A4	K2
R913	A4	K2
R914	A4	K2
U400B	A2	E1
U500	E5	F1
U510	E5	F1
U520C	D5	F2
U520D	E2	F2
U530C	D5	F3
U530D	E2	F3
U540	F4	F3
U600	D3	G1
U620	D4	G2
U640	F3	G2
U700	B1	I1
U710	C1	I2
U810A	C2	J2
U810B	C2	J2
U810C	C2	J2
U810D	A2	J2
U810E	C3	J2
U810F	C3	J2
U810G	B4	J2
U810H	C2	J2
U820	C2	J2
U830	E1	I2
U920A	F6	K2
U920D	F6	K2
U920E	A4	K2
U920F	A3	K2
U930B	B3	K3
U930C	A3	K3
U930D	A2	K3
U950B	A3	K4

Partial A18 also shown on diagrams 10, 18, 21 and 22.





5223 GPIB OPTION

3715-122

CENTRAL PROCESSING UNIT 23

5223 Option 10

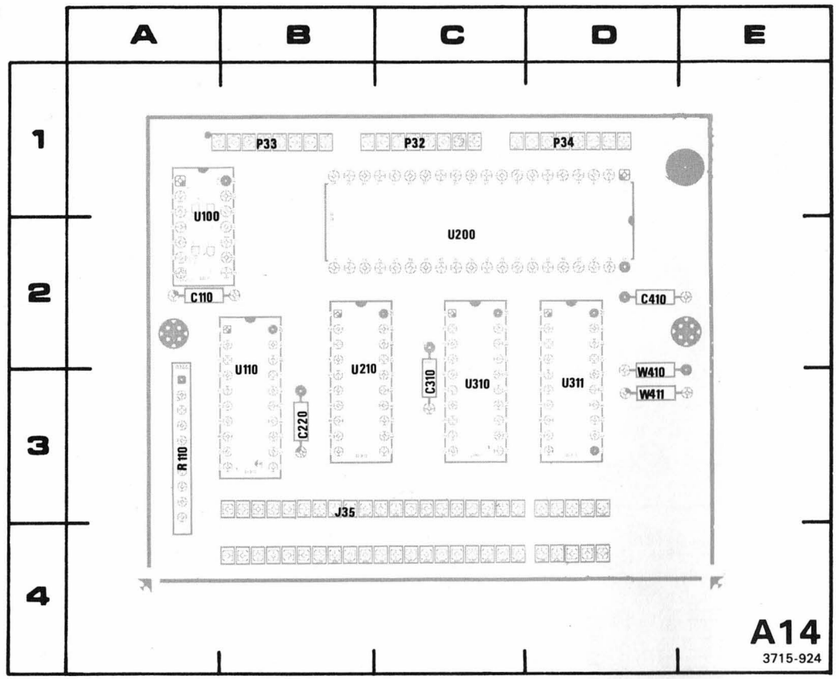


Figure 9-30. A14-Driver circuit board assembly.

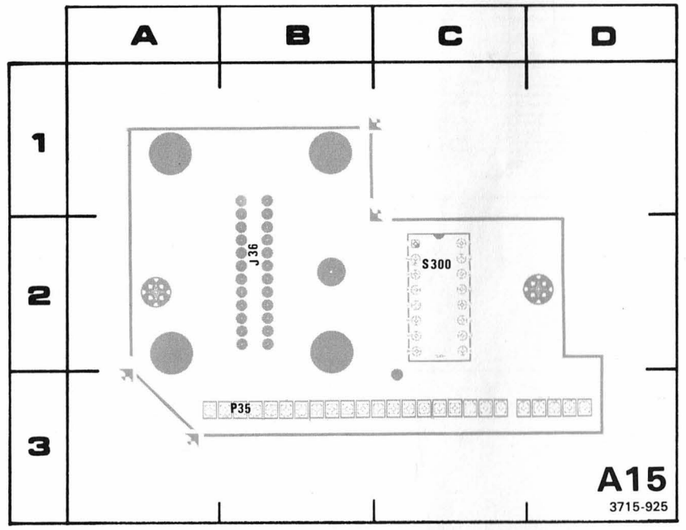
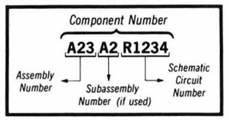


Figure 9-31. A15-Rear Panel circuit board assembly.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



@ Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

A14—Driver, A15—Rear Panel Circuit Bd Assemblies

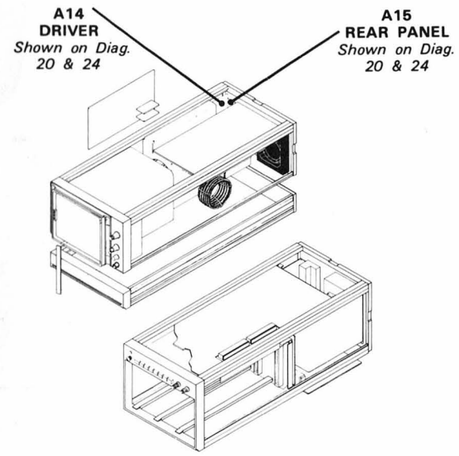
GPIB DRIVERS DIAGRAM 24

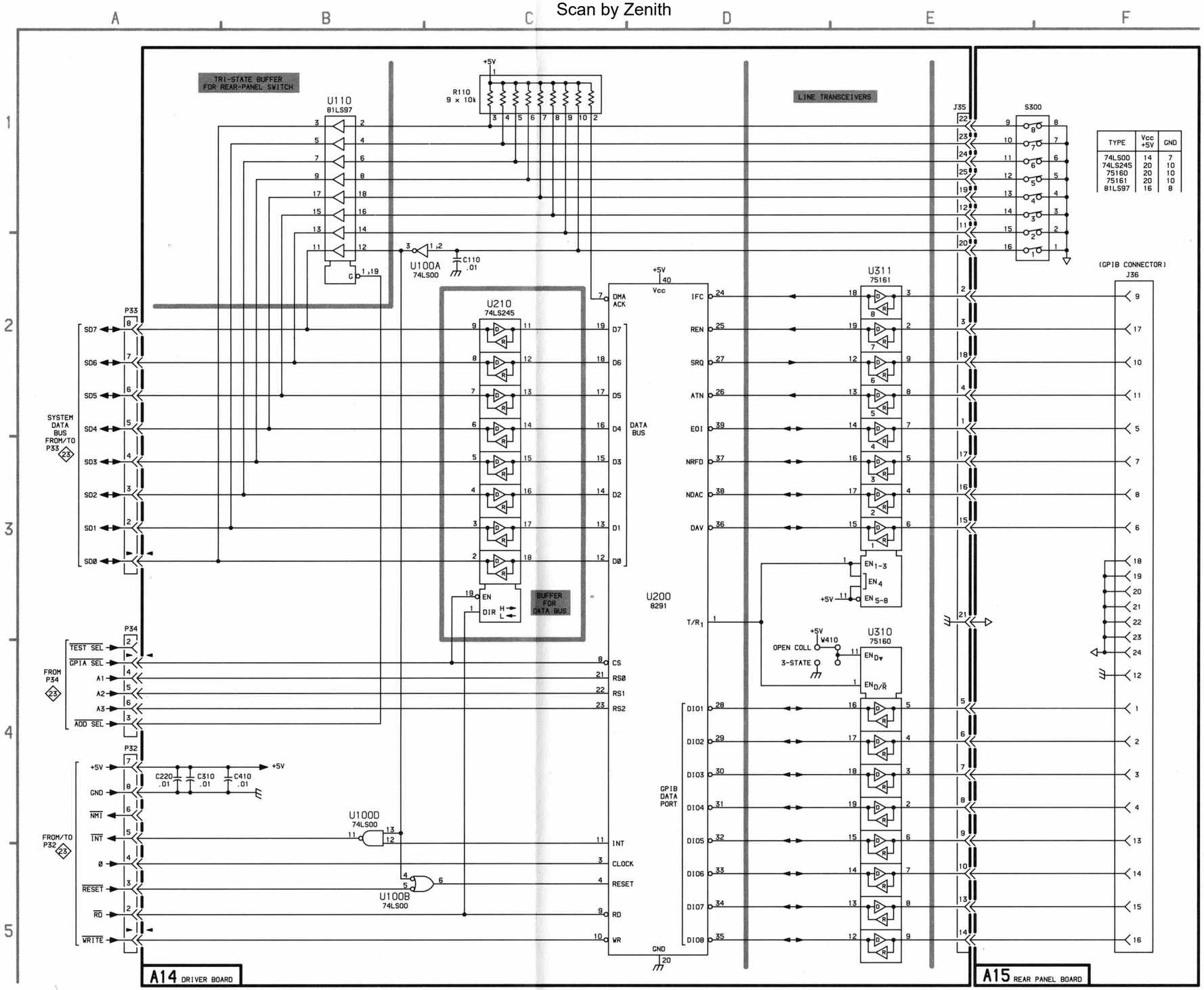
ASSEMBLY A14

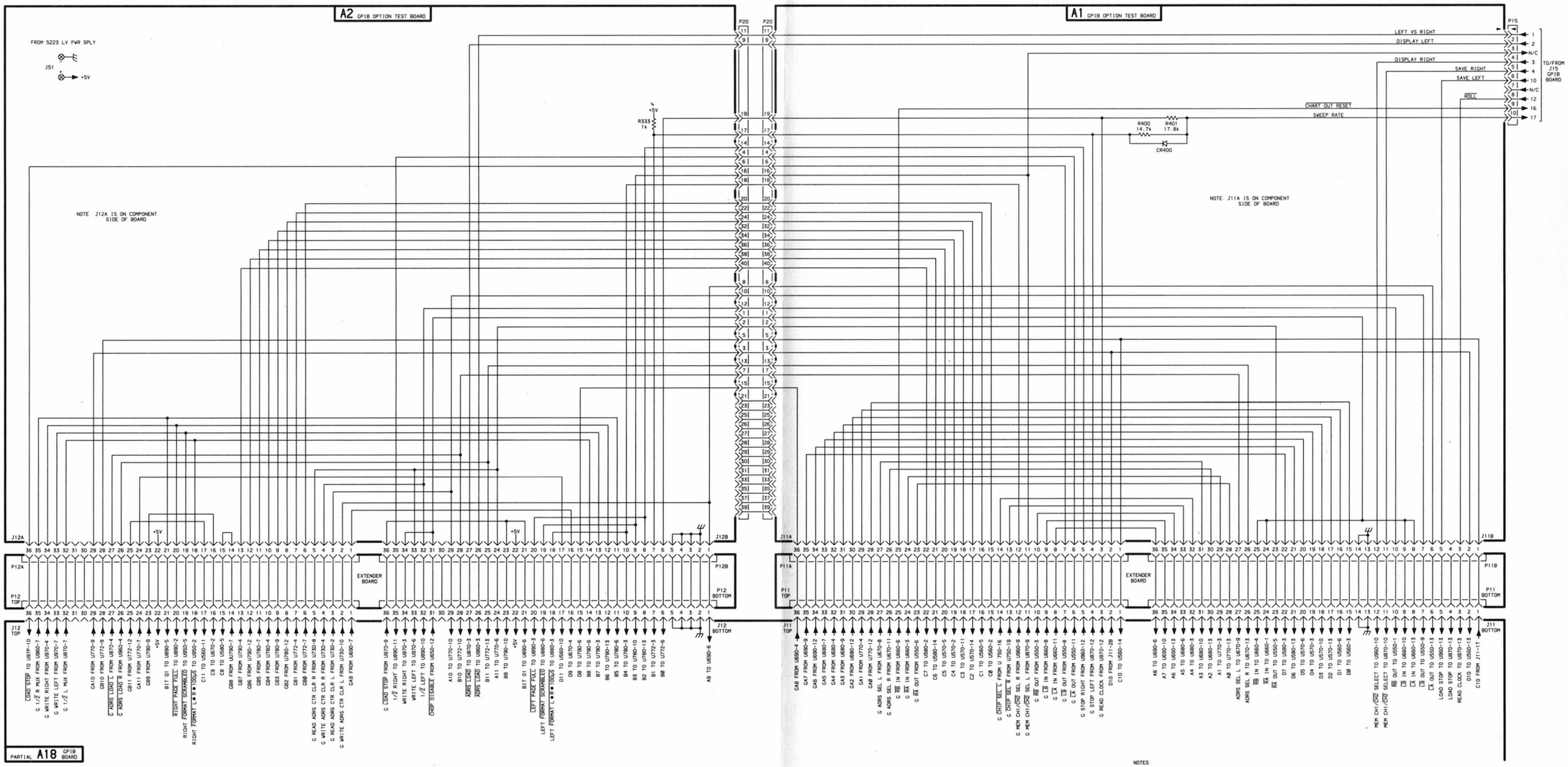
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	C2	A2
C220	A4	B3
C310	A4	C3
C410	B4	D2
J35	E1	B3
P32	A4	C1
P32	A5	C1
P33	A2	B1
P33	A3	B1
P34	A3	D1
P34	A4	D1
R110	C1	A3
U100A	C2	A2
U100B	B5	A2
U100D	B4	A2
U110	B1	B3
U200	D3	C2
U210	C2	B3
U310	E3	C3
U311	E2	D3
W410	E3	D3

ASSEMBLY A15

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J36	F2	B2
S300	F1	C2

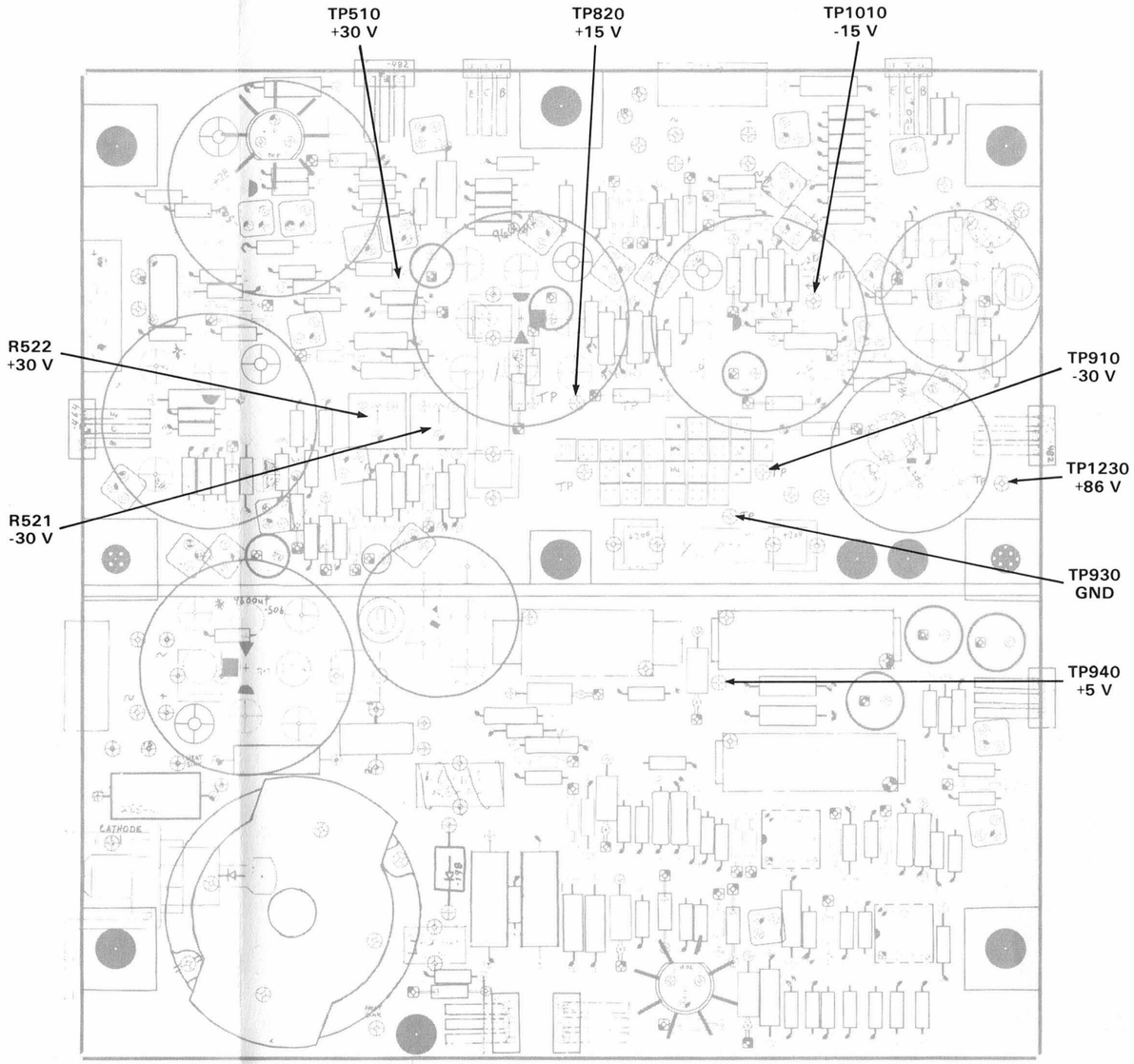




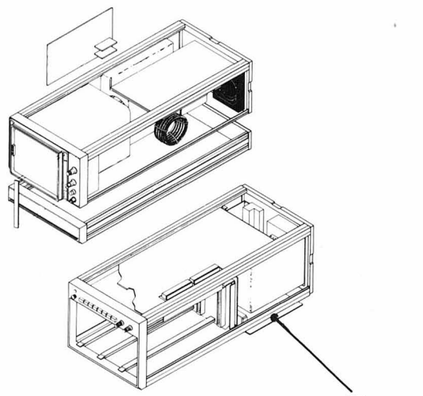


NOTES.
1. EXTENDER BOARDS ARE PART OF 067-0967-00 EXTENDER KIT
2. A1,A2,&4 EXTENDER BOARDS ARE NOT PART OF 5223 OPTION 10

067-0966-00
Loop Thru & Extender Board

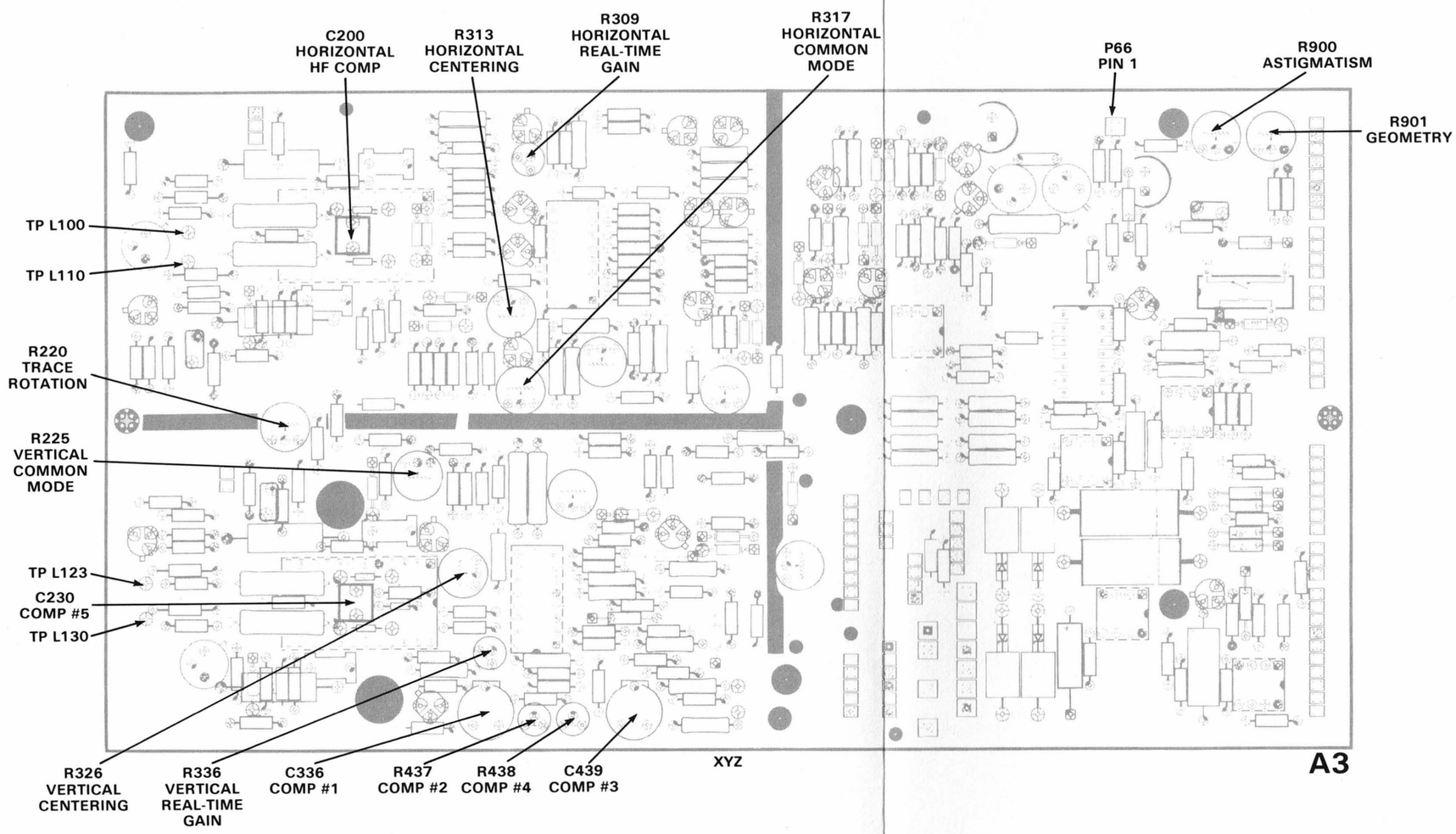


POWER SUPPLY BOARD **A7**



A7
POWER SUPPLY
Shown on Diag. 7

Figure 9-32. Test Point and Adjustment Locations A.



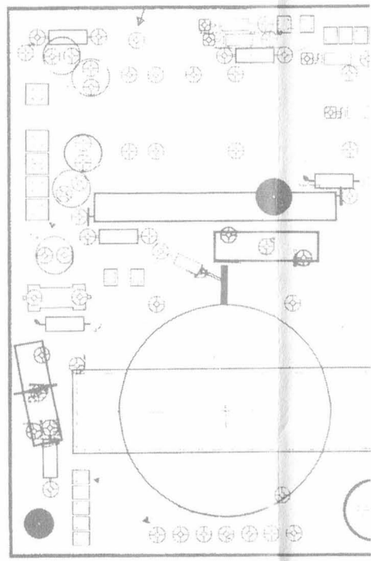
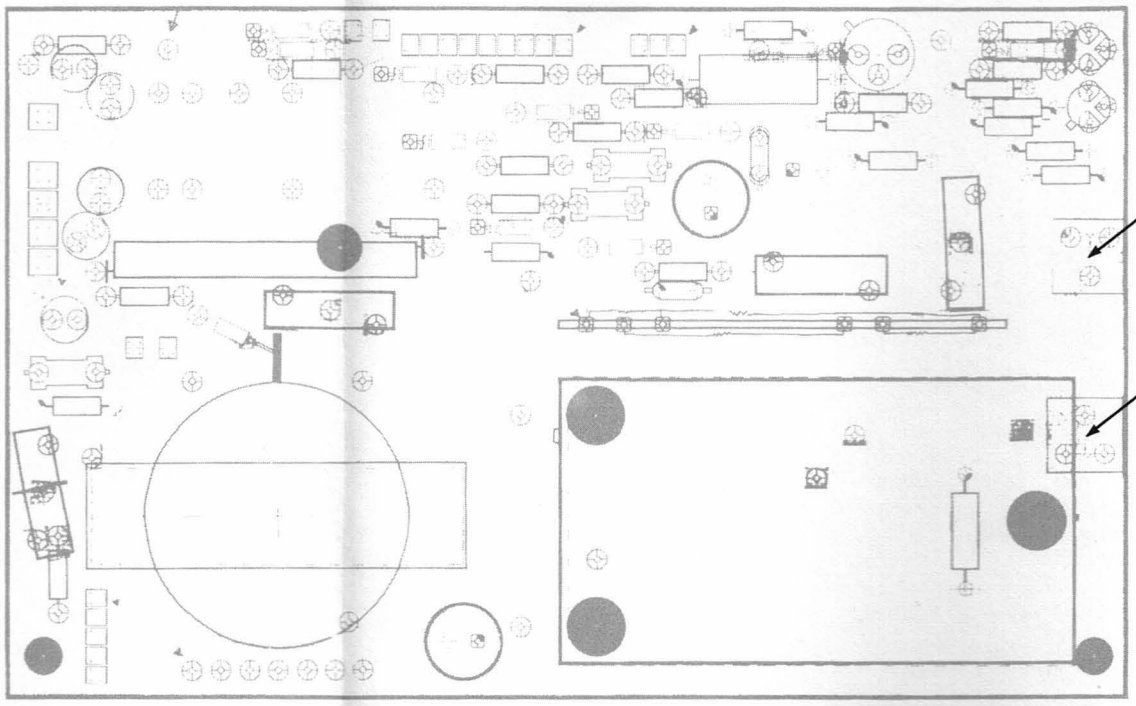
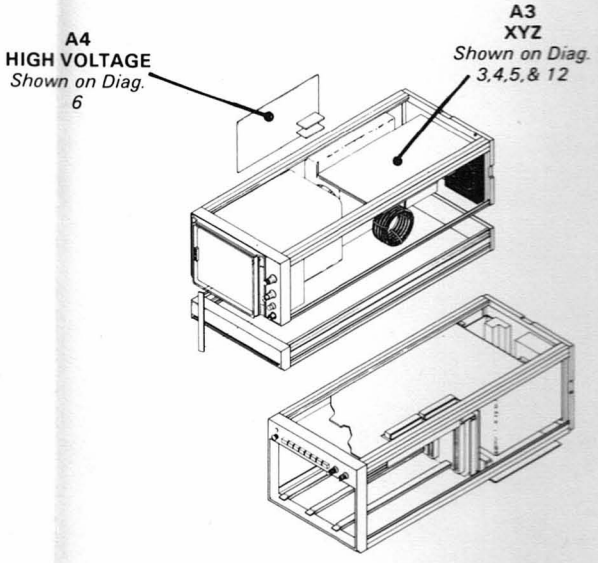


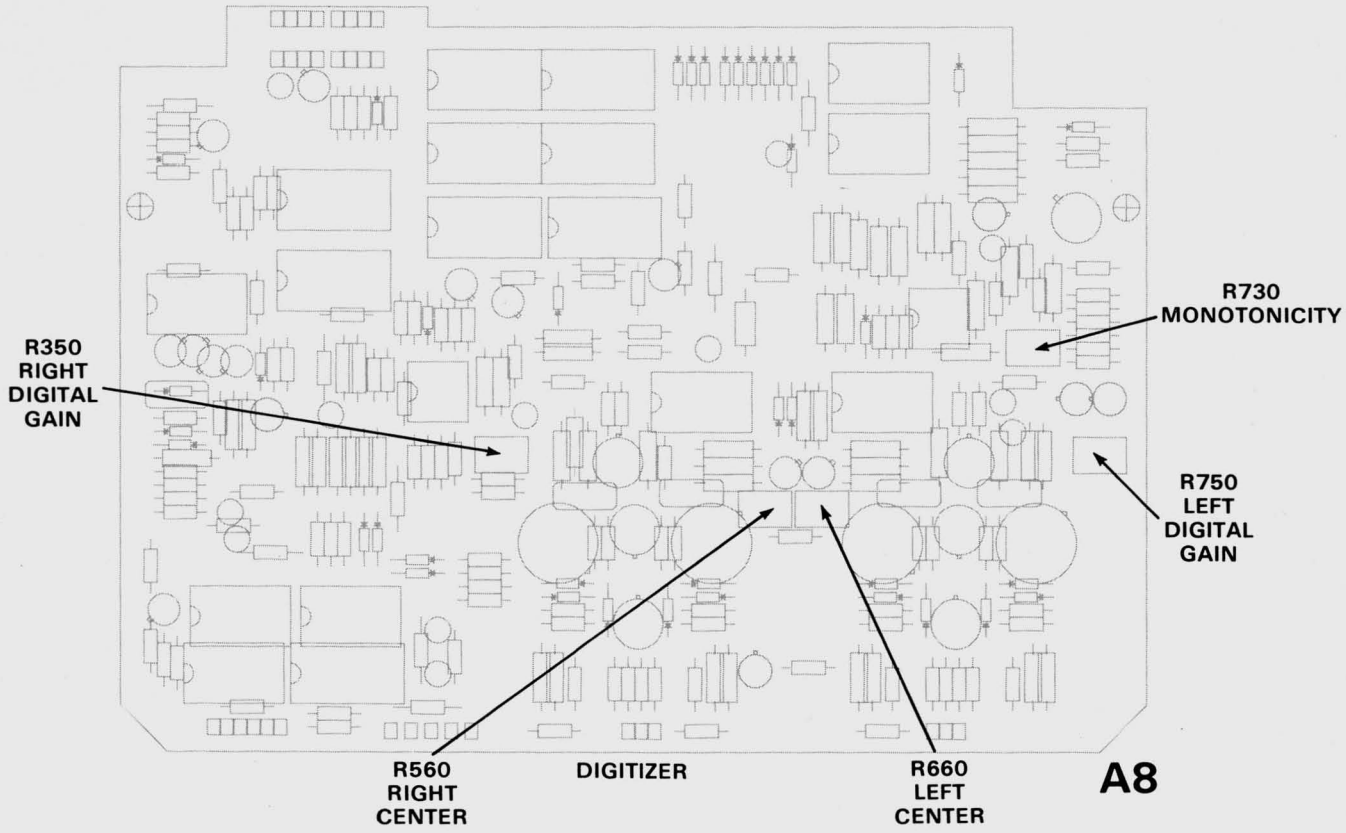
Figure 9-33. Test Point and Adjustment Locations B.

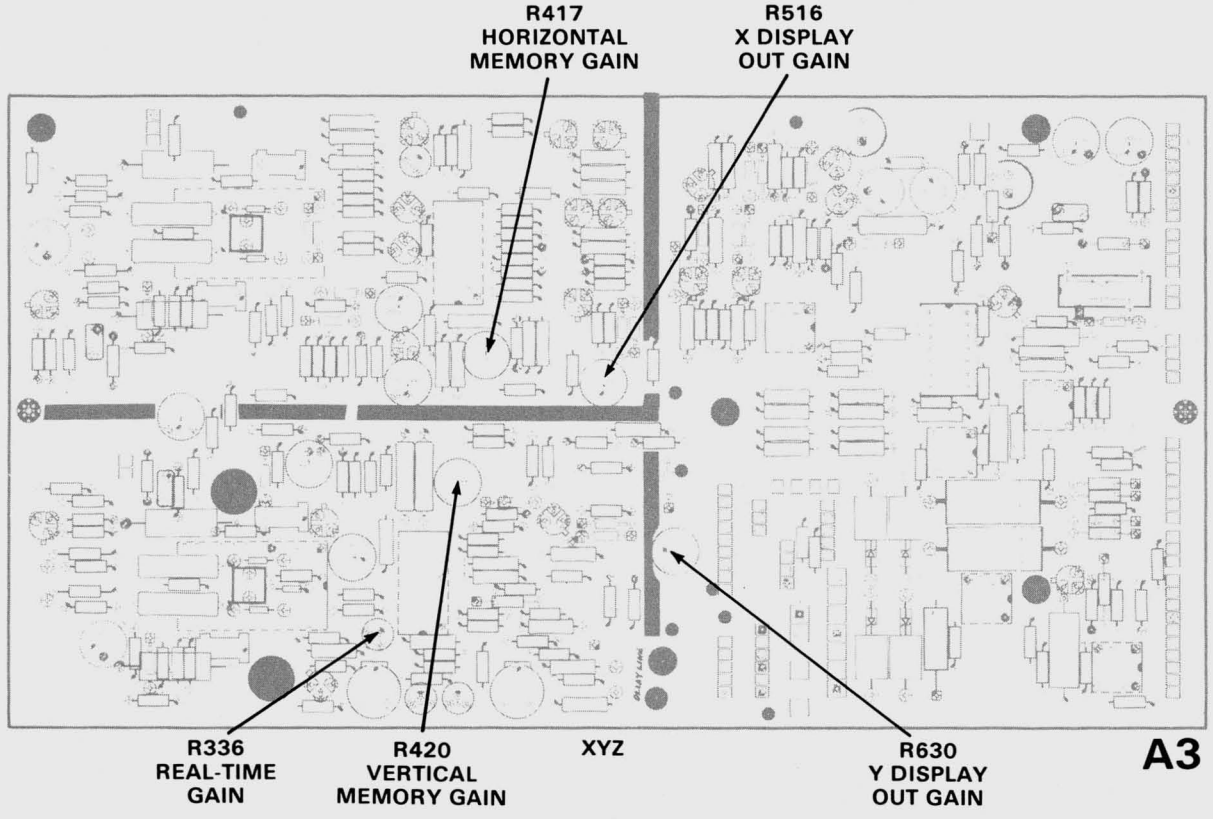


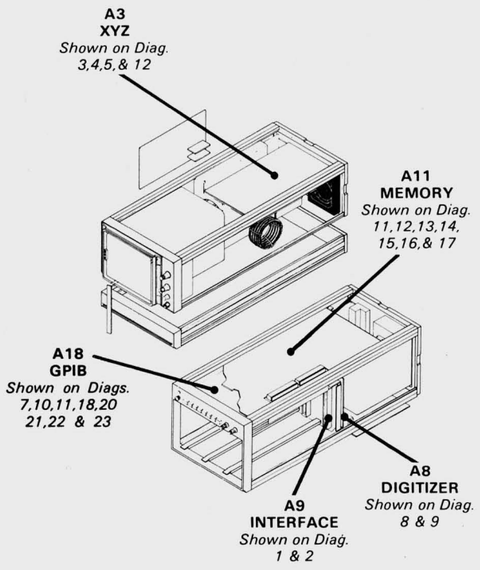
HIGH VOLTAGE **A4**

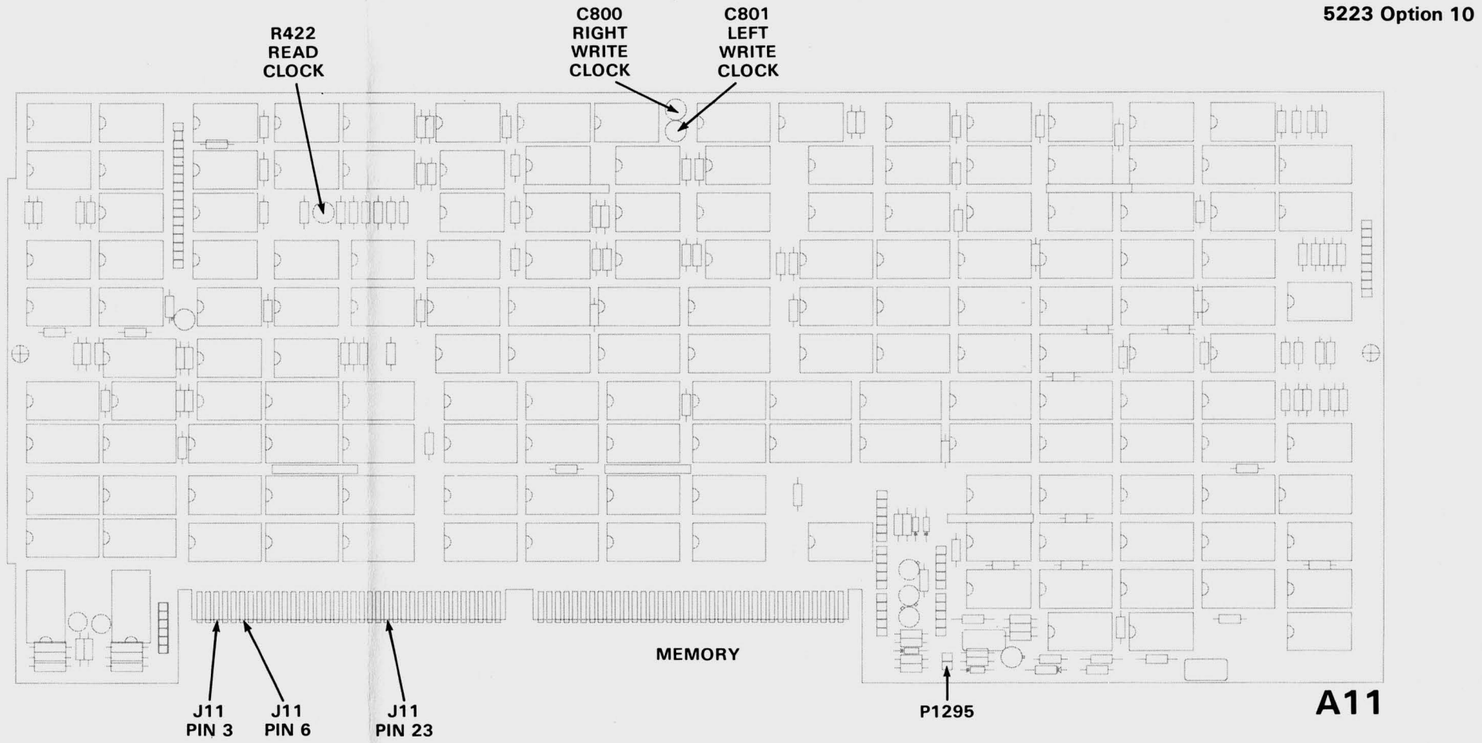


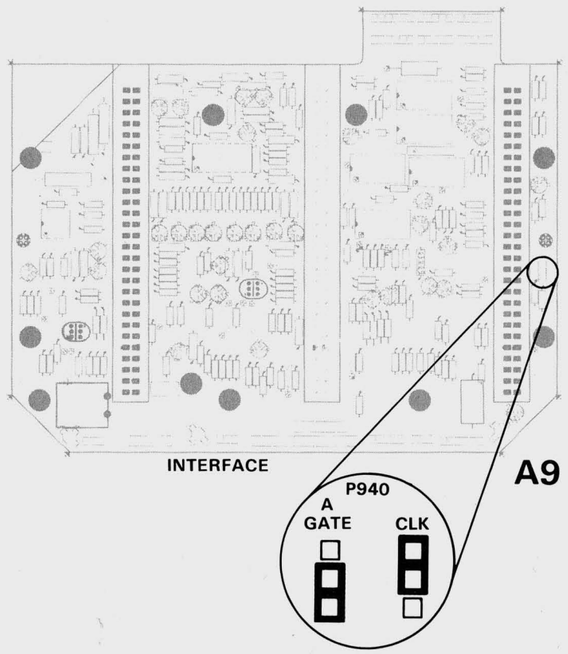
:ions B.











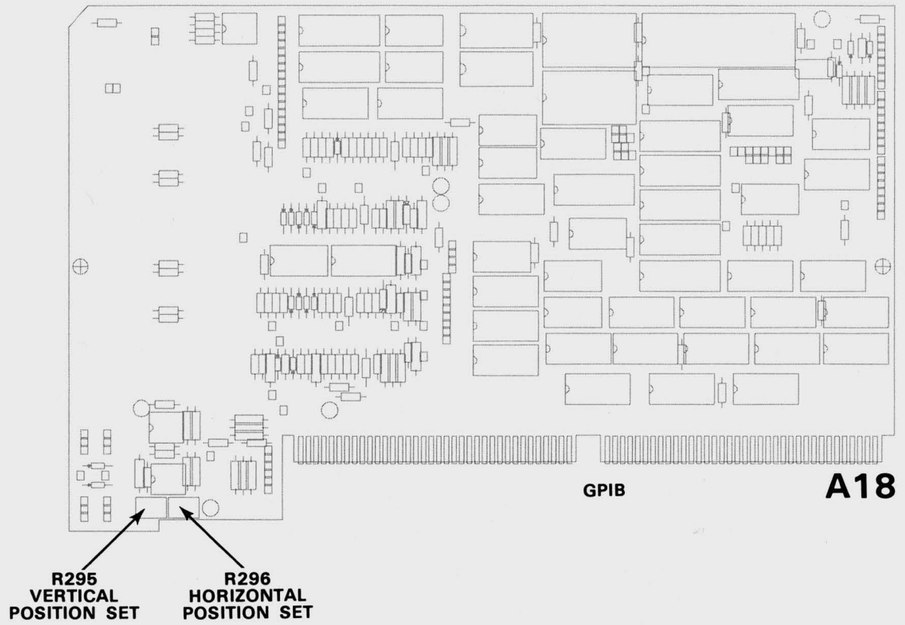
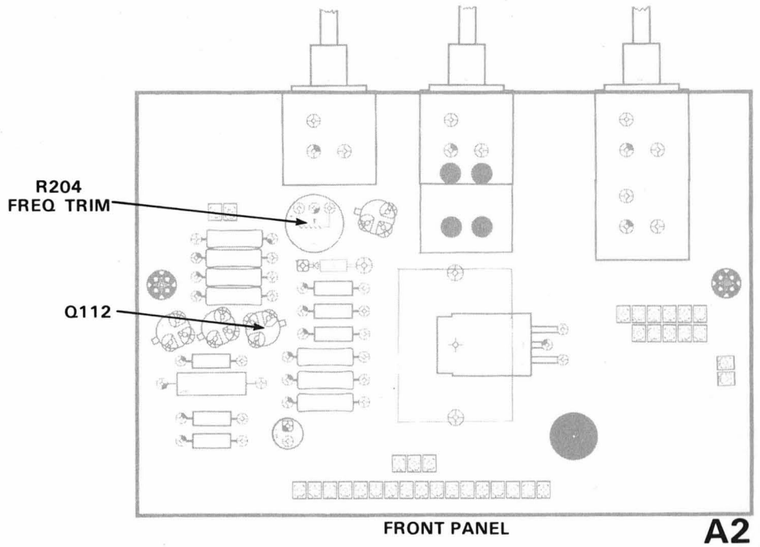
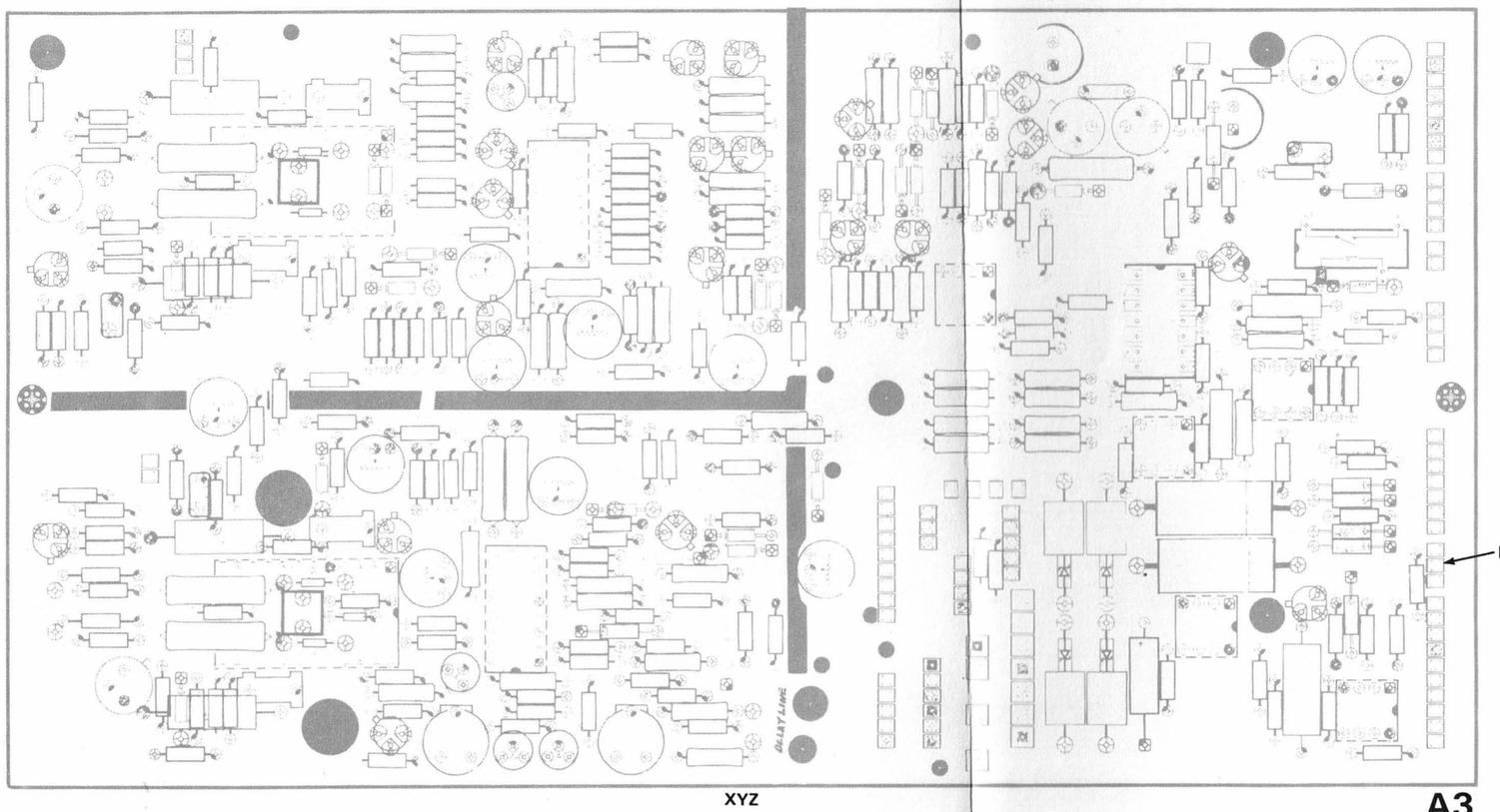


Figure 9-34. Test Point and Adjustment Locations C.





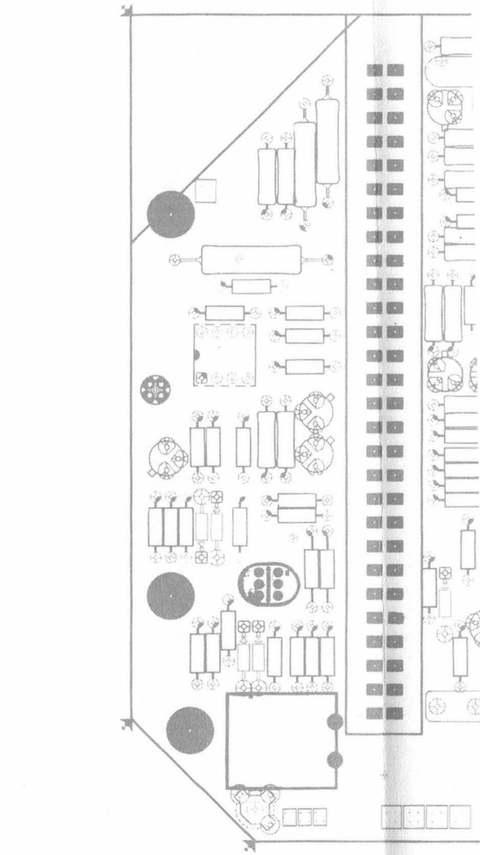
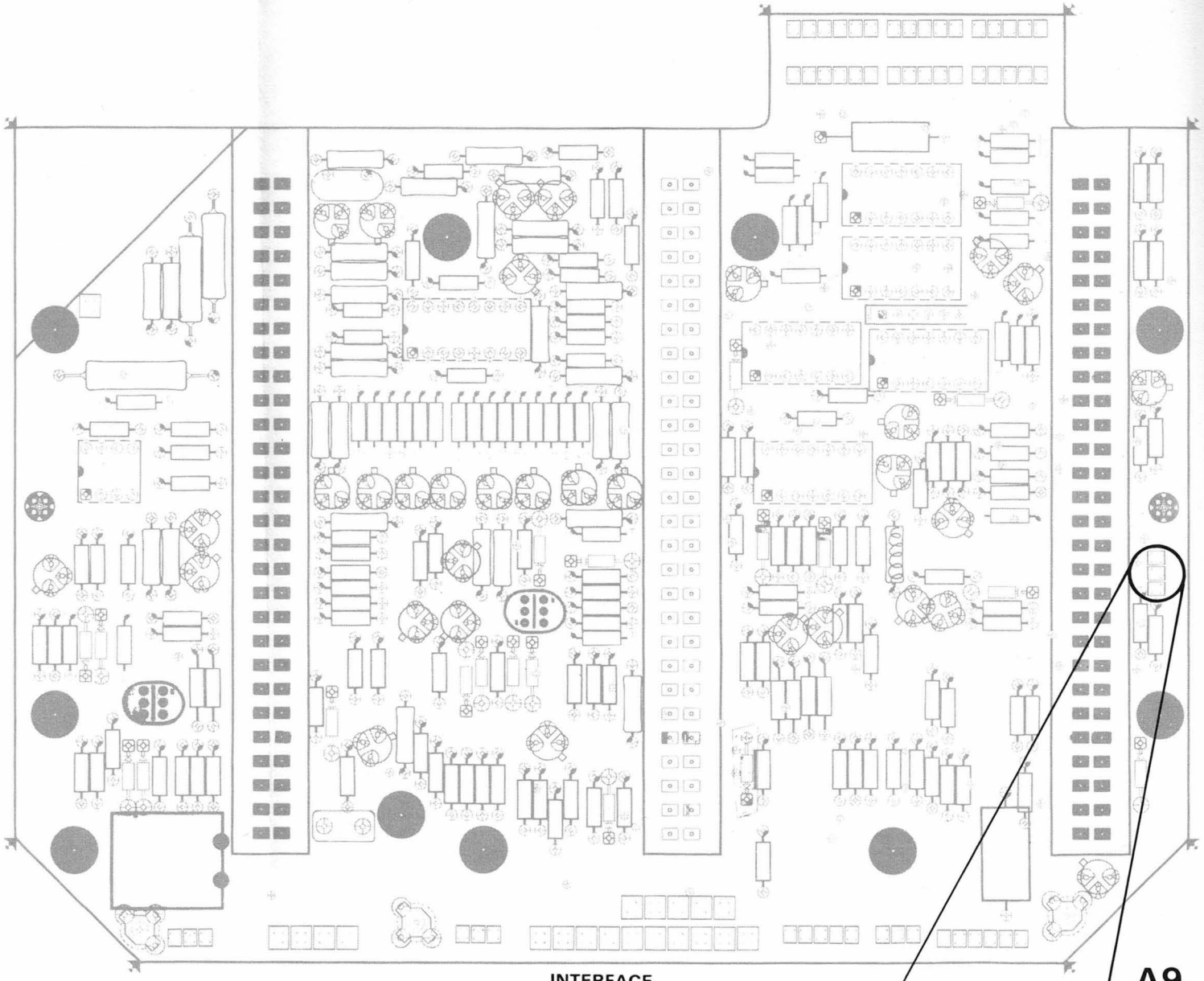


Figure 9-35. Test Point and Adjustment Locations D.

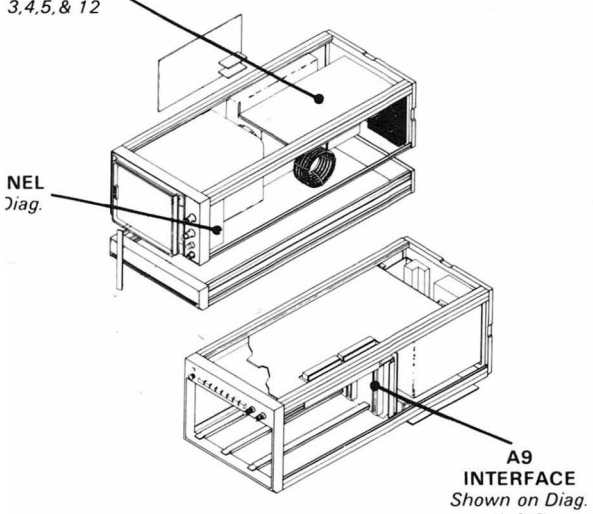


INTERFACE

A9

A3
XYZ
hown on Diag.
3,4,5,& 12

NEL
Diag.



A9
INTERFACE
Shown on Diag.
1 & 2

APPENDIX A

TROUBLESHOOTING CHARTS (INTRODUCTION)

The troubleshooting charts on the following foldout pages provide a guide for locating defective components on the A18-GPIB and A11-Memory board.

Working knowledge of digital circuit theory and troubleshooting techniques are a must for a quality and timely repair job.

Refer to Section 3, Theory of Operation, for detailed discussion of the circuits mentioned in these troubleshooting foldouts.

USING THE CHARTS

Begin at START in the upper left hand corner.

Perform the instrument check(s) shown in the box, answer the question in the following diamond, then proceed in the direction that your answer indicates (Yes—across, No—down) until all checks have been performed, or the defective circuit/component has been identified.

A numbered diamond (within a box) refers to the schematic that the particular test point or component can be found.

SETUP CONDITIONS

1. Install a 5B25N Time Base and 2 dual channel plug-ins (5A38, 5A48) in the appropriate compartments of the 5223.

2. Apply either sine or triangle waves to the 4 inputs of the amplifier plug-ins.

NOTE

Do not use square waves, as imperfections, if any, in the digital display, can be hidden.

3. Pull ON the power switch. Check that the signals applied to the plug-in inputs appear on the crt in a normal fashion.

4. Check that all normal scope controls function properly.

5. Refer to the Index Of Symptoms then proceed to the appropriate chart.

INDEX OF SYMPTOMS

NOTE

Refer to 'Self-Test and Signature Analysis Troubleshooting' in Section 4, Maintenance; then proceed to Signature Set D-4 in Appendix B.

TROUBLESHOOTING HINTS

From our experience with development and manufacture of the 5223 Digitizing Oscilloscope, we've compiled a few service "hints" which may prove useful in troubleshooting the instrument. These service "hints" are meant to supplement the standard fold-out troubleshooting flow charts in the 5223 Digitizing Oscilloscope Service manual, and also apply to servicing the standard instrument.

Service Hints:

1. If the common mode output voltage of the X and Y output amplifiers is not set correctly (step B2 of the calibration procedure), bizarre effects may be seen at high frequencies.

2. If CRT grid bias is not set properly (step B3 of the calibration procedure), memory/realtime interaction will be considerable (step B8 of the calibration procedure).

3. Monotonicity (step C6 of the calibration procedure) should not need to be set unless a component is changed in the circuit (see schematic 9).

4. If the memory does not update, ensure the real time sweep is running and that there is activity on the sample pulse line and on the load stop line.

NOTE

The instrument is in its simplest configuration in the ROLL mode (load stop is not used).

5. Removal of P40 (Memory to XYZ board) will make XYZ board default to real-time only. Ensure that blank P10 (interface to memory) pin 5 is in the high state.

6. Due to special circumstances associated with this timebase range, avoid using the timebase range setting of 100 μs/div when checking out oscilloscope operation. (This has to do with the Extra Write discussed in the Theory of Operation section under the heading of: Scratch pad controller, block LL, part of this discussion for diagram 11.)

7. Removal of A7Q960 will aid in troubleshooting the control circuit on the 5 V power supply by opening the power loop.

8. If 5V crowbar circuit A7Q1341 has tripped, wait two minutes to allow reservoir capacitor A7C340 to discharge.

9. Do not replace A7F340 with a higher rated fuse if it should blow out. This fuse is essential to the crowbar, A7Q1340,to ensure that all TTL and other components in the instrument do not get "overvolted". A likely cause of crowbar operation is that A7Q960, 760, or 660 are shorted.

10. Some distortion of vector displays in expanded mode is normal.

11. Hot switching of plug-ins may result in blowing the 200 V fuse.

12. When disconnecting J51, ensure that the leads DO NOT touch the adjacent 200 V fuseholder—otherwise the complete memory board and other circuits will be destroyed.

13. If one compartment memory is running and the other is defective, use the working memory system to compare (they are identical).

14. If a problem arises on the XYZ board, always ensure that +86 V is present.

15. If there is no high voltage, check A7F620 first.

16. When checking power supplies, always check the transformer secondary voltages on the power supply board to ensure that fuses have not blown.

17. Defective memory control buttons can be removed from the front by using ordinary "bull-nose" pliers. A new button can then be installed without complete instrument tear-down.

18. Many digital memory circuits can be separated from each other by simply removing the GPIB board/memory board interface connectors.

19. Make sure the TEST switch on the rear panel is in the correct position. When the TEST switch is in the ON position, the instrument branches into its stimulation routines.

@

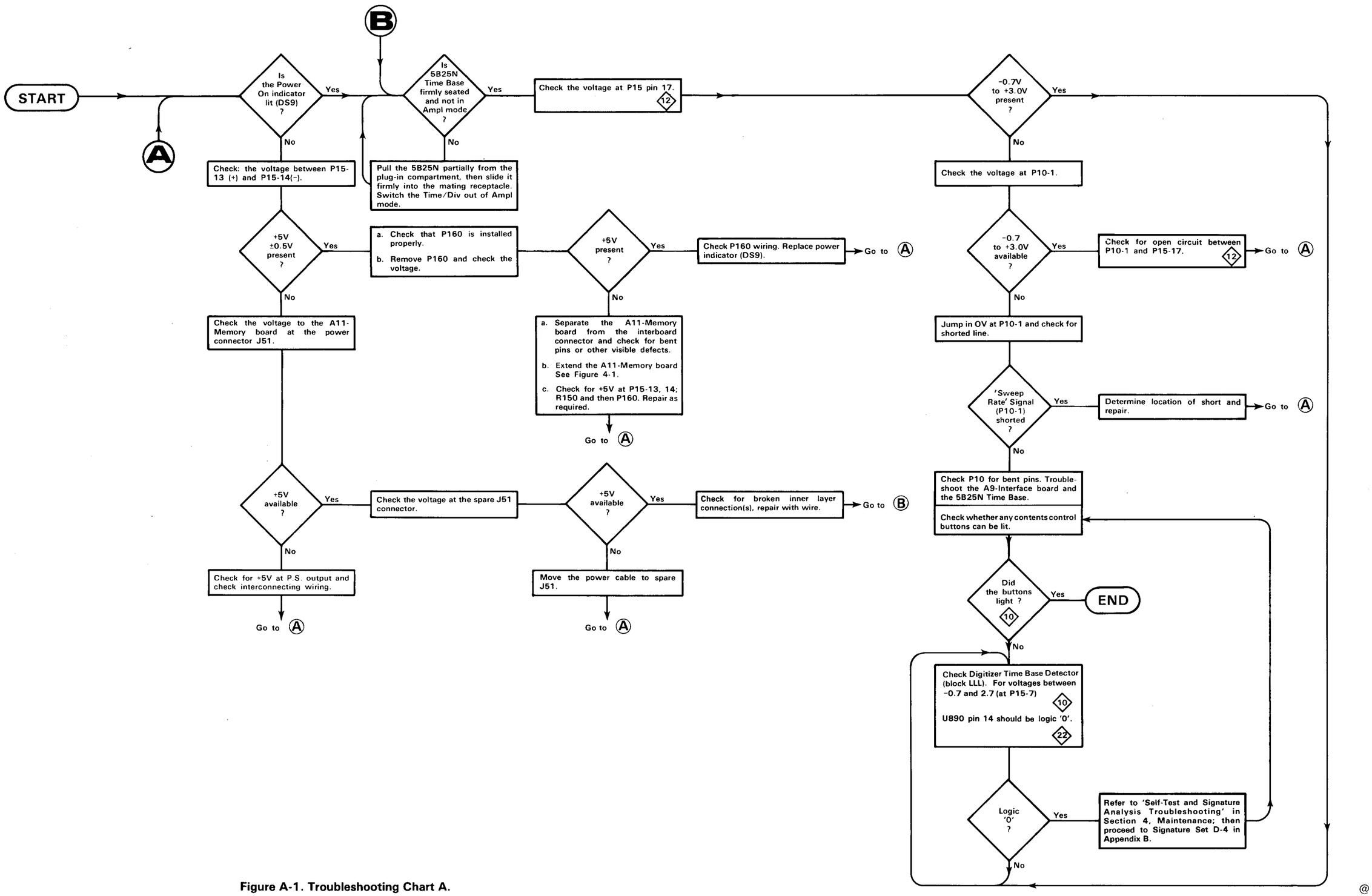
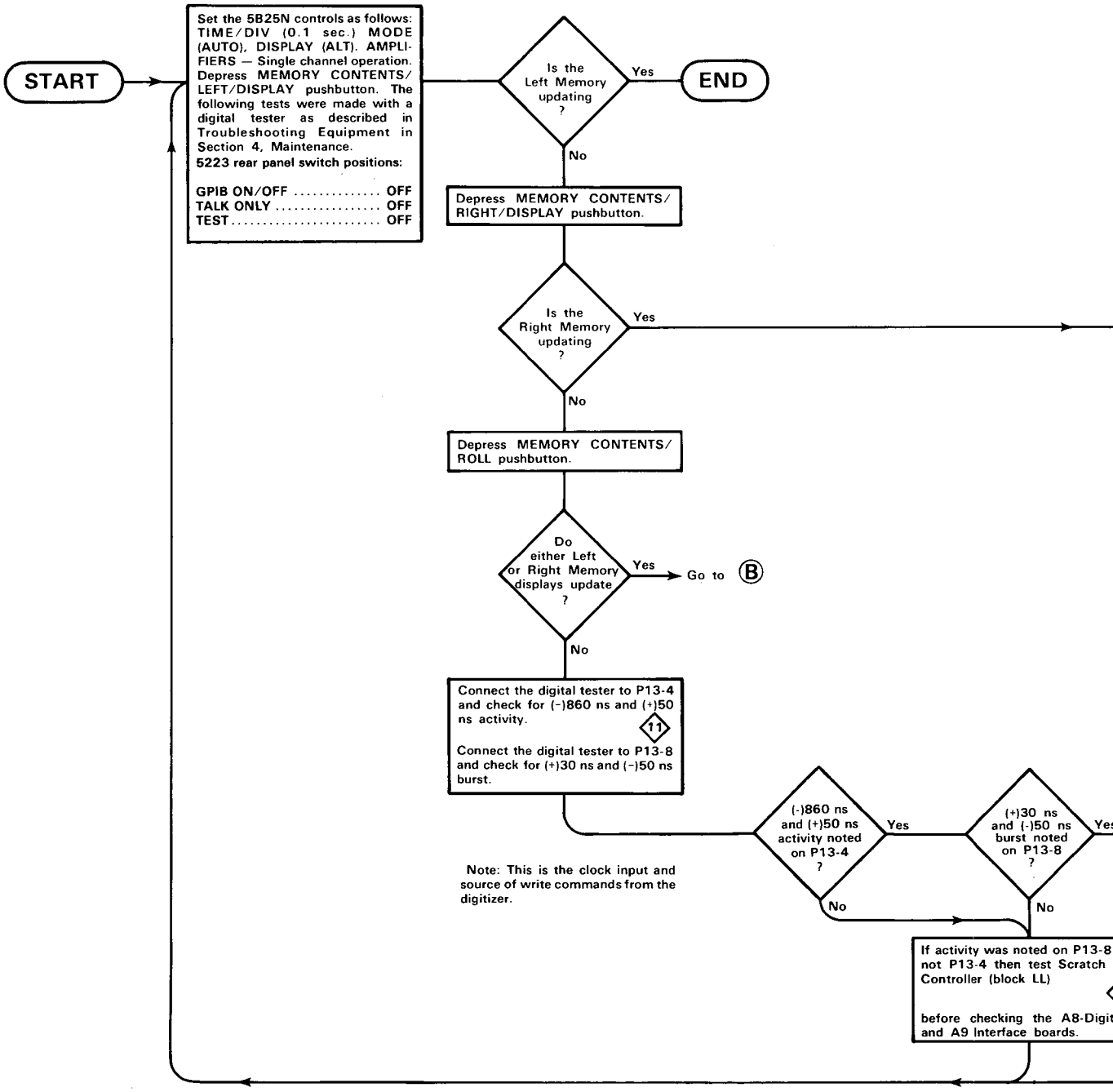


Figure A-1. Troubleshooting Chart A.

LEFT MEMORY COMPARTMENT WILL NOT UPDATE



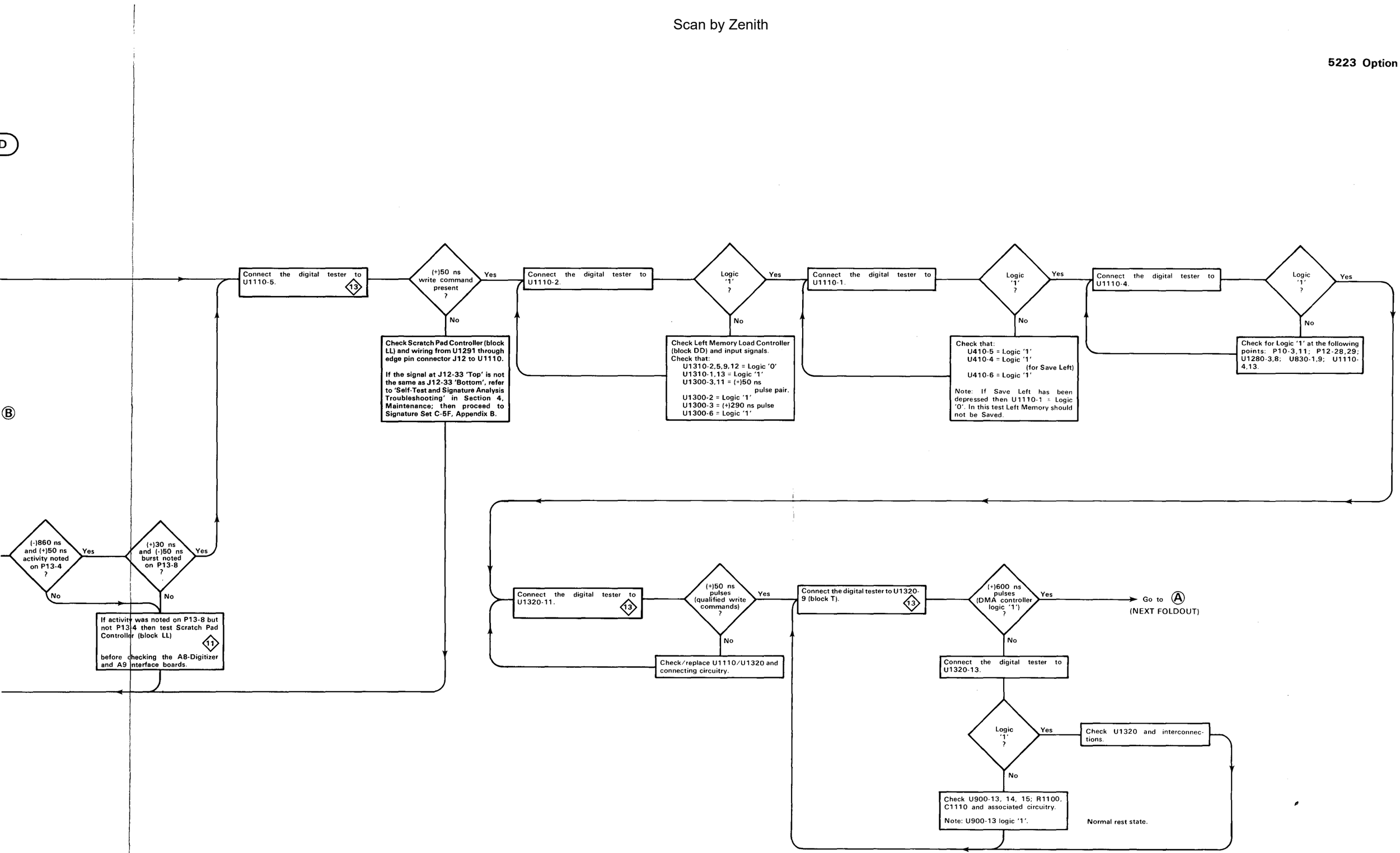
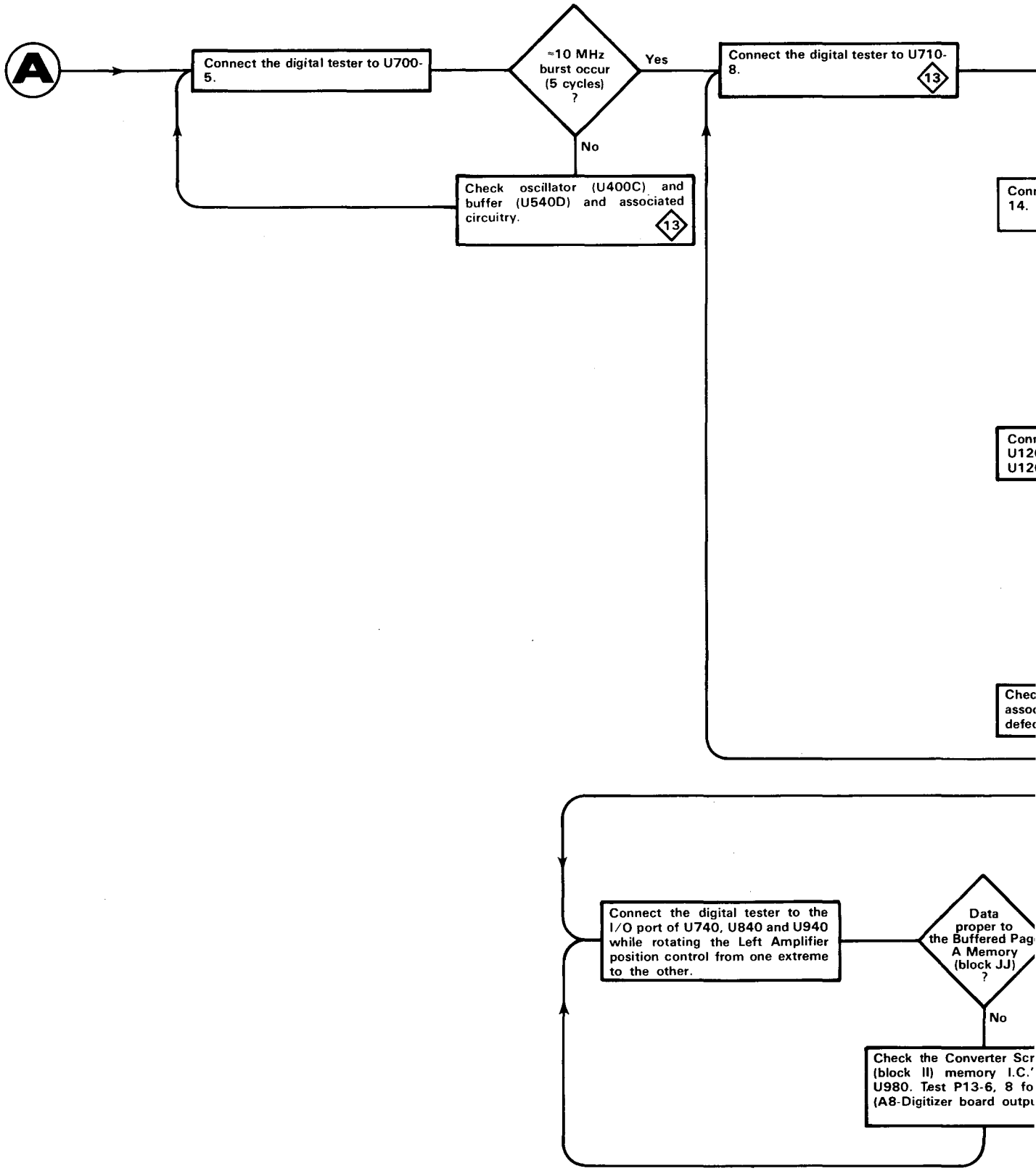


Figure A-2. Troubleshooting Chart B.

@

LEFT MEMORY COMPARTMENT WILL NOT UPDATE (CONT)



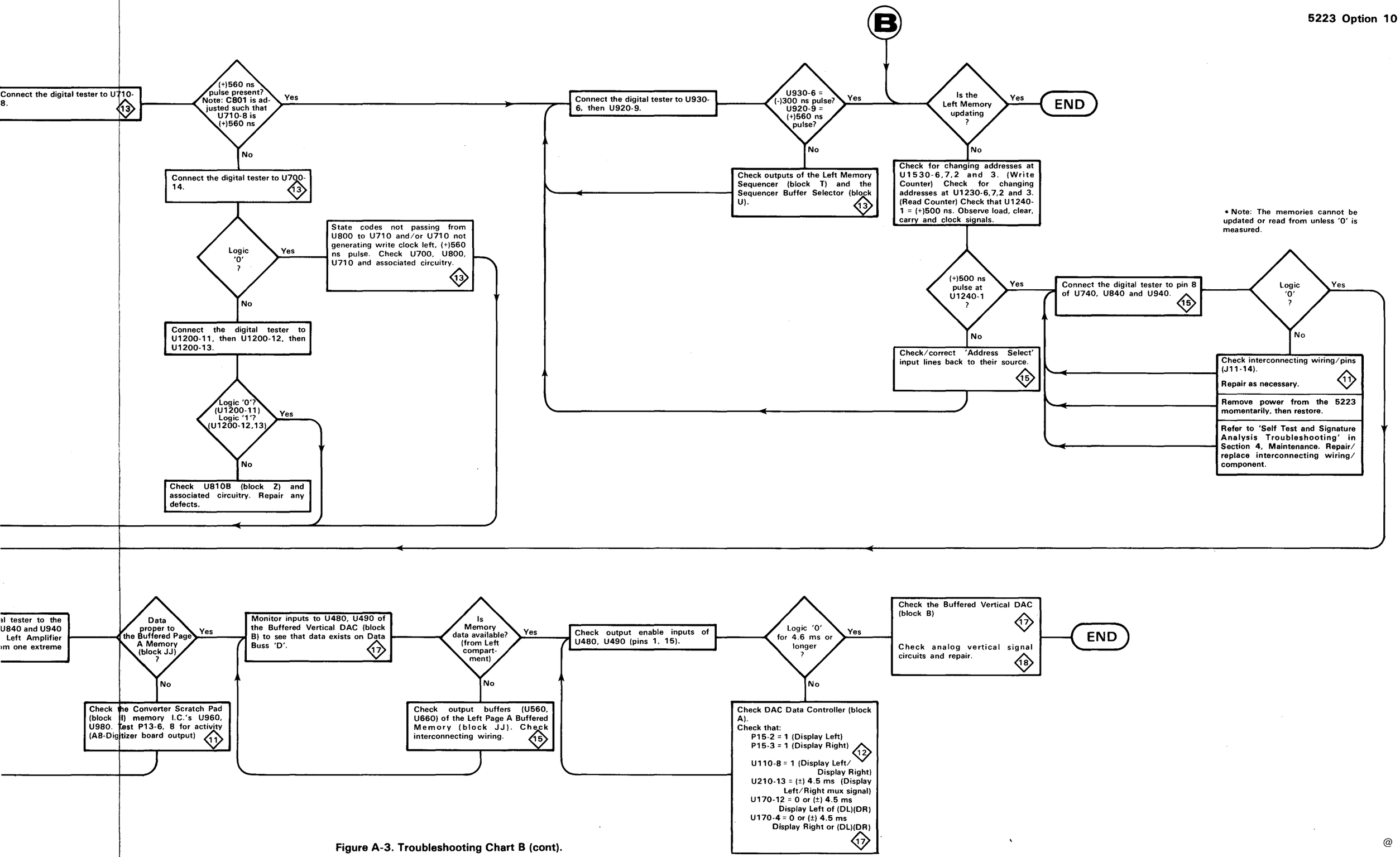
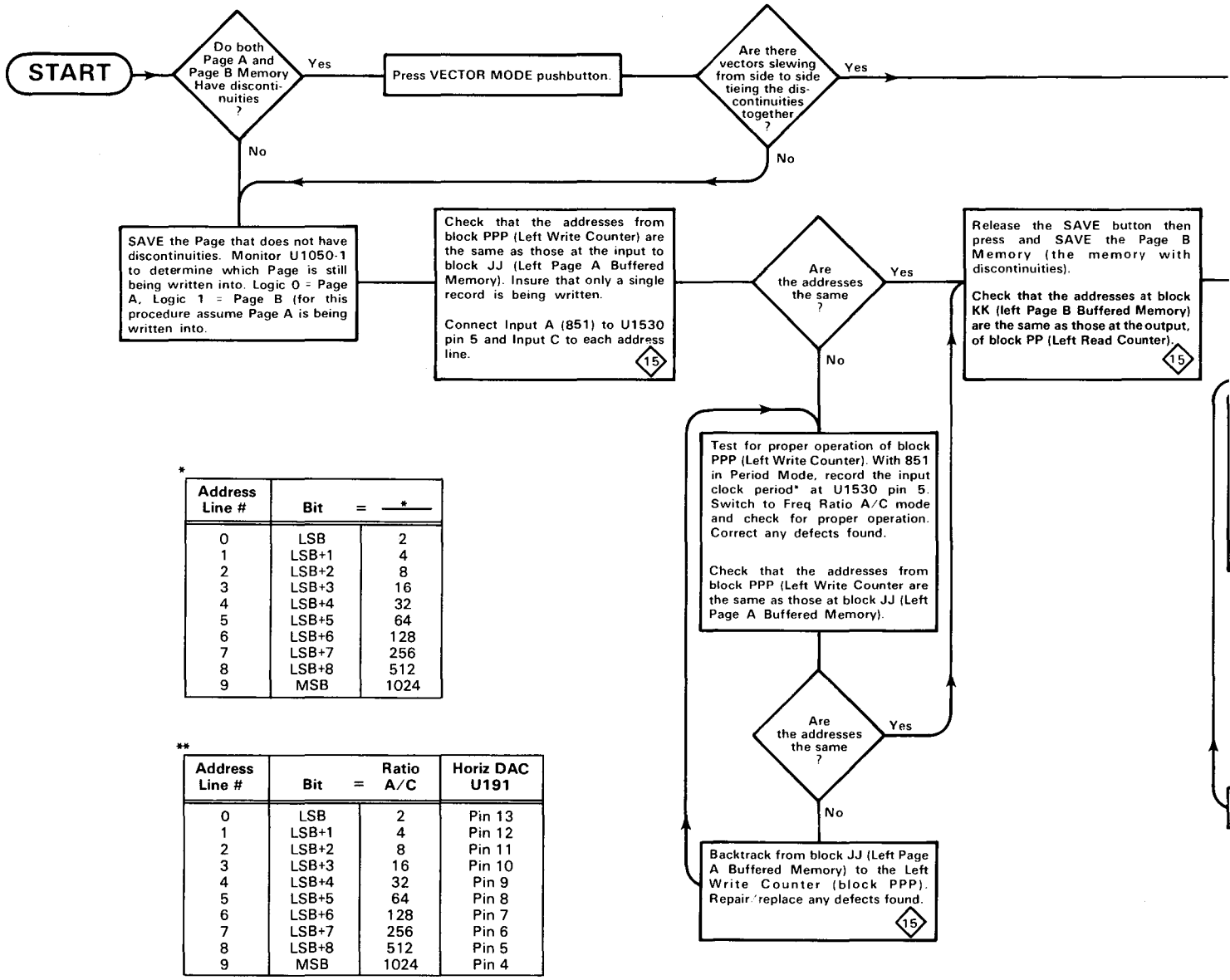


Figure A-3. Troubleshooting Chart B (cont).

LEFT MEMORY DISPLAYED WAVEFORMS HAVE ADDRESSING PROBLEM

Use 851 Digital Tester in Freq Ratio A/C mode unless noted otherwise.



*

Address Line #	Bit	= —*—
0	LSB	2
1	LSB+1	4
2	LSB+2	8
3	LSB+3	16
4	LSB+4	32
5	LSB+5	64
6	LSB+6	128
7	LSB+7	256
8	LSB+8	512
9	MSB	1024

**

Address Line #	Bit	= Ratio A/C	Horiz DAC U191
0	LSB	2	Pin 13
1	LSB+1	4	Pin 12
2	LSB+2	8	Pin 11
3	LSB+3	16	Pin 10
4	LSB+4	32	Pin 9
5	LSB+5	64	Pin 8
6	LSB+6	128	Pin 7
7	LSB+7	256	Pin 6
8	LSB+8	512	Pin 5
9	MSB	1024	Pin 4

Yes

Release the SAVE button then press and SAVE the Page B Memory (the memory with discontinuities).

Check that the addresses at block KK (left Page B Buffered Memory) are the same as those at the output, of block PP (Left Read Counter). ◇15

Are the addresses the same ?

Yes

No

Test for proper operation of block PP (Left Read Counter). With 851 in Period Mode, measure the input clock period at U1230-5 (4.5 μs).

Switch to Freq Ratio A/C mode (851) and check for proper operation. (Input A connected to U1230-5, Input C connected to each address line).

All addresses correct ?

Yes

No

Check that the addresses at block KK (Left Page B Buffered Memory) are the same as those at the output of block PP (Left Read Counter). ◇15

All addresses correct ?

Yes

No

Backtrack from block KK (Left Page B Buffered Memory) through address multiplexers to block PP (Left Read Counter). Repair/ replace any defects found.

Replace defective read counter as determined by preceding test.

Press VECTOR MODE pushbutton on 5223 mainframe.

Are there vectors slewing from side to side tieing the discontinuities together ?

Yes

No

Try another symptom.

END

With 851 in Period Mode, measure the input clock period at U270 pin 5 (4.5 μs).

Correct clock present ?

Yes

No

Clock originates at U260 pin 9 (block N, diagram 12). Repair/ replace any defects found. ◇12

Connect Input A (851) to U1530 pin 5 and Input C to each address line.**

Correct data found ?

Yes

No

Backtrack those incorrect bits and repair/replace any defects found.

Replace U191 (DAC). If trouble persists proceed to the A18 GPIB board analog circuitry diagram 18. ◇18

END

Figure A-4. Troubleshooting Chart C.

@

LEFT MEMORY DISPLAYED WAVEFORMS HAVE START SWEEP PROBLEM

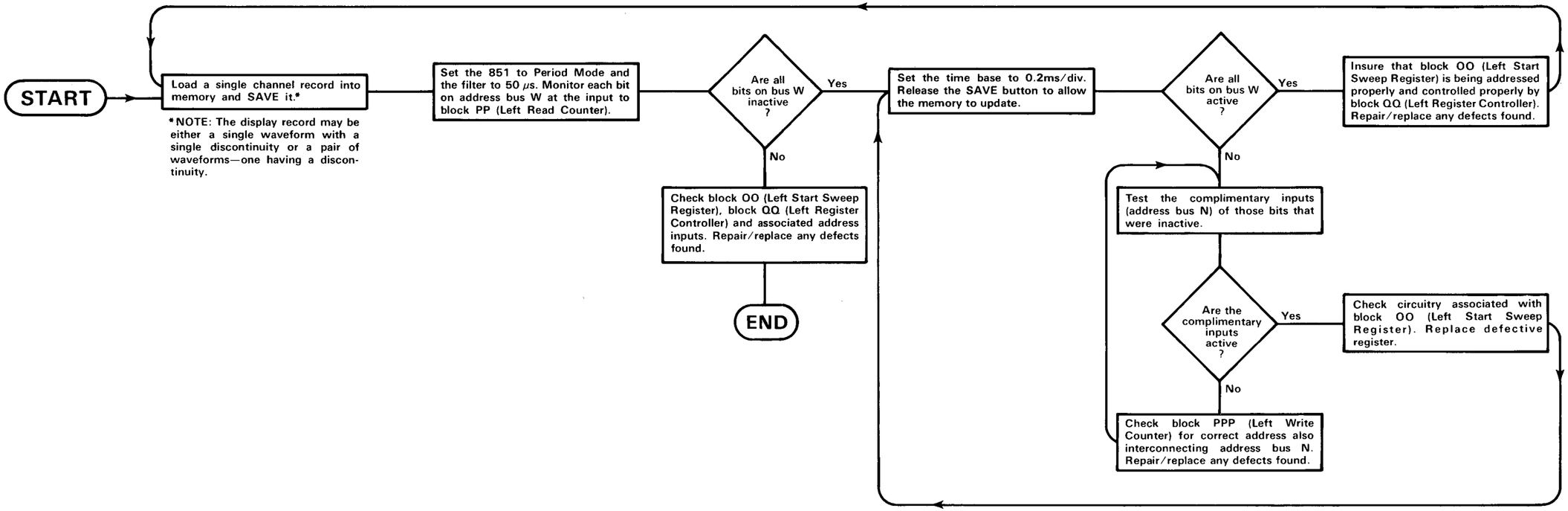
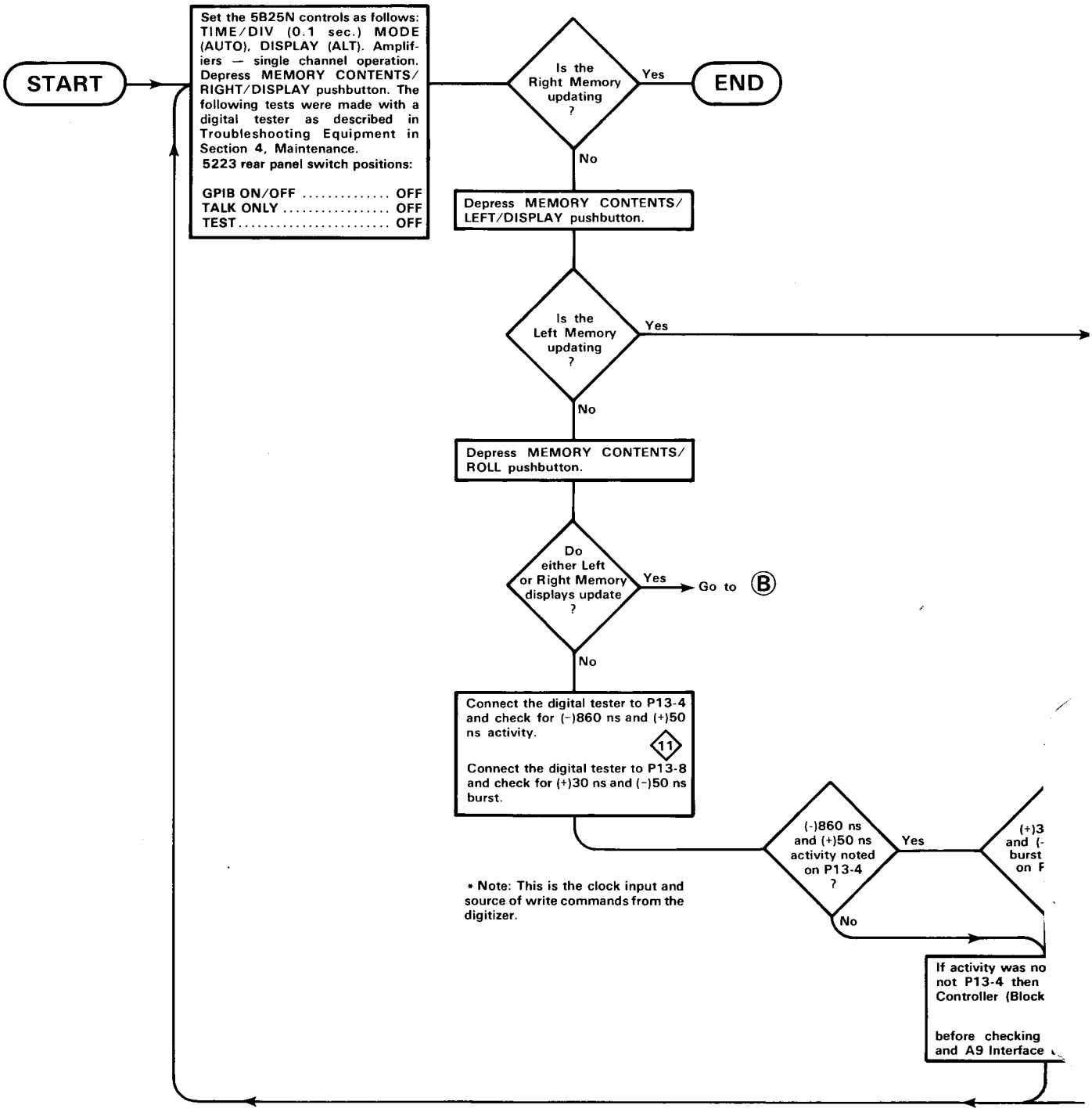


Figure A-5. Troubleshooting Chart D.

RIGHT MEMORY COMPARTMENT WILL NOT UPDATE



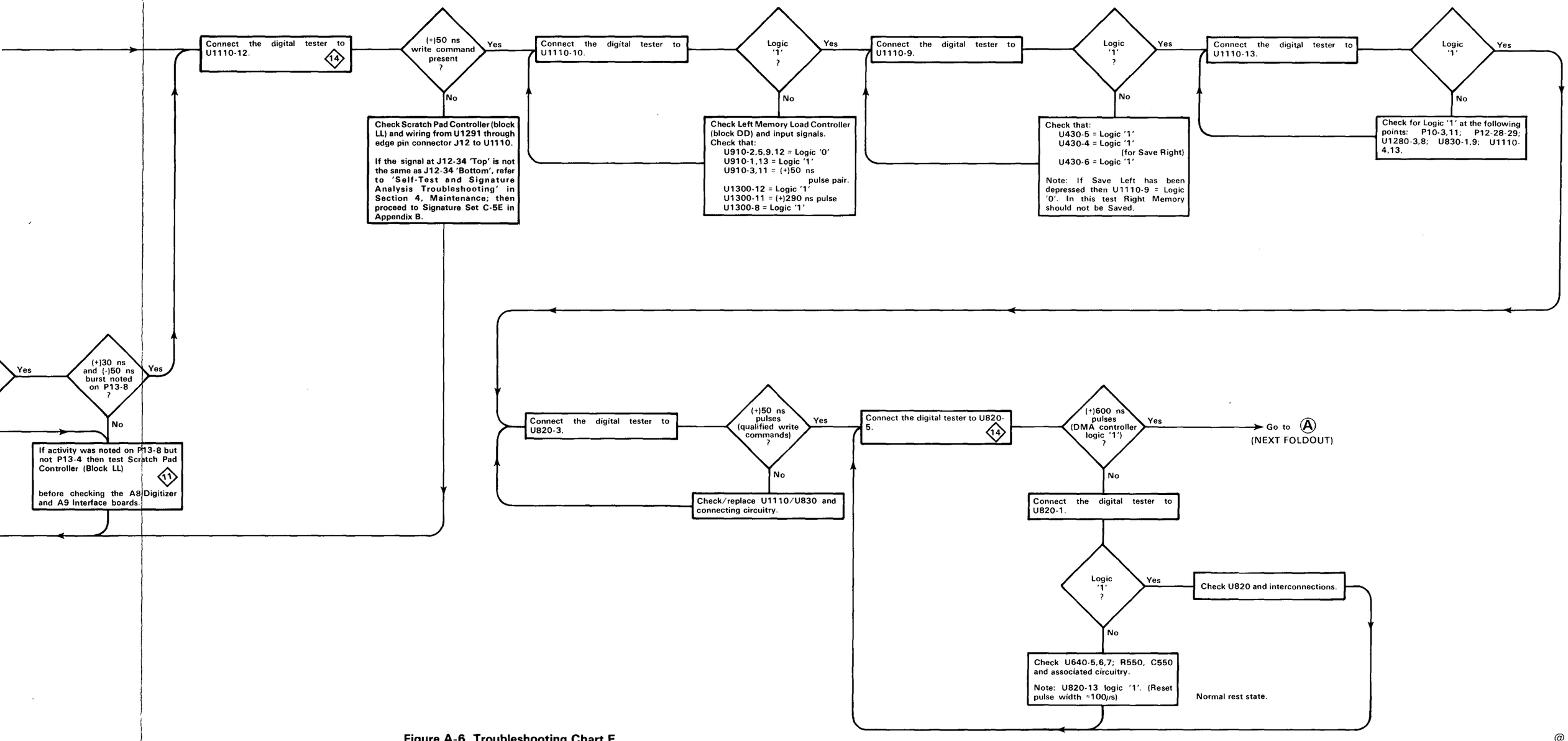
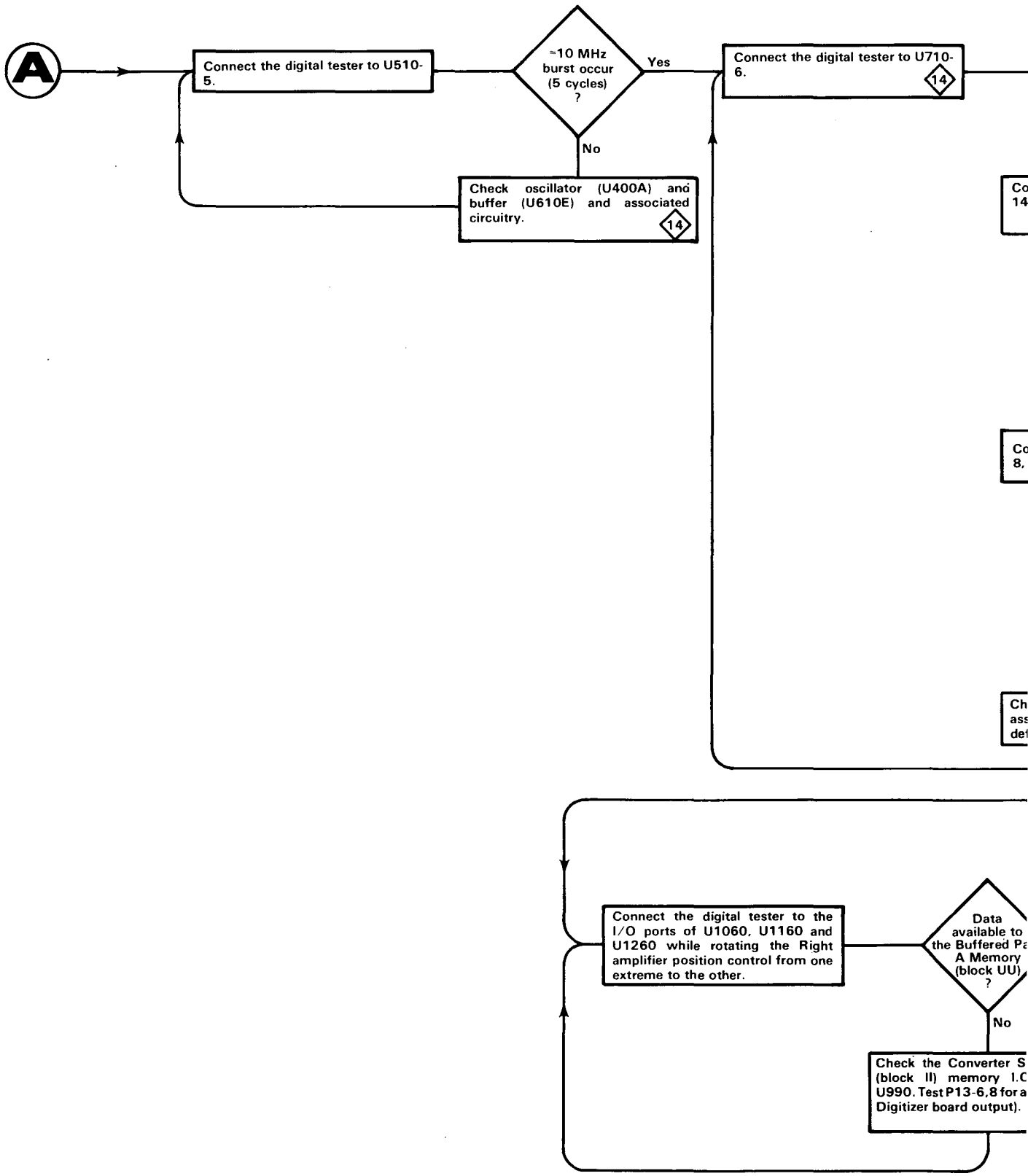


Figure A-6. Troubleshooting Chart E.

RIGHT MEMORY COMPARTMENT WILL NOT UPDATE (CONT)



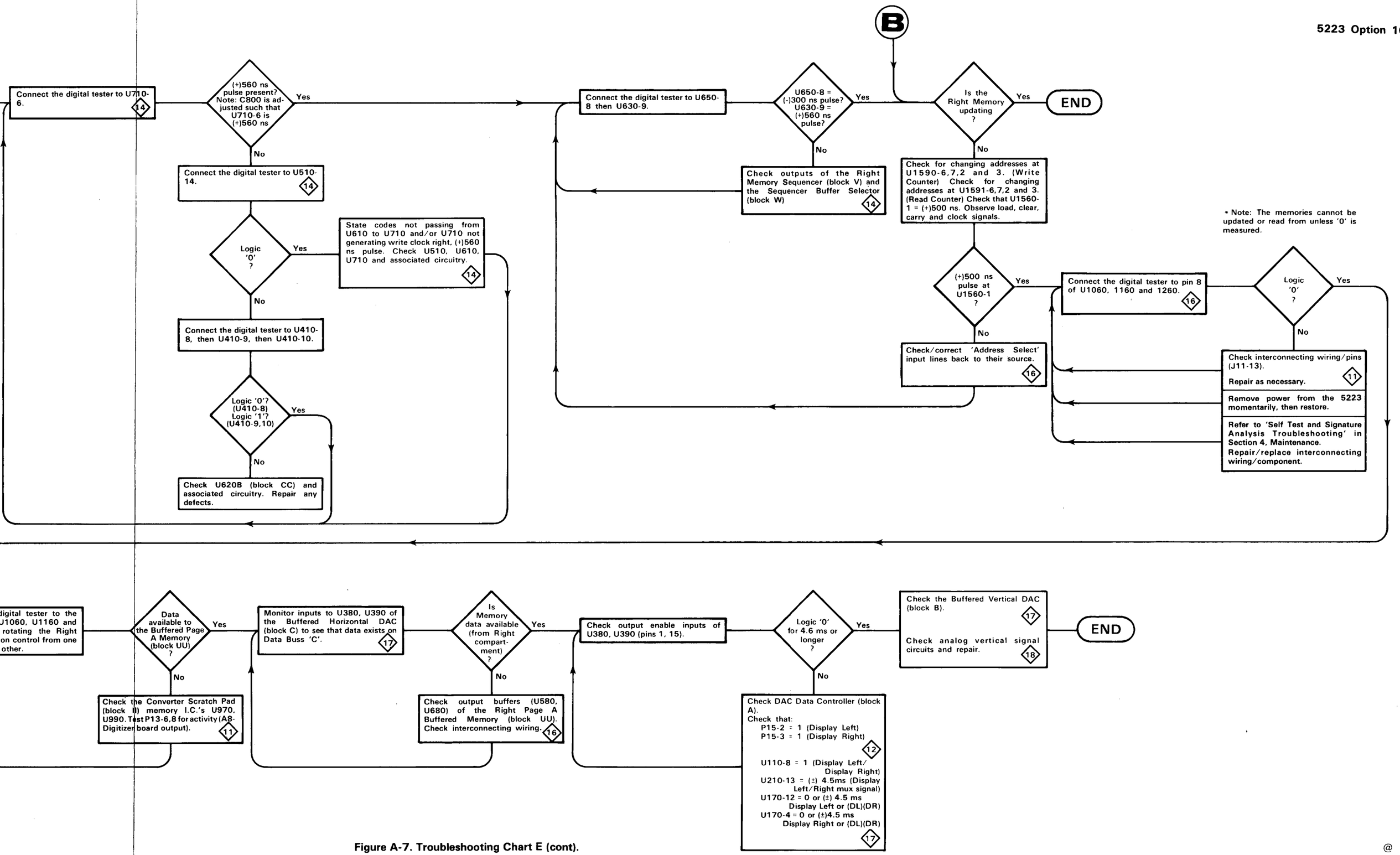
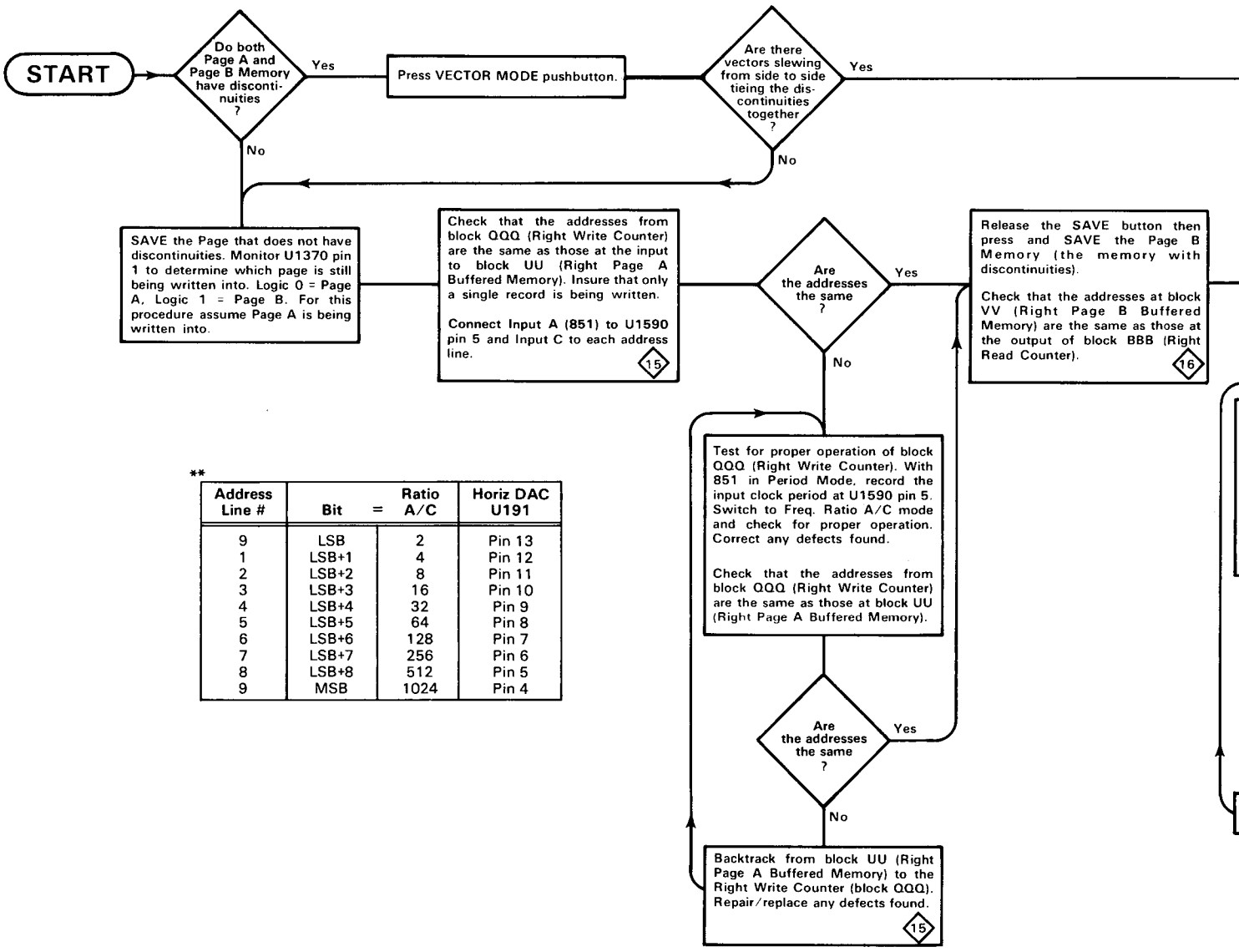


Figure A-7. Troubleshooting Chart E (cont).

RIGHT MEMORY DISPLAYED WAVEFORMS HAVE ADDRESSING PROBLEM

Use 851 Digital Tester in Freq Ratio A/C mode unless noted otherwise.



**

Address Line #	Bit	= Ratio A/C	Horiz DAC U191
9	LSB	2	Pin 13
1	LSB+1	4	Pin 12
2	LSB+2	8	Pin 11
3	LSB+3	16	Pin 10
4	LSB+4	32	Pin 9
5	LSB+5	64	Pin 8
6	LSB+6	128	Pin 7
7	LSB+7	256	Pin 6
8	LSB+8	512	Pin 5
9	MSB	1024	Pin 4

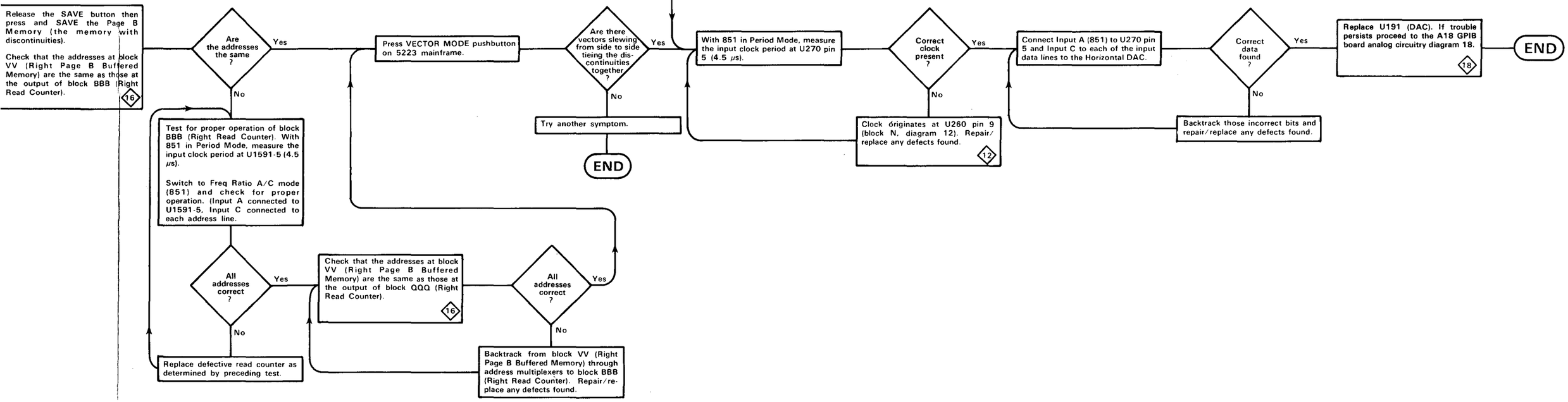


Figure A-8. Troubleshooting Chart F.

RIGHT MEMORY DISPLAYED WAVEFORMS HAVE START SWEEP PROBLEM

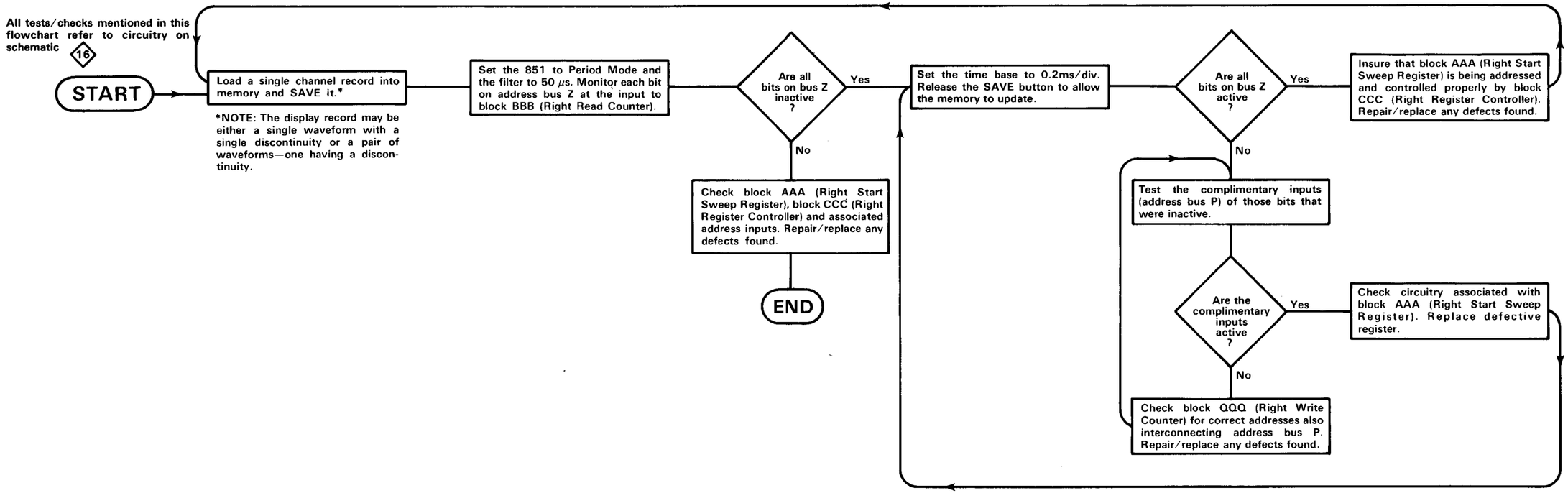


Figure A-9. Troubleshooting Chart G.

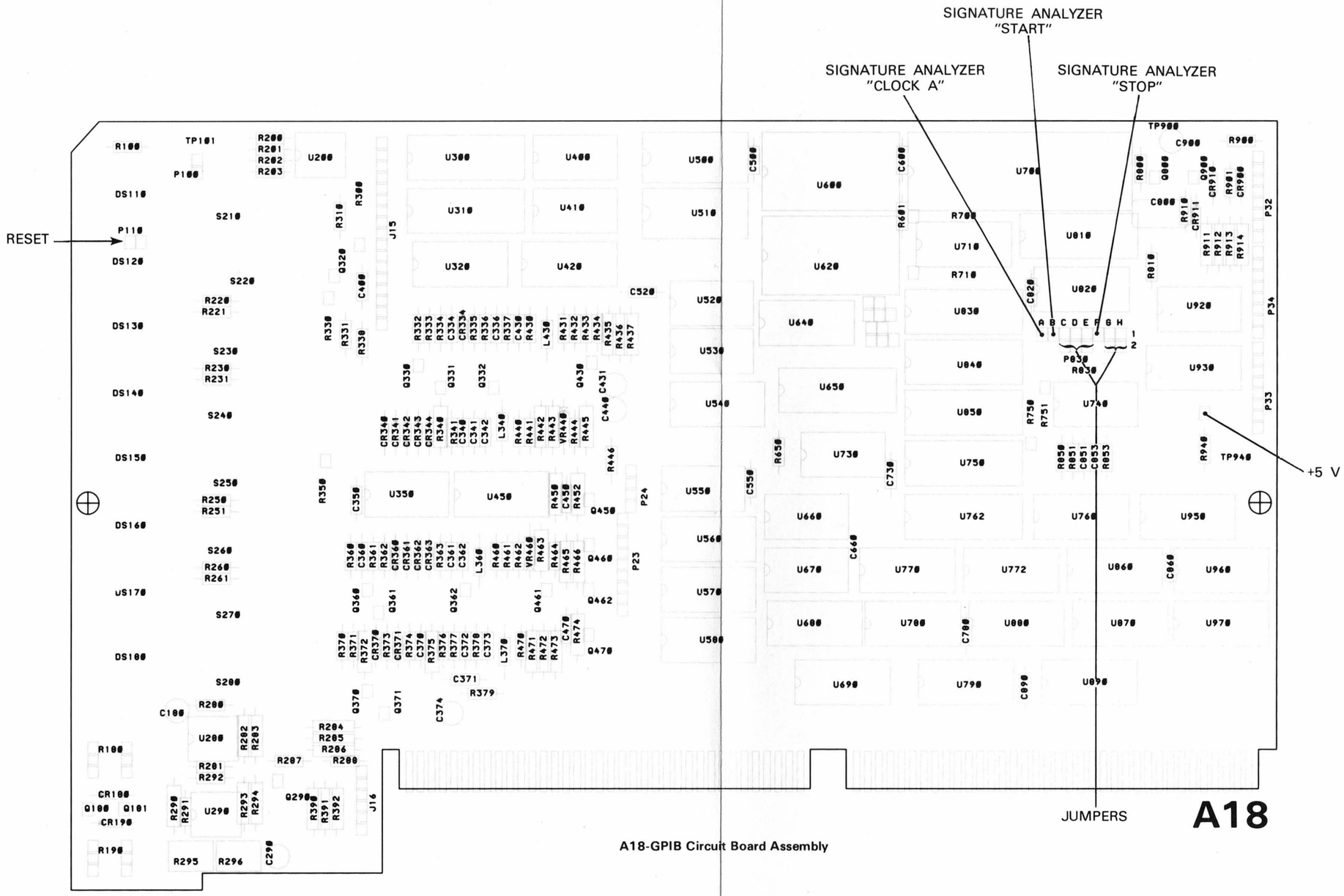
APPENDIX B

SIGNATURE ANALYSIS TROUBLESHOOTING FLOW-CHARTS AND SIGNATURE SETS

The following fold-out pages contain the Signature Analysis Troubleshooting Flow-Charts and associated Signature Sets used for performing signature analysis troubleshooting on the 5223 Option 10.

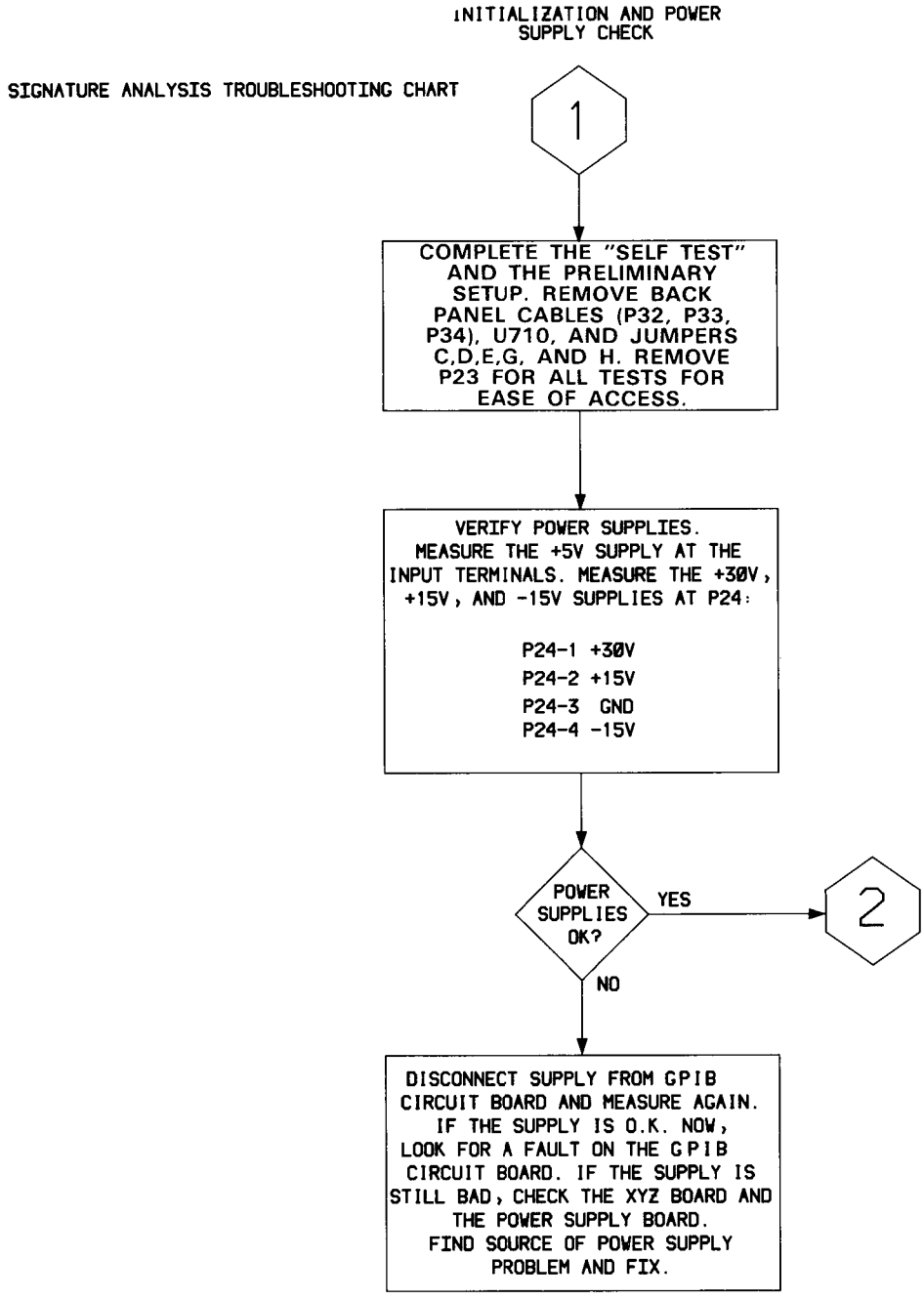
Though the power-up self-test may direct you to begin at a point other than at the beginning of these troubleshooting charts, it is important to perform the set-up procedure described in the Maintenance portion of this supplement before you start. The set-up procedure explains how to remove the A11-Memory board, install the Loop-Through board set, and select the necessary stimulation routines that excercise the 5223 Option 10 circuitry.

The Signature Analysis Troubleshooting Flow-Charts in this Appendix are arranged in procedural blocks. Each chart appears with its corresponding Signature Sets.



A18-GPIB Circuit Board Assembly

SIGNATURE ANALYSIS TROUBLESHOOTING CHART



@

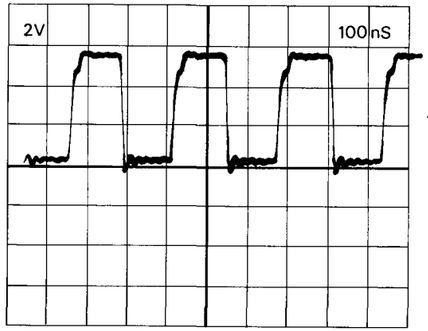
SIGNATURE ANALYSIS TROUBLESHOOTING CHART 2

VERIFY CLOCK OPERATION

CHECK Z80A CLOCK SPECIFICATIONS OBSERVE THE SIGNAL AT U700-6 WITH THE TEST OSCILLOSCOPE. THIS SIGNAL SHOULD:

1. BE A SQUARE-WAVE OF 3.7 TO 4MHz.
2. EXCEED 4.4V FOR AT LEAST 110NS.
3. BE LESS THAN 0.45V FOR AT LEAST 110NS.
4. BE WITHIN +5.3V AND -0.3V.

TYPICAL WAVEFORM:



WAVEFORM OK? YES → 4

NO

EXAMINE U920-11 FOR A 3.7 TO 4MHz TTL LEVEL SQUARE-WAVE.

WAVEFORM OK? NO → FIX OSCILLATOR CIRCUITRY (Q800, Q900, ETC.). BEGIN AT THE OSCILLATOR AND WORK BACK TO MICROPROCESSOR.

YES

LOOK FOR SQUARE-WAVE AT U810D-8.

WAVEFORM OK? NO → FIX U920E OR CONNECTION TO U810D.

YES

3

SIGNATURE ANALYSIS TROUBLESHOOTING CHART 3

IF SIGNAL AMPLITUDE IS A PROBLEM LOOK AT THE PULL-UP CIRCUITRY (R910, CR910, AND CR911). VERIFY PROPER RESISTOR VALUES, DIODE DIRECTIONS AND THE OPERATION OF U820D. IF THE CLOCK FREQUENCY FAILS TO MEET SPECIFICATIONS FOR HIGH AND LOW MINIMUM TIMES, THE FREQUENCY CAN BE ADJUSTED BY CHANGING C800. INCREASING THE VALUE OF C800 LOWERS THE FREQUENCY WHILE LOWERING THE VALUE OF C800 INCREASES THE THE FREQUENCY. FIND AND CORRECT THE PROBLEM.

2

@

SIGNATURE ANALYSIS TROUBLESHOOTING CHART

4

CHECK MICROPROCESSOR DC LEVELS AND VERIFY RESET

VERIFY DC LEVELS ON U700 (MICROPROCESSOR)
LOOK FOR 1'S ON THE INTERRUPTS (ACTIVE LOW). LOOK FOR Ø'S ON THE DATA BUS (MICROPROCESSOR FREE RUNNING).

PIN 7 <Ø.8V (D4)
PIN 8 <Ø.8V (D3)
PIN 9 <Ø.8V (D5)
PIN 10 <Ø.8V (D6)
PIN 11 +5V ± 5% (V_{cc})
PIN 12 <Ø.8V (D2)
PIN 13 <Ø.8V (D7)
PIN 14 <Ø.8V (DØ)
PIN 15 <Ø.8V (D1)
PIN 16 >2V ($\overline{INT}$)
PIN 17 >2V ($\overline{NMI}$)
PIN 25 >2V ($\overline{BUSRQ}$)
PIN 29 ØV (GROUND)

DATA BUS (MICROPROCESSOR FREE RUNNING)

VOLTAGES OK?

NO

VERIFY REMOVAL OF U710 AND JUMPERS C, D, E, G, AND H. LOOK FOR SHORTS, OPEN RESISTORS, ETC. CORRECT THE PROBLEM.

YES

VERIFY RESET OPERATION BY MEASURING VOLTAGE AT PIN 26 OF U700 WITH AN OSCILLOSCOPE OR VOLTMETER. U700 SHOULD BE >2V WHEN THE RESET TEST POINTS ARE OPEN, AND <Ø.8V WHEN THE TEST POINTS ARE SHORTED. THE HIGH TO LOW TRANSITION TIME SHOULD BE <Ø.5 SEC.

RESET OK?

NO

VERIFY U810-5 TO U700-26 CONNECTION. CORRECT THE PROBLEM.

YES

5

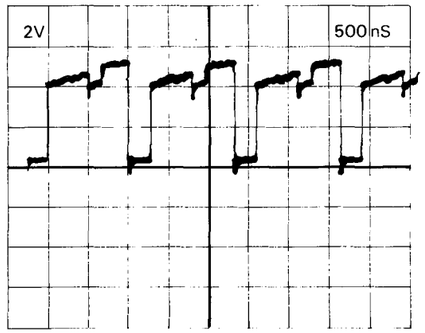
SIGNATURE ANALYSIS TROUBLESHOOTING CHART

5

CHECK WAIT STATE GENERATOR

VERIFY THE WAIT SIGNAL TO U700 IS OK. WITH TEST OSCILLOSCOPE, LOOK AT THE SIGNAL ON PIN 24 OF U700. THIS SIGNAL SHOULD BE A TTL LEVEL, NEGATIVE-GOING PULSE TRAIN OF 800KHz:

TYPICAL WAVEFORM:



WAVEFORM OK?

YES

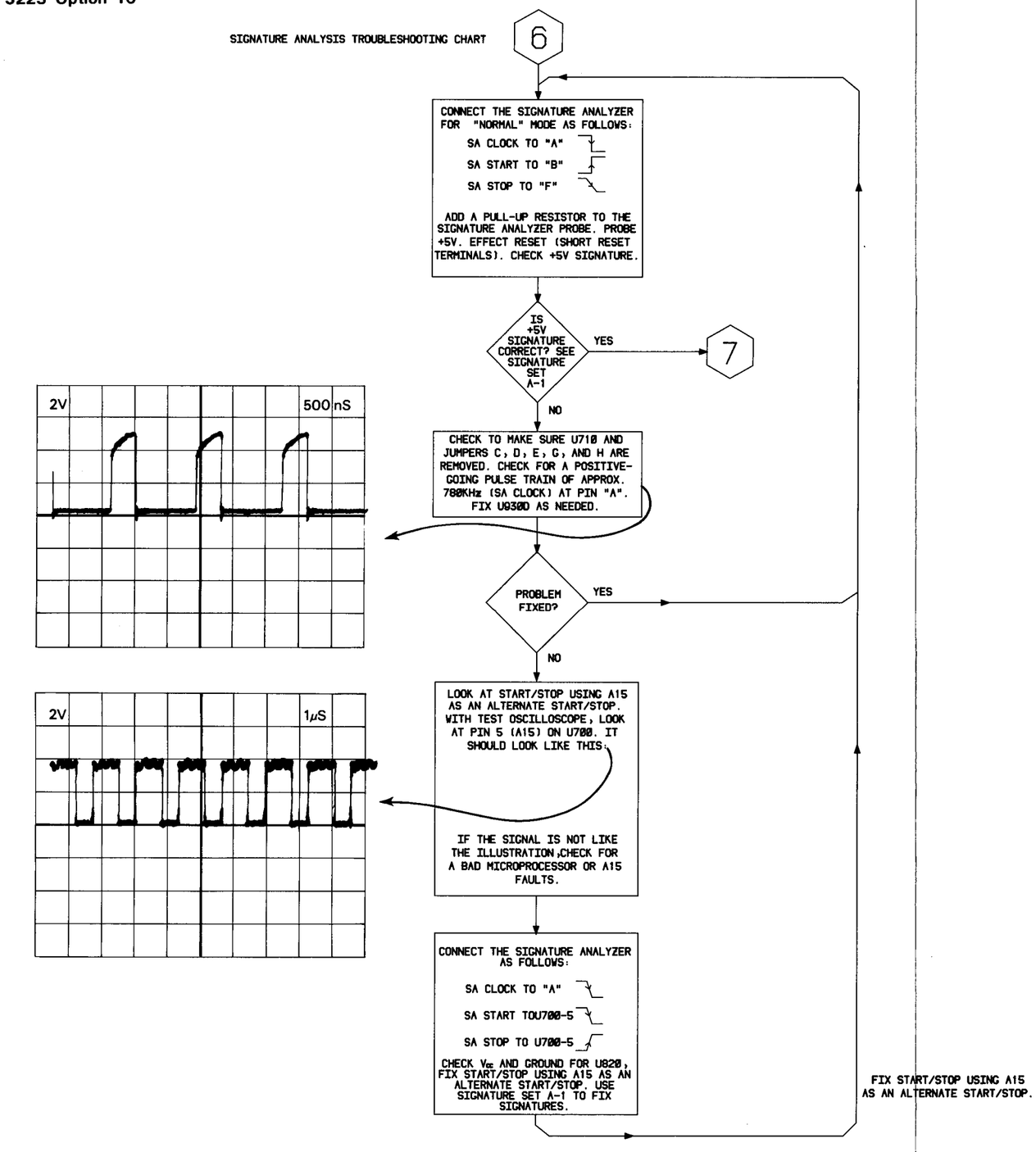
6

NO

WITH THE TEST OSCILLOSCOPE, CHECK PIN 12 OF U950B FOR A SQUARE WAVE OF APPROX. 3.8MHz. ALSO VERIFY THE POWER SUPPLIES TO U920, U930, AND U950. ALSO CHECK THAT PINS 11 AND 14 OF U950B ARE AT +5V. LOOK FOR SHORTED OR OPEN CIRCUIT BOARD RUNS. IF THE PROBLEM CANNOT BE FOUND, LOOK AT THE SETS , RESETS, CLOCKS, ETC. OF THE FLIP FLOPS TO VERIFY PROPER LOGICAL ACTION. IF ALL THE LOGIC LOOKS OK, THEN CONSIDER THAT THE MICROPROCESSOR MAY BE ILL. CORRECT THE PROBLEM.

@

5223 Option 10



@

SIGNATURE SET A-1

SET-UP

5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A
START: U820-5
STOP: U820-5

Pin	Name	Signatures
+5V		755U
U700-2	(A12)	AC99
U700-3	(A13)	PCF3
U700-4	(A14)	1180
U700-5		0000
U700-28	(RFSH)	755U
U820-1	(A12)	AC99
U820-2	(A13)	PCF3
U820-3	(A14)	1180
U820-4		0000
U820-5	(A15)	0000
U820-6	(RFSH)	755U
U820-7	(Y7)	U731

SIGNATURE SET A-2

SET-UP

5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Boards Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		4POA
U810-3	(A3)	OP40
U810-7	(WR)	4POA
U810-9	(RD)	0000
U810-14	(A0)	F5U9
U810-16	(A1)	4357
U810-18	(A2)	PA44

SIGNATURE SET A-3

SET-UP

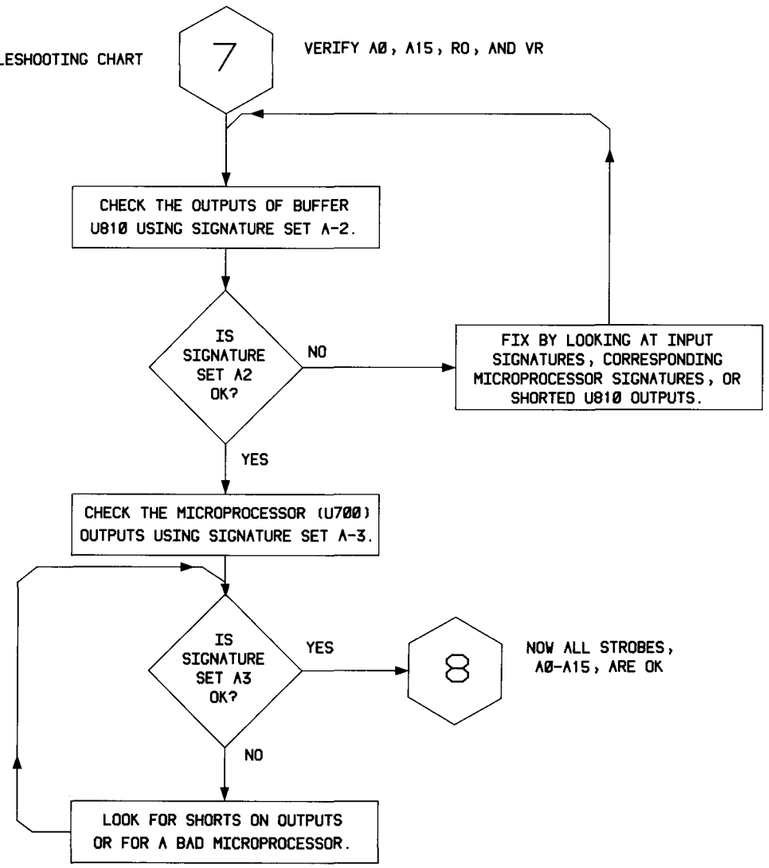
5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

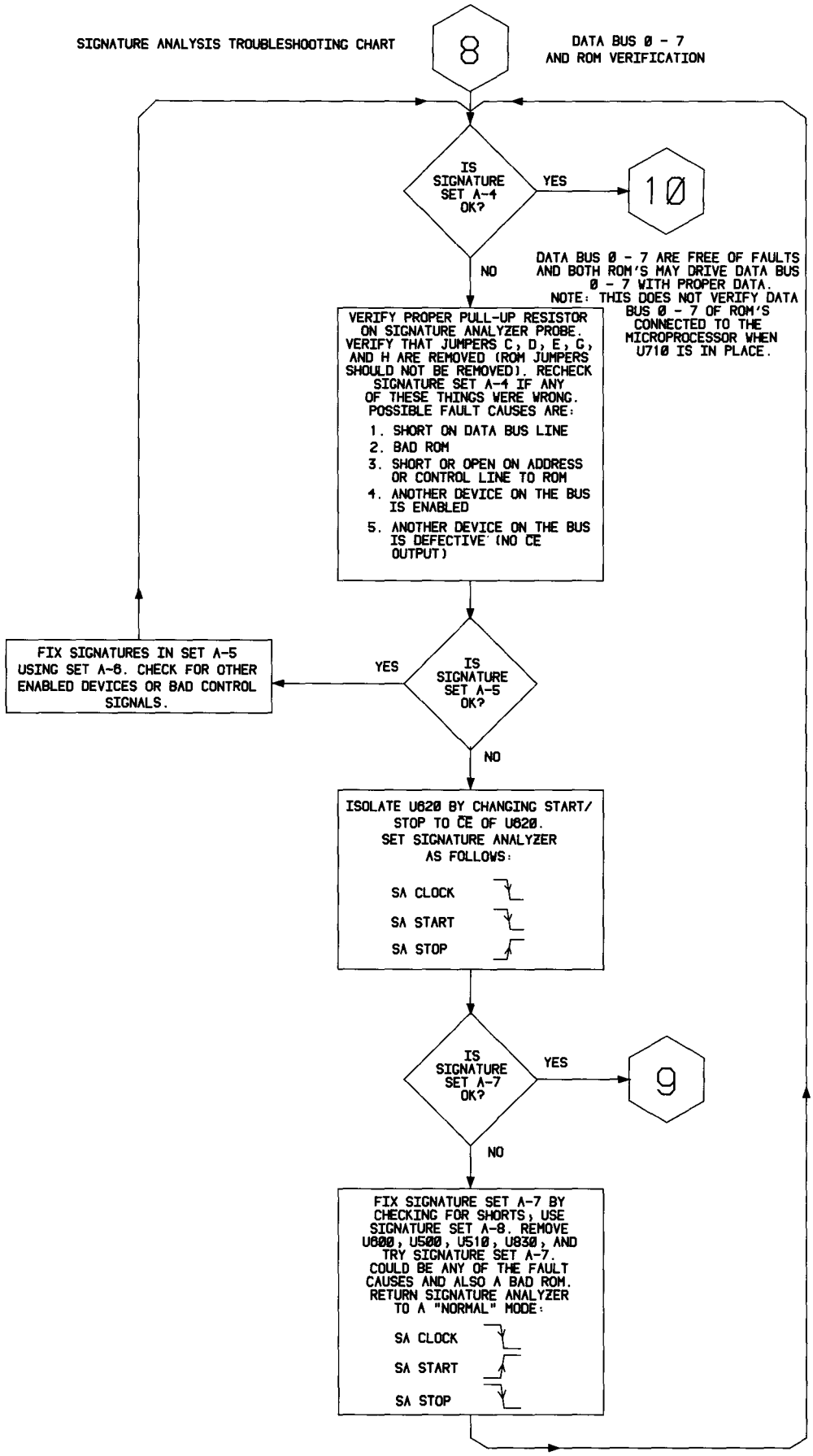
Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		4POA
U700-1	(A11)	4P5F
U700-2	(A12)	AFH7
U700-3	(A13)	759F
U700-4	(A14)	4HCC
U700-5	(A15)	561H
U700-19	(MREQ)	0000
U700-28	(RFSH)	4POA
U700-27	(M1)	0000
U700-34	(A4)	555C
U700-35	(A5)	FC92
U700-36	(A6)	PPCC
U700-37	(A7)	HH90
U700-38	(A8)	AHPP
U700-39	(A9)	H7U6
U700-40	(A10)	8058

SIGNATURE ANALYSIS TROUBLESHOOTING CHART



5223 Option 10



@

SIGNATURE SET A-4

SET-UP

5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		4POA
U620-9	(DB0)	1P34
U620-10	(DB1)	3A1F
U620-11	(DB2)	8U1U
U620-13	(DB3)	985U
U620-14	(DB4)	5P30
U620-15	(DB5)	7UUP
U620-16	(DB6)	4PHC
U620-17	(DB7)	0856

SIGNATURE SET A-5

SET-UP

5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		4POA
U830-10	(GND)	
U830-19	(EN,TTL High)	
U830-20	(Vcc)	
U500-8	(CS, TTL High)	
U500-9	(GND)	
U500-18	(Vcc)	
U510-8	(CS, TTL High)	
U510-9	(GND)	
U510-18	(Vcc)	
U600-12	(GND)	
U600-24	(Vcc)	
U620-12	(GND)	
U620-24	(Vcc)	
U620-18	(CE)	P461
U620-20	(OE)	P461
U600-18	(CE)	PHU6
U600-20	(OE)	PHU6

SIGNATURE SET A-6

SET-UP

5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		4POA
U820-1	(A12)	AFH7
U820-2	(A13)	759F
U820-3	(A14)	4HCC
U820-4	(GND)	0000
U820-5	(A15)	561H
U820-6	(RFSH)	4POA
U820-14	(Y1)	P461
U820-15	(Y0)	PHU6

SIGNATURE SET A-7

SET-UP

5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: U820-14 ↓
STOP: U820-14 ↑

Pin	Name	Signatures
+5V		826P
U620-9	(DB0)	C34C
U620-10	(DB1)	3040
U620-11	(DB2)	2094
U620-13	(DB3)	3873
U620-14	(DB4)	809U
U620-15	(DB5)	6H97
U620-16	(DB6)	4A2U
U620-17	(DB7)	3F42

SIGNATURE SET A-8

SET-UP

5223 OPTION 10:
TEST switch on.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: U820-14 ↓
STOP: U820-14 ↑

Pin	Name	Signatures
+5V		826P
U620-1	(A7)	C25F
U620-2	(A6)	7C47
U620-3	(A5)	3319
U620-4	(A4)	8P3U
U620-5	(A3)	C133
U620-6	(A2)	A206
U620-7	(A1)	2A1F
U620-8	(A0)	7P25
U620-12	(GND)	
U620-18	(CE)	0000
U620-19	(A10)	HP66
U620-20	(OE)	0000
U620-21	(A11)	826P
U620-22	(A9)	19H6
U620-23	(A8)	5H21
U620-24	(Vcc)	

SIGNATURE SET A-9

SET-UP

5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: U820-14 ↓
STOP: U820-14 ↑

Pin	Name	Signatures
+5V		826P
U600-9	(DB0)	C34C
U600-10	(DB1)	3040
U600-11	(DB2)	2094
U600-13	(DB3)	3873
U600-14	(DB4)	809U
U600-15	(DB5)	6H97
U600-16	(DB6)	4A2U
U600-17	(DB7)	3F42

SIGNATURE SET A-10

SET-UP

5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: U820-15 ↓
STOP: U820-15 ↑

Pin	Name	Signatures
+5V		826P
U600-9	(DB0)	1A23
U600-10	(DB1)	4HPH
U600-11	(DB2)	9635
U600-13	(DB3)	67HA
U600-14	(DB4)	U113
U600-15	(DB5)	0HUU
U600-16	(DB6)	0A62
U600-17	(DB7)	986H

SIGNATURE SET A-11

SET-UP

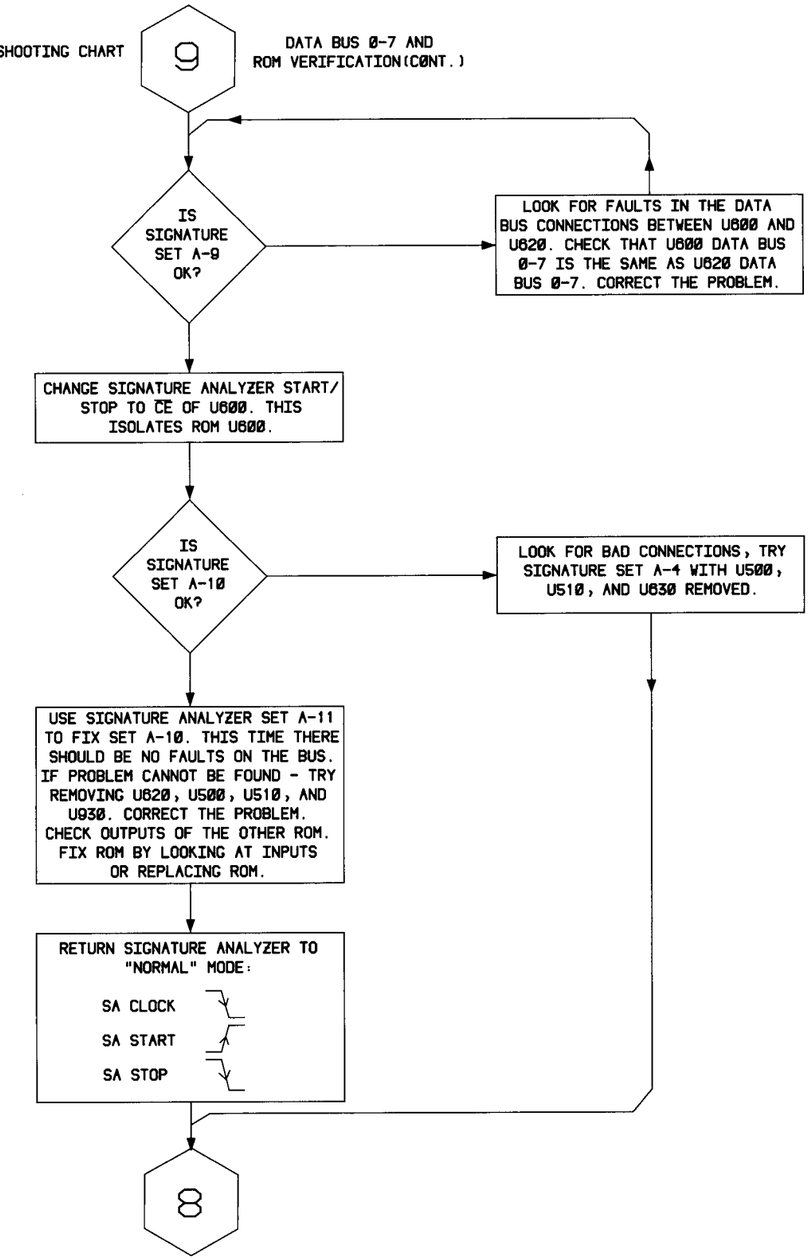
5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers C, D, E, G, and H removed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: U820-15 ↓
STOP: U820-15 ↑

Pin	Name	Signatures
U600-1	(A7)	C25F
U600-2	(A6)	7C47
U600-3	(A5)	3319
U600-4	(A4)	8P3U
U600-5	(A3)	C133
U600-6	(A2)	A206
U600-7	(A1)	2A1F
U600-8	(A0)	7P25
U600-12	(GND)	
U600-18	(CE)	0000
U600-19	(A10)	HP66
U600-20	(OE)	0000
U600-21	(A11)	7A70
U600-22	(A9)	19H6
U600-23	(A8)	5H21

SIGNATURE ANALYSIS TROUBLESHOOTING CHART



SIGNATURE SET B-1

SET-UP

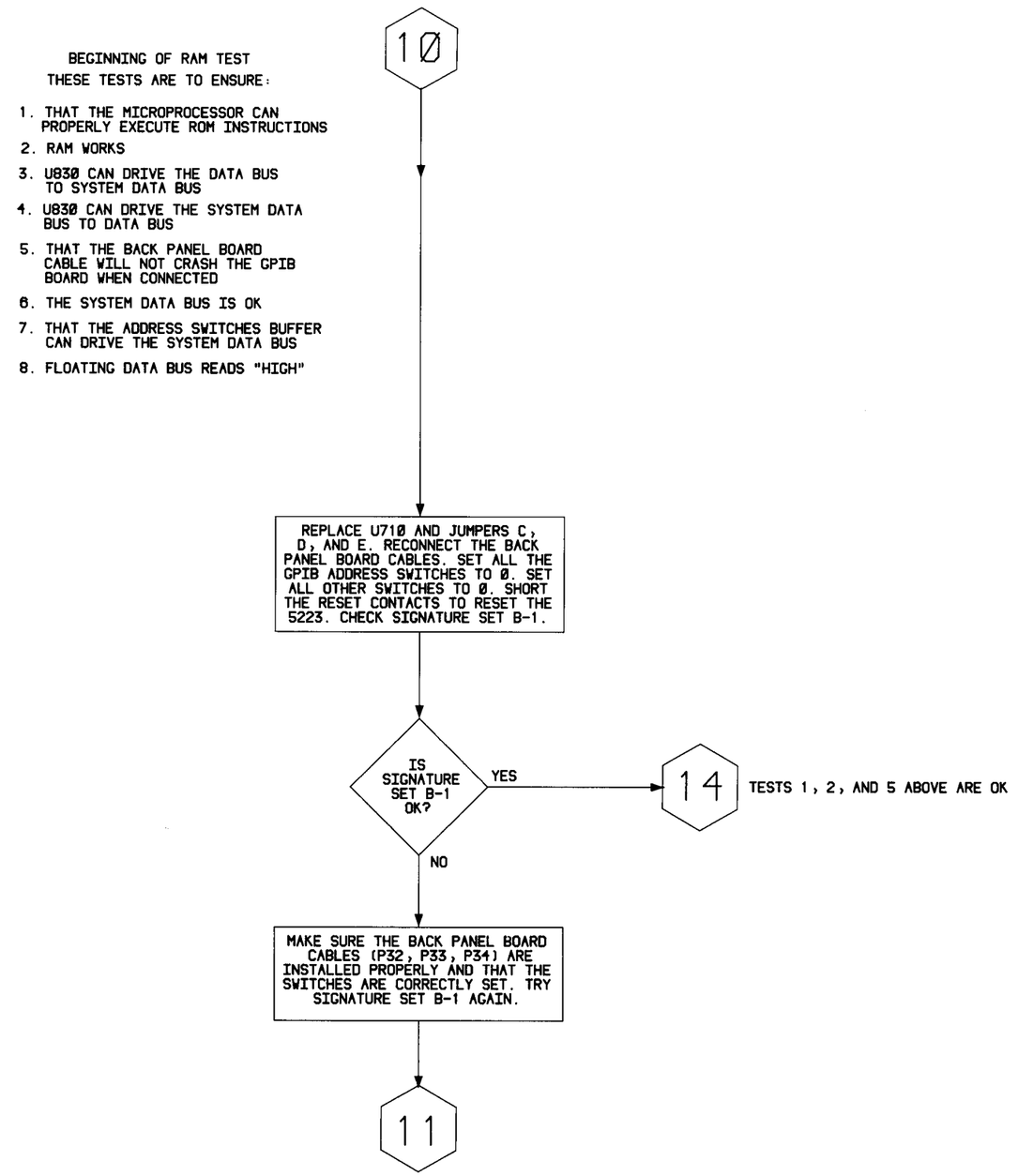
5223 OPTION 10:
TEST switch ON.
Stimulation routine 0 running.
U710 installed.
Jumpers G, and H removed; Jumpers C, D, and E installed.
Back Panel Board Cables; P32, P33, and P34 connected.
Set all rear-panel switches to zero.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A
START: B
STOP: F

Pin	Name	Signatures
+5V		7442
U700-7	(DB4)	04P6
U700-8	(DB3)	3HF7
U700-9	(DB5)	4682
U700-10	(DB6)	4H4U
U700-12	(DB2)	7641
U700-13	(DB7)	4HA4
U700-14	(DB0)	83P1
U700-15	(DB1)	C680

SIGNATURE ANALYSIS TROUBLESHOOTING CHART



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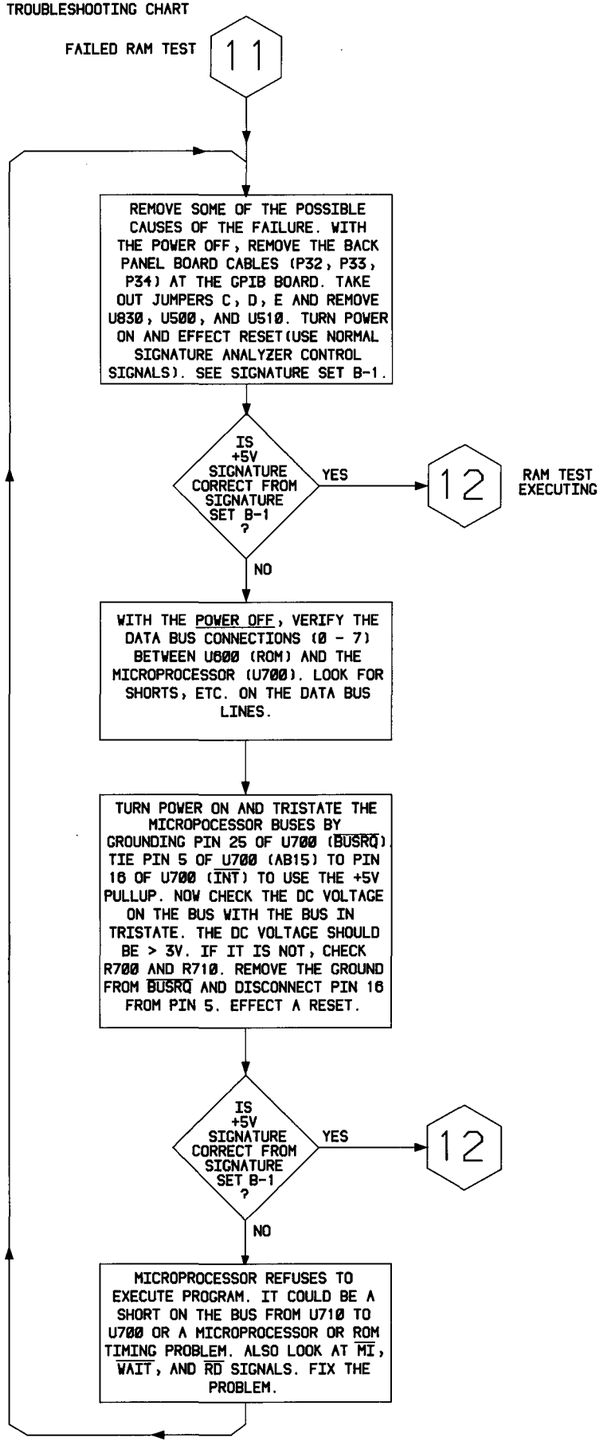
SIGNATURE ANALYSIS TROUBLESHOOTING CHART

SIGNATURE ANALYSIS
RAM TEST (Continued)



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SIGNATURE SET B-1

SET-UP

5223 OPTION 10:
- TEST switch ON.
- Stimulation routine 0 running.
- U710 installed.
- Jumpers G, and H removed; Jumpers C, D, and E installed.
- Back Panel Board Cables; P32, P33, and P34 connected.
- Set all rear-panel switches to zero.

SIGNATURE ANALYZER:

- Install pull-up resistor on probe.
- CLOCK: A ⊓
- START: B ⊔
- STOP: F ⊓

Pin	Name	Signatures
+5V		7442
U700-7	(DB4)	04P6
U700-8	(DB3)	3HF7
U700-9	(DB5)	4682
U700-10	(DB6)	4H4U
U700-12	(DB2)	7641
U700-13	(DB7)	4HA4
U700-14	(DB0)	83P1
U700-15	(DB1)	C680

SIGNATURE SET B-2

SET-UP

5223 OPTION 10:
TEST switch ON:
Stimulation routine 0 running.
U710 installed.
Jumpers D, E, G, and H removed; Jumper C installed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5		7442
U700-7	(DB4)	04P6
U700-8	(DB3)	3HF7
U700-9	(DB5)	4682
U700-10	(DB6)	4H4U
U700-12	(DB2)	7641
U700-13	(DB7)	8PP4
U700-14	(DB0)	83P1
U700-15	(DB1)	C680

SIGNATURE SET B-3

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 0 running.
U710 installed.
Jumpers, C, D, E, G, and H removed.
Back Panel Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		7442
U500-11	(DB7)	1344
U500-12	(DB6)	2209
U500-13	(DB5)	3A54
U500-14	(DB4)	F18P
U510-11	(DB3)	9FU3
U510-12	(DB2)	5528
U510-13	(DB1)	7372
U510-14	(DB0)	5485

SIGNATURE SET B-4

SET-UP

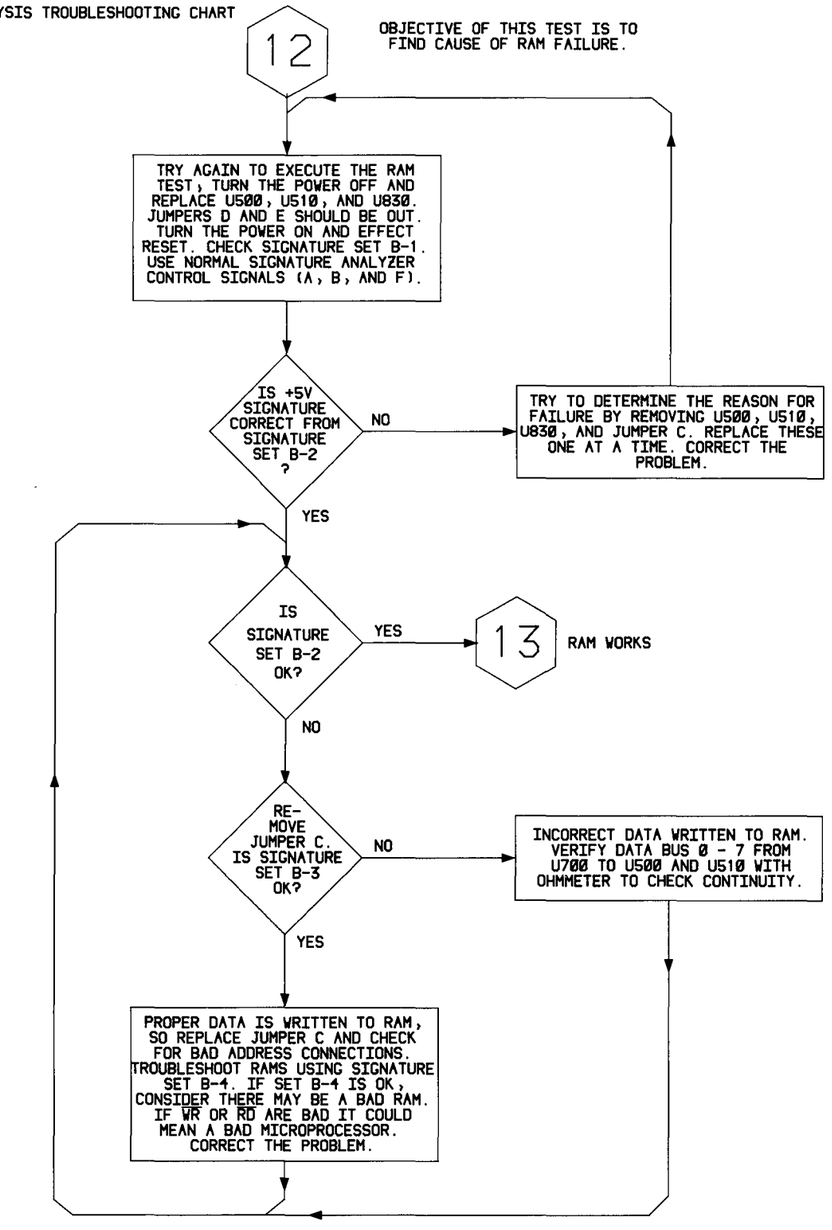
5223 OPTION 10:
TEST switch on.
Stimulation routine 0 running.
U710 installed.
Jumpers D, E, G, and H removed; jumper C installed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		7442
U500, U510-10	(WE)	PHC8
U500, U510-1	(A6)	0234
U500, U510-2	(A5)	8AF9
U500, U510-3	(A4)	331A
U500, U510-4	(A3)	3914
U500, U510-5	(A0)	IU81
U500, U510-6	(A1)	H168
U500, U510-7	(A2)	3152
U500, U510-8	(CS)	H6F7
U500, U510-10	(WE)	PHC8
U500, U510-15	(A9)	AUUA
U500, U510-16	(A8)	U3U6
U500, U510-17	(A7)	56U4
U520-9	(WR)	PHC8
U520-10	(RD)	99UA
U530-9		0000
U530-10		H6F7

SIGNATURE ANALYSIS TROUBLESHOOTING CHART



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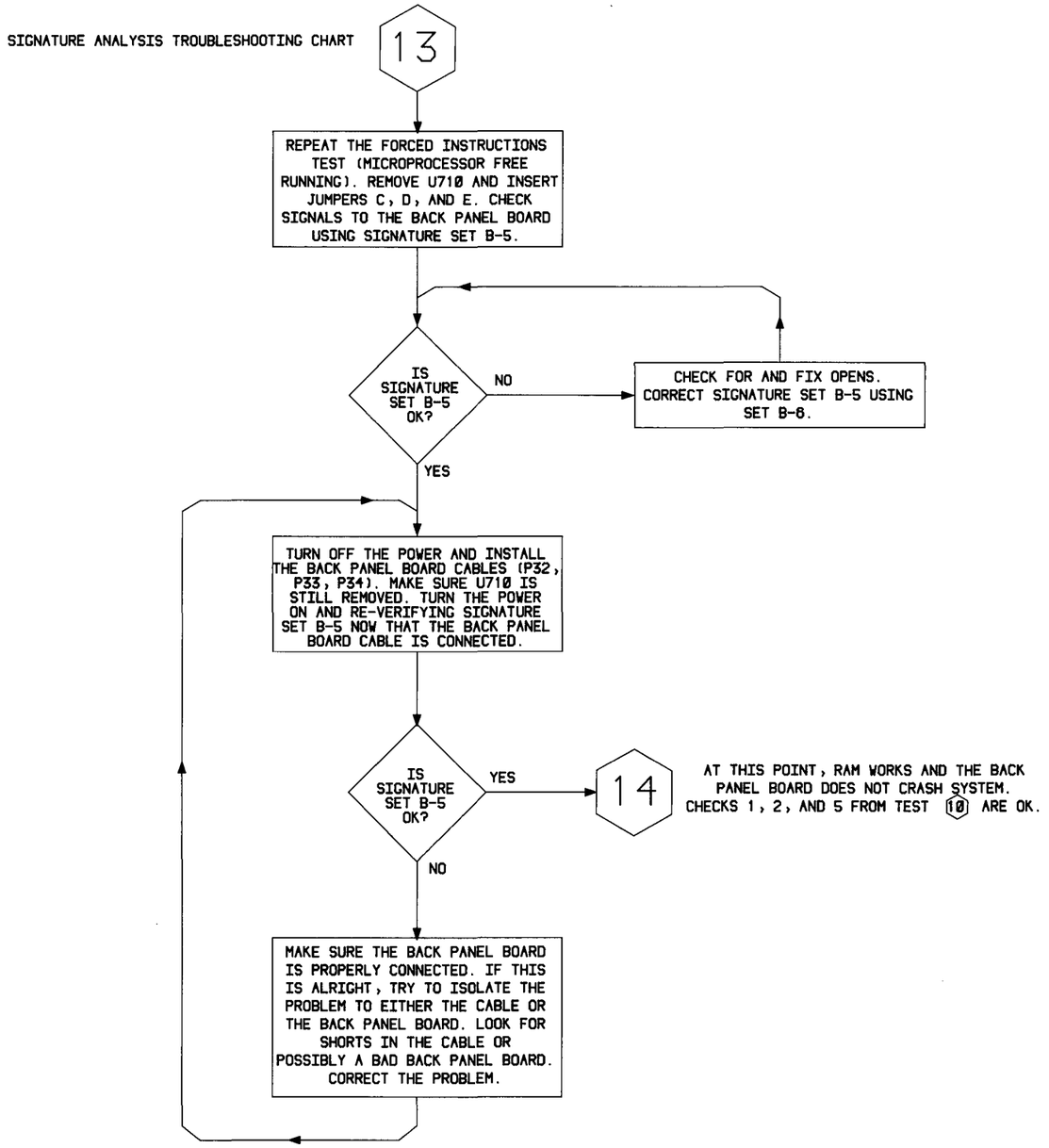

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SIGNATURE SET B-5

SET-UP

5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers G, and H removed; jumpers C, D, and E installed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A
START: B
STOP: F

Remove jumpers D and E, effect RESET then re-install jumpers D and E before taking signatures.

Pin	Name	Signatures
+5V		4P0A
P34-3	(ADD SEL)	5FUP
P34-4	(A1)	4357
P34-5	(A2)	PA44
P34-6	(A3)	OP40
P32-7	VCL	(+5V)
P32-8	GND	(0V)

SIGNATURE SET B-6

SET-UP

5223 OPTION 10:
TEST switch ON.
Microprocessor free running (Stimulation routine 0).
U710 removed.
Jumpers G, and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A
START: B
STOP: F

Pin	Name	Signatures
+5V		4P0A
U640-1	(A1)	4357
U640-2	(A2)	PA44
U640-3	(A3)	OP40
U640-4	(Y4 OF U820)	2P30
U640-5	(RD)	0000
U640-6	(A11)	4P5F
U640-7	(ADDSEL)	5FUP
U640-8	(GND)	0V
U640-16	(VCC)	+5V

SIGNATURE SET B-7

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 0 running.
U710 installed.
Jumpers G, and H removed; jumpers C, D, and E installed.
Back Panel Board Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A
START: B
STOP: F

To take these signatures first set all rear-panel switches to 0, remove jumpers D and E and effect RESET. Re-install jumpers D and E and take signatures for all switches in 0 position, then set all switches to 1 position and take remaining signatures.

Pin	Name	Rear-panel GPIB Select Switches Set For: 0	1	Name
U830-11	(SD0)	957U	563U	GPIB-1
U830-12	(SD7)	97HC	549C	GPIB ON/OFF
U830-13	(SD1)	31CP	U2UP	GPIB-2
U830-14	(SD6)	P4P7	27A7	TALK ONLY
U830-15	(SD2)	F371	0031	GPIB-4
U830-16	(SD5)	3549	U609	TEST
U830-17	(SD3)	7936	CA76	GPIB-8
U730-18	(SD4)	5723	9463	GPIB-16

SIGNATURE SET B-8

SET-UP

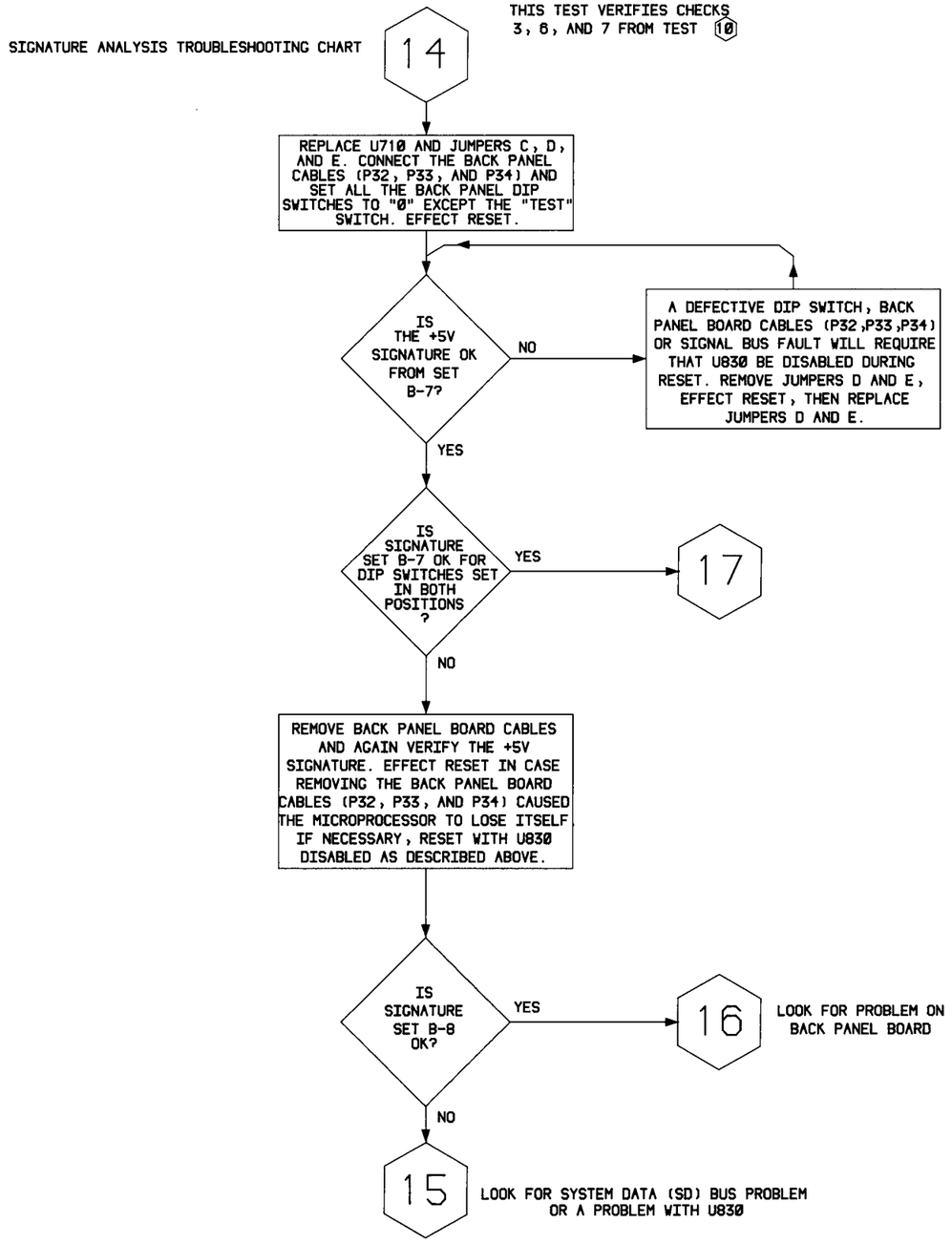
5223 OPTION 10:
TEST switch ON.
Stimulation routine 0 running.
U710 installed.
Jumpers G, and H removed; jumpers C, D, and E installed.
Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A
START: B
STOP: F

To take these signatures just set all rear-panel switches to 0, remove jumpers D and E, effect RESET, re-install jumpers D and E, then take signatures.

Pin	Name	Signatures
+5 V		7442
U830-11	(SD0)	957U
U830-12	(SD7)	549C
U830-13	(SD1)	31CP
U830-14	(SD6)	P4P7
U830-15	(SD2)	F371
U830-16	(SD5)	3549
U830-17	(SD3)	7936
U830-18	(SD4)	5723



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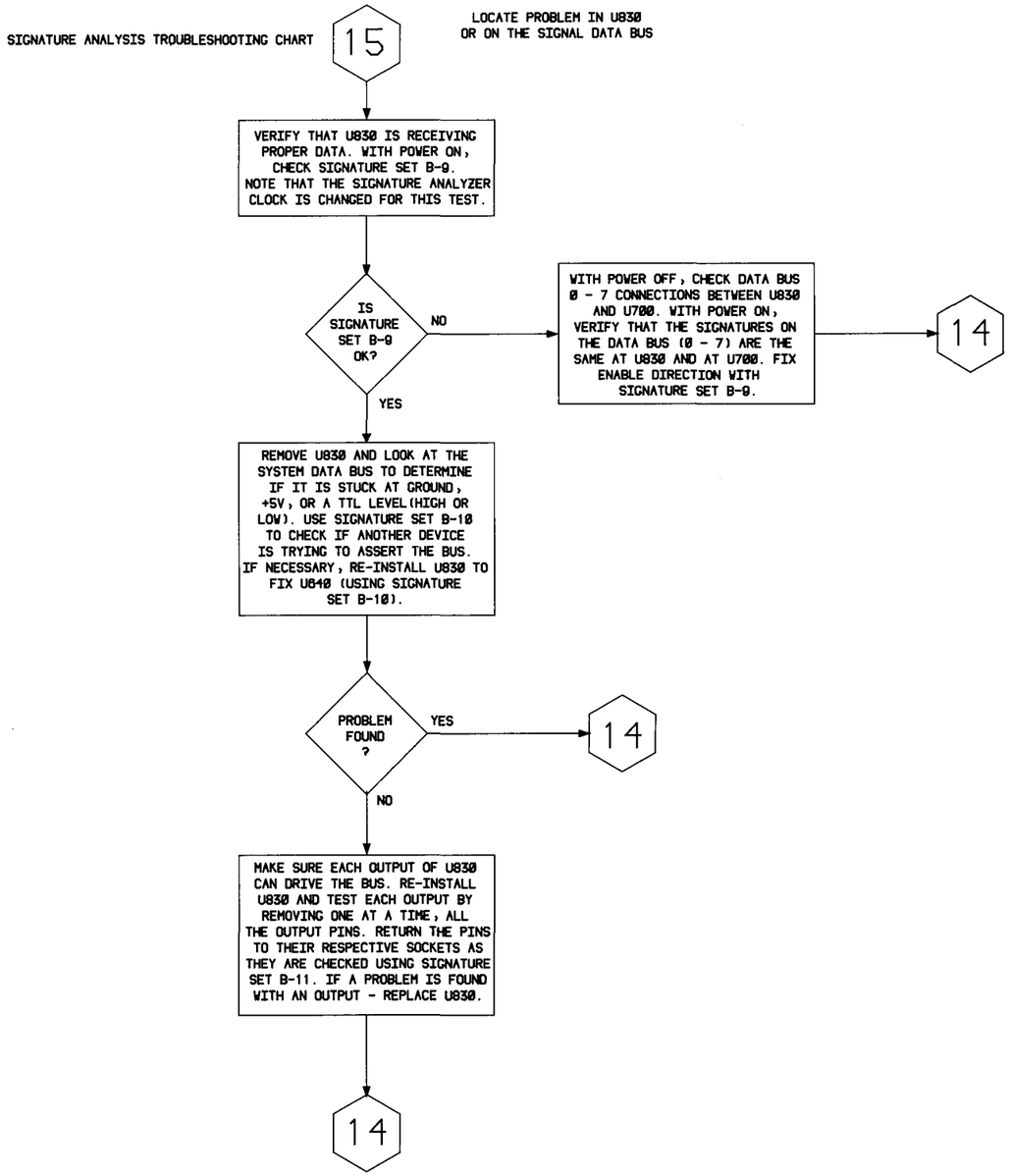

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SIGNATURE SET B-9

SET-UP

5223 OPTION 10:
- TEST switch ON.
- Stimulation routine 0 running.
- U710 installed.
- Jumpers G, and H removed; jumpers C, D, and E installed.
- Back Panel Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

To take these signatures just set all rear-panel switches to 0, remove jumpers D and E, effect RESET, re-install jumpers D and E, then take signatures.

Pin	Name	Signatures
+5V		6055
U830-1	$\overline{RD}$	6055
U830-2	(DB4)	8CF2
U830-3	(DB3)	8F84
U830-4	(DB5)	54HH
U830-5	(DB2)	P06U
U830-6	(DB6)	1467
U830-7	(DB1)	FFC2
U830-8	(DB7)	P7C8
U830-9	(DB0)	9P3U
U830-10	(GND)	0V
U520-12		6055
U520-13		HA08
U830-19	(EN)	HA08
U830-20	(Vcc)	+5V

SIGNATURE SET B-10

SET-UP

5223 OPTION 10:
- TEST switch ON.
- Stimulation routine 0 running.
- U710 installed.
- Jumpers G, and H removed; jumpers C, D, and E installed.
- Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

To take these signatures just set all rear-panel switches to 0, remove jumpers D and E, effect RESET, re-install jumpers D and E, then take signatures.

Pin	Name	Signatures
+5V		7442
U320-15		TTL HIGH
U420-15		TTL HIGH
U560-15		TTL HIGH
U570-15		TTL HIGH
U580-15		TTL HIGH
U640-8	(GND)	(0V)
U640-16	(Vcc)	(5V)
U860-15		TTL HIGH
U880-15		TTL HIGH
U890-15		TTL HIGH
U640-1		H168
U640-2		3152
U640-3		3914
U640-4		0C36
U640-5		99UA
U640-6		H6F7
U640-9		7442
U640-11		7442
U640-13		7442
U640-14		7442
U640-15		7442

SIGNATURE SET B-11

SET-UP

5223 OPTION 10:
- TEST switch ON.
- Stimulation routine 0 running.
- U710 installed.
- Jumpers G, and H removed; jumpers C, D, and E installed.
- Back Panel Board Cables; P32, P33, and P34 disconnected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: $\overline{WR}$ (U520-9) ↓
START: B ↓
STOP: F ↓

To take these signatures just set all rear-panel switches to 0, remove jumpers D and E, effect RESET, re-install jumpers D and E, then take signatures.

Pin	Name	Signatures
+5V		6055
U830-11	(SD0)	PUAF
U830-12	(SD7)	77CA
U830-13	(SD1)	6514
U830-14	(SD6)	PH5C
U830-15	(SD2)	9820
U830-16	(SD5)	3F87
U830-17	(SD3)	9AH5
U830-18	(SD4)	0AU3

SIGNATURE SET B-12

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 0 running.
U710 installed.
Jumpers G, and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A
START: B
STOP: F

To take these signatures just set all rear-panel switches to 0, remove jumpers D and E, effect RESET, re-install jumpers D and E, then take signatures.

Pin	Signatures
+5V	7442
U640-7	C702

SIGNATURE SET B-13

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 0 running.
U710 installed.
Jumpers G, and H removed; jumpers C, D, and E installed.
Back Panel Board Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A
START: B
STOP: F

To take these signatures just set all rear-panel switches to 0, remove jumpers D and E, effect RESET, re-install jumpers D and E, then take signatures.

Pin	Signatures
+5V	7442
U640-1	H168
U640-2	3152
U640-3	3914
U640-4	0C36
U640-5	99UA
U640-6	H6F7
U640-7	C702

SIGNATURE SET B-14

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 0 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Board Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A
START: B
STOP: F

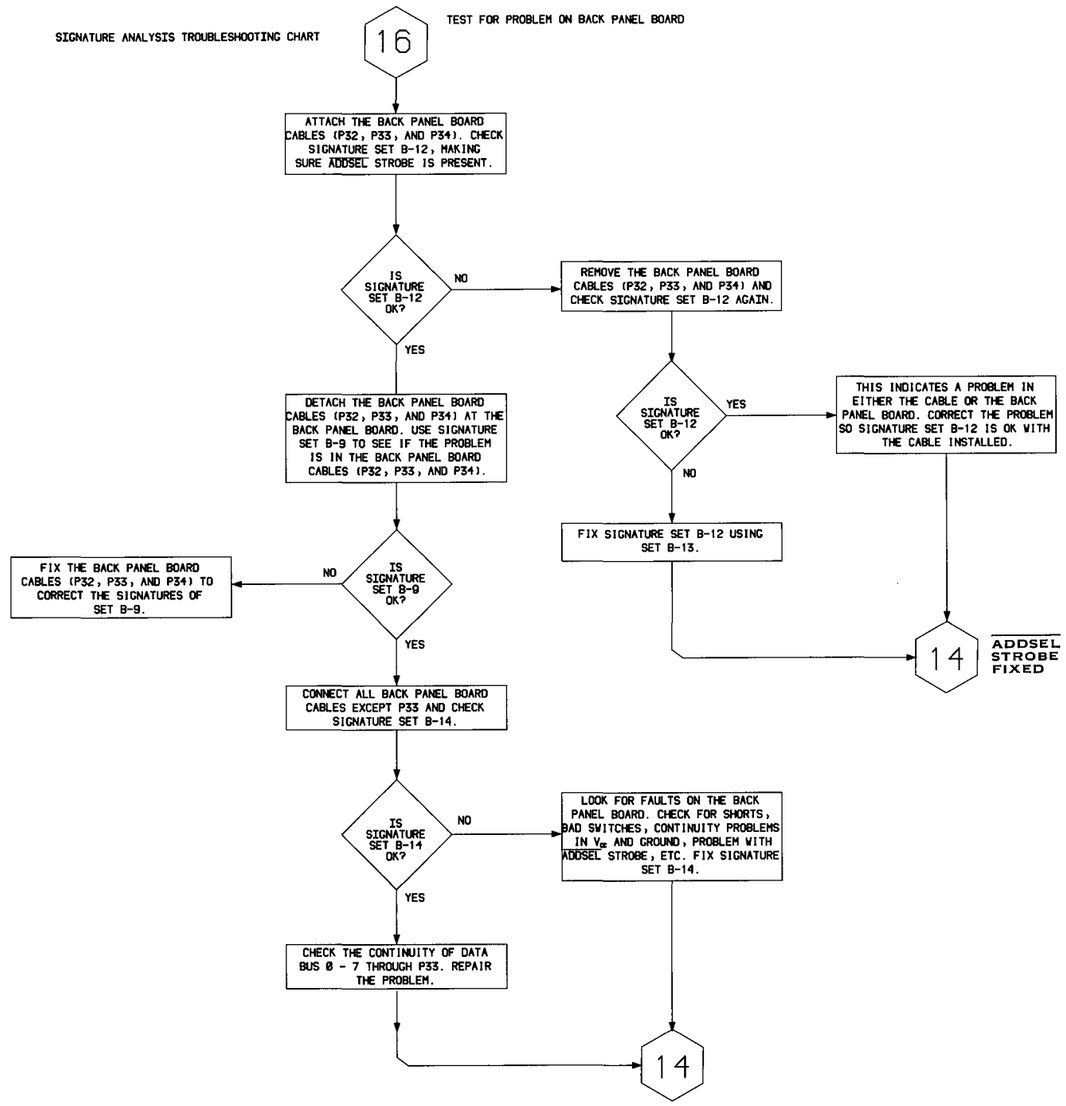
To take these signatures just set all rear-panel switches to 0, remove jumpers D and E, effect RESET, re-install jumpers D and E, then take signatures.

Verify U110 switch operation to inputs (high/low = open/closed)

+5V sig = 7442

Take signatures on U110 or P32, P33 & P34 connector on GPIB Driver Board.

Pin	Rear-panel GPIB Select Swithces Set For: 0	1	Cable connection
U110-1	C702	C702	P34-3
U110-3	957U	563U	P33-1
U110-5	31CP	U2UP	P33-2
U110-7	F371	0031	P33-3
U110-9	7936	CA76	P33-4
U110-10	(GND)	(0V)	P32-8
U110-11	97HC	549C	P33-8
U110-13	P4P7	27A7	P33-7
U110-15	3549	U609	P33-6
U110-17	5723	9463	P33-5
U110-19	C702	C702	P34-3
U110-20	(VCC)	(+5V)	P32-7



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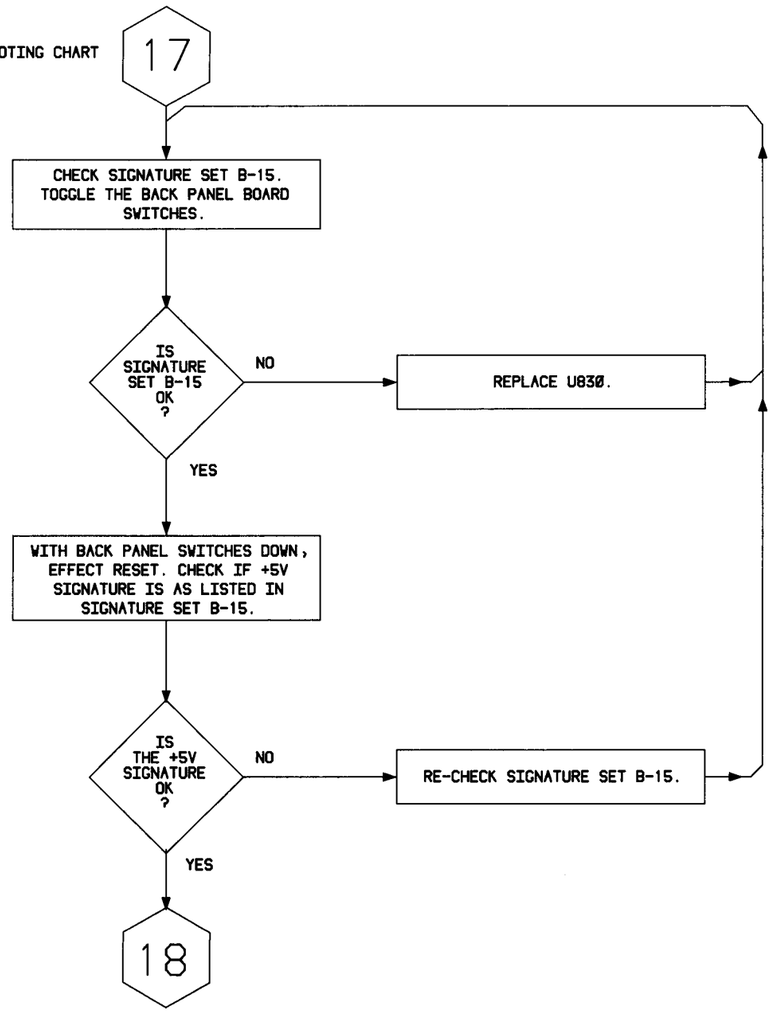
SIGNATURE ANALYSIS TROUBLESHOOTING CHART



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SIGNATURE SET B-15

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 0 running.
U710 installed.
Jumpers G, and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A
START: B
STOP: F

To take these signatures first set all rear-panel switches to 0, remove jumpers D and E, effect RESET, re-install jumpers D and E, then take signatures.

+5V sig = 7442

Pin	Name	Rear-panel Select Switches Set: 0	1	Name
U700-7	(DB4)	04P6	F7A6	GPIB 16
U700-8	(DB3)	3HF7	UP87	GPIB 8
U700-9	(DB5)	4682	85F2	TEST SEL
U700-10	(DB6)	4H4U	8P0U	TALK ONLY
U700-12	(DB2)	7641	C501	GPIB 4
U700-13	(DB7)	4HA4	8PP4	GPIB ON/OFF
U700-14	(DB0)	83P1	40A1	GPIB 1
U700-15	(DB1)	C680	75F0	GPIB 2

SIGNATURE SET C-1

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 4 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		FH1C
U830-11	(SD0)	AH90
U830-12	(SD7)	548F
U830-13	(SD1)	69C3
U830-14	(SD6)	A59F
U830-15	(SD2)	UUHC
U830-16	(SD5)	U2U1
U830-17	(SD3)	H6HP
U830-18	(SD4)	P945

SIGNATURE SET C-2

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 4 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		FH1C
U320-15	(IN6)	FH1C
U420-15	(IN6)	FH1C
U560-15	(IN0)	2U8C
U570-15	(IN1)	P691
U580-15	(IN1)	P691
U860-15	(IN4)	FH1C
U880-15	(IN2)	65C5
U890-15	(IN2)	65C5
U530-11	($\overline{GPIA}$ $\overline{SEL}$)	FH1C

SIGNATURE SET C-3

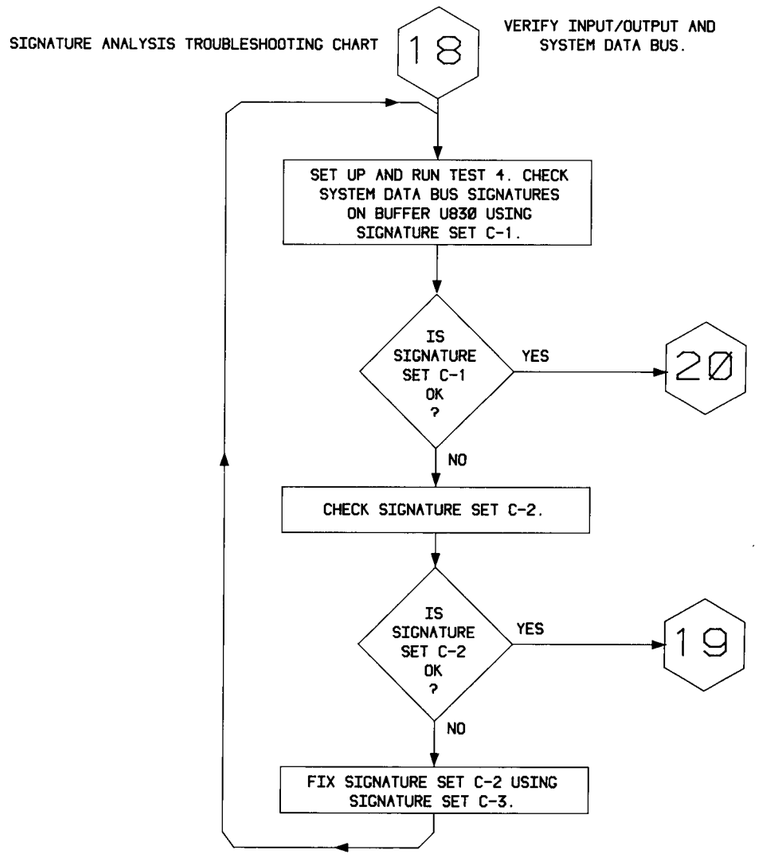
SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 4 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		FH1C
U640-1		8179
U640-2		6A1F
U640-3		UCFP
U640-4		P529
U640-5		P740
U640-6		CHP8
U640-9	(IN6)	FH1C
U640-11	(IN4)	FH1C
U640-13	(IN2)	65C5
U640-14	(IN1)	P691
U640-15	(IN0)	2U8C



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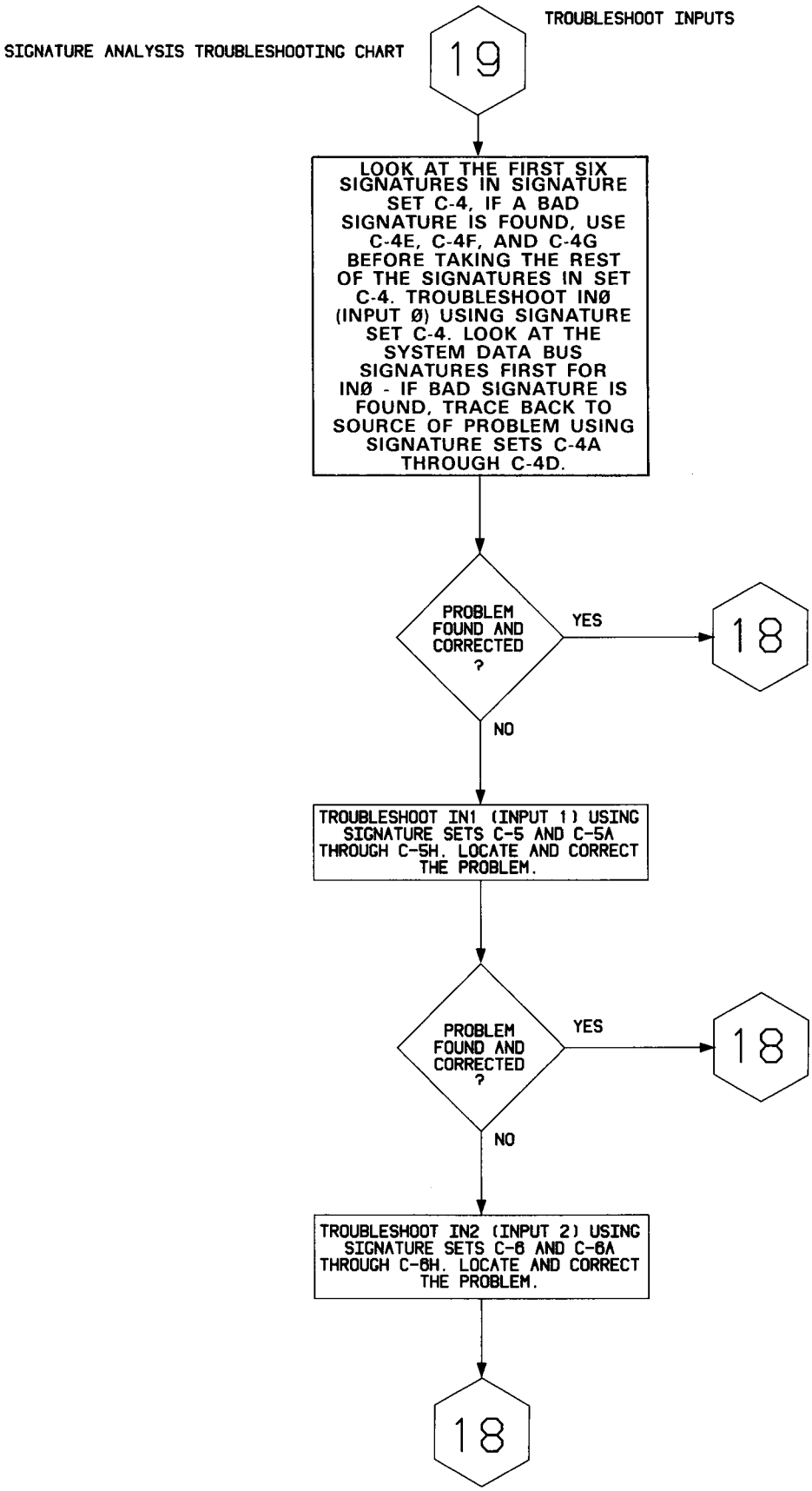
SIGNATURE ANALYSIS TROUBLESHOOTING CHART



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SIGNATURE SET C-4 (IN0)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 5 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
**U850-1	(SSB)	A040
U850-11	(SSA)	3694
U300-1	(SSD)	0000
U300-11	(SSC)	3291
**U840-1	(SSF)	UC8P
U840-11	(SSE)	8127
U560-1	(A0)	9PH6
U560-4	(SD6)	1FF1
U560-7	(SD7)	U6CU
U560-9	(SD4)	H165
U560-12	(SD5)	2HOP
U560-15	(IN0)	AFAU
+5V		FH1C

*Use $\overline{WR}$ for clock.
**This signature must be taken with the pull-up resistor disconnected from the signature analyzer probe.

SIGNATURE SET C-5 (IN1)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 6 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
+5V		FH1C
U570-1	(A0)	9PH6
U570-4	(SD2)	A9A5
U570-7	(SD3)	UC2U
U570-9	(SD1)	U9F0
U570-12	(SD0)	2H22
U570-15	(IN1)	AFAU
U580-1	(A0)	9PH6
U580-4	(SD5)	0A62
U580-7	(SD6)	4970
U580-9	(SD7)	C923
U580-12	(SD4)	9U4F
U580-15	(IN1)	AFAU

SIGNATURE SET C-6 (IN2)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 7 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
U890-1	(A0)	9PH6
U890-4	(SD3)	91A3
U890-7	(SD1)	CP0P
U890-9	(SD2)	P566
U890-12	(SD0)	9653
U890-15	(IN2)	AFAU
U880-1	(A0)	9PH6
U880-4	(SD5)	242C
U880-7	(SD6)	4H39
U880-9	(SD7)	9PU2
U880-12	(SD4)	65CH
U880-15	(IN2)	AFAU

SIGNATURE SET C-4A (IN0-SD4)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 5 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures	Pin	Name	Signatures
U560-10		U654			
U560-11		A08U			
U770-7		U654	U772-12		A08U
U770-5		7U62	U772-13		99UP
U770-6		648U	U772-14		7U62
U770-15		0000	U772-1	($\overline{GPC}$)	1330
U770-1	($\overline{GPC}$)	1330	U772-15		0000
U760-7		7U62	U760-7		7U62
*U760-5	(SD4)	CUC7	U760-9	(OUT 0)	CPF1
U760-9		CPF1	*U760-5	(SD4)	CUC7
U760-1		FH1C	U760-1		FH1C
U730D-8		648U	U960-4		99UP
U730D-9		A994	U960-1	($\overline{GPC}$)	1330
U850-12		A994	U960-15		0000
*U850-13	(SD0)	PH4A	U960-2		F1AF
+5V		FH1C	U960-3		6U2U
*+5V		3274	U850-16		F1AF
			*U850-17	(SD2)	F435
			U300-15		6U2U
			*U300-14	(SD5)	99P4

*Use $\overline{WR}$ for clock.

SIGNATURE SET C-4B (IN0-SD5)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 5 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatues traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U560-13		5912			
U560-14		CF06			
U772-9		CF06	U770-9		5912
U772-11		157F	U770-11		157F
U772-10		52UF	U770-10		5786
U772-15	(EN)	0000			
U772-1	(SEL)	1330	U760-10		157F
			U760-9	(OUT0)	CPF1
U760-10		157F	*U760-12	(SD5)	99P4
*U760-12	(SD5)	99P4			
U760-9	(OUT0)	CPF1	U730-2		5786
U760-1		FH1C	U730-1		9A9H
U870-4		52UF	U840-12		9A9H
U870-3		30A8	*U840-13	(SD0)	PH4A
U870-2		UFFU			
U870-1		1330			
U840-16		UFFU			
*U840-17	(SD2)	F435			
U300-19		30A8			
*U300-18	(SD7)	2415			
+5V		FH1C			
*+5V		3274			

*Use $\overline{WR}$ for clock.

5223 Option 10

SIGNATURE SET C-4C (IN0-SD6)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 5 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signature traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U560-3		9588			
U560-2		FF5U			
U772-7		FF5U	U770-12		9588
U772-5		6P33	U770-13		3322
U772-6		9A74	U770-14		6P33
			U770-1		1330
U760-15		6P33	U760-15		6P33
*U760-13	(SD6)	0163	*U760-13	(SD6)	0163
U760-9	(OUT 0)	CPF1	U760-9	(OUT 0)	CPF1
+5V		FH1C			
*+5V		3274	U550-6		3322
			U550-5		648U
			U550-4		57AH
			U650-6		57AH
			*U650-7	(SD2)	F435
			U650-11	(OUT 3)	48U5
			U730-8		648U
			U730-9		A994
			U850-12		A994
			*U850-13	(SD0)	PH4A

*Use $\overline{WR}$ for clock.

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SIGNATURE SET C-4D (IN0-SD7)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 5 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U560-6		9HC2			
U560-5		4C96			
U772-4		4C96	U770-4		9HC2
U772-3		826H	U770-3		214P
U772-2		9724	U770-2		9724
U760-2		9724	U760-2		9724
*U760-4	(SD7)	2415	*U760-4	(SD7)	2415
U760-9	(OUT0)	CPF1	U760-1		FH1C
			U760-9	(OUT0)	CPF1
U870-12		826H			
U870-13		622U	U660-3		214P
**U870-14		6624	U660-2		F3F2
			U660-1		4556
**U840-19		6624			
*U840-18	(SD3)	5326	U650-12		4556
			*U650-13	(SD4)	CUC7
			U650-1		0000
U300-16		622U	U750-6		F3F2
+U300-17	(SD6)	0163	*U750-7	(SD1)	HAHH
+5V		FH1C	U750-11	(OUT6)	3A63
*+5V		3274			

*Use $\overline{WR}$ for clock.
**This signature must be taken with the pull-up resistor disconnected from the signature analyzer probe.

SIGNATURE SET C-4E

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 5 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
U840-11	(SSE)	8127
**U840-1	(SSF)	UC8P
U740-13	(SSE)	8127
U740-12	(A5)	1271
U740-11	(OUT4)	7AA8
U740-1	(SSF)	UC8P
U740-2		2171
U740-3		8127
U750-12		2171
*U750-13	(SD7)	2415
U750-11	(OUT6)	3A63
U750-1	(GND)	0000
+5V		FH1C
*+5V		3274

*Use $\overline{WR}$ for clock.
**This signature must be taken with the pull-up resistor disconnected from the signature analyzer probe.

SIGNATURE SET C-4F

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 5 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
U850-11	(SSA)	3694
**U850-1	(SSB)	FH1C
U740-8	(OUT4)	7AA8
U740-9	(A4)	H477
U740-10	(SSA)	3694
U740-4	(SSB)	A040
U740-5		2U70
U740-6		3694
U750-1	(GND)	0000
U750-11	(OUT6)	3A63
*U750-14	(SD6)	0163
U750-15		2U70
+5V		FH1C
*+5V		3274

*Use $\overline{WR}$ for clock.
**This signature must be taken with the pull-up resistor disconnected from the signature analyzer probe.

SIGNATURE SET C-4G

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 5 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

Pin	Name	Signatures
U300-1	(SSD)	0000
U300-11	(SSC)	3291
U530-1	(WRITE PROTECT)	8686
U530-2	(OUT5)	C62F
U530-3	(SSC)	3291
U410-1	(RESET)	FH1C
U410-2		FH1C
U410-3	(SSD)	0000
U410-4	(SSD)	0000
U410-5	(OUT5)	C62F
U410-6		FH1C
U650-1	(GND)	0000
U650-8		672H
U650-9	(WRITE PROTECT)	8686
U650-11	(OUT3)	48U5
+5V		FH1C
*+5V		3274

*Use $\overline{WR}$ for clock.

5223 Option 10

SIGNATURE SET C-5A (IN1-SD0)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 6 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9)
START: B
STOP: F

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U570-13		9U41			
U570-14		PU8P			
U780-12		PU8P	U680-12		9U41
U780-13		4144	U680-13		F879
U780-14		H154	U680-14		H154
U762-12		H154	U680-1	($\overline{GPC}$)	1330
U762-11	(OUT1)	UA26	U762-12		H154
*U762-13	(SD0)	PH4A	*U762-13	(SD0)	PH4A
U960-12		4144	U670-11		F879
U960-13		622U	U670-12		5187
**U960-14		P180	U670-13		99UP
**U850-19		P180	U650-5		5187
*U850-18	(SD3)	5326	*U650-4	(SD1)	HAHH
			U650-11		48U5
			U650-1		0000
U300-16		622U	U960-4		99UP
+5V		FH1C	U960-1	($\overline{GPC}$)	1330
*+5V		3274	U960-2		F1AF
			U960-3		6U2U
			U300-15		6U2U
			*U300-14	(SD5)	99P4
			U850-16		F1AF
			*U850-13	(SD0)	PH4A

*Use $\overline{WR}$ for clock.
**This signature must be taken with the pull-up resistor disconnected from the Signature Analyzer probe.

SIGNATURE SET C-5B (IN1-SD1)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 6 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9)
START: B
STOP: F

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U570-9	(SD1)	U9F0			
U570-10		7A88			
U570-11		2A07			
U780-9		2A07	U680-9		7A88
U780-10		3232	U680-10		2F80
U780-11		4A3F	U680-11		4A3F
U762-15		4A3F	U762-15		4A3F
*U762-14	(SD1)	HAHH	*U762-14	(SD1)	HAHH
U762-11	(OUT7)	UA26			
U870-9		3232	U670-8		2F80
U870-10		057A	U670-9		52UF
U870-11		C51C	U670-10		7P7F
U300-12		057A	U650-15		7P7F
*U300-13	(SD4)	CUC7	*U650-14	(SD5)	99P4
			U650-11	(OUT3)	48U5
U920-6		C51C	U870-4		52UF
U920-5		7800	U870-3		30A8
U650-2		7800	U870-2		UFFU
*U650-3	(SD0)	PH4A	U870-1	($\overline{GPC}$)	1330
U650-1		0000	U840-16		UFFU
U650-11	(OUT3)	48U5	*U840-17	(SD2)	F435
+5V		FH1C	U300-19		30A8
*+5V		3274	*U300-18	(SD7)	2415

*Use $\overline{WR}$ for clock.

SIGNATURE SET C-5C (IN1-SD2)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 7 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U570-3		0FC2			
U570-2		P220			
U780-4		P220	U680-4		0FC2
U780-3		A93P	U680-3		3P2U
U780-2		9H55	U680-2		9H55
U762-16		9H55	U762-16		9H55
*U762-17	(SD2)	F435	*U762-17	(SD2)	F435
U762-11	(OUT1)	UA26	U762-11	(OUT1)	UA26
U960-9		A93P	U750-16		3P2U
U960-10		2565	*U750-17	(SD5)	99P4
U960-11		C51C	U750-11	(OUT6)	3A63
U300-2		2565			
*U300-3	(SD3)	5326			
U920-6		C51C			
U920-5		7800			
U650-2		7800			
*U650-3	(SD0)	PH4A			
U650-11	(OUT3)	48U5			
+5V		FH1C			
*+5V		3274			

*Use $\overline{WR}$ for clock.

SIGNATURE SET C-5D (IN1-SD3)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 6 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33 and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U570-6		5H9P			
U570-5		8301			
U780-7		8301	U680-7		5H9P
U780-6		4485	U680-6		AC0C
U780-5		43HF	U680-5		43HF
U762-19		43HF	U762-19		43HF
*U762-18	(SD3)	5326	*U762-18	(SD3)	5326
U762-11	(OUT1)	UA26	U762-11	(OUT1)	UA26
U960-7		4485	U750-19		AC0C
U960-6		4P0F	*U750-18	(SD4)	CUC7
U960-5		7800	U750-11	(OUT6)	3A63
U960-1	(GPC)	1330			
U650-2		7800			
*U650-3	(SD0)	PH4A			
U650-11	(OUT3)	48U5			
U550-11		4P0F			
U550-12		165P			
U550-13		5852			
U650-16		165P			
*U650-17	(SD6)	0163			
U650-11	(OUT3)	48U5			
U730-10		5852			
U730-11		9549			
U840-15		9549			
*U840-14	(SD1)	HAHH			
+5V		FH1C			
*+5V		3274			

*Use $\overline{WR}$ for clock.

5223 Option 10

SIGNATURE SET C-5E (IN1-SD4)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 6 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U580-14		HH31			
U580-13		160P			
U690-12		160P	U790-12		HH31
U690-13		P2PP	U790-13		F203
U690-14		363F	U790-14		363F
U762-2		363F	U762-2		363F
*U762-3	(SD4)	CUC7	*U762-3	(SD4)	CUC7
U762-11		UA26	U762-11		UA26
550-3		P2PP			
550-1		C543	U970-4		F203
550-2		57AH	**U970-2		PC84
U650-6		57AH	U970-3		4556
*U650-7	(SD2)	F435	**U850-6		PC84
U650-11		48U5	*U850-7	(SD6)	0163
U730-4		C543			
U730-3		7858	U650-12		4556
			*U650-13	(SD4)	CUC7
U850-15		7858	U650-11		48U5
*U850-14	(SD1)	HAHH			
+5V		FH1C			
*+5V		3274			

*Use $\overline{WR}$ for clock.
**This signature must be taken with the pull-up resistor disconnected from the Signature Analyzer probe.

SIGNATURE SET C-5F (IN1-SD5)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 6 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U580-3		4P5P			
U580-2		528A			
U790-4		528A	U690-9		4P5P
U790-3		P80A	U690-10		U3C6
U790-2		A09H	U690-11		A09H
U790-1	($\overline{GPC}$)	1330	U690-1	($\overline{GPC}$)	1330
U762-5		A09H	U762-5		A09H
*U762-4	(SD5)	99P4	*U762-4	(SD5)	99P4
U762-11	(OUT1)	UA26	U762-11	(OUT1)	UA26
U970-7		P80A	U660-8		U3C6
U970-6		648U	U660-9		H6H0
U970-5		H9H2	U660-10		4556
U840-6		H9H2	U750-5		H6H0
*U840-7	(SD6)	0163	*U750-4	(SD2)	F435
			U750-11	(OUT6)	3A63
U730-8		648U	U650-12		4556
U730-9		A994	*U650-13	(SD4)	CUC7
U850-12		A994	U650-11	(OUT3)	48U5
*U850-13	(SD0)	PH4A			
+5V		FH1C			
*+5V		3274			

*Use $\overline{WR}$ for clock.

SIGNATURE SET C-5G (IN1-SD6)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 6 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U580-6		CA66			
U580-5		F7F4			
U790-7		F7F4	U690-4		CA66
U790-6		8UH5	U690-3		F643
U790-5		9729	U690-2		9729
U790-1	($\overline{GPC}$)	1330			
U762-6		9729	U762-6		9729
*U762-7	(SD6)	0163	*U762-7	(SD6)	0163
U762-11	(OUT1)	UA26	U762-11		UA26
U870-7		8UH5	U660-11		F643
U870-6		C543	U660-12		4350
U870-5		7800	U660-13		4556
U650-2		7800	U750-2		4350
*U650-3	(SD0)	PH4A	*U750-3	(SD3)	5326
U650-11	(OUT3)	48U5	U650-12		4556
U730-4		C543	*U650-13	(SD4)	CUC7
U730-3		7858	U650-11	(OUT3)	48U5
U850-15		7858			
*U850-14	(SD1)	HAHH			

*Use $\overline{WR}$ for clock.

SIGNATURE SET C-5H (IN1-SD7)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 6 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signatures	Pin	Name	Signatures
U580-10		9155			
U580-11		81CP			
U670-3		81CP	U670-6		9155
U670-2		4FA5	U670-4		5F4P
U790-9		4FA5	U690-7		5F4P
U790-10		AUF8	U690-6		5852
U790-11		4469	U690-5		4469
U790-15		0000	U730-6		4469
U730-6		4469	U730-5		8972
U730-5		8972	U762-9		8972
U762-9		8972	*U762-8	(SD7)	2415
*U762-8	(SD7)	2415	U730-10		5852
U762-11	(OUT1)	UA26	U730-11		9549
U970-9		AUF8	U840-15		9549
U970-11	(+5V)	FH1C	*U840-14	(SD1)	H4HH
U970-10		41H8			
U970-1	($\overline{GPC}$)	1330			
U550-8		41H8			
U550-9		5786			
U550-10		165P			
U650-16		165P			
*U650-17	(SD6)	0163			
U650-11	(OUT3)	48U5			
U730-2		5786			
U730-1		9A9H			
U840-12		9A9H			
*U840-13	(SD0)	PH4A			

*Use $\overline{WR}$ for clock.

5223 Option 10

SIGNATURE SET C-6A (IN2-SD0)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 7 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signature	Pin	Name	Signature
*U890-13		7F67			
*U890-14		1C7A			
*U200-7		***IC7A	*U200-1		***7F67
U200-6		FH1C			
U200-5		FH1C			
U970-12		9A74	U870-12		826H
U970-13		H064	U870-13		622U
U970-14		H06P	**U870-14		6624
U970-1	($\overline{GPC}$)	1330			
			**U840-19		6624
U930-4		H06P	*U840-18	(SD3)	5326
U930-3		59PF			
U930-2		4CP0			
U840-2		4CP0	U300-16		622U
*U840-3	(SD4)	CUC7	U300-17	(SD6)	0163
U850-2		59PF			
*U850-3	(SD4)	CUC7			
U410-11		H064			
U410-12 & 13		1H7U			
U300-6		1H7U			
*U300-7	(SD1)	HAHH			
+5V		FH1C			
*+5V		3274			

*Use $\overline{WR}$ for clock.
**This signature must be taken with the pull-up resistor disconnected from the Signature Analyzer probe.
***If either of these signatures is bad, it could be caused from U970-12 or from U870-12. Trace both paths and use $\overline{WR}$ as clock.

@

SIGNATURE SET C-6B (IN2-SD1)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 7 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signature	Pin	Name	Signature
U890-6		AUF8			
U890-5		4485			
U960-7		4485	U970-9		AUF8
U960-6		4P0F	U970-10		41H8
U960-5		7800	U970-11		FH1C
U960-15		0000	U970-15		0000
U960-1	($\overline{GPC}$)	1330	U970-1	($\overline{GPC}$)	1330
U650-2		7800	U550-8		41H8
*U650-17	(SD6)	0163	U550-9		5786
			U550-10		165P
			U650-16		165P
U550-11		4P0F	*U650-17	(SD6)	0163
U550-12		165P	U650-11		48U5
U550-13		5852	U650-1		0000
U650-16		165P	U730-2		5786
*U650-17	(SD6)	0163	U730-1		9A9H
U650-11		48U5			
U650-1		0000	U840-12		9A9H
U730-10		5852	*U840-13	(SD0)	PH4A
U730-11		9549			
U840-15		9549			
*U840-14	(SD1)	HAHH			

*Use $\overline{WR}$ for clock.

SIGNATURE SET C-6C (IN2-SD2)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 7 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33 and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signature	Pin	Name	Signature
U890-10		C543			
U890-11		4P0F			
U550-11		4P0F	U730-4		C543
U550-12		165P	U730-3		7858
U550-13		5852	U850-15		7858
U650-16		165P	*U850-14	(SD1)	HAHH
*U650-17	(SD6)	0163			
U650-11	(OUT3)	48U5			
U650-1		0000			
U730-10		5852			
U730-11		9549			
U840-15		9549			
*U840-14	(SD1)	HAHH			
+5V		FH1C			
*+5V		3274			

*Use $\overline{WR}$ for clock.

SIGNATURE SET C-6D (IN2-SD3)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 7 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signature	Pin	Name	Signature
U890-3		4144			
U890-2		F203			
U970-4		F203	U960-12		4144
U970-3		4556	U960-13		622U
**U970-2		PC84	**U960-14		P180
			U960-15		0000
**U850-6		PC84	U960-1	($\overline{GPC}$)	1330
*U850-7	(SD6)	0163			
			**U850-19		P180
U650-12		4556	*U850-18	(SD3)	5326
*U650-13	(SD4)	CUC7			
U650-11	(OUT3)	48U5			
U650-1		0000			
+5V		FH1C	U300-16		622U
*+5V		3274	*U300-17	(SD6)	0163

*Use $\overline{WR}$ for clock.
**This signature must be taken with the pull-up resistors disconnected from the Signature Analyzer probe.

@

5223 Option 10

SIGNATURE SET C-6E (IN2-SD4)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 7 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signature	Pin	Name	Signature
U880-12	(SD4)	65CH			
U880-13		52UF			
U880-14		99UP			
U960-4		99UP	U870-4		52UF
U960-3		6U2U	U870-3		30A8
U960-2		F1AF	U870-2		UFFU
U960-1	($\overline{GPC}$)	1330	U870-1	($\overline{GPC}$)	1330
U960-15		0000	U870-15		0000
U850-16		F1AF	U840-16		UFFU
*U850-17	(SD2)	F435	*U840-17	(SD2)	F435
U300-15		6U2U	U300-19		30A8
*U300-14	(SD5)	99P4	*U300-18	(SD7)	2415
+5V		FH1C			
*+5V		3274			

*Use $\overline{WR}$ for clock.

SIGNATURE SET C-6F (IN2-SD5)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 7 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signature	Pin	Name	Signature
U880-4	(SD5)	242C			
U880-3		A93P			
U880-2		8UH5			
U870-7		8UH5	U960-9		A93P
U870-6		C543	U960-10		2565
U870-5		7800	U960-11		C51C
U650-2		7800	U960-1	($\overline{GPC}$)	1330
*U650-3	(SD0)	PH4A	U960-15		0000
U650-11	(OUT3)	48U5	U920-6		C51C
U730-4		C543	U920-5		7800
U730-3		7858	U650-2		7800
U850-15		7858	*U650-3	(SD0)	PH4A
*U850-14	(SD1)	HAHH	U650-11	(OUT3)	48U5
+5V		FH1C	U300-2		2565
*+5V		3274	*U300-3	(SD3)	5326

*Use $\overline{WR}$ for clock.

SIGNATURE SET C-6G (IN2-SD6)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 7 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signature	Pin	Name	Signature
U880-6		3232			
U880-5		P80A			
U970-7		P80A	U870-9		3232
U970-6		648U	U870-10		057A
**U970-5		225F	U870-11		C51C
U970-15		0000			
U970-1	($\overline{GPC}$)	1330	U920-6		C51C
			U920-5		7800
**U840-6		225F			
*U840-7	(SD6)	0163	U650-2		7800
			*U650-3	(SD0)	PH4A
			U650-11	(OUT3)	48U5
			U650-1		0000
U730-8		648U			
U730-9		A994	U300-12		057A
			*U300-13	(SD4)	CUC7
U850-12		A994			
*U850-13	(SD0)	PH4A			
+5V		FH1C			
*+5V		3274			

*Use $\overline{WR}$ for clock.
**This signature must be taken with the pull-up resistor disconnected from the signature analyzer probe.

SIGNATURE SET C-6H (IN2-SD7)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 7 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

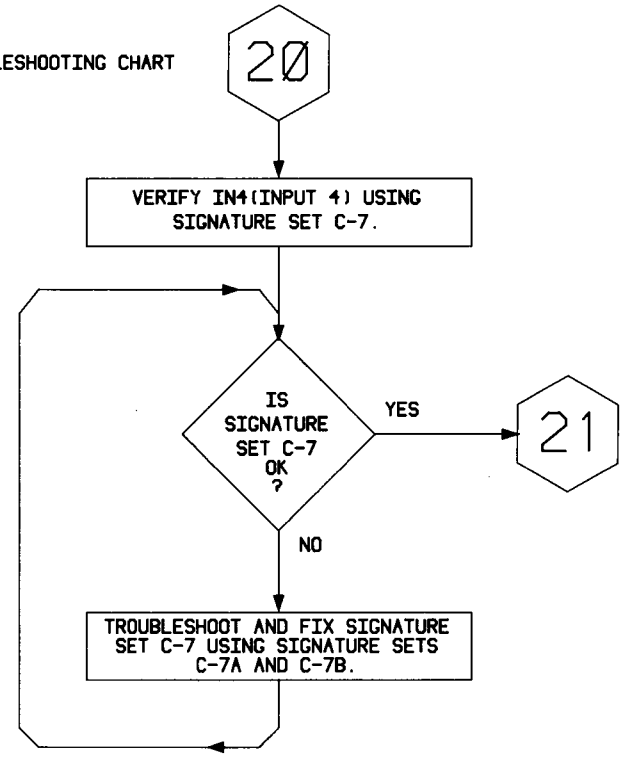
Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signature
U880-10		0000
U880-11		0000
		0000
U950-6		
U950-1		A994
		A994
U920-4		
U920-3		648U
		648U
U730-8		
U730-9		A994
		A994
U850-12		
*U850-13	(SD0)	PH4A
+5V		FH1C
*+5V		3274

*Use $\overline{WR}$ for clock.

SIGNATURE ANALYSIS TROUBLESHOOTING CHART



@

SIGNATURE SET C-7 (IN4)

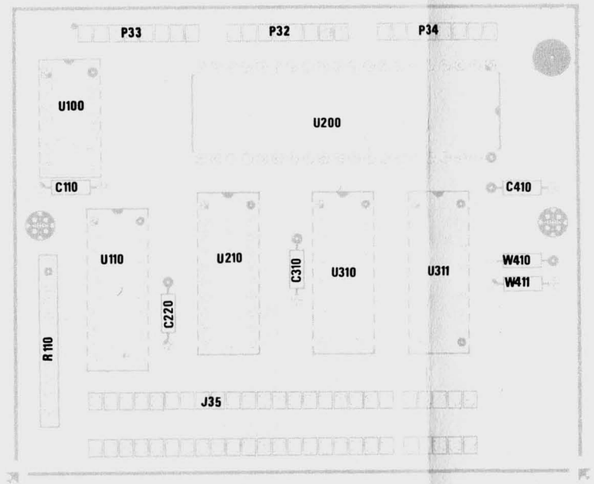
SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 8 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32; P33, and P34 connected.

SIGNATURE ANALYZER:

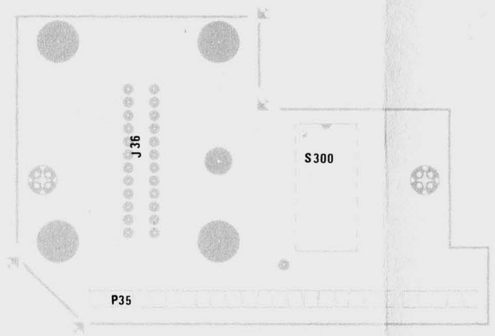
Install pull-up resistor on probe.
CLOCK: A ⊓
START: B ⌐
STOP: F ⊓

Pin	Name	Signatures
U860-1 U860-2	(A0)	9PH6 52UF
U860-3 U860-4	(SD0)	5786 8P58
U860-5 U860-6		8195 8195
U860-7 U860-15 +5V	(SD2) (IN4)	P200 AFAU FH1C



A14

A14-Driver Circuit Board Assembly



A15

A15-Rear Panel Circuit Board Assembly

SIGNATURE SET C-7A (IN4-SD0)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 8 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signature	Pin	Name	Signature
U860-3		5786			
U860-2		52UF			
U870-4		52UF	U730-2		5786
U870-3		30A8	U730-1		9A9H
U870-2		UFFU			
U870-1	($\overline{GPC}$)	1330	U840-12		9A9H
U870-15		0000	*U840-13	(SD0)	PH4A
U840-16		UFFU			
*U840-17	(SD2)	F435			
U300-19		30A8			
*U300-18	(SD7)	2415			
+5V		FH1C			
*+5V		3274			

*Use $\overline{WR}$ for clock.

SIGNATURE SET C-7B (IN4-SD2)

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 8 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A or $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

The arrows on this signature set indicate electrical connections. Working down either column of signatures traces backward to the origins of the top signature in the set.

Pin	Name	Signature
U860-5		8195
U860-6		8195
U400-5		8195
**U400-1		8AU2
U660-6		8AU2
U660-5		007F
U660-4		4556
U650-12		4556
*U650-13	(SD4)	CUC7
U650-11	(OUT3)	48U5
U650-1		0000

*Use $\overline{WR}$ for clock.
**This signature must be taken with the pull-up resistor disconnected from the Signature Analyzer probe.

@

SIGNATURE SET D-1

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 9 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back panel board cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Signatures IN	OUT	Pushbutton
U830-11	H3FC	C119	VECTOR
U830-12	H3FC	C119	DISP L
U830-13	H3FC	C119	ROLL
U830-14	H3FC	C119	SAVE L
U830-15	H3FC	C119	OUTPUT SAVE
U830-16	H3FC	C119	L VS R
U830-17	H3FC	C119	DISP R
U830-18	H3FC	C119	SAVE R
+5V	U399		

SIGNATURE SET D-2

SET-UP

5223 OPTION 10:
TEST switch ON.
Stimulation routine 4 running.
U710 installed.
Jumpers G and H removed, jumpers C, D, and E installed.
Back Panel Board Cables; P32, P33 and P34 connected.

SIGNATURE ANALYZER:

Install pull-up resistor on probe.
CLOCK: $\overline{WR}$ (U520-9) ↓
START: B ↑
STOP: F ↓

Pin	Signatures
U320-4	99P4
U320-7	CUC7
U320-9	0163
U320-12	2415
U420-4	HAHH
U420-7	PH4A
U420-9	F435
U420-12	5326
+5V	3274

SIGNATURE SET D-3

SET-UP

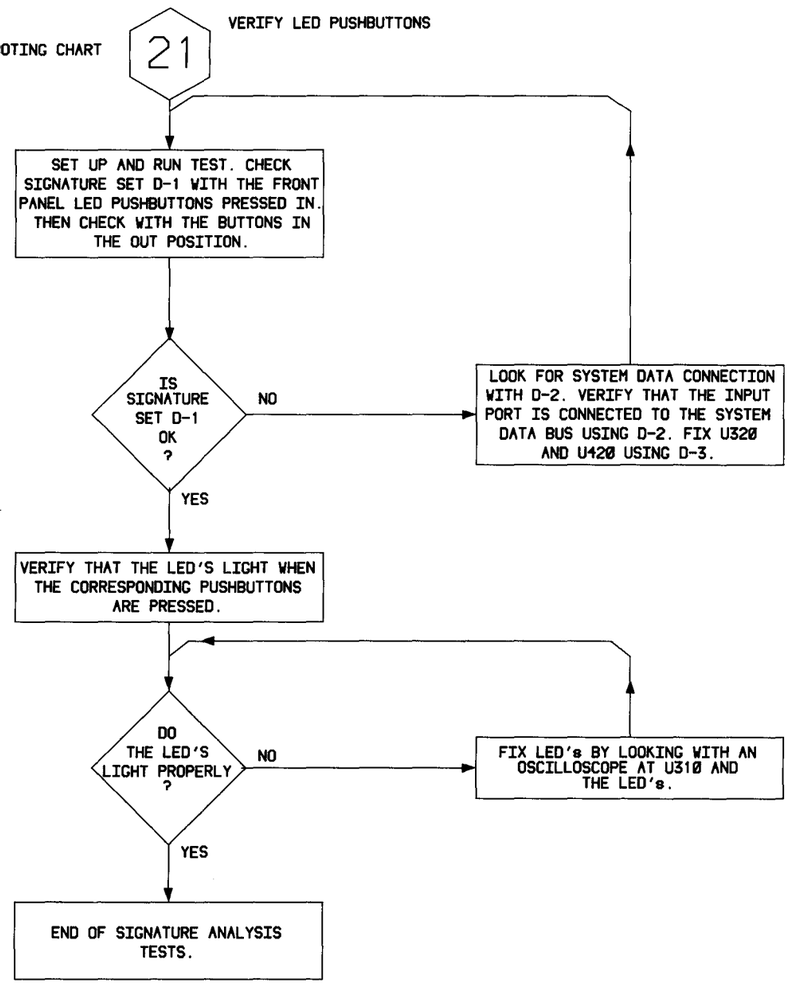
5223 OPTION 10:
TEST switch ON.
Stimulation routine 9 running.
U710 installed.
Jumpers G and H removed; jumpers C, D, and E installed.
Back Panel Cables; P32, P33, and P34 connected.

SIGNATURE ANALYZER:

CLOCK: A ↓
START: B ↑
STOP: F ↓

Pin	Voltages		
U320-8	GND		
U320-16	+5 Volts		
U420-8	GND		
U420-16	+5 Volts		
Pin	**Signatures**		
U320-1	AH69		
U320-15	936P		
U420-1	AH69		
U420-15	936P		
+5V	U399		
	Voltages Measured with Button: OUT	IN	BUTTON
U320-2	0	+5	L VS R
U320-3	+5	0	L VS R
U320-5	0	+5	SAVE R
U320-6	+5	0	SAVE R
U320-10	+5	0	SAVE L
U320-11	0	+5	SAVE L
U320-13	+5	0	DISP L
U320-14	0	+5	DISP L
U420-2	0	+5	ROLL
U420-3	+5	0	ROLL
U420-5	0	+5	VECTOR
U420-6	+5	0	VECTOR
U420-10	+5	0	OUTPUT
U420-11	0	+5	OUTPUT
U420-13	+5	0	DISP R
U420-14	0	+5	DISP R

SIGNATURE ANALYSIS TROUBLESHOOTING CHART



REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000BB	BERQUIST COMPANY	4350 WEST 78TH	MINNEAPOLIS, MN 55435
000BH	FAB-TEK	17 SUGAR HALLOW ROAD	DANBURY, CT 06810
000CY	NORTHWEST FASTENER SALES, INC.	7923 SW CIRRUS DRIVE	BEAVERTON, OREGON 97005
000FW	WESTERN SINTERING CO INC.	2620 STEVENS DRIVE	RICHLAND, WA 99352
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
02107	SPARTA MANUFACTURING COMPANY	ROUTE NO. 2, BOX 128	DOVER, OH 44622
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
05820	WAKEFIELD ENGINEERING, INC.	AUDUBON ROAD	WAKEFIELD, MA 01880
06540	AMATOM ELECTRONIC HARDWARE, DIV. OF MITE CORP.	446 BLAKE ST.	NEW HAVEN, CT 06515
06666	GENERAL DEVICES CO., INC.	525 S. WEBSTER AVE.	INDIANAPOLIS, IN 46219
07707	USM CORP., USM FASTENER DIV.	510 RIVER RD.	SHELTON, CT 06484
11897	PLASTIGLIDE MFG. CORPORATION	P O BOX 867, 1757 STANFORD ST.	SANTA MONICA, CA 90406
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
12360	ALBANY PRODUCTS CO., DIV. OF PNEUMO DYNAMICS CORPORATION	145 WOODWARD AVENUE	SOUTH NORWALK, CT 06586
13103	THERMALLOY COMPANY, INC.	2021 W VALLEY VIEW LANE P O BOX 34829	DALLAS, TX 75234
17217	GORE, W. L. AND ASSOCIATES, INC.	555 PAPER MILL RD.	NEWARK, DE 19711
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
26365	GRIES REPRODUCER CO., DIV. OF COATS AND CLARK, INC.	125 BEECHWOOD AVE.	NEW ROCHELLE, NY 10802
28520	HEYMAN MFG. CO.	147 N. MICHIGAN AVE.	KENILWORTH, NJ 07033
49671	RCA CORPORATION	30 ROCKEFELLER PLAZA	NEW YORK, NY 10020
52961	PRODUCTS SERVICES CO.	86365 COLLEGE VIEW RD.	EUGENE, OR 97405
55285	BERQUIST CO INC.	THE 5300 EDINA INDUSTRIAL BLVD	MINNEAPOLIS, MN 55435
58474	SUPERIOR ELECTRIC CO.	383 MIDDLE ST.	BRISTOL, CT 06010
59730	THOMAS AND BETTS COMPANY	36 BUTLER ST.	ELIZABETH, NJ 07207
71159	BRISTOL SOCKET SCREW, DIV. OF AMERICAN CHAIN AND CABLE CO., INC.	P O BOX 2244, 40 BRISTOL ST.	WATERBURY, CT 06720
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
78471	TILLEY MFG. CO.	900 INDUSTRIAL RD.	SAN CARLOS, CA 94070
79807	WROUGHT WASHER MFG. CO.	2100 S. O BAY ST.	MILWAUKEE, WI 53207
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
85471	BOYD, A. B., CO.	2527 GRANT AVENUE	SAN LEANDRO, CA 94579
86445	PENN FIBRE AND SPECIALTY CO., INC.	2032 E. WESTMORELAND ST.	PHILADELPHIA, PA 19134
86928	SEASTROM MFG. COMPANY, INC.	701 SONORA AVENUE	GLENDALE, CA 91201
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101
95238	CONTINENTAL CONNECTOR CORP.	34-63 56TH ST.	WOODSIDE, NY 11377
95987	WECKESSER CO., INC.	4444 WEST IRVING PARK RD.	CHICAGO, IL 60641
97913	INDUSTRIAL ELECTRONIC HARDWARE CORP.	109 PRINCE STREET	NEW YORK, NY 10012

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	200-2192-01			1		COVER,OPENING:RIGHT,CRT RETAINER	80009	200-2192-01
-2	200-2193-00			1		COVER,OPENING:LEFT,CRT RETAINER	80009	200-2193-00
-3	426-1468-00			1		FRAME,MASK:PLASTIC	80009	426-1468-00
-4	204-0811-00			1		BODY,TERMINAL:OUTER	80009	204-0811-00
-5	204-0812-00			1		BODY,TERMINAL:INNER	80009	204-0812-00
-6	131-2303-01			3		TERMINAL,PIN:1.503 L X 0.025 SQ,BRASS	80009	131-2303-01
-7	378-0876-00			1		FILTER LT,CRT:BLUE	80009	378-0876-00
-8	200-2143-00			1		RTNR,CRT SCALE:ALUMINUM	80009	200-2143-00
						(ATTACHING PARTS)		
-9	213-0808-00			4		SCREW,TPG,TR:8-32 X 0.625 L,TAPTITE,FILM	93907	OBD
						- - - * - - -		
-10	337-2537-00			1		SHLD,IMPLOSION:5.854 X 4.714X 0.09,CLEAR	80009	337-2537-00
-11	366-1327-00			1		KNOB:GRAY	80009	366-1327-00
	213-0153-00			1		. SETSCREW:5-40 X 0.125,STL BK OXD,HEX	000CY	OBD
-12	366-1283-00			1		KNOB:GRAY	80009	366-1283-00
	213-0153-00			1		. SETSCREW:5-40 X 0.125,STL BK OXD,HEX	000CY	OBD
-13	366-1122-00			1		KNOB:GRAY	80009	366-1122-00
	213-0246-00			1		. SETSCREW:5-40 X 0.093 ITL BK OXD,HEX SKT	71159	OBD
-14	366-1120-00			1		KNOB:GRAY,0.600 INCH HIGH	80009	366-1120-00
	213-0153-00			2		. SETSCREW:5-40 X 0.125,STL BK OXD,HEX	000CY	OBD
-15	366-1189-00			1		KNOB:GRAY	80009	366-1189-00
	213-0246-00			1		. SETSCREW:5-40 X 0.093 ITL BK OXD,HEX SKT	71159	OBD
-16	131-0955-01			1		CONN,RCPT,ELEC:BNC,FEMALE,MODIFIED	80009	131-0955-01
-17	210-0255-00			1		TERMINAL,LUG:0.391" ID INT TOOTH	80009	210-0255-00
-18	343-0003-00			1		CLAMP,LOOP:0.25 INCH DIA	95987	1-4 6R
						(ATTACHING PARTS)		
-19	211-0012-00			1		SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	OBD
-20	210-0851-00			1		WASHER,FLAT:0.119 ID X 0.375 INCH OD,STL	12327	OBD
-21	210-0586-00			1		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-22	----- -----			1		CKT BOARD ASSY:FRONT PANEL(SEE A2 REPL)		
						(ATTACHING PARTS)		
-23	210-0583-00			2		NUT,PLAIN,HEX.:0.25-32 X 0.312 INCH,BRS	73743	2X20317-402
-24	210-0940-00			2		WASHER,FLAT:0.25 ID X 0.375 INCH OD,STL	79807	OBD
-25	220-0495-00			1		NUT,PLAIN,HEX.:0.375-32 X 0.438 INCH BRS	73743	OBD
-26	210-0978-00			1		WASHER,FLAT:0.375 ID X 0.50 INCH OD,STL	78471	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-27	131-2533-00			17		. TERMINAL,PIN:0.65 L X 0.025 SQ,BRS GOLD	22526	48087
-28	131-0608-00			18		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-29	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-30	136-0220-00			1		. SKT,PL-IN ELEK:TRANSISTOR 3 CONTACT,PCB MT	71785	133-23-11-034
-31	214-2518-00			1		. HEAT SINK,XSTR:TO-220 OR TO-202	000BH	106B-B-HT
-32	----- -----			1		CKT BOARD ASSY:GRATICULE ILLUM(SEE A1 REPL)		
-33	378-0116-00			1		. REFLECTOR,LIGHT:INTERNAL SCALE ILLUM	80009	378-0116-00
-34	343-0768-00			1		RETAINER,SPRING:LIGHT REFLECTOR	80009	343-0768-00
-35	343-0751-00			4		CLAMP,CRT:6.0 INCH CRT	80009	343-0751-00
						(ATTACHING PARTS)		
-36	211-0669-00			4		SCREW,MACHINE:6-32 X 0.75,FLH,90 DEG,SST	93907	OBD
						- - - * - - -		
-37	348-0276-01			1		SHLD,GSKT,ELEK:MESH TYPE,0.124 OD,7.442 L	80009	348-0276-01
-38	348-0276-02			2		SHLD,GSKT,ELEK:MESH TYPE,0.124 OD,4.22 L	80009	348-0276-02
-39	426-1517-03			1		FRAME,CABINET:FRONT	80009	426-1517-03
						(ATTACHING PARTS)		
-40	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE,FILH		
						- - - * - - -		
-41	----- -----			1		COIL,TUBE DEFL:(SEE L51 REPL)		
-42	334-1379-00			1		LABEL:CRT,ADHESIVE BACK	80009	334-1379-00
-43	214-0291-00			1		CONTACT,SPRING:1.188 X 0.375 X 0.25 INCH	80009	214-0291-00
						(ATTACHING PARTS)		
-44	211-0168-00			1		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	12360	OBD
-45	210-0586-00			1		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-46	348-0067-00			1		GROMMET,PLASTIC:0.312 INCH DIA	80009	348-0067-00
-47	348-0532-00			1		GROMMET,PLASTIC:BLACK,ROUND,0.625 ID	28520	SB-750-10

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-48	337-2613-01			1		SHIELD,CRT:PAINTED	80009	337-2613-01
-49	----- -----			1		CKT BOARD ASSY:XYZ AMP(SEE A3 REPL)		
						(ATTACHING PARTS)		
-50	211-0008-00			7		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
-51	210-0851-00			2		WASHER,FLAT:0.119 ID X 0.375 INCH OD,STL	12327	OBD
-52	214-1042-00			2		SPRING,HLCPS:0.282 OD X 0.37 L,CLOSED	80009	214-1042-00
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-53	214-0579-00			2		. TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-54	136-0252-07			48		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-55	131-0827-00			9		. CONTACT,ELEC:0.55 INCH LONG	22526	47349
-56	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-57	131-0589-00			47		. TERM,PIN:0.46 L X 0.025 SQ.PH BRZ GL	22526	47350
-58	131-0608-00			35		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-59	129-0317-00			1		. POST,ELEC-MECH:4-40 X 0.187 X 0.125 INCH L	80009	129-0317-00
-60	136-0260-02			2		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-61	136-0269-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,LOW CLE	73803	CS9002-14
-62	343-0144-00			1		CLAMP,LOOP:0.125 INCH ID,BLK NYLON	95987	1-8-2
						(ATTACHING PARTS)		
-63	211-0008-00			1		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
-64	210-0994-00			1		WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5702-201-20
						- - - * - - -		
-65	255-0334-00			1		PLASTIC CHANNEL:12.75 X 0.175X 0.155,NYL	11897	122-37-2500
-66	342-0516-00			1		INSULATOR,PLATE:HEAT SINK,SILICON RUBBER	55285	OBD
-67	210-0202-00			1		TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
						(ATTACHING PARTS)		
-68	211-0504-00			1		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-69	441-1472-00			1		CHASSIS SCOPE:CIRCUIT BOARD	80009	441-1472-00
						(ATTACHING PARTS)		
-70	211-0603-00			4		SCREW,MACHINE:6-32 X 0.312 INCH,HEX HD STL	83385	OBD
						- - - * - - -		
	672-0852-00			1		CKT BOARD ASSY:HIGH VOLTAGE	80009	**672-0852-00**
						(ATTACHING PARTS)		
-71	213-0789-00			4		SCREW,TPG,TF:6-32 X 0.375,TAPTITE,PNH	93907	OBD
-72	211-0008-00			2		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
-73	211-0040-00			2		SCREW,MACHINE:4-40 X 0.25",BDGH PLSTC	26365	OBD
-74	210-0004-00			1		WASHER,LOCK:#4 INTL,0.015THK,STL CD PL	78189	1204-00-00-0541C
						- - - * - - -		
-75	136-0280-00			2		SOCKET,PLUG-IN:FOR TO-3	97913	LST 2202-2
						(ATTACHING PARTS)		
-76	211-0038-00			2		SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG	83385	OBD
-77	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-78	----- -----			2		TRANSISTOR:(SEE Q60 AND Q62 REPL)		
						(ATTACHING PARTS)		
-79	213-0146-00			4		SCR,TPG,THD FOR:6-20 X 0.313 INCH,PNH STL	83385	OBD
						- - - * - - -		
-80	386-0978-00			2		INSULATOR,PLATE:TRANSISTOR,MICA	80009	386-0978-00
-81	441-1473-00			1		CHASSIS SCOPE:CIRCUIT BOARD	80009	441-1473-00
-82	----- -----			1		CKT BOARD ASSY:HIGH VOLTAGE(SEE A4 REPL)		
						(ATTACHING PARTS)		
-83	211-0008-00			4		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-84	214-0579-00			1		. TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-85	131-0608-00			11		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-86	131-0589-00			7		. TERM,PIN:0.46 L X 0.025 SQ.PH BRZ GL	22526	47350
-87	----- -----			1		. SEMICOND DEVICE:(SEE A4CR220 REPL)		
-88	334-2363-00			1		. MARKER INDENT:WARNING,DANGER,HV	80009	334-2363-00
-89	129-0098-00			2		. POST,ELEC-MECH:0.250 HEX.X0.406 INCH L,BRS	80009	129-0098-00
-90	129-0143-00			2		. INSULATOR,STDF:0.312 OD X 0.406" L,NYLON	80009	129-0143-00
						(ATTACHING PARTS)		
-91	213-0789-00			2		. SCREW,TPG,TF:6-32 X 0.375,TAPTITE,PNH	93907	OBD
						- - - * - - -		

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-92	129-0236-00			1		. SPACER,POST:0.188 HEX X 0.375 INCH LONG	06540	9726-A-0440
-93	----- -----			1		. CKT BOARD ASSY:FOCUS(SEE A5 REPL)		
-94	131-1261-00			4		. CONTACT,ELEC:F-SHAPED	00779	1-380953-0
-95	----- -----			1		. CKT BOARD ASSY:Z AXIS(SEE A6 REPL)		
	131-1261-00			4		. CONTACT,ELEC:F-SHAPED	00779	1-380953-0
-96	343-0006-00			2		CLAMP,LOOP:0.50 INCH DIAMETER,PLSTC	95987	1-2-6B
						(ATTACHING PARTS)		
-97	211-0510-00			2		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
-98	210-0863-00			2		WSHR,LOOP CLAMP:FOR 0.50" WIDE CLAMP,STL	95987	C191
						- - - * - - -		
-99	----- -----			1		DELAY LINE:(SEE DL90 REPL)		
						(ATTACHING PARTS)		
-100	211-0510-00			3		SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
-101	210-0802-00			3		WASHER,FLAT:0.15 ID X 0.312 INCH OD	12327	OBD
						- - - * - - -		
-102	255-0334-00			2		PLASTIC CHANNEL:12.75 X 0.175X 0.155,NYL	11897	122-37-2500
-103	407-2159-00			4		BRACKET,CMPNT:LOWER EXTENSION,ALUMINUM	80009	407-2159-00
-104	441-1474-00			1		CHASSIS,SCOPE:CIRCUIT BOARD	80009	441-1474-00
-105	366-0497-00			1		KNOB:GY,0.127 ID X0.706 OD	80009	366-0497-00
-106	----- -----			1		RESISTOR,VAR:(SEE R47 REPL)		
						(ATTACHING PARTS)		
-107	210-0583-00			1		NUT,PLAIN,HEX.:0.25-32 X 0.312 INCH,BRS	73743	2X20317-402
-108	210-0940-00			1		WASHER,FLAT:0.25 ID X 0.375 INCH OD,STL	79807	OBD
						- - - * - - -		
-109	131-0955-01			2		CONN,RCPT,ELEC:BNC,FEMALE,MODIFIED	80009	131-0955-01
-110	210-0255-00			1		TERMINAL,LUG:0.391" ID INT TOOTH	80009	210-0255-00
-111	129-0064-00			2		POST,BDG,ELEC:CHARCOAL,5-WAY MINIATURE	58474	BINP BB10167G13T
						(ATTACHING PARTS)		
-112	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
-113	358-0181-00			2		INSULATOR,BSHG:CHARCOAL	58474	BB10166G13BX
						- - - * - - -		
-114	----- -----			1		FAN,TUBEAXIAL:(SEE B25 REPL)		
						(ATTACHING PARTS)		
-115	211-0511-00			4		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
-116	210-0457-00			4		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-117	378-0780-00			1		GRILLE,FAN:3.182 X 3.182 INCH	80009	378-0780-00
-118	386-4438-00			1		PLATE,COVER:ALUMINUM	80009	386-4438-00
						(ATTACHING PARTS)		
-119	211-0097-00			3		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-120	333-2662-00			1		PANEL,REAR:	80009	333-2662-00
						(ATTACHING PARTS)		
-121	213-0820-00			4		SCREW,TPG,TF:8-32 X 0.5,TAPTITE,PNH,STL	93907	OBD
						- - - * - - -		
-122	426-1449-05			1		FRAME,CABINET:REAR,AL	80009	426-1449-05
						(ATTACHING PARTS)		
-123	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE	80009	213-0863-00
						- - - * - - -		
-124	426-1570-00			4		FRAME SECT,CAB.:	80009	426-1570-00
	198-3744-00			1		WIRE SET,ELEC:	80009	198-3744-00
	175-0931-00			1		. WIRE ELECTRICAL:STRD,24 AWG,9KV	17217	OBD

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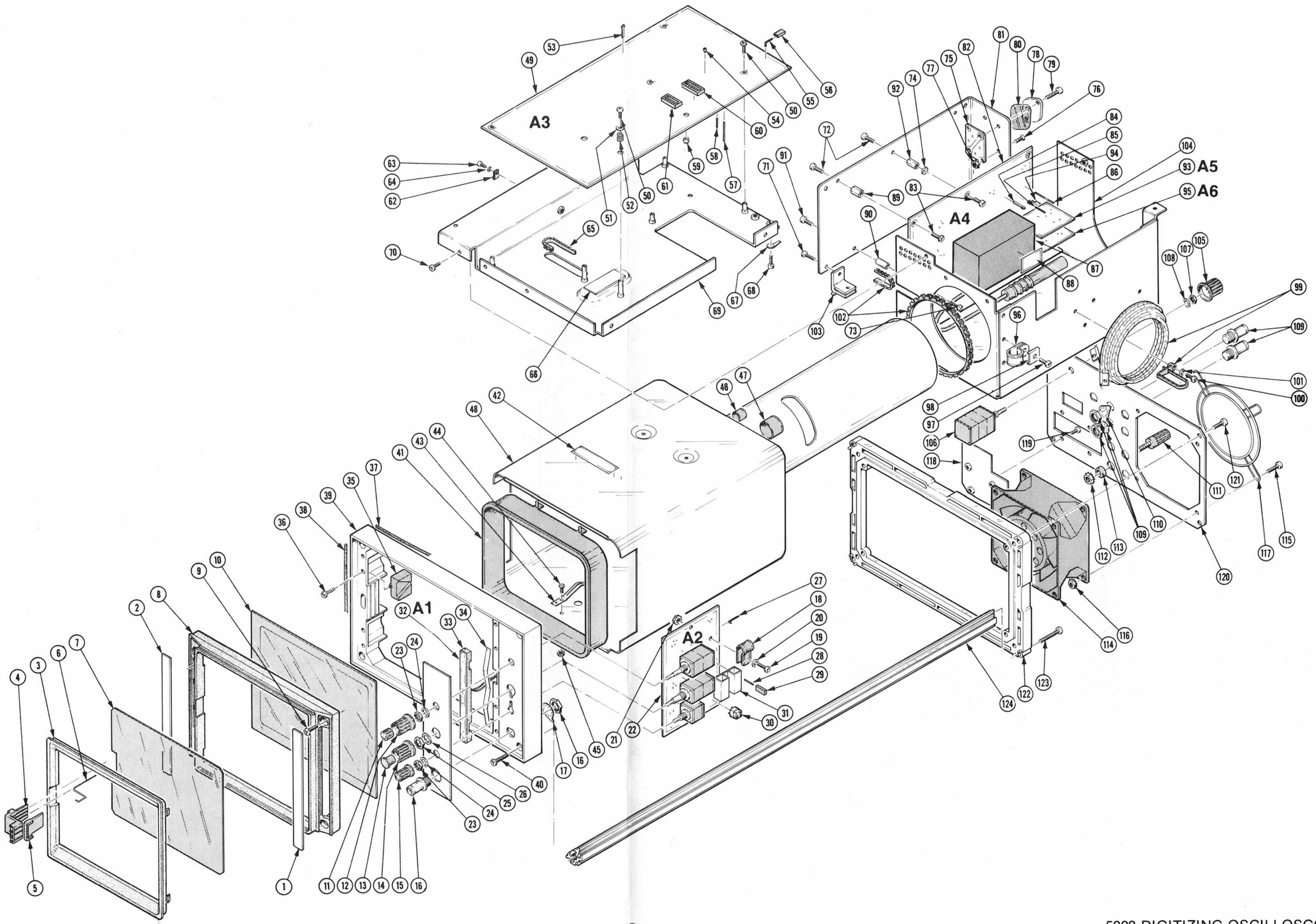
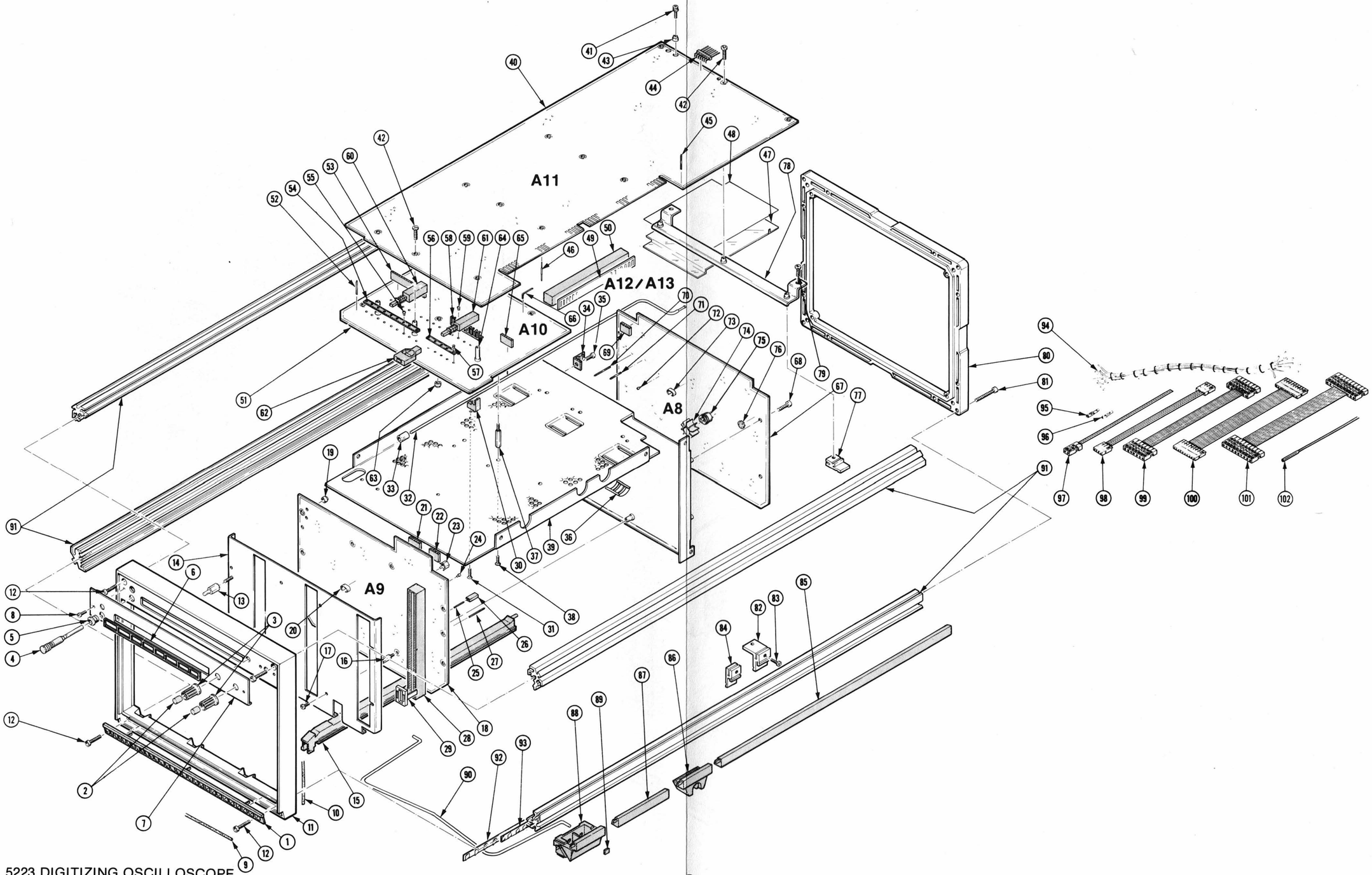


Fig. 1. DISPLAY

Fig. 2. MAINFRAME



5223 DIGITIZING OSCILLOSCOPE

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-1	378-0130-00			1		GRILLE,PLASTIC:8.164 X 0.462,SILVER GRAY	80009	378-0130-00
-2	366-1319-03			2		KNOB:GY,W/IDX,0.79 ID,0.28 OD,0.32 H	80009	366-1319-03
-3	366-1077-00			2		KNOB:GRAY	80009	366-1077-00
	213-0246-00			2		. SETSCREW:5-40 X 0.093 ITL BK OXD,HEX SKT	71159	OBD
-4	366-1789-00			1		KNOB:GRAY,0.3 DIA,W/12.58 L X 0.125 DIA	80009	366-1789-00
-5	358-0216-00			1		BUSHING,PLASTIC:0.257 ID X 0.412 INCH OD	80009	358-0216-00
-6	426-1628-00			2		FRAME,PB:PLASTIC,SILVER GRAY	80009	426-1628-00
-7	333-2528-00			1		PANEL,FRONT:	80009	333-2528-00
						(ATTACHING PARTS)		
-8	213-0055-00			2		SCR,TPG,THD FOR:2-32 X 0.188 INCH,PNH STL	93907	OBD
						- - - * - - -		
-9	348-0276-01			1		SHLD GSKT,ELEK:MESH TYPE,0.124 OD,7.442 L	80009	348-0276-01
-10	348-0276-03			2		SHLD GSKT,ELEK:MESH TYPE,0.124 OD,5.97 L	80009	348-0276-03
-11	426-1586-01			1		FRAME PNL,CAB.:	80009	426-1586-01
						(ATTACHING PARTS)		
-12	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE	80009	213-0863-00
						- - - * - - -		
-13	129-0797-00			1		POST,LOCKOUT:0.7 L X 6-32 THD ONE END,AL	80009	129-0797-00
-14	337-2614-00			1		SHIELD,ELEC:CIRCUIT BOARD	80009	337-2614-00
-15	351-0566-00			3		GUIDE,PL-IN UNI:BOTTOM	80009	351-0566-00
-16	129-0236-00			8		SPACER,POST:0.188 HEX X 0.375 INCH LONG	06540	9726-A-0440
						(ATTACHING PARTS)		
-17	211-0008-00			8		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-18	----- -----			1		CKT BOARD ASSY:INTERFACE(SEE A9 REPL)		
-19	129-0317-00			1		. POST,ELEC-MECH:4-40 X 0.187 X 0.125 INCH L	80009	129-0317-00
-20	214-0973-00			2		. HEAT SINK,ELEC:0.28 X 0.18 OVAL X 0.187"H	80009	214-0973-00
-21	131-1771-00			1		. CONNECTOR,RCPT,:CIRCUIT CARD,6 FEMALE	22526	65001-111
-22	131-2002-00			2		. CONN,RCPT,ELEC:CKT BD,5 CONTACT FEMALE	22526	65001-110
-23	131-1003-00			3		. CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
-24	136-0252-07			3		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-25	131-0608-00			23		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-26	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-27	131-0589-00			18		. TERM,PIN:0.46 L X 0.025 SQ.PH BRZ GL	22526	47350
-28	131-1078-00			3		. CONNECTOR,RCPT,:28/56 CONTACT	95238	600-1156Y256DF30
-29	200-2601-00			3		. COVER,ELEC CONN:W/POLARIZING KEY	80009	200-2601-00
-30	351-0627-00			2		GUIDE,SHAFT:PLASTIC	80009	351-0627-00
						(ATTACHING PARTS)		
-31	211-0038-00			2		SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG	83385	OBD
						- - - * - - -		
-32	384-1554-00			1		SHAFT,SWITCH:11.388 L X 0.125 OD,AL	80009	384-1554-00
-33	376-0029-00			1		CPLG,SHAFT,RGD:0.128 ID X 0.312 OD X 0.5"L	80009	376-0029-00
-34	344-0133-00			2		CLIP,SPR,TNSN:CIRCUIT CARD MOUNTING	80009	344-0133-00
						(ATTACHING PARTS)		
-35	211-0008-00			2		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-36	131-2423-00			3		CONTACT,ELEC:PLUG-IN GND,CU BE BRT DIP	80009	131-2423-00
-37	129-0784-00			6		SPACER,POST:0.687 L,W/4-40 THD EA END	80009	129-0784-00
						(ATTACHING PARTS)		
-38	211-0038-00			6		SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG	83385	OBD
						- - - * - - -		
-39	441-1475-00			1		CHASSIS,SCOPE:CIRCUIT BOARD	80009	441-1475-00
-40	----- -----			1		CKT BOARD ASSY:MEMORY(SEE A11 REPL)		
						(ATTACHING PARTS)		
-41	211-0244-00			3		SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH STL	78189	OBD
-42	211-0008-00			12		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-43	129-0317-00			4		. POST,ELEC-MECH:4-40 X 0.187 X 0.125 INCH L	80009	129-0317-00
-44	131-1426-00			1		. CONTACT SET,ELE:R ANGLE,0.250L,STRIP OF 36	22526	65524-136
-45	131-0608-00			2		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-46	131-2533-00			49		. TERMINAL,PIN:0.65 L X 0.025 SQ BRZ GOLD	22526	48087
-47	337-2777-00			1		. SHIELD,ELEC:CIRCUIT BOARD	80009	337-2777-00
-48	342-0513-00			1		. INSULATOR,PLATE:CIRCUIT BOARD PLASTIC	80009	342-0513-00
-49	----- -----			2		CKT BOARD ASSY:MEMORY SHORTING(SEE A12,A13 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-50	131-1499-00			2		. CONN,RCPT,ELEC:CKT BD 36/72 CONTACT	95238	K600121GE72Y44
-51	----- -----			1		CKT BOARD ASSY:SWITCH(SEE A10 REPL)		
-52	131-0608-00			2		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-53	131-2184-00			1		. CONN,RCPT,ELEC:CKT BD,1 X 17FEM,TOP ENTRY	22526	65780-017
-54	343-0495-05			1		. CLIP,SWITCH:FRONT,7.5MM X5 UNIT	80009	343-0495-05
						(ATTACHING PARTS)		
-55	210-3033-00			10		. EYELET,METALLIC:0.59 OD X 0.156 INCH LONG	07707	SE-25
						- - - * - - -		
-56	343-0495-10			1		. CLIP,SWITCH:FRONT,10 UNITS	80009	343-0495-10
						(ATTACHING PARTS)		
-57	210-3033-00			5		. EYELET,METALLIC:0.59 OD X 0.156 INCH LONG	07707	SE-25
						- - - * - - -		
-58	343-0499-05			1		. CLIP,SWITCH:REAR,7.5MM X 5 UNIT	80009	343-0499-05
						(ATTACHING PARTS)		
-59	210-3033-00			15		. EYELET,METALLIC:0.59 OD X 0.156 INCH LONG	07707	SE-25
						- - - * - - -		
-60	----- -----			7		. SWITCH:(SEE A10S150,250,251,350,351,550,		
	----- -----			-		. 650 REPL)		
-61	----- -----			1		. SWITCH:(SEE A10S450 REPL)		
-62	366-1818-00			8		. PUSH BTN ASSY:W/RED,LED	80009	366-1818-00
-63	129-0656-00			4		. SPACER,POST:0.288 L,W/4-40 THD ONE FND	80009	129-0656-00
-64	129-0561-00			3		. SPACER,POST:0.535 L,W-4-40 INTL ONE END	80009	129-0561-00
-65	131-2471-00			1		. CONN,RCPT,ELEC:CKT BD,6/CONT,FEMALE	22526	65780-006
-66	131-0589-00			13		. TERM,PIN:0.46 L X 0.025 SQ.PH BRZ GL	22526	47350
-67	----- -----			1		CKT BOARD ASSY:DIGITIZER(SEE A8 REPL)		
						(ATTACHING PARTS)		
-68	211-0008-00			2		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-69	131-2002-00			2		. TERMINAL,PIN:0.46 L X 0.025 SQ PH	22526	65001-110
-70	131-0589-00			5		. TERM,PIN:0.46 L X 0.025 SQ.PH BRZ GL	22526	47350
-71	131-0608-00			12		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-72	136-0252-07			16		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-73	214-0973-00			4		. HEAT SINK,ELEC:0.28 X 0.18 OVAL X 0.187"H	80009	214-0973-00
-74	214-1291-00			2		. HEAT SINK,ELEC:XSTR,0.72 OD X 0.375"H	05820	207-AB
-75	136-0241-00			1		. SOCKET,PLUG-IN:10 CONTACT,ROUND	71785	133-99-12-064
-76	342-0324-00			1		. INSULATOR,DISC:TO-5 TRANSISTOR	13103	7717-5N-BLUE
-77	407-2156-00			2		BRACKET,CMPNT:ALUMINUM	80009	407-2156-00
-78	386-4111-00			1		SUPPORT,CKT BOARD:	80009	386-4111-00
						(ATTACHING PARTS)		
-79	213-0789-00			2		SCREW,TPG,TF:6-32 X 0.375,TAPTITE,PNH	93907	OBD
						- - - * - - -		
-80	426-1469-04			1		FRAME,CABINET:REAR,AL	80009	426-1469-04
						(ATTACHING PARTS)		
-81	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE	80009	213-0863-00
						- - - * - - -		
-82	407-2158-00			2		BRACKET,CMPNT:UPPER EXTENSION	80009	407-2158-00
						(ATTACHING PARTS)		
-83	213-0789-00			2		SCREW,TPG,TF:6-32 X 0.375,TAPTITE,PNH	93907	OBD
						- - - * - - -		
-84	407-2156-00			7		BRACKET,CMPNT:ALUMINUM	80009	407-2156-00
-85	124-0376-00			2		STRIP,TRIM:CORNER,BOTTOM,PVC	80009	124-0376-00
-86	343-0829-00			2		RTNR BLK,SCOPE:BLUE PLASTIC	80009	343-0829-00
-87	124-0375-00			2		STRIP,TRIM:CORNER,BOTTOM,PVC	80009	124-0375-00
-88	348-0617-00			4		FOOT,CABINET:	80009	348-0617-00
-89	348-0596-00			4		PAD,CAB.FOOT:0.69 X 0.255 X 0.06,PU	80009	348-0596-00
-90	348-0282-00			1		FLIPSTAND,CAB.:3.438 H,SST	80009	348-0282-00
-91	426-1570-00			4		FRAME SECT,CAB.:	80009	426-1570-00
-92	348-0632-00			3		SHLD GSKT,ELEK:FINGER TYPE 19.0 L	52961	OBD
-93	348-0633-00			3		SHLD GSKT,ELEK:FINGER TYPE,19.0 L	52961	OBD
-94	179-2738-00			1		WIRING HARNESS:MAIN	80009	179-2738-00
	179-2740-00			1		WIRING HARNESS:RACKMOUNT	80009	179-2740-00
	179-2753-00			1		WIRING HARNESS:HV X,Y,Z INTERCONNECT	80009	179-2753-00
-95	131-0621-00			26		CONNECTOR,TERM:22-26 AWG,BRS& CU BE GOLD	22526	46231
-96	131-0707-00			56		CONNECTOR,TERM.:22-26 AWG,BRS& CU BE GOLD	22526	47439
-97	175-3158-00			1		CA ASSY,SP,ELEC:2,26 AWG,6.0 L,RIBBON	80009	175-3158-00

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-98	175-2585-00			1		CA ASSY,SP,ELEC:4,22 AWG,8.0 L,RIBBON	80009	175-2585-00
-99	175-3571-00			1		CA ASSY,SP,ELEC:7,26 AWG,14.0 L,RIBBON	80009	175-3571-00
-100	175-2586-00			1		CA ASSY,SP,ELEC:9,22 AWG,6.0 L	80009	175-2586-00
-101	175-2627-00			1		CA ASSY,SP,ELEC:10,26 AWG,14.0 L	80009	175-2627-00
	175-3774-00			1		CA ASSY,SP,ELEC:10,26 AWG,14.0 L	80009	175-3774-00
-102	195-1368-00			1		LEAD,ELECTRICAL:26 AWG,4.0 L,9-4	80009	195-1368-00

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-	620-0293-00			1		POWER SUPPLY:	80009	620-0293-00
						(ATTACHING PARTS)		
-1	213-0801-00			4		SCREW,TPG,TF:8-32 X 0.312,TAPTITE,PNH	93907	OBD
-2	211-0507-00			2		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-3	----- -----			1		. TRANSFORMER:(SEE T25 REPL)		
						(ATTACHING PARTS)		
-4	212-0523-00			4		. SCREW,MACHINE:10-32 X 2.750,HEX HD STL	83385	OBD
-5	210-0010-00			4		. WASHER,LOCK:INT,0.20 ID X0.376" OD,STL	78189	1210-00-00-0541C
-6	166-0457-00			4		. INSUL SLVG,ELEC:0.19 ID X 1.875"LONG MYLAR	80009	166-0457-00
-7	210-0812-00			3		. WASHER,NONMETAL:#10,FIBER	86445	OBD
-8	210-0445-00			4		. NUT,PLAIN,HEX.:10-32 X 0.375 INCH,STL	83385	OBD
-9	210-0458-00			1		. NUT,PL,ASSEM WA:8-32 X 0.344 INCH,STL	78189	511-081800-00
	343-0004-00			1		. CLAMP,LOOP:0.312 INCH DIAMETER,PLSTC	95987	5-16-6B
	210-0863-00			1		. WSHR,LOOP CLAMP:FOR 0.50" WIDE CLAMP,STL	95987	C191
						- - - * - - -		
-10	200-0234-00			1		. COVER,ELEC XFMR:3.437 X 4.125X 1.0,STEEL	80009	200-0234-00
-11	----- -----			1		. SELECTOR,VOLTS W/LINE FILTER:(SEE FL20 REPL)		
-12	334-3379-01			1		. MARKER,IDENT:MARKED GROUND SYMBOL	80009	334-3379-01
-13	210-0407-00			3		. NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
-14	210-0202-00			1		. TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
-15	210-0204-00			1		. TERMINAL,LUG:0.146 INCH DIA DE,45 DEG BEND	78189	2157-06-01-2520N
-16	----- -----			1		. SWITCH,THRMSTC:(SEE S21 REPL)		
						(ATTACHING PARTS)		
-17	211-0097-00			2		. SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
-18	210-0406-00			2		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-19	210-0004-00			2		. WASHER,LOCK:#4 INTL,0.015THK,STL CD PL	78189	1204-00-00-0541C
						- - - * - - -		
-20	361-0974-00			1		. SPACER,XFMR:0.08 X 4.126 X 3.438,AL	80009	361-0974-00
-21	220-0547-01			1		. NUT,BLOCK:0.38 X 0.25 X 0.282"OA	C00FW	OBD
						(ATTACHING PARTS)		
-22	211-0008-00			1		. SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-23	333-2529-00			1		. PANEL,REAR:POWER SUPPLY	80009	333-2529-00
						(ATTACHING PARTS)		
-24	211-0097-00			3		. SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-25	343-0004-00			2		. CLAMP,LOOP:0.312 INCH DIAMETER,PLSTC	95987	5-16-6B
						(ATTACHING PARTS)		
-26	211-0559-00			2		. SCREW,MACHINE:6-32 X 0.375"100 DEG,FLH STL	83385	OBD
-27	210-0407-00			2		. NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
-28	210-0863-00			2		. WSHR,LOOP CLAMP:FOR 0.50" WIDE CLAMP,STL	95987	C191
						- - - * - - -		
-29	----- -----			1		. SWITCH,PUSH-PULL:(SEE S22 REPL)		
-30	334-3763-00			1		. MARKER,IDENT:MKD CAUTION	80009	334-3763-00
-31	352-0595-00			2		. FUSEHOLDER,BLK:(3) 3AG	71400	2245-3
						(ATTACHING PARTS)		
-32	211-0510-00			4		. SCREW,MACHINE:6-32 X 0.375,PNH,STL,CD PL	83385	OBD
-33	210-0457-00			4		. NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-34	----- -----			1		. TRANSISTOR:(SEE Q120 REPL)		
						(ATTACHING PARTS)		
-35	211-0038-00			1		. SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG	83385	OBD
-36	210-0406-00			1		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-37	210-1178-00			1		. WSHR,SHOULDERED:FOR MTG TO-220 TRANSISTOR	49671	DF 137A
						- - - * - - -		
-38	342-0354-00			1		. INSULATOR,PLATE:TRANSISTOR,SILICON RUBBER	000BB	7403-10-52
-39	----- -----			1		. SEMICOND DEVICE:(SEE CR150 REPL)		
						(ATTACHING PARTS)		
-40	210-0445-00			1		. NUT,PLAIN,HEX.:10-32 X 0.375 INCH,STL	83385	OBD
-41	210-0206-00			1		. TERMINAL,LUG:SE #10	86928	A373-147-1
-42	210-0805-00			1		. WASHER,FLAT:0.204 ID X 0.438 INCH OD,STL	12327	OBD
-43	342-0498-00			1		. INSULATOR,WSH:0.625 OD X 0.196 ID	02107	OBD
-44	210-0910-00			1		. WASHER,NONMETAL:0.188 ID X 0.313" OD,TEFLON	02107	OBD
-45	342-0498-00			1		. INSULATOR,WSH:0.625 OD X 0.196 ID	02107	OBD
						- - - * - - -		

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-46	210-0201-00			1		. TERMINAL,LUG:SE #4	86928	A373-157-2
						(ATTACHING PARTS)		
-47	211-0008-00			1		. SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
-48	210-0406-00			1		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
						- - - * - - -		
-49	214-2980-00			1		. HEAT SINK,XSTR:TO-220,AL	80009	214-2980-00
						(ATTACHING PARTS)		
-50	211-0038-00			2		. SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG	83385	OBD
-51	210-0406-00			2		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-52	210-1178-00			2		. WSHR,SHOULDERED:FOR MTG TO-220 TRANSISTOR	49671	DF 137A
						- - - * - - -		
-53	342-0354-00			2		. INSULATOR,PLATE:TRANSISTOR,SILICON RUBBER	000BB	7403-10-52
-54	----- -----			2		. SEMICOND DEVICE:(SEE CR140 & CR900 REPL)		
						(ATTACHING PARTS)		
-55	211-0102-00			2		. SCREW,MACHINE:4-40 X 0.500",FLH,STL	83385	OBD
-56	210-0406-00			2		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-57	210-0801-00			2		. WASHER,FLAT:0.14 ID X 0.28I OD NP STL	12327	OBD
						- - - * - - -		
-58	----- -----			2		. TRANSISTOR:(SEE Q660 & Q760 REPL)		
						(ATTACHING PARTS)		
-59	211-0097-00			2		. SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
-60	210-0201-00			1		. TERMINAL,LUG:SE #4	86928	A373-157-2
-61	210-0406-00			2		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-62	210-1178-00			2		. WSHR,SHOULDERED:FOR MTG TO-220 TRANSISTOR	49671	DF 137A
						- - - * - - -		
-63	342-0354-00			2		. INSULATOR,PLATE:TRANSISTOR,SILICON RUBBER	000BB	7403-10-52
-64	214-2980-00			1		. HEAT SINK,XSTR:TO-220,AL	80009	214-2980-00
						(ATTACHING PARTS)		
-65	211-0097-00			2		. SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
-66	210-0406-00			2		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-67	210-1178-00			2		. WSHR,SHOULDERED:FOR MTG TO-220 TRANSISTOR	49671	DF 137A
						- - - * - - -		
-68	342-0354-00			2		. INSULATOR,PLATE:TRANSISTOR,SILICON RUBBER	000BB	7403-10-52
-69	----- -----			1		. SCR:(SEE Q1340 REPL)		
						(ATTACHING PARTS)		
-70	211-0038-00			1		. SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG	83385	OBD
-71	210-0406-00			1		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-72	210-1178-00			1		. WSHR,SHOULDERED:FOR MTG TO-220 TRANSISTOR	49671	DF 137A
						- - - * - - -		
-73	342-0355-00			1		. INSULATOR,PLATE:TRANSISTOR,SILICONE RUBBER	000BB	7403-09FR-51
-74	----- -----			2		. TRANSISTOR:(SEE Q500 & Q1320 REPL)		
						(ATTACHING PARTS)		
-75	211-0038-00			2		. SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG	83385	OBD
-76	210-0406-00			2		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-77	210-1178-00			2		. WSHR,SHOULDERED:FOR MTG TO-220 TRANSISTOR	49671	DF 137A
						- - - * - - -		
-78	342-0355-00			1		. INSULATOR,PLATE:TRANSISTOR,SILICONE RUBBER	000BB	7403-09FR-51
-79	348-0150-00			1		. GROMMET,PLASTIC:U SHAPED	80009	348-0150-00
-80	----- -----			1		. TRANSISTOR:(SEE Q1200 REPL)		
						(ATTACHING PARTS)		
-81	211-0025-00			1		. SCREW,MACHINE:4-40 X 0.375 100 DEG,FLH STL	83385	OBD
-82	210-0406-00			1		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-83	210-1122-00			1		. WASHER,LOCK:0.228 ID X 0.375 INCH OD,STL	04713	B52200F006
						- - - * - - -		
-84	342-0355-00			1		. INSULATOR,PLATE:TRANSISTOR,SILICONE RUBBER	000BB	7403-09FR-51
-85	----- -----			1		. TRANSISTOR:(SEE Q600 REPL)		
						(ATTACHING PARTS)		
-86	211-0025-00			1		. SCREW,MACHINE:4-40 X 0.375 100 DEG,FLH STL	83385	OBD
-87	210-0406-00			1		. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-88	210-1122-00			1		. WASHER,LOCK:0.228 ID X 0.375 INCH OD,STL	04713	B52200F006
						- - - * - - -		
-89	342-0355-00			1		. INSULATOR,PLATE:TRANSISTOR,SILICONE RUBBER	000BB	7403-09FR-51
-90	----- -----			1		. CKT BOARD ASSY:(SEE A7 REPL)		
						(ATTACHING PARTS)		
-91	211-0008-00			7		. SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-	----- -----			-		. . CKT BOARD ASSY INCLUDES:		
-92	136-0183-00			2		. . SOCKET,PLUG-IN:3 PIN,ROUND	80009	136-0183-00
-93	214-1291-00			2		. . HEAT SINK,ELEC:XSTR,0.72 OD X 0.375"H	05820	207-AB
-94	131-0589-00			24		. . TERM,PIN:0.46 L X 0.025 SQ.PH BRZ GL	22526	47350
-95	214-0579-00			8		. . TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-96	344-0326-00			6		. . CLIP,ELECTRICAL:FUSE,BRASS	75915	102071
-97	129-0455-00			2		. . SPACER,POST:0.305 L,W/4-40 THD THRU BRS	80009	129-0455-00
-98	----- -----			1		. . SEMICOND DEVICE:(SEE A7CR110 REPL)		
						(ATTACHING PARTS)		
-99	211-0038-00			1		. . SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG	83385	OBD
						- - - * - - -		
-100	343-0549-00			3		. STRAP,TIEDOWN:0.091 W X 3.62 INCH LONG	59730	TY23M
-101	195-0433-00			1		. LEAD,ELECTRICAL:18 AWG,7.0 L,8-19	80009	195-0433-00
	195-0436-00			1		. LEAD,ELECTRICAL:18 AWG,2.5 L,8-04	80009	195-0436-00
-102	195-0430-00			1		. LEAD,ELECTRICAL:18 AWG,7.0 L,8-01	80009	195-0430-00
	195-0432-00			1		. LEAD,ELECTRICAL:18 AWG,7.0 L,8-9	80009	195-0432-00
-103	195-0431-00			1		. LEAD,ELECTRICAL:18 AWG,8.0 L,8-02	80009	195-0431-00
-104	343-0004-00			2		CLAMP,LOOP:0.312 INCH DIAMETER,PLSTC	95987	5-16-6B
						(ATTACHING PARTS)		
-105	211-0559-00			2		SCREW,MACHINE:6-32 X 0.375"100 DEG,FLH STL	83385	OBD
-106	210-0863-00			2		WSHR,LOOP CLAMP:FOR 0.50" WIDE CLAMP,STL	95987	C191
						- - - * - - -		
-107	376-0127-00			1		COUPLER,SHAFT:PLASTIC	80009	376-0127-00
-108	211-0008-00			2		SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
-109	386-4160-00			1		STIF,CKT BOARD:	80009	386-4160-00
-110	211-0097-00			3		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD

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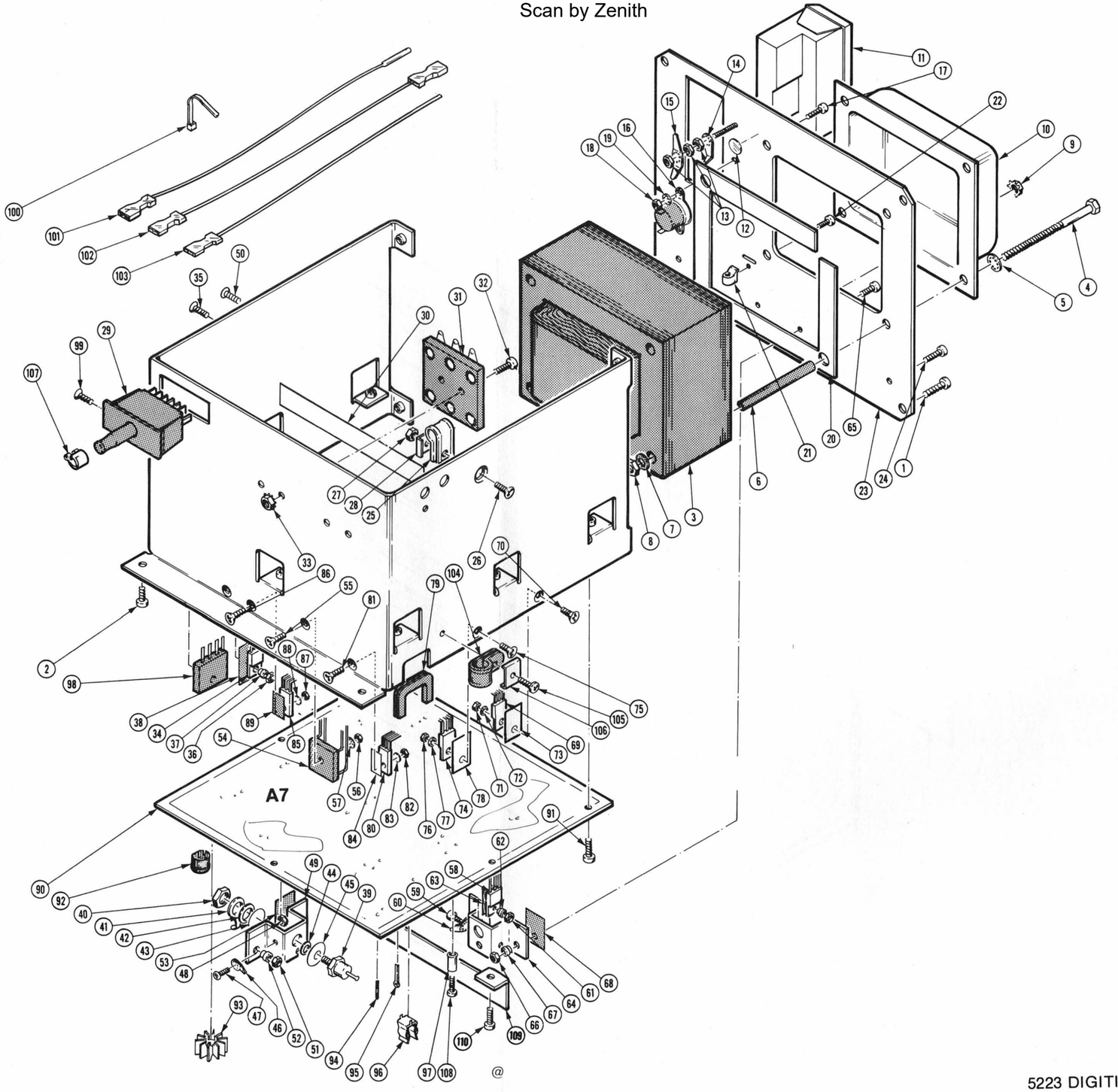

Fig. 3. POWER SUPPLY

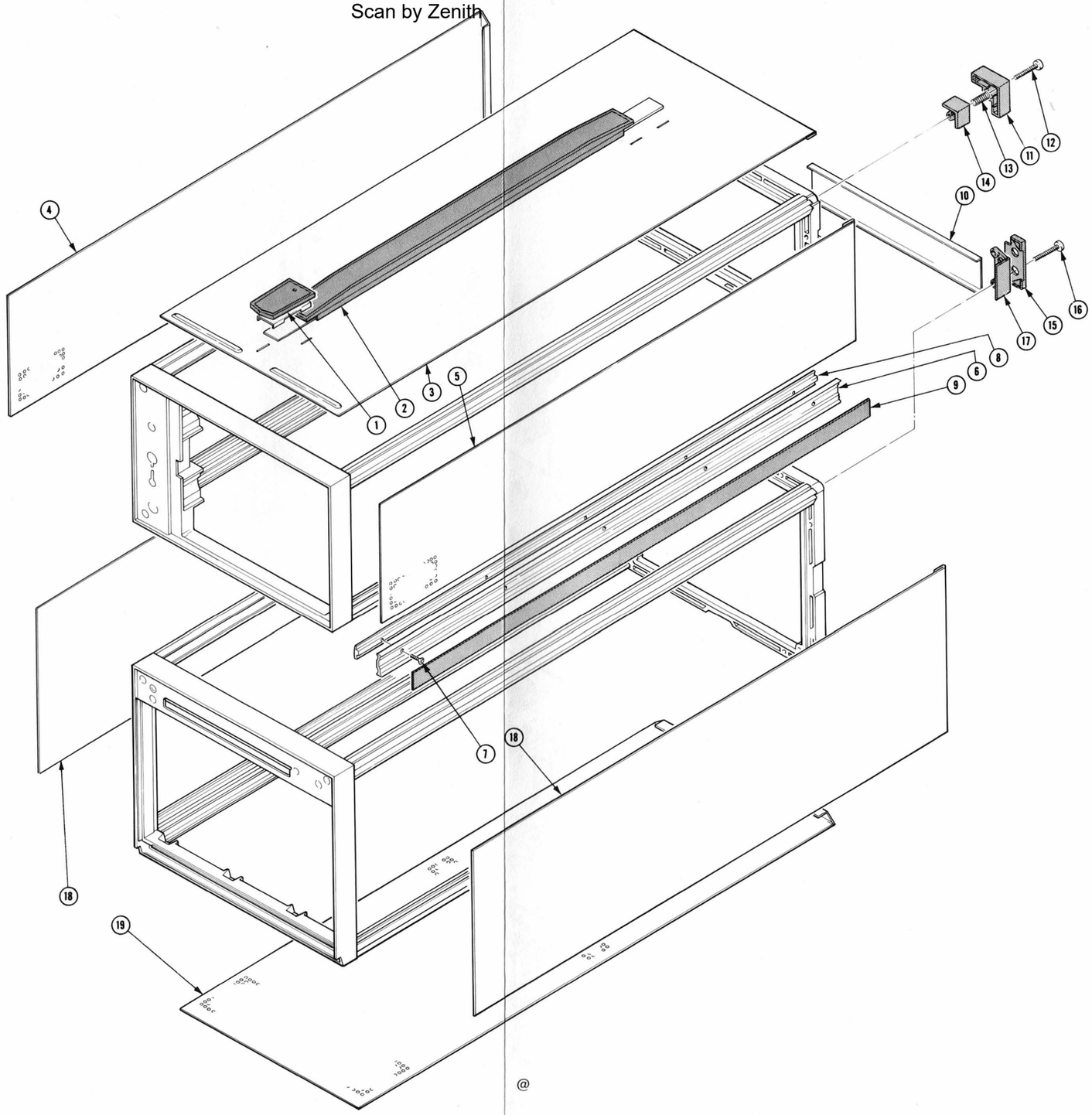

Fig. 4. BENCH CABINET

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
4-1	200-2191-00			2		CAP,RETAINER:PLASTIC	80009	200-2191-00
-2	367-0248-01			1		HANDLE,CARRYING:16.341 L,W/CLIP	80009	367-0248-01
-3	390-0674-01			1		CABINET TOP:HALF RACK	80009	390-0674-01
-4	390-0732-00			1		CAB. SIDE,SCOPE:LEFT	80009	390-0732-00
-5	390-0731-00			1		CAB. SIDE,SCOPE:RIGHT	80009	390-0731-00
-6	426-1565-00			2		FRAME SECT,CAB.:INTERLOCK,OUTER	80009	426-1565-00
						(ATTACHING PARTS)		
-7	211-0667-00			10		SCREW,MACHINE:6-32 X 0.281,FLH,100 DEG	93907	OBD
						- - - * - - -		
-8	426-1566-00			2		FRAME SECT,CAB:INTERLOCK,INNER	80009	426-1566-00
-9	124-0357-00			2		STRIP,TRIM:INTERLOCK,BLUE	80009	124-0357-00
-10	343-0773-00			1		RETAINER,CAB:0.5 RACK X (2) 5.25,AL	80009	343-0773-00
-11	343-0876-00			4		RTNR,CAB. COVER:OUTER CORNER	80009	343-0876-00
						(ATTACING PARTS)		
-12	212-0140-00			4		SCREW,MACHINE:8-32 X 0.75,SPCL 0.375 OD	80009	212-0140-00
						- - - * - - -		
-13	214-3078-00			4		SPRING,HLCPS:0.24 OD X 0.5 L	80009	214-3078-00
-14	343-0875-00			4		RTNR,CAB COVER:INNER CORNER	80009	343-0875-00
-15	343-0877-00			2		RETAINER,COVER:OUTER CORNER	80009	343-0877-00
						(ATTACHING PARTS)		
-16	212-0140-00			4		SCREW,MACHINE:8-32 X 0.75,SPCL 0.375 OD	80009	212-0140-00
						- - - * - - -		
-17	343-0878-00			2		RETAINER,COVER:INNER CORNER	80009	343-0878-00
-18	390-0662-00			2		CABINET SIDE:7.0 X 19.946	80009	390-0662-00
-19	390-0733-00			1		CAB. BOT,SCOPE:	80009	390-0733-00

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
5-1	333-2553-00			1		PANEL,FRONT:	80009	333-2553-00
						(ATTACHING PARTS)		
-2	210-0457-00			1		NUT,PL,ASSEM WA:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-3	378-0130-00			1		GRILLE,PLASTIC:8.164 X 0.462	80009	378-0130-00
-4	426-1593-01			1		FRAME PNL,CAB.:FRONT,1.75 X 1/2 RACK	80009	426-1593-01
						(ATTACHING PARTS)		
-5	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375 TAPTITE,FILH	80009	213-0863-00
						- - - * - - -		
-6	348-0614-00			1		GASKET:8.05 X 1.38 X 0.025	80009	348-0614-00
-7	105-0786-01			2		RELEASE,LATCH:W/COVER,PLASTIC	80009	105-0786-01
-8	105-0787-00			2		LATCH,RETAINING:RACKMOUNT,SST	80009	105-0787-00
-9	212-0567-00			2		SCREW,MACHINE:10-32-0.875,OVH,STL,NI PL	83385	OBD
-10	210-1298-00			2		WSHR,SHLDR & RECD:0.195 ID X 0.195 THK	80009	210-1298-00
-11	390-0717-02			1		CABINET SIDE:SPECIAL LEFT W/HANDLE	80009	390-0717-02
-12	390-0729-00			1		CAB. TOP,SCOPE:LEFT	80009	390-0729-00
-13	390-0672-00			1		CABINET BOTTOM:HALF RACK	80009	390-0672-00
-14	343-0876-01			1		RTNR,CAB. COVER:OUTER CORNER	80009	343-0876-01
						(ATTACHING PARTS)		
-15	212-0140-00			1		SCREW,MACHINE:8-32 X 0.75,SPCL 0.375 OD	80009	212-0140-00
						- - - * - - -		
-16	214-3078-00			1		SPRING,HLCPS:0.24 OD X 0.5 L	80009	214-3078-00
-17	343-0875-00			1		RTNR CAB COVER:INNER CORNER	80009	343-0875-00
-18	426-1598-03			1		FRAME,CABINET:REAR	80009	426-1598-03
						(ATTACHING PARTS)		
-19	213-0863-00			4		SCREW,TPG,TF:8-32 X 1.375,TAPTITE,FILH	80009	213-0863-00
						- - - * - - -		
-20	343-0817-00			1		RETAINER,CAB.:REAR STRIP,HALF RACK	80009	343-0817-00
-21	343-0816-00			1		RETAINER,CAB.:REAR STRIP 5.25 H	80009	343-0816-00
-22	343-0878-00			1		RETAINER COVER:INNER CORNER	80009	343-0878-00
-23	343-0877-00			1		RETAINER,COVER:OUTER CORNER	80009	343-0877-00
						(ATTACHING PARTS)		
-24	212-0140-00			2		SCREW,MACHINE:8:32 X 0.75,SPCL 0.375 OD	80009	212-0140-00
						- - - * - - -		
-25	343-0767-04			1		RETAINER,CAB.:CORNER	80009	343-0767-04
						(ATTACHING PARTS)		
-26	212-0140-00			2		SCREW,MACHINE:8-32 X 0.75,SPCL 0.375 OD	80009	212-0140-00
						- - - * - - -		
-27	337-2872-00			1		SHIELD,ELEC:PLUG-IN BOX	80009	337-2872-00
						(ATTACHING PARTS)		
-28	211-0501-00			2		SCREW,MACHINE:6-32 X 0.125 INCH,PNH STL	83385	OBD
						- - - * - - -		
-29	426-1665-00			2		FRAME SECT,CAB:	80009	426-1665-00
-30	426-1566-00			1		FRAME SECT,CAB.:INTERLOCK,INNER	80009	426-1566-00
-31	426-1565-00			1		FRAME SECT,CAB.:INTERLOCK,OUTER	80009	426-1565-00
						(ATTACHING PARTS)		
-32	211-0667-00			5		SCREW,MACHINE:6-32 X 0.281,FLH,100 DEG	93907	OBD
						- - - * - - -		
-33	124-0357-00			1		STRIP,TRIM:INTERLOCK	80009	124-0357-00
-34	426-1565-00			1		FRAME SECT,CAB.:INTERLOCK,OUTER	80009	426-1565-00
						(ATTACHING PARTS)		
-35	211-0667-00			5		SCREW,MACHINE:6-32 X 0.281,FLH,100 DEG	93907	OBD
						- - - * - - -		
-36	426-1566-00			1		FRAME SECT,CAB.:INTERLOCK,INNER	80009	426-1566-00
-37	390-0730-00			1		CAB. TOP,SCOPE:RIGHT	80009	390-0730-00
-38	343-0875-00			3		RTNR,CAB COVER:INNER CORNER	80009	343-0875-00
-39	343-0876-00			3		RTNR,CAB COVER:OUTER CORNER	80009	343-0876-00
						(ATTACHING PARTS)		
-40	212-0140-00			3		SCREW,MACHINE:8-32 X 0.75,SPCL 0.375 OD	80009	212-0140-00
						- - - * - - -		
-41	214-3078-00			3		SPRING,HLCPS:0.24 OD X 0.5 L	80009	214-3078-00
-42	124-0389-00			2		STRIP,TRIM:RACKMOUNT HANDLE	80009	124-0389-00
-43	361-1007-00			2		SPACER,HANDLE:0.156 THK,1.25 W,0.65 H	80009	361-1007-00
-44	348-0631-00			4		PAD,CUSHIONING:0.375 X 0.5 X 0.062	85471	348-0631-00

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
5-45	351-0104-03			PR		SLIDE SECT,DWR:12.625 L,W/O HARDWARE	06666	C-720-2
						(ATTACHING PARTS)		
-46	212-0070-00			10		SCREW,MACHINE:8-32 X 0.312"100 DEG,FLH STL	83385	OBD
-47	210-0458-00			10		NUT,PL,ASSEM WA:8-32 X 0.344 INCH,STL	78189	511-081800-00
						- - - * - - -		
-48	351-0241-02			PR		SLIDE,DWR,EXT:20.0 L,PAIR	80009	351-0241-02
-49	390-0718-01			1		CABINET SIDE:LEFT,W/HANDLE	80009	390-0718-01
-50	390-0733-00			1		CAB. BOT,SCOPE:	80009	390-0733-00
-51	124-0359-00			2		STRIP,TRIM:CORNER,BOT.	80009	124-0359-00

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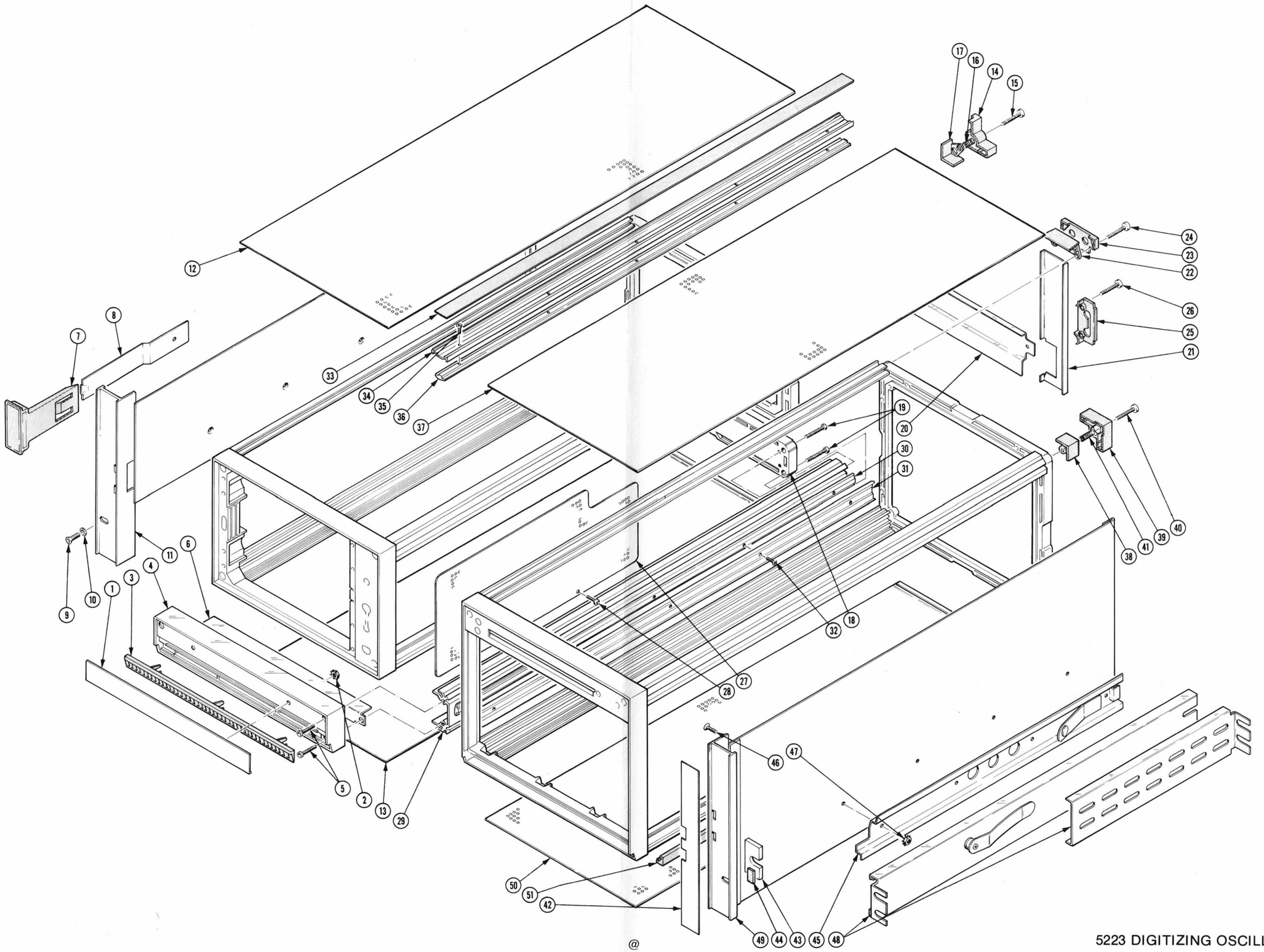


Fig. 5. RACKMOUNT CABINET

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
\- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
\- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
\- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

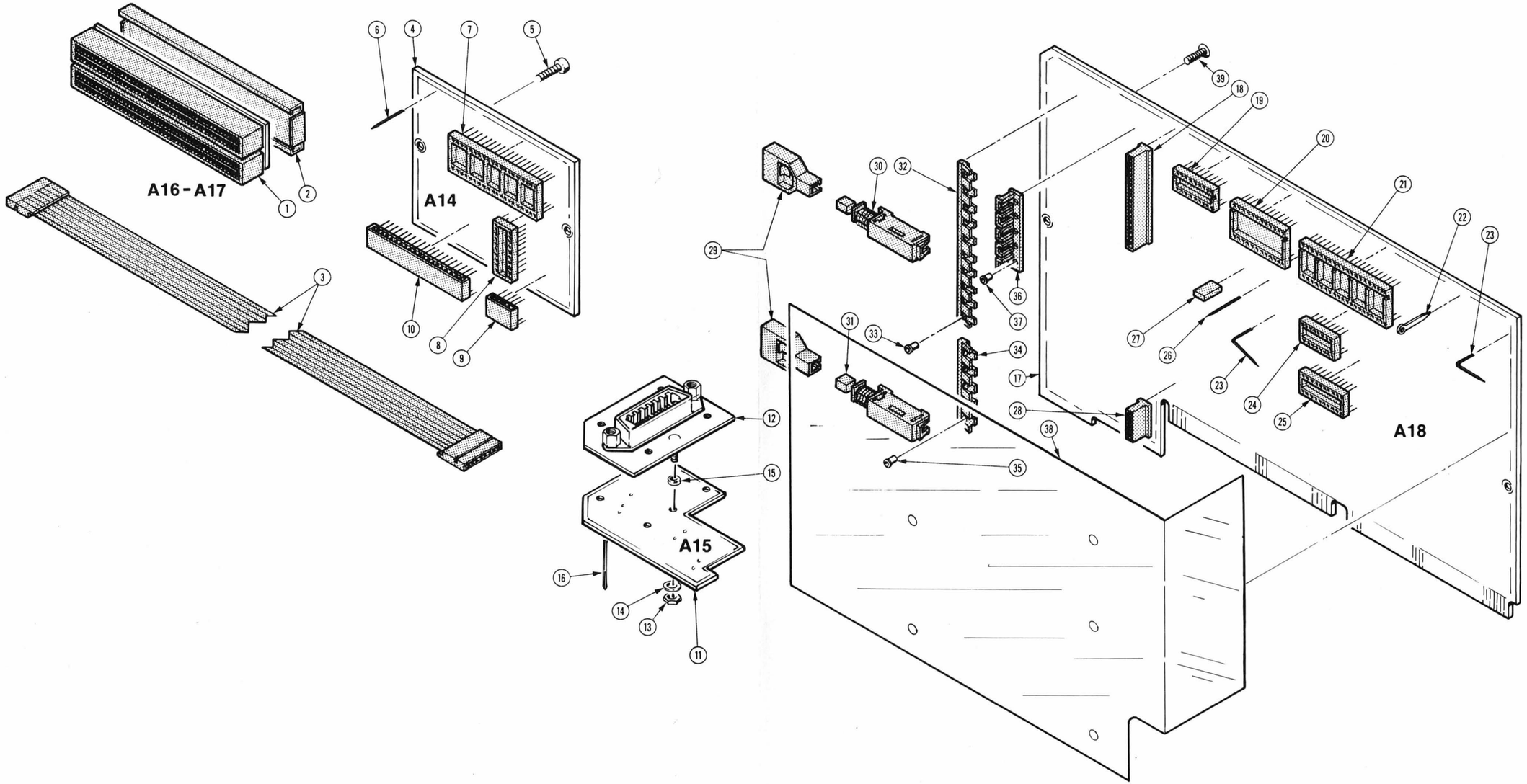
ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
07707	USM CORP., USM FASTENER DIV.	510 RIVER RD.	SHELTON, CT 06484
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
59730	THOMAS AND BETTS COMPANY	36 BUTLER ST.	ELIZABETH, NJ 07207
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
77250	PHEOLL MANUFACTURING CO., DIVISION OF ALLIED PRODUCTS CORP.	5700 W. ROOSEVELT RD.	CHICAGO, IL 60650
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
86928	SEASTROM MFG. COMPANY, INC.	701 SONORA AVENUE	GLENDALE, CA 91201

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
7-1	----- -----			2		CKT. BOARD ASSY:INTERCONNECT(SEE A16 & A17 REPL)		
-2	200-2487-00			2		COVER,CONNECTOR:GPIB,PLASTIC	80009	200-2487-00
-3	175-3804-00			1		CA ASSY,SP,ELEC:8,26 AWG,27.0 L RIBBON	80009	175-3804-00
	----- -----			-		(5223 ONLY)		
	175-3805-00			1		CA ASSY,SP,ELEC:8,26 AWG,27.0 L,RIBBON	80009	175-3805-00
	----- -----			-		(5223 ONLY)		
	175-3806-00			1		CA ASSY,SP,ELEC:8,26 AWG,27.0 L,RIBBON	80009	175-3806-00
	----- -----			-		(5223 ONLY)		
	175-3807-00			1		CA ASSY,SP,ELEC:8,26 AWG,36.0 L,RIBBON	80009	175-3807-00
	----- -----			-		(R5223 ONLY)		
	175-3808-00			1		CA ASSY,SP,ELEC:8,26 AWG,36.0 L,RIBBON	80009	175-3808-00
	----- -----			-		(R5223 ONLY)		
	175-3809-00			1		CA ASSY,SP,ELEC:8,26 AWG,36.0 L,RIBBON	80009	175-3809-00
	----- -----			-		(R5223 ONLY)		
	343-0549-00			4		STRAP,TIEDOWN:0.091 W X 3.62 INCH LONG	59730	TY23M
-4	----- -----			1		CKT. BOARD ASSY:DRIVER(SEE A14 REPL)		
						(ATTACHING PARTS)		
-5	211-0079-00			1		SCREW,MACHINE:2-56 X 0.188 INCH,PNH STL	77250	OBD
						- - - * - - -		
-6	131-0608-00			24		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-7	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
-8	136-0634-00			2		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-9	131-2002-00			1		. CONN,RCPT,ELEC:CKT BOARD,5 CONTACT,FEM	22526	65001-110
-10	131-1632-00			1		. CONNECTOR,RCPT,:CKT CD MTG,20CONTACT,FEM	22526	65001-025
-11	----- -----			1		CKT. BOARD ASSY:REAR PANEL(SEE A15 REPL)		
-12	386-4229-00			1		. PLATE,REAR:	80009	386-4229-00
						(ATTACHING PARTS)		
-13	210-0551-00			1		. NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	83385	OBD
-14	210-0994-00			1		. WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5714-147-20N
-15	361-0326-00			1		. SPACER,SLEEVE:0.18 ID X 0.25 OD X 0.10"L	80009	361-0326-00
						- - - * - - -		
-16	131-0787-00			25		. CONTACT,ELEC:0.64 INCH LONG	22526	47359
-17	----- -----			1		CKT. BOARD ASSY:GPIB(SEE A18 REPL)		
-18	131-2184-00			1		. CONN,RCPT,ELEC:CKT BD,1 X 17FEM,TOP ENTRY	22526	65780-017
-19	136-0670-00			2		. SKT,PL-IN ELEK:MICROCKT,18 PIN,LOW PROFILE	73803	CS9002-18
-20	136-0578-00			2		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-21	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
-22	214-0579-00			2		. TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-23	131-0787-00			13		. CONTACT,ELEC:0.64 INCH LONG	22526	47359
-24	136-0260-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CL	71785	133-51-92-008
-25	136-0634-00			1		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-26	131-0608-00			18		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-27	131-0993-00			5		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-28	131-2471-00			1		. CONN,RCPT,ELEC:CKT BOARD,6 CONTACT,FEM	22526	65780-006
-29	366-1818-00			8		. PUSH BTN ASSY:W/RED LED	80009	366-1818-00
-30	----- -----			1		. SWITCH PB ASSY:(SEE S260 REPL)		
-31	----- -----			7		. SWITCH,PB ASSY:(SEE S210,220,230,240,250,270		
	----- -----			-		. 280 REPL)		
-32	343-0495-05			1		. CLIP,SWITCH:FRONT,7.5MM X5 UNIT	80009	343-0495-05
						(ATTACHING PARTS)		
-33	210-3033-00			10		. EYELET,METALLIC:0.59 OD X 0.156 INCH LONG	07707	SE-25
						- - - * - - -		
-34	343-0495-10			1		. CLIP,SWITCH:FRONT,10 UNITS	80009	343-0495-10
						(ATTACHING PARTS)		
-35	210-3033-00			5		. EYELET,METALLIC:0.59 OD X 0.156 INCH LONG	07707	SE-25
						- - - * - - -		
-36	343-0499-05			3		. CLIP,SWITCH:REAR,7.5MM X 5 UNIT	80009	343-0499-05
						(ATTACHING PARTS)		
-37	210-3033-00			15		. EYELET,METALLIC:0.59 OD X 0.156 INCH LONG	07707	SE-25
-38	337-2811-00			1		. SHIELD,ELEC:CKT BOARD	80009	337-2811-00
						- - - * - - -		
-39	211-0038-00			2		SCREW,MACHINE:4-40 X 0.312,FLH,100 DEG	83385	OBD



5223 Option 10

FIG. 7 OPTION 10

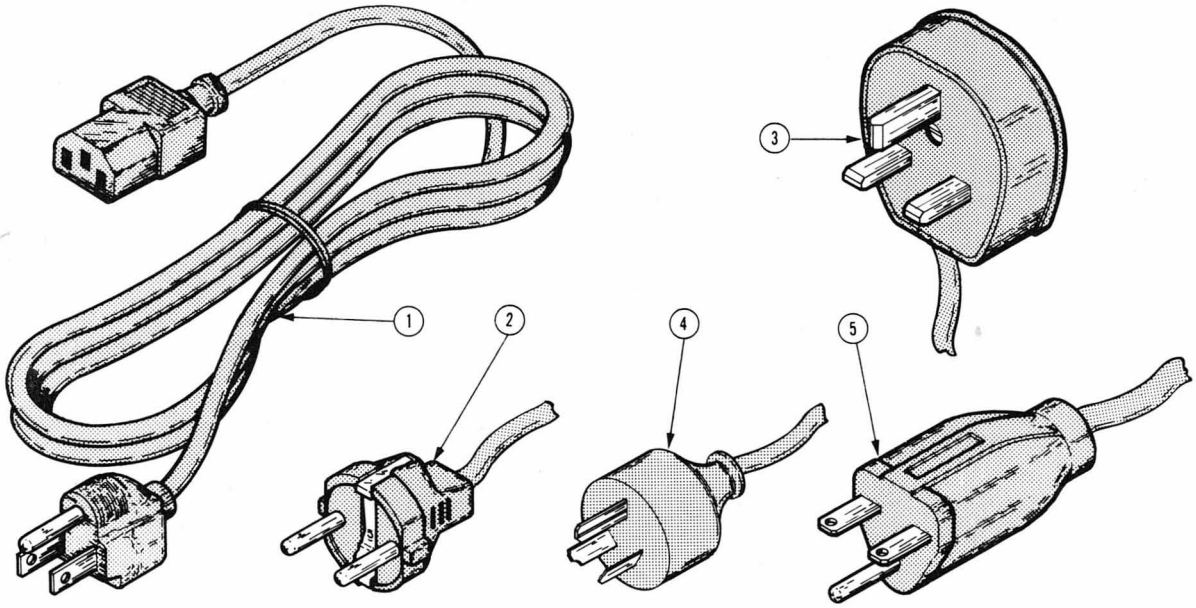


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	012-0630-01			1		CABLE,INTCON:2 METERS LONG	70903	YH-8925
	070-3714-00			1		MANUAL,TECH:OPERATORS	80009	070-3714-00
	070-3715-00			1		MANUAL,TECH:SERVICE	80009	070-3715-00
1-	161-0066-00			1		CABLE ASSY,PWR:3,18 AWG,115V,98.0 L	80009	161-0066-00
2-	161-0066-09			1		CABLE ASSY,PWR:3,0.75MM SQ,220V,96.0 L	80126	OBD
	----- -----			-		(OPTION A1 - EUROPEAN)		
3-	161-0066-10			1		CABLE ASSY,PWR:3,0.75MM SQ,240V,96.0 L	80126	OBD
	----- -----			-		(OPTION A2 - UNITED KINGDOM)		
4-	161-0066-11			1		CABLE ASSY,PWR:3,0.75MM,240V,96.0 L	80126	OBD
	----- -----			-		(OPTION A3 - AUSTRALIAN)		
5-	161-0066-12			1		CABLE ASSY,PWR:3,18 AWG,240V,96.0 L	80126	OBD
	----- -----			-		(OPTION A4 - NORTH AMERICAN)		
	378-0876-00			1		FILTER LT,CRT:BLUE	80009	378-0876-00

INSTRUCTIONS FOR COMPLETING THE SOFTWARE/FIRMWARE PERFORMANCE REPORT

I. Please type or print clearly. Use a separate Software/Firmware Performance Report (SFPR) for each problem.

II. SECTION A
Fill in serial number of instrument. List "ID?" response (see Section 3, GPIB Information) and copy the entire line of information.

III. SECTION B
Use the complete company mailing address. Include the name and phone number of the person reporting the error. Also, be sure to fill in the name of the person submitting the SFPR.

IV. SECTION C
Check the reason for report and whether the error is reproducible. We cannot fix a problem when we cannot reproduce the error condition.

V. SECTION D
Give a complete description of the system configuration on which the problem occurred. Include related peripherals, interfaces, options, special switch and/or strap settings and operating system.

VI. SECTION E
Describe the problem completely. Include any information which might help in evaluating the error with the SFPR. If you have determined a procedure to avoid the error condition, please include this procedure. If this problem prevents you from accomplishing any useful work with the product, please state this fact. Be sure to include with the SFPR any information (programs, listings, hard copies, etc.) which will help us to duplicate your problem.

VII. SECTION F
This section is for use by Tektronix Lab Scopes Software Maintenance personnel. DO NOT WRITE IN THIS SPACE.

VIII. Mail **all** copies of the Software/Firmware Performance Report to:

TEKTRONIX, INC.
LAB SCOPES SOFTWARE MAINTENANCE (39-111)
P.O. BOX 500
BEAVERTON, OREGON 97077

SEND TO: TEKTRONIX, INC.
LAB SCOPES SOFTWARE MAINTENANCE (39-111)
P.O. BOX 500
BEAVERTON, OREGON 97077

5223 SOFTWARE/FIRMWARE PERFORMANCE REPORT

PRODUCT NAME R/5223 Digitizing Oscilloscope OPTION 10 **SERIAL #** _____

LIST "ID?" RESPONSE (See Section 3, GPIB Information) _____

Ⓑ

COMPANY NAME: _____

USER: _____

ADDRESS: _____

CITY: _____ STATE: _____ ZIP: _____

PHONE: _____ EXTENSION: _____

FORM SUBMITTED BY: _____ DATE: _____

REASON FOR REPORT:
- ☐ Software/Firmware Error
- ☐ Documentation Error
- ☐ Suggested Enhancement

Ⓒ

IS THE ERROR REPRODUCIBLE?
- ☐ Yes ☐ No
- ☐ Intermittent

Ⓓ SYSTEM DESCRIPTION: (Hardware, software, firmware and host related to the problem)

Ⓔ DESCRIPTION OF PROBLEM:

LIST ENCLOSURES:

INTERNAL USE ONLY
(DO NOT WRITE BELOW THIS LINE)

Ⓕ

DATE RECEIVED _____

SPR # _____

SPR LOG

This form may be reproduced

Tektronix
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MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

SERVICE NOTE

Because of the universal parts procurement problem, some electrical parts in your instrument may be different from those described in the Replaceable Electrical Parts List. The parts used will in no way alter or compromise the performance or reliability of this instrument. They are installed when necessary to ensure prompt delivery to the customer. Order replacement parts from the Replaceable Electrical Parts List.

CALIBRATION TEST EQUIPMENT REPLACEMENT

Calibration Test Equipment Chart

This chart compares TM 500 product performance to that of older Tektronix equipment. Only those characteristics where significant specification differences occur, are listed. In some cases the new instrument may not be a total functional replacement. Additional support instrumentation may be needed or a change in calibration procedure may be necessary.

Comparison of Main Characteristics

DM 501 replaces 7D13		
PG 501 replaces 107	PG 501 - Risetime less than 3.5 ns into 50 Ω.	107 - Risetime less than 3.0 ns into 50 Ω.
108	PG 501 - 5 V output pulse; 3.5 ns Risetime	108 - 10 V output pulse 1 ns Risetime
PG 502 replaces 107		
108	PG 502 - 5 V output	108 - 10 V output
111	PG 502 - Risetime less than 1 ns; 10 ns Pretrigger pulse delay	111 - Risetime 0.5 ns; 30 to 250 ns Pretrigger pulse delay
PG 508 replaces 114	Performance of replacement equipment is the same or better than equipment being replaced.	
115		
2101		
PG 506 replaces 106	PG 506 - Positive-going trigger output signal at least 1 V; High Amplitude output, 60 V.	106 - Positive and Negative-going trigger output signal, 50 ns and 1 V; High Amplitude output, 100 V.
067-0502-01	PG 506 - Does not have chopped feature.	0502-01 - Comparator output can be alternately chopped to a reference voltage.
SG 503 replaces 190, 190A, 190B	SG 503 - Amplitude range 5 mV to 5.5 V p-p.	190B - Amplitude range 40 mV to 10 V p-p.
191		
067-0532-01	SG 503 - Frequency range 250 kHz to 250 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
SG 504 replaces 067-0532-01	SG 504 - Frequency range 245 MHz to 1050 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
067-0650-00		
TG 501 replaces 180, 180A	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	180A - Trigger pulses 1, 10, 100 Hz; 1, 10, and 100 kHz. Multiple time-marks can be generated simultaneously.
181		181 - Multiple time-marks
184	TG 501 - Trigger output-slaved to market output from 5 sec through 100 ns. One time-mark can be generated at a time.	184 - Separate trigger pulses of 1 and 0.1 sec; 10, 1, and 0.1 ms; 10 and 1 μs.
2901	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	2901 - Separate trigger pulses, from 5 sec to 0.1 μs. Multiple time-marks can be generated simultaneously.

NOTE: All TM 500 generator outputs are short-proof. All TM 500 plug-in instruments require TM 500-Series Power Module.

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MANUAL CHANGE INFORMATION

Date: 1-21-81 Change Reference: C1/181

Product: 5223 OPTION 10 SERVICE Manual Part No.: 070-3715-00

DESCRIPTION

SIGNATURE ANALYSIS CORRECTIONS

APPENDIX B, SIGNATURE ANALYSIS KERNAL TEST (continued)

Tab page (rear side), center panel

The Signatures column for SIGNATURE SET A-4 SETUP CHANGE TO READ:

Signatures
4POA
1A35
9P89
C660
2FUH
4782
AUF1
4A73
702H

The Signatures column for SIGNATURE SET A-7 SETUP CHANGE TO READ:

Signatures
826P
61HC
6AF8
3P96
52CF
62UA
4158
8HH0
1565

APPENDIX B, SIGNATURE ANALYSIS KERNAL TEST (continued)

Tab page (front side), center panel

The Signatures column for SIGNATURE SET A-9 SETUP CHANGE TO READ:

Signatures
826P
61HC
6AF8
3P96
52CF
62UA
4158
8HH0
1565

The Signatures column for SIGNATURE SET A-10 SETUP CHANGE TO READ:

Signatures
826P
5405
3C06
F4FA
76P6
C480
5HP7
P042
1PU4

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MANUAL CHANGE INFORMATION

Date: 4-13-81 Change Reference: M41674

Product: 5223 DIGITIZING OSCILLOSCOPE & OPTION 10 Manual Part No.: see below

DESCRIPTION

EFF SN B010152

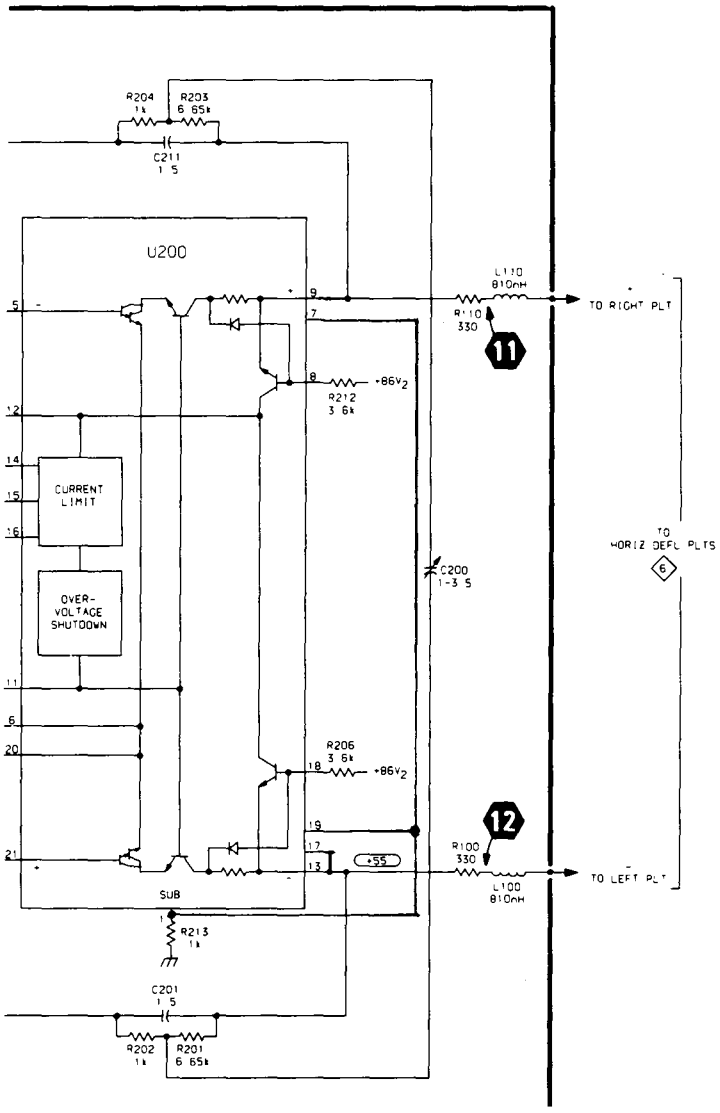
STANDARD INSTRUMENT (070-2932-00)

OPTION 10 INSTRUMENT (070-3715-00)

SCHEMATIC CHANGE

Change Diagram 4, Horizontal Amplifier, as shown:

Pin 7 and pin 19 go to R213.



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MANUAL CHANGE INFORMATION

Date: 4-13-81 Change Reference: M42550

Product: 5223 DIGITIZING OSCILLOSCOPE & OPTION 10 Manual Part No.: see below

DESCRIPTION

EFF SN B010272

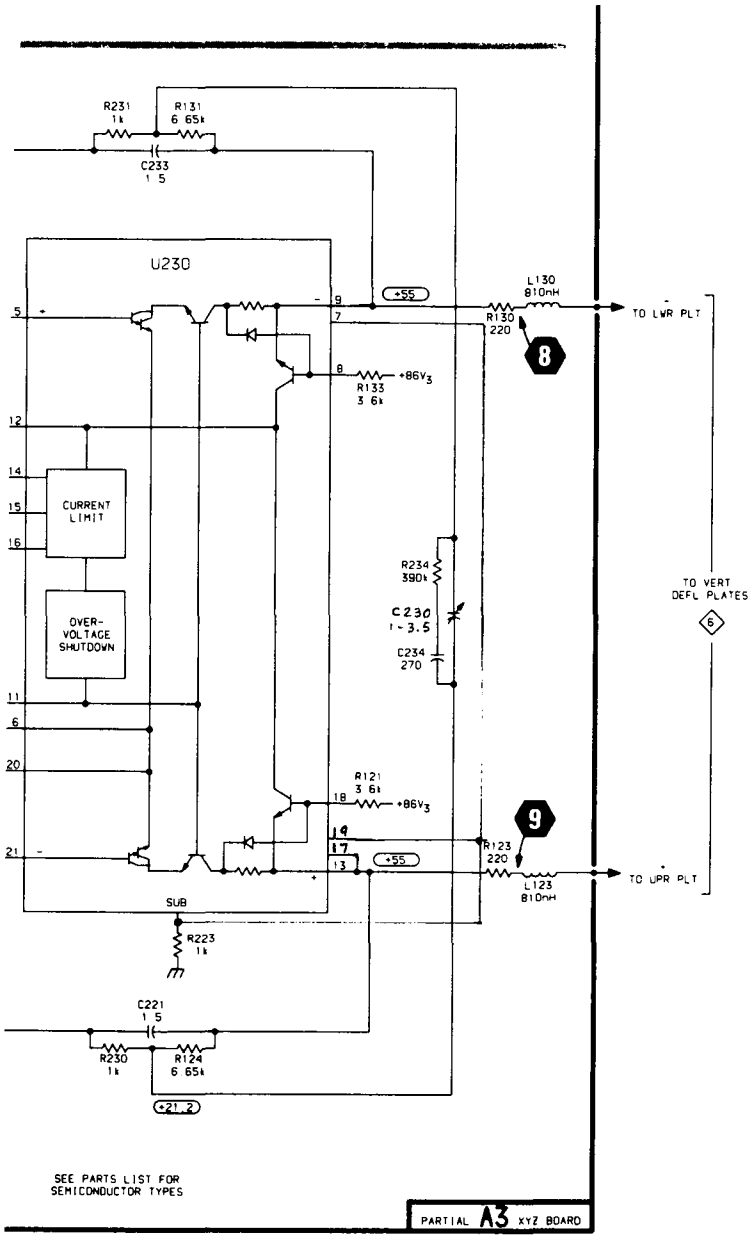
STANDARD INSTRUMENT (070-2932-00)

OPTION 10 INSTRUMENT (070-3715-00)

SCHEMATIC CHANGES

Change Diagram 3, Vertical Amplifier, as shown:

Pin 7 and pin 19 go to R223.



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MANUAL CHANGE INFORMATION

Date: 3-31-81 Change Reference: M42315 REV.

Product: 5223 DIGITIZING OSCILLOSCOPE & OPTION 10 Manual Part No.: see below

DESCRIPTION

EFF SN B010216 (070-2932-00) STANDARD,(070-3715-00) OPTION 10

REPLACEABLE ELECTRICAL PARTS AND SCHEMATIC CHANGES

CHANGE TO:

A3	670-5944-01	CKT BOARD ASSY:XYZ AMPLIFIER
C613	281-0773-00	CAP.,FXD,CER DI:0.01MFD,10%,100V

C613 is located on the XYZ circuit board and is shown on diagram 5 Z-Axis Amplifier & Front Panel.