THEORY OF OPERATION

This section describes the circuitry used in the 7104 Oscilloscope. The description begins with a discussion of the instrument, using the block diagram shown in Figure 3-1, and continues in detail, showing the relationships between the stages in each major circuit. Schematics of all major circuits are given in Section 8, Diagrams and Circuit Board Illustrations. Stages are outlined on the schematics with wide shaded lines. Stage names are in shaded boxes. Refer to these schematics throughout the following circuit description for specific electrical values and relationships.

BLOCK DIAGRAM

The following discussion is provided to assist in understanding the overall concept of the 7104 Oscilloscope mainframe before the individual circuits are discussed in detail. A basic block diagram of the 7104 is shown in Figure 3-1. Only the basic interconnections between the individual blocks are shown on this diagram. Each major circuit within the instrument is given a block. The number of each block refers to the complete circuit diagram located at the rear of this manual.

DESCRIPTION

Vertical signals to be displayed on the crt are applied to the Vertical Channel Switch circuit from both vertical plug-in compartments. The VERTICAL MODE switch is connected to the logic circuit and determines whether the signal from the LEFT VERT or RIGHT VERT compartment is displayed on the crt. The Vertical Channel Switch receives an X-Y inhibit signal from the Readout System to provide the time sharing between the vertical and readout signals.

The selected vertical signal passes through the Delay Line and is amplified by the Vertical Amplifier circuit to drive the vertical deflection plates of the crt (cathode-ray tube). The Vertical Amplifier circuit includes an input from the Readout System to produce the vertical portion of the alpha-numeric readout display.

Horizontal signals for display on the crt are connected to the Horizontal Channel Switch from both horizontal plug-in compartments. The signal from B HORIZ plug-in compartment may pass through the optional X-Y delay compensation network (Option 2 instruments only). The HORIZONTAL MODE switch determines whether the signal from the A HORIZ or B HORIZ compartment is displayed by the crt. The Horizontal Channel Switch receives an X-Y inhibit signal from the Readout System to provide the time sharing between the vertical and readout signals.

The selected horizontal signal is amplified by the Horizontal Amplifier circuit to provide horizontal deflection of the crt. The Horizontal Amplifier circuit accepts an input signal from the Readout System to produce the horizontal portion of the alpha-numeric readout display.

The Readout System provides an alpha-numeric display of information encoded by the plug-in unit(s). The readout display is written on the crt on a time-shared basis with the analog waveform display. The VERTICAL and HORIZONTAL MODE switch circuits determine which plug-in unit(s) displays readout information. The Readout System sends inhibit commands to the Vertical Channel Switch, Horizontal Channel Switch and Z-Axis logic circuits. The Readout System provides signals to produce the alpha-numeric display to the Vertical, Horizontal and Z-Axis Amplifier circuits.

The Logic circuit develops control signals for use in other circuits within the instrument and the plug-in units. These control signals automatically determine the correct instrument operation in relation to the plug-in units, plug-in unit control settings, and 7104 front-panel control settings. The Logic circuit performs three functions:

(1) Receives

a. The external Z-Axis Input signal.

b. The Single Sweep Reset Input from the rear panel.

c. The Z-Axis Inhibit Command from the Readout System.

(2) Sends the A and B SINGLE SWEEP READY signals to the rear panel.

(3) Develops the Z-Axis signal for use by the Z-Axis Amplifier.

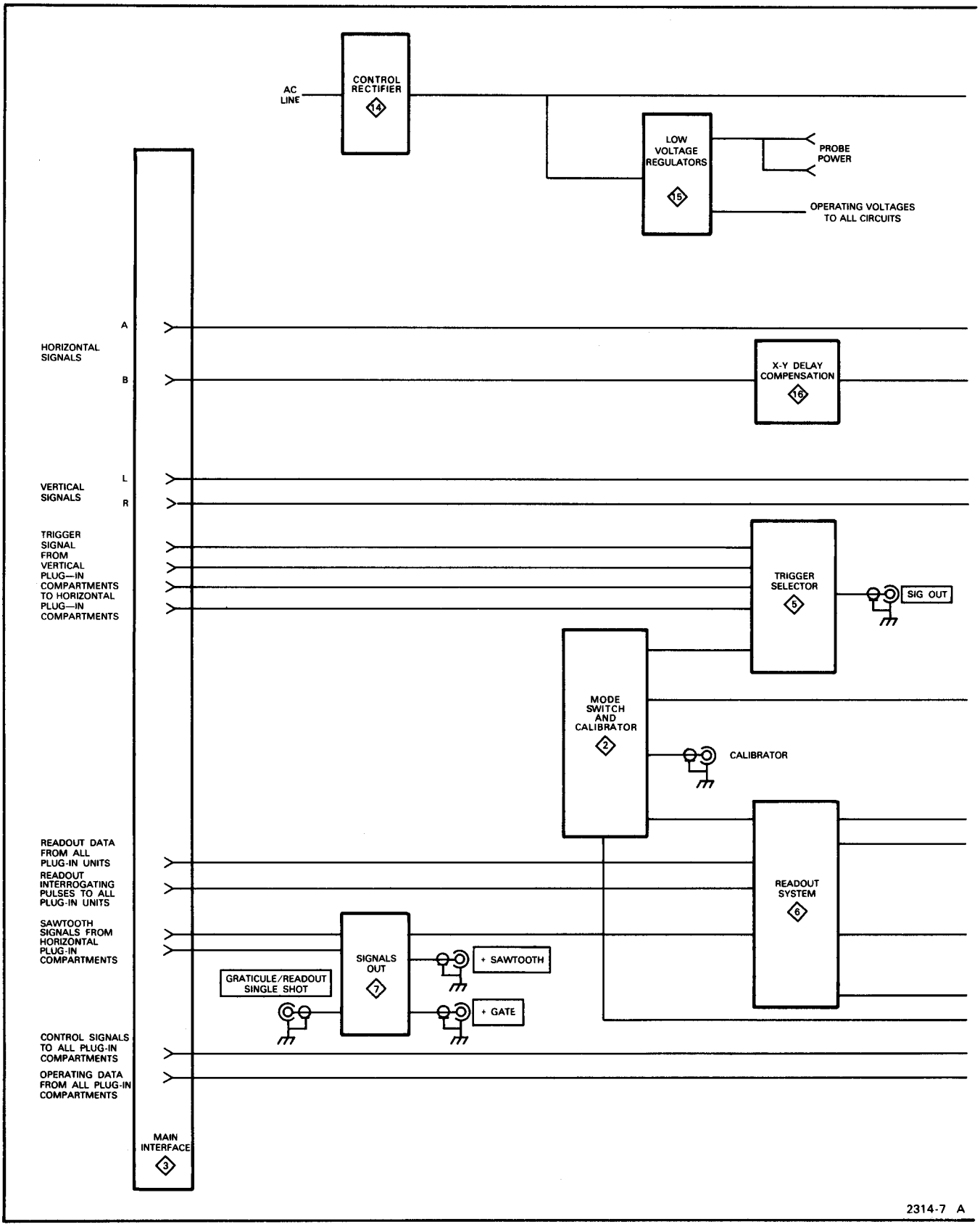


Figure 3-1. Basic block diagram of the 7104 Oscilloscope.

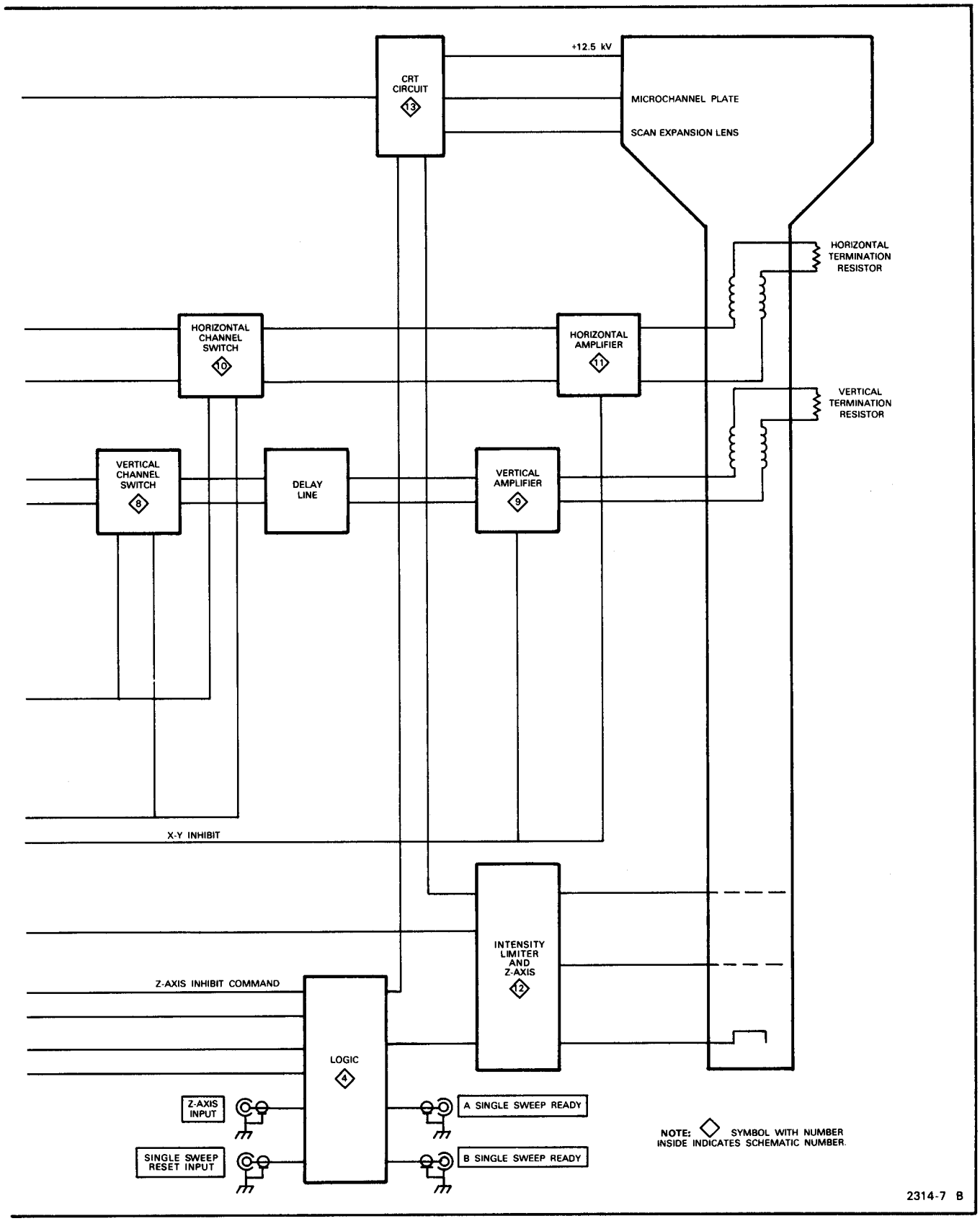


Figure 3-1. Basic block diagram of the 7104 Oscilloscope (continued).

In addition to control circuitry, the CRT Circuit supplies voltages necessary for operation of the crt by:

(1) Developing the operating voltages for the crt Microchannel Plate and the Scan Expansion Lens.

(2) Providing a signal proportional to the average screen current to the input of the intensity limiter level.

(3) Receiving a signal proportional to the intensity level setting from the logic circuit to be used by the Microchannel Plate supply for biasing. The Z-Axis Amplifier provides the drive signal to control the intensity level of the crt display.

The Calibrator circuit produces a one kilohertz square-wave signal which can be used to check the calibration of this instrument and the compensation of probes. The calibrator signal is available as a voltage at the CALIBRATOR connector or as a current through a 40 milliampere optional current loop accessory.

The internal trigger signals from the vertical plug-in units are connected to the Trigger Selector circuit. The Trigger Selector circuit determines whether the trigger signal from the left or right vertical unit is connected to the A or B horizontal unit. The B Trigger Channel Switch also produces the drive signal for the SIG OUT circuit to provide an output that is a sample of the vertical signal.

The Signals Out circuit processes signals from the plug-in units for the front-panel +GATE and +SAWTOOTH outputs.

The Control/Rectifier and Low-Voltage Regulator circuits provide the power necessary to operate the instrument. These voltages are connected to all circuits within the instrument.

DETAILED CIRCUIT OPERATION

A detailed description of the electrical operation and relationship of the circuits in the 7104 Oscilloscope mainframe is provided in this section. The theory of operation for circuits unique to this instrument is described in detail in the discussion. Circuits commonly used in the electronics industry are not described in detail. If more information is desired on these commonly used circuits, refer to the following textbooks:

Gordon V. Deboo, *Integrated circuits and Semiconductor Devices,* McGraw-Hill, New York, 1971.

Albert Paul Malvino, *Transistor Circuit Approximations,* McGraw-Hill, New York, 1973.

Joseph Milman and Herbert Taub, *Pulse, Digital and Switching Waveforms,* McGraw-Hill, New York, 1965.

LOGIC FUNDAMENTALS

Digital logic techniques are used to perform many functions within the instrument. The function and operation of the logic circuits are described using logic symbology and terminology, aiding in the understanding of these symbols and logic concepts, not a comprehensive discussion of the subject. For further information on binary number systems and the associated Boolean algebra concepts, the derivation of logic functions, or a more detailed analysis of digital logic, refer to the following textbooks:

Robert C. Baron and Albert T. Piccirilli, *Digital Logic and Computer Operation,* McGraw-Hill, New York, 1967.

Thomas C. Bartee, *Digital Computer Fundamentals,* McGraw-Hill, New York, 1966.

Yaohan Chu, *Digital Computer Design Fundamentals,* McGraw-Hill, New York, 1962.

Joseph Milman and Herbert Taub, *Pulse, Digital and Switching Waveforms,* McGraw-Hill, New York, Chapters 9-11, 1965.

SYMBOLS

The operation of circuits in this instrument which use digital techniques is described using the graphic symbols set forth in military standard MIL-STD-806B. Table 3-1 provides a basic logic reference for the logic devices used within this instrument. Any deviations from the standard symbology, or devices not defined by the standard are described in the circuit description for the applicable device.

NOTE

Logic Symbols used on the diagrams depict the logic function as used in this instrument and may differ from the manufacturer's data.

LOGIC POLARITY

All logic functions are described using the positive logic convention. Positive logic is a system of notation where the more positive of two levels (HI) is called the true or 1-state; the more negative level (LO) is called the false or 0-state. The HI-LO method of notation is used in this logic description. The specific voltages that constitute a HI or LO state vary between individual devices. Whenever possible, the input and output lines are named to indicate the function that they perform when at the HI (true) state.

TABLE 3-1
Basic Logic Reference

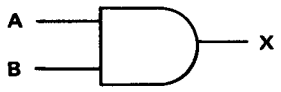
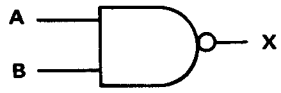
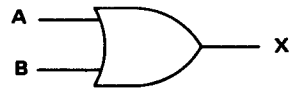
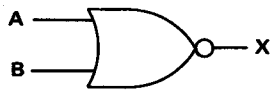
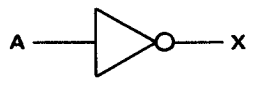
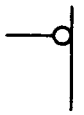
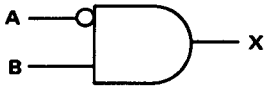
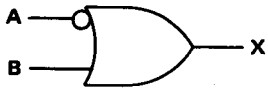
Device	Symbol	Description	Input/Output Table
AND gate		A device with two or more inputs and one output. The output of the AND gate is HI if and only if all of the inputs are at the HI state.	Input / Output A B X LO LO LO LO HI LO HI LO LO HI HI HI
NAND gate		A device with two or more inputs and one output. The output of the NAND gate is LO if and only if all of the inputs are at the HI state.	Input / Output A B X LO LO HI LO HI HI HI LO HI HI HI LO
OR gate		A device with two or more inputs and one output. The output of the OR gate is HI if one or more of the inputs are at the HI state.	Input / Output A B X LO LO LO LO HI HI HI LO HI HI HI HI
NOR gate		A device with two or more inputs and one output. The output of the NOR gate is LO if one or more of the inputs are at the HI state.	Input / Output A B X LO LO HI LO HI LO HI LO LO HI HI LO
Inverter		A device with one input and one output. The output state is always opposite to the input state.	Input / Output A X LO HI HI LO

TABLE 3-1 (CONT.)
Basic Logic Reference

<table>
<tr><th>Device</th><th>Symbol</th><th>Description</th><th>Input/Output Table</th></tr>
<tr><td>LO-state indicator</td><td> 
 

 
</td><td>A small circle at the input or output of a symbol indicates that the LO state is the significant state. Absence of the circle indicates that the HI state is the significant state. Two examples follow:

AND gate with LO-state indicator at the A input.

The output of this gate is HI if and only if the A input is LO and the B input is HI.

OR gate with LO-state indicator at the A input:

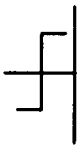
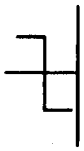
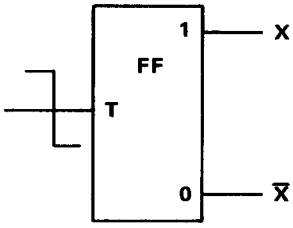
The output of this gate is HI if either the A input is LO or the B input is HI.</td><td>Input / Output
<table><tr><th>A</th><th>B</th><th>X</th></tr><tr><td>LO</td><td>LO</td><td>LO</td></tr><tr><td>LO</td><td>HI</td><td>HI</td></tr><tr><td>HI</td><td>LO</td><td>LO</td></tr><tr><td>HI</td><td>HI</td><td>LO</td></tr></table>
Input / Output
<table><tr><th>A</th><th>B</th><th>X</th></tr><tr><td>LO</td><td>LO</td><td>HI</td></tr><tr><td>LO</td><td>HI</td><td>HI</td></tr><tr><td>HI</td><td>LO</td><td>LO</td></tr><tr><td>HI</td><td>HI</td><td>HI</td></tr></table></td></tr>
<tr><td>Edge symbol</td><td> 
  </td><td>Normally superimposed on an input line to a logic symbol. Indicates that this input (usually the trigger input of a flip-flop) responds to the indicated transition of the applied signal.</td><td></td></tr>
<tr><td>Triggered (toggle) Flip-Flop</td><td> 
</td><td>A bistable device with one input and two outputs (either or both outputs may be used). When triggered, the outputs change from one stable state to the other stable state with each trigger. The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity depending on the device.</td><td>Input / Output
<table><tr><th colspan="2">Condition before trigger pulse</th><th colspan="2">Condition after trigger pulse</th></tr><tr><td>X</td><td>$\overline{X}$</td><td>X</td><td>$\overline{X}$</td></tr><tr><td>LO</td><td>HI</td><td>HI</td><td>LO</td></tr><tr><td>HI</td><td>LO</td><td>LO</td><td>HI</td></tr></table></td></tr>
</table>

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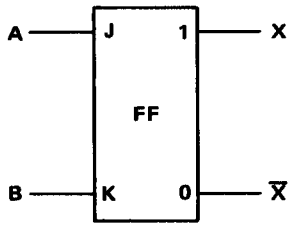
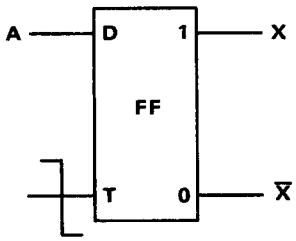
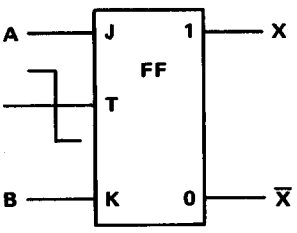
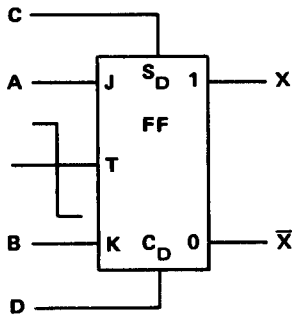
TABLE 3-1 (CONT.)
Basic Logic Reference

Device	Symbol	Description	Input/Output Table
Set-Clear (J-K) Flip-Flop		A bistable device with two inputs and two outputs (either or both outputs may be used). The outputs change state in response to the states at the inputs. The outputs are complementary (i.e., when one output is HI the other is LO).	Input / Output A | B | X | $\overline{X}$ LO | LO | No change LO | HI | LO | HI HI | LO | HI | LO HI | HI | Changes state
D (data) Type Flip-Flop		A bistable device with two inputs and two outputs (either or both outputs may be used). When triggered the state of the "1" output changes to the state at the data (D) input prior to the trigger. The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity, depending on the device.	Input / Output A | X | $\overline{X}$ LO | LO | HI HI | HI | LO **Output conditions shown after trigger pulse**
Triggered Set-Clear (J-K) Flip-Flop		A bistable device with three or more inputs and two outputs (either or both outputs may be used). When triggered, the outputs change state in response to the states at the inputs prior to the trigger. The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity depending on the device.	Input / Output A | B | X | $\overline{X}$ LO | LO | No change LO | HI | LO | HI HI | LO | HI | LO HI | HI | Changes state **Output conditions shown after trigger pulse**
Flip-Flop with Direct Inputs (may be applied to all triggered flip-flops)		For devices with direct-set (S_D) or direct-clear (C_D) inputs, the indicated state at either of these inputs over-rides all other inputs (including trigger) to set the outputs to the states shown in the input/output table.	Input / Output A | B | C | D | X | $\overline{X}$ 1 | 1 | LO | LO | No change[1] Φ | Φ | LO | HI | LO | HI Φ | Φ | HI | LO | HI | LO Φ | Φ | HI | HI | Undefined **Φ = Has no effect in this case** **[1]Output state determined by conditions at triggered inputs**

INPUT/OUTPUT TABLES

Input/Output (truth) tables show the input combinations important to a particular function, along with the resultant output conditions. This table may be given either for an individual device or for a complete logic stage. Examples of input/output tables for individual devices can be seen in Table 3-1.

NON-DIGITAL DEVICES

Not all of the integrated circuit devices in this instrument are digital logic devices. The function of non-digital devices is described individually, using operating waveforms or other techniques to illustrate their function.

CABLE DISTRIBUTION

Diagram 1, shows the cable inter-connections between circuit boards within the 7104.

MODE SWITCH AND CALIBRATOR

A schematic diagram of the Mode Switch and Calibrator circuits is given on diagram 2, in section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by gray shaded lines separating the circuitry into major stages. These stages aid in locating components mentioned here. Sub-headings use the stage names to further identify portions of the circuitry on diagram 2.

CALIBRATOR

The Calibrator circuit provides voltage outputs of 40 millivolts, 0.4 volt and 4 volts at the CALIBRATOR output connector. A current output of 40 milliamperes is available from the Calibrator circuit with an optional current loop adapter. When using the current loop adapter the Calibrator must be operated only in the 4 V switch position, for stated output.

Transistors Q376 and Q382 form a 1 kilohertz, square-wave oscillator. Oscillation occurs as follows: Initially assume that Q376 is conducting and Q382 is not conducting. The voltage at the emitter of Q382 becomes more negative as C376 discharges through R381. Capacitor C376 discharges until the emitter-base junction of Q382 becomes forward biased. As Q382 begins conducting the oscillator changes states. Regeneration starts when Q382 conducts and C376 stops discharging; this reduces the collector current of Q376. Thus, the collector voltage of Q376 rises positive which causes the base and emitter of Q382 to rise positive. The positive going voltage is coupled by C376 to the emitter of Q376, turning it off.

At this time, Q382 is conducting and Q376 is not conducting. The voltage at the emitter of Q376 goes negative as C376 charges through R376. When the emitter-base junction of Q376 becomes forward biased the oscillator will again change states to complete the cycle.

The square-wave signal produced at the collector of Q382 switches Q384 on and off. When Q384 is on, the current from R383 and R384 flows to ground. When Q384 is off, this current flows through CR386 and R386 into the voltage divider network of R387, R392, R393, R394, R395, R396, and R397 to produce the 4 volt, 0.4 volt and 40 millivolt Calibrator output voltages. The accuracy of the Calibrator is set by the 0.4 Volts DC adjustment, R385. Both the 4V and 0.4V calibrator switches must be engaged when adjusting R385. The Calibrator frequency is set by the 1 kHz adjustment, R375.

MODE SWITCHING

The Mode Switching circuit includes front-panel switching and provides the logic for selection of the vertical and horizontal compartments to provide deflection for the crt. The Mode Switching circuit operates in conjunction with the Logic circuit (diagram 4) to develop control signals for use in other circuits within this instrument and plug-in units installed in the plug-in compartments. Table 3-2 shows the outputs produced with all combinations of the front-panel switch positions.

MAIN INTERFACE

Diagram 3 shows the plug-in interface and the inter-connections between the plug-in compartments, circuit boards, etc. of this instrument. The signal and voltage connections of each interface connector are also identified in diagram 3.

LOGIC

A schematic diagram of the Logic circuit is given on diagram 4, in section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by gray shaded lines separating the circuitry into major stages. These stages aid in locating components mentioned here. Sub-headings in the following discussion use these stage names to further identify portions of the circuitry on diagram 4.

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TABLE 3-2
Mode Switching Inputs/Outputs

FRONT-PANEL SWITCH POSITIONS (INPUTS)																MODE SWITCHING OUTPUTS						
A TRIGGER SOURCE SWITCH			B TRIGGER SOURCE SWITCH			VERTICAL MODE SWITCH					HORIZONTAL MODE SWITCH				A TIME-BASE UNIT DELAY MODE	$\overline{\text{VERT MODE SIG}}$	HORIZ SLAVE ENABLE	RIGHT	$\overline{\text{ADD}}$	A AND B TRIGGER SWITCH LIGHTS		
VERT MODE	LEFT VERT	RIGHT VERT	VERT MODE	LEFT VERT	RIGHT VERT	LEFT	ALT	ADD	CHOP	RIGHT	A	ALT	CHOP	B						VERT MODE	LEFT VERT	RIGHT VERT
	●			●														LO	HI		ON	
		●			●													HI	HI			ON
●			●			●										HI	LO	LO	HI	ON	ON	
●			●					●								HI	LO	LO	LO	ON	ON	ON
●			●						●							CHOP	LO	LO	HI	ON	ON	
●			●							●						LO	LO	HI	HI	ON		ON
●			●				●				●					ALT	LO	ALT	HI	ON	ON	ON
●			●				●							●		ALT	LO	ALT	HI	ON	ON	ON
●							●					●				ALT	HI	HI	HI	ON		ON
●							●						●			ALT	HI	HI	HI	ON		ON
			●				●					●				ALT	HI	LO	HI	ON	ON	
			●				●						●			ALT	HI	LO	HI	ON	ON	
			●				●								●	ALT	LO	ALT	HI	ON	ON	ON

The Logic circuit develops control signals for use in other circuits within this instrument and any plug-in units installed in the vertical and horizontal compartments. These control signals automatically determine the correct instrument operation in relation to the plug-in units installed or selected, plug-in control settings, and 7104 control settings.

HORIZONTAL LOGIC

The Horizontal Logic stage performs three separate logic functions: A Sweep Lockout, B Sweep Lockout, and Alternate Pulse Generation. The majority of the Logic for these functions are contained within the Horizontal Logic IC, U4428. Figure 3-2 identifies the three individual stages of U4428 and the input and output terminals associated with each. Note that some of the input levels are connected internally to more than one of the individual stages.

A Sweep Lockout

The A Sweep Lockout portion of the Horizontal Logic IC (U4428) produces an output level at the collector of Q4462 (A Sweep Inhibit) that determines when the A HORIZ time-base unit can produce a sweep. If this output is HI, the A HORIZ unit is locked out (disabled) not producing a sweep. If the level is LO, the A HORIZ unit is enabled and produces a sweep when triggered.

Only two combinations of input conditions to U4428 will produce a HI A Sweep Inhibit level, as shown by Table 3-3. If non-delayed operation is being used, the first combination disables the A sweep while the B sweep is being displayed in the ALT horizontal mode (both units must be in time-base mode). The second combination disables the A sweep during delayed-sweep operation enabling the B sweep to complete its holdoff before the next A sweep begins.

B Sweep Lockout

The B Sweep Lockout stage produces an output level at the collector of Q4468 determining whether the B HORIZ time-base unit can produce a sweep. A HI output level locks out (inhibits) the B HORIZ unit and a LO level enables the B HORIZ unit to produce a sweep.

The output of this stage is HI only under one set of input conditions to U4428, as shown by Table 3-4. (This set of conditions disables the B sweep while the A sweep is being displayed in the ALT, HORIZONTAL MODE switch position, if both time-base units are in a sweep mode and

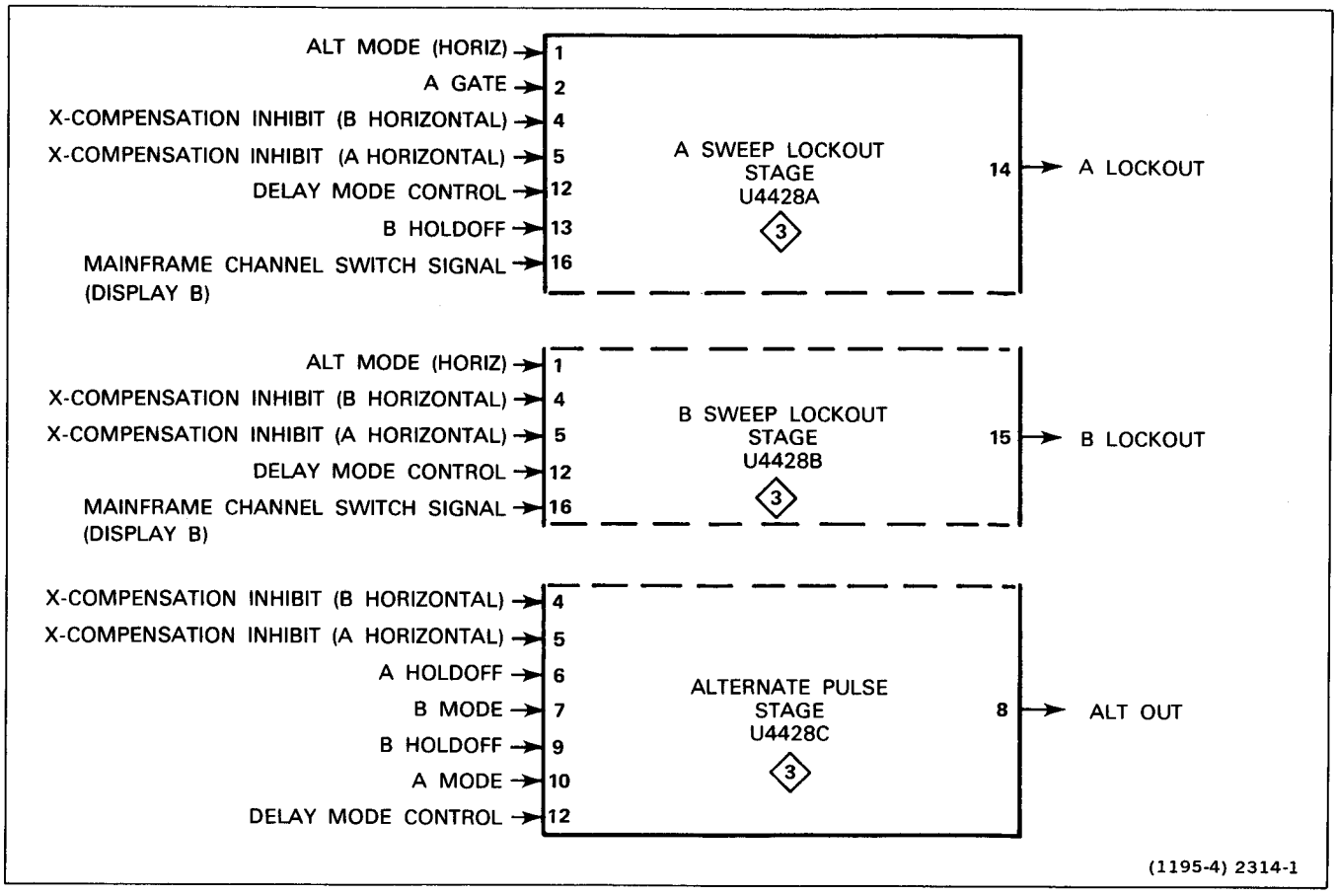

Figure 3-2. Breakdown of separate stages within Horizontal Logic IC (4428).

TABLE 3-3
Input/Output Combinations for A Lockout (U4428 Pin 14)

INPUT							OUTPUT
ALT MODE (HORIZ)	A GATE	X-COMPENSATION INHIBIT (B HORIZONTAL)	X-COMPENSATION INHIBIT (A HORIZONTAL)	DELAY MODE CONTROL	B HOLDOFF	DISPLAY B COMMAND	A LOCKOUT
1	2	4	5	12	13	16	14
HI	Φ	HI	HI	LO	Φ	HI	HI
Φ	LO	Φ	Φ	HI	HI	Φ	HI
ALL OTHER COMBINATION							LO

Φ = HAS NO EFFECT IN THIS CASE

TABLE 3-4
Input/Output Combinations for B Lockout (U4428 Pin 15)

INPUT						OUTPUT
ALT MODE (HORIZ)	X-COMPENSATION INHIBIT (B HORIZONTAL)	X-COMPENSATION INHIBIT (A HORIZONTAL)	DELAY MODE CONTROL	DISPLAY B COMMAND	B LOCKOUT
1	4	5	12	16	15
HI	HI	HI	LO	LO	HI
ALL OTHER COMBINATIONS					LO

non-delayed sweep is used.) For any other combination of input conditions, the B Sweep Lockout level is determined by the Delay Gate (from A time-base unit); see Main Interface, diagram 3.

Alternate Pulse Generator

The third function performed by the Horizontal Logic stage is the production of an Alternate Pulse signal for use by the Plug-In Binary and Vertical Binary stages. The holdoff gate produced at the end of the sweep by the respective time-base unit is differentiated by either C4335 or C4423, providing a positive-going pulse to pin 6 or 9 of U4428. The differentiated A or B holdoff gate may produce the alternate pulse depending upon the operating conditions as shown in Table 3-5.

(1) A (Only) Mode

An Alternate Pulse is produced at the end of each A sweep when the HORIZONTAL MODE switch is set to the A position.

(2) B (Only) Mode

In the B position of the HORIZONTAL MODE switch, an Alternate Pulse is produced at the end of each B sweep. (The A time-base must be in independent, non-delayed mode.)

TABLE 3-5
Input/Output Combinations for Alternate Pulse (U4428 Pin 8)

INPUT							OUTPUT	
X-COMPENSATION INHIBIT (B HORIZONTAL) 4	X-COMPENSATION INHIBIT (A HORIZONTAL) 5	A HOLDOFF 6	B MODE 7	B HOLDOFF 9	A MODE 10	DELAY MODE CONTROL 12	TIME-BASE WHICH IS SOURCE OF ALTERNATE PULSE 8[2]	HORIZONTAL CONDITIONS
HI	Φ	HI[1]	LO	Φ	HI	Φ	A	A ONLY
Φ	HI	Φ	HI	HI[1]	LO	LO	B	B ONLY
HI	HI	HI[1]	LO	HI[1]	LO	LO	A AND B	ALT OR CHOP
HI	HI	HI[1]	Φ	Φ	Φ	HI	A	A DELAYS B
HI	LO	HI[1]	LO	LO	Φ	Φ	A	A WITH VERTICAL UNIT IN B COMPARTMENT.
LO	HI	LO	Φ	HI[1]	LO	LO	B	B WITH VERTICAL UNIT IN A COMPARTMENT.
ALL OTHER COMBINATIONS							NO OUTPUT PULSE (LO AT OUTPUT)	

Φ = Has no effect in this case.

[1]Positive-going pulse. Where both A and B Holdoff are required to be HI, a HI at either input produces an alternate pulse.

[2]Negative-going pulse.

(3) Alt or Chop Mode

When the HORIZONTAL MODE switch is set to ALT or CHOP (the A time-base unit must be in independent, non-delayed mode), an Alternate Pulse is produced at the end of each sweep. For example, an Alternate Pulse is produced at the end of the A sweep, then at the end of the B sweep, again at the end of the A sweep, etc. Although Alternate Pulses are produced in the CHOP horizontal mode, they are not used in this instrument.

(4) Delayed Sweep (A Delays B)

When the A time-base unit is set for delayed operation, the operation of the Alternate Pulse Generator is changed producing an Alternate Pulse only at the end of the A sweep, even when the HORIZONTAL MODE switch is set to B. This is necessary since the A time-base establishes the amount of delay time for the B time-base unit whenever it is displayed.

(5) Amplifier Unit in Horizontal Compartment

When an amplifier unit is installed in either of the horizontal plug-in compartments, the Alternate Pulse can be produced only from the remaining time-base unit. If amplifier units are installed in both horizontal compartments, an Alternate Pulse is not produced since there are no time-base units to produce a holdoff pulse.

Z-AXIS LOGIC

The Z-Axis Logic stage produces an output current signal at pin 8 of U4485 which sets the intensity of the crt display except for the readout display which is controlled by the Readout System. The output current at pin 8 is determined by the setting of the A or B INTENSITY controls, and the Auxiliary Z-Axis input. The Auxiliary Z-Axis input is produced by either the External Z-Axis input or by an input from any of the plug-in units; see Main Interface, diagram 3. The input current from the A and B INTENSITY controls is switched matching the output current to the horizontal display. The Vertical Chopped Blanking, Horizontal Chopped Blanking, and readout blanking signals are applied to this stage to block the output current and blank the crt display for vertical chopping, horizontal chopping, or during a readout display.

The inputs to the Z-Axis Logic stage (U4485) pins 1, 2, 9, and 16 are current-driven and are variable from zero to four milliamperes.

The Vertical Chopped Blanking signal, the Horizontal Chopped Blanking and the Z-Axis Inhibit signal enables or disables this stage to control all output current. Quiescently, the level at pins 6 and 7 is HI so that the intensity current from pins 1, 2, 9, and 16 can pass to the output. However, both pins 6 and 7 go LO during Vertical Chopped Blanking, during Horizontal Chopped Blanking or during a readout display. This blocks the output

current and the crt is blanked. The Vertical Chopped Blanking signal is connected to pins 6 and 7 of U4485 directly from pin 4 of U4320. The Horizontal Chopped Blanking Inhibit signal is connected to U4485 from pin 4 of U4340 through LR4338, Q4336 and CR4471. Notice that this signal is connected to the collector of Q4336. This transistor is normally operating in the saturated condition, and the HI Horizontal Chopped Blanking Inhibit level from U4340 is the collector source voltage. When the Horizontal Chopped Blanking Inhibit level goes LO, the current through Q4336 drops producing a corresponding LO level at its emitter. This level is connected to pins 6 and 7 of U4485 through CR4471.

Transistor Q4336 also controls the levels at pins 6 and 7 for readout displays. The Z-Axis Inhibit from the Readout System is connected to the base of Q4336 through VR4334 and R4335. This level is normally HI, so Q4336 operates as controlled by the Horizontal Chopped Blanking Inhibit level at its collector. When a readout display is to be presented, the Z-Axis Inhibit level drops LO and is coupled to the base of Q4336 through VR4334. Transistor Q4336 is then reverse biased producing a LO level at its emitter. This level is coupled to pins 6 and 7 of U4485 through CR4471 to block the Z-Axis Logic output current during the readout display. (The intensity of the readout display is determined by a separate Readout intensity level connected directly to the Z-Axis Amplifier; see CRT Circuit description.) Diode CR4472 clamps the emitter of Q4336 at about -0.6 volt when the transistor is off.

The A INTENSITY control sets the output current level when the A Gate at pin 14 is HI and the Display B Command connected to pin 15 through Q4488 and Q4492 is LO. The A Intensity current is blocked whenever the A Gate level goes LO indicating that the A sweep is complete or the Display B Command goes HI indicating that the B sweep is being displayed. The current from the A INTENSITY control is connected to pin 16 through R4482.

In the delayed mode, current is added to the A INTENSITY current during the A-sweep time to intensify a portion of the trace. This intensified portion is coincident with the B-sweep time providing an indication of which portion of the A sweep is displayed in the delayed mode. The A Intensified current is supplied to pin 2 of U4485 from the A INTENSITY control through R4481. With this configuration, the intensified current increases as the A INTENSITY control setting is advanced to provide a proportional intensity increase in the intensified zone as the overall A-sweep intensity increases. Therefore, the intensified zone is more readily visible at high intensity levels. A front-panel screwdriver adjustment (B CONTRAST, R2015) allows for optimum contrast between the intensified portion and the overall sweep. The intensified current is added to the A INTENSITY current to produce an intensified zone on the A sweep under the following conditions: HI A Gate level at pin 14, LO Display B Command at pin 15, HI B Gate level at pin 4, and HI Delay Mode Control Out level at pin 5.

The B INTENSITY control determines the output current when the B Gate level at pin 4 and the Display B Command at pin 15 are both HI. The current from the B INTENSITY control is connected to the Z-Axis Logic stage through R4483.

The current level established by the intensity controls can be altered by the Auxiliary Z-Axis current level at pin 9. The current at this pin can come from the Z-AXIS INPUT connector on the rear panel (see diagram 3) or from any of the plug-in compartments. This current either increases or decreases (depending on polarity) the output current to modulate the intensity of the display. Input from the Z-AXIS INPUT connector allows the trace to be modulated by external signals. The Auxiliary Z-Axis inputs from the plug-in compartments allow special-purpose plug-in units to modulate the display intensity. Diodes CR4473 and CR4474 limit the maximum voltage change at pin 9 to about + and -0.6 volt to protect the Z-Axis Logic stage if an excessive voltage is applied to the Z AXIS INPUT connector. Table 3-6 shows Input/Output combinations of the Z-Axis Logic stage.

HORIZONTAL BINARY

The Horizontal Binary stage develops the Display B Command to determine which horizontal plug-in unit provides the sweep displayed on the crt. When the level is HI, the B horizontal unit is displayed; when it is LO, the A horizontal unit is displayed.

The Display B Command is used in the following stages within the Logic circuit: Horizontal Logic (A and B Sweep Inhibit), Z-Axis Logic, Vertical Binary, and Trace Separation. In addition, it is connected to the following circuits elsewhere in the instrument to indicate which horizontal unit is to be displayed: Main Interface (A and B HORIZ plug-in compartments), Horizontal Interface (for horizontal channel selection).

The levels on pins 3, 4, 7, and 10 of U4358 are determined by the HORIZONTAL MODE switch (see diagram 2) which indicates which horizontal mode has been selected by providing a HI output level on only one of four output lines. The remaining lines are LO.

The Horizontal Binary stage operates as follows for each 4 positions of the HORIZONTAL MODE switch (refer to Table 3-7 for input/output conditions):

1. A MODE. By setting the HORIZONTAL MODE switch to A, the Display B Command is LO indicating to all circuits that the A horizontal unit is to be displayed.

2. B MODE. Selecting the B horizontal mode provides a HI Display B Command to all circuits.

3. CHOP MODE. In the CHOP position of the HORIZONTAL MODE switch, the Display B Command switches between the HI and LO levels to produce a display that switches between the A and B horizontal

TABLE 3-6
Input/Output Combinations for the Z-Axis Logic Stage

A INTENSITY 16	B INTENSITY 1	INTENSIFIED 2	A GATE 14	B GATE 4	DELAY MODE CONTROL 5	DISPLAY B COMMAND 15	Z-AXIS SIGNAL 8	SOURCE OF Z-AXIS SIGNAL
VAR	Φ	Φ	HI	Φ	LO	LO	VAR	A INTENSITY
VAR	Φ	Φ	HI	LO	HI	LO	VAR	A INTENSITY
VAR	Φ	VAR	HI	HI	HI	LO	VAR	A INTENSITY PLUS INTENSIFIED
Φ	VAR	Φ	Φ	HI	Φ	HI	VAR	B INTENSITY
OTHER COMBINATIONS							LO	NO OUTPUT

HI = MAX VOLTAGE OR CURRENT
LO = MIN VOLTAGE OR CURRENT
VAR = VARIABLE CURRENT, 0 to 4 mA
Φ = HAS NO EFFECT

TABLE 3-7
Input/Output Combinations of the Horizontal Binary Stage

	INPUT						OUTPUT
HORIZONTAL CHOPPED BLANKING 1	A MODE 3	B MODE 4	B MODE 7	ALTERNATE PULSE 8	CHOP MODE (HORIZ) 10	DISPLAY B COMMAND 6	HORIZONTAL DISPLAY
Φ	HI	LO	LO	Φ	LO	LO	A HORIZONTAL UNIT
Φ	LO	HI	HI	Φ	LO	HI	B HORIZONTAL UNIT
LO[1]	LO	LO	LO	Φ	HI	n+1[2]	CHOP BETWEEN A AND B
Φ	LO	LO	LO	LO[1]	LO	n+1[3]	ALTERNATE BETWEEN A AND B

Φ = Has no effect in this case.
n+1 = If output is LO prior to LO[1], it goes HI, and vice versa.
[1]Actuated by negative-going edge.
[2]Repetition rate one-half horizontal chopped blanking rate.
[3]Repetition rate one-half alternate pulse rate.

units at a 0.2-megahertz rate. The repetition rate of the Display B Command in this mode is determined by the Horizontal Chopped Blanking pulse (see Chop Counter description). Each time the Horizontal Chopped Blanking pulse at pin 1 drops LO, the output at pin 6 switches to the opposite state.

4. ALT MODE. For ALT horizontal operation, the Display B Command switches to the opposite state each time the negative portion of the Alternate Pulse is received from the Horizontal Logic stage. Repetition rate of the Display B Command in this mode is one-half the repetition rate of the Alternate Pulse applied to pin 8.

VERTICAL BINARY

The Vertical Binary stage produces the Vertical Alternate Command, at pin 6 to determine which vertical unit is to be displayed when the VERTICAL MODE switch is set for ALT. When this output level is HI, the RIGHT VERT unit is displayed; when it is LO, the LEFT VERT unit is displayed. In the ALT or CHOP positions of the HORIZONTAL MODE switch (non-delayed operation only), the output of this stage is slaved to the output of the Horizontal Binary stage so that the Vertical Alternate Command is always HI when the Display B Command is LO, and vice versa. This action allows independent-pairs operation (sweep-slaving) in the ALT position of the VERTICAL MODE switch and the ALT or CHOP positions of the HORIZONTAL MODE switch, whereby the LEFT VERT unit is always displayed at the sweep rate of the B time-base and the RIGHT VERT unit is displayed at the sweep rate of the A time-base. Thus, independent-pairs operation can simulate dual-beam operation for repetitive sweeps.

When the A time-base unit is set to the delaying mode, the repetition rate of the Vertical Alternate command is one-half the repetition rate of the Display B Command. This results in each vertical unit being displayed first against the A time-base unit (delaying), then the B time-base unit (delayed), before the display is switched to the other vertical unit.

The Vertical Alternate Command is used in the Plug-In Binary and Vertical Mode Logic stages. The Vertical Binary stage (U4368) uses the same type of IC as the Horizontal Binary stage. Notice the display B Command level at pin 7. This input is the inverse of the Display B Command level at pin 8 (Q4364 generates the display B Command level). Also, notice the line connected to pin 4 of the Vertical Binary IC U4368. The level at pin 4 Horiz Slave Enable is generated by Q4424 and is HI only when the HORIZONTAL MODE switch is set for ALT or CHOP and the time-base units are in nondelayed operation. The Vertical Binary IC uses the information at pin 4 for correct slaving of the Vertical Alternate Command to the Display B Command (necessary for independent-pairs operation). Horizontal Slave Enable is also used by the trigger select logic.

The operation of the Vertical Binary stage in relation to the modes of operation that can occur is described in the following:

1. A OR B MODE. When the HORIZONTAL MODE switch is set to either A or B the Vertical Alternate Command switches to the opposite state each time an Alternate Pulse is received from the Horizontal Logic stage. Repetition rate of the Vertical Alternate Command in this mode is one-half the repetition rate of the Alternate Pulse. The input conditions for these modes are:

Pin 1 LO-Alternate Pulse generated by Horizontal Logic stage goes negative.

Pin 4 Horizontal Slave Enable LO-HORIZONTAL MODE switch in any position except ALT or CHOP, or the A time-base unit is set for delayed sweep.

Pin 10 HI-HORIZONTAL MODE switch set to A or B.

2. ALT OR CHOP MODE (HORIZ): NONDELAYED. In the ALT or CHOP positions of the HORIZONTAL MODE switch, the output level at pin 6 is the same as the Display B Command level at pin 7. The Display B Command level is produced by inverting the Display B Command from the Horizontal Binary stage. Therefore, the repetition rate of the output signal is the same as the Display B Command. With the VERTICAL MODE switch set to ALT and the A time-base unit set for nondelayed operation, the result is that the RIGHT VERT unit is always displayed at the sweep rate of the A time-base unit, and the LEFT VERT unit is always displayed at the sweep rate of the B time-base unit (independent-pairs operation or sweep slaving). The input conditions to provide a HI output level so that the RIGHT VERT unit can be displayed at the A sweep rate are:

Pin 4 Horizontal Slave Enable HI-HORIZONTAL MODE switch set to ALT or CHOP with nondelayed sweep.

Pin 7 HI-The A sweep is to be displayed (Display B Command LO).

Pin 10 LO-HORIZONTAL MODE switch set to any position except A or B.

The input conditions to provide a LO output level so that the LEFT VERT unit can be displayed at the B-sweep rate are:

Pin 4 Horizontal Slave Enable HI-HORIZONTAL MODE switch set to ALT or CHOP with nondelayed sweep.

Pin 7 LO-The B sweep is to be displayed (Display B Command HI).

Pin 10 LO-HORIZONTAL MODE switch set to any position except A or B.

3. ALT OR CHOP MODE (HORIZ): DELAYED. If the A time-base unit is set to the delayed mode when the HORIZONTAL MODE switch is set to either ALT or CHOP, the operation of the stage is changed from that discussed above. Now, the Vertical Alternate Command switches between the HI and LO states at a rate that is one-half the repetition rate of the Display B Command. The resultant crt display in the ALT position of the VERTICAL MODE switch allows the RIGHT VERT unit to be displayed first against the A sweep (delaying) and then against the B sweep (delayed). Then the display switches to the LEFT VERT unit and is displayed consecutively against the A and B sweeps in the same manner. The input conditions for this mode of operation are:

Pin 4 Horizontal Slave Enable LO-The A time-base unit set for delayed operation.

Pin 8 HI or LO-Vertical Alternate Command changes state at HI to LO transition of Display B Command.

Pin 10 LO-HORIZONTAL MODE switch set to any position except A or B.

Table 3-8 shows the input/output combinations for the Vertical Binary stage.

PLUG-IN BINARY

The Plug-In Binary stage produces the Plug-in Alternate Command to alternate dual-trace units. The Plug-In Binary stage, U4412 uses the same type of integrated circuit as the Horizontal Binary and Vertical Binary stages.

When the Plug-In Alternate Command level is HI and the plug-in unit is set for alternate operation, Channel 2 of the dual-trace unit is displayed. When it is LO, Channel 1 is displayed. The repetition rate of the Plug-In Alternate Command is determined by the setting of the VERTICAL MODE switch. For all positions of the VERTICAL MODE switch except ALT, the Plug-In Alternate Command is the same as the Vertical Alternate Command at pin 6 of U4368 (Vertical Binary stage). Since Vertical Alternate Command is derived directly from the Display B Command, this allows the two channels of a dual-trace vertical unit to be slaved to the time-base units (non-delayed, dual-sweep horizontal modes only) in the same manner as previously described for independent-pairs operation between the vertical and time-base units. The resultant crt presentation, when the dual-trace unit is set for alternate operation, displays the Channel 1 trace at the sweep rate of the B time-base unit and the Channel 2 trace at the sweep rate of the A time-base unit.

The Plug-In Alternate Command switches from HI to LO as the Display B Command from the Horizontal Binary stage switches from LO to HI, and vice versa.

When the VERTICAL MODE switch is set to ALT, pin 6 of the Vertical Binary stage switches the vertical display between the two vertical units. However, if either of the vertical plug-in units are dual-trace units, they can be operated in the alternate mode also. To provide a switching command to these units, the Plug-In Binary stage produces an output signal with a repetition rate that is one-half the repetition rate of the signal at pin 6 of U4368. The sequence of operation, when two dual-trace vertical units are installed in the vertical plug-in compartments and they are both set for alternate operation, is as follows (VERTICAL MODE and HORIZONTAL MODE switches set to ALT): 1. Channel 1 of LEFT VERT unit at sweep rate of B time-base unit; 2. Channel 1 of RIGHT VERT unit at sweep rate of A time-base unit; 3. Channel 2 of LEFT VERT unit at sweep rate of B time-base unit; 4. Channel 2 of RIGHT VERT unit at sweep rate of A time-base unit. Notice that under these conditions, both channels of the LEFT VERT unit are displayed at the B-sweep rate and that both channels of the RIGHT VERT unit are displayed at the A-sweep rate. Input conditions when the VERTICAL MODE switch is set at ALT are:

Pin 4 LO-VERTICAL MODE switch set to ALT.

TABLE 3-8
Input/Output Combinations for the Vertical Binary Stage

INPUT						OUTPUT	
ALTERNATE PULSE	HORIZ SLAVE ENABLE	DISPLAY B COMMAND	DISPLAY B COMMAND	A OR B MODE	VERTICAL ALTERNATE COMMAND		
1	4	7	8	10	6	HORIZONTAL MODE SWITCH	
LO[1]	LO	Φ	Φ	HI	n+1[2]	A OR B	
Φ	HI	HI	LO	LO	HI	DISPLAY RIGHT	ALT OR CHOP, NON-DELAYED MODE (SWEEP-SLAVING)
Φ	HI	LO	HI	LO	LO	DISPLAY LEFT	
Φ	LO	Φ	LO[1]	LO	n+1[3]	ALT OR CHOP, DELAYED MODE	

Φ = Has no effect in this case.

n+1 = If output is LO prior to LO[1] it goes HI, and vice versa.

[1]Actuated by negative-going edge.

[2]Repetition rate one-half alternate pulse rate.

[3]Repetition rate one-half display B rate.

Pin 8 HI or LO-Plug-In Alternate Command signal changes state at HI to LO transition of the Vertical Alternate Command signal.

Table 3-9 gives the input/output combinations for the Plug-In Binary stage.

VERTICAL CHOPPED BLANKING

Part of integrated circuit U4320 along with the external components shown in Figure 3-3 make up the clock generator stage. Component parts R1, Q1, Q2, and Q3 represent an equivalent circuit within U4320. This circuit along with discrete components C4314-R4312-R4313-R4314 compose a two-megahertz free-running oscillator to provide a timing (clock) signal used to synchronize the vertical, horizontal, and plug-in chopping modes.

This stage operates as follows: Assume that Q2 is conducting and Q1 is off. The collector current of Q2 produces a voltage drop across R1 to turn off Q1. This negative level at the collector of Q2 is also connected to pin 14 through Q3 (see waveforms in Fig. 3-3B at time T_0). Since there is no current through Q1, C4314 begins to charge towards -15 volts through R4312-R4313. The emitter of Q1 goes negative as C4314 charges, until it reaches a level about 0.6 volts more negative than the level at its base. Then Q1 is forward biased and its emitter rapidly rises positive (see Time T_1 on waveforms). Since C4314 cannot change its charge instantaneously, the sudden change in voltage at the emitter of Q1 pulls the emitter of Q2 positive. With Q2 reverse biased, its collector rises positive to produce a positive output level at pin 14.

Now, conditions are reversed. Since Q2 is reverse biased, there is no current through it. Therefore, C4314 can begin to discharge through R4314. The emitter level of Q2 follows the discharge of C4314, until it reaches a level of about 0.6 volt more negative than its base. Then Q2 is forward biased and its collector drops negative to reverse-bias Q1. The level at pin 14 drops negative also, to complete the cycle. Once again, C4314 begins to charge through R4312-R4313 to start the second cycle. Two outputs are provided from this oscillator. The Delay Ramp signal from the junction of R4312-R4313 is connected to the Vertical Chopped Blanking stage. This signal has the same waveshape as shown by the waveform at pin 13; its slope is determined by the divider ratio between R4312-R4313. A wide pulse train output is provided at pin 14. The frequency of this pulse train is determined by the overall RC relationship between C4314-R4312-R4313-R4314 and its duty cycle is determined by the ratio of R4312 and R4313 to R4314.

The pulse train at pin 14 is connected to pin 16 through C4315. Capacitor C4315, along with the internal resistance of U4320, differentiates the pulse train at pin 14 to produce a narrow negative-going pulse coincident with the falling edge of the pulse train (positive-going pulse coincident with rising edge has no effect on circuit operation). This negative-going pulse is connected to pin 15 through an inverter-shaper circuit that is also part of U4320. The output at pin 15 is a positive-going clock pulse with a repetition rate of about two megahertz.

The Vertical Chopped Blanking stage is made up of the remainder of U4320. This stage determines if Vertical Chopped Blanking pulses are required, based upon the

TABLE 3-9
Input/Output Combinations for the Plug-In Binary Stage

INPUT				OUTPUT	
ALT MODE INHIBIT (VERT)	VERTICAL ALTERNATE COMMAND	VERTICAL ALTERNATE COMMAND	PLUG-IN ALTERNATE COMMAND		
4	7	8	6	COMMENTS	
LO	Φ	LO[1]	n+1[2]	ALT VERTICAL MODE	
HI	LO	Φ	LO	CHANNEL 1 DISPLAYED	ALL VERTICAL MODES EXCEPT ALT PROVIDE SWEEP-SLAVING FOR NON-DELAYED DUAL-SWEEP OPERATION.
HI	HI	Φ	HI	CHANNEL 2 DISPLAYED	

Φ = Has no effect in this case.

n+1 = If output is LO prior to LO[1] it goes HI, and vice versa.

[1]Actuated by negative-going edge.

[2]Repetition rate one-half Vertical Alternate Command rate.

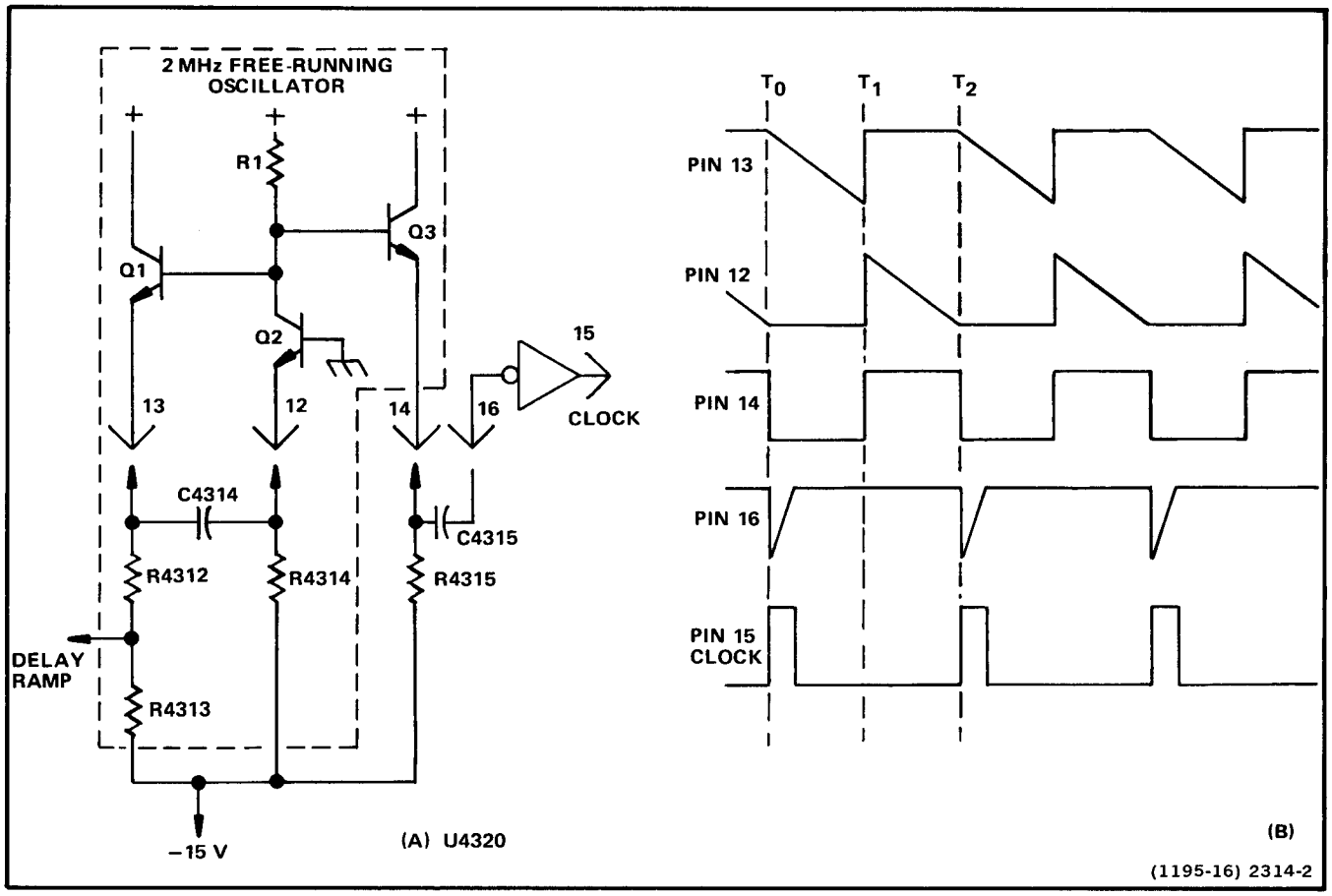

Figure 3-3. (A) Diagram of clock generator stage; (B) Idealized waveforms for clock generator stage.

operating mode of the vertical system or the plug-in units (dual-trace units only). Vertical Chopped Blanking pulses are produced if: 1. VERTICAL MODE switch is set to CHOP; 2. Dual-trace vertical unit is operating in the chopped mode and that unit is being displayed. The repetition rate of the negative-going Vertical Chopped Blanking pulse output at pin 4 is two megahertz for all of the above conditions as determined by the clock generator stage. Table 3-10 shows the input/output combinations for the Vertical Chopped Blanking stage.

The delay ramp signal from the clock generator stage determines the repetition rate and pulse width of the Vertical Chopped Blanking pulses. The delay ramp from pin 13 (U4320) applied to pin 10 starts to go negative from a level of about +1.1 volts coincident with the leading edge of the clock pulse (see waveforms in Fig. 3-4). This results in a HI quiescent condition for the Vertical Chopped Blanking pulse. The slope of the negative-going delay ramp is determined by the clock generator stage. As it reaches a level slightly negative from ground, the Vertical Chopped Blanking pulse output level changes to the LO state and remains LO until the delay ramp goes HI again.

Notice the delay between the leading edge of the clock pulse generated by U4320, and the leading edge of the Vertical Chopped Blanking pulses. The amount of delay between the leading edges of these pulses is determined by the delay ramp applied to pin 10. This delay is necessary due to the delay line in the vertical deflection system. Otherwise, the trace blanking resulting from the Vertical Chopped Blanking pulse would not coincide with the switching between the displayed traces. The duty cycle of the wide pulse train produced in the clock generator stage determines the pulse width of the Vertical Chopped Blanking pulses.

CHOP COUNTER

The Chop Counter stage U4340 produces the Vertical Chopped signal, the Plug-In Chop Command, and the Horizontal Chopped Blanking signal. The clock pulse produced by the clock generator stage provides the timing signal for this stage. The functions of the input and output pins for the Chop Counter IC, U4340, are identified in Figure 3-5A. Idealized waveforms showing the timing relationship between the input and output signals for this stage are shown in Figure 3-5B.

TABLE 3-10
Input/Output Combinations for the Vertical Chopped Blanking Stage

INPUT						OUTPUT	
CHOP MODE (VERT) 3	LEFT PLUG-IN MODE (CHOP INHIBIT) 5	DISPLAY RIGHT COMMAND 6	ADD MODE (VERT) 7	RIGHT PLUG-IN MODE (CHOP INHIBIT) 8	DELAY RAMP 10[1]	VERTICAL CHOPPED BLANKING 4[2]	CONDITIONS
HI	Φ	Φ	LO	Φ	LO	LO	CHOP MODE (VERT)
LO	LO	LO	LO	Φ	LO	LO	LEFT PLUG-IN CHOPPED
LO	Φ	HI	LO	LO	LO	LO	RIGHT PLUG-IN CHOPPED
LO	LO[3]	LO	HI	LO[3]	LO	LO	ADD MODE, LEFT OR RIGHT PLUG-IN CHOPPED
ALL OTHER COMBINATIONS						HI	NO VERTICAL CHOPPED BLANKING PULSES AT OUTPUT

Φ = Has no effect in this case.

[1]Ramp signal; considered LO when more negative than about zero volts.

[2]Negative-going pulse at two megahertz rate.

[3]Pin 5 can be HI and not affect operation if pin 8 is LO, and vice versa.

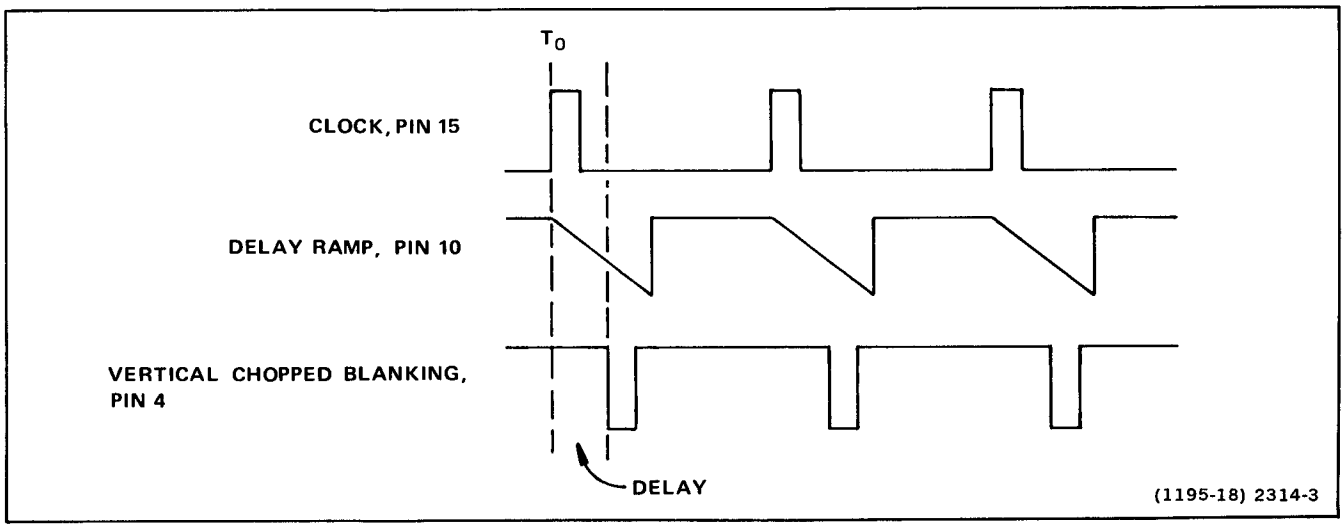

Figure 3-4. Idealized waveforms for the Vertical Chopped Blanking IC (U4320).

The repetition rate of the output signals from this stage is determined by the setting of the HORIZONTAL MODE switch. When the HORIZONTAL MODE switch is set to any position except CHOP, the repetition rate of the Vertical Chopping Signal output at pin 1 is one megahertz (one-half clock rate). This determines the switching between the LEFT and RIGHT VERT units when the VERTICAL MODE switch is set to CHOP. At the same time, the repetition rate of the Plug-In Chop Command at pin 8 is 0.5 megahertz (one-fourth clock rate). This provides a chopping signal to dual-trace vertical units to provide switching between the two channels. The relationship between these output signals and the clock input is shown by the waveforms in Figure 3-5B in the area between T_0 and T_1. During this time, the Horizontal Chopped Blanking at pin 4 remains HI.

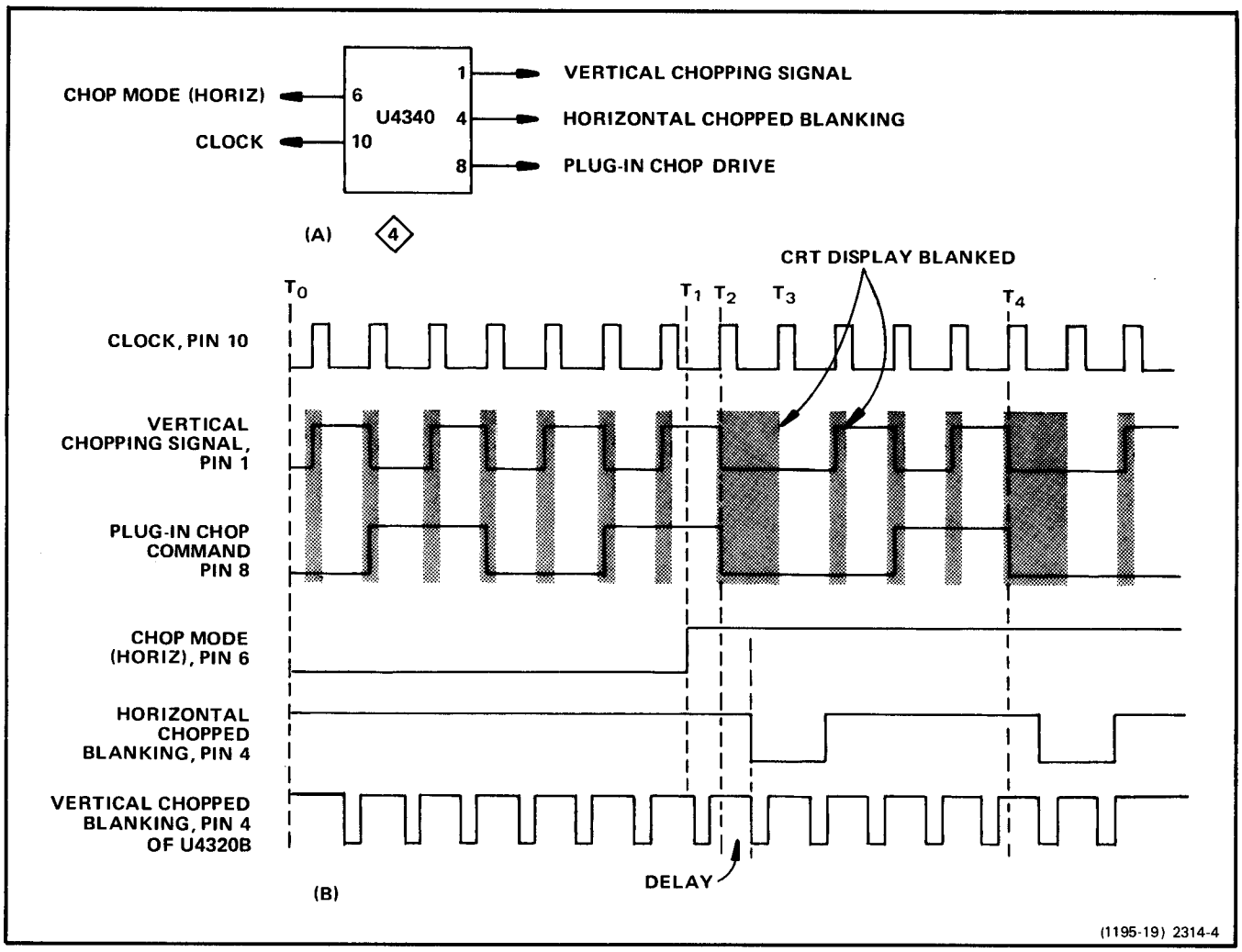

Figure 3-5. (A) Input and output pins for Chop Counter IC, U4340; (B) Idealized waveforms for Chop Counter stage.

When the HORIZONTAL MODE switch is set to CHOP, the basic repetition rate of the Vertical Chopping Signal and the Plug-In Chop Command is altered. For example, if the HORIZONTAL MODE switch is changed to the CHOP position at time T_1 (see Fig. 3-5B), a HI level is applied to pin 6. This stage continues to produce outputs at pins 1 and 8 in the normal manner until both outputs are at their HI level. (See time T_2; this condition only occurs once every fifth clock pulse and only when the HORIZONTAL MODE switch is set to CHOP.) When both of these outputs are at their HI level, the next clock pulse switches both outputs LO, and at the same time switches the Horizontal Chopped Blanking to the LO level.

This change at time T_2 does not appear at pin 4 immediately, due to a delay network in the circuit. The delay is necessary to make the Horizontal Chopped Blanking coincide with the Vertical Chopped Blanking produced by U4320 and the switching between the displayed signals. (Compare bottom two waveforms of Fig. 3-5B; also see Vertical Chopped Blanking for further information.) After the delay time, the output level at pin 4 goes LO where it remains for about 0.5 microsecond which is equal to the period of the clock pulse (two-megahertz repetition rate).

The Horizontal Chopped Blanking time must be longer than the Vertical Chopped Blanking time, since it takes more time for the display to switch between horizontal units than between vertical units. During the time that the level at pin 4 is LO, the crt is blanked and the Vertical Chopping Signal and the Plug-In Chop Command cannot change levels. The clock pulse at T_3 changes only the Horizontal Chopped Blanking output at pin 4. The level on this pin goes HI after the delay time to unblank the crt.

For the next three clock pulses, the Vertical Chopping Signal output and Plug-In Chop Command operate in the normal manner. However, just prior to the fourth clock pulse (time T_4), both outputs are again at their HI level. The fourth clock pulse at T_4 switches the output at pin 1, pin 8, and pin 4 (after delay) to the LO level to start the next cycle. Notice that a Horizontal Chopped Blanking

pulse is produced at pin 4 with every fifth clock pulse. Also notice that with the HORIZONTAL MODE switch set to CHOP, two complete cycles of the Vertical Chopping Signal are produced with each five clock pulses (repetition rate two-fifths clock rate) and one complete cycle of the Plug-In Chop Command for every five clock pulses (one-fifth clock rate). Notice that the large shaded area produced by the Horizontal Chopped Blanking pulse (see Fig. 3-5) is not part of the display time (crt display blanked). However, about the same time segment is displayed from the vertical signal source with or without Horizontal Chopped Blanking, due to the change in repetition rate when in the CHOP horizontal mode.

The Vertical Chopping Signal at pin 1 of U4340 is connected to the Vertical Mode Logic stage (see following description) through LR4342. This signal is HI when the RIGHT VERT unit is to be displayed and it is LO when the LEFT VERT unit is to be displayed. The Plug-In Chop Command at pin 8 is connected to the plug-in units in the vertical compartments through LR4344, via the Main Interface board. When this signal is HI, Channel 2 of the plug-in units can be displayed; when this level is LO, Channel 1 can be displayed. The Horizontal Chopped Blanking signal at pin 4 is connected through LR4338 to the Horizontal Binary stage U4358, and to the Z-Axis Logic stage U4485 by way of Q4336. When this signal is HI, the crt is unblanked to display the selected signal. When it is LO, the crt is blanked to allow switching between the horizontal units.

VERTICAL MODE LOGIC

The Vertical Mode Logic stage is made up of discrete components CR4323-CR4322, CR4369-CR4368 and buffer Q4382-Q4392. These components develop the Display Right Command, which is connected to the Main Interface, Vertical Interface, and Trigger Selector circuits to indicate which vertical unit is to be displayed. When this output level is HI, the RIGHT VERT unit is displayed; when it is LO, the LEFT VERT unit is displayed.

The VERTICAL MODE switch shown on diagram 2 provides control levels to this stage. This switch provides a HI level on only one of five output lines to indicate the selected vertical mode; the remaining lines are LO. Notice that only four of the lines from the VERTICAL MODE switch are connected to the Logic circuit. Operation of this stage is as follows: When the VERTICAL MODE switch is set to RIGHT, a HI level is connected to the base of Q4382 through R4321. This forward biases Q4382, and the positive-going level at its emitter is connected to the emitter of Q4392. The collector of Q4392 goes HI to indicate that the RIGHT VERT unit is to be displayed. For the CHOP position of the VERTICAL MODE switch, a HI level is applied to the anodes of CR4323-CR4322 through R4322. Both diodes are forward biased so that the Vertical Chopping Signal from pin 1 of U4340 can pass to the base of Q4382. This signal switches between the HI and LO levels at a one-megahertz rate and produces a corresponding Display Right Command output at the collector of Q4392. When the Display Right Command is HI, the RIGHT VERT unit is displayed and when it switches to LO, the LEFT VERT unit is displayed.

In the ALT position of the VERTICAL MODE switch, a HI level is applied to the anodes of CR4369-CR4368 through R4369. These diodes are forward biased so the Vertical Alternate Command from pin 6 of the Vertical Binary stage can pass to the base of Q4382 to determine the Vertical Mode Command level. The Vertical Alternate Command switches between its HI and LO levels at a rate determined by the Vertical Binary stage.

The control levels in the LEFT and ADD positions of the VERTICAL MODE switch are not connected to this stage. However, since only the line corresponding to the selected vertical mode can be HI, the RIGHT, CHOP, and ALT lines must remain at their LO level when either LEFT or ADD is selected. Therefore, the base of Q4382 remains LO to produce a LO Display Right Command signal output level at the collector of Q4392.

A logic diagram of the Vertical Mode Logic stage is shown in Figure 3-6. The discrete components that make up each logic function are identified.

TRACE SEPARATION

The Trace Separation stage is made up of discrete components Q4438, Q4442, Q4448, and Q4456. This stage produces the Trace Separation output to the AUX Y-Axis Input of the Vertical Amplifier circuit to offset the B-sweep display when operated in a dual-sweep mode (horizontal). The level of this output current is determined by the setting of the VERT TRACE SEPARATION (B) control. The current from the VERT TRACE SEPARATION (B) control is switched so that the Trace Separation output is provided only when the B sweep is being displayed in the ALT or CHOP horizontal modes and not when the B sweep only is being displayed, nor for independent-pairs operation (sweep-slaving).

The VERT TRACE SEPARATION (B) control provides current to the Trace Separation output through R4456 and Q4456 when Q4456 is forward biased. When the B sweep is being displayed (for ALT or CHOP horizontal operation), the Display B Command at the base of Q4442 is HI. This forward biases Q4442 causing its collector to go negative to forward bias Q4448. This causes Q4448 to saturate and its collector goes positive to forward bias Q4456. During the time the A sweep is being displayed, the Display B Command is LO. This reverse biases Q4442 and Q4448; Q4456 is reverse biased and the VERT TRACE SEPARATION (B) control is disconnected while the A-sweep is being displayed.

When the HORIZONTAL MODE switch is set to B (only), a HI level is connected to the emitter of Q4442 through R4431. This reverse biases Q4442 even though the Display B Command at its base is HI for this mode. Therefore, the VERT TRACE SEPARATION (B) control has no effect. When the VERTICAL MODE switch is set to ALT and the Delay Mode Control level from the A time-base unit is LO (indicating nondelayed sweep operation), a HI level is applied to the emitter of Q4442 through R4438 and CR4434. This HI level reverse biases Q4442 even though the Display B Command is HI. This action disconnects the VERT TRACE SEPARATION (B) control

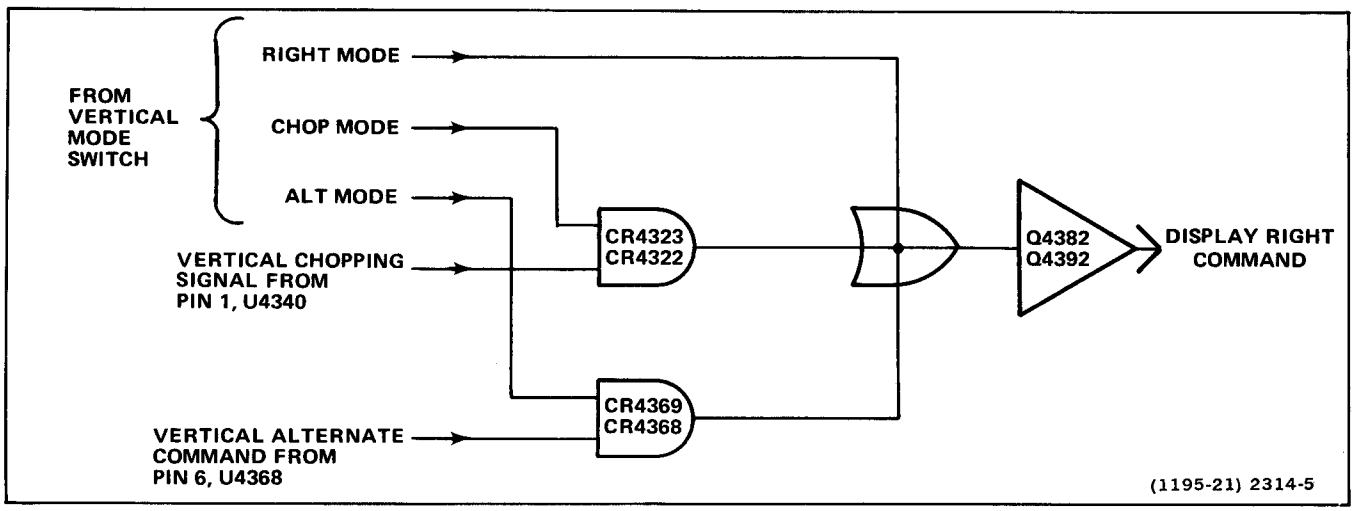

Figure 3-6. Logic diagram of Vertical Mode Logic stage.

for independent-pairs operation so that the vertical position of the B-sweep display is determined by the slaved LEFT VERT plug-in unit only. If delayed-sweep operation is selected, the Delay Mode Control Out level is HI to forward bias Q4438 and Q4443. This allows the VERT TRACE SEPARATION (B) control to position the B-sweep display, since independent-pairs operation is not possible when operating in a delayed-sweep mode.

A logic diagram of the Trace Separation stage is shown in Figure 3-7A. The discrete components which make up each logic function are identified. An input/output table for this stage is given in Figure 3-7B.

MCP (MICROCHANNEL PLATE) INTENSITY TRACKING

The MCP output voltage increases as the A or B INTENSITY controls are rotated past midrange. Tracking is provided by circuitry within U4508. The signal at the collector of Q4494 determines whether A or B INTENSITY control is tracked, if this signal is HI (Q4494 off) the voltage on the bases of transistors A and D of U4508 is -4.3 volts. This voltage is more positive than the voltage on the bases of B and C. Transistors A and D of U4508 are turned on, while transistors C and B of U4508 are turned off. The voltage at pins AS and AR varies from 0 to -10 volts, depending on the setting of the A and B INTENSITY controls. At maximum intensity the voltage is -10 volts. At midrange (-5 volts on pins AS and AR) emitter current stars flowing in transistors D and A of U4508. Current derived from the B INTENSITY control is diverted to ground by transistor A, and current derived from the A INTENSITY control flows through transistor D into the intensity sense line.

With A INTENSITY control set to midrange, current begins to flow in the Intensity Sense line. The current increases to 50 microamperes when the A INTENSITY control is at maximum. On the High Voltage board (diagram 3) the Intensity Sense line is connected to a current summing node (pin 2 of U1714A) where the MCP output voltage increases in proportion to the Intensity Sense current; this causes a maximum voltage increase of 375 volts.

If the signal at the collector of Q4494 is LO the voltage at the bases of transistors B and C (U4508) is -4.3 volt. This voltage is more positive than the base voltage of transistors D and A of U4508. Now, transistors B and C of U4508 are turned on and the Intensity Sense current is derived from the B INTENSITY control.

The signal at the collector of Q4494 is LO when the HORIZONTAL MODE switch is in ALT, CHOP, or B. Therefore, B INTENSITY control provides the MCP output voltage tracking when the HORIZONTAL MODE switch is in ALT, CHOP, or B. The A INTENSITY control provides the tracking voltage when the HORIZONTAL MODE switch is set to A.

TIME-BASE CONTROLLED Z-AXIS FOR X-Y DISPLAYS

X-Y displays can only be obtained in conjunction with a time-base unit. When an amplifier unit is installed in the A (B) HORIZ compartment, the Z-Axis is controlled by the time-base unit in the B (A) HORIZ compartment, independent of the setting of the HORIZONTAL MODE switch. The B (A) indicator lamp automatically turns on; the selection of the horizontal mode by the HORIZONTAL MODE switch is not affected. X-Y displays often consist of a display where a fast switching transient occurs between two stable states. The switching may be such that the display is predominantly in these two stable states. If the Z-Axis was not duty cycled, but turned on permanently this would result in a display with two bright spots and a barely or not at all visible transient,

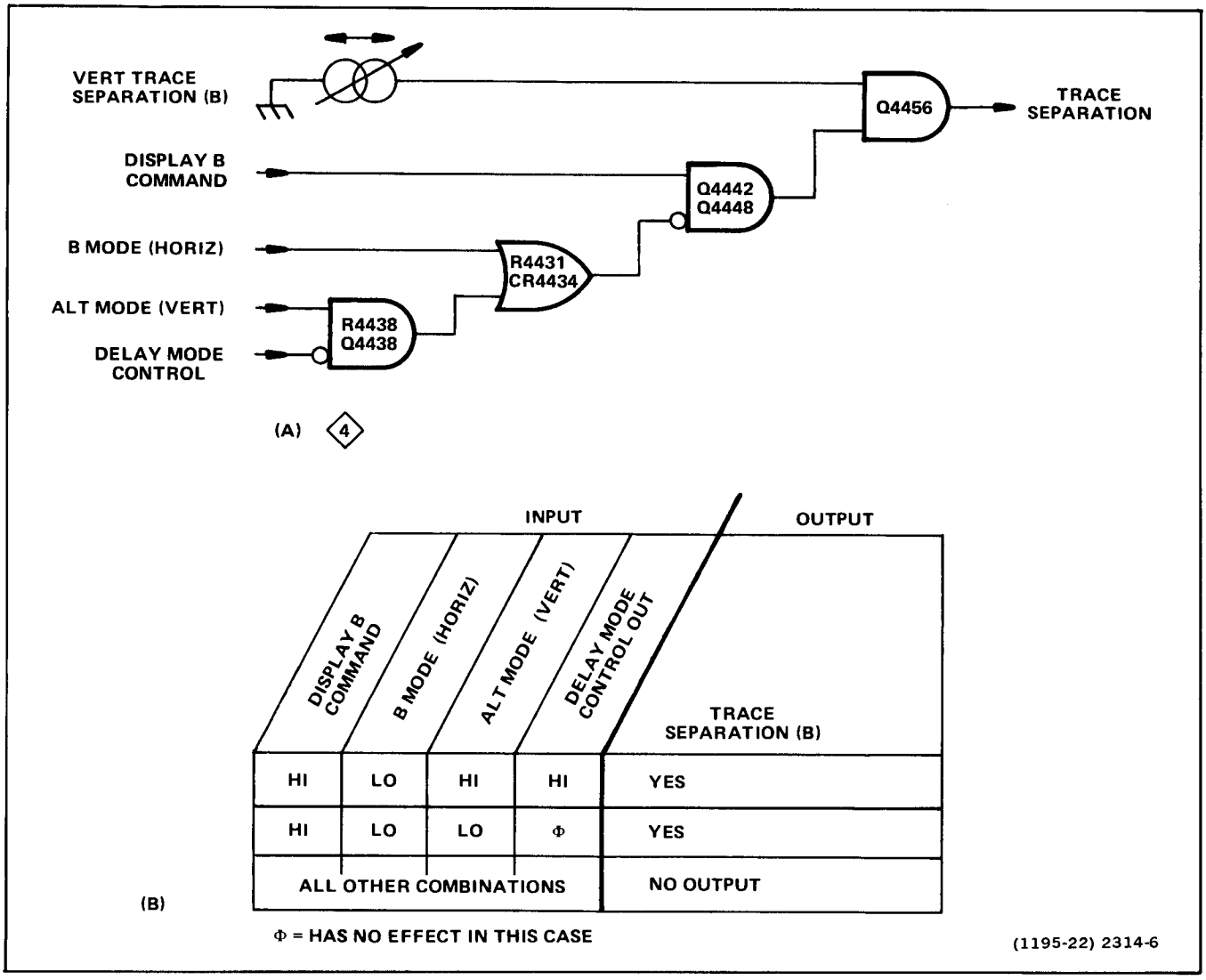

Figure 3-7. (A) Logic diagram of Trace Separation stage; (B) Table of input/output combinations.

since the average screen current associated with these bright spots can be large enough to enable the intensity limiter.

By triggering the time-base unit with the Y-Axis signal, the duty cycle of the Z-Axis can be controlled with the time-base unit time/division control. With the HORIZONTAL MODE switch set to ALT an X-Y display alternating with a Y-T display is obtained. The Z-Axis for both displays is on only during the time that is displayed in the Y-T display. This is a visible aid for optimum control of the Z-Axis duty cycle of X-Y displays. For certain applications of X-Y display, it may be desirable that control of the Z-Axis is determined by the selection of the HORIZONTAL MODE switch. A slide switch located on the Logic board selects how the Z-Axis is controlled during X-Y displays. Normally the switch should be in the IN position such that for X-Y displays the Z-Axis is controlled by a time-base unit.

Without a vertical plug-in unit in a horizontal compartment; diodes CR4487 and CR4495 do not conduct. Q4488 acts as an emitter follower. Resistors R4486 and R4487 perform a dc level shift approximately equal to the emitter-base drop of Q4488. Q4492 is turned off, so the voltage at the collector of Q4492 is a duplicate of the Display B Command. If diode CR4487 is connected to ground by an amplifier unit in the B HORIZ compartment the Display B Command is not applied to the base of Q4488 and the signal at the collector of Q4492 is LO. In this condition the Z-Axis logic IC selects the A INTENSITY input only, independent of other control inputs. If diode CR4495 is connected to ground by an amplifier unit installed in the A HORIZ compartment, Q4492 is saturated. The emitter of Q4488 is held at a HI level, so even when the Display B Command is HI, Q4488 does not conduct. The Z-Axis logic IC selects the B Intensity input when the signal at the collector of Q4492 is HI, regardless of other control inputs.

Transistors Q4494 and Q4498 drive the A and B INTENSITY indicator lights. With an amplifier unit installed in either A or B HORIZ compartments diode CR4496 or CR4493 conducts. This prevents Q4494 and Q4498 from turning on when the HORIZONTAL MODE switch is set to ALT or CHOP.

With an amplifier unit installed in the A HORIZ compartment the signal at the collector of Q4492 is HI, to turn on Q4494 and the B INTENSITY indicator lamp. This indicates that the Z-Axis is controlled by the time-base unit installed in the B HORIZ compartment. The signal at the collector of Q4492A is LO when an amplifier is installed in the B HORIZ compartment. Now, Q4498 is saturated. Base current flows from the +5 V lamp supply, through the B indicator lamp and the resistor R4493 to the base of Q4498. This base current is not sufficient to light the B INTENSITY indicator lamp, so the A INTENSITY indicator lamp is turned on. This indicates that the Z-Axis is controlled by the time-base unit in the A HORIZ compartment.

When time-base units are installed in both A and B horizontal compartments, Q4494 and Q4498 are saturated (with the HORIZONTAL MODE switch in ALT or CHOP). Base current is provided from the +5 V supply on the Mode Switch board, through either the ALT or CHOP switch contacts, and through resistors R4493 and R4496 to the bases of Q4494 and Q4498. Both A and B INTENSITY indicator lights are on.

When the HORIZONTAL MODE switch is set to A or B, the voltage at the collector of Q4492 (which is derived from the Display B Command signal) controls the A and B INTENSITY lights as was previously described.

TRIGGER SELECTOR

The Trigger Selector circuit determines the source of the internal triggering signals connected to the A and B horizontal compartments. A schematic diagram of the Trigger Selector is given on diagram 5, in section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by gray shaded lines separating the circuitry into major stages. These stages aid in locating components mentioned here. Sub-headings in the following discussion use these stage names to further identify portions of the circuitry on diagram 5.

A AND B TRIGGER CHANNEL SWITCHES

The operation of the A and B Trigger Channel Switch stages is similar. Therefore, only a discussion of the A Trigger Channel Switch is given.

Amplifier units installed in the vertical compartments provide a differential trigger signal to the mainframe. These signals are terminated into 50 ohm power dividers. The 50-ohm strip transmission lines carry half of the input signal from the power dividers to the A and B Trigger Selector circuits. The inputs of the channel switches, U232 and U432, have a 50 ohm input impedance and terminate the transmission lines.

A Trigger Channel Switch

Channel switch U232 has two differential inputs and one differential output. Control voltages at pins 1, 2, 11 and 12 determine whether the input signals are terminated within the channel switch or are coupled through to the output. Active components U252A and Q254 keep the output dc common-mode voltage on pin 3 and pin 13 at +3.2 volts for all modes of the channel switch, U232. The dc common-mode voltage is sensed by resistors R237 and R247 and is compared with a +3.2 volt reference set by divider R251 and R252. If resistors R237 and R247 sense a voltage higher than +3.2 volts, the output of U252A goes negative lowering the base voltage on Q254. This reduces the current into pin 13A which causes the dc common-mode voltage at pin 3 and 13 to decrease. The voltage at pin 13A depends on the channel switch mode. When the VERTICAL MODE switch is set to LEFT, RIGHT or ALT the voltage on pin 13A is +3.8 volts. When the VERTICAL MODE switch is set to ADD the voltage on pin 13A is +4.6 volts.

Each channel within U232 has an independent pair of control pins for channel selection. If the "On" pin is more positive than the "Off" pin, that channel is selected. All of the "On" pins are held at +2.0 volts, the "Off" pins are either at +2.5 volts or at a T^2L LO level. The A Trigger Channel Switch has four operating modes: Left, Right, Alt, and Add; in the Left and Right modes the $\overline{\text{Add}}$ logic level is HI (on pin CF) and the Right logic level (on pin CG) is LO for Left and is HI for Right. In the ALT mode, $\overline{\text{Add}}$ is HI and Right alternates between LO and HI. In the ADD mode both $\overline{\text{Add}}$ and Right are LO. (See the discussion on Mode Switching, diagram 2 in this section of the manual).

Zener diodes VR237 and VR247 shift the dc level downward by 9 volts, to set the output of U274 near ground. Diodes VR237 and VR247 are matched for voltage to within 100 mV.

A and B TRIGGER AMPLIFIER

The operation of the A and B Trigger Amplifiers is similar. Therefore, only a discussion of the A Trigger Amplifier is given. Integrated circuit U274 provides final amplification of the trigger signal. Components R261 and R272 are bias resistors for U274. Zener diodes VR237 and VR247 have a 5% voltage tolerance, therefore the dc voltage level at pins 7 and 9 of U274 is -5.8 volts within 0.45 volt. The dc common-mode voltage, with its 0.45 volt uncertainty, is picked off at pin 5 and pin 12 of U274 and applied to the noninverting input of U252B. The output of U252B is 1.2 volts more positive than the input and is used for internal biasing at pin 15 of U274. Resistor R274 determines the gain of U274. The overall voltage gain of the A trigger selector (from the input connectors J202, J203 and J402, J403 to the output J270, J271 into a load of 50 ohm per side) is one. The dc

output level of U274 is zero volts, R235 sets the dc Centering and R279 adjust the DC Common Mode voltage.

Thermal compensation for U232 and U274 is provided by four time constants R240 and C240, C237, R250 and C250, R270, and C270.

The operation of the B trigger selector is similar, except for the signal pickoff of pin 2 and pin 4 of U474 which is used to generate the Vertical Signal Out.

VERTICAL SIGNAL OUTPUT AMPLIFIER

A differential signal is picked off at pin 2 and pin 4 of U474 and is amplified by U492. Before the signal reaches the input of U492 it passes through a compensation circuit consisting of C483, R483, R486, L486, R496, C492 and R493. The characteristic impedance of this circuit is 100 ohms differentially and terminates the 50-ohm strip transmission lines running from the pickoff points, at pin 2 and pin 4 of U474. At pin 2 and pin 4 there is an uncertainty in the dc common-mode level due to the 5% voltage tolerance of zener diodes VR437 and VR447. Integrated circuit U452B passes on this uncertainty for biasing U492. The output signal at J496 is centered at 0 volt by R485. The Vertical Signal Out amplitude is 25 millivolts/division of vertical deflection into a load of 50 ohms, and 0.5 volt/division of vertical deflection into a 1 megohm load. Two time constants R480 and L480, R490 and C490 provide for thermal compensation.

6 READOUT SYSTEM

A schematic diagram of the Readout System is given on diagram 6, in section 8 of this manual (Diagrams and Circuit Board Illustrations). This schematic is divided by gray shaded lines separating the circuitry into major stages. These stages aid in locating components mentioned here. Stage name headings in the following discussion are used to further identify portions of the circuitry on diagram 6.

The Readout System provides an alpha-numeric display of information encoded by the plug-in units. This display is presented on the crt and is written by the crt beam on a time-shared basis with the analog waveform display.

The following terms are used to describe the Readout System:

Character—A single number, letter or symbol displayed on the crt, either alone or in combination with other characters.

Word—A group of related characters. In the Readout System, a word can consist of up to 10 characters.

Frame—A display of all words for a given operating mode and plug-in combination. Up to 8 words can be displayed in one frame. Figure 3-8 shows the position of each word in a complete frame.

Column—One of the vertical lines in the Character Selection Matrix (see Fig. 3-9). Columns C-0 (column zero) through C-10 (column 10) can be addressed by the system.

Row—One of the horizontal lines in the Character Selection matrix. Rows R-1 (row 1) through R-10 (row 10) and R-14 (row 14) can be addressed by the system.

Time-Slot—A location in a pulse train. In the Readout System, the pulse train consists of 10 negative-going pulses. Each time-slot pulse is assigned a number between 1 and 10. For example, the first time-slot is TS-1.

Time-Multiplexing—Transmission of data from two or more sources over a common path by using different time intervals for different signals.

DISPLAY FORMAT

Up to 8 words of readout information can be displayed on the crt. The position of each word is fixed and is directly related to the plug-in unit from which it originated. Figure 3-8 shows the area of the graticule where the readout from each plug-in unit is displayed. Notice that Channel 1 of each plug-in unit is displayed within the top division of the crt and Channel 2 is displayed directly

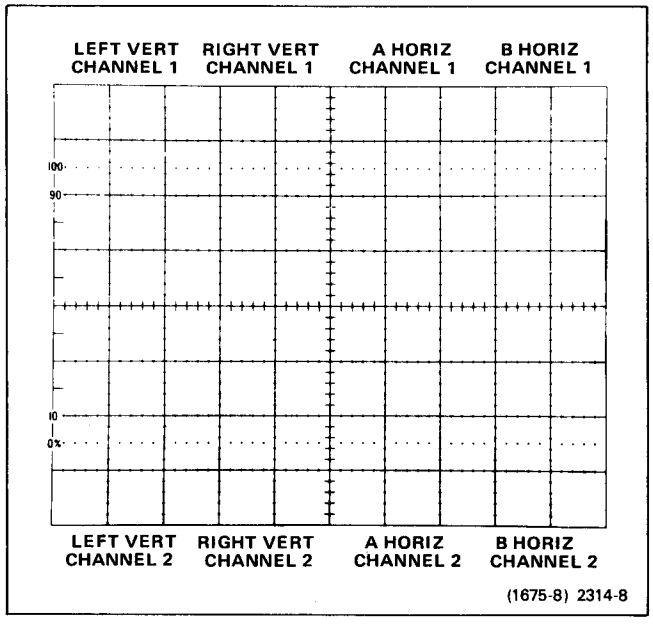

Figure 3-8. Location of readout display on the crt identifying the originating plug-in and channel.

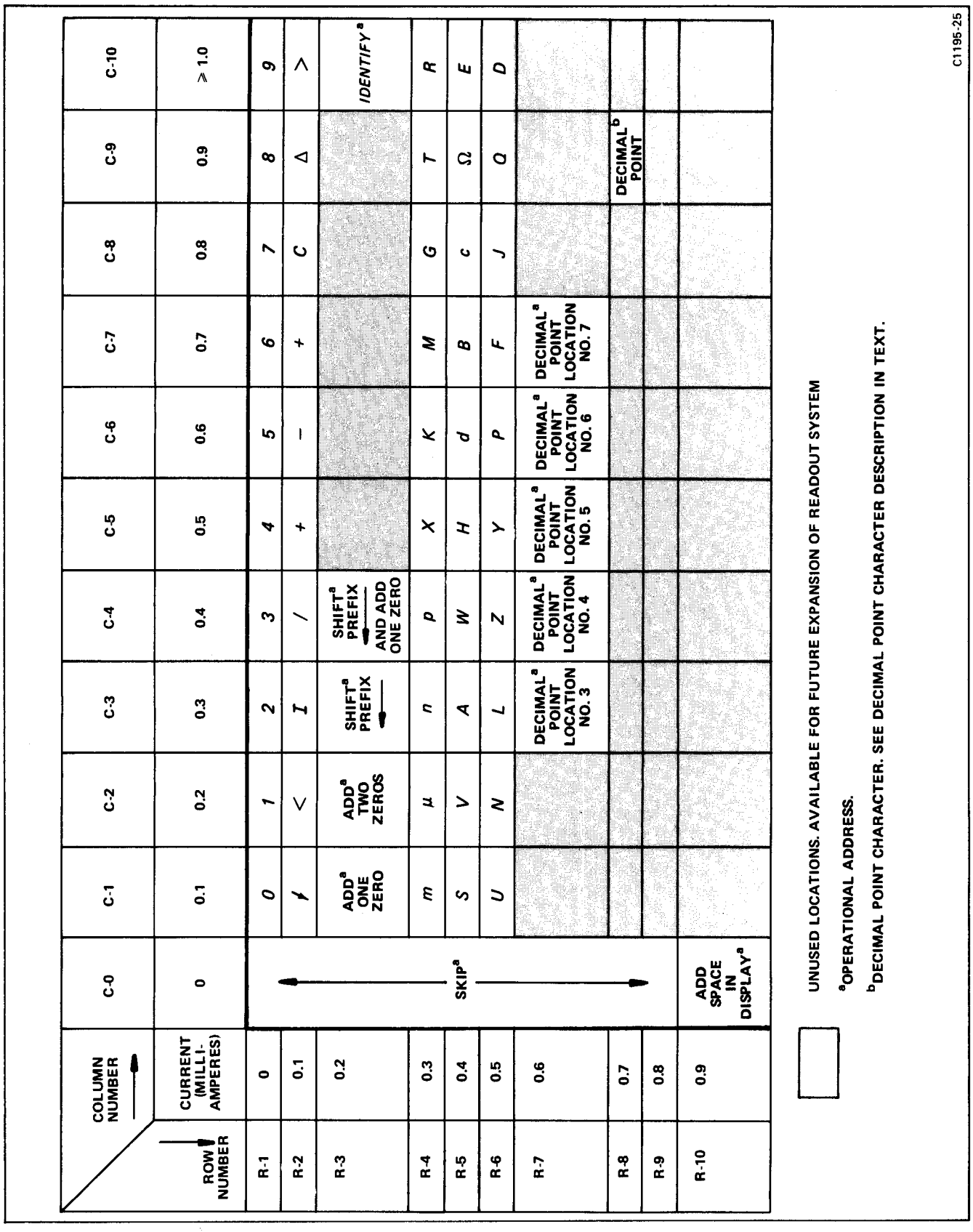

Figure 3-9. Character selection matrix for 7104 Readout System.

below within the bottom division. Figure 3-10 shows a typical display where only Channel 2 of the Right Vertical and B Horizontal units is selected for display.

Each word in the readout display can contain up to 10 characters, although the typical display will contain between 2 and 7 characters per word. The characters are selected from the Character Selection Matrix shown in Figure 3-9. In addition, 12 operational addresses are provided for special instructions to the Readout System. The unused locations in the Matrix (shaded area) are available for future expansion of the Readout System. The method of addressing the locations in the Character Selection Matrix is described in the following discussion.

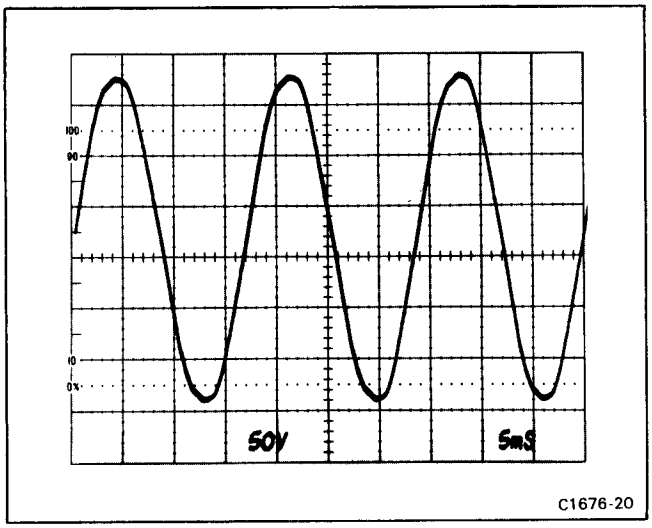

Figure 3-10. Typical readout display where only channel 2 of the Right Vertical and B Horizontal units is displayed.

DEVELOPING THE DISPLAY

This description is intended to relate the basic function of each stage to the operation of the overall Readout System. Detailed information on circuit operation is given later.

The key block in the Readout System is the Timer Stage (see schematic 6). This stage produces the basic signals that establish the timing sequences within the Readout System. The period of the timing signal is about 250 microseconds (drops to about 210 microseconds when Display-Skip is received; see detailed description of Timer stage for further information). This stage also produces control signals for other stages within this circuit and interrupt signals to the Vertical Amplifier, Horizontal Amplifier, and Logic circuits, which allow a readout display to be presented. The Time-Slot Counter stage receives a trapezoidal voltage signal from the Timer stage and directs it to one of ten output lines. These output lines are labeled TS-1 through TS-10 (time-slots 1 through 10) and are connected to the vertical and horizontal plug-in compartments as well as to various stages within the Readout System. The output lines are energized sequentially, so there is a pulse on only one of the 10 lines during any 250 microsecond timing period. After the Time-Slot Counter stage has counted time-slot 10, it produces an End-of-Word pulse which advances the system to the next channel.

Two output lines (row and column) are connected from each channel of the plug-in unit back to the Readout System. Data is typically encoded on these output lines by connecting resistors between them and the time-slot input lines. The resultant output is a sequence of 10 analog current levels that range from 0 to 1 milliampere (100 microamperes/step) on the row and column output lines. This row and column correspond to the row and column of the Character Selection Matrix in Figure 3-9. The standard format for encoding information onto the output lines is given in Table 3-11. (Special-purpose plug-in units may have their own format for readout; these special formats will be defined in the manuals for these units.)

The encoded column and row data from the plug-in units is selected by the Column Data Switch and Row Data Switch stages respectively. These stages take the analog current from the 8 data lines (2 channels from each of the 4 plug-in compartments) and produce a time-multiplexed analog voltage output containing all of the column and row information from the plug-ins. The Column Data Switch and Row Data Switch are

TABLE 3-11
Standard Readout Format

Time-Slot Number	Description
TS-1	Determines Decimal Magnitude (number of zeros displayed or prefix change information) or the IDENTIFY function (no display during this time-slot).
TS-2	Indicates normal or inverted input (no display for normal).
TS-3	Indicates calibrated or uncalibrated condition of plug-in variable control (no display for calibrated condition).
TS-4	Scaling.
TS-5 TS-6 TS-7	Not encoded by plug-in unit. Left blank to allow addition of zeros by Readout System.
TS-8	Defines the prefix which modifies the units of measurement.
TS-9 TS-10	Defines the units of measurement of the plug-in unit. May be standard unit of measurement (V, A, S, etc.) or special units selected from the Character Selection Matrix.

sequenced by the binary Channel Address Code from the Channel Counter.

The time-multiplexed output of the Column Data Switch is monitored by the Display-Skip Generator to determine if it represents valid information that should be displayed. Whenever information is not encoded in a time-slot, the Display-Skip Generator produces an output level to prevent the Timer stage from producing the control signals that normally interrupt the crt display and present a character.

The analog outputs of the Column Data Switch and Row Data Switch are connected to the Column Decoder and Row Decoder stages respectively. These stages sense the magnitude of the analog voltage input and produce an output current on one of ten lines. The outputs of the Column Decoder stage are identified as C-1 through C-10 (column 1 through 10) corresponding to the encoded column information. Likewise, the outputs of the Row Decoder stage are identified as R-1 through R-10 (row 1 through 10) corresponding to the encoded row information. The primary function of the row and column outputs is to select a character from the Character Selection Matrix to be produced by the Character Generator stage. These outputs are also used at other points within the system to indicate when certain information has been encoded. One such stage is the Zeros Logic and Memory. During time-slot 1 (TS-1), this stage checks if zero-adding or prefix-shifting information has been encoded by the plug-in unit, and stores it in the memory until time-slots 5, 6, or 8. After storing this information, it triggers the Display-Skip Generator stage so that there is no display during time-slot 1 (as defined by Standard Readout Format; see Table 3-11). When time-slots 5, 6, and 8 occur, the memory is addressed and any information stored there during time-slot 1 is transferred to the input of the Column Decoder stage to modify the analog data during the applicable time-slot.

Also, the Zeros Logic and Memory stage produces the IDENTIFY function. When time-slot 1 is encoded for IDENTIFY (column 10, row 3), this stage produces an output level, which connects the Column Data Switch and Row Data Switch to a coding network within the Readout System. Then, during time-slots 2 through 9, an analog current output is produced from the Column Data Switch and Row Data Switch, which addresses the correct points in the Character Selection Matrix to display the word "IDENTIFY" on the crt. The Zeros Logic and Memory stage is reset after each word by the Word Trigger pulse.

The Character Generator stages produce the characters which are displayed on the crt. Any of the 50 characters shown on the Character Selection Matrix of Figure 3-9 can be addressed by proper selection of the column and row currents. Only one character is addressable in any one time-slot; a space can be added into the displayed word by the Decimal-Point Logic and Character Position Counter stage when encoded by the plug-in. The latter stage counts the number of characters generated and produces an output current to step the display one character position to the right for each character. In addition, the character position is advanced once during each of time-slots 1, 2, and 3, whether a character is generated during these time-slots or not. This action fixes the starting point of the standard-format display such that the first digit of the scaling factor always starts at the same point within each word regardless of the information encoded in time-slot 1, 2, or 3 preceding this digit. Also, by encoding row 10 and column 0 during any time-slot, a blank space can be added to the display. Decimal points can be added to the display at any time by addressing the appropriate row and column. (See Character Selection Matrix for location of decimal points.) The Decimal-Point Logic and Character Position Counter stage is reset after each word by the Word Trigger pulse.

The Format Generator stage provides the output signals to the vertical and horizontal deflection systems of the instrument to produce the character display. The binary Channel Address Code from the Channel Counter stage is connected to this stage, so that the display from each channel is positioned to the area of the crt associated with the plug-in and channel originating the word (see Fig. 3-8). The positioning current or decimal point location current generated by the Decimal Point Logic and Character Position Counter stage is added to the Horizontal (X) signal at the input to the Format Generator stage to provide horizontal positioning of the characters within each word. The X- and Y-Readout signals are connected to the Horizontal Amplifier and Vertical Amplifier through the X- and Y-Buffer stages.

The Word Trigger stage produces a trigger from the End-of-Word pulse generated by the Time-Slot Counter stage after the tenth time-slot. This Word Trigger pulse advances the Channel Counter to display the information from the next channel or plug-in. It also provides a reset pulse to the Zeros Logic and Memory stage and the Decimal Point Logic and Character Position Counter stage. This Word Trigger stage can also be advanced to jump a complete word or a portion of a word when a Jump Command is received from the Row Data Switch stage.

TIMER

The Timer stage establishes the timing sequence for all circuits within the Readout System. This stage produces 7 time-related output waveforms (see Fig. 3-11). The triangle waveform produced at pin 6 forms the basis for the remaining signals. The basic period of this triangle waveform is about 250 microseconds as controlled by RC network R2135 and C2135. The triangle waveform is clipped and amplified by U2126 to form the trapezoidal output signal at pin 10. The amplitude of this output signal is exactly 15 volts as determined by U2126 (exact amplitude is necessary to accurately encode data in plug-in units; see Encoding the Data). The trigger output at pin 5 provides the switching signal for the Time-Slot Counter and Word Trigger stages.

The signals at pins 12, 13, 14, and 16 are produced only when the triangle waveform is on its negative slope and the trapezoidal waveform has reached the lower level. The timing sequence of these waveforms is important to

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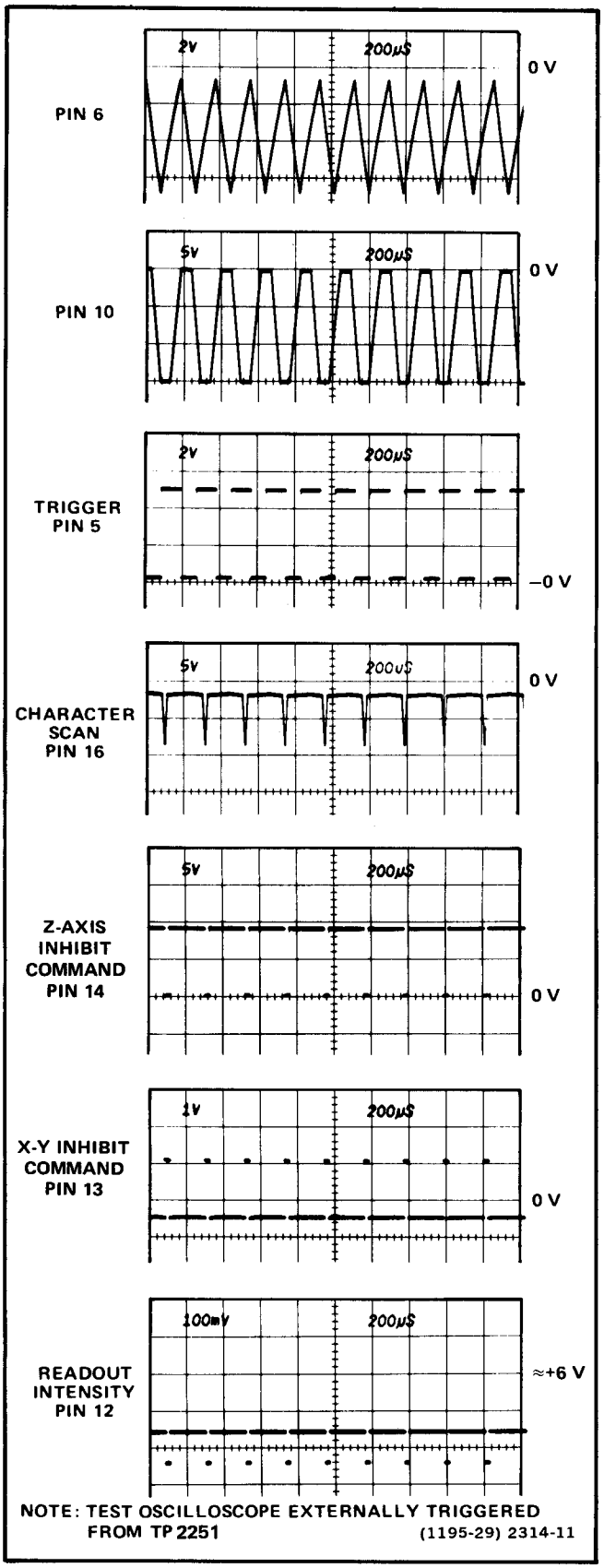


Figure 3-11. Output waveforms of the Timer stage.

the operation of the Readout System (see expanded waveforms in Fig. 3-12). The Z-Axis Inhibit command at pin 14 is produced first. This negative-going signal provides a blanking pulse to the Z-Axis Logic stage (see diagram 4) to blank the crt before the display is switched to the Readout System. It also produces the strobe pulse through Q2138 and CR2142 to signal other stages within the Readout System to begin the sequence necessary to produce a character. The collector level of Q2138 is also connected to Symbol Character Generator U2272 by way of CR2140. This activates U2272 during the quiescent period of the strobe pulse (collector of Q2138 negative) and diverts the output current of Row Decoder U2185 to row 2. The purpose of this configuration is to prevent the Zeros Logic and Memory stage U2232 from storing incorrect data during the quiescent period of the strobe pulse. When the strobe pulse goes positive, CR2140 is reverse biased to disconnect Q2138 from U2272 and allow the Row Decoder to operate in the normal manner.

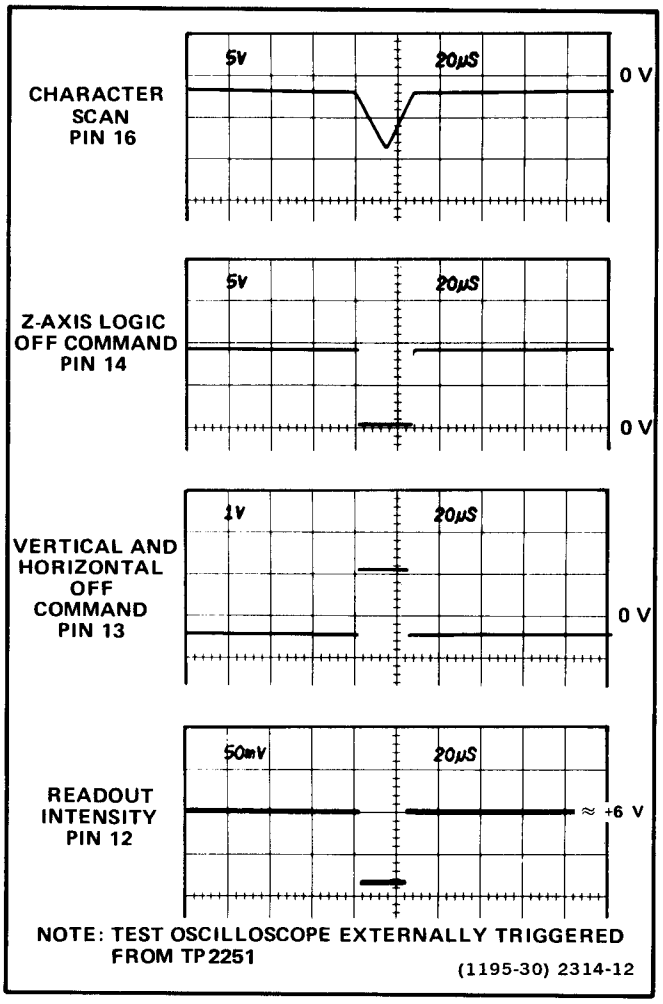


Figure 3-12. Detail of output at pins 12, 13, 14 and 16 of U2126.

The next signal to be produced is the X-Y Inhibit Command at pin 13. This positive-going signal disconnects the plug-in signals from the vertical and horizontal deflection systems. The Ready signal derived from this output is connected to the Decimal Point Logic and Character Position Counter stage and the Format Generator stage.

The Z Readout output at pin 12 is produced next. This current is connected to the crt circuit to unblank the crt to the intensity level determined by the voltage on the Gate Readout Intensity line. The Character Scan ramp at pin 16 started to go negative as this timing sequence began. However, character generation does not start until the readout intensity level has been established. The triangular Character Scan ramp runs from about -2 volts to about -8.5 volts, then returns back to the original level. This waveform provides the scanning signal for the Character Generator stages. Character Scan adjustment, R2128, sets the dc level of the Character Scan ramp for complete characters on the display.

The Timer stage operates in one of two modes as controlled by the Display-Skip level at pin 4. The basic mode just described is a condition that does not occur unless all ten characters of each word (80 characters total) are displayed on the crt. Under typical conditions, only a few characters are displayed in each word. The Display-Skip level at pin 4 determines the period of the Timer output signal. When a character is to be generated, pin 4 is LO and the circuit operates as just described. However, when a character is not to be displayed, a HI level is applied to pin 4 of U2126 through CR2125 from the Display-Skip Generator stage. This signal causes the Timer to shorten its period of operation to about 210 microseconds. The waveforms in Figure 3-13 show the operation of the Timer stage when the Display-Skip condition occurs for all positions in a word. Notice that there is no output at pins 12, 13, 14, and 16 under this condition. This means that the crt display is not interrupted to display characters. Also notice that the triangle waveform at pin 6 does not go as far negative, and that the negative portion of the trapezoidal waveform at pin 10 is shorter. Complete details on operation of the Display-Skip Generator are given later.

The Timer operation is also controlled by the Single-Shot Lockout level at pin 2. If this level is LO, the Timer operates as just described. However, if the Single-Shot Lockout stage sets a HI level at this pin, the Timer stage is locked out and can not produce any output signals (see Single-Shot Lockout description for further information).

A negative voltage on the Readout Intensity line sets the intensity of the readout display independently of the A or B INTENSITY controls. The Readout Intensity line also provides a means of turning the Readout System off when a readout display is not desired. When the Readout Intensity line is left open, the current from pin 11 of U2126 is interrupted, and at the same time, a positive voltage is applied to pin 4 through CR2124. The positive voltage switches the stage to the same conditions as were present under the Display-Skip condition.

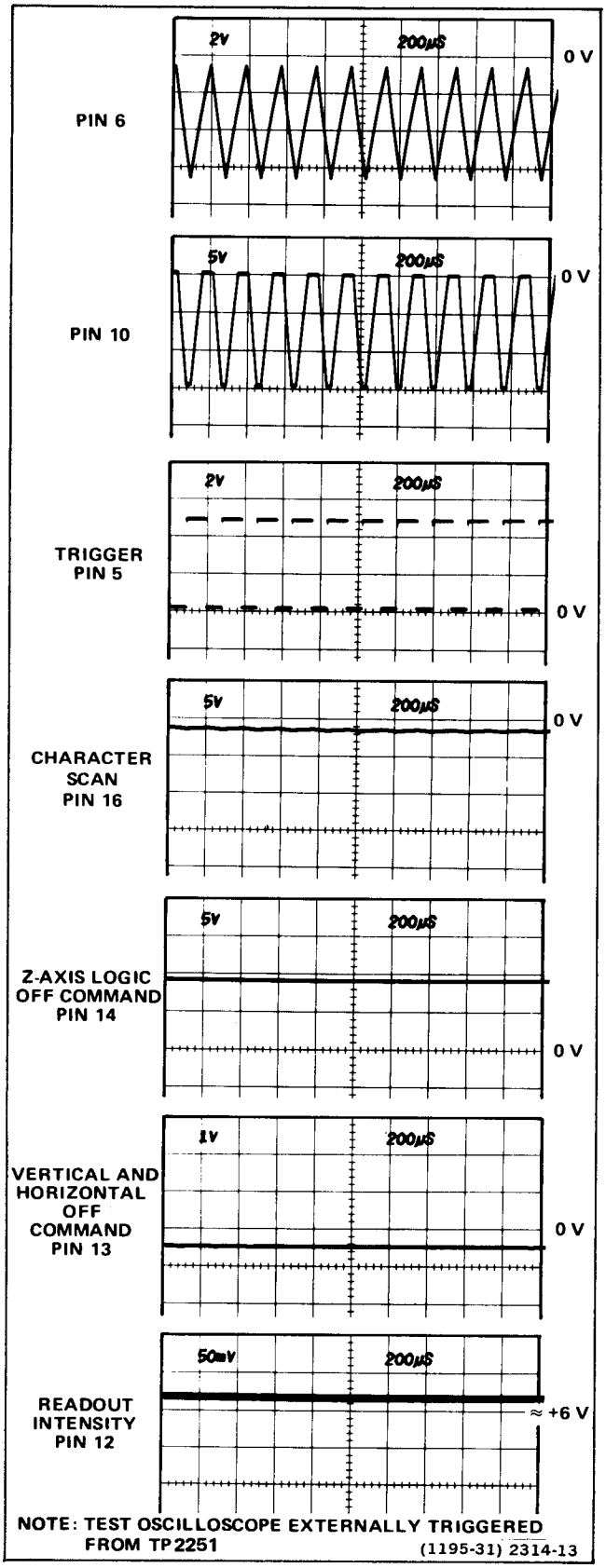


Figure 3-13. Timer stage operation when display-skip condition occurs.

Therefore, the crt display is not interrupted to present characters. However, time-slot pulses continue to be generated.

TIME-SLOT COUNTER

Time-Slot Counter U2159 is a sequential switch which directs the trapezoidal-waveform input at pin 8 to one of its 10 output lines. These time-slot pulses are used to interrogate the plug-in units to obtain data for the Readout System. The trigger pulse at pin 15 switches the Time-Slot Counter to the next output line; the output signal is sequenced consecutively from time-slot 1 through time-slot 10. Figure 3-14 shows the time relationship of the time-slot pulses. Notice that only one line carries a time-slot pulse at any given time. When time-slot 10 is completed, a negative-going end-of-word pulse is produced at pin 2. The End-of Word pulse provides a drive pulse for the Word Trigger stage and also provides an enabling level to the Display-Skip Generator during time-slot 1 only.

Pin 16 is a reset input for the Time-Slot Counter. When this pin is held LO, the Time-Slot Counter resets to time-slot 1. The Time-Slot Counter can be reset in this manner only when a Jump Command is received by U2155C and D (see following discussion).

WORD TRIGGER

The Word Trigger stage is made up of U2155A and B. Quiescently, pin 3 of U2155A is LO as established by the operating conditions of U2155D and C. Therefore, the LO End-of-Word pulse produced by the Time-Slot Counter results in a HI level at pin 1 of U2155A. This level is inverted by U2155A to provide a negative-going Word Trigger pulse to the Channel Counter.

Also, a Word Trigger pulse is produced by U2155B when a Jump Command is received at pin 9 of U2155C. This condition can occur during any time-slot (see Row Decoder for further information on origin of the Jump Command). Integrated circuit U2155D and C are connected as a bistable flip-flop. The positive-going Jump Command at pin 9 of U2155C produces a LO at pin 10. This LO is inverted by U2155D to produce a HI at pin 13, which allows pin 9 to be pulled HI through CR2156. The flip-flop has now been set and remains in this condition until reset, even though the Jump Command at pin 8 returns to its LO level. The HI output level at pin 13 turns on Q2159 to pull pin 16 of the Time-Slot Counter LO. This resets the Time-Slot Counter to time-slot 1 and holds it there until the Word Trigger is reset. At the same time, a HI level is applied to pin 4 of the Timer through CR2157 and CR2125. This HI level causes the Timer to operate in the Display-Skip mode, so a character is not generated.

The next Trigger pulse is not recognized by the Time-Slot Counter, since U2159 is locked in time-slot 1 by U2155. However, this Trigger pulse resets the Word Trigger stage through C2155. Pin 1 of U2155D goes LO to enable the Time-Slot Counter and Timer stages for the next time-slot pulse. Simultaneously, when U2155D switches output states, the resulting negative-going edge

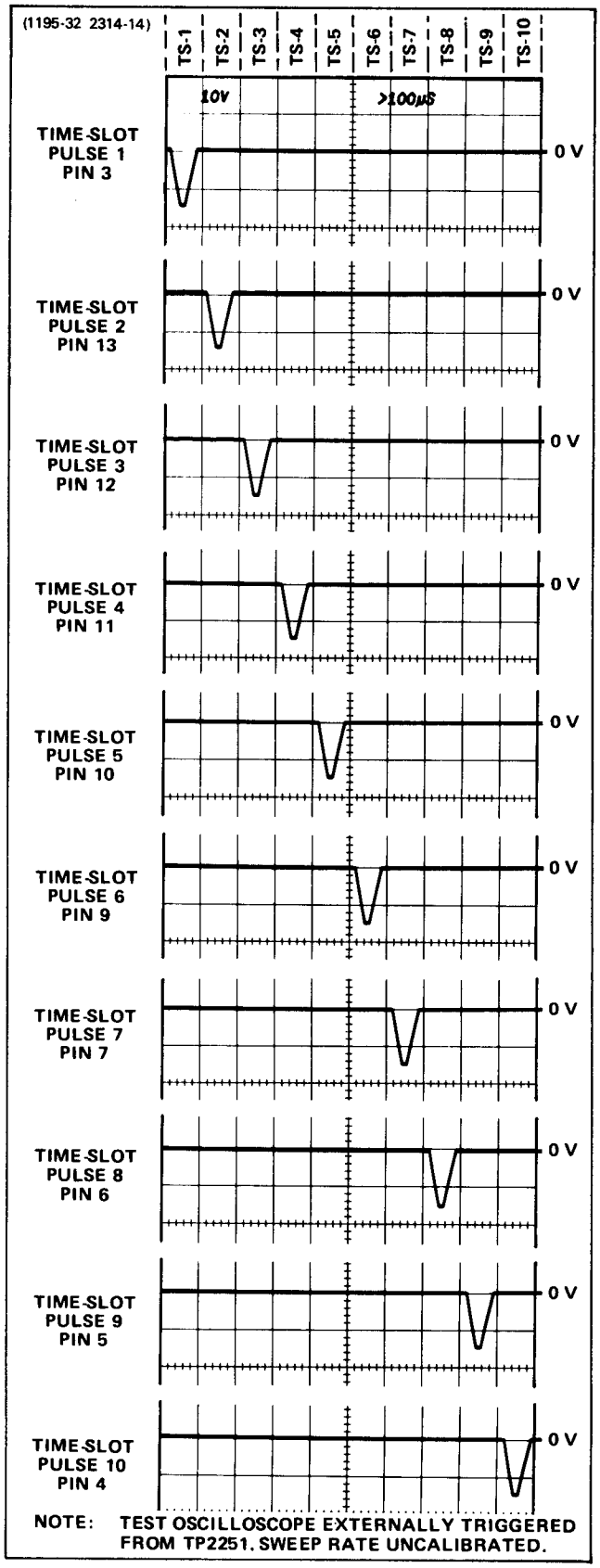


Figure 3-14. Timer relationship of the time-slot (TS) pulses produced by Q2159.

is connected to pin 3 of U2155A. This results in a negative-going Word Trigger output at pin 4 of U2155B to advance the Channel Counter to the next word. When the next Trigger pulse is received at pin 15 of U2159 the Time-Slot Counter returns to the normal sequence of operation and produces an output on the time-slot 1 line.

CHANNEL COUNTER

Channel Counter U2250 is a binary counter that produces the Channel Address Code for the Column and Row Decoder stages and the Format Generator stage. This code instructs these stages to sequentially select and display the 8 channels of data from the plug-ins. Table 3-12 gives the 8 combinations of the Channel Address Code and the resultant channel selected with each combination.

TABLE 3-12
Channel Address Code

Pin 11 U2250	Pin 8 U2250	Pin 9 U2250	Channel Displayed
LO	LO	LO	Channel 2 Left Vertical
LO	LO	HI	Channel 1 Left Vertical
LO	HI	LO	Channel 2 Right Vertical
LO	HI	HI	Channel 1 Right Vertical
HI	LO	LO	Channel 2 A Horizontal
HI	LO	HI	Channel 1 A Horizontal
HI	HI	LO	Channel 2 B Horizontal
HI	HI	HI	Channel 1 B Horizontal

SINGLE-SHOT LOCKOUT

The Single-Shot Lockout stage allows a single readout frame (8 complete words) to be displayed on the crt, after which the Readout System is locked out, so further readout displays are not presented until the circuit is reset. Integrated circuit U2120C and U2120B are connected to form a bistable flip-flop. For free-run operation, pin 8 of U2120C is held HI. This activates U2120C and results in a LO output level at pin 10, enabling the Timer stage to operate in a free-running manner.

The output of the Single-Shot Lockout stage remains LO to allow U2126 to operate in the free-running mode until a LO is received at pin 8 of U2120C. When this occurs, the output level at pin 10 of U2120C does not change immediately. However, the Readout System is now enabled as far as the single-shot lockout function is concerned. If the Channel Counter has not completed word 8, the Readout System continues to operate in the normal manner. However, when word 8 is completed, the negative-going end-of-frame pulse is produced at pin 11 of U2250 as the Channel Counter shifts to the code necessary to display word one. This pulse is coupled to pin 3 of U2120A. The momentary HI at pin 3 activates U2120B and its output stage goes LO to disable U2120C (pin 8 is already LO). The output of U2120C goes HI to disable the Timer stage, so it operates in the Display-Skip mode. The HI at pin 10 of U2120C also holds U2120B enabled, so it maintains control of the flip-flop.

The Single-Shot Lockout stage remains in this condition until a positive-going trigger pulse is applied to pin 8 of U2120C. This trigger pulse produces a LO at pin 10 of U2120C to enable U2126 and disable U2120B. Now, the Timer stage can operate in the normal manner for another complete frame. When word 8 is completed, the Channel Counter produces another end-of-frame pulse to again lock out the Timer stage.

ENCODING THE DATA

Data is conveyed from the plug-in units to the Readout System in the form of an analog (current level) code. The characters that can be selected by the encoded data are shown on the Character Selection Matrix (see Fig. 3-9). Each character requires two currents to define it; these currents are identified as the column current and the row current, corresponding to the column and row of the matrix. The column and row data is encoded by the programming of the plug-in units. Figure 3-15 shows a typical encoding scheme using resistors for a voltage-sensing amplifier plug-in unit. Notice that the 10 TS (time slot) pulses produced by the Time-Slot Counter stage are connected to the plug-in unit. However, time-slots 5, 6, and 10 are not used by the plug-in unit to encode data when using the Standard Readout Format. (See Table 3-11 for Standard Readout Format.) The amplitude of the time-slot pulse is exactly -15 volts as determined by the Timer stage. Therefore, the resultant output current from the plug-in units can be accurately controlled by the programming resistors in the plug-in units.

For example, in Figure 3-15 resistors R10 through R90 control the row-analog data, which is connected back to the Readout System. Figure 3-16 shows an idealized output current waveform of row-analog data, which results from the time-slot pulses. Each of the row levels of current shown in these waveforms correspond to 100 microamperes of current. The row numbers on the left-hand side of the waveform correspond to the rows in the Character Selection Matrix (see Fig. 3-9). The row-analog data is connected back to the Readout System via terminal B37 of the plug-in interface.

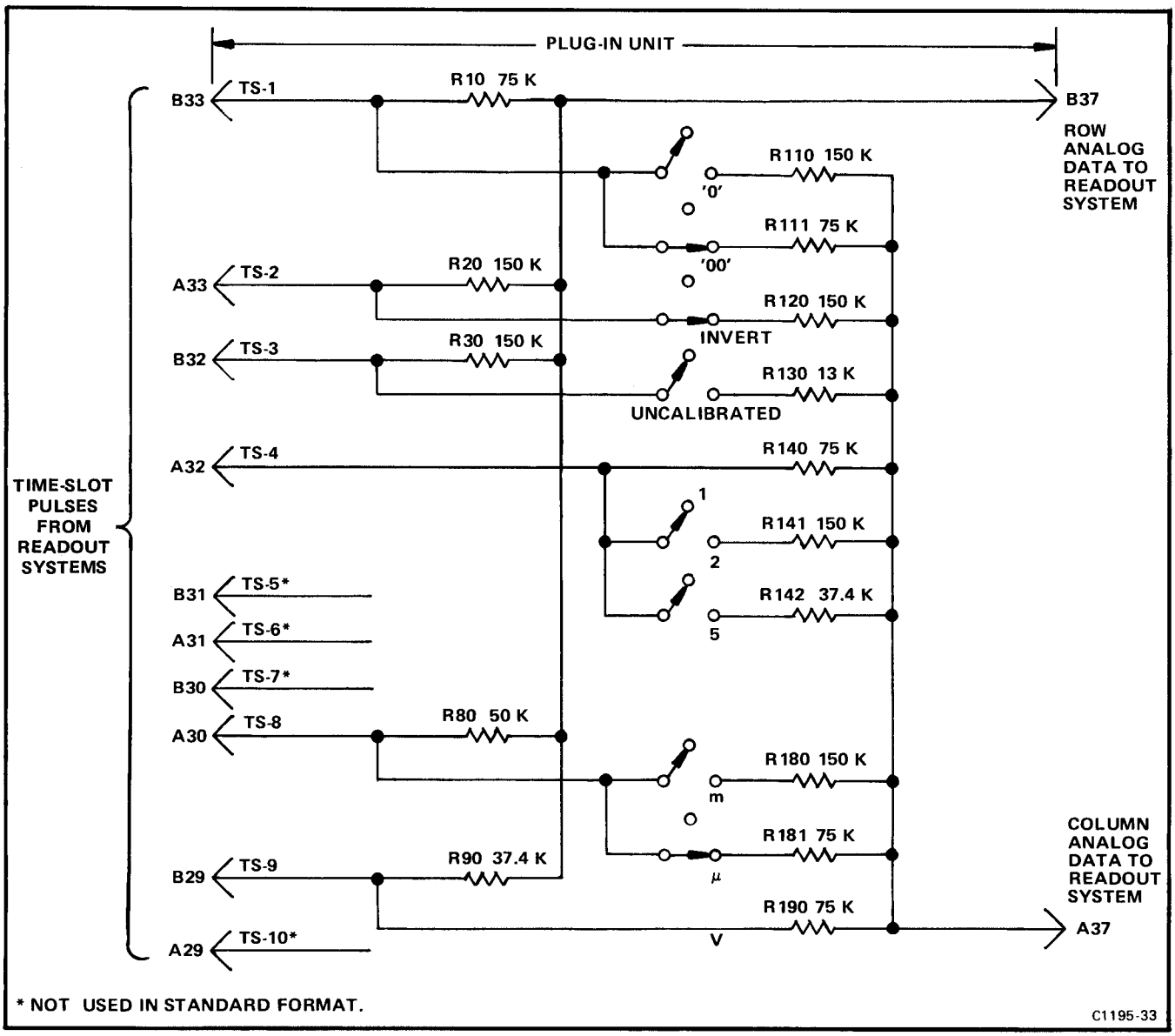


Figure 3-15. Typical encoding scheme for voltage-sensing plug-in unit. Coding shown for deflection factor of 100 microvolts.

The column-analog data is defined by resistors R110 through R190. The program resistors are connected to the time-slot lines by switch closures to encode the desired data. The data, as encoded by the circuit shown in Figure 3-15, indicates a 100 microvolt sensitivity with the crt display inverted and calibrated deflection factors. This results in the idealized output current waveforms shown in Figure 3-16 at the column-analog data output, terminal A37 of the plug-in interface.

Resistor R111, connected between time-slot 1 and the column-analog data output, encodes two units of current during time-slot 1. Referring to the Character Selection Matrix, two units of column current, along with the two units of row current encoded by resistor R10 (row 3), indicates that two zeros should be added to the display.

Resistor R120 adds one unit of column current during time-slot 2 and, along with the one unit of current from the row output, the Readout System is instructed to add an invert arrow to the display. Resistor R130 is not connected to the time-slot 3 line, since the deflection factor is calibrated. Therefore, there is no display on the crt. (See Display-Skip Generator for further information.)

During time-slot 4, two units of column current are encoded by R140. There is no row current encoded during this time-slot; this results in the numeral 1 being displayed on the crt. Neither row-n or column-analog data is encoded during time-slots 5, 6, and 7 as defined by the Standard Readout Format. During time-slot 8, two units of column current and three units of row current are encoded by resistors R181 and R80, respectively. This

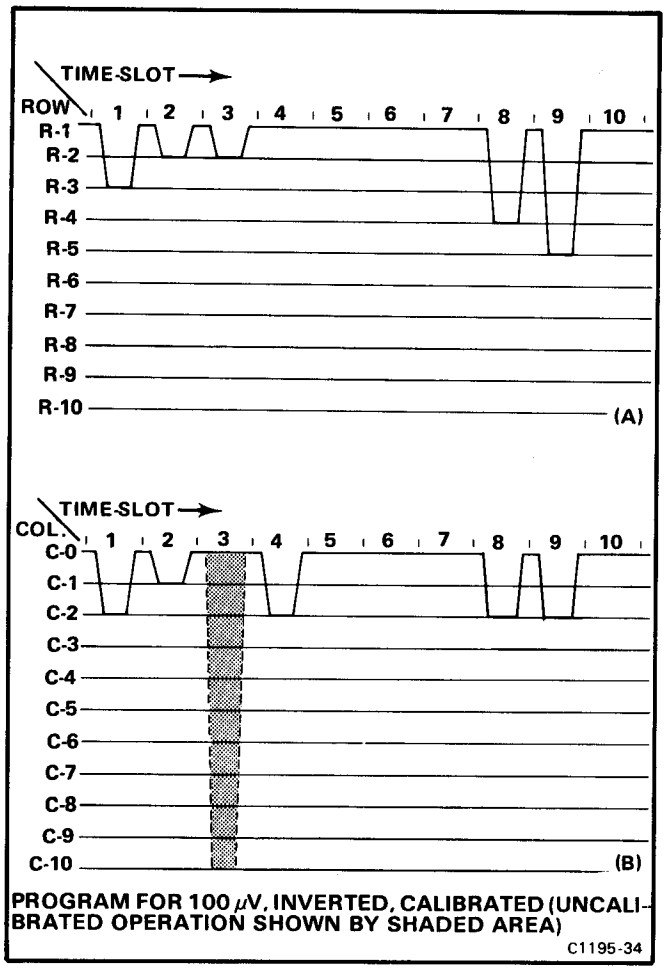


Figure 3-16. Idealized current waveforms of (A) Row analog data and (B) Column analog data.

addresses the μ prefix in the Character Selection Matrix. The final data output is provided from time-slot 9 by R190 connected to the column output and R90 to the row output. These resistors encode two units of column current and four units of row current to cause a V (volts) symbol to be displayed. Time-slot 10 is not encoded, in accordance with the Standard Readout Format. The resultant crt readout will be ⌊ 100 μV.

In the above example, the row-analog data was programmed to defined which row of the Character Selection Matrix was addressed to obtain information in each time-slot. The column data changes to encode the applicable readout data as the operating conditions change. For example, if the variable control of the plug-in unit was activated, R130 would be connected between time-slot 3 and the column-analog data output line. This encodes 10 units of column current (see shaded area in time-slot 3 of the waveform shown in Fig. 3-16). Since one unit of row current is also encoded during this time-slot by R30, a > (greater than) symbol is added to the display. The crt readout will now show > 100 μV. In a similar manner, the other switches can change the encoded data for the column output and thereby change the readout display. See the descriptions which follow for decoding this information.

The column analog data encoded by most plug-in units can be modified by attenuator probes connected to the input connectors of amplifier plug-in units. A special coding ring around the input connector of the plug-in unit senses the attenuation ratio of the probe (with readout-encoded probes only). The probe contains a circuit that provides additional column current. For example, if a 10X attenuator probe is connected to a plug-in unit encoded for 100 microvolts as shown in Figure 3-15, an additional unit of current is added to the column-analog data during time-slot 1. Since two units of current were encoded by R111, this additional current results in a total of three units of column-analog current during this time-slot. Referring to the Character Selection Matrix, three units of column current, along with the two units of row current encoded by R10, indicates that the prefix should be shifted one column to the left. Since this instruction occurs in the same time-slot that previously indicated that two zeros should be added to the display and only one instruction can be encoded during a time-slot, the zeros do not appear in the display. The crt readout will now be changed to 1 mV (readout program produced by plug-in same as for previous example).

Three other lines of information are connected from the plug-in compartments to the Readout System. The column- and row-analog data from channel 2 of a dual-channel plug-in are connected to the Readout System through terminals A38 and B38 of the plug-in interface, respectively. Force-readout information is encoded on terminal A35; the function of this input is described under Column and Row Data Switches. The preceding information gave a typical example of encoding data from an amplifier plug-in unit. Specific encoding data and circuitry is shown in the individual plug-in unit manuals.

COLUMN AND ROW DATA SWITCHES

The encoding data from the plug-in units is connected to the Column and Row Data Switch stages. A column-data line and a row-data line convey analog data from each of the 8 data sources (2 channels from each of the 4 plug-in compartments).

The Column Data Switch U2190 and the Row Data Switch U2180 receive the Channel Address Code from the Channel Counter (refer to diagram 6 at the rear of this manual). This binary code directs the Column Data Switch and the Row Data Switch as to which channel should be the source of the encoding data. Table 3-12 gives the eight combinations of the Channel Address Code and the resultant channel selected with each combination. These stages have nine inputs and provide a time-multiplexed output at pin 7, which includes the information from all of the input channels. Eight of the nine inputs to each stage originate in the plug-in units; the ninth input comes from a special data-encoding network composed of resistors R2191 through R2199 and R2201 through R2209. (See Zeros Logic and Memory description for further information on ninth channel.)

In addition to the encoding data inputs from the plug-in units, inputs are provided to the Column Data Switch from the VERTICAL MODE and HORIZONTAL MODE switches to inhibit the readout for any plug-in unit(s) not selected for display. When a unit is not selected, the line corresponding to the opposite channel is HI to forward bias the associated diodes: CR2162 and CR2163, CR2166 and CR2167, CR2170 and CR2171, or CR2174 and CR2175. The forward-biased diodes cause the channel switches to bypass the encoded data from the inhibited channel. However, since it may be desired to display information from special-purpose plug-in units (even though they do not produce a normal waveform display on the crt), a feature is provided to override the channel inhibit. This is done by applying a LO to the associated Force Readout input. The LO level diverts the HI channel-inhibit current and allows the data from this plug-in unit to reach the Column Data Switch, even though it has not been selected for display by the mode switch.

Row Match adjustment, R2183, sets the gain of the Row Data Switch to match the gain of the Row Decoder for correct output. Column Match adjustment, R2214, performs the same function for the Column Data Switch stage.

DISPLAY-SKIP GENERATOR

The Display-Skip Generator is made up of Q2215, Q2223, Q2229, and Q2225. This stage monitors the time-multiplexed column data at the output of the Column Data Switch during each time-slot to determine if the information is valid data that should result in a crt display. Quiescently, there is about 100 microamperes of current flowing through R2213 from Q2240 and the Zeros Logic and Memory stage. (The purpose of this quiescent current will be discussed in connection with the Zeros Logic and Memory stage.) This current biases Q2215A so that its base is about 0.2 volt more positive than the base of Q2215B in the absence of column data. Therefore, since Q2215A and Q2215B are connected as a comparator, Q2215A will remain on unless its base is pulled more negative than the base of Q2215B.

The analog data output from the Column Data Switch produces a 0.5 volt (approximately) change for each unit of column current that has been encoded by the plug-in unit. Whenever any information appears at the output of the Column Data Switch, the base of Q2215A is pulled more negative than the base of Q2215B, resulting in a negative (LO) Display-Skip output to the Timer stage through Q2225. Recall that a LO was necessary at the skip input of the Timer so it could perform the complete sequence necessary to display a character.

Transistors Q2223 and Q2229 also provide Display-Skip action. The End-of-Word level connected to their emitters is LO only during time-slot 1. This means they are enabled only during this time-slot. These transistors allow the Zeros Logic and Memory stage to generate a Display-Skip signal during time-slot 1 when information that is not to be displayed on the crt has been stored in memory (further information is given under Zeros Logic and Memory).

COLUMN AND ROW DECODERS

The Column Decoder U2244 and Row Decoder U2185 sense the magnitude of the analog voltages at their inputs (pin 10) and produce a binary output on one of ten lines corresponding to the column or row data encoded by the plug-in unit. These outputs provide the Column Digital Data and Row Digital Data, which is used by the Character Generator stages to select the desired character for display on the crt. The column and row data is also used throughout the Readout System to perform other functions.

The input current at pin 9 of the Column Decoder stage is steered to only one of the ten Column Digital Data outputs. When a Display-Skip signal is present (collector of Q2225 HI), pin 9 is pulled HI through CR2226. This ensures that no current is connected to the Character Generator stage under this condition. Notice the corresponding input on the Row Decoder. This input is connected to ground and causes only one of the ten row outputs to saturate to ground.

The network at the input of the Row Decoder, made up of Q2153 and its associated components, is a row-14 detector that produces the Jump Command. This row current is encoded by special-purpose plug-ins to cause all or part of a word to be jumped. Whenever row 14 (13 units of row current, or 1.3 milliamperes) is encoded, the base of Q2153 is pulled negative enough so that this transistor is reverse biased to produce a HI Jump Command output at its collector. The Jump Command is connected to the Word Trigger stage to advance the Channel Counter to the next word and to reset the Time-Slot Counter to time-slot 1.

ZEROS LOGIC AND MEMORY

The Zeros Logic and Memory stage, U2232, stores data encoded by the plug-in units to provide zeros-adding and prefix-shifting logic for the Readout System. The Strobe pulse at pin 15 goes positive when the data has stabilized and can be inspected. This activates the Zeros Logic and Memory stage so that it can store the encoded data.

Typical output waveforms of the five possible input conditions that can occur are shown in Figure 3-17. When time-slot 1 occurs, a store command is given to all of the memories. If the plug-in units encoded data for column 1, 2, 3, 4, or 10 during time-slot 1, the appropriate memory (or memories) is set. Notice that row 3 information from the Row Decoder must also be present at pin 16 for data to be stored in the memory of U2232.

If data was encoded during time-slot 1, a negative-going output is produced at pin 7 while the memories are being set. This negative-going pulse is connected to the base of Q2229 in the Display-Skip Generator to produce a Display-Skip output. Since the information encoded during time-slot 1 was only provided to set the memories and not intended to be displayed on the crt at this time, the Display-Skip output prevents a readout display during this time-slot.

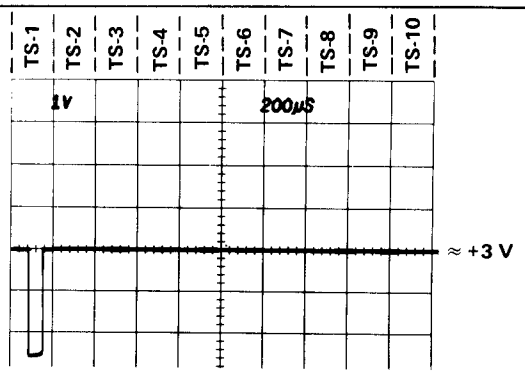
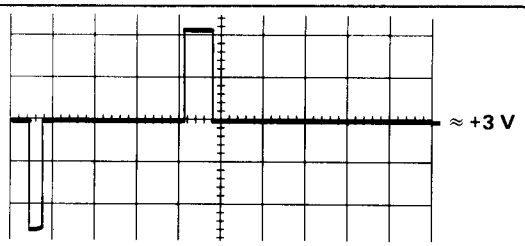
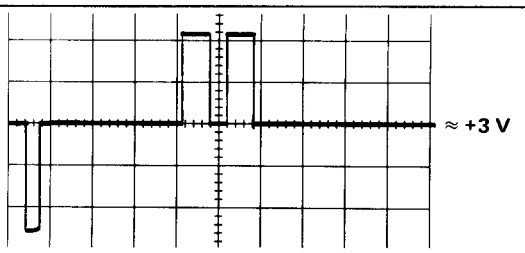
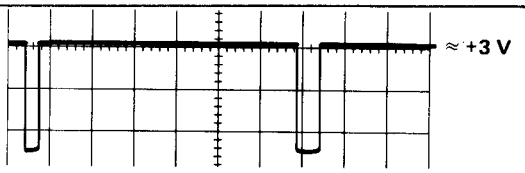
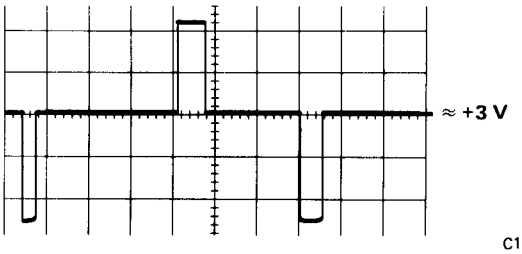
INPUT PIN OF U2232 ACTIVATED	COMMAND	TIME-SLOTS
14	IDENTIFY	
12	ADD ONE ZERO	
13	ADD TWO ZEROS	
10	DECREASE PREFIX	
11	DECREASE PREFIX AND ADD ONE ZERO	

Figure 3-17. Typical output waveforms for Zeros Logic and Memory stage operation (at pin 7 of U2232).

During time-slot 5, a memory within U2232 is interrogated. If information was stored in this memory, a positive-going output is produced at pin 7. This pulse is connected to pin 10 of the Column Decoder through Q2240 to add one unit of current at the input of the Column Decoder. This produces a zero after the character displayed during time-slot 4. During time-slot 6, another memory within U2232 is interrogated to see if another zero should be added. If another zero is necessary, a second positive output is produced at pin 7, which again results in a column 1 output from the Column Decoder and a second 0 in the crt display.

Finally, another memory within U2232 is interrogated during time-slot 8 to obtain information on whether the prefix should be changed, or left at the value that was encoded. If data has been encoded that calls for a shift in prefix, a negative-going output level is produced at pin 7. This negative level subtracts one unit of column current

from the data at the input to the Column Decoder. Notice, on the Character Selection Matrix of Figure 3-9, that when row 4 is programmed, a reduction of one column results in a one-column shift of the prefix. For example, with the 100 μV program shown in Figure 3-15, if the data received from the plug-in called for a shift in prefix, the crt readout would be changed to 1 mV (zeros deleted by program; see Encoding the Data).

The 100 microamperes of quiescent current through R2213 provided by Q2240 (see Display-Skip Generator) allows the prefix to be shifted from m (100 microamperes of column current, column 1) to no prefix (0 column current, column 0) so only the unit of measurement encoded during time-slot 9 is displayed. Notice that reducing the prefix program from column 1 to column 0 programs the Readout System to not display a character at this readout location.

A further feature of the Zeros Logic and Memory is the Identify function. If 10 units of column current are encoded by the plug-in unit along with row 3 during time-slot 1, the Zeros Logic and Memory produces a negative-going output pulse at pin 1 to switch the Column Data Switch and Row Data Switch to the ninth channel. Then, time-slot pulses 2 through 9 encode an output current through resistors R2201 and R2199 for column data and R2201 and R2209 for row data. This provides the current necessary to display the word IDENTIFY in the word position allotted to the channel that originated the Identify command. After completion of this word, the Column Data Switch and Row Data Switch continue with the next word in the sequence.

The Word Trigger signal from the Word Tigger stage is connected to pin 9 of U2232 through C2242. At the end of each word of readout information, this pulse goes LO. This erases the four memories in the Zeros Logic and Memory in preparation for the data to be received from the next channel.

CHARACTER GENERATOR

The Character Generator stage consists of five similar integrated circuits (U2270, U2272, U2274, U2276, U2278), which generate the X (horizontal) and Y (vertical) outputs at pins 16 and 1, respectively, to produce the character display on the crt. Each integrated circuit can produce 10 individual characters; U2270 (designated "Numerals") can produce the numerals 0 through 9 shown in row 1 of the Character Selection Matrix (Fig. 3-9). Integrated circuit U2272 can produce the symbols shown in row 2 of the Character Selection Matrix and U2274 produces the prefixes and some letters, used as prefixes, shown in row 4. Integrated circuits U2276 and U2278 produce the remaining letters shown in rows 5 and 6 of the Character Selection Matrix.

All of the Character Generator stages receive the Column Digital Data from the Column Decoder U2244 in parallel. However, only one of the Character Generators receives row data at a particular time and only the stage receiving this row data is activated. For example, if column 2 is encoded, the five Character Generators are enabled so that either a 1, >, μ, V, or an n can be produced. If row 4 has been encoded at the same time, only the Prefix Character Generator U2274 will produce an output to result in a μ being displayed. The activated Character Generator provides current output for the Format Generator to produce the selected character on the crt. In a similar manner, any of the characters shown in the Character Selection Matrix can be displayed by correct addressing of the row and column.

DECIMAL POINT LOGIC AND CHARACTER POSITION COUNTER

Decimal Point Logic and Character Position Counter U2260 performs two functions. The first function is to add a staircase current to the X (horizontal) signal to space the characters horizontally on the crt. After each character is generated, the negative-going edge of the Ready signal at pin 5 advances the Character Position Counter. This produces a current-step output at pin 3 which, when added to the X signal, causes the next character to be displayed one character space to the right. This stage can also be advanced when a Space instruction is encoded so a space is left between the displayed characters on the crt. Row 10 information from the Row Decoder is connected to pin 4 of U2260. When row 10 and column 0 are encoded, the output of this stage advances one step to move the next character another space to the right. However, under this condition, no display is produced on the crt during this time-slot, since the Character Generators are not activated.

Time-slot pulses 1, 2, and 3 are also connected to pin 4 of U2260 through VR2262, VR2263, and VR2264 respectively and R2262 and R2265. This configuration adds a space to the displayed word during time-slots 1, 2, and 3 even if information is not encoded for display during these time-slots. With this feature, the information displayed during time-slot 4 (scaling data) always starts in the fourth character position whether data has been displayed in the previous time-slots or not. Therefore, the resultant crt display does not shift position as normal-invert or cal-uncal information is encoded. The Word Trigger pulse connected to pin 8 resets the Character Position Counter to the first character position at the end of each word.

The Decimal Point Logic portion of this stage allows decimal points to be added to the crt display. With the Standard Readout Format, row 7, encoded coincident with columns 3 through 7, addresses a decimal at one of the five locations identified in row 7 of the Character Selection Matrix (Fig. 3-9). This instruction refers to the decimal-point location in relation to the total number of characters possible in one word (see Fig. 3-18). For example, column 3 encoded with row 7 during time-slot 1 places a decimal point in location number 3. As shown in Figure 3-18, this displays a decimal point after the third character that can be displayed on the crt. (The first three time-slots produce a space whether data is encoded or not; see previous paragraph.)

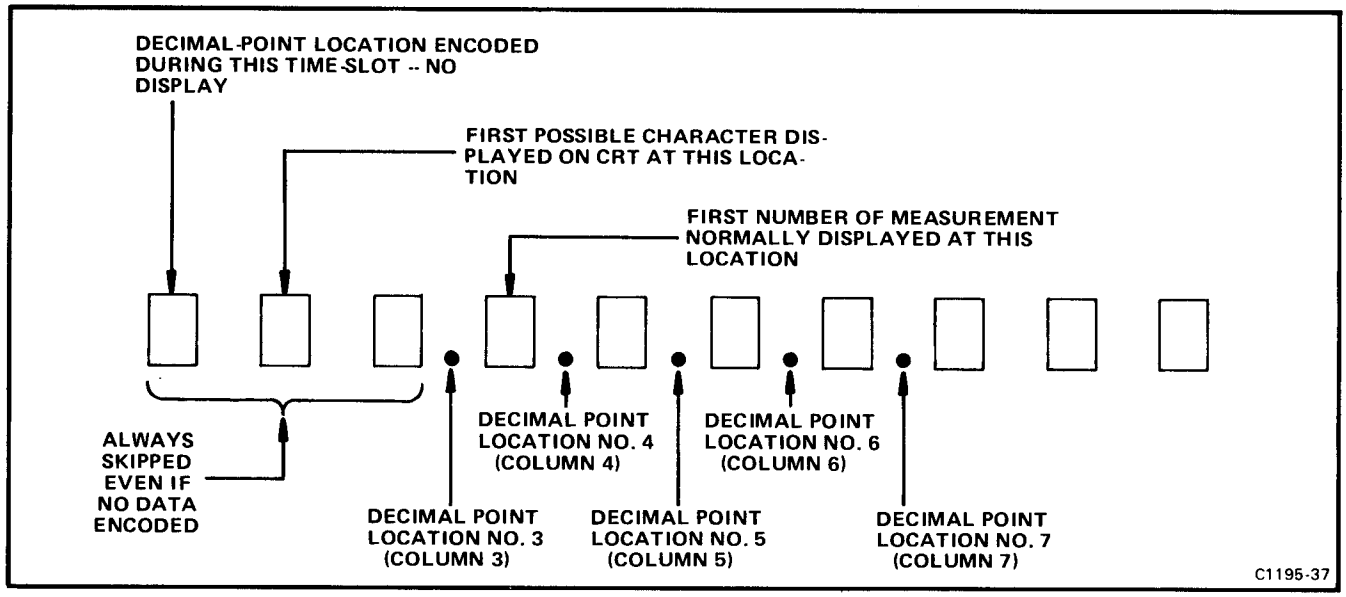


Figure 3-18. Readout word relating 10 possible character locations to the decimal point instructions that can be encoded; and the resultant crt display.

When decimal-point data is encoded, the crt is unblanked so a readout display is presented. Since row 7 does not activate any of the five Character Generators, the crt beam is deflected vertically by the application of row-7 data to the Y input of the Format Generator through R2278 and R2280. This places the decimal point between the characters along the bottom line of the readout word. After the decimal point is produced in the addressed location, the crt beam returns to the location indicated by the Character Position Counter to produce the remainder of the display.

FORMAT GENERATOR

The X- and Y-deflection signals produced by the Character Generator stage are connected to pins 2 and 7, respectively, of the Format Generator. The Channel Address Code from the Channel Counter is also connected to pins 1, 8, and 15 of this stage. The Channel Address Code directs the Format Generator to add current to the X and Y signals to deflect the crt beam to the area of the crt associated with the plug-in channel that originated the information (see Fig. 3-8). The Channel Address Code and the resultant word positions are shown in Table 3-12. The Ready signal at pin 13 (coincident with the X/Y Inhibit Command output) activates this stage when a character is to be displayed on the crt. Variable resistor R2273 determines the horizontal and vertical size of the displayed characters. The character-position current from the Decimal Point Logic and Charcter-Position Counter stage is added to the X (horizontal) input signal to space the characters horizontally on the crt (see previous discussion).

Y-OUTPUT

The Y-output signal at pin 6 of Format Generator U2284 is connected to the Y-Output amplifier Q2287 and Q2299. This stage provides a low impedance load for the Format Generator while providing isolation between the Readout System and the driven circuits. Vertical Separation adjustment R2291 changes the gain of this stage to control the vertical separation between the readout words displayed at the top and bottom of the graticule area.

X-OUTPUT

The X-Output amplifier Q2286 and Q2296 operates like the Y-Output amplifier, to provide the horizontal deflection from the readout signal available at pin 4 of U2284. The gain of this stage is fixed by the values of the resistors in the circuit.

DISPLAY SEQUENCE

Figure 3-19 shows a flow chart for the Readout System. This chart illustrates the sequence of events that occurs in the Readout System each time a character is generated and displayed on the crt.

SIGNALS OUT

The Signals Out circuit provides the + SAWTOOTH and + GATE signals to the front panel. These output signals are samples of signals from the associated time-base units.

A schematic diagram of the signals Out circuit is given on diagram 7, in Section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by gray shaded lines separating the circuitry into major

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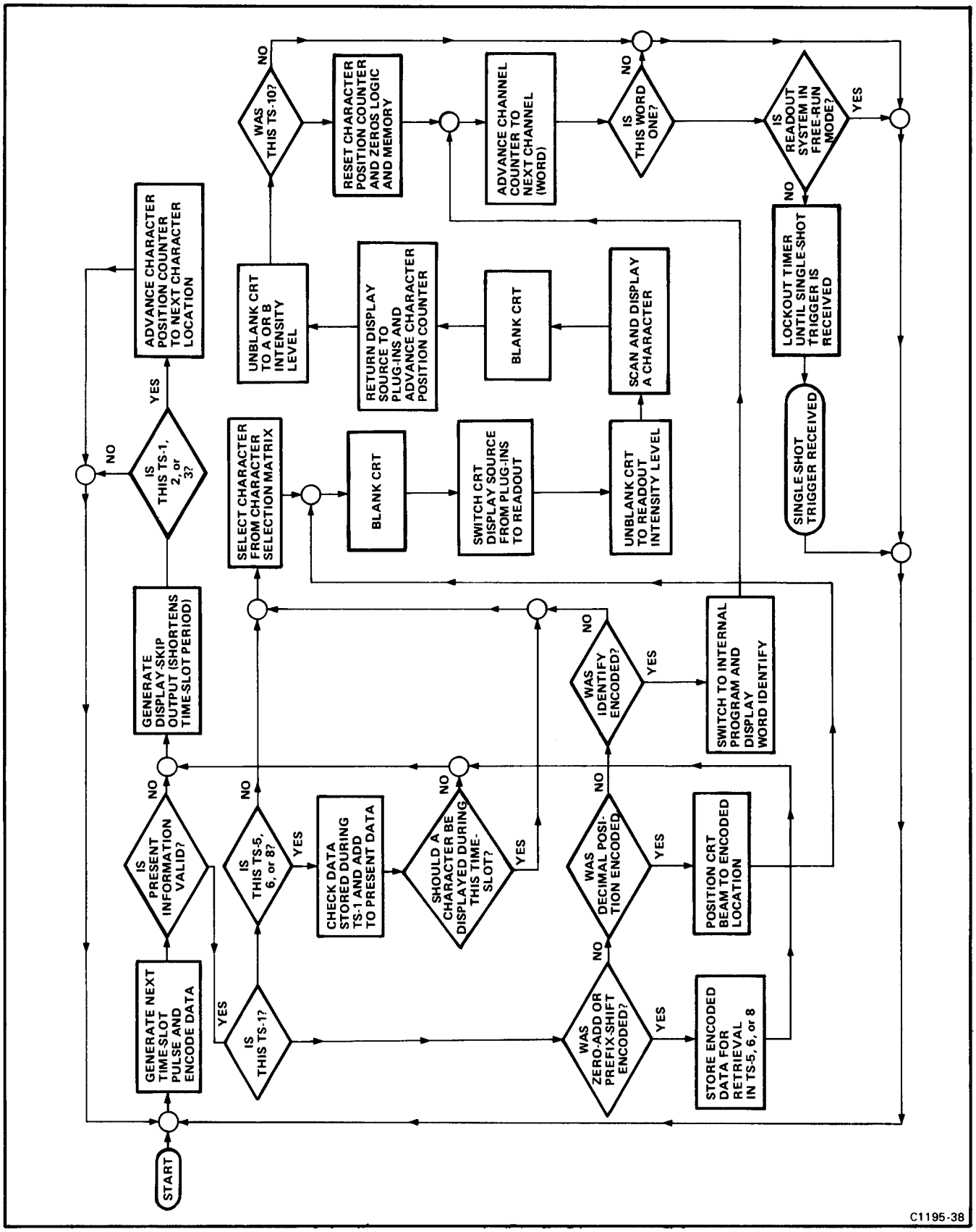

Figure 3-19. Flow chart for character generation by the Readout System.

stages. These stages aid in locating components mentioned here. Sub-headings in the following discussion use the stage names to further identify portions of the circuitry on diagram 7.

+ SAWTOOTH AMPLIFIER

The sawtooth signals from the A and B time-base units are connected to the Sawtooth Amplifier stage through series resistors R93 and R95 respectively (see diagram 3). The front-panel selector switch, S1930, determines whether the A-sweep or the B-sweep sawtooth signal provides the + SAWTOOTH signal. The unused sawtooth signal is terminated by R1941.

Transistors Q1943-Q1942-Q1946 form an inverting feedback amplifier. Gain of the stage is about 2, as determined by the ratio of feedback resistor R1944 to the input resistance (made up of R1940 and on diagram 3, either R93 or R95 depending on which sawtooth source is selected).

+ GATE AMPLIFIER

The front-panel + GATE switch (S1940) selects the gate signal from either A or B time-base unit. The unused + gate is terminated in R1931. Before a gate occurs, Q1934 is biased off and Q1938 is conducting; its collector potential is low enough to cut off Q1928. When a gate occurs, it is coupled to the base of Q1934, causing it to conduct thereby cutting off Q1938. The current through R1911 now flows through Q1928 to produce the + GATE signal. The signal at the collector of Q1934 is picked off to drive the Graticule Illumination stage and/or the readout system in PULSED mode.

GRATICULE ILLUMINATION

Variable resistor R1900 (GRAT ILLUM) determines the brightness of the graticule lights (except when in the PULSED position) by controlling the output of the graticule light supply (see LV Regulators, diagram 15). Variable resistor R1902 (GRAT ILLUM PRESET) determines the brighness of the graticule lights when the GRAT ILLUM control is set to PULSED. In the PULSED mode, the graticule lights are gated on for approximately 0.5 second. Programmable unijunction transistor Q1908, in conjunction with Q1910, generates the pulse to turn the graticule lights on. A negative signal (from the MAN pushbutton, the + Gate or from an external input) will cause Q1908 to conduct and start discharging C1908. At this time, Q1910 turns off, which allows R1902 to control the output of the graticule light supply. Capacitor C1908 discharges until Q1908 cannot maintain conduction. As Q1908 turns off C1908 begins to charge positive until the zener voltage of CR1910 is reached which turns on Q1910; its collector then goes negative to turn the graticule light supply off. When in the PULSED mode and operating from the + GATE source, the graticule lights will turn on momentarily at the trailing edge of the + GATE (end of each sweep).

8

VERTICAL CHANNEL SWITCH

The Vertical Channel Switch circuit selects the vertical deflection signal from the output of the LEFT and/or RIGHT VERT plug-in compartment(s) for display on the crt.

A schematic diagram of the Vertical Channel Switch is given on diagram 8, in Section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by gray shaded lines separating the circuitry into major stages. These stages aid in locating components mentioned here. Sub-headings in the following discussion use the stage names to further identify portions of the circuitry on diagram 8.

CHANNEL SWITCH

The vertical deflection signal from the left and right vertical plug-in units is either terminated within the stage or coupled through the stage as determined by the Vertical Channel Selector stage. The Channel Switch stage is made up primarily of integrated circuit U668. Inputs 7 and 9 provide a differential input for the signal from the right vertical plug-in unit. Input pins 17 and 19 provide a differential input for the signal from the left vertical plug-in unit. The differential output signal at pins 3 and 13 is connected to J694 and J592 respectively.

Components U682, Q682, Q676, and Q672 supply standing current to U668 and maintain the output common-mode dc level at +8.5 volts for all Channel Switch modes. The common-mode level at pins 3 and 13 of U668 is sensed by R559-R659, and compared with a reference level determined by divider R680-R681. Assume, for example, that pin 2 of U682 is lower than pin 3, indicating an output level below +8.5 volts. The output of U682 at pin 6 will be driven positive and current will flow in R683. This current must be supplied from the +15 V supply via R682, thereby lowering the base voltage of Q682. This increases the collector current in Q682. Transistor Q676 operates as a common-base amplifier and passes along the increased collector current to pin 3a of U668. This increases the output common-mode level, thus bringing U682 into balance. The voltage at pin 3a of U668 depends on the Channel Switch mode: in LEFT, RIGHT, ALT, or CHOP pin 3a is at +10.5 V; in ADD it is +12.5 V; when X-Y Inhibit is HI, pin 3a is +8.5 volts. In all modes, the current supplied by Q676 is 160 milliamperes plus or minus small variations required to keep the output level at +8.5 volts.

VERTICAL CHANNEL SELECTOR

The Vertical Channel Selector interfaces the Channel Switch, U668, to the logic signals arriving from the Main Interface. The Channel Switch stage requires two pairs of complementing control voltages; one pair for each channel. The HI control voltage is +4.0 V, the

complementing LO voltage is +3.5 V. To select a channel, the HI level must be applied to the On input of U668 (pin 2 for LEFT, and pin 12 for RIGHT VERTICAL MODE switch positions) and the LO level must appear at the OFF input (pin 1 for LEFT, and pin 11 for RIGHT VERTICAL MODE switch positions). To inhibit a channel the control voltages should be reversed.

When the VERTICAL MODE switch is set to LEFT the Display Right line, entering on P680 pin 6, is set LO (-0.6 V), the Add line (P680 pin 5) is LO (0 V) and, normally, X-Y Inhibit is LO (-0.6 V). Transistors Q652, Q658 and Q558 are turned on; Q656 and Q556 are off. The result is pins 1 and 12 of U668 are pulled down to +3.5 V but pins 2 and 11 are only pulled down to +4.0 V. Consequently, the LEFT VERT channel is turned on while the RIGHT VERT channel is turned off. Signals appearing at J602 and J603 are amplified and fed to the outputs at J592 and J694. Similarly, if Display Right is HI (+1 V), the RIGHT VERT channel is turned on and LEFT VERT channel off. RIGHT VERT channel signals are amplified and fed to the outputs. LEFT VERT channel signals are terminated within U668.

When the VERTICAL MODE switch is set to either ALT or CHOP, the Display Right signal line switches between the LO and HI levels at a rate determined by either the Chop Counter or Vertical Binary stages (see Logic description diagram 4). This action displays the signal from the left vertical unit when the Display Right signal line is LO and displays the signal from the right vertical unit when the signal line is HI.

When ADD vertical mode operation is selected, the Add signal line is HI, and the Display Right signal is LO. This allows both the right and left vertical signals to pass to the output of U668. The signals from both vertical units are algebraically added and the resultant signal determines the vertical deflection. The X-Y Inhibit command has absolute control over the output of the Channel Switch stage. Quiescently, this signal is LO; however when the Readout System is ready to display information on the crt, this level goes HI, to block the signals from both vertical units.

When X-Y Inhibit is HI (+1 V) Q652 is turned off. Current in R653 now flows through CR552 and CR654 lowering the base voltage of Q556 by one diode drop, and that of Q658 by two diode drops. This ensures that Q558 and Q656 are turned on regardless of the state of Display Right or Add.

RIGHT AND LEFT CHANNEL FEEDBESIDE

The operation of the Left and Right Channel Feedbeside stages are identical. Therefore, only a discussion of the Right Channel Feedbeside is given.

The function of the Feedbeside stage is to compensate for low-frequency imperfections in the frequency response of the Channel Switch stage, U668. Self heating of the transistor base-emitter junction, in some transistors within U668, causes the low-frequency gain to appear larger than the midband gain. To correct this, a portion of the input signal is picked off through R502 and R504 and applied to U508. This differential signal is converted to a single-ended signal and distributed into four RC (resistive-capacitative) networks, each having a different time constant. Variable components R512, R515, R520, R525, R530, and C538 are adjusted to provide an accumulated waveform. This waveform is converted to a paraphase signal by U538, Q542 and Q548, and is then injected into U668 through pins 6 and 4, where it is subtracted from the signal entering U668 at pins 7 and 9. Proper adjustment results in flat-frequency response and optimum-transient response at the output pins 3 and 13.

9

VERTICAL AMPLIFIER

A schematic diagram of the Vertical Amplifier is given on diagram 9, in section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by gray shaded lines separating the circuitry into major stages. These stages aid in locating components mentioned here. Sub-headings in the following discussion use the stage names to further identify portions of the circuitry on diagram 9.

The Vertical Amplifier circuit provides final amplification for the vertical signal received from delay-line DL694 before it is applied to the crt vertical deflector. In addition, low-frequency signals to provide the VERT TRACE SEPARATION (B) function and crt scale factor readout are accepted at the Aux Y-Axis and Y Readout inputs, respectively. The vertical portion of the BEAMFINDER function is also handled in the Vertical Amplifier.

DELAY-LINE COMPENSATION

Delay-line DL694 delays the vertical signal approximately 51 nanoseconds to allow the horizontal circuits time to initiate a sweep before the vertical signal reaches the crt vertical deflector. This allows the instrument to display the triggering event when using internal triggering. The delay-line is composed of a matched pair of 50 ohm coaxial cables. The signal from the delay lines is coupled on to the 50 Ω microstrip via J702 and J704. Transient response front-corner adjustment is provided by RLC network R705, C705 and parasitic inductance of C705.

Hybrid circuit U762 and its associated circuitry provides frequency compensation to offset delay line losses due to "skin-effect" in the cable. This compensation is achieved by attenuating the signal at low-frequencies approximately 4.8 dB. At high frequencies (above 1.5 gigahertz) the signal passes with little attenuation. Hybrid circuit U762 also terminates the delay line in its characteristic impedance (50 ohms) for frequencies greater than about 50 MHz. At dc, U762 presents an impedance of 41 Ω to each cable; reverse termination of U668. Vertical Channel Switch, prevents standing waves below 50 MHz.

OUTPUT AMPLIFIER

The Output Amplifier consists of 2 thin-film, hybrid wideband amplifiers, U842 and U862, and their associated bias circuitry. These amplifiers provide a voltage gain of approximately 4.5 each, resulting in an overall voltage gain from J702 and J704 to the crt vertical deflector of about 11. All signal path interconnections between and within hybrids are made with 50 ohm strip transmission lines via the HYPCON system.

Integrated circuit U842 receives the delayed and compensated signal from U762 at input pins 7 and 9. Variable resistor R855 provides Vertical Amplifier gain adjustment by shunting the differential signal. Trimmer R836 is a transient response adjustment effective in the first 10 nanoseconds of the step response. The output of U842 is fed through level shifters VR852 and VR862 to U862. Bias current for U842 is supplied by Q892 and R893 through U862. Active devices Q892, U876B and associated circuitry operate as a power supply with (negative) output impedance of 25 ohms. This supply acts to maintain a constant common-mode dc level at the input to U862 regardless of current demand from U842.

Bias levels for U862 are provided by U876A. Diode CR875 temperature compensates the +23.9 V supply to maintain constant standing current in U862.

FEEDBESIDE

The function of the Feedbeside stage is to compensate for low-frequency imperfections in the frequency response of the Output Amplifier stage, U842 and U862. Self heating of the transistor base-emitter junction, in some transistors within U842 and U862, cause the low-frequency gain to appear larger than the midband gain. To correct this, a portion of the input signal is picked off via the Delay Line Compensation stage and applied to U782. The paraphase signal is converted to a single-ended signal by U782 and distributed into six RC (resistive-capacitive) networks, each having a different time constant. Resistors R785, R787, R791, R795, R801, R806, and Capacitor C808 are adjusted to provide an accumulated waveform. This waveform is converted to a paraphase signal by U808, Q824, and Q814, and is then injected into U842 through pins 1 and 5, where it is subtracted from the signal entering U842 at pins 7 and 9. Proper adjustment of the seven RC components results in a flat-frequency response and optimum-transient response at the output of U862 (pins 17 and 19).

Diodes CR767 and CR777 improve the vertical amplifier overdrive recovery by limiting the amplitude of the feedbeside-correction signals that exceed the dynamic range of the Output Amplifier. Thermistor RT813 adjusts the gain of the feedbeside amplifier to provide increased correction at high ambient temperature where transistor self-heating is aggravated.

AUXILIARY AMPLIFIER

The Auxiliary Amplifier is used to inject low-frequency (≤ 2 MHz) signals associated with crt scale-factor readout and alternate sweep switching into the vertical deflection system. Normally, the X-Y Inhibit signal entering on pin 8 of P789 is LO (-0.6 V), Q722 and Q712 are off, and Q732 is on. The Aux Y-Axis signal (trace separation) on pin 1 of P790 is coupled through Q732 to the input of paraphase amplifier Q742 and Q752. Transistors Q748 and Q758 form a shunt-feedback amplifier with sufficient gain to drive the inputs of U762 (pins 5 and 11).

When the Readout System initiates a character display, it sets the X-Y Inhibit logic level HI (+1 V). Emitter follower Q718 turns Q722 on. The voltage on the collector of Q772 drops to zero which turns Q732 off and turns Q712 on. The Aux Y-Axis signal is then blocked by Q732. Y Readout signals are inverted by U705. Readout centering is added to the composite readout signal and then applied to the input of the paraphase amplifier via Q712. At the end of the character display period X-Y Inhibit returns to -0.6 V.

OUTPUT AMPLIFIER

The BEAMFINDER switch when depressed changes the current source for U862 to provide the BEAMFINDER function. Normally, the current source for U862 is supplied from the +15 V supply through Q862 and R862. However, when the BEAMFINDER switch is actuated, Q862 is turned off so the only current source for U862 is through R862. This limits the dynamic range of the stage by limiting its available current, so the display is compressed vertically within the crt graticule area.

Components Q878, VR878, and R878 clamp the output dc common-mode level to less than 44 V when the BEAMFINDER switch is depressed.

The signal at the output of U862 (pins 17 and 19) is connected via a flexible coplanar transmission line to the crt vertical deflector neck pins. A distributed deflector is used in the crt for maximum bandwidth. The signal travels along the deflector at a velocity essentially the same as the velocity of the electron beam passing through the vertical deflector. This synchronism of the deflection signal and the electron beam reduces the loss in high-frequency sensitivity due to electron-transit time through the deflector. After propagating along the deflector, the signal exits the crt via a second flexible coplanar transmission line and terminates in U883. A double-terminated transmission-line system, with a characteristic impedance of 200 ohms side-to-side, is formed by the output of U862, the two flexible lines, the crt vertical deflector, U883, and the crt vertical termination. Standing current for U862 is supplied from +50 V supply via U883 and the crt deflector transmission-line system.

POWER SUPPLY SHUTDOWN

The 23.9 V supply is monitored by the Power Supply Shutdown stage. When this voltage drops significantly, indicating an overload condition, Q864 will turn on pulling the gate of Q873 positive to cause Q873 to turn on. This action overloads the +50 V power supply which in turn causes the high-efficiency power supply to shutdown.

A drop in the +23.9 V supply may indicate either an open connection or a short to ground in the crt deflector transmission line system (or supply). The latter case is particularly serious and may damage U862, even with the Power Supply Shutdown stage operating. For this reason, care should be taken not to short or open the crt deflector connections when the instrument power is on.

The Power Supply Shutdown circuit also accepts an input from the Horizontal Amplifier circuit (diagram 11) via a thermal cutout, from pin 10 of P782. This input is normally about +14.8 V but will decrease if a fault occurs in the Horizontal Amplifier or if the thermal cutout opens. The latter case indicates excessive temperature in the Horizontal and Vertical Amplifier circuits which will significantly reduce amplifier operating life. The thermal cutout will open at about +55° C ambient if the fan is operating properly or at +35° C ambient if the fan is disabled or totally blocked.

10

HORIZONTAL CHANNEL SWITCH

A schematic diagram of the Horizontal Channel Switch is given on diagram 10, in Section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by a gray shaded line separating the circuitry into major stages. These stages aid in locating components mentioned here. Sub-headings in the following discussion use the stage names to further identify portions of the circuitry on diagram 10.

The Horizontal Channel Switch circuit determines whether the signal from the output of the A horizontal or B horizontal plug-in unit provides the horizontal deflection signal. This circuit also accepts an input from the Readout System (diagram 6) which blocks the horizontal signal while the readout display is presented on the crt.

CHANNEL SWITCH

The Channel Switch stage consists primarily of U962. The differential horizontal signal from the A HORIZ plug-in compartment is applied to pins 17 and 19. The differential horizontal signal from the B HORIZ plug-in compartment is applied to pins 7 and 9. The Display B control signal determines whether the A or B horizontal signal is coupled to the output pins 3 and 13.

Integrated circuit U962 has a standing current of approximately 37 milliamperes for each channel. The standing current in channel A is the quiescent current drawn by current sinks Q992 and Q994, and by R998 and R999. The standing current in channel B is the quiescent current drawn by current sinks Q962 and Q964, and by R968 and R969. The standing current in both channels is summed together in U962 and flows out of pins 3 and 13. This current is also the standing current for U1018 (see diagram 11), the Input Clamp. It is important to notice that the current sinks described above control the standing currents in both channels of the Channel Switch and the Input Clamp. This current comes from the +15 V supply primarily through R1047, R1043, R1067, and R1063 at the Channel Switch stage output. Thus the current sinks described above affect dc levels from the Channel Switch stage to the input of U1082.

HORIZONTAL CHANNEL SELECTOR

The Horizontal Channel Selector stage interfaces the Channel Switch stage, U962, to the logic signals arriving from the Main Interface (diagram 3). The Channel Switch stage requires two pairs of complementary control voltages, one pair for each channel. A HI control signal is +3.3 volts (emitter voltage of Q914). The complementary LO control signal is about +1.9 volts. To select a channel, the HI voltage is applied to the On input of U962 (pin 2 for Ch A, pin 12 for Ch B), and the LO voltage to the Off input (pin 1 for Ch A, pin 11 for Ch B).

When the HORIZONTAL MODE switch is set to B, the Display B line is HI (+1.1 V). This voltage is applied to one input, Q924C, of the differential pair (Q924C and Q924D) controlling the channel A input. Transistor Q924C is turned on and Q924D is turned off thereby inhibiting channel A. The LO level at the collector of Q924C turns Q924E off, and Q924B on, turning on channel B. When channel A is selected the Display B line is LO (-0.6 V), the opposite transistor in the two differential pairs above are on, and channel A is turned on, with channel B inhibited.

When the HORIZONTAL MODE switch is set to ALT or CHOP, the Display B signal switches between the HI and LO levels, at a rate determined by the Horizontal Binary stage in the Logic circuit (diagram 4). The X-Y Inhibit signal from the Readout System, diagram 6, applied to pin 7 of P882 has absolute control over the Horizontal Channel Selector stage. Quiescently, this signal is LO to allow the signal from the selected horizontal unit to pass to the output. However, when the Readout System displays infomation on the crt, this signal goes HI to block the signals from both horizontal compartments.

A AND B CHANNEL FEEDBESIDE

The operation of the A and B Channel Feedbeside stages are identical. Therefore, only a discussion of the A Channel Feedbeside is given.

The function of the A Channel Feedbeside stage is to compensate for low-frequency imperfections in the

frequency response of the Channel Switch stage, U962. Self heating of the transistor base-emitter junction, in some transistors within U962, causes the low-frequency gain to appear larger than the midband gain. To correct this, a portion of the input signal is picked off through R942 and R941 and applied to U944. The differential signal is converted to a single-ended signal and distributed into four RC (resistive-capacitive) networks, each having a different time constant. Resistors R945, R950, R952, R955, and R958 are adjusted to provide an accumulated waveform. This waveform is converted to a paraphase signal by Q962 and Q964, and is then injected into U962 through pins 6 and 4, where it is subtracted from the signal entering U962 at pins 7 and 9. Proper adjustment results in a flat-frequency response and optimum-transient response at the output, pins 3 and 13.

HORIZONTAL AMPLIFIER

The Horizontal Amplifier circuit amplifies the push-pull horizontal deflection signal from the plug-in unit installed in either horizontal compartment and connects it to the horizontal deflection plates of the crt.

A schematic diagram of the Horizontal Amplifier is given on diagram 11, in Section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by a gray shaded line separating the circuitry into major stages. These stages aid in locating components mentioned here. Sub-headings in the following discussion use the stage names to further identify portions of the circuitry on diagram 11.

READOUT POSITIONING

When readout is displayed, the X Readout signal is applied to the Horizontal Amplifier through P882. At the same time, the X-Y Inhibit signal (HI) causes Q1022 to conduct, turning Q1024 off. This action enables the horizontal readout center (R.O. CTR) adjustment R1025. Ungrounding the center tap allows R1025 to horizontally position the readout display on the crt.

OUTPUT AMPLIFIER

The Output Amplifier stage is a parallel path amplifier, having a fast path and a slow path. The fast path is a non-feedback amplifier, with 50 Ω impedance throughout, except at the output. The slow path is a feedback amplifier, used to correct thermal gain errors in the fast path, and also to inject the readout signal.

Fast Path

The fast path consists primarily of U1082 (the driver) and U1094 (the output amplifier).

The differential signal is applied to pins 7 and 9 of U1082. The input is 50 Ω push-pull (100 Ω differential). The gain of U1082 is set by the HF Gain adjustment R1082 providing a nominal current gain of about 3. The output of U1082 is applied to the input of U1094, the output stage. This stage has a 50 Ω push-pull input. Accordingly, the voltage gain through the driver will be about 3, since it has equal input and output resistances.

The output stage, U1094, has a current gain of about 3.3, and has a differential load impedance of 365 Ω. The voltage gain of the stage is then 12 (the current gain times the resistance gain).

The crt has a distributed horizontal deflection structure with a differential impedance of about 365 Ω. The crt horizontal deflection structure is connected to the amplifier output and to the horizontal terminator resistor via the 365 Ω flexible transmission lines. The termination board (A20) is adjustable to match the crt impedance.

Slow Path

The slow path is a feedback amplifier, and is used for correction of thermal errors inherent in the fast path. The slow path can be considered to be an operational amplifier, and will be described as such.

The input for the slow path is from R1044 and R1064 which picks off a fraction of the output signal from the Input Clamp stage. The input signal is amplified by Q1046 and Q1066 and injected into the operational amplifier summing nodes (base of Q1052 and Q1072). The output signal at the crt is picked off by a pair of 20 kilohm resistors within U1094. This signal is applied through R1034 and R1037 to the summing nodes. Any error signal at the summing nodes is amplified by the differential transistor pair Q1052 and Q1072 and further amplified by the differential transistor pair Q1058 and Q1078. The amplified signal is then injected into the fast path via pins 1 and 5 of U1082, to correct the signal applied to the crt.

The gain of the slow path is set with the LF Gain adjustment, R1062, independent of the fast path gain. The step response of the slow path is adjusted using the Delay adjustment (C1036) and S.P. Damp (R1073), the slow path damping adjustment.

Since the slow path is a feedback circuit, it can cause difficulties in locating problems in the Output Amplifier circuit. The feedback path can be disabled by removing Q1052 and Q1072, and then shorting the emitter run to collector run on the circuit board for each transistor. This can be done by inserting a U-shaped wire, the same diameter as the transistor leads, in the emitter and collector sockets. With the feedback path open, the amplifier will operate as before, with two exceptions. First, thermal errors will not be corrected; and secondly, readout is disabled since it is injected into the slow path. All dc voltages will remain essentially unchanged. This will simplify troubleshooting the Horizontal Amplifier.

INPUT CLAMP

The Input Clamp prevents the Ouput Amplifier stage from being overdriven. Signal limiting occurs in the Input

Clamp stage when the + and - horizontal signal, applied to pins 5 and 6 of U1018, approaches a level which will overdrive the transistors within U1094. The Input Clamp requires about 75 milliamperes from pin 16 to pin 5 and from pin 13 to pin 8 for proper operation. This current is supplied by the Channel Switch stage on diagram 10. Pins 13 and 16 are normally about +7.0 volts, and pins 5 and 8 about +6.2 volts.

The voltage at pin 6 of U1018 is set with the Clamp Adj adjustment R1005 at about 0.3 volts more positive than pins 5 and 8. Now, assume a differential signal is applied to pins 5 and 8 of the Input Clamp stage, with pin 5 going negative, and pin 8 going positive; clamping occurs when pin 5 goes negative enough to turn on the transistor inside U1018 with its emitter tied to pin 5. The signal from pin 5 flows through the transistor to pin 13, effectively shunting the excess signal to the other side of the differential line. In a like manner, the other transistor causes clamping when pin 5 is positive-going and pin 8 is negative-going. Note that both transistors are never on at the same time.

The Input Clamp stage output common-mode voltage is sensed at pin 15 of U1018 and applied to U1006. This causes the voltage at pin 6 to track the common-mode voltage in the Input Clamp stage, so that the clamping point does not change as the common-mode voltage changes.

The BEAMFINDER input goes from 15 volts to ground when the BEAMFINDER button is depressed. This raises the voltage at pin 6 of U1018 to cause the horizontal signal to be confined to the crt screen.

INTENSITY LIMITER AND Z-AXIS

A schematic diagram of the Intensity Limiter and Z-Axis is given on diagram 12, in Section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by gray shaded lines separating the circuitry into major stages. These stages aid in locating components mentioned here. Sub-headings in the following discussion use the stage names to further identify portions of the circuitry on diagram 12.

INTENSITY LIMITER

The gain of the microchannel plate is reduced in proportion to the logarithm of the charge output. In the area of sustained trace operation this gain reduction manifests itself as reduced writing speed. The Intensity Limiter stage limits the crt screen current and prevents long-term on-screen trace operation. Even with the Intensity Limiter stage, it is possible to incur distinguishable display gain loss, depending on the use of the instrument. For more information on proper usage see the Operating Instructions in this manual under: Reduction of Display Gain With Display Output Charge.

The Screen I Sense output of the Anode Multiplier stage, U1700 (diagram 13) carries a current which equals the average screen current. Operational amplifier U1952 with the 1 megohm feedback resistor R1951 converts this current to a voltage at the rate of 1 volt per microampere of average screen current. A divider string formed by R1952, R1959 and R1960 biases the inverting input of the operational amplifier U1958B at 0.2 volt. When the average screen current is larger than 0.2 microampere the noninverting input of the operational amplifier U1958B is greater than +0.2 volt and its output, TP1962, goes positive. This turns on the yellow LED, DS1970, through R1975 to indicate limited viewing time. Also, Q1974 is turned off, allowing C1971 to charge. In addition to this, the 3 hertz oscillator is started. Timer U1968 and its associated external components is set up such that it oscillates at a frequency of 3 hertz. When the output of operational amplifier U1958 goes positive, pin 4 of U1968 goes positive starting the oscillator.

Operational amplifier, U1970, with C1971 form an integrator, integrating the current through R1958. This resistor is connected to the output of operational amplifier U1952 so the current through R1958 is proportional to the screen current. The output of U1970 ramps down from ground. When the amplitude reaches -10 volts, the timer U1986 starts. How fast the output reaches -10 volts depends on the average screen current. As will be seen later, the average screen current cannot exceed 2 microamperes. At this level the output of the integrator reaches the -10 volt output level in about 2 minutes. Below average screen currents of 0.2 microamperes, Q1974 is on to prevent the integrator from operating. At an average screen current of 0.2 microamperes, the integrator reaches the -10 volt level in about 20 minutes. If the output of the integrator has not reached the -10 volt level and the average screen current drops below 0.2 microamperes, Q1974 turns on through R1974 to discharge C1971 giving the integrator a fresh start when the screen current again goes over the 0.2 microampere threshold.

When the output of the integrator reaches -10 volt and pin 2 of timer U1986 reaches about +2 volts the timing starts. The output, pin 3 of U1986, goes high but drops low again after 10 seconds when the timer has timed out. Capacitor C1985 determines the period of the timer.

When the timer starts (pin 3 goes high), the following occurs: With pin 3 of U1986 low, diode CR1991 clamps the drive of the red LED (DS1944) to ground. When pin 3 goes high, the red LED receives its current through R1969 and CR1993, and blinks at a 3 hertz rate to indicate that shutdown will occur in about 10 seconds.

Integrator capacitor C1971 is discharged, through divider R1988 and R1989 and the base of Q1980 is held at +2.4 volts. If pin 3 of U1986 is LO, Q1982 conducts and the collector voltage of Q1982 is too positive for transistor Q1978 to conduct. When pin 3 of U1986 goes high, Q1982 ceases to conduct and Q1978 turns on to discharge capacitor C1971, which allows the integrator a

fresh start. The waveform at pin 3 of U1986 is differentiated by C1993 and inverted by Q1997. Flip-flop U1992 is triggered on a positive going pulse, so, at the end of the 10 second timing interval U1992 is triggered and the output at pin 8 goes HI.

This output goes high to cause the following to occur:

(1) The Z-Axis turns off.

(2) The red LED is turned on steady, to indicate the shutdown of the Z-Axis system. Transistor Q1994 turns off when the Z-Axis Off signal goes HI and the red LED DS1944 is turned on steady from the +15 volt supply through R1994. Pin 2 of U1986 goes HI to inhibit the 10 second timer.

The Intensity Limiter stage can be reset several ways:

(1) By either pressing the RESET button S1988 before shutdown occurs, or by reducing the display intensity so that the average screen current is less than 0.2 microamperes.

If the RESET button is pressed before shutdown occurs, the base of Q1980 is shorted to ground, Q1981 turns off, and Q1978 conducts to discharge timing capacitor C1971.

If the screen current is below 0.2 microamperes, the output of the operational amplifier U1958B goes LO and Q1974 conducts, thereby discharging timing capacitor C1971 through R1974.

(2) By either pressing the RESET button S1988 during the 10 second delay before shutdown (when the red LED is flashing), or by reducing the intensity so that the average screen current is below 0.2 microamperes.

If the RESET button is pressed during the 10 second delay before shutdown occurs, the base of Q1980 is shorted to ground, Q1981 turns off, and Q1978 conducts to discharge timing capacitor C1971.

If the screen current goes below 0.2 microamperes during the 10 second delay before shutdown occurs, the output of operational amplifier U1958B goes LO, the base of Q1998 is pulled LO, Q1998 conducts and Q1999 is saturated. The saturation of Q1999 has the same effect as pressing the RESET button.

(3) By pressing the RESET button S1988 after shutdown occurs. During shutdown, Q1974 and Q1978 conduct discharging timing capacitor C1971 through R1974, and the 10 second timer is reset. Also, flip-flop U1992 is reset and the Z-Axis Off signal goes LO turning the Z-Axis back on.

If the average screen current exceeds 2 microamperes the output of operational amplifier U1952 exceeds +2 volts. Since the noninverting input of U1958A is biased at +2 volts, the output of this operational amplifier goes positive and diode CR1963 conducts. The current through Q1956 will increase and the voltage level of the intensity reference at TP1956 will increase from -10 volts to a more positive value. The intensity reference is connected to the A and B INTENSITY control network (see Mode Switch and Calibrator, diagram 2). If this reference goes more positive the input drive to the Z-Axis logic is reduced. Therefore, the beam current of the crt is reduced which results in a lower average screen current. If this feedback loop reaches equilibrium, then the voltage level of the intensity reference is such that the average screen current equals 2 microamperes. Single-shot screen currents are not limited to 2 microamperes since the feedback loop has a long time constant.

When the intensity limiter is limiting the average screen current to 2 microamperes the output of U1958A is high, with the result that Q1970 is driven into saturation. This causes the yellow LED to flash (indicates that the intensity is limited).

Figure 3-20 illustrates two operating conditions of the Intensity Limiter. The maximum viewing time period (approximately 20 minutes) is shown in Figure 3-20A; this condition occurs with the minimum average screen current of 0.2 microampere required to actuate the limited viewing time circuitry. The minimum viewing time (approximately 2 minutes) is shown in Figure 3-20B; this condition occurs when the intensity is limited to an average screen current of 2 microamperes.

Diodes are connected to the A and B INTENSITY controls to prevent interaction between the intensity controls when the HORIZONTAL MODE switch is set for ALT or CHOP operation (see Mode Switch and Calibrator, diagram 2). This interaction may occur when the display is alternating between time-base units. If either diode CR2019 or CR2009 is shorted, the following will occur: If the A INTENSITY control is advanced to the point where the Intensity Limiter stage limits the average screen current to 2 microamperes, the voltage level of the intensity reference becomes more positive than -10 volts. Also, the B intensity level is reduced. In the extreme case the reduction of the B intensity could be such that the B trace is not visible. Present limiting of the B intensity will only occur if diode CR2019 conducts. Diode CR2019 will conduct if the B intensity level is set high enough that the cathode of CR2019 is more negative than the intensity reference voltage level at the anode of CR2019.

Z-AXIS AMPLIFIER

The Z-Axis Amplifier stage controls the crt display intensity by varying the crt grid drive. The Logic circuit and the Readout System provide input signals to the Z-Axis Amplifier at J1606 and J1632 respectively.

The Z-Axis Amplifier consists of three stages; an impedance matching stage, a preamplifier, and output driver. The impedance matching stage consists of Q1618 and Q1608. This stage provides isolation between the

Readout and Logic inputs in addition to providing termination of the input coax cables. The collector current out of this stage is fed to the Auto Focus amplifier through R1606, developing a voltage signal to drive the Z-Axis preamplifier. Transistor Q1626 limits the voltage drive to the preamplifier by clamping the output of Q1608 at a level determined by Clamp Level adjustment R1226.

The Z-Axis preamplifier, a transconductance amplifier, consists of Q1632, Q1648, and Q1652, which provides a current drive for the output stage. Z-Axis Gain adjustment, R1637, sets the gain of this stage and is used to set the gain for the entire Z-Axis system. Adjustments R1635, C1635, and R1651 provide current peaking to the output stage for optimum transient response. The Z-Axis Level adjustment R1645 is used to adjust the Z-Axis baseline to the proper level. The preamplifier is disabled by a shutdown signal from the Intensity Limiter circuit, which saturates Q1644.

The output driver is a shunt feedback stage with gain set by R1660. Q1658, Q1668, Q1666 and Q1676 form a direct coupled amplifier with a high open loop gain; thus the input at the base of Q1658 is a virtual ground. These transistors are capable of providing high speed transitions in the negative going direction only. Fast positive transistions are achieved by peaking the base of Q1676 via Q1664 and T1664. Capacitor C1663 adjusts the drive to Q1676 for optimum response. Transistor Q1672 establishes the collector voltage supply for Q1676. VR1671, R1677, CR1675, and CR1678 provide protection from high transient voltages.

AUTO FOCUS

The Auto Focus stage maintains optimum focus of the crt display over a range of sweep speeds. The crt needs focus correction only at high Z-Axis drive conditions. Consequently, the output of the Auto Focus amplifier is ac coupled to the focus grid. The collector current of Z-Axis impedance matching stage, which consists of Q1618 and Q1608, is fed to the input of the Auto Focus amplifier, Q1603. The emitter voltage of emitter follower Q1607 is held steady at -8.6 volts. At zero volts, drive of the Z-Axis the collector current of Q1603 is maximum (8 milliamperes) which causes clamping diode CR1609 to conduct. At midrange Z-Axis drive, the collector current of Q1603 drops to 6 milliamperes and the voltage at the anode of CR1609 is -8.0 volts which causes the clamping diode CR1609 to barely conduct. For a Z-Axis drive over midrange, diode CR1609 becomes reverse biased and a negative going signal appears at the base of Q1617. The amplifier, consisting of Q1617 and Q1620, is noninverting and has a voltage gain of approximately four. The negative going signal at the collector of Q1620 is connected to emitter follower Q1629 and then ac coupled through C1628 to the focus grid.

CRT CIRCUIT

A schematic diagram of the CRT Circuit is given on diagram 13, in Section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by gray shaded lines separating the circuitry into major stages. These stages aid in locating components mentioned here. Sub-headings in the following discussion use the stage names to further identify portions of the circuitry on diagram 13.

CONTROL GRID DC RESTORER

The purpose of the Control Grid DC Restorer stage is to elevate the two low voltage grid control signals to a large negative potential. These inputs are the output signal from the Z-Axis amplifier, coupled through R1680 to the first input of the Control Grid DC Restorer stage and the crt grid bias (with its associated crt grid cut off warmup compensation circuit) coupled through R1748 to the second input of the Control Grid DC Restorer stage.

The Control Grid DC Restorer stage is current driven from the square wave at the high voltage winding through R1788, R1789, R1812, and R1811. When the voltage at terminal 9 of transformer T1770 goes positive diode CR1749 conducts at the voltage determined by the first input, the Z-Axis amplifier output level. This clamping action establishes the positive swing of the dc restorer drive. On the negative swing of T1770 diode CR1747 conducts at the voltage determined by the second input; the crt grid bias voltage. This clamping action establishes the negative swing of the dc restorer drive. The ac swing of the dc restorer is coupled from the low voltage section to the high voltage section by capacitor C1793. On the negative swing of the dc restorer drive, the high voltage end of C1793 is clamped to the -2400 volt supply by CR1794. On the positive swing of the dc restorer drive, CR1792 changes the high voltage end of C1792 to a voltage more positive than the -2400 volt supply by an amount equal to the sum of the absolute value of the voltages of the two inputs; the Z-Axis amplifier output voltage level and the grid bias voltage level.

The crt cathode voltage is 135 volts more positive than the -2400 volt supply, as determined by the Grid Bias Supply stage. Therefore, the grid is negative with respect to the cathode by 135 volts (minus the sum of the absolute values of the voltages of the Z-Axis amplifier output voltage level and the crt grid bias voltage level). The CRT Grid Bias adjustment R1746 is set with the Z-Axis amplifier output at the low level for the proper crt cutoff voltage. The CRT Grid Bias adjustment has a range of 50 volts.

The Grid Bias Supply stage not only helps to protect the crt during turn-on of the instrument (see description of the Grid Crow Bar circuit) but also when a malfunction of the Control Grid DC Restorer stage occurs. In the case of

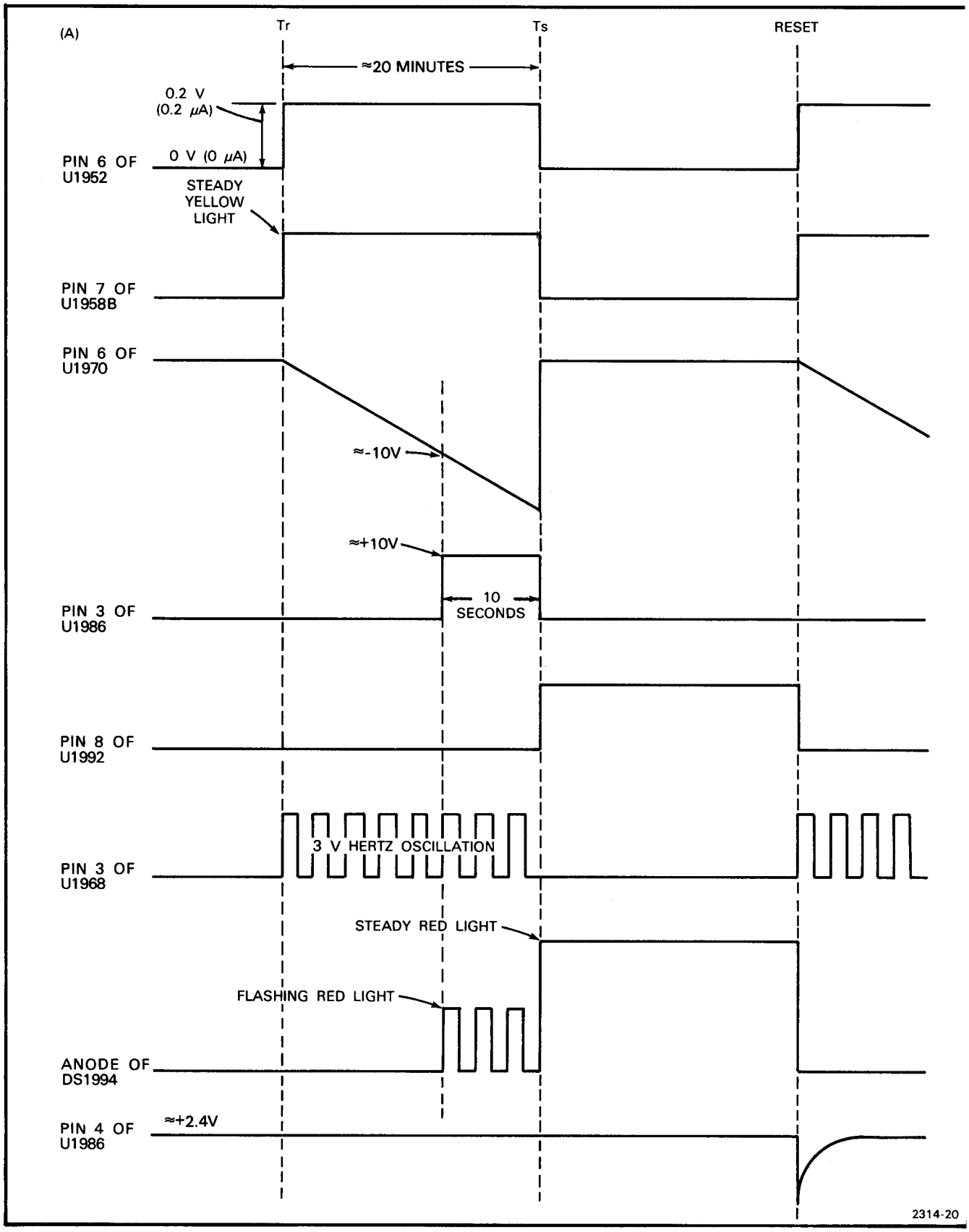

Figure 3-20. Theoretical timing diagrams for the Intensity Limiting stage.

(B)

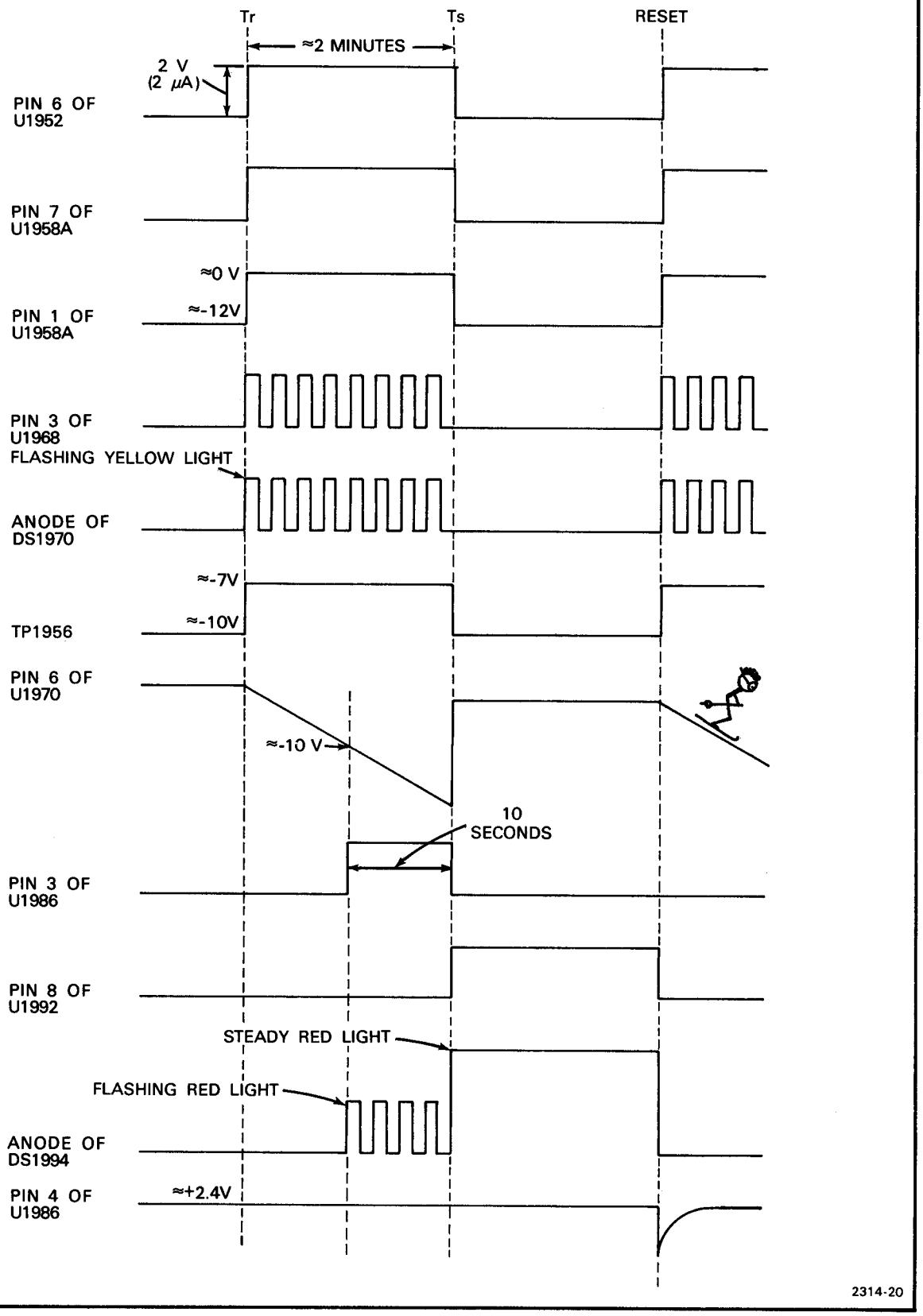

Figure 3-20. Theoretical timing diagrams for the Intensity Limiting stage (continued).

a malfunction, the grid will become more negative than the cathode, thereby turning the crt off.

Neons DS1792 and DS1794 as well as the various resistors in series with the diodes provide protection (voltage and current limiting) to the components of the Control Grid DC Restorer stage during turn-on and turn-off of the instrument, as well as protection from short circuits. Capacitor C1681 provides fast ac coupling between the Z-Axis Amplifier stage and the crt grid. The slower ac path is by way of R1680 and C1792.

FOCUS GRID DC RESTORER

The purpose of the Focus Grid DC Restorer stage is to elevate the low voltage focus control to a high negative potential.

The Focus Grid DC Restorer stage is current driven from the square wave at the high voltage winding through R1788, R1789, R1813 and R1814. When the voltage at terminal 9 of T1770 goes positive, CR1820 conducts at the voltage determined by the setting of FOCUS control R2005. This clamping action establishes the positive swing of the Focus Grid DC Restorer drive. On the negative swing of T1770, CR1816 conducts at ground. This clamping action establishes the negative swing of the Focus Grid DC Restorer drive. The ac swing of the Focus Grid DC Restorer is coupled from the low voltage section to the high voltage section by C1819. On the positive swing of the Focus Grid DC Restorer drive signal, the high voltage end of C1819 is clamped to the Focus Preset adjustment voltage by CR1819. During the negative swing of the Focus Grid DC Restorer drive, CR1818 charges C1818 to a voltage more negative than the Focus Preset voltage by an amount equal to the voltage set by the FOCUS control.

Neons DS1818, DS1819, and DS1820 and the resistors in series with the various diodes provide protection (voltage and current limiting) to the components of the Focus Grid DC Restorer stage during turn-on and turn-off of the instrument as well as short circuit protection.

The voltage from the FOCUS control passes through the BEAMFINDER switch. When this switch is depressed the input to the Focus Grid DC Restorer stage is grounded, thereby defocusing the display.

HIGH-VOLTAGE TRANSFORMER

High-Voltage Transformer T1770 provides pre-regulated voltages for the +2400 volt and -2400 volt high-voltage supplies, and 6.3 volts rms for the crt heater. The crt heater is elevated to the cathode potential through R1848. The high-voltage winding of T1770 also provides the drive to the Anode Voltage Multiplier, Focus-Grid DC Restorer and the Control-Grid DC Restorer stage.

ANODE VOLTAGE MULTIPLIER

Positive accelerating potential for the crt anode is supplied by the five-times voltage multiplier contained within U2012. The applied voltage to the input of U1700 from the high voltage secondary of T1770 is about 2500 volts peak-to-peak. This results in an output voltage of about 12.5 kilovolts at the crt anode. The output resistance of this supply is about 100 megohms and may be subject to meter loading when measured.

GRID BIAS SUPPLY

The Grid Bias Supply is a 135 volt power supply connected between the crt cathode and the -2400 Volt Supply. The polarity is such that the cathode is at a more positive potential (-2365 volts). The purpose of the cathode supply is explained in the Grid Crowbar circuit description.

The -2400 Volt Supply holds the current in the thick film high-voltage resistor R1802 constant at approximately 100 microamperes. The voltage developed across R1802C is 100 volts and is used as the voltage reference for the cathode supply. The comparator consisting of Q1835 and Q1838 requires both bases to be at the same potential. This condition is satisfied if there is 135 volts across the voltage divider of R1839 and R1840. If the voltage across the voltage divider R1839-R1840 is higher than 135 volts, the base voltage of Q1830 exceeds the base voltage of Q1835. Q1838 turns on harder; this in turn increases the current in the series regulator Q1842. This reduces the current through the voltage divider R1839 and R1840 lowering the voltage until it is 135 volts. The cathode supply furnishes current to the cathode, to the focus string, and to the resistor string which supplies the negative voltages to the scan expansion lens. Protection neons DS1842, DS1844 and DS1846 limit the maximum voltage across the supply.

MICROCHANNEL PLATE SUPPLY

The MCP (Microchannel Plate) Supply receives a 25 kilohertz square-wave signal of about 54 volts peak from the Control Rectifier circuit (diagram 14). If pin 1 of the transformer T1708 was grounded, the transformer would step this voltage up to 625 volts peak. Components C1711, CR1710, CR1711 and C1710 form a voltage doubler to develop 1250 volts dc at TP1175.

Assume that by some means the collector of Q1708 would be held at a +20 volt level. The 25 kilohertz square-wave signal is clipped by diode CR1708 to a maximum of +20.6 volts and clipped by diode CR1707 to a minimum of -0.6 volt at the cathode of diode CR1707. With the circuit in equilibrium the average current in capacitor C1707 must be zero. This is reached when C1707 is charged up to 10 volts. This means that a 25 kilohertz square-wave signal of 10.6 volts peak is on pin 1 of transformer T1708. This voltage is subtracted from the 54 volt peak drive at pin 2 of T1708, so the primary of the transformer is driven by a voltage of 43.4 volts peak. The dc output voltage is then reduced to about 1000 volts.

Components U1714A and Q1708 regulate the dc output voltage of T1175. Pin 2 of U1714A is at ground potential and is the current summing point for the regulator. If

there is zero current in R1722 and R1719, pin 2 of U1714A can only be at ground potential; when the dc output voltage at TP1171 is +562.5 volts. If pin 2 is above ground, the output of operational amplifier U1714A will go negative, turning off Q1708, this will charge C1708 more positive and reduce the primary drive of the transformer. This will result in a reduced dc output voltage at TP1175 until the voltage on pin 2 of U1714A returns to ground. Resistor R1722 carries the Intensity Sense current developed by the MCP Intensity Tracking stage on the Logic Schematic, diagram 4.

The Intensity Sense current varies between 0 and 50 microamperes depending on the setting of the INTENSITY control and gives the MCP Supply voltage a maximum increase of 375 volts. The higher the voltage across the MCP the greater the gain of the MCP (electrons out for electrons in) which results in a brighter crt display (this is needed at faster sweep speeds to obtain writing rate). MCP Gain adjustment R1720 sets the output voltage at TP1775; its range is 300 volts.

MCP Gain adjustment R1720 controls the writing speed of the instrument. At the factory this adjustment is set so that a single shot, 1 gegahertz sinewave with an amplitude of 7.5 divisions is visible when photographed using type 107 3000 ASA polaroid film (camera setting is f 1.9 at a reduction ratio of 1:0.85). If the MCP output voltage is set higher both the visual as well as the photographic writing rate increase, however a background scintillation of the MCP may appear on photographs. This effect randomly covers the photographs with small bright spots.

Depending on instrument use, increased MCP output voltage may reduce the display gain. Refer to: Reduction of Display Gain With Display Output Charge in the Operating Instructions section of this manual.

When the INTENSITY control is advanced, the MCP output voltage increases to produce a brighter crt display. This also causes the Readout display to be brighter which is undesirable. The purpose of U1714B is to prevent this. When the Intensity Sense current increases from 0 to 50 microamperes, the voltage at pin 5 of U1714B increases from 0 to 1 volt. The voltage at the emitter of Q1724 follows this voltage at pin 5 of U1714B. Therefore, the collector current of Q1724 (Aux RO Intensity current) increases from 0 to approximately 0.25 milliampere. Aux RO intensity current is subtracted from the Readout Intensity current to reduce the readout intensity current while the MCP output voltage increases. This results in a constant intensity of the readout display.

GRID BIAS

The Grid Bias stage provides a dc reference voltage to the Control Grid DC Restorer stage. This reference level is adjustable by means of the CRT Grid Bias adjustment R1746, which sets the grid cutoff voltage of the crt. The grid cutoff voltage drifts during warmup of the instrument; the purpose of U1736 and Q1742 is to compensate for this. Initially, at instrument turn on, capacitor C1736 is discharged, both inputs of the operational amplifier U1736 are at +7.0 volts, and a small current flows through R1733 which begins to charge capacitor C1736. The output of the operational amplifier U1736 is initially at +7.3 volts but gradually, after about 10 minutes, increases to +12.5 volts. Transistor Q1742 conducts until the voltage level at the output of the operational amplifier U1736 has increased to +12.5 volts. The current from Q1742 develops a voltage drop across R1747. Emitter follower Q1748 provides a voltage source reference for R1747. During warmup of the instrument the dc reference voltage to the Control Grid DC Restorer gradually becomes more negative and compensates for the grid cutoff voltage drift of the crt. When the instrument is turned off capacitor C1736 discharges with the same time constant (diode CR1736 prevents a fast discharge). If, after a few minutes the instrument is turned on again, less warmup compensation is required. This is accomplished by not allowing capacitor C1736 to discharge fast.

-2400 VOLT SUPPLY

Components C1750, CR1762, CR1763, and C1764 form a voltage doubler. A 1250 volt peak square wave is applied to the input of this doubler. The dc voltage at TP1844 is about -2500 volts if the voltage at the collector of Q1784 (TP2784) is near ground. Components U1802 and Q1784 form the regulator for the -2400 Volt Supply. Under nominal conditions the voltage at TP1784 is 100 volts. Diodes CR1776 and CR1778 alternately clip the waveform at pin 7 of the secondary winding of T1770 between the 100 volt level and ground level. The voltage across the secondary of T1770 is 1250 volts peak. With the waveform at pin 7, the voltage at pin 9 switches between 1250 and -1150 volts. This charges C1750 to 1250 volts and C1764 (at TP1844) to -2400 volts. To maintain equilibrium, the average current through C1788 must be zero. During one half of the cycle CR1778 conducts and draws current through C1778; during the other half CR1776 conducts, and CR1778 is turned off. The collector current from Q1784 that flows through C1778 is such that the total average current in C1778 equals zero. The voltage at TP1784 can only be pulled down by Q1784. The zener diode VR1784 limits the voltage at this test point to a maximum of 200 volts. This would happen if transistor Q1784 is removed.

Pin 3 of the operational amplifier U1802 is at ground potential and is the current summing point. If the current in R1804 and in R1806 is zero, pin 3 can only be at ground potential if the current in the thick film high voltage resistor R1802A, R1802B and R1803C is 100 microamperes. This produces a voltage of -2400 volts at TP1844. If the voltage at TP1844 is slightly more positive than -2400 volts, pin 3 of U1802 is above ground, the output (pin 6) goes more positive, Q1784 turns on harder pulling more current through C1778 to charge capacitor C1778 less positive. The voltage at TP1784 drops and, as a result, the -2400 Volt Supply is pulled back down toward -2400 volts dc. Regulation by means of this path is slow (several cycles of the 25 kilohertz square wave are required to make a correction), and C1786 provides for faster regulation. When Q1784 is turned on hard, current flows through C1784 and pulls down the -2400 Volt Supply.

The -2265 Adjust, R1805, sets the dc high voltage. Divider network R1800, R1803, R1804 and thermistor RT1804 vary the -2400 Volt Supply with changes in temperature. This means that the velocity of the electron beam through the vertical and horizontal crt deflectors changes, which in turn changes the vertical and horizontal deflection sensitivity. The change in deflection sensitivity compensates for gain change with temperature in the vertical and horizontal amplifiers.

A regulated +2400 volt supply (TP1754) is generated for use by the scan expansion lens. The -2400 Volt Supply regulator also regulates the +2400 volt supply, but for slow changes only, as was seen in the circuit description of the -2400 Volt Supply. Under nominal conditions for the -2400 Volt Supply regulator the collector of Q1784 is at 100 volts and the voltage at pin 9 of the high voltage transformer (T1770) switches at a 25 kilohertz rate, between +1250 volts and -1150 volts resulting in -2400 volts dc at the output of the -2400 Volt Supply. The voltage at the cathode of CR1762 switches between 0 volt and -2400 volts and is the input to the +2400 volt supply voltage doubler consisting of C1752, CR1752, CR1753 and C1754) causing the output at TP1754 to be +2400 volts dc. The scan expansion lens requires a lower voltage than +2400 volts. Since the lens draws zero current, a resistive divider can be used to bring the voltage down. Capacitors C1756 and C1800 filter the scan expansion lens voltage.

A semi-regulated +105 volts is generated for use by the Z-Axis amplifier. The input signal to transformer T1770 is connected to a voltage doubler formed by C1770, CR1772, CR1771 and C1774 to generate +105 volts dc at R1771.

The +105 volt supply develops a negative voltage across R1774, if overloaded. When the +2400 volt supply or the -2400 volt supply is overloaded a negative voltage is developed across R1776. The I Sense line is connected through P1785, pin 8, to the voltage Balance Sense line of the inverter control IC, in the power supply. This is a high impedance point, and when pin 2 is pulled 100 millivolts negative or positive the inverter control IC shuts down the power supply. Under overload conditions of the above mentioned supplies, either diode CR1774 or CR1775 will turn on and shut down the power supply.

GRID CROW BAR

The Grid Crow Bar stage prevents the crt grid from becoming more positive than the cathode during turn-on of the instrument. This action is needed to protect the crt cathode during the time that the cathode and grid voltages are settling. The grid voltage is forced more negative than the cathode by connecting the -2400 Volt Supply voltage to the crt grid through VR1688, Q1688, CR1687 and R1688 (during the period of time that Q1688 is on, which is primarily determined by C1687 and R1687). Initially, C1687 has no charge. When the instrument power is turned on C1687 receives charging current from the -2400 Volt Supply through the emitter-base junction of Q1688 and R1685. Transistor Q1688 remains on as long as the charging current through R1685 is large enough to cause VR1688 to conduct.

CRT

The 7104 crt is a high resolution, high frequency, micro-channel plate crt. Transformer T1770 has a secondary winding that supplies 6.3 volts to the crt heater. The crt heater is held at the cathode potential through R1848 and DS1848. The conventional oxide structured cathode is held at -2265 volts. The Z-Axis amplifier provides a maximum of 55 volts unblanking to the grid.

Incorporated into the first anode is an ion trap. Gas ions which might normally damage the cathode are drawn out of the anode and deposited on a gas absorbing surface. The demagnification lens (which works in conjunction with the primary focus lens) is operated at the cathode potential.

Stigmator adjustment R1894 is connected to the stigmator lens and is used to adjust the axis of astigmatism for optimum spot symmetry. The primary focus lens is connected to the output of the Focus Grid DC Restorer stage which contains the Focus Preset adjustment R1825. At high voltage Z-Axis drive a focus correction is required. Capacitor C1628 couples the focus grid voltage drive to the output of the Auto Focus amplifier. The front-panel screwdriver adjustment ASTIG (R2005) applies a voltage to the astigmatism lens. The front panel ASTIG and FOCUS controls are used in conjunction with each other to obtain best overall focus.

The vertical and horizontal deflectors are traveling wave deflectors. They are helical transmission line deflectors where the velocity of the input signal along the helical conductors is equal to the speed of light. The phase velocity along the length of the helix is matched to the crt electron beam velocity as it propogates along the helix. The impedance of the vertical deflector is 200 ohms, the deflection factor is 1 volt per division and the bandwidth is about 3 gigahertz. To minimize skin effect losses, the deflector is silver plated. The impedance of the horizontal deflector is 365 ohms, the deflection factor is 2 volts per division and the bandwidth is about 1.5 gigahertz. The connections to the vertical and horizontal deflectors are made through carefully spaced neck pins. The vertical deflector also employs stripline lead-ins between the deflector and the neck pins. Both deflectors use external termination resistors.

The 7104 crt utilizes a scan expansion lens. Without this lens, to obtain the desired scan size and deflector sensitivities, the crt would have to be over seven feet in length. In operation this lens is a strong positive lens in the vertical axis and causes the beam to cross over or invert the vertical deflection to cause vertical scan expansion of 4.5 times. In the horizontal axis the lens is a negative lens, which enhances the deflection of the beam. The horizontal scan is expanded 4 times. Seven potentials are required to operate the lens. The voltages are adjustable, differentially as well as the dc level. The adjustments on diagram 13 are labeled for their primary function, however, secondary effects are present:

Vertical Linearity adjustments R1854 and R1855 align the overall vertical linearity of the crt display. The

differential Vertical Linearity adjustment R1853 and R1856 align the keystone geometry effect of the crt. The Geometry adjustments R1864 and R1865 align crt vertical geometry. The differential geometry adjustments R1863 and R1866 align the top and bottom linearity of the crt display. Horizontal Sensitivity adjustments R1874 and R1875 sets the horizontal deflection factor. The differential Horizontal Sensitivity R1873 and R1876 aligns the center vertical line bowing.

The input of the microchannel plate (MCP) is held at ground potential and the output is connected to a variable positive supply thus providing the bias for the MCP. The higher the bias across the MCP the higher the gain or electron multiplication. Due to the MCP the instrument achieves its extremely high writing rate.

The MCP bias is adjusted with the INTENSITY controls. The bias across the MCP is held constant at INTENSITY control settings below about midrange, but it increases linearly from midrange to the fully clockwise position. Adjustment R1720 on the High Voltage board also adjusts the MCP output voltage. At the factory, this adjustment is set to achieve a photographic writing speed of 20 cm/nanosecond using a standard camera (f 1.9 lens) and standard film (Polaroid Type 107; 3000 ASA).

If the MCP output voltage adjustment is set high, both the visual as well as the photographic writing speed increase; however, on photographs a background scintillation may appear. At a high MCP bias setting the channels being excited by stray electrons can have an electron multiplication factor high enough to become visible on photographs. Depending on instrument use, increased MCP output voltage may reduce the display gain. Refer to Reduction of Display Gain With Display Output Charge in the Operating Instructions section of this manual. The MCP is located about 0.3 cm from an aluminized screen (with standard P31 phosphor crts). About 11.5 kilovolts is applied across this gap to accelerate the electrons exciting the MCP.

The orthogonality coil, wound on the crt neck at the exit of the vertical deflector, allows for correction of rotational alignment errors between the deflection axis and scan expansion lens. In addition to the orthogonality coil, a trace rotation coil is wound on the envelope of the glass ceramic interface.

CONTROL RECTIFIER

The Control Rectifier circuit provides the operating power for this instrument from an ac line-voltage source. A schematic diagram of the Control Rectifier is given on diagram 14, in Section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by gray shaded lines separating the circuitry into major stages. These stages aid in locating components mentioned here. Sub-headings in the following discussion use the stage names to further identify portions of the circuitry on diagram 14.

LINE INPUT

Power is applied through line filter FL1200, line fuse F1200, and POWER switch S1200. The line filter is designed to keep power-line interference from entering the instrument and to keep the approximate 25-kilohertz Inverter signal from entering the power line. Components R1205, C1205, and C1206 suppress reverse-recovery transients of CR1215.

The LINE VOLTAGE SELECTOR switch S1212 allows the instrument to operate from either a 115 volt nominal or a 230 volt nominal line voltage source. In the 115 volt position, rectifier CR1215 operates as a full-wave doubler with energy-storage capacitors C1215 and C1217, so the voltage across the two capacitors in series will be the approximate peak-to-peak value of the line voltage. For 230 volt operation, CR1215 is connected as a bridge rectifier and the voltage across C1216 and C1217 will be the approximate peak value of the line voltage. Thus, the dc voltage applied to the Inverter stage is about the same for either 115 volt or 230 volt operation.

Thermistors RT1209 and RT1213 limit the surge current when the power supply is first turned on. After the instrument is in operation, the resistance of the thermistors decreases so that they have little effect on the circuit. When the instument is turned off, the Inverter Control stage turns off the Inverter which prevents it from discharging C1216 and C1217; C1216 and C1217 discharge slowly through R1221 to allow for thermistor thermal-recovery time. This ensures sufficient thermistor resistance to limit the turn-on surge current to a safe level. Since C1216 and C1217 discharge slowly, dangerous potentials exist within the power supply for several minutes after the POWER switch is turned off. The presence of voltage in the circuit is indicated by relaxation oscillator R1219, C1219, and DS1219. Neon bulb DS1219 will blink until the potential across C1216 and C1217 drops to about 80 volts.

Spark gap electrodes E1208 and E1213 are surge-voltage protectors. When the LINE VOLTAGE SELECTOR switch is in the 115 volt position, only E1208 is connected across the line input. If a peak voltage greater than 230 volts is present on the line, E1208 will conduct and quickly open line fuse F1200 to interrupt the input power before the instrument can be damaged. In the 230 volt position, E1208 and E1213 are connected in series across the line input to provide protection for peak voltages greater than 460 volts.

Transformer T1208 provides a sample of the line voltage to the plug-in connectors for triggering at line frequencies. This line frequency signal is also connected to the Inverter Control stage to sense when line voltage is present.

INVERTER START NETWORK

Network R1210, R1238, and C1235 is connected between the input line (ac) and the negative side of C1217 (through T1225). Capacitor C1235 charges on each cycle of the input line voltage. When the charge on C1235 reaches about 33 volts, zener diode VR1238 turns

on and programmable unijunction transistor Q1238 starts conducting to provide base drive to turn on Q1241 through C1239. When Q1241 turns on, it shock-excites series-resonant network L1237 and C1237 to generate a damped oscillation. This damped oscillation provides the drive necessary to start the Inverter switching action. After the Inverter is operating, the recurrent waveform at the collector of Q1241 keeps C1235 discharged through CR1249, thus disabling the Inverter Start Network while the instrument is on.

INVERTER

The Inverter stage converts the dc voltage across C1216 and C1217 to a sine-wave current to drive power transformer T1310. Once the Inverter has been started by the Inverter Start Network, transformer T1230 provides feedback to the bases of Q1234 and Q1241 to sustain oscillation. These transistors operate at a forced beta of 4 due to the turns ratio of T1230. Also, T1230 provides a 60:1 turn center-tapped winding for pre-regulation and fault protection shut-down. The Inverter Control stage short circuits one-half of this winding to either delay the turn-on of Q1234 and Q1241 or to completely stop their switching action.

The switching action of Q1234 and Q1241 generates a square-wave voltage with an amplitude approximately equal to the dc voltage at the input to this stage. The square-wave voltage at the emitter of Q1234 supplies the drive necessary to maintain a sine-wave current in the series-resonant network of L1237 and C1237. Diodes CR1234 and CR1241 provide paths for series-resonant current when Q1234 and Q1241 are held off for pre-regulation.

To aid in understanding circuit operation, Figure 3-21A shows a representation of the Inverter stage as a switch. The three possible states of the Inverter are depicted by the three possible switch positions: Q1234 is on in position (a); Q1241 is on in position (c); or both transistors are held off for pre-regulation in position (b). In the composite current waveform of Figure 3-21B, the relative phase and amplitude of each component of I_t is shown for periods T_a, T_b, and T_c corresponding to the three switch positions. Figure 3-21C and Figure 3-21D show the relationship of the Inverter voltage and primary winding voltages with respect to the current waveform.

The normal sequence of operation is as follows: Assume that I_t is passing through zero and is increasing in the direction which forward biases CR1241 to conduct I_1 as shown in Figure 3-21B. When the Inverter current crosses through zero the Inverter Control stage holds off Q1234 and Q1241. At a time determined by the Inverter Control stage, Q1234 is allowed to conduct I_2 which reverse bias CR1241. Transistor Q1234 conducts as I_2 goes through its peak and back to zero. At zero crossing the Inverter Control stage again holds off Q1234 and Q1241. During this hold-off time, CR1234 conducts I_3. Next, Q1241 is turned on to conduct I_4 which reverse biases CR1234. Transistor Q1241 conducts as I_4 goes through its peak and back to zero. The cycle then repeats itself.

During conduction of Q1234 power is delivered to the series resonant circuit L1237-C1237, and to T1310. Part of this power, stored in the resonant circuit, is returned to the supply when diode CR1234 conducts. Pre-regulation is achieved by varying the holdoff of the inverter transistors, T_b in Figure 3-21B, thereby determining the net power delivered to T1310.

OVER-VOLTAGE STOP

Whenever the voltage across the primary of T1310 exceeds a safe level, the Over-Voltage Stop stage shuts down the Inverter to protect the Inverter components from damage. For example, this stage activates whenever the normal voltage regulating path through Q1252 and T1230 is inoperative.

Capacitor C1243 charges through CR1244 to the peak voltage across the primary of T1310. If this voltage exceeds a safe level, Q1245 conducts to cause Q1243 and Q1246 to turn on. When Q1246 turns on, the base-drive winding of T1230 is short-circuited, which stops the Inverter switching action. Since Q1243 is turned on, C1235 in the Inverter Start Network is prevented from charging to the breakdown voltage of CR1238, thus preventing the Inverter from starting. Transistors Q1245 and Q1243 continue to conduct until the discharge current of C1243 through R1243 drops below the holding current of Q1245. After Q1243 turns off, CR1249 continues to inhibit the Inverter Start Network while C1243 charges through R1244 and CR1244. When the voltage on C1243 is sufficient to turn on CR1238, the Inverter will start.

INVERTER CONTROL

The Inverter Control stage, made up of primarily U1275, provides pre-regulation and fault protection functions. For pre-regulation purposes, U1275 varies the hold-off time T_b, in Figure 3-21B of the Inverter switching transistors.

Under normal operating conditions, only the E Sense input at pin 15 controls the hold-off time. However, various fault conditions can affect hold-off time or stop Inverter operation altogether. The operation of each individual function of the Inverter Control stage is described in the following discussion.

Pre-Regulator

The Pre-Regulator operation of U1275, maintains constant voltage at the outputs of the low-voltage rectifiers. It also provides constant peak-to-peak voltage to the high-voltage supply.

Transformer T1235 provides Inverter phase information and power to U1275. The phase information is connected to pins 10 and 11 through C1277 and C1278. Bridge rectifier CR1272, CR1274, CR1276, and CR1275, provides positive and negative operating voltages to U1275. A shunt regulator in U1275 maintains the +7.5 volts at pin 6. The -2 volt (nominal) supply connected to pin 7 is unregulated. Zener diode VR1272 is for protection against open circuit conduction (U1275 removed) and is normally not conducting.

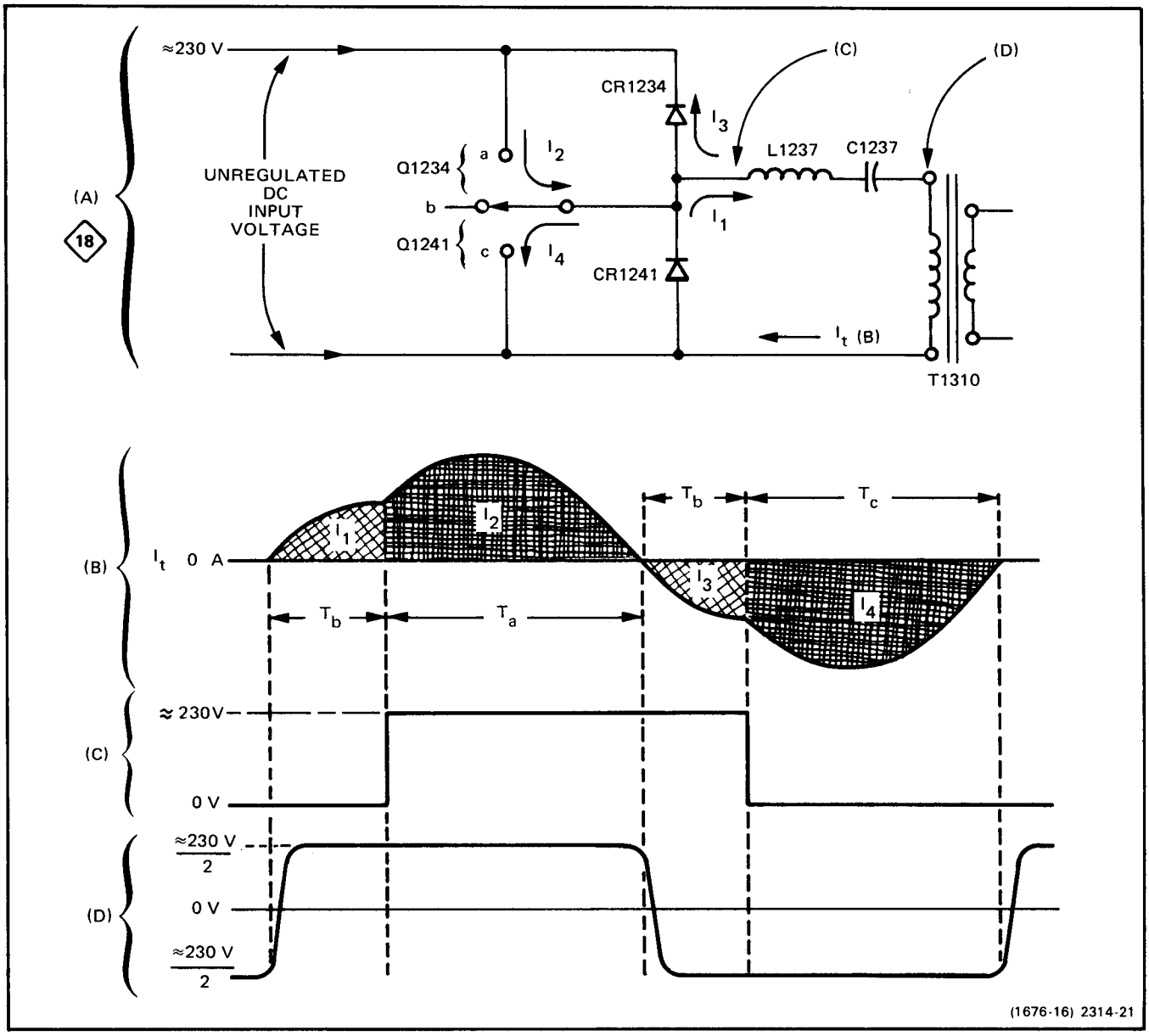

Figure 3-21. (A) Representation of Inverter stage. Idealized waveforms of (B) total inverter current, I_t, (C) voltage of CR1234 and CR1241, and (D) voltage across primary.

Pin 15 is the voltage sensing (E Sense) point of the Pre-Regulator circuit. Zero volts at pin 15 indicates proper regulation. Zener diode VR1272 provides a stable reference voltage for the sensing-divider resistors R1292, R1293, R1295, R1286 and R1287. Resistor R1295 in this divider adjusts the ratio of the divider to adjust the output of the +108 volt supply. Outputs of the other supplies are then set by the turns ratio of T1310.

Integrated circuit U1275 regulates the Inverter by varying the hold-off time of the switching transistors, Q1234 and Q1241. A variable pulse-width monostable multivibrator in U1275 is triggered at pins 10 and 11 whenever the Inverter current changes direction. The pulse width holds off the Inverter by turning on transistor Q1252 through pin 9 of U1275, thus shorting out the base drive to Q1234 and Q1241. The pulse width, and therefore hold-off, is controlled by a ramp at pin 12. If the voltage at the E Sense input, pin 15, is too low, the ramp is not allowed to rise very high and the pulse width and hold-off are short. As the E Sense voltage rises, the ramp is allowed to rise to a higher voltage level, increasing the hold-off time.

Fault Protection

The fault-protection portions of U1275 provide protection for the power-supply components from damage due to

short circuits, turn-on surge currents, and other malfuncions. When a fault is detected at the Fault Sense input (pin 2) or I Sense input (pin 13), a current from the Fault Holdoff Time output (pin 1) charges C1264. If the detected fault lasts longer than about 10 milliseconds, C1264 will charge positive enough to initiate a positive output at pin 8. This output turns on Q1254 and Q1252 which turns off the Inverter. The Inverter will remain off while C1254 discharges through R1254 which keeps Q1254 and Q1252 turned on. The Inverter restarts in roughly 500 milliseconds when the current through R1254 is insufficient to keep Q1254 and Q1252 turned on. When the inverter restarts, C1254 is recharged through CR1259 and R1259. This cycle repeats until the fault is corrected, with the Inverter on for about 10 milliseconds, and off for about 500 milliseconds.

Inverter Current Limiter

The Inverter Current Limiter provides protection for the Inverter components from damage due to excessive current turn-on or short circuits. Operation of this stage is similar to the Pre-Regulator (voltage regulation). The Inverter Current Limiter takes control of the Inverter hold-off time whenever pin 13 starts to go negative. T1235 is a current step-down transformer. The current is rectified and flows through R1284, the current-sensing resistor. The voltage across R1284 is negative and proportional to the Inverter current. The I Sense input at pin 13 is normally held positive through divider R1281 and R1283. The Inverter Current Limiter takes control of regulation when pin 13 approaches zero volts. Peak Inverter current is limited to about 5 amperes. If the voltage at pin 13 remains near zero for more than about 10 milliseconds, pin 8 will go positive to turn off the Inverter.

Fault Sense

The Fault Sense portion of U1275 provides overload protection for those supplies on the LV Regulator schematic, diagram 15, and other supplies generated throughout the instrument. Resistive networks from supplies are connected to the Fault Sense input at pin 2 of U1275. During normal operation, the voltage at the Fault Sense input remains near zero. If one of the inputs changes sufficiently to cause this voltage level to vary 200 millivolts (positive or negative) for more than 10 milliseconds, a positive output is produced at pin 8 of U1275 to stop the Inverter.

Line Stop

The Line Stop portion of U1275 stops the Inverter when the POWER switch is turned off. The Line Stop stage will also stop the Inverter if the ac line voltage falls below a minimum value.

The line-frequency signal from transformer T1208 is connected to pin 4, the Line Stop Sense input of U1275. During normal operation, the line-frequency signal causes the Line Stop Timer terminal (pin 3) to periodically discharge to ground. When the line-frequency signal is interrupted or falls below a minimum value, C1267 will charge to approximately +0.7 volt causing the Line Stop stage to produce a positive output at pin 8 of U1275 to stop the Inverter.

POWER ON LOGIC

When the instrument is first turned on, the Power On Logic circuit produces a LO output on Pin 6 of U1374B for about 2 seconds, after which time, a HI is produced, indicating that power is on. Pin 6 of U1374B goes HI after C1371 charges sufficiently to reduce the voltage on pin 13 of U1374 to the LO state.

When the instrument is turned off this circuit produces a LO output before the regulated power supply voltages begin to drop. The Inverter Stop signal, pin 8 of U1275, goes HI allowing Q1362 to produce a LO at pin 6 of U1374B. The Power On Logic circuit is not used by the 7104.

15

LV REGULATOR

A schematic diagram of the Low-Voltage Regulators is given on diagram 15, in Section 8 of this manual (Diagrams and Circuit Board Illustrations). The schematic is divided by gray shaded lines separating the circuitry into major stages. Sub-headings in the following discussion use the stage names to further identify portions of the circuitry on diagram 15.

The Low-Voltage Regulators convert semi-regulated voltages from the Control Rectifier circuit to stabilized low-ripple output voltages. The regulators are series type, using the +50 volt supply as a reference.

OPERATIONAL AMPLIFIER POWER SUPPLIES

The operational amplifiers, used to regulate the +50, +15, +5, -50, and -15 volt supplies, require that four special voltages be generated for their operation:

(1) The +22 volt supply is generated from the semi-regulated +54 volts by reference zener diode VR1432 and emitter follower Q1434.

(2) The -22 volt supply is generated from the semi-regulated -54 volts by reference zener diode VR1435 and emitter follower Q1438.

(3) The +5.6 volt supply is generated from the semi-regulated +17 volts by zener diode VR1552.

(4) The -5.6 volt supply is generated from the semi-regulated -17 volts by zener diode VR1556.

+50 VOLT SUPPLY

Semi-regulated +54 volts from the Control Rectifier circuit provides the unregulated voltage source for this supply. Operational amplifier U1415 is connected as a differential amplifier to compare the feedback voltage at pin 2 against the reference voltage at pin 3. The error output at pin 6 of U1415 reflects a difference between these two inputs. Zener diode VR1412 sets a reference level of about +9 volts at pin 3 of U1415. A sample of the output voltage from the +50 Volt Supply is connected to pin 2 of U1415 through divider network R1416, R1415, and R1414. Resistor R1415 in this divider is adjustable to set the output level of this supply. Notice that the feedback voltage of this divider is obtained from a line labeled +50 V Sense. If the feedback voltages were obtained at the supply, the voltage at the load would not stay constant, due to the inherent resistance of the interconnecting cable between the supply and its load. The Sense configuration overcomes this problem by sensing the voltage at the load. Since the current in the Sense line is small and constant, the load voltage is held constant regardless of the load current.

Regulation of voltage occurs as follows: If the output level of this supply decreases (becomes less negative) due to an increase in load or a decreased input voltage (as a result of line-voltage change or ripple) the voltage across divider R1416, R1415, and R1414 decreases also. This results in a less positive level at pin 2 of U1415 than that established by zener diode VR1412 at pin 3 of U1415. This decreases the current through CR1415 and VR1417, causing a successive increase in current through the base-emitter junction of Q1428. This results in increased conduction of Q1428, the +50 volt series regulator. The load current increases and therefore the voltage across the load also increases (becomes more positive) sufficiently to balance the input into differential amplifier U1415. The +50 Volt adjustment, R1415, sets the output level of this supply.

Current limiting is provided for the +50 Volt Supply if excessive current is demanded from the supply. Since the load is connected to this supply through R1428, all current from the +50 Volt Supply must flow through this resistor. Under normal operation there is insufficient voltage drop across R1428 to turn Q1422 off. However, when excessive current is demanded from the +50 volt series regulator (Q1428) due to a short circuit or similar malfunction at the output of this supply, the voltage drop across R1428 increases until it is sufficient to reverse bias Q1422. The reduced collector current of Q1422 results in a reduction of current through Q1428. This current limiting protects Q1428 from damage due to excessive power dissipation.

Several protection diodes are also included in this circuit. Diode CR1428 prevents the output of this supply from going more negative than about -0.6 volt if it is shorted to a negative supply. Zener diode VR1410 and diode CR1410 supply a turn-on voltage for U1415 to start the +50 Volt Supply when the instrument is first turned on. As soon as the +50 Volt Supply turns on, CR1410 stops conducting.

-15 VOLT SUPPLY

Basic operation of all stages in the -15 Volt Supply is the same as for the +50 Volt Supply. The reference level for this supply is established to ground through R1482 at pin 5 of U1484B. The divider ratio of R1480 and R1481 sets a level of zero volts at pin 6 of U1484B. The level on the +50 V Sense line is held stable by the +50 Volt Supply. Any change at the output of the -15 Volt Supply appears at pin 5 of U1484B as an error signal. The output voltage is regulated in the same manner as described for the +50 Volt Supply. Diode CR1496 limits the output of this supply from going more positive than about +0.6 volt if it is shorted to one of the more positive supplies. Operational amplifier U1484A provides short circuit protection for Q1494 by monitoring the voltage drop across R1495. When too much current is demanded from the supply the increased voltage drop across R1495 allows U1484A to turn Q1488 off, in turn reducing the current through Q1494.

+5 VOLT SUPPLY

The operation of the +5 Volt Supply is basically the same as described for previous supplies. Error voltage to pin 2 of U1514A is provided through R1531 to pin 2 of U1514A; pin 3 is referenced to the +50 V Sense line. The divider ratio of R1513 and R1514 is 10:1, so pin 3 of U1514A is at +5 volts when the supply is operating normally. The level on the +50 V Sense line is held stable by the +50 Volt Supply. Therefore, any change at the output of the +5 Volt Supply appears at pin 2 of U1514A as an error signal. The output voltage is regulated in the manner described previously for the +50 Volt Supply. Diode CR1532 limits the output of this supply to about -0.6 volt if it is shorted to one of the negative supplies.

The +5 volt current limiting is accomplished by U1514B, which protects this supply from excessive output current damage. With normal supply current through R1533 and R1534, the voltage drop is such that the base of Q1518 is biased on. If the current through R1533 and R1534 increases above a safe level, pin 7 of U1514B reduces the forward bias current to Q1518. Now, the base current of Q1522 is reduced which decreases the voltage on the base of Q1526. This limits the conduction of Q1526 to a safe current level.

+15 VOLT SUPPLY

The +15 Volt Supply regulates in the same manner as the +50 Volt Supply; current limiting operates in the manner described for the +5 Volt Supply. Error feedback voltage to pin 2 of U1464A is provided through R1469. Pin 3 of U1464A is referenced to the +50 V Sense line. The divider ratio of R1461 and R1462 sets pin 3 of U1514 at +15 volts. Any change in the output level of the +15 Volt Supply appears at pin 2 of U1464A as an error signal. This results in an opposite change at the output (pin 1 of U1464A) which is conveyed to the +15 volt series regulator (Q1474 through CR1464 and Q1468) to correct the error in the output voltage of the supply. Diode CR1476 limits the output of this supply to about -0.6 volt if it is shorted to one of the negative supplies.

-50 VOLT SUPPLY

Operation of the -50 Volt Supply is basically the same as described for the +50 Volt Supply; current limiting operates in a similar manner as described for the +50 Volt Supply. Error voltage to pin 2 of U1445 is provided by divider R1445-R1446, and is referenced to the -50 V Sense line, from the +50 V Sense line. The divider ratio of R1445 and R1446 sets the level at pin 2 of U1445 at zero volts when the output of this supply is correct. Protection diode CR1458 limits the output voltage of this supply to +0.6 volt should the supply be shorted to a positive supply.

FAN CIRCUIT

The fan motor used in this instrument is a brushless dc motor, using Hall Effect devices. The 2 Hall Effect devices sequentially drive the 4 transistors (U1690 A, B, C, and D) which, in turn, control the current flow through the 4 field windings. The fan motor speed is regulated by limiting the current flow through Q1698. Diodes CR1691, CR1692, CR1694, and CR1696 rectify the back emf produced by the 4 field windings. This voltage is applied to the base of Q1698 through resistive divider network R1697, R1695, RT1696 and R1698; the voltage developed by this circuit is proportional to the motor speed. If the motor speed starts to increase, the current drive to the base of Q1698 will decrease, reducing the current to the motor, thus maintaining a constant motor speed. As the temperature increases the value of thermistor R1696 decreases reducing the base voltage of Q1698; Q1698 then conducts more current and the speed of the motor is increased.

GRATICULE-LIGHT SUPPLY

The Graticule-Light Supply provides power to illuminate the graticule lights. The front-panel GRAT ILLUM controls the output of this supply to set the brightness of the graticule lights. Transistors Q1544, Q1548, and diode CR1548 form a pseudo-differential amplifier. The output voltage at the collector of Q1548 follows the voltage set at the base of Q1544 by the divider made up of R1542, R1541, R1543 and the GRAT ILLUM control R1900 (see diagram 7). Resistor R1548 limits the output current from this supply to protect Q1548 from damage due to a short circuit.

16

DELAY COMP (OPTION 2)

A schematic diagram of the Delay Compensation circuit is given at the rear of Section 8 in this manual (Diagrams and Circuit Board Illustrations). The X-Y Delay Compensation network (Option 2 only) provides a delay for the horizontal (X) signal from the B HORIZ plug-in compartment to match the delay of the vertical (Y) signal due to the Delay Line (see diagram 8). The Horizontal (X) signal from the A HORIZ plug-in compartment is coupled directly to the horizontal channel switch, diagram 9, without a delay compensation network.

TIME-BASE OPERATION

When the plug-in unit installed in the B HORIZ compartment is operated as a standard time-base unit to produce a horizontal sweep for deflection of the crt beam, the Delay Compensation network is effectively disabled. The X Compensation Inhibit (B) line is open (through pin 5 of P984); relays K1112-K1162 are not actuated. Therefore, the relay contacts remain in the normally-closed position so the horizontal signal passes directly through this network to the Horizontal Channel Switch.

X-Y OPERATION

If the time-base unit installed in the B HORIZ compartment is operated as an amplifier, or if an amplifier unit is installed in the B HORIZ compartment, the X-Compensation Inhibit (B) line, through pin 5 of P984 is held at ground. This actuates relays K1112-K1162 to connect the delay compensation network into the circuit. The B horizontal signal then passes through the X-Y Delay Compensation circuit and through the Delay Line. The horizontal signal is delayed to match the vertical signal, and the losses in the Delay Line are compensated for on the X-Y Delay Compensation circuit board.

As the B horizontal signal passes through the X-Y Delay Compensation stage, U1140 provides gain and frequency compensation. Gain of the stage is determined by R1120. Components R1110, R1112, R1113, R1114 and C1114 are adjusted for optimum step response. Centering adjustment R1105 balances the dc level of the signal. The front corner of the step response is adjusted with R1157. Standing current for U1140 is provided by the +15 Volt Supply through R1152, R1150, and R1161. The current is returned through emitter long tail resistor R1103 and R1104. Operational amplifier U1166A is a +3 volt supply for the output bases of U1140. Operational amplifier U1166B and transistor Q1166 form a regulator which holds the common-mode output voltage of the amplifier at zero volts.

The X-Y Delay Compensation network is an optional feature. For instruments which are not equipped with this feature, the B horizontal signal from the B HORIZ plug-in compartment is connected directly to the Horizontal Channel Switch through the Horizontal Interconnect board.