INSTRUCTION MANUAL

7503 OSCILLOSCOPE

MANUFACTURERS OF CATHODE-RAY OSCILLOSCOPES

INSTRUCTION MANUAL

Serial Number B090834

7503 OSCILLOSCOPE

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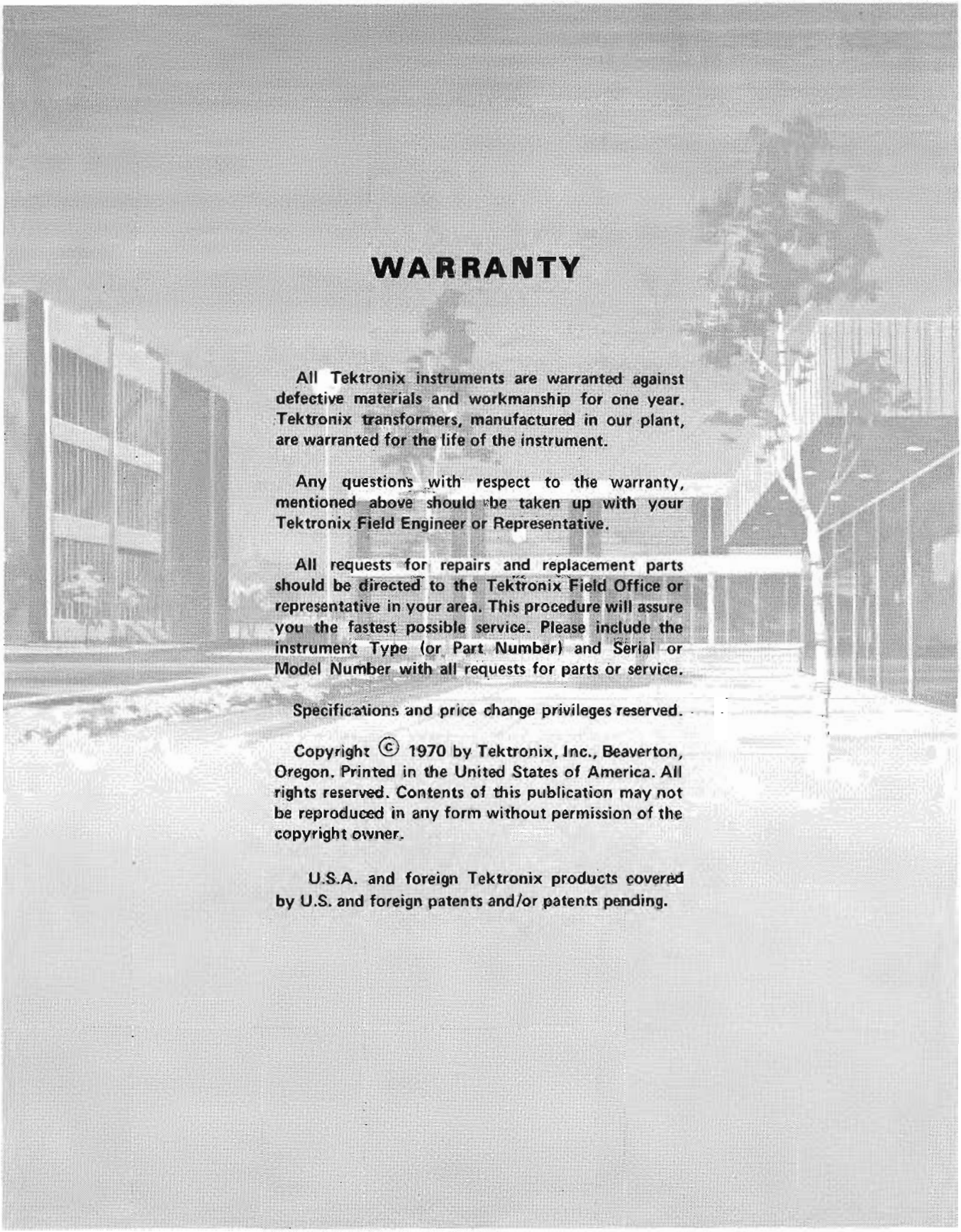

WARRANTY

All Tektronix instruments are warranted against defective materials and workmanship for one year. Tektronix transformers, manufactured in our plant, are warranted for the life of the instrument.

Any questions with respect to the warranty, mentioned above should be taken up with your Tektronix Field Engineer or Representative.

All requests for repairs and replacement parts should be directed to the Tektronix Field Office or representative in your area. This procedure will assure you the fastest possible service. Please include the instrument Type (or Part Number) and Serial or Model Number with all requests for parts or service.

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U.S.A. and foreign Tektronix products covered by U.S. and foreign patents and/or patents pending.

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Abbreviations and symbols used in this manual are based on or taken directly from IEEE Standard 260 "Standard Symbols for Units", MIL-STD-12B and other standards of the electronics industry. Change information, if any, is located at the rear of this manual.

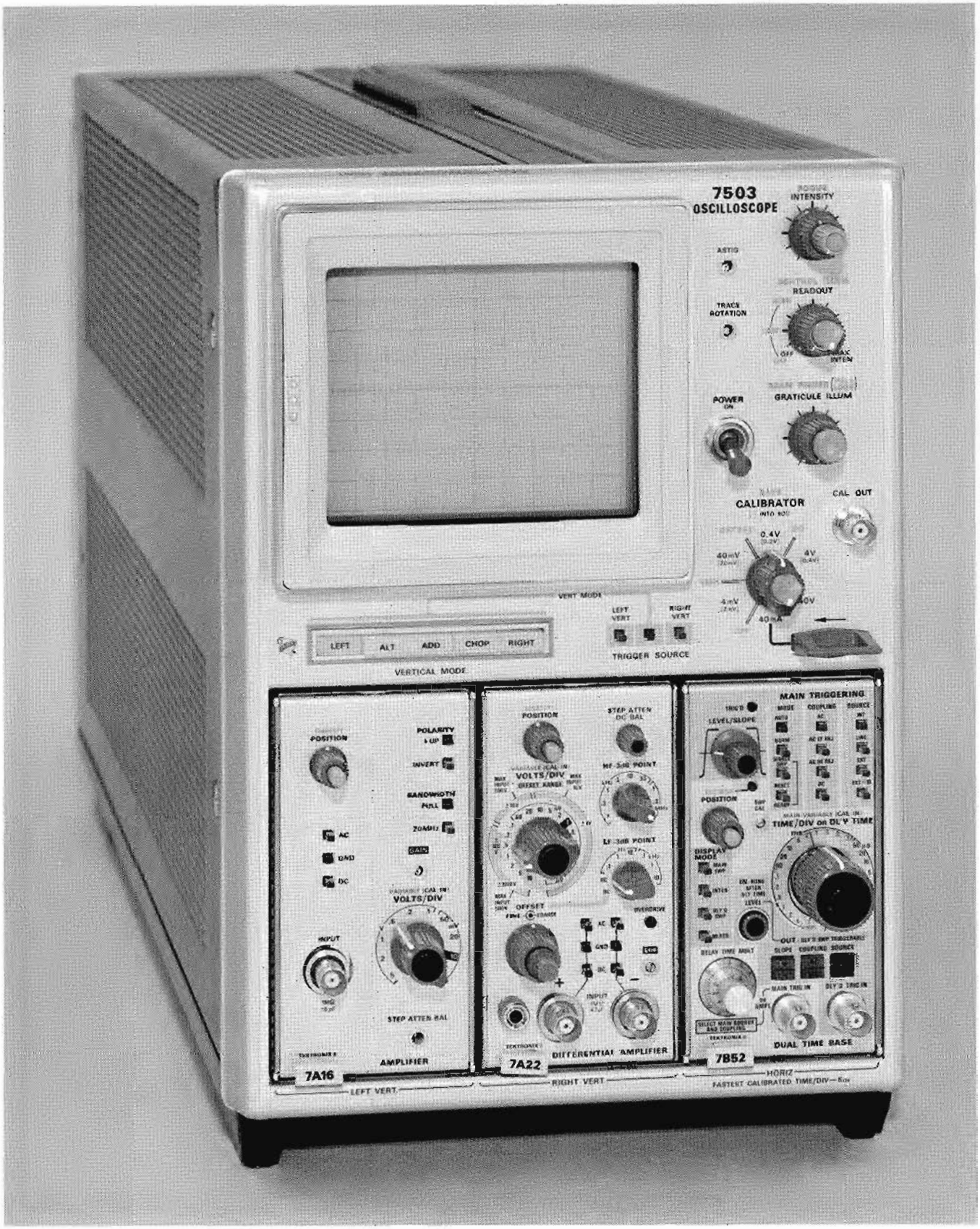


Fig. 1-1. 7503 Oscilloscope.

SECTION 1
7503 SPECIFICATION

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

The Tektronix 7503 Oscilloscope is a solid-state, high performance instrument designed for general-purpose applications. This instrument accepts Tektronix 7-series plug-in units to form a complete measurement system. The flexibility of this plug-in feature and the variety of plug-in units available allow the system to be used for many measurement applications.

The 7503 has three plug-in compartments. The left and center plug-ins are connected to the vertical deflection system. The right plug-in is connected to the horizontal deflection system. Electronic switching between the plug-ins connected to the vertical deflection system allows a dual-trace vertical display. This instrument features regulated DC power supplies to assure that performance is not affected by variations in line voltage and frequency, or by changes in load due to the varying power requirements of the plug-in units. Maximum power consumption of this instrument is about 260 watts (60 Hertz, 115-volt line).

The 7503 features a CRT with an 8 X 10 centimeter graticule area with small spot size and high writing rate. Additionally, the instrument includes a readout system providing CRT display of alpha-numeric information from the plug-ins, including deflection factor, sweep rate and other encoded parameters.

This instrument will meet the electrical characteristics listed in Table 1-1 following complete calibration as given in Section 5. The performance check procedure given in Section 5 provides a convenient method of checking instrument performance without making internal checks or adjustments. The following electrical characteristics apply over a calibration interval of 1000 hours and an ambient temperature range of 0°C to +50°C, except as otherwise indicated. Warmup time for given accuracy is 20 minutes.

NOTE

Many of the measurement capabilities of this instrument are determined by the choice of plug-in units. The following characteristics apply to the 7503 only. See the system specification later in this section for characteristics of the complete system.

TABLE 1-1

ELECTRICAL

Characteristic	Performance
VERTICAL DEFLECTION SYSTEM	
Deflection Factor	Compatible with all 7-series plug-in units.
Deflection Accuracy	Less than 1% difference between compartments.
Low-Frequency Linearity	0.1 division or less compression or expansion of a center-screen two-division signal when positioned to the top and bottom of the graticule area.
Isolation Between Compartments	At least 100:1 from DC to 75 megahertz.
Chopped Mode Repetition Rate	One megahertz ±20%.
Time segment from each compartment	0.4 to 0.6 microsecond.
Delay Line	Permits viewing of leading edge of triggering signal.
Vertical Display Modes (selected by front-panel VERTICAL MODE switch)	LEFT: Left vertical only. ALT: Dual-trace, alternate between vertical units. ADD: Added algebraically. CHOP: Dual-trace, chopped between vertical units. RIGHT: Right vertical only.

Characteristic	Performance
TRIGGERING	
Trigger Source (selected by front-panel TRIGGER SOURCE switch)	VERT MODE: Determined by vertical mode. LEFT VERT: From left vertical unit only. RIGHT VERT: From right vertical unit only.

Characteristic	Performance
HORIZONTAL DEFLECTION SYSTEM	
Deflection Factor	Compatible with all 7-series plug-in units.
Fastest Calibrated Sweep Rate	Five nanoseconds/division.
Phase Shift Between Vertical and Horizontal Deflection Systems	
With phase correction	Adjustable to less than 2° from DC to two megahertz.

Characteristic	Performance
CALIBRATOR	
Wave Shape	Square wave.
Polarity	Positive going with baseline at zero volts.
Output Voltage (selected by front-panel CALIBRATOR switch)	
Open circuit	Four millivolts to 40 volts in five decade steps.
Into 50 ohms	Two millivolts to 0.4 volts in four steps.
Output Current	40 milliamperes through current loop.
Amplitude Accuracy (Voltage and Current)	
+15°C to +35°C	Within 1%.
0°C to +50°C	Within 2%.

Characteristic	Performance	
Repetition Rates (selected by front-panel RATE switch)	One kilohertz. One-half repetition rate of sweep gate. DC.	
One-Kilohertz Accuracy	+15°C to +35°C	0°C to +50°C
	Within 0.25%	Within 0.5%
Duty Cycle	50% ± 0.5%.	
Risetime and Falltime		
4 mV through 4 V and 40 mA	Less than 0.25 microsecond.	
40 V	Less than two microseconds with 10 pF load.	

Characteristic	Performance
EXTERNAL Z-AXIS INPUTS	
High Sensitivity Input	
Sensitivity	Two volts peak-to-peak provides trace modulation over full intensity range.
Useful input voltage vs. repetition frequency	Two volts peak-to-peak, DC to two megahertz; reducing to 0.4 volts peak-to-peak at 10 megahertz.
Polarity of operation	Positive-going signal decreases trace intensity; negative-going signal increases trace intensity.
Minimum pulse width that provides intensity modulation	40 nanoseconds at two volts.
Input resistance	500 ohms ±10%.
Maximum input voltage	15 volts (DC + peak AC).
High Speed Input	
Sensitivity	60 volts peak-to-peak provides trace modulation over full intensity range from DC to 75 megahertz.
Polarity of operation	Positive-going signal decreases trace intensity; negative-going signal increases trace intensity.

Characteristic	Performance
Minimum pulse width that provides intensity modulation	Five nanoseconds at 60 volts.
Input resistance at DC	18 kilohms ±15%.
Maximum input voltage	60 volts (DC + peak AC). 60 volts peak-to-peak AC.

SIGNAL OUTPUTS

+ Sawtooth	
Polarity	Positive-going with baseline at zero volts ±one volt (into one megohm).
Output voltage	
Rate of rise	
Into 50 ohms	50 millivolts/unit of time ±15%.[1]
Into one megohm	One volt/unit of time ±10%.[1]
Peak voltage	
Into 50 ohms	Greater than 500 millivolts.
Into one megohm	Greater than 10 volts.
Output resistance	950 ohms ±2%.
+ Gate	
Source (selected by Gate switch)	MAIN GATE from displayed time-base; DELAYED GATE from delaying time-base unit; or AUX GATE from dual-sweep time-base unit.
Output voltage	
Into 50 ohms	0.5 volt ±10%.
Into one megohm	10 volts ±10%.
Risetime into 50 ohms	20 nanoseconds or less.
Output resistance	950 ohms ±2%

[1] Unit of time selected by time-base time/division switch.

Characteristic	Performance
Vertical Signal Output	
Source	Determined by TRIGGER SOURCE switch.
Output voltage	
Into 50 ohms	25 millivolts/division of vertical deflection ±25%.
Into one megohm	0.5 volt/division of vertical deflection ±25%.
Output resistance	950 ohms ±2%.

POWER SUPPLY

Line Voltage Range (AC, RMS)	*Line voltage and range selected by Line Voltage Selector assembly on rear panel.*
115-volts nominal	90 to 110 volts. 104 to 126 volts. 112 to 136 volts.
230-volts nominal	180 to 220 volts. 208 to 252 volts. 224 to 272 volts.
Line Frequency	48 to 440 hertz.
Maximum Power Consumption	258 watts, 3.0 amperes at 60 hertz, 115-volt line.

CATHODE-RAY TUBE (CRT)

Graticule	
Type	Internal with variable edge lighting.
Area	Eight divisions vertical by ten divisions horizontal. Each division equals one centimeter.
Resolution	
Horizontal	At least 15 lines/division.
Vertical	At least 15 lines/division.
Geometry	0.1 division or less total bowing of a displayed horizontal or vertical line.
Beam Finder	Limits display within graticule area.

Characteristic	Performance
Photographic Writing Speed (without film fogging techniques)	
Tektronix C-51 Camera with f1.2 lens and 1:0.5 object-to-image ratio	At least 2250 centimeters/microsecond with Polaroid[2] Type 410 film (10,000 ASA) and P31 CRT phospor.
Tektronix C-27 Camera with f1.5 lens and 1:0.5 object-to-image ratio	At least 1500 centimeters/microsecond with Polaroid Type 410 film (10,000 ASA) and P31 CRT phosphor.

TABLE 1-2

ENVIRONMENTAL

Characteristic	Performance

NOTE

This instrument will meet the electrical characteristics given in Table 1-1 over the following environmental limits. Complete details on environmental test procedures, including failure criteria, etc., can be obtained from Tektronix, Inc. Contact your local Tektronix Field Office or representative.

Temperature Range	
Operating	0°C to +50°C.
Non-operating	−55°C to +75°C.
Altitude	
Operating	15,000 feet.
Non-operating	Test limit 50,000 feet.

[2] **Registered trademark of the Polaroid Corporation.**

Characteristic	Performance
Electro-magnetic Interference (EMI) as tested in MIL-I 6181 D (when equipped with EMI modification only)	
Radiated interference	Interference radiated from the instrument under test within the given limits from 150 kilohertz to 1000 megahertz.
Conducted interference	Interference conducted out of the instrument under test through the power cord within the given limits from 150 kilohertz to 25 megahertz.
Transportation (packaged instruments, without plug-ins)	Qualifies under National Safe Transit Committee test procedure 1A.

TABLE 1-3

PHYSICAL

Characteristic	Performance
Ventilation	Safe operating temperature is maintained by convection cooling. Automatic resetting thermal cutout protects instrument from overheating.
Warmup Time	20 minutes for rated accuracy.
Finish	Anodized front panel. Blue-vinyl painted aluminum cabinet.
Overall Dimensions (measured at maximum points)	
Height	13.5 inches (34.2 centimeters).
Width	9.2 inches (23.4 centimeters).
Length	24.6 inches (62.2 centimeters).
Net Weight (instrument only)	47 pounds (21.3 kilograms).

STANDARD ACCESSORIES

Standard accessories supplied with the 7503 are listed on the last pull-out page of the Mechanical Parts List illustrations. For optional accessories available for use with this instrument, see the Tektronix, Inc. catalog.

INSTRUMENT OPTIONS

General

The following options are available for the 7503 and can be installed as part of the instrument when ordered, or they can be installed at a later time. Complete information on all options for this instrument is given in this manual. For further information on instrument options, see your Tektronix, Inc. catalog, or contact your local Tektronix Field Office or representative.

Option 1

This option deletes the Readout System. Operation of the instrument is unchanged except that there is no alphanumeric display on the CRT and the READOUT control is non-functional. The Readout System can be added at any time by ordering the readout conversion kit.

Option 2

With option 2 installed, the instrument will meet the EMI interference specifications given in Table 1-2.

SYSTEM SPECIFICATIONS

Your 7000-Series oscilloscope system will provide exceptional flexibility in operation with a wide variety of general and special purpose plug-in amplifiers and time bases. The Type number of a particular plug-in identifies it thus: the first digit (7) denotes the oscilloscope system (7000); the second character describes the use of the plug-in—A for amplifier, B for "real time" time base, J or K for spectrum analyzer, L for single-unit spectrum analyzer (a double-width plug-in). M for miscellaneous, S for sampling unit, and T for sampling time base. The third and fourth digits in the plug-in title are sequence numbers. The table following lists specifications that are dependent upon the system as a whole.

7000-SERIES OSCILLOSCOPE SYSTEM SPECIFICATION

	7500-Series			7700-Series		Vertical System Deflection Factor Accuracy*			SIG OUT		Horizontal System
Plug-In Unit	Probe	BW	T_r	BW	T_r	EXT CAL 0-50°C	INT CAL 15°-35°C	INT CAL 0-50°C	BW	T_r	
7A11	Integral	90 MHz	3.9 ns	150 MHz	2.4 ns	2%	3%	4%	60 MHz	5.9 ns	Horizontal System bandwidth with 2 units of the same type operated X-Y with phase correction is 2 MHz for the 7500-Series, 3 MHz for the 7700-Series unless otherwise stated. Without phase correction the 7700-Series horizontal bandwidth upper 10% down point is 3 MHz; that of the 7500-Series is 5 MHz, unless otherwise indicated. X-Y phase shift with correction is 2° at 2 MHz for both Series unless otherwise stated.
7A12	None	75 MHz	4.7 ns	105 MHz	3.4 ns	2%	3%	4%	55 MHz	6.4 ns	
	P6053	75 MHz	4.7 ns	105 MHz	3.4 ns	3%	4%	5%	55 MHz	6.4 ns	
7A13	None	75 MHz	4.7 ns	100 MHz	3.5 ns	1 1/2%	2 1/2%	3 1/2%	55 MHz	6.4 ns	
	P6053	75 MHz	4.7 ns	100 MHz	3.5 ns	1 1/2%	2 1/2%	3 1/2%	55 MHz	6.4 ns	
7A14	P6021	45 MHz	7.8 ns	50 MHz	7.0 ns	2%	3%	4%	40 MHz	8.8 ns	
	P6022	75 MHz	4.7 ns	105 MHz	3.4 ns	2%	3%	4%	50 MHz	7.0 ns	
7A16	None	90 MHz	3.9 ns	150 MHz	2.4 ns	2%	3%	4%	60 MHz	5.9 ns	
	P6053	90 MHz	3.9 ns	150 MHz	2.4 ns	3%	4%	5%	60 MHz	5.9 ns	
7A22	None or	1.0 MHz	350 ns	1 MHz	350 ns	2%	3%	4%	1.0 MHz	350 ns	Both the 7700- and 7500-Series are specified as follows: Bandwidth with phase correction is 800 kHz; without phase correction bandwidth is 1 MHz ±10%; X-Y phase shift with phase correction is 1° at 100 kHz.
	Any	±10%	±9%	±10%	±9%				±10%	±9%	

***Deflection Factor accuracy is checked as follows:**

EXT CAL 0°C to 50°C, plug-in gain is set at a temperature within 10°C of operating temperature, using an external calibrator whose accuracy is within .25%.

INT CAL 15°C to 35°C, plug-in gain is set while operating within a temperature range of +15°C to +35°C, using the oscilloscope calibrator.

INT CAL 0°C to 50°C, plug-in gain is set using the oscilloscope calibrator (within 10°C of the operating temperature) in a temperature range between 0°C and +50°C.

PLUG-IN OPTIONS
MAJOR CHARACTERISTICS
AMPLIFIERS

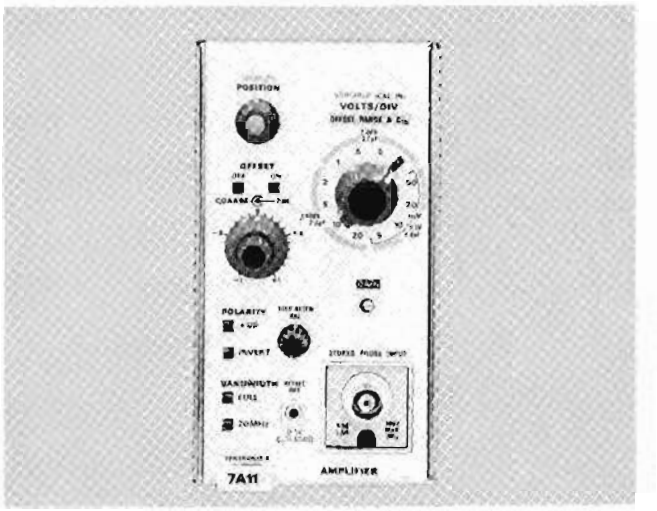


Fig. 1. 7A11 FET Probe Wide Band Amplifier (All specifications at Probe tip).

7A11 FET Probe Wide Band Amplifier
(All specifications at Probe tip)

Deflection Factor	5 mV/div to 20 V/div
Input Resistance	1 MΩ within 1%
Input Capacitance	2 to 6 pF depending on Volts/div setting
DC Offset	Up to 400 V referred to input

Attenuation via integral FET Probe and/or amplifier from X1 through X400 controlled automatically by Volts/div switch to prevent display from overscaning screen.

7A12 Dual Trace Wide Band Amplifier

Deflection Factor	5 mV/div to 5 V/div, pushbutton selected
Input Resistance	1 MΩ within 2%
Input Capacitance	24 pF within 1 pF for all deflection factors
DC Offset	Equivalent to at least 1000 div
Operating Modes	CH 1 Only, CH 2 Only, Chopped, Alternate and Added. Either channel can be inverted for differential measurements.

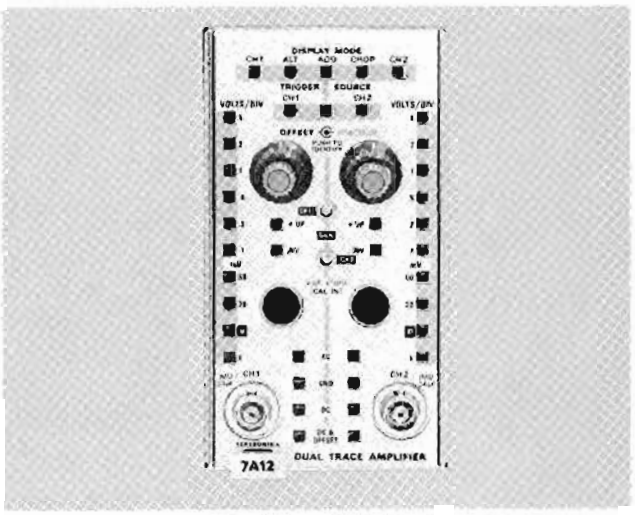


Fig. 2. 7A12 Dual Trace Wide Band Amplifier.

AMPLIFIERS (Cont)

7A13 Differential Comparator & Differential Amplifier

Deflection Factor	1 mV/div to 5 V/div
Calibrated Comparison Voltages	0 to +10 Volts or 0 to −10 Volts
Input Resistance	1 MΩ within 0.15%
Input Capacitance	20 pF within 0.4 pF

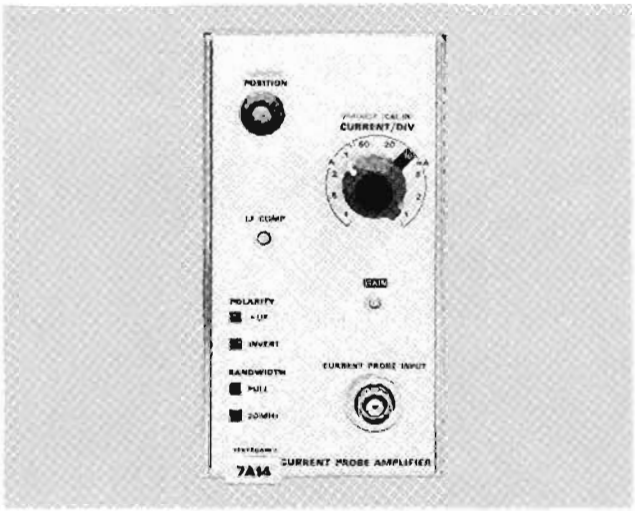


Fig. 4. 7A14 Current Probe Amplifier.

7A16 Wide Band Amplifier

Deflection Factor	5 mV/div to 5 V/div
Input Resistance	1 MΩ within 2%
Input Capacitance	15 pF within 0.5 pF
Bandwidth	(See System Specification) Maintains full bandwidth capabilities of system over complete range of deflection factors

Fig. 3. 7A13 Differential Comparator and Differential Amplifier.

7A14 Current Probe Amplifier

Deflection Factor	1 mA/div to 1 A/div
Input Connector	Special BNC connector senses type of probe in use and switches internal compensation circuit so no gain adjustment is needed.

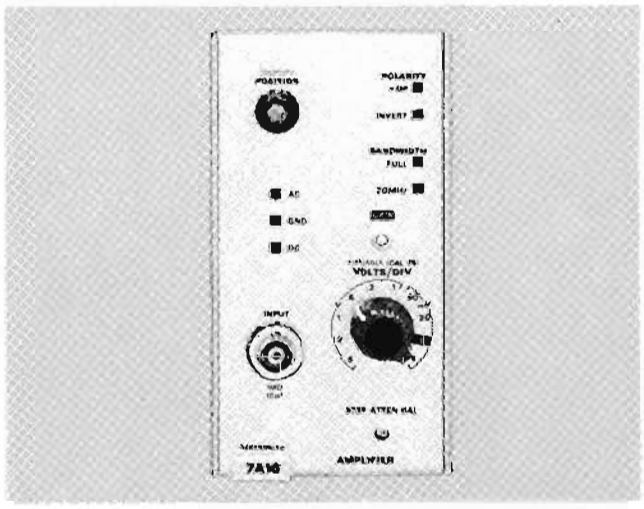


Fig. 5. 7A16 Wide Band Amplifier.

AMPLIFIERS (Cont)

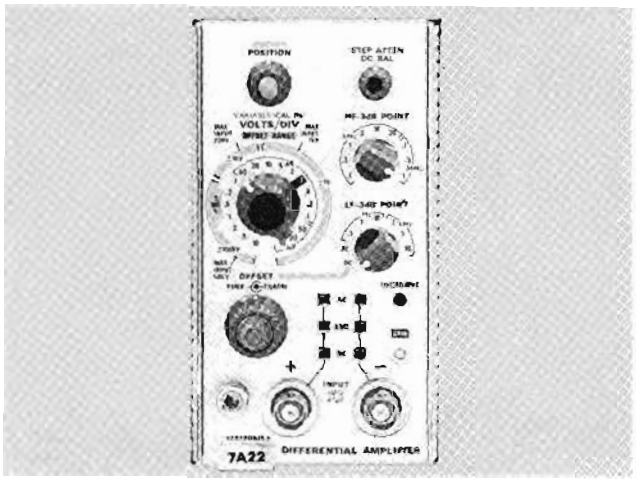


Fig. 6. 7A22 High-Gain Differential Amplifier.

7A22 High-Gain Differential Amplifier

Deflection Factor	10 µV/div to 10 V/div
Input Resistance	1 MΩ within 1%
Input Capacitance	47 pF within 2.5 pF
Displayed Noise	16 µV at 10 µV/div at maximum bandwidth, tangentially measured.

REAL TIME TIME BASES

7B50 Time Base

Sweep Rate	5 s/div to 50 ns/div (5 ns/div with X10 MAGNIFIER) in 25 calibrated steps
Triggering	To 100 MHz or vertical amplifier bandwidth, whichever is less. Sweep free runs providing bright baseline in the absence of adequate triggering signal in P-P AUTO and AUTO triggering modes
Internal Trigger Jitter	1 ns or less at 75 MHz
Display Mode	Time-Base for normal sweep operation. Amplifier for X-Y operation

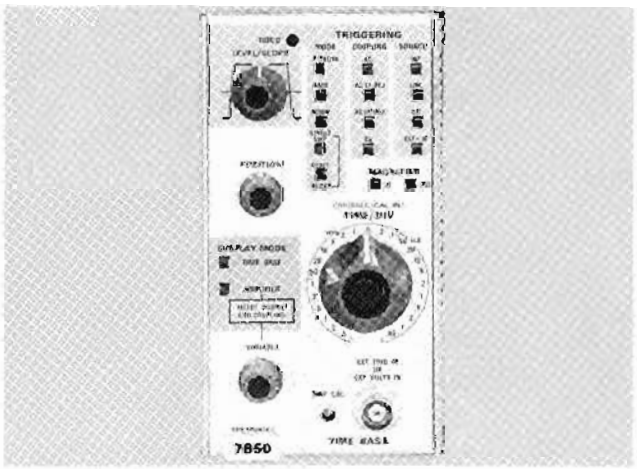


Fig. 7. 7B50 Time Base.

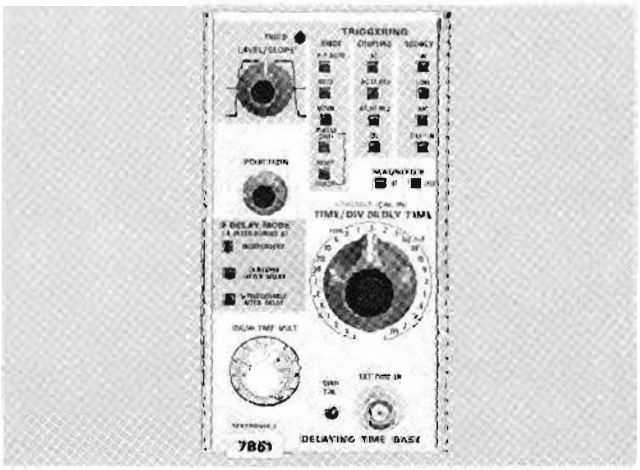


Fig. 8. 7B51 Delaying Time Base.

7B51 Delaying Time Base

Used singly in 7500-Series oscilloscope as conventional time base, or in combination with Type 7B50 as delaying sweep time base.

Sweep Rate and Triggering	Same as Type 7B50
Delay Time Multiplier Range	0 to 10 times the time/div setting
Accuracy	5 s/div to 1 s/div within 2% 0.5 s/div to 1 µs/div within 1%.
Multiplier Incremental Linearity	Within 0.2%
Jitter	1 part or less in 50,000 of 10X the TIME/DIV setting

REAL TIME TIME BASES (Cont)

7B52 Dual Time Base Unit

Designed specifically for the 7500-Series Oscilloscopes but is compatible with all the 7000-Series.

Sweep Rate	0.05 µs/div to 5 s/div (5 ns/div with 10X MAGnifier) in 25 calibrated steps.
Triggering	To 100 MHz or vertical amplifier bandwidth, whichever is less. Man sweep free runs in Auto Mode, providing bright trace in the absence of a triggering signal. Delayed sweep is triggerable after delay.
Display Mode	Main Sweep, Manix Sweep intensified during Delayed Sweep, Delayed Sweep only, and Mixed (display of Main Sweep and Delayed Sweep). Horizontal Amplifier can be used for X-Y operation.

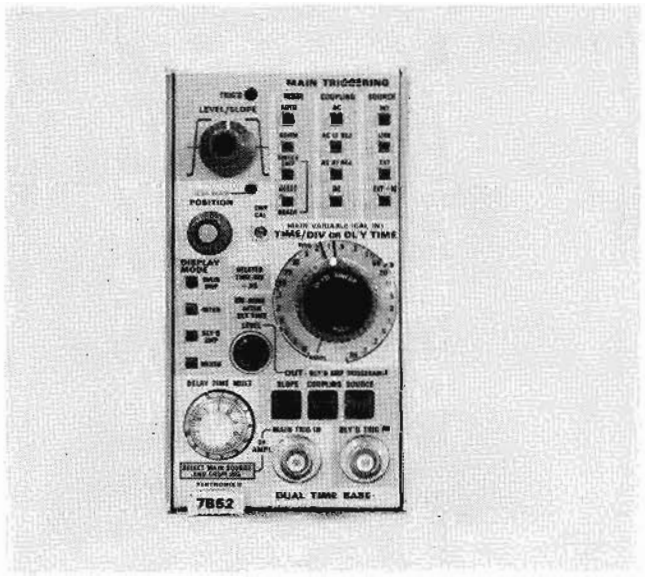


Fig. 9. 7B52 Dual Time Base.

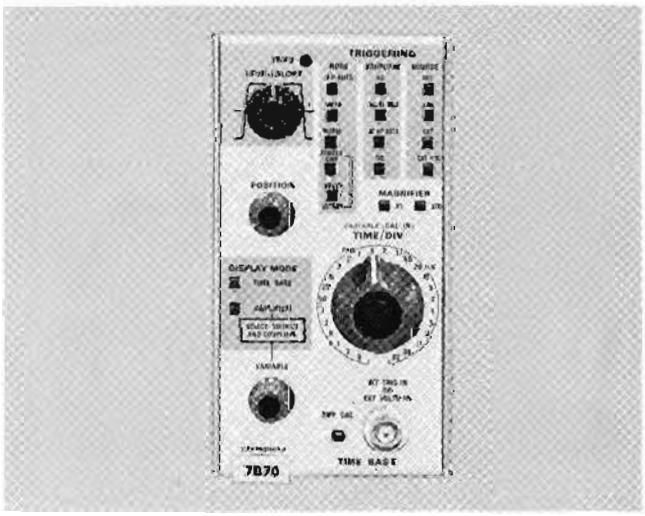


Fig. 10. 7B70 Time Base.

7B70 Time Base

Sweep Rate	0.02 µs/div to 5 s/div (2 ns/div with X10 MAGNIFIER) in 26 calibrated steps
Triggering	To 200 MHz or vertical amplifier bandwidth, whichever is less. Sweep free runs providing bright base line in the absence of adequate triggering signal in P-P AUTO and AUTO triggering modes.
Display Mode	Time-Base for normal sweep operation. Amplifier for X-Y operation and phase measurements.

REAL TIME TIME BASES (Cont)

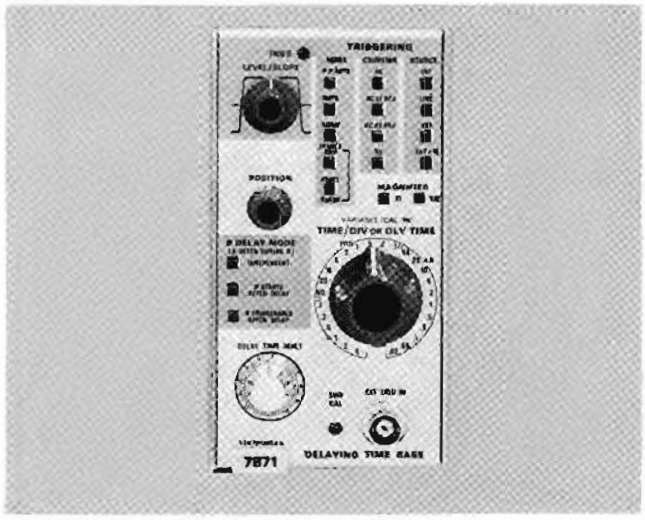


Fig. 11. 7B71 Delaying Time Base.

7B71 Delaying Time Base

Used singly in 7700-Series oscilloscope as conventional time base, or in combination with Type 7B70 as delaying sweep time base.

Sweep Rate and Triggering	Same as Type 7B70
Delay Time Multiplier	
Range	0 to 10 times TIME/DIV setting
Accuracy	5 s/div to 1 s/div within 2%
	0.5 s/div to 1 µs/div within 1%
Multiplier Incremental Linearity	within 0.2%
Jitter	1 part or less in 50,000 of 10X TIME/DIV setting.

SAMPLING UNIT

7S11 Sampling Unit

Single channel sampling unit accepting all Tektronix sampling heads. Vertical characteristics set by the sampling head in use.

DC Offset	±1 volt
Units/Div	2 to 200
Polarity	Display normal or inverted
Output connectors	Offset & Vertical Signal

Internal Trigger circuits operate with sampling heads containing trigger pickoff circuitry. Will operate with a second 7S11 for dual-trace sampling, both controlled by a 7T11 Sampling Sweep Unit.

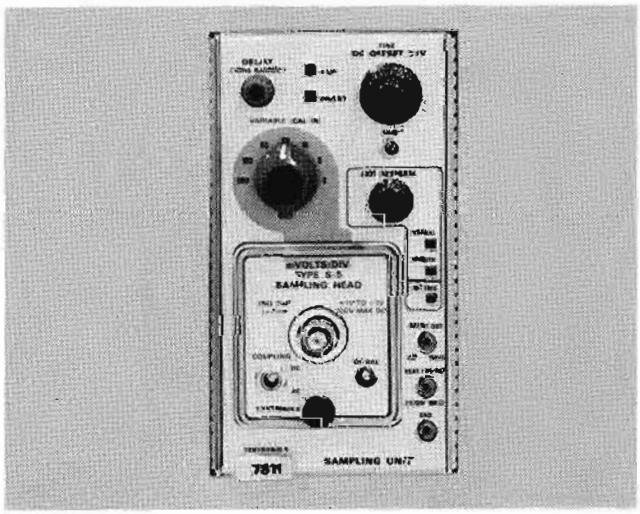


Fig. 12. 7S11 Sampling Unit.

SAMPLING SWEEP

7T11 Sampling Sweep Unit

Automatically provides equivalent time or real time sampling process. Random mode or sequential mode available during equivalent time sampling. Operates with one or two 7S11 Sampling Units.

Sweep Rates	Equivalent time, 5 μs/Div to 10 ps/Div Real time, 5 ms/Div to 0.1 μs/Div
Time Position Ranges	Equivalent time, 50 ns to 50 μs Real time, 0.5 ms to 50 ms
Triggering	Internal (except with S-3 plug-in head) or External.
Modes	Frequency Range
Internal	DC to 500 MHz
External, 50 Ω Input	DC to 500 MHz
External, 1 MΩ Input	DC to 100 MHz
External, 50 Ω Input HF sync	500 MHz to 12.4 GHz
Frequency coverage	DC coupled through 12.4 GHz HF Sync
Sensitivity	5 mV to 2 V P-P (50 mV internal)
Dot Density	Variable, 50 to 1000 dots/Div

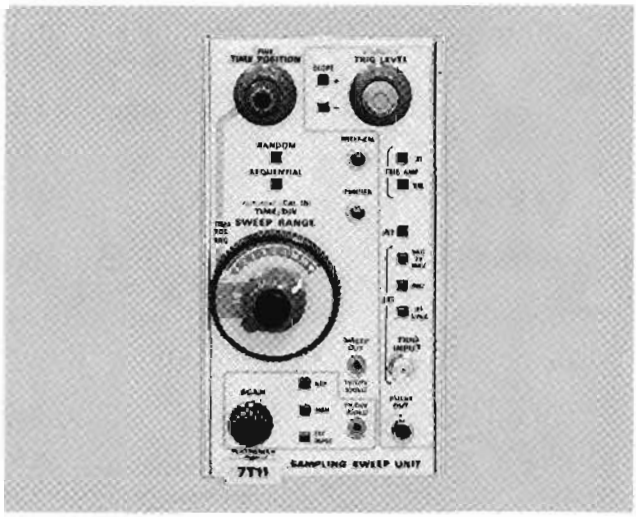


Fig. 13. 7T11 Sampling Sweep Unit.

DELAY LINE

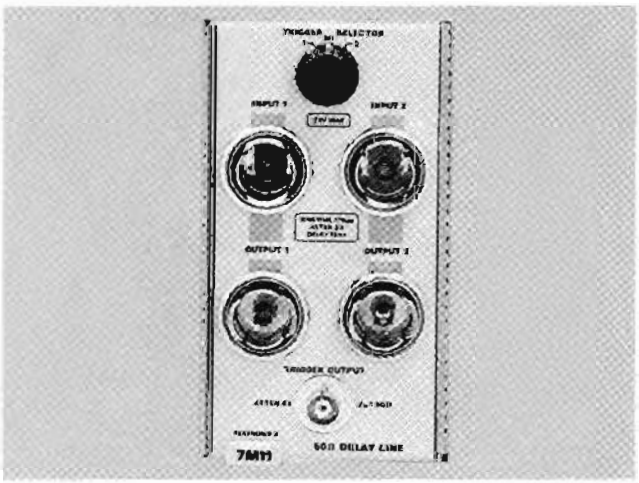


Fig. 14. 7M11 50 Ω Delay Line, Dual channel.

7M11 50 Ω Delay Line, Dual Channel

Signal Delay	75 ns, 30 ps or less time difference between channels
Risetime	175 ps or less
Attenuation	2X
Trigger Pickoff	Selectable from either channel

An accessory for sequential sampling systems without internal delay lines, or for random sampling systems operated at low signal repetition rates requiring a pretrigger.

SAMPLING HEADS

Signal Input Heads

S-1 Sampling Head

Input Resistance	50 Ω
Risetime	350 ps
Random noise	less than 2 mV

S-2 Sampling Head

Input Resistance	50 Ω
Risetime	50 ps
Random noise	Less than 6 mV

S-3 Sampling Head (with attached probe)

Input Resistance	100 kΩ
Input Capacitance	2.3 pF
Risetime	350 ps
Random noise	Less than 3 mV

S-4 Sampling (3 mm input connector)

Input Resistance	50 Ω
Risetime	25 ps
Random noise	Less than 5 mV

S-5 Sampling Head

Input Resistance	1 MΩ
Risetime (with 10X probe)	1 ns
Noise	Less than 500 μV

Special Purpose Heads

S-50 Pulse Generator Head (3 mm output connector)

Pulse Risetime	25 ps
Pulse Amplitude	+400 mV
Pulse Duration	100 ns, with pre-trigger out

S-51 Trigger Countdown Head (3 mm input connector)

Trigger Countdown	1 to 18 GHz
Input Signal Voltage	100 mV P-P to 5 V P-P

SECTION 2
OPERATING INSTRUCTIONS

Change information, if any, affecting this section will be found at the rear of the manual.

General

To effectively use the 7503, the operation and capabilities of the instrument must be known. This section describes the operation of the front-, rear-, and side-panel controls and connectors and gives first time and general operating information.

PRELIMINARY INFORMATION

Operating Voltage

WARNING

This instrument is designed for operation from a power source with its neutral at or near earth (ground) potential with a separate safety-earth conductor. It is not intended for operation from two phases of a multi-phase system, or across the legs of a single-phase, three-wire system.

The 7503 can be operated from either a 115-volt or a 230-volt nominal line voltage source. The Line Voltage Selector assembly on the rear panel converts this instrument from one operating voltage to the other. In addition, this assembly changes the primary connections of the power transformer to allow selection of one of three regulating ranges. The assembly also includes the two line fuses to provide the correct protection for the instrument as the line voltage is changed. Use the following procedure to obtain correct instrument operation from the line voltage available.

1. Disconnect the instrument from the power source.

2. Loosen the two captive screws which hold the cover onto the selector assembly; then pull to remove the cover.

3. To convert from 115-volts to 230-volts nominal line voltage, or vice versa, pull out the Voltage Selector switch bar (see Fig. 2-1); turn it around 180° and plug it back into the remaining holes. Change the line-cord plug to match the power-source receptacle or use a 115-to 230-volt adapter.

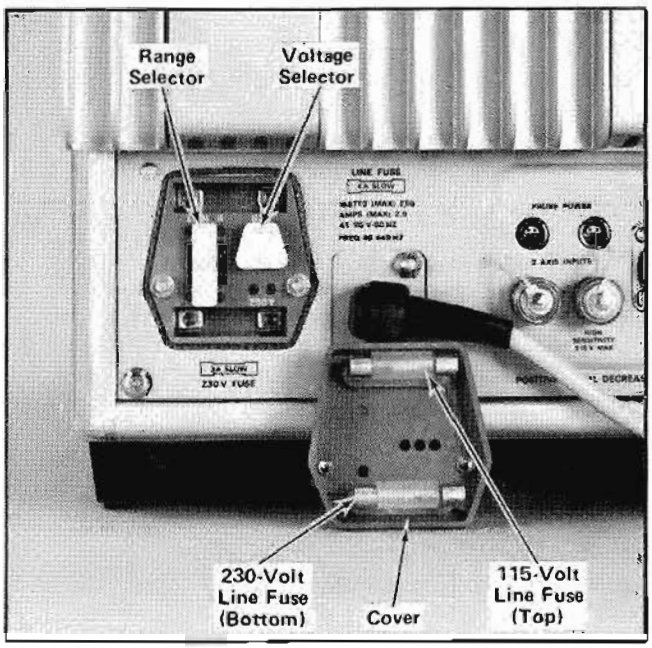


Fig. 2-1. Line Voltage Selector assembly on rear panel (shown with cover removed).

NOTE

Color-coding of the cord conductors is as follows (in accordance with National Electrical Code):

Line	*Black*
Neutral	*White*
Safety earth (ground)	*Green*

4. To change regulating ranges, pull out the Range Selector switch bar (see Fig. 2-1); slide it to the desired position and plug it back in. Select a range which is centered about the average line voltage to which the instrument is to be connected (see Table 2-1).

5. Re-install the cover and tighten the captive screws.

6. Before applying power to the instrument, check that the indicating tabs on the switch bars are protruding through the correct holes for the desired nominal line voltage and regulating range.

TABLE 2-1

Regulating Ranges

Range Selector Switch Position	Regulating Range 115-volts nominal	230-volts nominal
LO (switch bar in left holes)	90 to 110 volts	180 to 220 volts
M (switch bar in middle holes)	104 to 126 volts	208 to 252 volts
HI (switch bar in right holes)	112 to 136 volts	224 to 272 volts

CAUTION

This instrument may be damaged if operated with the Line Voltage Selector assembly set to incorrect positions for the line voltage applied.

The 7503 is designed to be used with a three-wire AC power system. If the three- to two-wire adapter is used to connect this instrument to a two-wire AC power system, be sure to connect the ground lead of the adapter to earth (ground). Failure to complete the ground system may allow the chassis of this instrument to be elevated above ground potential and pose a shock hazard.

Operating Temperature

The 7503 can be operated where the ambient air temperature is between 0° C and +50° C. This instrument can be stored in ambient temperatures between −55° C and +75° C. After storage at temperatures beyond the operating limits, allow the chassis temperature to come within the operating limits before power is applied.

The 7503 is cooled by convection air flow through the instrument. Components which require the most cooling are mounted externally on a heat radiator at the rear of this instrument. Adequate clearance must be provided on all sides to allow heat to be dissipated from the instrument. Do not block or restrict the air flow through the holes in the cabinet or the heat radiator on the rear. Maintain the clearance provided by the feet on the bottom and allow about two inches clearance on the top, sides, and rear (more if possible).

A thermal cutout in this instrument provides thermal protection and disconnects the power to the instrument if the internal temperature exceeds a safe operating level. Power is automatically restored when the temperature returns to a safe level. Operation in confined areas or in close proximity to heat-producing instruments may cause the thermal cutout to open more frequently.

Operating Position

A bail-type stand is mounted on the bottom of this instrument. This stand permits the 7503 to be tilted up about 10° for more convenient viewing (see Fig. 2-2).

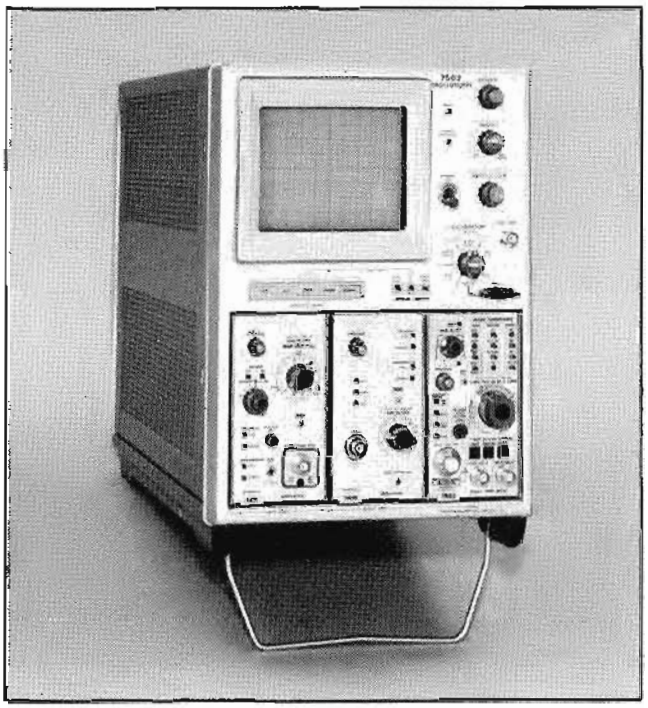


Fig. 2-2. Instrument positioned on bail-type stand.

PLUG-IN UNITS

General

The 7503 is designed to accept up to three Tektronix 7-series plug-in units. This plug-in feature allows a variety of display combinations and also allows selection of bandwidth, sensitivity, display mode, etc. to meet the measurement requirements. In addition, it allows the oscilloscope system to be expanded to meet future measurement requirements. The overall capabilities of the resultant system are in large part determined by the characteristics of the plug-in selected. A list of the currently available plug-ins along with their major specifications, is given in Section 1. For more complete information, see the current Tektronix, Inc. catalog.

Installation

To install a plug-in unit into one of the plug-in compartments, align the slots in the top and bottom of the plug-in with the associated guide rails in the plug-in compartment. Push the plug-in unit firmly into the compartment until it locks into place. To remove a plug-in, pull the release latch on the plug-in unit to disengage it and pull the unit out

of the compartment. Plug-in units can be removed or installed without turning off the instrument power. However, installation of the plug-ins with the power on may on without turning off the instrument power. However, installation of the plug-ins with the power on may on occasion cause the power-supply protection circuits of the 7503 to interrupt the power to the instrument. This is due to the sudden surge of current that is demanded as a plug-in is connected to the power-supply circuits. If the 7503 is not operating after the plug-ins are inserted, turn off the POWER switch momentarily and return it to ON.

It is not necessary that all of the plug-in compartments be filled to operate the instrument; only the plug-ins needed for the measurement to be made are necessary. However, at environmental extremes, interference may be radiated into this instrument through the open plug-in compartment; also, the instrument may radiate interference into other equipment. Blank plug-in panels are available from Tektronix, Inc. to cover the unused compartment; order Tektronix Part No. 016-0155-00.

When the 7503 is calibrated in accordance with the calibration procedure given in this instruction manual, the vertical and horizontal gain are normalized. This allows calibrated plug-in units to be changed from one plug-in compartment to another without recalibration. However, the basic calibration of the individual plug-in units should be checked when they are installed in this system to verify their measurement accuracy. See the operating instructions section of the plug-in unit instruction manual for verification procedure.

The plug-in feature of the 7503 allows a variety of display modes with many different plug-ins. Specific information for obtaining these displays is given later, in this section. However, the following information is provided here to aid in plug-in installation.

To produce a single-trace display, install a single-channel vertical unit (or dual-channel unit set for single-channel operation) in either of the vertical compartments. For dual-trace displays, either install a dual-channel vertical unit in one of the vertical compartments or install a single-channel vertical unit in each vertical compartment. A combination of a single-channel and dual- channel vertical unit allows a three-trace display; likewise, a combination of two dual-channel vertical units allows a four-trace display.

For time-base displays, a 7B-series plug-in is placed in the Horizontal compartment.

X-Y displays can be obtained in two ways with the 7503 system. If a 7B-series time- base plug-in is available which has an amplifier feature, the X signal can be routed through one of the vertical units via the internal-trigger pickoff circuitry to the horizontal system. Then, the vertical (Y) signal is connected to the remaining vertical unit. Also, a 7A-series amplifier plug-in can be installed in the horizontal compartment for X-Y operation.

Special purpose plug-ins may have specific restrictions regarding the plug-in compartments in which they can be installed. This information will be given in the instruction manuals for these plug-ins.

CONTROLS AND CONNECTORS

General

The major controls and connectors for operation of the 7503 are located on the front panel of the instrument. Several auxiliary functions are provided on the side and rear panels. Fig. 2-3 shows the front, side, and rear panels of the 7503. To make full use of the capabilities of this instrument, the operator should be familiar with the function and use of each of these controls and connectors. A brief description of each control and connector is given here. More detailed operating information is given under General Operating Information.

Cathode-Ray Tube (CRT)

ASTIG	Screwdriver adjustment used in conjunction with the FOCUS control to obtain a well-defined display. Does not require readjustment in normal use.
INTENSITY	Controls brightness of the trace. Control is inoperative when the HORIZ compartment is vacant.
FOCUS	Provides adjustment for optimum display definition.
BEAM FINDER (PULL LOCK)	Compresses display within graticule area independent of display position or applied signals. Momentary actuation provided when button is pressed; display remains compressed when knob is pulled outward to lock it in the "find" position.
READOUT	Controls brightness of the readout portion of the CRT display. In the fully counterclockwise position, the Readout System is inoperative.

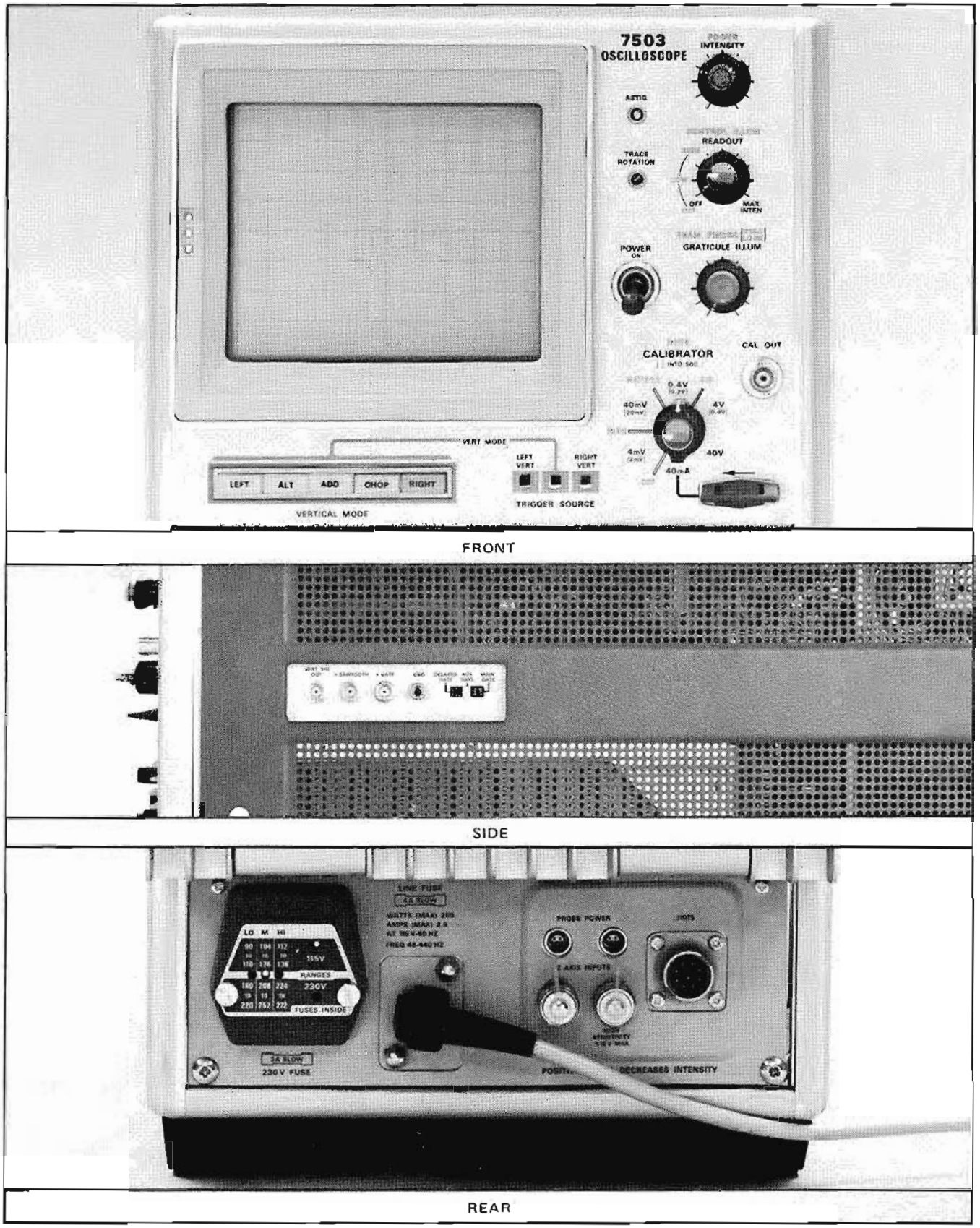


Fig. 2-3. Front-, side- and rear-panel controls and connectors.

CONTROL ILLUM — Controls illumination level of pushbutton switches on the 7503 and the associated plug-ins.

OFF: All pushbutton lights off.

LOW: All pushbuttons illuminated at low intensity.

HIGH: Pushbuttons illuminated at maximum intensity.

TRACE ROTATION — Screwdriver adjustment to align trace with horizontal graticule lines.

GRATICULE ILLUM — Controls graticule illumination.

Mode Selectors

VERTICAL MODE — Selects vertical mode of operation.

LEFT: Signal from plug-in unit in LEFT VERT compartment is displayed.

ALT: Signals from plug-in units in both LEFT VERT and RIGHT VERT compartments are displayed. Display switched between vertical plug-ins after each sweep.

ADD: Signals from plug-in units in both LEFT VERT and RIGHT VERT compartments are algebraically added and the algebraic sum displayed on the CRT.

CHOP: Signals from plug-in units in both LEFT VERT and RIGHT VERT compartments are displayed. Display switched between vertical plug-ins at a one-megahertz repetition rate.

RIGHT: Signal from plug-in unit in RIGHT VERT compartment is displayed.

TRIGGER SOURCE — Selects source of internal trigger signal for time-base unit in the Horizontal compartment.

VERT MODE: Trigger signal automatically follows the vertical display except in CHOP; then the trigger signal is the same as for ADD.

LEFT VERT: Trigger signal is obtained from plug-in unit in LEFT VERT compartment.

RIGHT VERT: Trigger signal is obtained from plug-in unit in RIGHT VERT compartment.

Calibrator

CALIBRATOR — Selects amplitude of output at CAL OUT connector or 40 mA current through current loop. Outputs available from four millivolts to 40 volts, into high-impedance load, in decade steps, or from two millivolts to 0.4 volt into 50-ohm load (output into 50 ohms shown in brackets on panel).

RATE — Selects the mode and repetition rate of the output from the Calibrator.

OFF: Calibrator is disabled. No current through current loop and no voltage at CAL OUT connector.

1 kHz: Calibrator operates at one-kilohertz rate. 40-milliampere square-wave current through current loop or square-wave voltage (amplitude determined by CALIBRATOR switch) at CAL OUT connector.

GATE ÷2: Calibrator operates at one-half the repetition rate of the gate signal from the time-base unit in the Horizontal compartment. 40-milliampere square-wave current through current loop or square-wave voltage (amplitude determined by CALIBRATOR switch) at CAL OUT connector.

DC: DC voltage available at CAL OUT connector (amplitude determined by CALIBRATOR switch), or 40 milliampere DC current through current loop.

Outputs

CAL OUT — Provides positive-going calibrator output when voltage operation is selected.

40 mA Current Loop — Probe loop providing calibrator current output when CALIBRATOR switch is set to 40 mA postiion.

Side Panel

VERT SIG OUT — Provides output signal from the vertical plug-ins. Source of the output signal at the VERT SIG OUT connector is selected by the TRIGGER SOURCE switch.

+ SAWTOOTH	Positive-going sample of sawtooth signal from a time-base unit in the HORIZ compartment.
+ GATE	Positive-going gate signal from a time-base unit in the HORIZ compartment. Switch allows selection of one of three gate signals: MAIN GATE, coincident with the sweep being displayed; AUX GATE, depends upon type of time-base unit; DELAYED GATE, coincident with the delay period (delaying sweep time-base units only).
GND	Binding post to establish common ground between the 7503 and any associated equipment.

Rear Panel

Line Voltage Selector (not labeled)	Switching assembly to select the nominal operating voltage and the line voltage range. The assembly also includes the line fuses. Voltage Selector: Selects nominal operating voltage range (115 or 230 volts). Range Selector: Selects line voltage range (low, medium, high).
PROBE POWER	Power source for active probe systems.
Z-AXIS INPUTS	Input connectors for intensity modulation of the CRT display. HIGH SPEED: Input connector for high-amplitude Z-axis signals; usable over full frequency range of instrument. HIGH SENSITIVITY: Input connector for low-amplitude Z-axis signals; usable for signals with repetition rates of DC to 10 megahertz; input voltage derating necessary between two and 10 megahertz.
J1075	Nine-pin connector which provides remote single-sweep reset and ready indication for the time-base unit in the HORIZ compartment (with compatible time-base units only).

FIRST-TIME OPERATION

General

The following steps demonstrate the use of the controls and connectors of the 7503. It is recommended that this procedure be followed completely for familiarization with this instrument.

Set-up Information

1. Set the front-panel controls as follows:

INTENSITY	Counterclockwise
FOCUS	Midrange
BEAM FINDER	Released
READOUT	OFF
CONTROL ILLUM	HIGH
GRATICULE ILLUM	Counterclockwise
POWER	OFF
CALIBRATOR	4 V
RATE	1 kHz
VERTICAL MODE	LEFT
TRIGGER SOURCE	VERT MODE

2. Connect the 7503 to a power source that meets the voltage and frequency requirements of this instrument. If the available line voltage is outside the limits of the Line Voltage Selector switch (on rear panel), see Operating Voltage in this section.

3. Insert Tektronix 7A-series amplifier units into both the LEFT VERT and RIGHT VERT compartments. Insert a Tektronix 7B-series time-base unit into the HORIZ compartment.

4. Set the POWER switch to ON. Allow several minutes warmup so the instrument reaches a normal operating temperature before proceeding.

5. Set both vertical units for a vertical deflection factor of two volts/division and center the vertical position controls.

6. Set the time-base unit for a sweep rate of 0.5 millisecond/division in the auto, internal trigger mode.

7. Advance the INTENSITY control until the trace is at the desired viewing level (near midrange).

8. Connect the CAL OUT connector to the input connector of the left vertical unit with a BNC-to-BNC patch cord (supplied accessory).

9. Adjust the FOCUS control for a sharp, well-defined display over the entire trace length. (If focused display cannot be obtained, see Astigmatism Adjustment in this section.)

10. Disconnect the input signal and position the trace with the left vertical unit position control so it coincides with the center horizontal line of the graticule.

11. If the trace is not parallel with the center horizontal line, see Trace Alignment Adjustment in this section.

12. Rotate the GRATICULE ILLUM control throughout its range and notice that the graticule lines are illuminated as the control is turned clockwise (most obvious with tinted filter installed). Set control so graticule lines are illuminated as desired.

Calibration

13. Connect the CAL OUT connector to the input connectors of both vertical units with the BNC-to-BNC jumper leads.

14. The display should be two divisions in amplitude with five complete cycles shown horizontally. An incorrect display indicates that the plug-ins need to be recalibrated. See the instruction manual of the applicable unit for complete information.

Vertical Mode

15. Notice that the position control of only the left vertical unit has any effect on the displayed trace. Position the start of the trace to the farthest left line of the graticule with the time-base unit position control, and move the trace to the upper half of the graticule with the left vertical unit position control.

16. Press the RIGHT button of the VERTICAL MODE switch.

17. Notice that the position control of only the right vertical unit has any effect on the displayed trace. Move the display to the bottom half of the graticule with the right vertical unit position control.

18. Press the ALT button of the VERTICAL MODE switch. Notice that two traces are displayed on the CRT. The top trace is produced by the left vertical unit, and the bottom trace is produced by the right vertical unit. Reduce the sweep rate of the time-base unit to 50 milliseconds/division. Notice that the display alternates between the left and right vertical units after each sweep. Turn the time-base sweep rate switch throughout its range. Notice that the display alternates between vertical units at all sweep rates.

19. Press the CHOP button of the VERTICAL MODE switch. Turn the time-base unit sweep rate switch throughout its range. Notice that a dual-trace display is presented at all sweep rates, but unlike ALT, both vertical units are displayed on a time-sharing basis. Return the time-base unit sweep rate switch to 0.5 millisecond/division.

20. Press the ADD button of the VERTICAL MODE switch. The display should be four divisions in amplitude. Notice that the position control of either vertical unit moves the display. Return the VERTICAL MODE switch to the LEFT position.

Triggering

21. Center the display on the CRT with the left vertical unit position control. Disconnect the input signal from the right vertical unit input connector. Press all of the VERTICAL MODE switch buttons in sequence. Notice that a stable display is obtained in all positions of the VERTICAL MODE switch (straight line in RIGHT position).

22. Press the LEFT VERT button of the TRIGGER SOURCE switch. Again, press all of the VERTICAL MODE buttons in sequence. Notice that the display is again stable in all positions, as in the previous step.

23. Press the RIGHT VERT button of the TRIGGER SOURCE switch. Press all the VERTICAL MODE switch buttons in Sequence and notice that a stable display cannot be obtained in any position. This is because there is no input signal connected to the right vertical unit.

Control Illumination

24. Notice that the selected switch buttons of the 7503 and the plug-in units are illuminated.

25. Change the CONTROL ILLUM switch to the LOW position. Notice that the selected buttons of the 7503 and the plug-ins are illuminated at a reduced intensity.

26. Change the CONTROL ILLUM switch to the OFF position. Notice that none of the buttons are illuminated.

Readout

27. Turn the READOUT control clockwise until a digital display is visible within the top or bottom division of

the CRT. Change the deflection factor of the vertical unit selected for display. Notice that the readout display changes as the deflection factor is changed. Change the sweep rate of the time-base unit. Notice that the readout display for the time-base unit changes also as the sweep rate is changed.

28. Set the time-base unit for magnified operation. Notice that the readout display changes to indicate the correct magnified sweep rate. If a readout-coded 10X probe is available for use with the vertical unit, connect it to the input connector of the vertical plug-in. Notice that the deflection factor indicated by the readout is increased by 10 times when the probe is added. Return the time-base unit to normal sweep operation and disconnect the probe.

29. Press all of the VERTICAL MODE switch buttons in sequence. Notice that the readout from a particular plug-in occupies a specific location on the display area. If either of the vertical units is a dual-trace unit, notice that the readout for channel 2 appears within the lower division of the CRT.

Beam Finder

30. Set the vertical deflection factor of the vertical plug-in which is displayed to 0.1 volt/division. Notice that no square wave display is visible, since the deflection exceeds the scan area of the CRT.

31. Press the BEAM FINDER button. Notice that the display is returned to the viewing area in compressed form. Release the BEAM FINDER switch and note that the display again disappears from the viewing area. Pull the BEAM FINDER outward so it locks in the "find" position. Notice that the display is again returned to the viewing area in compressed form, but that in this position it remains on the viewing area as long as the BEAM FINDER switch is locked in the outward position.

32. With the BEAM FINDER switch locked in the outward position, increase the vertical and horizontal deflection factors until the display is reduced to about two divisions vertically and horizontally (when the time-base unit is in the time-base mode, change only the deflection factor of the vertical unit). Adjust the position controls of the vertical unit and time-base unit to center the compressed display about the center lines of the graticule. Press the BEAM FINDER switch in and release. Notice that the display remains within the viewing area.

Calibrator

33. Set the RATE switch to the GATE÷2 position. Notice that the display appears as two horizontal lines. The repetition rate of the displayed signal is one-half that of the gate signal produced by the time-base unit (approximately 10 times the setting of the sweep rate switch). Notice that two individual lines can be obtained alternately when the time-base unit sweep rate switch is set to the slower rates. Also notice that the vertical deflection (separation between the lines) is adjustable with the CALIBRATOR switch.

34. Set the RATE switch to DC. Establish a ground reference level on the CRT (such as center horizontal line of graticule). Set the vertical unit for DC input coupling. Notice that the display is a straight line deflected from the ground reference line by the amplitude selected by the CALIBRATOR switch.

35. If a current-probe amplifier plug-in is available, the current function of the Calibrator can be demonstrated. Install the current-probe amplifier plug-in in the 7503 and press the VERTICAL MODE button which will display this unit. Set the RATE switch to the 1 kHz position and the CALIBRATOR switch to the 40 mA position. Connect the current probe to the 40 mA current loop (observe current direction shown by arrow). Set the deflection factor of the current-probe amplifier to display several divisons of the calibrator waveform. Set the RATE switch to the GATE ÷2 position. Notice that the display is the same amplitude as obtained previously, but that the repetition rate is variable with the time-base unit sweep rate switch. Change the RATE switch to the DC position. Notice that there is no deflection on the CRT. The DC current function can be demonstrated only with a current-probe that is sensitive to DC current.

Z-Axis Input

36. If an external signal is available (five volts peak-to-peak minimum), the function of the Z-AXIS INPUTS can be demonstrated. Remove the BNC caps from both Z-AXIS INPUTS (on rear panel). Connect the external signal to both the input connector of the displayed vertical unit and the HIGH SENSITIVITY connector. Set the sweep rate of the time base to display about five cycles of the waveform. Adjust the amplitude of the signal generator until intensity modulation is visible on the display (change the vertical deflection factor as necessary to produce an on-screen display). The positive peaks of the waveform should be blanked out and the negative peaks intensified. Notice that the setting of the INTENSITY control determines the amount of intensity modulation that is visible.

37. Disconnect the external signal from the HIGH SENSITIVITY connector and reconnect it to the HIGH SPEED connector. Increase the amplitude of the signal generator again until trace modulation is apparent on the displayed waveform. Notice that a higher amplitude signal is necessary to produce trace modulation. Again, the positive peaks

of the waveform should be blanked out and the negative peaks intensified. Also, notice that the setting of the INTENSITY control affects the amount of trace modulation. The major difference between these two methods of obtaining trace modulation is that the HIGH SENSITIVITY input is more sensitive, but the HIGH SPEED input has a higher usable frequency range. Replace the BNC caps on both Z-AXIS INPUTS.

This completes the description of the basic operating procedure for the 7503. Instrument operations not explained here, or operations which need further explanation are discussed under General Operating Information.

TEST SET-UP CHART

General

Fig. 2-4 shows the front, side- and rear-panels of the 7503. This chart may be reproduced and used as a test-setup record for special measurements, applications or procedures, or training purposes.

GENERAL OPERATING INFORMATION

Simplified Operating Instructions

General. The following information is provided to aid in quickly obtaining the correct setting for the 7503 to present a display. The operator should be familiar with the complete function and operation of the instrument as described in this section before using this procedure. For detailed operating information for the plug-in units, see the instruction manuals for the applicable units.

Single-Trace Display. The following procedure will provide a display of a single-trace vertical unit against the time-base unit. For simplicity of explanation, the vertical unit is installed in the LEFT VERT compartment and a time-base unit is installed in the HORIZ compartment. Other compartments can be used if the following procedure is changed accordingly.

1. Install a 7A-series vertical unit in the LEFT VERT compartment.

2. Press the LEFT button of the VERTICAL MODE switch.

3. Install a 7B-series time-base unit in the HORIZ compartment.

4. Press the VERT MODE button of the TRIGGER SOURCE switch.

5. Set the POWER switch to ON. Allow several minutes warmup.

6. Connect the signal to the input connector of the vertical unit.

7. Set the vertical unit for AC input coupling and calibrated deflection factor.

8. Set the time-base unit for auto mode, internal triggering at a calibrated sweep rate of one millisecond/division.

9. Advance the INTENSITY control until a display is visible. (If no display is visible with INTENSITY at about midrange, press the BEAM FINDER switch and adjust the vertical deflection factor until the display is reduced in size vertically; then center the compressed display with vertical and horizontal position controls. Release the BEAM FINDER.) Adjust the FOCUS control for a well-defined display.

10. Set the vertical deflection factor and vertical position control for a display which remains within the graticule area vertically.

11. If necessary, set the time-base triggering controls for a stable display.

12. Adjust the time-base position control so the display begins at the left line of the graticule. Set the time-base sweep rate to display the desired number of cycles.

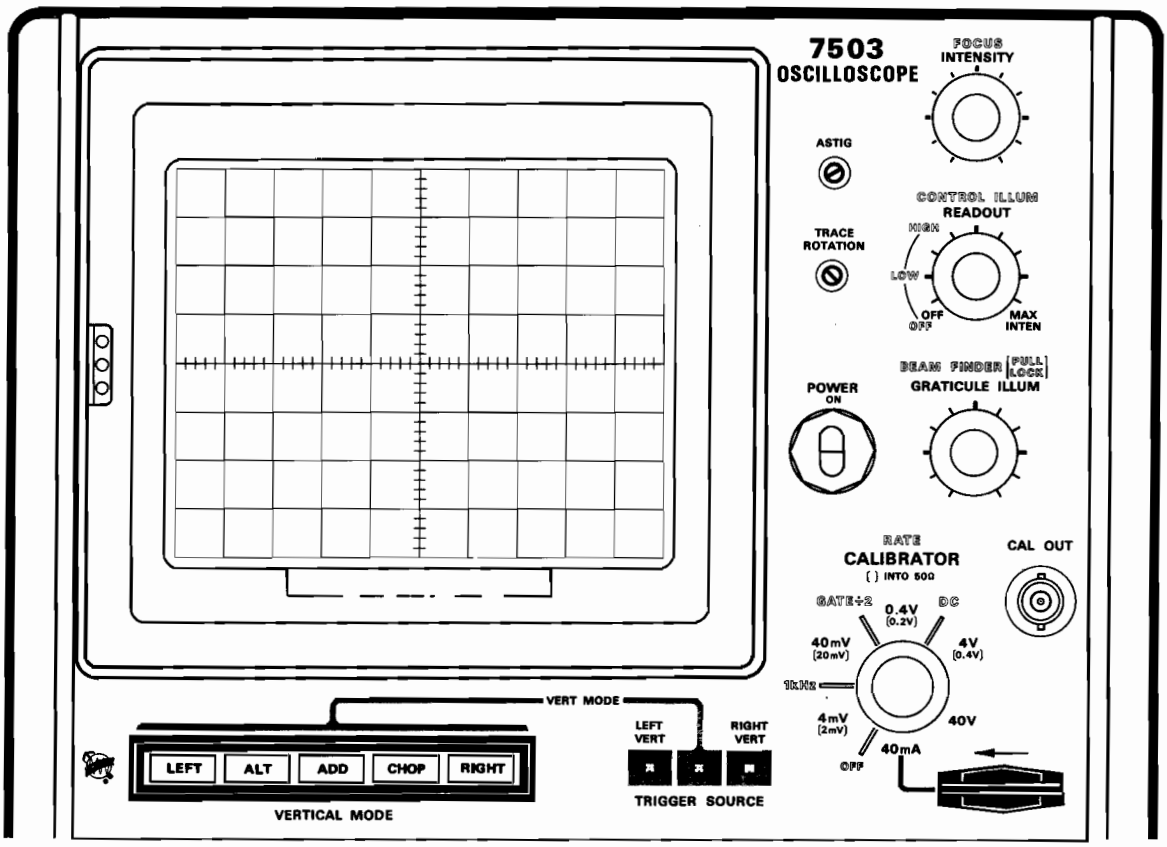
Dual-Trace Display. The following procedure will provide a display of two single-trace vertical units.

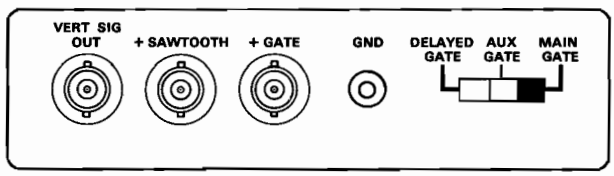
1. Install 7A-series vertical units in both vertical plug-in compartments.

2. Press the LEFT button of the VERTICAL MODE switch.

3. Install a 7B-series time-base unit in the HORIZ compartment.

7503 TEST SETUP CHART





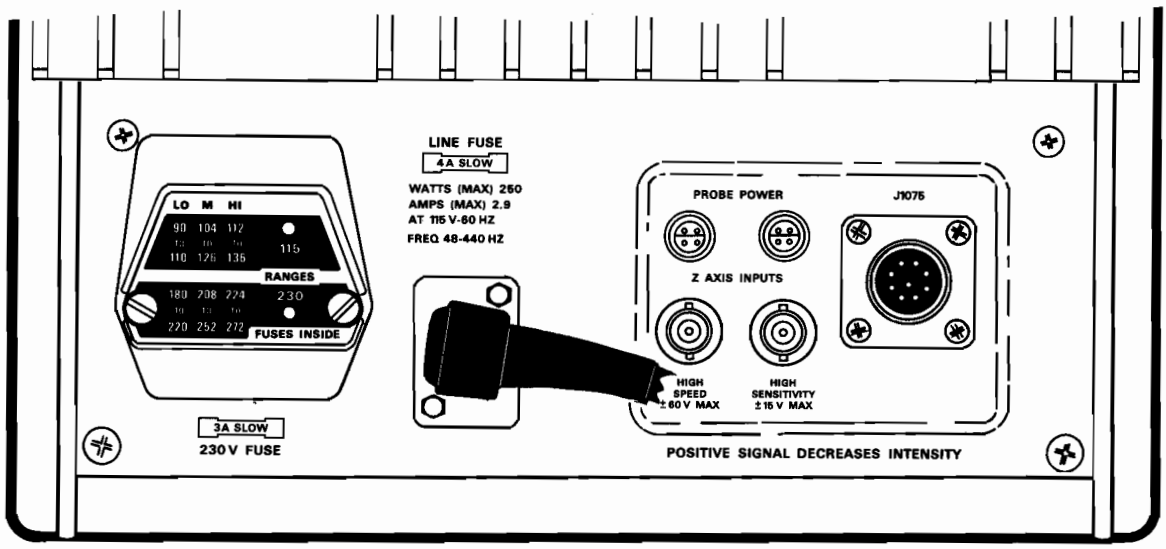


Fig. 2-4.

4. Press the VERT MODE button of the TRIGGER SOURCE switch.

5. Set the POWER switch to ON. Allow several minutes warmup.

6. Connect the signals to the input connectors of the vertical units.

7. Set the vertical units for AC input coupling and calibrated deflection factors.

8. Set the time-base unit for auto mode, internal triggering at a sweep rate of one millisecond/division.

9. Advance the INTENSITY control until a display is visible. (If no display is visible with INTENSITY at midrange, press BEAM FINDER switch and adjust vertical deflection factor until display is reduced in size vertically; then center compressed display with vertical and horizontal position controls. Release the BEAM FINDER.) Set the FOCUS control for a well-defined display.

10. Set the left vertical unit deflection factor for a display about four divisions in amplitude. Adjust the left vertical position control to move this display to the top of the graticule area.

11. Press the RIGHT button of the VERTICAL MODE switch.

12. Set the right vertical unit deflection factor for a display which is about four divisions in amplitude (if display cannot be located, use BEAM FINDER switch). Position this display to the bottom of the graticule area with the right vertical position control.

13. Press the ALT or CHOP button of the VERTICAL MODE switch. A dual-trace display of the signal from the left vertical and right vertical plug-ins should be presented on the CRT. (For more information on choice of dual-trace mode, see Vertical Mode in this section.)

14. If necessary, adjust the time-base triggering controls for a stable display.

15. Adjust the time-base position control so the display begins at the left graticule line. Set the time-base sweep rate for the desired horizontal display.

X-Y Display. The following procedure will provide an X-Y display (one signal versus another, rather than against time).

NOTE

Some 7B-series time-base units have provisions for amplifier operation in the X-Y mode; see X-Y Operation in this section for details of operation in this manner.

1. Install 7A-series amplifier units in both the LEFT VERT and the HORIZ compartments.

2. Press the LEFT button of the VERTICAL MODE switch.

3. Set the POWER switch to ON. Allow several minutes warmup.

4. Connect the X-signal to the amplifier unit in the HORIZ compartment.

5. Connect the Y-signal to the amplifier unit in the LEFT VERT compartment.

6. Set both amplifier units for AC input coupling and calibrated deflection factors.

7. Advance the INTENSITY control until a display is visible. (If no display is visible, press BEAM FINDER switch and adjust the deflection factors of both amplifier units until display is reduced in size both vertically and horizontally; then center compressed display with the position controls. Release BEAM FINDER.)

8. Set the deflection factors of both amplifier units for the desired display and center the display with the position controls. The amplifier unit in the LEFT VERT compartment controls the vertical deflection.

Intensity Controls

The 7503 has two separate intensity controls. The INTENSITY control determines the brightness of the display produced by the plug-in unit in the HORIZ compartment. The READOUT intensity control determines the brightness of only the readout portion of the CRT display.

The setting of the intensity controls may affect the correct focus of the display. Slight re-adjustment of the

FOCUS control may be necessary when the intensity level is changed. To protect the CRT phosphor, do not turn the intensity controls higher than necessary to provide a satisfactory display. The light filters reduce the observed light output from the CRT. When using these filters, avoid advancing the intensity controls too high, as the trace may become de-focused. When the highest intensity display is desired, remove the filters and use only the clear faceplate protector (permanently installed behind bezel). Apparent trace intensity can also be improved in such cases by reducing the ambient light or using a viewing hood. Also, be careful that the INTENSITY control is not set too high when changing the time-base unit sweep rate from a fast to a slow sweep rate, or when changing to the X-Y mode of operation. The instrument incorporates protection circuitry which automatically reduces the display intensity to a lower level when the time-base unit is set to a slow sweep rate. This reduces the danger of damaging the CRT phosphor at these slower sweep rates.

Astigmatism Adjustment

If a well-defined display cannot be obtained with the FOCUS control, adjust the ASTIG adjustment as follows:

NOTE

To check for proper setting of the ASTIG adjustment, slowly turn the FOCUS control through the optimum setting. If the ASTIG adjustment is correctly set, the vertical and horizontal portions of the display will come into sharpest focus at the same position of the FOCUS control. This setting of the ASTIG adjustment should be correct for any display. However, it may be necessary to reset the FOCUS control slightly when the intensity of the display is changed.

1. Connect the CAL OUT connector to the vertical unit with a BNC-to-BNC jumper lead.

2. Set the CALIBRATOR switch to 4 V and the RATE switch to 1 kHz. Adjust the vertical deflection factor to produce a two-or three-division display.

3. Set the time-base unit for a sweep rate of 0.2 millisecond/division.

4. Set the INTENSITY control so the display is at normal intensity (about midrange).

5. Turn the FOCUS control fully counterclockwise and set the ASTIG adjustment to midrange.

6. Adjust the FOCUS control so the top and bottom of the displayed square wave are as thin as possible, but not elongated.

7. Set the ASTIG adjustment so the top and bottom of the displayed square wave are as thin as possible.

8. Repeat parts 6 and 7 for best overall focus.

Trace Alignment Adjustment

If a free-running trace is not parallel with the horizontal graticule lines, set the TRACE ROTATION adjustment as follows: Position the trace to the center horizontal line and adjust the TRACE ROTATION adjustment so the trace is parallel with the horizontal graticule lines.

Graticule

The graticule of the 7503 is marked on the inside of the faceplate of the CRT, providing accurate, no-parallax measurements. The graticule is divided into eight vertical and ten horizontal divisions. Each division is one centimeter square. In addition, each major division is divided into five minor divisions at the center vertical and horizontal lines. The vertical gain and horizontal timing of the plug-ins are calibrated to the graticule so accurate measurements can be made from the CRT. The illumination of the graticule lines can be varied with the GRATICULE ILLUM control.

Fig. 2-5 shows the graticule of the 7503 and defines the various measurement lines. The terminology defined here will be used in all discussions involving graticule measurements.

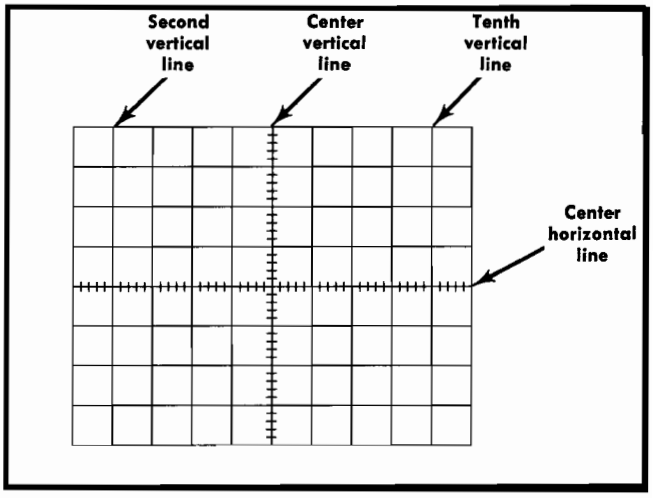


Fig. 2-5. Definition of measurement lines on the 7503 graticule.

Light Filter

The tinted filter provided with the 7503 minimizes light reflections from the face of the CRT to improve contrast when viewing the display under high ambient light conditions. This filter should be removed for waveform photographs or when viewing high-writing-rate displays. To remove the filter, pull outward on the bottom of the plastic CRT mask and remove it from the CRT. Remove the tinted filter (leave the metal light shield in place) and snap the plastic CRT mask back into place. A clear plastic faceplate protector is mounted between the CRT faceplate and the bezel. This faceplate protector should be left in place at all times to protect the CRT faceplate from scratches.

An optional mesh filter is available for use with the 7503. This filter provides shielding against radiated EMI (electro-magnetic interference) from the face of the CRT. It also serves as a light filter to make the trace more visible under high ambient light conditions. The mesh filter fits in place of the plastic CRT mask. The filter can be ordered by Tektronix Part No. 378-0603-00.

Beam Finder

The BEAM FINDER switch provides a means of locating a display which overscans the viewing area either vertically or horizontally. When the BEAM FINDER switch is pressed, the display is compressed within the graticule area. This switch can also be pulled outward to lock it in the beam-finder position. The latter feature is convenient when attempting to locate traces from more than one of the plug-in units in the 7503. Press the BEAM FINDER switch in to release it from the locked position. To locate and re-position an overscanned display, use the following procedure:

1. Press the BEAM FINDER switch in (or if desired, pull it outward to lock position).

2. While the display is compressed, increase the vertical and horizontal deflection factors until the vertical deflection is reduced to about two divisions and the horizontal deflection is reduced to about four divisions (the horizontal deflection needs to be reduced only when in the X-Y mode of operation).

3. Adjust the vertical and horizontal position controls to center the display about the vertical and horizontal center lines of the graticule.

4. Release the BEAM FINDER switch; the display should remain within the viewing area.

Control Illumination

The CONTROL ILLUM switch determines the illumination level of the pushbutton switches on the 7503 and the associated plug-in units. This switch controls the illumination of only the pushbutton switches on the plug-in units and does not affect the intensity of lights which are used as function indicators (for example, it does not affect the illumination of the ready light on a time-base unit which has the single-sweep feature). In the OFF position, all pushbutton lights on the 7503 and the associated plug-ins are off. In the LOW position, the selected buttons are illuminated at low intensity. This is the recommended position for the CONTROL ILLUM switch, since it provides an adequate indication of switch position and also results in longest bulb life. The HIGH position provides maximum intensity for the pushbuttons and can be used so the selected switch is obvious even under high ambient light conditions.

Readout

NOTE

If the Readout System is not installed in this instrument (Option 1), disregard the following information. Also, the READOUT control has no effect upon instrument operation in this case.

The Readout System of the 7503 allows alpha-numeric display of information on the CRT along with the analog waveform displays. The information displayed by the Readout System is obtained from the plug-in units which are installed in the plug-in compartments. The characters of the readout display are written by the CRT beam on a time-shared basis with the signal waveforms. However, the waveform display is interrupted for only about 20 microseconds for each character that is displayed. Only about 0.1% of total available display time (including retrace and holdoff time of time-base unit) is used to display each character.

The readout information from each plug-in is called a word. Up to six words of readout information can be displayed on the 7503 CRT (two channels from each of the three plug-in compartments). The location at which each readout word is presented is fixed, and is directly related to the plug-in unit and channel from which it originated. Fig. 2-6 shows the area of the graticule where the readout from each plug-in unit and/or channel is displayed. Notice that the readout from channel 1 of each plug-in unit is displayed within the top division of the graticule, and the readout from channel 2 is displayed directly below within the bottom division of the graticule. Only the readout from plug-ins and/or channels which are selected for display by the VERTICAL MODE switch, or by the mode switches of dual-channel plug-ins, appear in the readout display.

An "identify" feature is provided by the Readout System to link the readout word with the originating plug-

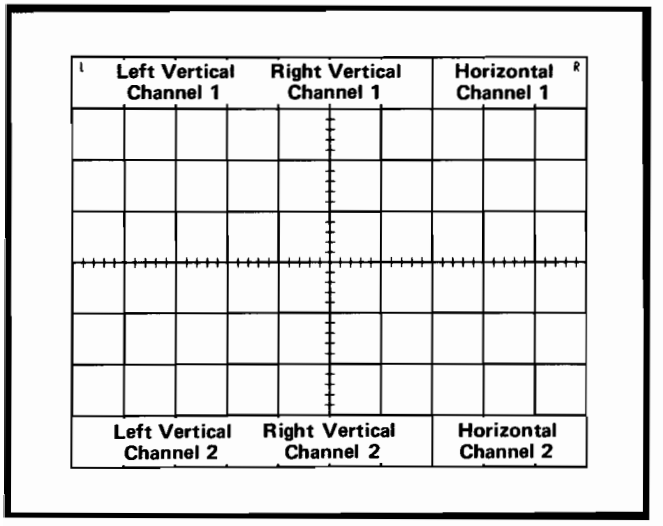


Fig. 2-6. Location of readout words on the CRT identifying the originating plug-in and channel.

in unit and channel (amplifier units only). When the "Identify" button of an amplifier unit is pressed, the word IDENTIFY appears in the readout location allocated to that plug-in and channel. Other readout words in the display remain unchanged. When the "Identify" button is released, the readout display from this plug-in channel is again displayed. Circuitry may be provided in the amplifier unit which produces a noticeable change in the analog waveform display to also identify the associated trace when the "Identify" button is pressed; see the plug-in instruction manual for details.

The READOUT control determines the intensity of the readout portion of the display only, independent of the other traces. The Readout System is inoperative in the fully counterclockwise OFF position. This may be desirable when the top and bottom divisions of the graticule are to be used for waveform display, or when the trace interruptions necessary to display characters do not allow satisfactory waveform display to be obtained.

Vertical Mode

Left and Right Mode. When the LEFT or RIGHT button of the VERTICAL MODE switch is pressed, only the signal from the plug-in unit in the selected compartment is displayed.

Alternate Mode. The ALT position of the VERTICAL MODE switch produces a display which alternates between the plug-in units in the LEFT VERT and RIGHT VERT compartments with each sweep on the CRT. Although the ALT mode can be used at all sweep rates, the CHOP mode provides a more satisfactory display at sweep rates below about 20 milliseconds/division. At these slower sweep rates, alternate-mode switching becomes visually perceptible.

The TRIGGER SOURCE switch allows selection of the triggering for an alternate display. When the switch is set to the VERT MODE position, each sweep is triggered by the signal being displayed on the CRT. This provides a stable display of two unrelated signals, but does not indicate the time relationship between the signals. In either the LEFT VERT or the RIGHT VERT positions, the two signals are displayed showing true time relationship. However, if the signals are not time-related, the display from the plug-in which is not providing a trigger signal will appear unstable on the CRT.

Chopped Mode. The CHOP position of the VERTICAL MODE switch produces a display which is electronically switched between channels at a one-megahertz rate. In general, the CHOP mode provides the best display at sweep rates slower than about 20 milliseconds/division, or whenever dual-trace, single-shot phenomena are to be displayed. At faster sweep rates, the chopped switching becomes apparent and may interfere with the display.

Correct internal triggering for the CHOP mode can be obtained in any of the three positions of the TRIGGER SOURCE switch. When the TRIGGER SOURCE switch is set to VERT MODE, the internal trigger signals from the vertical plug-ins are algebraically added and the time-base unit is triggered from the resultant signal. Use of the LEFT VERT or RIGHT VERT trigger-source positions triggers the time-base unit on the internal trigger signal from the selected vertical unit only. This allows two time-related signals to be displayed showing true time relationship. However, if the signals are not time-related, the display from the channel which is not providing the trigger signal will appear unstable. The CHOP mode can be used to compare two single-shot, transient, or random signals which occur within the time interval determined by the time-base unit (ten times selected sweep rate). To provide correct triggering, the display which provides the trigger signal must precede the second display in time. Since the signals show true time relationship, time-difference measurements can be made from the display.

Algebraic Addition. The ADD position of the VERTICAL MODE switch can be used to display the sum or difference of two signals, for common-mode rejection, to remove an undesired signal, or for DC offset (applying a DC voltage to one channel to offset the DC component of a signal on the other channel). The common-mode rejection ratio between the vertical plug-ins of the 7503 is greater than 20:1 at 75 megahertz. The rejection ratio increases to 100:1 at DC.

The overall deflection on the CRT in the ADD mode is the resultant of the algebraic addition of the signals from the two vertical plug-in units. It is difficult to determine the voltage amplitude of the resultant display, unless the ampli-

tude of the signal applied to one of the plug-ins is known. This is particularly true when the vertical units are set to different deflection factors, since it is not obvious which portion of the display is a result of the signal applied to either plug-in unit. Also, the polarity and repetition rate of the applied signals enters into the calculation.

The following general precautions should be observed to provide the best display when using the ADD mode.

1. Do not exceed the input voltage rating of the plug-in units.

2. Do not apply large signals to the plug-in inputs. A good rule to follow is not to apply a signal which exceeds an equivalent of about eight times the vertical deflection factors. For example, with a vertical deflection factor of 0.5 volt/division, the voltage to that plug-in should not exceed four volts. Larger voltages may result in a distorted display.

3. To ensure the greatest dynamic range in the ADD mode, set the position controls of the plug-in units to a setting which would result in a mid-screen display if viewed in the LEFT or RIGHT positions of the VERTICAL MODE switch.

4. For similar response from each channel, set the plug-in units for the same input coupling.

Trigger Source

The TRIGGER SOURCE switch allows selection of the internal trigger for the time-base unit. For most applications, this switch can be set to the VERT MODE position. This position is the most convenient, since the internal trigger signal is automatically switched as the VERTICAL MODE switch is changed, or as the display is electronically switched between the LEFT VERT and RIGHT VERT plug-ins in the ALT position of the VERTICAL MODE switch. It also provides a usuable trigger signal in the ADD or CHOP positions of the VERTICAL MODE switch, since the internal trigger signal in these modes is the algebraic sum of the signals applied to the vertical plug-in units. Therefore, the VERT MODE position ensures that the time-base unit receives a trigger signal regardless of the VERTICAL MODE switch setting, without the need to change the trigger source selection. However, if correct triggering for the desired display is not obtained in the VERT MODE position, the trigger source can be changed to obtain the trigger signal from either the LEFT VERT or RIGHT VERT plug-in. The internal trigger signal is obtained from the selected vertical compartment, whether the plug-in in that compartment is selected for display on the CRT or not. If the internal trigger signal is obtained from one of the vertical units but the other vertical unit is selected for display, the internal trigger signal must be time-related to the displayed signal in order to obtain a triggered (stable) display.

X-Y Operation

In some applications, it is desirable to display one signal versus another (X-Y) rather than against time (internal sweep). The flexibility of the plug-in units available for use with the 7503 provides a means for applying an external signal to the horizontal deflection system for this type of display. Some of the 7B-series time-base units can be operated as amplifiers in addition to their normal use as time-base generators. This feature allows an external signal to provide the horizontal deflection on the CRT. For most of the time-base units with the amplifier function, the X (horizontal) signal can be connected either to an external input connector on the time-base unit or it can be routed to the time-base unit through the internal triggering system (see time-base instruction manual for details). If the latter method is used, the TRIGGER SOURCE switch must be set so that the X (horizontal) signal is obtained from one of the vertical units and the Y (vertical) signal is obtained from the other vertical unit. It is advantageous to use the internal trigger system to provide the X signal, since the attenuator switch of the amplifier unit providing the horizontal signal determines the horizontal deflection factor, to allow full-range operation; and also, the plug-in units do not have to be moved between compartments when X-Y operation is desired.

Another way to obtain an X-Y display is to install an amplifier plug-in unit in the horizontal plug-in compartment. (Check amplifier unit gain as given in the plug-in instruction manual to obtain calibrated horizontal deflection factors.) This method provides the best X-Y display, particularly if two identical amplifier units are used, since both the X and Y input systems will have the same delay time, gain characteristics, input coupling, etc. For further information on obtaining X-Y displays, see the plug-in unit manuals. Also, the reference books listed under Applications provide information on X-Y measurements and interpreting the resultant lissajous displays.

An X-Y delay compensation network is automatically switched into the horizontal deflection system when an amplifier plug-in unit is installed in the HORIZ compartment, or when a time-base unit is operated in the amplifier mode. This network provides close delay-matching between the vertical and horizontal deflection systems up to two megahertz for use in X-Y applications which require precise phase measurement.

Intensity Modulation

Intensity (Z-axis) modulation can be used to relate a third item of electrical phenomena to the vertical (Y-axis)

and the horizontal (X-axis) coordinates, without affecting the waveshape of the displayed signal. The Z-axis modulating signal applied to the CRT circuit changes the intensity of the displayed waveform to provide this type of display. "Gray scale" intensity modulation can be obtained by applying signals which do not completely blank the display. Large amplitude signals of the correct polarity will completely blank the display; the sharpest display is provided by signals with a fast rise and fall. The voltage amplitude required for visible trace modulation depends on the setting of the INTENSITY control.

Time markers applied to the Z-AXIS INPUTS provide a direct time reference on the display. With uncalibrated horizontal sweep or X-Y mode operation, the time markers provide a means of reading time directly from the display. However, if the markers are not time-related to the displayed waveform, a single-sweep display should be used (for internal sweep only) to provide a stable display.

Two modes of intensity modulation are provided in the 7503. The following discussions list the use and limitations of each mode.

HIGH SENSITIVITY Input. The HIGH SENSITIVITY input (on rear panel) permits intensity modulation of the CRT display through the Z-axis Amplifier circuit. A two-volt peak-to-peak signal will completely blank the display, even at maximum intensity levels. Lower amplitude signals can be used to just change the trace brightness, rather than completely blank the display. Negative-going modulating signals increase the display intensity, and positive-going modulating signals decrease the display intensity. Bandwidth for this mode of intensity modulation is DC to 10 megahertz (input voltage derating necessary above two megahertz). The maximum input voltage in this mode should be limited to 15 volts (DC plus peak AC). Since this input is the most sensitive, it can be used for all applications requiring bandwidth of 10 megahertz or less. When the HIGH SENSITIVITY input is not in use, replace the BNC cap.

HIGH SPEED Input. Intensity modulation signals connected to the HIGH SPEED connector (on rear panel) are connected primarily to the cathode circuit of the CRT. A 60-volt peak-to-peak signal will provide complete blanking of the display, even at maximum intensity settings. Negative-going modulating signals increase the display intensity, and positive-going modulating signals decrease the display intensity. Bandwidth for this mode is DC to 75 megahertz. Maximum input voltage for signals connected to the HIGH SPEED input is 60 volts (DC plus peak AC). Replace the grounding BNC cap when the HIGH SPEED input is not in use.

Raster Displays

A raster-type display can be used to effectively increase the apparent sweep length. For this type of display, the trace is deflected both vertically and horizontally by sawtooth signals. This is accomplished in the 7503 by installing a 7B-series time-base unit in one of the vertical plug-in compartments. Normally, the time-base unit in the vertical compartment should be set to a slower sweep rate than the time-base unit in the horizontal compartment; the number of horizontal traces in the raster depends upon the ratio between the two sweep rates. Information can be displayed on the raster using several different methods. In the ADD position of the VERTICAL MODE switch, the signal from an amplifier unit can be algebraically added to the vertical deflection. With this method, the vertical signal amplitude on the CRT should not exceed the distance between the horizontal lines of the raster. Another method of displaying information on the raster is to use the Z-AXIS INPUTS to provide intensity modulation of the display. Complete information on operation using the Z-axis feature is given under Intensity Modulation. This type of raster display could be used to provide a television-type display.

To provide a stable raster display, both time-base units must be correctly triggered. Internal triggering is not provided for the time-base unit when operated in the vertical compartments; external triggering must be used. Also, blanking is not provided from the time-base unit when operated in a vertical compartment. To blank out the retrace portion from the time-base unit in the vertical compartment, special connections must be made from this time-base unit to the blanking network of the 7503.

Calibrator

General. The internal calibrator of the 7503 provides a convenient signal source for checking basic vertical gain and sweep timing. The calibrator output signal is also very useful for adjusting probe compensation as described in the probe instruction manual. In addition, the calibrator can be used as a convenient signal source for application to external equipment.

Voltage. The calibrator provides accurate output voltages at the CAL OUT connector from four millivolts to 40 volts in decade steps into high impedance loads. In addition, the positions from 4 mV to 4 V provide an output of two millivolts to 0.4 volt into 50 ohms (shown on front panel in brackets). The output voltage is selected by the CALIBRATOR switch. The output voltage is available at the front-panel CAL OUT connector.

Current. The current loop provides a 40-milliampere output current which can be used to check and calibrate current-measuring probe systems. The current signal is obtained by clipping the probe around the current loop. The

arrow above the current loop indicates conventional current flow; i.e., from plus to minus.

Repetition Rate. The calibrator circuit uses frequency-stable components to maintain accurate frequency and constant duty cycle. Thus, the calibrator can be used for checking the basic sweep timing of time-base units (one-kilohertz rate only). The RATE switch selects the repetition rate of the calibrator. Two positions of the RATE switch provide a square-wave output signal either at the CAL OUT connector or through the current loop. In the 1 kHz position, the repetition rate of the calibrator is one kilohertz. The GATE ÷2 position of the RATE switch provides a variable calibrator repetition rate. In this position, the repetition rate of the calibrator output signal is one-half the repetition rate of the gate signal produced by the time-base unit in the HORIZ compartment (length of gate is about ten times the setting of the sweep rate switch). This position of the RATE switch allows selection of repetition rate of the calibrator output signal by changing the sweep rate of the time-base unit in the HORIZ compartment. The calibrator circuit maintains a constant 50% duty cycle on the output waveform, regardless of the repetition rate.

In the DC position, positive DC voltage levels are available at the CAL OUT connector; the amplitude of the DC voltage is determined by the setting of the CALIBRATOR switch to one of the voltage ranges. When the CALIBRATOR switch is set to the 40 mA position, a DC current of 40 mA is provided through the current loop.

Wave Shape. The square-wave output signal of the calibrator can be used as a reference wave shape when checking or adjusting the compensation of passive, high-resistance probes. Since the square-wave output from the calibrator has a flat top, any distortion in the displayed waveform is due to the probe compensation.

Signal Outputs

+ Sawtooth. The + SAWTOOTH connector provides a positive-going sample of the sawtooth signal from the time-base unit in the horizontal plug-in compartment. Rate of rise of the sawtooth output signal is about 50 millivolts/unit of time into a 50-ohm load or about one volt/unit of time into a one-megohm load. Unit of time is determined by the time-base time/division switch (e.g., if time/ division is set to one millisecond/division, a unit of time is one millisecond; at five milliseconds/division, a unit of time is five milliseconds). The peak output voltage is greater than 500 millivolts into a 50-ohm load or greater than 10 volts into a one-megohm load.

+ Gate. The + GATE output connector provides a positive-going rectangular output pulse from the time-base unit in the horizontal plug-in compartment. The Gate switch allows the output signal to be selected from the displayed sweep, or the delayed gate from a delaying-sweep time-base unit, or the AUX GATE from a dual- sweep time-base unit. Duration of the gate output signal is the same as the duration of the sweep or, in the case of the delayed gate, it ends at the end of the delay period. Amplitude of the output signal at the + GATE connector is about 0.5 volt into 50 ohms, or about 10 volts into one megohm.

Vertical Signal. The VERT SIG OUT connector provides a sample of the vertical deflection signal. The source of the output signal at this connector is determined by the TRIGGER SOURCE switch. In the VERT MODE position of the TRIGGER SOURCE switch, the output signal is determined by the setting of the VERTICAL MODE switch. The output signal in the LEFT and RIGHT positions of the VERTICAL MODE switch is obtained only from the selected vertical unit. In the ALT position of the VERTICAL MODE switch, the output signal at the VERT SIG OUT connector switches between vertical units along with the CRT display. However, the vertical output signal in the CHOP position is a composite signal, and is the same as obtained in the ADD position due to the requirements of the triggering system. The LEFT VERT and RIGHT VERT positions of the TRIGGER SOURCE switch provide the vertical output signal only from the selected vertical unit, even when it is not selected for display. The output voltage into a 50-ohm load is about 25 millivolts/division of CRT display and about 0.5 volt/division of display into a one-megohm load. The bandwidth of the output signal is determined by the vertical plug-in unit used (see Systems Specification given in Section 1).

Probe Power Connectors

The two PROBE POWER connectors on the rear panel provide operating power for active probe systems. It is not recommended that these connectors be used as a power source for applications other than the compatible probes or other accessories which are specifically designed for use with this system.

Remote Connector

The nine-terminal connector J1075 on the rear panel of the 7503 provides input for remote operation of the instrument and the associated plug-in unit. Table 2-2 lists the function of each terminal of J1075. The mating connector for J1075 is Tektronix Part No. 134-0049-00 (one mating connector supplied as standard accessory). The methods of obtaining remote single-sweep reset and ready indication are given under Remote Single-Sweep Reset. Notice that there are several blank terminals on J1075. These terminals can be used for special remote applications.

Remote Single-Sweep Reset

Remote single-sweep reset operation can be provided to 7B-series time-base units with compatible features through rear-panel connector J1075. The remote single-sweep reset actuation can be obtained from either an active system (pulse generator, logic circuit, etc.) or a passive system (switch or relay). Input requirements for remote single-sweep reset operation are: Closure to ground (−5 volts to −0.5 volt provides actuation) at 10 milliamperes maximum current; minimum pulse width of 10 microseconds at 50% amplitude points; 15 volts maximum input voltage.

TABLE 2-2

Remote Connections

J1075 Terminal	Function
A	Remote single-sweep reset
B	Chassis ground
C	Remote ready indicator
D	No connection
E	No connection
F	No connection
H	No connection
J	No connection
K	No connection

Fig. 2-7 shows a typical passive system to provide remote single-sweep reset operation. The remote ready light is optional and can be used with an active or passive system whenever it is necessary to provide an indication at the remote location that reset has occurred.

Applications

The 7503 Oscilloscope and its associated plug-in units provide a very flexible measurement system. The capabilities of the overall system depend mainly upon the plug-ins chosen for use with this instrument. Specific applications for the individual plug-in units are described in the plug-in unit manuals. The overall system can also be used for many applications which are not described in detail either in this manual or in the manuals for the individual plug-in units. Contact your local Tektronix Field Office or representative for assistance in making specific measurements with this instrument.

The following books describe oscilloscope measurement techniques which can be adapted for use:

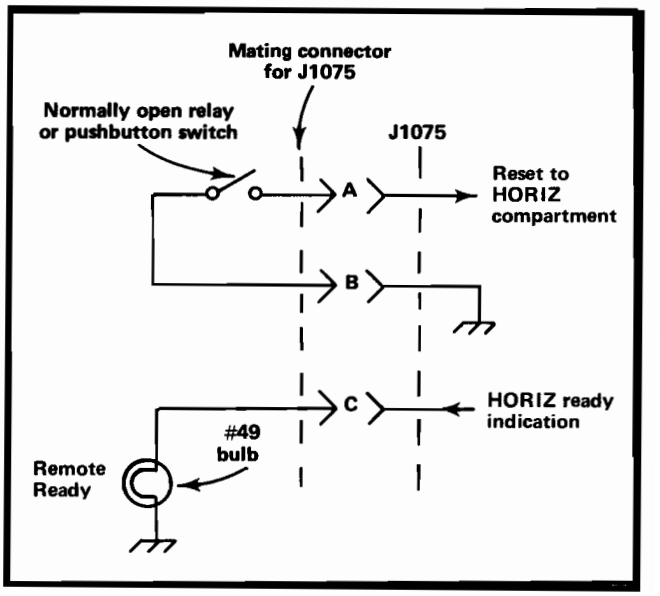


Fig. 2-7. Typical circuit for remote single-sweep reset operation.

Harley Carter, "An Introduction to the Cathode Ray Oscilloscope", Philips Technical Library, Cleaver-Hume Press Ltd., London, 1960.

J. Czech, "Oscilloscope Measuring Techniques", Philips Technical Library, Springer-Verlag, New York, 1965.

Robert G. Middleton and L. Donald Payne, "Using the Oscilloscope in Industrial Electronics", Howard W. Sams & Co. Inc., The Bobbs-Merrill Company Inc., Indianapolis, 1961.

John F. Rider and Seymour D. Uslan, "Encyclopedia of Cathode-Ray Oscilloscopes and Their Uses", John F. Rider Publisher Inc., New York, 1959.

John F. Rider, "Obtaining and Interpreting Test Scope Traces," John F. Rider Publisher Inc., New York, 1959.

Rufus P. Turner, "Practical Oscilloscope Handbook", Volumes 1 and 2, John F. Rider Publisher Inc., New York, 1964.

SECTION 3
CIRCUIT DESCRIPTION

Change information, if any, affecting this section will be found at the rear of this manual.

Introduction

This section of the manual contains a description of the circuitry used in the 7503 Oscilloscope. The description begins with a discussion of the instrument using the basic block diagram shown in Fig. 3-1. Then, each circuit is described in detail using detailed block diagrams to show the interconnections between the stages in each major circuit and the relationship of the front-panel controls to the individual stages.

A complete block diagram is located in the Diagrams section at the back of this manual. This block diagram shows the overall relationship between all of the circuits. Complete schematics of each circuit are also given in the Diagrams section. Refer to these diagrams throughout the following circuit description for electrical values and relationships.

BLOCK DIAGRAM

General

The following discussion is provided to aid in understanding the overall concept of the 7503 before the individual circuits are discussed in detail. A basic block diagram of the 7503 is shown in Fig. 3-1. Only the basic interconnections between the individual blocks are shown on this diagram. Each block represents a major circuit within the instrument. The number on each block refers to the complete circuit diagram which is located at the rear of this manual.

Vertical signals to be displayed on the CRT are applied to the Vertical Interface circuit from both vertical plug-in compartments. The vertical Interface circuit determines whether the signal from the left and/or right vertical unit displayed. The vertical signal selected is then amplified by the Vertical Amplifier circuit to bring it to the level necessary to drive the vertical deflection plates of the CRT. This circuit also includes an input to produce the vertical portion of a readout display.

Horizontal signals for display on the CRT are connected to the X-Y Delay Compensation and Horizontal Amplifier circuit from the horizontal plug-in compartment. The X-Y Delay Compensation network provides a delay for the horizontal (X) portion of an X-Y display to match the delay of the vertical (Y) signal due to the delay line. The horizontal signal is connected to the Horizontal Amplifier circuit, which amplifies it to provide the horizontal deflection for the CRT. This circuit also accepts the X-signal from the Readout System to produce the horizontal portion of a readout display. The Readout System provides alpha-numeric display of information encoded by the plug-in units. This display is presented on the CRT and is written by the CRT beam on a time-shared basis with the analog waveform display.

The internal trigger signals from the vertical plug-in units are connected to the Trigger Selector circuit. This circuit selects the trigger signal which is connected to the horizontal plug-in unit. It also provides the drive signal for the Output Signals circuit to produce an output which is a sample of the vertical signal. The Output Signals circuit also provides a sample of the sawtooth signal and a gate signal from a time-base unit in the horizontal compartment. The Calibrator circuit produces a square-wave output with accurate amplitude which can be used to check the calibration of this instrument and the compensation of probes. The repetition rate of the output signal is selectable; either DC, one kilohertz, or one-half the sweep gate. This signal is available as a voltage at the CAL OUT connector or as a current through the 40 mA current loop.

The Logic Circuit develops control signals for use in other circuits within this instrument and the plug-in units. These output signals automatically determine the correct instrument operation in relation to the plug-ins installed and/or selected, plug-in control settings, and 7503 control settings. The Z-Axis Amplifier circuit provides the drive signal to control the CRT intensity level through the CRT Circuit. The CRT Circuit produces the voltages and contains the controls necessary for operation of the cathode-ray tube.

The Low-Voltage Power Supply circuit provides the power necessary for operation of this instrument. This voltage is connected to all circuits within the instrument. The Mode Switching and Rear Panel Connectors circuit shows the switching logic of the front-panel controls. It also includes the input network for the Z-AXIS INPUTS and the output connectors to supply probe power to active probe systems.

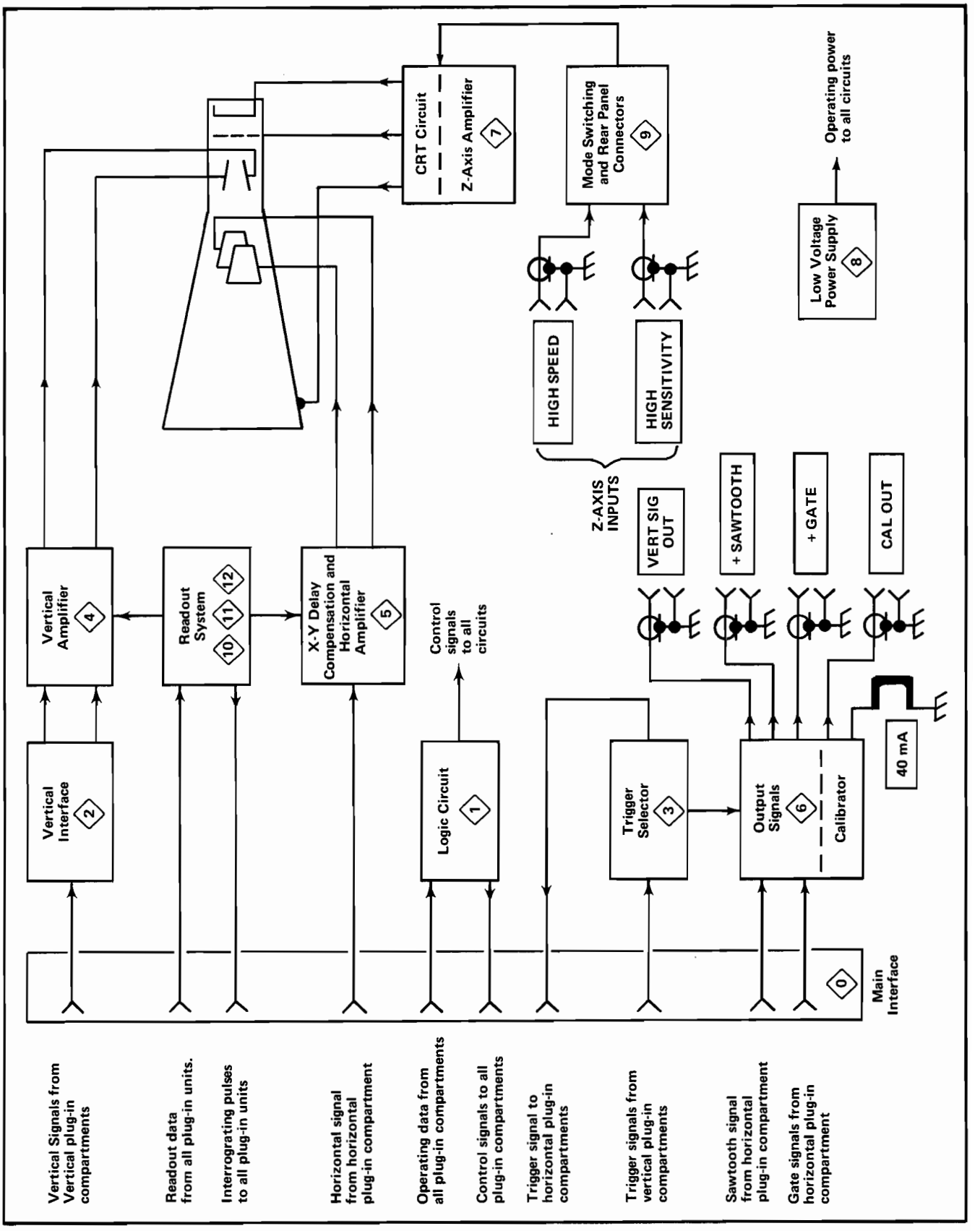


Fig. 3-1. Basic block diagram of the 7503 Oscilloscope.

CIRCUIT OPERATION

General

This section provides a detailed description of the electrical operation and relationship of the circuits in the 7503 Oscilloscope. The theory of operation for circuits unique to this instrument is described in detail in this discussion. Circuits which are commonly used in the electronics industry are not described in detail. If more information is desired on these commonly used circuits, refer to the following textbooks:

Tektronix Circuit Concepts Books (order from your local Tektronix Field Office or representative):

Cathode-Ray Tubes, Tektronix Part No. 062-0852-01.

Oscilloscope Trigger Circuits, Tektronix Part No. 062-1056-00.

Power Supply Circuits, Tektronix Part No. 062-0888-01.

Sweep Generator Circuits, Tektronix Part No. 062-1098-00.

Phillip Cutler, "Semiconductor Circuit Analysis", McGraw-Hill, New York, 1964.

Lloyd P. Hunter (Ed.), "Handbook of Semiconductor Electronics", second edition, McGraw-Hill, New York, 1964.

Jacob Millman and Herbert Taub, "Pulse, Digital, and Switching Waveforms", McGraw-Hill, New York, 1965.

The following circuit analysis is written around the detailed block diagrams which are given for each major circuit. These detailed block diagrams give the names of the individual stages within the major circuits, and show how they are connected together to form the major circuits. The block diagrams also show the inputs and outputs for each circuit and the relationship of the front-panel controls to the individual stages. The circuit diagrams from which the detailed block diagrams are derived are shown in the Diagrams section.

NOTE

All references to direction of current in this manual are in terms of conventional current; i.e., from plus to minus.

LOGIC FUNDAMENTALS

General

Digital logic techniques are used to perform many functions within this instrument. The function and operation of the logic circuits are described using logic symbology and terminology. This portion of the manual is provided to aid in the understanding of these symbols and terms. The following information is a basic introduction to logic concepts, not a comprehensive discussion of the subject. For further information on binary number systems and the associated Boolean Algebra concepts, the derivation of logic functions, a more detailed analysis of digital logic, etc., refer to the following textbooks:

Tektronix Circuit Concepts booklet, "Digital Concepts", Tektronix Part No. 062-1030-00.

Robert C Baron and Albert T. Piccirilli, "Digital Logic and Computer Operations", McGraw-Hill, New York, 1967.

Thomas C. Bartee, "Digital Computer Fundamentals", McGraw-Hill, New York, 1966.

Yaohan Chu, "Digital Computer Design Fundamentals", McGraw-Hill, New York, 1962.

Joseph Millman and Herbert Taub, "Pulse, Digital, and Switching Waveforms", McGraw-Hill, New York, 1965, Chapters 9-11.

Symbols

The operation of circuits within the 7503 which use digital techniques is described using the graphic symbols set forth in military standard MIL-STD-806B. Table 3-1 provides a basic logic reference for the logic devices used within this instrument. Any deviations from the standard symbology, or devices not defined by the standard will be described in the circuit description for the applicable device.

Logic Polarity

All logic functions are described using the positive logic convention. Positive logic is a system of notation where the more positive of two levels (HI) is called the true or 1-state; the more negative level (LO) is called the false or 0-state. The HI-LO method of notation is used in this logic description. The specific voltages which constitute a HI or LO state vary between individual devices.

NOTE

The HI-LO logic notation can be conveniently converted to 1-0 notation by disregarding the first letter of each state. For example:

HI = HI
LO = LO

Wherever possible, the input and output lines are named to indicate the function they perform when at the HI (true) state. For example, the line labeled "Display Right Command" means that the Right Vertical unit will be displayed when this line is HI or true. Likewise, the line labeled "X-Compensation Inhibit" means that the X-Compensation function is inhibited or disabled when this line is HI.

Input/Output Tables

Input/output (truth) tables are used in conjunction with the logic diagrams to show the input combinations which are of importance to a particular function, along with the resultant output conditions. This table may be given either for an individual device or for a complete logic stage. For examples of input/output tables for individual devices, see Table 3-1.

Non-Digital Devices

It should be noted that not all of the integrated circuit devices in this instrument are digital logic devices. The functions of non-digital devices will be described individually using operating waveforms or other techniques to illustrate their function.

TABLE 3-1

Basic Logic Reference

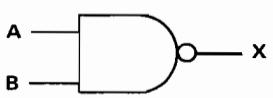
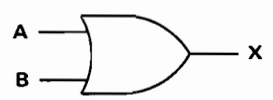
Device	Symbol	Description	Input/Output Table
AND gate		A device with two or more inputs and one output. The output of the AND gate is HI if and only if all of the inputs are at the HI state.	Input / Output A B X LO LO LO LO HI LO HI LO LO HI HI HI
NAND gate		A device with two or more inputs and one output. The output of the NAND gate is LO if and only if all of the inputs are at the HI state.	Input / Output A B X LO LO HI LO HI HI HI LO HI HI HI LO
OR gate		A device with two or more inputs and one output. The output of the OR gate is HI if one or more of the inputs are at the HI state.	Input / Output A B X LO LO LO LO HI HI HI LO HI HI HI HI

TABLE 3-1 (cont.)

Basic Logic Reference

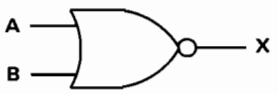
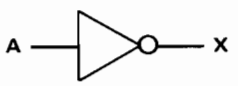
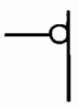
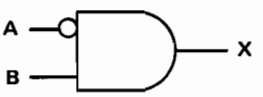
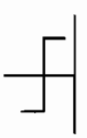
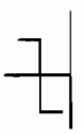
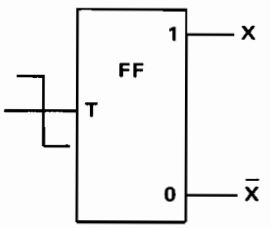
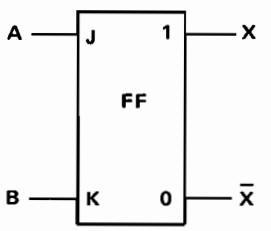
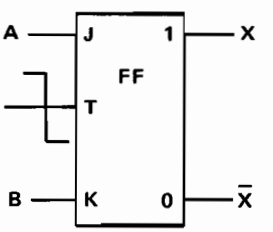
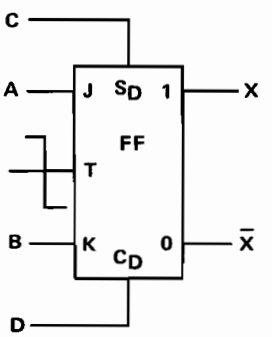
Device	Symbol	Description	Input/Output Table
NOR gate		A device with two or more inputs and one output. The output of the NOR gate is LO if one or more of the inputs are at the HI state.	Input / Output A B X LO LO HI LO HI LO HI LO LO HI HI LO
Inverter		A device with one input and one output. The output state is always opposite to the input state.	Input / Output A X LO HI HI LO
LO-state indicator		A small circle at the input or output of a symbol indicates that the LO state is the significant state. Absence of the circle indicates that the HI state is the significant state. Two examples follow:	
		AND gate with LO-state indicator at the A input. The output of this gate is HI if and only if the A input is LO and the B input is HI.	Input / Output A B X LO LO LO LO HI HI HI LO LO HI HI LO
		OR gate with LO-state indicator at the A input: The output of this gate is HI if either the A input is LO or the B input is HI.	Input / Output A B X LO LO HI LO HI HI HI LO LO HI HI HI
Edge symbol		Normally superimposed on an input line to a logic symbol. Indicates that this input (usually the trigger input of a flip-flop) responds to the indicated transition of the applied signal.	
			

TABLE 3-1 (cont.)

Basic Logic Reference

Device	Symbol	Description	Input/Output Table
Triggered (toggle) Flip-Flop		A bistable device with one input and two outputs which changes output states from one stable state to the other stable state with each trigger (either or both outputs may be used). The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity depending on the device.	Input / Output Condition before trigger pulse: X, $\bar{X}$ — Condition after trigger pulse: X, $\bar{X}$ LO, HI — HI, LO HI, LO — LO, HI
Set-Clear (J-K) Flip-Flop		A bistable device with two inputs and two outputs which changes output states in response to the states at the inputs (either or both outputs may be used). The outputs are complementary (i.e., when one output is HI the other is LO).	Input / Output A, B — X, $\bar{X}$ LO, LO — No change LO, HI — LO, HI HI, LO — HI, LO HI, HI — Changes state
Triggered Set-Clear (J-K) Flip-Flop	Without direct inputs  With direct inputs 	A bistable device with three or more inputs and two outputs (either or both inputs may be used). When triggered, the output changes states in response to the states at the inputs prior to the trigger. The outputs are complementary (i.e., when one output is HI the other is LO). The edge symbol on the trigger (T) input may be of either polarity depending on the device. For devices with direct-set (S_D) or direct-clear (C_D) inputs, the indicated state at either of these inputs over-rides all other inputs (including trigger) to set the outputs to the states shown in the input/output table.	Input / Output A, B, C[1], D[1] — X, $\bar{X}$ Conditions for triggered operation (output condition after trigger pulse) LO, LO, LO, LO — No change LO, HI, LO, LO — LO, HI HI, LO, LO, LO — HI, LO HI, HI, LO, LO — Changes state Conditions for direct-set, direct-clear operation Φ, Φ, LO, LO — No change Φ, Φ, LO, HI — LO, HI Φ, Φ, HI, LO — HI, LO Φ, Φ, HI, HI — Undefined Φ = Has no effect in this case [1] Applies only with direct inputs.

MAIN INTERFACE

General

Diagram 0 in the rear of the manual shows the plug-in interface and the interconnections between the plug-in compartments, circuit boards, etc. of this instrument.

LOGIC CIRCUIT

General

The Logic Circuit develops control signals for use in other circuits within this instrument. These output signals automatically determine the correct instrument operation in relation to the plug-ins installed and/or selected, plug-in control settings, and the 7503 control settings.

Block Diagram

A block diagram of the Logic Circuit is shown in Fig. 3-2. This diagram shows the source of the input control signals, the output signals produced by this stage, and the basic interconnections between blocks. The interconnections shown are intended only to indicate inter-relation between blocks; and do not indicate a direct connection, or that only a single connection is made between the given blocks. Details of the inter-relation between stages in this circuit are given in the circuit description which follows. A schematic of this circuit is shown on diagram 1 at the rear of this manual.

The operation of each of these stages is discussed relating the input signals and/or levels to the output, with consideration given to the various modes of operation that may affect the stage. A logic diagram is also provided for stages where applicable. These diagrams are not discussed in detail, but are provided to aid in relating the function performed by a given stage to standard logic techniques. It should be noted that these logic diagrams are not an exact representation of the circuit but are only a logic diagram of the function performed by the stage. An input/output table is given, where applicable, for use along with the circuit description and logic diagram. These input/output tables document the combination of input conditions which are of importance to perform the prescribed function of an individual stage.

Vertical Mode Control

The Vertical Mode Control stage is made up of gates CR124-CR125, CR126, and CR130-CR155-CR172 and buffer amplifier Q132-Q137. These components develop the Vertical Mode Command which is connected to the Main Interface circuit (vertical plug-in compartments and trigger selection circuitry) and the Vertical Interface circuit to indicate which vertical unit is to be displayed. When this output level is HI, the Right Vertical unit is displayed and when it is LO, the Left Vertical unit is displayed.

Logic. The VERTICAL MODE switch located on diagram 9 provides control levels to this stage. This switch provides a HI level on only one of four output lines to indicate the selected vertical mode; the remaining lines are LO. The fifth mode, LEFT, is indicated when all four output lines are LO. Operation of this stage in all positions of the VERTICAL MODE switch is as follows:

RIGHT:

When the VERTICAL MODE switch is set to RIGHT, a HI level is connected to the buffer amplifier through R126 and CR126. The other diodes connected to the buffer input (CR125-CR130) are reverse biased, as their anodes are LO. The output of the buffer is not inverted with respect to its input (see discussion of buffer); so the output level is HI, indicating that the Right Vertical unit is to be displayed.

CHOP:

The VERTICAL MODE siwtch in the CHOP position applies a HI level to the anodes of CR124-CR125 through R125. The Vertical Chop Signal from the Chop Counter stage is connected to the cathode of CR124 through R124, and when it is HI, will reverse bias CR124. The HI level applied to CR125 through R125 will forward bias CR125, putting a HI at the input to the buffer. The buffer couples the HI level input to the output, indicating that the Right Vertical unit is to be displayed. When the Vertical Chop Signal is LO, CR124 is forward biased. This places a LO at the junction of R125-CR125 and reverse biases CR125, putting a LO at the input to the buffer. The buffer output then is LO, indicating that the Left Vertical unit is to be displayed. Since the Vertical Chop Signal from the Chop Counter stage is switching between a HI level and a LO level, the output of the buffer (the Vertical Mode Command signal) will switch at the same rate.

ALT:

In this mode, the VERTICAL MODE switch applies a HI level to the anodes of three diodes through R130. CR130 is connected to the input of the buffer. A switching signal is applied to the cathode of either CR155 or CR172 while the other diode is reverse biased. (The switching signals applied to CR155-CR172 are from the Vertical Binary stage and the Alternate Buffer and Switch stage. The selection of the applied signal is determined by these and other stages in the Logic Circuit and is covered in the discussion of these stages.) When the level of the switching signal is HI, CR155 and CR172 are reverse biased, and the HI level applied to CR130 through R130 forward biases CR130. This applies the HI level to the input of the buffer, which couples it to the output. When the switching signal level to CR155 or CR172 is LO, the selected diode (CR155 or CR172) is forward biased, putting a LO at the junction of R130-CR130. This reverse biases CR130, putting a LO at the input of the buffer. The buffer couples the LO to the output. The output of the buffer, the Vertical Mode

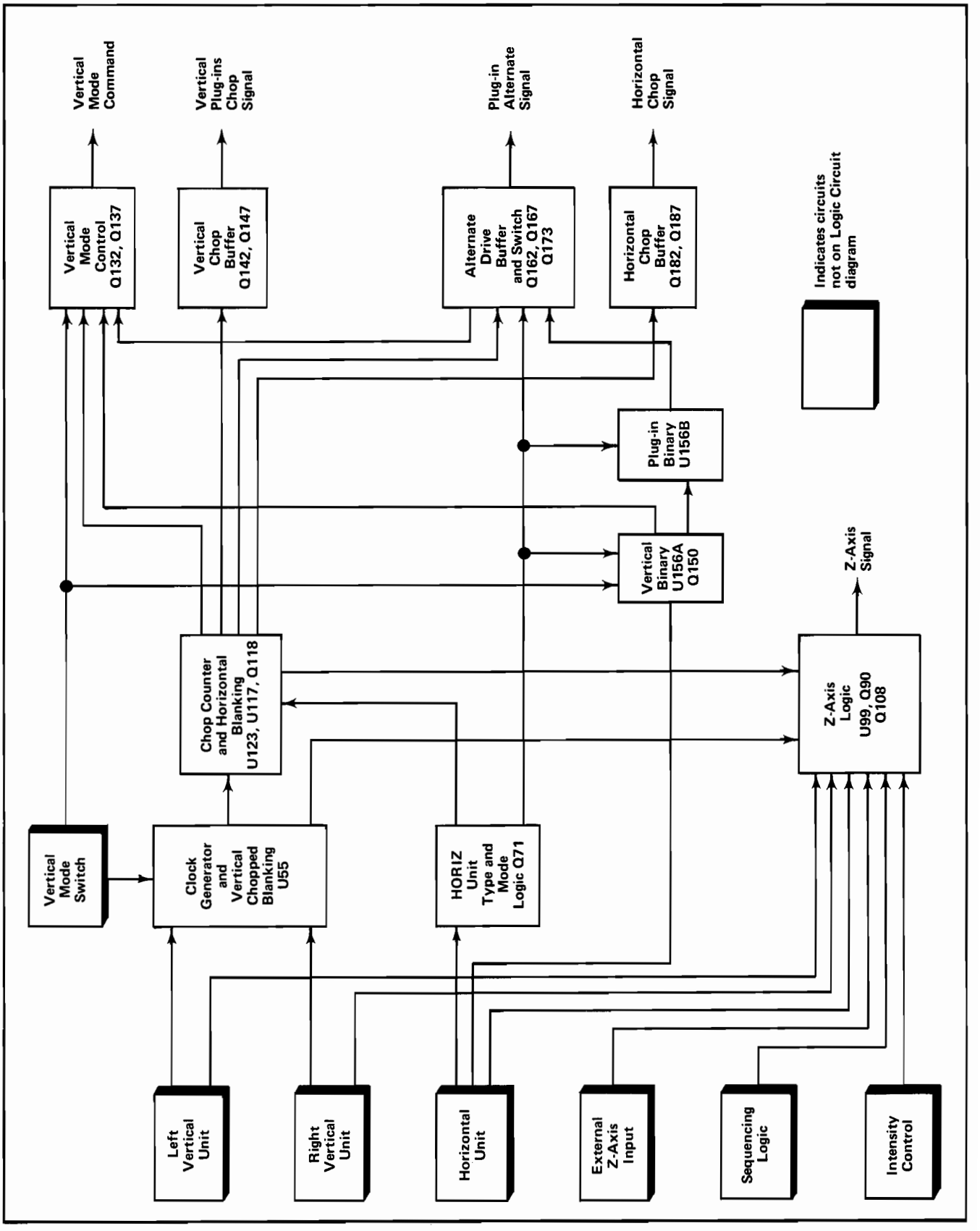


Fig. 3-2. Basic block diagram of the Logic Circuit.

Command signal, now switches between a HI and LO level at a rate determined by either the Vertical Binary stage or the Chop Counter stage.

ADD and LEFT:

The control levels from the VERTICAL MODE switch are not connected to the Vertical Mode Control stage when the VERTICAL MODE switch is set to ADD or LEFT. Since all the inputs to the buffer are LO, the Vertical Mode Command will be LO. This indicates that the Left Vertical unit is to be displayed. For more information on instrument operation in the ADD mode, see the discussion on the Vertical Interface circuit.

A logic diagram of the Vertical Mode Control stage is shown in Fig. 3-3. The discrete components which make up each logic function are identified. The gate connected to the input of the buffer is a phantom-OR gate. A phantom-OR gate performs the OR-logic function merely by interconnection of the two signals.

Buffer

The buffer consists of Q132 and Q137. The input to the buffer is the emitter of common-base connected Q132. This provides a low-impedance load for diode gates. The collector of the input transistor is connected to the output through emitter-follower Q137, providing isolation between the input to the buffer and the circuits driven by this stage. R136, R134, C135, and C136 are used to limit and standardize the risetime of the output signal.

A HI level at the input to this stage will cause current to flow into Q132, raising the collector to a HI. The emitter of Q137 will follow this level, providing a HI level at the output. A LO applied to the input will reverse bias Q132. No current will flow into Q132 and the collector will be LO. This is coupled to the output through Q137, putting a LO level at the output. So the level at the output of the buffer is shown to be in phase with the level applied to the input.

Clock Generator

One half of integrated circuit U55 along with the external components shown in Fig. 3-4A make up the Clock Generator stage. R1, Q1, Q2, and Q3 represent an equivalent circuit contained within U55A. This circuit along with discrete components C59, R56, R57, and R59 comprise a two-megahertz free-running oscillator to provide a timing signal (clock) for main frame vertical and plug-in chopping.

The stage operates as follows: Assume that Q2 is conducting and Q1 is off. The collector current of Q2 produces a voltage drop across R1 which holds Q1 off. This negative level at the collector of Q2 is also connected to pin 14 through Q3 (see waveforms in Fig. 3-4B at time T_0). Since there is no current through Q1, C59 begins to charge towards −15 volts through R56-R57. The emitter of Q1 goes negative as C59 charges, until it reaches a level about 0.6 volt more negative than the level at its base. When the emitter reaches this level, the base-emitter junction becomes forward-biased and Q1 saturates. This causes the emitter to rapidly rise positive (see time T_1 on waveforms).

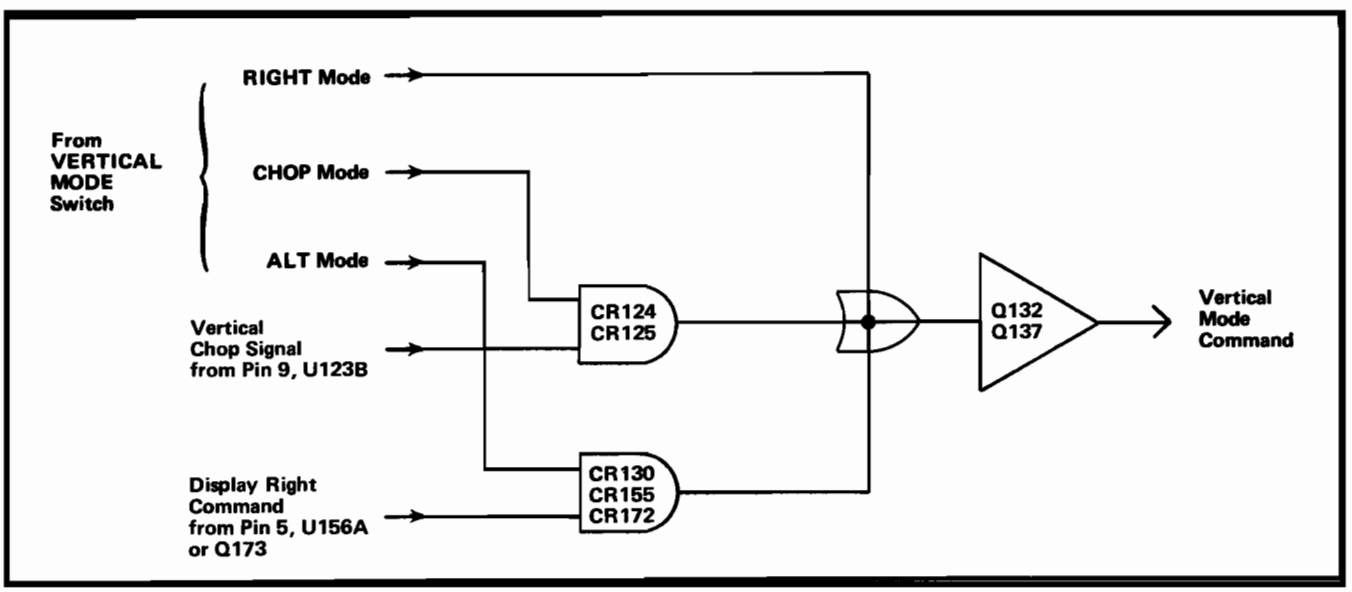


Fig. 3-3. Logic diagram of Vertical Mode Control stage.

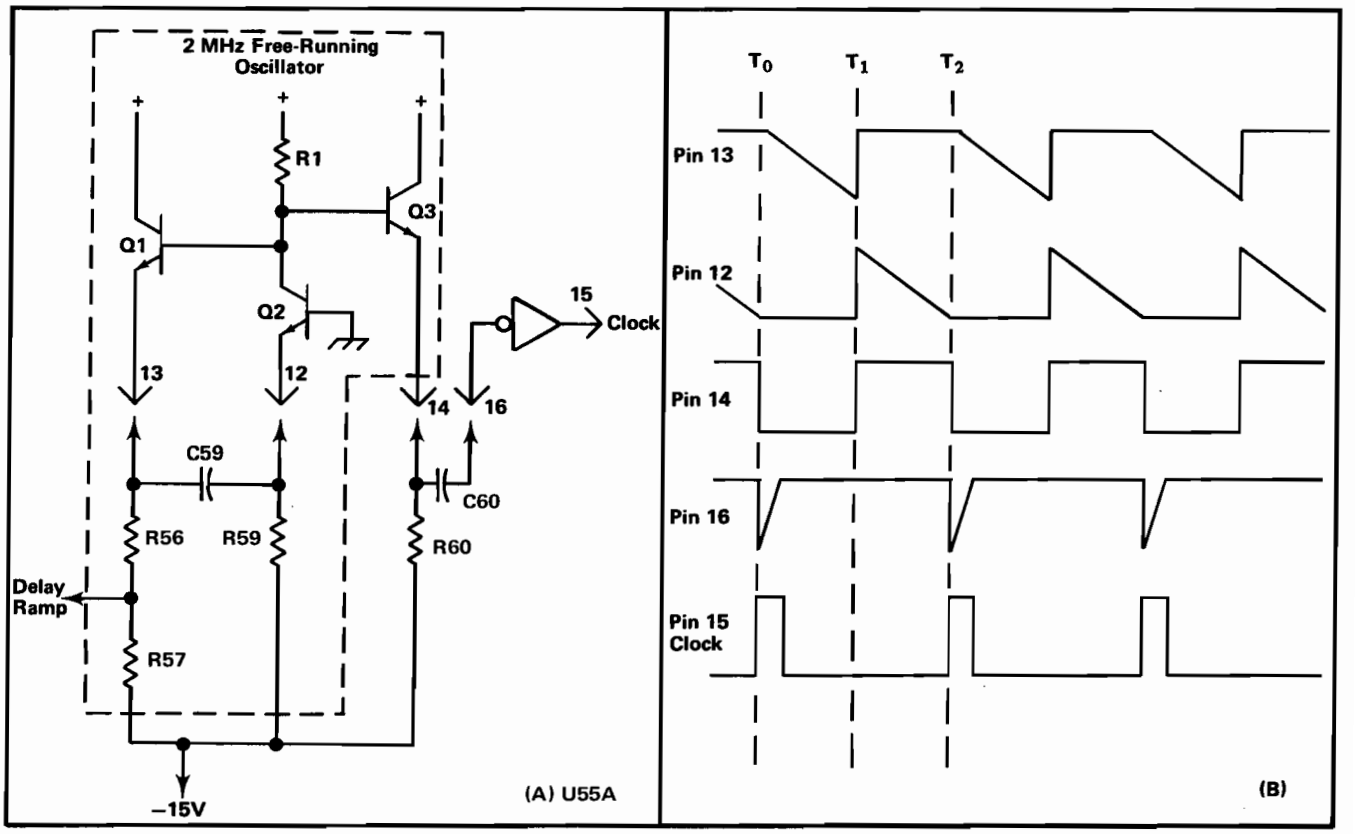


Fig. 3-4. (A) Diagram of Clock Generator stage, (B) Idealized waveforms for Clock Generator stage.

Since C59 cannot change its charge instantaneously, the sudden change in voltage at the emitter of Q1 pulls the emitter of Q2 positive also, to reverse-bias it. With Q2 reverse-biased, its collector rises positive to produce a positive output level at pin 14. This negative-going pulse is connected to pin 15 through an inverter-shaper which is also part of U55A. The output at pin 15 is a positive-going Clock pulse at a repetition rate of about two megahertz.

Now, conditions are reversed. Since Q2 is reverse biased, there is no current through it. Therefore, C59 can begin to discharge through R59. The emitter level of Q2 follows the discharge of C59 until it reaches a level about 0.6 volt more negative than its base. Then Q2 is forward biased and its collector drops negative to reverse-bias Q1. The level at pin 14 drops negative also, to complete the cycle. Once again, C59 begins to charge through R56-R57 to start the second cycle.

Two outputs are provided from this oscillator. The Delay Ramp signal from the junction of R56-R57 is connected to the Vertical Chopped Blanking stage. This signal has the same waveshape, as shown by the waveform at pin 13 with its slope determined by the divider ratio between R56-R57. A square-wave output is provided at pin 14. The frequency of this square wave is determined by the RC relationship between C59 and R1 ($F \approx \frac{1}{4R1C59}$). The duty cycle is determined by the ratio of R56-R57 to R59.

The square wave at pin 14 is connected to pin 16 through C60. C60, along with the internal resistance of U55A, differentiates the square wave at pin 14 to produce a negative-going pulse coincident with the falling edge of the square wave (positive-going pulse coincident with rising edge has no effect on circuit operation).

Vertical Chopped Blanking

The Vertical Chopped Blanking stage is made up of the remaining half of integrated circuit U55. This stage determines if Vertical Chopped Blanking pulses are required, based upon the operating mode of the vertical system or the plug-in units (dual-trace units only). Vertical Chopped Blanking pulses are produced if: (1.) VERTICAL MODE switch is set to CHOP; (2.) Dual-trace vertical unit is operating in the chopped mode, and that unit is being displayed; (3.) Dual-trace vertical unit is operating in the chopped mode with the VERTICAL MODE switch set to ADD. The repetition rate of the negative-going Vertical Chopped Blanking pulse output at pin 4 is always two megahertz, as determined by the Clock Generator stage.

The Delay Ramp signal from the Clock Generator stage determines the repetition rate and pulse width of the Vertical Chopped Blanking pulses. The Delay Ramp applied to pin 10 starts to go negative from a level of about +1.1 volts, coincident with the leading edge of the Clock pulse (see waveforms in Fig. 3-5B). This results in a HI quiescent condition for the Vertical Chopped Blanking pulse. The slope of the negative-going Delay Ramp is determined by the Clock Generator stage. As it reaches a level slightly negative from ground, the Vertical Chopped Blanking pulse output level changes to the LO state. This signal remains LO until the Delay Ramp goes HI again. Notice the delay between the leading edge of the Clock pulse generated by U55A and the leading edge of the Vertical Chopped Blanking pulses (see Fig. 3-5B). The amount of delay between the leading edges of these pulses is determined by the slope of the Delay Ramp applied to pin 10. This delay is necessary due to the delay line in the vertical deflection system. Otherwise, the trace blanking resulting from the Vertical Chopped Blanking pulse would not coincide with the switching between the displayed traces. The duty cycle of the square wave produced in the Clock Generator stage determines the pulse width of the Vertical Chopped Blanking pulses (see Clock Generator discussion for more information).

Whenever this instrument is turned on, Vertical Chopped Blanking pulses are being produced at a two-megahertz rate. However, these pulses are available as an output at pin 4 only when the remaining inputs to U55B are at the correct levels. The following discussions give the operating conditions which produce Vertical Chopped Blanking pulses to blank the CRT during vertical chopping. Fig. 3-5A identifies the function of the pins of U55B.

1. CHOP VERTICAL MODE

When the VERTICAL MODE switch is set to CHOP, Vertical Chopped Blanking pulses are available at pin 4 at all times. The input conditions necessary are:

Pin 3 HI—VERTICAL MODE switch set to CHOP.

Pin 7 LO—VERTICAL MODE switch set to any position except ADD.

Pin 10 LO—Delay Ramp more negative than about zero volts.

2. LEFT VERTICAL UNIT SET FOR CHOPPED MODE

If the Left Vertical unit is set for chopped operation, the setting of the VERTICAL MODE switch determines whether the Vertical Chopped Blanking pulses are available. If the VERTICAL MODE switch is set to the CHOP position, conditions are as described in #1 previously. Operation in the ADD position of the VERTICAL MODE switch is given later. For the LEFT position of the VERTICAL MODE switch, or when the Left Vertical unit is to be displayed in the ALT mode, Vertical Chopped Blanking pulses are available at all times (two-megahertz rate). The input conditions are:

Pin 3 LO—VERTICAL MODE switch set to any position except CHOP.

Pin 5 LO—Left Vertical unit set to chopped mode.

Pin 6 LO—Left Vertical unit to be displayed (Vertical Mode Command LO).

Pin 7 LO—VERTICAL MODE switch set to any position except ADD.

Pin 10 LO—Delay Ramp more negative than about zero volts.

Notice that the Vertical Mode Command at pin 6 must be LO for output pulses to be available at pin 4. This means that when the VERTICAL MODE switch is set to ALT, Vertical Chopped Blanking pulses will be produced only

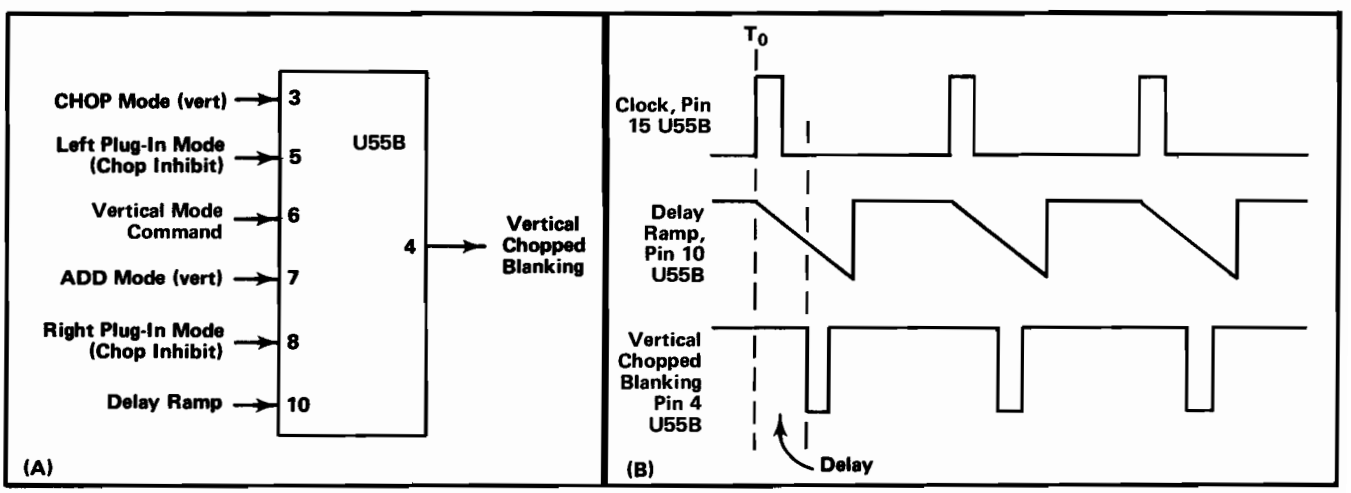


Fig. 3-5. (A) Input and output pins for Vertical Chopped Blanking stage, (B) Idealized waveform for Vertical Chopped Blanking stage.

during the time that the Left Vertical unit is to be displayed (unless Right Vertical unit is also set for chopped operation).

3. RIGHT VERTICAL UNIT SET FOR CHOPPED OPERATION

If the Right Vertical unit is set for chopped mode, operation is the same as described before for the Left Vertical unit except that Vertical Chopped Blanking pulses are produced when the VERTICAL MODE switch is set to RIGHT or when the Vertical Mode command is HI in the ALT mode. The input conditions are:

Pin 3 LO—VERTICAL MODE switch set to any position except CHOP.

Pin 6 HI—Right Vertical unit to be displayed (Vertical Mode Command HI).

Pin 7 LO—VERTICAL MODE switch set to any position except ADD.

Pin 8 LO—Right Vertical unit set to chopped mode.

Pin 10 LO—Delay Ramp more negative than about zero volts.

4. ADD VERTICAL MODE

When the VERTICAL MODE switch is in the ADD position and either or both of the vertical units are operating in the chopped mode, Vertical Chopped Blanking pulses must be available to block out the transition between the traces of the vertical units. The input conditions are:

Pin 3 LO—VERTICAL MODE switch set to any position except CHOP.

Pin 5 LO—Left Vertical unit set to chopped mode (can be HI if pin 8 is LO).

Pin 7 HI—VERTICAL MODE switch set to ADD.

Pin 8 LO—Right Vertical unit set to chopped mode (can be HI if pin 5 is LO).

Pin 10 LO—Delay Ramp more negative than about zero volts.

Fig. 3-6A shows a logic diagram of the Vertical Chopped Blanking stage. Notice the comparator block on this diagram (one input connected to pin 10). The output of this comparator is determined by the relationship between the levels at its inputs. If pin 10 is more positive (HI) than the grounded input, the output is HI also; if it is more negative (LO), the output is LO. An input/output table for this stage is given in Fig. 3-6B.

HORIZ Unit Type and Mode Logic

This stage of the Logic circuit supplies control levels to indicate the type and operating mode of the plug-in unit installed in the HORIZ compartment. The plug-in provides the inputs to this stage via the Main Interface circuit to pins EA and EF on the Logic board. The inputs are the X-Compensation Inhibit and Plug-In Mode respectively. The outputs are the Sweep Command and Horizontal Chop Blanking Command. A simplified schematic showing input and output points is given in Fig. 3-7A.

The Sweep Command Signal is connected to the Alternate Drive Buffer and Switch, Vertical Binary, and Plug-in Binary stages to indicate if a sweep is being used or not. See the discussion of these individual stages for more information.

The Sweep Command is derived directly from the X-Compensation Inhibit at pin EA. The level here is HI for sweep units and LO for non-sweep units (LO for sweep units operated in an amplifier mode).

The Horizontal Chop Blanking Command from the collector of Q71 is connected to the Chop Counter stage to alter the counting rate (see discussion of Chop Counter stage). The Horizontal Chop Blanking Command is derived from the level of the Plug-in Mode input at pin EF in conjunction with the Sweep Command. An input/output table for Q71 is shown in Fig. 3-7B. The plug-in Mode signal is supplied by dual-trace amplifier units and will be between approximately 0 and +5 volts. The modes and corresponding voltage levels are: CH 1, +5 V; CH 2, +4 V; ADD, +2 V; ALT, +1 V; CHOP, 0 V. A single-channel amplifier unit leaves the line open or treats it as CH 1. A HI level (single-channel) at pin EF will block current through CR67, and Q71 will be turned on. The collector of Q71 will be LO, indicating a single-channel unit. A LO level (below +1 V) at pin EF will turn CR67 on and Q71 off. The collector of Q71 will go HI, generating the Horizontal Chop Blanking Command.

Chop Counter

The Chop Counter stage produces the Vertical Chopping Signal, the Vertical Plug-in Chopping Signal, the Horizontal Plug-in Chopping Signal, and the Horizontal Chopped Blanking Signal. The Clock pulse produced by the Clock Generator stage provides the timing signal for this stage. The function of the input and output connections for the Chop Counter stage are identified in the logic diagram of the Chop Counter stage, Fig. 3-8.

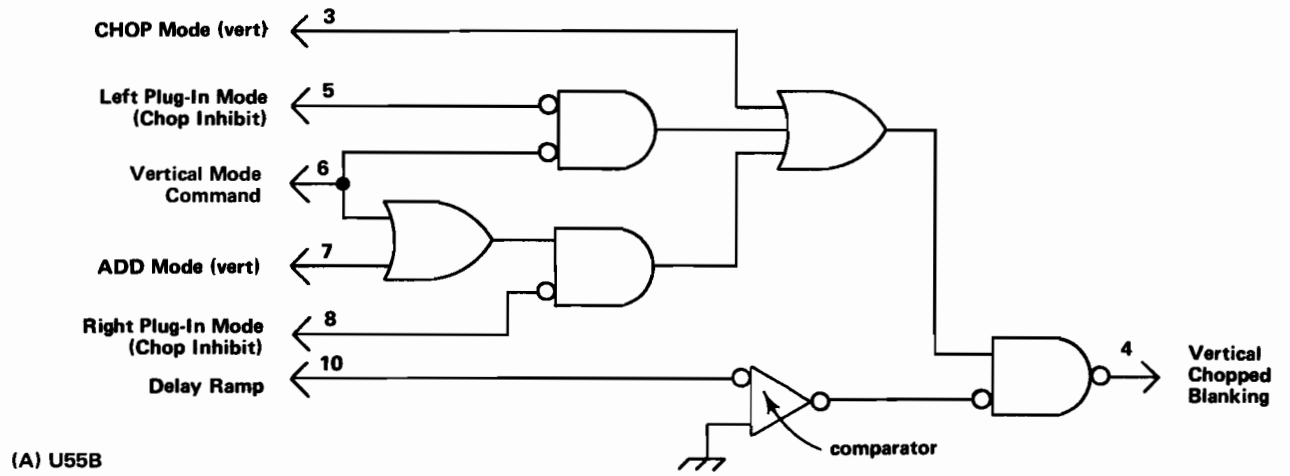
The Chop Counter stage is made up of two integrated circuits U117-U123, and transistor Q118. U117 and U123 each contain two D-type, triggered flip-flops with direct-set,

direct-clear inputs and complementary outputs. A D-type flip-flop, upon application of a positive-going trigger, will transfer to the 1 output the state at the D input prior to triggering. By connecting the D input to the 0 output, the 1 output will change states each time the flip-flop is triggered; thus, the device operates as a triggered flip-flop. U117A, U123A, and U123B are connected in this manner with U123A and U123B using the direct-set input also. U117B is operated as a D-type flip-flop with direct-clear input. Fig. 3-9A shows the input/output table for U117B. Fig. 3-9B shows the input/output table for U123A or U123B. For an input/output table for U117A, see Table 3-1, Basic Logic Reference. Q118 is used as an AND gate with three inputs inverted i.e., the output is HI when all three inputs are LO.

The repetition rate of the output signals from the Chop Counter stage is determined by the state of the Horizontal Chop Blanking Command input. The following discussions describe the operation of this stage for both states of the Horizontal Chop Blanking Command.

CONDITION 1

Horizontal Chop Blanking Command—LO



(A) U55B

(B)

Input						Output	
CHOP Mode (vert) 3	Left Plug-In Mode (Chop Inhibit) 5	Vertical Mode Command 6	Add Mode (vert) 7	Right Plug-In Mode (Chop Inhibit) 8	Delay Ramp 10[1]	Vertical Chopped Blanking 4[2]	Conditions
HI	Φ	Φ	LO	Φ	LO	LO	CHOP Mode (vert)
LO	LO	LO	LO	Φ	LO	LO	Left Plug-in Chopped
LO	Φ	HI	LO	LO	LO	LO	Right Plug-in Chopped
LO	LO[3]	Φ	HI	LO[3]	LO	LO	ADD Mode, Left or Right Plug-in Chopped
All other combinations						HI	No Vertical Chopped Blanking pulses at output.

Φ = Has no effect in this case.

[1] Ramp signal; considered LO when more negative than about zero volts.

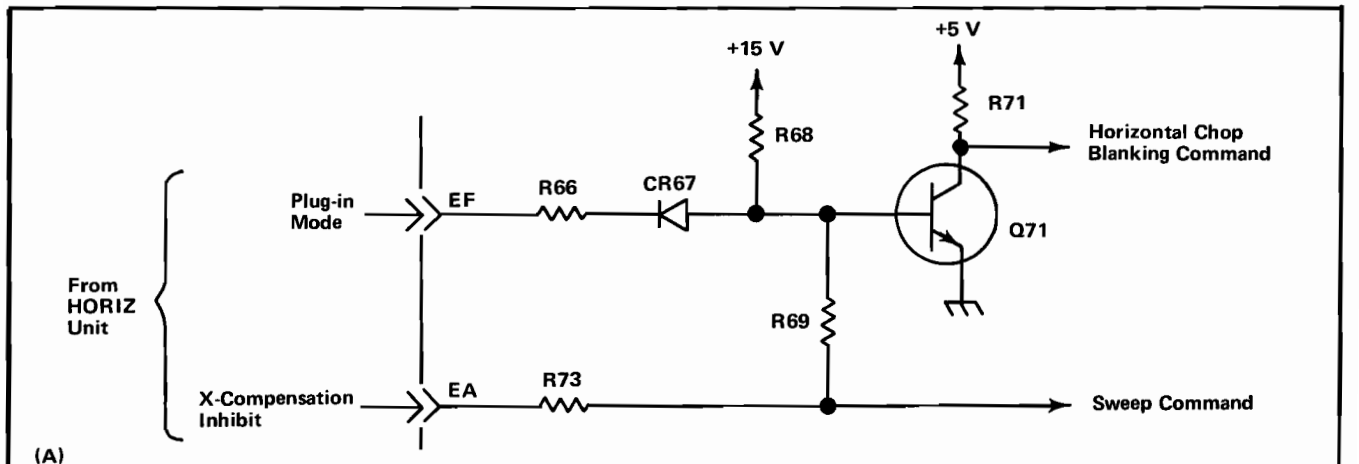
[2] Negative-going pulse at two megahertz rate.

[3] Pin 5 can be HI and not affect operation if pin 8 is LO, and vice versa.

Fig. 3-6. (A) Logic diagram for Vertical Chopped Blanking stage, (B) Table of input/output combinations for Vertical Chopped Blanking stage.

This is the normal operating level of the Horizontal Chop Blanking Command (for more information, see the discussion on the HORIZ Unit Type and Mode Logic stage).

The direct-clear input of U117B (pin 13) being forced LO by the Horizontal Chop Blanking Command over-rides the other inputs, and sets the level at pin 9 LO and at pin 8 HI (see Fig. 3-9A). The HI level from pin 8, U117B connected to the direct-set inputs of U123B and U123A (pins 10 and 4 respectively) enables them to operate as triggered flip-flops (or divide by two counters). Clock pulses at a 2 MHz rate from the Clock Generator stage are applied to the T input of U123B at pin 11. U123B will change states with each positive-going Clock pulse, and its output at pin 9 will be a square wave, switching between the HI and LO levels at a 1 MHz rate. This signal is connected to the Vertical Mode Control stage through R124 as the Vertical Chopping Signal. The square wave from pin 9, U123B is also connected to the T input of U123A. U123A will also change states with each positive-going pulse to generate a 500 kHz square wave at pin 5. The output at pin 5 is switching between HI and LO levels and is connected to the T input of U117A through R128 and to the Vertical Plug-in Chop Buffer stage through R140-CR140. U117A will count down from the 500 kHz square wave to generate a 250 kHz square wave at its output at pin 5. This square wave is connected to the Horizontal Plug-in Chop Buffer stage through R180-CR180,



(A)

Input			Output	
X-Compensation Inhibit	HORIZ Plug-in Mode	Horizontal Chop Blanking Command	Horizontal Unit	
EA	EF	Collector Q71	Mode	Type
HI	Φ	LO	Sweep	Time-Base Unit
LO	HI	LO	CH 1	Dual-Trace Amplifier Unit
LO	LO	HI	ALT	
LO	HI	LO	ADD	
LO	LO	HI	CHOP	
LO	HI	LO	CH 2	

Φ = Has no effect in this case

(B)

Fig. 3-7. (A) Simplified schematic diagram HORIZ Unit Type and Mode Logic stage, (B) Input/output table for Q71.

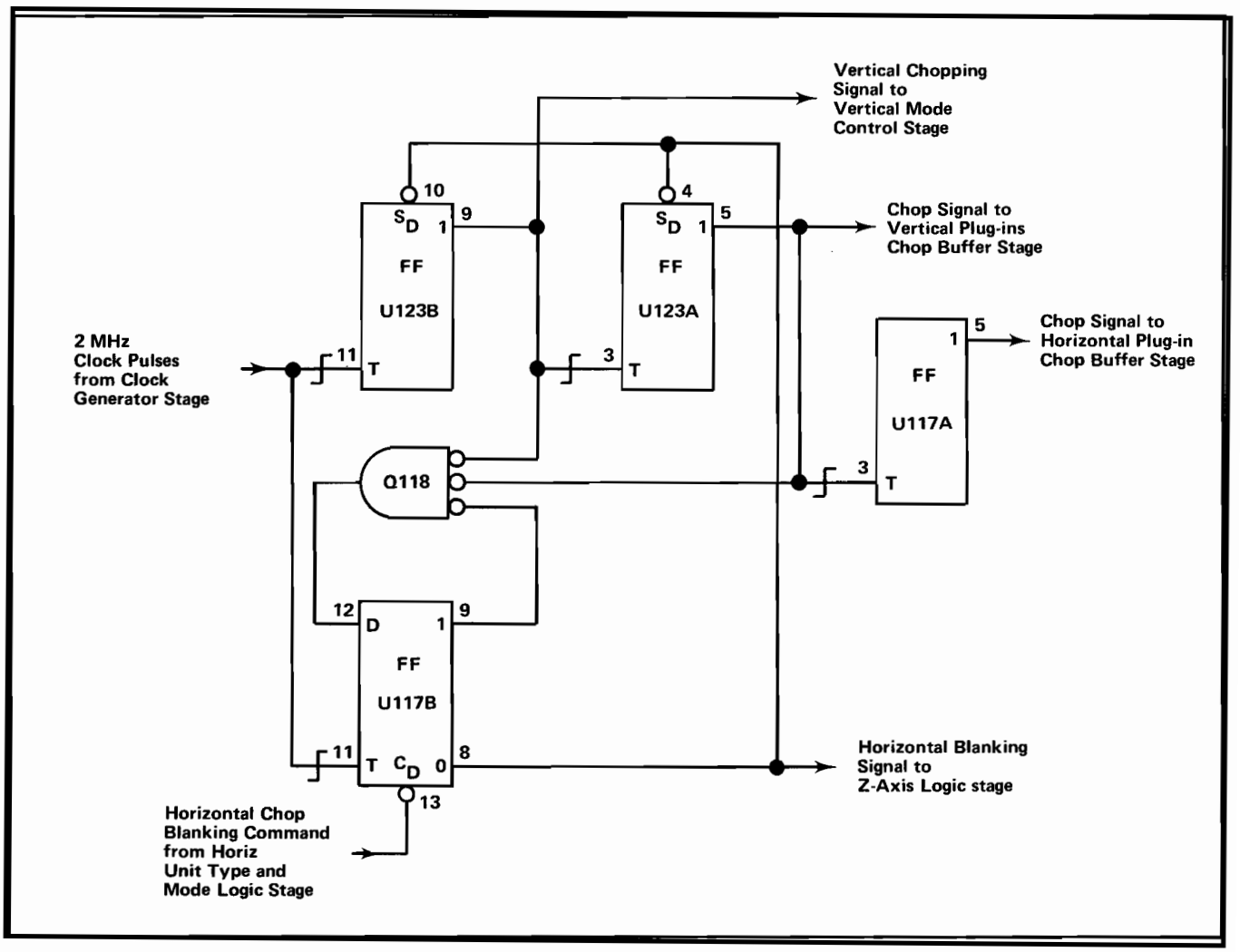


Fig. 3-8. Detailed logic diagram of Chop Counter stage.

and to the Alternate Buffer and Switch stage through R174. Idealized waveforms showing the timing relationship between the input and output signals for this stage when operating in condition 1 are shown in Fig. 3-10.

CONDITION 2

Horizontal Chop Blanking—HI

This is the state the Horizontal Chop Blanking Command will assume when a vertical unit in a dual-trace mode is operated in the HORIZ compartment.

In this condition, the direct-clear input of U117B (pin 13) is HI, which enables it to transfer the level at the D input (pin 12) to the 1 output (pin 9) upon the arrival of each Clock pulse at its T input (pin 11). The D input is connected to the collector of Q118, which is LO until all three inputs (counter outputs) to its base are LO. With the D input of U117B LO, the next Clock pulse will set the 1 output LO and the 0 output HI. This is the condition at time T_0 in Fig. 3-11. At this time, the HI level at the direct-set inputs to U123B and U123A from pin 8-U117B enables them to count down. At time T_1, the output of each counter is LO and the level at the collector of Q118 goes HI. This HI level is transferred to the 1 output of U117B (pin 9) upon the arrival of the next Clock pulse at time T_2. At this time, the 0 output of U117B (pin 8) goes LO, setting U123B and U123A 1 outputs to a HI level. The collector of Q118 drops to a LO level, since the inputs went HI. The Clock pulse arriving at time T_3 has no effect on the state of U123B since its direct-set input is LO, but it will trigger U117B to transfer the LO level at its D input to the 1 output. After the Clock pulse at time T_3 has triggered U117B to change states, U123B and U123A are enabled to count and conditions are the same as they were at time T_0. U117A has changed states on each positive-going change at its T input (pin 3) to produce the waveform shown in Fig. 3-11 for pin 5-U117A. This waveform is connected to the Horiz Unit Chop Buffer stage. The waveform at pin 8-U117B is connected to the Z-Axis Logic stage to blank the CRT during the horizontal unit switching time.

Input			Output		
	13	12	9	8	
Conditions for triggered operation (output condition after trigger pulse)					
	HI	LO	LO	HI	
	HI	HI	HI	LO	
Conditions for direct-clear operation					
	LO	Φ	LO	HI	

Φ Has no effect in this case

(A)

Input				Output		
	S_D	1	0	1	0	
Condition before trigger pulse				Condition after trigger pulse		
	HI	HI	LO	LO	HI	
	HI	LO	HI	HI	LO	
	LO	HI	LO	HI	LO	over-rides trigger

(B)

Fig. 3-9. (A) Input/output table for U117B, (B) Input/output table for U123A or U123B.

Vertical Plug-in Chop Buffer

This stage, consisting of Q142 and Q147, provides isolation between the Vertical Plug-in Chopping Signal from pin 5-U123A and the Vertical plug-in units. The Vertical Plug-in Chop Signal is a square wave which is switching between HI and LO levels at a rate determined by the inputs to the Chop Counter stage (see the discussion on the Chop Counter stage for more information). A dual-trace unit operating in the CHOP mode will display CH 2 when this signal level is HI, and CH 1 when the level is LO. The input to the buffer is the emitter of common-base connected Q142, which is connected to the Chop Counter output through R140-CR140. The collector of the input transistor is connected to the output through emitter-follower Q147. R146, R144, C145, and C146 are used to limit and standardize the risetime of the output signal.

When the level of the Vertical Plug-in Chop Signal from pin 5-U123A is HI, CR140 is reverse biased. The level at the emitter of Q142 will be HI through R141. Current will flow through R141 into Q142, raising its collector to a HI level. The emitter of Q147 will follow this level, providing a HI at the output. When the level at pin 5-U123A goes LO, CR140 will be forward biased, pulling the emitter of Q142 LO. No current will flow into Q142 and its collector will be LO. This LO is coupled through Q147 to make the output level LO. So the output of the buffer is shown to follow the level applied to the input.

HORIZ Plug-in Chop Buffer

This stage, consisting of Q182 and Q187, provides isolation between the output of the Chop Counter stage at pin 5-U117A and the HORIZ plug-in unit. The HORIZ Plug-in Chop Signal is a square wave which is switching

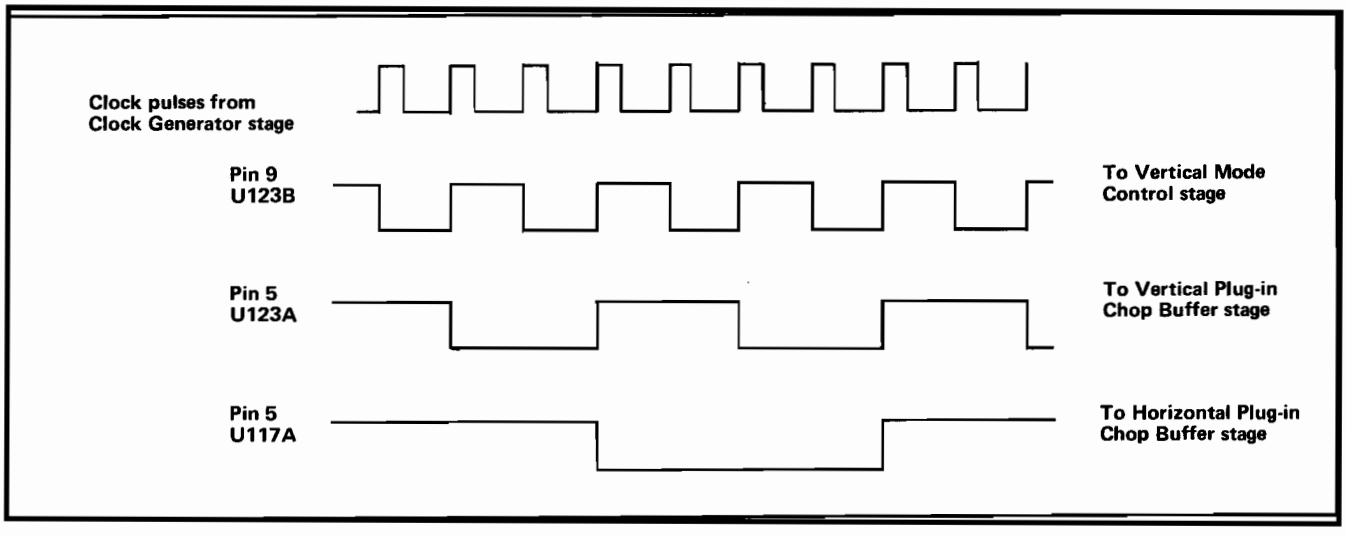


Fig. 3-10. Idealized input and output waveforms of Chop Counter stage when operating in condition 1.

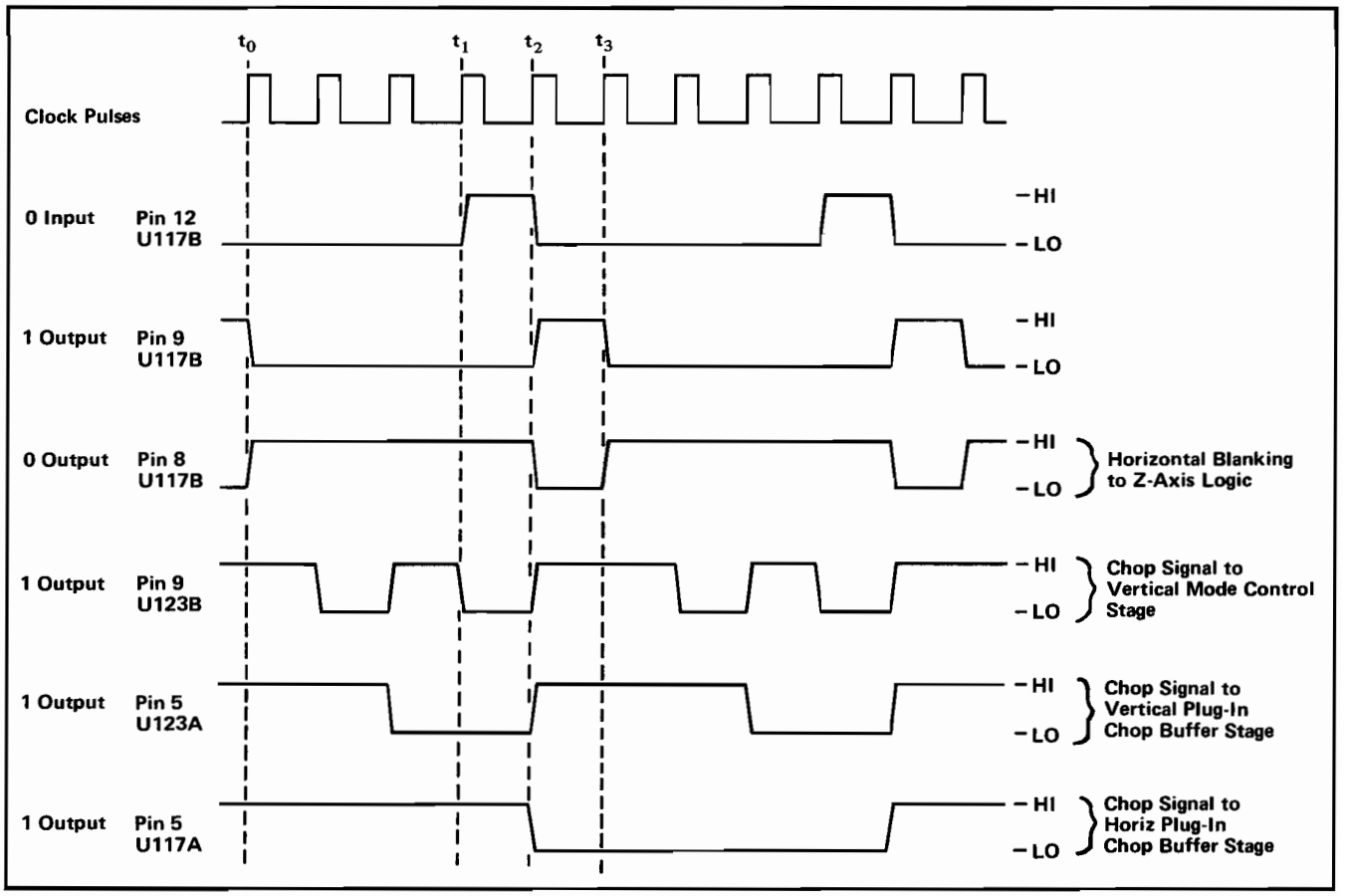


Fig. 3-11. Idealized input and output waveforms of Chop Counter stage when operating in condition 2.

between HI and LO levels at a rate determined by the inputs to the Chop Counter stage (see the discussion on the Chop Counter stage for more information). A dual-trace unit operating in the CHOP mode will display CH 2 when this signal level is HI, and CH 1 when the level is LO. The output of the Chop Counter stage at pin 5-U117A is connected to this stage through R180-CR180 to the emitter of Q182. The circuit and operation of this stage is identical to the Vertical Plug-in Chop Buffer stage. For more information, see the discussion on the Vertical Plug-in Chop Buffer stage.

Vertical Binary, Plug-in Binary, Alternate Drive Buffer and Switch

These three stages are closely related in their function of producing alternate switching signals to drive other circuits in the instrument. The operation of each individual stage is, therefore, more easily understood by first discussing their function and general operation as a unit in relation to the modes of operation that can occur.

CONDITION 1

VERTICAL MODE Switch—ALT.

HORIZ Unit—Time-base unit operating in a sweep mode.

This operating condition requires a signal from the Vertical Binary stage through R155 to the Vertical Mode Control stage, to switch the vertical display between the two vertical units at the completion of each sweep. The Display Right Command signal is a square wave which is switching between HI and LO levels at a rate determined by the sweep rate. To do this, the Vertical Binary stage operates as a divide by two counter triggered by the Holdoff pulse from the time-base unit. The Display Right Command signal is also used to trigger the Plug-in Binary stage which counts down by two to produce a switching waveform at one-fourth the sweep rate. This signal is available to the plug-in units through the Buffer Amplifier and Switch stage for switching between channels at a rate which is one-half the switching rate between vertical units. The Plug-in Alternate Drive signal is also a square wave which is switching between HI and LO levels. A dual-trace unit operated in the alternate mode will display CH 2 when this level is HI, and

CH 1 when the level is LO. The output waveforms of the Vertical Binary stage and the Plug-in Binary stage for Condition 1 are shown in relation to the sweep sawtooth and Holdoff waveforms in Fig. 3-12.

CONDITION 2

VERTICAL MODE Switch—Set to any position but ALT

HORIZ Unit—Time-base unit operating in a sweep mode

This condition requires a signal from the Plug-in Binary stage to the plug-ins for channel switching at a sweep rate. This is accomplished by the ALT Command from the VERTICAL MODE switch going to a LO level to change the function of the Vertical Binary stage. Now, the output of the Vertical Binary stage is a regeneration of the Holdoff waveform. This output is then divided by two by the Plug-in Binary stage to provide a waveform switching at one-half the sweep rate and available to the plug-ins for channel switching. The output of the Plug-in Binary stage now has the same relation to the sweep as the Vertical Binary stage output had in Condition 1.

CONDITION 3

VERTICAL MODE Switch—Any position

HORIZ Unit—Amplifier unit or a sweep unit operated in a non-sweep mode.

In this condition, there is no holdoff waveform from which to derive alternate switching pulses for either the Vertical Mode Control stage or for the plug-in units. The Sweep Command Signal from the HORIZ Unit Type and Mode Logic stage is LO when the unit installed in the HORIZ compartment is an amplifier unit, or a time-base unit operating in an amplifier mode. This turns on the Switch section of the Alternate Drive Buffer and Switch stage to connect chopping pulses from the Chop Counter stage to the plug-ins via the buffer. These chopping pulses are also connected to the Vertical Mode Control stage through CR172 when the VERTICAL MODE switch is in the ALT position.

Vertical Binary

The Vertical Binary stage consists of integrated circuit U156A and transistor Q150. U156A is a D-type flip-flop connected as a triggered flip-flop with direct-set and direct-clear inputs. An input/output table for U156A is shown in Fig. 3-13. The Sweep Command signal is connected to the direct-set input (pin 4) of U156A through CR157 to inhibit the flip-flop operation when the plug-in in the HORIZ compartment is not a time-base unit, or is a time-base unit operated in an amplifier mode. The ALT Command from the VERTICAL MODE switch is connected to the emitter of Q150 through R152. When the VERTICAL MODE switch is in a position other than ALT, the Vertical Binary stage is changed from a divide by two counter to a Holdoff regenerator. The operation of this stage for each of the

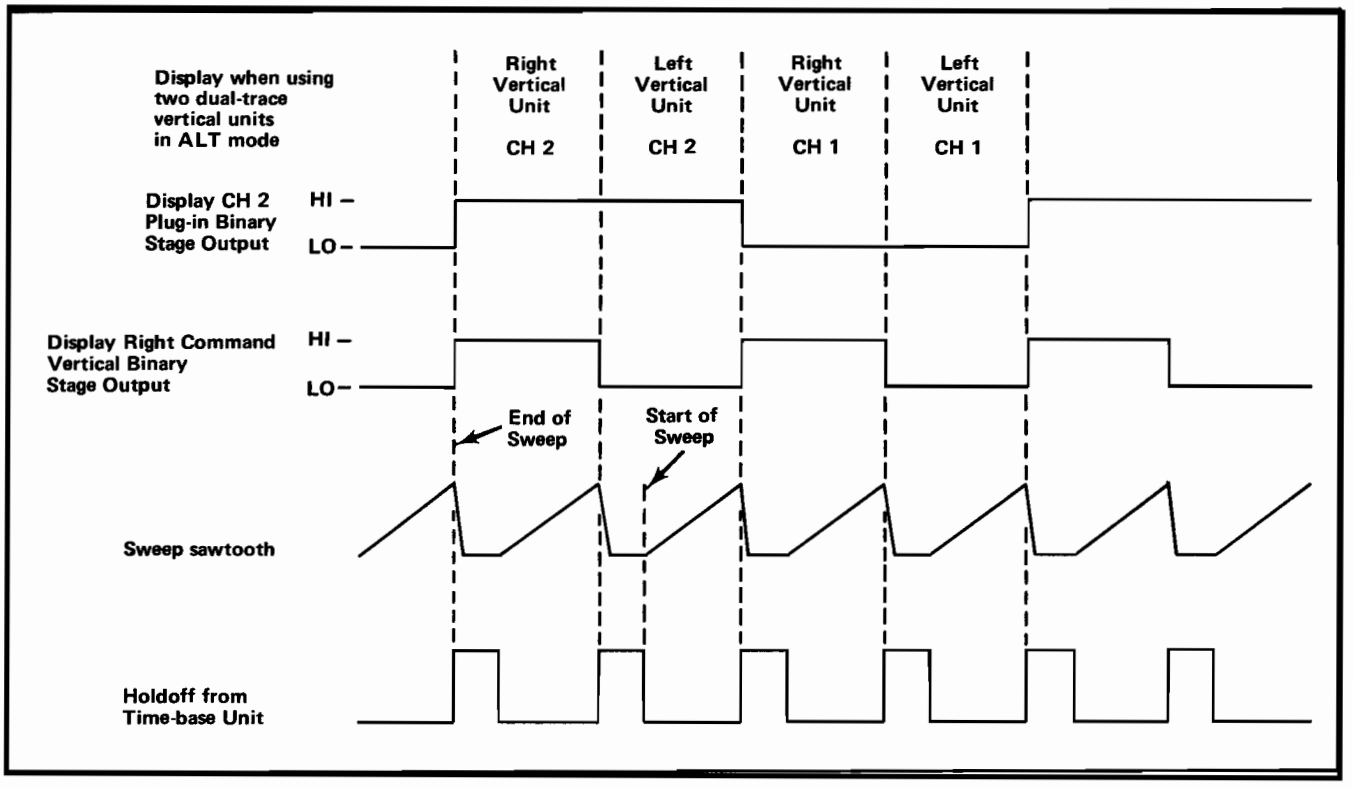


Fig. 3-12. Idealized waveforms showing relationship between sweep sawtooth and output of Vertical Binary and Plug-in Binary stages when operating in condition 1.

Input				Output		
S_D	C_D	1	0	1	0	
Condition before trigger pulse				Condition after trigger pulse		
HI	HI	HI	LO	LO	HI	
HI	HI	LO	HI	HI	LO	
LO	HI	HI	LO	HI	LO	Over-rides trigger
HI	LO	LO	HI	LO	HI	Over-rides trigger
LO	LO	Not allowed				

Fig. 3-13. Input/output table for U156A.

conditions mentioned in the general discussion is as follows:

CONDITION 1

Input levels:

ALT Command—HI
Sweep Command—HI

Holdoff—A pulse which changes from a LO level to a HI level at the end of each sweep.

The HI level from the ALT Command to the emitter of Q150 reverse-biases Q150 to keep its collector at a HI level. This HI level is applied to the direct-clear input of U156A at pin 1. The direct-set input (pin 4) of U156A is also at a HI level as a result of the Sweep Command being applied through CR157. The direct-set and direct-clear inputs being HI enables U156A to operate as a triggered flip-flop. U156A is triggered each time the level of the Holdoff connected to the trigger input (pin 3) through R159 goes HI. Thus, U156A is operating as a divide by two counter, generating a square wave which is switching between a HI and LO level at one-half the rate set by the time-base unit (see Fig. 3-12, which shows the time relationship between the Holdoff pulse and the output of the Vertical Binary stage). The output from pin 5-U156A is connected to CR155 in the Vertical Mode Control stage through R155 and to the plug-in Binary stage at pin 11-U156B.

CONDITION 2

Input levels:

ALT Command—LO
Sweep Command—HI

Holdoff—A pulse which changes from a LO level to a HI level at the completion of each sweep.

The HI level from the Sweep Command reverse-biases CR157, putting a HI level at the direct-set input (pin 4) of U156A. The emitter of Q150 is LO as a result of the ALT Command being LO, so Q150 can conduct whenever its base is HI. The base of Q150 is connected to pin 5 of U156A; and when the 1 output goes HI, Q150 will begin to conduct. In a time determined by the value of R154 and the capacitance between the collector and base of Q150, the collector will drop from its HI level to put a LO at the direct-clear input (pin 1) of U156A. This sets the 1 output (pin 5) to a LO level and turns Q150 off. The collector of Q150 is now HI once again, removing the LO from the direct-clear input of U156A and enabling the flip-flop. Now, upon the arrival of the next positive-going holdoff pulse at the trigger input, pin 5 of U156A will go hi to complete the cycle. The output of the Vertical Binary stage is now a pulse which switches from a LO level to a HI level and back at a rate determined by the time-base unit. This output is connected to the Plug-in Binary stage as a trigger input.

CONDITION 3

Input levels:

ALT Command—Has no effect in this case

Sweep Command—LO

Holdoff—LO

The LO from the Sweep Command forward biases CR157 to put a LO at the direct-set input (pin 4) of U156A. This inhibits the trigger and D inputs and sets the 1 output (pin 5) HI, thus disabling the Vertical Binary stage.

Plug-in Binary

The Plug-in Binary stage consists of U156B, connected as a triggered flip-flop. The output of the Vertical Binary stage is connected to the trigger input (pin 11) of U156B. Each time the level at the trigger input goes positive, the 1 output (pin 9) changes states. Thus, U156B has an output that is switching between HI and LO levels at a rate equal to one-half that of the Vertical Binary stage, or is a divide by two counter. The output of this stage is connected to the Alternate Drive Buffer and Switch stage through R160-CR160. The operation of the Plug-in Binary stage is the same for both Condition 1 and Condition 2. For Condition 3, the LO from the Sweep Command forward biases CR157, putting a LO on the direct-set input (pin 10) of U156B. This inhibits the trigger and D inputs and sets the 1 output (pin 9) to a HI level, thus disabling U156B.

Alternate Drive Buffer and Switch

This stage is made up of buffer Q162-Q167 and transistor Q173, which acts as a switch. The buffer provides isolation between the input signal and the circuits driven by

its output. The buffer circuitry is identical to the buffer in the Vertical Plug-in Chop Buffer stage. For more information on the operation of the buffer, see the discussion on the Vertical Plug-in Chop Buffer stage. The output of the buffer is connected to all three plug-in compartments via the Main Interface Circuit. The output level of the buffer is either HI or LO depending on the level of the input. The effect of the output level on a dual-trace plug-in is shown in Fig. 3-12.

The switch section of this stage is controlled by the Sweep Command through R170 to the base of Q173. When the Sweep Command level is HI (for conditions 1 and 2 as mentioned previously); Q173, CR173, and CR172 are reverse biased. The input to the buffer is from pin 9-U156B through R160 and CR160. In Condition 3, as previously noted, pin 9-U156B is HI (see Plug-in Binary stage discussion) and the Sweep Command is LO, CR160 is reverse biased by the HI level applied through R160. The base of Q173 is at a LO level from the Sweep Command, so Q173 is forward biased, as is CR173. The level at the emitter of Q173 and the input to the buffer is now determined by the level at the collector of Q173, which is connected to pin 5-U117A through R174. Now the output of the buffer will follow the output at pin 5-U117A, which is the Horizontal Plug-in Chopping Signal. When the VERTICAL MODE switch is set to ALT, CR172 becomes forward biased to pass the Horizontal Plug-in Chopping Signal to the Vertical Mode Control Stage.

Z-Axis Logic

The Z-Axis Logic stage produces an output current which sets the intensity of the display on the CRT. The level of this output current is determined by the setting of the front-panel INTENSITY control, or by an external signal. The Vertical Chopped Blanking, Horizontal Chopped Blanking, and Readout Blanking are applied to this stage to limit the output current and blank the CRT display for vertical chopping, horizontal chopping, or during a readout display. The Intensity Limit input provides protection for the CRT phosphor at slow sweep rates.

The Z-Axis Logic stage consists of transistor Q108, dual-transistor Q90, and integrated circuit U99, which is a five-transistor array. The individual transistors of U99 are identified in Fig. 3-14. A simplified schematic diagram of the Z-Axis Logic stage is shown in Fig. 3-15.

The output transistor for this stage is common-base connected Q3-U99 whose collector load is the input of the Z-Axis Amplifier in the CRT Circuit. The inputs previously mentioned limit and/or block the current through Q3-U99 by controlling current-limiter Q4 and Q5 of U99. The current limiter also controls the current from the external inputs and the current from the INTENSITY control through CR113. The operation of this stage is as follows: The output current, shown as I_1 in Fig. 3-15, must flow into the collector of Q4-U99 at pin 11. The current into the collector of Q4-U99 through CR113, I_2, is established by the divider R92-R93 and is quiescently maximum. The maximum amount of I_t into the collector of Q4-U99 is determined by the current I_1 into R110 from the +15-Volt Supply through network R75-R76-R77, R62-CR62, and R109-R108 which is maximum when the blanking and limiting inputs are HI. The Maximum Intensity adjustment R75 is set to provide optimum writing rate on the CRT when the INTENSITY control is set fully clockwise. When the Sweep Gate input goes HI, the current set by the

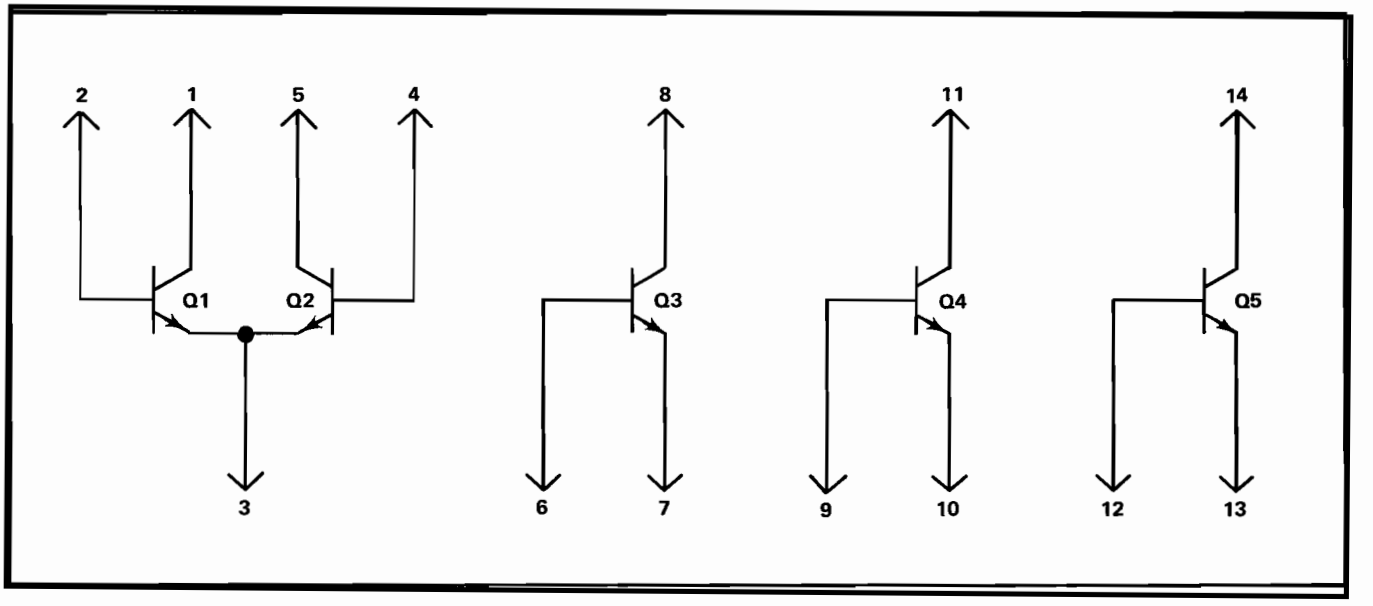


Fig. 3-14. Schematic diagram of five-transistor array identifying pins of individual transistors.

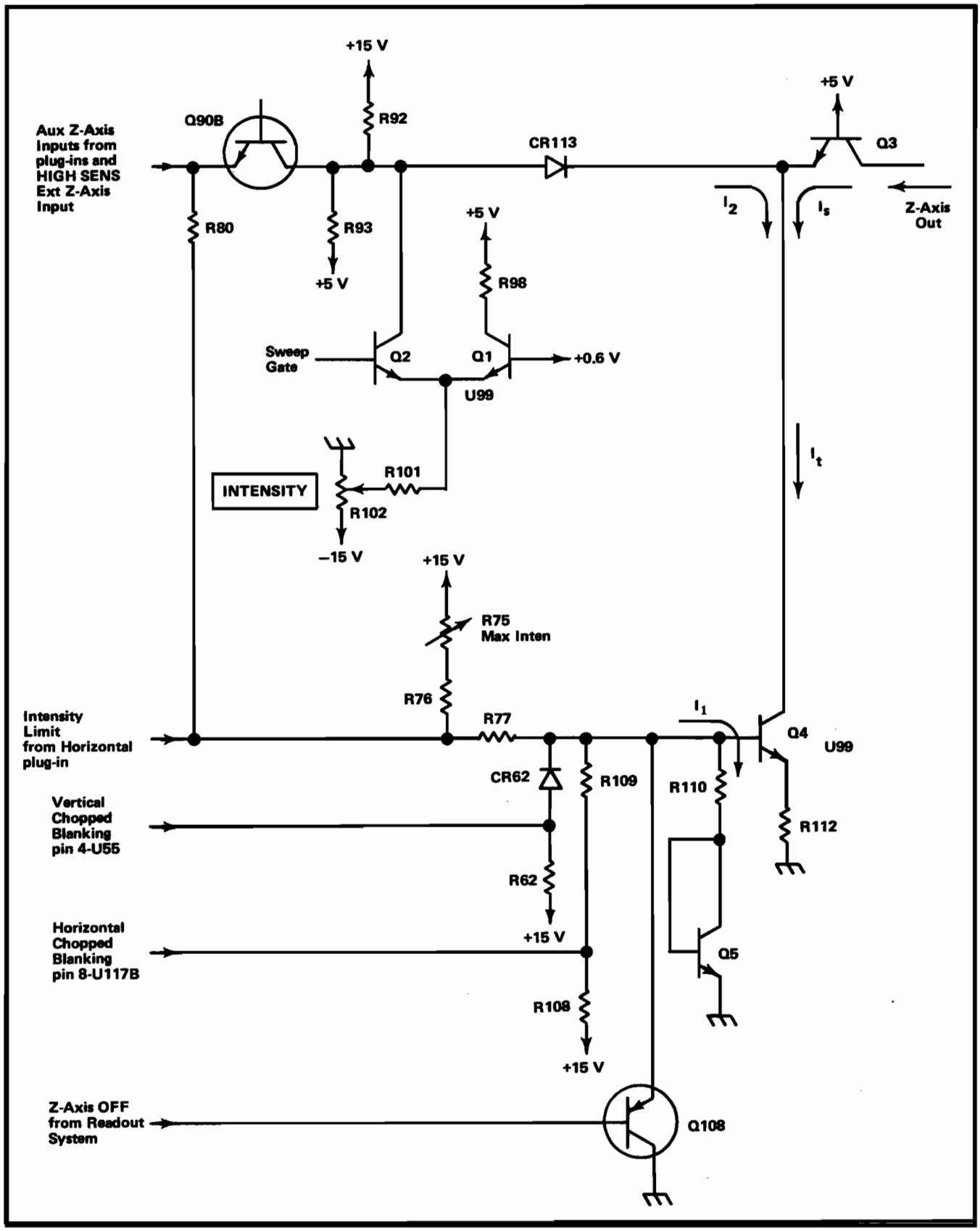


Fig. 3-15. Simplified schematic diagram of Z-Axis Logic stage.

INTENSITY control flows into the collector of Q2-U99 and is subtracted from the current I_2. Since I_t into Q4-U99 is set by I_1 into R110, I_s must increase by the same amount as the decrease in I_2, which results in an increased output current to the Z-Axis Amplifier. The Aux Z-Axis inputs from plug-ins and the HI SENS Ext Z-Axis input are connected to the emitter of Q90B to modulate I_2.

Since I_s plus I_2 is equal to I_t, if I_t is decreased or dropped to zero, the output I_s must also decrease or fall to zero. During Vertical Chopped Blanking, the level at pin 4-U55 goes LO. The current through R62-CR62 is blocked from flowing into R110 during that time, reducing I_1 (and I_t) by that amount, which is approximately 1.5 mA. During horizontal chopped blanking, the level at pin 8-U117B goes LO and the current through R108 is blocked, reducing I_1 by approximately 4.5 mA. When readout information is to be displayed on the CRT, the Z-Axis Logic OFF Command signal from the Readout System goes LO. This forward biases Q108, and it saturates, shunting I_1 through Q108 to ground. This reduces the output current to zero during the readout time.

The Intensity Limit function limits the output current of this stage, which in turn limits the maximum trace intensity for all CRT displays whenever the time-base unit is set to a sweep rate that requires intensity limiting. For conditions that do not require limiting, approximately 1.5 mA is supplied to I_1 by R75-R76-R77. When the time-base unit is set to a sweep rate which requires intensity limiting, pin EV is connected to ground through the time-base unit. This reduces I_1 by approximately 1.5 mA. However, the emitter of Q90 is also connected to pin EV through R80. When pin EV is grounded, I_2 is also decreased by approximately the same amount as I_1. So, while I_t was reduced, I_2 was reduced leaving I_s about the same. The intensity limit function then does not change the absolute value of the intensity below the limited value, but limits the maximum setting.

TRIGGER SELECTOR

General

The Trigger Selector circuit determines the trigger signal which is connected to the Time Base unit as controlled by the TRIGGER SOURCE switch. This circuit also provides the drive signal for the Vertical Signal Amplifier circuit. Fig. 3-16 shows a detailed block diagram of the Trigger Selector circuit, along with a simplified diagram of all the circuitry involved in the selection of the trigger source. A schematic of the Trigger Selector circuit is shown on diagram 3 at the rear of this manual. Also see diagrams 0 and 9 for the trigger selection circuitry not shown on diagram 3.

Trigger Mode and ADD Signals

General. The circuitry shown on the left side of the simplified diagram in Fig. 3-16 determines the operation of the Trigger Channel Switch stage. TRIGGER SOURCE switch S1011 controls the Trigger Channel Switch U324 through Q314. When the TRIGGER SOURCE switch is set to the VERT MODE position, the setting of the VERTICAL MODE switch determines the trigger selection. In the LEFT VERT or RIGHT VERT positions, the trigger signal is obtained from the indicated vertical unit. The following discussions give detailed operation in each position of the TRIGGER SOURCE switch.

VERT MODE. In the VERT MODE position of the TRIGGER SOURCE switch, the setting of the VERTICAL MODE switch determines the operation of the Trigger Channel Switch stage. In the LEFT position of the VERTICAL MODE switch, the base of Q314 is connected to ground through the ALT and RIGHT sections of S1021, CR1021 and CR1026 and S1011. This holds Q314 reverse biased to provide a LO level to pin 4 of U324 (see Fig. 3-17).

When the VERTICAL MODE switch is set to ALT, +5 volts is applied to the base of Q314 through CR1021 and S1011. Q314 is forward biased and its emitter level is determined by the Vertical Mode Command signal from the Logic Circuit applied to the collector. This signal switches between the HI level (Right Vertical unit to be displayed) and the LO level (Left Vertical unit to be displayed) at the end of each sweep. When the Vertical Mode Command is HI, it provides a positive collector voltage to Q314. Q314 is saturated due to CR1021, and its emitter level is very near the collector level. This provides a HI output level to the Trigger Channel Switch stage. As the Vertical Mode Command goes LO, the collector supply for Q314 also goes negative. Q314 remains saturated and the output again follows the collector level to supply a LO output level to U324.

For ADD and CHOP vertical mode operation, +5 volts is connected to pin 14 of U324 through CR1023 or CR1024 and S1011. At the same time, the base of Q314 is held LO by the ground connection through the ALT and RIGHT sections of S1021 so the level at pin 4 of U324 is LO also (produces an ADD mode in Trigger Channel Switch; see description of this circuit which follows). In the RIGHT position of the VERTICAL MODE switch, +5 volts is connected to the base of Q314 through CR1026 and S1011 to forward-bias the transistor. The Vertical Mode Command signal connected to the collector of Q314 is also HI in this mode and a HI output level is produced at the emitter of Q314.

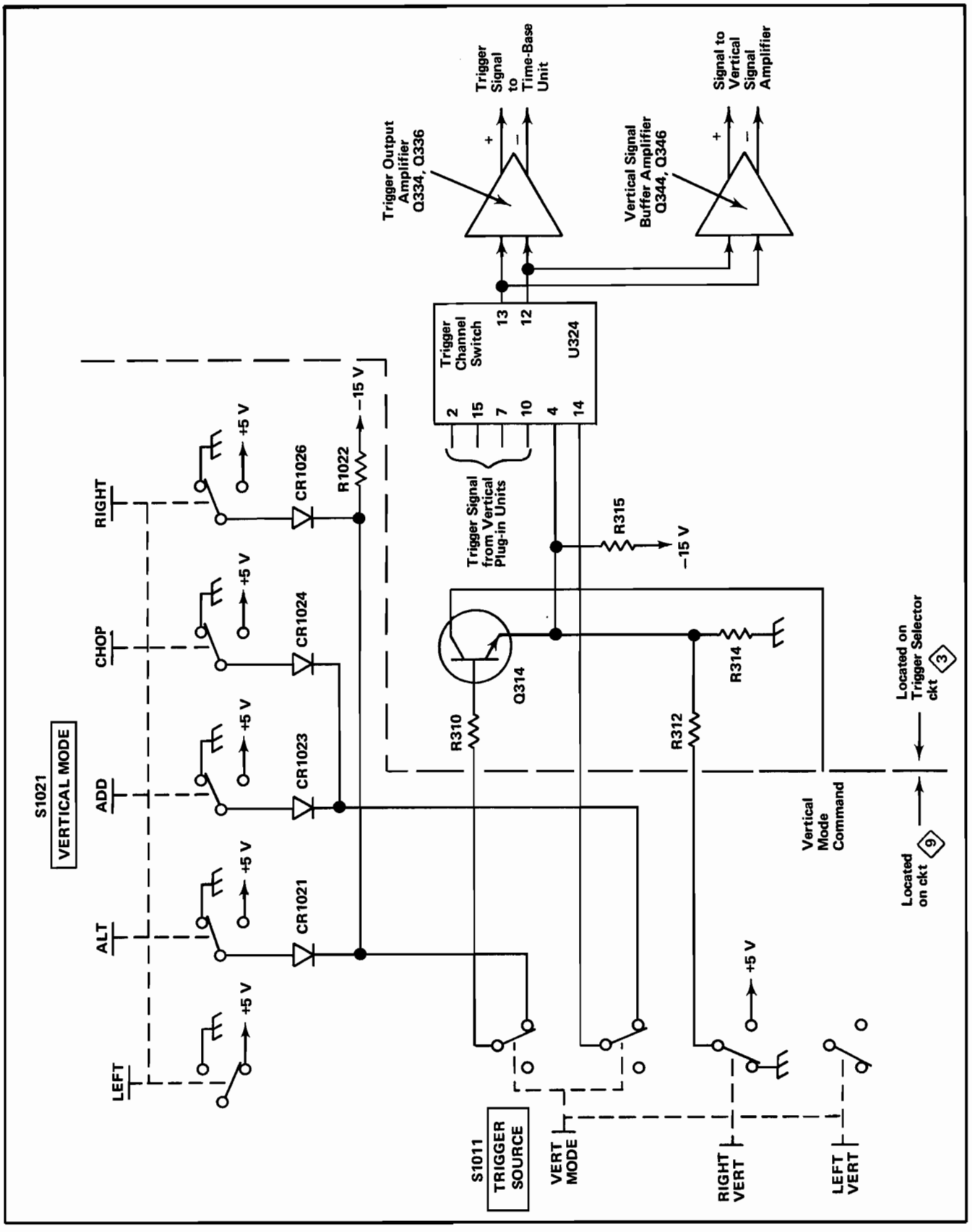


Fig. 3-16. Detailed block diagram of Trigger Selector circuit along with simplified schematic diagram of trigger source selection circuitry.

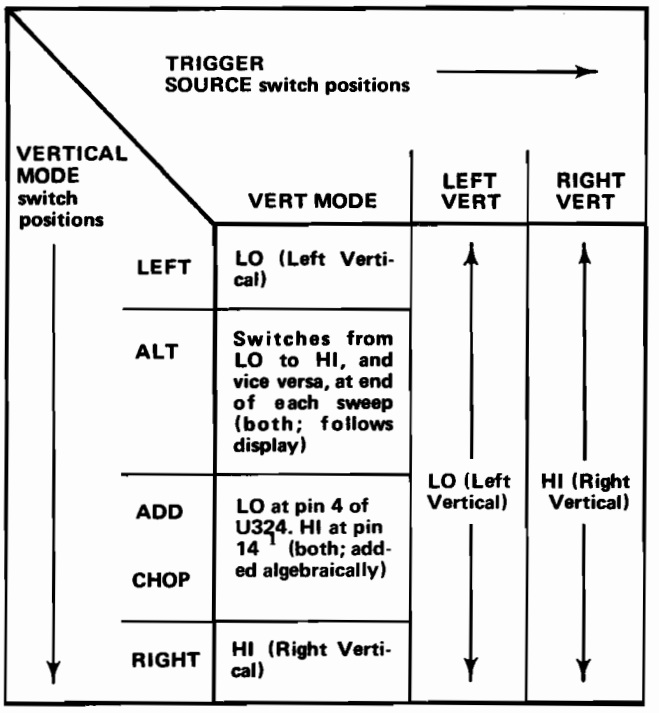


Fig. 3-17. Input levels at pin 4 of U324 (source of triggering signal is shown in parenthesis).

LEFT VERT. When the LEFT VERT trigger source is selected, the VERTICAL MODE switch is disconnected from the trigger selector circuitry. Now, the ground connection through the RIGHT VERT section of S1011 establishes a LO output level at the emitter of Q314.

RIGHT VERT. In the RIGHT VERT position of the TRIGGER SOURCE switch, +5 volts is connected to the emitter of Q314 through S1011 and R312. This produces a HI output level to the Trigger Channel Switch stage.

Trigger Channel Switch

The Trigger Channel Switch stage determines which input signal provides the trigger signal to the time-base unit as controlled by the trigger mode and ADD signals from the trigger selection circuitry.

Resistors R317-R319 establish the input resistance of this stage and provide a load for the trigger output of the Right Vertical plug-in unit (R20-R24 on the Main Interface provide a load for the Left Vertical plug-in unit). R321-R323-R324 and R326-R327-R329 establish the operating level of the Trigger Channel Switch; R321-R323 and R326-R327 set the current gain for each channel. This stage is made up primarily of integrated circuit U324. An input/output table for U324 is shown in Fig. 3-18. U324 provides a high impedance differential input for the trigger signal from the Left Vertical unit at pins 2 and 15 for the trigger signal from the Right Vertical unit at pins 7 and 10. The output signal at pins 12 and 13 is a differential signal. The sum of the DC current at pins 12 and 13 is always equal to the sum of the DC currents at pins 1, 8, 9 and 16 in all modes. This provides a constant DC bias to the stages which follow as the TRIGGER SOURCE or the VERTICAL MODE switches are changed.

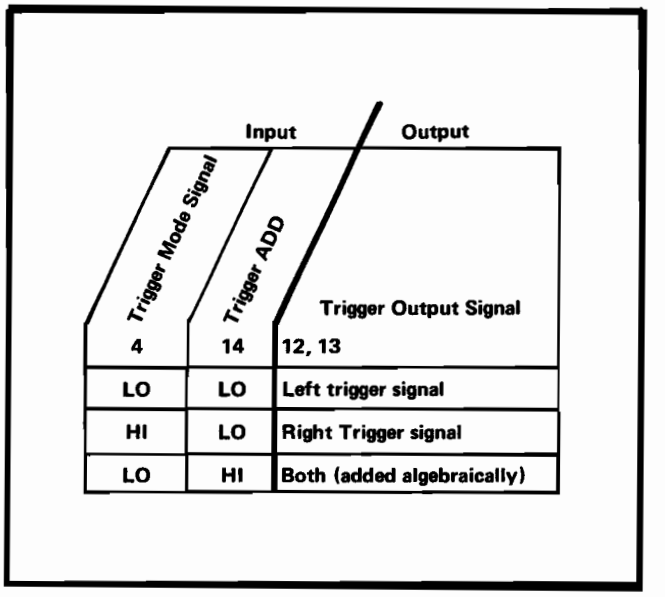


Fig. 3-18. Input/output table for Trigger Channel Switch stage.

When the level at pin 4 is LO (see Trigger Mode and ADD Signals discussion and Fig. 3-18), the trigger signal from the Left Vertical unit passes to the output while the trigger signal from the Right Vertical unit is blocked. A HI level at pin 4 connects the trigger signal from the Right Vertical unit to the output and the trigger signal from the Left Vertical unit is blocked. For VERT MODE operation in the ALT position of the VERTICAL MODE switch, the level at pin 4 switches between the LO and HI level at a rate determined by the Vertical Binary stage (see Logic Circuit description). This action obtains the trigger signal from the Left Vertical unit when the Left Vertical unit is being displayed and from the Right Vertical unit when this unit is being displayed.

When the level at pin 4 is LO and the level at pin 14 is HI, the trigger signal from both the Left and Right Vertical units passes to the output pins. This condition occurs only when the TRIGGER SOURCE switch is set to VERT MODE and the VERTICAL MODE switch is set to either ADD or CHOP. Under this operating mode, the trigger output signal is the algebraic sum of the trigger input signals from the Left and Right Vertical units to prevent triggering on the vertical chopping transition, or only on one signal of an added display.

Trigger Output Amplifier

The trigger output at pins 12 and 13 of U324 is connected to the bases of Q344-Q346 to provide the internal trigger signal for the HORIZ unit (via the Main Interface circuit). This stage provides isolation between the HORIZ unit and the Vertical Signal Buffer stage. The HORIZ unit provides a 50-ohm differential load for this stage. If it is removed from its compartment, the collector load for Q344-Q346 changes and the voltage swing at their collectors increases. The action of this stage prevents this change from affecting the Vertical Signal Buffer stage. CR341-CR349 clamp the collectors of Q344 and Q346 at about +0.6 volt to prevent these transistors from saturating under this no-load condition.

Vertical Signal Buffer

The trigger output signal at pins 12 and 13 of U324 is also connected to the emitters of common-base amplifier Q334-Q336. The output signal at the collectors of Q334 and Q336 is connected to the Vertical Signal Amplifier (see Output Signals and Calibrator description) through R336 and R337. R339 provides a differential output resistance of about 100 ohms.

VERTICAL INTERFACE

General

The Vertical Interface circuit selects the vertical deflection signal from the output of the Left Vertical and/or the Right Vertical plug-in unit. This stage also includes an input from the Readout System to block the vertical signal while readout information is displayed on the CRT. Fig. 3-19 shows a detailed block diagram of the Vertical Interface circuit. A schematic of this circuit is shown on diagram 2 at the rear of this manual.

Vertical Channel Switch

The Vertical Channel Switch determines which input signal provides the vertical signal to the Delay-Line Driver stage as controlled by the Vertical Mode Command from the Logic Circuit. Resistors R200-R202 and R204-R206 establish the input resistance of this stage and provide a load for the Left and Right Vertical units. Resistors R209-R211-R212 and R216-R218-R219 establish the operating levels for this stage. R209-R212 and R216-R219 set the current gain for each channel. C208-R208 and C215-R215 provide frequency compensation.

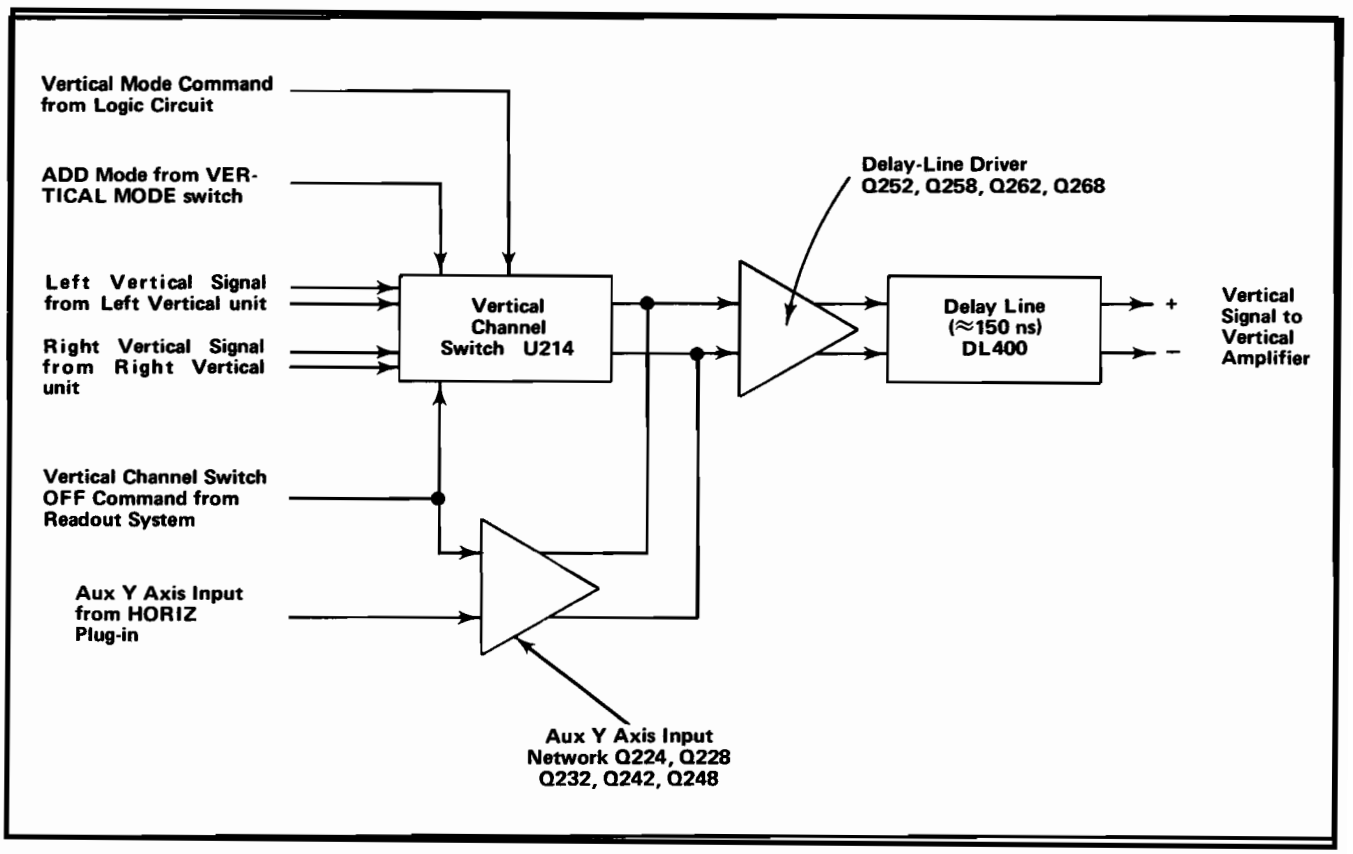


Fig. 3-19. Vertical Interface detailed block diagram.

This stage is made up primarily of integrated circuit U214, which is the same type as used for the Trigger Channel Switch. An input/output table for U214 is shown in Fig. 3-20. U214 provides a high-impedance differential input for the signal from the Left Vertical unit at pins 2 and 15 and the signal from the Right Vertical unit at pins 7 and 10. The output signal at pins 12 and 13 is a differential signal which is connected to the Delay-Line Driver stage through R221-R222. The sum of the DC current at pins 12 and 13 is always equal to the sum of the DC currents at pins 1, 8, 9 and 16 in all modes. This provides a constant DC bias to the following stage as the VERTICAL MODE switch is changed.

When the VERTICAL MODE switch is set to LEFT, the level at pin 4 is LO. This level allows the signal from the Left Vertical unit to pass to the output while the signal from the Right Vertical unit is blocked. In the RIGHT position of the VERTICAL MODE switch, the level at pin 4 is HI. Now, the signal from the Right Vertical unit is connected to the output while the signal from the Left Vertical unit is blocked.

Input			Output
Vertical Mode Command	ADD Mode (Vert)	Vertical Channel Switch OFF	Output signal
4	14	6	12, 13
LO	LO	LO	Left vertical signal
HI	LO	LO	Right vertical signal
LO	HI	LO	Both (added algebraically)
Φ	Φ	HI	Neither (blocked by Readout System)

Φ = Has no effect in this case

Fig. 3-20. Input/output table for Vertical Channel Switch.

When the VERTICAL MODE switch is set to either ALT or CHOP, the Vertical Mode Command at pin 4 switches between the LO and HI levels at a rate determined by either the Chop Counter or the Vertical Binary stages (see Logic Circuit description). This action allows the signal from the Left Vertical unit to be displayed when the Vertical Mode Command is LO and the signal from the Right Vertical unit is displayed when the Vertical Mode Command is HI. When ADD vertical mode operation is selected, a HI level is applied to pin 14 and the level at pin 4 is LO as determined by the Vertical Mode Control stage in the Logic Circuit. This allows both the Right and Left Vertical Signals to pass to the output pins. Now, the signal from both vertical units is algebraically added and the resultant signal determines the vertical deflection.

The Vertical Channel Switch OFF signal from the Readout System which is applied to pin 6 has final control over the output signal from this stage. Quiescently, this signal is LO and the signal from the selected vertical unit can pass to output pins 12 and 13. However, when the Readout System is ready to display readout information, the level at pin 6 goes HI. This level blocks the signal from both vertical units so there is no signal output from this stage under this condition.

Aux Y-Axis Input

The Aux Y-Axis Input from a HORIZ plug-in having this function provides a positioning voltage to offset the display. The Aux Y-Axis signal is connected to a paraphase amplifier consisting of Q224 and Q228. The effective load for the paraphase amplifier is R234 in parallel with R241 on Q224, and R235 in parallel with R238 on Q228. Current from the paraphase amplifier produces a voltage drop across the effective load resistors which causes more current to flow through Q242 and Q248. Q242 and Q248 act as current sources for the Vertical Channel Switch and for Q252-Q258. So, the currents from the Vertical Channel Switch and the Aux Y-Axis Input are summed in the emitters of Q252 and Q258. The Vertical Channel Switch OFF Signal from the Readout System is applied to this stage to block the signal from the Aux Y-Axis Input when readout information is to be displayed on the CRT. Quiescently, this signal is LO and a signal from the Aux Y Axis Input will be added to the signal from the Vertical Channel Switch as described. However, when the Readout System is ready to display readout information, the base of Q232 will go HI. Q232 will conduct and will take over the emitter current in Q224 and Q228. Now, the current that was flowing through these two transistors will flow through Q232. The current through Q232 produces about the same voltage drop across the effective load resistors as was produced by the paraphase amplifier. This limits the common-mode shift that would otherwise occur when the Vertical Channel Switch OFF signal from the Readout System is applied.

Delay-Line Driver

The output of the Vertical Channel Switch stage, along with any current from the Aux Y-Axis Input Network, is connected to the emitters of Q252-Q258. These transistors are connected as common-base amplifiers to provide a low-impedance current-summing point. The signal at the collectors of Q252-Q258 is connected to the bases of Q262-Q268 through R252 and R257. When the trace is at center screen,

diodes CR264-CR266 in the emitter circuits of Q262-Q268 are slightly forward biased by the positive voltage applied to their anodes through R265. As the emitter of either Q262 or Q268 goes positive due to the applied signal at the base, the corresponding diode is reverse biased and its internal resistance increases. This change in resistance produces a decrease in the gain of this stage for large signals, which compensates for the inherent expansion characteristic of the CRT. The output signal from the Delay-Line Driver stage is connected to the Delay Line through T270. This transformer prevents high-frequency common-mode oscillation of Q262-Q268. R271 provides the reverse termination for the Delay Line.

Delay Line

Delay Line L400 provides approximately 150 nanoseconds delay for the vertical signal, to allow the horizontal circuits time to initiate a sweep before the vertical signal reaches the vertical deflection plates of the CRT. This allows the instrument to display the leading edge of the signal originating the trigger pulse when using internal triggering. The delay line used in this instrument has a characteristic impedance of about 50 ohms per side or about 100 ohms differentially. It is of the coaxial type, which does not produce preshoot or phase distortion in the CRT display.

VERTICAL AMPLIFIER

General

The Vertical Amplifier circuit provides the final amplification for the vertical signal before it is applied to the vertical deflection plates of the CRT. This circuit includes an input to produce the vertical portion of a readout display. The BEAM FINDER switch limits the dynamic range of this circuit to compress an over-scanned display within the viewing area of the CRT. Fig. 3-21 shows a detailed block diagram of the Vertical Amplifier circuit. A schematic of this circuit is shown on diagram 4 at the rear of this manual.

Buffer Amplifier

The Buffer Amplifier stage, Q404-Q406, provides a low input impedance for the Vertical Amplifier circuit to permit accurate Delay Line termination. C401-R401, C407-R407 and C400, along with the input resistance of this stage, provide the forward termination for the Delay Line. Collector current for the Delay-Line Driver stage in the Vertical Interface circuit is provided from this stage. The Centering adjustment R405 balances the quiescent DC levels in the Vertical Amplifier circuit so the trace is displayed at the center of the CRT when the inputs to this stage are at the same potential. R406 adjusts the thermal

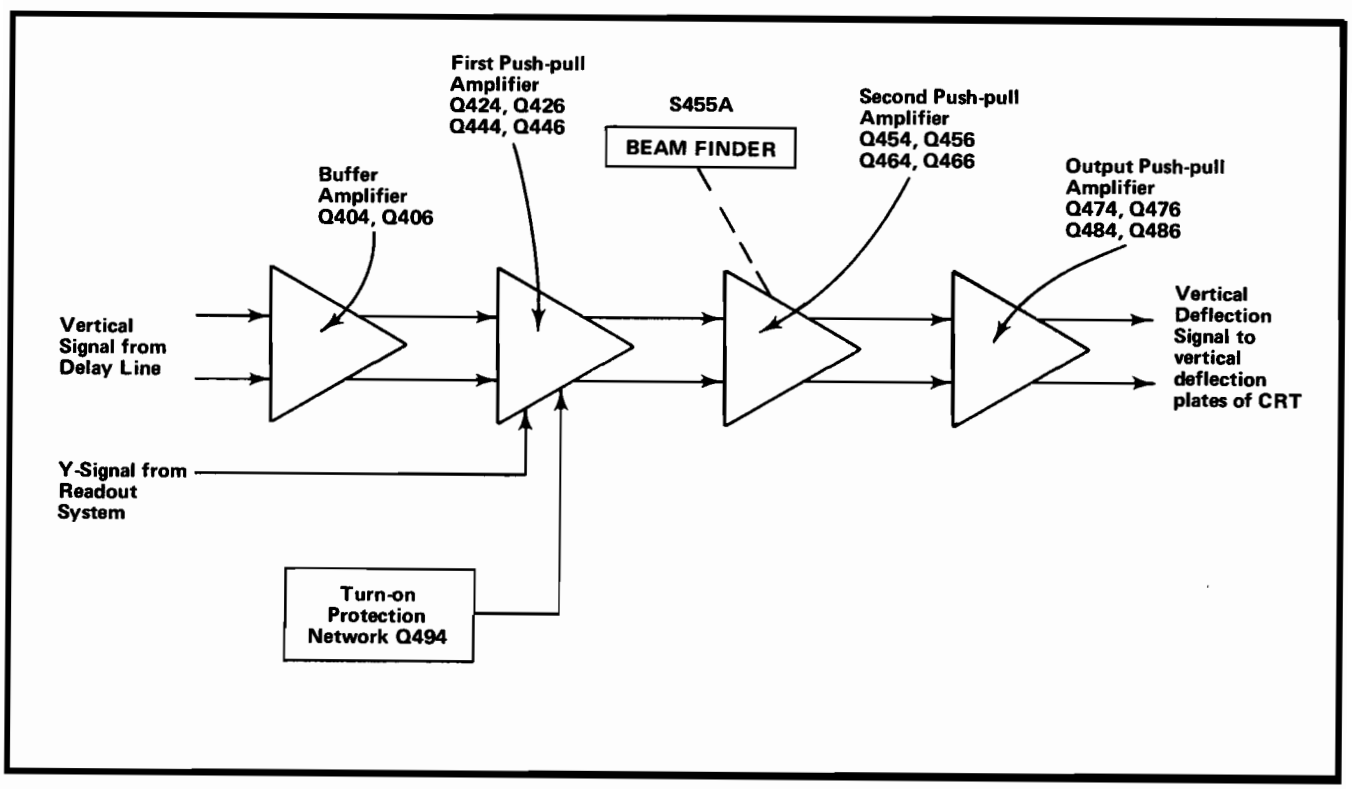


Fig. 3-21. Vertical Amplifier detailed block diagram.

balance of the Vertical Amplifier circuit by varying the emitter current of Q404-Q406. The output signal from the Buffer Amplifier stage is connected to the First Push-Pull Amplifier stage through C411-R411 and C412-R412.

First Push-Pull Amplifier

Q424-Q444 and Q426-Q446 are connected as a push-pull cascode amplifier stage. The Vertical Gain adjustment R415 sets the resistance between the bases of Q424 and Q426 to control the current gain of Q424-Q444. This adjustment sets the overall gain of the vertical deflection system. Thermistors RT423-RT424 and varactors CR431-CR432 provide high frequency temperature compensation for the Vertical Amplifier circuit. As the internal temperature of the instrument rises, the resistance of RT423-RT424 decreases to reduce the reverse bias on CR431-CR432. This increases the capacitance of varactors CR431-CR432 to change the emitter compensation of Q424-Q426 to maintain high-frequency response at high temperatures. The network C434-C435-C436-C437-C439-R434-R435-R436-R437-R439 provide high frequency compensation. C435-R435 in this network are adjustable to provide high-frequency delay-line compensation. C434-R434 provide high-frequency response adjustment for this stage. The output signals at the collectors of Q424-Q426 are connected to the common-base transistors Q444-Q446 through C428-R428-R441 and C429-R429-R442. The low input resistance of the Q444-Q446 common-base transistors allows this stage to provide maximum high-frequency performance.

Q494 and its associated components provide a positioning voltage to deflect the CRT beam upward, off the display area when the instrument is turned on to protect the CRT phosphor from damage due to a high-intensity spot on the display area. When this instrument is turned off, C491 quickly discharges through CR491. Then, when the instrument is turned back on, C491 begins to charge toward −15 volts through R491 since CR491 is reverse biased. While C491 is charging, Q494 is forward biased, and it conducts current away from Q446 through CR493. This current-shunting deflects the display off the viewing area vertically until the high-voltage circuits reach their full operating capabilities. As C491 continues to charge, the collector level of Q494 rises positive until CR493 is reverse biased, which disconnects the Turn-on Protection Network from the Emitter circuit of Q446.

For readout displays, the Y-signal from the Readout System is connected to the emitter of Q446 through R494. Since the signal from the vertical units is blocked in the Vertical Channel Switch under this condition (see Vertical Interface discussion), the readout signal provides the only vertical deflection. Although this signal is connected to the emitter of Q446 as a single-ended signal, it is converted to a push-pull signal by the cross-coupling networks in the following stages.

Second Push-Pull Amplifier

The Second Push-Pull Amplifier, Q454-Q464 and Q456-Q466 operates in the same manner as the previous stage. The main difference between the stages is the compensation networks and the BEAM FINDER switch located in this circuit. L447-R446 in the base circuit and C450 in the emitter circuit of Q454-Q456 provide high-frequency compensation for the Vertical Amplifier circuit.

Normally, the emitter current for Q454-Q456 is supplied through parallel paths; S455A-L454-C454 and R454. When S455A is pressed in, the current source through L454 is interrupted and the only emitter-current source for Q454-Q456 is through R454. This limits the dynamic range of this stage by limiting its current, so the display is compressed vertically within the graticule area. At the same time, −15 volts is connected to the emitters of Q464-Q466 through R461-R462 to maintain the same DC currents in the following stages as when the Beam Finder switch is in the normal position. The BEAM FINDER switch can also be pulled out to lock it in the "find" position to aid in locating the traces of several plug-in units.

Output Push pull Amplifier

The collector signals from Q464-Q466 are connected to the bases of Q474-Q476 in the Output Push pull Amplifier through L474-L476. These inductors provide series peaking for the very high-frequency components of the vertical signal. Q474-Q484 and Q476-Q486 operate in the same manner as the previous stages. The output signals at the collectors of Q484-Q486 provide the vertical deflection signal for the CRT. RC networks C484-R484 and C486-R486 in the base circuits of Q484-Q486, and LR networks LR486-LR487 prevent oscillation of the output transistors. Diode CR485 provides protection for the output transistors by disconnecting the base circuit of Q484-Q486 from the +15-volt supply if it is shorted to ground or to a negative supply. R475-R477 also provide protection for these transistors by providing a small current source to the emitters of Q484-Q486 to prevent them from turning off completely if no current is supplied from the previous transistors. Additional high-frequency compensation for this stage is provided by variable inductor L485.

X-Y DELAY COMPENSATION and HORIZONTAL AMPLIFIER

General

The Horizontal Amplifier circuit amplifies the push-pull horizontal deflection signal from the HORIZ plug-in via the Delay Compensation Network and connects it to the horizontal deflection plates of the CRT. This circuit also includes a stage with inputs from the Readout System to produce the horizontal portion of a readout display. The X-Y Delay Compensation Network provides a delay for the horizontal (X) portion of an X-Y display to match the

delay of the vertical (Y) signal due to the Delay Line. Fig. 3-22 shows a detailed block diagram of the Horizontal Amplifier circuit. A schematic of this circuit is shown on diagram 5 at the rear of this manual.

Delay Compensation Network

Time-Base Operation. When the plug-in unit installed in the HORIZ compartment is operated as a standard time-base unit to produce a horizontal sweep for deflection of the CRT beam, the Delay Compensation Network is effectively disabled. The X Compensation Inhibit Command is HI and relays K521-K525 are not actuated. Therefore, the relay contacts remain in the normally closed position so the horizontal signal passes directly through this network to the Horizontal Amplifier without delay.

X-Y Operation. If the time-base unit installed in the HORIZ compartment is operated as an amplifier or if a vertical unit is installed in the HORIZ compartment, the X Compensation Inhibit to the Delay Compensation Network drops to the LO level (zero volts). This provides an actuating level to relays K521-K525 to connect the Delay Compensation Network into the circuit. Diode CR525 shunts the voltage produced across the relays when the actuating level is removed. For example, if the X Compensation Inhibit from the HORIZ unit goes LO, K521 and K525 close to route the horizontal signal through the Delay Compensation Network. LR networks L521-R521 and L522-R522 along with capacitors C521 and C522 provide a constant input impedance. The LC network composed of C523-C524-C526-C525-L524-L523-L525-L526 provides a fixed delay from DC to about two megahertz to provide minimum phase shift between the X and Y portions of the CRT display. C521 is adjusted to match the horizontal delay to the vertical delay up to at least two megahertz.

Horizontal Signal Input Amplifier

The horizontal signal from the Delay Compensation Network is connected to the bases of Q530 and Q534. Resistors R529-R533 establish the input resistance of this stage and provide a load for the signal output of the HORIZ plug-in unit. This stage provides adjustments to set the overall gain of the Horizontal Amplifier circuit and to

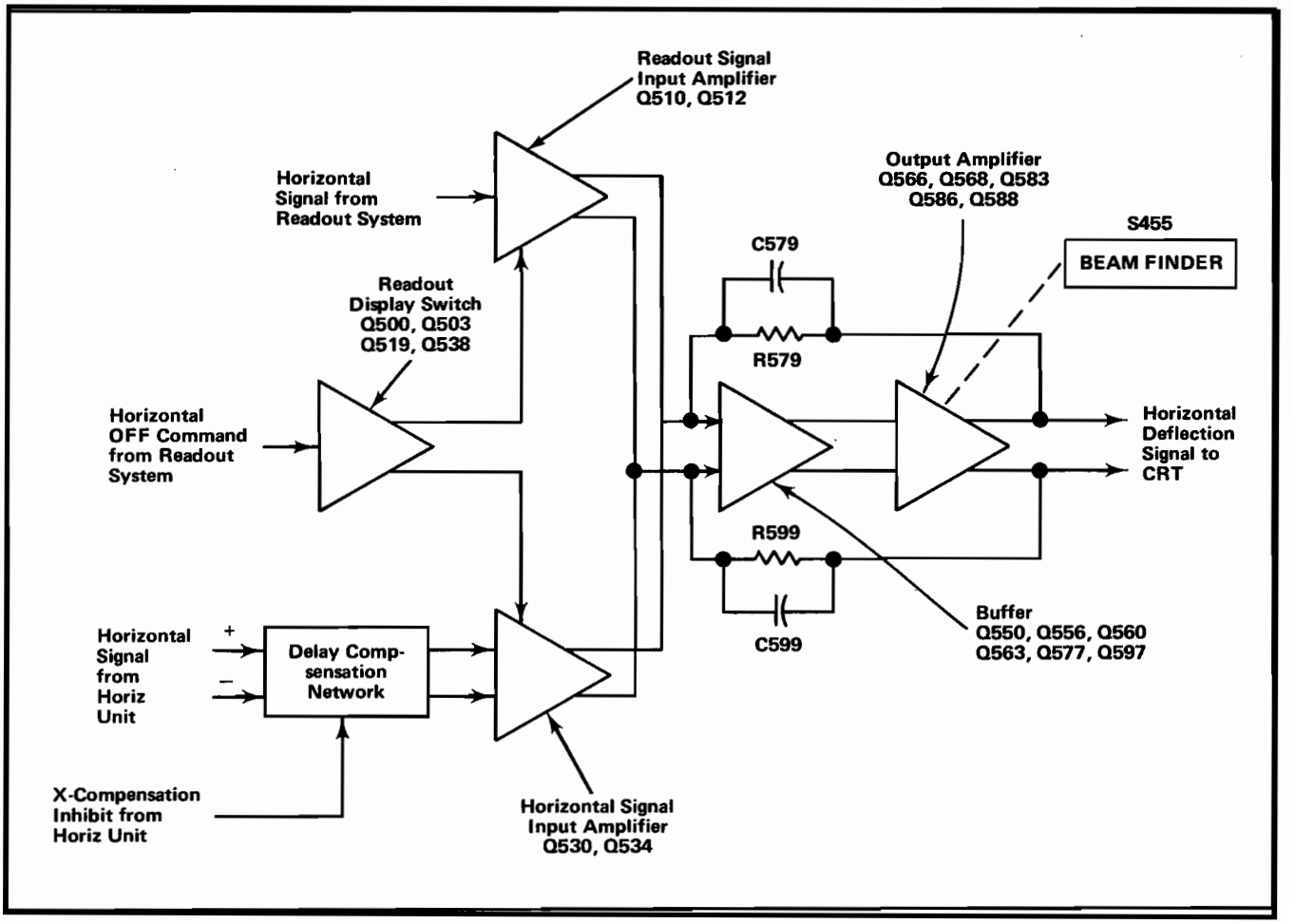


Fig. 3-22. Horizontal Amplifier detailed block diagram.

balance the collector current of Q530 and Q534. Resistors R532-R533-R535-R537-R530 provide degeneration between the emitters of Q530 and Q534. Horizontal Gain adjustment R530 determines the amount of emitter degeneration to control the signal gain of this stage. DC Center adjustment R536 balances the quiescent current through Q530 and Q534 to produce a centered spot on the CRT with no horizontal deflection signal applied. Emitter current for Q530 and Q534 is supplied through Q538 when Q538 is conducting. Q538 is in the Readout Display Switch stage, and will be conducting current except when readout information is to be displayed on the CRT. For instruments which are not equipped with a Readout System, R538 is added between the collector of Q538 and ground. The signal current output from this stage is connected through R542 and R543 to the input of the Buffer Amplifier stage, where it is summed together with the output of the Horizontal Readout Input stage.

Horizontal Readout Input Amplifier

The X signal from the Readout System is connected to the base of Q510 through R507. Q510 and Q512 operate as a paraphase amplifier to convert the single-ended readout signal to a push-pull signal. Resistors R510-R512-R511-R515-R517 provide degeneration between the emitters of Q510 and Q512. R512 determines the amount of emitter degeneration to control the signal gain of this stage. R516 balances the quiescent current through Q510 and Q512 to center the readout display on the CRT. Q519 supplies emitter current for Q510 and Q512 when it is conducting. Q519 is part of the Readout Display Switch stage and is conducting only when readout information is to be displayed. The collectors of Q510 and Q512 are connected, through R540 and R541, to the input of the Buffer Amplifier stage. Here, the signal current from this stage is summed together with the signal current from the Horizontal Signal Input Amplifier stage.

Readout Display Switch

The Readout Display Switch stage blocks the signal from the HORIZ unit when readout information is to be displayed on the CRT. Conversely, this stage blocks readout signals except when the readout information is to be displayed. The Horizontal OFF Command signal from the Readout System is connected to the base of Q503. Q503 and Q500 are emitter-coupled to form a differential switch. The Horizontal OFF Command signal is quiescently LO, so the emitter-base junction of Q503 is forward biased and Q500 is turned off. The current through R504 will flow through Q503 and R539. The resultant voltage drop across R539 forward biases the emitter-base junction of Q538. Q538 then can supply the emitter current for Q530 and Q534 to pass the signal from the HORIZ plug-in. Because Q500 is not conducting, the base-emitter junction of Q519 is reverse biased. Therefore, there is no source of emitter current for Q510 and Q512 and the X signal from the Readout System is blocked. When readout information is to be displayed, the Horizontal OFF Command signal goes HI. This turns off Q503 and Q500 is allowed to conduct. Q519 is turned on to supply emitter current for Q510 and Q512 to pass the X-Readout Signal. Q538 is turned off, and the signal from the HORIZ plug-in is blocked.

Buffer Amplifier and Output Amplifier

The Buffer Amplifier consists of Q550-Q556 and Q560-Q563. Q550 and Q556 are common-base connected to provide low-impedance summing points at their emitters. The input signals are connected to the Buffer Amplifier through the limiting network CR542-CR543-CR545-CR547. These diodes protect the Buffer Amplifier stage from being overdriven by excessive current drive from the input stages. The output signals from the input stages are current signals. With normal horizontal deflection signals which produce an on-screen display, CR545 and CR547 remain forward biased and CR542-CR543 are reverse biased. However, when high-amplitude horizontal deflection signals are applied to this circuit as a result of sweep magnification or high-amplitude external horizontal signals, either CR545 or CR547 is reverse biased, depending on the polarity of the overdrive signal. This results in a sufficient voltage change at the anode of either CR542 or CR543 to forward bias it. The shunt diodes provide a current path for the signal current to limit the voltage change during the overdrive condition. Limit Center adjustment R548 balances the quiescent current at the emitters of Q550 and Q556 so limiting does not occur during the displayed portion of the horizontal deflection signal.

The signal at the collectors of Q550-Q556 is connected to the Output Amplifier through emitter followers Q560-Q563. Q560 and Q563 provide a current gain for the horizontal deflection signal. Each half of the Output Amplifier is a current driven stage with a voltage output to drive the horizontal deflection plates of the CRT and feedback to the input of the Buffer Amplifier stage for linearity. The Output Amplifier has a low input impedance and requires very little voltage change at the input to produce the desired output change. Q583 provides a stable voltage source for the bases of Q568-Q588. Diodes CR560-CR563 limit the negative level at the bases of Q566 and Q586 to about 0.6 volt to protect these transistors in case of failure or removal of Q550 or Q556. Negative feedback is provided from the collectors of Q568 and Q588 to the input of the Buffer Amplifier through feedback networks C579-R579-Q577-C570-R571-R570 and C599-R599-Q597-C590-R591-R590. Emitter followers Q577-Q597 in the feedback networks provide isolation between the input of the Buffer Amplifier and the output of the Output Amplifier stage. With this configuration, the input impedance of the Buffer Amplifier appears low, since the feedback network beyond the emitter followers is effectively disconnected as far as the input signal is concerned. However, the total feedback network is active for the feedback signal. Variable capacitors C573 and C593 adjust the transient response of the feedback networks to provide good linearity at fast sweep rates.

The BEAM FINDER switch, S455, reduces horizontal scan by limiting the voltage swing of Q568 and Q588 when actuated. Normally, the collectors of these transistors are returned to +150 volts, and CR455 is reverse biased to disconnect the +75-volt level. However, when the BEAM FINDER switch is actuated, the power from the +150-volt supply is interrupted and the collector voltage for Q568-Q588 is supplied from the +75-volt supply through CR455. This reduced collector voltage limits the output voltage swing at the collectors of Q568-Q588 to limit the trace within the graticule area.

OUTPUT SIGNALS AND CALIBRATOR

General

The Output Signals and Calibrator circuit provides output signals to the connectors located on the front and side panels. These output signals are either generated within this instrument, or they are samples of signals from the associated plug-in units. Fig. 3-23 shows a detailed block diagram of the Output Signals and Calibrator circuit. A schematic of this circuit is shown on diagram 6 at the rear of this manual.

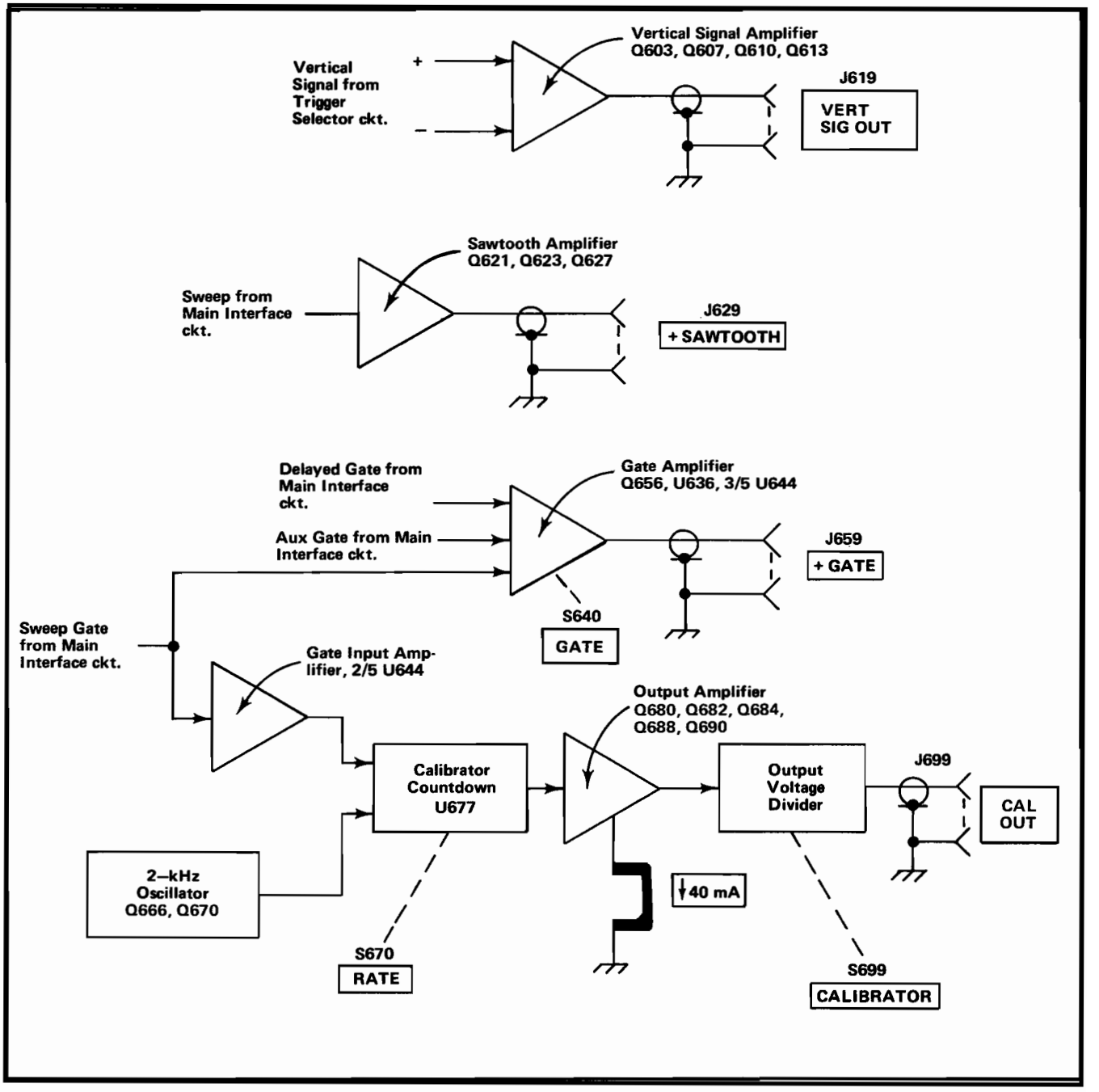


Fig. 3-23. Output Signals and Calibrator detailed block diagram.

Vertical Signal Amplifier

The Vertical signal selected by the Trigger Channel Switch (see Trigger Selector description for more information) is connected to the bases of differential amplifier Q603-Q607. Resistors R600-R601 establish an input resistance of about 50 ohms for this stage. The amplified signal at the collectors of Q603 and Q607 is connected to buffer amplifier Q610-Q613 through RC networks C608-R608 and C609-R609. These networks provide thermal balance for this stage. The single-ended signal at the collector of Q613 is connected to the side-panel VERT SIG OUT connector, J619. The signal at the collector of Q610 is connected to the chassis ground. CR616 and CR617 protect this stage if high-level voltages are accidentally applied to the VERT SIG OUT connector. CR616 provides protection from positive voltages and CR617 provides protection from negative voltages.

Sawtooth Amplifier

The sawtooth signal from the time-base unit is connected to the Sawtooth Amplifier stage through series resistor R40 (on the Main Interface board). Transistors Q621, Q623 and Q627 comprise an inverting feedback amplifier. The gain of this stage is about two, as determined by the ratio of feedback resistor R631 to the input resistance made up of R620 and R40. The signal at the collector of Q627 is connected to the side-panel +SAWTOOTH connector, J629, through R629. RC network C628-R628 provides frequency response stabilization for this stage. Diode CR624 provides protection from high-level positive voltages inadvertently connected to the output connector, by providing a current path to the +15-volt supply through the collector-base junction of Q627. If such a high-level voltage occurs, CR624 is forward biased to clamp the base of Q627 at this level. CR630 provides protection from high-level negative voltages at the +SAWTOOTH connector by clamping the output if it attempts to go more negative than about −15.6 volts.

Gate Amplifier

The output signal at side-panel +GATE connector J659 is selected from three input gate signals by GATE switch S640. The gate signals from the HORIZ plug-in compartment (for gate output signals available, see time-base unit instruction manual) are connected to three comparators, made up from transistors in U644 and U636 transistor arrays (see Fig. 3-24 for schematic diagram of five-transistor array). The GATE switch selects a gate input by supplying a current path to −15 volts for the emitters of the proper comparator. The three comparators share the collector load resistors R646-R647. The input signal selected by S640 is connected to the emitter of Q656 through Q3-U636 and Q3-U644. Diode CR655 provides temperature compensation for common-base connected Q656. The signal at the collector of Q656 is connected to the +GATE connector through CR657 and R659. CR657 protects Q656 if a high-level positive voltage is applied to the +GATE connector, and CR658 clamps the output at about −0.6 volt if a negative voltage is applied to the connector.

Calibrator

General. The Calibrator circuit provides a 40 milliampere current output at the front-panel current loop and a voltage output in calibrated steps from four millivolts to 40 volts at the front-panel CAL OUT connector. Mode and repetition rate of the output signal are selected by the calibrator RATE switch, and the output voltage amplitude is selected by the CALIBRATOR switch.

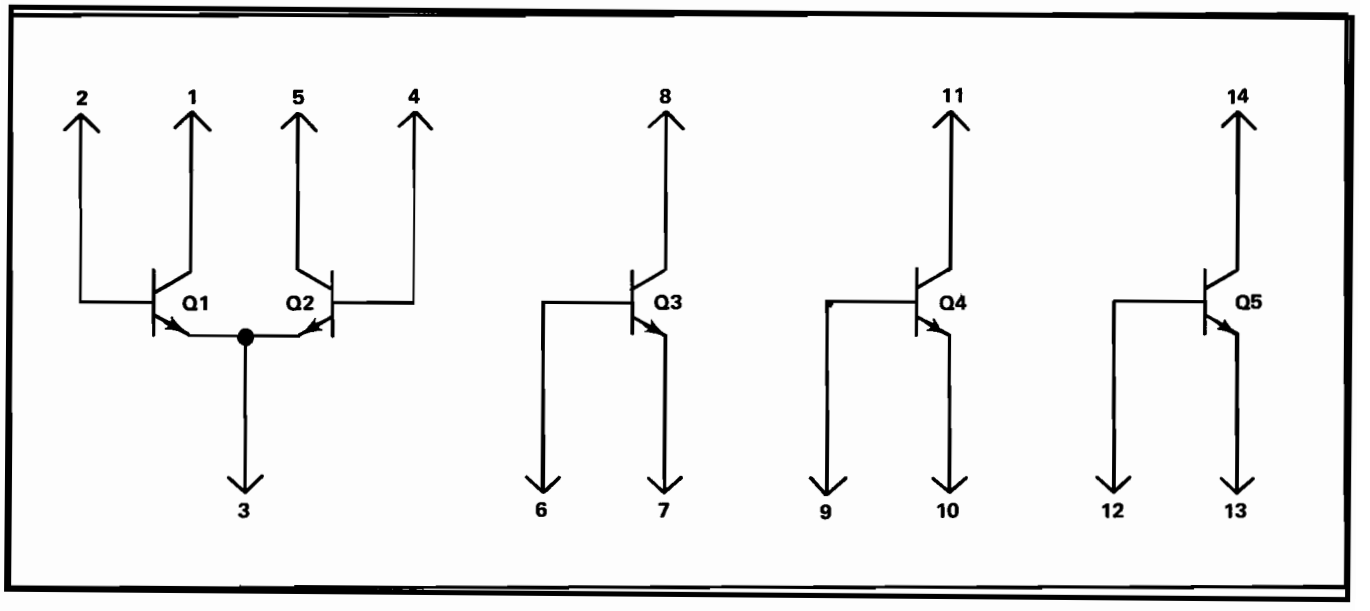


Fig. 3-24. Schematic diagram of five-transistor array identifying individual transistors.

2-kHz Oscillator. Q666 and Q670 are connected as a two-kilohertz square-wave oscillator to provide the drive signal for the Calibrator Countdown stage (one-kilohertz output rate only). Oscillation occurs as follows: Assume that Q666 is conducting and Q670 is off. The collector current of Q666 through R666-R665 produces a voltage level which holds the base of Q670 low. This keeps Q670 turned off, and since there is no current through it, its collector goes positive to produce the positive portion of the square wave. At the same time, C669 begins to charge toward −50 volts through R672. The emitter of Q670 goes negative also as C669 charges, until it reaches a level about 0.6 volt more negative than the level at its base. Then, Q670 is forward biased and its emitter rapidly rises positive. Since C669 cannot change its charge instantaneously, the sudden change in voltage at the emitter of Q670 pulls the emitter of Q666 positive also, to reverse bias it. The current through Q670 produces a voltage drop at its collector to produce the negative portion of the square wave.

Now, conditions are reversed. Since Q666 is reverse biased, there is no current through it. Therefore, C669 can begin to discharge through R668. The emitter level of Q666 follows the discharge of C669 until it reaches about −0.6 volt. Then, Q666 is forward biased and its collector drops negative to reverse bias Q670. This interrupts the current through Q670 and its collector goes positive again to complete the square wave. Once again, C669 begins to charge through R672 to start the second cycle. The signal produced at the collector of Q670 is a two-kilohertz square wave. C673 differentiates this signal to produce positive- and negative-going output pulses, coincident with the rise and fall of the square wave, which provides negative-going trigger pulses for the Calibrator Countdown stage (positive-going pulses have no effect on circuit operation). The 1 kHz adjustment, R665, sets this stage so an accurate one-kilohertz square wave is produced at the output of the Calibrator circuit.

Sweep Gate Buffer. When the RATE switch is in the GATE ÷ 2 position, Q1-Q2 of U644 (5-transistor array) are switched in to invert the Sweep Gate signal to provide negative-going trigger pulses at the sweep rate for the Calibrator Countdown stage.

Calibrator Countdown. Integrated circuit U677 is a triggered set-clear (J-K) flip-flop. An input/output table for this device is shown in Fig. 3-25. The calibrator RATE switch S670 determines the operating mode of U677, and also selects the source of its trigger signal. S670 is a cam-type switch; a contact-closure chart showing its operation is given on diagram 6. The dots on this chart indicate when the associated contact is closed. For the DC position, a LO level is applied to the J input (pin 1) and a HI level is applied to the K input (pin 3). The next negative-going trigger from the 2-kHz Oscillator stage switches the output at pin 7 to its LO level (see input/output table). The output

Input		Output
3	1	Condition at pin 7 after trigger pulse
LO	LO	Output changes state with each trigger pulse
LO	HI	HI
HI	LO	LO
HI	HI	No change

Fig. 3-25. Input/output table for U677.

at pin 7 remains at the LO level as long as the RATE switch remains in this position.

For the 1 kHz position, all contacts except 3 are closed. This places a LO level at both the J and K inputs so that pin 7 changes output levels with each negative-going trigger from the 2-kHz Oscillator stage. This results in a one-kilohertz square wave output signal at pin 7. The J and K inputs are also held LO in the GATE ÷ 2 position of S670 so that U677 changes output levels with each negative-going pulse at its trigger input. However, the signal from the 2-kHz Oscillator is disconnected and the Gate signal provides the trigger to pin 2, resulting in an output square wave with a repetition rate which is one-half the Gate repetition rate.

Output Amplifier

Transistors Q684 and Q688 are connected as a comparator with the reference level at the base of Q688 determined by network R692-R693-R694-R695-Q690. This network establishes a voltage level at the base of Q688 which results in a 40 volt level at its collector when it is on. The 0.4 V adjustment R695 is set in the 0.4 V position of the CALIBRATOR switch, to provide accurate calibrator output voltages at the CAL OUT connector J699. Output Voltage Divider R697 A-H and R696 form a current divider to determine the current through the front-panel 40 mA current loop when S699 is in the 40 mA position. The current loop is a five-turn current transformer, so the effective current applied to a current probe is 40 milliamperes.

The output of the Calibrator Countdown stage is connected to the base of Q680 through R678. Q680 acts as a switch to control the current through Q682, and the output of Q682 controls the conduction of comparator Q684-Q688. When DC operation is selected by the calibrator RATE switch, a LO level is applied to the base of Q680

to cut it off. Therefore, there is no current through Q682 and the base of Q684 rises positive to cut it off also. Now, the collector current of Q688 produces a voltage drop across the Output Voltage Divider to provide a DC voltage output at the CAL OUT connector.

For the 1 kHz and GATE ÷ 2 positions, the base of Q680 varies between the LO and HI levels at the rate selected by the calibrator RATE switch. When the base of Q680 is LO, Q684 is off and Q688 is conducting. This produces an output voltage at the CAL OUT connector as for DC operation. When the level at the base of Q680 is switched to HI, Q684 conducts and Q688 is reverse biased. Now, the voltage level at the CAL OUT connector drops to zero.

Output Voltage Divider. The collector current of Q688 in the Output Amplifier stage is applied across the voltage divider made up of R697 A-H. This divider is designed to provide a low output resistance in all positions while allowing selection of output voltages between 4 mV and 40 V. The CALIBRATOR switch S699 selects the output from the divider to provide the output voltages listed on the front panel (into high-impedance load). The values shown in brackets indicate the output voltage into a 50-ohm load (notice that 40 V position lists no output into 50 ohms and should not be used in this manner). S699 is a cam-type switch and the dots on the contact-closure chart (see diagram 6) indicate when the associated contact is closed.

CRT CIRCUIT

General

The CRT Circuit produces the high-voltage potentials and provides the control circuits necessary for the operation of the cathode-ray tube (CRT). This circuit also includes the Z-Axis Amplifier stage to set the intensity of the CRT display. Fig. 3-26 shows a detailed block diagram of the CRT Circuit. A schematic of this circuit is shown on diagram 7 at the rear of this manual.

High-Voltage Oscillator

Unregulated voltage for operation of the high-voltage supply is provided from the +15-Volts Rectifier (see Low-Voltage Power Supply). Diode CR760 disconnects the negative side of this unregulated voltage from the collector of Q760 at the time of turn-on. This allows the starting current for the High-Voltage Oscillator to be supplied from the +15-Volt Supply through R760 and Q760. As the output of the high-voltage supply increases to its required output level, the collector of Q760 goes negative until

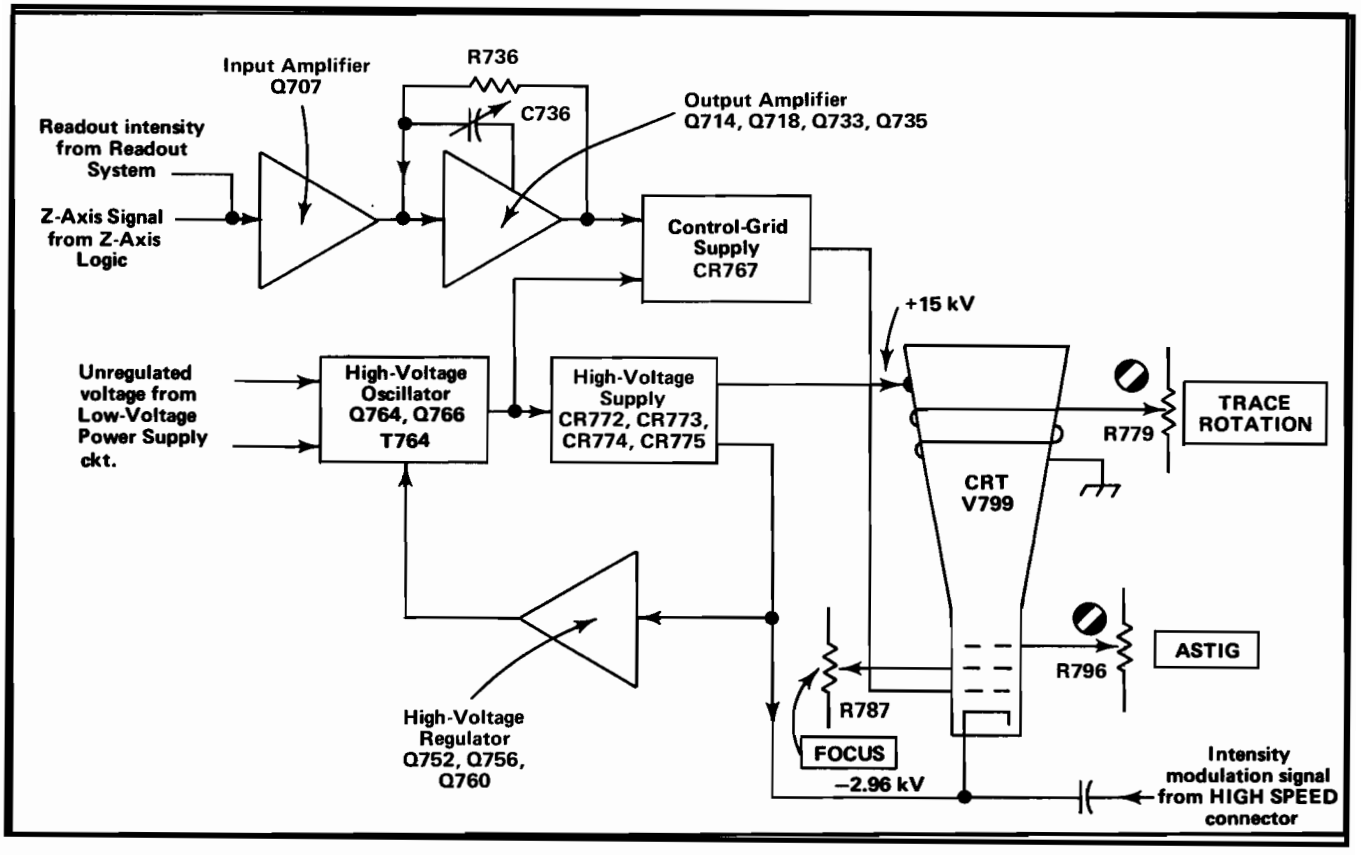


Fig. 3-26. CRT Circuit detailed block diagram.

CR760 is forward biased. Now the collector supply level for Q760 is provided by the negative side of the unregulated voltage. This configuration provides a controlled starting current for the High-Voltage Oscillator at turn-on, and at the same time allows the High-Voltage Regulator stage to control the current for the High-Voltage Oscillator after the stage reaches operating potentials to regulate the output level.

Q764-Q766 and the associated circuitry comprise the high-voltage oscillator to drive the high-voltage transformer T764. When the instrument is turned on, starting current is supplied to the bases of both Q764 and Q766. Both transistors are forward biased, and they both attempt to come into conduction. However, since the transistors will not have identical characteristics (even though they are of the same type), one transistor conducts more heavily than the other. For purposes of the explanation, assume that Q764 conducts more heavily. The collector current of Q764 produces a corresponding current increase in the base-feedback winding of T764 to further increase the bias on Q764. At the same time, the voltage developed across the base-feedback winding connected to Q766 reverse biases it. As long as the collector current of Q764 continues to increase, a voltage is induced into the base-feedback winding of T764 which holds Q764 forward biased. However, when the collector current of Q764 stabilizes, the magnetic field built up in T764 begins to collapse. This induces an opposite current into the base windings which reverse biases Q764, but forward biases Q766. When the induced voltage at the base of Q766 exceeds the bias set by Q760, Q766 is forward biased and the amplified current at its collector adds to the current flowing through T764 due to the collapsing field. Then as the current through T764 stabilizes again, the magnetic field around it once more begins to collapse. This induces a voltage into the base windings which forward biases Q764 and reverse biases Q766 to start another cycle.

The signal produced across the primary of T764 is a sine wave at a frequency of 35 to 45 kilohertz. C765-L765 shapes the signal in the primary of T764 so it maintains essentially a sine-wave characteristic. The amplitude of the oscillations in the primary of T764 is controlled by the High-Voltage Regulator stage to set the total accellerating potential for the CRT. Filter network C762-L762 decouples high peak operating currents from the +15-Volt Supply.

High-Voltage Regulator

A sample of the secondary voltage from T764 is connected to the High-Voltage Regulator stage through divider R740-R744A-R744B-R744C. Q752 and Q756 are connected as an error amplifier to sense any change in the voltage level at the base of Q752. The −15-Volt Supply, connected to the emitter of Q752 through R754, provides the reference level for this stage. High-Voltage adjustment R746 sets the quiescent level at the base of Q752 to a level which establishes a −2.96 kV operating potential at the CRT cathode. CR740 protects Q752 from excessive reverse emitter-base voltage.

Regulation occurs as follows: If the output voltage at the −2.96 kV test point starts to go positive (less negative), a sample of this positive-going change is connected to the base of Q752. Both Q752 and Q756 are forward biased by this positive change, which in turn increases the conduction of Q760. This results in a more positive level at the emitter of Q760 and a more positive bias level at the bases of Q764 and Q766. Now, the bases of both Q764 and Q766 are biased closer to their conduction level so that the feedback voltage induced into their base-feedback windings produces a larger collector current. This results in a larger induced voltage in the secondary of T764 to produce a more negative level at the −2.96 kV test point to correct the original error. In a similar manner, the circuit compensates for output changes in a negative direction. Since the amplitude of the voltage induced into the secondary of T764 also determines the output level of the positive supply and the Control-Grid Supply, the total high-voltage output is regulated by sampling the output of the negative supply.

High-Voltage Supplies

High-voltage transformer T764 has three output windings. One winding provides filament voltage for the cathode-ray tube. Two high-voltage windings provide the negative and positive accelerating potentials for the CRT and provide the bias voltage for the control grid. All of these outputs are regulated by the High-Voltage Regulator stage to maintain a constant output voltage as previously described.

Positive accelerating potential for the CRT anode is supplied by C772-C773-C774-CR772-CR773-CR774. This rectified voltage is filtered by R776 and the capacitance of the CRT to provide a constant output of about +15 kilovolts. All of these components are included in an encapsulated assembly. The negative accelerating potential for the CRT cathode is also obtained from this same secondary winding. Half-wave rectifier CR775 provides an output voltage of about −2.96 kilovolts which is connected to the CRT filament and cathode through L788 and R789. The cathode and filament are connected together through R789 to prevent cathode-to-filament breakdown due to a large difference in potential between these CRT elements. A sample of the negative accelerating voltage is connected to the High-Voltage Regulator stage to maintain a regulated high-voltage output.

Half-wave rectifier CR767 provides a negative voltage for the control grid of the CRT. Output level of this supply

is set by CRT Grid Bias adjustment R768. Neon bulbs DS786A-DS786B-DS786C protect the CRT by limiting the voltage difference between the cathode and control grid to a maximum of about 165 volts if either the Control-Grid Supply or negative High-Voltage Supply should fail. The Unblanking Gate from the Z-Axis Amplifier circuit is connected to the positive side of this circuit. As the Unblanking Gate level changes, it shifts the overall supply level to change the bias on the CRT to control the intensity of the display.

Intensity modulating signals from the rear panel HIGH SPEED Z AXIS connector are applied to the CRT cathode through C785 and RC network C783-R783-R784. This signal changes the CRT bias, and thereby the intensity of the display, by changing the level on the cathode.

CRT Control Circuits

Focus of the CRT display is determined by FOCUS control R787. This control is part of divider R788-R787-R744D-VR786 between the negative high-voltage supply and ground. Therefore, the voltage applied to the focus grid is more positive (less negative) than the voltage on either the control grid or cathode. The ASTIG adjustment R796, which is used in conjunction with the FOCUS control to obtain a well-defined display, varies the positive level on the astigmatism grid. Geom adjustment R792 varies the positive level on the horizontal deflection plate shields to control the overall geometry of the display.

Two adjustments control the trace alignment by varying the magnetic field around the CRT. Y Axis Alignment R794 controls the current through L794 which affects the CRT beam after vertical deflection, but before horizontal deflection. Therefore, it affects only the vertical (Y) components of the display. The TRACE ROTATION adjustment R779 controls the current through L779 and affects both the vertical and horizontal rotation of the beam.

Z-Axis Amplifier

General. The Z-Axis Amplifier circuit is a current driven, shunt-feedback amplifier with a voltage output. This output voltage provides the drive signal to control the CRT intensity level through the Control-Grid Supply. Details of operation for the stages in this circuit follow.

Input Amplifier. Transistor Q707 is a common-base amplifier to estabilsh a low input impedance for the Z-Axis Amplifier stage. The output level of this stage is determined by the input current from either of two circuits. For normal operation, the Z-Axis Signal from the Logic Circuit sets the input current as determined by the front-panel INTENSITY control, the chopped blanking logic or an external signal connected to the rear-panel HIGH-SENSITIVITY Z-AXIS INPUT. For readout displays, the Z-Axis Signal is blocked in the Logic Circuit. In this case, the input current is provided from the Readout System as determined by the READOUT intensity control on the front panel.

Output Amplifier. The output stage is a shunt-feedback operational amplifier with feedback connected from the output to the input through C736-R736. The output voltage is determined by the input current multiplied by the feedback resistor and is expressed by the formula: $E_{out} = I_{in} \times R_{FB}$, where R736 is R_{FB}. The signal current change at the base of Q714 for maximum intensity is about 4 milliamperes. The maximum output voltage change is set for 64 volts (about 4 mA X 15.4 kΩ). AC feedback is provided by C736, which is adjusted for optimum step response. This provides a fast-rise unblanking gate output signal with minimum overshoot and ringing. Otherwise, the CRT display would vary in intensity level following sudden changes in blanking level.

The signal from the Input Amplifier stage is amplified by Q714-Q718. Variable resistor R712 in the base circuit of Q714 provides transient response adjustment for this stage. The signal at the collector of Q718 is connected to the base of transistor Q733 through C729 and to the base of Q735 through R720-C727-R727. These transistors are connected as a collector-coupled complementary amplifier to provide a linear, fast output signal while consuming minimum quiescent power. Q735 maintains the low-frequency response of the input signal and provides a fast falling edge on the output signal. Only the fast-changing portions of the input signal are coupled to the base of Q733 through C729. Since Q733 is a PNP transistor, it responds faster to negative-going changes at its base than to positive-going changes. This action provides a fast rising edge on the output signal (fast falling edge by Q735, an NPN transistor). The signal at the collectors of Q733-Q735 is connected to the Control-Grid Supply through R738-R739.

Diodes CR731-CR714-CR735 provide protection for the Z-Axis Amplifier. CR731 protects this stage from damage due to high-voltage surges connected back into the circuit from the High-Voltage Supply. CR735 protects Q735 by clamping its base at −0.6 volt if Q718 fails or is removed from its socket. CR714 protects Q714 against excess reverse base-emitter voltage.

LOW-VOLTAGE POWER SUPPLY

General

The Low-Voltage Power Supply circuit provides the operating power for this instrument from seven regulated supplies. Electronic regulation is used to provide stable, low-ripple output voltages. Each regulated supply contains a short-protection circuit to prevent instrument damage if a supply is inadvertently shorted to ground. The Power Input stage includes the Voltage Selector Assembly. This assembly allows selection of the nominal operating voltage and regulating range for the instrument. Fig. 3-27 shows a detailed block diagram of the Low-Voltage Power Supply

circuit. A schematic of this circuit is shown on diagrams 8A, 8B and 8C at the rear of this manual.

Power Input

Power is applied to the primary of transformer T801 through the EMI (electro-magnetic interference) filter FL801, 115-volt line fuse F801, POWER switch S801, thermal cutout S800, Voltage Selector switch S802 and Range Selector switch S803. Voltage Selector switch S802 connects the two halves of the primary of T801 in parallel for 115-volt nominal operation, or in series for 230-volt nominal operation. A second line fuse, F802, is connected into the circuit when the Voltage Selector switch is set to 230 V position to provide the correct protection for 230-volt operation (F802 current rating is less than the rating of F801).

Range Selector switch S803 allows the instrument to regulate correctly on higher or lower than normal line voltages. Each half of the primary of T801 has taps above and below the 115-volt (230) nominal point. As Range Selector switch S803 is switched from LO to M to HI, more turns are effectively added to the primary winding and the turns ratio is decreased. This configuration compensates for higher or lower than normal line voltage to extend the regulating range of the Low-Voltage Power Supply.

Thermal cutout S800 provides thermal protection for this instrument. If the internal temperature of the instrument exceeds a safe operating level, S800 opens to interrupt the applied power. When the temperature returns to a safe level, S800 automatically closes to re-apply the power.

–50-Volt Supply

The following discussion includes the description of the –50-Volt Rectifier, –50-V Series Regulator, –50-V Feedback Amplifier, –50-V Reference and –50-V Current Limiting stages. Since these stages are closely related in the production of the –50-volt regulated output voltage, their operation is most easily understood when discussed as a unit.

The –50-V Rectifier assembly CR821 rectifies the output at the secondary of T801 to provide the unregulated voltage source for this supply. CR821 is connected as a bridge rectifier, and its output voltage is filtered by C822 before it is applied to –50-V Series Regulator Q823. Q825-Q827 and Q1-Q2-Q5 of transistor array U840 (see Fig. 3-28) operate as a feedback-stabilized regulator circuit to maintain a constant –50-volt output level. Q1-Q2 of U840 are connected as a differential amplifier to compare the feedback signal at pin 2 against the reference signal at pin 4. The error output signal at pin 5 reflects the difference, if any, between the two inputs. The change in level at the error output is always in the same direction as the change at the feedback input (in phase). The error output signal at pin 5 is connected to the –50-V Series Regulator through emitter follower Q827-Q825. Q5 of U840 is diode connected to provide further temperature compensation for the differential amplifier.

Zener diode VR840 sets a reference level of about –9 volts at pin 4 of U840. A sample of the output voltage from this supply is connected to the feedback input (pin 2) through divider R844-R845-R846-R488. R848 in this divider is adjustable to set the output voltage level of the supply. Notice that the feedback voltage to this divider is obtained from a line labeled –50 V Sens. Fig. 3-29 illustrates the reason for this configuration. The inherent resistance of the interconnecting wire between the output of the –50-Volt Supply and the load produces a voltage drop which is equal to the output current multiplied by the resistance of the interconnecting wire. Even though the resistance of the wire is small, it results in a substantial voltage drop due to the high output current of this supply. Therefore, if the feedback voltage were obtained ahead of this drop, the voltage at the load might not maintain close regulation. However, the –50 V Sens configuration overcomes this problem, since it obtains the feedback voltage from a point as close as practical to the load. Since the current in the –50-C Sens line is quite small, the feedback voltage is an accurate sample of the voltage applied to the load.

Regulation occurs as follows: If the output level of this supply decreases (less negative) due to ripple, changes in load, or changes in line voltage, the voltage at pin 2, U840 decreases also. A positive-going change at the feedback input to the differential amplifier results in a positive-going change in the error output signal at pin 5. This allows more base current to flow through Q827 and Q825, resulting in increased conduction of –50-V Series Regulator Q823. This action increases the load current, and the output voltage of this supply increases (more negative). The feedback voltage from the –50 V Sens line increases, and the feedback input to the differential amplifier returns to the same level as the reference input. Similarly, if the output level of this supply increases (more negative), the error output signal to the base of Q827 becomes more negative. Less current can flow through Q827 and Q825, reducing the conduction of Q823 to decrease the output voltage of this supply.

The –50 Volts adjustment R848 determines the divider ratio to pin 2 of U840 and thereby determines the feedback voltage. This adjustment sets the output level of the supply in the following manner: if R848 is adjusted so the voltage at its variable arm goes less negative (closer to ground), this appears as an error signal at pin 2 of U840. In the same manner as described previously, this positive-going change at the feedback input (pin 2) increases the conduction of

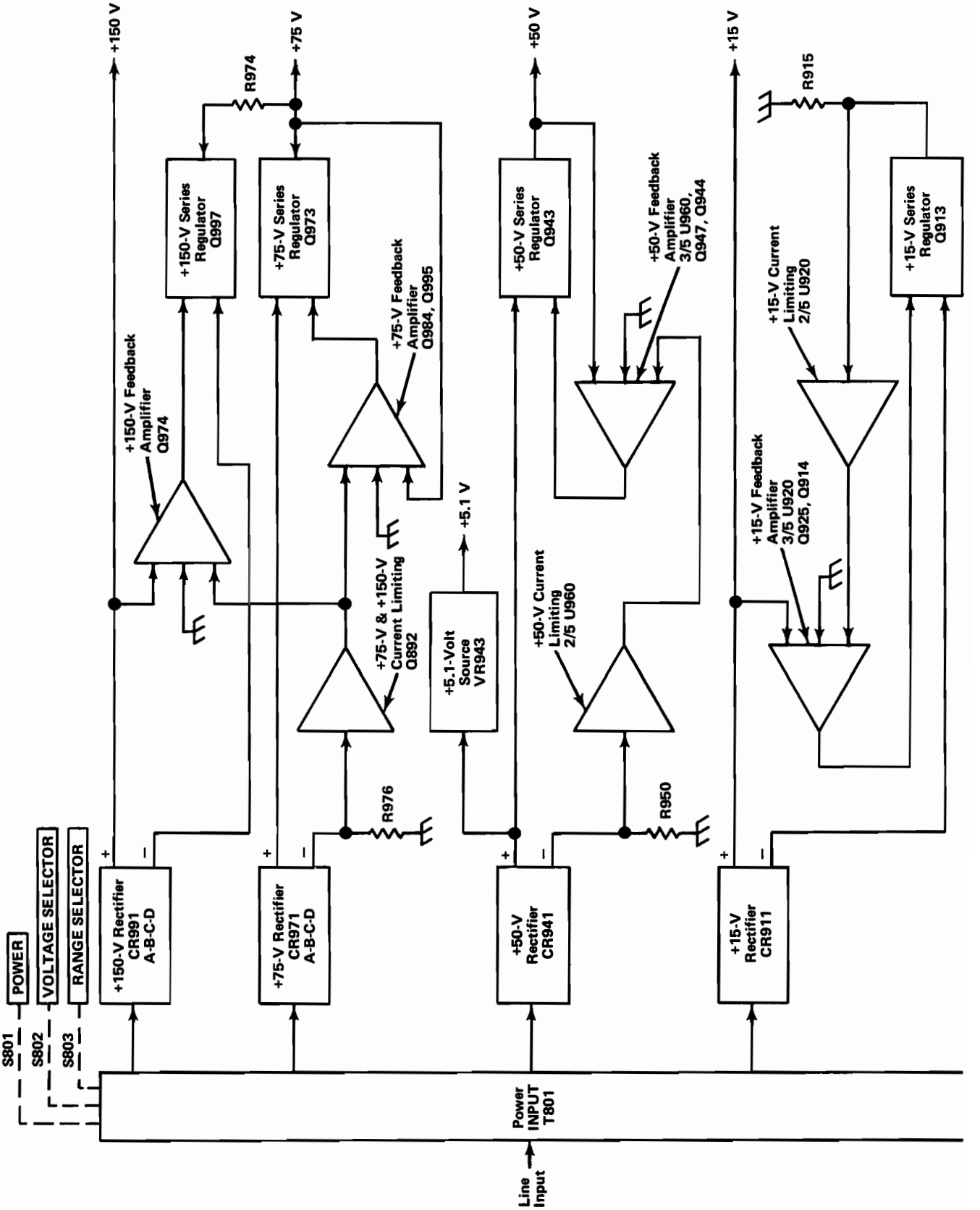


Fig. 3-27. Low-Voltage Power Supply detailed block diagram.

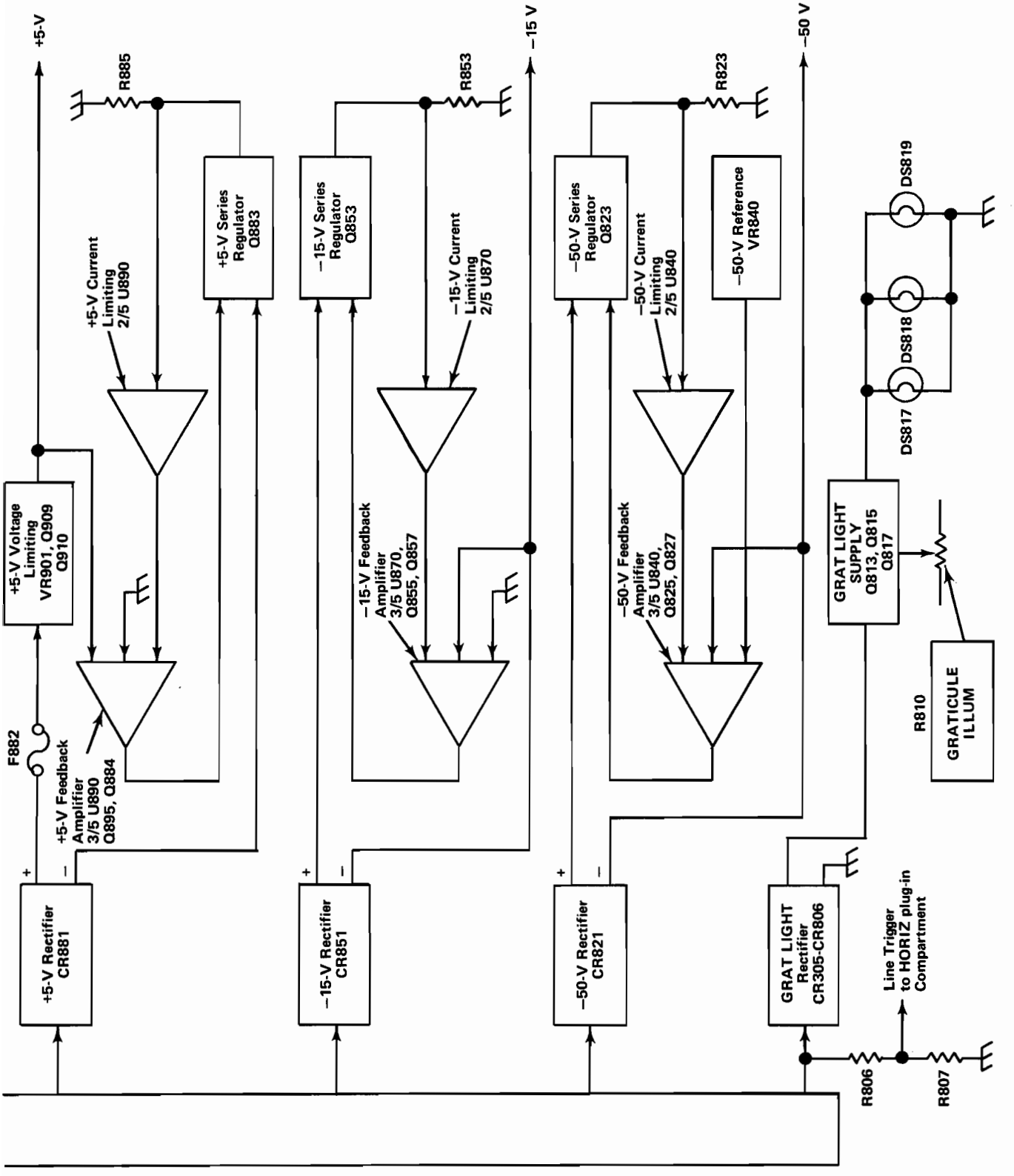


Fig. 3-27. Low-Voltage Power Supply detailed block diagram.

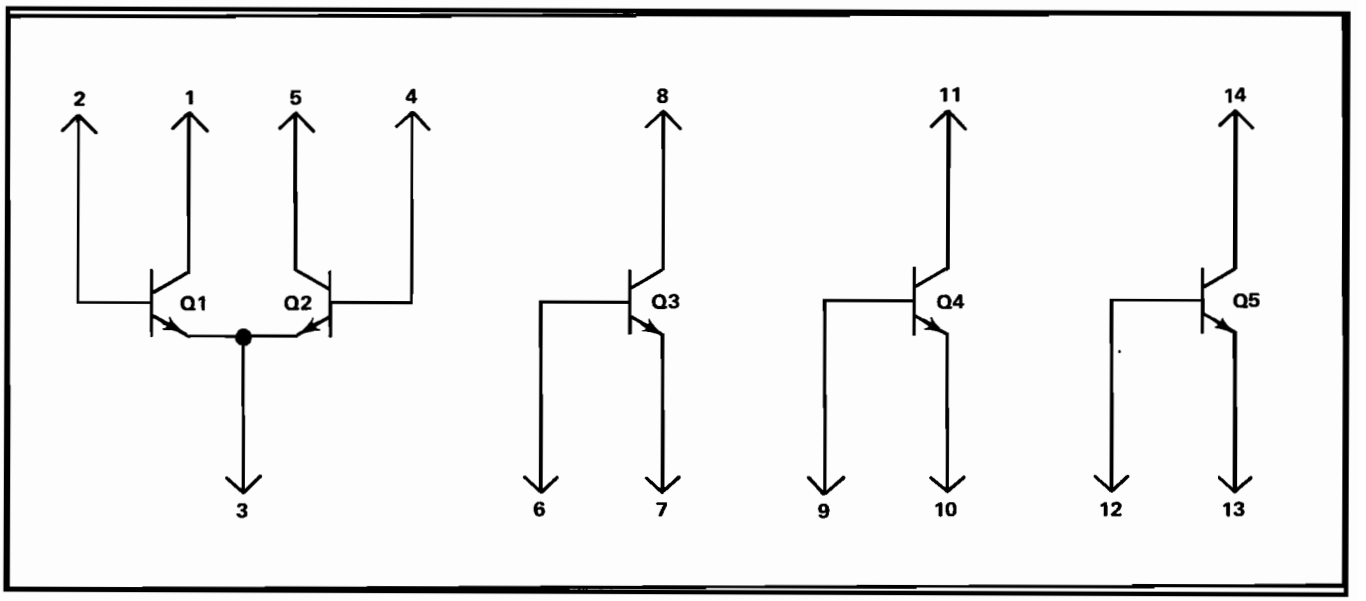


Fig. 3-28. Schematic diagram of five-transistor array identifying individual transistors.

the —50 V Series Regulator to produce more current through the load, and thereby increase the output voltage of this supply. This places more voltage across divider R844-R846-R845-R848, and the divider action returns the feedback input (pin 2) to about —9 volts. Notice that the feedback action of this supply forces a change in the output level which always returns the feedback input (pin 2) to the same level as the reference input (pin 4). In this manner, the output level of the —50-Volt Supply can be set to exactly —50 volts by correct adjustment of R848.

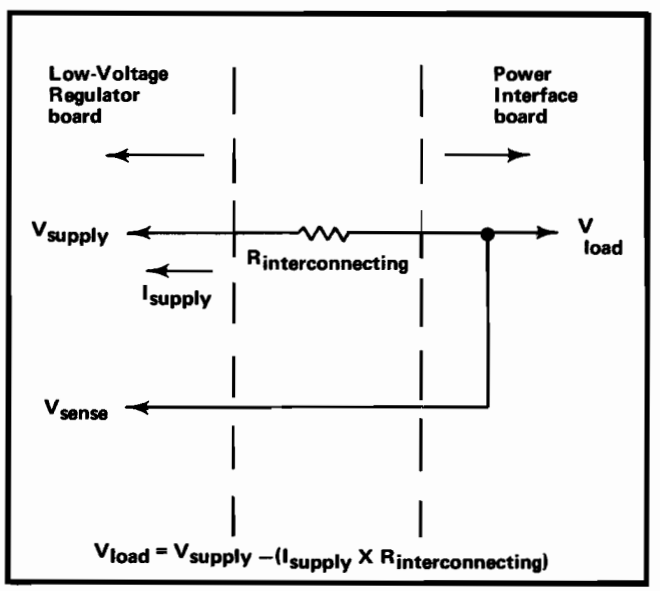


Fig. 3-29. Schematic illustrating voltage drop between power-supply output and load due to resistance of interconnecting wire.

The —50-V Current Limiting stage Q3-Q4 of U840 protects the —50-Volt Supply if excess current is demanded from this supply. Since the ground return for the —50-Volt Supply is through R823, all current from the —50-Volt Supply must flow through R823. The voltage drop across R823 is connected to the base of Q4, U840 through diode-connected Q3, U840 and divider R830-R831. Transistor Q4, U480 senses the voltage drop across R823 and compares it to the voltage at its emitter established by divider R838-R839. When excess current is demanded from the —50-V Series Regulator due to a short circuit or similar malfunction at the output of this supply, the voltage drop across R823 increases until the voltage at pin 9, U840 is sufficient to forward bias Q4, U840. The collector current of Q4, U840 results in a reduction of current through Q827 and Q825 to limit the conduction of Q823. As the output voltage decreases due to the malfunction at the output, the bias established by divider R830-R831 increases. This increases the conduction of Q4, U840 to further limit the current through Q823. The current limiting protects Q823 from damage due to excess power dissipation. CR849 protects the —50-V Supply from damage if its output is shorted to one of the positive supplies. C834-R834 prevent oscillation in the feedback network.

—15-Volt Supply

Rectified voltage for operation of the —15-Volt Supply is provided by rectifier assembly CR851. This voltage is filtered by C852 to provide the unregulated voltage source for this supply. Basic operation of all stages in the —15 V Supply is the same as for the —50-Volt Supply. Reference level for this supply is established by divider R870-R871 between the —50-V Sens and ground. The output voltage is regulated in the same manner as described for the —50-Volt Supply.

+5-Volt Supply

Bridge rectifier CR881 A-B-C-D provides the rectified voltage for the +5-Volt Supply. The +5-V Series Regulator Q883 operates the same as the series regulators in the negative supplies, except that it is connected in the negative side of the supply. Reference level for this supply is ground applied to the differential comparator at pin 2, U890. A sample of the output of this supply is connected to the feedback input of the comparator (pin 4) through divider R903-R904. The error output signal at pin 1, U890 is inverted by Q895 and is connected to the +5-V Series Regulator through emitter-follower Q884. The output voltage is regulated in the following manner: if the output level of this supply increases (more positive), the voltage at pin 4, U890 also increases. A positive-going change at the feedback input to the differential comparator results in a positive-going change at pin 1, U890. This positive-going error signal is inverted by Q895 to a negative-going change and is applied to the +5-V Series Regulator through Q884. This action results in decreased conduction of the +5-V Series Regulator, which decreases the load current and thereby decreases the output voltage. The feedback voltage from the +5-V Sens now decreases the level at pin 4, U890 returns to that of the reference input to pin 2, U890 (ground). Similarly, if the output level of this supply decreases, the error output signal to the base of Q883 becomes more positive. This increases the conduction of Q883 to increase the output voltage of the supply.

The ground return for the +5-V Series Regulator is through current-sensing resistor R885. The voltage drop across R885 is sensed by a differential comparator composed of Q3-Q4, U890. The voltage drop across R885 is applied to pin 6, U890 through R886 and divider R887-R888. When the current through R885 is normal, the resulting voltage applied to pin 6, U890 will forward bias that base-emitter junction. As a result, the other transistor in the comparator, Q4-U890, is shut off. When excess current is demanded from this supply, the voltage drop across R885 increases (becomes more negative). The resulting voltage at pin 6, U890 reverse biases that base-emitter and causes Q4-U890 to conduct. The collector current through Q4-U890 removes the emitter current for Q895, thereby removing the drive for Q884 and Q883. As the output voltage decreases due to the malfunction at the output, the bias established by divider R887-R888 decreases to keep Q3-U890 reverse biased.

The +5-V Voltage Limiting stage provides protection for the light bulbs and integrated circuits which are powered from this supply if the output voltage rises above the normal five-volt level. The +5-volt output of this supply is connected across zener diode VR907 through R907. Under normal conditions, there is not enough voltage across VR907 to place it in the zener region. However, if the output of this supply rises positive due to a short to a more positive supply, or similar malfunction, the gate of Q909 (programmable unijunction transistor) is clamped at about +6.5 volts through R908 by zener diode VR907. As the output voltage increases to about +6 volts, Q909 is forward biased and its cathode current triggers silicon-controlled rectifier Q910 through R910. When Q910 conducts, it effectively shorts the output of the +5-V Supply to ground, demanding high output current. This high current is sensed by the +5-V Current Limiting stage and the output current is reduced as described previously. The output remains limited until the instrument is turned off and the problem is corrected. A momentary voltage surge may also trigger the +5-V Voltage Limiting stage and cause the +5-Volt Supply to shut down. Power can be restored in this case by momentarily turning off the POWER switch and returning it to ON.

Fuse F882 provides further protection for this supply. If the +5-V Current Limiting stage malfunctions (for example, collector of +5-V Series Regulator shorted to ground) and a condition occurs which demands current limiting, F882 opens to interrupt the output of this supply before damage can occur. Due to the high current output of this supply, a separate ground return is used for this supply to prevent its heavy return current from affecting other supplies in the instrument.

+15-Volt Supply

Rectifier assembly CR911 provides the rectified voltage for the +15-Volt Supply. This unregulated voltage is also connected to the High-Voltage Oscillator stage in the CRT circuit through F912. This fuse protects the +15-V Rectifier from damage due to failures in the High-Voltage Oscillator stage. Basic operation of the stages in this circuit are the same as described for the previous supplies.

+50-Volt Supply

Bridge rectifier assembly CR941 provides the rectified voltage for the +50-V Supply. This unregulated voltage is applied across zener diode VR943 through R943 to provide a +5.1-volt source for operation of several circuits within the Low-Voltage Power Supply circuit. Regulation occurs much the same as described for the previous supplies. The Feedback Amplifier is referenced to ground at pin 2, U960. The feedback input is supplied from the +50-V Sens through divider R966-R967. The error output signal from pin 1, U960 is inverted by Q947 and is applied to the +50-V Series Regulator through emitter-follower Q944. When the feedback input goes positive, a negative-going change is applied to the +50-V Series Regulator to decrease the conduction of Q943. A similar but opposite action occurs if the feedback input goes negative. The +50-V Current Limiting stage is made up of Q3-Q4, U960. It senses the voltage drop across R950 to provide protection for this supply if excess current is demanded.

+75-Volt Supply

Unregulated +75-volts is provided by bridge rectifier CR971 A-B-C-D and filtered by C972-R972. Q973 is con-

nected as a series regulator in the positive side of the supply. Q984 is connected as the +75-V Feedback Amplifier. Q984 applies an inverted error output signal to Q973 through emitter-follower Q995. Notice that the collector supply voltage for Q995 is taken from the +150-V Supply through R995. The current limiting function for the +75-V Supply is shared with the +150-V Supply and is described in the discussion of that supply.

+150-V Supply

Bridge rectifier assembly CR991 A-B-C-D provides the rectified voltage for the +150-Volt Supply. However, this secondary winding of T801 does not supply the full potential necessary to obtain the +150-volt output level. To provide the required output level, the negative side of this supply is connected to the output of the +75-Volt Supply through the +150-V Series Regulator so that the two supplies are effectively connected in series between ground and the +150-volt output. The +150-V Feedback Amplifier Q974 and +150-V Series Regulator Q997 provide basic regulation for the output level in a manner similar to that described for the +75-Volt Supply. Changes in the output level appear as error signals at the base of Q974 (reference established by +75-volts connected to emitter through R974). These changes are reflected to the base of Q997 to provide regulation of the output level. The ground return for both the +75-V Supply and the +150-V Supply is through current-sense resistor R976. The bias established on the base of Q982 by divider R978-R979 will forward bias Q982 under normal conditions. If the current demand on either supply becomes excessive, the resulting voltage at the base of Q982 will reduce the forward bias on the base-emitter of Q982 and the collector will rise. This is connected to the feedback amplifiers of both supplies; to Q984 through R988 and divider R986-R987, and to Q974 through R982 and CR974. This action results in decreased conduction through both series regulators.

Graticule-Light Supply

The graticule lights DS817-DS818-DS819 are powered by the Graticule Light Supply consisting of Q813-Q815-Q817. Rectified voltage for this supply is provided by CR805-CR806 from a center-tapped secondary winding of T801. The setting of the front-panel GRATICULE ILLUM control determines the voltage at the emitter of Q813 and applies it to the graticule lights through emitter-follower Q817 and R818-R819. Current limiting protection for this supply is provided by Q815 should a short or similar malfunction occur on the line to the graticule lights. Circuit operation is as follows: The voltage level at the center arm of the GRATICULE ILLUM control R810 is applied to the base of Q813 through divider R811-R812. The resulting voltage level at the base of Q813 is applied to the graticule lights through emitter-followers Q813-Q817 and R818-R819. A voltage level is applied to the base of Q815 from the emitter of Q813 through divider R814-R815-R816 which is more positive than the voltage applied to the the graticule lights. If the current through R818-R819 becomes excessive due to a short or similar malfunction, the emitter current through Q815 will increase. This will result in the collector of Q815 dropping, which will cut off the drive to Q813 and Q817, thereby protecting Q817 from damage due to excessive conduction.

Voltage divider R806-R807 provides a sample of the line voltage to the plug-in connectors in the Main Interface circuit for internal triggering at line frequency or for other applications.

MODE SWITCHING AND REAR-PANEL CONNECTORS

General

Diagram 9 shows the mode switches of the 7503 and the interconnections between these switches and the circuit boards, as well as interconnections between the circuit boards within this instrument.

Switch Logic

The VERTICAL MODE switch determines the operating mode of the Vertical Interface circuit. This switch is designed so that it is self-canceling; i.e., only one of the buttons can be pressed at a time. Operation of this switch is discussed in connection with the circuits it controls.

The TRIGGER SOURCE switch controls the operation of the Trigger Selector circuit. This switch is also self-canceling so that only one of the buttons can be pressed at a time. Operation of this switch is discussed in connection with the Trigger Selector circuit.

Indicator Lights

The indicator lights shown in connection with the VERTICAL MODE switch indicate which mode has been selected. When one of the buttons of the switch is pressed, it completes the circuit between the associated bulb and the lamp-common line. Notice that a separate bulb is used for each mode switch position. The selected button of the TRIGGER SOURCE switch is also illuminated to indicate the trigger source. Notice that only one bulb is associated with the TRIGGER SOURCE switch. The source switch is designed so that the button which is pressed receives light from the bulb, but the remaining buttons remain unlighted.

The CONTROL ILLUM switch S1040 determines the illumination level of the pushbutton switches on the 7503 and the associated plug-in units. In the HIGH position of this switch, the lamp power from the Low-Voltage Power Supply circuit is connected directly to the light bulbs. In

the LOW position, the lamp power is connected to the bulbs through diodes CR1041 and CR1042. The forward drop across these diodes reduces the current available to the bulbs so that they operate at a lower intensity level. In the OFF position, the lamp power to all of the pushbutton switches is disconnected.

The Z-Axis Inputs, HIGH SPEED J1055 and HIGH SENSITIVITY J1060, located on the rear panel of the 7503 connect into P1002, to connect into P12 on the Main Interface circuit for routing to the appropriate circuits. The rear-panel PROBE POWER connectors, J1080 and J1085, provide high voltages from the Low-Voltage Power Supply circuit to operate active probes. The 9-Pin Connector J1075 permits external resetting of the single sweep function, and a lamp supply to indicate that the sweep is ready for single sweep operation.

READOUT SYSTEM

Introduction to Readout System

General. The Readout System in the 7503 provides alphanumeric display of information encoded by the plug-in units. This display is presented on the CRT and is written by the CRT beam on a time-shared basis with the analog waveform display. Schematics for the total Readout System are shown on diagrams 10, 11 and 12 at the rear of this manual.

The definitions of several terms must be clearly understood to follow this description of the Readout System. These are:

Character—A character is a single number, letter, or symbol which is displayed on the CRT, either alone or in combination with other characters.

Word—A word is made up of a related group of characters. In the 7503 Readout System, a word can consist of up to ten characters.

Frame—A frame is a display of all words for a given operating mode and plug-in combination. Up to six words can be displayed in one frame. Fig. 3-30 shows one complete frame (simulated readout) and the position at which each of the six words is displayed.

Column—One of the vertical lines in the Character Selection Matrix (see Fig. 3-31). Columns C-0 (column zero) to C-10 (column 10) can be addressed in the 7503 system.

Row—One of the horizontal lines in the Character Selection Matrix (Fig. 3-31). Rows R-1 (row 1) to R-10 (row 10) can be addressed in the 7503 system.

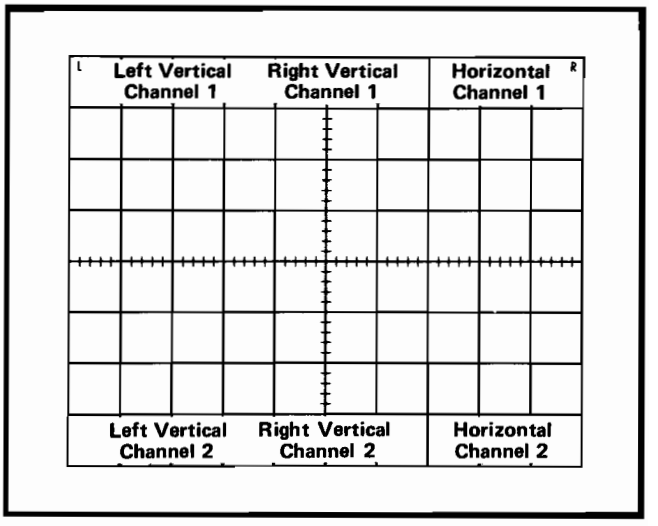


Fig. 3-30. Location of readout words on the CRT identifying the originating plug-in and channel (one complete frame shown, simulated readout).

Time-slot—A location in a pulse train. In the 7503 Readout System, the pulse train consists of 10 negative-going pulses. Each of these time-slots is assigned a number between one and ten. For example, the first time-slot is TS-1.

Time-multiplexing—Transmission of data from two or more sources over a common path by using different time intervals for different signals.

Display Format. Up to six words of readout information can be displayed on the 7503 CRT. The position of each word is fixed and is directly related to the plug-in unit from which it originated. Fig. 3-30 shows the area of the graticule where the readout from each plug-in unit is displayed. Notice that channel 1 of each plug-in unit is displayed within the top division of the CRT and channel 2 is displayed directly below within the bottom division. Fig. 3-32 shows a typical display where only channel 1 of the Right Vertical and both channels of the Horizontal unit are selected for display.

Each word in the readout display can contain up to 10 characters, although the typical display will contain between two and seven characters per word. The characters are selected from the Character Selection Matrix shown in Fig. 3-31. Any one of the 50 separate characters can be addressed and displayed on the CRT. In addition, 12 operational addresses are provided for special instructions to the Readout System. The unused locations in the Matrix (shaded areas) are available for future expansion of the Readout System. The method of addressing the locations in the Character Selection Matrix is described in the following discussion.

Row Number ↓ / Column Number →	Current (Milli-amperes)	C-0	C-1	C-2	C-3	C-4	C-5	C-6	C-7	C-8	C-9	C-10
		0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	⩾1.0
R-1	0		*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*
R-2	0.1		↓	<	*I*	/	+	–	+	*C*	Δ	>
R-3	0.2		Add* one zero	Add* two zeros	Reduce* prefix	Reduce* prefix and add one zero						*IDENTIFY**
R-4	0.3		*m*	*μ*	*n*	*p*	*X*	*K*	*M*	*G*	*T*	*R*
R-5	0.4	SKIP*	*S*	*V*	*A*	*W*	*H*	*d*	*B*	*c*	Ω	*E*
R-6	0.5		*U*	*N*	*L*	*Z*	*Y*	*P*	*F*	*J*	*Q*	*D*
R-7	0.6				Decimal* point location #3	Decimal* point location #4	Decimal* point location #5	Decimal* point location #6	Decimal* point location #7			
R-8	0.7											
R-9	0.8											
R-10	0.9	Add Space In Display*										

Unused locations. Available for future expansion of Readout System

Operational address.

Fig. 3-31. Character Selection Matrix for 7503 Readout System.

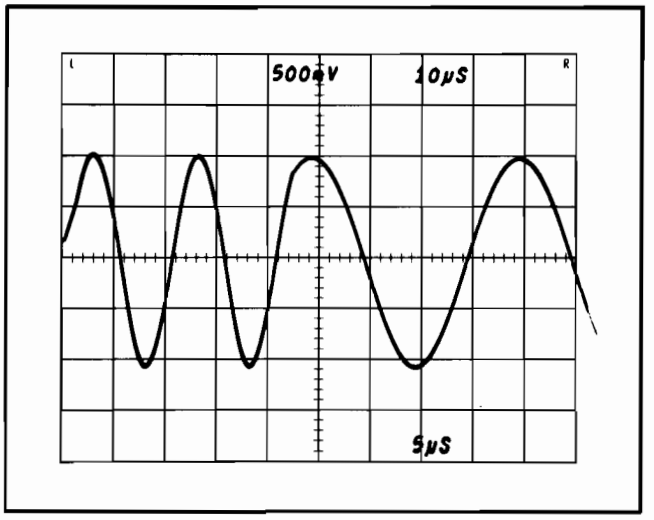


Fig. 3-32. Typical readout display where channel 1 of the Right Vertical unit and both channels of the Horizontal unit are displayed.

Developing the Display. The following basic description of the Readout System uses the block diagram shown in Fig. 3-33. This description is intended to relate the basic function of each stage to the operation of the overall Readout System. Detailed information on circuit operation is given later.

The key block in the Readout System is the Timer stage. This stage produces the basic signals which establish the timing sequences within the Readout System. Period of the timing signal is about 250 microseconds (drops to about 210 microseconds when Display-Skip is received; see detailed description of Timing stage for further information). This stage also produces control signals for other stages within this circuit and interrupt signals to the Vertical Interface and Horizontal Amplifier circuits, CRT Circuit, and Z-Axis Logic stage which allow a readout display to be presented. The Time-Slot Counter stage receives a trapezoidal voltage signal from the Timer stage and directs it to one of ten output lines. These output lines are labeled TS-1 through TS-10 (time-slots one through 10) and are connected to the vertical and horizontal plug-in compartments as well as to various stages within the Readout System. The output lines are energized sequentially so that there is a pulse on any one of the 10 lines during any 250 microsecond timing period. When the Time-Slot Counter stage has completed time-slot 10, it produces an End-of-Word pulse which advances the system to the next channel.

Two output lines, row and column, are connected from each plug-in channel back to the Readout System. Data is typically encoded on these output lines by connecting resistors between them and the time-slot input lines. The resultant output is a sequence of ten analog current levels which range from zero to one milliampere (100 microamperes/step) on the row and column output lines. This row and column correspond to the row and column of the Character Selection Matrix in Fig. 3-31. The standard format in which information is encoded onto the output lines is given in Table 3-2 (special purpose plug-in units may have their own format for readout; these special formats will be defined in the manuals for these units).

TABLE 3-2

Standard Readout Format

Time-Slot Number	Description
TS-1	Determines decimal magnitude (number of zeros displayed or prefix change information) or the IDENTIFY function (no display during this time-slot).
TS-2	Indicates normal or inverted input (no display for normal).
TS-3	Indicates calibrated or uncalibrated condition of plug-in variable control (no display for calibrated condition).
TS-4	1-2-5 scaling.
TS-5 TS-6 TS-7	Not encoded by plug-in unit. Left blank to allow addition of zeros by Readout System.
TS-8	Defines the prefix which modifies the units of measurement.
TS-9 TS-10	Define the units of measurement of the plug-in unit. May be standard units of measurement (V, A, S, etc.) or special units selected from the Character Selection Matrix.

The encoded column and row data from the plug-in units is selected by the Column Data Switch and Row Data Switch stages respectively. These stages take the analog currents from the eight data lines (two data lines from each of the three plug-in compartments and two unused) and produce a single time-multiplexed analog voltage output which contains all of the column or row information from the plug-ins. The Column Data Switch and Row Data Switch are sequenced by the binary Channel Address Code from the Channel Counter.

The time multiplexed output of the Column Data Switch is monitored by the Display-Skip Generator to

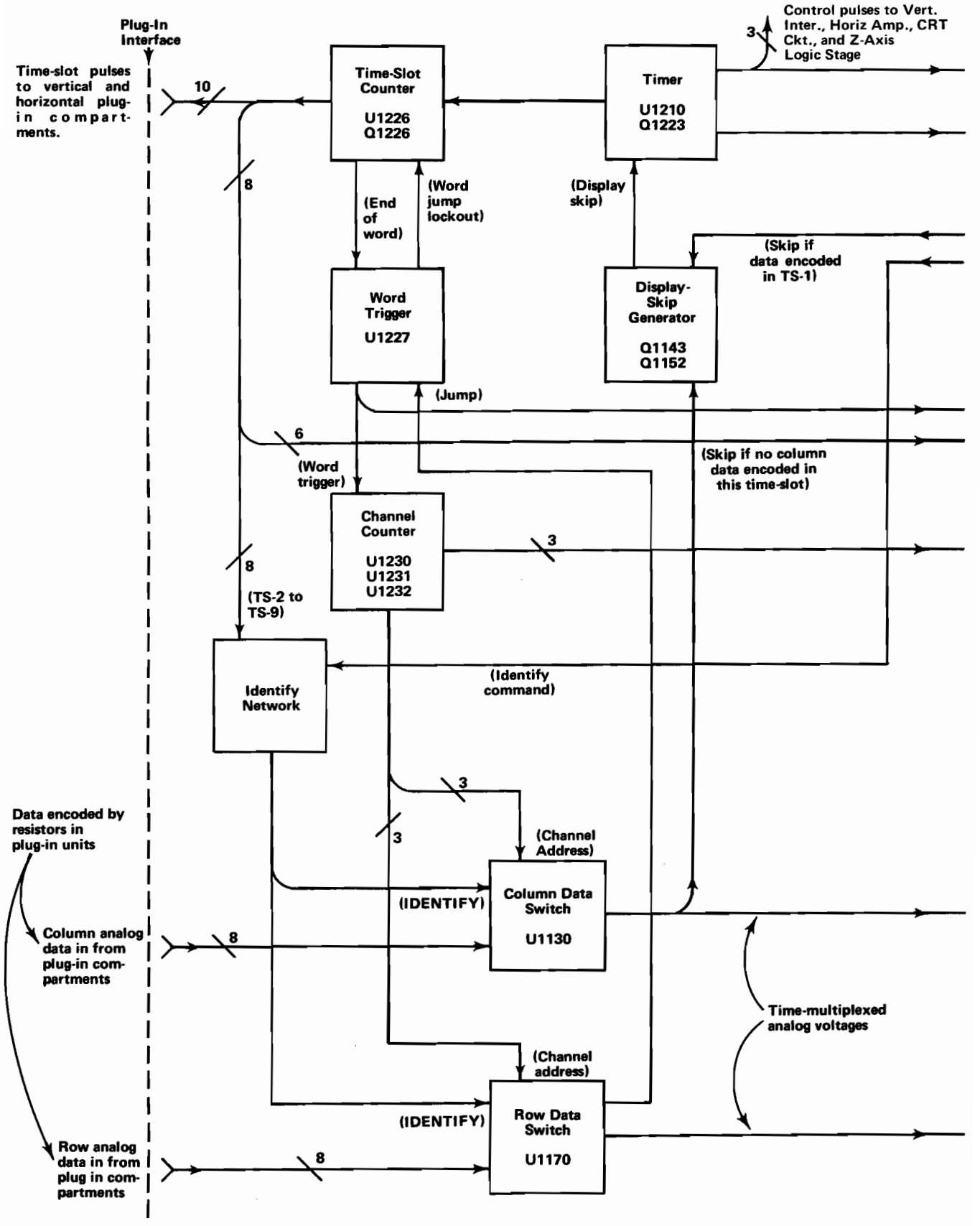


Fig. 3-33. Detailed block diagram of Readout System.

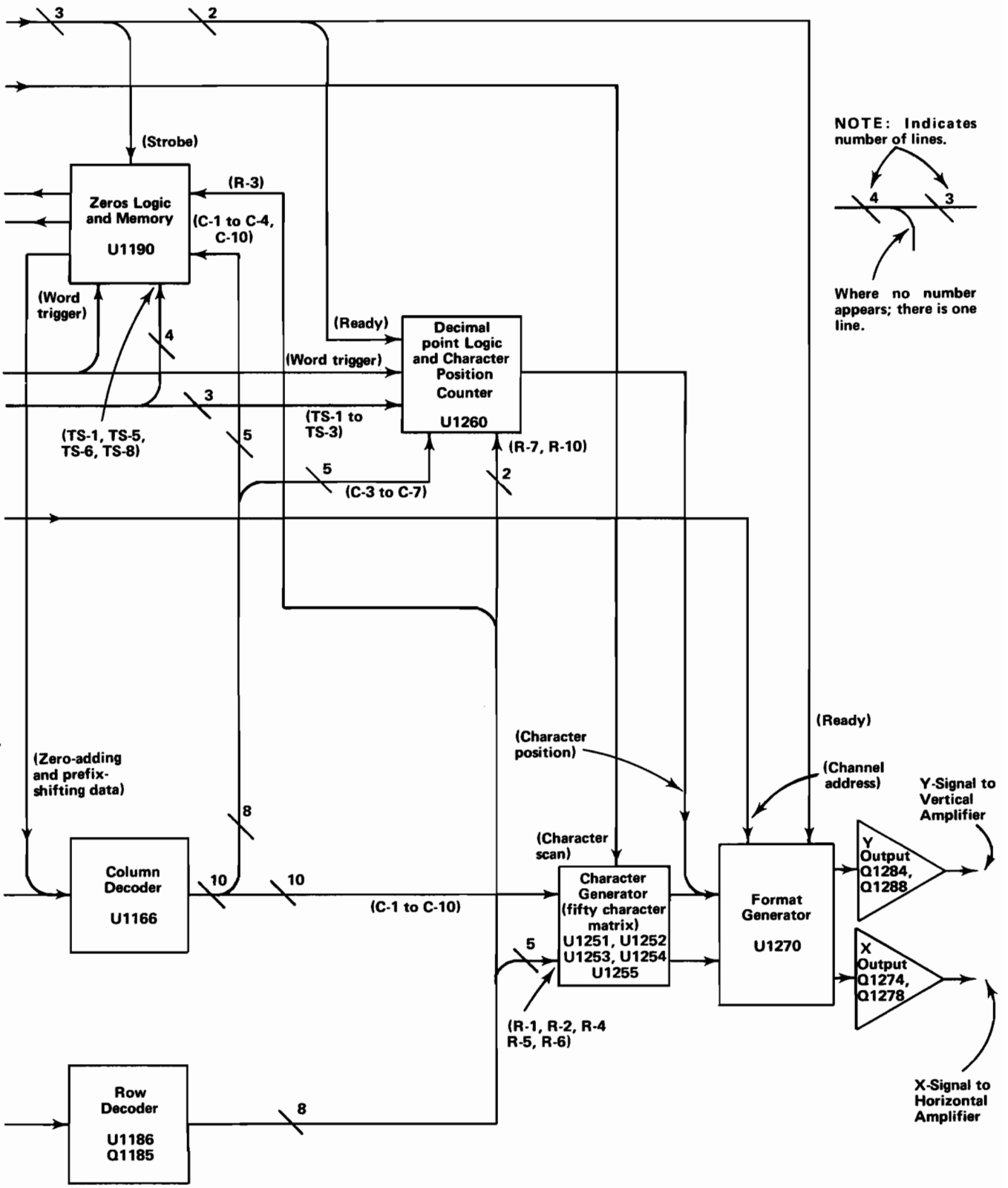


Fig. 3-33. Detailed block diagram of Readout System.

determine if it represents valid information which should be displayed. Whenever information is not encoded in a time-slot, the Display-Skip Generator produces an output level to prevent the Timer stage from producing the control signals which normally interrupt the CRT display and present a character.

The analog output of the Column Data Switch and Row Data Switch are connected to the Column Decoder and Row Decoder stages respectively. These stages sense the magnitude of the analog voltage input and produce an output current on one of ten lines. The outputs of the Column Decoder stage are identified as C-1 to C-10 (column 1 to 10) which correspond to the column information encoded by the plug-in unit. Likewise, the outputs of the Row Decoder stage are identified as R-1 to R-10 (row 1 to 10) which correspond to the row information encoded by the plug-in unit. The primary function of the row and column outputs is to select a character from the Character Selection Matrix to be produced by the Character Generator stage. However, these outputs are also used at other points within the system to indicate when certain information has been encoded. One such stage is the Zeros Logic and Memory. During time-slot 1 (TS-1), this stage checks if zero-adding or prefix-shifting information has been encoded by the plug-in unit and stores it in memory until time-slots 5, 6 or 8. After storing this information, it triggers the Display-Skip Generator stage so there is no display during this time slot (as defined by Standard Readout Format; see Table 3-2). When time-slots 5, 6 and 8 occur, the memory is addressed and any information stored there during time-slot 1 is transferred out and connected to the input of the Column Decoder stage to modify the analog data during the applicable time-slot.

Another operation of the Zeros Logic and Memory stage is to produce the IDENTIFY function. When time-slot 1 is encoded for IDENTIFY (column 10, row 3), this stage produces an output level which connects the Column Data Switch and Row Data Switch to a coding network within the Readout System. Then, during time-slots 2 through 9, an analog current output is produced from the Column Data Switch and Row Data Switch which addresses the correct points in the Character Selection Matrix to display the word "IDENTIFY" on the CRT. The Zeros Logic and Memory stage is reset after each word by the Word Trigger pulse.

The Character Generator stage produces the characters which are displayed on the CRT. Any of the 50 characters shown on the Character Selection Matrix of Fig. 3-31 can be addressed by proper selection of the column and row current. Only one character is addressable in any one time-slot; a space can be added into the displayed word by the Decimal Point Logic and Character Position Counter stage when encoded by the plug-in. The latter stage counts how many characters have been generated and produces an output current to step the display one character position to the right for each character. In addition, the character position is advanced once during each of time-slots 1, 2 and 3 whether a character is generated during these time-slots or not. This action fixes the starting point of the standard-format display such that the first digit of the scaling factor always starts at the same point within each word regardless of the encoded information in time-slot 2 (normal/invert) or time-slot 3 (cal/uncal) which precedes this digit. Also, by encoding row 10 and column 0 during any time-slot, a blank space can be added to the display. Decimal points can be added to the display at any time by addressing row 7 and columns 3 through 7 (see Character Selection Matrix for location of these decimal points). The Decimal Point Logic and Character Position Counter stage is reset after each word by the Word Trigger pulse.

The Format Generator stage provides the output signals to the vertical and horizontal deflection systems of the instrument to produce the character display. The binary Channel Address Code from the Channel Counter stage is connected to this stage so that the display from each channel is positioned to the area of the CRT which is associated with the plug-in and channel originating the word (see Fig. 3-30). The positioning current or decimal point location current generated by the Decimal Point Logic and Character Position Counter stage is added to the horizontal (X) signal at the input to the Format Generator stage to provide horizontal positioning of the characters within each word. The X- and Y-output signals are connected to the Horizontal Amplifier and Vertical Amplifier through the Horizontal Output and Vertical Output Stages respectively.

The Word Trigger stage produces a trigger from the End-of-Word pulse generated by the Time-Slot Counter stage after the tenth time-slot. This Word Trigger pulse advances the Channel Counter to display the information from the next channel or plug-in. It also provides a reset pulse to the Zeros Logic and Memory stage and the Decimal Point Logic and Character Position Counter stage. The Word Trigger stage can also be advanced to jump a complete word or a portion of a word when a Jump command is received from the Row Decoder stage.

Circuit Analysis of Readout System

The following analysis of the Readout System discusses the operation of each stage in detail. Complete schematics of the Readout System are shown on diagrams 10, 11 and 12 at the rear of this manual.

Timer

The Timer stage U1210 establishes the timing sequence for all circuits within the Readout System. This stage produces seven time-related output waveforms (see Fig. 3-34). The triangle waveform produced at pin 6 forms the basis for the remaining signals. The basic period of this triangle waveform is about 250 microseconds as controlled

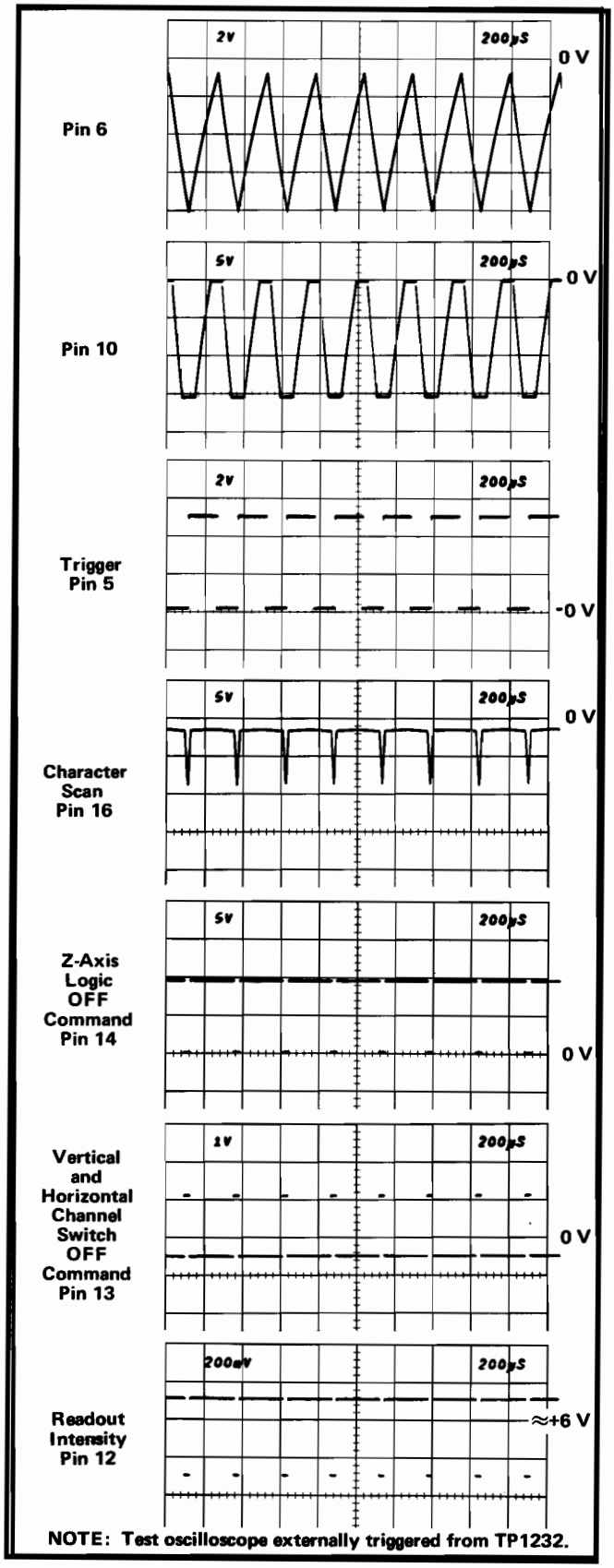


Fig. 3-34. Output waveforms of Timer stage.

by RC network C1214-R1214. The triangle waveform is clipped and amplified by U1210 to form the trapezoidal output signal at pin 10. The amplitude of this output signal is exactly 15 volts as determined by U1210 (exact amplitude necessary to accurately encode data; see Encoding the Data). The Trigger output at pin 5 provides the switching signal for the Time-Slot Counter and Word Trigger stages.

The signals at pins 12, 13, 14 and 16 are produced only when the triangle waveform is on its negative slope and the trapezoidal waveform has reached the lower level. The timing sequence of these waveforms is very important to the correct operation of the Readout System (see expanded waveforms in Fig. 3-35). The Z-Axis Logic OFF Command at pin 14 is produced first. This negative-going signal provides a blanking pulse to the Z-Axis Logic stage (see diagram 1) to blank the CRT before the display is switched to the Readout System. It also produces the Strobe pulse through R1221, Q1223 and CR1224 to signal other stages within the Readout System to begin the sequence necessary to produce a character. The collector level of Q1223 is also connected to Character Generator #2, U1252, through C1222-CR1222. This activates U1252 during the quiescent period of the Strobe pulse (collector of Q1223 negative) and diverts the output current of the Row Decoder stage U1186 to row 2. The purpose of this configuration is to prevent the Zeros Logic and Memory stage U1190 from storing incorrect data during the quiescent period of the Strobe pulse. When the Strobe pulse goes positive, CR122 is reverse biased to disconnect Q1223 from U1252 and allow the Row Decoder stage to operate in the normal manner.

The next signal to be produced is the Vertical/Horizontal Channel Switch OFF Command at pin 13. This positive-going signal disconnects the plug-in signals in the vertical and horizontal deflection systems so the plug-ins do not control the position of the CRT beam. The Ready signal derived from this output is connected to the Decimal Point Logic and Character Position Counter stage and the Format Generator stage (see diagram 12). The Readout Intensity output at pin 12 is produced next. This current is connected to the Z-Axis Intensity circuit to unblank the CRT to the level determined by the READOUT intensity control R1040. The Character Scan ramp at pin 16 started to go negative before this timing sequence began. However, character-generation does not start until the readout intensity level has been established. The triangular Character Scan ramp runs negatively from about −2 volts to about −8.5 volts and then returns back to the original level. This waveform provides the scanning signal for the Character Generator stages (see diagram 12). The Character Scan adjustment R1219 sets the DC level of the Character Scan ramp to provide complete characters on the display.

The Timer stage operates in one of two modes as controlled by the Display-Skip level at pin 4. The basic

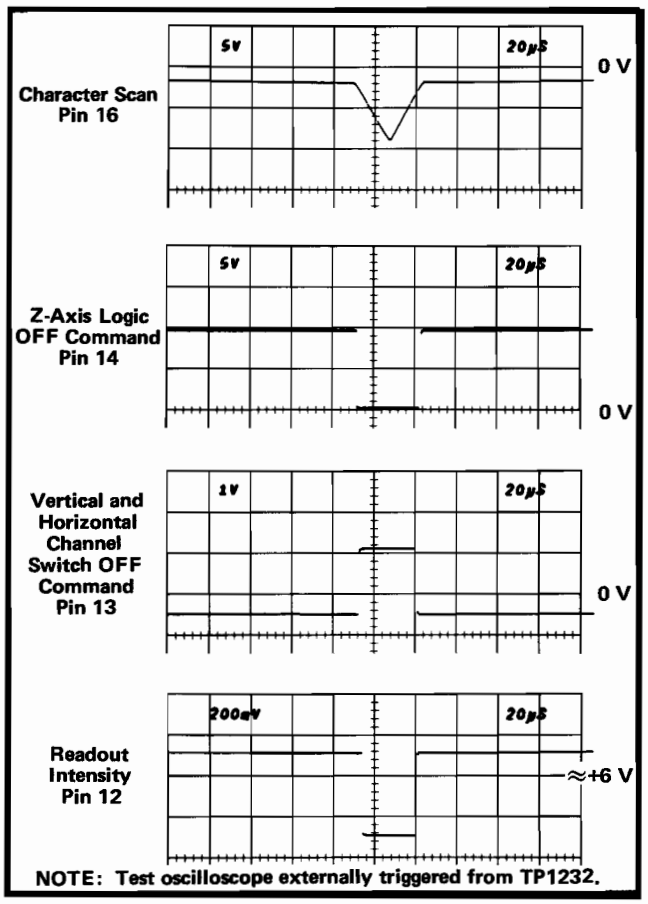


Fig. 3-35. Detail of output at pins 12, 13, 14 and 16 of U1210.

mode just described is a condition which does not occur unless all ten characters of each word (80 characters total) are displayed on the CRT. Under typical conditions only a few characters are displayed in each word. The Display-Skip level at pin 4 determines the period of the Timer output signal. When a character is to be generated, pin 4 is LO and the circuit operates as just described. However, when a character is not to be displayed, a HI level is applied to pin 4 of U1210 through CR1207 from the Display-Skip Generator stage (diagram 11). This signal causes the Timer stage to shorten its period of operation to about 210 microseconds. The waveforms shown in Fig. 3-36 show the operation of the Timer stage when the Display-Skip condition occurs for all positions in a word. Notice that there is no output at pin 12, 13, 14 and 16 under this condition. This means that the CRT display is not interrupted to display characters. Also notice that the triangle waveform at pin 6 does not go as far negative and that the negative portion of the trapezoidal waveform at pin 10 is shorter. Complete details on operation of the Display-Skip Generator are given later.

The READOUT intensity control R1040 sets the intensity of the readout display independently of the

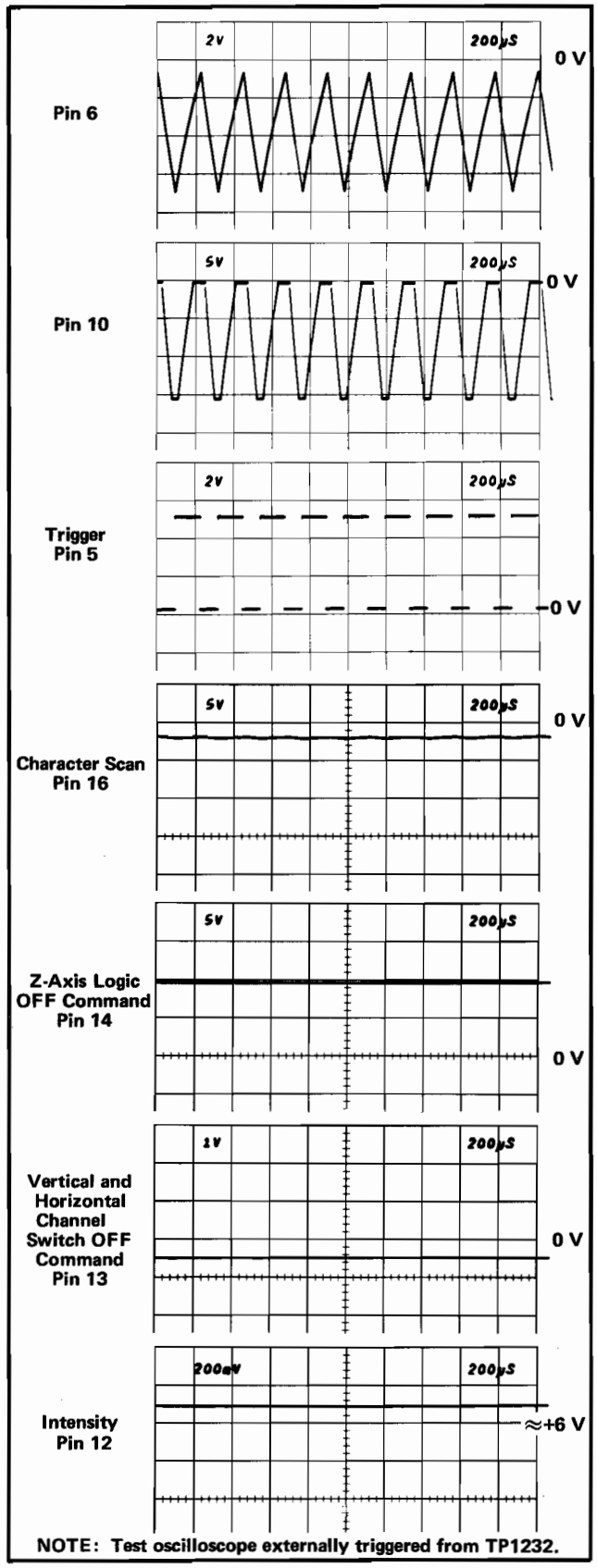


Fig. 3-36. Timer stage operation when Display-Skip condition occurs.

INTENSITY control. The READOUT intensity control also provides a means of turning the Readout System off when a readout display is not desired. When R1040 is turned fully counterclockwise, switch S1040A opens. This interrupts the current to pin 11 of U1210 and at the same time allows a positive voltage to be applied to pin 4 through R1206 and CR1206. This positive voltage switches the stage to the same conditions as were present under the Display-Skip condition. Therefore, the CRT display is not interrupted to present characters. However, time-slot pulses continue to be generated.

Time-Slot Counter

The Time-Slot Counter stage U1226 is a sequential switch which directs the trapezoidal waveform input at pin 8 to one of its ten output lines. These time-slot pulses are used to interrogate the plug-in units to obtain data for the Readout System. The Trigger pulse at pin 15 switches the Time-Slot Counter to the next output line; the output signal is sequenced from time-slot 1 through time-slot 10. Fig. 3-37 shows the time-relationship of the time-slot pulses. Notice that only one of the lines carries a time-slot pulse at any given time. When time-slot 10 is completed, a negative-going End-of-Word pulse is produced at pin 2. The End-of-Word pulse provides a drive pulse for the Word Trigger stage and also provides an enabling level to the Display-Skip Generator during time-slot 1.

Pin 16 is a reset input for the Time-Slot Counter stage. When this pin is held LO, the Time-Slot Counter resets to time-slot 1. The Time-Slot Counter can be reset in this manner only when a Jump signal is received by U1227A (see following discussion).

Word Trigger

The Word Trigger stage is made up of 4 two-input NOR gates in U1227. Quiescently, pin 2 of U1227C is LO as established by the operating conditions of U1227A-U1227B. Therefore, the LO End-of-Word pulse produced by the Time-Slot Counter stage results in a HI level at pin 1 of U1227C. This level is inverted by U1227D to provide a negative-going advance pulse to the Channel Counter stage.

A negative-going advance pulse is also produced by U1227D when a Jump signal is received at pin 8 of U1227A. This condition can occur during any time slot (see Row Decoder for further information on origin of the Jump signal). U1227A and U1227B are connected as a bistable flip-flop. The positive-going Jump signal at pin 8 of U1227A produces a LO level at pin 10. This LO level is inverted by U1227B to produce a HI level at pin 13 which allows pin 9 of U1227A to be pulled HI through R1227. The flip-flop has now been set to its HI state where it remains until reset, even though the Jump signal at pin 8 returns to its LO level. The HI output level at pin 13 turns on Q1226 through R1226 to pull pin 16 of the Time-Slot Counter LO. This resets the Time-Slot Counter to time-slot

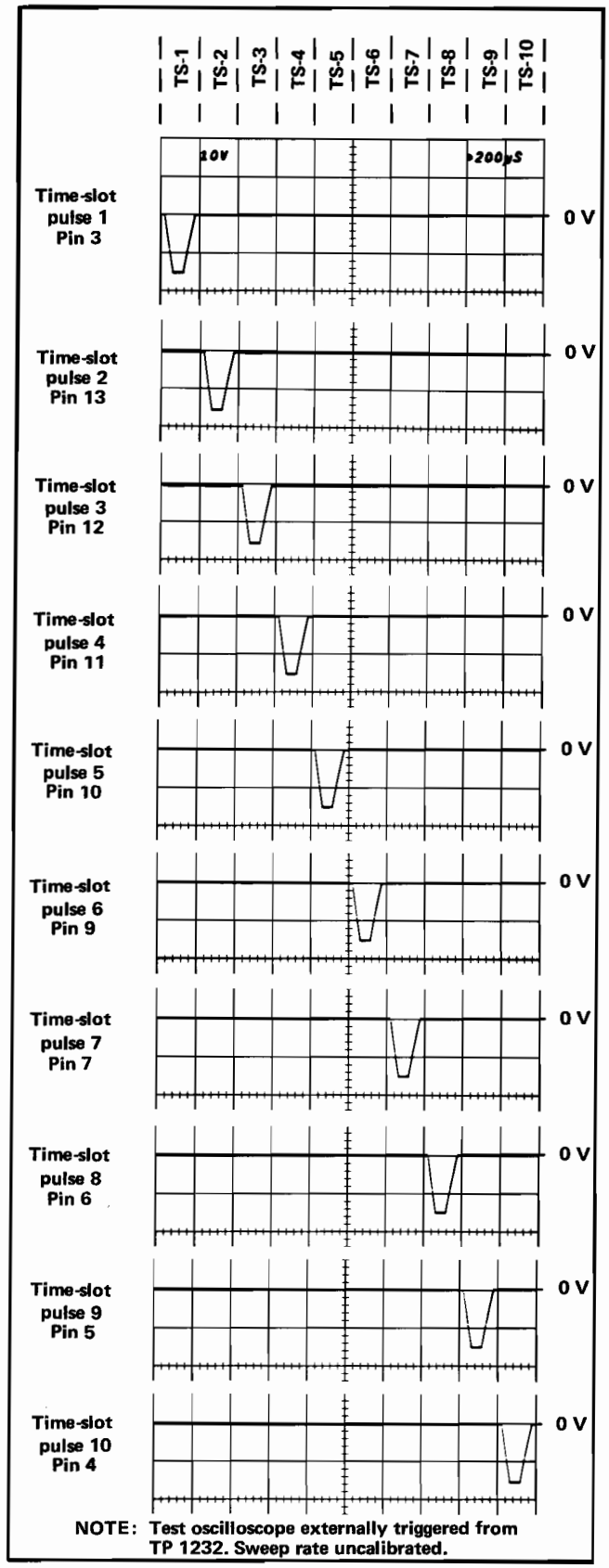


Fig. 3-37. Time relationship of the time-slot (TS) pulses produced by U1226.

1 and holds it there until U1227 is reset. At the same time, a HI level is applied to pin 4 of the Timer stage through CR1208 and CR1207. This HI level causes the Timer stage to operate in the display-skip mode so that a character is not generated.

The next Trigger pulse is not recognized by the Time-Slot Counter stage, since it is held in Time-Slot 1 by U1227. However, this trigger pulse resets the Word Trigger stage through C1227. This produces a LO level at pin 13 of U1227B which enables the Time-Slot Counter and Timer stages for the next time-slot pulse. At the same time, the negative-going edge produced as U1227B switches output states is connected to pin 2 of U1227C. This results in a negative-going Word Trigger output at pin 4 of U1227D to advance the Channel Counter to the next word. When the next Trigger pulse is received at pin 15, the Time-Slot Counter produces an output on the time-slot 1 line.

Channel Counter

The Channel Counter stage made up of integrated circuits U1230, U1231 and U1232 is a binary counter which produces the Channel Address Code for the Column and Row Decoder stages (diagram 11) and the Format Generator stage (diagram 12). This code instructs these stages to sequentially select and display the eight channels of data from the plug-ins (two channels unused). The input channel which is displayed with each combination of the Channel Address Code is given in the discussion for the applicable stages.

Encoding the Data

Data is conveyed from the plug-in unit to the Readout System in the form of an analog code having up to 11 current levels (from zero to one milliampere in 100 microampere steps). The characters which can be selected by the encoded data are shown on the Character Selection Matrix (see Fig. 3-31). Each character requires two currents to define it; these currents are identified as the column current and the row current which correspond to the column and row of the matrix. The column and row data is encoded by resistive programming in the plug-in units. Fig. 3-38 shows a typical encoding scheme for a voltage-sensing amplifier plug-in unit. Notice that the 10 time-slot (TS)

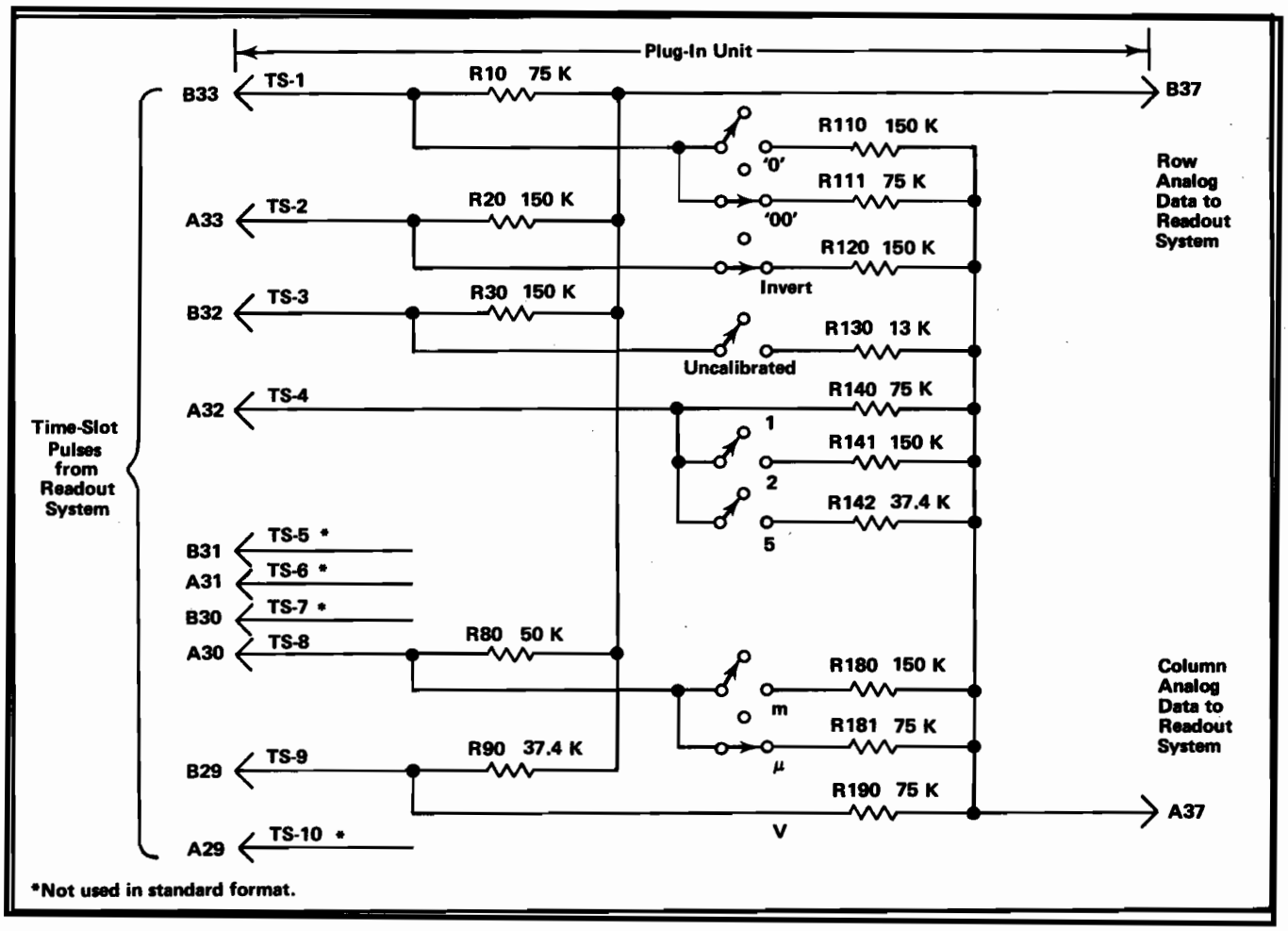


Fig. 3-38. Typical encoding scheme for voltage-sensing plug-in unit. Coding shown for deflection factor of 100 microvolts.

pulses produced by the Time-Slot Counter stage are connected to the plug-in unit. However, time-slots 5, 6, 7 and 10 are not used by the plug-in unit to encode data when using the Standard Readout Format (see Table 3-2 for Standard Readout Format). The amplitude of the time-slot pulses is exactly −15 volts as determined by the Timer stage. Therefore, the resultant output current from the plug-in units can be accurately controlled by the programming resistors in the plug-in units.

For example, in Fig. 3-38, resistors R10 through R90 control the row analog data which is connected back to the Readout System. These resistors are of fixed value and define the format in which the information will be presented by the Readout System. Fig. 3-39A shows an idealized output current waveform of row analog data which results from the 10 time-slot pulses. Each of the steps of current shown in these waveforms corresponds to 100 microamperes of current. The row numbers on the left-hand side of the waveform correspond to the rows in the Character Selection Matrix shown in Fig. 3-31. The row analog data is connected back to the Readout System via terminal B37 of the plug-in interface.

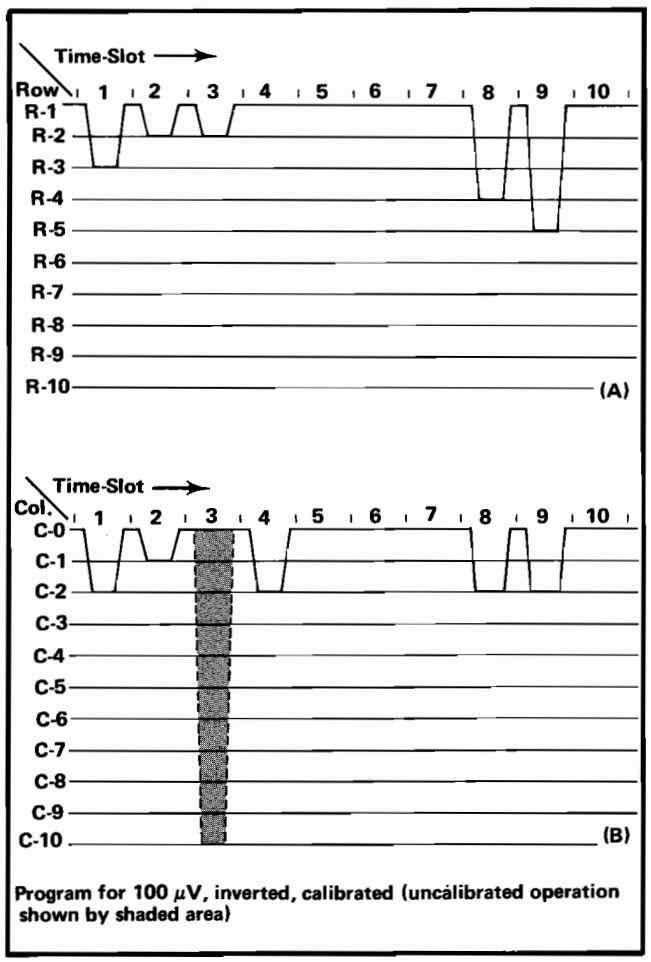


Fig. 3-39. Idealized current waveforms of: (A) Row analog data, (B) Column analog data.

The Column analog data is defined by resistors R110 through R190. The program resistors are connected to the time-slot lines by switch closures to encode the desired data. The data as encoded by the circuit shown in Fig. 3-38 indicates a 100 microvolt sensitivity with the display inverted and calibrated vertical deflection factors. This results in the idealized output current waveforms shown in Fig. 3-39B at the column analog data output, terminal A37 of the plug-in interface. Resistor R111, connected between time-slot 1 and the column analog data output encodes two units of current during time-slot 1. Referring to the Character Selection Matrix, two units of column current along with the two units of row current encoded by R10 (row 3) indicates that two zeros should be added to the display. Resistor R120 adds one unit of column current during time-slot 2 and along with the one unit of current from the row output, the Readout System is instructed to add an invert arrow to the display. R130 is not connected to the time-slot 3 line since the vertical deflection factors are calibrated. Therefore, there is no column current output during this time-slot and there is no display on the CRT (see Display-Skip Generator for further information). During time-slot 4, two units of column current are encoded by R140. There is no row current encoded during this time-slot and this results in the numeral 1 being displayed on the CRT. Neither row nor column analog data is encoded during time-slots 5, 6 and 7 as defined by the Standard Readout Format. During time-slot 8, two units of column current and three units of row current are encoded by resistors R181 and R80 respectively. This addresses the μ prefix in the Character Selection Matrix. The final data output is provided from time-slot 9 by R190 connected to the column output and R90 to the row output. These resistors encode three units of column current and four units of row current to cause a V (volts) to be displayed. Time-slot 10 is not encoded in accordance with the Standard Readout Format. The resultant CRT readout will be ↓ 100 μV.

In the above example, the row analog data was programmed to define which row of the Character Selection Matrix was addressed to obtain information in each time-slot. The column data changes to encode the applicable readout data as the operating conditions change. For example, if the variable control of the plug-in unit was activated, R130 would be connected between time-slot 3 and the column analog data output lines. This encodes 10 units of column current (see shaded area in time-slot 3 of the waveform shown in Fig. 3-39B). Since one unit of row current is also encoded during this time-slot by R30, a > symbol is added to the display. The CRT readout will now say ↓ > 100 μV. In a similar manner, the other switches can change the encoded data for the column output and thereby change the readout display. For information on decoding this information, see the descriptions which follow.

The column analog data encoded by the plug-in can be modified by attenuator probes connected to the input

connectors of vertical plug-in units. A special coding ring around the input connector of the plug-in unit senses the attenuation ratio of the probe (with readout-coded probes only). The probe contains a resistor which results in additional column current. For example, if a 10X attenuator probe is connected to a plug-in with the coding for 100 microvolts as shown in Fig. 3-38, an additional unit of current is added to the column analog data during time-slot 1. Since two units of current were encoded by R111 (see Fig. 3-38), this additional current results in a total of three units of column analog current during this time-slot. Referring to the Character Selection Matrix, three units of column current along with the two units of row current encoded by R10 indicates that the prefix should be reduced. Since this instruction occurs in the same time-slot which previously indicated that two zeros should be added to the display and only one instruction can be encoded during a time-slot, the zeros do not appear in the display. The CRT readout will now be reduced to 1 mV (readout program produced by plug-in same as for previous example).

Likewise, if a 100X readout-coded probe is connected to the input of the plug-in unit, the column current during time-slot 1 will be increased two units for a total of four units of column current. This addresses an instruction in the Character Selection Matrix which reduces the prefix and adds one zero to the display. The resultant CRT readout with the previous program is 10 mV.

Three other lines of information are connected from the plug-in compartments to the Readout System. The column and row analog data from channel 2 of a dual-channel plug-in are connected to the Readout System through terminals A38 and B38 of the plug-in interface, respectively. Force readout information is encoded on terminal A35; function of this input is described under Column and Row data Switches.

The preceding information gave a typical example of encoding data from an amplifier plug-in unit. Specific encoding data and circuitry is shown in the individual plug-in unit manuals.

Column and Row Data Switches

The readout data from the plug-in units is connected to the Column and Row Data Switch stages in the Readout System. A column-data line and a row-data line convey analog data from each of the eight data sources. The Readout System is designed to display data from four plug-ins; thus eight data sources are possible. Since the 7503 accommodates three plug-ins, only six data sources are connected to the Readout System. The Readout System operates the same as it would in a four plug-in oscilloscope with one plug-in not being operated.

The Column Data Switch U1130 and the Row Data Switch U1170 receive the Channel Address Code from the Channel Counter stage. This binary code directs the Column Data Switch and the Row Data Switch as to which channel should be the source of the readout data. Table 3-3 gives the eight combinations of the Channel-Address-Code and the resultant channel which is selected with each combination. These stages have nine inputs and provide a single time-multiplexed output at pin 7 which includes the information from all of the input channels. Eight of the nine inputs to each stage originate in the plug-in units and the ninth input comes from a special data-encoding network composed of resistors R1131 through R1138 and R1171 through R1178 (see Zeros Logic and Memory description for further information on ninth channel).

TABLE 3-3

Channel Address Code to Column and Row Decoder Stages

Pin 1 U1190 "Identify" Command	Pin 5 U1232	Pin 5 U1231	Pin 5 U1230	Channel Selected
HI	HI	HI	HI	Channel 1 Left Vertical
HI	HI	HI	LO	Channel 2 Left Vertical
HI	HI	LO	HI	Channel 1 Right Vertical
HI	HI	LO	LO	Channel 2 Right Vertical
HI	LO	HI	HI	Channel 1 Horizontal
HI	LO	HI	LO	Channel 2 Horizontal
HI	LO	LO	HI	Channel 1 Unused
HI	LO	LO	LO	Channel 2 Unused
LO	Φ	Φ	Φ	IDENTIFY

Φ = Has no effect in this case.

In addition to the data inputs from the plug-ins, channel-inhibit inputs are provided from each of the plug-in units. The channel inhibit lines are LO only when the associated plug-in unit has been selected for display. When a plug-in unit is not selected, the respective line is HI which forward biases the associated diode CR1112, CR1113, CR1117, CR1118, CR1122, CR1123, CR1127 or CR1128 to by-pass the encoded data from this plug-in. Notice that the channel inhibit line for the fourth (unused) plug-in is connected to

+5-V to inhibit that channel of information. However, since it may be desired to display information from special-purpose plug-ins even though they do not produce a normal display on the CRT, a feature is provided to over-ride the channel inhibit. This is done by applying a LO level to the associated Force over-ride input. The LO level diverts the HI channel inhibit current and allows the data from this plug-in unit to reach the Column Data switch, even though it has not been selected for display by the mode switches.

Display-Skip Generator

The Display-Skip Generator stage, Q1143-Q1150-Q1152- Q1155, monitors the time-multiplexed column data at the output of the Column Data Switch during each time-slot to determine if the information at this point is valid data which should result in a CRT display. The base of Q1143B is fixed at about +14.25 volts by divider R1146-R1147-R1148. Quiescently, there is about 100 microamperes of current flowing through R1141 from Q1163 and the Zeros Logic and Memory stage (purpose of this quiescent current will be discussed in connection with the Zeros Logic and Memory stage). This current biases Q1143A so its base is at about +14.5 volts in the absence of column data. Therefore, since Q1143A and Q1143B are connected as a comparator, Q1143A will remain on unless its base is pulled more negative than about +14.25 volts. The analog data output from the Column Data Switch produces a 0.5-volt change for each unit of column current that has been encoded by the plug-in. Therefore, whenever any information appears at the output of the Column Data Switch, the base of Q1143A is pulled more negative than the base of Q1143B, resulting in a negative (LO) Display-Skip output to the Timer stage through Q1155. Recall that a LO was necessary at the skip input of the Timer stage so that the Timer stage could perform the complete sequence necessary to display a character.

Q1150-Q1152 also provide display-skip action. The End-of-Word level that is connected to their emitters through R1152 is LO only during time-slot 1. This means that these transistors are only enabled during this time-slot period. These transistors allow the Zeros Logic and Memory stage to generate a display-skip signal when information has been stored in memory which is not to be displayed on the CRT (further information given under Zeros Logic and Memory discussion).

Column and Row Decoder

The Column Decoder stage U1166 and Row Decoder stage U1186 sense the magnitude of the analog voltages at their inputs and produce a binary output on one of ten lines corresponding to the column or row data which was encoded by the plug-in. These outputs provide the Column Digital Data and Row Digital Data which is used by the Character Generator stages to select the desired character for display on the CRT. The column and row data is also used throughout the Readout System to perform other functions. The input current at pin 9 of the Column Decoder stage is steered to only one of the ten Column Digital Data outputs. The size of the character which will be displayed on the CRT is determined by the value of R1156. When a display-skip signal is present (collector of Q1155 HI), pin 9 is pulled HI through CR1155. This ensures that no current is connected to the Character Generator stage under this condition. Notice the corresponding input on the Row Decoder. This input is connected to ground and causes only one of the ten row outputs to saturate to ground.

The network at the input of the Row Decoder stage made up of Q1185 and its associated components is a Row 13 detector which produces the Jump command. This row current is encoded by special-purpose plug-ins to cause all or part of a word to be jumped. Whenever row 13 (thirteen units of row current; 1.3 milliamperes) is encoded, the base of Q1185 is pulled negative enough so that this transistor is reverse biased to produce a HI Jump output at its collector. This Jump command is connected to the Word Trigger stage (diagram 10) to advance the Channel Counter stage to the next word and to reset the Time-Slot Counter stage to time-slot 1.

Zeros Logic and Memory

The Zeros Logic and Memory stage U1190 stores data encoded by the plug-ins to provide zeros-adding and prefix-shifting logic for the Readout System. The Strobe pulse at pin 15 goes positive when the data has stabilized and can be inspected. This activates the Zeros Logic and Memory stage so it can store the encoded data. A block representation of the memory sequence is shown in Fig. 3-40. Typical output waveforms for the five possible input conditions that can occur are shown in Fig. 3-41. When time-slot 1 occurs, a store command is given to all of the memories. If the plug-in unit encoded data for column 1, 2, 3, 4 and 10 during time-slot 1, the appropriate memory (or memories) is set. Notice that row 3 information from the Row Decoder stage must also be present at pin 16 for data to be stored in the memory of U1190. If data was encoded during time-slot 1, a negative-going output is produced at pin 7 as the memories are being set. This negative-going pulse is connected to the base of Q1152 in the Display-Skip Generator stage to produce a Display-Skip output. Since the information that was encoded during time-slot 1 was only provided to set the memories and was not intended to be displayed on the CRT at this time, the display-skip output prevents a readout display during this time-slot.

During time-slot 5, memory A is interrogated. If information was stored in this memory, a positive-going output is produced at pin 7. This pulse is connected to pin 10 of the Column Decoder stage through Q1163 to add one unit of current at the input of the Column Decoder stage. This produces a zero after the character displayed on the CRT during time-slot 4. During time-slot 6, memory B is interro-

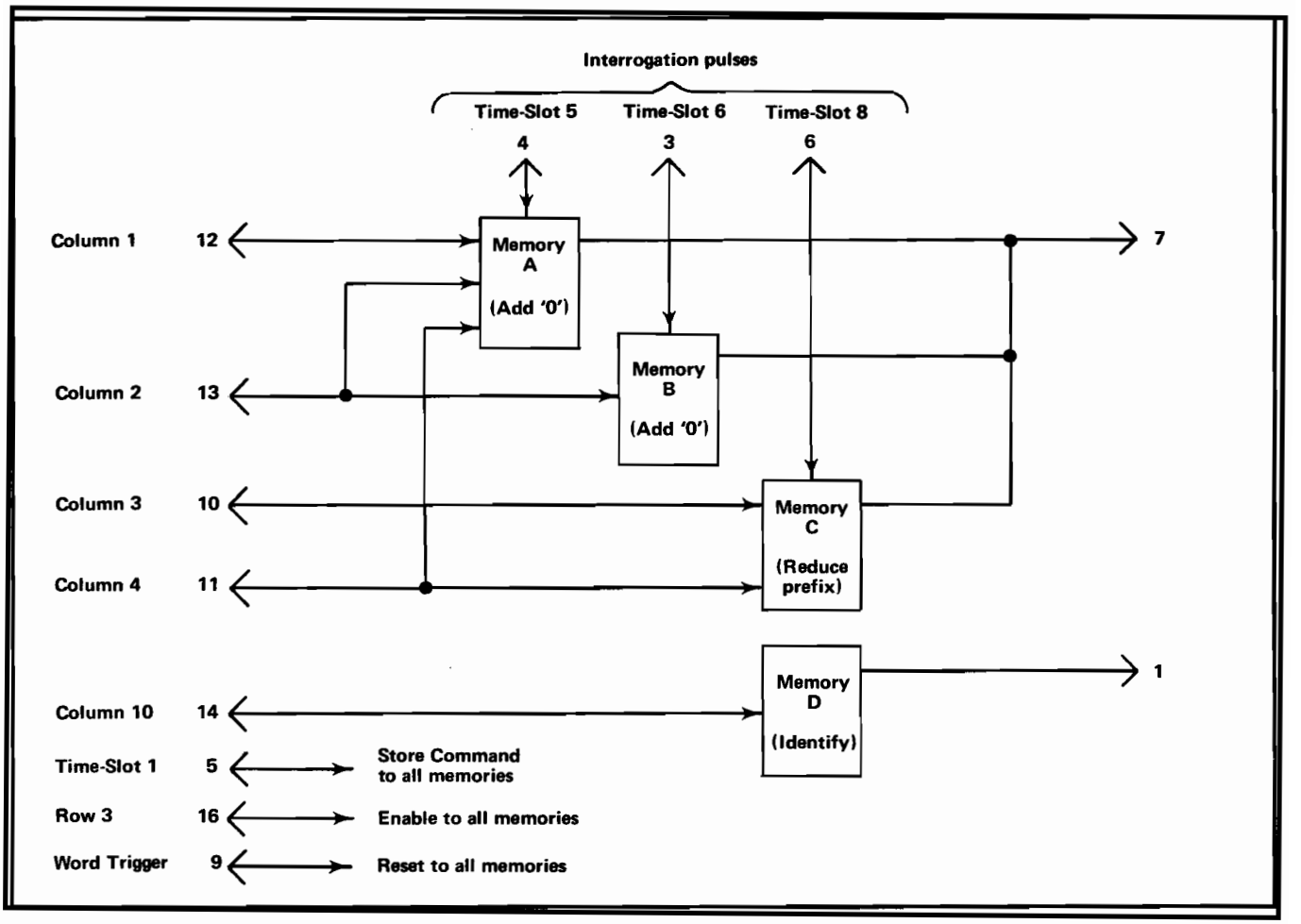


Fig. 3-40. Block representation of memory sequence in U1190.

gated to see if another zero should be added. If another zero is necessary, a second positive output is produced at pin 7 which again results in a column 1 output from the Column Decoder stage and a second zero in the CRT display.

Finally, memory C is interrogated during time-slot 8 to obtain information on whether the prefix should be reduced or left at the value which was encoded. If data has been encoded which calls for a reduction in prefix, a negative-going output level is produced at pin 7. This negative level subtracts one unit of column current from the data at the input to the Column Decoder stage. Notice on the Character Selection Matrix of Fig. 3-31 that a reduction of one column when row 4 is programmed results in a one unit reduction of the prefix. For example, with the 100 μV program shown in Fig. 3-38, if the data received from the plug-in called for a reduction in prefix the CRT readout would be changed to 1 mV (zeros deleted by program; see Encoding the Data).

The 100 microamperes of quiescent current through R1141 that was provided by Q1163 (see Display-Skip Generator) allows the prefix to be reduced from m (100 microamperes column current; column 1) to no prefix (zero column current; column zero) so only the unit of measurement encoded during time-slot 9 is displayed. Notice that reducing the prefix program from column 1 to column 0 programs the Readout System to not display a character at this readout location.

A further feature of the Zeros Logic and Memory stage is the Identify function. If 10 units of column current are encoded by the plug-in unit along with row 3 during time-slot 1, the Zeros Logic and Memory stage produces a negative-going output pulse at pin 1 which switches the Column Data Switch and Row Data Switch stages to the ninth channel. Then, time-slot pulses 2 through 9 encode an output current through resistors R1131-R1138 for column data and R1171-R1178 for row data. This provides the currents necessary to display the word IDENTIFY on the CRT in the word position allotted to the channel which originated the Identify command. After completion of this word, the Column Data Switch and Row Data Switch continue with the next word in sequence.

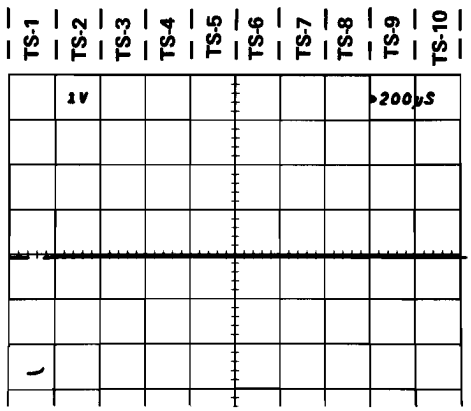
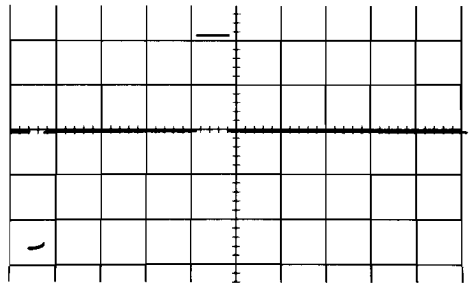
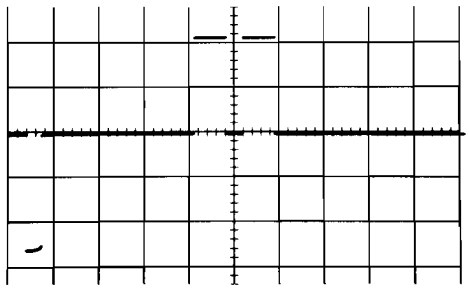
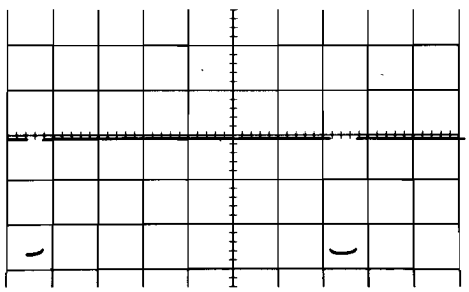
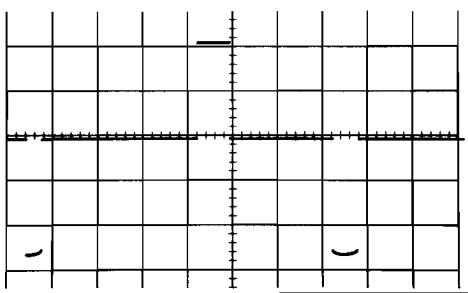
Input Pin of U1190 Activated	Command	Time-Slots
14	IDENTIFY	 0 V
12	Add one zero	 0 V
13	Add two zeros	 0 V
10	Decrease prefix	 0 V
11	Decrease prefix and add one zero	 0 V

Fig. 3-41. Typical output waveforms for Zeros Logic and Memory stage operation (at pin 7 of U1190).

The Word Trigger signal from the Word Trigger stage is connected to pin 9 of U1190 through C1190. At the end of each word of readout information, this pulse goes low. This erases the four memories in the Zeros Logic and Memory stage in preparation for the data to be received from the next channel.

Character Generators

The Character Generator stage consists of five similar integrated circuits U1251-U1255 which produce the X (horizontal) and Y (vertical) outputs at pins 16 and 1 respectively to produce the character displayed on the CRT. Each integrated circuit can produce 10 individual characters. U1251, which is designated as the "Numerals" Character Generator, can produce the numerals 0 through 9 shown in row 1 of the Character Selection Matrix (Fig. 3-31). U1252 can produce the symbols shown in row 2 of the Character Selection Matrix and U1253 produces the prefixes and some letters of the alphabet which are used as prefixes in row 4. U1254 and U1255 produce the remaining letters of the alphabet shown in rows 5 and 6 of the Character Selection Matrix. All of these stages receive the column digital data from the Column Decoder stage U1166 in parallel. However, only one of the character generators receives row data at a particular time. Therefore, only the stage which receives both row and column data is enabled. For example, if column 2 is encoded by the plug-in, the five Character Generators are enabled so that either a 1, <, μ, V or an N can be produced. However, if at the same time row 4 has also been encoded by the plug-in, only the Prefix Character Generator U1253 will produce an output to result in a μ displayed on the screen. This integrated circuit provides current outputs to the Format Generator stage which produce the selected character on the CRT. In a similar manner, any of the 50 characters shown in the Character Selection Matrix can be displayed by correct addressing of the row and column.

Decimal Point Logic and Character Position Counter

The Decimal Point Logic and Character Position Counter stage U1260 performs two functions. The first function is to produce a staircase current which is added to the X (horizontal) signal to space the characters horizontally on the CRT. After each character is generated, the negative-going edge of the Ready signal at pin 5 advances the Character Position Counter. This produces a current step output at pin 3 which, when added to the X signal, causes the next character to be produced one character space to the right. This stage can also be advanced when a Space instruction is encoded by the plug-in unit so that a space is left between the displayed characters on the CRT. Row 10 information from the Row Decoder stage is connected to pin 4 of U1260 through R1265. When row 10 and column 0 are encoded, the output of this stage advances one step to move the next character another space to the right. However, under this condition, no display is produced on the CRT during this time-slot.

Time-slot pulses 1, 2 and 3 are also connected to pin 4 of U1260 through VR1261, and VR1262 respectively and R1260, R1265. This configuration adds a space to the displayed word during time-slots 1, 2 and 3 even if information is not encoded for display during these time-slots. With this feature, the information which is displayed during time-slot 4 (1-2-5 data) always starts in the fourth character position whether data has been displayed in the previous time-slots or not. Therefore, the resultant CRT display does not shift position as normal/invert or cal/uncal information is encoded by the plug-in. The Word Trigger pulse connected to pin 8 of U1260 through C1267 returns the Character Position Counter to the first character position at the end of each word.

The Decimal Point Logic portion of this stage allows decimal points to be added to the CRT display as encoded by the plug-in units. When row 7 is encoded in coincidence with columns 3 through 7 (usually encoded during time-slot 1), a decimal point is placed at one of the five locations on the CRT identified in row 7 of the Character Selection Matrix (Fig. 3-31). This instruction refers to the decimal point location in relation to the total number of characters that can be displayed on the CRT (see Fig. 3-42). For example, if column 3 and row 7 are encoded during time-slot 1, the system is instructed to place a decimal point in location #3. As shown in Fig. 3-42, this displays a decimal point before the third character that can be displayed on the CRT (first three time-slots produce a space whether data is encoded or not; see previous paragraph). The simultaneous application of row 7 data to the Y-input of the

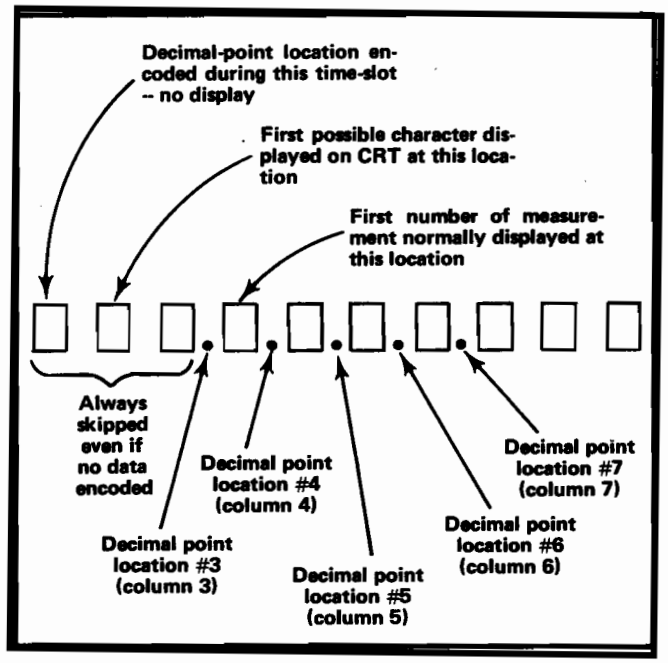


Fig. 3-42. Readout word relating 10 possible character locations to the decimal point instructions that can be encoded, and the resultant CRT display.

Format Generator stage through R1269 raises the decimal point so it appears between the displayed characters.

When decimal-point data is encoded, the CRT is unblanked so a readout display is presented. However, since row 7 does not activate any of the five Character Generators, the CRT beam is not deflected but instead remains in a fixed position to display a decimal point between the characters along the bottom line of the readout word. After the decimal point is produced in the addressed location, the CRT beam returns to the location indicated by the Character Position Counter to produce the remainder of the display.

Format Generator

The X- and Y-deflection signals produced by the Character Generator stage, are connected to pins 2 and 7 respectively of the Format Generator stage U1270. The Channel Address Code from the Channel Counter stage is also connected to pins 1, 8 and 15 of this stage. The Channel Address Code adds current to the X and Y signals to deflect the CRT beam to the area of the CRT which is associated with the plug-in channel that originated the information (see Fig. 3-30). The Channel Address Code and the resultant word positions are shown in Table 3-4. In addition, the character position current from the Decimal Point Logic and Character Position stage is added to the X (horizontal) input signal to space the characters horizontally on the CRT (see previous discussion). The Ready signal at pin 13 (coincident with Vertical/Horizontal OFF Command) activates this stage so it can produce the output from the Readout System.

Y-Output Amplifier

The Y-output signal at pin 6 of U1270 is connected to the Y-Output Amplifier Q1284-Q1288. This stage provides a low impedance load for the Format Generator while providing isolation between the Readout System and the Vertical Amplifier. The Vertical Separation adjustment R1285 changes the gain of this stage to control the vertical separation between the words displayed at the top and bottom of the graticule area.

TABLE 3-4

Channel Address Code to Format Generator Stage

Pin 7 U1232	Pin 7 U1231	Pin 5 U1230	Channel Displayed
LO	LO	HI	Channel 1 Left Vertical
LO	LO	LO	Channel 2 Left Vertical
LO	HI	HI	Channel 1 Right Vertical
LO	HI	LO	Channel 2 Right Vertical
HI	LO	HI	Channel 1 Horizontal
HI	LO	LO	Channel 2 Horizontal
HI	HI	HI	Channel 1 Unused
HI	HI	LO	Channel 2 Unused

X-Output Amplifier

The X-Output Amplifier Q1274-Q1278 operates similarly to the Y-Output Amplifier to provide the Horizontal deflection from the readout signal available at pin 4 of U1270. The gain of this stage is fixed by the values of the resistors in the circuit.

Display Sequence

Fig. 3-43 shows a flow chart for the Readout System. This chart illustrates the sequence of events which occurs in the Readout System each time a character is generated and displayed on the CRT.

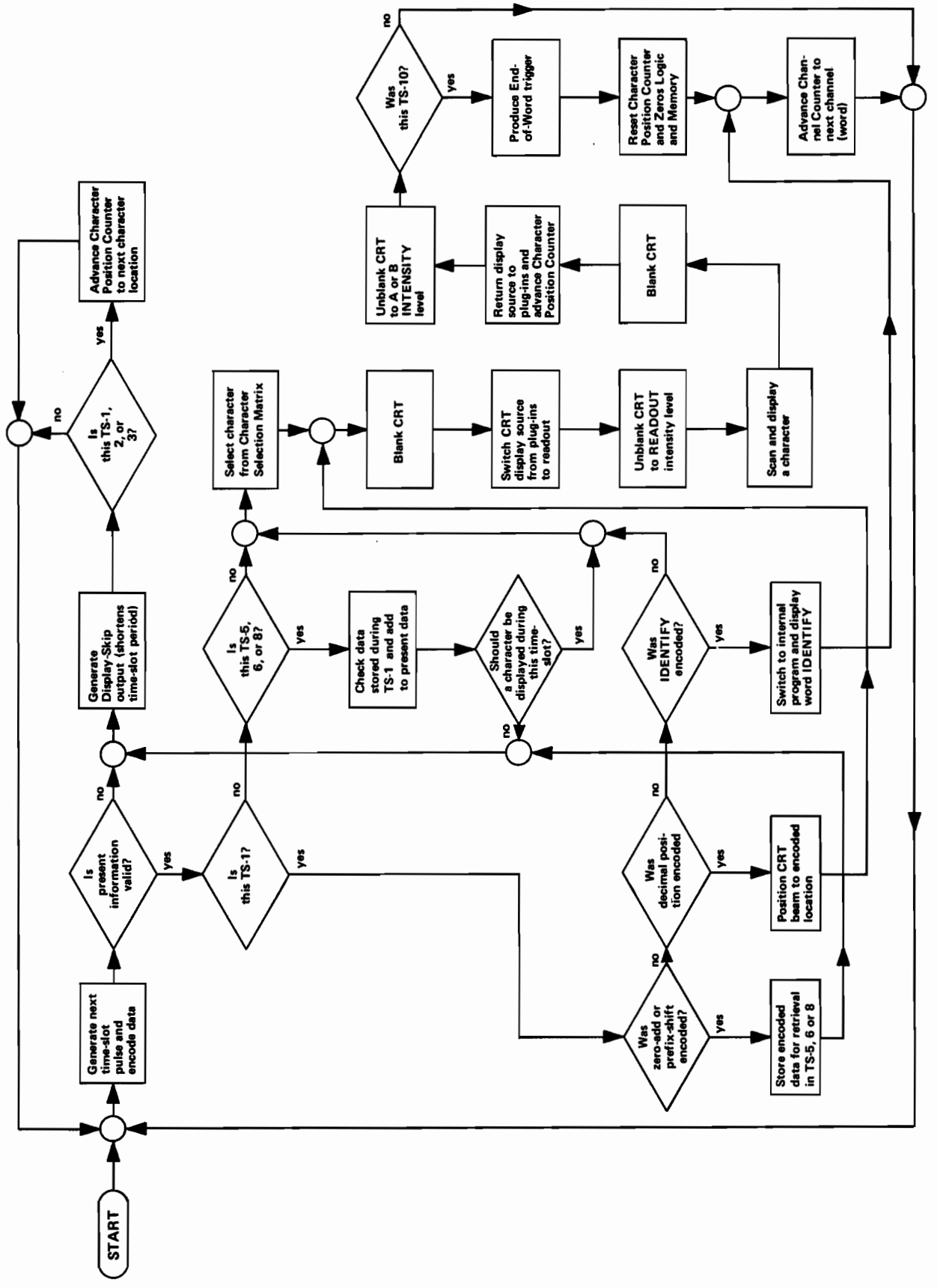


Fig. 3-43. Flow chart for character generation by the Readout System.